



Energy band alignment of atomic layer deposited HfO₂ on epitaxial (110)Ge grown by molecular beam epitaxy

M. K. Hudait, Y. Zhu, D. Maurya, and S. Priya

Citation: [Applied Physics Letters](#) **102**, 093109 (2013); doi: 10.1063/1.4794838

View online: <http://dx.doi.org/10.1063/1.4794838>

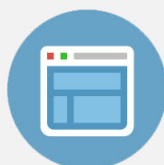
View Table of Contents: <http://scitation.aip.org/content/aip/journal/apl/102/9?ver=pdfcov>

Published by the [AIP Publishing](#)

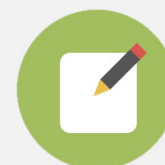


Re-register for Table of Content Alerts

Create a profile.



Sign up today!



Energy band alignment of atomic layer deposited HfO₂ on epitaxial (110)Ge grown by molecular beam epitaxy

M. K. Hudait,^{1,a)} Y. Zhu,¹ D. Maurya,² and S. Priya²

¹Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, Virginia 24061, USA

²Center for Energy Harvesting Materials and Systems (CEHMS), Virginia Tech, Blacksburg, Virginia 24061, USA

(Received 4 December 2012; accepted 25 February 2013; published online 6 March 2013)

The band alignment properties of atomic layer HfO₂ film deposited on epitaxial (110)Ge, grown by molecular beam epitaxy, was investigated using x-ray photoelectron spectroscopy. The cross-sectional transmission electron microscopy exhibited a sharp interface between the (110)Ge epilayer and the HfO₂ film. The measured valence band offset value of HfO₂ relative to (110)Ge was 2.28 ± 0.05 eV. The extracted conduction band offset value was 2.66 ± 0.1 eV using the bandgaps of HfO₂ of 5.61 eV and Ge bandgap of 0.67 eV. These band offset parameters and the interface chemical properties of HfO₂/(110)Ge system are of tremendous importance for the design of future high hole mobility and low-power Ge-based metal-oxide transistor devices.

© 2013 American Institute of Physics. [<http://dx.doi.org/10.1063/1.4794838>]

With the scaling of Si complementary metal-oxide semiconductor (CMOS) technology, each transistor has become smaller and faster leading to unprecedented increase in microprocessor performance. In future, transistor scaling will require the introduction of high mobility channel materials, including III-V and Ge, and device architectures. According to the International Technology Roadmap for Semiconductors,¹ channel materials with superior transport properties, high- κ gate dielectric, and multi-gate transistor configuration in a CMOS logic device under 10 nm regime are required to achieve further increase in transistor drive current and resultant ULSI performance improvement. In recent years, low bandgap high electron mobility III-V compounds coupled with high- κ gate dielectrics²⁻⁴ have been demonstrated in n-channel device configuration operating at 0.5 V;⁵⁻⁸ however, the demonstration of a high hole mobility p-channel device configuration along with high- κ dielectric is mandatory to realize energy-efficient CMOS logic. For this reason, the enhancement of carrier transport properties in the channel using high hole mobility channel materials,⁹⁻¹¹ different surface orientations to improve the carrier mobility,^{12,13} and optimal channel direction¹⁴⁻¹⁶ have been proposed for further enhancement of CMOS devices. Very recently, it has been demonstrated that the carrier mobility of Ge can be enhanced by utilizing a Ge channel with different orientations; the carrier mobility was expected to be high in (111)Ge for electrons¹⁷ and in (110)Ge for holes.¹⁸ In fact, transistors fabricated on (110)Ge substrates exhibited higher hole mobilities of ~ 650 cm²/Vs along $\langle 110 \rangle$ direction.¹⁴ Dissanayake *et al.*¹⁵ have reported that the hole mobility of (110)Ge channel orientation along the $\langle 110 \rangle$ direction exhibited $2.3\times$ higher hole mobility compared with the (100)Ge surface and thus have a potential advantage for p-channel field-effect device operation.

Significant research on the high- κ gate dielectrics HfO₂,^{18,19} ZrO₂,²⁰ Al₂O₃,^{21,22} Y₂O₃,²³ Lu₂O₃,²⁴ CeO₂,²⁵ rare

earth oxides,²⁶ as well as germanium-oxynitride²⁷ have been conducted on the (100)Ge metal-oxide semiconductor devices, hoping that the integration of high- κ dielectrics with Ge will not only allow continued scaling of transistors but will also provide higher low-field intrinsic carrier mobility for improving device speed.⁹ Although excellent device performances were achieved using high- κ gate dielectrics on (100)Ge and oxide/(100)Ge band alignment properties, little attention has been devoted towards the integration of high- κ gate dielectrics on the (110)Ge and the associated energy band alignment at the interface. High-quality dielectric on (110)Ge interface is essential to eliminate the formation of high density intrinsic defects with energy levels in the semiconductor band gap²⁸ due to poor quality native oxides, resulting in Fermi level pinning²⁹ at the oxide-semiconductor interface. Furthermore, the selected high- κ material should have valence and conduction band discontinuities larger than 1 eV relative to the semiconductor channel material³⁰ to act as a barrier for both holes and electrons.

In this letter, we report on the band alignment properties between the atomic layer HfO₂ deposited on top of the epitaxial Ge grown on (110)GaAs substrate using solid source molecular beam epitaxy (MBE). The investigations were conducted by using x-ray photoelectron spectroscopy (XPS). The experimental results from this study are the first step towards achieving high-performance Ge channel material on (110)GaAs for p-channel field-effect transistor, which can be ultimately heterogeneously integrated to Si substrate through a III-V buffer layer for the realization of ultra-low power and high-speed CMOS logic.

The undoped epitaxial 60-80 nm thick Ge layers were *in-situ* growth process on (110) epi-ready GaAs substrates using separate solid source MBE growth chambers for Ge and III-V materials, connected *via* ultra-high vacuum transfer chamber. Substrate oxide desorption was done at ~ 580 °C under an arsenic overpressure of $\sim 1 \times 10^{-5}$ Torr in a III-V MBE chamber. An initial 0.2 μ m undoped GaAs buffer layer was then deposited on (110)GaAs substrate to

^{a)}Author to whom correspondence should be addressed. Electronic mail: mantu.hudait@vt.edu. Tel.: (540) 231-6663. Fax: (540) 231-3362.

generate a smooth surface at 550 °C under a stabilized As₂ flux prior to transferring (110)GaAs wafer to the Ge MBE chamber for Ge epilayer growth. The growth temperature of Ge was ~400 °C. The detail of the growth procedure is reported elsewhere.^{31,32} The 1 nm and 5 nm HfO₂ films were grown by atomic layer deposition (ALD) in a Cambridge NanoTech system on epitaxial (110)Ge using a Tetrakis(dimethylamino)hafnium compound as Hf precursor and H₂O as the oxygen source. During the HfO₂ growth, the surface temperature of (110)Ge film and Hf precursor temperature was kept constant at 250 °C and 75 °C, respectively. Epitaxial (110)Ge layers were cleaned using NH₄OH:H₂O₂:H₂O (2:1:1000 volume ratio) for 5 s prior to loading to ALD chamber for HfO₂ deposition. The band alignment of HfO₂/(110)Ge structures was investigated using a PHI Quantera SXM XPS system with a monochromated Al-K α (energy of 1486.7 eV) x-ray source.³³ The Ge 3d and Hf 4f_{7/2} core level (CL) binding energy spectra as well as Ge and Hf valence band binding energy spectra were collected with a pass energy of 26 eV and an exit angle of 45°. The binding energy was corrected by adjusting the carbon (C) 1s CL peak position to 285.0 eV for each sample surface. Curve fitting was done by the CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background. The CL energy position was defined to be the center of the peak width at the half of the peak height (i.e., full width at half maximum). The bandgap of the HfO₂ film,^{18,19} the core level, and valence electrons emitted from the film determined from the XPS measurement will allow to determine the valence band offset of HfO₂ relative to the (110)Ge film by the method described in Ref. 32. The error bar we defined in this paper is due to the scatter of valence band spectra during the fitting of valence band maximum (VBM) position and considering the linearity and stability of the energy scale of the XPS binding energy spectrum.

Figures 1(a) and 1(b) show cross-sectional transmission electron microscopy (TEM) micrograph of HfO₂/Ge/(110)GaAs structure and high-resolution TEM micrograph of HfO₂/(110)Ge interface, respectively. These TEM micrographs show a sharp interface between the Ge epilayer and the HfO₂ film as well as Ge and (110)GaAs substrate. The HfO₂ thickness measured by TEM is ~5 nm, consistent with the ALD deposited thickness. From Fig. 1(b), one can find that there is no interfacial layer formed during the deposition of HfO₂ on (110)Ge layer which implies that the removal of interfacial oxide can be easily obtained on (110)Ge and thus have a potential advantage of HfO₂/(110)Ge for high-hole mobility p-channel transistor application. On contrary, a thinner interfacial layer consists of a mixture of GeO and GeO₂, as reported by several researchers,³⁴ on (100)Ge layer.³⁵ On one hand, removal of this unwanted layer is essential due to the lower dielectric constant of GeO₂ ($\kappa = 3.0\text{--}3.8$)³⁴ as well as poor chemical and thermal stability due to dissolution in acidic, alkaline solutions, and by warm water. Further, the elimination of this poor quality unstable oxide layer is desired to obtain better electrical transport characteristics namely, equivalent oxide layer thickness, capacitance-voltage hysteresis, and frequency dispersion. The relatively unstable nature of Ge oxide implies that the removal of unwanted interfacial

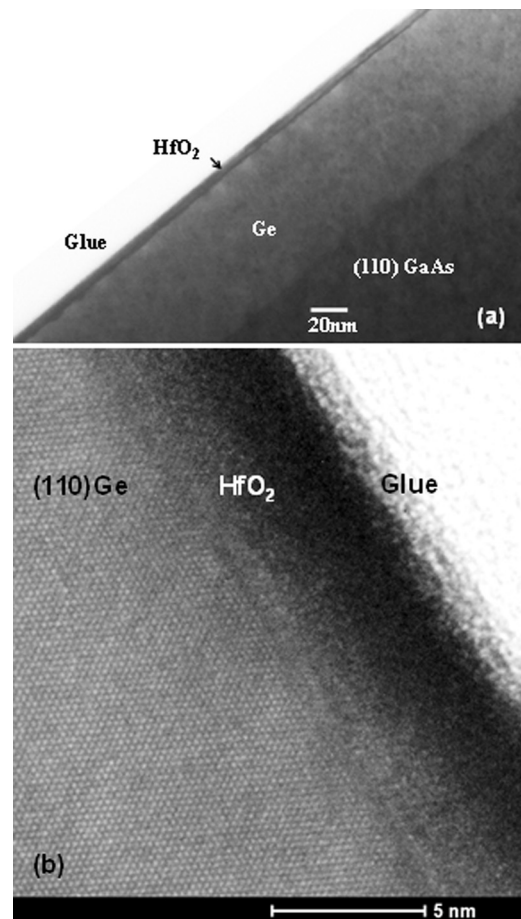


FIG. 1. (a) Cross-sectional TEM micrograph of HfO₂ layer deposited on epitaxial Ge grown on (110) GaAs substrate. (b) High-resolution TEM micrograph at the HfO₂/(110)Ge interface exhibits the absence of interfacial layer. The sharp interface between HfO₂ and Ge as well as Ge and (110) GaAs was achieved.

oxide can be easily achieved and thus have a potential advantage of high- κ on Ge system.³⁴

As discussed earlier, the energy band alignment at the high- κ /Ge interface is of great importance, since the sufficient barriers for electron and hole are needed to suppress the tunneling leakage current. Also, the reported hole mobility is higher on (110)Ge substrate, and the measured valence and conduction band offset values of HfO₂ relative to (110)Ge will provide further insights into the predicted electrical transport mechanisms in the predefined Ge channel layer thickness grown on a large bandgap GaAs barrier layer. The valence band offset ΔE_v at the HfO₂/(110)Ge was determined using XPS system and angle integrated photoelectron energy distribution curves for the VBM. Using these methods, Ge 3d, Hf 4f_{7/2} core levels spectra were recorded. The peak separation of Ge 3d_{5/2} and 3d_{3/2} due to spin-orbit splitting is too small to be separated. The binding energy was corrected by adjusting the C 1s core-level peak position to 285.0 eV for each sample surface. XPS spectra were recorded from the following 3 samples: (i) (110)Ge epitaxial layer, (ii) 1 nm HfO₂ on (110)Ge layer, and (iii) 5 nm thick HfO₂ film on (110)Ge. Figures 2(a) and 2(b) show the Ge 3d core level (E_{Ge3d}^{Ge}) spectrum of the (110)Ge film and VBM (E_{VBM}^{Ge}) (shown in inset) as well as Hf 4d_{7/2} core level ($E_{Hf4f_{7/2}}^{Hf}$) spectrum of 5 nm HfO₂ film and VBM (E_{VBM}^{Hf}) (shown in inset), respectively.

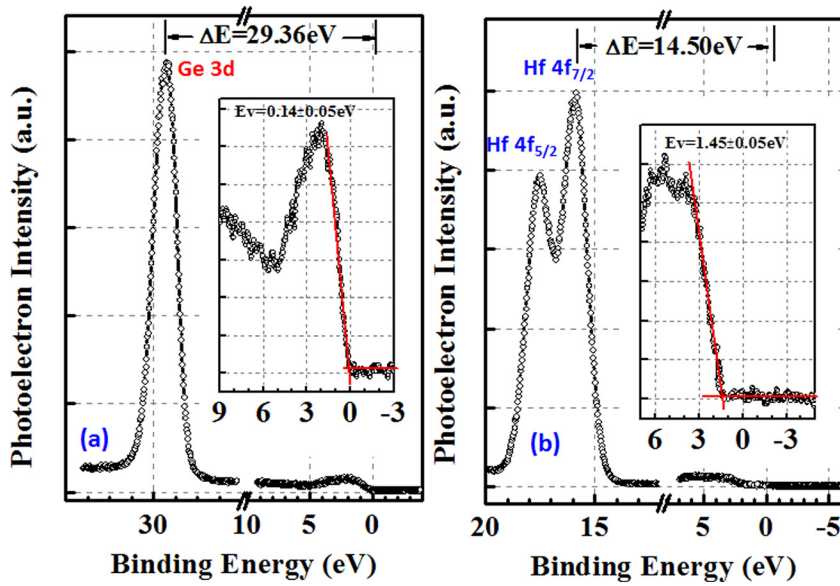


FIG. 2. XPS spectra of (a) Ge 3d core level (E_{Ge3d}^{Ge}) and valence band maximum, VBM (E_{VBM}^{Ge}) of (110) Ge film; (b) Hf 4d_{7/2} core level ($E_{Hf4f_{7/2}}^{Hf}$) spectrum and VBM (E_{VBM}^{Hf}) of 5 nm HfO₂ film, respectively.

Figure 3 shows the Ge 3d core level (E_{Ge3d}^{Ge}) and Hf 4d_{7/2} core level ($E_{Hf4f_{7/2}}^{Hf}$) spectrum of 1 nm HfO₂ on (110) Ge interface, respectively. The valence band offset, ΔE_v for a HfO₂/(110)Ge interface, was determined from the following equation³⁶ using core level spectra

$$\Delta E_v = (E_{Ge3d}^{Ge} - E_{VBM}^{Ge})^{Ge} - (E_{Hf4f_{7/2}}^{Hf} - E_{VBM}^{Hf})^{5nmHfO_2} - (E_{Ge3d}^{Ge} - E_{Hf4f_{7/2}}^{Hf})^{1nmHfO_2/Ge\ interface}. \quad (1)$$

We have selected Hf 4f_{7/2} core level spectra rather than Hf 4f_{5/2} since the measured binding energy separation between the Hf 4f_{7/2} and Hf 4f_{5/2} peaks is fixed to 1.7 eV from each measurement. As a result, the band offset result would not change if we select Hf 4f_{5/2} as the core level binding energy peak. Finally, the conduction band offset, ΔE_c for a HfO₂/(110)Ge interface is determined from the following equation:

$$\Delta E_c = E_g^{HfO_2} - E_g^{Ge} - \Delta E_v, \quad (2)$$

where $E_g^{HfO_2}$ and E_g^{Ge} are the bandgaps of HfO₂ and Ge, respectively.

The position of the Ge 3d peak centroid from the XPS measurement was found to be 30.05 ± 0.005 eV as shown in Fig. 2(a). This value was obtained by measuring the center of the peak width at half of the peak height after Shirley background subtraction.¹⁹ The VBM for (110)Ge was determined as the intersection between the linear fits of the background and the linear portion of the VB leading edge,¹⁹ as shown in inset of Fig. 2(a). The energy difference between the Ge 3d centroid and the (110)Ge VBM was measured to be 29.36 ± 0.05 eV, providing excellent agreement with the results of HfO₂ on (100) Ge.^{18,19} Similarly, the energy difference between the Hf 4f_{7/2} centroid and the VBM was found to be 14.50 ± 0.05 eV for the 5 nm-thick HfO₂ film. For the 1 nm HfO₂ film on (110)Ge, the energy difference between the Ge 3d centroid and the Hf 4f_{7/2} core lines was determined to be 12.58 ± 0.05 eV. Using these measured data and Eq. (1), the measured value of ΔE_v for the HfO₂/(110)Ge

interface is 2.28 ± 0.05 eV and this value is lower by ~ 0.6 eV than on (100)Ge substrate. To explain the observed differences in the ΔE_v values for the HfO₂ on (110)Ge and HfO₂ on (100)Ge, reflection high energy electron diffraction (RHEED) patterns were recorded from the epitaxial (110)Ge and (100)Ge layers and also from the starting GaAs substrates. The RHEED patterns from the surface of the Ge epilayer were recorded after transferring the Ge epilayer from the Ge MBE chamber to the III-V MBE chamber. These RHEED patterns shed light on the reconstruction of epitaxial Ge layer grown on (100)GaAs and (110)GaAs substrates and thus the resulting band offset values of HfO₂ on (110)Ge and (100)Ge. A (100)Ge layer was deposited on a reconstructed (2×4) GaAs surface with a surface layer being mainly arsenic exhibited (2×2) surface reconstruction of Ge layer on (100)GaAs.³² On the other hand, the (110)GaAs surface exhibited a (1×1) RHEED pattern,³² consistent with the other researchers and the deposited epitaxial Ge film on such

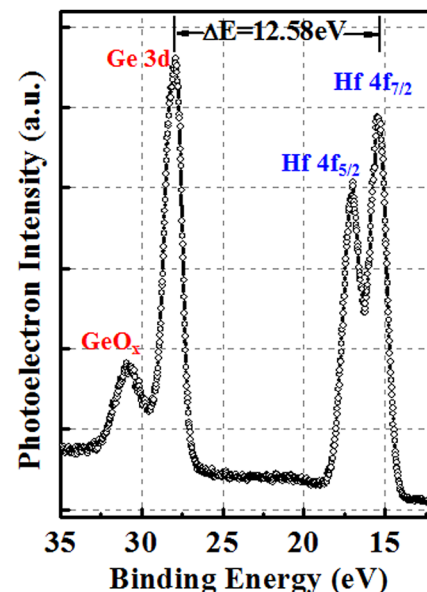


FIG. 3. XPS spectra of Ge 3d (E_{Ge3d}^{Ge}) and Hf 4d_{7/2} core level ($E_{Hf4f_{7/2}}^{Hf}$) spectrum of 1 nm thin HfO₂ film/(110)Ge interface.

surface orientated GaAs showed a streaky (3×4) RHEED pattern.³² As a result of different in surface reconstruction of Ge, the deposited band offset of HfO_2 on crystallographic oriented epitaxial Ge would exhibit different values of band offset. In fact, it has been reported that band offsets can depend on substrate orientation, overlayer crystallinity, surface reconstruction, deposition temperature, deposition rate, microscopic interface dipole, and interdiffusion or reactivity.³⁷ Furthermore, the absence of interfacial layer at the HfO_2 /(110)Ge interface, as shown in Fig. 1(b) compared to the reported $\text{HfO}_2/\text{GeO}_x$ /(100)Ge,³⁵ indicates the clear difference in the interface properties and thus have a different in the band alignment properties of the HfO_2 deposited in crystallographic oriented Ge layers. The conduction band offset, ΔE_C for the HfO_2 on (110)Ge is calculated to be 2.66 ± 0.1 eV, similar to the band offset of HfO_2 on (100)Ge substrates,¹⁸ using Eq. (2), measured ΔE_v , bandgap 0.67 eV of Ge and reported bandgap 5.61 eV of HfO_2 .^{18,19} These results suggest that the barrier height of HfO_2 /(110)Ge is enough to obtain very low leakage current using high- κ gate dielectrics on (110)Ge.

Figure 4 shows the band alignment diagram of the HfO_2 /(110) Ge heterojunction based on the present XPS results. The valence band and conduction band offsets are well above 1 eV, as needed for blocking electrons and holes³⁰ for carrier transport in the fabricated Ge metal-oxide semiconductor field effect transistors. The transport properties will strongly depend on the interface states between the high- κ and the (110)Ge layer. The band alignment of Ge on (110)GaAs substrate is included from Ref. 32. Thus, the measured band offset values on (110)Ge can provide a promising path for p-channel Ge field effect devices for low-power and high-speed computing platforms.

In summary, the experimental study of the band offset properties of HfO_2 on epitaxial (110)Ge grown by MBE was investigated using XPS. Cross-sectional TEM micrograph shows a sharp interface between the (110)Ge epilayer and the HfO_2 film. XPS results showed the valence band offset of 2.28 ± 0.05 eV at the HfO_2 /(110)Ge heterointerface. The conduction band offset is calculated to be 2.66 ± 0.1 eV using the bandgap of HfO_2 of 5.61 eV and with the well-known

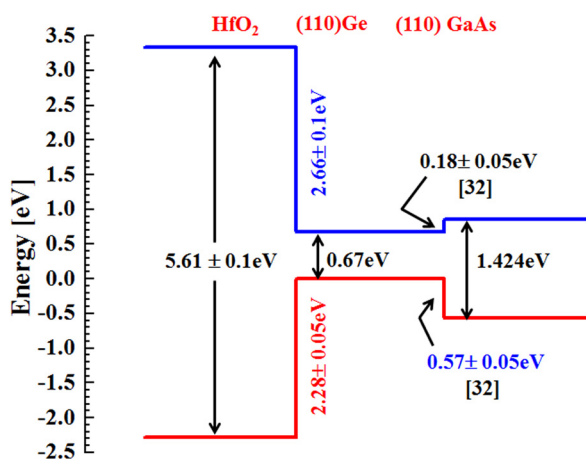


FIG. 4. Energy-band diagram of the HfO_2 /Ge heterojunction obtained from XPS measurements. The Ge/(110) GaAs band offset is included from Ref. 32.

Ge bandgap of 0.67 eV. These band offset parameters and the interface chemical properties of the HfO_2 /(110)Ge system are vital for Ge-based p-channel metal-oxide transistor device design.

This work is supported in part by Intel Corporation.

- ¹International Technology Roadmap for Semiconductors (ITRS), *Process Integration, Devices, and Structures (PIDS)*, 2011 edition (2011).
- ²M. Radosavljevic, B. Chu-Kung, S. Corcoran, M. K. Hudait, G. Dewey, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, W. Rachmady, U. Shah, and R. Chau, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2009), p. 319.
- ³Y. Sun, in *International Symposium on VLSI Technology, Systems, and Applications* (IEEE, New York, 2010), p. 149.
- ⁴A. Ali, H. Madan, M. J. Barth, M. J. Hollander, J. B. Boos, B. R. Bennett, and S. Datta, in *International Symposium on VLSI Technology, Systems, and Applications* (IEEE, New York, 2012), p. 181.
- ⁵M. K. Hudait, *ECS Trans.* **45**, 581 (2012).
- ⁶M. K. Hudait, G. Dewey, S. Datta, J. M. Fastenau, J. Kavalieros, W. K. Liu, D. Lubyshev, R. Pillarisetty, W. Rachmady, M. Radosavljevic, T. Rakshit, and R. Chau, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2007), p. 625.
- ⁷L. Ming, L. Haiou, T. Chak Wah, and L. Kei May, *IEEE Electron. Device Lett.* **33**, 498 (2012).
- ⁸M. Radosavljevic, T. Ashley, A. Andreev, S. D. Coomber, G. Dewey, M. T. Emeny, M. Fearn, D. G. Hayes, K. P. Hilton, M. K. Hudait, R. Jefferies, T. Martin, R. Pillarisetty, W. Rachmady, T. Rakshit, S. J. Smith, M. J. Uren, D. J. Wallis, P. J. Wilding, and R. Chau, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2008), p. 727.
- ⁹R. Pillarisetty, B. Chu-Kung, S. Corcoran, G. Dewey, J. Kavalieros, H. Kennel, R. Kotlyar, V. Le, D. Lionberger, M. Metz, N. Mukherjee, J. Nah, W. Rachmady, M. Radosavljevic, U. Shah, S. Taft, H. Then, N. Zelick, and R. Chau, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2010), p. 150.
- ¹⁰A. Nainani, S. Raghunathan, D. Witte, M. Kobayashi, T. Irisawa, T. Krishnamohan, K. Saraswat, B. R. Bennett, M. G. Ancona, and J. B. Boos, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2009), p. 857.
- ¹¹J. B. Boos, B. R. Bennett, N. A. Papanicolaou, M. G. Ancona, J. G. Champlain, Y. C. Chou, M. D. Lange, J. M. Yang, R. Bass, D. Park, and B. V. Shanabrook, *IEICE Trans. Electron.* **E91-C**, 1050 (2008).
- ¹²Y. Sun, S. E. Thompson, and T. Nishida, *Strain Effect in Semiconductors: Theory and Device Applications*, 1st ed. (Springer, 2009).
- ¹³M. V. Fischetti and S. E. Laux, *J. Appl. Phys.* **80**, 2234 (1996).
- ¹⁴B.-F. Hsieh and S.-T. Chang, *Solid State Electron.* **60**, 37 (2011).
- ¹⁵S. Dissanayake, Y. Zhao, S. Sugahara, M. Takenaka, and S. Takaghi, *J. Appl. Phys.* **109**, 033709 (2011).
- ¹⁶K. Minami, Y. Nakamura, S. Yamasaka, O. Yoshitake, J. Kikkawa, K. Izunome, and A. Sakai, *Thin Solid Films* **520**, 3232 (2012).
- ¹⁷T. Krishnamohan, D. Kim, T. V. Dinh, A. Pham, B. Meinerzhagen, C. Jungemann, and K. Saraswat, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, New York, 2008), p. 899.
- ¹⁸J. H. Choi, Y. Mao, and J. P. Chang, *Mater. Sci. Eng. R.* **72**, 97 (2011).
- ¹⁹M. Perego, G. Seguini, and M. Fanciulli, *J. Appl. Phys.* **100**, 093718 (2006).
- ²⁰S. J. Wang, A. C. H. Huan, Y. L. Foo, J. W. Chai, J. S. Pan, Q. Li, Y. F. Dong, Y. P. Feng, and C. K. Ong, *Appl. Phys. Lett.* **85**, 4418 (2004).
- ²¹H. Seo, F. Bellenger, K. B. Chung, M. Houssa, M. Meuris, M. Heyns, and G. Lucovsky, *J. Appl. Phys.* **106**, 044909 (2009).
- ²²S. Swaminathan, Y. Sun, P. Pianetta, and P. C. McIntyre, *J. Appl. Phys.* **110**, 094105 (2011).
- ²³S. Y. Chiam, W. K. Chim, C. Pi, A. C. H. Huan, S. J. Wang, J. S. Pan, S. Turner, and J. Zhang, *J. Appl. Phys.* **103**, 083702 (2008).
- ²⁴M. Perego, G. Seguini, G. Scarel, and M. Fanciulli, *Surf. Interface Anal.* **38**, 494 (2006).
- ²⁵M. S. Rahman, E. K. Evangelou, A. Dimoulas, G. Mavrou, and S. Galata, *J. Appl. Phys.* **103**, 064514 (2008).
- ²⁶M. S. Rahman, E. K. Evangelou, N. Konofaos, and A. Dimoulas, *J. Appl. Phys.* **112**, 094501 (2012).

- ²⁷H. Shang, H. Okorn-Schimdt, J. Ott, P. Kozlowski, E. C. Jones, H.-S. P. Wong, and W. Hanesch, *IEEE Electron Device Lett.* **24**, 242 (2003).
- ²⁸W. E. Spicer, I. Lindau, P. Skeath, C. Y. Su, and P. Chye, *Phys. Rev. Lett.* **44**, 420 (1980).
- ²⁹P. Chiaradia, M. Fanfoni, P. Nataletti, P. De Padova, L. J. Brillson, M. L. Slade, R. E. Viturro, D. Kilday, and G. Margaritondo, *Phys. Rev. B* **39**, 5128 (1989).
- ³⁰J. Robertson and B. Falabretti, *J. Appl. Phys.* **100**, 014111 (2006).
- ³¹M. K. Hudait, Y. Zhu, N. Jain, S. Vijayaraghavan, A. Saha, T. Merritt, and G. A. Khodaparast, *J. Vac. Sci. Technol. B* **30**, 051205(2012).
- ³²M. K. Hudait, Y. Zhu, N. Jain, and J. L. Hunter, Jr., *J. Vac. Sci. Technol. B* **31**, 011206 (2013).
- ³³J. Schweppe, R. D. Deslattes, T. Mooney, and C. J. Powell, *J. Electron. Spectrosc. Relat. Phenom.* **67**, 463 (1994).
- ³⁴S. J. Lee, C. Zhu, and D. L. Kwong in *Advanced Gate Stacks for High-Mobility Semiconductors*, edited by A. Dimoulas, E. Gusev, P. C. McIntyre, and M. Heyns (Springer, Berlin, 2007).
- ³⁵S. V. Elshocht, B. Brijs, M. Caymax, T. Conard, T. Chiarella, S. D. Gendt, B. D. Jaeger, S. Kubicek, M. Meuris, B. Onsia, O. Richard, I. Teerlinck, J. V. Steenbergen, C. Zhao, and M. Heyns, *Appl. Phys. Lett.* **85**, 3824 (2004).
- ³⁶E. Kraut, R. Grant, J. Waldrop, and S. Kowalczyk, *Phys. Rev. Lett.* **44**, 1620 (1980).
- ³⁷L. J. Brillson, *Surfaces and Interfaces of Electronic Materials* (Wiley-VCH, Germany, 2010).