High Power Density and High Temperature

Converter Design for Transportation Applications

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Abstract

The continual development of high-power-density power electronic converters is driven particularly by modern transportation applications like electrical vehicles and more electric aircraft where the space and carrier capability is limited. However, there are several challenges related to transportation applications such as fault tolerance for safety concern, high temperature operation in extreme environments and more strict electromagnetic compatibility requirement. These challenges will increase difficulties for more electrical system adoption in the transportation applications.

In this dissertation, comprehensive methodologies including more efficient energy storage solution, better power electronics devices capability, better packaging performance and more compact EMI filter design are analyzed and proposed for the goal of high power density converter design in transportation applications.

The dissertation is divided into five sections. Chapter 1 describes the motivation and objective of this research. After examining the surveyed results from the literature, the challenges in this area of research are addressed. Chapter 2 presents the energy storage capacitor size reduction by using an active ripple energy storage method in fault tolerance transportation applications. With the minimum ripple energy storage requirement, the feasibility of the capacitor volume reduction is verified. Then, a bidirectional buck-boost converter as the ripple energy storage circuit is proposed which can effectively reduce the capacitor size. Meanwhile, the feed forward control method is implemented with the

active circuit. Chapter 3 demonstrates the high temperature converter design in transportation applications. A novel hybrid structure packaging method is proposed to utilize the benefits of both wirebond structure and planar structure. Detailed analysis was conducted for the hybrid structure packaging in terms of parasitic reduction and thermal reliability. Then, a detailed high temperature converter design procedure is proposed together with a multi-chip power module packaged in hybrid structure. The whole converter is capable of working in harsh environment. Chapter 4 shows a more compact EMI filter design procedure including both transfer gain and insertion gain analysis. With the transfer gain analysis, both the low frequency and high frequency attenuation requirement is considered and an optimum number of stages can be derived in terms of minimum volume. Since the EMI noise source and load impedance cannot be treated as ideal cases in the real applications, a frequency domain model based on the impedance measurement is utilized to provide EMI noise attenuation prediction. Mask impedance can then be employed to linearize the EMI noise source impedance. After this, the magnetic component near-field coupling phenomenon is studied. Displacement current influence to the near field distribution is discovered and analyzed in detail. Finally, Chapter 5 presents the summary and conclusions.

TO MY FAMILY

My Parents: Qindan Wang and Yanping Li

My Parents-in-law: Chengshu Zhang and Rongju Gao

My Wife: Le Zhang

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Chapter 1. Introduction

This chapter starts with an introduction to the motivation and objective of this research, the design of high power density and high temperature converter for transportation applications. After examining the surveyed results from the literature, the challenges in this area of research are addressed. Finally, the layout of the research dissertation is presented.

1.1 Motivation and Objective

With a recent emphasis on environmental concerns, there has been an increasing demand for lower fuel consumption in modern transportation applications such as vehicle, aviation and marine [1]. In addition, there is always the traditional demand for ever increasing power.

(a). Nissan's electrical vehicle: The Nissan Leaf (b). Boeing's more electrical aircraft: Boeing 787

Figure 1-1 Electrically intensive transportation applications

As shown in Figure 1-1, electrical power is utilized more and more in electric vehicle applications for propulsion purposes. Also, a greater degree of utilization for assistance purposes in aircraft applications is being realized than in previous aircraft generations. The benefits of the electrical vehicle compared with the traditional

vehicle are very clear since the electric vehicle has zero emissions. The less well known benefits of more electric aircraft are summarized as below:

Today the conventional civil aircraft is characterized by four different secondary power distribution systems: mechanical, hydraulic, pneumatic and electrical, as shown in Figure 1-2 [2]. The characteristics of all of these four different non-propulsive power systems are summarized in

Table **1-1**.

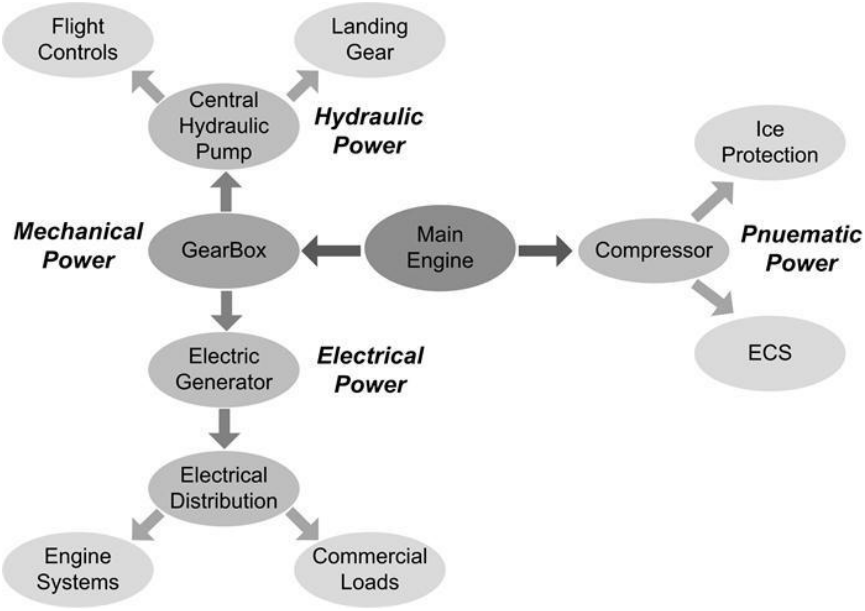


Figure 1-2 Schematic of a conventional power distribution system in aircraft application

Table 1-1 Summary of the four different secondary power system in an aircraft

Types	Source	Usage	Characteristics
Pneumatic Power	The engine's high-pressure compressors	The Environmental Control System (ECS) and supply hot air for the Wing-Anti-Icing (WAI)	Low efficiency, difficult leak detection.
Mechanical Power	The engine with mechanical gearboxes	Mechanical driven subsystems.	
Hydraulic	The central hydraulic	Actuation systems for primary and	Heavy and inflexible

Power	pump	secondary flight control; landing gear for deployment, retraction, braking, engine actuation, numerous ancillary systems	infrastructure (piping) and the potential leakage of dangerous and corrosive fluids.
Electrical Power	The main generator	Power for avionics, cabin and aircraft lighting, galleys and commercial loads.	Does not require a heavy infrastructure and is very flexible. Higher risk of fire(in the case of a short circuit)

As each system becomes more and more complex, the interactions between different pieces of equipment reduce the efficiency of the whole system. In order to reduce this complexity, and to improve the efficiency, power density and reliability, the aircraft manufacture trend is gravitating towards the More Electrical Aircraft (MEA) concept that is the wider adoption of electrical systems in preference to the others. The advantages of adoption of more electrical systems are not confined to only aircraft. Other transportation applications such as marine propulsion are also moving into this direction.

However, the challenges are enormous. Power electronics components and converters must operate in extreme environments, have minimal weight and provide reliability much greater than has hitherto been produced by industrial drives.

As mentioned above, adoption of more electrical systems will bring benefits to the whole system by reducing the total weight and increasing the whole system efficiency and power density. This will reduce fuel consumption while simultaneously reducing emissions.

For all the more electrical transportation applications such as vehicle [3, 4], aviation [5-8] and marine [9-11], higher power density electrical system design becomes the

key issue because of the limited space and carrier capability. However, besides the high power density, the transportation applications also share another common characteristic: harsh operating environments (especially high temperature) [12-18]. Figure 1-3 shows the environmental temperature distribution in some transportation applications. The harsh environments inherent in these applications introduce a new level of complexity in the design of the electrical system.

(a). Temperature distribution in electrical vehicle (b). Temperature distribution in JET engine

Figure 1-3 Environmental temperature distribution in transportation applications

Meanwhile, fault tolerance and redundancy are sometimes required for safety concerns in transportation applications such as aerospace. The fault tolerance capability will guarantee no single electrical fault may cause the system as a whole to stop functioning. The principal electromagnetic faults which may occur within the machine are [19]

- winding open-circuit;
- winding short-circuit (phase/phase);
- winding short-circuit at terminals;

Within the power converter the faults under consideration are as follows:

- power device open-circuit;
- power device short-circuit;
- dc link capacitor failure;

This fault tolerance can be achieved through combinations of partitioning and redundancy in the system [20-22]. A successful design approach involves a multiple-phase drive in which each phase may be regarded as a single module. The operation of any one module must have minimal impact upon the others, so that in the event of a module failing the others can continue to operate unaffected.

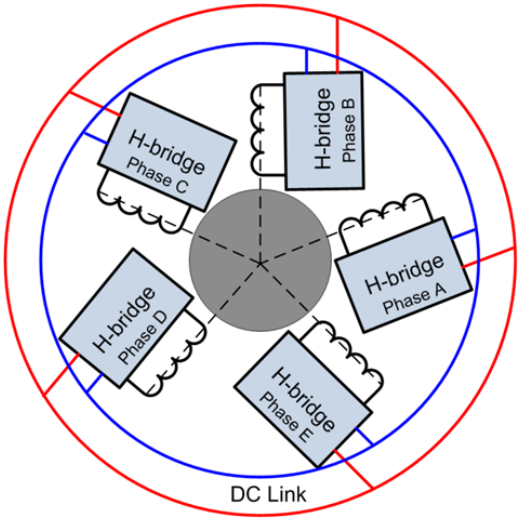
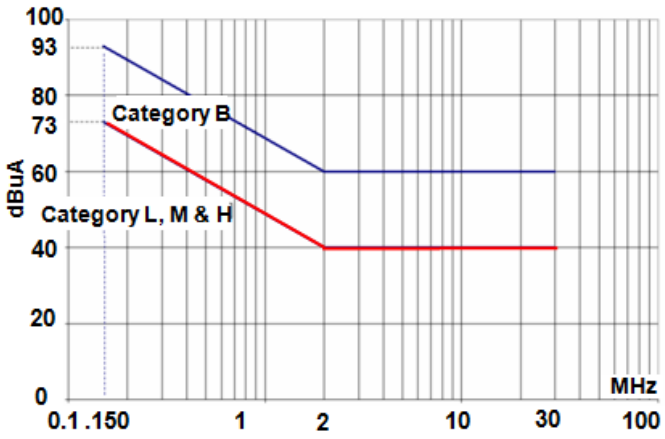


Figure 1-4 Fault-tolerant five-phase generator converter

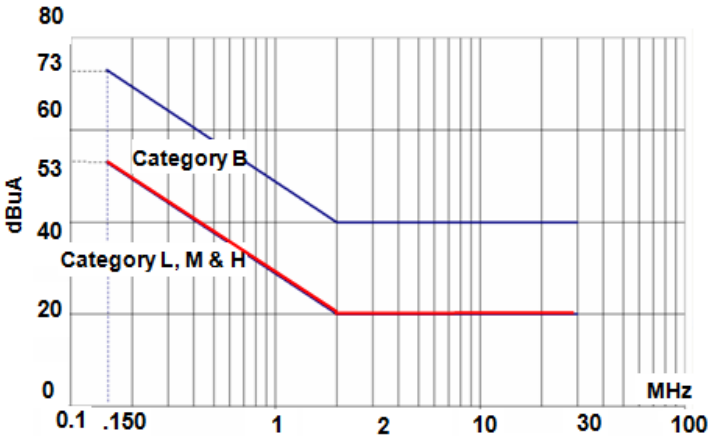
Figure 1-4 shows a fault-tolerant five-phase generator converter schematic. It consists of five separate H-bridge converters, each equipped with its own bank of DC-link capacitors. In the event of a single phase fault, the system level controller will modify the demand currents in the remaining phases to achieve the desired output power. Since reliability is an issue as important as weight in transportation applications, achieving higher power density electrical design while considering reliability becomes important.

In addition, more electrical aircraft applications will lead to an increase in electrical power consumption. The increased number of power electronic converters connected to an aircraft's electrical supply networks increases the harmonic levels [23]. However, for the power electronics converter designed for transportation applications, the conduction electromagnet interference (EMI) is a very important concern since the

conduction EMI will impair other electronics systems and therefore reduce the system reliability. This is especially true for aircraft systems. Reference [24] specifies the aircraft EMI standard from the Boeing DO-160, and the required standard is shown in Figure 1-5. However, adding an EMI filter to the converter will obviously increase the converter volume and decrease the volume density [25, 26]. Because of the increased number of power electronics converters in aviation applications within limited space, very compact EMI filters are required. The design of such filters is very complex, and trial-and-error is often needed to meet both the EMI specifications and high power density requirements.



(a) Interconnecting cable test



(b) Power line test

Figure 1-5 The DO-160 EMI standard for aircraft applications

Meanwhile, a more compact EMI filter design will inevitably decrease the distances between the passive components of the EMI filter and affect the filter performance significantly by coupling especially in the EMI spectrum range [27, 28]. Thus, achieving a better EMI filter design for transportation applications becomes important.

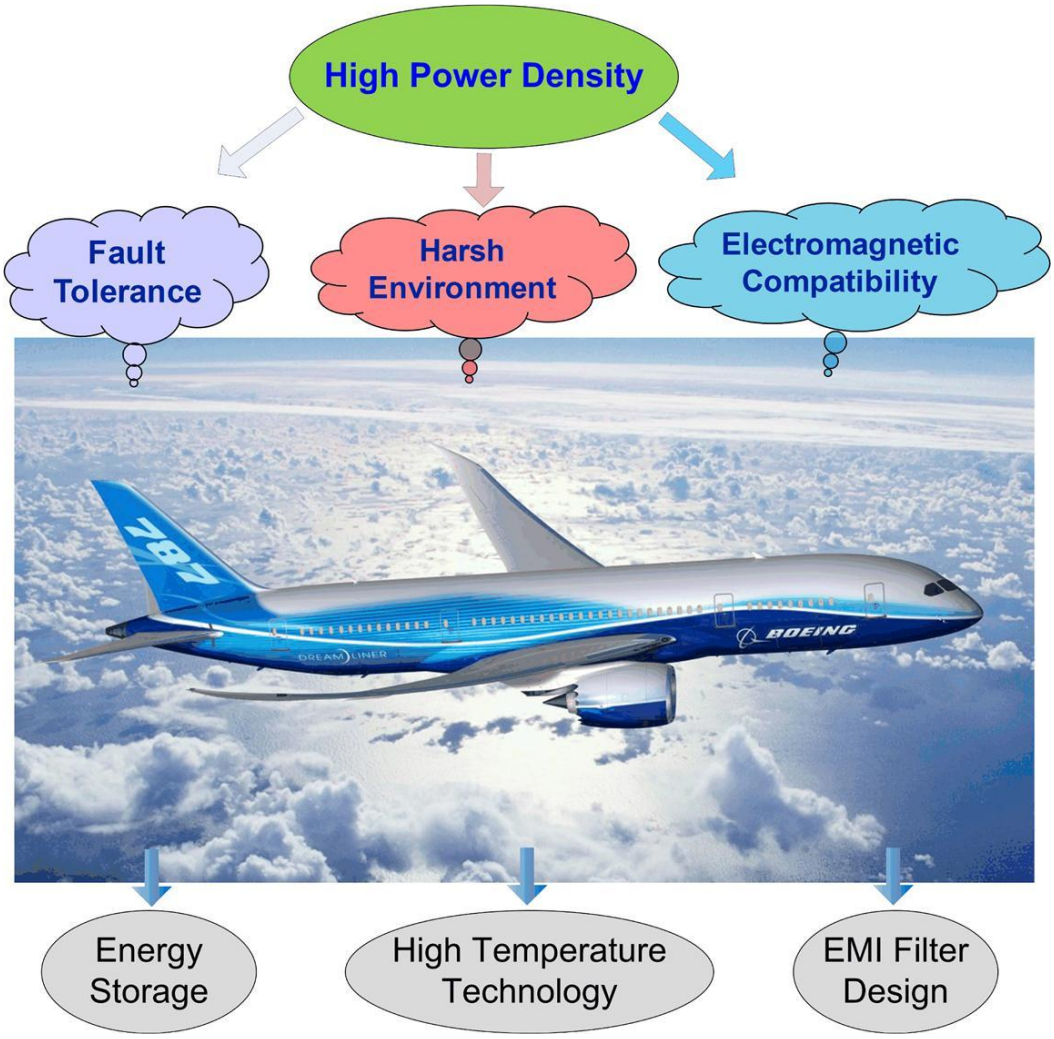


Figure 1-6 Motivation and objective

Based on the analysis above, the research motivations and objectives are summarized in Figure 1-6. The key objective is to achieve a high power density converter design for transportation applications. However, due to the operational characteristics of transportation applications, the high power density converter design will focus on three aspects: fault tolerance, harsh environment operation, and electromagnetic compatibility. From the technological point of view, higher energy

storage efficiency, better power electronics devices capability, better packaging performance and better EMI filter design will help to satisfy the motivation and objective.

1.2 Challenges and Literature Survey

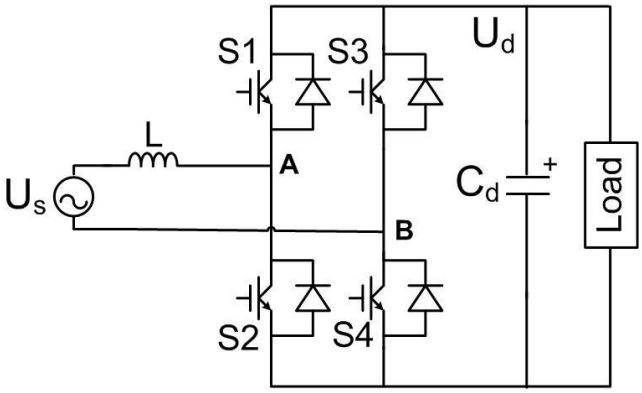
As discussed above, several techniques are required to further increase converter power density for transportation applications. This section will first summarize the state-of-the-art in these techniques. The unsolved problems of these techniques are also addressed. Based on the addressed problems, the challenges of this research are proposed.

1.2.1 Energy storage in fault tolerance

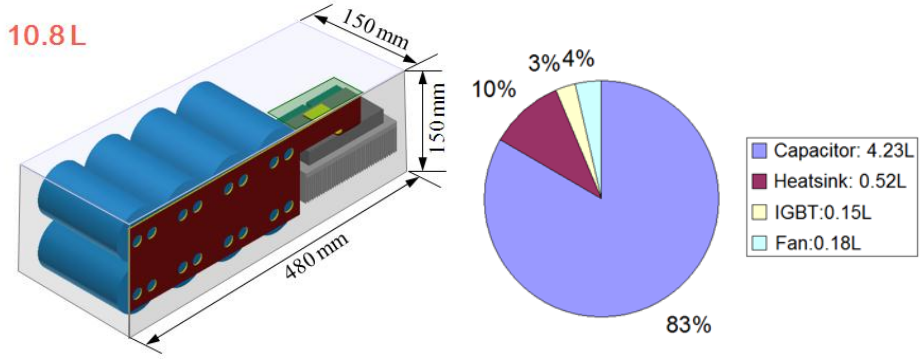
In order to achieve fault tolerance in transportation applications with safety considerations, the typical design approach involves a multiple-phase drive in which each phase may be regarded as a single module. This results in the whole converter consisting of several separate H-bridge converters. However, unlike the typical three phase converter, the H-bridge converter doesn't have a natural sort of power balance. Energy storage components are required in the system to store the second order ripple power. Usually, the dc link capacitor plays the role of the ripple energy storage component. A real design for such a 15 kW single phase PWM rectifier with the relevant parameters is summarized in Table 1-2 and is shown in Figure 1-7.

Table 1-2 Summary for the system parameters

Power rating	15 kW	Input voltage	213 V (peak)
DC bus	540 V	Supply frequency	233 Hz
Input inductance	1.24 mH	DC voltage ripple	±2%



(a) H-bridge schematic



(b) Preliminary layout design

Figure 1-7 Layout design and main component's volume comparison for H-bridge rectifier

From this comparison, the dc link capacitor can be clearly identified as the key size contributor to the total volume of the system. This means that the capacitor is the power density barrier for the single phase PWM rectifier. Using a bulky dc-link capacitor is an inefficient way of filtering the low-frequency ripple energy.

Hence the need for a better solution to achieve high power density in single-phase rectifiers is apparent, as is the need for an alternative way to filter the low-frequency ripple energy intrinsic to the converter operation. Based on the paper survey, several active methods have been proposed to deal with this second-order ripple power, such as dc ripple reduction circuits [29-32], two-stage cascaded power factor correction [33], parallel power factor correction [34] [35] and the dc bus conditioner [36]. These

can be used to reduce the dc ripple current, tighten the regulation of the output voltage, improve the transient dynamic response of the system and also help to maintain the bus stability, respectively. Although these methods do not focus on the reduction of capacitor volume and the increase of power density, the principle and idea of active ripple energy storage can be utilized.

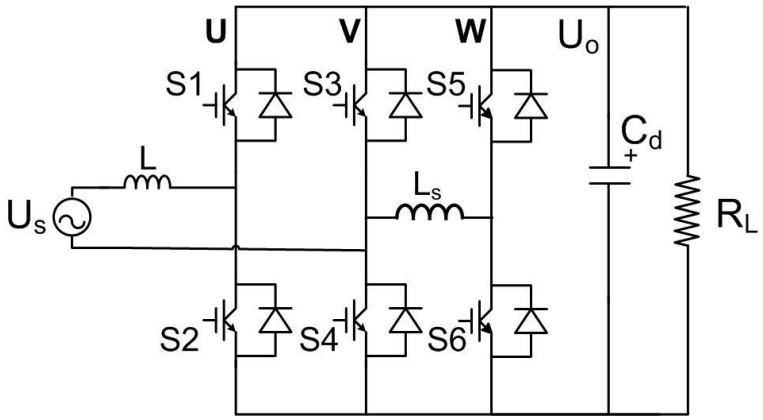


Figure 1-8 Inductive ripple energy storage method[30]

The inductive ripple energy storage method schematic diagram is shown in Figure 1-8. The characteristics of this inductive ripple energy storage method can be summarized as:

- Additional phase-leg W and an inductor L_f make up the ripple reduction circuit
- U and V phases still controlled as a typical PWM rectifier
- W phase is controlled to store the ripple energy in inductor L_s.

The drawbacks of this method are:

(1) The inductor energy density may be lower than the capacitor energy density.

(2) Since the auxiliary circuit (W phase) control is dependent on the H-bridge rectifier, the control freedom is limited.

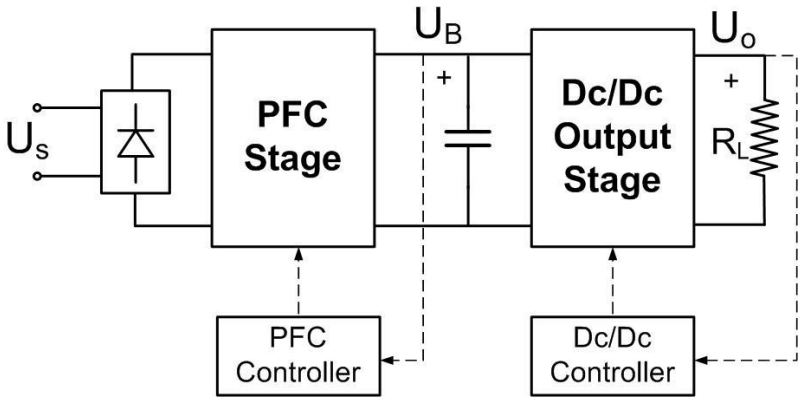


Figure 1-9 Two-stage cascaded power factor correction circuit[33]

The two-stage cascaded power factor correction circuit schematic diagram is shown in Figure 1-9. The characteristics of this two-stage cascaded PFC can be summarized as:

- The energy storage capacitor has a high bus voltage (V_B) that is loosely regulated
- The output voltage (V_o) is tightly regulated by the Dc/Dc output stage
- Two stages are controlled independently

The drawbacks of this method are:

(1) The input power needs to be converted twice to reach the output, which is inefficient.

(2) High voltage exists in the system

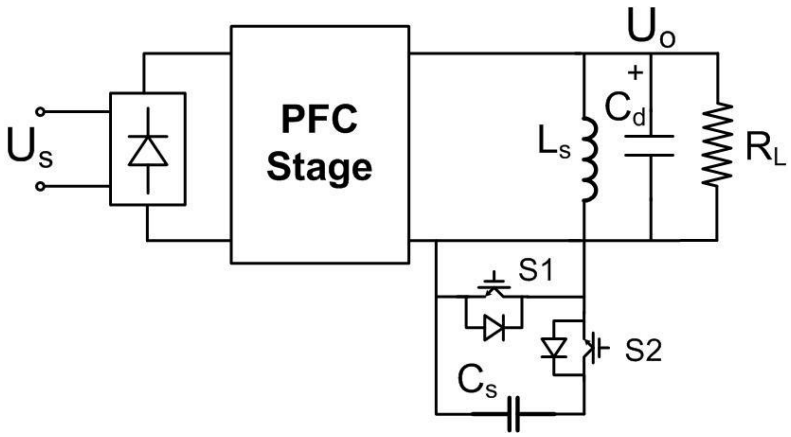


Figure 1-10 Parallel power factor correction[34, 35]

The parallel power factor correction circuit schematic diagram is shown in Figure 1-10. The characteristics of this parallel PFC can be summarized as:

- The boost PFC converter controls the input current.
- The output voltage (V_o) is tightly regulated by the bi-directional boost/buck converter
- The two stages are controlled independently

  The drawback of this method is the high voltage that exists in this system.

1.2.2 High temperature technologies in converter design

Besides the fault tolerance requirements, the high-temperature (HT) converters design has also become more and more important in transportation applications where the converter may operates in a harsh environment. New wideband gap devices made of materials such as silicon carbide (SiC) or gallium nitride (GaN) provide a much higher bandgap, thermal conductivity and breakdown field, which offers them the potential capability to overcome the temperature, frequency and power management limitations of traditional silicon (Si) devices. The comparison results are shown in Figure 1-11.

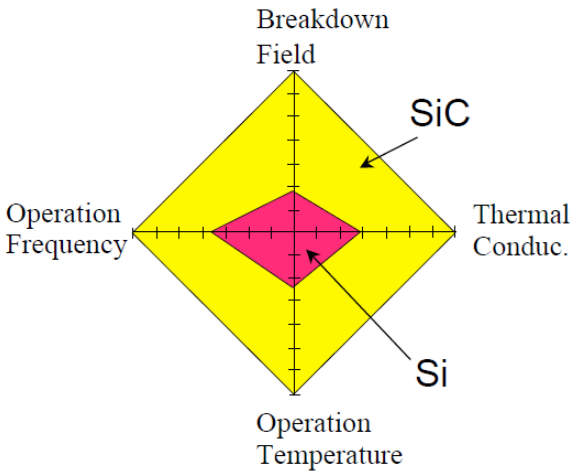


Figure 1-11 Silicon Carbide and Silicon material characteristic comparison

Silicon Carbide (SiC) has a theoretical junction temperature limit in excess of more than 600°C [37]. Since the SiC JFETs are the first available SiC devices on the market, most of the surveyed works [15, 38-48] demonstrate the SiC JFETs devices high temperature capability. Besides the JFETs based papers, there are also papers that demonstrate the SiC MOSFET [47, 49, 50] , SiC BJT [51, 52] and SiC IGBT [53] performance. In addition to the SiC devices high temperature capability, the SiC devices also have a much lower conduction and switching loss when compared with silicon devices [48, 54-58]. Because of these characteristics, the SiC devices can work at a higher switching frequency and higher junction temperature thus leading a much higher power density in the converter design by reducing the heatsink volume and passive component size [59-61].

Although the SiC device bare die can support high temperature applications, the power module packaging technique also plays an important role. For example, Powrex is manufacturing a SiC MOSFET power module with the Cree devices [62]. Even though the papers [50] already claim that the SiC MOSFET has a high temperature capability up to 200 °C, this module can only support 150 °C. This temperature value is constrained by the low temperature packaging. In order to fully utilize SiC's high temperature characteristics, some publications show high temperature packaging with SiC semiconductors [17, 40, 44, 63-68]. However, these publications still use the commercial wirebond packaging structure designed for Si devices that may limit the advantages of SiC semiconductors for faster switching speed. When compared with this conventional method, the planar packaging structure will bring several advantages, such as a smaller footprint, smaller parasitic parameters, more flexible routing, and also double-side cooling capability [69-74]. However, this structure is also faced with challenges like the connections of small top

pads, the alignment of interconnections, the limited choices for die attachment materials, and the complicated and time consuming process, etc [69, 70]. In addition to this, double-side solderable devices are generally not available which constrain the applications of the planar structure. To fully utilize the SiC device's high temperature tolerance and fast-switching capability, a reliable high-temperature packaging method for the SiC devices with smaller parasitic is desired.

Meanwhile, the harsh environment of some applications requires not only high-temperature semiconductor power modules, but also high-temperature passive components and high-temperature control electronics that are able to operate in these environments.

For the high temperature passive components, paper [13, 75] shows the selected high temperature magnetic and capacitor components for the gate drive circuit, and paper [38] shows the high temperature inductor for the main circuit.

For control electronics, junction leakage is a major concern in bulk CMOS processes. Junction leakage causes junction temperatures to be higher than the ambient, and can lead to the failure of the circuit. SiC-based devices are expected to be able to operate up to 600°C. However, SiC-based integrated circuit manufacturing is not yet available. With silicon-on-insulator (SOI) technology, the leakage current for high-temperature operations can be effectively reduced. A buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and the source p-n junction diodes. In addition, the threshold voltage variation with temperature is smaller in SOI devices than in bulk silicon-based devices. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at a higher temperature. These properties make SOI-based circuits

capable of operating successfully in the 200°C-300°C temperature range, which is well above the range of conventional bulk silicon-based devices [18, 49, 76-80].

Based on the limited available active and passive high temperature components, the system subfunctions such as high temperature gate drive, high temperature sensors and high temperature controllers need to be designed and built accordingly to make the whole converter capable of working in the harsh enviroment.

Since there is no commercial high-temperature opto-coupler available, transformer isolation is the only choice for a isolated high-temperature gate drive design. Papers [40, 75, 81] present the isolated high temperature gate drive. [78] presents the non-isolated gate drive direct with the SOI components.

1.2.3 Electromagnetic interference

As mentioned above, because of the strict EMI requirement for transportation applications, the EMI filter becomes one of the key contributors to the system volume. The paper [25] systematically studied the impact of the EMI filter on the power density of three-phase PWM converters, and proposed the design method for a high density EMI filter.

However, previous works only focus on the low frequency range and the high frequency information is missing. [82, 83] Studied the EMI filter design with an integration concept that utilized the leakage inductance from the common mode as the differential mode inductance. However, these studies don't include the non-ideal conditions from both the parasitic and also the coupling. Papers [84-88] discuss the filter layout influence to the EMI performance by both self parasitic and coupling in

the DC/DC converter from the small signal test. In order to reduce the self parasitic influences, references [89-93]show different parasitics cancellation methods.

Meanwhile, EMI noise source and attenuation prediction are also challenges in power converter applications. Both time consuming simulations to get noise profiles and the large amount of parasitic elements that count in the noise propagation contribute to this challenge. In order to handle this complex problem, some research has been conducted to predict the noise of power converters. The time domain simulation of the converter, including all the parasitic and noise sources are included in [94, 95]. The noise spectrum is then obtained by computing the FFT of the resulting currents. This approach gives good results as long as the switches and circuit models are very close to the real physical devices. Other papers [96, 97] based on behavioural models are utilized to measure the switching noise profile of a semiconductor for different current levels. Specific measurement techniques are required to obtain good result as well as special LISN. This approach is not yet suited to deal with high complexity converters. Some frequency domain equivalent circuit analysis is proposed in the literatures of [94, 95, 98-100]. In the frequency domain, all the circuit impedances are in phase form, allowing very fast computations of the resulting noise spectrum without costly software and time consuming simulations.

Moreover, more compact EMI filter design will inevitably decrease the distances between the passive components of the EMI filter and meanwhile affect the filter performance significantly by coupling especially in the EMI spectrum range. A lot of research has been carried out during the past few years to improve EMI filter performance. Generally, there are two non-ideal factors, which influence the EMI filter design procedure and performance: self-parasitic and mutual parasitic. Beside self-parasitic, mutual parasitic has a strong relationship between the components

coupling. Coupling between filter components has been analyzed in numerous works [85-87, 90, 101, 102] to improve filter performances. Papers [84-88, 103] discuss the layout influence to EMI performance including the effect of both self-parasitic and coupling. Papers [102, 104] show the coupling influence in the three phase EMI filter design and also show that magnetic shielding helps to improve the performance. Paper [105] studied the winding imperfection influence to the stray flux.

1.2.4 Challenges

The target of this research is to design and develop a high power density and high temperature converter for transportation applications specifically for aircraft. As discussed above in this section, there are many unsolved issues existing in this area. As shown in Figure 1-6, the most challenging works are summarized below in three different aspects:

(1). Better energy storage solution:

Although some of the surveyed results use other energy storage components instead of the dc link capacitor for the single phase converter design, most of the literature does not focus on converter power density. First, the relationship between ripple energy and other system parameters in the single phase converter is not clear. Is there a minimum ripple energy storage requirement with a fixed operating point? Theoretically speaking, whether inductor or capacitor will lead to smaller volume with a given ripple energy storage requirement. Is it possible to use more active devices instead of passive components to better store the ripple energy and to reduce the whole system volume? In addition, transportation applications require no voltage

higher than dc bus. Thus, it is still not clear how to design high power density single phase converter in a medium or high power range application.

(2). High temperature converter design:

As shown above, a high temperature converter design will bring system level benefits by achieving a higher power density for transportation applications. SiC devices provide promising performances both for higher temperature capability and higher efficiency. Some of the previous work demonstrates the high temperature packaging in both the wirebond and planar structure. However, the wirebond structure will lead to a larger footprint and larger parasitic, which cause difficulty in routing and higher loss. For the planar structure, the fabrication process is too complex and the die-attachment material selection is too limited. In addition, a lack of solderable devices will also constrain the application of the planar packaging. How to design a reliable high temperature power module with smaller parasitic becomes an important issue.

Although there was some discussion about the high temperature power module, few papers discuss the high temperature gate drive design. Also, systematically classification and comparison of the potential high temperature gate drive topologies is desired. Better topologies need to be proposed if possible.

In addition, other high temperature components need to be surveyed and tested for high temperature applications. Moreover, previous works mostly focus on the high temperature module design, which doesn't include the whole system. Some other functions such as the high temperature sensor, filter and protection need to be designed.

(3). More compact electromagnetic interference filter (EMI) design:

Previous literatures studies the EMI filter design process both for Dc/Dc and three phase applications. However, most of the previous work focuses only on low frequency design, but the high frequency performance is not addressed properly. Although some literatures discussed parasitic and coupling influence to the filter design and proposed some post-design solutions, a method to systematically design a minimum volume EMI filter by including consideration of the non-ideal conditions is desired. Moreover, most of the previous analysis are based on the small signal and can hardly been duplicated in a real in-circuit power test. Before we further improve the EMI filter design, we need to be able to predict the in-circuit attenuation and link with the small signal test. This link allows the designer to improve their EMI filter without proceeding back and forth with the power converter prototype, an approach that is costly, ineffective and potentially destructive due to multiple manipulations.

Finally, it is still not known how to design an EMI filter with smaller components coupling without post-design solutions. The relationship between magnetic components near field distribution and excitation frequency is still not clear.

1.3 Dissertation Layout

This research report is organized as follows:

Chapter 2 studies the capacitor reduction by using the active ripple energy storage method in the fault-tolerance transportation applications. First, the minimum ripple energy storage requirement is derived independently of a specific topology. Based on the minimum ripple energy requirement, the feasibility of the active capacitor's reduction schemes is verified. Then, a bidirectional buck-boost converter is proposed as the ripple energy storage circuit, which can effectively reduce the energy storage

capacitance. Moreover, this proposed topology doesn't suffer from a high voltage problem and can easily be integrated together with the main circuit as one phase leg. A 15 kW single phase rectifier is developed to verify the proposed active ripple energy storage method. The proposed single phase H-bridge rectifier implemented with the active method can decrease the volume to 70% when compared with the traditional rectifier without the active method.

Chapter 3 studies the high temperature design in transportation applications. First, a novel hybrid structure packaging method is proposed to utilize the benefits of both wirebond structure and planar structure. Detailed analysis are conducted for the hybrid structure packaging in terms of parasitic and reliability. The hybrid structure is demonstrated with a multi-chip power module for a three phase single switch rectifier topology. The test results prove that the developed hybrid packaging SiC power module can support a 250°C junction temperature. Then, several different high temperature gate drive topologies are compared and an improved edge triggered gate drive topology is proposed for high temperature applications. Some key high temperature components are characterized in the high temperature ambient. Afterwards, the whole system design process including the controller, regulator, protection, voltage sensor, etc is presented. Finally, the system is tested in the ambient temperature from -50°C to 150°C.

Chapter 4 firstly presents a compact EMI filter design procedure with consideration of both low and high frequency attenuation requirement. The design procedure is conducted with the transfer gain consideration and components volume and parasitic models are utilized in this design. Then, the optimum number of stages for the EMI

filter can be derived based on the procedure presented above. The second part presents the EMI noise attenuation prediction with the mask impedance. This prediction belongs to a frequency domain method. First, the frequency domain equivalent circuit is presented. Both the LISN, cable, EMI filter and source can not be treated as ideal. Then, the source impedance are analyzed both for common mode and differential mode. The anlaysis proves that, the source impedance variability can be confined within a very small range with some external mask impedance, which means the source impedance can be trated as a linear item. Afterwards, the experimental results show a very good match with the prediction results both for common mode and differencial mode. Finally, a detailed analysis for the magnetic components coupling and its influence to the EMI filter design is presented in the third part. This part reveales that the magnetic coupling should be divided into two categories: low frequency coupling and high frequency coupling. It is proved that the coupling is frequency related and the high frequency near-field distribution can be dramatically different compared with the low frequency condition. Displacement current is the major reason for the change in the near-field distribution. By using the Biot-Savart equation together with the displacement current consideration, the high frequency near-field distribution can be well predicted and matched with the experimental results. In addition, a LC stage filter is utilized to demonstrate the influence from the high frequency coupling.

Chapter 5 presents the summary and future works.

Chapter 6 presents the references.

Chapter 2. Ripple Energy Storage Components Reduction

Single-phase converter is utilized in the transportation applications with the consideration of fault tolerance. However, it is also well-known that single-phase PWM rectifiers have second-order harmonic currents and corresponding ripple voltages on the dc bus. The low-frequency harmonic current is normally filtered using a bulk capacitor in the bus, which results in low power density. However, pursuing high power density in converter design is a very important goal in aerospace applications. This chapter studies methods for reducing the energy storage capacitor for single-phase rectifiers. The minimum ripple energy storage requirement is derived independently of a specific topology. Based on the minimum ripple energy requirement, the feasibility of the active capacitor's reduction schemes is verified. Then, we propose a bidirectional buck-boost converter as the ripple energy storage circuit, which can effectively reduce the energy storage capacitance. The analysis and design are validated by simulation and experimental results.

2.1 Introduction

A critical characteristic of single-phase PWM rectifiers is the pulsating power transfer that occurs from the ac line to the dc bus, which generates a ripple on the dc bus voltage at twice the line frequency when the input voltage and current are sinusoidal. The converter input instantaneous power has then both a dc and ac components, i.e., the ripple power. To limit this low-frequency ripple, a bulk dc-link capacitor is usually used. This, however, results in a large converter volume and low

power density. For aerospace application, the overall system cost will dramatically increase with the large converter volume. The usual choice for this function is the aluminum electrolytic (AE) capacitor, which offers low cost and a high energy density, partially offsetting the overall increase in the power converter volume. However, this type of capacitor is known for having a somewhat short lifetime, which is unacceptable in many applications[106, 107]. Hence the need for a better solution to achieve high power density in single-phase rectifiers is apparent, as is the need for an alternative way to filter the low-frequency ripple energy intrinsic to the converter operation [26].

Several active methods have been explored to deal with this second-order ripple power from the ac side in single-phase applications; namely a dc ripple reduction circuit [29-32], two-stage cascaded power factor correction (PFC) [33], parallel PFC [34, 35], dc bus conditioners [36], and ac side active filter [108]. Any of these can be used to reduce the dc ripple current, increase the regulation of the output voltage, and improve the transient dynamic response of the system while also helping to maintain the dc bus stability. All these methods have in common the use of an auxiliary circuit and auxiliary ripple energy storage devices. These methods are summarized and classified in Figure 2-1. In terms of storage elements, the methods are classified into inductive and capacitive energy storage, whereas from a topology standpoint they are classified into single- and multi-stage active circuits. For the latter case, the auxiliary circuit can be connected either in series or in parallel with the main power circuit, and its control strategy can be implemented dependent or independently of the control of the single-phase PWM rectifier.

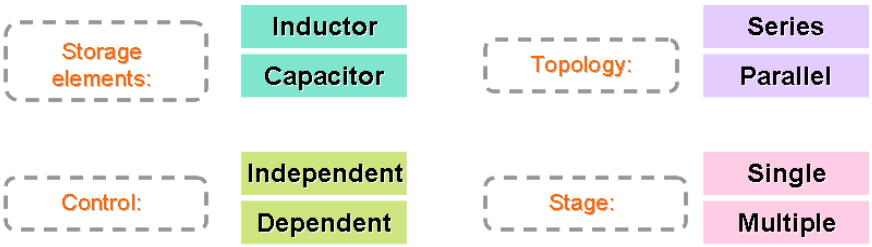


Figure 2-1 Circuit and storage approach classification.

The ripple cancellation methods discussed above have not quantitatively analyzed the low-frequency ripple energy storage requirements for single-phase rectifiers nor have they focused on the reduction of the converter volume. In this chapter, the ripple energy of the single-phase PWM rectifier is analyzed in detail, and a theoretical analysis is presented to verify the feasibility of reducing the converter volume by means of a capacitive auxiliary energy storage system. Building upon this result, this chapter proposes a bidirectional buck-boost converter as an auxiliary ripple energy storage circuit, which can effectively reduce the converter energy storage capacitance and thus lead to a 50% volume reduction of the system size. The control methodology and design considerations of this bidirectional buck-boost converter are presented in this chapter. Finally, simulation and 15 kW experimental results are provided for verification purposes.

2.2 Single-Phase Rectifier Ripple Energy Analysis

The traditional H-bridge rectifier has a simple circuit topology and a low component count. This leads to low cost and high efficiency [109, 110]. The following analysis examines a single-phase PWM rectifier prior to the selection of a specific energy storage component, as shown in Figure 2-2.

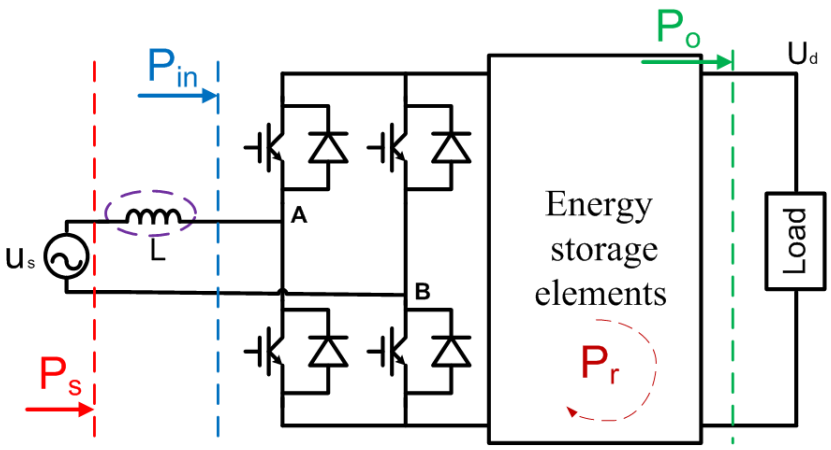


Figure 2-2 A typical H-bridge single phase PWM rectifier.

The ac supply voltage u_s and current i_s are assumed to be sinusoidal, as shown in the following equations:

$$u_s(t) = U_s \sin \omega t \tag{2-1}$$

$$i_s(t) = I_s \sin(\omega t - \varphi) \tag{2-2}$$

where U_s and I_s are the voltage and current peak values, respectively; φ is the angle between the supply voltage and current; and ω is the supply angular frequency. The supply power from the ac source can be expressed as :

$$P_{in} = u_s(t) i_s(t) = \frac{U_s I_s}{2} \cos \varphi - \frac{U_s I_s}{2} \cos(2\omega t - \varphi) \tag{2-3}$$

The energy of the input inductor can be expressed as (2-4) and the corresponding power is (2-5)

$$E_L = \frac{1}{2} L i_s^2(t) = \frac{1}{2} L I_s^2 \sin^2(\omega t - \varphi) \tag{2-4}$$

$$P_L = \omega L I_s^2 \sin(\omega t - \varphi) \cos(\omega t - \varphi) \tag{2-5}$$

where L is the input inductance.

The input power of the rectifier after the input inductor can be obtained by subtracting (2-3) and (2-5).

$$P_{in} = P_o + P_r = \frac{U_s I_s}{2}\cos\varphi - (\frac{U_s I_s}{2}\cos(2\omega t - \varphi) + \frac{\omega L I_s^2}{2}\sin(2\omega t - 2\varphi)) \quad (2\text{-}6)$$

As we can see in (2-6), the instantaneous power consists of two parts: a constant power and a ripple power, defined respectively in (2-7) and (2-8).

$$P_o = \frac{U_s I_s}{2}\cos\varphi \quad (2\text{-}7)$$

$$P_r = -(\frac{U_s I_s}{2}\cos(2\omega t - \varphi) + \frac{\omega L I_s^2}{2}\sin(2\omega t - 2\varphi)) \quad (2\text{-}8)$$

The constant power (2-7) feeds the dc load, whereas the ripple power (2-8) is a second-order harmonic power, which can be rewritten in the following form.

$$P_r = \sqrt{\frac{U_s^2 I_s^2}{4}\cos^2\varphi + (\frac{\omega L I_s^2}{2} - \frac{U_s I_s}{2}\sin\varphi)^2}\,\sin(2\omega t - 2\varphi + \psi) \quad (2\text{-}9)$$

where $\psi = \arctan\dfrac{\frac{U_s I_s}{2}\cos\varphi}{\frac{\omega L I_s^2}{2} - \frac{U_s I_s}{2}\sin\varphi}$.

If an ideal lossless power converter is assumed, the output power P_o equals the constant power in (2-7). The peak ac-side supply current can then be expressed as follows.

$$I_s = \frac{2P_o}{U_s\cos\varphi} \quad (2\text{-}10)$$

By using the ripple power (2-9) and peak current (2-10), the ripple energy can be determined as,

$$E_r = \frac{P_{r\_peak}}{\omega} = \frac{\sqrt{P_o^2 + (\frac{2\omega L P_o^2}{U_s^2\cos^2\varphi} - P_o\frac{\sin\varphi}{\cos\varphi})^2}}{\omega} \quad (2\text{-}11)$$

Equation (2-11) shows the relationship between the ripple energy, the output power, the ac input voltage, the ac frequency, the input inductor and the input power factor. The only way to avoid this ripple from affecting the dc load is to provide an alternative ripple energy storage device or component, which should simply act as a ripple filter.

The parameters of an example 15 kW single-phase PWM rectifier are summarized in Table 1-2. With the above analysis, the relationship between different variables and ripple energy is plotted in Figure 2-3 and Figure 2-4.

Figure 2-3 shows the relationship between the ac side supply frequency, power angle and ripple energy with the condition of a fixed 1.24mH input phase inductor. It can be observed that the supply frequency has an obvious influence on the ripple energy, and the lowest supply frequency leads to the worst case for the ripple energy storage. Figure 2-4 shows another relationship between the phase inductor, power angle and ripple energy with the assumption of a fixed 233Hz supply frequency. We can see an obvious influence of the phase inductor on the ripple energy. With unity power factor, the higher the inductance, the more ripple energy needs to be stored. This can be considered as a tradeoff between the system ripple energy and the ac side current harmonics. The reason can be explained by (2-8). The total system ripple power is composed of two parts: The first part of the ripple power comes from the ac source; this is characteristic of the single-phase system, because the power is not balanced. The second part of the ripple power comes from the phase inductor, especially when the phase inductance and supply frequency are high and the influence is more obvious.

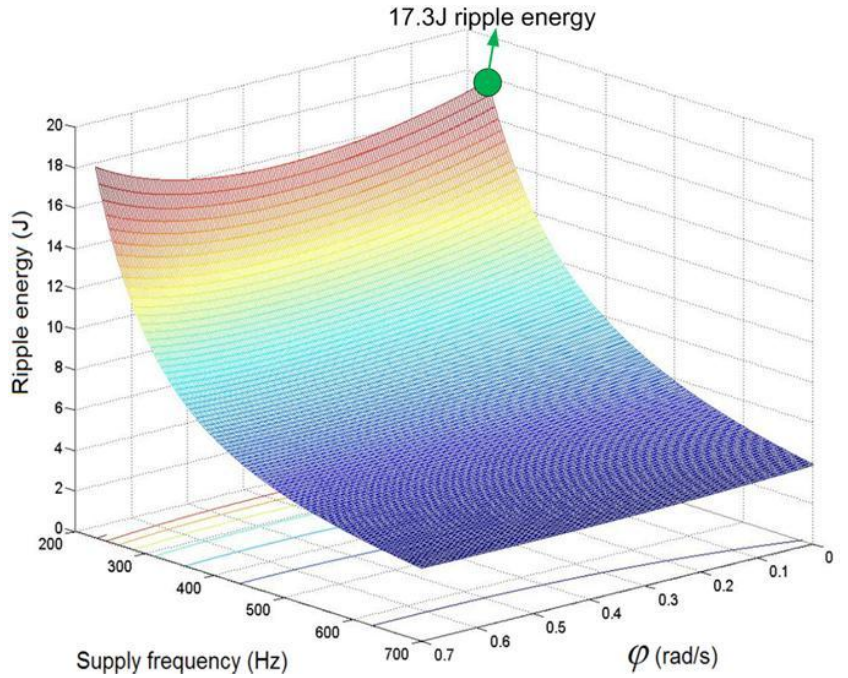


Figure 2-3 The relationship between f φ & ripple energy.

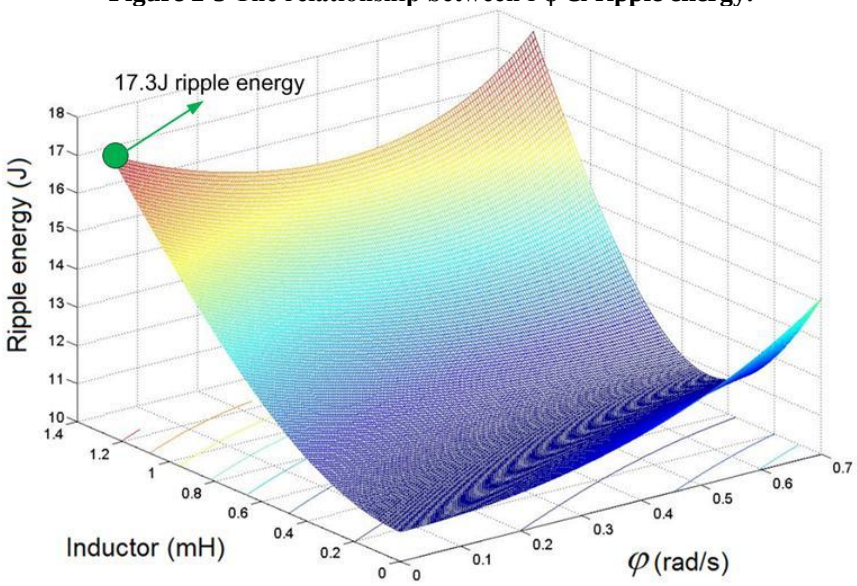


Figure 2-4 The relationship between L φ & ripple energy.

As shown in Figure 2-3 and Figure 2-4, there is a minimum of 17.3 J ripple energy for the example single-phase system, regardless of energy storage component types or rectifier circuit.

2.3 *Inductive Energy Storage Analysis*

2.3.1 Optimum energy storage inductor design methodology

In principle, both the capacitor and the inductor can be used as energy storage components in an electrical circuit. This section will focus on the inductor energy storage and the minimum volume inductor will be designed according to the optimal design procedure.

Figure 2-5 shows the design process. The purpose for this design is to select the minimum size inductor with a given ripple energy and the frequency. We can traverse all the possible core materials, core shapes and core dimensions. The inductors that satisfy all the design constraints will be saved. The minimum size inductor will be picked up from these inductors.

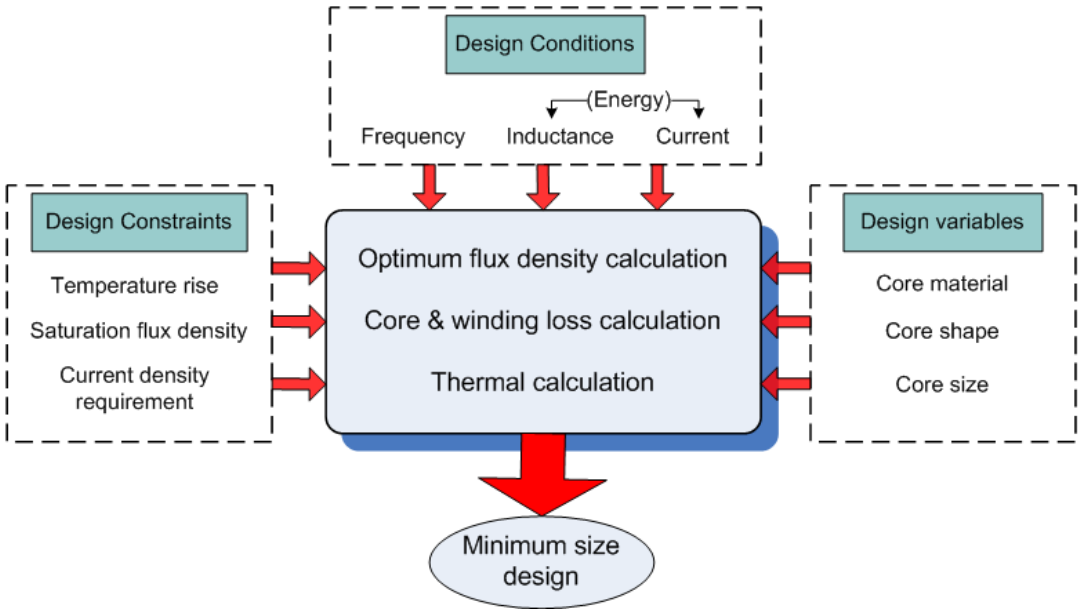


Figure 2-5 Minimum size inductive ripple energy storage design process

The detailed design process is shown as:

Step 1: Determine a core type, specify the temperature rise requirement.

(1). Determine the core material. (Ferrite, Amorphous, etc)

(2). Determine the core type. (C core, EE core, etc)

Step 2: Calculate the core loss:

$$P_c = V_c \cdot K \cdot f_{fixed}{}^{\alpha} \cdot (\Delta B)^{\beta} \tag{2-12}$$

Step 3: Calculate the winding loss:

$$R_{cu} = K_r \cdot n \cdot MLT \cdot \frac{1}{(\frac{A_{window} K_u}{n})} \tag{2-13}$$

Where: $n = \frac{L \cdot I_{\max}}{A_c \cdot B_{\max}}$

Step 4: Calculate the total loss and derived the optimal flux density

$$P_{total} = V_c \cdot K \cdot f_{fixed}{}^{\alpha} \cdot (\Delta B)^{\beta} + \frac{K_r \cdot MLT \cdot L^2 \cdot I_{\max}^2 \cdot I_{rms}^2}{A_c^2 \cdot A_{window} \cdot K_u \cdot (\Delta B)^2} \tag{2-14}$$

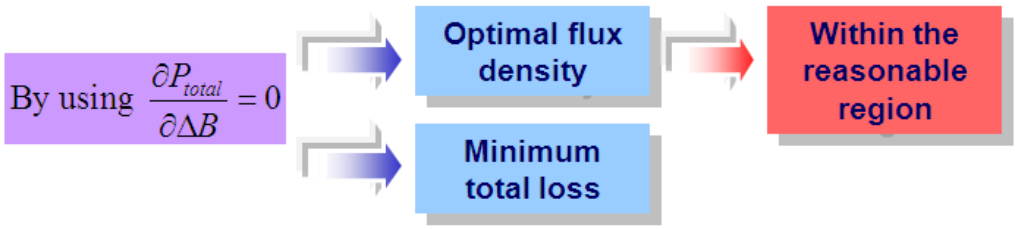


Figure 2-6 Minimum loss design

As shown in (2-14), the optimal flux corresponding to the minimum loss can be derived. It should be within the core material's reasonable region.

Step 5: Calculate the temperature rise according to the minimum total loss. The temperature rise should be within our requirements.

Step 6: Determine the minimum size.

We can select the minimum size that reaches all the requirements.

Table 2-1 Magnetic material characteristics

Material	Bsat/Bmax (T)	Core loss density (mW/cm³) $P_{core}=K*f^{\alpha}*B^{\beta}$	Manufacturer
Ferrite P	0.5/0.35	K=18.092, α=1.63, β=2.62	Magnetics
Finemet FT-3M	1.23/0.8	K=8, α=1.62, β=1.98	Hitachi
Supermalloy	0.8/0.65	K=12.25, α=1.7, β=1.937	Magnetic Metals
Amorphous-2605SA	1.56/1	K=58.6, α=1.32, β=1.68	Metglas

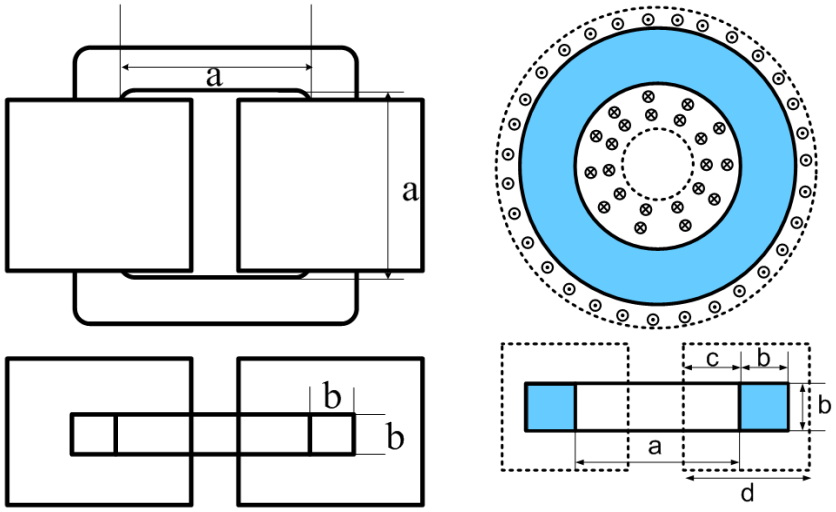
Table 2-2 Design conditions and constrains

Material	B_{sat}/B_{max} (T)
Supply frequency	466 Hz
Storage energy	18 J
Maximum temperature rise	100°C
Current density constrain	<800A/cm²

Table 2-1 shows four different core materials parameters. They are ferrite core, finemet core, supermalloy core and amorphous core. The design constrains are summarized in Table 2-2.

C core and Toroid core are selected as the core shape.

To simplify the analysis, both the C core and toroid core dimensions are shown in Figure 2-7.



(a). C core (b).Toroid core

Figure 2-7 Dimension for the C core and toroid core

The C core inductor volume, surface area and mean length per turn are derived from (2-15) to (2-17).

$$V = (a+2b)\cdot(b+a\cdot Ku)\cdot(a+2b+a\cdot Ku) \tag{2-15}$$

$$A_s = 8ab + 8a^2 Ku + 2ab^2 + 4b^3 \tag{2-16}$$

$$MLT = 4b + 2a\cdot Ku \tag{2-17}$$

The toroid core inductor volume, surface area and mean length per turn are derived from (2-18) to (2-20).

$$V = \frac{\pi d(a-2c+2d)^2}{4} \tag{2-18}$$

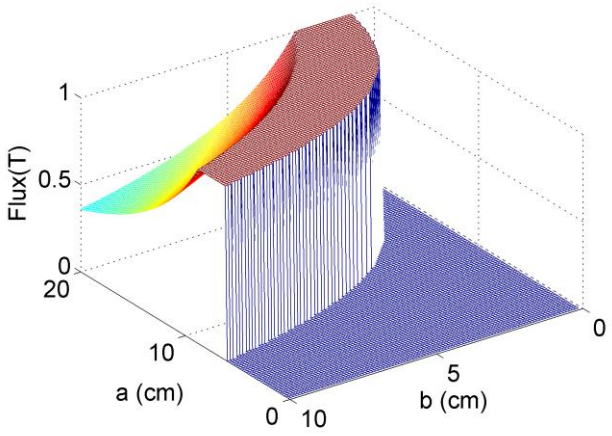
$$MLT = 2d + 2b \tag{2-19}$$

$$A_s = \pi\left[\frac{(a-2c+2d)^2-(a-2c)^2}{2} + (a-2c+2d)\cdot d + (a-2c)\cdot d\right] \tag{2-20}$$

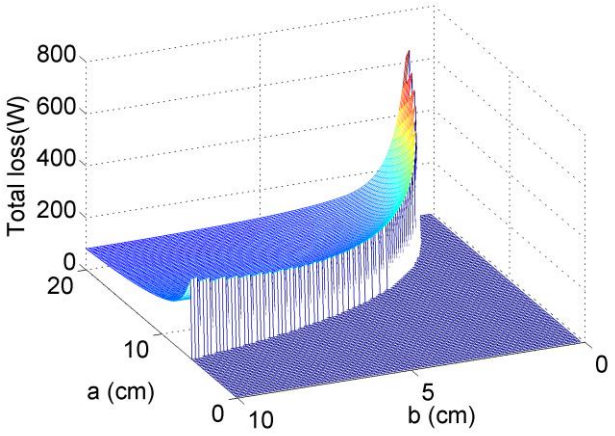
Where: $c = \frac{a-a\sqrt{1-Ku}}{2}$ $d = \frac{\sqrt{(a+2b)^2+a^2Ku}-a\sqrt{1-Ku}}{2}$

2.3.2 Inductive energy storage design results

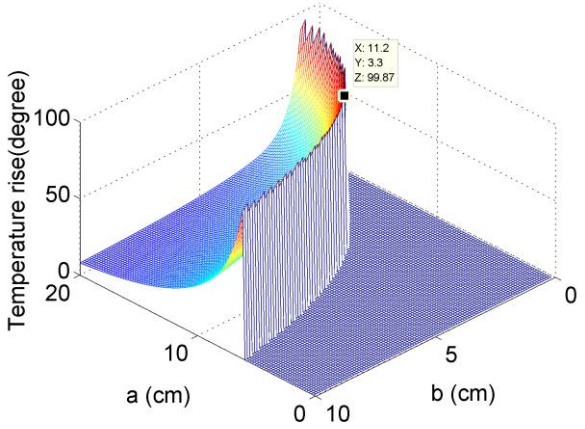
Design example: (C core, Amorphous Core (2605SA))



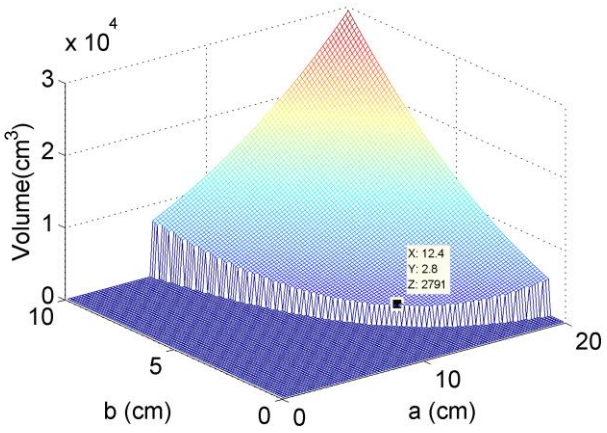
(a) Selection the flux density



(b) Total loss



(c) Temperature rise



(d) Volume of the inductor

Figure 2-8 Minimum inductor design result with Amorphous C core

Figure 2-8 shows the design result with amorphous C core. The minimum volume with the Amorphous core is 2.8L.

The calculation results are summarized in Table 2-3:

Table 2-3 Calculation results for different core shapes and core materials

Miminum volume (unit: L)	Finemet (B_{max}<0.8T)	Ferrite (B_{max}<0.35T)	Amorphous (B_{max}<1T)	Supermalloy (B_{max}<0.65T)
C	3.281	6.67	2.789	3.921
Toroid	3.41	6.9	3.11	4.076

With a certain energy storage requirement and operating frequency, inductor and capacitor volume is compared and shown in Figure 2-9. The inductor is found not to be as good as a capacitor in terms of energy density for an application using a few hundred hertz. There are two major reasons for this preliminary conclusion. First, the magnetic material saturation flux will limit the volume. In order to meet the flux saturation requirement for the energy storage inductor, a larger magnetic core size is required. Second, the inductor has more loss compared with the capacitor, in order to

meet the temperature rise requirement, more volume is required for thermal dissipation.

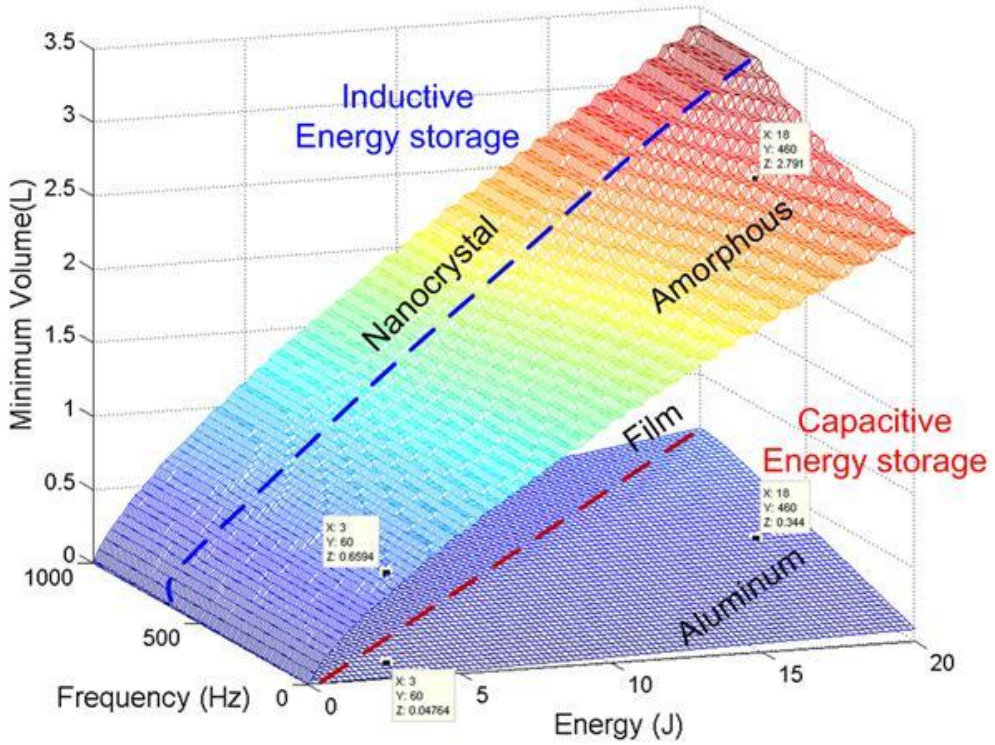


Figure 2-9 Inductor and capacitor energy storage comparison

2.4 Capacitive Energy Storage Analysis

With the conclusions drawn above, the following analysis and study is focused on the capacitive energy storage. With a given voltage rating, the selection of the capacitor is based on two aspects: capacitance and current rating. Thus the capacitive energy storage analysis should be conducted based on these two aspects. When charging a capacitor, its voltage increases from the capacitor's minimum value to the maximum value. When discharging a capacitor, its voltage decreases from the maximum value to the minimum value. Consequently, the voltage ripple fluctuation of a capacitor makes it capable of absorbing ripple power. For a conventional single-

phase PWM rectifier design, a ripple energy storage capacitor is usually put in the dc bus when there is a tight voltage ripple requirement. With the derived single-phase ripple energy requirement (2-11) and the voltage ripple requirement ΔU_d, the dc bus capacitance needed can be calculated as (2-21):

$$C_b = \frac{\sqrt{P_o^2 + (\frac{2\omega L P_o^2}{U_s^2 \cos^2\varphi} - P_o \frac{\sin\varphi}{\cos\varphi})^2}}{2U_d \Delta U_d \omega} \tag{2-21}$$

Then, based on this equation, a 1.6mF dc bus capacitance is needed with the 2% dc bus voltage ripple requirement for the example converter specified in Table.2-1. The corresponding current rating of the capacitor is then given by:

$$i_{cb\_rms} = \frac{P_{r\_peak}}{\sqrt{2}U_d} \tag{2-22}$$

If we were to use capacitors to store the ripple energy and neglect a specific application, we could determine the capacitor voltage and capacitor current for absorbing a sinusoidal ripple power using the following equations.

Let's suppose the ripple power goes to the capacitor can be expressed as:

$$P_r = P_{r\_peak} \sin(2\omega t) \tag{2-23}$$

If the capacitor voltage is expressed as U_{cs}, based on the power balance relationship, the differential equation is shown as:

$$\frac{dU^2{}_{cs}}{dt} = \frac{2 \cdot P_{r\_peak}}{C_s} \sin 2\omega t \tag{2-24}$$

Solving this differential equation yields the capacitor voltage:

$$U_{cs} = \sqrt{\frac{P_{r\_peak}}{C_s \omega}(k - \cos 2\omega t)} \tag{2-25}$$

where $k = \frac{U_{cs\_\max}^2 C_s \omega}{P_{r\_peak}} - 1$ ($k \geq 1$).

Then, the low-frequency capacitor current can be expressed as:

$$i_{cs} = \frac{P_{r\_peak} \sin 2\omega t}{\sqrt{\frac{P_{r\_peak}}{C_s \omega}(k - \cos 2\omega t)}} \tag{2-26}$$

The coefficient k is defined as the energy storage margin coefficient; its physical meaning can be expressed by (2-27).

$$\frac{k+1}{2} = \frac{E_{cs\_\max}}{E_r} \tag{2-27}$$

If k=1, the maximum energy stored in the capacitor is equal to the ripple energy, which means the capacitor is totally charged and discharged. The higher the value for k, the more redundant energy that is not used is stored in the system. For example, if we put the 1.6mF dc bus capacitor in the single-phase system with the parameters summarized in Table 1-2, then the energy storage margin coefficient is k=14, which means 86.7% of the energy stored in the dc bus capacitor is redundant.

To help visualize a smaller redundant energy storage (smaller k) in the single-phase system, Figure 2-10 plots the capacitor voltage and capacitor current with k=1, k=1.5 and k=2 according to (2-25) and (2-26). The capacitance selected for energy storage is 200μF.

As shown in Figure 2-10, k=1 represents the total charge and discharge. The capacitor voltage increases from zero to its maximum value during charge, and decreases from its maximum value to zero during discharge. The low-frequency capacitor current shows the highest peak and RMS values. When increasing k, both the capacitor voltage ripple and low-frequency capacitor current have a more sinusoidal shape. This is the reason a high k in a traditional single-phase rectifier makes the dc bus voltage ripple look like a second-order sinusoidal shape. Figure 2-10

also shows a higher k leading to a smaller capacitor current and smaller capacitor voltage ripple.

The 3D low-frequency capacitor voltage and capacitor current are plotted in Figure 2-11.

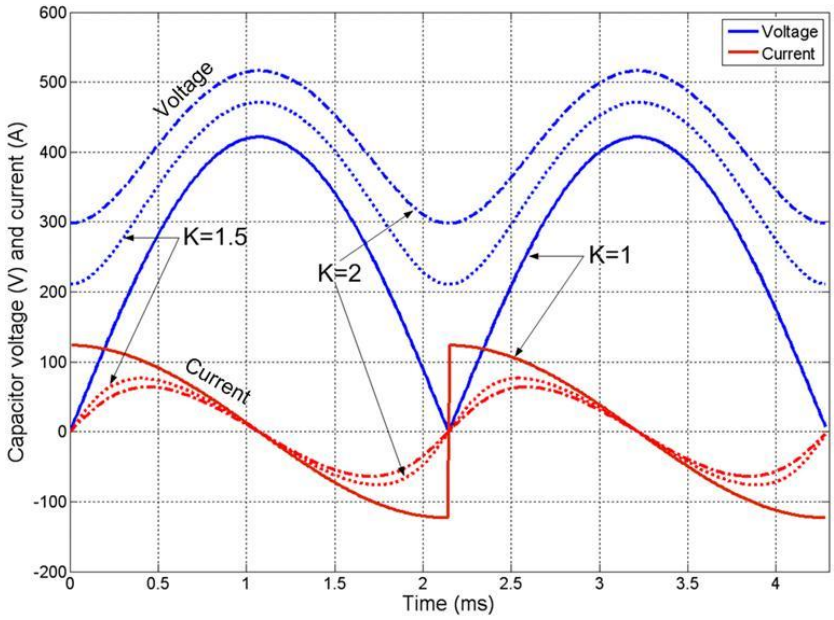
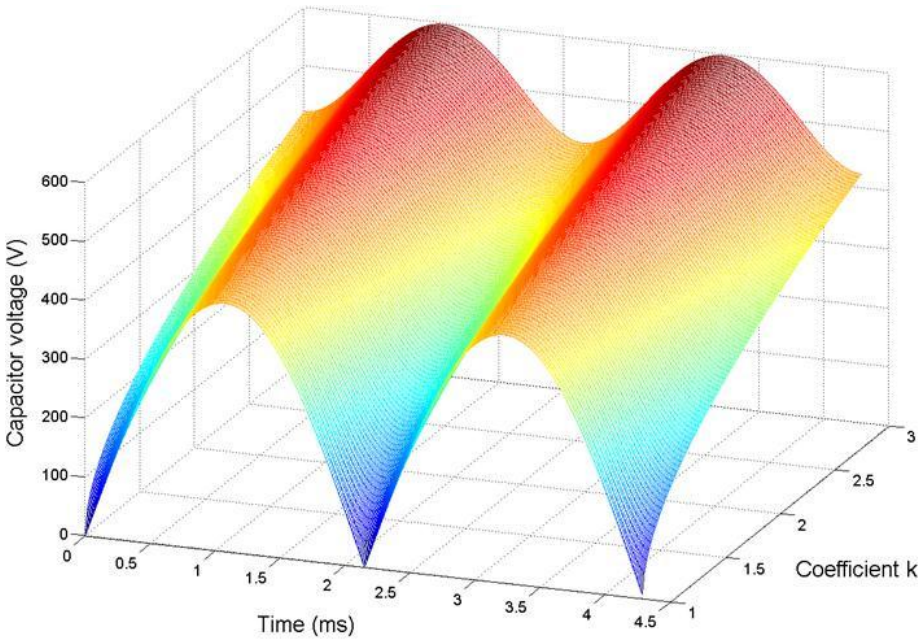
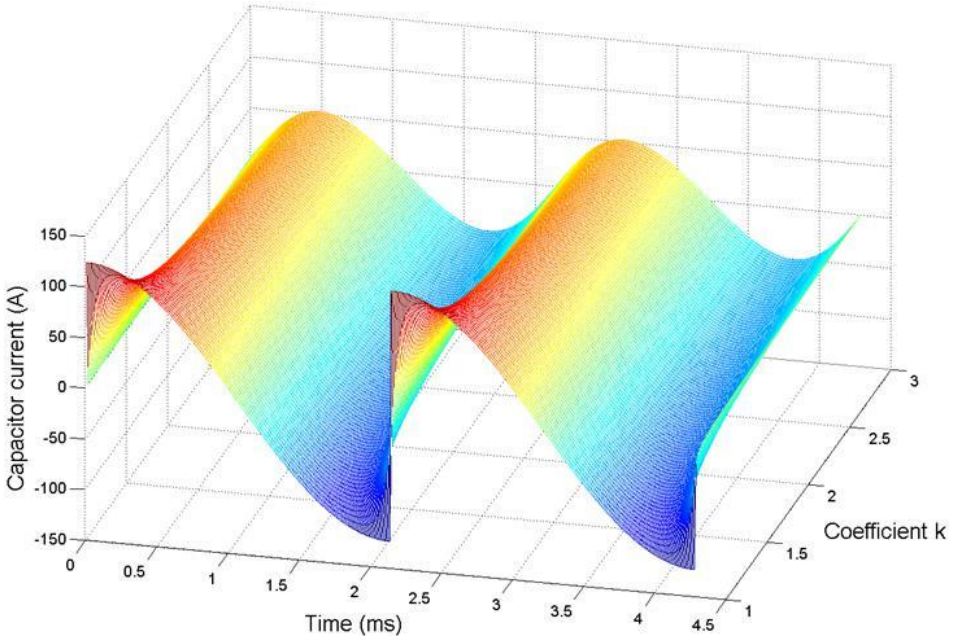


Figure 2-10 Low-frequency capacitive ripple current and capacitive ripple voltage.



(a) Capacitive ripple voltage



(b) Capacitive ripple current

Figure 2-11 Low-frequency capacitive ripple voltage (a) and capacitive ripple current (b).

As mentioned above, given a certain voltage rating, the capacitance and current rating are the two major factors that influence the selection of capacitors. Then, after derivation the capacitor voltage and current for the ripple energy storage, the capacitance and current rating analysis for the ripple energy storage needs to be conducted.

If we consider a complete charging and discharging of an auxiliary capacitor using the active method, as shown in equation (2-27), then k=1 , and the auxiliary capacitor voltage is charged from zero to a peak value; say U_{c_peak}. With these values, the minimum capacitance can be derived as

$$C_s = \frac{2P_{r\_peak}}{U_{c\_peak}^2 \omega} \tag{2-28}$$

Similar to the capacitance derivation, when fully charging and discharging the capacitor, the RMS current of the auxiliary capacitor can be derived from its current equation, as shown below.

$$i_{cs\_rms} = \sqrt{\frac{\omega}{\pi}\int_0^{\pi/\omega}\left(\frac{P_{r\_peak}\sin 2\omega t}{\sqrt{\frac{P_{r\_peak}}{C_s\omega}(1-\cos 2\omega t)}}\right)^2 dt} = \sqrt{P_{r\_peak}\cdot C_s\cdot\omega} \qquad (2\text{-}29)$$

Replacing (2-28) in (2-29) finally yields

$$i_{cs\_rms} = \frac{\sqrt{2}P_{r\_peak}}{U_{c\_peak}} \qquad (2\text{-}30)$$

It is a common practice to limit the system voltage to be as low as possible. In this chapter, the analysis and discussion are based on the assumption that the peak value of the energy storage capacitor voltage should be no higher than the dc bus voltage, which is 540 V in our example system. If this limit is relaxed, the same design and analysis procedure can be applied, but the results would naturally differ.

Equation (2-21) shows the conventional designed capacitance C_b needed for filtering the second-order ripple power if put in the dc bus, while (2-28) shows the capacitance C_s needed with the ideal condition that it can be totally charged and discharged. Figure 2-12 shows the capacitance comparison between the conventional method and the active method. Whereas in the former case a bulk dc-link capacitor is used, in the latter the active method is applied to completely charge and discharge the ripple energy storage capacitor. One horizontal coordinate is the dc bus voltage ripple requirement for the conventional design. The other horizontal coordinate is the peak voltage value U_{c_peak} of the auxiliary capacitor, which is fully charged and discharged. The vertical coordinate is the capacitance reduction using the active method compared with the traditional method. For instance, if the auxiliary energy storage capacitor voltage can be charged and discharged between zero and the dc-link bus voltage 540 V, the energy storage capacitance in the active method can decrease 12.5 times when compared with the conventional method within the 2% dc bus voltage ripple

requirement. That means the capacitance can decrease from 1.6mF to 125μF. In addition, a higher auxiliary capacitor peak voltage and the lower dc-link voltage ripple requirements lead to a further reduction of the capacitance by using active method.

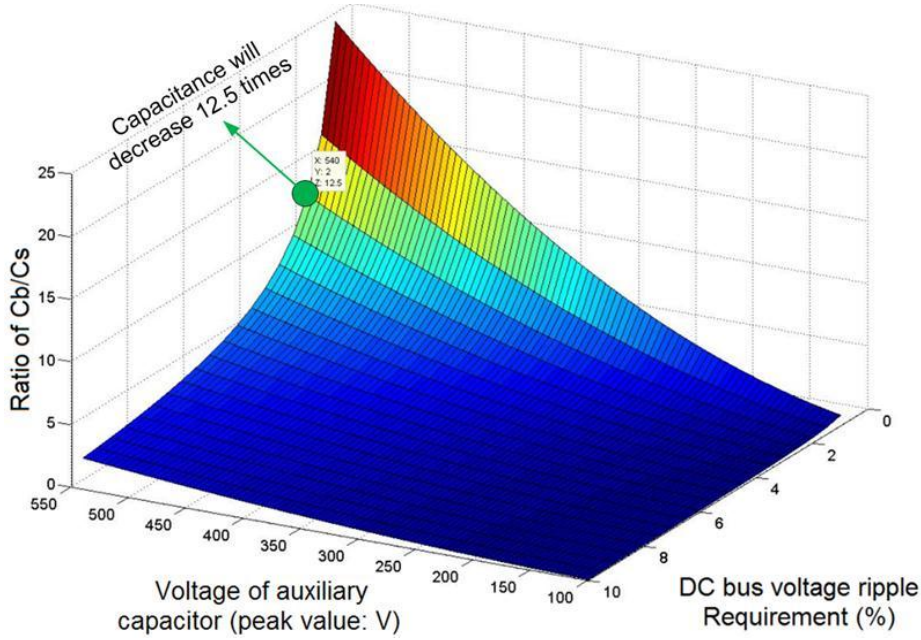


Figure 2-12 Capacitance comparison results between the conventional (passive) and active methods.

Besides the capacitance comparison between the traditional method and active method, a current-rating comparison between the conventional and active methods is also conducted, as shown in Figure 2-13. The current rating calculation of these two conditions are based on (2-22) and (2-26). As we can observe in Figure 2-13, the active method always has a higher current rating than the traditional method. If the auxiliary capacitor is completely charged and discharged between zero and the dc bus voltage, the current rating will increase to twice that of the conventional method. In addition, a lower auxiliary capacitor voltage results in a higher current rating when using the active method.

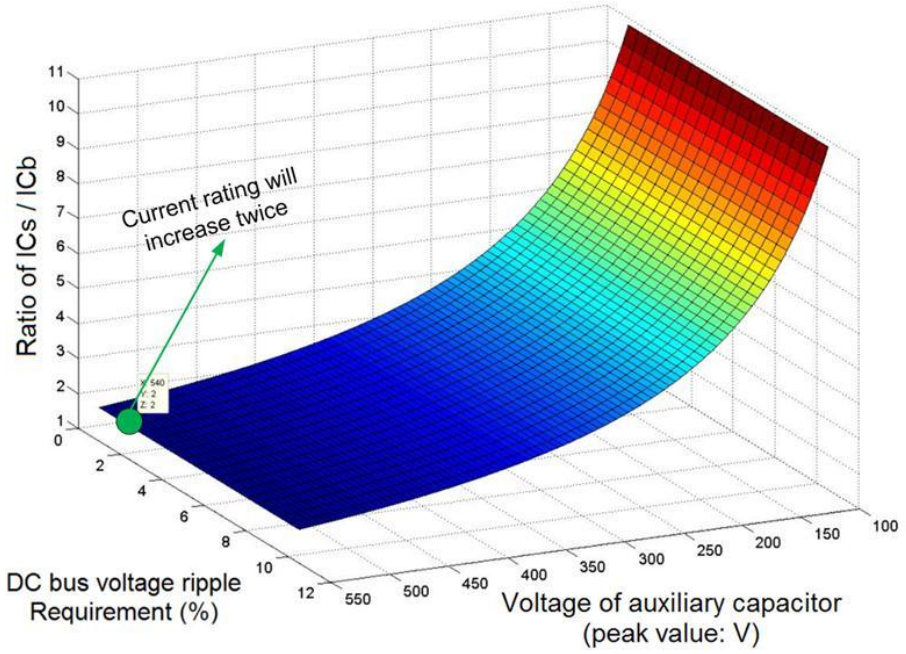


Figure 2-13 Current rating comparison results between the conventional (passive) and active method.

As mentioned above, the analysis and discussion in this chapter are based on the assumption that the peak value of the energy storage capacitor voltage should be no higher than the dc bus. Thus the voltage rating of the energy storage capacitor in both the traditional method and the active method stays the same. After viewing the capacitance and current rating comparisons between the traditional method and the active method shown in Figure 2-12 and Figure 2-13, an obvious tradeoff can be observed. By using the active method instead of the traditional method, the capacitance will decrease, but the current rating will increase. For instance, the active method will decrease the capacitance 12.5 times but increase the current rating to twice that of the traditional method in the example system shown in Table 1-2. Then, with a certain voltage rating, if the capacitance is the bottleneck for selecting the filter capacitors, a much smaller capacitor size will be achieved by using the active method, even though the current rating increases. This is because the active method is more effective in storing the ripple energy. It's also reasonable to increase the whole system's power density by using the active method. In addition, by decreasing the

capacitance, a longer life-time film capacitor can be used instead of an electrolytic capacitor.

2.5 Proposed Active Ripple Energy Storage Method

In the previous sections, we verify the feasibility of decreasing the capacitor size with an active method. The proposed topology for the ripple energy storage method is shown in Figure 2-14.

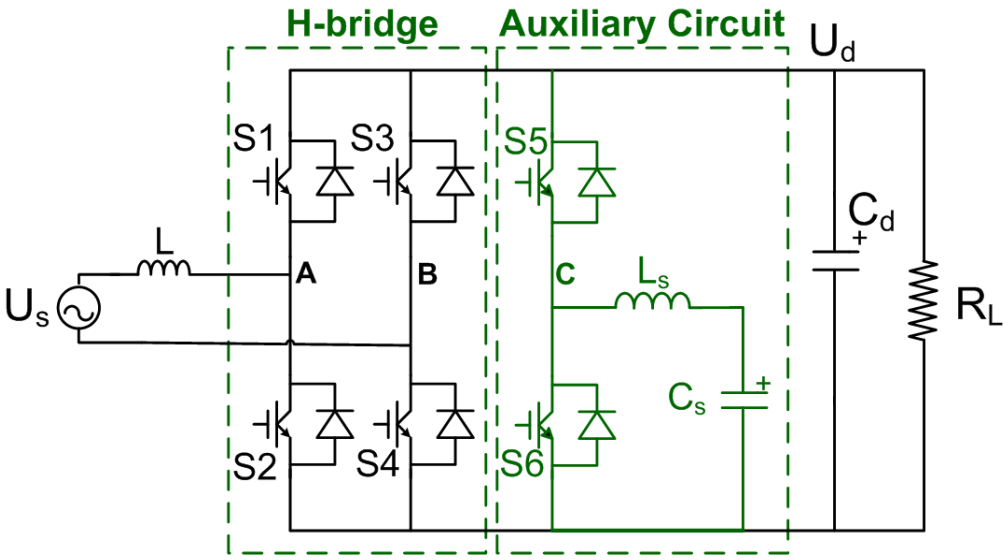


Figure 2-14 **Topology of the ripple energy storage method.**

In addition to the typical H-bridge rectifier, another bidirectional buck-boost converter connected on the dc bus works as an auxiliary circuit. The auxiliary circuit is composed of one phase leg, an auxiliary inductor, and an auxiliary capacitor. The dc bus voltage is still controlled by the H-bridge rectifier, while the ripple power that comes from the ac side is controlled by the auxiliary circuit. The auxiliary capacitor C_s is used as the energy storage component, and the auxiliary inductor L_s works as the energy transfer component that transfers the ripple energy between the auxiliary capacitor and the dc bus. When the ripple energy needs to be transferred from the dc bus to the auxiliary capacitor, switch S5 is used to control the auxiliary circuit

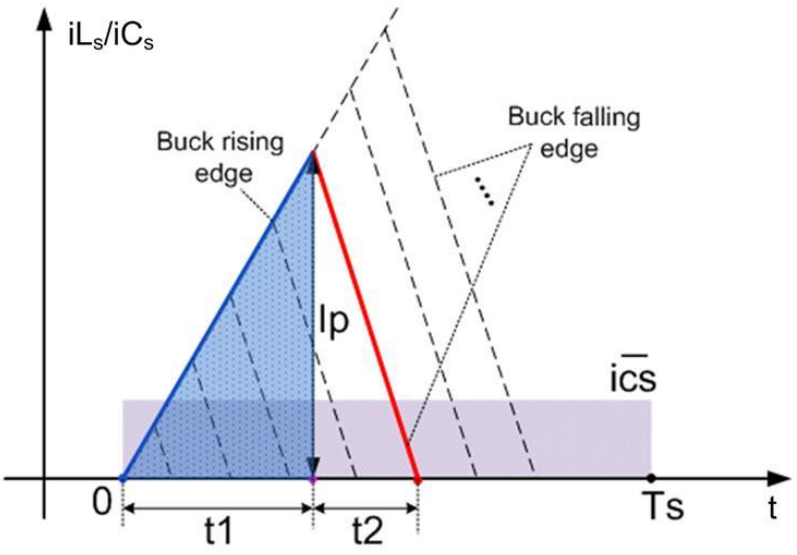
working in buck phase. During the turn-on interval of switch S5, the dc bus charges both the auxiliary inductor and the capacitor. The auxiliary inductor will further release its energy to the auxiliary capacitor during the S5 turn-off interval. If the ripple energy needs to be released from the auxiliary capacitor back to the dc bus, switch S6 is used to control the auxiliary circuit working in boost phase. During the turn-on interval of switch S6, the auxiliary inductor is charged by the auxiliary capacitor. During the turn-off interval of S6, both the auxiliary capacitor C_s and auxiliary inductor L_s will release energy back to the dc bus. Because the auxiliary capacitor is not put in the dc bus and there is no requirement for the auxiliary capacitor voltage ripple, using the auxiliary capacitor C_s to store the ripple power is much more efficient than using the dc bus capacitor, as stated above. Notice that a dc bus capacitor C_d is still needed at the output of the PWM rectifier for filtering the high-frequency ripple power and very minor low-frequency ripple power that is not totally assimilated by the auxiliary circuit. However, in this case C_d is significantly smaller than what it would be in the conventional method without the auxiliary ripple energy storage circuit.

The proposed active ripple energy storage method has several advantages. As shown in Figure 2-14, the active components in the auxiliary circuit form a typical phase leg (S5 and S6), which could be easily integrated together with the main circuit as another phase leg. Then, one three-phase module can be used for both the H-bridge rectifier and the auxiliary circuit, which will simplify the whole system hardware design. Meanwhile, because the auxiliary circuit belongs to the voltage step-down circuit, there is no voltage higher than the dc bus in this system.

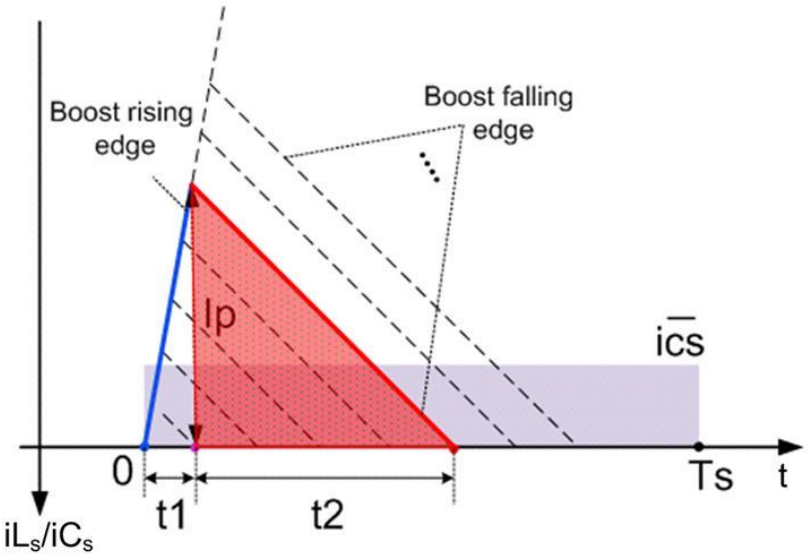
As mentioned above, the inductor is found to not be as good as a capacitor in terms of energy density for applications of a few hundred hertz. Therefore, the auxiliary

circuit is controlled in discontinuous current mode (DCM) to store all the ripple energy stored in the auxiliary capacitor but not in the auxiliary inductor. This means the auxiliary inductor works only as an energy transfer component. During each switching period, the auxiliary inductor releases all its energy to the dc bus or to the auxiliary capacitor. Therefore, once the ripple energy storage requirement is defined, the minimum required capacitance is also fixed. As observed in Figure 2-12, by using the active method, the capacitance can decrease to 12.5 times less than the capacitance with the traditional method. Thus, the theoretical minimum capacitance is 125μF. As shown in Figure 2-10 and Figure 2-11, a total charge and discharge of the capacitor leads to a high capacitor current rating. To leave some margin, the auxiliary capacitance C_s in our system is selected as 200μF. The dc bus capacitor C_d put in the system to filter the high-frequency ripple is selected as 140μF. The auxiliary inductance is selected as 45 μH and the detailed design process is shown later in this section.

2.5.1 Auxiliary circuit control method



(a) Buck charging phase



(b) Boost discharging phase

Figure 2-15 Charging and discharging duty-cycle generation strategy.

Because the switching frequency (20 kHz) is much higher than the second-order ripple frequency (466 Hz), during one switching period, the dc bus voltage and the auxiliary capacitor voltage can be considered constant. This means the auxiliary inductor can be considered to be linearly charging and discharging during each switching period. The auxiliary inductor current slopes can in turn also be considered constant. Figure 2-15 (a) shows the inductor current-charging phase for one switching period. t1 indicates the turn on time for switch S5; the inductor current increases linearly and the circuit is working in buck phase. After t1, switch S5 is turned off, and the inductor transfers its energy to the auxiliary capacitor. Because of the DCM, the inductor current goes to zero at time t2. Figure 2-15 (b) shows the inductor current discharging phase within one switching period, in which t1 is the turn-on time for switch S6. The inductor is also linearly charging, but the current direction is opposite that of the buck charging phase.

The control objective is to regulate the average auxiliary inductor current (the large triangular area, including t1 and t2) during one switching period following the current

reference derived in (2-26). Then, the duty cycle (corresponding to t1) both for S5 and S6 can be directly generated by calculation.

Defining the buck slope and boost slope as (2-31) and (2-32),

$$Boost\_slope = \frac{U_{cs}}{L} = \frac{I_p}{t_1} \tag{2-31}$$

$$Buck\_slope = \frac{U_d - U_{cs}}{L} = \frac{I_p}{t_2} \tag{2-32}$$

For the buck charging phase, the relationship between two time intervals t1 and t2 can be expressed by:

$$t2 = \frac{Buck\_slope}{Boost\_slope} t1 \tag{2-33}$$

According to the control objective, the average current within one switching cycle should be equal to the current reference; that is,

$$\frac{1}{2}(t1 + \frac{Buck\_slope \cdot t1}{Boost\_slope}) \cdot Buck\_slope \cdot t1 = \bar{i}_{cs} \cdot T_s \tag{2-34}$$

Then the duty cycle for the charging phase can be derived as

$$D1 = \sqrt{\frac{2 \cdot \bar{i}_{cs} \cdot f_s}{(1 + \frac{Buck\_slope}{Boost\_slope}) \cdot Buck\_slope}} \tag{2-35}$$

For the boost charging phase, the two time intervals' relationship can be expressed as follows:

$$t2 = \frac{Boost\_slope}{Buck\_slope} t1 \tag{2-36}$$

Like the derivation in the charging phase, the average current of the discharging phase within one switching period should also be equal to the reference:

$$\frac{1}{2}(t1 + \frac{Boost\_slope \cdot t1}{Buck\_slope}) \cdot Boost\_slope \cdot t1 = \bar{i}_s \cdot T_s \tag{2-37}$$

Then, the duty cycle for the discharging phase can be derived as

$$D1 = \sqrt{\frac{2 \cdot \bar{i}_{cs} \cdot f_s}{(1 + \frac{Boost\_slope}{Buck\_slope}) \cdot Boost\_slope}} \tag{2-38}$$

Equations (2-35) and (2-38) determine the duty cycle control laws for the charging and discharging operating modes.

The control method for the auxiliary circuit belongs to the feed-forward digital control. The duty cycle is directly calculated according to other system variables. However, it is not straightforward to obtain the current reference in (2-25), since this expression is derived based on the ripple energy balance. A similar but simpler duty cycle generation method based on the ripple current is proposed and implemented in our real application. In terms of the ripple current, the auxiliary circuit works as a parallel ripple-current filter, which is depicted in Figure 2-16. Compared with the traditional parallel active power filter, no inductor is connected in series with the auxiliary circuit input port. To prevent the ripple current from disturbing the load, the compensation current generated by the auxiliary circuit is used to counteract the ripple current. Because the compensation current is discontinuous, the auxiliary circuit has only a low-frequency ripple-current compensation capability, which is the objective.

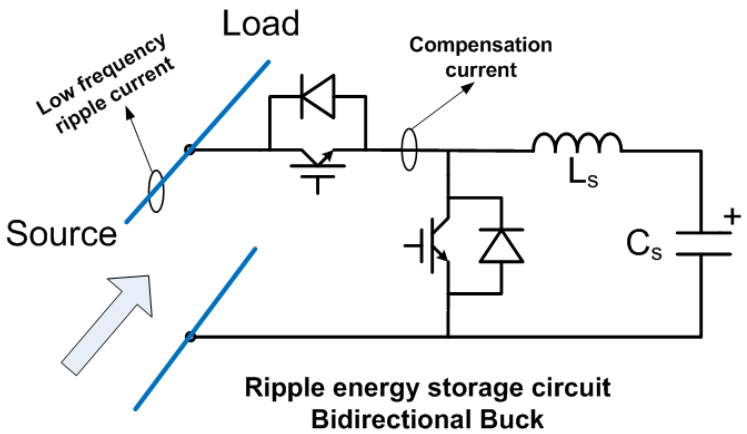


Figure 2-16 Auxiliary circuit working as a parallel ripple current filter.

The second-order low-frequency ripple current that comes from the ac side can be calculated by the H-bridge rectifier. Figure 2-17 shows the system control schematic. There are two loops for the H-bridge rectifier control [111]: the inner loop controls the ac current, and the outer dc bus voltage loops controls the dc bus voltage. A phase-locked loop (PLL) is used to track the ac voltage phase information [112]. These design considerations are shown in the next section. The ac-side current is sensed to control the inner current loop. By using this detected ac current and the control duty cycle generated for the H-bridge rectifier, the ripple current going to the dc bus can be derived as:

$$i_{ripple} = (2D-1)\cdot i_s \tag{2-39}$$

This ripple current is taken as our compensation current reference for the auxiliary bidirectional converter, which is similar to the previous derivation. As shown in Figure 2-15 (a), during the buck charging phase, the average compensation current going through switch S5 within each switching period can be calculated by the shaded triangular area (corresponding to t1). This compensation current should equal to the ripple current coming from the ac side. For the boost discharging phase, the average compensation currents going through switch S5 within one switching period can also be calculated by the shaded triangular area (corresponding to t2) in Figure 2-15 (b). Then the duty cycle for the charging phase is derived as (2-40), and the duty cycle for the discharging phase is derived as (2-41).

$$D1 = \sqrt{\frac{2\cdot \bar{i}_{comp}\cdot f_s}{Buck\_slope}} \tag{2-40}$$

$$D1 = \sqrt{\frac{2\cdot \bar{i}_{comp}\cdot f_s \cdot Buck\_slope}{Boost\_slope^2}} \tag{2-41}$$

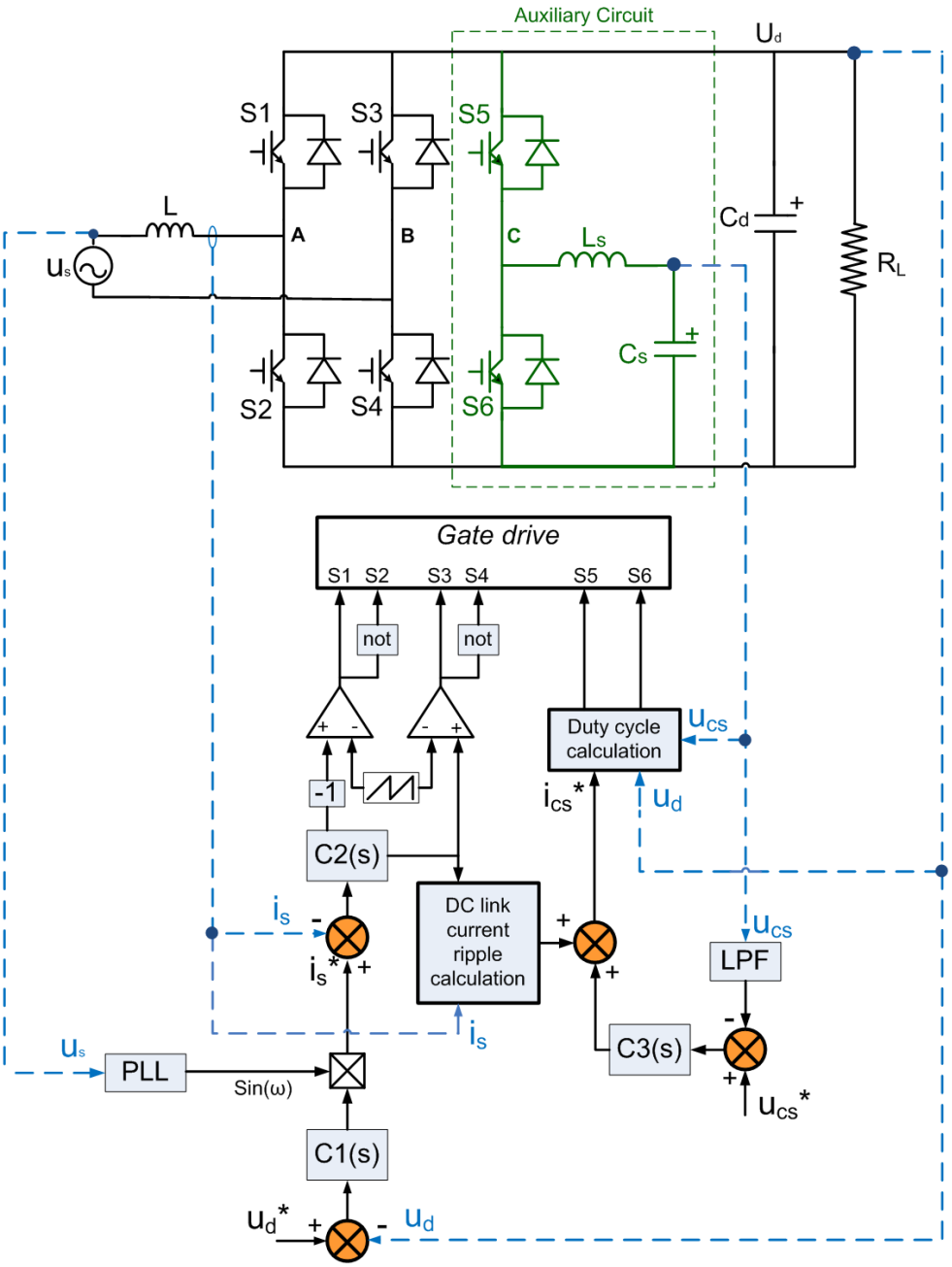


Figure 2-17 Control schematic figure for the system.

Besides the typical H-bridge rectifier control, the dc bus voltage and auxiliary capacitor voltage are sensed to generate the duty cycle for both charging and discharging phases shown in (2-39) and (2-40). If the compensation current is positive, the auxiliary circuit is controlled in the buck phase to assimilate the ripple power from the dc bus to charge the auxiliary energy storage capacitor. Similarly, when the compensation current is negative, the auxiliary circuit is controlled in the boost phase

to release the ripple energy stored in the auxiliary capacitor back to the dc bus. To prevent the overcharging and discharging of the auxiliary capacitor, another voltage loop is used to control the average value of the auxiliary capacitor voltage, where a 10 Hz low-pass filter is used to sense the average value of the auxiliary capacitor voltage.

2.5.2 H-bridge rectifier control method

2.5.3 Design considerations

A. H-bridge Modulation Method

Fig. 2-17 shows the single-phase discontinuous PWM modulation method [113]. One phase leg will not switch within half of the supply frequency. This DPWM method can lead to the minimum switching loss with a fixed switching frequency. Some variable switching frequency scheme can be used to further reduce switching loss within a given THD requirement. [114]

However, although the DPWM method shown in Figure 2-18 shows the minimum switching loss, it would lead to a thermal unbalance problem, which would not fully utilize the cooling system.

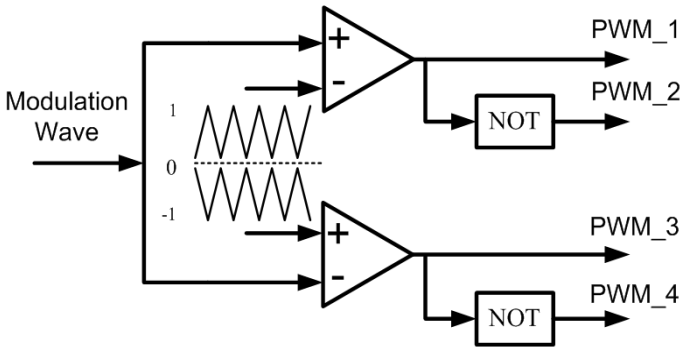


Figure 2-18 Single phase discontinuous PWM modulation method.

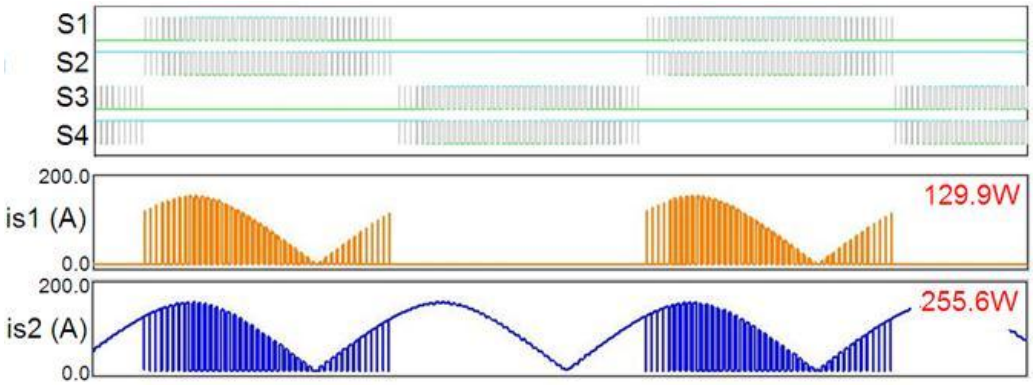
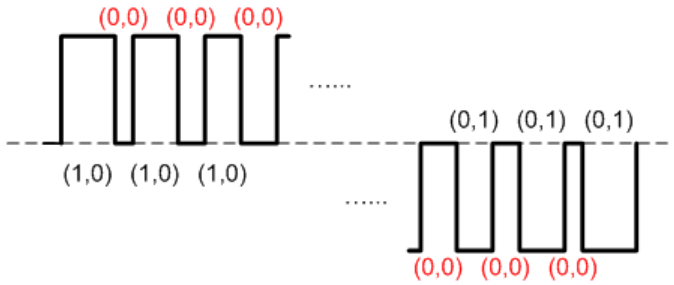
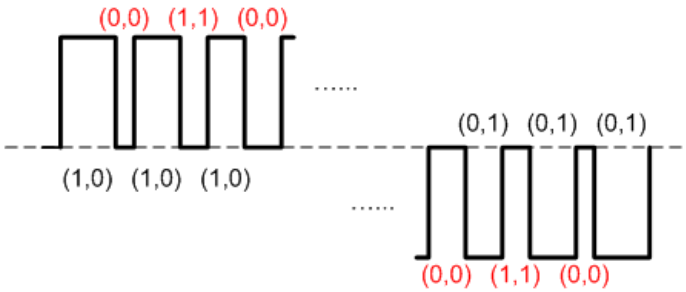


Figure 2-19 Discontinuous PWM method simulation results.

Figure 2-19 shows the simulation results of the modulation method in Figure 2-18. S1 and S2 are clamped when S3 and S4 are switching during half of the supply frequency. During the clamp period, S2 is always turned on and S1 is always turned off. Then, the loss distribution is not equal for the top and bottom switches.



(a) Asymmetrical zero vector



(b) Symmetrical zero vector

Figure 2-20 Terminal voltages and voltage vectors.

The reason for the unequal loss distribution is shown in Figure 2-20 (a). The only zero vector (0,0) is inserted with the previous method and causes this asymmetrical

problem. To prevent this, a symmetrical zero vector inserting method is proposed and shown in Figure 2-20 (b). Zero vectors (0,0) and (1,1) are inserted alternatively between each switching period.

The symmetrical zero vectors simulation results are shown in Figure 2-21. The loss distribution is uniformed for all the switches.

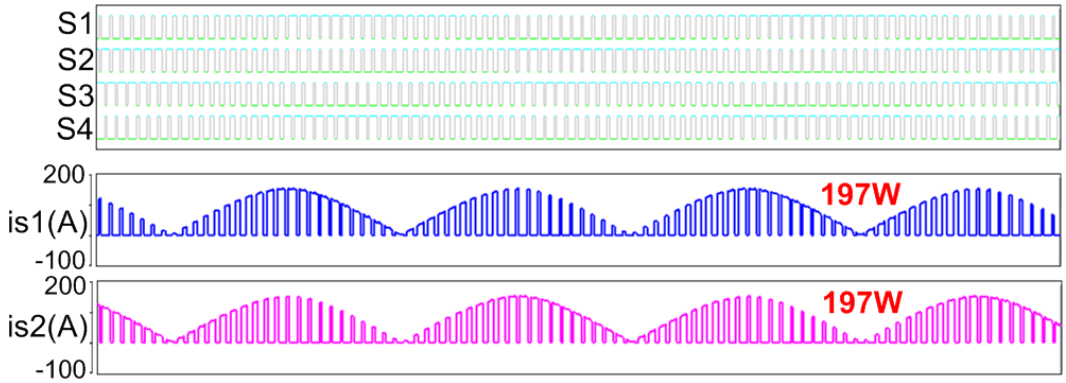


Figure 2-21 Symmetrical zero vector method simulation results

This leads to balanced thermal performance, and has been verified in a hardware test for better utilization of the heat sink.

B. Modeling of the H-bridge Rectifier

The H-bridge rectifier average model can be depicted in Figure 2-22.

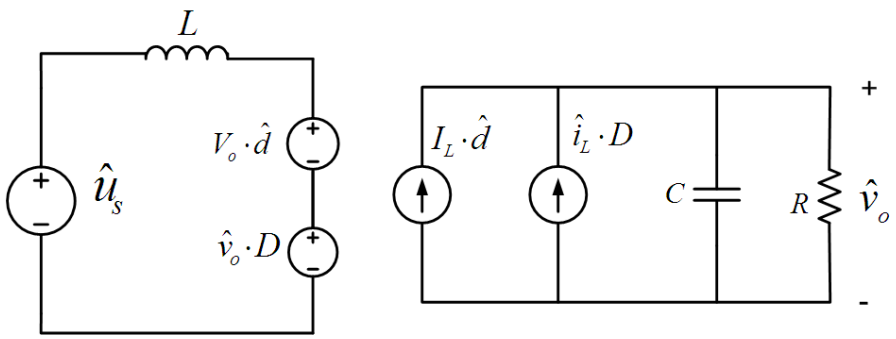


Figure 2-22 Average model of the H-bridge rectifier

The state space equation based on the average model of the H-bridge rectifier can be derived as:

$$\begin{cases} \dot{\vec{x}} = \dfrac{d}{dt}\begin{bmatrix}\hat{i}_L \\ \hat{v}_o\end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{D}{L} \\ \dfrac{D}{C} & -\dfrac{1}{RC}\end{bmatrix}\begin{bmatrix}\hat{i}_L \\ \hat{v}_o\end{bmatrix} + \begin{bmatrix} -\dfrac{V_o}{L} \\ \dfrac{I_L}{C}\end{bmatrix}\hat{d} + \begin{bmatrix}1 \\ 0\end{bmatrix}\hat{u}_s \\ y = \{[0 \quad 1] or [1 \quad 0]\}\begin{bmatrix}\hat{i}_L \\ \hat{v}_o\end{bmatrix} + 0 \cdot \hat{d} \end{cases} \tag{2-42}$$

Where, $A = \begin{bmatrix} 0 & -\dfrac{D}{L} \\ \dfrac{D}{C} & -\dfrac{1}{RC}\end{bmatrix}$, $B = \begin{bmatrix} -\dfrac{V_o}{L} \\ \dfrac{I_L}{C}\end{bmatrix}$, $C = [0 \quad 1]$ *or* $[1 \quad 0]$

With the assumption that the output dc bus voltage does not change too much, the control to inductor current transfer function and the control to the dc bus capacitor voltage transfer function can be expressed as:

$$G_{id}(s) = V_o \frac{2 + sRC}{D^2R + sL + s^2R \cdot L \cdot C} \tag{2-43}$$

$$G_{vd}(s) = \frac{-D \cdot R \cdot V_o + sR \cdot L \cdot I_L}{D^2R + sL + s^2R \cdot L \cdot C} \tag{2-44}$$

A second order Butterworth low pass filter is used to filter the sensed signal. Its effect should be considered in the controller design. The schematic diagram of the second order Butterworth filter is depicted in Figure 2-23.

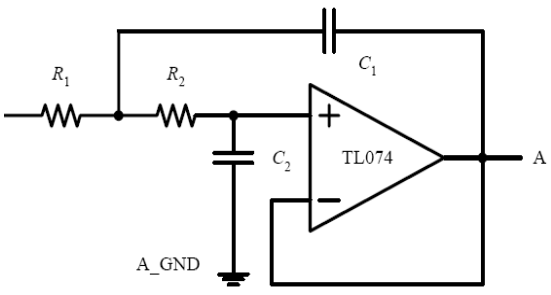


Figure 2-23 Second order butterworth filter

If the relevant parameters satisfy the relationship of: $R_1 = R_2$ and $C_1 = 2C_2$

Then the corner frequency can be expressed as:

$$f_{corner} = \frac{1.414}{2 \cdot \pi \cdot R_1 \cdot C_1} \tag{2-45}$$

Then, the transfer function of the inner loop gain without compensation can be expressed as:

$$T_{inner} = G_{id} \times G_{filter} \tag{2-46}$$

For the single phase rectifier, because the input voltage is sinusoidal, the duty cycle will not be fixed. When increasing the duty cycle from its minimum value (D=0.1) to its maximum value (D=0.9) , the low frequency inner loop gain will decrease and the cross-over frequency will increase, which means the maximum duty cycle D=0.9 is the worst case.

A PI compensator is designed for the inner current loop according to the maximum duty cycle. The cross over frequency is designed to be 5 kHz, and the phase margin is 40˚.

The outer voltage loop will be designed according to the designing results of the inner current loop.

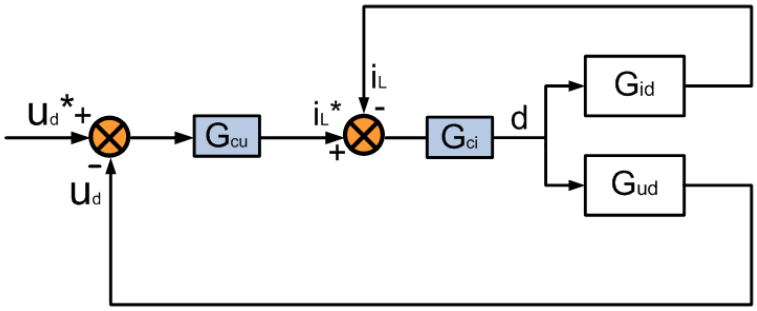


Figure 2-24 H-bridge control system schematic

Figure 2-24 shows the control topology for the two loops, the transfer function from the current reference to the dc bus voltage can be expressed in (2-47) according to the mason equation.

$$G_{ui} = \frac{u_d}{i_L^*} = \frac{G_{ci}G_{ud}}{1 + G_{ci}G_{id}} \tag{2-47}$$

The outer loop compensator is also a PI controller.

C. Auxiliary Inductance Selection

As mentioned above, the auxiliary circuit works in DCM, and the auxiliary inductor is the ripple energy transfer component. There are two criteria for selecting the auxiliary inductance L_s: The first criterion is the DCM limit, and the second criterion is the peak current limit.

As shown in Figure 2-15, in order to maintain DCM operation, which means t1+t2$\leq T_s$, the auxiliary inductor selection limit can be calculated as:

$$L \leq \frac{T_s}{2 \cdot \bar{i}_{cs}} \cdot \frac{U_d U_{cs} - U_{cs}^2}{U_d} \tag{2-48}$$

Equation (2-48) indicates that, with a certain switching frequency, the inductance should be smaller than a certain value to make sure the circuit works in the DCM range.

Meanwhile, the auxiliary circuit has one phase leg, which has the maximum current rating requirement. As shown in Figure 2-15, the peak current value in the buck charging phase and boost discharging phase can be expressed as:

$$Buck\_slope \cdot D1 \cdot T_s \leq I_{peak} \tag{2-49}$$

$$Boost\_slope \cdot D1 \cdot T_s \leq I_{peak} \tag{2-50}$$

Then the auxiliary inductor selection limit based on the peak current requirement is calculated as (2-51). The auxiliary inductance needs to be bigger than a certain value to make sure the peak current is lower than the requirement.

$$L \geq \frac{2 \cdot \bar{i}_{cs} \cdot T_s}{I_{peak}^2} \cdot \frac{U_d U_{cs} - U_{cs}^2}{U_d} \tag{2-51}$$

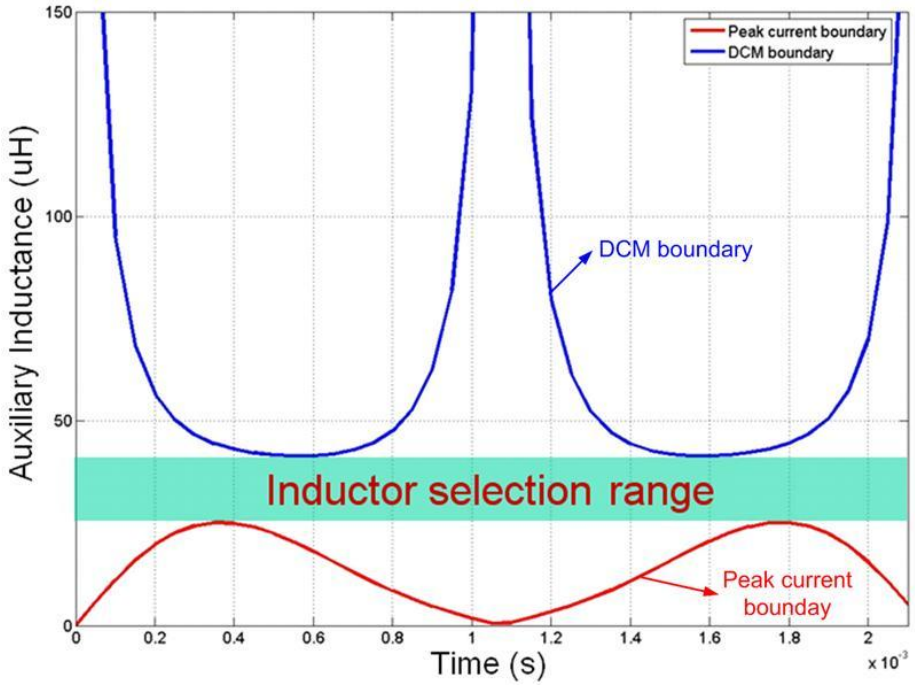
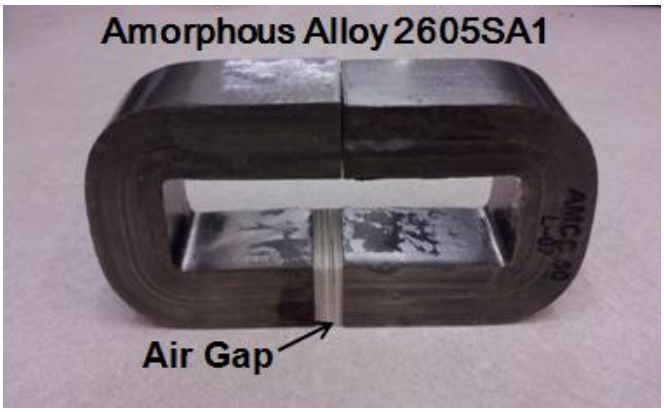


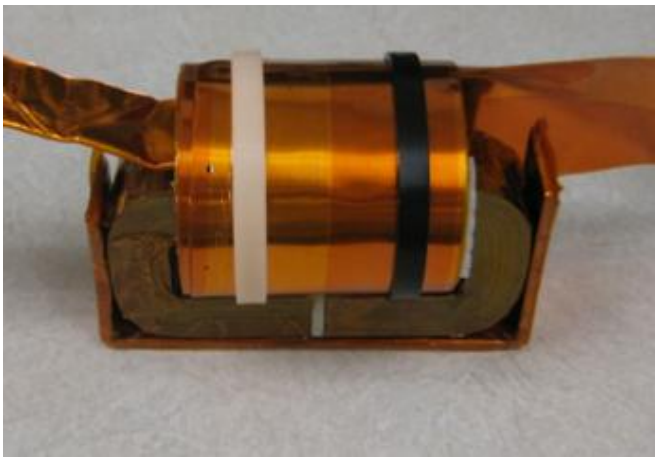
Figure 2-25 Auxiliary inductor selection.

Using (2-48) and (2-51), the auxiliary inductor selection range is plotted in Figure 2-25. The auxiliary inductance is selected as 45 μH in the system with the 20 kHz switching frequency and 200 A peak current rating considerations.

Copper foil is utilized as the auxiliary inductor winding. Since the inner winding has the worst thermal dissipation performance, asymmetrical air-gap structure is utilized to fabricate the auxiliary inductor in order to conduct better thermal distribution. As shown in Figure 2-26 (a), the air-gap only exists on one leg of the amorphous CC core. Copper foil winding is winded on the leg without air-gap to reduce the inner eddy current. The fabricated inductor is shown in Figure 2-26 (b). By using the asymmetrical design, the hot spot temperature (inner winding) can decrease from 249˚C to 164˚C compared with symmetrical design. It has been verified from the 15kW full power test, which is shown in Section 2.6.



(a) Fabricated asymmetrical air-gap core with amorphous alloy



(b) Fabricated copper foil winding auxiliary inductor with asymmetrical air-gap

Figure 2-26 Asymmetrical air-gap core design

D. Phase Lock Loop Control

Figure 2-27 shows the single phase phase lock loop control schematic diagram.

With assumption that:

$$U_s^*(t) = A \cdot \sin(\theta + \phi) \tag{2-52}$$

ϕ is the difference angle between the input signal and output signal.

Then, the error can be expressed as:

$$V_e = A \cdot \sin(\theta + \phi) \cdot \cos\theta - \sin\theta \cdot \cos\theta \tag{2-53}$$

Rewrite (2-53) in another form, the error can be expressed as:

$$V_e = \sqrt{\frac{(A\cdot\cos\phi - 1)^2}{4} + \frac{A^2\cdot\sin^2\phi}{4}}\sin(2\theta + \psi) + \frac{A\cdot\sin\phi}{2} \qquad (2\text{-}54)$$

Where $\psi = \arctan(\frac{A\cdot\cos\phi - 1}{A\cdot\sin\phi})$

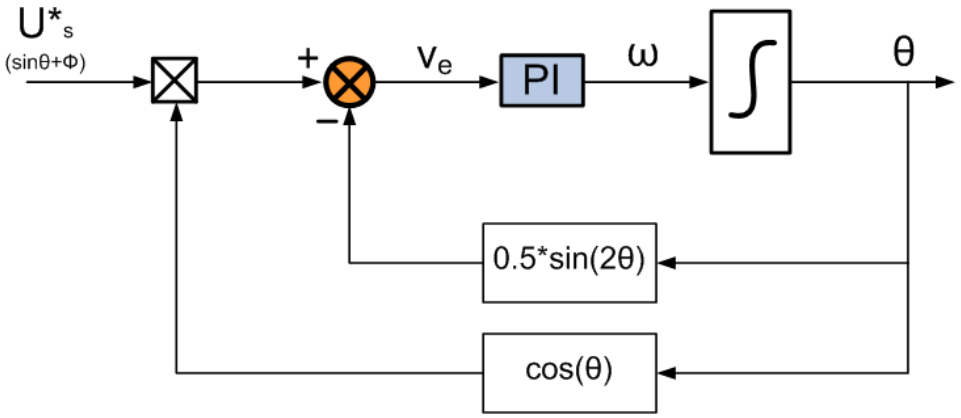
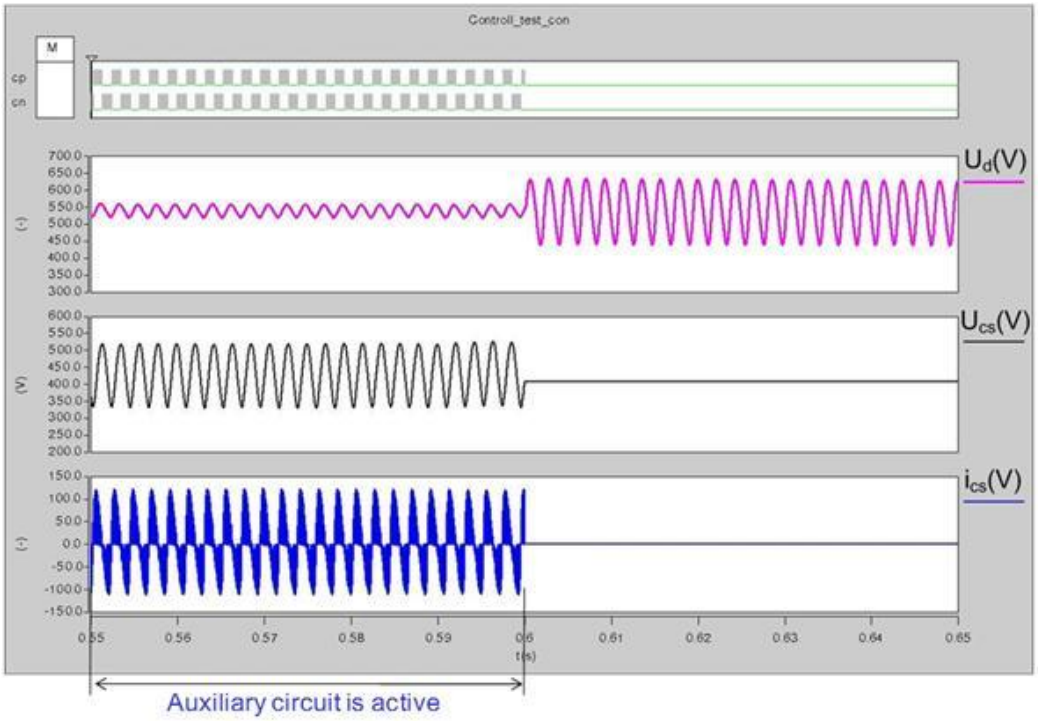


Figure 2-27 Phase lock loop control schematic

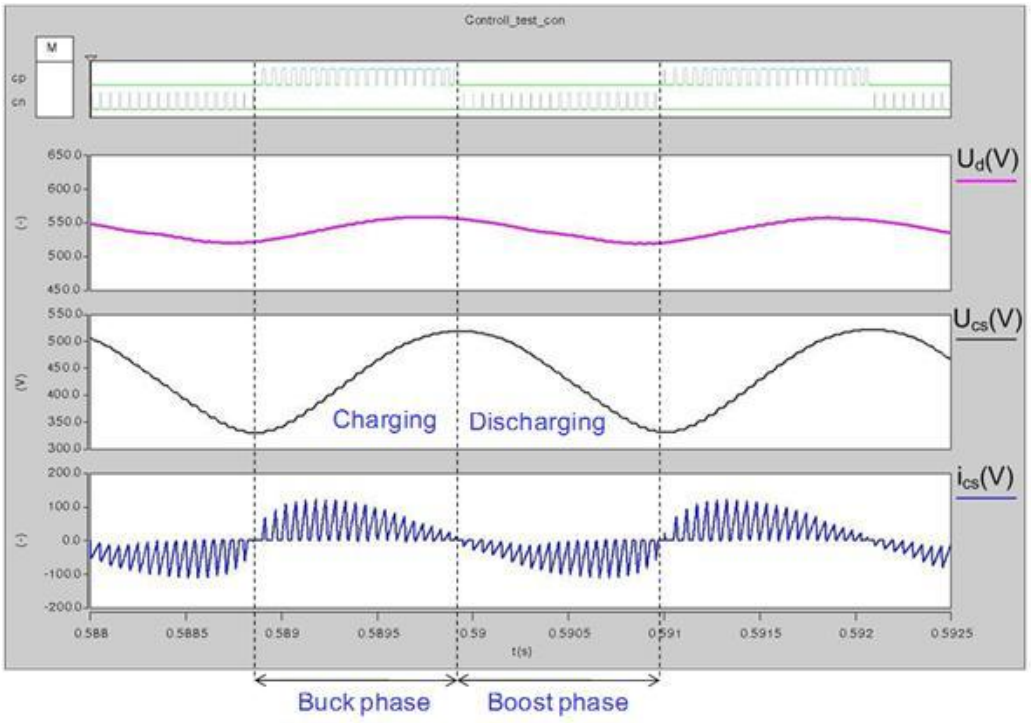
There are two parts in (2-54). The first part is the sinusoidal part, which is an ac component and the second part is a dc component. AC component will be eliminated by the low pass filter component. The dc component will generate a negtive feedback, which will helps to eliminate the error.

2.5.4 Simulation results

The simulation parameters of a single phase PWM rectifier are the same as those summarized in Table 1-2. As mentioned in the previous section, the auxiliary capacitor C_s is selected to be 200 μF, which is larger than the optimum value of 125 μF. The dc bus capacitor C_d is 140 μF, and the auxiliary inductor L_s is 45 μH. By using Synopsys Saber as a simulation tool, the ripple energy from the ac side of the H-bridge rectifier was verified to be effectively stored in the auxiliary capacitor C_s.



(a) Simulation waveforms



(b) Simulation waveforms when the auxiliary circuit is active

Figure 2-28 Simulation waveforms with active ripple energy storage.

As shown in Figure 2-28, the top two digital signals are the gate signals for the auxiliary circuit switch S5 and S6. During the buck charging phase, S5 switches and

S6 is turned off. During the boost discharging phase, S6 switches and S5 is turned off. The dc bus voltage, auxiliary capacitor voltage and auxiliary capacitor current are also shown in Figure 2-28. Before 0.6 s, the auxiliary circuit is active, and most of the ripple energy is stored in the auxiliary energy storage capacitor. Under this condition, the dc bus voltage ripple is within the required 2 % limit, even with a 140 μF auxiliary energy storage capacitance; using the conventional method, 1.6 mF was needed to meet the same requirement. The voltage ripple of the auxiliary capacitor is between 300 V and 500 V. The auxiliary circuit is controlled such that it works in DCM. After 0.6 s, the auxiliary circuit is inactive. Since most of the ripple energy goes to the small dc bus capacitor, a large dc bus voltage ripple can be observed.

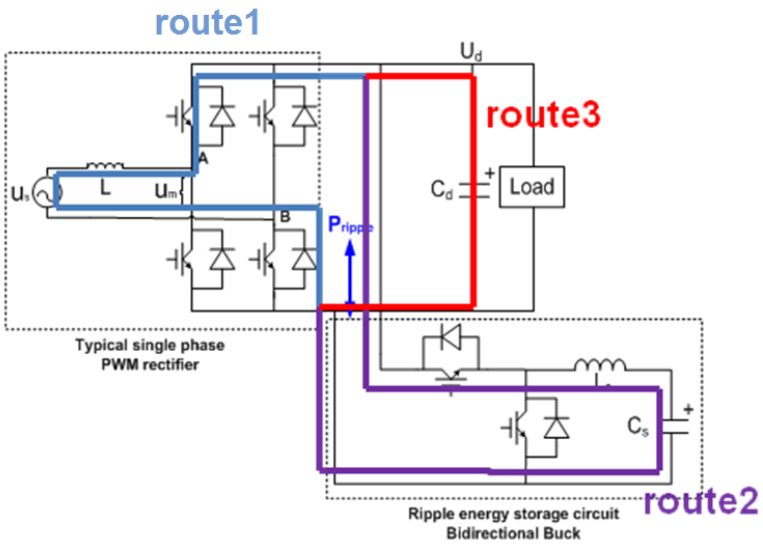


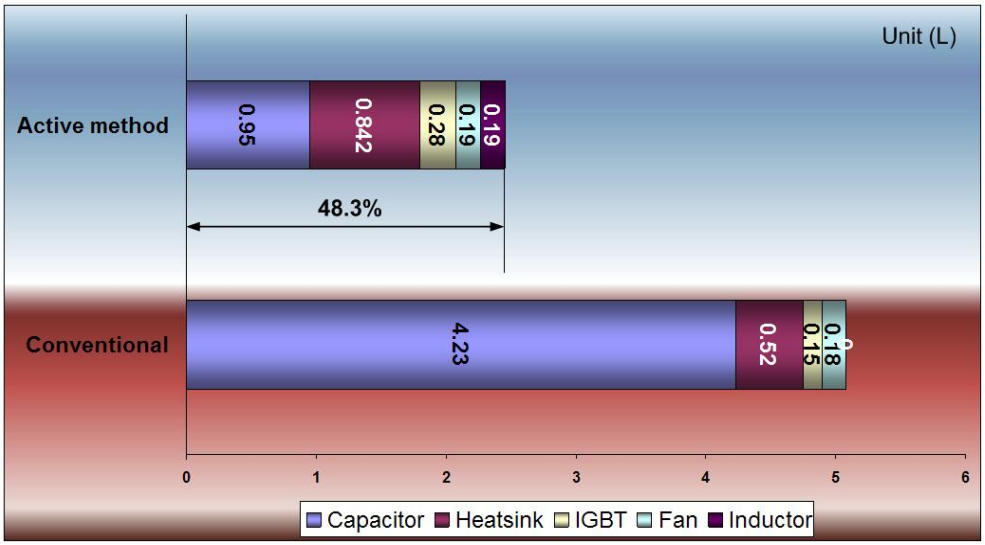
Figure 2-29 Different paths for the current ripple in the system.

As mentioned above, with a given voltage rating, both the capacitance and current rating influence the selection of the capacitor. From Figure 2-29, only the low-frequency current comparison between the traditional method and the active method is analyzed. Once the active method topology and control method are fixed, a current rating comparison can be conducted between the traditional method and the active method for the total current, including the high-frequency component. As shown in

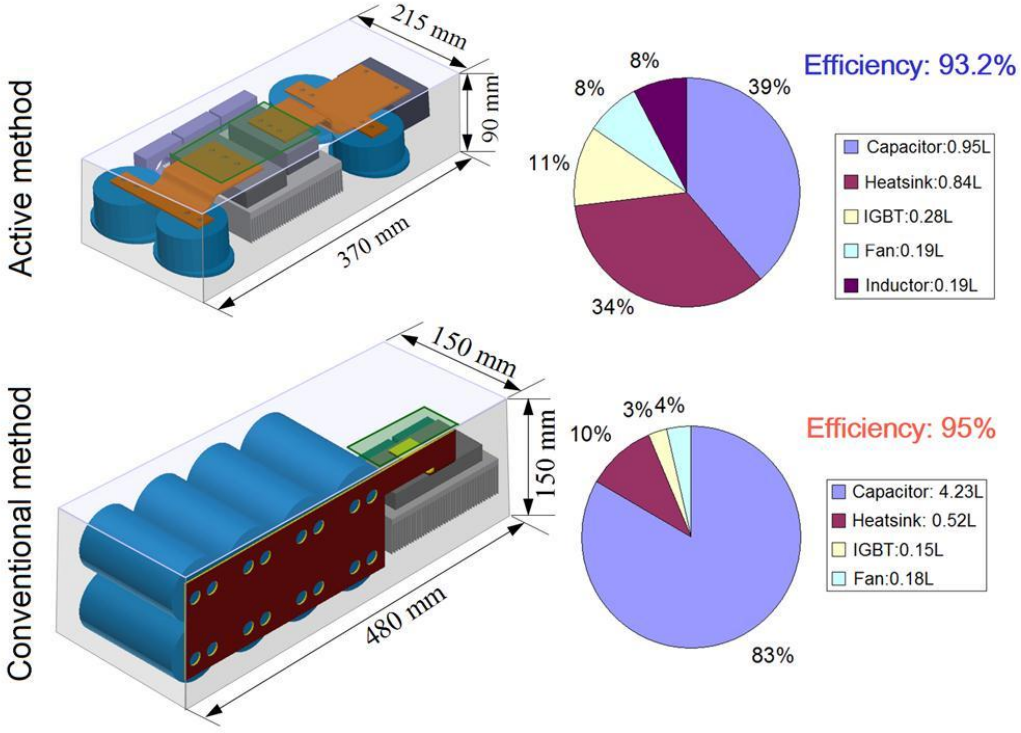
Figure 2-29, there are three current paths in this system. Current path 1 corresponds to the current coming from the H-bridge rectifier. It is composed of two parts; the dc current that feeds the load and the ac ripple current. The ac ripple current coming from the H-bridge rectifier is named as i_{cb}. For the traditional method, the i_{cb} goes to the dc bus capacitor. Current i_{cb} is also composed of two parts; the second-order low-frequency part and the high-frequency part. The current path 2 corresponds to the current coming from the auxiliary circuit. It also contains a low-frequency part and a high-frequency part. According to our control target, the low-frequency current that comes from the auxiliary circuit will compensate the low-frequency current that comes from the H-bridge rectifier, so that no low-frequency current will go to the dc bus. Because both path 1 and path 2 include an inductor, which can be considered to be high impedance for the high-frequency current ripple, the high-frequency ripple currents generated from path 1 and path 2 will go to path 3, which is the dc bus capacitor. With this active ripple energy storage method, the ripple current coming from the H-bridge rectifier, the auxiliary capacitor ripple current, and the dc bus capacitor ripple current are summarized in Table 2-4. The capacitor ripple current can be derived from simulation or calculation [115]. The traditional method would use a 1.6mF capacitor in the dc bus, which has a current rating of 57 A. The active method can split the 1.6 mF capacitor into two smaller capacitors, the 200 μF C_s and 140 μF C_d. The RMS current of these two capacitors are 58.2 A and 62.6 A, respectively. The total RMS current, including the high-frequency part, is also almost double that of the traditional method.

Table 2-4 RIPPLE CURRENT COMPARISON

	ic_b	ic_d	ic_s
Ripple Current (A,RMS)	57	62.6	58.2



(a) Main components volume comparison



(b) System layout comparison

Figure 2-30 Main component volume and system layout comparison between the active method and the conventional method.

A real design is conducted first, and a comparison of the volume of the main components in the conventional method and the active method is summarized in Figure 2-30 (a). By using the active method to store the ripple energy in a more

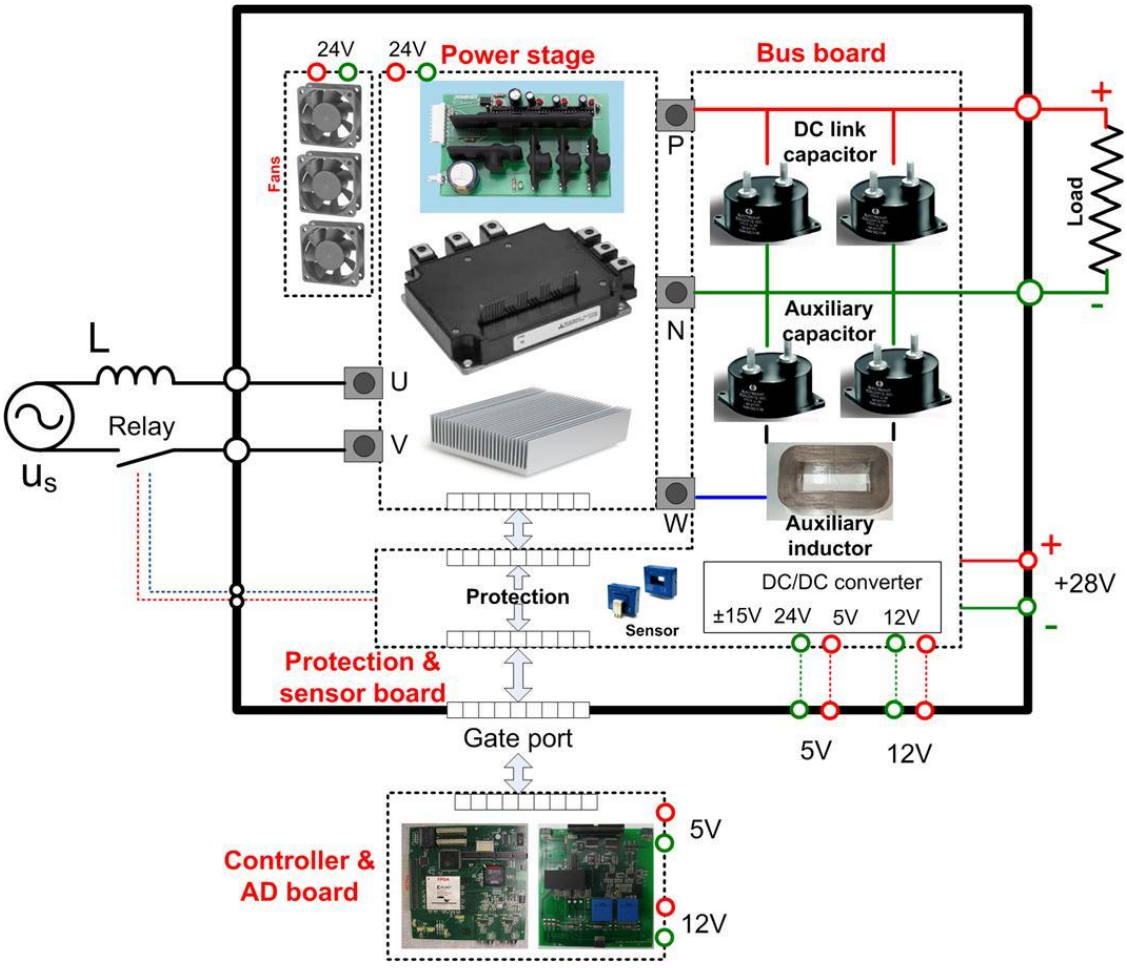
effective way, the volume of the energy storage capacitor significantly decreases from 4.23 L to 0.95 L. The auxiliary circuit, however, increases the system losses, which in turn increases the heatsink volume. An additional inductor and a larger switch component are needed in the active method as well. As a consequence, the whole system volume decreases to 48.3 % of the volume of the conventional method.

Figure 2-30 (b) illustrates the layout design and the volume of the main components by percentage for both the conventional method and the active method. The ratio of the capacitors to the whole volume can decrease from 83% to 39%. Because of the auxiliary circuit used in the active method, the active method has an estimated efficiency of almost 1.8 % lower than the traditional method. For a further increase of the system power density, some other methods should be considered, such as special and thermal design [116-118]. This chapter focuses on the dc bus capacitor reduction.

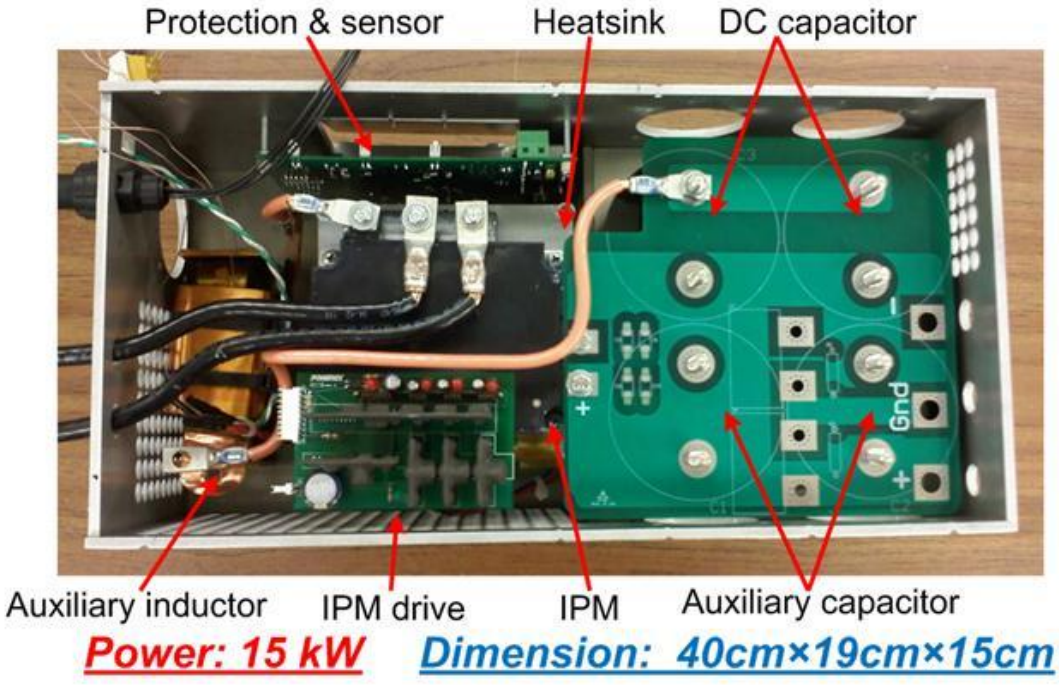
2.6 15kW Prototype Design and Experimental Results

A 15 kW prototype was built to verify the proposed active ripple energy storage method. The hardware design structure is shown in Figure 2-31 (a). A 5th generation CSTBT (carrier-stored trench gate bipolar transistor) IGBT three-phase intelligent power module (IPM) PM150CLA120 from Powerex is used as the active components in our system. The power rating of the IPM is 1200 V, 150 A. Two phases are used as the H-bridge rectifier, and the third is used as the auxiliary circuit. A pin-type heatsink and required fans from Cool Innovations were selected as the cooling system. The heatsink design is based on the IGBT loss calculation [119]. Because of the high saturation flux offered by amorphous materials, an amorphous core 2605SA2 from Metglas was selected to build a 45 μH auxiliary inductor. Since the inductor current is not purely sinusoidal, an improved Steinmetz equation is used to calculate the core loss [120]. Two 100 μF film capacitors UL31N107K from Electronics Concepts were

selected for the auxiliary capacitor C_s, and another two 100 μF film capacitors UL31N107K were used to filter the high-frequency ripple current as the dc bus capacitor C_d. The total current rating of two 100 μF film capacitors is 92 A at 85° C, which is higher than the required 60 A. A four-layer bus board was used to provide a connection for the components to the dc bus, and a protection and sensor board was used to provide auxiliary power, voltage and current sensing, and over-current and over-voltage protections. Figure 2-31 (b) is a picture of the 15 kW prototype.



(a). System hardware design structure



(b)15 kW prototype picture

Figure 2-31 Experiment setup built.

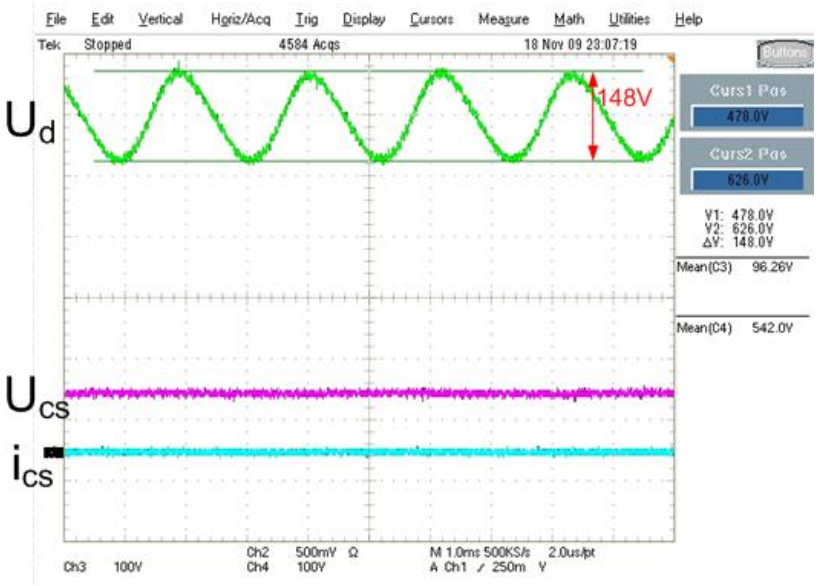
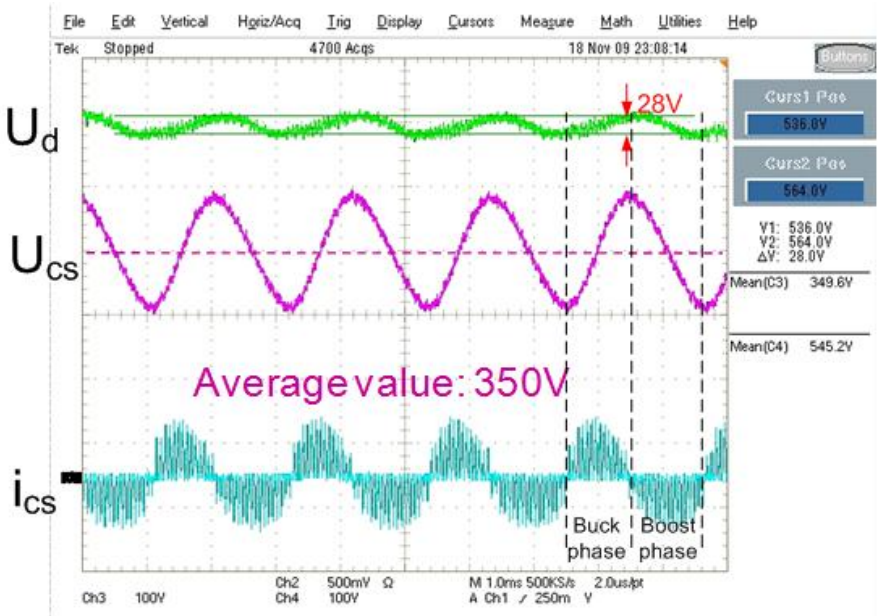


Figure 2-32 Experiment waveforms without active ripple energy storage method.

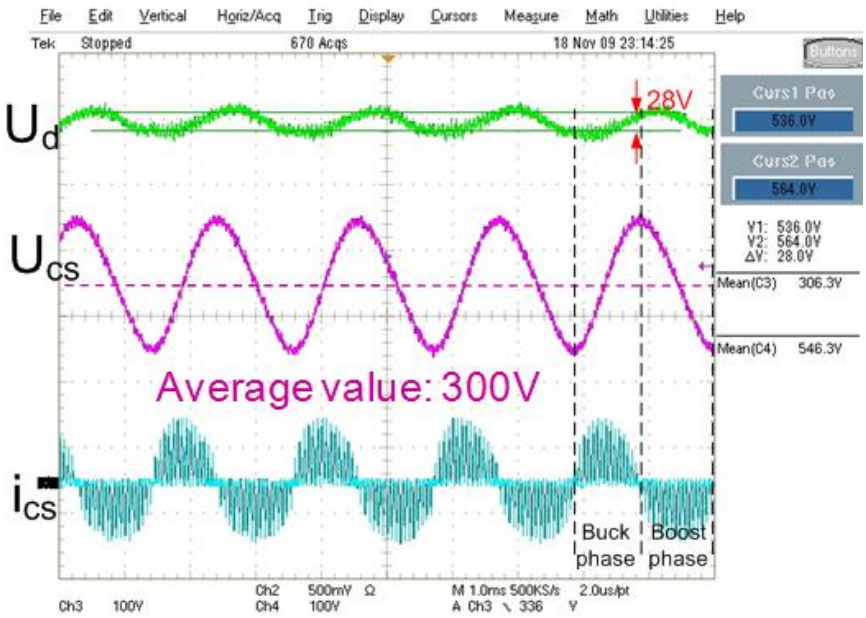
Figure 2-32 shows the test results of a 15 kW single-phase PWM rectifier without the active ripple energy storage method. The dc bus voltage is controlled as 540 V by an H-bridge rectifier. Because only a small dc bus capacitor of 200 μF is put in the dc

bus, the majority of the ripple energy goes to the dc bus capacitor, which leads to 148 V peak-to-peak voltage ripple. This huge voltage ripple will push the peak voltage of the dc bus goes to almost 630 V, which will also increase the components' voltage stress.

If the active ripple energy storage method is implemented, as shown in Figure 2-33, the auxiliary capacitor voltage fluctuates within a huge range to store most of the ripple energy, and the dc bus peak to peak voltage ripple decreases from 148 V to 28 V. The mean value of the auxiliary capacitor voltage is controlled by another voltage control loop, which is 350 V in Figure 2-33 (a) and 300 V in Figure 2-33 (b). We can also observe that the auxiliary capacitor voltage ripple and the auxiliary capacitor current i_{Cs} in Figure 2-33 (a) is smaller than in Figure 2-33 (b). This can be explained by Figure 2-10. The higher coefficient k will lead to a higher average auxiliary capacitor voltage, a smaller voltage ripple and smaller auxiliary capacitor current.



(a) The average auxiliary capacitor voltage (350 V)



(b) The average auxiliary capacitor voltage (300 V)

Figure 2-33 Experiment waveforms with active ripple energy storage method.

Figure 2-34 shows the auxiliary capacitor current, and its reference is indicated by the red dashed line. The auxiliary circuit is controlled in DCM. The peak current is controlled to be less than 150 A, which keeps roughly the same current rating as the H-bridge rectifier.

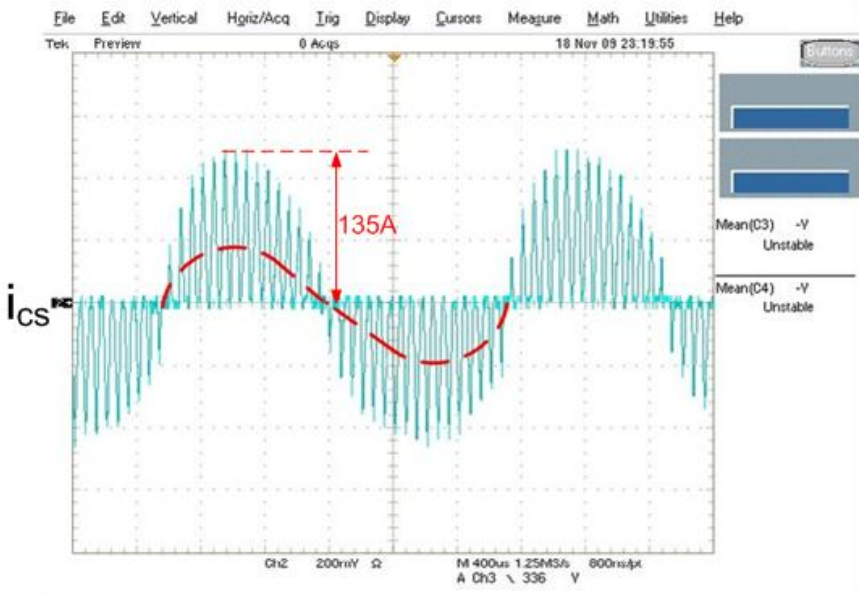


Figure 2-34 Auxiliary capacitor current and reference.

2.7 Conclusions

The barrier to high power density for a single-phase rectifier is its passive component required to filter the second-order ripple energy. This chapter analytically determines the minimum ripple energy storage requirement for single-phase PWM rectifiers is a function of different factors. Based on the ripple energy requirement, we have verified the feasibility of decreasing the dc bus capacitor volume using an active method, rather than the conventional method, that stores the ripple energy in the dc bus capacitor. Then, an active ripple energy storage method using an auxiliary bidirectional buck-boost circuit was proposed to illustrate the dc bus reduction concept. This active method can help to increase the single-phase PWM rectifier power density by 100 %. Meanwhile, the active method is easy to implement, and there is no high voltage in the system. Simulation and 15 kW experimental tests were conducted for verification purposes.

Chapter 3. High Temperature SiC Three-Phase PWM Rectifier Design for >150°C Ambient Temperature

This chapter describes a detailed design process for a high-temperature SiC three-phase PWM rectifier that can operate at ambient temperatures above 150°C. SiC high-temperature hybrid structure packaging is designed for the main semiconductor devices and an edge-triggered high-temperature gate drive is also proposed to drive the designed power module. The system is designed to make use of available high-temperature components, including the passive components, silicon-on-insulator chips and auxiliary components. Finally, a 1.4 kW lab prototype is tested in a harsh environment for verification.

3.1 Introduction

High-temperature (HT) converters have become more and more important in industrial applications where the converter operates in a harsh environment, such as hybrid electrical vehicles, aviation, and deep earth petroleum exploration [16-18]. Compared to traditional silicon (Si) devices, new wideband gap devices, made of materials such as silicon carbide (SiC) or gallium nitride (GaN) , provide a much higher bandgap, thermal conductivity and breakdown fields, which offers them the potential capability to overcome the temperature, frequency and power management limitations of Si devices. Several publications have shown that SiC devices have the capability to decrease loss and increase the device junction temperature, which will result in higher efficiency, a lighter cooling system and higher power density [38, 55,

119]. To fully utilize the SiC device's high-temperature tolerance and fast-switching capability, a reliable high-temperature packaging method is desired that will also allow the SiC based module to achieve smaller parasitic.

Meanwhile, the harsh environment of some applications require not only a high-temperature semiconductor power module, but also high-temperature gate drive circuits, high-temperature control electronics, high-temperature passive components and the like that are able to operate in these environments. These sub-functions of the converter need to be reliably designed with the limited selection of high-temperature components that are available.

This chapter presents the design process of a high-temperature SiC three-phase AC/DC PWM rectifier that can operate in ambient temperatures above 150 °C and an SiC power module that can work with a 250 °C junction temperature. With consideration of material availability, SiC diodes and JFETs are used as the main circuit devices and are packaged in a novel high-temperature hybrid structure. Besides the high-temperature SiC power module, a high-temperature transformer-isolated gate drive circuit is also proposed. Other functions such as the harmonic filter and the control system–including protection and sensor functions are designed according to the available high-temperature silicon-on–insulator (SOI) ICs and high-temperature passive components.

Because of both the simple topology and the simple control, a typical single-switch three-phase boost PFC circuit [120] is used to demonstrate the concept of high-temperature converter design. The structure and topology for the three-phase AC/DC rectifier is shown in Figure 3-1. The power module is composed of seven SiC diodes and one normally-on SiC JFET. The first six diodes are utilized as a diode rectifier stage, and another diode and JFET make up the second boost stage. The input voltage

is lower than 100V (rms/phase), and the output voltage is regulated to 270V. The system's power rating is 1.4kW for CCM mode and 500W for DCM mode.

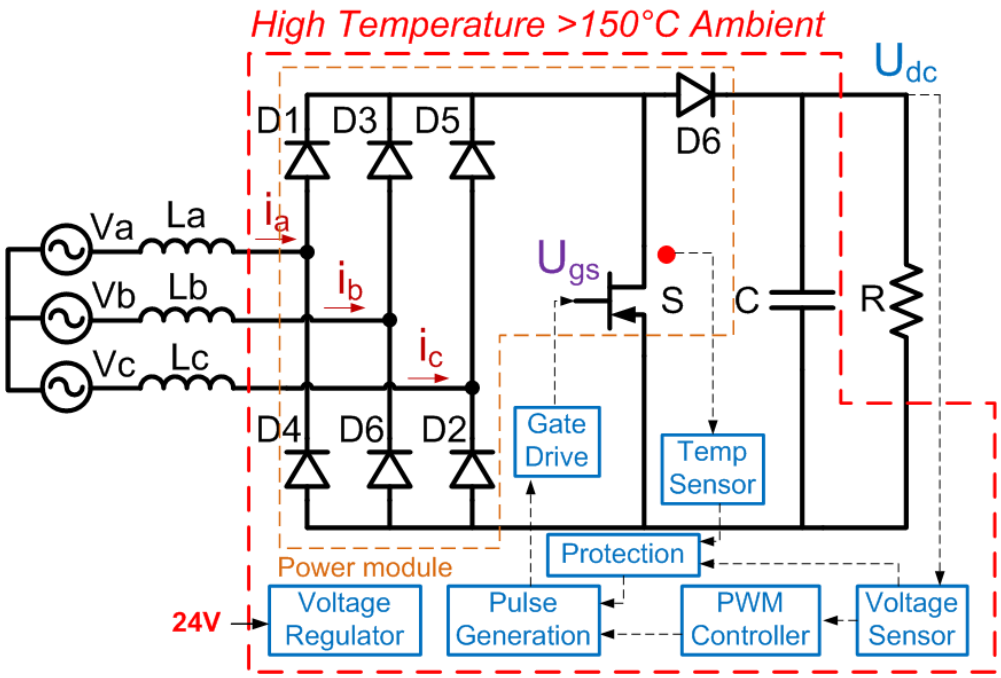


Figure 3-1 System Topology and Configuration

This chapter is organized as follows: Section 3.1 has provided the general topology of the proposed system and an introduction to the motivation behind this work; Section 3.2 describes the high-temperature hybrid structure packaging for the multiple-chips power module; Section 3.3 presents the surveyed high-temperature components besides the power module; Section 3.4 proposes the high-temperature gate drive design for both single switch and phase leg; Section 3.5 gives the detailed high-temperature system design process; Section 3.6 provides the high-temperature converter experimental results and discussion; and finally, Section 3.7 shows the conclusions drawn from this work.

3.2 A Novel Hybrid Packaging Structure for High-Temperature SiC Power Modules

Higher switching frequency and higher junction temperature capability help to reduce the sizes of the passive components and the cooling system, and to increase the power density [60]. In recent years, SiC devices have become more and more attractive and are offering the potential to overcome temperature, frequency and power management limitations of Si devices [121, 122]. However, a reliable high-temperature packaging method that entails smaller parasitic is desired to fully utilize the SiC devices high temperature and high frequency capability. Wirebond packaging structure [17, 44, 63-65] is widely utilized in industrial applications with the advantages of easy fabrication, high maturity and reliable connection. However, the traditional wirebond packaging structure also suffer from the disadvantages of large footprint and parasitic, which will constrain the SiC device high switching speed capability. Compared with wirebond packaging structure, the planar packaging structure has several advantages such as smaller footprint, smaller parasitic parameters, more flexible routing, and also double-side cooling capability [69-71]. However, this structure is also faced with challenges, like the connections of small top pads, the alignment of interconnections, limited choices for die attachment materials, and a complicated and time-consuming manufacturing process [69, 70]. In addition, since double-side solderable devices are generally not available, one of the way to use regular devices in the planar structure is to plate the top pads with solderable metals. Figure 3-2 shows the top pads of a SiC JFET and a SiC diode with electroplated silver. Because the top aluminum layer is very thin, the plating reliability is poor, which easily leads to the silver layer peeled off or loosely plated. This is the biggest challenge in the planar structure packaging. To resolve this, this section presents a novel hybrid packaging structure for high-temperature SiC power modules that combines the benefits of both the wirebond and planar packaging structure. With this

new structure, the power module can achieve the same footprint and similar parasitic as the planar structure without topside metallization. In addition, a more flexible die-attach material selection is possible and the processing complexity and time are reduced.

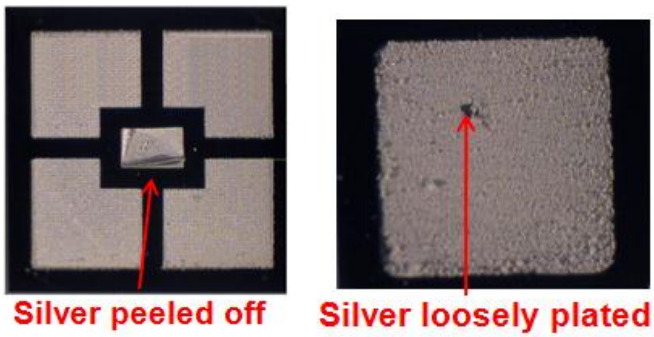
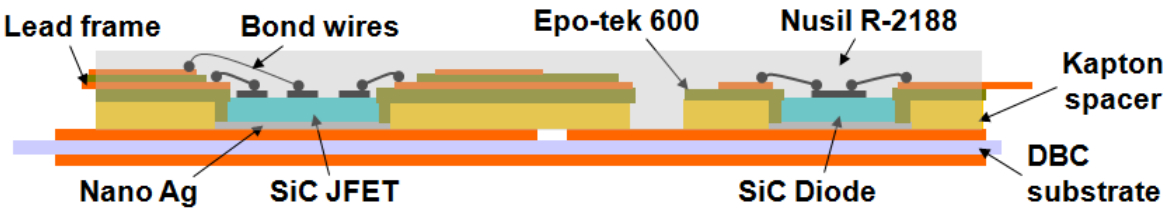


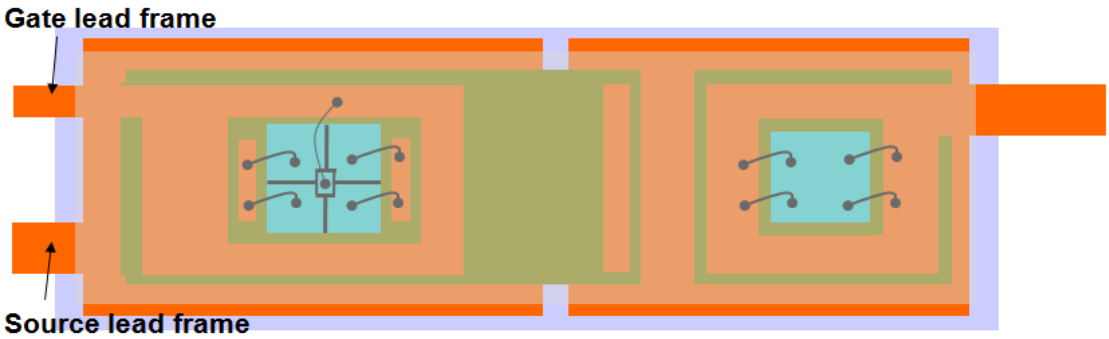
Figure 3-2 Plated SiC JFET and SiC Diode

3.2.1 Hybrid Structure and Fabrication Process

The cross-sectional and the top views of the hybrid structure for a single JFET and diode are shown in Figure 3-3 to demonstrate the basic idea. The bottom drain pad and cathode pad of the JFET and the diode are sintered on the DBC with die attachment material. Separated by the spacer and the insulation layer, the source and anode lead-frames are attached above the substrate with windows in the middle for the die wirebonding. The gate lead-frame of the JFET is attached above the source frame, separated by another insulation layer. Interconnections between the top pads and the source, gate and anode lead-frames are provided by wirebonding. An encapsulant layer covers the top of the module. This hybrid structure keeps the basic planar structure but with the top-side interconnection replaced with wirebonding, which doesn't require double-side solderable devices.



(a) Cross-sectional view



(b) Top view

Figure 3-3 Hybrid structure packaging

In order to utilize this hybrid structure packaging in the high temperature application, proper high temperature devices or materials selection becomes critical. As shown above, the SiC devices have a theoretical junction temperature limit much higher than typical silicon devices. Since the SiC JFETs are the first available SiC devices on the market, most of the surveyed works demonstrate the SiC JFETs devices high temperature capability. Besides the SiC JFETs based papers, there are also papers that demonstrate the SiC MOSFET, SiC BJT and SiC IGBT. With consideration of reliability and availability when this research was conducted, SiC JFETs from SiCed is selected as the active devices.

Besides the high temperature power semiconductor devices, other high temperature packaging materials are selected and shown below.

Direct Bond Copper (DBC) substrates usually provide support for mechanical, electrical and thermal. The candidate material for DBC substrates is listed in Table 3-1. Compared with alumina (Al_2O_3), aluminum nitride (AlN) and silicon

nitride(Si_3N_4) have smaller coefficient of thermal expansion (CTE) that can match better with SiC devices (CTE=3). Considering the highest thermal conductivity, ease of processing and lower cost, the AlN is selected. However, for high current applications that need to employ more copper thickness, Si_3N_4 will be a good candidate because of the high flexural strength, which will increase the DBC thermal reliability.

Table 3-1 Candidate materials for DBC substrate

Substrate	CTE (ppm/K)	Thermal Conductivity (W/m/K)	Tensile Strength (MPa)	Flexural Strength (MPa)
Al_2O_3	6.0	24	127.4	317
AlN	4.6	150-180	310	360
Si_3N_4	3.0	70	96	932

Besides the DBC material, solder for both lead based and gold based, silver glass and nano silver paste are summarized in Other materials selected for the prototype module are summarized in Table 3-3. All the materials are suitable for 250ºC operation.

Table 3-2 as candidates for high temperature die-attachment material. Ag glass may crack during the processing [123] that will reduce the reliability. Compared with high-temperature solder, the nano-silver paste [124] is selected for the die-attachment material for three reasons. First, the fixed processing temperature of nano-silver paste (275 ºC) is much lower than the high-temperature solder. Second, because the device top pads are much smaller, the nano-silver paste will keep its shape during the sintering process, which makes it easier to form the connection on the top of the device and provides more accurate alignment, which is very important in the hybrid

structure power module. Third, the nano-silver paste shows the highest thermal conductivity among all these candidates.

Other materials selected for the prototype module are summarized in Table 3-3. All the materials are suitable for 250ºC operation.

Table 3-2 Candidate materials for die-attachment

Different Materials	Processing Temp (°C)	Working temp (°C)	Thermal Conductivity (W/m/K)	CTE (ppm/K)
95%Pb 5%Sn	350	310	32	28
80%Au 20%Sn	320	280	57	16
80%Au 20%Ge	390	360	88	13
Hysol Ag glass	400	900	40	16
Sintered NanoAg	275	900	240	19

Table 3-3 Materials selection for the hybrid structure power module

SiC JFET	**1200V,3mm×3mm from SiCed**
SiC Diode	**1200V,2.7mm×2.7mm from SiCed**
Substrate	**AlN DBC (25 mils AlN, 8mils Cu)**
Encapsulant	**Nusil R-2188**
Die-attachment	**Nano-silver paste**
Spacer	**Kapton tape (2 mil)**
Insulation layer	**Epo-tek 600 or Duralco 128**
Bond wires	**Al (5mil, 10mil)**

For simplicity, the fabrication process with a single SiC JFET is shown in Figure 3-4. The patterned Kapton tape is attached to the DBC as both insulation and spacer layer. Then, the device is well positioned with the assistance of the spacers, and later attached to the DBC by sintering with nano-silver paste. In order to prevent the

electrical break down around the edges of the device, high temperature polyimide insulation material, Epo-tek 600 or Duralco 128 can be utilized to cover the device's guard rings and to fill the gaps between the spacer and the device. Then the source lead-frame is bonded to the spacer by curing polyimide in-between these two layers. In the next step, the second insulation layer is also formed by Epo-tek 600 or Duralco 128 on top of the source lead-frame, and the gate lead-frame layer is bonded by curing the polyimide again. Afterwards, the wirebonding process connects the top pads to the lead-frames. Finally, silicon gel Nusil R-2188 is selected as the encapsulant to cover the top of the module to protect the die and the bonding wires. In total, the hybrid packaging has one sintering step, two curing steps and one encapsulating step.

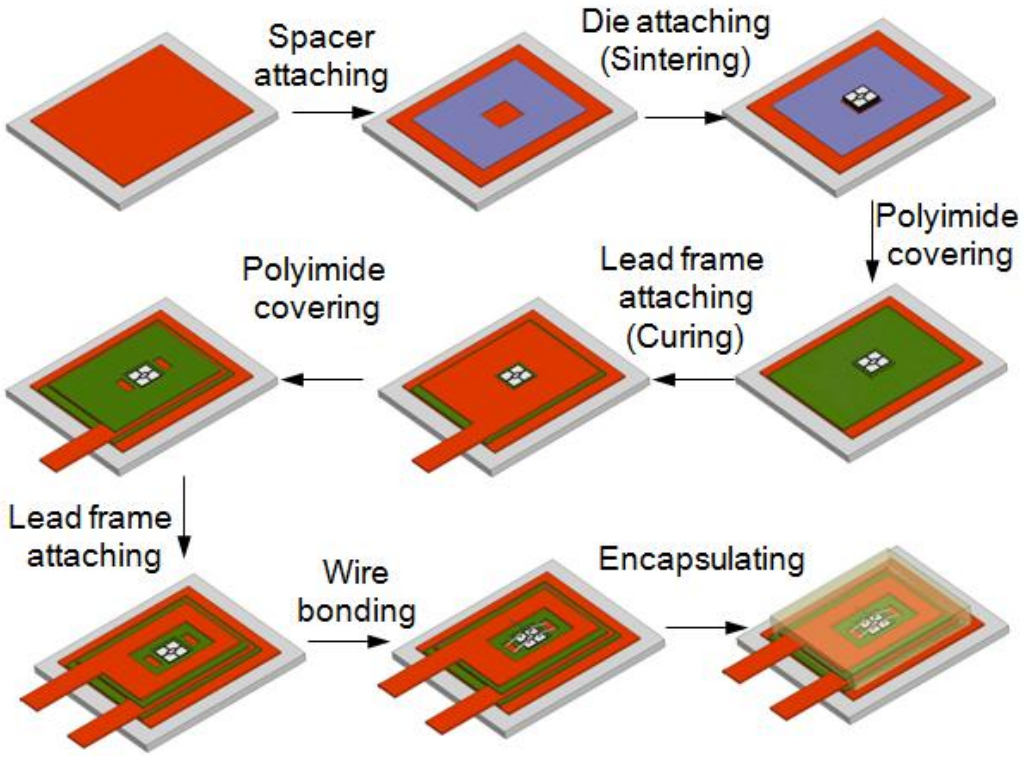


Figure 3-4 Hybrid structure packaging fabrication process

Figure 3-5 shows the prototype JFET module in hybrid structure. With the hybrid structure packaging, the lead frames are in three dimensions and the device top side is

connected to the lead frames with very short bonding wires. The static characterizations of the device show no visible change before and after the packaging.

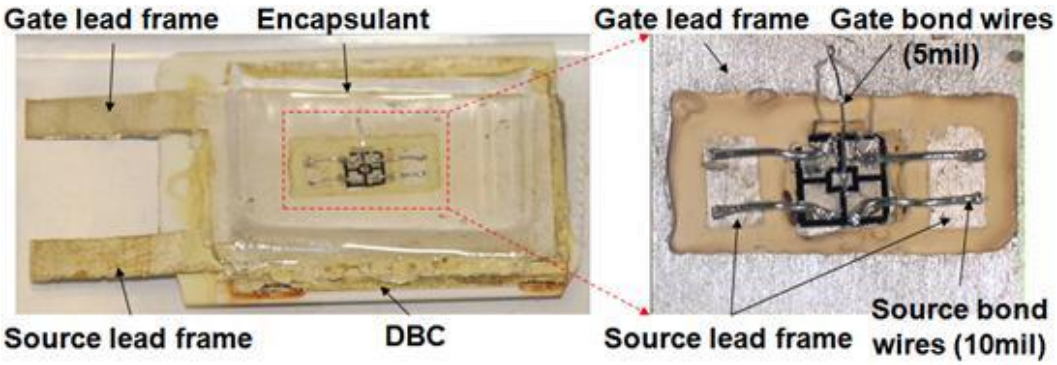


Figure 3-5 Hybrid structure SiC JFET module prototype

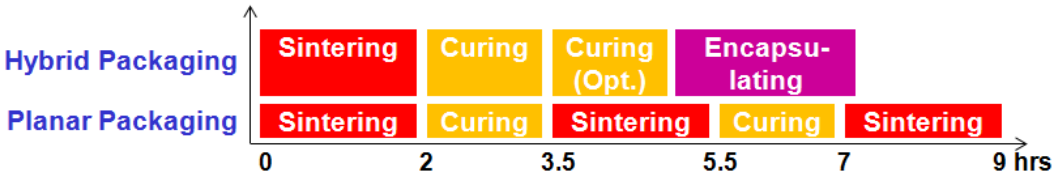


Figure 3-6 Processing time comparison results

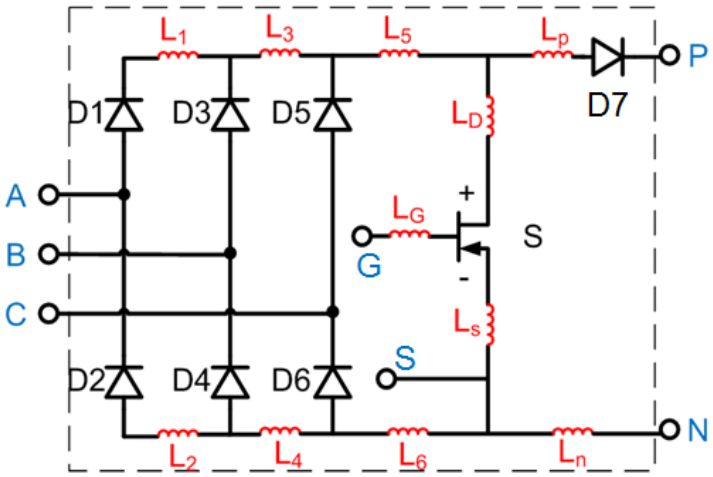
As shown in Figure 3-6, the processing time takes two hours less when compared with the planar structure [69, 70]. Besides, the planar packaging structure emploies the sintering process three times, and each process temperature must be at least 40°C lower than previous one to keep it from melting. This makes it difficult to select the die-attachment materials. However, since there is only one sintering process in the hybrid packaging structure, a more flexible die-attach material selection is possible.

3.2.2 Analysis and Comparisons of Parasitic Based on Multi-chip Power Module

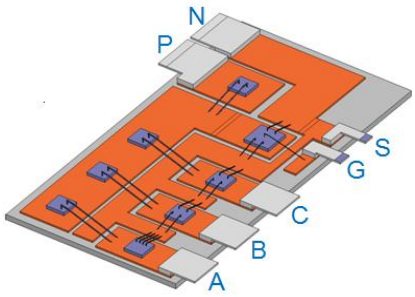
With the proposed hybrid structure packaging methodology, advantages of the smaller footprint and parasitic can be shown in the multiple chips power module. The three-phase single-switch rectifier [120] is used as an example to analyze the parasitic in multi-chip power module with different packaging structures. Figure 3-7 (a) shows

the system schematic. This circuit is composed of seven SiC diodes and one normally-on SiC JFET. The first six diodes are utilized as a diode rectifier stage, and another diode and JFET make up the second boost stage.

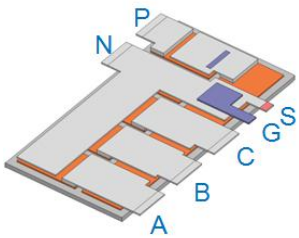
Figure 3-7 (b) to Figure 3-7 (d) show three different packaging structures. The traditional wirebond structure has the largest footprint. Because of the three dimentional layout for the lead frames, the hybrid structure has the same footprint as the planar structure and is 50% smaller than the wirebond structure.



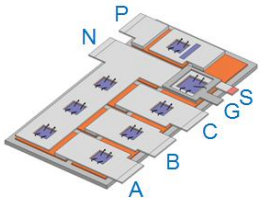
(a) System schematic



(b) Wirebond structure: 45×25×0.7mm3



(c) Planar structure: 35×18×0.7mm3



(d) Hybrid structure: 35×18×0.7mm3

Figure 3-7 Different packaging structure

The Ansoft Q3D software is used as the simulation tool to analyze the parasitic between different structures. The key parasitics [125]: gate loop inductance (L_G+L_S),

main loop inductance ($L_P+L_N+L_D+L_S$) and the common source inductance (L_S) are extracted and shown in Figure 3-8. The main loop inductance of the hybrid structure almost keeps the same as the planar structure owing to the same footprint. The reduced gate pad bonding wire compared with windbond structure will not only reduce the gate loop impedance but also reduce the coupling between the gate loop and the main loop, so the hybrid structure gate loop and the common source inductances are smaller than the wirebond structures.

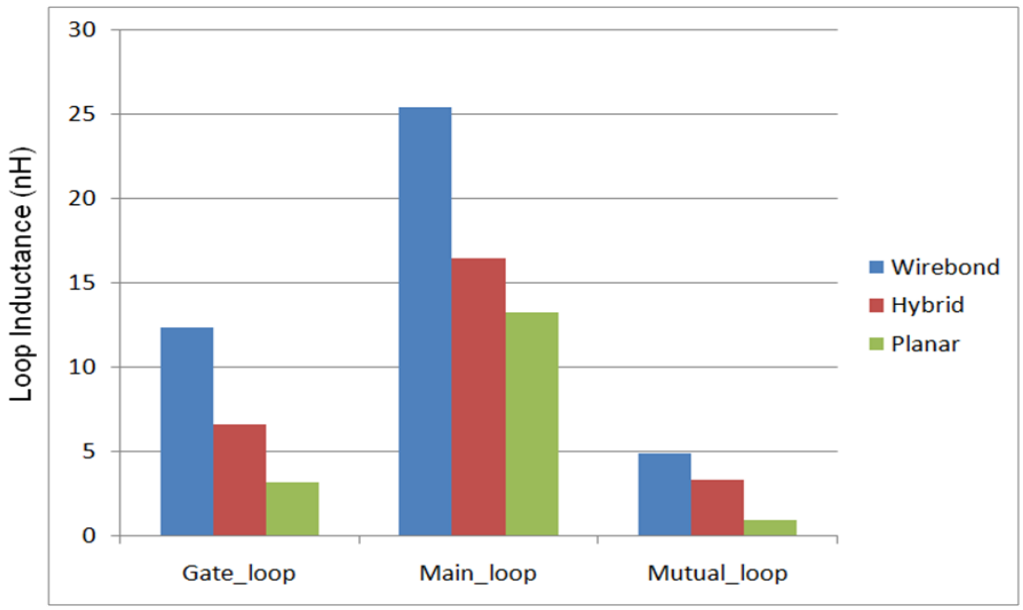


Figure 3-8 **Parasitic comparison results**

The three-phase single-switch rectifier is simulated in the Saber tool. The simulation system schematic and parameters are shown in Figure 3-21 and Table 3-5, which remain the same with the experimental results in the next section. The simulation results are shown in Figure 3-9. The input current is controlled in discontinuous current mode (DCM) and the peak value reaches 12A. The dc link voltage is regulated at 270V.

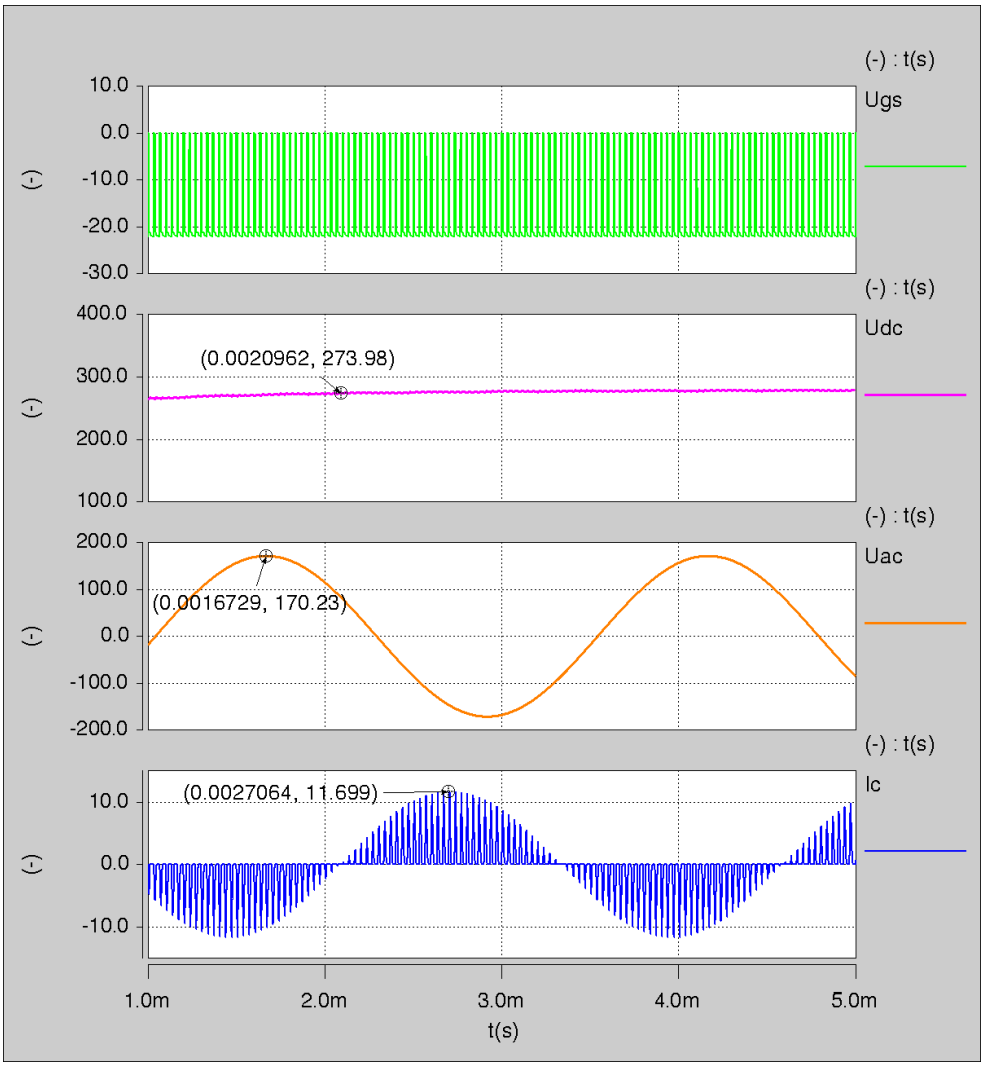


Figure 3-9 Simulation Waveforms in DCM mode

Since the system is working in DCM mode, the turn-on process occurs with soft switching and there is no turn-on switching loss for the JFET. The turn-off waveforms and the switch energy of the hybrid and wirebond structure are simulated and shown in Figure 3-10 with the relevant parasitic shown in Figure 3-8. According to the simulation, the switching waveforms are less sensitive to the gate-loop inductance than the other two loops because there is more damping existing in the gate loop, such as gate resistance and JFET internal gate resistance. However, the main loop and mutual loop inductance influence can be clearly seen from the Figure 3-10. The hybrid structure reduces the main loop inductanceto 16nH compared with 25nH in the wirebond structure, which reduces the JFET drain-source voltage spike from 305V to

289V. The reason for the decreased voltage stress can be analyzed in this paper [126] with a simple JFET turn off equivalent model as shown in Figure 3-11.

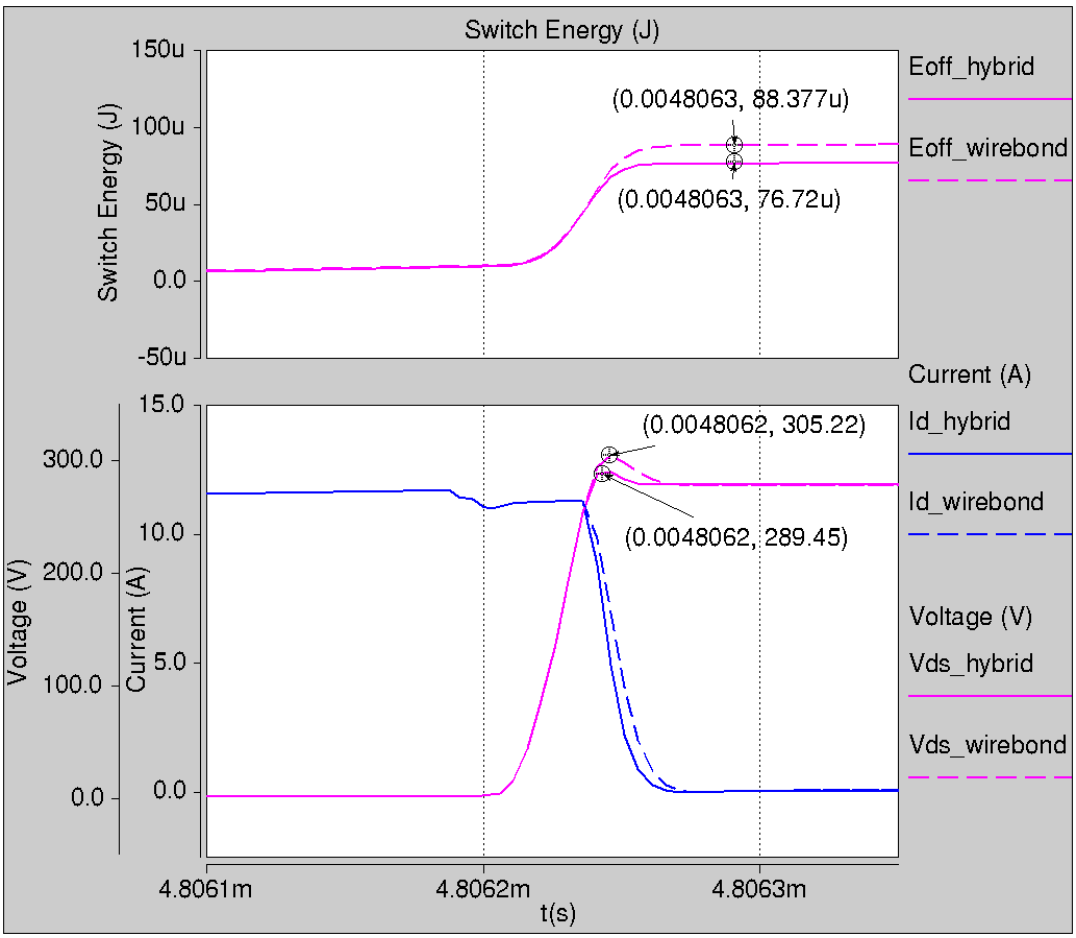


Figure 3-10 **Compared turn-off waveforms with different parasitic**

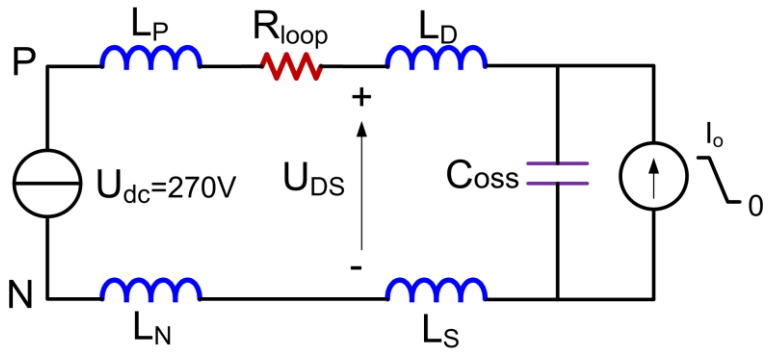


Figure 3-11 Model of the turn-off process

The calculation close loop equation for drain-source overvoltage can be expressed in (3-1).

$$\Delta V_{DS}(T_{peak}) = \frac{di}{dt}(L_P + L_N)\cdot[1 - \frac{1}{\sqrt{1-\xi^2}} e^{-\xi\omega_o T_{peak}} \sin(\omega_o \sqrt{1-\xi^2} T_{peak} + \psi)] \quad (3\text{-}1)$$

where, $L = L_P + L_N + L_D + L_S$, $\xi = R_{loop}\sqrt{C/L}/2$, $\omega_o = \frac{1}{\sqrt{LC}}$, $\psi = \arccos(\xi)$

The parameter study based on (3-1) can be depicted in Figure 3-12. Rloop=0.1Ω, Coss=100pF. By decreasing the main loop inductance from 25nH to 16nH, the peak drain-source overvoltage decreases from the 34V to 22V, which matches well with the simulation results.

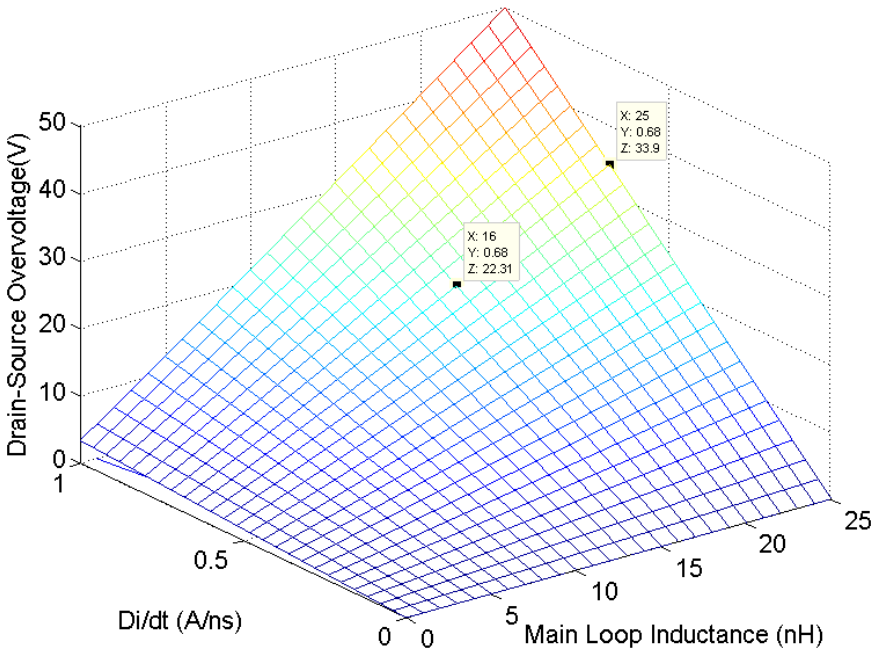


Figure 3-12 Drain-source overvoltage simulation results

Meanwhile, the reduced mutual loop inductance in the hybrid structure helps to increase the turn-off current speed compared with the wirebond structure. This can be explained by the negative feedback effect from the main loop to the gate loop. The voltage drop across the mutual inductance counteracts the change of the gate voltage during the drain current change, which slows it down a little bit [127]. Because of the reduced voltage spike and increased current speed, the hybrid structure decreases the

turn-off switch energy from 88.4μJ to 76.7 μJ compared with traditional wirebond structure.

3.2.3 Thermal Reliability Analysis

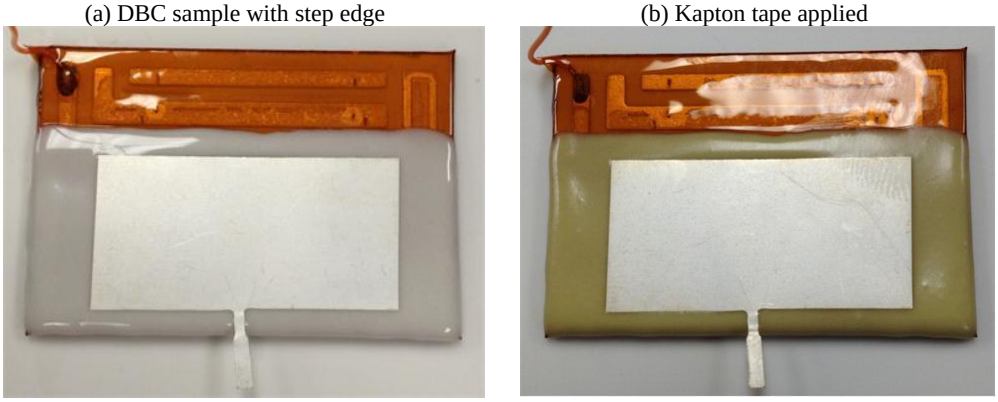
Die-attachment thermal reliability is a common concern for power modules. Since the nano-silver paste is selected as the die-attachment material, the nano-silver paste thermal reliability performance is critical to the whole module. Although no destructive test is directly applied to the hybrid structure power module, previous studies already demonstrate that nano-silver paste has good thermal reliability performance with respect to both the thermal cycling test and the thermal soaking test [128, 129]. Meanwhile, substrate thermal reliability is also a bottleneck for the high-temperature operation. By utilizing a sealed step edge for the copper, the peeling stress in the edge and corner of the substrate can be relieved [65]. In addition to these tests, thermal reliability tests were conducted with respect to the interconnection of different layers in the hybrid structure power module.

A Tenney TUJR thermal-cycling chamber is used to generate the thermal cycling condition. Figure 3-54 shows the thermal cycling temperature profile. The thermal cycling temperature ranges from -50°C to 200°C. Each cycle lasts for one hour, and the hot and cold temperature duration time is 13 minutes. The maximum slope we can achieve is roughly 20°C/min.

Nickel and silver plated step edge DBC substrates are utilized to build the samples to evaluate the interconnection reliability with thermal conductive epoxy (Duralco 128, ceramic based, 250°C) as an insulation layer between the DBC and the lead frame. The DBC sample shown in Figure 3-13 (a) has a similar size with the parasitic study multiple chips module shown in Figure 3-13 (c). The kapton tape is applied on top of the substrate. High temperature wire is soldered on the top left corner of the substrate

for stray capacitance measurement. In order to make the epoxy layer more uniform applied on top of the substrate, a ceramic stencil with a rectangular shape hole is utilized to hold the sample, and the epoxy is applied using stencil printing technique. Then, the lead frame is bonded on top of the substrate with a curing process. The curing for Duralco 128 is 1 hour in 120°C and 1 hour in 176°C. After curing, the color of the epoxy changes from silver to yellow. Four samples were made to conduct this reliability test.

(a) DBC sample with step edge (b) Kapton tape applied



(c) Before curing (Duralco 128) (d) After curing (Duralco 128)

Figure 3-13 Fabricated sample for thermal reliability test

Non-destructive tests were conducted to evaluate the thermal reliability of the fabricated samples. After each of the 25 cycles, the stray capacitance between the DBC and the lead frame is measured by the impedance analyzer and the weight of the whole sample is measured by Fisher Scientific ACCU-124 Analytical Balance (0.01mg resolution). One sample test result is summarized in Table 3-4. Before 100

cycles, total weight decreases from 6.8484g to 6.8474g. The weight values will not further decrease after 100 cycles. The leakage current is negligible (less than 1nA) with 1000V voltage stress between the DBC and the lead frame even higher than 100 thermal cycles. The stray capacitance decreases from 29.29pF to 28.39 pF for the first 100 cycles. However, after 100 cycles, the obvious decrease of the stray capacitance can be observed, which is mainly caused by the degradation between the epoxy and top copper lead frame.

Table 3-4 Test results after thermal cycling (sample1)

Cycling numbers	0	25	50	100	125
Stray capacitance: pF	29.29	28.65	28.46	28.39	20.93
Weight: g	6.8484	6.8475	6.8474	6.8474	6.8474

Other three samples show the similar trend as indicated in Table 3-4 and the stray capacitance versus thermal cycling numbers is dipected in Figure 3-14.

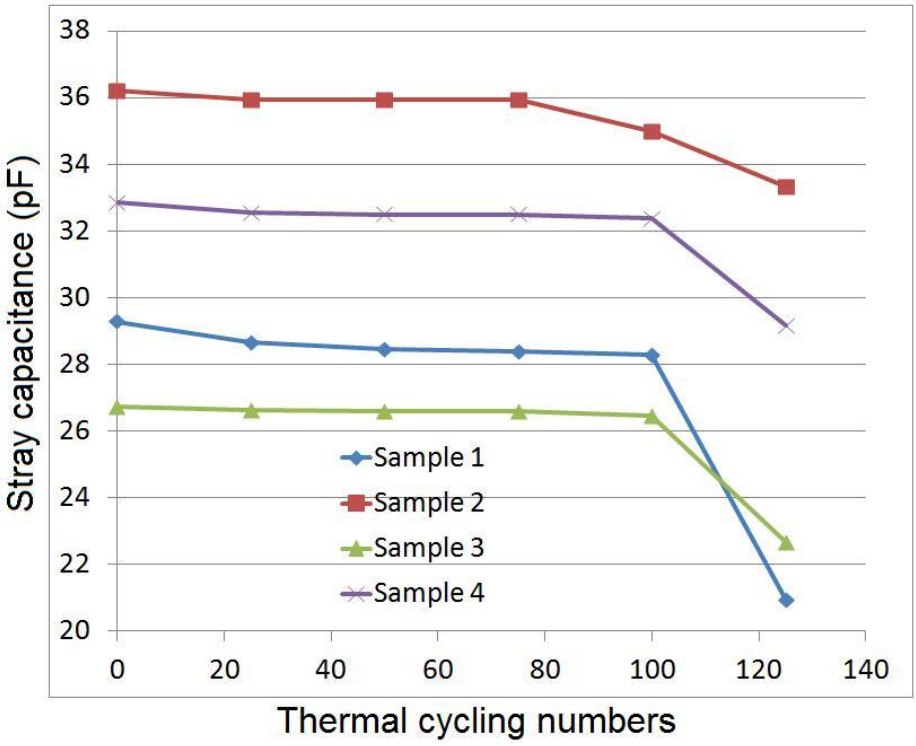


Figure 3-14 Thermal cycling test results

The fabricated samples reliability will degrade after 125 cycles. Since the fabricated samples utilize a large area copper lead frame, which will have more severe thermal stress than the real multiple chips power module fabricated in the next section, the thermal reliability will become higher with a smaller copper lead frame. However, thermal reliability might be further improved by using other bonding and insulation materials.

3.2.4 High Temperature Test for the Hybrid Structure Power Module

The three-phase single-switch rectifier is still used as an example to demonstrate the feasibility of multiple chips power module with proposed hybrid structure in high temperature applications.

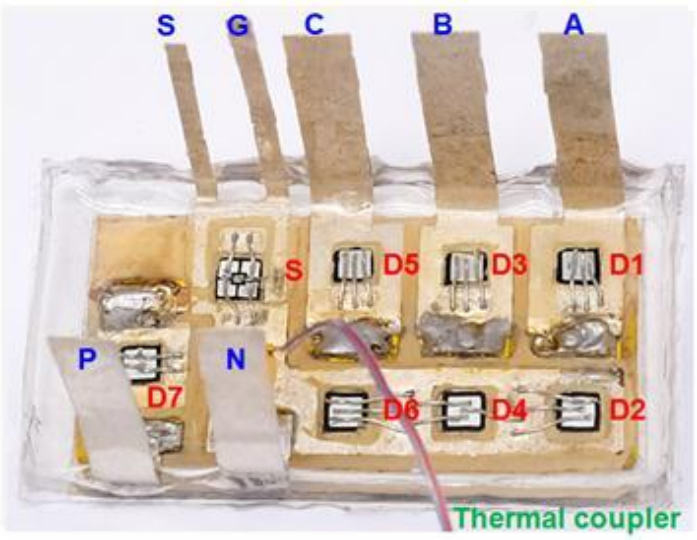


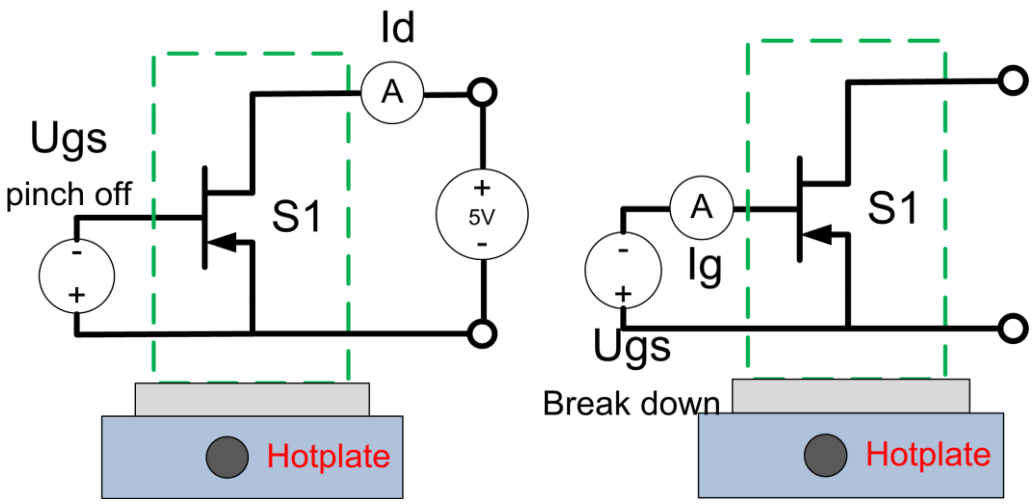
Figure 3-15 Multiple chips power module

The system schematic is shown in Figure 3-7 (a) and the fabrication process of the hybrid structures multiple chips SiC power module is similar to the process proposed in Figure 3-4 except more SiC diodes are utilized. The fabricated power module is shown in Figure 3-15. There are three input power lead-frames (A, B and C), two

output power lead-frames (P and N) and two gate drive lead-frames (G and S). Besides the SiC chips, a T-type thermocouple is also embedded in the power module to monitor the junction temperature.

Before the continuous power test, device pinch off and breakdown voltages are first tested with different operation temperatures. The test schematic is shown in Figure 3-16. The device under test is mounted on the hotplate to test the temperature influence on device pinch off and breakdown voltage.

For the SiC JFET gate pinch off test, the drain-source voltage is connected to an external 5V power supply. A negative voltage is applied to the device gate-source channel. The pinch off voltage is recorded when the drain current is monitored to be 10μA. For the gate breakdown test, a negative voltage is also applied to the device gate-source channel, meanwhile, the JFET gate channel current is also monitored. The breakdown voltage is recorded when the gate current goes up to 200 μA.



(a) Pinch off test (b) Breakdown test

Figure 3-16 Pinch off and breakdown voltage test schematic

The test result is shown in Figure 3-17. 10 different temperature points are tested from 25°C to 250°C with 25°C as a step in between. The pinch off voltage decreases from -23V in room temperature to -24V in 250°C. The breakdown voltage increases from -31.5V in room temperature to -30V in 250°C. The difference between the pinch

off voltage and breakdown voltage changes from 8.4V to 6V by increasing the temperature from 25°C to 250°C.

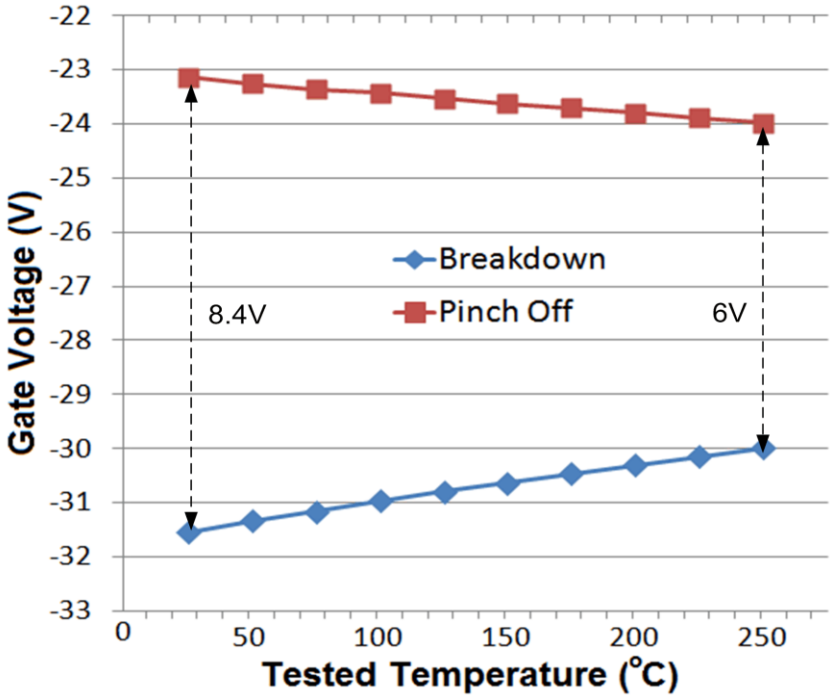


Figure 3-17 Tested pinch off and breakdown voltage

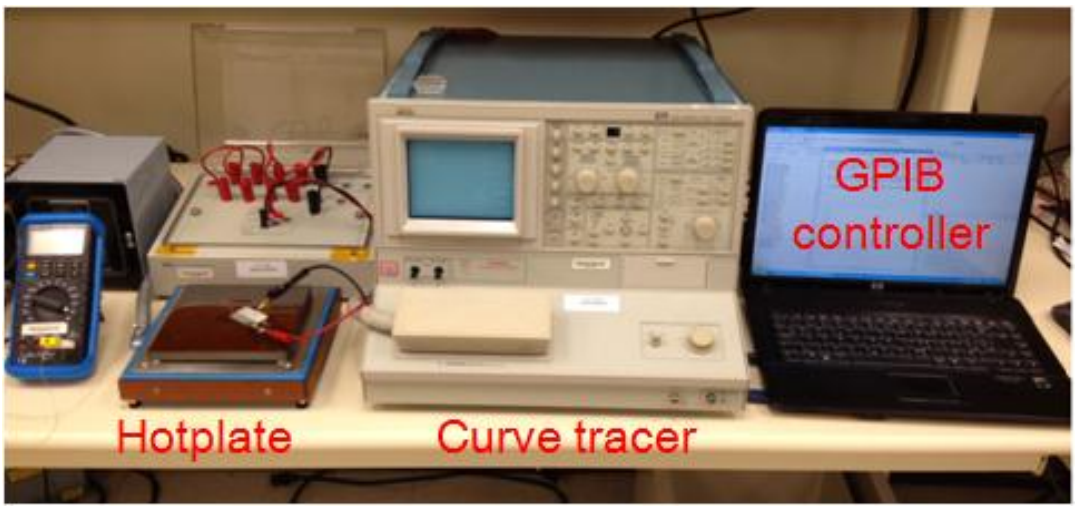


Figure 3-18 Device characteristics test setup

In order to safely switch the normally on SiC JFET, the gate voltage should be kept lower than -24V and higher than -30V.

After the SiC JFET gate channel test, statistic characterizations of both the SiC diode and JFETs are also conducted, and the test bed setup is shown in Figure 3-18. A hotplate is utilized to heat the module with a controllable temperature. A computer is connected to the curve tracer with a GPIB cable to extract data and plot with MATLAB.

Figure 3-19 shows diode (D7) forward characteristics with different temperatures. By increasing the junction temperature, the on-resistance visibly increases due to the reduction in the electron mobility at elevated temperatures. Figure 3-20 illustrates the measured forward characteristics of the SiC JFET. The gate-to-source voltage was controlled as 0V, -15V, -20V and -25V. Based on the test results, Rdson increases about threefold as the ambient temperature rises from 25 ºC to 250 ºC.

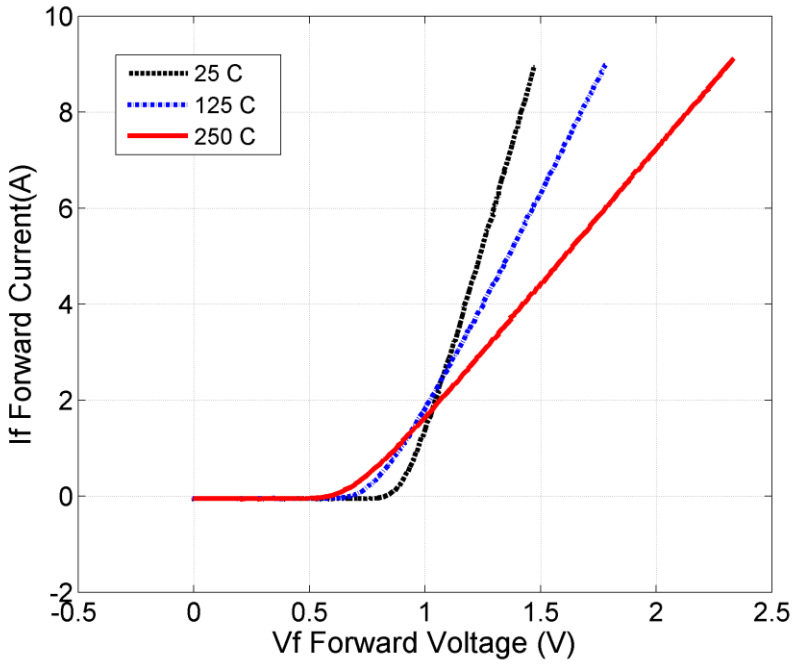


Figure 3-19 Diode (D7) forward characteristics vs temperature

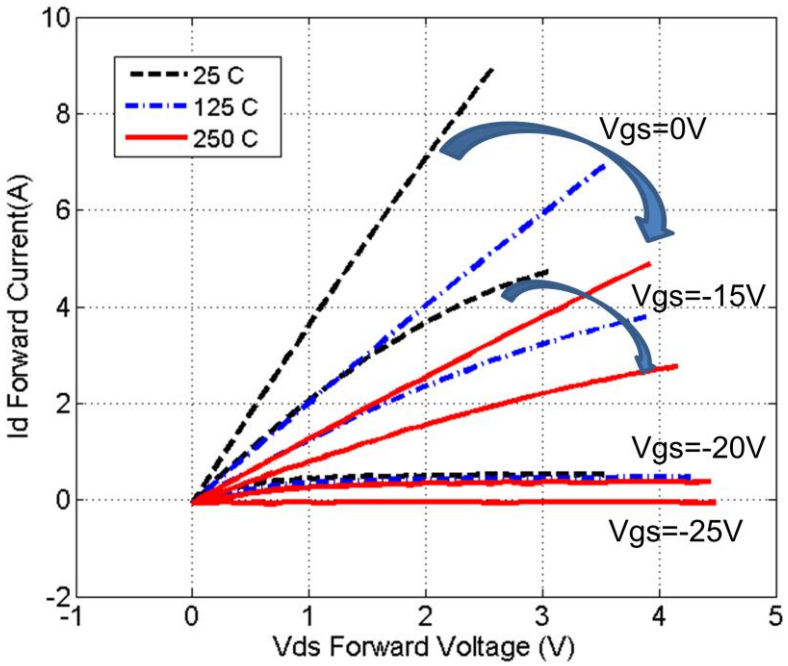


Figure 3-20 JFETs forward characteristics vs temperature

The system schematic and parameters are shown in Figure 3-21 and Table 3-5. The ac input voltage connected to the power module through the input inductors. The dc output of the power module is connected to the dc side capacitor and load. A low temperature gate drive board is designed to drive the SiC JFET. Besides the embedded thermocouple, another T-type thermocouple is used to sense the power module case temperature.

Table 3-5 System parameters

AC input voltage	**70Vrms**	Output Power	**500W**
Dc output voltage	**270V**	Dc capacitor	**20μF**
Supply frequency	**400Hz**	Input inductor	**50μH**
Switching frequency	**30kHz**	Load	**150Ω**

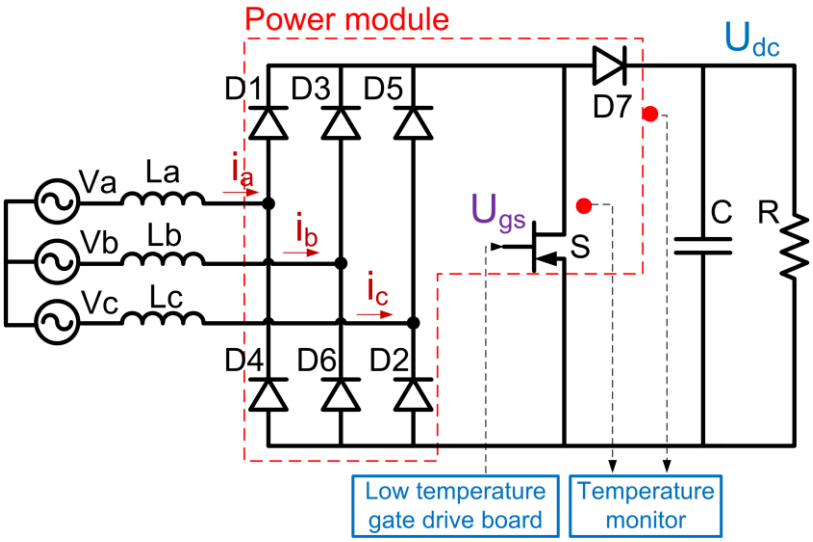
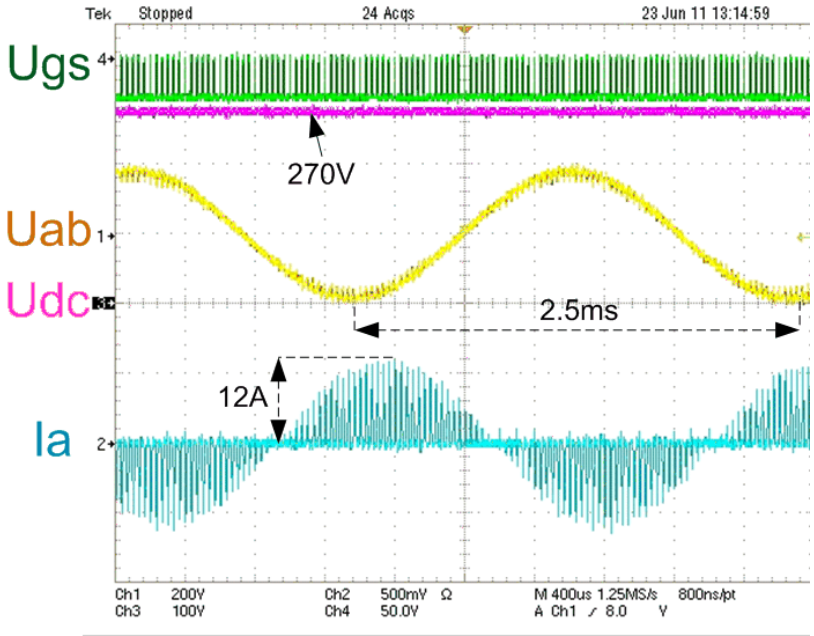
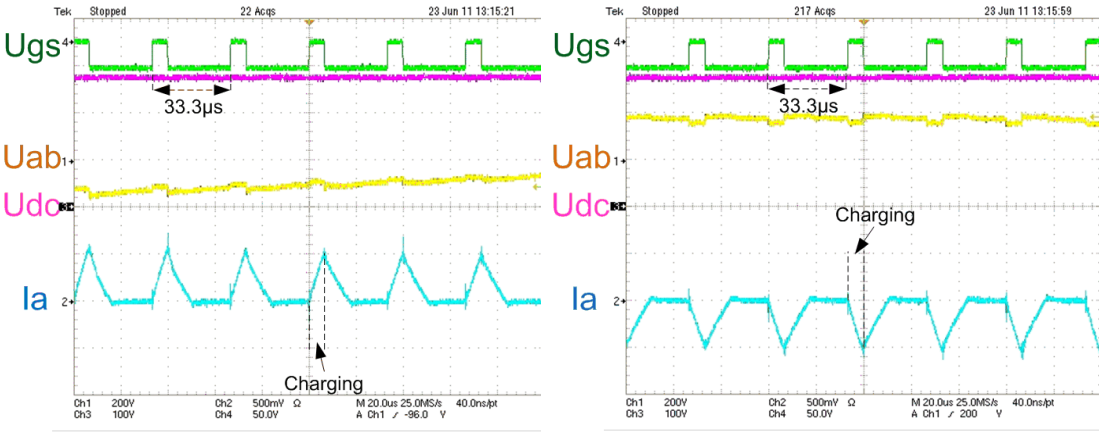


Figure 3-21 System schematic in experiment

The continuous power test is shown in Figure 3-22. The hybrid structure power module operated stably with 70Vrms input voltage (phase to neutral), 270V output voltage and 30 kHz switching frequency. The peak current reaches 12A and the efficiency of the power module is 97%.



(a) Experimental waveforms



(b) Positive input current range low diode (c) Negative input current range high diode

Figure 3-22 Continuous power test results (500W, 250°C junction temperature)

The thermal test results are shown in Figure 3-23. The embedded thermocouple tests the module inside temperature reaching 225°C and the case temperature reaching 202°C. Because the bonding point of the module embeded thermocouple is 1cm away from the SiC JFET, the estimated device junction temperature is around 250°C. The test results prove that the developed hybrid package SiC power module can support operation at a 250°C junction temperature. A FLIR SYSTEMS S65 thermal camera is utilized to take a thermal picture, which monitors the encapsulate temperature.

The monitored temperature and efficiency is shown in Table 3-6. The converter total efficiency is 96.1% for a 250°C junction temperature, which is 0.9% lower than at room temperature. The major reason for the higher loss is due to the positive temperature on resistance of the SiC diode and JFET as indicated in the Figure 3-19 and Figure 3-20. The test results prove that the developed hybrid package SiC power module can support operation at a 250°C junction temperature.

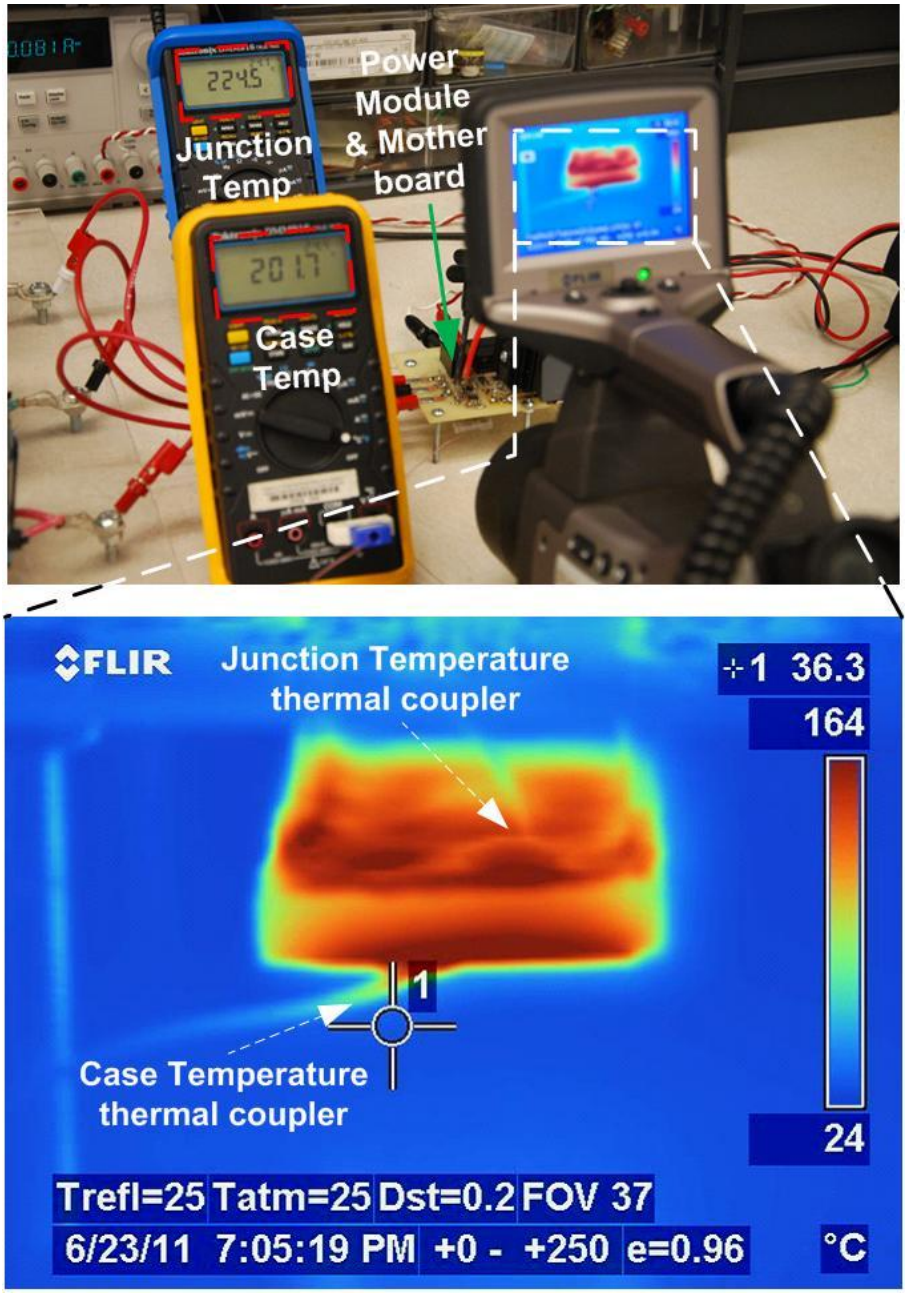


Figure 3-23 Thermal test results

Table 3-6. Measured Temperature Distribution and Efficiency

Time	JFET	Heatsink	Efficiency
0:00 minutes	24.5°C	24.5°C	97%
30:00 minutes	224.5°C	201°C	96.1%
40:00 minutes	224.5°C	201.7°C	96.1%

A novel hybrid structure for high-temperature SiC power modules is presented in this section. The hybrid structure can achieve the same footprint and similar parasitic as the planar structure without double-side solderable devices. In addition, a more flexible die-attachment material selection is possible and the processing complexity and time are reduced. A three-phase single-switch multiple chips power module prototype is built to demonstrate the feasibility of this packaging method. The experimental results demonstrate the three phase rectifier module capability of working in 250°C junction temperature.

3.3 Other High-Temperature Components

As shown in Figure 3-1, in addition to the main circuit devices, the DC-link capacitor, voltage and temperature sensor, protection, PWM controller and gate drive circuits must also be able to operate in a high-temperature environment.

For control electronics, the junction leakage current at high temperatures is a major concern in bulk CMOS processes and can lead to the failure of the circuit in a high-temperature environment. SiC-based devices are expected to be able to operate up to 600°C. However, there is no SiC-based integrated circuit manufacturing available yet. With the silicon-on-insulator (SOI) technology, the leakage current for high-temperature operation can be effectively reduced. As shown in Figure 3-24, a buried insulator layer in the SOI structure greatly decreases the leakage path associated with the drain and the source p-n junction diodes. In addition, the threshold voltage variation with temperature is smaller in SOI devices than in bulk devices. SOI also provides improved latch-up immunity, which ultimately increases the reliability of the circuit operation at a higher temperature. These properties make SOI-based circuits

capable of operating successfully in the 200°C-300°C temperature range, which is well above the range of conventional bulk silicon-based devices [76].

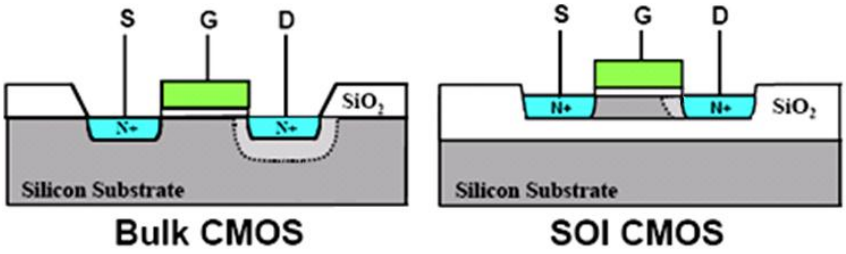


Figure 3-24 Structure comparison between Bulk CMOS and SOI CMOS

Cissoid and Honeywell provide high-temperature silicon-on-insulator semiconductor solutions. The typical SOI components include voltage regulators, voltage references, clock generators and timers, analog-to-digital converters, amplifiers, power MOSFETs and drivers. Some of the SOI components are shown in Figure 3-25.

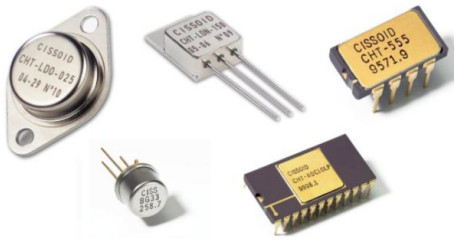


Figure 3-25 High-temperature SOI components from Cissoid

The high-temperature resistors are surveyed and listed in the Appendix Table A-1. High-temperature thickfilm resistors are selected during the design. The capacitors, which are rated for use at more than 200°C, are surveyed and summarized in Figure 3-26 and Table A-2. The data comes from the manufacturers' websites and surveyed literatures. Generally speaking, three types of capacitors provide high-temperature capability: ceramic, tantalum and mica. As shown in Figure 3-26, the tantalum capacitor covers a high-capacitance range with a very low voltage ranting. Conversely, the mica capacitor covers a low capacitance range with a high voltage rating. However, the ceramic capacitor fills the gap between the tantalum capacitor and mica capacitor. In our design, both the control and DC link capacitors are ceramic

capacitors. The high-temperature magnetic components rated above 200°C are summarized in Figure 3-27 and Table A-3. For applications requiring low saturation flux and high operation frequency, most publications utilize ferrite magnetic core [75, 130-132]. For high saturation applications, such as a boost filter or an EMI filter in a high-power converter, a nanocrystalline soft magnetic core could be a good candidate [133]. High-temperature low permeability NiZn ferrite toroid cores (4C65) from Ferroxcube are used in the gate drive transformer design.

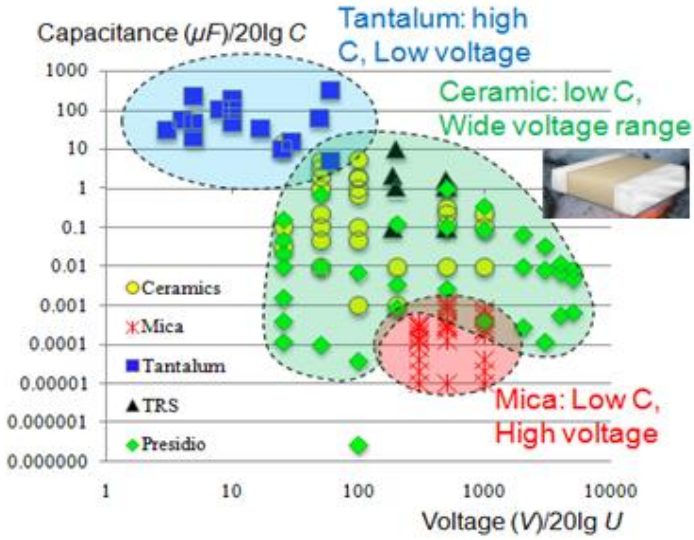


Figure 3-26 Summarized high-temperature capacitors

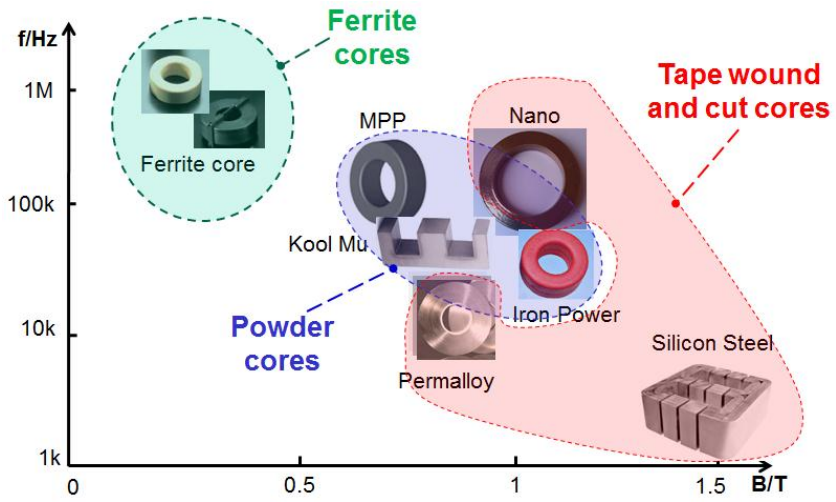


Figure 3-27 Summarized high-temperature inductor

95%Pb - 5%Sn high temperature solder from Amerway is chosen to solder the mother-board components. Advanced Circuits provides the high-temperature

hydrocarbon ceramic material laminate PCB (Rogers 4350), which can operate at temperatures up to 280°C, and be utilized to build the mother-board.

The thermal reliability characteristics of some of the selected components are also tested in the converter design, and the results are shown in the following sections.

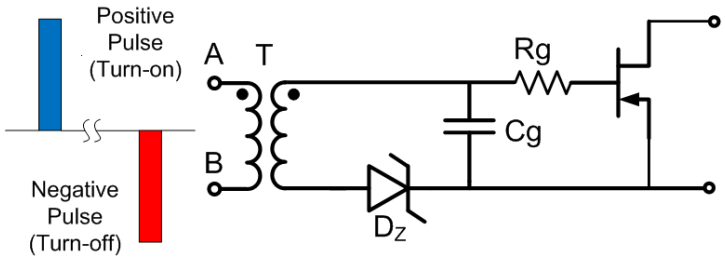
3.4 High Temperature Isolated Gate Drive Design

A gate drive circuit usually provides a connection between a low-power signal IC and the system power devices. Optical and magnetic methods are common ways to provide signal or power isolation from the signal IC to the power devices [134]. Since there is no commercial high-temperature opto-coupler available, transformer isolation is the only choice for a high-temperature isolated gate drive design.

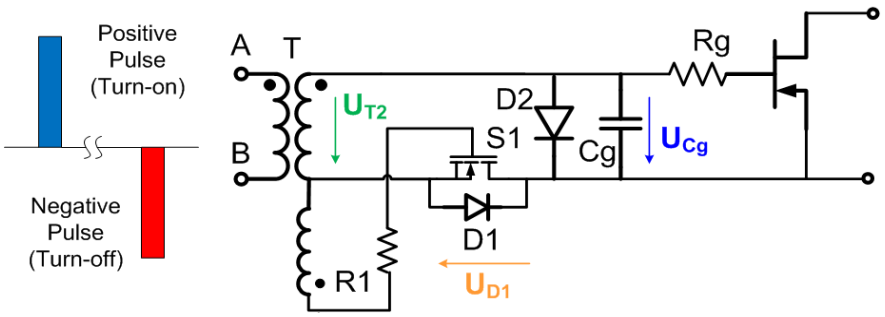
3.4.1 Transormer Isolated Gate Drive for Single Device

A. Existing Topologies Evaluation

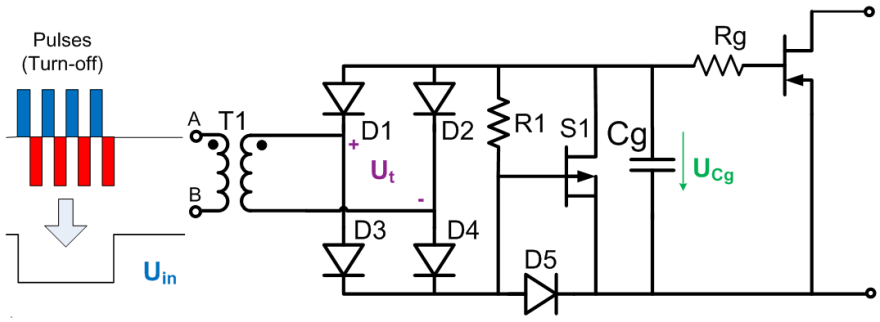
A pulsed transformer gate drive circuit can provide a smaller core size and easier volt seconds balance than other transformer-isolated gate drive circuits. Hence, the gate drive topology selection is based on different pulsed transformer gate drive circuits as shown in Figure 3-28.



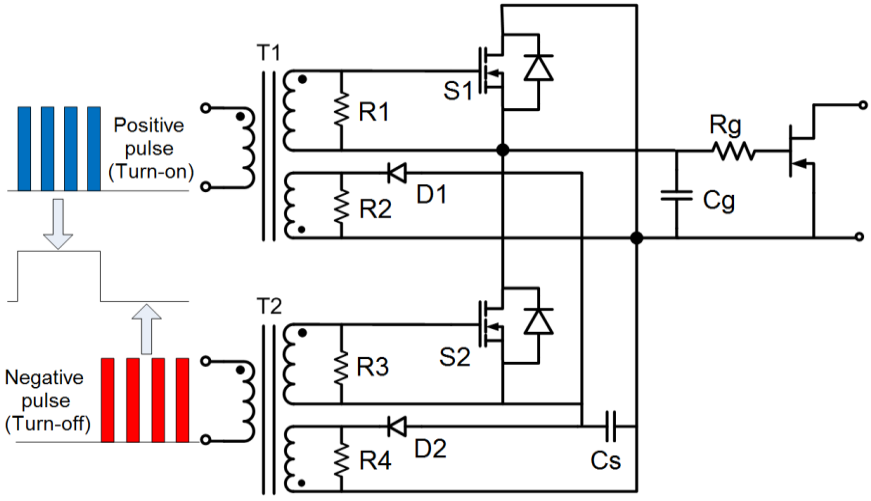
(a) Edge triggered circuit 1



(b) Edge triggered circuit 2



(c) High frequency modulation circuit 3



(d) High frequency modulation circuit 4

Figure 3-28 Different pulse transformer gate drive circuits

(1). Edge triggered circuit 1 [135]

This edge triggered gate drive circuit 1 depicted in Figure 3-28 (a) is originally used in MOSFET gate drive. A two terminals transformer is used as the isolation part. The primary side is the pulse generation circuit and the secondary side is the gate drive

circuit, which is made up of one Zenar-diode and one gate capacitor Cg. A negative pulse will charge the capacitor Cg to turn off the JFET and a positive pulse will discharge the capacitor Cg to turn on the JFET. Figure 3-29 shows the Zenar-diode characteristics. Since there is a large leakage current at the Zenar-voltage (Vz), the capacitor voltage Ucg after the negative pulse will move from the charge point to a higher hold-up value as indicated in Figure 3-29. The hold-up point value can easily be higher than the JFET pinch-off voltage, which is usually 5~6V higher than the breakdown voltage and unable to turn off the JFET.

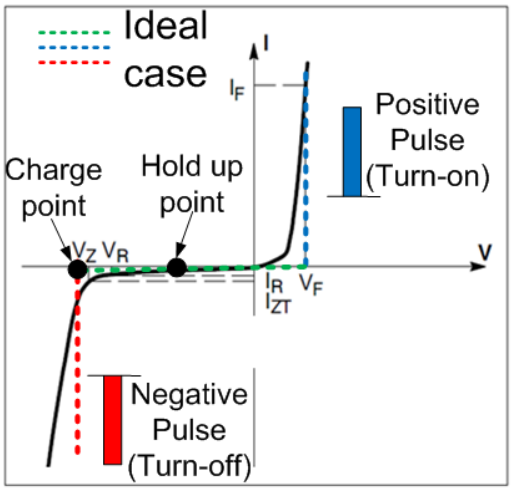
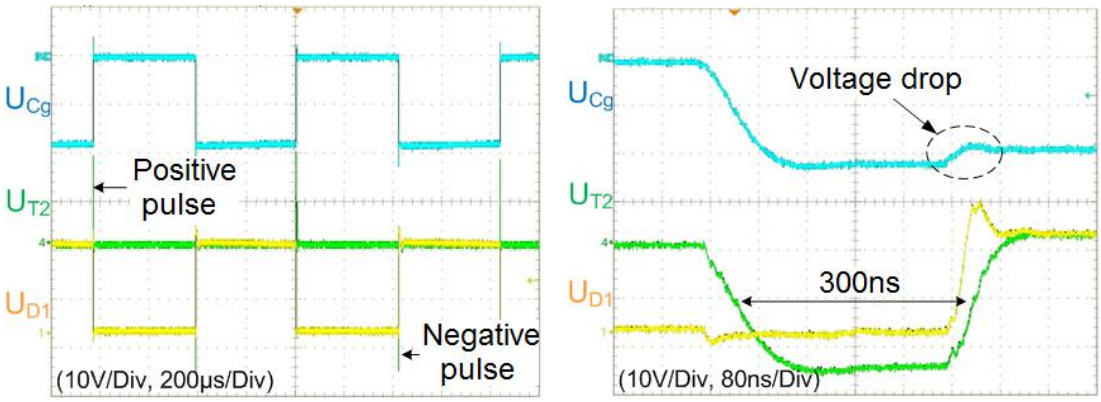


Figure 3-29 Zenar-diode characteristics

(2). Edge triggered circuit 2 [136]

In this topology, another discrete MOSFET is used on the secondary side of the transformer to better control the gate charging and discharging. Figure 3-30 shows the test results of this edge triggered gate drive circuit. When the positive pulse is applied on the primary side, the secondary side MOSFET is turned on and the diode D2 is conducted to short the gate capacitor Cg, which turns on the JFET. When the negative pulse is applied on the primary side, the MOSFET is turned off and the negative pulse charges the gate capacitor Cg through the MOSFET body diode D1. After the negative pulses, a voltage drop can be observed in the capacitor voltage U_{Cg} as shown

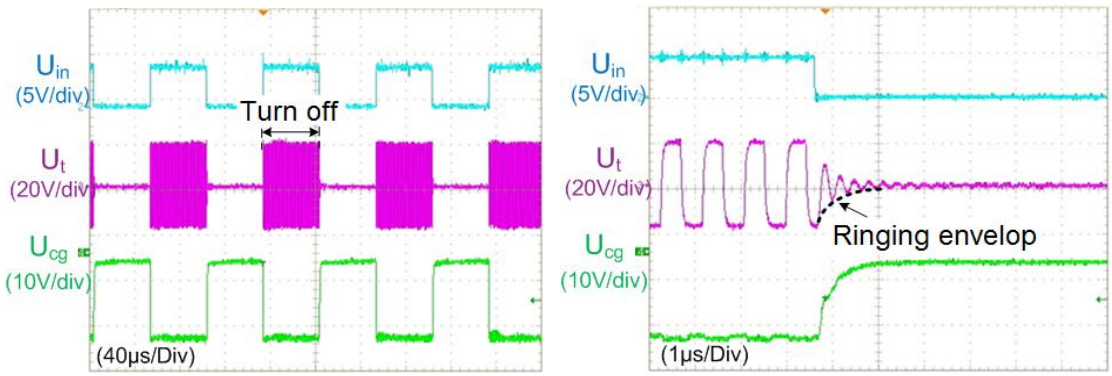
in Figure 3-30 (b). This is because the charge in the capacitor Cg is redistributed between itself and the MOSFET junction capacitor. The width of the pulse is controlled as 300ns.



(a) Switching waveforms (b) Turn off the JFET

Figure 3-30 Edge triggered gate drive circuit 2 test results

(3). High frequency modulation circuit 3[137, 138]



(a) Switching waveforms (b) Turn on the JFET

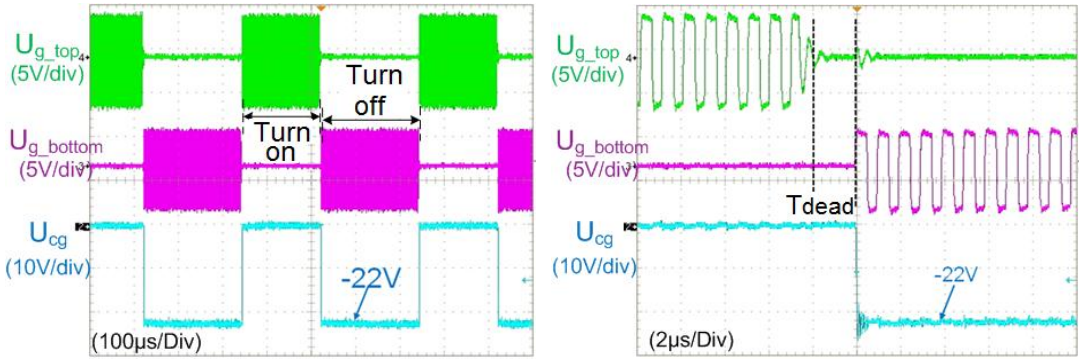
Figure 3-31 High frequency modulation gate drive circuit 1 test results

A high frequency modulation circuit 3 originally used in IGBT gate drive is shown in Figure 3-28 (c). The drive signal is modulated by another high-frequency carrier square wave of about 1MHz, which leads to a 3.5% duty cycle resolution for a 70kHz switching frequency. The PMOS is used to create a fast discharge route for capacitor Cg. Figure 3-31 shows the test results. The turn-on time is constrained by the ringing envelope of the terminal voltage as shown in Figure 3-31 (b). The ringing frequency

is determined by the resonance between the transformer magnetic inductance and the primary side totem pole device junction capacitors.

(4). High-frequency modulation circuit 4 [40]

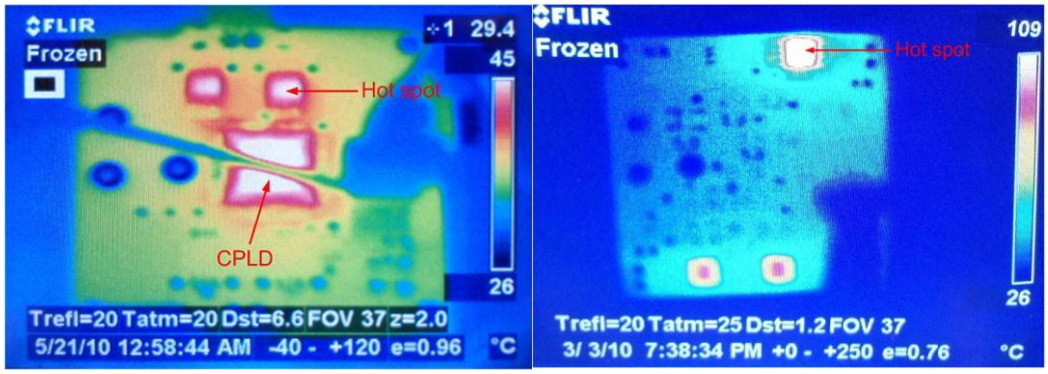
Like topology 3, in topology 4 the input gate signal will be modulated with a high frequency (1MHz) modulation signal. The output winding of transformer 1, which is connected with resistor R1 is used to turn on S1and short the gate resistor Cg to turn on the JFET. The output winding of transformer 2, which is connected with resistor R3 is used to turn on S2 and charge Cg from the energy storage capacitor Cs. Two other windings are used to charge the energy storage capacitor Cs, which allows this capacitor to be considered as a secondary side isolated power supply. Figure 3-32 shows the test results. To prevent overshooting between the switches S1 and S2, a dead time is inserted between the two transformers modulation signals.



(a) Switching waveforms (b) Turn off the JFET

Figure 3-32 High frequency modulation gate drive circuit 2 test results

Besides the gate drive board, the same totem pole chip (IXDD514) is used in both primary sides for pulse generation. The thermal performance comparison between these two pulse generation boards is shown in Figure 3-33. The high frequency modulation method has a hot spot temperature of 109 °C while the edge triggered method only reaches 45 °C.



(a) Edge triggered circuit2 (b) High frequency modulation circuit4

Figure 3-33 Pulse generation board thermal performance comparison

Table 3-7 Topologies comparison

Circuit	1	2	3	4
Gate drive complexity	low	medium	medium	high
Primary side complexity	medium	medium	low	medium
Safely turn off	no	yes	yes	yes
Switching speed	high	high	low	high
Duty cycle resolution	high	high	low	low
Thermal performance	good	good	poor	poor

The comparison results are shown in Table 3-7. Although topology 2 shows the best performance, it cannot achieve independent control for both turn-on and turn-off speed since the two subintervals share the same route. In order to solve this, improved gate drive topology is proposed in Figure 3-34.

B. Proposed Improved Edge Triggered Gate Drive Circuit

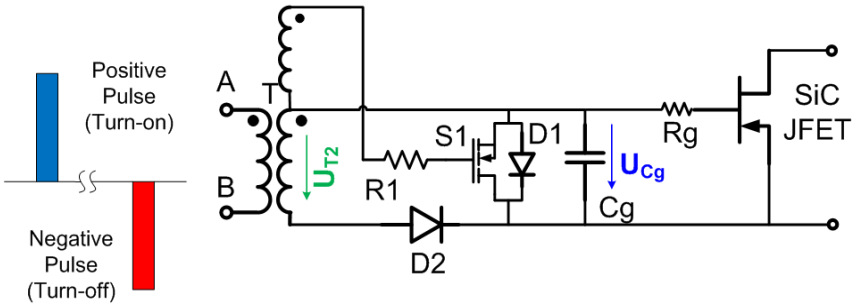
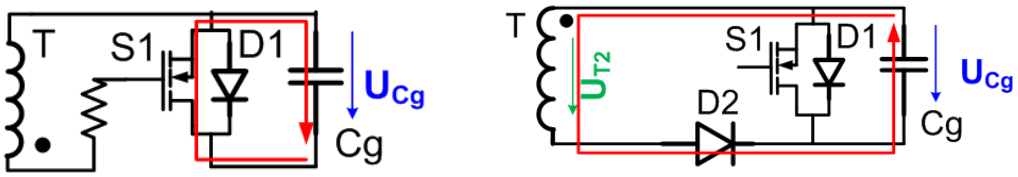


Figure 3-34 Improved gate drive topology

The topology is composed of a three-terminal transformer, secondary MOSFET S1, secondary diode D2, and gate capacitor Cg. The body diode of the MOSFET is depicted as D1. Since this topology is a pulse transformer-isolated gate drive, the positive pulse or negative pulse are applied to the primary side of the gate drive to turn on or turn off the SiC JFET. When the positive pulse is applied on the primary side, the secondary-side MOSFET S1 is turned on, which shorts the gate capacitor Cg to turn on the JFET. When the negative pulse is applied on the primary side, the gate capacitor is charged to the negative voltage through diode D2, and the negative voltage needs to be lower than the gate threshold voltage to turn off the JFET. After the negative pulse, the negative voltage can be held in the gate capacitor, and continue to turn off the JFET until another positive pulse is applied to turn on the JFET. The two subintervals are shown in Figure 3-35. For this edge-triggered gate drive circuit, both the signal and power are transferred from the primary side to the secondary side within the pulses. Since there is leakage current in the secondary gate drive circuit from both switch S1 and the JFET gate to source channel, the gate charge of capacitor Cg will decrease during the turn-off interval. A refreshing function needs to be applied to the primary side if the JFET needs to be statically turned off. The detailed

refreshing will be shown in the following design considerations. For this version of the transformer isolated gate drive, gate drive fail protection is not considered.

Because the two subinterval circuits utilize different routes for charging and discharging, the proposed gate drive can achieve independent control for both turn-on and turn-off speeds. No current-limiting resistor is requried during turn-on process.



(a) Positive pulse to turn on the JFET (b) Negative pulse to turn off the JFET

Figure 3-35 Turning on and turning off the JFET

An 80V voltage rating silicon-on-insulator (SOI) high-temperature power MOSFET (CHT-NMOS8010) from Cissoid is used for switch S1 and a 600V voltage rating SiC diode (C3D06060A) from Cree is used for diode D2.

The primary-side pulse generation function is achieved using Cissoid high-temperature half-bridge drive chips (CHT-HYPERION).

C. Edge-Triggered Isolated Gate Drive Design Considerations

For the edge-triggered isolated gate driver topology, the energy is only transferred from the primary side to the JFET within the turn-on or turn-off pulses. If the JFET doesn't switch for a long time, the leakage current in the gate drive circuit will cause the JFET gate-source voltage amplitude to decrease. Therefore, the refreshing functions need to be implemented to recharge the gate capacitor.

To achieve the refreshing function, the minimum refreshing frequency needs to be determined according to the leakage current analysis. As shown in Figure 3-36, three

different leakage current routes, marked in green, blue and red, cause the gate capacitor voltage amplitude to drop.

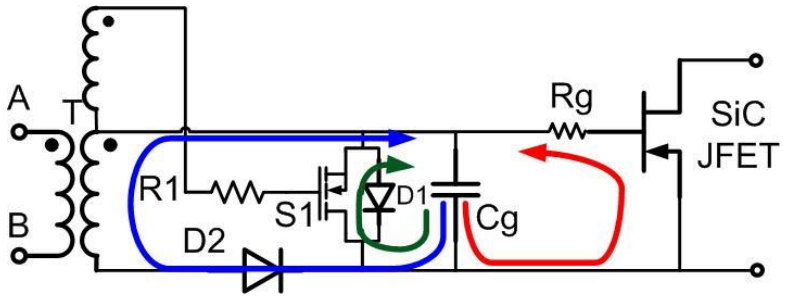


Figure 3-36 Leakage current analysis for the edge-triggered gate drive topology

The first leakage route is caused by the diode reverse current. The second leakage route is caused by the MOSFET leakage current during turn off (zero gate voltage). These two leakage current value can be obtained by the corresponding datasheet.

The third leakage route comes from the JFET gate leakage. The leakage current of the JFET depends on both the gate voltage and the drain-source voltage. Since there is no datasheet for the SiC JFET gate channel characteristic, the gate leakage current is tested and measured with the similar setup shown in Figure 3-16 (b). Since the different SiC JFET samples have slightly different gate pinch off and break down voltage, the medium value of the pinch off and break down is selected for each gate voltage for different samples. The gate channel leakage current is monitored with different applied drain-source voltage and the results are shown in Table 3-8.

Table 3-8 Leakage current test with different drain-source voltages

μA	#1	#2	#3	#4	#5	#6	#7	#8	#9
0V	0.467	0.437	15.66	0.054	81.2	0.85	0.4	0.56	53.1
50V	0.284	0.261	8.24	0.021	72.8	0.56	0.25	0.36	49
100V	0.262	0.272	7.07	0.018	69.9	0.527	0.233	0.32	48.7
150V	0.252	0.384	6.59	0.017	67.4	0.509	0.223	0.301	47.1
200V	0.244	0.59	6.25	0.015	65.7	0.495	0.216	0.286	46.2

It can be observed that several samples, such as #3, #5 and #9, will have very large leakage current compared with the other samples. The samples with huge gate

channel leakage current should be avoided for this gate drive design. Otherwise, a very high refreshing frequency needs to be applied to recharge the gate capacitor. Besides the high-leakage current samples, the leakage current characteristics of other samples corresponding to the drain-source voltage are plotted in Figure 3-37. Most samples have smaller gate channel leakage current when the drain source voltage increases, with the exception of sample #2. The leakage current range of most JFET samples is less than 1μA.

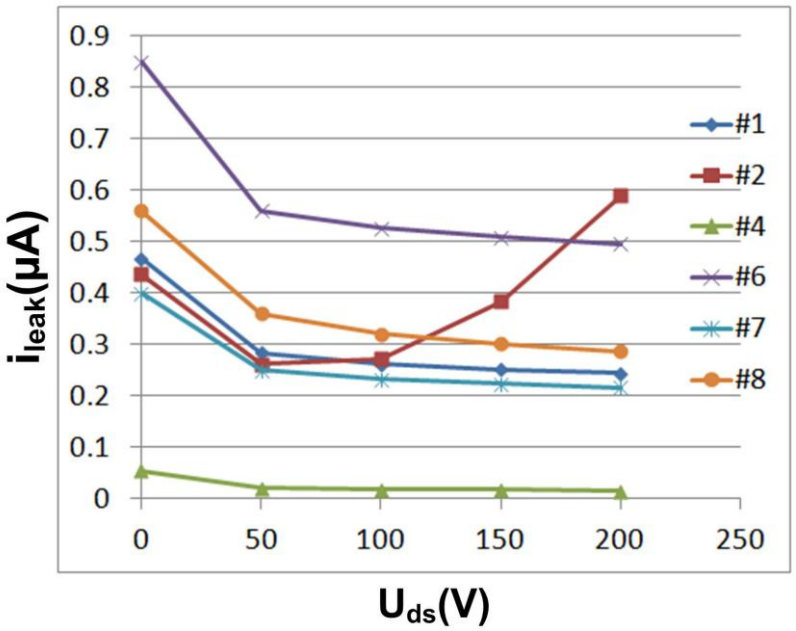


Figure 3-37 Leakage current test with different drain-source voltages

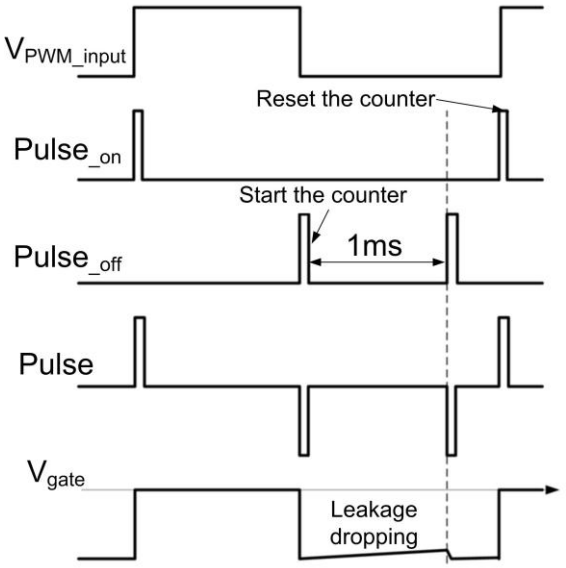
With the consideration of the leakage current analysis above, the total leakage current will be roughly less than 2 μA. If the voltage drop caused by the leakage current is smaller than 0.5 - 1V, the refresh time can be calculated by:

$$\Delta t = \frac{C_{gate}\Delta U}{I_{leak}} = 1 \sim 2ms \tag{3-2}$$

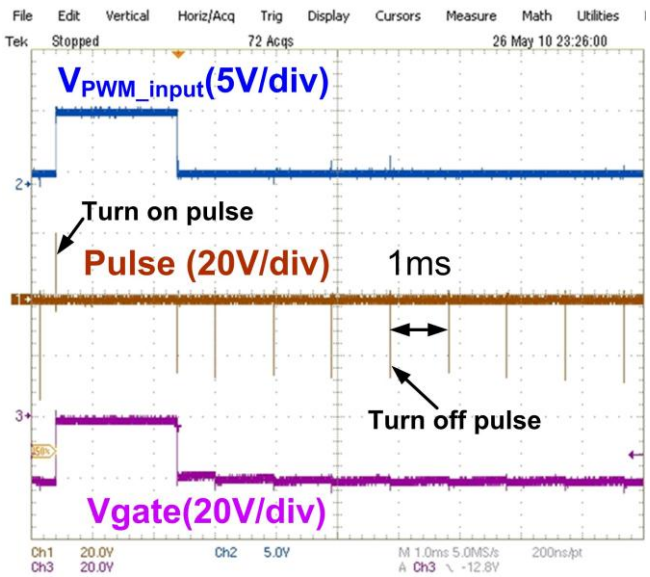
where $C_{gate} = 4nF$

The 1 kHz refreshing frequency test is shown in Figure 3-38. Figure 3-38 (a) shows the refreshing function schematic and (b) shows the test results. With the refreshing

function, the normally on SiC JFET gate voltage can keep a negative bias to statically turn off the device.



(a) Refreshing function schematic



(b) Refreshing function test

Figure 3-38 1kHz refreshing test for edge triggered gate drive

3.4.2 Transormer Isolated Gate Drive for Phase Leg

Beside the high temperture isolated gate drive design with single JFET, a phase-leg gate drive circuit is built based on two single JFET gate drive circuits proposed in Figure 3-34. The high-temperature components used in gate drive design include

high-temperature ferrite cores (4C65) from ferroxcube. A discrete power module implemented with two 1200V SiC JFETs and two 1200V SiC diodes is also built and connected to the gate drive board to verify the gate drive circuit design as shown in Figure 3-39.

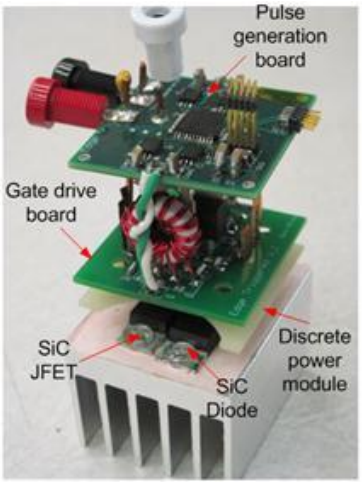


Figure 3-39 Picture of phase leg module

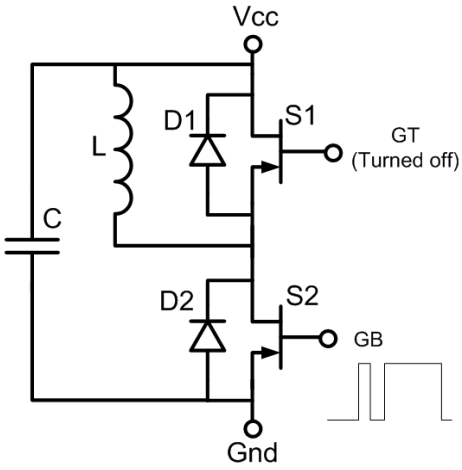


Figure 3-40 Double pulse test schematic

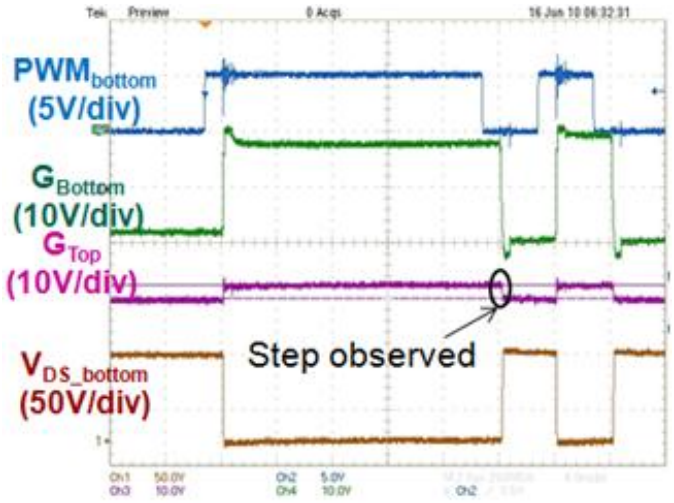
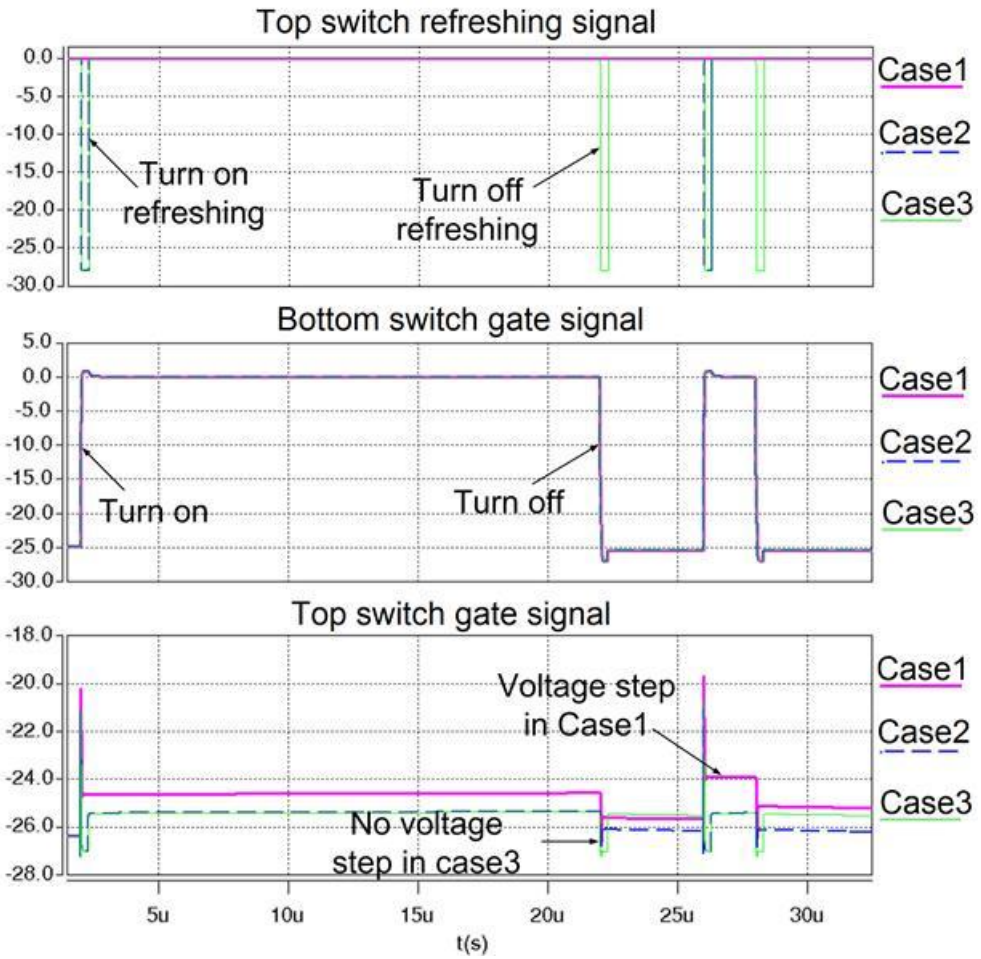
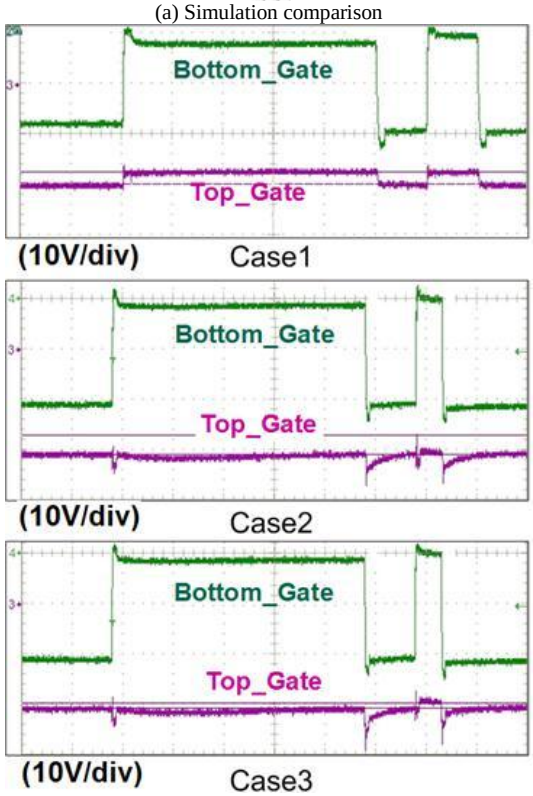


Figure 3-41 Double pulse test result

As mentioned above, since the gate drive energy is only transferred from the primary side to the secondary side by pulses, the leakage current from the gate drive circuit will cause the JFET turn-off voltage to decrease when there is very slow switching frequency or statistically turning off the JFET. The refreshing function is implemented by a CPLD on the pulse generation board. Figure 3-40 shows the double pulse test schematic. The preliminary test result is shown in Figure 3-41.



(a) Simulation comparison

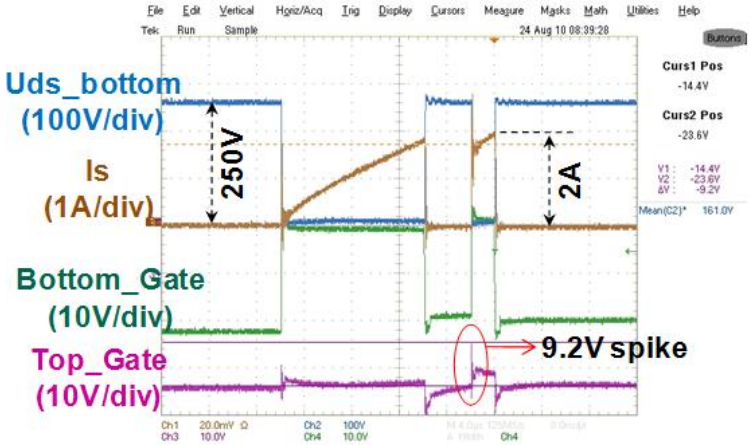


(b) Experiment comparison

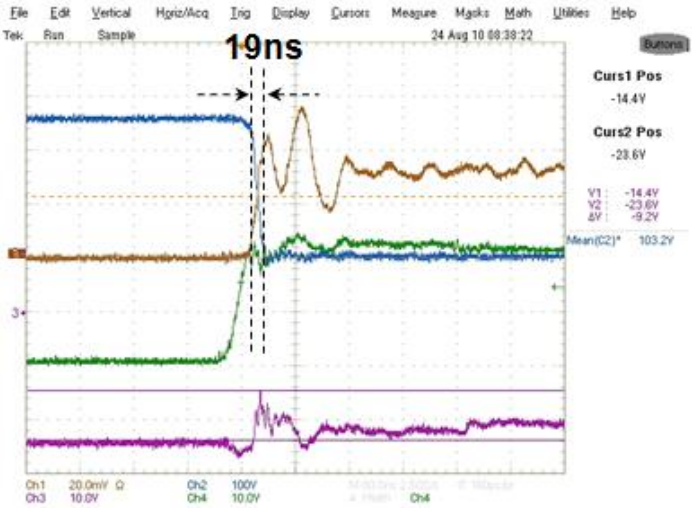
Case 1: w/o synchronous, Case2: w/ turn on synchronous, Case3: with both turn on/turn off synchronous

Figure 3-42 Reducing the voltage step cross-talking by synchronous refreshing of the top switch

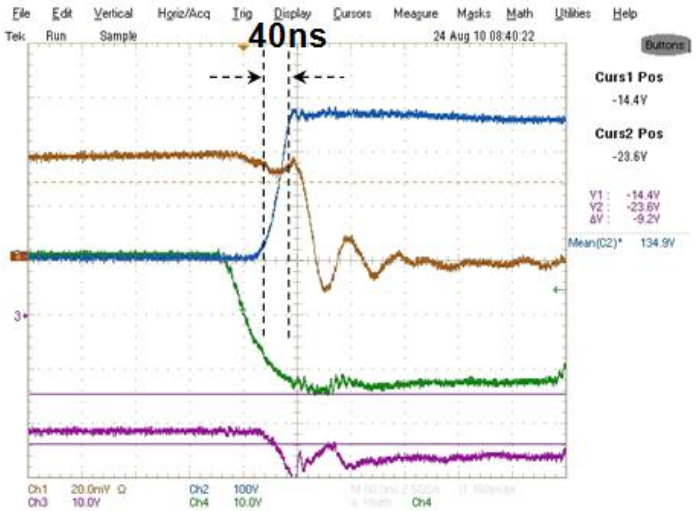
A gate voltage step caused by cross-talking can be observed. This voltage step can be alleviated by synchronizing the top and bottom switch refreshing signals as shown in Figure 3-42.



(a) Switching waveform



(b) Turn-on switch



(c) Turn-off switch

Figure 3-43 Double pulse test at 250V

The double pulse test with both turn-on and turn-off synchronous refreshing is adopted. However, when the dc link voltage goes up to 250V, a 9.2V spike in the top gate signal can be observed as shown in Figure 3-43.

To prevent or mitigate the parasitic turn-on effect due to the miller capacitor, an active miller clamp solution is usually implemented. However, the active clamp method will be difficult to implement in high temperature applications because of the limited availability of high-temperature components. To keep the same switching speed, if one can decrease gate resistance Rg, the voltage spike caused by cross-talking will be reduced. In order to achieve this target, an improved two stage gate drive method is proposed as illustrated in Figure 3-44.

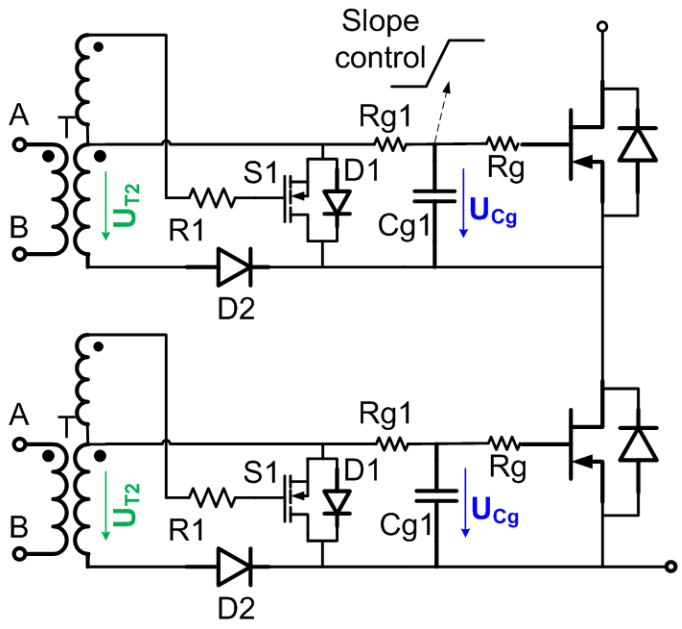
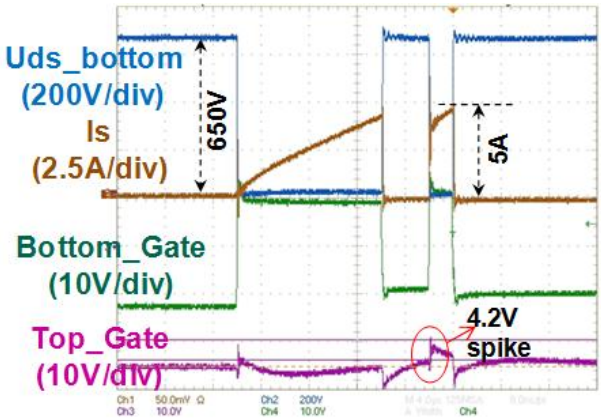


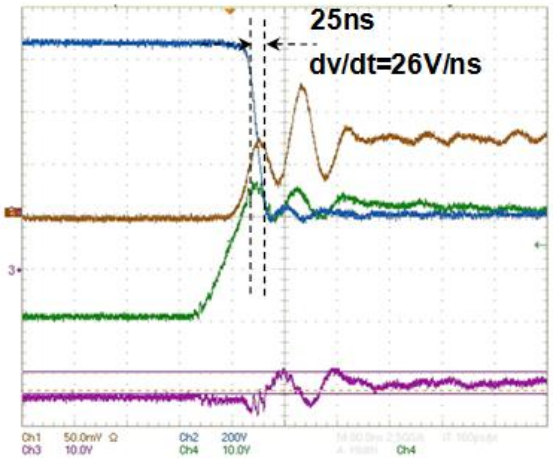
Figure 3-44 Improved two stage gate drive

With the controllable slop by resistor Rg1 and capacitor Cg1 in the first stage, gate resistance Rg can be greatly reduced to achieve the same switching speed and switching loss. Using the improved solution, the results of the full power test are shown in Figure 3-45. Even in the 650V DC link, the cross talking voltage can be controlled to within 4.2V with 26V/ns turn on speed.

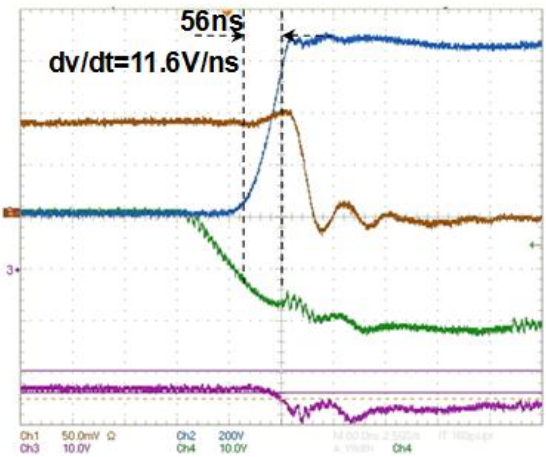
A SiC JFET model is used in the simulation [10]. The simulation and experiment results are summarized in Table 3-9. The improved method can achieve much less cross-talking with the same switching speed and switching loss.



(a) Switching waveform



(b) Turn-on switch



(c) Turn-off switch

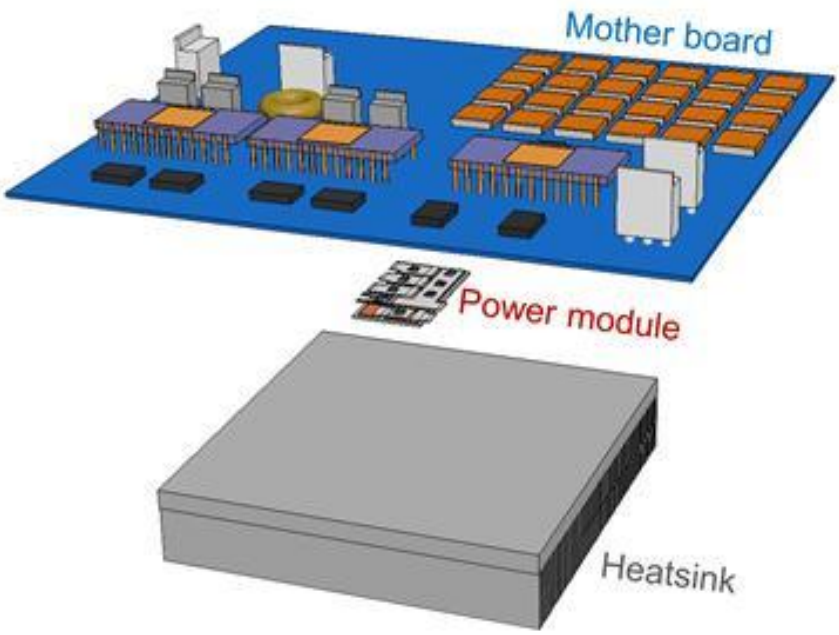
Figure 3-45 Double pulse test at 650V,5A with improved solution

Table 3-9 Summarized simulation and experiment results

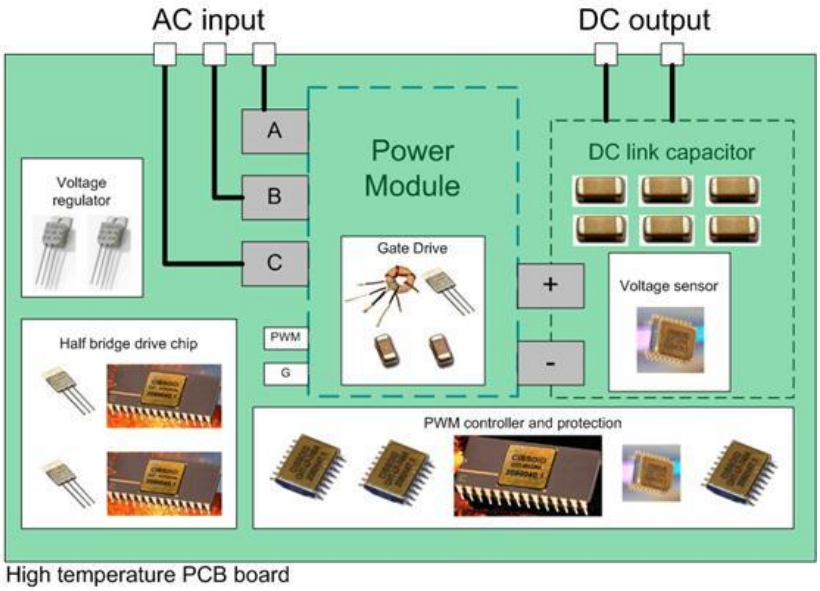
		w/o changing slope	
		Simulation	**Experiment**
250V DC	Cross-talking	5.2V	9.2V
	Turn-on(ns)	17ns	19ns
	Turn-off(ns)	34ns	40ns
650V DC	Cross-talking	8.1V	
	Turn-on(ns)	25.5ns	
	Turn-off(ns)	39ns	
		w/ changing slope	
		Simulation	**Experiment**
250V DC	Cross-talking	0.7V	1.5V
	Turn-on(ns)	17ns	18ns
	Turn-off(ns)	36ns	42ns
650V DC	Cross-talking	2V	4.2V
	Turn-on(ns)	20ns	25ns
	Turn-off(ns)	43ns	56ns

3.5 High-Temperature Three-Phase Rectifier System Design

3.5.1 System Structures and Functions:



(a) System structure



(b) Mother board functions defination

Figure 3-46 System functions defined

Figure 3-46 shows the system structure and motherboard functions for the three-phase PWM rectifier. In addition to the power module and heatsink, a high-temperature motherboard is designed to be placed on top of the power module. High-temperature ceramic DC-link capacitors are put on top of the motherboard to filter high-frequency current and a voltage sensor circuit and a temperature sensor circuit are implemented to sense the DC-link voltage and the device junction temperature. Using these sensors and protection circuits, the protection mode will be activated if the voltage and temperature are higher than the threshold values. Other functions implemented in the motherboard are the PWM controller, voltage regulator, pulse generation and gate drive circuit.

3.5.2 Sensor and Protection Design:

A DC-link voltage sensor is required for both control and protection. A non-isolated three-op-amp instrumentation amplifier is selected as the voltage sensor, as shown in

Figure 3-47. A high-temperature quad op-amp (CMT-OPA-PSOIC16) from Cissoid is used.

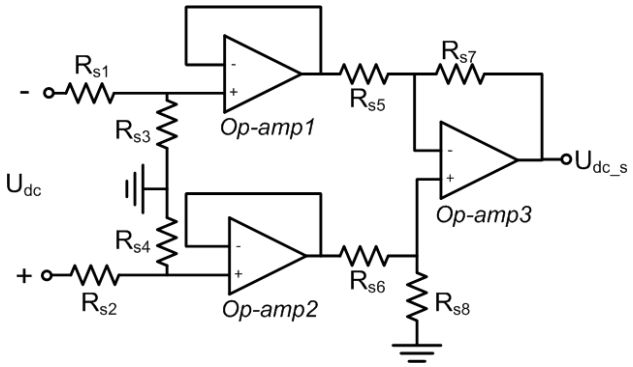


Figure 3-47 Voltage sensor topology

It's worthwhile to note that the high-temperature op-amp usually has a very low slew rate (1~2V/μs) [139], which might prohibit its use in high-frequency voltage sensing applications.

Either a thermistor or thermal couples can be used for the temperature sensor. However, the thermistor usually covers a temperature range of less than 150°C, which is not suitable for high-temperature applications. Thus a thermocouple is used in this system. The Type-T thermocouple's temperature range is from -200°C to 350°C and has a sensitivity of about 43μV/°C. The tested point of the thermocouple is embedded in the power module, and the other end of the thermocouple is connected to the motherboard as shown in Figure 3-48. The Seebeck voltage sensed by the thermocouple is shown as below:

$$V = \alpha[(T_{J1} + 273.15) - (T_{J2} + 273.15)] = \alpha(T_{J1} - T_{J2}) \quad (3\text{-}3)$$

Since the Seebeck voltage is very small, an amplification circuit using the high-temperature op-amp is built in the motherboard.

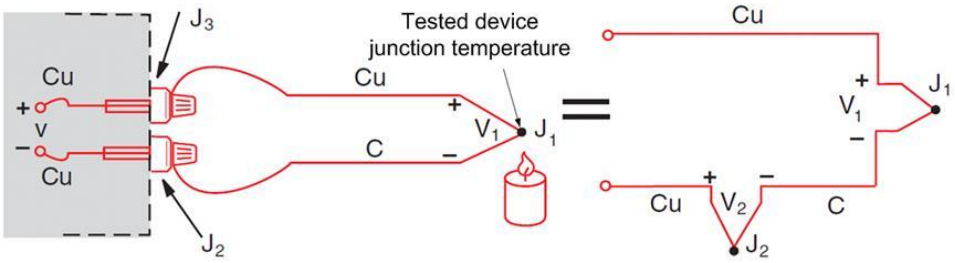


Figure 3-48 Thermal couple connection in the system

Both the sensed voltage and sensed temperature are sent to the protection circuit, which is composed of high-temperature op-amps and a high-temperature D-type flip-flop. Once the protection is activated, the turn-on pulses will be cut off and only turn-off pulses are applied for the refreshing functions tostatically turn off the SiC JFET.

3.5.3 Controller Design:

A high-temperature analog PWM controller from Cissoid (CHT-MAGMA) is used as our system controller. An integral controller with a soft-start circuit is built to achieve voltage loop control. As shown in Figure 3-49, the soft-start function will guarantee the compensation voltage starts at zero, which means the duty cycle will also start at zero.

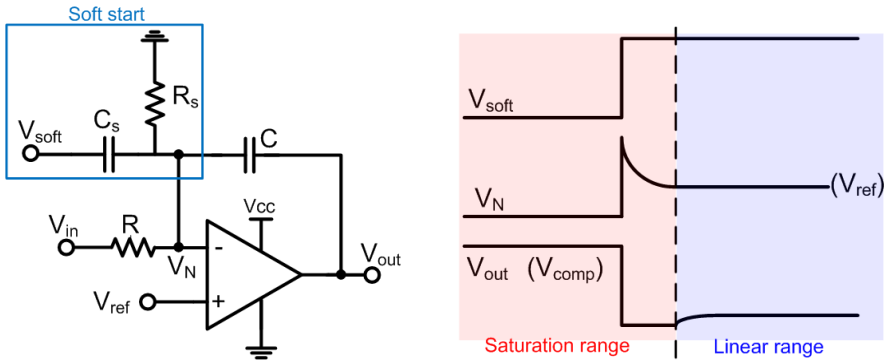


Figure 3-49 Controller and soft start

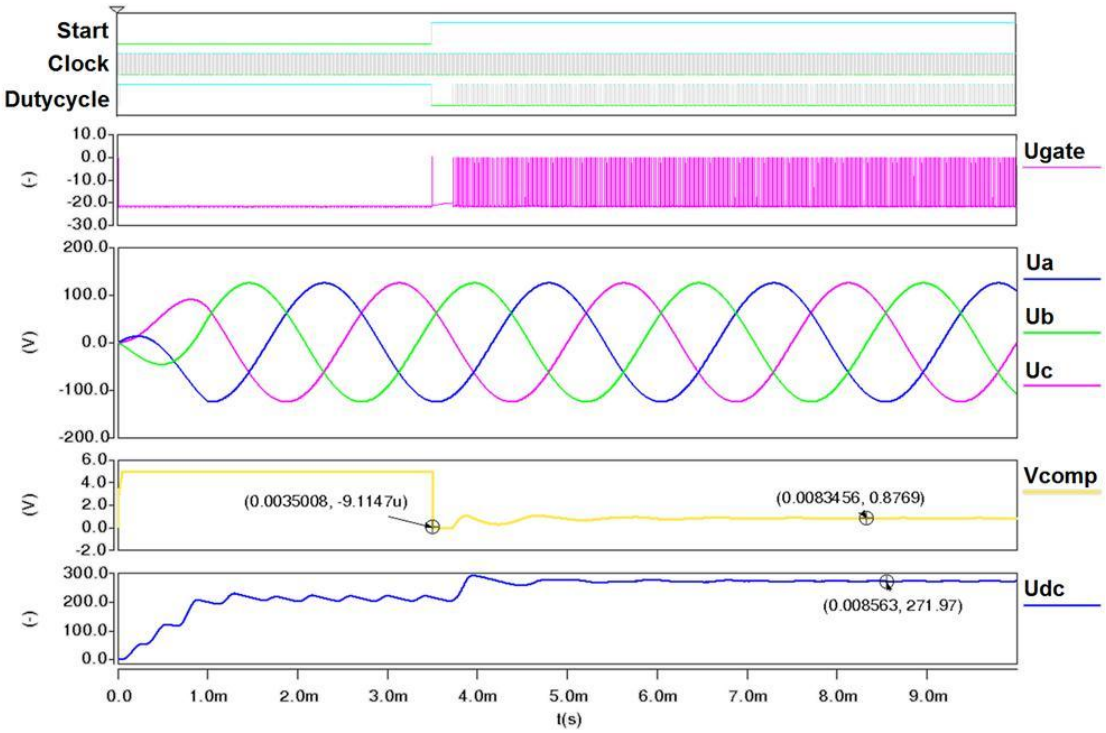


Figure 3-50 Simulation for the start process

The system start process is simulated and shown in Figure 3-50. This start process can be divided into two subintervals. At the beginning, the JFET is always turned off by applying the refreshing signals that will generate refreshing turn-off pulses to the gate drive circuit. The gate-source voltage is clamped lower than pinch off voltage, and the system works as a diode rectifier. When the start signal become active, the system converts from diode rectifier mode to PWM rectifier mode. The DC-link voltage is regulated at 270V. The soft-start function will gradually increase the duty cycle from zero to the rated value.

3.5.4 System Thermal Design:

The targets for the system thermal design before the real test are temperature prediction and better thermal management. Once the main devices, switching frequency and operation point are fixed, the detailed power module loss can be

calculated using Saber® tools. With the loss calculation results, thermal simulation tools such as ePhysics can be used to predict the temperature distribution for the power module with an assumed air-cooling speed , ambient temperature and system layout.

In order to have a 1.4 kW power output and not exceed the peak current, which is 12 A for this device, the power module will only operate in continuous current mode (CCM). The loss distributions for different components based on the CCM mode of operation are summarized in Figure 3-51. However, if working in DCM mode, the output power can only be 500W.

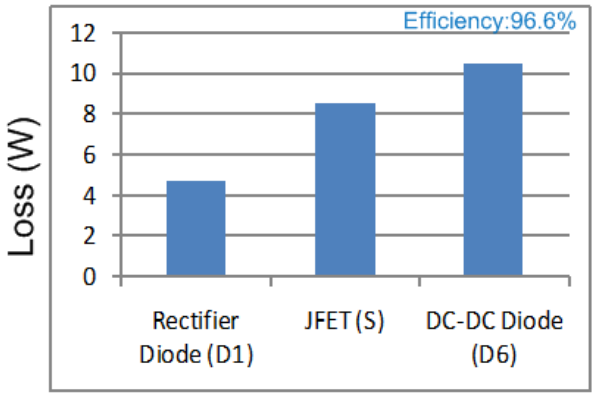


Figure 3-51 Loss distribution in the power module

Ansoft Ephysics is utilized as the tool to conduct the thermal analysis. The thermal performance simulation results with detailed loss distribution for the power module is shown in Figure 3-52. With the assumption of 150°C ambient temperature, heatsink dimensions of 6×6×1.5 cm^3, and 1m/s airflow speed, the maximum junction temperature of the power module reaches 240°C, which is lower than the designed maximum value of the planar structure power module. The embedded thermocouple is 1cm away from the JFET.

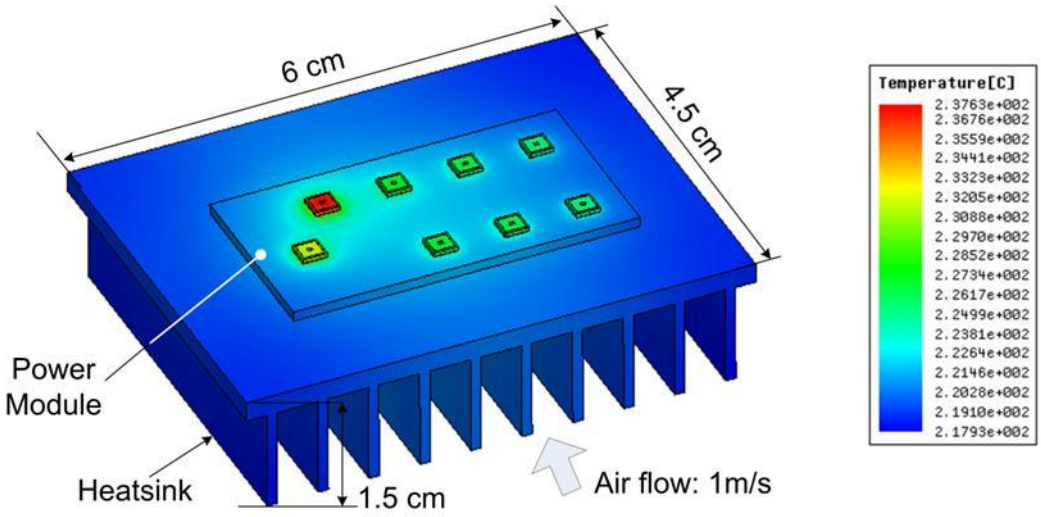


Figure 3-52 Thermal performance simulation results for the power module

The system prototype is shown in Figure 3-53. All the functions are defined and marked in the picture. The dimensions of the motherboard are 16.5cm×14cm, and the hybrid structure power module is put under the motherboard as indicated. The figure also shows that the power module occupies only a small portion of the footprint of the converter. The next section contains a detailed discussion about power density and benefits of high-temperature converter design.

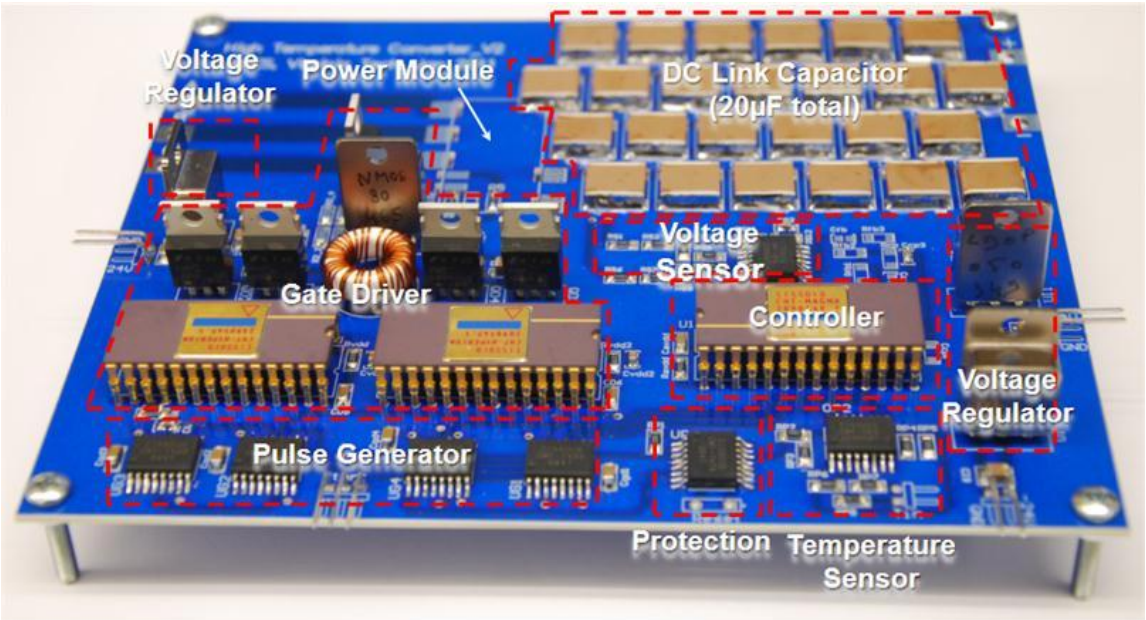


Figure 3-53 System prototype

3.6 Experimental Results

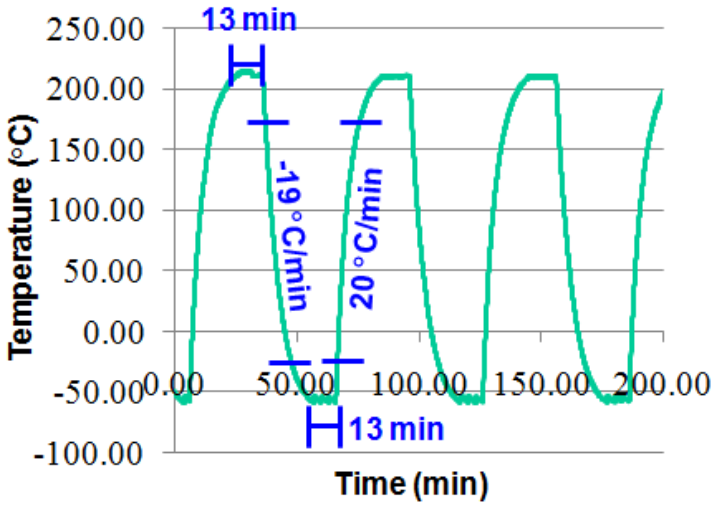
To verify the unit's ability to operate in a harsh environmental, both the components and the system are tested and debugged. This section shows the results of the thermal tests on some high-temperature components and the high-temperature converter debugging process in a harsh environment condition emulated by a thermal chamber.

3.6.1 Components Thermal Test:

As shown in the surveyed high-temperature capacitor results in Fig. 10, the ceramic capacitors are selected for both the DC-link capacitors and the control capacitors. Because surface-mounted chip capacitors are susceptible to fracture from thermally induced stresses, which may be caused by the capacitor itself or by the soldering process [140], the larger volume or thicker ceramic capacitors such as the DC-link capacitors (500V, 0.4μF, 3941XHT404M6P5) may make the thermal stress problem more severe.

The MIL-STD-883H standard [141] are used as a reference to conduct the thermal cycling tests for evaluating the reliability of the high-temperature ceramic capacitors under thermal stress. Meanwhile, the high-temperature PCB board (Roger 4350) and high temperature solder are also verified using the thermal cycling test.

(a) Tenny environment chamber



(b) Tested temperature profile

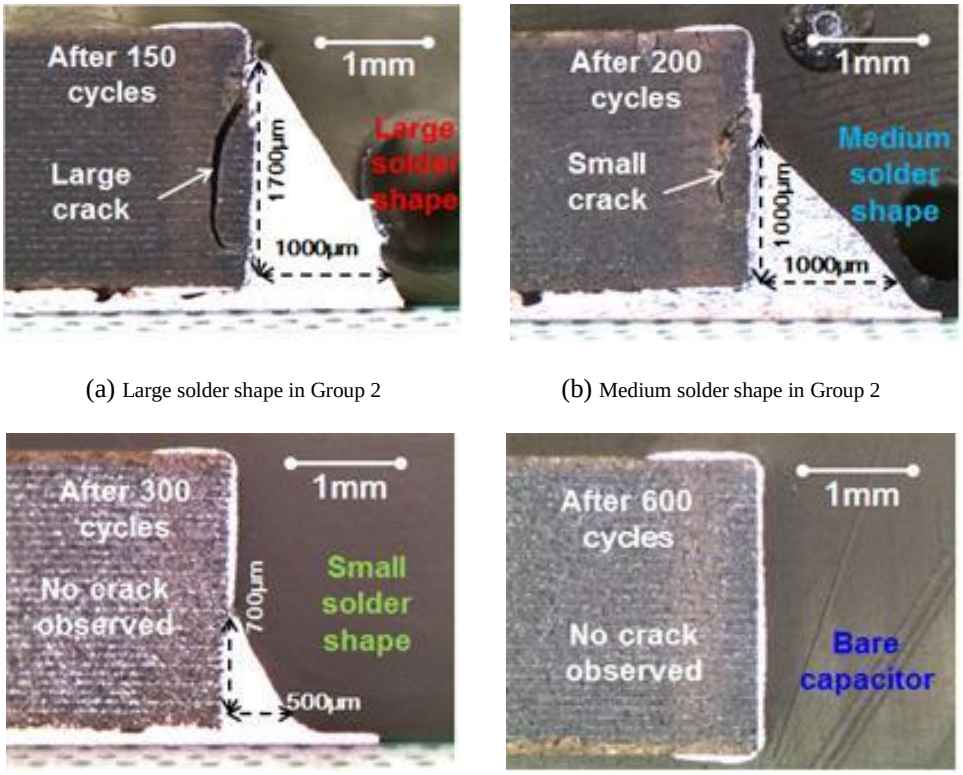
Figure 3-54 Thermal-cycling chamber and profile

A Tenney TUJR thermal-cycling chamber is used for testing. Figure 3-54 shows the thermal cycling chamber and profile. The thermal cycling temperature ranges from -50°C to 200°C. Each cycle lasts for one hour, and the hot and cold temperature duration time is 13 minutes. The maximum slope we can achieve is roughly 20°C/min.

For the ceramic capacitor, the middle electrode layers usually have a higher CTE than the ceramic layer, which tends to force the capacitor apart when heated. In

addition, after the ceramic capacitors are soldered to the high-temperature PCB, the PCB and solder CTE may also increase the thermal stress at the terminal and cause the capacitors to crack. To verify the thermal reliability of the high-temperature capacitors, 10 pieces of high-temperature DC-link ceramic capacitors samples were divided into two groups: five bare capacitors comprised Group 1, and five capacitors soldered on top of the high-temperature PCB board (Roger 4350) comprised Group 2. Different solder shapes were employed for Group 2. All these samples are put into the thermal-cycling chamber for cycling.

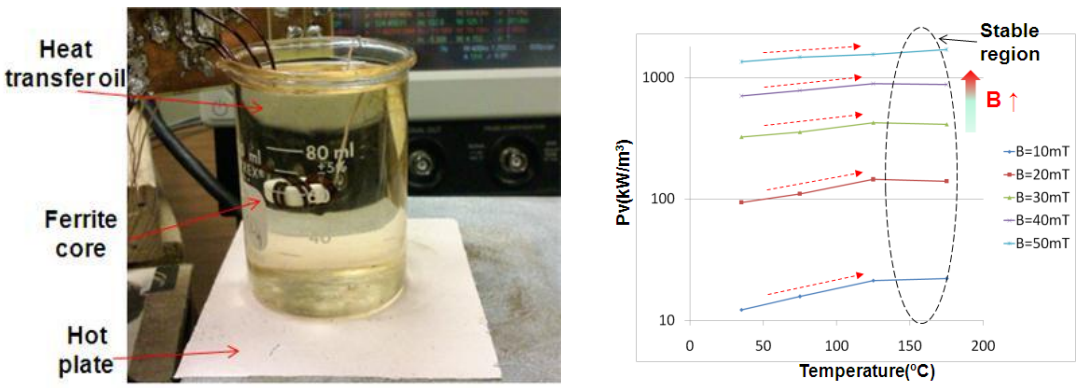
After the thermal cycles, the samples were mounted in molding epoxy for cross-sectioning and polishing. The cross-section view of these tested samples under microscope (STEMI-2000-C) is shown in Figure 3-55. Figure 3-55(a) to (c) indicate the samples that were soldered on the high-temperature PCB board with large, medium and small solder shapes. Figure 3-55 (d) illustrates the bare capacitors without soldering on top of the PCB board in Group 1. The bare capacitor has no crack observed even after 600 cycles. As shown in Figure 3-54 (a), a larger solder shape will generate more thermal stress to the capacitor and can create cracks even after only 150 cycles. Reducing the solder shape will help to reduce the thermal stress seen in Figure 3-55 (b) and (c). After 300 thermal cycles, the Group 2 samples with a small solder shape have no obvious changes in terms of appearance, capacitance value, or breakdown voltage level. In order to use the ceramic capacitor in high-temperature applications, we need to control the solder shape to a small value. To further reduce thermal stress and improve the ceramic capacitor thermal reliability, external through-hole leads can be utilized. Meanwhile, no obvious change is observed after 300 thermal cycles for the high-temperature PCB and solder.



(a) Large solder shape in Group 2 (b) Medium solder shape in Group 2

(c) Small solder shape in Group 2 (d) Bare capacitor in Group 1

Figure 3-55 Thermal cycling test for the high-temperature ceramic capacitor, cross-section view (-55~200°C)



(a) Core loss measurement setup (b) Core loss measurement results

Figure 3-56 High-temperature ferrite core loss measurement

Besides the high-temperature capacitor thermal reliability test, the high-temperature, low-permeability NiZn ferrite toroid cores (4C65) from Ferroxcube are also tested with respect to different ambient temperatures. Using the core loss measurement

method shown in [142], Figure 3-56 shows the high-temperature ferrite core loss measurement setup and results. The small high-temperature core used for the gate drive is dipped into the high-temperature heat transfer oil, whose temperature is controlled by the hotplate.

Several different exciting frequencies are used to measure the core loss. Figure 3-56 (b) shows the core loss measurement results for one exciting frequency point (1MHz). For most saturation flux values lower than 50mT, the high-temperature ferrite core loss will increase when the temperature increases from room temperature to 125°C ambient. After that, the core loss will stabilize, which guarantees this inductor will not have the thermal runaway problem. For the real design, the primary-side number of turns is selected to be 9, so the maximum flux density will be controlled to a value less than 40mT, as shown in (3-4). Since the tested stray capacitance between the transformers on the primary side and the secondary side is less than 6pF, the designed gate drive circuit will not suffer the dv/dt immunity issue.

$$B_{\max} \le \frac{u \cdot t_p}{n_1 \cdot A_c} = 40mT \tag{3-4}$$

3.6.2 System Harsh Environment Test:

With consideration of the thermal chamber inside space, the Envirotronics Thermal Chamber is selected to emulate the harsh environment for the soaking test. Nine different ambient temperature test points with 25°C steps from -50°C to 150°C were tested.

Figure 3-57 shows a picture of the converter inside the thermal chamber. The thermal chamber creates a harsh environment, with temperatures ranging from -50°C to 150°C. The thermocouple, 200°C monitor wires and power wires are connected outside the chamber through a hole that is sealed with a sponge plug. Several key

point temperatures monitored by the thermocouple are marked in the picture. Due to a lack of high-temperature fans that we can put inside the thermal chamber, the motherboard test and the power test are conducted separately inside and outside the thermal chamber.

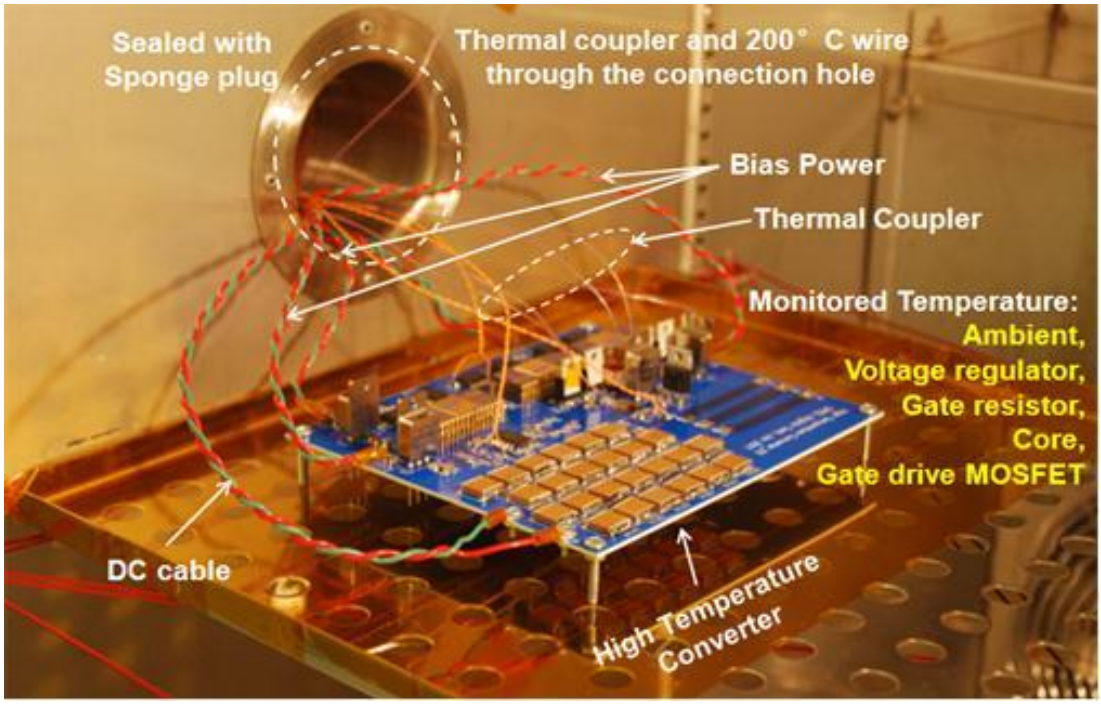
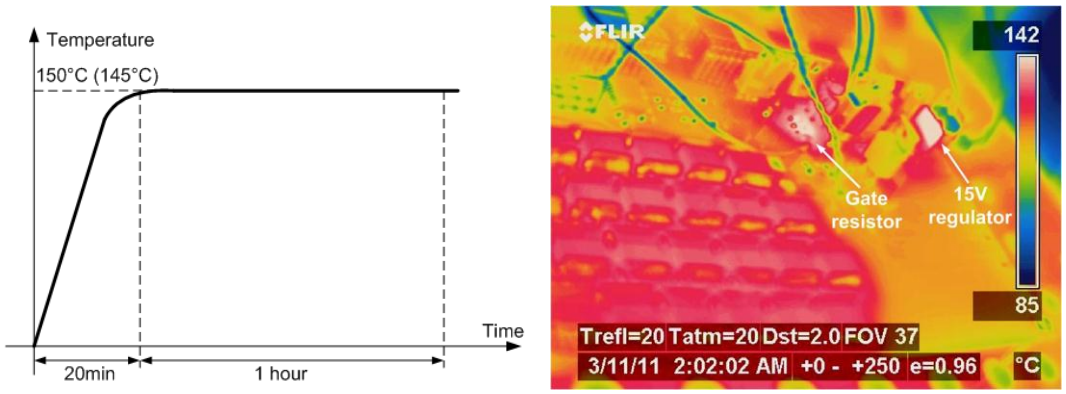


Figure 3-57 Picture of converter inside the thermal chamber



(a) Temperature profile for the soaking test (b) Thermal camera picture after the soaking test

Figure 3-58 Temperature profile and thermal camera picture after 150°C soaking test

For the motherboard test inside the chamber, the system is working as an open loop, and the fixed duty cycle is set. All the functions except the power module can be

verified during the nine temperature soaking tests. The 150°C ambient temperature soaking test is shown in Figure 3-58 to Figure 3-60. Figure 3-58 (a) shows the temperature profile for the 150°C soaking test. The temperature inside the thermal chamber increases from room temperature to 145°C (the steady state is 5°C less than the reference, as monitored by the thermocouple) within 20 minutes. Then the thermal chamber temperature stays constant for one hour. Figure 3-58 (b) shows the thermal camera picture after the 150°C soaking test. After the soaking test, the thermal chamber door is opened, and a picture is taken with the thermal camera outside the chamber. Because of the long distance between the thermal camera and the high-temperature converter, the value shown in the thermal picture may have some error. In addition, the internal metal case of the thermal chamber also reflects some infrared due to the ambient temperature after we open the door. However, we can still clearly see the gate resistor and 24V to 15V voltage regulator are the hottest spots.

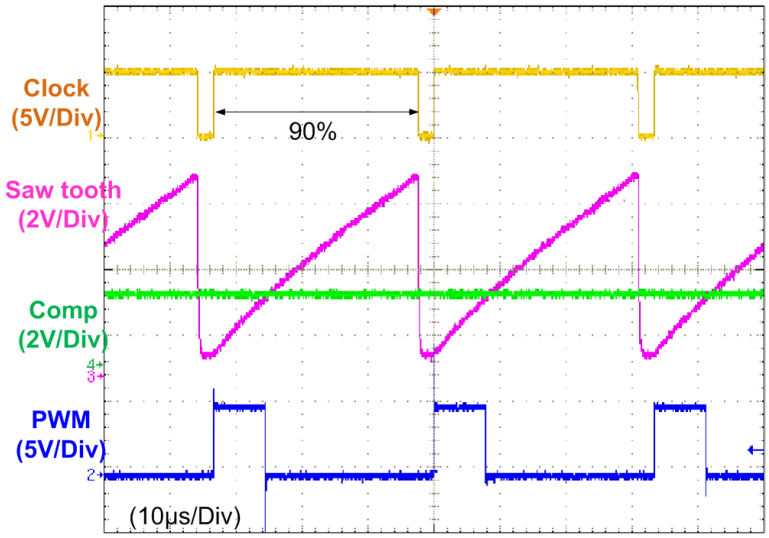


Figure 3-59 PWM generator test in 150°C soaking environment

The PWM generation by the controller is shown in Figure 3-59. The high-temperature CHT-MAGMA PWM controller is selected as our controller in the system. A constant 30 kHz clock signal is generated by the internal oscillator circuit together with the outside RC components. The clock signal duty cycle is 90%. During

the high logic of the clock signal, the sawtooth signal is linearly charged to its maximum value. The sawtooth signal is clamped at zero when the clock signal is at a low level, which means the maximum duty cycle generated by the controller will not exceed 90%.

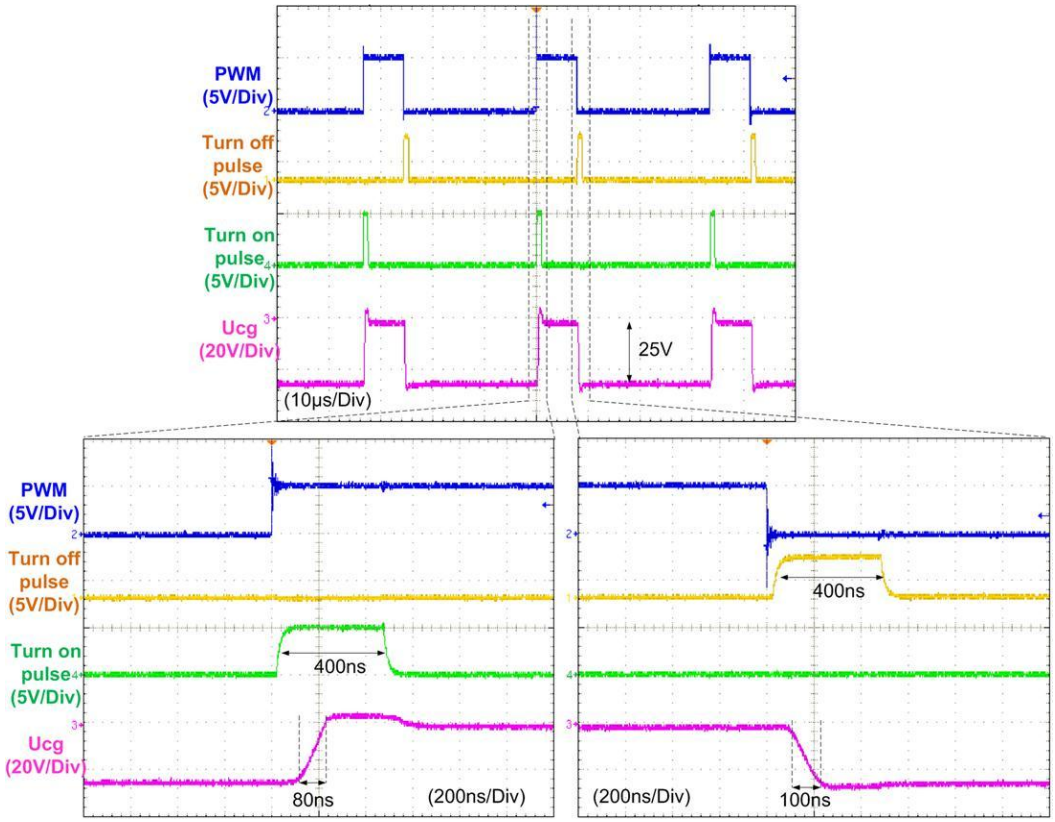
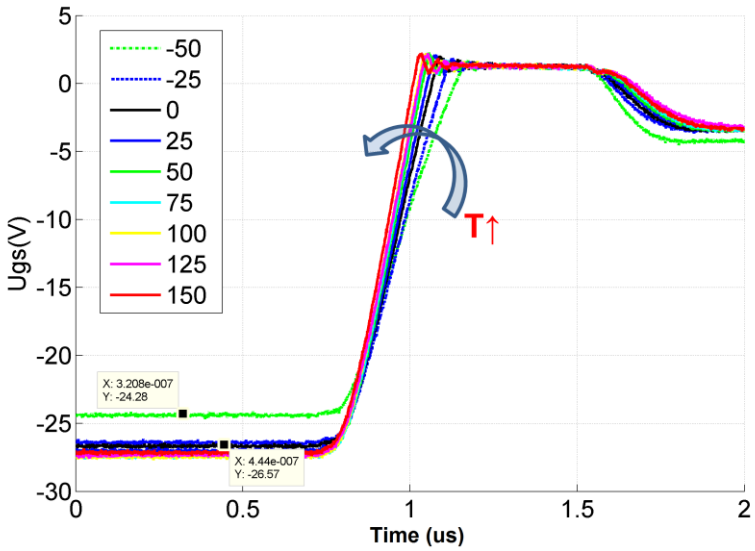


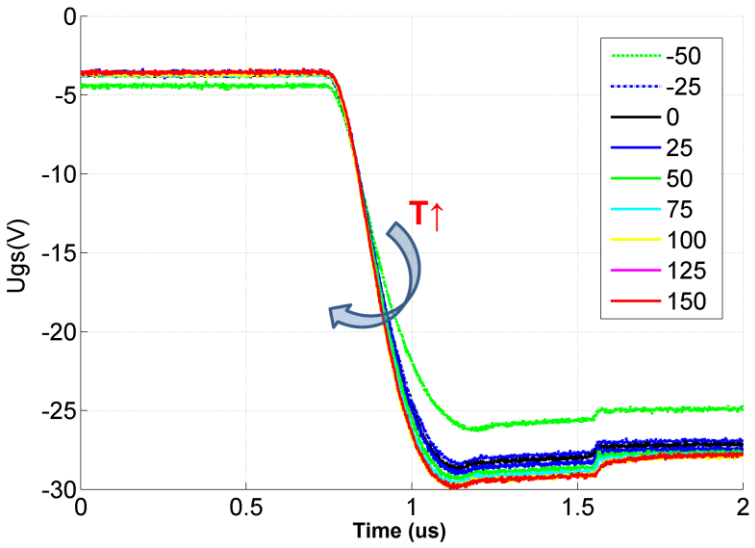
Figure 3-60 Edge-triggered gate drive circuit test results in 150°C soaking environment

Figure 3-60 shows the test results of the proposed edge-triggered gate drive circuit. The PWM signal coming from the PWM controller is transmitting to the pulse generation circuit, which will generate both turn-on and turn-off pulses. The width of the pulse is 400ns. When a positive pulse is applied on the primary side, the secondary-side MOSFET is turned on, which will also turn on the JFET. The turn-on gate slope is 80ns. When a negative pulse is applied on the primary side, the gate capacitor is charged to the negative voltage (-25V) through diode D2, which will turn off the JFET. The turn-off gate slope is 100ns.

The influence of different ambient temperatures on the converter performance is demonstrated from Figure 3-61 to Figure 3-64.



(a) Turn-on slope



(b) Turn-off slope

Figure 3-61 Monitored gate drive signal during harsh conditions

Figure 3-61 shows the monitored gate drive signal in different harsh environments. Both the turn-on and turn-off slopes become faster when the ambient temperature increases. The major reason for this is because the value of X7R capacitor Cg (4nF) from Fig. 15 will decrease 20% when the temperature goes up to 150°C. Besides the gate drive speed, the steady-state turn-off gate drive voltage is also influenced by different ambient temperatures. When the ambient temperature goes to -50°C , the

voltage is -24.3V. This is because the output voltage of the 15V voltage regulator (CHT-LDOP-150) will decrease when the ambient temperature decreases, especially when the ambient temperature reaches -50°C. Since the primary-side supply voltage decrease will lead to a voltage drop on the secondary side, the pulse transformer gate drive circuit will be sensitive to the supply voltage on the primary side.

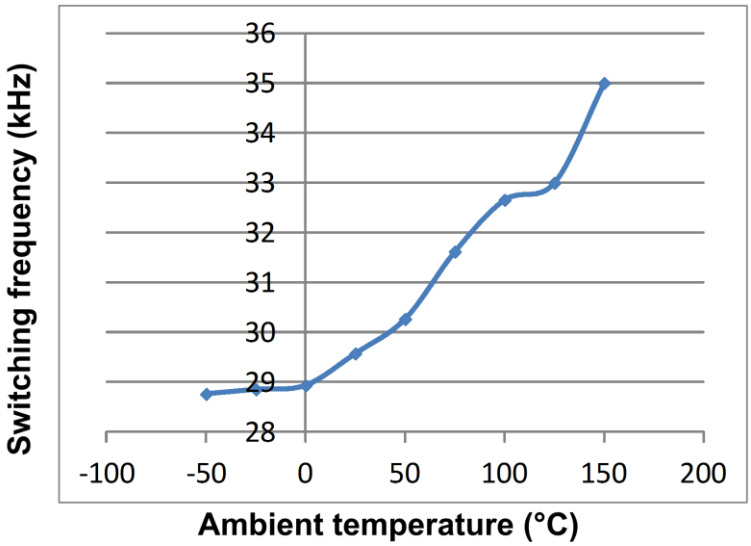


Figure 3-62 Monitored switching frequency during harsh environment

Figure 3-62 illustrates the monitored switching frequency with different harsh environments. As mentioned above, the switching frequency signal is generated by the clock output pin of the high-temperature analog controller chip (CHT-Magma), as shown in Figure 3-59. The clock signal is generated by an internal oscillator with both internal and external RC components. The passive components temperature dependence will cause a 15% change in switching frequency when the temperature increases from -50°C to 150°C.

The monitored temperatures for all the test points are summarized in Figure 3-63. As shown in Figure 3-58 (b), the gate resistor and voltage regulator are the hottest

spots in the system. All other monitored temperatures are within 10°C above the ambient temperature.

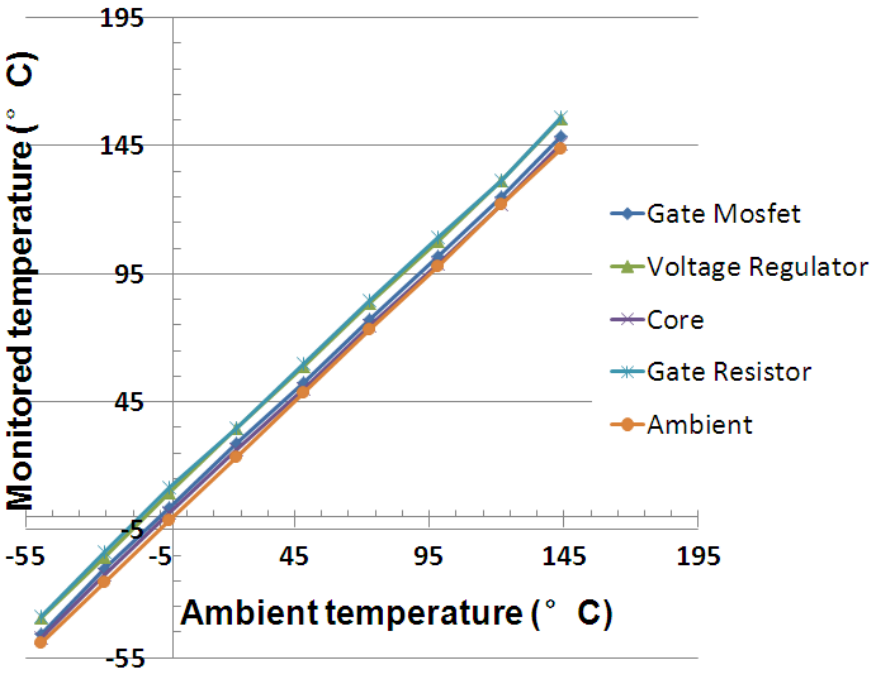
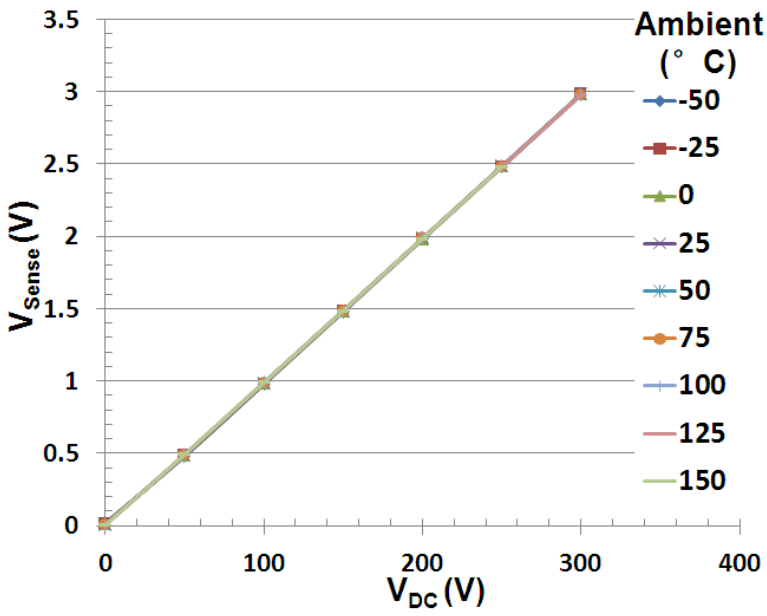
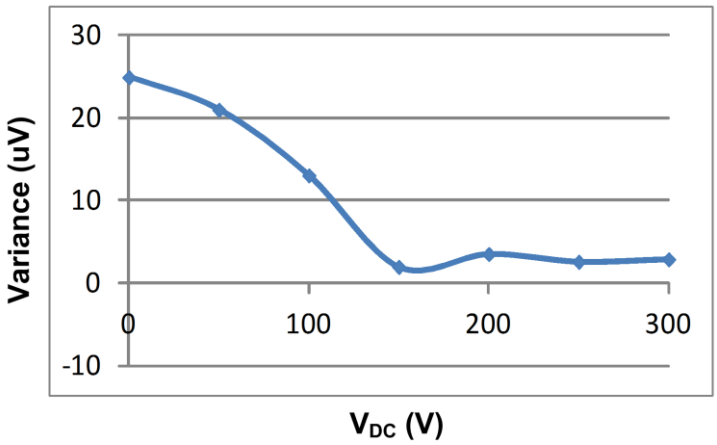


Figure 3-63 Monitored temperature point



(a) Voltage sensor test results



(b) Voltage sensor variance results

Figure 3-64 Voltage sensor test in harsh environments

Since the controlled DC-link voltage is 270V, the voltage sensor conversion ratio is designed to be 100.

Figure 3-64 shows the voltage sensor test at different ambient temperatures. Because of the three-op-amp structure shown in Figure 3-47, the input resistor's positive temperature coefficient will be canceled, and the voltage sensor results stay almost the same for different ambient temperatures. The voltage variance for different testing points can be controlled to be less than 30μV.

The power test with both the motherboard and power module is conducted outside the thermal chamber since no high temperature fans are available to put into the thermal chamber.

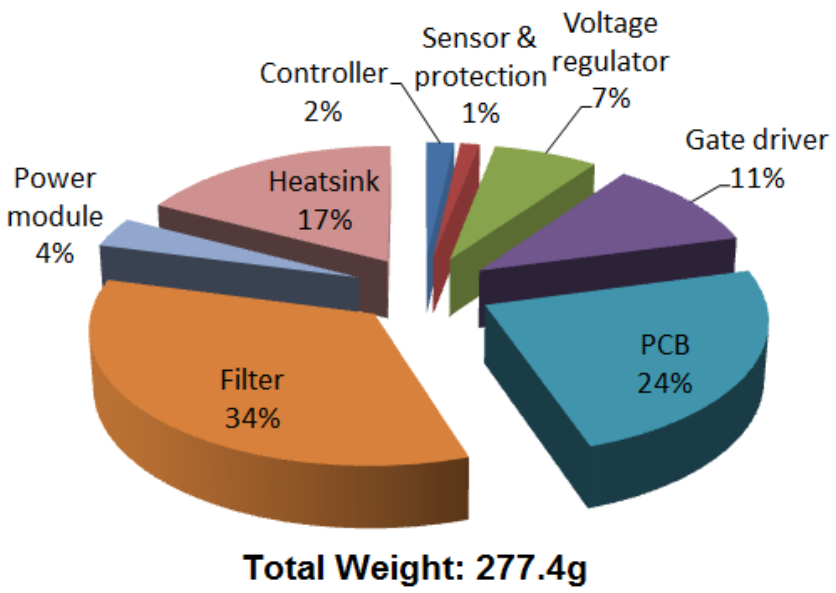
Based on the test results, the high-temperature power module in a hybrid structure meets the requirement of a 250 °C junction temperature. Compared with a traditional wire bonding packaging structure, the hybrid packaging structure will have a smaller footprint and smaller parasitics, which will lead to less loss and voltage stress to the devices. Therefore, the hybrid packaging structure is more suitable for SiC high-temperature applications. In addition to this, the three-dimensional lead frame structure of the hybrid power module will provide more flexible routing. However, to

push the device junction temperature to a higher value will increase the system loss and decrease the efficiency, as shown in Table 3-6. The major reason for the higher loss is due to the positive temperature on resistance of the SiC diode and JFET.

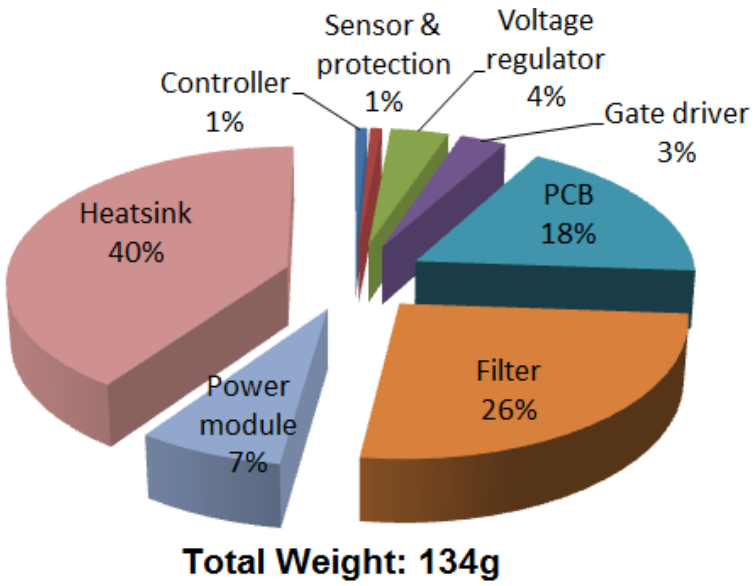
Besides the power module, the motherboard provides the capability of working up to 150 °C ambient temperature. In order to achieve this, silicon-on-insulator chips together with other high-temperature components are utilized to provide the functions as sensor, protection, controller, gate drive and filter. The proposed edge-triggered gate drive method is verified in high-temperature applications with simple topology and smaller loss. The hotspot of the gate resistor is only 12°C higher than the ambient temperature. However, since both the power and signal are transferred from the gate drive primary side to the secondary side within the pulses, refreshing functions need to be designed to statically turn off the JFET. Meanwhile, the gate drive speed and the turn-off voltage level will be influenced by the passive components and voltage regulator temperature characteristics. A high-temperature analog controller is utilized in this prototype, and the switching frequency may change due to the passive components' temperature dependence. Three op-amp structure voltage sensors cancel the temperature dependence effect of the passive components, and are suitable for high-temperature applications. A high-temperature ceramic capacitor is adopted to achieve the dc link filtering function. In order to increase the thermal reliability of the ceramic capacitor, thermal stress needs to be reduced by using a smaller solder shape or an external through-hole lead frame.

As mentioned above, the fabricated high-temperature system is not as compact as we expected. The total weight of the 1.4kW high temperature prototype is 277g, and the detailed weight distribution picture is shown in Figure 3-65 (a). Actually, the fabricated prototype is heavier than the equivalent low-temperature converter with a

similar power level, as shown in Figure 3-65 (b). For the high-temperature version converter, the PCB board and the related control electronics compose a large share of more than 45% of the total weight. This is because of the larger footprint and heavier weight for the high-temperature components, such as SOI or a complicated transformer gate drive design, due to the limited choice of available components. However, this weight ratio may decrease when the converter power level increases. Then, the heaviest parts will be the power module, heatsink and filter. However, if we compare the weight between the high-temperature version and low-temperature version, the heatsink and power module may not be too different, because there is a similar temperature difference between the junction and ambient. However, because of the high ambient temperature, the high-temperature ceramic capacitor is much heavier than the low-temperature version, which still makes the high-temperature converter heavier than the low-temperature converter.



(a). High-temperature version (150°C ambient, 250°C junction)



(b). Low-temperature version (25°C ambient, 125°C junction)

Figure 3-65 Weight distribution of the 1.4kW converter prototypes

However, a high-temperature converter will bring system-level benefits. The potential applications of a high-temperature converter can be transportation applications, such as vehicles, aviation and marine applications. Adoption of more electrical systems in modern transportation will bring benefits to the whole system by reducing the complexity, and can replace the traditional mechanical, pneumatic or hydraulic power. In addition, the total system weight will be reduced and the system power density will be increased, which will reduce fuel consumption while simultaneously reducing emissions. Thus, to design an electrical converter that can work in harsh environment is both critical and valuable. Besides transportation applications, deep-earth petroleum exploration applications also require electrical converters that can work in harsh environments.

Generally speaking, high-temperature converter design is possible, but still constrained by available components. With current technology, high-temperature converters will have a higher cost, heavier weight, and larger volume than equivalent low-temperature converters. Besides the semiconductor devices and related high-

temperature packaging methods, the development of auxiliary components, such as high-temperature control electronics and high-temperature passive components, are desired.

3.7 Conclusions

This chapter presents the detailed design process of a high-temperature SiC three-phase AC-DC converter that can operate at an ambient temperature above 150°C. The SiC diodes and JFET are used as the main circuit devices and are packaged in a novel high-temperature hybrid structure. An edge-triggered high-temperature gate drive solution is also proposed to drive the designed power module. In addition, the whole system is designed according to the available high-temperature components, including the passive components, silicon-on-insulator chips and the auxiliary components. Finally, the fabricated lab prototype is tested in a harsh environment ambient for verification.

Chapter 4. Compact EMI Filter Design with Consideration of Parasitic and Coupling

In this chapter, a more compact EMI filter design procedure is proposed based on consideration of both low frequency and high frequency attenuation requirement. For simplicity purpose, EMI filter transfer gain is utilized to conduct the analysis. With the proposed method, EMI filter optimum number of stages selection can be derived for both Differential mode (DM) and Common mode (CM). However, in the real application, the source and load impedance also need to be considered. In order to achieve better attenuation prediction without back and forth, the proposed prediction approach in this chapter is based on off line in-circuit measurements that enable accurate prediction of EMI filter performance without time consuming simulations. The last section of this chapter presents the detailed analysis for the magnetic components coupling and its influence on the EMI filter design. It is proved that the magnetic coupling is frequency related and the high-frequency near-field stray flux distribution can be dramatically different compared with low frequency condition. The change of near-field stray flux distribution is caused by the displacement current from the stray capacitors. By using Biot-Savart equation, the high frequency near-field distribution can be well predicted and matched with the experimental results.

4.1 Introduction

Improving power density of power electronics converter has become one of the primary goals in the past few decades. This is especially true for some special applications such as airplanes and electrical vehicles because of limited space and carrier capability. It has been shown that reducing the size of EMI filters can directly

help in achieving higher power density for the converters [25, 26, 143]. These EMI filters usually take 30% of the total converter volume or weight and they cannot be avoided due to the strict EMI requirements on the power converters.

A lot of work has already been done to improve EMI filter performance. The paper [25] systematically studies the impact of the EMI filter on the power density of three-phase PWM converters and proposes a design method for high density EMI filters. The paper [143] discusses the different number of stages influence to the overall EMI filter power density. However, previous works focus only on the low frequency design but the high frequency performance is not addressed properly. Some of the literatures have presented smaller self-parasitic components design by cancellation technologies [91, 92] or better passive components selection and integration[144, 145] to counter the degradation in high frequency performance. Papers [84-88] discuss the layout influence on EMI performance including the effect of both self-parasitic and coupling. Papers [102, 104] show the coupling influence in a three phase EMI filter design and also show that magnetic shielding helps to improve the performance. Although most of these papers have shown the problems with EMI filter at higher frequencies and have also provided some post-design solutions, a method to systematically design a minimum volume EMI filter by including consideration of the parasitic at the beginning itself is still unknown.

Meanwhile, EMI filter attenuation prediction is desired but also a challenge in power converter applications. Time consuming simulations to get noise profiles and the large amount of parasitic elements that count in the noise propagation contribute to this challenge. Another cause of complexity is the multiple uncontrolled noise sources, such as auxiliary power supply and logic circuits. In order to handle this complex problem, some research has been conducted to predict the noise of power

converters. This approach can be basically divided into three families. The first family is the time domain simulation of the converter [94, 95], including all the parasitic and noise sources. The noise spectrum is then obtained by computing the FFT of the resulting currents. This approach gives good results as long as the switches and circuit models are very close to the real physical devices. Meanwhile, the simulation step needs to be very fine for the high frequency analysis resolution which will be very difficult and time consuming for a complex system. The second family of noise prediction techniques are behavioural models [96, 97]. The key idea for this approach is to measure the switching noise profile of a semiconductor for different current levels. Specific measurement techniques are required to obtain good measurement as well as special LISN. Meanwhile, too many unknown variables together with the measurement error also constrain the application in more complex converters. The third family is the frequency domain analysis with an equivalent circuit of the real hardware [94, 95, 98-100]. In the frequency domain, all the circuit impedances are in phase form, allowing very fast computations of the resulting noise spectrum without costly software and time consuming simulations.

Moreover, a more compact EMI filter design will inevitably decrease the distances between the passive components of the EMI filter, which will affect the filter performance significantly by coupling in the EMI spectrum range [27, 28]. A lot of research has been carried out in the past few years to improve EMI filter performance. Generally, there are two non-ideal factors that influence the EMI filter design procedure and performance: self-parasitic and mutual parasitic. Besides self-parasitic as mentioned above, mutual parasitic has a strong relationship between the components coupling. Coupling between filter components has been analyzed in numerous works [85-87, 90, 101, 102] to improve filter performances. Papers [84-88,

103] discuss the layout influence on the EMI performance including the consideration of both self-parasitic and coupling. Papers [102, 104] show the coupling influence in the three phase EMI filter design and also show that magnetic shielding helps to improve the performance. Paper [105] studied the winding imperfection influence on the stray flux.

4.2 EMI Filter Volume Comparison Based on Transfer Gain

This section presents an EMI filter design procedure constructed to achieve the minimum volume with considerations of the component self-parasitic. Based on this design procedure, optimal selection of both EMI filter structures and EMI filter components values can be achieved. Since components near-field coupling effect is not included in this section, more coupling analysis and shielding method are proposed afterwards in section 4.3.

4.2.1 Compact EMI filter design methodology

Most of previous EMI filter design methods mainly consider low frequency noise. Based on the low frequency EMI filter attenuation, the inductance or capacitance can be calculated with a given EMI filter structure. It can be proven that the same value of each individual inductance and capacitance will lead to the smallest total inductance and capacitance. [26, 146] . However, the emergence of new semiconductor devices such as SiC and GaN make it possible for converters to work at higher and higher switching frequencies with very sharp rising and falling edges. Under these conditions, more and more noise will appear in the high frequency range [147]. Therefore, both low frequency and high frequency attenuation now needs to be considered during the design. In this section, all of the analysis and design procedures are based on the DM filter, however, a similar procedure can also been applied to the

CM filter design. A typical LC filter transfer gain is shown in Figure 4-1. The low frequency attenuation can be achieved after the first LC corner frequency by impedance mismatch. However, since the self-parasitic exist in the filter components, the attenuation starts to decrease after the components resonant frequency.

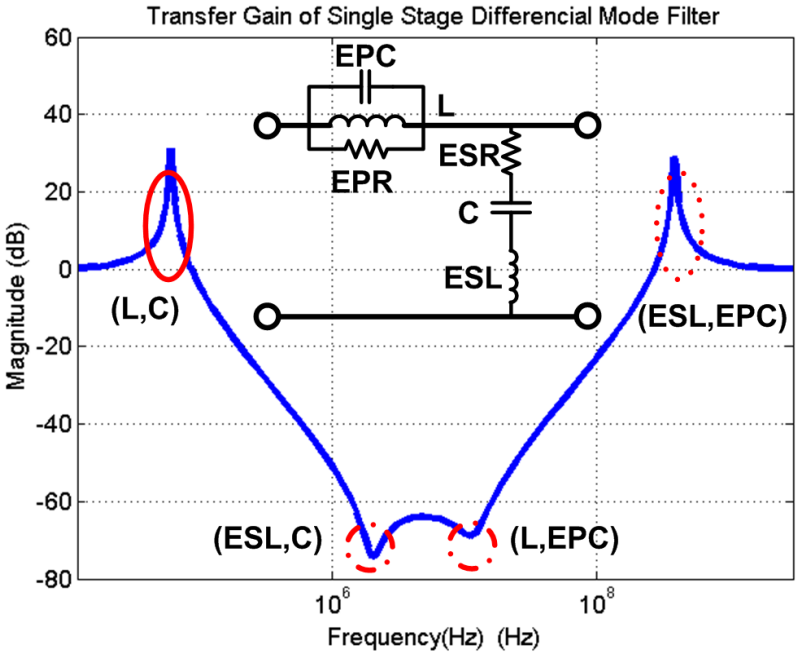


Figure 4-1 single stage LC filter transfer gain

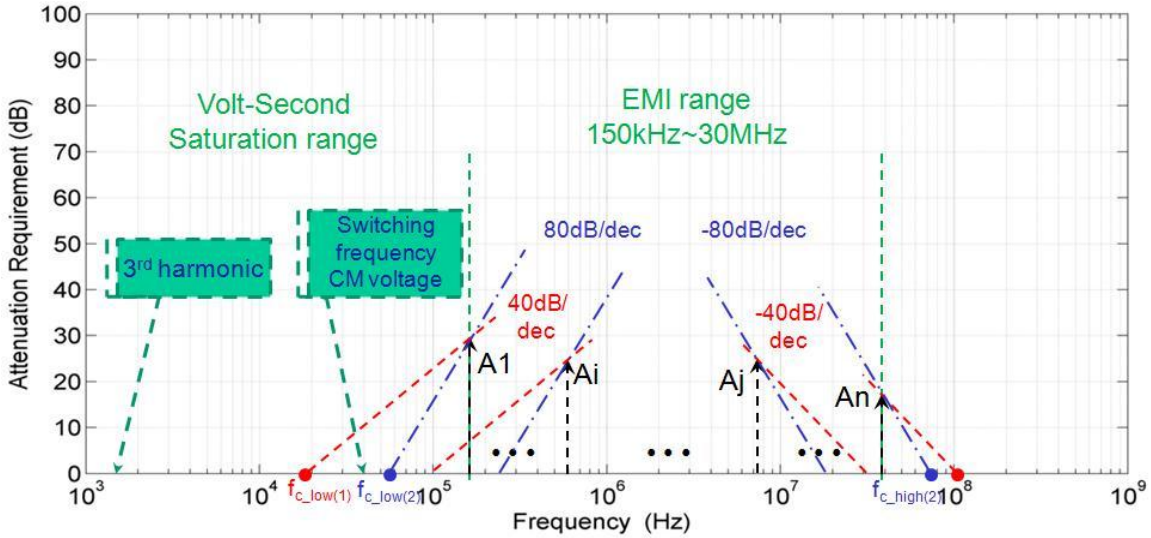


Figure 4-2 Attenuation requirement for low and high frequency

In order to show the design trade-off and trend, the transfer gain is still utilized as a tool for the EMI filter volume analysis. The EMI filter design based on both low frequency and high frequency attenuation is shown in Figure 4-2. Firstly, EMI

attenuation requirement can be derived by comparing the EMI bare noise with the standard. The derived attenuation requirements for both low frequency and high frequency range can be depicted from A1 to An as shown in Figure 4-2. Then, taking N as the number of stages in the filter, a negative $-40\times N$ dB/Dec slope is applied on each attenuation point to determine the lowest corner frequency marked as f_{c_low}. Afterwards, the highest corner frequency f_{c_high} is calculated by applying a positive $40\times N$ dB/Dec slope on each attenuation point. The low corner frequency contains the information of main inductance and capacitance values. The high corner frequency corresponds to the requirement for the components parasitic. Components volume and parasitic model needs to be considered so as to conduct the minimum volume design. The other simplified design assumptions can be classified into the following items:

- Approximated continuous functions is utilized with discrete values determined by the limited choice of cores and capacitors
- No PCB traces incur extra stray capacitance or stray inductance
- A Single RLC lumped model is utilized as the filter element
- Magnetic coupling is not considered
- The Simplified Steimetz equation is utilized to calculate the core loss
- 100°C maximum temperature rise is considered
- Simple heat dissipation function is utilized

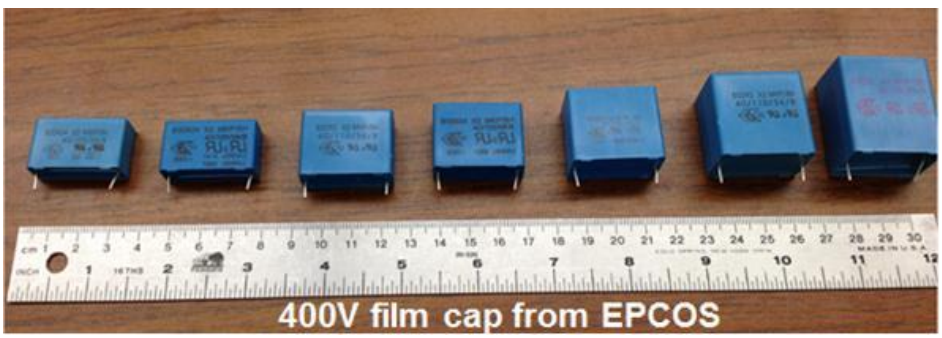
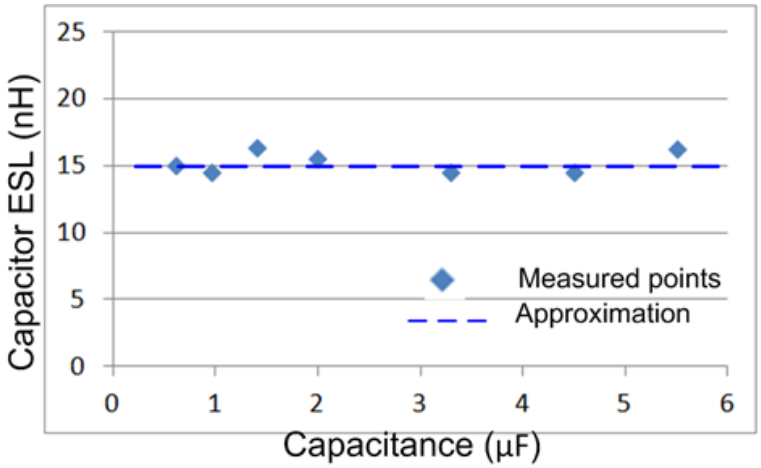
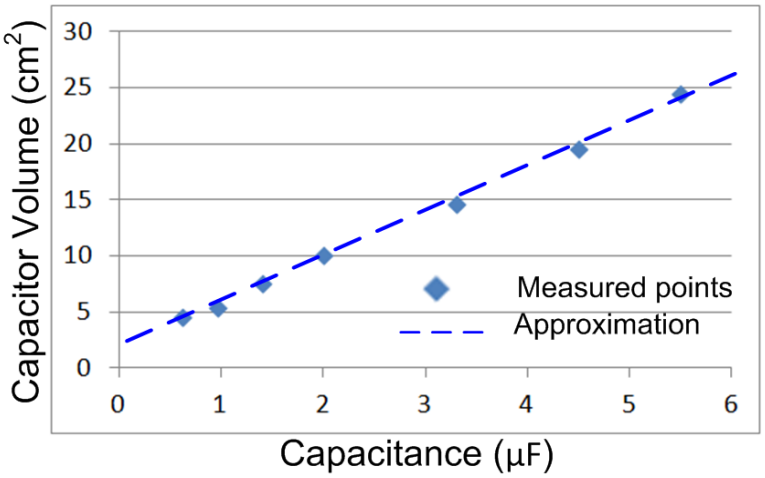


Figure 4-3 DM capacitor



(a) ESL of the film capacitor



(b) Volume of the film capacitor

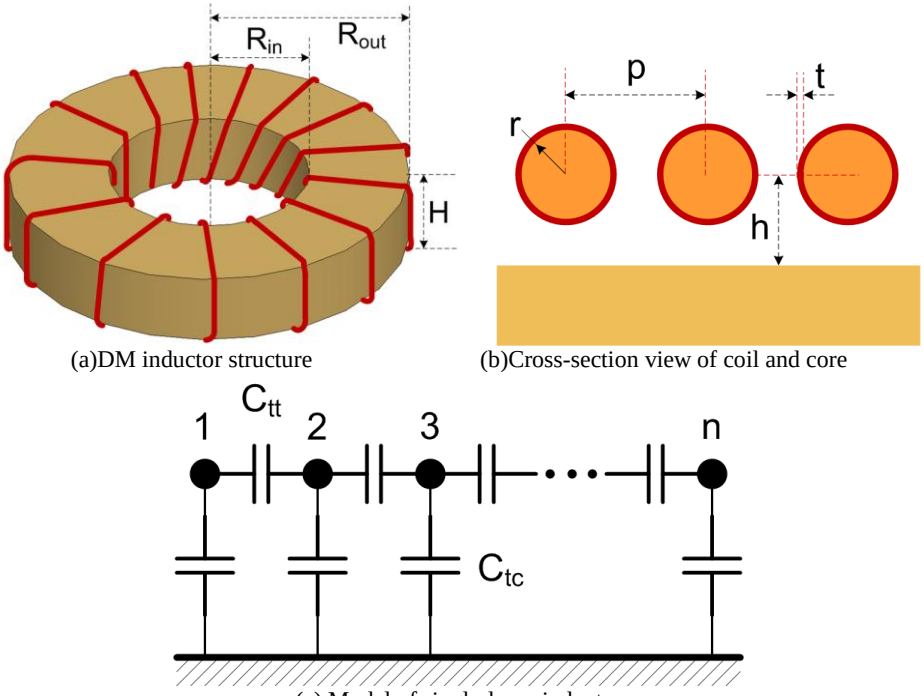
Figure 4-4 DM capacitor (400V film cap from EPCOS) equivalent series inductance (ESL) and box volume

The EMI capacitor is usually a commercial product. Figure 4-3 shows the 400V DM capacitor samples from EPCOS. For a given voltage level, a group of EMI film capacitors volume and corresponding equivalent series inductance (ESL) are shown in Figure 4-4. The ESL value obviously doesn't change with capacitance because all of these capacitors share the same length value, which will dominate the impedance in high frequency range. Based on this, the ESL of the film capacitance can be simply modeled as a constant value for a same type of capacitors. The volume of the capacitor is usually proportional to the energy stored in the cap plus a constant value [143]. The volume of the film capacitors and the curve fitting result are shown in Figure 4-4 (b). The capacitor volume can be expressed in (4-1).

$$V_C = k_{C1} \cdot U_{in}^2 \cdot C + k_{C2} \tag{4-1}$$

Where $k_{C1} = 25cm^3/(F \cdot V^2)$, $k_{C2} = 1.76cm^3$

An inductance value can be derived from the capacitance value and a fixed low corner frequency. Before conducting a minimum volume EMI filter design, DM inductor parasitic and volume model need to be considered.



(a)DM inductor structure (b)Cross-section view of coil and core

(c) Model of single-layer inductor

Figure 4-5 Toroid core DM inductor parasitic modeling

Inductor equivalent parallel capacitance (EPC) has been discussed in previous literatures [148-152]. The DM inductor structure is shown in Figure 4-5 (a). An approximate square shape core area (R_{out}-R_{in}=H) is considered just for simplicity. The inductor is designed with single-layer coil for the purpose of achieving smaller parasitic. The cross-section view of the coil and core is shown in Figure 4-5 (b). The coating thickness of the wire is t. Figure 4-5 (c) shows the equivalent capacitor model of the single-layer inductor. The influence of non-adjacent turns is ignored. The basic cell is composed of turn-to-turn capacitance C_{tt} and turn-to-core capacitance C_{tc}. The turn-to-turn capacitance C_{tt} can be calculated in (4-2) [150] . With the mirror method,

the turn to core capacitance can be expressed in equation (4-3). The total stray capacitance for multiple turns can be shown in (4-4).

$$C_{tt} = \frac{4\pi H\varepsilon_0}{\ln(F + \sqrt{F^2 - (1+t/r)^{2/\varepsilon_r}})} \tag{4-2}$$

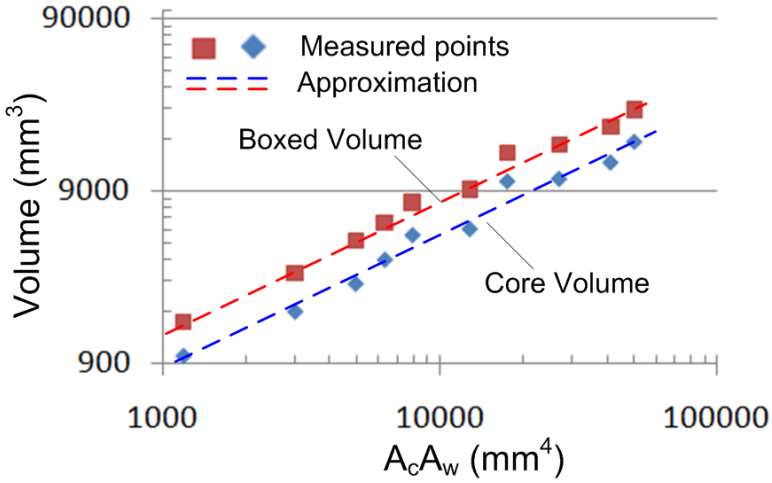
$$C_{tc} = \frac{8\pi H\varepsilon_0}{\ln(F' + \sqrt{F'^2 - (1+t/r)^{2/\varepsilon_r}})} \tag{4-3}$$

$$C_{stray} = \frac{1}{4}(\alpha + \sqrt{\alpha^2 + 4\alpha}) \cdot C_{tt} \tag{4-4}$$

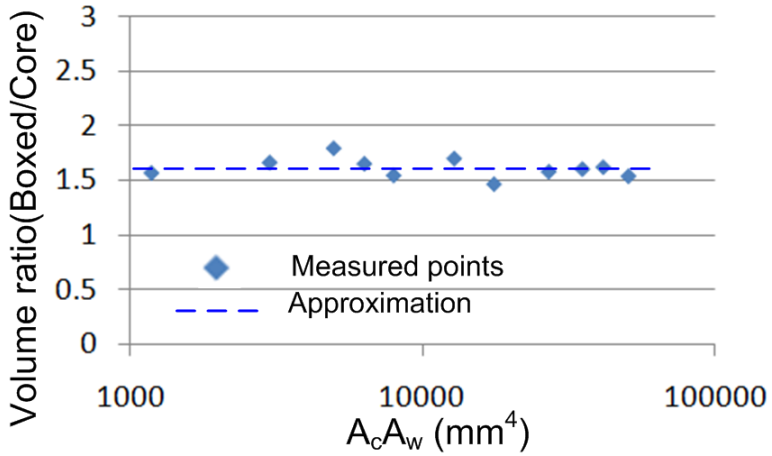
Where $F = \frac{p/2r}{(1+t/r)^{1-1/\varepsilon_r}}$, $F' = \frac{h/r}{(1+t/r)^{1-1/\varepsilon_r}}$, $\alpha = \frac{C_{tc}}{C_{tt}}$

Commercial iron-powder 26 series cores from Micrometals are selected and shown in Figure 4-6. Both the core volume and box volume corresponding to the core-window area product is shown in Figure 4-7. Although the core shape changes, the ratio between the boxed volume and the core volume almost maintains a constant 1.6 as shown in Figure 4-7 (b).

Figure 4-6 Iron powder 26 series from Micrometals (μ=75)



(a)DM inductor core and boxed volume values



(b) DM inductor core and boxed volume ratio

Figure 4-7 DM inductor cores volume modeling

4.2.2 Number of stages influence to EMI filter volume

With all the assumptions above, the optimal volume design is proposed. Suppose the converter requires low frequency attenuation A1 at frequency f1 and high frequency attenuation An at frequency fn as indicated in Figure 4-2. The low and high corner frequency can be calculated as (4-5) and (4-6). Based on the corner frequency and capacitor model, the inductance and its EPC requirement can be expressed as (4-7) and (4-8).

$$f_{c\_Low} = f1 \cdot 10^{\frac{-A1}{40 \cdot N}} \tag{4-5}$$

$$f_{c\_High} = f\,4\cdot 10^{\frac{A4}{40\cdot N}} \tag{4-6}$$

$$L = \frac{1}{(2\pi f_{c\_Low})^2 C} \tag{4-7}$$

$$EPC = \frac{1}{(2\pi f_{c\_High})^2 ESL} \tag{4-8}$$

With a certain inductance requirement, the inductor turns number needs to be higher than $N_{\min}$ to generate enough inductance and lower than $N_{\max}$ to meet the maximum flux density requirement. Then, the minimum inductor dimension can be derived with no margin when the two numbers are equal to each other as shown in (4-9). With the fixed dimension, stray capacitance can be calculated by (4-4) and compared with equation (4-8) as one design criterion. Together with the temperature rise criteria by simple thermal dissipation model with the calculated core and winding loss, the minimum total EMI volume can be determined by sweeping capacitance value over a given range. The design procedure shown above is summarized in Figure 4-8.

$$N_{\min} = \sqrt{\frac{L\cdot L_m}{\mu_0\mu_r\cdot A_C}} = \frac{B_{\max} L_m}{\mu_0\mu_r\cdot I_{pk}} = N_{\max} \tag{4-9}$$

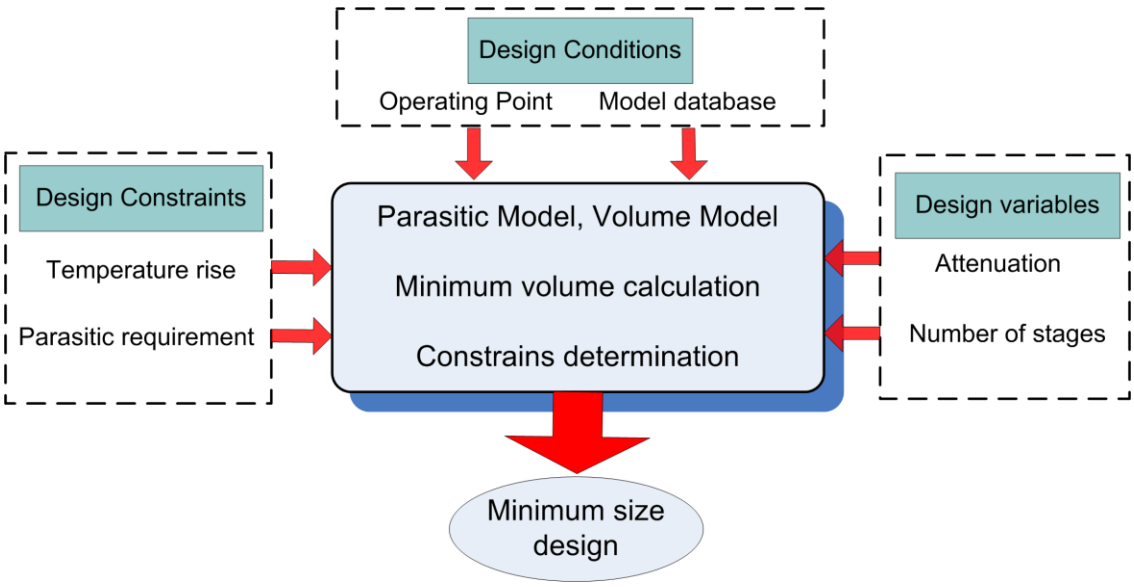
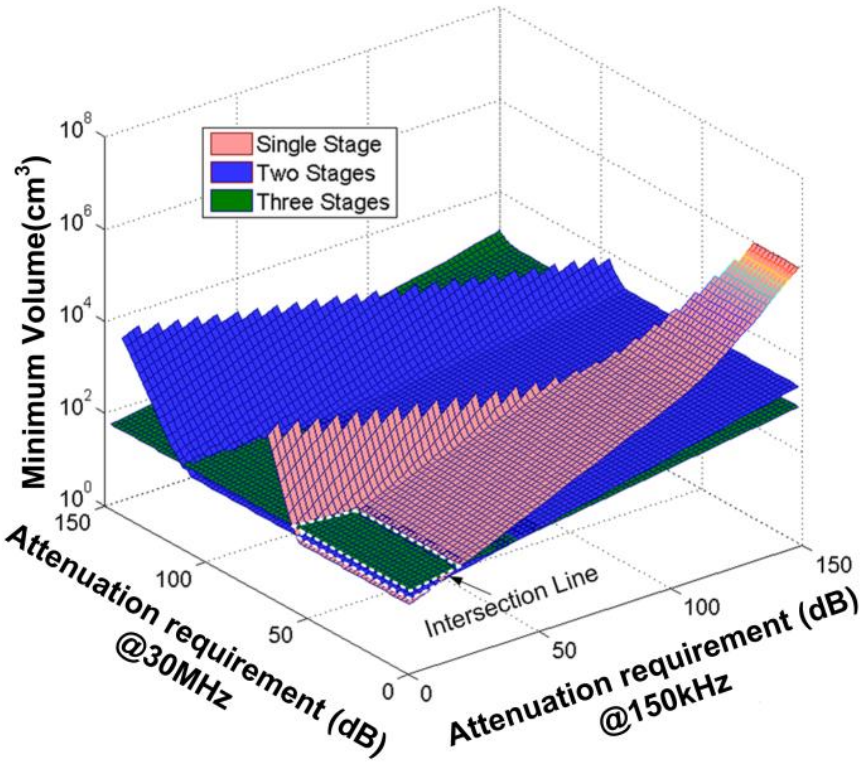


Figure 4-8 Design procedure

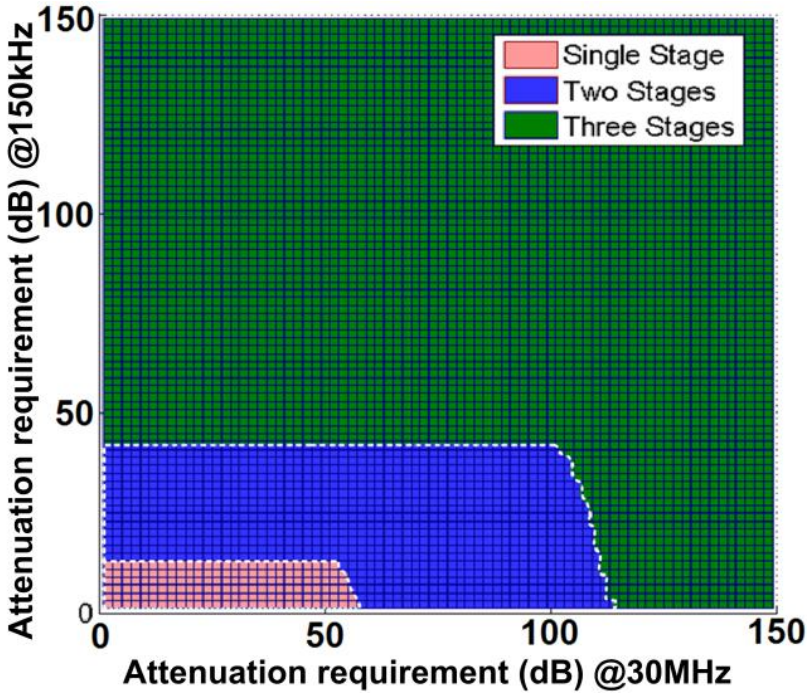
With the proposed design procedure, a minimum volume EMI filter with different low frequency and high frequency attenuations is designed as an example with the given parameters summarized in Table 4-1. The minimum volume EMI filter design result with different EMI stages is shown in Figure 4-9. With consideration of high frequency attenuation, the minimum EMI filter volume will increase when the high frequency attenuation requirement increases. The reason can be explained by the parasitic constrain as shown in (4-8). Single stage EMI filter has smaller volume than multiple stages when both the low frequency and high frequency attenuation requirements are low. However, multiple stages EMI filter lead to smaller volume when both the low and high frequency attenuation requirements are high. Figure 4-9 (b) shows the optimal stages selection with a given low and high frequency attenuation.

Table 4-1 Parameters of case design

Parameters	Values
U_{in}	400V
I_{rms}	20 A
I_{peak}	28.3 A
μ_r	60
J	500A/cm^2
ε_r	3.7
t	0.1 mm
f1	150kHz
fn	30MHz



(a) Minimum volume design



(b) Single stage or multiple stages selection

Figure 4-9 Low and high frequency attenuation influence to the EMI filter design

Two different cases are utilized to demonstrate the number of stages influence to the EMI filter design.

A. Case 1 Demonstration:50dB @150kHz, >30dB@30MHz

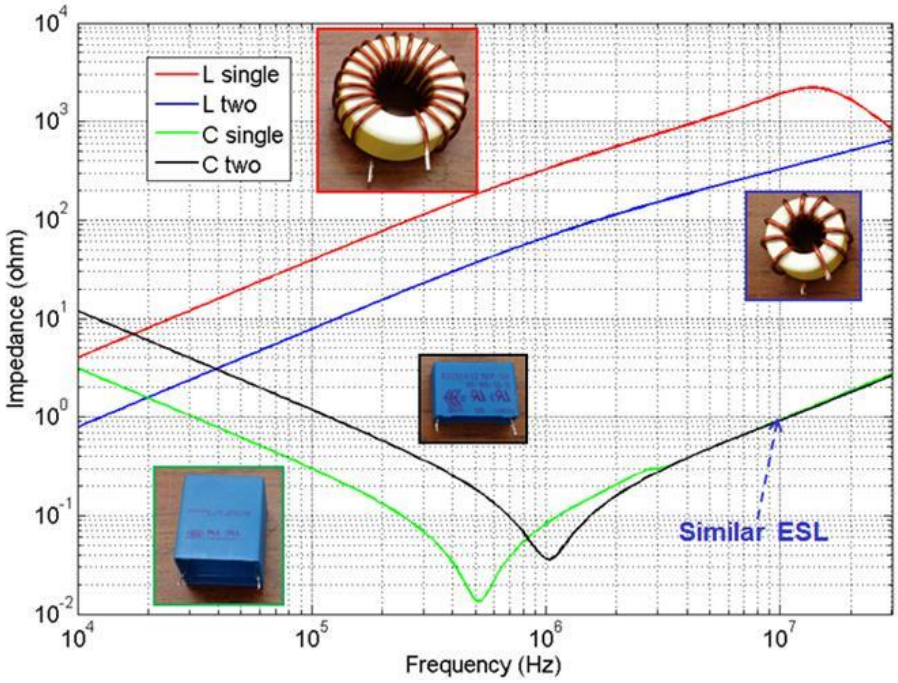


Figure 4-10 DM Components impedance test

According to the design procedure indicated in Figure 4-8, the components for the DM inductor and capacitor are selected from the available samples for the specified operating point. Both single stage and two stages DM EMI filters are designed. The components impedance are measured and shown in Figure 4-10. The measured capacitor impedance also indicates that the single stage DM capacitor and two stages DM capacitor have similar ESL.

Figure 4-11 shows the fabricated single stage and two stages DM filters with the designed components. The detailed comparison between the single stage EMI filter and the two stages EMI filter is summarized in Table 4-2. The real designed value matches well with the predicted design value. According to the design results, the two stages EMI filter is almost half the size when compared with the single stage EMI filter for this operation point. The fabricated single stage EMI filter volume is 61.5 cm^3 and the two stages EMI filter volume is 34.5 cm^3.

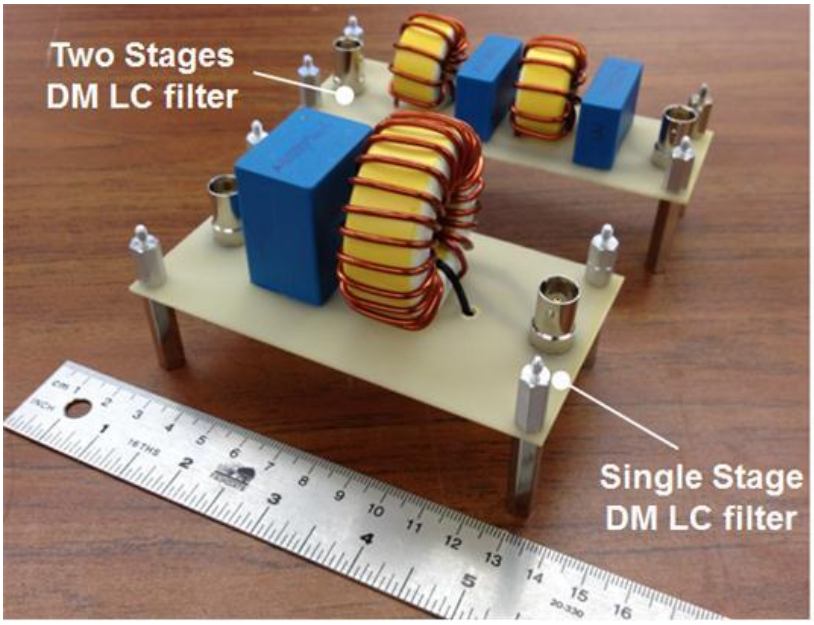


Figure 4-11 Single stage and two stages LC filter

Table 4-2 Comparison result

	C (μF)		L (μH)		Saturation turns		V_{total} (cm^3)	
	Predicted	Real	Predicted	Real	Predicted	Real	Predicted	Real
Single stage	5.5	5.67	57.7	61.4	21	20	54.92	61.5
Two stages	1.5	1.36	12.6	13.2	11	10	29.15	34.5

Figure 4-12 shows the transfer gain test for single stage and two stages DM filters. Both of them achieve approximate 50dB attenuation at around 150 kHz. Because of the smaller component parasitic in two stages filter, the high frequency attenuation (@30MHz) performance is better than single stage EMI filter which matches our previous analysis.

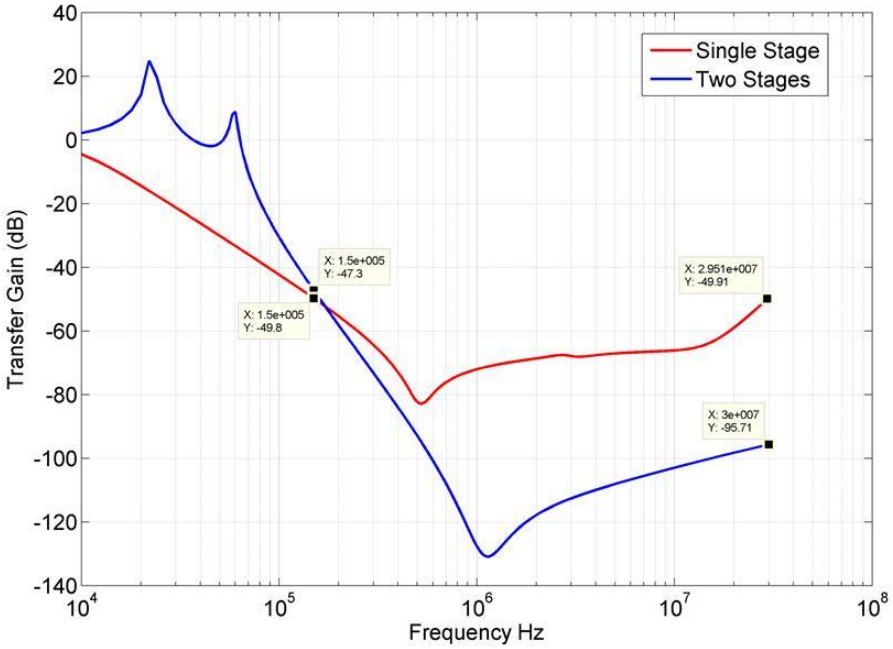


Figure 4-12 Transfer gain test

B. Case 2 Demonstration:15dB@150kHz, >30dB@30MHz

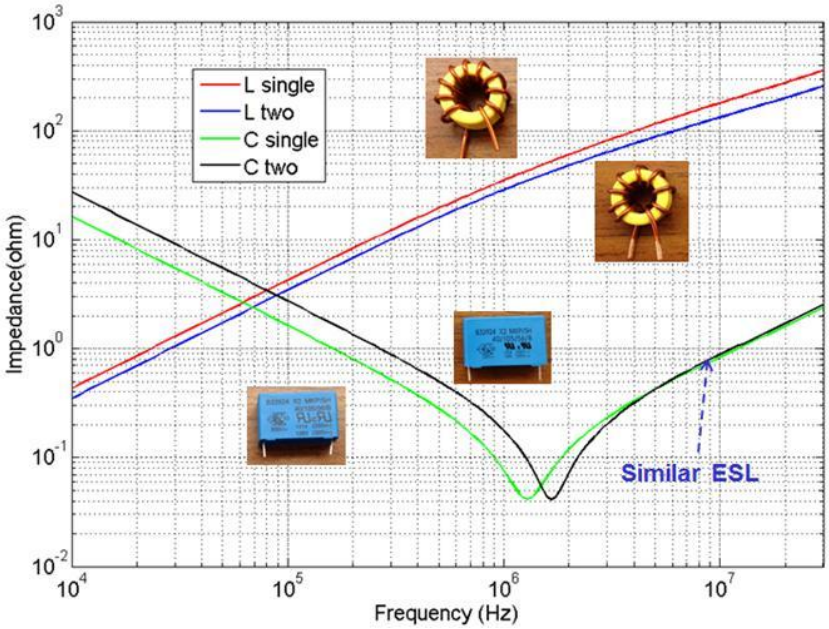


Figure 4-13 Components impedance test

As indicated by Figure 4-9, the single stage EMI Filter has a smaller size when the low frequency attenuation requirement is low. In order to demonstrate the design trade-off between single and multiple stages, another operating point (15dB @150kHz) is selected.

The designed components impedance is shown in Figure 4-13. Figure 4-14 shows the fabricated single stage and two stages EMI filter.

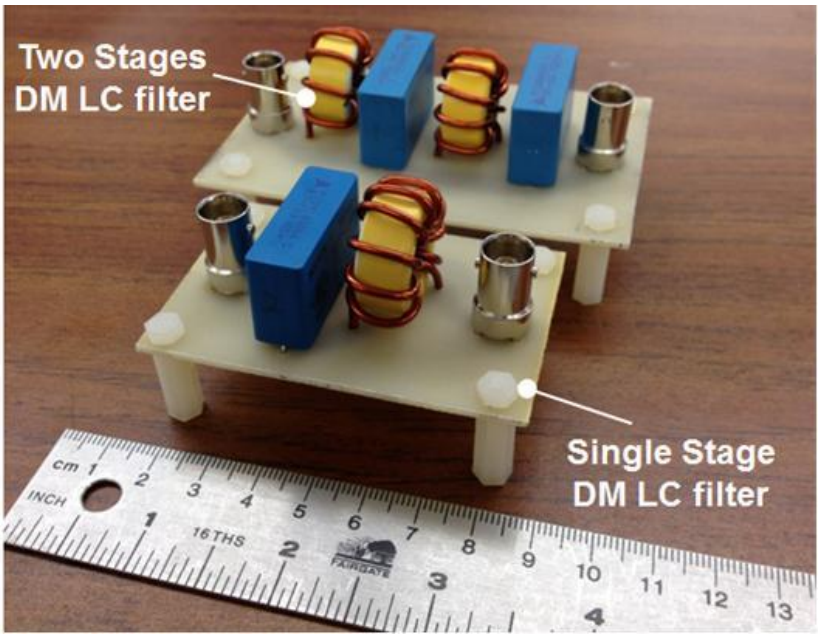


Figure 4-14 Single stage and two stages LC filter

Table 4-3 Comparison result

	C (μF)		L (μH)		Saturation turns		V_{total} (cm^3)	
	Predicted	Real	Predicted	Real	Predicted	Real	Predicted	Real
Single stage	0.8	0.98	7.9	6.63	11	10	9.2	10.23
Two stages	0.5	0.6	5.3	5.4	10	9	13.2	13.4

The detailed comparison between single stage and two stages EMI filter for this case is shown in Table 4-3. As indicated by the designed results, the fabricated single stage EMI filter volume is 10.23 cm^3 and the two stages EMI filter volume is 13.4 cm^3 which is slightly larger than the single stage filter.

Figure 4-15 shows the transfer gain test results comparison between the single stage and two stages DM EMI filter. The attenuation at 150 kHz is around 15dB for both cases. As is similar to the case 1 demonstrated above, the two stage filter has higher attenuation at high frequency because of smaller parasitic.

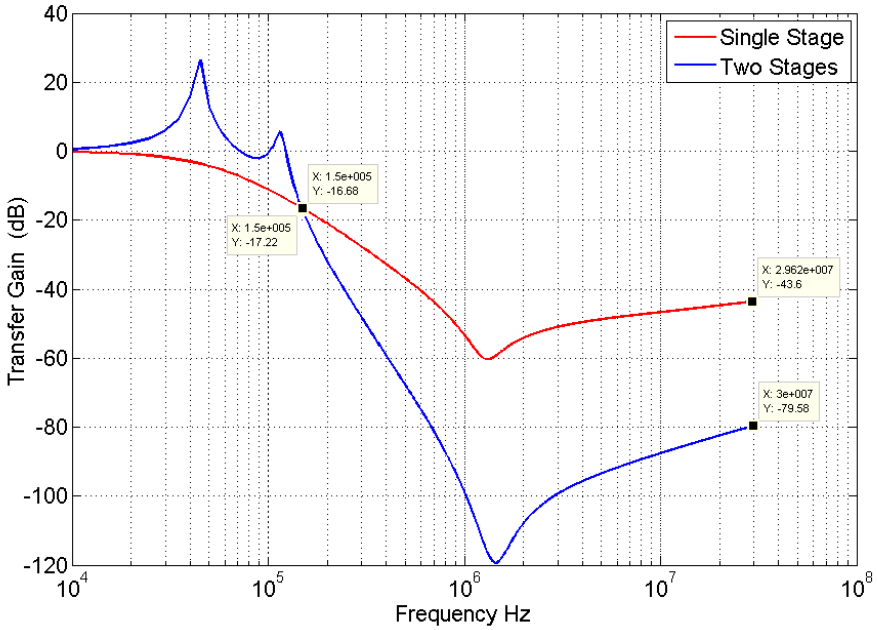


Figure 4-15 Transfer gain test

4.3 EMI in Circuit Noise Attenuation Prediction

The analysis and design approach presented above is based on EMI filter transfer gain. However, the real power converter that contains an EMI filter, cables, LISN and power source is a complex system as shown in Figure 4-16. The EMI noise source and load impedance may not be able to be considered as ideal cases. Resonance and non-linear loop impedance may exist in the system. Meanwhile, the previous lumped model may not be true. The approach proposed in this section belongs to the frequency domain model. Impedances involved in the prediction are measured directly by a precision impedance analyzer offering more precision on characteristics in the frequency range of interest. Moreover, this work clearly establishes a link between small signal measurements and real in-circuit power test. This link allows the designer to improve their EMI filter without proceeding back and forth with the

power converter prototype, an approach that is costly, ineffective and potentially destructive due to multiple manipulations.

4.3.1 Frequency domain equivalent circuit

In order to deal with this level of complexity, it is wise to divide this system into multiple smaller entities. Proceeding this way allows the study of each entity characteristics individually. As shown in Figure 4-16, it contains four components; namely, the load impedance (Z_L), the filter impedance, the noise source (V_{noise}) and the source impedance (Z_s). The basic assumption here is that the noise source is only determined by the operating point and will not change for different filter structures. All these components are treated separately in the following subsections.

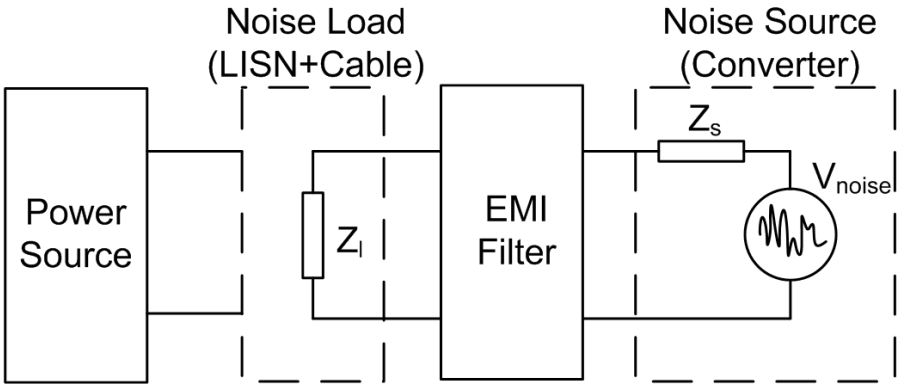


Figure 4-16 Equivalent circuit to predict EMI filter insertion gain for both DM and CM

4.3.2 EMI noise measurement (V_{noise})

As mentioned above, the noise source will stay the same for different filter structures. Therefore, the EMI noise in-circuit attenuation can be calculated by the EMI noise measurement results. In order to validate the proposed approach, common mode and differential mode noises must be measured. Common mode measurement is obtained by clamping the current probe on the three power leads as depicted by Figure 4-17 (a).

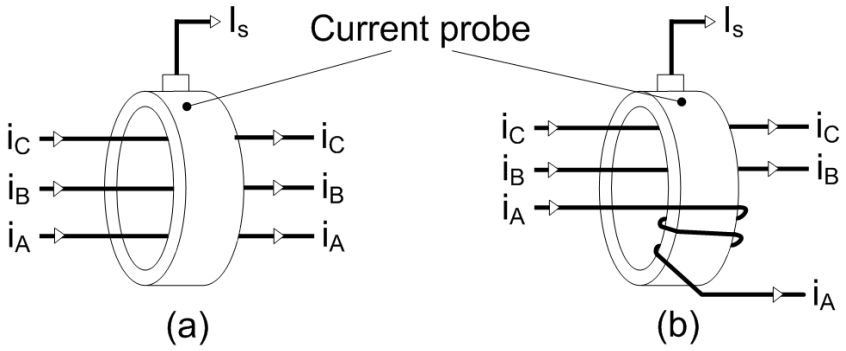


Figure 4-17 (a) Common mode noise measurement setup. (b) Differential mode noise measurement setup.

With the assumption of a balanced three wires system, differential currents cancel out and the sum of the common mode currents flowing in the three wires. By assuming balanced common mode impedances, it is therefore possible to divide the obtained spectrum by three to obtain the common mode current flowing in one wire. It's more complex to obtain the differential mode noise because the measurement is sensitive to the common mode as well. For a balanced system, the approach shown in Figure 4-17 (b) can be used. Two wires pass through the current probe directly and the third one is twisted in the opposite direction using two turns rather than only one. The purpose of this configuration is to cancel the common mode while keeping the differential mode. The collected current by the probe (Is) is given by (4-10)

$$I_s = -2i_A + i_B + i_C \tag{4-10}$$

Where $i_A = i_{Acm} + i_{Adm}$, $i_B = i_{Bcm} + i_{Bdm}$ and $i_C = i_{Ccm} + i_{Cdm}$

If common mode impedances are perfectly balanced and the common mode current in all the wires are equal, the common mode terms in equation (4-10) cancel and only the differential mode terms remain leading to equation (4-11).

$$I_s = -2i_{Adm} + i_{Bdm} + i_{Cdm} \tag{4-11}$$

In the differential mode, the sum of the currents flowing in the three-phase system must be equal to zero for a balanced system. Solving for i_{Cdm} yields to

$$i_{Adm} + i_{Bdm} + i_{Cdm} = 0 \quad \Rightarrow \; i_{Cdm} = -i_{Adm} - i_{Bdm} \tag{4-12}$$

Substituting i_{Cdm} in (4-11) will lead to (4-13)

$$I_s = -3i_{Adm} \tag{4-13}$$

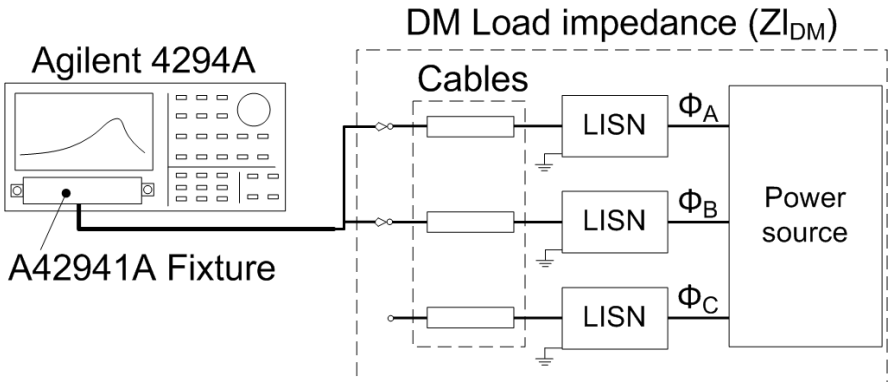


Figure 4-18 DM load impedance measurement including the cables, the LISN and the power source.

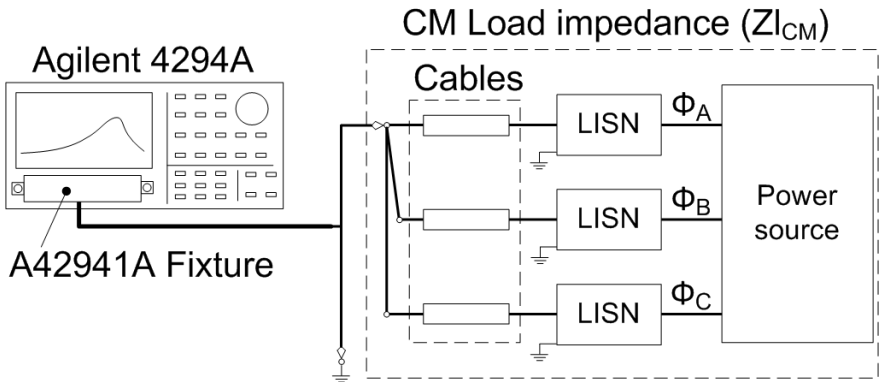


Figure 4-19 CM load impedance measurement including the cables, the LISN and the power source.

Load impedance (Z_L) includes LISN, cables and the power source. Both Z_{LCM} and Z_{LDM} can be directly measured using a precision impedance analyzer. The DM impedance measurement schematic is shown in Figure 4-18. For this measurement, one terminal of the impedance analyzer is connected to one cable and the other terminal is connected to a second power cable. The CM impedance measurement is shown in Figure 4-19. One terminal of the impedance analyzer is connected to the ground close to the converter. The second terminal is connected to the joint point of

the power cables to measure the average common mode impedance. Using these setups, impedance is obtained by sweeping over the frequency range of interest. Both magnitude and phase must be recorded for CM and DM.

Generally, impedance of the EMI filter cannot be measured directly because some components of the filter are in parallel with the load. This is particularity well illustrated in Figure 4-20 for the second order differential mode L-C filter inserted between the Vienna bridge (left side of Figure 4-20) and the load (right side of Figure 4-20). The situation is not different in CM as shown in Figure 4-21. Once again, the filter capacitors ($C_{F,CM}$) are in parallel with the load. To deal with this particularity in both cases, the component impedance is measured individually over the frequency range of interest. The electrical and magnetic coupling for these components is not considered.

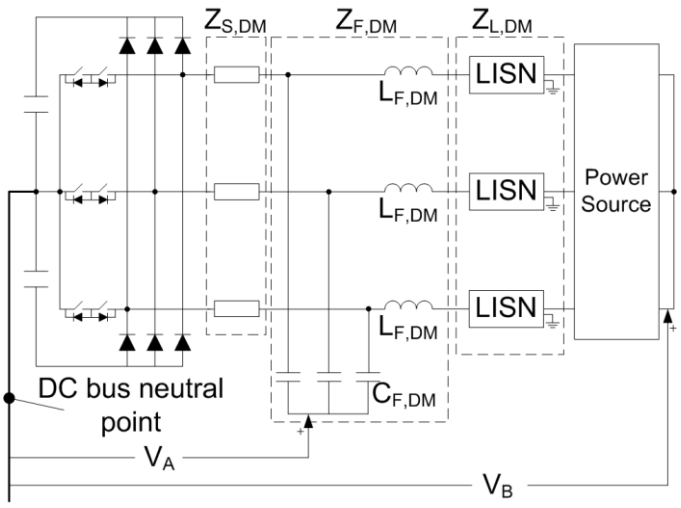


Figure 4-20 L-C DM filter configuration

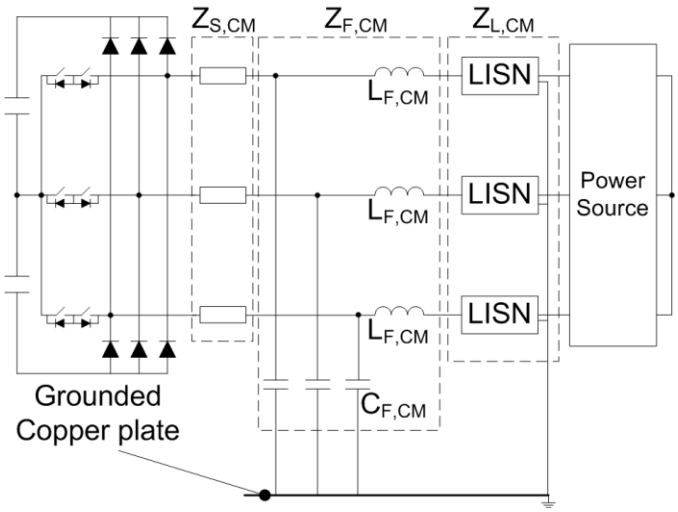


Figure 4-21 L-C CM filter configuration

Besides the load and EMI filter impedance, the EMI source impedance is the last unknown that needs to be characterized for predicting the insertion gain. As discussed above, power converters are time-varying non-linear systems, source impedance has been measured in [153, 154] using a vector spectrum analyzer with certain linearization assumption. These source impedances are plotted in frequency domain. However, after checking the previous literatures, some physical meanings can be interpreted from the plotted source impedance. The analysis contained in the next two sections brings some answers to this fundamental issue for the source impedance.

4.3.3 Source Impedance Analysis

As discussed above, power converters are time-varying non-linear systems. However, each power semiconductor switching reconfigures the converter in a new state, which is time-invariable until the next change. This means that for every switch combination, the system is divided into several subintervals, which are time-invariable linear systems. Since the targeted application of this work is a three-phase PFC boost converter, this analysis will be conducted for a boost-type converter only for the sake of simplicity. The buck-type converter can also be analyzed in the similar way.

A phase-leg in boost configuration is shown in Figure 4-22.

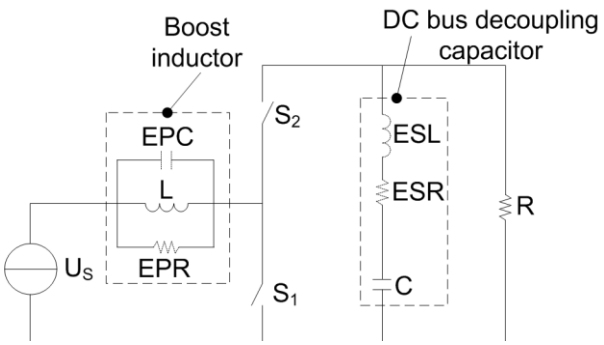


Figure 4-22 Boost converter equivalent circuit

The circuit includes two switches (S1 and S2), the boost inductors (L) with its parasitic (EPC and EPR), the resistive load (R) and the DC bus bulk capacitor (C) with its corresponding parasitic (ESL and ESR). Using the assumption that the converter works in Continuous Current Mode (CCM), which covers a lot of PFC applications, the circuit can be divided into two subintervals. The first subinterval, depicted in Figure 4-23, appears when S1 is ON and S2 is OFF. The second subinterval, shown in Figure 4-24, takes place when S1 is OFF and S2 is ON. For each subinterval, relevant parasitic components are shown in corresponding pictures. Further subdivision of the circuit is required to perform the study about the time unvarying part of the circuit: the internal and external impedances. In boost configuration, the external impedance is the boost inductor with its parasitic. The internal DM impedance includes the intrinsic converter parasitic (semiconductors parasitic capacitances and bulk cap ESL and ESR) as well as the bulk cap itself together with the load impedance. The equivalent internal impedance ($Z_{eq1,\,DM}$) for the first subinterval shown in Figure 4-23 is given by (4-14).

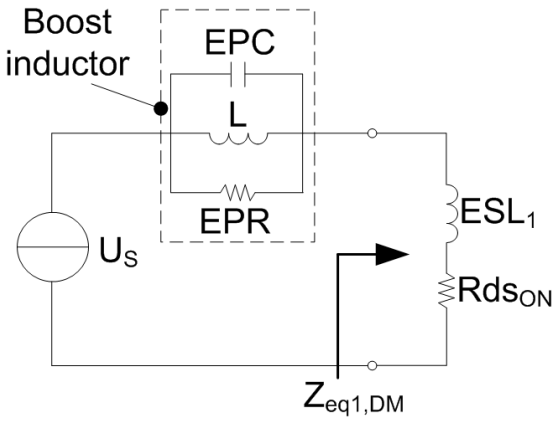


Figure 4-23 Turn on switch S1 subinterval.

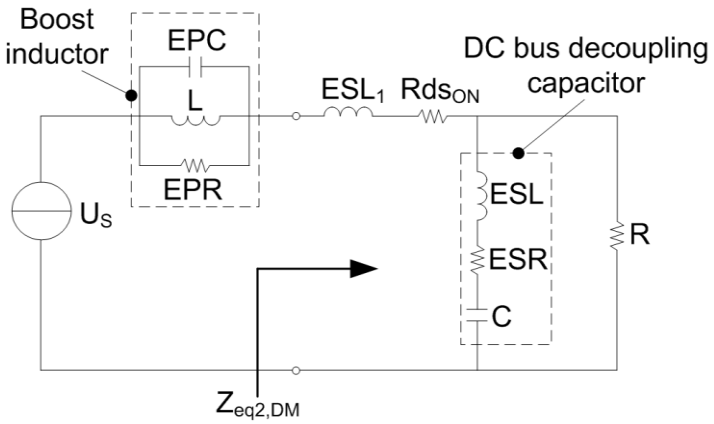


Figure 4-24 Turn on switch S2 subinterval.

$$Z_{eq1,DM} = Z_{ESL1} + Rds_{ON} \tag{4-14}$$

The equivalent impedance ($Z_{eq2,\,DM}$) for the second subinterval shown in Figure 4-24 is given by relation (4-15)

$$Z_{eq2,DM} = Z_{ESL1} + Rds_{ON} + (Z_{ESL} + Z_{ESR} + Z_C) \parallel R \tag{4-15}$$

Finally, the boost inductor impedance including the self-parasitic is given by (4-16)

$$Z_{Lboost} = \frac{Z_R Z_L Z_C}{Z_C (Z_R + Z_L) + Z_R Z_L} \tag{4-16}$$

In (4-15), one observes the presence of the load resistance (R). Basically, this value is not known and can change with different operating point. However, a fundamental observation is done by studying the rightmost term $(Z_{ESL} + Z_{ESR} + Z_C) \parallel R$ in equation

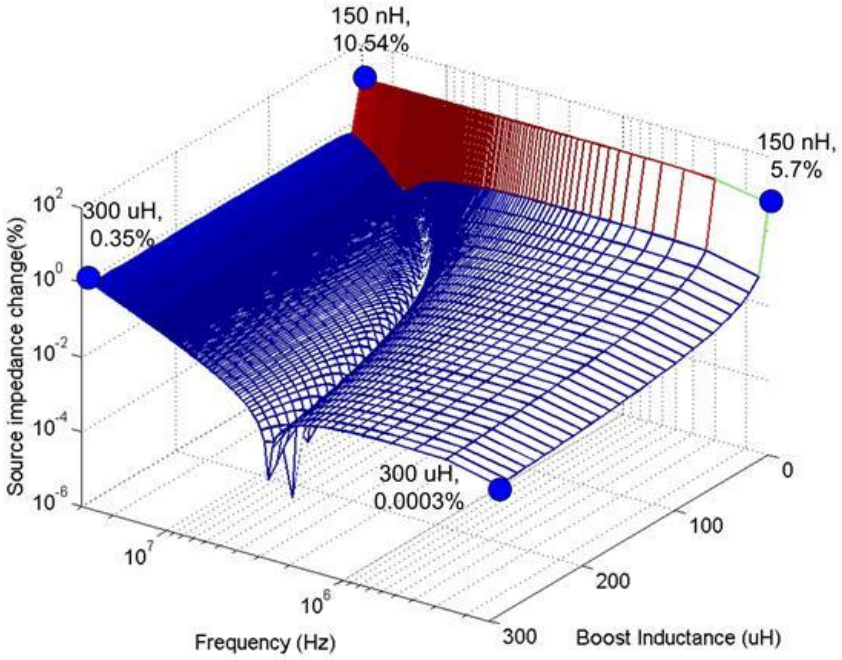
(4-15). This term shows that the bulk DC caps with its parasitic are in parallel with the load resistance. Therefore, by using good decoupling practice (i.e. film or ceramic capacitors with smaller parasitic), it is possible to keep the DC cap impedance very low 'screening' the load impedance in the frequency range of interest. In this case, the rightmost term in equation (4-15) disappears leading to equivalent impedances for subintervals 1 and 2 equal to each other. If the circuit decoupling is relatively poor, some changes in source impedance can be observed between the two subintervals. It becomes worthwhile to compare the internal impedance of each subinterval with the external impedance. The external impedance can be boost inductor or other type of impedance. For the analysis in this section, the boost inductor is selected as the external impedance. Since internal and external impedance are in series, it is important to determine which one is dominant. The impedance variability with external mask impedance is shown in equation (4-17).

It is obvious that stronger external impedance leads to a smaller variability of the different subintervals impedances. This external impedance can be utilized as mask impedance for the source impedance linearization.

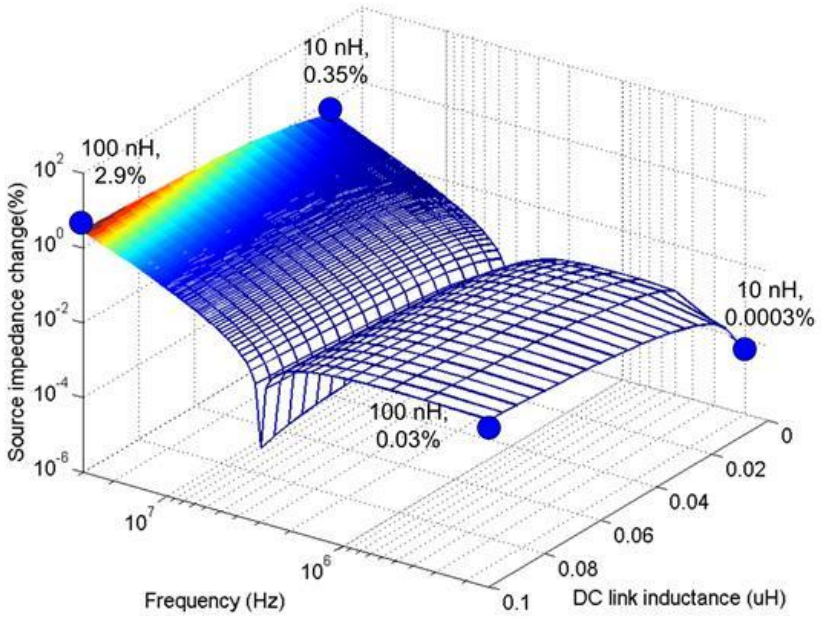
$$|\Delta Z_{s\_dm}| = 1 - \left| \frac{1 + \frac{Z_{eq1,DM}}{Z_{Lboost}}}{1 + \frac{Z_{eq2,DM}}{Z_{Lboost}}} \right| \tag{4-17}$$

The relevant parameters are listed in Table 4-4. Figure 4-25 (a) shows the external boost inductance influence on the source impedance variability considering a DC capacitor equivalent series inductance of 10nH. This graph is plotted for different subintervals using equation (4-17). The mask impedance (boost inductor) influence on reducing the source impedance variability can be obviously observed. However, even with a 150nH boost inductance, the source impedance variability can still be

controlled less than 11% for 30 MHz and 6% for 150 kHz. The valley in the curve corresponds to the self resonant of the boost inductor.



(a) Different boost inductance (L)



(b) Different dc link inductance (ESL).

Figure 4-25 DM impedance variability

Figure 4-25 (b) shows the DM source impedance variability with different DC capacitor equivalent series inductance (ESL). This graph is plotted using a 300μH boost inductance. As expected, the increased DC link inductance will increase the source impedance variability. However, in this specific case, the variation of the total impedance can still be controlled less than 3%.

Table 4-4 Parameters used for the impedance variability study

Components	Values	Components	Values
L	150nH~300μH	EPC	20pF
ESL	10nH~100nH	ESR	10mΩ
ESL1	10nH	Rdson	10 mΩ
EPR	10kΩ	Chg	200pF
C	100μF	C1	50pF
R	42Ω	C2	450pF

Many parasitic are relevant in both CM and DM. However, some of them are specific to CM.

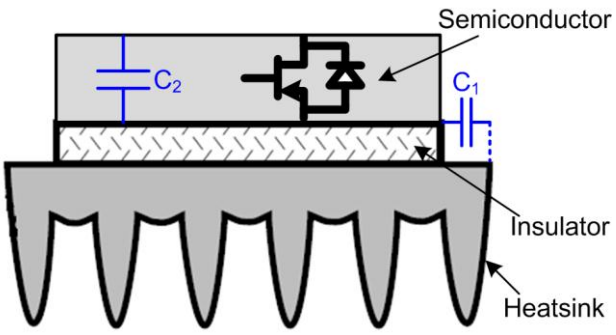


Figure 4-26 Semiconductor device parasitic model

A typical semiconductor device parasitic model is shown in Figure 4-26 as an example. The device is usually mounted on top of the heatsink or cold plate with an insulation layer. Stray capacitance between the device bottom layer and the heatsink is denoted as C_1. C_2 stands for the junction cap inside the semiconductor devices. Boost converter common mode equivalent circuit with the relevant parasitic is shown

in Figure 4-27. Beside the parameters shown in Figure 4-26, C_{hg} represents the stray capacitor between the heatsink and the ground.

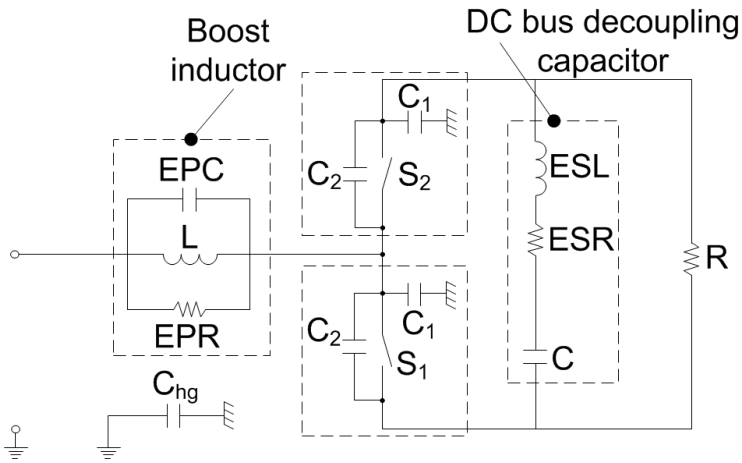


Figure 4-27 Boost converter CM equivalent circuit.

Since the impedance of device ON resistance is much smaller than the impedance of stray capacitance, the equivalent circuit for the switch S_1 turn on subinterval can be simplified as in Figure 4-28. Figure 4-29 shows the equivalent circuit of the turn on switch S_2 subinterval. Once again, the bulk DC capacitor with its parasitic is in parallel with the load resistance. Similar to the differential mode case analysis, good DC link decoupling plays an important role in the simplification of the subinterval, which is shown in Figure 4-28. If DC bus decoupling is well achieved, impedance of the DC bus bulk capacitor is much smaller than the load impedance. In this case, the bulk DC bus capacitor becomes in series with capacitor C_1. The impedance of C_1 is much higher than the bulk capacitor (C) and the latter impedance can be ignored. This branch impedance is then estimated to the impedance of C_1 only. Applying this simplification leads to the circuit shown in Figure 4-29 which is the subinterval when S_2 is activated. From these observations, it is obvious that impedance variability is very weak in common mode if the DC bus decoupling is well achieved.

The impedance of the first subinterval ($Z_{eq1,CM}$) (i.e. when S1 is closed and S2 is open) is given by

$$Z_{eq1,CM} = [((Z_{ESL} + Z_{ESR} + Z_C) \| R) \| Z_{C2} + Z_{C1}] \| Z_{C1} + Z_{Chg} \tag{4-18}$$

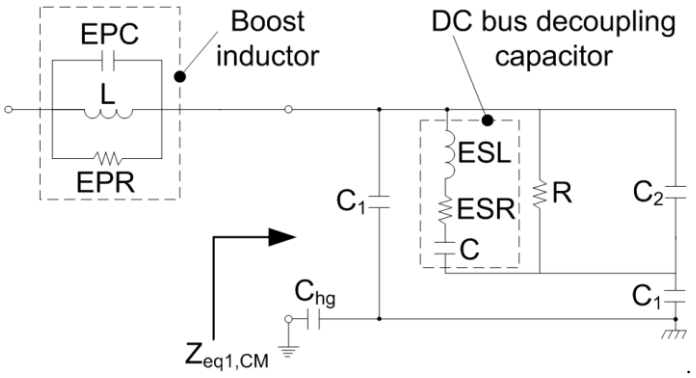


Figure 4-28 CM equivalent circuit for subinterval S1.

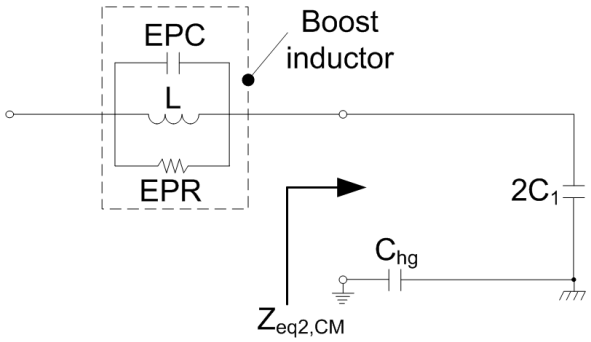


Figure 4-29 CM equivalent circuit for subinterval S2.

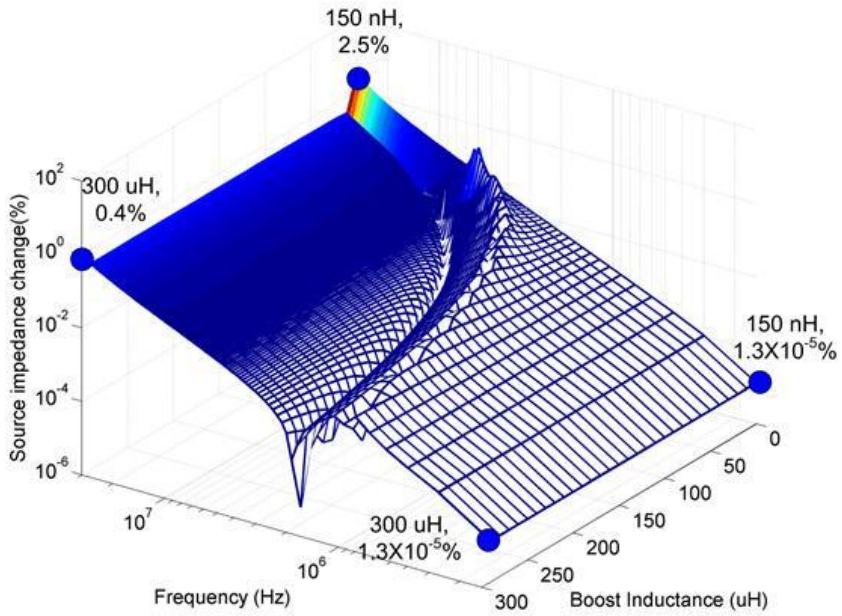
The impedance of the second subinterval ($Z_{eq2,CM}$) (i.e. when S1 is open and S2 is close) is given by

$$Z_{eq2,CM} = \frac{Z_{C1}}{2} + Z_{Chg} \tag{4-19}$$

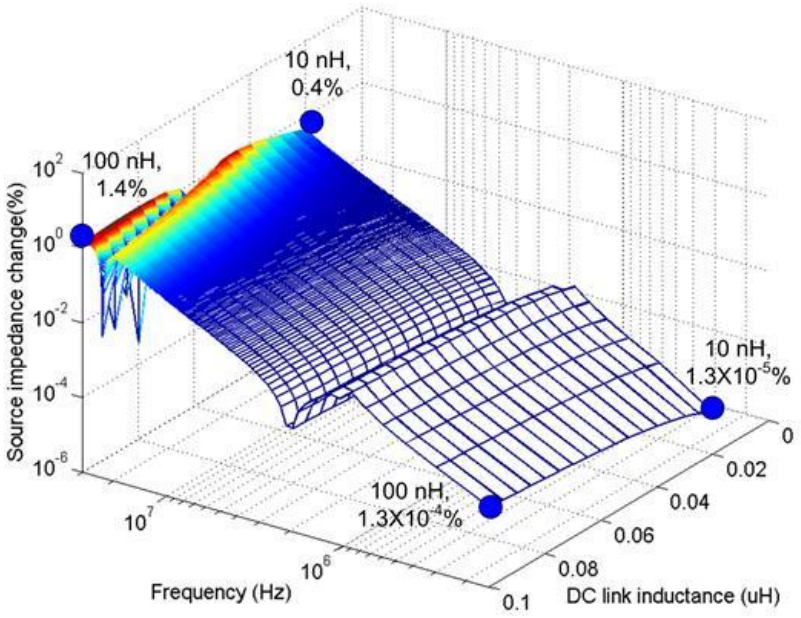
The boost inductance impedance is still given by equation (4-16). Once again, if the decoupling is poor, it becomes very useful to study the variability of the total source impedance depending on both subintervals. Equation (4-20) allows this quantification. Relevant parameters are also listed in Table 4-4.

$$|\Delta Z_{s\_cm}| = 1 - \left| \frac{1 + \frac{Z_{eq1,CM}}{Z_{Lboost}}}{1 + \frac{Z_{eq2,CM}}{Z_{Lboost}}} \right| \tag{4-20}$$

Figure 4-30 (a) shows the CM source impedance variability with different boost inductances (L) and a DC bus equivalent series inductance of 10nH. Because stray capacitances C_1 and C_{hg} are very small, they already play an important role to mask the change of the source impedance for different subintervals especially at low frequency. This explains why the boost inductance L doesn't have too much improvement in reducing the source impedance variability. Figure 4-30 (b) shows the DC bus equivalent series inductance influence to the source impedance variability with a 300μH boost inductance. When the DC bus parasitic increases, the variability of the CM source impedance also increases. However, as mentioned above, because of the stray capacitance, the variability is still very small.



(a) Different boost inductance (L)



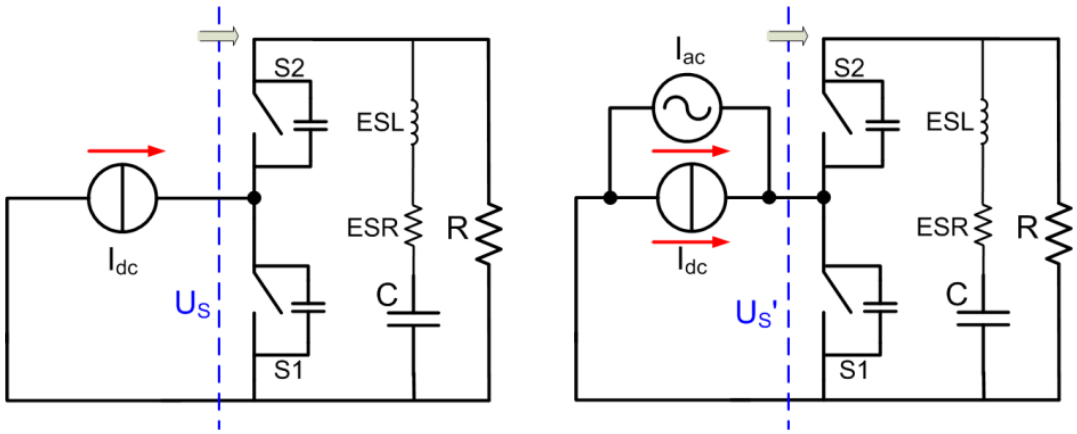
(b) different dc link inductance (ESL).

Figure 4-30 CM source impedance variability

Besides the different subintervals with different switch combinations, the transient impedance between different subintervals also influences the source impedance. Based on the analysis above, because the stray capacitance C_1 is very small, the converter CM source impedance is dominated by the stray capacitance C_1 and outside non-change impedance which is not sensitive to the switch impedance. So, the transient impedance analysis is conducted only for differential mode. Since the noise source transient impedance can't be directly measured, the transient impedance influence on the source impedance is analyzed indirectly. Different transient conditions are implemented to demonstrate its influence to total source impedance. To analyze the source impedance when the converter is running, describing function method is adopted in this section as linearization tools which is similar to [155] .

Figure 4-31 shows the equivalent circuit for a boost converter. The relevant parameters stay the same with Table 4-4. In order to get rid of the influence from

external impedance, ideal current source is utilized to replace the input inductor and also represent the CCM condition. Figure 4-31(b) has exactly the same circuit and parameters compared with (a) except a small ac excitation added to the input. The excitation current must be very small to prevent changing the operating point. The terminal voltage is sensed as the response signal. In the simulation environment, the source impedance is derived based on the measurement of the excitation signal and the response signal. Then, different transient conditions such as different switching speed are implemented to analyze its influence on the source impedance.



(a).With constant input current **(b).Add small ac excitation to the input**

Figure 4-31 Equivalent circuit for boost converter

Equation (4-21) shows the calculation for the source impedance. After the simulation, the terminal voltage spectrum with and without input ac excitation are extracted. By subtraction of the two terminal voltage spectrums, only the part response to the excitation can be obtained. Then, the response part is divided by the excitation signal to get the corresponding source impedance with certain frequency. After sweeping the frequency of the excitation signal, the corresponding source impedance can be obtained.

$$Z_s(f) = \frac{U_s'(f) - U_s(f)}{I_{ac}(f)} \tag{4-21}$$

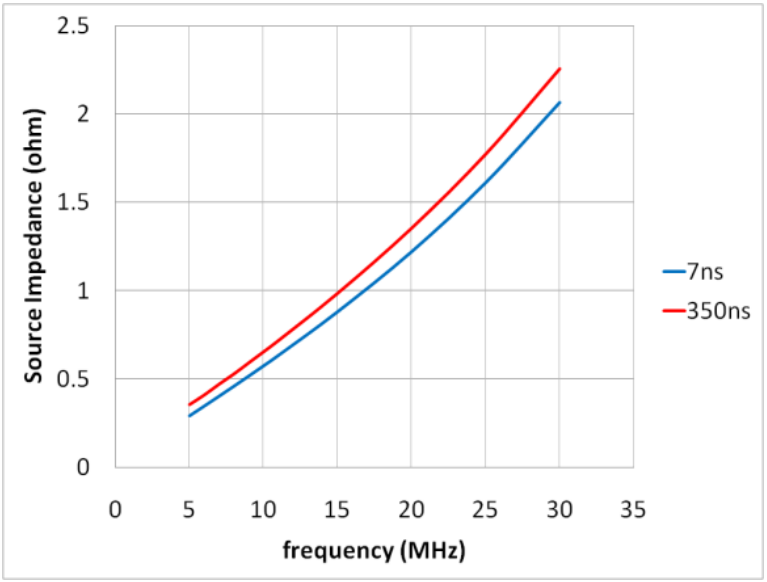


Figure 4-32 Switching slope influence to the source impedance (fs=100kHz)

Figure 4-32 shows the influence of changing switching time (7 ns to 350 ns) to the source impedance with a fixed switching frequency of 100 kHz and 0.5 duty cycle. With a higher excitation frequency, the source impedance becomes higher. This observed curve shape can be explained by the steady state subinterval circuit analyzed above. The stray inductors existed in both subintervals make the source impedance increasing with the spectrum frequency. Meanwhile, the slower switching speed lead to higher total source impedance.

Figure 4-33 shows the switching speed influence on the source impedance with different switching frequencies. The higher switching frequency leads to higher source impedance. The influence of the transient part becomes more obvious when the switching frequency is higher and the switching speed is lower.

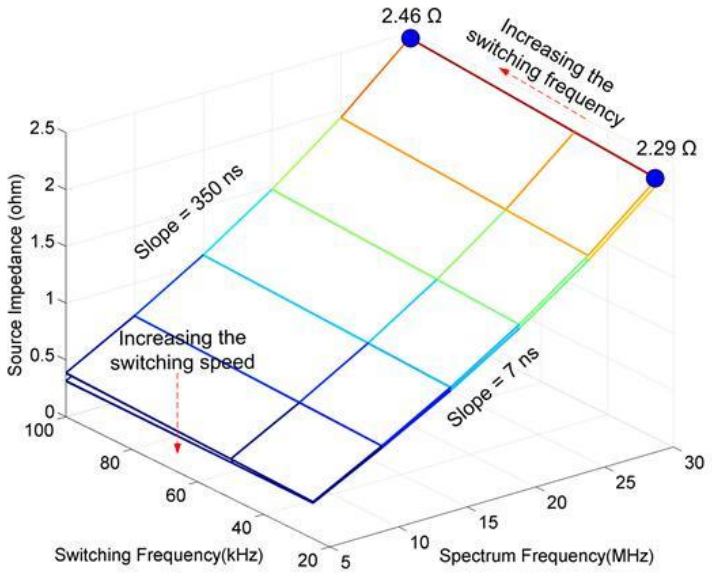


Figure 4-33 Switching slope influence to the source impedance with different switching frequency

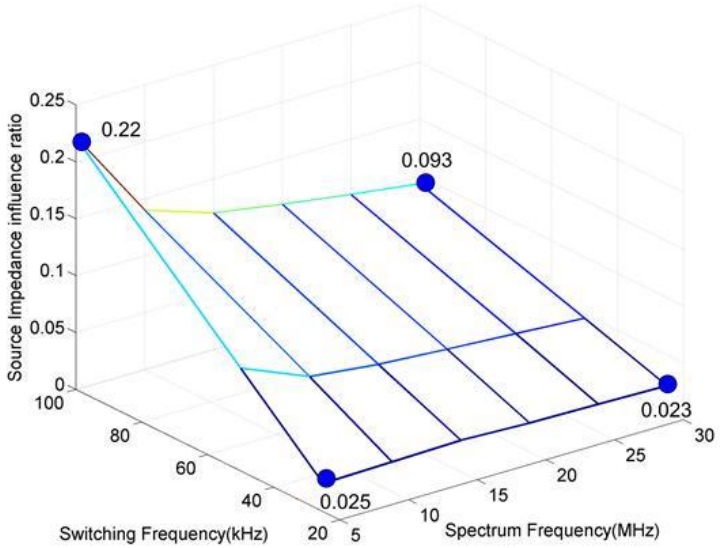


Figure 4-34 Switching slope influence to the source impedance with different switching frequency

Figure 4-34 shows the switching speed influence on the source impedance from a ratio point of view with different switching frequencies. As indicated by Figure 4-33, the highest source impedance corresponds to the higher spectrum frequency and higher switching frequency. Figure 4-34 shows that the source impedance only changes to around 10% by decreasing the switching speed from 7ns to 350ns at

30MHz spectrum frequency and 100 kHz switching frequency. This means the source impedance stays pretty stable even with a large range changing of the switching speed and switching frequency.

Based on the analysis of this chapter, the CM source impedance will stay relatively stable even without the external mask impedance and the DM source impedance variability can be controlled within a small value with an external mask impedance, such as the boost inductor. Meanwhile, a good DC link decoupling is necessary to reduce the variability of the source impedance. With these considerations, the non-linear source impedance characteristics can be approximately linearized. Then, the linearized source impedance can be used in the equivalent circuit as shown in Figure 4-16 to predict the EMI noise attenuation.

4.3.4 CM and DM insertion loss prediction

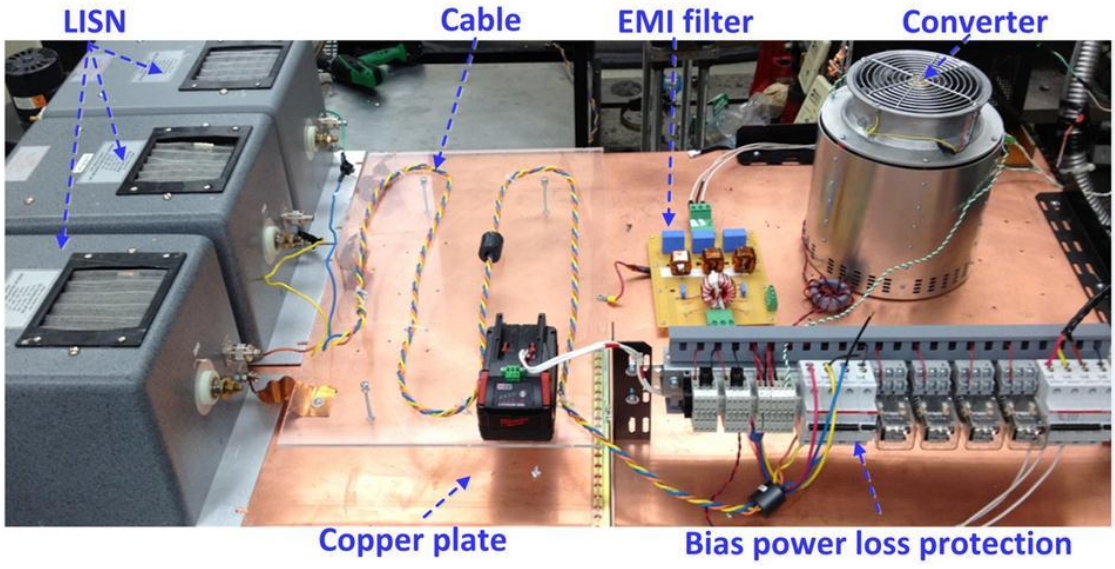
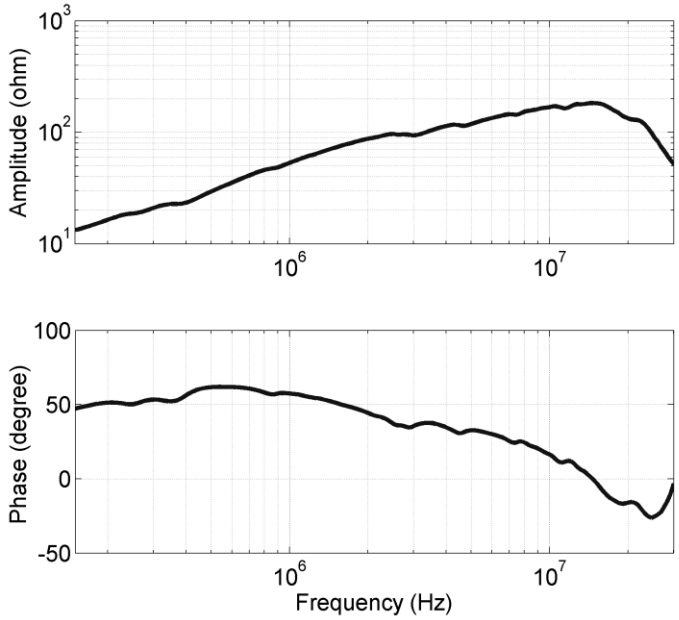


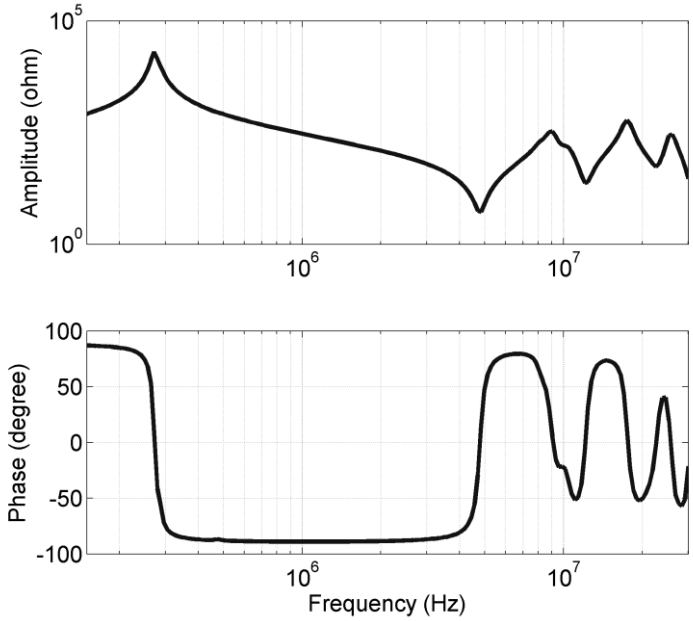
Figure 4-35 Experimental test setup.

With the analysis above, this section presents the experimental results obtained for insertion gain prediction. A Vienna type converter is utilized as an example. The

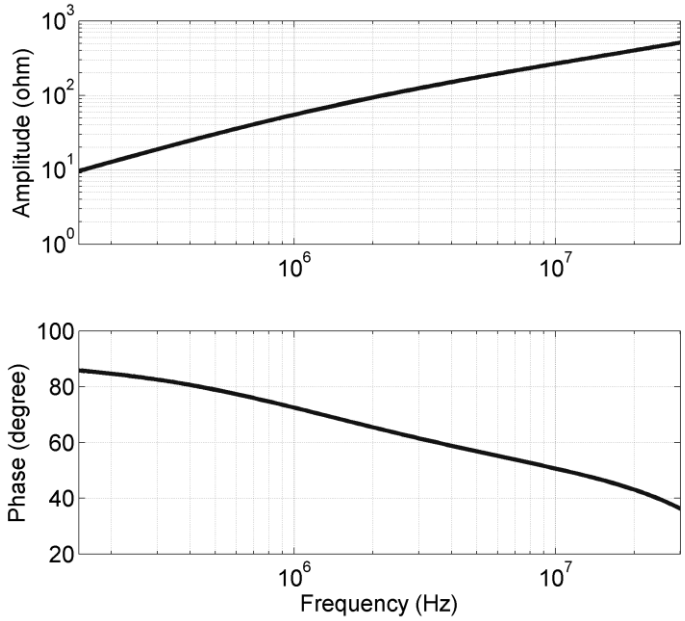
experimental setup is shown in Figure 4-35. Besides the LISN, cable, EMI filter and converter, the whole setup is on top of a grounded copper plate, as required by EMI standards. Normally on SiC JFETs are utilized as the main switches for the converter, thus, a bias power loss protection is also designed. The impedances included in the equivalent circuit from Figure 4-16 are measured first.



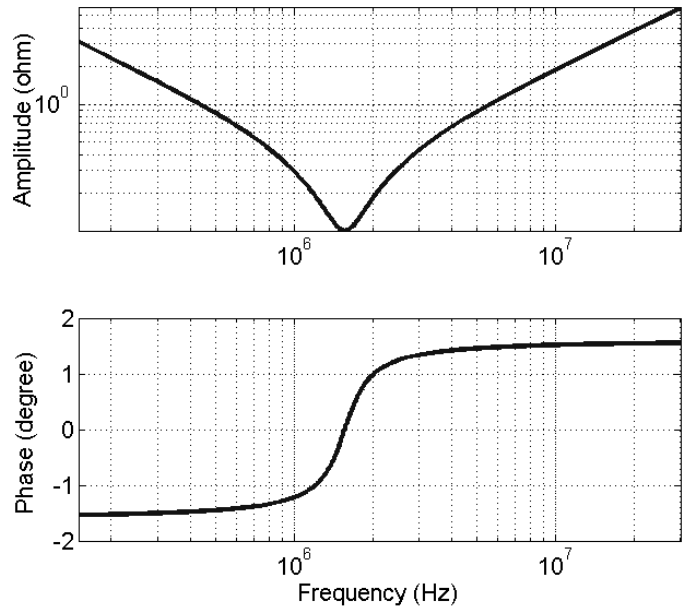
(a) DM load impedance Z_{lDM}.



(b) DM source impedance Z_{SDM}.



(c) DM filter inductance impedance $Z_{fL,DM}$.



(d) DM filter capacitance impedance $Z_{fC,DM}$.

Figure 4-36 DM impedance measurement

Figure 4-36 shows the relevant DM impedance measurement results. Figure 4-36 (a) is the measured load impedance using the setup shown in Figure 4-18. With the similar measurement setup, the source impedance including boost inductor is shown

in Figure 4-36 (b). Below 4.8 MHz, the boost inductor in parallel with its EPC can be clearly observed. Over 4.8 MHz, the impedance curve change in a very complex way which cannot be represented by lumped RLC model and using direct measurement in this case is very useful. The second order LC filter structure is shown in Figure 4-20. As mentioned before, component impedance in the filter must be measured individually. The impedance for the DM filter inductor is shown in Figure 4-36 (c). As expected, the behavior of the inductor changes with frequency. This is especially true for the phase which is decreasing slowly in Figure 4-36 (c) as frequency increases. This behavior is difficult to predict and direct measurement becomes essential. Figure 4-36 (d) shows the impedance of the DM filter capacitance.

With the measured relevant impedance in both amplitude and also phase, the insertion gain can be calculated using equation (4-22). Insertion gain prediction result is shown in Figure 4-37 for the second order LC filter shown in Figure 4-20. The bare noise is in blue color and the attenuated noise after LC filter is in green color. The predicted attenuation with (4-22) is in red and the experimental insertion gain, which is the differential between the blue and the green ones, is shown in black color. In spite of very small differences at high frequency, a very good agreement between the predicted insertion gain and the experimental one can be observed on Figure 4-37. Also, special attention must be paid to the complex noise profile at high frequency. By comparing Figure 4-37 and Figure 4-36, some relationship between the noise profile and the source impedance can be observed. It is obvious that this relation is complex but, by using direct measurements as suggested, it is able to handle with this level of difficulty.

$$IG = \frac{1 - \dfrac{Z_{sDM}}{Z_{sDM} + (Z_{fC\_DM} \parallel (Z_{fL\_DM} + Z_{LDM}))}}{(Z_{fL\_DM} + Z_{LDM})(Z_{LDM} + Z_{sDM})} \qquad (4\text{-}22)$$

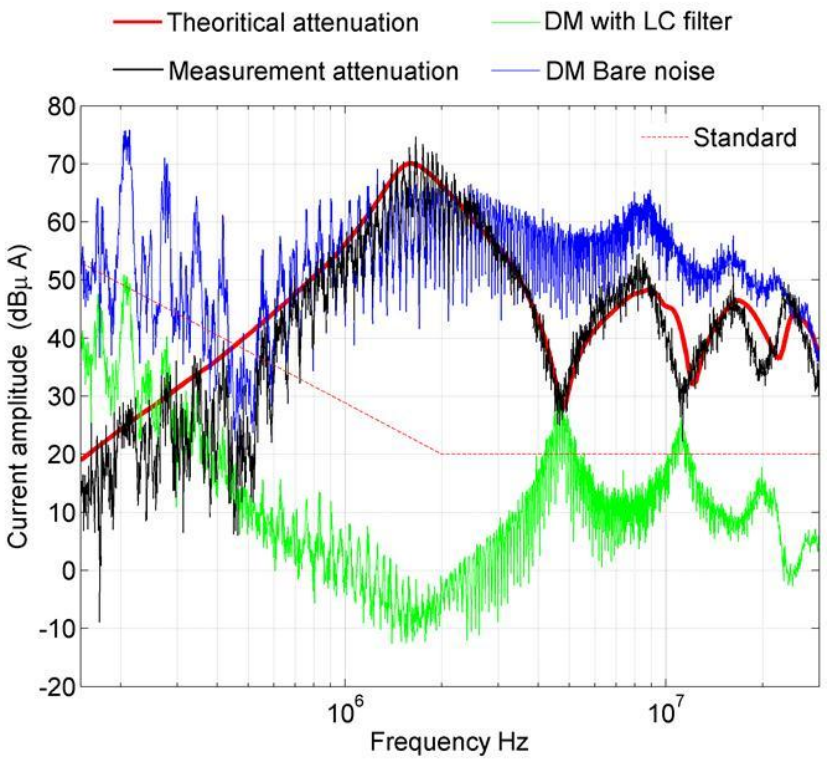


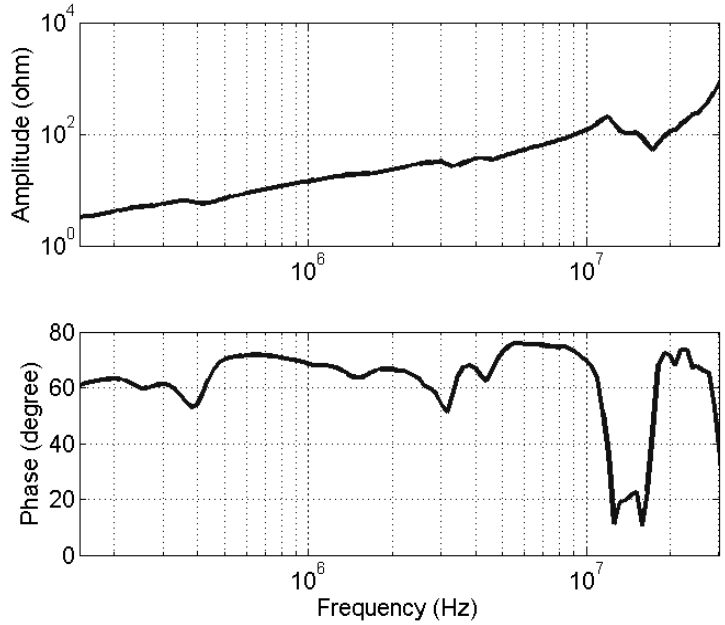
Figure 4-37 DM attenuation with two stages filter

Using the setup shown in Figure 4-19, CM load impedance is shown in Figure 4-38 (a). The CM source impedance with the similar measurement is shown in Figure 4-38 (b). Below 600 kHz, the source impedance is dominated by the stray capacitance and after that the boost inductance can be seen from the measured results. The second order LC filter structure is shown in Figure 4-21. The impedance for the CM filter inductor is shown in Figure 4-38 (c). The CM filter capacitance is shown in Figure 4-38 (d).

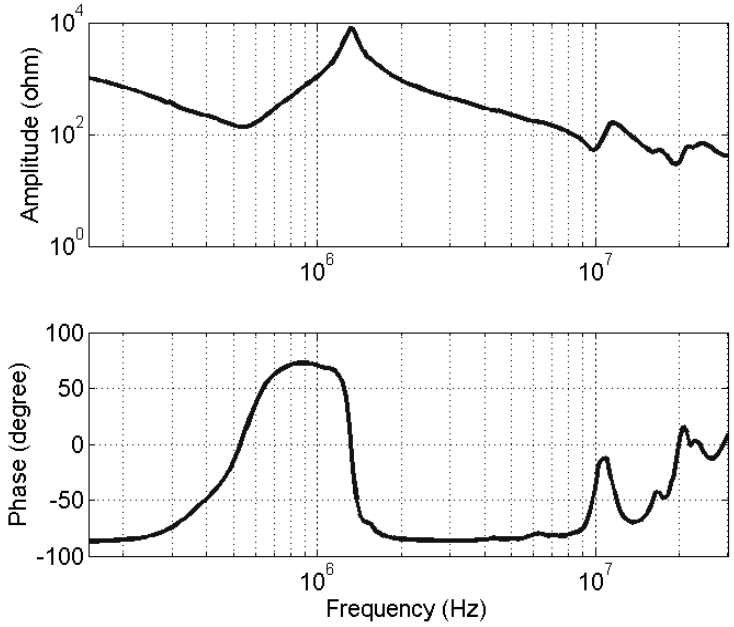
The Insertion gain prediction is shown in Figure 4-39 for the second order LC filter using equation (4-23). The bare noise is in blue and the attenuated noise is in green. The predicted attenuation is in red and the experimental insertion gain, which is the differential between the blue and the green ones, is shown in black. In spite of very

small differences at high frequency, a very good agreement between the predicted insertion gain and the experimental can also be observed.

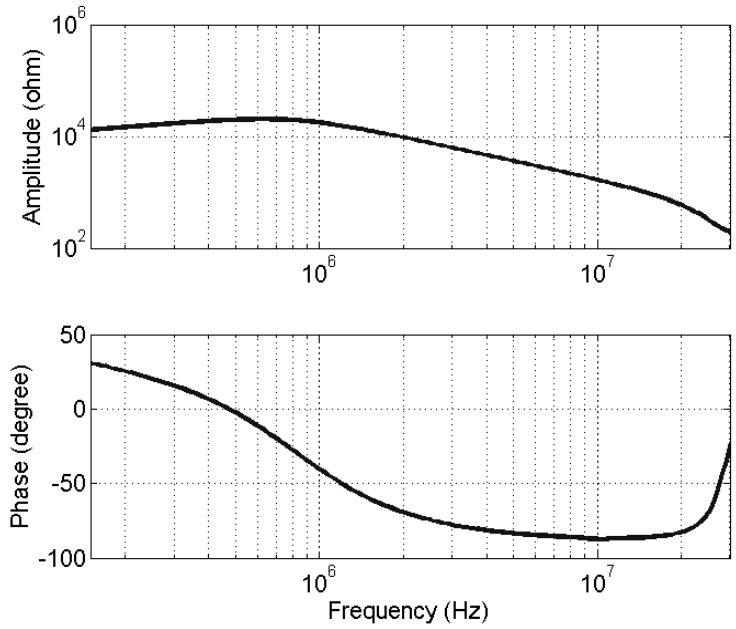
$$IG = \frac{1 - \dfrac{Z_{sCM}}{Z_{sCM} + (Z_{fC\_CM} \parallel (Z_{fL\_CM} + Z_{LCM}))}}{(Z_{fL\_CM} + Z_{LCM})(Z_{LCM} + Z_{sCM})} \tag{4-23}$$



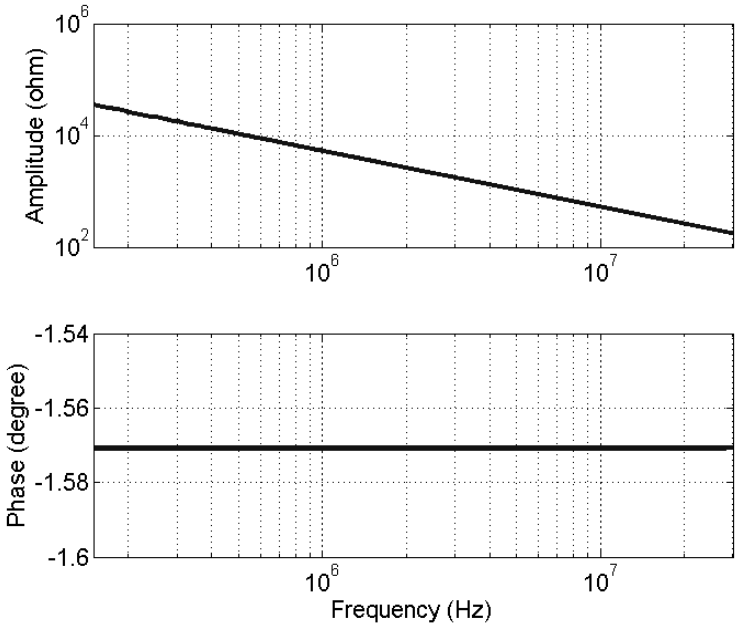
(a) CM load impedance Zl$_{CM}$



(b) CM source impedance Zs$_{CM}$



(c) CM filter inductance impedance $Z_{fL,CM}$



(d) CM filter capacitance impedance $Z_{fC,CM}$

Figure 4-38 CM impedance measurement

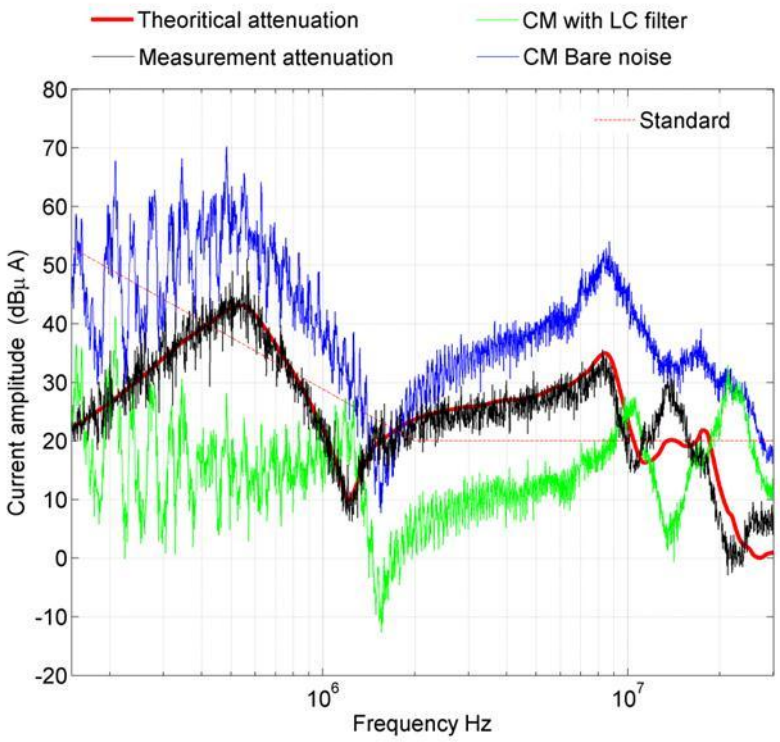


Figure 4-39 CM attenuation with two stages filter

With the successful attenuation prediction shown in this section, EMI filter design can be further improved by better algorithm without back and forth.

4.4 Compact EMI Filter Design with Coupling Consideration

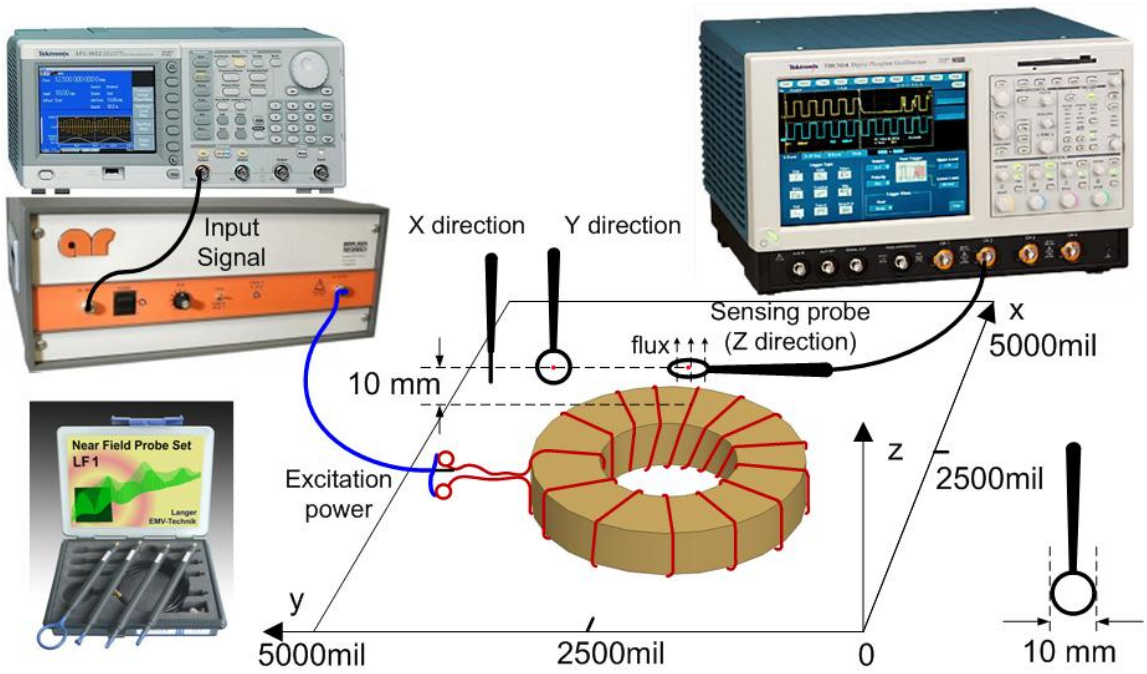
The previous analysis doesn't consider the near-field coupling between components. However, more compact EMI filter design will inevitably decrease the distances between the passive components of the EMI filter and meanwhile affect the filter performance significantly by coupling. The research effort presented in this section focuses on the coupling caused by the near-field stray flux. However, previous literature treats the self-parasitic and mutual parasitic independently. The mutual coupling is also treated statically, which means the coupling flux doesn’t change with different frequencies. The novelty included in this work is about the magnetic components behavior in the high frequency range of the EMI spectrum, which is close

or higher than the magnetic component resonant frequency. In this frequency range, the near-field distribution of the magnetic component will change dramatically when compared with a low frequency condition that has been covered in previous literatures. This is explained by the fact that the current in the winding becomes non-uniform in this frequency range due to the displacement currents, which are caused by the stray capacitors between turn to core and turn to turn. This non-uniform winding current, imposes a new field distribution around the core. In order to avoid performance reduction due to coupling in the filter, care should be given to both the low and high frequencies field distribution. By using the Biot-Savart equation, the high frequency near-field distribution can be well predicted and matched with the experimental results. In addition, a single stage LC DM filter is utilized to demonstrate the influence from the high frequency coupling.

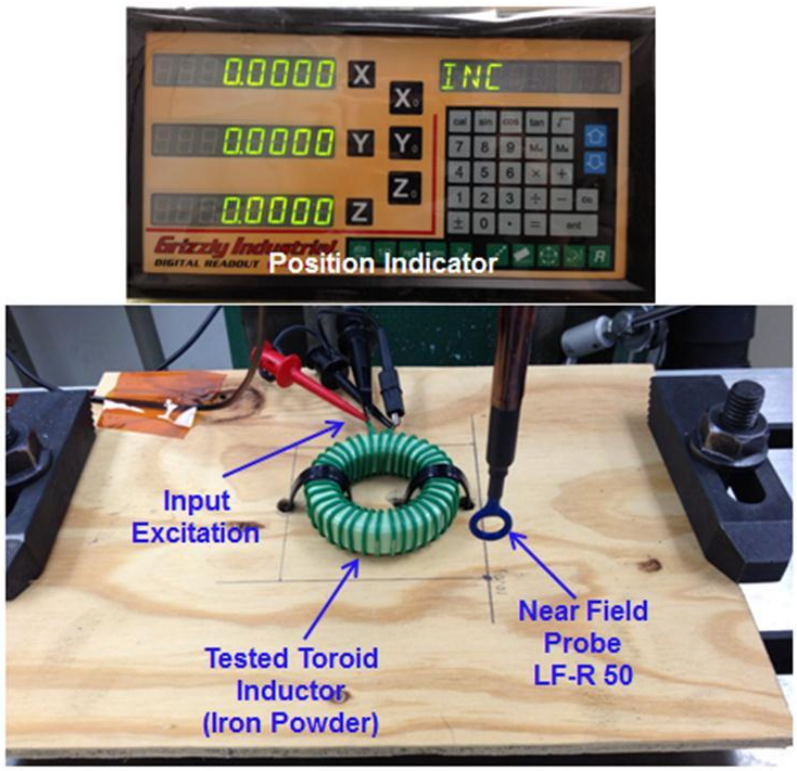
4.4.1 Near-field measurement and analysis

In order to visually display the magnetic components near-field flux distribution, magnetic near-field stray flux measurement setup is utilized and its schematic is shown in Figure 4-40 (a). The power excitation is composed of a Tektronix AFG3102 waveform generator and a 25W power amplifier. The excitation frequency can sweep from 10 kHz to 100 MHz. Besides the power excitation equipment and the magnetic component, near-field probes (LANGER EMV-Technik series) and Tektronix TDS 7054 scope are utilized to monitor the flux around the magnetic components. The magnetic component is placed and fixed on a XY table. The near-field probe LF-R 50 with a 10 mm diameter is utilized to monitor the flux magnitude in direction of both X, Y and Z. As shown in Figure 4-40 (b), the near-field probe is fixed and the XY table is moving and the accurate position is monitored by the position sensor. The middle point of the probe sensing coil is 10mm above the magnetic core top surface.

100 (10 by 10) points are measured to plot the flux distribution for different directions.



(a) Near-field measurement setup schematic



(b) Near-field measurement setup bed

Figure 4-40 Near-Field Measurement Setup

The measured data in different directions can be plotted visually. Both ferrite (NiZn), nanocrystalline and iron powder core are tested. Only the iron powder core test result is shown in this section.

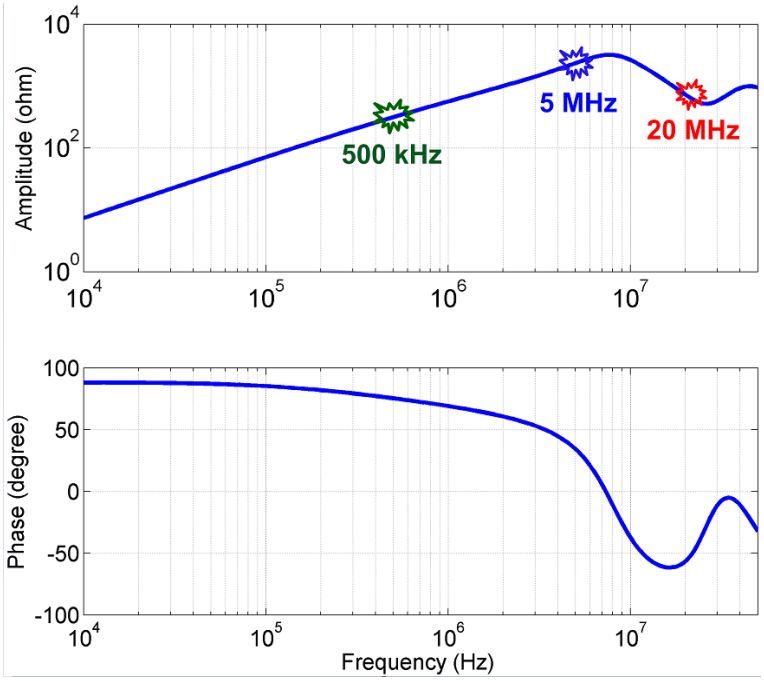
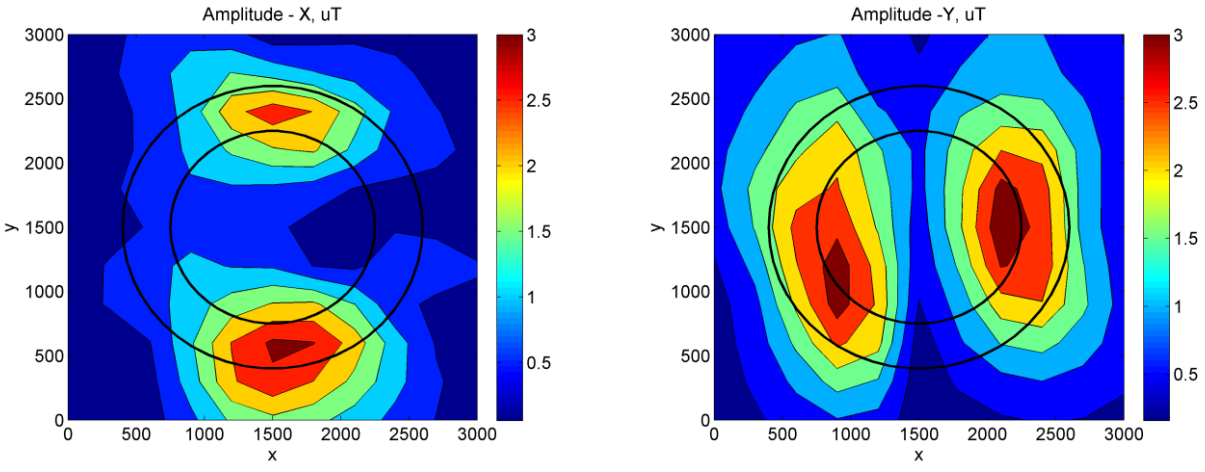


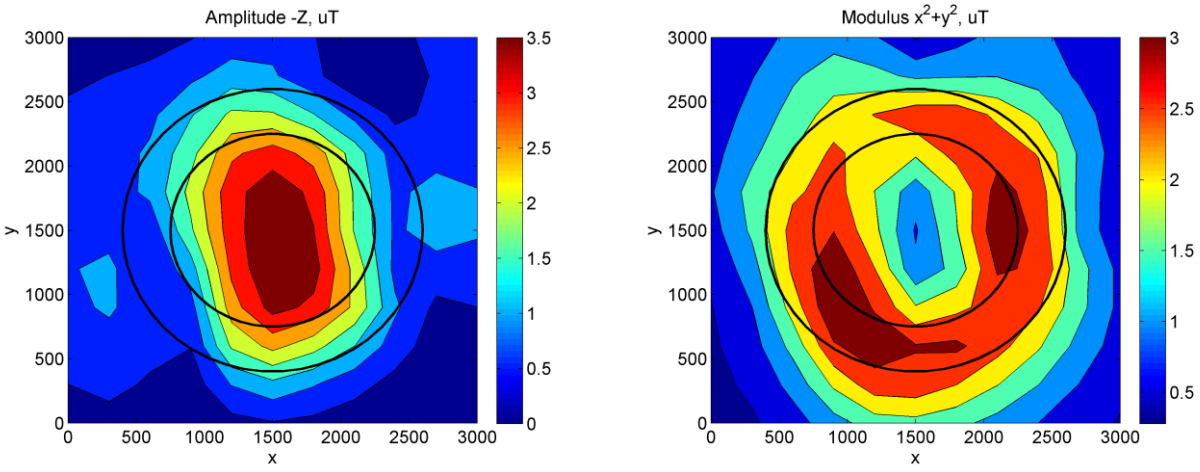
Figure 4-41 Measured impedance of the iron powder core

Figure 4-41 shows the measured impedance of the toroid shape iron powder inductor. The inductor resonant frequency is around 7MHz. In order to evaluate the near-field effect versus excitation frequency, three different frequency points are selected to do the measurement: 500 kHz, 5 MHz and 20 MHz.



(a) X direction

(b) Y direction



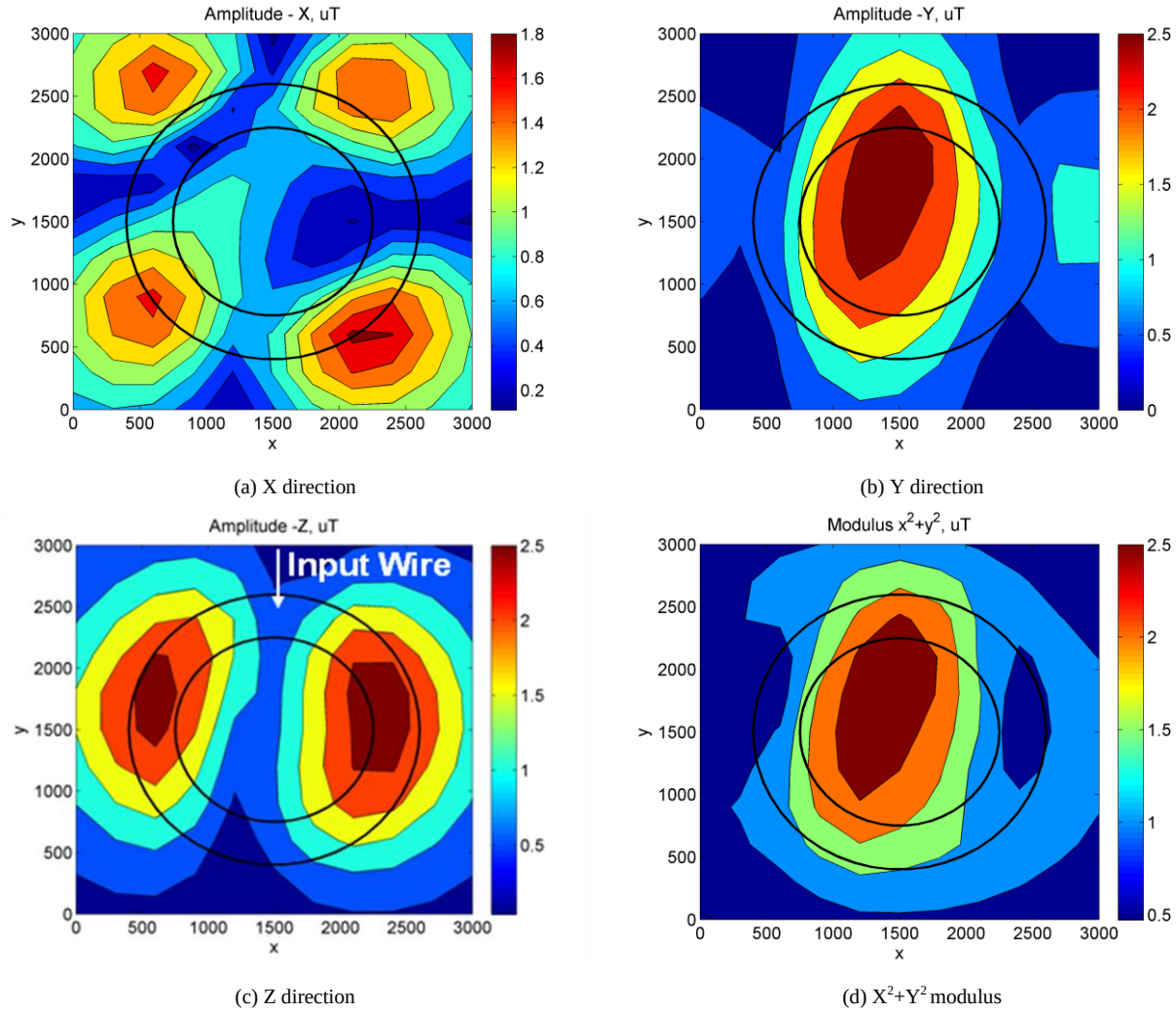
(c) Z direction (d) X^2+Y^2 modulus

Figure 4-42 Near-field stray flux measured with 500kHz excitation

The sensed near-field result is converted into flux in Tesla units. 62 V peak to peak voltage is applied to the inductor input terminal. 500 kHz excitation frequency measurement result is shown in Figure 4-42. The toroid core shape is also plotted with black line. Figure 4-42 (a), (b) and (c) show the sensed results in X, Y and Z directions. Using Figure 4-42 (a) and (b), Figure 4-42 (d) indicates the sensed modulus amplitude in XY plane. Excitation 500kHz is much lower than the tested inductor resonant frequency which is 7MHz. The near-field stray flux distribution is almost center symmetrical which matches our expectation. The Z direction shows the maximum value at the center area and the amplitude of the XY plane ($\sqrt{x^2+y^2}$) shows the minimum value at the center and maximum value with a ring shape on top of the core.

When the excitation frequency increased to 5 MHz, which is close to the inductor resonant frequency, the near-field stray flux measurement result dramatically changed when compared with the 500 kHz. The excitation voltage peak to peak value is still 62V. When comparing with center symmetrical distribution in 500 kHz tested results (Figure 4-42 (c)), two poles can be observed in 5 MHz excitation condition in the Z

direction. As shown in Figure 4-43 (c), two high stray flux amplitude areas can be observed. Because of the observed two poles, stay flux is coming from one pole to another. X direction measurement result in the middle area shows the minimum flux because the flux lines direction is parallel with the sensing coil. Y direction in the middle area shows the maximum flux amplitude because the flux lines direction is vertical to the sensing coil thus leads to maximum coupling in Y direction. Based on the measurement result, the near-field is no longer center symmetrical.



(a) X direction

(b) Y direction

(c) Z direction

(d) X^2+Y^2 modulus

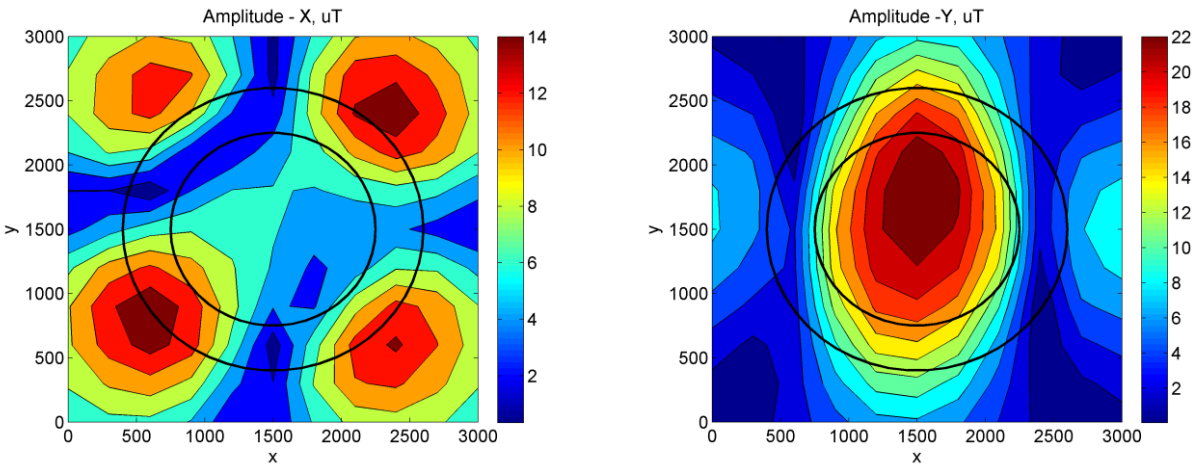
Figure 4-43 Near-field stray flux measured with 5MHz excitation

Keep the same excitation voltage peak to peak value, Figure 4-44 shows higher excitation frequency (20MHz) test results. The near-field distribution is also center

asymmetrical and two poles can be clearly observed. Meanwhile, the two poles position stays almost the same when compared with 5 MHz tested results as shown in Figure 4-43. But the amplitude is higher.

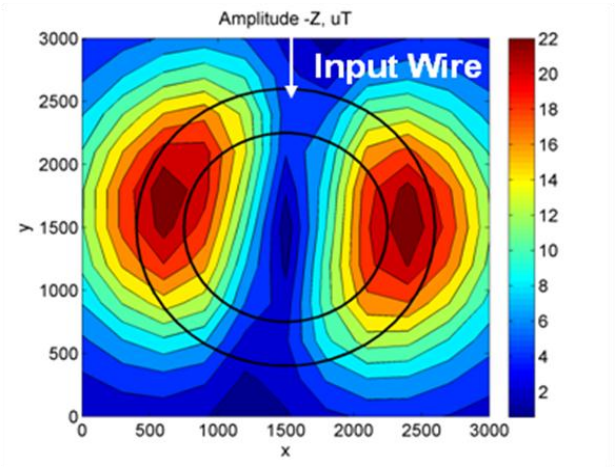
Based on the tested results shown above, the near-field stray flux measurement can be summarized. Firstly, the near-field distribution is frequency related. When the excitation frequency is low, the field distribution is center symmetrical as shown in Figure 4-42. However, when the excitation frequency close to the resonant frequency (5 MHz), two poles can be observed in Figure 4-43 and the poles positions will not change with even higher excitation frequency (20 MHz) as shown in Figure 4-44.

As shown in Figure 4-45, if the toroid core input wire is aligned with 12 o'clock in a watch, the two poles position when the excitation frequency becomes higher can be observed in the area of 3 and 9 o'clock. The changing of the near-field stray flux distribution will also change the magnetic coupling. Because of that, the Y direction coupling becomes strong and X direction coupling becomes weak in the center area.



(a) X direction

(b) Y direction



(c) Z direction (d) X^2+Y^2 modulus

Figure 4-44 Near-field measured with 20MHz excitation

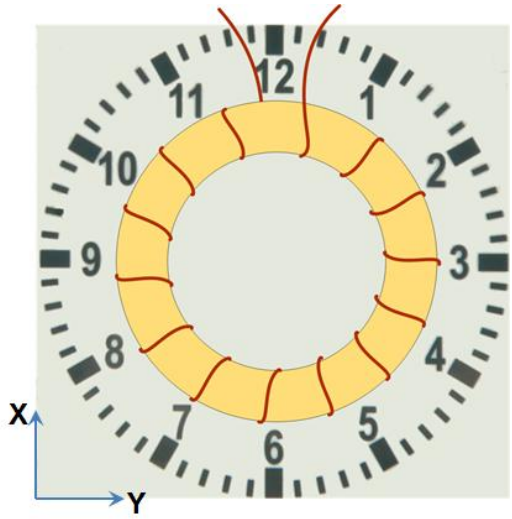


Figure 4-45 Alignment the core with the clock

4.4.2 Coupling explanation and prediction

Magnetic field coupling is essentially caused by the stray flux generated by the magnetic components such as inductors. By using the near-field probe in the measurement setup as shown above, the stray flux can be sensed and displayed visually. However, in order to explain the phenomenon and to study the near-field coupling issue with different cores or winding structures, a model is required to be

able to predict the stray flux and also predict the relationship between excitation frequency and stray flux.

A. Biot-Savart Integral Law Utilized to Calculate the Near-field

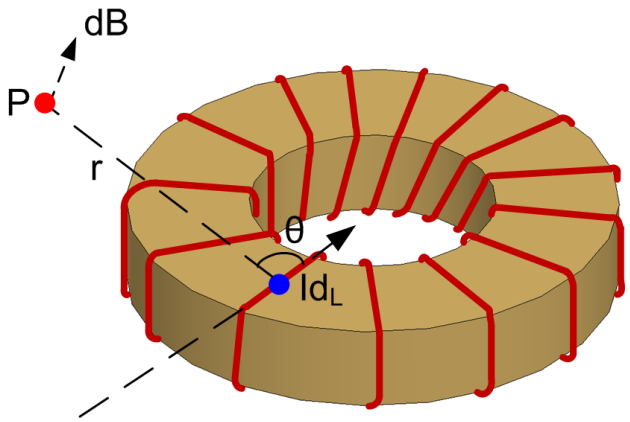


Figure 4-46 Biot and savart integral law illustration

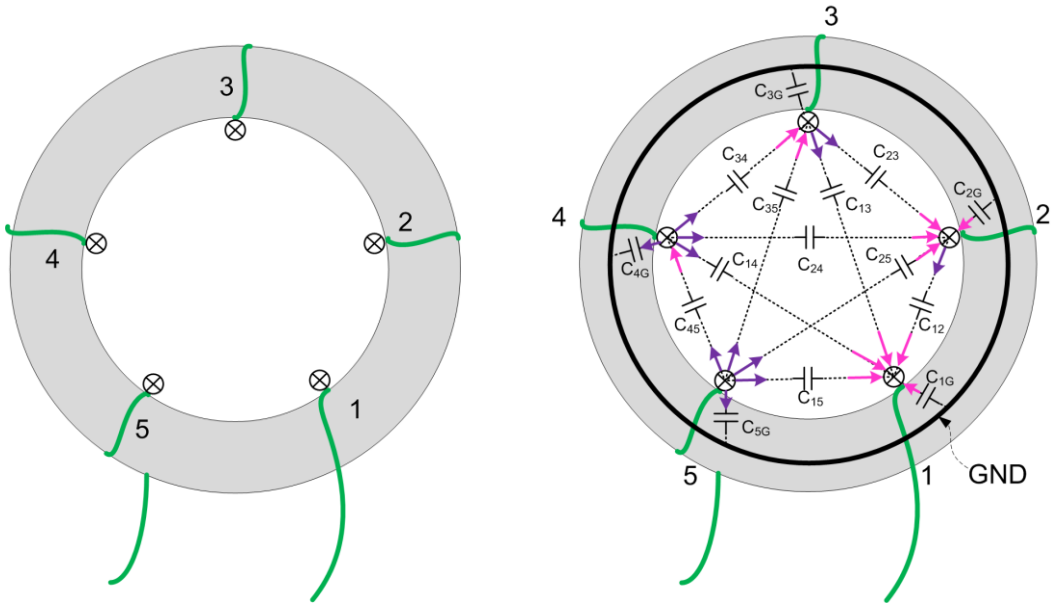
THE Biot-Savart equation is utilized to calculate the magnetic components near-field stray flux distribution. A similar concept to the Partial Element Equivalent Circuit (PEEC) will be utilized. As shown in Figure 4-46, the current cell influence to the point P can be expressed by (4-24). The total winding effect can be integrated with super-position law. The detailed calculation will be shown in Appendix and the code is implemented in MATLAB with the method proposed in [156]. This calculation will neglect the redirection of the field lines caused by the magnetic material. But similar to the assumptions in PEEC [87, 101, 157], the redirection of the field line is very limited because the focus of the investigation is only for stray flux which magnetic field lines propagate most of their way through non-ferromagnetic material.

$$dB = \frac{\mu_0}{4\pi} \cdot \frac{Idl \sin\theta}{r^2} \tag{4-24}$$

B. High Frequency Near-Field Explanation

As shown in Figure 4-42 above, center symmetrical stray flux distribution can be observed in 500 kHz measurement result which matches our expectation. However, as

shown in Figure 4-43 and Figure 4-44, the near-field distribution changes dramatically when the excitation frequency close to the inductor resonant frequency or higher. The reason will be analyzed in this section.



(a) Five turns model (b) Equivalent model including stray capacitance

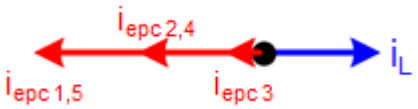
Figure 4-47 High frequency near-field explanation

A simplified five turns' model as shown in Figure 4-47 (a) is utilized to explain the near-field stray flux distribution in high-frequency condition. When the excitation frequency goes higher especially close to the inductor resonant frequency, the effect of the stray capacitor cannot be ignored, which means the coupling between the electrical field and magnetic field cannot be considered to be decoupled. The equivalent parallel capacitors (EPC) for both turn-to-core and turn-to-turn are depicted in Figure 4-47 (b). All the turn to core equivalent capacitors are shorted to represent the high conductivity of the core such as iron-powder. Since the excitation voltage is applied between the input wires turn 1 and turn 5, voltage stress will be different for different stray capacitors. Then, the displacement current caused by the stray capacitor will not become uniform but axial symmetrical. The axis passes through turn 3 and divided the core into left hand side and right hand side. The

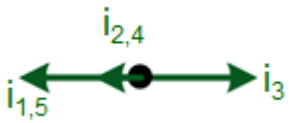
displacement current goes to turn 3 will be fully cancelled. The displacement current goes to turn 1 and 5 is maximum. Displacement current goes to turn 2 and turn 4 is lower than turn 1 and 5.

(a) Displacement & magnetic current for low frequency

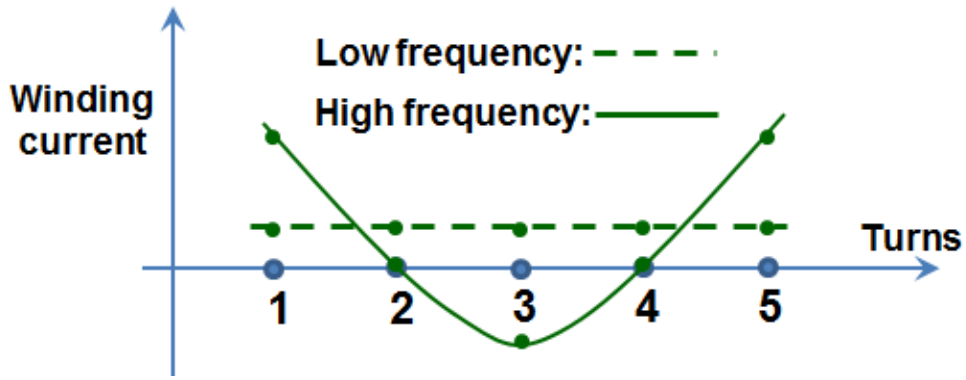
(b) Winding current for low frequency



(c) Displacement & magnetic current for high frequency



(d) Winding current for high frequency



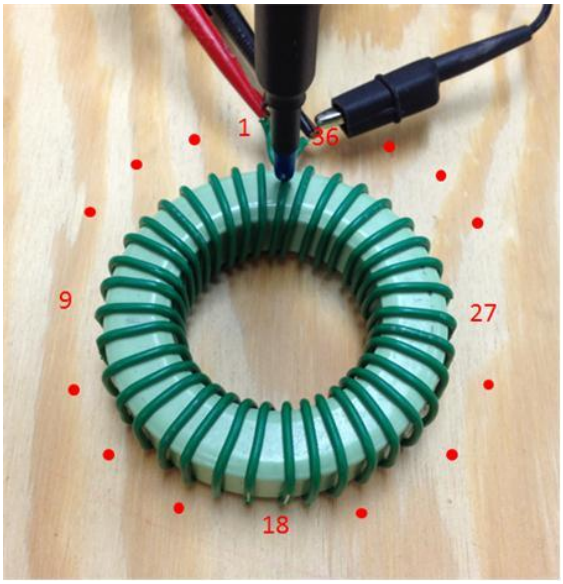
(e) Winding current distribution for both low and high frequency

Figure 4-48 Winding current distribution

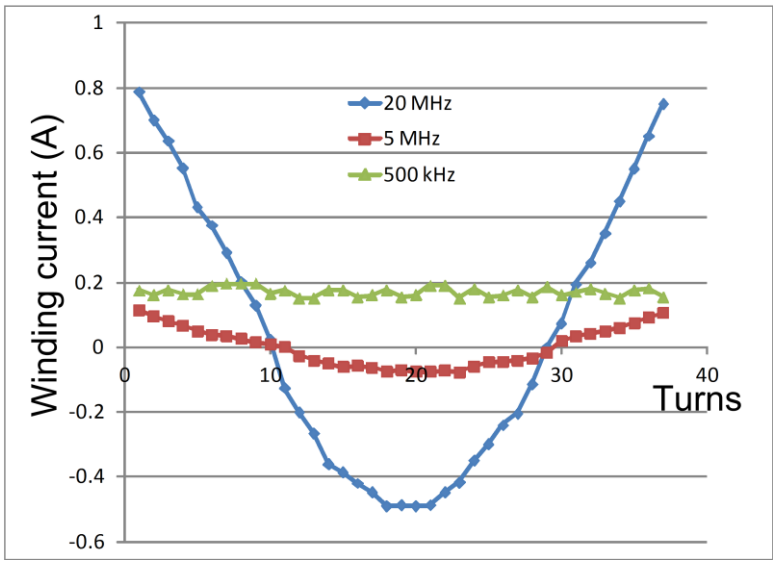
Based on the analysis above, the total winding current is composed of two parts: conductive current and displacement current caused by the stray capacitance. When the frequency becomes close or higher than the inductor resonant frequency, displacement current becomes dominant, which will in turn influence the winding current distribution.

Figure 4-48 shows the winding current distribution with both low and high frequency conditions. Figure 4-48 (a) and (b) demonstrate the principle when the frequency is low, displacement current is negligible and the winding current is uniform for all the turns. Because of that, the near-field flux caused by the magnetic components will become center symmetrical. The high frequency condition is shown

in Figure 4-48 (c) and (d). When the displacement current becomes dominant, the winding current distribution is not uniform and winding 1 and 5 show the maximum value.



(a) Winding current distribution measurement



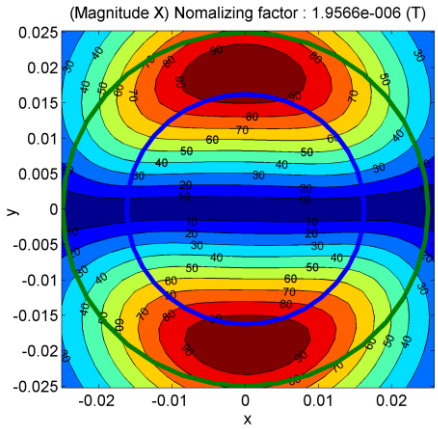
(b) Winding current distribution measurement results

Figure 4-49 Winding current distribution measurement

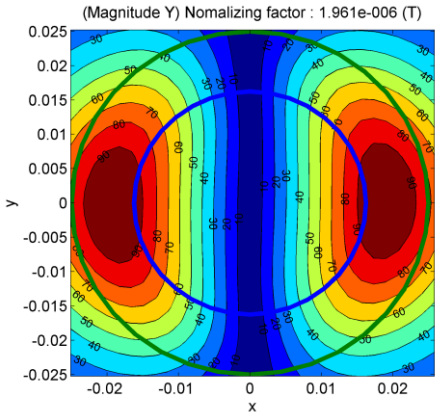
Based on the analysis, the real winding current is monitored by using probe LF-U 2,5 which is designed for selective detection of the current spectrum in singular small conducting paths and component connections. The setup for the winding current measurement is shown in Figure 4-49 (a). The winding turns are labeled from 1 to 36.

The excitation voltage amplitude keeps the same as previous measurement and is applied between turn 1 and turn 36. Three different excitation frequencies are applied to monitor the winding current distribution. Figure 4-49 (b) shows the tested results for both 500 kHz, 5 MHz and 20 MHz. For the lower frequency excitation, the winding current is almost uniform and the polarity of the winding current is always positive. However, for the higher frequency excitation, the winding current distribution is not uniform and matches with our analysis based on Figure 4-48 (e).

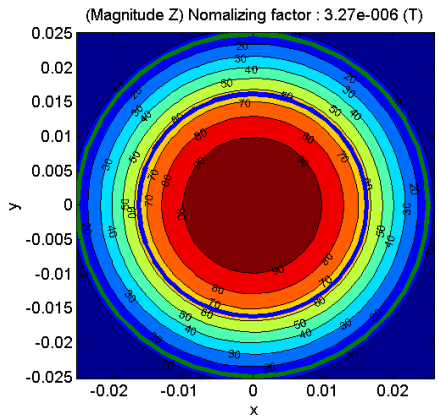
Based on the proposed calculation method with the Biot-Sarvart equations and measured winding current in Figure 4-49, the near-field stray flux distribution of toroid core with the uniform winding pattern in 500 kHz excitation frequency can be predicted and shown in Figure 4-50.



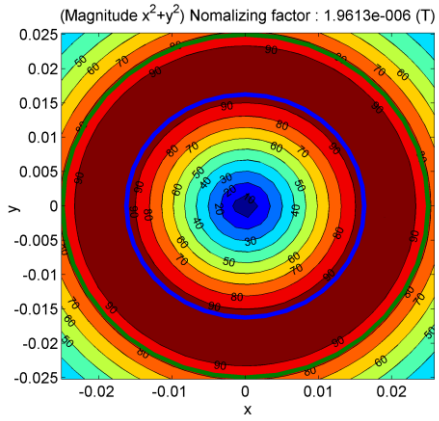
(a) X direction



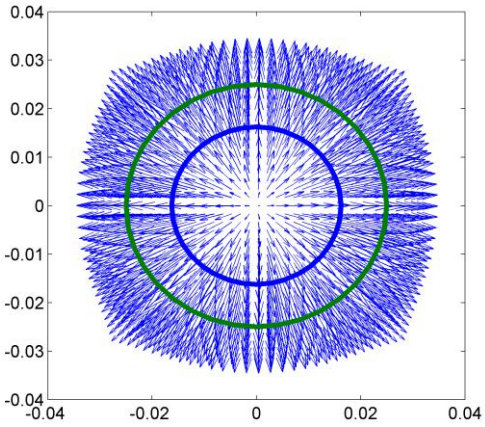
(b) Y direction



(c) Z direction



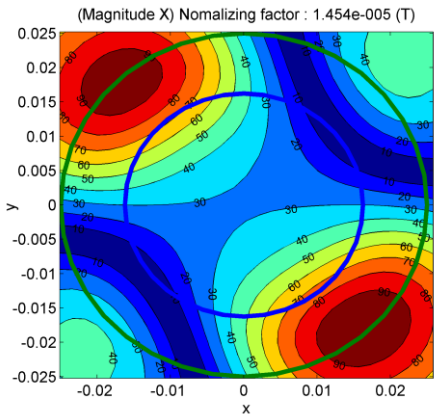
(d) X^2+Y^2 modulus



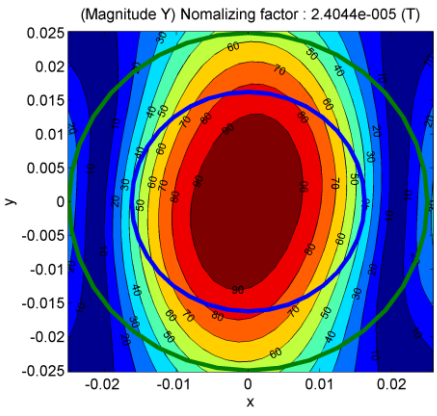
(e) Flux direction

Figure 4-50 Predicted near-field stray flux with biot-savart equation in 500 kHz

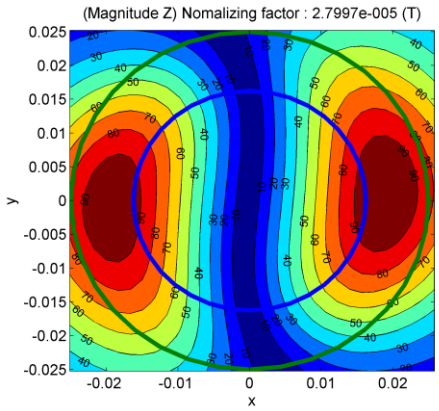
Figure 4-50 (a) to (d) matches the experimental results shown in Figure 4-42 in all the measured directions. Figure 4-50 (e) shows the flux direction by using the quiver function from MATLAB. The near-field distribution is center symmetrical. The flux comes from the center and spreads out to form a close loop that encircles the whole core. Because of that, the Z direction has maximum amplitude in the center area and the amplitude of the XY plane ($\sqrt{x^2 + y^2}$) has maximum amplitude with a ring shape on top of the core. With uniform current distribution, the predicted near-field matches well with the experimental results.



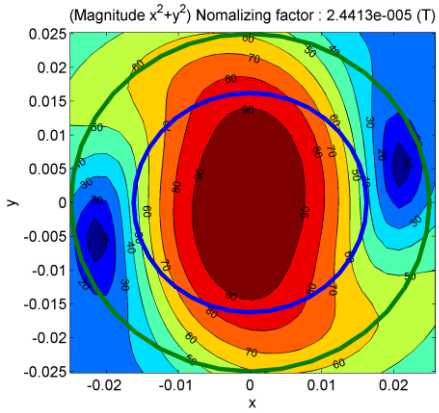
(a) X direction



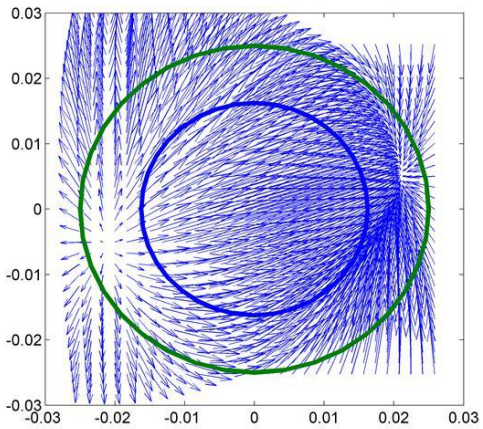
(b) Y direction



(c) Z direction



(d) X^2+Y^2 modulus



(e) Flux direction

Figure 4-51 Predicted near-field stray flux with biot-savart equation in 20 MHz

By using the calculation tool based on the Biot-Savart equations and the non-uniform current distribution in 20 MHz as shown in Figure 4-49, the near-field stray flux distribution for 20 MHz is shown in Figure 4-51. The predicted calculation results match very well with experiment results in Figure 4-44. Figure 4-51 (e) shows the flux direction and two poles can be observed. The two poles position located in the 3 and 9 o'clock which match well with the Figure 4-45.

In order to predict the displacement current distribution, a simplified model is presented in Figure 4-52. A high conductivity core is assumed. Beside the turn to core capacitor, only adjacent turn to turn capacitor is considered.

With the similar stray capacitance calculation as shown in Figure 4-5, the displacement current is calculated with 62V peak to peak excitation for both 5 MHz and 20 MHz excitation frequencies. The calculated displacement current is shown in Figure 4-53. The relationship of the displacement current versus the number of turns can be simplified as a triangular shape, which means the turn to core capacitor is more dominant when compared with turn to turn capacitor.

The displacement current becomes higher when the excitation frequency is higher which matches with the measurement results as shown in Figure 4-49. The relationship of the displacement current versus the input cable is shown in Figure 4-53 (b). Maximum displacement current can be observed around the input cable.

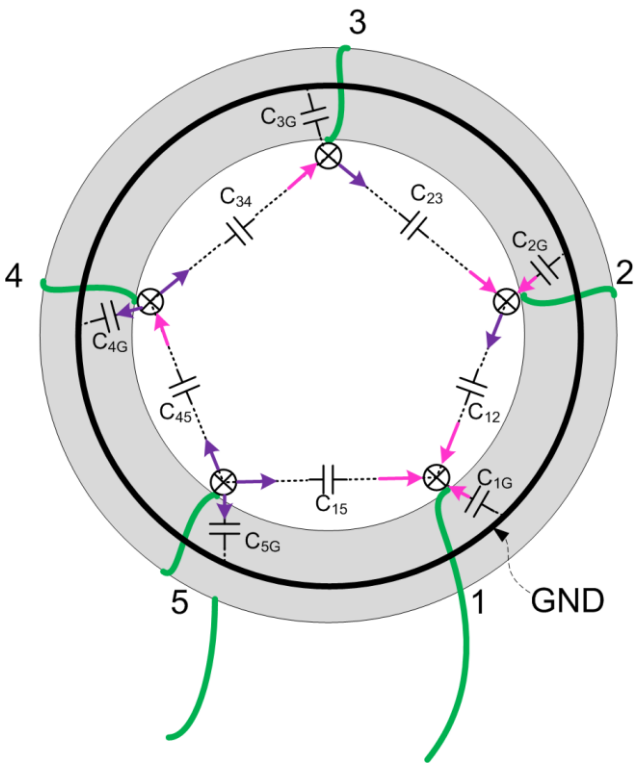
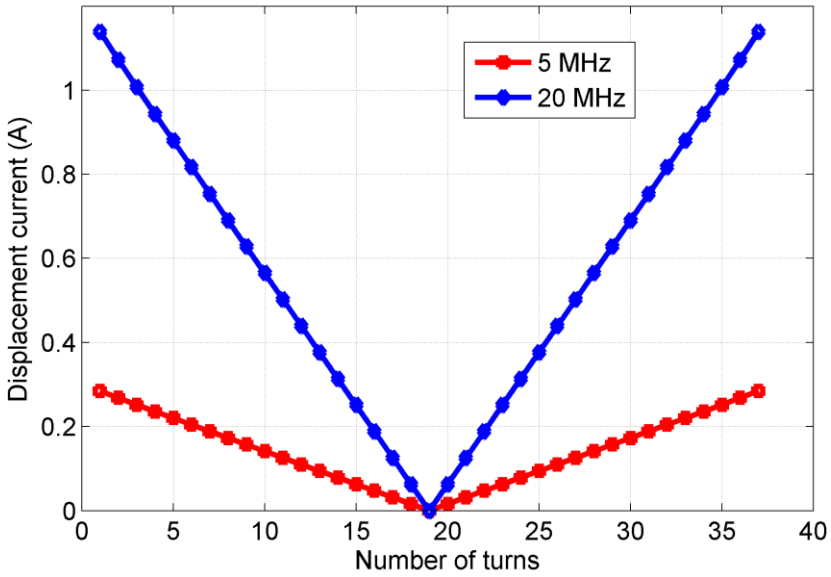
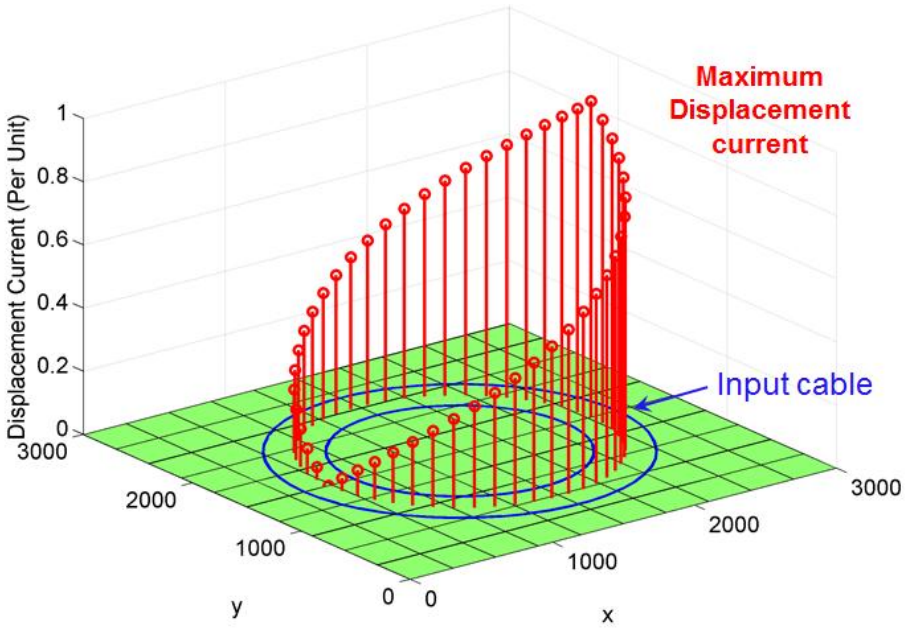


Figure 4-52 Simplified model to predict winding current



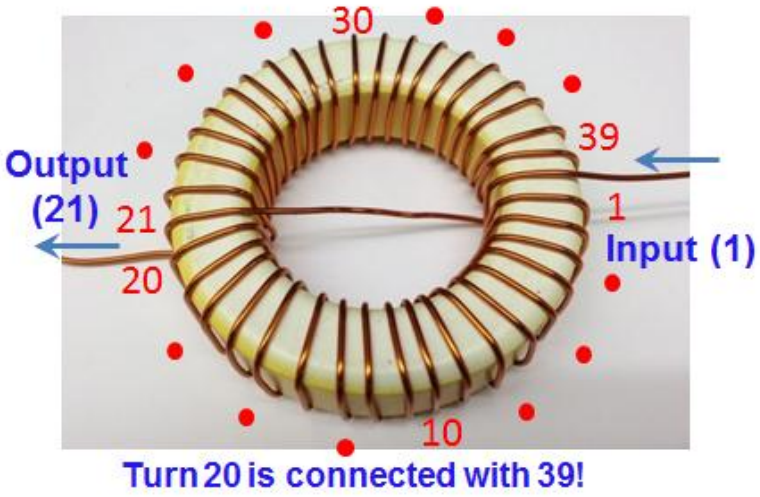
(a) Current distribution calculation with simplified model



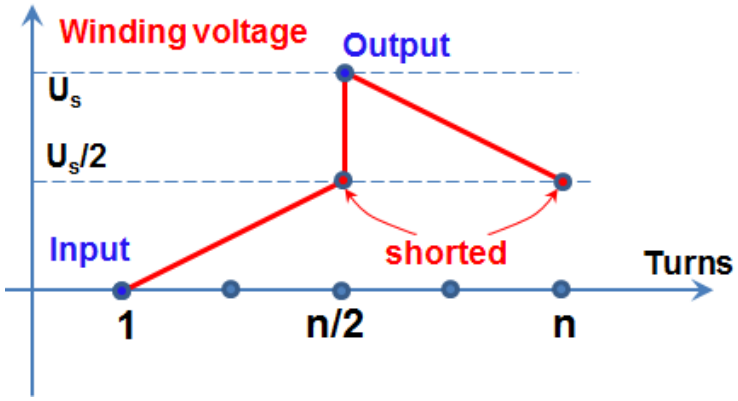
(b) Current distribution position with input cable

Figure 4-53 Current distribution

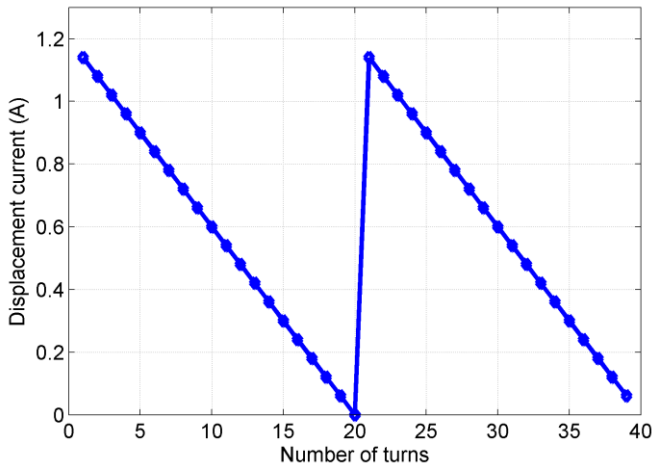
C. Near-Field Distribution Prediction with the Proposed Model



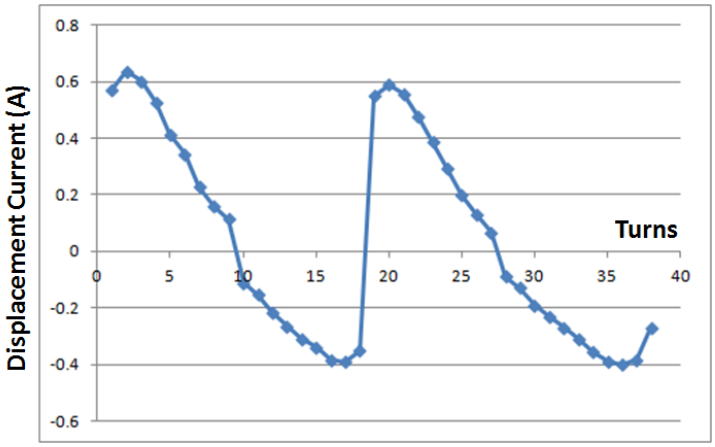
(a) Winding structure



(b) Winding voltage



(c) Winding current prediction



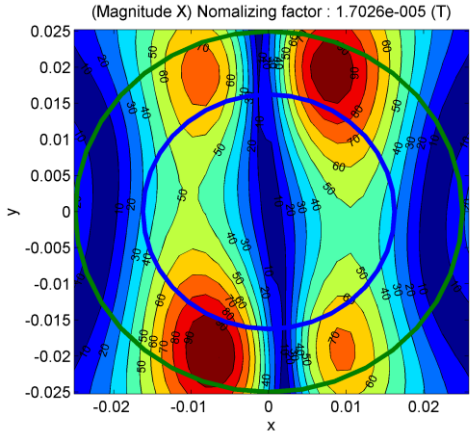
(d) Winding current measurement

Figure 4-54 Improved winding near-field prediction

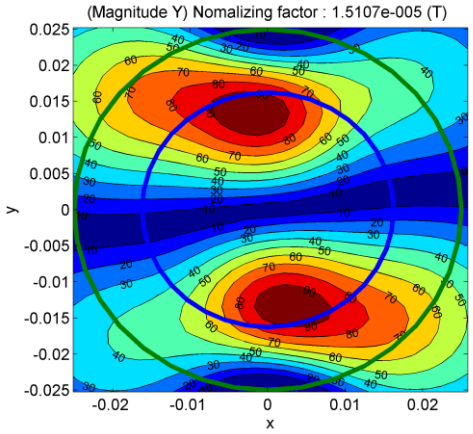
The previous analysis shows the displacement current influence to the winding current and the high frequency near-field stray flux distribution. Based on this analysis, high frequency near-field distribution for different winding structures should also be predictable.

Figure 4-54 (a) shows an improved winding structure which is widely used for cancelling the inner flux [103]. The inductor is composed of 39 turns. The input wire is turn 1 and the output wire is turn 21. Turn 20 and turn 39 are shorted. This improved winding structure will be utilized as an example to predict the near-field stray flux distribution in high frequency. With this winding structure, the winding voltage is shown in Figure 4-54 (b). Half of the excitation voltage is applied between turn 1 and turn 20. Since turn 20 and turn 39 are shorted, the voltage stress between turn 20 and turn 21 is also half of the total voltage. With the winding voltage as shown in Figure 4-54 (b), the winding current distribution prediction with conductive core (turn to core capacitance will be dominant) can be depicted as Figure 4-54 (c) in 20 MHz. The displacement current of the input and output winding shows the maximum value. The displacement current cancelled at half of the number of turns. With the same measurement setup as shown in Figure 4-49 (a), the winding

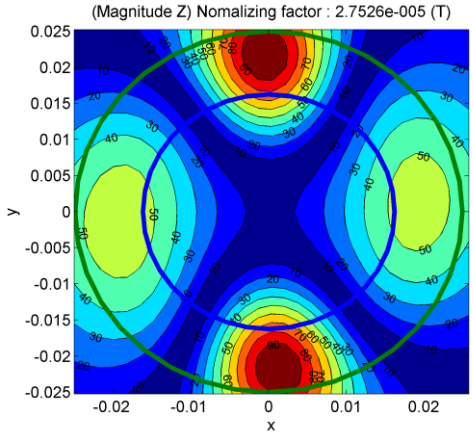
displacement current in 20 MHz is measured and shown in Figure 4-54 (d), which matches with the predicted results.



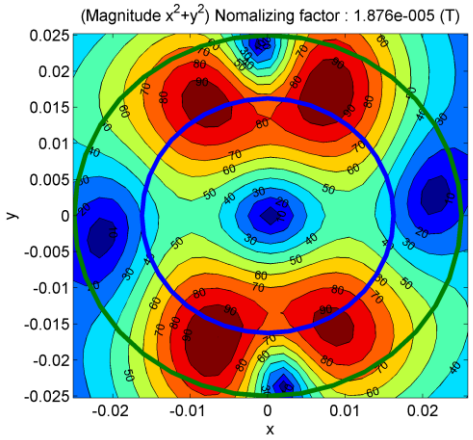
(a) X direction



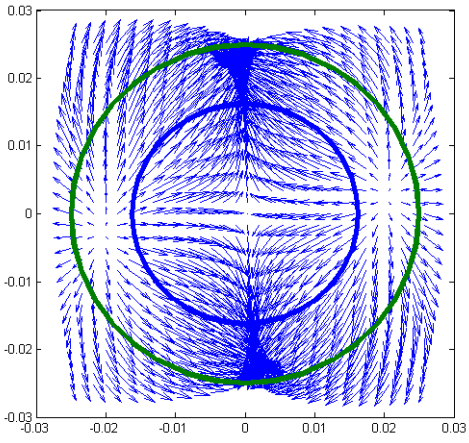
(b) Y direction



(c) Z direction



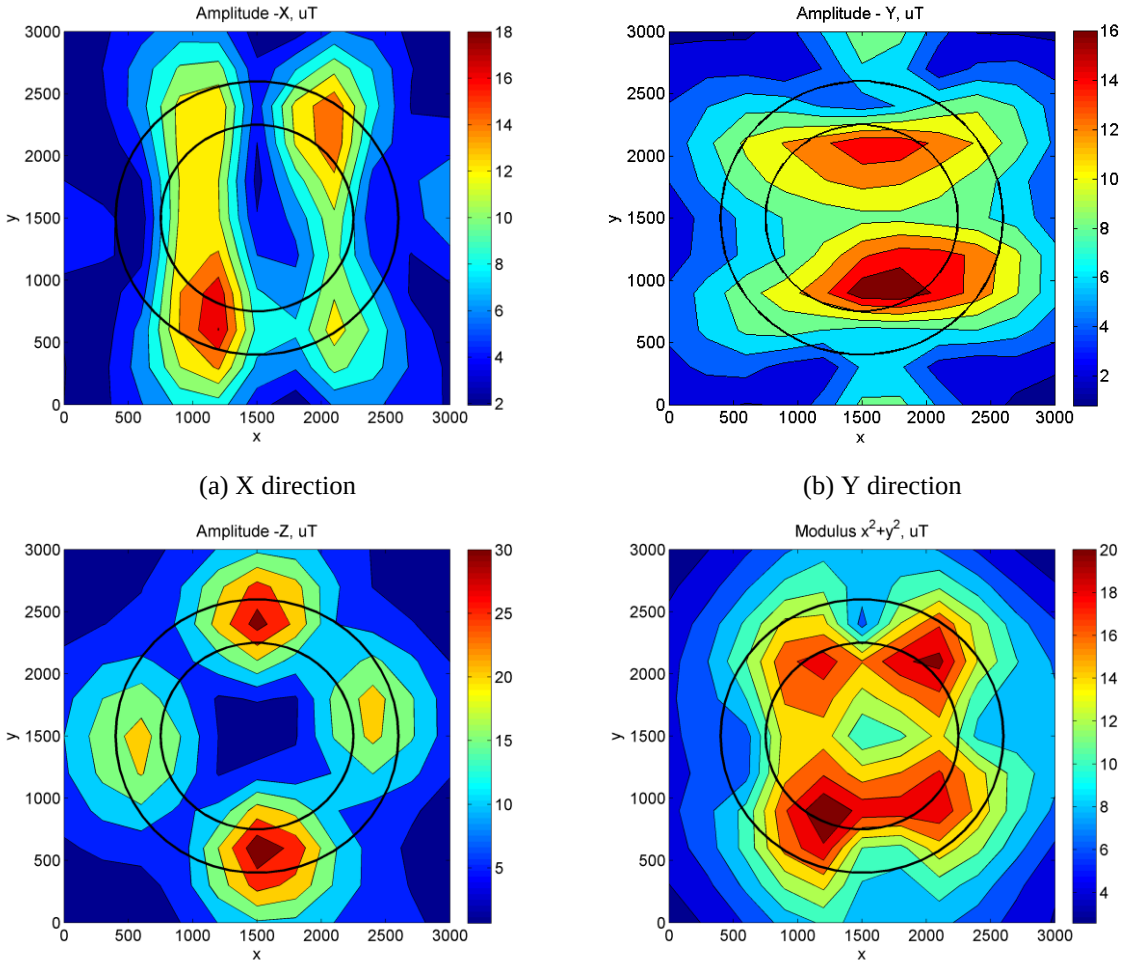
(d) X^2+Y^2 modulus



(e) Flux direction

Figure 4-55 Predicted near-field with biot-savart equation for improved winding structure in 20 MHz

With the predicted winding current distribution and the Biot-Savart equation, the near-field stray flux distribution for the improved winding structure in different directions is shown in Figure 4-55. Four poles can be observed with the predicted results. The flux comes out from two poles and merges into other adjacent two poles.



(a) X direction (b) Y direction

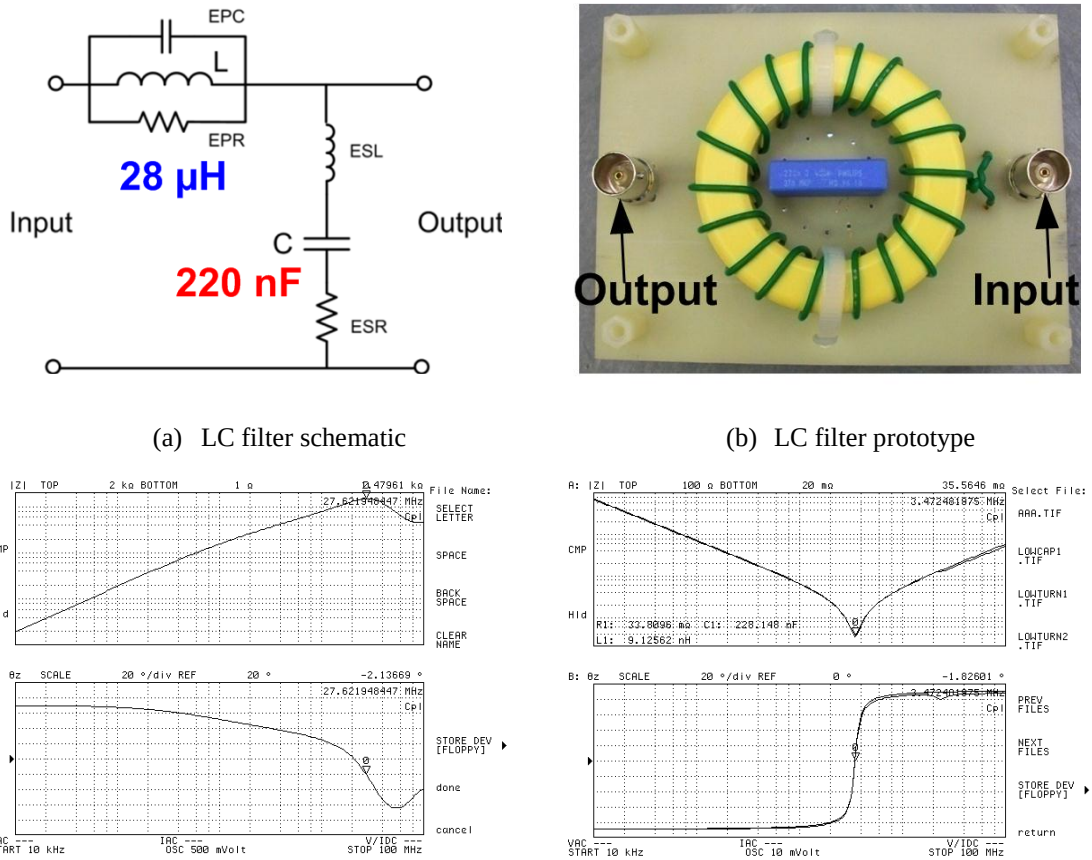
(c) Z direction (d) X^2+Y^2 modulus

Figure 4-56 Near-field stray flux measured with 20MHz excitation

The real near-field measurement with this winding structure in high frequency (20MHz) is also measured with the proposed method as shown in Figure 4-40. Figure 4-56 shows the measurement results. It matches very well with the theoretical prediction results shown in Figure 4-55. The proposed high frequency near-field distribution model is proved to be accurate enough.

With the proposed model and the knowledge that the coupling can be divided into both low frequency and high frequency, better EMI filter design procedure and layout solution can be proposed. An example is presented in the following section.

4.4.3 LC filter coupling demonstration



(a) LC filter schematic (b) LC filter prototype

(c) Inductance impedance measurement (d) Capacitance impedance measurement

Figure 4-57 Low turns inductor LC filter demonstration

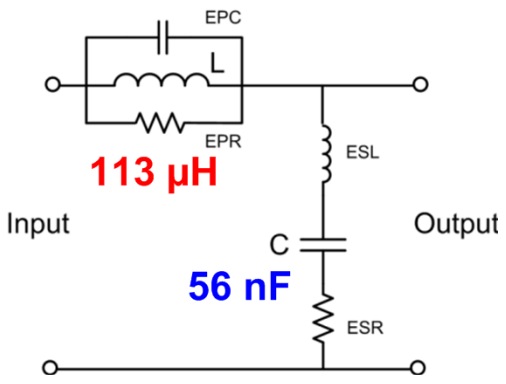
Based on the previous sections analysis, the magnetic component near-field stray flux distribution can be divided into low frequency and high frequency conditions. When the frequency gets close to the magnetic component resonant frequency, the displacement current caused by the stray capacitance will dramatically change the magnetic component near-field stray flux distribution and can be predicted

accordingly. Then, better EMI filter performance can be achieved by better layout design.

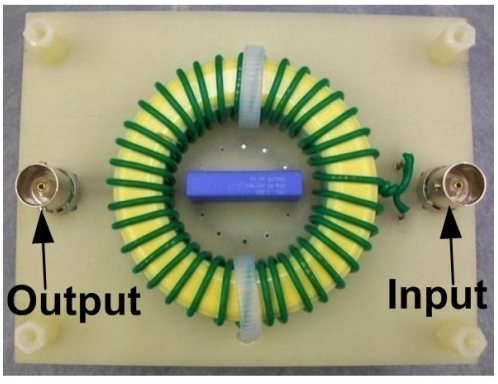
A single stage DM LC filter is utilized as an example to demonstrate this phenomenon and its influence to EMI filter performance.

Figure 4-57 shows the case 1 design with a low turns (20 turns) inductor (28μH) and capacitor (220nF) that composes a single stage DM LC filter. The inductor is made of iron-powder core which is tested in previous sections. The inductor and capacitor impedance is shown in Figure 4-57 (c) and (d). The corner frequency of the LC filter is 63 kHz and the resonant frequency of the inductor is around 30MHz. Since the resonant frequency of the inductor is high, the displacement current influence on the field distribution is negligible for the frequency range lower than 30 MHz.

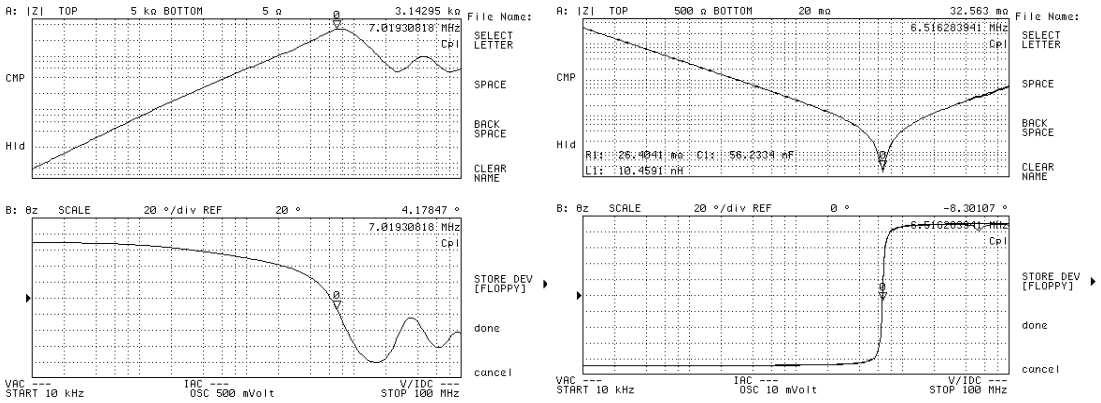
In contract with case 1, a second case 2 design of the DM LC filter utilizes a high turns (40 turns) inductor (113 μH) and a smaller capacitor (56nF) that have the same filter corner frequency of also 63kHz. However, since the resonant frequency of the inductor is only 7MHz as indicated by Figure 4-58 (c), the near-field flux becomes center asymmetrical when the excitation frequency gets close to 7MHz.



(a) LC filter schematic



(b) LC filter prototype



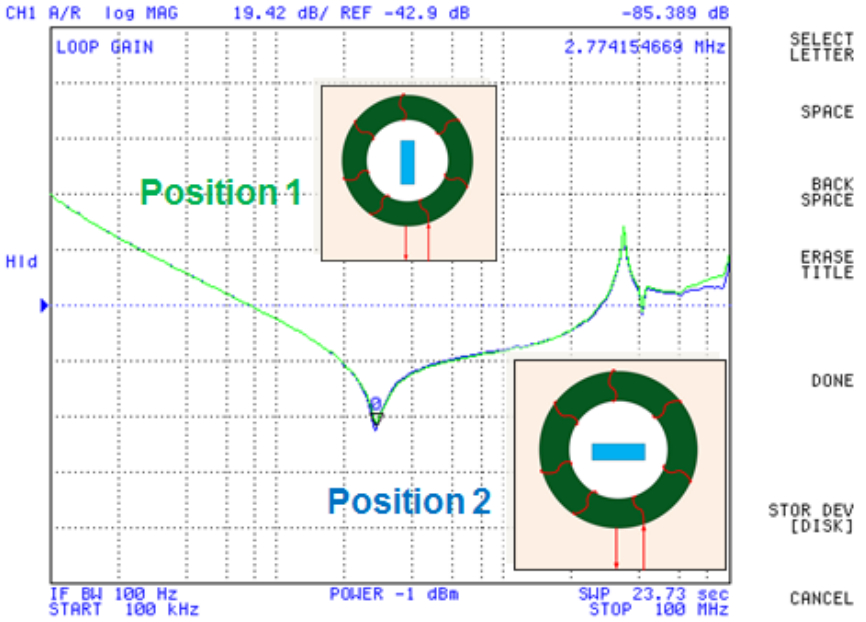
(c) Inductance impedance measurement (d) Capacitance impedance measurement

Figure 4-58 High turns inductor LC filter demonstration

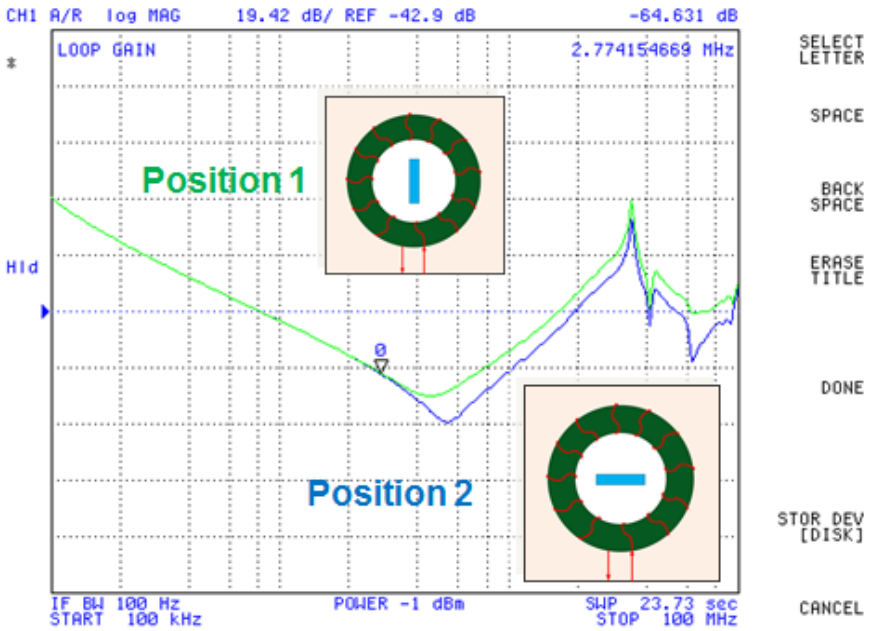
The layout of both the two cases DM LC filters is designed in the same way: the capacitor is put in the center area of the toroid core. Moreover, the center capacitor can be rotated to test the different performance in terms of coupling. As mentioned above, the resonant frequency of the low turns inductor case is very high so that the displacement current influence on the high frequency coupling is not obvious. The stray flux is still center symmetrical. Rotating the capacitor into both positions 1 and position2 shows no difference in terms of the LC filter transfer gain test, which is indicated in Figure 4-59 (a). However, for the high turns inductor case, the displacement current influence becomes obvious when the excitation frequency close to the inductor resonant frequency. Since two poles can be observed at 3 and 9 o'clock, which is indicated by Figure 4-45, the position 1 has maximum coupling and position 2 has minimum coupling. Figure 4-59 (b) shows the minimum coupling condition can achieve 10 to 15dB better performance compared with maximum coupling by LC filter transfer gain test.

By using only the low frequency coupling theory shown in the previous literatures, both the two positions are center symmetrical and should not be different. So, this phenomenon cannot be predicted by using only low frequency coupling theory.

However, with the proposed theory and model, it is now possible determine that the position 2 is preferred compare with position 1 since the coupling is smaller.



(a) Low turns inductor LC filter transfer gain



(b) High turns inductor LC filter transfer gain

Figure 4-59 Transfer gain test

4.4.4 Shielding method to alleviate coupling

As shown above, one of the most common concerns for compact EMI filter are the coupling issues which may degrade the filter attenuation capability. This is especially true for the transportation applications, the EMI filter need to be compact in order to fit in a limited space. Utilizing the method such as a tower type connection makes the coupling effect even worse. Thus, different shielding candidates are studied with a near-field probe in this section to evaluate the performance of coupling reduction in the compact multiple stage tower connection EMI filter design. Figure 4-60 shows the shielding candidates that includes copper plates and magnetic film. The copper plates are divided into two different thicknesses: 2 mil and 10 mil. The copper plates are also etched into different patterns with the same trace width of 50 mil. In addition to the copper shielding, Ferrite Polymer Composite (FPC) film sheet with relative permeability of μ=9±20% is also applied.

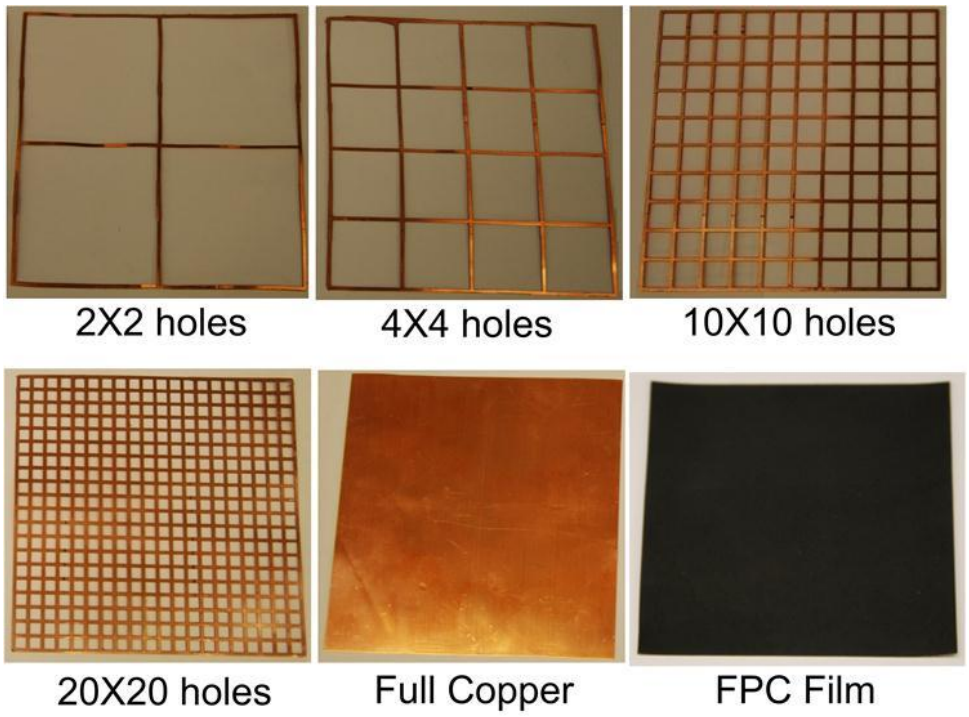
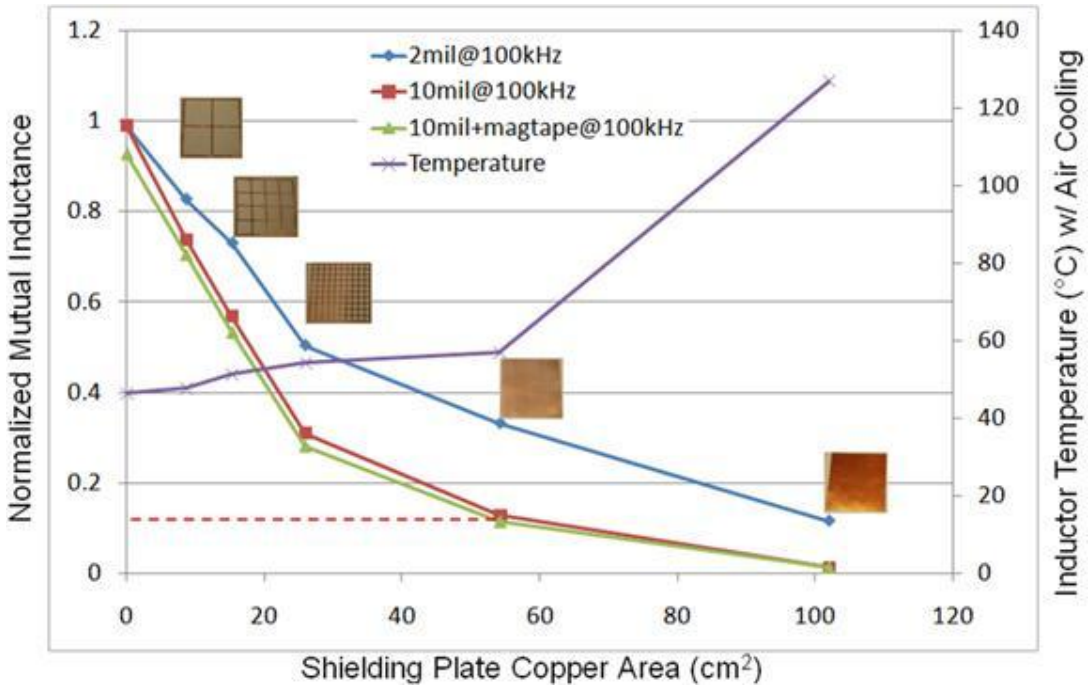


Figure 4-60 Shielding candidate

(a) Coupling measurement setup



(b) Coupling measurement results

Figure 4-61 Coupling measurement with near-field probe

In order to quantify the coupling effect, a coupling measurement setup was designed and is shown in Figure 4-61 (a). The Tektronix AFG3102 signal generator together with a power amplifier are utilized to generate the excitation power to the DM core, and the LF R 400 near-field probe from LANGER is connected to the scope to monitor the flux coming from the core. Different shielding candidates are inserted between the sensing probe and DM inductor. Meanwhile, a fan is blowing air from the top to the bottom. The sensed result is shown in Figure 4-61 (b). Different excitation frequencies are utilized from 100 kHz to 1 MHz. Only 100 kHz is shown in

this result. The 10 mil copper sample has a better shielding performance when compared with the 2mil copper sample under low frequency excitation. The performance difference between 2mil and 10mil is not obvious in high frequency because of the skin effect. The more copper utilized, the better the performance to reduce coupling. Copper with 20 by 20 holes pattern will decrease the coupling to around 10%. The shielding performance can be further improved with more copper but the thermal performance becomes dramatically worse because the air flow is blocked. The FPC film will improve the shielding performance a little. Based on the test results, 20 by 20 holes copper plate is selected as the shielding plate. Its improvement in the transfer gain test is shown in Figure 4-62.

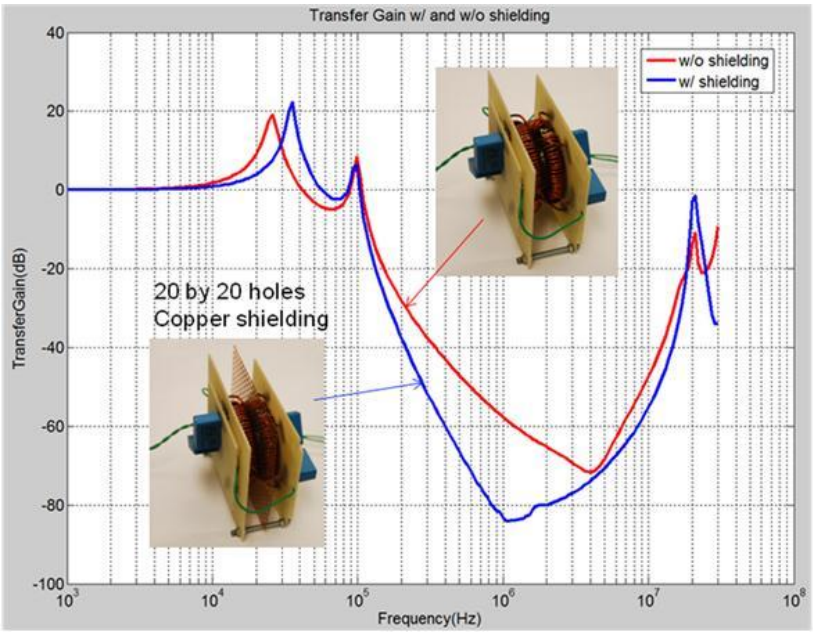


Figure 4-62 Transfer gain test with and without shielding

The noise measurement with in circuit test is shown in Figure 4-63. The noise decreases more than 10dB from 1MHz to 10MHz with shielding, which agrees with the small signal transfer gain test as shown in Figure 4-62.

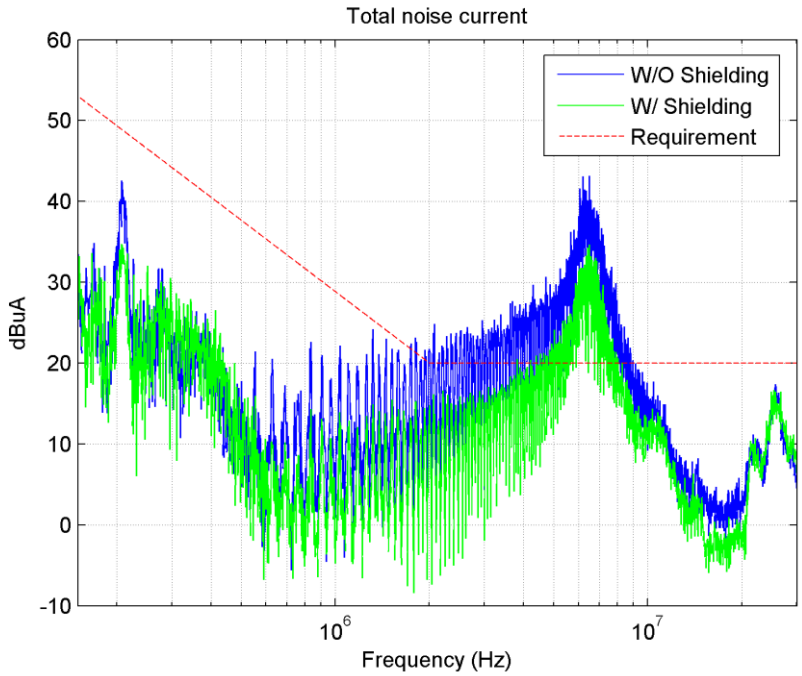


Figure 4-63 Noise measurement with in circuit test

4.5 Conclusions

This chapter proposed a design procedure for a high power density EMI filter with consideration of the parasitic. With the proposed method, the optimum number of stages and components value can be systematically derived given a fixed operating point. From the design results, the multiple stage DM EMI filter has a minimum volume when the low frequency and high frequency attenuation requirements are high. For CM EMI filter design, the optimum number of stages can be derived to avoid saturation problem and achieve minimum volume.

However, a real insertion loss might be different with transfer gain because of the non-ideal case for both source and load impedance. Besides the possible impedance resonant, a non-linear impedance also exists in the real system and lumped RLC model may not be able to be used. In order to deal with this, successful insertion gain predictions for both DM and CM for three-phase PFC converter has been presented in this work using a frequency domain model in the numerical way. This approach is based on a simple equivalent circuit containing four parameters, which are easy to

identify. A great part of this work focuses on the source impedance, which is the most complex part of this equivalent circuit. The objective of these analyses is exploring whether the source impedance can be masked by time invariant impedance. The study, based on equivalent circuit decomposition, shows that the source impedance, under certain conditions, can be masked by a time invariant impedance.

Meanwhile, this chapter also theoretically revealed and classified the EMI filter coupling issue into “Low Frequency Magnetic Field Coupling” and “High Frequency Magnetic Field Coupling” usually observed after the corner frequency in high frequency range. Both of them should be considered in the EMI filter design. For “High Frequency Magnetic Field Coupling”, the magnetic component near field distribution will change dramatically and the reason is caused by the displacement current through EPC. Since the field distribution changed a lot, the components layout will obviously influence the EMI filter performance which cannot be predicted by the “Low Frequency Magnetic Field Coupling” theory. Improper design may cause the high frequency magnetic field coupling range at low frequency (Even lower than 1MHz). In order to reduce the coupling effect caused by the components near-field, reticular shielding plates can be selected to achieve good balance of both shielding and thermal performance.

Chapter 5. Summary and Future Work

5.1 Summary

This research dissertation covers the work for high power density, high temperature converter design for transportation applications. The following is a summary of this work:

(1). If fault-tolerance function is required for the transportation applications, multiple single phase converters system will be adopted. For a single-phase rectifier, since the 2^{nd} order low-frequency ripple power will appear on the dc bus, a bulky dc bus capacitor is required to limit the dc bus voltage ripple, resulting in large converter volume and low power density. The relationship between ripple energy and other system parameters in the single phase converter is analyzed and established. Therefore, once the output power and the ac side system parameters are fixed, there is a minimum ripple energy storage requirement no matter what kind of single phase converter topologies or what kind of energy storage components are selected. The feasibility of decreasing the volume of the ripple energy storage capacitor is verified by using the active ripple energy storage method which can effectively store the ripple power in auxiliary capacitors instead of capacitors that are put in the dc bus.

(2). An active ripple energy storage method which uses a bidirectional buck-boost converter as the auxiliary ripple energy storage circuit is proposed. The proposed auxiliary ripple energy storage method will not lead to voltage higher than the dc bus in the system; meanwhile, the auxiliary circuit can be easily integrated together with

the H-bridge rectifier as one phase leg. Feed forward digital control is utilized for the auxiliary circuit. A 15 kW high power density single phase rectifier is developed to verify the proposed active ripple energy storage method. From the test results, the ripple energy can be effectively stored in the auxiliary circuit. The single phase H-bridge rectifier with the active ripple energy storage method can decrease the volume to 50% when compared with the rectifier without active method.

(3). A novel hybrid structure for high-temperature SiC power modules is presented in this work. The hybrid structure can achieve the same footprint and similar parasitic as the planar structure without using double-side solderable devices. In addition, more flexible die-attachment material selection is possible and the processing complexity and time are reduced. A three-phase single-switch multiple chips power module prototype is built to demonstrate the feasibility of this packaging method. The experimental results demonstrate the three phase rectifier module capability of working in 250°C junction temperature.

(4). A detailed design process of a high-temperature converter that can operate at an ambient temperature above 150°C is proposed. An edge-triggered high-temperature gate drive solution is also proposed to drive the designed power module. In addition, the whole system is designed according to the available high-temperature components, including the passive components, silicon-on-insulator chips and the auxiliary components. Finally, the fabricated lab prototype is tested in the harsh environment ambient for verification.

(5). A design procedure for high power density EMI filter with consideration of the parasitic is proposed. With the proposed method, the optimum stage number and components value can be systematically derived given a fixed operating point. From the design results, the multiple stage EMI filter has a minimum volume when the low frequency and high frequency attenuation requirements are high.

(6). Successful insertion gain predictions for both DM and CM for high temperature three-phase converter have been presented in this work. The approach is based on a simple equivalent circuit containing four parameters easy to identify. A great part of this work focuses on the source impedance, which is the most complex part of this equivalent circuit. The objective of these analyses is to explore whether source impedance can be approximated masked by time invariant impedance. The study, based on equivalent circuit decomposition, shows that the source impedance, under certain conditions, can be approximated by a time invariant impedance. On the other side, if these conditions are not met, all the equations are provided to study the variability of the source allowing the designer to apply the proposed approach to their own systems. Finally, the experimental results of both common mode (CM) and differential mode (DM) proves the accuracy of the predictions.

(7). This dissertation theoretically revealed and classified the EMI filter coupling issue into “Low Frequency Magnetic Field Coupling” and “High Frequency Magnetic Field Coupling” usually observed after the corner frequency in high frequency range. Both of them should be considered in the EMI filter design. For “High Frequency Magnetic Field Coupling”, the magnetic component near field distribution will change dramatically and the reason is caused by the displacement current through

EPC. Since the field distribution changed a lot, the components layout will obviously influence the EMI filter performance which cannot be predicted by the "Low Frequency Magnetic Field Coupling" theory. Improper design may cause the high frequency magnetic field coupling range at low frequency (Even lower than 1MHz).

5.2 Future Work

Based on the research presented in this report, there is still some work that needs to be done in order for this to be complete. Adding those missing parts will make this work more comprehensive and valuable.

(1). Even though the proposed active ripple energy storage circuit can effectively reduce the capacitor size to 25%, more work is still needed in this area. The proposed control method for the auxiliary circuit belongs to the feed forward digital control which requires accurate sensing and system parameters. However, in the real application, the system parameters such as the inductance may change with different Dc current bias and temperature. Therefore, feedback control for the auxiliary circuit is desired to have better utilization of the energy storage capacitor.

(2). The thermal reliability of the proposed high temperature hybrid packaging structure power module can be further improved by better material selection. Although the concept of the high temperature hybrid packaging power module has already been demonstrated in this dissertation, the thermal reliability of the existing version is not as good as we expected. More work need to be conducted to further improve the existing version thermal reliability by better selection the insulation materials.

(3). More functions need to be included in the high temperature gate drive design. Although one edge triggered gate drive topology is proposed in this dissertation and also verified in the phase leg configuration, more functions such as de-sat protection and miller clamping need to be considered for the next version.

(4). A successful insertion gain prediction has been presented in Chapter 4 with a frequency domain equivalent circuit. However, based on the prediction results, how to do better components selection or design is still not clear. Better optimal algorithm is required.

(5). In order to predict the magnetic component near-field stray flux distribution, winding current distribution including displacement current need to be predicted. A better magnetic component winding current distribution model need to be proposed to improve the existing simplified one. Meanwhile, a lot of work needs to be conducted to combine the near-field distribution in the EMI filter design and demonstrate the feasibility of achieving better performance with the consideration of near-field coupling.

(6). High temperature EMI filter could be another interesting topic in the transportation applications.

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Appendix

A. Surveyed High Temperature Passive Components

Table A-1. SURVEY OF HIGH-TEMPERATURE RESISTORS

Material	Vendor	Temperature
Carbon film	KOA Speer Electronics	-55 ~ 200 °C
Ceramic	Ohmite	-40 ~ 220 °C
	KOA Speer Electronics	-40 ~ 200 °C
Metal stripe	Vishay	-65 ~ 275 °C
Metal film	KOA Speer Electronics	-55 ~ 200 °C
	Vishay	-65 ~ 225 °C
Metal Oxide	IRC	-55 ~ 200 °C
Flip chip film	Ohmite	-55 ~ 200 °C
Wirewound	Bourns	-55 ~ 275 °C
	Vishay	-65 ~ 275 °C
Thick film	IRC	-55 ~ 200 °C
	Ohmite	-55 ~ 200 °C

Table A-2 SURVEY OF HIGH-TEMPERATURE CAPACITORS

Materials		Vendor	Capacitance	Temperature
Ceramic	NP0	Kemet Novacap Johanson Dielectric Eurofarad	1.0pF~ 0.12μF	-55~200°C
	X7R		100pF~ 3.3μF	-55~200°C
Teflon		Eurofarad	470pF~2.2 μ F	-55~200°C
Tantalum		Kemet	0.15μF~ 150μF	-55~175°C

Mica	CDE	1.0pF~1500pF	200°C

Table A-3 SURVEY OF HIGH-TEMPERATURE MAGNETICS

Vendor	Series	Inductance range	Temperature range
Vashay	TJ3-HT	0.39 ~ 100 µH	-55 ~ 200 °C
	TJ5-HT	0.47 ~ 470 µH	-55 ~ 200 °C
Datatronic	Dr-360	1.2 ~ 1000 µH	-55 ~ 200 °C
	Dr-361	1.2 ~ 1000 µH	-55 ~ 200 °C
	Dr-362	1.0 ~ 1000 µH	-55 ~ 200 °C
Ferroxcube	4C65		Up to 200°C
	3C93		Up to 200°C

B. Magnetic Field Computation Using Solid Rectangular Conductors.

In order to conduct the stray flux calculation with the Biot-Savart equation, one has to solve the integration over a straight wire beam of finite dimension. The computation presented here is, however, valid for beams directed in any directions. As an assumption, the current densities in conductors are supposed to be constant over the conductor section. To minimize the computation effort, one reports all the conductors at the origin with the homogenous coordinate transformation. By taking θ_y the rotation around the $\vec{y}$ axis and θ_z the rotation around the $\vec{z}$ axis, and T_x, T_y and T_z the translation in $\vec{x}$, $\vec{y}$ and $\vec{z}$ direction, respectively, one obtains the homogenous transformation matrix given by (A-2).

$$T_{n-1}^{n} = \begin{bmatrix} C\theta_y C\theta_z & -C\theta_y S\theta_z & S\theta_y & T_x \\ S\theta_z & C\theta_z & 0 & T_y \\ -C\theta_z S\theta_y & S\theta_y S\theta_z & C\theta_y & T_z \\ 0 & 0 & 0 & 1 \end{bmatrix} \quad \text{(A-2)}$$

Each transformation matrix is constant and can be easily computed. By reporting each segment at the origin with the homogenous transformation (A-2), all the current densities are oriented along the axis, which simplifies the cross product in (A-2)–(A-3)

$$\vec{B} = -\int_V \frac{(p_z - z)J_x}{R^{\frac{3}{2}}}\vec{u}_y dV + \int_V \frac{(p_y - y)J_x}{R^{\frac{3}{2}}}\vec{u}_z dV \tag{A-3}$$

where $R = \sqrt{(p_x - x)^2 + (p_y - y)^2 + (p_z - z)^2}$

By expanding each integral in (3), one obtains the following expressions (A-4) and (A-5) for B_y and B_z, respectively

$$B_y = \sum_{q=1}^{2}\sum_{m=1}^{2}\sum_{n=1}^{2}(-1)^{(m+n+q)}\beta \tag{A-4}$$

where $\beta = -\left|p_z - z_q\right|\arctan\left[\frac{p_x - x_n}{\left|p_z - z_q\right|}\right] - \frac{K_1^3 - K_1K_2}{K_1\left|p_z - z_q\right|}\arctan\left[\frac{K_1(p_x - x_n)}{\left|p_z - z_q\right|\alpha}\right]$
$- (p_x - x_n)\ln(K_1 + \alpha) - K_1\ln(p_x + \alpha - x_n) - x_n$

with $K_1 = (p_y - y_m)$, $K_2 = (p_y - y_m)^2 + (p_z - z_q)^2$ and

$\alpha = \sqrt{(p_x - x_n)^2 + (p_y - y_m)^2 + (p_z - z_q)^2}$

$$B_z = \sum_{q=1}^{2}\sum_{m=1}^{2}\sum_{n=1}^{2}(-1)^{(m+n+q)}\gamma \tag{A-5}$$

where $\gamma = -\left|p_y - y_m\right|\arctan\left[\frac{p_x - z_q}{\left|p_y - y_m\right|}\right] + \frac{W_1^3 - W_1W_2}{W_1\left|p_y - y_m\right|}\arctan\left[\frac{W_1(p_z - z_q)}{\left|p_y - y_m\right|\alpha}\right]$
$+ (p_z - z_q)\ln(W_1 + \alpha) + W_1\ln(p_z + \alpha - z_q) - z_q$

with $W_1 = (p_x - x_n)$, $W_2 = (p_x - x_n)^2 + (p_y - y_m)^2$ and

$\alpha = \sqrt{(p_x - x_n)^2 + (p_y - y_m)^2 + (p_z - z_q)^2}$