

Chapter 2.

State of the art topologies and improvements

2.1 Introduction

In the first chapter, the trends for distributed power system were discussed. High power density, high efficiency and low profile are the key driving forces for technology development for this application. To achieve these targets, high switching frequency and high efficiency power conversion is necessary.

In this chapter, first three state of the art topologies will be evaluated in detail. The issues of these converters will be discussed for this application. For the state of the art topologies, it almost reached the limit along this path with current technology. Switching loss and wide input range put lot of burden on these topologies, which prevented these topologies from increasing switching frequency and reaching higher efficiency.

Several techniques will be developed to improve the state of the art topologies. First two techniques, range winding technique and asymmetrical winding asymmetrical half bridge technique, are developed to deal with wide input range problem caused by hold up requirement.

For this application, with output current around 25A, secondary rectifier conduction loss is the biggest part in the total loss. Quasi Square Wave (QSW) Synchronous Rectifier technique is developed to reduce the secondary rectifier conduction loss.

Range winding solution is a universal solution for wide input range problem. The concept could be implemented to any isolated topologies. For asymmetrical winding solution, it is limited to asymmetrical half bridge converter only. With modified control scheme, it could also be used for full bridge converter. For QSW synchronous rectification, currently it is demonstrate with symmetrical half bridge, it could also be used for phase shift full bridge, asymmetrical winding asymmetrical half bridge and range winding solution. With the fast advance in power MOSFET technology, it could also be extended to asymmetrical half bridge if 300V MOSFET could outperform 300V diodes.

2.2 State of the art topologies and issues

2.2.1 Two-switch-forward converter

The schematic and waveform of two-switch forward (2SF) converter is shown in Figure 2.1 [A9][A10][A11]. The operation of two-switch-forward converter could be divided into three modes: energy transfer stage, transformer reset stage and dead time stage. In energy transfer stage, both primary switches are turned on; energy is transferred from input to output. In transformer-reset stage, two primary diodes will conduct and apply reversed input voltage to the transformer

winding to reset the transformer. When transformer is totally reset, converter will come into dead time stage with no current in the primary side while secondary side is freewheeling.

Two-switch forward got lot of interests and appreciations because of one reason: robust. Since two primary switches are not connected in totem pole configuration, they are turned on at the same time. This solved shoot through problem. For Half Bridge and Full Bridge converter, the primary switches are connected in totem pole structure. Whenever the two switches are turned on at the same time due to electromagnetic noise or radiation, it will be a destructive failure. For two-switch forward, this problem is solved, which is very critical for airspace power supply since they will be exposed to high-energy radiation. But to get this benefit, high price need to be paid.

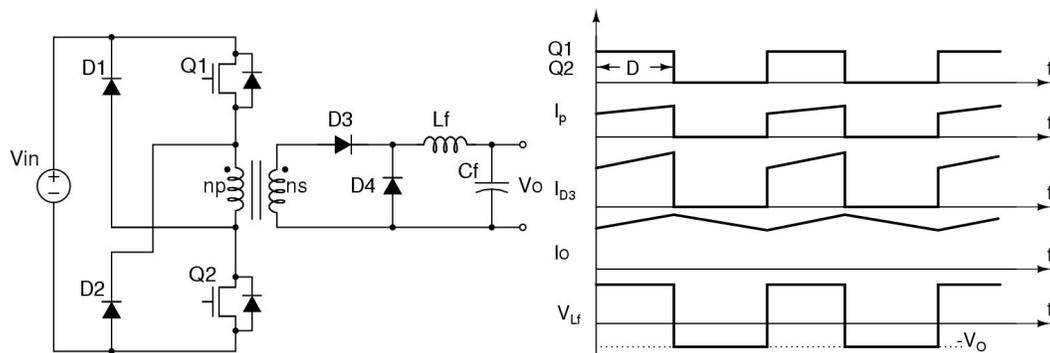


Figure 2.1. Two-switch forward converter and operating waveforms

The major disadvantages of two-switch forward are hard switching and large filter inductor.

Low efficiency is due to several reasons. First, two-switch forward is a hard switching converter; the switches are hard turn-on and turn-off. This will increase the switching loss for high frequency operation. Second, two-switch forward has higher conduction loss compare with half bridge and full bridge converters. This is because the energy transfer only happens during two switches are on. Because of transformer reset requirement, the maximum duty cycle can only reach 0.5. Which means at best, only half of the time this converter can transfer energy to the output; this will increase the RMS current through the primary switch. With same reason, the voltage-second on output inductor is much higher in two-switch-forward converter compared with half bridge and full bridge converter.

Because of these penalties of two-switch forward, it is not so widely used for this application now. For some application requires high reliability applications, it still been considered.

2.2.2 Phase Shift Full Bridge converter

The schematic and operating waveforms of phase shift full bridge converter are shown in Figure 2.2 [A12][A13][A14][A15][A16]. Phase shift full bridge converter, as one of the most popular topology for this application, has many good characteristics. It is a soft switching converter. All four switches on primary side can achieve Zero Voltage Switching (ZVS) with proper design. This is very helpful for high frequency operation. This topology has lower volt-sec on the output filter inductor. Phase shift full bridge can achieve smallest volt-sec for

same design specification compared with two-switch forward and half bridge converter.

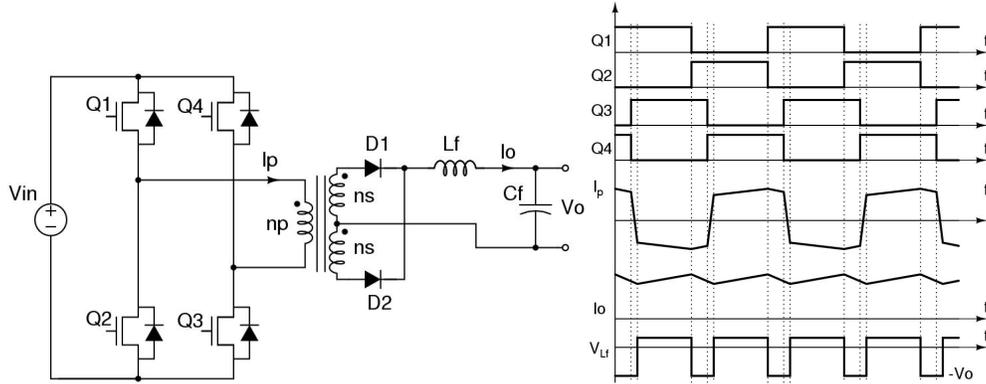


Figure 2.2. Full bridge converter and operating waveforms

Another benefit of phase shift full bridge is its capability to cover wide power range. For power from several hundreds watts to kilowatts, full bridge converter can perform very well. In recent years, even for low power application like Voltage Regulator Module, full bridge topology is been investigated and showed benefits.

There are several disadvantages for phase shift full bridge though. First, it is more complex than the other two topologies. With four switches on primary side, control and driver circuit will be more complex. Another problem is the leakage inductance. To achieve ZVS, large leakage inductance is needed. With large leakage inductance, the duty cycle loss due to charge and discharge leakage inductance will be significant. This will limit the choice of transformer turns ratio, which will affect the performance of whole converter. Even with large leakage inductance, still ZVS cannot be achieved at light load. There are many papers

discussed different methods to expand ZVS region for phase shift full bridge, but they are not widely adopted due to complexity.

Another issue for phase shift full bridge is the circulating current. As seen in the waveforms, during every switching cycle, there is a time interval during which two up switches or low switches are turned on at the same time. This will short the transformer primary side. During this time interval, secondary is freewheeling and no energy transfer from input to output. Primary current during this period is pretty high. This current circulates through the primary two switches and transformer winding. It will increase the conduction loss. Smaller the duty cycle, more circulating current will be.

Although some drawbacks for phase shift full bridge, it is still a popular topology for this application. Its capability to operate at high frequency and wide power range enable it to be used for multi applications.

2.2.3 Half bridge converter

As shown in Figure 2.3, half bridge converter has only two switches on the primary side [A17][A18][A19][A20][A21]. For half bridge converter, with different control signal, the converter operates very differently. The different operating waveforms are shown in Figure 2.4 and Figure 2.5. When the two switches are driven with symmetrical signals, which are identical to each other with 180-degree phase shift, the converter is called symmetrical half bridge. For the one with complementary driving signals, it is called asymmetrical half bridge.

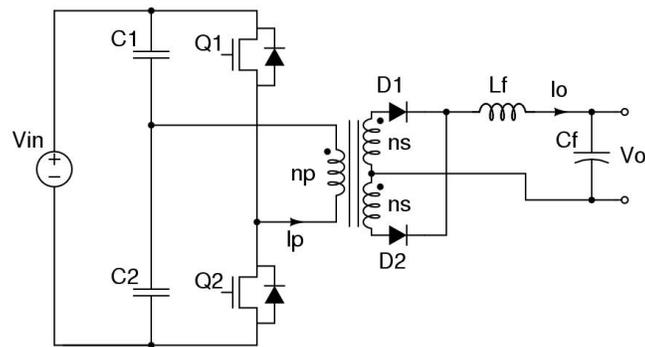
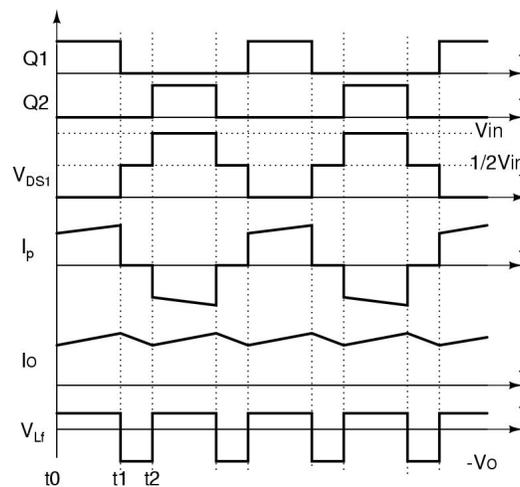


Figure 2.3. Schematic of half bridge converter

For symmetrical half bridge, it is hard switching topology. Leakage inductance is detrimental to the performance of converter. Normally snubber circuit is needed to absorb the ringing problem caused by leakage inductance during the period when both switches are off. For symmetrical half bridge, the power level is limited because of these limitations.

Figure 2.4. Operating waveforms of *symmetrical* half bridge converter

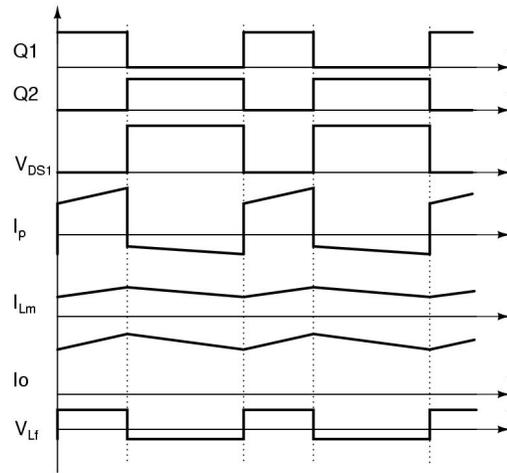


Figure 2.5. Operating waveforms of *asymmetrical* half bridge converter

Asymmetrical half bridge is a very interesting topology. It has some unique characteristics. First, asymmetrical half bridge is a soft switching converter. Primary two switches can achieve ZVS with help of leakage inductance. Since the two switches work complementarily, there is no ringing problem caused by leakage inductance. Also, since energy is transferred from input to output during whole switching period, there is no circulating current as seen in phase shift full bridge.

For asymmetrical half bridge, there are several drawbacks too. One problem is that the voltage stress on the secondary rectifier is asymmetrical and related to duty cycle. In some situations, the voltage stress on the output filter diodes could reach very high, which will limit the choice of diodes. Since asymmetrical half bridge also utilizes leakage inductance to achieve soft switching, there is similar problem as discussed for phase shift full bridge, which is lost of ZVS during light load condition.

For asymmetrical half bridge, the transformer is biased according to different duty cycle. So the design of asymmetrical half bridge transformer need take this into consideration.

Asymmetrical half bridge is very popular for power level less than 1kW application because its simplicity compared with phase shift full bridge.

Current doubler is a topology for secondary rectifier. It is widely used for low voltage, high current applications because of reduced transformer winding loss and easy to implement magnetic integration concept. For front-end DC/DC application, the secondary current can reach 25A. With current doubler and magnetic integration, higher efficiency and higher power density can be achieved.

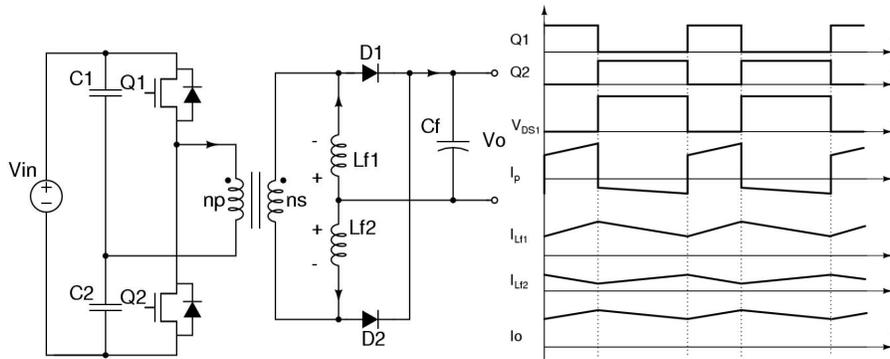


Figure 2.6. Asymmetrical half bridge with current doubler and waveforms

For asymmetrical half bridge with current doubler, its operation is same as traditional asymmetrical half bridge. For current doubler asymmetrical half bridge, since the two inductor L_{f1} and L_{f2} current could be different, the transformer doesn't need to be biased. With current doubler structure, the transformer loss could be reduced.

2.2.4 Comparison of three topologies

Figure 2.7 shows the loss comparison of these topologies for primary switches. Two switch forward and symmetrical half bridge converters have much higher loss compared with full bridge and asymmetrical half bridge converter. Since two-switch forward and symmetrical half bridge converter are hard switching converters, the operating frequency cannot be pushed too high. This will limit the achievable power density.

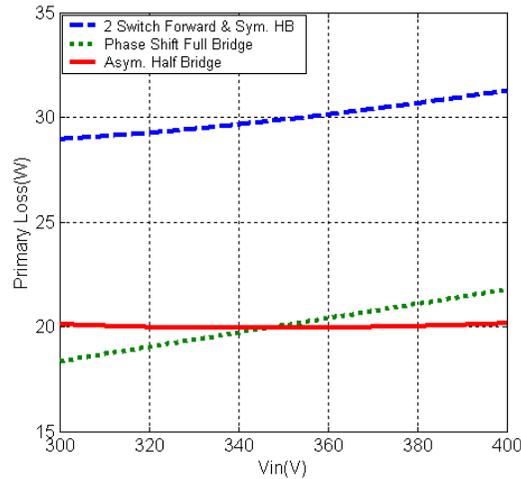


Figure 2.7. Loss comparison of three state of the art topologies

Figure 2.8 shows the comparison of volt-second on output filter inductor for these topologies. For half bridge and full bridge, when duty cycle reaches maximum, the volt-sec on the output filter inductor will be very small, this will reduce the required inductor size if same current ripple is assumed. For two switch forward, however, even with maximum duty cycle, the volt-sec is still very large due to the discontinuous energy transfer property of the converter. As seen

in Figure 2.8, two-switch forward converter has almost 5 times volt-sec on the output filter inductor compared with half bridge and full bridge converter.

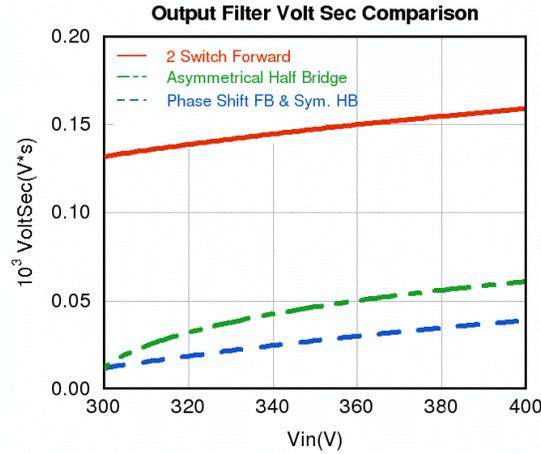


Figure 2.8. Output filter inductor volt-sec comparison of three topologies

From above comparison, two-switch forward and symmetrical half bridge converter are hard switching converters, which are not suitable for high frequency operation. For full bridge converter, and asymmetrical half bridge converters, they both have pros and cons. Full bridge converter could provide some improvement on output filter inductor volt-sec, but high circulating current and complex structure are its drawbacks. Half bridge converter has simple structure, although the volt-second on output filter inductor is a little bit higher than full bridge. In next part, the impact of hold up time on these two converters will be discussed.

2.3 Issue with hold up time requirement

Hold up time requirement is one special requirement for front-end application. It requires the front-end system to provide full power output for one AC line

cycle, which is 20ms ,after the AC line is lost. This hold up time will ensure the digital system to have enough time to respond to power failure.

With 1kW output power and 20ms hold up time requirement, the energy needed to store in the system will be at least 20Joule. Observing the system, there is no much choice but to use intermediate 400V DC bus capacitors as the energy storage component. This is because of several reasons. First, this intermediate bus is highest voltage bus; it is more efficient to put capacitor here to store more energy. Second, this bus voltage is loosely regulated; it can have a large variation. For 48V output, it needs to be tightly regulated, so it is not possible to use energy on the 48V DC bus capacitors.

During hold up time, energy is drawn from the 400V DC bus capacitor. With energy drawn from it, the voltage on these capacitors will drop. After the hold up time, the voltage on the bus capacitor will be much less than normal operating voltage that is 400V. This will be a design trade off to be made. With smaller bus capacitor, this variation will be larger. Although the size of the bus cap can be reduced, the performance of the front-end DC/DC converter will be greatly penalized due to the wide input range. While with big bus capacitor, the performance of front-end DC/DC could be optimized; the size and cost of bus cap will be a penalty.

In Figure 2.9, the relationship between capacitance needed for hold up time and lowest input voltage the bus will drop after hold up time is showed. For 400V

DC bus, 450V electrolytic capacitor is used. For this voltage rated capacitor, 330uF is most cost and volume effective. The choice will be how many 330uF capacitors will be needed.

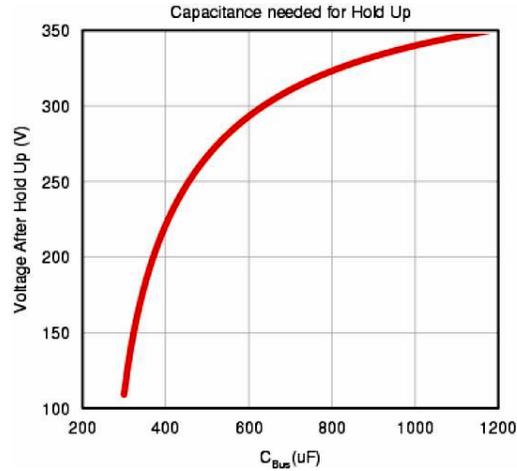


Figure 2.9. Capacitance for hold up time and DC bus voltage after hold up time

Table 2-1 shows the capacitance used and the input voltage range for the front-end DC/DC converter. It is easy to see that 660uF is a good choice, which is also the value used by many industry products.

Table 2-1. Input range of front-end DC/DC converter vs. DC bus capacitance

Bus Capacitance	330u	660u	990u
Voltage Range	160V to 400V	300V to 400V	330V to 400V

With 660uF bus capacitor used, the input voltage range of the front-end DC/DC converter will be 300 to 400V. During the whole lifetime of the converter, it worked with input voltage around 400V. Only in very rare power

failure, the converter will work down to 300V input. The question is how much penalty is paid for 400V input operation in order to operate the converter at 300V input. Next part asymmetrical half bridge and phase shift full bridge will be analyzed on this aspect.

2.3.1 Asymmetrical half bridge with hold up time design

For asymmetrical half bridge, the maximum duty cycle is 0.5. When duty cycle is 0.5, the converter reaches highest gain too. Because of the duty loss due to leakage inductance, the maximum achievable duty will be set to 0.45.

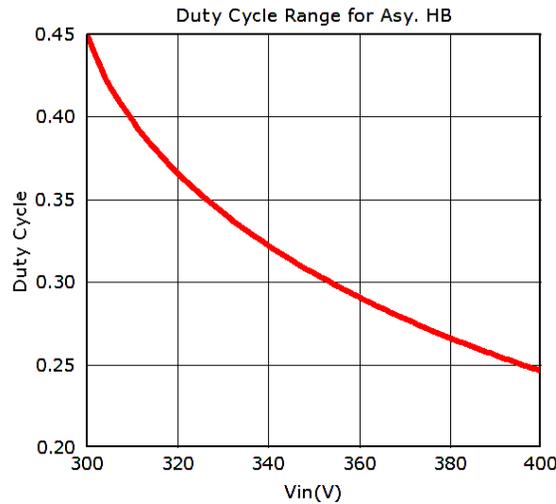


Figure 2.10. Duty cycle range for asymmetrical half bridge with hold up requirement

To cover input voltage from 300V to 400V, the highest gain need to be designed at 300V. With duty cycle equals to 0.45, transformer turns ratio is decided accordingly. When input voltage increase to 400V, duty cycle will reduce to reduce the gain and keep output voltage regulated. The duty cycle will be less than 0.25 when input voltage is 400V as shown in Figure 2.10. From this we can

see, to design with hold up time requirement, the duty cycle of the converter will be very small during normal operation. Next, the impact of small duty cycle at normal operation on the performance will be discussed.

For asymmetrical half bridge shown in Figure 2.6, the secondary side rectifier diodes voltage stress will be related to input voltage and duty cycle as:

$$V_{D1} = \frac{ns}{np} \cdot (1-D) \cdot V_{in} \quad \text{and} \quad V_{D2} = \frac{ns}{np} \cdot D \cdot V_{in} .$$

Average current flow through each diode will be:

$$I_{D1} = (1-D) \cdot I_o \quad \text{and} \quad I_{D2} = D \cdot I_o$$

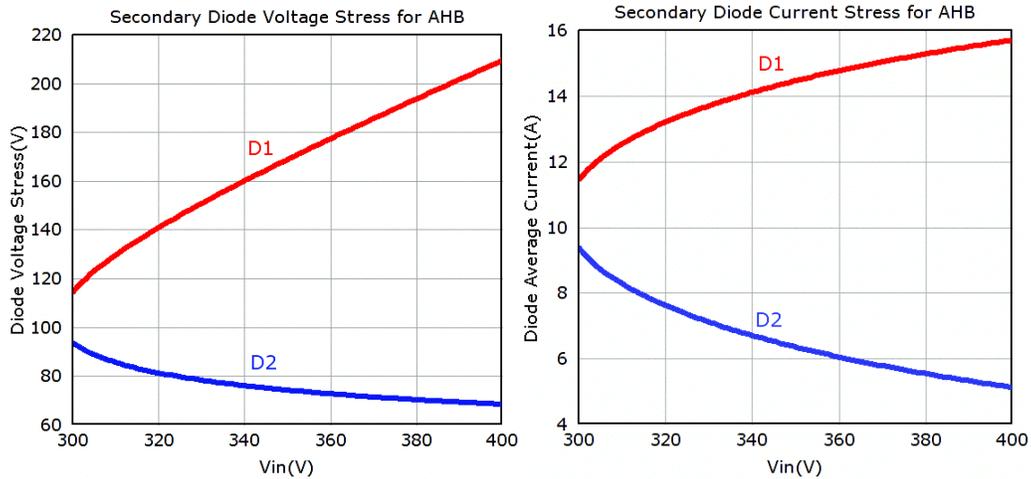


Figure 2.11. Secondary rectifier voltage and current stress for asymmetrical half bridge

As seen from Figure 2.11, when input voltage is 400V, the voltage stress for D1 reaches maximum because of high input voltage and small duty cycle. Also, most of the load current will be carried by D1 too. The maximum voltage is over

210V, so 300V diodes has to be used for the secondary rectifier. The highest voltage rating shottky diode available is 200V. With 300V diodes, the forward voltage drop and reverse recovery characteristic is much worse than 200V shottky diode. This will increase the conduction and switching loss.

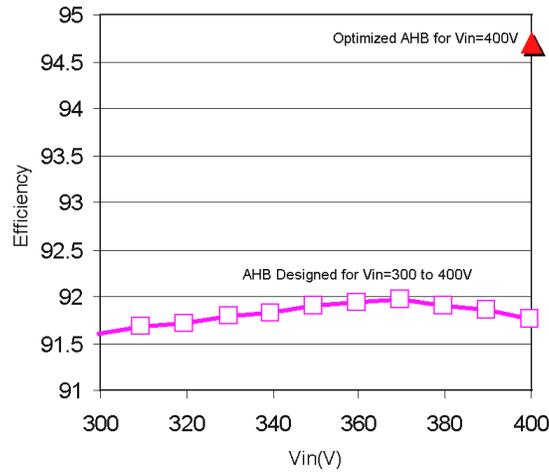


Figure 2.12. Test efficiency of asymmetrical half bridge

Figure 2.12 shows the test efficiency of asymmetrical half bridge for two cases. In first case, the converter is designed just to operate from 360V to 400V. In the other case, the converter is designed according to hold up time requirement with 300V to 400V input range. The differences between these two designs are shown in Table 2-2.

Table 2-2 Difference between two asymmetrical half bridge design

	Input Range	Xfmer turns ratio	Secondary diode	Primary Switch	Switching Frequency
Case 1	360-400V	10:6	MUR2002 200V Shottky Diode	IXFH22N50 500V 20A	200kHz
Case 2	300-400V	10:7	STTH3003 300V Fast recovery diode	IXFH22N50 500V 20A	200kHz

From test results we can see, because of this wide input range, efficiency at 400V drops more than 3%, which means more than 60% increase in loss because of wide input voltage range.

2.3.2 Phase shift full bridge with hold up time design

For phase shift full bridge, with hold up time requirement, its duty cycle range is shown in Figure 2.13. When input voltage drops to 300V, duty cycle reaches the maximum. When input voltage is 400V, duty cycle is only around 0.34.

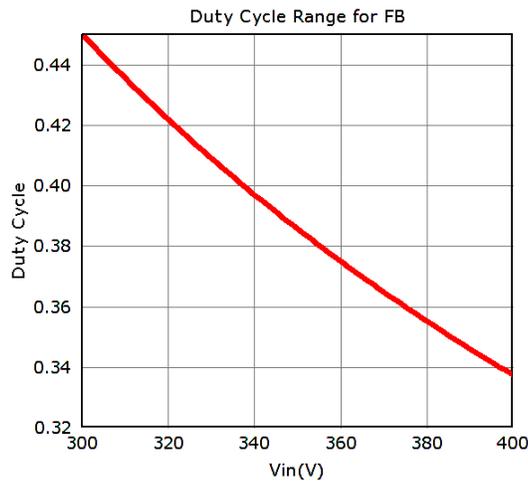


Figure 2.13. Duty cycle range for full bridge converter with hold up requirement

For phase shift full bridge, the secondary rectifier voltage stress is not a big concern. The major problem is the high circulating current during normal operation. As seen in Figure 2.14, during each switching cycle, there is a free wheeling period. Secondary current freewheels through secondary diodes in this time interval. Primary also has high current circulating through primary two switches. This primary circulating current will increase conduction loss and

should be minimized to achieve high efficiency. Unfortunately, to design for hold up time, the duty cycle at 400V is very small, less than 0.35. This means during each switching cycle, the current circulating for almost one third of the time.

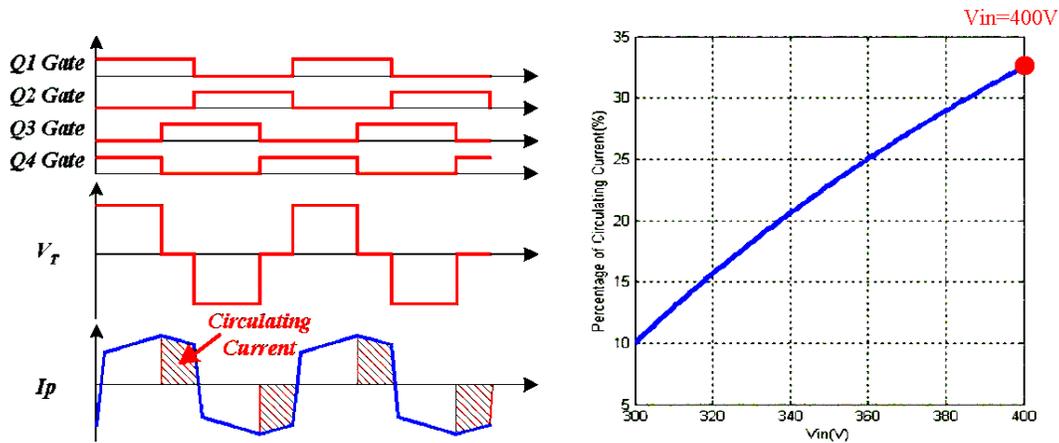


Figure 2.14. Circulating current of full bridge with different input voltage

2.3.3 Conclusion

From above analysis, following conclusion could be drawn:

1. For front-end DC/DC application, to design for hold up time, its input voltage range will be wide. With 660uF bus capacitor, the input voltage of front-end DC/DC converter will be 300 to 400V.
2. For phase shift full bridge, to design for this specification, more than one third of the primary current is circulating without transfer energy.
3. For asymmetrical half bridge, the secondary rectifier voltage stress will increase to very high due to wide input range requirement.
4. From test results, it can be seen that more than 60% loss increase will occur because of wide input range requirement.

A desired front-end DC/DC converter should have following characteristic:

- Could be optimized at high input voltage while still cover wide input range
- High efficiency and high switching frequency, so that high power density and low profile could be achieved with high switching frequency.

2.4 Range winding for wide input range

As discussed in the previous part, to deal with hold up time requirement, front end DC/DC converter need to cover wide input range. Within the input range, the converter will work at high input voltage for the whole lifetime. Only during 20ms hold up time, the converter will operate at low input voltage down to 300V. The performance at high input voltage is critical to system while the performance at hold up time is not a consideration as long as the converter still functional. Unfortunately, the PWM converter is working at better condition with low input voltage. As input voltage increases, duty cycle will reduce and the converter is working in worse condition. To design for wide input range, the efficiency at high input voltage will drop significantly. As shown in first chapter, with wide input range design, the efficiency at high input voltage is around 92%. If the converter is designed just for a narrow input range, the efficiency can reach 95%.

Range winding solution is a method to deal with this problem. The concept of range winding solution is to change the transformer turns ratio according to different input voltage so that the transformer could be optimized for high input

voltage. In the following part, asymmetrical half bridge with range winding will be discussed as an example to demonstrate the operation of range winding concept.

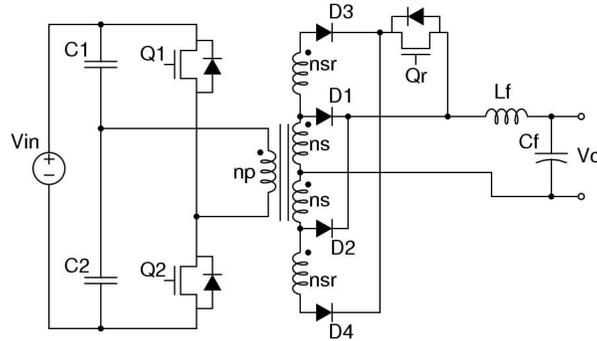


Figure 2.15. Asymmetrical half bridge converter with range winding

As shown in Figure 2.15, range-winding solution is built upon original asymmetrical half bridge converter by adding extra windings, diodes and switch. By adding those extra components, another freedom is added to the converter. With turn on or off the range switch Q_r , the transformer winding turns ratio could be changed. In this way, the gain of the converter could be regulated through two ways, duty cycle and range switch.

When range switch Q_r is turned off, the converter will have a gain:

$$V_o = \frac{V_{in} \cdot (1-D) \cdot D \cdot n_s}{n_p}, \text{ Which is same as an asymmetrical half bridge with}$$

transformer turns ratio $n_p: n_s$.

With the range switch turned on, the range winding will be added to the secondary, the converter will have a different gain:

$$V_o = \frac{V_{in} \cdot (1-D) \cdot D \cdot (n_s + n_{sr})}{n_p}$$

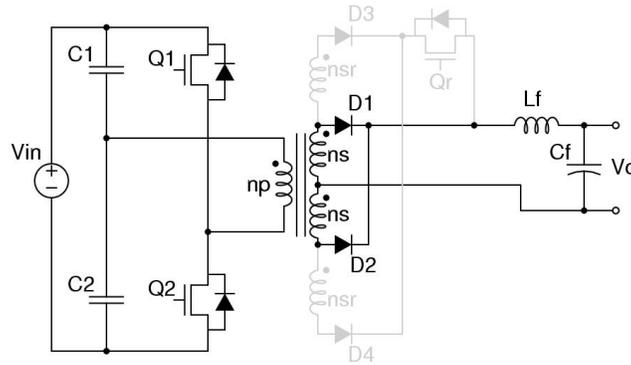


Figure 2.16 Circuit diagram for normal operation

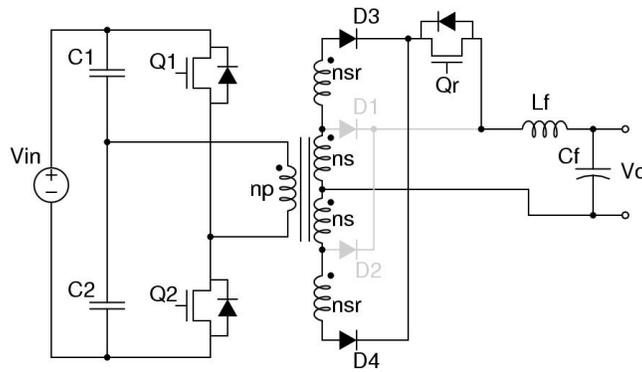


Figure 2.17 Circuit diagram for hold up operation

As shown in those equations, with range winding turned on, the transformer turns ratio will be reduced. The converter will have higher gain with lower turns ratio. By detect the input voltage of front end DC/DC converter, when it drops below given level, the range switch will be turned on, and the converter will have higher gain to cover lower input voltage. During normal operation, the range switch is turned off, the range winding and diodes will not affect the operation.

With range winding solution, the inner transformer turns ratio ($n_p:n_s$) could be optimized for high input voltage so that the converter will operate with large duty cycle at normal operation. At hold up time, the range switch will be turned on to increase the gain to cover wider input range.

To demonstrate the benefits of this solution, design examples of traditional asymmetrical half bridge and asymmetrical half bridge with range winding are performed and compared through analysis and experiments.

For a traditional asymmetrical half bridge, to design for input voltage range from 300V to 400V, the transformer turns ratio is choose to be 10:7 ($n_p:n_s$). With this turns ration, the duty cycle at 300V will be 0.45. The maximum duty cycle is set to 0.45 considering the duty loss caused by leakage inductance for soft switching. When input voltage is 400V, duty cycle is less than 0.25.

For asymmetrical half bridge with range winding, the transformer turns ratio ($n_p:n_s$) is designed to be 10:6. The range winding n_{sr} is just one turn. With turn ratio 10:6, the converter will be able to cover a input range from 360V to 400V. At 400V, the duty cycle is 0.34. When input voltage drops to below 360V, range switch will turn on and the converter will have same gain characteristic as traditional asymmetrical half bridge with turns ratio of 10:7. Next the effect of range winding will be explored.

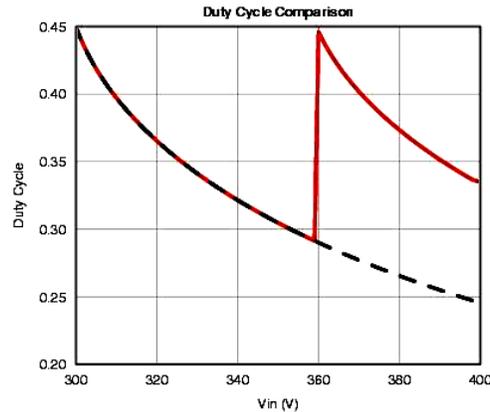


Figure 2.18 Duty cycle range comparison of asymmetrical half bridge with/without range switch

In Figure 2.18, the duty cycle of two converters at different input voltage are compared. For traditional asymmetrical half bridge, the duty cycle at 400V is less than 0.25. With range winding, the duty cycle is extended to 0.34, which is about 40% improvement over traditional asymmetrical half bridge. With extended duty cycle, the stress on all components will be changed.

First, as shown in Figure 2.19, the voltage stress on the rectifier diodes is reduced with range winding solution. Without range winding, the voltage stress on the rectifier diodes is more than 210V, normally 300V diode has to be used. For range winding solution, the voltage stress on the range winding is reduced to 160V; 200V shottky diode can be used. With shottky diode, forward voltage drop and reverse recovery loss are reduced significantly. For traditional asymmetrical half bridge, the secondary conduction loss is around 25W at full load condition. For range winding asymmetrical half bridge, the secondary conduction loss is reduced to 17W with shottky diodes. In traditional asymmetrical half bridge, the diode reverse recovery problem is very severe, snubber circuits have to be added

to reduce the ringing caused by reverse recovery current. With shottky diodes, the reverse recovery problem could be eliminated and snubber could be eliminated. This will improved the efficiency at high switching frequency. As shown in Figure 2.20, the current stress on the two rectifier diodes are also more balanced during normal operation condition, which is beneficial for thermal design.

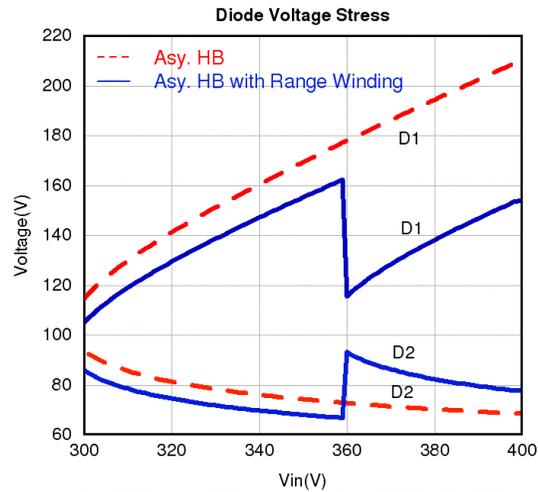


Figure 2.19 Diode voltage stress comparison

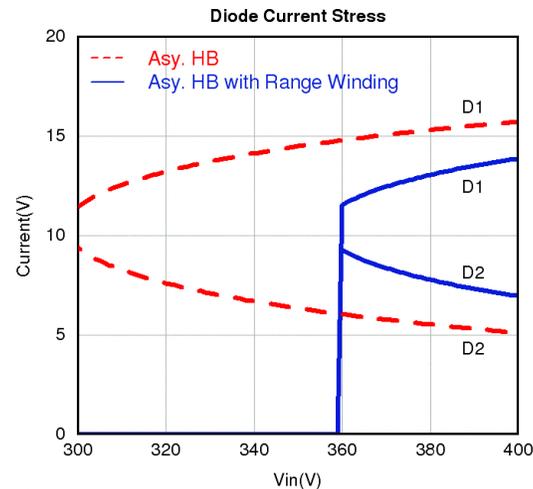


Figure 2.20 Diode average current comparison

Another benefit comes from the decreasing of primary RMS current and turn off current with extended duty cycle. As shown in Figure 2.21 and Figure 2.22, the RMS current and turn off current of the primary switches are reduced with range switching solution. With reduced RMS current, primary conduction loss could be reduced. With reduced turn off current, switching loss could also be reduced.

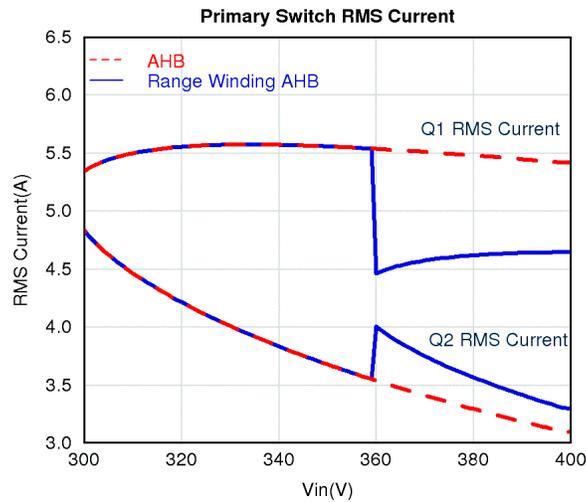


Figure 2.21 Primary switch RMS current comparison

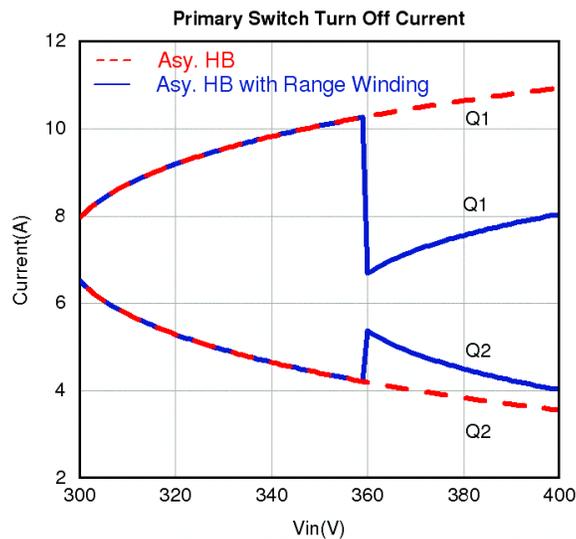


Figure 2.22 Primary switch turn off current comparison

Test circuits were built for these two cases. In Figure 2.24, the test efficiency for both converters is shown at normal operation condition.

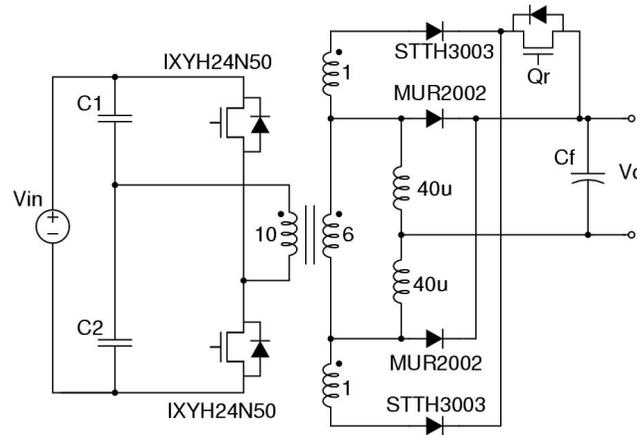


Figure 2.23 Test setup for range winding asymmetrical half bridge

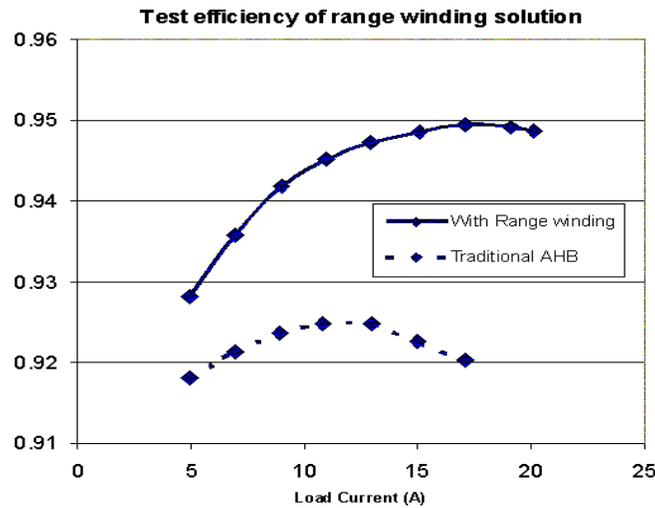


Figure 2.24 Test efficiency at normal operation for range winding solution

From the test efficiency result, it can be seen that range winding can improve the efficiency at normal operation condition significantly. The drawback is extra winding on the transformer and several extra devices.

Range winding concept could also be extended to other topologies like full bridge, and current doubler structure as shown in Figure 2.25.

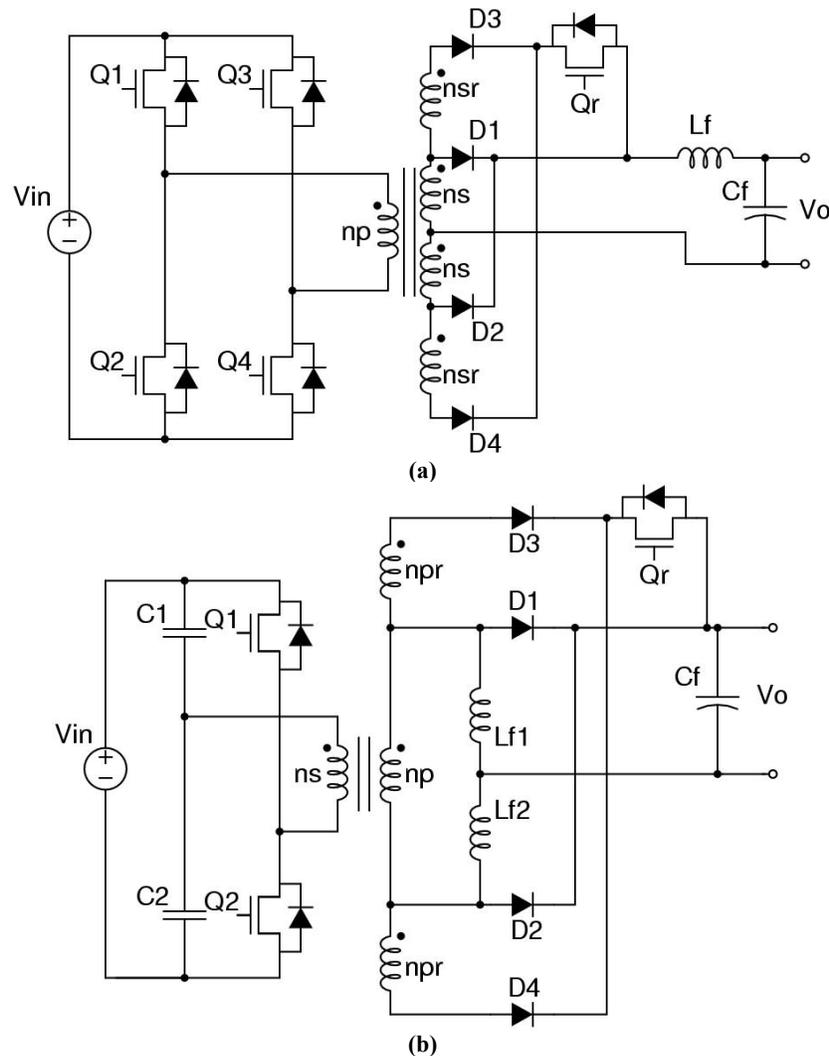


Figure 2.25 Range winding for (a) Full bridge (b) current doubler

2.5 Asymmetrical Winding Asymmetrical Half Bridge

With range winding solution, the performance of front end DC/DC converter could be improved significantly at high input voltage condition. This method could be extended to other isolated DC/DC topologies. The drawback of range

winding solution is that extra windings, diodes, switch and control circuit are needed, which makes this solution very complex. For asymmetrical half bridge with current doubler, another simpler yet effective solution is possible: asymmetrical winding asymmetrical half bridge.

For asymmetrical half bridge with current doubler, it has one transformer and two inductors as shown in Figure 2.26. This topology could be transformed into a two-transformer version with same operation and characteristic. The transform is demonstrated in Figure 2.27. Each step of the transformation is reversible, so these two topologies are exactly the same when the two transformers have same turns ratio as the single transformer.

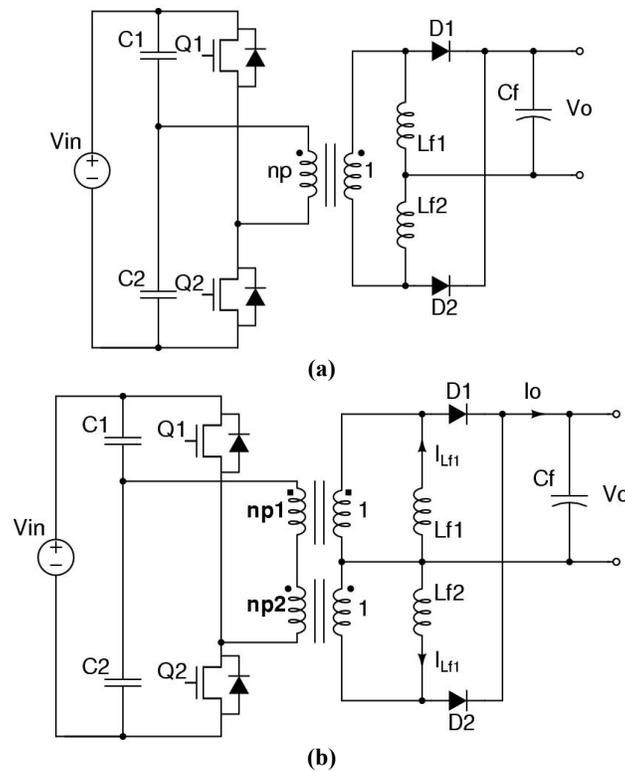


Figure 2.26 Half bridge current doubler with (a) one transformer and (b) Two transformers

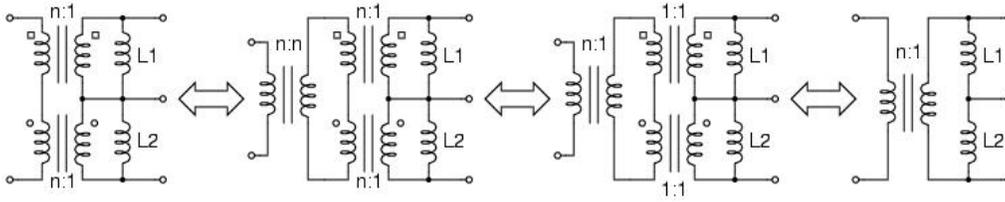


Figure 2.27 Topology transformation of current doubler

With two transformers, another dimension of freedom is provided to the designer. With different turns ratio for these two transformers, some interesting phenomenon could be observed.

For traditional asymmetrical half bridge, the equation for duty cycle in relationship with input, output voltage and turns ratio is:

$$V_o = \frac{V_{in} \cdot (1-D) \cdot D}{n_p}$$

For two-transformer asymmetrical half bridge, the duty cycle will be:

$$V_o = \frac{V_{in} \cdot (1-D) \cdot D}{n_{p1} \cdot D + n_{p2} \cdot (1-D)}$$

These equations are drawn in Figure 2.28. When the two transformers have same turns ratio, maximum gain is achieved at duty cycle equals to 0.5. This is same characteristic for one transformer asymmetrical half bridge. When the two transformers have different turns ratio, the maximum gain will be shifted from duty cycle equals to 0.5. When n_{p1} is larger than n_{p2} , the maximum gain will

shift to smaller duty cycle. When $np1$ is smaller $np2$, the maximum gain will shift to larger duty cycle.

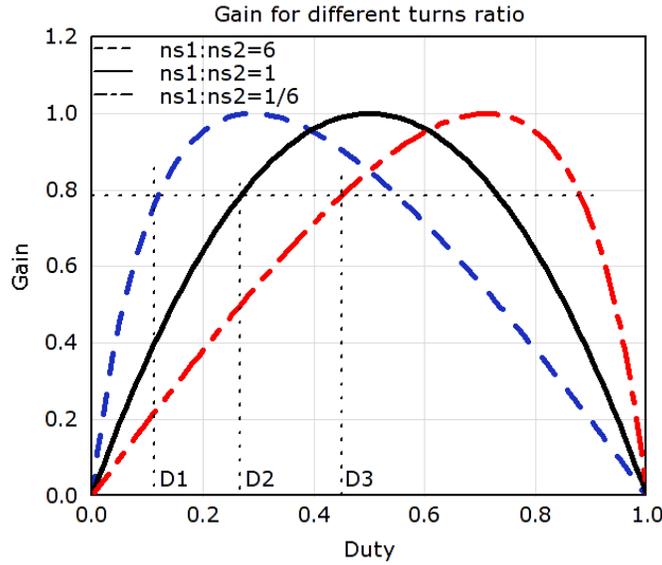


Figure 2.28 DC characteristic for different np ratio

The design goal for front end DC/DC converter is to optimize the performance at high input voltage. To achieve this goal, we would like to extend the duty cycle at high input voltage. From this prospective, $np1$ smaller than $np2$ is preferred. With $np1$ smaller than $np2$, the maximum gain will shift to duty cycle larger than 0.5 and the DC characteristic will tilt toward right. With this effect, the duty cycle at high input voltage will be extended too.

The duty cycle for the single transformer asymmetrical half bridge is:

$$D = \frac{V_{in} - \sqrt{V_{in}^2 - 4 \cdot V_{in} \cdot V_o \cdot np}}{2 \cdot V_{in}}$$

The duty cycle for two transformers asymmetrical half bridge is:

$$D = \frac{V_{in} + V_o \cdot (np2 - np1) - \sqrt{V_{in}^2 + V_o^2 \cdot (np2 - np1)^2 - 2 \cdot V_{in} \cdot V_o \cdot (np1 + np2)}}{2 \cdot V_{in}}$$

In Figure 2.29 duty cycle range for different np1 to np2 ratio are shown. With smaller np1 to np2 ratio, the duty cycle at 400V could be shifted closer to 0.5. Now the question is what ratio of np1 to np2 should be chosen. To answer this question, the impacts of different np1 to np2 ratio need to be investigated. In the following part, the secondary diode voltage stress, current stress, output current ripple and inductor current will be analyzed.

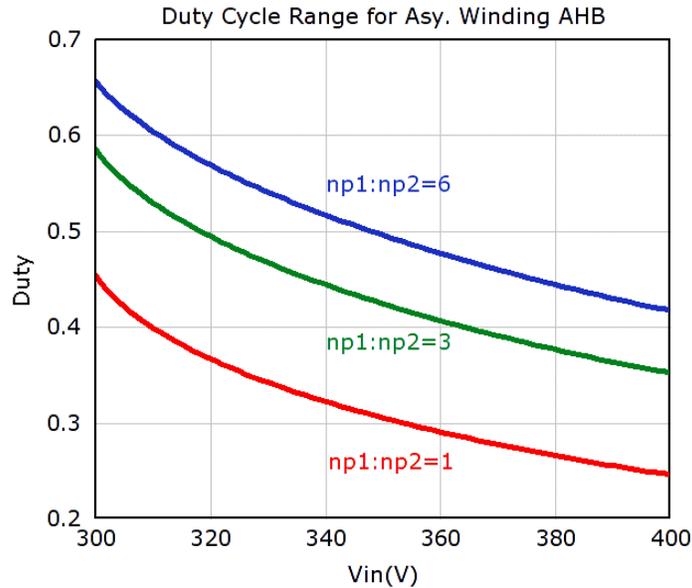


Figure 2.29 Duty cycle range with different turn ratios

For asymmetrical half bridge, because of the high voltage stress on the rectifier diode, high voltage rating diodes have to be used. This increases the conduction loss and switching loss of secondary rectifier significantly. In fact, the

secondary rectifier contributes almost half of the total loss. If the voltage stress of secondary diodes could be reduced so that lower voltage diodes could be used, the efficiency could be improved significantly.

For two transformer asymmetrical winding asymmetrical half bridge, the voltage stresses of the secondary diodes are:

$$V_{D1} = \frac{D \cdot V_{in}}{np1} + V_o \cdot \left(1 - \frac{np2}{np1}\right)$$

$$V_{D2} = \frac{(1-D) \cdot V_{in}}{np2} + V_o \cdot \left(1 - \frac{np1}{np2}\right)$$

In these equations, when $np1$ equals to $np2$ is used, it will be the voltage stress for traditional asymmetrical half bridge. Next the current of the two current doubler inductors will be analyzed. From the charge balance for the primary DC blocking capacitor, the current of two output inductors could be derived as:

$$I_{L1} = \frac{D \cdot I_o \cdot np1}{D \cdot np1 + (1-D) \cdot np2}$$

$$I_{L2} = \frac{(1-D) \cdot I_o \cdot np2}{D \cdot np1 + (1-D) \cdot np2}$$

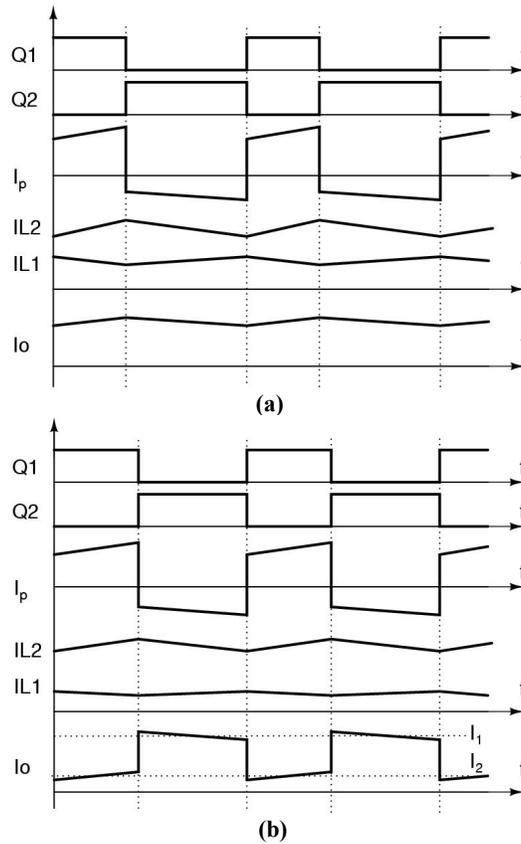


Figure 2.30 Operation waveforms of (a) asymmetrical half bridge and (b) asymmetrical winding asymmetrical half bridge

$$I_1 = I_{L2} + \frac{np1}{np2} I_{L1}$$

$$I_2 = I_{L1} + \frac{np2}{np1} I_{L2}$$

Above I_1 and I_2 is also the current stress on the two output diodes. It can be seen that the two diodes have very different current stress. One diode will see very high current while the other one only pass through very small current.

Above equations are drawn in Figure 2.31 to Figure 2.33.

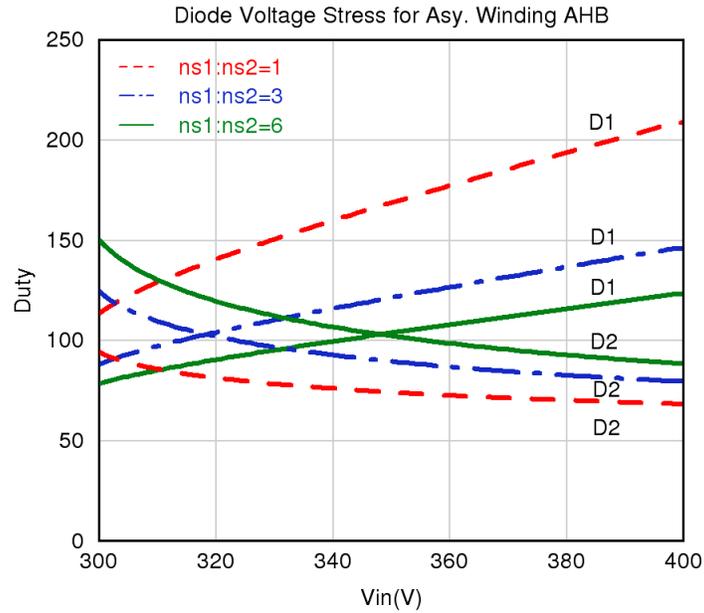


Figure 2.31 Diode voltage stress for asymmetrical winding asymmetrical half bridge

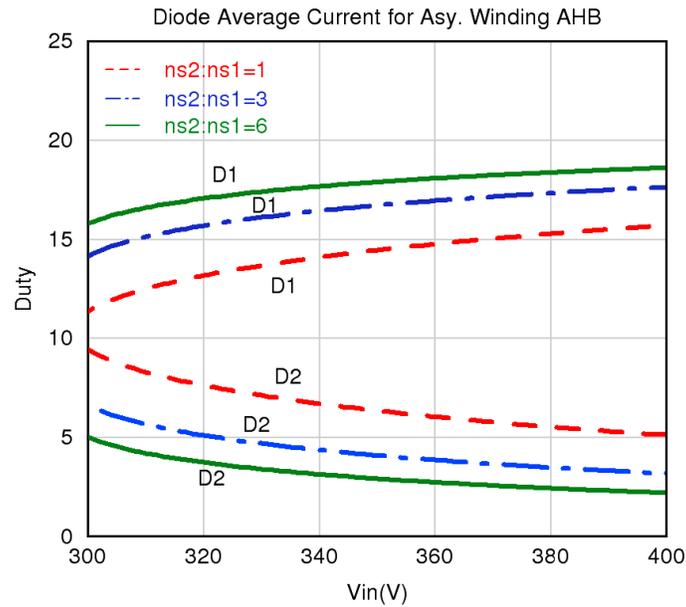


Figure 2.32 Diode current stress for asymmetrical winding asymmetrical half bridge

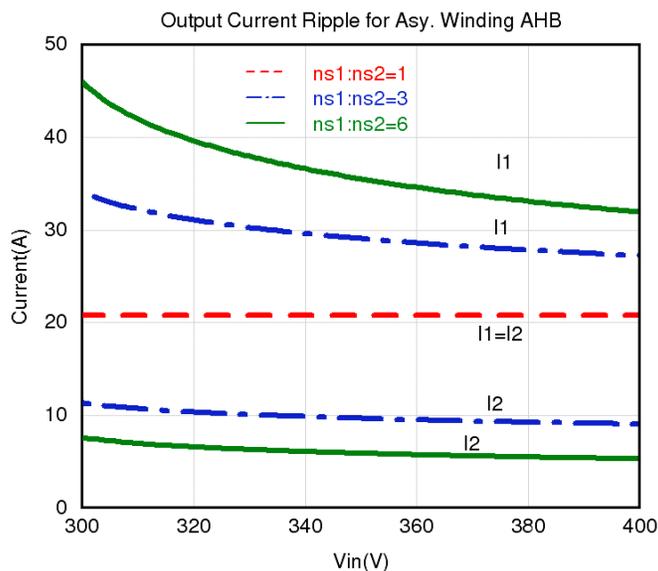


Figure 2.33 Output current ripple for asymmetrical winding asymmetrical half bridge

From above analysis, we can see that the voltage stress on the output diodes is reduced with asymmetrical winding solution. The penalty is the discontinuous output current and unbalanced current stress on the output diodes. This unbalance will also show in the power transfer ratio of the two transformers.

By balancing all these aspects, n_{p1} to n_{p2} ratio of 1:3 is chosen. With this ratio, the voltage stress of two diodes could be limited below 150V so that 200V shottky diodes could be used.

Figure 2.34 to Figure 2.36 shows the test circuit, test waveform and efficiency. From the test result, efficiency could be improved by 1.5% with this solution. The performance improvement of this solution is not as good as range winding solution, but because of its simplicity, it is a good solution for asymmetrical half bridge converter.

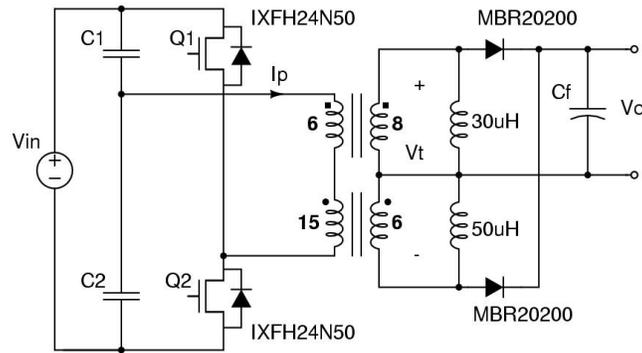


Figure 2.34 Test circuit diagram of asymmetrical winding asymmetrical half bridge

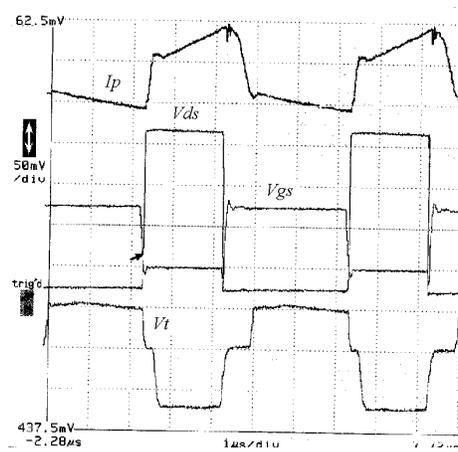


Figure 2.35 Test waveforms of asymmetrical winding asymmetrical half bridge

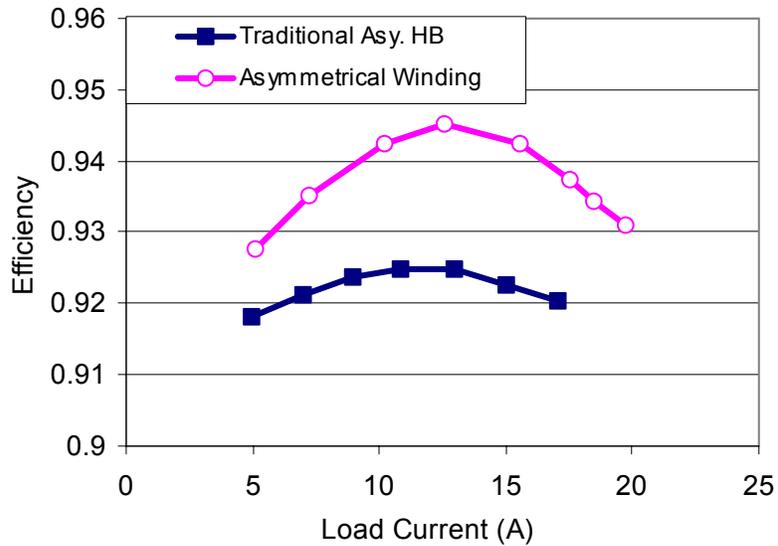


Figure 2.36 Test efficiency of asymmetrical winding asymmetrical half bridge

2.6 QSW Synchronous Rectification

2.6.1 Synchronous Rectifier for front end DC/DC Converter

In low voltage, high current application, secondary rectifier conduction loss is dominant in total system loss. With advanced power MOSFET technology, the conduction loss of a MOSFET is much less than diodes. Synchronous rectifier has been a must technology for low voltage, high current application. For front end DC/DC application, output current is higher than 20A. With diode rectifier, the conduction loss is a big part in total converter loss too. For example, with 300V diode in asymmetrical half bridge, the conduction loss of secondary diodes is about 25W, which is more than 30% of total loss. In this part, the synchronous rectification for this application will be discussed.

For front end DC/DC application, the voltage stress on the rectifier diodes is much higher than low voltage application. To verify the viability of synchronous rectification in front end DC/DC application, conduction loss for different devices will be compared first. For front end DC/DC converter, output voltage is 48V. The voltage stress for secondary diodes is shown in Figure 2.37. For asymmetrical half bridge, voltage stress on the diodes is higher than symmetrical half bridge and full bridge. With a safe margin, the device chosen for asymmetrical half bridge are 300V devices while for range winding, asymmetrical winding, symmetrical half bridge and full bridge, 200V devices could be used. Searching the available devices, following devices are been used for comparison:

300V diode: STTH3003 from IXYS, $V_f=1.2V$ with $trr=40ns$.

300V MOSFET: MTW32N25E from On-Semi, $R_{dson}=80mohm$.

200V diode: MUR202000, shottky diode with $V_f=0.9V$.

200V MOSFET: MTY55N20E from On-Semi,, $R_{dson}=28mohm$.

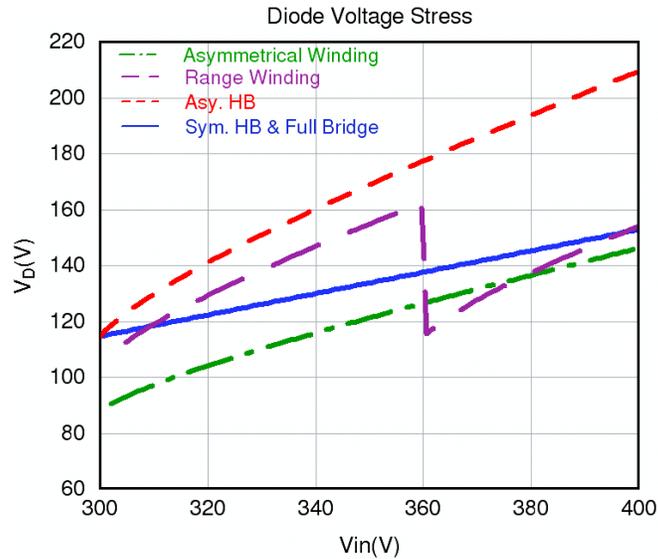


Figure 2.37 Rectifier diode voltage stress of different topologies

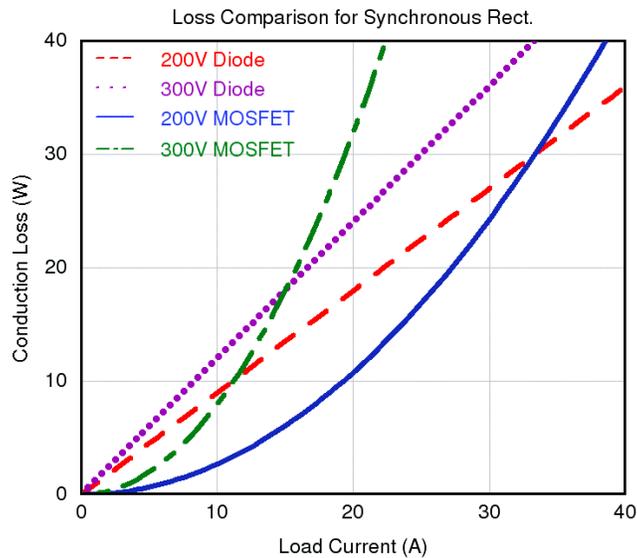


Figure 2.38 Conduction loss comparison of different devices

Figure 2.38 shows the conduction loss for different devices with load change. As seen in the graph, 200V MOSFET could provide much improved performance with current in 20A range over 200V diode. For 300V devices, single MOSFET cannot provide much different, only with more MOSFET in parallel so that the conduction loss can be reduced. It doesn't make much sense to parallel two or more MOSFET here since the thermal is manageable with only one device. To get improved performance with same amount of devices, 200V will be more meaningful. With voltage stress shown in Figure 2.37, it can be seen that asymmetrical half bridge will not get much benefit from synchronous rectification. For asymmetrical winding asymmetrical half bridge, range winding, full bridge and symmetrical half bridge converter, 200V devices could be used. In these topologies, synchronous rectifier might be beneficial.

For range winding solution, with synchronous rectifier, the converter will become very complex. Also the improvement will be limited since performance of 200V diode is not so bad.

For asymmetrical winding asymmetrical half bridge, it is possible to use synchronous rectifier. The problem is the unbalanced current stress on the two rectifier diodes. As shown in Figure 2.39, two rectifier diodes see very different current stress. Without parallel devices, synchronous rectifier will not show much improvement over one diode. With two 200V MOSFET parallel as one

synchronous rectifier, it is possible to reduce the conduction loss with the price of more devices as shown in Figure 2.40.

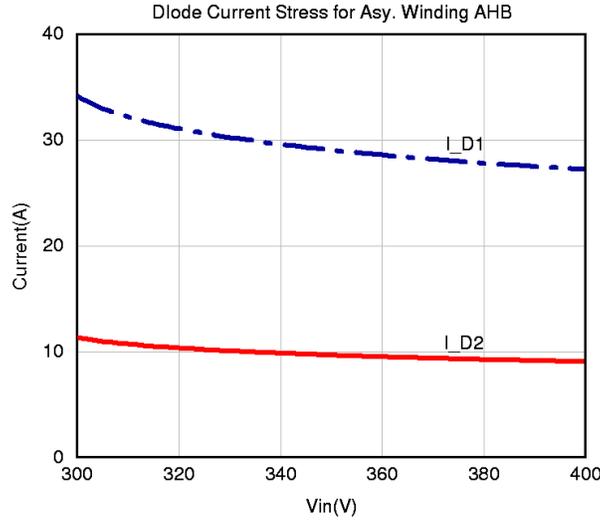


Figure 2.39 Rectifier diodes current stress for asymmetrical winding asymmetrical half bridge

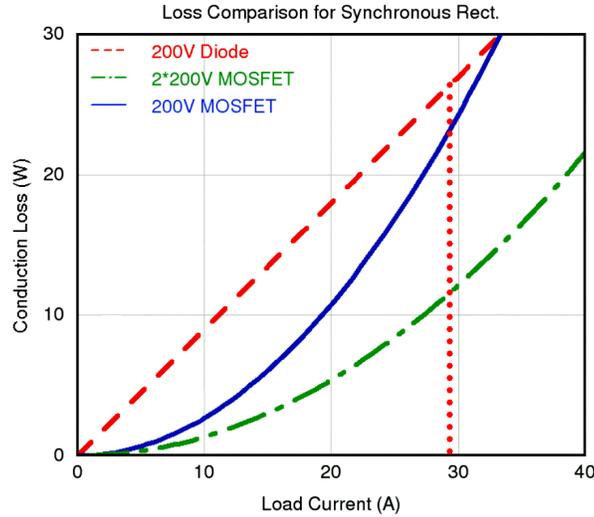


Figure 2.40 Conduction loss comparison of 200V diode and MOSFET

For symmetrical half bridge and full bridge converter, they will be good candidates to demonstrate the benefits of synchronous rectifier. In this part, symmetrical half bridge will be used to demonstrate this technique as shown in

Figure 2.41. All the method discussed here could be used for full bridge converter.

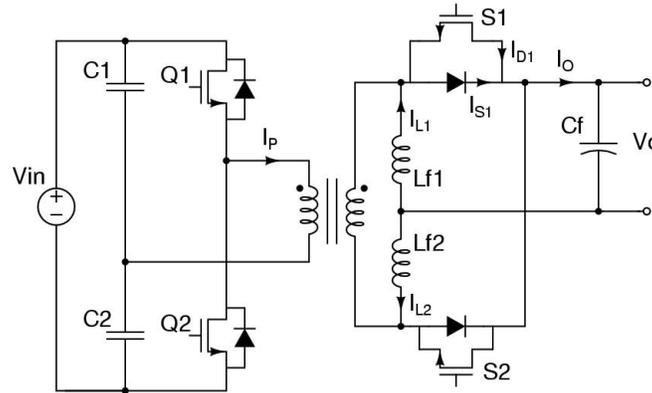


Figure 2.41 Circuit diagram of half bridge current doubler with synchronous rectifier

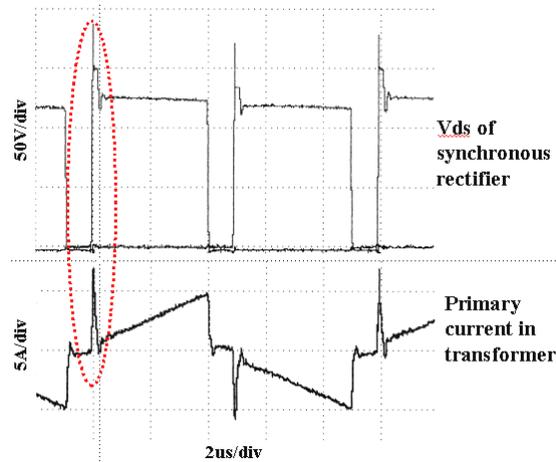


Figure 2.42 Test waveform of synchronous rectifier for front end converter'

Figure 2.42 shows the test waveform for symmetrical half bridge with synchronous rectifier. From the waveform, a huge current spike and voltage ringing could be observed. All these spikes are caused by the reverse recovery of body diodes of synchronous rectifier as shown in Figure 2.43

The two synchronous rectifiers are working complementary with primary switches. Before Q2 is turned on, S1 has to be turned off first; otherwise a short circuit will exist. To guarantee the safe operation, a dead time is inserted between turning on of Q2 at t_3 and turning off of S1 at t_2 . During the dead time, synchronous rectifier S1 is turned off. The current will flow through the body diode of synchronous rectifier S1. When Q2 is turned on at t_3 , the body diode of S1 will be forced turn off. Since the body diode of MOSFET is very slow, a huge reverse recovery current will appear. This reverse recovery current will also cause voltage ringing on the synchronous rectifier.

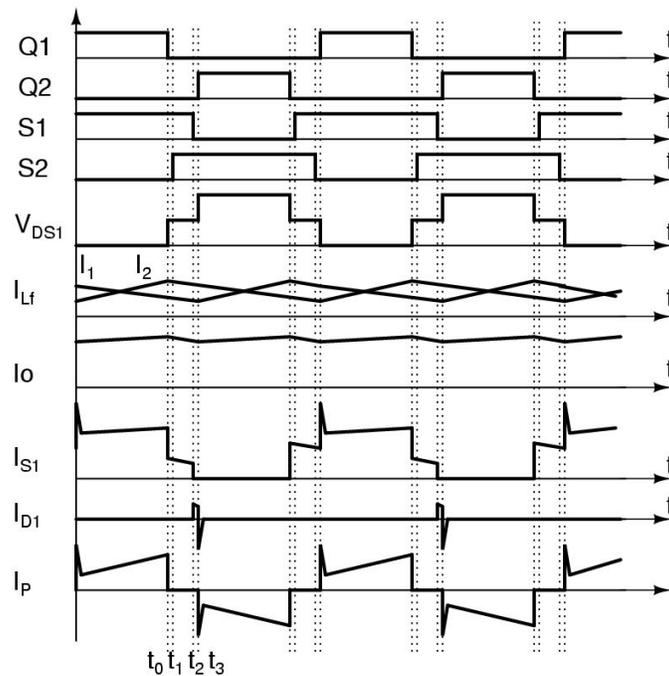


Figure 2.43 Operation waveform of synchronous rectifier for front-end converter

With the problem identified, the solution will be a method, which could prevent the conduction of the body diode of synchronous rectifier. Quasi Square

Wave (QSW) synchronous rectification is proposed to solve this problem. The concept of QSW synchronous rectification is shown in Figure 2.44.

2.6.2 QSW Synchronous Rectifier

The idea is by reducing the filter inductor, the ripple current of each inductor will increase, at some point, the ripple will be large enough so that the direction of the current will change during each switching cycle. As seen in the graph, if the inductor current goes to negative, at time t_2 when the synchronous rectifier S1 is turned off, the current is flowing through drain to source. This current cannot go through the body diode. So when synchronous rectifier is turned off, the body diode will not conduct. This way, the conduction of body diode is prevented.

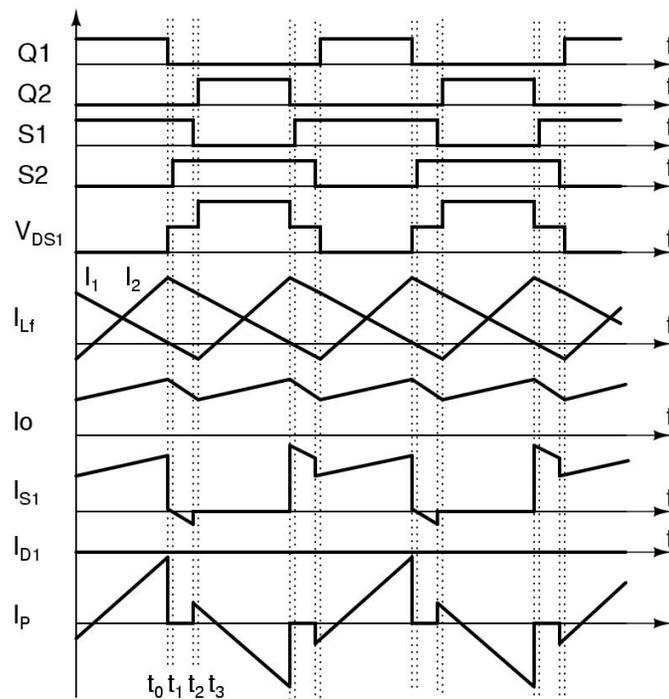


Figure 2.44 Operation waveform of QSW synchronous rectifier

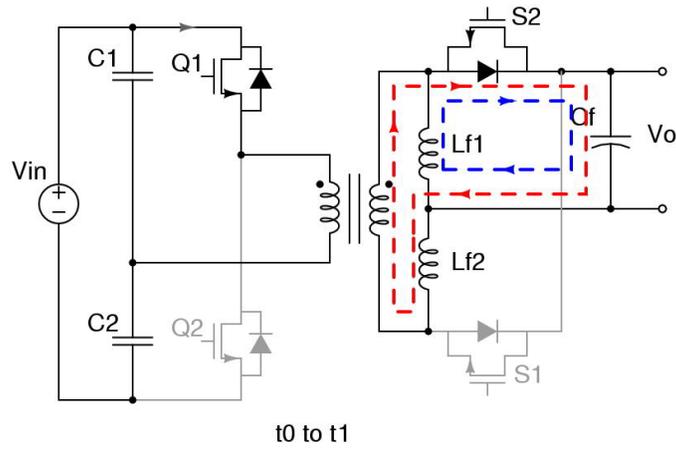


Figure 2.45 Operating mode 1 of half bridge with synchronous rectifier

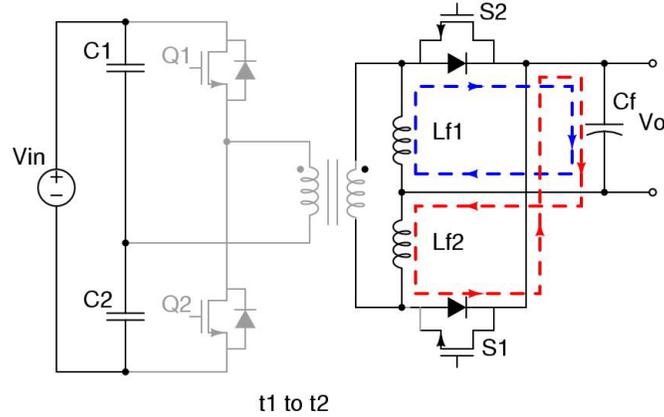


Figure 2.46 Operating mode 2 of half bridge with synchronous rectifier

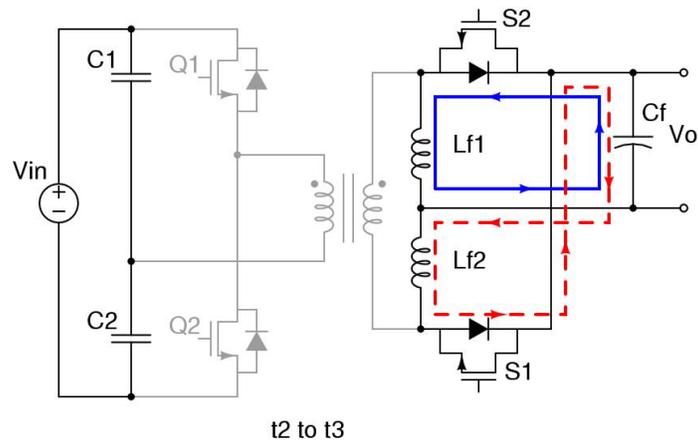


Figure 2.47 Operating mode 3 of half bridge with synchronous rectifier

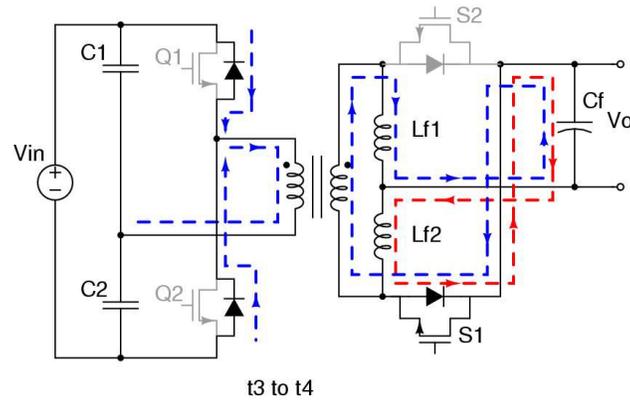


Figure 2.48 Operating mode 4 of half bridge with synchronous rectifier

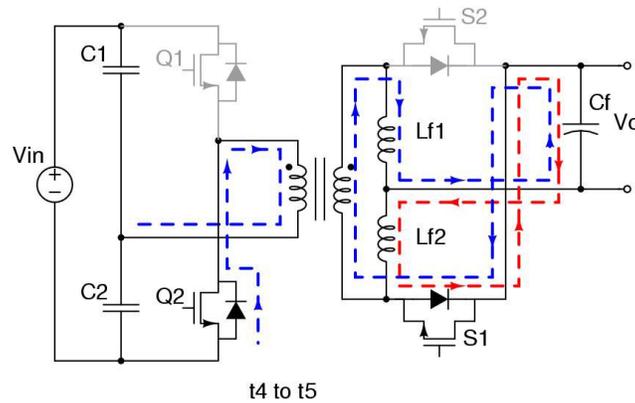


Figure 2.49 Operating mode 5 of half bridge with synchronous rectifier

Another benefit is Zero Voltage Switching. To use 200V MOSFET, symmetrical half bridge is used. With symmetrical half bridge, ZVS cannot be achieved. With QSW synchronous rectification, we can achieve ZVS for the primary switches. At time t_2 , synchronous rectifier S1 is turned off. Since the current is negative, it cannot go through the body diode. Then this current will be flow through transformer. This current then reflects to primary side of the transformer and it will discharge the output capacitor of primary switch Q1 and Q2 so that ZVS could be achieved.

With QSW synchronous rectification, reverse recovery problem of body diodes of synchronous rectifier could be solved. Primary switches also can achieve ZVS. But to achieve QSW operation mode, the inductor current ripple will be very large. The question is how much increasing of conduction loss will be caused by large current ripple.

For secondary two synchronous rectifiers, the current flowing through them is the sum of two inductor currents as seen in Figure 2.44. Since the two inductor currents are out of phase to each other. When they add up, the ripple will be much smaller. So for secondary side, the large current ripple will not show up. The question is the primary side two switches. For this technique, the primary switches will see the current ripple of each individual inductor. So conduction loss of primary switches will increase. But in this application, the primary conduction loss is not significant in total loss. As shown in Figure 2.50 although the primary conduction loss will increase about 35%, still better efficiency could be expected because of reduced conduction loss of secondary side and zero voltage switching for primary switches.

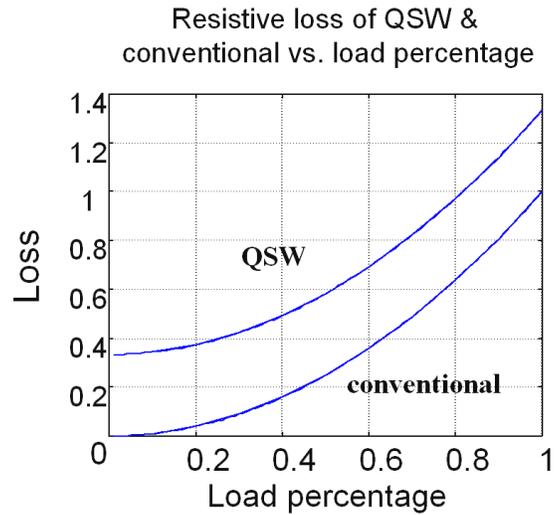


Figure 2.50 Primary loss comparison of QSW and conventional synchronous rectifier

Figure 2.51 shows the test circuit of half bridge with QSW synchronous rectifier. It is working as symmetrical half bridge.

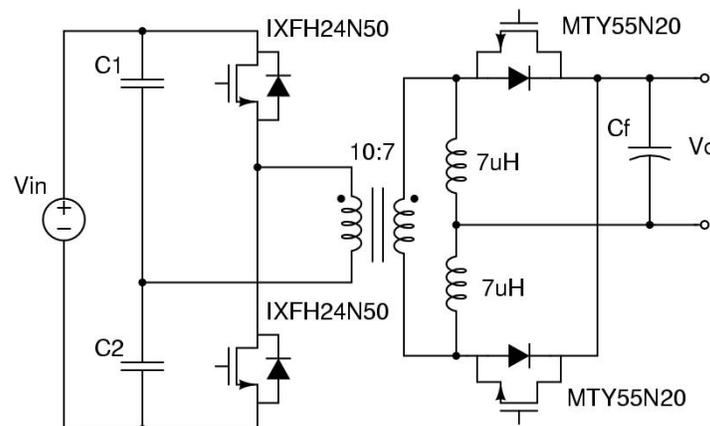


Figure 2.51 Test circuit of QSW synchronous rectifier

The test waveform is shown in Figure 2.52 for light load and in Figure 2.53 for heavy load. QSW operation mode could be identified from the negative current. There is no current spike in QSW operation mode. The efficiency test results are shown in Figure 2.54. With QSW synchronous rectification, the

efficiency at full load could reach 95%. For synchronous rectifier without QSW, after push output current over 10A, the devices will be destroyed by excessive reverse recovery loss.

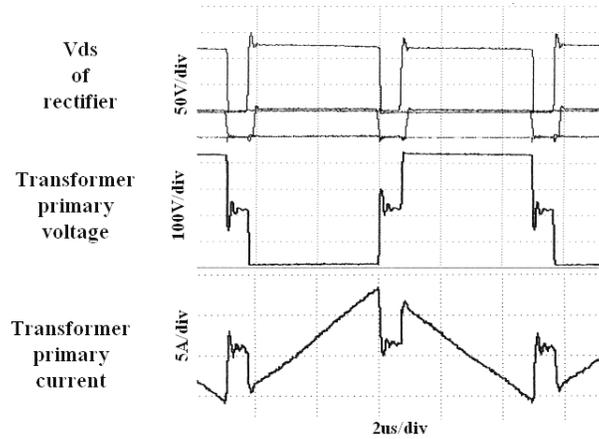


Figure 2.52 Test waveform of QSW synchronous rectifier at light load

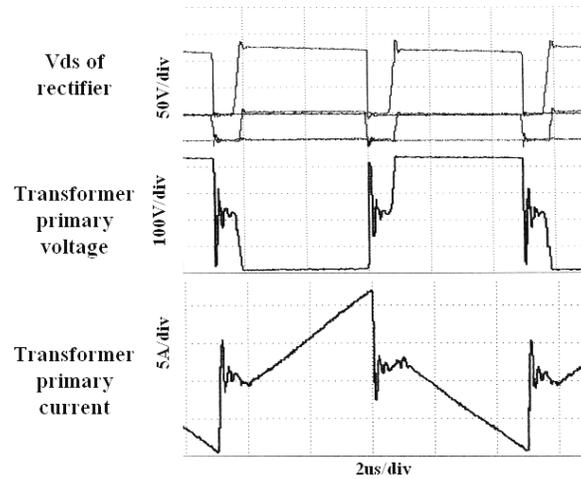


Figure 2.53 Test waveform of QSW synchronous rectifier at heavy load

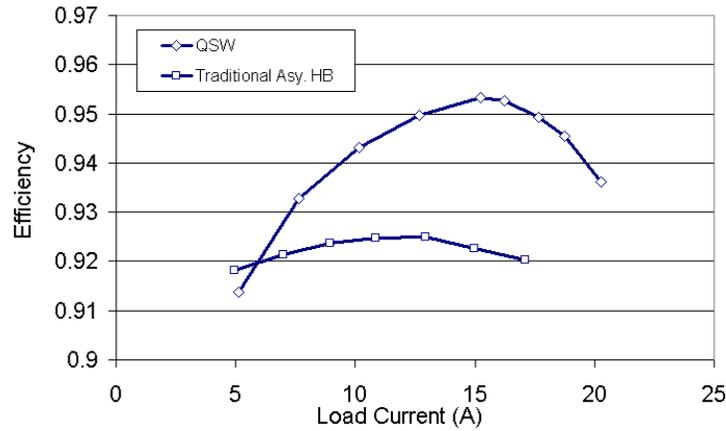


Figure 2.54 Test efficiency of half bridge with QSW synchronous rectifier

QSW synchronous rectification could effectively eliminate body diode reverse recovery problem of synchronous rectifier. With current doubler output filter, the current ripple on synchronous rectifier will not increase significantly compared with non-QSW mode. This method could be implemented to other topologies too. Figure 2.55 shows the diagram of Phase shift full bridge with QSW synchronous rectifier. In other application where synchronous rectifier is used, this method could also provide a simple solution to the body diode reverse recovery issue.

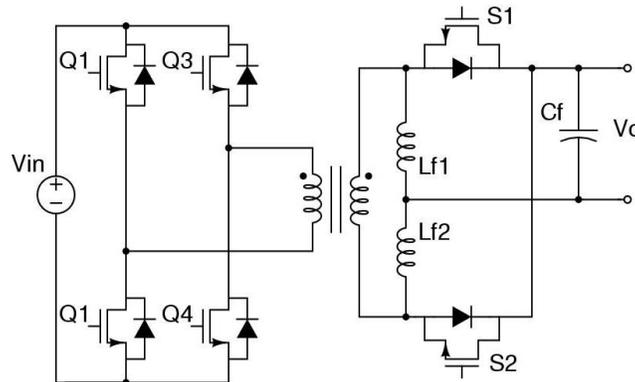


Figure 2.55 Full bridge with QSW synchronous rectifier

2.7 Summary and issues

In this chapter, several techniques are presented to improve the performance of half bridge converter. The target is to improve the efficiency at normal operation mode.

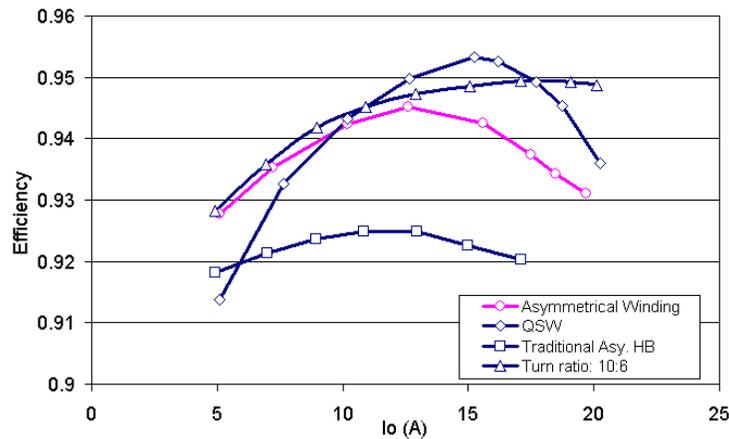


Figure 2.56 Efficiency comparison of different methods

Range winding solution can effectively improve the efficiency at high input voltage and use range winding to cover wide input range. It enables the design to be concentrated only on the performance of our interest and gives best performance possible. However, to implement range winding solution, extra components are needed which makes this solution very complex.

Asymmetrical winding solution is a simpler yet effective solution for asymmetrical half bridge converter. This method doesn't need extra components. With asymmetrical winding, the duty cycle at high input voltage could be extended. With extended duty cycle, the voltage stress of output rectifier could be reduced so that shottky diode could be used. With shottky diode, conduction loss

and switching loss could be reduced. There are some side effects of this method. With asymmetrical winding, the output current will be discontinuous. This requires more output capacitor. Also, the current stress is unbalanced for secondary devices. In the design, this should be taken into consideration.

The QSW synchronous rectification technique, which enables the using of synchronous rectification in this application, could reduce the conduction loss and also help primary switches to achieve zero voltage switching. With QSW mode, the body diode of synchronous rectifier will never conduct. Primary switches can achieve zero voltage switching at whole load range. Currently, because of the limitation of device, only when the voltage stress is lower than 200V, synchronous rectifier shows benefit over diode rectifier. These limits the topologies could use this technology. With more advanced power MOSFET technology, this limitation could be raised to high voltage. It will enable wider range of application for QSW synchronous rectification. The other problem with QSW synchronous rectifier is the high turn off current for primary switches, which will introduce high switching loss. This makes QSW synchronous rectifier not suitable for high switching frequency.

Compare the efficiency and complexity, range winding provides highest efficiency at normal operation with relatively simple circuit.

Although these methods could improve the efficiency of front-end converter at normal operation, to achieve high power density and low profile, high switching frequency operation is also necessary. But for both the state of the art

topologies, switching loss is a big obstacle for high frequency operation. Here the switching loss just take turn off loss of primary power MOSFET into consideration. From Figure 2.57, if switching frequency increases to 400kHz, switching loss will be much higher. This will require more space for thermal management of the power devices. This is a big limitation for PWM converter to achieve high power density.

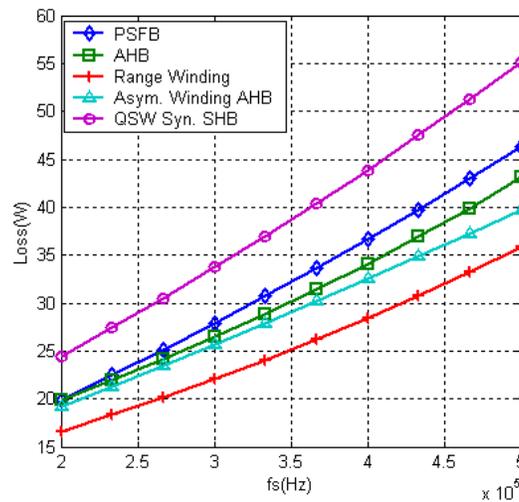


Figure 2.57. Primary switch total loss for different switching frequency

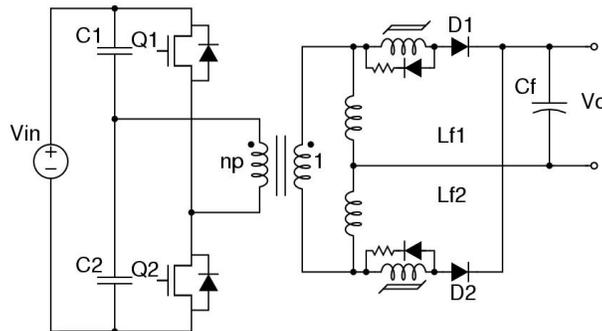


Figure 2.58 Half bridge converter with snubber circuit

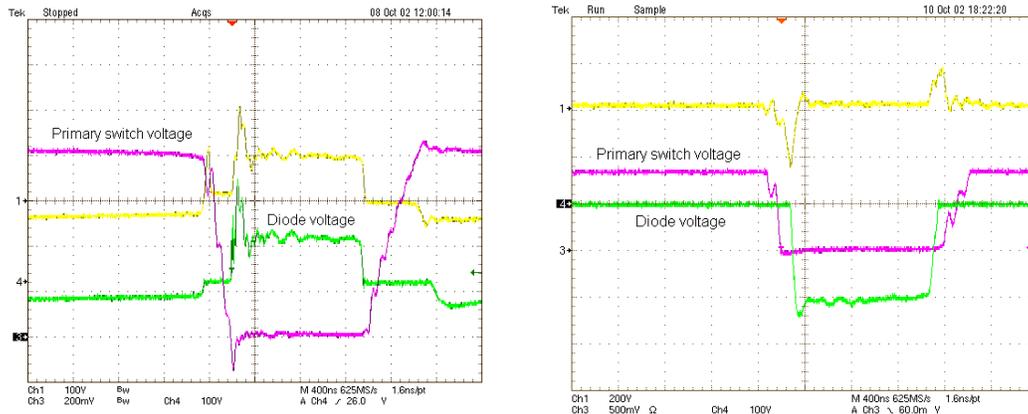


Figure 2.59 Test waveform with and without snubber circuit

Another problem for the state of the art topologies is the reverse recovery problem of secondary rectifier diodes. As seen in Figure 2.59, with diode reverse recovery, the current stress and voltage stress is a serious problem. With saturable core snubber shown in Figure 2.58, the problem could be reduced as shown in Figure 2.59. The problem is for snubber circuit; thermal problem and high loss prevent them to operate with high switching frequency. With 200kHz switching frequency, the temperature of the saturable core is already 85 degree.

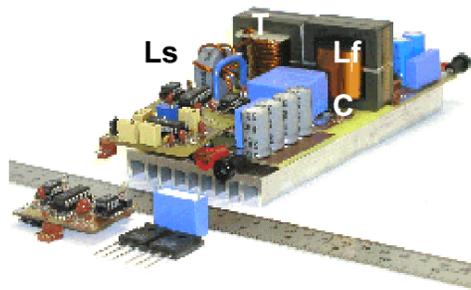


Figure 2.60 Prototype of 200kHz asymmetrical half bridge with discrete components

Figure 2.60 shows the prototype of a 200kHz asymmetrical half bridge converter. Magnetic and capacitor occupied huge space in the system. Non uniform profile also wasted lot of space. In fact, the active switches and the

driver also take lot of space in the system. In next chapter, the advanced packaging technology will be discussed for this converter. As will be demonstrated in next chapter, with advanced packaging technology, the power density of the converter could be significantly improved.