Q-Enhanced LC Resonators for Monolithic, Low-Loss Filters in Gallium Arsenide Technology

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(ABSTRACT)

The rapid development of wireless applications has created a demand for low-cost, compact, low-power hardware solutions. This demand has driven efforts to realize fully integrated, "single-chip" systems. While substantial progress had been made in the integration of many RF and baseband processing elements through the development of new technologies and refinements of existing technologies, progress in the area of fully monolithic filters has been limited due to the losses (low Qs) associated with integrated passive elements in standard IC processes.

The work in this thesis focuses on the development low-loss, Q-enhanced LC filters in GaAs E/D-SAGFET technology. This thesis presents a methodology for designing Q-enhanced LC resonators and low-loss, monolithic LC filters based on these resonators.

The first phase of this work focused on the Q-enhancement of LC resonator structures using FET-based active negative resistance circuits. Three passive resonators were designed, fabricated, and measured to determine their loss and frequency response. Furthermore, six Q-enhanced resonators were designed, fabricated, and measured to compare the performance of various negative resistance circuit designs.

In the second phase of this work, four of these Q-enhanced resonator designs were used to implement fully-integrated second-order Butterworth bandpass filters. Each filter was designed for a 60 MHz, -3 dB bandwidth centered at 1.88 GHz, corresponding to the North American PCS transmit band. The best filter design achieves 0 dB of passband insertion loss while consuming 16 mA of current from a 3 V source (48 mW). Passband *gain* (up to 15 dB) can be achieved with increased bias current before instability is encountered. The filter provides more than 30 dB of rejection at 1.7 and 2 GHz and more than 70 dB of rejection below 1.5 GHz. In the filter passband, the noise figure is 12 dB and the output 1 dB compression point is -18 dBm. These Q-enhanced LC filters have potential application as image-reject filters in GaAs integrated transceiver designs.

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Chapter 1

Introduction

There are significant advantages in monolithically integrating the functions of an RF transceiver onto a single chip using a standard process. Performance can be improved by the elimination of parasitics inherent in elements such as the package and bondwires. Previous physical constraints, such as the maximum number of pins available for a given package, can be eliminated, leading to the possibility of increased functionality. The ability to isolate the transceiver design from factors external to the chip results in fewer unknown sources of interference, leading to greater reliability. In addition, inter-stage matching requirements can be reduced since the design is no longer constrained to system impedance of off-chip elements. Increased integration will also potentially lead to a continual decrease in physical size and system cost. Finally, reducing the number of discrete devices required to produce a transceiver, will improve the manufacturability and reliability of the product.

Figure 1.1 illustrates the extent to which a generic heterodyne transceiver has been integrated commercially in Gallium Arsenide (GaAs) technology. The performance of standard MESFET, SAGFET, and pHEMT devices (high f_T and f_{max}, low gate resistance) allows for the design of high-performance, low-noise and general purpose amplifiers through millimeter-wave frequencies. In addition, given the high gate impedance of these devices, switches and switching mode mixers can be easily designed. However, to date, the performance of on-chip filtering structures has limited the integration of the entire transceiver subsystem.

The filters required in a heterodyne architecture must have high selectivity and low

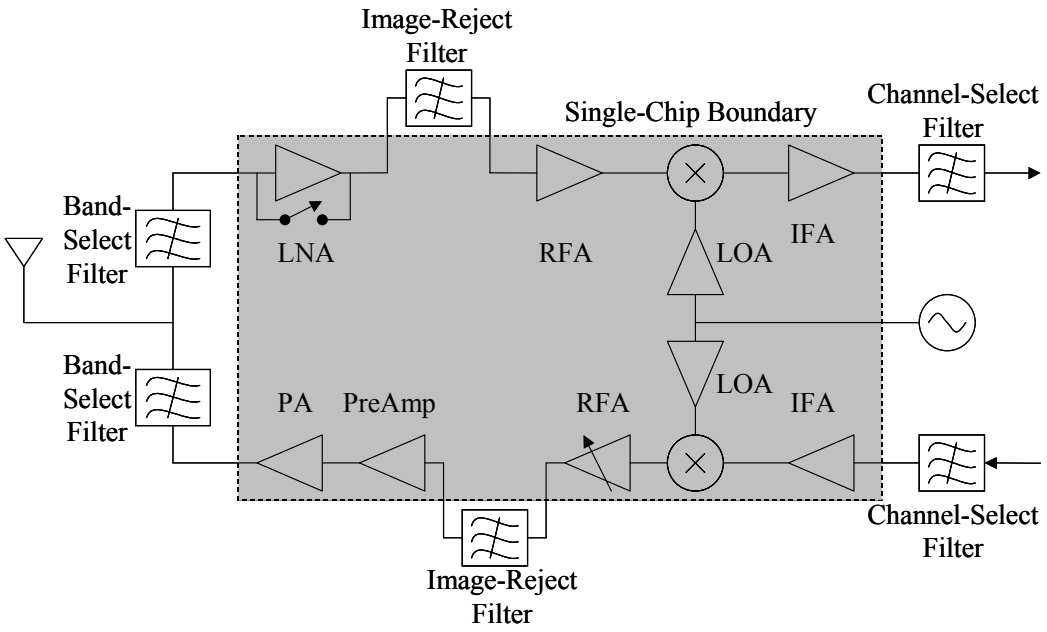


Figure 1.1: A highly integrated GaAs heterodyne transceiver.

passband insertion loss. The selectivity of a filter is defined as the fractional bandwidth, given by $\frac{BW}{f_0}$. High selectivity is required to reject unwanted interference while minimally attenuating the desired signal. In the case of the band-select filters, low loss is critical in order to minimize the noise figure of the receiver and maximize the power delivered to the antenna by the transmitter. However, due to losses associated with *integrated* filter elements (monolithic inductors and capacitors) and the loading by components preceding and following the filter in the transceiver, lumped element monolithic filters suffer from high passband insertion loss and low selectivity compared to alternative off-chip filtering technologies such SAW and ceramic filters. Furthermore, while low-loss monolithic alternatives can be designed using distributed elements, their physical size, especially at the frequency ranges required in this thesis (1-2 GHz), are prohibitively large.

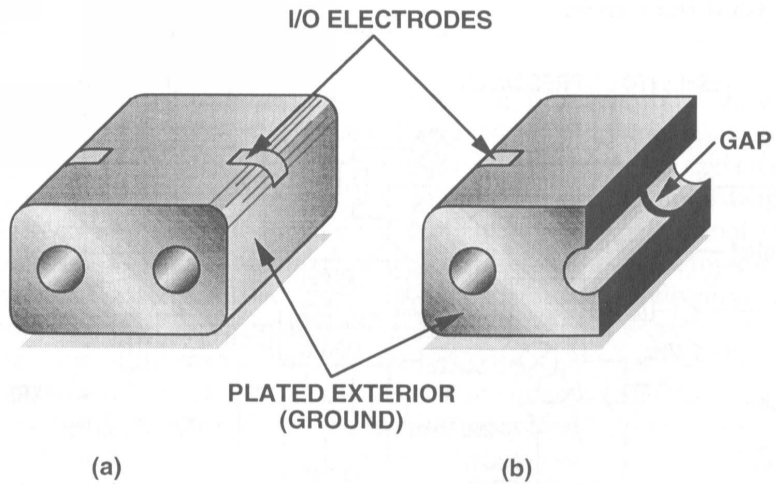


Figure 1.2: Dielectric block filter [1]: (a) Bottom side view; (b) Bottom side view cut-away.

1.1 Current Filter Technology

Current state-of-the-art mobile communications products typically use a combination of off-chip Surface Acoustic Wave (SAW) filters and ceramic filters to perform the frequency selection required. Low loss is typically required for the band select filter in order to minimize the noise figure of the receiver and to limit the loss after the power amplifier. Therefore, ceramic filters are typically used for band select filters because they have lower insertion loss than other technologies. On the other hand, while SAW filters do present more insertion loss, they typically have higher selectivity and out-of-band rejection than ceramic filters. Therefore, SAW filters are typically used for image rejection in both the receiver and transmitter, and for channel selection at the intermediate frequency (IF).

Ceramic filters are electrically equivalent to microwave interdigitated filters (Figure 1.2 [1]). In interdigital filters, a metal rod in a cavity forms a resonator and couples to other resonators to realize a filter [2]. Resonators are formed using short-circuited stubs (rods), then coupled through air to adjacent resonators to form a filter. Electrodes are placed on the input and output resonators for coupling into and out of the filter. The entire structure is then surrounded by a metal enclosure to form a cavity. To reduce the physical dimensions of the resonator and increase coupling, the air dielectric is replaced by a ceramic material to increase the dielectric constant. Because RF current only flows on the surface of the resonator rods due to the skin effect, the rods can be removed and

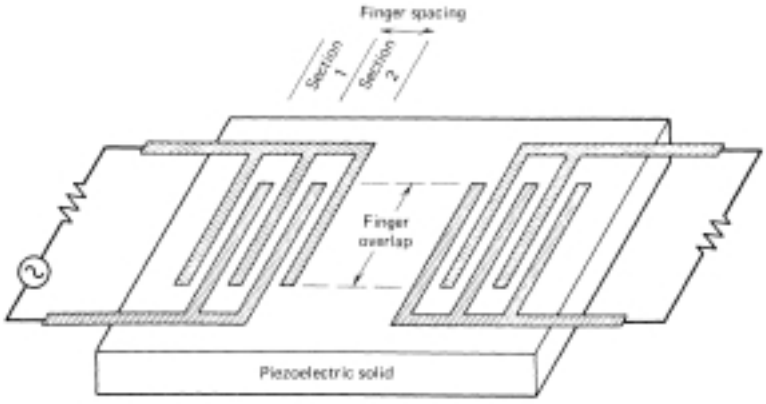


Figure 1.3: SAW filter structure [3].

the remaining holes can be plated with some low-loss metal (ex. silver) to define the resonators. The metal case can be replaced by plating the dielectric with a conductor to form the cavity.

A SAW filter incorporates two transducers consisting of interdigital arrays of thin-film metal electrodes fabricated on a piezoelectric substrate (Fig. 1.3 [3]). A piezoelectric material is one in which the electric field in the material has a reciprocal, linear relationship with the mechanical strain in the material. When a signal is applied to the input transducer, the alternating electrode voltage induces an electric field in the piezoelectric material, causing the material to expand and contract. This generates an acoustic wave that propagates across the surface of the device. This acoustic wave in turn generates a reciprocal electrostatic wave with potentials at the surface of the device, which are subsequently detected by the second (output) transducer. The electrode (finger) spacing determines the wavelength (frequency) of the acoustic wave, and the number of sections determines the bandwidth of the filter [3].

Though both SAW and ceramic filters have high selectivity, both are inherently limited by their structure. In each technology, the frequency of operation is fixed (by the electrode spacing for the SAW filter or the resonator length of the ceramic filter), and cannot be tuned electrically. Finally, the material requirements of both structures limits their integration into standard processes. Ceramic filters require the resonator to be encapsulated in a physically large dielectric block with a high dielectric constant. SAW filters require a piezoelectric material to generate and detect the acoustic wave.

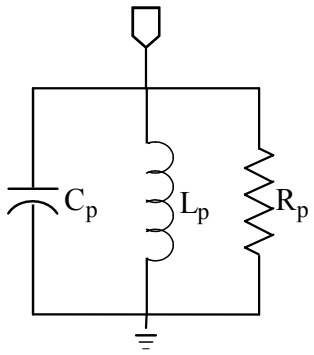


Figure 1.4: Parallel RLC resonator.

1.2 High-Selectivity, Low-Loss LC Filters

The goals of designing a filter with low loss and high selectivity is limited by the loss of the LC resonator(s) and the effects of external loading. Although the Q of a resonator does not directly correlate to the selectivity and the insertion loss of anything beyond a single-resonator filter, the unloaded and loaded Qs of the resonator do offer insights into the mechanisms that determine the selectivity and insertion loss of higher-order filters.

1.2.1 Resonator Qs

The filters designed in this thesis are based on shunt parallel LC resonators. Therefore, in analyzing the loss and Q of the resonators, the parallel equivalent model (Fig. 1.4) of the resonator is used. Though the loss (modeled by the resistance) is generated in series with the inductor, it can be extracted as an equivalent resistance in parallel with a lossless inductor. This will be discussed in Section 2.1.2.

Given the loss resistance, the quality factor (Q) of the resonator can be found. The Q of a resonator is defined as the ratio of maximum instantaneous energy stored in the circuit to the energy dissipated per cycle [3]. Therefore, the *unloaded* Q of the resonator is a measure of the loss of the resonator relative to the reactance of the resonator and can be computed by [3]:

$$Q_{unloaded} = \frac{R_p}{2\pi f L_p} \tag{1.1}$$

Ideally, the resonator would have no loss (infinite R_p) resulting in an infinite Q. Short of that, maximizing R_p by minimizing the loss will maximize the Q of the resonator. Chapter 2 will discuss how the Qs of integrated LC resonators are limited by the losses inherent in the design of monolithic spiral inductors.

Furthermore, when this resonator is driven by a system (modeled by a Thevenin equivalent source), the resonator will be loaded by the external source resistance ($R_{s,ext}$). This external resistance will not add loss to the resonator itself, but will change the frequency response of the impedance of the resonator due to the increased energy dissipation. The effect of this loading can be seen in the *loaded* Q of the resonator [2]:

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_{unloaded}} + \frac{1}{Q_{ext}} \tag{1.2}$$

where Q_{ext} is given by:

$$Q_{ext} = \frac{2\pi f L_s}{R_{s,ext}} = \frac{R_{p,ext}}{2\pi f L_p} \tag{1.3}$$

Finally, the loaded Q of the resonator can be used to find the half-power bandwidth of the resonator input impedance using the following relation [3]:

$$Q_{loaded} = \frac{f_0}{BW} \tag{1.4}$$

1.2.2 Single-Resonator Filters

To illustrate improvements in the insertion loss of filters obtained by improving the unloaded Q of individual resonators, one-port resonators will be designed (Chapter 3) and implemented in a shunt configuration, effectively creating 2-port, single-resonator filters (Fig. 1.5). For this structure, the filter selectivity and insertion loss can be predicted by the unloaded and loaded Qs of the one-port resonator. The loaded Q for this structure can be calculated by:

$$Q_{loaded} = \frac{R_p||R_{source}||R_{load}}{2\pi f L_p} \tag{1.5}$$

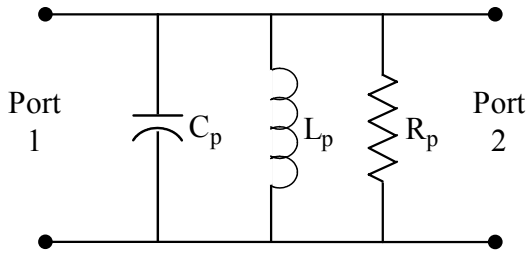


Figure 1.5: Single-resonator filter.

The bandwidth of the single-resonator filter can then be found by:

$$BW = \frac{f_0}{Q_{loaded}} \tag{1.6}$$

Furthermore, the insertion loss (in dB) can also be predicted using [4]:

$$L(f) = -10\log\left[\frac{1+\left(2Q_{loaded}\frac{f-f_0}{f_0}\right)^2}{\left(1-\frac{Q_{loaded}}{Q_{unloaded}}\right)^2}\right] \tag{1.7}$$

At the center frequency ($f = f_0$) of the filter, this expression simplifies to:

$$L(f_0) = 20\log\left(1-\frac{R_p||R_{source}||R_{load}}{R_p}\right) \tag{1.8}$$

Therefore, while determining the loss away from the center frequency of the filter requires knowledge of both the loaded and unloaded Qs, determining the insertion loss at the center frequency only requires the loss of the resonator and the source and load impedances. For example, consider a resonator with L_p=1 nH, C_p=7.2 pF (f_0 = 1.88 GHz), and R_p=100 Ω in a 50 Ω system. Using Equation 1.5, the loaded Q of this resonator is found to be 1.69, leading to a resonator BW of 1.1 GHz. Furthermore, using Equation 1.8, the insertion loss at the center frequency is calculated to be -1.93 dB. Simulating the single-resonator filter in Agilent EESof Series IV [5] (Fig. 1.6), the resulting 3 dB bandwidth and insertion loss are 1.1 GHz and -1.93 dB, respectively, as predicted.

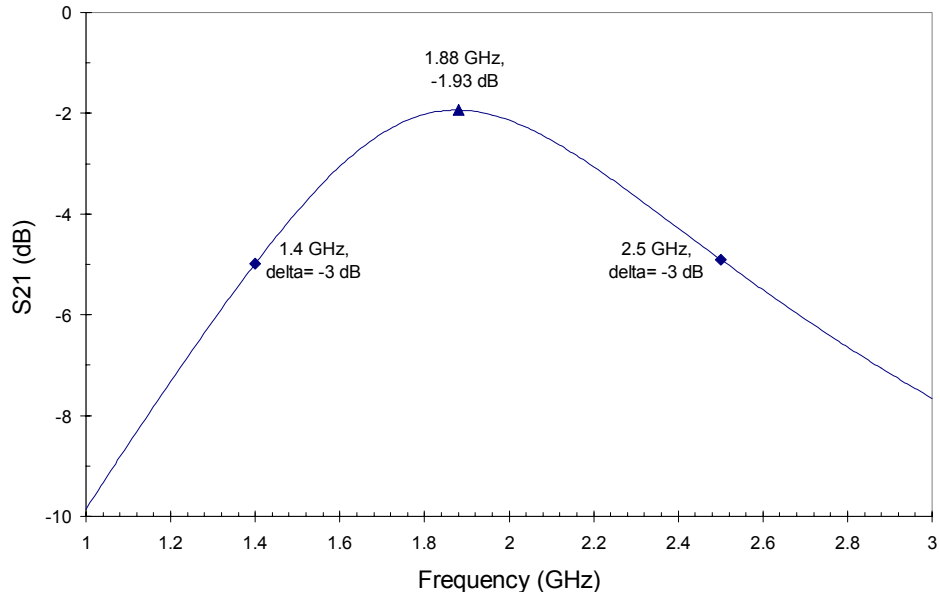


Figure 1.6: Single-resonator filter example.

1.2.3 Higher Order Filters

The insertion loss of higher-order filters will be a function of both the loss of the individual resonators and the coupling of the resonator stages. Low-loss, high-Q (unloaded) resonators are necessary for low-loss filters. However, tightly coupled resonators, essential for highly selective filters, will lead to increased filter insertion loss. Therefore, the selectivity of the filter becomes a trade-off for loss. Figure 1.7 shows the how the passband insertion loss of a second order Butterworth filter increases with a reduction in the unloaded Q of the individual resonators.

As indicated above, for higher order filters, the coupling between the resonators will, in large part, determine the selectivity of the filter. Improving the loaded Q of the resonator can improve the selectivity of the filter. However, high selectivity can still be achieved using a low Q resonator by tightly coupling the resonators.

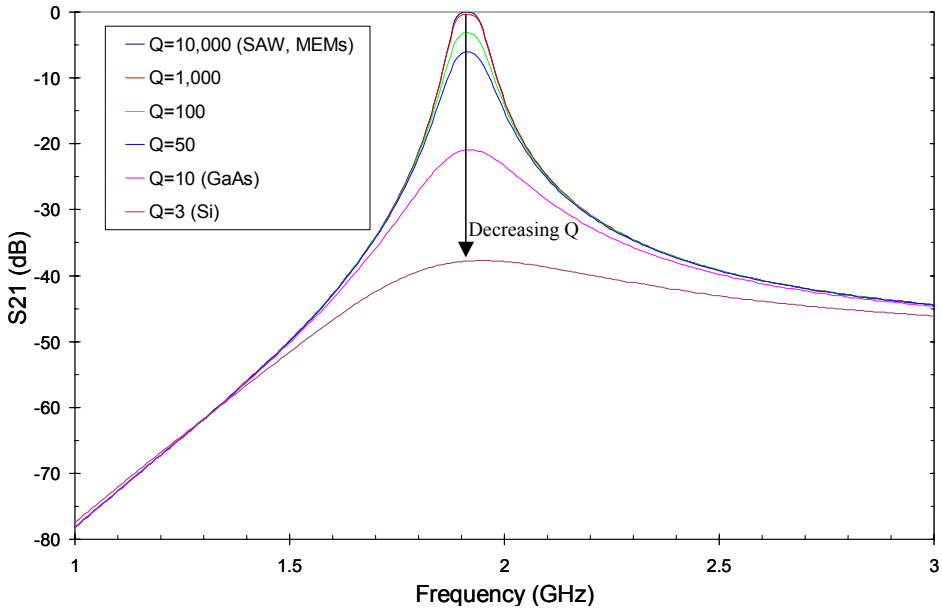


Figure 1.7: Response of 2^{nd} order Butterworth filter to decreased resonator Q.

1.3 Monolithic Filters

Given the goal of designing monolithic filter structures, there are a number of options found in the literature. Distributed element effects can be exploited to design filters. Ring resonators are one example of filters based on distributed element effects. Also, advances in micromachining have enabled the development of micro-mechanical resonators which can be used to design electromechanical filters. Finally, lossy lumped element filters can be improved by using active elements.

Ring resonators with loss compensation have been used to design monolithic filters [6]. These filters can be designed using a standard process since they require only a transmission line structure and a transistor circuit for loss compensation. However, for the frequency range of interest in this thesis ($\backsim$1-2 GHz), the physical transmission line lengths required by these structures are far too large to be feasible for on-chip integration.

The rapid development of micromachining technologies has led to the development of microelectromechanical (MEM) filters [7]. Using these techniques, mechanical resonators with extremely high Qs ($>$ 80,000 in vacuum) can be coupled together to form an electromechanical filter. Although the processing techniques required are not yet a part of

many standard processes, these structures could be integrated on chip with the other elements of the transceiver. However, at present the main limitation to the design of these filters is the maximum frequency of the mechanical resonator. To date, MEM resonators have only been demonstrated at frequencies into the low VHF range (30-90 MHz) [8], far below the frequency range ($\backsim$1-2 GHz) required in this thesis.

This thesis will focus on the design of lumped element LC resonators capacitively coupled together to form a filter. Lumped element filters can achieve the desired passband frequency ranges while remaining relatively compact. The basic approach is to design an L-C ladder network with element values chosen to synthesize the desired filtering response. However, realizing a monolithic version of the LC network is not as straightforward as it might first appear. On the one hand, monolithic capacitors can occupy relatively large chip areas and may present electrostatic discharge problems. Their high-frequency loss is generally not prohibitive for their use in monolithic LC filters, especially on a semi-insulating substrate. Monolithic inductors, on the other hand, can suffer from significant RF losses that limit their Q, and can also occupy large chip areas at the frequencies of interest. Furthermore, monolithic spiral inductors have significant inter-winding capacitances that result in a self-resonant frequency (f_{SR}), above which the inductor becomes capacitive in nature rather than inductive. Roughly speaking, as the number of turns or the outer segment length of the inductor is increased for higher inductor values, the Q decreases due to the increased series resistance of the spiral, and the f_{SR} decreases due to the increased inter-winding capacitance. It is the Q limitation that makes the monolithic inductor the performance-limiting passive device in lumped element designs at RF frequencies. As discussed above, a resonator designed with a low-Q inductor will suffer high loss and low resonator Q. As a result, there are currently major on-going research efforts into improving the performance of spiral inductors (or replacing them outright) for monolithic lumped element RF networks.

1.3.1 Active Inductors

One method of designing integrated low-loss LC resonators is to replace a passive inductor entirely with a circuit that generates an equivalent inductive reactance. These circuits are often referred to as *active inductors*. The majority of previous realizations of active inductors have utilized a capacitively terminated gyrator circuit (Fig. 1.8) [9].

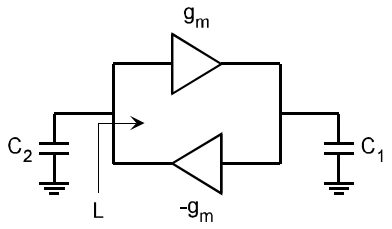


Figure 1.8: LC resonator realized with a gyrator and two capacitors.

A gyrator is a back-to-back connection of inverting and non-inverting transconductance (g_m) elements. When the inverting input node of the gyrator is terminated with a capacitor (C_1), the impedance looking into the non-inverting input node behaves as an inductor with a value:

$$L = \frac{C_1}{g_m^2} \tag{1.9}$$

Thus, an effective LC resonator can be realized by shunting the non-inverting input node with a capacitor (C_2). The resonant frequency of the circuit is given by:

$$f_0 = \frac{g_m}{2\pi\sqrt{C_1 C_2}} \tag{1.10}$$

In addition, a tunable resonator can be realized with variable capacitors (varactors) or tunable transconductors. Therefore, there is not only the potential for reducing chip size by eliminating spiral inductors from the circuit layout, but also the potential for increased functionality (tunability.)

The primary difficulty in the design of active inductors is the design of the gyrator circuit. Hara, et al. [10] examined three topologies for the design of active inductors on GaAs and compared their resulting input impedances. The first topology [Fig. 1.9(a)] uses a common source FET cascode with feedback through a resistor. This is not strictly a gyrator circuit, but operates in a similar manner. In this topology, the resistor (R_{ext}) acts as the non-inverting transconductance, the cascode acts as the inverting transconductance, and the C_{gs} of the common source FET ($C_{gs,1}$) acts as the terminating capacitor. If the two FETs in the cascode have identical g_m and C_{gs}, the resulting input impedance of the network is approximately:

$$Z_{in} \approx \frac{1}{g_m} + j\frac{\omega C_{gs} R_{ext}}{g_m} \tag{1.11}$$

Thus the network looks like an inductor with a series loss arising from the value of g_m. However, since the g_ms for the devices are typically on the order of tens of mS, the resulting series resistance will be on the order of tens of ohms, which is much too large for low-loss filter resonator applications.

In an attempt to eliminate the loss term from the equivalent circuit, Hara, et al. [10] proposed a second topology [Fig. 1.9(b)] where the external resistor is replaced with a common gate FET that acts as the non-inverting transconductance ($g_{m,f}$). Again assuming the two FETs in the cascode are matched, the resulting input impedance is approximately:

$$Z_{in} \approx j\frac{\omega C_{gs}}{g_m g_{m,f}} \tag{1.12}$$

Despite the elimination of the real term, secondary effects still contribute loss, thereby limiting the effective inductor Q to $\backsim$ 2 at 3 GHz. Although this is an improvement from the first topology, passive spiral inductors on GaAs still have better performance.

The third topology [Fig. 1.9(c)] not only eliminates the loss term from the input impedance, but also creates an equivalent negative resistance with another FET cascode in the feedback path. Assuming both sets of cascodes are individually matched, the resulting input impedance is approximately:

$$Z_{in} \approx -\frac{C_{gs}}{C_{gs,f} g_m} + j\frac{\omega C_{gs}}{g_m g_{m,f}} \tag{1.13}$$

The negative resistance overcomes the losses and results in a maximum inductor Q of 65 at 8 GHz, which greatly exceeds the performance of a standard spiral inductor on GaAs. However, this improvement is at the expense of power consumption since there are now two cascodes that require biasing.

Complete filter designs using active inductors have also been published. Kaunisto, et al. [9] presented results on a 6th order Chebyshev bandpass filter using a similar active inductor topology to that of Hara, et al. However, they employed GaAs HBT technology

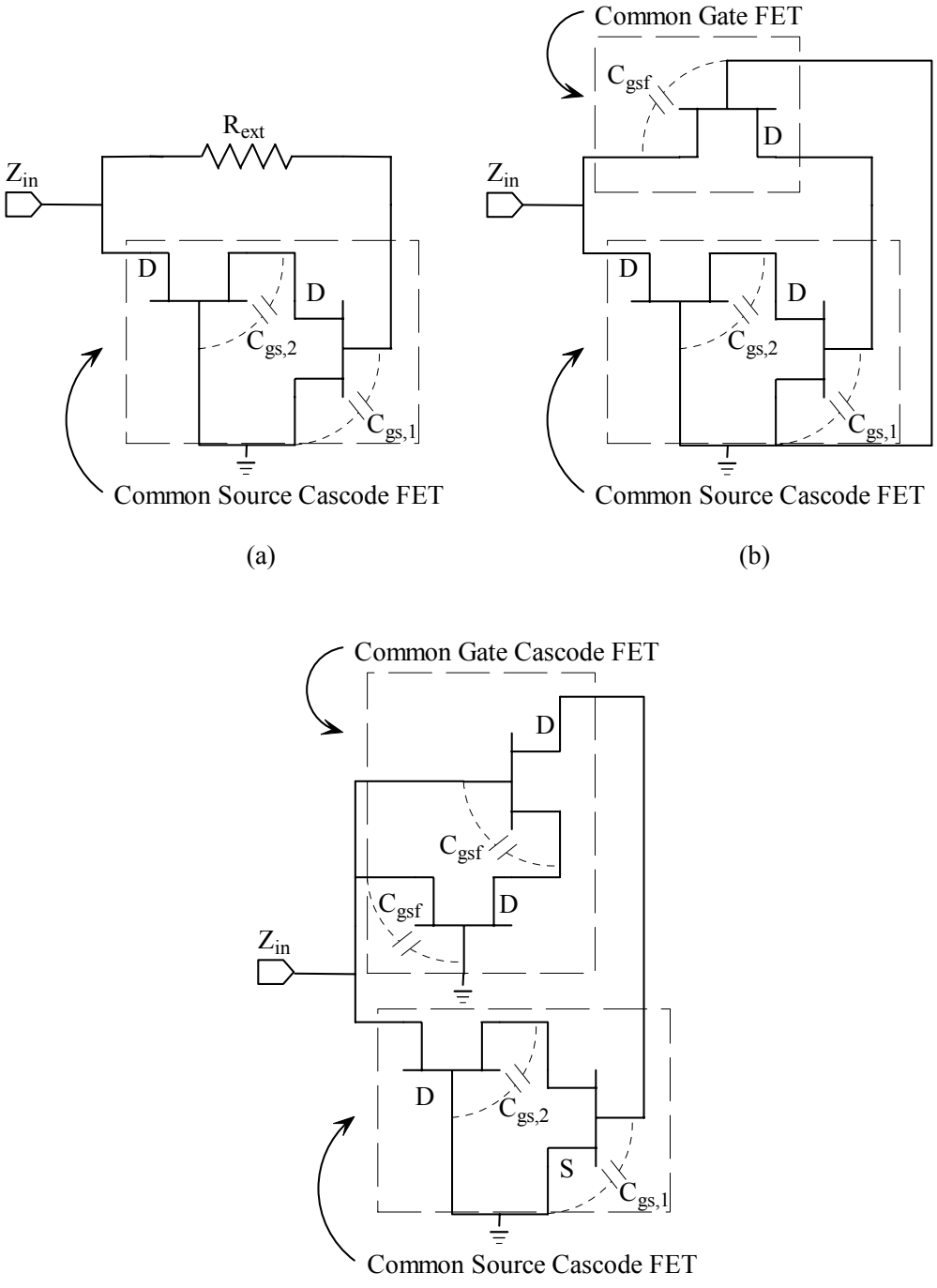


Figure 1.9: Active Inductor circuits: (a) Common Source Cascode with resistor feedback; (b) Common Source Cascode with Common Gate feedback; (c) Common Source Cascode with Common Gate Cascode feedback.

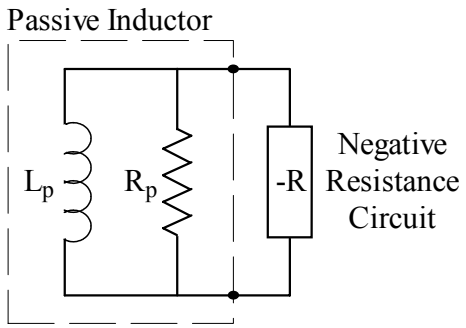


Figure 1.10: The Q-enhancement concept.

citing better performance and lower power consumption. The non-inverting transconductance was realized using a common base transistor and the inverting transconductance was realized using a common-emitter transistor. A MIM capacitor terminated the inverting input node. A varactor circuit was also added to the non-inverting input node to resonate with the active inductor and tune the center frequency. The design yielded a nominal center frequency of 2.32 GHz that could be tuned from 2.17-2.39 GHz. The bandwidth was on the order of 300 MHz, with an out of band rejection of 30 dB at ± 600 MHz off center. The power consumption is 25 mW with a 3 V supply. However, the major drawback of this filter design is a noise figure estimated at 35 dB. Also, at the stated DC power, the filter remains linear (measured by the 1 dB compression point) to only –20 dBm input power.

1.3.2 Q-Enhanced Inductors

Q-enhancement refers to the use of an active device to generate a negative resistance that compensates for the resistive losses of a physical (lossy) spiral inductor (Fig. 1.10). This negative resistance cancels the (parallel equivalent) resistance due to the loss of the inductor, thus effectively improving the Q of the inductor. Furthermore, if the loss of the inductor is dominant over the loading effects, reducing the inductor loss will also lead to an improvement in the resonator Q_{loaded}.

The negative resistance circuit can be realized using active elements in many different topologies (to be discussed in Chapter 3). The resulting Q-enhanced inductor can then be used in L-C filter topologies. In theory, a negative resistance circuit could also be used

the eliminate the loss of a capacitor. However, the non-ideal effects resulting from the addition of active devices outweigh the cancellation of the nominal loss of the capacitor. Though the majority of examples of Q-enhancement have been shown using a Si substrate [11], some recent examples of GaAs monolithic LC filters using active Q-enhanced spiral inductors follow.

Hopf, et al. [12] realized a first order bandpass filter at 5.5 GHz and two second order bandpass filters at 1.8 GHz (one fixed frequency, one tunable) on GaAs. The 5.5 GHz filter had a measured insertion *gain* of 2.9 dB, but suffered from low out-of-band rejection (first order). The fixed frequency 1.8 GHz filter had a 3 dB BW of 110 MHz, 0.17 dB insertion gain, and 20 dB rejection at 1.68 and 2 GHz, but suffered from a –7.2 dBm 1 dB compression point (P_{1dB}) and 700 mW of DC power consumption.

Kaunisto, et al. [13] took the approach of designing for large dynamic range by minimizing noise within the limitations of an active resonator structure. On a GaAs substrate, a 3.8 GHz second order filter with a BW of 40 MHz and a 3.4 GHz fourth order filter with a BW of 400 MHz were presented. The second order filter had a noise figure of 19 dB (only 2.2 dB above the theoretical minimum for the Q of that filter) and an IIP3 of -12 dBm. The lower-Q fourth order filter had a noise figure of 11 dB and an IIP3 of 8.5 dB. The nominal operating currents for the second order and fourth order filters were 5 and 10 mA respectively.

1.4 Objective

The objective of the work presented in this thesis is to develop a design methodology for integrated low-loss LC filters, and to demonstrate monolithic filter designs for PCS band applications. Since power consumption is an important consideration in this design, Q-enhanced inductors rather than active inductors will be used. The specific application for these filters will be image reject filtering for the PCS transmit band (1850 MHz - 1910 MHz). However, this work will primarily represent a comparative study into the design of these filters rather than an optimization for this specific application. The resulting filters will be compared on the basis of small-signal response, noise figure, dynamic range, DC power consumption, and physical die area.

1.5 Thesis Overview

The chapters in this thesis will present the steps in designing a Q-enhanced LC filter, culminating in the demonstration of a GaAs IC filter for PCS band applications.

Since the inductors are the major source of loss in the filters to be designed, Chapter 2 will focus on both the design of the monolithic spiral inductors and the impact of their inherent loss. To assist in the design of the inductors, a model will be introduced to predict the loss of the spiral inductor. Using this model, two spiral inductor structures will be introduced and compared on the basis of physical size, and electrical parasitics. Finally, since resonators will utilize parallel-mode Q-enhancement, the parallel equivalent resistance used to model the loss of the LC resonator will be derived.

Chapter 3 will focus on negative resistance circuits. Several negative resistance circuits used to Q-enhance lossy devices will be introduced and evaluated for their applicability. The input impedance of the chosen negative resistance circuit will be derived in order to find the parameter dependency and magnitude of the negative resistance. Finally, since this negative resistance circuit will be placed in parallel with a lossy resonator, the parallel equivalent negative resistance will be derived.

The design, layout, and measurements for a number of Q-enhanced LC resonators will be presented in chapter 4. The design of three LC resonator structures as well as the derivation of the total loss of each resonator will be presented. Negative resistance circuits will then be designed to Q-enhance the resonators. Finally, a number designs will be laid out, fabricated, and measured to evaluate the small-signal performance of the Q-enhanced resonators.

In Chapter 5, the Q-enhanced resonators introduced in Chapter 4 will be used to design a second order Butterworth filters. The filters will be designed as image reject filters for the PCS transmit band (1.85-1.91 GHz). Measured results for 7 filters designed and fabricated will be presented to quantify the small-signal response, the large-signal linearity, and noise figure.

Finally, Chapter 6 will conclude this work and discuss possible future research directions.

1.5.1 M/A-COM E/D SAGFET Process

The process made available by M/A-COM for fabrication of the circuits designed in this thesis is the Fab II E/D self-aligned gate FET (SAGFET) on a 10 mil (250 μm) gallium arsenide (GaAs) substrate. This is a two metal layer (excluding gate metal) process without vias or backside metallization. Capacitors are designed using the two metal layers and a fixed sheet capacitance. Spiral inductors can be designed either using the two metal layers plated on top of each other, or as two separate spirals on each metal layer (discussed in detail in Section 2.1). Finally, this process offers both an enhancement-mode FET[1] with a positive threshold voltage (positive V_{gs}) and a depletion-mode FET with a negative threshold voltage. Models for all these structures were provided by M/A-COM (update 08/01/2000) for simulation using Agilent Series IV version 6.6 [5]. During the initial phases of the research, December 1999 models were used; these were later updated with the August 2000 models.

[1]The potential has been shown for reduced noise using an enhancement-mode FET in place of a depletion-mode FET.

Chapter 2

GaAs MMIC Spiral Inductors

As discussed in the introduction, the overwhelming majority of the loss in a passive monolithic LC resonator will be due to the conductor loss associated with the inductor. Therefore, in order to understand the loss of the resonator structure, the first step is to determine the mechanisms and magnitude of the loss associated with the MMIC spiral inductors in the available process. In this chapter, the loss mechanisms for spiral inductors will be introduced along with both a general model and application-specific approximation of the general model to account for the parasitic effects of the inductor. Given these models, the different spiral structures available for the given process will be analyzed and compared. Finally, in order to limit the number of variables in the design of subsequent LC resonators, three baseline spiral inductors will be introduced for application in the resonator designs in this thesis. These three spiral structures will be analyzed in a manner addressing each element of the first order model of the spiral.

2.1 MMIC Spiral Inductor Models

In generating a model for a spiral inductor, two dominant parasitic effects should be included. First, the loss due to the resistivity of the metal traces of the spiral must be included. Secondly, parasitic capacitive effects, both between the spiral windings and between the metal traces and ground, must be accounted for in order to determine the useful frequency range, as limited by self resonance. The self-resonance frequency (SRF) is the frequency at which the net parasitic capacitance parallel resonates with the

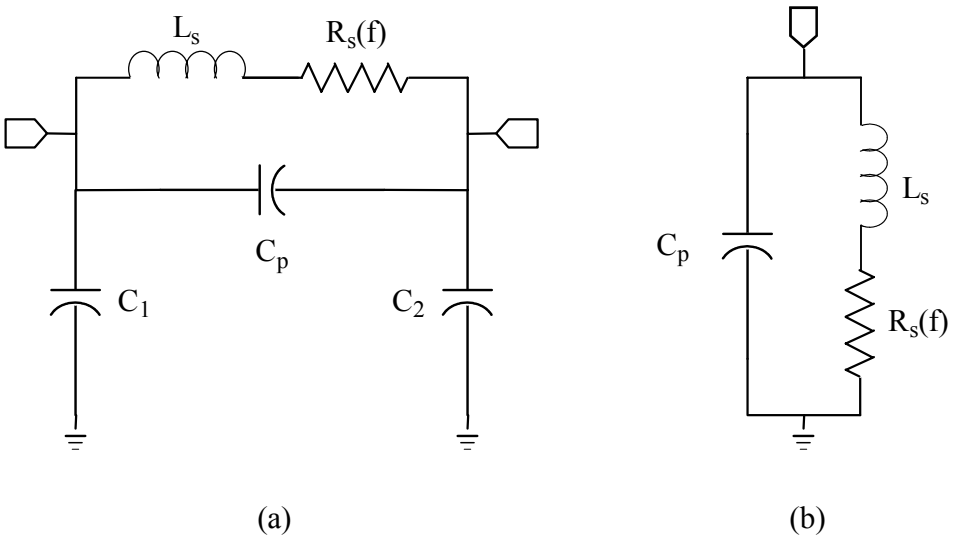


Figure 2.1: Spiral inductor models: (a) General model; (b) Simplified, application specific model.

inductance of the spiral, above which the spiral appears capacitive. Furthermore, these capacitive effects will limit the maximum effective inductance that can be achieved.

2.1.1 First Order Model

Figure 2.1(a) shows a general model commonly used for spiral inductors. In this model L_s models the inductance of the spiral, R_s models the cumulative effects of the resistivity of the metal traces, C_p models the effects of the capacitance between the windings of the spiral, and C_1 and C_2 model the capacitance between the metal traces and ground.

However, this model can be simplified based on the specific application in this thesis. First, given that the GaAs substrate is semi-insulating (high resistivity), the effects of coupling through the substrate to ground (modeled by C_1 and C_2) will have minimal effect. In addition, given that the spiral inductors used in this work will be shunted to ground in the resonator structure, one of these capacitors (C_1 or C_2) will be bypassed by ground and the other will add in parallel with C_p. Given the magnitude of C_p, relative to C_1 or C_2, the effect of adding the two in parallel will be negligible. Therefore, in this thesis, the effects of C_1 and C_2 can be ignored, resulting in the model shown in Figure 2.1(b).

Inductance (L_s)

An approximation for the inductance of a square spiral is given by [14]:

$$\mathrm{L_s} \approx \mu_0 N^2 r \tag{2.1}$$

where μ_0 is the permeability of free space ($4\pi \times 10^{-7}$H/m), N is the number of turns, and r is the radius of the spiral. However, instead of using the radius of a square spiral, the outer segment length, which is equal to twice the radius, will be used as the variable in the design of the spiral.

Capacitance (C_p)

The dominant capacitance modeled by C_p is the capacitance between two adjacent traces in the spiral and can be approximated by:

$$\mathrm{C_p} \approx \frac{\epsilon_{gap}(t_{trace} \times l_{trace})}{w_{gap}} \tag{2.2}$$

Given a constant metal thickness (t_{trace}), the resulting capacitance is proportional to the overall trace length (l_{trace}) and inversely proportional to the width of the gap (w_{gap}). For the standard spirals on this process, the gap width is set at 6 μm. Therefore, to design for minimum C_p, the overall trace length, which is roughly proportional to the number of turns (N) and the outer segment length (or radius, r), should be minimized. Thus, small inductance values will result in a small C_p while large inductance values will result in a larger C_p.

Loss (R_s)

Resistive effects of the metal traces dominate the series resistance (R_s) of the spiral inductors used in this work. However, this loss is not constant, but will increase with frequency due to the skin effect. At DC and frequencies at which the skin depth is larger than the thickness of the trace, the physical cross sectional area of the trace and resistivity of the thin-film metal will account for the loss. At frequencies above that at

which the skin depth is equal to the thickness of the trace ($f > f_b$), the effective cross sectional area will be decreased resulting in increased in loss. A model for R_s is given by ([15]):

$$R_s(f) \approx R_{dc}\sqrt{\frac{f}{f_b} + \frac{1}{1+\frac{f}{f_b}}} \tag{2.3}$$

where R_{dc} is the DC resistance of the spiral, given by:

$$R_{dc} = \frac{\rho \times l_{\text{trace}}}{w_{\text{trace}} \times t} \tag{2.4}$$

and f_b is the frequency at which the skin depth is equal to the thickness of the trace, given by:

$$f_b = \frac{\rho}{t^2 \pi \mu_0} \tag{2.5}$$

The DC resistance (Eqn. 2.4) is proportional to the resistivity (ρ) of the trace metal ($2.44\times10^{-8}\ \Omega m$ for gold) and the overall length of the trace (l_{trace}, roughly proportional to number of turns and outer segment length), and inversely proportional to both the width (w_{trace}) and thickness (t) of the trace. Finally, f_b is proportional to the resistivity of the trace metal and inversely proportional to the square of the trace thickness (t).

This model allows for the design of a low-loss spiral at a given frequency. To minimize the loss, R_{dc} must be minimized through the width of the trace (w_{trace}), the number of turns (N), and the outer segment length. Since the trace thickness is standard for the given process, f_b is fixed ($\sim$0.4 GHz).

2.1.2 Parallel Equivalent Model

In terms of the first order model developed above, designing a smaller spiral would lead to a smaller series resistance. Indeed, if such spirals were used in series with other elements for applications such as matching networks, feedback, or degeneration, the use of smaller spirals with less series resistance would obviously be advantageous. However, when using these spirals in parallel with a capacitor to form a parallel LC resonator, it will be the *parallel equivalent resistance* of the spiral (R_p), not the series resistance, that will determine the loss at the resonance point. Thus, the first order model must be

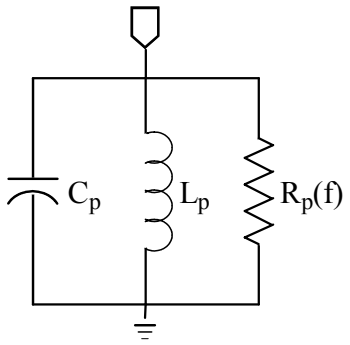


Figure 2.2: Parallel equivalent first order model of spiral inductor.

modified in order to find the parallel equivalent resistance of each spiral.

The first step in transforming the model in Figure 2.1(b) to a parallel equivalent model (Fig. 2.2) is to compute the quality factor (Q) of the series L-R branch using [3]:

$$Q_s(f) = \frac{X_s(f)}{R_s(f)} = \frac{2\pi f L_s}{R_s(f)} \tag{2.6}$$

Next, the parallel equivalent resistance, R_p, is computed as follows:

$$R_p(f) = \left[Q_s^2(f) + 1\right] R_s(f) \tag{2.7}$$

$$R_p(f) = \left[\frac{(2\pi f L_s)^2}{R_s^2(f)} + 1\right] R_s(f) \tag{2.8}$$

$$R_p(f) = \frac{(2\pi f L_s)^2}{R_s(f)} + R_s(f) \tag{2.9}$$

Finally, the parallel equivalent inductance, L_p, is computed with:

$$L_p = L_s \left[\frac{Q_s^2(f) + 1}{Q_s^2(f)}\right] \tag{2.10}$$

To illustrate the implications of these results, the parallel equivalent resistance (R_p) of a spiral with L_s=1 nH and R_s=1 Ω and a spiral with L_s=2 nH and R_s=2 Ω are compared in Figure 2.3. Despite having a larger series resistance, the 2 nH inductor has a *larger* R_p than the 1 nH inductor. Furthermore, the resulting parallel resistance has

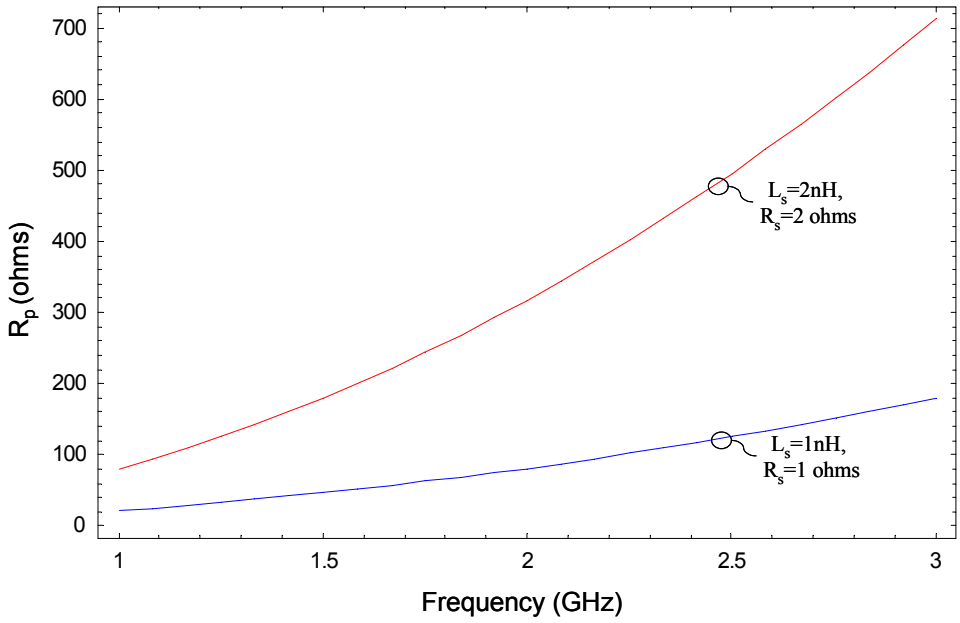


Figure 2.3: Parallel equivalent resistance comparison.

a minimum at DC and increases with frequency, since the original series resistance is in series with an inductive impedance that increases with frequency. Therefore, although perhaps counterintuitive, achieving a large R_p requires a high inductor value despite an increased series resistance inherent to a larger spiral .

2.2 Spiral Inductor Structure Comparison

The two standard spiral inductors modeled and available for use with the M/A-COM E/D SAGFET process include: (1) a single layer, plated spiral; and, (2) a multi-layer, stacked spiral. These spirals are designed for a 10 mil (250 μm) GaAs substrate with no backside metal. The gap width between traces is standardized to 6 μm. For each of these structures, the width of the spiral trace, outer segment length of the spiral, and number of turns can be chosen by the designer. Simulated results (August 2000 models) will be presented in order to compare these structures. These results are obtained by simulating the one-port input impedance of each spiral with one terminal grounded [Fig. 2.2(b) and 2.2], from which the inductance [both series (L_s) and parallel (L_p)], resistance [both series (R_s) and parallel (R_p)], unloaded Q, and self-resonant frequency can be calculated.

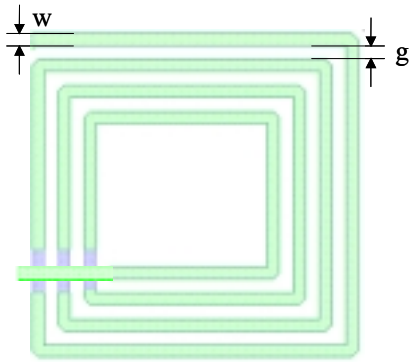


Figure 2.4: Plated spiral structure.

2.2.1 Single Layer, Plated Spirals

The single layer, plated spiral is a basic structure typically used to obtain maximum inductance with minimal loss. In this structure (Figure 2.4), the top and bottom metal layers are placed on top of each other in order to maximize the thickness of the trace. By increasing the trace width, the cross sectional area of the trace is maximized in order to minimize the loss of the spiral. However, the primary drawback of this structure is that it consumes a large amount of die area.

2.2.2 Multi-Layer, Stacked Spiral

The multi-layer, stacked spiral is an inductor structure motivated by the need to reduce the die area required for a given amount of inductance. In this structure (shown in Figures 2.5 and 2.6) die area is decreased by effectively placing two smaller spiral inductors (each on a different metal layer) in series in order to generate the required inductance [16]. As the figures illustrate, the multi-layer inductor is actually broken up into a number of alternating single turn spiral segments in series with each other in order to minimize the parasitic capacitive effect. While this structure does reduce the die area consumed by the spiral, this comes at the expense of increased loss. By separating the two layers, the metal trace thickness and corresponding cross-sectional area for each layer of the spiral are decreased, leading to an overall increase in series resistance (Eqn. 2.3.)

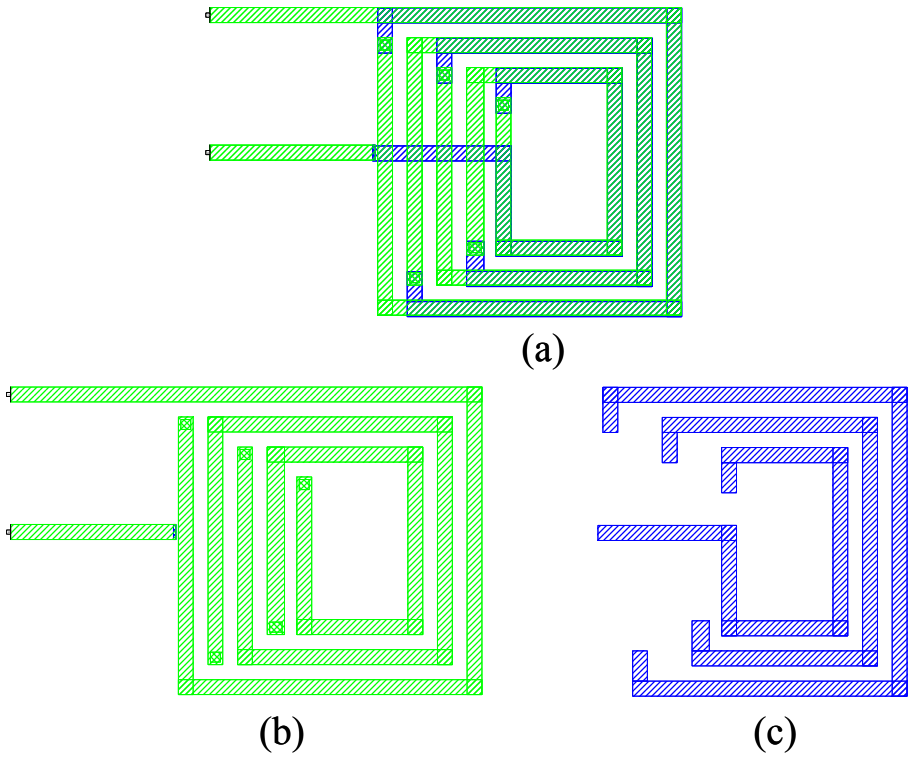


Figure 2.5: Stacked spiral structure, top view: (a) Both layers; (b) Top metal layer; (c) Bottom metal layer.

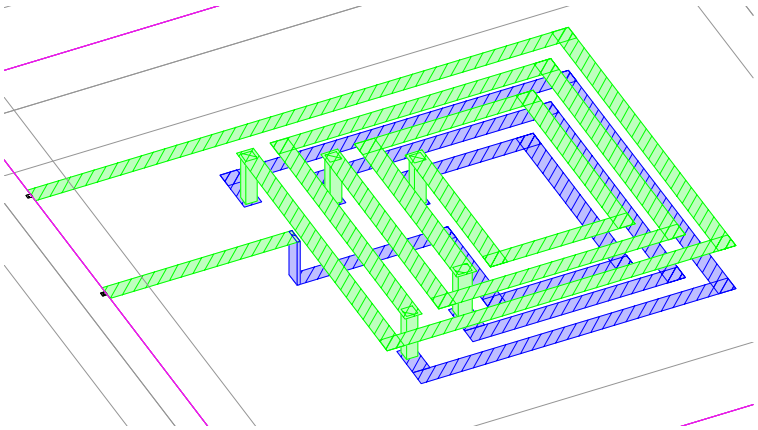


Figure 2.6: Stacked spiral structure: Iso view.

2.2.3 Structural Comparison

The two inductor structures were evaluated based on a 3 nH design. Each structure used the same number of turns (3.75) in order to provide a fair comparison between the size, capacitive parasitics, and loss of each structure. Furthermore, in order to compare the effects of the trace width on the loss for each structure, two variations of each spiral were designed: one with w=6μm and the other with w=15 μm. The resulting physical parameters for these spiral are shown in Table 2.1.

Table 2.1: Spiral structure comparison: Physical parameters

Structure	N (Turns)	Outer Segment Size (μm)	Die Area (μm^2)
Single Layer, W=6 μm	3.75	175	30,625
Single Layer, W=15 μm	3.75	240	57,600
Multi-Layer, W=6 μm	3.75	135	18,225
Multi-Layer, W=15 μm	3.75	180	32,400

From these physical parameters alone, it is evident that the equivalent multi-layer structure is roughly 40% smaller than its single-layer counterpart. In addition, for each structure, reducing the trace width from 15 μm to 6 μm (gap spacing kept constant at g = 6 μm) also decreases the die area by roughly 45%. However, these reductions in die area come at the expense of loss. The simulated series resistance for each of these structures is shown in Figure 2.7, and the parallel equivalent resistance for each structure is shown in Figure 2.8. Figure 2.9 compares the Q for each spiral structure.

These simulated results support two main conclusions. First, the trace width has a more dominant effect on the loss than the structure of the spiral. Second, given the same trace width, the single layer spiral has less loss than the multi-layer spiral below 3 GHz. However, comparing both the single- and multi-layer structures with a trace width of 15 μm, while R_p does decrease (increased loss) by about 10%, the resulting die area decreases by roughly 45%. Consequently, this slight increase in loss may be an acceptable trade-off for reduced die area for some applications.

Finally, a perceived disadvantage of multi-layer spiral structures is that there is more inherent parasitic capacitance since the structure is no longer planar and the traces are placed on top of each other. However, due to the orientation of the trace segments in these multi-layer spirals (Fig. 2.5-2.6), the parasitic capacitance of the multi-layer

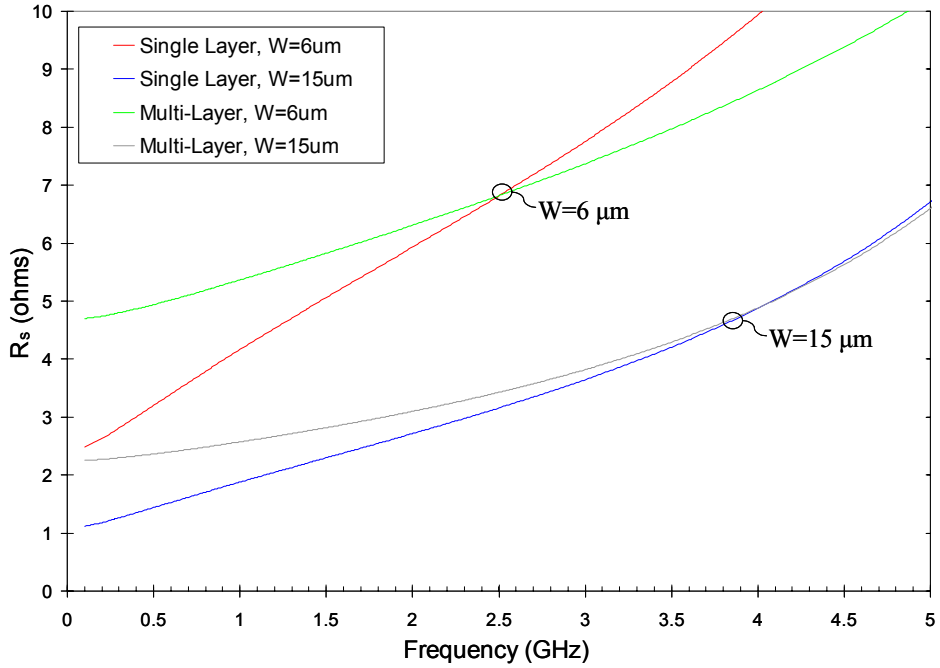


Figure 2.7: 3 nH spiral structure comparison: Simulated series resistance (R_s).

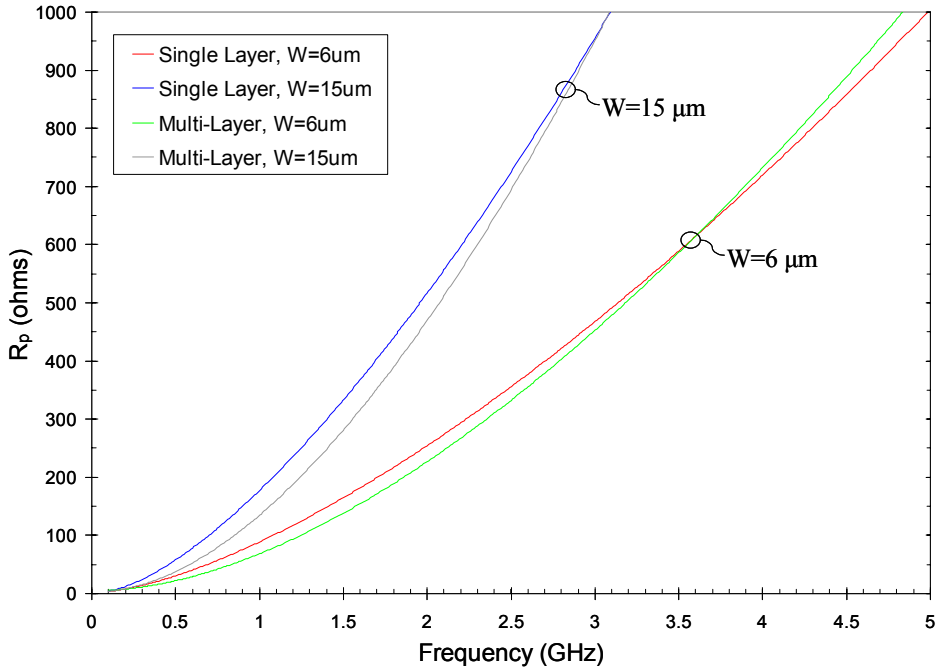


Figure 2.8: 3 nH spiral structure comparison: Simulated parallel equivalent resistance (R_p).

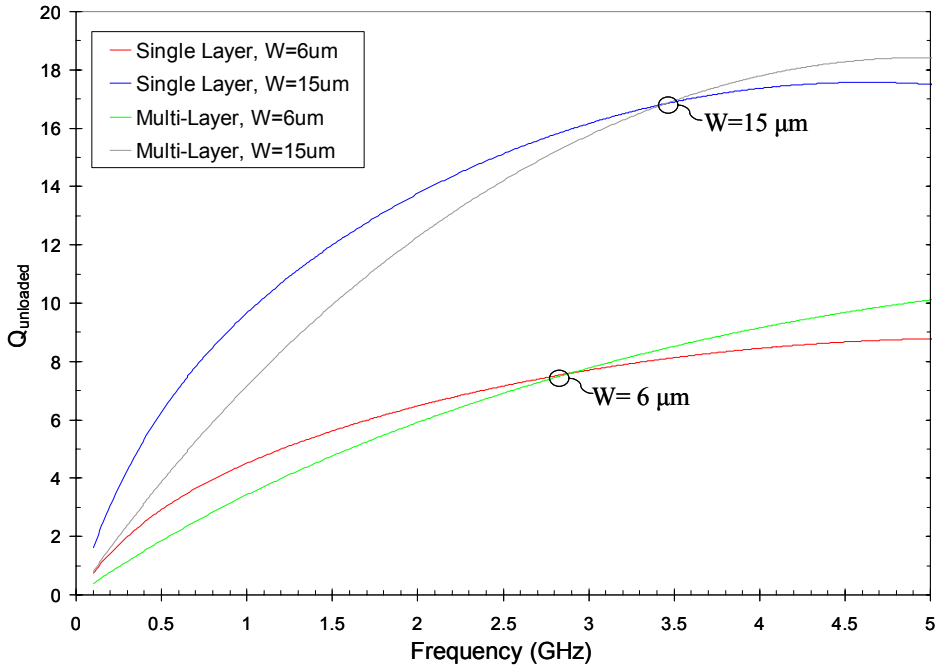


Figure 2.9: 3 nH spiral structure comparison: Simulated Q.

structure, and hence the self resonant frequency (shown in Figure 2.10), is no worse, and in some cases even better, than the equivalent single layer spiral. Therefore, these multi-layer spirals will have as much, and in some cases more, usable frequency range than the equivalent single-layer alternative.

Table 2.2 summarizes the results of this structural comparison. It can be seen that for low loss applications where die area is not restrictive, the single layer structure with a trace width of 15 μm is the best choice. For this reason, as well as concerns about the accuracy of the multi-layer spiral modeling[1], the single-layer spiral inductor structure with w = 15 μm is used in this thesis.

[1]Decision based on December 1999 models that were available during the original design. In retrospect, based on the August 2000 models, the multi-layer spirals are more feasible than were thought at the time of the original design.

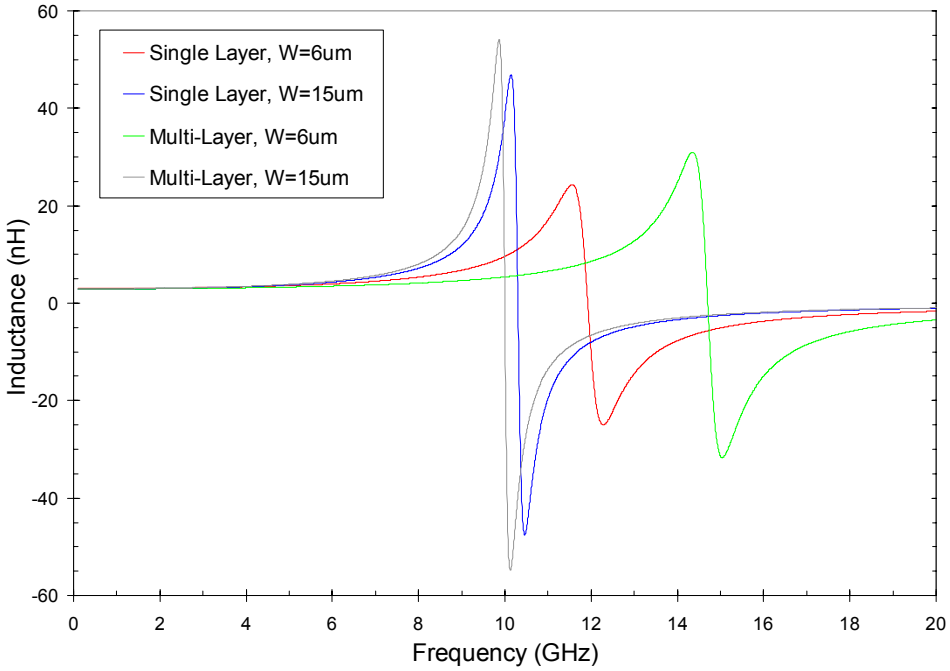


Figure 2.10: 3 nH spiral structure comparison: Self resonance frequency.

Table 2.2: Simulated spiral structure comparison: Electrical properties

Structure	R_p @ 1.88 GHz	$Q_{unloaded}$ @ 1.88 GHz	Self Resonance
Single Layer, W=6 μm	232	6.3	11.92 GHz
Single Layer, W=15 μm	470	13.4	10.31 GHz
Multi-Layer, W=6 μm	204	5.65	14.7 GHz
Multi-Layer, W=15 μm	421	11.75	10 GHz

2.3 Baseline Spiral Inductors

Three baseline spiral inductors were designed (1 nH, 2 nH, and 3 nH) and used exclusively in all subsequent resonator designs. Recognizing that external loading rather than the loss of these inductors will dominate the Q_{loaded} of resonators in a 50 Ω system, low inductor values were chosen in order to maximize Q_{loaded} ($\frac{R_p}{2\pi f L_p}$). However, minimizing the loss of the spiral inductor is still critical in reducing the loss of subsequent resonators, so all three baseline designs use the single layer, plated spiral structure with a conductor width of 15 μm.

The following sections explain the design of the baseline spirals and the subsequent analysis of the parasitics. In addition to the simulated results, measured results for the 1 nH and 2 nH spirals are presented. Test structures were fabricated for the 1 nH baseline spiral inductor (Fig. A.2 in Appendix A) as well as the 2 nH baseline spiral inductor (Fig. A.8 in Appendix A). S_{11} of these inductors was measured measured versus frequency, from which the input impedance (Z_{in}) was calculated. Given Z_{in} which the inductance, resistance, and self-resonant frequency were extracted.

2.3.1 Inductance

Given a specific structure, substrate thickness, gap width, and conductor width of the spiral (specified previously), the two variables available for designing for a desired inductance are the outer segment length and the number of turns. As predicted by Equation 2.1, the resulting inductance of the spiral increases linearly with the outer segment length. However, simulations based on previously modeled results (M/A-COM model library) showed that the resulting inductance only increased linearly with the number of turns, as opposed to the square of the number of turns predicted by Equation 2.1. Furthermore, by increasing the outer segment length or the number of turns in order to increase the inductance, the overall length of the spiral conductor increases, thereby increasing the series resistance. Additionally, increasing the outer segment length of the spiral increases the effective die area consumed by the spiral. While increasing the number of turns per some given outer segment length does not increase the effective die area of the spiral, it will increase the parasitic capacitance as well as the loss of the spiral. Therefore, the design of a spiral to achieve a particular inductance involves a series of trade-offs between

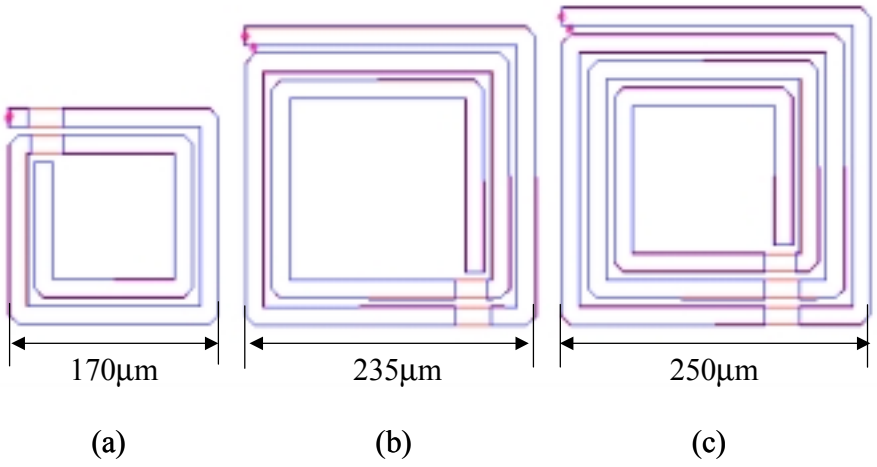


Figure 2.11: Baseline spiral inductor designs: (a) 1 nH (2 turns, 170 μm); (b) 2 nH (2.5 turns, 235 μm); (c) 3 nH (3.5 turns, 250 μm).

loss, parasitic capacitance, and die area.

During the design of the three baseline inductors, consideration of the subsequent resonator design served as guidance in making the trade-offs described above. Loss was the primary concern in the design of the baseline spirals. Beyond loss considerations, preference was given to increasing the outer segment length rather than the number of turns in order to minimize the parasitic capacitance and hence maximize the effective inductance. The resulting designs are show in Figure 2.11. The 1 nH inductor [Fig. 2.11(a)] was designed with a 2 turns and a 170 μm outer segment length. For the 2 nH spiral [Fig. 2.11(b)], the number of turns were increased marginally to 2.5 and the outer segment length was increased to 235 μm. Finally, the 3 nH spiral [Fig. 2.11(c)] was designed with 3.5 turns and a 250 μm outer segment length.

Figure 2.12 shows the simulated series inductance for each of these spirals as well measurements from the one-port spiral test structures mentioned earlier. As shown, the measured series inductance of the 1 nH inductor matched simulation well. However, the measured series inductance of the baseline 2 nH inductor, was roughly 2.5 nH while simulations predicted 2 nH. Unfortunately, this discrepancy was discovered after both the resonators and filters using this inductor had already been fabricated, resulting in a shift in the frequency response of the resonator. The reason for this discrepancy is likely inaccuracies in the model.

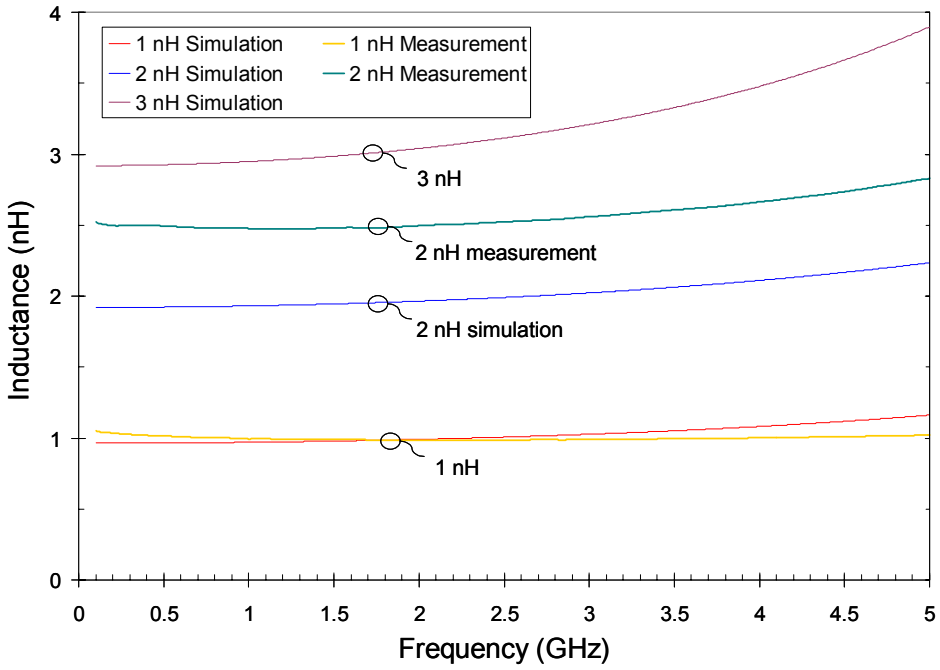


Figure 2.12: Inductance of baseline spirals: Simulations and measurements.

2.3.2 Capacitive Effects

As previously discussed, an advantage of smaller spirals for low inductance values is their lower parasitic capacitance. As a result, these spirals have a high self resonant frequency. Figure 2.13 plots the inductance of the three baseline spirals to 20 GHz to illustrate the frequencies at which each spiral self-resonates. The results for the 1 and 2 nH baseline spirals are measured results from the spiral test structure while the results for the 3 nH baseline spiral are simulated. As predicted, the larger inductors, and hence larger spirals, have a lower SRF than the smaller inductors. All three spirals have a SRF at or above 10 GHz. Therefore, at 1.8 GHz, where the inductance will be critical for the operation of the resonators designed in this thesis, the capacitive effects of the spiral are minimal. Furthermore, the inductance of each spiral is fairly constant about the operating frequency with only the 3 nH design beginning to show an increase above $\backsim$3 GHz (see Figure 2.12)

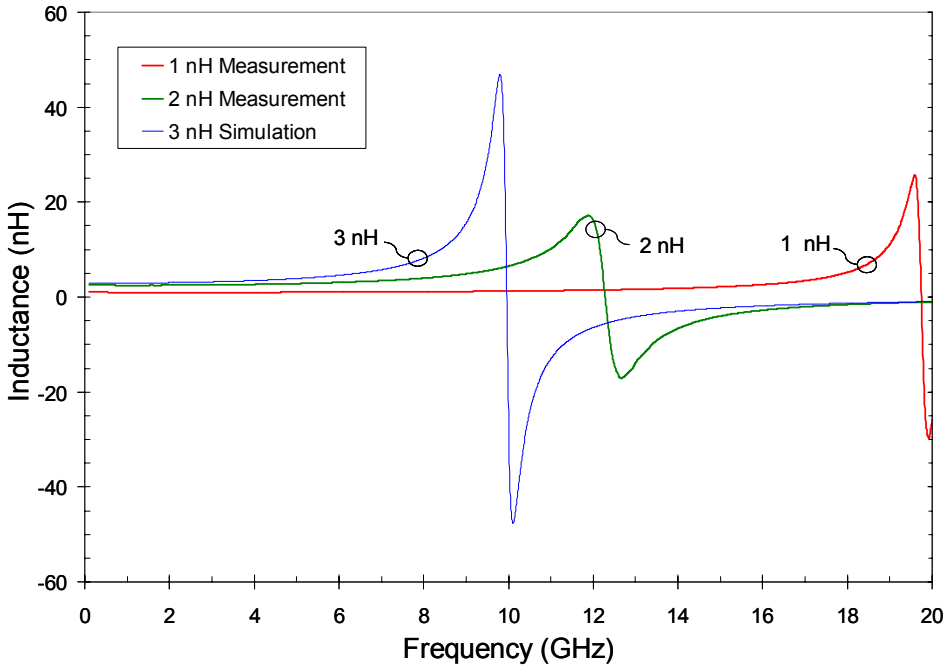


Figure 2.13: Self resonance of baseline spirals (measured for 1 and 2 nH, simulated for 3 nH).

2.3.3 Loss

The last element of the baseline spirals that needs to be accounted for is the loss. For this process, the loss primarily is generated in series with the inductance of the spiral, and therefore can be modeled as a resistor in series with the inductor. However, it is the parallel equivalent resistance of the inductor that will be useful in determining the loss of subsequent parallel resonators. Therefore, as described in Section 2.1.2, the parallel equivalent resistance can be found from the series resistance and the inductance.

Series Resistance

The first step in evaluating the loss of the resonator will be to generate a simpler mathematical model for the series resistance of the spiral inductor. Figure 2.14 shows the simulated series resistance, R_s, in red. As expected, the larger spirals have a larger R_s. Noting that the series resistance appears nearly linear with frequency over the band of interest (1 GHz - 3 GHz), the blue lines in Figure 2.14 represent the following linear

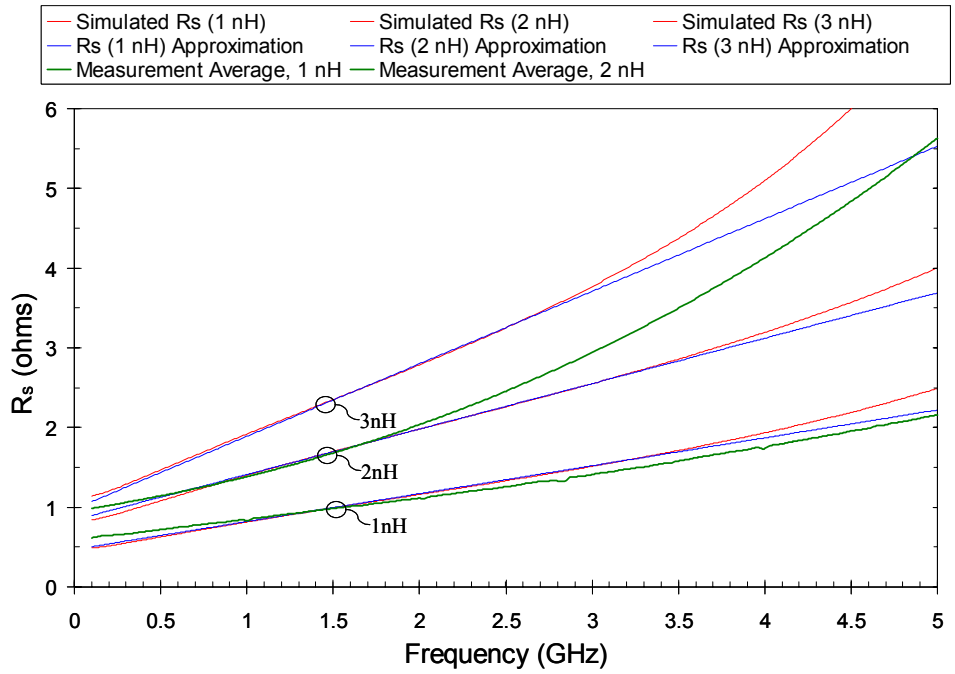


Figure 2.14: Spiral inductor series resistance: Simulation, approximation, and measurement

approximations:

$$1 \text{ nH: } R_s = 0.35 \times f(\text{GHz}) + 0.47, 0.1 \text{ GHz} \leq f \leq 4 \text{ GHz} \tag{2.11}$$

$$2 \text{ nH: } R_s = 0.57 \times f(\text{GHz}) + 0.84, 0.1 \text{ GHz} \leq f \leq 4 \text{ GHz} \tag{2.12}$$

$$3 \text{ nH: } R_s = 0.91 \times f(\text{GHz}) + 0.98, 0.1 \text{ GHz} \leq f \leq 3 \text{ GHz} \tag{2.13}$$

Finally, the green lines in Figure 2.14 (for the 1 and 2 nH inductor only) show the measured series resistance from the spiral test structures mentioned earlier. The series resistance of the measured 1 nH spiral matched very well. The measured series resistance of the 2 nH spiral matched the simulation until roughly 2 GHz, at which point it increases beyond what was predicted by simulation. However, for the purposes of this thesis, the series resistance at the center frequency of subsequent resonators (1.88 GHz) is of primary importance, at which point the simulations and measurements agree.

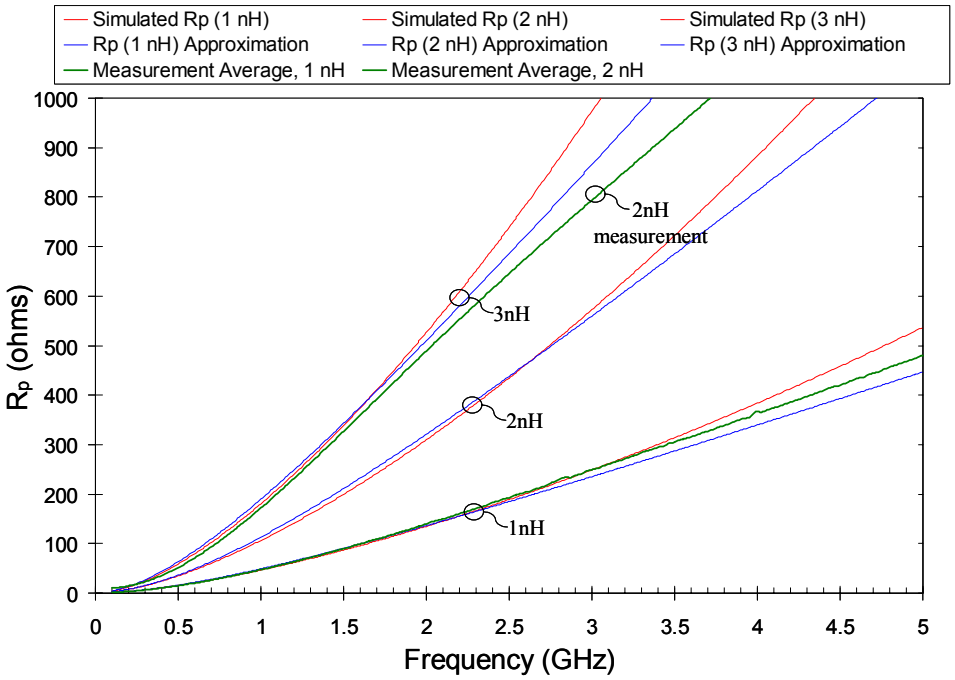


Figure 2.15: Parallel equivalent resistance: Simulation, approximation, and measurement

Parallel Equivalent Resistance

Given the approximations for series resistance (Eqn. 2.11, 2.12 and 2.13) and the series inductance (simulated), the following approximations for the parallel equivalent resistance can be calculated using the procedure discussed in Section 2.1.2 (Eqn. 2.9):

$$1 \text{ nH} : R_p = \frac{39.6 \times f^2(\text{GHz}) + 0.33 \times f(\text{GHz}) + 0.22}{0.35 \times f(\text{GHz}) + 0.47}, 0.1 \text{ GHz} \leq f \leq 4 \text{ GHz} \quad (2.14)$$

$$2 \text{ nH}: R_p = \frac{158.24 \times f^2(\text{GHz}) + 0.96 \times f(\text{GHz}) + 0.71}{0.57 \times f(\text{GHz}) + 0.84}, 0.1 \text{ GHz} \leq f \leq 4 \text{ GHz} \quad (2.15)$$

$$3 \text{ nH}: R_p = \frac{356.13 \times f^2(\text{GHz}) + 1.78 \times f(\text{GHz}) + 0.96}{0.91 \times f(\text{GHz}) + 0.98}, 0.1 \text{ GHz} \leq f \leq 3 \text{ GHz} \quad (2.16)$$

Figure 2.15 compares these approximations to the simulated and measured results. These results show that the approximation holds reasonably well to $\backsim$ 2 GHz below the maximum limit of the series resistance (3 GHz for 1 nH and 2 nH, 2 GHz for 3 nH), and is a conservative estimate beyond that. The parallel approximation breaks down before the series approximation because it assumes that the inductance remains constant versus fre-

Table 2.3: Baseline Spirals: Electrical Properties

	(@ 1.88 GHz)			
Structure	L_p	R_p	$Q_{unloaded}$	Self Resonance
1 nH baseline (measured)	1 nH	127 Ω	10.75	19.74 GHz
2 nH baseline (measured)	2.5 nH	452 Ω	15.3	12.3 GHz
3 nH baseline (simulated)	3 nH	479 Ω	13.3	9.96 GHz

quency while, in reality, the inductance slowly increases with frequency due to the affects of the parasitic capacitance (Fig. 2.12). Comparing both the approximation and the simulated results to the measurements, the 1 nH measurements concur with the approximated and simulated results, while the 2 nH measurements were much higher than the approximations and simulations predicted. The discrepancy between the approximation and the measurement of the 2 nH inductor is because the approximation was calculated using an inductance of 2 nH where measurements showed the actual inductance to be 2.5 nH.

2.3.4 Summary of Baseline Spiral Inductors

Table 2.3 summarizes the electrical performance of the three spirals.

Chapter 3

Negative Resistance Circuits

As discussed in the introduction, the goal of "parallel-mode" Q-enhancement is to present a negative resistance in parallel with a lossy resonator. This negative resistance is designed to cancel with parallel equivalent resistance of the resonator to negate the effects of the resonator loss. In Chapter 2, a method of determining the parallel equivalent resistance of the resonator (inductor) was shown. The goal of this chapter is to design a circuit that generates a desired negative resistance. Given that parasitics will be associated with the negative resistance circuit, the circuit can be transformed such that the negative resistance (R_{neg}[1]) is isolated in parallel with the parallel equivalent resistance (R_p) of the resonator.

3.1 Negative Resistance Circuit Topologies

Due to the body of knowledge arising from the design of integrated oscillators, there are a number of well-known negative resistance topologies available to the designer. Given that only GaAs MESFET devices are available in this project, the focus here will be limited to FET topologies.

Common-gate inductive feedback [Fig. 3.1(a)] can be used to generate both the negative resistance and inductance of a Q-enhanced LC resonator [12]. As shown in Figure 3.1(b),

[1]Throughout this chapter and the remainder of this thesis the *magnitude* of the negative resistance (R_{neg}) will be discussed and used in calculations to minimize confusion. All schematics will be labeled with -R_{neg} to account for the negative sign.

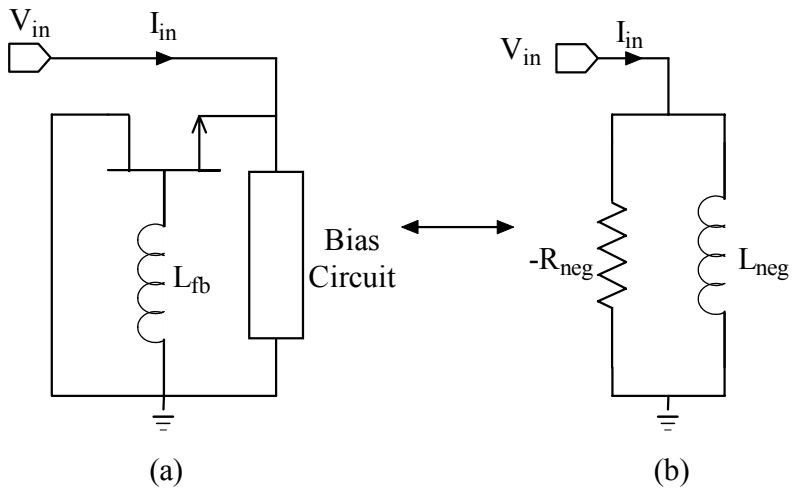


Figure 3.1: Common-gate inductive feedback: (a) Circuit; (b) Equivalent circuit.

the equivalent circuit consists of an inductor in parallel with a negative resistance. This structure has an advantage of being very compact and simple. However, the main restriction to its use is that with the drain of the FET grounded, a negative voltage must be generated at the source to bias the device.

Common-source capacitive feedback is also frequently used to generate negative resistance (Fig. 3.2). In this circuit, negative resistance can be generated at either the gate [Fig. 3.2(a)] or the drain [Fig. 3.2(c)] of the FET. The equivalent circuit for either topology [Fig. 3.2(b)] consists of the negative resistance and a capacitance in series. In cases of wide passband filters, where low-Q resonators allows for a large inductor and small capacitor, this circuit can act as both the negative resistance and the capacitance of the Q-enhanced LC resonator. However, in most cases, this capacitance is too small and only acts to offset the capacitance in the resonator circuit. An additional feature of this circuit is that the negative resistance can be tuned by varying the capacitive feedback (C_{fb}) using a varactor.

For the designs presented in this thesis, the common-source capacitive feedback circuit in Figure 3.2(a) will be used. By generating the negative resistance at the gate, the presence of the bias circuit at the drain and the source should have a minimal impact on the operation of the resonator.

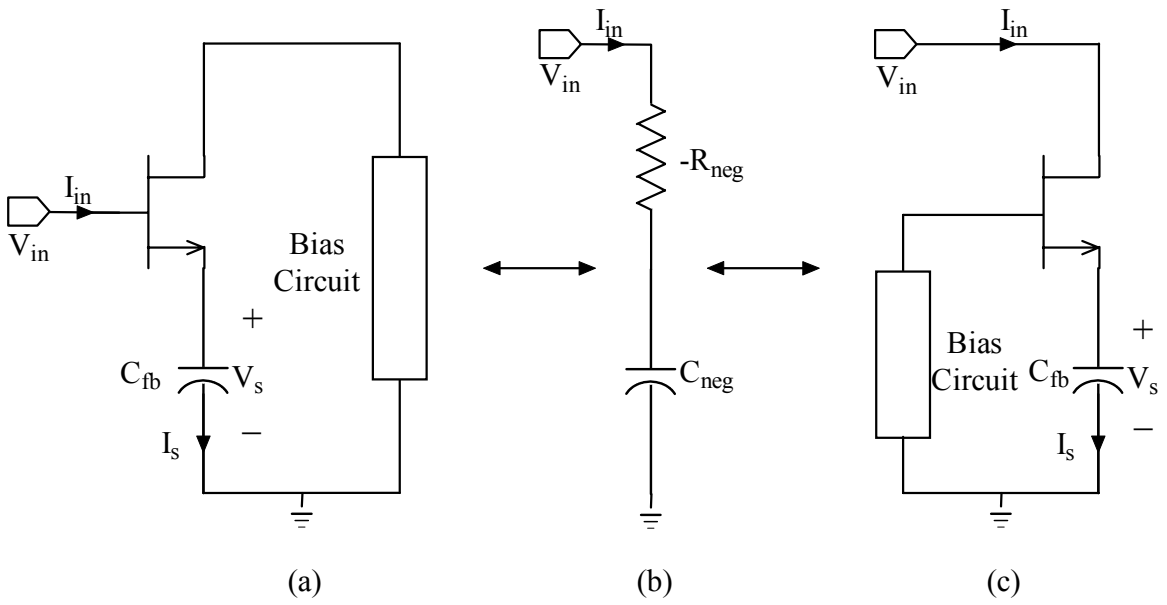


Figure 3.2: Common-source capacitive feedback: (a) Gate output circuit; (b) Equivalent circuit; (c) Drain output circuit.

3.2 Derivation of Common-Source Capacitive Feedback

Given the choice of the common-source capacitive feedback structure [Fig. 3.2(a)], it is useful at this point to derive the input impedance of the negative resistance circuit. From the input impedance, the magnitudes and dependencies of both R_{neg} and C_{neg} can be found. For the purposes of this derivation, the FET will be replaced by a small-signal equivalent circuit and the effects of the bias circuit will be ignored. The resulting circuit is shown in Figure 3.3 [17] where the circuit elements inside the box represent the small signal equivalent circuit of the FET.

Given the definitions of V_{in}, I_{in}, V_s, and I_s (all small-signal quantities) shown in Figure 3.3, the derivation of the input impedance (Z_{in}) is as follows [17]:

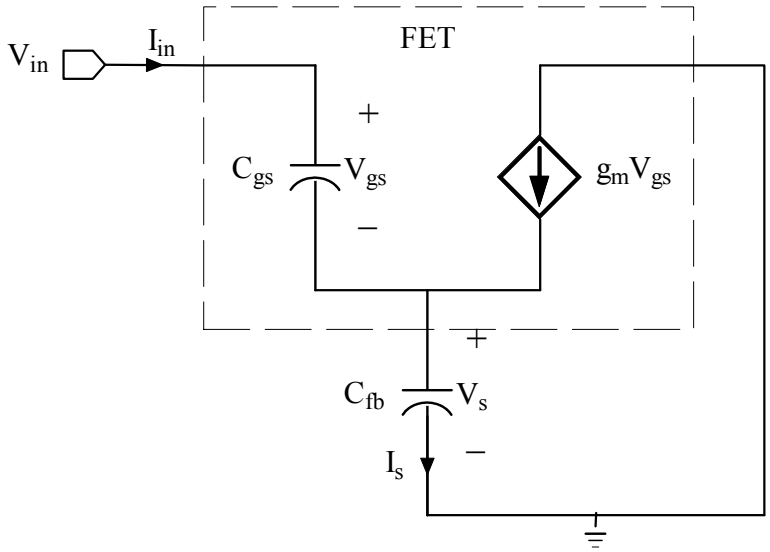


Figure 3.3: Common-source capacitive feedback: Small-signal equivalent circuit.

$$
\begin{aligned}
V_{in} &= V_{gs} + V_s \\
I_{in} &= I_s - g_m V_{gs} \\
V_s &= I_s \frac{1}{j\omega C_{fb}} \\
V_{gs} &= I_{in} \frac{1}{j\omega C_{gs}} \\
V_{in} &= I_s \frac{1}{j\omega C_{fb}} + I_{in} \frac{1}{j\omega C_{gs}} \\
I_{in} &= I_s - g_m I_{in} \frac{1}{j\omega C_{gs}} \\
I_s &= I_{in} \left(1 + \frac{g_m}{j\omega C_{gs}} \right) \\
V_{in} &= I_{in} \left(1 + \frac{g_m}{j\omega C_{gs}} \right) \frac{1}{j\omega C_{fb}} + I_{in} \frac{1}{j\omega C_{gs}} \\
Z_{in} &= \frac{V_{in}}{I_{in}} = \left(1 + \frac{g_m}{j\omega C_{gs}} \right) \frac{1}{j\omega C_{fb}} + \frac{1}{j\omega C_{gs}} \\
Z_{in} &= -\frac{g_m}{(2\pi f)^2 C_{gs} C_{fb}} - j \left(\frac{1}{\omega C_{gs}} + \frac{1}{\omega C_{fb}} \right)
\end{aligned}
\tag{3.1}
$$

Therefore, the resulting input impedance is composed of a negative real impedance and a negative (capacitive) imaginary impedance. Correlating this result to the equivalent circuit shown in Figure 3.2(b), the resulting expressions for R_{neg} and C_{neg} are:

$$R_{neg} = \frac{g_m}{(2\pi f)^2 C_{gs} C_{fb}} \tag{3.2}$$

$$C_{neg} = \frac{C_{gs} C_{fb}}{C_{gs} + C_{fb}} \tag{3.3}$$

Ignoring for the moment any frequency dependence of g_m or C_{gs}, the resulting negative resistance is equal to the transconductance (g_m) of the FET times the reactances of both C_{gs} and C_{fb}. Therefore, an optimal negative resistance circuit would allow for a large transconductance (g_m) and a small parasitic capacitance (C_{gs}). Unfortunately these two parameters cannot be optimized at the same time. In order to generate a large transconductance (g_m), a large FET must be used. However, a large FET will inherently have larger parasitics, resulting in a larger C_{gs}. Therefore, designing the FET in this circuit for maximum negative resistance will be a trade-off between maximizing g_m and minimizing C_{gs}. Fortunately, the value of the source feedback capacitor (C_{fb}) is another variable available to design for a desired negative resistance.

The resulting equivalent capacitance (C_{neg}) is simply the series equivalent capacitance of C_{gs} and C_{fb}. In order to minimize capacitive effects on the resonator, C_{neg} should be large, and hence have a small impedance. However, due to the relative sizes of C_{gs} ($\sim$.75 pF) to C_{fb} (on the order of 10 pF), the resulting capacitance will be dominated by C_{gs} and thus be small. C_{neg} will become a critical factor in determining the parallel equivalent negative resistance, as well determining the center frequency of subsequent Q-enhanced resonators.

3.3 Modified Common-Source Capacitive Feedback

Beyond the small-signal design, previous results [18] have shown that the linearity of the negative resistance circuit is strongly dependent on the value of the source feedback capacitor (C_{fb}) and the gate-to-source capacitance of the FET. Theoretical and experi-

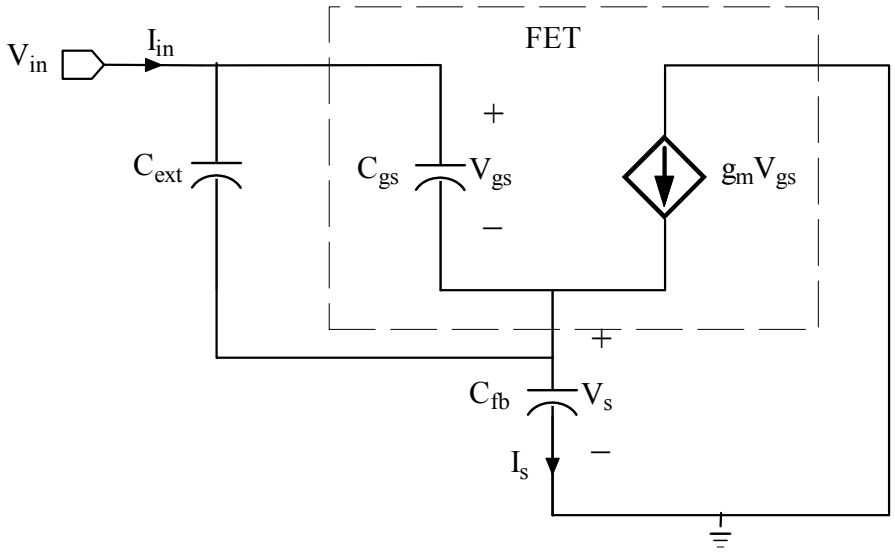


Figure 3.4: Modified common-source capacitive feedback: Small-signal equivalent circuit.

mental results have shown that linearity of the negative resistance circuit is improved by reducing the source feedback capacitance (C_{fb}) and increasing the gate-to-source capacitance.

However, there are small-signal consequences to these changes, specifically in terms of the resulting negative resistance (R_{neg}). Increasing the gate-to-source capacitance would imply choosing a larger FET, resulting in a larger transconductance (g_m) and larger R_{neg}. Therefore, increasing the size of the FET (hence increasing g_m and C_{gs}) and decreasing the source feedback capacitor (C_{fb}) to improve the linearity would also increase R_{neg} and C_{neg}. To alleviate this trade-off, a second capacitor can be added to the circuit between the gate and the source (C_{ext} in Figure 3.4) in order to effectively increase the gate-to-source capacitance without increasing the size of the FET. This addition will modify the expressions for Z_{in}, R_{neg}, and C_{neg} to:

$$Z_{in} = -\frac{g_m}{(2\pi f)^2 (C_{gs} + C_{ext}) C_{fb}} - j \left[\frac{1}{2\pi f (C_{gs} + C_{ext})} + \frac{1}{2\pi f C_{fb}} \right] \tag{3.4}$$

$$R_{neg} = \frac{g_m}{(2\pi f)^2 (C_{gs} + C_{ext}) C_{fb}} \tag{3.5}$$

$$C_{neg} = \frac{(C_{gs} + C_{ext})C_{fb}}{C_{gs} + C_{ext} + C_{fb}} \tag{3.6}$$

Adding gate to source capacitance (C_{ext}) effectively introduces a free variable into the expressions for both R_{neg} and C_{neg}. The addition of C_{ext} in the denominator of R_{neg} will allow the source feedback capacitor (C_{fb}) to be decreased and will effectively increase the gate-to-source capacitance without changing the FET size. This leads to decreased distortion and gain compression without changing the FET size or the resulting negative resistance. Furthermore, adding C_{ext} will increase the resulting C_{neg} and hence decrease the resulting impedance and capacitive effects.

3.4 Parallel Equivalent Model

The parallel equivalent negative resistance ($R_{p,neg}$) must be found in order to understand how much of the loss of the inductors can be negated by a particular negative resistance circuit. Furthermore, while little attention was paid to the parallel equivalent inductance of the inductors due to their relatively high Q ($L_p \approx L_s$), determining the parallel equivalent capacitance of the negative resistance circuit is critical as it will affect the resonance frequency of a Q-enhanced LC resonator. It is therefore useful to convert to a parallel equivalent model (Fig. 3.5).

The first step is to compute the series Q of the negative resistance circuit [3]:

$$Q_s(f) = \frac{X_s(f)}{R_s(f)} = \frac{\frac{1}{2\pi f C_{neg}}}{R_{neg}(f)}$$

where R_{neg} and C_{neg} are given by Equations 3.5 and 3.6, respectively. Simplifying this expression:

$$Q_s(f) = \frac{2\pi f\,(C_{gs} + C_{ext} + C_{fb})}{g_m} \tag{3.7}$$

Unlike the inductors where a high Q was preferred in order to minimize the loss, for the negative resistance circuit, a low Q (ideally 0) is preferred in order to generate the maximum negative resistance. Therefore, Equation 3.7 suggests using small capacitors

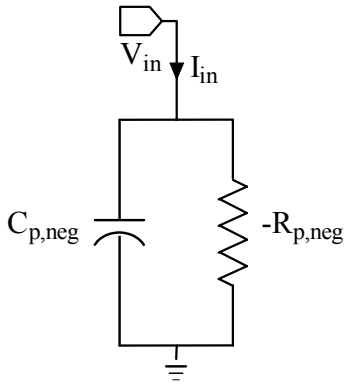


Figure 3.5: Parallel equivalent negative resistance circuit.

and a large FET just as in Equation 3.5.

Given the Q, the parallel equivalent negative resistance can by found by:

$$
\begin{aligned}
R_{p,neg}(f) &= [Q_s^2(f)+1]R_{neg}(f) \\
R_{p,neg}(f) &= \left[\frac{(\frac{1}{2\pi f C_{neg}})^2}{(R_{neg}(f))^2}+1\right]R_{neg}(f) \\
R_{p,neg}(f) &= \frac{1}{R_{neg}(f)\left(2\pi f C_{neg}\right)^2}+R_{neg}(f) \\
R_{p,neg}(f) &= \frac{1}{R_{neg}(f)\left(2\pi f C_{neg}\right)^2}+R_{neg}(f) \\
R_{p,neg}(f) &= \frac{g_m}{(2\pi f)^2\left(C_{gs}+C_{ext}\right)C_{fb}}+\frac{\left(C_{gs}+C_{ext}+C_{fb}\right)^2}{g_m(C_{gs}+C_{ext})C_{fb}}
\end{aligned}
\tag{3.8}
$$

The resulting expression (Eqn. 3.8), though not in its simplest form, offers some insight into the mechanics of the transformation. Rewriting this equation:

$$
R_{p,neg}(f) = R_{neg}(f)+\frac{\left(C_{gs}+C_{ext}+C_{fb}\right)}{g_m C_{neg}} \tag{3.9}
$$

This expression (Eqn. 3.9) shows that only the first term (R_{neg}) dependents on frequency. Therefore the parallel equivalent negative resistance will have the same general response

versus frequency as the series negative resistance, but offset by the the second term.

Finally, the expression to transform C_{neg} into its parallel equivalent is [3]:

$$C_{p,neg} = C_{neg}\left(\frac{Q_s^2(f)}{Q_s^2(f)+1}\right) \tag{3.10}$$

Unfortunately, the expression does not simplify to a form that offers much additional insight. However, so long as the value of $C_{p,neg}$ is known, when the negative resistance circuit is used to Q-enhance a resonator, the resonator capacitance can be decreased by $C_{p,neg}$ to compensate and achieve the desired center frequency.

3.5 Design Trade-offs

Now that an expression for the parallel equivalent negative resistance has been found, an example will be presented to show how the different design parameters (FET size, C_{fb}, C_{ext}) affect the response of the parallel equivalent negative resistance. Figure 3.6 compares the parallel equivalent negative resistance of each of the following four circuits:

1. *Baseline Circuit*: Baseline FET (g_m=0.1 mS, C_{gs}=1 pF), C_{ext}=1 pF, C_{fb}=10 pF
2. *Smaller FET*: Smaller FET (g_m=0.05 mS, C_{gs}=0.5 pF), C_{ext}=1 pF, C_{fb}=10 pF
3. *Reduced C_{ext}*: Baseline FET (g_m=0.1 mS, C_{gs}=1 pF), C_{ext}=0.5 pF, C_{fb}=10 pF
4. *Reduced Feedback*: Baseline FET (g_m=0.1 mS, C_{gs}=1 pF), C_{ext}=1 pF, C_{fb}=5 pF

The results in Figure 3.6 offer a number of insights into the generated R_{neg} (Eqn. 3.5) and its transformation across C_{neg} into $R_{p,neg}$ (Eqn. 3.9). Comparing the circuit with the reduced FET size (#2) to the baseline (#1), g_m proves dominant over C_{gs} and increases the parallel equivalent negative resistance (degraded loss reduction) as predicted by Equation 3.5. However, when comparing the circuits with a reduced C_{ext} (#3) and reduced C_{fb} (#4) to the baseline (#1), the parallel equivalent negative resistance increased (degraded loss reduction) despite an increase in R_{neg} (Eqn. 3.5). Therefore, for circuits #3 and #4, the series to parallel conversion across C_{neg} had more of an effect on $R_{p,neg}$ than the change in R_{neg}.

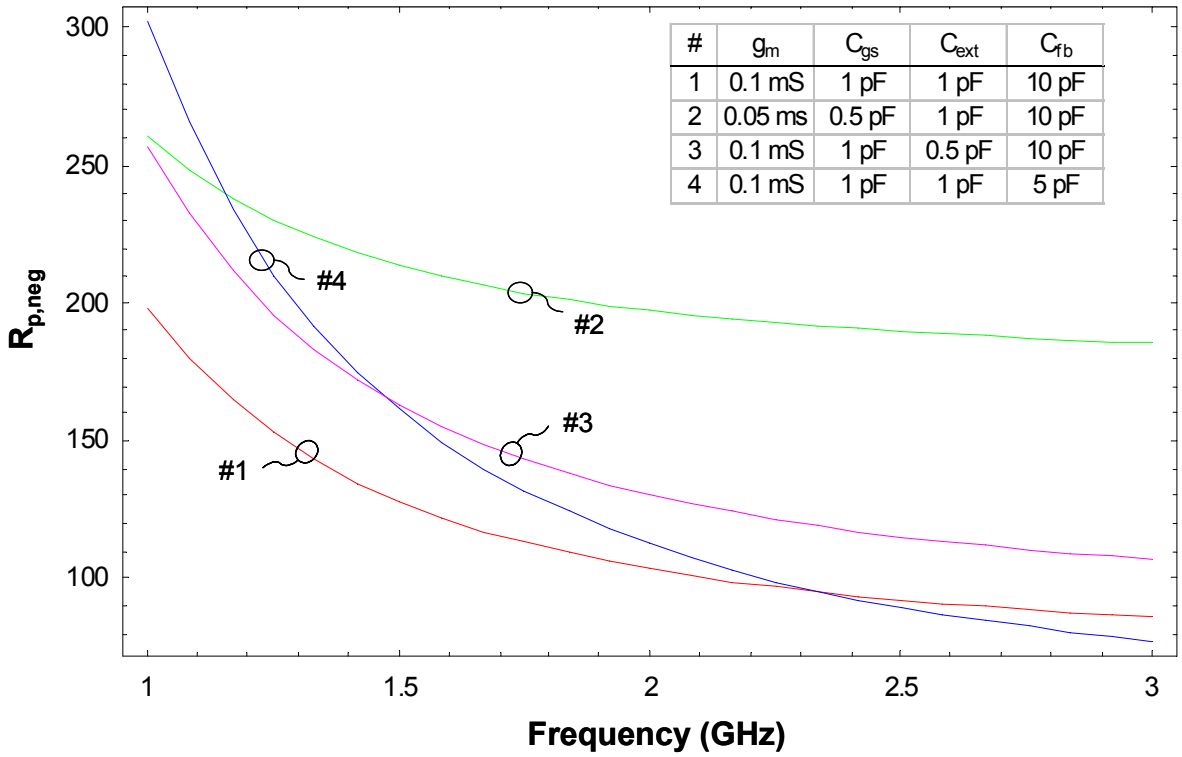


Figure 3.6: Parallel equivalent negative resistance frequency response.

Chapter 4

Q-Enhanced Resonators

Now that negative resistance circuits capable of offsetting the loss of monolithic inductors have been studied, LC resonators can be designed and then Q-enhanced using this technique. This chapter will discuss the design process for Q-enhancing resonators as well as present measured results of Q-enhanced LC resonators fabricated as part of this thesis.

Before continuing, it is important to distinguish between a single-port parallel resonator and the two-port, single-resonator filter which can be used to show the insertion loss, selectivity, and frequency response of the shunt resonator. The single-port resonator itself has a frequency response, characterized by S_{11}, which contains information about the loss and the nature of the reactance of the resonator. However, the corresponding 2-port insertion loss and selectivity are not obvious from the 1-port characterization. Therefore, to illustrate the effects of the resonator loss on insertion loss and selectivity, the resonator is implemented as a shunt device in a 2-port structure (Figure 4.1). A parallel resonance creates a pole and a series resonance creates a zero in the frequency response of this filter. Single-resonator filters corresponding to each resonator structure studied in this chapter will be used to compare the insertion loss, selectivity, and general frequency response of each resonator.

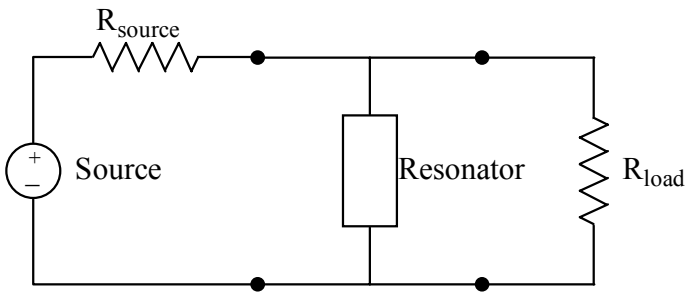


Figure 4.1: Single-resonator filter structures.

4.1 Design Procedure

The first step in designing Q-enhanced resonators is to design the passive resonator circuit. Three LC resonator structures are introduced along with the relevant design equations in Section 4.1.1. In Section 4.1.2, the loss of each resonator is derived. Knowledge of the loss of each resonator structure is a prerequisite for the design of the negative resistance circuit. Section 4.1.3 compares the three resonator structures on the basis of loss, loading effects, and the resulting selectivity of a single-resonator filter based on each resonator. Section 4.1.3 also establishes a baseline design for each resonator, which will allow the performance of Q-enhanced designs to be evaluated. In Section 4.1.4, negative resistance circuits are designed to completely compensate for the loss of each of the resonator structures. Finally, simulated results of fabricated Q-enhanced resonators, are presented in Section 4.1.5.

4.1.1 Resonator Structures and Design

Three resonator structures were analyzed and Q-enhanced as part of this thesis. The three structures are shown in Figure 4.2.

Given the desired parallel resonance frequency, the design of each resonator simplifies to the equation for parallel resonance:

$$f_0 = \frac{1}{2\pi\sqrt{L_p C_p}} \tag{4.1}$$

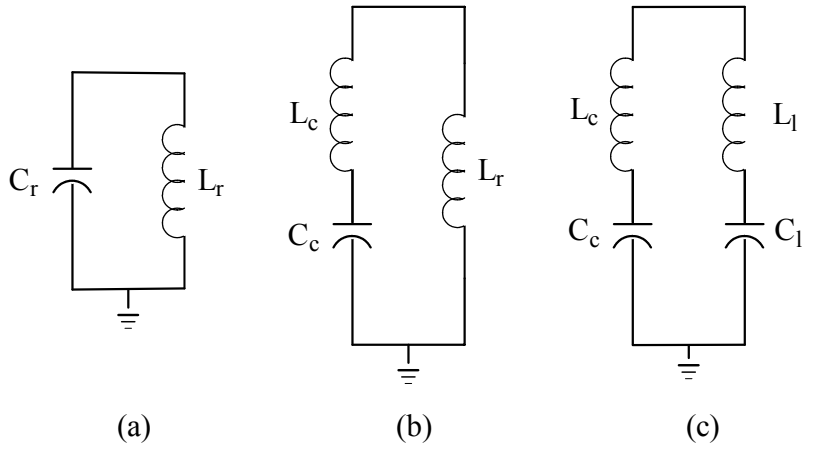


Figure 4.2: Passive resonator structures: (a) Single-pole; (b) Pole-zero; (c) Zero-pole-zero.

However, the manner in which L_p and C_p are synthesized depends on the particular resonator structure.

For simplicity, values of L_p are limited to the baseline values introduced in Chapter 2.

Single-Pole LC Resonator

The first resonator, which will be referred to as a single-pole resonator, consists simply of an inductor (L_r) and a capacitor (C_r) in parallel [Figure 4.2(a)]. The resonating mechanism in this case is simply the parallel resonance between L_r and C_r, which creates a pole in the response of a single-resonator filter based on this resonator structure.

Equation 4.1 completely describes the design where $L_p = L_r$ and $C_p = C_r$. Given the value of the inductor (L_r), Equation 4.1 can be rewritten as:

$$C_r = \frac{1}{(2\pi f_0)^2 L_r} \tag{4.2}$$

to determine the value of the capacitor (C_r).

For this thesis, two baseline single-pole resonators were designed using the 1 and 2 nH baseline inductors. In order to resonate at 1.88 GHz, the required capacitor values are 7.2 and 3.6 pF, respectively. These inductor values were chosen to illustrate the trade-off between the loaded Q of the resonator (introduced in Section 1.2 and discussed below)

and the loss of the resonator (discussed below). The 2 nH resonator should have less loss due to the larger parallel equivalent resistance (as discussed in Chapter 2), but due to the dominant effect of loading on the resonator, the 1 nH resonator will have a higher loaded Q.

Pole-Zero LC Resonator

The second resonator, which will be referred to as a pole-zero resonator, consists of an inductor (L_r) placed in parallel with an inductor (L_c) and capacitor (C_c) in series [Figure 4.2(b)]. In order for this structure to parallel resonate, the reactance of the capacitive arm of the resonator (L_c and C_c in series) must be equal to the negative of the reactance of L_r at the parallel resonance frequency:

$$2\pi f_0 L_c - \frac{1}{2\pi f_0 C_c} = -2\pi f_0 L_r \tag{4.3}$$

In addition, L_c and C_c will resonate in series, introducing a transmission zero into the response of the of the resonator. Furthermore, since this series LC will appear capacitive at the parallel resonant frequency, this series resonance will occur at some frequency greater than the parallel resonant frequency. Given L_c and C_c, this series resonance frequency can be found by:

$$f_{s,c} = \frac{1}{2\pi\sqrt{L_c C_c}} \tag{4.4}$$

Based on the choice of L_c and C_c, this series resonance can be designed to reject a particular frequency band (above the pole frequency) or be tuned to a frequency near the pole frequency in order to improve the frequency selectivity of a filters based on this resonator. However, as will be discussed in Section 4.1.2, the choice of L_c and C_c will also affect the loss of the resonator, which will limit how closely the pole and the zero can be placed together.

The baseline pole-zero resonator designed in this thesis uses the 2 nH baseline inductor for L_r, the 3 nH baseline inductor for L_c, and a 1.3 pF capacitor for C_c. While the pole resulting from the parallel resonance is still at 1.88 GHz, there is now a zero created by the series resonance at 2.54 GHz.

Zero-Pole-Zero LC Resonator

Finally, the third resonator structure, which will be referred to as a zero-pole-zero resonator, consists of two sets of series inductors and capacitors are placed in parallel [Figure 4.2(c)]. In order to parallel resonate, the reactance of the capacitive arm of the resonator (L_c and C_c in series) must be equal to the negative of the reactance of the inductive arm of the resonator (L_l and C_l in series) at the parallel resonance frequency:

$$2\pi f_0 L_c - \frac{1}{2\pi f_0 C_c} = -\left(2\pi f_0 L_l - \frac{1}{2\pi f_0 C_l}\right) \tag{4.5}$$

Similar to the pole-zero resonator, the zero-pole-zero resonator will have a zero, due to the series resonance of L_c and C_c, at some frequency above the pole frequency created by the parallel resonance. This series resonant frequency can be found using Equation 4.4.

Furthermore, the zero-pole-zero resonator will have an additional zero, due to the series resonance of L_l and C_l. Since the series combination of L_l and C_l appear inductive at the parallel resonant frequency, this series resonance will occur at a frequency below the pole frequency. This series resonant frequency can be determined by:

$$f_{s,l} = \frac{1}{2\pi\sqrt{L_l C_l}} \tag{4.6}$$

Similar to the pole-zero resonator, each of these series resonances can be selected to reject a certain frequency band on either side of the pole frequency or be tuned near the pole frequency to improve the selectivity of filters based on this resonator. Again, the design of L_c, C_c, L_l, and C_l will also determine the loss of the resonator. Furthermore the proximity of either zero frequency to the pole frequency will be limited by this loss.

The baseline zero-pole-zero resonator used in this thesis was designed with L_l equal to 3 nH, C_l equal to 18 pF, L_c equal to 6 nH, and C_c equal to 0.67 pF. The series combination of L_l and C_l create an effective inductance of 2.6 nH at the pole frequency of the resonator and places the lower zero frequency at 680 MHz. The series combination of L_c and C_c places the upper zero frequency at 2.5 GHz.

4.1.2 Resonator Loss

The next step is to determine the loss of the resonators. Given that the inductors contribute the majority of the loss of these resonators, the contribution of each inductor must be included. The loss of a resonator will be modeled as a resistance in parallel with a lossless resonator. This will determine the negative resistance required to negate the loss of the resonator.

Single-Pole Resonator Loss

Determining the loss of the single-pole resonator is rather straightforward since the inductor is already isolated in parallel. The parallel equivalent resistance of the resonator is equal to the parallel equivalent resistance of the inductor, previously derived in Section 2.1.2

In this thesis, single-pole resonators are designed using the 1 and 2 nH baseline inductors introduced in Section 2.3. The parallel equivalent resistance, plotted as a function of frequency, for each of these inductors (and resonators) is shown in Figure 4.3. The parallel equivalent resistances at 1.88 GHz for the 1 and 2 nH inductors are 123 Ω and 298 Ω, respectively. This results in unloaded Qs of 10.4 and 12.3 respectively at the center frequency.

Pole-Zero Resonator Loss

Deriving the parallel equivalent resistance of the pole-zero resonator is more difficult since there are inductors in both arms of the resonator (L_r and L_c), and L_c is in series with a capacitor (C_c). To find the parallel equivalent resistance of this resonator, the resistance due to L_c must be transformed across the C_c and then combined (in parallel) with the parallel equivalent resistance from L_r (Fig. 4.4). The transformation of the series resistance of an inductor (found in Chapter 2) across a series LC is similar to the series-to-parallel transformation performed on each of the inductors in Section 2.3. The first step is to find the Q of the series elements:

$$Q_s(f) = \frac{|X_s(f)|}{R_s(f)} = \frac{\left|2\pi f L_c - \frac{1}{2\pi f C_c}\right|}{R_{s,L_c}(f)} \tag{4.7}$$

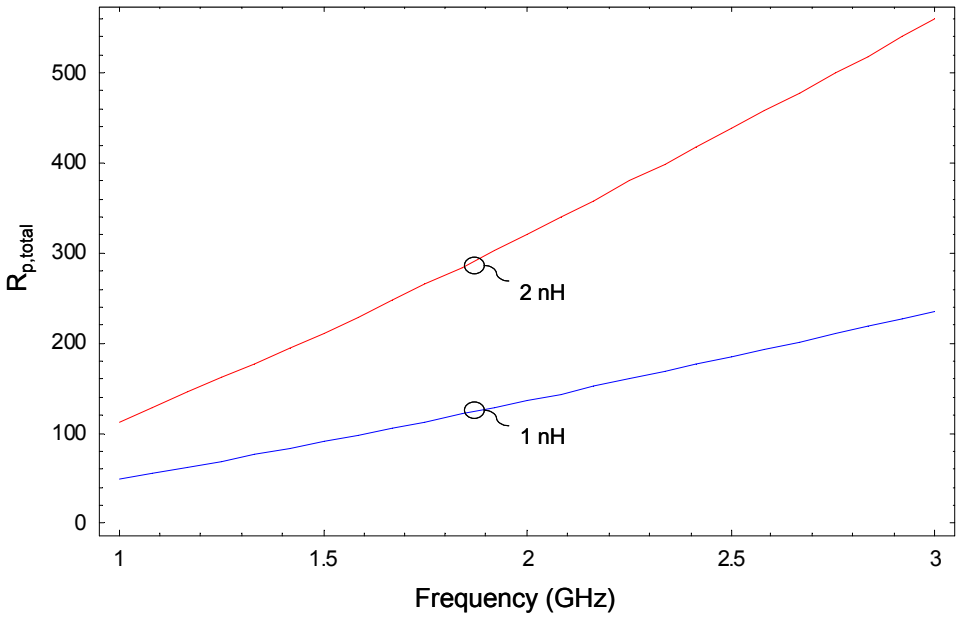


Figure 4.3: Calculated parallel equivalent resistance of 1 and 2 nH single-pole resonators.

Next, the parallel equivalent resistance of the series RLC can be found using [3]:

$$R_{p,L_c}(f) = \left[Q_s^2(f) + 1\right] R_{s,L_c}(f) \tag{4.8}$$

$$R_{p,L_c}(f) = \left[\frac{(2\pi f L_c - \frac{1}{2\pi f C_c})^2}{R_{s,L_c}^2(f)} + 1\right] R_{s,L_c}(f) \tag{4.9}$$

$$R_{p,L_c}(f) = \frac{(2\pi f L_c - \frac{1}{2\pi f C_c})^2}{R_{s,L_c}(f)} + R_{s,L_c}(f) \tag{4.10}$$

Furthermore, with the exception of frequencies near the zero frequency, Q_s will be so large that the parallel equivalent reactance of the series LC will equal to the series reactance. Therefore, the values of L_c and C_c will not change as a result of this transformation.

With the equivalent resistance of the series LC in parallel with the resonator, the overall parallel equivalent resistance of the resonator is given by:

$$R_{p,total} = R_{p,L_c}(f) || R_{p,L_r}(f) \tag{4.11}$$

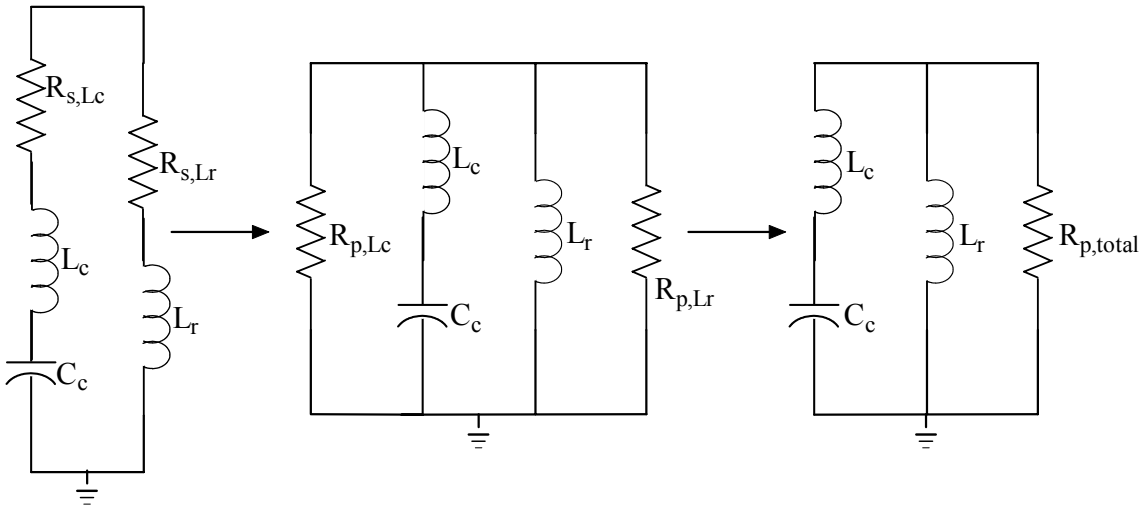


Figure 4.4: Steps in the derivation of the parallel equivalent resistance for the pole-zero resonator.

$$R_{p,total} = \left[\frac{(2\pi f L_c - \frac{1}{2\pi f C_c})^2}{R_{s,L_c}(f)} + R_{s,L_c}(f)\right] || \left[\frac{(2\pi f L_r)^2}{R_{s,L_r}(f)} + R_{s,L_r}(f)\right] \tag{4.12}$$

Therefore, for the pole-zero resonator, the loss of the resonator is affected by each of the inductors (L_l and L_c) as well as C_c. Furthermore, should the value of the capacitor change, the resulting loss will change as well.

Indeed, C_c will change due to the effect of the negative resistance circuit. As was discussed in Chapter 3, there is a capacitance ($C_{p,neg}$) that is generate by the negative resistance circuit used to Q-enhance these resonators. This capacitance will add to the capacitance of the resonator and will consequently shift the center frequency higher. Therefore, to maintain the same center frequency, the capacitance in the resonator must be decreased to compensate. Furthermore, while the capacitance due to the negative resistance circuit itself will not affect the loss of the resonator, the amount by which C_c is reduced to compensate will effect the resonator loss. Therefore, although the original value for C_c was 1.3 pF, to compensate for the capacitance from the negative resistance circuit, C_c is lowered to 0.9 pF. By reducing C_c, the loss of the resonator must be recalculated. Performing this compensation during the passive resonator design allows the negative resistance circuit to be accurately designed for the expected resonator loss (R_p).

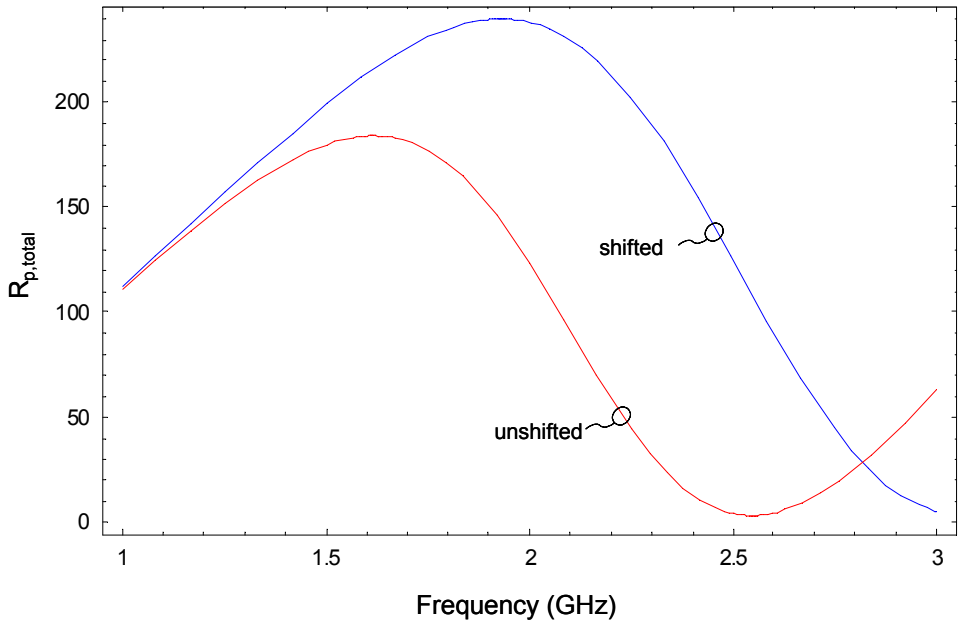


Figure 4.5: Calculated parallel equivalent resistance of 2 nH pole-zero resonator.

Using the series resistance approximations from Chapter 2, the resulting parallel equivalent resistance for both the unshifted (C_c=1.3 pF) and shifted (C_c=0.9 pF) resonators are plotted versus frequency in Figure 4.5. Decreasing C_c in order to pre-shift the resonator response also acts to decrease the overall loss by limiting the effects of the loss of L_c in the transformation. The effect of adding L_c can be seen as the parallel equivalent resistance of the pole-zero resonator peaks near the center frequency of the resonator, leading to a nearly symmetric response. This symmetry will prove to be useful. Furthermore, at the center frequency, adding L_c only reduces the parallel equivalent resistance to 239 Ω (down from 298 Ω in the 2 nH single-pole resonator). The unloaded Q of this resonator at the center frequency is 10.1.

Zero-Pole-Zero Resonator Loss

The derivation of the parallel equivalent resistance for the zero-pole-zero resonator is similar to that of the capacitive arm of the pole-zero resonator; however, now Equation 4.10 must be used for both the inductive and capacitive arms of the resonator. Figure 4.6 illustrates the steps in the derivation of the equivalent resistance of the zero-pole-zero resonator. The first step is to find the parallel equivalent resistance of each arm of the

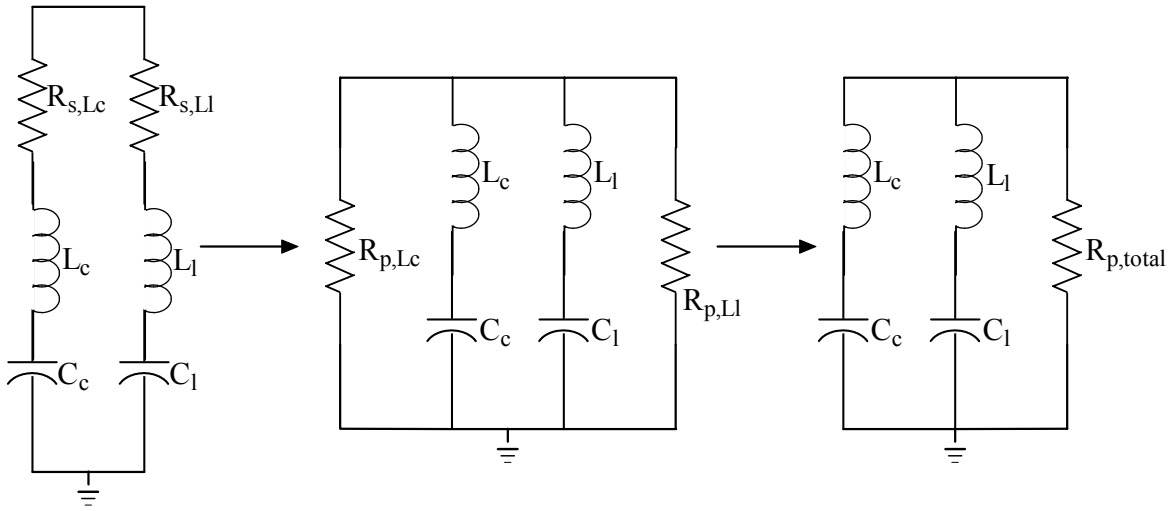


Figure 4.6: Steps in the derivation of the parallel equivalent resistance for the zero-pole-zero resonator.

resonator. Using Equation 4.10, the parallel equivalent resistance of each series RLC is:

$$R_{p,L_c} = \frac{(2\pi f L_c - \frac{1}{2\pi f C_c})^2}{R_{s,L_c}(f)} + R_{s,L_c}(f) \tag{4.13}$$

$$R_{p,L_l} = \frac{(2\pi f L_l - \frac{1}{2\pi f C_l})^2}{R_{s,L_l}(f)} + R_{s,L_l}(f) \tag{4.14}$$

Combining the two resistances in parallel, the resulting parallel equivalent resistance for this resonator structure is:

$$R_{p,total} = \left[\frac{(2\pi f L_c - \frac{1}{2\pi f C_c})^2}{R_{s,L_c}(f)} + R_{s,L_c}(f)\right] || \left[\frac{(2\pi f L_l - \frac{1}{2\pi f C_l})^2}{R_{s,L_l}(f)} + R_{s,L_l}(f)\right] \tag{4.15}$$

Again, the loss of the resonator is a function of each of the inductors and capacitors in the resonator. Thus, as was seen with the pole-zero resonators, it is important to pre-shift the response in order to compensate for the capacitance of the negative resistance circuit. The shifted values are $C_c = 0.4$ pF and $C_l = 18$ pF. Using the series resistance approximations

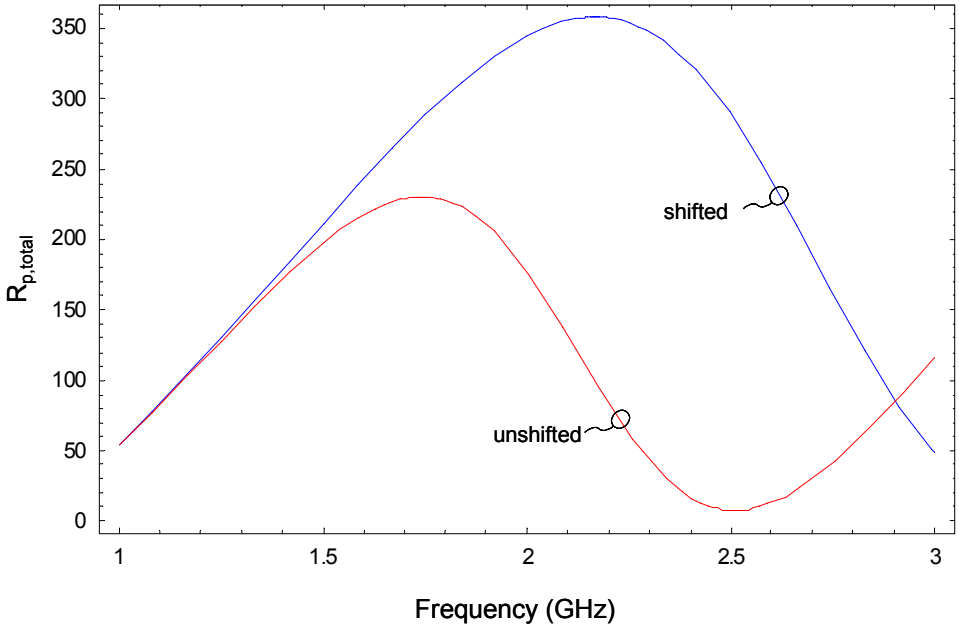


Figure 4.7: Calculated parallel equivalent resistance of 3 nH zero-pole-zero resonator.

Table 4.1: Summary of resonator loss and Q (values @ 1.88 GHz).

Structure	**Inductor Value(s)**	$\mathbf{R}_p$	$\mathbf{Q}_{unloaded}$
Single-Pole	1 nH	123 Ω	10.4
Single-Pole	2 nH	298 Ω	12.3
Pole-Zero	L_r=2 nH, L_c=3 nH	239 Ω	10.1
Zero-Pole-Zero	L_l=3 nH, L_c=6 nH	321 Ω	9.1

[for the 6 nH[1] inductor: $R_s(f) \approx 3f(GHz)$], the parallel equivalent resistance for both the unshifted (C_c=0.67 pF) and shifted (C_c=0.4 pF) resonators are plotted versus frequency in Figure 4.7. Again, decreasing C_c in order to pre-shift the response acts to limit the loss by limiting the effects of R_{s,L_c}. Furthermore, L_c only reduces the parallel equivalent resistance to 321 Ω (down from 479 Ω for the 3 nH inductor alone) at the center frequency. The unloaded Q of this resonator at the center frequency is 9.1.

A summary of the four resonator designs is shown in Table 4.1.

[1]Although this inductor is not one of the original baseline inductors, it was used for L_c in the zero-pole-zero resonator in order to avoid L_c dominating the resonator loss given L_l = 3 nH.

4.1.3 Selectivity and Insertion Loss in a Single-Resonator Filter

Having derived an expression for the loss of each resonator structure, the effects of loading can now be considered. In order to illustrate the effects of loading, single-resonator filters corresponding to each resonator structure (Fig. 4.1), are evaluated in a 50 Ω system. The loaded Q of each resonator can be calculated using:

$$\frac{1}{Q_{loaded}} = \frac{1}{Q_{unloaded}} + \frac{1}{Q_{ext}} \tag{4.16}$$

where Q_{ext} is given by:

$$Q_{ext} = \frac{R_{p,ext}}{2\pi f L_p} \tag{4.17}$$

In this configuration, the resistance seen in parallel with the resonator is 50 Ω due to the source (R_s) and 50 Ω due to the load (R_l). Therefore, $R_{p,ext}$ will be equal to the parallel combination of R_s and R_l (25 Ω). The resulting loaded Qs of each of the resonator structures are listed in Table 4.2.

Furthermore, for the single-pole resonator, the loaded Q can be used to find the -3 dB bandwidth of the single-resonator filter. However, this is not valid for the pole-zero or the zero-pole-zero resonators since the relationship between Q_{loaded} and the -3 dB bandwidth is derived for a single RLC resonator. Though the pole-zero and zero-pole-zero resonators behave like a parallel RLC resonator near the pole frequency, on either side of these frequencies, the response of the input impedance differs from the response from which the Q_{loaded}/-3 dB bandwidth relationship was derived. The calculated -3 dB bandwidths for each of the single-pole resonators, are listed in Table 4.2.

To confirm the -3 dB bandwidth of the single-pole resonators and find the -3 dB bandwidth of the pole-zero and zero-pole-zero resonators, corresponding single-resonator filters were simulated. The magnitude of S_{21} of each filter plotted versus frequency is shown in Figure 4.8. The simulated -3 dB bandwidths of each filter, as well as the corresponding Q_{loaded} for the single-pole resonator are listed in Table 4.2.

Comparing the simulated results for the -3 dB bandwidth and Q_{loaded} to the calculations for the single-pole resonators, the simulated -3 dB bandwidth are higher than the cal-

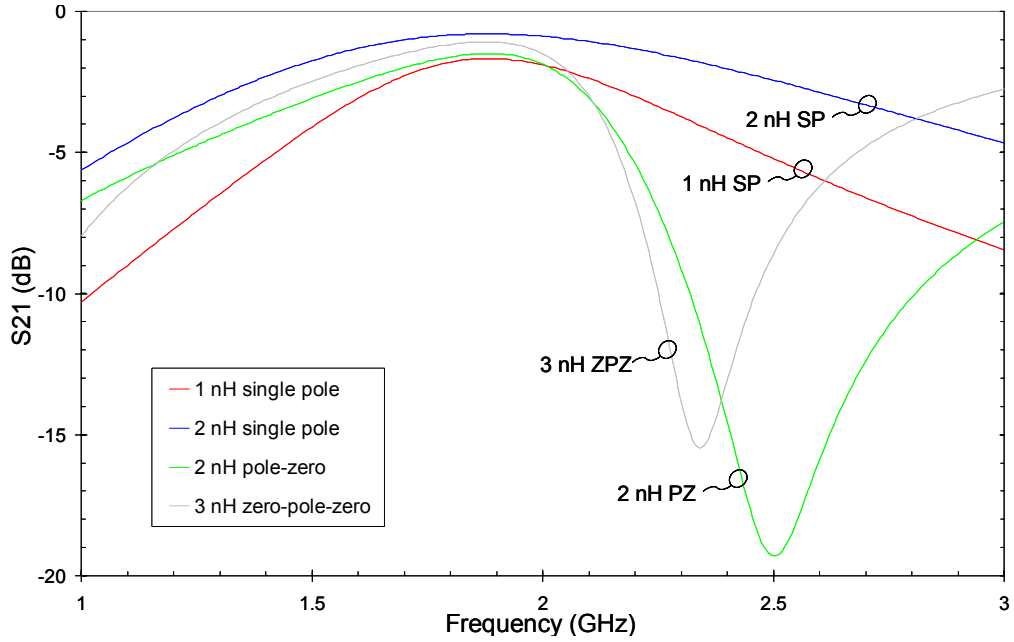


Figure 4.8: Simulated frequency response of passive resonators.

Table 4.2: Single-resonator filter Q and BW (values @ 1.88 GHz).

Resonator Structure	**Inductor Value(s)**	**Calculated**		**Simulated**	
		Q_{loaded}	**BW (GHz)**	**Q_{loaded}**	**BW (GHz)**
Single-Pole	1 nH	1.75	1.07	1.92	0.98
Single-Pole	2 nH	0.98	1.92	1.16	1.61
Pole-Zero	L_r=2 nH, L_c=3 nH	0.96	-	-	0.89
Zero-Pole-Zero	L_l=3 nH, L_c=6 nH	0.65	-	-	0.85

Table 4.3: Summary of single-resonator filter insertion loss (values @ 1.88 GHz).

Resonator Structure	**Inductor Value(s)**	**Simulated Insertion Loss (dB)**
Single-Pole	1 nH	1.67
Single-Pole	2 nH	0.798
Pole-Zero	L_r=2 nH, L_c=3 nH	1.49
Zero-Pole-Zero	L_l=3 nH, L_c=6 nH	1.08

culated values. This discrepancy occurs because the parallel equivalent resistance of the resonator (which is responsible for the unloaded Q of the resonator) is not constant, but increases with frequency (Fig. 4.3). The relationship between Q_{loaded} and the -3 dB bandwidth is derived based on a constant resistance. Therefore, the bandwidths calculated from Q_{loaded} do not take into account the frequency dependence of R_p, only the value of R_p at the pole frequency. On the other hand, the simulation does not rely on the Q_{loaded} to determine the bandwidth. It simply calculates the input impedance of the resonator at each frequency, which would account for the frequency dependence of R_p. Therefore, the simulated bandwidth is more accurate than the bandwidth calculated from Q_{loaded}.

Furthermore, comparing the resulting -3 dB bandwidths of each of the filters offers a number of insights into the effects of the loading. Comparing the filters using the 1 and 2 nH single-pole resonators, the 1 nH resonator actually has a higher loaded Q that the 2 nH resonator, despite having more than twice the loss ($\frac{1}{2}R_p$), because of the reduced inductance. Similarly, comparing the 2 nH single-pole to the 3 nH zero-pole-zero resonator, despite having roughly the same loss, the loaded Q of the 2 nH resonator is larger due to reduced inductance. From these results it is clear that the loading effect dominates the resistance (numerator) of the loaded Q. Therefore, in order to increase the selectivity of the resonator, the value of the inductor should be decreased. Alternatively, if the input/output impedances could be increased (as would be possible in a fully-integrated transceiver), the loading effects would be reduced leading to a higher selectivity.

The effects of the loss of the resonators can also be seen in the insertion loss of each the single-resonator filters. Table 4.3 summarizes the simulated results. The results show that the insertion loss is reduced by using larger inductors (larger R_p).

4.1.4 Q-Enhancement of Resonators

The final step in the implementation of a Q-enhanced resonator is to design the appropriate negative resistance circuit and place it in parallel with the lossy resonator. The parallel equivalent negative resistance combines with R_p of the resonator to reduce or eliminate the effects of the loss (Fig. 4.9). The design of the negative resistance circuit is presented in Chapter 3. The purpose of this discussion is to address issues related to Q-enhancing resonators using these negative resistance circuits. Three design considerations for the proper operation of the resulting Q-enhanced resonator are: (1) the negative resistance circuit must be designed such that the negative resistance at the center frequency of the resonator reduces the loss of resonator by the desired amount while minimizing the potential for instability due to excess negative resistance at other frequencies; (2) a DC bias circuit must be added to properly bias the active components with minimal effect on the RF performance of the circuit; and (3) the resonator design must be compensated for the net parasitic capacitance of the negative resistance circuit. The following sections discuss these design considerations in more detail.

Negative Resistance Design

The most difficult part of designing Q-enhanced resonators is designing the negative resistance circuit for a particular resonator. The synthesized parallel equivalent negative resistance ($R_{p,neg}$) must be at least equal to the parallel equivalent resistance of the resonator ($R_{p,res}$) at the center frequency of the resonator. Furthermore, $R_{p,res}$ needs to be generated using a minimal amount of current. Section 3.4 discusses how to design the negative resistance circuit for a given $R_{p,neg}$. However, the effect of the negative resistance beyond the center frequency of the resonator, where $R_{p,neg}$ is not necessarily equal to $R_{p,res}$, must also be considered.

Beyond the center frequency of the resonator, there is no need to exactly match $R_{p,neg}$ to $R_{p,res}$. However, should $R_{p,neg}$ and $R_{p,res}$ diverge by a substantial amount, there are ramifications for the rejection and the stability of the resonator. For the negative resistance circuit chosen in this thesis, it is not possible to match $R_{p,neg}$ and $R_{p,res}$ at all frequencies. This is because the resonator loss is in series with the inductor, resulting in a low pass response (or band pass response in the case of the pole-zero and zero-pole-zero resonators). The negative resistance is in series with a capacitor, resulting high

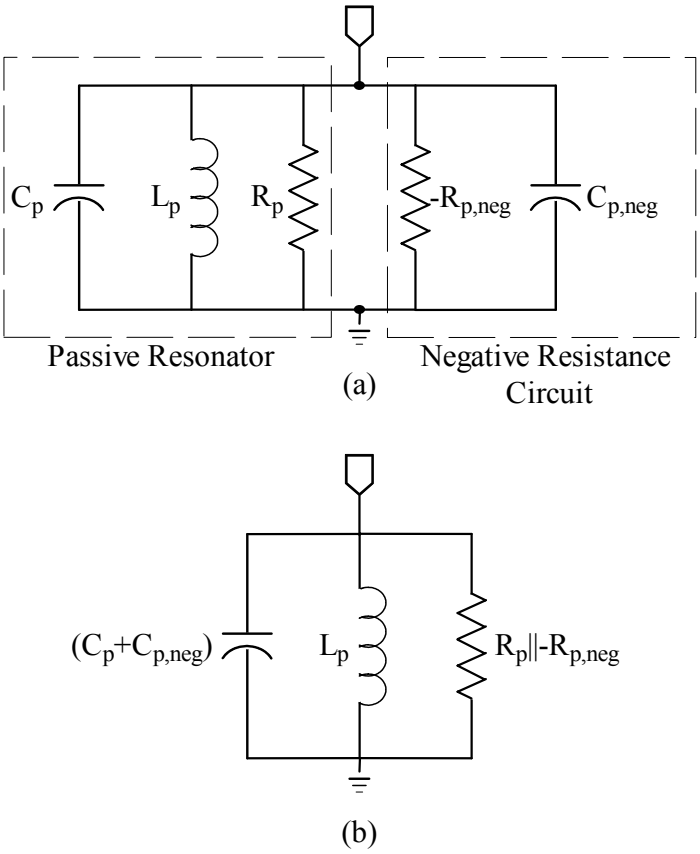


Figure 4.9: Equivalent circuits of Q-enhanced resonators near parallel resonance.

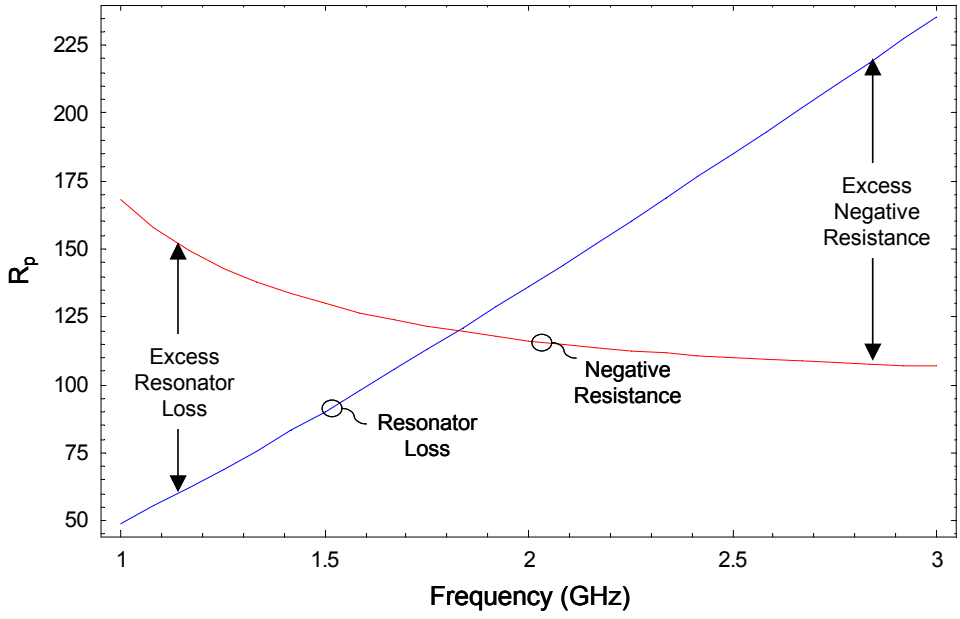
pass response (Fig. 4.10). When matched at the center frequency of the resonator, at frequencies below the resonance point, $R_{p,res}$ will be less than $R_{p,neg}$ [Fig. 4.10(a) and (b)], meaning the loss of the resonator will be greater than what the negative resistance circuit can compensate for. This excess resonator loss is actually beneficial in that it provides additional out-of-band rejection. At frequencies above the resonance point, each of the resonator structures behaves differently. For the single-pole resonator (for which the loss has a low pass response), above the resonance frequency $R_{p,res}$ will be greater than $R_{p,neg}$ [Fig. 4.10(a)] resulting in excess negative resistance. Excess negative resistance is detrimental to the design, not only because it degrades the rejection of resonator, but because it also presents the possibility for instability. Should $R_{p,neg}$ become less than or equal to the parallel combination of $R_{p,res}$ and the loading resistance, the circuit can become unstable. On the other hand, the loss response of the pole-zero and zero-pole-zero resonators are bandpass in nature. Therefore, for these resonators, above the resonance frequency $R_{p,res}$ will be less than $R_{p,neg}$ [Fig. 4.10(b)], resulting in excessive resonator loss on the high side of f_0, improving the rejection. Therefore, the Q-enhanced pole-zero and zero-pole-zero resonators are inherently more stable than the Q-enhanced single-pole resonator.

Bias Circuit Design

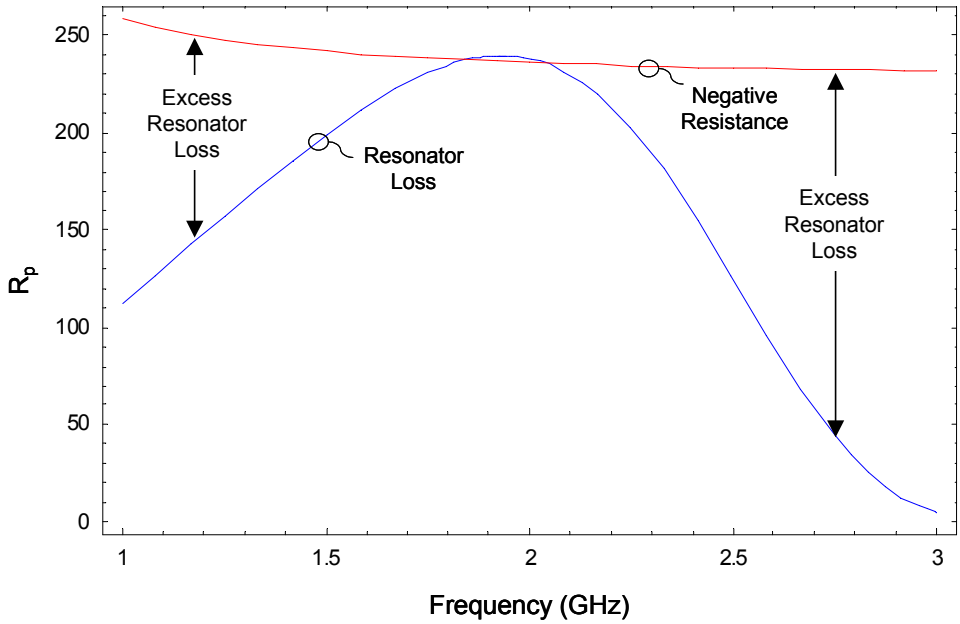
The goal of designing the bias circuit is to supply the required voltages to the active device with minimal impact on the RF performance of the circuit. Where possible, positive voltages are preferred to negative voltages in order to minimize the number of power sources required by the system that the filter will be used in.

To bias either enhancement- (E-) or depletion- (D-) mode FETs, a positive voltage must be generated between the drain and the source (V_{ds}) and a voltage, either a positive or negative, is required between the gate and the source (V_{gs}) of the FET. D-FETs require a negative V_{gs} to turn on the device. Conversely, E-FETs require a positive V_{gs}.

When a D-FET is used, a negative V_{gs} can be obtained by DC grounding the gate of the FET and applying a positive voltage to the source, or DC grounding the source and applying a negative voltage to the gate of the FET. For the single-pole and pole-zero resonators, the gate of the FET is DC grounded through the shunt inductor of the resonator (L_r). Furthermore, in the negative resistance circuit, the source of the FET is



(a)



(b)

Figure 4.10: Calculated frequency response of resonator loss and negative resistance: (a) single pole resonator; (b) pole-zero or zero-pole-zero resonator.

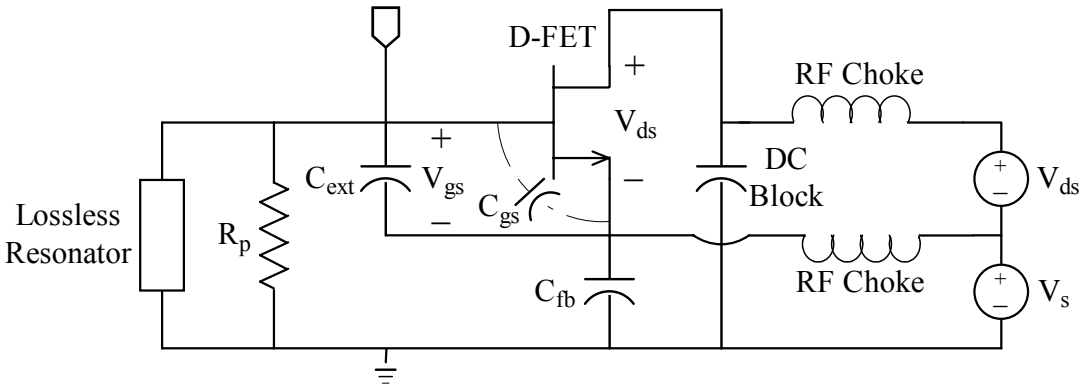


Figure 4.11: Q-Enhanced resonator with D-FET bias circuit

already isolated from ground at DC by C_{fb} and C_{ext}. Therefore, for the single-pole and pole-zero resonators, a D-FET can be biased at the source of the FET with a positive voltage (Fig. 4.11). However, in the zero-pole-zero resonator, the gate of the FET is isolated from ground at DC, requiring either a negative voltage at the gate, or a positive voltage at the source and the gate of the FET (through the port of the resonator) to be DC grounded (without bypassing the resonator at RF).

Similarly, using an E-FET, a positive V_{gs} can be obtained by DC grounding the gate of the FET and applying a negative voltage to the source, or DC grounding the source and applying a positive voltage to the gate of the FET. Again, for the single-pole and pole-zero resonators, the gate of the FET is at DC ground through L_r in the resonator circuit, requiring a negative voltage at the source of the device. For the zero-pole-zero resonator, however, the gate of the FET is isolated from ground at DC by the capacitors in each arm of the resonator. Therefore, a positive voltage can be applied to the gate of the FET, through the RF port of the resonator, and the source can be DC grounded through an RF choke (Fig. 4.12).

Therefore, for the single-pole and pole-zero resonators, using a depletion-mode FET requires the minimum complexity and requires only positive voltage sources. The circuit in Figure 4.11 is used to supply the voltage to the drain and the source of the device. At the drain, a large capacitor is required to provide a good RF ground and block the DC being injected through an RF choke. At the source, an RF choke is required to apply the DC voltage without providing an RF bypass path around C_{fb}.

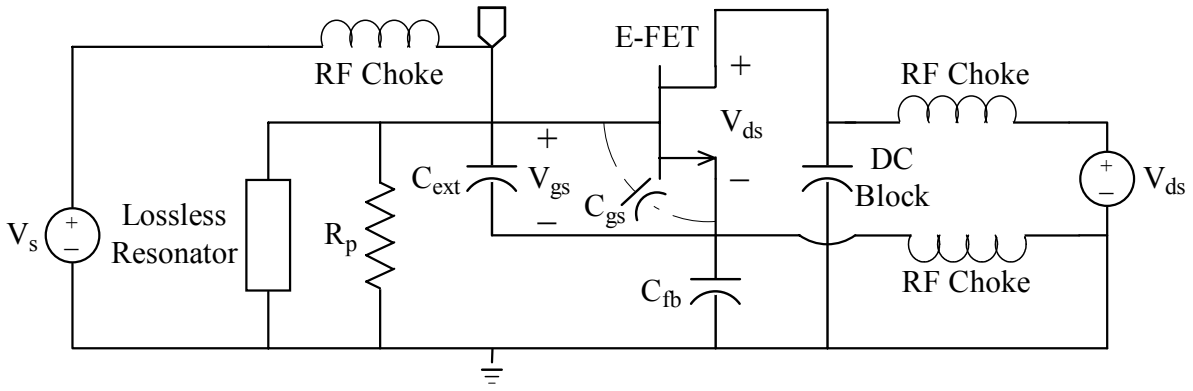


Figure 4.12: Q-Enhanced resonator with E-FET bias circuit

For the zero-pole-zero resonator, the enhancement mode FET is used since the gate of the FET is DC blocked by the resonator. The circuit shown in Figure 4.12 can be used to apply a positive gate voltage in through the port of the resonator and DC ground the source through an RF choke.

Capacitance Equalization

As was discussed previously, the negative resistance circuit produces a negative resistance is series with a capacitance. Furthermore, in Section 3.4, the series combination of the negative resistance and capacitance was transformed into the parallel equivalent negative resistance ($R_{p,neg}$) and capacitance ($C_{p,neg}$) [Fig. 4.9(a)]. $C_{p,neg}$ is a function of C_{fb}, C_{ext}, and the size and bias point of the FET, which is also discussed in detail in Section 3.4. When the negative resistance is placed in parallel with the passive resonator, $C_{p,neg}$ combines in parallel with the capacitance (or equivalent capacitance in the case of the pole-zero or zero-pole-zero resonators) of the resonator (C_r). The resulting capacitance (C_r+$C_{p,neg}$) shifts the center frequency of the resonator to a lower frequency [Fig. 4.13(a)]. Therefore, to maintain the desired center frequency, C_r must be reduced by $C_{p,neg}$ to resonate with L_p at the desired frequency [Fig. 4.13(b)].

For the pole-zero and zero-pole-zero resonators, there are consequences to changing the equivalent capacitance of the resonators. To lower the equivalent capacitance of these resonators, the capacitance (C_c) must be reduced or the inductance (L_c) must be increased (or some combination of the two). Increasing the value of L_c results in a higher series

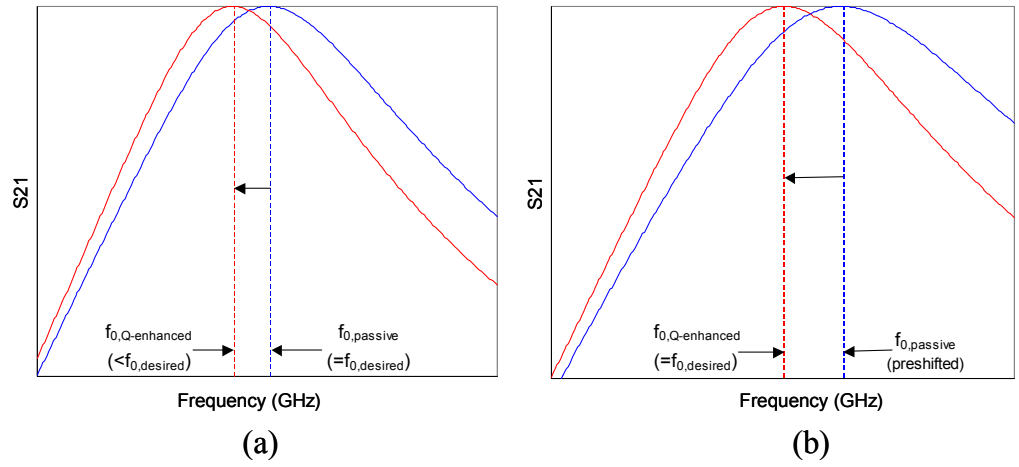


Figure 4.13: Illustration of frequency shift due to negative resistance circuit: (a) Without preshifted passive resonator (b) With preshifted passive resonator

resistance, changing the resonator loss found in section 4.1.2. However, in decreasing C_c, the transformation of the series resistance ($R_{s,Lc}$) to the parallel equivalent ($R_{p,Lc}$) changes, affecting the net loss of the resonator. Hence, either choice requires the recalculation of the loss of the resonator. In this way, the design of these Q-enhanced resonators is an iterative process. However, as was discussed in Section 4.1.2, the resonators were pre-shifted and their loss calculated. In order to minimize die area, the value of C_c was reduced rather than increasing the size of the inductor (L_c).

Furthermore, increasing the inductance (L_c) or decreasing the capacitance (C_c) in the pole-zero or zero-pole-zero resonators will also shift the zero frequency, due to the series resonance of L_c and C_c, to a higher frequency [see Fig. 4.16(d) as an example]. The more capacitance due the negative resistance circuit that needs to be compensated for, the more the zero frequency will increase. Therefore, to maintain a sharp rolloff by keeping the zero close to the pole frequency of the resonator, the parallel equivalent capacitance of the negative resistance circuit must be minimized.

4.1.5 Q-Enhanced Resonator Simulations

Nine resonator designs were simulated both as 1-port resonators and as a 2-port single-resonator filters (Fig. 4.1). For the purposes of illustrating the effects of the resonator loss and subsequent Q-enhancement, simulations presented here will be of the resonators

as shunt devices in 2-port single-resonator filters.

Single-Pole Resonators

Figure 4.14 shows the simulated results of the three single-pole resonators that were designed as part of this study (Fig. 4.15). All three filters used the 1 nH baseline inductor for L_r. The first design [Fig. 4.15(a)] consists of the baseline passive resonator. The simulated baseline single-resonator filter has an insertion loss of 1.67 dB and a -3 dB bandwidth of 950 MHz at a center frequency of 1.88 GHz (Fig. 4.14). The two Q-enhanced single-pole resonators [Fig. 4.15(b) and 4.15(c)] use nearly identical negative resistance circuits, the only difference being that one uses a D-FET and the other uses an E-FET. In simulation, the response of the two circuits was nearly identical. Each of the Q-enhanced single-pole single-resonator filters achieve 0 dB insertion loss and a -3 dB bandwidth of 790 MHz at a center frequency of 1.9 GHz[2] (Fig. 4.14). In order to achieve 0 dB insertion loss, the D-FET circuit drew 13.8 mA of current while the E-FET circuit drew 10.23 mA. Therefore, Q-enhancing the resonator not only removes the loss, but also marginally increases the selectivity of the single-resonator filter. However, this improvement is at the expense of added power consumption.

Pole-Zero Resonators

Figure 4.16(d) shows the simulated, small-signal response of each of the pole-zero single-resonator filters in Figure 4.16(a)-(c). The baseline passive single-resonator filter [Fig. 4.16(a)] has an insertion loss of 1.49 dB and a -3 dB bandwidth of 890 MHz at a center frequency of 1.88 GHz. The response of the second passive single-resonator filter [Fig. 4.16(b)] illustrates the effects of reducing the capacitance to account for the capacitance of the negative resistance circuit. The zero frequency, due to the series resonance of L_c and C_c, is shifted higher in frequency. Finally, the response of the Q-enhanced pole-zero single-resonator filter [Fig. 4.16(c)] attains a 0 dB insertion loss and a 1,100 MHz, -3 dB bandwidth at 1.88 GHz. Under these conditions, the negative resistance circuit draws 3 mA of current. This is much lower current consumption than the Q-enhanced 1 nH

[2]Each circuit was originally designed to have an insertion loss of 0.5 dB. By increasing the bias, the insertion loss was later reduced to 0 dB. However, by increasing the bias, the parallel equivalent capacitance of the negative resistance circuit decreased, leading to a slight increase in the center frequency of the resonator.

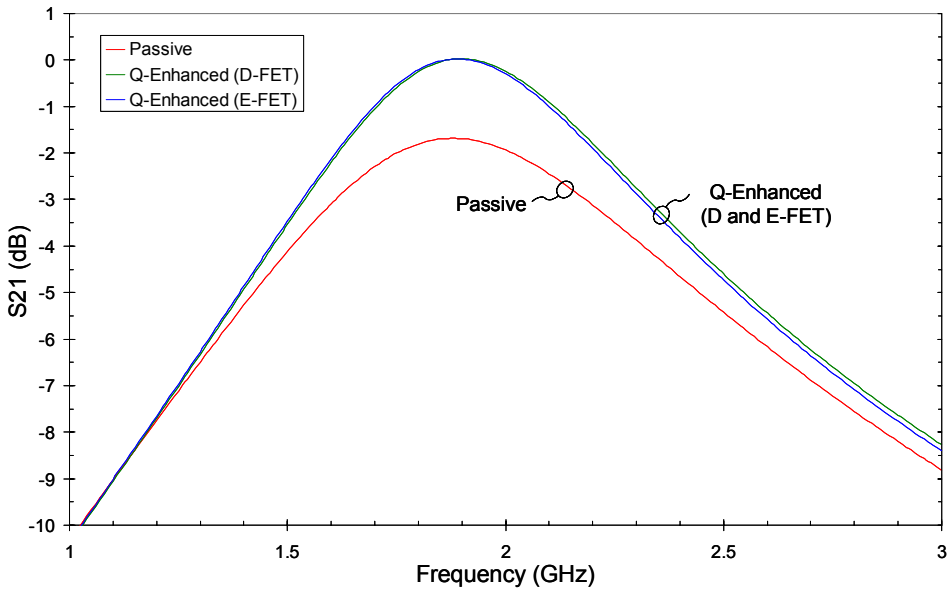


Figure 4.14: Simulated single-pole resonator response.

single-pole resonators because the loss of the 2 nH pole-zero resonator was less than that of the 1 nH single-pole resonator. The difference in loss was due, primarily, to the size of the inductor used. Therefore, it is not that the Q-enhanced pole-zero resonator is more current efficient, but that the 2 nH inductor has less loss to Q-enhance. Furthermore, although Q-enhancing the resonator reduces the insertion loss to 0 dB, it also decreases the selectivity of the filter due to a higher zero frequency.

Zero-Pole-Zero Resonators

Finally, Figure 4.17(d) shows the simulated, small-signal response of each of the zero-pole-zero single-resonator filters shown in Figure 4.17 (a)-(c). The baseline passive zero-pole-zero single-resonator filter [Fig. 4.17(a)] has an insertion loss of 1.08 dB and a -3 dB bandwidth of 850 MHz at 1.88 GHz. Similar to the pole-zero structure, the response of the second passive single-resonator filter [Fig. 4.17(b)] illustrates the effects of reducing the resonator capacitance to account for the capacitance of the negative resistance circuit, shifting the zero higher in frequency. In Q-enhancing this structure [Fig. 4.17(c)], roughly 2 mA is required to achieve 0 dB insertion loss and a -3 dB bandwidth of 1270 MHz at 1.88 GHz. Again, the low current required to Q-enhance this resonator is due to the low

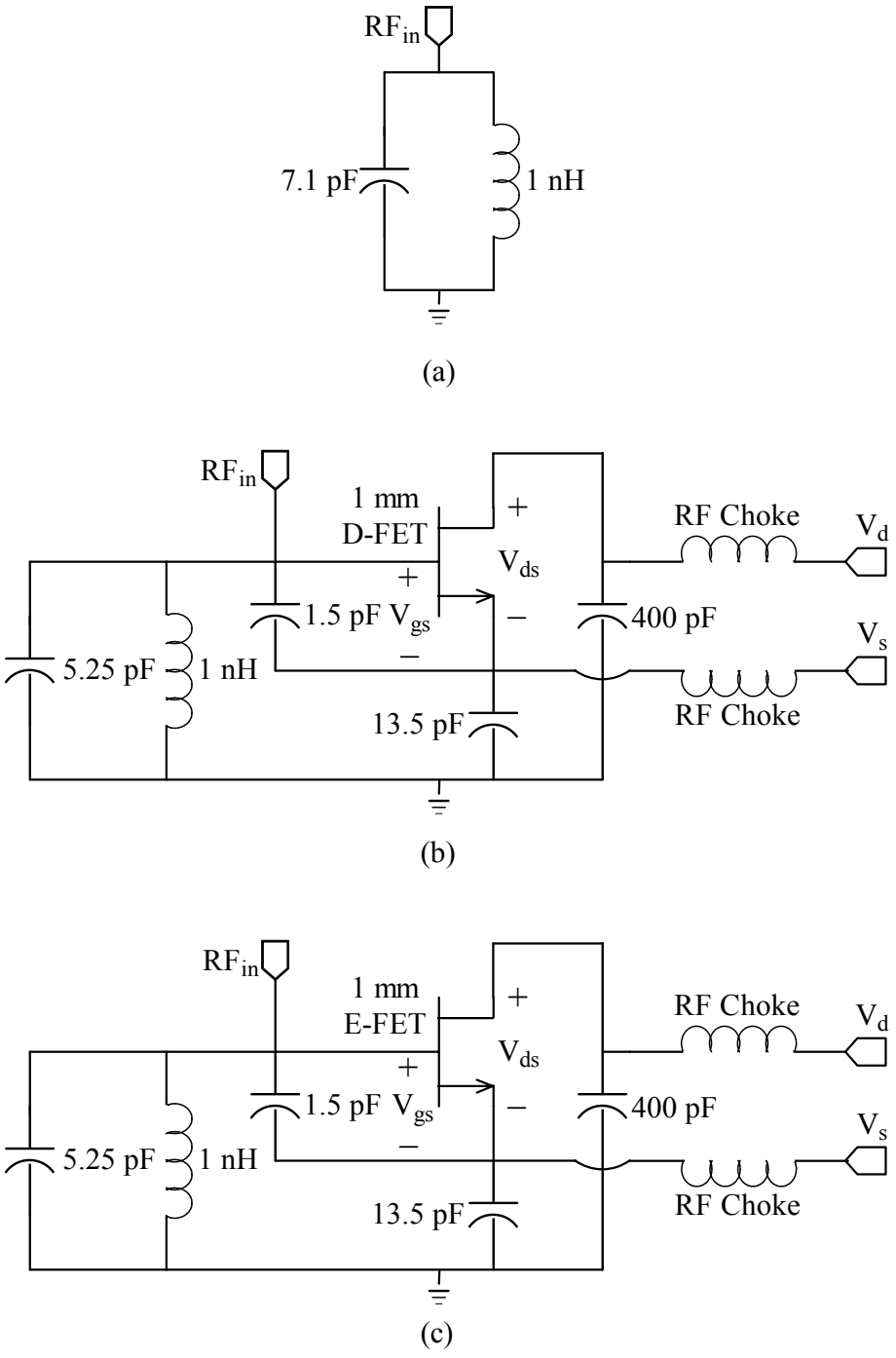
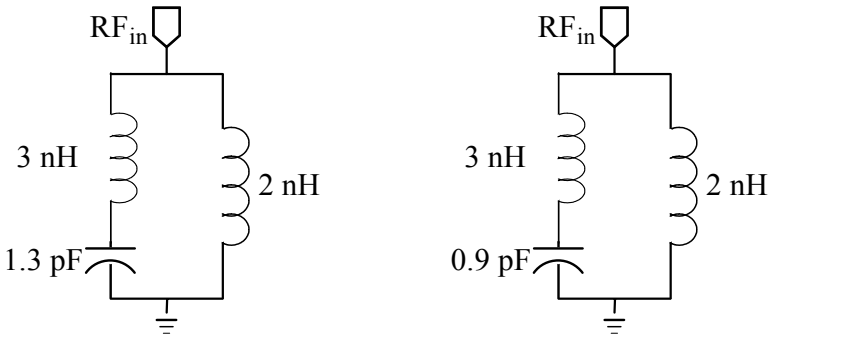
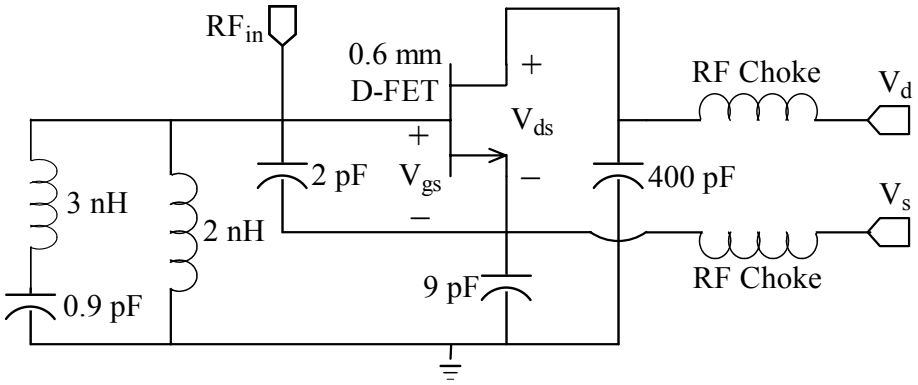


Figure 4.15: Single-pole resonator designs: (a) baseline passive; (b) Q-enhanced with 1 mm D-FET; (c) Q-enhanced with 1 mm E-FET.

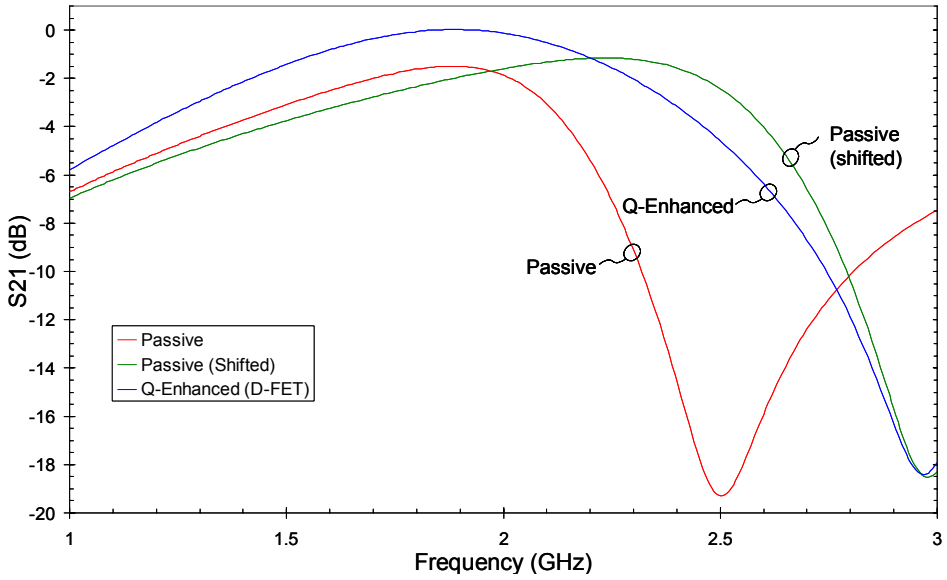


(a)

(b)



(c)



(d)

Figure 4.16: Pole-zero resonator designs: (a) passive baseline; (b) shifted passive; (c) Q-enhanced; (d) single stage filter simulation.

Table 4.4: Summary of simulated resonators used for single stage filter tuned for 0 dB insertion loss.

Structure	**FET**	$\mathbf{I_{ds}}$ **(mA)**	$\frac{\mathbf{f_0}}{\textbf{-3 dB BW}}$
Single-Pole (1 nH)	D-FET	13.83	2.4
Single-Pole (1 nH)	E-FET	10.23	2.4
Pole-Zero (2 nH)	D-FET	3	1.71
Zero-Pole_Zero (3 nH)	E-FET	2	1.48

resonator loss associated with the 3 nH inductor. Furthermore, while Q-enhancing the resonator eliminates insertion loss of the filter, it also decreases the selectivity due to the higher upper zero frequency.

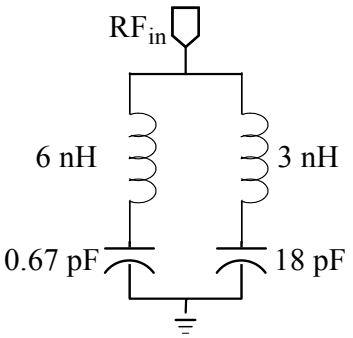
Table 4.4 summarizes the results of the resonator simulations.

4.2 Fabrication and Measurements

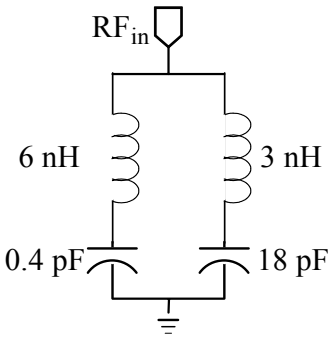
9 resonator designs were fabricated to evaluate the performance of the Q-enhanced resonators presented above. The general layouts used for each of the designs are discussed in Section 4.2.1. The designs were intended for testing using on-wafer probing techniques. However, due to limitations in available die area, the DC blocking capacitor (C_d) for each design was implemented using an external chip capacitor ($\backsim$400 pF). Therefore, some post-fabrication assembly was required to allow measurements of the structures. Section 4.2.2 discusses the setup used to measure the 1-port S-parameter (S_{11}) of the fabricated resonators. Finally, the measured small-signal S-parameters for each structure are discussed in Section 4.2.3.

4.2.1 Layout and Assembly

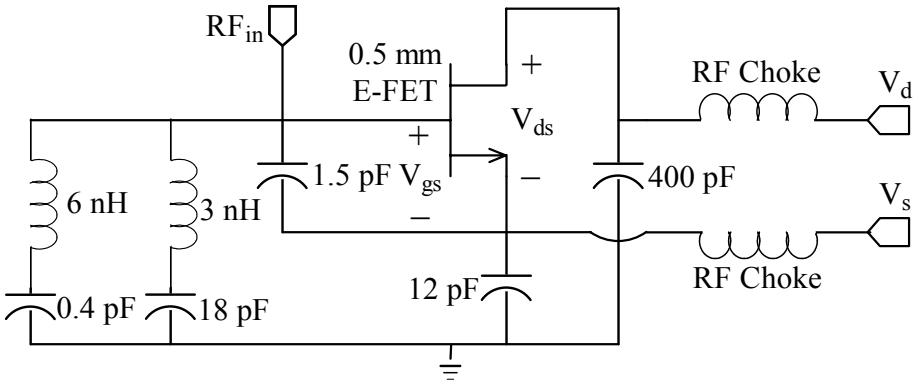
The final layouts of all nine one-port resonator test structures, as well as a one-port test structure for the 1 nH baseline inductor are included in Appendix A of this thesis (Fig. A.1-A.4). The ten structures were combined to fit on four chips fabricated. The preliminary layouts were designed using the layout editor in Series IV [5]. Final layouts were then completed by M/A-COM.



(a)



(b)



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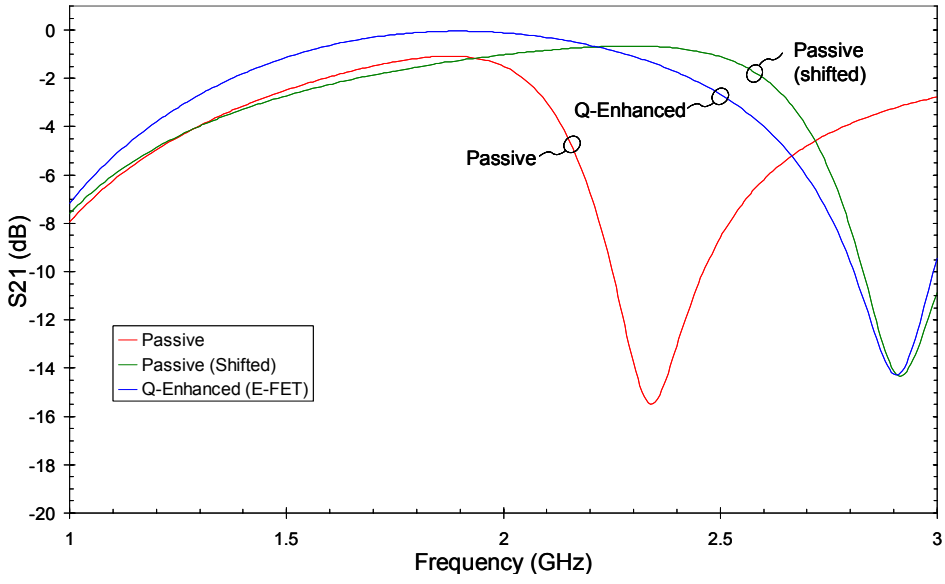


(d)

Figure 4.17: Zero-pole-zero resonator designs: (a) baseline passive; (b) shifted passive; (c) Q-enhanced; (d) single stage filter simulation.

The following structures were fabricated during the first phase of the study:

- 1 nH baseline spiral inductor [layout: A.2]
- Passive 1 nH single-pole resonator [schematic: Fig. 4.15(a), layout: A.1]
- Q-enhanced 1 nH single-pole resonator with 1 mm D-FET [schematic: Fig. 4.15(b), layout: A.1]
- Q-enhanced 1 nH single-pole resonator with 1mm E-FET [schematic: Fig. 4.15(c), layout: A.1]
- Passive 2 nH shifted pole-zero resonator[3] [schematic: Fig. 4.16(b), layout: A.3]
- Q-enhanced 2 nH pole-zero resonator [schematic: Fig. 4.16(c), layout: A.3]
- Passive 3 nH shifted zero-pole-zero resonator[3] [schematic: Fig. 4.17(b), layout: A.4]
- Q-enhanced 3 nH zero-pole-zero resonator [schematic: Fig. 4.17(c), layout: A.4]

Figure 4.18 shows the layout of the Q-enhanced 1 nH single-pole resonator with 1 mm D-FET as an example of the general layout structure used for the single-pole resonators. The resonator (L_r || C_r) is fed directly at the RF_{in} port and the inductor is grounded through the bottom plate of the capacitor. The negative resistance circuit is connected through the top plate of C_r. The source bias is applied at the port labeled V_s, which is connected to the source of the FET through the top plate of C_{fb}. The drain voltage is applied at the port labeled V_d, which connects directly with the drain bar of the FET. Since the gate of the FET is DC grounded through L_r, V_{gs} and V_{ds} are set by V_d and V_s. The entire structure is surrounded by a ground ring, enabling Ground-Signal-Ground (GSG) probes (150 μm pitch) to make proper contact. The chips were epoxied to a conductive substrate for mechanical stability.

To minimize the die area consumed by the individual circuits, neither the RF chokes nor the DC block (at the drain of the FET) were included in the layout. To allow an

[3]The *shifted* passive pole-zero and zero-pole-zero resonator designs were fabricated rather than the properly centered passive structure in order to more conclusively troubleshoot the respective Q-enhanced resonators as necessary.

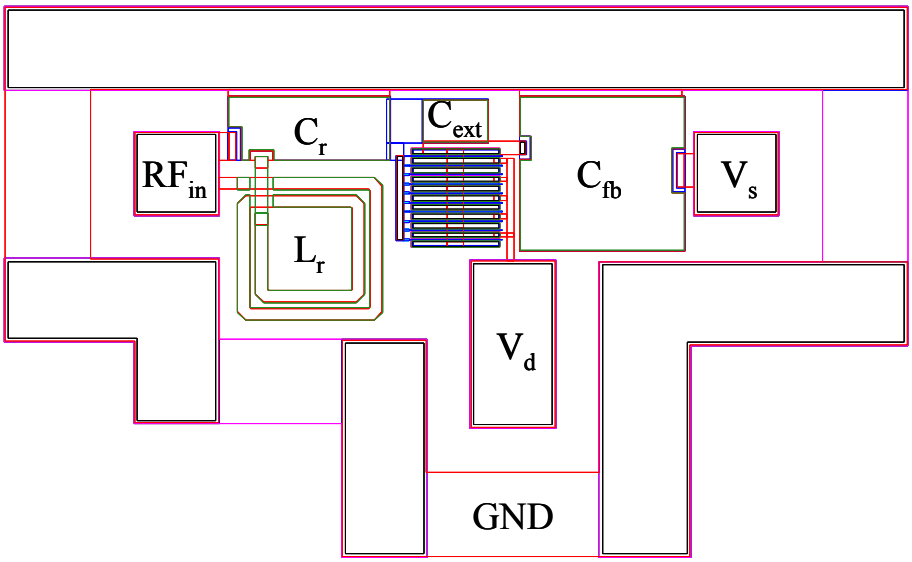
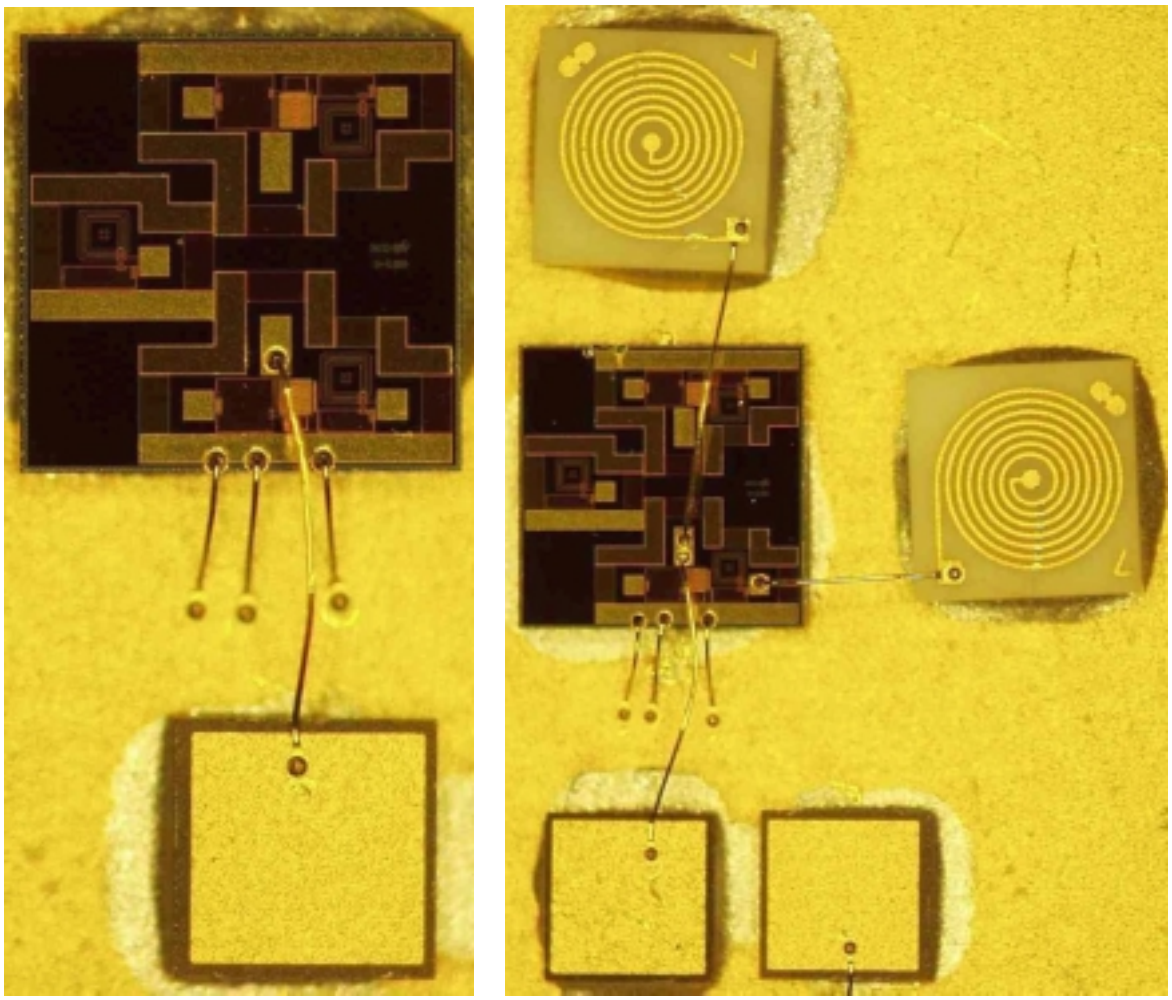


Figure 4.18: Layout of one-port, Q-enhanced 1 nH, single-pole resonator.

external chip capacitor to be bonded into this circuit as the DC block, the bond pad labeled V_d was lengthened to accommodate the bondwire as well as the DC bias probe [Fig. 4.19(a)]. In addition, multiple bondwire were used between the ground ring and the conductive substrate to ensure continuity of the system ground (conductive epoxy was used to ground of the external capacitor to the conductive substrate). Initially, the necessary RF chokes were implemented using external bias tees. However, due to measurement difficulties using the bias tees, in some cases external inductors were also be bonded into the circuit [see Fig. 4.19(b)]. Using these inductors as RF chokes, the bias voltage was applied to the center of the inductor using a DC probe.

Figure 4.20 shows the layout of the Q-enhanced 3 nH zero-pole-zero resonator as an example of the general layout structure used for all the pole-zero and zero-pole-zero resonators. Each arm of the resonator is fed directly by the RF_{in} port. For both resonator structures, C_c is small enough to be placed in the center cavity of L_c in order to minimize die area. The negative resistance circuit is connected directly to the RF_{in} port. The drain bias is applied to the port labeled V_d which connects directly to the drain bar of the FET. The source bias is injected through the port labeled V_s and is connected to the source of the FET through the top plate of C_{fb} and the bottom plate of C_{ext}. The entire structure is surrounded by a ground ring designed to accommodate a 150 μm pitch GSG probe for the RF_{in} port and a 150 μm pitch Ground-Signal-Signal-Ground (GSSG)



(a) (b)

Figure 4.19: Assembled Q-enhanced resonator: (a) With external DC blocking capacitors; (b) With external DC blocking capacitors and chip inductors for RF chokes on the bias lines.

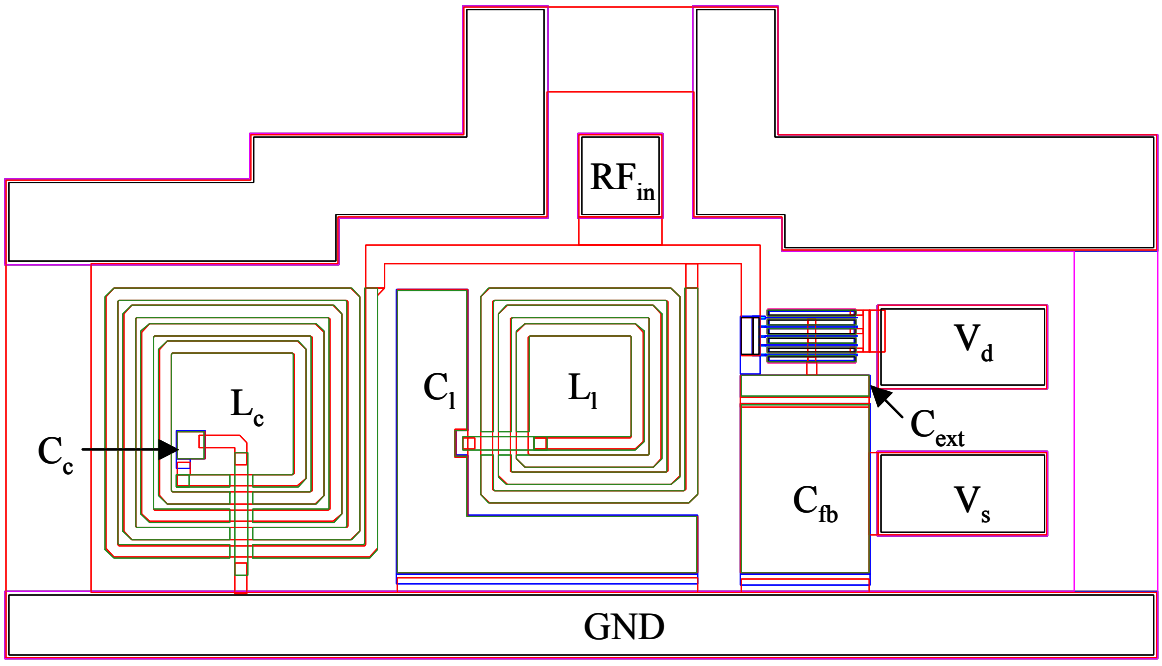


Figure 4.20: Layout of one-port, Q-enhanced 3 nH, zero-pole-zero resonator.

probe for V_d and V_s ports.

As with the single-pole resonator layouts, neither the RF chokes nor the DC block were included in the layout. The pads for V_d and V_s were lengthened to allow for an external capacitor and external RF choke inductors to be bonded into the circuit as necessary.

4.2.2 Measurements

The equipment and setup used to measure S_{11} of the resonator test structures is shown in Figure 4.21. A Short-Open-Load (SOL) 1-port calibration was performed to calibrate to the probe tips using a Cascade calibration substrate.

Since the RF chokes required in the bias circuit were not integrated on chip, bias tees were used to supply the DC voltage without grounding the RF. However, ripples were noted in the measurements, most likely due to standing waves on the cable between the probe and the bias tee. A terminated circulator was therefore placed at the RF port of the bias tee to surpress the reflections. The circulator corresponding to the drain voltage was terminated with a short since C_d should ideally short the RF in the circuit.

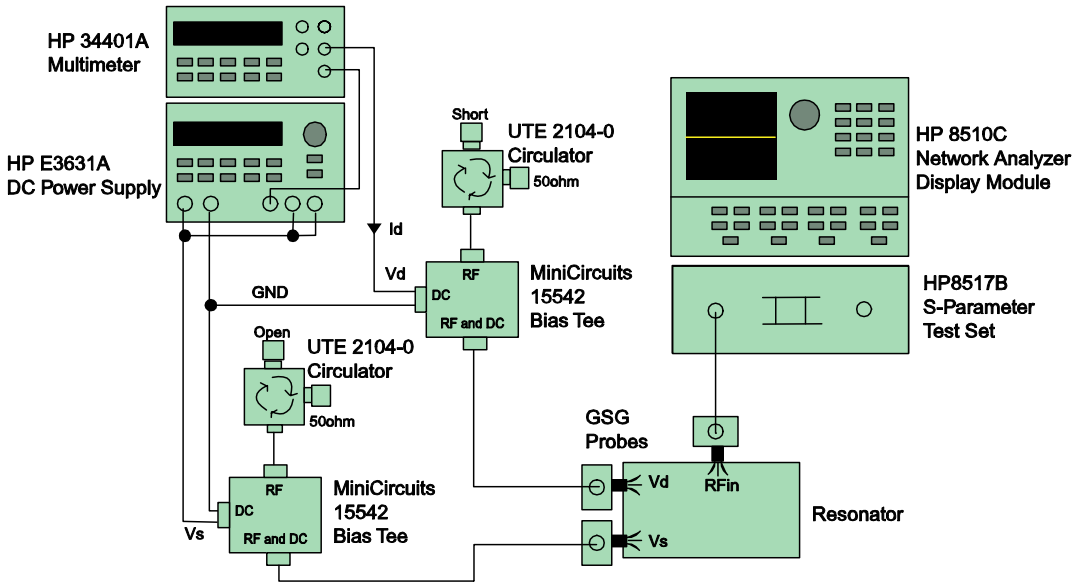


Figure 4.21: S_{11} measurement setup.

The circulator corresponding to the source voltage was terminated with an open in order to avoid creating a path bypassing C_{fb}. The addition of the circulator eliminated the ripple for the most part. Furthermore, the response using this setup closely matched the response using chip inductors as RF choke and DC probes to apply the bias. The chip inductors used were in limited supply, so this approach was used only to validate the measurements made using the setup in Figure 4.21.

An automated extraction program using HP VEE [19] was employed to record the S-parameters and DC power consumption of each of the resonators at various bias points. The data was recorded using the MDIF file format (shown in Appendix B) enabling the results to be imported into Series IV [5] and tuned on the basis of bias point.

4.2.3 S-Parameters

The S_{11} measurements were imported into Series IV [5] using the MDIF file format and configured as a shunt device in a single-resonator filter (Fig. 4.1). The results presented in this section represent S_{11} data transformed into a two-port filter measurement.

Unfortunately, the E-FET based circuits were unable to be measured due to unresolved

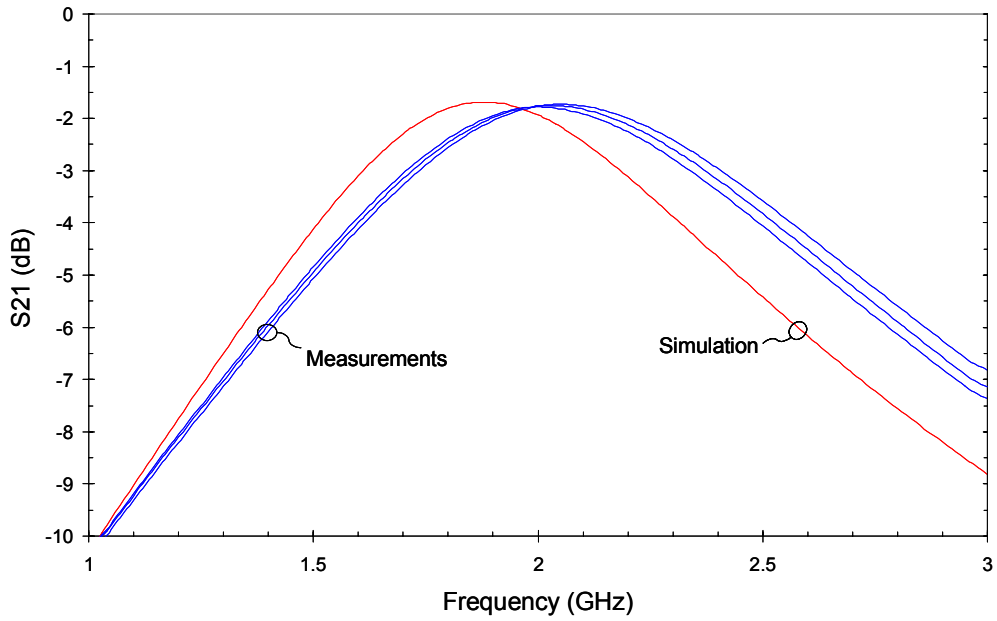


Figure 4.22: Passive single-pole resonator S_{21}: Simulated versus measured results.

problems in biasing the FETs. Furthermore, due to the standing wave problems in the bias networks, some ripple can still be noted on the results presented.

Single-Pole Resonators

The small-signal response of the single-resonator filter based on the passive single-pole resonator in Figure 4.15(a) is shown in Figure 4.22. The mean measured insertion loss of the filter was 1.76 dB (slightly higher than the 1.67 dB predicted by simulation) and the -3 dB bandwidth of the filter was 1,120 MHz at a center frequency of 2.02 GHz (compared to 950 MHz simulated at 1.88 GHz center frequency). The higher center frequencies of the resonators accounts for the decreased selectivity of the filter due to a decreased Q. Given the that the 1 nH baseline spiral inductors measured in Section 2.3 precisely matched the simulations, this shift in center frequency is most likely due to the actual capacitance of the resonator MIM capacitor being smaller than expected.

The single-resonator filters using the Q-enhanced single-pole resonator with the D-FET negative resistance circuit [Fig. 4.15(b)] also had their center frequencies shifted by a similar amount as the passive structure (Fig. 4.23). Again, the actual capacitance

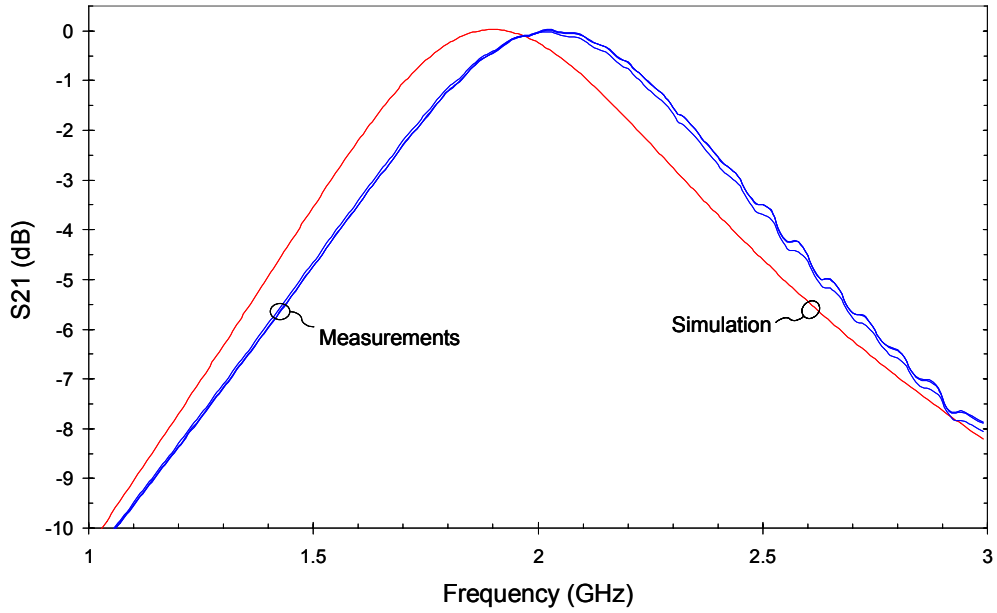


Figure 4.23: D-FET Q-enhanced single-pole resonator S_{21}: Simulated versus measured results.

realized for the resonator is the most likely cause. Regardless, the response of these filters achieved 0 dB insertion loss with a mean bias current of 11.75 mA. The -3 dB bandwidth of the mean response was 810 MHz at a center frequency of 2.02 GHz, compared to the 790 MHz at a 1.88 GHz center frequency predicted by simulation. Again, the decreased selectivity of the filter compared to the simulation is due to the decrease in R_p of the resonator at higher frequencies. However, when compared to the measurements of the passive structure at the same center frequency, Q-enhancing the resonator increased the selectivity by nearly 30%.

Pole-Zero Resonators

The small-signal response of the filter using the *shifted* passive pole-zero resonator is shown in Figure 4.24. The measured responses deviate from simulation in both the location of the pole frequency (center frequency) as well as the zero frequency. The pole of the resonator being lower than simulated is due in part to L_r. Recalling the discussion in Section 2.3, the 2 nH baseline spiral used in this resonator was designed and simulated to be 2 nH, but measured 2.5 nH of inductance. Furthermore, the lower zero frequency suggests that either C_c is larger than simulated (unlikely given that the

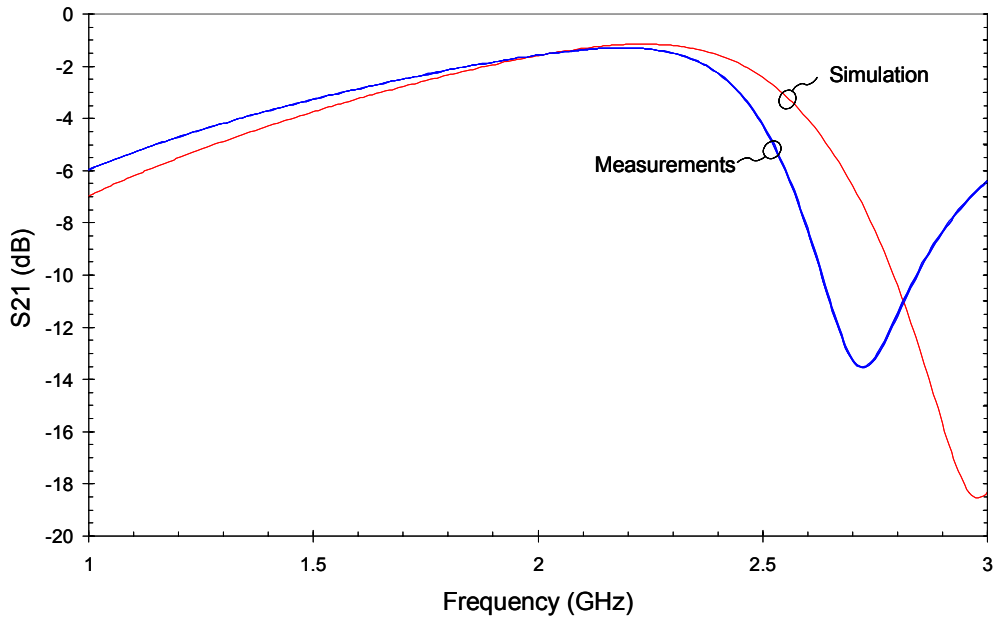


Figure 4.24: Shifted passive pole-zero resonator S_{21}: Simulated versus measured results.

capacitors in the single-pole resonators were found to be smaller than simulated), or that L_c is larger than simulated. The latter is more likely; however, no test structure for the 3 nH baseline spiral inductor was fabricated to validate this assertion. Furthermore, L_c being larger than simulated would also account, in part, to the pole frequency being lower than simulated.

Measurements of the Q-enhanced version of the pole-zero resonator (Fig. 4.25) also show a shifted zero frequency in comparison to simulation. However, the pole frequency of the measured filters matches simulation. Given the conclusions listed for the passive circuit, this would suggest that the capacitance due to the negative resistance circuit, was less than simulations predicted, leading to offsetting differences. The corresponding filters achieve 0 dB insertion loss with a mean bias current of 3 mA, as predicted by simulations. The -3 dB bandwidth of the mean response is 1,160 MHz at center frequency of 1.88 GHz compared to the 1,100 MHz -3 dB bandwidth predicted in simulation.

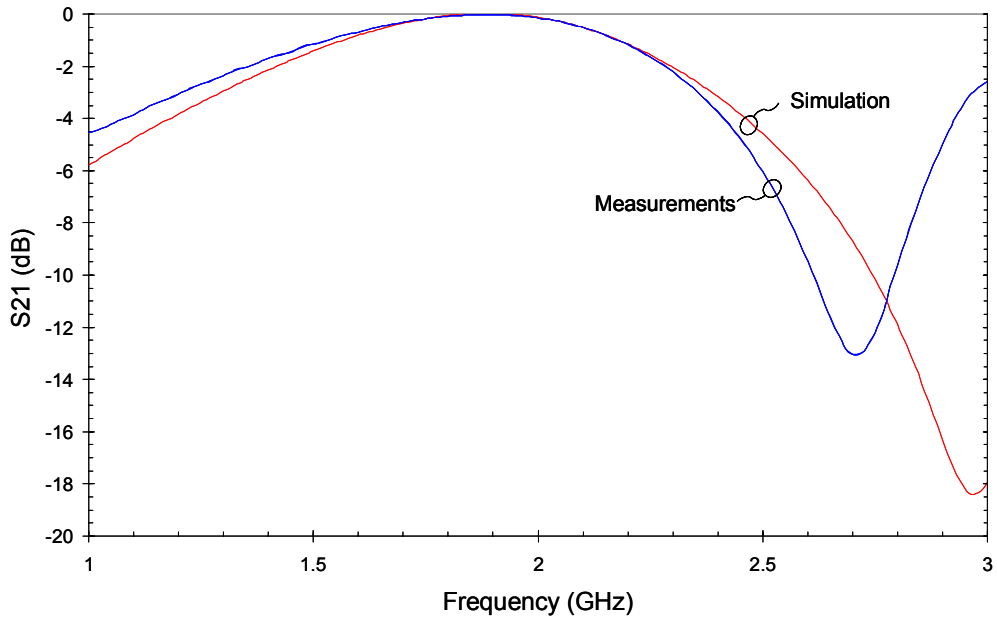


Figure 4.25: D-FET Q-enhanced pole-zero resonator S_{21}: Simulated versus measured results.

Zero-Pole-Zero Resonators

The response of the filter using the shifted passive zero-pole-zero resonator is shown in Figure 4.26. As with the filter based on the shifted passive pole-zero resonator, both the pole and the upper zero frequency are lower than predicted by simulations. Again, this is most likely due to L_c being larger than simulated, leading the capacitive arm of the resonator to have a higher capacitance than simulated and, hence reducing both the pole and upper zero frequencies.

Again, the Q-enhanced version of this resonator was not able to be measured due to problems in biasing the E-FET.

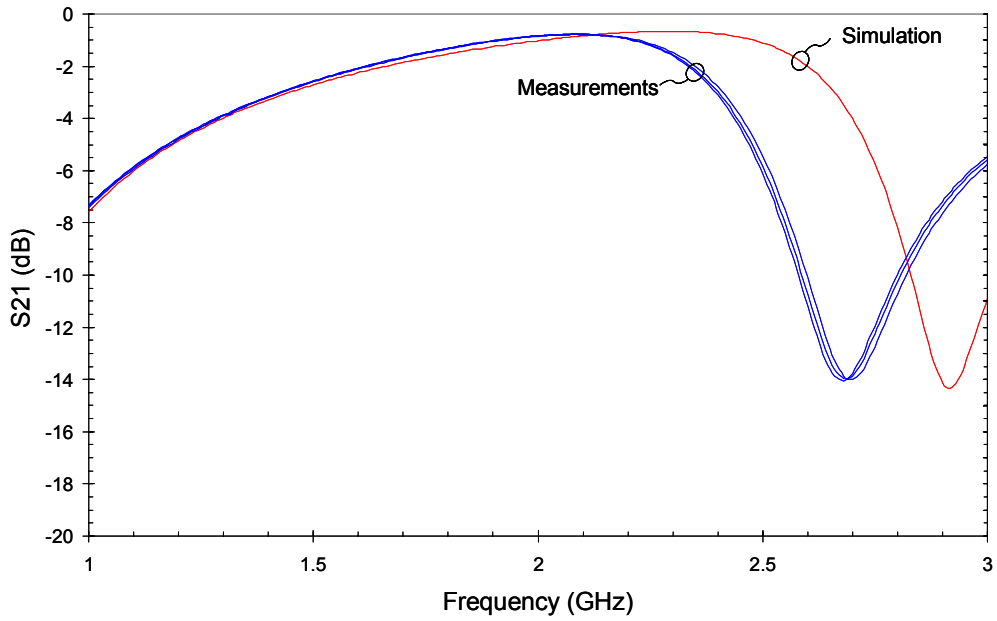


Figure 4.26: Shifted passive zero-pole-zero resonator S_{21}: Simulated versus measured results.

4.2.4 Summary of Results

Table 4.5 summarizes the measured results of the fabricated Q-enhanced resonators. Although some redesign is required to obtain the desired center frequency, measured results show the single-pole and pole-zero resonators can be Q-enhanced to the point of being lossless, giving validity to the simulated results.

Table 4.5: Summary of measured Q-enhanced resonators used for single stage filters tuned for 0 dB insertion loss.

Structure	**FET**	$\mathbf{I_{ds}}$ **(mA)**	$\frac{\mathbf{f_0}}{\textbf{-3 dB BW}}$
Single-Pole (1 nH)	D-FET	11.75	2.5
Pole-Zero (2 nH)	D-FET	3	1.62

Chapter 5

Filter Design

Having successfully Q-enhanced individual LC resonators, higher order filters can be designed using these structures. In this chapter, a procedure for designing a second-order Butterworth bandpass filter is introduced and then applied using the Q-enhanced resonators presented in Chapter 4. Measured results of fabricated filter designs are presented.

5.1 Design Procedure

The filter structure used in this thesis is a second-order Butterworth bandpass filter. Filter designs were limited to second-order due to die area constraints.

5.1.1 Second-Order Butterworth Bandpass Filter Design

A lumped element, second-order Butterworth filter is shown in Figure 5.1 [20]. The first step in the design of the filter is to design the resonators (L_r and C_r). Given the desired center frequency of the filter (f_0) and the inductor value[1] (L_r), the required capacitance is simply:

[1] As with the designs in Chapter 4, the resonator inductor value is treated as an independent variable, restricted to the baseline inductors designed in Chapter 2.

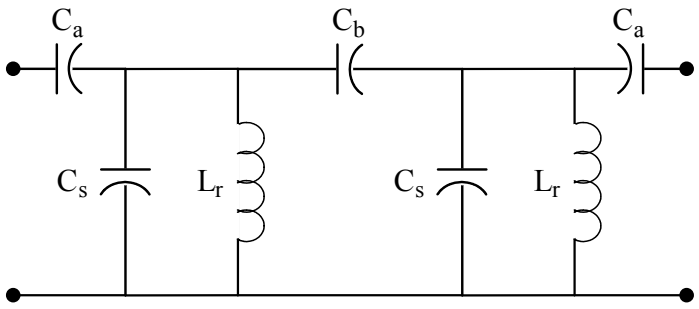


Figure 5.1: Second-order Butterworth bandpass filter. Note that C_s is the compensated resonator capacitance (Eqn. 5.4).

$$C_r = \frac{1}{(2\pi f_0)^2 L_r} \tag{5.1}$$

The next step is to find the capacitive coupling required between the resonators. The value of C_b can be found by:

$$C_b = \frac{1}{1.414(2\pi f_0)^2 L_r} \left(\frac{f_{upper} - f_{lower}}{f_0} \right) \tag{5.2}$$

where (f_{upper} - f_{lower}) is the desired -3 dB bandwidth of the filter. It is important to point out that C_b is proportional to the -3 dB bandwidth and, hence, the selectivity of the filter.

Next, the input and output coupling capacitances can be found by:

$$C_a = \frac{1}{2\pi f_0 Z_0} \sqrt{\frac{2\pi f_0 C_b Z_0}{1 - 2\pi f_0 C_b Z_0}} \tag{5.3}$$

where Z_0 is the characteristic impedance of the system (50 Ω for the designs presented in this thesis).

Finally, the capacitive coupling will act to offset the resonator slightly, so the capacitance of the shunt resonator must be reduced slightly to compensate. The compensated resonator capacitance (C_s) is found by:

$$C_s = C_r - C_b - \frac{C_a}{1 + (2\pi f_0 C_a Z_0)^2} \tag{5.4}$$

As with the compensation required of the resonator capacitance due to the capacitance generated by the negative resistance circuit (discussed in Chapter 4), the above compensation can also affect the loss of the passive resonator. Therefore, a rigorous design of the Q-enhanced resonator requires that the loss of the resonator be recalculated and the negative resistance circuit be redesigned. However, for the high-selectivity filters designed in this thesis, where C_b and C_a are very small relative to C_r (C_a and $C_b \sim 0.1$ - 0.5 pF, $C_r \sim 3$ - 5 pF), the change in loss due to this minor compensation is negligible.

5.1.2 Design and Simulation

Second-order Butterworth bandpass filters were designed using both passive and Q-enhanced single-pole and pole-zero resonators. The zero-pole-zero resonators were not used in filter designs due to die area constraints. Each resonator was designed for a 60 MHz -3 dB bandwidth centered at 1.88 GHz, corresponding to the North American PCS transmit band.

Three[2] second-order Butterworth bandpass filters based on the single-pole resonator structure were designed. The first [Fig. 5.2(a)] uses a passive 1 nH single-pole resonator. Simulations (Fig. 5.3) predict an insertion loss of 21.8 dB at 1.88 GHz and a -3 dB bandwidth of 150 MHz. This reduction in the selectivity of the filter is a consequence of the resonator loss. In the other two filters, this passive resonator is Q-enhanced and tuned for 0 dB insertion loss at the center frequency of the filter. One filter uses the Q-enhanced resonator with a 1 mm D-FET (presented in Section 4.1.5) [Fig. 5.2(b)]. When tuned to 0 dB of insertion loss, simulations confirm a -3 dB bandwidth of 60 MHz and predict a current consumption of 23.11 mA at $V_{ds} = 3$ V. The second Q-enhanced filter utilizes the negative resistance circuit used to Q-enhance the pole-zero resonators in the previous chapter [Fig. 5.2(c)]. Again, simulations confirm a -3 dB bandwidth of

[2]Two additional filters based on the single-pole resonator were actually designed using a passive 2 nH single-pole resonator and a Q-enhanced 2 nH single-pole resonator. Though both were fabricated, unfortunately, neither was able to be measured due to layout errors. Furthermore, the simulation of the Q-enhanced 2 nH single-pole resonator appears to be errant. Therefore, neither of these structures will be discussed.

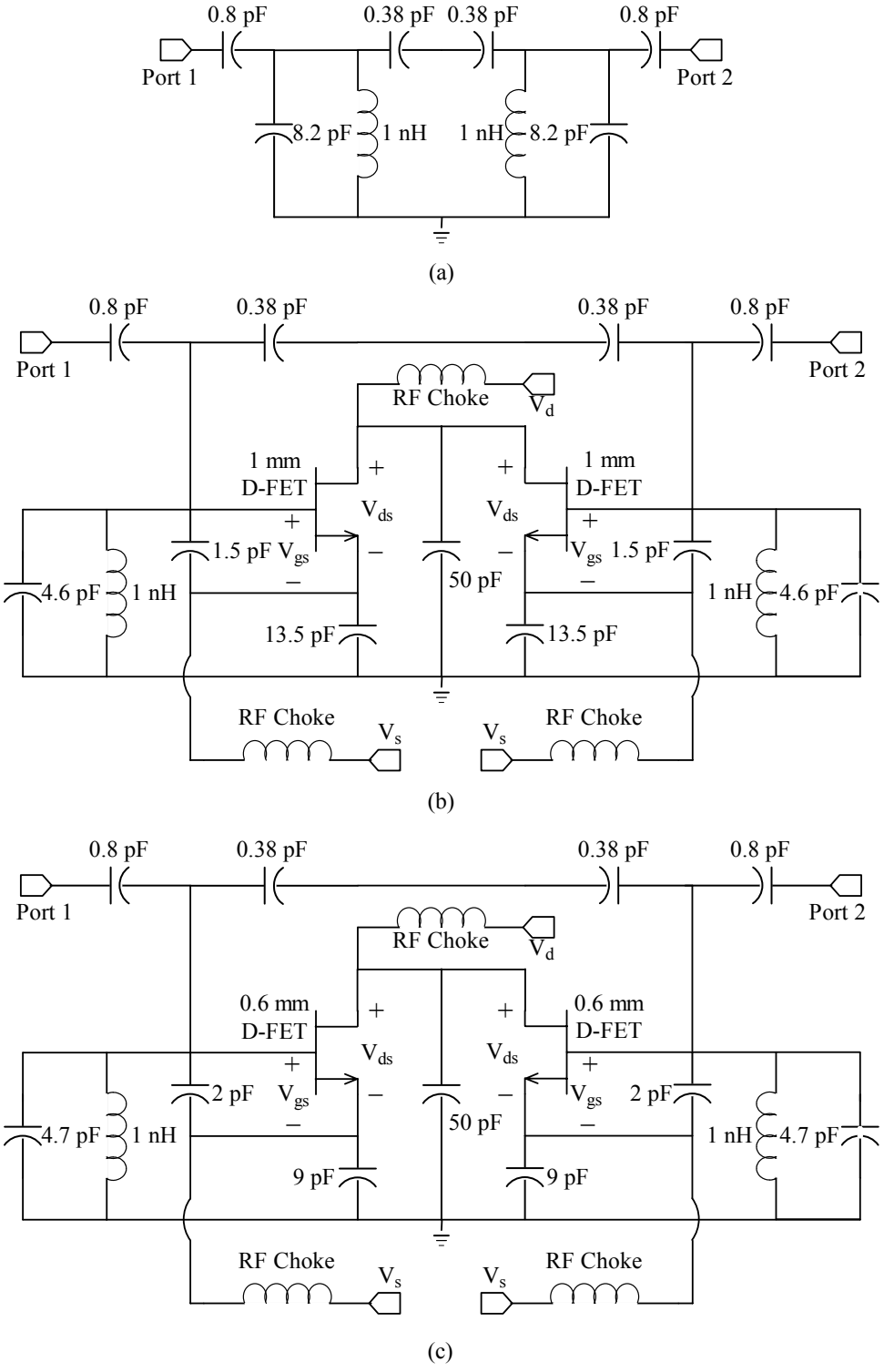


Figure 5.2: Second-order Butterworth bandpass filter designs using single-pole resonators: (a) Passive 1 nH single pole resonator; (b) Q-enhanced 1 nH single pole resonator with 1 mm D-FET; (c) Q-enhanced 1 nH single pole resonator with 0.6 mm D-FET.

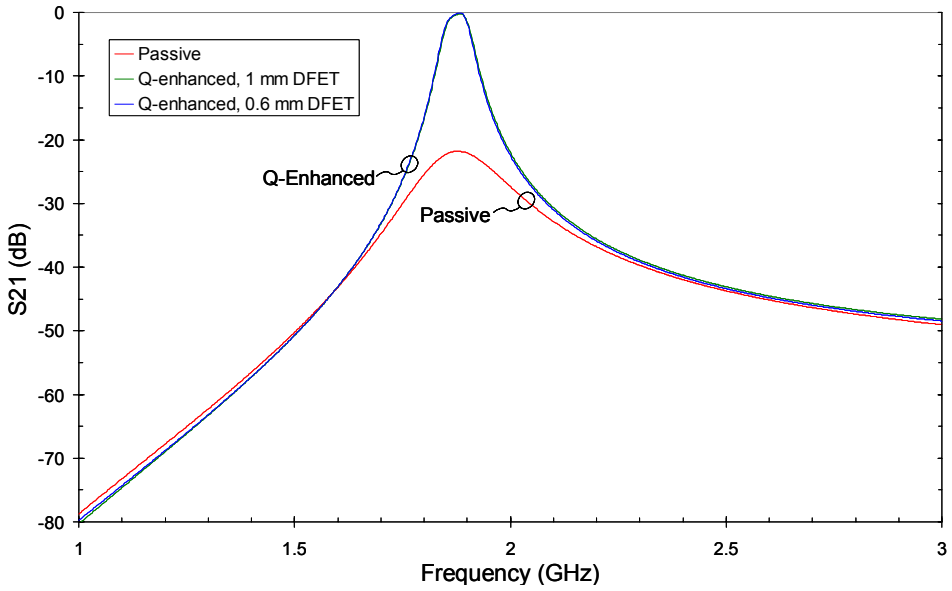


Figure 5.3: Second-order Butterworth bandpass filter simulation using single-pole resonators.

60 MHz and predict a current consumption of 17.7 mA at $V_{ds} = 3$ V.

Two second-order Butterworth bandpass filters based on the pole-zero resonator structure were also designed. The first uses the passive 2 nH pole-zero resonator from Section 4.1.5 [Fig. 5.4(a)]. Simulations of this circuit (Fig. 5.5) predict an insertion loss of 27.4 dB at 1.88 GHz and a -3 dB bandwidth of 110 MHz. The second filter uses the Q-enhanced 2 nH pole-zero resonator from the previous chapter [Fig. 5.2(b)]. The effect of compensating the resonator capacitance, due to the capacitance of the negative resistance circuit, can be seen as the zero is shifted higher in frequency when Q-enhanced. When tuned for 0 dB insertion loss, simulations confirm a 60 MHz -3 dB bandwidth at 1.88 GHz and predict a current consumption of 4.38 mA at $V_{ds} = 3$ V.

One unexpected and unexplained result of these simulations is that the total current consumption of the two negative resistance circuits in each of these filters is less than twice the simulated current consumption (at the same voltage bias) of the individual Q-enhanced resonators presented in the previous chapter (Section 4.1.5). For example, simulations show that the filter using the Q-enhanced 1 nH single-pole resonator with 1 mm D-FET consumes 23.11 mA while simulations show the individual resonators consume 13.8 mA each. Therefore, should these results be verified in measurement, diminishing marginal current consumption may occur in the design of higher order filters

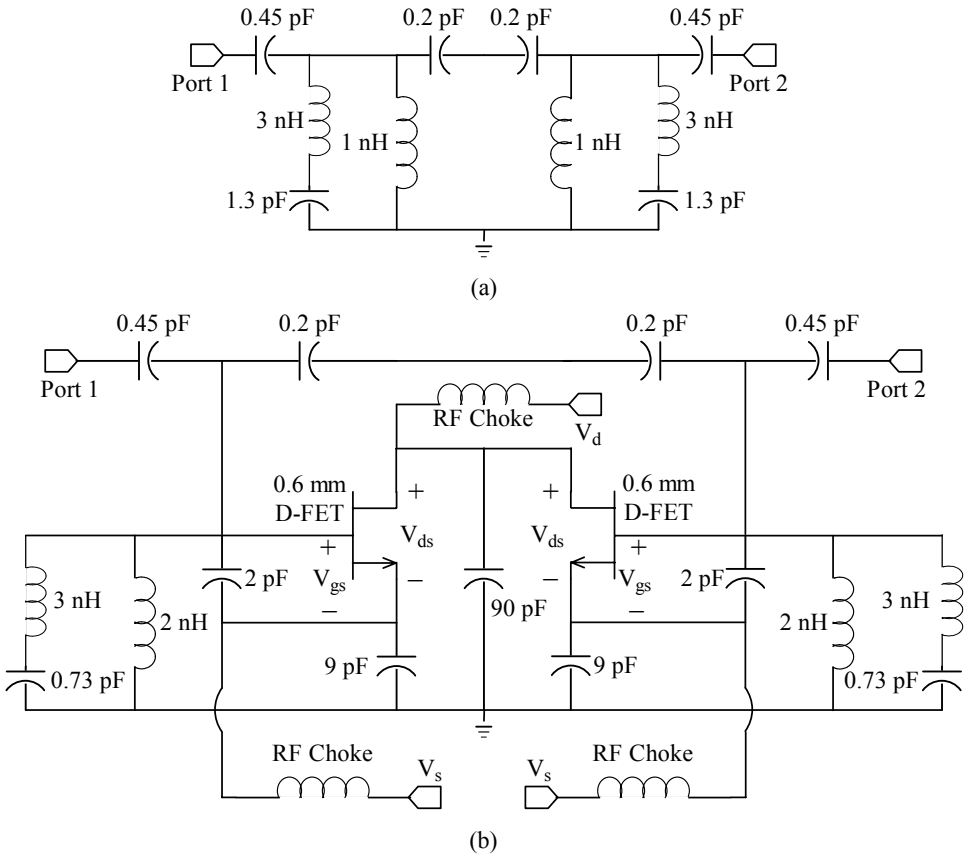


Figure 5.4: Second-order Butterworth bandpass filter designs using pole-zero resonators: (a) Passive 2 nH single pole-zero; (b) Q-enhanced 2 nH pole-zero resonator with 0.6 mm D-FET.

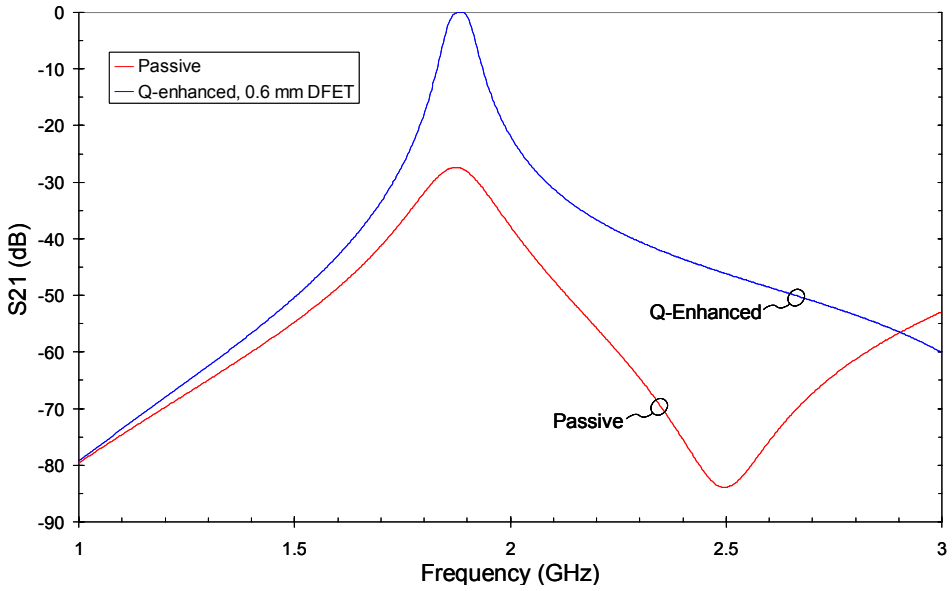


Figure 5.5: Second-order Butterworth bandpass filter simulation using pole-zero resonators.

It is also interesting to note that, despite the passive pole-zero resonator having less loss than the passive single-pole resonator, the filter corresponding to the passive pole-zero resonator has a greater passband insertion loss than the filter corresponding to the passive single-pole resonator. This is because the 2 nH pole-zero resonators must be more tightly coupled than the 1 nH single-pole resonators to result in the same -3 dB bandwidth. Therefore tightly coupling the resonators will magnify the effects of the resonator loss. When Q-enhanced, however, the loss of each individual resonator is reduced prior to coupling, thereby making the Q-enhancement independent of the coupling. Therefore, it is more power efficient to Q-enhance each individual resonator then to Q-enhance the passive filter.

5.2 Fabrication and Measurement

5.2.1 Layouts

Seven filter test designs, a 2 nH baseline inductor test structure, and a capacitor test structure (shown in Figures A.5-A.9 in Appendix A) were fabricated (M/A-COM E/D SAGFET process) in the second phase of this thesis. These structures include:

- 5.2 pF capacitor (layout: A.8)
- 2 nH baseline spiral inductor (layout: A.8)
- Second-order Butterworth bandpass filter using passive 1 nH single-pole resonator [schematic: Fig. 5.2(a), layout: A.8]
- Second-order Butterworth bandpass filter using Q-enhanced 1 nH single-pole resonator with 1 mm D-FET [schematic: Fig. 5.2(b), layout: A.5]
- Second-order Butterworth bandpass filter using Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET [schematic: Fig. 5.2(c), layout: A.6]
- Second-order Butterworth bandpass filter using passive 2 nH single-pole resonator [layout: A.8]
- Second-order Butterworth bandpass filter using Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET [layout: A.7]
- Second-order Butterworth bandpass filter using passive 2 nH pole-zero resonator [schematic: Fig. 5.4(a), layout: A.8]
- Second-order Butterworth bandpass filter using Q-enhanced 2 nH pole-zero resonator with 0.6 mm D-FET [schematic: Fig. 5.4(b), layout: A.9]

Figure 5.6 shows the layout of the second-order Butterworth bandpass filter using Q-enhanced 1 nH single-pole resonator with 1 mm D-FET as an example of the general layout structure used for the all the filters designed. Coupling capacitors are placed at either input (C_a), and between the two resonators (C_b). Due to the small value of C_b, the relatively long physical length between the two resonators, and the desire to keep the layout symmetric, C_b was actually realized by placing two capacitors of of value $2C_b$ in series.

The core resonators are virtually identical to those fabricated in the previous chapter. However, to compensate for the lower capacitances measured in Section 4.2.3, an additional 0.9 pF was added in parallel with C_r (labeled $C_{r,add}$) for each the 1 nH single-pole resonators. The value of $C_{r,add}$ was determined from simulation by placing an additional capacitance in parallel with the data file representing the measured results, and tuning

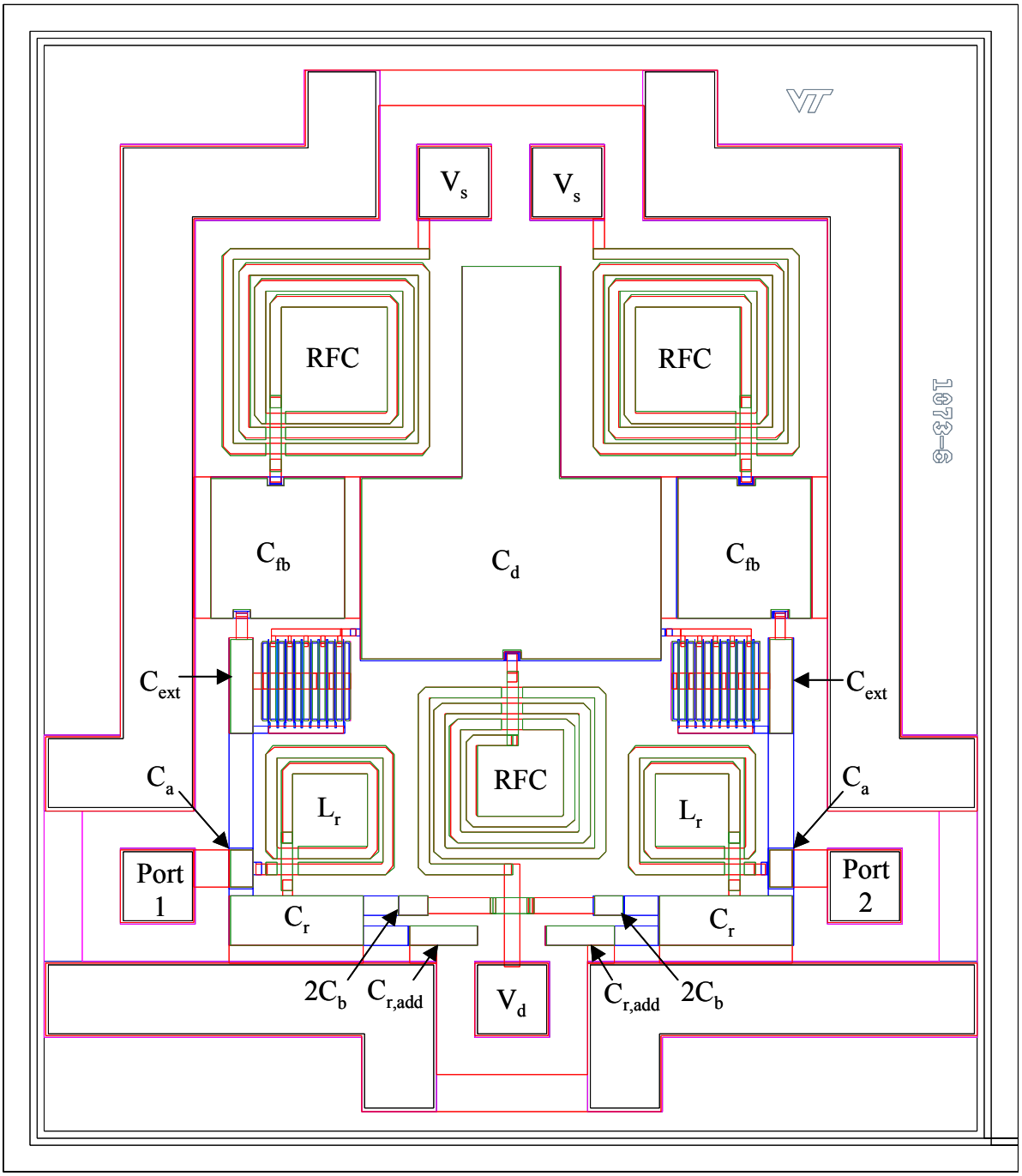


Figure 5.6: 2^{nd} order Butterworth filter with 1 mm D-FET Q-enhanced 1 nH LC resonators.

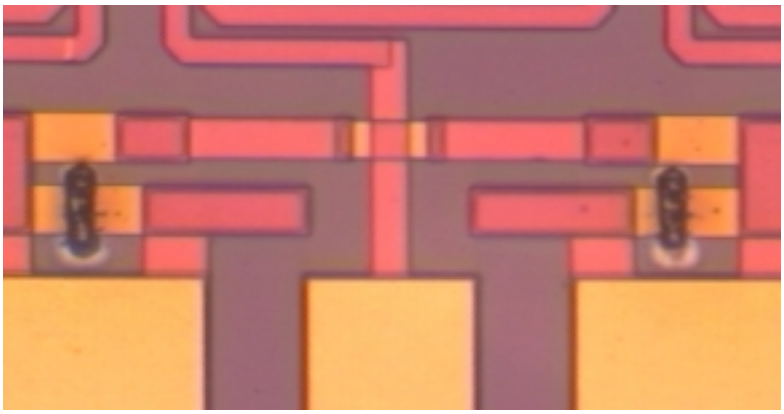


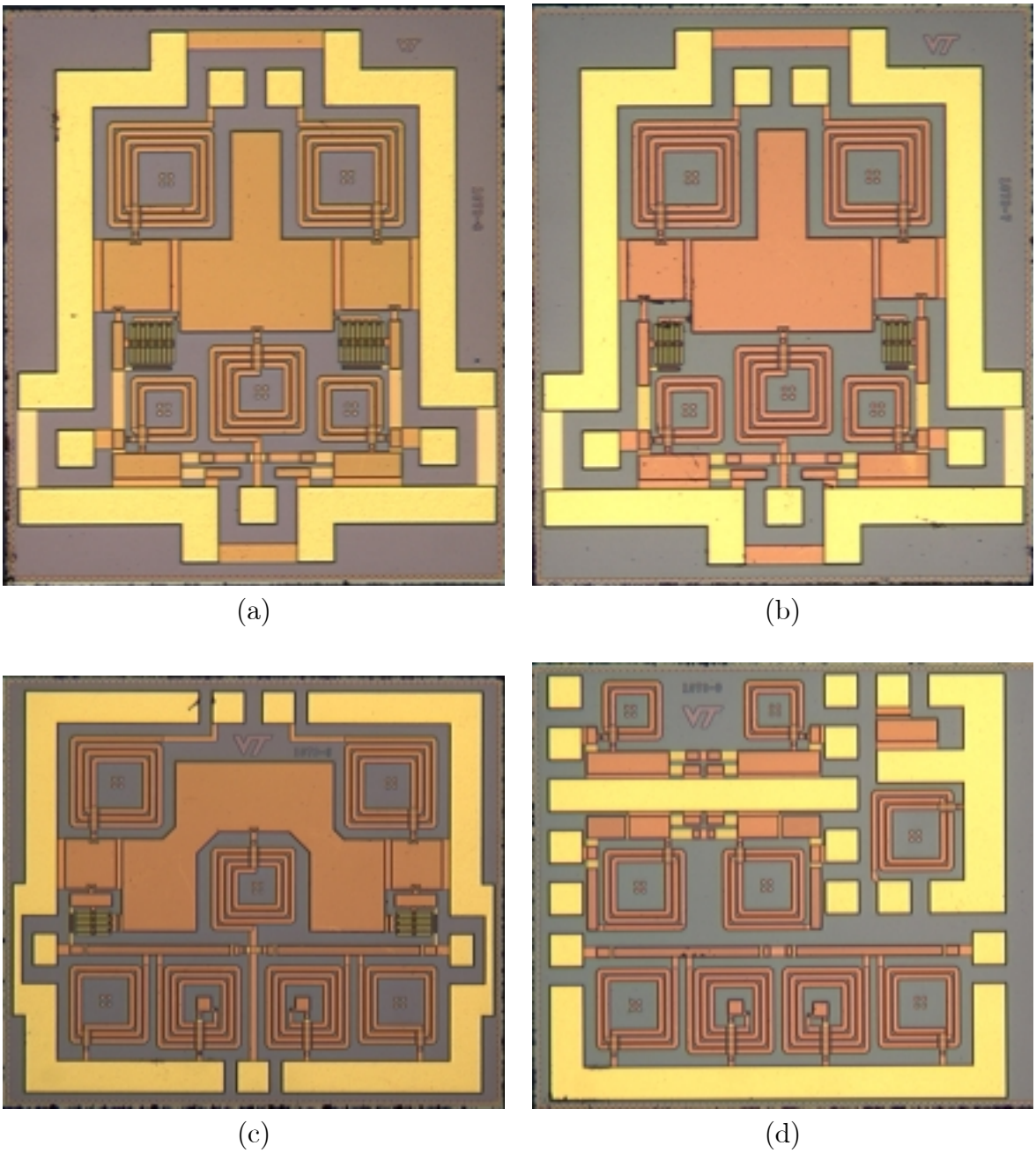
Figure 5.7: Laser trimmed traces to remove $C_{r,add}$.

the capacitance until the correct pole frequency was attained. This additional capacitance could be removed from the circuit by laser trimming the traces connecting C_r and $C_{r,add}$ in parallel (as shown in Figure 5.7) if the capacitance deviation did not reoccur.

The filter layouts also included the RF chokes and DC blocks in order to avoid post-fabrication assembly. The DC blocking capacitor (C_d) is connected to the drain of each FET and grounded through the bottom plated of C_{fb}. The value of C_d is anywhere from 50 pF to 90 pF, depending on the die area available with each filter structure. Furthermore, the drain voltage is applied to the pad labeled V_d and injected through an RF choke (RFC), through the top plate of C_d, to the drain of each FET. The source of each FET is biased using separate circuits to limit feedback and to allow for the bias points of one FET to be set independently of the other. For each circuit, the source voltage is applied to the pad labeled V_s and injected through an RF choke, through the top plate of C_{fb}, through the bottom plate of C_{ext}, to the source of the FET.

Finally, a ground ring surrounds the filter structures such that the ports labeled Port 1, Port 2, and V_d can be probed using a 150 μm pitch Ground-Signal-Ground (GSG) probe and the port labeled V_s can be probed using a 150 μm pitch, 4 finger DC probe. However, due to limited die area, for a few of the filter designs, the ground ring did not fully encompass the circuit (ex. A.9).

Figure 5.8 shows photographs of 4 of the 5 chips fabricated. The bright gold corresponds to areas of exposed metal, where the top passivation layer has been opened to facilitate probing of the circuits.



(a) (b)

(c) (d)

Figure 5.8: Pictures of fabricated filters using: (a) Q-enhanced 1 nH single-pole resonators with 1 mm D-FET; (b) Q-enhanced 1 nH single-pole resonators with 0.6 mm D-FET; (c) Q-enhanced 2 nH pole-zero resonator; (d) passive resonators and other test structures.

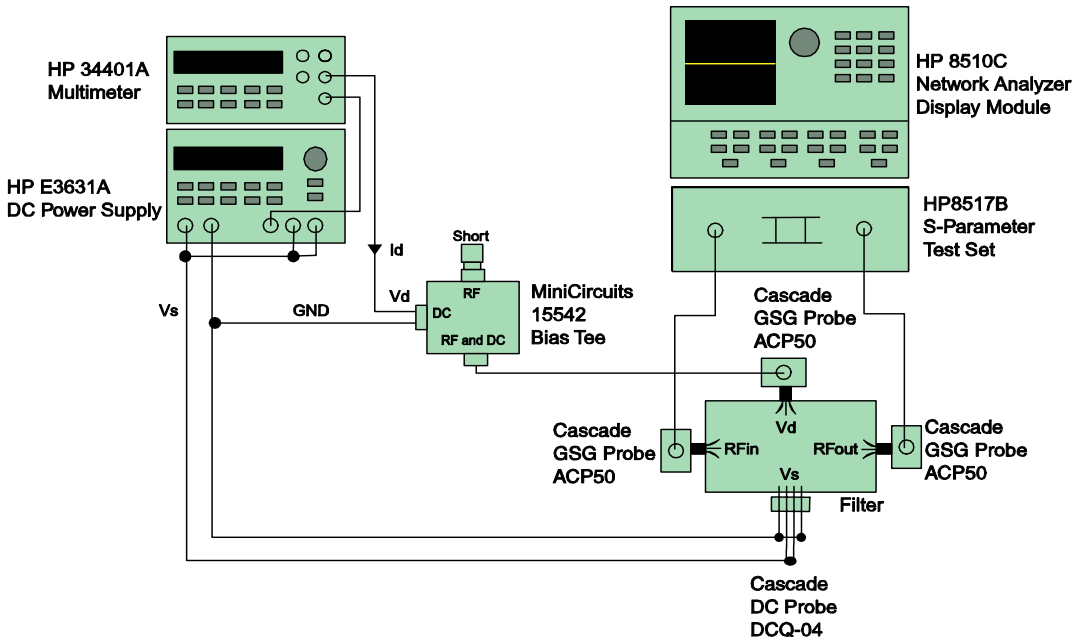


Figure 5.9: Filter S-Parameter test setup.

5.2.2 Measurements

Three measurements were performed to characterize the performance of the fabricated filters: (1) small-signal S-Parameters; (2) noise figure; (3) 1 dB compression test.

Small-Signal S-Parameters

The two-port S-Parameters of the filter were measured versus frequency and bias using the setup shown in Figure 5.9. A two-port Short-Open-Load-Through (SOLT) calibration was performed using a Cascade calibration substrate. An automated extraction program was written and used to record the S-Parameters and power consumption at various bias points to a data file using the MDIF format (shown in Appendix B). These data files were imported into Series IV [5] for comparison to the results predicted in simulation

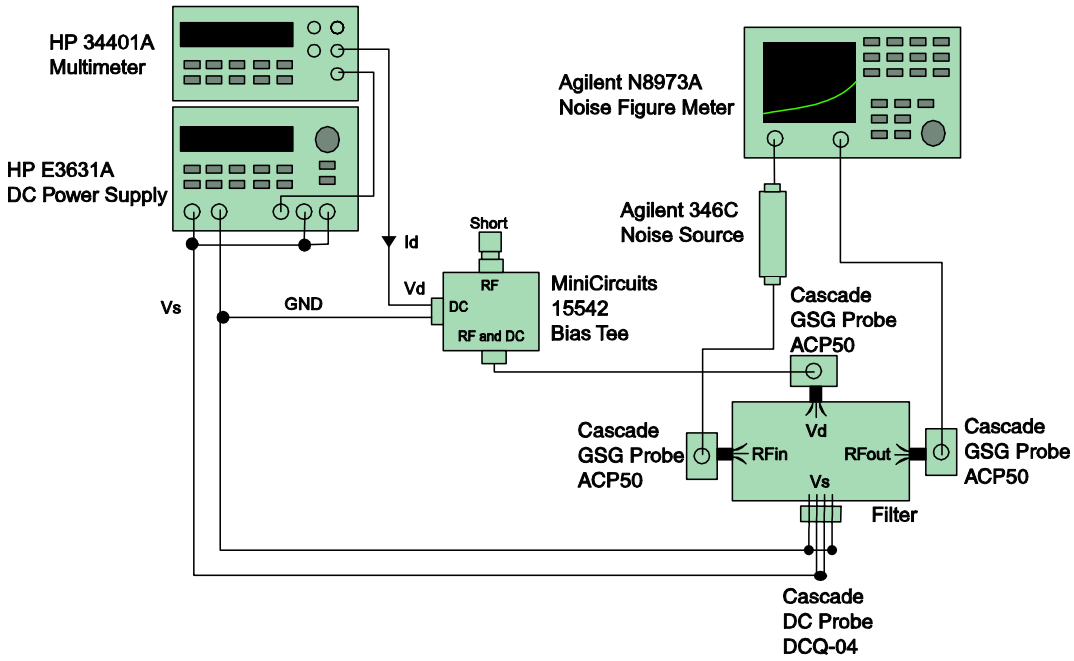


Figure 5.10: Filter noise figure test setup.

Noise Figure

The noise figure in the passband of each filter was measured at five bias points, corresponding to a filter insertion loss of -10, -5, 0, 5, and 10 dB. The measurement was made using an Agilent N8973A Noise Figure Meter and the setup shown in Figure 5.10. The loss of the cables and probes in the setup were calibrated out by probing a threw line on the Cascade calibration substrate and calibrating the noise figure meter.

Linearity

The 1 dB compression point of each filter was measured at two bias points, corresponding to a filter insertion loss of -10 and 0 dB. The setup for this measurement is shown in Figure 5.11. In order to verify that the power meter was measuring the power of the fundamental tone with negligible contributions from higher order harmonics, a spectrum analyzer was also used to verify the compression of the fundamental tone. However, the spectrum analyzer was not used for the compression measurement due to its limited magnitude precision. The calibration for this measurement was performed in two steps. First, the

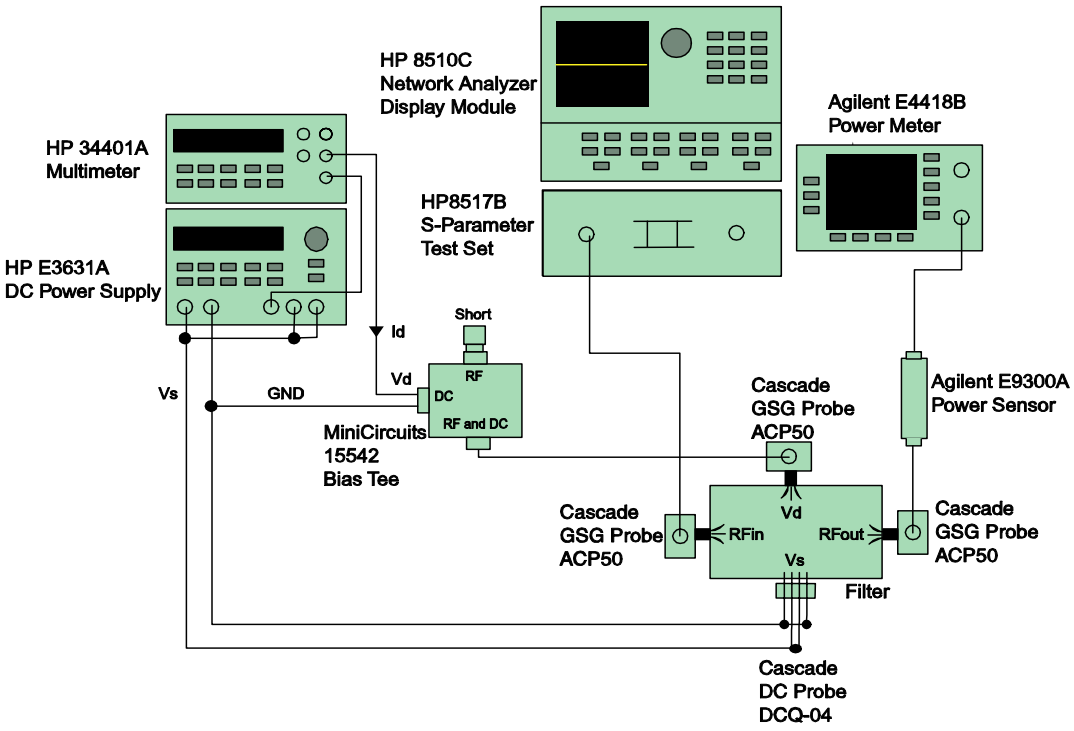


Figure 5.11: 1 dB compression point test setup.

offsets between the set source power and the power measured (using the power meter) at the port of the S-parameter test set were recorded at each power level. Secondly, using identical cables from the input and output probes, the loss of the cables and probes were determined by probing a through line on the Cascade calibration substrate and measuring the power after the output cable. The loss between the source and the input of the device was assumed to be half this loss.

Using this setup, the compression point was measured by:

1. Starting at an input power well below the compression point, recording the difference between the input and output power.

2. Increasing the input power level and measuring the difference between the input and output power. (Repeating until the difference between the input and output power increases by 1 dB.)

The resulting input/output 1 dB compression point is the input/output power corre-

sponding to this 1 dB increase (calibrated to the input/output of the device).

5.2.3 Measured Results

Second-order Butterworth filters corresponding to the:

- Passive 1 nH single-pole resonator
- Q-enhanced 1 nH single-pole resonator with 1 mm D-FET
- Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET
- Passive pole-zero resonator

were measured as described in the previous section. Each of the filters based on single-pole resonators were measured with the additional 0.9 pF resonator capacitance included in the layout. Unfortunately, the second-order Butterworth filters corresponding to the passive 2 nH single-pole resonator, Q-enhanced 2 nH single-pole resonator with 0.6 mm D-FET, and Q-enhanced pole-zero resonator were not able to be measured due to layout errors.

Small-Signal S-Parameters

Figure 5.12 shows the measured transmission response (S_{21} versus frequency) of the filter based on the passive 1 nH single-pole resonator. Despite the additional 0.9 pF of resonator capacitance, the pole frequencies of the filter are still slightly higher than simulated. The mean average of the responses indicates an insertion loss of 22.2 dB and a -3 dB bandwidth of 180 MHz at a center frequency of 1.97 GHz.

The insertion loss/gain of each of the filters using Q-enhanced resonators can be tuned by changing the operating point of the FET. Figure 5.13 shows the frequency response of S_{21} for one of the filters based on Q-enhanced 1 nH single-pole resonators with 1 mm D-FET at bias points corresponding to a passband insertion loss/gain of -10, -5, 0, 5, and 10 dB. There are two notable effects on the response as drain current increases: (1) the pole frequencies of the filter shift higher in frequency, and (2) the coupling of each of the

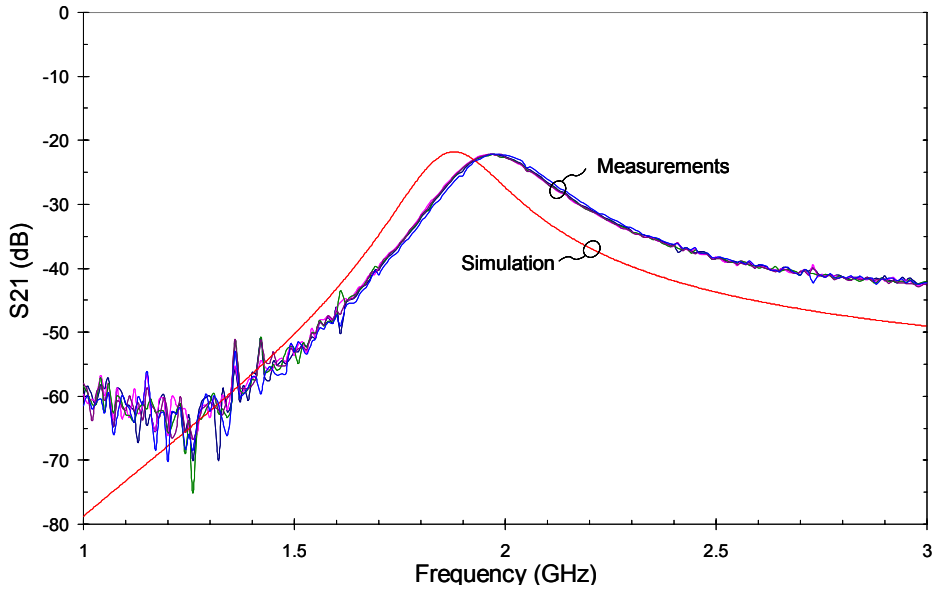


Figure 5.12: S_{21} of filter based on passive 1 nH single-pole resonator.

resonators is reduced, leading to greater ripple in the passband. Both of these effects are due to a decrease in the parallel equivalent capacitance of the negative resistance circuit ($C_{p,neg}$) with the g_m of the FET (or drain current). This decrease in $C_{p,neg}$ is due to an increase in the series negative resistance (R_{neg}). When R_{neg} is increased, the Q of the series negative resistance circuit is decreased, leading to a decrease in $C_{p,neg}$ (see Section 3.4). Therefore, a bias point must be chosen prior to the final design of the filter in order to achieve the desired passband response.

Figure 5.14 shows the measured transmission response of the filter based on the Q-enhanced 1 nH single-pole resonator with 1 mm D-FET. When biased for 0 dB insertion loss, the measured -3 dB bandwidth of the mean response was 42.5 MHz at a center frequency of 1.8425 GHz and a current consumption of 18-19 mA at V_{ds} = 3V. Again the errors in capacitor values are the likely cause of the deviation from simulation. The narrower than expected -3 dB bandwidth is most likely due to the fabricated coupling capacitors being smaller than predicted by simulations

The transmission response of the filter based on the Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET is shown in Figure 5.15. When biased for 0 dB insertion loss, the measured -3 dB bandwidth of the mean response was 42.5 MHz at a center frequency of 1.845 GHz and a current consumption of 16-17 mA at V_{ds} = 3V.

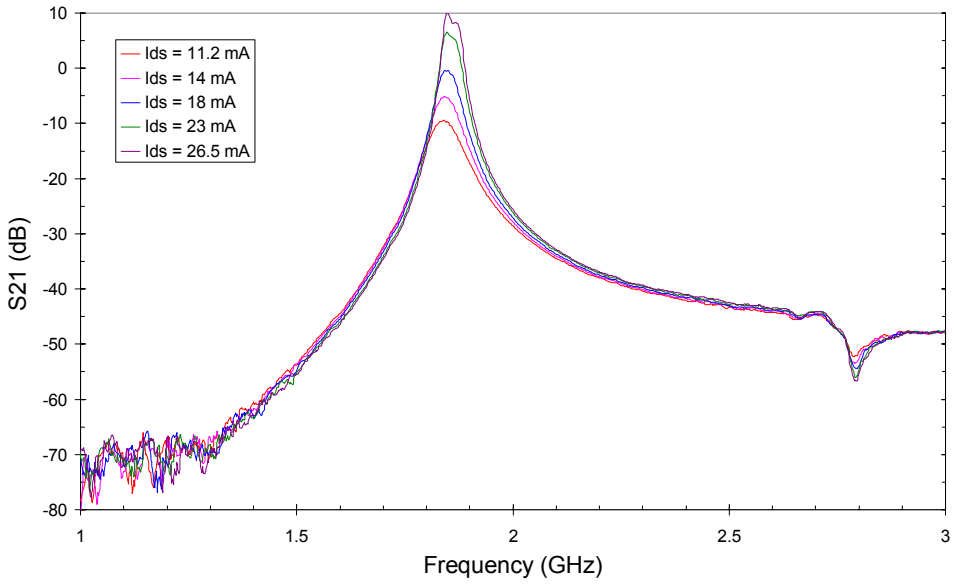


Figure 5.13: Frequency response of S_{21} versus FET bias point for filter based on Q-enhanced 1 nH single-pole resonator with 1 mm D-FET.

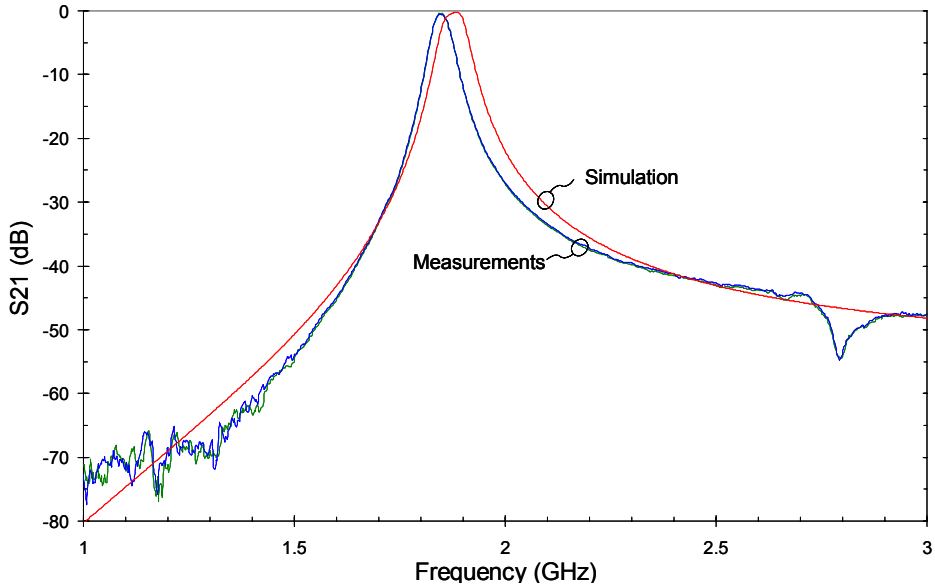


Figure 5.14: S_{21} of filter based on Q-enhanced 1 nH single-pole resonator with 1 mm D-FET.

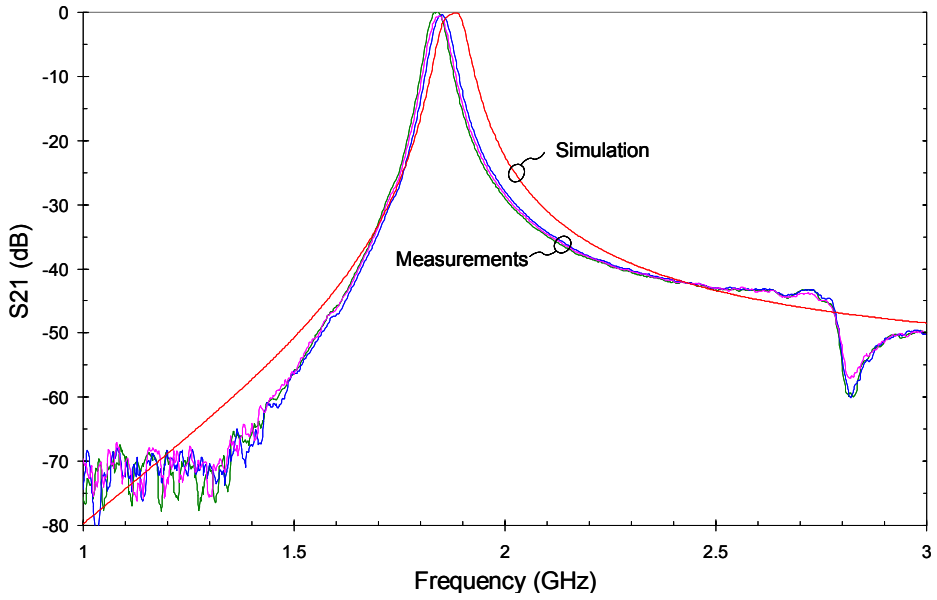


Figure 5.15: S_{21} of filter based on Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET.

Finally, the transmission response of the filter based on the passive 2 nH pole-zero resonator is shown in Figure 5.16. There were a few suspect connections in the capacitive arm of these resonators, which effectively removed the capacitance from the resonator, causing this shift in the pole frequencies. This would account for the high pole frequencies since the resonator inductor would parallel resonate with the capacitance due to the negative resistance circuit at roughly 2.5 GHz. Furthermore, this would account for the zero not being seen in the measured response

An unexpected result of the simulation of these filters (Section 5.1.2) that was verified in these measurements is that the current required to tune the filter to 0 dB insertion loss is less than twice the value required to tune the individual single-resonator filters (Section 4.2.3). While there is no obvious explanation for this effect, it is advantageous for the design of higher order filters.

In summary, compared to simulation, the realized capacitors appear to be smaller than simulated, resulting in: (1) shifted pole frequencies; and (2) too much capacitive coupling leading to a narrower than simulated -3 dB bandwidth.

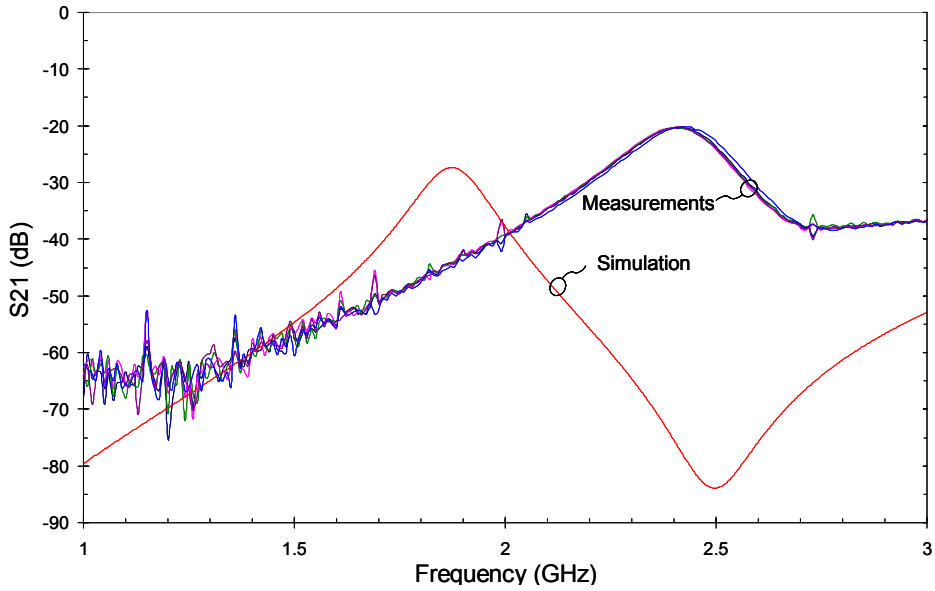


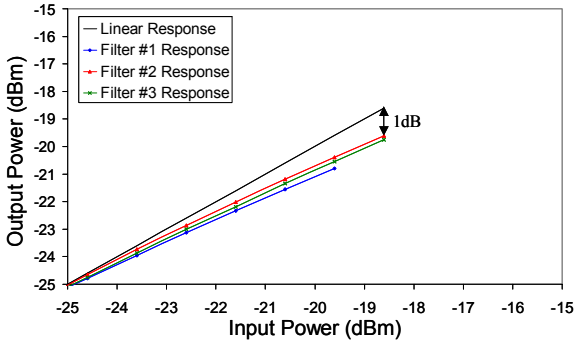
Figure 5.16: S_{21} of filter based on passive 2 nH pole-zero resonator.

Linearity

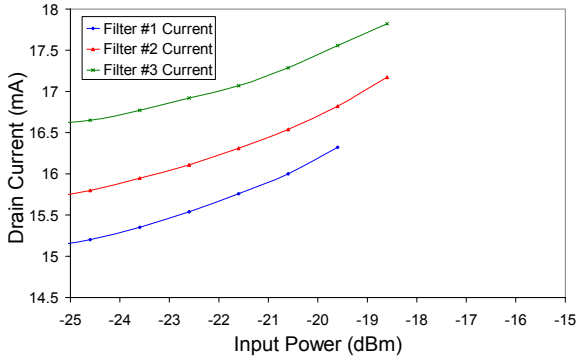
The linearity of the filters, as measured by the 1 dB compression point, corresponding to the Q-enhanced 1 nH single-pole resonator with 1 and 0.6 mm D-FET are shown in Figure 5.17. The linearity of each filter [3 samples for the 1 mm D-FET (#1-3) and 2 sample for the 0.6 mm D-FET (#1-2)] at 0 dB insertion loss is shown in Figures 5.17 (a) (1 mm D-FET) and (c) (0.6 mm D-FET). Furthermore, the filter using the Q-enhanced 1 nH single-pole resonator with 0.6 mm D-FET was also measured at an insertion loss of -10 dB [Fig. 5.17(d)]. Finally, Figure 5.17 (b) shows how the drain current increased with the input power .

The usefulness of this measurement is limited given that the drain current was able to increase with input power [Fig. 5.17(b) as an example]. This occurred because the source voltage was held constant by an external voltage source independent of I_{ds}. This allowed these circuits to compensate for the increase in input power by increasing I_{ds} and g_m, thereby increasing the gain of the filter. Were the circuit self-biased (replacing the this voltage source with resistor tuned to provide the proper source voltage) as is typically required in actual product design, any increase in drain current would have been counteracted by an increase in source voltage, thereby reducing V_{gs}, which would

Q-enhanced with 1 mm D-FET (C_{fb} = 13.5 pF, C_{ext} = 1.5 pF)

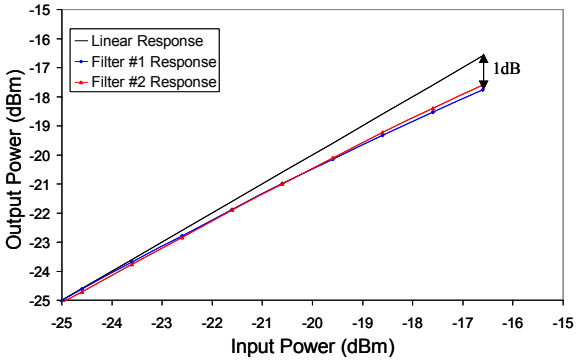


(a)

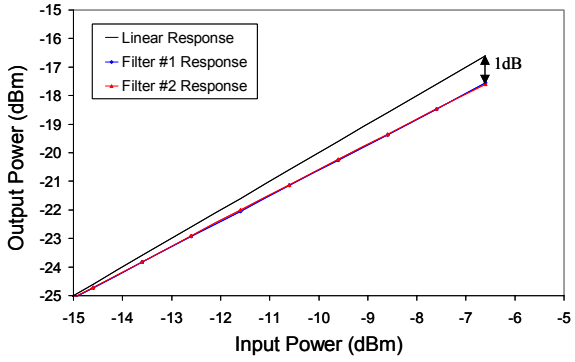


(b)

Q-enhanced with 0.6 mm D-FET (C_{fb} = 9 pF, C_{ext} = 2 pF)



(c)



(d)

Figure 5.17: 1 dB compression point measurements: (a) Compression point of filter using Q-enhanced 1 nH single pole resonator with 1 mm D-FET at 0 dB insertion loss; (b) Drain current increase as a function of input power; (c) Compression point of filter using Q-enhanced 1 nH single pole resonator with 0.6 mm D-FET at 0 dB insertion loss; (d) Compression point of filter using Q-enhanced 1 nH single pole resonator with 0.6 mm D-FET at -10 dB insertion loss.

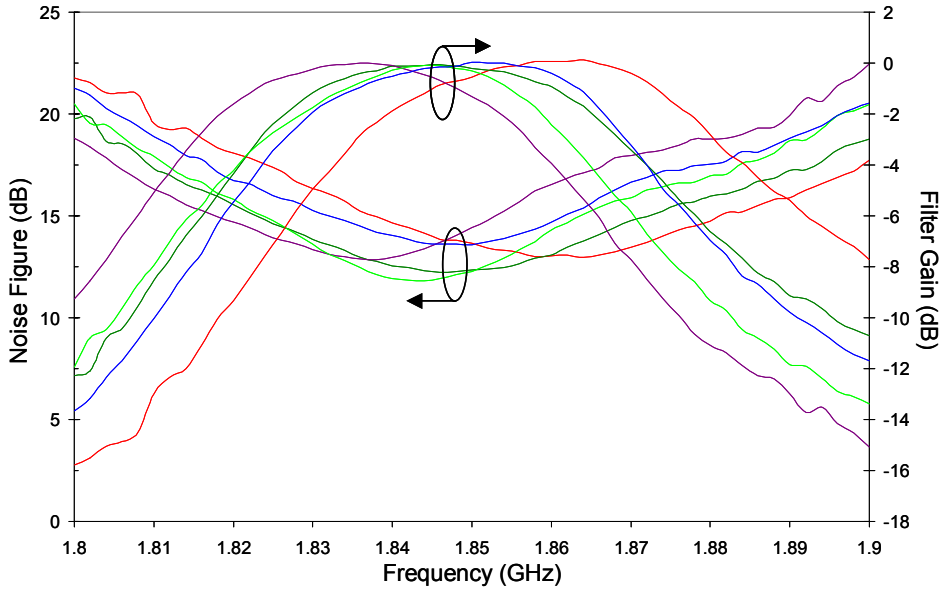


Figure 5.18: Passband noise figure and gain of each Q-enhanced design at 0 dB insertion loss.

in turn reduce the I_{ds}.

However, considering the measurements on a relative basis, a number of interesting results are evident. First, comparing the results of the 0.6 mm D-FET filter at 0 and -10 dB insertion loss, the output 1 dB compression point remains the same regardless of the gain of filter. Secondly, as predicted by Cheng and Chan [18], the negative resistance circuit with the lower C_{fb} has a higher 1 dB compression point. The difference would have been even more substantial if the two circuits were compared on the basis of equal FET size since the larger FET slightly offsets the effect of the larger C_{fb}.

Noise Figure

Finally, the noise figure of the passband of each of the filters using Q-enhanced resonators was measured. Figure 5.18 shows the frequency response of the noise figure and gain of each filter. In each case, the minimum passband noise figure corresponds to the frequency at which the filter has minimum insertion loss. At 0 dB insertion loss, the noise figure of the filters range between 12 and 13 dB. Neither design (1 mm D-FET or 0.6 mm D-FET) distinguishes itself from the other on the basis of noise figure.

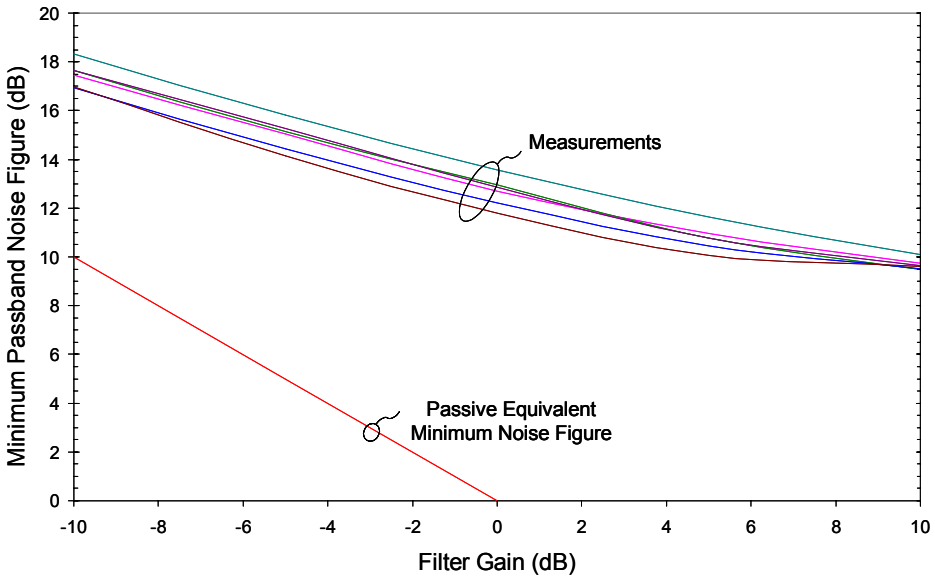


Figure 5.19: Filter noise figure as a function of filter gain (insertion loss).

Figure 5.19 plots the minimum passband noise figure (measured at the frequency corresponding to minimum insertion loss) as a function of the gain (or insertion loss) of the filter. Furthermore, in order to distinguish between the noise due to the loss of the filter and the noise contributed by the active elements, the noise figure of the passive equivalent filter (a passive filter that has the same insertion loss) is also shown. The difference in the slope of the filter measurements and that of the passive equivalent reflects the amount by which the noise contribution by the active components increases with the filter gain (primarily due to increased channel current I_{ds}).

5.2.4 Measurement Conclusions

Unfortunately, due to the problems with the filters based on the 2 nH single-pole resonator and the filter based of the Q-enhance 2 nH pole-zero resonator, few specific conclusions can be drawn at this point. One comparison that can be made is between the D-FET negative resistance circuits used to Q-enhance the 1 nH single-pole resonators (Table 5.1). Clearly, the negative resistance circuit with the 0.6 mm D-FET is superior to the negative resistance circuit with the 1 mm D-FET on the basis of current consumption, linearity, and die area.

Table 5.1: Comparison of negative resistance circuits based on filter measurements made with filters biased at 0 dB insertion loss.

Negative Resistance Circuit	Effective Die Area (w/o RFCs and C_d)	Current (mA)	Output Compression Point	Noise Figure (dB)
1 mm D-FET C_{fb} = 13.5 pF C_{ext} = 1.5 pF	245,000 μm^2	18-19	$\backsim$-18dBm	12-13
0.6 mm D-FET C_{fb} = 9 pF C_{ext} = 12 pF	198,000 μm^2	16-17	$\backsim$-20dBm	12-13

Chapter 6

Conclusions and Future Work

The objective of this work in this thesis was to develop a design methodology for low-loss LC filters, and demonstrate monolithic filter designs for PCS band applications. The former was accomplished through the discussion of each step in the design of integrated Q-enhanced LC filters. Furthermore, this thesis demonstrated through simulation and measurements a number of monolithic filter designs that have the potential for use in a number of integrated filtering applications.

6.1 Resonator Structures

One issue with the work presented in this thesis is that all the single-pole resonators presented were designed with 1 nH inductors[1], the pole-zero resonators were all designed with 2 nH inductors, and the zero-pole-zero resonators were all designed with 3 nH inductors. In examining the measured results of both the resonators and filters, one might be led to conclude that Q-enhancing pole-zero resonators is more current-efficient since the Q-enhanced filters using pole-zero resonators (designed with a 2 nH inductor) draws less current than the Q-enhanced filters using the single pole resonators (designed with a 1 nH inductor). This conclusion is incorrect because the amount of current required is based on the amount of negative resistance needed to compensate for the loss of the resonator. As was shown in Section 4.1.2 the loss of the resonator at the pole frequency

[1]Two filters based on 2 nH single pole resonators were designed, but fell victim to simulation and layout errors in the second fabrication phase of this work.

depends much more on the inductor value than on the resonator structure. In reality, for a given inductor value, the pole-zero resonator would have more loss than the single pole resonator due to the additional loss contributed by the second inductor, requiring more current to Q-enhance. The filter design based on a 2 nH single-pole resonator, had it been work, would require less power consumption than this filter based on the 2 nH pole-zero resonator to Q-enhance. Therefore, the power efficiency of the Q-enhanced resonators and filters should be compared on the basis of resonator inductance and loss, rather than the resonator structure alone.

Where the resonator structures do differentiate themselves from one another is in the frequency response of subsequent filters. Compared to filters based on the single-pole resonator, filters based on the pole-zero resonator contain a zero in the frequency response, which, if properly placed, improves the out-of-band rejection above the pole frequency. This additional functionality comes at the expense of a marginal increase in the loss of the resonator. However, the frequency response of this additional loss reduces the potential for instability when Q-enhancing the resonator. Similar results were shown for the zero-pole-zero resonator.

6.2 Potential Application

It is apparent from the measured results presented in Chapter 5 that the filters implemented in this thesis are not likely to be used in the front-end of a receiver due to their high noise figure and low compression point. However, in a transmitter, possibly as an image-reject filter, high noise figure and low linearity may not be prohibitive. For this application, the power consumption and selectivity of a Q-enhanced filter will determine its potential for application.

Assuming for the moment that the frequency selectivity is sufficient, the power efficiency of the Q-enhanced filter can be judged by comparing it to an alternative solution. One alternative is to cascade an amplifier with the passive filter to compensate for the loss. The second order Butterworth filter based on the passive 1 nH single pole resonator measured in Chapter 5 had an insertion loss of 22.2 dB. Furthermore, when Q-enhanced to achieve 0 dB insertion loss, the measured bias current required was $\backsim$16 mA (@ 3 V, 48 mW). Alternatively, a 22 dB amplifier, which might draw $\backsim$8 mA (ex. M/A-COM

MAAM12031, @ 3 V, 24 mW) cascaded with the passive filter would result in the same low-loss passband. Furthermore, this alternative would have a lower cascaded noise figure ($\backsim$5 dB for 1.46 dB amplifier NF) and roughly the same 1 dB compression point (7 dBm at the output of the amplifier, -15 dBm at the output of the filter). Therefore, the power efficiency of Q-enhancing 1 nH resonators is poor compared to simply driving a passive filter with an amplifier.

However, filters based on Q-enhanced 2 nH resonators, with the same frequency selectivity (tighter coupling capacitors), were simulated with 0 dB insertion loss at a bias current of $\backsim$3 mA. This is because the 2 nH resonators had much less loss than the 1 nH resonator, requiring less Q-enhancement. Though this solution requires a larger die area, it is far more current efficient than the cascaded amplifier-filter alternative and would have better frequency selectivity since the frequency selectivity of the passive filters was degraded by the loss.

Therefore, in terms of potential application, filters based on the Q-enhanced 1 nH resonators (or any resonator based on an inductor $<$ 1 nH) will probably not be used due to the high power consumption required to Q-enhance the relatively high-loss resonator. Filters based on tightly coupled Q-enhanced 2 nH resonators could likely be used in light of the low loss of the resonator and the lower power consumption required to Q-enhance the resonator. However, although resonators based on larger inductors would have less loss (requiring less power consumption to Q-enhance), the coupling capacitors required to achieve the desired selectivity would be prohibitively small. Therefore, Q-enhanced filters can be used, but only over a narrow range of resonator inductance values in order to achieve high selectivity and low power consumption.

6.3 Future Work

There are a few unresolved issues in this thesis that will be addressed. First, the layout errors mentioned throughout this thesis should be corrected and these designs re-fabricated. Specific results of interest include the filters based on the pole-zero resonators, which have the potential for an increased maximum stable gain, and the filters based on the 2 nH single-pole resonators, which should provide a lower-power (less current consumption) solution due to the decreased resonator loss. Secondly, the cause of the capacitance devi-

ation between simulation and measurements must be determined, and corrective action should be taken in future design iterations.

Beyond the work in this thesis, there are areas which may be able to provide potential improvement to the results presented here. Some suggestions are listed below.

6.3.1 Multi-layer Spirals

In this thesis, single-layer spirals were used in order to minimize the loss. At the time of the original design, the models for the multi-layer spiral inductors were only preliminary while the single-layer spirals models were proven. However, given that the multi-layer spiral models are now proven and can be used with confidence, their application in the filter designs could greatly reduce the die area. In particular, multi-layer spirals could be used for RF chokes, where a marginal increase in loss would not degrade the performance of the filter. The multi-layer spirals could also be used in the LC resonator; however, reduction in die area would come at the expense of a marginal increase in the power consumption required for Q-enhancement.

6.3.2 Improved Linearity

The linearity of the filters measured in this thesis were prohibitively low for many applications. Therefore, improvements are required and are possible by modifying the design of the negative resistance circuits. Chen et al. demonstrated in [18] that the linearity of the filter can be improved by reducing the value of C_{fb} in the negative resistance circuit. Indeed, in the measurements presented in Chapter 5, the filter with the lowest C_{fb} had the highest 1 dB compression point. Therefore, C_{fb} should be further reduced in future filter designs to help further improve the linearity. Furthermore, the filters presented with the smallest C_{fb} were designed with a smaller FET which offset the improvement in linearity. In this case, increasing the size of the FET should also improve the linearity.

6.3.3 Negative Resistance Circuits/Stability Analysis

As was discussed in Section 4.1.4, if the frequency response of the negative resistance does not match the frequency response of the loss of the resonator, there is the potential

for instability. This is an issue when Q-enhancing single-pole resonators since the loss of the resonator has a low-pass response (in series with an inductor) and the negative resistance has a high pass response (in series with a capacitor). Therefore, to minimize the potential for instability, alternative negative resistance circuits, such as the common-gate inductive feedback circuit introduced in Chapter 3, should be explored such that the frequency response of the negative resistance can be designed to match the loss of the resonator.

6.3.4 Bias Tracker Circuit

In this work, the gate-source bias (V_{gs}) was set by an external source in order to adjust for changes in the threshold voltage (V_t) of the FETs. However, in practice, V_{gs} will not be set by an external source, but by some integrated bias circuit.

A common method of internally biasing a circuit is to self-bias the FET, where a resistor is placed at the source of the FET, biasing the source at the product of the drain current and the resistance. However, in self-biasing the FET, should the threshold voltage change (a common occurrence in many semiconductor processes) the bias point will shift, due to the change in drain current, settling at a new bias point that does not necessarily result in the same transconductance (g_m). Therefore, a bias circuit that can compensate for shifts in the threshold voltage is required.

In conclusion, the designs presented in this thesis offer the potential for monolithic low-loss filtering. The improvements discussed above could improve the potential of these filters to be included in GaAs integrated transceiver designs.

Appendix A

Chip Layouts

The layouts for the chips fabricated in this thesis were initially designed using the layout tool in Series IV. Upon submission of the preliminary layout, design schematic, and IFF file for LVS check, the final layouts were generated in Mentor Graphics by MA-COM personnel.

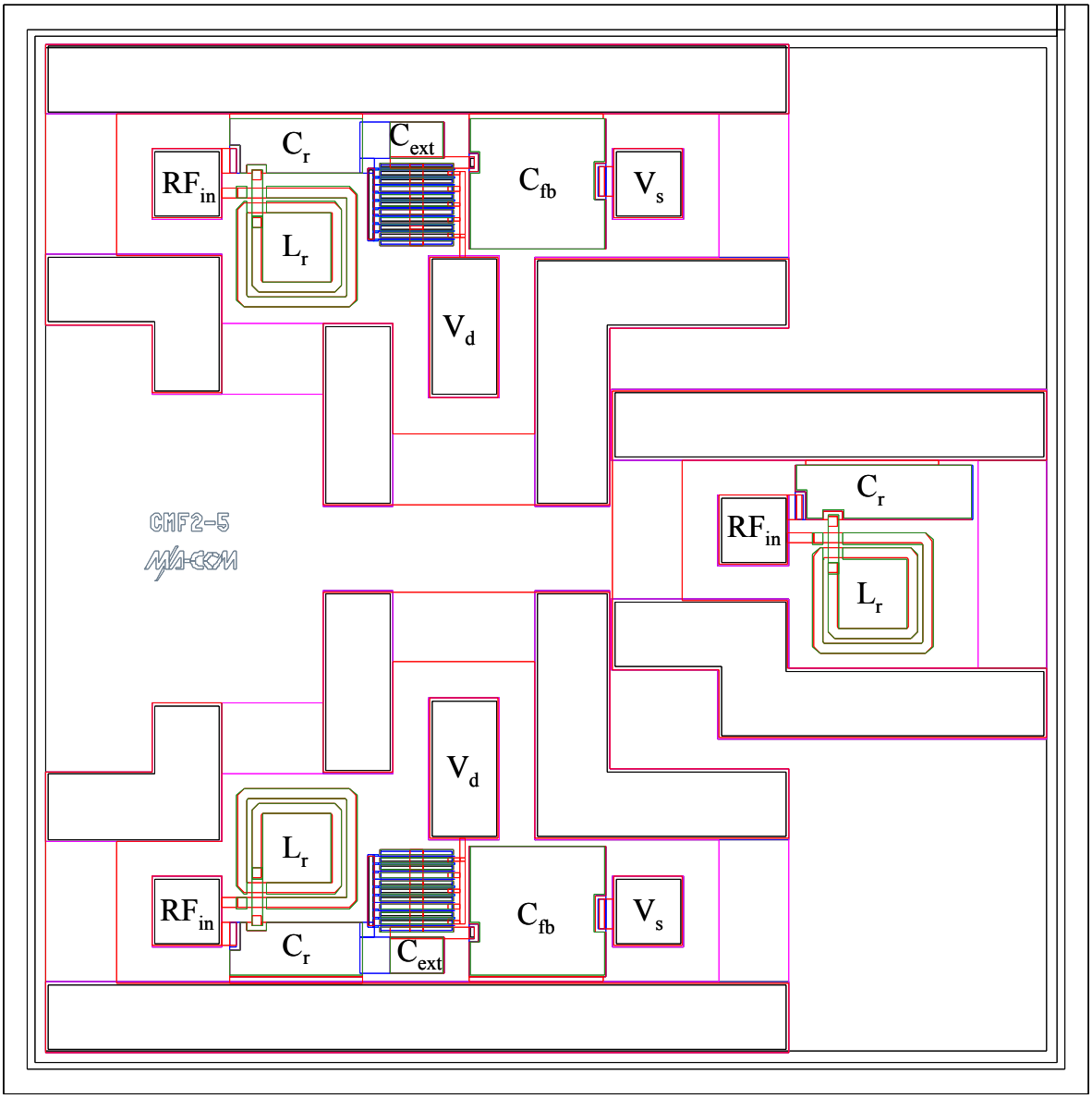


Figure A.1: CMF2-5: (Top) Q-Enhanced 1 nH LC resonator with 1 mm D-FET, (Bottom) Q-Enhanced 1 nH LC resonator with 1 mm E-FET, (Right) Passive 1 nH LC resonator.

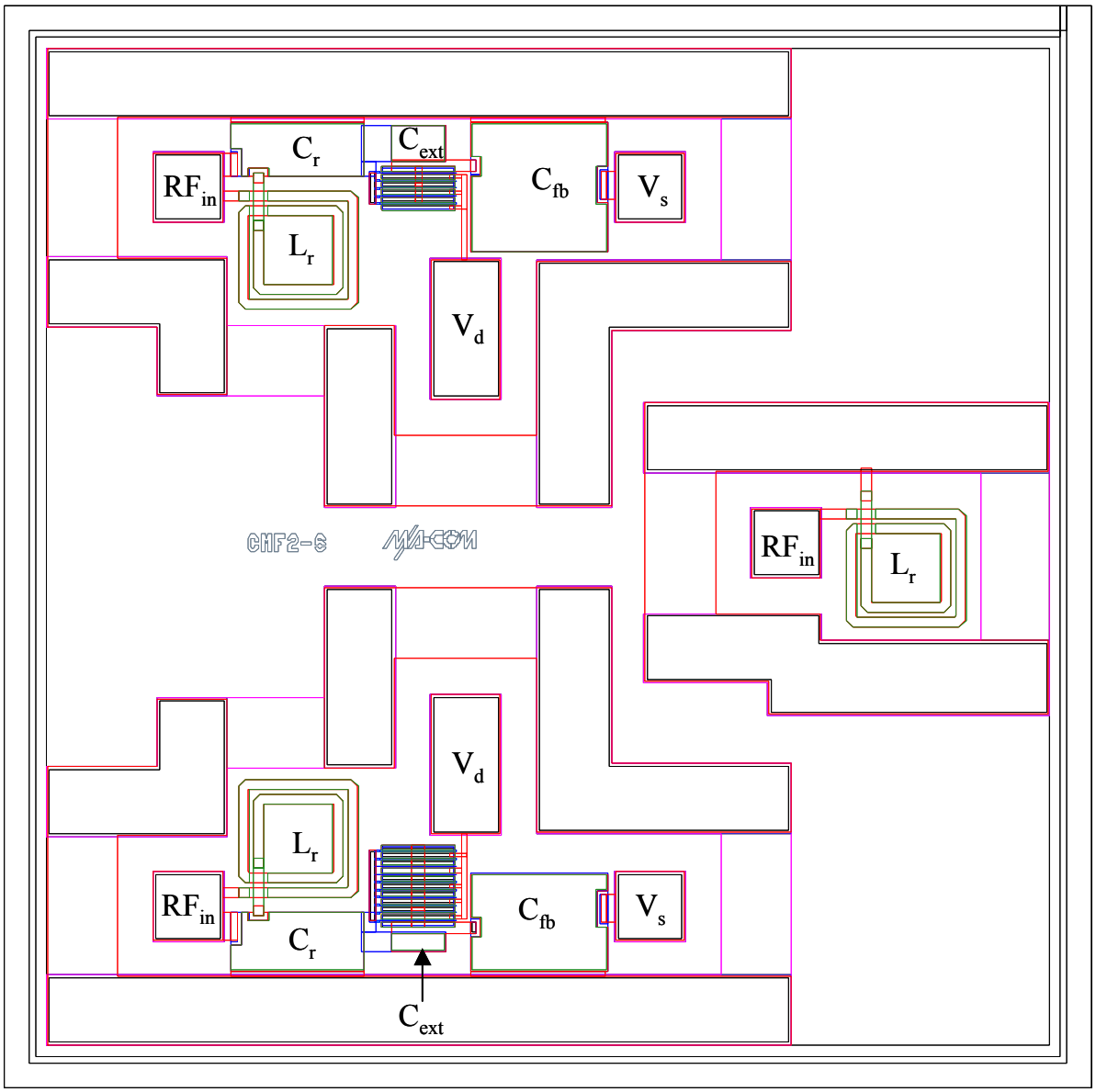


Figure A.2: CMF2-6: (Top) Q-Enhanced 1 nH LC resonator with 0.5 mm D-FET, (Bottom) Q-Enhanced 1 nH LC resonator with 1 mm D-FET and modified C_{ext} and C_{fb}, (Right) Passive 1 nH inductor breakout.

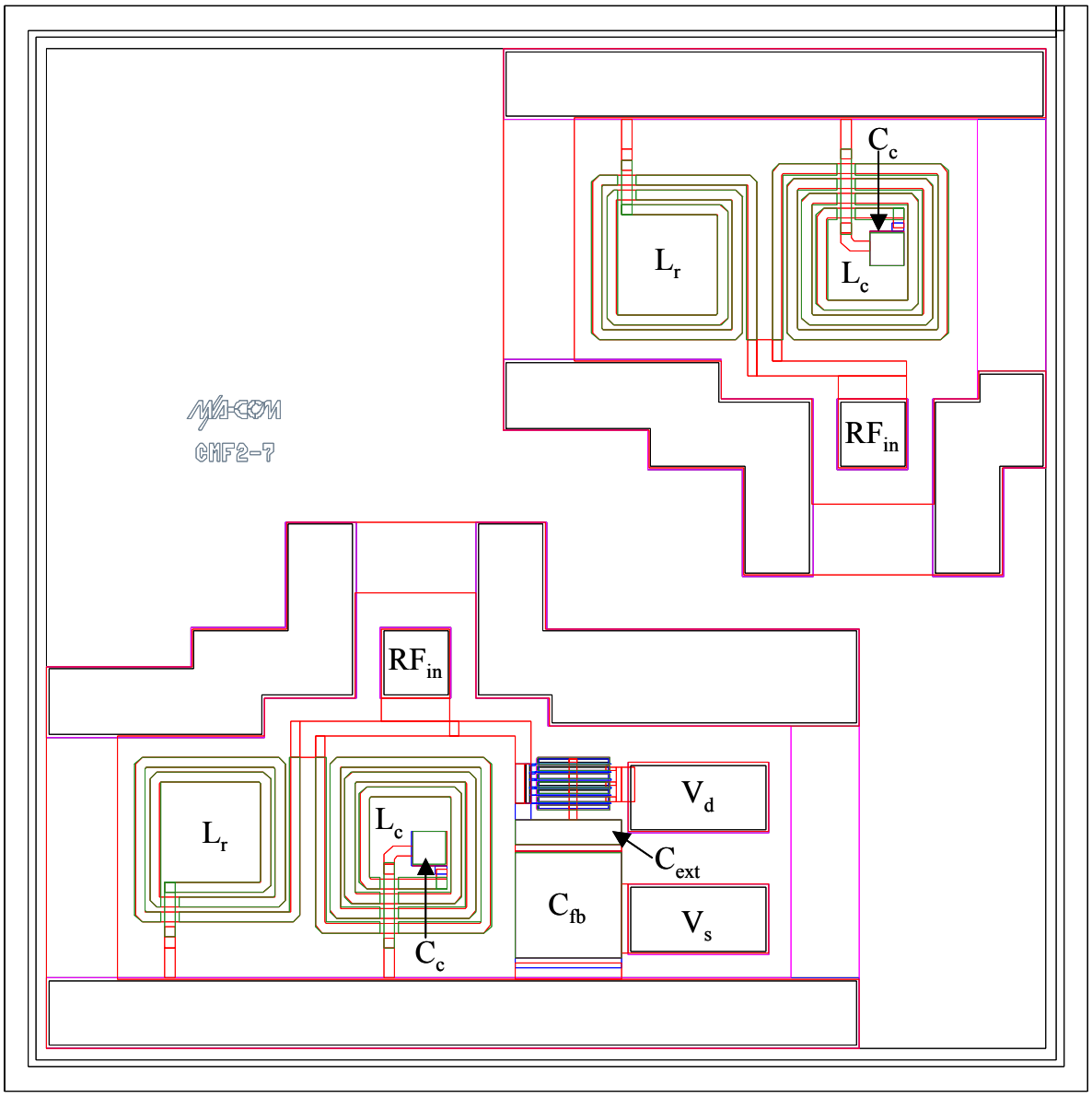


Figure A.3: CMF2-7: (Top) Passive 2 nH Pole-Zero resonator breakout, (Bottom) Q-Enhanced 2 nH Pole-Zero resonator with 0.6 mm D-FET.

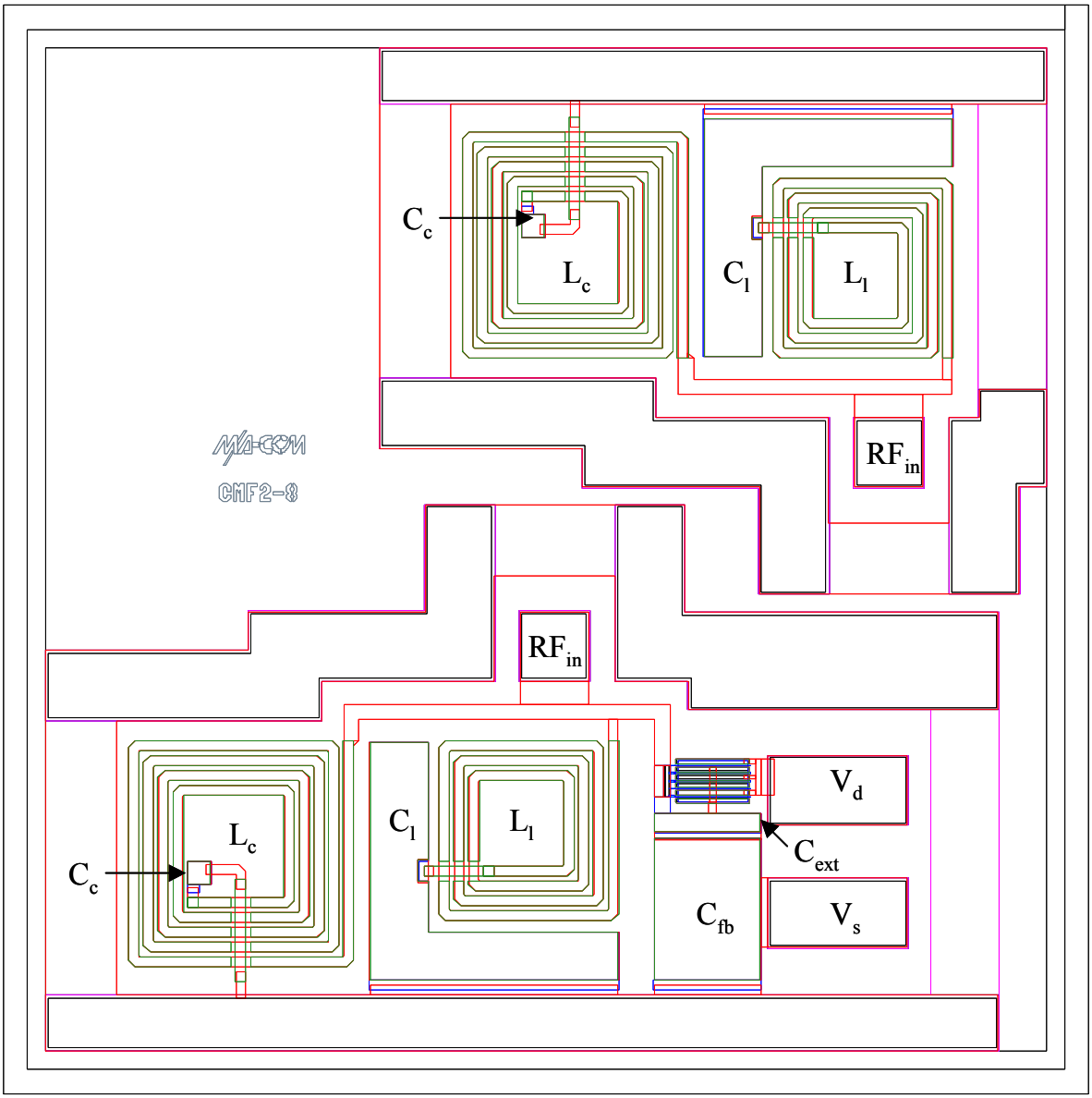


Figure A.4: CMF2-8: (Top) Passive 2 nH Zero-Pole-Zero resonator breakout, (Bottom) Q-Enhanced 2 nH Zero-Pole-Zero resonator with 0.5 mm E-FET.

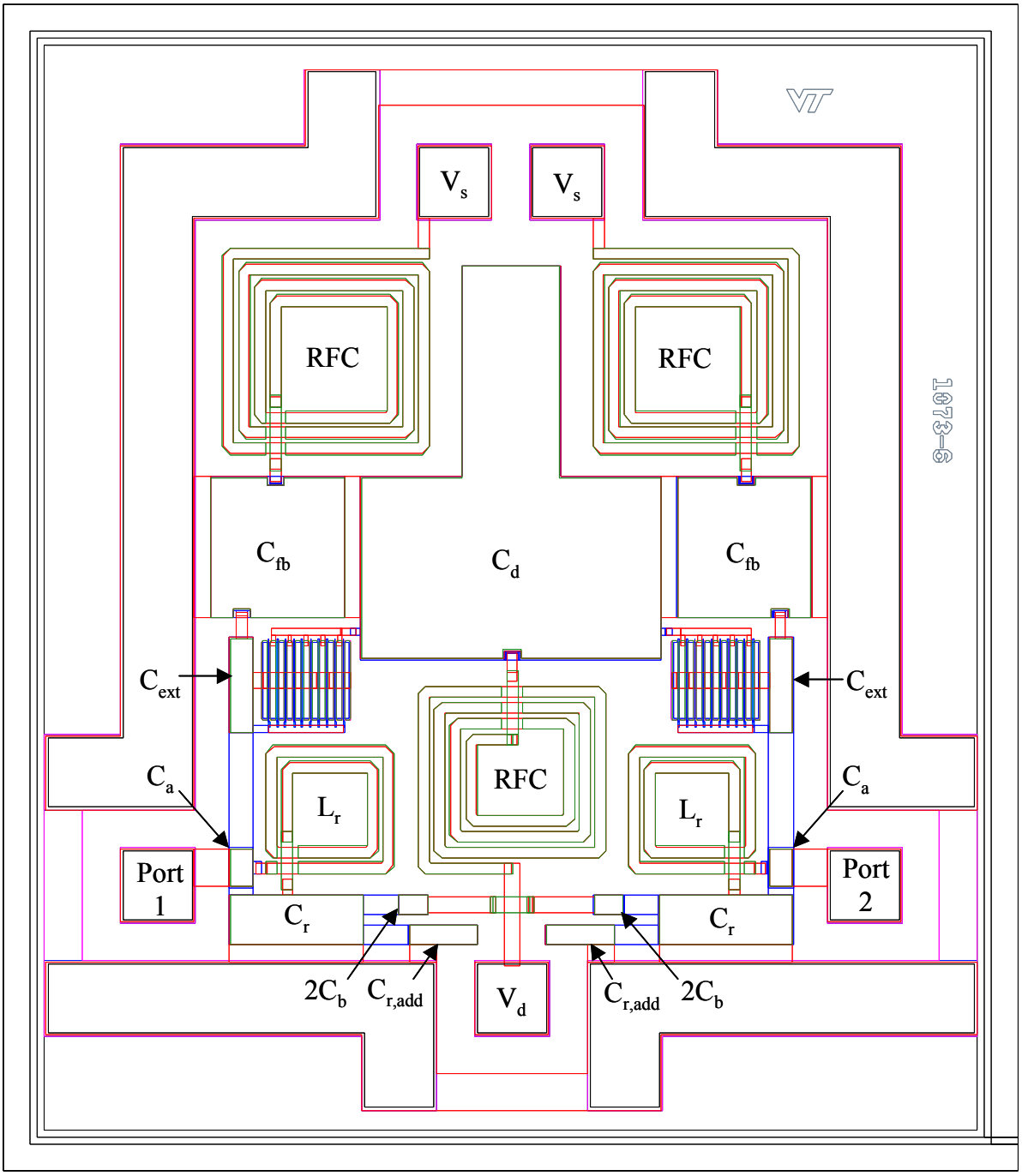


Figure A.5: 1073-6: 2^{nd} order Butterworth filter with 1 mm D-FET Q-Enhanced 1 nH LC resonators.

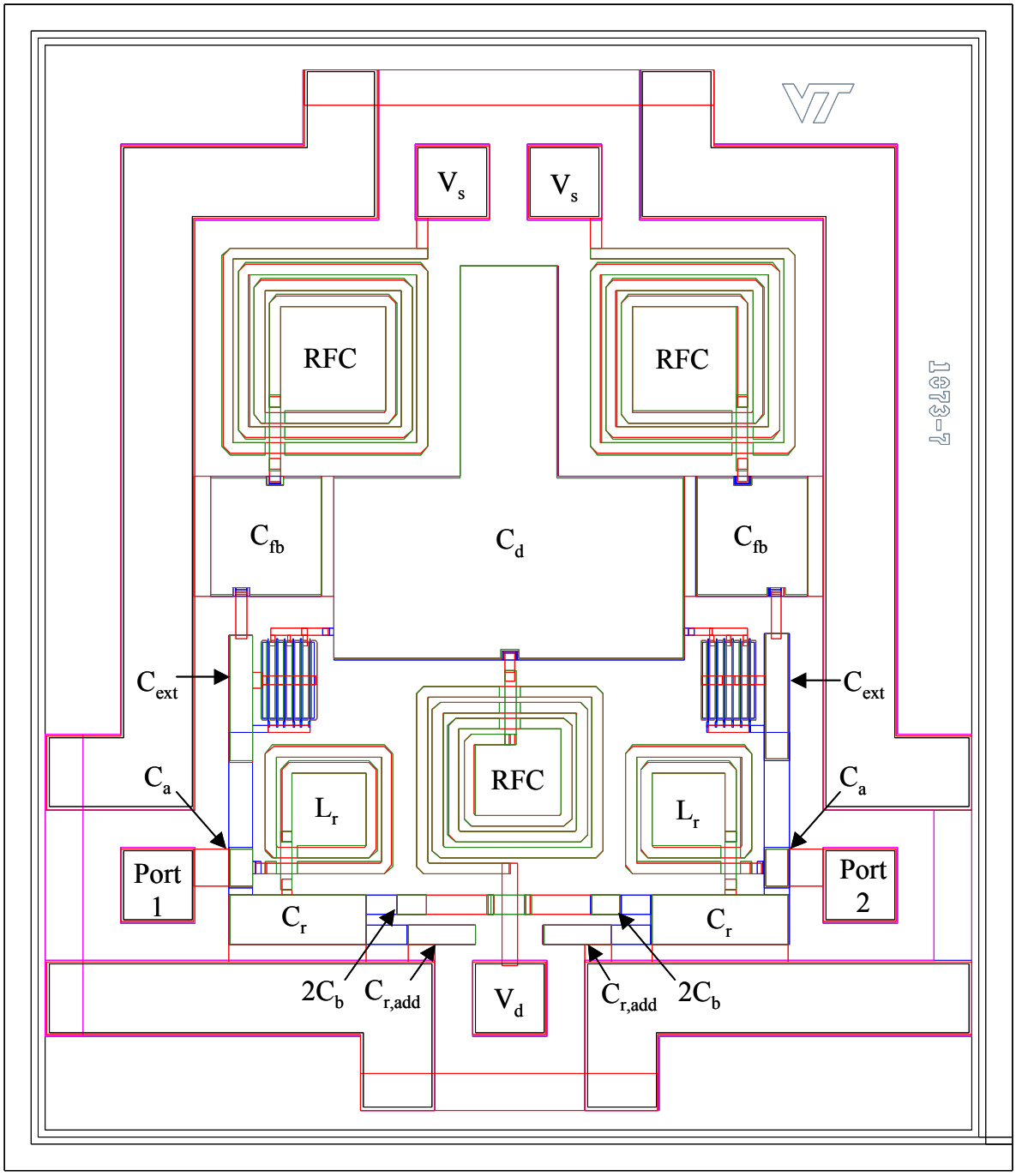


Figure A.6: 1073-7: 2^{nd} order Butterworth filter with 0.6 mm D-FET Q-Enhanced 1 nH LC resonators.

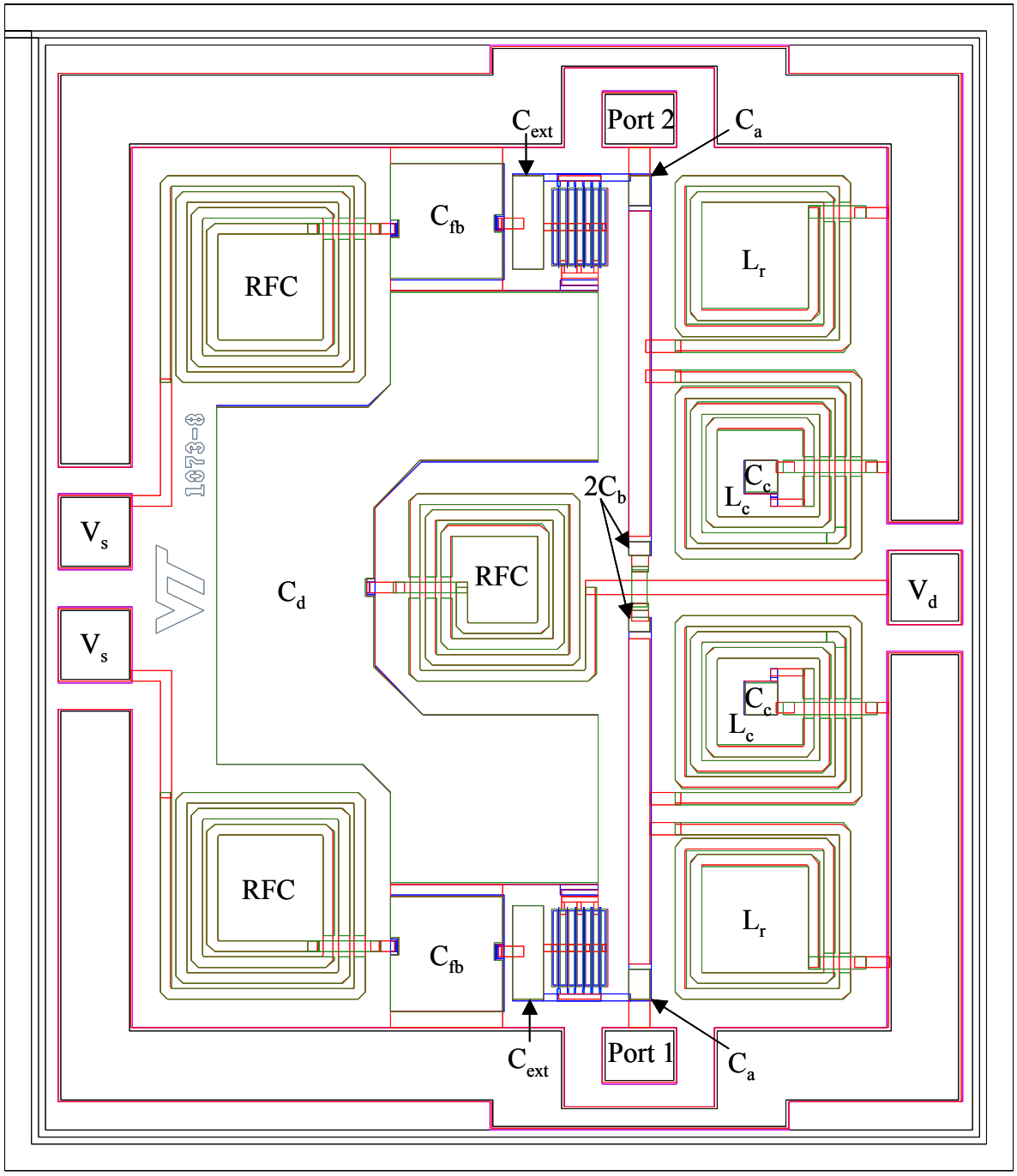


Figure A.7: 1073-8: 2^{nd} order Butterworth filter with 0.6 mm D-FET Q-Enhanced 2 nH Pole-Zero resonators.

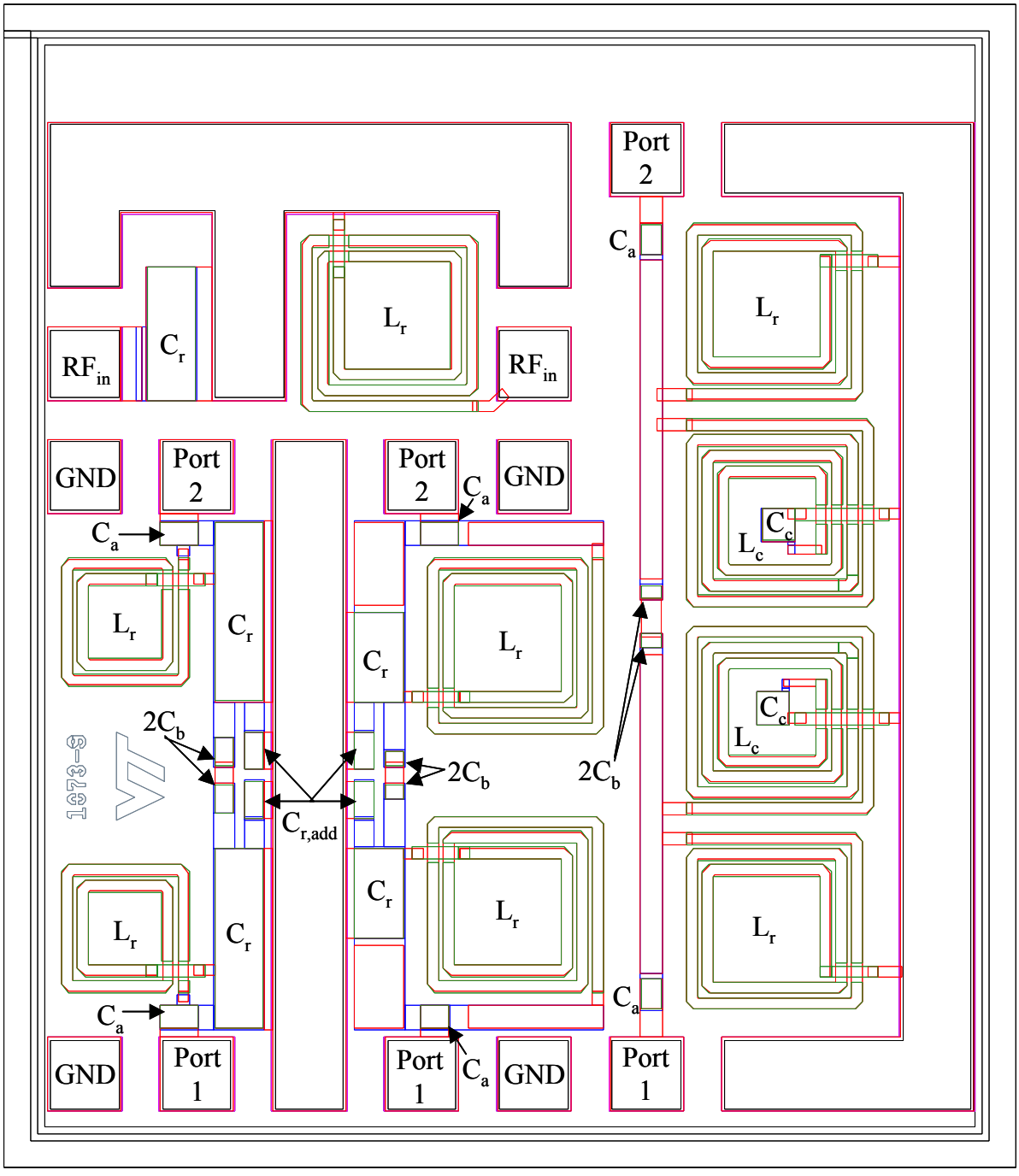


Figure A.8: 1073-9: (Top-Left) Passive 5.2 pF capacitor breakout, (Top-Center) Passive 2 nH inductor breakout, (Right) 2^{nd} order Butterworth filter with passive 2 nH Pole-Zero resonators, (Bottom-Center) 2^{nd} order Butterworth filter with passive 2 nH LC resonators, (Left) 2^{nd} order Butterworth filter with passive 1 nH LC resonators.

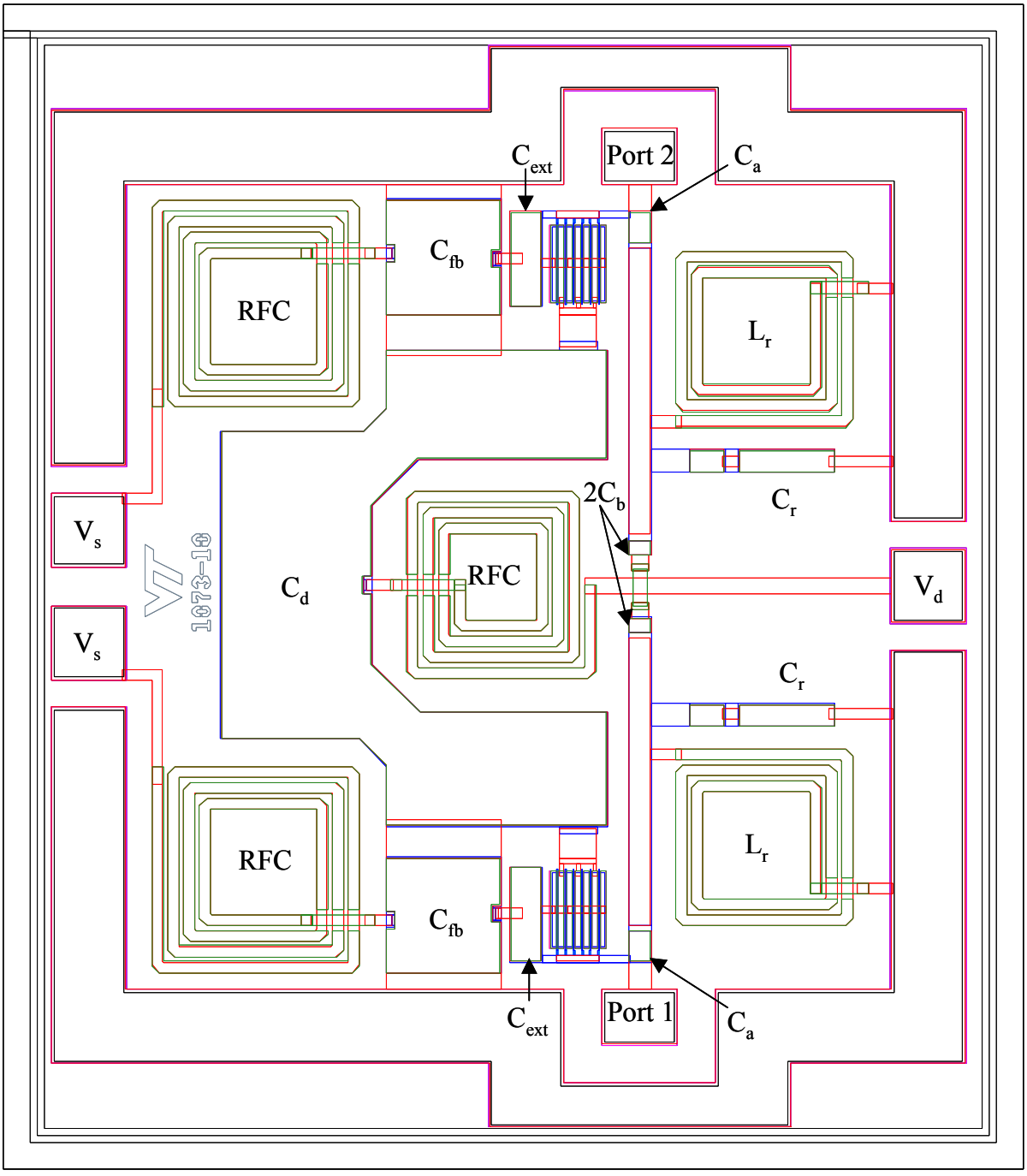


Figure A.9: 1073-10: 2^{nd} order Butterworth filter with 0.6 mm D-FET Q-Enhanced 2 nH LC resonators.

Appendix B

MDIF File Format

The MDIF S-parameter file format (shown below) is available in Series IV [5] for recording S-parameters as a function of variable instead of using many separate data files. The file can be imported into Series IV and the response can be tuned based on the variable choosen. For the purposes of the resonator and filter measurements, V_{sg} was the variable choosen to tune the bias of the negative resistance circuits. Furthermore, the voltage and current measurements were recorded.

```
!Source:   Vds=3.001781   Ids=0.0003   Vsg=0.502   Isg=0.0017
!Meter:      Ids=0.000746
VAR      Vsg=0.5
Begin      ACDATA
#      GHZ      S      DB      R      50
%F    N11X   N11Y   N21X   N21Y   N12X   N12Y   N22X   N22Y
1.00  -0.26  -23.08  -73.92  31.80  -75.55  31.80  -0.29  -23.33
1.02  -0.28  -23.19  -75.32  56.80  -74.75  56.80  -0.33  -23.36
....
2.98  -0.27  -55.61  -47.38  37.96  -47.87  38.85  -0.39  -56.01
3.00  -0.34  -55.61  -46.90  36.11  -47.38  40.45  -0.28  -56.02
End      ACDATA
```

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Vita

Edward Daniel McCloskey was born and raised in Penfield, NY. He graduated from Penfield High School in 1994. Daniel continued his education at Virginia Tech, studying Electrical Engineering. While attending Virginia Tech, Daniel interned at Grayson Wireless of Forest, Virginia as an RF Design Engineer, assisting in the design and verification of repeater and microcell systems. He recieved his Bachelor of Science degree in May of 1998.

Upon graduation, Daniel worked as an RF Design Engineer at M/A-COM in Lowell, Massachuetts. In this role, he designed high performance RF switches and attenuators and assisted in the development of multifunction chip sets for mobile phones. In August of 1999, Daniel returned to Virginia Tech to pursue a graduated degree in Electical Engineering.

Daniel will have completed the requirements for the Master of Science degree in Electrical Engineering in April 2001. Upon completion, he will join AeroAstro in Herndon, Virginia as an RF Design Engineer.