# Mixed As/Sb and tensile strained Ge/InGaAs heterostructures for low-power tunnel field effect transistors

Yan Zhu

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Mantu Hudait, Chair
Luke Lester
Masoud Agah
Majid Manteghi
Chenggang Tao

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## ABSTRACT

Reducing supply voltage is a promising way to address the power dissipation in nano-electronic circuits. However, the fundamental lower limit of subthreshold slope (SS) within metal-oxide-semiconductor field-effect transistors (MOSFETs) is a major obstacle to further scaling the operation voltage without degrading ON/OFF-ratio in today's integrated circuits. Tunnel field-effect transistors (TFETs) benefit from steep switching characteristics due to the quantum-mechanical tunneling injection of carriers from source to channel, rather than by conventional thermionic emission in MOSFETs. TFETs based on group III-V compound semiconductor and Ge heterostructures further improve the ON-state current and reduce SS due to the low bandgap energies and smaller carrier tunneling mass. The mixed arsenide/antimonide (As/Sb) $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ and $Ge/In_xGa_{1-x}As$ heterostructures allow a wide range of bandgap energies and various band alignments depending on the alloy compositions in the source and channel materials. Band alignments at source/channel heterointerface can be well modulated by carefully controlling the compositions of the $In_xGa_{1-x}As$ or $GaAs_ySb_{1-y}$. In particular, this research systematically investigate the development and optimization of low-power TFETs using mixed As/Sb and $Ge/In_xGa_{1-x}As$ based heterostructures including: basic working principles, design considerations, material growth, interface engineering, material characterization, band alignment determination, device fabrication, device performance investigation, and high-temperature reliability. A comprehensive study of TFETs using mixed As/Sb and $Ge/In_xGa_{1-x}As$ based heterostructures shows superior structural properties and distinguished device performances, both of which indicate the mixed As/Sb and $Ge/In_xGa_{1-x}As$ based TFET as a promising option for high performance, low standby power and energy efficient logic circuit application.

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# Chapter 1 Introduction

## 1.1 Limitations of metal-oxide-semiconductor field-effect-transistor scaling

The dimension of silicon (Si) metal-oxide-semiconductor field-effect-transistors (MOSFETs) has been scaled by 3 orders of magnitude in the past decades in order to achieve low-power, high-performance devices and integrated circuits. Extraordinary improvements have been achieved in switching speed, device density, functionality, and cost of microprocessors due to the downscaling of device geometry. However, further downscaling of conventional Si MOSFETs faces critical issues: the increasing difficulty in further reducing the supply voltage, and the increasing leakage current that degrades the switching current ratio between ON and OFF states ($I_{ON}/I_{OFF}$ ratio), both of which will result in high power consumption. As can be seen from Fig. 1.1 [1], which is a plot of active power density (blue line) and subthreshold power density (red line) from commercial Si MOSFETs, the leakage power starts to dominate in advanced transistor as scaling of gate length. The leakage power density will exceed the active power density if the gate length is below the cross-over point of these two lines as labeled in the figure. Besides, as the transistor gate length is reduced, supply voltage ($V_{DD}$) should be lowered to keep high device performance and reduce power dissipation. In order to meet the $I_{ON}$ requirement, the threshold voltage $V_{TH}$ needs to be scaled with $V_{DD}$. However, for Si MOSFETs, $I_{OFF}$ exponentially increases with $V_{TH}$ reduction and is given by [2],

$$I_{OFF} = I_{DS} \cdot 10^{-V_{TH}/SS} \tag{1.1}$$

where $I_{DS}$ is the drain to source current and SS is the subthreshold slope (also referred to as inverse subthreshold slope in literature) of the device which is the change of gate voltage, $V_{GS}$, that must be applied in order to create one decade increase in the output current or as defined as [3]

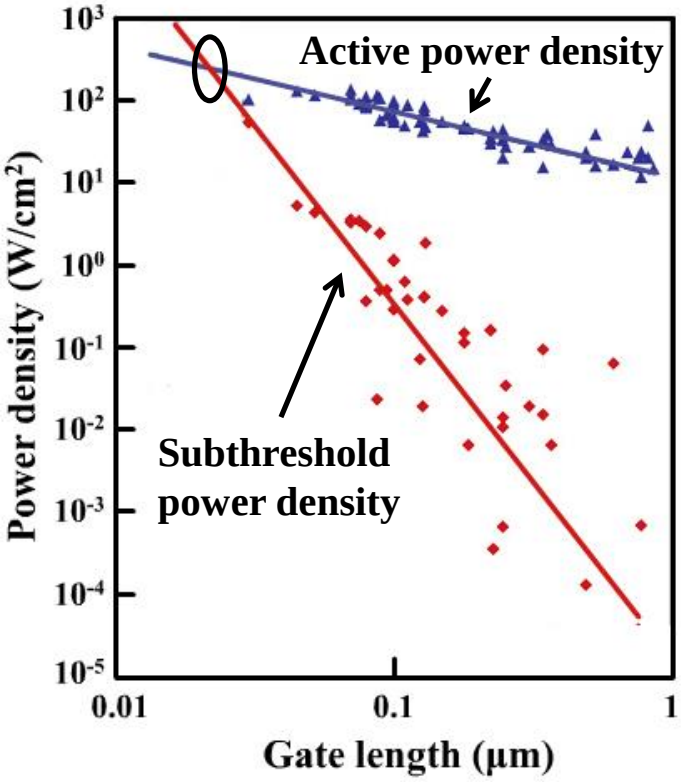


**Figure 1.1** Power density of the active region (blue line) and subthreshold region (red line) from commercial Si MOSFETs. The subthreshold power density is taking more and more proportion of the total power consumption with the scaling of gate length. The subthreshold leakage power density will be higher than the active power density if the gate length is below the cross point of these two lines as labeled in the figure. Used with permission of Nanotechnology Reviews.

$$SS = \frac{dV_{GS}}{d(logI_{DS})}[\mathrm{mV/dec}]. \tag{1.2}$$

For the conventional MOSFET, the subthreshold current is the diffusion current and SS is independent of $V_{GS}$ and is given by [4]

$$SS = \frac{kT}{q} ln10\left(1 + \frac{C_{DM}}{C_{OX}}\right) \tag{1.3}$$

where, kT/q is the thermal factor, $C_{DM}$ is the depletion capacitance, and $C_{OX}$ is the gate oxide capacitance. Equation 1.3 approaches a well-known lower limit of approximately 60mV/dec at T = 300K when $\frac{C_{DM}}{C_{OX}}$ is close to zero. But in practice, caused by the short-channel effects (SCEs),

SS is far worse than an ideal value of 60mV/dec [1, 5]. Typically, SS is about 70-90mV/dec for bulk MOSFETs. The change of transfer characteristics ($I_{DS}$ versus $V_{GS}$) of a MOSFET as the scaling of $V_{TH}$ is shown in Fig. 1.2 (black lines). It can be seen from this figure that MOSFET shows an exponential increase in $I_{OFF}$ due to the incompressible lower limit of SS. As demonstrated in Eq. 1.1, in order to lower $V_{TH}$ without the degradation (increasing $I_{OFF}$) of transistor performance, transistor with a steep SS, called steep-slope-switches (SSS, as shown in the green line in Fig. 1.2) are expected to reduce both ON-sate and OFF-state power consumption.

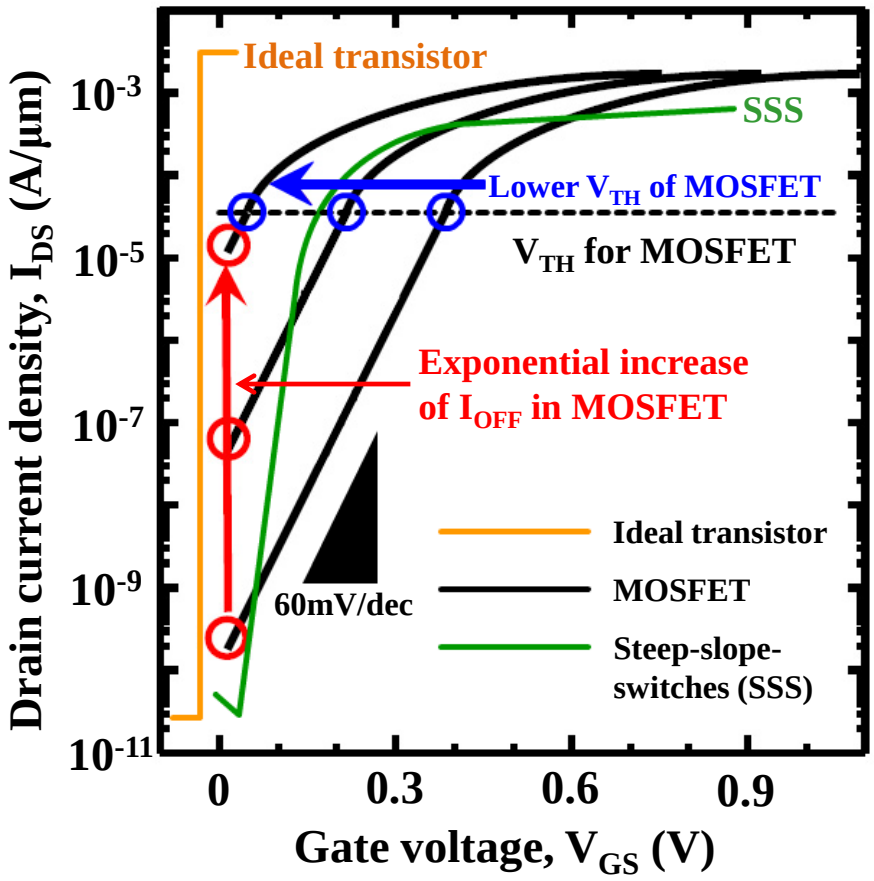


**Figure 1.2** Comparison of the transfer characteristics ($I_{DS}$ versus $V_{GS}$) of ideal transistor (orange line), MOSFET (black lines) and steep-slope-switches (SSS, green line). Due to the incompressible 60mV/dec SS at 300K for MOSFETs, $I_{OFF}$ of MOSFETs shows exponential increase with the scaling of $V_{TH}$. Used with permission of Nanotechnology Reviews.

Recently, tunnel field-effect-transistors (TFETs) [6-15] based on band-to-band tunneling (BTBT) injection mechanism have been proposed as one of SSS to replace MOSFET for low-power applications. TFETs have advantages over conventional MOSFETs in terms of lower $I_{OFF}$ and steeper SS [9-10, 16]. In order to design a TFET with high performances, proper material system needs to be selected. Among all material systems, III-V heterostructures can provide a smaller effective tunneling mass [5, 15, 17] and allow different band alignments between source/channel tunnel junction [5-15] for the enhancement of $I_{ON}$ and reduction of $I_{OFF}$. Among them, mixed As/Sb based heterostructures [9, 11-15] namely, $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ provide a wide range of bandgaps and band alignments depending on the alloy compositions in the source and channel materials [11-15]. As a result, the band offset of source/channel junction can be well modulated to guarantee high $I_{ON}$ without sacrificing $I_{OFF}$ by properly selecting the material compositions in the source and channel regions. Thus, the mixed As/Sb material system has been proposed as a promising candidate for high performance TFET application. On the other hand, the tensile strained $Ge/In_xGa_{1-x}As$ heterostructure also satisfies the requirements for low band gap material system in a TFET design. More importantly, by carefully controlling the alloy composition in $In_xGa_{1-x}As$ material, the magnitude of tensile strain inside the Ge layer can be tailored such that the band offset between the Ge source and the InGaAs channel can also be well-modulated, both of which will facilitate the further optimization of TFET structure. As a result, both the mixed As/Sb and tensile strained $Ge/In_xGa_{1-x}As$ heterostructures show great potential for low-power tunnel field effect transistor applications.

## 1.2 Fundamental operating principles of tunnel field effect transistor

### 1.2.1 Basic working principles

The TFET is a gated $p^+$-i-$n^+$ diode with a gate over the intrinsic region. The gated $p^+$-i-$n^+$ diode is always reverse biased to obtain ultra-low leakage current. A schematic cross section of an n-type TFET device with applied source ($V_S$), gate ($V_{GS}$) and drain ($V_{DS}$) voltages is shown in Fig. 1.3 (a) [4, 18]. For an n-type TFET, the heavily p-type doped region is called the source, the intrinsic region is called the channel and the heavily n-type doped region is called the drain. When a positive voltage is applied to the heavily n-type doped region, the $p^+$-i-$n^+$ diode is reverse-biased and ready to be switched by the gate. The schematic band diagrams of the TFET device at the OFF-state is shown by red lines in Fig. 1.3 (b) [4, 18]. As shown in the figure, under zero gate-source bias voltage ($V_{GS}$ = 0), the BTBT process is suppressed due to the gap between the source valence band maximum and the channel conduction minimum (and the resulting lack of available states with appropriate energy within the channel conduction band to accept tunneling electrons). When a TFET is on OFF state, only $p^+$-i-$n^+$ diode leakage current flows between the source and drain, and this current can be extremely low. In contrast, the band diagram of the n-type TFET on the ON-state is shown by green lines in Fig. 1.3 (b) [4, 18]. With positive $V_{GS}$, the energy bands of the intrinsic channel region are pushed down by $q\Delta V_{GS}$ as labeled in Fig. 1.3 (b) [4, 18]. With increasing $V_{GS}$, the channel conduction band minimum was pushed below the source valence band maximum. As a result, the tunneling barrier width (labeled as $\lambda$ in Fig. 1.3 (b) [4, 18]) between the p-type source and intrinsic channel is significantly reduced (less than 10nm). The reduced tunneling barrier enables significant amount of electrons tunnel from occupied states in source valence band to unoccupied states in the channel conduction band with the same energy alignment in an energy window of $\Delta\Phi$ as labeled in Fig. 1.3 (b) [4, 18, 16] and these tunneling electrons will finally be collected by the drain.

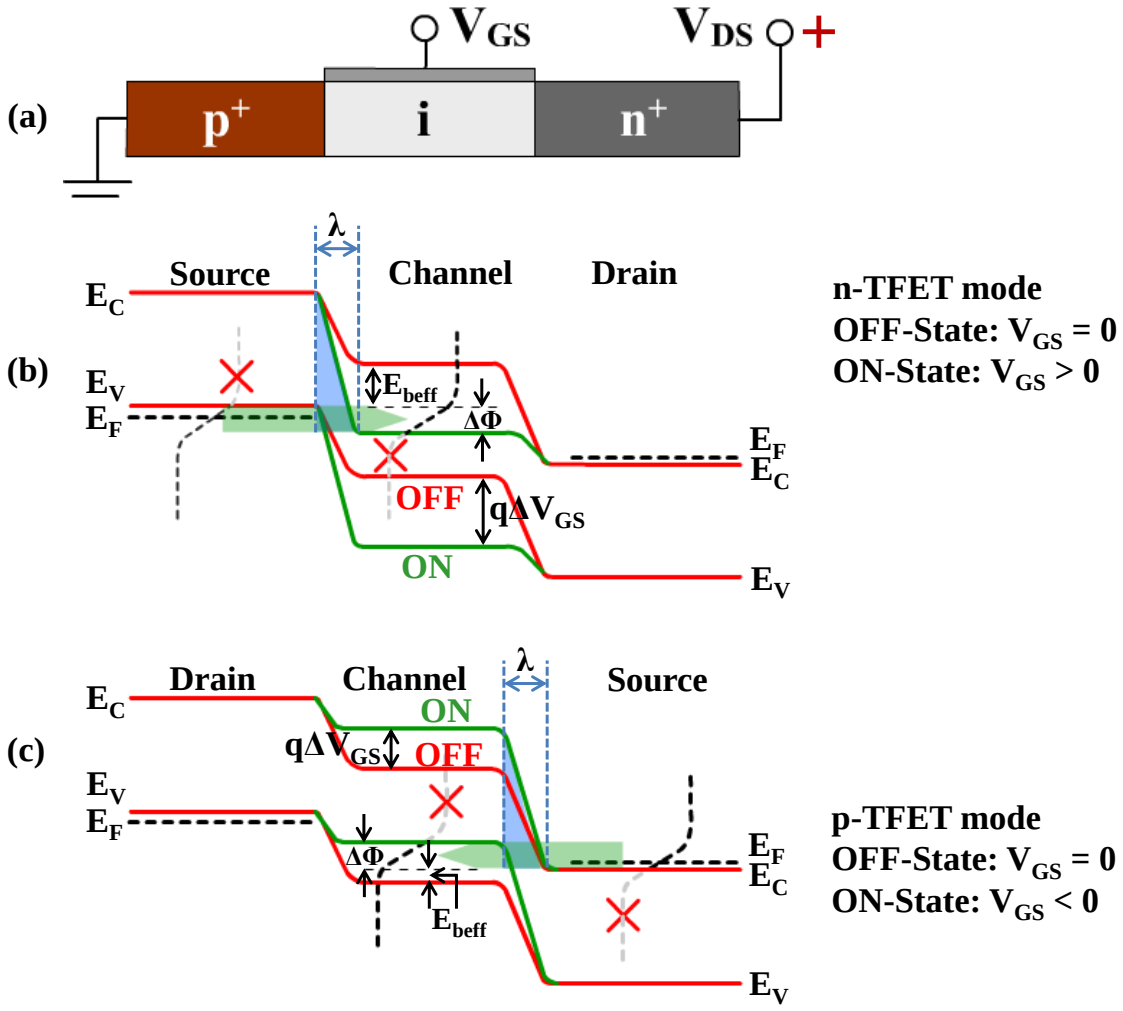


**Figure 1.3** (a) Schematic cross-section of a TFET structure with applied source ($V_S$), gate ($V_{GS}$) and drain ($V_{DS}$) voltages. (b) Schematic energy band diagram for the OFF-state (red lines with $V_{GS} = 0$ and $V_{DS} > 0$) and ON-states (green lines with $V_{GS} > 0$ and $V_{DS} > 0$) of n-type TFET. (c) Schematic energy band diagram for the OFF-state (red lines with $V_{GS} = 0$ and $V_{DS} > 0$) and ON-states (green lines with $V_{GS} < 0$ and $V_{DS} > 0$) of p-type TFET.

In principle, the TFET is an ambipolar device with symmetry between the n-type and p-type sides (similar doping levels, similar gate alignment, etc.), showing n-type behavior with dominant electron conduction and p-type behavior with dominant hole conduction. The band diagram of the same structure as shown in Fig. 1.3 (a) working as a p-type TFET is shown in Fig. 1.3 (c) [4, 18]. For a p-type TFET, the heavily n-type doped region is called the source, the intrinsic region is called the channel and the heavily p-type doped region is called the drain. As

shown in red lines in Fig. 1.3 (c) [4, 18], the OFF-state band diagram of a p-type TFET is the same as that for an n-type TFET. No conduction is taking place in the TFET without gate bias due to the valence band maximum of the intrinsic channel located below the conduction band minimum of the n-type source. The BTBT process is suppressed, leading to very small OFF-state leakage current which is dictated by the reverse-biased $p^+$-i-$n^+$ diode. By applying a negative gate voltage, the energy bands of the channel were pulled up as shown in green lines in Fig. 1.3 (c) [4, 18]. A conductive channel opens as soon as the channel valence band maximum is lifted above the source conduction band minimum since holes in the source conduction band can now tunnel into empty states of the channel valence band (or it can also be described as electrons in the channel valence band can tunnel into empty states of the source conduction band) [4]. The tunneling holes are finally collected by the p-type drain.

### 1.2.2 ON-state current

The $I_{ON}$ of a TFET depends on the tunneling probability of the BTBT process [18]. The tunneling barrier for TFET can be approximated by a triangular potential [4], as indicated in the blue shading in Fig. 1.3 (b) and 1.3 (c) [4, 18], and the tunneling probability can be calculated using WKB (Wentzel – Kramers - Brillouin) approximation [19, 20]

$$T_{WKB} \approx \exp\left[-2\int_0^w |k(x)|dx\right] \tag{1.4}$$

where $|k(x)|$ is the absolute value of the wave vector of the carrier inside the barrier. $x = 0$ and $x = w$ are the classical boundaries of triangular potential shown in Fig. 1.4 [19]. The wave vector inside a triangular barrier can be expressed from the E-k relationship [19]

$$\mathrm{k(x)} = \sqrt{\frac{2m^*}{\hbar^2}(V - E_C)} \tag{1.5}$$

where V is the potential energy. For tunneling consideration, the incoming electron has a potential energy equal to the bottom of the energy gap and the varying conduction-band edge $E_C$

can be expressed in terms of the electric field **E** as a function of x. Thus, the wave vector inside the triangular barrier is given by [19]

$$k(x) = \sqrt{\frac{2m^*}{\hbar^2}(-q\boldsymbol{E}x)}. \tag{1.6}$$

Substituting Eq. 1.6 into Eq. 1.4 yields [19],

$$T_{WKB} \approx \exp[-2\int_0^{x_2}\sqrt{\frac{2m^*}{\hbar^2}(-q\boldsymbol{E}x)}\,dx. \tag{1.7}$$

For a triangular barrier as shown in Fig. 1.4 [19] with a uniform electric field, $w = E_G/Eq$, so [19]

$$T_{WKB} \approx \exp(-\frac{4\sqrt{2m^*}E_G^{3/2}}{3q\hbar\boldsymbol{E}}). \tag{1.8}$$

Equation 1.8 is a general expression for BTBT transmission probability. This equation can be improved by making it more specific for TFETs. Now comparing Fig. 1.4 to the TFET band diagrams shown in Fig. 1.3 (b) and 1.3 (c) [4, 18], it can be found that the height of the triangular barrier is $\Delta\Phi + E_G$, and the tunneling barrier width is $\lambda$. Here, $\Delta\Phi$ is the energy window over which tunneling can take place. As a result, the electric field in Eq. 1.8 can be expressed as, $E = (\Delta\Phi + E_G)/\lambda$. Equation 8 can be rewired as,

$$T_{WKB} \approx \exp(-\frac{4\lambda\sqrt{2m^*}E_G^{3/2}}{3q\hbar(\Delta\Phi + E_G)}) . \tag{1.9}$$

Here, m* is the effective mass and $E_G$ is the bandgap. Based on the triangular barrier approximation discussed above, $\Delta\Phi + E_G$ is the triangular barrier height for carriers to tunnel from source to channel. As shown in Fig. 1.3 (b), for an n-type TFET, the triangular barrier was denoted as blue shading and $E_G$ corresponds to the band gap energy of source material. The triangular barrier for a p-type TFET is also shown as blue shading in Fig. 1.3 (c). Different as the case with n-type TFET, $E_G$ corresponds to the band gap energy of channel material for a p-type

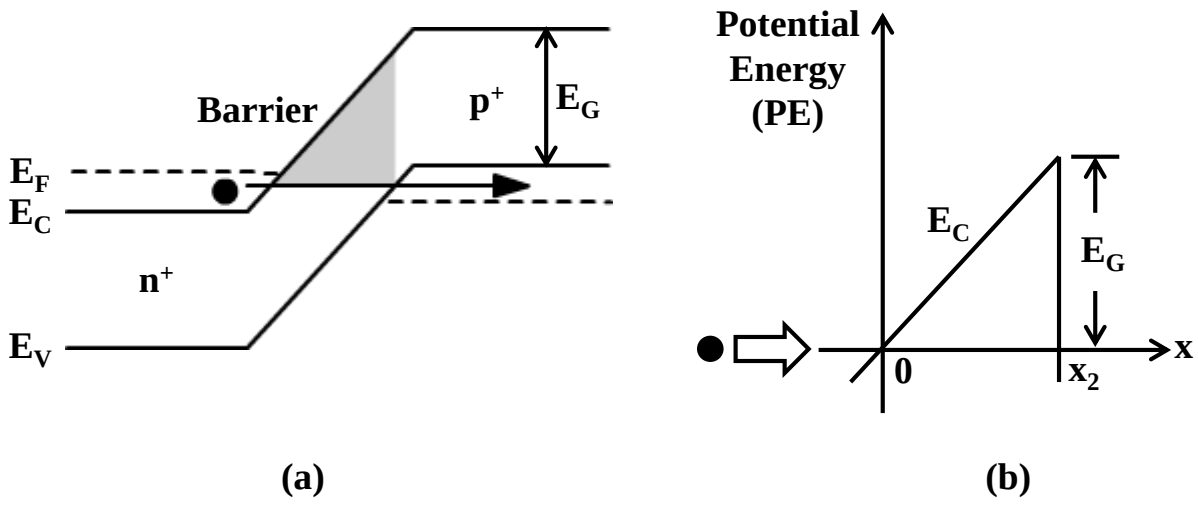


**Figure 1.4** (a) Band diagram of tunneling carrier from source to channel over a triangular potential. (b) Band to band tunneling can be calculated by approximating the tunneling barrier as a triangular potential, where carriers should tunnel through the base of the triangle. Used with permission of Nanotechnology Reviews.

TFET [4, 18]. There are four important requirements in order for BTBT to take place: available states in the source to tunnel from, available state in the channel to tunnel into, a tunneling barrier width that is narrow enough for tunneling through and the conservation of momentum [21]. For indirect semiconductor materials such as Si, crystal phonons are necessary to conserve momentum in order to assist the tunneling process. In that case, $E_G$ in the numerator of Eq. 1.9 should be replaced by $E_G$-$E_P$, where $E_P$ is the phonon energy [21] and the effective mass m* should be changed to $m_{rx}$*, which is the reduced effective mass in the tunneling direction. If these changes are not made in Eq. 1.9, the BTBT current will be overestimated for indirect materials. A higher BTBT current can be expected if m* and λ can be make as small as possible. In principle, a reduction of $E_G$ can also increase the tunneling probability. However, a small energy bandgap will lead to an increase of $I_{OFF}$ due to the thermal emission gets more pronounced [18] and as a result, a proper $E_G$ should be selected to meet a desired $I_{ON}/I_{OFF}$ ratio.

### 1.2.3 OFF-state leakage

For an ideal TFET at OFF state, the leakage current is only the $p^+$-i-$n^+$ leakage current flows between the source and the drain. This leakage current can be extremely low and less than a fA/μm as indicated by simulation [21]. However, in practice, there are five primary leakage mechanisms contributing to the OFF-state leakage of TFET [22]: (1) gate leakage through the high-κ gate dielectric; (2) thermionic emission over the source-drain built-in potential (the $p^+$-i-$n^+$ diode leakage current as we mentioned above); (3) Shockley-Read-Hall generation-recombination (SRH G-R) in the heavily doped source and drain depletion regions; (4) direct tunneling and defect-assisted tunneling process; and (5) ambipolar conduction. As the first two are well known, the other three mechanisms were explained below.

The SRH G-R mechanism is illustrated in Fig. 1.5 (a) [22]. The SRH G-R current is a common leakage current component especially in III-V material based TFETs due to the low band gap energy of these materials [9-11, 15, 23-24]. The most obvious feature of the SRH G-R dominated $I_{OFF}$ is its strong temperature dependence [11, 23-24]. The main contribution to the temperature dependence of the SRH G-R mechanism arises from the intrinsic carrier concentration $n_i$ which is proportional to exp ($-E_G/2kT$), where $E_G$ is the bandgap energy, k is the Boltzmann constant, and T is the temperature [23]. TFETs with a SRH G-R dominated leakage current usually shows an activation energy ($E_A$) about half of $E_G$ [23-24]. As the SRH G-R current increases exponentially with temperature, the SRH G-R dominated leakage will deteriorate the performance of TFET devices at high temperature. Experimental results showed that the SRH G-R current increased by 3 orders from 25°C to 150°C in an $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ n-type TFET [24], which in turn reduced the $I_{ON}/I_{OFF}$ ratio by several orders of magnitude.

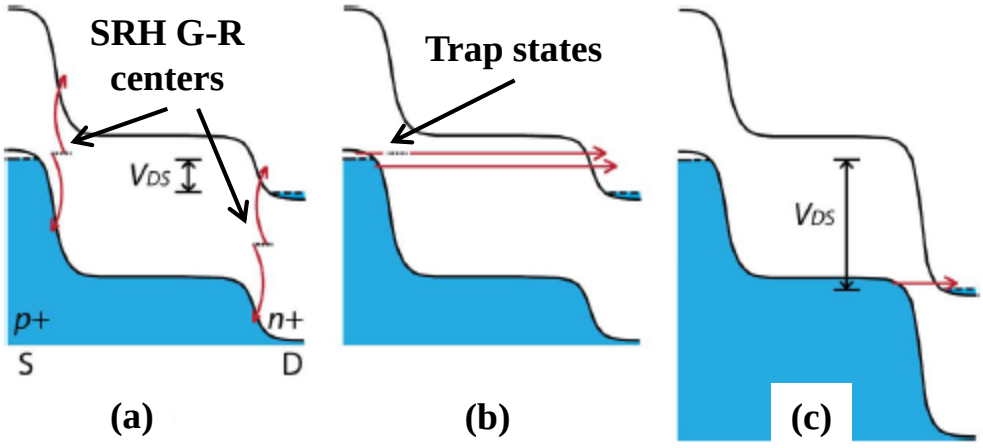


**Figure 1.5** Energy band diagrams showing the leakage mechanisms of n-type TFET at OFF-state: (a) Shockley-Read-Hall generation in the source (S) and drain (D) regions; (b) direct and defect-assisted tunneling from source to drain; and (c) ambipolar transportation with hole injection from drain to channel. [22] Used with permission of Nanotechnology Reviews.

Another leakage mechanism for a TFET is the tunneling leakage current, including both direct BTBT and the defect-assisted tunneling. With the scaling of gate lengths, direct BTBT as well as defect-assisted tunneling become dominate especially for narrow bandgap channel such as InAs [25] and for graphene nanoribbon [26]. Figure 1.5 (b) [22] shows the band diagrams of this leakage mechanism. It should be noted that the direct BTBT mechanism will dominate the OFF-state transport of some heterostructure TFETs even with a high gate length [11, 13]. High defect density at the source/channel heterointerface will introduce fixed positive charges, which will change the band alignment at the interface of source/channel and assist the band lineup transition from a staggered gap to broken gap. Thus, this broken gap band alignment caused by high defect density will enable the BTBT transport even at OFF state [11, 13]. This defect assisted band alignment transition will be discussed more in detail in ***Chapter 5.5***.

Besides, the ambipolar current as illustrated in Fig. 1.5 (c) [22] can also contribute to the OFF-state leakage of a TFET device. As discussed in ***Chapter 1.2.1***, the TFET is an ambipolar

device if the n-type and p-type regions are symmetric. If a negative bias is applied to the gate of an n-type TFET, the energy bands of the channel will be lifted up. If the negative gate bias is large enough to pull the channel valence band maximum above the drain conduction band minimum as shown in Fig. 1.5 (c) [22], reverse tunneling at the drain can inject minority carriers into the channel that leads to an ambipolar leakage. Ways to suppress this ambipolar leakage of TFETs will be discussed in detail in ***Chapter 1.2.5***.

### 1.2.4 Subthreshold slope

The SS of a TFET without a lower limit is one of the key advantages over traditional MOSFET. As can be seen from Fig. 1.3 (b) and 1.3 (c), due to the bandgap of source material, the low energy tail of Fermi distribution is cut-off in the source side. The channel also cuts-off the high energy part of the Fermi distribution such that the tunnel junction acts as a band-pass filter allowing only carriers in the energy window $\Delta\Phi$ can tunnel into the channel [18]. Thus, the electronic system is effectively "cooled down", behaving as a conventional MOSFET at a lower temperature. This filtering function makes it possible to achieve an SS lower than 60mV/dec at 300K [4].

To derive an expression of the SS for a BTBT device, the expression for the tunneling current through a reverse-biased p-n junction can be used [19, 21, 27],

$$\mathrm{I} = \mathrm{a}V_{eff}\boldsymbol{E}exp(-\frac{b}{\boldsymbol{E}}) \tag{1.10}$$

where $V_{eff}$ is the tunnel junction bias as shown in the inset of Fig. 1.6 (a) [27], **E** is the electric field, and a and b are coefficients determined by the material properties of the junction and the cross-sectional area of the device [22, 27]. Specifically,

$$\mathrm{a} = \mathrm{A}q^3\sqrt{2m^*/E_G}\Big/4\pi^2\hbar^2 \tag{1.11}$$

and

$$b = {4\sqrt{m^*}E_G^{2/3}}\Big/{3q\hbar^2}\cdot \tag{1.12}$$

Using the definition of SS from Eq. 1.2, the SS of a TFET can be described as,

$$SS = \ln 10\left[\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{GS}} + \frac{\boldsymbol{E}+b}{\boldsymbol{E^2}}\frac{dE}{dV_{GS}}\right]^{-1}. \tag{1.13}$$

From Eq. 1.13, it can be found that there are two terms involved to determine the SS of a TFET device and these terms are not limited to kT/q [22, 27]. The first term reflects the control of gate bias ($V_{GS}$) to the tunnel junction bias ($V_{eff}$). As a result, the transistor should be engineered so that the $V_{GS}$ can directly and efficiently control $V_{eff}$, which suggests that a transistor with a thin geometry and/or high-κ gate dielectric is desired to make sure that the gate bias can directly modulate the channel [27]. For an equivalent oxide thickness (EOT) approaching 1nm, $\frac{dV_{eff}}{dV_{GS}} \approx 1$ and the first term of Eq. 1.13 is approximately inversely related to $V_{GS}$. As a result, the SS of TFET increases with $V_{GS}$, which is a main difference of TFET from MOSFET and this changing trend is illustrated in Fig. 1.6 (a) [21] with different gate dielectrics. Therefore, if the transfer characteristics ($I_{DS}$-$V_{GS}$) of a TFET is plotted with $I_{DS}$ in a log scale, the subthreshold region of TFET does not appear as a straight line as that of MOSFET [21]. This difference is clearly shown in Fig 1.6 (b) [30] by comparing the transfer characteristics of a typical MOSFET and a typical TFET. The SS of TFET is smallest at the lowest $V_{GS}$, and increasing with $V_{GS}$. These characteristics of TFET have been observed both in experiments [6] and simulations [28, 29]. On the other hand, the SS can be minimized by maximizing the second term of Eq. 1.13. This occurs if the gate is placed in a proper direction to align the applied gate electric field with the internal electric field of the tunnel junction. In this way, the gate electric

field adds to the internal electric field and thus the tunneling probability was enhanced in a TFET device [22].

Due to the strongly dependence of SS on $V_{GS}$, it is useful to define two different types of SS, point SS ($SS_{pt}$) and average SS ($SS_{avg}$) (the latter one is more important for switching properties) [2]. The inset of Fig. 6 (b) [2, 21] shows these two SS. Point SS is the smallest value of the SS on the $I_{DS}$-$V_{GS}$ curve, typically found just as the device leaves its OFF-state and tunneling current starts to flow. Average SS is taken from the point where the device starts to be turned ON, up to $V_{TH}$ [21], [22], [31] and the average SS can be expressed as,

$$SS_{avg} = \frac{V_{TH} - V_{OFF}}{\log(I_{TH}/I_{OFF})}. \quad (14)$$

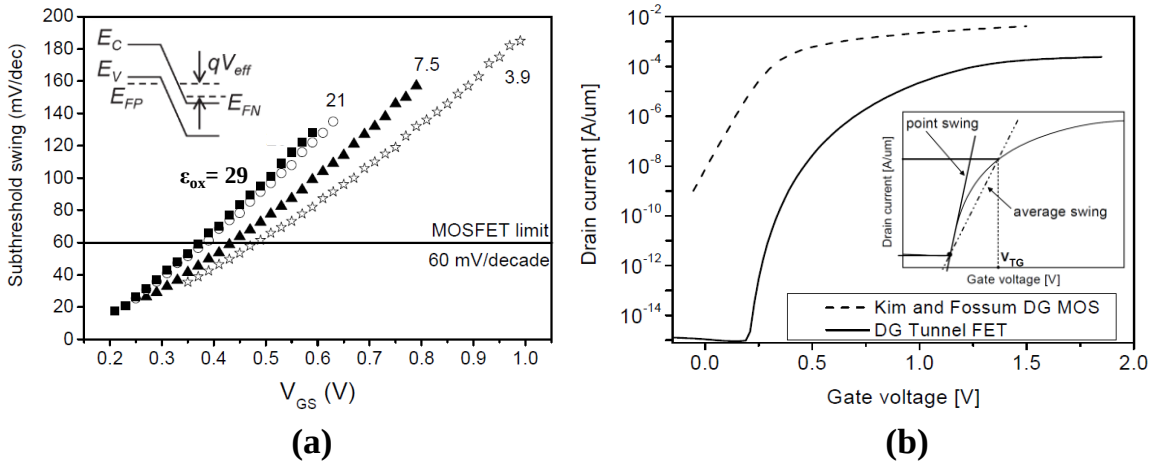


**Figure 1.6** (a) Dependence of the TFET subthreshold slope on gate voltage for different gate oxide with different dielectric constants, from numerical simulation. Each curve goes up to the threshold voltage of that device. The points were generated by taking the slope value ($dV_{GS}/d(\log I_{DS})$) at each point on the $I_{DS}$-$V_{GS}$ curves. [21] The inset shows the $p^+$-$n^+$ tunnel-junction energy band diagram under a tunnel junction bias $V_{eff}$. [27] (b) Qualitative comparison of the transfer characteristics ($I_{DS}$-$V_{GS}$) of a MOSFET [30] and a TFET showing a non-constant subthreshold swing for the TFET. The SS of TFET is smallest at the lowest $V_{GS}$, and rising with increasing $V_{GS}$. [21] The inset shows the definitions of point SS, taken at the steepest point of the $I_{DS}$-$V_{GS}$ curve, and average SS, taken as the average from turn-on to threshold voltage. [2, 21] Used with permission of Nanotechnology Reviews.

### 1.2.5 Approaches to reduce ambipolar behavior

As discussed in ***Chapter 1.2.1***, the TFET is an ambipolar device if the $n^+$ region and the $p^+$ region are symmetric in geometry and doping concentration, which shows n-type tunneling properties with positive gate bias but shows p-type tunneling properties with negative gate bias. As a result, the ambipolar properties result in similar transfer characteristics with positive and negative gate biases, as shown in Fig. 1.7 [32], leading to parasitic conduction at OFF-state. Therefore, different methods should be used to reduce the ambipolar behavior of a TFET device.

For an n-type TFET, device is turned on by applying positive gate bias, which creates an $n^+$ inversion layer underneath the gate. With increasing gate voltage, electron concentration in the

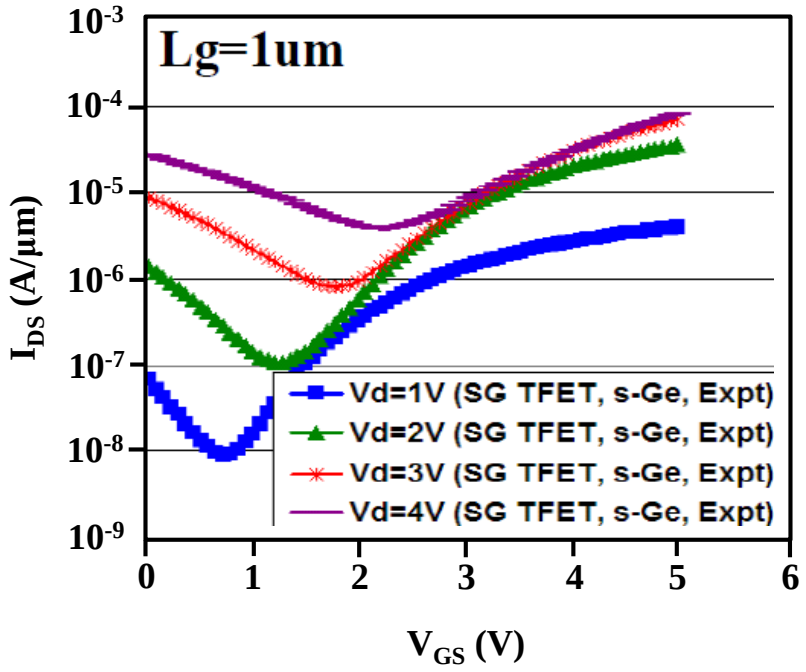


**Figure 1.7** TFETs with symmetric doping and geometry architecture exhibit ambipolar characteristics and show high OFF-state current with negative gate bias. [32] Used with permission of Nanotechnology Reviews.

$n^+$ inversion layer increases, thereby decreasing the $p^+$-$n^+$ tunneling barrier width (λ) at the source side. The reduction of this tunneling barrier width directly results in an increase of $I_{ON}$ as long as the dominant resistance between the source and drain is formed by this tunneling barrier, which means that the channel resistance is only a small fraction of the tunneling barrier

resistance. Furthermore, the tunneling barrier width is determined by the carrier concentration in the $n^+$ layer close to the source region. As a result, it is possible to create a high resistance region

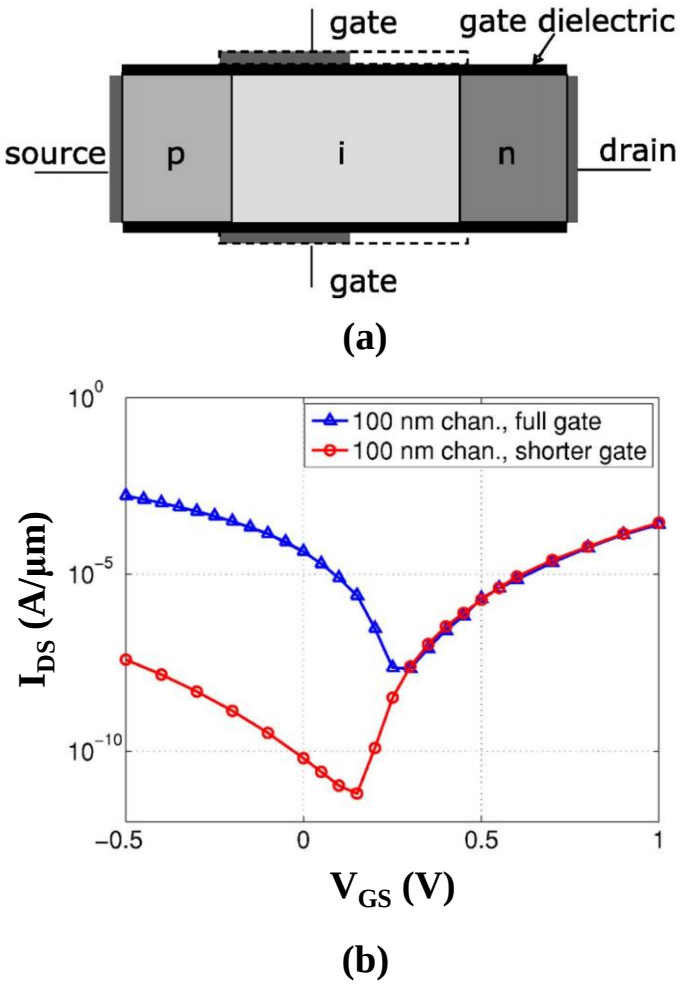


**Figure 1.8** (a) N-type TFET ($p^+$ source, intrinsic channel and $n^+$ drain) with different gate alignment: the dashed line shows the conventional gate structure with a full gate, the filled box represents a shorted gate. (b) Simulated transfer characteristics of TFETs with different gate alignment. Source and drain have the same doping concentration: $10^{20}/cm^3$; channel doping: p-type, $10^{15}/cm^3$. For the full gate (blue) device: source-drain overlap is 5nm. For the shorted gate (red) device: source-drain separation is 15nm. Reduction of the source-drain overlap with 20nm reduces the ambipolar current with three to five orders of magnitude. With permission of Nanotechnology Reviews.

in the channel near the drain without affecting $I_{ON}$ of the TFET [33]. This high resistance region near the drain can effectively block the ambipolar tunneling if a negative gate bias is applied. Based on this consideration, TFET devices without gate-drain overlap were proposed to reduce

the ambipolar behavior [33]. The schematic cross-section of this TFET device is shown in Fig. 1.8 (a) [33] and the simulated transfer characteristics of TFET devices with and without gate-drain overlap are compared in Fig. 1.8 (b) [33]. It can be seen from Fig. 1.8 (b) that with similar doping levels in source and drain, the TFET with gate-drain overlap is ambipolar, whereas the $I_{OFF}$ of the TFET without gate-drain overlap remains low, which is due to the high resistance region in the channel near the drain. In the TFET without gate-drain overlap, the large carrier density buildup by negative gate bias in the gated channel region no longer extends to the drain, leaving an area with low hole concentration adjacent to the drain/channel junction. In addition, due to the reduced inversion carrier concentration near the drain, the build-in electrical field at drain/channel junction was reduced. As a result, tunneling of holes from drain to the channel at the drain/channel junction with a negative gate bias is reduced and the OFF-state condition of the device can be properly controlled [33]. Similar approaches are also achieved by other researchers to reduce the ambipolar properties [32, 34], all of which illustrated significant reduction of ambipolar current using this method.

Another approach of reducing ambipolar current of a TFET is to lower the doping concentration of the drain region, which can increase the tunneling barrier width for holes at the channel/drain interface due to the enlarged tunneling barrier width at a lower doping concentration [34]. For n-type TFET, the p-type tunneling between channel and drain is significantly suppressed, since tunneling current decreases exponentially with increasing tunneling barrier width. In contrast, the $I_{ON}$ is controlled by the electron BTBT from source to channel, so it is insensitive to the drain doping concentration. As a result, asymmetric source-drain doping offers a successful scheme for suppressing the ambipolar characteristics of TFETs [34]. As shown in Fig. 1.9, by reducing the drain side doping concentration, the BTBT from the

drain to the channel was significantly suppressed and the ambipolar current was reduced by several orders of magnitude [34]. Actually, both of these approaches, by reducing channel-drain overlap or decreasing drain doping concentration, are not fundamentally different and both suppress the ambipolar current by introducing a long depletion width and low electric field on the drain side [32]. As a result, combination of these two methods can further reduce the ambipolar current of a TFET device.

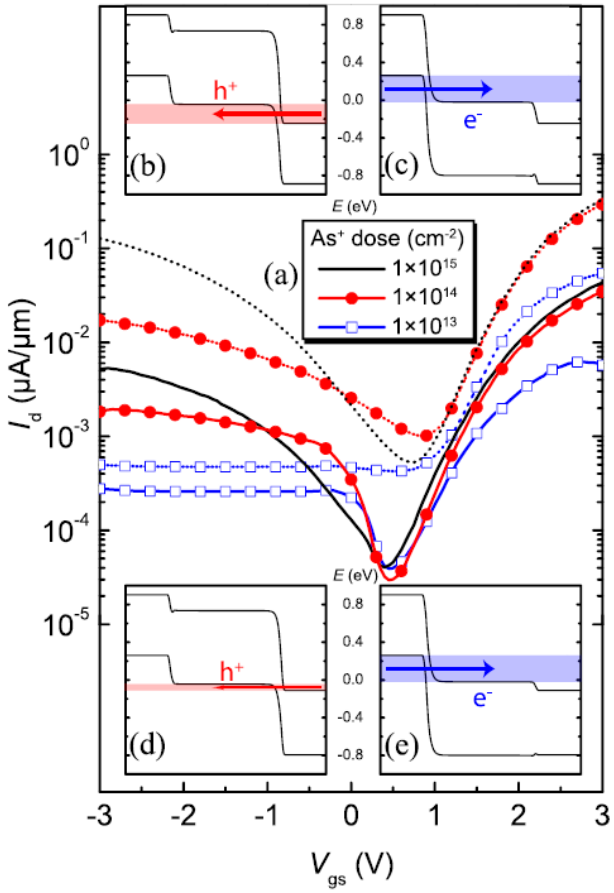


**Figure 1.9** (a) Transfer characteristics of $Si_{0.5}Ge_{0.5}$ n-TFETs with Source/Drain implantations of $1\times10^{15}$ $BF_2^+/cm^2$ [$1\times10^{15}$ $BF_2^+/cm^2$ (black), $1\times10^{14}$ (red) and $1\times10^{13}$ $As^+/cm^2$ (blue), respectively]. Solid curves are for $V_{DS}$=0.5V and dotted for $V_{DS}$=1.7V. (b)-(e) The simulated band structure displayed in the insets indicate the influence for the drain dopant concentration on the tunneling current: (b) and (c) $N_A = N_D = 2\times10^{20}cm^{-3}$; (d) and (e) $N_A = 2\times10^{20}cm^{-3}$, $N_D = 1\times10^{19}cm^{-3}$. The bias conditions are (b) and (d) $V_{DS}$ = 0.1V, $V_{GS}$ = -0.5V and (c) and (e) $V_{DS}$ = 0.1V, $V_{GS}$ = 0.5V. [34] Used with permission of Nanotechnology Reviews.

## 1.3 A brief history and state-of-the-art results of TFETs

In 1978, Quinn *et al.* at Brown University [35] firstly proposed the gated p-i-n structure of TFET. Banerjee *et al.* at Texas Instruments [36] studied the behavior of a three-terminal silicon tunnel device using a $p^-$ region instead of an i-region under the gate. Takeda *et al.* at Hitachi [37] fabricated a band-to-band tunneling MOS device on silicon and showed lack of $V_{TH}$ roll-off as scaling of the device. In 1995, Reddick and Amaratunga at Cambridge [38] demonstrated the measured characteristics of silicon surface tunnel transistors to replace traditional MOSFETs with faster operating speed and without scaling problems. In 2000, Hansch *et al.* at University of the German Federal Armed Forces in Munich [39] showed experimental results from a reverse-biased vertical silicon tunneling transistor made by molecular beam epitaxy (MBE). The transistor has a heavily delta doped layer to create an abrupt tunnel junction and noted the saturation behavior in the output characteristics. In 2004, Appenzeller *et al.* [40] demonstrated BTBT in carbon nanotube. The research of TFET is under a rapid growth after 2004 by using different material systems, including Ge [32, 41, 42], SiGe [43, 44], III-V [8-15], *etc*.

In recent years, the performances of TFET devices were significantly improved by the utilization of III-V material systems, heterostructures, band alignment engineering, high-κ gate dielectric and strain engineering. Table 1.1 summarizes the recently reported experimental III-V TFET devices and state-of-the-art performances of TFETs with different band alignments. Dewey *et al.* [45] firstly reported an III-V TFET in experimental with a room temperature minimum SS less than 60mV/dec (~58eV/dec) in an $In_{0.53}Ga_{0.47}As$ homojunction using a thin $In_{0.7}Ga_{0.3}As$ pocket layer at the source/channel interface. However, due to the large tunneling barrier within homojunction TFETs, the $I_{ON}$ is still remains low. Mookerjea and Mohata *et al.* [9, 15, 46] studied the $In_xGa_{1-x}As$ homojunction TFETs with different In compositions.

Experimental results showed that by increasing In composition from 0.53 to 0.7, $I_{ON}$ increased by 167%, from 24μA/μm to 60μA/μm. The increase in $I_{ON}$ is due to the enhanced tunneling probability caused by the reduction of bandgap energy. By using $In_{0.7}Ga_{0.3}As$ $p^+/i$ high indium composition pocket layers at source/channel junction as well as using $HfO_2$ as gate oxide, Zhao *et al.* [47] reported an $In_{0.53}Ga_{0.47}As$ homojunction TFET with an $I_{ON}$ of 50μA/μm and room temperature minimum SS of 86mV/dec. The SS was predicted to be further reduced by eliminating $D_{it}$ at $HfO_2$/InGaAs interface. The application of heterojunctions further improved the performance of TFETs, especially in an $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered gap heterostructure. Mohata *et al.* [9], [48] reported $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered TFETs with different effective tunneling barrier height. The effective tunneling barrier height was reduced by increasing In composition in $In_xGa_{1-x}As$ side and increasing Sb composition in $GaAs_ySb_{1-y}$ side while keeping the active region ($In_xGa_{1-x}As/GaAs_ySb_{1-y}$) to be internally lattice matched. The $I_{ON}$ of fabricated TFETs was increasing with reduced $E_{beff}$. Besides, the $I_{ON}$ of mixed As/Sb staggered gap TFETs is much higher than that of homojunction device with the same channel material, which directly demonstrated the advantages of this mixed As/Sb staggered gap structure. The $I_{ON}/I_{OFF}$ ratio was also improved by interface engineering. By using $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ as source/channel material, Mohata *et al.* [48] reported a TFET with high $I_{ON}$ of 135μA/μm with $I_{ON}/I_{OFF}$ ratio of 27,000. In 2013, Bijesh *et al.* demonstrated the record drive current of 740μA/μm at a cut-off frequency of 19GHz at drain to source voltage of 0.5V using $In_{0.9}Ga_{0.1}As/GaAs_{0.18}Sb_{0.82}$ near broken gap material system [49]. However, due to the traps-assist-tunneling (TAT) process involved in the transport of subthreshold region, the SS of the mixed As/Sb staggered gap TFETs is not sub-60mV/dec. As a result, further investigations should be taken to optimize the device fabrication process and additional studies are necessary to

find better high-κ dielectric with low interface states and better gate control. Table 1.1 also summarized the latest experimental results of mixed As/Sb broken gap (InAs/GaSb or $InAs_ySb_{1-y}$/GaSb) TFETs. Zhou *et al.* [50] reported $I_{ON}$ of 380μA/μm in a TFET using an InAs/GaSb heterostructure with a broken band alignment. Nevertheless, additional measures should be taken to turn OFF this kind of devices due to the normally ON properties of the broken gap alignment [51, 52]. Cho *et al.* [42] simulated Si compatible compound semiconductor TFET structures (Ge/GaAs) and demonstrated promising performance. Guo *et al.* [53] firstly demonstrated strained Ge/$In_{0.53}Ga_{0.47}As$ TFET experimental by re-growth of Ge on $In_{0.53}Ga_{0.47}As$ buffer. However, due to the high resistance associated with the tunneling junction and the channel region, the drive current of this transistor is low. The transfer characteristics of recently reported experimental III-V and strained Ge/InGaAs TFET devices are summarized in Fig. 1.10. The SS of 60mv/dec is also denoted in this figure.

## 1.4 Dissertation objective and organization

The objective of this work is to comprehensively investigate the structure properties and device performances correlations of TFETs using mixed As/Sb and Ge/InGaAs based heterostructures, including the structural design, alloy composition control, TFET structure growth by MBE, heterointerface engineering, material characterization, device fabrication, device performance measurement and high temperature reliability studies.

This dissertation is organized in 9 chapters. Chapter 2 introduces and discusses in detail of the key considerations for design of TFETs. The trade-off parameters, including band alignments, doping concentration, channel length and gate dielectrics were discussed systemically. A comprehensive consideration of TFET structure design and material system selection was presented based on all these discussions.

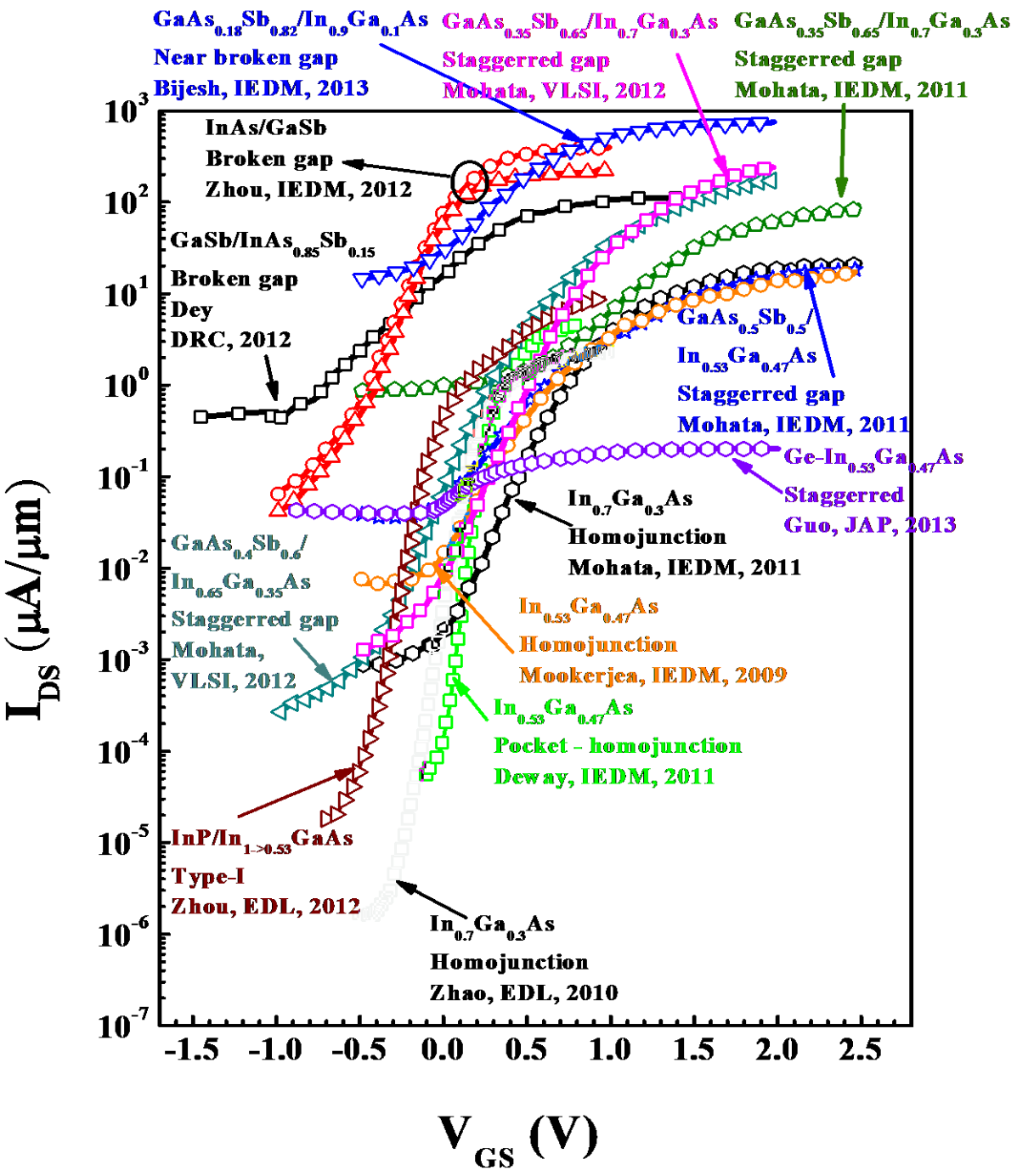


**Figure 1.10** Summaries the transfer characteristics of experimental III-V and Ge/InGaAs TFET devices. The SS of 60mv/dec is also denoted in this figure.

Chapter 3 presents the experimental methods used in this study for material growth, structural characterization and device fabrication.

Chapter 4 presents the MBE growth of mixed anion $GaAs_ySb_{1-y}$ materials in a wide Sb composition range from 15% to 62%. The influence of different growth parameters, such as growth temperature, Sb/Ga ratio, As/Ga ratio, *etc.*, on the alloy composition was systemically investigated. Three different high-κ gate dielectric, *i. e.*, $Al_2O_3$, $HfO_2$, $Ta_2O_5$, were integrated on $GaAs_{0.38}Sb_{0.62}$ material by atomic layer deposition. The band alignment of these different high-κ gate dielectric materials on $GaAs_{0.38}Sb_{0.62}$ was investigated by x-ray photoelectron spectroscopy (XPS).

Chapter 5 presents the structural properties and device performances of MBE grown mixed As/Sb tunnel FET heterostructures with GaAs-like and InAs-like interface at the source/channel region. The structural properties and device performances of these two structures with different heterointerface were compared. The interface engineering during the switching from Sb rich $GaAs_{0.35}Sb_{0.65}$ to As rich $In_{0.7}Ga_{0.3}As$ was optimized. The band alignment properties of these structures were investigated using XPS. Based on these results, the tailor-made effective tunneling barrier height and a high quality source/channel interface with well-maintained low defect density is highlighted for mixed As/Sb TFET structure.

Chapter 6 presents the high temperature reliability studies of both structural and electrical properties of mixed As/Sb staggered gap TFETs from 25$^o$C to 150$^o$C. The high temperature reliability studies showed stable structural properties and distinct device performances of this mixed As/Sb staggered gap TFETs at high operation temperature, which highlights the importance of the reliability on high temperature operation of TFETs for future low-power digital logic applications.

Chapter 7 presents the structural properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type TFET structure grown by MBE for complementary TFET applications. These structural properties showed high quality of this structure and provided critical guidance for the fabrication of As/Sb based staggered gap complementary TFETs for ultra-low standby power and energy efficient logic applications.

Chapter 8 presents the tensile strained $Ge/In_{0.16}Ga_{0.84}As$ heterostructure grown *in-situ* by MBE using two separated growth chambers for Ge and III-V materials as an alternative path to further improve the performance of TFETs. The superior structural properties suggest tensile strained $Ge/In_{0.16}Ga_{0.84}As$ heterostructure would be a promising candidate for high-performance and energy-efficient tunnel field-effect transistor applications.

Finally, Chapter 9 summarizes the conclusions of this work and recommended possible future areas of investigation.

**Table 1.1** Performance comparisons of experimental III-V and Ge/InGaAs TFETs with different band alignments.
$SS_{MIN}$ and $SS_{EFF}$ stands for the minimum (point) and effective subthreshold slope, respectively. $SS_{EFF} = (V_{ON}-V_{OFF})/\log(I_{ON}/I_{OFF})$

| Reference | Source | Channel | Band alignment | Dielectric | EOT (nm) | $I_{ON}$ (μA/μm) | $V_{DS}$ (V) | $V_{GS}$ (V) | $V_{ON}$-$V_{OFF}$ (V) | $I_{ON}/I_{OFF}$ | $SS_{MIN}$ mV/dec | $SS_{EFF}$ mV/dec |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Zhou *et al.* IEDM, 2012 [50] | GaSb | InAs | Broken | $Al_2O_3/HfO_2$ | 1.3 | 380 | 1 | 1 | 2 | 7,500 | 200 | 520 |
| Zhou *et al.* IEDM, 2012 [50] | GaSb | InAs | Broken | $Al_2O_3/HfO_2$ | 1.3 | 180 | 0.5 | 0.5 | 1.5 | 6,000 | 200 | 400 |
| Dey *et al.* DRC, 2012 [54] | GaSb | $InAs_{0.85}Sb_{0.15}$ | Broken | $Al_2O_3/HfO_2$ | 2.3 | 110 | 0.3 | 1.5 | 3 | 275 | 300 | 1200 |
| Zhou *et al.* EDL, 2012 [55] | InP | $In_{1->0.53}GaAs$ | Type I | $Al_2O_3/HfO_2$ | 1.3 | 20 | 0.5 | 1 | 1.75 | 450,000 | 93 | 310 |
| Mohata *et al.* VLSI, 2012 [48] | $GaAs_{0.35}Sb_{0.65}$ | $In_{0.7}Ga_{0.3}As$ | Staggered | $Al_2O_3/HfO_2$ | 2 | 135 | 0.5 | 1 | 1.5 | 27,000 | 169 | 350 |
| Mohata *et al.* VLSI, 2012 [48] | $GaAs_{0.4}Sb_{0.6}$ | $In_{0.65}Ga_{0.35}As$ | Staggered | $Al_2O_3/HfO_2$ | 2 | 78 | 0.5 | 1 | 1.5 | 15,000 | 179 | -- |
| Mohata *et al.* IEDM, 2011 [9] | $GaAs_{0.5}Sb_{0.5}$ | $In_{0.53}Ga_{0.47}As$ | Staggered | $Al_2O_3/HfO_2$ | 1.5 | 60 | 0.75 | 1 | 1.5 | >1,000 | ~300 | -- |
| Zhao *et al.* EDL, 2010 [47] | $In_{0.7}Ga_{0.3}As$ | $In_{0.7}Ga_{0.3}As$ | Pocket-homojunction | $HfO_2$ | 1.2 | 50 | 1.05 | 2 | -- | >10,000 | 86 | 380 |
| Mohata *et al.* IEDM,2011 [9] | $In_{0.7}Ga_{0.3}As$ | $In_{0.7}Ga_{0.3}As$ | Homo-junction | $Al_2O_3/HfO_2$ | 1.5 | 60 | 0.75 | 1 | 1.5 | 6,000 | ~200 | -- |
| Mookerjea *et al.* IEDM, 2009 [46] | $In_{0.53}Ga_{0.47}As$ | $In_{0.53}Ga_{0.47}As$ | Homo-junction | $Al_2O_3$ | 4.5 | 24 | 0.75 | 1 | 1.5 | 10,000 | ~200 | -- |
| Dewey *et al.* IEDM, 2011 [45] | $In_{0.53}Ga_{0.47}As$ | $In_{0.53}Ga_{0.47}As$ | Pocket-homojunction | $TaSiO_x$ | 1.1 | 5 | 0.3 | 0.8 | 0.9 | 70,000 | 58 | 190 |
| Bijesh *et al.* IEDM,2013 [49] | $GaAs_{0.18}Sb_{0.82}$ | $In_{0.9}Ga_{0.1}As$ | Staggered | $Al_2O_3/HfO_2$ | 2 | 740 | 0.5 | 2.0 | 2.5 | ~40 | ~300 | -- |
| Guo *et al.* JAP 2013 [53] | Ge | $In_{0.53}Ga_{0.47}As$ | Staggered | $Al_2O_3$ | 2.5 | 0.4 | 0.2 | 2 | 3 | ~300 | 177 | -- |

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# Chapter 2 Key considerations for design of TFETs

## 2.1 Band alignments and effective tunneling barrier height

Based on different band alignment types of the source/channel materials, TFET can be classified to (i) homojunction, (ii) staggered gap, and (iii) broken gap structures. The schematic band diagrams of these three types of TFET at ON-state are shown in Fig. 2.1 (a), (b) and (c), respectively. For a homojunction TFET, the same material was used in both source and channel regions and the tunnel junction is formed by the heavy doping concentration in the source side. As a result, the sharpness of the doping profile at the tunnel junction is critical for a homojunction TFET, as it determines the tunneling barrier width (λ) of carrier from source to the channel. A major drawback of homojunction TFETs is the lack of high $I_{ON}$ [1] due to the relatively larger tunneling barrier width (λ). By taking the advantage of band alignments in heterojunction transistors, this figure of merit can be drastically improved, as predicted theoretically [2]. Some heterostructures offer a staggered band alignment, allowing a steeper band structure profile over the junction than homojunction which is achievable only by using doping modulation [3]. As shown in Fig. 2.1 (b), the staggered gap TFET is formed by two different materials with a type-II band alignment (e.g., $In_xGa_{1-x}As/GaAs_ySb_{1-y}$) at source/channel interface. Compared with homojunction as shown in Fig. 2.1 (a), the tunneling barrier width (λ) is reduced in the staggered gap TFET, resulting in higher $I_{ON}$ [4, 5]. A broken gap TFET is formed by a type-II broken (also been referred as type-III) heterointerface (e.g., InAs/GaSb) at the source/channel interface, which further reduced the tunneling barrier width (λ) and leading to even higher $I_{ON}$.

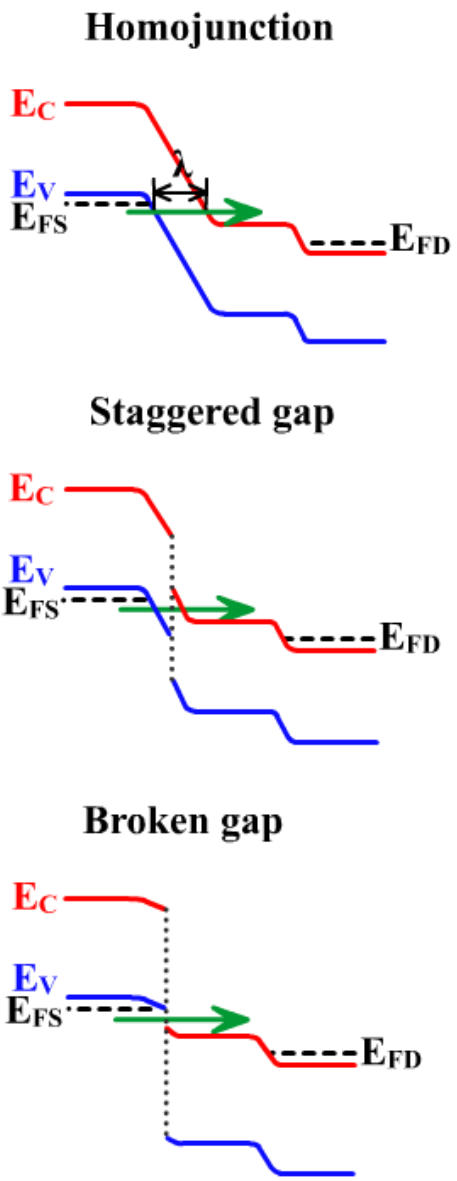


**Figure 2.1** The schematic band diagrams of (a) homojunction (b) staggered gap and (c) broken gap TFET at ON-state. For homojunction TFETs, the same material was used for source, channel and drain regions. Homojunction TFETs usually exhibit low ON-state current due to the relatively large tunneling barrier width (λ). For staggered gap TFET, the source/channel junction is formed by two different materials with a type-II staggered band alignment (like $In_xGa_{1-x}As/GaAs_ySb_{1-y}$). The tunneling barrier width (λ) of a staggered gap TFET is reduced compared with homojunction, resulting in a much higher $I_{ON}$. For broken gap TFET, the source/channel tunnel junction is formed by a type-II broken heterostructure (also been referred as type-III, like InAs/GaSb), which further reduces the tunneling barrier width (λ) and leads to even higher $I_{ON}$. However, due to the normally ON feature of the broken gap TFET, an additional gate voltage is needed to turn OFF this kind of device.

An important parameter for designing a TFET device is the effective tunneling barrier height ($E_{beff}$), which is defined as the energy difference between the channel conduction band minimum and the source valence band maximum for an n-type TFET but the energy difference between the source conduction band minimum and the channel valence band maximum for a p-type TFET, as shown in Fig. 1.3 (b) and 1.3 (c), respectively. This $E_{beff}$ plays a significant role on the performance of a TFET device, which not only determines the ON-state tunneling current but also sets the blocking barrier for the OFF-state leakage [6]. For homojunction and staggered gap TFETs, the $E_{beff}$ is a positive value. The advantage of the staggered gap TFET is that the $E_{beff}$ can be well modulated by changing the material compositions on both source/channel sides. As a result, a tailored-made $E_{beff}$ can be achieved in a staggered gap TFET to boost $I_{ON}$ without sacrificing $I_{OFF}$. In principle, a lower $E_{beff}$ is always preferred in designing TFET structures so that more tunneling carriers can be generated under the same gate bias, which in turn leads to a higher $I_{ON}$. Experiments have already proved that by reducing $E_{beff}$ from 0.5eV to 0.25eV results in at least 200% improvement of $I_{ON}$ in mixed As/Sb heterojunction TFETs due to the increase of tunneling transmission coefficient [4, 7]. However, if $E_{beff}$ is scaled to a negative value ($E_{beff} < 0$), a broken bandgap alignment will be formed at the source/channel interface. Although further improvement is expected on $I_{ON}$ for a broken gap TFET due to the removal of tunneling barrier, $I_{OFF}$ will increase simultaneously and thus additional gate bias is required to turn off this tunneling mechanism [8]. As a result, for a broken gap TFET with negative $E_{beff}$, the direct tunneling is taking place even without gate bias and an extra gate bias (negative for n-type and positive for p-type) is needed to turn this kind of device OFF.

## 2.2 Doping levels and band gap energy of source, channel and drain

The doping levels of TFET source, channel and drain must be carefully optimized in order to maximize $I_{ON}$ and minimize $I_{OFF}$ [9]. In principle, the source region must be heavily and abruptly doped to boost $I_{ON}$. Dopant abruptness less than 4nm/decade is necessary to maximize the junction electric field that enable high $I_{ON}$ [10]. This common practice, however, has some tradeoffs to $I_{ON}$ and SS if the source doping concentration is too high. As shown in Fig. 2.2 (a) for a n-type TFET, the source region is highly degenerated due to heavily p-type doping, which results in the source Fermi level $E_{FS}$ lies below the valence band maximum $E_V$. At a given temperature, electrons will partially occupy the states in the valence band between $E_V$ and $E_{FS}$ according to the Fermi Dirac distribution. When a gate bias is applied, channel conduction band states will firstly be paired with source valence band electrons whose energy is between $E_V$ and $E_{FS}$ [11]. However, due to high degenerate source material, these states are only partially occupied, which results in a reduced fraction of paired tunneling states to contribute to the conduction and thus degrades $I_{ON}$. On the other hand, to achieve higher efficiency of turn-on, which relates to steeper SS, every paired source valence band and channel conduction band states should be utilized to transport electrons via BTBT [11]. As a result, the high degenerate source material also degrade SS due to less available electrons in the source valence band within the energy window $\Delta\Phi$ as shown in Fig. 2.2 (a). In contrast, a TFET structure with a lower doped source region demonstrates an $E_{FS}$ closer to $E_V$ in Fig. 2.2 (b). In this case, majority of the source valence band states are occupied, providing ample supply of electrons to contribute to tunneling when paired up states are available [10, 11], resulting in steeper SS and higher $I_{ON}$ at lower $V_{GS}$.

Despite of the degradation of SS and $I_{ON}$, the highly degenerated source also increases the OFF-state leakage due to the tunneling process via band tail states [3, 12]. The band tails caused

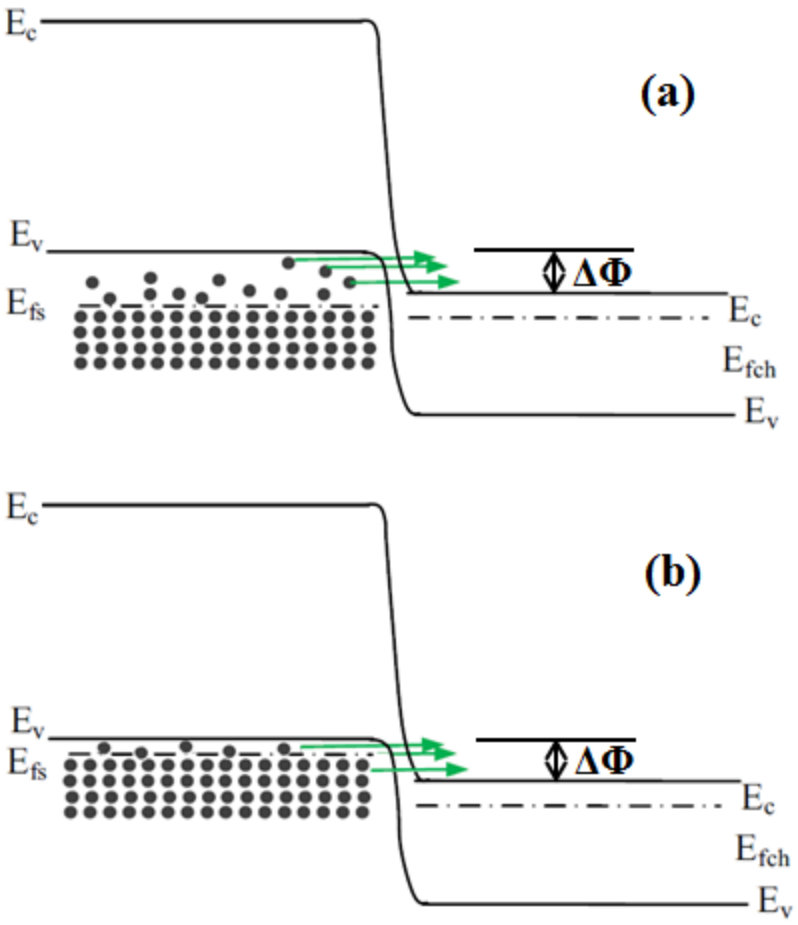


**Figure 2.2** (a) Schematic band diagram of inefficient turn-ON of an n-type TFET device if the source region is highly degenerated. Energy states in the source valence band in the energy window ΔΦ is only partially occupied according to Fermi Daric distribution, resulting in reduced $I_{ON}$ and degraded SS. [11] (b) Schematic band diagram of a TFET structure with a lower doped source. Majority of the source valence band energy states are occupied, providing ample supply of electrons to contribute to tunneling when paired up states are available, resulting in steeper SS and higher $I_{ON}$ at lower $V_{GS}$. Used with permission of Nanotechnology Reviews.

by heavy doping decay exponentially [13, 14, 15] into the bandgap as $e^{-|E-E_{C,V}|/E_0}$, where $E_{C,V}$ is the conduction (valence) band edge and $E_0$ is the Urbach parameter which can be comparable to the room temperature thermal energy, $k_BT$ = 26meV[12]. The band tails extend density of states into the bandgap, which gives rise to the enhancement of tunneling from band tail states to the channel at OFF-state, resulting in further increase of $I_{OFF}$. Besides, the energy states from

band tails extending into the bandgap reduce the energy difference between these states and the mid-gap traps, which in turn enhance the SRH G-R leakage at OFF-state [12]. Nevertheless, although an over-doped source region can degrade SS, $I_{ON}$ and $I_{OFF}$, it is not desirable to introduce a lightly doped source in TFET structures, which reduces the electric field at the tunnel junction and increases excessive series resistance. A possible compromise may introduce moderately heavily doped pocket layer only adjacent to the tunnel junction and keep the other region of the source at an appropriate lower doping concentration [4, 5, 12].

The channel region of TFET is kept unintentionally doped in most TFET designs [4, 5, 16, 17]. Although simulations show that the lightly doped channel will not change the turn-on properties significantly [9], the $I_{OFF}$ is increasing simultaneously with the increasing doping concentration of the channel [18]. The drain side doping significantly influences the performance of TFET devices especially at OFF-state due to the ambipolar characteristics as discussed in ***Chapter 1.2.5***. As a result, an appropriate doping concentration in the drain region is also necessary to balance the series resistance and the ambipolar leakage.

The selection of bandgap energies of source, channel and drain is another key factor during the design of TFET structures. Using a smaller band gap material in the source is predicted to significantly enhance the tunneling current [2, 19]. However, the reduction of source material bandgap also introduces the risk of increasing $I_{OFF}$ due to the enhanced thermal emission at OFF-state, which is proportional to $e^{-(E_G/nkT)}$. In practice, the channel material with a larger bandgap is preferred to reduce the standby leakage current caused by thermal generation. The channel material with a larger bandgap can also provide higher joint density of states to accept the source electrons. However, in the mixed As/Sb staggered gap n-type heterostructure TFET using $GaAs_ySb_{1-y}$ as the source and $In_xGa_{1-x}As$ as the channel and drain, a channel material with higher

Indium (In) composition (corresponds to lower $In_xGa_{1-x}As$ bandgap) is needed to reduce the $E_{beff}$ and enhance $I_{ON}$. Giving these material considerations, appropriate channel band gap should be selected to yield reasonable large $I_{ON}$ without increasing excessive leakage [11]. The bandgap of the drain side is usually selected to be large in order to introduce asymmetric to reduce the ambipolar leakage from drain to channel.

## 2.3 High- κ gate dielectric

The gate dielectric determines the capacitive coupling of the gate with the tunnel junction in a TFET device [20]. It has already been reported that high-κ gate dielectric provides the gate with better capacitive control of the tunnel junction [17, 21], which leads to better performance of TFET devices, both steeper SS and higher $I_{ON}$. As shown in Fig. 2.3 (a), Boucart *et al.* [21] demonstrated by simulation that $I_{DS}$ of TFETs increases as the gate dielectric constant increases. In this figure, $Si_3N_4$ (ε = 7.5) and two high-κ gate dielectric with dielectric constants of 21 and 29 (such as $HfO_2$ and $ZrO_2$) are compared with $SiO_2$ (ε = 3.9), all of which has a physical thickness of 3nm. It can also be found in this figure that, in addition to the improvement of $I_{ON}$, both the point and average SS are improved due to the better gate coupling given by a high-κ dielectric [9, 21]. Despite the high dielectric constant, the thickness of high-κ gate dielectric also significantly influences the performance of TFETs. Mohata *et al.* [5] demonstrated that by scaling the electrical oxide thickness ($T_{OXE}$) of gate dielectric ($Al_2O_3/HfO_2$ stack) from 2.3nm to 2nm, an enhancement of $I_{ON}$ by a factor of 3.5 was obtained in an n-channel $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered gap TFET. However, the reduction of gate dielectric thickness also introduces the risk of increasing in gate leakage. Zhao *et al.* [17] reported in $In_{0.7}Ga_{0.3}As$ TFETs that with 8nm $HfO_2$ gate dielectric, both SRH G-R and BTBT currents contribute to $I_{OFF}$; however, for TFETs with 5nm $HfO_2$ gate oxide, the gate leakage current also contributes to $I_{OFF}$, resulting in a smaller $E_A$

(activation energy). In addition to the improvement of ON-state performance, the high-κ dielectric also provides the gate with better control of turning OFF the device, especially at a shorter gate length [20].

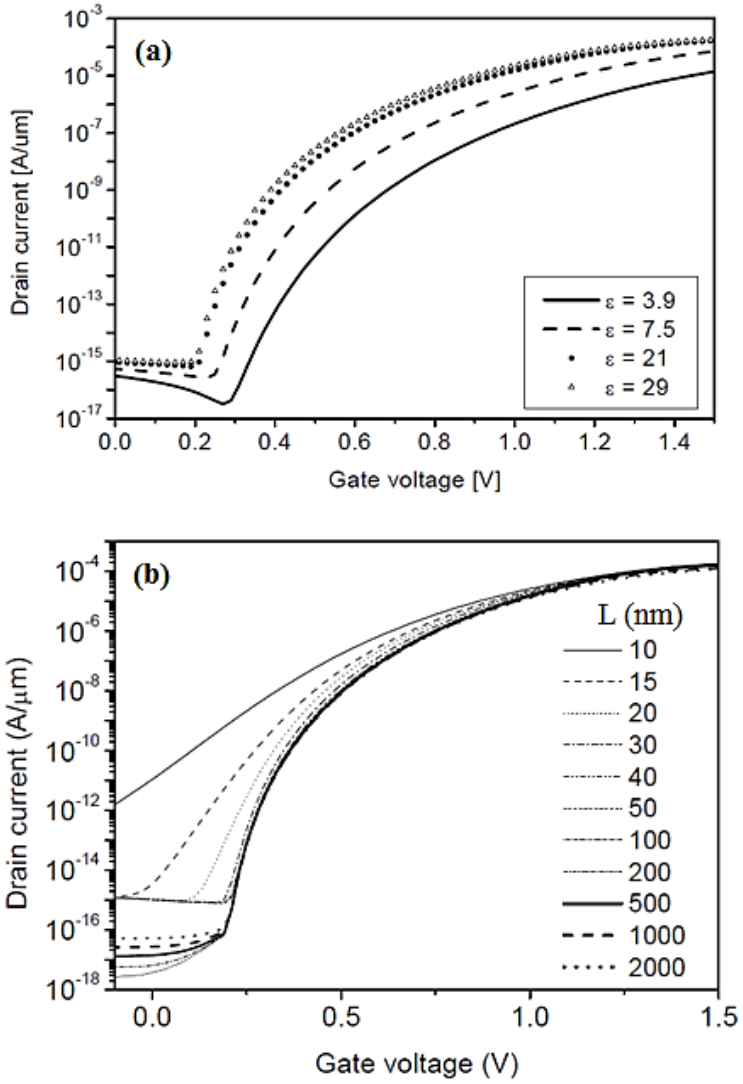


**Figure 2.3** (a) Comparison of transfer characteristics of TFETs with different gate dielectrics by simulation. Four different gate oxides with the same physical thickness of 3nm are used in the simulation. By using high-κ gate dielectric, both the drive current and SS of TFETs are improved due to better gate coupling. (b) Comparison of the transfer characteristics of TFETs with different channel lengths. The ON-state current of TFET does not change obviously with reduced channel length, however, the OFF-state leakage current increases by several orders of magnitude with scaling of channel length. OFF-state current increases sharply as the channel length less than 50nm. [20] Used with permission of Nanotechnology Reviews.

While high-κ gate dielectrics have advantages for device performances, they can also bring in defects at the semiconductor/high-κ interface if the high-κ gate dielectric is deposited directly on the channel material [9], which will introduce the deleterious effects on the carrier mobility of the device [9, 20, 22, 23]. Although the drive current of TFETs is less sensitive to the changes of channel mobility than MOSFETs since the tunneling transport at source/channel junction dominates any scattering in the channel, these interface defects will deteriorate the performance of TFETs and lead to degradation of SS. These interface traps can retard the Fermi-level movement of the intrinsic channel layer which is controlled by the gate bias, and they can also result in the interface trap assisted tunneling and the subsequent thermal emission, which caused the high temperature dependence of SS [5, 24, 25, 26]. In order to reduce these interface states and also to be compatible with standard CMOS fabrication techniques, an interfacial oxide layer with better oxide/semiconductor interface is required between the high-κ gate dielectric and the semiconductor channel. Zhao *et al.* [17] compared the performance of an $In_{0.7}Ga_{0.3}As$ TFET with and without the interfacial oxide layer, which shows that $Al_2O_3/HfO_2$ bilayer gate oxides effectively improve SS compared with single $HfO_2$ gate oxide due to a better InGaAs/oxide interface. On the other hand, $Al_2O_3/HfO_2$ bilayer oxides do not show an effective improvement of $I_{ON}$ compared with single $HfO_2$ gate oxide, which also proved that the $I_{ON}$ of TFETs primarily depends on the tunneling probability at source/channel interface instead of the channel electron mobility.

## 2.4 Channel length

The channel length of TFET is not as critical as that of MOSFET on determining the ON-state performance as the $I_{ON}$ of TFET is determined by the tunneling current at the source/channel junction instead of the scattering in the channel. In contrast, the OFF-state

leakage of TFET is greatly dependent on the channel length especially as the channel length is aggressively scaled. Figure 2.3 (b) [20] shows the simulated transfer characteristics of TFETs using high-κ gate dielectric (ε = 25, without interfacial oxide layer) with different gate lengths. It can be found from this figure, without noticeable change of $I_{ON}$, the $I_{OFF}$ increases by several orders of magnitude with scaling of channel length, especially as the channel length is less than 50nm [20], which indicates that the gate lost its ability to efficiently turn off the device. This can be explained by Zener breakdown mechanism [20, 27], where electrons can still tunnel through the tunnel junction at OFF-state without gate voltage. The reduced channel length decreases the tunneling barrier width from source to channel and results in the Zener breakdown in TFET devices.

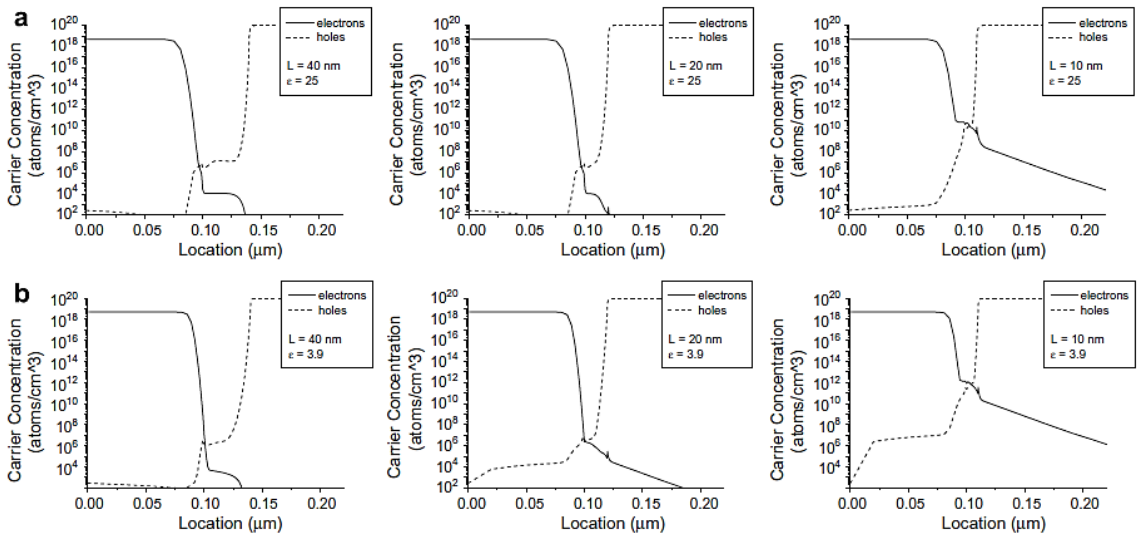


**Figure 2.4** Electron and hole concentrations of the cross-section of a TFET using different gate dielectrics, (a) ε = 25 and (b) ε = 3.9, there is no interfacial oxide layer within the high-κ gate dielectric stacks. With the scaling of channel length, the depleted regions are becoming narrower and less defined. With the channel length equals to 10nm, devices with both types of gate dielectrics are showing Zener breakdown (electron tunneling) at OFF-state, although the high-κ device shows a small advantage of showing a lower carrier concentration in the intrinsic region under the gate. [20] Used with permission of Nanotechnology Reviews.

Toshio Baba [28] predicted that it would be possible to scale TFETs (surface tunnel transistors) to a gate length equals to the depletion layer width, on the order of 10nm, where electron tunneling is suppressed. In an ungated p-i-n diode, the depletion region includes the entire intrinsic region in addition to the depleted areas of the p- and n- regions. Figure 2.4 (a) and (b) [20] demonstrates the electron and hole concentrations of the cross-section of a TFET using different gate dielectrics (ε = 3.9 and ε = 25, the high-κ gate dielectric is without interfacial oxide layer) by simulations. With the scaling of channel length, the depleted regions are becoming narrower and less defined. At channel length equals 10nm, devices with both types of gate dielectrics are showing Zener breakdown (electron tunneling) at OFF-state.

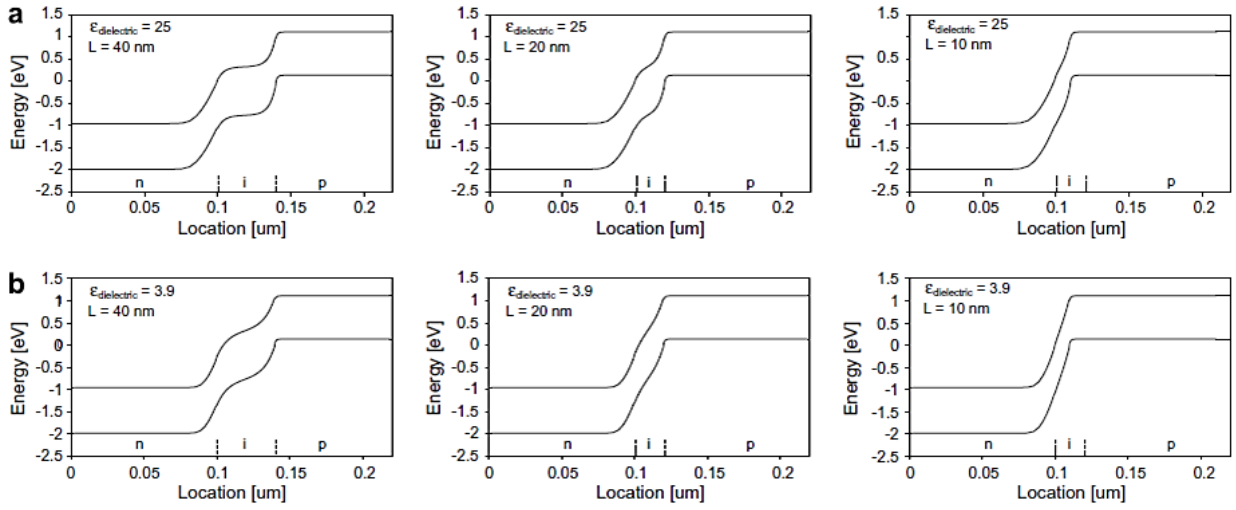


**Figure 2.5** Schematic band diagrams of TFETs with different gate dielectrics, (a) ε = 25 and (b) ε = 3.9, there is no interfacial oxide layer within the high-κ gate dielectric stacks. With a channel length of 40nm, both devices are effectively turned off and the depletion region was well-defined. When the channel length was reduced to 20nm, the TFET using low gate dielectric (ε = 3.9) begins to break down. At channel length of 10nm, the devices break down in both cases with a tunneling width less than 10nm. [20] Used with permission of Nanotechnology Reviews.

Another way to check the depletion region width is to examine the energy band diagram across the TFET devices [9, 20]. The depletion region corresponds to the region between the flat band within the n-type region and flat band within the p-type region in energy band diagrams. As

shown in Fig. 2.5 (a) and (b) [20] for TFET band diagrams using different gate dielectrics (ε = 3.9 and ε = 25, the high-κ gate dielectric is without interfacial oxide layer) by simulations, both of the devices are effectively turned OFF with the well-defined depletion region with a channel length of 40nm. When the channel length was reduced to 20nm, the TFET using low gate dielectric (ε = 3.9) begins to break down. At channel length of 10nm, the devices break down in both cases with a tunneling barrier width less than 10nm. In that case, neither of the devices can be well turned OFF, and the gate lost its control to the tunneling barrier modulation, resulting in high leakage current as shown in Fig. 2.3 (b). As a result, the channel length of TFETs cannot be aggressively scaled to result in the Zener breakdown of the device.

## 2.5 Comprehensive consideration of the TFET design

Based on all these discussions above, structure and device design optimization should be applied to increase $I_{ON}$, reduce $I_{OFF}$ and improve SS, simultaneously, to offer a device with a comprehensive desirable performance. As TFET is a device depending on the BTBT mechanism at the source/channel junction to transport carriers, the tunneling probability determines the tunneling current of a TFET device. In order to achieve higher tunneling probability, the tunneling barrier should be reduced, which can be achieved by using higher source doping concentration, smaller bandgap source material and staggered or broken band alignment. As high degeneration caused by heavily source doping will reduce available states for tunneling and thus degrade the $I_{ON}$ and SS [11], a modulated heavily pocket doping layer only near the tunnel junction is essential [5]. In addition, a direct band gap and smaller carrier effective mass can also contribute to improve $I_{ON}$ [6, 7, 29, 30]. In this respect, III-V materials are highly attractive, as they typically have low effective carrier mass and direct band gaps that allow for efficient tunneling [3].

Another optimization criterion is to reduce $I_{OFF}$, including all leakage current components: the ambipolar leakage, the SRH G-R leakage, and the tunneling leakage. In order to reduce ambipolar current, asymmetric configuration, both asymmetric bandgaps and asymmetric doping concentration between the source and drain, should be introduced for the design of TFET structures [31]. Considering a source region with smaller bandgap and higher doping is necessary to increase $I_{ON}$, the drain material should be designed to have a relatively larger bandgap and lower doping concentration (but not be too low to increase serial resistance). Besides, in order to reduce SRH G-R leakage, large bandgap materials are desired, but large band gap materials are not desired for ON-state performance. As a result, the material bandgaps should be carefully selected to achieve higher $I_{ON}$ without scarifying $I_{OFF}$. Furthermore, in order to reduce the tunneling leakage, the tunnel barrier at source/channel junction should be enlarged to block unwanted tunneling at OFF-state [6], which can be achieved by homojunction or staggered band alignment. As the homojunction TFET has its own drawback for low $I_{ON}$, the staggered band alignment is a preferable choice for TFET design to achieve higher $I_{ON}$ and lower $I_{OFF}$. Besides, the tunneling barrier height should also be well modulated for a staggered band alignment to achieve a balance between high $I_{ON}$ and low $I_{OFF}$.

A sharp interface at the source/channel junction is needed to achieve steep SS, which requires both abrupt doping profile and minimum atoms inter-diffusion. To achieve better gate control to the channel energy bands movement, a high-κ gate dielectric is also necessary. Besides, an interfacial oxide layer is needed between high-κ gate dielectric and channel to reduce carrier scattering at the channel/oxide interface. In addition, it has been increasingly clear that the high-κ dielectric on the Al bearing III-V compounds showed an increased SS due to larger

interface induced defects ($D_{it}$) [32]. As a result, a channel material without Al component is also benefitted to achieve steeper SS.

All the above considerations related to TFET design are summarized in Fig. 2.6. In view of all these considerations, mixed As/Sb based heterostructures namely, $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ are very attractive as they allow a wide range of bandgaps and staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at the source/channel heterointerface can be tailed-made by carefully controlling the compositions of the mixed As/Sb material system while keeping this material system internally lattice matched. Besides, sharp heterojunction interface and abrupt doping profile can also be achieved by molecular beam epitaxy (MBE). Minimum atoms inter-diffusion can be well realized by carefully control the shutter sequence during switching from Sb rich material to As rich material [29]. As a result, the mixed As/Sb staggered gap TFET is considered as a promising option for high-performance, low standby power and energy efficient logic application.

Another approach for designing high performance TFET is utilizing tensile strained Ge/InGaAs heterostructures. In past few decades, Ge has been actively investigated due to its high intrinsic carrier mobility, small band gap energy and silicon (Si) compatible process flow [33, 34, 35]. In addition, tensile strained Ge exhibited further reduction in band gap energy and enhanced electron and hole mobility [34, 35, 36], making it a highly promising material for low power TFET applications. Ge/InGaAs heterostructure satisfies the requirements for low band gap material system in a TFET design. More importantly, by carefully controlling the alloy composition in InGaAs material, the magnitude of tensile strain inside the Ge layer can be tailored such that the $E_{beff}$ between the Ge source and the InGaAs channel can also be well-modulated, both of which will facilitate the further optimization of TFET structure.

In the following chapters, the detailed material growth, structure optimization, material characterization, device fabrication, together with the related experimental or simulated structural properties and device performances of TFETs using both mixed As/Sb and tensile strained Ge/InGaAs heterostructures will be discussed.

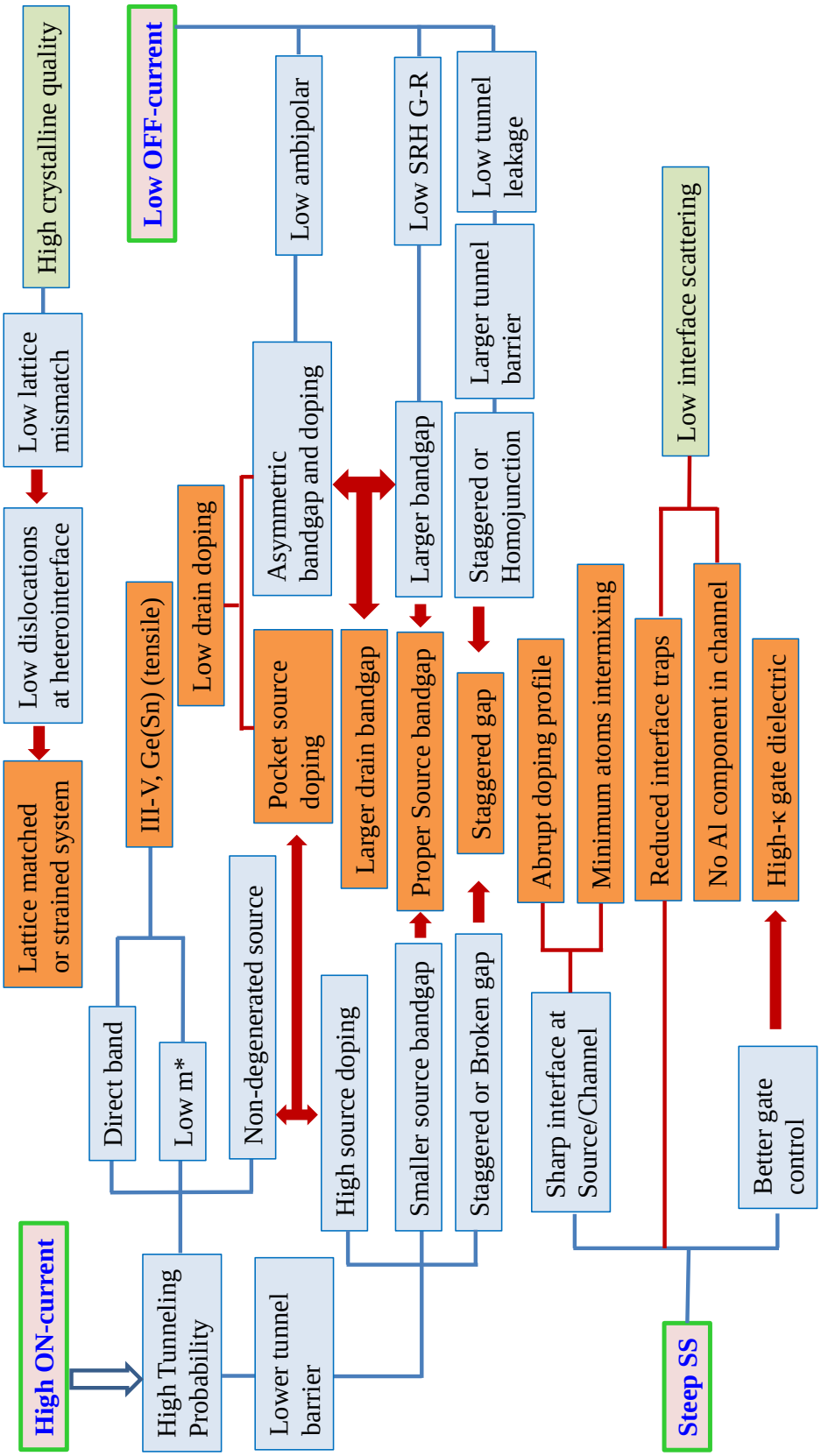


**Figure 2.6** A comprehensive consideration of a TFET design.

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# Chapter 3 Experimental methods: TFET structure growth, characterization and device fabrication

## 3.1 Molecular beam epitaxy growth of mixed As/Sb and tensile strained Ge TFET structures

All the structures studied in this dissertation were grown by solid source molecular beam epitaxy (MBE). MBE is a physical-vapor deposition technique, which is widely applied in research labs and industrial production. The constituent elements of the crystalline solid are transported from the sources to the substrate using molecular beams. A molecular beam is a directed ray of neutral atoms or molecules in a vacuum chamber. In MBE, the beams are usually thermally evaporated from solid or liquid elemental sources. The characteristic feature of MBE is the mass transport in molecular or atomic beams. A vacuum environment is required to ensure that no significant collisions occur among the beam particles and between beam and background vapor. A schematic diagram of an MBE growth chamber is shown in Fig. 3.1 [1]. The vacuum is generated in a chamber by different pumps (roughing dry pump, turbo pump, ion pump, cryo-pump, *etc*.) and cryo-shrouds. Usually effusion cells mounted opposite to the substrate producing beams of different species by evaporation. The duration of the exposure on the substrate is individually controlled by shutters for a rapid change of material composition or doping. The substrate is mounted on a heated holder and can be loaded and unloaded under vacuum conditions by a manipulating mechanism. An ion gauge can be placed opposite to the substrate heater to measure and calibrate the beam-equivalent pressure (BEP) produced by the individual sources. The vacuum environment maintained during epitaxy provides an excellent opportunity for *in-situ* monitoring of the growth process. Virtually any MBE system is equipped with an

electron-diffraction setup. Usually reflection high-energy electron diffraction (RHEED) with an electron beam nearly parallel to the growth surface is applied, yielding structural information on the surface crystallography during oxide-desorption and during the epitaxy [1].

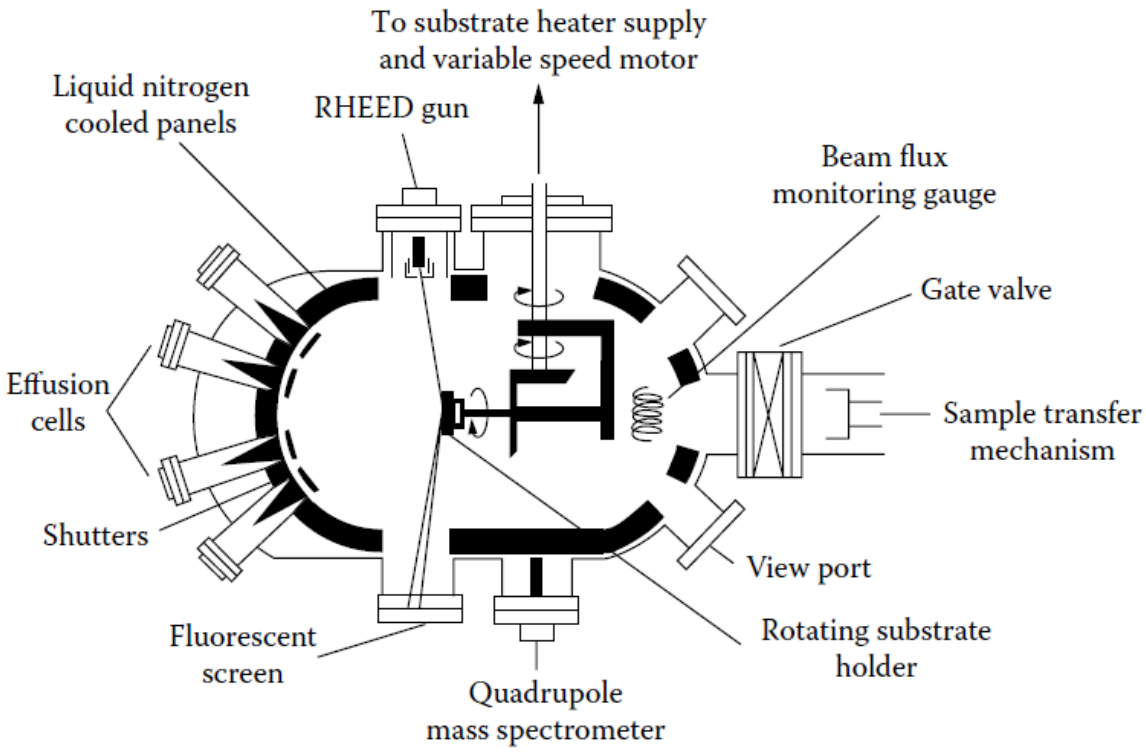


**Figure 3.1** Schematic representation of MBE growth chamber. The circular arrow indicates the positioning of the gauge at the location of the substrate to calibrate the beam-equivalent pressure of the cells which contain different source materials.

MBE is performed in ultra-high vacuum (UHV), *i. e.*, at a residual-gas pressure below $10^{-7}$ Pa ($10^{-9}$ torr). The requirement of UHV conditions arising from the purity requirement also ensures the beam nature of the molecular sources. The condition of a sufficiently large mean free path of effused particles in the range of typical dimensions of MBE setup (order of $10^{-1}$ m) is already fulfilled in a pressure range below $10^{-1}$ Pa. To reach UHV, all materials used in the vacuum chamber must have very low evolution of gas and a high chemical stability. Tantalum and molybdenum are widely used for shutters, heaters and other components. The entire MBE

chamber is baked out typically at 200$^{o}$C for several days any time after having vented the system. Spurious fluxes of atoms and molecules from the walls of the chamber are minimized by a cryogenic cooling shroud chilled using liquid $N_2$ [1]. Besides, all the substrate materials used for MBE growth also need to be well degassed before loading into the growth chamber. Take GaAs substrate as an example, the substrate is firstly baked in the intro-chamber at 180$^{o}$C for three hours and then been transferred into a buffer chamber to be further outgassed at 420$^{o}$C for more than 60 minutes to remove the residual impurities from the substrate. After that, the substrate will be transferred into the growth chamber. The oxide-desorption process will be performed to remove the native oxide on the surface of the substrate before any epitaxial growth. The surface temperature for GaAs oxide-desorption is typically 580$^{o}$C measured by pyrometer. The oxide desorption process is performed under group-V elements protection and usually monitored by RHEED.

In a typical RHEED experiment, a high energy (10-100 KeV) beam of electrons is incident on the sample surface at a shallow angle of 1 to 2$^{o}$. Diffraction of the electrons is governed by the Bragg law, as with x-ray diffraction (XRD). However, there are two important differences between RHEED and XRD. First, the electrons do not penetrate significantly into the sample, so diffraction is essentially from the two-dimensional lattice on the surface. Second, for the high-energy electrons used in RHEED, the Ewald sphere is large in diameter, so many reflections are excited at once [2]. Because the diffraction occurs from a two-dimensional net of atoms on the surface, the reciprocal lattice comprises a set of rods perpendicular to the surface in real space. The electrons in a RHEED experiments behave as waves, with a de Broglie wavelength given by $\lambda = \frac{hc}{E}$, where h is the Plank constant, c is the speed of light, and E is the electron energy. For an electron has an energy of 100 KeV corresponding to a de Broglie wavelength of 3.7pm, the

radius of the Ewald sphere is $|k_0|$ = 1700 $nm^{-1}$, whereas the separation of the rods in the reciprocal lattice $2\pi/a$ might be about $20nm^{-1}$. The Ewald sphere is so large compared to the separation of the reciprocal lattice rods that it will intersect several rods, exciting several Bragg reflections for any given geometry. The diffraction pattern therefore comprises a set of streaks as shown in Fig. 3.2 [2].

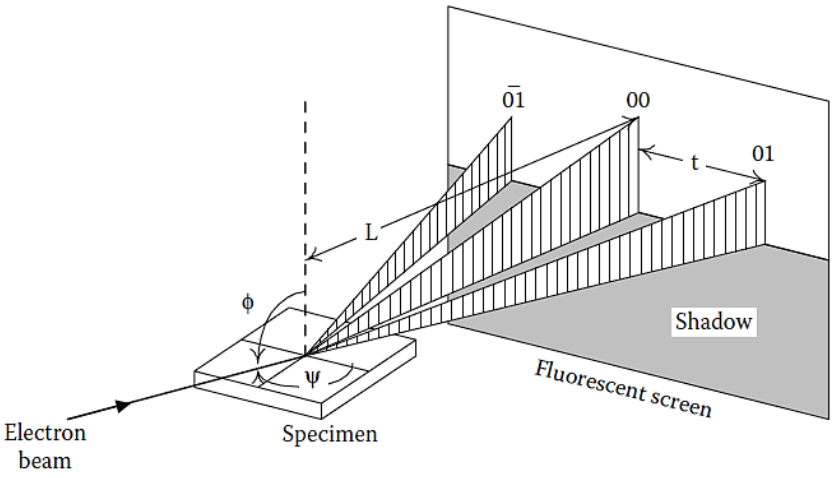


**Figure 3.2** Schematic of RHEED experiment.

RHEED is commonly used *in-situ* during MBE growth to discern the growth mode and growth rate. The surface roughness, and therefore the growth mode, may be discerned from the nature of the RHEED pattern. As noted previously, a streaky pattern is an indication of an atomically flat surface. In the case of a rough surface, the electron beam will penetrate islands or other structures on the surface, giving rise to diffraction from a three-dimensional lattice. Therefore, the RHEED pattern becomes spotty in this case. The growth rate may be determined from RHEED intensity oscillations, for which the period corresponds to one monolayer of growth [2]. The measured RHEED oscillation from the GaAs surface is shown in Fig. 3.3. By recording the oscillation frequency and incorporating the monolayer thickness (half of lattice constant for GaAs), the growth rate can be determined.

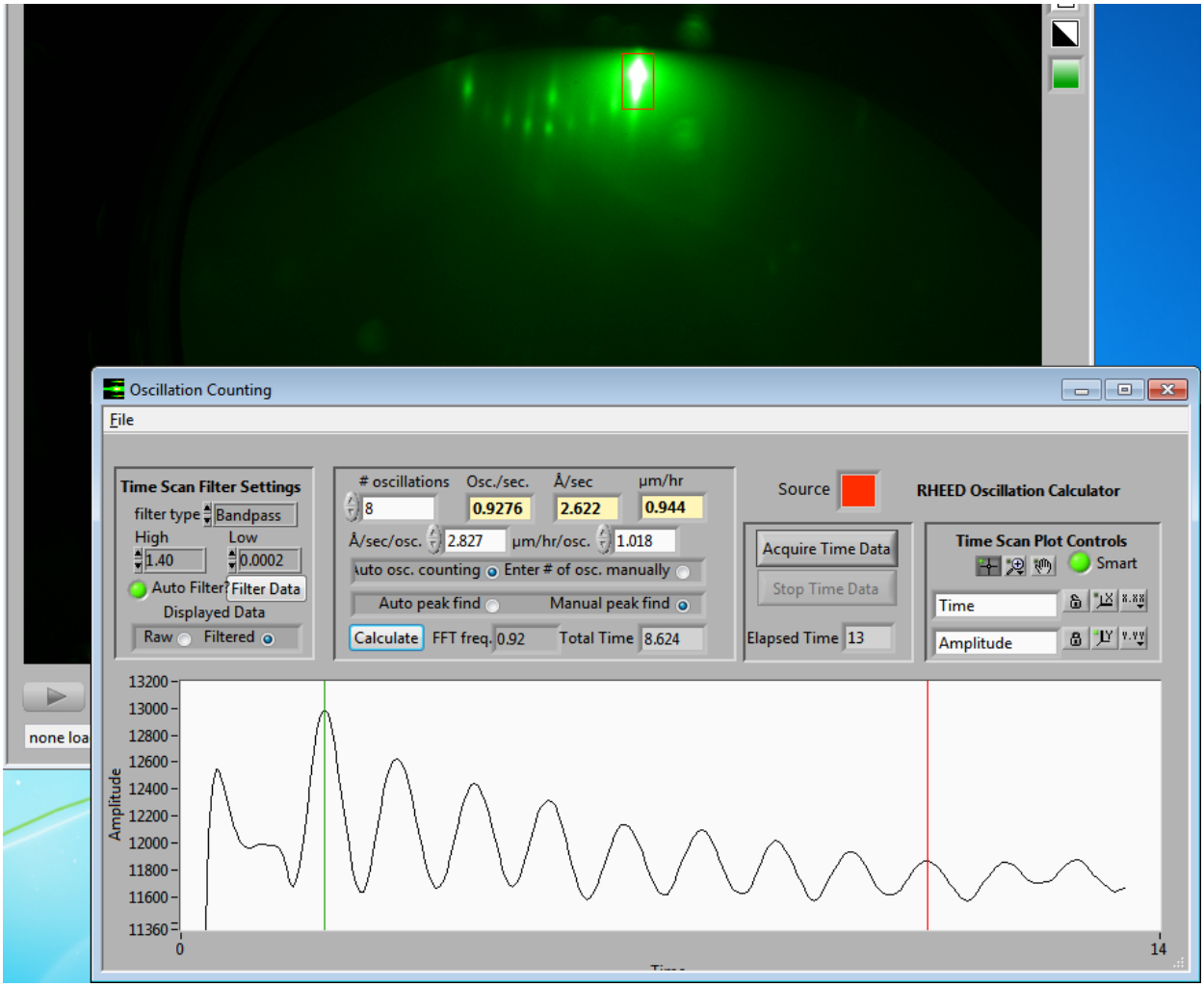


**Figure 3.3** RHEED oscillation from the GaAs surface. The growth rate of GaAs can be determined from RHEED oscillations by recording the oscillation frequency and incorporating the mono-layer thickness.

In practice, different growth rates at different growth III element BEP will be measured for GaAs, InAs and AlAs, respectively. The substrate used for RHEED oscillation must be on-axis. After the measurement of growth rate at different growth III element BEP, the relationship of growth rate as a function of group III BEP can be plotted. Figure 3.4 shows the relationship of GaAs growth rate with Ga BEP. It can be seen from this figure that the GaAs growth rates show a linear relationship with Ga BEP in a wide range. Once this relationship has been fitted, other growth rates can be determined by measuring the corresponding group III element BEP.

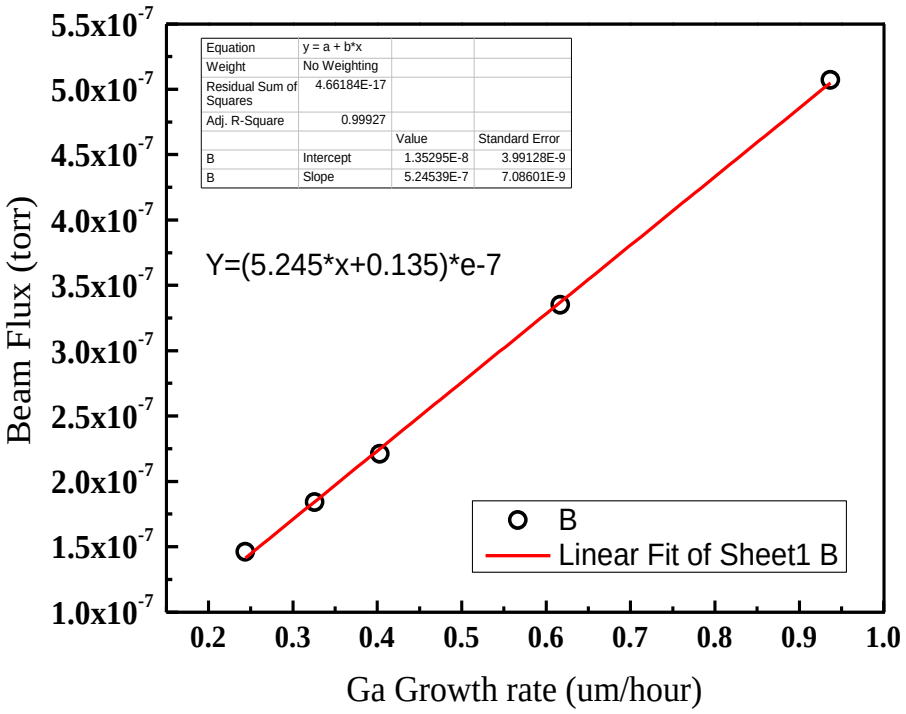


**Figure 3.4** GaAs growth rate as a function of Ga BEP.

The growth rate calibration of GaAs, InAs and AlAs will be performed separately on different substrates (GaAs and AlAs are on GaAs substrate, InAs is on InAs substrate). However, the growth rate will be different for the same material at the same BEP depending on the different substrates it is growing on. For example, the InAs growth rate is calibrated on InAs substrate, but different InAs growth rate is expected if the same BEP is used but grown on GaAs substrate because of the lattice constant difference between GaAs and InAs. As a result, a sensitivity factor should be included in the calculation of growth rates if different elements are used in the MBE growth. The growth rate difference of InAs on InAs substrate and GaAs substrate can be calculated using the following equation:

$$(R_{InAs})_{onInAs} = (\frac{a_{InAs}}{a_{GaAs}})^2 \times (R_{InAs})_{onGaAs} = (\frac{6.0584}{5.6532})^2 \times (R_{InAs})_{onGaAs} = 1.148\,(R_{InAs})_{onGaAs} \quad (3.1)$$

where $(R_{InAs})_{onInAs}$ is the growth rate of InAs on InAs substrate in the unit of ML/s and $(R_{InAs})_{onGaAs}$ is the growth of InAs under the same In BEP but grown on GaAs substrate.

The doping concentration of MBE grown films can be calibrated by Electrochemical Capacitance-voltage (ECV) measurements. GaAs layers with different doping source temperature can be grown on the same substrate and the doping concentration of each layer can be measured by ECV. The doping cell temperature has exponential relationship with the doping concentration which will be a straight line if the doping concentration is plotted in a log scale on y-axis as shown in Figure 3.5. 2D delta is open used during MBE growth, the relationship of 2D doping with 3D doping can be calculated in the following equation:

$$n(2D)\left[\frac{\#}{cm^2}\right] = n(3D)\left[\frac{\#}{cm^3}\right] \times growth\ rate\ \left[\frac{cm}{s}\right] \times dopingtime\ [s] \quad (3.2)$$

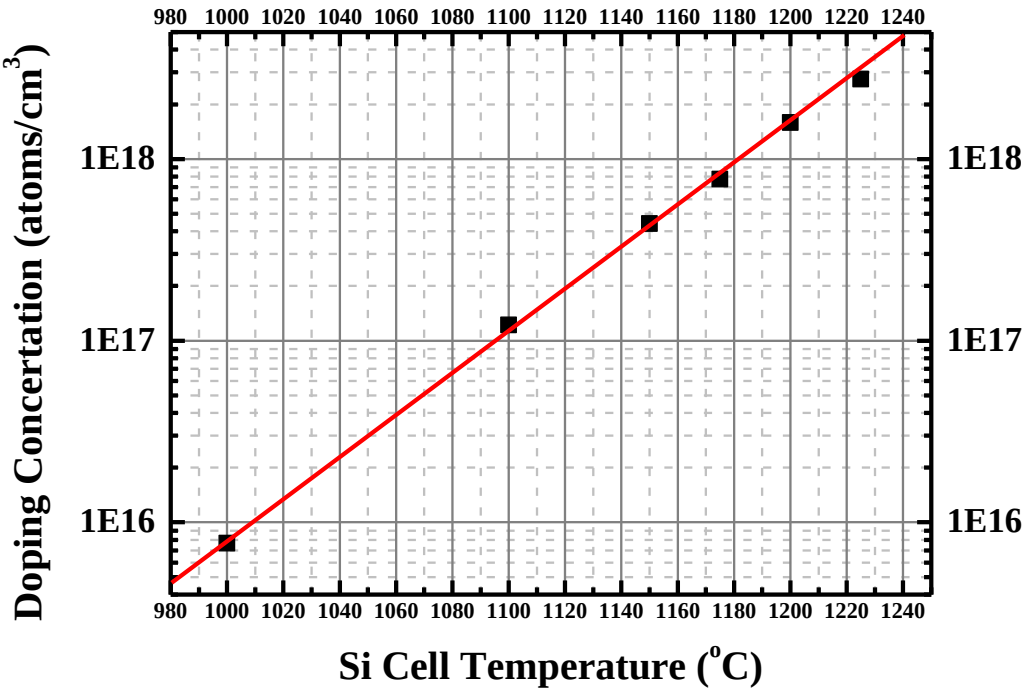


**Figure 3.5** Relationship of doping concentration of GaAs with doping cell temperature.

## 3.2 Material properties characterization methods

### 3.2.1 Strain relaxation properties: X-ray diffraction

High-resolution x-ray diffraction (HRXRD) is important in the structural characterization of heteroepitaxial layers, revealing lattice constants, strains, crystallographic orientation and defect densities. A typical HRXRD is illustrated in Fig. 3.6 (a). The source of x-ray is usually an x-ray tube, producing a divergent beam with a broad spectrum. The beam is conditioned (limited in both angular divergence and wavelength spread) by four diffracting surfaces arranged in a Bartels monochromator. The conditioned beam is then diffracted by the specimen crystal and measured using a scintillation detector. In a rocking curve measurement, the specimen is rotated about the ω-axis as shown in Fig. 3.6(b) [3]. The diffracted intensity is measured as a function of the specimen angle ω. The positions, intensities, and widths of the intensity peaks in the rocking curve are used to characterize the structural properties of the specimen crystal.

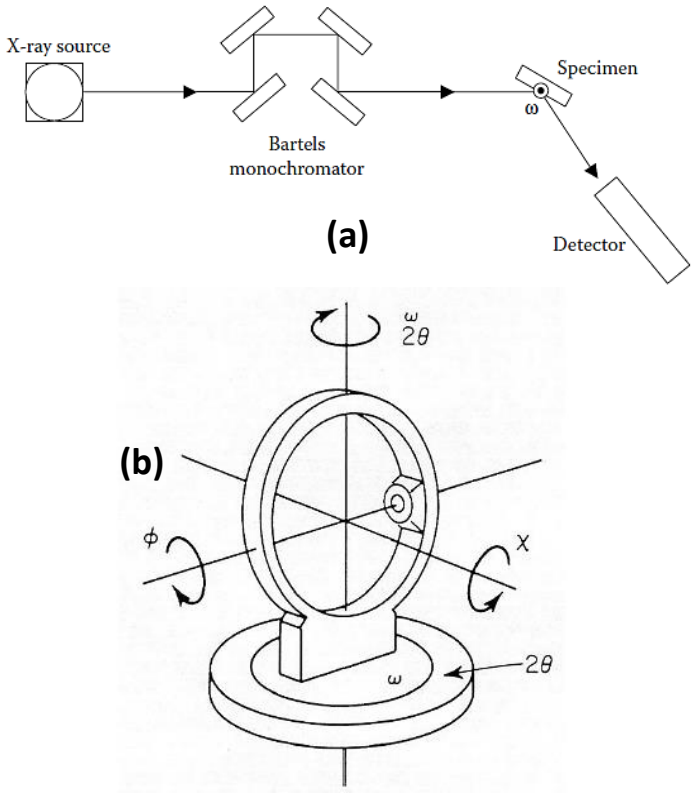


**Figure 3.6** (a) Basic setup for high-resolution x-ray diffraction and (b) four circle diffractometer.

The characterization of XRD can be performed using two equivalent ways: the Bragg equation, which is a geometric equation in real space, and the Laue equations, which are the equivalent condition expressed in reciprocal space. Figure 3.7 shows the diffraction of x-ray beam which can be calculated by Bragg equation. Here an x-ray beam is incident on a set of crystal planes with separation d. If the angles of the incidence and reflection are equal to θ (specular reflection), then the path difference Δ between the beams a and b is 2dsinθ. The condition for constructive interference is Δ = nλ, where n is an integer and λ is the x-ray wavelength. Thus, the condition for diffraction is [2]

$$2d\sin\theta_B = n\lambda \tag{3.3}$$

where n is the order of the reflection. This is the Bragg equation, and $\theta_B$ is the Bragg angle.

For a cubic crystal with lattice constant *a*, the spacing of the (hkl) planes is

$$d(hkl) = \frac{a}{\sqrt{h^2+k^2+l^2}}. \tag{3.4}$$

The *hkl* Bragg angle is then

$$\theta_B(hkl) = sin^{-1}[\frac{\lambda\sqrt{h^2+k^2+l^2}}{2a}] \tag{3.5}$$

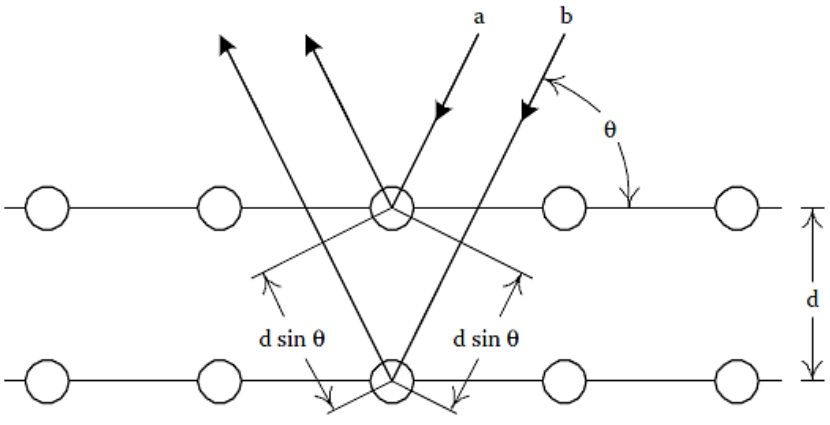


**Figure 3.7** The Bragg condition for diffraction.

Detailed strain relaxation analysis for diamond and zinc-blende semiconductors can be applied by reciprocal space maps (RSM). Formation of 60 ° a/2<110> {111} misfit dislocations (MDs) at film/substrate interfaces are the primary mechanism to relax misfit strain [4] and the lattice mismatch between the substrate and the mismatch epilayer can be accommodated by dislocation glide. Asymmetric dislocation distribution would result in different in-plane lattice constants along two orthogonal [110] and [1$\bar{1}$0] dislocation directions. As a result, the projection of the incident x-ray beam could be aligned with each of the in-plane <110> directions to measure the anisotropy in strain relaxation of the structures. Both symmetric (004) and asymmetric (115) RSMs need to be recorded to determine the alloy composition, the lattice mismatch, and the strain relaxation. In-plane lattice constant, *a* and out-of-plane lattice constant, *c* can be determined using Bragg's law from asymmetric and symmetric RSMs, respectively. The relaxed layer lattice constant, $a_r$ and the strain, ε of each layer with respect to the substrate can be calculated using [5]

$$a_r = \frac{2\upsilon}{1+\upsilon} a + \frac{1-\upsilon}{1+\upsilon} c \tag{3.6}$$

$$\varepsilon = \frac{a_r - a_s}{a_s} \tag{3.7}$$

where, $a_s$ is the lattice constant of the substrate, υ is Poisson's ratio of each ternary layer calculated from the elastic constants of InAs, AlAs, GaAs and GaSb using Vegard's law. From RSMs with different incident x-ray beam directions, $a_r$ and ε along [110] and [1$\bar{1}$0] directions can be determined. Relaxation of each layer with respect to the substrate in each <110> direction can also be expressed as,

$$R_{[110]} = \frac{a_{[110]} - a_s}{c_{[110]} - a_s} \text{ and } R_{[1\bar{1}0]} = \frac{a_{[1\bar{1}0]} - a_s}{c_{[1\bar{1}0]} - a_s}. \tag{3.8}$$

For isotropic relaxation, $R_{[110]} = R_{[1\bar{1}0]}$ and the average relaxation is $\bar{R} = (R_{[110]} + R_{[1\bar{1}0]})/2$.

The perpendicular lattice mismatch of epilayer with respect to the "virtual" substrate is [6]

$$f_{\perp} = \frac{c - a_0}{a_0} \tag{3.9}$$

where, $a_0$ is the relaxed lattice constant of "virtual" substrate. Similarly, the parallel lattice mismatch measured along the [110] and $[1\bar{1}0]$ directions are

$$f_{\parallel[110]} = \frac{a[110] - a_0}{a_0}; f_{\parallel[1\bar{1}0]} = \frac{a[1\bar{1}0] - a_0}{a_0} \tag{3.10}$$

where $a[110]$ and $a_{[}1\bar{1}0_{]}$ are in-plane lattice constants of epilayer along [110] and $[1\bar{1}0]$ directions, receptively. For the fully relaxed case, the lattice mismatch $f_r$ for fully relaxed layer is described as [4],

$$f_r = \frac{1-v}{1+v} f_{\perp} + \frac{v}{1+v}\left(f_{\parallel[110]} + f_{\parallel[1\bar{1}0]}\right). \tag{3.11}$$

The critical thickness, $h_c$ for the formation of misfit dislocations due to the strain relaxation can be estimated using the theoretical expression proposed by Matthews and Blakeslee [7],

$$h_c = \frac{b}{2\pi f_r} \frac{(1 - v\cos^2\alpha)}{(1+v)\cos\lambda} \left(ln\frac{h_c}{b} + 1\right) \tag{3.12}$$

where $b = |\boldsymbol{b}|$ is the magnitude of the dislocation Burgers vector **b**, α is the angle between the dislocation line and its Burgers vector, β is the angle between the slip direction and the direction in the film plane which is perpendicular to the line of intersection of the slip plane and the interface. Here, Burgers vectors of the dislocations were $\frac{1}{2}a\langle 110\rangle$ type and were inclined at 45 ° to (001) such that $b = |\boldsymbol{b}| = \frac{a_r}{\sqrt{2}}$ [8]. For 60°a/2 <110> {111} slip system, cosα = cosβ = ½ [7].

The strain relaxation properties of epitaxial layers can be represented from RSMs relating to **q** vectors. In RSMs, the vector **q** represents the deviation between the reciprocal lattice points (RLPs) of the substrate and epilayers. There are two components involve in **q** vector, $q_x$ and $q_z$, which corresponds to the angular splitting ω and 2θ, respectively, in real space. Reciprocal lattice points in RSMs might have different $q_x$ and $q_z$ positions depending on different relaxation degree and misorientation, corresponding to a fully strained (pseudomorphic) and a partially relaxed layer, or a fully relaxed (metamorphic) layer [9]. For a (115) asymmetric RSM of an ideal, fully relaxed epitaxial layer without tilt, the diffracted intensity from this layer is expected to fall on the fully relaxed line joining the (115) RLP of the substrate and having a 15.8 ° angle between the (001) and (115) direction. In contrary, a fully strained layer is expected to follow the fully strained line that joins the (115) RLP of the substrate and along (001) direction.

### 3.2.2 Surface morphology: Atomic force microscopy

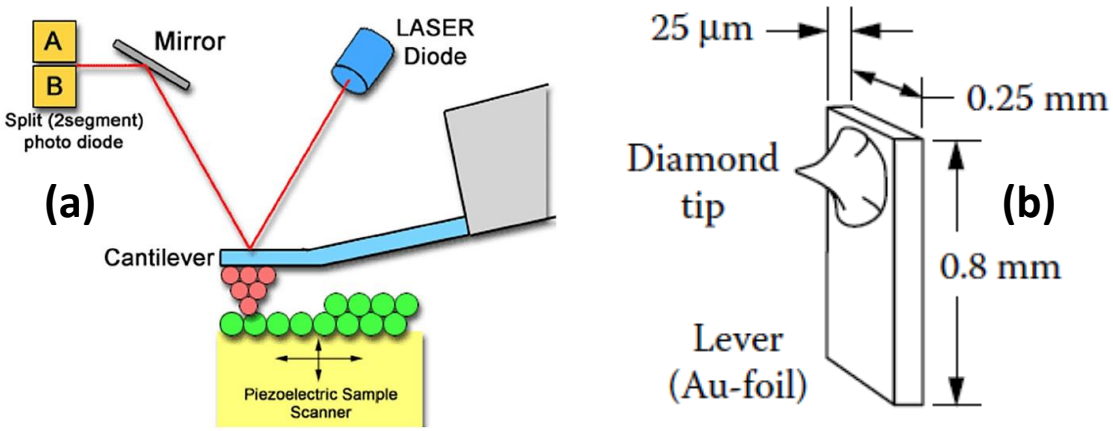


**Figure 3.8** (a) The schematic of atomic force microscopy and (b) the AFM tip.

The atomic force microscopy (AFM) is one of scanning probe microscopy (SPM) techniques which can reach a vertical resolution in angstrom range. The operation of AFM is shown in Fig. 3.8 (a). A cantilever with a sharp tip (which need not to be conducting as shown in

Fig. 3.8 (b)) is placed between the tip and the sample. In one scanning mode, a very small and constant force is maintained on the AFM tip. In another mode of operation, the force exerted on the AFM stylus by its piezoelectric element is adjusted for constant tunneling current. Regardless of the details of how the feedback system is employed, the z displacement of the tip corresponds to the z displacement of the surface examined by the AFM [2].

### 3.2.3 Defect properties: Transmission electron microscopy

Transmission electron microscopy (TEM) is a valuable technique for the observation of dislocations, stacking faults, twin boundaries, and other crystal defects in heteroepitaxial layers. TEM characterization is applicable to most heteroepitaxial semiconductor samples, provided that they can be thinned to transmit electrons and that they can stable when exposed to a high-energy electron beam in an ultrahigh vacuum. Conventional TEMs use electron energies of ~100 KeV, whereas this number can be ~1 MeV in a high-voltage TEM. For observation in a conventional TEM, typical heteroepitaxial semiconductor samples must be thinned to less than about 100nm.

The operation of a TEM instrument is shown schematically in Figure 3.8. Collimated high-energy electrons from a condenser lens impinge on the semiconductor specimen and are transmitted through it. The electrons are scattered into particular directions by the crystalline sample according to the Bragg law for diffraction. These diffracted beams are brought into focus at the focal plane for the objective lens. In the diffraction mode, the first intermediate lens is focused on the back focal plane of the objective lens, thus capturing the diffraction pattern. This diffraction pattern is magnified and projected by the combination of the intermediate and projection lenses. The diffraction pattern displayed on the screen comprises an array of spots, each corresponding to a particular diffraction vector **g**. The diffraction mode is used to index the diffraction beams and to facilitate the selection of the diffraction spots to be used in ultimately

forming an image. In the imaging mode, the intermediate lens is focused on the inverted image of the sample formed by the objective lens. This image is magnified and projected onto the screen with an overall magnification of up to $10^6$. An aperture at the back focal plane of the objective lens is used to select only one diffracted beam to form the image. If the beam transmitted directly through the image **g** = [000] is chosen, a bright-field image results. If one of the diffracted beams is chosen to form the image, then a dark-field image is produced [2].

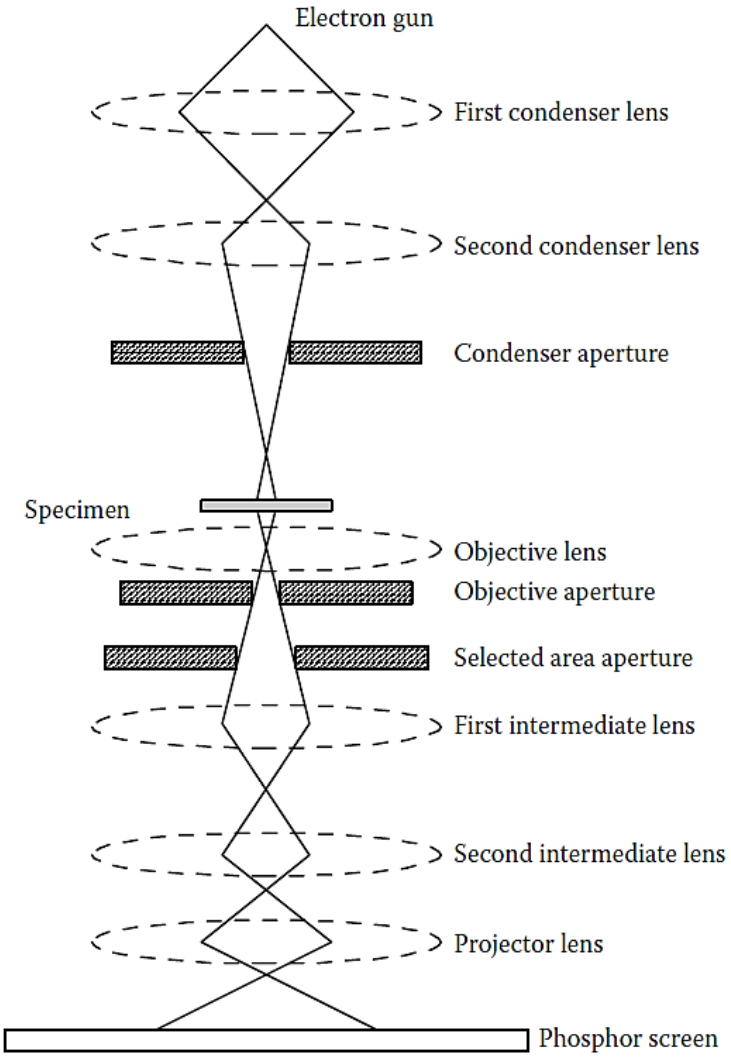


**Figure 3.9** Setup for Transmission Electron Microscopy.

### 3.2.4 Band alignment properties: X-ray photoelectron spectroscopy

The band alignment at the interface of heterostructures can be measured using x-ray photoelectron spectroscopy (XPS). The detailed experimental setup for measurement of band alignments will be discussed in detail in the following chapters. Figure 3.9 (a) shows the working principle of XPS equipment. X-ray beam irradiates a sample surface resulting in the ejection of photoelectrons from the core level (CL) of the atoms present in the sample as shown in Fig. 3.9(b). Photoelectrons are extracted and filtered with respect to their energy by the analyzer. The kinetic energy $E_k$ of photoelectrons is representative of the elements in the sample. The $E_k$ can be calculated using $E_k = h\upsilon - E_b - \phi$, where $h\upsilon$ is the energy of x-ray, $E_b$ is the binding energy of the elements being measured and $\phi$ is the work function of the sample material. The number of electron detected is measured as a function of their kinetic energy and then be converted to the binding energy. Due to the scattering of photoelectrons inside of the sample, only photoelectrons produced near the surface (<10nm depth) will have a higher probability of escaping from the surface without losing energy and will therefore produce a peak in the spectrum. Photoelectrons that lose energy will appear as a background at lower kinetic energy. Analysis depth is determined by the electron inelastic mean free path in the measured material.

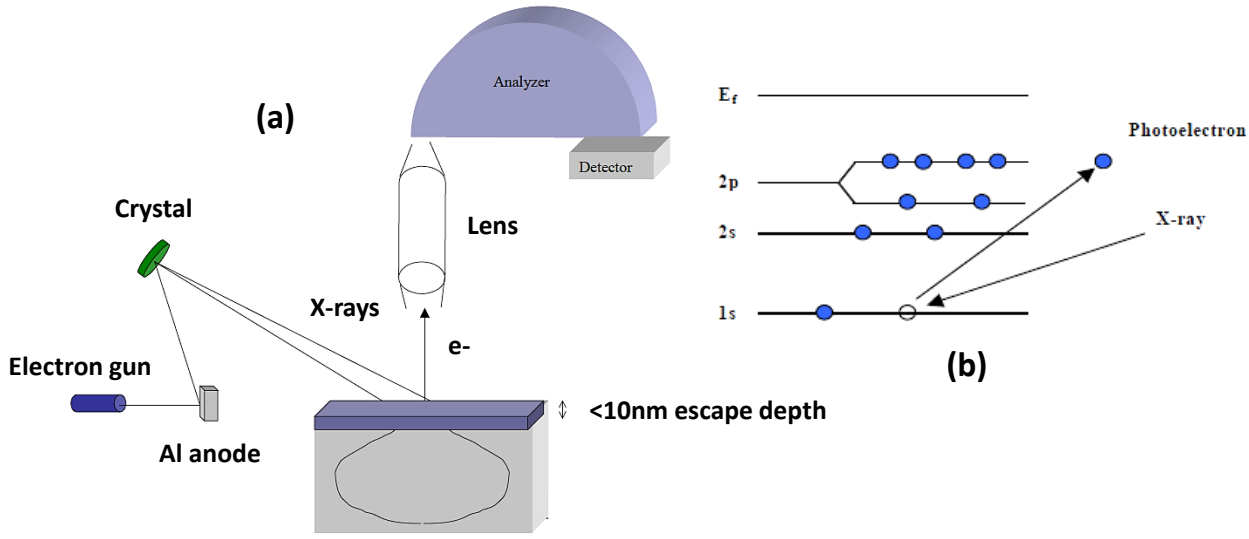


**Figure 3.10** (a) Setup for x-ray photoelectron spectroscopy and (b) excitation of photoelectrons by x-ray.

### 3.2.5 Interface and doping profile abruptness: Secondary ion mass spectrometry

Dynamic secondary ion mass spectrometry (SIMS) is a commonly used method to measure the heterointerface sharpness and doping profile abruptness. For SIMS measurement, an energetic ion beam (primary ion beam) bombards a sample surface causing surface material to be sputtered. Some part of the sputtered material is ionized (secondary ions) and these ions are extracted from the sample surface into a mass spectrometer (MS). MS separates the secondary ions according to their mass to charge ratios and counts them. An element profile can be generated with continues sputtering of the sample. The dynamic SIMS has an ultra-low detection limit down to 10 ppt. However, there are also some limits for SIMS measurements. The secondary ions yield is different between different matrices and this is referred as SIMS matrix effect. As a result, SIMS standards are required because secondary ion yield varies (by decades) both for different elements in the same matrix and for the same element in different matrices. Besides, high levels of an impurity (>1% atomic) can also affect the ion yield of the impurity by changing the observed ion concentration. Therefore, the upper detection limit for dynamic SIMS is 1%. In this respect, dynamic cannot be used to analyze the composition of compound semiconductors.

## 3.3 TFET device fabrication process

A main challenge for the fabrication of MBE grown vertical heterostructures TFETs is to perfectly align the gate on the channel area. Based on different fabrication processes, there are several different TFET device structures reported in the literature, such as single vertical side wall device structure [10-12], ring-type vertical side wall device structure [13, 14], self-aligned gate nano pillar device structure [15-18], *etc*. In order to further increase $I_{ON}$, double gate [19] or gate-all-round TFET [17, 20] device designs are used. Besides, the device design demands

extremely scaled gate oxide EOT and ultra-thin body geometry in order to achieve low $I_{OFF}$ and desired transistor performance [17]. In this dissertation, a vertical TFET fabrication process with self-aligned gate [17] was used which can ultimately lead to the ultra-thin gate-all-round device geometry to achieve superior TFET performance.

Figure 3.11 shows the cross-section schematics of the fabricated $In_{0.7}Ga_{0.3}As$ homojunction TFET device following by key process steps [17]. A summary of the entire fabrication process flow is also shown in this figure. 250nm thick molybdenum (Mo) was blanket deposited on the $n^+$ $In_{0.7}Ga_{0.3}As$ layer using e-beam evaporation. Cr/Ti dry etch masks with minimum width of 250nm were created on the top of Mo using e-beam lithography, e-beam evaporation and lift-off techniques. A nano-pillar was formed after the dry etch of Mo and $In_{0.7}Ga_{0.3}As$ layer. Wet etch process was performed to remove sidewall damage and create undercut. An undercut of about 50nm was obtained and it was ready for the formation of self-aligned gate. Here, the "self-aligned" referred to the isolation of the top contact and the side wall gate as a result of wet etch undercut of the nano-pillar. After the wet etch, high-κ gate dielectric layers consisting of 1nm $Al_2O_3$/3.5nm$HfO_2$ were deposited using plasma-enhanced atomic layer deposition at 250$^o$C and 20nm Palladium (Pd) gate was vertically deposited using e-beam evaporation. The entire structure was then planarized with benzocyclobutene (BCB) and cured at 250$^o$C for 60 minutes in nitrogen ambient. After curing, BCB was etched back to expose Pd on the top of Mo. Pd and high-κ on the source and drain areas were bombarded off using $Cl_2$ and Ar based dry etch recipe. Lithography was followed to open large contact pads for source, drain and the gate. Ti/Pd/Au probing contacts were then deposited and lifted off. A 3D schematic diagram of such fabricated nano-pillar device is shown in Fig. 3.12.

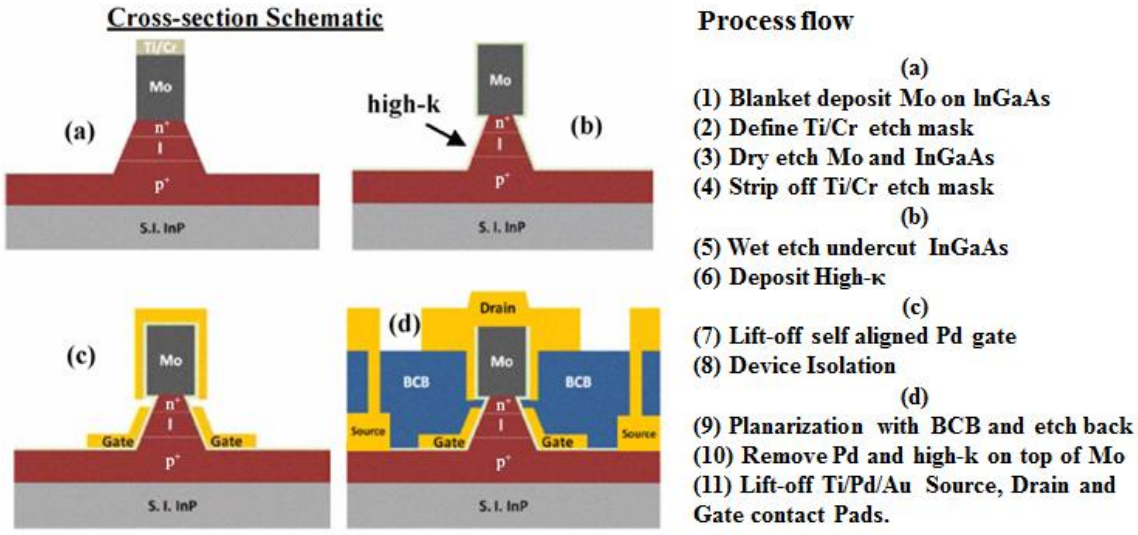


**Figure 3.11** Cross-section schematics of the TFET device following by key process steps. The fabrication process flow is shown on the right. [17] Used with permission of Nanotechnology Reviews.

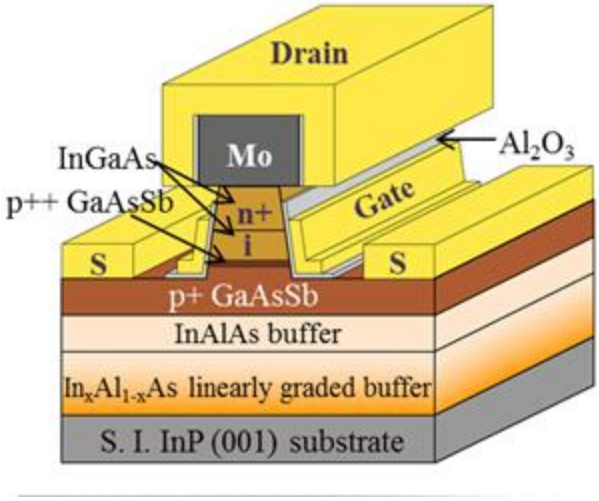


**Figure 3.12** Schematic of self-aligned gate nano-pillar staggered gap TFET device. [11] Used with permission of Nanotechnology Reviews.

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# Chapter 4 MBE growth, strain relaxation properties and high-κ dielectric integration of mixed anion $GaAs_ySb_{1-y}$ metamorphic materials

As discussed in ***Chapter 2***, the mixed As/Sb based material system ($GaAs_ySb_{1-y}/In_xGa_{1-x}As$) is promising for TFET applications as they allow a wide range of bandgap energies and staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at the source/channel heterointerface can be tailed by carefully controlling the compositions of the mixed As/Sb material system while keeping this material system internally lattice matched. The utilization of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterostructures for TFET applications demands high quality $GaAs_ySb_{1-y}$ materials with various Sb compositions. Thermodynamics predicts that an immiscibility zone exists for $GaAs_ySb_{1-y}$ alloys with Sb composition between 0.25 to 0.7 [1-3], which will lead to spinodal decomposition of the GaAsSb alloy in this composition range. The spinodal decomposition is expected to be suppressed to a large extent using thermodynamically nonequilibrium epitaxy technique [1], such as molecular beam epitaxy (MBE). However, the MBE growth of the mixed anion (III-V-V') alloys is more challenging to control alloy compositions compared with the mixed cation (III-III'-V) counterparts due to the strong competition between the incorporations of anions, which leads to different sticking coefficients of V and V' species [4-6]. Unlike mixed cation ternaries where the alloy composition is determined by the flux ratios of the group III elements over a wide range of temperature, in a mixed anion ternary the composition also depends on the growth temperature [4-6]. Moreover, it has been reported that the As/Sb ratio [6] and Ga flux [6] can also influence the alloy composition during MBE growth, which bring in more complexity. On the other hand,

realizing energy-efficient complementary logic circuits requires the development of a high-performance p-type TFET within the same material system. In order to keep the staggered band alignment at the source/channel interface, $GaAs_ySb_{1-y}$ will be used as the channel material in p-type TFET structures based on the band alignment between $GaAs_ySb_{1-y}$ and $In_xGa_{1-x}As$. A major challenge of using $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ material system for p-type TFET application is the integration of high-κ gate dielectric with acceptably low interface traps and high band offset values [7]. A few studies have reported on the integration of high-κ dielectrics on GaSb with focus on the lower part of the bandgap between the midgap and the valence band, whereas the study of high-κ gate dielectric on mixed As/Sb based material system with useable Sb composition (>50%) and different high-κ materials have not been addressed [8-10].

In this chapter, mixed anion $GaAs_ySb_{1-y}$ materials with a wide range of Sb composition (15% ~ 62%) were grown by MBE. The influence of different growth parameters, such as V/III ratio, Sb flux, growth temperature, *etc.*, on the alloy composition was systemically investigated. Three different high-κ gate dielectric, *i. e.*, $Al_2O_3$, $HfO_2$, $Ta_2O_5$, were integrated on $GaAs_{0.38}Sb_{0.62}$ material by atomic layer deposition (ALD). The band alignment of these different high-κ gate dielectric materials on $GaAs_{0.38}Sb_{0.62}$ was investigated by x-ray photoelectron spectroscopy (XPS). The comprehensive investigation of the influence of different growth parameters on Sb composition during MBE growth and the knowledge of band alignment of different high-κ gate dielectric on $GaAs_{0.38}Sb_{0.62}$ will facilitate the further material growth and device fabrication of both n-type and p-type TFETs using mixed As/Sb material system.

## 4.1 MBE growth $GaAs_ySb_{1-y}$ metamorphic materials

All the samples studied in this chapter were grown using solid source MBE system on semi-insulating GaAs (001) substrates. The Sb flux was provided by an effusion cell. A Valved

Cracker was used to provide the As flux with the cracking zone held at 900$^{o}$C to ensure an $As_2$ rich flux. Oxide desorption was performed under $As_2$ flux at ~680$^{o}$C monitored by reflected high energy electron diffraction (RHEED). The Ga beam-equivalent pressure was kept as 2.76e-7 torr for each run, corresponding to a growth rate of ~0.5μm/h based on the earlier performed calibration by RHEED oscillation. For each sample, several layers of $GaAs_ySb_{1-y}$ materials were deposited using different Sb/Ga, As/Ga ratio and different growth temperature. The thickness of each layer was kept to be 750nm. The growth parameters for different samples and different $GaAs_ySb_{1-y}$ layers were summarized in Table 4.1. All temperature referred in this chapter stands for the thermocouple temperature. The alloy composition and strain relaxation properties of each $GaAs_ySb_{1-y}$ from different samples were characterized by high-resolution x-ray diffraction (XRD). Both XRD rocking curve (ω/2θ scan) and reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 as x-ray source.

Following the MBE growth of the GaAsSb structures, 1.5nm and 10nm $Al_2O_3$, HfO2 and $Ta_2O_5$ were independently deposited by ALD in a Cambridge NanoTech system using $H_2O$ as the oxygen source and the following precursors: Tantalum(V) ethoxide (99.99%, Strem Chemicals); Tetrakis(dimethylamino)hafnium (99.99%, Strem Chemicals); and, Trimethlyaluminum (98%, Strem Chemicals). Prior to being loaded into the ALD reactor chamber, all GaAsSb structures were removed of native oxides in 1:10 dilute hydrochloric acid (36.5 w-%, J.T. Baker). During oxide deposition, each GaAsSb/GaAs substrate was heated to a constant temperature dependent on the growth kinetics of the oxide being deposited. For the $Ta_2O_5$ and $Al_2O_3$ depositions, the GaAsSb/GaAs substrate temperature was held at a constant 250 ℃, while for the $HfO_2$ thin-film depositions, the GaAsSb/GaAs substrate temperature was held at a constant 200 ℃. To ensure that the precursor flux was sufficient to saturate the

substrate during each growth cycle, the Ta and Hf precursors were heated to 145 ℃ and 75 ℃, respectively, while the Al precursor required no heating during deposition. Under the aforementioned conditions, the growth rates for each $Ta_2O_5$, $HfO_2$ and $Al_2O_3$ oxide film were, in order, 0.61 Å/cycle, 1.01 Å/cycle and 1.05 Å/cycle. Table 4.2 summarizes the deposition conditions as well as the corresponding number of growth cycles required to deposit each 1.5 nm and 10 nm thick oxide.

**Table 4.1** Summary of different growth parameters and structural properties for $GaAs_ySb_{1-y}$.

| Run NO. | Growth Parameters | | | Structural properties | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| | Sb/Ga | As/Ga | Growth Temperature (°C) | Sb% | Lattice constants (Å) [a] | | | Relaxation (%) | FWHM (aresec) | *rms* [b] (nm) |
| | | | | | c | a | $a_l$ | | | |
| A | 1 | 15 | 450 | 15 | 5.72 | 5.71 | 5.71 | 93% | 188.13 | 1.31 |
| | 1 | 10 | 450 | 19 | 5.74 | 5.73 | 5.73 | 93% | 90.50 | |
| | 1 | 5 | 450 | 21 | 5.75 | 5.73 | 5.74 | 85% | 70.45 | |
| B | 2 | 15 | 450 | 32 | 5.79 | 5.79 | 5.79 | 97% | 263.52 | 1.18 |
| | 2 | 10 | 450 | 40 | 5.83 | 5.82 | 5.83 | 97% | 184.86 | |
| | 2 | 10 | 410 | 44 | 5.85 | 5.84 | 5.84 | 97% | 132.66 | |
| C | 3 | 15 | 450 | 36 | 5.82 | 5.79 | 5.80 | 92% | 377.60 | 1.85 |
| | 3 | 10 | 450 | 42 | 5.85 | 5.81 | 5.83 | 91% | 744.33 | |
| | 3 | 10 | 410 | 46 | 5.87 | 5.83 | 5.85 | 91% | 104.25 | |
| D [c] | 3.58 | 10 | 410 | 49 | 5.88 | 5.85 | 5.86 | 93% | 384.58 | 1.73 |
| | 3.58 | 10 | 400 | | | | | | | |
| | 3.58 | 10 | 390 | | | | | | | |
| | 3.58 | 10 | 375 | 51 | 5.89 | 5.85 | 5.87 | 91% | 729.46 | |
| E | 4.31 | 15 | 450 | 41 | 5.84 | 5.82 | 5.83 | 94% | 443.23 | 1.40 |
| | 4.31 | 10 | 450 | 52 | 5.88 | 5.87 | 5.87 | 96% | 349.20 | |
| | 4.31 | 10 | 410 | 57 | 5.91 | 5.88 | 5.90 | 95% | 230.94 | |
| F | 6.16 | 15 | 450 | 44 | 5.85 | 5.84 | 5.84 | 97% | 479.98 | 1.28 |
| | 6.16 | 10 | 450 | 59 | 5.91 | 5.91 | 5.91 | 99% | 277.92 | |
| | 6.16 | 10 | 410 | 62 | 5.93 | 5.91 | 5.92 | 97% | 283.71 | |

[a] *c* is the out-of-plane lattice constant, *a* is the in-plane constant and $a_l$ is the relaxed lattice constant.
[b] The surface roughness is taken from the top layer of each sample.
[c] The XRD peaks were merge together for the first three layers in sample D.

**Table 4.2** Summary of deposition conditions as well as corresponding number of growth cycles required to deposit each 1.5 nm and 10 nm thick oxide.

| Materials | GaAsSb/GaAs Substrate Temperature (℃) | Precursor Temperature (℃) | Growth Rate (Å/cycle) | Growth Cycles ($t_{ox}$ ≈ 1.5 nm) | Growth Cycles ($t_{ox}$ ≈ 10 nm) |
|---|---|---|---|---|---|
| $Ta_2O_5$ | 250 | 160 | 0.61 | 25 | 165 |
| $HfO_2$ | 200 | 75 | 1.01 | 15 | 100 |
| $Al_2O_3$ | 250 | 25 | 1.05 | 15 | 95 |

## 4.2 Strain relaxation properties of $GaAs_ySb_{1-y}$ metamorphic structures

The symmetric (004) XRD rocking curves of structures A-F are shown in Figure 4.1 with the measured Sb compositions labeled to each layer. It can be seen from Figure 4.1 that with different As/Ga ratio, Sb/Ga ratio and growth temperature, the Sb composition can be modulated in a wide range from 15% to 62%. In TFET applications, $GaAs_ySb_{1-y}$ materials with high Sb composition (>50%) is desirable to reduce the tunneling barrier from the source to the channel. The increase of Sb composition also reduces the bandgap energy of the $GaAs_ySb_{1-y}$ material, which will also contribute to increase the tunneling current. The detailed strain relaxation states of each $GaAs_ySb_{1-y}$ layer within each sample were analyzed from symmetric (004) and asymmetric (115) RSMs. Figures 4.2 (a) and (b) show the symmetric (004) and asymmetric (115) RSMs from each structure, respectively. Distinct reciprocal lattice points (RLPs) were found in RSMs of each structure, corresponding to $GaAs_ySb_{1-y}$ material with different Sb compositions. From RSMs, the lattice constant in the out-of-plane, *c* (from symmetric 004 reflection), and the lattice constant in the growth plane, *a* (from the asymmetric 115 reflection), were determined. The relaxed lattice constant $a_r$ and strain relaxation values were also extracted from RSMs using the methods introduced in ***Chapter 3.2.1***. Table 4.1 summarized the in-plane and out-of-plane lattice constants, relaxed lattice constants and alloy composition in each layer of

different structures. Using the extracted alloy compositions in Table 4.1, it can be seen that the Sb composition has a direct dependence on the growth temperature, Sb/Ga and As/Ga ratio. Firstly, Sb composition increases with the reduction of growth temperature. The changing trend of Sb composition with temperature is reported in a fairly linear manner for both high and low Sb content by other researchers [5, 11]. This behavior has been attributed to an As/Sb exchange reaction that increases with increased temperature [5]. Secondly, the Sb composition increases at higher Sb/Ga ratio as expected, but is appears to be a nonlinear relationship. By comparing the first layer of sample A and B, C and F, it can be found that at a set growth temperature (450$^{o}$C) and set As/Ga ratio (15), the Sb composition doubled from 15% to 32% between sample A and B by doubling the Sb/Ga ratio from 1 to 2, however, the Sb composition only increased by 8% from 36% to 44% between sample C and F by doubling Sb/Ga ratio from 3 to 6.16. This behavior also reported by Wu *et al.* [12], where the Sb content at a fixed growth temperature was found to be very sensitive to change in Sb flux for low Sb flux while being less sensitive for higher fluxes and contents. Thirdly, the reduction of As/Ga ratio at fixed Sb/Ga ratio and set growth temperature also result in the increase of Sb content as expected. This is also due to the competition of As and Sb atoms at the surface. The increase of Sb composition caused by the reduction of As/Ga ratio is more sensitive at high Sb flux due to the much higher incorporation efficiency of Sb than As [4]. Furthermore, other researchers also reported that the Sb mole fraction increases with increasing of Ga flux, when the As and Sb fluxes and the growth temperature are kept constant [4]. This implies that the surface dissociation of Sb-containing species is more effective in the presence of larger concentration of Ga on the growing surface. These results agree with prediction made by nonequilibrium thermodynamic analysis of III-V-V' compounds [13]. The surface root-mean-square (*rms*) roughness of each sample is characterized

by atomic force microscopy (AFM) in a contact mode using 20μm × 20μm scan. All samples show a smooth surface with a low *rms* roughness ranging from 1.18nm (sample B) to 1.85nm (sample D). The smooth surface is attributed to the surfactant effect of Sb. The 20μm × 20μm and 1μm × 2μm AFM micrograph of sample F are shown in Fig. 4.3 (a) and (b) respectively. Mounds with a dimension of several hundred nanometers appear on the $GaAs_{0.38}Sb_{0.62}$ surface corresponding to a saturation region of strain relaxation [14]. The strain relaxation of $GaAs_ySb_{1-y}$ on GaAs goes through several regions, which correlated to the surface morphology and the nucleation of dislocations. The fast relaxation regime is characterized by the nucleation of small islands and an abrupt increase in the number of edge dislocations, while the saturation regime is distinguished by coalesce of small islands [14].

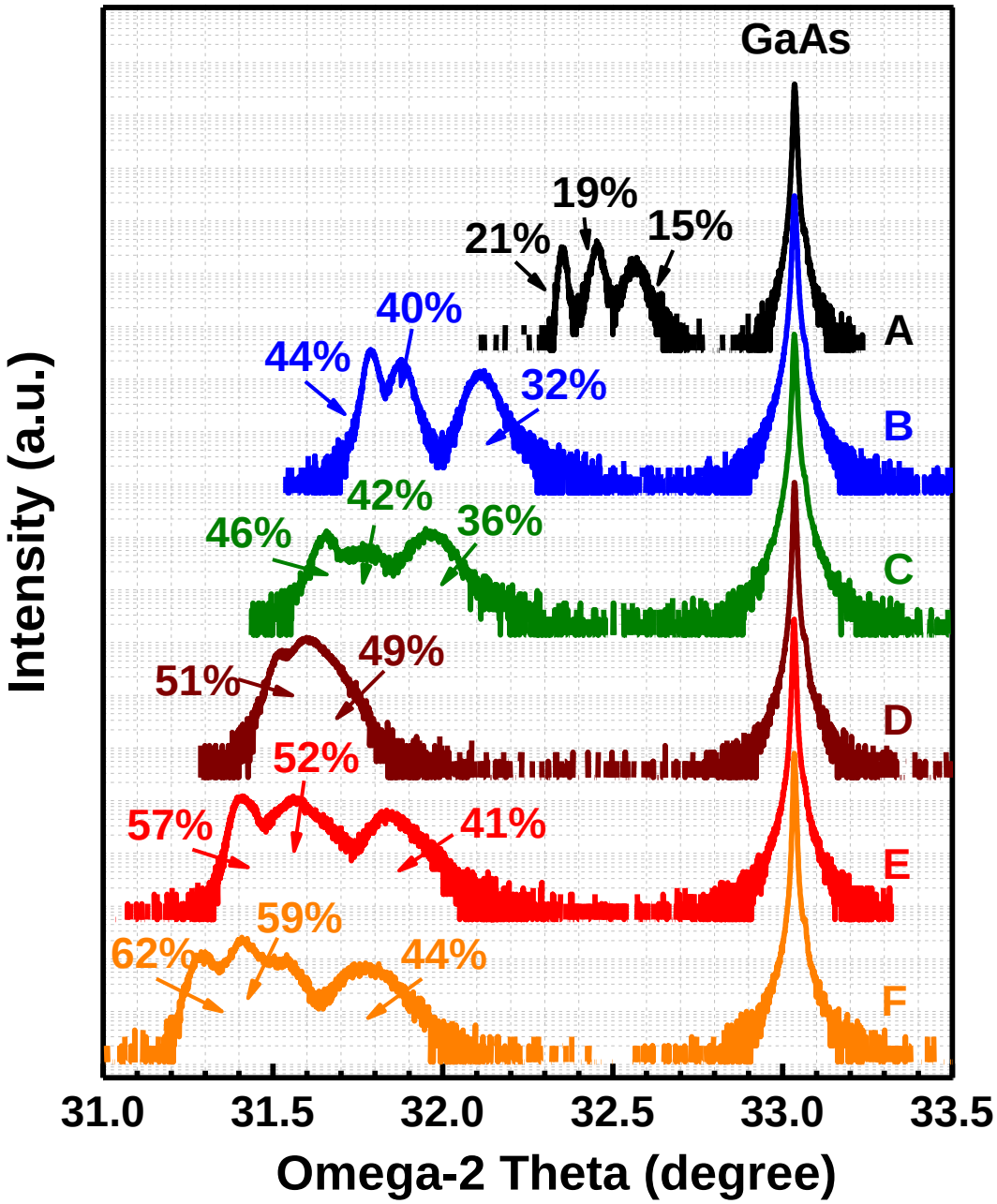


**Figure 4.1** Symmetric (004) XRD rocking curves of structures A-F. The measured Sb composition of each layer in each sample was also labeled to the corresponding peak.

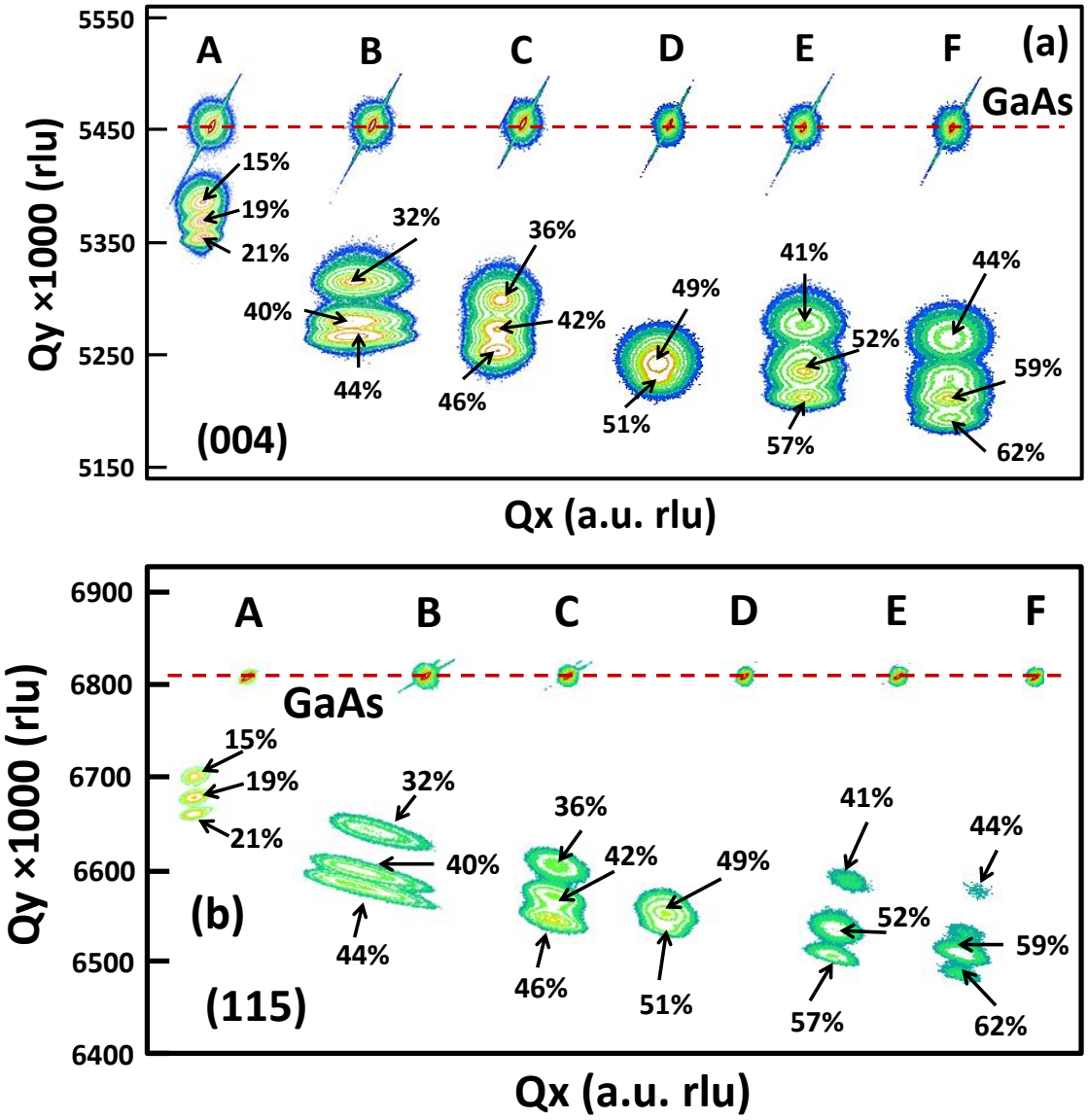


**Figure 4.2** (a) Symmetric (004) and (b) asymmetric (115) RSMs of samples A-F. The measured Sb composition was labeled to each reciprocal lattice points.

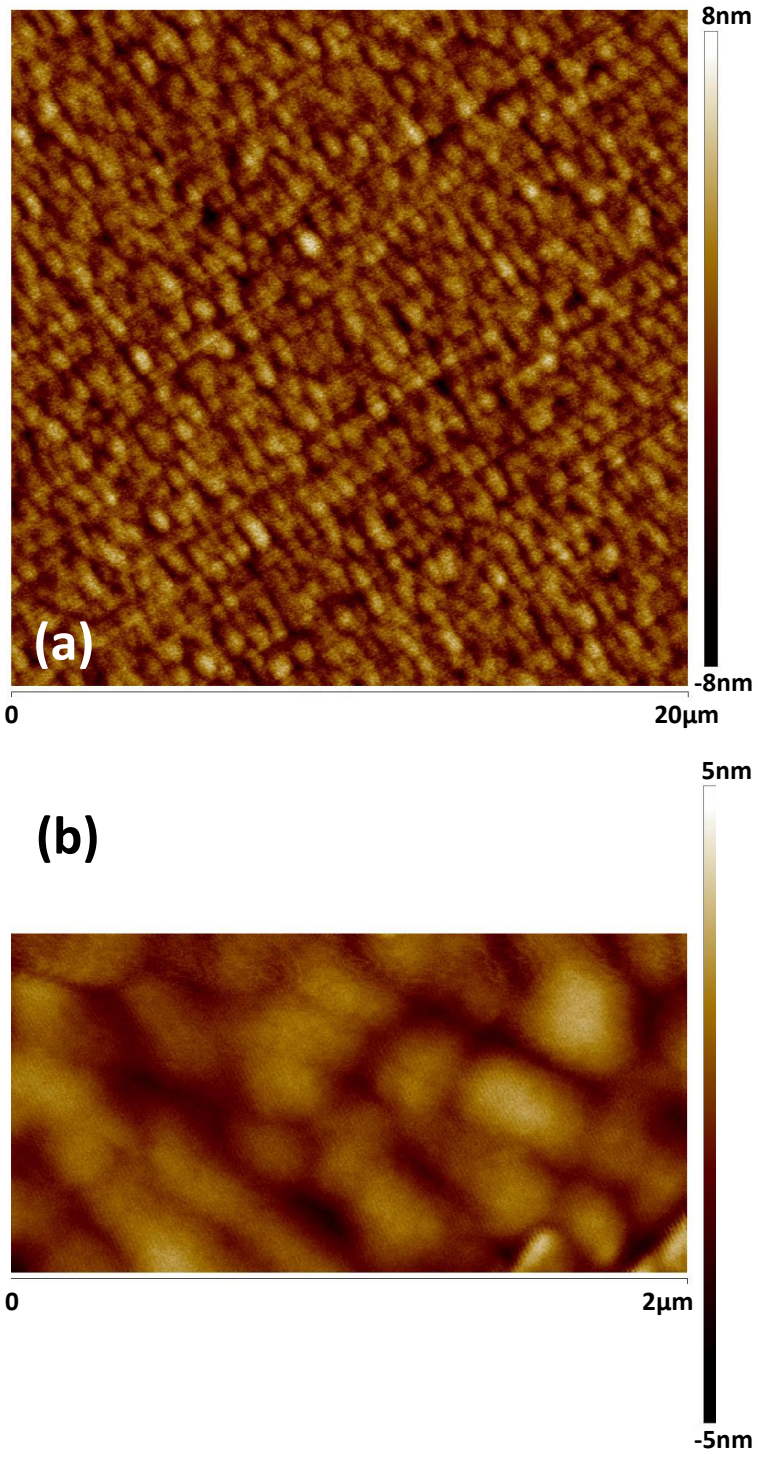


**Figure 4.3** AFM micrograph of sample F ($GaAs_{0.38}Sb_{0.62}$) from (a) 20µm × 20µm scan and (b) 1µm × 2µm scan. The *rms* roughness is determined to be 1.28nm from 20µm × 20µm scan. Mounds with a dimension of several hundred nanometers appear on 1µm × 2µm scan corresponding to a saturation region of strain relaxation.

## 4.3 High-κ dielectric integration and band offset analysis on $GaAs_{0.38}Sb_{0.62}$ material

According to the design considerations for mixed As/Sb heterostructure TFETs as discussed in ***Chapter 2***, high Sb composition (>50%) in $GaAs_ySb_{1-y}$ material is needed to reduce the tunneling barrier. In the meantime, high In composition is also needed inside of $In_xGa_{1-x}As$ material to keep these two materials to be internally lattice matched. For p-type TFET applications, in order to obtain the staggered band alignment, $n^{++}$ InGaAs material is used as source and intrinsic GaAsSb material is used as channel [15-17]. In this respect, the gate dielectric will be integrated on GaAsSb material with high Sb composition. In fact, one of the most important considerations of selecting gate dielectric materials on GaAsSb regarding the valence band and conduction band offset values, which should be larger than 1eV to block the carrier injection from the semiconductor to the insulator [18]. In respect of these considerations, the integration of different gate dielectric on GaAsSb channel as well as understanding of the interfacial properties are vital for advancing further development of TFET devices. Besides, the research of different gate dielectric materials on GaAsSb will provide more information for future studies of utilizing GaAsSb material for multifunctional device applications. $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ are three commonly used high-κ gate dielectric materials for advanced field-effect-transistor (FET) applications due to the high dielectric constant (~9 for $Al_2O_3$, ~25 for $HfO_2$ and 20~25 for amorphous $Ta_2O_5$ and as high as 52 for crystalline $Ta_2O_5$), relatively high band gap energies and high thermal and chemical stability. In this section, detailed XPS analysis was conducted to determine the band offset values of $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ material. The valence band offset (VBO) values were measured using Kraut's method [19]. The

conduction band offset (CBO) values were calculated using the measured VBO values and the band gap energies of $GaAs_{0.38}Sb_{0.62}$, $Al_2O_3$, $HfO_2$ and $Ta_2O_5$, respectively.

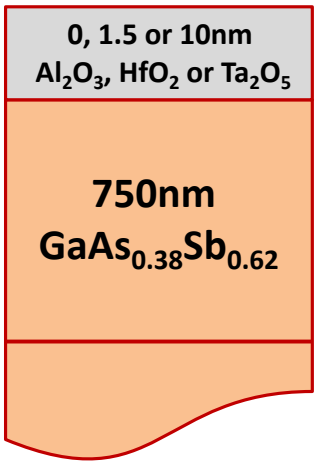


**Figure 4.4** Schematic diagram of high-κ dielectric material ($Al_2O_3$, $HfO_2$ and $Ta_2O_5$) integrated on $GaAs_{0.38}Sb_{0.62}$ for band alignment measurements.

**Table 4.3** Summary of peak position of core level and valence band maximum (VBM) from bulk $GaAs_{0.38}Sb_{0.62}$, $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$.

| **Structures** | **Peak assignment** | **Binding energy (eV)** | **Band offset** * |
|---|---|---|---|
| 750nm $GaAs_{0.38}Sb_{0.62}$ | Sb4d5/2 | 31.70 | |
| | VBM | -0.28 | |
| 1.5nm $Al_2O_3$ on $GaAs_{0.38}Sb_{0.62}$ | Al2p | 74.46 | **$\Delta E_C$ = 2.71eV** **$\Delta E_V$ = 3.09eV** |
| | Sb4d5/2 | 31.70 | |
| 10nm $Al_2O_3$ on $GaAs_{0.38}Sb_{0.62}$ | Al2p | 73.00 | |
| | VBM | 1.35 | |
| 1.5nm $HfO_2$ on $GaAs_{0.38}Sb_{0.62}$ | Sb4d5/2 | 31.80 | **$\Delta E_C$ = 2.09eV** **$\Delta E_V$ = 2.73eV** |
| | Hf4f7/2 | 16.80 | |
| 10nm $HfO_2$ on $GaAs_{0.38}Sb_{0.62}$ | Hf4f7/2 | 16.55 | |
| | VBM | 2.30 | |
| 1.5nm $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ | Sb4d5/2 | 31.70 | **$\Delta E_C$ = 0.71eV** **$\Delta E_V$ = 2.99eV** |
| | Ta4f7/2 | 26.14 | |
| 10nm $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ | Ta4f7/2 | 26.05 | |
| | VBM | 2.62 | |

* $\Delta E_C$ is calculated using the measured value of $\Delta E_V$ and the band gap energy of $GaAs_{0.38}Sb_{0.62}$, $Al_2O_3$, $HfO_2$ and $Ta_2O_5$, respectively.

The band alignment of $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ were investigated using the PHI Quantera SXM XPS system with a monochromated Al-Kα (energy of 1486.7 eV) x-ray source. The VBO values between $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$) and $GaAs_{0.38}Sb_{0.62}$ were determined by measuring the binding energy from shallow core levels (CLs) of Sb4d, Al2p, Hf4f, Ta4f and corresponding valence band maxima (VBM) from each material, respectively. The schematic diagram of the structures used in this study is shown in Fig. 4.4. As shown in Fig. 4.4, XPS spectra were collected from three samples of each high-κ gate oxide: (1) 1.5nm $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$)/750nm $GaAs_{0.38}Sb_{0.62}$ was used to measure the CL binding energy of Al (Hf or Ta) and Sb at the interface; (2) 10nm $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$)/750nm $GaAs_{0.38}Sb_{0.62}$ was used to measure the CL binding energy of Al (Hf or Ta) and VBM of $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$); (3) 750nm $GaAs_{0.38}Sb_{0.62}$ without the top gate oxide layer was used to measure the CL binding energy of Sb and VBM of $GaAs_{0.38}Sb_{0.62}$. Sample charging was occurred during XPS measurement and was a particular problem on the fully oxidized materials [18]. Compensation of the charging by an electron flood source was used in all measurements to minimize the binding energy shift. Besides, the measured CLs and VBM binding energy values were corrected by shifting C1s CL peak to 285.0eV. All XPS spectra were recorded using pass energy of 26eV and a step size of 0.025eV. Curve fitting was done by the CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background.

After collecting the binding energy information from each sample surface, the VBO value can be determined by Kraut's method [19]

$$\Delta E_V = \left(E_{CL}^{GaAsSb} - E_{VBM}^{GaAsSb}\right) - \left(E_{CL}^{Oxide} - E_{VBM}^{Oxide}\right) + \Delta E_{CL}(i), \tag{4.1}$$

where $E_{CL}^{GaAsSb}$ and $E_{CL}^{Oxide}$ are shallow CL binding energies of Sb4d and Al2p (Hf4f or Ta4f), respectively. $E_{VBM}^{GaAsSb}$ and $E_{VBM}^{Oxide}$ are the VBM of $GaAs_{0.38}Sb_{0.62}$ and $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$),

respectively. $E_{VBM}$ of each material was determined by linearly fitting the leading edge of valence band spectra to the base line [15-18]. $\Delta E_{CL}(i) = E_{CL}^{Oxide}(\mathrm{i}) - E_{CL}^{GaAsSb}(i)$ is the CL binding energy difference of Al2p (Hf4f or Ta4f) and Sb4d measured at the interface from 1.5nm $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$)/750nm $GaAs_{0.38}Sb_{0.62}$ of each structure. Once the VBO was obtained, the conduction band offset (CBO) can be estimated by [15-18]

$$\Delta E_C = E_G^{Oxide} - \Delta E_V - E_G^{GaAsSb}, \tag{4.2}$$

where $E_G^{Oxide}$ and $E_G^{GaAsSb}$ are the band gap energies of $Al_2O_3$ ($HfO_2$ or $Ta_2O_5$) and $GaAs_{0.38}Sb_{0.62}$, respectively. The band gap energy of $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ were found to be 6.50eV [20], 5.52eV [21] and 4.40eV [22]. The band gap energy of $GaAs_{0.38}Sb_{0.62}$ is determined to be 0.7eV by empirical model [23].

Figure 4.5(a) shows the Sb4d CL and $GaAs_{0.38}Sb_{0.62}$ VB spectra from 750nm $GaAs_{0.38}Sb_{0.62}$. Figure 4.5(b) shows Al2p CL and Sb4d CL spectra measured from 1.5nm $Al_2O_3$/750nm $GaAs_{0.38}Sb_{0.62}$ at the interface. Figure 4.5(c) shows Al2p CL and $Al_2O_3$ VB spectra from 10nm $Al_2O_3$/750nm $GaAs_{0.38}Sb_{0.62}$. The measured and fitted peak positions from each structure are summarized in Table 4.3. The results show that the value of $(E_{Al2p}^{Al2O3} - E_{VBM}^{Al2O3})$ is 71.65eV. The measured value of $\left(E_{Sb4d5/2}^{GaAsSb} - E_{VBM}^{GaAsSb}\right)$ is 31.98eV. The binding energy difference between the Al2p and the Sb4d5/2 states at the interface ($\Delta E_{CL}(i)$) was found to be 42.76eV. Using these results, the VBO of $GaAs_{0.38}Sb_{0.62}$ with respect to $Al_2O_3$ is determined to be 3.09 $\pm$ 0.05 eV. The uncertain value of 0.05eV is from the curve fitting process together with the scatter of VB curve during the fitting of VBM position. Similar measurements were also performed on $HfO_2$/$GaAs_{0.38}Sb_{0.62}$ and $Ta_2O_5$/$GaAs_{0.38}Sb_{0.62}$ structures. The CL and VB spectra from $HfO_2$/$GaAs_{0.38}Sb_{0.62}$ and $Ta_2O_5$/$GaAs_{0.38}Sb_{0.62}$ were shown in Figs. 4.6(a) – (b) and Figs. 4.7(a) –

(b), respectively. The peak positions from the measured and fitted results were summarized in Table 4.3. The VBO is 2.73 ± 0.05eV for $HfO_2/GaAs_{0.38}Sb_{0.62}$ and 2.99 ± 0.05 eV for $Ta_2O_5/GaAs_{0.38}Sb_{0.62}$. The CBO values of all three high-κ gate dielectrics on $GaAs_{0.38}Sb_{0.62}$ are estimated from Eq. 4.2 using bandgap energies of $Al_2O_3$, $HfO_2$, $Ta_2O_5$ and $GaAs_{0.38}Sb_{0.62}$ together with the measured VBO values. The CBO was calculated to be ~2.71eV for $Al_2O_3/GaAs_{0.38}Sb_{0.62}$, ~2.09eV for $HfO_2/GaAs_{0.38}Sb_{0.62}$ and ~0.71eV for $Ta_2O_5/GaAs_{0.38}Sb_{0.62}$, respectively. All calculated CBO values are summarized in Table 4.3.

Figure 4.8 shows the histogram of $\Delta E_V$ and $\Delta E_C$ distribution of $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ based on the results presented above. It can be seen from this figure that all these three high-κ gate dielectric provide more than 2eV VBO on $GaAs_{0.38}Sb_{0.62}$, which indicates that all these three high-κ gate dielectric materials can be integrated on $GaAs_{0.38}Sb_{0.62}$ for p-type FET applications especially for the utilization of TFET devices due to the distinct staggered band alignment of GaAsSb and InGaAs. For the conduction band alignment, both $Al_2O_3$ and $HfO_2$ can provide a CBO value higher than 2eV, suggesting that these two oxide materials can also be used on $GaAs_{0.38}Sb_{0.62}$ for n-type transport application. However, the CBO value of $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ is limited to be 0.71eV due to the low band gap energy of $Ta_2O_5$. As a result, additional interfacial dielectric layers should be integrated between $Ta_2O_5$ and $GaAs_{0.38}Sb_{0.62}$ in order to utilize $Ta_2O_5$ as part of gate stacks on $GaAs_{0.38}Sb_{0.62}$ for n-type FET applications. In addition, further investigations are needed to study the electrical properties of utilizing $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ as high-κ gate dielectric materials on $GaAs_{0.38}Sb_{0.62}$. The measured band offset values between $Al_2O_3$, $HfO_2$, $Ta_2O_5$ and $GaAs_{0.38}Sb_{0.62}$ will provide a promising reference for future design of mixed As/Sb TFETs as well as other multi-functional devices using $GaAs_{0.38}Sb_{0.62}$ as channel materials.

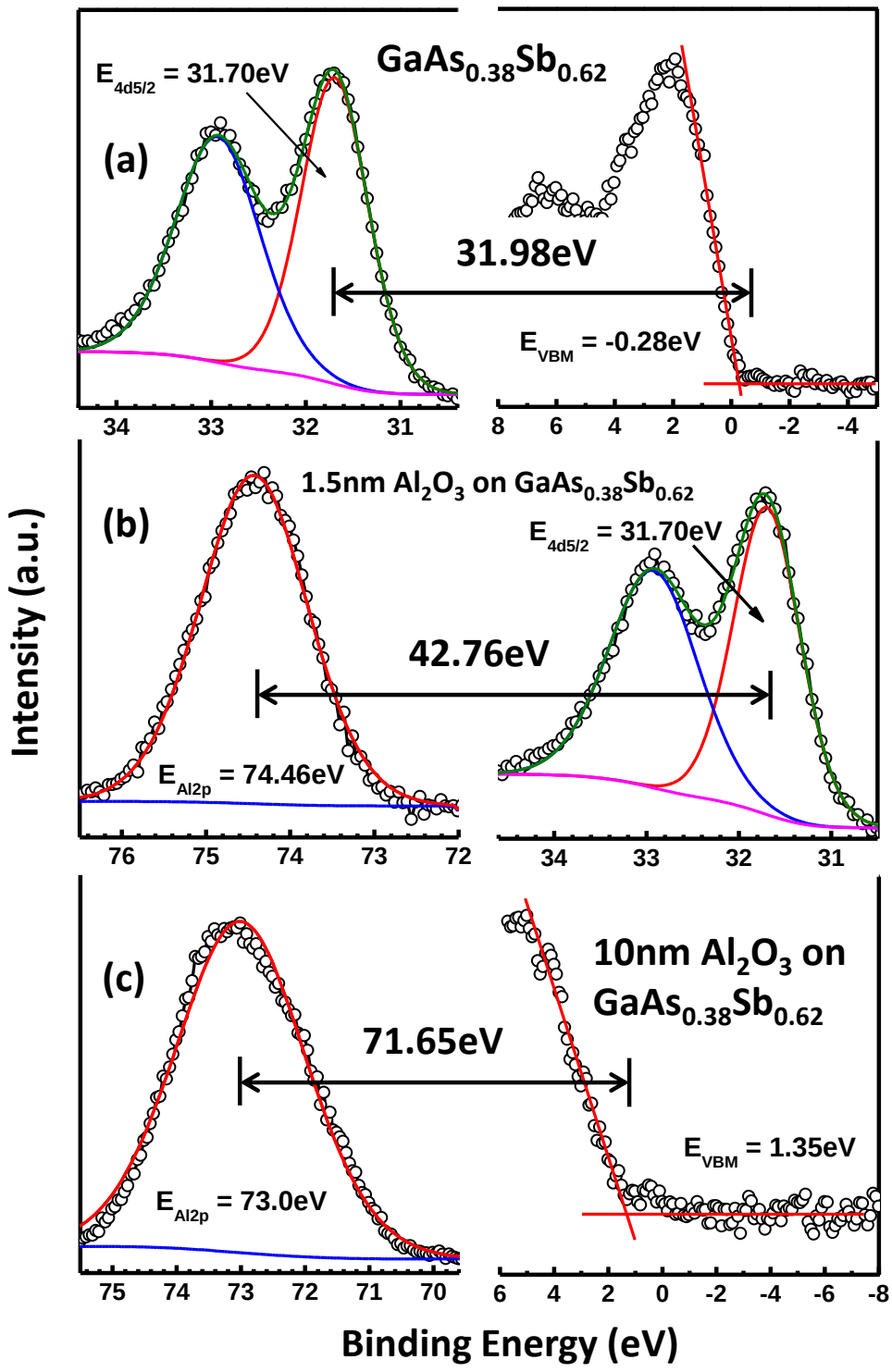


**Figure 4.5** XPS spectra of (a) Sb4d core level and valence band from bulk $GaAs_{0.38}Sb_{0.62}$; (b) Al2p and Sb4d core level from 1.5nm $Al_2O_3$ on bulk $GaAs_{0.38}Sb_{0.62}$; (c) Al2p core level and valence band from 10nm $Al_2O_3$ on bulk $GaAs_{0.38}Sb_{0.62}$. Core level spectra were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maximum is determined by linearly fitting the leading edge of valence band spectra to the base line.

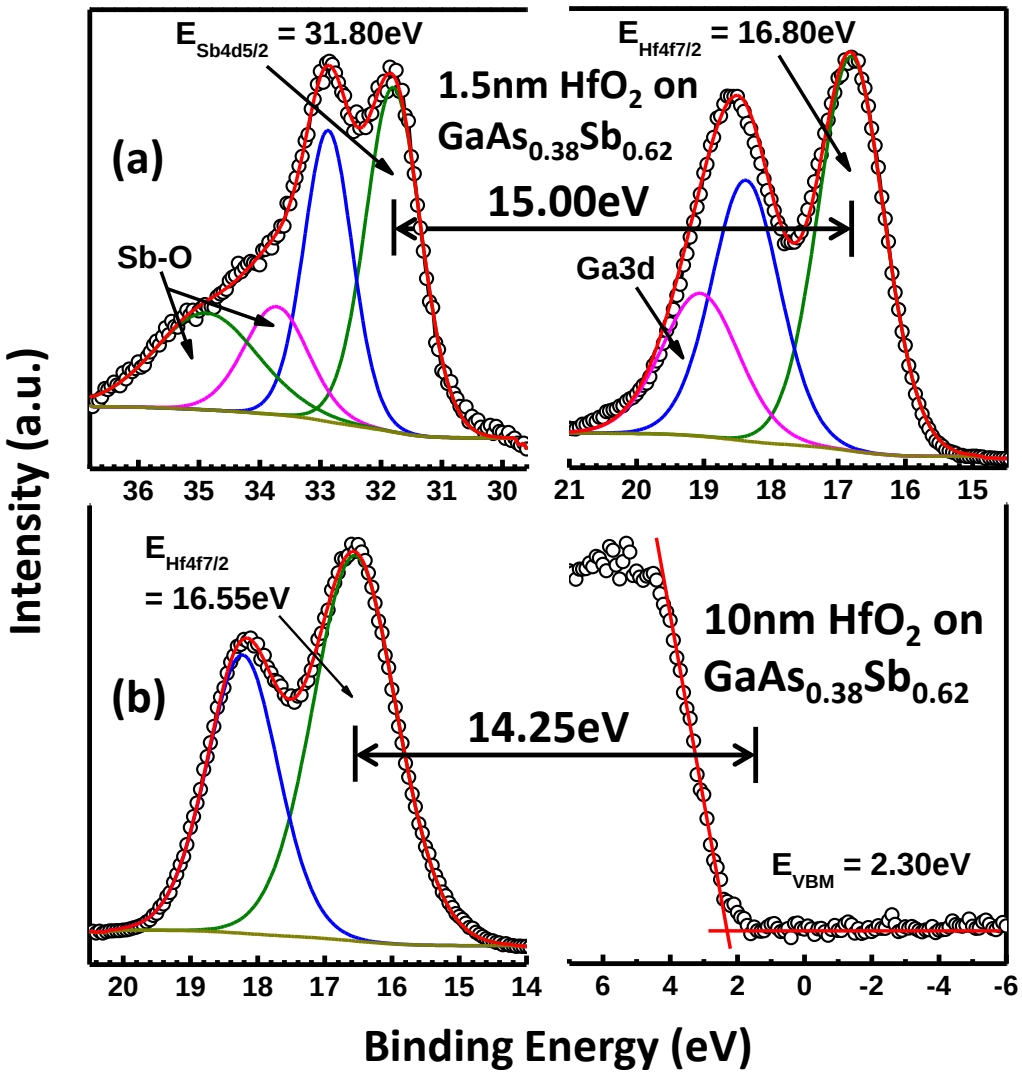


**Figure 4.6** XPS spectra of (a) Sb4d and Hf4f core level from 1.5nm $HfO_2$ on bulk $GaAs_{0.38}Sb_{0.62}$; (b) Hf4f core level and valence band from 10nm $HfO_2$ on bulk $GaAs_{0.38}Sb_{0.62}$. Core level spectra were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maximum is determined by linearly fitting the leading edge of valence band spectra to the base line.

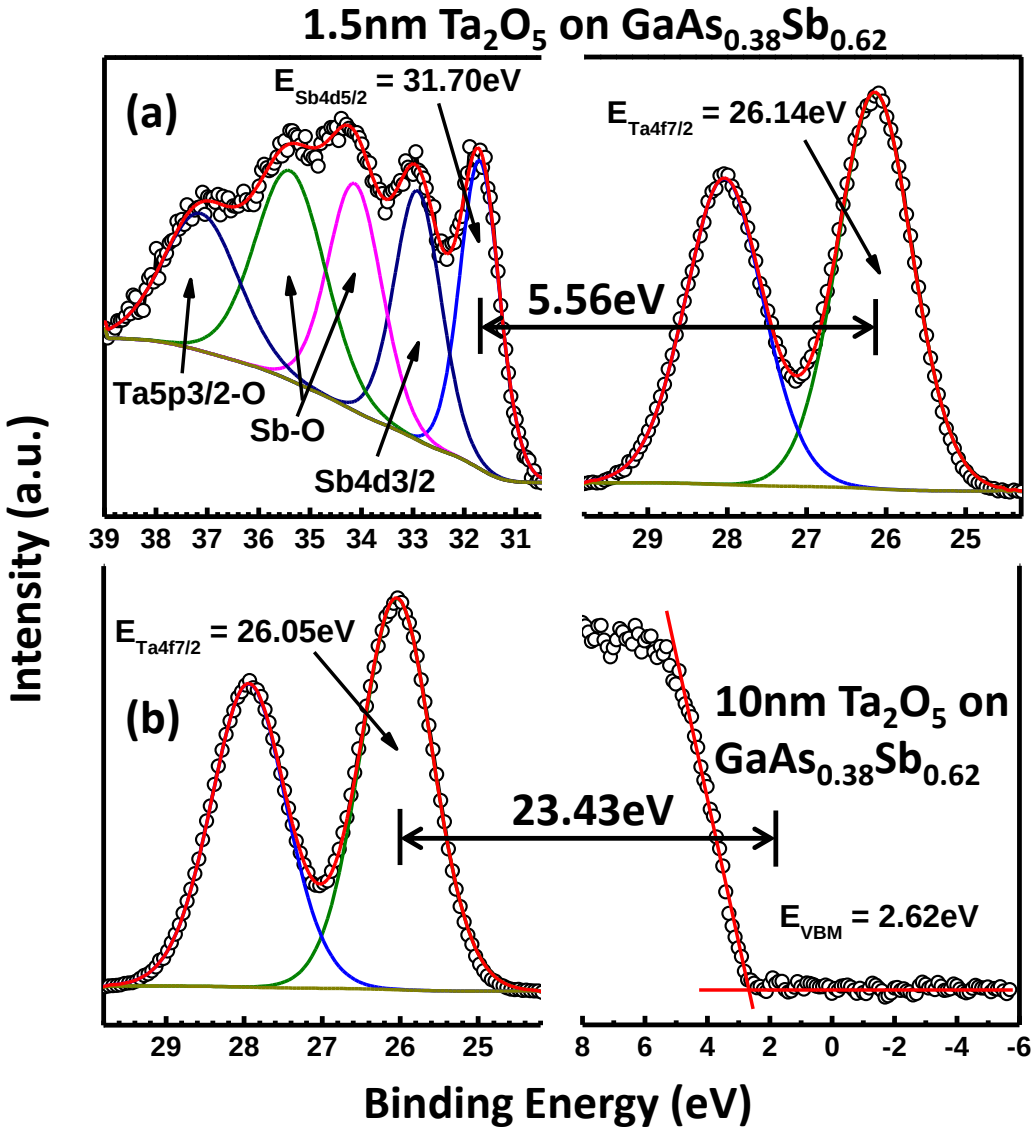


**Figure 4.7** XPS spectra of (a) Sb4d and Ta4f core level from 1.5nm $Ta_2O_5$ on bulk $GaAs_{0.38}Sb_{0.62}$; (b) Ta4f core level and valence band from 10nm $Ta_2O_5$ on bulk $GaAs_{0.38}Sb_{0.62}$. Core level spectra were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maximum is determined by linearly fitting the leading edge of valence band spectra to the base line.

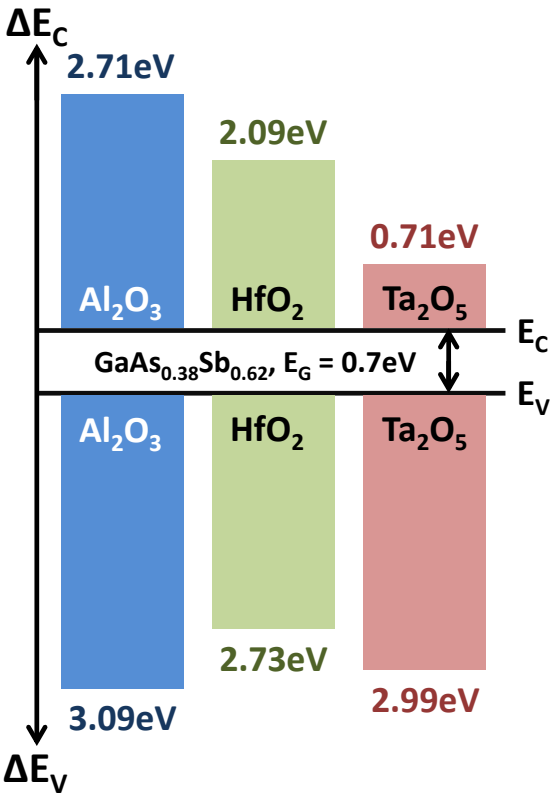


**Figure 4.8** Histogram of band offset distribution of $Al_2O_3$, $HfO_2$ and $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$.

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# Chapter 5 Mixed As/Sb n-type heterostructure TFETs

## 5.1 Composition and tunneling barrier height engineering

One of the key advantages of the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ material system is that it can modulate the $E_{beff}$ easily and accurately by carefully controlling the alloy compositions in $GaAs_ySb_{1-y}$ and $In_xGa_{1-x}As$ layers while keeping the material system to be internally lattice matched. Figure 5.1 shows the simulated changing trade (red dashed line) between $E_{beff}$ and In/Sb compositions. The inset demonstrated the band alignment of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ without bias and the definition of $E_{beff}$ is also shown in this figure. It can be seen from this figure that $E_{beff}$ is decreasing linearly with increasing In and Sb compositions. This $E_{beff}$ plays a significant role on the performance of a TFET device, which not only determines the ON-state tunneling rate but also sets the blocking barrier for the OFF-state leakage [1, 2]. The structural properties and device performances of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ n-type TFETs with different $E_{beff}$ were studies by changing alloy compositions in source and channel materials. The schematic diagram of these TFET layer structures with different alloy compositions are shown in Fig. 5.2 (a), (b) and (c), respectively. All these three structures were grown by solid source MBE on semi-insulating InP substrates. For the $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ structure, the active regions are lattice matched to the InP substrate, however, both the other two structures ($GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) are lattice mismatched to the InP substrate. In order to accommodate the lattice mismatch induced defects, linearly graded $In_xAl_{1-x}As$ buffers were used in these two structures. Table 5.1 summarized the structural information and device performances of these three structures. It can be seen from this table that the $I_{ON}$ of TFETs is increasing with scaling of $E_{beff}$. As a result, reducing $E_{beff}$ is one efficient way to boost the ON-state performance of TFETs. However, the scaling of $E_{beff}$ also introduces the risk of

increasing $I_{OFF}$. Firstly, both the direct BTBT and traps-assisted-tunneling (TAT) leakage are enhanced due to the reduced tunneling barrier height. Secondly, the bandgap energies of both $GaAs_ySb_{1-y}$ and $In_xGa_{1-x}As$ are decreasing with increasing Sb and In compositions, which will increase the SRH G-R leakage current. Besides, the increased Sb composition in the $GaAs_ySb_{1-y}$ layer also brings in the potential of atoms inter-diffusion at the heterointerface. As a result, proper interfacing engineering at $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterointerface is indispensable to achieve superior structural properties and device performances, which will be discussed in detail in the next section.

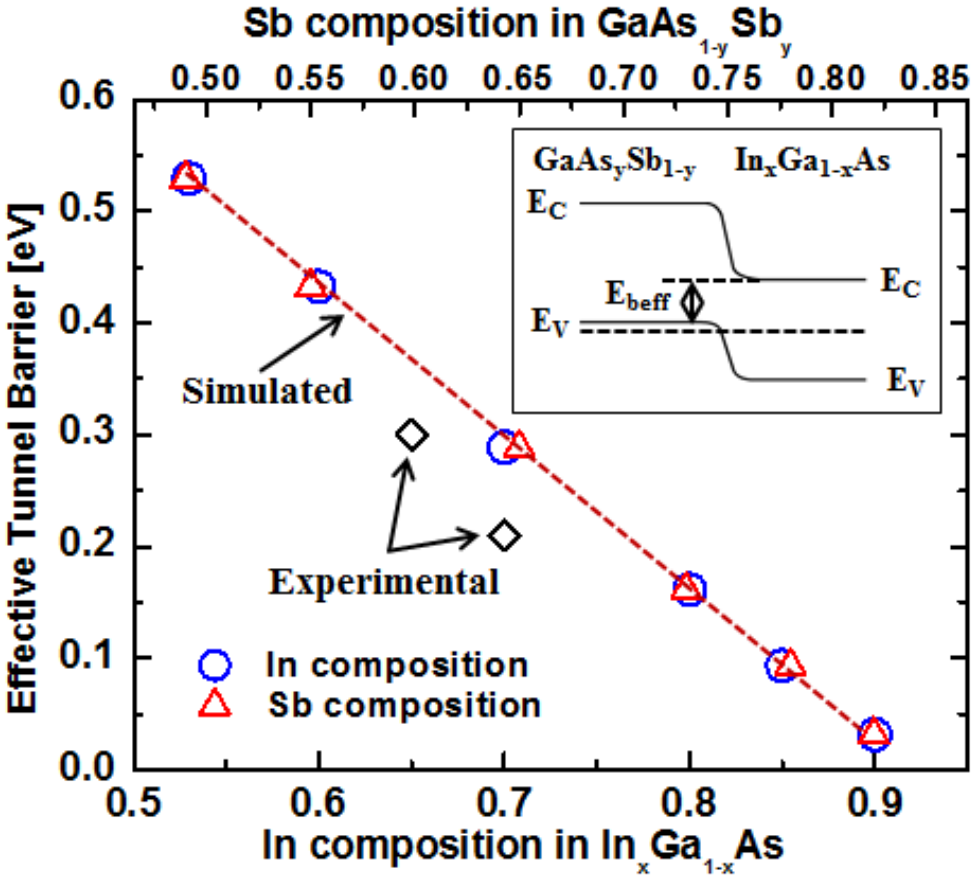


**Figure 5.1** Simulated changing trade (red dashed line) between effective tunneling barrier height ($E_{beff}$) and In/Sb compositions. The inset demonstrated the band alignment of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ without bias. The definition of $E_{beff}$ is also shown in this figure. The effective tunneling barrier height is decreasing linearly with increasing In and Sb compositions. The two squared points are experimental determined effective tunneling barrier height values, both

of which showed similar values as the simulated ones. The slightly smaller values may due to fixed positive charges at the interface.

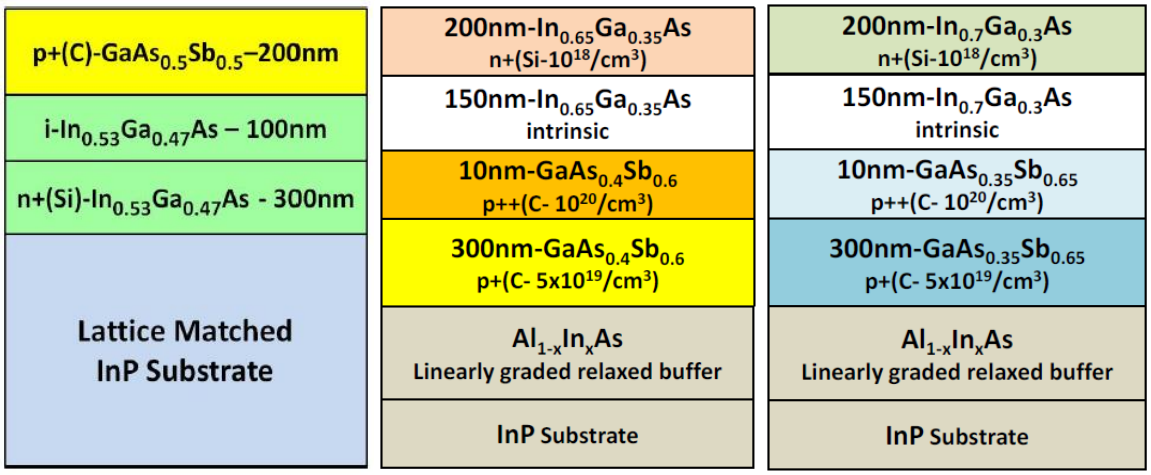


**Figure 5.2** Schematic layer diagram of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ staggered gap TFET structures with different alloy compositions. (a) $GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As$ structure shows an $E_{beff}$ of 0.5eV; (b) $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ structure shows an $E_{beff}$ of 0.31eV; (c) $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ structure shows an $E_{beff}$ of 0.25eV. All the $E_{beff}$ values are from simulation. [1, 3] Used with permission of Nanotechnology Reviews.

**Table 5.1** Summary of structural information and device performances of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ n-type staggered gap TFETs with different effective tunneling barrier height. [1, 3] Used with permission of Nanotechnology Reviews.

| | Source | Channel | Drain | $E_{beff}$ (eV) | $I_{ON}$ (μA/μm) |
|---|---|---|---|---|---|
| (a) | $p^{++}$-$GaAs_{0.5}Sb_{0.5}$ | i-$In_{0.53}Ga_{0.47}As$ | $n^{+}$-$In_{0.53}Ga_{0.47}As$ | 0.5 | 60 |
| (b) | $p^{++}$-$GaAs_{0.4}Sb_{0.6}$ | i-$In_{0.65}Ga_{0.35}As$ | $n^{+}$-$In_{0.65}Ga_{0.35}As$ | 0.31 | 78 |
| (c) | $p^{++}$-$GaAs_{0.35}Sb_{0.65}$ | i-$In_{0.7}Ga_{0.3}As$ | $n^{+}$-$In_{0.7}Ga_{0.3}As$ | 0.25 | 135 |

## 5.2 Heterointerface engineering

Engineering an abrupt source/channel heterointerface is critical for the type II staggered gap TFETs. However, the abrupt switching from mixed anion $GaAs_ySb_{1-y}$ to mixed cation $In_xGa_{1-x}As$ is a significant growth challenge due to different surface sticking coefficients of As and Sb at the specific growth temperature [2]. Furthermore, improper change of group-V fluxes at the source and channel interface will introduce intermixing between As and Sb that leads to uncontrolled layer composition at the heterointerface, which in turn produces high dislocation density in this region [2, 4]. These dislocations will introduce fixed charges [5] at the source/channel interface and thus, it will affect the band alignment as well as the value of $E_{beff}$. In practice, high Sb and In compositions are used in $GaAs_ySb_{1-y}$ and $In_xGa_{1-x}As$ layers, respectively, to reduce $E_{beff}$ and improve $I_{ON}$. The high Sb composition further increased the growth challenge for engineering an abrupt heterointerface with superior quality. When it comes to the specific layer structure as shown in Fig. 5.2 (c), two different surface terminations, i.e., (a) GaAs-like and (b) InAs-like can be realized when switching from Sb rich $GaAs_{0.35}Sb_{0.65}$ and to As rich $In_{0.7}Ga_{0.3}As$. For the former case, the GaAs-like interface was formed by the residual Ga atoms in the growth chamber together with the As overpressure. For the latter case, 1~2 monolayers (MLs) of In was added intentionally prior to the growth of $In_xGa_{1-x}As$ layer when the As flux was ramping up from 35% to 100% [1, 4]. If the GaAs-like interface formed at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface, the lattice mismatch between the top $In_{0.7}Ga_{0.3}As$ layer and the GaAs-like interface is as large as 5%, which gives high possibility to generate dislocations at the interface and inside of the $In_{0.7}Ga_{0.3}As$ top layer. In contrast, if the InAs-like interface formed, this mismatch is only limited to 2%, which provides better basis for the growth of the top $In_{0.7}Ga_{0.3}As$ layer. These two different interface engineering will influence both the structural

properties and the device performances of the mixed As/Sb staggered gap TFETs, which will be discussed separately in detail in the following sections of this chapter

## 5.3 Structural properties of mixed As/Sb staggered gap TFETs with different interface engineering

Different terminated interface atoms determines the lattice mismatch between the top layer and the interface layer [4], and different interface engineering can also introduce different amount of fixed positive charges [2, 4], both of which will influence the structural properties of these structures, including the strain relaxation properties, the surface morphologies and the dislocation densities.

### 5.3.1 Strain relaxation properties

The strain relaxation properties of epilayers can be characterized using x-ray diffraction. Out-of-plane lattice constant and in-plane lattice constant can be obtained from reciprocal space maps (RSMs) using symmetric scan and asymmetric scan, respectively. The relaxation states and residual strain of each epilayer can be calculated from the obtained lattice constants. The symmetry of the relaxation states of each epilayer can also be compared by aligning the incident x-ray beam along different directions. For the TFET structure as shown in Fig. 5.2 (c), the symmetric (004) and asymmetric (115) RSMs of the InAs-like interface structure are shown in Fig. 5.3 (a) and (b), respectively, with incident x-ray beam along $[1\bar{1}0]$ direction. Each layer was labeled to its corresponding reciprocal lattice point (RLP) based on wet chemical etching experiments [4]. As shown in Figs. 5.3 (a) and (b), four distinct RLP maxima were found in RSMs of InAs-like interface structure, corresponding to (1) the InP substrate, (2) $GaAs_{0.35}Sb_{0.65}$ source layer, (3) $In_{0.7}Ga_{0.3}As$ channel/drain layer, and (4) the 100nm $In_{0.7}Al_{0.3}As$ uppermost layer

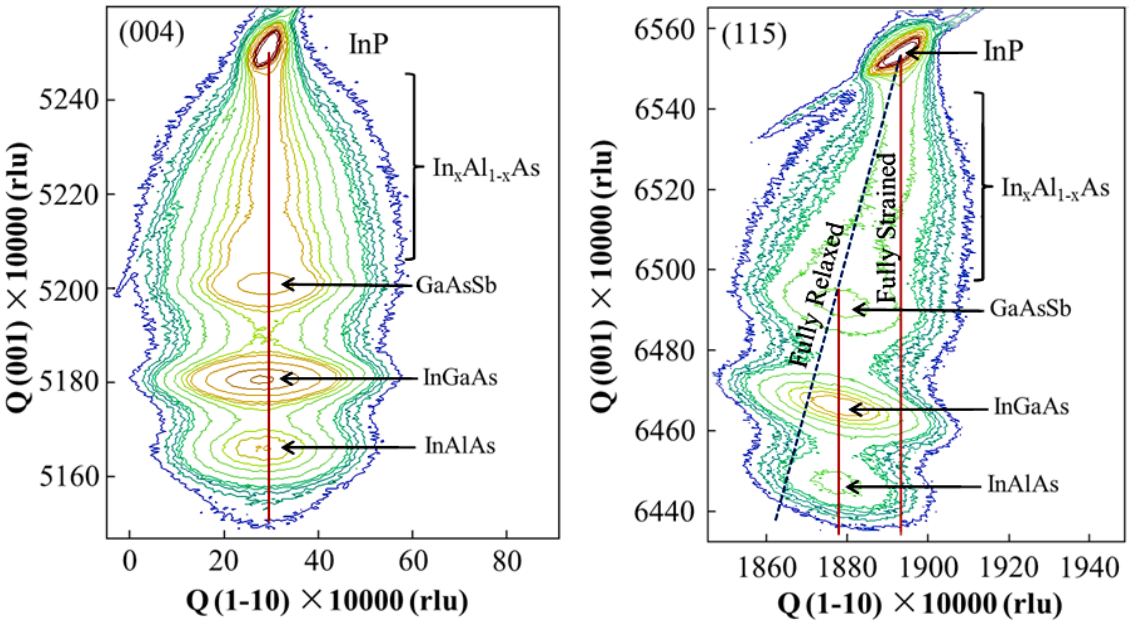


**Figure 5.3** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the InAs-like interface TFET with a layer structure as shown in Fig. 5.2 (c) using an incident x-ray beam along [$1\bar{1}0$] direction. Used with permission of Nanotechnology Reviews.

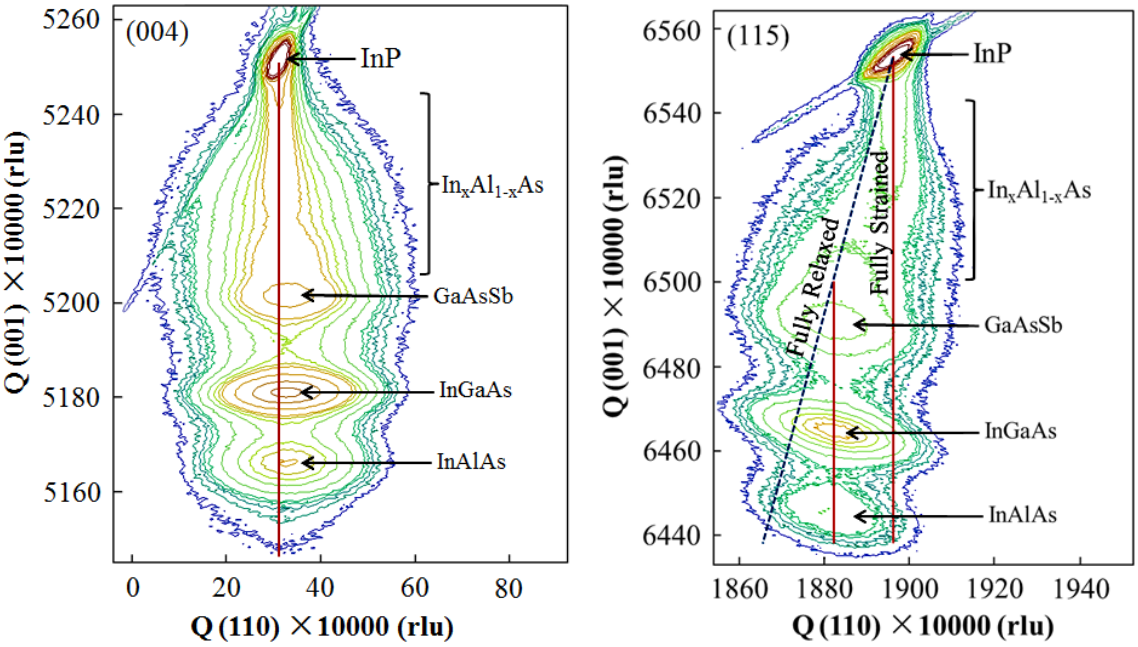


**Figure 5.4** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the InAs-like interface TFET with a layer structure as shown in Fig. 5.2 (c) using an incident x-ray beam along [110] direction. Used with permission of Nanotechnology Reviews.

of the linearly graded $In_xAl_{1-x}As$ buffer. Due to the residual strain within the $GaAs_{0.35}Sb_{0.65}$, $In_{0.7}Ga_{0.3}As$ and $In_{0.7}Al_{0.3}As$ buffer layers together with the heavily C doping caused lattice contraction in the $GaAs_{0.35}Sb_{0.65}$ layer, these three layers with the same designed lattice constant were shown in separate RLPs. Detailed strain relaxation analysis based on the symmetric (004) and asymmetric (115) RSMs shows symmetric strain relaxation states of the InAs-like structure along [110] and [$1\bar{1}0$] directions (the symmetric and asymmetric RSMs of InAs-like interface structure with incident x-ray beam along [110] direction are shown in Fig. 5.4 (a) and 5.4 (b)). Only ~ 4% strain relaxation in the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ active layers with respective to the $In_{0.7}Al_{0.3}As$ "virtual substrate" was obtained from InAs-like interface structure [4], suggesting the pseudomorphic nature of these two layers, indicating few dislocations formed within the active region of this structure.

Similarly, the symmetric (004) and asymmetric (115) RSMs of the GaAs-like interface structure are shown in Fig. 5.5 (a) and (b), respectively, with incident x-ray beam along [$1\bar{1}0$] direction. Different from the RSMs of InAs-like interface structure, one can find from Fig. 5.5 (a) and (b) that the contour of $In_{0.7}Ga_{0.3}As$ channel/drain layer was merged with $GaAs_{0.35}Sb_{0.65}$ source layer in RSM of GaAs-like interface structure. Calculation shows higher percentage of strain relaxation of 94% of these two layers with respect to InP substrate than that in the InAs-like interface structure, which is ~ 75% for $In_{0.7}Ga_{0.3}As$ layer and ~ 80% for $GaAs_{0.35}Sb_{0.65}$ layer, respectively [4]. The symmetric (004) and asymmetric (115) RSMs of the GaAs-like interface structure with incident x-ray beam along [110] direction are shown in Fig. 5.6 (a) and (b), respectively. Almost identical strain relaxation values are obtained from the RSMs with the incident X-ray along [110] direction, suggesting symmetric strain relaxation of this structure.

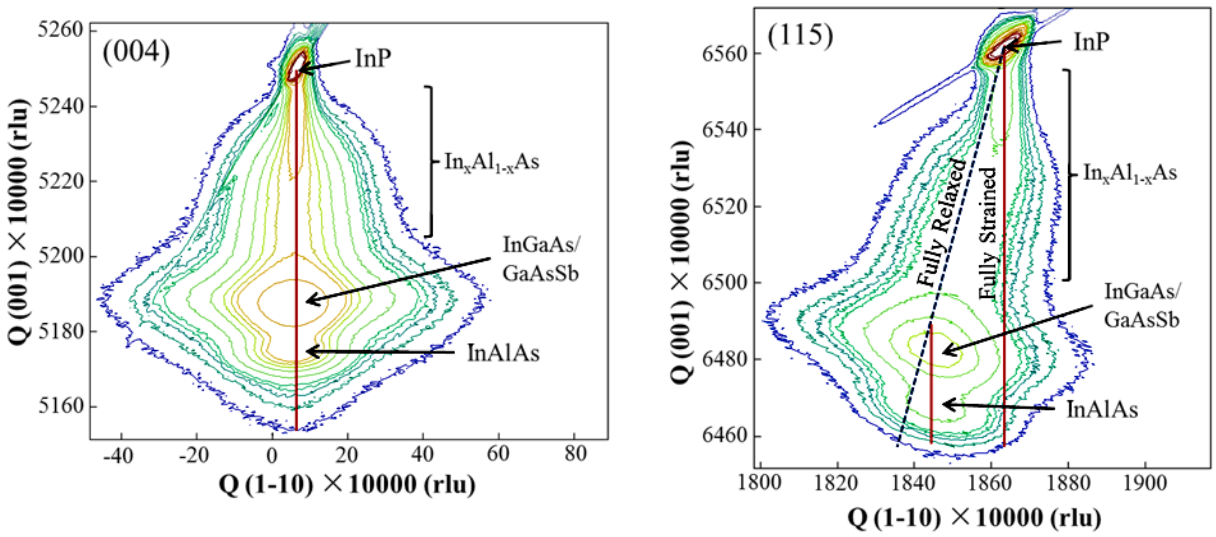


**Figure 5.5** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the GaAs-like interface TFET with a layer structure as shown in Fig. 5.2 (c) using an incident x-ray beam along [$1\bar{1}0$] direction. Used with permission of Nanotechnology Reviews.

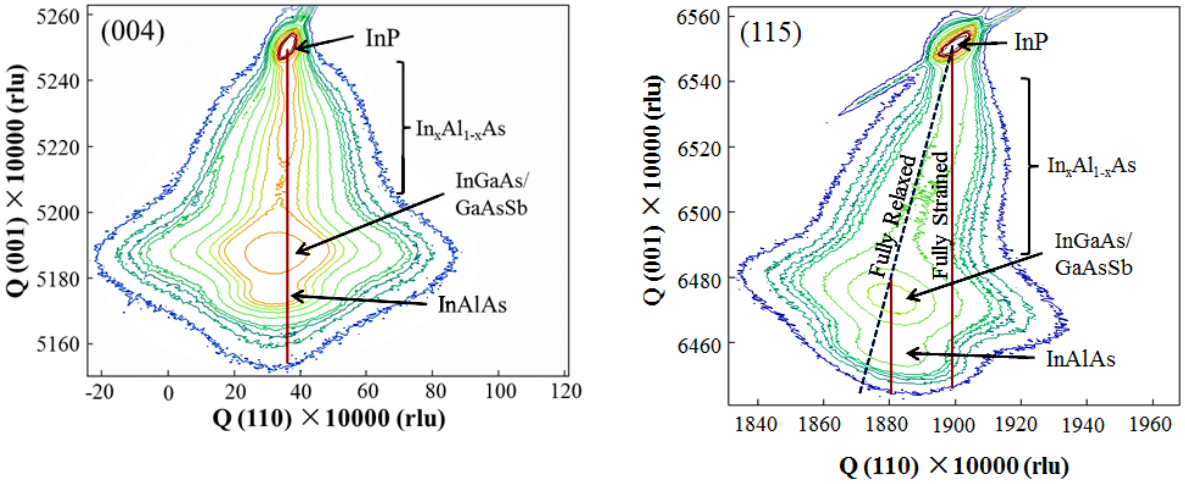


**Figure 5.6** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the GaAs-like interface TFET with a layer structure as shown in Fig. 5.2 (c) using an incident x-ray beam along [110] direction. Used with permission of Nanotechnology Reviews.

In addition, higher degree of strain relaxation states indicates higher dislocation density within $In_{0.7}Ga_{0.3}As$ channel/drain layers of the GaAs-like interface structure, supported by larger elongation of the corresponding RLP along the x-axis of RSM as shown in Fig. 5.5 and 5.6. In

fact, the elongation of this RLP is highly enfeebled after removing the top $In_{0.7}Ga_{0.3}As$ layer from the GaAs-like interface structure, and the relaxation value of the $GaAs_{0.35}Sb_{0.65}$ layer of the GaAs-like interface structure was recalculated and found to be ~ 80% after etching the top $In_{0.7}Ga_{0.3}As$ layer, which is quite identical with that in the GaAs-like interface structure [4]. The comparison of (004) and (115) RSMs of the GaAs-like interface TFET structure before and after etching the top $In_{0.7}Ga_{0.3}As$ layer is shown in Fig. 5.7 and Fig. 5.8, respectively. The above results reveal that the $GaAs_{0.35}Sb_{0.65}$ layer is not as defective as the $In_{0.7}Ga_{0.3}As$ layer in the GaAs-like interface structure and the higher dislocation density is only confined within the top $In_{0.7}Ga_{0.3}As$ layer.

The lattice parameters, mismatch, composition and relaxation of each layer from both the InAs-like interface and GaAs-like interface structures are summarized in Table 5.2 [4]. As shown in the table, both of these two structures show symmetric strain relaxation along two orthogonal [110] and $[1\bar{1}0]$ directions, indicating approximately equal amount of α and β dislocations formed in the relaxation of strain. In addition, from the measured in-plane and out-of-plane lattice constants of the InAs-like interface structure, the pseudomorphic nature of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ was confirmed, indicating low dislocation within these two layers. Therefore, the InAs-like interface TFET structure creates a "virtually" defect-free active region than GaAs-like interface TFET structure, which is desirable for improving the performance of TFET devices with lower OFF-state $p^+$-i-$n^+$ leakage and higher $I_{ON}/I_{OFF}$ ratio.

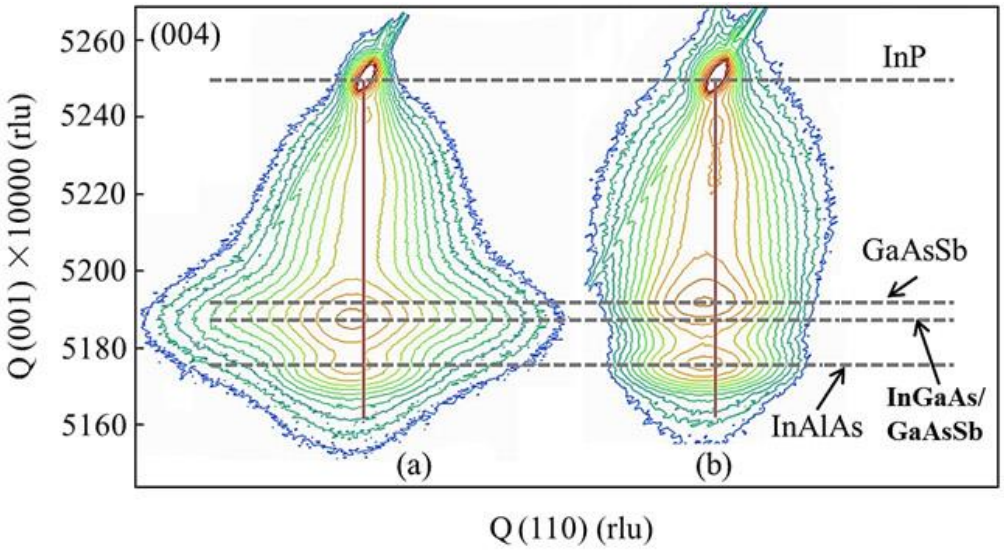


**Figure 5.7** (a) Symmetric (004) RSMs of the GaAs-like interface TFET structure before etching the top $In_{0.7}Ga_{0.3}As$ layer and (b) symmetric (004) RSMs of the GaAs-like interface TFET structure after etching the top $In_{0.7}Ga_{0.3}As$ layer.

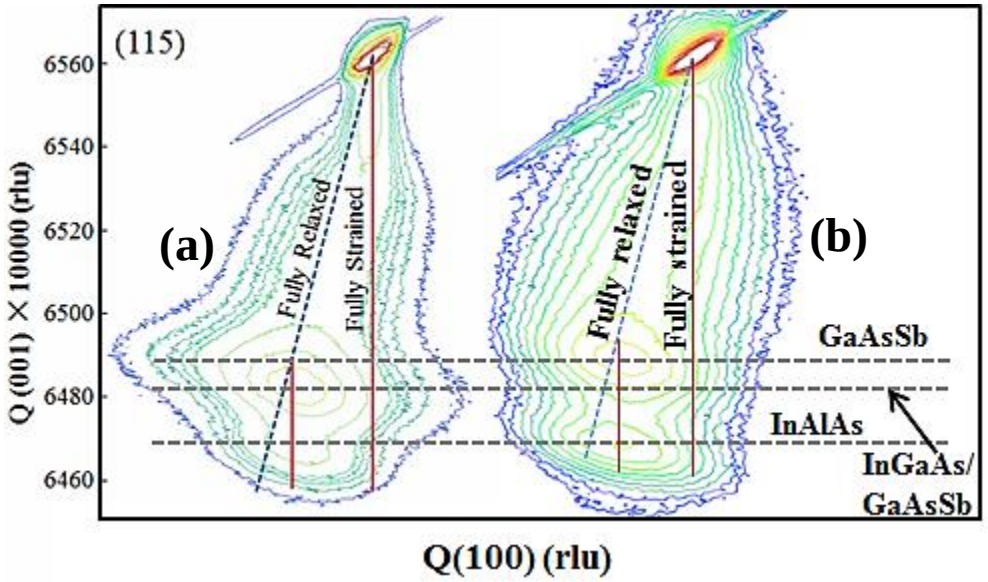


**Figure 5.8** (a) Asymmetric (115) RSMs of the GaAs-like interface TFET structure before etching the top $In_{0.7}Ga_{0.3}As$ layer and (b) asymmetric (115) RSMs of the GaAs-like interface TFET structure after etching the top $In_{0.7}Ga_{0.3}As$ layer.

**Table 5.2** Summary of InAs-like and GaAs-like interfaces TEFT structures with incident x-ray beam along [1$\bar{1}$0] and [110] directions. c is out-of-plane lattice constant, a is in-plane lattice constant and $a_r$ is relaxed lattice constant. [4] Used with permission of Nanotechnology Reviews.

| Sample | Incident Beam Direction | Layers | Lattice Constant (Å) | | | Composition | Relaxation (%) | Tilt (arcsec) | Strain (%) |
|---|---|---|---|---|---|---|---|---|---|
| | | | c | a | $a_r$ | | | | |
| (a) GaAs-like Interface | [1$\bar{1}$0] | InGaAs/ GaAsSb | 5.9401 | 5.9322 | 5.9361 | In: 70% Sb: 65% | 94 | -37 | 1.15 |
| | | InAlAs | 5.9538 | 5.9180 | 5.9359 | In: 70% | 73 | -43 | 1.14 |
| | [110] | InGaAs/ GaAsSb | 5.9400 | 5.9284 | 5.9342 | In: 69% Sb: 64% | 91 | -145 | 1.11 |
| | | InAlAs | 5.9537 | 5.9182 | 5.9360 | In: 69% | 74 | -164 | 1.15 |
| (b) InAs-like Interface | [1$\bar{1}$0] | GaAsSb | 5.9249 | 5.9064 | 5.9157 | Sb: 64% | 80 | -19 | 0.80 |
| | | InGaAs | 5.9481 | 5.9159 | 5.9318 | In: 69% | 75 | -43 | 1.08 |
| | | InAlAs | 5.9651 | 5.9235 | 5.9443 | In: 71% | 72 | -44 | 1.29 |
| | [110] | GaAsSb | 5.9247 | 5.9065 | 5.9156 | Sb: 64% | 81 | 95 | 0.80 |
| | | InGaAs | 5.9481 | 5.9168 | 5.9323 | In: 69% | 76 | 78 | 1.08 |
| | | InAlAs | 5.9655 | 5.9235 | 5.9445 | In: 71% | 72 | 95 | 1.29 |

### 5.3.2 Surface morphology

The study of surface morphology of metamorphic structures is an important figure of merit due to the expected crosshatch pattern resulting from ideal strain relaxation of the linearly graded $In_xAl_{1-x}As$ buffer with minimum concentrations of threading dislocations. For the TFET structure as shown in Fig. 5.2 (c), surface morphology of the TFET structures with different source/channel interface engineering was examined by AFM in contact mode from the top $In_{0.7}Ga_{0.3}As$ surface. The 20μm × 20μm AFM micrographs of the InAs-like interface structure and GaAs-like interface structure and related line profiles in two orthogonal <110> directions are

shown in Figures 5.9 and 5.10, respectively. From Fig. 5.9, the anticipated two-dimensional crosshatch pattern is well-developed and quite uniform, as expected for an ideal graded buffer, from the InAs-like interface TFET structure. The peak-to-valley height from line profiles in the two orthogonal <110> direction is also included in these figures. The uniform distribution of the crosshatch pattern from [110] and $[1\bar{1}0]$ directions for the InAs-like interface TFET structure suggests a symmetric relaxation of the linearly graded buffer layer, which is in agreement with the XRD results. The AFM micrograph of the InAs-like interface structure shows a smooth surface morphology with surface root-mean-square (*rms*) roughness of 3.17nm. Compared to the surface morphology of InAs-like interface, the GaAs-like interface structure does not exhibit 2-dimensional crosshatch surface morphology. A grainy texture dispersed crossing the surface was observed from the AFM micrograph of the GaAs-like interface structure. From the line profiles along [110] and $[1\bar{1}0]$ directions, the peak-to-valley height of GaAs-like interface sample is 3× higher than the InAs-like interface structure, indicating a significantly poor surface quality due to the large amount of dislocation embedded within the TFET structure. The surface *rms* roughness of the GaAs-like interface sample is 4.46 nm which is much higher than that of the InAs-like interface structure. The rough surface and deterioration of the two-dimensional cross-hatch pattern on the surface of GaAs-like interface structure should be attributed to the higher dislocation density of the $In_{0.7}Ga_{0.3}As$ layer introduced by the GaAs-like interface, which was also confirmed by the broadening of the RLP during x-ray measurement as introduced in ***Chapter 5.3.1***. From the AFM micrographs of these two structures, it can be concluded that the InAs-like interface structure shows a much better surface morphology with typical two-dimensional cross-hatch patterns and lower peak-to-valley height corresponding to a reduced *rms* roughness compared with the GaAs-like interface structure. As the two structures are identical

except the interface between $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, one can indicate that the InAs-like interface can provide a better surface morphology relating to higher crystalline quality of the $In_{0.7}Ga_{0.3}As$ layer and thus one can expect a much lower defect density in the InAs-like interface TFET structure and superior electrical transport properties [4].

### 5.3.3 Dislocation and defects

In order to further investigate the influence of different terminated atoms to the structural properties of mixed As/Sb staggered gap TFET structures, the dislocations, defects and the crystalline quality of both GaAs-like interface and InAs-like interface structures are characterized by cross-sectional TEM analysis. Figures 5.11 (a) and (b) show cross-sectional TEM micrographs of the InAs-like interface and GaAs-like interface structures, respectively. All the layers were labeled in these figures and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface was denoted by an arrow in each micrograph. One can find from these figures that the linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch induced dislocations between the active layers and the InP substrate in both structures. No threading dislocations observable in the $GaAs_{0.35}Sb_{0.65}$ layers grown on the linearly graded $In_xAl_{1-x}As$ buffers in both of the two structures, indicating that the $In_xAl_{1-x}As$ linearly graded buffer effectively accommodate the lattice mismatch between the active layer and the InP substrate and thus provides a high-quality virtual substrate for the TFET structures.

It can be seen from Figure 5.11 (a) that no threading dislocations were observed in the top $In_{0.7}Ga_{0.3}As$ layer of the InAs-like interface TFET structure at this magnification, indicating a threading dislocation density (TDD) in this layer on the order of or below $\sim 10^7/cm^2$. The low

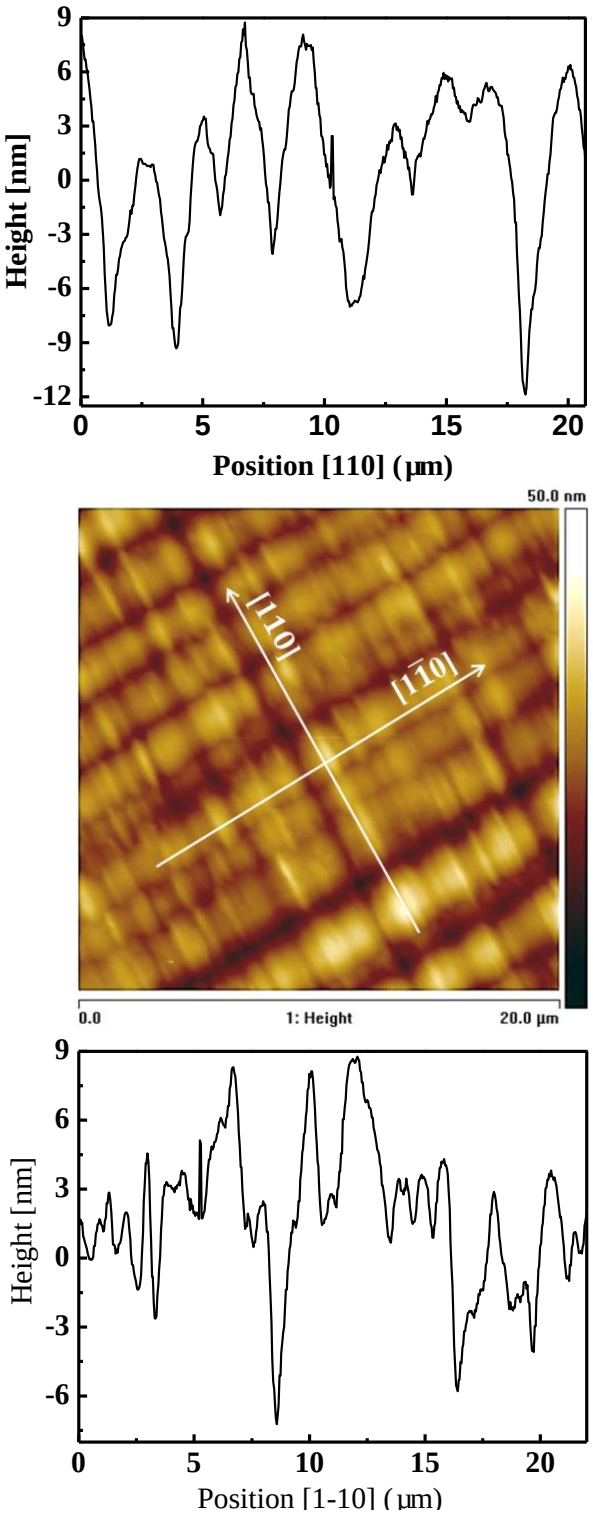


**Figure 5.9** 20µm×20µm AFM surface morphology and line profiles in two orthogonal <110> directions of the InAs-like interface TFET structure (The layer diagram of this structure is shown in Fig. 5.2 (c)). The micrograph shows typical cross-hatch pattern with *rms* roughness of 3.17nm. [4] Used with permission of Nanotechnology Reviews.

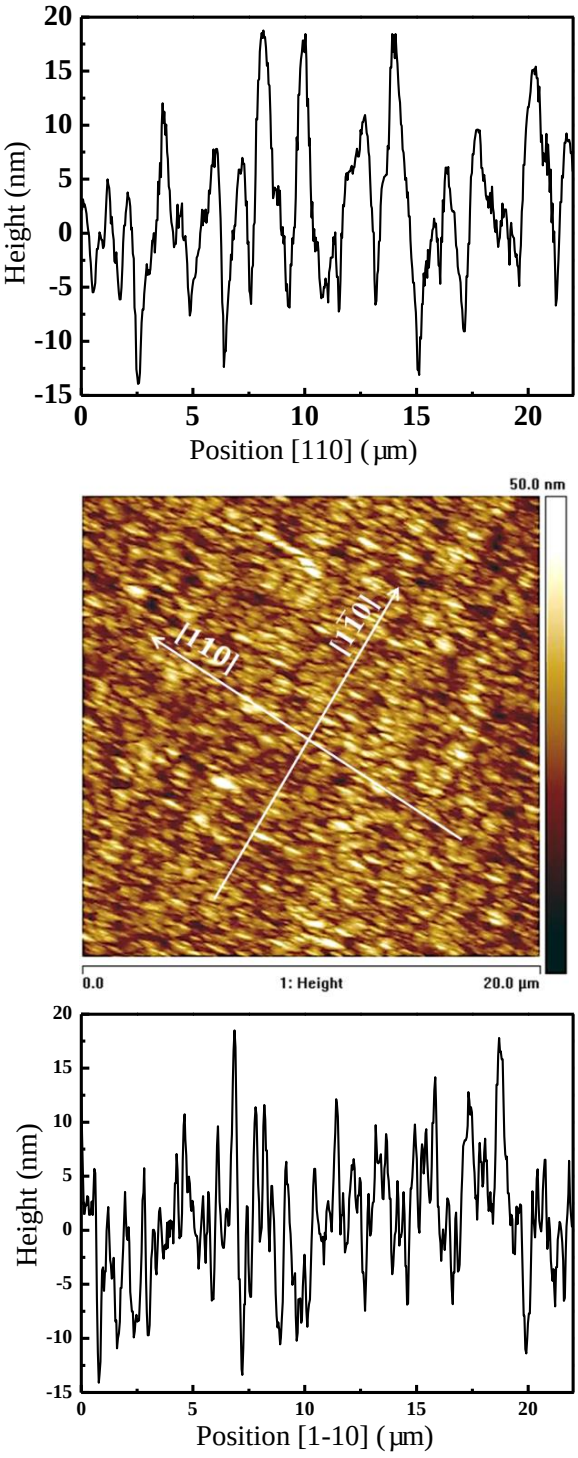


**Figure 5.10** 20µm×20µm AFM surface morphology and line profiles in two orthogonal <110> directions of the GaAs-like interface TFET structure (The layer diagram of this structure is shown in Fig. 5.2 (c)). The micrograph shows a grainy texture dispersed crossing the surface with *rms* roughness of 4.46nm. [4] Used with permission of Nanotechnology Reviews.

dislocation density of the $In_{0.7}Ga_{0.3}As$ layer in the InAs-like interface structure leads to a superior surface and well-developed two dimensional crosshatch pattern from the linearly graded buffer, both of which are confirmed with the results from AFM analysis. Moreover, the low dislocation density also contributes to the pseudomorphic characteristic of the $In_{0.7}Ga_{0.3}As$ layer and the small $\Delta\omega$ broadening of the RLP in RSMs from InAs-like interface TFET structure. In contrast, high dislocation density was detected in the $In_{0.7}Ga_{0.3}As$ layer of the GaAs-like interface TFET structure. Threading dislocations were generated from the interface of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ and went all the way up through the $In_{0.7}Ga_{0.3}As$ layer. The dislocation density in the $In_{0.7}Ga_{0.3}As$ layer was too high to be quantified. As no dislocation was observed from the bottom $GaAs_{0.35}Sb_{0.65}$ layer on which the $In_{0.7}Ga_{0.3}As$ was grown, it was reasonable to conclude that the GaAs-like interface contributed to the high dislocation density in the $In_{0.7}Ga_{0.3}As$ layer and it is consistent with the XRD analysis discussed in ***Chapter 5.3.1***. Moreover, it is also clear that the poor surface morphology of the GaAs-like interface TFET structure from AFM measurement and the elongation of the RLP in RSMs are due to a very high defect density present in the top $In_{0.7}Ga_{0.3}As$ layer, as observed by cross-sectional TEM.

Based on the above analysis, the InAs-like interface provides a high-quality TFET structure compared to GaAs-like interface, where higher dislocations are detected in the channel and drain $In_{0.7}Ga_{0.3}As$ layer, as characterized from X-ray, AFM and cross-sectional TEM analysis. The higher dislocation density at the source/channel interface and within the channel/drain layer of the GaAs-like interface structure will enhance both the SRH G-R and tunneling process at the heterointerface, which will contribute to the higher OFF state leakage current and degrades the $I_{ON}/I_{OFF}$ ratio of the TFET devices.

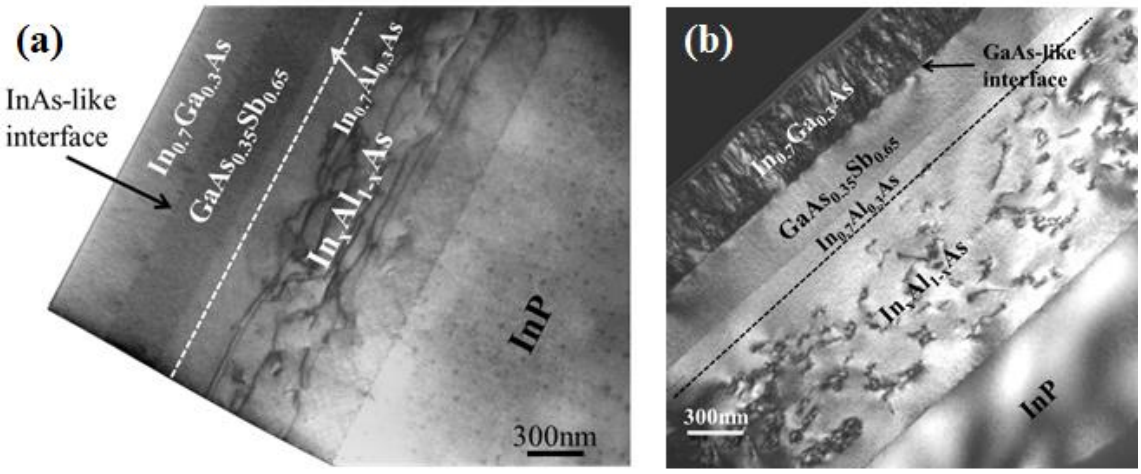


**Figure 5.11** Cross-sectional TEM micrographs of (a) InAs-like interface and (b) GaAs-like interface $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered gap TFET structures. No threading dislocations are observed in the $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers of the InAs-like interface structure, indicating a threading dislocation density on the order of or below $10^7$ $cm^{-2}$ in this region. High dislocation density was detected at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface and in the $In_{0.7}Ga_{0.3}As$ layer of the GaAs-like interface structure. The InAs-like interface provides a high-quality TFET structure compared to GaAs-like interface structure. [4] Used with permission of Nanotechnology Reviews.

## 5.4 OFF-state performance

As shown in ***Chapter 5.3***, different terminated atoms at $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface greatly influence the structural properties of the TFET structures. These structural properties difference, such as strain relaxation and defect density differences will further influence the device performances. Especially, the high dislocation density at the source/channel interface of the GaAs-like interface structure may change the OFF-state transport mechanism of the fabricated devices and lead to high leakage current. In order to assess the impact of different interface engineering on the OFF-state performance of TFETs, two sets of $p^+$-i-$n^+$ diodes were fabricated using the process flow discussed in ***Chapter 3.3***. As the OFF-state current of TFETs is govern by the leakage current of the reverse-biased $p^+$-i-$n^+$ diode [4, 6], current-voltage (I-V) characteristics of these $p^+$-i-$n^+$ diodes were measured and compared. Figure 5.12 [4] shows the

room temperature I-V characteristics of the $p^+$-i-$n^+$ diodes from the InAs-like interface and GaAs-like interface structure. About four orders higher leakage current density was observed from the GaAs-like interface structure than the InAs-like interface $p^+$-i-$n^+$ diodes at 300K, indicating different OFF-state transport mechanisms are involved in these TFET structures. In order to gain insight into the OFF-state current mechanism for these TFET structures, temperature dependent I-V measurements were carried out on these reverse-biased $p^+$-i-$n^+$ diodes with temperature ranging from 150K to 300K and simulations have been performed with Sentaurus [7] to explain the difference in OFF-state transport between two structures.

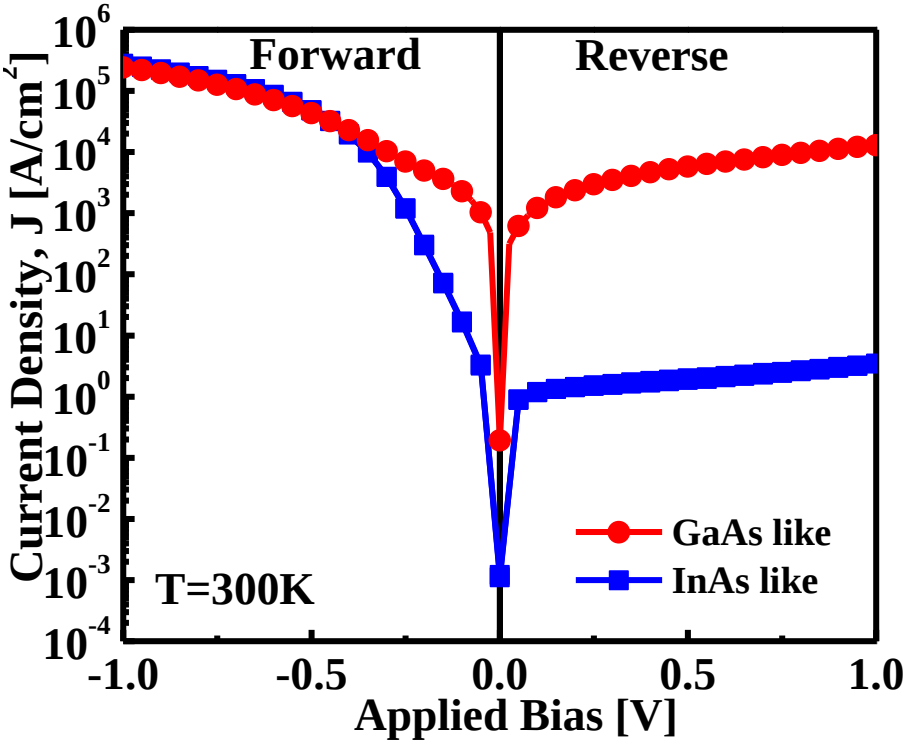


**Figure 5.12** Measured I-V characteristic of GaAs-like interface and InAs-like interface reverse biased $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode at T=300K. Almost four orders higher leakage current density was observed from the GaAs-like interface $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode than the InAs-like interface $p^+$-i-$n^+$ diode. [4] Used with permission of Nanotechnology Reviews.

Figure 5.13 (a) [4] shows the I-V characteristics of the reverse biased $p^+$-i-$n^+$ diode at different measurement temperatures from the InAs-like interface device. One can find from this

figure that the OFF-state leakage current increasing exponentially with rising temperature. A field enhanced SRH G-R model [8] was used to explain the OFF-state leakage mechanism of the InAs-like interface $p^+$-i-$n^+$ diode at different temperature. A lower positive fixed change density, $Q_f = 10^{12}cm^{-2}$ due to lower defect density at the source/channel interface was also incorporated in the simulation along with the field enhanced SRH G-R process to explain the OFF-state leakage current. The simulated I-V characteristics (solid lines) agreed well with the measured data (scattered line) at different temperatures, suggesting the validation of the model used in InAs-like interface $p^+$-i-$n^+$ diode. Figure 5.13 (b) [4] shows the Arrhenius plot of the OFF-state leakage from the reverse-biased $p^+$-i-$n^+$ diode as a function of 1/kT at various reverse bias voltages. A straight line fitting to these data points at a given reverse bias yield a gradient which corresponds to the activation energy of $E_A = E_C - E_T$, which is responsible for the OFF-state leakage current generation. Here, $E_C$ stands for the conduction band minimum of channel near the source/channel interface and $E_T$ is the energy of trap states. One can find from this figure that $E_A$ decreases with increasing reverse bias voltage from 0.17eV to 0.125eV, results in an increasing leakage current trend. This is due to the fact that the electrical field intensity across the $p^+$-i-$n^+$ diode was enlarged as increasing the reverse bias voltage. The enlarged electrical field further increases the band-bending which leads to a stronger field enhanced SRH G-R process across the interface.

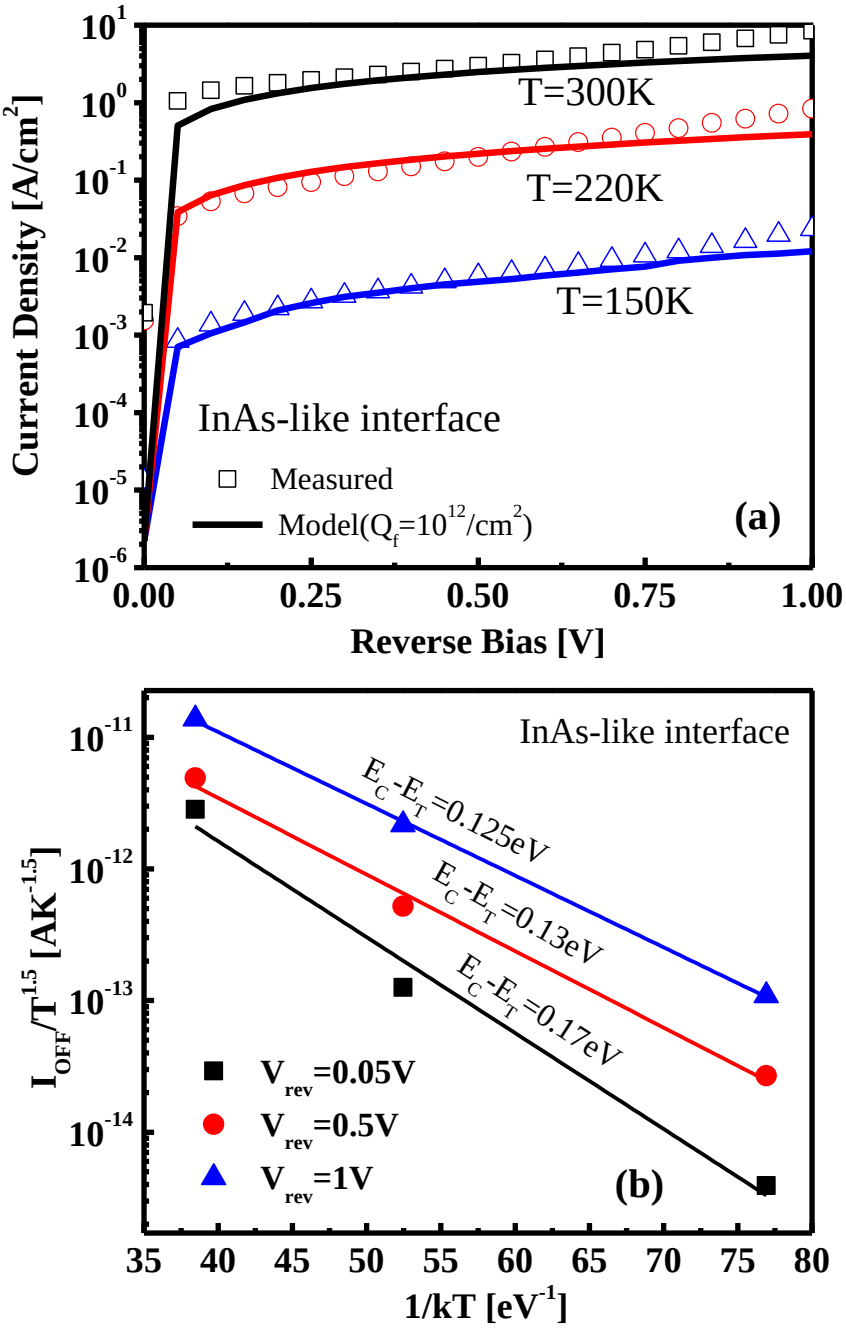


**Figure 5.13** (a) Measured and simulated I-V characteristics of reverse biased InAs-like interface $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode for temperature ranging from 150K to 300K and (b) an extraction of the activation energy for leakage current generation as a function of reverse bias voltage of InAs-like interface $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode. The field enhanced SRH G-R model agrees well with the measured data. The activation energy shows dependence of reverse bias voltage. [4] Used with permission of Nanotechnology Reviews.

Figure 5.14 [4] shows the I-V characteristics of the reverse biased $p^+$-i-$n^+$ diode at different measurement temperatures of the GaAs-like interface device. One can find from this figure that the OFF-state leakage current is much higher than that of InAs-like interface device at each temperature step. The leakage current reduces with decreasing temperature from 300K to 150K, as expected, but the decrease trade is not as strong as the InAs-like interface device. Moreover, the weaker temperature dependence and the higher leakage current confirmed that the tunneling process dominates the OFF-state transport of the GaAs-like interface $p^+$-i-$n^+$ diode, which is indeed the case due to higher dislocation density present in the $In_{0.7}Ga_{0.3}As$ channel and drain regions. A direct BTBT model [9] was performed to explain the observed high OFF-state current caused by high dislocation density observed at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. As shown in Figure 5.14 [4], the simulated I-V characteristics (solid lines) agreed well with the measured data (scattered lines) at all temperatures. To explain why the BTBT process dominates the OFF-state transport of the GaAs-like interface TFET structure, positive fixed charges caused by Tamm states and point defects which are widely observed at the heterointerface of mixed As/Sb material systems [10, 11] were introduced at the GaAs-like interface region in the simulation. The fixed positive charges cause energy band bending at the GaAs-like heterointerface region. Figure 5.15 (a) [4] shows the simulated band diagram of the GaAs-like interface TFET structure and the inset shows the position of the fixed positive charges in this energy band diagram. A high fixed positive charge density of $1.5\times10^{13}/cm^2$ due to higher defect density is needed to induce the large band bending in the GaAs-like interface structure to generate the OFF-state current as measured in different temperature steps. As shown in Figure 5.15 (a) [4], the fixed charge density at this level can convert the band alignment of the TFET structure from staggered gap to broken gap, resulting in an overlap of the valence band of

$GaAs_{0.35}Sb_{0.65}$ source with the conduction band of $In_{0.7}Ga_{0.3}As$ channel, causing the device to be normally ON even at OFF-state. As a result, the high fixed positive charge density caused by Tamm states and point defects related to the high defect density at the GaAs-like interface leads to the interband tunneling which dominates the OFF-state transport of the GaAs-like interface TFET structure.

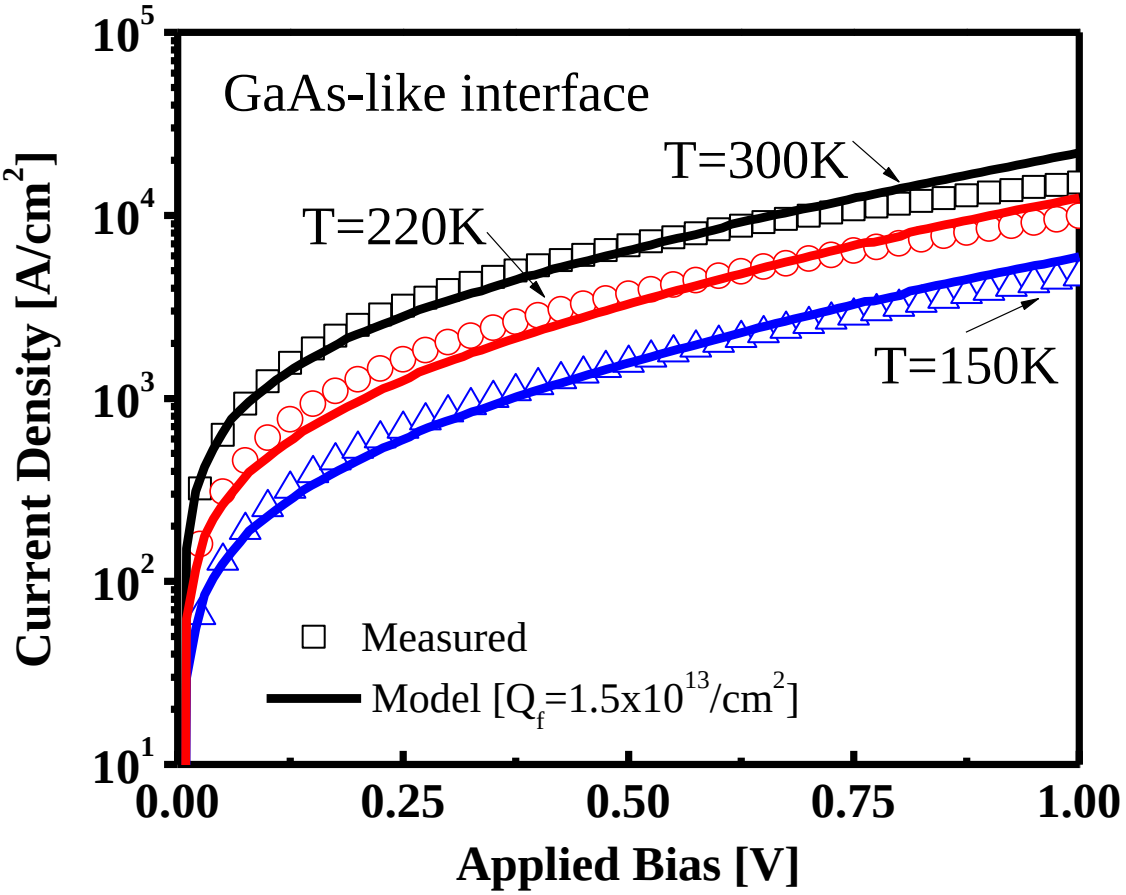


**Figure 5.14** Measured and simulated I-V characteristics of reverse biased GaAs-like interface $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode for temperature ranging from 150K to 300K. The direct BTBT model agrees well with the measured data at different temperature ranges. The small temperature dependence and the high leakage current confirm that the tunneling process is the dominating OFF-state transport mechanism in this structure. [4] Used with permission of Nanotechnology Reviews.

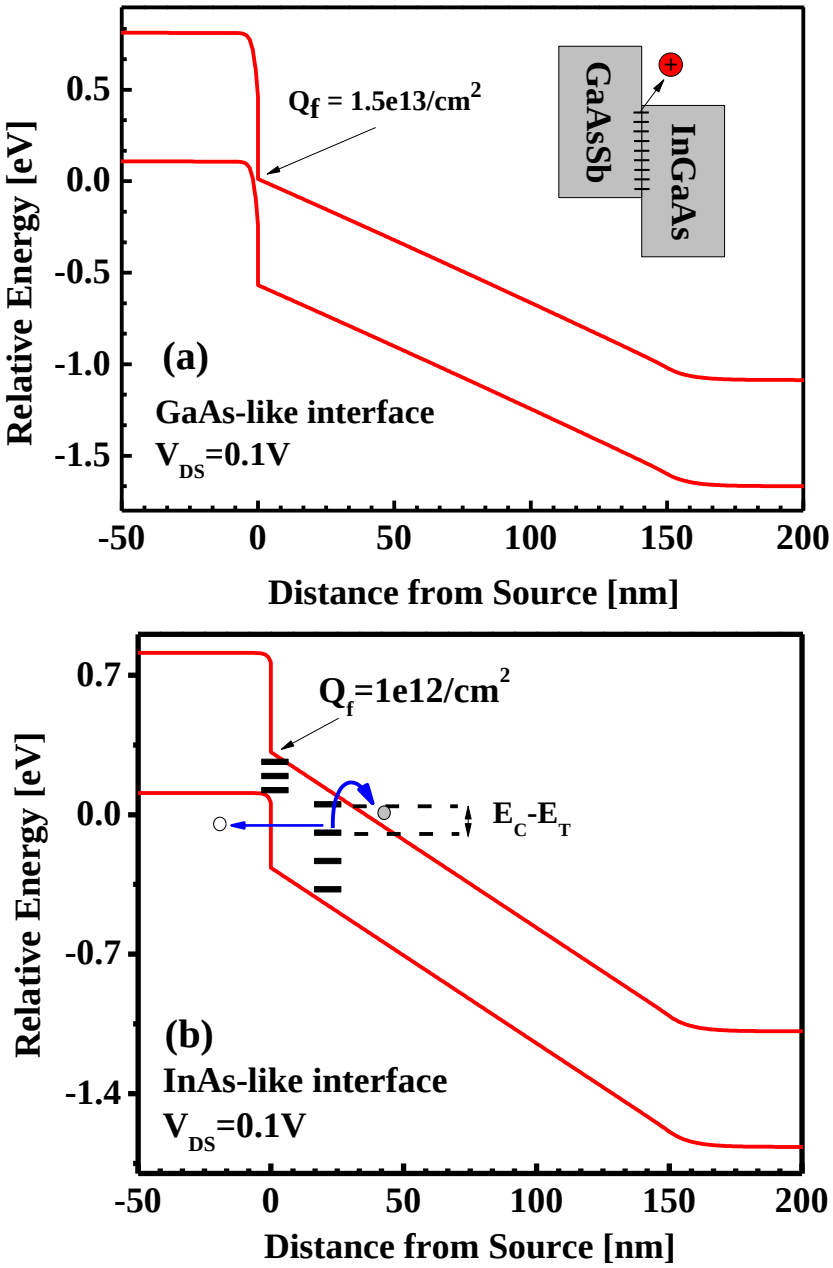


**Figure 5.15** (a) Simulated band diagram of GaAs-like interface TFET structure with $V_{DS}$ = 0.1V. The inset shows the position of fixed positive charge. High fixed charge density bends energy bands, resulting in overlap of the valence band of $GaAs_{0.35}Sb_{0.65}$ source and conduction band of $In_{0.7}Ga_{0.3}As$ channel, causing the device to be normally on even at OFF state. (b) Simulated band diagram of InAs-like interface TFET structure with $V_{DS}$ = 0.1V. Fixed charges and trap states are indicated in the figure. The staggered band alignment is well kept due to lower fixed charge density at the interface region of source/channel. [4] Used with permission of Nanotechnology Reviews.

In contrast, a lower positive fixed change density, $Q_f = 10^{12}cm^{-2}$ due to lower defect density at the source/channel interface was incorporated in the simulation of OFF-state performance of InAs-like interface device. The simulated energy band diagram of the InAs-like interface TFET structure with a fixed interface charge density of $Q_f = 10^{12}cm^{-2}$ is shown in Figure 5.15 (b) [4]. One can find from this figure that the type-II staggered band alignment was well maintained in the InAs-like interface TFET structure which leads to lower leakage current at OFF-state. The field enhanced SRH G-R mechanism [8] is also noted in this figure, where the carriers in the $p^+$ source region firstly tunnel into mid-gap states and a subsequent thermal emission process inject them into the conduction band of the channel. In order to gain further insight into the band alignment of these TFET structures as a function of fixed positive charge density within the source/channel interface region, simulation was performed to generate band diagrams at different $Q_f$. As shown in Figure 5.16 [4], the $E_{beff}$ is decreasing with increasing value of $Q_f$. One can find from this figure that by varying $Q_f$ value, the band lineup can be converted from staggered to broken gap. Although a broken lineup yields the best ON-state performance, it can also increase the OFF-state leakage current and thus significantly reduces the $I_{ON}/I_{OFF}$ ratio. Figure 5.16 [4] inset shows the $E_{beff}$ as a function of $Q_f$. It can be seen from this figure that the fixed positive charge density below $1\times10^{12}/cm^2$ have minimal impact on the change of $E_{beff}$ in the InAs-like interface TFET structure. However, the band alignment changes rapidly with the positive fixed charge density greater than $1\times10^{12}/cm^2$. Moreover, the band alignment is converted from staggered gap to broken gap at the fixed charge density of $\sim6\times10^{12}/cm^2$, corresponding to an $E_{beff}$ value of 0eV. In order to maintain the staggered band alignment, a lower $Q_f$ is indispensable, which can be achieved by minimizing the interface defect density in a TFET structure. The InAs-like interface provides lower defect density which leads to lower $Q_f$ at the source/channel

heterointerface, resulting in well maintained type-II staggered gap band alignment. It also leads to lower OFF-state leakage current, higher $I_{ON}/I_{OFF}$ ratio and shows a great potential for future high-performance heterostructure TFETs for low-power logic applications.

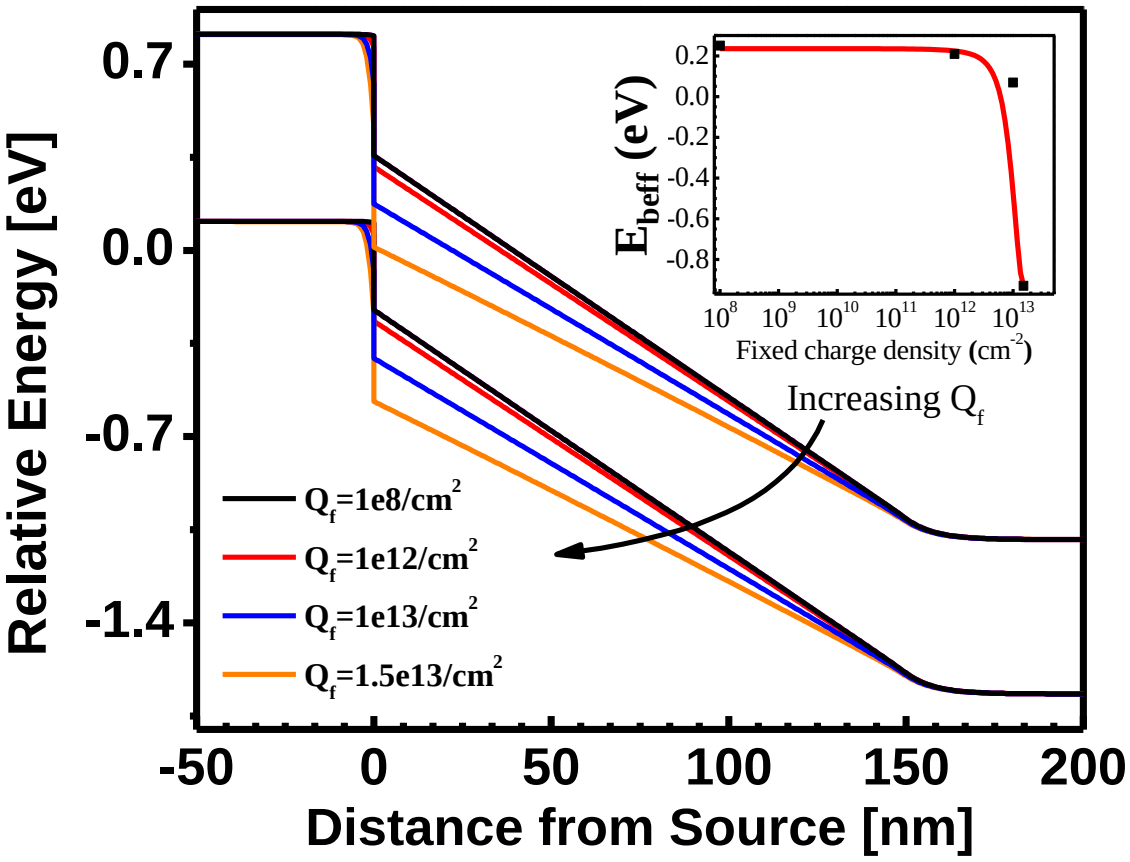


**Figure 5.16** Simulated band diagrams of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ n-channel heterostructure TFET structures with different fixed charges at source/channel interface region. The inset shows the effective tunneling barrier height changes as a function of fixed charge density. The band alignment is converted from staggered gap to broken gap at the fixed charge density of ~$6\times10^{12}/cm^2$. [4] Used with permission of Nanotechnology Reviews.

## 5.5 Experimental determination of band alignments

During the MBE growth of mixed As/Sb heterostructure TFETs, improper change of group-V fluxes at the source and channel interface will introduce intermixing between As and Sb atoms that leads to uncontrolled layer composition at this heterointerface, which in turn will produce

high dislocation density in this region [1, 12]. These dislocations will introduce fixed charges at the source/channel interface [13] and thus, it will affect the band alignment as well as the value of $E_{beff}$ [4]. In ***Chapter 5.4***, simulations showed that the band alignment is converted from staggered gap to broken gap with a fixed positive charge density of ~ $6\times10^{12}/cm^2$ caused by high dislocation density at the source/channel $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface [4]. This resulted in four orders of higher leakage current experimentally measured from this fabricated TFET structure. Therefore, it is necessary to verify this defects assisted band alignment transition by experimental proof in a mixed As/Sb tunnel FET heterostructure.

Kraut *et al.* [14] demonstrated one experimental method to determine the band offset of heterostructures by measuring the core level (CL) and valence band maxima (VBM) binding energies of the materials in the structure using x-ray photoelectron spectroscopy (XPS). To measure the valence band offset (VBO) of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterojunction, $Sb3d_{5/2}/In3d_{5/2}$ CLs and VBM of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ should be detected. In this section, the band alignments of $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterojunction from three structures with different material composition and interface engineering are measured, as discussed above. Structure A has a layer structure as shown in Fig. 5.2 (b) ($GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$) with an InAs-like heterointerface; Structure B has a layer structure as shown in Fig. 5.2 (c) ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) with an InAs-like heterointerface; Structure C also has a layer structure as shown in Fig. 5.2 (c) ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) but with a GaAs-like heterointerface. The structural properties of structure B and C have already been discussed in ***Chapter 5.3***. The structural properties of TFET structure A shows similar properties as structure B due to the InAs-like interface within both of these two structures. As a result, low dislocation density should be expected at the heterointerface of both structures A and B, but high dislocation density is expected at the

heterointerface of structures C. Detailed XRD and cross-sectional TEM studies [2] also confirmed this speculation. Table 5.3 summarized the composition, interface engineering and defect density difference of these three TFET structures. As shown in Fig. 5.17 [2], XPS spectra were collected from three samples of each structure: (1) 5nm InGaAs/310nm GaAsSb was used to measure CL binding energy of In and Sb at the interface; (2) 150nm InGaAs/310nm GaAsSb was used to measure the CL binding energy of In and VBM of InGaAs; (3) 310nm GaAsSb without the top InGaAs layer was used to measure the CL binding energy of Sb and VBM of GaAsSb. XPS measurements were performed on a Phi Quantera Scanning XPS Microprobe instrument using a monochromatic Al Kα (1486.7eV) x-ray source. $In3d_{5/2}$ CL, $Sb3d_{5/2}$ CL, $In_xGa_{1-x}As$ valence (VB) and $GaAs_ySb_{1-y}$ VB spectra were recorded using pass energy of 26eV. An exit angle of 45 ° was used in all measurements. Oxide layers on all sample surfaces were carefully removed by wet chemical etching using citric acid/hydrogen peroxide ($C_6H_8O_7$:$H_2O_2$) at volume ratio of 50:1 for 10 seconds on $In_xGa_{1-x}As$ surface and 1 minutes on $GaAs_ySb_{1-y}$ surface, respectively, before loading into the XPS chamber. About 2-3nm was etched from each sample surface according to the premeasured etching rate [4].

Once the binding energy information from each sample surface was collected, the VBO can be determined by Kraut's [14] method,

$$\Delta E_V = \left(E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}\right) - \left(E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}\right) - \Delta E_{CL}(i) \qquad (5.1)$$

where $E_{Sb\ 3d_{5/2}}^{GaAsSb}$ and $E_{In\ 3d_{5/2}}^{InGaAs}$ are CL binding energies of $Sb3d_{5/2}$ and $In3d_{5/2}$; $E_{VBM}$ is the valence band maxima (VBM) of the corresponding samples. $E_{VBM}$ was determined by linearly fitting the leading edge of the VB spectra to the base line [15]. $E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$ and $E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}$ were measured from 150nm InGaAs/310nm GaAsSb and 310nm GaAsSb without the top InGaAs layer, respectively. $\Delta E_{CL}(i) = E_{Sb\ 3d_{5/2}}^{GaAsSb}(i) - E_{In\ 3d_{5/2}}^{InGaAs}(i)$ is the CL binding energy

**Table 5.3** Summary of composition and defect density difference of the TFET structures studied in the work. [2] Used with permission of Nanotechnology Reviews.

| Structure details | Composition | | Interface engineering | Defect density at source/channel interface and in InGaAs layer |
|---|---|---|---|---|
| | Source | Channel/Drain | | |
| A | $GaAs_{0.4}Sb_{0.6}$ | $In_{0.65}Ga_{0.35}As$ | InAs-like | Low |
| B | $GaAs_{0.35}Sb_{0.65}$ | $In_{0.7}Ga_{0.3}As$ | InAs-like | Low |
| C | $GaAs_{0.35}Sb_{0.65}$ | $In_{0.7}Ga_{0.3}As$ | GaAs-like | High |

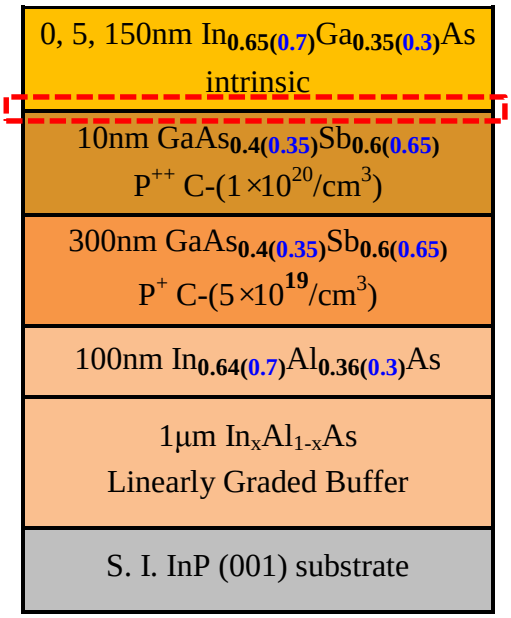


**Figure 5.17** (a) Schematic diagram of GaAsSb/InGaAs heterostructures with different InGaAs thickness for band offset measurements. 5nm InGaAs/310nm GaAsSb was used for the measurement of binding energy at the heterointerface, while 150nm InGaAs/310nm GaAsSb and 310nm GaAsSb without the top InGaAs layer were used to measure the binding energy of bulk InGaAs and GaAsSb, respectively. The dashed box denotes the source/channel interface. [2] Used with permission of Nanotechnology Reviews.

difference of $Sb3d_{5/2}$ and $In3d_{5/2}$ measured at the heterointerface from 5nm InGaAs/310nm GaAsSb sample of each structure. The conduction band offset (CBO) can be estimated by [15],

$$\Delta E_C = E_g^{GaAsSb} + \Delta E_V - E_g^{InGaAs} \quad (5.2)$$

where, $E_g^{GaAsSb}$ and $E_g^{InGaAs}$ are the band gaps of GaAsSb and InGaAs, respectively. The effective tunneling barrier of the TFET is described as,

$$\mathrm{E}_{beff} = E_g^{InGaAs} - \Delta E_V \tag{5.3}$$

where $\Delta E_V$ is the above measured valence band offset.

Figures 5.18 (a) – (f) show the CL and VB spectra from each sample of structure A. The CL energy position was defined to be the center of the peak width at half of the peak height (i.e., full width at half maximum). The CL to VBM binding energy difference for $GaAs_{0.4}Sb_{0.6}$ and $In_{0.65}Ga_{0.35}As$ of structure A were summarized in Table II. The results show that the values of $\left(E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}\right)$ and $\left(E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}\right)$ are 527.66eV and 443.71eV, respectively. The binding energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ at the heterointerface ($\Delta E_{CL}(i)$) was found to be 83.60eV. Using these results, the VBO of $In_{0.65}Ga_{0.35}As$ channel relative to $GaAs_{0.4}Sb_{0.6}$ source is determined to be $0.35 \pm 0.05$eV. The uncertainly value of 0.05eV is from the scatter of VB curve during the fitting of VBM positions. The CL and VB spectra from each sample of structure B and C were shown in Fig. 5.19 and Fig. 5.20, respectively. The measured values of $\left(E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}\right)$, $\left(E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}\right)$ and $\Delta E_{CL}(i)$) from structure B and C are also summarized in Table 5.4. The calculated VBO was 0.39eV for structure B and 0.63eV for structure C.

**Table 5.4** Summary of core level to valence-band maxima binding energy difference (eV) for GaAsSb and InGaAs, and the binding energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ at the heterointerface ($\Delta E_{CL}(i)$) from the three structures. The calculated valence band offset ($\Delta E_V$), conduction band offset ($\Delta E_C$) and effective tunneling barrier ($E_{beff}$) are also listed in the table. [2] Used with permission of Nanotechnology Reviews.

| | Structure A | Structure B | Structure C |
|---|---|---|---|
| $E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}$ (eV) | 527.66 | 527.70 | 527.59 |
| $E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$ (eV) | 443.71 | 443.79 | 443.74 |
| $\Delta E_{CL}(i)$ (eV) | 83.60 | 83.52 | 83.22 |
| $\Delta E_V$ (eV) | 0.35 | 0.39 | 0.63 |
| $\Delta E_C$ (eV) | 0.42 | 0.49 | 0.73 |
| $E_{beff}$ (eV) | 0.30 | 0.21 | -0.03 |

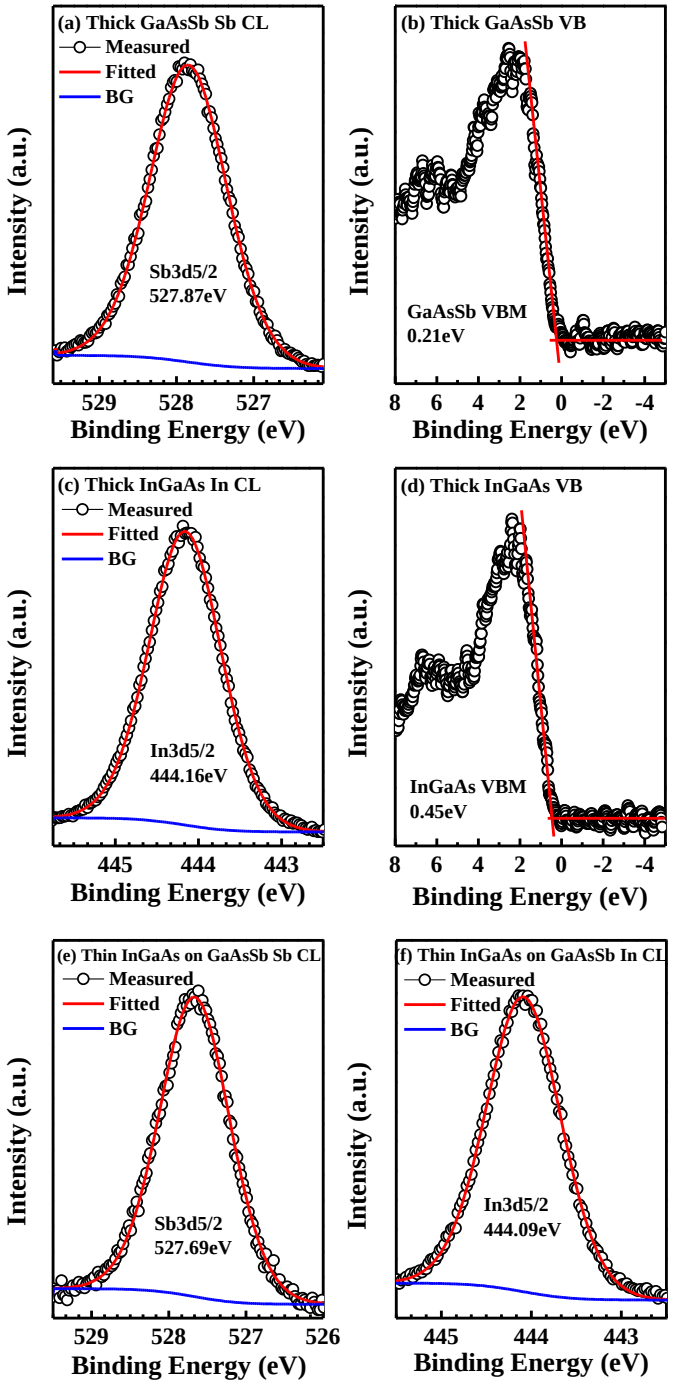


**Figure 5.18** XPS spectra of structure A: (a) $Sb3d_{5/2}$ core level (CL) and (b) $GaAs_{0.4}Sb_{0.6}$ valence band (VB) from 310nm $GaAs_{0.4}Sb_{0.6}$ without the top $In_{0.65}Ga_{0.35}As$ layer of structure A; (c) $In3d_{5/2}$ CL and (d) $In_{0.65}Ga_{0.35}As$ VB from 150nm $In_{0.65}Ga_{0.35}As$/310nm $GaAs_{0.4}Sb_{0.6}$ of structure A; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL from 5nm $In_{0.65}Ga_{0.35}As$/310nm $GaAs_{0.4}Sb_{0.6}$ structure measured at the heterointerface of structure A. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maxima (VBM) were determined by linearly fitting the leading edge of the VB spectra to the base line. Used with permission of AIP.

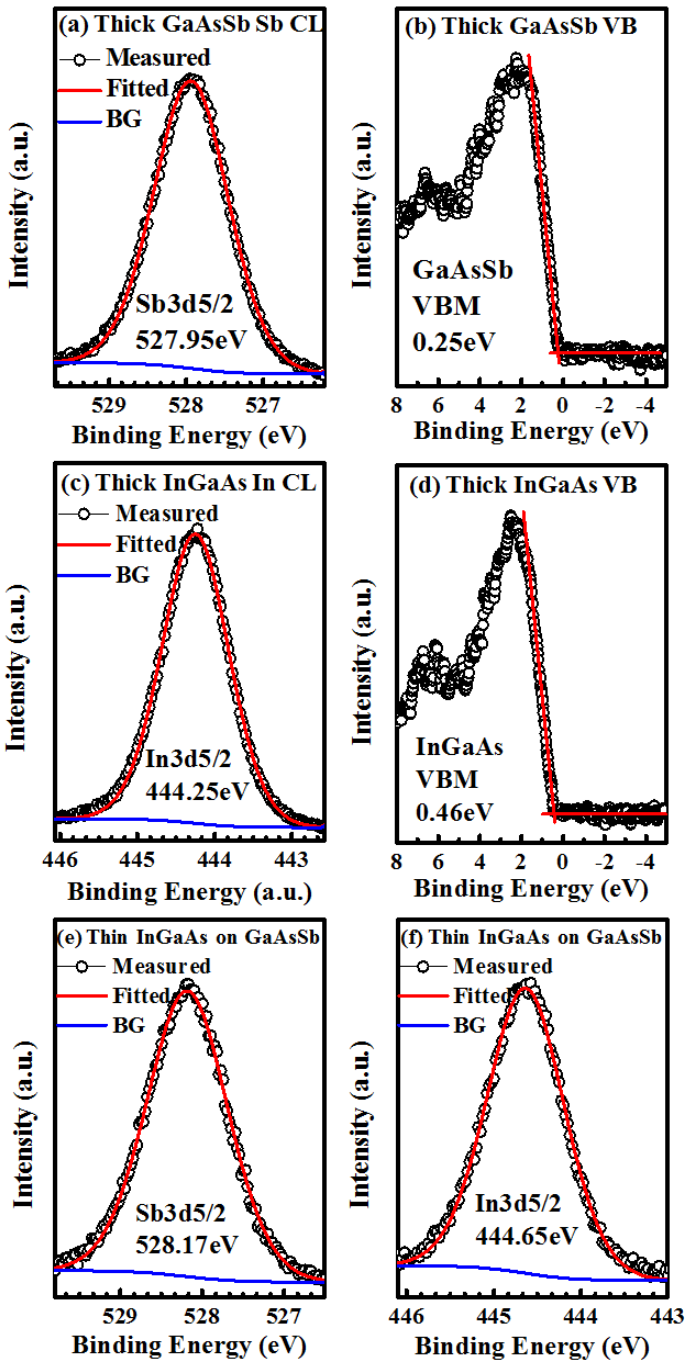


**Figure 5.19** XPS spectra of structure B: (a) $Sb3d_{5/2}$ CL and (b) VB spectra from 310nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer; (c) $In3d_{5/2}$ CL and (d) VB spectra from 150nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ sample; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL spectra from 5nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ sample measured at the interface; (g) high resolution scan in the range of 526-540eV and no O1s peak or Sb-O bond was detected. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. Used with permission of AIP.

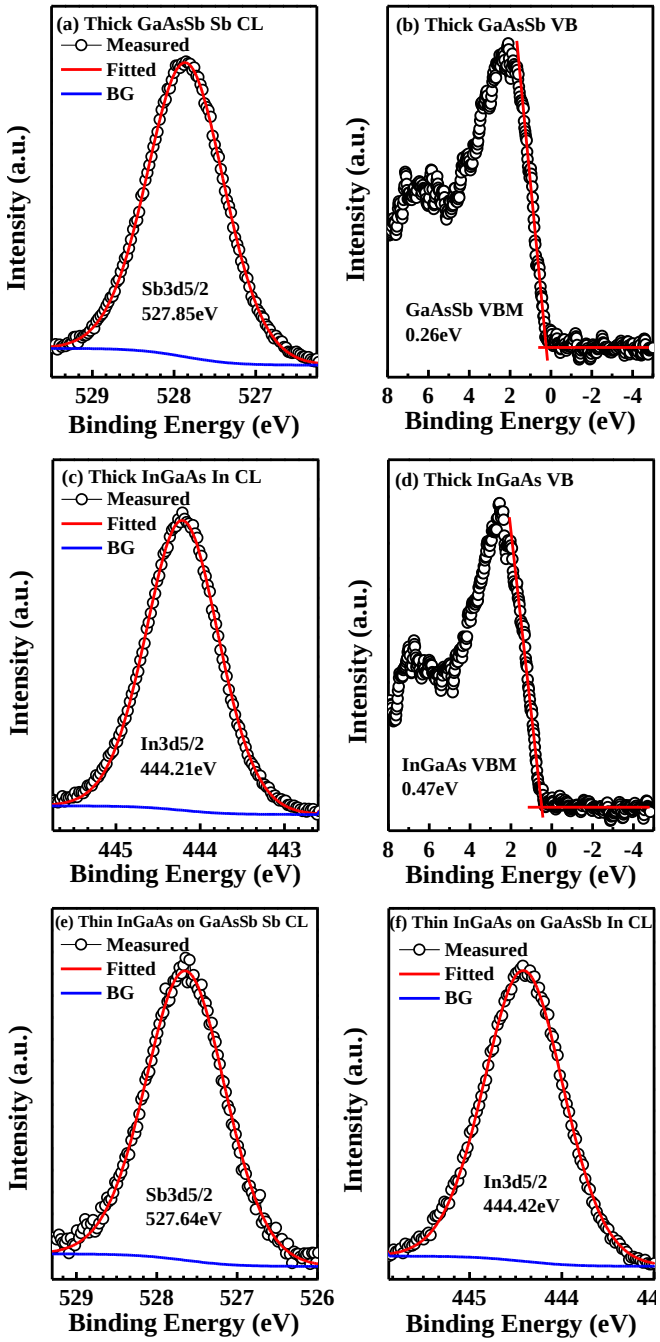


**Figure 5.20** XPS spectra of structure C: (a) $Sb3d_{5/2}$ core level (CL) and (b) $GaAs_{0.35}Sb_{0.65}$ valence band (VB) from 310nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer of structure C; (c) $In3d_{5/2}$ CL and (d) $In_{0.7}Ga_{0.3}As$ VB from 150nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ of structure C; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL from 5nm $In_{0.7}Ga_{0.3}As$/310nm $GaAs_{0.35}Sb_{0.65}$ structure measured at the heterointerface of structure C. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maxima (VBM) were determined by linearly fitting the leading edge of the VB spectra to the base line. Used with permission of AIP.

Based on the measured XPS CL and VBM values and using Kraut's [14] method, the measured VBO ($\Delta E_V$), calculated conduction band offset ($\Delta E_C$) and $E_{beff}$ are summarized in Table 5.4. Here, the $E_{beff}$ determines the type of band alignment in the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterostructure, *i.e.*, the band alignment is staggered lineup if $E_{beff} > 0$ but broken lineup if $E_{beff} < 0$. Positive effective tunneling barrier height of 0.30eV and 0.21eV were determined on structure A (In = 0.65, Sb = 0.6) and B (In = 0.7, Sb = 0.65), respectively, indicating a staggered band alignment.

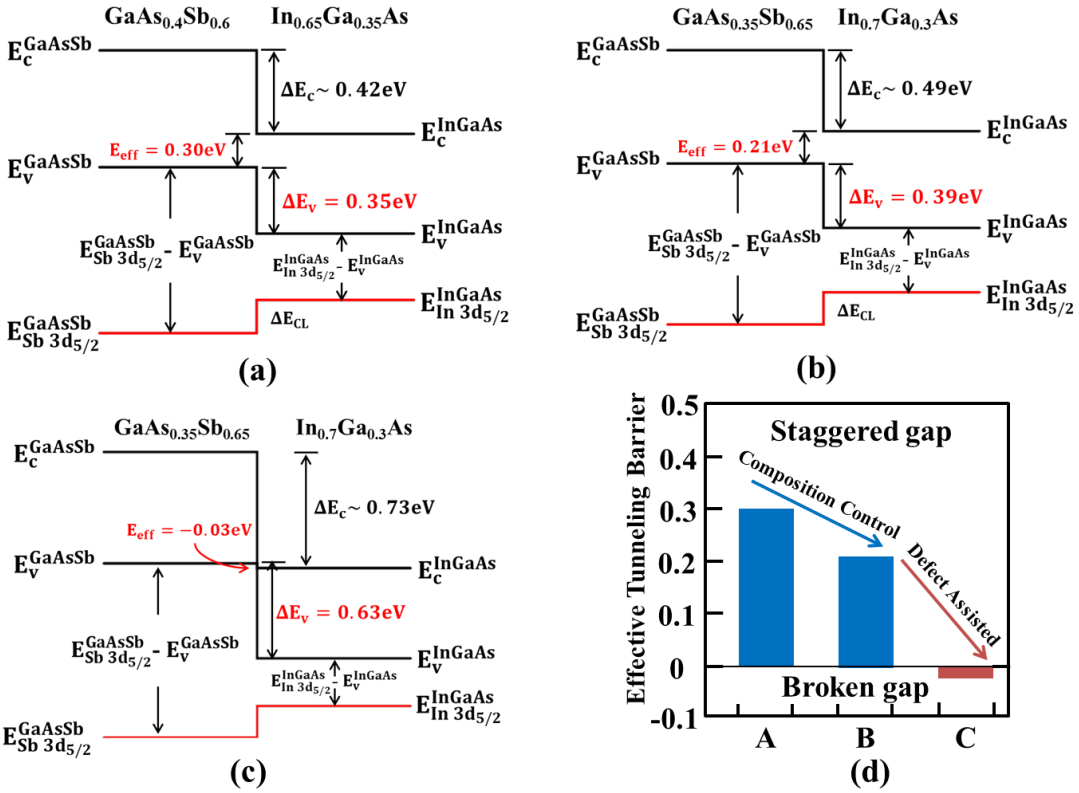


**Figure 5.21** Schematic energy band diagram of (a) structure A, (b) structure B and (c) structure C. A type-II staggered band lineup with positive effective tunneling barrier height of 0.30eV and 0.21eV were determined at the heterointerface of structure A and B, respectively, while a broken band lineup with negative tunneling barrier height of -0.03eV was found at the heterointerface of structure C. (d) Histogram summarized the effective tunneling barrier height and the corresponding band alignment types of these structures. [2] Used with permission of Nanotechnology Reviews.

Figures 5.21 (a) and (b) [2] show the schematic band alignments of structure A and B based on the band gap energy values determined above and the experimental results of VBO measured by XPS. From these figures, one can find that the measured VBO of intrinsic $In_xGa_{1-x}As$ channel layer with respect to $GaAs_ySb_{1-y}$ source layer is 0.35eV and 0.39eV for In (Sb) compositions of 0.65 (0.60) and 0.70 (0.65), respectively. The higher value of VBO for In compositions of 0.7 compared to 0.6, is expected due to the lower bandgap of $In_{0.7}Ga_{0.3}As$. Wang *et al.* [16] systematically calculated the valence band offsets between most of the III-V semiconductor alloys by a self-consistent band structure method. Using these calculations, the VBO of intrinsic $In_{0.65}Ga_{0.35}As$ relative to intrinsic $GaAs_{0.4}Sb_{0.6}$ as well as intrinsic $In_{0.7}Ga_{0.3}As$ with respect to intrinsic $GaAs_{0.35}Sb_{0.65}$ was determined to be 0.32eV and 0.34eV, respectively. The measured VBO values are in close agreement with the calculated ones. The difference in VBO values between experimental and calculation may be due to the doping induced band gap narrowing effect in $GaAs_ySb_{1-y}$ layer. By comparing the effective tunneling barrier height for structures A and B, it can be seen that by increasing In alloy composition from 65% to 70% in $In_xGa_{1-x}As$ layer and simultaneously increasing Sb alloy composition from 60% to 65% in $GaAs_ySb_{1-y}$ layer to keep internally lattice matching with respect to each other, the $E_{beff}$ reduces from 0.30eV to 0.21eV. Thus, one can modulate the values of $E_{beff}$ at the mixed As/Sb based lattice matched heterojunctions ($GaAs_ySb_{1-y}/In_xGa_{1-x}As$) by carefully controlling both Sb and In compositions. As a result, the mixed As/Sb based material system is a preferred choice for TFET application as it provides a wide range of compositionally controlled $E_{beff}$.

The value of $E_{beff}$ can be drastically reduced at the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterojunction if the defects level is high. Figure 5.21 (c) shows the schematic band alignment of structure C where large amount of defects were confined at the interface as well as $In_{0.7}Ga_{0.3}As$ layer [2].

Note that the alloy compositions of In and Sb were the same as that in structure B except the higher defect density at the interface as well as in $In_{0.7}Ga_{0.3}As$ layer in structure C. One can find from Fig. 5.21 (c) [2] that the value of $E_{beff}$ is -0.03eV, suggesting a broken band lineup. It is interesting to note that the band alignment was converted from staggered gap (structure A or B) to broken gap (structure C) due to the presence of large amount of defects in structure C. Figure 5.21 (d) [2] summarizes the effective tunneling barrier height and the corresponding band alignment types of these three structures. Previously in ***Chapter 5.4***, it has been predicted by simulation that fixed positive charges induced by defects at the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterointerface would bend the energy band and reduces the value of $E_{beff}$ [4]. If the fixed charge density is large enough ($> 6\times10^{12}/cm^2$), it will assist the band alignment transition from staggered to broken gap in a mixed As/Sb heterostructure [4]. Thus, the experimental data corroborated with the simulation result and confirmed the band alignment conversion from staggered to broken gap lineup in a mixed As/Sb TFET heterostructure. Although, greater BTBT probability is expected in a broken gap TFET than staggered gap due to lower tunneling barrier, the OFF-state leakage will drastically increase due to the reduced blocking barrier at OFF-state. As a result, reducing defect density at the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ interface is indispensable to achieve a tailored-made tunneling barrier height and possess the staggered band alignment, without which the steep switching and higher $I_{ON}/I_{OFF}$ ratio of a TFET device would not be realized.

## 5.6 Transfer characteristics

The $E_{beff}$ of the $GaAs_ySb_{1-y}/In_xGa_{1-x}As$ heterostructure TFET can be modulated by changing Sb and In compositions in each side of the heterostructure, respectively, and different interface engineering will also change the $E_{beff}$ due to different dislocation densities. In order to assess the

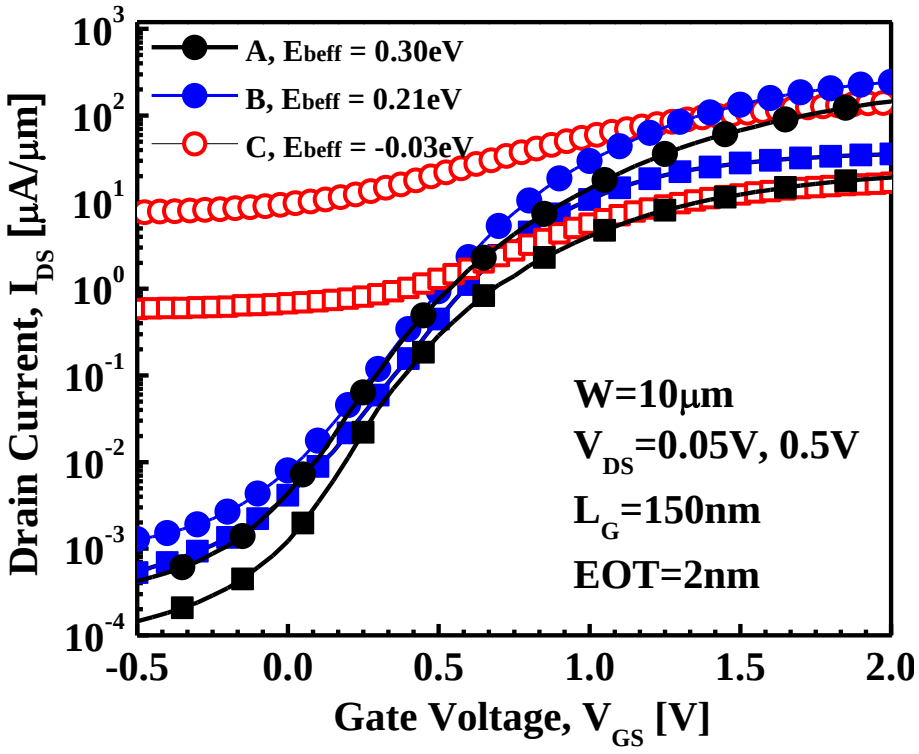


**Figure 5.22** Measured transferred characteristics ($I_d$-$V_g$) of TFET devices (L = 150nm, W = 10μm and EOT = 2nm) fabricated from structures A, B and C at $V_{DS}$ of 0.05 and 0.5V. The TFET B ($E_{beff}$ = 0.21eV) demonstrated 2× improvement in ON-state current compared with A ($E_{beff}$ of 0.30eV). About 4 orders of magnitude increase in OFF-state leakage current was observed from TFET C than B due to the reduction of $E_{beff}$ from 0.21eV to -0.03eV. [2] Used with permission of Nanotechnology Reviews.

impact of different effective tunneling barrier height and different band alignments on the transfer characteristics of TFET devices, three sets of TFET devices with self-aligned gates were fabricated and tested. Figure 5.22 [2] shows the room temperature transfer characteristics ($I_{DS}$-$V_{GS}$) of TFET devices fabricated from structure A, B and C as shown in Table 5.3 measured at $V_{DS}$ = 0.05V and 0.5V. By comparing the transfer characteristics of TFETs fabricated from structure A and B, it is observed that $I_{ON}$ increased by ~ 2× with the reduction in $E_{beff}$ from 0.30eV to 0.21eV. This is due to the reduced effective tunneling barrier height that enhances the tunneling transmission coefficient [12], which effectively increased BTBT rate and $I_{ON}$ current. Besides, the SS is also improved with reducing $E_{beff}$ due to the bandpass filter behavior cutting

off the high and low energy tail of the source Fermi distribution as a result of the particular band alignment condition [17]. In addition, the same tunneling current can be achieved at a lower applied gate voltage with a reduced $E_{beff}$, indicating that the low $E_{beff}$ TFET device is more suitable for low power operation. In contrast, the $I_{OFF}$ also increased due to the reduction of $E_{beff}$, and essentially, $I_{OFF}$ increased faster than $I_{ON}$ with the scaling of $E_{beff}$. This is due to the reduced $E_{beff}$ decreases the blocking barrier, which enhances both the BTBT probability and traps assisted tunneling process at OFF-state condition [6]. Furthermore, the bandgaps of source and channel materials also decreased with reducing $E_{beff}$ and a small energy gap leads to an additional increase of the OFF-state leakage due to more pronounced thermal emission process [18]. Therefore, a proper $E_{beff}$ with appropriate bandgap energy in source and channel layer should be selected in order to fulfill high $I_{ON}$ with desired $I_{ON}/I_{OFF}$ ratio.

By comparing transfer characteristics of the TFET devices from structure C with structure B, significant difference within $I_{ON}$ and $I_{OFF}$ was found between these two structures although the Sb and In composition in source and channel materials kept the same. About 4 orders of magnitude higher OFF-state leakage current was observed from the structure C than that from structure B due to higher defect density within the source/channel interface and channel/drain layers of structure C. The value of $I_{OFF}$ was extensively amplified due to the broken band alignment nature of structure C. In this case, the direct BTBT process dominates the OFF-state transport [4], which is different as the Shockley-Read-Hall recombination mechanism in the OFF-state transport of most staggered gap TFETs [4, 6]. An additional negative gate bias is required to turn off the OFF-state tunneling mechanism [18]. Besides, $I_{ON}$ of the TFET from structure C is smaller than that from structure B under the same applied voltage. It is due to the fact that higher degree of recombination occurs owing to trap centers caused by much greater

defect density in structure C. In addition, more than 4 orders in magnitude deterioration of $I_{ON}/I_{OFF}$ ratio was found in the TFET devices fabricated from structure C than structure B. The largely increased $I_{OFF}$ and degraded $I_{ON}/I_{OFF}$ ratio indicates that high defect density present at the source/channel interface that assists the transition of band alignment from staggered to broken gap. Measure must be taken to prevent the formation of large amount of defects at the critical heterointerface during the growth of mixed As/Sb heterostructure TFETs. Consequently, great efforts should be taken to preserve the staggered band alignment with low $E_{beff}$, otherwise, all performance improvement of TFET brought by $E_{beff}$ modulation will be in vain due to the band alignment transition.

## 5.7 MBE growth and interface engineering of InAs/GaSb broken gap structure

Further increase of ON-state current using mixed As/Sb material system implies the utilization of InAs/GaSb broken gap heterostructures. Compared with the InGaAs/GaAsSb staggered gap TFETs, the $E_{beff}$ is negative in the InAs/GaSb broken gap heterostructure, which indicates that there is no tunneling barrier for carriers transporting from source to channel. As a result, higher tunneling probability together with improved tunneling current is expected in broken gap TFET structures. However, it well known that there are great challenges to engineer high quality InAs/GaSb or GaSb/InAs heterointerface during MBE growth [10, 19]. At InAs/GaSb interfaces, both the cation and the anion change, in contrast to the common-cation InGaAs/GaAsSb system. As a result, there are two kinds of bond configurations possible: In-Sb bonds and Ga-As bonds, the mix depending on growth details, and leading to a technology dependent interface bond and defect configuration. The nature of the interface can be influenced by the shutter sequence during the crossover between the materials, with significant differences

between “upper” (GaSb on InAs) and “lower” (InAs on GaSb) interfaces [10]. Experimental studies have already reported the device failure in an InAs/GaSb broken gap TFET device due to improper switching sequence at the interface [20]. An additional interfacial GaAsSb layer was detected at the interface as indicated by XRD and TEM, which brings in high density of defects in this region, resulting in traps assistant tunneling and leading to high leakage current and degraded SS of the fabricated devices [20]. In this respect, it is necessary to perform a detailed study on the switching sequence of both the “upper” (GaSb on InAs) and “lower” (InAs on GaSb) interfaces for the MBE growth of InAs/GaSb heterostructures.

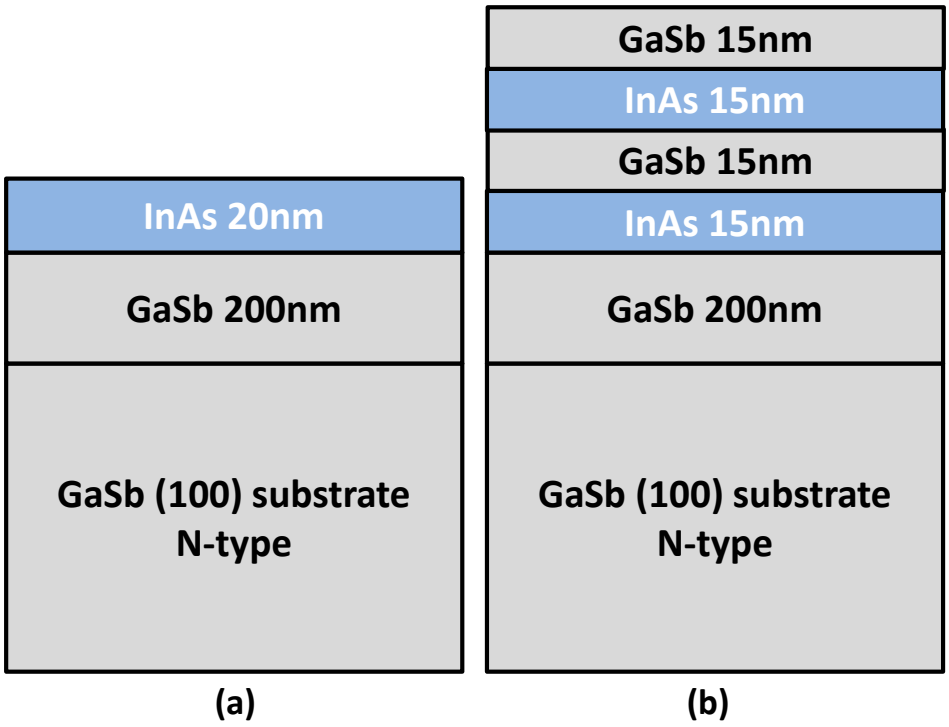


**Figure 5.23** Schematic diagrams of layer structures for (a) InAs/GaSb heterostructure and (b) GaSb/InAs/GaSb/InAs/GaSb mutil-heterostructures.

In the section, two structures comprise (a) InAs/GaSb heterostructure (referred as structure A) and (b) GaSb/InAs/GaSb/InAs/GaSb mutil-heterostructures (referred as structure B) were grown by solid source MBE on n-type GaSb (100) substrates. The oxide desorption was

performed under Sb ambient at 600$^{o}$C. For both structures, 200nm GaSb buffer layers were grown at 550$^{o}$C with a Sb/Ga ratio of 5. After that, 20nm InAs layer was deposited on GaSb on structure A and multi-heterostructures consisting 15nm GaSb/15nm InAs/15nm GaSb/15nm InAs was deposited on structure B with a substrate temperature of 550$^{o}$C. Different shutter sequences were used for the "upper" (GaSb on InAs) and "lower" (InAs on GaSb) interfaces. The Ga, Sb, In, and As shutter sequence for both heterointerface are shown in Fig. 5.24. For the "lower" interface, a 4s In and Sb overlap was used after the growth of GaSb bottom buffer and before the growth of InAs layer to intentionally form a InSb-like heterointerface. For the "upper" interface, a 6s exposure of Sb was used after the growth of InAs to remove the residual As atoms on the sample surface and to smooth the interface due to the surfactant effect of Sb atoms. The strain relaxation properties of these structures were characterized using high resolution x-ray diffraction (XRD). XRD rocking curves (RC, ω-2θ scan) and reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 as an x-ray source. The band alignment of InAs on GaSb was determined by x-ray photoelectron spectroscopy (XPS) using Kraut's [14] method as discussed in above sections.

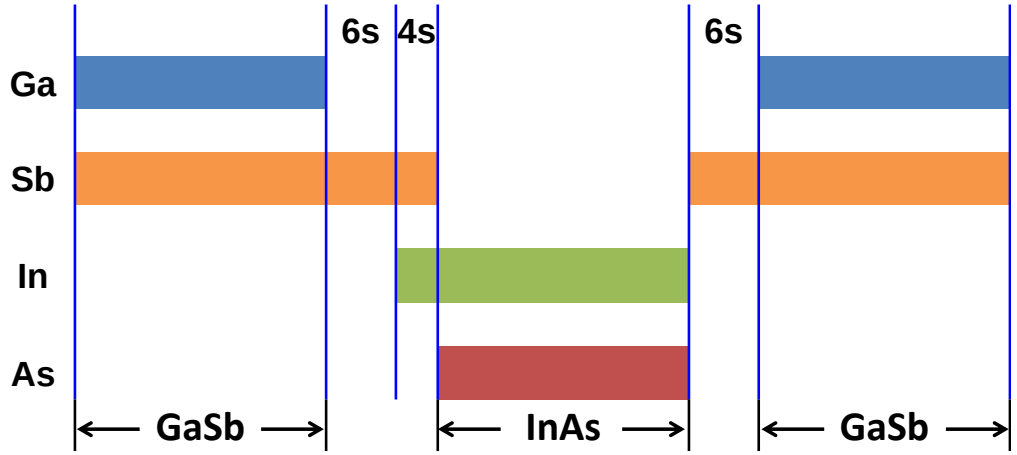


**Figure 5.24** Switching sequences for the InAs on GaSb and GaSb on InAs.

Figure 5.25 shows the RC of structure A from a symmetric (004) scan. Figure 5.26 (a) and (b) show the symmetric (004) RSM and RC of structure B, respectively. For both of these two structures, Pendellösung oscillation fringes appear on the RC and RSMs. The appearance of Pendellösung oscillation fringes on both sides of the GaSb substrate peak implies a parallel and very sharp heterointerface presents in this structure. This interference originates from the beating of x-ray wave fields generated at heterointerface as well as at sample surface. As a result, interference can only be observed in crystals that have almost perfectly parallel boundaries. Different as reported in Ref. 20, no additional interfacial peaks appear in both of these two structures, indicating abrupt interfaces with minimum atoms intermixing have formed. This abrupt heterointerface will reduce the tunneling distance of carriers from source to channel and reduce defects at the interface, both of which will upgrade the performance of devices fabricated from this structure. The band alignment of InAs on GaSb was measured by XPS using Kraut's method [14]. Figure 5.27 show the CL and VB XPS spectra obtained from 20nm InAs/GaSb, bulk GaSb and 5nm InAs/GaSb, respectively. Using the method discussed in ***Chapter 5.5***, the VBO of InAs with respect to GaSb is determined to be 0.52eV, which is higher than the bandgap energy of intrinsic InAs (0.36eV), indicating a broken gap band alignment is formed at the InAs/GaSb interface. The schematic band alignment of this heterostructure from XPS measurements is shown in Fig. 5.27 (G) with all measured parameters. The structural analysis of these two structures show that broken gap InAs/GaSb heterostructures with sharp interface and without interfacial layers were obtained by MBE using specific switching sequence for "upper" and "lower" interfaces. Further investigations are needed on the high-κ integration and device fabrication using these structures to fully utilize the benefit of high ON-current from broken band alignment for TFET applications. Furthermore, additional cares should be taken to avoid high

OFF-state leakage due to the normal ON properties of these TFET devices brought by the broken gap band alignment.

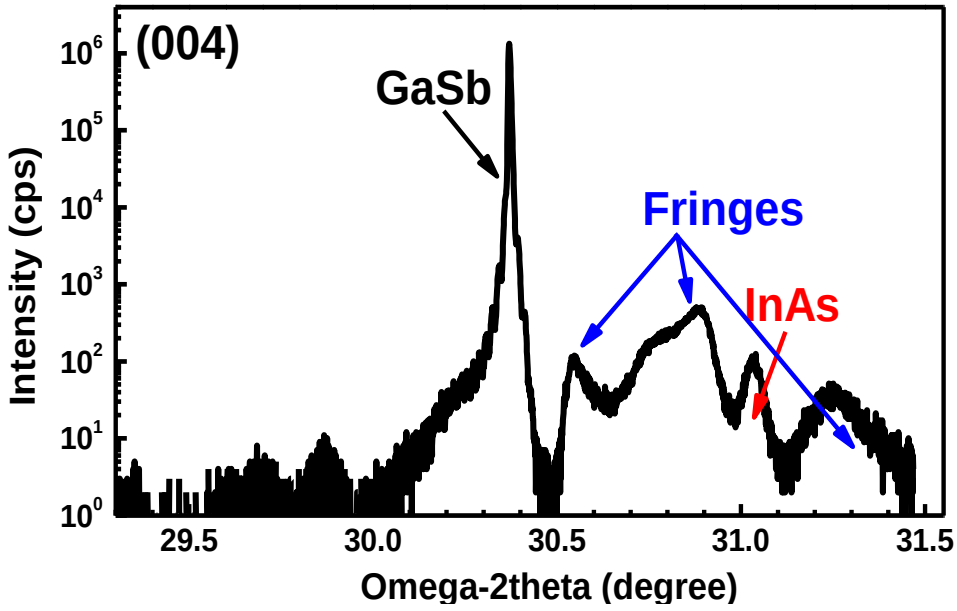


**Figure 5.25** (004) rocking curve of 20nm InAs grown on GaSb. No additional interfacial layers were detected.

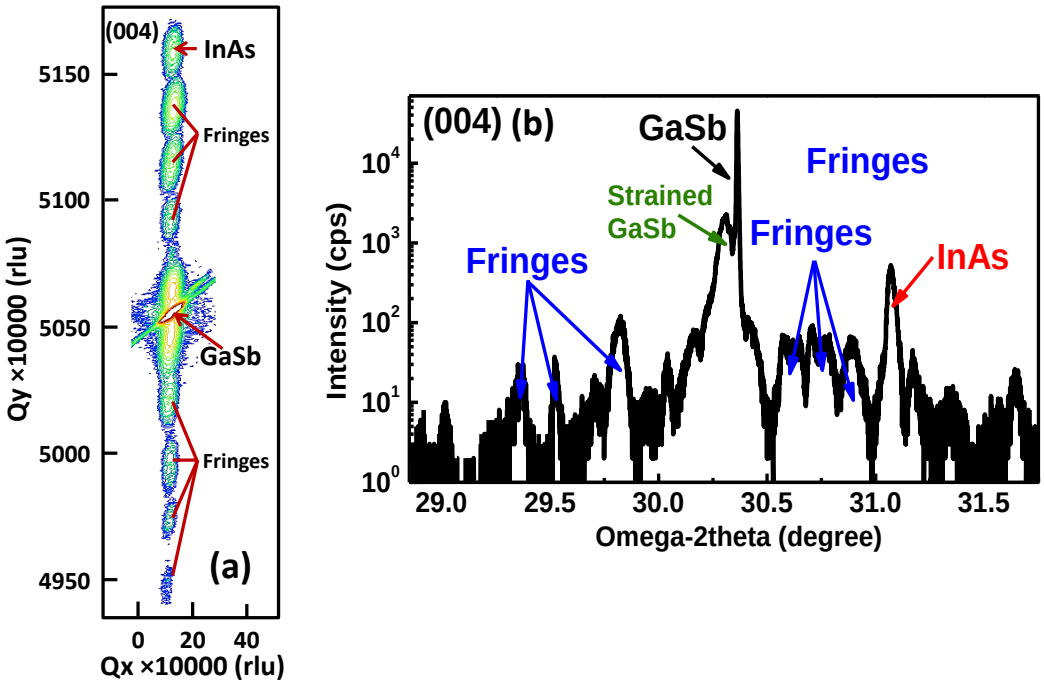


**Figure 5.26** (a) Symmetric (004) RSM and (b) (004) rocking curve of structure B. No additional interfacial layers were detected. The appearance of Pendellösung oscillation fringes on both sides implies a parallel and very sharp heterointerface presents in this structure.

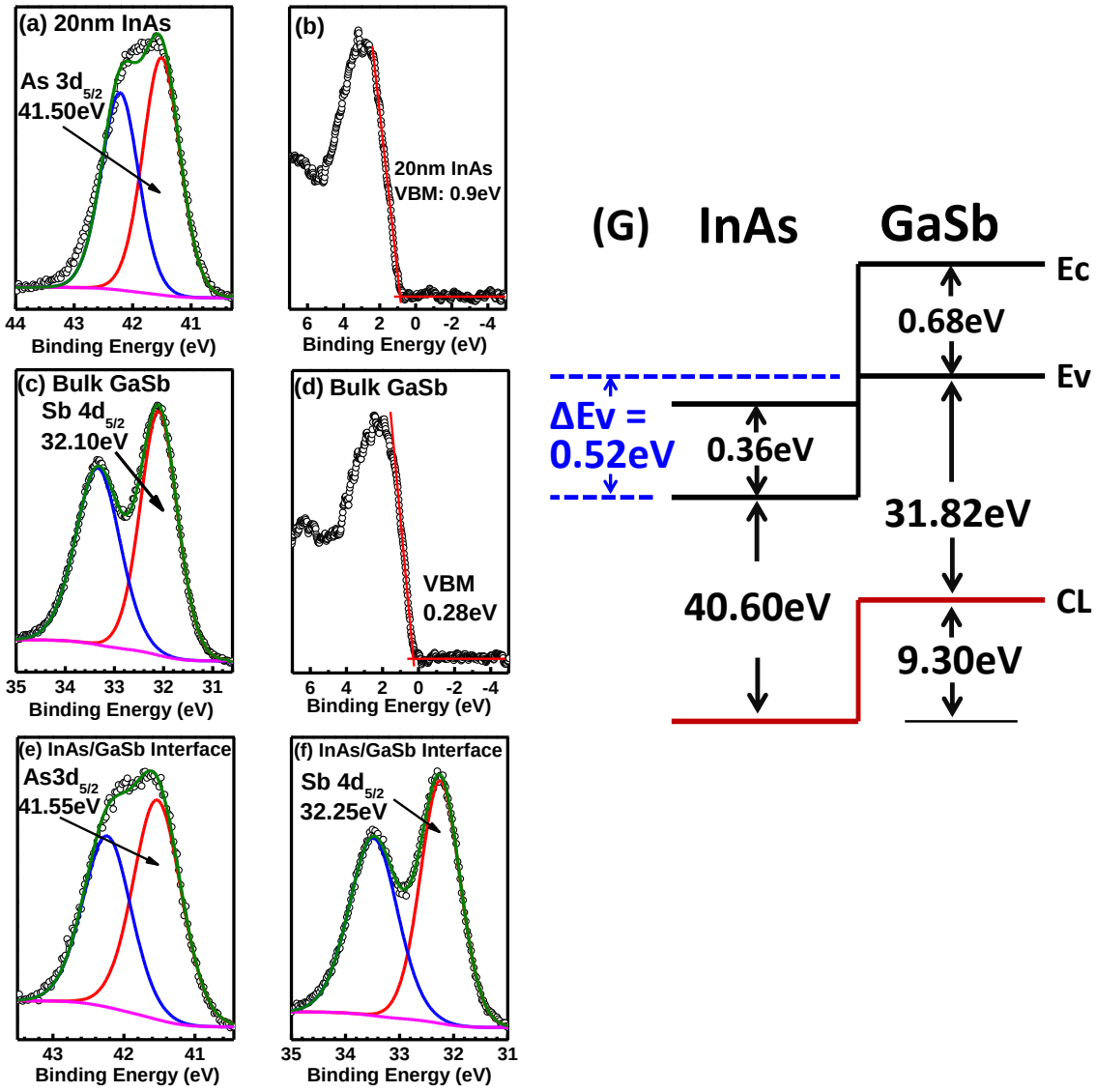


**Figure 5.27** XPS spectra of (a) $As3d_{5/2}$ core level (CL) and (b) InAs valence band (VB) from 20nm InAs on GaSb; (c) $Sb4d_{5/2}$ CL and (d) GaSb VB from bulk GaSb; (e) $As3d_{5/2}$ CL and (f) $Sb4d_{5/2}$ CL from 5nm InAs/GaSb structure measured at the heterointerface. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maxima (VBM) were determined by linearly fitting the leading edge of the VB spectra to the base line. (G) Schematic energy band diagram of InAs/GaSb heterostructure. A broken band lineup was confirmed in this structure.

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# Chapter 6 Reliability studies on high-temperature operation of mixed As/Sb staggered gap TFET material and devices

Due to the low standby voltage and steep SS, TFET is suitable for low-power applications with a supply voltage lower than 0.5V. In practice, there is a growing demand for TFETs to be integrated with other devices (e.g., CMOS, optical devices, detectors, *etc.*) for complex circuit applications. In that case, the performance of TFET may be impacted by other devices which can produce heat during operation in the working environment. This leads to the necessity for the transistors to be operated at high temperature working environment without degradation of the device performance. However, for the mixed As/Sb staggered gap TFET structures, due to large lattice mismatch between active layers ($GaAs_{1-y}Sb_y/In_xGa_{1-x}As$) and the substrate, there will be some residual strain exists within the active region [1]. The residual strain tends to relax during high temperature operation, which will generate dislocations in these layers. Furthermore, fixed charges caused by defects and dislocations at the heterointerface [1] will convert the energy band alignment from staggered gap to broken gap [2], which will drastically increase the $I_{OFF}$ and decrease $I_{ON}/I_{OFF}$ ratio [1]. Moreover, the high temperature operation may aggravate the intermixing of Sb and As at the $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ heterointerface that will result in uncontrolled layer composition, which will lead to uncontrolled band alignment and may introduce high dislocation density due to compositional mismatch. Besides, high temperature operation may lead to decrease in bandgap of materials in the active layers as well as increase in channel resistance [3, 4], both of which will influence the ON-state performance of TFET devices [5]. Furthermore, due to the enhanced Shockley-Read-Hall (SRH) generation-recombination (G-R) and the increased TAT process during high temperature operation [6, 7, 8],

$I_{OFF}$ may be significantly increased compared with that at room temperature. Therefore, it is necessary to experimentally investigate the reliability of mixed As/Sb staggered gap heterojunction TFET materials and devices for high temperature operation. In this chapter, both the structural properties and device performances of a $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ staggered gap TFET is studied in the temperature range of 25°C to 150°C. The schematic layer structure of this TFET structure is shown in Fig. 6.1 (a). The simulated band structure is shown in Fig. 6.1 (b). The reliability studies of high-temperature operation of mixed As/Sb staggered gap tunnel FET material and devices will contribute to better understanding the operation principles within these devices at high operating temperature and will provide important guidance on the material growth optimization and device fabrication for future TFETs.

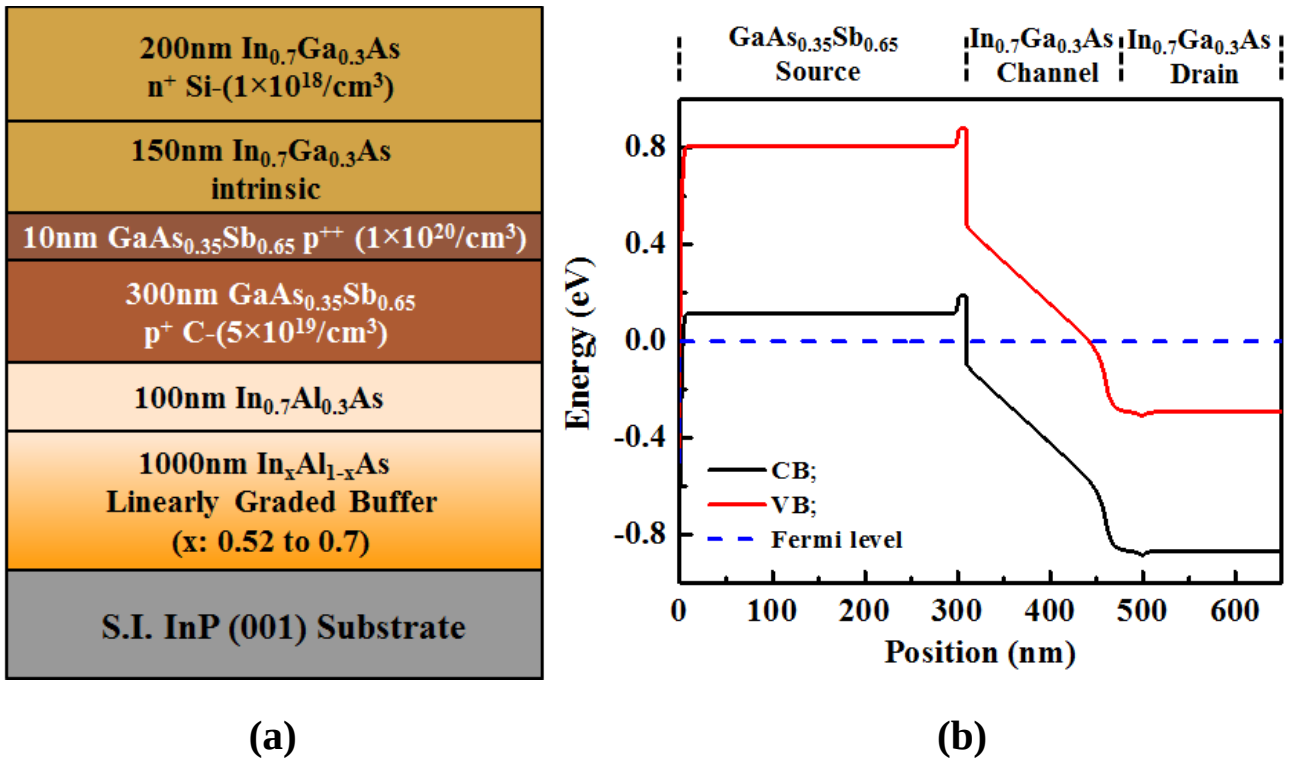


**Figure 6.1** (a) Schematic diagram of n-channel TFET layer structure. (b) Energy band diagram of the structure. The 10nm $p^{++}$ heavily C doped GaAsSb layer is clearly shown in the band diagram. [7] Used with permission from IEEE.

## 6.1 Strain relaxation properties at high operation temperature

The relaxation state and residual strain of epilayers at each temperature step were obtained from symmetric (004) and asymmetric (115) reflections of RSMs of the structure as shown in Fig. 6.1 (a). Figures 6.2 (a) and (b) showed symmetric (004) and asymmetric (115) RSMs of the structure at different temperatures steps, respectively. Each layer was labeled to its corresponding reciprocal lattice point (RLP) based on wet chemical etching experiments as described in detail in reference [1]. It can be seen from Fig. 6.2 (a) and (b) [7] that four distinct RLP maxima were shown in symmetric (004) and asymmetric (115) RSMs at each temperature step, the same as described in ***Chapter 5.3.1***. Analysis were performed at each temperature step using the symmetric (004) and asymmetric (115) RSMs. Similar strain relaxation values at each temperature step (~ 75% for $In_{0.7}Ga_{0.3}As$, ~ 82% for $GaAs_{0.35}Sb_{0.65}$ and ~ 72% for $In_{0.7}Al_{0.3}As$) as those at 25$^{o}$C from each epilayer respect to InP substrate were extracted. The calculated strain relaxation values were summarized in Table 6.1. The nearly identical strain relaxation states of each epilayer at different temperature steps indicate that the pseudomorphic nature of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ layers were well maintained and negligible residual strain was relaxed during the high temperature operation. It also indicates that no extra dislocations caused by strain relaxation should be expected during high temperature operation up to 150$^{o}$C. The similar strain relaxation state of each epilayer during high temperature operation is supported by comparing the position of each RLP with respect to the fully relaxed line (the red dashed line) in (115) RSMs at different temperature steps. As shown in Fig. 6.2 (b) [7], almost the same distance from the center of each RLP to the fully relaxed line was observed at different temperature, indicating nearly identical strain relaxation states of each layer.

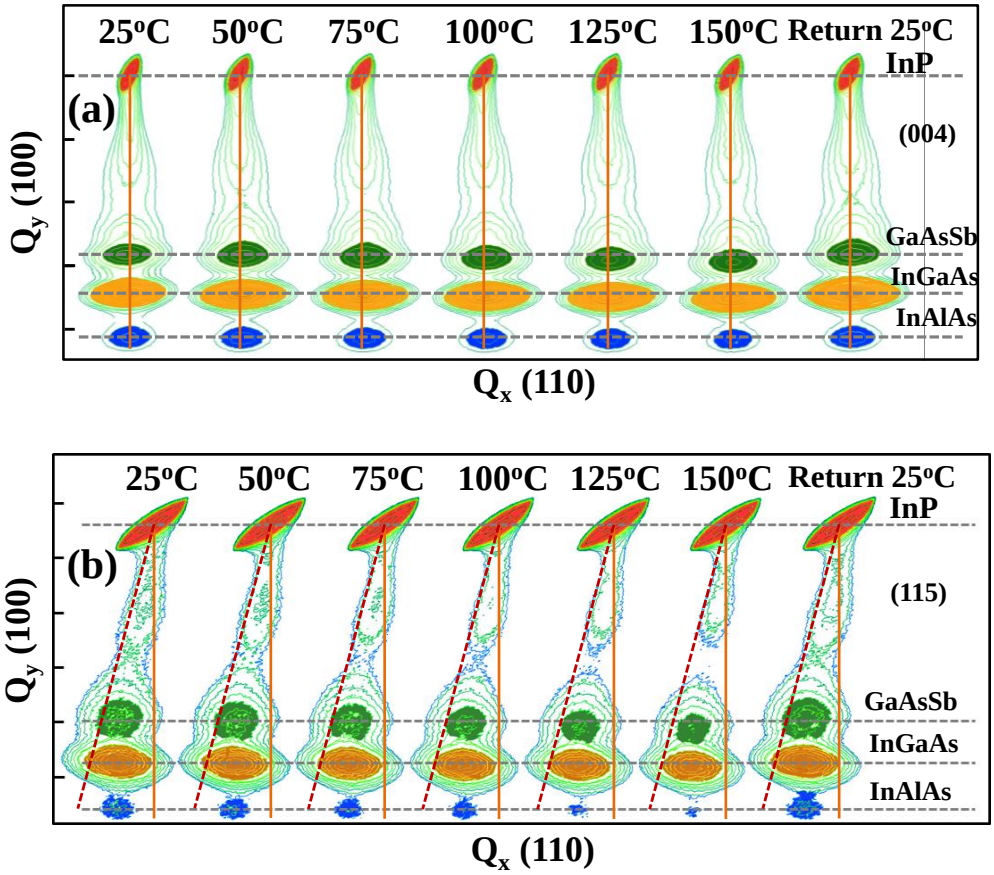


**Figure 6.2** (a) Symmetric (004) and (b) asymmetric (115) reciprocal space maps of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure at different temperature. Similar strain relaxation values were extracted from RSMs at different temperatures, indicating the strain relaxation properties of this structure keep stable up to 150°C. [7] Used with permission from IEEE.

It can also be seen from Fig. 6.2 (a) [7] that the RLPs of epilayers were marginally moving away from the InP substrate with increasing temperature. This may be caused by the lattice constant change at higher measurement temperature. The change of lattice parameter of each epilayer recovered after the sample was cooled down to room temperature, which can be confirmed by the RSMs recorded after the temperature cycle. The intensity of each RLP was decreased at high temperature and it was caused by the small displacements of atoms due to thermal vibrations [9]. In fact, the reduction of intensity was recovered when the sample was cooled down to room temperature after temperature cycle. Furthermore, the identical features of

(004) and (115) RSMs before and after the temperature cycle measured at 25$^{o}$C indicate that the strain relaxation properties of this structure does not affect by the high temperature operation up to 150$^{o}$C.

## 6.2 Surface morphology before and after high temperature operation

The 10μm×10μm AFM micrographs of the TFET structure before and after temperature cycle were shown in Fig. 6.3 (a) and (b) [7], respectively. From Fig. 6.3 (a) and (b) [7], the anticipated two-dimensional crosshatch patterns were well developed and quite uniform, as expected for ideal graded buffer [10, 11], from both surfaces before and after high temperature operation. The well maintained two-dimensional crosshatch patterns and similar surface morphology after the high temperature cycle suggests that the strain within the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ layers were not relaxed during the high temperature operation. Otherwise, dislocations would be formed in these layers and the 2-D crosshatch pattern developed by the graded buffer will be sheltered by high density dislocations and a grainy texture with higher surface roughness will be expected [1]. The surface *rms* roughness before and after temperature cycle were measured to be 3.17nm and 2.66nm, respectively. Despite of the experimental error, the surface was smoother after high temperature operation. Similar improvements of crystalline quality by high temperature annealing on metamorphic structures were also reported by other researchers where the lattice reformation might have resulted in the improvements in the structural quality [12, 13, 14]. In this case, although the annealing temperature was limited to 150$^{o}$C, the sample was kept at the specific temperature for long time (~ 2 hours) during the collection of RSMs data at each temperature step. The annealing temperature was not set high to relax the residual strain within the epilayers, however, some defects (i.e., point defects) might have annihilated during the long annealing duration by the

redistribution of atoms and hence improve the surface morphology. In fact, the improvement of crystalline quality by reduction of defects was also confirmed by the decrease of the $p^+$-i-$n^+$ leakage current of the fabricated TFET devices, which will be disused in **Sec. 6.4**.

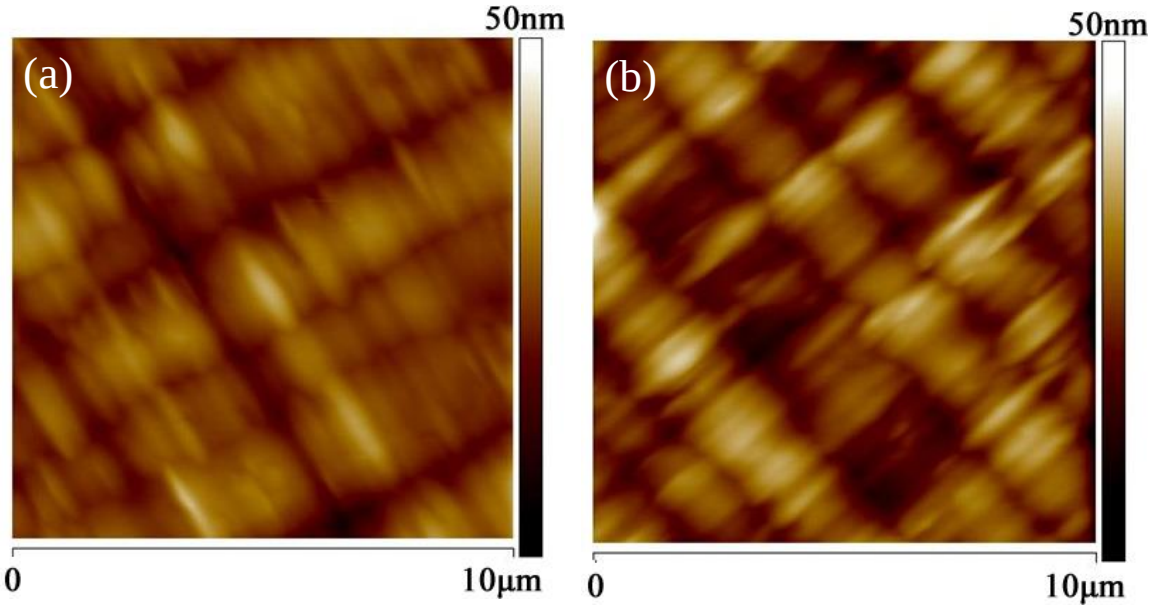


**Figure 6.3** 10μm × 10μm AFM surface morphology of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure (a) before temperature cycle with *rms* roughness of 3.17nm and (b) after temperature cycle with *rms* roughness of 2.66nm. Typical crosshatch patterns were observed in both cases. The well maintained crosshatch pattern and similar surface morphology after the temperature cycle suggests no significant structural properties change was generated in the structure up to 150°C. [7] Used with permission from IEEE.

## 6.3 Atoms inter-diffusion before and after high temperature operation

There could be a potential concern of the mixed As/Sb staggered gap TFET devices for high temperature operation due to the possible intermixing between As and Sb atoms at the source/channel heterointerface. The intermixing between different atoms will be more promoted at higher temperature due to the enhanced ad-atoms diffusion. Besides, high temperature operation may also cause the diffusion of dopant atoms (C) from heavily doped $GaAs_{0.35}Sb_{0.65}$ source to the intrinsic $In_{0.7}Ga_{0.3}As$ channel layer. This will reduce the abruptness of the doping

profile at the tunnel junction, which will in turn reduce the tunneling probability and lead to decrease in $I_{ON}$ of the TFET devices [5, 6]. In order to determine the influence of high temperature operation on the junction and doping profiles of the TFET structure, dynamic SIMS measurements were performed to characterize the compositional profiles of As, Sb, Ga, In, Si and C atoms at the interface before and after temperature cycle. Figure 6.4 (a) [7] showed Ga, In, As and Sb depth profiles of the TFET structure before temperature cycle, which displayed an abrupt $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. The transition between $GaAs_{0.35}Sb_{0.65}$ to $In_{0.7}Ga_{0.3}As$ was less than 10nm, within the sputter-induced broadening of the ion beam, indicating low value of As and Sb intermixing at the heterointerface. Figure 6.4 (b) [7] showed the C and Si doping profiles in the source and drain regions of the TFET structure. It depicted an abrupt junction profile at the source/channel interface with an expected C pocket doping concentration of $\sim 1 \times 10^{20}/cm^3$. Similarly, the Ga, In, As, Sb depth profiles and C, Si doping profiles after the temperature cycle were shown in Fig. 6.5 (a) and (b) [7], respectively. Almost identical, sharp junction and abrupt doping profile as that before the temperature cycle were obtained, which indicated that no detectable intermixing was taken place within the heterointerface up to $150^oC$. The stability of junction profiles assured the anticipated staggered band alignment with desired effective tunneling barrier height ($E_{beff}$) and sharp tunnel junction interface with minimal tunneling width for the TFET to operate at high temperature.

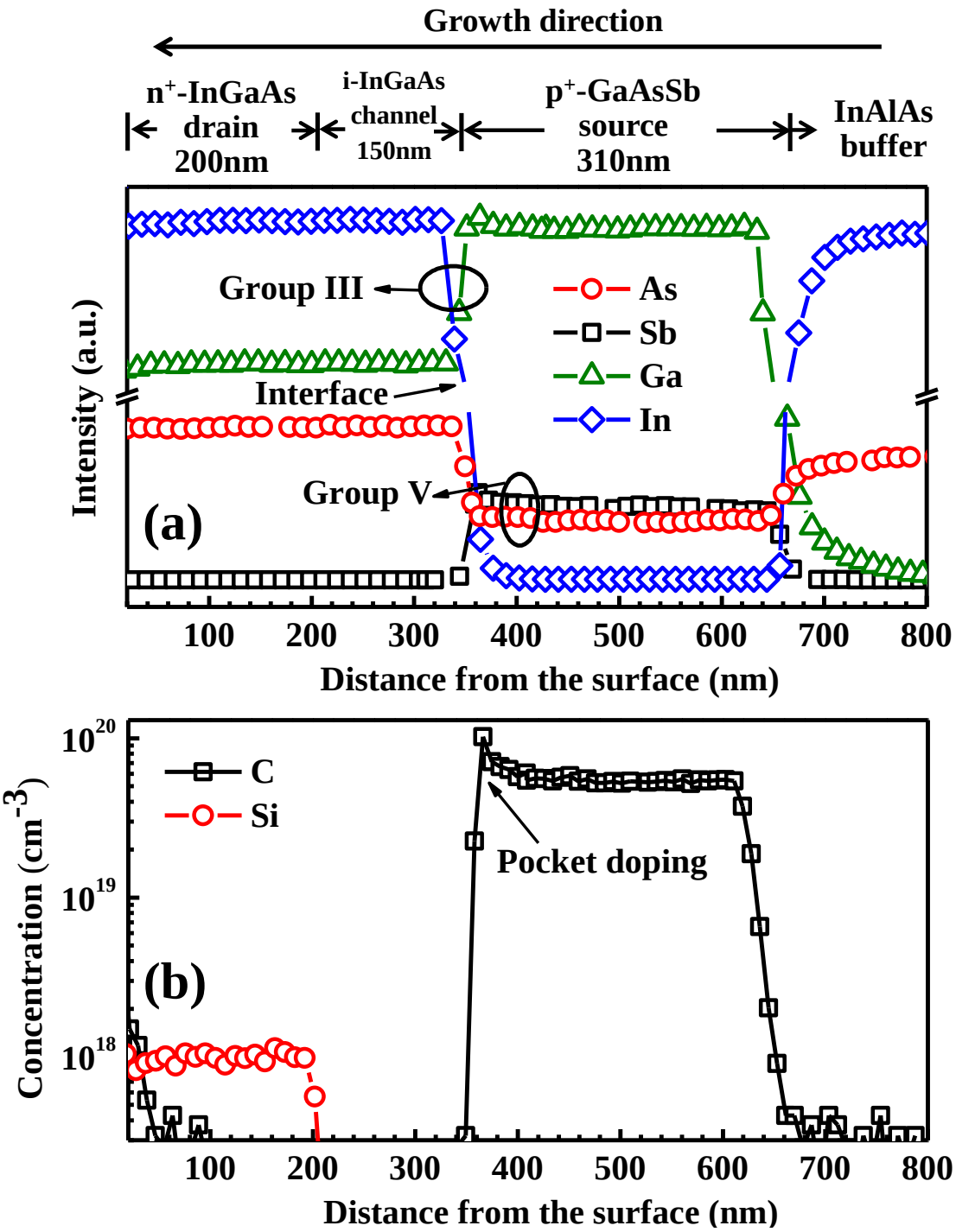


**Figure 6.4** (a) Dynamic SIMS depth profiles of Ga, In, As and Sb of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure before temperature cycle. An abrupt $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface with a transition less than 10nm was confirmed. (b) Doping concentration profiles of C in the source and Si in the drain region before temperature cycle. An abrupt doping profile was observed at the interfaces. [7] Used with permission from IEEE.

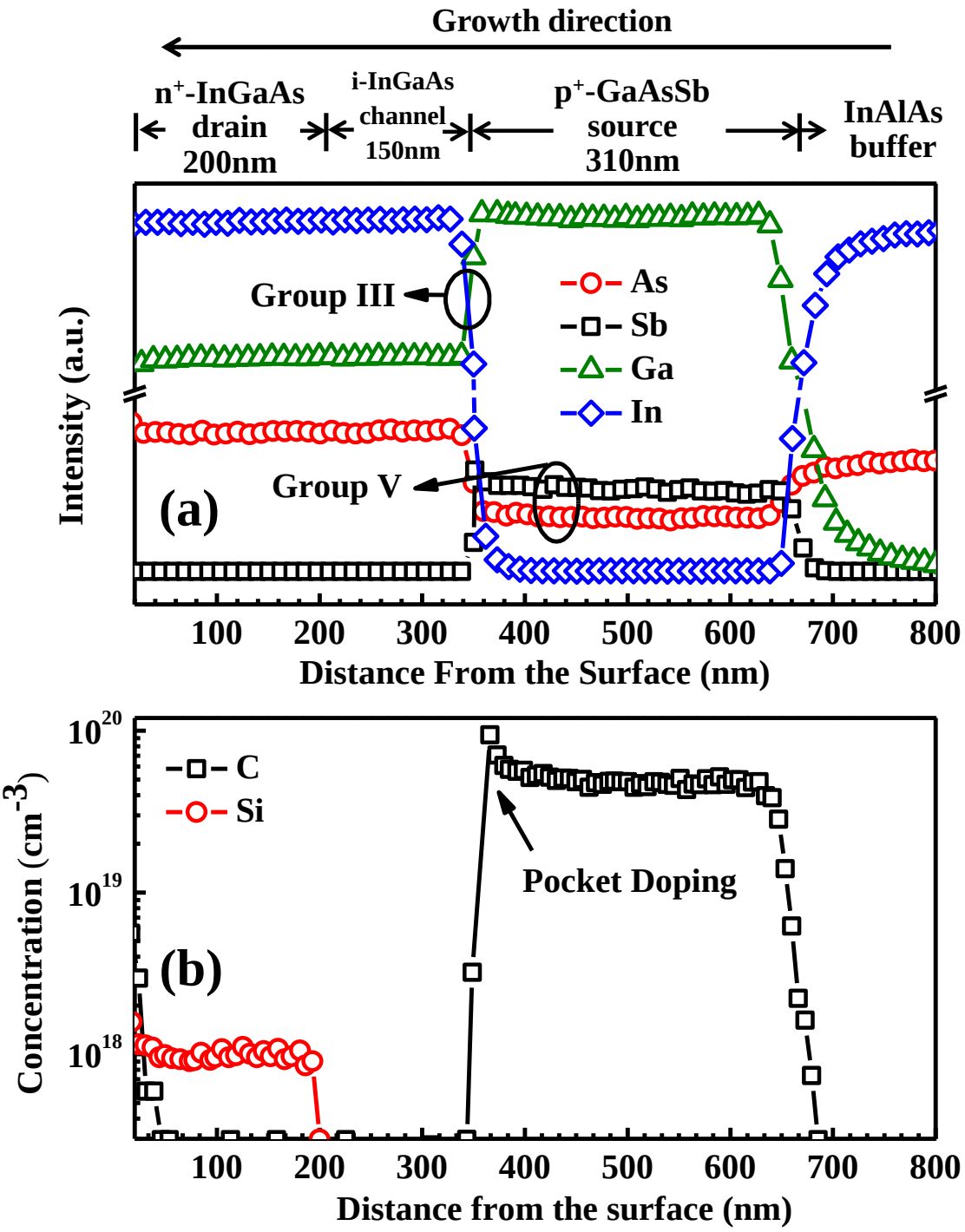


**Figure 6.5** (a) Dynamic SIMS depth profiles of Ga, In, As and Sb of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure after temperature cycle. (b) Doping concentration profiles of C in the source and Si in the drain region after temperature cycle. The junction and doping profiles were similar as those before temperature cycle, indicating no detectable intermixing was taken place within the heterointerface up to 150°C. [7] Used with permission from IEEE.

## 6.4 OFF-state performances at high operation temperature

Temperature dependent I-V measurements were carried out on the reverse-biased $p^+$-i-$n^+$ diode with temperature ranging from 25°C to 150°C with 25°C as a step. Besides, the measurement was repeated at 25°C on the same device after the temperature cycle to determine the influence of the temperature cycle on the OFF-state performance. Figure 6.6 (a) [7] showed the measured leakage current of the reverse-biased $p^+$-i-$n^+$ diode at different temperature steps. It can be seen from this figure that at each fixed reverse-bias, the leakage current increased exponentially with increasing temperature, as expected. The variation tendency of $I_{OFF}$ with temperature was consistent with the SRH-dominated OFF-state transport mechanism, within which the main contribution to the temperature dependent factor arises from the intrinsic carrier concentration which is proportional to $\exp(-E_G/2kT)$, where $E_G$ is the bandgap energy of active layers materials, k is the Boltzmann constant, and T is the temperature. In order to confirm this proposition, numerical simulations were performed using a SRH G-R model to determine the OFF-state transport of the TFET device. All simulations were performed using Sentaurus [15] with temperature ranging from 25°C to 150°C. As shown in Fig. 6.6 (a) [7] (solid lines), the simulated I-V characteristics of the reverse-biased $p^+$-i-$n^+$ diode is in agreement with the measured data (scattered line) at all temperatures, suggesting the validation of this model. The SRH-dominated OFF-state transport mechanism was also confirmed by the Arrhenius plot, shown in Fig. 6.6 (b) [7]. The extracted activation energy is 0.33eV, 0.35eV, and 0.36eV at a reverse-bias of 1V, 0.5V, and 0.1V, respectively. All of these values were approximately $E_G/2$ of $In_{0.7}Ga_{0.3}As$ (~ 0.6eV at 300K) and $GaAs_{0.35}Sb_{0.65}$ (~ 0.72eV at 300K), indicating $I_{OFF}$ components of SRH G-R were from both mid-gap interface traps and mid-gap bulk traps.

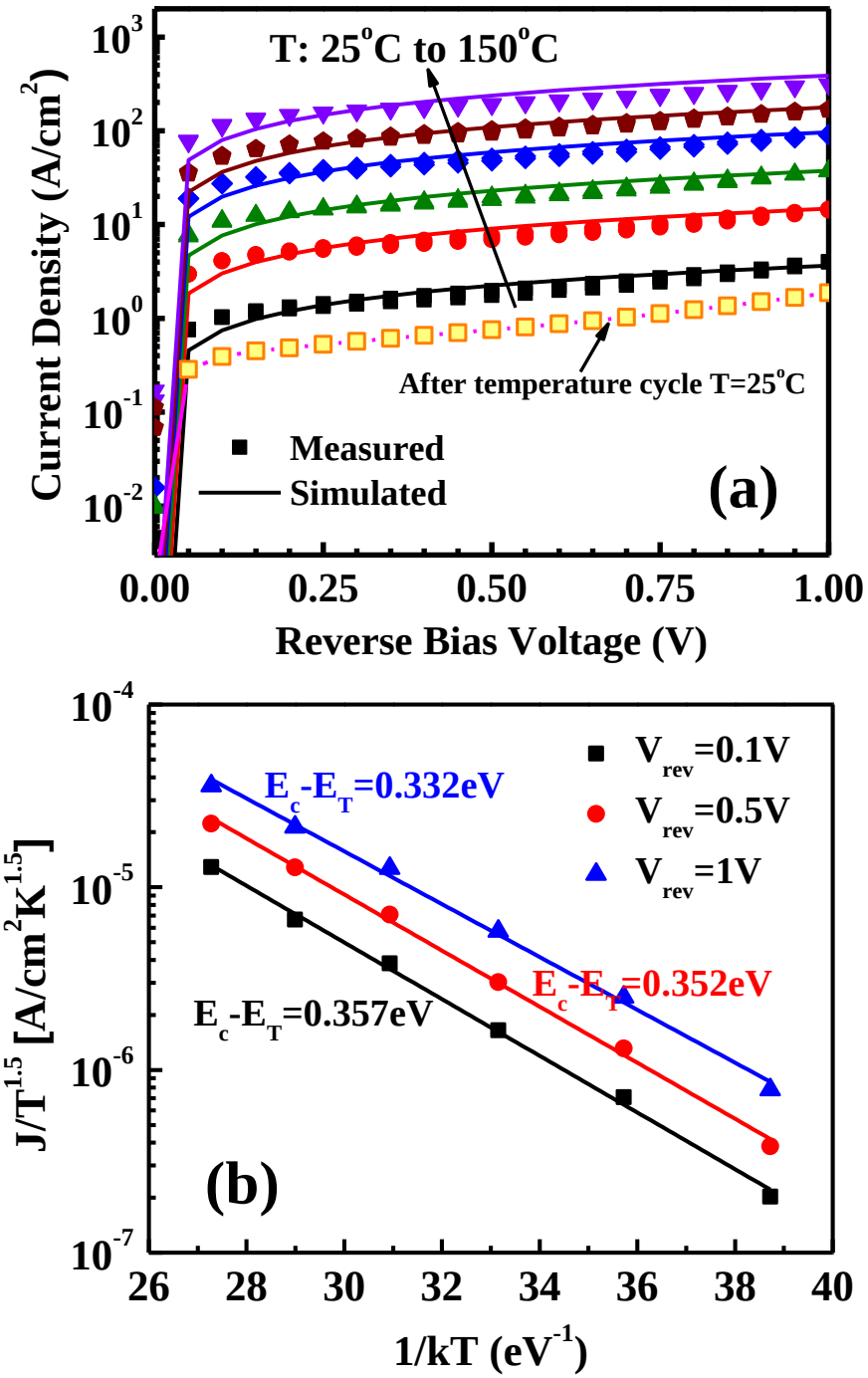


**Figure 6.6** (a) Measured and simulated I-V characteristics of the reverse-biased $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ $p^+$-i-$n^+$ diode with temperature ranging from 25°C to 150°C and (b) an extraction of the activation energy for the leakage current. The activation energy was between $E_G/2$ of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, indicating SRH G-R from both mid-gap interface traps and mid-gap bulk traps dominate the OFF-state transport of the TFET devices. [7] Used with permission from IEEE.

It is interesting to find that the room temperature leakage current of the reverse-biased $p^+$-i-$n^+$ diode was reduced by almost 2× after the temperature cycle. This may be due to removal of some deep level traps during high temperature operation. The G-R centers in the mid-gap of bulk materials and within the depletion region of each junction were reduced by atom reformation in the long duration of temperature cycle [14], which will reduce the contribution of SRH G-R current. The improvement of crystalline quality can also be supported by the reduction of *rms* roughness after temperature cycle discussed earlier.

## 6.5 Transfer characteristics at high operation temperature

In order to gain insight into the switching properties of the mixed As/Sb staggered gap TFETs at high operating temperature, transfer characteristics of these TFET devices were measured at both $V_{DS}$ = 0.05V and 0.5V from 25$^o$C to 150$^o$C using 25$^o$C as a temperature step. Figure 6.7 (a) [7] showed the transfer characteristics of the TFET device measured at $V_{DS}$ = 0.05V with different temperature. As shown in this figure, at low gate voltages (<-0.3V), the drain current was almost constant without gate modulation, which set the leakage floor of the device, and increased exponentially with rising temperature. With increasing gate voltages from -0.3V to 0.4V, the $I_{DS}$ was less temperature dependent, which indicated that the BTBT current was becoming the dominant current component. For $V_{GS}$ > 0.4V, $I_{DS}$ is weak temperature dependent and it corresponds to the drive current ($I_{DR}$) of the TFET. In order to further study the impact of high operating temperature on $I_{DR}$, the $I_{DS}$-$V_{GS}$ characteristics was re-plotted in a linear scale with $V_{GS}$ from 1.0V to 1.5V, which was shown in Fig. 6.7 (b) [7]. As shown in Fig. 6.7 (b), $I_{DR}$ has a weak temperature dependent characteristics corresponding to the BTBT current at ON-state condition. The inset of Fig. 6.7 (b) [7] shows the changing trend of $I_{DS}$ with temperature at $V_{GS}$ = 1.5V. It is interesting to find that $I_{DS}$ was decreasing with rising temperature from 25$^o$C to

100°C, but increasing from 100°C to 150°C. The former trend of $I_{DS}$ can be explained by the variation of channel resistance with temperature and the latter can be explained by the reduction of bandgap energy of active region materials as well as the decrease of effective tunneling barrier height. According to Knoch *et al.* [16], the tunnel junction acts as a band-pass filter allowing only carriers with energies around the Fermi level in an energy window ΔΦ (as shown in Fig. 1.3 (b) and (c)) to tunnel from source to channel. With increasing temperature, the increase of channel resistance will result in the reduction of drain current. Moreover, the source region of TFET is highly degenerated due to heavily p-type doping. Thus, the degeneracy reduces the number of electrons available for tunneling which reduces the ON-state current and degraded the SS [17, 18]. In addition, due to the temperature dependence of the Fermi tail caused by heavily p-type doping, the degradation of ON-state current will be more pronounced at high temperature that leads to additional ON-state current loss. However, at higher temperature of greater than 100°C, the energy window ΔΦ will be enlarged by the decrease of bandgap energies of the source/channel materials [4]. Furthermore, according to Kane's model [19] (also shown in Eq. 1.8), the $I_{DR}$ of TFET is directly related to the BTBT generation rate $G_{BTBT}$, which is exponentially related to $-(E_G)^{3/2}$. The exponential factor of $E_G$ predominantly determines the $G_{BTBT}$ on $E_G$ and contributes to the increase of $I_{DR}$ with rising temperature from 100°C to 150°C. The increased $I_{DR}$ due to reduction of $E_G$ of active region materials may dominant over variation of Fermi distribution from 100°C to 150°C. In addition, the $E_{beff}$ will also reduce due to the reduction of bandgap [6], which may provide extra increase in $I_{DR}$ at higher temperature of operation.

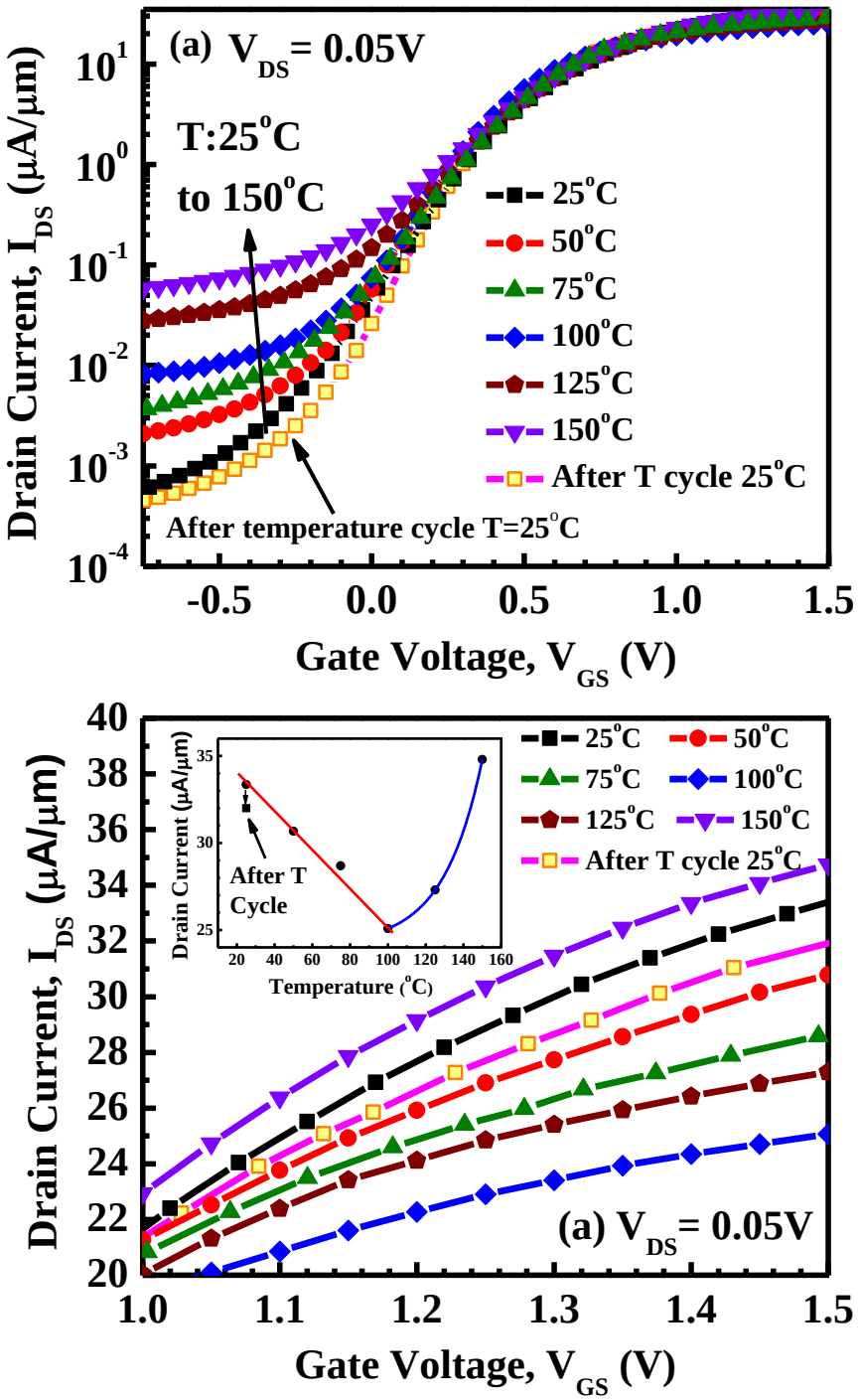


**Figure 6.7** (a) Transfer ($I_{DS}$-$V_{GS}$) characteristics of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET devices at $V_{DS}$ = 0.05V with $I_{DS}$ in a log scale from 25°C to 150°C. (b) $I_{DS}$ ($V_{GS}$ from 1.0V to 1.5V) of the TFET devices at $V_{DS}$ = 0.05V with $I_{DS}$ in a linear scale from 25°C to 150°C. The inset shows the changing trend of $I_{DS}$ with temperature at $V_{GS}$ = 1.5V. $I_{DS}$ decreases from 25°C to 100°C due to the variation of Fermi distribution with temperature but increases from 100°C to 150°C due to the reduction of $E_G$. [7] Used with permission from IEEE.

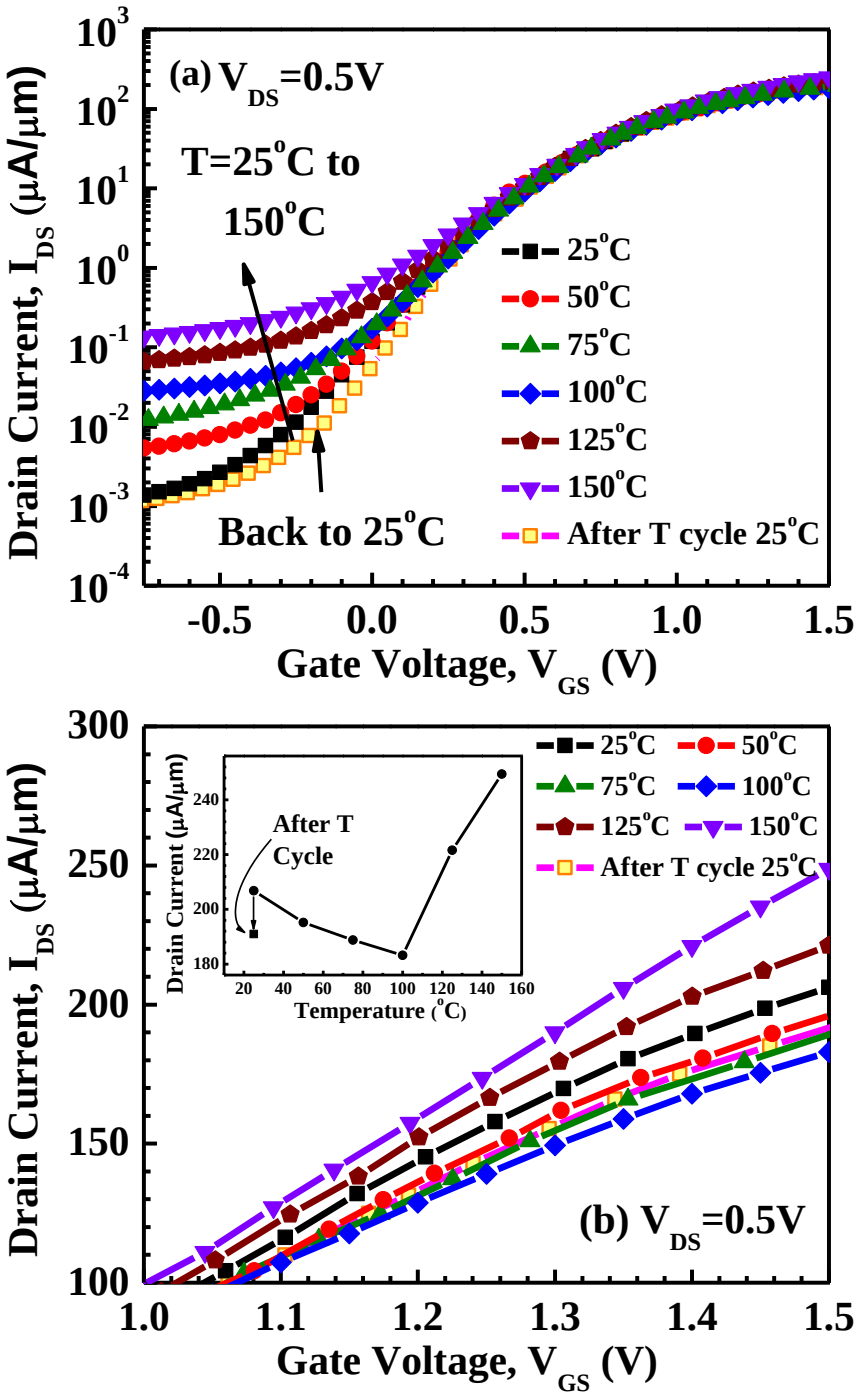


**Figure 6.8** (a) Transfer ($I_{DS}$-$V_{GS}$) characteristics of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET devices at $V_{DS}$ = 0.5V with $I_{DS}$ in a log scale from 25°C to 150°C. (b) $I_{DS}$ ($V_{GS}$ from 1.0V to 1.5V) of the TFET devices at $V_{DS}$ = 0.5V with $I_{DS}$ in a linear scale from 25°C to 150°C. The inset shows the changing trend of $I_{DS}$ with temperature at $V_{GS}$ = 1.5V. Similar $I_{DS}$ changing trend with temperature was observed as that with $V_{DS}$ = 0.05V. [7] Used with permission from IEEE.

Figure 6.8 (a) [7] shows the transfer characteristics of the same TFET device measured at $V_{DS}$=0.5V with different temperature. As shown in this figure, $I_{DR}$ is about 1 order higher than that with $V_{DS}$=0.05V (as shown in Fig. 6.7 (a)), as expected, at each temperature step, which is due to the enhanced electrical field at the tunneling junction brought by higher drain voltage. Similarly, at $V_{DS}$=0.5V, the OFF-state leakage floor showed strong temperature dependence and the $I_{DR}$ displayed weak temperature dependence, which indicate that the SRH G-R mechanism and the BTBT processes, respectively, dominated the OFF-state and ON-state transport of the TFET device. In order to gain better insight into the impact of temperature on $I_{DR}$, the $I_{DS}$-$V_{GS}$ characteristics of the TFET device was re-plotted in Fig. 6.8 (b) [7] with $V_{GS}$ from 1.0V to 1.5V in a linear scale. The inset of Fig. 6.8 (b) [7] shows the changing trend of $I_{DS}$ with temperature at $V_{GS}$ = 1.5V. Nearly identical changing trend of $I_{DR}$ with temperature at $V_{DS}$ = 0.5V and $V_{DS}$ = 0.05V was obtained, indicating that the temperature has similar effect on the transport mechanism at 0.05V and 0.5V drain voltages. The $I_{DS}$ is not increasing exponentially with temperature from 100$^{o}$C to 150$^{o}$C, different with the case of $V_{DS}$=0.05V. This might be due to an enhanced electrical field inside the channel brought by the higher drain voltage. Moreover, the enhanced electrical field leads to a larger voltage drop over the channel due to increased channel resistance at a higher temperature of >100$^{o}$C. As a result, the exponential increase trend of $I_{DS}$ dominated by the reduction of $E_G$ is not as remarkable as that with $V_{DS}$ = 0.05V. Furthermore, the $I_{DS}$-$V_{GS}$ measurements on the same device at 25$^{o}$C showed similar performance before and after temperature cycle operation both at $V_{DS}$ = 0.05V and 0.5V. It also suggests that no significant structural properties change, such as strain relaxation, inter-diffusion *etc.*, took place during high temperature operation up to 150$^{o}$C within the TFET structure. The $I_{OFF}$ of the TFET device was reduced after the temperature cycle due to the removal of some trap states.

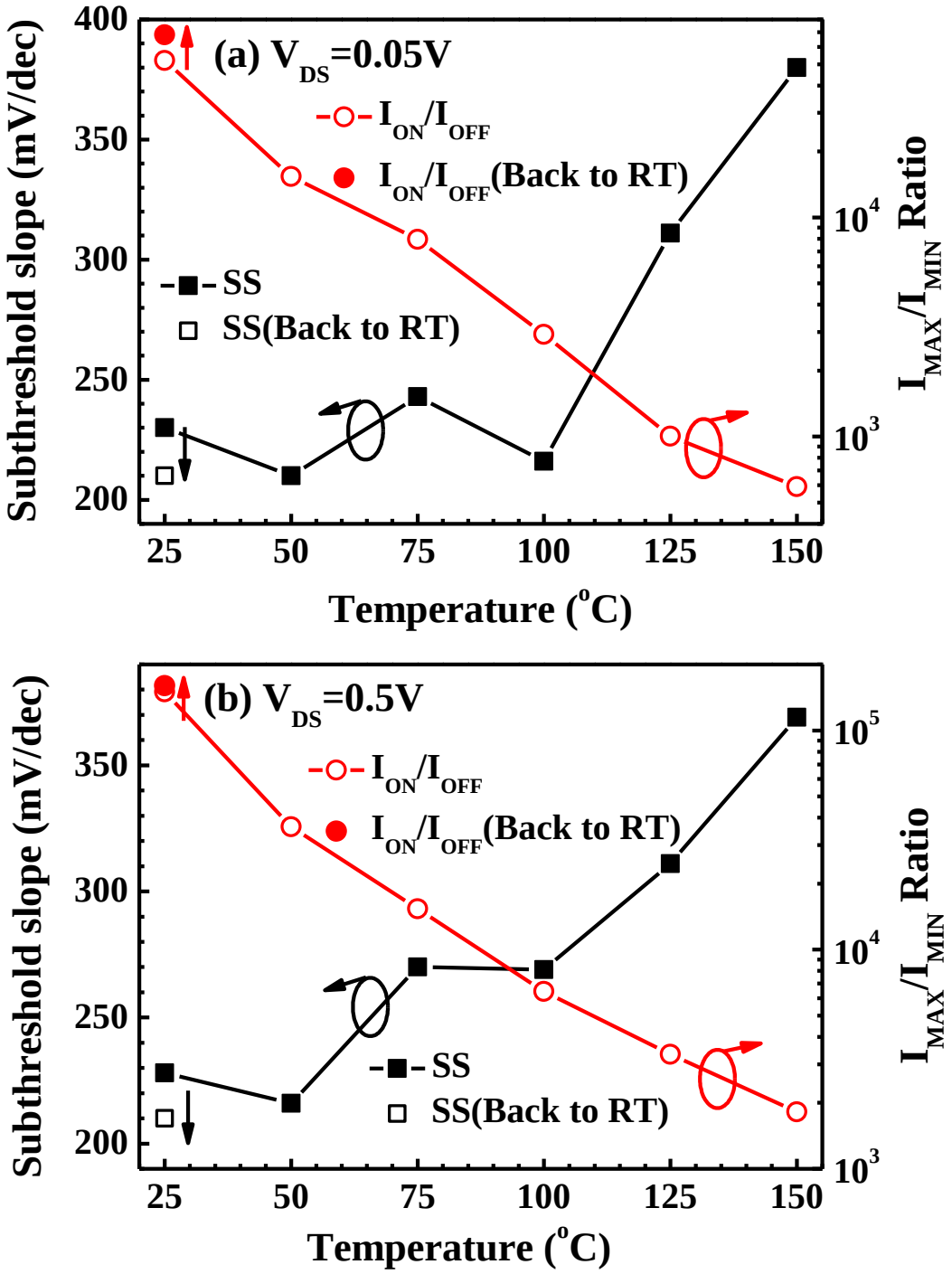


**Figure 6.9** Changing of subthreshold slope and $I_{MAX}/I_{MIN}$ ratio of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET devices with temperature for (a) $V_{DS}$ = 0.05V and (b) $V_{DS}$ = 0.5V. The strong temperature dependence of SS at high temperature (> 100°C for $V_{DS}$ = 0.05V and > 75°C for $V_{DS}$ = 0.5V) may be caused by trap-assisted tunneling by mid-gap traps. The $I_{MAX}/I_{MIN}$ ratio decreased from ~ $10^5$ at 25°C to ~ $10^3$ at 150°C. This degradation of device performance was mainly caused by the high leakage current at high temperature. [7] Used with permission from IEEE.

Figure 6.9 (a) and (b) [7] showed the SS and $I_{MAX}/I_{MIN}$ ratio ($I_{MAX}$ is $I_{DS}$ at $V_{GS}$ = 1.5V and $I_{MIN}$ is $I_{DS}$ at $V_{GS}$ = -0.5V) of the TFET device as a function of temperature for $V_{DS}$=0.05V and 0.5V, respectively. The value of SS was not sub-60mV/dec due to high mid-gap traps and surface charges at the channel/high-κ oxide interface. These interface traps and surface charges can retard the Fermi-level movement of the intrinsic channel controlled by $V_{GS}$, and they can also result in TAT and the subsequent thermal emission [6, 20], all of which will degrade SS. For both $V_{DS}$ = 0.05V and 0.5V, SS was almost constant with temperature up to 100$^{o}$C, but increases sharply at temperature greater than 100$^{o}$C and it has a strong positive temperature dependent coefficient from 100$^{o}$C to 150$^{o}$C. The strong temperature dependence of SS is caused by TAT in the subthreshold region, in which the electrons in the valence band of $p^{++}$ $GaAs_{0.35}Sb_{0.65}$ source tunneled into the mid-gap traps and followed by a subsequent thermal emission into the conduction band of $In_{0.7}Ga_{0.3}As$ channel, which gives rise to the strong temperature dependence as well as deterioration of SS. In order to improve the SS, surface chemical passivation is essential to suppress these dominant mid-gap traps and surface charges. In addition, SS was improved after temperature cycle for both $V_{DS}$=0.5V and 0.05V and it is due to the removal of some trap states during the long duration of annealing. The $I_{MAX}/I_{MIN}$ ratio decreases exponentially with increasing temperature for both $V_{DS}$=0.05V and 0.5V. This can be explained by the combined effects of exponential dependence of $I_{OFF}$ with temperature and the weak temperature dependence of $I_{DR}$. The $I_{MAX}/I_{MIN}$ ratio decreased from ~ $10^5$ at 25$^{o}$C to ~ $10^3$ at 150$^{o}$C. This degradation of device performance was mainly due to the high leakage current at higher temperature (> 100$^{o}$C). Moreover, the $I_{MAX}/I_{MIN}$ ratio recovered to its initial level when the device was cooled down to 25$^{o}$C after temperature cycle, which indicates that the high temperature operation was not destructive to the TFET structure up to 150$^{o}$C.

In summary, the high temperature reliability studies demonstrated stable structural properties and distinguished device characteristics of the mixed As/Sb staggered gap TFETs at higher operating temperature. The temperature dependent structural and device properties of the mixed As/Sb staggered gap TFET highlights the importance of the reliability on high temperature operation of TFETs for future low-power digital logic applications.

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# Chapter 7 Structural properties of complementary p-channel mixed As/Sb TFET structure

In recent years, great efforts have been devoted to investigate and upgrade the structural properties and device performances of n-type $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ staggered gap TFETs [1-12]. However, the study of p-type TFET is impeded due to the limited density of states in the conduction band of III-V materials. The trade-off between high ON-state current and steep subthreshold slope prompted us to study high-quality p-type TFET structures within the same material system to achieve complementary energy efficient logic circuits [13, 14]. In this chapter, a comprehensive study was carried out on the structural properties of a metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type staggered gap TFET structure grown by molecular beam epitaxy (MBE). The schematic layer structure is shown in Fig. 7.1. The source (S), channel (C) and drain (D) regions are labeled in this figure and the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface is denoted in a box. The schematic band alignment of the p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFET structure is shown in Fig. 7.2. The measured valence band offset, calculated conduction band offset and effective tunneling barrier height ($E_{beff}$) were also labeled in this figure. The experimental results demonstrated high material quality of this TFET structure.

## 7.1 Strain relaxation properties

The symmetric (004) XRD rocking curve of this p-channel TFET structure is shown in Fig. 7.3. Each layer was labeled to its corresponding peak based on wet chemical etching experiments.[12] According to the epilayer structure as shown in Fig. 7.1, the $In_{0.7}Al_{0.3}As$ buffer layer, the $GaAs_{0.35}Sb_{0.65}$ channel/drain layers and the $In_{0.7}Ga_{0.3}As$ source layer were designed to

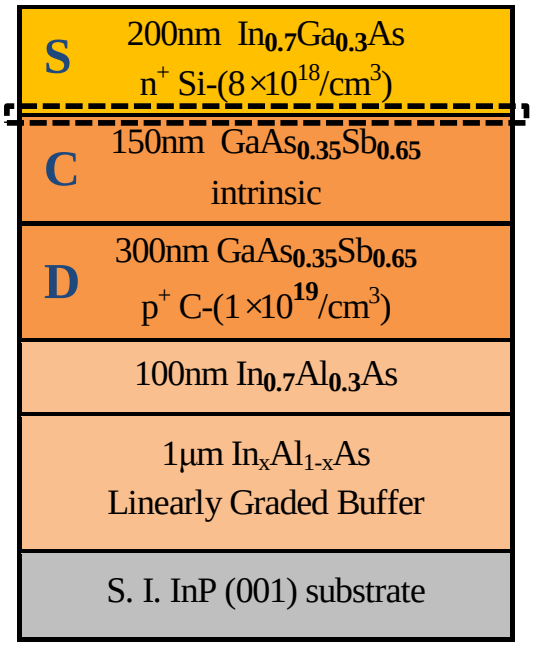


**Figure 7.1** Schematic diagram of the metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type TFET layer structure. The source (S), channel (C) and drain (D) regions are labeled in this figure and the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface is denoted in a box. Used with permission from AIP.

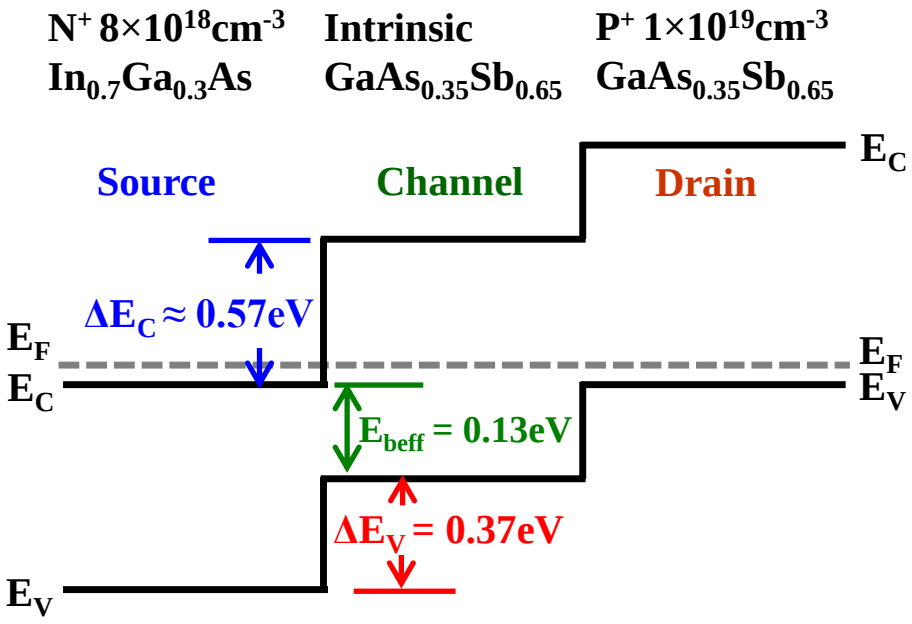


**Figure 7.2** Schematic band diagram of the metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type TFET structure. The measured valence band offset, calculated conduction band offset and effective tunneling barrier height ($E_{beff}$) were also labeled in this figure. Used with permission from AIP.

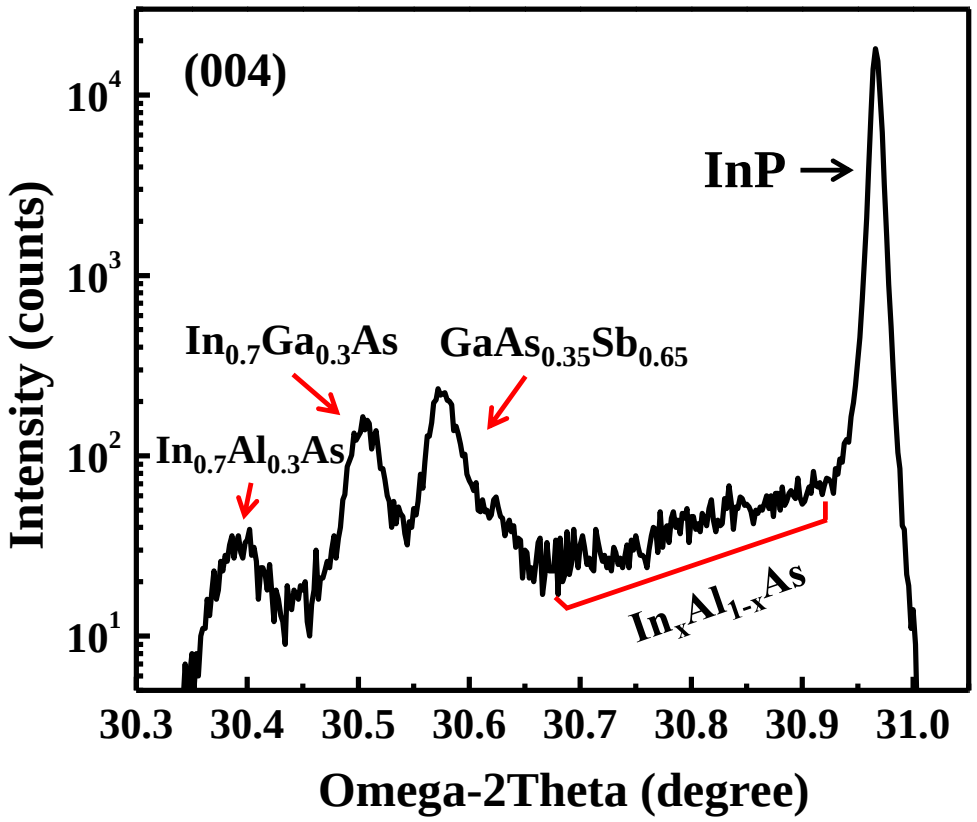


**Figure 7.3** Symmetric (004) x-ray rocking curve of the metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type TFET structure. Each layer was labeled to its corresponding peak based on early performed wet chemical etching experiments. Used with permission from AIP.

be internally lattice matched. However, due to the residual strain within the $In_{0.7}Al_{0.3}As$ buffer layer [15], as well as heavily carbon (C) doping induced lattice contraction [9] in the $GaAs_{0.35}Sb_{0.65}$ layer, these three layers appear as three separate peaks in the XRD rocking curve spectrum as shown in Fig. 7.3. The distinct XRD peak positions suggest different lattice constants within each epilayer, which indicates different strain relaxation states of the epilayers. The detailed strain relaxation states and residual strain of each epilayer were analyzed from symmetric (004) and asymmetric (115) RSMs. Figure 7.4 (a) and (b) show the symmetric (004) and asymmetric (115) RSMs of the p-type TFET structure with incident x-ray beam along $[1\bar{1}0]$ direction. Four distinct reciprocal lattice points (RLPs) were found in RSMs of this structure, corresponding to (1) the InP substrate, (2) $GaAs_{0.35}Sb_{0.65}$ channel/drain layer, (3) $In_{0.7}Ga_{0.3}As$

source layer and (4) 100nm $In_{0.7}Al_{0.3}As$, the uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. From RSMs, the lattice constant in the out-of-plane, *c* (from the symmetric 004 reflection), and the lattice constant in the growth plane, *a* (from the asymmetric 115 reflection), were determined. The relaxed lattice constant $a_r$ and strain relaxation values were also extracted from RSMs. Table 7.1 summarized the in-plane and out-of-plane lattice constants, relaxed lattice constants, strain relaxation values, residual strain and alloy composition of each epilayer with the projection of x-ray beam along $[1\bar{1}0]$ direction. Using the extracted lattice constant values in Table 7.1, it can be seen that the active layers ($In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$) are pseudomorphic to the $In_{0.7}Al_{0.3}As$ buffer, which indicates that low dislocation density should be expected within the active layers. Besides, the low dislocation density within the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers can be further supported by the relatively short elongation of RLPs of these two layers along Q (1-10) direction as shown in Fig. 7.4 (a) and (b). Smaller dislocation density in [110] (or $[1\bar{1}0]$) direction leads to less diffuse scattering of x-ray in its orthogonal $[1\bar{1}0]$ (or [110]) direction, resulting in the shorter elongation of RLPs along Q (1-10) (or Q (110)) in RSMs. Furthermore, it can be found from the asymmetric (115) RSM as shown in Fig. 7.4 (b) that, the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers are aligned in a vertical line (fully strained line, red dashed line in Fig. 7.4 (b)) with respect to the $In_{0.7}Al_{0.3}As$ buffer, which additionally confirmed the pseudomorphic nature of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers [16]. Although the in-plane lattice constants of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ are slightly smaller than that of $In_{0.7}Al_{0.3}As$ in this p-type TFET structure, the small difference in lattice constant does not generate strain relaxation of these two layers due to the critical layer thickness consideration, which lead to the pseudomorphic nature and low dislocation density within these two layers.

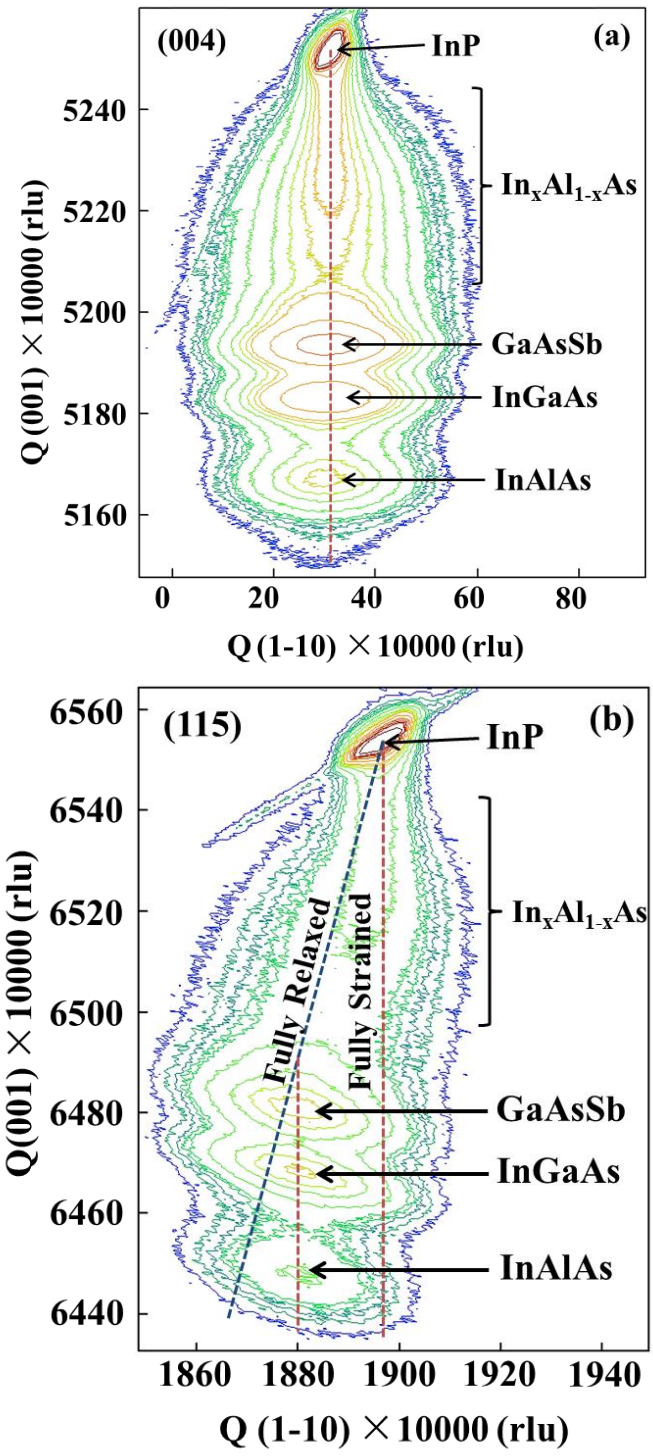


**Figure 7.4** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the p-type TFET structure with the incident x-ray beam along $[1\,\bar{1}0]$ direction. The RSMs together with the extracted lattice parameters confirmed the pseudomorphic nature of the active layers ($In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$) respect to the $In_{0.7}Al_{0.3}As$ buffer, which indicates that low dislocation density should be expected within the active layers. Used with permission from AIP.

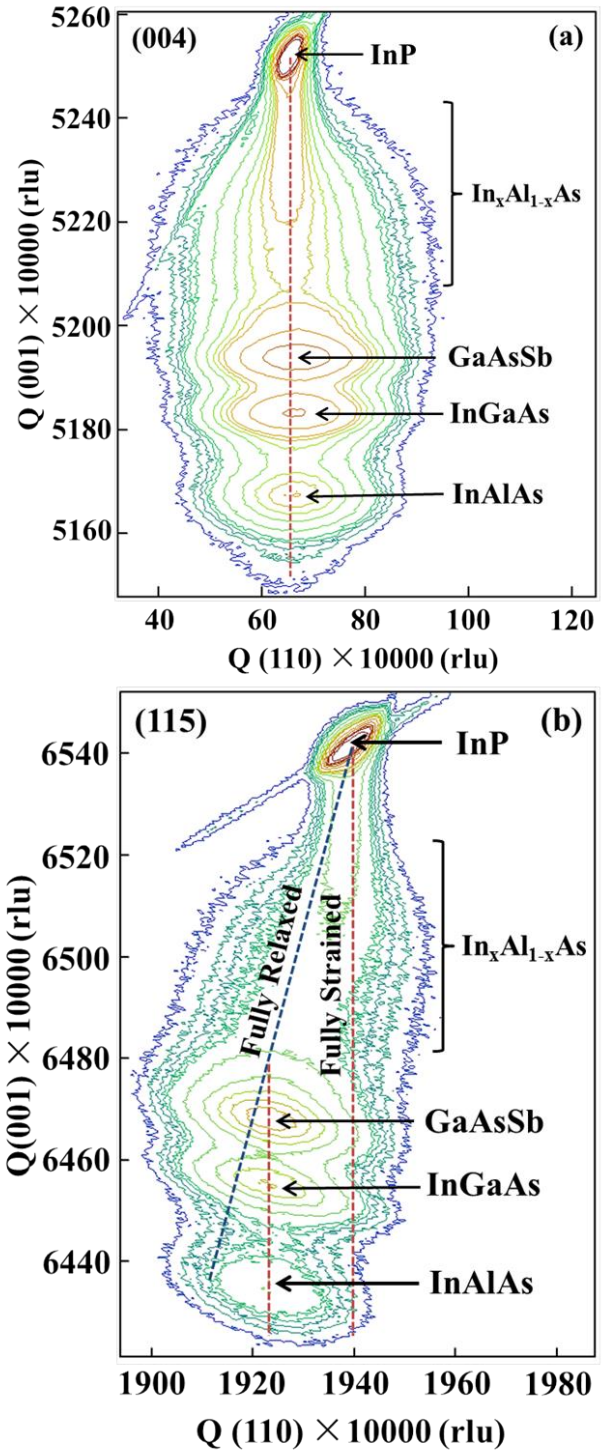


**Figure 7.5** (a) Symmetric (004) and (b) asymmetric (115) RSMs of the p-type TFET structure with the incident x-ray beam along [110] direction. The strain relaxation values of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the $In_{0.7}Al_{0.3}As$ buffer are almost identical along two orthogonal <110> directions, which indicates symmetric strain relaxation of this structure. Used with permission from AIP.

**Table 7.1** Summary of strain relaxation properties of the p-channel TEFT structure with incident x-ray beam along [$1\bar{1}0$] and [110] directions. Used with permission from AIP.

| Incident Beam Direction | Layers | Lattice Constant (Å) | | | Composition | Relaxation (%) | Tilt (arcsec) | Strain (%) |
|---|---|---|---|---|---|---|---|---|
| | | c | a | $a_r$ | | | | |
| [$1\bar{1}0$] | GaAsSb | 5.9347 | 5.9127 | 5.9237 | Sb: 62% | 80 | -19 | 0.94 |
| | InGaAs | 5.9468 | 5.9162 | 5.9314 | In: 69% | 76 | -38 | 1.07 |
| | InAlAs | 5.9649 | 5.9202 | 5.9426 | In: 71% | 70 | -58 | 1.26 |
| [110] | GaAsSb | 5.9343 | 5.9132 | 5.9237 | Sb: 62% | 81 | 56 | 0.94 |
| | InGaAs | 5.9465 | 5.9146 | 5.9304 | In: 68% | 74 | 35 | 1.05 |
| | InAlAs | 5.9648 | 5.9226 | 5.9437 | In: 71% | 72 | 35 | 1.28 |

For metamorphic zinc-blende semiconductor structures, the lattice mismatch between substrate and epilayers can be accommodated by dislocation glide. However, asymmetric strain relaxation will lead to different dislocation densities along two orthogonal <110> directions, which will in turn result in different lattice constants along [110] and [$1\bar{1}0$] directions [17]. As a result, the anisotropy in strain relaxation states of the TFET structure can be determined by aligning the projection of the incident x-ray beams along two orthogonal <110> directions. Therefore, x-ray RSMs were recorded once again on this structure with the incident x-ray beam along [110] direction and Fig. 7.5 (a) and (b) show the symmetric (004) and asymmetric (115) RSMs from this measurement, respectively. The lattice parameters and strain relaxation values extracted from Fig. 7.5 (a) and (b) were also summarized in Table 7.1. One can find from Table 7.1 that the strain relaxation values of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the $In_{0.7}Al_{0.3}As$ buffer are almost identical along two orthogonal <110> directions, which indicates

symmetric strain relaxation of this structure. The symmetric strain relaxation of these layers suggests that the total length of misfit dislocations in each <110> direction is approximately the same. Besides, the lattice tilt amplitude observed from (004) RSMs was less than 200 *arc sec* from each epilayers in both measurements, indicating nearly equal amount of α and β dislocations participated during the relaxation process. The small lattice tilt also supports the observed symmetric strain relaxation of the lineally graded $In_xAl_{1-x}As$ buffer, $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers. The symmetric strain relaxation properties not only indicate the homogeneity and effectiveness of the graded buffer on the relaxation of mismatch induced strain, but also provide more flexibility for the alignment of channel direction during the device fabrication with side-wall architecture. [3] As a result, the pseudomorphic nature of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the symmetric strain relaxation of the structure provide a "virtually" defect free and isotropic active region for the p-type TFET structure, which is desirable for improving the performance of TFET devices with low OFF-state leakage and high ON/OFF-ratio.

## 7.2 Surface morphology

Strain within the linearly graded buffer was primarily relaxed by formation of 60 ° *a*/2 <110> {111} misfit dislocations at epilayer/substrate interface [17]. These dislocations can glide along {111} planes[21] and thread toward the surface at 60 ° angle within <110> directions [17, 18], which results in a cross-hatch pattern on the sample surface. As a result, characterization of the surface morphology is an important metric for the metamorphic TFET structure as it directly relates to the strain relaxation properties. Figure 7.6 shows the 10μm ×10μm AFM micrograph of the TFET structure, which displays the anticipated two-dimensional cross-hatch surface morphology. The two-dimensional cross-hatch pattern is well developed and quite uniform with ridges and grooves parallel to [110] and $[1\bar{1}0]$ directions, as labeled in the figure. The line

profiles in the two orthogonal <110> directions are also included in this figure. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggest a symmetric strain relaxation of the linearly graded buffer layer, which is in agreement with the XRD results. Besides, the AFM measurement shows a smooth surface with a root-mean-square (*rms*) roughness of 2.58nm. The well maintained two-dimensional cross-hatch pattern and low surface *rms* roughness also indicates the low dislocation density of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers; otherwise, the two-dimensional cross-hatch pattern developed by the graded buffer will be sheltered by high density dislocations and a grainy texture with much higher surface roughness will be expected [9].

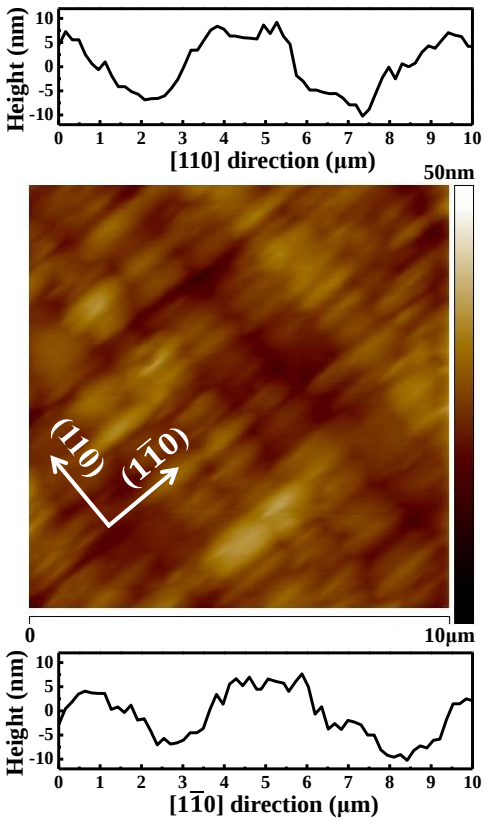


**Figure 7.6** 10μm×10μm AFM micrograph of the p-type metamorphic TFET structure. The line profiles in the two orthogonal <110> directions are also included. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggests a symmetric strain relaxation of the linearly graded buffer layer. The AFM measurement shows a smooth surface morphology of the TFET structure with a root-mean-square (*rms*) roughness of 2.58nm.

## 7.3 Dislocation and defects

The crystalline quality of the p-type TFET structure was further characterized by cross-sectional TEM. Figure 7.7 (a) shows the bright field cross-sectional TEM micrograph of the TFET structure. All layers were labeled in this figure and the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface was denoted by an arrow. It can be seen from this figure that the linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch by the formation of dislocations between $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the InP substrate. Most of the dislocations were confined within the graded $In_xAl_{1-x}As$ buffer and the upper region of the graded buffer with a thickness of ~200nm has a minimal dislocation density which cannot be detected at this magnification. As the linearly graded buffer relaxed most of lattice mismatch induced strain, the residual strain within the top of the graded buffer layer is small. No further relaxation took place in this region, leaving a strained and dislocation-free region on the top of the graded buffer, providing a high-quality virtual substrate for the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers of the TFET structure. Besides, only one threading dislocation was observed in the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers at this magnification, indicating a threading dislocation density in these layers on the order of $\sim 10^7/cm^2$. Figure 7.7 (b) and (c) shows the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface of this p-type TFET structure with high magnification. High contrast at the heterointerface indicates a sharp interface between $n^+$ $In_{0.7}Ga_{0.3}As$ source and intrinsic $GaAs_{0.35}Sb_{0.65}$ channel, which is benefited to reduce the effective tunneling barrier width and increase in tunneling current of the TFET device [19]. Besides, no dislocations were observed at the heterointerface from the TEM micrographs with high magnification. The low dislocation density within active layers and the heterointerface

suggests high crystalline quality of the p-type TFET structure, which is indispensable for high device performance in fabricated TFETs.

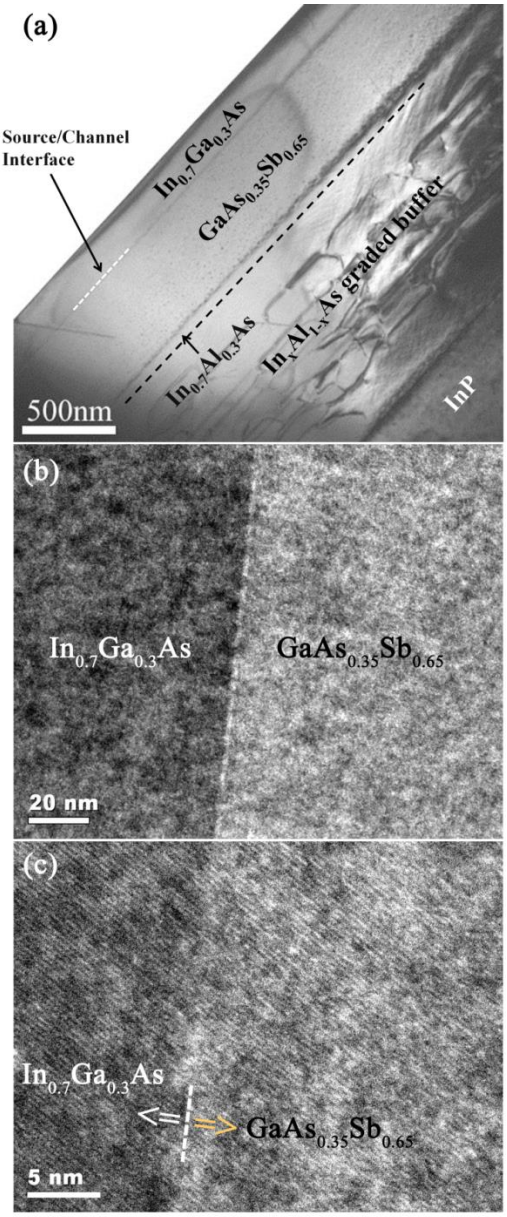


**Figure 7.7** (a) Cross-sectional TEM micrograph of the p-type metamorphic TFET structure. The linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch between $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers and the InP substrate. Only one threading dislocation was observed in the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers at this magnification, indicating high crystalline quality of the p-type TFET structure. (b) and (c) cross-sectional TEM micrograph of the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface with high magnification. A sharp heterointerface with high crystalline quality was observed. Used with permission from AIP.

## 7.4 SIMS profiles

The abruptness of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterojunction as well as the sharpness of Si doping profile is critical to the performance of TFET devices as they directly determine the tunneling barrier width for carrier to transport from source to channel [19], which directly relates to the ON-state current of TFETs. Besides, the intermixing of As and Sb at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ interface will result in uncontrolled layer composition, which will lead to unintended band alignment and may introduce high dislocation density due to compositional mismatch. In order to determine the atomic intermixing of As and Sb as well as the sharpness of Si doping at the source/channel interface, dynamic SIMS measurements were performed to characterize the compositional profiles of As, Sb and Si in the source and channel regions. Figure 7.8 (a) shows the As, Sb and Si depth profiles of the p-type TFET structure. The concentration of different elements was not quantified due to the lack of corresponding standards for SIMS measurement. An abrupt $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface was also found in this structure. The transition from As rich $In_{0.7}Ga_{0.3}As$ to Sb rich $GaAs_{0.35}Sb_{0.65}$ is less than 10nm, within the sputter induced broadening of the ion beam, depicting a minimum intermixing between As and Sb at the heterointerface. Figure 7.8 (b) shows the calibrated Si doping profile of the p-type TFET structure. The fluctuation of Si doping profile in the source region may due to the secondary ion beam signal variability in the sputtering process. The dopant abruptness is less than 2nm/decade from $n^+$ $In_{0.7}Ga_{0.3}As$ source to intrinsic $GaAs_{0.35}Sb_{0.65}$ channel, which is less than the critical dopant abruptness (4nm/decade) [20] of TFET devices to maximize the junction electric fields and thus enable high ON-state current. The well controlled interface transition with minimum As/Sb intermixing assured the anticipated staggered band alignment with desired effective tunneling barrier height; the abrupt dopant change reduced the carrier tunneling

distance and maximized the junction electric field, both of which enhanced high ON-state current.

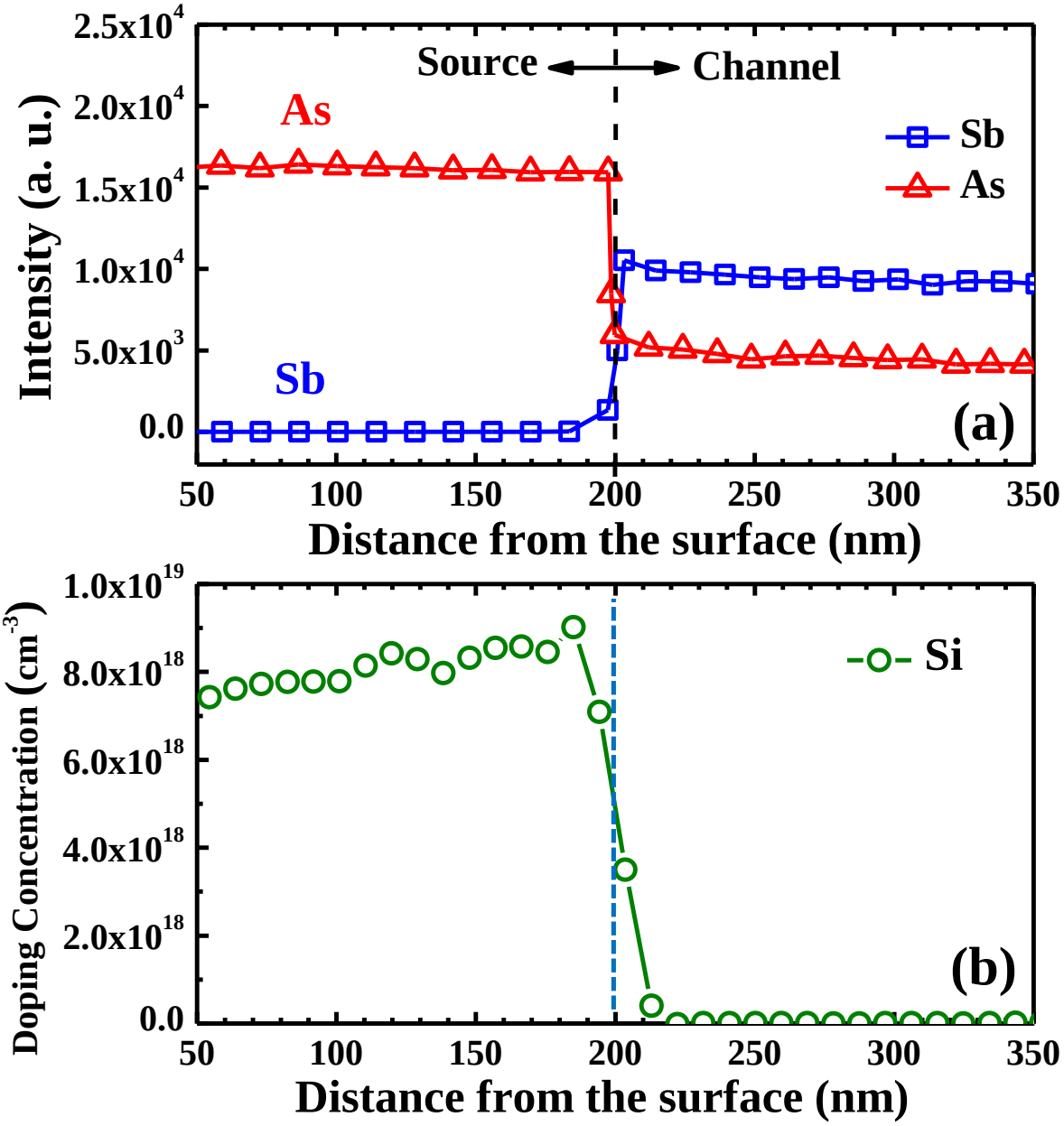


**Figure 7.8** (a) Dynamic SIMS depth profiles of As, Sb from the p-type TFET structure. As abrupt As/Sb change with a transition less than 10nm was confirmed, indicating low level intermixing between As and Sb at the interface. (b) Si doping profile of the p-type TFET structure. An abrupt Si doping profile with the dopant abruptness less than 2nm/decade suggests a steep junction formed at the source/channel interface. Used with permission from AIP.

## 7.5 Band alignment properties

The band alignment between the $In_{0.7}Ga_{0.3}As$ source and $GaAs_{0.35}Sb_{0.65}$ channel is determined by Kraut's method [21] as mentioned in ***Chapter 5.5***. The same experimental setting of XPS instrument is used in this section. In order to measure the band alignment between source and channel materials, three samples from the p-type TFET structure were used. The 5nm $In_{0.7}Ga_{0.3}As$/450nm $GaAs_{0.35}Sb_{0.65}$ structure was used for the measurement of binding energy information at the heterointerface, while 200nm $In_{0.7}Ga_{0.3}As$/450nm $GaAs_{0.35}Sb_{0.65}$ and 450nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer were used to measure the binding energy information of bulk $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively [13]. The core level (CL) and valence band (VB) spectra from each sample were shown in Fig. 7.9 (a) – (f). In order to improve accuracy of the measured binding energy information, high resolution measurements with a step-size of 0.025eV was performed to resolve the spin-orbit splitting of In and Sb 3d peaks. Curve fitting was done on each CL spectra to separate In-As and Sb-Ga bonds from the In-O and Sb-O bonds. The measured binding energy of In-O and Sb-O bonds was about 444.90eV and 530.0eV, respectively, which were in agreement with the reported values [22, 23]. The binding energy difference between Sb-O and Sb-Ga bonds are large enough to resolve the Sb-O bond as a separated peak (not shown in Fig. 7.9) from Sb-Ga spectrum. As a result, unlike $In3d_{5/2}$ CL spectrum, which was a combination of In-As and In-O bonds, the measured $Sb3d_{5/2}$ CL peak was Lorentzian shape without curve fitting. All measured binding energy values are summarized in Table. 7.2. The VBO of $In_{0.7}Ga_{0.3}As$ source relative to $GaAs_{0.35}Sb_{0.65}$ channel is $0.37 \pm 0.05$eV. The uncertainty value 0.05eV is due to the scatter of VB with respect to the fitting in VBM position. The conduction band offset (CBO) $In_{0.7}Ga_{0.3}As$ with respect to $GaAs_{0.35}Sb_{0.65}$ was calculated to be $\Delta E_C \sim 0.57$eV using bandgap of intrinsic $GaAs_{0.35}Sb_{0.65}$

(0.7eV at 300K) and bandgap of heavily doped $In_{0.7}Ga_{0.3}As$ (0.50eV at 300K with Si doping of 8 × $10^{18}/cm^3$). The band alignment between $In_{0.7}Ga_{0.3}As$ source and $GaAs_{0.35}Sb_{0.65}$ channel is shown in Fig. 7.2.

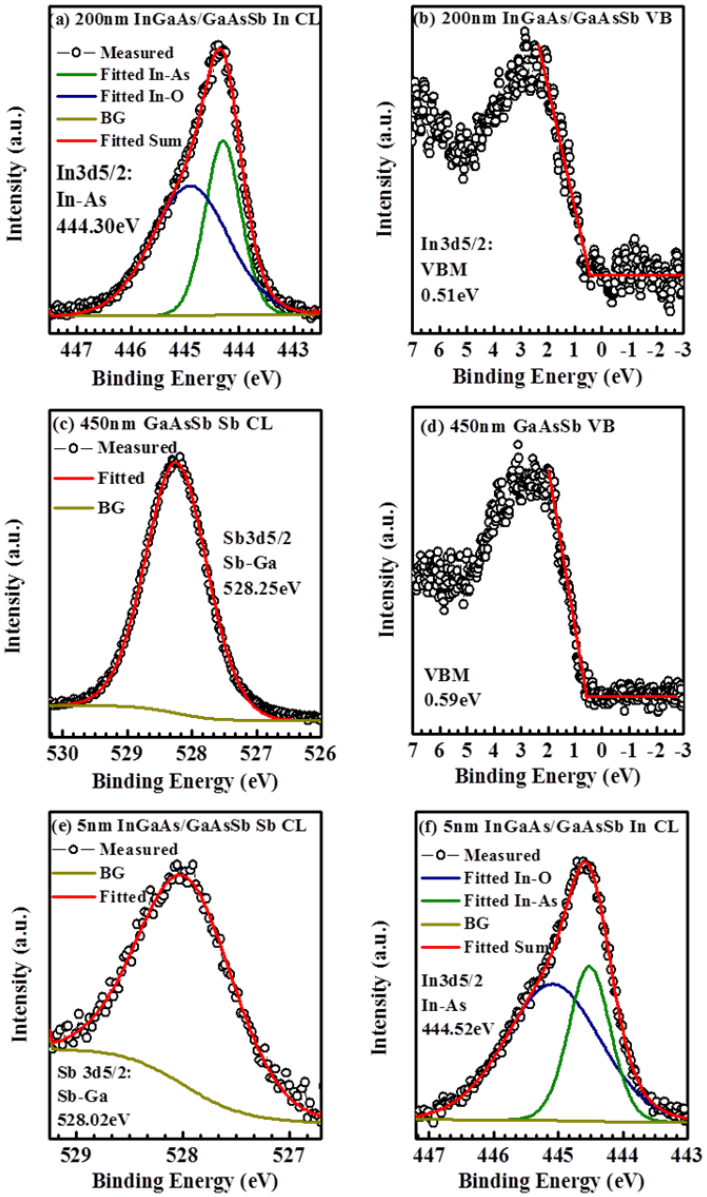


**Figure 7.9** XPS spectra of (a) $In3d_{5/2}$ core level (CL) and (b) valence band (VB) from 200nm $In_{0.7}Ga_{0.3}As$/150nm $GaAs_{0.35}Sb_{0.65}$ sample; (c) $Sb3d_{5/2}$ CL and (d) VB from 150nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL from 5nm $In_{0.7}Ga_{0.3}As$/150nm $GaAs_{0.35}Sb_{0.65}$ measured at the interface. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. Valence band maxima (VBM) were determined by linear extrapolation of the leading edge of VB spectra to the base line.

**Table 7.2** XPS core level spectra results after curve fitting and valence band maxima (VBM) positions obtained by linear extrapolation of the leading edge to the extended base line of the valence band spectra.

| Sample | States | Binding Energy (eV) | Bonding |
|---|---|---|---|
| 200nm $In_{0.7}Ga_{0.3}As$/ 450nm $GaAs_{0.35}Sb_{0.65}$ | $In3d_{5/2}$ | 444.30 | In-As |
| | $In3d_{5/2}$ | 444.90 | In-O |
| | VBM | 0.51 | |
| 450nm $GaAs_{0.35}Sb_{0.65}$ | $Sb3d_{5/2}$ | 528.25 | Sb-Ga |
| | $Sb3d_{5/2}$ | 530.00 | Sb-O |
| | VBM | 0.59 | |
| 5nm $In_{0.7}Ga_{0.3}As$/ 450nm $GaAs_{0.35}Sb_{0.65}$ | $Sb3d_{5/2}$ | 528.02 | Sb-Ga |
| | $In3d_{5/2}$ | 444.52 | In-As |
| | $In3d_{5/2}$ | 445.07 | In-O |

## 7.6 OFF-state performance and comparison with n-type TFET device structure

Due to the great challenge of MBE growth of mixed As/Sb $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructures for p-type staggered gap TFET applications [9-11], systematically investigation of the structural properties of this heterostructure is essential prior to device fabrication. Studies of growth parameters and optimization of shutter sequences are indispensable for this structure in order to engineer an abrupt change from Sb-rich $GaAs_ySb_{1-y}$ to As-rich $In_xGa_{1-x}As$ layer. Otherwise, improper change of group-V fluxes at the $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterointerface will form a GaAs-like heterointerface, which will in turn produce higher dislocation density at the

heterointerface and within the $In_xGa_{1-x}As$ layer [9-10]. These dislocations will introduce fixed charges and change the band alignment from staggered gap to broken gap, resulting in high leakage current of TFET devices [9]. In order to investigate the OFF-state performance of the p-type TFETs, $n^+$-i-$p^+$ diodes were fabricated from this structure. As the OFF-state current of p-type TFETs is governed by the leakage current of the reverse-biased $n^+$-i-$p^+$ diode [9, 19], current-voltage (I-V) characteristics of the $n^+$-i-$p^+$ diode were measured. Figure 7.10 (a) shows the room temperature I-V characteristic of the reverse-biased $n^+$-i-$p^+$ diode. The room-temperature I-V characteristic of the reverse-biased $p^+$-i-$n^+$ diode fabricated from the n-type $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure with both (b) InAs-like heterointerface and (c) GaAs-like heterointerface (as discussed in detail in ***Chapter 5.4***) are also used for comparison [9]. Similar leakage current level was observed from the p-type TFET as that from the n-type TFET with an InAs-like heterointerface, indicating that an InAs-like interface with high crystalline quality was formed at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface in the p-type TFET structure. Besides, due to superior material quality, $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFETs with an InAs-like heterointerface exhibits 3 orders of magnitude lower leakage current compared with TFETs with a GaAs-like heterointerface (as shown in Fig. 7.10 (c)). The relatively low leakage current of the p-type TFET supports our structural analysis presented here.

This study demonstrated preferable strain relaxation properties and high crystalline quality of the p-type TFET structure together with minimum ad-atom intermixing at the heterointerface, all of which are necessary for high performance devices. Earlier studies showed that the type-II staggered band alignment with an effective tunneling barrier height ($E_{beff} = E_G^{InGaAs} - \Delta E_V$) of 0.13eV was formed at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterointerface [13]. This effective tunneling barrier height plays a significant role on the performance of either n-channel [10] or p-

channel TFET devices, which not only determines the ON-state BTBT current but also sets the blocking barrier for the OFF-state leakage. It has been also reported that high ON-state current of 135μA/μm with recorded high $I_{ON}/I_{OFF}$ ratio of $2.7\times10^4$ was achieved in an n-type TFET device using similar $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ heterostructure [2, 8]. OFF-state performance studies also confirmed similar leakage current level of this n-type TFET with the p-type TFET structure using in this study. As a result, promising device performance is expected to be achieved in the structure used in this study for complementary p-type TFET applications.

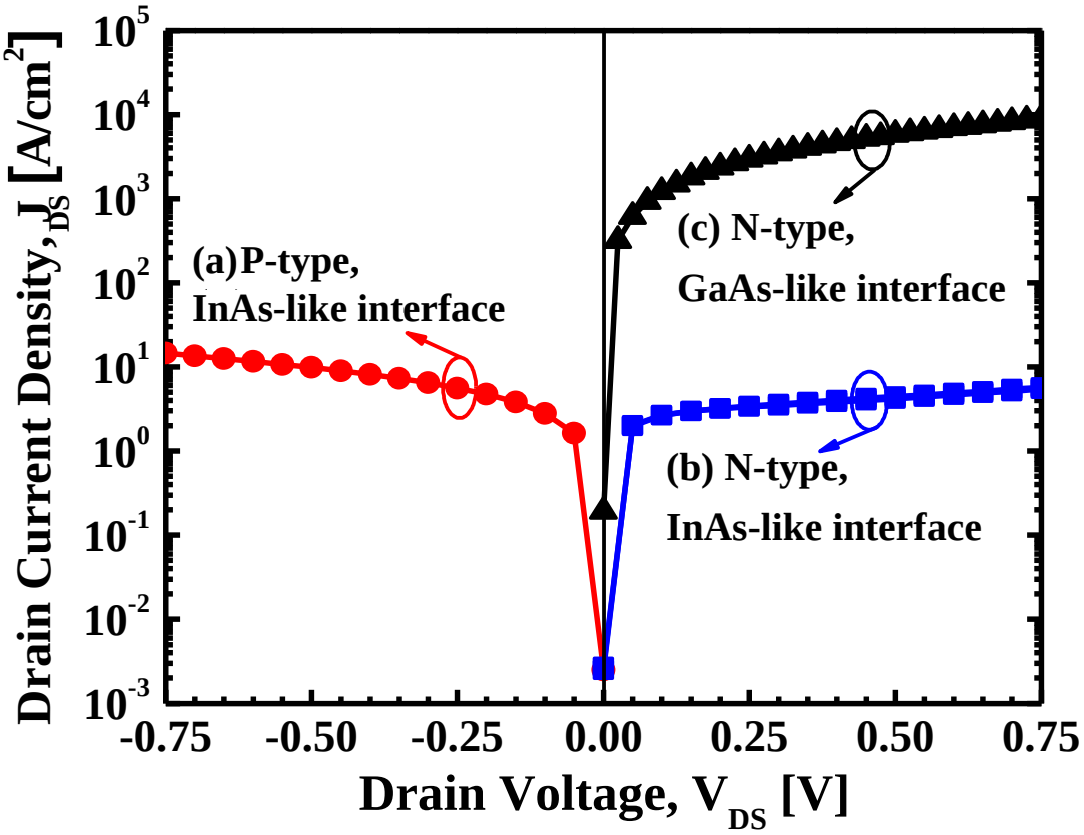


**Figure 7.10** (a) Room-temperature I-V characteristic of the reverse-biased $n^+$-i-$p^+$ diode fabricated from the p-type $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ TFET structure. The room-temperature I-V characteristic of the reverse-biased $p^+$-i-$n^+$ diode fabricated from the n-type $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ TFET structure with both (b) InAs-like heterointerface and (c) GaAs-like heterointerface are also used for comparison. Similar leakage current level of the p-type TFET as that of the N-type TFET with a InAs-like heterointerface indicates that the InAs-like heterointerface with high crystalline quality was formed at source/channel interface of the p-type TFET structure.

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# Chapter 8 Tensile strained Ge/$In_{0.16}Ga_{0.84}As$ structure for TFET applications

In the former chapters, detailed structural properties and device performances analysis were performed on the mixed As/Sb TFET heterostructures. The experimental results show great potential of the mixed As/Sb heterostructures for low power TFET applications. As an alternative path, the tensile strained Ge/InGaAs heterostructures were also proposed for TFET application.

## 8.1 Utilization of tensile strained Ge/$In_xGa_{1-x}As$ heterostructures as an alternative path for TFET applications

In order to achieve high band-to-band-tunneling (BTBT) probability and high $I_{ON}$, small band gap materials such as germanium (Ge) and III-V materials should be employed [1-4, 7-15]. In past few decades, Ge has been actively investigated due to its high intrinsic carrier mobility, small band gap energy and silicon (Si) compatible process flow [15-17]. In addition, tensile strained Ge exhibited further reduction in band gap energy and enhanced electron and hole mobility [16-18], making it a highly promising material for low power TFET applications. For further improvement, the band alignment engineering is essential to improve the $I_{ON}$ and reduce the SS of TFET structures. Heterojunction TFET structure as a replacement for homojunction has been used to efficiently reduce the effective tunneling barrier height ($E_{beff}$) between the source and the channel [2, 4, 6-11] that resulted in additional enhancement of TFET device performances. In this aspect, the Ge/InGaAs heterostructure satisfies the requirements for low band gap material system in a TFET design. More importantly, by carefully controlling the alloy composition in InGaAs material, the magnitude of tensile strain inside the Ge layer can be

tailored such that the $E_{beff}$ between the Ge source and the InGaAs channel can also be well-modulated, both of which will facilitate the further optimization of TFET structure. Simulations predicted [19] and experiments demonstrated [13] that wide range of In composition from 0% to 53% can be used in Ge/InGaAs heterostructures for TFET applications, providing various selection of tensile strain values inside of Ge and different band alignments at the Ge/InGaAs heterointerface. In order to reduce the tunneling distance and increase the tunneling current, a high quality Ge/InGaAs heterostructure with a sharp heterointerface between the tensile strained Ge source and the InGaAs channel is indispensable [11, 13, 20]. As a result, there is a great demand for the growth of high quality tensile strained Ge/InGaAs heterostructures to fully explore the benefits of low power TFET applications. Control of the tensile strain magnitude in the heterostructure provides an additional parameter towards tuning the transistor behavior.

To date, all reported Ge/InGaAs heterostructures have been grown by metal-organic chemical vapor deposition (MOCVD) [13, 16]. However, solid-source molecular beam epitaxy (MBE) is now receiving interest for TFET applications due to its extreme precision and growth uniformity, since it provides an opportunity to investigate and potentially optimize *in-situ* grown tensile strained Ge on InGaAs within a very different growth regime compared to MOCVD. Using MBE, superior quality of GaAs/Ge/GaAs and Ge/GaAs heterostructures have been reported recently [17, 18]. This chapter will demonstrate the study of *in-situ* grown tensile strained Ge/InGaAs heterostructures by MBE. Detailed structural analysis provided here will facilitate the application of this heterostructure for TFET design and optimization of device performance.

## 8.2 MBE growth of tensile strained Ge/$In_{0.16}Ga_{0.84}As$ TFET structure

In this chapter, high quality tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was grown by solid source MBE using two separated growth chambers for Ge and III-V materials. These two growth chambers were connected *via* ultrahigh vacuum transfer chamber. The separation of Ge growth chamber from III-V growth chamber reduces the diffusion of arsenic (As) atoms into Ge, decreasing excess As point defects inside the Ge layer [17, 18] and preserving the sharp heterointerface between Ge and InGaAs. The reduction of As point defect will reduce the traps assisted tunneling access and the abrupt Ge/InGaAs heterointerface will shorten the tunneling distance of carriers from Ge source to InGaAs channel, both of which are critical for reducing the SS and improving $I_{ON}$ of TFETs. By utilizing the *in-situ* MBE growth process and carefully optimizing the growth parameters, the presence of 0.75% in-plane tensile strain was identified by x-ray diffraction (XRD) within the 15 nm Ge layer deposited on $In_{0.16}Ga_{0.84}As$. The tensile strained nature of Ge layer and a sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was confirmed by high resolution transmission electron microscopy (TEM) analysis.

The Ge/$In_{0.16}Ga_{0.84}As$ TFET heterostructure was grown on offcut (100) epi-ready semi-insulating GaAs substrate (2 ° offcut toward <110> direction). Substrate oxide desorption was done at ~680 ℃ under arsenic overpressure of ~$1\times10^{-5}$ torr in the III-V growth chamber. *In-situ* reflection high energy electron diffraction (RHEED) was used to monitor the oxide desorption process as well as the surface reconstruction of each epilayer. An initial 250 nm undoped GaAs buffer layer was deposited at 650 ℃ under a stabilized $As_2$ flux with a V/III ratio of 25. In order to accommodate the lattice mismatch between $In_{0.16}Ga_{0.84}As$ active layer and the GaAs substrate, 500 nm linearly graded $In_xGa_{1-x}As$ buffer was grown with indium (In) composition increasing from 3% to 16%. Then, the 400 nm Si-doped $n^+$ $In_{0.16}Ga_{0.84}As$ drain layer with doping concentration of $2\times10^{18}/cm^3$ was deposited followed by 150 nm intrinsic $In_{0.16}Ga_{0.84}As$ channel

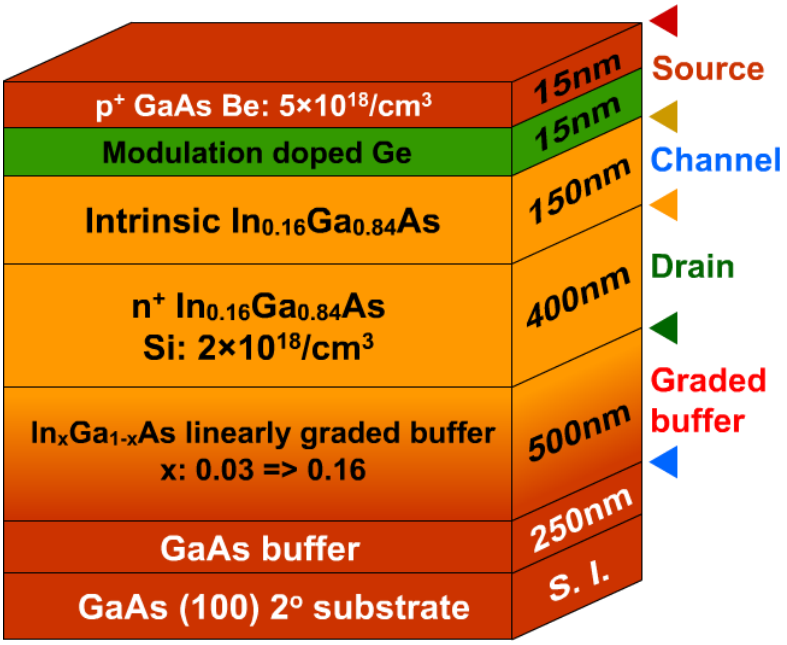


**Figure 8.1** Schematic layer diagram of the strained Ge/$In_{0.16}Ga_{0.84}As$ tunnel FET structure. The source, channel and drain regions are labeled in this figure. Used with permission from ACS.

layer. The $In_xGa_{1-x}As$ linearly graded buffer and the $In_{0.16}Ga_{0.84}As$ channel/drain layers were grown at a substrate temperature of 560°C. After that, the wafer was slowly cooled down below 150 ℃ with arsenic overpressure and transferred to the Ge growth chamber through high vacuum transfer chamber. A 15 nm tensile strained Ge layer was grown on top of intrinsic $In_{0.16}Ga_{0.84}As$ channel at 400 ℃ using a low growth rate of 20 nm/hr. In order to protect the surface of tensile strained Ge layer as well as to form the p-type source contact, the wafer was transferred once again to III-V growth chamber under high vacuum and a 15 nm $p^+$ GaAs was deposited with beryllium (Be) doping concentration of $5\times10^{18}/cm^3$. The growth temperature of the top $p^+$ GaAs cap layer is 350°C for the first 3nm utilizing migration-enhanced-epitaxy (MEE) growth technique followed by 12nm $p^+$ GaAs with growth temperature of 500°C. The low temperature MEE growth technique is confirmed to efficiently reduce the inter-diffusion between Ge and GaAs as well as suppress the anti-phase-domain in early studies [17, 18]. All temperatures referred in this paper represent the thermocouple temperature and the V/III ratio represents the

V/III beam-equivalent-pressure ratio. It should be noted that the further improvement of TFET performance can be expected by *in-situ* doped p-type Ge source layer. However, in this study, by utilizing the modulation doping effect from $p^+$ GaAs top layer to Ge, high hole sheet concentration of ~$1\times10^{13}/cm^2$ was confirmed in the Ge layer by Hall effect measurement using Van der Pauw technique. The schematic of layer structure for this work is shown in Fig. 8.1, where the source, channel and drain regions were labeled in the figure. The strain relaxation properties of this Ge/$In_{0.16}Ga_{0.84}As$ TFET structure were investigated by high-resolution XRD. Both rocking curve (RC, ω/2θ scan) and reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu Kα-1 line-focused x-ray source. The defect properties, crystallinity and interface quality of this structure were characterized by cross-sectional TEM. TEM samples were prepared by conventional mechanical thinning procedure followed by $Ar^+$ ion milling. The contact mode atomic force microscopy (AFM) was used to analyze the surface morphology of this structure. The band alignment of Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was investigated by x-ray photoelectron spectroscopy (XPS) on a PHI Quantera SXM system using a monochromatic Al Kα (1486.7 eV) x-ray source. All XPS measurements were performed using pass energy of 26 eV and an exit angle of 45 °. Curve fitting was performed by CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background.

## 8.3 Structural properties and band alignment determination of tensile strained Ge/$In_{0.16}Ga_{0.84}As$ TFET structure

### 8.3.1 Surface re-construction and strain relaxation properties

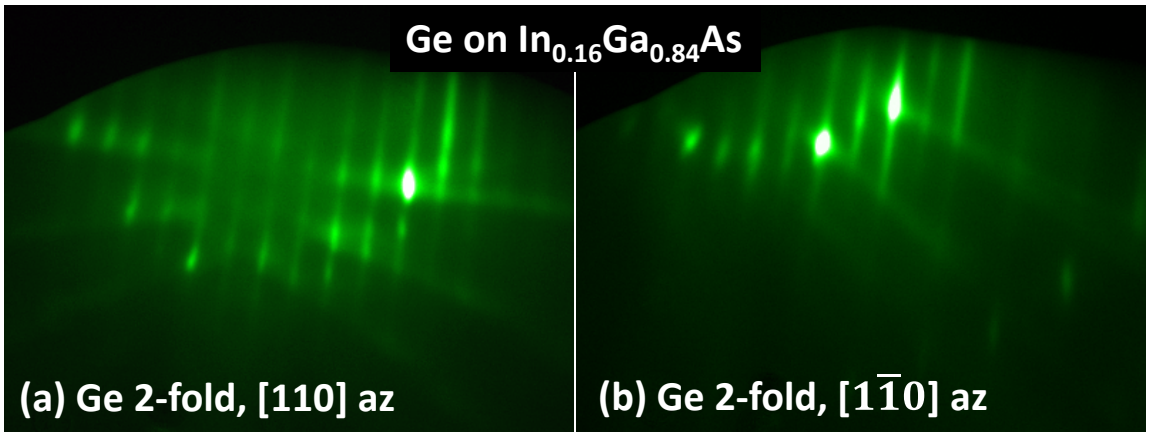


**Figure 8.2** RHEED patterns from the surface of 15nm Ge on $In_{0.16}Ga_{0.84}As$ along (a) [110] and [1$\bar{1}$0] azimuth. The RHEED patterns exhibited a (2×2) Ge surface reconstruction. The sharp and streak RHEED patterns indicate a high-quality Ge layer with smooth surface morphology. Used with permission from ACS.

The surface reconstruction of strained Ge was investigated by RHEED. Figure 8.2 shows the RHEED pattern of the Ge surface for the in-plane [110] and [1$\bar{1}$0] azimuths. The sharp and streaky (2x2) RHEED patterns indicate a high-quality Ge layer with smooth surface morphology. The RHEED patterns exhibited a (2×2) Ge surface reconstruction, which was also observed in our early studies from *in-situ* growth of Ge on (100) GaAs [17, 18]. The symmetric (004) rocking curve, symmetric (004) and asymmetric (115) RSMs from this structure are shown in Figs. 8.3 (a), (b) and (c), respectively, with each layer labeled to its corresponding peak or reciprocal lattice point (RLP). As can be seen from Fig. 8.3 (a), different from the XRD spectra of Ge grown on GaAs (shown in references 17, 18), the Ge peak in this study shows a larger Bragg angle than the GaAs substrate peak, relating to a smaller out-of-plane lattice constant, indicating the presence of in-plane tensile strain in the Ge layer. As shown in the inset of Fig. 8.3(a), due to the larger lattice constant of $In_{0.16}Ga_{0.84}As$ layer, the in-plane lattice constant of Ge layer grown on $In_{0.16}Ga_{0.84}As$ was stretched to match the in-plane lattice constant of $In_{0.16}Ga_{0.84}As$, resulting in a tensile strained Ge layer with expanded in-plane lattice constant

(labeled as *a*) and reduced out-of-plane lattice constant (labeled as *c*). The detailed analysis of the tensile strain values and relaxation state of Ge was conducted by accounting for the symmetric (004) and asymmetric (115) RSMs as shown in Figs. 8.3 (b) and (c), respectively. From these RSMs, the in-plane lattice constant (*a*) and out-of-plane lattice constant (*c*) of Ge and $In_{0.16}Ga_{0.84}As$ were extracted. The relaxed lattice constants ($a_r$) of each layer were calculated using *a* and *c* together with the Poisson's ratio of each material [10, 20]. Table 8.1 summarizes the values of extracted in-plane, out-of-plane and relaxed lattice constant of $In_{0.16}Ga_{0.84}As$ and Ge layers. Using the relaxed lattice constant of InGaAs and Vegard's law, the In composition in InGaAs channel/drain layers was determined to be 15.7%, which is consistent with the designed value. Besides, the $In_{0.16}Ga_{0.84}As$ layer was ~90% relaxed with respect to the GaAs substrate, indicating that the $In_xGa_{1-x}As$ linearly graded buffer efficiently accommodates the lattice mismatch induced strain between the $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate. In addition, in-plane tensile strain of 0.75% was determined within the Ge layer. The relaxation state of Ge with respect to $In_{0.16}Ga_{0.84}As$ is only limited to be ~9%, suggesting the pseudomorphic nature of the Ge layer. Furthermore, it can also be found from the asymmetric (115) RSM as shown in Fig. 8.3(c) that the Ge RLP is aligned in a vertical line [fully strained line, red dashed line in Fig. 8.3(c)] with $In_{0.16}Ga_{0.84}As$, which additionally confirms the pseudomorphic properties of the Ge layer. The 0.75% tensile strain within the Ge layer can reduce the band gap energy of Ge [14, 16] and prevent the generation of misfit dislocations, all of which are desirable to improve the performance of TFET devices.

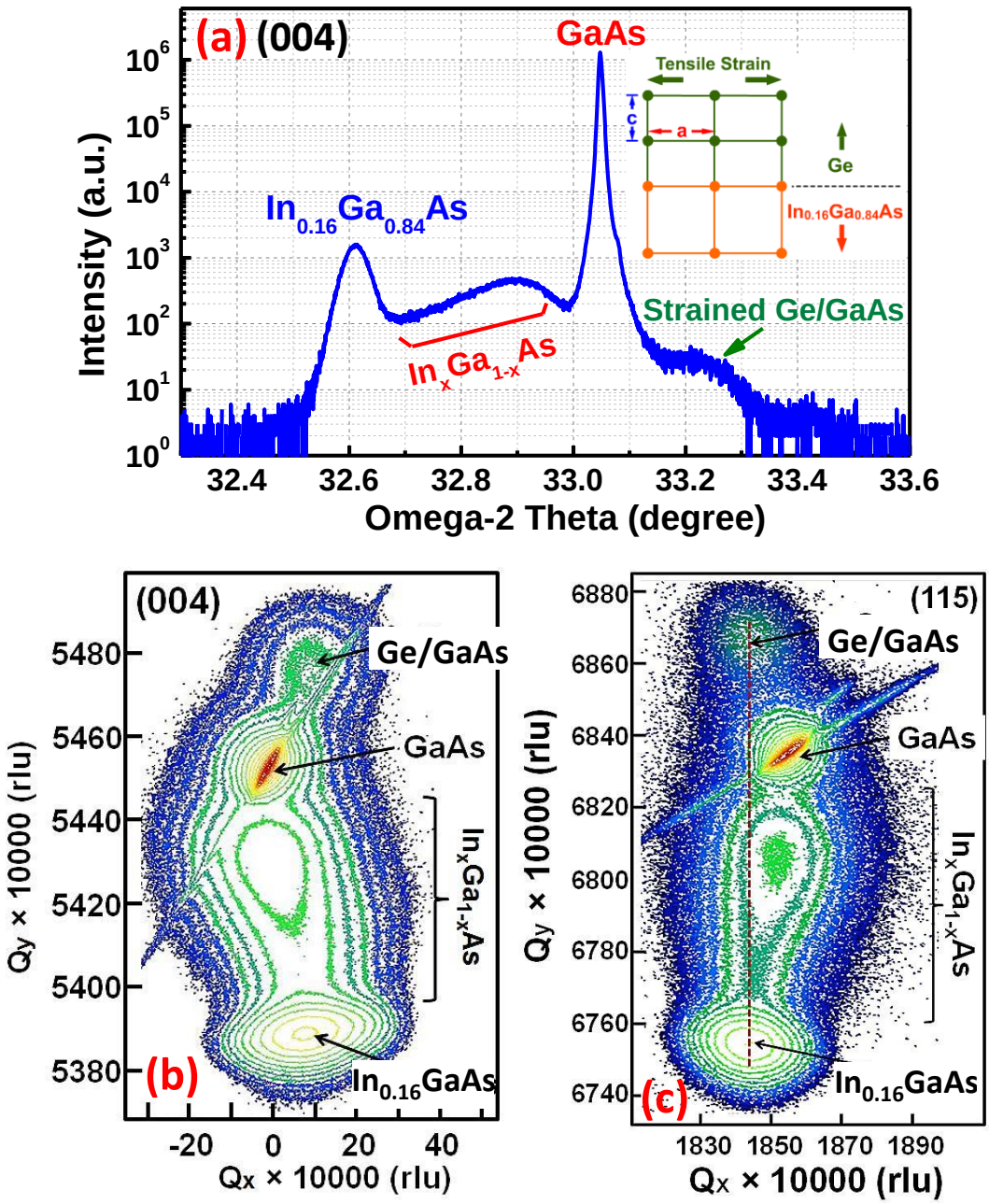


**Figure 8.3** (a) Symmetric (004) rocking curve (ω/2θ scan) of the Ge/$In_{0.16}Ga_{0.84}As$ structure. The Ge peak shows a larger Bragg angle than GaAs substrate, indicating a smaller out-of-plane lattice constant, suggesting the presence of in-plane tensile strain in the Ge layer. The insect shows the schematic of tensile strained Ge lattice on $In_{0.16}Ga_{0.84}As$. (b) Symmetric (004) and asymmetric (115) reciprocal space maps of the TFET structure. The in-plane tensile strain value inside of Ge layer is determined to be 0.75% and the relaxation state of Ge with respect to $In_{0.16}Ga_{0.84}As$ is limited to be ~9%. Used with permission from ACS.

**Table 8.1.** Summary of out-of-plane, in-plane and relaxed lattice constants of $In_{0.16}Ga_{0.84}As$ and Ge layers[a].

[a]The in-plane tensile strain of Ge is $\varepsilon = (a - a_r)/a_r = 0.75\%$

| Material | Lattice constants (Å) | | |
|---|---|---|---|
| | Out-of-plane ($c$) | In-plane ($a$) | Relaxed ($a_r$) |
| $In_{0.16}Ga_{0.84}As$ | 5.7201 | 5.7123 | 5.7164 |
| Ge | 5.6275 | 5.7121 | 5.6698 |

### 8.3.2 Interface and dislocation properties

Further insight into the crystalline quality and the $Ge/In_{0.16}Ga_{0.84}As$ heterointerface is provided by high resolution cross-sectional TEM analysis. For the sake of confirmation, TEM analysis was conducted on various spots and the representative results are shown in Figure 8.4. Figure 8.4 (a) shows the cross-sectional TEM micrograph of the $Ge/In_{0.16}Ga_{0.84}As$ TFET structure with a low magnification and all layers are labeled in this figure. It can be seen that the $In_xGa_{1-x}As$ linearly graded buffer layer effectively accommodates the lattice mismatch between the $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate by formation of dislocations. Most of the dislocations were confined within the linearly graded $In_xGa_{1-x}As$ buffer. The $In_{0.16}Ga_{0.84}As$ channel/drain layers and the lattice matched GaAs/Ge source region has a minimal dislocation density which cannot be detected at this magnification. As the linearly graded buffer relaxed most of the lattice mismatch induced strain, the residual strain within the top $In_{0.16}Ga_{0.84}As$ channel/drain layers is small (<0.1%), which is in agreement with the XRD analysis. The graded buffer provided a high-quality "virtual" substrate for the active layers ($GaAs/Ge/In_{0.16}Ga_{0.84}As$) of the TFET structure. Further investigation of the tensile strained Ge layer and the $Ge/In_{0.16}Ga_{0.84}As$ heterointerface were performed using a high magnification TEM micrograph as shown in Fig. 8.4 (b). Uniform thickness of the Ge layer with a smooth $Ge/In_{0.16}Ga_{0.84}As$

heterointerface was observed in Fig. 8.4 (b) in a relative long range. Figure 8.4 (b) also shows high contrast between the Ge/$In_{0.16}Ga_{0.84}As$ as well as the GaAs/Ge heterointerfaces. The sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is also benefited to reduce the effective tunneling barrier width

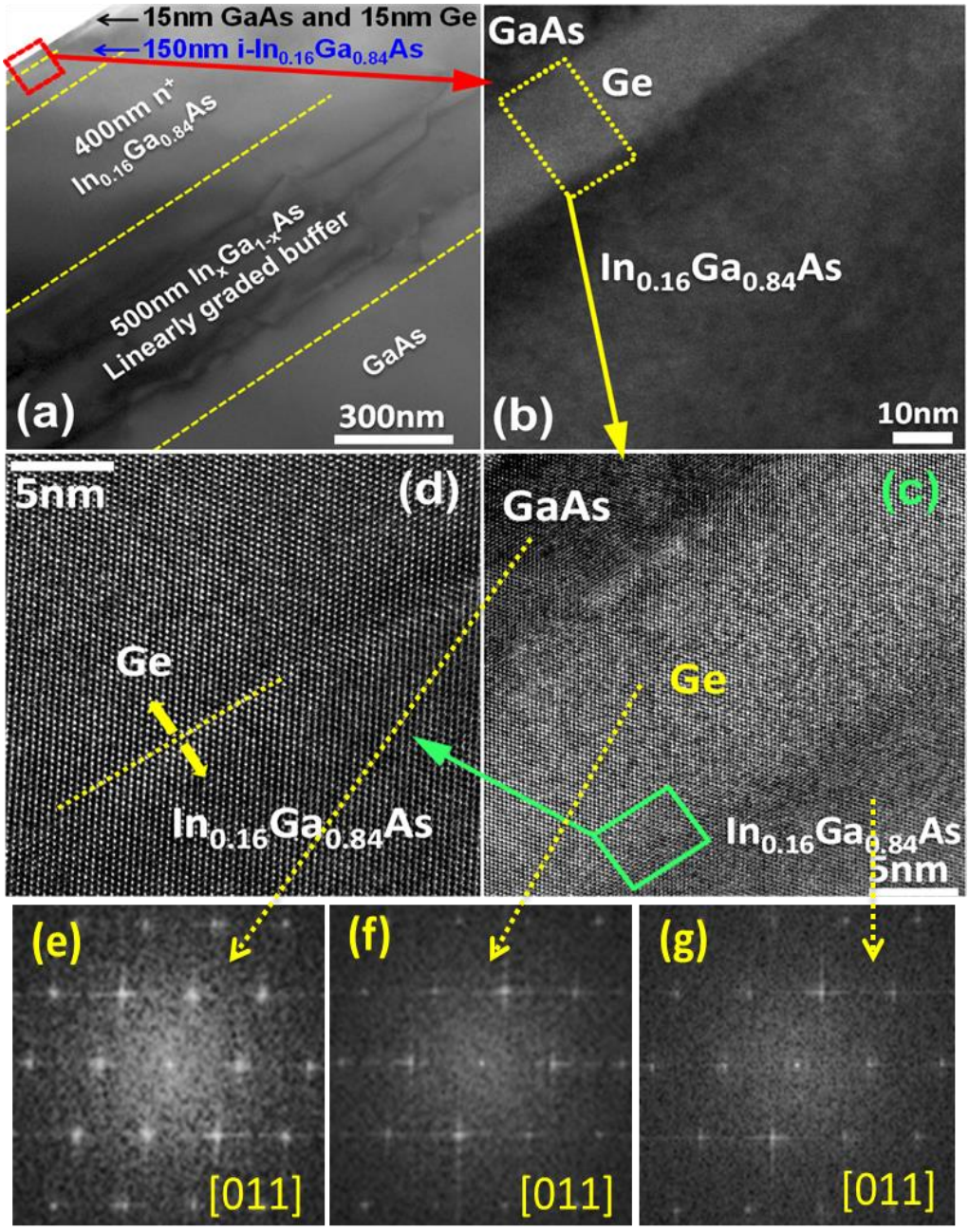


**Figure 8.4** (a) Cross-sectional TEM micrograph of the TFET structure with each layer labeled in this figure. The $In_xGa_{1-x}As$ linearly graded buffer effectively accommodates the lattice mismatch between $In_{0.16}Ga_{0.84}As$ channel/drain layers and the GaAs substrate. No dislocations are observed in the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ active

layers at this magnification. (b) High magnification TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces. Uniform thickness of the Ge layer with a smooth Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was observed in this figure in a relative long range. A sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface was also shown in this figure, indicating minimal atoms inter-diffusion. (c) High-resolution TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces. No dislocations were observed at the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface and within the Ge layer, suggesting the pseudomorphic of the Ge layer. (d) A zoomed-in view of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface. A defect free interface with well aligned lattice indexing is shown in this figure. (e)-(f) Fast Fourier Transform patterns (FFT) corresponding to various layers marked with arrows in (c). Used with permission from ACS.

and increase in tunneling current of TFET devices [2-7, 21]. High-resolution TEM micrograph of the GaAs/Ge/$In_{0.16}Ga_{0.84}As$ heterointerfaces as indicated in the dashed box of Fig. 8.4 (b) is shown in Fig. 8.4 (c). No dislocations were observed at the heterointerfaces as well as within the Ge layer at this magnification, suggesting the pseudomorphic nature of the Ge which is consistent with the results from the XRD measurement. A selected high magnification view of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface is shown in Fig. 8.4 (d). A defect free interface with atomic scale periodicity can be observed in this figure. Figures 8.4 (e)-(g) shows Fast Fourier Transform (FFT) patterns corresponding to the region marked with arrows in Fig. 8.4 (c). The indexing of these FFT patterns indicates that the electron beam was parallel to [011] orientation. It can also be observed that the FFT patterns recorded from various layers are similar with the same zone axis. Moreover, the FFT patterns obtained from both the interfacial areas are the same with absence of any spot splitting or satellite peaks, which further indicates high quality epitaxial growth with coherent interfaces. The high-resolution TEM analysis of the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure shows a sharp Ge/$In_{0.16}Ga_{0.84}As$ interface and dislocation free GaAs/Ge/$In_{0.16}Ga_{0.84}As$ active layers. The results from the TEM analysis indicate the high quality of the films with atomic smoothness reflecting the overall defect-free structure. This optimization of the growth parameters in conjunction with the atomic scale imaging is significant

achievement towards demonstrating the correlated synthesis – structure – property behavior. In conjunction with the presence and control of the resulting tensile strain in Ge layer the intended property was obtained in terms of the band diagram.

### 8.3.3 Surface morphology

Characterization of the surface morphology is another important metric for metamorphic structures due to the development and propagation of 60 ° *a*/2 <110> {111} misfit dislocations within the linearly graded buffer during the relaxation of strain [22-24]. These dislocations glide along {111} planes and thread at 60 ° angle toward the surface along <110> directions, resulting in a cross-hatch pattern on the sample surface [22-24]. Figure 8.5 shows the 20μm×20μm AFM micrograph of the TFET structure, which shows the anticipated two-dimensional (2D) cross-hatch surface morphology. The 2D cross-hatch patterns are well-developed and quite uniform along the [110] and [$1\bar{1}0$] directions, as labeled in this figure. Line profiles in the two orthogonal <110> directions are also included in this figure, showing a low a peak-to-valley height of less than 5 nm. The uniform distribution of the cross-hatch pattern along [110] and [$1\bar{1}0$] directions suggests a symmetric strain relaxation of the linearly graded buffer layer. Besides, the AFM analysis shows a smooth surface with a root-mean-square (*rms*) roughness of 1.26 nm. The well-developed 2D cross-hatch pattern indicates ideal strain relaxation of the linearly graded buffer and low surface *rms* roughness suggests high crystalline quality of the TFET structure. Besides, the 2D cross-hatch pattern also confirm the strained nature of the Ge layer, otherwise, this cross-hatch pattern will be sheltered by dislocations and a grainy texture with much higher *rms* roughness will appear on the surface [10].

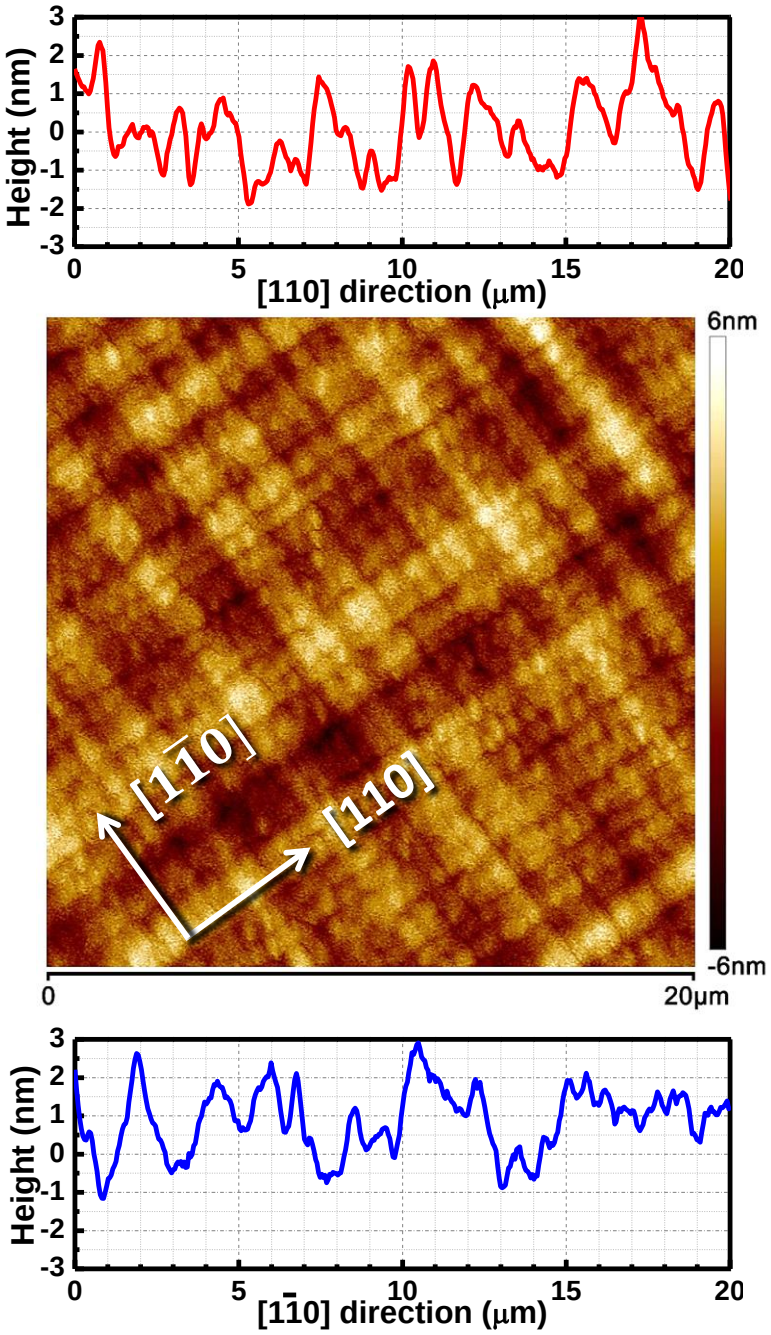


**Figure 8.5** 20μm×20μm AFM micrograph of the TFET structure shows anticipated two-dimensional cross-hatch patterns. Line profiles in the two orthogonal <110> directions are also included. The uniform distribution of the cross-hatch pattern along [110] and [1$\bar{1}$0] directions suggests a symmetric strain relaxation of the linearly graded buffer. The well-developed two-dimensional cross-hatch patterns suggest the pseudomorphic nature of the Ge layer. The AFM analysis shows a smooth surface morphology of the TFET structure with a root-mean-square (rms) roughness of 1.26nm. Used with permission from ACS.

### 8.3.4 Band alignment properties

The band alignment properties of the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure were determined using XPS by measuring the binding energy from core levels (CL) of Ge3d/As$3d_{5/2}$ and valence band maxima (VBM) of Ge and $In_{0.16}Ga_{0.84}As$, respectively, using Kraut's method [25-29].

XPS spectra were collected from three samples: (1) 15 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ was used to measure the CL and VBM binding energy of Ge; (2) 150 nm $In_{0.16}Ga_{0.84}As$ without the top Ge layer was used to measure the CL binding energy of As and VBM of $In_{0.16}Ga_{0.84}As$; (3) 1.5 nm Ge/150 nm $In_{0.16}Ga_{0.84}As$ was used to measure CL binding energy of Ge and As at the heterointerface. Native oxide on the surface of each sample was removed using wet etching process [18]. Figure 8.6 (a) - (c) shows the CL and VB spectra from each sample. The insect shows the schematic layer diagram of the sample used for each measurement. All measured binding energy values are summarized in Table 8.2. From the XPS measurements, the values of $E^{Ge}_{Ge\ 3d} - E^{Ge}_{VBM}$, $E^{InGaAs}_{As\ 3d_{5/2}} - E^{InGaAs}_{VBM}$ and $\Delta E_{CL}(i)$ are determined to be 29.32 eV, 40.56 eV and 11.55 eV, respectively. The VBO is determined to be 0.31 ±0.05 eV. The uncertainty value is from the scatter of VB data with respect to the fitting in VBM position. The bandgap energy of intrinsic $In_{0.16}Ga_{0.84}As$ at 300K is found to be ~1.19 eV by the commonly used equation given by Nahory *et al* [30]. The reduced Ge indirect bandgap energy of 0.64 eV was used due to the splits of energy levels for the light hole and heavy hole bands at the VBM point caused by 0.75% tensile strain [16, 31]. Using these data, the CBO is calculated to be ~0.24 eV. Figure 8.7 (a) shows the schematic band alignment diagram of the Ge/$In_{0.16}Ga_{0.84}As$ heterojunction based on the present result above. In addition, a Ge/GaAs TFET was also grown using the same *in-situ* MBE growth process to compare the band alignment difference. The band alignment properties of this structure were also investigated by XPS. The energy band diagram of the Ge/GaAs

structure is shown in Fig. 8.7 (b). The VBO and CBO values of Ge/GaAs TFET heterostructure were determined to be ~0.21 eV and ~0.54 eV, respectively. Compared with the measured band offset values from the Ge/$In_{0.16}Ga_{0.84}As$ structure (~0.31 eV for VBO and ~0.24 eV for CBO), it can be seen that the VBO value increased with the increase of In composition but the CBO value decreased. Besides, preliminary band alignment studies of a Ge/$In_{0.53}Ga_{0.47}As$ heterostructure showed further reduction of CBO and a staggered band alignment. The increase of In composition in InGaAs layer will reduce the bandgap energy of InGaAs material, increase the amount of in-plane tensile strain of the Ge layer deposited on InGaAs and decrease the effective tunneling barrier height ($E_{beff} = E_{G,\ Ge} + \Delta E_C$), all of which will improve the performance of TFET devices. However, further increase of In composition in InGaAs layer will drastically reduce the critical layer thickness of Ge (e.g. the critical thickness of Ge on $In_{0.16}Ga_{0.84}As$ is ~25nm and it reduced to ~7.6nm if the In composition is increased to 53%) and thus potentially introduce defects at the heterointerface and inside the Ge layer [13], which is detrimental for device performances [10, 13, 26]. As a result, a balance of Indium composition is essential in order to obtain a tensile strained Ge layer with defect-free high crystalline quality.

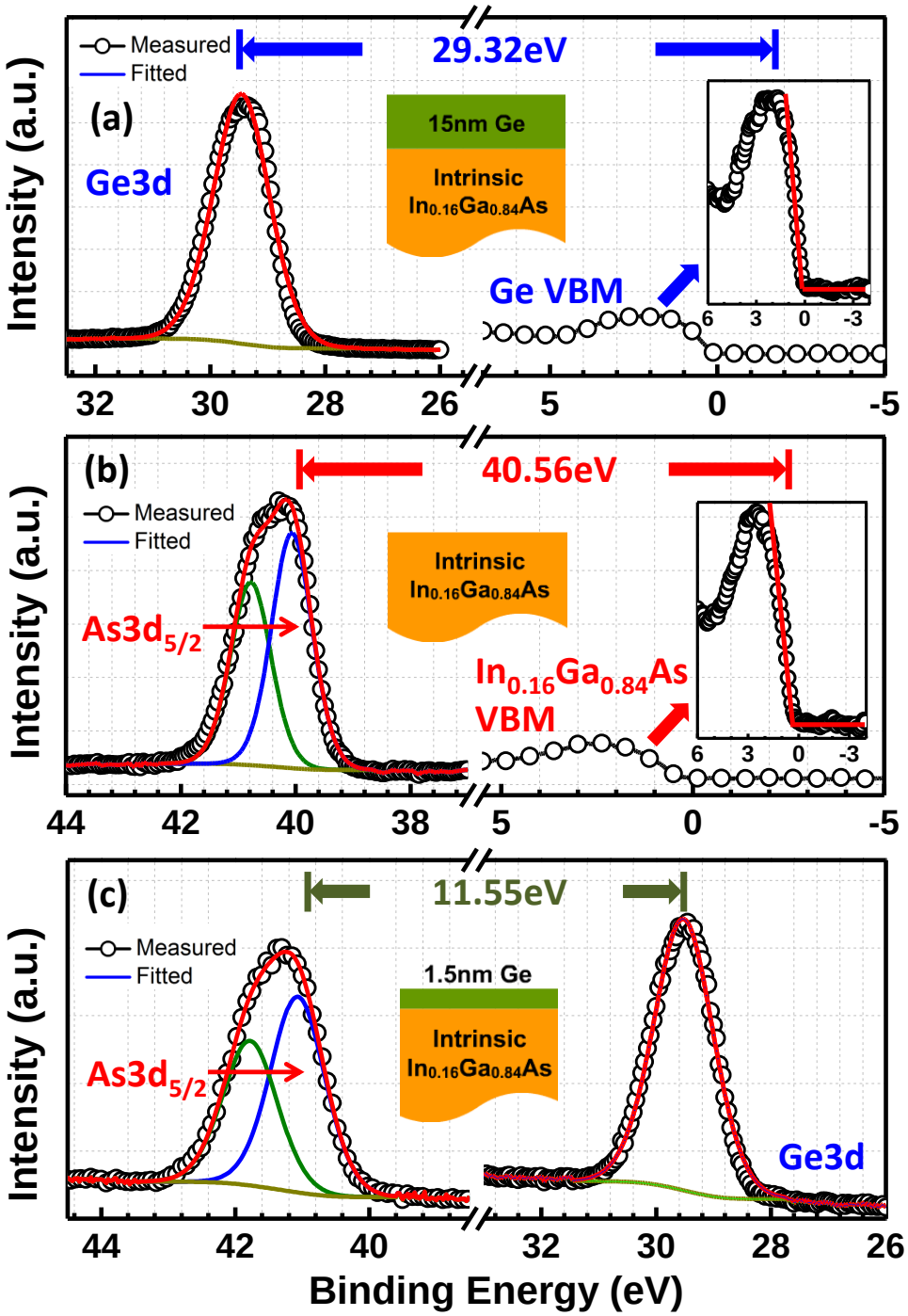


**Figure 8.6** XPS spectra of (a) Ge3d core level and valence band from 15nm Ge/150nm $In_{0.16}Ga_{0.84}As$ sample; (b) As3d core level and $In_{0.16}Ga_{0.84}As$ valence band from 150nm $In_{0.16}Ga_{0.84}As$ without the Ge layer and (c) As3d and Ge3d core level from 1.5nm Ge/150nm $In_{0.16}Ga_{0.84}As$ measured at the interface. The insect shows the schematic layer diagram of the sample used in each measurement. The valence band offset value at Ge/ $In_{0.16}Ga_{0.84}As$ heterointerface is determined to be 0.31 ±0.05eV using the measured XPS spectra. Used with permission from ACS.

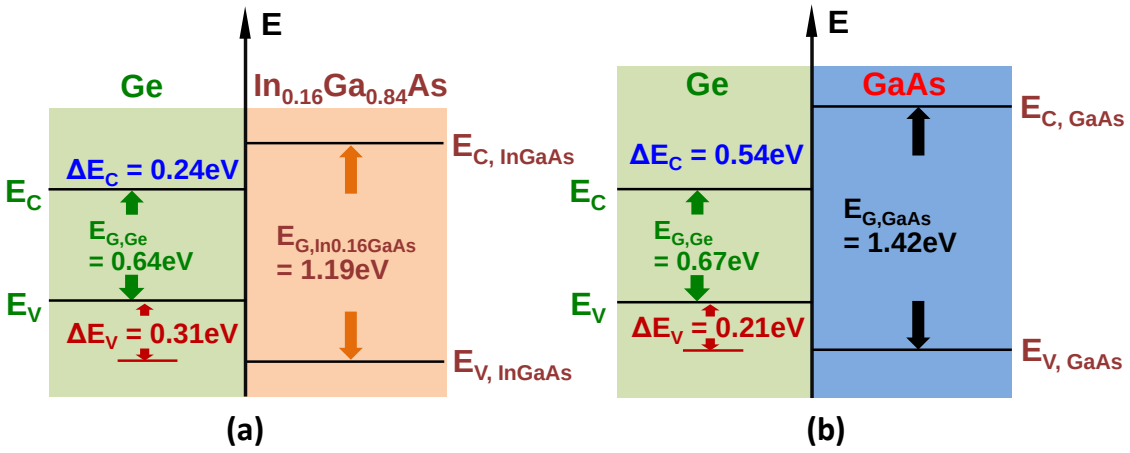


**Figure 8.7** (a) Schematic energy band diagram of the Ge/$In_{0.16}Ga_{0.84}As$ heterointerface in the TFET structure and (b) band diagram of the Ge/GaAs heterostructure. The conduction band offset was much reduced in the Ge/$In_{0.16}Ga_{0.84}As$ heterostructure by utilizing tensile strain inside of Ge. Used with permission from ACS.

**Table 8.2** Summary of measured XPS CL and VBM values from different samples.

| Sample | States | Binding Energy (eV) |
|---|---|---|
| 15nm Ge/150nm $In_{0.16}Ga_{0.84}As$ | Ge3d | 29.45 |
| | VBM | 0.13 |
| 150nm $In_{0.16}Ga_{0.84}As$ | $As3d_{5/2}$ | 41.05 |
| | VBM | 0.49 |
| 1.5nm Ge/150nm $In_{0.16}Ga_{0.84}As$ | Ge3d | 41.08 |
| | $As3d_{5/2}$ | 29.53 |

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# Chapter 9 Conclusion and Prospects

## 9.1 Summary

Tunnel field-effect transistor has been proposed as one of the most promising steep-slope-switch candidates to be used under a supply voltage below 0.3V for ultra-low standby power logic applications. The unique band-to-band tunneling transport mechanism enables TFET to offer significantly reduced subthreshold slope (SS) thereby lower operation voltage and power dissipation. Using group III-V materials in a TFET structure significantly improves the ON-state current and reduces SS due to the low bandgap energies as well as smaller carrier tunneling mass. The mixed arsenide/antimonide $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ heterostructure allows a wide range of bandgap energies and various staggered band alignments depending on the alloy compositions in the source and channel materials. Band alignments at source/channel heterointerface can be well modulated by carefully controlling the compositions in the $In_xGa_{1-x}As/GaAs_ySb_{1-y}$ material system. The tensile strained $Ge/In_xGa_{1-x}As$ heterostructures provide an alternative path to further upgrade the performance of TFET devices. In this research, structural properties and device performances of TFETs using mixed As/Sb and tensile strained $Ge/In_xGa_{1-x}As$ heterostructures were systemically investigated. The works are summarized below:

(1) Mixed anion $GaAs_ySb_{1-y}$ materials in a wide Sb composition range of 15% ~ 62% were achieved by molecular beam epitaxy (MBE). The influence of different growth parameters, such as growth temperature, Sb/Ga ratio, As/Ga ratio, *etc.*, on the alloy composition was systemically investigated. Three different high-κ gate dielectric, *i. e.*, $Al_2O_3$, $HfO_2$, $Ta_2O_5$, were integrated on $GaAs_{0.38}Sb_{0.62}$ material by atomic layer deposition. The band alignment of these different high-κ gate dielectric materials on $GaAs_{0.38}Sb_{0.62}$ was investigated by x-ray photoelectron spectroscopy (XPS). All these three high-κ gate dielectric provide more than 2eV valence band offset on

$GaAs_{0.38}Sb_{0.62}$, indicating the potential applications for p-type FETs. For the conduction band alignment, both $Al_2O_3$ and $HfO_2$ can provide a conduction band offset (CBO) value higher than 2eV, however, the CBO value of $Ta_2O_5$ on $GaAs_{0.38}Sb_{0.62}$ is limited to be 0.71eV due to the limited band gap energy of $Ta_2O_5$.

(2) The strain relaxation behavior, surface morphology and dislocation properties of MBE grown mixed As-Sb tunnel FET heterostructures with GaAs-like and InAs-like interface at the source/channel region were investigated. The OFF-state leakage current transport mechanisms of these tunnel FET devices with two different interfaces were studied. Both GaAs-like and InAs-like interface TFET structures exhibited symmetric strain relaxation. However, the GaAs-like interface introduced high dislocation density, while the InAs-like interface creates a defect-free interface for the pseudomorphic growth of the $In_{0.7}Ga_{0.3}As$ channel and drain layer. Higher OFF-state leakage current dominated by band-to-band tunneling process was observed in the GaAs-like interface TFET while the device with InAs-like interface exhibited significantly low OFF-state leakage current. The band alignment properties of these structures were investigated using XPS. Experimental results confirmed that the band alignment of the GaAs-like interface structure was converted from staggered gap to broken gap due to high defect density at the interface. Therefore, a proper selection of $E_{beff}$ and a high quality source/channel interface with well-maintained low defect density is essential in a mixed As/Sb TFET structure in order to achieve high ON-state current and low OFF-state leakage.

(3) The reliability of structural and electrical properties of mixed As/Sb staggered gap TFETs for high-temperature operation was investigated comprehensively from 25$^{o}$C to 150$^{o}$C. Temperature dependent x-ray diffraction (XRD), atomic force microscopy (AFM) and secondary ion mass spectrometry (SIMS) measurements suggest no significant structural properties change

during high temperature operation. The leakage current of the fabricated $p^+$-i-$n^+$ diode increased exponentially with increasing temperature due to Shockley-Read-Hall generation-recombination mechanism. The ON-state drain current showed weak temperature dependence, and it decreased with increasing temperature from 25$^o$C to 100$^o$C due to the variation of Fermi distribution and the increase in channel resistance but increased from 100$^o$C to 150$^o$C due to the reduction of both bandgap energy as well as the effective tunneling barrier height. The subthreshold slope has a strong positive temperature dependent property especially at higher temperature due to trap-assistant tunneling process. The temperature dependent structural and device properties of the mixed As/Sb staggered gap TFET highlights the importance of the reliability on high temperature operation of TFETs for future low-power digital logic applications.

(4) Structural properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type TFET structure grown by MBE were comprehensively investigated. High resolution XRD revealed symmetric strain relaxation and pseudomorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ active layers, indicating a low dislocation density within the active region. The surface morphology of this structure exhibited a typical two-dimensional cross-hatch pattern with a low root-mean-square (*rms*) roughness of 2.58nm. Cross-sectional transmission electron microscopy (TEM) demonstrated a low threading dislocation density within the active region. Dynamic SIMS exhibited an abrupt doping profile over the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ source/channel junction as well as minimal level of intermixing between As and Sb atoms. These structural properties showed high quality of this structure and provided critical guidance for the fabrication of As/Sb based staggered gap complementary TFETs for ultra-low standby power and energy efficient logic applications.

(5) Tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure was grown *in-situ* by MBE using two separated growth chambers for Ge and III-V materials. Controlled growth conditions led to the

presence of 0.75% in-plane tensile strain within Ge layer. High-resolution TEM confirmed pseudomorphic Ge with high crystalline quality and a sharp Ge/$In_{0.16}Ga_{0.84}As$ heterointerface. AFM revealed a uniform two-dimensional cross-hatch surface morphology with an *rms* roughness of 1.26nm. XPS demonstrated reduced tunneling-barrier-height compared with Ge/GaAs heterostructure. The superior structural properties suggest tensile strained Ge/$In_{0.16}Ga_{0.84}As$ heterostructure would be a promising candidate for high-performance and energy-efficient tunnel field-effect transistor applications.

This research show superior structural properties and excellent device performances of TFETs using mixed As/Sb and tensile strain Ge/$In_xGa_{1-x}As$ heterostructures, which indicates TFET as a promising path for low standby power logic application. Experimental results along with device simulations demonstrated the potential performance improvement within these heterostructures and leap forward a path to be further optimized. Such TFETs would provide excellent opportunities to be integrated with Si-MOSFETs as ultra-low power devices in an advanced hybrid circuit platform and also provide chances to replace MOSFET for beyond CMOS applications.

## 9.2 Prospects for future works

This research explores and evaluates the structural properties and device performances of TFETs using mixed As/Sb and tensile strained Ge/$In_xGa_{1-x}As$ heterostructures. In order to fully exploit the advantages of TFET devices, future investigations can be done in the following areas:

(1) Future increase of ON-state current of TFETs using mixed As/Sb heterostructures can be achieved by reducing $E_{beff}$ by modulating the In and Sb compositions to even higher levels in each side. The graded buffer layer should be re-designed to accommodate the increased lattice mismatch. In this case, the possibility of generating threading dislocations in the active region

will be higher than the structure with less lattice mismatch. Besides, higher Sb composition in the $GaAs_ySb_{1-y}$ layer indicates larger composition change from Sb-rich $GaAs_ySb_{1-y}$ layer to As-rich $In_xGa_{1-x}As$ layer during MBE growth and measures must be taken in order to preserve the internally lattice matched condition. New buffer layers should be designed to more effectively accommodate the larger lattice mismatch between active layers and the substrate. Furthermore, the switching sequence at the mixed As/Sb heterointerface should be further optimized in order to accommodate the larger change of the group-V fluxes.

Another stratagem to reduce $E_{beff}$ without significantly increasing lattice mismatch between the active region and the substrate is to insert high In/Sb composition thin pocket layers at the source/channel heterointerface. The advantage of this approach is that it can modulate the $E_{beff}$ at the heterointerface without changing the compositions of the entire active area. Therefore, the lattice mismatch value and strain properties of the active region will be kept similar as the existed structure. As a result, the same graded buffer scheme as well as source/channel/drain materials can be used for the demonstration of mixed As/Sb staggered gap TFET structures with different $E_{beff}$ for further increase in $I_{ON}$. Besides, the thickness of the inserted high composition layer should be below the critical layer thickness, so that no lattice mismatch induced dislocations are expected at the source/channel heterojunction, which guarantees the high crystalline quality of the active region.

(2) Most fabricated mixed As/Sb staggered gap TFETs show high value of SS due to high interface traps between the gate oxide and the channel. Improved surface passivation chemistry might suppress these dominant mid-gap traps that will improve SS in future TFET devices. New surface passivation techniques should be investigated to effectively reduce the interface trap density without introducing any structural property degradation. Besides, further reliability

studies should be taken to characterize the material properties of new structures at higher temperature.

(3) One of the final objectives of the research of the mixed As/Sb staggered gap TFET structure is heterogeneously integrated onto Si substrate. Heteroepitaxy of this structure on large diameter, cheaper, and readily available Si substrate will not only offer a path for low cost and high-performance mixed As/Sb staggered gap TFET but also significantly increase their yield per die. However, viability of III–V TFET structures on Si relies on the ability to grow high-quality GaAs buffer layer on Si with careful lattice engineering and substrate treatment. The polar-on-nonpolar epitaxy and the 4% lattice mismatch between GaAs and Si may result in the formation of various defects and dislocations. These dislocations can propagate into the active region, significantly changing the band alignment and therefore impeding the performance the device. As a result, high quality buffer layers on Si is needed in future research to integrate the mixed As/Sb staggered gap TFETs on Si substrate with similar performances of that on InP substrate.

(4) In the past recent years, great efforts have been devoted to boost performances of the mixed As/Sb staggered gap TFET. However, most of the researches were restricted to n-channel TFETs. A study of high-performance p-channel TFET within the same material system is equally important, without which the energy efficient complementary logic circuits will not be realized. In this respect, more efforts should be devoted onto the research of high performance p-channel TFETs using the mixed As/Sb and tensile Ge based heterostructures to realize a complementary TFET logic application.

# Appendix

## List of publications in Virginia Tech

### JOURNAL PAPERS:

1. **Y. Zhu**, D. Maurya, S. Priya, and M. K. Hudait, "Tensile Strained Nano-scale Ge/$In_{0.16}Ga_{0.84}As$ Heterostructure for Tunnel Field-Effect Transistor", *ACS Appl Mater Interfaces* (Accepted, 2014)

2. **Y. Zhu**, N. Jain, D. Maurya, R. Varghese, S. Priya, and M. K. Hudait, "X-ray photoelectron spectroscopy analysis and band offset determination of $CeO_2$ deposited on epitaxial (100), (110) and (111)Ge", *J. Vac. Sci. Technol.* B **32**, 011217 (2014).

3. N. Jain, **Y. Zhu**, D. Maurya, R. Varghese, S. Priya, and M. K. Hudait, "Interfacial band alignment and structural properties of nanoscale $TiO_2$ high-k gate dielectric for integration with epitaxial crystallographic oriented germanium", *J. Appl. Phys.* **115**, 024303 (2014).

4. B. Rajamohanan, D. Mohata, **Y. Zhu**, M. K. Hudait, Z. Jiang, M. Hollander, G. Klimeck, and S. Datta, "Design, fabrication and analysis of P-channel Arsenide/Antimonide Hetero-junction Tunnel Transistors", *J. Appl. Phys.* **115**, 044502 (2014).

5. M. K. Hudait, **Y. Zhu**, N. Jain, D. Maurya, Y. Zhou, R. Varghese, and S. Priya, "$BaTiO_3$ Integration with Nanostructured Epitaxial (100),(110), and (111) Germanium for Multifunctional Devices", *ACS Appl. Mater. Interface* **5**, 11446 (2013).

6. **Y. Zhu**, M. K. Hudait, D. K. Mohata, B. Rajamohanan, S. Datta, D. Lubyshev, J. M. Fastenau, and Amy K. Liu, "Structural, morphological, and defect properties of metamorphic $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ p-type tunnel field effect transistor structure grown by molecular beam epitaxy", *J. Vac. Sci. Technol.* B **31**, 041203 (2013).

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9. **Y. Zhu,** N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, Amy K. Liu, and M. K. Hudait, "Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application", *J. Appl. Phys.* **113**, 024319 (2013).

10. M. K. Hudait, **Y. Zhu**, D. Maurya, Y. Zhou, R. Varghese, and S. Priya, "Quasi-zero lattice mismatch and band alignment of $BaTiO_3$ on epitaxial (110)Ge", *J. Appl. Phys.* **114**, 024303 (2013).

11. M. K. Hudait, **Y. Zhu**, D. Maurya, S. Priya, P. K. Patra, A.W. K. Ma, A. Aphale, and I. Macwan, "Structural and band alignment properties of $Al_2O_3$ on epitaxial Ge grown on (100), (110) and (111)A GaAs substrates by molecular beam epitaxy", *J. Appl. Phys.* **113**, 134311 (2013).

12. M. K. Hudait and **Y. Zhu**, "Energy band alignment of atomic layer deposited $HfO_2$ oxide film on epitaxial (100)Ge, (110)Ge and (111)Ge layers", *J. Appl. Phys.* **113**, 114303 (2013).

13. M. K. Hudait, **Y. Zhu**, S. W. Johnston, D. Maurya, S. Priya, and R. Umbel, "Ultra-high frequency photoconductivity decay in GaAs/Ge/GaAs double heterostructure grown by molecular beam epitaxy", *Appl. Phys. Lett.* **102**, 093119 (2013).

14. M. K. Hudait, **Y. Zhu**, D. Maurya, and S. Priya, "Energy band alignment of atomic layer deposited $HfO_2$ on epitaxial (110)Ge grown by molecular beam epitaxy", *Appl. Phys. Lett.* **102**, 093109 (2013).

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17. **Y. Zhu**, N Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. W. K. Liu, and M. K. Hudait, "Structural properties and band offset determination of p-channel mixed As/Sb type-II staggered gap tunnel field-effect transistor structure", *Appl. Phys. Lett.* **101**, 112106 (2012).

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20. **Y. Zhu**, M. Clavel and M. K. Hudait, "MBE growth, strain relaxation properties and high-κ dielectric integration of mixed anion $GaAs_ySb_{1-y}$ metamorphic materials", *ACS Appl Mater Interfaces* (*Planning*, 2014)

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1. M. K. Hudait, **Y. Zhu**, D. Maurya, and S. Priya, "Integration of high-k dielectrics on epitaxial (100), (110) and (111) germanium for multifunctional devices", $224^{th}$ ECS Meeting in San Francisco, California, Oct. 27 – Nov. 1, 2013.

2. D. K. Mohata, R. Bijesh, **Y. Zhu**, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan and S. Datta, "Demonstration of improved heteroepitaxy, scaled gate stack and reduced interface states enabling heterojunction tunnel FETs with high drive current and high on-off ratio" IEEE Symposia on VLSI Technology and Circuits, Honolulu, June 12-15, 2012.