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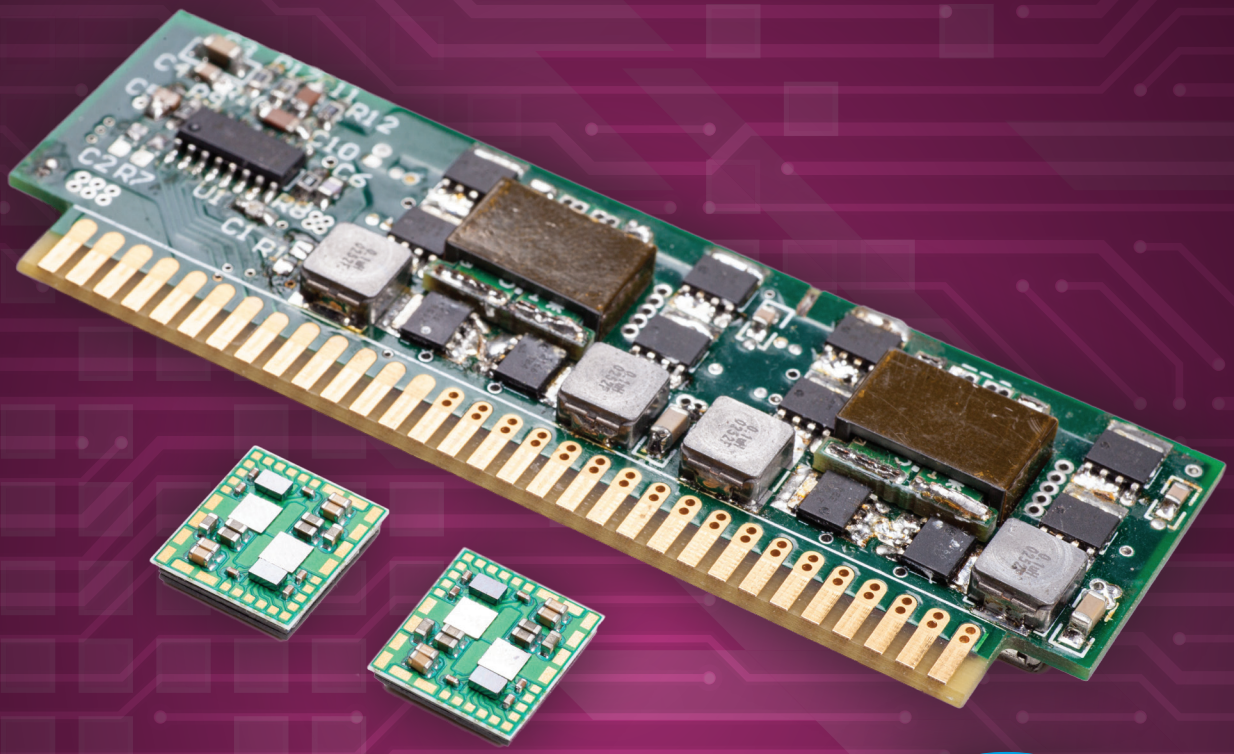

CPES
Center for Power Electronics Systems

2013 CPES ANNUAL REPORT

VIRGINIA TECH · BLACKSBURG, VIRGINIA

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Produced by Uncork-it, Inc.

INTRODUCTION

The Center for Power Electronics Systems at Virginia Tech is a research center dedicated to improving electrical power processing and distribution that impact systems of all sizes – from battery – operated electronics to vehicles to regional and national electrical distribution systems.

Our mission is to provide leadership through global collaborative research and education for creating advanced electric power processing systems of the highest value to society.

CPES, with annual research expenditures of $4-5 million US dollars, has a worldwide reputation for its research advances, its work with industry, and its many talented graduates. From its background as an Engineering Research Center for the National Science Foundation during 1998 - 2008, CPES has continued to work towards making electric power processing more efficient and more exact in order to reduce energy consumption.

Power electronics is the "enabling infrastructure technology" that promotes the conversion of electrical power from its raw form to the form needed by machines, motors and electronic equipment. Advances in power electronics can reduce power conversion loss and in turn increase energy efficiency of equipment and processes using electrical power. This results in increased industrial productivity and product quality. With widespread use of power electronics technology, the United States would be able to cut electrical energy consumption by 33 percent. This energy savings in the United States alone is estimated to be the equivalent of output from 840 fossil fuel based generating plants. This savings would result in enormous economic, environmental and social benefits.

OVERVIEW

CPES INDUSTRY CONSORTIUM

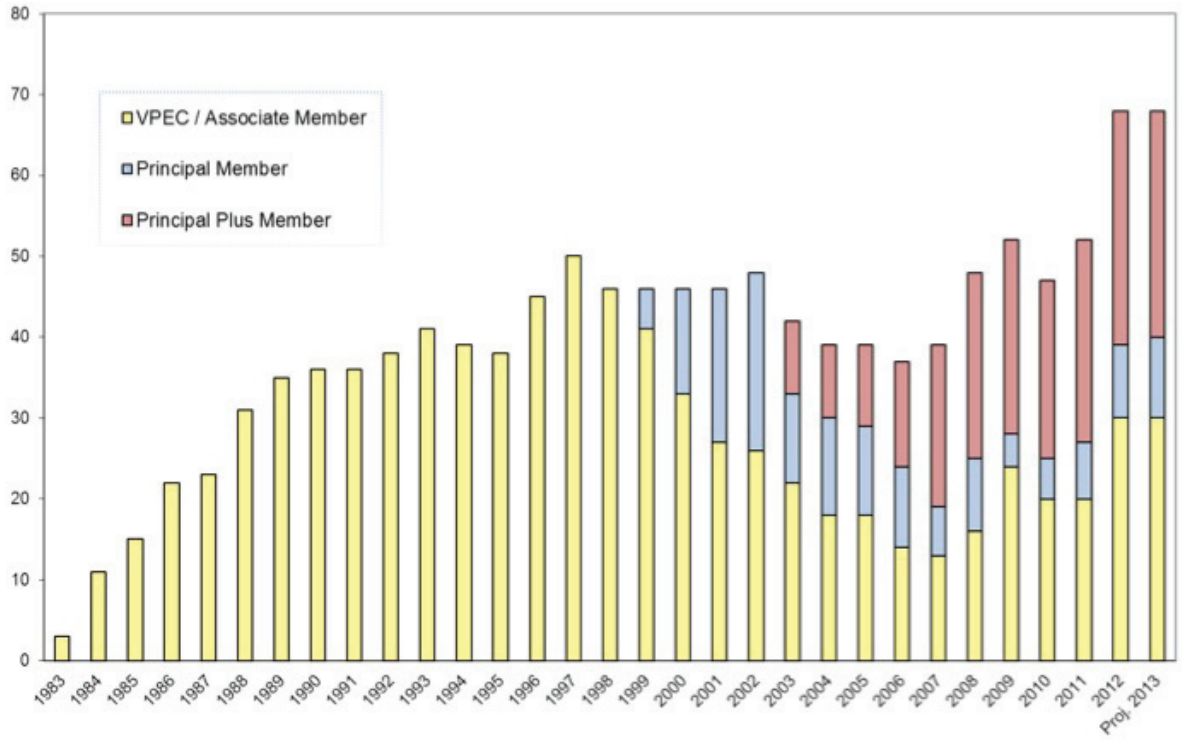
The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members.

The CPES industrial consortium offers:

- The best mechanism to stay abreast of technological developments in power electronics
- The ideal forum for networking with leading-edge companies and top-notch researchers
- The CPES connection provides the competitive edge to industry members via:
- Access to state-of-the-art facilities, faculty expertise, top-notch students
- Leveraged research funding of over $4-10 million per year
- Industry influence via Industry Advisory Board and research champions
- Intellectual properties with early access for Principal Plus and Principal members via CPES IPPF (Intellectual Property Protection Fund)
- Technology transfer made possible via special access to the Center's multi-disciplinary team of researchers, and resulting publications, presentations and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

CPES MEMBERSHIP COMPANY GROWTH



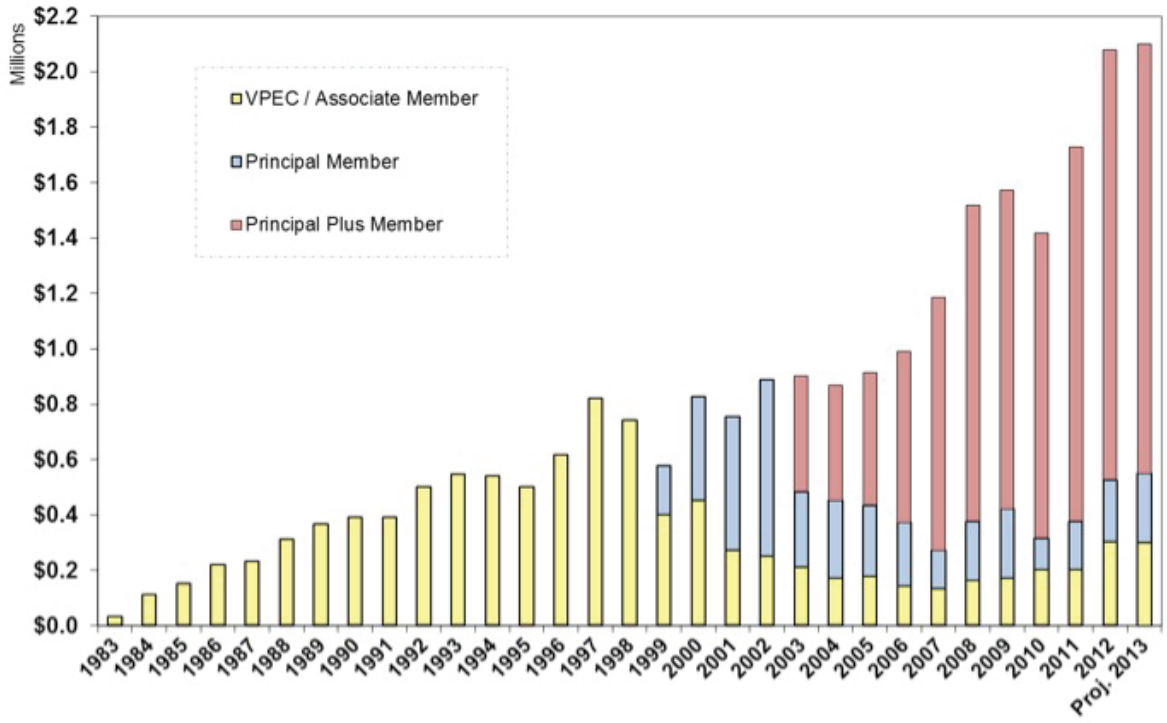
Principal Plus Members (annual contribution - $50,000) - gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research -- PMC (Power Management Consortium), HDI (High Density Integration), or REN (Renewable Energy and Nanogrids). They also have easy access to cutting-edge IPs via CPES IPPF (Intellectual Property Protection Fund). Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.

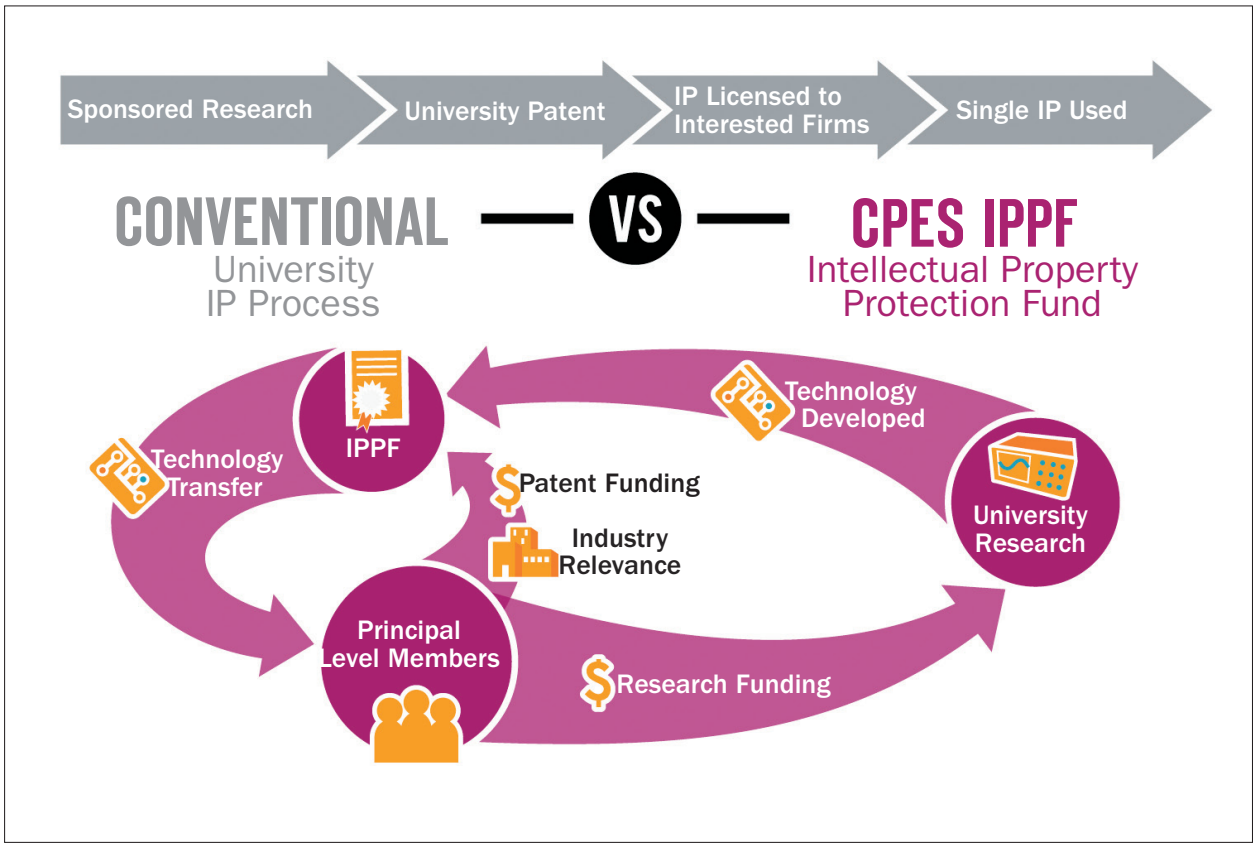
Principal Members (annual contribution - $25,000) - are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. They also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund).

Associate Members (annual contribution - $10,000) - gain the competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges and continuing education to stay updated on new technologies.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires Center Director approval.

INDUSTRY MEMBERSHIP FUNDING GROWTH





Intellectual Property Protection Fund

IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF. Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.

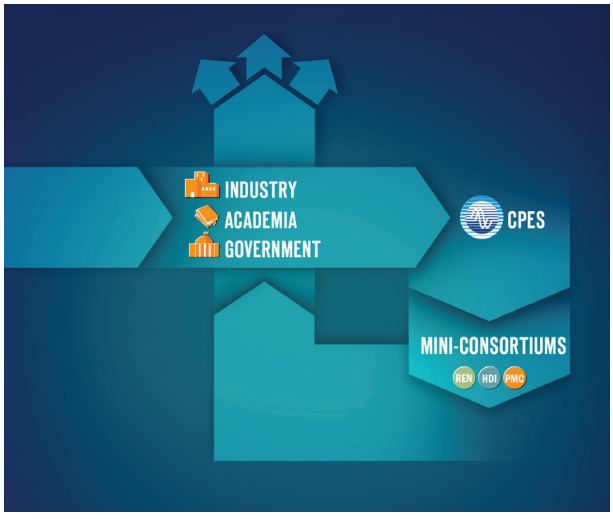
CPES Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contribution of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- PMC (Power Management Consortium)
- HDI (High Density Integration)
- REN (Renewable Energy and Nanogrids)

Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.

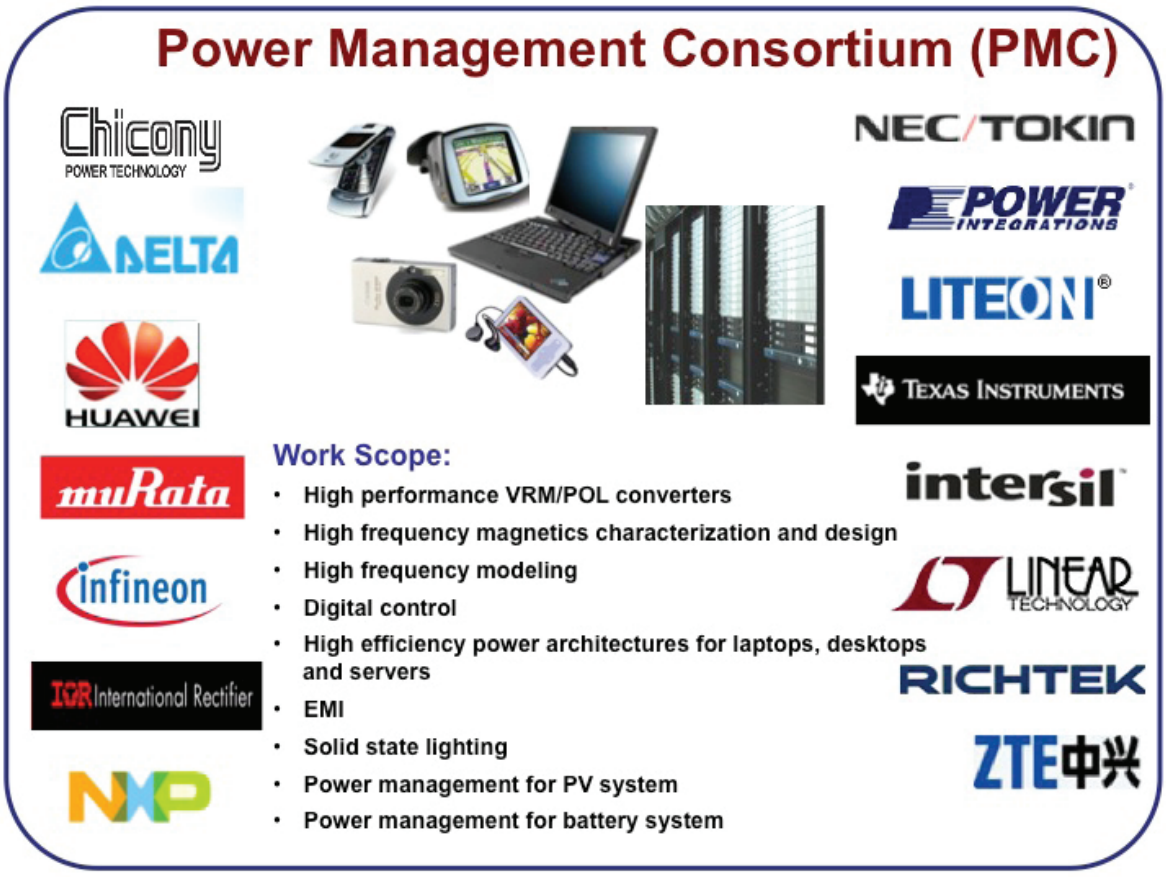


Power Management Consortium (PMC)

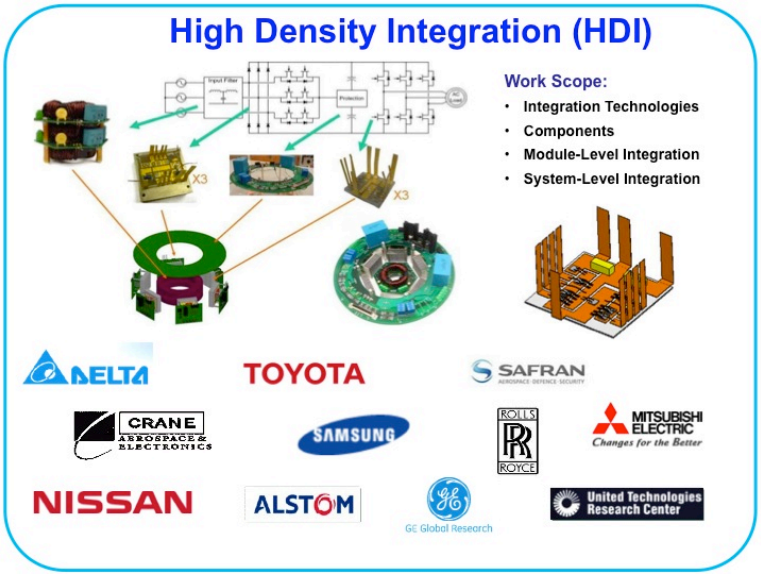
In 1997, at the request of Intel, CPES established a mini-consortium to address the issue of power managemenfor future generations of microprocessors, targeting at sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team has developed a multi-phased voltage regulator module. Instead of paralleling power semiconductor devices in order to meet the current demand and efficiency requirements, the research team has proposed to parallel a number of mini-converters. By paralleling the mini-converters and phase-shifting the clock signal, not only we were able to cancel the significant part of the output current ripple, but also to increase the ripple frequency by N time, where N is the number of channels we parallel. This has resulted in demonstrated improvement, specifically, 4 times improvement in transient response, 10 times reduction in output filter inductors, 6 times reduction in output capacitors, 6 times improvement in power density, and 3 times improvement in profile.

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This particular mode of operation is necessary to conserve energy, as well as to extend the operation time for any battery-operated equipment. The challenge for the voltage regulator module in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as fast as possible to the microprocessor.

Today, every Intel processor is powered by such multi-phased VRMs developed by CPES. CPES researchers are continuing to conduct research in this particular subject by exploring new topologies in power semiconductor devices, magnetics, and integrated packaging concepts in order to improve the transient response and minimize the I2R loss due to continuous reduction in voltage as well as continuous increase in load current. We have been exploring a range of input voltages in VRM technologies, from 12V up to 48V, to accomplish this objective.



Mini-Consortium on High Density Integration (HDI)



Over the past two decades, CPES has secured research funding from major industries, such as GE, Rolls-Royce, Boeing, Alstom, ABB, Toyota, Nissan, Raytheon, and MKS, as well as from government agencies including the NSF, DOE, DARPA, ONR, U.S. Army, and the U.S. Air Force, in research pursuing high-density system design. CPES has developed unique high-temperature packaging technology critical to the future power-electronic industry.

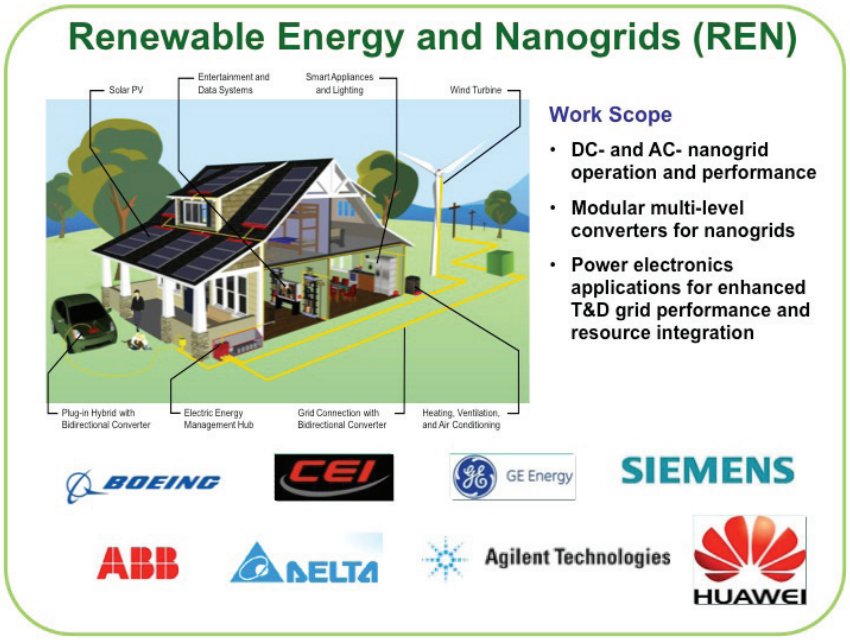
In the proposed mini-consortium, the goal of high power density will be pursued following two coupled paths, both leveraging the availability of wide-bandgap power semiconductor, as well as high-temperature passive components and ancillary functions. The switching frequency will be pushed as high as component technologies, thermal management, and reliability permit. At the same time, the maximum component temperatures will be pushed as high as component technologies, thermal management, and reliability permit.

Mini-Consortium on Renewable Energy and Nanogrids (REN)

Building upon the Center's Sustainable Building Initiative (SBI) sponsored under the NSF ERC Program, with the initial focus on the development and demonstration of advanced power electronics technology for electrical systems in sustainable buildings, CPES will further develop ac and dc-based renewable energy powered system as a testbed, a living lab, for future sustainable building electric power system.

The renewable and alternative energy sources would include primarily photovoltaic solar cells, wind generators, micro-turbines, fuel cells, and energy storage. The testbed will be used as a vehicle to address many of the nanogrid and grid interface related issues, such as dc bus architecture, energy/power management, and various forms of utility interface converters and inverters. The site of the "living lab" will be the home of CPES in Whittemore Hall at Virginia Tech.

The program will concentrate on finding integrative solutions to satisfy the energy, functional, comfort, and zero-CO2 emission goals for building/home environment.

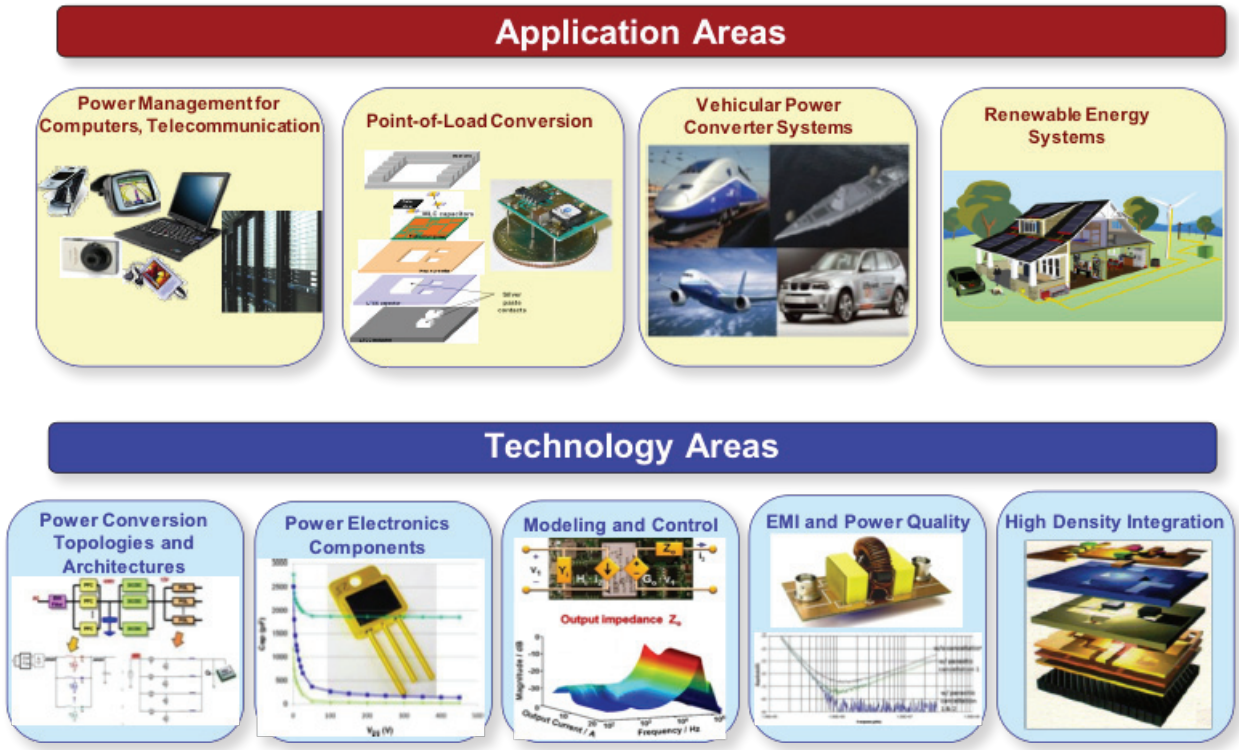


RESEARCH

In its efforts to develop power processing systems to take electricity to the next step, CPES has developed research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; (5) high density integration.

These technology areas target applications that include: (1) Power management for information and communications technology; (2) Point-of-load conversion for power supplies; (3) Vehicular power conversion systems; (4) Renewable energy systems.

In 2013, CPES sponsored research totaled approximately $2 million. The following abstracts provide a quick insight to the current research efforts.



Sponsored Research

Power Supplies On A Chip (PSOC)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology)
Research collaborators: International Rectifier, University of Delaware, Enpirion
Performance Period: September 1, 2010- October 31, 2013

The first phase of the project aims to develop a proof-of-concept prototype power supply on chip (PSOC) using GaN devices operating at 5-lOMHz. The target was to achieve a power density greater than 1000W/in3 with 88% efficiency. The proposed three-dimensional PSOC would be constructed using IR's GaN devices and Si gate driver IC's assembled on top of a 1 mm magnetic substrate using a high frequency soft magnetic material. Such a level of integration has never been attempted with a current greater than 5A. The proposed prototypes will extend the current to 20- 40A at 12V input voltage, targeting such applications as computer, mobile electronics, and telecommunication.

After successful completion of phase 1, a 5MHz, 12V to 1.2V, 20A, two-phase integrated POL converter with GaN transistors and coupled-inductor substrate is demonstrated with power density as high as 1000 W/in^{3,} which is a factor of 10 improvements compared to industry products at the same current level. In phase II, CPES is collaborating with Enpirion and focusing on commericalizing this 3D integrated POL module. We are trying to transfer CPES's technologies, such as inductor substrate and 3 packaging design into Enpirion's products to develop silicon based 1-2MHz, 15-20A, 3D integrated POL module, which still can achieve power density as high as 900W/in^3.

Isolated Converter With Integrated Passives And Low Material Stress

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency-Energy, Agile Delivery of Electrical Power Technology)
Research collaborators: University of Florida, University of Texas - Dallas
Performance Period: September 1, 2010- November 30, 2013

This project will develop a monolithic power converter to be used in efficient power adapters for mobile applications, such as netbooks. The chip converter will include the integration of a transformer, ultra-high-density capacitors, and a nano-magnetic material dispensable with high precision by low-cost inkjet printing. The magnetic structure, with a 3X improvement in energy storage, is introduced to keep the transformer volume at a minimum. The resulting highly efficient (>90%) converters with high power density will reduce the 15 tera watt-hours of energy consumed by notebooks and netbooks annually.

Gallium Nitride Switch Technology for Bi-Directional Battery to Grid Charger Application

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency - Energy, Agile Delivery of Electrical Power Technology)
Sub – Awardee of: HRL
Performance Period: October 1, 2010 – March 31, 2014

The purpose of the project is to develop efficient, high power, and cost effective power converters with application to the automotive sector. More specifically, it will utilize high voltage Gallium Nitride (GaN) on low cost silicon substrate switches operating at megahertz frequencies. GaN semiconductors process electricity faster than the silicon semiconductors used in most conventional EV battery chargers. These high-speed semiconductors can be paired with lighter-weight electrical circuit components, which helps decrease the overall weight of the EV battery charger. The innovative design will result in a battery-to-grid bi-directional charger that enables efficient, cost effective power management focusing on grid-interactive distributed energy systems for the automotive sector.

Dual Bi-Directional Silicon LGBTS Modules Enables Breakthrough PV Inverter Using Current-Modulation Topology

Sponsored by: ARPA-E, SunShot Program
Sub -Awardee of: Ideal Power
Performance Period: January 1, 2012- January 29, 2015

Ideal Power Converters is developing light-weight electronics to connect photovoltaic solar panels to the grid. Their technology explores innovative circuits using revolutionary transistor designs to develop solar panel electronics for commercial-scale buildings that are compact enough to be installed on walls or roof-tops. The project goal is to reduce the weight of these electronics by 98%, reducing the cost of materials, manufacturing, shipping

and installation, and supporting the aggressive cost-reduction goals of the Department of Energy's SunShot Initiative. Virginia Tech's role will be the development of a mechanically balanced dual chip module using proprietary wave joints to enable low inductances, low strain and passive heat extraction via two-sided cooling.

High Density Motor Controller

Sponsored by: The Boeing Company (August 1, 2005 – April 30, 2013)

In this project, a 10 kW high power density three-phase ac-dc-ac converter together with a high density PCB axial flux motor were developed and electrically evaluated. The converter consists of a Vienna-type rectifier front end and a two-level voltage source inverter (VSI). In order to reduce the switching loss and achieve a high operating junction temperature, SiC JFETs and SiC Schottky diodes are utilized. The design considerations for the phase-leg units, the gate driver, the input filter, the system protection and motor operation are investigated in detail. Experiments are carried out under different conditions, and the results verify the feasibility of the full system.

A second phase of the project has devoted its effort to the weight minimization of the inverter and EMI filters required by 50 kW motor controllers. To this end parallel converter configurations have been explored using symmetric and asymmetric interleaving PWM techniques, which have achieved harmonic cancellation at both the AC and DC terminals of power converters with a great impact on the EMI filter weight minimization. Additionally, multi-level power converter topologies have been investigated seeking further reduction of EMI emissions and overall higher power conversion efficiency.

System Stability And Analysis

Sponsored by: The Boeing Company (October 22, 2004 – December 31, 2013)

CPES has developed design criteria and analysis tools for integrating ac and dc distributed power electronics conversion systems for the stable, safe and reliable operation of future aircraft electrical power systems. These power electronics systems combine numerous and different types of power converters, which when interconnected can easily interact with each other if no precautionary measures are taken. These interactions can easily lead to instabilities and system faults. Therefore, it is important to study the operation of the system carefully as part of its design process. As a demonstration testbed, CPES modeled a large electrical distribution system where it addressed the actual model implementation of the several components considered using the detailed switching models. CPES also evaluated the testbed correct operation by means of Lyapunov's indirect method—local assessment of large signal stability, studying as well the effect of faults in the system providing insight into the choice of models for the respective studies conducted. In addition, CPES developed ac-system-small-signal-stability criteria. For the verification of these stability analyses, CPES has developed an AC impedance tester to be capable of measuring the synchronous d-q frame impedance of ac networks and power converters for later use in stability studies. After delivering a first unit, CPES has developed an upgraded impedance tester unit capable of measuring in both shunt and series connection modes for improved accuracy.

In order to facilitate complex system-level simulation and analysis, CPES is developing enhanced average models that should be capable of capturing not just the fundamental frequency but also the mid-frequency range (up to half of switching frequency) large-signal behavior of power converters. The enhanced converter models will enable the simulation and study of phenomena otherwise neglected by conventional average models, including distortion induced by dead-time, digital sampling, and other controller and power stage non-linearities.

To this end CPES has adopted an advanced modeling framework, namely validation, verification and uncertainty quantification (VV&UQ), which will empower the simulations conducted to fully estimate the level of uncertainty in the simulation predictions by taking into consideration all random (aleatory) uncertainty and lack-of-knowledge (epistemic) uncertainty in model inputs. In addition, it incorporates uncertainty due to the mathematical form of the model (relative to actual test data) and it provides a procedure for quantifying uncertainty due to numerical errors.

Optimization of AC/AC Motor Controller Power Quality and EMI Filter Topology

Sponsored by: United Technologies Aerospace Systems
(January 1, 2012- December 31, 2013)

The object of this work is the optimization of the combined power quality and EMI filters for motor controller comprising input power circuits fed by variable frequency power bus, and output power circuits that drive variable speed electric motors. The effect of the thermal and electrical characteristics associated with new materials with particular application on the EMI and PQ filters will be researched.

The next phase of this work will look at optimization of one or more small local converters, each built on a PC card addressing the combined power quality, EMI and thermal requirements and fed by variable frequency AC or higher voltage DC power bus and output power circuits that provide regulated 28 V DC power. The effect of the thermal and electrical characteristics associated with a number of power topologies and the trade off in their performance in terms of weight, size and perceived reliability will be investigated.

High-Temperature Packaging of Planar Power Modules by Low-Temperature Sintering of Nanoscale Silver Paste

Sponsored by: NBE Technologies/DOE-SBIR (August 12, 2009 -August 31, 2013)

In present electric vehicles (PHEV/HEV/EV), an extra cooling loop is needed to lower the power-electronics coolant temperature below about 65° C from the radiator coolant temperature of 105° C. One way to reduce the cost of future EVs is to eliminate the extra cooling loop by developing reliable high-temperature power inverter modules that are sufficiently cooled by the radiator coolant. This calls for the development of power packaging technologies that can enable silicon and/or SiC power devices working at junction temperature in excess of 175°C. In the current phase of our power packaging research effort, we have focused on replacing the solder-reflow technique for die-attaching power chips by an emerging low-temperature joining technology (LTJT) which involves low-temperature sintering of silver powders. To reduce the process complexity of the conventional LTJT arising from the need of high pressure (30 to 40 MPa or 300 to 400 Kg-force per cm2, a nanosilver paste material was used to lower the die attach temperature below 270°C with zero or less than 5 MPa pressure. This simplified LTJT is less likely to damage the chips and allows us to implement a planar packaging scheme for interconnecting both sides of the power devices without using wire bonds. The planar power modules have low parasitic inductances thus less ringing noises from the device-switching action and can be cooled from both sides of the devices for improved thermal management. The electrical performance of the planar power module was tested and the results show that it can work properly under 175° C junction temperature.

A Study of Multi-Channel Constant Current Driver for Multiple Solid-State Light Sources on DC Distribution System

Sponsored by: Panasonic Electric Works (April 1, 2011 – March 31, 2012)

Recently, many applications such as display backlighting, indoor lighting and street lighting, all prefer multi-channel LED drivers. In this project, a design methodology for MC3 LLC LED driver has been developed. The frequency-controlled analog dimming solution has been verified by both simulation and experimentation. The circuit behavior under open and short failure is investigated as well. Moreover, in order to achieve lower dimming ratio and keep higher efficiency, the hybrid control approach combining with asymmetrical PWM control and frequency control is proposed.

High-Temperature, High Power Density Power Converter for Embedded Generators

Sponsored by: Rolls Royce (January 1, 2011 – June 30, 2013)

The conducting project is to evaluate and demonstrate feasibility of developing a complete high-power, high-temperature, high-power-density bidirectional three-phase ac-dc power converter unit required to operate embedded generators in the temperature range of 200-250° C. In the Phase II of this program, the focus is on the development and validation of the critical system components at the rated power and temperature, and on the functional integration of the equivalent low-temperature subsystems at reduced power level.

Based on the work conduced from Phase I and Phase II, the phase III of this project will concentrate on the final thermo-mechanical design, integration of all the system components and subsystems, and on testing, characterization, evaluation, and demonstration of the complete system at full power and high ambient temperature.

Study and Development of an AC/DC Impedance Tester for Medium Voltage High Power Systems

Sponsored by: Newport News Shipbuilding–Huntington Ingalls (July 1, 2009 - April 30, 2012)

The objective is to identify and/or develop a feasible impedance measurement technique that be used for high power and medium voltage DC and AC power systems, and to develop an AC impedance tester that can be used to test impedances at AC and DC interfaces for systems up to 13.8 kV and 36 MW.

Terminal Modeling of Noise Source in Switching Power Converters

Sponsored by: Hispano Suiza, SAFRAN (October 1, 2010 -September 30, 2014)

The main objective of this research is to develop terminal models of noise sources in switching converters for easy EMI analysis. These models must be scalable for different load and source conditions. Conventional methods of EMI modeling use physics based models of semi-conductor devices and EMI coupling paths. Due to the complex nature of these models the simulations often fail to converge or lead to unusable results.

In its latest phase this project is exploring the use of terminal models for the development of EMI filter design procedure. Its main focus is the design of filters for parallel inverters using interleaved PWM techniques.

The efforts in this research are aimed at simplifying the simulations by using Thevenin or Norton models of these noise cells. Here "noise-cell" may refer to both device level (single device or a Phase-leg) and converter level abstraction. The final goal is to make a terminal EMI model of a 3-phase voltage source inverter (VSI) to estimate EMI in power train set-up as shown above.

With the success of the generalized terminal modeling technique, another direction of research pursues estimating the worst case EMI noise on a debus that feeds several converters in parallel. In previous research, the generalized modeling technique was shown to accurately model switching power converters from the dc input side. The aim is to estimate conducted EMI noise on dc bus with terminal models of several converters in parallel. The converters may switch in a synchronized or in unsynchronized fashion. The technique should be able to estimate the worst case noise on dc bus for un-synchronized switching of several converters.

Low-Loss 1 MHz Inductor

Sponsored by: Transphorm Inc./ ARPA-E (April 1, 2012 – December 31, 2012)

In the megahertz frequency range, the cores of high-power inductors are usually made of metal powder or ferrites, each generating its own loss mechanism. Metal powder exhibits significantly higher core loss than ferrites, whereas ferrites require gaps which generate excessive loss in the winding. In this project, a hybrid approach is taken to realize an inductor with low core loss and low winding loss. The approach also takes advantage of a new metal powder with low permeability and low loss recently developed at CPES.

Multi-Phase Auto-Tuning Self Compensating Power Supply Control Systems

Sponsored by: Energy Research Corporation
(September 1, 2012 – August 31, 2013)

The multi-phase voltage regulator (VR) has been widely used to power microprocessors. For multi-phase VR, a constant output impedance design is usually used to reduce the output capacitor bank. Conventionally, a fixed analog compensation network is chosen to compensate the worst-case component (such as inductor and output capacitor) variations on the plant, which will limit the converter bandwidth. Furthermore, since a microprocessor runs into sleep mode very frequently, several green-mode functions have been used to improve the light load efficiency such as phase shedding, discontinuous mode operation, and frequency changes. However, the plant characteristic will also change with these techniques under sleep mode, and will influence the stability and transient response during mode transitions. Therefore, it is very challenging and attractive to investigate multi-phase self-tuning power supply control systems which can compensate the component variation and mode transition without suffering from the worst-case design compromises. In this project, a self-tuning power supply control system will be developed to self-identify the plant characteristic change from component variation and operating mode transitions, and then adaptively adjust the compensation parameters to maintain stability and system performance. Therefore, external compensation circuitry and the output capacitor bank can be reduced to reduce total cost.

Constant-Flux Magnetics for Power Conversion

Sponsored by: National Science Foundation
(November 15, 2012 – October 31, 2015)

At least 30% of the volume in commercial inductors store no or negligible energy. The "constant-flux" concept improves energy density by filling the available volume with as much magnetic (core) materials as practically feasible, then dispersing the windings to shape the distribution of magnetic flux, e.g., to distribute magnetic flux uniformly. In this project, guiding principles will be developed from the structural and field standpoints to realize the constant-flux concept. Performance metrics, such as inductances, capacitances, and quality factor will be modeled, quantified, and compared with the corresponding benchmarks.

Linear Actuator with Permanent Magnets

Sponsored by: GE Appliances and Light (GEAL)
(October 1, 2012 – September 30, 2013)

In this project, CPES will work to improve the design procedure and performance of GEAL's Linear Actuator with Permanent Magnets (LAPM) by determining the proper materials to use, validating flux models, predicting force vs. position, and making an improved LAPM design to meet a cost function.

Impedance Measurement Unit (IMU) for 4160V AC Networks

Sponsored by: Office of Naval Research (November 1, 2012 – October 31, 2013)

In this project, CPES will design, construct, integrate and test a medium voltage (MV) impedance measurement unit (IMU) to assess the stability of electric power systems and components for future Navy electric ships. The IMU will be rated at 4160 V AC, 100 A, and use silicon carbide (SiC) semiconductor devices to demonstrate their operation at higher voltages and power level, as well as their exceedingly faster switching speeds enabling the IMU to characterize impedances from DC up to 1kHz. At the intermediate scale, the IMU will be capable of injecting 5 % system current and 5 % system voltage, performing all the data acquisition and necessary post processing. CPES will investigate the use of modular power converter topologies suitable for scaling the IMU towards higher MV networks, as well as single-phase injector solutions capable of measuring three-phase synchronous d-q frame impedances in an effort to reduce the overall complexity of the IMU.

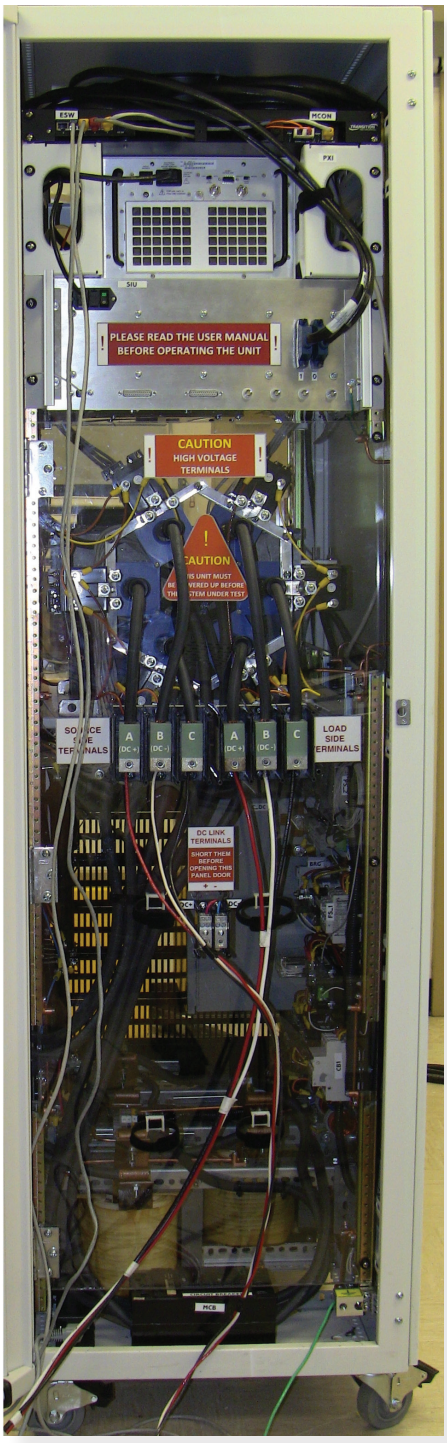
The Next Generation Power Converter: Applications for Enhanced T&D Grid Performance and Resource Integration

Sponsored by: URS Energy and Construction/National Energy Technology Laboratory (July 1, 2012 November 14, 2013)

As a member of the NETL-RUA Grid Technologies Collaborative (GTC) group, CPES has been putting efforts on researching power electronics converter technology that can enable major improvements in performance, reliability, and maximal utilization of the renewable energy sources and energy storage systems that can be integrated into the electric power system. The main goal of the work in the first phase of the project was to explore functionality and performance of the bidirectional three-phase ac/dc (micro)grid-interface converter for the medium-voltage high-power applications (through functional average models), together with developing some specifications for the converter design that allow an on-demand active and reactive power delivery, as well as P-f control of the grid.

The second phase of the project will focus on analyzing the low-frequency dynamic interactions caused by power converters and synchronous generators, as well as exploring relationships and defining the physical/mathematical equivalency between them using both, analytical approach and simulation (average) models.

Front view



Back view

Impedance Measurement Unit (IMU)

INTELLECTUAL PROPERTY

U.S. Patents Awarded

11-049
High Frequency Loss Measurement Apparatus and Methods for Inductors and Transformers
Ming Xu, Fred C. Lee
U.S. PATENT: 2013/0049744
Issued: February 28, 2013

08-036
Switching Capacitor-PWM Power Converter
Ming Xu, Ke Jin, Fred C. Lee
U.S. PATENT: 8,331,110
Issued: December 11, 2012

Invention Disclosures

13-085
1/4/13
V^2 Control with Capacitor Current Ramp Compensation using Self-Calibrated Lossless Capacitor Current Sensing
Yingyi Yan, Pei-Hsin Liu, Fred C. Lee

13-046
10/24/12
Multi-Channel Constant Current LED Driver with Coupled Inductor [CIP: 10-095]
Weiyi Feng, Fred C. Lee

13-032
9/12/12
Transformer Shielding Technique for Common-Mode Noise Reduction in Isolated Converters
Yuchen Yang, Daocheng Huang, Qiang Li, Fred C. Lee

13-029
9/11/12
Packaging Method for Semiconductor Dice with Multiple Contacts on Both Front and Back Sides

13-025
8/27/12
Islanding Detection Using Phase-Locked-Loop Small-Signal Instability for Three-Phase Power Inverters
Dong Dong, Dushan Boroyevich, Paolo Mattavelli, Bo Wen

13-014
8/15/12
I^2 Average Current Mode Control for Switching Converters
Yingyi Yan, Fred C. Lee, Paolo Mattavelli

13-008
7/20/12
STability Analysis SUite (STASU) for DC and Three-Phase AC Electrical Power Systems
Sheau-Wei Fu, Kamiar Karimi, Marko Jaksic, Bo Zhou, Bo Wen, Paolo Mattavelli, Dushan Boroyevich

12-152
5/18/12
Optimal Trajectory Control of LLC Resonant Converter for LED PWM
Weiyi Feng, Fred C. Lee, Shu Ji

12-131
5/18/12
Optimal Trajectory Control of LLC Resonant Converter for Soft Start-Up
Weiyi Feng, Fred C. Lee

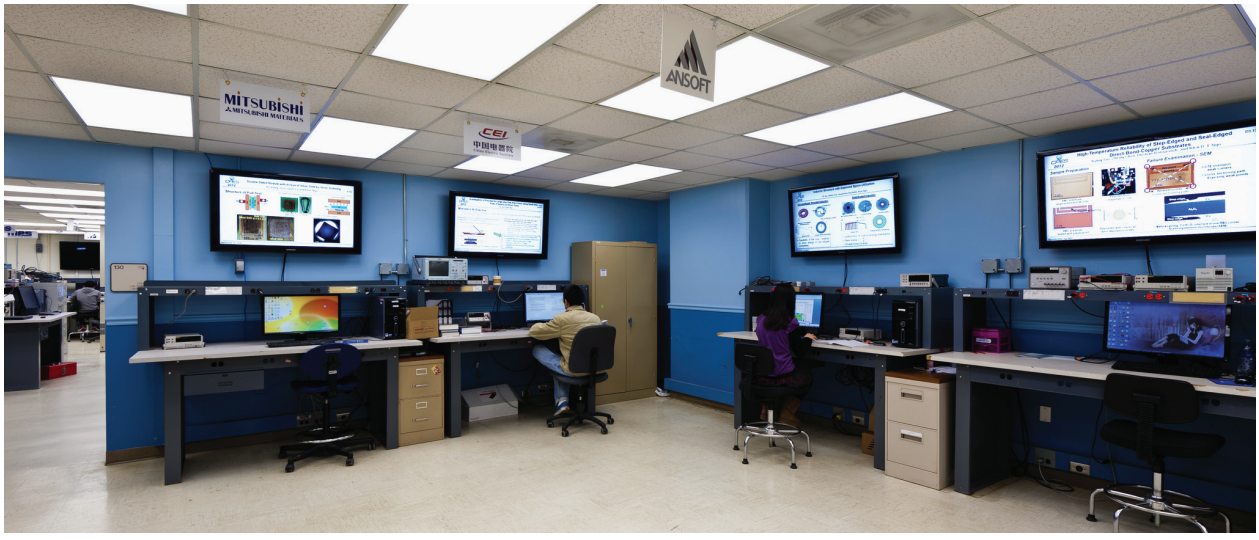
12-130
5/18/12
External Ramp Auto-Tuning for Current Mode Control of Switching Converter
Pei-Hsin Liu, Fred C. Lee, Yingyi Yan, Paolo Mattavelli

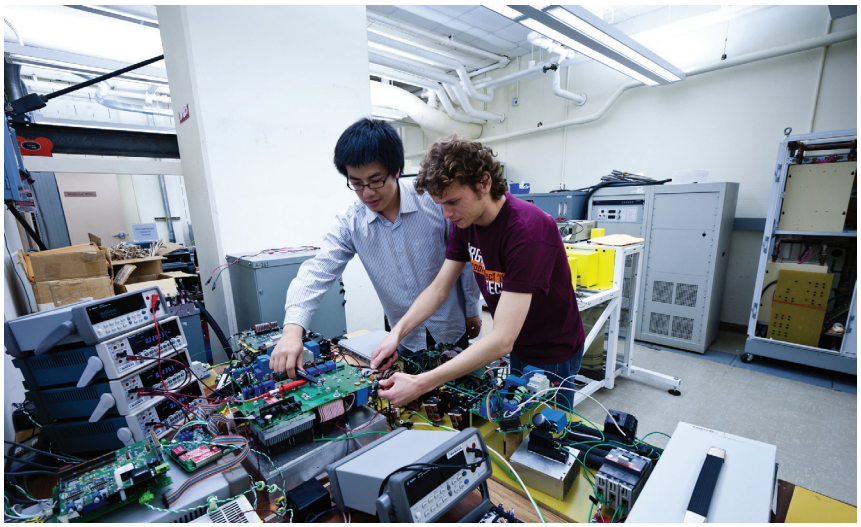
12-122
4/23/12
Common input voltage control and output power maximum power point tracking (MPPT) for Sub-panel converters with series outputs
Xinke Wu, Zijian Wang, Fred C. Lee, Feng Wang

VIRGINIA TECH FACILITIES

Introduction

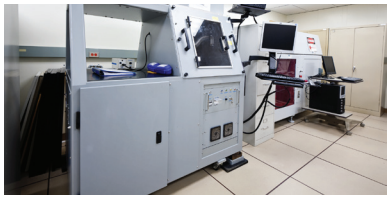
The Center headquarters is located at Virginia Tech, occupying office and lab facilities encompassing more than 19,000 sq.ft. of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab and computer lab. In addition to the headquarters labs and offices, a research library and a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators is maintained. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.





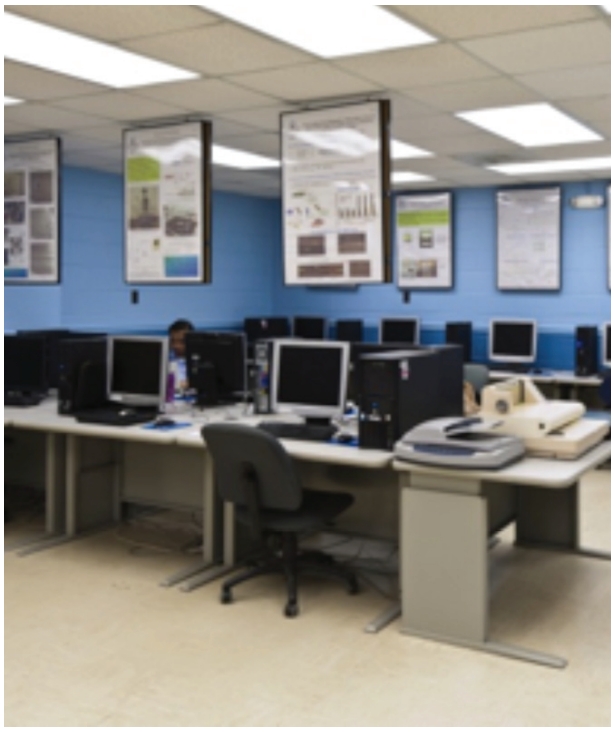
Electrical Research Laboratory

The electrical research laboratory is equipped with state-of-the-art power testing equipment, dynamometers, prototype PWB manufacturing equipment, an EMI chamber, a clean room, a mechanical shop. The Power Electronics Research Lab is equipped with state-of-the-art tools and instrumentation necessary for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6 kV, 1 MW. Each student bench is equipped with Dell Studio XPS computers with an i7 core processor and multiple GBs of RAM for running simulations. Standard instrumentation is comprised of GHz oscilloscopes, multi-channel function generators, electronic loads, network, spectrum, impedance, logic and power analyzers, thermal sensors and AC/DC bench supplies of all sizes. Specialized test room equipment includes: thermal imaging equipment, thermal cycling chambers, Hi-Pot tester, 3-D magnetic field scanner, EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, programmable and variable loads, and liquid cooled heat-exchanger.



Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculties, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab is established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide the state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 clean room space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. The IP lab also has the ability to mount bare dies and SMT components using high precision pick-n-place machine, solder reflow belt furnace, and convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants an automated precision dispensing system and a spin coater have been added in the lab. In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The Component- and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Low and high power curve tracers, impedance analyzers, and precision multimeters can be used for electrical property measurements. Thermal performance evaluation can be made by the setup of thermocouples, optic-fiber sensors, IR imaging, and thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and the ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.



Computer Lab

The Computer Lab supports all major software used in power electronics analysis and design including: SPICE, Saber, I-DEAS, Math Products – Matlab and Mathcad, Ansoft Products- Maxwell 2-D and 3-D finite-element analyzers,ePhysics, and Q3D, Mentor Graphics and Cadence circuit simulation software, SIMPLIS, PLECS, FLOTHERM circuit thermal analyzer software, and Inventor Professional.

High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost sharing of more than $250K for renovations, the electrical research lab area at VT has been renovated and upfit to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160 V level. The unique installation distinguishes VT as one of a few select universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

PEOPLE

STUDENTS

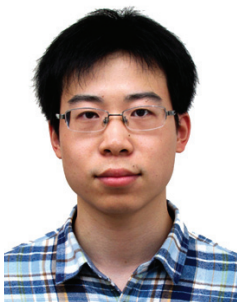

Ken Atavatkul


Syed Bari

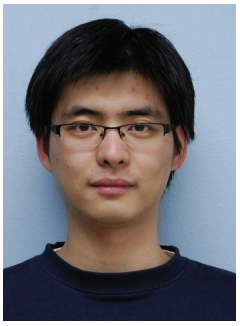

David Berry


Hemant Bishnoi

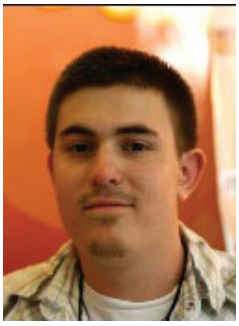

Zhongsheng Cao


Fang Chen


Xuebing Chen

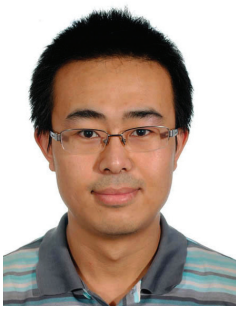

Zheng Chen (Henry)

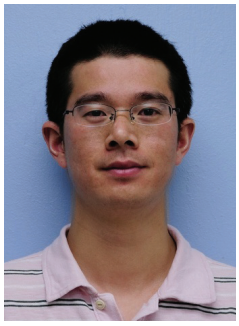

Han Cui


Nicholas Dahlin


Milisav Danilovic


Christina DiMarino


Chao Fei


Weiyi Feng


Kumar Gandharva


Dongbin Hou


Daocheng Huang


Xiucheng Huang


Marko Jaksic


Li Jiang


Yang Jiao

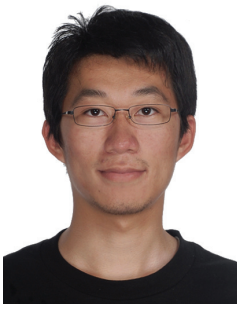

Mudassar Khatib


Woochan Kim


Chi Li

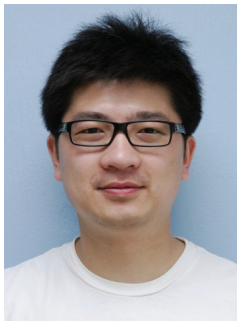

Pei-Hsin Liu

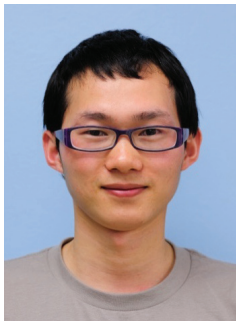

Zhengyang Liu


Ming Lu


Yincan Mao

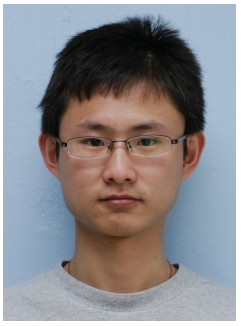

Niloofar Rashidi Mehravadi

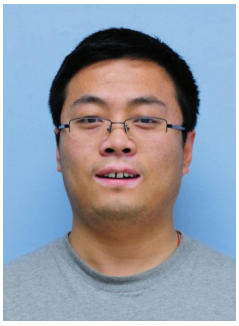

Yipeng Su


Shuilin Tian


Jun Wang


Qiong Wang

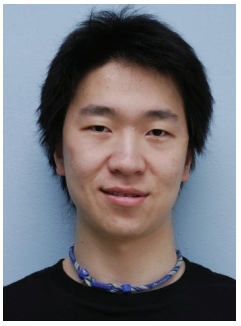

Bo Wen

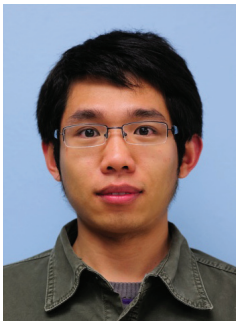

Lingxiao Xue


Yuchen Yang


Yiying Yao

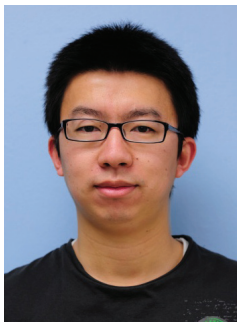

Wei Zhang


Xuning Zhang


Zhemin Zhang (Jimmy)

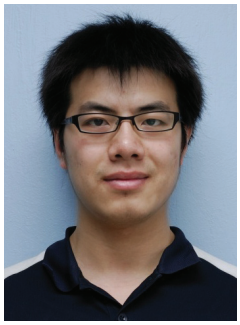
PEOPLE

STUDENTS



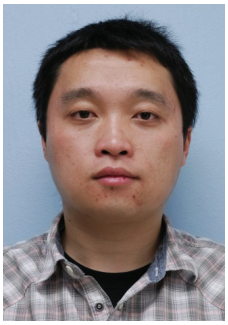
Hanguang Zheng (Jason)

GRADUATES



Dong Dong

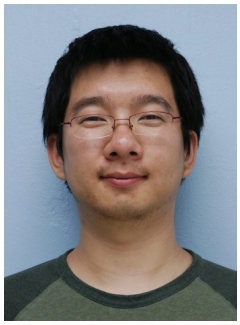
Shu (Alex) Ji



Li Jiang

Mingkai Mu

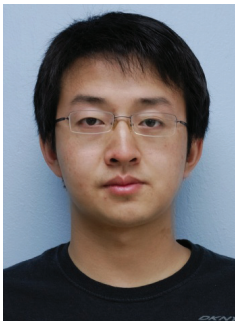
David Reusch



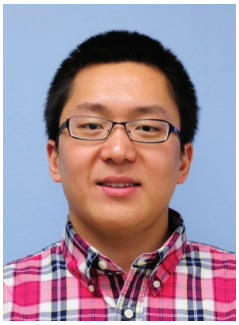
Zhiyu Shen

Tao Tao

Yin Wang



Ruxi Wang



Di Xu

Yingyi Yan

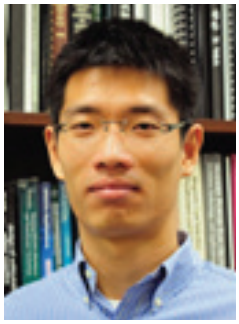
Bo Zhou

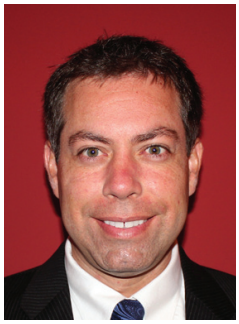
FACULTY


Fred C. Lee


Dushan Boroyevich


Khai Ngo


Qiang Li


Rolando Burgos

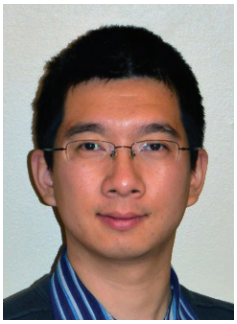
ADJUNCT FACULTY

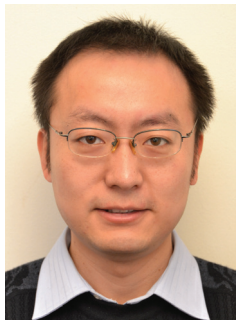

Paolo Mattavelli

AFFILIATE FACULTY


Guo-Quan Lu

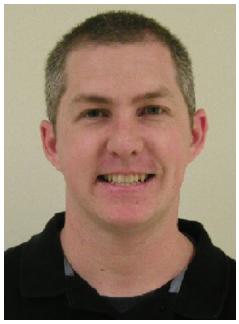
RESEARCH FACULTY


Zhiyu Shen


Minkar Mu

STAFF

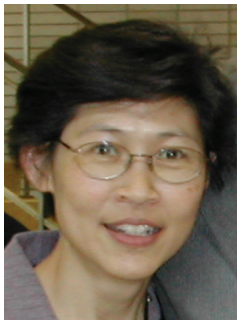

Igor Cvetkovic


David Gilham


Marianne Hawthorne


Linda Long

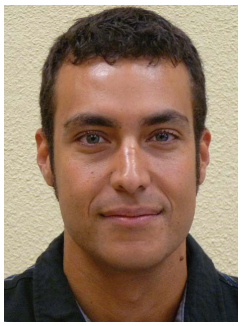

Trish Rose


Teresa Shaw


Wenli Zhang

PEOPLE

VISITING SCHOLARS


Daniel Diaz


Fabien Dubois


Ewan Farr


Genevieve Frantz

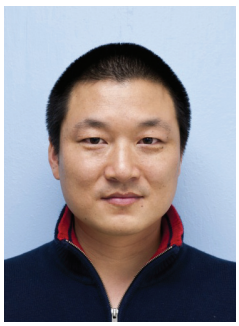

Nico Hensgens


Jani Hiltunen


Chun-Shih (Lion) Huang


Kyozo Kanamoto

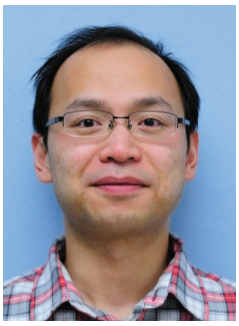

Konjedic Tine

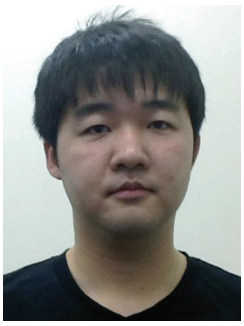

Weijun Lei


Zeng Li


Sizhao Lu


Oscar Lucia


Fang Luo


Wenlong Ming


Hamed Nademi


Milijana Odavic


David Reusch


Mingsong Shao

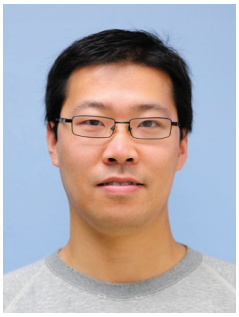

Yamagami Shigeharu

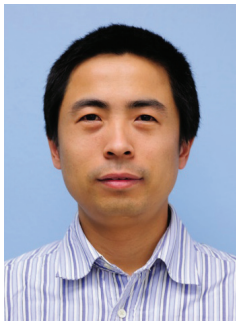

Sharmil Sumsurooah


Tatsuhiro Suzuki


Virgilio Valdivia


Montie Vitorino


Feng Wang


Xinke Wu


Mingyu Xue


Qing-Chang Zhong


Xiwei Zhou

PUBLICATIONS

Transactions Papers

Modes of Operation and System-Level Control of Single-Phase Bidirectional PWM Converter for Microgrid Systems
Dong Dong, Tim Thacker, Igor Cvetkovic, Rolando Burgos, Dushan Boroyevich, Fred Wang, Glenn Skutt
IEEE Transactions on Smart Grid, March 2012, Volume 3, No. 1, pp. 93-104

Total Flux Minimization Control for Integrated Inter-Phase Inductors in Paralleled, Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation
Di Zhang, Fred Wang, Rolando Burgos, Dushan Boroyevich
IEEE Transactions on Power Electronics, April 2012, Volume 27, No. 4, pp. 1679-1688

Reliability-Oriented Design of Three-Phase Power Converters for Aircraft Applications
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Leakage Current Reduction in Single-Phase Bi-Directional AC-DC Full-Bridge Inverter
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A Testbed for Experimental Validation of a Low-Voltage DC Nanogrid for Buildings
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Impact of Interleaving on Input Passive Components of Paralleled DC/DC Converters for High Power PV Applications
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Performance Evaluation of SiC Power MOSFETs for High-Temperature Applications
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Analysis and Design of Average Current Mode Control Using Describing Function-Based Equivalent Circuit Model
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Small-signal Laplace-domain Model for Digital Predictive Current Mode Controls
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High Frequency High Power Density 3D Integrated GaN Based Point of Load Module
Shu Ji, David Reusch, Fred C. Lee
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Optimization of a High Density Gallium Nitride Based Non-Isolated Point of Load Module
David Reusch, Fred Lee, David Gilham and Yipeng Su
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High Frequency Isolated Bus Converter with Gallium Nitride Transistors and Integrated Transformer
David Reusch and Fred Lee
2012 IEEE Energy Conversion Congress and Exposition (ECCE), September 15-20, 2012, Raleigh, NC

Digital V2 Control with Fast-Acting Capacitor Current Estimator
Pei-Hsin Liu, Yingyi Yan, Paolo Mattavelli, Fred C. Lee
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EMI Filter Design Considering In-Circuit Impedance Mismatching
Fang Luo, Dushan Boroyevich, Paolo Mattavelli
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Bo Wen, Dushan Boroyevich, Paolo Mattavelli, Zhiyu Shen, Rolando Burgos
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Dong Dong, Dushan Boroyevich, Paolo Mattavelli, Bo Wen, Yaosuo Xue
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Three-Level Driving Method for GaN Power Transistor in Synchronous Buck Conver
Xiaoyong Ren, David Reusch, Shu Ji, Zhiliang Zhang, Mingkai Mu, Fred C. Lee
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Theses & Dissertations

High Frequency, High Power Density Integrated Point of Load and Bus Converters
David Reusch
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Small-signal Analysis and Design of Constant-ontime V2 Control for Ceramic Caps
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AC-DC Bus Interface Bi-Directional Converters in Renewable Energy Systems
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Montie Vitorino
Dissertation, August 2012

Self-Oscillating Unified Linearizing Modulator
Yin Wang
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Integrated Current Sensor Using Giant Magneto Resistive (GMR) for Planar Power Module
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Online Measurement of Three-phase AC Power System Impedance in Synchronous Coordinates
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Loss Analysis of 600V Gallium Nitride HEMT in Cascode Structure with Simulation Model

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EMI Filter Design and Optimization for Both AC and DC Side in a DC-fed Motor Drive System

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Impact and Compensation of Dead Time on Common Mode Elimination Modulation for Neutral-Point-Clamped Three-Phase Inverters

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Low Temperature Joining Technique of Die-attachment by Silver Sintering

Fabrication of a Double-side Cooled, High Temperature Power Module with Sintered Nanosilver Interconnect for Automotive Applications

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Physics-Based Analytical Model for High-Voltage Bidirectional GaN Transistor Using Lateral GaN Power HEMT

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Monolithic Optoelectronic Integration of GaN High-Voltage Power FETs and LEDs with a Selective Epi Removal Process

Investigation of Pyroelectric Polarization Effect On GaN MOS Capacitors and Field-Effect Transistors

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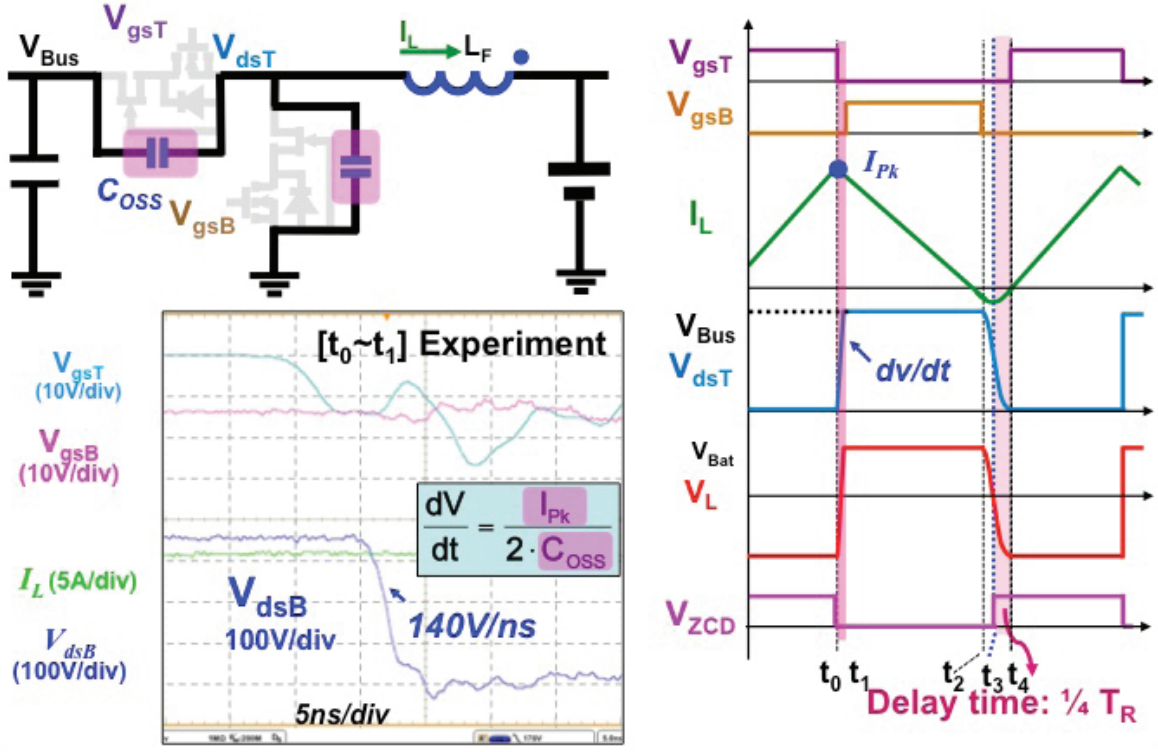
Avalanche Breakdown Design Parameters in GaN

See detailed Research Nuggets, pages 32-106

Research Nuggets

Design Considerations for High Frequency Battery Charger with GaN Device

The overall performance of 600V GaN device, including a low RDS(on) and a small parasitic capacitance (CGD, CDS, CGS), make it very attractive for onboard bidirectional battery charger/discharger applications which require high power density and system efficiency to boost the battery performance and improve fuel economy. Preliminary test results demonstrate >98% efficiency over a wide load range with a 500 kHz, 8.4kW bidirectional buck-boost converter. On the other hand, small parasitic capacitance allows a GaN device to switch very fast and introduces a high di/dt (≈10A/ns) and dV/dt (>100V/ns), which is 5~8 times higher than that of state-of-the-art MOSFET device. These fast transient will falsely trigger gate drive through either a typical low-transient-immunity high side gate driver or a common source inductance, causing shoot through for the GaN-based bridge configuration. Therefore, typical design guidelines and device selection would not satisfy these harsh switch environments and most commercial parts fail under testing. This presentation will first investigate the above design challenges for a gate driver and system reliability of GaN based battery charger, and then introduce several possible solutions.



Evaluation and Application of 600V GaN HEMT in Cascode Structure

Gallium nitride high electron mobility transistor (GaN HEMT) has matured dramatically over the last few years. More and more devices have been manufactured and fielded in applications ranging from a low power voltage regulator to high power infrastructure base-stations. Compared to the state-of-the-art silicon MOSFET, GaN HEMT has a much better figure of merit and has the potential for high frequency application. In general, a 600V GaN HEMT is intrinsically normally-on device. To easily apply the depletion mode GaN HEMT in the circuit design, a low voltage silicon MOSFET is in series to drive the GaN HEMT, which is well known as cascode structure shown in Fig. 1. This paper studies the characteristics and operation principles of a 600V cascode GaN HEMT. Evaluations of the GaN HEMT performance based on a Buck converter under hard-switching and soft-switching conditions are presented. The key converter parameters are listed in table I. Experimental results illustrate that the GaN HEMT is superior to the silicon MOSFET but still needs soft-switching in high frequency operation due to considerable package and layout parasitic inductors and capacitors. The detailed loss breakdown is shown in Fig. 2. Then GaN HEMT is applied to a unregulated LLC converter with parameters listed in table II. Comparison of the experimental results with the state of art silicon MOSFET is shown in Fig. 3 to validate the advantages of GaN HEMT.

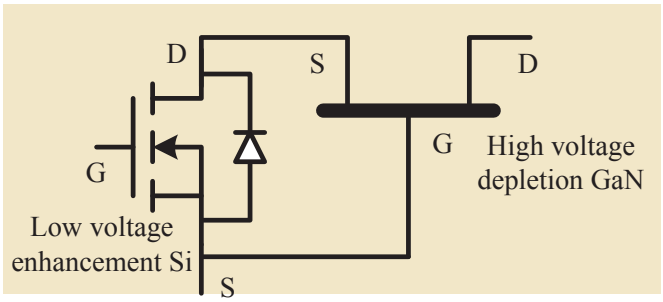


Fig. 1. Cascode structure of 600V normally-on GaN HEMT with low voltage silicon MOSFET

TABLE I Parameters of Buck Converter

Parameters	Value
Input voltage	380V
Output voltage	200V
Maximum output current	6A
Inductor current ripple	3A
Switching frequency	500k
Inductor core material	3F35

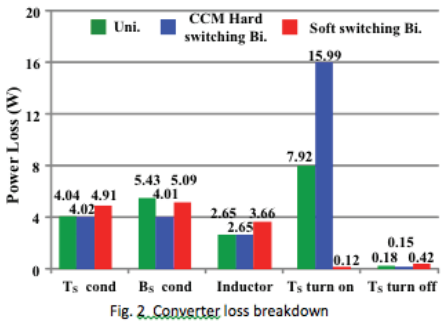


Fig. 2 Converter loss breakdown

Fig. 2. Converter loss breakdown

TABLE II Parameters of LLC Converter

Parameters	Value
Input voltage	400V
Output voltage	12V
Maximum output current	25A
Switching frequency	1MHz
core material	N49

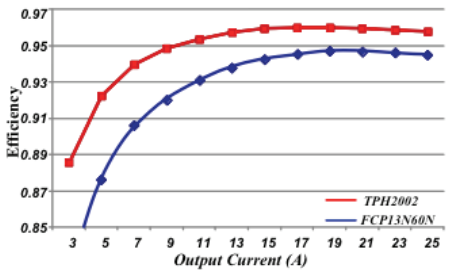


Fig. 3 Efficiency comparison between cascode GaN HEMT and state of art silicon MOSFET in 1MHz LLC converter

Fig. 3. Efficiency comparison between cascode GaN HEMT and state of the art silicon MOSFET in 1MHz LLC converter

Loss Analysis of 600V Gallium Nitride HEMT in Cascode Structure with Simulation Model

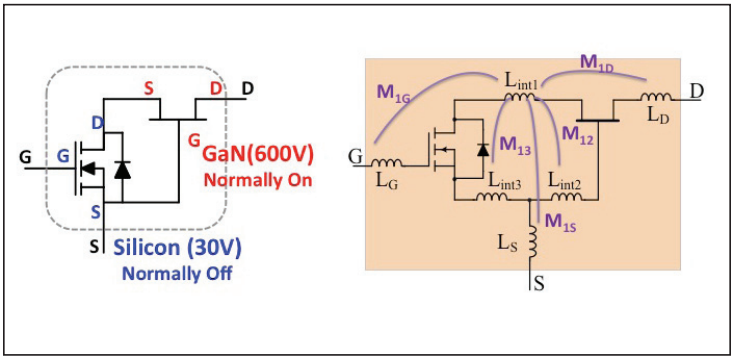


Fig. 1. GaN HEMT cascode structure and package parasitic inductance

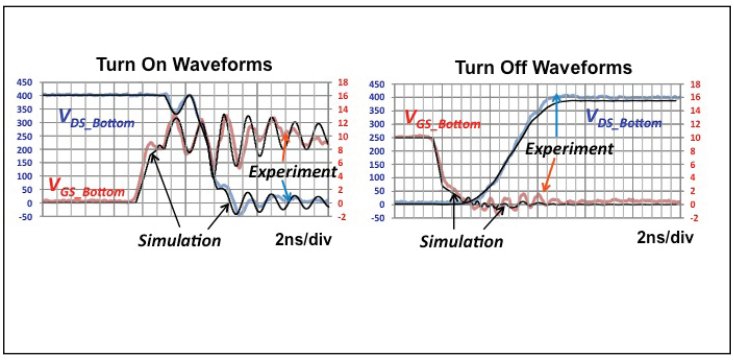


Fig. 2. GaN HEMT switching waveforms matching between simulation and experiment

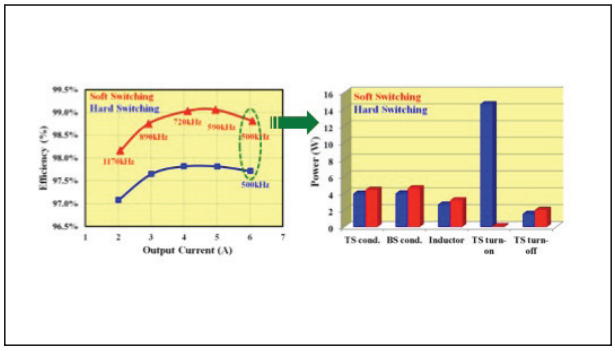


Fig. 3. Buck converter efficiency and loss breakdown at Vin=380V, Vout=200V condition

The emerging Gallium Nitride (GaN) high electron mobility transistor (HEMT) is considered as a promising candidate for future power conversion technology due to its much better figure of merit when compared to the state-of-the-art silicon MOSFET. So far in high voltage range, the GaN HEMT in cascode structure (Fig. 1) is widely used. In order to better evaluate the characteristics of the 600V GaN HEMT in cascode structure, a good behavior level simulation model is in need. This paper presents the development of simulation model for the 600V cascode GaN HEMT. A method is proposed to accurately extract the device package parasitic inductance, which is of vital importance to better predict the high frequency performance of the device. The accuracy of the simulation model is verified by the experiment. The simulation results match well with the experiment in both switching waveforms (Fig. 2) and switching loss. Based on the simu-lation model, a detailed Buck converter loss breakdown (Fig. 3) is made, which indicates that the switching loss is dominant in hard switching conditions; and soft switching is still critical to achieve the high frequency and high efficiency operation of the high voltage cascode GaN HEMT.

Three-Level Driving Method for GaN Power Transistor in Synchronous Buck Converter

The emerging Gallium-Nitride (GaN) based power transistors offer the potential to achieve higher efficiency and higher switching frequencies than possible with Silicon MOSFET's. This paper first discusses the enhancement-mode GaN device characteristics. The high reverse conduction voltage of the GaN devices makes it not preferred for synchronous converters. A three-level driving method is proposed to overcome the high reverse conduction loss issue of the GaN power transistor. Finally, a 12V to 1.2V Synchronous Buck converter with a full load current of 20A is built to verify the proposed method. The experimental results show that the proposed method is necessary and effective for efficiency improvement in high switching applications of a GaN power transistor.

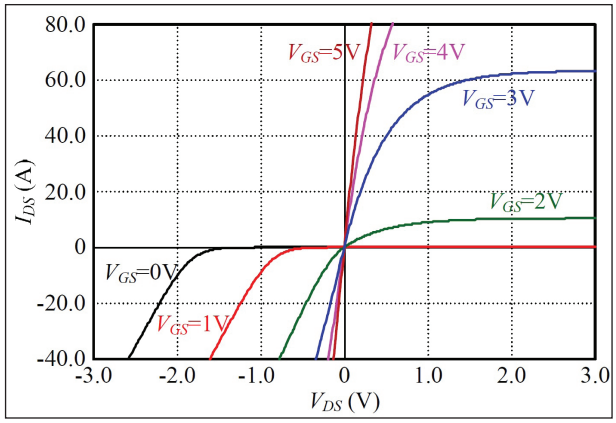


Figure 1 V-I curve of GaN power transistor (EPC 1015)

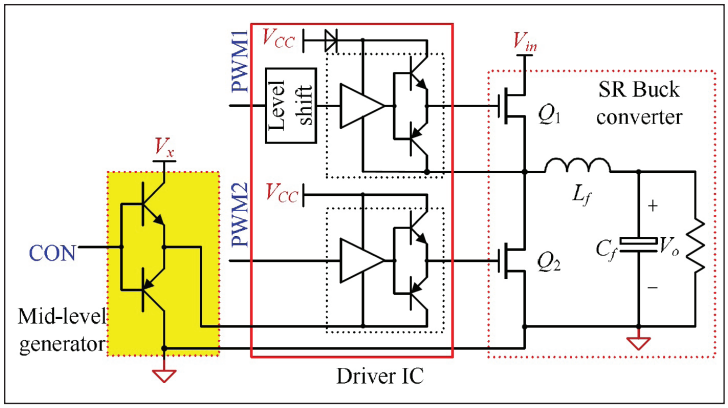


Figure 3 Schematic of 3-level driving method for buck converter

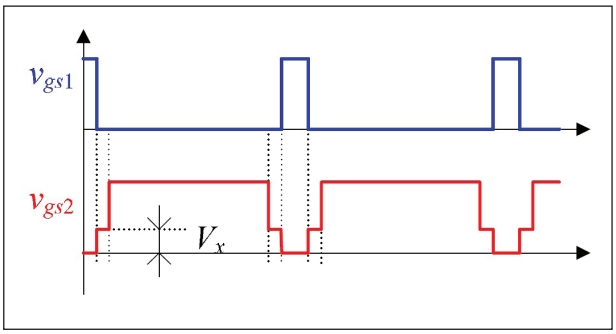


Figure 2 3-level driving method for SR buck converter

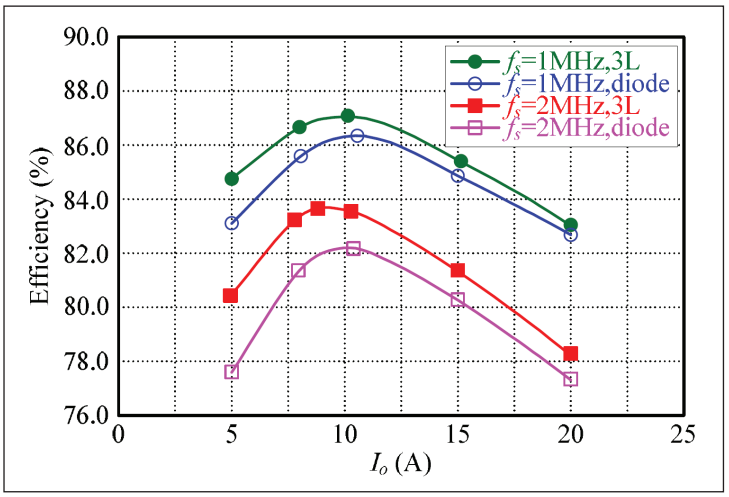


Figure 4 Efficiency comparison of diode vs 3-level at different frequency

Optimization of a High Density Gallium Nitride Based Non-Isolated Point of Load Module

The demand for future power supplies to achieve higher output currents, smaller size, and higher efficiency cannot be achieved with conventional technologies. There are limitations in the packaging parasitics, thermal management, and layout parasitics that must be addressed to push for higher frequencies and improved power density. To address these limitations, the use of integrated 3D point of load converters utilizing GaN transistors, low profile magnetic substrates, and ceramic substrates with high thermal conductivity must be considered.

This paper discusses the effect of parasitics on the performance of the high frequency GaN POL, methods to improve the circuit layout of a highly integrated 3D integrated POL module, and the thermal design of a high density module using advanced substrates with improved thermal conductivity. The final demonstration is a 900W/in^3 12V 2MHz Alumina DBC GaN converter, which offers unmatched power density compared to state of the art industry products and research. It also demonstrates a highly integrated 3D DBC module with an integrated low profile magnetic.

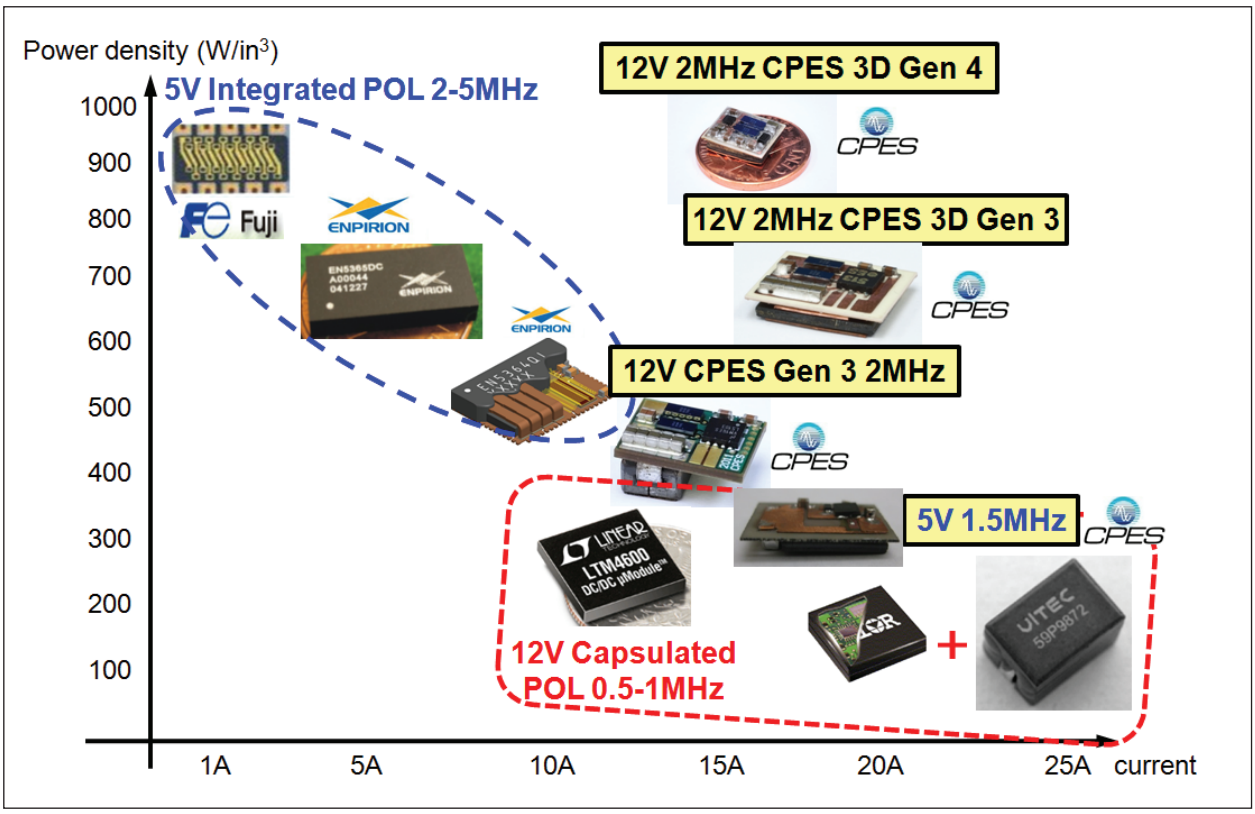


Figure 1: Power Density Map of Current High Density Power Modules

Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration

The GaN high electron mobility transistor (HEMT) has emerged as a promising device for high frequency, high efficiency, high density power conversion because of its better figure of merit than comparable Si and SiC transistors. With GaN HEMT, the switching frequency has been continuously pushed up to several Mega Hz in order to reduce the passive components size and increase power density. An accurate loss model for the high voltage GaN to estimate switching loss is highly desirable for predicting maximum junction temperatures and overall power converter efficiency.

One popular analytical loss model is the piecewise linear model, which enables simple and rapid estimation of switching loss. However, the main drawback is that it doesn't consider the parasitic inductors and nonlinearity of the junction capacitors of the device. Therefore, the result normally doesn't match the experimental results very well, especially in high frequency applications.

The other popular way to estimate switching loss of a high voltage device is based on measurement. For example, turn on energy (Eon) and turn off energy (Eoff) can be calculated based on double-pulse-test waveforms. However, the current probes introduce a substantial delay in the waveforms, typically a few nanoseconds. This delay can be estimated and proper correction introduced, but for fast switching circuits (capable of traversing from rail to rail in few nanoseconds) the error will remain huge. On the other hand, the Eon / Eoff obtained from the double-pulse-test only applies to certain test conditions including the PCB layout parasitic inductors, the capability of the driver and the characteristic of the freewheeling diode etc.

This paper analyzes the switching loss of the high voltage GaN HEMT in cascode configuration with a novel analytical model. The proposed model considers the package including the PCB layout parasitic inductors, the nonlinearity of the junction capacitors and the transconductance of the cascode GaN transistor. The switching loss is obtained by solving the equivalent circuits during the switching transition. The model is easy to understand and provides a deep insight into the switching process.

To analyze the switching loss, a simple Buck converter is used as an example. A freewheeling diode is used as the bottom switch and the parameters of the diode represent whatever electric characters in the real case. The inductor current is treated as a current source during the transition time. The final circuit model used to analyze the cascode GaN transistor switching loss is shown in Fig. 1. Actually, the simplified equivalent circuit in Fig. 5 is also suitable for other bridge configuration based topologies, such as Boost, Buck-Boost etc., to analyze the device behaviors during transition period.

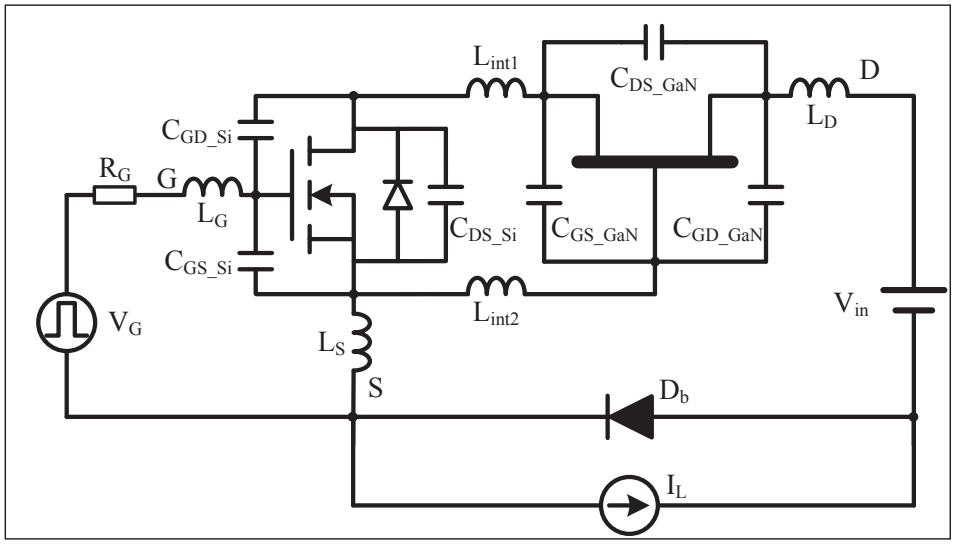


Fig. 1. Simplified equivalent circuit to analyze switching loss of cascode GaN transistor

Characterization and comparison of seven different 1.2 kV SiC power semiconductor devices at high temperature

The growing popularity of HEVs and MEAs heightens the need for high-temperature converters with high power densities. Wide-bandgap semiconductors such as Silicon Carbide (SiC) make such converters feasible due to their high thermal conductivity and high breakdown field. In previous work, SiC devices were shown to have better performance than those of conventional Si semiconductors in high-power applications. Namely, SiC devices have proven to experience lower on-resistances and faster switching speeds. Further, SiC devices have high-temperature relia-bility, which Si lacks. This improved performance has led to the commercialization of various SiC power semiconductor devices.

With the emergence of these new SiC devices, the question of how the performances of each compare to one another arises. Consequently, the focus of this research is to characterize and compare SiC power semiconductors. The static and dynamic characteristics of seven 1.2 kV SiC power semiconductor devices will be analyzed at temperatures from 25 °C to 200 °C. The studied devices are: three 1.2 kV SiC MOSFETs, two 1.2 kV SiC BJTs, a 1.2 kV normally-off SiC JFET, and a 1.2 kV SiC SJT.

For the static performance comparison, the specific on-resistance of each device will be analyzed.

The on-resistance of each semiconductor will be measured up to 200 °C, and then specific on-resistance will be calculated using die area (Fig. 1). This is done to allow for valuable comparison among the various devices since resistance and size are indirectly related. The means of comparison for the dynamic performance of each device is switching energy loss density. A double-pulse test (DPT) will be performed on each device up to 200 °C, from which the switching loss will be computed. Dividing this computed loss by the die area yields the switching energy loss density. Fig. 2 shows the high-temperature DPT setup used for measuring switching loss.

A full comparison among all of the devices will then be obtained by using the on-resistance to compute the conduction power loss density and the switching energy loss density to calculate the switching power loss density. It is expected that there will be a tradeoff between the static and dynamic performances, thus it is important to take both into account when comparing all of the devices by summing the conduction and switching power loss densities to find the total power loss density.

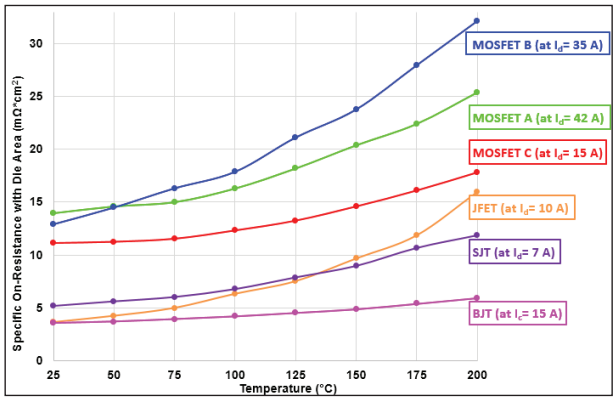


Fig. 1. Specific on-resistance vs. temperature

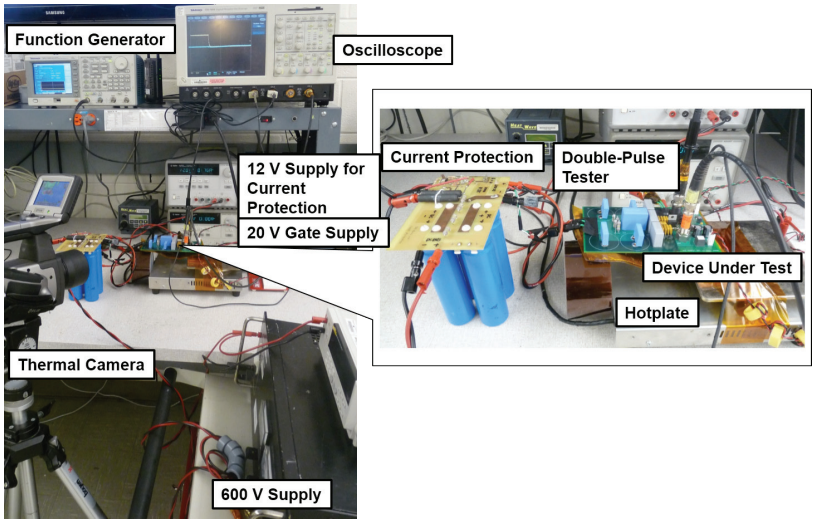


Fig. 2. High temperature DPT setup

Behavioral Comparison of Si and SiC Power MOSFETs for High-Frequency Applications

SiC MOSFETs have been proven to be ideal substitutes for Si IGBTs in medium-voltage power converters. However, how these devices are different from their Si counterparts have not been fully discussed. These questions are answered in this work through a comprehensive comparison between Si and SiC power MOSFETs in their static characteristics, switching performances, temperature behaviors, etc.

The comparison is conducted between a 600 V Si CoolMOS and a 1.2 kV SiC MOSFET, both representing the state-of-the-art technology in their respective domain. In static characteristics, the SiC MOSFET presents a lower and less temperature-sensitive $R_{DS(on)}$ than Si, especially at elevated temperatures, but also requires a higher turn-on gate voltage (Fig. 1). In terms of the dynamic parameters, the SiC MOSFET exhibits only one-quarter C_{ISS}, but comparable C_{OSS} and C_{RSS} compared to Si (Fig. 2). Smaller C_{ISS} leads to roughly 75% reduction in the total QG and much faster gate voltage responses. The switching loss of the SiC MOSFET is also more temperature-insensitive. Nevertheless, its overall switching loss is still higher than Si due to its smaller transconductance.

Through the comparison, the strengths of the SiC MOSFET are found in its high operating voltage, low conduction loss, high-temperature operation capability, and temperature-insensitivity in device losses. Due to its higher switching loss (than Si MOSFET), lower frequencies such as 70-100 kHz are more desirable for the SiC MOSFET to achieve higher efficiency and power density for the converter, although very high switching frequency operation (e.g. 500 kHz) is still possible for special applications.

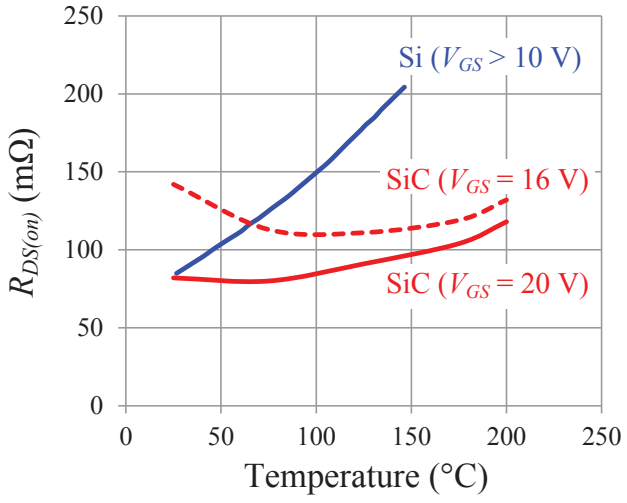


Fig. 1. Comparison of on-state resistance

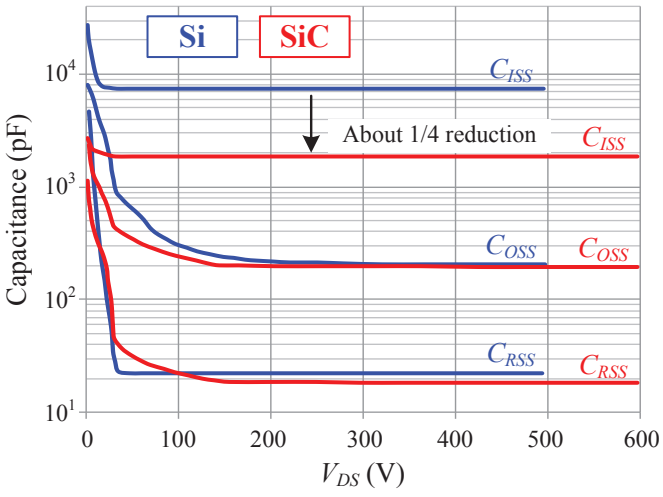


Fig. 2. Comparison of junction capacitances

Magnetic Composite Materials for High Frequency Application

Magnetic materials used for high frequency applications are usually composed of ceramic ferrite types such as the NiZn ferrites. They usually have high permeabilities and high electrical resistivities as well as low loss making them suitable at high frequencies. However, these cores are usually fabricated with an air gap that results in field fringing that increases the winding loss. Magnetic powder cores on the other hand are usually made of metal or metallic alloys such as iron and Permalloy. They have lower permeabilities and have distributed air gaps due to the built-in gaps between particles. Since they are electrically conductive, their applications are limited to low frequencies because of an increase in eddy current loss at higher frequencies, which increases faster than the hysteresis loss. The goal of this research is to develop a process and material where the particles can be coated with an insulating layer to reduce the eddy current loss and extend the bandwidth and potential application to the megahertz range. A simple low-temperature solution-based process was developed to coat magnetic powder with an insulating polymer. Compacted cores made out of Permalloy-polymer composite (Figure 1) showed a permeability that remained flat to at least 10 MHz and a resonance beyond 100 MHz. A comparison with the uncoated powder (Figure 2) showed at least an order of magnitude improvement in frequency range. The permeability of s commercial MPP core begins to drop before 1 MHz. The core loss density of each material is shown in Figure 3. For the uncoated Permalloy powder core, a core loss density of 300 mW/cc is reached at a flux density of less than 15 G at 5 MHz, while for the composite the same core loss density is reached at nearly 100 G. The core loss density of the composite at 1 MHz also matches that of the MPP core at only 500 kHz. Further development of the material may make it possible to replace bulkier cores in applications operating in the MHz range, such as the converter shown in Figure 4 in order to reduce the volume and increase powder density.

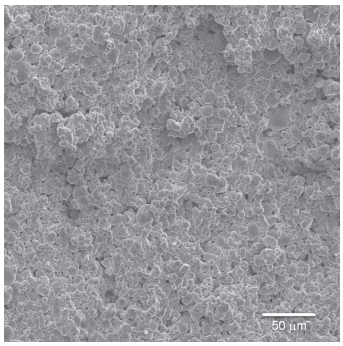


Figure 1. Microstructeof pressed Permalloy powder coated with polymer insulation.

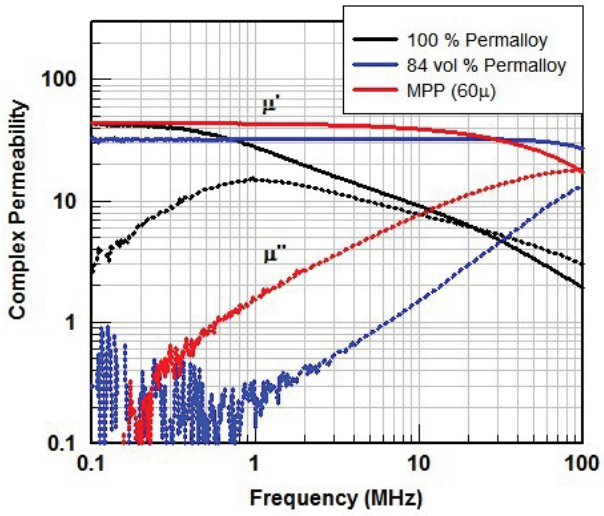


Figure 2. Complex permeabilities of uncoated Permalloy powder, Permalloy-polymer composite, and a commercial molybdenum Permalloy powder (MPP) core.

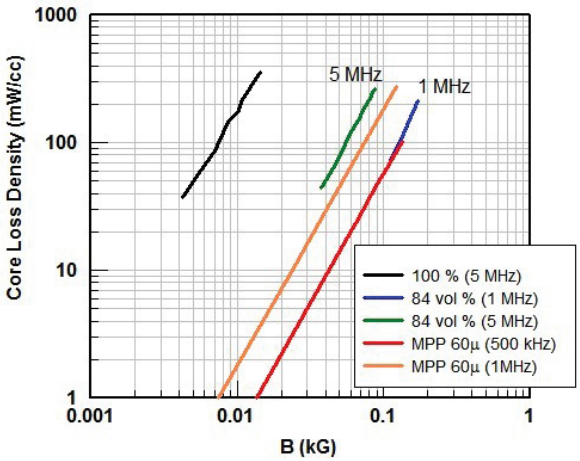


Figure 3. Core loss density comparison for uncoated Permalloy powder core, Permalloy-polymer composite powder core, and commercial MPP core.

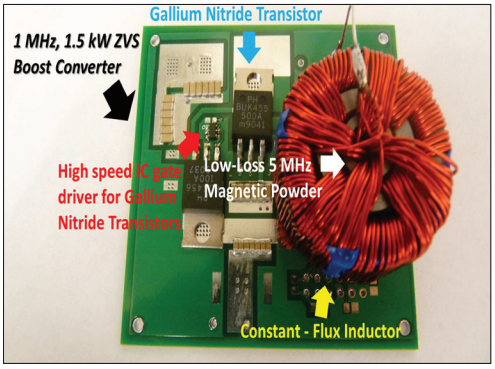


Figure 4. 1.5 kW output single phase converter operating at 1 MHz.switching frequency with 94 % efficiency.

Optimal Trajectory Control of LLC Resonant Converters for Soft Start-up

An optimal soft start-up process for the LLC resonant converter is proposed based on the graphical state-plane analysis. To settle the initial condition, the unsymmetrical-band approach, slop-band control, and two-pulse control are investigated as shown in Fig.1.

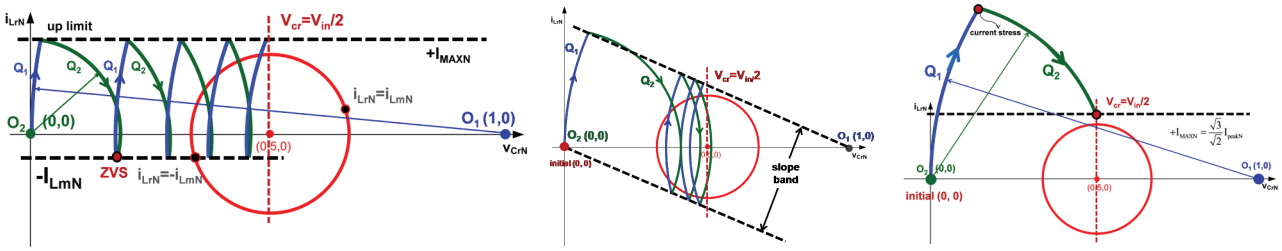


Fig. 1 Initial condition settling with different control approaches

Then, by sensing the output voltage, the optimal frequency is determined within a current limiting band as shown in Fig.2. Therefore, no current and voltage stress in the resonant tank is guaranteed during the soft start-up. Fig. 3's experimental results show that the resonant current iLr is well controlled to the current limitation band (±IMax) as designed and that the output voltage increases smoothly and quickly.

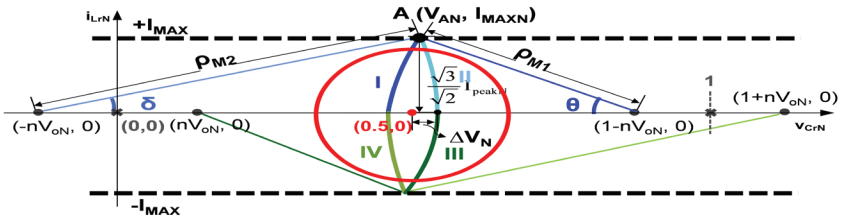


Fig. 2 Optimal trajectory control in the current limitation band

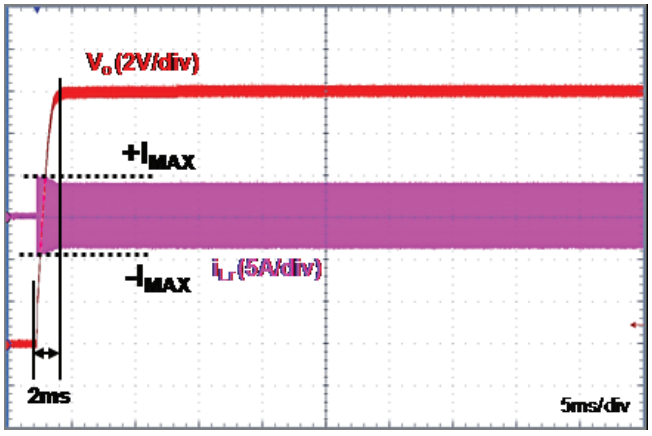


Fig.3 Experimental result of proposed optimal soft start-up

High Switching Frequency, High Efficiency, Modularized 3-level Neutral Point Clamped Phase Leg Building Block

To implement a power conversion system (PCS) or energy control center (ECC) for medium voltage high power renewable energy and nano-grid applications, a 3-phase 3-level neutral point clamped (NPC) phase leg building block was designed and fabricated as a basic building block for a grid interface converter. To achieve excellent performance of this converter, such as high switching frequency, high efficiency, high reliability and also high power density, the phase leg should be carefully designed for its layout and gate driver. Switching performance optimization is also needed for each switch.

The phase leg structure and layout are shown in Fig.1. Each phase leg has four main switches, which are 1200V/400A single IGBT module. Two clamping devices are in the same rating. DC link capacitors are evenly distributed on each phase leg to support the DC link voltage. All the interconnection for devices and phase leg are implemented by laminated bus bar, which can effectively reduce the loop parasitic inductance. The optimized layout design reduces loop inductance and can therefore improve switching performance.

The switching loop in a 3-level phase leg can be categorized into two types as shown in Fig.2. The switching loop for the outer switch is shorter with 2 modules and 1 connection. On the contra-ry, the inner switch loop is longer with 4 modules and 3 connections, resulting in a larger loop parasitic inductance. The switching characteristics for the inner and outer switch loop are there-fore different. The gate resistor for the inner and outer switch should be selected accordingly. The gate resistance is a key factor for switching performance optimization as it influences both the switching loss and stress. To achieve both a high switching frequency and a high efficiency, a gate resistor value should be small enough to minimize switching loss. But voltage and current stress will be inevitably increased. The tradeoff for loss and stress should be considered and treated differently for inner and outer switch for an optimum switching characteristic. Based on the experimental result, the total loss for one line cycle can be calculated under a different operating condition. Fig.3 gives the total system loss for both the diode clamped NPC (DNPC) and the active clamped (ANPC) converter under a different power factor. The system efficiency is around 98% with a 20 kHz switching frequency.

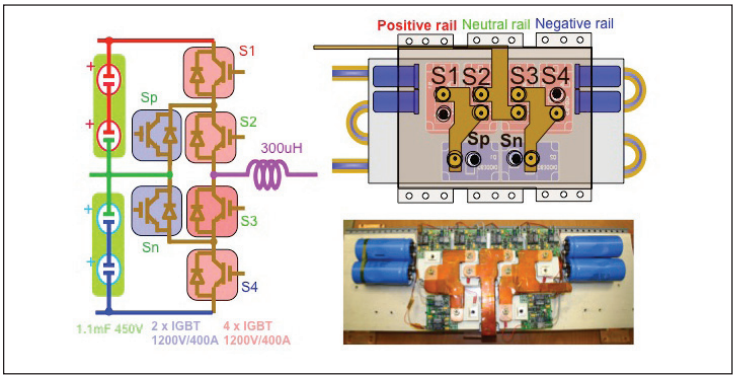


Fig. 1.3-level NPC phase leg structure and layout

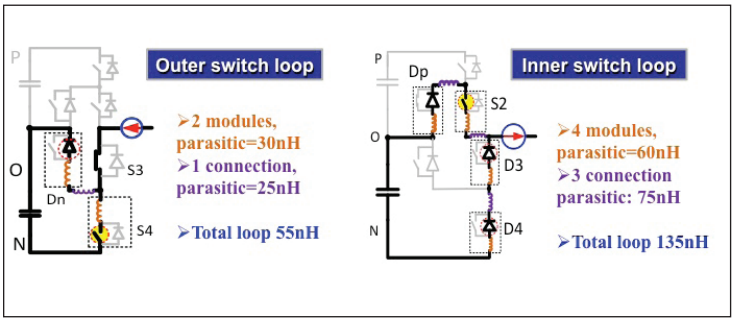


Fig.2. Parasitic inductance with different switching loops

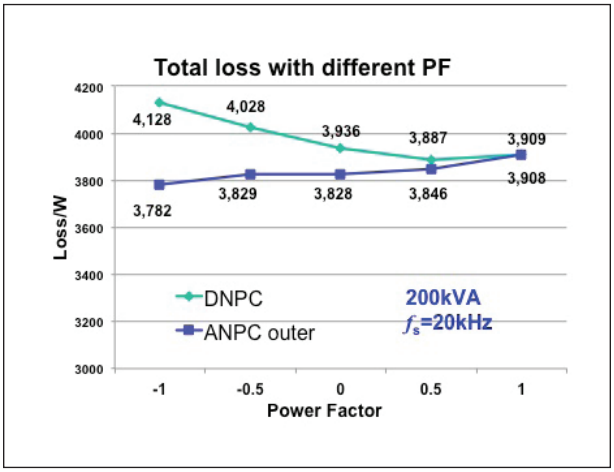


Fig. 3 Total system loss with different power factor for DNPC and ANPC phase leg

External Ramp Autotuning for Current Mode Control of Switching Converters

Many current mode controllers try to cover a wide input and output voltage operation range. However, for peak current-mode control when the duty cycle (D) is above 0.5, subharmonic oscillations occur and the quality factor (Q_2) of the high-frequency double pole in the control to output voltage transfer function ($V_o(s)/V_c(s)$) becomes negative as shown in (1). An external ramp slope (S_e) is added to help stabilize the system. Conventionally, to ensure the stability for a wide duty cycle range, a fixed S_e over-compensates the double pole, so the system bandwidth (BW) is limited. Therefore, several adaptive ramp strategies have tried to make S_e tracks S_f change, so proper S_e can be chosen for different D.(this does not make sense) Figure (1) shows that when $S_e=S_f$, $Q=2/\varpi$. However, the tracking error from the inductor variation still causes overcompensation, because Q is no longer constant when $S_e \neq S_f$.

This paper discovers that as long as S_e is tuned with the real current slope change (S_n, S_f), Q_2 can be well-controlled, since input voltage, output voltage, and inductance variations are exhibited in the current feedback signal (i_L*R_i). The high frequency characteristic of $V_o(s)/V_c(s)$ is fixed and immune to those variations, so a high BW design can be achieved. S_n and S_f are sensed by differentiating the current feedback signal with the RC circuit and then sample-and-holding the two slope values. After that, the external ramp for desired Q_2 can be calculated by the simple control law in Figure (2).

Finally, simple digital and analog implementations are proposed to realize the autotuning method into peak current mode, valley current mode, and average current mode controllers. Also, they can be used in different topologies without changing control law and tuning circuitry. The simulation and experimental results verified the effectiveness of proposed method, as shown in Fig. 3.

$$Q=\frac{1}{\pi\left(\frac{s_n+s_e}{s_n+s_f}-0.5\right)} \quad (1) \qquad S_e=\left(\frac{1}{Q\pi}+0.5\right)\cdot S_f+\left(\frac{1}{Q\pi}-0.5\right)\cdot S_n \quad (2)$$

Where S_n and S_f are the rising and falling slope of the inductor current respectively. For the buck converter, $S_n=(V_{in}-V_o)R_i/L$ and $S_f=V_oR_i/L$. R_i is the current sensing gain and L is the filter inductance.

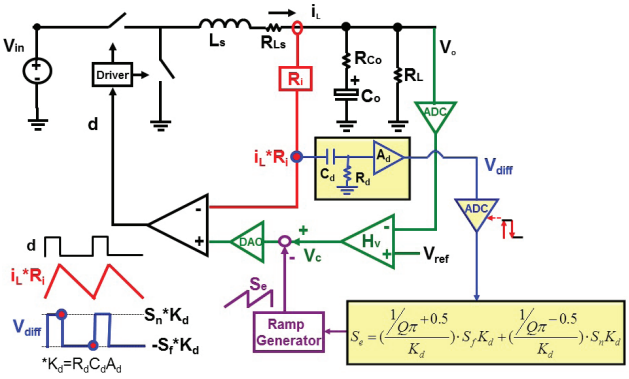


Fig. 1. Peak Current Mode Control with Digital Autotuning Block

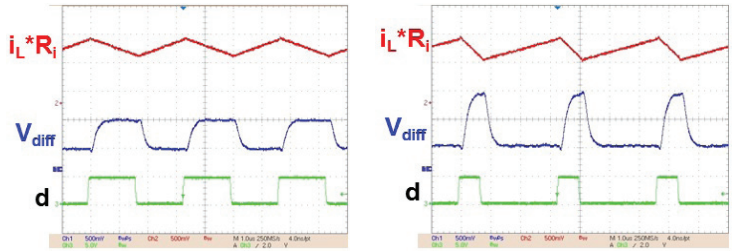


Fig. 2. Measurement of differentiated waveform (V_{diff})

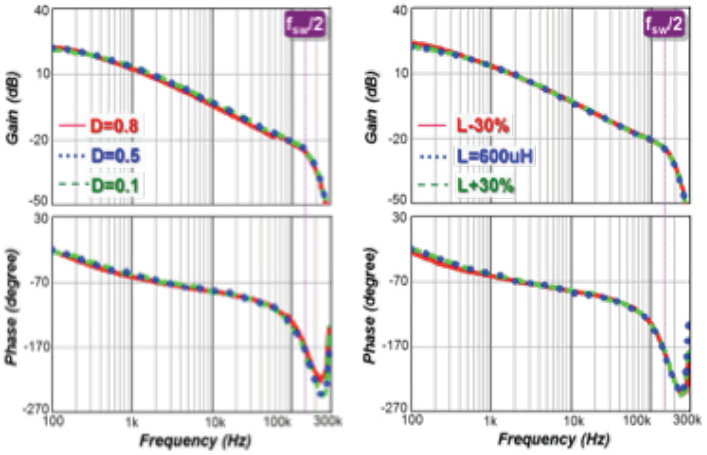


Fig. 3. Measured $V_o(s)/V_c(s)$ with digital autotuning block

Dual Active Bridge based Battery Charger for Plug-in Hybrid Electric Vehicle with Charging Current Containing Low Frequency Ripple

High power density is strongly preferable for the on-board battery charger of a Plug-in Hybrid Electric Vehicle (PHEV). Wide band gap devices, such as Gallium Nitride HEMTs are being explored to push higher switching frequencies and reduce passive component size. In this case, the bulk DC link capacitor of the AC-DC Power Factor Correction (PFC) stage, which is usually necessary to store ripple power of two times the line frequency in a DC current charging system, becomes a major barrier on power density. If this low frequency ripple is allowed in the battery, the DC link capacitance can be significantly reduced. Recent studies show that the performance of lithium-ion batteries does not deteriorate much with the current ripple at two times line frequency. If all ripple power flows into the batteries, the charging current will behave in a sinusoidal waveform with a DC bias as

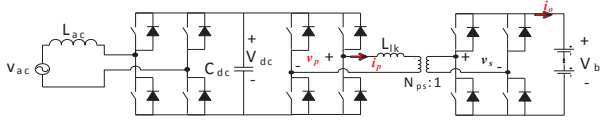


Fig. 1. Battery charger topology with a Full Bridge (FB) AC-DC stage plus a Dual Active Bridge (DAB) DC-DC stage

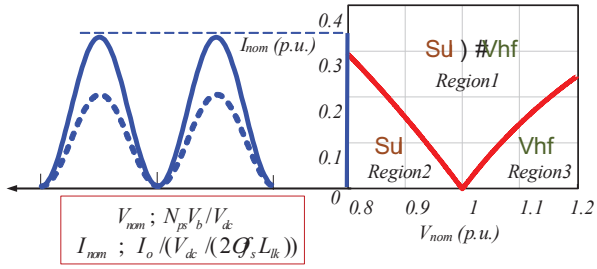


Fig. 2. DAB ZVS analysis with phase shift modulation

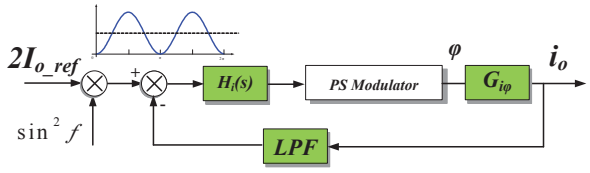


Fig. 3. Block diagram of the control loop

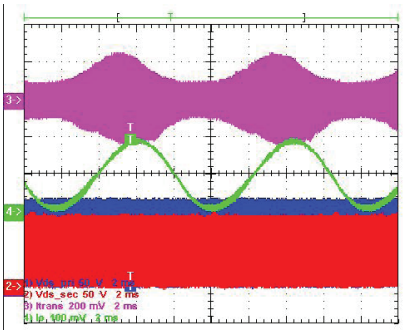


Fig. 4. Experiment results of sinusoidal charging

$$i_o(t) = p_{in}(t)/V_{bat} = V_{ac}I_{dc}/V_{bat}\cdot[1-\cos(2\omega t)] = I_o(1-\cos 2\omega t) = 2I_o\sin^2(\omega t) \quad (1)$$

The ripple power at two times the line frequency in (1) will compensate the ripple power at the input side, thus ideally the DC link capacitors to store this ripple power can be eliminated. This idea is implemented in a battery charging system comprised of one Full Bridge (FB) AC-DC stage and one Dual Active Bridge (DAB) DC-DC stage. DAB is a promising topology especially for isolated and bi-directional power conversion. It has many benefits, such as Zero Voltage Switching (ZVS) for both primary and secondary bridges, small passive sizes, utilization of parasitic and fixed switching frequency. The DAB ZVS range is shown in Fig.2 when phase shift modulation is used. It can be seen that hard switching of the devices, either in the primary bridge or the secondary bridge, always happens due to the severe variation of the sinusoidal output current. In order to realize sinusoidal charging, the control schemes in Fig. 3 is proposed. Since the transfer function from phase-shift to output current can be modeled as a constant gain, the main part of the dynamic behavior of the DAB will be determined by the low pass filter used to attenuate the high frequency current ripple at the output.

The experimental results are shown in Fig. 4.

A Universal Adaptive Driving Scheme for Synchronous Rectification in LLC Resonant Converters

A universal adaptive driving scheme for a synchronous rectification (SR) is proposed as shown in Fig. 1. The drain to source voltage of the synchronous rectifier is sensed, so that the paralleled body diode conduction is detected. Using the proposed SR driving scheme, the SR turn-off time is tuned to eliminate the body diode conduction as illustrated in Fig. 2. The SR gate driving signal can be tuned within all operating frequency regions. Compared to analog ones, it enables more intelligent and precise SR control, improving converter efficiency.

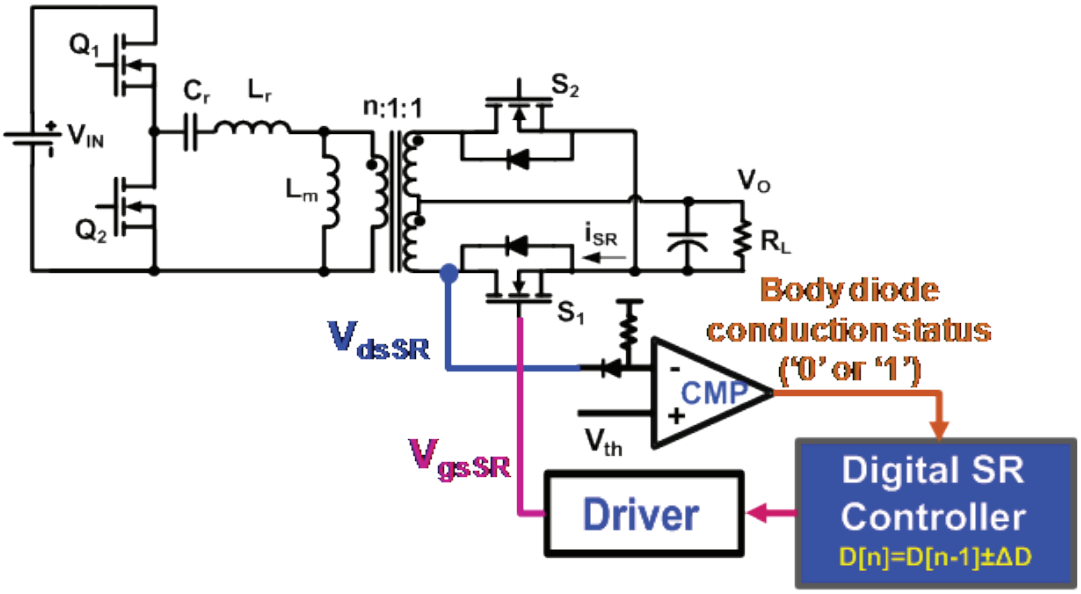


Fig.1 Control scheme of proposed intelligent SR driving scheme

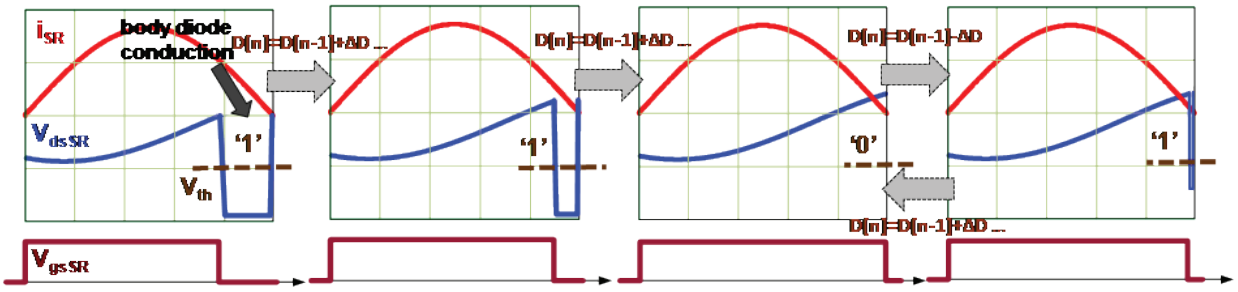


Fig.2 SR tuning process by sensing drain-to-source voltage

Optimal Trajectory Control of Burst Mode for LLC Resonant Converter

A novel LLC resonant converter burst mode control with constant burst time and optimal switching pattern is proposed for the highest light load efficiency. A three pulse switching pattern is applied during burst time. The first pulse width is optimized to settle the steady-state under the highest efficiency load condition in one pulse. Zero current detection (ZCD) of the resonant current is implemented to achieve a first switch partial ZVS, further increasing the light load efficiency.

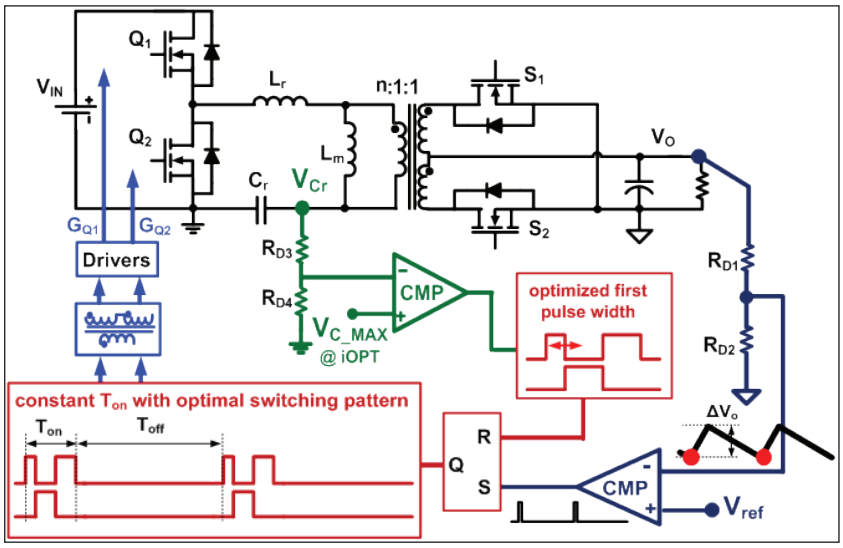


Fig.1 Control block of proposed burst mode

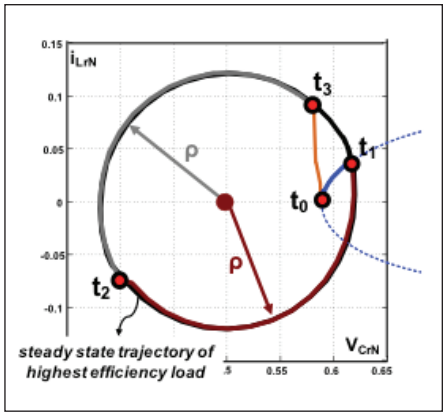


Fig.2 Trajectory of proposed burst mode

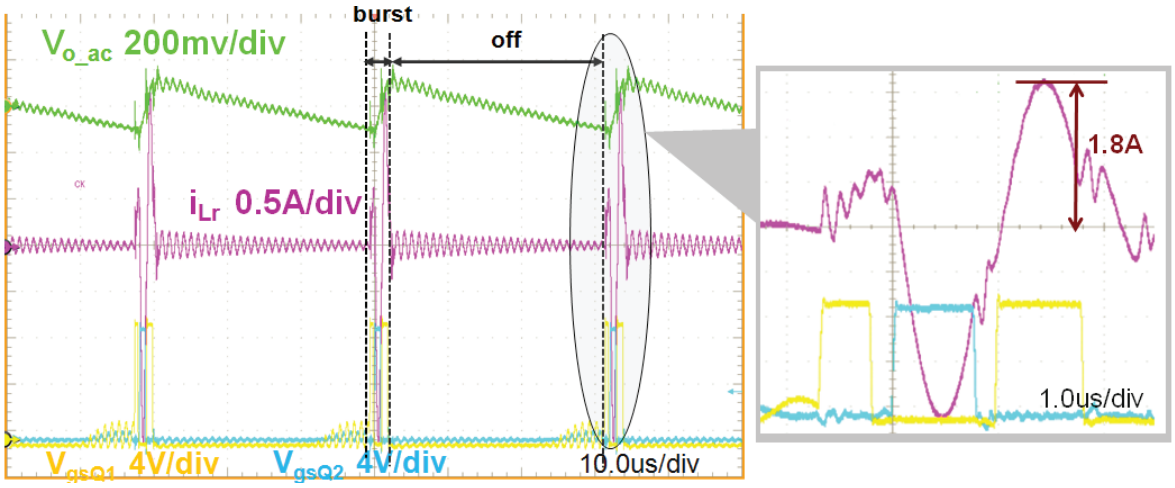


Fig.3 Burst waveform when light load is 1A

Modulation Methods Comparison for Neutral-Point-Clamped Three-Phase Inverters

The voltage-source pulse-width modulation (PWM) inverter has made a significant contribu-tion in achieving energy conservation and improving system performance in many applications. Compared with two level voltage source inverters, neutral-point-clamped (NPC) inverters can achieve better performances on ripples, harmonics and EMI. The additional choices in switching the states of the NPC converter provide many opportunities for optimizing a system to reach a low differential mode harmonic performance and, minimum dc-link ripple current, also known as nearest three space vectors (NTSV) modulation. To reduce the EMI filter size, the additional choices in switching states of the NPC converter also provide the options to reduce the common mode (CM) output voltage generation known as common mode reduction (CMR) modulation. There is also a modulation method which can theoretically eliminate the common mode voltage referred as common mode elimination (CME) modulation to further reduce the EMI filter size.

Based on the detailed implementation of the three modulation methods, system performance on CM noise reduction, NP voltage ripple and semiconductor losses are analyzed and compared in detail. The results show that CMR modulation can help to reduce both DM and CM noise in the EMI range. CME modulation will increase system DM noise but it can help to reduce the CM noise, while the benefit of CME modulation is highly related to the DT in the system. The analytical calculation method of the NP voltage ripple is discussed in detail and both analytical and experimental results are shown to compare

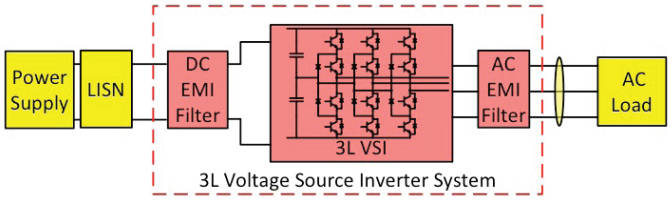


Figure 1: Three level voltage source inverter system

the NP voltage ripples using three different modulation method. Moreover, the loss calculation is also discussed in the paper, the analytical calculation result is shown, which shows that the losses are comparable between NTSV and CME modula-tion while CMR modulation can reduce the switching losses by about 30%.

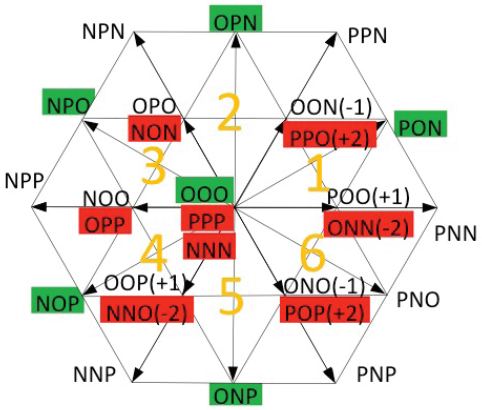


Figure 2: switching states in 3L VSI

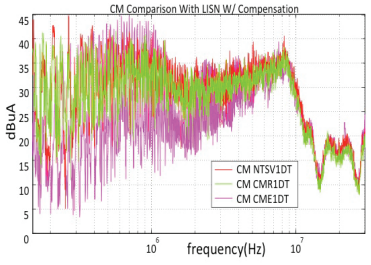


Figure 3: CM current spectrum

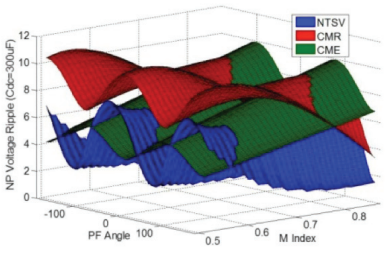


Figure 4: NP voltage ripple comparison

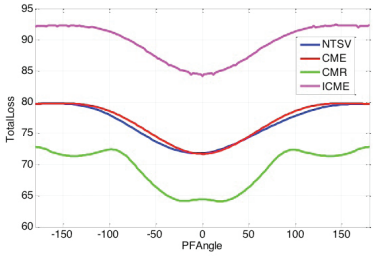


Figure 5: device loss comparison

Ripple Power Balance Analysis on Plug-in Hybrid Electric Vehicle Charger with Sinusoidal Charging

High power density is strongly preferable for the on-board battery charger of a Plug-in Hybrid Electric Vehicle (PHEV). Wide band gap devices, such as Gallium Nitride HEMTs are being explored to push higher switching frequencies and reduce passive component size. In this case, the bulk DC link capacitor of the AC-DC Power Factor Correction (PFC) stage, which is usually necessary to store ripple power of two times the line frequency in a DC current charging system, becomes a major barrier on power density. If this low frequency ripple is allowed in the battery, the DC link capacitance can be significantly reduced. Recent studies show that the performance of lithium-ion batteries does not deteriorate much with the current ripple at two times line frequency. If all ripple power flows into the batteries, the charging current will behave in a sinusoidal waveform with a DC bias as

$$i_o(t) = p_{in}(t)/V_{bat} = V_{ac}I_{ac}/V_{bat}\cdot[1-\cos(2\omega t)] = I_o(1-\cos 2\omega t) = 2I_o\sin^2(\omega t) \quad (1)$$

The ripple power at two times the line frequency in (1) will compensate the ripple power at the input side, thus ideally the DC link capacitors to store this ripple power can be eliminated. However, non-ideal effects, such as control delay and converter losses will cause ripple power imbalance, and increase on the DC link voltage ripple if the capacitance is fixed. For example, constant conversion loss in the AC/DC stage can be represented by an equivalent paralleled resistor in the converter average model of Fig. 2, then the ripple power between input and output becomes imbalanced. The ripple power in the DC link capacitor will be

$$p_{ripple}(t) = -P_{loss}\cos(2\omega t) \quad (2)$$

To solve this issue, the imbalance can be compensated by controlling the output current in the form of (b) in Fig. 3. With the proposed loss compensation control scheme, the dc link voltage ripple can be reduced from 16.8V to 19.9V with only 10% compensation. It is a 15.6% reduction, as shown in Fig. 4.

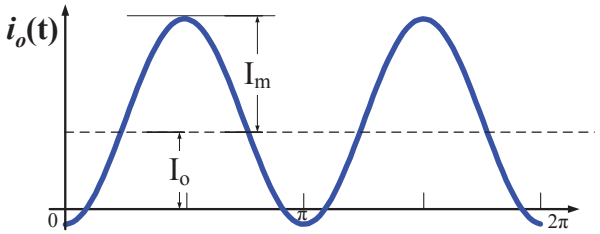


Fig. 3. Output current waveform with loss compensation

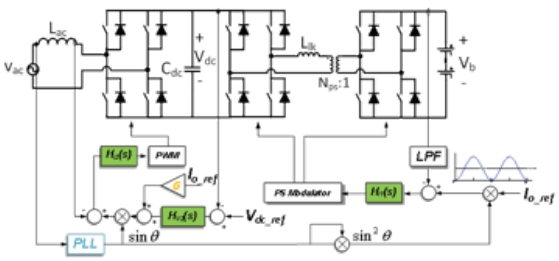


Fig. 1. Battery charger topology with a Full Bridge (FB) AC-DC stage plus a Dual Active Bridge (DAB) DC-DC stage

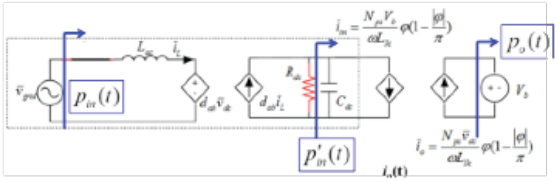


Fig. 2. Average model of topology considering constant loss in AC/DC stage.

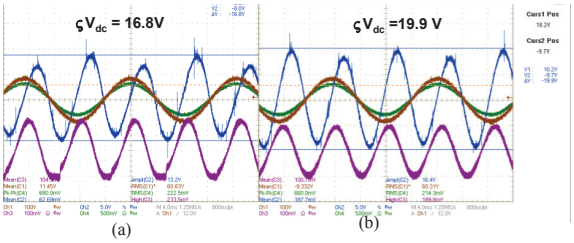


Figure 4: Experimental results of DC link voltage ripple

A Testbed for Experimental Validation of a Low voltage DC Nanogrid for Buildings

The architecture of an electric power system is a major factor for the system structural practicability, safety, size, weight, energy efficiency, reliability, and ultimately the cost of energy utilization. Although most of these are actually quantifiable physical variables, the final choice of the electrical architecture when building or designing new electric power systems is, quite logically, very often made as a result of either different engineering traditions and experiences, or higher confidence in using proven and established practices. A dc nanogrid, which is a hypothetical future sustainable home electronic power distribution system with dc-based distribution and the presence of renewable energy sources is examined in this paper.

The DC nanogrid system presents an integrative solution to satisfy the energy, functional, comfort, and zero-CO_2 emission goals for a future building/home environment by utilizing an autonomous operation of the various system components. Although still in the early phase, the testbed described in this paper provides an environment for research, evaluation, and demonstration of advanced technologies for sustainable buildings. It also offers an opportunity to lower down the cost, improve acceptance, and increase the overall energy harvesting efficiency of a renewable energy sources for the future home.

DC nanogrid infrastructure, in some preliminary form, has been built and installed in the lab as depicted in the Fig.1, along with the three components of the nanogrid system: grid-, battery-, and PV-interface converter. Fig. 2 shows one of the experimental waveforms steady state.

The future work on this testbed will, among other tasks, address the major issues of the load sharing and shedding, stability, power management and protection. Additionally, more research effort will be put on the system-level operation including wind generation, PHEV, and constant power loads.

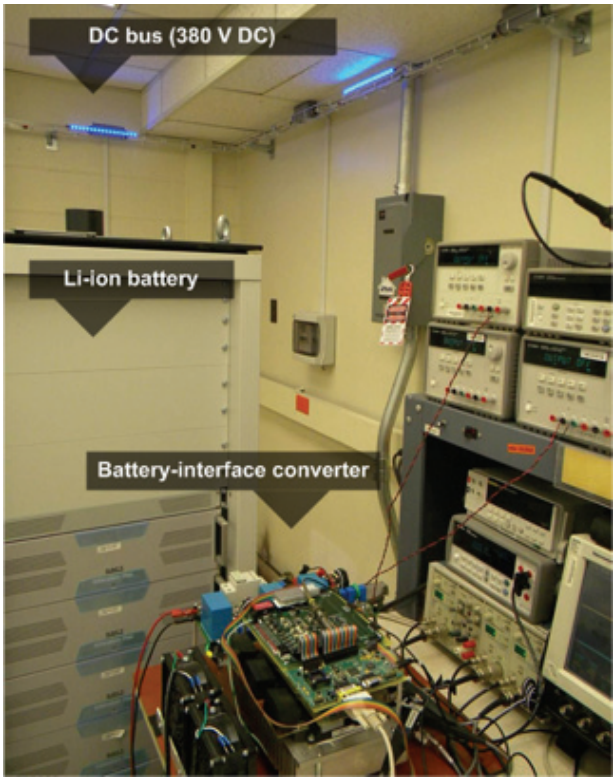


Fig. 1. The laboratory setup showing the 10 kW prototype of the bi-directional battery interface converter, Lithium-ion battery bank and a part of the dc-bus.

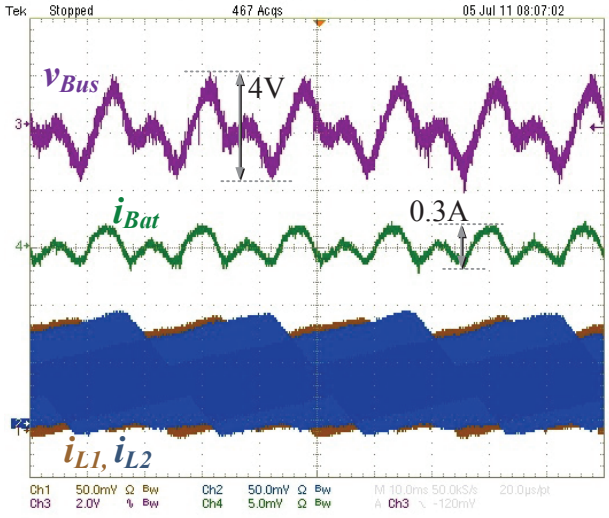


Fig. 2. Bus voltage and battery current ripple in the steady state (iL_1 an iL_2 are two out of three battery interface converter inductor currents)

Leakage Current Reduction in Single-phase Bi-directional ac-dc Full-Bridge Inverter

The leakage current in grid-interface converter systems presents a considerable issue in regard to safety and efficiency. The full-bridge inverter is a well-accepted topology in single-phase power conversion applications. The high-frequency PWM modulation schemes are normally applied to the full-bridge topology because of its smaller ac filter size. This generates a high-frequency dc-side leakage current resulting in an enormous negative impact on dc components, such as photovoltaic (PV) panels and energy storage elements. In this nugget, a modified full-bridge inverter topology to reduce the dc-side leakage current as well as to mitigate the ac-side CM electromagnetic interference (EMI) noise is proposed with detailed design procedures. Compared to the other existing methods, the proposed solution provides a reliable performance for bi-directional operation, minimum additional components, low cost, and a simple design process.

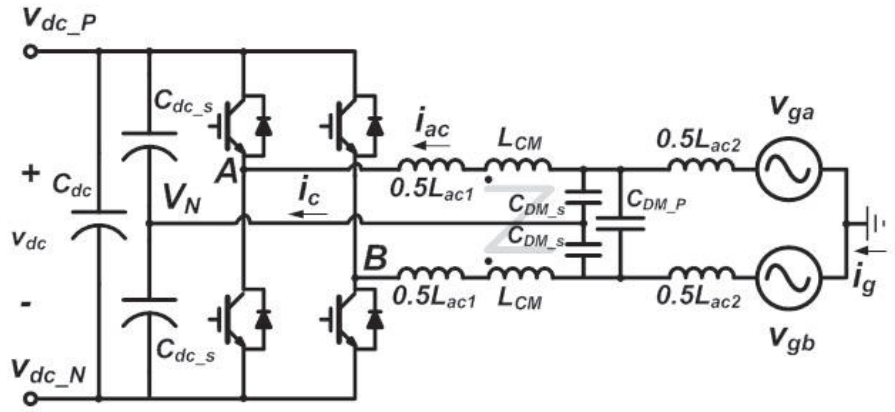


Fig. 1 modified full-bridge inverter

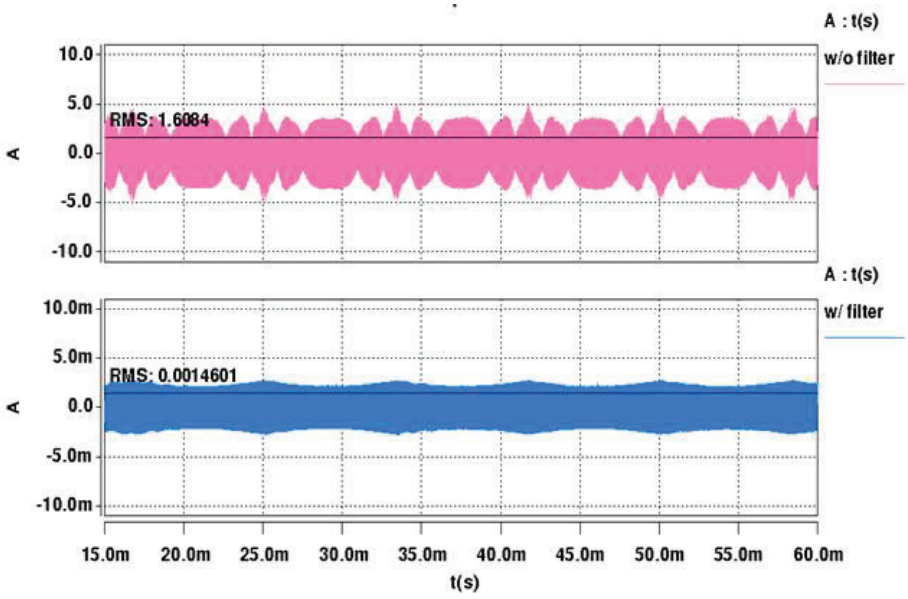


Fig. 2. Leakage current level by using the typical full-bridge inverter (upper waveform, [5A/DIV]) and the modified full-bridge inverter (lower waveform, [5mA/DIV])

Modular-Multilevel-Converters Family – A Survey of Features, Topologies, Controls and Applications

Modular-Multilevel-Converters (MMC) are merging to be attractive in both industrial applications and academic research. The most distinctive advantage of MMC is that it delivers very high voltage with excellent harmonic performance by stacking modular cells that are merely composed of low voltage rating components, without any transformers for isolation. Thus, the transformer-less modularity and scalability brought by the features of MMC cause it to be competitive in high voltage applications. Typical examples are the SIEMENS HVDC-Plus and ABB HVDC-Light, both of which have already been operating steadily as mature products for years. Additionally, re-search is also taking place to address the problems in utilizing MMC for medium voltage applica-tions such as STATCOMs and motor drives.

The building-block cell is the basic unit of the MMC giving unipolar or bipolar voltages at its output terminals. Normally, a half-bridge or H-bridge is most often used as the circuit for each cell, however, theoretically it could be any topology that has a capacitive DC and two-terminal AC outputs. Those cells could be connected in various topologies, such as Star/Delta, Matrix and Hexagonal MMC, in order to meet specific application requirements. e.g. the basic MMC topology in Fig.1 fits perfectly for the HVDC transmission.

One feature of the MMC that is different from other multilevel converters is the circulating current induced by harmonic ripples on cell capacitors. This current can bring about additional power loss and unstable risks, so it should be controlled for proper purpose in specific applications.

Researching endeavors on MMC can be categorized into different function blocks respective-ly, shown in Fig.2. Literature has been published that aims to solve problems or to raise new proposals in domains such as V/I or P/Q controller design, circulation current control, capacitor voltage balancing, PWM multilevel modulators and so forth. Furthermore, research on variable frequency applications like motor drives, where there is probably the biggest disadvantage for MMC locates, is also being carried out to expand the areas of implementation of this topology.

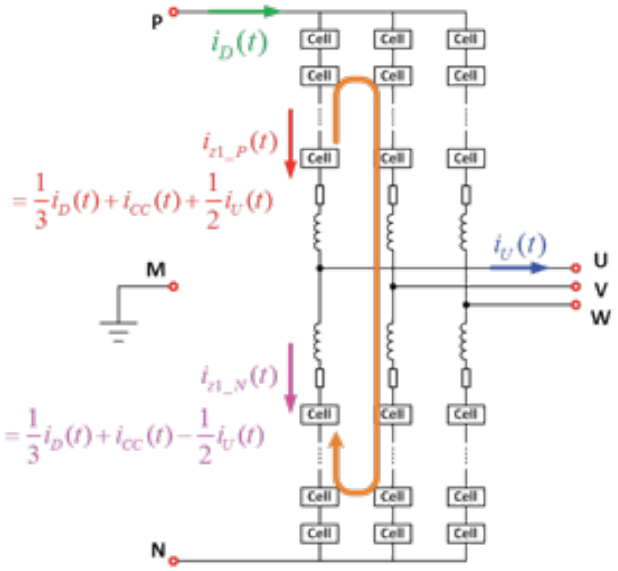


Fig. 1. Three-phase bridge of Modular-Multilevel-Converter

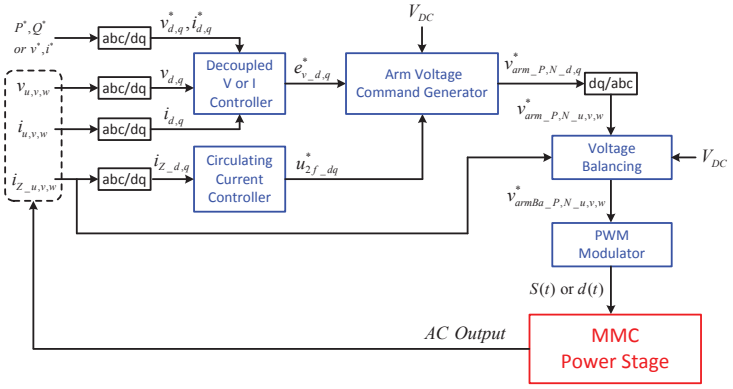


Fig. 2. Basic control diagram of Modular-Multilevel-Converter

FPGA-Based Gain-Scheduled Controller for Control Optimization of Resonant Converters Applied to Domestic Induction Heating

Fig. 1. Induction heating appliances: main parts of an induction heating cooktop.

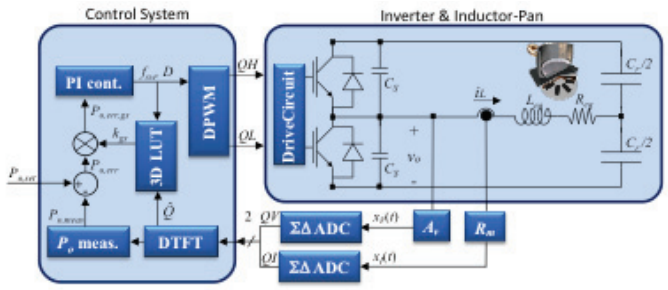


Fig. 2. Proposed gain-scheduled controller block diagram.

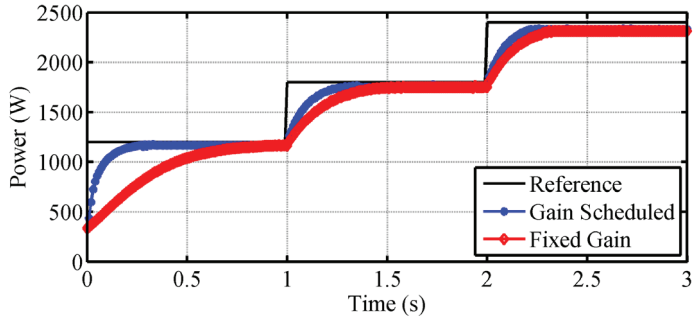


Fig. 3. Experimental results for several output power steps at different operating conditions for a standard PI controller and the proposed gain-scheduled controller.

Induction heating has become the technology of choice for domestic applications (Fig. 1) due to advantages in efficiency, quickness, safety, and accurate power control. One of the main ele-ments to achieve this performance is the resonant inverter used to supply the inductor that generates the electromagnetic field to heat the induction target, i.e. the pot.

The resonant tank of the inverter is composed of the inductor-pot system. One of the most challenging points when designing an IH appliance is to accurately adjust the control system, since the resonant tank changes with the frequency, temperature, pot materials and geometry. In this paper, a gain-scheduled controller is proposed to improve the dynamic performance under different operating conditions. The proposed approach takes advantage of digital control techniques to obtain improved performance and safety. The proposed controller (Fig. 2) combines information about the operating conditions, i.e. inverter switching frequency and duty cycle, with a real-time impedance identification system to adapt the controller gain. As a result, transient performance is improved over the wide range of operating and load conditions of an induction heating appliance.

The proposed approach has been tested with a 3-kW resonant inverter. Fig. 3 shows several transients comparing a classical PI controller with the gain-scheduled one. It can be seen that the proposed controller improves the performance in complete operation range, whereas the PI controller is just optimized for a single operation point.

State of the art: survey of FACTS devices

Flexible AC Transmission System (FACTS) devices improve the operation of power systems thanks to the development of power electronics. FACTS devices are invented with three main objectives: 1) to increase the power transmission capability; 2) to direct the power flow to the desired paths; 3) to optimize the control of the whole power system. Clearly, FACTS devices will largely utilize the existing and new transmission facilities and make it easier to adopt more renewable resources to the grid.

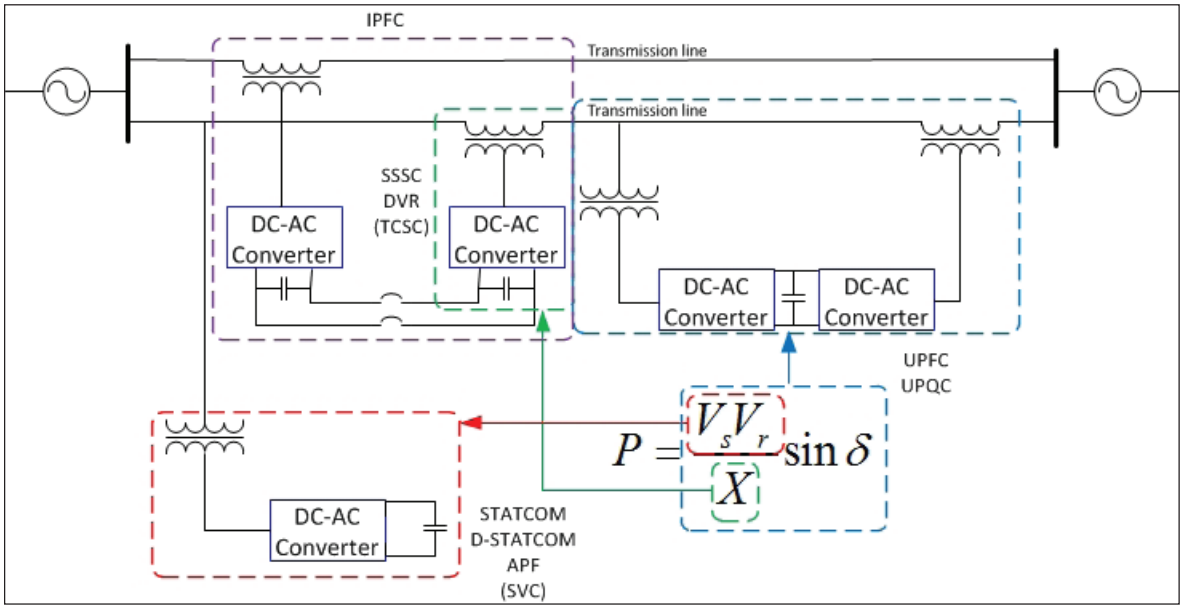


Fig. 1. A whole picture of FACTS devices family

As Fig. 1 shows, FACTS devices can be derived by changing different terms of the transmission capability equation. To control the end voltage, a static var compensator (SVC) and a static synchronous compensator (STATCOM) are used. To change the line reactance, a thyristor controlled series compensator (TCSC) and a static synchronous series compensator (SSSC) are suitable to utilize. For a more powerful control over power flow, there are unified power flow con-trollers (UPFC) and interline power flow controllers (IPFC). Applications in distribution systems are distributed to a static synchronous compensator (D-STATCOM), a dynamic voltage restorer (DVR), an active power filter (APF) and a unified power quality compensator (UPQC).

The two main applications of FACTS in the power system are power flow control and oscilla-tion damping, which needs accurate models to apply FACTS into the conventional program. To achieve the functions, a global control with coordination of multiple FACTS devices and optimiza-tion is extremely important while selection of control inputs and measurement variables also need to be taken into account. Furthermore, the location of FACTS devices can also be an issue with respect to different characteristics of the devices and the power system.

Because of the faster response and more potentially powerful compensation capability than the traditional compensators, FACTS devices are very promising under high penetration of re-newable energies, which will probably be realized within a few decades.

Small Signal Analysis of V² Control Using Current Mode Equivalent Circuit Model

In V² control, the direct feedback contains the information of both state variables. In this paper, by separating current feedback and capacitor voltage feedback, an equivalent circuit of V² control based on the equivalent circuit of current mode control is proposed. The proposed equivalent circuit provides a clear physical insight of V² control. V² control can be interpreted as an implementation of current mode control with direct voltage feedback and load current feedback. The load current feed-forward dramatically reduces the output impedance. The model is extended to enhanced V² control. The proposed equivalent circuit model is applicable to both variable frequency modulation and constant frequency modulation.

The direct output voltage vo feedback consists of inductor current, capacitor voltage and load current feedback. Inductor current feedback loop does not have a low pass filter, so all the sideband frequencies (f_{sw}-f_m, $f_{sw+}f_m$, etc.) are fed back to the modulator. Other feedbacks are simpler: for a voltage regulator, the impedance of the capacitor branch is much smaller than that of the load resistor at $f>f_{sw}/10$. Assuming the capacitor ESR zero is well below half switching frequency, the impedance of ESR is much larger than that of the intrinsic capacitance, so the sideband components at v_{cap} are overwhelmed by the ESR voltage.

According to the analysis above, it is reasonable to consider all the sideband frequency feedback effect in the inductor current loop, but only consider fundamental frequency in the capacitor voltage and load current feedback. The inductor current loop is a highly nonlinear entity. It potentially has sub-harmonic instability. A three-terminal switch equivalent circuit model based on the result that the describing function derivation accurately predicts the small signal properties of this nonlinear entity. Substitute the closed current loop and the PWM switch by the equivalent circuit mode, the proposed equivalent circuit model of V² control is shown in Fig.1.

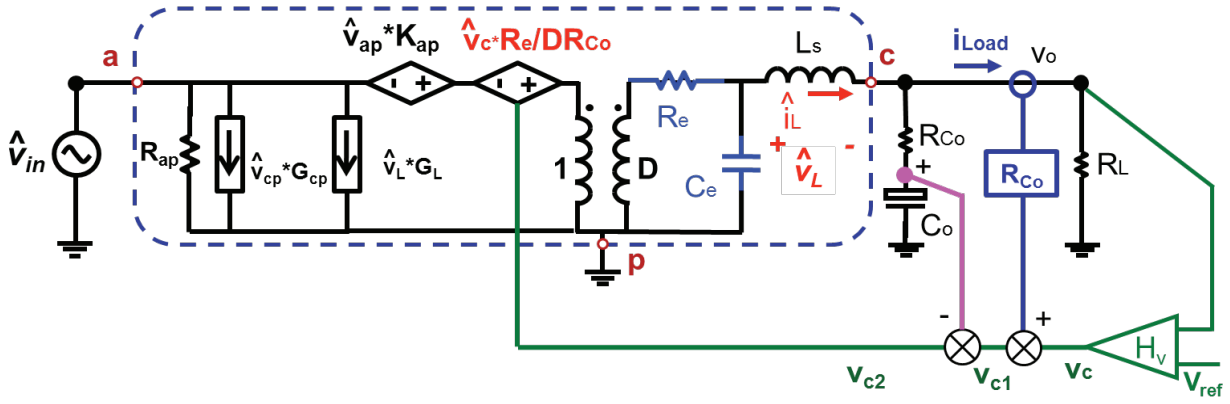


Fig.1 Small signal equivalent Circuit of V² Control

Nonlinear Sideband Effects in Small-Signal Input dq Admittance of Six-Pulse Diode Rectifiers

This paper focuses on the modeling of the small-signal input dq admittance of six-pulse diode rectifiers, providing comparison between well-known averaged value models (AVMs), the switching simulation model and hardware measurements. The analytical AVM (AAVM) is a widely used solution for modeling a six-pulse diode rectifier, but it is shown that it has to be modified in order to model the input dq admittance more accurately. Analytical expressions of small-signal input dq admittance of AAVM are derived and given in (1). The obtained analytical expressions are compared to small-signal dq admittances of a switching simulation model as shown in Fig. 1.

$$\begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix} = \sqrt{0.5} \begin{bmatrix} (\beta_d Y_{dc}(s) A_{dc} + G_d) & -\dfrac{I_{sq}}{V_{srms}} \\ (\beta_q Y_{dc}(s) A_{dc} + G_q) & \dfrac{I_{sd}}{V_{srms}} \end{bmatrix} \quad (1)$$

Furthermore, a parametric AVM (PAVM) is included in the analysis. "Slightly modified" and analytical expressions for all four dq admittances are also derived in this case. However, it is concluded that both AVMs predict two admittances, Ydd(s) and Yqd(s), very precisely even beyond the switching frequency. On the other hand, the prediction of the other two admittances, Ydq(s) and $Y_{qq}(s)$, is accurate only up to one fourth and one half of the switching frequency, respectively. The main sources of differences are found to be the sideband resonant points that are mainly present in the response to a q-channel injection. The main reason is that the q-channel injection modulates the commutation angle and yields significant sideband admittances around multiples of the switching frequency, which is typical behavior for nonlinear systems.

Furthermore, a hardware set-up is built, measured and modeled, showing that the switching simulation model captures nonlinear sideband effects accurately. In the end, a six-pulse diode rectifier feeding a constant power load is analyzed with the modified AAVM and through the detailed simulations of the switching model, proving the effectiveness of the proposed modifications. The nonlinear sideband admittances are an inevitable phenomenon in a six-pulse diode rectifier as sidebands are found in all test-cases. Through the detailed analysis, it is found that both AVMs are simplifications of the switching model and both models fail to predict the complete small-signal dq admittance characteristic of the six-pulse diode rectifiers, especially in the frequency range beyond the switching frequency (360 Hz). This paper analyzes the new effect: sideband admittances around multiples of switching frequency, which was not previously observed in the six-pulse diode rectifiers but has contributed to the nonlinear behavior of the di-ode rectifier. The new phenomenon is captured both in hardware measurements and in the switching simulation model.

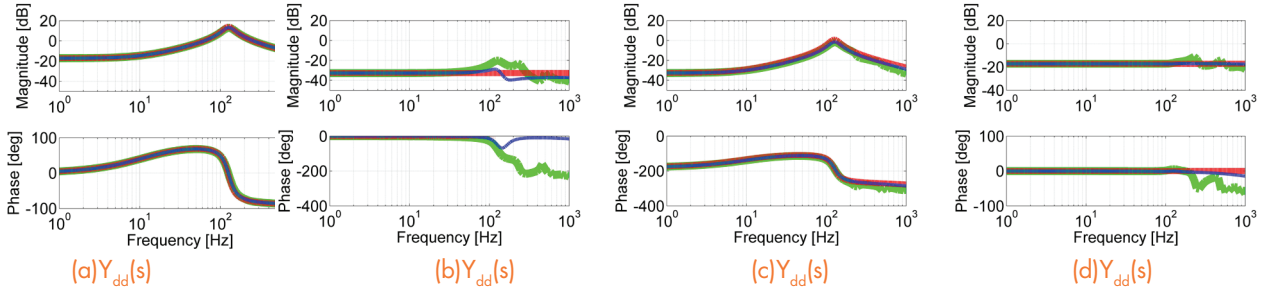


Fig. 1. Input dq admittance of six-pulse diode rectifier (AAVM red line, PAVM blue line, switching simulation model green line)

Influence of Phase-Locked Loop on Input Admittance of Three-Phase Voltage Source Converters

This paper studies the impact of Phase-Locked Loop (PLL) on the input admittance of a three-phase Voltage-Source-Converter (VSC). Two dq domains are defined to analyze the impact of PLL. One is the system dq domain that uses the ac source angle to transform from the abc frame to the dq frame. The other one is the converter dq domain. Converter senses ac source voltage and uses PLL to track the angle of the ac source. The output angle of PLL is used for dq transformation inside the converter. Fig. 1 shows the two dq domains and how perturbation on the ac source voltage propagates to the PLL output angle. From here it moves further to the sys-tem abc domain duty ratio and then to the VSC input current in the system dq domain. Fig. 1 indi-cates that PLL is a bridge that the VSC input voltage perturbation can pass through so that it can introduce perturbation on the input current. The PLL dynamic will then influence the VSC input admittance. To make the analysis of VSC input admittance simple, the transfer function matrices flow chart shown in Fig. 2 is developed to represent the small-signal model of the circuit shown in Fig. 1. Fig. 3 shows the effect of the current loop and the PLL on the VSC input admittance. Clearly, the resonance shown by the open loop admittance is smoothed out by the current loop controller. PLL only affects Y_{dq} and Y_{qq} elements. Changes in the PLL bandwidth only influence the VSC admittance on its Y_{dq} and Y_{qq} elements, where a faster PLL will yield lower admittances within its bandwidth. The same conclusion still holds when the voltage control loop is closed. Possible instability can happen when different PLL designs are used. In the paper, results for admittances of different PLL designs with current and voltage loop control are shown. Stable and unstable cases caused by PLL are also discussed.

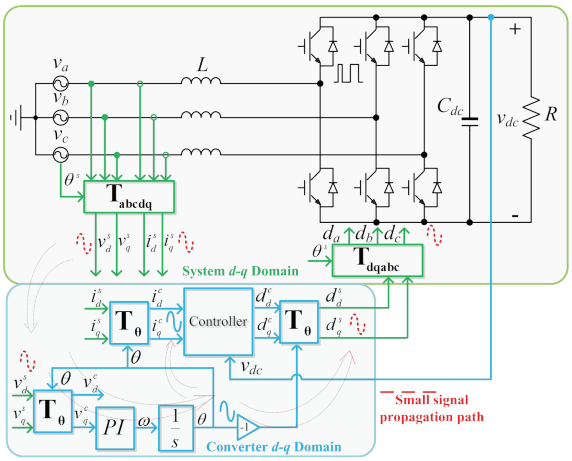


Fig. 1. Influence of PLL on VSC input admittance

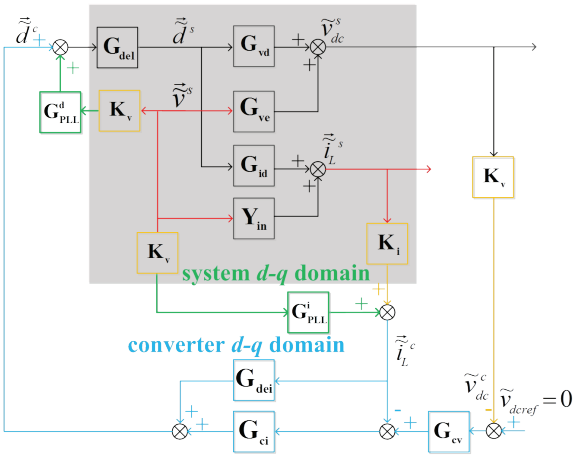


Fig. 2. Transfer function matrix flow chart representation of VSC small signal model including PLL and current feedback control

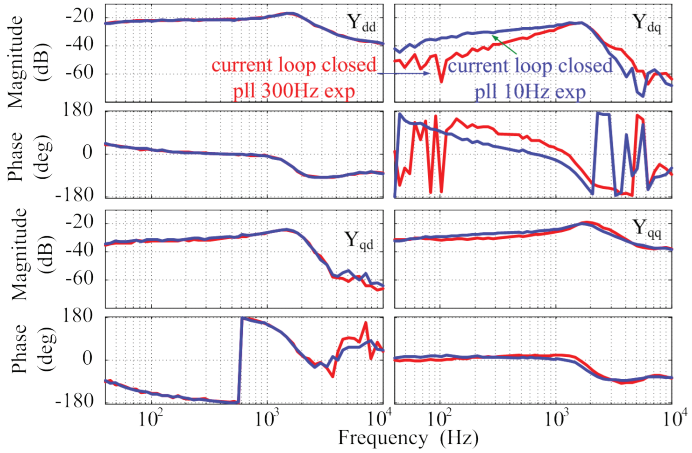


Fig. 3. Experimental results of VSC input admittance with different PLL bandwidth with current feedback control

Small-Signal Analysis and Design of Constant Frequency V² Peak Control

Constant frequency V² peak control is widely researched in literature and used in industry in DC-DC converters due to its simple implementation and fast transient response. However, the effect of the capacitor voltage feedback needs to be clarified for design purposes. This nugget analyzes the small-signal model for constant frequency V² peak control. There are two pairs of double poles located at ½ f_{sw} in this control structure because of two kinds of feedback information. First, the sidebands of the inductor current information cause a sample-and-hold effect resulting in one pair of double poles located at ½ $f_{sw.}$ Next, the sidebands of the capacitor voltage information cause another pair of double poles located also at ½ f_{sw}. The Instability issue occurs not only in a large duty cycle case, but also in the case with small capacitor time constants.

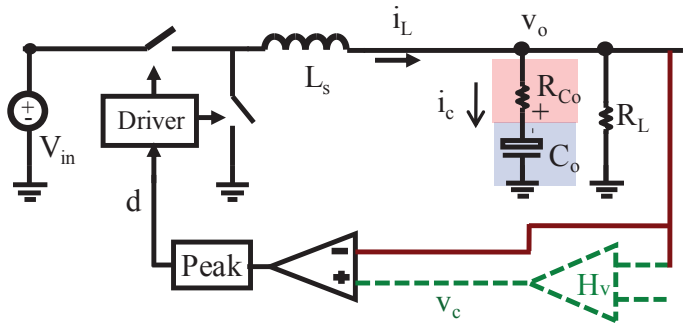


Fig. 1. Constant Frequency V² Peak Control

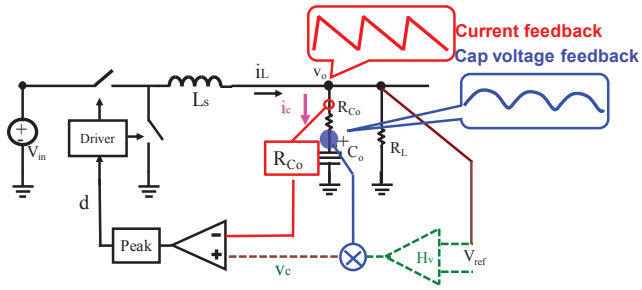


Fig. 2. Separation of Feedback Infomation

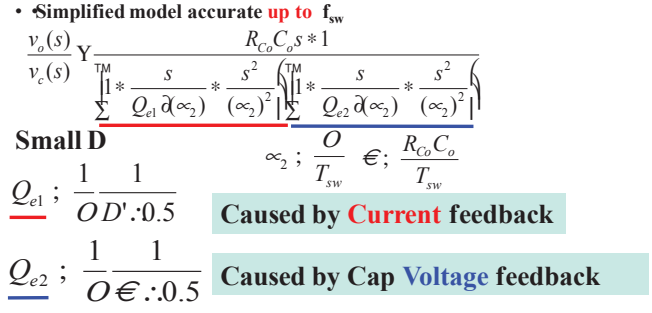


Fig. 3. Two pairs of double poles caused by current and cap voltage feedback

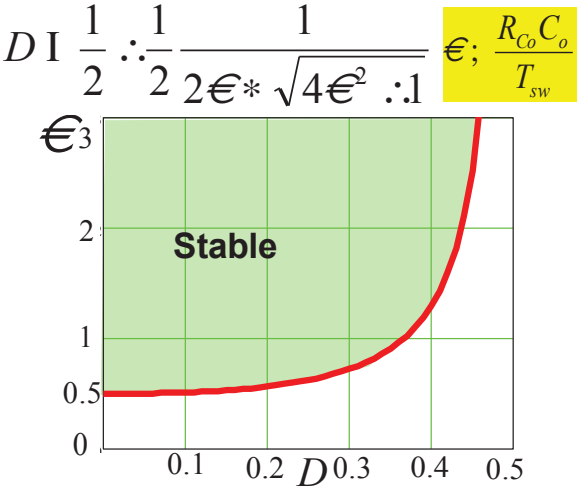


Fig. 4. Stability Criterion

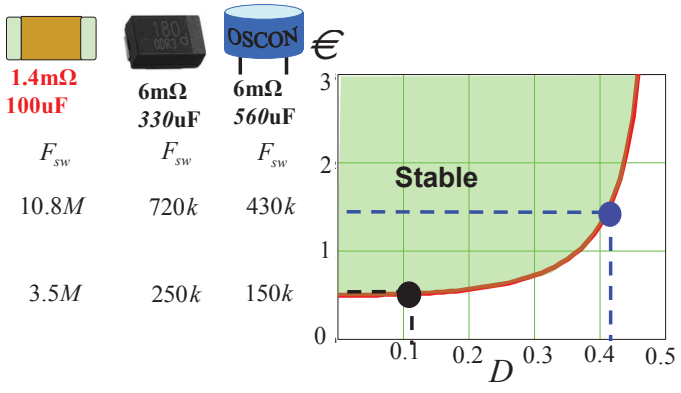


Fig. 5. Design Considerations for different types of capacitors.

Small-Signal Analysis and Design of Constant Frequency V² Peak Control

To solve the instability issue which occurs either in the large duty cycle case or with the small capacitor time constant case, two types of compensations (either by adding an external ramp or a current ramp) are adopted. However, the effects of the external ramp and current ramp need to be further clarified for design purposes to obtain a well-damped dynamic performance. By examining the small-signal model with ramp compensations, design guidelines for the ramp compensations are proposed. It is found that the external ramp is good enough to get a well-damped performance when feedback strength is strong (for example, when employing OSCON caps). However, a current ramp is necessary to achieve a good dynamic performance when feedback strength is weak (for example, when employing Ceramic caps).

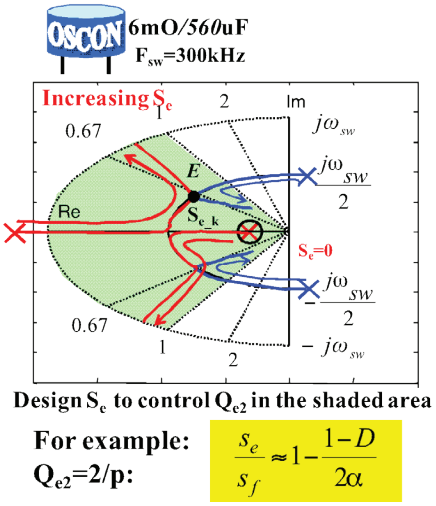


Fig. 3. Design Guideline for External Ramp with OSCON Cap

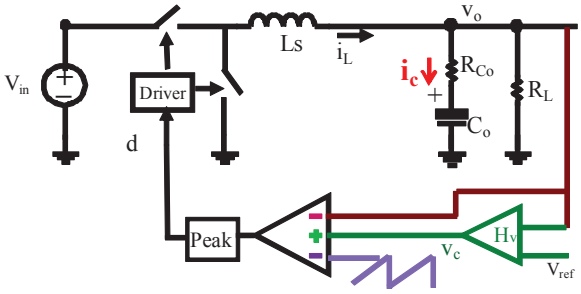


Fig. 1. Constant Frequency V2 Peak Control with External Ramp

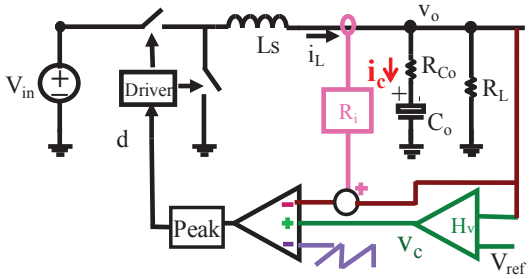


Fig. 4. Hybrid Ramp Compensation for Ceramic Cap

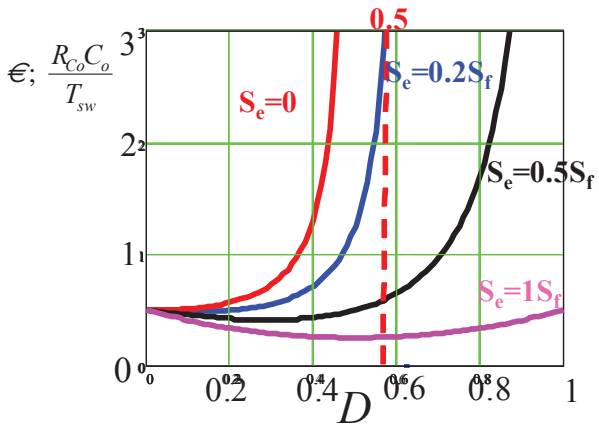


Fig. 2. Stability criterion with external ramp

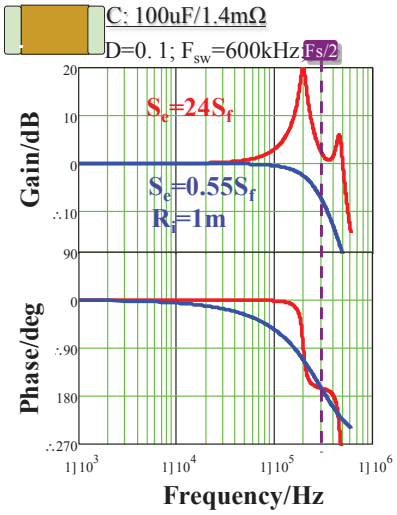


Fig. 5. Performance Comparison for Ceramic Cap with Hybrid Ramp and External Ramp

I² Average Current Mode Control for Switching Converters

The constant frequency average current mode control is a widely used control scheme for the converters requiring precise current control, but its transient response is relatively slow, while the switching loss and driving loss significantly diminish the light load efficiency. To solve these issues, the I² control average current mode is proposed. By combining the fast direct current feedback and integral feedback, the I² control achieves both high bandwidth and accurate current control. As a particular embodiment of this concept, by adopting constant on-time modulation, constant on-time I² control needs no artificial ramp, and has fast dynamic response. Moreover, due to the decrease in the switching frequency, constant on-time I² control improves the efficiency in discontinuous-conduction-mode. The concept of I² control can be extended to other modulations. A small signal model using a describing function based an equivalent circuit model is proposed. The model is accurate up to 1/2 switching frequency. Based on the model, the design guidelines are discussed.

Fig.1 shows the proposed I² average current mode control structure. The current loop consists of a fast direct feedback loop and a slow integral feedback loop. The integration provides a dynamic offset between v_c and v_{ci} to eliminate a low frequency control error. Voltage loop is the outer loop for voltage regulation. As the current information is used twice in control loop, following the name V² control, the proposed control is named as I² control.

The I² control can achieve fast and accurate current control, without requiring an external ramp. In CCM, as on-time is fixed, the switching frequency f_{sw} of I² control is independent on the inductor value. When the average current is below half of the inductor current ripple, the circuit operates in discontinuous-conduction-mode (DCM). In DCM, the synchronized rectifier is turned off when the inductor current reverses to minimize efficiency loss due to reverse current flow and gate charge switching.

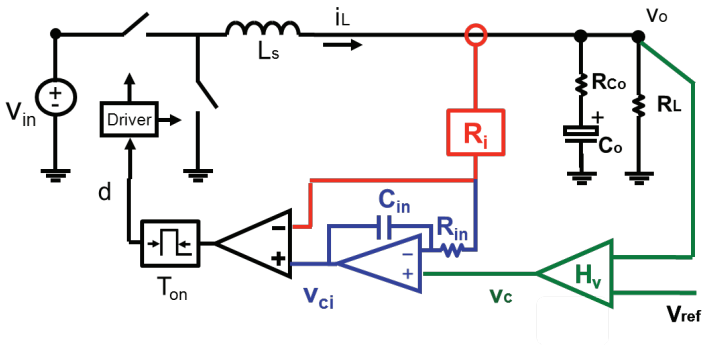


Fig.1 Proposed I² average current mode control

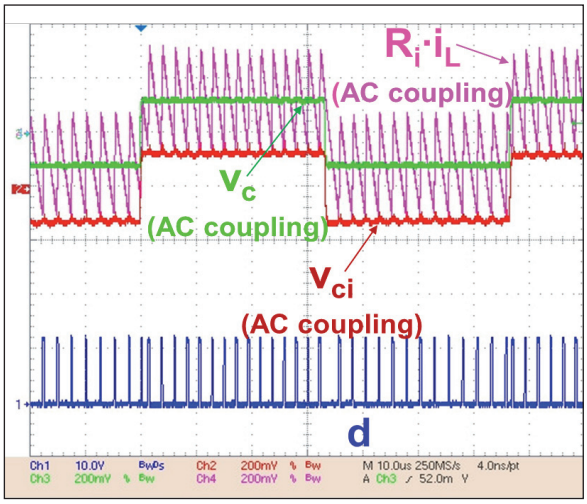


Fig.2 Transient Response of I² control in CCM

Small Signal Analysis and Design of Active Droop Control Using Current Mode Equivalent Circuit Model

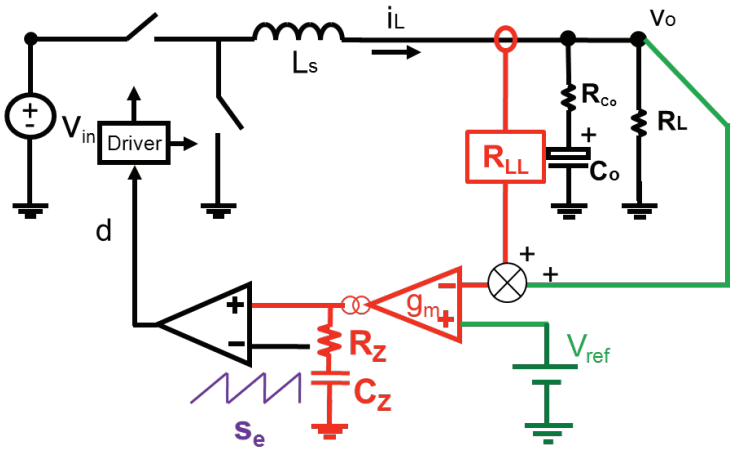


Figure 1. Buck converter with active droop control

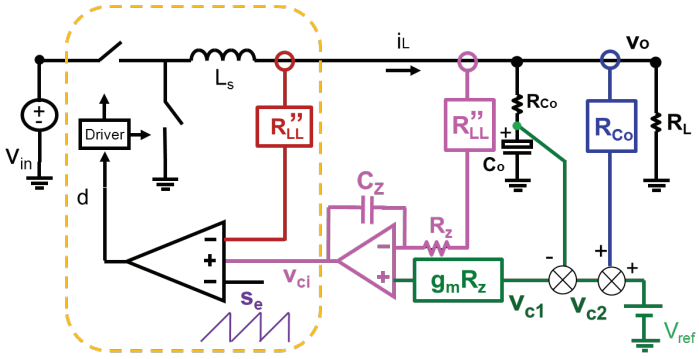


Figure 2. Small signal equivalent circuit for active droop control with ESR dominant output capacitor

Active droop control is widely used in Voltage Regulators for microprocessing. Since a summed signal of the inductor current and the output voltage is fed back, the active droop control is interpreted as a special implementation of current mode control. However, in the conventional small signal model, the nonlinearity of the current feedback is not taken into consideration. Moreover, for the VR with an OSCON capacitor, the output voltage triangle ripple is comparable with the inductor current ripple, because the ESR is designed to be equal to the droop resistance R_{LL}. The output voltage switching ripple is also ignored in the conventional model. In terms of feedback design, the conventional model does not provide any clue about the optimization of the artificial ramp in the PWM modulator. As a result, many commercial controllers actually apply excessive ramp, which results in the complication of the compensator. This paper proposes a small signal equivalent circuit model for active droop control. The equivalent circuit is different for the case using the OSCON capacitor and the ceramic capacitor as an output capacitor. The design guidelines of the compensator and external ramp are proposed. The proposed design guideline can accurately evaluate the high frequency small signal performance, simplify the compensation, maximize the bandwidth and reduce the output capacitor numbers.

Active droop control is essentially an average current mode control with proportional voltage feedback. The voltage feedback DC gain is also a finite gain.

Analysis of Phase Locked Loop (PLL) Influence on DQ Impedance Measurement win Three-phase AC Systems

AC small signal stability of three-phase systems can be analyzed using the load and source impedances in the d-q synchronous reference frame and many solutions have been recently proposed to measure d-q impedances. One fundamental part of the measurement system is the Phase-Looked Loop (PLL), which tracks the supply voltage phase in order to transform voltage and current terms from abc to dq coordinates. This paper analyzes the influence of PLL dynamics on the accuracy of the impedance measurement results, focusing on two errors: 1) on the generation of voltage/current perturbation, 2) on the measured voltage and current components used for impedance extraction.

Figure 1 explains the PLL's role in the measurement path. The analysis shows that it changes the measured voltage and current spectrum, thus changing the impedance result. For this reason, the PLL bandwidth in existing systems is much smaller than the lowest frequency of the measured impedance, strongly increasing the measurement time. However, the effect can be compensated offline using:

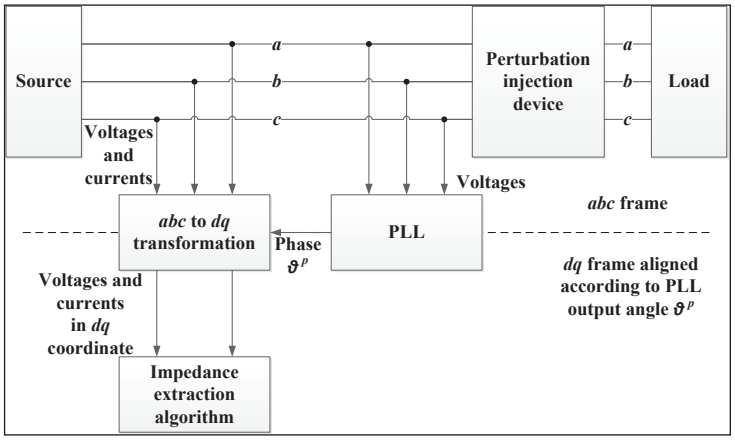


Figure 1. Impedance measurement setup of three-phase systems represented in *abc* coordinates

$$\boldsymbol{Z}^{s}_{dq}(s) = \left(\boldsymbol{Z}^{p}_{dq}(s)^{-1} \cdot \begin{bmatrix} 1 & V^{s}_{q0} H_{PLL}(s) \\ 0 & 1 - V^{s}_{d0} H_{PLL}(s) \end{bmatrix} - \begin{bmatrix} 0 & I^{s}_{q0} H_{PLL}(s) \\ 0 & -I^{s}_{d0} H_{PLL}(s) \end{bmatrix} \right)^{-1}$$

where $Z^{5}_{dq}(s)$ is the correct system impedance, $Z^{5}_{dq}(s)$ is the measured impedance, $H_{PLL}(s)$ is the transfer function of PLL, and all the variables with 0 in subscription are steady state value of the variables. Figure 2 demonstrates the compensation result. It can be seen that the PLL causes a huge error on the measurement of impedance of a diode rectifier. But the compensation can correct the result back to very close to the real impedance. The offline compensation enables a higher PLL bandwidth and a significantly faster measurement system.

PLL's effect on perturbation injection is also analyzed in the paper. It has no influence on the perturbation if no DC component is injected. Therefore, the bandwidth of the injection PLL does not affect the measurement.

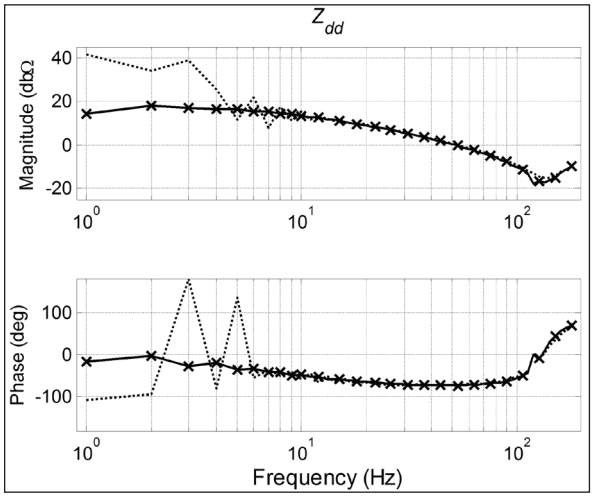


Figure 2. Impedace correction sample Extracted dio-de-rectifier impedances (Solid line: no PLL; dotted line: 50 Hz bandwidth; 'x' markers: result back calculated from 50 Hz result)

Design and Implementation of Three-phase AC Impedance Measurement Unit (IMU) with Series and Shunt Injection

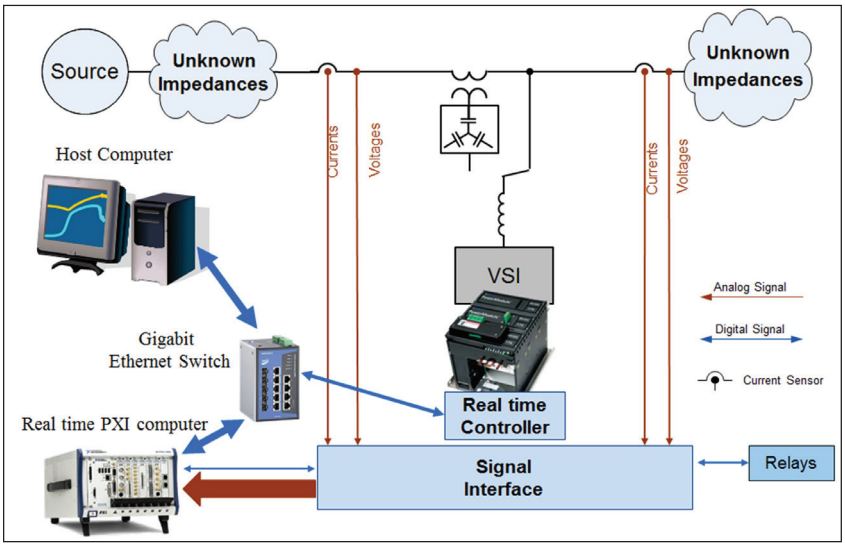


Figure 1. Impedance measurement system function block diagram

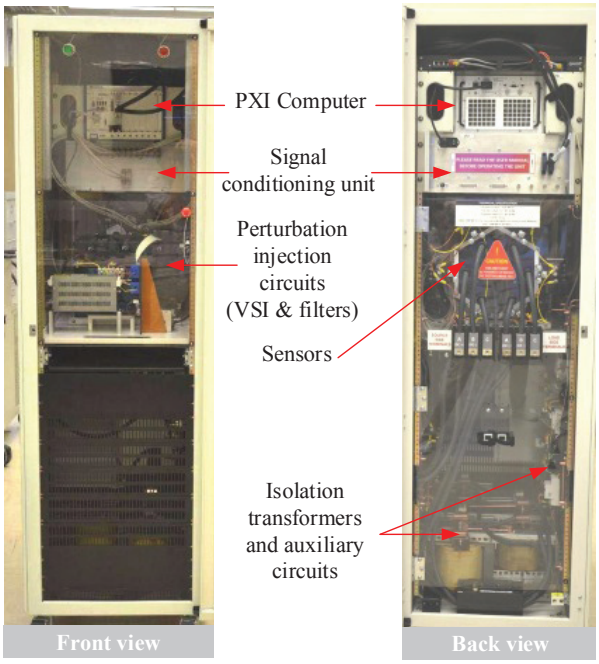


Figure 2. Front and Back view of the IMU

Measurement of the source and load impedances is needed to assess small-signal stability in the electrical power system based on power electronics converters. This paper presents the design and implementation of an Impedance Measurement Unit (IMU) based on the dq reference frame impedances suitable for load power up to 100 kW.

The most critical issue is to increase the SNR without increasing the IMU injection level. SNR is improved by using:

1) both shunt and series injection modes to improve the perturbation distribution between source and load and to enhance the response signal SNR;

2) analog filtering and oversampling to increase the resolution of the AD conversion;

3) correlation between the reference of injected signal and the measured perturbation to reduce the uncorrelated noise present in the measurement system.

Figure 1 illustrates the function that blocks the IMU. It uses a voltage source inverter to create perturbation, a PXI computer for sampling and real time signal processing, and a PC for data offline processing to get the final impedance result. The assembled hardware is shown in Figure 2.

The performance of the designed measurement unit is tested with a low-output-impedance source. Both linear and nonlinear loads are measured and the results show good matching with the theoretical and simulation values. The proposed IMU is also scalable to higher power applications and it is an important instrument to investigate stability in electrical power system applications as in microgrid, aerospace, naval and transportation applications.

Three-phase AC System Impedance Measurement Unit (IMU) using Chirp Signal Injection

Power electronics technology has infiltrated the power processing and generation fields in contemporary electric power systems. Power electronic technology provides exceptional performance the negative incremental impedance characteristics of the converters introduces the possibility of system instability. Similar to DC power systems, the stability in balanced three-phase AC systems can be analyzed using the output and input impedances at the interface in the synchronous d-q coordinates. Within this scenario, there is a need to fully characterize the impedances of the various AC interfaces in electrical power systems.

The frequency sweep method widely used in literature takes a long time to extract the whole impedance curve, especially at low frequency range. This paper proposes using a chirp signal, which is one kind of wide bandwidth signal, to increase the measurement speed.

Figure 1 shows an example of chirp signal. Compared to other wide bandwidth signals, it has a low crest factor and a controlled spectrum shape.

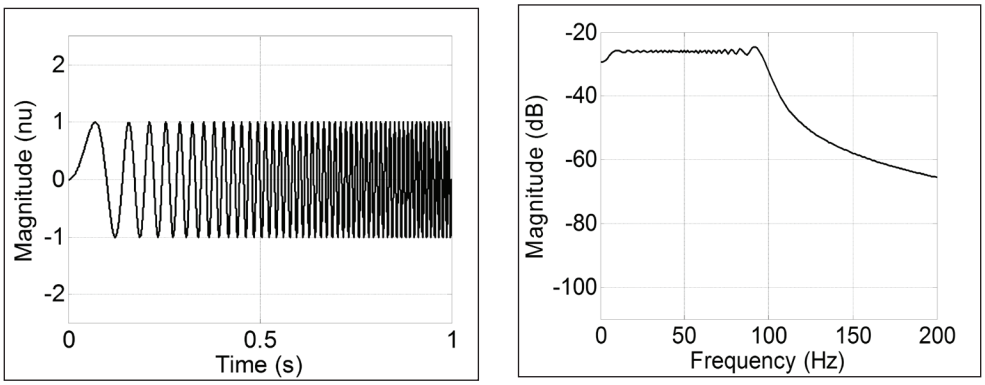


Figure 1. Chirp signal example

As a wide bandwidth signal, the chirp signal spreads the energy over a frequency range, which results in a lower SNR compared to the sinusoidal signal used in a frequency sweep. A corresponding data procedure used with the chirp signal is developed. It includes oversampling the raw signals to increase the analog-to-digital conversion resolution, cross correlation to remove the non-correlated noise, and frequency domain averaging to further improve the signal SNR. The method is tested with both linear and nonlinear load. Figure 2 shows the measurement result of a diode rectifier when compared to the simulation result, which is extracted using a frequency sweep method. The two results show a good match.

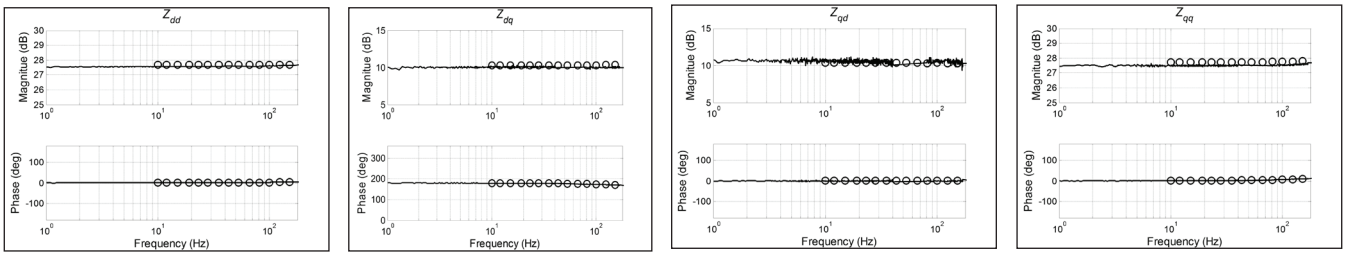


Figure 2. Input impedance of a diode rectifier
(Solid line: measurement result; circles: simulation result)

Grid-Synchronization Modeling and Its Stability Analysis for Multi-Paralleled Three-Phase Inverter Systems

The issue of synchronization instability and the corresponding low-frequency power oscillation phenomenon between synchronous generators is already found in electric power systems and addressed by various solutions. However, the grid-synchronization behaviors and the potential instabilities between multi-paralleled power electronic inverters is not well-understood due to the different synchronization mechanisms.

CPES researchers present a set of small-signal modeling methodologies to predict the low-frequency behaviors of the grid-synchronization loops in multi-paralleled inverter systems. The proposed model can predict the low-frequency unstable oscillation in large-penetrated renewable-energy systems as well as assess the effectiveness of frequency-based islanding-detection under multi-paralleled inverter conditions.

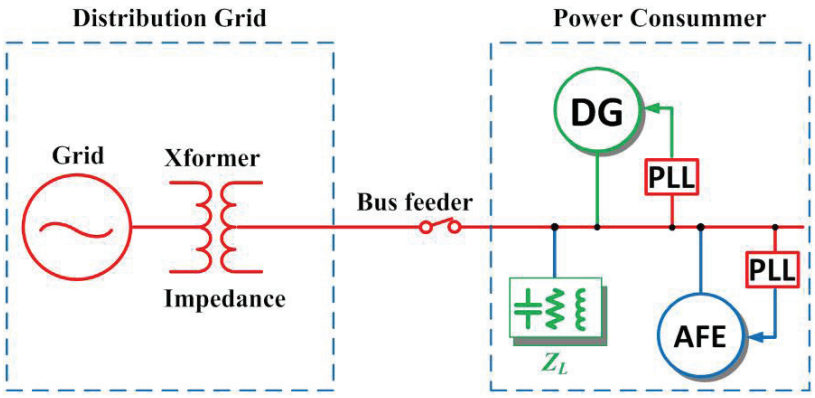


Fig. 1 multi-paralleled power electronic converter system

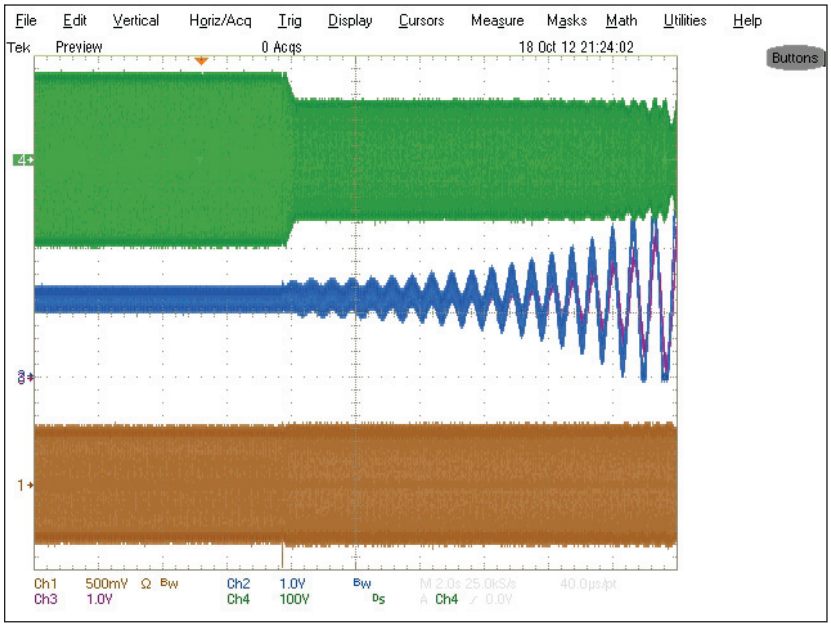
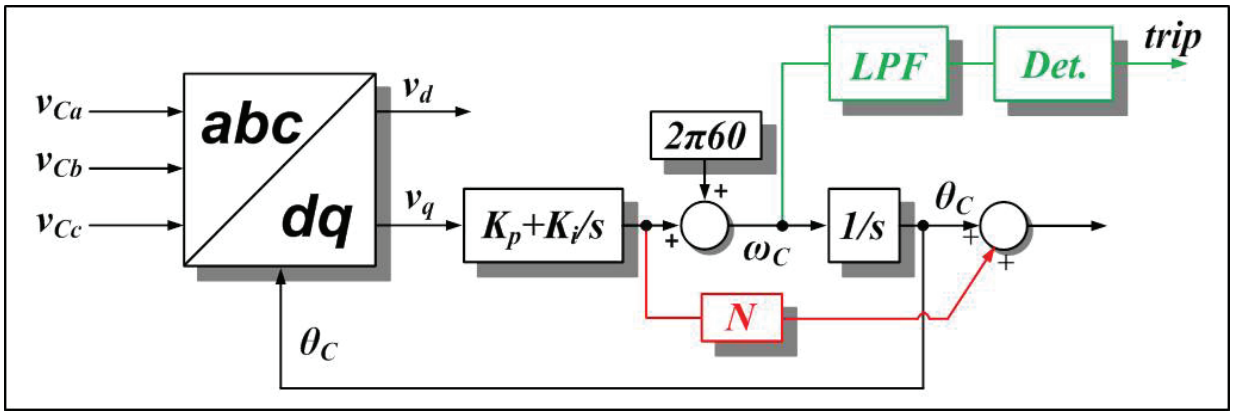


Fig. 2. Experimental test result showing the unstable PLL output: V_{ga} [100 V/DIV], $i_{C1}a$ [10 A/DIV], W_{C1} ωW_{C2} [0.05 Hz/DIV].

Anti-Islanding Protection in Three-Phase Converters using Grid Synchronization Small-Signal Stability

It is required in IEEE Std. 929-2000 and 1547-2003 that the distributed generation unit below 10 MW rating, such as solar inverters, has to effectively detect the islanding condition. CPES researchers present the islanding detection algorithms for three-phase grid-interface converters based on the grid synchronization small-signal stability. To study the grid synchronization behavior at the islanding condition, a low-frequency small-signal phase-locked loop (PLL) model is proposed by considering the converter interaction with the system impedances. Many of the frequency-related behaviors are explained and the crucial system parameters which impact the PLL stability are quantified by the proposed model as well. Based on the model, new islanding detection algorithms based on the small-signal stability theory are proposed to effectively detect the islanding event under the worst loading conditions. The proposed algorithms feature a small impact to the converter system operation as well as an easy implementation.



Proposed modified PLL system with small-signal feedback

Fig. 1 the proposed islanding detection method

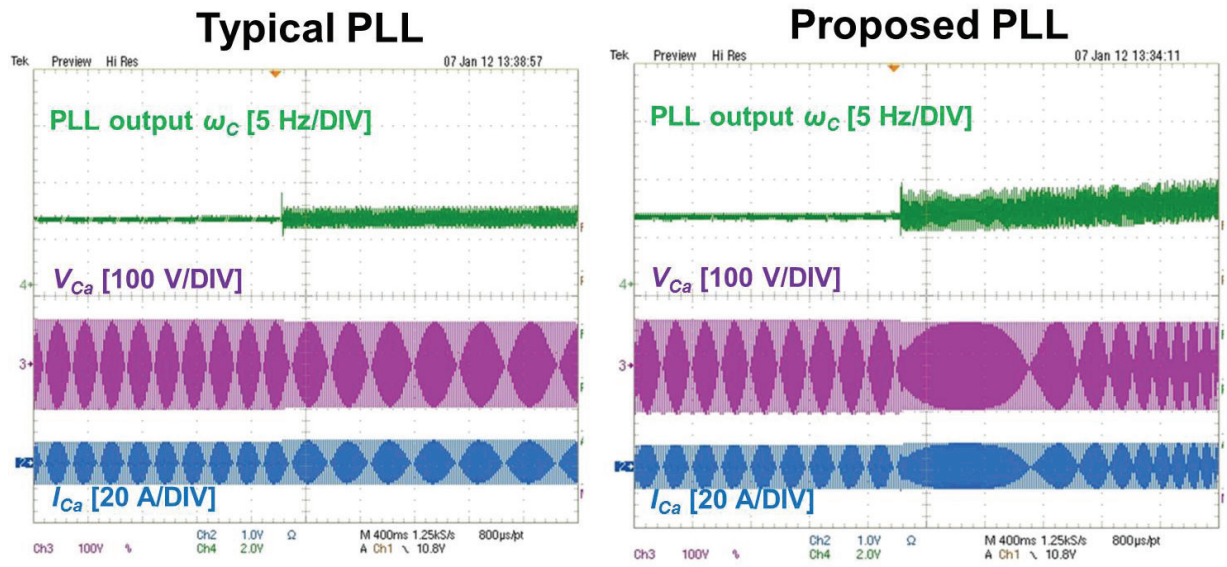


Fig. 2. Experimental test result showing the typical PLL output (left) and modified PLL output when islanding event occurs.

A Droop Controller is intrinsically a Phase-Locked Loop

In order to address the energy and sustainability issues being faced worldwide nowadays, more and more renewable energy sources are being connected to power systems, often via DC/AC converters (also called inverters). These inverters are required to synchronize with a connected system. Another important requirement for these inverters is that they should take part in the regulation of system frequency and volt-age, in particular, when the penetration of renewable energy exceeds a certain level.

There are many ways to synchronise an inverter with the grid but the most commonly adopted strate-gies are based on phase-locked loops. A basic phase-locked loop (PLL) adopts a control loop to track the phase of an input signal. It can often provide the frequency information of the signal as well, but normally without the information of the voltage amplitude. Also, in order to obtain the amplitude information of the input signal, the enhanced PLL (EPLL) shown in Fig. 1 can be adopted.

What is fundamental to the operation and regulation of the frequency and voltage of a power system is the so-called droop control strategy. It was originally adopted to operate synchronous generators and has recently been adopted to operate inverters connected in parallel. The generators and/or inverters change the reactive power and real power output according to the system voltage and frequency. The conventional droop control strategy is often regarded as a static control law. It actually includes an integral effect in each channel. After some manipulations, the droop controller can be drawn in an equivalent form shown in Fig. 2 (for the case with resistive impedance). The filter H(s) is a hold filter so it does not cause any major dif-ference.

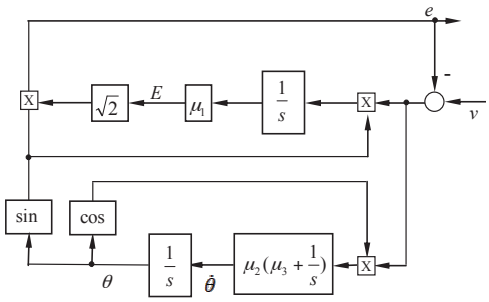


Fig. 1. Enhanced phase-locked loop (EPLL)

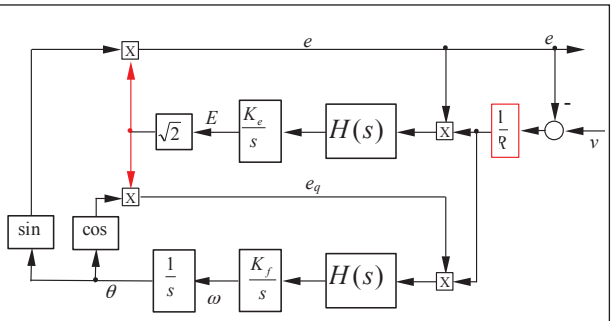


Fig.2. Droop control for systems with resistive impedance

Fig. 1. Enhanced phase-locked loop (EPLL)

Fig.2. Droop control for systems with resistive impedance

Comparing these two figures, it can be seen that they are more or less the same. In other words, a droop controller is intrinsically an (enhanced) phase-locked loop. Both figures have two channels: a fre-quency channel and a voltage channel. When the voltage channels are ignored, what is left in Fig.2 is the frequency droop control and what is left in Fig. 1 is a basic PLL. This means the frequency droop control is intrinsically a basic phase-locked loop.

What is discovered in this study opens up several lines for future research: (1) PLLs can be improved by adopting what is done to droop control strategies; (2) Droop control strategies can be improved via look-ing at the vast literature of PLLs; (3) It is a challenge to analyze the stability of systems with more than one droop controller. What is done in the PLL community about the stability of PLLs can be borrowed; (4) A dynamic droop controller can be designed to improve the performance of droop control.

Small-Signal Impedance Identification of Three-phase diode rectifier with multi-tone injection

AC and DC impedances of power converters are used for stability analysis of modern power systems at AC and DC interfaces. The basic idea for impedance extraction is an ac sweep approach with a sinusoidal signal injection, here denoted as a single-tone. However, the approach is time consuming because the time-domain simulation runs many times. Therefore the approach of the multi-tone signal injection is implemented so that multiple frequency responses can be measured in only one time-domain simulation. In linear loads, the multi-tone approach can give the same results as a single-tone approach because superposition holds true for the linear system. For three-phase nonlinear loads such as a 6-pulse Diode Bridge Rectifier, different results are observed from the multi-tone and single-tone approach. In this paper an algorithm is implemented to improve the multi-tone approach and avoid result differences. The idea of this algorithm is to adjust every perturbation frequencies to avoid perturbation frequency overlap, which is caused by the commutating behavior of 6-pulse diode bridge rectifier.

The result comparison of a multi-tone and single-tone approach validates the proposed algorithm. With this algorithm, the multi-tone approach could accurately measure the impedance of a 6-pulse diode bridge rectifier in a large frequency range

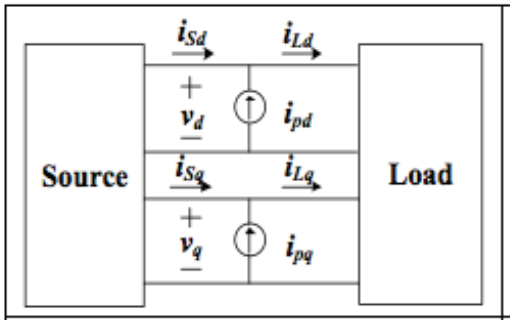


Fig 1. DQ frame impedance measurement

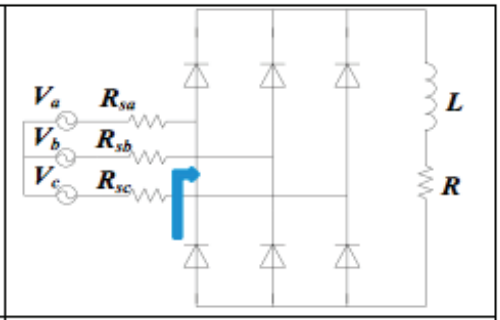


Fig 2. 6-pulse diode bridge rectifier

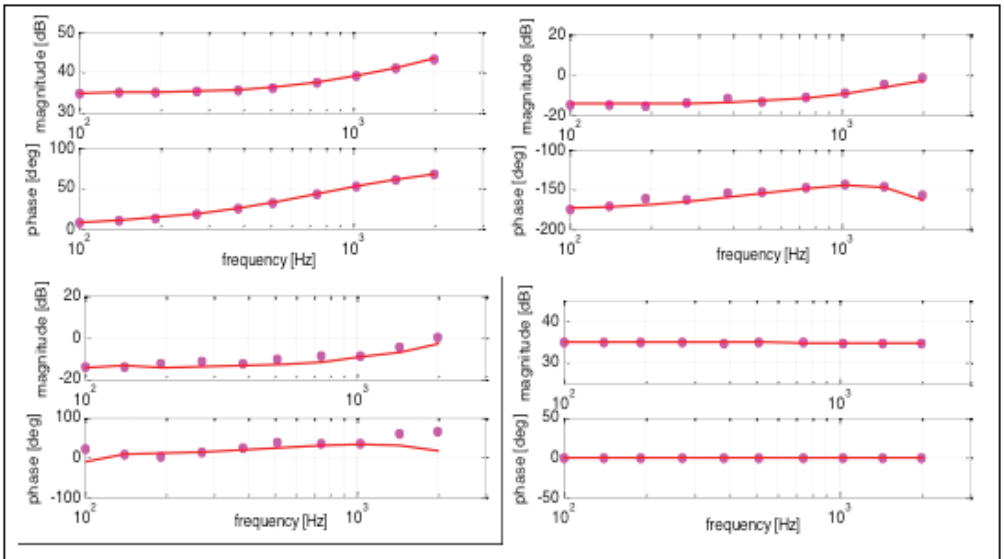


Fig 3. Input impedance result comparison (line:single-tone dot:multi-tone)

Application of multi-tone approach in three-phase AC system impedance measurement

AC and DC impedances of power converters are used for stability analysis of modern power systems at AC and DC interfaces. The basic idea for impedance extraction is an ac sweep approach with a sinusoidal signal injection, here denoted as single-tone. However, the approach is time consuming because the time-domain measurement will run many times. Therefore the approach of a multi-tone signal injection is implemented in which multiple frequency responses can be measured in only one time-domain measurement. A frequency selection algorithm is designed to assure the accuracy of measurement.

Three phase passive loads are measured and the result is compared with the analytical expression. The effectiveness of the multi-tone approach is verified.

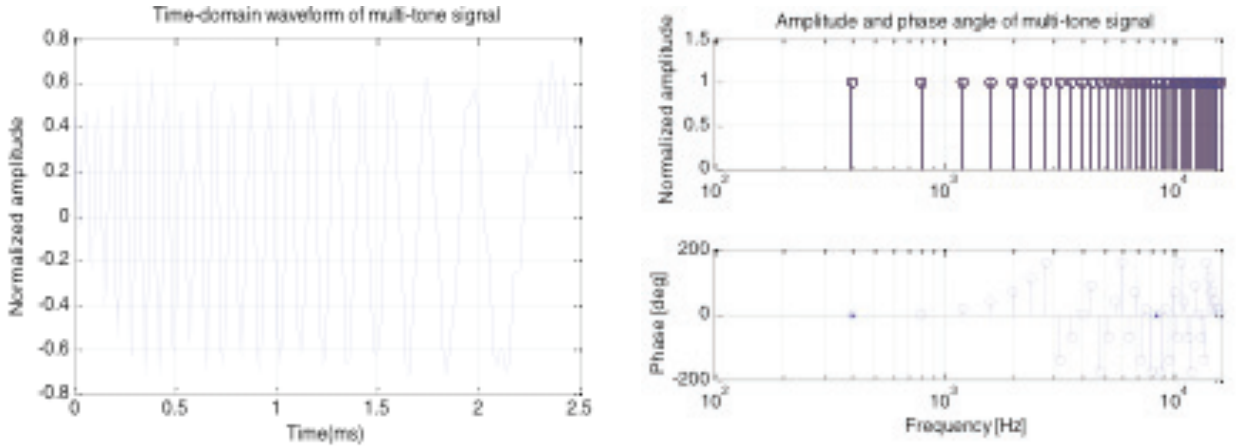


Fig 1. Multi-tone signal example

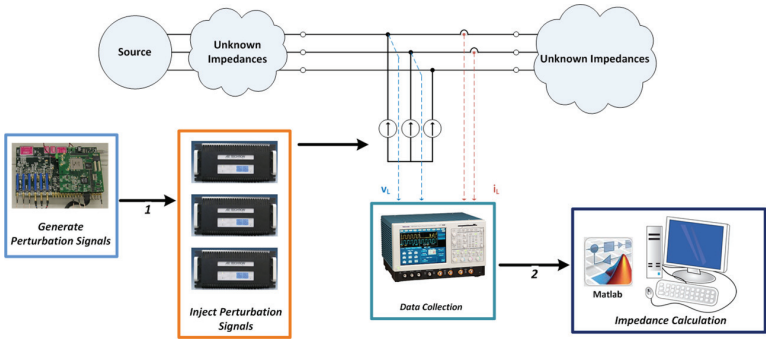


Fig 2. Multi-tone measurement system setup

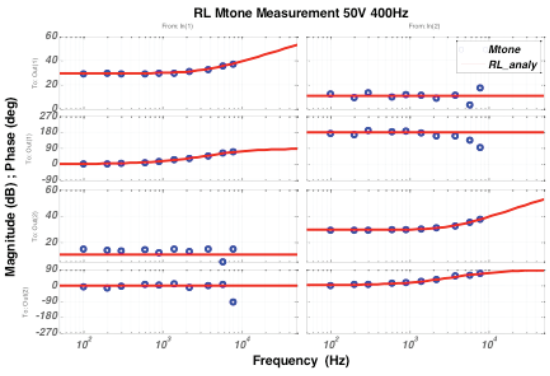


Fig 3. Input impedance result comparison (line:analytical dot:multi-tone)

Matrix Transformer for LLC Resonant Converters

Nowadays, efficiency and power density are two major driving forces in power delivery systems. High switching frequency introduces high power density. However, the switching loss and magnetic related losses are also high. The soft-switching techniques (LLC) and emerging GaN devices give the opportunity to diminish the switching loss. After that, the major loss comes from the transformer.

In Fig. 1, the matrix transformer of a LLC resonant converter is built by four small transform-ers series in primary and parallel in secondary. This transformer helps to reduce leakage induct-ance and winding AC resistance by splitting the secondary side current, while increasing the size and loss of the magnetic cores. To reduce them, two small transformers can merge into one by flu cancellation. However, the winding loss is still high due to the termination loss. Fig. 2 shows one merged transformer winding structure. The SR devices and output capacitors are part of secondary side winding, which can eliminate the AC termination loss and via loss. Based on the FEA simulation results in Fig. 3, the current and magnetic flux distribution are quite even, which means a low AC resistance and leakage inductance. Fig. 4 gives the prototype of the proposed matrix transformer in a 400V/12V, 1kW LLC resonant converter.

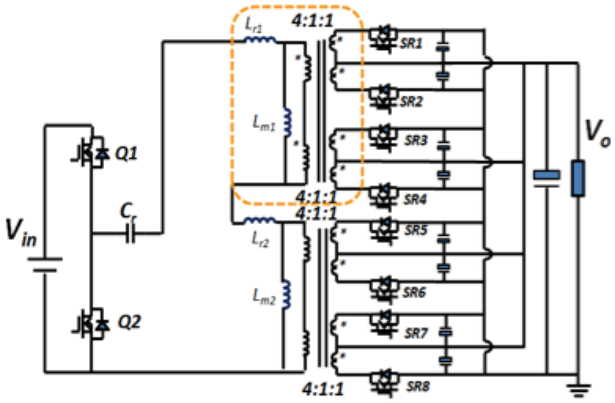
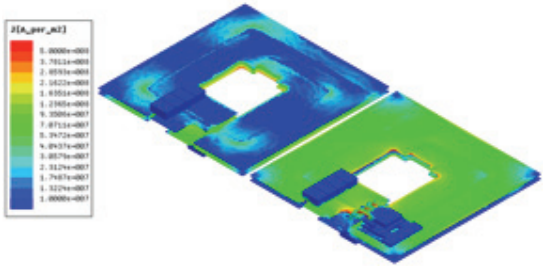
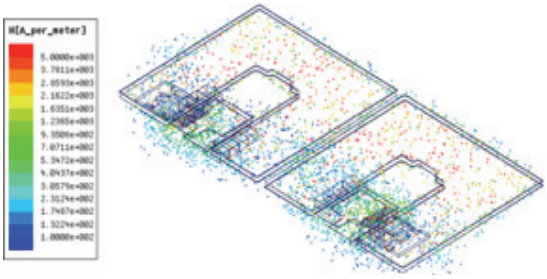


Fig. 1. Proposed LLC Resonant Converter Transformer Structure

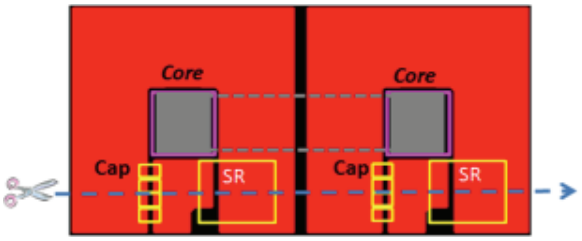


(a) Current Density Distribution

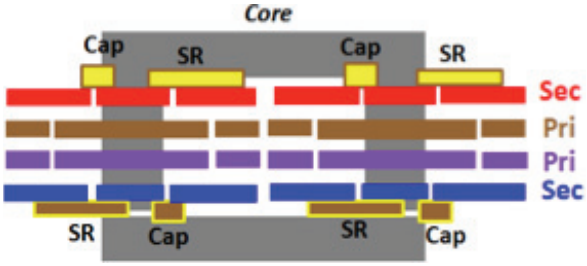


(b) Magnetic Field Intensity Plot

Fig. 3. FEA Simulation results of Proposed Winding Structure



(a) Top view



(b) Cross view

Fig. 2. Proposed Winding Structure

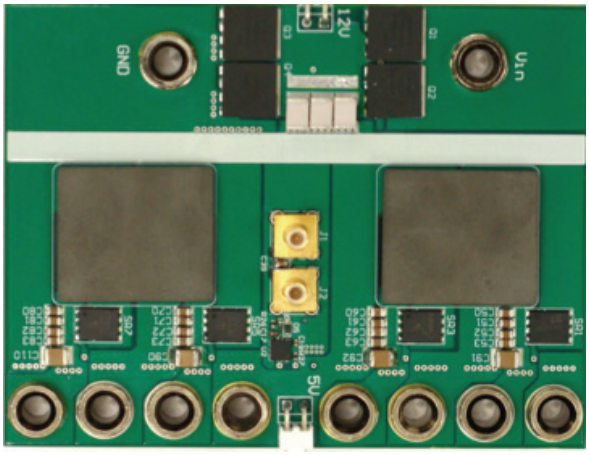


Fig. 4. The prototype of Proposed Matrix Transformer

Transformer Shielding Technique for Common Mode Noise Reduction in Isolated Converters

Isolated converters are widely used in telecom, server systems and point-of-load conversion for portable electronics. These applications must meet the EMI standard. In an isolated converter, the transformer is a main path of the common mode current. Methods to reduce transformer noise have been widely studied. One effective technique is using a shield between the primary and secondary winding. In this paper, the EMI noise transferring path and the EMI model for typical isolated converters are analyzed and the survey about different methods of shielding is discussed. Pros and cons are analyzed. The balance concept is then introduced and our proposed double shielding, which uses a balance concept for the wire winding transformer is raised. Fig. 1 shows a two layer shielding that is added between the primary and secondary windings. However, the shielding is wound and divided into two parts. In one part of the shielding, one layer is connected to A and the other layer is connected to C. In the other part of the shielding, one layer is connected to B and the other layer is connected to D. Hence, through the shielding, CAC and CBD are created, and we can adjust the value of CAC and CBD by changing the wounded position. It can control the parasitic capacitance accurately and is easy to manufacture. Next, a newly proposed single layer shielding for a PCB winding transformer is discussed. The shielding is rotated 180 degree, as shown in Fig.3. On half of the windings, the voltage of the shielding is higher than the secondary winding and there is a current flow from the shielding to the secondary winding. On the other half of the winding, the voltage of secondary winding is higher than the shielding and there is current flow from the secondary winding to the shielding. Although the voltage is not identical between the secondary winding and the shielding, the current is circulating between them. Hence there is no common mode noise current flowing through the transformer. The experiment results are provided to verify the methods.

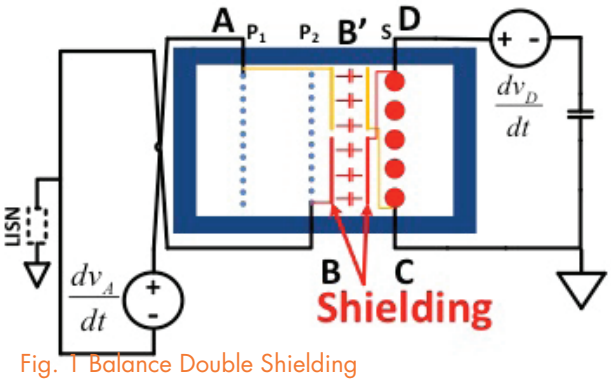


Fig. 1 Balance Double Shielding

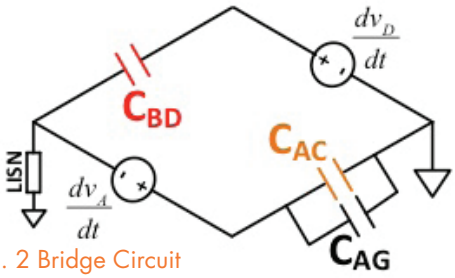


Fig. 2 Bridge Circuit

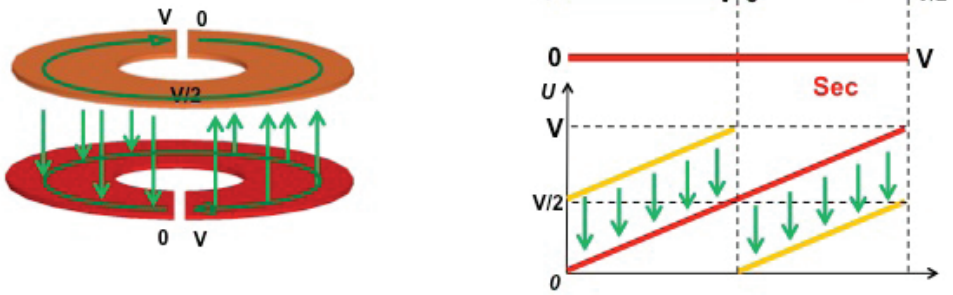


Fig. 3 Single Layer Shielding for PCB Winding

EMI Terminal Modelling of DC-Fed Motor Drives I: Common-Mode Noise

Terminal electromagnetic interference (EMI) models of power converters have been shown to successfully predict conducted emissions of up to at least 30 MHz. For a fixed load, these models can accurately predict the input side of EMI converters for changes in the source impedance. In other words, these models cannot predict the input side EMI for changes in the load side parame-ters. Such terminated EMI models have limited utility as they cannot be used for converters that have a strong coupling between the EMI input and output side. Moreover, in aerospace applica-tions, the conducted EMI standards (DO-160) dictate limits on the noise currents in all power lines and cable bundles, thus compelling development of models that can predict the EMI on both sides of the power converters. The proposed un terminated EMI terminal model in this paper directly predicts the input and output side common mode (CM) noise currents in a motor drive system for changes in both source and load side impedances. Such models can be very useful in understanding how EMI filters and harnesses affect the overall EMI in a motor drive system.

The model is based on the Thevenin equivalent of a three-terminal network and is shown in Fig. 1. The model's impedance matrix is approximated directly using measurements under power-off conditions and then optimized using noise measurements done while the drive is in operation. The noise sources are approximated using in-circuit measurements. The prediction accuracy of the input and output side CM currents when the input LISN impedance is changed from 50 to 1k is shown in Fig. 2. Fig. 3 shows the prediction accuracy with a 50 LISN at the input side and a DM filter at the output. It can be clearly seen that the model can predict both input and output side CM currents up to 30 MHz.

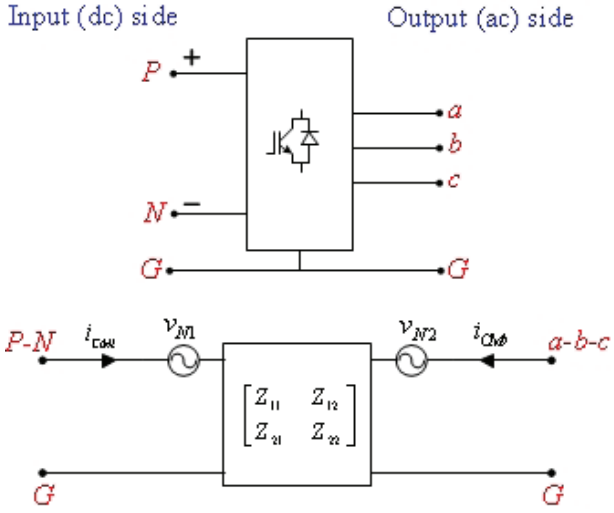


Fig. 1: DM noise models for a motor-drive system

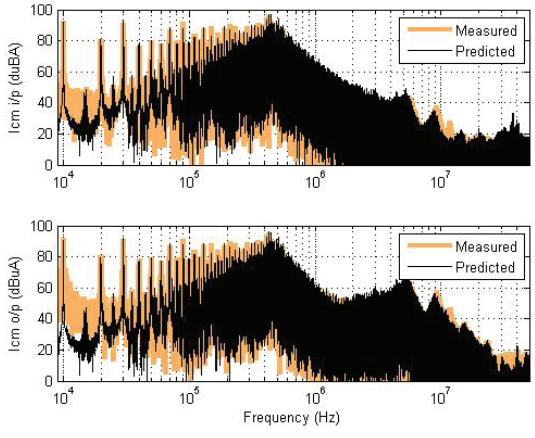


Fig. 2: CM noise prediction for a 1kΩ LISN

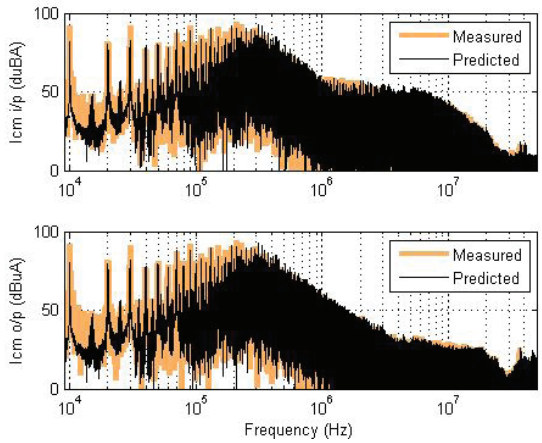
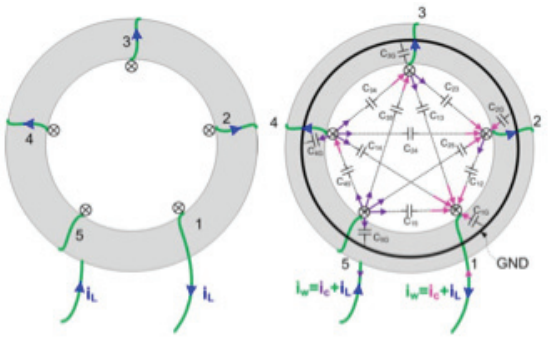


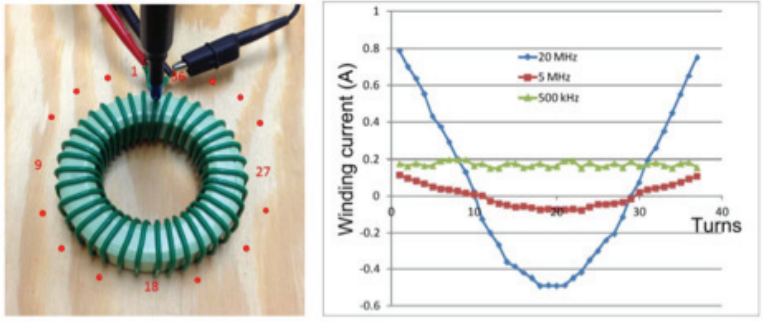
Fig. 3: CM noise prediction for an output side DM filter

Influence of High-Frequency Near-Field Coupling between Magnetic Components on EMI Filter Design

This work presents a detailed analysis of magnetic component coupling and its influence on EMI filter design. In contrast with other literature, the novelty of this paper reveals that magnetic coupling should be divided into two categories: low-frequency coupling and high-frequency coupling. It is proven that coupling is frequency related and high-frequency near-field stray flux distribution can differ dramatically from low frequency condition. The change of the near-field stray flux distribution is caused by displacement current from stray capacitors. By using the Biot-Savart equation, high frequency near-field distribution can be well predicted and matched with experimental results. In addition, single stage DM LC filters are utilized to demonstrate the influence of high-frequency coupling.



(a) Five turns model (b) Equivalent model with stray cap
Fig.1 High frequency near-field stray flux explanation



(a) Measurement setup (b) Measurement results
Fig.2 Winding current distribution measurement

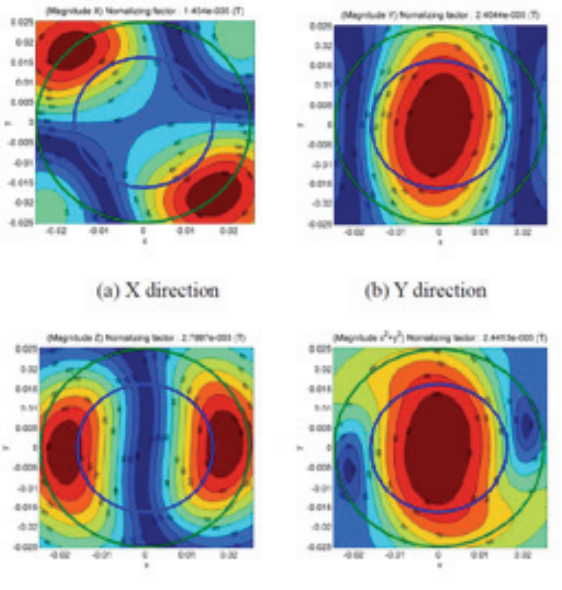


Fig.3 Predicted near-field stray flux for high frequency (20MHz)

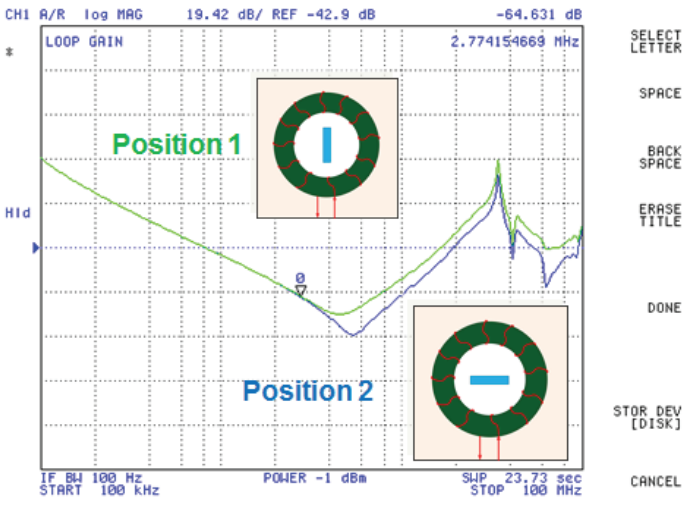


Fig.4 LC filter transfer gain affect by the near field coupling

Impact of Interleaving on EMI Noise Reduction of Paralleled Three Phase Voltage Source Converters

An adjustable-speed motor drive with a voltage-source pulse-width modulation inverter with long cables (shown as Fig.1) brings the EMI issues to the motor drive system [1]. Usually EMI filters are the part of the system that makes both the AC and DC side meet the EMI requirement (such as DO160E standard), which takes a large portion of the system weight. To improve the system power density and reliability, paralleled and interleaved converter topology is commonly used. By phase-shifting the PWM switching cycles of individual converters with an appropriate angle, the total voltage ripple due to PWM switching at the ac terminal can be reduced. Because of the reduction of the ripple voltage, the ac line harmonic current can be reduced. As a result, the use of this PWM technique has the potential to reduce the size of the converters passive components and increase power density.

To study the impact of interleaving on system EMI performance, the equivalent circuit is given as Fig.2, which shows that interleaving will change the noise sources for both CM and DM noise. The impact of interleaving can be predicted using a double Fourier integral analysis and the selection of optimized interleaving angle is related to the system noise propagation path impedance as shown in Fig.3. Both simulation and experimental results prove that by using an optimal interleaving angle the EMI noise can be reduced by 10~12dB in the impedance resonant frequency range, which can reduce the EMI filter size significantly.

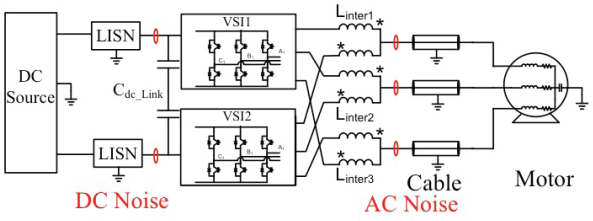
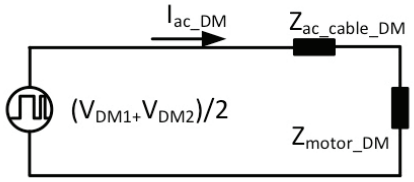
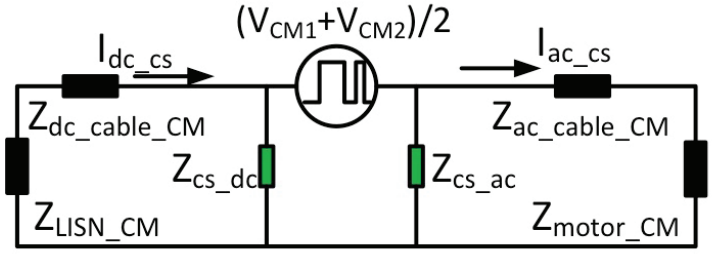


Figure 1: Interleaved 2L VSI DC-fed motor drive system



(a) DM equivalent circuit



(b) CM equivalent circuit

Figure 2: Equivalent circuit for converter output DM and CM noise of dc-fed system with interleaving

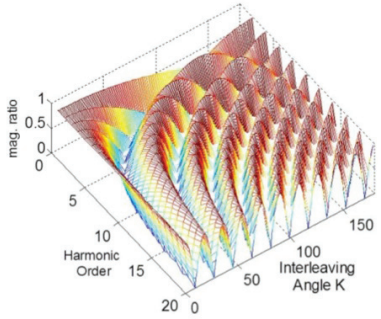


Figure 3:Voltage noise source magnitude reduction on different order harmonics of interleaving with different interleaving angle

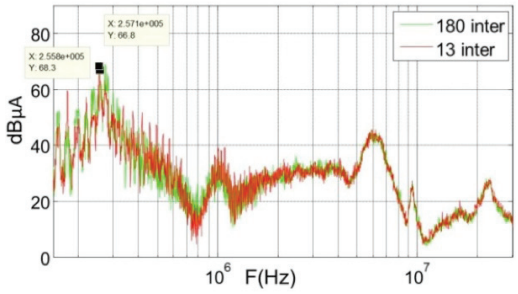


Figure 4: Experimental ACCM noise (180° interleaving: green and 13° interleaving: red)

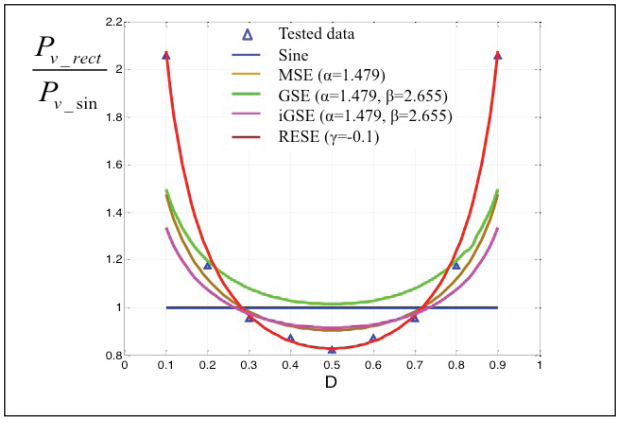
Core loss Model for Rectangular AC Voltages and DC Bias

For most power converters, the voltage waveforms are mostly rectangular or composed of rectangular shapes. The waveform will have an impact on the value of the core loss. And for power inductor, the core will usually be biased by a DC current. The DC bias will affect the core loss. Generally, the core loss will increase by several fold if the bias is strong. An accurate model is necessary in order to predict the core loss under such excitations and assist in the design trade-offs. The most popular core loss models now are the modified Steinmetz equation (MSE), the generalized Steinmetz equation (GSE) and the improved generalized Steinmetz equation (iGSE). However, the measurement data shows these models don't give accurate prediction. A new model is proposed to improve the accuracy for the core loss under rectangular AC voltages and DC bias current by employing a parameter γand DC bias factor, which depends on the material, frequency and temperature. Several ferrite materials are characterized and modeled.

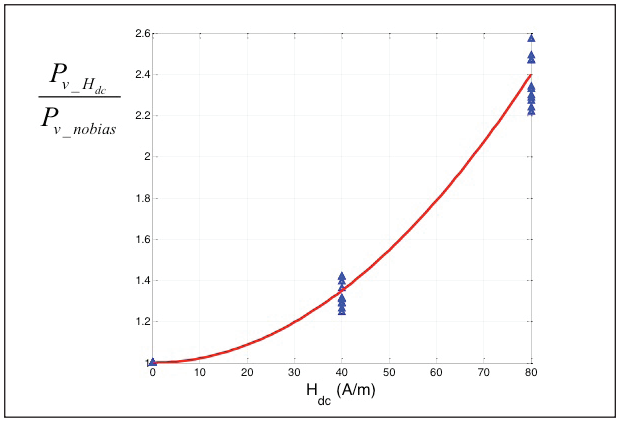
$$P_v \; ; \; SteinmetzEqu.] \; F_{waveform}(D)] \; F_{bias}(H_{dc})$$

$$F_{waveform}(D) \; ; \; \frac{2}{O^2 4^{\prime}[D(1 \therefore D)]^{\prime * 1}}$$

Fdc is curve fitted with measurement



(a) Waveform impact (500kHz, RT)



(b) DC bias factor (500kHz, RT)

Figure 1. Test data and various models of 3F35 MnZn ferrite

High Frequency Isolated Bus Converter with Gallium Nitride Transistors and Integrated Transformer

The trend in isolated DC/DC converters is increasing output power demands and higher operating frequencies. Improved topologies combined with gallium nitride (GaN) transistors can allow for lower loss at higher frequencies. A major barrier to further improvement is the transformer design. With high current levels and high frequency effects the transformers can become the major loss component in the circuit. This paper will study the impact of increased switching frequencies on transformer size, the ability of GaN transistors to increase switching frequency in high frequency resonant topologies, and propose an improved integrated transformer design that can decrease core loss and further improve the performance of traditional matrix transformers. The final demonstration being a Vin=48V, Vo=12V, Io=30A, 1.6MHz GaN converter with an improved integrated transformer offering a power density of 900W/in^3.

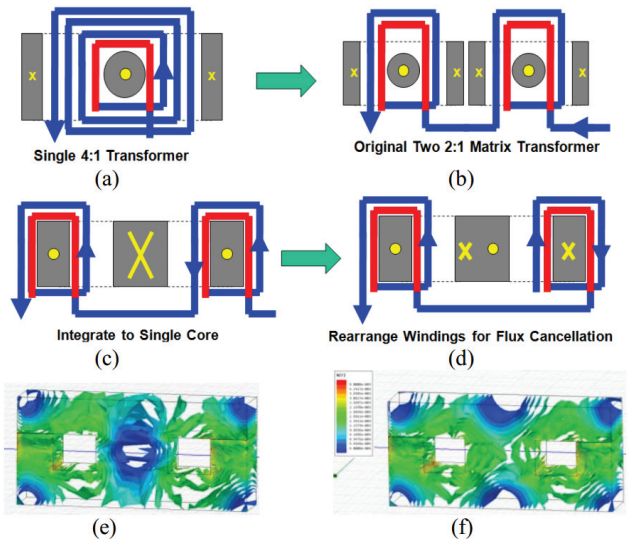


Figure 1.

(a) Traditional single core design
(b) Original matrix transformer design
(c) Core simplification combining to single EI core
(d) Winding rearrangement to cancel AC flux in center leg
(e) FEA simulation with AC flux cancellation
(f) FEA simulation without AC flux cancellation

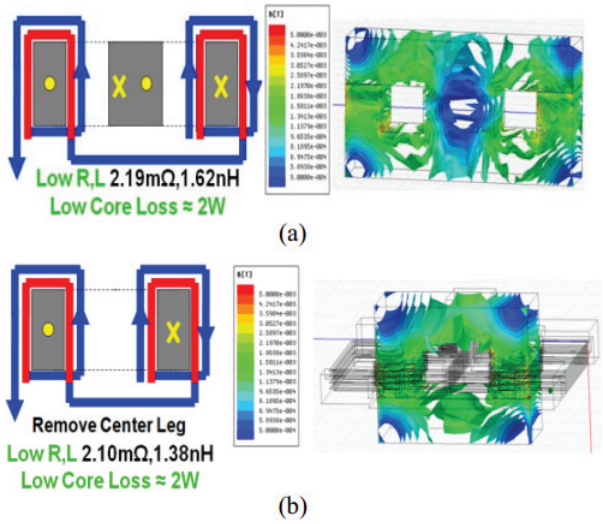


Figure 2.

(a) Integrated single core matrix structure with flux cancellation in center leg
(b) Integrated single core matrix transformer without center leg

Overview of Three-Dimension Integration for Point-of-Load Converters

High density integrated Point-of-Load (POL) converter is today's industry trend for portable electronic applications. Three-dimension (3D) integration concept is widely used for low current integrated POL converters. With this solution, a very low profile planar inductor is built as a substrate for the active components of the POL converter. By doing so, the footprint of POL converter can be dramatically saved, and the available space is also fully utilized. These 3D integrated POL converters can achieve 300-1000W/in3 power density, however, with considerably less current. In order to alleviate the intense thirst from the computing and telecom industry for high power-density high-current POL converters, the 3D integration concept needs be extended from low current applications to high current applications. In the past 10 years, CPES spent tremendous research efforts in this area and has successfully developed a series of technologies for high current 3D integrated POL converters. First, DBC based active layer was proposed to improve the thermal performance. Meanwhile, several methods were also proposed to reduce parasitic inductance of active layer, such as embedding bare die devices into active layer, building shielding layer. Then, Low profile LTCC inductors are used as the substrates for the 3D integrated POL converters. The thickness of the LTCC inductor substrate can be significantly reduced by pushing the switching frequency to several MHz. The performance of the LTCC inductor can be further improved by inverse coupling, which results in more than 40% core thickness reduction. Furthermore, the GaN HEMT was also evaluated and packaged for 3D integrated POL converter to help further increase switching frequency. Fig. 1 shows power density comparison between CPES 3D integrated POL converters with industry products. It can be seen that the proposed 3D integration technologies have successfully penetrated the barriers of high density integration for high current POL converters. Recently, A 5MHz, 12V to 1.2V, 20A, two-phase integrated POL converter with GaN transistors and LTCC coupled inductor is demonstrated with power density as high as 1000 W/in3, which is a factor of 10 improvements compared to industry products at the same current level.

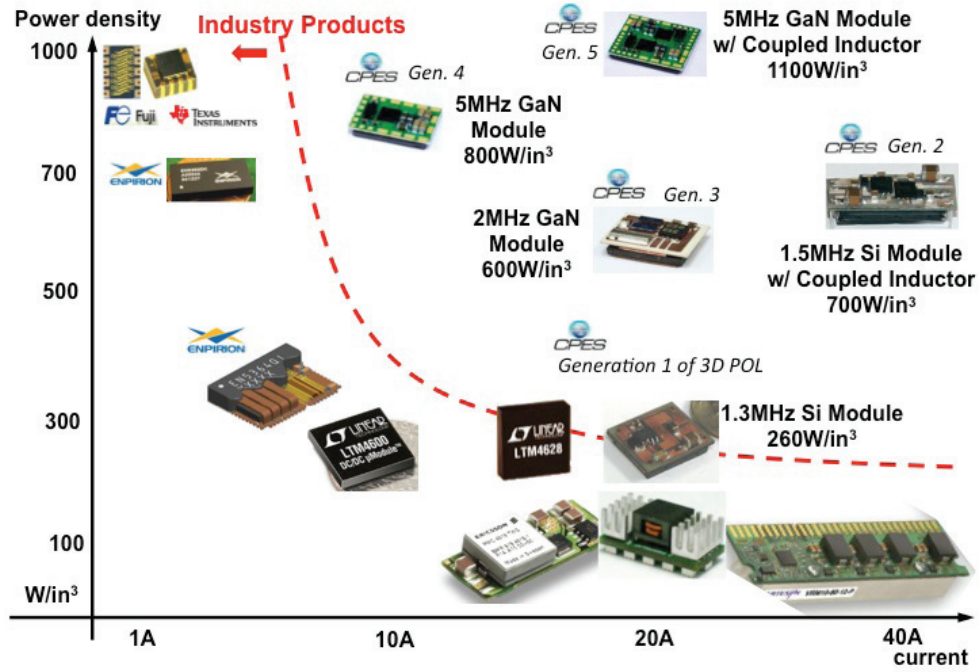


Figure 1. Power density of POL converters

Improvement in Magnetic Material Characterization Method for Arbitrary Wave Excitation

An accurate core loss characterization of a magnetic material is important in the material selection and core loss calculation in the magnetic design for DC-DC converters. The two conventional material selection criteria are based on sinusoidal excitation measurement however, none of the excitation waveforms of a DC-DC converter are sinusoidal. Therefore, the core loss measurement methods for arbitrary excitation need to be developed. A method with good accura-cy in principle was proposed recently by M. Mu, but its measurement waveform still suffers from the oscillation caused by the parasitic capacitance C1~C6 as shown in Fig. 1. To overcome this problem, a method is proposed to reduce the parasitic capacitance by reducing the thickness and turns number of the core under test. The effect of doing so is twofold: 1) The parasitic capacitance of the core under test is reduced because of a larger distance between windings and a shorter winding length. 2) The magnetizing inductance of the core under test is reduced, so the required cancellation inductance (which is the mag-netizing inductance of the reference core) is reduced accordingly. This also reduces the required turns number on the reference core, which in turn reduces the parasitic capacitance on the reference core too. As a result, a clean waveform with almost no oscillation can be achieved as shown in Fig. 2. Using the proposed method, the core loss density of 3F35 at 500kHz 100°C is measured, and the waveform oscillation impact on the measurement results is shown in Fig. 3. It can be seen that the error caused by the oscillation can be positive or negative; and the oscillation impact is more severe at a smaller flux density and non-symmetrical duty cycle (other than 50% duty cycle).

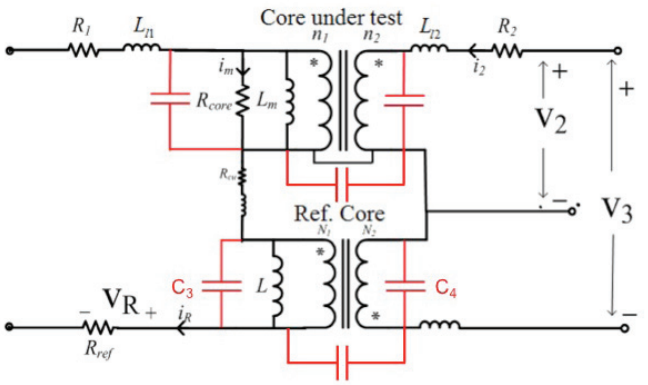


Fig. 1. Core loss measurement method for arbitrary wave-form excitation and its major parasitic capacitance

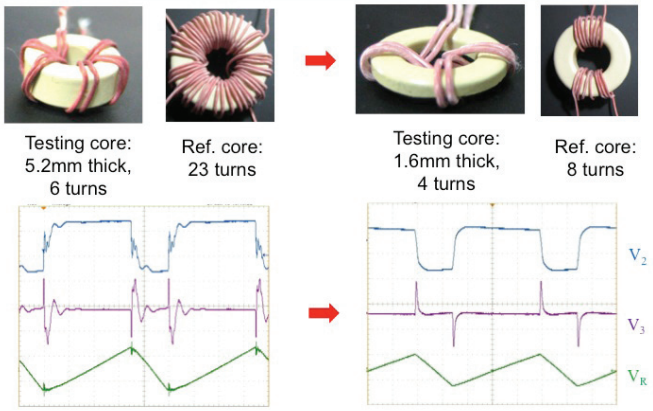


Fig. 2. Proposed method to decrease the waveform oscillation.

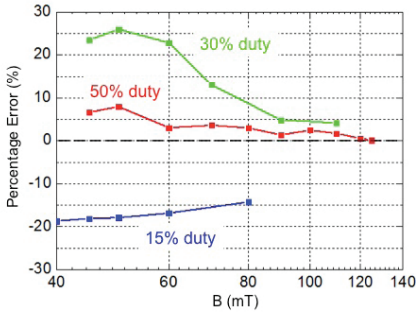


Fig. 3. Error caused by the waveform oscillation.

EMI Terminal Modelling of DC-Fed Motor Drives II: Differential Mode & Total Noise

A three-terminal noise-model was shown earlier to predict the common-mode (CM) currents at the input and output side of a dc fed motor-drive system. Accuracy of this model was found to be good up to 30 MHz. The DO-160 standards for aerospace applications however are based on total noise, therefore having just a CM model is not enough when simulating for EMC compliance. This paper proposes simple terminal models to predict the differential mode (DM) noise currents in a motor-drive system. In the end, predictions from the CM and DM models are combined to estimate the total noise at the input and output side of the motor-drive system.

The model is based on Thevenin equivalent of a two terminal network. Investigations re-vealed that in differential mode (DM), the input and output side of the motor-drive can be considered decoupled, provided the dc-link at the input side is adequately decoupled. Under this assumption the DM model can be split and extracted independently for both input and output side. This idea is shown in Fig. 1.

The model impedances (ZDM-dc and ZDM-ac) are approximated using direct measurements under power-off conditions and the model sources (VDM-dc and VDM-ac) are extracted experimentally using terminal modelling techniques. Once the models are extracted, the prediction of DM EMI currents for an input side DM filter shown in Fig. 2 is carried out. Also, the total noise is estimated by adding the predicted noise from the DM model and the CM noise from the previously developed CM model. These prediction results are shown in Fig. 3 and 4.

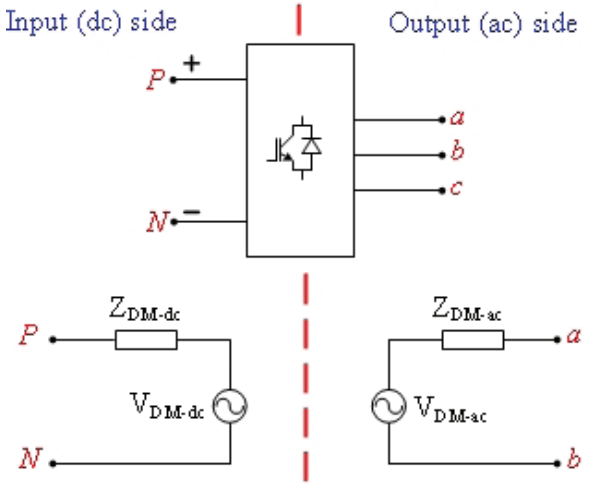


Fig.1: DM noise models for a motor-drive system

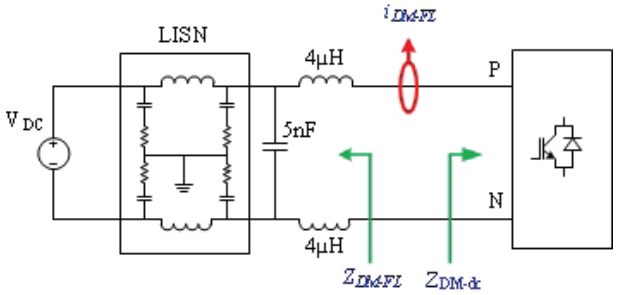
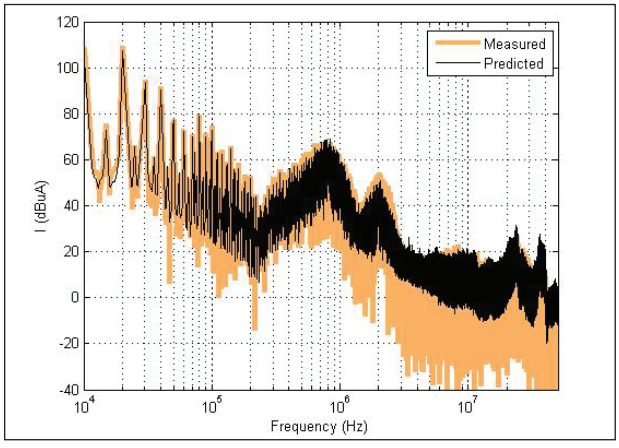


Fig. 2: DM noise prediction (i_{DM-FI})



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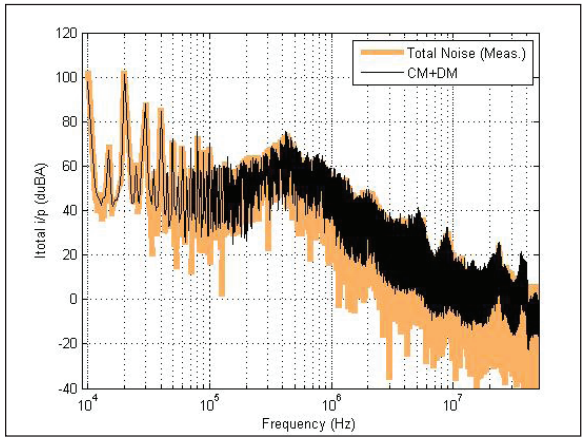


Fig. 4: Total-noise prediction at input side

Total Flux Minimization Control for Integrated Inter-Phase Inductors in Paralleled, Interleaved Three-Phase Two-Level Voltage-Source Converters With Discontinuous Space-Vector Modulation

Three-phase voltage source converters (VSCs) are very popular in AC medium and high power applications. Paralleled three-phase VSCs have the benefits of higher power, modularity, redundancy and, flexibility. Interleaving can reduce output harmonic currents in a paralleled VSCs system, which has the potential to increase power density; a desired effect for many applications such as vehicle and aircraft. This benefit is more significant for rectifier applications as shown in Fig.1, where the interphase inductor that is used to suppress the circulating current generated by interleaving can be integrated with the boost inductors which already exist in the system.

Due to the phase-shifting of the two converters in the interleaving topology, the total flux in the integrated input inductors will include the low frequency part that is related to the output current, and the high frequency part that is related to the circulating current, as shown in Fig. 2. Without proper control, those two parts will add together and the total flux will be larger than the non-interleaving case. However, with proper control of the circulating current, the high frequency flux can be controlled as in Fig.2b, then the total flux is minimized and the input inductor size can be smaller.

In the interleaving topology shown as Fig.1, when a discontinuous PWM modulation method is used, the circulating current will not change after the switches are clamped in one phase. Total flux can be minimized if the circulating current in this phase can be controlled to zero before switches are clamped. The amplitude of the CM circulating current can be adjusted by controlling the portion between ppp and nnn in the zero vector duration as shown in Fig.3. Since the CM circulating current is part of the total circulating current, the amplitude of the total circulating current can also be adjusted to zero by controlling the amplitude of the CM circulating current. Using this method, the total flux of the input inductor can be minimized and the inductor size can be reduced.

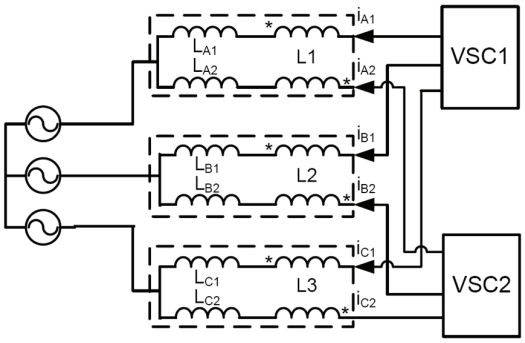


Figure 1: Interleaved three phase rectifier

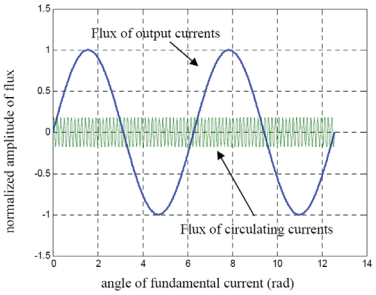


Figure 2a: flux without control

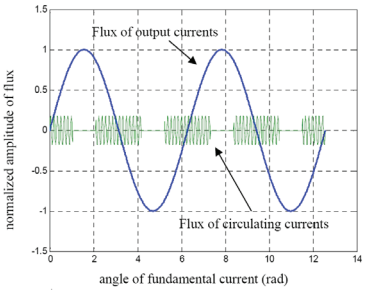


Figure 2b: flux with flux minimization control

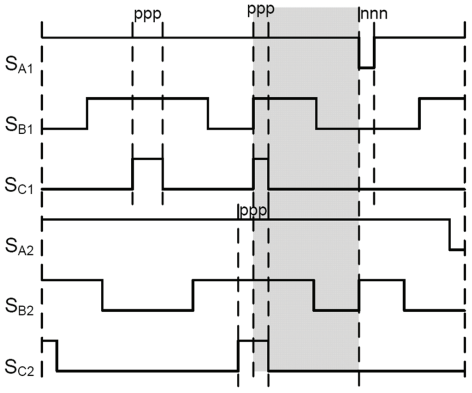


Fig. 3 Control method for flux minimization control

EMI Filter Design Considering In-Circuit Impedance Mismatching

A simple insight is created into how the impedance at the input and output side of the EMI filter affects their noise attenuation performance. These impedances are also called propagation path impedances. An understanding of these impacts can help in choosing the optimum filter topology for any given set of propagation path impedances. Fig. 1 shows a noise source connected to an external network. In a conducted EMI set-up, the noise source is the power converter and the external network is the line impedance stabilization network (LISN). To attenuate the noise flowing into the network, a filter is inserted which alters the path of the noise and provides imped-ance mismatching on either side. The attenuation provided by the filter in Fig. 1 can be calculated as

$$Atten\ ;\ \frac{I_s}{I_0}\ ;\ \frac{(1*\frac{Z_{22}}{Z_{LISN}})(1*\frac{Z_s}{Z_{11}})\ \therefore\frac{Z_c^{\ 2}}{Z_{LISN}Z_{11}}}{(1*\frac{Z_s}{Z_{LISN}})T_{21}}$$

$$where\ \ T_{21}\ ;\ \frac{Z_{21}}{Z_{11}}$$

It is evident that the noise attenuation comes from three terms: Z_{22}/Z_{LISN}, Z_S/Z_{11} and T_{21}. Other terms like Z_S and Z_{LISN} are fixed by the design and the standards used for EMI compliance. For the differential mode (DM) filter the impedance Z_S is decided by the large input dc-link capacitor of the converter and when Z_{LISN} equals 100 (standard LISN). Thus, for a simple LC filter and a very small Z_S, the inductor (L) of the filter should be facing the converter so that Z_{11} can be easily made greater than Z_S , which results in Z_S/Z_{11} becoming very small. On the other hand, if the capacitor (C) of the LC filter is facing the LISN, this will make Z_{22}/ Z_{LISN} small as well. In this way the attenuation will be decided by T_{21} only. In order to make the attenuation larger, T_{21} should be as small as possible, which can be easily achieved when the LC filter with L is facing the converter $Z_{11} = Z_L + Z_C$ and $Z_{21} = Z_C$.

A similar understanding is created in the case of the common-mode (CM) filter. Here contrary to the DM - LC filter, the C should be facing the converter as the CM capacitance of the converter is usually very small thus causing Z_S to be very large. Moreover, in CM the LISN impedance is only 25 so the L should face the LISN. Such a choice will provide the optimum impedance mismatching in the case of CM as it will make both Z_S/Z_{11} and Z_{22}/ Z_{LISN} very large, which causes the attenuation to be large as well.

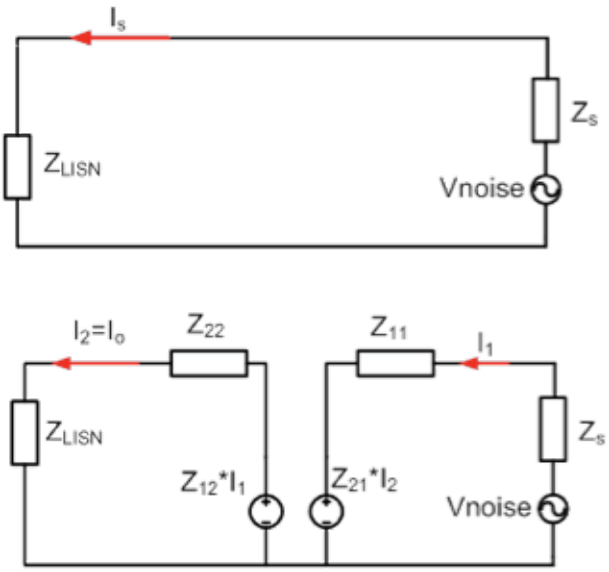


Fig. 1: DM noise models for a motor-drive system

EMI Filter Design and Optimization for Both AC and DC Side in a DC-fed Motor Drive System

Huge bulky EMI filters are inevitable parts in power electronic systems, which not only provide attenuation to the EMI noise but also take a significant portion of the total volume and weight of converters. It is more obvious in DC-fed motor drive systems (shown as Fig. 1) with long con-nection cables where EMI filters are required for both the AC output and the DC input side. Inter-action exists between the AC and DC side, for DM noises, due to the presence of the big dc-link capacitor, the AC and DC side are somehow decoupled and the equivalent circuit can be separated for the DC and AC side at a certain operation point. Adding a filter on one side will not change the propagation path impedance of the other side. However, the noise source for the AC side is related to the voltage harmonics on the DC link capacitor and the noise source for the DC side is related to the harmonics of the output AC current. Adding filters on one side will change those harmonics, thus it will change the noise source of the other side and there is still interaction between AC and DC DM filters.

Considering that the CM noise is going though both the AC and DC side, and there is no such big low impedance path as the dc link capacitor in DM propagation path, the equivalent circuit includes the interaction between the AC and DC side for the CM noise. Adding an EMI filter on one side will influence the EMI noise level on the other side. If this interaction is not considered in the filter design procedures, even though one can design an optimized filter for one side to meet the standard, adding a filter on the other side will make the noise worse on this side and finally fail to meet the standard. To minimize the impact on the EMI noise of one side caused by adding a filter on the other side, a certain design order must be followed to design the AC, DC, CM and DM filters. Fig.2 shows an optimized design procedure for designing both AC and DC filters. Using this method, both AC and DC noises can meet the standard.

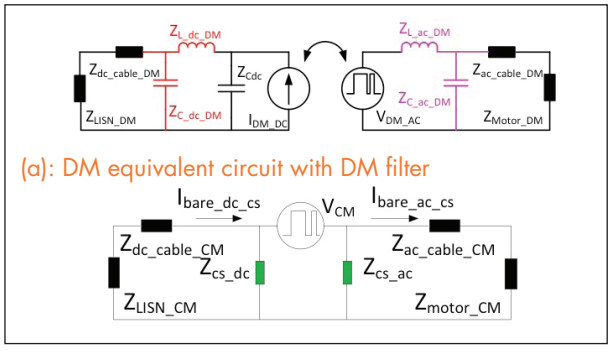


Fig. 1. Equivalent circuits for EMI filter analysis

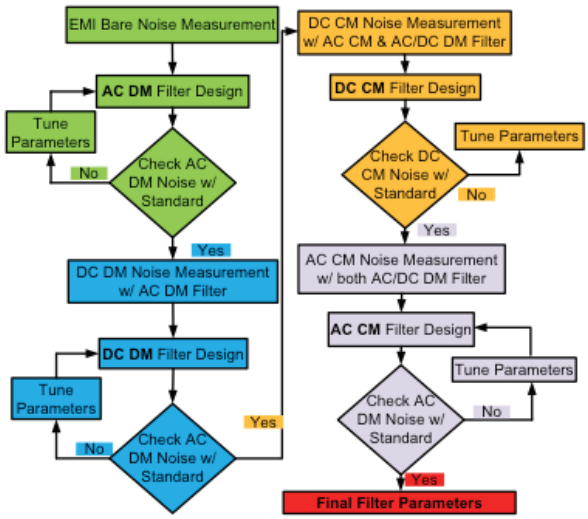


Figure 2: EMI filter design sequence for both AC and DC Side

Size and Weight Dependence of the Single Stage Input EMI Filter on Switching Frequency for Low Voltage Bus Aircraft Applications

There is hope that Gallium-nitride (GaN) power electronics technology can lead to significant increases in the switching frequency of power converters. The ability to switch more frequently gives the potential to increase the power density of converters. EMI filters engage a large portion of system weight and volume, and it is not so straight forward to conclude that increasing switching frequency will benefit the size and weight reduction of EMI filters. In this work, the impact of increasing switching frequency on the single stage EMI filter size and weight is inves-tigated in a DC/DC converter for low voltage bus aircraft applications. In the initial paper design, it was assumed that the corner frequency of the EMI filter is determined by the low frequency noise spike. Obtained in that way, the differential mode (DM) filter size and weight would reduce increasing switching frequency, while the Common Mode (CM) filter show very little increase due to a smaller CM propagation path impedance at higher frequencies. For verification purposes, two different resonant LLC converters are implemented at switching frequencies of 1 MHz and 2 MHz.

Experiment results show that the EMI filter was larger and heavier for the 2 MHz case (Fig. 4) due to high frequency noise spikes at tens of mega-hertz (Figs. 1-2). This conclusion was made based on the low frequency attenuation requirement. However, in the hardware implementation the real limitation comes from the spectrum at high frequencies, 20 MHz - 30 MHz. The problems at high frequencies arise from several different factors. First, the permeability of the nanocrystaline material drops significantly with the frequency, thus making this material less effective in the 20 MHz - 30 MHz range. Secondly, parasitics of the filter components, such as the ESL of the capacitors and EPC of the inductors, degrade the performance of the filter. The conclusions of this paper are limited to the assumptions and approaches taken, such as single stage passive filtering, magnetics materials choice, no integration (Fig 3) and the design procedure.

Fig. 3. 1 MHz EMI filter

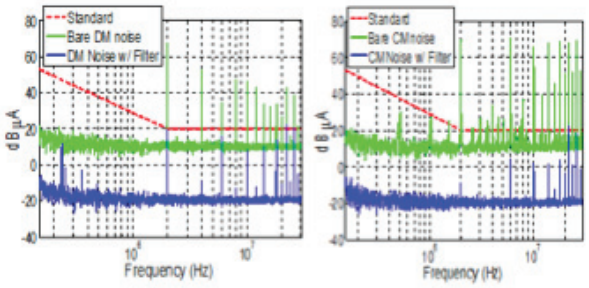


Fig. 1. 2 MHz noise spectrum.

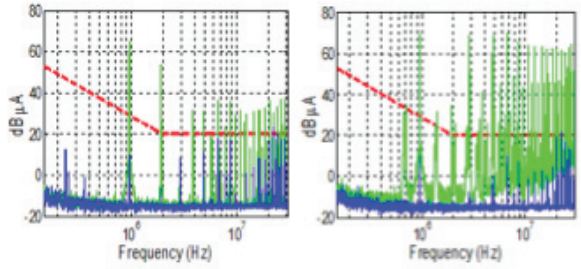


Fig. 1. 2 MHz noise spectrum: left-DM noise; right-CM noise

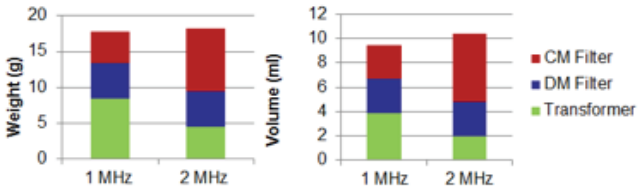


Fig. 4. Converter magnetics volume and weight for 1 MHz and 2 MHz.

Improved Common Mode Elimination Modulation for Neutral-Point-Clamped Three-Phase Inverters

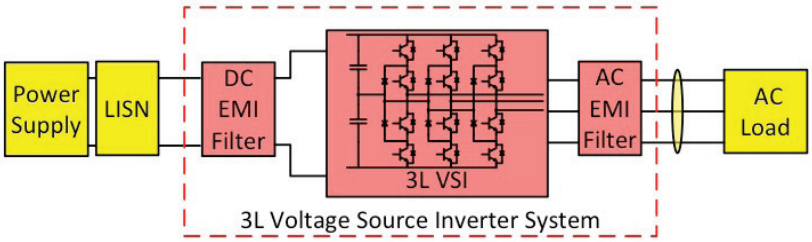


Fig. 1: Three level voltage source inverter system

The voltage-source pulse-width modulation (PWM) inverter has made a significant contribution to achieving energy conservation and improving system performance in many applications. Compared with two level voltage source inverters, neutral-point-clamped (NPC) inverters can achieve better performances on ripples, harmonics and EMI. The common mode elimination (CME) modulation is a well-known modulation method which can theoretically eliminate the common mode voltage. However, in the real implementation, due to the existence of dead time (DT) which avoids the shoot through problem during operation, the real benefit from CME modulation is limited and the penalty on voltage utilization ratio and the loss of neutral voltage balancing capability make this modulation method less practical.

To overcome the penalty for adding DT, an improved compensation method is proposed, based on the switching states analysis of each 3L phase leg. The impact of DT on CM voltage generation can be calculated as shown in Fig.2. To eliminate this impact, the vector sequence in CME modulation can be adjusted based on the current direction of the three phases.

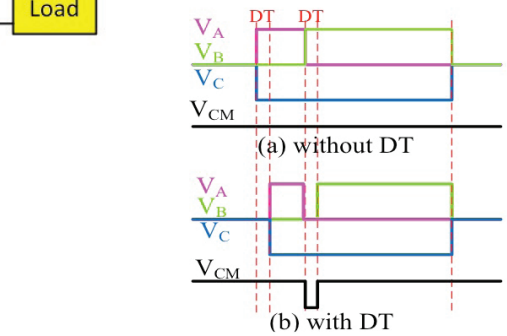
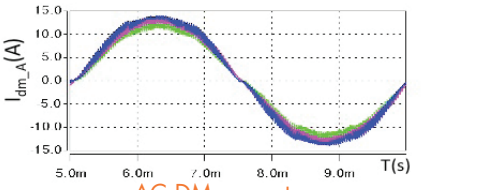


Fig. 2: Impact of DT on CM voltage generating in one swithcing period

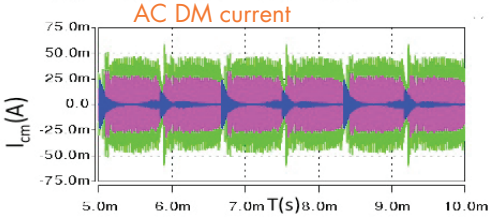
Table I: Vector sequence selection of ICME in sector 1

when I_{out} direction of phase A, C is differnet with Phase B						
Dwell time	$T_0/2$	$T_1/2$	$T_2/2$	$T_3/2$	$T_1/2$	$T_0/2$
A	O	O	P	P	O	O
B	O	P	O	O	P	O
C	O	N	N	N	N	O
when I_{out} direction of phase B, C is differnet with Phase A						
Dwell time	$T_0/2$	$T_2/2$	$T_1/2$	$T_1/2$	$T_2/2$	$T_0/2$
A	O	P	O	O	P	O
B	O	O	P	P	O	O
C	O	N	N	N	N	O
when I_{out} direction of phase BC is differnet with Phase C						
Dwell time	$T_1/2$	$T_0/2$	$T_2/2$	$T_2/2$	$T_1/2$	$T_0/2$
A	O	O	P	P	O	O
B	P	O	O	O	O	P
C	N	O	N	N	O	N

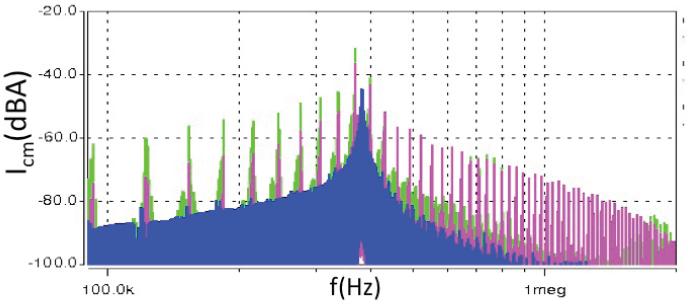
Verification results show that the CM noise can be reduced significantly with this compensation method. However, there will be more distortion in the output current.



AC DM current



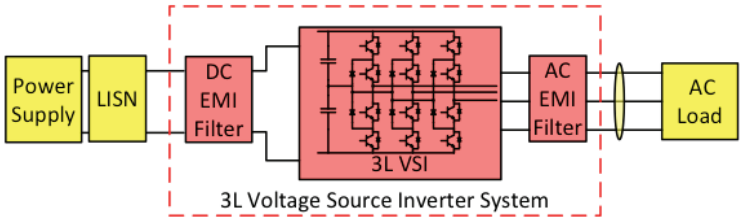
AC CM current



AC CM current spectrum

Fig. 3 System test results: With 0.5 us DT: pink: with 1us DT: Green, with 1us DT and DT compensation: blue

Impact and Compensation of Dead Time on Common Mode Elimination Modulation for Neutral-Point-Clamped Three-Phase Inverters



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The voltage-source pulse-width modulation (PWM) inverter has made a significant contribution to achieving energy conservation as well as improving system performance and productivity in many applications such as variable frequency motor drives, uninterruptible power systems and renewable energy systems. Compared with two level voltage source inverters, neutral-point-clamped (NPC) inverters can achieve better performances on ripples, harmonics and EMI. The common mode elimination (CME) modulation is a well-known modulation method which can theoretically eliminate the common mode voltage, however, in the real implementation, due to the existence of dead time (DT) to avoid shoot through problem during operation, the real benefit from CME modulation is limited and the penalty on voltage utilization ratio and the loss of neutral voltage balancing capability make this modulation method less practical.

To overcome the penalty for adding DT, a compensation method can be applied based on the switching states analysis of each 3L phase leg. The impact of DT on CM voltage generation can be calculated as shown in Fig.2. To eliminate this impact, a compensation algorithm is proposed as shown in Table I.

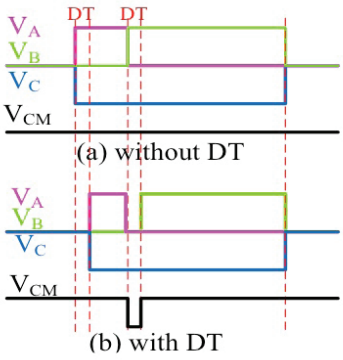


Figure 2: Impact of DT on CM voltage generating in one swithcing period

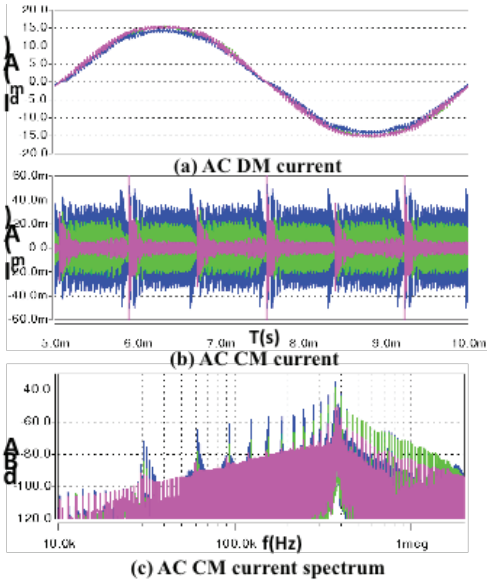


Figure 3: System test results; With0.5us DT: Green; with 1us DT: blue, with 1usDT and DTcompensation : pink

System verification results show that the CM noise can be reduced significantly with this com-pensation method. Moreover, there is less distortion in the output current.

TABLE I. DEAD TIME COMPENSATION ALGORITHM

Voltage transition	Compensation	
	phase current i>0	*phase current i<0*
O→P→O	Add DT at the beginning of S1,S3	Reduce DT in the end of S1,S3
O→N→O	Reduce DT in the end of S2,S4	Add DT at the beginning of S2,S4

Impact of Interleaving on Common Mode EMI Filter Weight Reduction of Paralleled Three-Phase Voltage-Source Converters

An adjustable-speed motor drive with a voltage-source pulse-width modulation inverter with long cables (shown as Fig.1) brings the EMI issues to the motor drive system [1]. Usually EMI filters are part of the system that makes both AC and DC sides meet the EMI requirement (such as DO160E standard), which takes a large portion of the system weight. To improve system power density and reliability, a paralleled and interleaved converter topology is commonly used. By phase-shifting the PWM switching cycles of individual converters with an appropriate angle, the total voltage ripple due at PWM switching at the ac terminal can be reduced, which provides the possibility of EMI filter weight reduction. To reduce EMI filter weight, a small angle interleaving is presented in the previous study, which shows the reduction on inductor values (as shown in Fig.2). However, in inductor design, inductor weight is also related with the volt-second on the inductor (as shown in Fig.3) where symmetrical interleaving has a higher benefit.

Considering the noise propagation path impedance and volt-second on the induc-tors, the selection of the interleaving angle is analyzed in detail in order to study the im-pact of interleaving on the real EMI filter weight reduction. Different interleaving angles are compared for both the AC and DC side of the EMI filter design. This shows that symmet-ric interleaving gives a smaller EMI filter weight for the AC side, however a small angle interleaving is better for DC side (as shown in Fig.4).

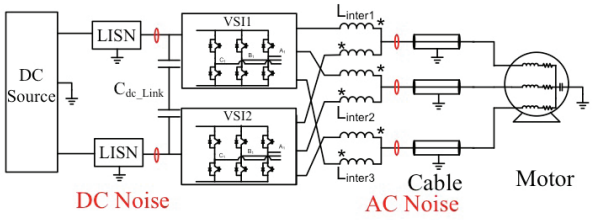


Figure 1: Interleaved 2L VSI DC-fed motor drive system

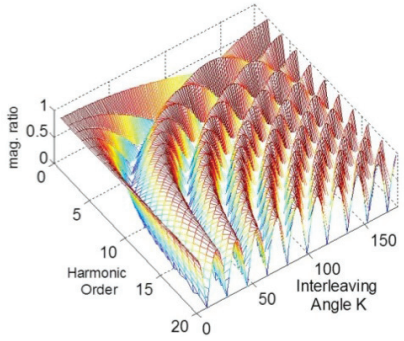


Figure 2: Voltage reduction ratio on different order harmonics with different k

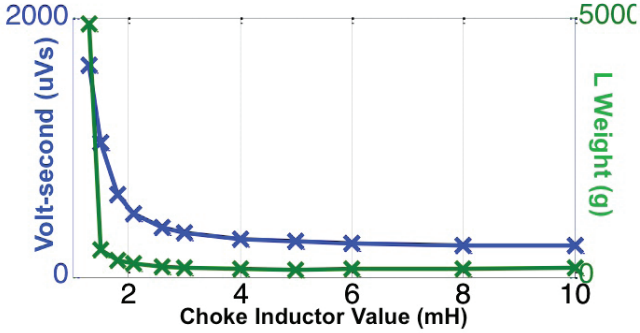


Figure 3: Filter weight : green and volt-second blue: VS inductor value

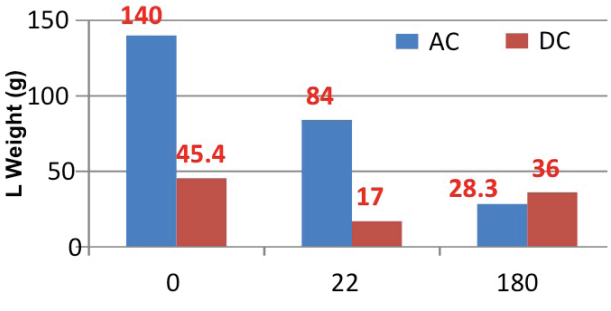


Figure 4: AC and DC side EMI filter weight comparison with different interleaving angle

High-Frequency Model of a Transformer for Conducted EMI Analysis

The switching frequency of power electronic systems is continuously increasing to meet the higher power density requirements. It is getting increasing more difficult to simultaneously meet the stringent EMC standards and converter performance. Accordingly, virtual prototyping is gain-ing popularity as it offers the designer a comprehensive insight into the electromagnetic behavior of the system before the final hardware design.

An accurate simulation model is needed for each component of the power converter to analyze the complete system. With this goal in mind, a high-frequency model of the transformer (Fig. 1) used in a commercial battery charger system is proposed. The simulation results are verified against the measured data.

The existing high frequency models are not able to accurately predict the impedance, either common- or differential-mode, over a wide frequency range (10 kHz-110 MHz). The existing methods for modeling a choke ignore the inter-winding capacitance for simplicity. This is not the case for a transformer, and hence a new lumped circuit model is proposed in Fig. 2. The coupling factors kC and kD are adjusted so that the common-mode current does not have any effect on the differential-mode elements and vice-versa.

A series or parallel R-L-C combination is used to predict the predominant capacitive or inductive behavior of the common- or differential-mode impedance, respectively. The no. of resonance peaks determines the number of stages of R-L-C used.

The simulation model is obtained by numerically fitting a lumped circuit of R-L-C in MATLAB to the measurement results. Finally, all the passives are combined to obtain the complete high-frequency model of the transformer, and the impedance measured in different configurations is compared against the Saber simulation model. The results of the common-mode impedance are shown in Fig. 3; it is within 3 dB of the measured result.

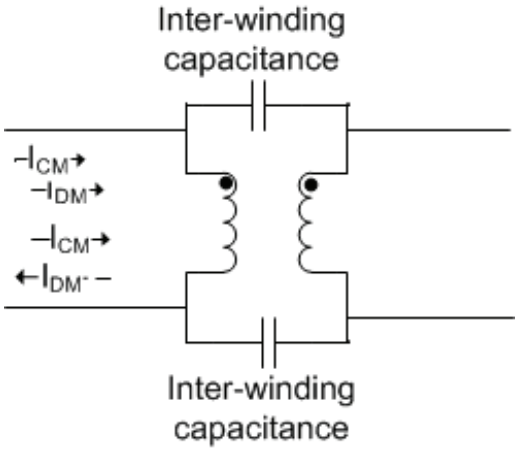
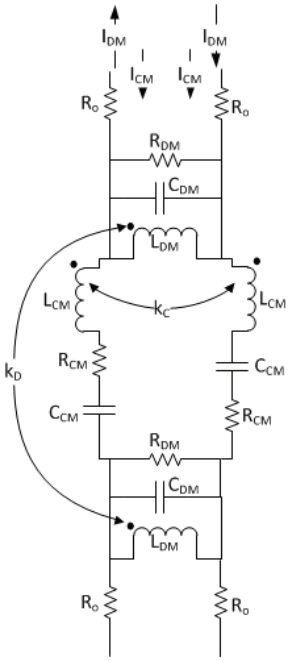


Fig. 1. 2-winding transformer

Fig. 2. Proposed high frequency model of 1:1 transformer to predict the first resonance peak



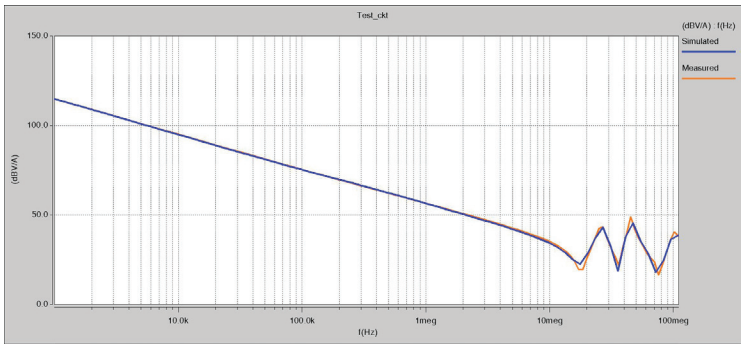
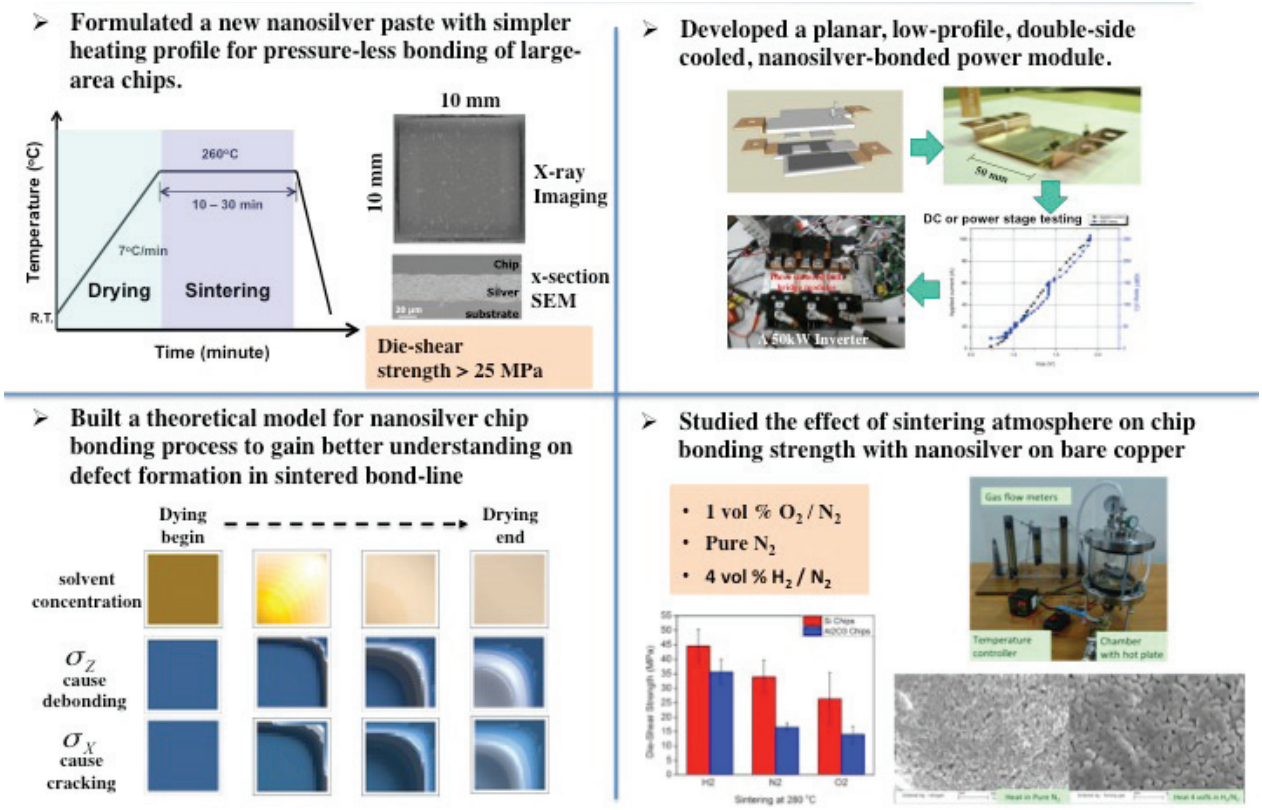


Fig. 3. Comparison of common-mode impedance by measure-ment and the simulation model

An Update on Recent Advances in Nanosilver Paste for Packaging Power Semiconductor Devices



A 1200 V, 60 A SiC MOSFET Multi-Chip Phase-Leg Module for High-Temperature, High-Frequency Applications

The requirement of high power density for today's power converters is continuously pushing the Si devices to their limits, in both the operating temperature and switching frequency. In many applications, the newly commercialized SiC devices have become the ideal choice for substitute.

In this work, commercial SiC MOSFETs are used to build a 1200 V, 60 A phase-leg module for high-temperature operation. Three 1200 V, 20 A SiC MOSFETs and three 1200 V, 10 A SiC Schottky diodes are paralleled in each switch position to reach the rated current. The power module is designed and fabricated with all high-temperature packaging materials. In order to reduce the package parasitics, an improved substrate layout based on the "switch pair" concept is adopted to minimize the main switching loop inductance, which is critical in causing the switching transient ringing. The switching performance is further improved by embedding DC decoupling capacitors inside the module, which helps to decouple the parasitics from the module's busbar (Fig. 1). With this design, the SiC power module can achieve much faster switching speed than conventional Si IGBT modules without suffering from serious parasitic ringing. Continuous test successfully verifies the high-temperature and high-frequency operation of the module by running the devices at 200 °C and 100 kHz (Fig. 2).

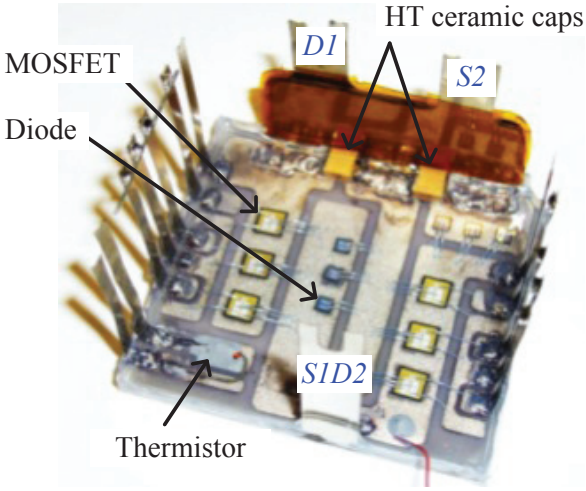
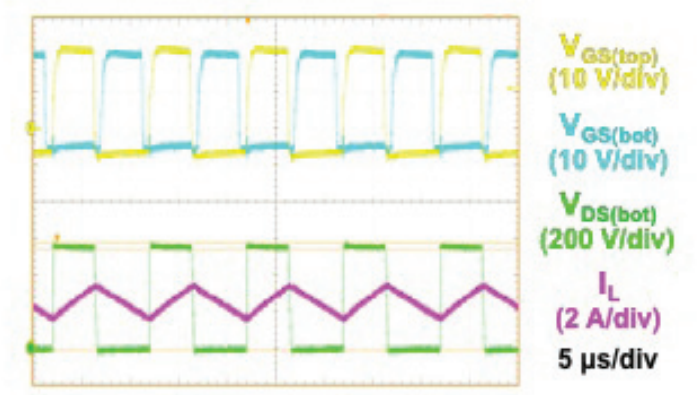
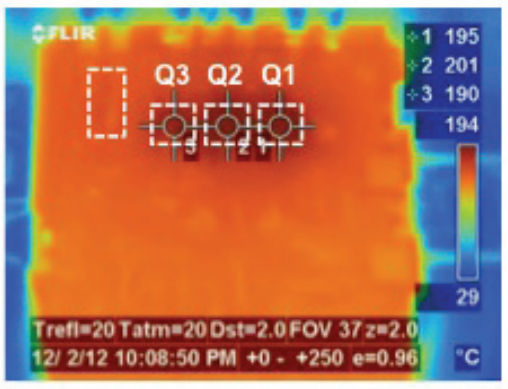


Fig. 1. SiC MOSFET phase-leg module



(a)



(b)

Fig. 2. Buck-mode test of the module at 200 °C and 100 kHz
(a) Experimental waveforms, (b) thermograph picture showing the temperature distribution

PCB Embedded Magnetics Core with Improved Flake Materials

The magnetic components usually dominate the weight and volume of the switching power supply. Significant improvements are possible by integrating the magnetic core into the PCB, and by using this PCB as the substrate that carries the rest of the components of the converter. Therefore, a more compact and thinner structure can be achieved especially when compared to the conventional circuit. In addition, the standardized manufacturing process reduces the cost because less manual steps are necessary.

In previous PCB integration techniques, the magnetic materials either have a very low permeability, or are difficult to be shaped with low temperature processing. The SENFOLIAGE metallic flake material developed by NEC/Tokin improves the permeability to several hundreds, which is much higher than that of the conventional flake material. By aligning the small flake pieces as shown in Fig. 1, the eddy current loss in megahertz is reduced dramatically. More important, the core material is very easy to be patterned. The laminated multi-layer PCB with SENFOLIAGE plate is proposed as Fig. 2 and fabricated as Fig. 3. The surface copper on the PCB can be used to build the windings and the circuit connection. The SEM image in Fig. 4 shows the lamination of FR4 and magnetic core is cohesive and no delamination is observed. Therefore, the SENFOLIAGE is compatible with the conventional PCB process and it is good candidate for PCB integration of high frequency converters.

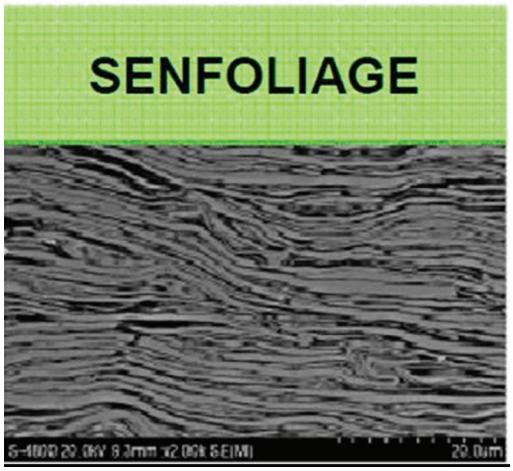


Fig. 1 Laterally aligned flake magnetic material

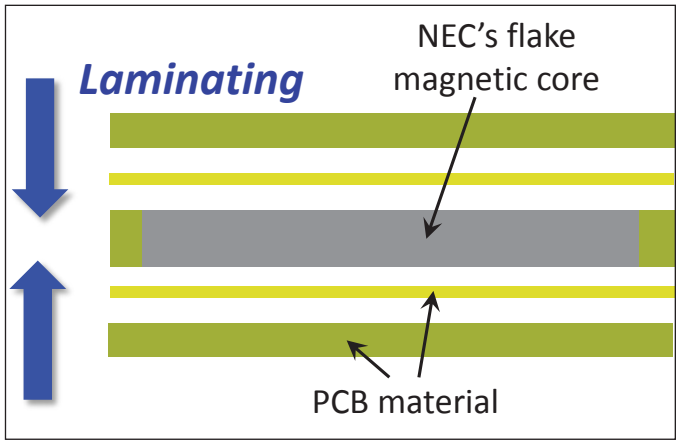


Fig. 2 Multi-layer PCB structure with embedded core

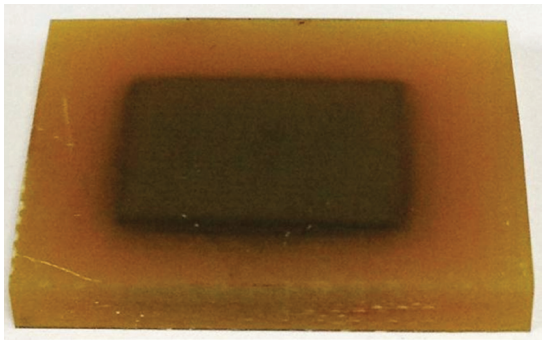


Fig. 3 Fabricated PCB embedded magnetic core

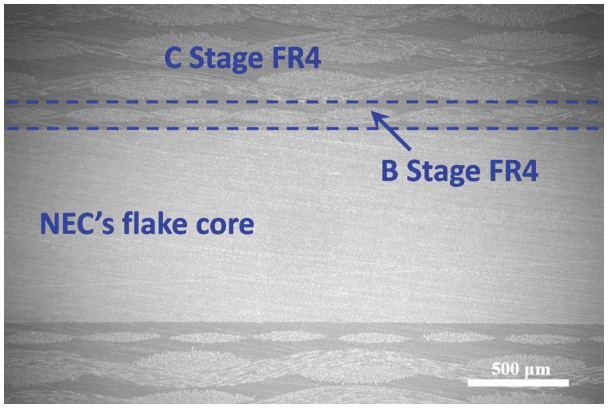


Fig. 4 SEM image with cross-sectional view

High Frequency 3D integrated POL Module Based on PCB Embedded Core

With a low profile LTCC inductor substrate and a GaN device, the 3D integrated POL module demonstrates the ability to achieve a 1kW/in3 power density at 15A with a multi-megahertz switching frequency. However, the fabrication still involves a high temperature process and the cost of this solution is relatively high.

Fig. 1 and Fig. 2 show the PCB embedded inductor substrate and the PCB integrated POL module with a 20A output current. The improved flake material, SENFOLIAGE, is sandwiched into multi-layer PCB as the core. The silicon based NexFET power stage from TI is used to build the active circuit. The efficiency and the power density of the POL module are measured in Fig. 3. The PCB integrated module achieves almost the same power density as the LTCC integrated alternative, except that the cost is reduced and it's easier to fabricate with the low temperature process.

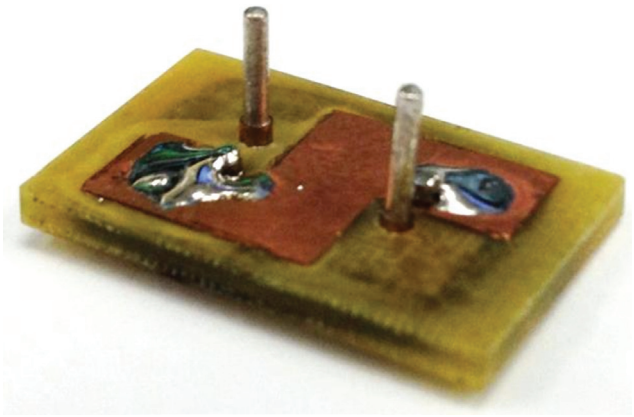


Fig. 1. Low profile PCB integrated inductor substrate

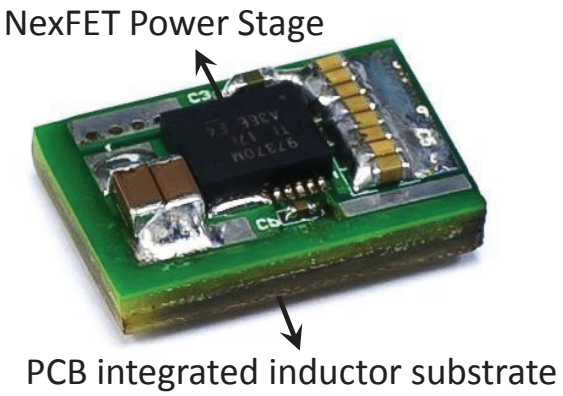


Fig. 2. 3D PCB integrated POL module

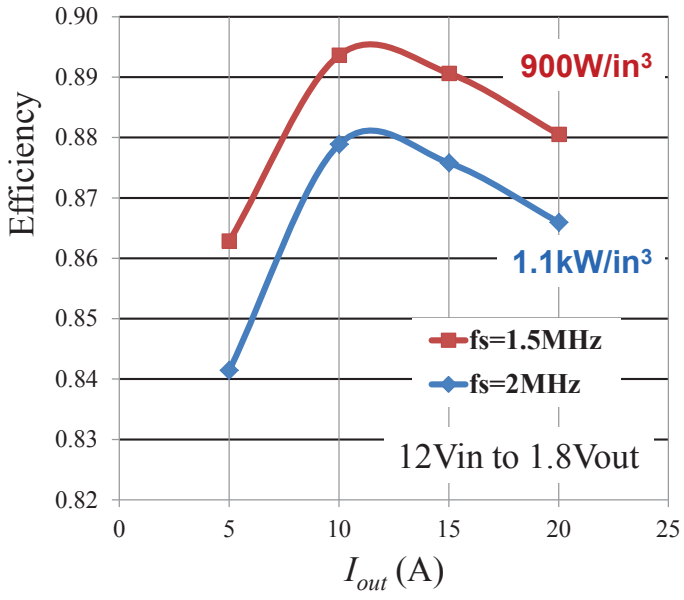


Fig. 3 Measured efficiency and power density of the 3D PCB integrated POL module

Survey of High-Temperature Polymeric Encapsulants for Power Electronic Packaging

Semiconductor encapsulant is crucial to electronic packaging because it protects the packages from mechanical stresses, electrical breakdown, chemical erosions, γ radiations, etc. Conventional encapsulants, including acrylic-, urethane-, and most epoxy-based polymers, are only applicable below 150°C. However, with increasing demand for high-density and high-temperature packaging, encapsulants that can work beyond 200°C are required. In this survey, four types of encapsulants, including conformal coatings, underfills, molding compounds, and potting compounds, are studied. Recommended properties and selection criteria for each type are listed. Standard testing methods for glass transition temperature (Tg), coefficient of thermal expansion (CTE), dielectric strength, etc. are introduced. Also, commercial products and current research topics for high-temperature encapsulation are surveyed. Novel material compositions, including silicone-, cyanate ester-, bismaleimide (BMI)-, and polyimide-based composites, are identified as potential high-temperature encapsulants for power electronic packaging.

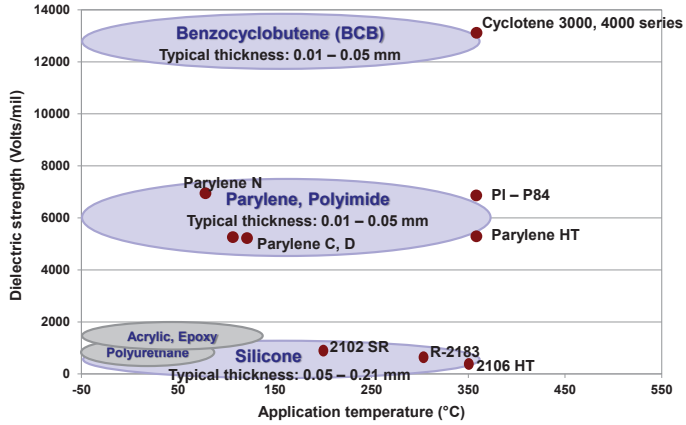


Fig. 1. Dielectric strength and operation temperature range of commercial conformal coatings

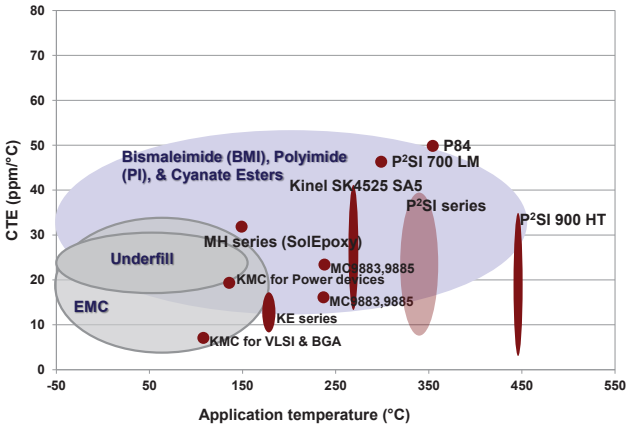


Fig. 2. Dielectric strength and operation temperature range of commercial underfills and molding compounds

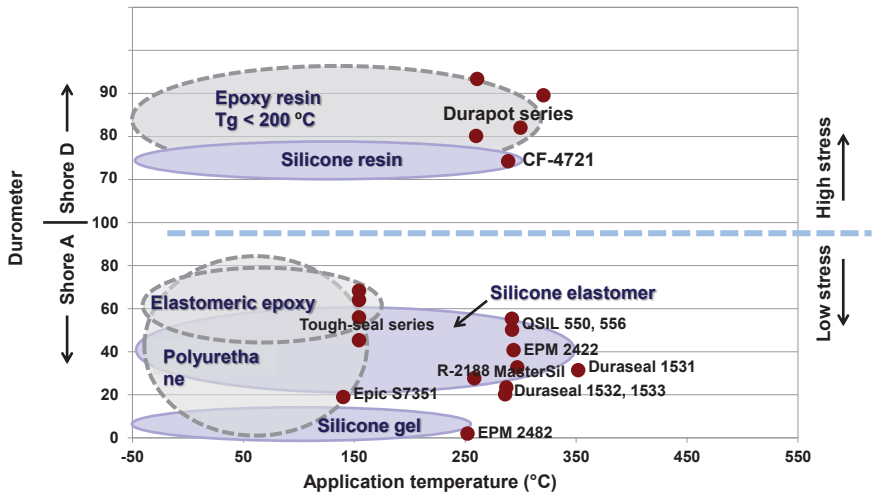


Fig. 3. Dielectric strength and operation temperature range of commercial potting compounds.

Improved Procedure to Design Coupled Inductors Based on Geometry Constant

With the fast development of telecom, computer, and network systems, it is desirable to re-duce both power consumption and volume. In these systems, magnetic components usually oc-cupy most of the volume for the whole converter. In order to minimize magnetic loss, the design of coupled inductors becomes more critical at a multi-megahertz range. This paper is to propose a step-by-step inductor design approach based on a geometetrical constant method with mini-mum total loss.

A design example of coupled inductors is shown to illustrate the entire design procedure. The planar coupled inductors are utilized in the Quasi-Square-Wave (QSW) flyback converter shown in Fig. 1 with a switching frequency of 5 MHz and an output power of 30 W. The turns-ratio is 4:1 and the magnetizing inductance is 1 μH.

After surveying the commercial magnetic materials for a 1-5 MHz operation, Ni-Zn ferrite (4F1) is chosen to be the core material. The geometrical constant Kg, as a measure of the effective magnetic size of a core, is used to select the core dimensions for the application. The criterion of core selection is derived in (1). Because of thermal limitations in the core material, a flux density ΔB was limited to 10 mT. The value of the left side, which is related to the core ge-ometry, needs to be as close as possible to the value on the right side, which is based on electri-cal specifications and Steinmetz coefficients of the material.

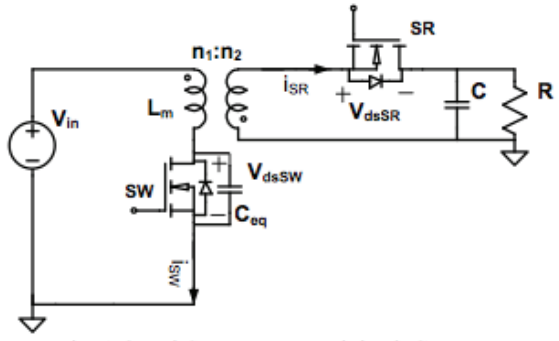


Fig. 1 Quasi-Square-Wave Flyback Converter

The coupled inductors are shown in Fig. 2 with a size of ER 18×3.2×10 mm, a two-layer PCB winding with top and bottom 70-μm-thick copper and 0.127-mm-thick dielectric material.

$$\frac{W_A A_c^3 l_e}{MLT};\ \frac{(\sqrt{D}*\sqrt{D\bullet})^2\ \hat{}\partial L_m^2}{2K_u\ \Upsilon K_{fe}}\sqrt{\frac{i_{dc}^2}{n^2 D\bullet^2}}\ \text{TM}\frac{V_{in}D}{\sum L_m f}\Big|^2 * \frac{1}{12}\ \text{TM}\frac{V_{in}D}{\sum L_m f}\Big|^4 \lambda \varsigma B^{:(\Upsilon\%2)}$$

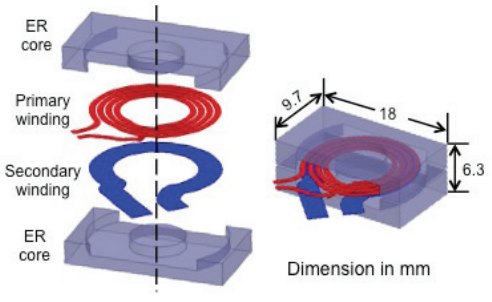


Fig. 2. Exploded view of planar structure

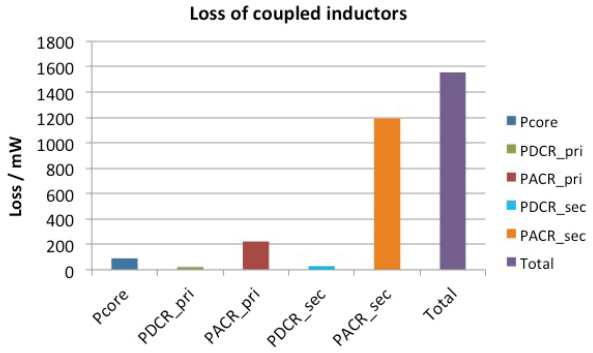


Fig. 3. The loss breakdown of coupled inductors

Fig. 3 shows the loss breakdown of the coupled inductors. The overall loss exhibited 5.2% of 30 W output power. In the future, a proximity effect will be taken into consideration to optimize the design.

Power Cycling the IGBT Module and Zth Measurement of Die Attach

The reliability of the die attach layer is of utmost importance for switching devices like IGBTs and MOSFETs. Power cycling is one of the ways to determine the reliability of the device in an accelerated manner. This would save time and hence speed up the productivity. The thermal impedance (Z_{th}) of the die attach layer is the parameter used here to define the failure of the joint in the module.

The gate emitter voltage (V_{ge}) of the IGBT is used as a temperature-sensitive parameter to accurately sense the junction temperature (T_j) of the IGBT during transients. A pre-characterized relationship between the junction temperature and the V_{ge} voltage is used to express the junction temperature of the device, directly in terms of corresponding voltage.

Using this temperature – voltage relationship, a window comparator is used to set the two temperature limits in terms of voltages. A high current passed through the IGBT controls the heating of the device. Power dissipated in the IGBT is maintained constant during this time using a feedback loop. The relationship between the junction temperature (T_j) and V_{ge} is measured and utilized at very low current (2 mA) to avoid self-heating. Hence, during the heating phase of the module, the device current is lowered to 2 mA, so that V_{ge} (and thus T_j) is measured for a very short duration (in µs), and then the heating continues. This measured V_{ge} is stored using a sample-and-hold IC until the next measurement.

The Z_{th} of the die attach layer is measured periodically, after a certain number of cycles, using the below equation.

$$Z_{th} = \frac{\Delta V_{ge}}{kP}$$

Here, the change in V_{ge} (ΔV_{ge}) is calculated by measuring V_{ge} before heating and after heating by applying power P. The k-factor denoted by 'k' is obtained from the characterized relationship between V_{ge} and T_j. The criteria for the failure of the die attach joint is a 20% change in the Z_{th} value.

NI USB-6211 hardware and NI LABVIEW software are used to remotely control this entire setup using a PC. The LabVIEW interface on the computer makes controlling and monitoring the setup quite user friendly. The software displays in real time, the number of completed power cycles, time taken for each cycle, measured Zth and other related information, on the computer screen.

The power cycling of the IGBT modules is affected by the temperature limits as well as the frequency of cycling. One of the suggested set of parameters in JEDEC standard JESD-A122 is used. An IGBT module is cycled between 40°C and 100°C at the frequency of 6 cycles per hour. As seen in the above plot (Fig. 3), it was observed that the sample under test failed at 1700 power cycles.

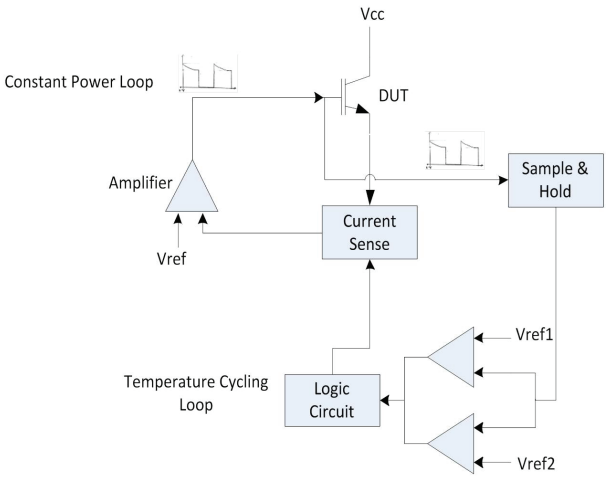


Fig. 1. Block diagram of the system for power cycling

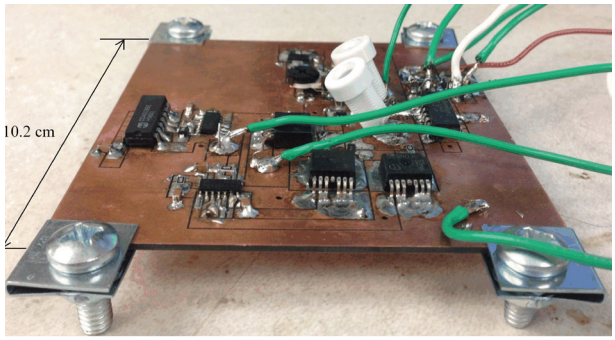


Fig. 2. K factor for IRG4CH30K at 2mA ICE

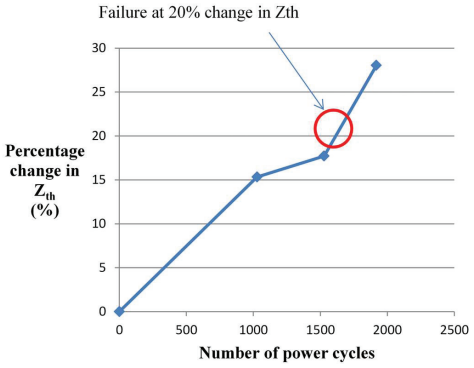


Fig. 3. Plot of % change in Zth vs number of power cycles.

Inductor Geometries with Significantly Reduced Height

The average energy density is low in commercial inductors since the flux density distribution throughout the volume is not constant. The core volume is filled by a large space with little energy, which suggests very low flux density and a magnetic material that is not fully utilized.

Figure 1. (a) A commercial inductor with 2.2 μH inductance and 4 mm packaging height; (b) axi

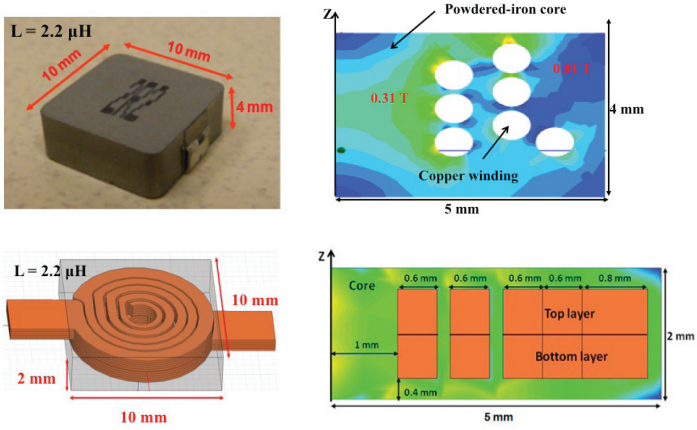


Figure 1. (a) A commercial inductor with 2.2 μH inductance and 4 mm packaging height; (b) axisymmetric view of the commercial inductor showing unevenly dis-tributed flux density inside the core; (c) 3D structure of a constant-flux inductor; total thickness is reduced by half to 2 mm, whereas inductance is kept at the same 2.2 μH; (d) relatively uniform distribution of flux density in the core of the con-stant-flux inductor.

symmetric view of the commercial inductor showing unevenly dis-tributed flux density inside the core; (c) 3D structure of a constant-flux inductor; total thickness is reduced by half to 2 mm, whereas inductance is kept at the same 2.2 μH; (d) relatively uniform distribution of flux density in the core of the con-stant-flux inductor.

The constant-flux inductor introduced herein has the windings configured to distribute the magnetic flux uniformly throughout the magnetic volume to obtain a higher energy density and a smaller package volume. A relatively constant flux distribution is advantageous not only from the density standpoint, but also from the thermal standpoint via the reduction of hot spots, and from the reliability standpoint via the suppression of flux crowding. Therefore, the volume of the inductor can be reduced significantly, whereas the inductance and dc resistance remains the same.

Following the design procedure introduced in the paper, an example inductor was designed and fabricated using the milling method. The measurement results for the designed inductor prototype demonstrate that the constant-flux concept reduced the inductor volume by more than 60%. A commercial inductor with slightly less inductance and 25% less dc resistance would be three times as large as the constant-flux inductor. If the constant-flux inductor were designed for dc resistance of 6 m , it would be 2.5 times smaller than the commercial product.

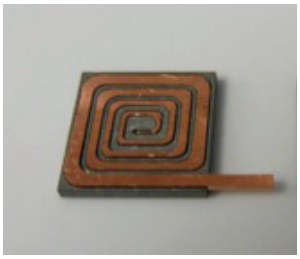


Figure 2. Prototype of milled core and milled copper winding.

TABLE II MEASUREMENT RESULT OF CFI

	CFI	Commercial
Measured L	1.42 μH	1.36 μH
Measured DCR	8 mΩ	6.0 mΩ
Volume	10 × 10 × 2 mm³	13 × 13 × 3.5 mm³

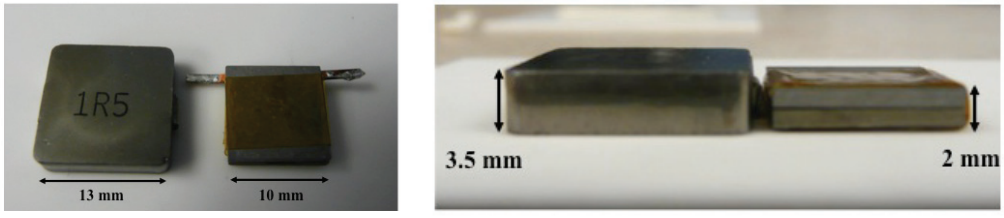


Figure 3. Dimension comparison between constant-flux inductor and a commercial inductor from Maglayers MMD-12CE-1R5M-V1.

Integrated Current Sensor using Giant Magneto Resistive (GMR) Field Detector for Planar Power Module

Conventional wire-bonded power modules show limitations for high power applications mainly because of their poor thermal-management capability. Planar power modules are a promising packaging alternative for high power applications thanks to their lower parasitic inductance, lower thermal/electrical resistance, and double-sided cooling capability. Integration of over-current protection circuit into a planar power mod-ule has been a challenge due to the limited space available. Thus, a proper current-sensing method suitable for planar power module has to be identified. Several current-sensing methods were reviewed based on the following parameters:

- High bandwidth
- High reliability
- Compact size
- Consistent measurement over wide range of temperature
- Repeatable packaging process
- Low extra cost for integration

The bandwidth of the sensor should be high enough to sense at the switching frequency of the current. The sensor should be durable considering the application of the planar module is the automobile. The coolant temperature of the automobile is usually 105°C, and the ambient temperature seen by the current sensor is even higher by the influence of the additional power loss from switching devices. The consistent measurement capability over a wide range of operating temperatures is important in order to integrate the current sensor into the module. Above all, the compact size of the sensor is important to truly integrate a current sensor into the module. Some current-sensing methods are reviewed based on the above parameters, and categorized according to their characteristics. After a detailed review, the GMR sensor was chosen as an integratable current-sensing method.

As mentioned earlier, the GMR sensor in the planar module is highly influenced by the change of junction temperature. The measurement error that came from the varying ambient temperature was experimentally measured, and the measurement result is shown and analyzed in the paper. The GMR sensor is a magnetic-field detector, so the magnetic-flux distribution of the planar power module had to be very carefully analyzed. The paper also shows the magnetic-flux distribution based on the finite-element analysis (FEA) using Maxwell 15, as well as the optimum location of the GMR sensor in the planar power module. Based on the simulation result, a test board was fabricated as designed, including the GMR sensor on top. Preliminary measurement results of the GMR sensor contained excessive noise that had to be attenuated to be used for over-current protection. The design of the signal-conditioning circuit and over-current protection circuit is reported in the paper.

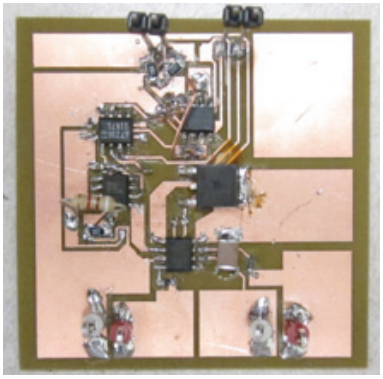
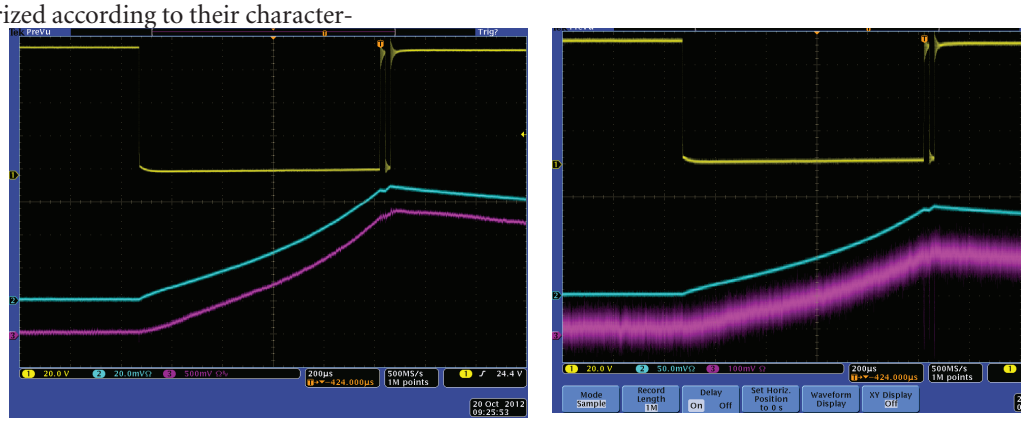


Figure 1. Fabricated test board for signal conditioning.



(a) (b)

Figure 2. (a) Output voltage of the GMR sensor. (b) Output voltage of the signal conditioning circuit

Simplification of the Nanosilver Sintering Process for Bonding Large-Area Semiconductor Chips: Reduction of Hot-Pressing Temperature below 200°C

Die-attach by low-temperature sintering of nanoparticles of silver is an emerging lead-free joining solution for electronic packaging because of the high thermal/electrical conductivity and high reli-ability of silver. For bonding small chips, the attachment can be achieved by a simple heating profile under atmospheric pressure. However, for bonding chips with an area larger than 1 cm2, an external pressure of a few Mpa's is reported necessary at the sintering temperature of about 250°C. This hot-pressing process in excess of 200°C can add significant complexity and costs to manufacture and maintenance. In this study, we ran a fractional factorial design of experiments aimed at lowering the temperature at which pressure is required for the die-attach process. In particular, we examined the feasibility of applying pressure during the drying stage of the process at temperatures below 180°C followed by the sintering stage without pressure. The experiments helped to identify the importance and interaction of various processing parameters, such as pres-sure, temperature and time, on the bonding strength and microstructure of sintered nanosilver joints. Furthermore, the positive effect of pressure applied during drying on the bonding quality was demonstrated. The relationships between die-shear stress, microstructure of sintered silver joint and applied pressure during drying stage are shown in Fig. 1. Based on the results, a sim-pler process, consisting of pressure-drying at 180°C under 3 MPa pressure, followed by sintering at 275°C under atmospheric pressure was found to produce attachments with die-shear strengths in excess of 30 MPa.

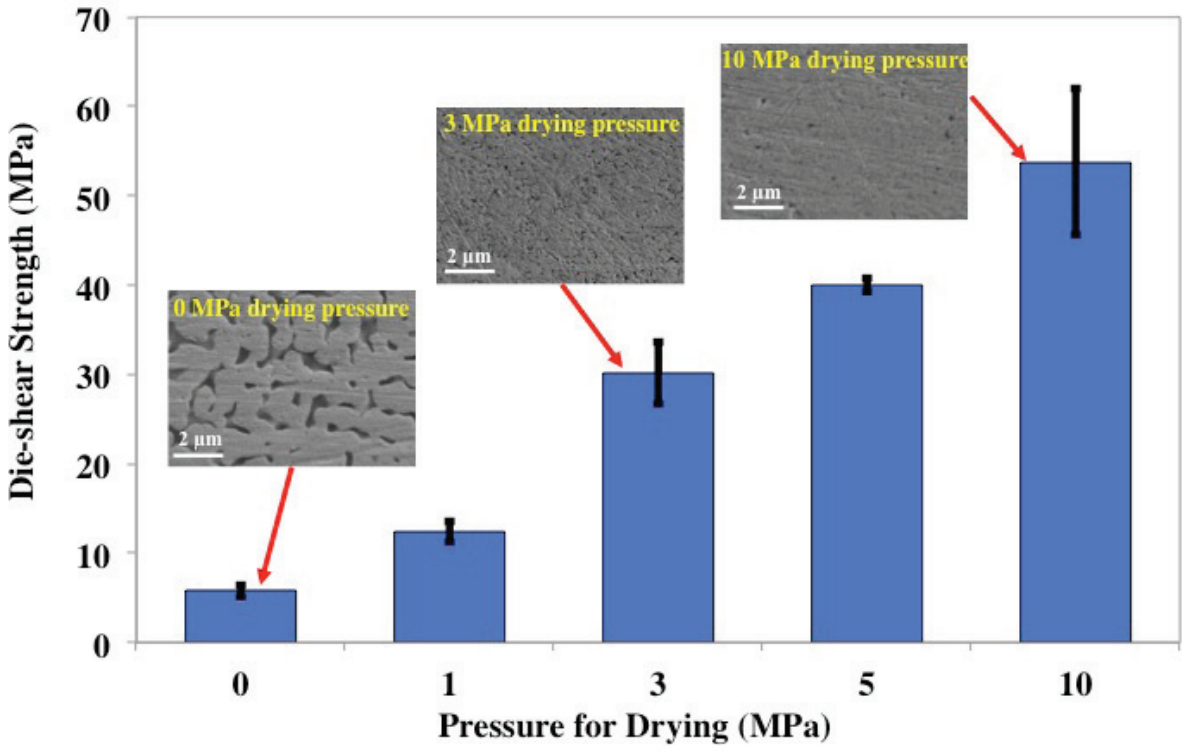


Fig. 1 Relationship between die-shear strength and pressure of drying for 10 x 10 mm2 large area die-attachments. Inset figures are SEM images showing the microstructures of sintered silver un-der corresponding drying pressures.

Low Temperature Joining Technique of Die-attachment by Silver Sintering

Two different brands of silver pastes, nanoTach and Ablestik SSP2000, were used to demonstrate the low-temperature joining technology (LTJT) by silver sintering for die-attachment. In this study, the bonding qualities such as the void percentage of attachment layers and die-shear strength, are evaluated. X-ray images of the sintered nanoTach and Ablestik SSP2000 silver lay-ers show that the void percentages were 2% and 1%, respectively. It indicated that the coverage of these sintered silver layers was much better than traditional solder layers, of which void per-centages were around 15%. The die-shear strength of nanoTach sintered die-attachments was 29.8±5.7 MPa, and that of Ablestik SSP2000 sintered die-attachments was 15.7±4.0 MPa. Comparing to traditional solders, nanoTach silver paste offers a comparable bonding strength, and Ablestik SSP2000 silver paste offers a lower bonding strength. The microstructures of sintered silver in the attachment layers are also studied in order to further understand the perfor-mance of sintered silver attachments. As shown in Fig. 1 (a) and (b), both the cross sections and failure surfaces of the sintered silver layers by nanoTach and Ablestik SSP2000 exhibit porous structures. Using SEM, the thicknesses of sintered silver layers are measured. The nanoTach and Ablestik SSP2000 silver pastes shrank 62% and 28% in thickness, respectively. The higher shrinkage of the nanoTach silver paste leads to a higher relative density in the sintered silver lay-er when compared to the Ablestik SSP2000.

The microstructures of failure surfaces of nanoTach sintered silver show remarkable plastic deformation regions, which coincides with the die-shear testing results that show that the nanoTach sintered silver layers have a higher strength than the Ablestik SSP2000 sintered silver layers. Other than die-shear strength, the measurement of the transient thermal impedance shows that when compared to the SN100C solder die-attachments, the nanoTach and the Ablestik SSP2000 sintered silver die-attachments exhibit 18% and 13% lower thermal impedance with a 40 ms heating pulse, respectively.

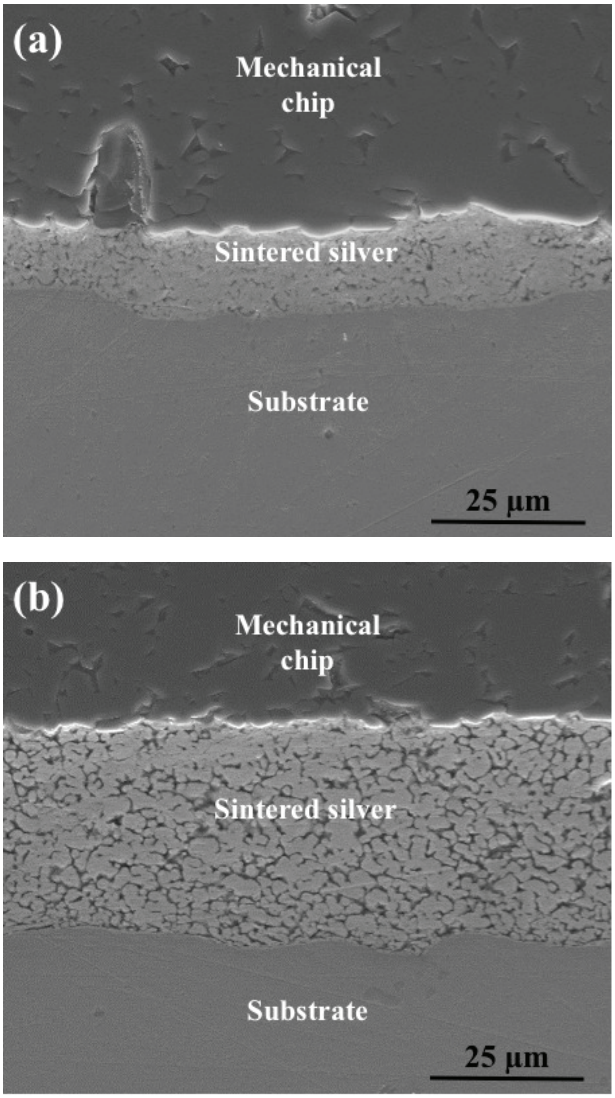


Fig. 1. SEM image of cross-sectioned silver attachment layer sintered by (a) nanoTach silver paste and (b) Ablestik SSP2000 silver paste

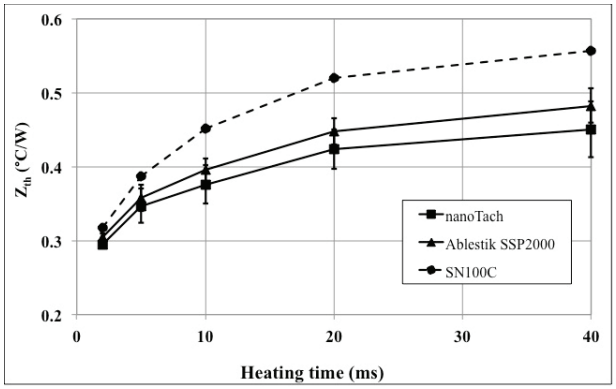


Fig. 2. Thermal impedance of samples with different die-attach materials

Fabrication of a Double-side Cooled, High Temperature Power Module with Sintered Nanosilver Interconnect for Automotive Applications

One way to reduce the cost of future electric vehicles is to eliminate the extra cooling loop by developing reliable high-temperature power inverter modules that can be cooled directly from the radiator coolant. Wide band gap (WBG) devices, like SiC or GaN, will operate at higher tempera-tures but these devices are still in the early stages of development and cost is still a barrier to integration. Power packaging technologies that can enable silicon power semiconductor devices to reliably work at junction temperatures in excess of 175°C present the best solution. In our re-search effort, we focused on the design and fabrication of a thin planar structure that utilizes the emerging low-temperature joining technology (LTJT) of nanosilver paste in order to maximize the surface area for cooling from both sides and enable reliable high temperature operation of the power semiconductor devices.

Solder alloys generally have low electrical and thermal conductivity, and are unreliable when cy-clic loaded. As operating temperatures approach melting points joint reliability worsens. By utiliz-ing the emerging low-temperature joining technology (LTJT), which is based on the sintering of silver powders, the die interconnect thermal and electrical properties can be enhanced. In addition, several leading European manufacturers of power modules have demonstrated a significantly improved performance and reliability of power modules interconnected by the LTJT technology over the soldering technology. However, a barrier for implementing the technology has been the requirement of pressure, 10 to 40 MPa or 100 to 400 kg-force on a 100 mm2 chip, to lower the silver sintering temperature from over 700°C down to about 250°C. This limits production throughput, complicates the manufacturing process, and places critical demands on substrate flatness and thickness of the chips.

For this research we utilize a newly designed nanosilver paste that can be sintered with zero or pressure less than 5 MPa for speeding up the LTJT implementation. Reduction of pressure coupled with the lower sintering temperatures allows for the manufacture of more intricate geometries. In this study, we focused on making a quarter-bridge module consisting of one IGBT in parallel with one diode. Module schematics of the proposed quarter bridge circuit utilizing a top and bottom DBC substrate can be seen in Figure 1. The quarter bridge circuit can easily be combined with other units for a full inverter package and the double-side design is ideal for integration and thermal management. In this paper, we report the use of this enabling nanomaterial for successful fabrication of planar, double-side cooled quarter bridge power modules.

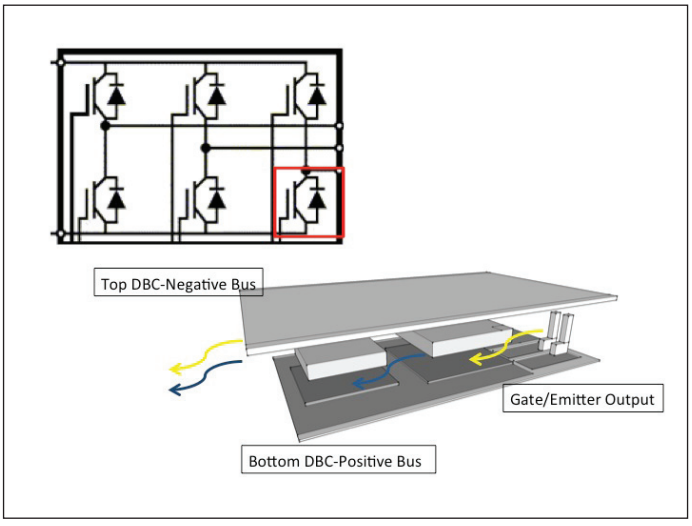
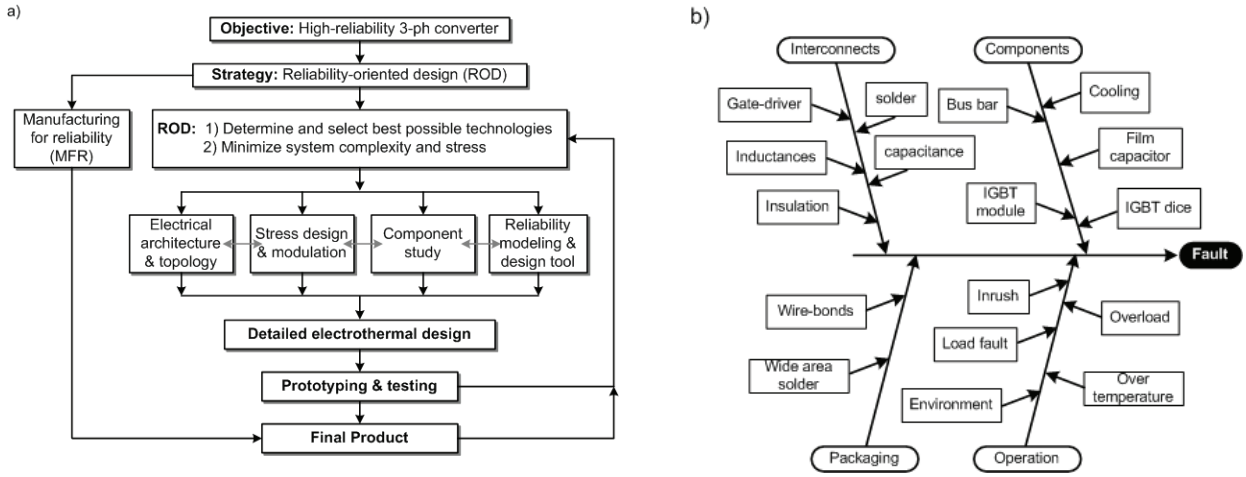


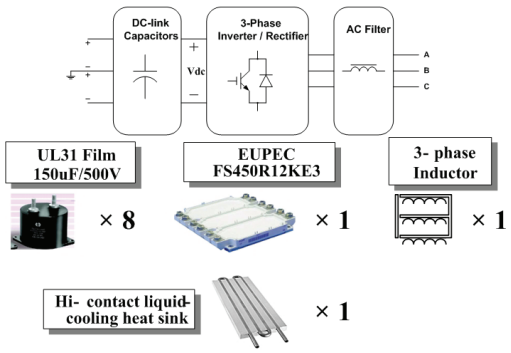
Figure 1: Schematic design of a planar, double-side cooled quarter-bridge power module.

Reliability-Oriented Design of Three-Phase Power Converters for Aircraft Applications

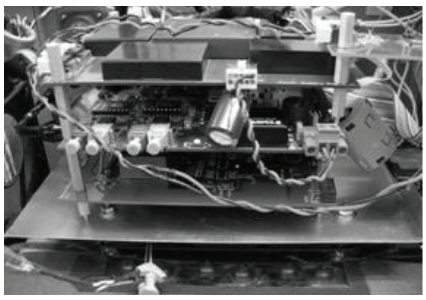
Aircraft applications require the highest reliability levels for all system components; hence the need to maximize the reliability of three-phase power converters, which are in increasing demand and use in commercial and military aircrafts as a result of the more-electric aircraft initiative. Addressing this need, the proposed procedure takes reliability up-front in the design process of power converters, carrying out the design in three steps. First, the identification of critical system components; second, the assessment of reliability factors such as risk analysis, failure mode analysis, and fishbone diagrams; and third, the actual design, which is carried out by minimizing system complexity and stress, and by the use of the most reliable components, materials and structures. To this end, reliability models were developed for all critical components based on the military handbook MIL-HDBK-217F, and field and vendor data. For verification purposes, the reliability-oriented design of a 60 kW three-phase power converter for aircraft applications is included together with experimental results of the prototype constructed.



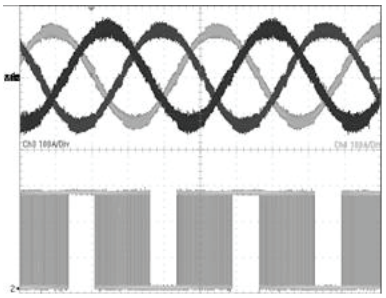
(a) Block diagram of reliability-oriented design (ROD); (b) fish-bone diagram of power converter (example).



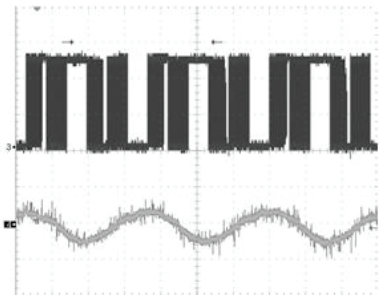
Proposed design for the power stage of the converter.



(a) Prototype liquid-cooled converter and (b) its controller



(a)



(b)

(a) Converter operating at 53 kW with discontinuous SVM and deadtime compensation; waveforms depicted at 4ms/div; Top trace: line currents (100 A/div); Bottom trace: IGBT voltage (200 V/div). (b) Voltage and current waveforms with low current at 4 ms/div are: Top trace: IGBT voltage (200 V/div); Bottom trace: line current Ia (10 A/div).

Physics-Based Analytical Model for High-Voltage Bidirectional GaN Transistor Using Lateral GaN Power HEMT

Figure 1 shows the schematic representation of a bidirectional transistor consisting of two discrete switches. This circuit was realized with a commercially available 200V, 3A GaN HEMTs (EPC-2012) laid out on a PCB. The constituent transistors were fully characterized, then modeled using Statz' GaAs JFET model as a reference. Figure 2 demonstrates the accuracy of the model compared to experimental data. The model shows a very good correlation to the experimental results all the way up to 125°C.

Next, the bidirectional switch was simulated using the model developed for the con-stituent transistors, its output I-V compared to experimental results is detailed in Figure 3.

Finally, the bidirectional transistor was used to switch 100V at 3A with a switching speed of 21ns. In addition, it exhibited an on-state resistance of only 114m and a blocking voltage of 200V in both polarities with the gate voltage equal to 0V!

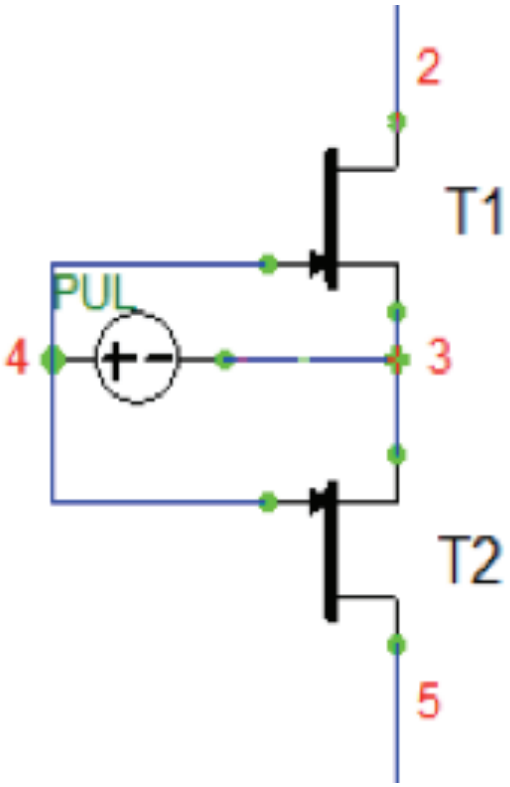


Figure 1 Schematic representation of bidi-rectional switching GaN transistor. Nodes 2 and 5 are the drains of transistors T1 and T2 respectively. Node 3 connects the source of T1 and T2. Node 4 is the gate for T1 and T2.

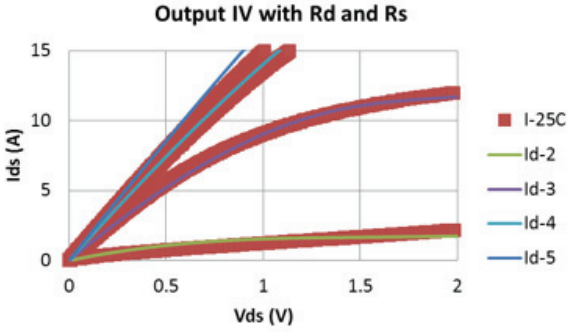


Figure 2 Model for EPC 2012 (solid lines) versus data (■) in the first quadrant at 25°C and VG from 2 to 5V

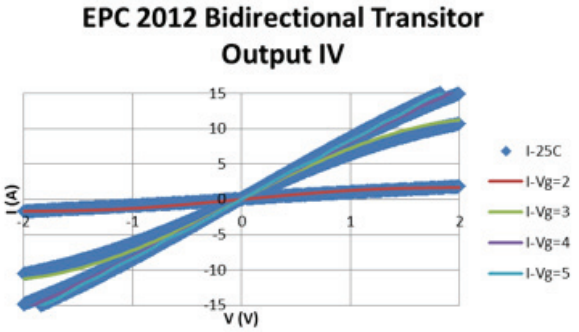


Figure 3 Model for EPC 2012 (solid lines) versus data (◆) in the third quadrant at 125C and gate voltages from 2V to 5V

Evaluation of Commercial SiC and GaN Devices using Full Bridge Inverter Simulation

Figure 1 shows the schematic of the full bridge inverter circuit topology used for SPICE simulations. It consists of four switches (S1-S4) and four anti-parallel diodes (D1-D4). This type of circuit is typically used to drive inductive loads such as motor drives, represented here using an inductor with a series resistance. The switches are typically driven through a gate drive circuit, simulated here using a pulsed voltage source. The SPICE simulation is performed for an all SiC and all GaN circuit and compared with an all Si based circuit. For the SiC based circuit, SPICE models for the 1200V SiC DMOSFET from Cree Inc. were used. A SiC Schottky model devel-oped by us for a 600V SiCED SiC Schottky was used for the antiparallel diode. For the GaN based circuit, a SPICE model for a lateral 200V GaN HEMT from EPC was used, and a GaN Schottky model developed by us was used for the antiparallel diode. The GaN HEMT was simu-lated as three devices in series to simulate the increased conduction losses for an equivalent 600V device. Bus voltage of 600V was used and the load was adjusted to get a load current of 10A. A duty cycle of 50% was used for the gate drive voltage sources and a dead time was introduced between the voltage sources in the same branch so as not to short the bus voltage to ground due to the finite rise and fall times of the voltage sources. The gate voltage for the SiC MOSFET was switched from 0V to 20V and the gate voltage for the GaN HEMT was switched from 0V to 5V, since the gate turns on beyond 5V.

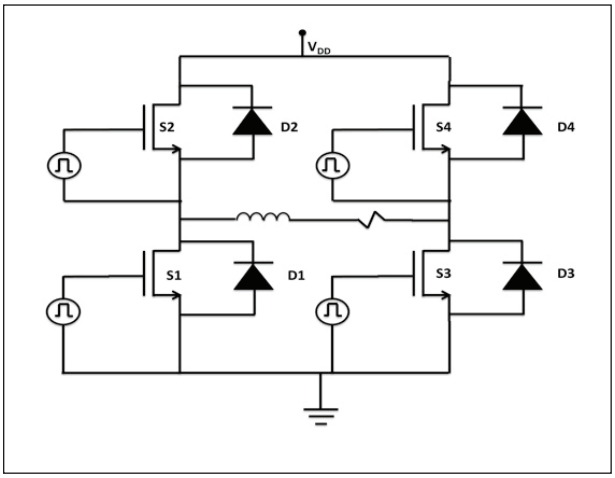


Fig. 1 Full Bridge inverter circuit topology.

The efficiency of the circuit was measured by calculating all the losses in the switches, diodes and gate drives. The efficiency of the GaN is higher at higher frequencies than the SiC and drops off less slowly compared to the SiC. This performance improvement in the GaN at high frequen-cy is largely due to the lateral structure of the GaN device. SiC MOSFET is a vertical device and hence has larger gate-drain overlap capacitances when compared to a lateral device.

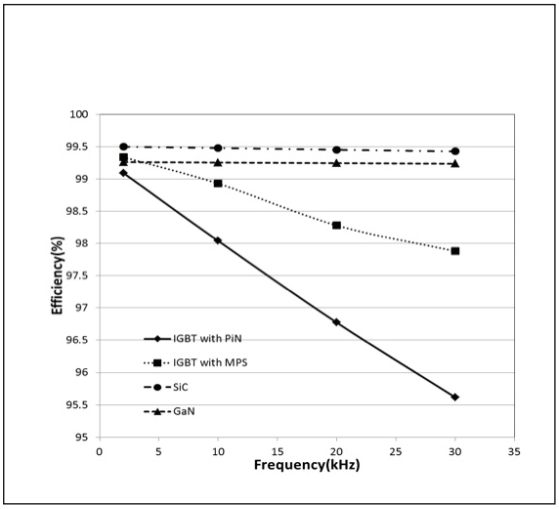


Fig.2 Efficiency comparison at low frequencies.

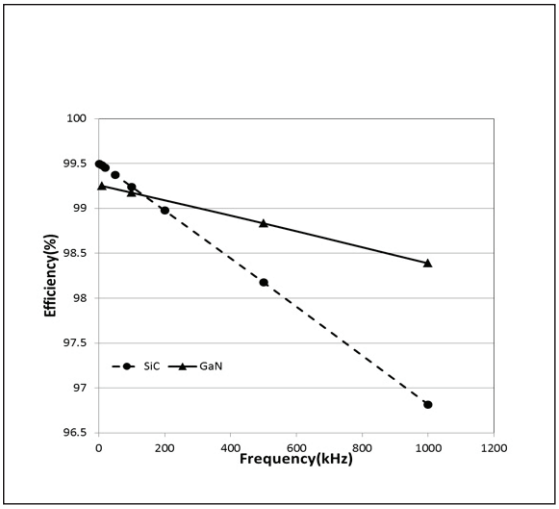


Fig.3 Efficiency comparison at high frequencies.

Monolithic Optoelectronic Integration of GaN High-Voltage Power FETs and LEDs with a Selective Epi Removal Process

This paper presents a novel approach to merge these two promising technologies into a monolith-ically integrated Light Emitting Power IC (LEPIC), extending the functionalities of LEDs enabling them to be embedded into smart lighting systems.

Monolithic optoelectronic integration increases the maximum modulation frequency by lowering the parasitic inductance at least two orders of magnitude when compared to a discrete packaged LED and power FET. We employ a lateral, enhancement-mode MOS-Channel-HEMT (MOSC-HEMT) as the power transistor in combination with a quasi-vertical LED all on one substrate.

The Selective epi Removal (SER) approach employs the growth of the epi for the LED on top of the epi layers for electronic devices, as shown in Figure 1. Then it selectively etches the epi layers away to process the GaN electronics, allowing devices to share common epi layers and thus, saving processing costs. SER also eliminates the need to implement any epi re-growth steps, saving fabrication time. SER enables the emitted light to be extracted from either the top or the bottom of the LEPIC. The first full integration of a GaN LED and MOSC-HEMT is underway; however, the process has been validated with a short loop MOS capacitor lot. The two largest technical barriers with this approach are: 1) not compromising the quality of the electronic epi during the LED epi growth and 2) removing all of the LED epi in the areas where FETs are to be fabricated, without over-etching. The short loop MOS capacitor experiment was designed to verify that both of these barriers can be overcome.

To confirm the growth of the LED epi did not substantially affect the electronic epi, the 2DEG concentration was measured using a MOS capacitor on two samples, one without LED epi growth, and one with LED epi growth. After the LED epi was grown, half the sample was masked off, and the other half was etched down to expose the electronic epi. In this area, MOS capacitors were fabricated. If the bottom layer of the LED was not removed, the MOS capacitor would not be able to be depleted. If the thin electron generating layer was removed by an over etch, the MOS capacitor would be depleted too easily. The 2DEG concentration of the sample without LED epi was 3.2e12/cm^2 while the sample with LED epi was 3.0e12/cm^2, see Figure 2 and 3. These results confirm that the LED growth cycle was not detrimental to the electronic epi, and that the etch depth can be controlled well enough to isolate the MOSC-HEMT epi from the LED epi. We are in the process of making prototype circuit building blocks which integrates high-voltage MOSC-HEMTs and LEDs.

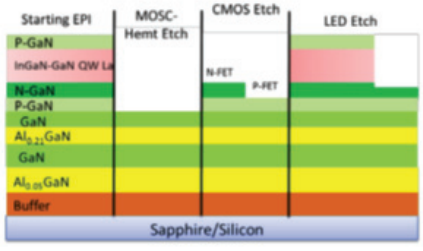


Figure 1 Selective epi removal showing layers for GaN power transistor, logic and LED

Fig. 1 Selective epi removal showing layers for GaN power transistor, logic and LED

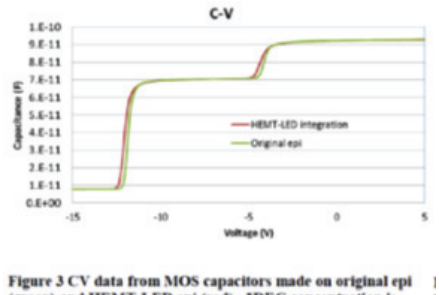


Figure 3 CV data from MOS capacitors made on original epi (green) and HEMT-LED epi (red). 2DEG concentration is measured by the integration of C where it is plateaued from ~-5V to -12V from the depletion of 2DEG.

Fig. 2 CV data from MOS capacitors made on original epi (green) and HEMT-LED epi (red). 2DEG concentration is measured by the integration of C where it is plateaued rom ~-5V to -12V from the depletion of 2DEG.

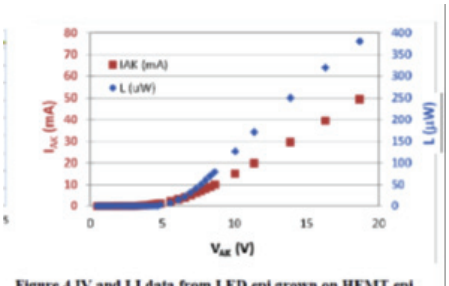


Figure 4 IV and LI data from LED epi grown on HEMT epi. Results taken before fabrication with the use of Indium Schottkycontacts

Fig. 3 IV and LI data from LED epi grown on HEMT epi. Results taken before fabrication with the use of Indium Schottkycontacts

Investigation of Pyroelectric Polarization Effect On GaN MOS Capacitors and Field-Effect Transistors

Due to asymmetry of the wurtzite crystal structure, a 2H-GaN exhibits strong lattice polarization effects. At high temperatures, the GaN is capable of generating electric charges in response to the heat flow. This pyroelectricity would lead to much bigger temperature dependence of the flatband voltage and threshold voltage for GaN MOS capacitors and transistors when compared with Si devices.

We prepared both GaN MOS capacitors and MOSC-HEMTs on different substrates. One of the capacitor samples was fabricated on a commercial (0001) UID GaN epitaxial layer grown by MOCVD on sapphire substrate, while the other was on a bulk GaN substrate. PECVD SiO2 was deposited, followed by a 30 min. anneal at 1000°C in N2. Then 500nm of Al was used to form contacts. The three MOSC-HEMTs have the same device structure except for its epi. They were fabricated on 30nm UID Al0.22Ga0.78N on 3μm UID GaN on sapphire substrate (MOSC-HEMT 1), 20nm UID GaN cap on 20nm UID Al0.25Ga0.75N on GaN buffer on Si (111) substrate (MOSC-HEMT 2), and 22nm UID Al0.23Ga0.77N on UID GaN on bulk GaN (MOSC-HEMT 3). ICP etch was used to remove the AlGaN layer as well as the 2DEG in the channel in order to get enhancement-mode devices. Wet etch was done right afterwards to remove surface damages. 100nm PECVD SiO2 was deposited on MOSC-HEMT 1 and 3, while 50nm on MOSC-HEMT 2, followed by 30 min annealing at 1000°C in N2. Ti/Al was deposited and annealed at 400°C for 15min for n+ ohmic contacts. We measured the Capacitance-Voltage characteristics of the two capacitors from 23°C to 150°C, and the I-V for the MOSC-HEMTs from 23°C to 250°C. The flatband voltage shifts positively with increasing temperature, which gives us a pyroelectric voltage coefficient of 7.4×10^-4 V/mK and 8.5×10^-4 V/mK for sapphire and bulk GaN substrate. We fit the experimental plots with the piezoelectric constants given by F. Bernardini [3] and the lattice parameters in Table I, as shown in Fig. 1. Since the calculated ideal bulk GaN (without lattice mismatch) curve does not fit the experimental value, we estimate the lattice mismatch to be 50%. The threshold voltage shift for MOSC-HEMT in Fig. 2 seems more complex than the capacitors since we are measuring the current across the channel, instead of directly measuring the induced charge. We attribute the differences to the change of interface traps and mobile charges with increasing temperature.

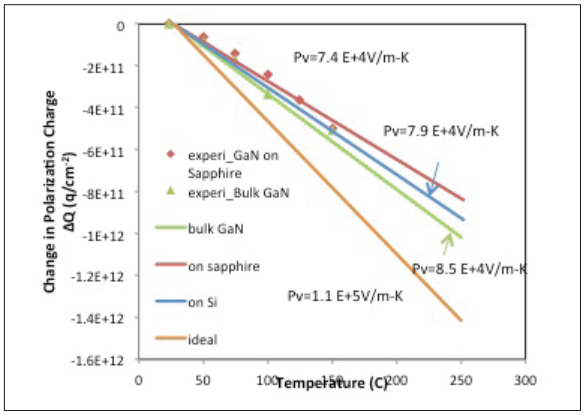


Fig. 1 Polarization charges vs. Temperature for GaN capacitors on different substrates

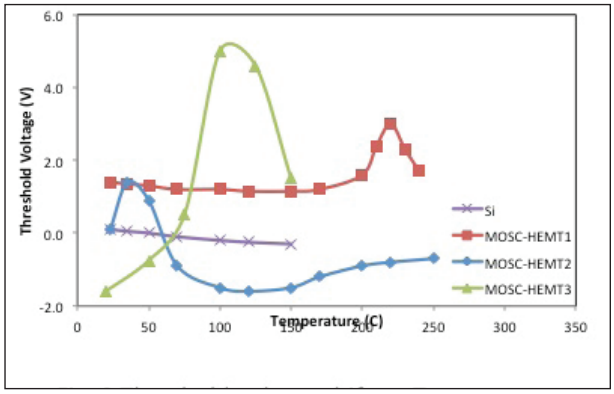


Fig. 2 Threshold voltage shift vs. Temperature for GaN MOSC-HEMTs on different substrates

Table I. Lattice parameters and thermal expansion coefficients for calculation

Material	a at 300K (A)	c at 300K (A)	Thermal expan. coeff. of a (×10↑−6)	Thermal expan. coeff. of c (×10↑−6)
GaN	3.19	5.19	5.59	3.17
Sapphire(30°)	2.75	7.51	2.80	3.20
Si(111)	3.84		2.60	

Table I. Lattice parameters and thermal expansion coefficients for calculation

Estimate of Avalanche Breakdown Voltage in 4H-SiC

Published impact ionization coefficients of (0001) 4H-SiC are used to fit a power-law-approximated effective impact ionization, which is accurate in the range of electric field strengths from 1.5 to 5MV/cm. This power law approximation is used to generate 1D equations for critical electric field, avalanche breakdown voltage, and depletion layer width of 4H-SiC devices as a function of doping concentration. One-dimensional avalanche breakdown of 4H-SiC Schottky diodes was simulated for various epi layer doping levels, to evaluate the fidelity to these and other published 1D breakdown equations. Our (RPI) equations best fit the Schottky diode simulation and correlate well with published 4H-SiC device results.

Measured sets of impact ionization coefficients have been published for the 4H-polytype of Silicon Carbide, as well as approximated sets of 1D breakdown equations for calculation of drift layer requirements for design of SiC power devices. This type of equations is useful as a starting point in new device design, and so having accurate analytical equations are important for development of new device structures. Fidelity of these equations with simulation using accepted ionization coefficients and with published experimental device results can be used to compare and contrast the accuracy of these analytical approximations.

A power law relationship was fit to accepted impact ionization coefficients, as shown in Fig. 1. The fitted equation for ionization rate as a function of electric field is given in equation (1). This relationship approximates the published impact ionization coefficients well for electric fields of 1.5 to 5MV/cm. Solving the ionization integral using this relationship leads to 1D equations (2), (3), and (4).

$$\gamma_a = 1.746\times10\text{-}35\times E6\ [\text{cm-}1] \quad (1)$$

$$Ec = 1.333\times104\times ND1/7 \quad (2)$$

$$BVpp = 4.766\times1014\times ND\text{-}5/7 \quad (3)$$

$$WD,pp = 7.151\times1010\times ND\text{-}6/7 \quad (4)$$

4H-SiC Schottky diodes were simulated with varied doping concentrations, using the Konstantinov impact ionization coefficients. Our equations show strong fidelity to simulation, and published device results (Fig. 2, 3). As expected, physical devices lie slightly below the calculated BVPP due to termination, cell structure, etc. By contrast, other sets of previously published equations overestimate the breakdown voltage by up to 80%.

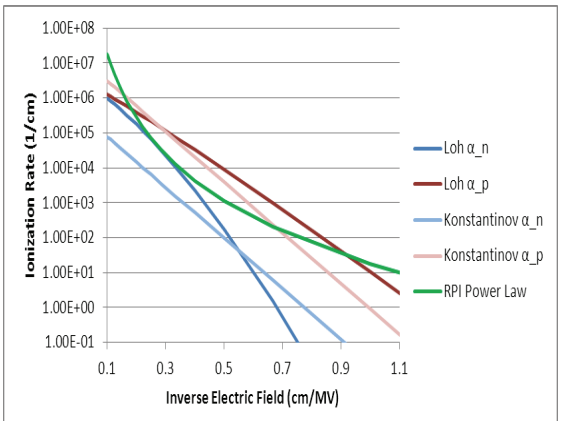


Fig. 1: Ionization Rate as a function of electric field in Silicon Carbide at room temperature.

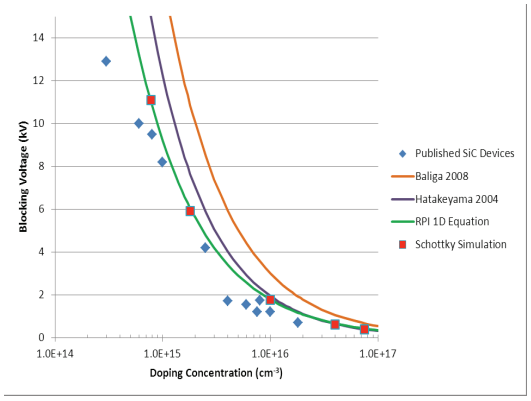


Fig. 2: Blocking voltage versus drift layer doping concentration. Schottky simulations were run using the Konstantinov impact ionization coefficients.

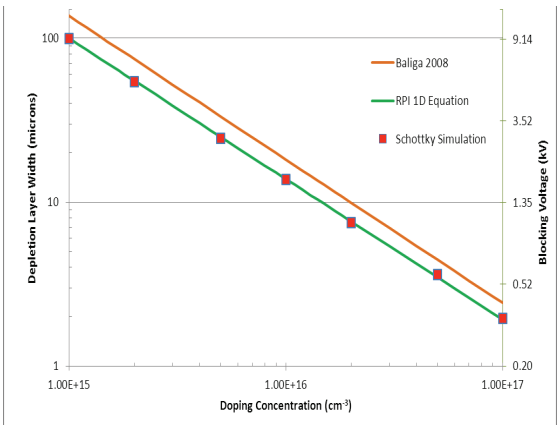


Fig. 3: Depletion layer width versus drift layer doping concentration, with non-punch-through blocking voltage on the secondary y-axis. Schottky simulations were run using the Konstantinov impact ionization coefficients.

Avalanche Breakdown Design Parameters in GaN

The breakdown voltages were obtained from simulations as a function of the low side doping for GaN p+/n and n+/p junctions, showing a power law relation (see Fig. 1). In silicon, using Fulop's approximation which assumes a power law relation between the ionization coefficient and electric field ψE^n, it can be derived that BVψN^(-(n-1)/(n+1)) with n=7. For GaN, the power n was found to be 9.2 from approximating the power law for the effective ionization coefficient (ψ_eff=(a_n-a_p)/lnψ(a_n/a_p)) vs. electric field, and n=9 was obtained from the BV vs. doping plot for both p+/n and n+/p junctions, which is higher than the previously reported value of 8. The higher n value of GaN suggests that BV decreases faster as doping increases when compared with silicon.

Next, the shapes of the avalanche breakdown I-Vs of the GaN obtained from numerical simulations were examined. The avalanche I-V was found to be sharper for GaN n+/p junctions than p+/n junctions with the same doping. Similarly to silicon, the sharpness of the GaN avalanche I-V can be measured by the factor m as in the analytical approximation =I_0/(1-(V/BV)^m), where I0 is the pre-avalanche leakage current. For silicon, m is different for different BVs, although it has been known to be 6 for p+/n junctions and 4 for n+/p junctions for simplification. The m is also related to the BV of BJTs in terms of BV_cbo/BV_ceo=ψ(1+ψ)ψ^(1/n) , and has been extracted for SiC BJTs to be around 8 to 10. We have extracted the m value as a function of BV for GaN fitting the GaN avalanche I-Vs from simulations with the analytical approximation (see Fig. 2), and got m increasing from 5.7 to 8.5 in the BV range of 1.2kV to 12kV for GaN n+/p junction; and m decreasing from 1.9 to 1.8 for GaN p+/n junction (see Fig. 3). We also obtained m by calculating the ionization integral numerically as a complementary method, and received similar results (see Fig. 3). The slight difference may be attributed to the fact that the ionization integration method lacks the field modification by the carriers in transient. Because the higher m yields a sharper avalanche I-V, GaN n+/p junction is projected to be a better choice for the main voltage blocking junction in GaN power devices.

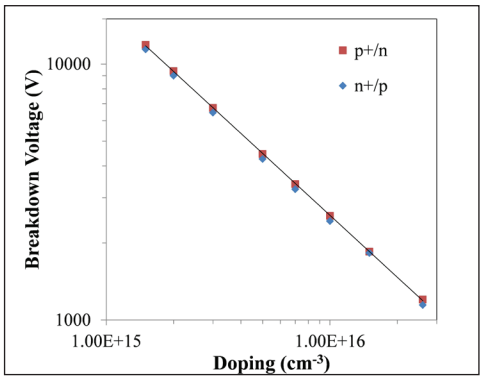


Fig. 1 Breakdown voltage vs. doping for GaN p+/n and n+/p junctions from simulations

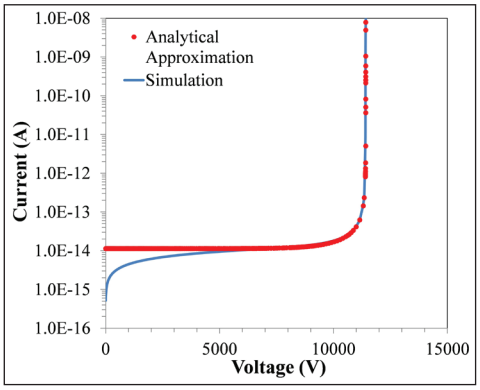


Fig. 2 Fitting of the breakdown I-V of GaN n+/p junction from simulation with analytical approximation

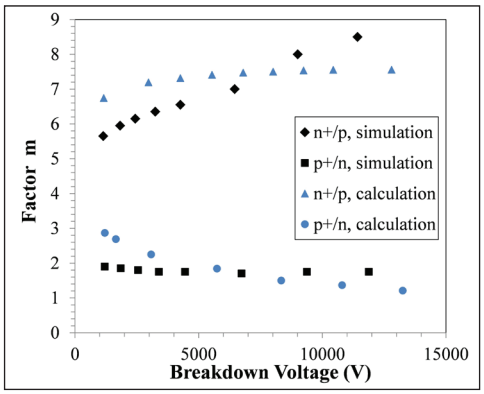


Fig. 3 Factor m vs. breakdown voltage for GaN p+/n and n+/p junctions from simulations and calculation of ionization integral

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