CPES

Center for Power Electronics Systems

ANNUAL REPORT 2015

Virginia Tech - Blacksburg, Virginia

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INTRODUCTION

The Center for Power Electronics Systems at Virginia Tech is a research center dedicated to improving electrical power processing and distribution that impact systems of all sizes—from battery-operated electronics to vehicles to regional and national electrical distribution systems.

Our mission is to provide leadership through global collaborative research and education for creating advanced electric power processing systems of the highest value to society.

CPES, with annual research expenditures of $4.5 million U.S. dollars, has a worldwide reputation for its research advances, its work with industry, and its many talented graduates. From its background as an Engineering Research Center for the National Science Foundation during 1998 - 2008, CPES has continued to work towards making electric power processing more efficient and more exact in order to reduce energy consumption.

Power electronics is the "enabling infrastructure technology" that promotes the conversion of electrical power from its raw form to the form needed by machines, motors and electronic equipment. Advances in power electronics can reduce power conversion loss and in turn increase energy efficiency of equipment and processes using electrical power. This results in increased industrial productivity and product quality. With widespread use of power electronics technology, the United States would be able to cut electrical energy consumption by 33 percent. The energy savings in the United States alone is estimated to be the equivalent of output from 840 fossil fuel based generating plants, with enormous economic, environmental and social benefits.

OVERVIEW

CPES INDUSTRY CONSORTIUM

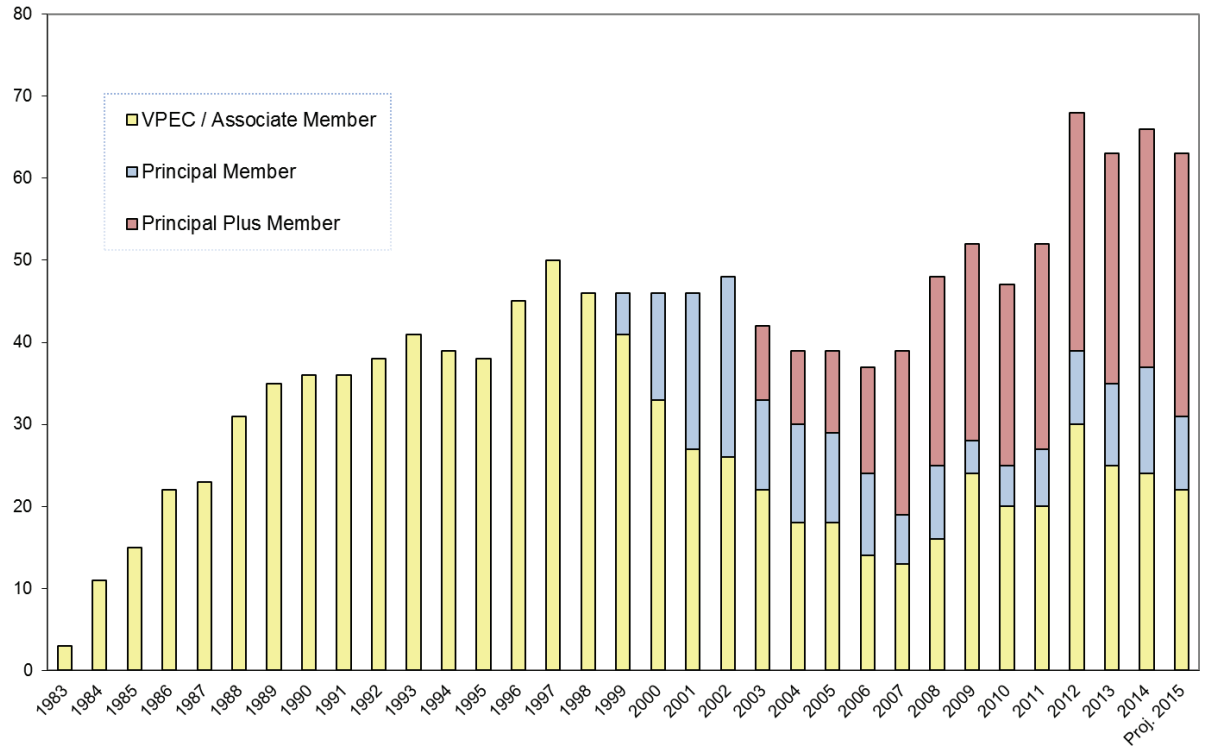
The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members. The CPES industrial consortium offers the best mechanism to stay abreast of technological developments in power electronics.

The CPES connection provides the competitive edge to industry members via:

- Access to state-of-the-art facilities, faculty expertise, top-notch students
- Leveraged research funding of more than $4.5 million per year
- Industry influence via Industry Advisory Board and research champions
- Intellectual properties with early access for Principal Plus and Principal members via CPES IPPF (Intellectual Property Protection Fund)
- Technology transfer made possible via special access to the Center's multi-disciplinary team of researchers, and resulting publications, presentations and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount
- Option to send engineers to work with CPES researchers on Campus via the Industry Residence Program.

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

CPES MEMBERSHIP COMPANY GROWTH



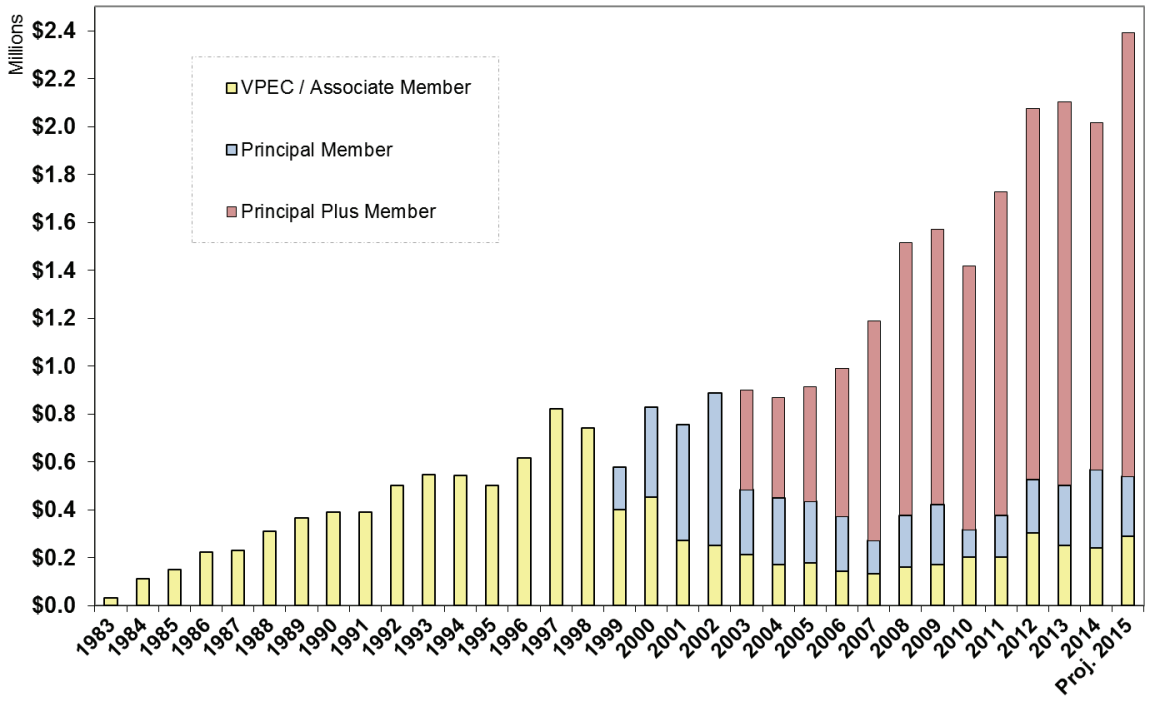
Principal Plus Members (annual contribution - $50,000) - gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research—PMC (Power Management Consortium), HDI (High Density Integration), or REN (Renewable Energy and Nanogrids). Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each. In addition to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting-edge IPs via CPES IPPF (Intellectual Property Protection Fund).

Principal Members (annual contribution - $30,000) - are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund), in addition to all the benefits offered to Associate Members.

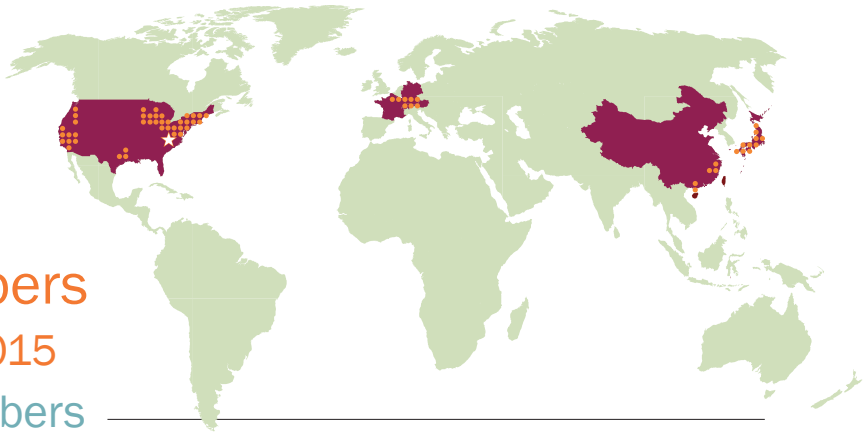
Associate Members (annual contribution - $15,000) - gain the competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short course to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the Center in technical areas that are of mutual interest, to be determined jointly with CPES faculty host.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires Center Director approval.

INDUSTRY MEMBERSHIP FUNDING GROWTH



CPES



Industry members

April 2014 - April 2015

Principal Plus Members

3M Company
ABB, Inc.
Alstom Transport
Altera - Enpirion Power
Chicony Power Technology Co., Ltd.
Crane Aerospace & Electronics
CSR Zhuzhou Institute Co., Ltd.
Delta Electronics, Inc.
Dowa Metaltech Co., Ltd.
Eltek
Emerson Network Power
GE Global Research
GE Power Conversion, Inc.
General Motors
Groupe SAFRAN
Huawei Technologies Co., Ltd.
International Rectifier
Keysight Technologies
Linear Technology
Macroblock, Inc.
Mitsubishi Electric Corporation
Murata Manufacturing Co., Ltd.
NEC TOKIN Corporation
Nissan Motor Co., Ltd.
NXP Semiconductors
Panasonic Corporation
Richtek Technology Corporation
Rolls-Royce
Siemens Corporate Research
Sonos, Inc.
Sumitomo Electric Industries, Ltd.
Texas Instruments
The Boeing Company
Toyota Motor Engineering & Manufacturing North America, Inc.
United Technologies Research Center

Principal Members

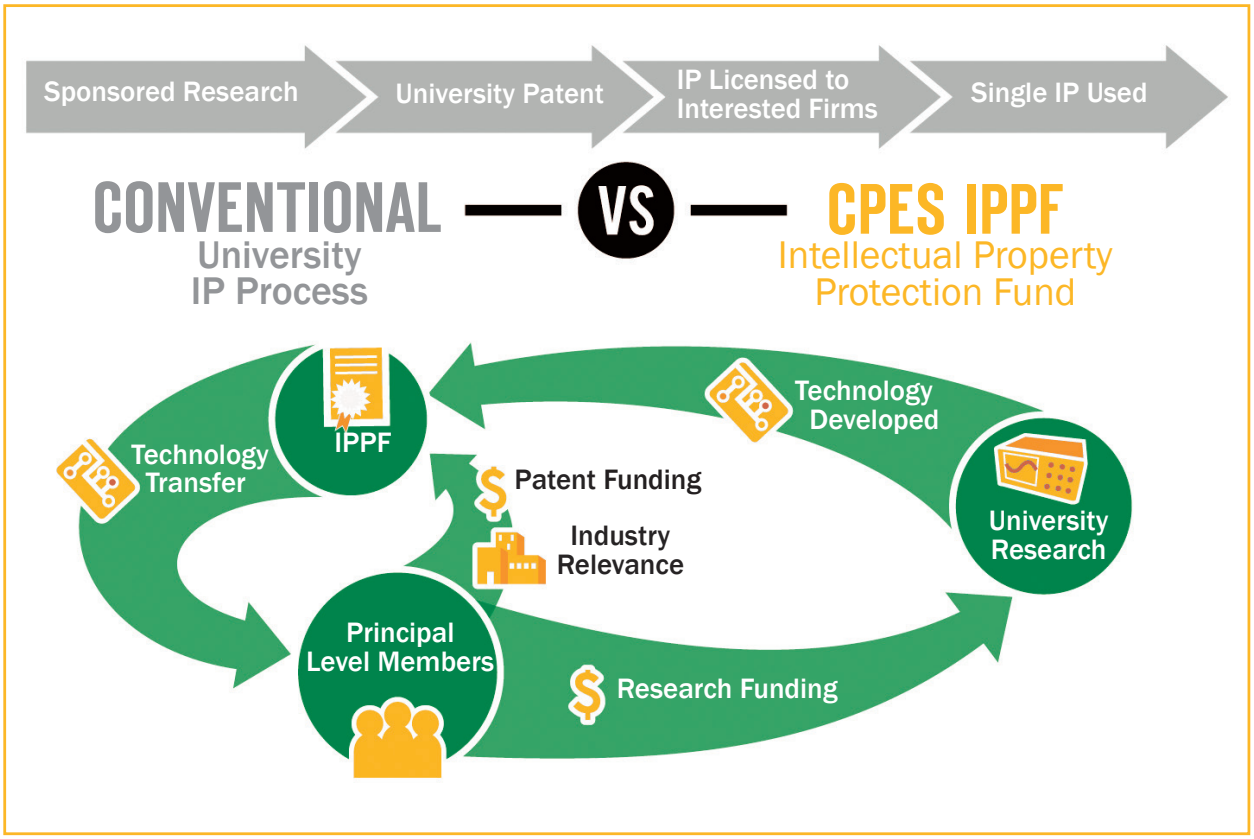
AcBel Polytech, Inc.
Analog Devices
China Nat'l Electric Apparatus Res. Inst.
Fairchild Semiconductor Corp.
Halliburton
Infineon Technologies
Maxim Integrated Products
MKS Instruments, Inc.
ON Semiconductor
Power Integrations
Toshiba Corporation
ZTE Corporation

Associate Members

Calsonic Kansei Corporation
Crown International
Cummins, Inc.
Delphi Electronics & Safety
Dyson Technology Ltd.
Eaton Corporation, Innovation Center
Efficient Power Conversion
Ford Motor Company
GHO Ventures, LLC
Inventronics (Hangzhou), Inc.
Johnson Controls, Inc.
Lite-On Technology Corporation
LS Industrial Systems Co., Ltd.
Metamagnetics, Inc.
Microsoft Corporation
NetPower Technologies, Inc.
OSRAM Sylvania, Inc.
Rockwell Automation
Schaffner EMV AG
Shindengen Electric Mfg. Co., Ltd.
Silergy Technology
TDK Lambda Corporation
Toyota Motor Corporation
United Silicon Carbide, Inc.
Universal Lighting Technologies, Inc.

Affiliate Members

ANSYS, Inc.
CISSOID
Electronic Concepts
Mentor Graphics Corporation
Plexim GmbH
Powersim, Inc.
Rohde & Schwarz
Simplis Technologies, Inc.
Synopsys, Inc.
Tektronix, Inc.
Transphorm, Inc.
VPT, Inc.



Intellectual Property Protection Fund

IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF. Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.

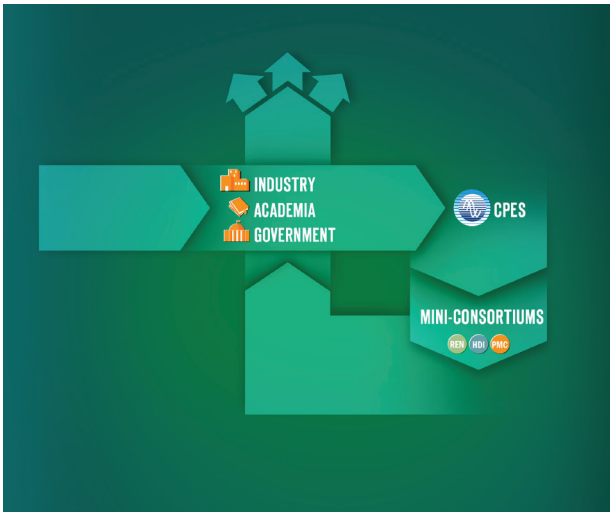
CPES Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contribution of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- PMC (Power Management Consortium)
- HDI (High Density Integration)
- REN (Renewable Energy and Nanogrids)

Companies interested in more than one focused research areas may join another mini-consortium for an additional annual contribution of $50,000 each.



Power Management Consortium (PMC)

In 1997, at the request of Intel, CPES established a VRM mini-consortium to address the issue of power management for future generations of microprocessors, targeting sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team has developed a multi-phased voltage regulator module (VRM). Instead of paralleling power semiconductor devices to meet the current demand and efficiency requirements, the research team proposed to parallel a number of mini-converters. By paralleling the mini-converters and phase-shifting the clock signal, the team was able to both cancel the significant part of the output current ripple and increase the ripple frequency by N time, where N is the number of channels paralleled. This resulted in significant demonstrated improvement—specifically:

- 4 times improvement in transient response
- 10 times reduction in output filter inductors
- 6 times reduction in output capacitors
- 6 times improvement in power density, and 3 times improvement in profile

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This mode of operation is necessary to conserve energy, and to extend the operation time for battery-operated equipment. The challenge for the voltage regulator module in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as fast as possible to the microprocessor. Today, every Intel processor is powered by such multiphased VRMs developed by CPES.

Power Management Consortium (PMC) is an outgrowth of the early VRM mini-consortium initiated in 1997. The goal is to extend its research scope with a focus on developing pre-competitive technologies in the areas of power management for distributed power system architectures, EMI/EMC, power quality, ac/dc converters, dc/dc converters, POL converters in applications including microprocessors, tablets, notebooks, desktops, servers, data centers, networking products, telecom equipment, solid state lighting, battery chargers and other industrial and consumer electronic applications.

The PMC mini-consortium has accumulated a wealth of knowledge and made significant contributions to the power management industry. Since its inception, the program has been supported by more than 30 major semiconductor and power supplies companies. PMC currently has 17 members, as shown in the image below. In the past year six new members joined the PMC, including 3M, Altera-Enpirion Power, Emerson Network Power, Eltek, Sonos Inc., and Panasonic Corp.

The PMC places a significant emphasis on developing high-efficiency, high-power density switch-mode power supplies based on recent developments in wide-bandgap power devices such as gallium-nitride (GaN) devices and silicon carbide (SiC) devices. This emphasis will be highly leveraged with the recent DOE award of "PowerAmerica." CPES is a partner in this multi-industry multi-university collaboration program for a period of five years. The CPES role is to work with the wide-bandgap (WBG) manufacturing industry to explore potential applications and impacts of GaN and SiC devices to power conversion technologies.

The proposed GaN-based research will use several test beds to demonstrate the benefit of GaN-based power converters:

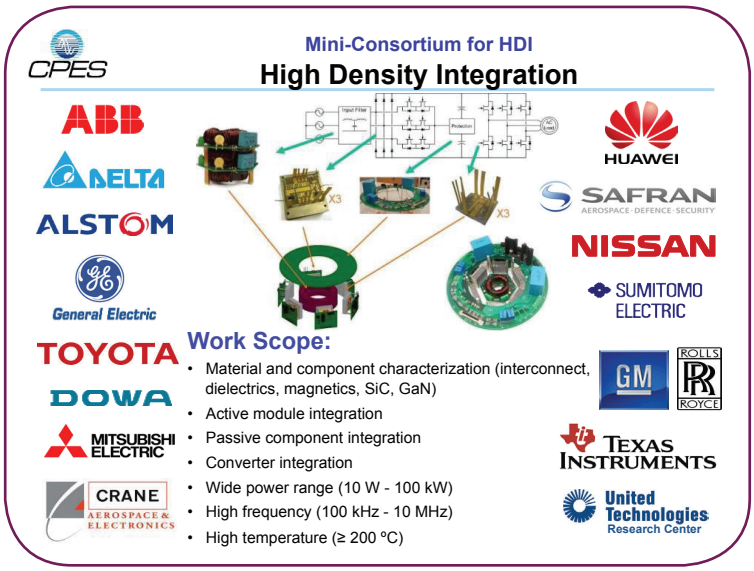
(a) High frequency adapter with 26W/in^3 power density and above 93% efficiency.

(b) High frequency 1-3kW off-Line distributed power systems with 200-300W/in^3 power density and above 96% efficiency.

(c) High frequency 6.6kW bidirectional on-board charger (OBC) for plug-in electric vehicles (PEVs) with 95% efficiency and 30-50% volume reduction.

Mini-Consortium on High Density Integration (HDI)

Over the past two decades, CPES has secured research funding for high-density system design from major firms, such as GE, Rolls-Royce, Boeing, Alstom, ABB, Toyota, Nissan, Raytheon, and MKS, as well as from government agencies including the NSF, DOE, DARPA, ONR, U.S. Army, and the U.S. Air Force. CPES has developed unique high-temperature packaging technology critical to the future power-electronics industry.



The HDI mini-consortium pursues its goal of high power density via two coupled paths—both leveraging the availability of wide-bandgap power semiconductors, and high-temperature passive components and ancillary functions. Both the switching frequency and maximum component temperatures will be pushed as high as component technologies, thermal management, and reliability permit.

The emergence of wide-bandgap semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) makes it possible to realize power switches that operate at frequencies beyond 5 MHz and temperatures beyond 200°C. As the switching frequency increases, switching noise shifts to a higher frequency and can be filtered with small passive components, leading to improved power density. Higher operating temperatures enable increased power density and applications in harsh environments, such as military systems, transportation systems, and outdoor industrial and utility systems.

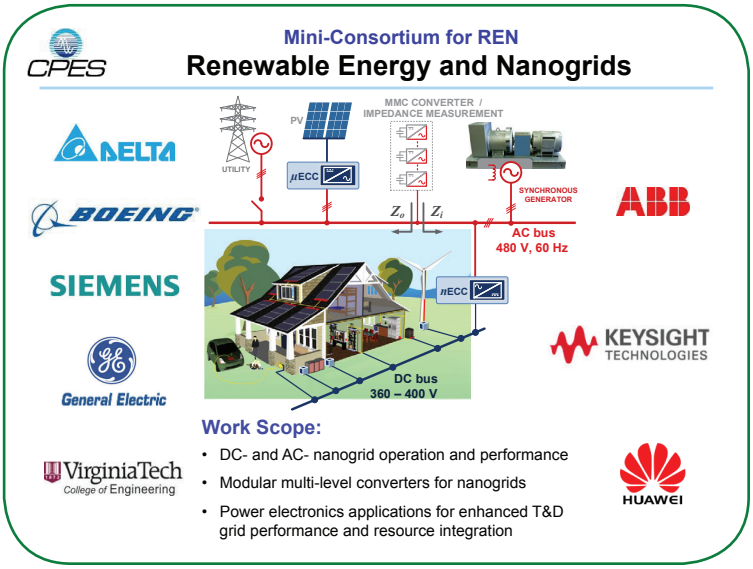
The HDI mini-consortium recognizes that the high-frequency, high-temperature switches must be accompanied by high-frequency or high-temperature components and packages in the remainder of the power-electronics system. Thus, HDI has developed die-attach materials that can be processed at low temperature, yet are reliable at the temperature of the wide-bandgap junction. Processes have been developed to encapsulate ultra-thin planar packages with polymer having high glass-transition temperature and dielectric strength. Techniques to decouple the noise loops have been identified to enable high-dV/dt commutation. Magnetic powder with low core loss density has been synthesized from magnetic metals for 1–5 MHz operation. Inductors have been integrated into the converter package as a substrate to achieve power density approaching 1 kW/in^3. Design methodologies for high-temperature capacitors, power buses, protection, sensing, digital control, etc. have also been documented.

The current scope of work being conducted within HDI includes the following topics:

- **Integration technologies -**
  - Die-attachment on copper surface by sintering of nano-scale silver paste.
  - Magnetic materials for high-frequency conversion- and EMI containment
- **Components**
  - Characterization and modeling of wide-bandgap semiconductor devices (SiC and GaN)
  - Low-profile magnetic substrate
  - Magnetic structures with high energy density
- **Module-level integration**
  - High-temperature characterization of thermal impedance of bond layer for SiC dice
  - Electro-thermal modeling of paralleled SiC dice
  - Gate drive power supply and gate driver circuit integration for co-packaged or system on chip module design
- **System-level integration**
  - SiC based Power Electronics Building Blocks (PEBB) design and integration
  - Integration of inductive power transfer systems
  - High frequency motor drive system
  - EMI and emission containment for high frequency power converters
  - High-temperature converter packaging

Mini-Consortium on Renewable Energy and Nanogrids (REN)

This CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The REN mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and sharing the research results among mini-consortium members. The main objective of the REN mini-consortium is to expand CPES' expertise in autonomous electric power systems (already established for transportation and IT), into the area of renewable energy and storage systems integration in the electric grid through power electronic converters, while providing competitive research and education in that area.



The current research directions of the REN mini-consortium comprise three different topics listed below with corresponding sub-topics. Additionally a REN system testbed structure is planned to be designed and built in the near future for nexperimental validation purposes.

WORK SCOPE:

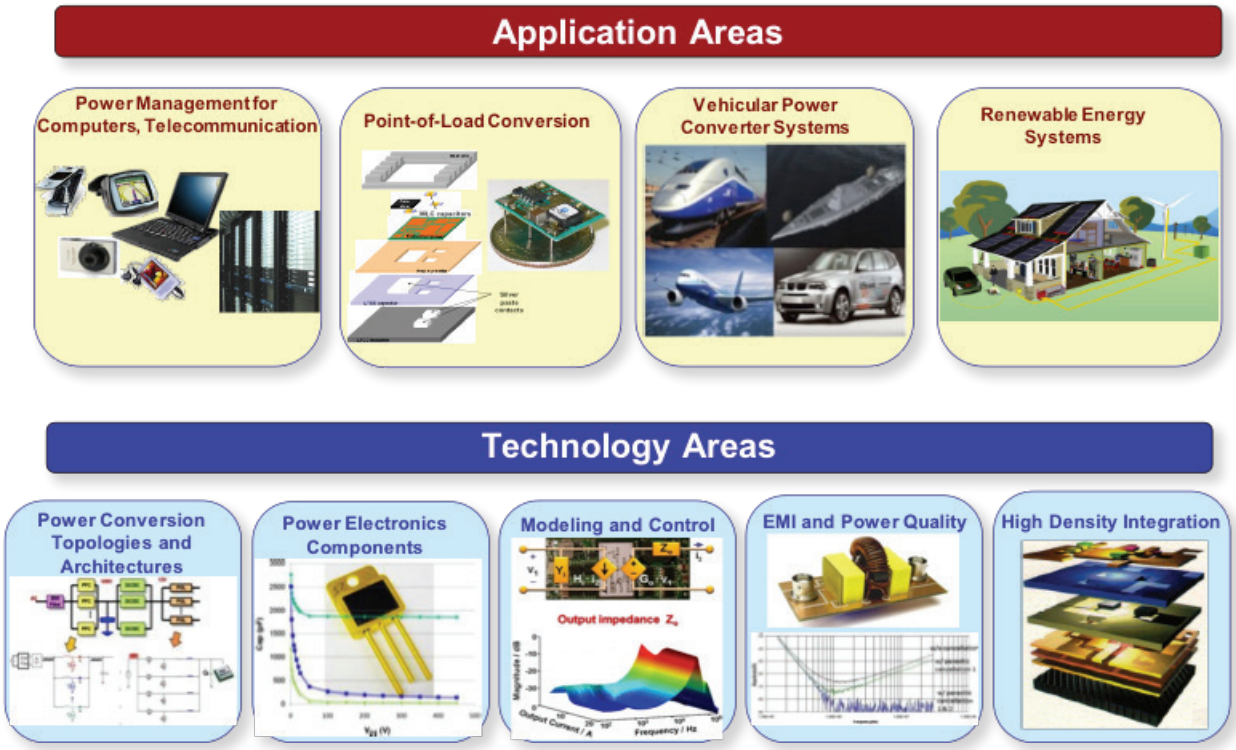
- **dc- Nanogrid Operation and Performance-**
  - Nanogrid architectures and design (380 V dc bus,48 V dc bus, and 480 V ac bus)
  - Bidirectional ac-dc nanogrid-interface converter –Energy Control Center
  - Battery-, PV- and wind- interface converters
  - Power management strategies and optimization of energy utilization (wind, PV and storage in nanogrids)
  - System stability, operation and performance
  - Hierarchical system modeling, analysis, and design
  - Dc outlets, ac and dc fault current limiting, system protection, prevention of arcing, etc.
- **Modular Multi-level Converters for Nanogrids**
  - SiC-based Power Electronic Building Blocks (PEBB)
  - SiC-based High Frequency DC/DC Transformer
  - -3-level bidirectional ac-dc nanogrid-interface converter
  - -Harmonic/EMI filter design for interconnection of multi-level converters to nanogrids
  - -Modeling, design and control of modular multi-level converters
  - -Modular multi-level converter for impedance measurements in ac- and dc- nanogrids
- **Power Electronics Applications for Enhanced Grid Performance and Resource Integration**
  - Hierarchical network of dynamically-decoupled electronically-interconnected sub-networks (picogrid, nanogrid, microgrid, …intergrid)
  - Power sharing, dynamic interactions, and stability in grid-connected and islanded systems with power electronics converters
  - Use of power electronics converters at distribution and transmission levels for P-f and Q-V operation.

RESEARCH

In its efforts to develop power processing systems to take electricity to the next step, CPES has developed research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; (5) high density integration.

These technology areas target applications that include: (1) Power management for information and communications technology; (2) Point-of-load conversion for power supplies; (3) Vehicular power conversion systems; (4) Renewable energy systems.

In 2015, CPES sponsored research totaled approximately $2.2 million. The following abstracts provide a quick insight to the current research efforts.



Sponsored Research

Power Supplies on a Chip (PSOC)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology)
Research collaborators: International Rectifier, University of Delaware, Enpirion
(September 1, 2010- June 30, 2014)

The first phase of the project aims to develop a proof of- concept prototype power supply on chip (PSOC) using- GaN devices operating at 5-l0MHz. The target was to achieve a power density greater than 1000W/in^3 with 88% efficiency. The proposed three-dimensional PSOC would be constructed using IR's GaN devices and Si-gate driver IC's assembled on top of a 1mm magnetic substrate using a high frequency soft magnetic material. Such a level of integration has never been attempted with a current greater than 5A. The proposed prototypes will extend the current to 20- 40A at 12V input voltage, targeting such applications as computer, mobile electronics, and telecommunication. After successful completion of phase 1, a 5MHz, 12V to 1.2V, 20A, two-phase integrated POL converter with GaN transistors and coupled-inductor substrate is demonstrated with power density as high as 1000 W/in^3,which is a 10x improvement compared to industry products at the same current level.

In phase II, CPES collaborated with Enpirion/Altera and focused on commercializing this 3D integrated POL module. We successfully transferred CPES's technologies, such as inductor substrate and 3D packaging design into Enpirion's products. We demonstrated a silicon based single-phase 12V/3.3V 17A 3D integrated module with 93% peak efficiency and 900W/in^3 power density. We also developed a two-phase 5V/3.3V 18A 3D integrated module with 94% peak efficiency and 1000W/in^3 power density.

Multi-Phase Auto-Tuning Self Compensating Power Supply Control Systems

Sponsored by: Energy Research Corporation
(September 1, 2012 – August 31, 2015)

The multi-phase voltage regulator (VR) has been widely used to power microprocessors. For multi-phase VR, a constant output impedance design is usually used to reduce the output capacitor bank. Conventionally, a fixed analog compensation network is chosen to compensate the worst-case component (such as inductor and output capacitor) variations on the plant, which will limit the converter bandwidth. Furthermore, since a microprocessor runs into sleep mode very frequently, several green-mode functions have been used to improve the light load efficiency such as phase shedding, discontinuous mode operation, and frequency changes. However, the plant characteristic will also change with these techniques under sleep mode, and will influence the stability and transient response during mode transitions. Therefore, it is very challenging and attractive to investigate multi-phase self tuning power supply control systems which can compensate the component variation and mode transition without suffering from the worst-case design compromises. In this project, a self-tuning power supply control system is developed to self-identify the plant characteristic change from component variation and operating mode transitions, and then adaptively adjust the compensation parameters to maintain stability and system performance. Therefore, external compensation circuitry and the output capacitor bank can be reduced to reduce total cost. We have already proposed several control methods with auto-tuning function to improve transient performance of voltage regulator, including self-compensated DCR current sensing, adaptive PLL loop for variable frequency control, and high bandwidth DDR VR with adaptive zero positioning. The proposed control concepts have been validated with Intel CPU emulator (Gen4 VTT tool).

A Study of Multi-Channel Constant Current Driver for Multiple Solid-State Light Sources on DC Distribution System

Sponsored by: Panasonic Electric Works
(April 1, 2011 - March 31, 2014)

Recently, many applications such as display backlighting, indoor lighting, and street lighting, all prefer multi-channel LED drivers. In this project, a design methodology for MC3 LLC LED driver was developed. The frequency controlled analog dimming solution has been verified by both simulation and experimentation. The circuit behavior under open- and short-failure was also investigated. Moreover, in order to achieve lower dimming ratio and keep higher efficiency, the hybrid control approach combining with asymmetrical PWM control and frequency control was proposed. We are currently developing a two stage LED driver with multi-channel constant current

resonant converter, which can drive multiple LED strings with uneven LED number.

High Efficiency High Density GaN Based 6.6kW Bi-Directional On-board Charger for Plug-in Electric Vehicles (PEVs)

Sponsored by: Department of Energy
Sub- Awardee of: Delta Products Corporation
(October 1, 2014 –September 30, 2017)

This project involves the development and commercialization of a lightweight, compact and efficient bidirectional on-board charger (OBC) for plug-in electric vehicles (PEVs). PEV hereafter refers to plug-in hybrid electric vehicles (PHEV) and battery electric vehicles (BEV).

The OBC uses novel circuit architectures and control schemes enabled by Gallium Nitride (GaN) based wide-bandgap (WBG) semiconductors to obtain charger efficiency better than 95% and reduce volume and mass by approximately 30% to 50% of the existing state-of-the-art silicon (Si) based chargers by pushing converter switching frequency to the MHz range. A Si-based bidirectional OBC is typically implemented with two separate modules: a charger and an inverter. A GaN-based bidirectional OBC can integrate both functions in a single module. It will result in substantial reductions in size, weight and cost.

With Chrysler's commitment, this project aimes to demonstrate the viability and commercial potential for WBG semiconductors in PEV applications. The core charger/inverter technology will also provide the added consumer benefits of providing emergency or convenience ac power on a vehicle, a feature that is strongly desired by consumers. In addition, it supports effective vehicle-to-grid (V2G) integration. V2G enables more efficient energy management practices, such as wind and solar photovoltaic distributed generation, peak shaving, and discounted off-hour charging rates for customers. All of which will help support the mainstream commercialization of PEVs.

This project brings together four world-class organizations including: the Center for Power Electronics Systems (CPES); Transphorm, Inc.; Delta Products Corporation; and Chrysler LLC.

In this project, CPES will focus on developing advanced circuit architectures and control schemes for GaN based battery charger. The main tasks included high-frequency GaN device and driver evaluation; topology selection and evaluation; high-frequency magnetic components development; reference design of high frequency PFC stage, dc/dc stage and EMC filters.

Gallium Nitride Switch Technology for Bi-Directional Battery to Grid Charger Application

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency - Energy, Agile Delivery of Electrical Power Technology)
Sub – Awardee of: HRL
October 1, 2010 – June 30, 2014)

The purpose of the project was to develop efficient, high power, and cost-effective power converters with application to the automotive sector. More specifically, it utilizes 600V Gallium Nitride (GaN) on low cost silicon substrate switches operating at 1 MHz. GaN semiconductors process electricity faster than the silicon semiconductors used in most conventional EV battery chargers. These high-speed semiconductors can be paired with lighter-weight electrical circuit components, which helps decrease the overall weight of the EV battery charger. The innovative design will result in a battery-to-grid bi-directional charger that enables efficient, cost effective power management focusing on grid-interactive distributed energy systems for the automotive sector.

High Density Motor Controller

Sponsored by: The Boeing Company
(August 1, 2005 – August 31, 2014)

In this project, a 10 kW high power density three-phase ac-dc-ac converter together with a high density PCB axial flux motor was developed and electrically evaluated. The converter consists of a Vienna-type rectifier front end and a two-level voltage source inverter (VSI). In order to reduce the switching loss and achieve a high operating junction temperature, SiC JFETs and SiC Schottky diodes are utilized. The design considerations for the phase-leg units, the gate driver, the input filter, the system protection and motor operation are investigated in detail. Experiments are carried out under different conditions, and the results verify the feasibility of the full system.

A second phase of the project devoted its effort to the weight minimization of the inverter and EMI filters required by 100 kW motor controllers. To this end parallel converter configurations have been explored using symmetric and asymmetric interleaving PWM techniques, which have achieved harmonic cancellation at both the ac and dc terminals of power converters with a great impact on the EMI filter weight minimization. Additionally, multi-level power converter topologies were investigated seeking further reduction of EMI emissions, higher power conversion efficiency, and superior power density.

Optimization of ac/ac Motor Controller Power Quality and EMI Filter Topology

Sponsored by: United Technologies Aerospace Systems
(January 1, 2012- December 31, 2015)

The objective of this work is the optimization of the combined power quality and EMI filters for motor con- troller comprising input power circuits fed by variable frequency power bus, and output power circuits that drive variable speed electric motors. The effect of the thermal and electrical characteristics associated with new materi- als with particular application on the EMI and PQ filters was thoroughly investigated demonstrating the advan- tages offered. From an EMI-filter weight minimization standpoint, interleaved two-level topologies, three-level topologies and 18-switch matrix converters were evalu- ated and compared face-to-face against the state-of-the- art two-level topology.

The second phase of this work has honed its efforts on the optimization of small local converters, each built on PCB cards addressing the combined power quality, EMI and thermal requirements and fed by variable frequency acor higher voltage dc power bus and output power circuits that provide regulated 28 V dc power. The effect of the thermal and electrical characteristics associated with a number of power topologies and the trade off in their performance in terms of weight, size and perceived reliability was investigated. Addressing single-phase power conversion first, a novel three-level semi-bridgeless PFC topology was developed to achieve 99% efficiency. For three-phase power conversion, a dual channel Vienna-type three-level converter was developed and tested surpassing 99% efficiency too.

The third phase of this project, also targeting PCB-based power converters, addressed the efficient power conversion from 270 V DC to 28 V DC, for which a multi-kilowatt resonant converter with isolation was designed and developed achieving 98% efficiency. The focus in this case was on the transformer design, high current operation (> 100A), and EMI filter design to meet input and output requirements.

The fourth phase of this project, to be completed in 2015, will consolidate the work of the past two years merging the ac-dc and dc-dc power conversion stages to design a three-phase 115V ac to 28V dc isolated power converter of maximum power density and maximum efficiency for a given form factor, which has required the reformulation of the design optimization procedure used to explore the potential of PCB-based power conversion systems.

Terminal Modeling of Noise Source in Switching Power Converters

Sponsored by: Hispano Suiza, SAFRAN
(October 1, 2010 -September 30, 2016)

The main objective of this research over the past years has been on the development of terminal models of noise sources in switching converters for simplified EMI analysis, models which must be scalable for different load and source conditions. Conventional methods of EMI modeling on the other hand use physics based models of semiconductor devices and EMI coupling paths. Due to the complex nature of these models the simulations often fail to converge or lead to unusable results.

In its last two phases, this project has explored the use of terminal models for the development of EMI filter design procedure. Its main focus was the design of filters for parallel inverters using interleaved PWM techniques. Research efforts aimed at simplifying the simulations by using Thevenin or Norton models of these noise cells. Here "noise-cell" may refer to both device level (single device or a Phase-leg) and converter level abstraction. This method has been successfully demonstrated so far on an industrial low-voltage 10kW motor drive, for which the unterminated EMI model of its 3-phase voltage source inverter (VSI) was built showing how it could predict the EMI behavior of the motor drive under varying conditions. In 2014, the method developed was extended to enable the modeling and prediction of EMI noise generated by converters operating at higher switching frequency (50–100 kHz) enabled by the use of SiC devices. This required the complete reformulation of the measuring techniques and modeling methodology employed, rendering the approach capable of predicting common-mode (CM) up to 30 MHz; a feat which had not been achieved before.

In its new phase, planned from 2015–2016, this project will make use of the EMI modeling and filter design procedures developed in the past year to support the design of integrated power supplies for gate-drive and avionics applications operating in harsh environment in terms of dv/dt transients and also high temperature. Specifically, the gate-drive power supply will be used to power an active gate-driver circuit with dv/dt and di/dt control to be developed for 600V GaN semiconductors, while the avionic power supply will additionally have to withstand high input voltage variability (10–100%). The project will also conduct a system study to determine the tradeoffs between switching frequency, dv/dt rate, inverter efficiency, EMI filter, and harness and motor size.

Impedance Measurement Unit (IMU) for 4160V AC Networks

Sponsored by: Office of Naval Research

(November 1, 2012 – June 30, 2014)

In this project, CPES designed, constructed, integrated and tested a medium voltage (MV) impedance measurement unit (IMU) to assess the stability of electric power systems and components for future Navy electric ships. The IMU is rated both for 4,160 V AC and 8,000 V dc networks, and is capable of injecting 5% system current and 5% system voltage, performing all the data acquisition and necessary post processing to determine the system impedances and be able to monitor and predict stability in the distribution system.

A key feature of the IMU is its modular structure, which allows it to operate in shunt and series injection mode, where its modules are connected in series and in parallel respectively. Additionally, the IMU has served as test platform to demonstrate the exceedingly high power processing capabilities of SiC power semiconductor devices, since by using 10kV, 120A, SiC DMOSFET/JBS diode power modules the IMU not only minimized the number of modules necessary to operate in MV networks, but also thanks to its ultra-high switching frequency (60 kHz), it made possible the characterization for the first time of impedances from dc up to 1 kHz in MV distribution systems; a definitive world record.

Strategies for Wide-Bandgap, Inexpensive Transistors for Controlling High Efficiency Systems (Switches)

Sponsored by: ARPA-E, ADEPT Program (Advanced Research Projects Agency Energy, Agile Delivery of Electrical Power Technology) Sub – Awardee of: HRL

(March 6, 2014-March 7, 2017)

With the sponsorship of ARPA-E, CPES has partnered with HRL Laboratories to demonstrate ultra-high efficiency low-cost power modules for future 1.2kV, 100A, vertical Gallium-Nitride (GaN) devices under development at HRL. These devices, expectedly capable of commutation speeds in the 100–200 V/ns range, will minimize switching losses to the extent were system efficiencies of >99 % are expected at the power converter level. To this end, CPES will build a 30kW, 800V dc, three-phase boost rectifier demonstrator. In its first year, the CPES has developed several ultra-low parasitic inductance package concepts using ribbon topside interconnections for the GaN devices and Flex PCB for the gate-terminals, with which it has reduced this parasitic component to less than 5 nH. Similarly, the module design has targeted the minimization of the parasitic capacitances to ground as an EMI containment strategy. A first prototype of the power module using 1.2kV, 90A, SiC MOSFET devices has recently been built to validate the module design.

Thermal-Electrical-Mechanical Modeling of IGBT Module Failure Modes

Sponsored by: Huazhong University of Science and Technology

(August 8, 2014 – July 31, 2017)

Insulated Gate Bipolar Transistors (IGBT) are one of the major players in modern power conversion, especially for medium and high power applications. The reliability of these devices remains to be a major concern, topic which Huazhong University of Science and Technology (HUST) has been studying jointly with Techsem Semiconductor Co., and now is interested in pursuing jointly with CPES. The primary goal of this research will be to investigate the possible failure modes of commercial IGBTs, including: 1) module layout and its influence on the electric field and thermal distribution; 2) wire bond structure and its impacts on the internal current distribution; 3) Direct Bond Copper (DBC) substrate preparation and its reliability; 4) thermal interface material (TIM) selection and its influence on the module reliability; 5) encapsulation of high voltage IGBT modules.

Optimal Magnetic Component Design for Boost Converters

Sponsored by: General Motors

(September 5, 2014 – March 31, 2015)

The push towards higher power, while simultaneously targeting higher power density in drive systems for traction applications, has resulted in the need to rise the dc-bus voltage of the converter system, to increase efficiency as well as to provide the needed design flexibility for the traction inverter and electrical motor. This is enabled by the use of a boost dc-dc converter to interface the battery pack and the inverter, which regulates the dc bus voltage under varying battery voltage and state of charge (SOC). The boost ratio required ranges from 2:1 to 4:1, for power levels ranging from 60–100 kW. The electrothermal stress on the boost inductor of this converter is hence significant, which has become a key barrier in the accomplishment of the system power density goals. CPES has accordingly initiated a focused effort to explore alternative dc-dc boost converter and boost inductor topologies, ultimately pursuing the formulation of new design criteria that can minimize the inductor weight. To this end, the research conducted has focused on the development of new elec-

trothermal models for the inductors, pursuing the use of closed-form analytical equations instead of the time-consuming finite-element method conventionally used.

Reliability-Oriented Design of Modular MV and HV Power Converters

Sponsored by: ABB Corporate Research

(May 1, 2013 – July 31, 2014)

The critical nature of grid applications in power engineering demands the utmost levels of reliability of its apparatus, as well as high availability and low maintenance requirements. The latter implies a high lifetime of all components used. Power electronics, now a mature technology, currently employed in critical applications such as commercial aviation, is being increasingly introduced in grid applications to improve the controllability and efficiency of power flow within power grids. The design of power converters at medium voltage (MV) and high voltage (HV) levels, nonetheless, still represents an immense challenge for power engineers in terms of reliability.

To this end, this project developed a Reliability-Oriented Design (ROD) procedure for modular MV and HV multilevel power converters addressing reliability upfront in the design process. This was done in three steps; first, the identification of critical system components; second, the assessment of reliability factors such as risk analysis, failure mode analysis, and fish bone diagrams; and third, the actual design, which was carried out by minimizing system complexity and stress, and by the use of the most reliable components, materials, structures, and converter configurations. Reliability models based on the latest release of RIAC-HDBK-217Plus were developed using existent knowledge and field data. These were used to conduct reliability evaluations based on Markov-Chain Models, which enabled the required state-wise reliability prediction required in modular power converters due to their inherent operation.

The methodology developed was applied, in what is a two-tier approach, first to the power modules of the converter, and then to the phase-arm structure as a representative of the whole power converter. At the power module, both the capacitor bank and IGBT phase-legs (half-bridge configuration) were analyzed in depth, investigating several alternative configurations, taking non-redundant and redundant solutions into consideration. Then, the best designs were used to assess the reliability of the power converter, for which the reliability of the phase-arm structure was investigated. Stress minimization and control were also investigated, for which the reliability model of the power module was used to ultimately select of the most propitious PWM scheme, circulating current controller, and switching frequency of the power modules. These results, expectedly, can readily serve as guide for the design of modular multilevel converters in both medium and high voltage applications seeking the highest reliability levels for its power converters.

SiC-PEBB Modules for Next Generation MVDC Integrated Power Systems— Development of the SiC-Based PEBB 1000

Sponsored by: Office of Naval Research

(August 1, 2014 – July 31, 2016)

This project will develop 1kV Silicon-Carbide (SiC) based power electronics building block (PEBB) modules, named PEBB 1000. These SiC-PEBBs will truly enable, for the first time, the notion of a high power density PEBB-only integrated power system for future Navy ships, profiting doubly from the system and commercial advantages featured by the PEBB modular concept, and from the power processing ad-vantages offered by SiC semiconductors. As such, power density, efficiency, high control band-width, modularity, voltage and current scalability, reconfiguration flexibility, simplicity, and the potential for low-cost commercial off-the-shelf technology become a factual reality. For demonstration and evaluation purposes, multiple PEBB 1000 units will be developed by CPES to evaluate the performance of the PEBB in ac-dc, dc-ac and dc-dc applications. This will allow for a comprehensive assessment of the PEBBs, converters, and their system-level impact. The project is also evaluating alternative SiC devices, and will target the use of 1.7 kV, 300 A, SiC MOSFET power modules from CREE, as well as 1.5 kV 200 A, SiC MOSFET power modules from GE.

In a parallel effort funded by ONR, GE Global Research will develop the PEBB 6000 unit using 10kV SiC MOSFET power modules from Powerex, using CREE devices, which will enable the comprehensive evaluation of the SiC-PEBB integrated power systems for future Navy ships.

SiC Module EMI Control by Transient Shaping and Shielding Technique

Sponsored by: Toyota Motor Engineering Manufacturing NA, Inc.

(August 15, 2014 – March 31, 2015)

The transition edges of PWM gate current and gate-source voltage will be synthesized from such basis functions as linear, exponential, and sinusoidal. The resultant gate-drive waveforms will excite silicon and silicon-carbide modules in a bidirectional boost converter over specified voltage and power ranges. Selected transition shapes will be synthesized using commercial parts for experimental verification. The project will document the tradeoffs among transition shapes, switch materials, interconnects, loss, and noise, along with recommendations for preferred practices.

Control of Modules of Parallel SiC Switching Cells

Sponsored by: Toyota Motor Engineering Manufacturing NA, Inc.

(August 15, 2014 – March 31, 2016)

The objective of the project is to develop a gate driver/controller that would commutate a large number of paralleled SiC MOSFETs reliably, as well as balance the performance of the dies with respect to power or thermal distributions. Development of guiding principles for the design and fabrication of a power module of such paralleled MOSFETs will also be achieved.

Constant-Flux Magnetics for Power Conversion

Sponsored by: National Science Foundation

(November 15, 2012 – October 31, 2015)

At least 30% of the volume in commercial inductors store no or negligible energy. The "constant-flux" concept improves energy density by filling the available volume with as much magnetic (core) materials as practically feasible, then dispersing the windings to shape the distribution of magnetic flux, e.g., to distribute magnetic flux uniformly.

In this project, guiding principles will be developed from the structural and field standpoints to realize the constant-flux concept. Performance metrics, such as inductances, capacitances, and quality factor will be modeled, quantified, and compared with the corresponding benchmarks.

Linear Actuator with Permanent Magnets

Sponsored by: GE Appliances and Light (GEAL)

(October 1, 2012 – March 31, 2014)

In this project, CPES worked to improve the design procedure and performance of GEAL's Linear Actuator with Permanent Magnets (LAPM) by determining the proper materials to use, validating flux models, predicting force vs. position, and making an improved LAPM design to meet a cost function.

MHz Power Amplifier – Proof of Feasibility

Sponsored by: Halliburton Energy Sources, Inc.

(October 23, 2013 – October 24, 2014)

This project supported the development of a power amplifier for an inductive load. The amplifier is to employ simple, efficient, and reliable circuit topology. A boost output and a buck front end have been selected to achieve soft switching and envelope control. The amplifier is controlled to shape the amplitude and phase of the current in load to follow prescribed window functions. Silicon carbide switches are used to enable operation at high frequency and high temperature.

PowERazor: an Innovative Electronic Packaging Technique for Manufacturing High-Reliability Power Electronic Modules

Sponsored by: NBE/NSF SBIR Phase I

(October 1, 2013 – December 31, 2014)

This project was to demonstrate the feasibility of an innovative packaging technology or PowERazor for manufacturing a high-reliability, low-profile, double-side cooled power electronics module. A robust workflow was developed for successful and repeatable fabrication of power module packages. Basic electrical parameters were characterized for feedback throughout the manufacturing process. Electrical test beds were constructed to ascertain power module package quality using device self-heating. Thermal testbeds were established to aid in quantifying the thermal management benefits of additional top side (double side) cooling. Reliability testing schemes were established and test beds were constructed for testing. Long term active and passive cycling schemes have been initiated.

MHz GaN Converter with Isolation

Sponsored by: Texas Instruments

This project starts with the design of the converter for zero-voltage switching over the full range of input voltage and output power to establish component requirements. Magnetic design of leakage inductance and harmonic losses in the coupled inductors with different winding structures are analyzed by finite-element simulation. The design of gate drive, loss analysis, effect of layout impedance, and other issues are addressed, leading to hardware verification with efficiency exceeding 85% at 5MHz and 30W output.

High-Density Integrated Inductor

Sponsored by: Texas Instruments

The "constant-flux" concept proposed recently is leveraged to distribute magnetic flux to improve energy density, lowering the profile of an inductor. The optimal flux distribution is identified mathematically, and verified by simulation. It is then applied to reduce the dc resistance of a commercial inductor by a factor of two, keeping the outer dimensions and inductance the same. Thermal-limited current rating is improved by 50%, whereas saturation-limited current rating is improved by 20% thanks to the suppression of flux crowding.

Design of Gapped Inductor under DC Bias

Sponsored by: Texas Instruments

Ferrite inductor with air gap is widely used because of low core loss and high inductance under dc bias. Conventional inductance formula for a gapped ferrite core assumes uniform or negligibly high permeability. When the core is designed to operate near saturation (to maximize core utilization) at rated current, such assumption is invalid owing to the appearance of regions with low, non-uniform permeabilities. Finite-element simulation uncovers a peak in the plot of inductance versus gap length that shifts with bias current, and that is not predicted by the conventional inductance formula. A reluctance model is formulated to explain the nonlinear behavior, and is verified experimentally.

New Projects approved and starting in the coming months:

High Power Solid State Circuits

Sponsored by: Office of Naval Research

Sub – Awardee of: ABB

Next Generation Power Electronics Manufacturing Innovation Institute (NGPEMII)

Sponsored by: Department of Energy

Sub – Awardee of: North Carolina State University

INTELLECTUAL PROPERTY

U.S. Patents Awarded

11-074

Three-Level Active Neutral Point Clamped Zero Voltage Switching Converter

Jin Li, Dushan Boroyevich, Jinjun Liu
U.S. PATENT: 8,929,114
Issued: 01/06/15

13-025

Anti-Islanding Protection in Three-Phase Converters Using Grid Synchronization Small-Signal Stability

Dong Dong, Dushan Boroyevich, Paolo Mattavelli, Bo Wen
U.S. PATENT: 8,957,666
Issued: 02/17/15

11-130

Multilayer Packaged Semiconductor Device and Method of Packaging

Ruxi Wang, Zheng Chen, Dushan Boroyevich
U.S. PATENT: 8,829,692
Issued: 09/09/14

11-049

High Frequency Loss Measurement Methods for Inductors and Transformers

Mingkai Mu, Fred C. Lee
U.S. PATENT: 8,823,370
Issued: 09/02/14

11-002

Pulse-Width-Modulated Resonant Power Conversion

Khai D.T. Ngo, Xiao Cao, Tatsuhiro Suzuki
U.S. PATENT: 8,811,039
Issued: 08/19/14

10.031/10.030

The use of PLL Stability for Islanding Detection

Timothy Thacker, Dushan Boroyevich, Fred Wang
U.S. PATENT: 8,823,416
Issued: 09/02/14

09.124

Adaptive On-Time Control for Power Factor Correction Stage Light Load Efficiency

Qian Li, Fred C. Lee, Ming Xu, Chuanyun Wang
U.S. PATENT: 8,803,489
Issued: 08/12/14

09.096

Multi-Phase EMI Noise Separator

Shuo Wang, Fred C. Lee
U.S. PATENT: 8,698,579
Issued: 04/15/14

INTELLECTUAL PROPERTY

Invention Disclosures

15-071
1/27/15
Multi-Step Simplified Optimal Trajectory Control Based on Only V_o and I_{load}
Chao Fei, Fred C. Lee, Weiyi Feng, Qiang Li

15-070
1/27/15
Adaptive SR Driving Scheme for Resonant Converter
Chao Fei, Fred C. Lee, Weiyi Feng, Qiang Li

15-069
2/2/15
Universal System Structure for Low Power Adapters
Fred C. Lee, Xiucheng Huang, Qiang Li

15-068
2/2/15
A Novel Driving Scheme for Synchronous Rectifier in CRM Flyback Converters
Xiucheng Huang, Fred C. Lee, Qiang Li

15-067
1/26/15
New Current Mode Control Based on Charge Control Concept
Syed Bari, Fred C. Lee, Qiang Li

15-064
1/21/15
Improved Current-Mode Control with Single-Step Load Transient
Virginia Li, Pei-Hsin Liu, Qiang Li, Fred C. Lee

15-063
1/20/15
Boost Power Amplifier Operated at the Synchronous Switching Frequency with Small Input Inductance and High Efficiency
Milisav Danilovic, Khai D. T. Ngo

15-062
1/20/15
Active Compensation of Buck-Boost Power Amplifier for Constant Frequency Operation under Wide-Load Variation
Milisav Danilovic, Khai D. T. Ngo

15-061
1/9/15
Boost Power Amplifier with Improved Bandwidth
Khai D. T. Ngo, Yincan Mao

15-053
12/1/14
Optimal Battery Current Waveform for Bidirectional PHEV Battery Charger
Lingxiao Xue, Paolo Mattavelli, Dushan Boroyevich

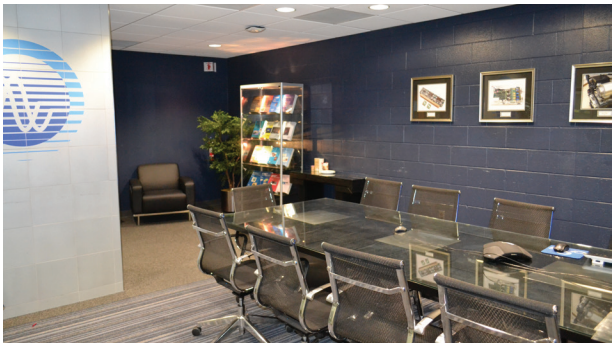
15-049
11/12/14
Coupled Inductor for Interleaved Multiphase Three-Level DC-DC Converters and Its Integrated Designs
Mingkai Mu, Sizhao Lu, Yang Jiao, Fred C. Lee

14-147
5/21/14
Switching-Cycle Control For The Modular Multilevel DC/DC Converter
Jun Wang, Rolando Burgos, Dushan Boroyevich

14-144
5/22/14
Low Profile Coupled Inductor Substrate with Transient Speed Improvement
Yipeng Su, Dongbin Hou, Fred C. Lee, Qiang Li

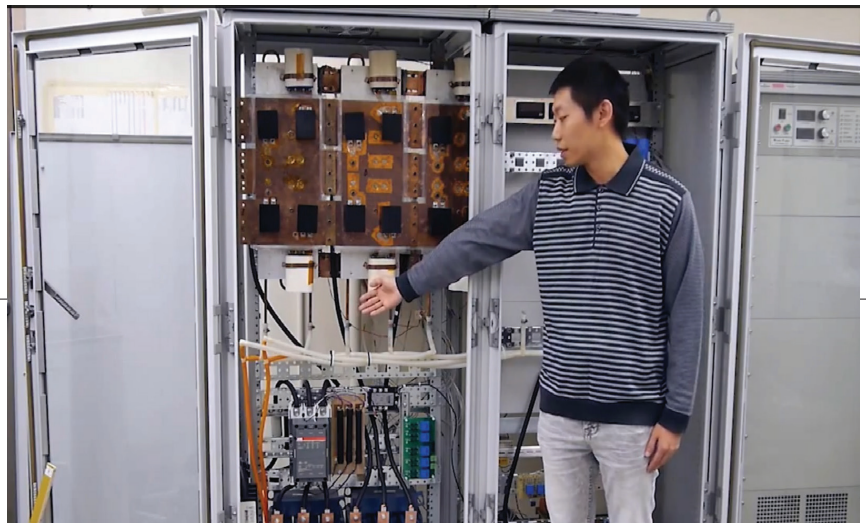
14-101
3/4/14
Transient Performance Improvement for Constant On Time Control
Syed Bari, Fred C. Lee, Qiang Li, Pei-Hsin Liu

VIRGINIA TECH FACILITIES



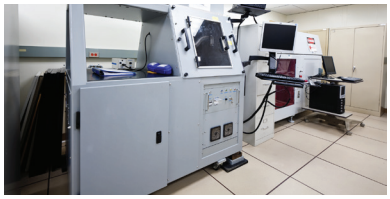
Introduction

The Center headquarters is located at Virginia Tech, occupying office and lab facilities encompassing more than 19,000 sq ft of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab, and computer lab. In addition to the headquarters labs and offices, a research library, and a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators is maintained. Interactive collaboration is routinely facilitated through conference calls, WebEx online conferencing, student and faculty exchanges, and face-to-face research project review meetings.



Electrical Research Laboratory

The electrical research laboratory is equipped with state of the art tools and equipment for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6kV, 1MW. It also includes PWB manufacturing equipment, an EMI chamber, a clean room and a mechanical shop. New this year is a state of the art curve tracer that is capable of characterizing up to 10kV and 1500A. Each student bench is equipped with Dell computers with an i7 core and up to 16 GB of RAM for running complex simulations. Standard instrumentation includes: GHz oscilloscopes, multi-channel function generators, electronic loads, network, spectrum, impedance, logic, and power analyzers, thermal sensors, and ac/dc bench supplies of all sizes. Specialized test room equipment includes: thermal imaging, thermal cycling chambers, Hi-Pot tester, 3D magnetic field scanner, EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, magnetic core loss testing, programmable and variable loads, and liquid cooled heat-exchanger.

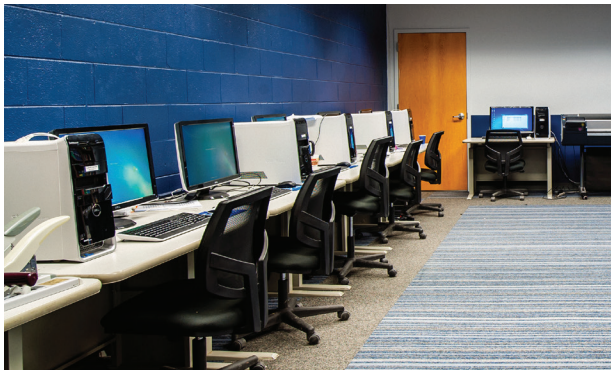


Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculties, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab is established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide the state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 clean room space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. The IP lab also has the ability to mount bare dies and SMT components using high precision pick-n-place machine, solder reflow belt furnace, and convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants an automated precision dispensing system and a spin coater have been added in the lab. In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The Component- and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Low and high power curve tracers, impedance analyzers, and precision multimeters can be used for electrical property measurements. Thermal performance evaluation can be made by the setup of thermocouples, optic-fiber sensors, IR imaging, and thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and the ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.

Library and Computer Lab

The computer lab supports all major software used in power electronics design including: SPICE, Saber, Simplis, Code Composer, Math products – Matlab and Mathcad, Ansys Products – Workbench and Mechanical, Ansys Electromagnetics – Maxwell, Electronics Desktop (Q3D, HFSS), Simplorer, SIWave, Mentor Graphics Flowtherm, PLECS, and Altium Designer.



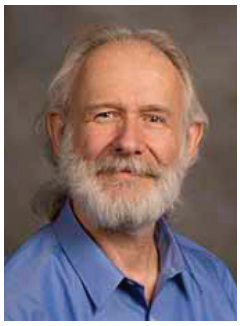
High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost sharing of more than $250,000 for renovations, the electrical research lab area at Virginia Tech has been renovated and upfit to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160V level. The unique installation distinguishes Virginia Tech as one of a few select universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

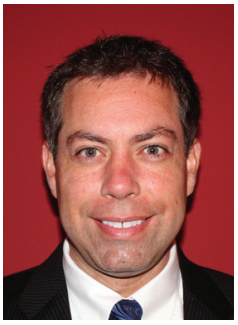
PEOPLE

FACULTY


Fred C. Lee


Dushan Boroyevich


Khai Ngo


Rolando Burgos


Qiang Li

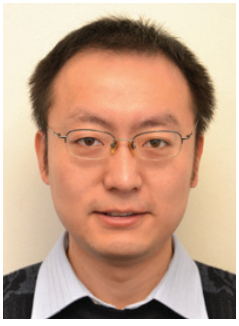
AFFILIATE FACULTY

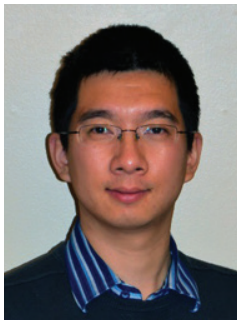

Guo-Quan Lu

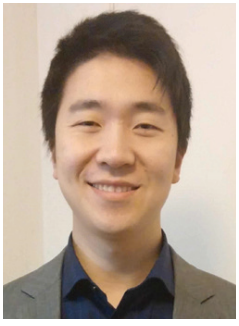
RESEARCH FACULTY


Wenli Zhang

RESEARCH SCIENTISTS


Mingkai Mu


Zhiyu Shen


Xuning Zhang

TECHNICAL STAFF

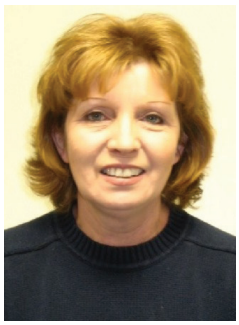

Igor Cvetkovic


David Gilham

SUPPORT STAFF


Marianne Hawthorne

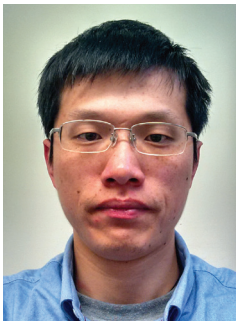

Linda Long


Trish Rose


Teresa Shaw

VISITING SCHOLARS


Adegbie, Daniel


Cai, Chaofeng

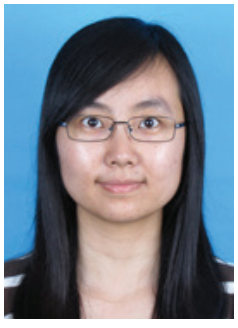

Cai, Hui


Chen, Alian


Chen, Xiaofei


Cucak, Dejana


Du, Guiping

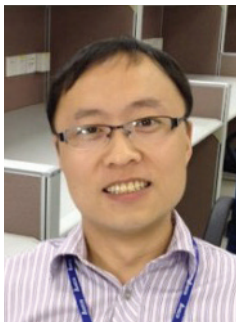

Du, Weijing


Emori, Kenta


Granig, Wolfgang

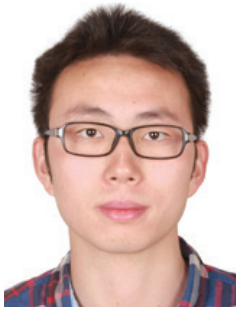
PEOPLE

VISITING SCHOLARS


Hu, Peiqing


Huang, Pin-Yu


Li, Daniel (Yan-Cun)


Li, Kai


Ming, Xin


Reusch, David


Rizzoli, Gabriele


She, Shuojie


Shin, Jong-Won


Sumsurooah, Sharmila


Tardy, Alain

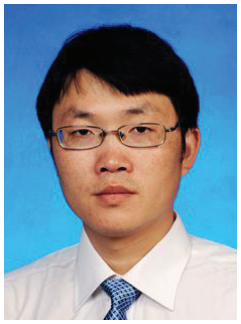

Vasquez Quintero, Juan Carlos


Wang, Li


Williams, Joseph Mark


Yang, Jingwei


Yang, Lijun

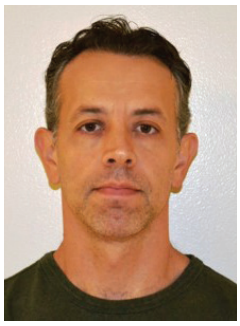

Yang, Rongfeng


Yuki, Seiya

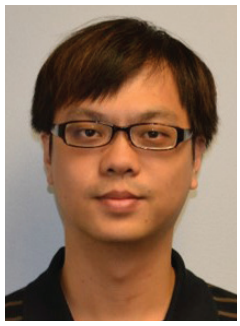
STUDENTS

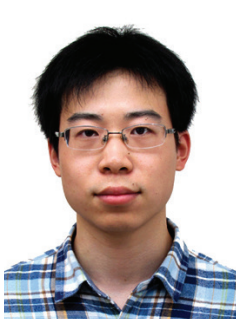

Ahmed, Mohamed


Bari, Syed


Berry, David


Cao, Zhongsheng


Chen, Chien-An


Chen, Fang

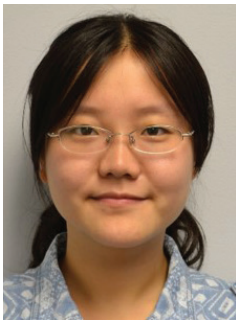

Chen, Xuebing

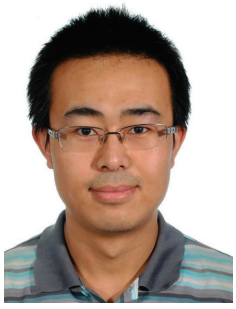

Cui, Han

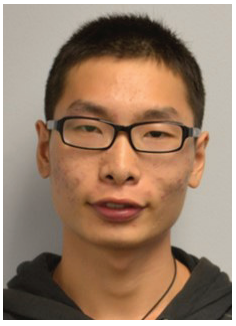

Cvetkovic, Igor


Danilovic, Milisav


DiMarino, Christina

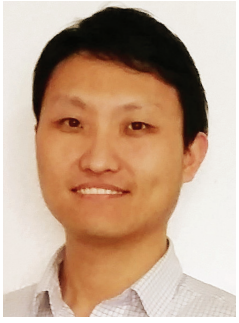

Fan, Ye

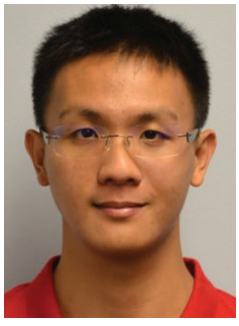

Fei, Chao


Feng, Junjie


Ge, Ting


Haryani, Nidhi


Hou, Dongbin


Hsieh, Yi-Hsun


Huang, Xiucheng


Huang, Zhengrong

PEOPLE

STUDENTS


Jaksic, Marko


Jiao, Yang


Kim, Woochan


Li, Bin

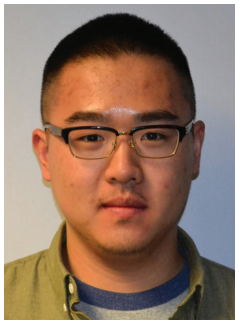

Li, Chen


Li, Chi

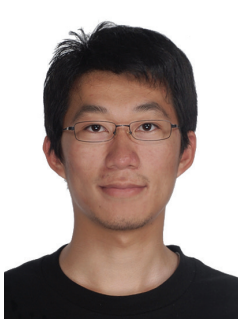

Li, Virginia

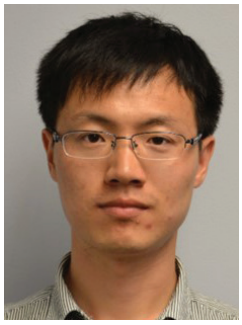

Liu, Pei-Hsin


Liu, Tao

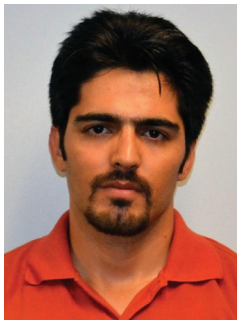

Liu, Xingye


Liu, Zhengyang


Lu, Ming


Lyu, Yadong


Mao, Yincan


Marzoughi, Alinaghi

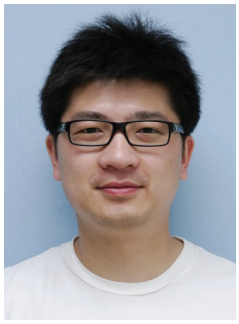

Miao, Zichen


Mukherjee, Subhajyoti

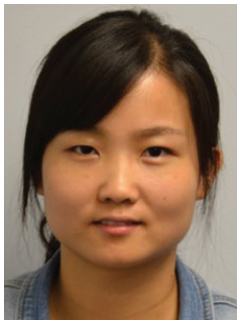

Najmi, Vahid

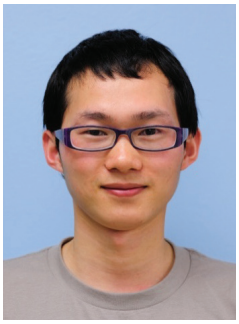

Qin, Ruiyang


Rashidi Mehrabadi, Niloofar

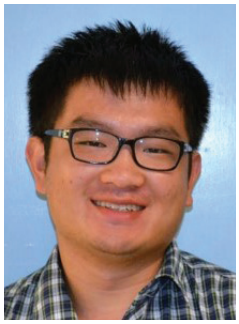

Su, Yipeng

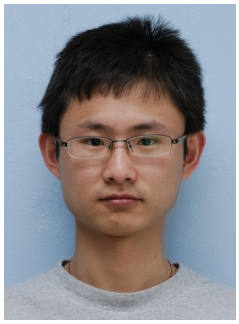

Sun, Bingyao

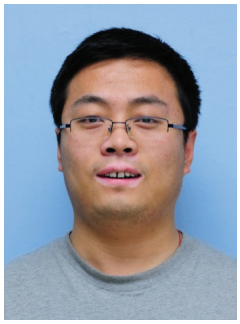

Tang, Ye


Tian, Shuilin


Wang, Jun


Wang, Qiong

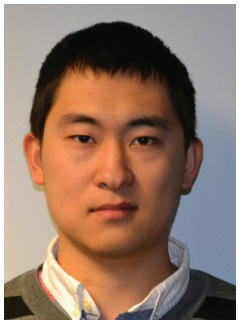

Wen, Bo


Xue, Lingxiao


Yan, Yasmine

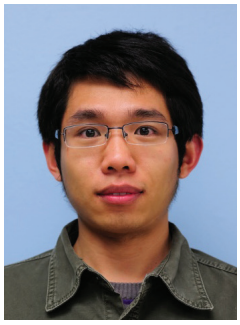

Yang, Yuchen


Yao, Yiying

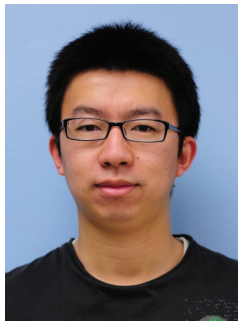

Yu, Jianghui


Zhang, Lujie


Zhang, Wei

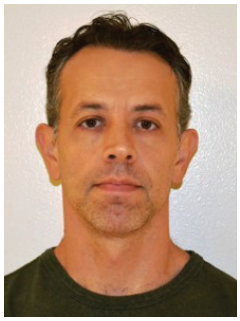

Zhang, Zhemin (Jimmy)


Zhao, Shishuo


Zheng, Hanguang (Jason)

PEOPLE

GRADUATES

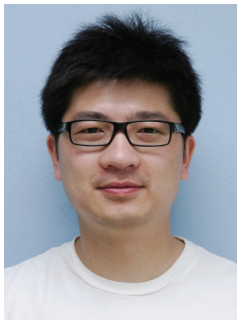

Berry, David

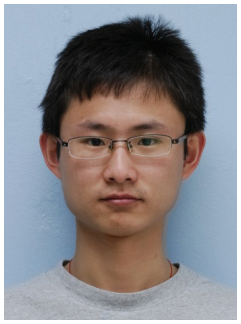

Cao, Zhongsheng


Chen, Xuebing


Jaksic, Marko


Kim, Woochan


Su,Yipeng


Wen, Bo


Yao, Yiying

SCIENTIFIC ADVISORY BOARD (SAB)

Ralph Cavin	Semiconductor Research Corporation
John Kassakian	Massachusetts Institute of Technology
Tom Lipo	University of Wisconsin-Madison (retired)
Bob Steigerwald	GE Global Research (retired)
Al Tucker	Office of Naval Research (retired)

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Chi-Ming (Jimmy) Wang	Toyota Motor Engineering & Manufacturing North America, Inc.
Luis Arnedo	United Technologies Research Center
Jianping Zhou	ZTE Corporation

HONORS & RECOGNITIONS

National and International Honors

Fred C. Lee

Recipient of 2015 IEEE Medal in Power Engineering
"For contributions to power electronics, especially high-frequency power conversion"

Honorary Chair Professor,
National Chiao Tong University, Taiwan

Khai Ngo

IEEE Fellow
"For contributions to unified synthesis and modeling of switched-mode converters"

Keynote Addresses

Fred C. Lee:

"Energy and Power Electronics,"
The Sustainable Development Forum on Power Electronics in China, Shenzhen, People's Republic of China, July 27-28, 2014

Fred C. Lee:

"Is GaN a Game Changing Device,"
Power Electronics and Motion Control Conference (PEMC), Antalya, Turkey, September 22-24, 2014

Fred C. Lee:

"Is GaN a Game Changing Device?"
2nd Workshop on Wide Bandgap Power Devices and Application (WiPDA), Knoxville, Tennessee, October 13-15, 2014

Dushan Boroyevich:

"Power Sharing and Stability in AC Systems with large Penetration of Renewables,"
International Conference on Renewable Energy Research and Education (ICRERA), Milwaukee, Wisconsin, October 19-22, 2014

Fred C. Lee:

"Energy and Power Electronics," Power Electronics Application Conference (PEAC)",
Shanghai, People's Republic of China, November 5-8, 2014

Invited Talks

Qiang Li:

"GaN Devices and Applications: The Current Landscape,"
presented in Technology Roundtable on "Standards for GaN Power Electronics", UC Santa Barbara, March 11-12, 2014.

Dushan Boroyevich:

"DC Nanogrids for Buildings with Net-Zero Electric Energy Costs?"
Power Electronics and Electrical Challenges for Engineering Energy-Efficient Building: A Focused Workshop, Fort Worth, Texas, March 15, 2014

Fred C. Lee:

"Power Electronics and Energy,"
Academia Sinica, Taipei, Taiwan, July 5, 2014

Qiang Li:

"High-Density Integrated Voltage Regulator Module,"
ECE Department of the University of Maryland, August 1, 2014.

Fred C. Lee:

"Trends to Switch-Mode Power Supplies"
Texas Instruments, Sunnyvale, California, October 4, 2014

Rolando Burgos:

"High Power Conversion Systems,"
Johnson Controls, York, Pennsylvania, November 14, 2014.

Fred C. Lee:

"Power Electronics and Energy",
Distinguished Lecture Series, University of Miami, College of Engineering, Miami, Florida, December 1, 2014

Fred C. Lee:

"Power Electronics and Energy,"
Booz Allen Hamilton Distinguished Colloquium Series, University of Maryland, College Park, Maryland, February 27, 2015

2014 CPES Annual Conference Best Student Presentation Awards

Sponsored by Delta Electronics, Huawei Technologies, and CPES

Dongbin Hou
Best Technical Presentation Award

Christina DiMarino
Best Dialogue Paper Presentation Award

Marko Jaksic
Best Dialogue Paper Presentation Award

Wei Zhang
Best Dialogue Paper Presentation Award

APEC 2014 Outstanding Presentation Awards

"Modeling and Autotuning of AVP Control with Inductor DCR Current Sensing,"
Pei-Hsin Liu, Fred C. Lee, Qiang Li

"Impedance-Based Analysis of Grid-Synchronization Stability for Three-Phase Paralleled Converters,"
Bo Wen, Dushan Boroyevich, Paolo Mattavelli, Rolando Burgos, Zhiyu Shen

ECCE 2014 Best Student Poster Presentation Award

"Compression of the Load Resistance Range in Constant Frequency Resonant Inverters,"
Milisav Danilovic, Khai D.T. Ngo, Zhemin Zhang

IMAPS 2014 Outstanding Student Paper Award

"Compressive-Post Packaging of Double-Sided Die,"
Woochan Kim, Jia-Woei Wu, Bill Alexander, Sauvik Chowdhury, Collin Hitchcock, Nga C. Lee, James J. Q. Lu, T. Paul Chow, and Khai D. T. Ngo

PUBLICATIONS

Transactions Papers

A Family of Switching Capacitor Regulators
Ling Gu, Ke Jin, Xinbo Ruan, Ming Xu, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 2, February 2014, pp. 740-749

Optimal Trajectory Control of LLC Resonant Converters for LED PWM Dimming
Weiyi Feng, Fred C. Lee, Paolo Mattavelli
IEEE Transactions on Power Electronics, Vol. 29, No. 2, February 2014, pp. 979-987

Analysis of Unified Output MPPT Control in Subpanel PV Converter System
Feng Wang, Xinke Wu, Fred C. Lee, Zijian Wang, Pengju Kong, Fang Zhuo
IEEE Transactions on Power Electronics, Vol. 29, No. 3, March 2014, pp. 1275-1284

Optimal Trajectory Control of LLC Resonant Converters for Soft Start-Up
Weiyi Feng, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 3, March 2014, pp. 1461-1468

Package Parasitic Inductance Extraction and Simulation Model Development for the High-Voltage Cascode GaN HEMT
Zhengyang Liu, Xiucheng Huang, Fred C. Lee, Qiang Li
IEEE Transactions on Power Electronics, Vol. 29, No. 4, April 2014, pp. 1977-1985

Forced-Air Cooling System Design Under Weight Constraint for High-Temperature SiC Converter
Puqing Ning, Fred Wang, Khai Ngo
IEEE Transactions on Power Electronics, Vol. 29, No. 4, April 2014, pp. 1998-2007

I^2 Average Current Mode Control for Switching Converters
Yingyi Yang, Fred C. Lee, Paolo Mattavelli, Pei-Hsin Liu
IEEE Transactions on Power Electronics, Vol. 29, No. 4, April 2014, pp. 2027-2036.

An FPGA-Based Gain-Scheduled Controller for Resonant Converters Applied to Induction Cooktops
O. Lucia, O. Jiménez, I. Urriza, L. A. Barragán, P. Mattavelli, and D. Boroyevich
IEEE Transactions on Power Electronics, Vol. 29, No. 4, April 2014, pp. 2143-2152

Evaluation of Thermal Cycling Reliability of Sintered Nanosilver Versus Soldered Joints by Curvature Measurement
Li Jiang, Thomas G. Lei, Khai D.T. Ngo, Guo-Quan Lu, S. Luo
IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 4, No. 5, May 2014, pp. 751-761

Analytical Loss Model of High Voltage GaN HEMT in Cascode Configuration
Xiucheng Huang, Qiang Li, Zhengyang Liu, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 5, May 2014, pp. 2208-2219 (Special Issue on Wide Bangap Devices and Their Applications)

A 1200-V, 60-A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications
Zheng Chen, Yiying Yao, Dushan Boroyevich, Khai Ngo, Paolo Mattavelli, Kaushik Rajashekara
IEEE Transactions on Power Electronics, Vol. 29, No. 5, May 2014, pp. 2307-2320 (Special Issue on Wide Bangap Devices and Their Applications)

Evaluation and Application of 600V GaN HEMT in Cascode Structure
Xiucheng Huang, Zhengyang Liu, Qiang Li, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 5, May 2014, pp. 2453-2461 (Special Issue on Wide Bangap Devices and Their Applications)

Compensation of DC-Link Oscillation in Single-Phase to Single-Phase VSC/CSC and Power Density Comparison
Montie Vitorino, Ruxi Wang, Marucio B. R. Correa, Dushan Boroyevich
IEEE Transactions on Industry Applications, Vol. 50 No. 3., May/June 2014, pp. 2021-2028

Digital Hybrid Ripple-Based Constant On-Time Control for Voltage Regulator Modules
Kuang-Yao (Brian) Cheng, Shuilin Tian, Feng Yu, Fred C. Lee, Paolo Mattavelli
IEEE Transactions on Power Electronics, Vol. 29, No. 6, June 2014, pp. 3132-3144

Switching Performance Optimization of a High Power High Frequency 3-level Active Neutral Point Clamped Phase Leg
Yang Jiao, Sizhao Lu, Fred. C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 7, July 2014, pp. 3255-3266

Design and Implementation of Integrated Common Mode Capacitors for SiC-JFET Inverters
Remi Robutel, Christian Martin, Cyril Buttay, Herve Morel, Paolo Mattavelli, Dushan Boroyevich, Regis Meuret
IEEE Transactions on Power Electronics, Vol. 29, No. 7, July 2014, pp. 3625-3636

LLC Resonant Converter with Matrix Transformer
Daocheng Huang, Shu Ji, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 29, No. 8, August 2014, pp. 4339-4347

New Core Loss Measurement Method for High-Frequency Magnetic Materials
Mingkai Mu, Qiang Li, David Joel Gilham, Fred C. Lee, Khai D. T. Ngo
IEEE Transactions on Power Electronics, Vol. 29, No. 8, August 2014, pp. 4374-4381

Small-signal Analysis and Optimal Design of External Ramp for Constant On-Time V^2 Control with Multilayer Ceramic Caps
Shuilin Tian, Fred C. Lee, Paolo Mattavelli, Kuang-Yao (Brian) Cheng, Yingyi Yan
IEEE Transactions on Power Electronics, Vol. 29, No. 8, August 2014, pp. 4450 - 4460

EMI Behavioral Models of DC-Fed Three-Phase Motor Drive Systems
Hemant Bishnoi, Paolo Mattavelli, Rolando Burgos, Dushan Boroyevich
IEEE Transactions on Power Electronics, Vol. 29, No. 9, September 2014, pp. 4633-4645

Improving High Frequency Performance of an Input Common Mode EMI Filter using an Impedance-Mismatching Filter
Fang Luo, Dong Dong, Dushan Boroyevich, Paolo Mattavelli, Shuo Wang
IEEE Transactions on Power Electronics, Vol. 29, No. 10, October 2014, pp. 5111-5115.

Inductor Geometry with Improved Energy Density
Han Cui, Khai D. T. Ngo, Jim Moss, Michele H. Lim, Ernesto Rey
IEEE Transactions on Power Electronics, Vol. 29, No. 10, October 2014, pp. 5446-5453.

A Unified Control for the Combined Permanent Magnet Generator and Active Rectifier System
Zhuxian Xu, Di Zhang, Fred Wang, Dushan Boroyevich
IEEE Transactions on Power Electronics, Vol. 29, No. 10, October 2014, pp. 5644-5656

Space Vector Modulation for 3-level NPC Converter with Neutral Point Voltage Balancing and Switching Loss Reduction
Yang Jiao, Fred. C. Lee, Sizhao Lu
EEE Transactions on Power Electronics, Vol. 29, No. 10, October 2014, pp. 5579-5591

Special Issue on Modeling and Control of Power Electronics for Renewable Energy and Power Systems
Rolando Burgos, Jian Sun
IEEE Journal of Emerging and Selected topics in Power Electronics, Vol. 2, No. 4, December 2014, pp. 713-714

PUBLICATIONS

Modeling and Design of Islanding Detection Using Phase-Locked Loops in Three-Phase Grid-Interface Power Converters
Dong Dong, Bo Wen, Paolo Mattavelli, Dushan Boroyevich, Yaosuo Xue
IEEE Journal of Emerging and Selected topics in Power Electronics, Vol. 2, No. 4, December 2014, pp. 1032-1040

Switching-Cycle State-Space Modeling and Control of the Modular Multilevel Converter
Jun Wang, Rolando Burgos, Dushan Boroyevich
IEEE Journal of Emerging and Selected topics in Power Electronics, Vol. 2, No. 4, December 2014, pp. 1159-1170

Direct-Bond-Copper Switch Module for Management of Temperature and Noise in 220-W/in^3 Power Assembly
Woochan Kim, Jongwon Shin, Khai D. T. Ngo
Journal of Microelectronics and Electronic Packaging, Vol. 11, No. 4, Fourth Quarter 2014, pp. 174-180

Analysis of Phase-Locked Loop Low-Frequency Stability in Three-Phase Grid-Connected Power Converters Considering Impedance Interactions
Dong Dong, Bo Wen, Dushan Boroyevich, Paolo Mattavelli, Yaosuo Xue
IEEE Transactions on Industrial Electronics, Vol. 62, No. 1, January 2015, pp. 310-321

Model for Electromagnetic Actuator with Significant Fringing Using Minimal Fitting Parameters
Ming Lu, Khai D. T. Ngo, Mariano Filippa, and William Bicknell (GE Appliances?)
EEE Transactions on Magnetics, Vol, 51, No. 1, Part 2, January 2015 (800207)

Survey of High-Temperature Polymeric Encapsulants for Power Electronic Packaging
Yiying Yao, Guo-Quan Lu, Dushan Boroyevich, Khai D. T. Ngo
IEEE Transactions on Components, Packaging, and Manufacturing Technology, Vol. 5, No. 2, February 2015, pp. 168-181

High Density Integration of High Frequency High Current Point-of-Load (POL) Modules with Planar Inductors
Wenli Zhang, Yipeng Su, Mingkai Mu, David Gilham, Qiang Li, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 30, No. 3, March 2015, pp. 1421-1431

Small-Signal Analysis and Optimal Design of Constant Frequency V^2 Control
Shuilin Tian, Fred C. Lee, Paolo Mattavelli, Yingyi Yan
IEEE Transactions on Power Electronics, Vol. 30, No. 3, March 2015, pp. 1724-1733

Conference Papers

Conducted EMI and Systems Integration (Invited)
Dushan Boroyevich, Xuning Zhang, Hemant Bishnoi, Rolando Burgos, Paolo Mattavelli, Fred Wang
2014 CIPS (8th International Conference on Integrated Power Electronics Systems, Nuremburg, Germany, February 25-27, 2014

Small Signal Analysis and Design of Active Droop Control Using Current Mode Equivalent Circuit Model
Yingyi Yan, Pei-Hsin Liu, Fred C. Lee
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Space Vector Modulation for 3-level NPC Converter with Neutral Voltage Balancing and Switching Loss/Noise Reduction
Yang Jiao, Fred C. Lee, Sizhao Lu
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

New Core Loss Measurement Method with Partial Cancellation Concept
Dongbin Hou, Mingkai Mu, Fred. C. Lee, Qiang Li
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Unified Equivalent Circuit Model for V^2 Control
Shuilin Tian, Fred Lee, Qiang Li, Yingyi Yan
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Modeling and Autotuning of AVP Control with Inductor DCR Current Sensing (Outstanding Presentation Award)
Pei-Hsin Liu, Fred C. Lee, Qiang Li
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Control Loop Design of a Two-Stage Bidirectional AC/DC Converter for Renewable Energy System
Fang Chen, Dong Dong, Rolando Burgos, Dushan Boroyevich
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Design Considerations for GaN HEMT Multichip Halfbridge Module for High-Frequency Power Converters (Outstanding Presentation Award)
Fang Luo, Brian Hughes, Henry Chen, Lingxiao Xue, Paolo Mattavelli, Dushan Boroyevich
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Analysis and Reduction of Common Mode EMI Noise for Resonant Converters
Yuchen Yang, Daocheng Huang, Fred Lee, Qiang Li
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Evaluation of High-Voltage Cascode GaN HEMT in Different Packages
Zhengyang Liu, Xiucheng Huang, Wenli Zhang, Fred C. Lee, Qiang Li
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Gate Drive Design Considerations for High Voltage Cascode GaN HEMT
Wei Zhang, Xiucheng Huang, Fred C. Lee, Qiang Li
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

LLC Resonant Converter with Matrix Transformer
Daocheng Huang, Shu Ji, Fred C. Lee
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

State-Trajectory Control of LLC Converter Implemented by MCU
Chao Fei, Weiyi Feng, Fred C. Lee, Qiang Li
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Bi-Directional PHEV Battery Charger Based on 300V Normally-Off GaN-on-Si Multi-Chip Module
Lingxiao Xue, Brian Hughes, Paolo Mattavelli, Mingkai Mu, Zhiyu Shen, Dushan Boroyevich, Rolando Burgos
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Efficiency Evaluation of Two-level and Three-level Bridgeless PFC Boost Rectifiers
Qiong Wang, Bo Wen, Rolando Burgos, Dushan Boroyevich, Adam White
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Modeling the Output-Impedance Negative Incremental Resistance Behavior of Grid-Tied Inverters
Bo wen, Dushan Boroyevich, Paolo Mattavelli, Rolando Burgos, Zhiyu Shen
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

PUBLICATIONS

Impedance-Based Analysis of Grid-Synchronization Stability for Three-Phase Paralleled Converters (Outstanding Presentation Award)
Bo Wen, Dushan Boroyevich, Paolo Mattavelli, Rolando Burgos, Zhiyu Shen
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

A 30-W Flyback Converter Operating at 5 MHz
Zhemin Zhang, Khai D. T. Ngo, Jeff L. Nilles
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Multi-Level Single-Phase Shunt Current Injection Converter used in Small-Signal dq Impedance Identification
Marko Jaksic, Zhiyu Shen, Igor Cvetkovic, Dushan Boroyevich, Rolando Burgos, Paolo Mattavelli
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Small-Signal Impedance Identification of Three-Phase Diode Rectifier with Multi-Tone Injection
Bo Zhou, Marko Jaksic, Zhiyu Shen, Bo Wen, Paolo Mattavelli, Dushan Boroyevich, Rolando Burgos
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Adaptive Ripple-Based Constant On-Time Control with Internal Ramp Compensations for Buck Converters (Outstanding Presentation Award)
Kuang-Yao (Brian) Cheng, Fred C. Lee, Paolo Mattavelli
2014 APEC (29th Annual IEEE Applied Power Electronics Conference & Exposition), Fort Worth, Texas, March 16-20, 2014

Alternate Arm Converter (AAC) Operation Under Faulted AC-Grid Conditions
Ewan Farr, Ralph Feldman, Alan Watson, Rolando Burgos, Jon Clare, Pat Wheeler, Dushan Boroyevich
IET PEMD 2014, April 2014

High Frequency High Current Point of Load Modules with Integrated Planar Inductor
Wenli Zhang, Yipeng Su, David Gilham, Mingkai Mu, Qiang Li, Fred C. Lee
2014 Electronic Components & Technology Conference (ECTC), Orlando, FL, May 27-30, 2014

Efficiency Optimized AC Charging Waveform for GaN Bidirectional PHEV Battery Charger
Lingxiao Xue, Paolo Mattavelli, Dushan Boroyevich, Brian Hughes, Rolando Burgos
EPE'14 ECCE Europe, Lappeenranta, Finland, August 26-28, 2014

Modeling the Output Impedance of Three-Phase Uninterruptible Power Supply in D-Q Frame
Bo Wen, Dushan Boroyevich, Rolando Burgos, Paolo Mattavelli
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Evaluation and Control Design of Virtual-Synchronous-Machine-Based STATCOM for Grids with High Penetration of Renewable Energy
Chi Li, Rolando Burgos, Igor Cvetkovic, Dushan Boroyevich, Lamine Mili, Pedro Rodriguez
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Droop Voltage Range Design in DC Micro-Grids Considering Cable Resistance
Fang Chen, Wei Zhang, Rolando Burgos, Dushan Boroyevich
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Design and Evaluation of the Constant-Flux Inductor with Enclosed-Winding
Han Cui, Khai D. T. Ngo, Jim Moss, Michele H. Lim, Ernesto Rey
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Modular Interleaved Single-Phase Series Voltage Injection Converter Used in Small-Signal dq Impedance Identification
Marko Jaksic, Dushan Boroyevich, Paolo Mattavelli, Rolando Burgos, Zhiyu Shen, Igor Cvetkovic
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Compression of the Load Resistance Range in Constant Frequency Resonant Inverters (Best student poster session prize and also the best student poster presentation overall)
Milisav Danilovic, Khai D.T. Ngo, Zhemin Zhang
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

A New Core Loss Model for Rectangular AC Voltages
Mingkai Mu, Fred C. Lee
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Hybrid Interleaving Structure with Adaptive PLL Loop for Constant On-time Switching Converter
Pei-Hsin Liu, Fred Lee, Qiang Li
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Auto-tuning and Self-calibration Techniques for V2 Control with Capacitor Current Ramp Compensation Using Lossless Capacitor Current Sensing
Pei-Hsin Liu, Yingyi Yan, Fred C. Lee, Qiang Li
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Equivalent Circuit Model of Constant On-time Current Mode Control with External Ramp Compensation
Shuilin Tian, Fred C.Lee, Jian Li, Qiang Li, Pei-hsin Liu
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Thermal Analysis and Improvement of Cascode GaN HEMT in Stack-Die Structure
Shuojie She, Wenli Zhang, Weijing Du, Xiucheng Huang, Zhengyang Liu, Fred C. Lee, Qiang Li
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Modularized High Frequency High power 3-level Neutral Point Clamped PEBB cell for Renewable Energy System
Sizhao Lu, Yang Jiao, Mingkai Mu, Fred C. Lee, Zhengming Zhao, Liqiang Yuan, Ting Lu
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Gap Design for Nonlinear Ferrite Cores to Maximize Inductance
Ting Ge, Khai Ngo, Jim Moss, Michele Lim
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An Adaptive Backstepping Observer for Modular Multilevel Converter
Vahid Najmi, Hamed Nademi, Rolando Burgos
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High Reliability Capacitor Bank Design for Modular Multilevel Converters in MV Applications
Vahid Najmi, Jun Wang, Rolando Burgos, Dushan Boroyevich
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Energy Management System Control and Experiment for Future Home
Wei Zhang, Fred C. Lee, Pin-Yu Huang
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PUBLICATIONS

Avoiding Si MOSFET Avalanche and Achieving True Zero-Voltage-Switching for Cascode Devices
Xiucheng Huang, Weijing Du, Zhengyang Liu, Fred C. Lee, Qiang Li
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Multi-Channel LED Driver with CLL Resonant Converter
Xuebing Chen, Daocheng Huang, Qiang Li, Fred C. Lee
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

LCL Filter Design and Inductor Ripple Analysis for 3-level NPC Grid Interface Converter
Yang Jiao, Fred C. Lee
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Analysis and Filter Design of Differential Mode EMI Noise for GaN-based Interleaved MHz Critical Mode Boost PFC Converter
Yuchen Yang, Zhengyang Liu, Fred Lee, Qiang Li
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Loss Minimization for Coupled Inductors with Significant AC Flux
Zhemin Zhang, Milisav Danilovic, Khai D.T. Ngo, Jeff L. Nilles
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Exploration of a Switching Loop Snubber for Parasitic Ringing Suppression
Zheng Chen, Yiying Yao, Dushan Boroyevich, Khai D.T. Ngo, Paolo Mattavelli
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An Ultra-Fast SiC Phase-Leg Module in Modified Hybrid Packaging Structure
Zheng Chen, Yiying Yao, Dushan Boroyevich, Khai D.T. Ngo, Wenli Zhang
2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, September 14-18, 2014

Design and Evaluation of GaN-Based Dual-Phase Interleaved MHz Critical Mode PFC Converter
Zhengyang Liu, Xiucheng Huang, Mingkai Mu, Yuchen Yang, Fred Lee, Qiang Li
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DBC Switch Module for Management of Temperature and Noise in 220-W/in3 Power Assembly
Woochan Kim, Jongwon Shin, Khai D. T. Ngo
2014 International Microelectronics Assembly and Packaging Society (IMAPS), San Diego, CA, October 13-16, 2014

Compressive-Post Packaging of Double-Sided Die [Outstanding Student Paper Award]
Woochan Kim, Jia-Woei Wu, Bill Alexander, Sauvik Chowdhury, Collin Hitchcock, Nga C. Lee, James J. Q. Lu, T. Paul Chow, and Khai D. T. Ngo
2014 International Microelectronics Assembly and Packaging Society (IMAPS), San Diego, CA, October 13-16, 2014

Maximum Power Extraction in Wave Energy Harvesting System with Magnetostrictive Material
Jongwon Shin, Mudassar Khatib, Subhajyoti Mukherjee, Khai D. T. Ngo
2014 International Conference on Renewable Energy Research and Application (ICRERA), Milwaukee, WI, October 19-22, 2014

Fault Tolerant Operation of 5L-ANPC Converter
Jun Li, Jing Xu, Lisa Qi, Rolando Burgos
2014 IECON (40th Annual Conference of the IEEE Industrial Electronics Society), Dallas, TX, October 29-November 1, 2014

A Novel Control Method for Neutral Point Clamped Inverters with a Single Z-Source Network
Xiangyang Xing, Alian Chen, Weisheng Wang, Chenghui Zhang, Vahid Najmi
2014 IECON (40th Annual Conference of the IEEE Industrial Electronics Society), Dallas, TX, October 29-November 1, 2014

Investigation and Comparison of Cascaded H-Bridge and Modular Multilevel Converter Topologies for Medium-Voltage Drive Application
Alinaghi Marzoughi, Rolando Burgos, Dushan Boroyevich, Yaosuo Xue
2014 IECON (40th Annual Conference of the IEEE Industrial Electronics Society), Dallas, TX, October 29-November 1, 2014

Theses & Dissertations

High Temperature Characterization and Analysis of Silicon Carbide (SiC) Power Semiconductor Transistors
Christina DiMarino
Thesis, May 2, 2014

Characterization and Failure Mode Analysis of Cascode GaN HEMT
Zhengyang Liu
Thesis, May 8, 2014

Transformer Shielding Technique for Common Mode Noise Reduction in Switch Mode Power Supplies
Yuchen Yang
Thesis, May 9, 2014

On Methodology for Verification, Validation and Uncertainty Quantification in Power Electronic Converters Modeling
Niloofar Rashidi
Thesis, July 15, 2014

Two-Stage Multi-Channel LED Driver with CLL Resonant Converter
Xuebing Chen
Thesis, August 8, 2014

Multi-Phase Smart Converter for PV System
Zhongsheng Cao
Thesis, August 12, 2014

Design, Analysis, and Experimental Verification of a Mechanically Compliant Interface for Fabricating Reliable, Double-Side Cooled, High-Temperature, Sintered Silver Interconnected Power Modules
David Berry
Dissertation, August 13, 2014

Thermal Stability of Al2O3/Silicone Composites as High-Temperature Encapsulants
Yiying Yao
Dissertation, September 22, 2014

High Frequency, High Current 3D Integrated Point-of-Load (POL) Module
Yipeng Su
Dissertation, October 2, 2014

Identification of Small-Signal dq Impedances of Power Electronics Converters via Single-Phase Wide-Bandwidth Injection
Marko Jaksic
Dissertation, October 23, 2014

Development of Bidirectional Module using Wafer-Bonded Chips
Woochan Kim
Dissertation, November 18, 2014

Stability Analysis of Three-phase AC Power Systems Based on Measured D-Q Frame Impedances
Bo Wen
Dissertation, November 18, 2014

Power Management Consortium Nuggets

GaN-based MHz Totem-pole PFC Rectifier

Multi-Step Simplified Optimal Trajectory Control (SOTC) for LLC Resonant Converter

Simple Equivalent Circuit Model of a Series Resonant Converter

A Novel Phase Lock Loop (PLL)-based Interleaving Structure for Variable-Frequency Controlled Voltage Regulators

Characterization and Enhancement of High Voltage Cascode GaN Devices

Multiphase Smart Converter for PV System

Digital Hybrid Ripple-Based Constant On-Time Control for Voltage Regulator Modules

MHz LLC Resonant Converter Design with Planar Matrix Transformer for Telecom Application

Adaptive Synchronous Rectifier Driving Scheme for LLC Resonant Converter

Soft Start-up for High Frequency LLC Resonant Converter with Optimal Trajectory Control

New Variable Frequency Current Mode Control Using Charge Control Concept

Improved Current-Mode Control with Single-Step Load Transient

Simplified Optimal Trajectory Control (SOTC) for Burst Mode of High Frequency LLC Resonant Converter

PMC Research Team (April 2014 – April 2015):

Faculty:

Fred C. Lee

Qiang Li

Research Faculty:

Mingkai Mu

Graduate Students:

Mohamed Ahmed

Syed Bari

Zhongsheng Cao

Xuebing Chen

Chao Fei

Junjie Feng

Dongbin Hou

Yi-Hsun Hsieh

Xiucheng Huang

Bin Li

Virginia Li

Chen Li

Kai Li

Pei-Hsin Liu

Tao Liu

Zhengyang Liu

Yincan Mao

Xin Ming

Yipeng Su

Shuilin Tian

Yuchen Yang

Visiting Scholars:

Chaofeng Cai

Weijing Du

Wolfgang Granig

Peiqing Hu

Pin-Yu Huang

Daniel Li

Xin Ming

GaN-based MHz Totem-pole PFC Rectifier

With the advent of 600V gallium-nitride (GaN) power semiconductor devices, the totem-pole bridgeless power factor correction (PFC) rectifier, which was a nearly abandoned topology, has suddenly become a popular solution for applications like a front-end converter for server and telecommunication power supplies. This is mostly attributed to the significant performance improvement of the GaN high-electron-mobility transistor (HEMT) compared to the silicon (Si) metal–oxide–semiconductor field-effect transistor (MOSFET).

Based on previous study, soft switching truly benefits the cascode GaN HEMT. As the cascode GaN HEMT has a high turn-on loss and an extremely small turn-off loss due to the current-source turn-off mechanism, critical mode (CRM) operation is very suitable. In order to evaluate the impact and system-level benefits of high frequency, the cascode GaN HEMT is applied in the totem-pole PFC rectifier while pushing frequency to above 1MHz.

Several important high-frequency issues, which were less significant at low-frequency, are emphasized and the corresponding solutions are proposed. Detailed design considerations are presented in this work, including ZVS extension in order to solve switching loss caused by non-ZVS valley switching; variable on-time control to improve the power factor, particularly the zero-crossing distortion caused by negative current and traditional constant on-time control; and interleaving control for input current ripple cancellation.

Finally, a prototype of the 1.2kW 1MHz GaN-based dual-phase interleaved CRM totem-pole PFC rectifier is demonstrated. With ZVS soft switching, 99% peak efficiency is achieved at megahertz frequency range. And at the same time, the volume of passive components, like the inductor and the DM filter, are shrunk dramatically so that the power density of the system increases significantly to as high as 200W/in^3.

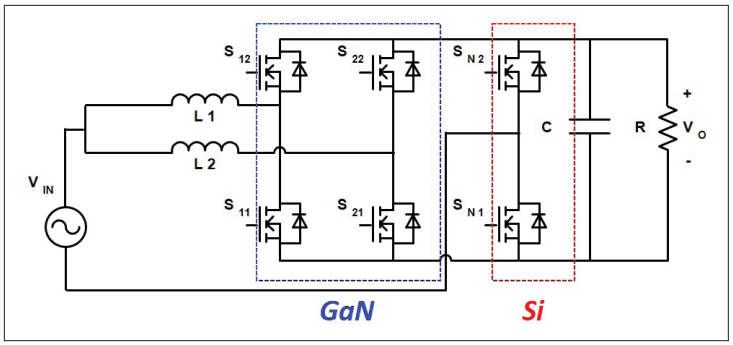

Fig. 1. GaN-based megahertz totem-pole PFC rectifier .

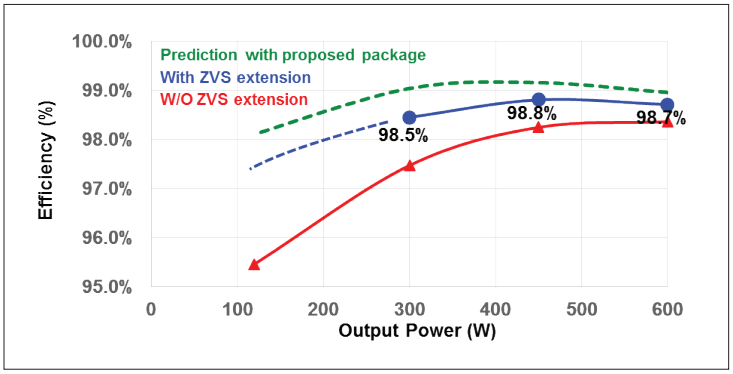

Fig. 2. Efficiency of single-phase totem-pole PFC rectifier.

Multi-Step Simplified Optimal Trajectory Control (SOTC) for LLC Resonant Converter

Simplified optimal trajectory control (SOTC) can solve the challenge of fast load transient response based on state-trajectory analysis. SOTC senses load current and modifies the pulse widths of driving signals, which works as a load current feed-forward loop and improves transient response significantly. In addition, digital controllers have superior advantages over analog controllers, and cost-effective microcontrollers (MCU) are preferred in industrial applications. High-frequency LLC converters have also become more popular in recent years due to their high power density and integrated magnetics, which reduce total cost. It is therefore useful to apply SOTC to the high-frequency LLC converter with low-cost MCU.

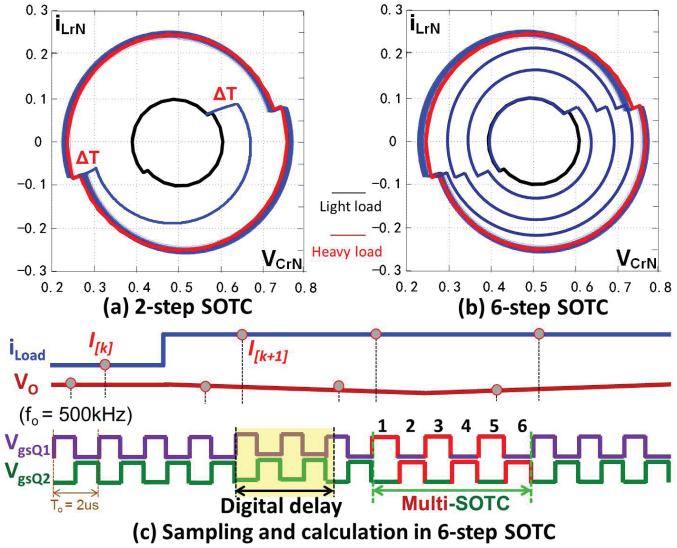

Fig. 1. Multi-step SOTC for high-frequency LLC converter.

In this work, first, implementation of SOTC is optimized and can be applied to the LLC converter with a maximum switching frequency of 250kHz with 60MHz MCU. To further improve switching frequency, multi-step SOTC is proposed to apply a low-cost MCU to a high-frequency LLC converter. The basic concept is that instead of using two-step SOTC to settle the resonant tank, which is the optimal method for the LLC converter, **n**-step SOTC is instead used to settle the resonant tank, in which **n** is determined by delay of controller and switching frequency of power stage (**n** = 1, 2, 3, 4…). The comparison of two-step SOTC and six-step SOTC is shown in Fig. 1(a) and Fig. 1(b). Fig. 1(c) is an example of implementation of multi-step SOTC for a 500kHz LLC converter, in which digital delay takes three switching cycles, and fast load transient response is achieved within six steps.

Multi-step SOTC for fast load transient response is verified on a 500kHz LLC converter, which is designed based on a matrix transformer for LLC resonant converters. The hardware is shown in Fig. 2(a). The experimental results of multi-step SOTC for load step up from 40A to 80A are shown in Fig. 2(b).

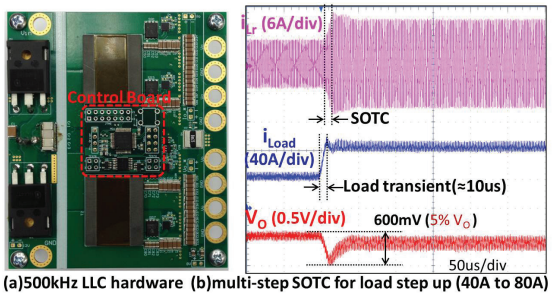

Fig. 2. Experimental results of multi-step SOTC on 500-kHz LLC.

In summary, the proposed multi-step SOTC settles resonant tank within **n**-step instead of fixed two-step, where **n** is selected based on delay of controller. Multi-step SOTC makes it feasible to use a low-cost MCU to control the high frequency LLC converter, while simultaneously achieving nearly the same performance as simplified optimal trajectory control.

Simple Equivalent Circuit Model of a Series Resonant Converter

The series resonant converter (SRC), shown in Fig. 1, is the simplest resonant converter. It is widely used for power conditioning in the sophisticated aerospace industry, as well as in some industrial applications, such as laser power supply. Up to now, the most successful equivalent circuit model proposed by E. Yang was based on the extended describing function method. However, the original equivalent circuit model is a complicated fifth-order circuit, and a numerical solution is used to obtain small-signal characteristics.

This nugget simplifies the original equivalent circuit model, and proposes a simple equivalent circuit model of a series resonant converter. Shown in Fig. 2, the proposed equivalent circuit model is a third-order circuit. The components C_e and L_e forms a beat frequency double pole and R_e is responsible for the damping. When switching frequency fs is far away from resonant frequency f_o, R_e is large. The quality factor of the beat frequency double pole is large, thereby enabling its observation. In this case, the circuit is a third order with a beat frequency double pole and a low frequency single pole caused by the output filter. When switching frequency f_s is close to resonant frequency f_o, R_e is small causing the beat frequency double pole to split. In this case, no beat frequency double pole is observed. Instead, L_e will resonant with output capacitor C_f to form a low frequency double pole. With the analytical model, the beat frequency dynamics can be explained, and the region where the beat frequency double pole is observed can be determined analytically. Furthermore, for the first time, analytical expressions of the transfer functions are derived. The equivalent circuit model and analytical transfer functions are valuable tools to design the feedback control appropriately.

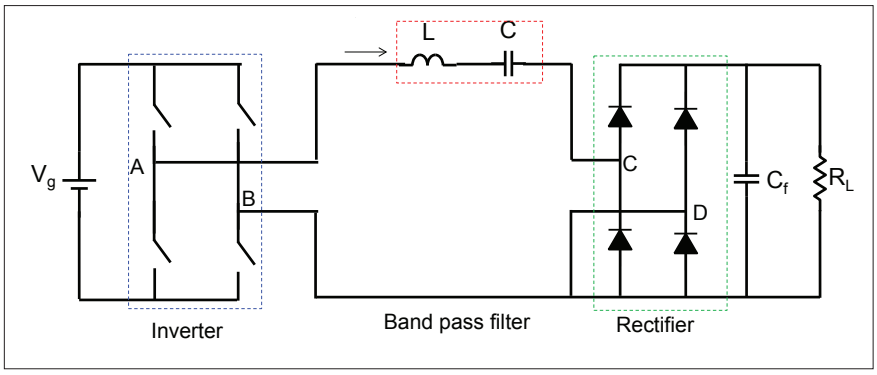

Fig. 1. Schematic of full-bridge series resonant converter (SRC).

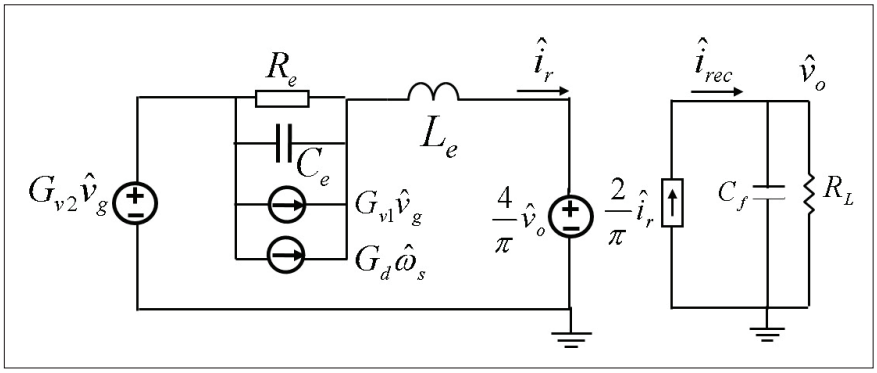

Fig. 2. Proposed simplified equivalent circuit model.

A Novel Phase Lock Loop (PLL)-based Interleaving Structure for Variable-Frequency Controlled Voltage Regulators

Ramp Pulse Modulation (RPM) has recently become widely used in the latest voltage regulator (VR) design of power microprocessors. The light load efficiency is as good as Constant On-Time (COT) control. Also, it saves more output capacitors than COT control, because both on time and off time can change immediately to improve load transient response. However, the switching frequency (f_{sw}) varies due to input voltage (V_{in}) and output voltage (V_o) changes, which makes interleaving challenging. Currently, a pulse distribution structure has been proposed to achieve interleaving and minimize frequency variation. Nevertheless, three issues limit its performance: first is the inability to overlap PWM signals during transient; second is the noise sensitivity caused by the ripple cancellation effect of the summed inductor current feedback; third is the reduction of fsw variation, which is not enough to minimize the impact on efficiency, and also generate a beat-frequency ripple by interacting with other VRs in a system.

This work proposes an interleaving method incorporating PLL to solve all above issues. Fig 1(a) shows the dual-phase configuration, where two PLL forces D_1 and D_2 follow two fixed-frequency clocks (f_{CLK1}, f_{CLK2}) in 180° phase shift by slowly adjusting on time through on-time control signals (V_{on1}, V_{on2}). The benefits are as following: firstly, D_1 and D_2 can be naturally overlapped to speed up the load transient, as shown in Fig. 1(b); secondly, since V_c compares with the individual phase current, the current feedback does not suffer a ripple cancellation; thirdly, since the steady-state f_{sw} is locked with f_{CLK}, so VR can operate at an optimal efficiency point; fourthly, the beat frequency ripple current is eliminated by synchronizing the clock frequency of every VR controllers in a multi-processor motherboard.

The loop gain of the PLL loop (TP) in Fig. 1(a) is analyzed by a proposed small-signal model, and the compensation guideline is provided. Moreover, enlightened by the model, an adaptive PLL loop is presented to simplify the loop compensation by auto-tuning the control bandwidth anchored at the peak phase margin, as shown in Fig. 2. After that, a hybrid interleaving technique, a combining pulse distribution method, and a PLL method are developed to significantly reduce the circuit complexity by using the PLL loop for the high phase number application, all while transient performance remains comparable. Finally, the simulation and experimental results verify the proposed method.

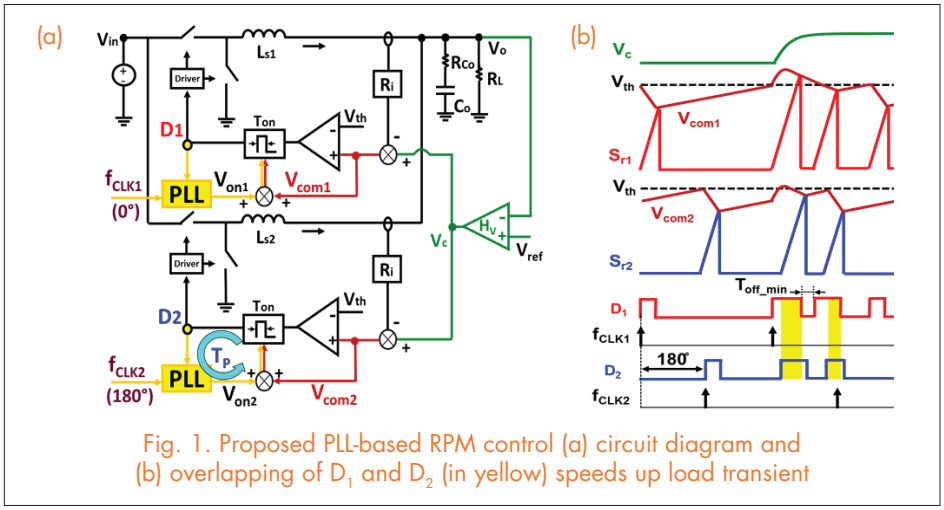

Fig. 1. Proposed PLL-based RPM control (a) circuit diagram and (b) overlapping of D_1 and D_2 (in yellow) speeds up load transient

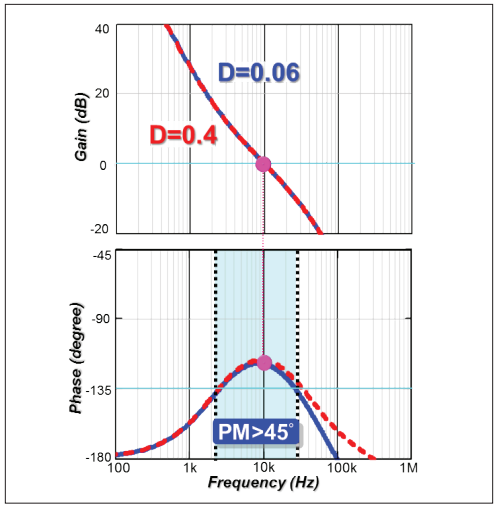

Fig.2. T_p of adaptive PLL loop

Characterization and Enhancement of High-Voltage Cascode GaN Devices

Gallium nitride (GaN) devices are gathering momentum, with a number of recent market introductions for a wide range of applications such as point-of-load converters (POL), offline switching power supplies, battery chargers and motor drives. This paper studies the basic characteristics of a 600V cascode GaN switch, such as voltage distribution during the turn-on and turn-off transitions. The switching loss mechanism of the cascode GaN switch is analyzed in detail, including the impact of the package parasitic inductance in both hard-switching and soft-switching modes. A soft-switching 5MHz boost converter is developed and shows the advantages and the potential of the cascode GaN.

For offline applications, enhancement-mode (normally-off) and depletion-mode (normally-on) GaN switches are available. The depletion-mode switches usually have a lower on-resistance and a smaller junction capacitance than the enhancement-mode switches. They are therefore deemed more attractive for applications that require high efficiency at a higher frequency. The depletion-mode GaN switch in series with a low-voltage silicon MOSFET is also an appealing alternative. This configuration is known as cascode structure. In the cascode structure, the voltage distribution between GaN and Si MOSFET may result in the unwanted avalanche of the Si MOSFET as well as the internal switching loss for the depletion-mode GaN switch even when it is intended to operate under the soft-switching turn-on transition. A simple and effective way to solve the issues is to add an extra capacitor in parallel with a drain source of Si MOSFET to compensate the capacitor charge mismatch as shown in Fig. 1. A parallel extra capacitor between the drain-source terminals of the Si MOSFET will not increase its driving loss, and the turn-off loss is still very small due to the merits of the cascode structure. This simple approach could enhance the switching performance of the cascode GaN switch. Moreover, this prevents the silicon MOSFET from reaching avalanche and improves the device reliability.

To demonstrate the advantages and explore the potential of the high-voltage cascode GaN switch, a 5 MHz 180V/400V CRM boost converter is developed. To avoid device capacitor mismatch and the package parasitic inductance impact on switching performance, a chip-on-chip packaged cascode GaN integrated with an extra capacitor (800 pF, 1mm x 0.5mm x 0.5mm) is fabricated and applied in this converter. The prototype of the cascode GaN switch and the boost converter are shown in Fig. 2. The converter can achieve 98% efficiency and 1000 W/in^3 power density at 600W output conditions.

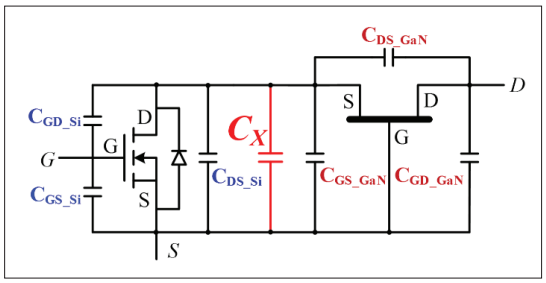

Fig. 1. Adding an extra capacitor to the cascode GaN switch.

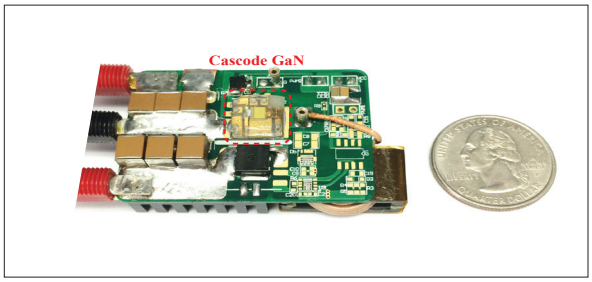

Fig. 2. Prototype of 5 MHz converter with cascode GaN switch.

Multiphase Smart Converter for PV System

Recent research and industrial accomplishment has revealed the advantages of a cascaded, smart converter, photovoltaic (PV) system over a traditional centralized and string PV system. However, a smart converter normally has a higher cost than the central-level or string-level MPPT PV system due to each smart converter needing an individual MPPT controller, along with voltage and current sensors. To solve this problem, a multiphase smart converter with a single controller is proposed in this work. By comparing to a traditional smart converter, the proposed solution can largely reduce cost by saving MPPT controllers, current and voltage sensors without sacrificing energy production. The effectiveness of the proposed structure is verified by both simulation and hardware testing. The proposed multiphase smart converter also can be extended to work on subpanel-level and string-level multiphase PV converters.

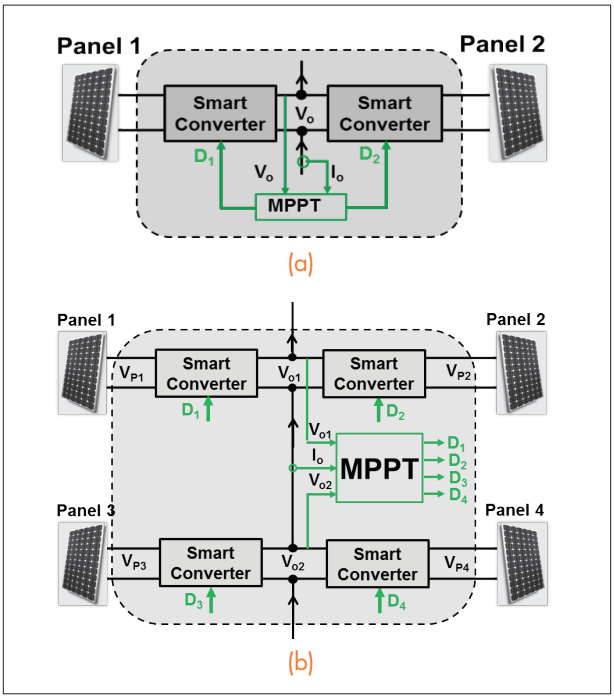

Fig. 1. Proposed multiphase smart converter: (a) 2-phase smart converter; (b) 4-phase smart converter.

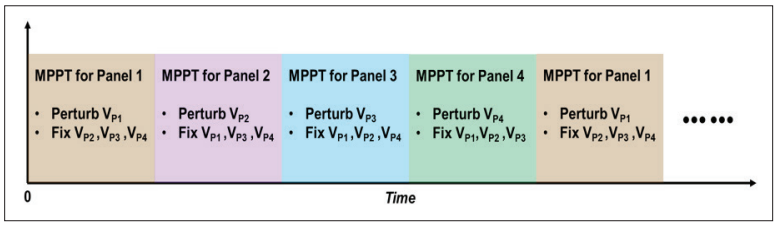

Fig. 2. Concept of time-sharing MPPT control for a 4-phase smart converter.

Digital Hybrid Ripple-Based Constant On-Time Control for Voltage Regulator Modules

This paper presents a digital hybrid ripple-based constant on-time control scheme for voltage regulator modules (VRMs). Due to the sampling effects of the digital implementation, stability issues become worse than in analog ripple-based control schemes, especially when low-ESR decoupling capacitors are used to filter output. In order to stabilize the system and fulfill the output impedance requirements of adaptive voltage positioning (AVP), a hybrid ramp-compensation strategy, which includes the external ramp and the estimated current ramp, is proposed. A small-signal model of the proposed architecture is derived to provide the design guideline for the ramp compensation gains and the number of output and decoupling capacitors. In addition, only low sampling-rate analog-to-digital converters (ADCs) are required to sample the input voltage, the output voltage, and the average current, making the proposed architecture compatible with the cost/complexity constraints of VRM applications. Simulation and experimental results show that the ripple-based control scheme can be used to achieve high-bandwidth performance, and the proposed digital control architecture can fulfill the AVP design requirements of single-phase VRMs.

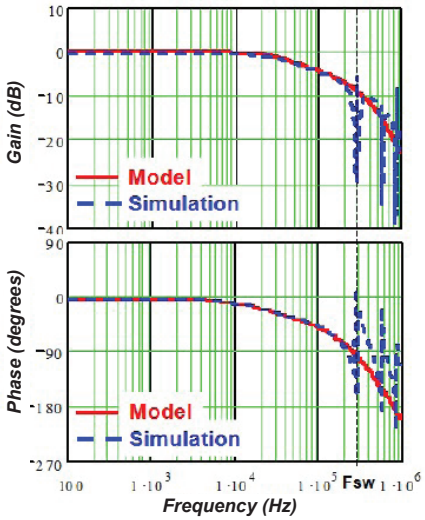

Fig. 1. Comparison of the control-to-output transfer function of the analog enhanced ripple-based control scheme with capacitor combinations.

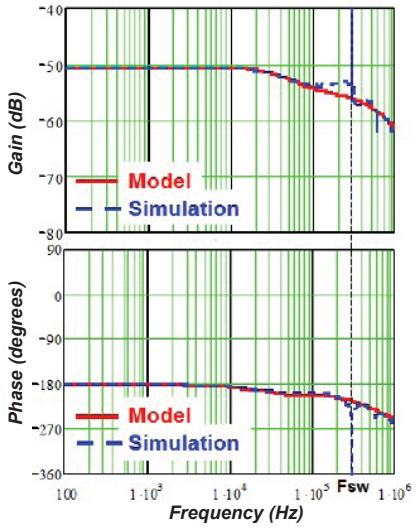

Fig. 2. Comparison of the output impedance transfer function of the analog enhanced ripple-based control scheme with capacitor combinations.

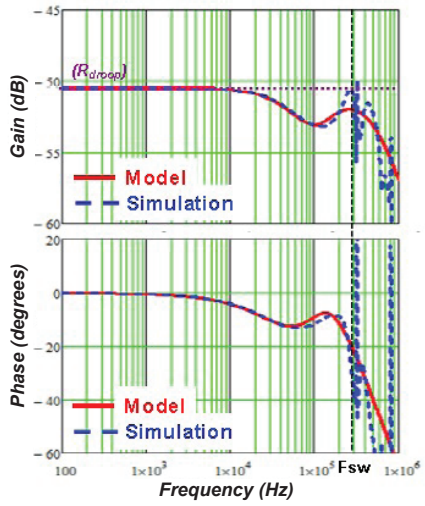

Fig. 3. Theoretical and simulated frequency response of the output impedance of the proposed hybrid ripple-based constant on-time control scheme.

MHz LLC Resonant Converter Design with Planar Matrix Transformer for Telecom Application

Today's single-phase telecom power supply modules usually consist of two stages: an ac-dc PFC stage, which converts the ac line input to a 400V dc bus; and an isolated dc/dc stage, which regulates the 400V DC bus to a 48V intermediate bus. For the second stage, LLC resonant conversion is popular due to its inherent soft switching mechanism and hold-up capability. In addition, the maturity of wide-bandgap devices, such as the Gallium Nitride (GaN) MOSFET, offers an opportunity to push the switching frequency up to multi-MHz, bringing the efficiency and power density of the secondary stage to a new level. However, with use of this high switching frequency, further study of the converter's design, especially the magnetic component, is necessary.

A design procedure for the secondary dc/dc stage is proposed. First, the secondary side topology is chosen from among a full bridge rectifier, voltage doubler, and center tap, according to the trade-off between device number, device stress, core loss, and winding loss. Second, the primary side and secondary side of the device are selected according to the breakdown voltage, R_{dson} and Q_g, which represent its conduction loss and switching loss respectively. Third, in order to get a low profile, and easily manufacture the converter, a multi-layer PCB-winding-based planar transformer is used, as shown in Fig. 1. This winding structure takes into consideration interleaving between windings as well as termination between windings and synchronous rectification devices, and helps to minimize the ac winding loss due to proximity and skin effect, which is dominant over dc winding loss in high-frequency applications. Fourth, an analytical transformer loss model is constructed based on three kinds of transformer loss: 1) winding loss, 2) core loss and 3) termination loss. The Dowell equation and modified Steinmetz equation are adopted to calculate the winding loss and core loss respectively, and 3D FEA simulation is used to determine the termination loss. This analytical transformer loss model is verified by 3D FEA simulation. With this loss model, much simulation time can be saved and an optimized transformer design with the lowest loss and volume is accomplished, as shown in Fig. 2, which also shows the predicted efficiency curve.

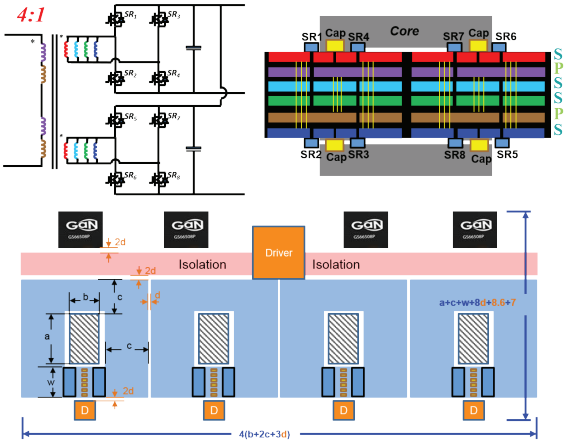

Fig. 1. Multi-layer PCB winding based planar transformer.

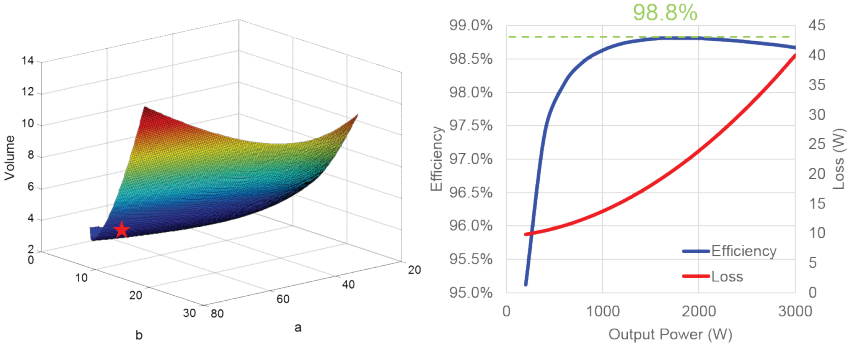

Fig. 2. Transformer optimization and converter efficiency prediction.

Adaptive Synchronous Rectifier Driving Scheme for LLC Resonant Converter

To improve the LLC resonant converter's overall efficiency, synchronous rectifiers (SRs) should be employed. It is important to choose SR gate driving signals that provide the greatest efficiency for the LLC resonant converter due to the discrepancy between the driving of primary and secondary switching. Digital controllers also have notable advantages over analog controllers. Among digital controllers, cost-effective microcontrollers (MCU) are preferred in industrial applications. It is therefore advantageous to implement adaptive SR driving via MCU instead of using additional SR control chips.

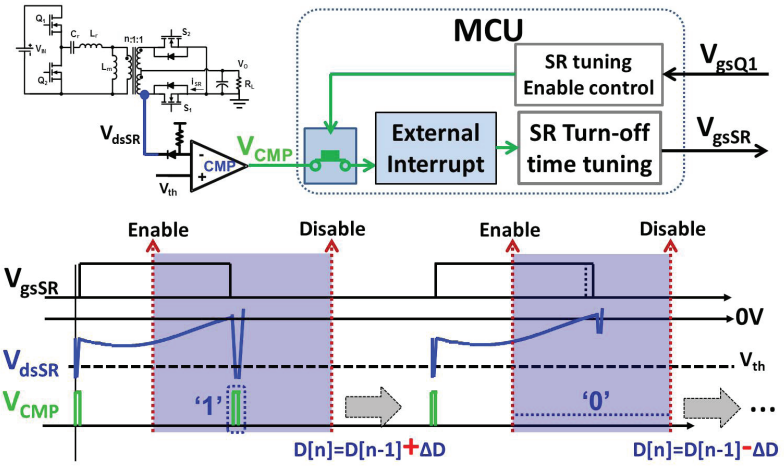

Fig. 1. MCU-based implementation of adaptive SR driving for a conventional LLC converter.

The drain-to-source voltage of the synchronous rectifier is sensed and compared with the threshold voltage in order to detect the paralleled body diode conduction. For the conventional LLC converter, the SR turn-on time is synchronized with the primary side switches, and the SR turn-off time is tuned to eliminate body diode conduction based on the output of the comparator, which is in turn connected to the external interrupt of MCU, as shown in Fig. 1.

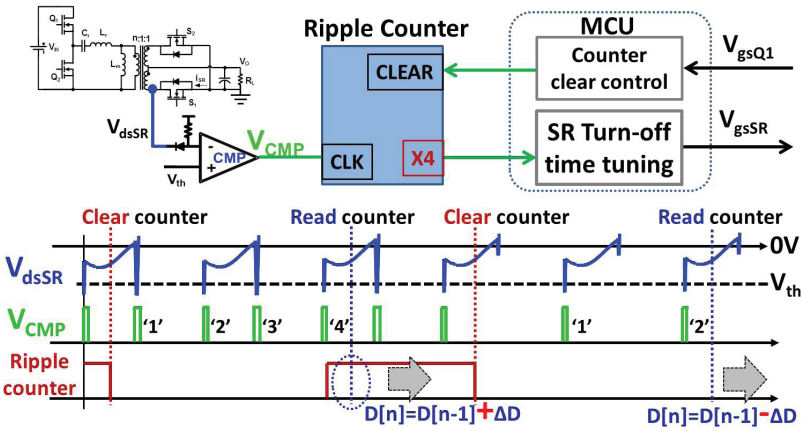

Fig. 2. MCU-based implementation of adaptive SR driving for a high-frequency LLC converter.

For the high-frequency LLC converter, if the SR turn-off time is tuned every switching cycle, the CPU of the MCU will be busy most of the time. To release the burden on the MCU, the output of the comparator is connected to a ripple counter instead of the external interrupt of the MCU, as shown in Fig. 2. The SR turn-on time is still synchronized with the primary side switches, but the SR turn-off time is tuned based on the status of the counter's output. The counter is cleared every third switching cycle for a 500kHz LLC converter.

Adaptive SR driving for a conventional LLC converter is verified on a 130kHz LLC converter with MCU TMS320F2808. Adaptive SR driving for a high frequency LLC converter is verified on a 500kHz LLC converter with MCU TMS320F28027. The desired performance is achieved in both cases.

Soft Start-Up for the High-Frequency LLC Resonant Converter with Optimal Trajectory Control

Start-up is the most critical process in the control of the LLC resonant converter. Very large current and voltage stresses can occur if the process is not well controlled. Optimal trajectory control (OTC) for soft start-up is used to address this problem. Note that in this scenario, digital controllers have superior advantages over analog controllers. Among digital controllers, cost-effective microcontrollers (MCU) are also preferred in industrial applications for the power supply of the server, telecom, datacenter, and so on. Further efforts need to be made to determine how to reduce the impact of the digital delay so that soft start-up can be implemented with commercial low-cost MCUs.

Two methods are proposed to solve this problem. One proposed method is a mixed-signal implementation, as shown in Fig. 1(a). In addition to the MCU, there are two comparators in the analog portion. The resonant current i_{Lr} is sensed as the positive input of Comparator 1 and the negative input of Comparator 2. The positive band is set to be I_{MAX} as the negative input of Comparator 1. The negative band is controlled by the MCU, which is $-I_{LM}$ in Stage 1 and $-I_{MAX}$ in Stage 2. The outputs of the two comparators are directly fed back to the PWM module in the MCU. Since the propagation delay of the comparators and PMW module is negligible, the delay of the whole control loop is very small, and thus suitable for the optimal trajectory control for soft start-up. Another proposed method is digital implementation with a look-up table, as shown in Fig. 1(b), which only requires the sensing of V_O. The table in Fig. 1(b) is based on the parameters of a 130-kHz LLC power stage. When the input voltage reaches around 400V, the MCU will start the soft start-up process. In Stage 1, the pre-calculated $\Delta T1$, $\Delta T2$ … ΔTn are consequently generated. In stage 2, the MCU senses V_O and controls the switching frequency based on the pre-calculated f_S vs. V_O table. In Stage 3, the MCU decreases the switching frequency gradually until V_O = 12V.

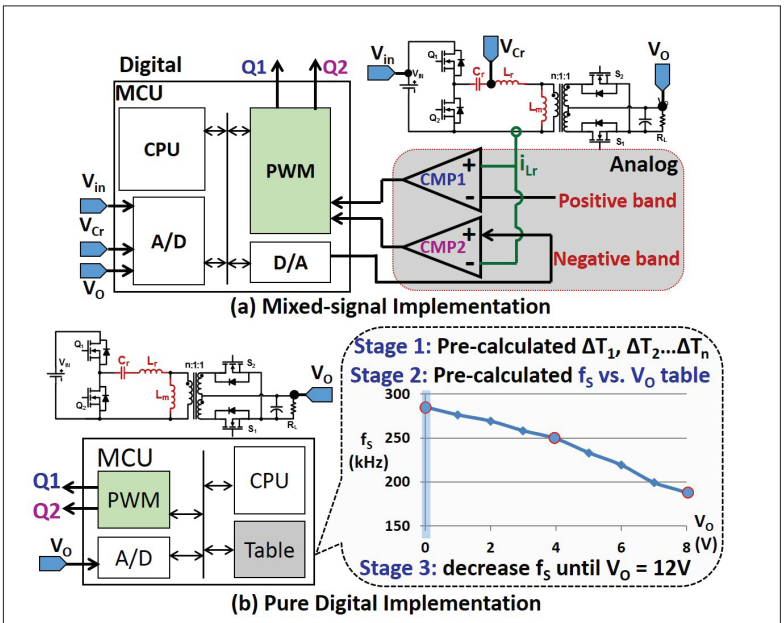

Fig. 1. Two methods of implementation for soft start-up.

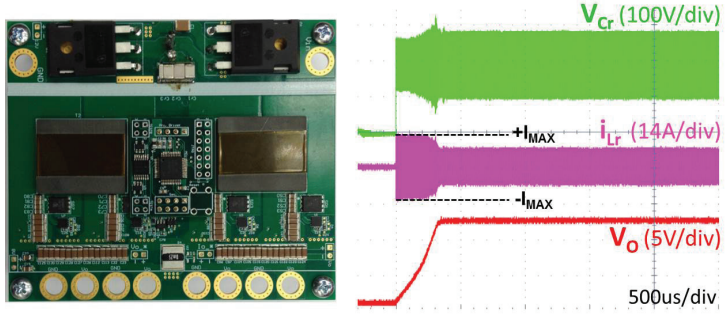

Fig. 2. 500kHz 1kW LLC converter and soft start-up waveform.

Method 2 for soft start-up is verified on a 500kHz LLC converter. The hardware of the 500kHz LLC converter and the soft start-up waveform are shown in Fig. 2. The start-up condition is 385V input voltage and 0.178 Ω resistive load (81% load). Results show the whole start-up process to be smooth and the maximum resonant current to be within the current limiting band.

New Variable Frequency Current Mode Control Using Charge Control Concept

Ripple-based current mode control is currently very widely used for its excellent small signal property. The issue of this ripple-based current mode control is that when the inductor current ripple becomes small because of the ripple cancellation effect for a multiphase operation, control becomes very noise sensitive, and creates a jittering at the output. Today, constant on-time control is widely used for VR applications because of its higher light-load efficiency, and higher bandwidth design capability. In the constant on-time control, current mode control based on the inductor current ripple is very widely used because of its very simple compensation. One issue of the ripple-based current mode constant on-time control is that, in the heavy load step up transient, the inductor current increment becomes limited by on-time and minimum-off-time ratio in each cycle. This can create a large undershoot at the output. On the other hand, in the load step-down case, if the load change occurs at the beginning of the fixed T_{on}, a large overshoot can occur at the output as well. For the multiphase operation case, a limited pulse overlapping capability of different phases becomes an issue at heavy load step up transient. A new current mode control based on a charge control concept is proposed to solve these limitations of ripple-based current mode controls.

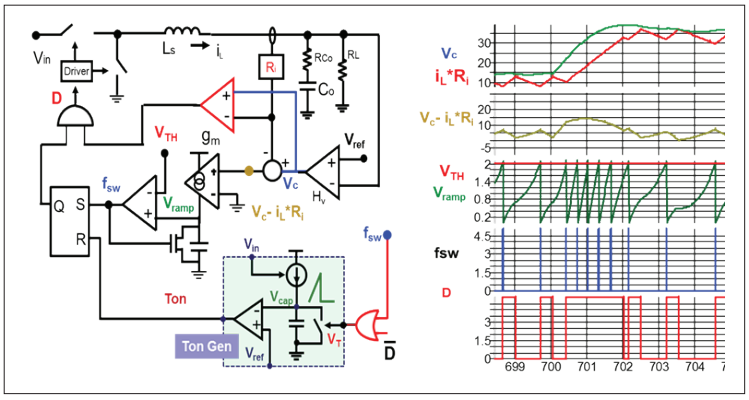

Fig. 1. Proposed constant on-time charge control with waveforms.

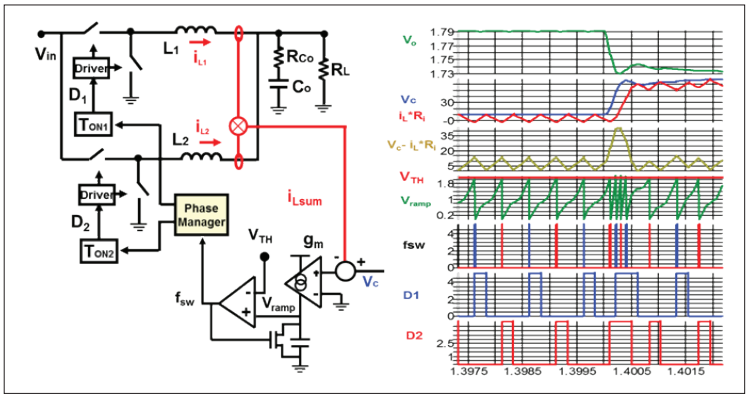

Fig. 2. Proposed control for multiphase with waveforms.

The proposed structure with its waveforms in load step up transient response is presented in Fig. 1 where the difference between V_c and I_L x R_i is converted into current by using a gm amplifier, and this current is used to charge a capacitor. Then this capacitor voltage (V_{ramp}) is compared with a fixed threshold voltage (V_{TH}) to create pulse frequency f_{sw}. When V_{ramp} touches V_{TH}, off time ends and a fixed on time (T_{on}) is started. In the case of a large load step up transient, when $V_c - I_L$ x R_i becomes very large, f_{sw} pulses can occur even before the end of the previous on time. If these very close pulses are allowed to merged together to create a longer on-time, significant undershoot reduction can be done at the output.

In the proposed structure, a control pulse can occur even before the on-time finishes. In a multiphase operation, the proposed COT charge control can improve the load step up transient performance by achieving a natural pulse overlapping feature, shown in Fig. 2.

The main features and advantages of this proposed method are: transient improvement by natural T_{on} extension at load step-up, transient improvement in a multiphase operation by natural pulse overlapping, improvement of noise sensitivity at the ripple cancellation point, and a truncated T_{on} at load step-down, which makes it very easy to reduce overshoot.

Improved Current-Mode Control with Single-Step Load Transient

For dc-dc converters, variable-frequency controls are widely used to improve light-load efficiency, increase transient response speed, and reduce the amount of output capacitors by utilizing high-bandwidth designs. Two popular variable-frequency current-mode controls are constant on-time (COT) and ramp pulse modulation (RPM). COT control achieves variable frequency by having a fixed on-time (T_{on}). Since the input voltage (V_{in}) and output voltage (Vout) vary, with fixed T_{on}, the frequency naturally varies. However, due to the fixed Ton, the performance of COT is limited during transient. Unlike COT, RPM operates with variable frequency and variable T_{on}. The transient performance of RPM is better than the COT due to the variable Ton. Although the load step-up transient performance of RPM is better than COT, it may still take multiple steps to achieve a steady-state.

The fastest transient response can be achieved using a single-step transient. Two methods to improve the load step-up transient performance of COT and RPM to achieve a single-step transient response are proposed. For both methods, transient detection utilizes the V_{com} signal. Unlike RPM, COT does not use V_{com} however, V_{com} can be created using the COT control signals.

For the first method, shown in Fig .1 using RPM as an example, V_{com} and a single V_{up}, placed above V_{th}, are used to determine transient. Transient is determined when V_{com} increases higher than V_{up} and ends when V_{com} decreases below V_{th}. During transient, S_r is turned off to extend T_{on}. Once transient ends, normal control operation is resumed and a single-step load step-up transient response is achieved. This method is extended to the multiphase operation but undesirable ringback can be observed due to total phase overlapping while using the original control scheme to turn off T_{on}.

For the second method, shown in Fig. 2 using RPM as an example, Vcom and two V_{up} thresholds are used to determine transient. Transient is determined when V_{com} increases higher than V_{up1}, placed above V_{th}, and ends when V_{com} reaches V_{up2}, placed at V_{com_min}. During transient, an additional $K \times V_c$ signal is injected into the V_{com} signal that is compared with S_r only. This does not affect the V_{com} used for transient detection or any other part of the control. The gain of the injected signal, K, must be high enough such that S_r will not reach the modified signal until the termination of the transient. Once transient ends, the modified V_{com} signal drops due to the termination of the injected signal, and meets with S_r, thus turning off T_{on} and a single-step load step-up transient response is achieved. Since this modified transient detection allows the T_{on} to be terminated once the modified transient detection ends, it allows the T_{on} to be better controlled in a multiphase operation to alleviate the ringback issue observed in the first method.

For a single-phase transient, the second method yields the same results as the first method. For a multiphase transient, the second method relieves the ringback issue of the first method. Both proposed improvement methods effectively and easily allows a single-step load step-up transient response to be achieved for current-mode controls.

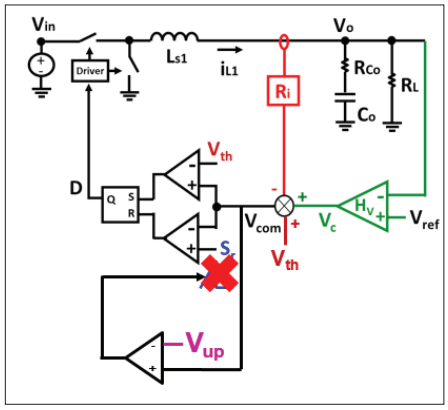

Fig 1. RPM with proposed single-step load transient improvement.

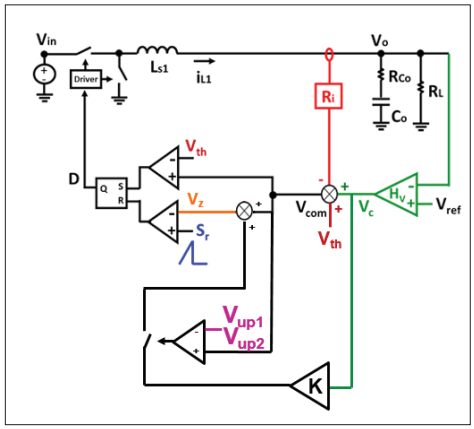

Fig 2. RPM with proposed improved single-step load transient improvement

Simplified Optimal Trajectory Control (SOTC) for Burst Mode of High Frequency LLC Resonant Converter

The light-load efficiency of an LLC converter with frequency control cannot meet increasing efficiency requirements, such as 80 PLUS® and ENERGY STAR. The high-frequency LLC converter has become more popular in recent years due to its high power density and integrated magnetics, which reduce total costs. And digital controllers, especially cost-effective microcontrollers (MCU), are gradually taking the place of analog controllers of LLC resonant converters. It is therefore worthwhile to extend burst mode to the high-frequency LLC converter with low-cost MCUs.

Due to the dynamics of the resonant tank, conventional burst control for the LLC converter is problematic in that the resonant tank cannot maintain the efficiency-optimal state trajectory. Based on state-plane analysis, the OTC for burst mode with a fixed three-pulse pattern can solve this problem. However, when the OTC for burst mode is applied to the high frequency LLC converter with MCU, the burst mode operation range is limited. This is because in burst off-time, the digital controller must leave enough time to blank sensing noise, sample, and update control signal. With minimum off-time T_{off_min}, the maximum average power delivered to the secondary side is limited, as shown in Fig. 1(a).

To extend the burst operation range for the high-frequency LLC converter, SOTC for burst mode with adaptive burst on-power and adaptive multi-step are proposed in this paper. The first strategy is to increase the burst on-power; however, the desired trajectory is not fixed to the efficiency-optimal trajectory. The second strategy is to increase the burst pulses as shown in Fig. 1(b). This strategy works using the following principles: assuming the load increases from an empty load, initially a three-pulse pattern is applied; when the load increases to the three-pulse pattern's limit, then a five-pulse pattern is applied; the same principles are applied going forward.

The SOTC for burst mode with adaptive multi-step is verified on a 500kHz LLC converter controlled by a 60MHz MCU. The efficiency curve is shown in Fig. 2, and light efficiency improvement is shown to be significant compared with conventional burst mode.

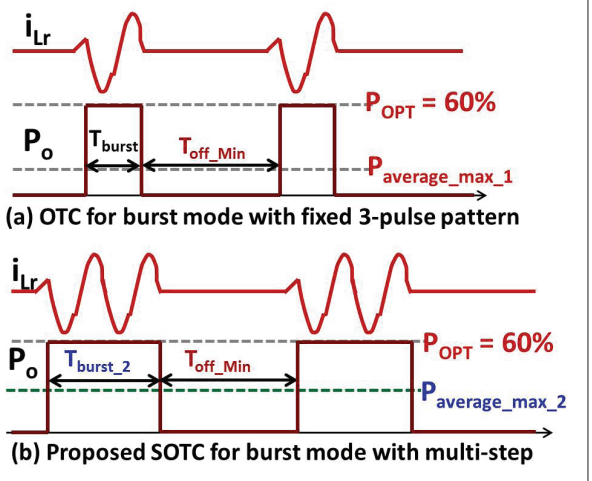

Fig. 1. Comparison of OTC for burst mode and SOTC for burst mode with multi-step.

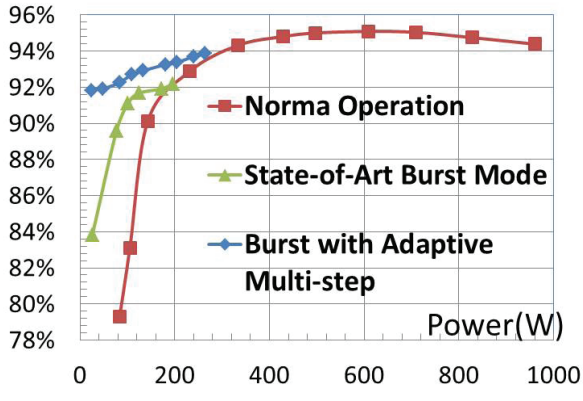

Fig. 2. Efficiency of proposed burst mode for high-frequency LLC converter.

High Density Integration Nuggets

Balance Technique for MHz-Critical Mode PFC Rectifier with Coupled Inductor

Design of 3.3kW Wireless Inductive Power Transfer System with 95% Efficiency Over 10cm Air Gap

Analysis of Dead Time Influence on Common Mode Volt-Second and Inductor Saturation in Three-Phase DC-Fed Motor Drive Systems

On Discussion of Mixed Mode Noise in H-Bridge Converters

Temperature Cycling Reliability Assessment of Die-Attachment on Bare Copper by Pressureless Nanosilver Sintering

Efficiency optimized AC charging waveform for GaN Bidirectional PHEV Battery Charger

GaN-based High Frequency Totem-Pole Bridgeless PFC Design with Digital Implementation

Characterization of 650V enhancement mode GaN HEMT

An Ultra-Fast SiC Phase-Leg Module in Modified Hybrid Packaging Structure

Integrated Design by Optimization of Electrical Power Systems for More Electric Aircraft

HDI Research Team (April 2014 – April 2015):

Faculty:

Dushan Boroyevich

Rolando Burgos

Fred Lee

Qiang Li

Guo-Quan Lu

Khai Ngo

Research Faculty:

Fang Luo

Zhiyu Shen

Xuning Zhang

Graduate Students:

David Berry

Helen Cui

Christina DiMarino

Ye Fan

Nidhi Haryani

Marko Jaksic

Tao Liu

Zheygyang Liu

Ming Lu

Alinaghi Marzoughi

Vahid Najmi

Yipeng Su

Jun Wang

Lingxiao Xue

Yuchen Yang

Yiying Yao

Lujie Zhang

Shishuo Zhao

Hanguang Zheng

Visiting Scholars:

Kenta Emori

Jongwon Shin

Seiya Yuki

Balance Technique for MHz-Critical Mode PFC Rectifier with Coupled Inductor

The coupled inductor has been widely adopted in VR applications for many years because of its benefits, which include reducing current ripple and improving transient performance. In this presentation, the coupled inductor concept is applied to an interleaved megahertz Totem-pole CRM PFC converter with GaN devices. The coupled inductor in the CRM PFC converter can reduce switching frequency variation, which helps to achieve ZVS, and reduce circulating energy. Hence, the coupled inductor can improve the performance of the PFC converter. In addition, a balance technique is applied to help minimize the CM noise. Previously, the balance technique was developed for an interleaved boost PFC converter with independent inductors. This presentation will introduce how to achieve balance with a coupled inductor. The inductor design procedure and FEA simulation will be provided.

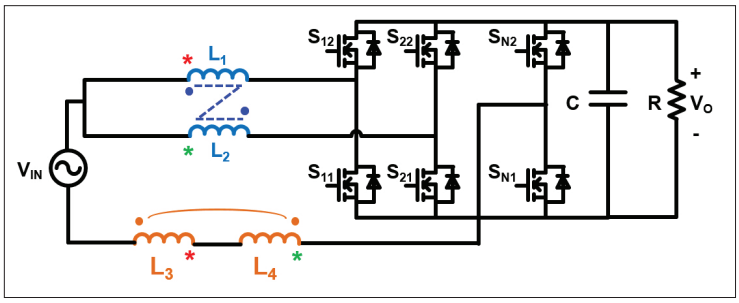

Fig 1. Interleaved megahertz totem-pole PFC with coupled inductor and balance technique.

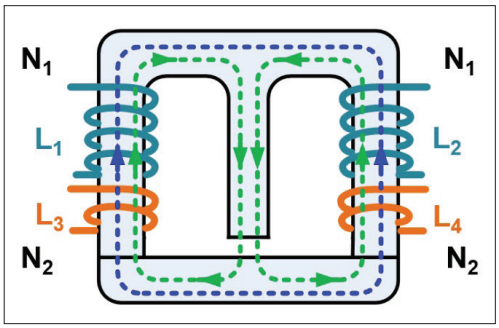

Fig 2. Inductor core structure (principle drawing).

Design of 3.3kW Wireless Inductive Power Transfer System With 95% Efficiency Over 10cm Air Gap

By transferring energy through a magnetic field between transmitter and receiver coils, a wireless inductive power transfer (WIPT) system is a good solution for charging electric vehicles (EVs), as it eliminating plugs and cords, making the charging process more convenient. However, the disadvantages of wireless charging for EVs include lower efficiency than traditional charging methods, sensitivity to misalignment between transmitter and receiver coils, and radiated EMI problems. This work focuses on solving the efficiency problem with proper design procedures for the WIPT system, including transmitter and receiver coils, resonant capacitors, and converters. The designed WIPT system, as shown in Fig. 1, can transfer 3.3kW of power over a 10cm air gap with 95% efficiency.

The coil design includes optimization of coil structure, and selection of inductance, and calculation of ac resistance. Circular planar coils with ferrite plates placed below are used, and the coupling coefficient between the transmitter and receiver can achieve 0.25 when perfectly aligned. The range of the inductance value is selected based on the operating frequency range (90 – 110kHz) and the power requirement (P_{out} = 3.3kW). The turns number is tuned to change the self-inductance within the selected range for an optimized coupling coefficient, winding loss, and density. The ac resistance of the coils is calculated based on the Bessel function, with magnetic field information from an FEA simulation.

Resonant capacitors face the problem of high-voltage stress up to 1.3kV RMS value at 100kHz. To solve this problem, a capacitor bank of film capacitors is applied, with 87 capacitors on the primary side and 38 on the secondary side. Calculations show that the conduction loss on the resonant tanks is 1.8% for 400V output and 3.3kW output power.

Frequency control is implemented for the primary side inverter. The hardware of the inverter is shown in Fig. 2. When the output voltage or coupling coefficient changes, frequency has to be adjusted for 3.3kW output power. Soft switching is achieved for turn-on due to the coils' design for operating frequency range, and hard switching for turn-off. Experimental results prove that 95% efficiency is achieved for 3.3kW output power.

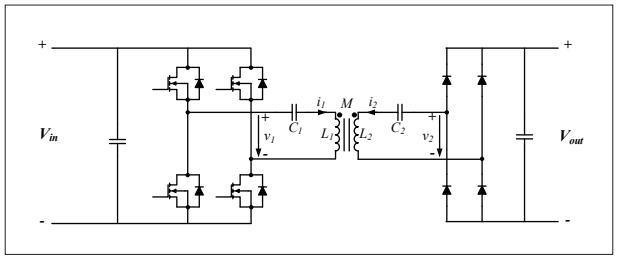

Fig. 1. Topology of the designed 3.3 kW WIPT system, with primary side full bridge inverter, series-series resonant tanks, and secondary side diode bridge.

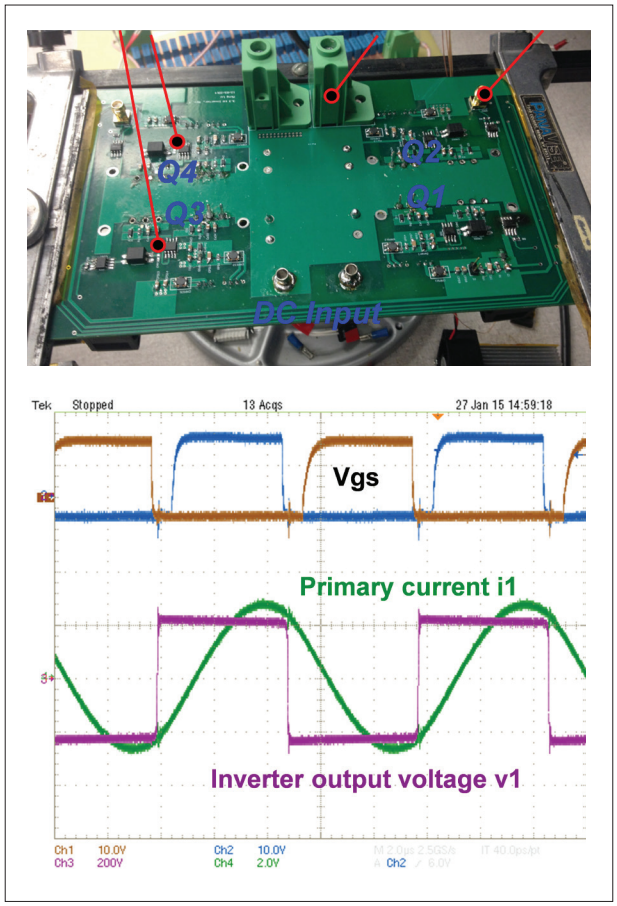

Fig. 2. Hardware of the full bridge inverter used for the WIPT system and waveforms for its output voltage and current.

Analysis of Dead-Time Influence on Common Mode Volt-Second and Inductor Saturation in Three-Phase DC-Fed Motor Drive Systems

In dc-fed motor drive systems as shown in Figure 1, EMI filters are inevitable parts that provide EMI noise attenuation to avoid interference between different components. In the EMI filter design process, inductor volt-second is an important design condition for inductor optimization. In order to predict the volt-second for inductor optimization, a frequency domain prediction model is proposed in Fig. 2. The noise source can be calculated using a double Fourier integral transformation method, and the propagation path impedance can be directly measured from the system or calculated based on the impedance model in frequency domain. With the proposed model, the inductor volt-second can be predicted accurately and the model is verified through experimental tests.

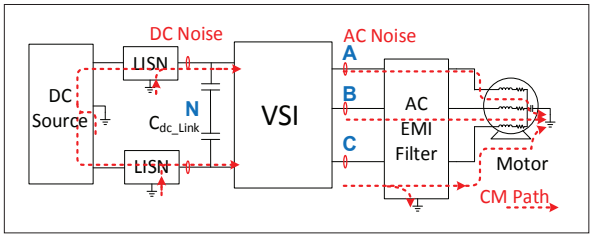

Fig. 1. DC-fed motor drive system with EMI Filters.

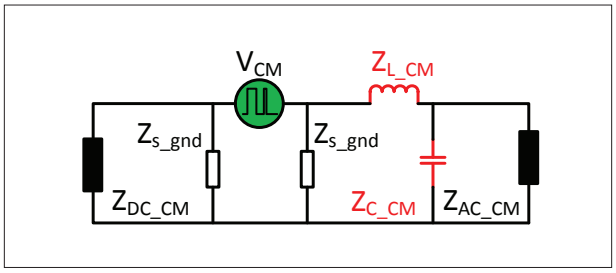

Fig. 2. Inductor volt-second prediction model.

In real applications, dead time is necessary to avoid a shoot-through error in the converter. Dead time (DT) will change the voltage noise source in the prediction model as shown in Fig. 3, therefore it also changes the volt-second on the inductor. Fig. 4 shows the impact of DT on inductor volt-second with continuous SVM modulation method. The results (Fig. 5) show that the impact of dead time on inductor saturation is related to system modulation methods, dead time value and also the value selection of the inductors and capacitors of the EMI filters. The dc-fed motor drive system with an output EMI filter is chosen as an example, and the analyzing method can also be applied to other converters.

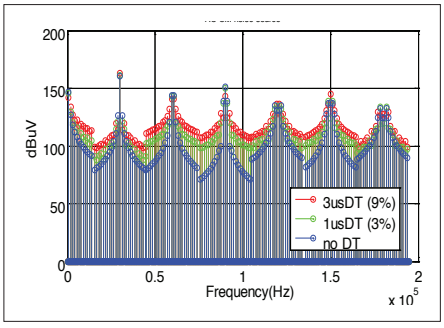

Fig. 3. Voltage spectrum change with dead time.

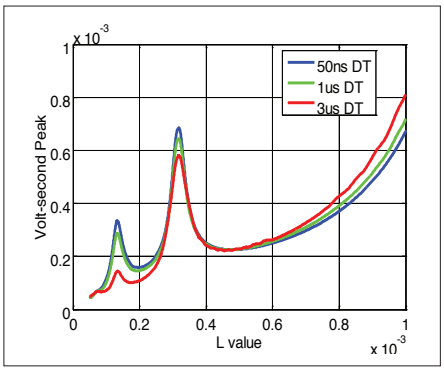

Fig. 4. Impact of DT on inductor volt-second.

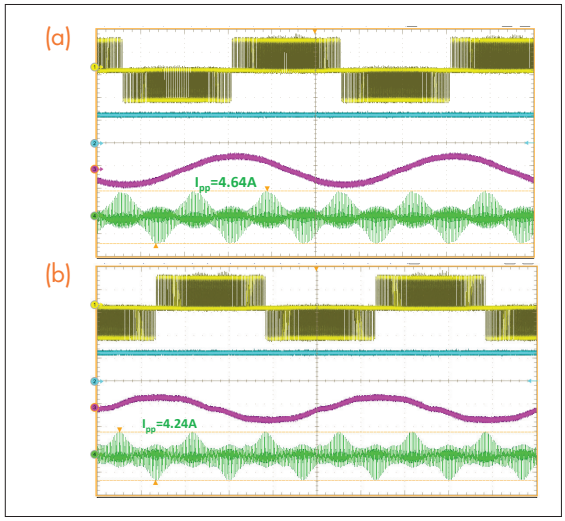

Fig. 5. 150 uH EMI filter test results (V_{dc}=270 V) (V_{ab}: yellow (200V/div); V_{dc}: Blue (200V/div); I_{out}: pink (20A/div); I_{cm_L}: green (2A/div))

On Discussion of Mixed Mode Noise in H-Bridge Converters

PWM converters have made a significant contribution when it comes to achieving energy conservation, and improving system performance in many applications, such as transportation systems and renewable energy systems. In single-phase applications, H-bridge converters, such as the VSI or PFC circuit (shown in Fig. 1), are commonly used due to their good performance. In such applications, certain electromagnetic interference (EMI) standards must be met to ensure that the system is working normally, and filters are inevitable in order for these systems to meet applicable standards, which represents a big portion of the total size and cost of PWM inverters. EMI models are necessary for an optimized EMI filter design. The conducted EMI noise is separated by common-mode (CM) and differential-mode (DM) according to the conventional theory, each mode of the noise is dealt with the respective section of an EMI filter. However, in real applications, there is an additional noise-coupling mode, called the mixed mode (MM), that has a significant impact on the filter design effectiveness and needs to be dealt with.

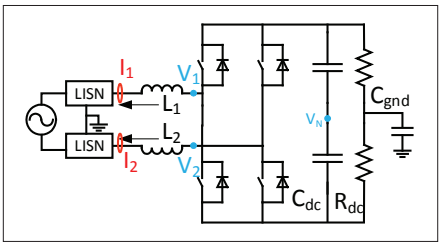

Fig 1. Single-phase PFC with H-bridge converter.

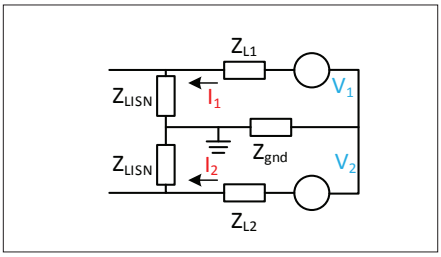

Fig. 2. EMI model in frequency domain.

Based on the time domain voltage, current relationship and the definition of DM and CM noise source and noise current, a noise prediction model is proposed in frequency domain with the consideration of system symmetry regarding the noise propagation path impedance. The model indicates that the mixed mode noise is the coupling between the CM/DM noise source and the DM/CM noise current due to circuit asymmetry. With the noise source calculated and circuit impedance measured or modeled in frequency domain, the mixed mode noise can be predicted based on the proposed model.

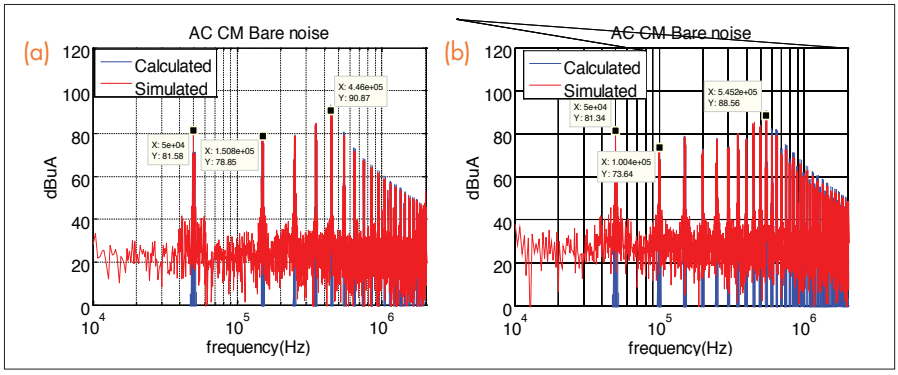

Fig. 3. EMI noise comparison (predicted: blue; simulated: red). (a) CM noise with symmetric load. (b) CM noise with asymmetric load.

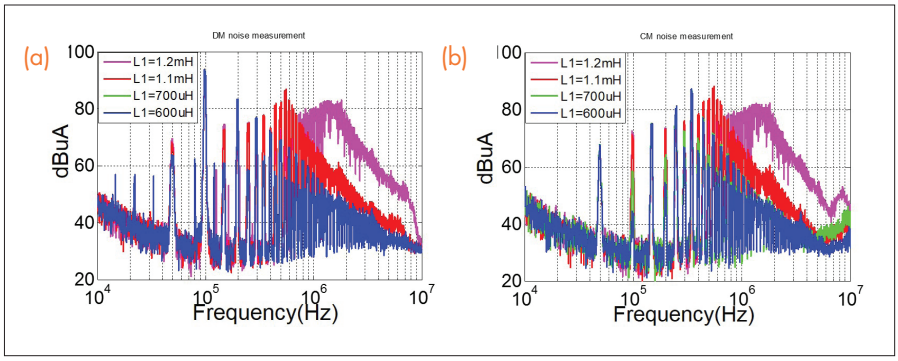

Fig. 4. Measured EMI noise with different circuit asymmetry. (a) CM noise with asymmetric load. (b) DM noise with asymmetric load

Temperature Cycling Reliability Assessment of Die-Attachment on Bare Copper by Pressureless Nanosilver Sintering

Power electronics engineers use semiconductor switching devices to shape the forms of electrical energy to enable efficient and reliable operation of electrical and electronic devices. Performance of power electronics devices has improved significantly with the development of wide-bandgap semiconductors, such as silicon carbide (SiC) and gallium nitride (GaN). Compared to silicon-based devices, wide-bandgap devices are capable of fast turn-on and turn-off, have lower conduction and switching losses, and can be operated at high temperatures (e.g., 250°C). At the first level of packaging, die-attach material and processing are crucial for the overall performance and reliability of the final product, and therefore innovations in die-attach technologies are urgently needed.

Nanosilver paste, an emerging die-attach material, was formulated by mixing nanosilver particles with several types of organic additives. Extensive research has been done on the application of nanosilver paste for die-attachment. It has been demonstrated that nanosilver paste can be applied for attaching power devices of different sizes onto silver and gold surfaces by pressureless or low-pressure-assisted (<5 MPa) sintering, with sintering temperature lower than 280°C.

The goal of this study was to evaluate the temperature cycling reliability of the pressureless, forming-gas-enhanced sintering process for bonding chips on copper using nanosilver paste. Thick silicon chips were attached to the DBC with a bare copper surface for die shear testing, while thin silicon chips were attached to copper lead frames for microstructure analysis. Samples were subjected to temperature cycles in the range of -40°C to 125°C with a cycling period of 60 minutes. Die shear tests were performed on cycled samples. X-ray tomography was applied to detect the defects in the die-attach joints for the silicon samples. Microstructures of cross sections of the joints were characterized by SEM.

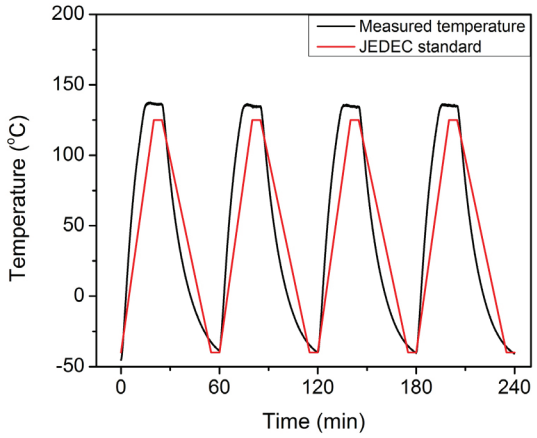

Fig. 1. Measured temperature cycling profile in comparison with JEDEC standard.

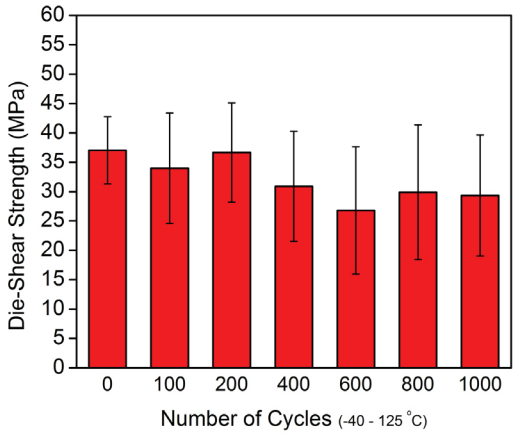

Fig. 2. Die-shear strength of joints versus number of temperature cycles.

Efficiency Optimized AC Charging Waveform for the GaN Bidirectional PHEV Battery Charger

Automobile manufacturers are invested in significantly reducing the weight and volume of the on-board charger for Lithium-Ion batteries in Plug-in Hybrid Electric Vehicles (PHEVs). Sinusoidal charging, which allows current ripple at double line frequency to the battery, can boost the power density of the battery charger by significantly reducing the dc link capacitance. However, the charger's efficiency drops due to the loss of zero-voltage-switching for the switches in the dc-dc stage at the lower part of the charging current waveform. In this paper, different ac charging waveforms are investigated in order to achieve a better balance between charger efficiency and dc link capacitance.

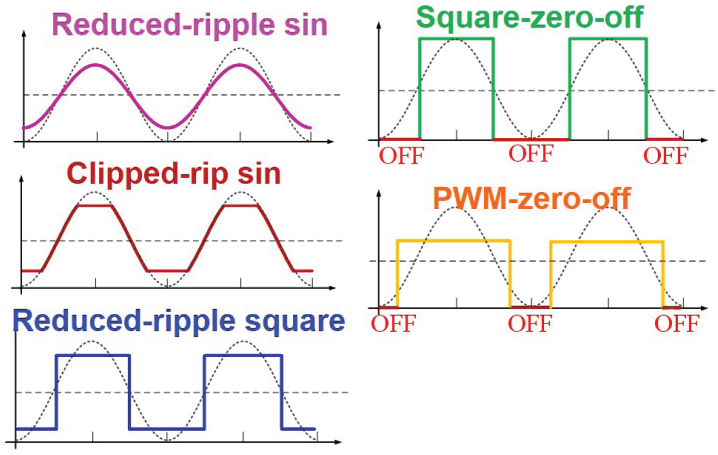

Fig. 1. Evaluated AC charging waveforms.

The waveforms under investigation are shown in Fig. 1. While all the waveforms should deliver the same average value, as determined by the charging profile, they can be divided into two categories. The left three waveforms have adjustable ripple amplitude, while the right two waveforms have fixed ripple amplitude. Since the charging current of the right two waveforms always touches zero, the dc-dc stage is turned off at the zero part of the output current, where, essentially, no power is delivered. For all of the five charging waveforms, we need to evaluate the converter efficiency and dc link capacitance requirements. Or, equivalently but more conveniently, we can evaluate the converter loss and dc link voltage ripple. The best charging waveform should give both minimum converter loss and minimum dc link voltage ripple.

The evaluation results are shown in Fig. 2. From the top figure, we can see that PWM-zero-off charging gives the minimum amount of loss and dc link voltage ripple compared with all of the other waveforms. The bottom chart shows the measurement waveform of a GaN-based battery charger. With PWM-zero-off charging, the charger saves 39% of converter loss with the same dc link voltage ripple, as compared to the second best charging waveform – reduced-ripple sinusoidal charging.

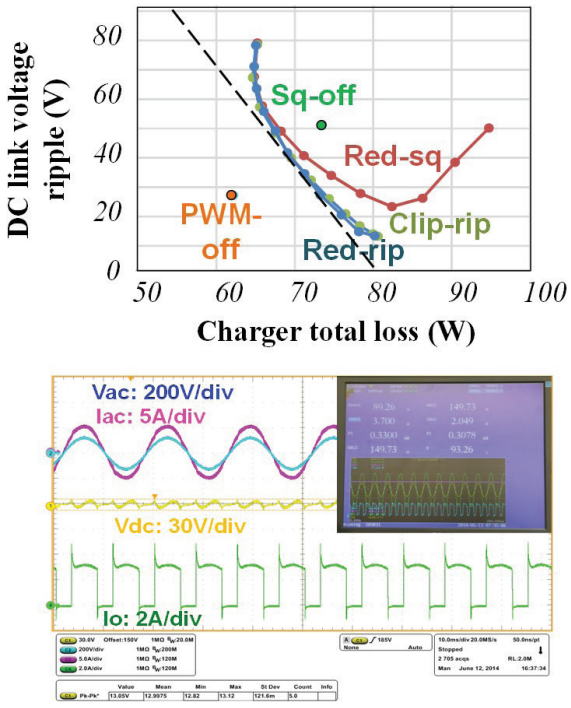

Fig. 2. Experimental results. Top: dc link voltage ripple and con-verter loss. Bottom: measured waveform of PWM-zero-off charging.

GaN-based High-Frequency Totem-Pole Bridgeless PFC Design with Digital Implementation

The totem-pole Bridgeless Power Factor Correction (PFC) converter is a promising topology for GaN transistors because of its very low reverse recovery charge compared to the body diodes of silicon MOSFETs. However, this topology has some inherent challenges to be overcome before it can be used for high-frequency PFC converters.

Fig. 1 shows the schematics of this topology. In this investigation, all four switches in the H-bridge are active switches. The low-frequency (LF) phase leg only commutates at line frequency, while the high-frequency (HF) phase leg will chop the dc voltage at high frequency. In this case, the low frequency phase leg can use very large Si MOSFETs, and thus the on-resistance can be reduced. The HF phase leg is built with GaN devices.

The first issue when using this topology is addressing the significantly different switching speeds of the HF leg and LF leg switches. From the bottom-left chart in Fig. 1, we can see that when the voltage transition of the LF leg has a certain delay, the dc link voltage will directly apply across the ac inductors, causing a current spike. This delay is equal to the dead time of the LF leg. The second issue of this topology deals with the minimum pulse width of the HF leg. At zero-crossing, the duty cycle of the HF leg needs to change abruptly from 100% to 0%. However, the phase leg cannot output such narrow or wide pulses, so those extreme pulses are eventually blanked as high or low levels. Thus, ac voltage is applied across the ac inductor for multiple switching cycles, leading to current spike.

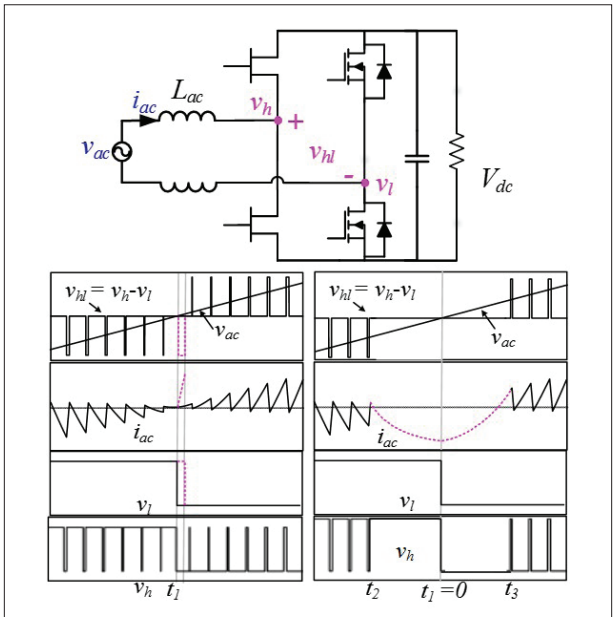

Fig. 1. Schematics and totem-pole bridgeless PFC and two issues causing current spike at zero-crossing.

By carefully designing the digital modulator, the two aforementioned issues can be resolved. A lead time of dead-time length is programmed in the ePWM module so that the delay of the LF leg is compensated for. The second issue is resolved by digital dithering. The PWM pulses are delivered in a batch of ten. If some of the pulses are skipped in one batch, then the equivalent pulse width of the batch is increased by ten.

Without improvement of the digital modulator, a current spike can be observed at the zero crossing of the ac voltage, as shown in the upper portion of Fig. 2. After implementing both LF leg compensation and HF leg dithering, the current spike is eliminated (Fig. 2 bottom). This work provided solutions to the inherent issue of current spike of the totem-pole bridgeless PFC converter. These solutions could prove even more important when ac inductance is reduced further due to higher switching frequency.

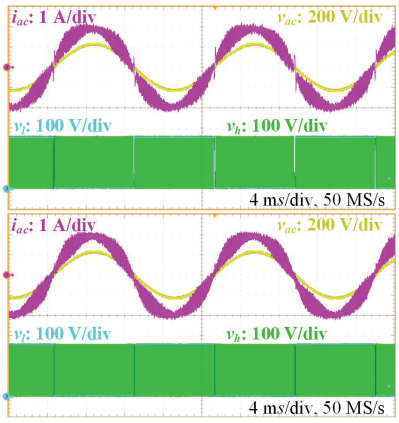

Fig. 2. Experimental results.

Characterization of 650-V Enhancement-Mode GaN HEMT

Gallium Nitride (GaN) power transistors are divided into three categories: depletion mode, enhancement mode, and cascode configuration. The depletion-mode (normally-on) power MOSFETS are not preferred for a switching operation, hence the cascode configuration is packaged by GaN on Silicon technology. A low-blocking-voltage Si transistor is cascaded with the high-blocking voltage depletion-mode GaN transistor to make the configuration a normally-off one. The Transphorm 600V, 17A GaN transistor is based on the cascode configuration. Another high-blocking voltage GaN High Electron Mobility Transistor (HEMT) is manufactured by EPC with a rated blocking voltage of 200V. Recently, the GaN systems enhancement mode GaN transistor became commercially available. Rated at 650V, 30A it looks very promising since it has a considerably lower on-resistance, especially when compared to a Transphorm GaN transistor with similar ratings, which is a normally-off device.

The static characterization results show that the device has an on-resistance of 55 mΩ at 9 A drain current and 7V gate-to-source voltage. The transistor package also has a separate source-sense pad to keep the gate-to-source loop independent of the drain-source loop, as shown in Fig. 1. The blocking capability of the device is also tested, and the blocking voltage is found to be 650V with a leakage current of 2.4 μA at 25ºC. The reverse characteristics (as shown in Fig. 2) are similar to that of a MOSFET with a body diode, but the GaN HEMT has no intrinsic body diode; the junction conducts during the off-state. The on-state reverse characteristics are similar to the on-state forward characteristics.

Fig. 1. GaN Systems GaN transistor (left: Transistor package; right: Device Schematic).

From these measurements, the on-resistance at 9A drain current and 7V gate to-source voltage during reverse conduction is found to be 54.5 mΩ. The on-resistance during forward and reverse conduction at 100ºC is found to be 136 mΩ with similar operating conductions. The transconductance is found to be 15 S at 25ºC and 7.95 S at 100ºC. In conclusion, by reviewing the output characteristics, the recommended on state gate to source voltage should be between 6-10V.

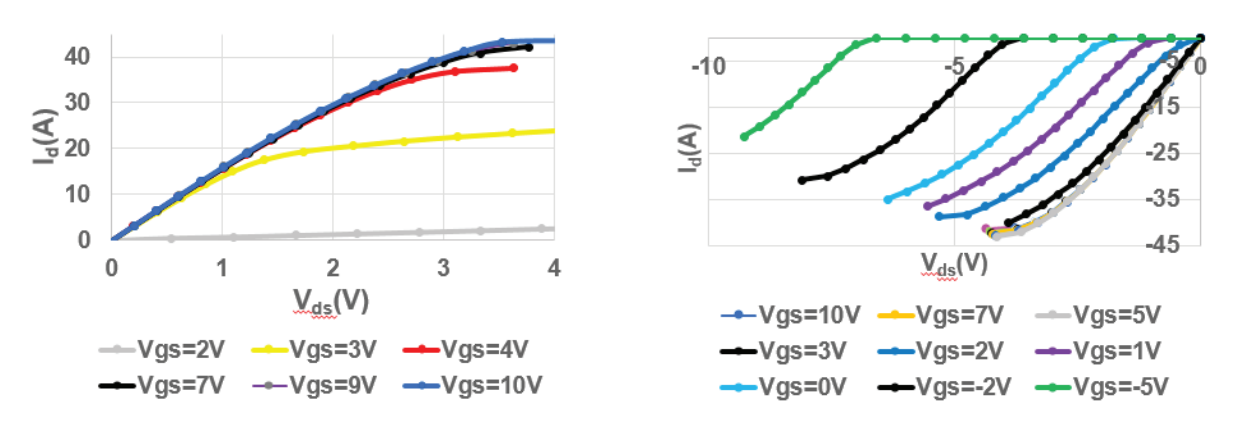

Fig. 2. I-V Transfer curves (left: Forward characteristics; right: Reverse characteristics).

An Ultra-Fast SiC Phase-Leg Module in Modified Hybrid Packaging Structure

This paper presents the development of an ultra-fast SiC phase-leg module built in modified hybrid structure. Because of the three-dimensional (3D) packaging technology, the hybrid structure achieves the same footprint and similar parasitics to the planar packaging, but requires no double-sided solderability on the bare dice, which is not available on current SiC devices. Compared to its previous generation, the modified hybrid structure also simplifies the fabrication significantly, and allows a much more complicated module design. A compact 1200V, 10A SiC MOSFET phase-leg module is designed and built in the proposed structure. Through proper layout design, ultra-low switching loop inductances can be realized, and experiments verify that the switching speed of the SiC MOSFET can be pushed to its very limit without excessive parasitic ringing.

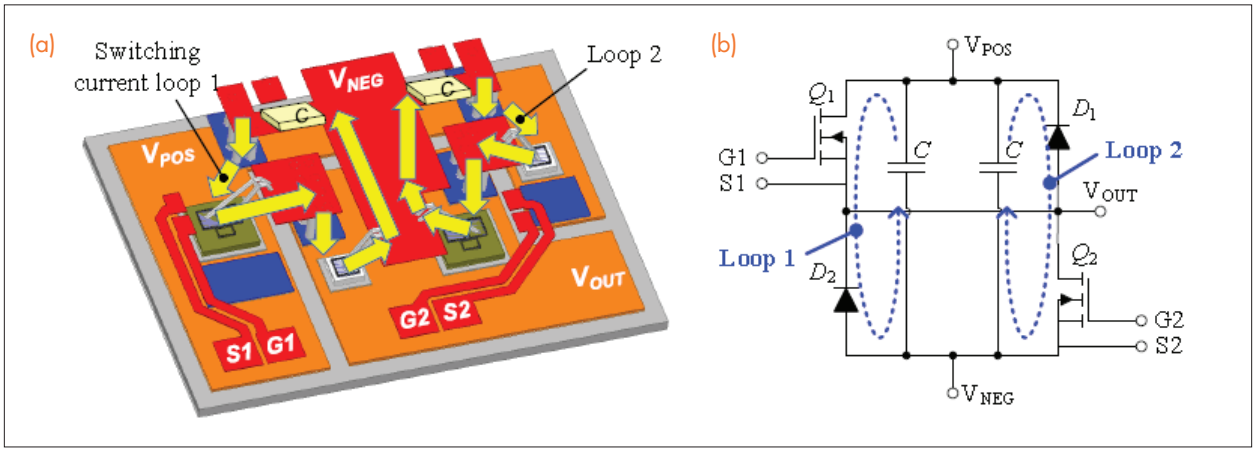

Fig. 1. (a) Internal structure and (b) equivalent circuit of the hybrid SiC MOSFET phase-leg module with switching loops identified.

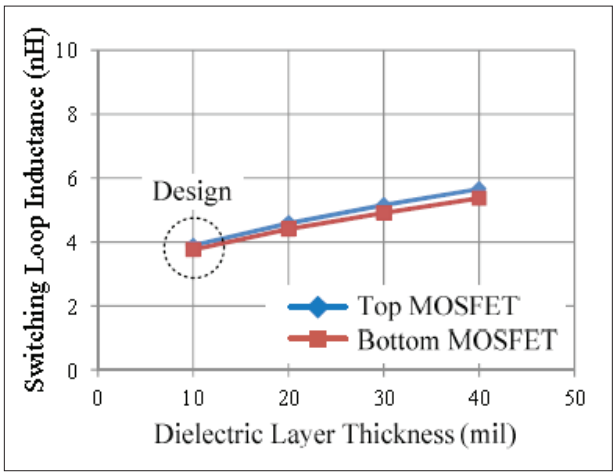

Fig. 2. Simulated switching loop inductances vs. PCB dielectric layer thickness.

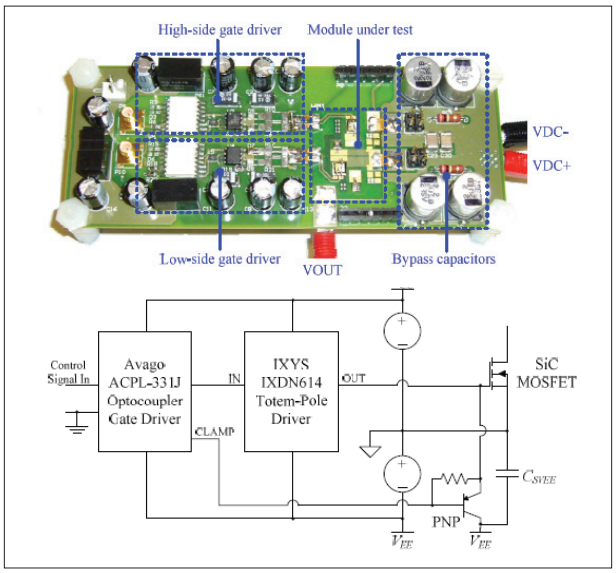

Fig. 3. Hybrid module tester. (a) Gate drive circuit and (b) tester board.

Integrated Design by Optimization of Electrical Power Systems for More Electric Aircraft

As aircraft-installed electrical power continues to increase, maintaining the advantages of the MEA approach highly relies on the ability to design low-weight on-board electrical network and power electronic conversion systems. However, design and integration of the power system still follows the legacy standards, where locally optimized individual components may not result in optimum system. This paper presents an attempt at exploring the advantages and barriers to integrated design where subsystem interactions are accounted for and the power system is optimized as a whole. As an example, the weight of a notional subsystem of the MEA electrical power system—consisting of a dc bus, a rectifier, an ECS, and an EMA—is studied and optimized as a function of the dc bus voltage, while taking into account the power quality, EMI, and stability constraints. Although the example follows a traditional (decoupled) design approach, the individual component modeling and design processes are formalized with similar structures, so that future system-level integrated design by optimization can be evaluated.

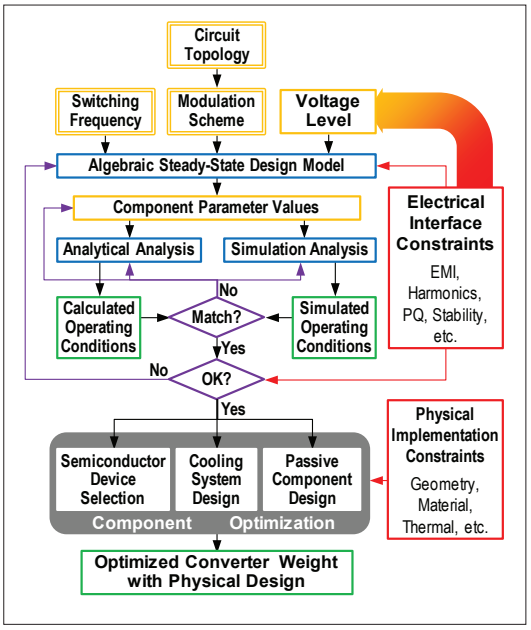

Fig. 3. Converter design and optimization process.

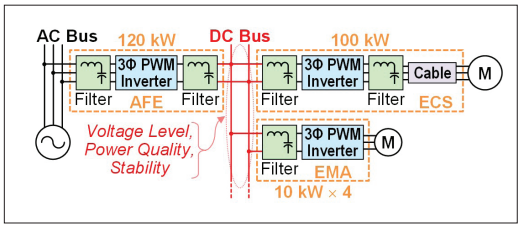

Fig. 1. Notional MEA subsystem structure

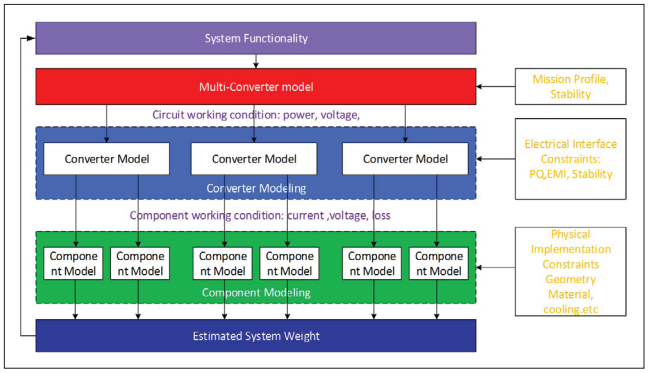

Fig. 2. Simplification levels for whole system optimization.

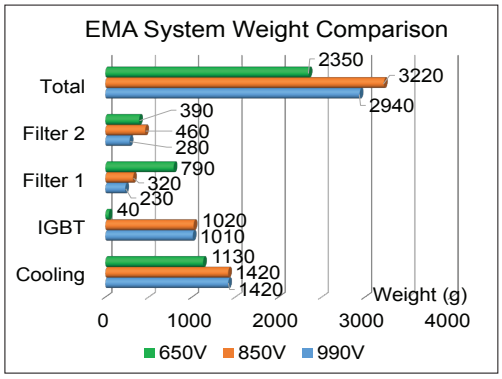

Fig. 4. EMA converter weight breakdown

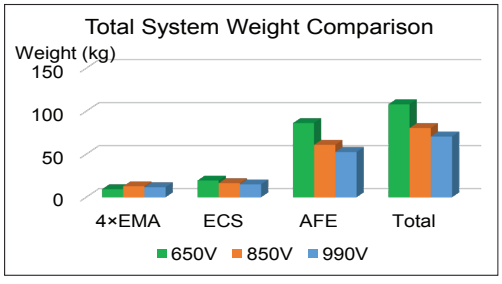

Fig. 5. Total system weight comparison

Renewable Energy & Nanogrids Nuggets

Magnetic Design and Loss Analysis for High-Frequency High-Power DC/DC Transformer

Investigation and Design of Modular Multilevel Converter in AFE Mode with Minimized Passive Elements

New Modulation Scheme for Three-level Active Neutral Point Clamped Converter with Loss and Stress Reduction

Analysis and Design of Coupled Inductor for Interleaved Multiphase Three-level DC-DC Converters

Modeling and Design of Islanding Detection Using Phase-Locked Loops in Three-Phase Grid-Interface Power Converters

Steady-State Analysis of Voltages and Currents in Modular Multilevel Converter Based on Average Model

Analysis and Design of Virtual-Synchronous-Machine-Based STATCOM Controller

Droop Voltage Range Design in DC Micro-Grids Considering Cable Resistance

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Modularized High Frequency High power 3-level Neutral Point Clamped PEBB cell for Renewable Energy System

Modeling the Output Impedance of Three-Phase Uninterruptible Power Supply in D-Q Frame

REN Research Team (April 2014 – April 2015):

Faculty:

Dushan Boroyevich

Rolando Burgos

Fred C. Lee

Research Faculty:

Igor Cvetkovic

Zhiyu Shen

Graduate Students:

Fang Chen

Pin-Yu Huang

Marko Jaksic

Yang Jiao

Chi Li

Alinaghi Marzoughi

Subhajyoti Mukherjee

Ruiyang Qin

Niloofar Rashidi

Jun Wang

Bo Wen

Wei Zhang

Shishuo Zhao

Visiting Scholars:

Kai Li

Sharmila Sumsurooah

Juan Carlos Vasquez Quintero

Rongfeng Yang

Magnetic Design and Loss Analysis for High-Frequency High-Power DC/DC Transformer

The Solid State Transformer (SST), which is a converter with an isolation transformer running at much higher working frequency, has gained increasing importance to substitute traditional line frequency transformer in terms of high power density and compatibility. The medium voltage ditribution application of high frequency isolation transformer are reviewed in this paper. Based on the wide-bandgap material silicon carbide (SiC) power MOSFET, CLCC resonant converter can operate at tens or even hundreds of kilo hertz. An accurate core loss model and litz wire winding loss model are necessary to investigate high frequency transformer design for this resonant converter. A simple core loss and winding loss model are employed with acceptable accuracy under certain assumptions. Detailed analysis and optimal design of transformer are achieved with supporting rationale from these models.

Nanocrystalline is the best candidate for the SST design in terms of core loss and saturation flux density for frequency around 50kHz. A transformer's core loss is determined by a working flux waveform, which is excited by input voltage. Our proposed CLLC resonant converter is a frequency controlled converter with a square input voltage waveform. A Rectangular Extension Steinmetz Equation (RESE) is employed to exactly predict core loss under rectangular voltage excitation. Calculation results are verified by actually measuring core loss density at different working temperatures, frequencies, and different flux density amplitude.

A litz wire is used in the SST transformer since it contains separately insulated wire strands twisted or braided together, enabling low-resistance high-current conductors at frequencies up to hundreds of kHz. Based on valid assumptions, the litz wire winding loss model should only consider both eddy current flowing inside each strand due to an external field and a conduction loss neglecting the eddy current effect. The former can be analytically calculated basing on the field distribution characteristic shown in Fig. 1. The latter is easy to calculated via a dc resistance of conductor. This winding loss model is also verified by a sample transformer with a similar structure.

To simplify analysis, the first step determines the strand diameter as an AWG 38 strand. Wide range turn number N and strand number Ns are swept to calculate the transformers total loss and total volume. For each specific volume among different combination of N and Ns, a minimum loss point (red point) can always be found. The connection line of these points should contribute to the optimal design curve for different volume values. Design trade-offs between total loss and volume is explained basing on loss calculation and volume evaluation. The strand diameter and core loss density impact on transformer design are all investigated. Finally, a completed SST design result is proposed with the necessary design parameters.

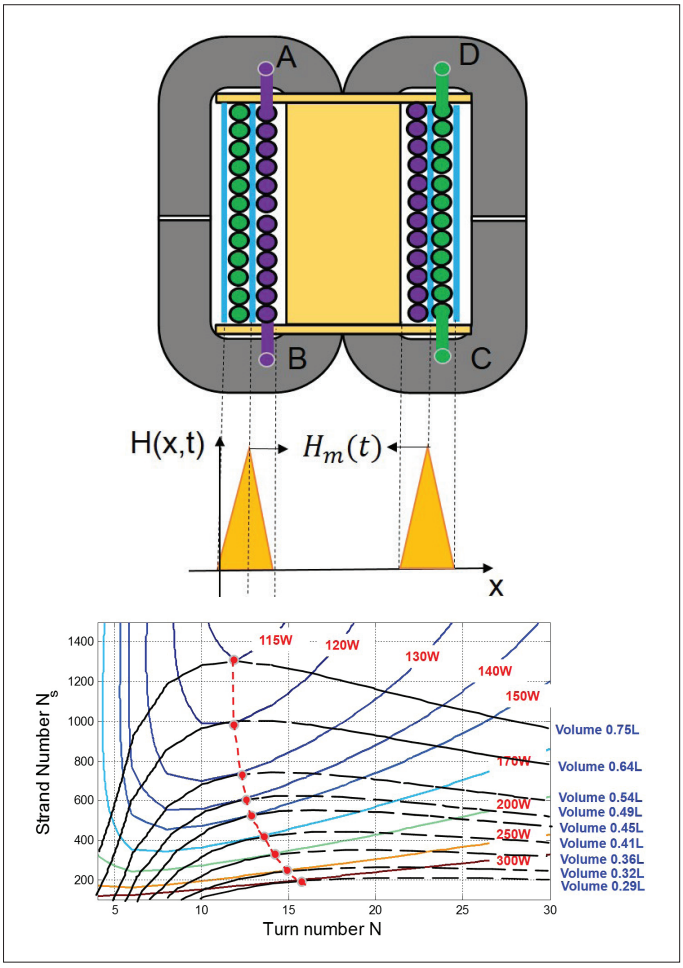


Fig. 1. Transformer preliminary design (top) and field distribution characteristics (bottom).

Investigation and Design of a Modular Multilevel Converter in AFE Mode with Minimized Passive Elements

This paper investigates the design procedure of a modular multilevel converter (MMC) in an active front-end (AFE) mode of operation. The design aims to minimize the number of passive elements, including arm inductances and submodule capacitances. This has been accomplished using the basic controllers needed for the operation of the MMC in AFE mode, without employing any additional controllers in the circuit. In other words, the design takes advantage of properly locating arm inductance and submodule capacitance magnitudes with respect to the intrinsic resonance phenomenon in the MMC converter. A model is developed in the MATLAB/Simulink environment in order to show the feasibility of the proposed design and also to provide a comparison between the proposed MMC AFEs and the formal designs. The comparison in the shown case study reveals a 90% reduction in arm inductance magnitude and a 40% reduction in submodule capacitance values, at the expense of adding filter inductances with a much smaller size.

Proper sizing of the arm inductances is crucial for the MMC AFE. At higher powers and currents, the main issue with the MMC AFE is the design of large arm inductances capable of restricting the input current in case of a fault on the MMC's DC bus. In high-current MMC AFEs, where it becomes non-beneficial to design huge inductances, using an H-bridge-based MMC is proposed as a solution, as it has an intrinsic capability to suppress fault currents.

In this paper, an AFE MMC is designed with special focus on minimizing the passive elements' size, while keeping the same power quality and fault protection level. No additional controller is added in order to reduce the size of the passive elements. The proposed design can extend the operation range of the half-bridge-based MMC AFE by decreasing the amount of inductances needed. The performed reduction of passive elements (i.e., arm inductances and submodule capacitances) will result in reduced initial investment costs, and of active power loss in the passive elements.

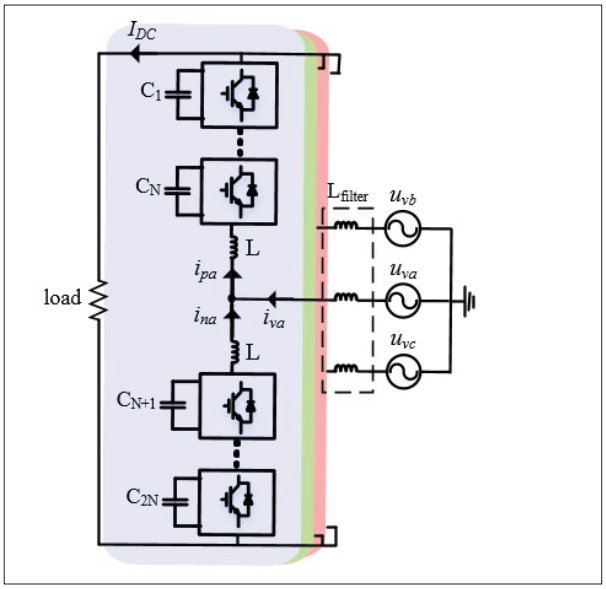


Fig. 1. (a) MMC AFE with grid connection and (b) half-bridge submodule as building-block of MMC AFE.

New Modulation Scheme for Three-Level Active Neutral Point Clamped Converter with Loss and Stress Reduction

In this paper, the modulation schemes for a three-level neutral point clamped (NPC) phase leg is thoroughly investigated using phase leg loss and stress distribution analysis. Since the conventional modulation schemes have some issues when using a SVM modulation strategy with a NP voltage balance, an improved modulation scheme for a three-level ANPC phase leg is proposed. Taking advantage of the flexibility of the neutral current path configuration for the ANPC phase leg, this modulation scheme uses both neutral current paths to conduct neutral current. Thus, the conduction loss is significantly reduced. Compared with the conventional modulation schemes for ANPC, which have a different neutral state for the positive and negative half line cycle, the proposed modulation scheme has a unified neutral state for both the positive and negative half-line cycle. With the new modulation scheme, new switching loops for the three-level ANPC phase leg are generated in the four-quadrant operation. The new switching loops have two pairs of complimentary switches and two pairs of synchronized switches. The two inner switches share the high frequency loss and stress for the two clamping switches instead of doing line frequency switching with the conventional method. In the new switching loops, two paralleled switching devices commutate simultaneously with another switching device. So the load current is shared by the two switches, and the switching stress is reduced. The double pulse test measures the switching characteristics for the new loops. It shows a largely reduced switching stress, and basically an unchanged switching loss for the new loop. The phase leg loss distribution shows the more evenly distributed phase leg loss and stress. Also, the system loss breakdown shows a 15% conduction loss reduction. With this modulation scheme, the 200kVA three-level ANPC power converter operating at 20kHz can reach up to 98.5% efficiency. Another benefit for the proposed method is that only two pairs of PWM channels are needed for each phase leg with the proposed method. So the three-phase system can save six PWM channels. The proposed method is also verified on a 200kVA, 20kHz three-level ANPC converter hardware.

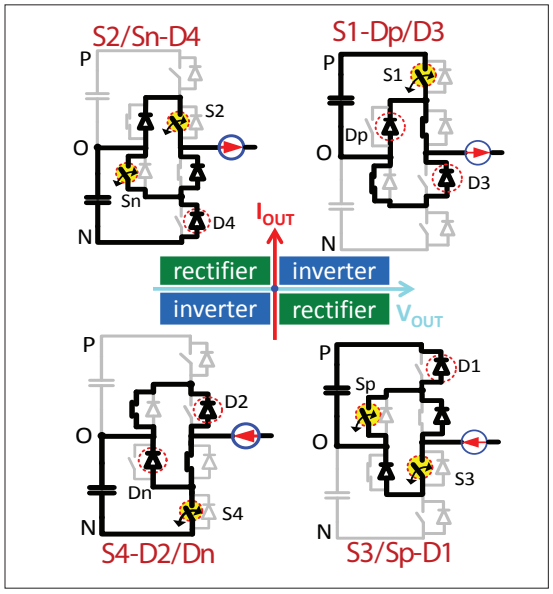


Fig. 1. Four-quandrant operation and switching loops for the new modulation for ANPC phase leg

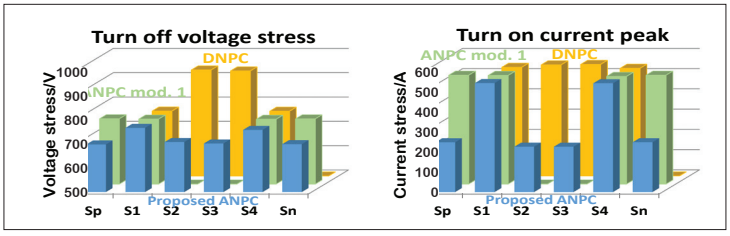


Fig. 2. Inverter side current ripple waveform.

Analysis and Design of Coupled Inductor for Interleaved Multiphase Three-Level DC-DC Converters

The coupled inductor can reduce large inductor current ripple in the interleaved multiphase three-level converter, while retaining the benefits of interleaving. The design of the coupled inductor is different from conventional two-level converters. This paper analyzes the flux in the coupled inductors of interleaved multiphase three-level dc-dc converters. Based on flux analysis, a design procedure is introduced. A new structure for the coupled inductor is also proposed, in which two types of coupling are utilized, and only one integrated component is needed for the multiphase interleaved three-level converter. To utilize the tape-wound core (an amorphous, nanocrystalline material), a new structure is introduced, which simplifies the structure and reduces cost. A prototype using a nanocrystalline core that could reduce the inductor volume by over 40% was built and experimentally verified.

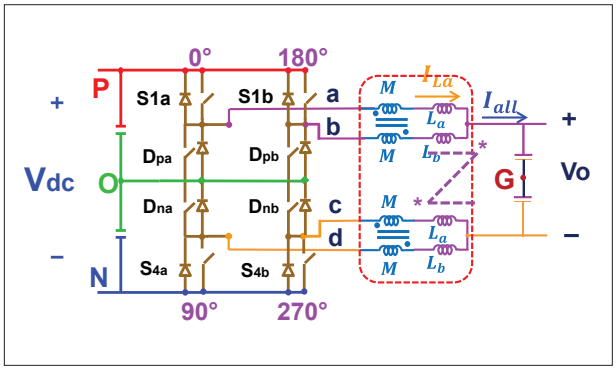


Fig. 1. Three-level dc-dc converter with integrated coupled inductor.

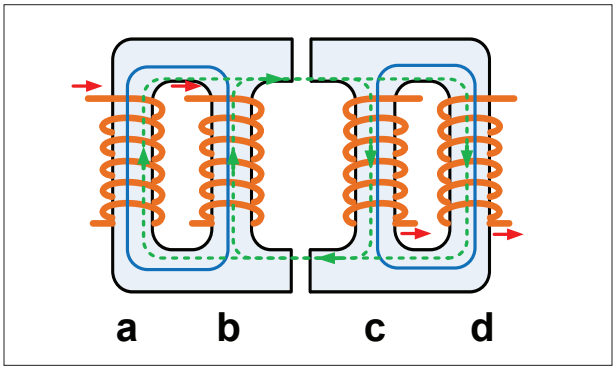


Fig. 2. Integrated core structure (principle drawing)

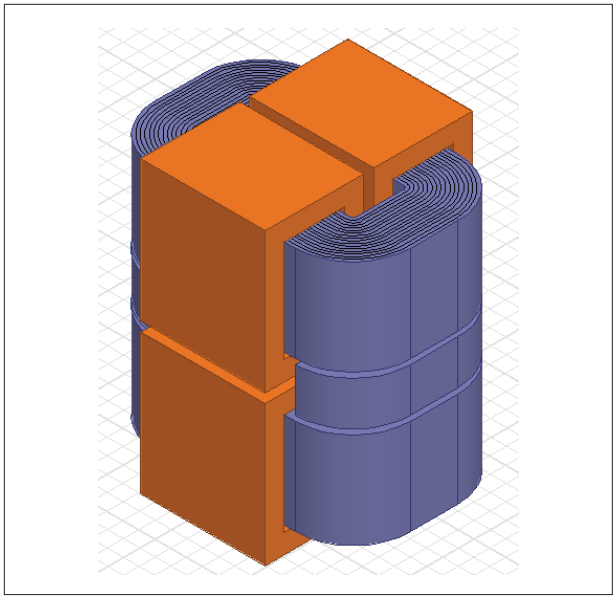


Fig. 3. Integrated coupled inductor design

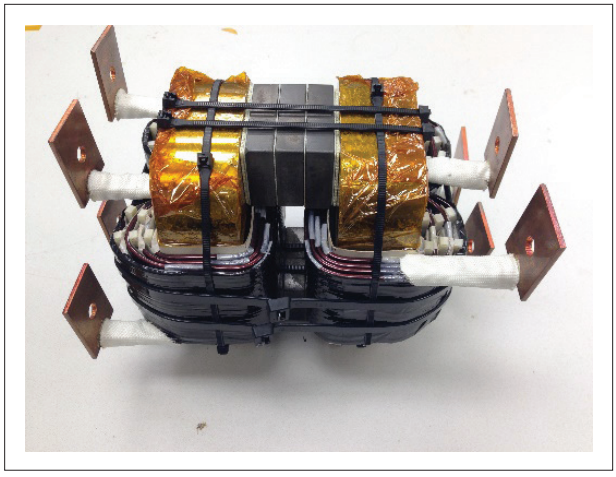


Fig. 4. Coupled inductor built with nanocrystalline tape-wound core

Modeling and Design of Islanding Detection Using Phase-Locked Loops in Three-Phase Grid-Interface Power Converters

Islanding detection is critical to safety and power quality as well as the control mode of grid-interface power converters. This paper addresses islanding-detection methods on the basis of the grid synchronization instability mechanism. Although many modified phase-locked loop (PLL) methods have been proposed to achieve islanding detection, the PLL modeling and design are not clear in existing literature and a cut-and-trial process is usually required during the design phase. This paper proposes a systematic PLL modeling and design approach to evaluate different frequency-based islanding detection methods. Two different types of PLL-based islanding detection solutions are discussed, accounting for a majority of the existing methods. The first method is to modify the PLL to constantly move the stable-equilibrium point. The second method is to modify the PLL small-signal characteristics to achieve a monotonic instability behavior under the islanded conditions. The design procedures of these methods are presented using the pro-posed PLL modeling approach. The impact of the modified PLLs on the converter's operation is also analyzed.

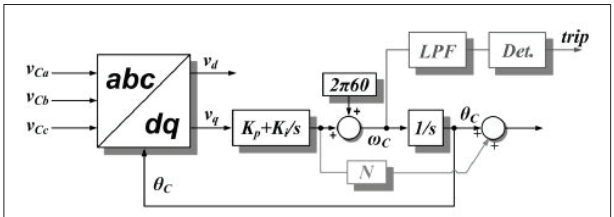


Fig. 1. Modified PLL with small-signal feedforward for islanding detection.

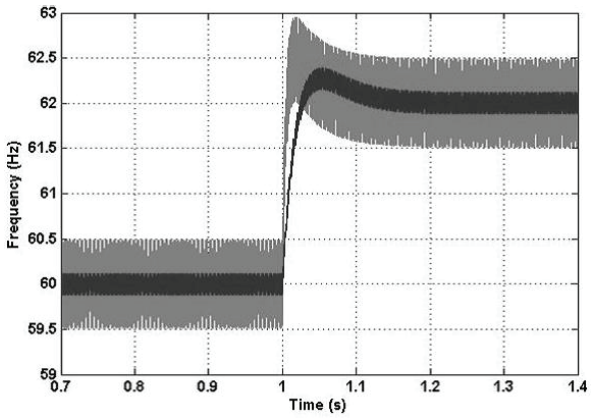


Fig. 2. Modified PLL 2 Hz input step response with 1% 600 Hz grid harmonics.

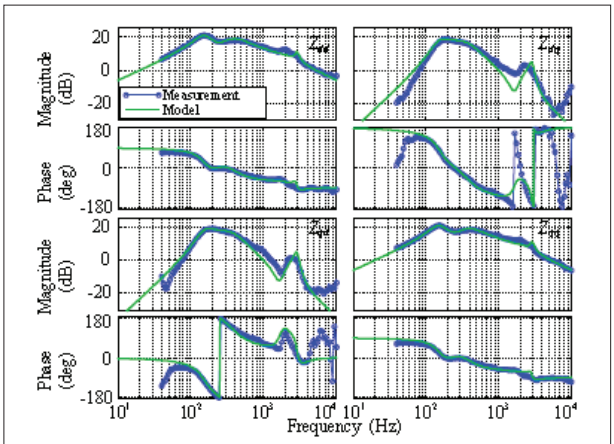


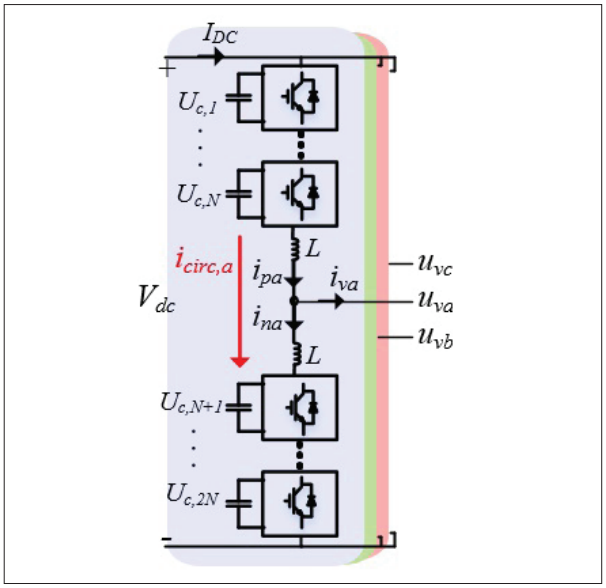
Fig. 3. Measurement results compared with model for voltage control.

Steady-State Analysis of Voltages and Currents in the Modular Multilevel Converter Based on an Average Model

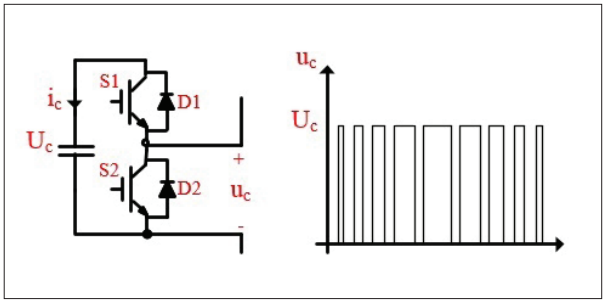
The modular multilevel converter (MMC) is being considered as the next generation converter among multilevel topologies, and with the introduction of MMC, a new era has opened in the field of medium-, and high-voltage, high-power converters. Sizing the passive elements and design of the converter along with its performance evaluation is thus of great importance for researchers in this area. This paper provides a steady-state analysis of the MMC based on an average model. The magnitudes and phase angles of current and voltage quantities are calculated herein. Further, equations are solved for different components of the circulating current and submodule voltage, and the resonance behavior in circulating current harmonics is investigated. Based on the resonance behavior of circulating current harmonics, a guideline is given for choosing the magnitude of submodule capacitance and arm inductance. A model is developed in the MATLAB/Simulink environment in order to verify the performed calculations' accuracy.

The wide variety of applications, along with the need for a significant amount of passive elements installed, requires the best possible MMC converter design. In order to understand the operation of the MMC and then design the converter for the target application, an accurate analysis of the voltage and current waveforms in the MMC are of great importance.

In this paper, a detailed analysis of submodule voltages and arm currents is done based on an average model. The analysis takes into consideration the arm current components up to the fourth, and submodule voltage ripple components up to the fifth, harmonic. Also, the resonant behavior of the second and fourth order harmonics in the circulating current is investigated and the relationship between resonance frequency and the magnitude of passive elements is derived. Then, a guideline to select the size of arm inductance and submodule capacitance is discussed. Finally, validity of the derived equations is shown via simulations in MATLAB/Simulink.



(a)



(b)

Fig. 1. (a) Three-phase MMC inverter and (b) Half-bridge submodule as building-block of MMC AFE.

Analysis and Design of a Virtual Synchronous Machine Based-STATCOM Controller

This paper extends the virtual synchronous machine (VSM) concept, recently proposed as an alternative means to synchronize grid-connected inverters, by developing a VSM-based STATCOM controller operating as synchronous condenser. In this article, the test bed studied is as shown in Fig. 1, where the wind farm is providing power to an infinite bus bar with a shunt-connected STATCOM, tracking and regulating the PCC voltage, v_{PCC}. To this end, a mathematical model is derived and used to analyze the inherent dynamics of the VSM-based STATCOM controller. The dynamics are then used to formulate design guidelines that further detach the proposed method from the perceived physical constraints introduced by the VSM concept. To gain a better understanding, we can transform the testbed and the proposed controller in the abc frame into the dq frame, as shown in Fig 2. It should be noted that there are two dq frames: the system dq frame with superscript ^{s} rotating at the nominal frequency ω_n, and the controller dq frame with superscript ^{c} at frequency ω, and the angular difference δ, which is necessary for the coordinate transformation T_θ between both dq frames. Based on the model in the dq frame, the effects of each parameter are studied by investigating the Bode plots of the control loops, raising some discussion about trade-offs in parameter selections.

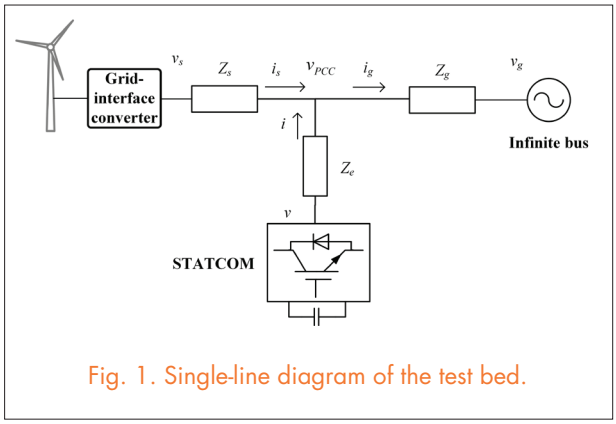
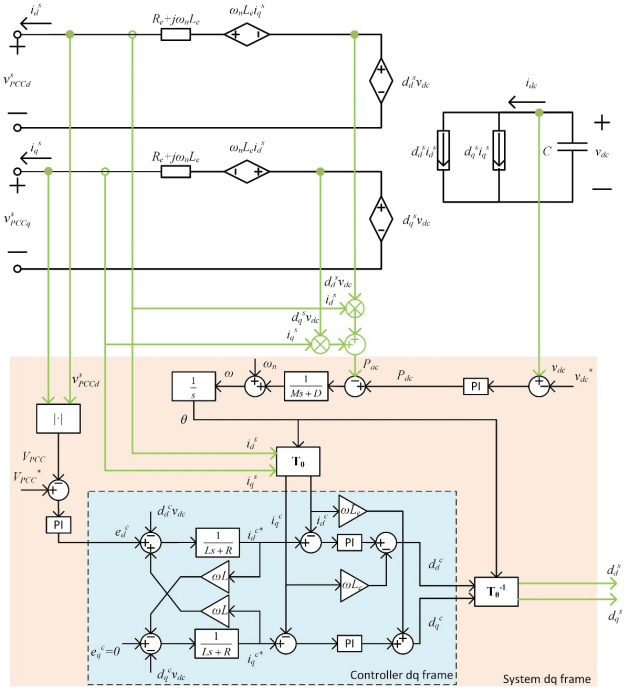


Fig. 1. Single-line diagram of the test bed.



$$\mathbf{T}_\theta = \begin{bmatrix} \cos\delta & \sin\delta \\ -\sin\delta & \cos\delta \end{bmatrix}$$

Fig. 2. Power stage with VSM controller in dq frame.

Droop Voltage Range Design in DC Microgrids, Considering Cable Resistance

The dc microgrid has gained more and more attention recently due to the ease of integrating different renewable sources (solar cells, energy storage, wind turbines etc.), the absence of frequency issues, and the possibility of achieving higher efficiency. To coordinate multiple sources in a dc grid that are paralleled to a common bus, droop control is broadly accepted, as shown in Fig. 1. By introducing a virtual output impedance to each source, the circulating current can be suppressed and load sharing among sources is realized.

Though the droop principle is discussed in many papers, the practical design of droop in a dc system is seldom discussed. In real cases, cable resistance and voltage regulation errors will impact the load sharing performance with droop control. In addition, the voltage distribution within the dc system will be different from that in the ideal case.

In this paper, the impact of cable resistance and voltage regulation error on droop control was investigated. Cable resistance changes the load-sharing ratio among sources, while the voltage regulation error introduces a constant current error. To suppress the impact from cable resistance, larger droop resistance is preferred, but voltage regulation is sacrificed as a result. The cable size and possible voltage range for droop in a dc system are analyzed, and the quantitative relation between droop voltage range and unbalanced current was derived for two-source systems as shown in Fig. 2.

The worst-case scenarios for three-source and multi-source multi-load systems were identified. Though proper distribution of sources and loads helps relieve the load sharing unbalance, the worst-case scenario remains the same as was discussed for the two-source one-load system. Therefore, the conclusion for the two-source system can be used to estimate the worst-case scenario for the multi-source system. The dc system designer can use the quantitative results from this paper to choose proper droop voltage range and guarantee the sharing unbalance within the required range. If necessary, detailed load-sharing results for a particular configuration can be calculated using a numerical method.

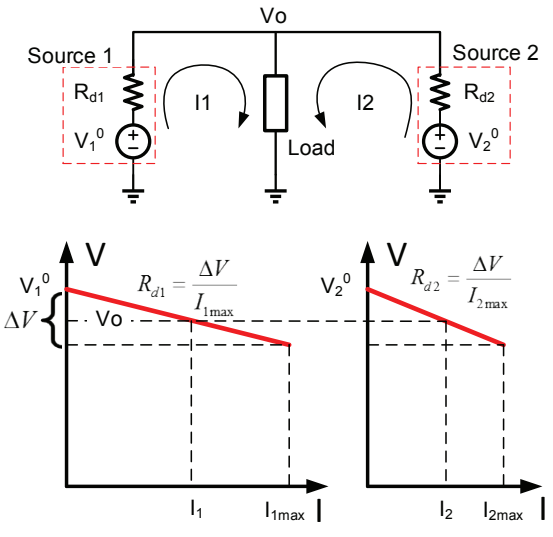


Fig. 1. Droop control in a 2-source 1-load dc system.

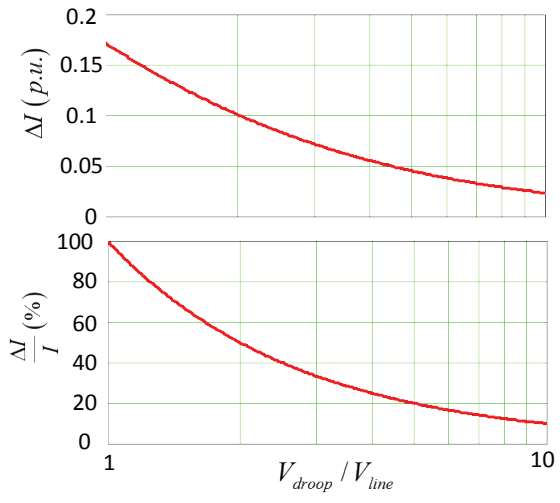


Fig. 2. Sharing error as a function of droop voltage range.

Modeling of a Virtual Synchronous Machine-Based Grid-Interface Converter for Renewable Energy Systems Integration

To date, the common, and with some exceptions the only, method to interconnect high-power renewable energy sources and energy storage systems to the grid has been the use of power electronics converters that operate as current sources to the grid for the purpose of achieving maximum primary-source power tracking. When the grid is not available, such sources would not be allowed to continue operating and would be shut down after anti-islanded algorithms recognized the loss of the grid. Although existing standards and requirements still limit grid-interface converters to regulating voltage in the grid, the functionality discussed in this paper will inevitably be part of the power system's operation in the future. This paper addresses physical and mathematical equivalency between power electronics converters and synchronous generators, and emphasizes how an inherent synchronization feature of the synchronous generators can be used to improve the performance of the grid-interface converters. It has also been shown that if operated as a voltage source, the grid-interface converter could have significant stabilizing effects on the system dynamics due to non-delayed power delivery.

Fast, digitally controlled converters offer endless possibilities for the most optimal utilization of renewable resources. Moreover, power-electronics-based distributed generators can enhance power system controllability due to their fast dynamic response to the power system disturbances and deviations of the voltage and frequency. However, the grid-interface converter's phase-locked loops can cause frequency instability in cases where grid output impedance becomes very high, or when there are multiple grid-interface converters connected to the same or an adjacent bus with a "weak" link to the strong grid. On the other hand, thousands of synchronous generators can work in parallel, and share the power with much "milder" interactions in the sense that they synchronize with the grid and to each other. This paper addresses that issue by showing what features of the synchronous generators' operation offer dynamic advantages that could be useful in the future for control of the next generation of grid-interface converters. This paper additionally shows how a grid-interface converter with an adaptive virtual inertia has the ability to stabilize the system after large disturbance.

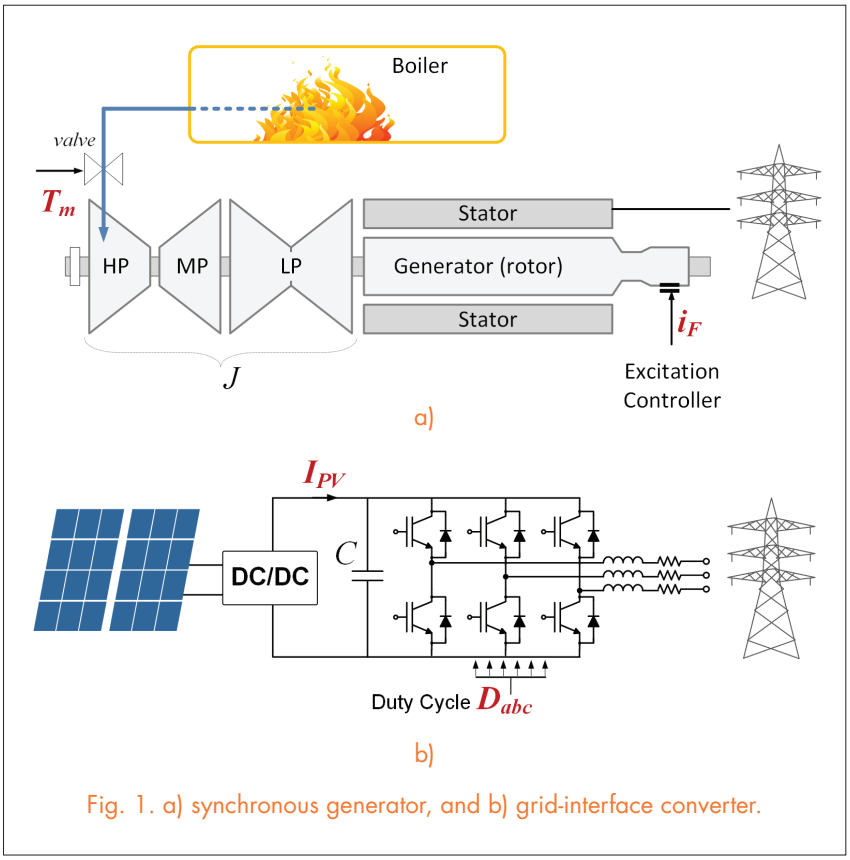


Fig. 1. a) synchronous generator, and b) grid-interface converter.

One of the main contributions of this paper is the way how frequency-locked loop of the grid interface converters is realized (duty-cycle angle θ obtained by integrating dc-link voltage). Although obvious choice for the grid-interface converters that behave as synchronous machines, this synchronization concept could open up a research space for reinvestigating the need for the conventional phase-locked loops (PLL) in the grid-interface converters in general.

Switching-Cycle Capacitor Voltage Control for Modular Multilevel DC-DC Converters

Modular Multilevel Converters (MMC) have been increasingly considered for medium-voltage and high-voltage applications due to their favorable high-modularity and scalability features. It is worth noting that the cell capacitor voltage ripple of the MMC is inversely proportional to the fundamental frequency, and proportional to the line current, which becomes an issue that prevents the MMC from being applied in low fundamental frequency and high-load conditions. Injecting different types of circulating current and common-mode voltages are approaches that have been proposed and compared. When it comes to MMC operations at very low fundamental frequencies (0.5~5 Hz), people begin looking into the possibility of dc current generation with MMC or MMC-like topologies. It has been shown that dc current can be delivered at the lines with the injection of a low frequency square-wave circulating current. Similar approaches have shown that the injection of a low frequency circulating current can enable the MMC power arms to operate in dc-dc conversions. Recently, a control method called Switching-Cycle Capacitor Voltage Control (SCCVC) was proposed for the MMC to balance the cell capacitor voltage in every switching cycle. Since the SCCVC can effectively decouple the capacitor voltage ripple from the fundamental frequency, the SCCVC can work for any fundamental frequency, including dc operations. This paper discusses the application of SCCVC in dc-dc power conversions.

Another concept—wherein a number of identical power cells are stacked in series to construct a power converter, motivated by the MMC—is also quite promising in HV and MV applications, since the voltage rating of devices in each power cell will cause a bottleneck. A comparison between the MMC topology and the conventional two-level three-phase converter raises the idea that the power arm can be regarded as equivalent to a single switch. As long as a loop composed of two power arms and a large capacitor exists, the SCCVC is able to control any low frequency or dc current delivered through a third branch that is connected to the two power arms at the same node. At the same time, all the cell capacitor voltages are balanced in one switching cycle. Leveraging the SCCVC, theoretically speaking, all the dc-dc topologies can be modified to a Modular Multilevel dc-dc Converter (MMDC), in order to extend the applications from low-voltage domains to high-voltage domains. This paper begins by illustrating the SCCVC for the MMDCs using the example of a Modular Multilevel Buck Converter (MMBC), and showing its fundamentals, benefits and limitations, and behaviors for a vast range of application domains.

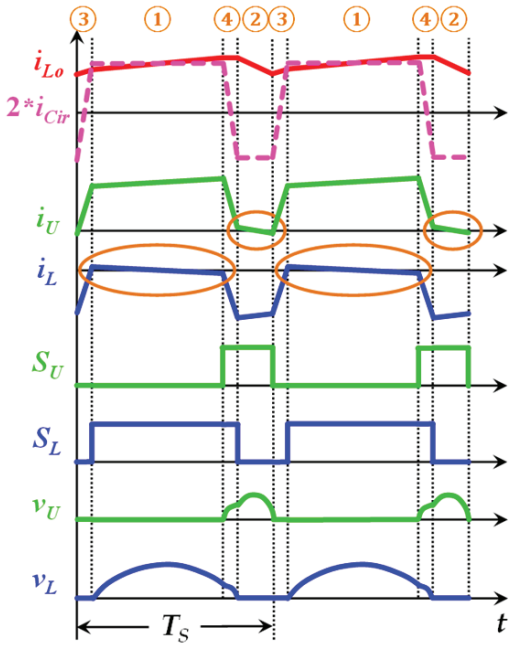


Fig. 1. Principle of the SCCVC for MMDC.

Analysis and Simplification of Modular Multilevel Converter and Circulating Current Injection

The modular multilevel converter (MMC) has emerged as a new multilevel topology for high-voltage applications during recent years. Because voltage fluctuation exists in submodules, relatively large capacitors are required to limit the voltage ripple in submodules, resulting in large capacitor size and cost. Generally, in order to reduce capacitance, voltage ripple is suppressed. With suppressed voltage ripple, under the same ripple tolerance standard, smaller capacitance can be used.

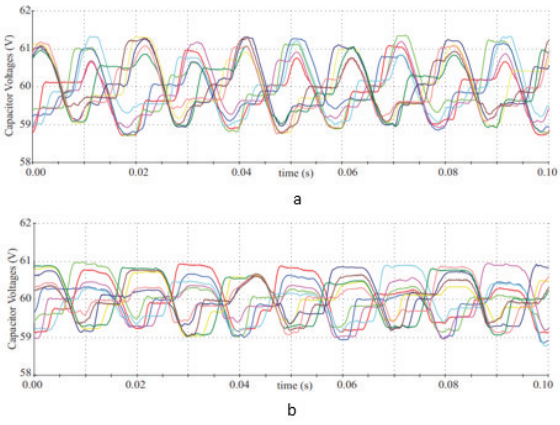


Fig. 1. (a) Capacitor voltage without injecting, (b) capacitor voltage with injecting.

One method for reducing capacitance is injecting a second-order circulating current. In an MMC system, there is a circulating current in the phase arm, which includes a second-order and a higher-order harmonic. Meanwhile, on the capacitor, there exists power with a second-order harmonic that is closely related to capacitor voltage ripple. By controlling the duty cycle, the circulating current can be modulated to be a given second-order harmonic. With that circulating current, the second harmonic of the power in the capacitor can be eliminated. Hence, the capacitor voltage ripple can be suppressed as shown in Fig. 1. As a result, given the previous voltage ripple toler-ance, a smaller capacitance can be used. However, the RMS value of the arm current will increase and along with it, the loss.

Another method for reducing capacitance is injecting high-frequency common-mode voltage and circulating current. This works only for a three-phase MMC system. In a three-phase MMC system, there are currents that circulate among three phases, and a common-mode voltage in the neutral point of the three phases. These are two factors to consider in realizing high-frequency power flow. The capacitor's energy fluctuation has an inverse relationship with its power frequency, which also means that a higher-frequency power results in a smaller capacitor-voltage ripple. The resulting suppression of the voltage ripple is shown in Fig. 2. This method works especially well in a low-modulation-index situation, such as a motor drive.

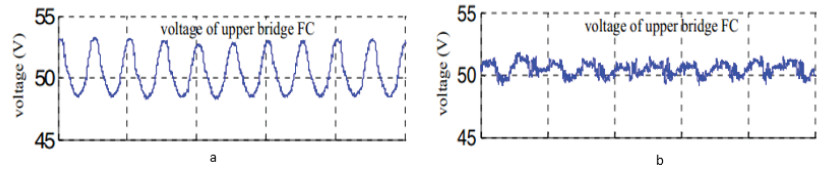


Fig. 2. (a) Capacitor voltage without injecting, (b) capacitor voltage with injecting.

In both of the methods discussed above, reducing capacitor voltage ripple usually results in a higher arm-current RMS value. Therefore, the tradeoff between capacitor size and loss should be considered carefully.

Direct Circulating Current Control and Reducing Cap-Voltage Ripple of MMC

The modular multilevel converter (MMC) has attracted a lot of attention in the past decade. Because of its modularity and scalability features, the output of MMC can, in theory, be extended to arbitrary voltage levels. Therefore, it is an excellent choice in high-power applications such as HVDC transmission, STAT-COM, medium-voltage motor drives, and so on. However, MMC has very bulky capacitors in each module, greatly increasing converter size and cost. Thus, figuring out how to reduce capacitance is one of the challenges for MMC. This paper focuses on reducing the cap-voltage ripple by injecting different circulating currents.

First, the paper analyzes the basic working principle of MMC. Conventionally, the control law of MMC is given based on two assumptions: the cap voltage is constant; the voltage over the arm inductor is relatively small. As a result of these two assumptions, we can say that the output voltage does not exactly follow the reference, and that a second-order circulating current exists. In order to precisely control the output voltage and the circulating current, this paper provides a new control law. It has been shown that for eliminating the circulating current, this control law is approximately equivalent to the conventional closed-loop control with a circulating current suppressing controller. Based on this new control law, the MMC's operation is analyzed further, and the modulation index limitation is given when the circulating current is eliminated.

This paper next deals with the issue of reducing cap-voltage ripple. When injecting different kinds of circulating current, the cap-voltage ripple of the MMC should be different. According to the new control law, circulating current can be accurately controlled and thus a comparison of cases where different circulating currents are injected can be easily given. This paper attempts to provide an optimized injected circulating current that would bring the smallest cap-voltage ripple.

The previous conclusions were reached based on a single-phase MMC, but are also suitable for a three-phase MMC. Additionally, the three-phase MMC offers a common-mode voltage, which can also be used to reduce cap-voltage ripple. Therefore, there are more choices and possibilities for a three-phase MMC; for example, a high-frequency common-mode voltage and circulating current could be injected at the same time. In the conclusion, this paper provides an analysis of the aforementioned method based on the new control law.

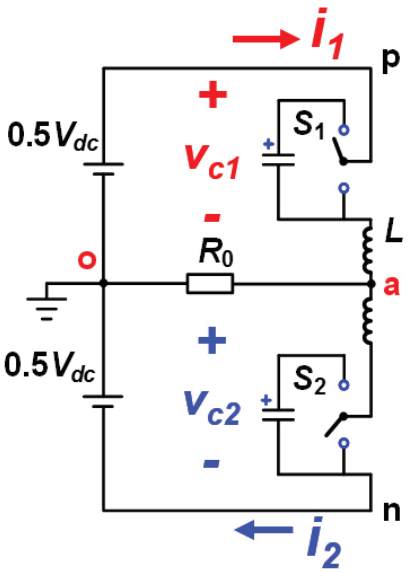


Fig. 1. MMC topology

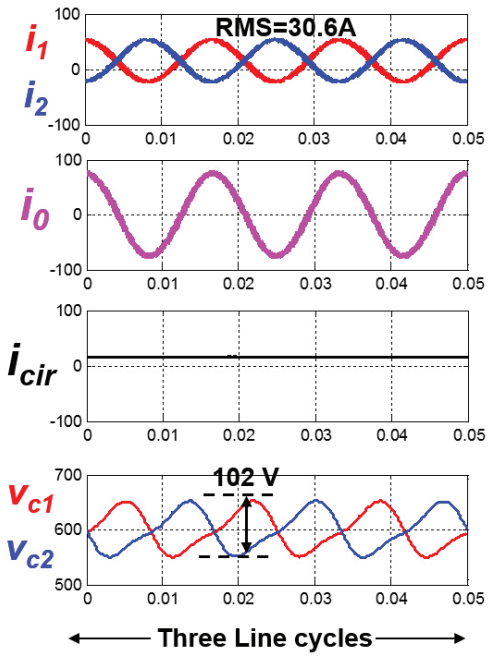


Fig. 2. Circulating current and cap voltage ripple of MMC

LCL Filter Design and Inductor Current Ripple Analysis for Three-level NPC Grid Interface Converter

The harmonic filter for a three-level neutral point clamped (NPC) grid interface converter is designed with good filtering performance and small component size. Different filter topologies are evaluated, and the LCL topology is selected because of the attenuation and size tradeoff. The basic design procedure and guideline for the LCL filter is introduced first. The design of the inverter side inductor L1 is emphasized due to its cost. A detailed inductor current ripple analysis is given based on the space vector modulation (SVM). The analysis derives the inductor volt-second and the maximum current ripple equation in the line cycle. The analytical expression for the maximum inductor current ripple is established with the analysis. It also reveals the switching cycle and current ripple distribution over a line cycle, including the power factor consideration. The total system loss is calculated with a different ripple current, and inductor L1 is determined by the loss and size tradeoff.

The capacitor and grid side inductor L2 is designed based on the attenuation requirement and the reactive power consumption. The grid code harmonic and the inverter output voltage spectrum together setup the attenuation requirement for the LCL filter. The L2 inductance is designed to meet that requirement. Finally, the resonant peak of the LCL filter is considered with the passive damping circuit. Different damping circuit topologies for the LCL filter are compared and investigated in detail. The RLC damping circuit is selected based on the damping result, component size, and the power loss. The filter design is verified by both simulation and a 200kVA three-level NPC converter hardware.

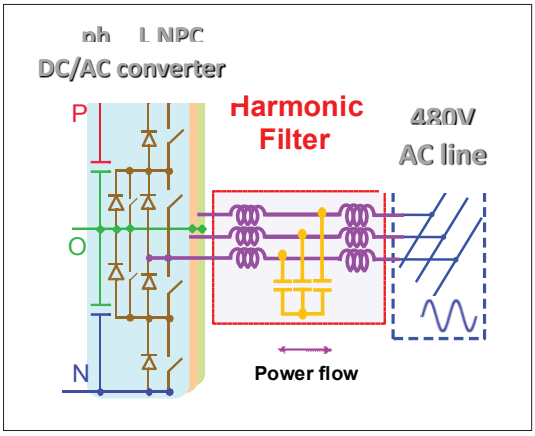


Fig. 1. Three-level NPC converter with LCL filter.

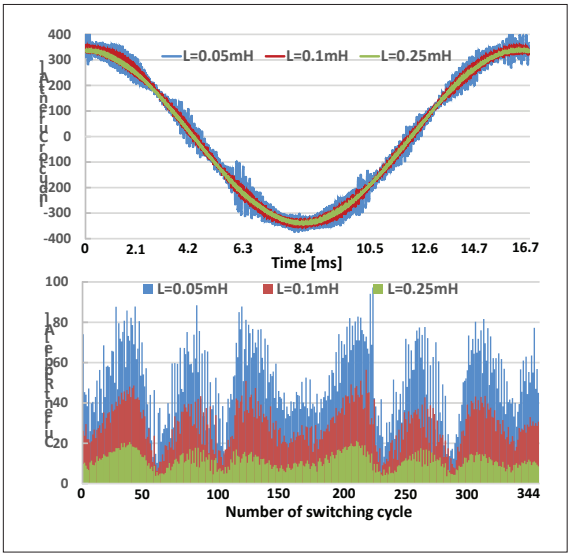


Fig. 2. Inverter side current ripple waveform.

Design and Comparison of Cascaded H-Bridge, 5-L Active Neutral Point Clamped and Modular Multilevel Converter Topologies for Medium-Voltage Drive Applications

This paper investigates the design procedure of cascaded H-bridge (CHB), 5-L active neutral point clamped (ANPC) and modular multilevel converter (MMC) topologies for medium-voltage and high-power industrial motor drive applications. The design is carried out using 1.7-kV insulated gate bipolar transistor (IGBT) technology for MMC and CHB topologies, and using 3.3-kV and 4.5-kV IGBTs for a 5-L ANPC converter. A model is derived for a multi-pulse transformer to take into account its leakage parameters' effect on converter design. A comparison is also made between topologies at different voltage and power levels. For MMC and CHB, the three following voltage levels are chosen: 4.16, 6.9 and 13.8 kV. The 5-L ANPC is designed only at the two lower levels of the aforementioned voltages. Converters are designed at the following three different power levels: 1, 3 and 5 MVA. A comparison is done from several points of view, such as capacitance requirements, diode front-end and inverter stage losses, semiconductor rating and junction temperature, and parts count.

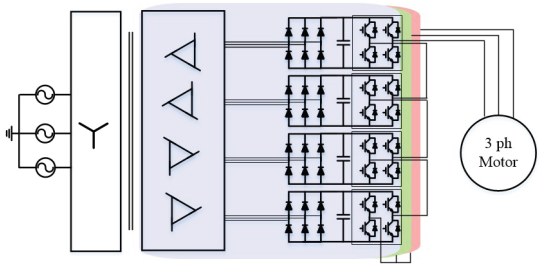


Fig. 1. Cascaded H-bridge converter with diode front-end rectifier for motor drive application.

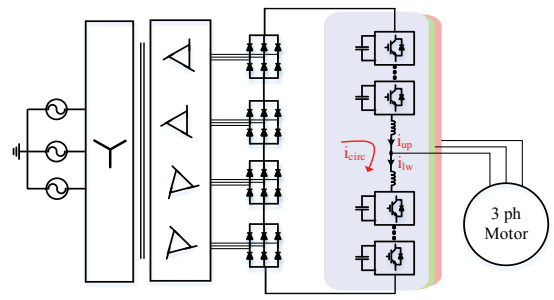


Fig. 2. Modular multilevel converter with diode front-end rectifier for motor drive application.

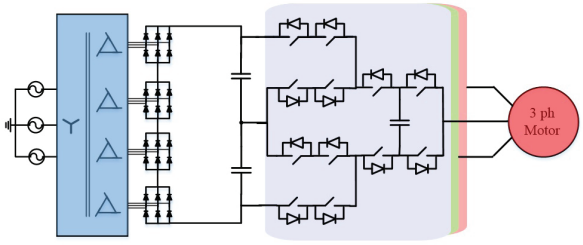
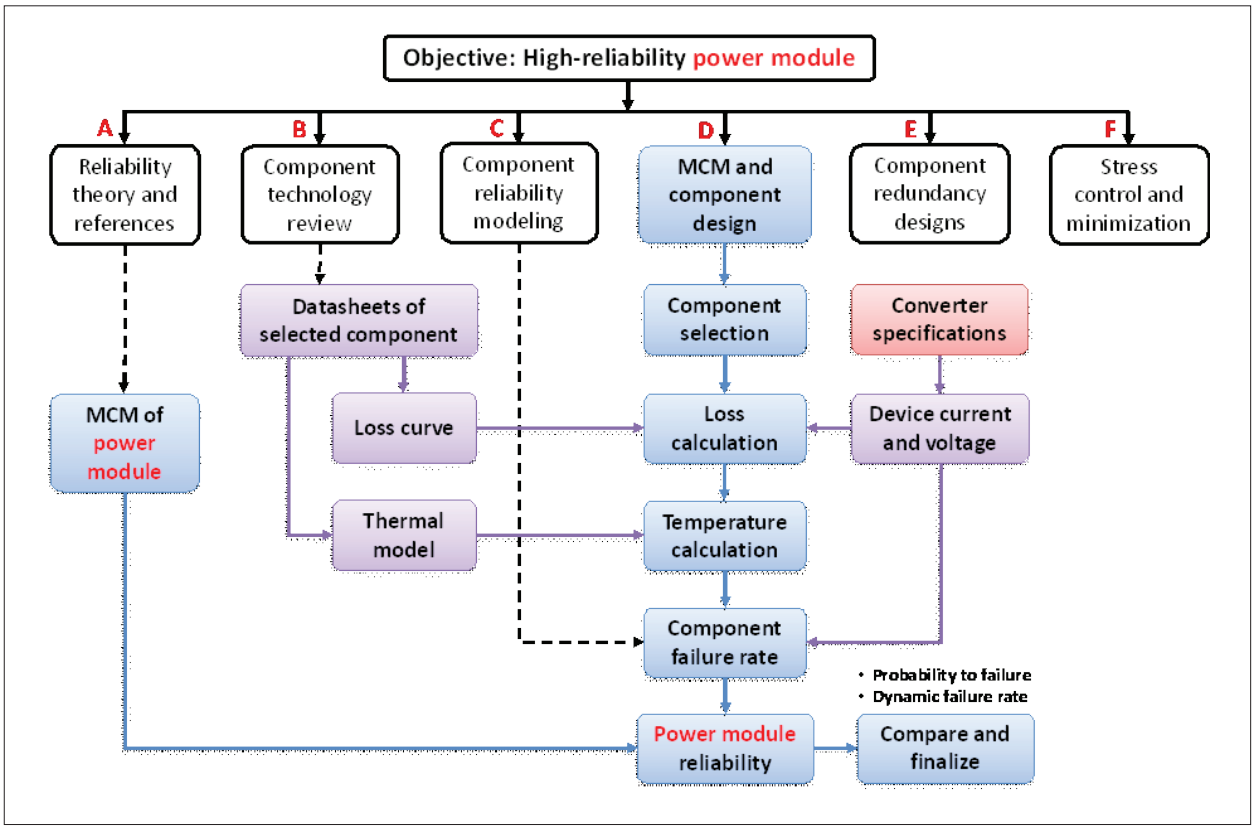


Fig. 3. 5-L ANPC converter with diode front-end rectifier for motor drive application.

Reliability-Oriented IGBT Selection for High-Power Converters

The critical nature of grid applications in power engineering demands the utmost levels of apparatus reliability as well as high availability and low maintenance. The latter additionally implies a high lifetime for all components used. Power electronics, now a mature technology, is currently employed in critical applications such as commercial aviation, and is being increasingly introduced in grid applications to improve the controllability and efficiency of power flow within power grids. The design of power converters at medium voltage and high voltage levels nonetheless still represents an immense challenge in terms of reliability. As a critical step in the Reliability-Oriented Design (ROD) of power converters, the IGBT selection should be conducted in a reliability-oriented manner. Detailed procedures of Reliability-Oriented IGBT selection are presented in this paper.

The conventional approach to deciding the current rating of IGBTs for a power converter design is basically to guarantee that the junction temperature of the IGBT will not exceed its maximum allowable value in all ranges of operating conditions. However, the lowest junction temperature does not necessarily indicate the highest reliability or the longest lifetime, which are instead related to the chip and packaging technologies from different manufacturers. Therefore, this paper mainly focuses on the impact of chip and packaging technologies on reliability performance. Comprehensive comparisons are made to determine the final IGBT selection in order to achieve the highest reliability.



Modeling of Multi-phase Three-level DC/DC Converter with Integrated Coupled Inductor

This paper investigates a multi-level approach to increase both voltage and power ratings of dc-dc converters with a paralleled phase legs configuration for renewable energy systems. And one two-phase paralleled, three-level dc-dc converter was built to work with dc-ac stage and handle 200kW power rating with 20kHz working frequency. By applying a coupled inductor the circulating current ripple is small. And the two separated coupled inductors in the converter can be further integrated as one. With one integrated coupled inductor, as shown in Fig. 1, the power density can be further increased to compare with the conventional coupled inductor case. Based on the flux analysis of the integrated coupled inductor, the mathematical model of the integrated coupled inductor can be defined first. By mapping the mathematical model in the circuit, the cirguit model can be built. As shown in Fig. 2, six mutual inductances are used to represent different coupling effects between converter arms, and four single inductance are applied to represent the leakage flux in each arm of the converter. Here, M_{ab} and M_{cd} represent the negative coupling between arm a and arm b, and between arm c and arm d, respectively. M_{ac}, M_{ad}, M_{bc}, M_{bd} represent the positive coupling between arm a, b, c, and d. And such positive coupling is designed to further reduce the output current ripple. For the paralleled phase legs, the model can be built with the concept of the three-terminal switch easily. By combining the model of paralleled phase legs with the model of the integrated coupled inductor, one can have a complete model of this converter for control-loop design.

This paper also gives and analyzes the modeling of such a converter under a symmetrical parameters assumption.

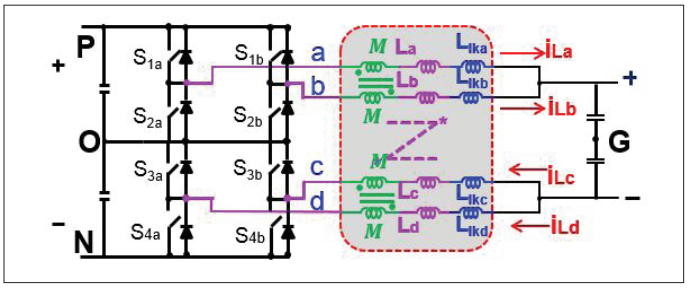


Fig. 1. 3-level dc-dc Converter with Integrated Coupled Inductor

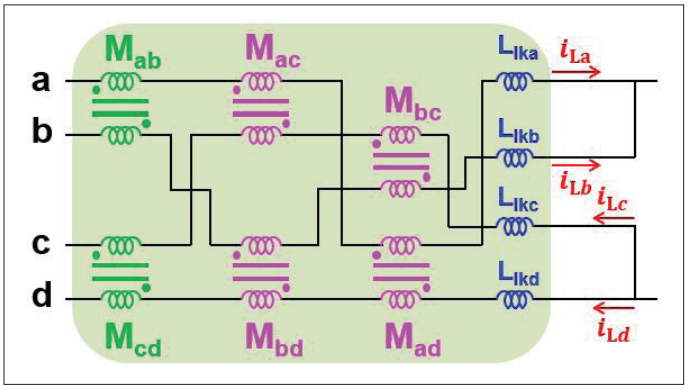


Fig. 2. Model of Integrated Coupled Inductor

With this assumption, the control-to-output transfer function is a second-order one. By further neglecting all the parasitics in the circuit, one can find that the control-to-output transfer function has a similar form compared to a conventional buck converter. M_{ab} and M_{cd} do not show up in transfer function, which means that the negative coupling effect will not affect transient response under a symmetrical parameters assumption.

With the control-to-output transfer function, both current-loop and coltage-loop control can be designed and simulation results are given.

Modularized High Frequency High Power Three-level Neutral Point Clamped PEBB cell for Renewable Energy System

This paper presents a modularized high-frequency, high-power, three-level, neutral point clamped power electronics building block (PEBB) for renewable energy system. The three-level diode neutral point clamped (NPC) and the three-level active NPC are the most popular topologies used in industrial applications based on the modularized building block. However, since the single three-level diode NPC or active NPC cell is not able to form a three-level dc-dc chopper, the applications of PEBB cells based on these two circuits are limited where a dc-dc chopper is needed. In this paper, loss analysis for the three-level chopper built by two three-level diode NPC cells or active NPC cells are conducted. Switching loops in the PEBB cells are identified, and double pulse tests are conducted for turn on and turn off transient of the switching loops. Based on the double pulse tests, the switching losses will be quantified for different switching loops. Two three-level bidirectional chopper circuits based on the active NPC PEBB cells are presented and compared. Then, the modified PEBB cell that is derived from a single active NPC cell is proposed for the three-level bidirectional chopper. Based on a common active NPC PEBB cell, the power converter can be built with a modularized structure to achieve high frequency, high efficiency, and low cost.

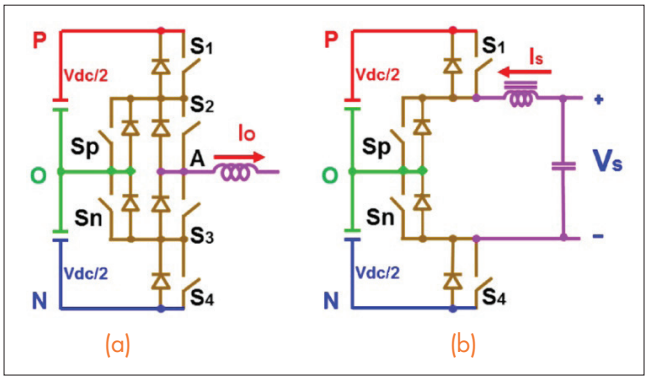


Fig. 1. PEBB cells for renewable energy system. (a) Active NPC cell for dc-ac power conversion. (b) Modified active NPC cell for dc-dc power conversion

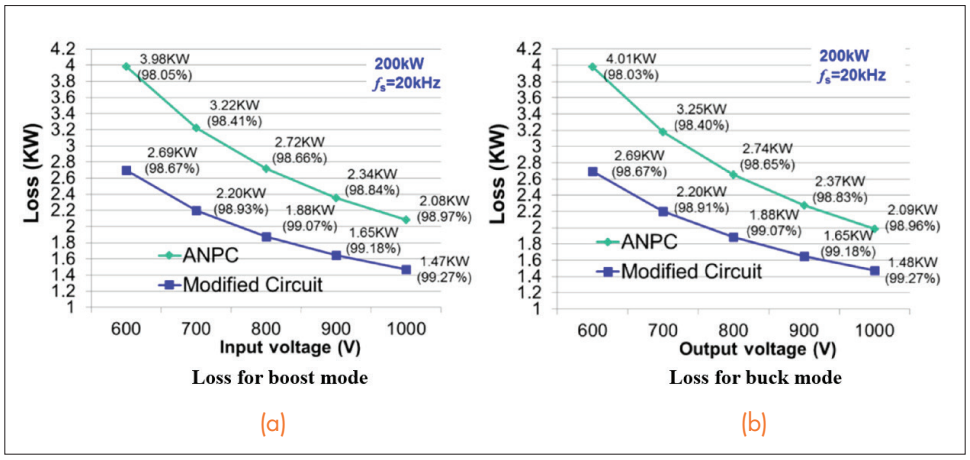


Fig. 2. Loss breakdown. (a) Boost mode. (b) Buck mode.

Modeling the Output Impedance of the Three-Phase Uninterruptible Power Supply in D-Q Frame

The three-phase uninterruptible power supply (UPS) is widely used to protect critical loads. The output impedance is a very important design specification of a UPS inverter, since the output impedance of a UPS inverter determines the voltage distortion caused by the nonlinear loads and also the stability of the whole system. This paper models the output impedance of a three-phase UPS inverter with current and voltage feedback control in d-q frame. An analytical model of UPS output impedance is derived, and experimental results are shown to verify the analysis.

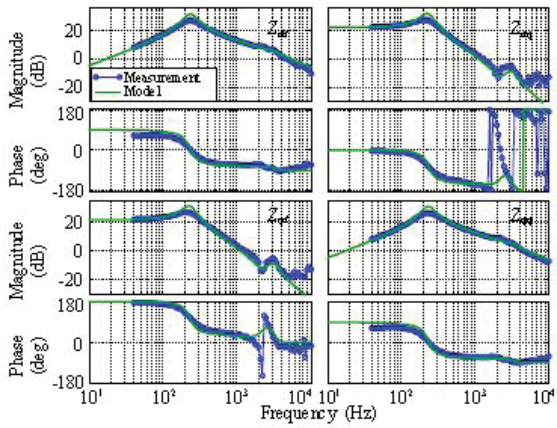


Fig.2. Measurement results compared with model for current loop control.

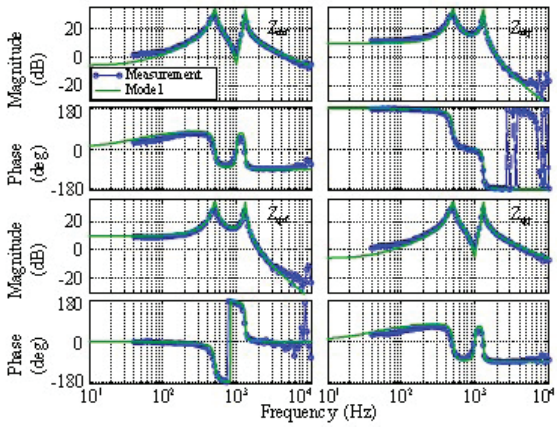


Fig. 1. Measurement results compared with model for open loop.

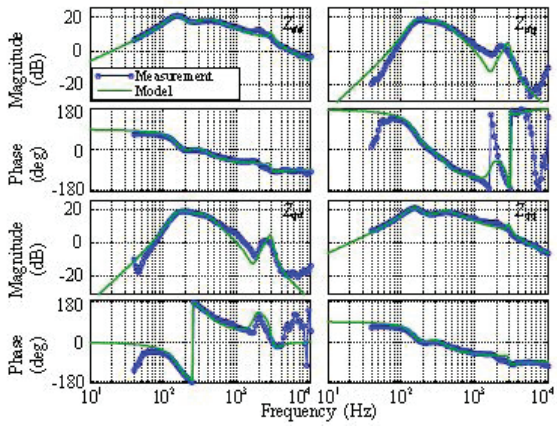


Fig. 3. Measurement results compared with model for voltage control.

Sponsored Research Nuggets

Improved Unterminated Behavioral Model for Common-Mode EMI Emission of SiC Power Converters with Different Switching Frequency

The Optimal Design of GaN-based Dual Active Bridge for Bi-Directional Plug-in Hybrid Electric Vehicle (PHEV) Charger

10kV, 120A SiC MOSFET modules for a power electronics building block (PEBB)

Modular Interleaved Single-Phase Series Voltage Injection Converter Used in Small-Signal dq Impedance Identification

Design and Implementation of Interleaved Vienna Rectifier with Greater than 99% Efficiency

Improving High-Frequency Performance of an Input Common Mode EMI Filter Using an Impedance-Mismatching Filter

EMI Behavioral Models of DC-Fed Three-Phase Motor Drive Systems

Improving the Efficiency and Dynamics of 3D Integrated POL

Evaluation of Thermal-Cycling Reliability of Sintered Nanosilver Versus Soldered Joints by Curvature Measurement

Effect of Sintering Temperature on Magnetic Core-loss Properties of a NiCuZn Ferrite for High-frequency Power Converters

Design and Evaluation of the Constant-Flux Inductor with Enclosed Winding

Gap Design for Nonlinear Ferrite Cores to Maximize Inductance

Compressive-Post Packaging of Double-Sided Die

DBC Switch Module for Management of Temperature and Noise in 220W/in^3 Power Assembly

Loss Minimization for Coupled Inductors with Significant AC Flux

Package Influence on Switching Performance of SiC Modules

Design and Implementation of Integrated Common Mode Capacitors for SiC-JFET Inverters

A 50 kW SiC Three-Phase AC-DC Converter Design for High Temperature Operation

A 1200V, 60A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications

Sensitivity Analysis of a Modular Multilevel Converter

Stress Analysis and Minimization for a Modular Multilevel Converter (MMC) to enhance the Reliability of the Converter

Reliability-Oriented Switching Frequency Analysis for Modular Multilevel Converter (MMC)

DC Fault Ride-Through Capability of Modular Multilevel Converters

Compensation of DC-Link Oscillation in Single-Phase to Single-Phase VSC/CSC and Power Density Comparison

Hybrid Modulation for Neutral Point Voltage Reduction in DC-fed Three-Level Motor Drive Systems

Discontinuous Pulse Width Modulation Methods with Neutral Point Voltage Balancing For Three Phase Vienna Rectifiers

Modular Multilevel Alternate-Arm Converter (AAC): Modeling, Design, and Control

Resistance Compression T-Networks with Active-Switch Compensation in the Input Branch for Constant-Frequency Resonant Power Conversion

A Unified Control for the Combined Permanent Magnet Generator and Active Rectifier System

Verification, Validation and Uncertainty Quantification (VV&UQ) Framework Applicable to Power Electronics Systems

Determination of “Resonant Frequency” for Current-Fed Power Amplifier Using Multifrequency Modeling Technique

Improved Unterminated Behavioral Model for Common-Mode EMI Emission of SiC Power Converters with Different Switching Frequencies

With silicon carbide (SiC) devices increasing in commercial availability, high switching frequency is becoming a general trend to increase the power density of power converters. However, high switching frequency operation exacerbates EMI emissions in a system, resulting in the need for accurate EMI power converter models to predict noise and aid in the design of their EMI filters. The unterminated behavioral model (UBM), which can predict a power converter's CM noise in the conducted EMI frequency range using equivalent noise sources and impedances, has been verified as an effective tool for learning the EMI noise generation and propagation in an inverter (motor drive) system, as shown in Fig. 1. The accuracy between the model's prediction and the actual measurement is limited to 10MHz.

In this paper, the noise floor, which is the main factor limiting UBM prediction above 10MHz, is found to occur from 6MHz in the experiments. This is caused by the limited vertical resolution of the oscilloscope. The development of a segmented-frequency measurement with high-pass filters is proposed to acquire the CM spectrum above 6MHz, by ranges of 6MHz to 15MHz, and 15MHz to 30MHz, which covers the whole EMI range. With this proposed method, there is no noise floor in the noise spectrums, and the UBM prediction capacity is extended to 30MHz in the experiment. In Fig. 2, the prediction of input and output CM spectrums by the UBM matches the measurement of the 3kW, 300V dc, SiC three-phase inverter, switching at 20kHz. Additionally, when the inverter is working with a switching frequency as high as 70kHz, the UBM can provide good prediction of CM input and output noise, matching measurements in the entire EMI range.

Furthermore, this paper improves the extraction fixture by reducing the equivalent series inductance and acquiring high-accuracy impedance measurements. With the redesigned fixture, the error between the prediction from the UBM and the actual measurement is even smaller, showing a perfect match.

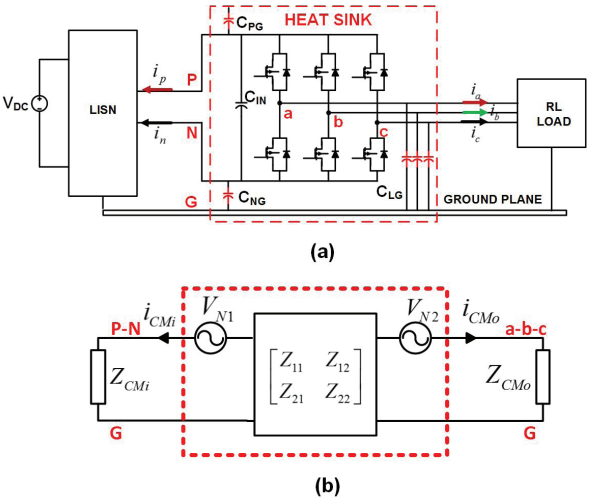


Fig. 1. (a) Three-phase SiC MOSFET inverter setup schematic diagram, (b) Unterminated behavioral model to be extracted.

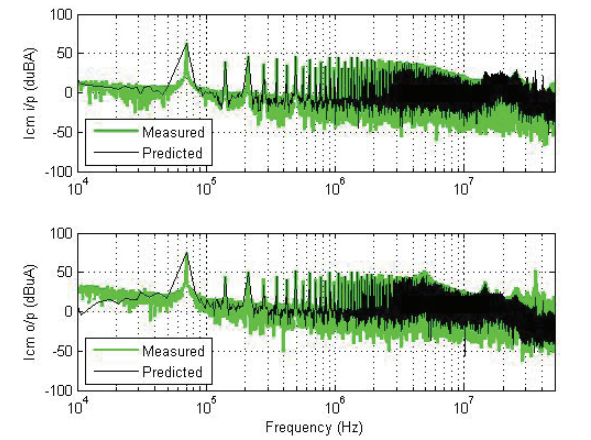


Fig. 2. Comparisons between the measurements (light) and the predictions (dark) for the 20 kHz validation case with some chokes.

The Optimal Design of a GaN-based Dual Active Bridge for a Bi-Directional Plug-in Hybrid Electric Vehicle (PHEV) Charger

A high-frequency, high-efficiency bi-directional battery charger for a Plug-in Hybrid Electric Vehicle (PHEV) is built with high-voltage normally-off GaN-on-Si HFETs. The optimal design of the isolated 500kHz Dual Active Bridge dc-dc stage is detailed herein, taking into account the wide battery voltage range and sinusoidal charging, in order to eliminate the large dc link capacitor.

This work first characterizes the GaN multi-chip module in terms of static and dynamic performances, including forward and reverse conduction characteristics, turn-on and turn-off switch-ing energy, dynamic on-resistance, and output capacitance. A loss model of the DAB converter is thus developed and compared with experimental measurements.

To optimally design the dual active bridge converter, the commutation inductance value must be determined. Since the battery charger has a wide load current and voltage range, the selection criteria of the inductance is to achieve minimum charging loss through the entire charging cycle based on the loss model developed above. The total energy loss through the charging cycle with different commutation inductance is plotted in Fig. 1. Minimum energy loss is obtained when commutation inductance equals 3μH.

A high-frequency transformer with an integrated commutation inductor is built with 3F35 material. A certain amount of space is intentionally left between the interleaved primary and secondary windings so that enough leakage flux can be stored to reach the desired leakage inductance value, as shown in Fig. 1 (bottom).

Experimental results of a 500kHz DAB converter with a discrete inductor and transformer can achieve 97.2% efficiency at 1kW and 96.4% efficiency at 2.4kW. By integrating the inductor into the transformer, 98.2% efficiency is achieved at 1kW, as shown in Fig. 2.

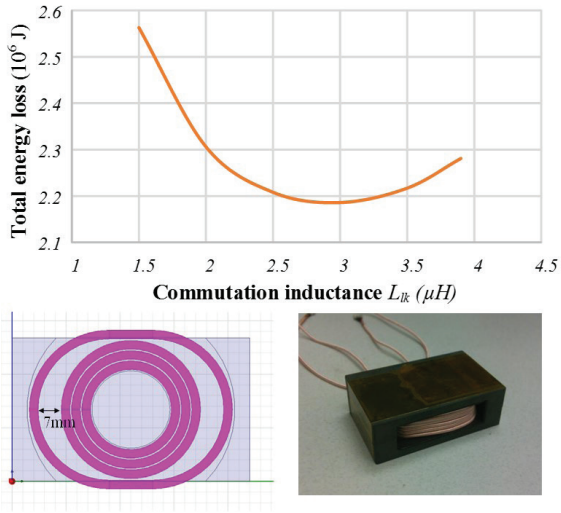


Fig. 1. Commutation inductance selection and the integrated transformer design with integrated commutation inductor.

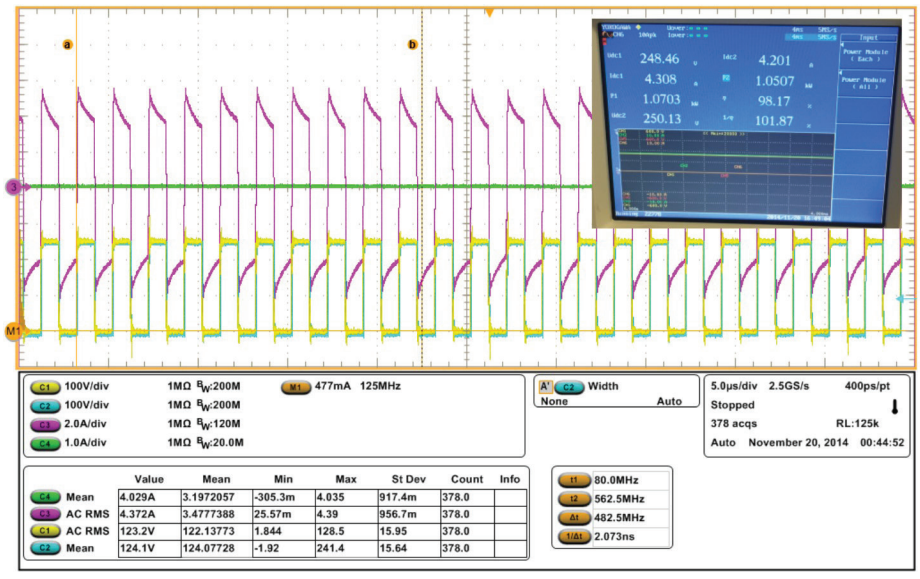


Fig. 2. GaN converter with integrated inductor at 1 kW reaches 98.2% efficiency.

10kV, 120A SiC MOSFET Modules for a Power Electronics Building Block (PEBB)

For this work 10kV, 120A all-SiC half-bridge modules were tested and simulated for use in 4kV, 100A power electronics building blocks (PEBBs), which are standard, multifunctional units that can replace specialized devices in order to simplify the design and reduce the cost of converter systems. This PEBB design consists of four 10kV SiC modules in an H-bridge configuration (Fig. 1). Each module contains twelve parallel 10-kV SiC DMOSFETs, and six parallel 10kV SiC junction barrier Schottky (JBS) diodes. Double-pulse tests (DPTs) were conducted on the 10kV modules up to 4.7kV and 100A in order to evaluate their hard switching capabilities. The DPT results revealed fast switching of the modules, and minimal ringing and overshoot. A Saber model of the module was then compared to the experimental results, which showed sufficient agreement with the testing waveforms. This model was then used to simulate the PEBB operation.

The PEBB structure and layout are shown in Fig. 1. In addition to the SiC H-bridge, each PEBB has two arm inductors, two series dc link capacitors, and a 6.5kV IGBT for short-circuit protection. The IGBT is always conducting unless the desaturation protection on the IGBT gate driver is triggered. This is meant to protect the H-bridge from the energy stored in the DC link capacitors. All the interconnections are implemented with a laminated bus bar, which can effectively reduce the loop parasitic inductance. The optimized layout design reduces loop inductance and can therefore improve switching performance.

DPTs were carried out on ten 10kV, 120A SiC MOSFET modules up to 4.7kV and 100A. Testing was conducted at room temperature, with applied on-state and off-state voltages of +18V and -8V, respectively, and an external gate resistance of 5Ω. Fig. 2 shows a waveform for one of the modules at 4.7kV and 100A. Rise and fall times of 110ns and 180ns, and slew rates of 0.73A/ns and 21V/ns, were achieved. As shown in the figure, minimal ringing and overshoot (approximately 30A and no voltage overshoot) were observed. Turn-on and turn-off switching losses at 4.7kV and 100A were calculated to be 172mJ and 21mJ, respectively. All of the modules demonstrated similar DPT waveforms and switching performance. The waveforms from a Saber model of the 10-kV SiC MOSFET and JBS half-bridge developed by Al Hefner at NIST were then compared to the experimental results, and sufficient agreement was observed. With this verification, the PEBB functionality was then simulated, followed by experimental testing.

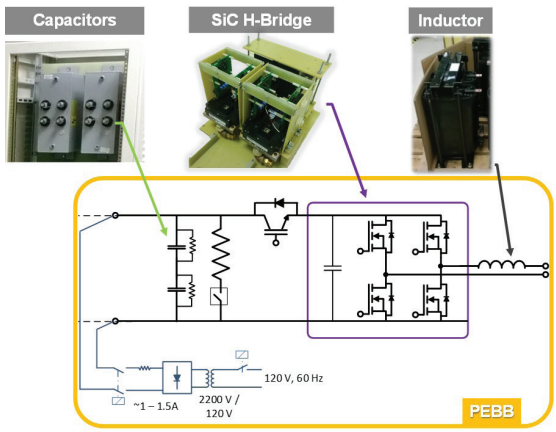


Fig. 1. PEBB with bulk capacitors, SiC H-bridge, and inductor.

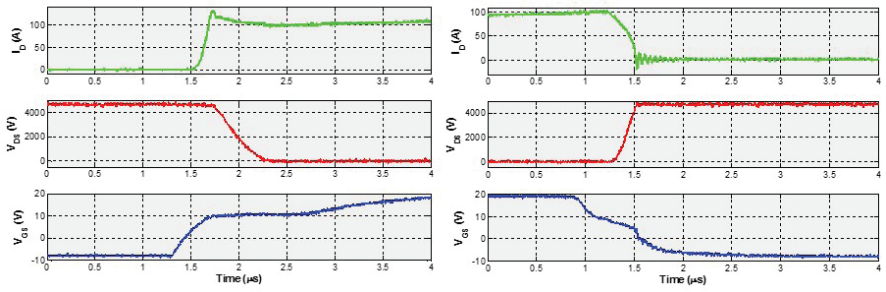


Fig. 2. Turn on (left) and turn off (right) DPT waveforms at 4.7kV and 100A with the drain current (top), drain-source voltage (middle), and gate-source voltage (bottom) shown.

Modular Interleaved Single-Phase Series Voltage Injection Converter Used in Small-Signal DQ Impedance Identification

Stability analysis of modern three-phase ac power systems is performed using small-signal impedances identified in a synchronous reference dq frame. A single-phase series voltage injec-tion is used to perturb ac and dc systems in order to perform small-signal impedance identification. This paper proposes using an interleaved cascaded H-bridge converter to generate a volt-age perturbation in series with the power system. Special attention is focused on the design procedure, including the selection of inductor and capacitor values, in an attempt to optimize the converter's performance and maximize the injection range. Decoupling control is proposed to regulate ac injection voltage, providing a robust and reliable strategy for regulating series voltage injection. Furthermore, low-bandwidth dc voltage control is incorporated into the control, assuring dc voltage control for each H-bridge module. Analytical expressions, which describe the control procedure, are derived and presented in the analysis. The proposed converter is extensively sim-ulated using a switching simulation model, and subsequent results show the excellence of the developed design procedure. The simulation model and hardware prototype results verify the effectiveness of the proposed series voltage injection solution.

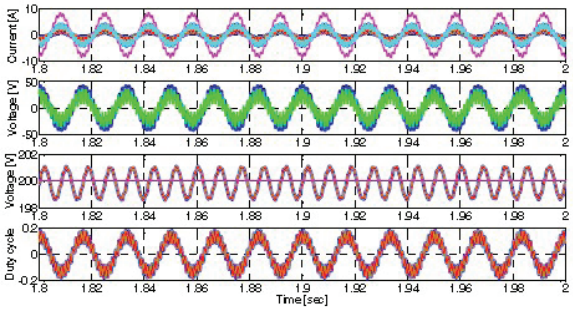


Fig. 1. Simulation waveforms of interleaved SVI converter when perturbing a power system with an 800Hz injection: (a) Inductor currents (b) injected voltage and reference voltage (c) dc voltages and dc reference voltage (d) H-bridge duty cycles.

Design and Implementation of Interleaved Vienna Rectifier with Greater than 99% Efficiency

Three-phase rectifiers have been widely used in many industries and increasing efficiency has always been a hot topic. Conventional two-level six-switch boost rectifiers are dominant due to their simplicity. However, for a higher efficiency, three-level converters are better options because lower switching voltage allows for the use of lower-voltage switches, which usually presents lower on resistance and smaller-junction capacitors. Among the three-level topologies, Vienna rectifiers are widely used to achieve high efficiency. With the use of a SiC diode, the reverse recovery loss from diodes in Vienna rectifiers can be totally eliminated, which further makes the Vienna rectifier a promising topology in achieving high efficiency. Additionally, unlike other bi-directional topologies, there is no need to worry about the shoot-through problem. Thus, in this paper, a Vienna rectifier is selected as the basic converter unit for the interleaved system.

Paralleling switches or converters are commonly used to achieve higher efficiency and better thermal management. In such practices, interleaving the gate signals of several sub-converters instead of simply gating them simultaneously can further enhance efficiency and power density. The cancellation effect among the interleaved sub-converters allows for smaller input filters. In other words, to achieve the same power quality with the same passive components, the switching frequency of each sub-converter in the interleaved systems can be lower, which lowers switching loss. Additionally, applying the interleaving technique may reduce EMI filter size due to its cancellation effect among sub-converters. Thus, the interleaved Vienna rectifier, which merges the advantages of the Vienna rectifier and interleaved systems in achieving high efficiency, is discussed.

In this paper, the design of a 3kW, three-phase, two-channel interleaved Vienna rectifier with greater than 99% efficiency is presented. The converter efficiency is optimized for 230V, 360-800Hz input voltage, 650V output voltage and 3kW output power under a power quality requirement from a standard DO-160E. The operation principle of the interleaved Vienna rectifier is presented, with special attention given to circulating current generation and suppression. A comprehensive design procedure for the interleaved Vienna rectifier, including a design flowchart, loss estimation for the converter, design guideline of inter-phase inductors and semiconductor selection is described. A converter prototype is built and experiment results are shown, verifying the validity of the design procedure.

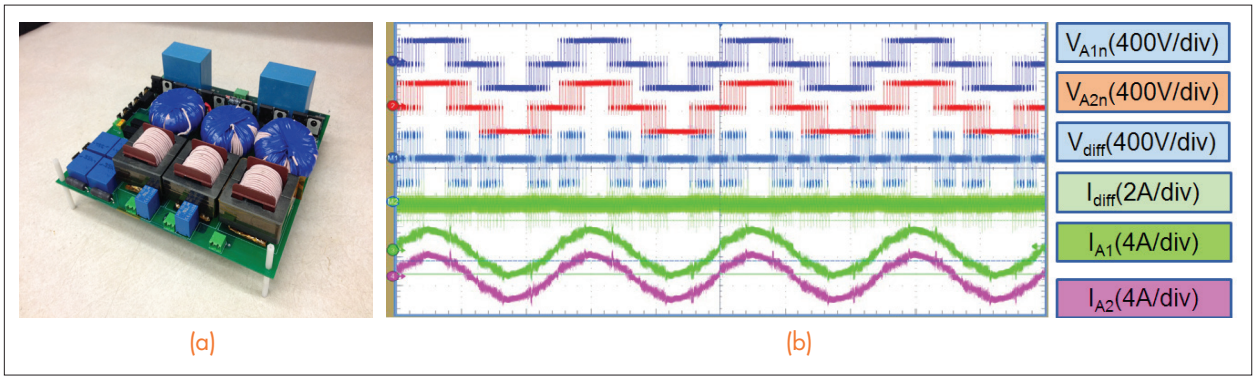


Fig. 1. (a) Converter prototype. (b) Experimental waveforms at nominal load.

Improving High-Frequency Performance of an Input Common Mode EMI Filter Using an Impedance-Mismatching Filter

This paper investigates the impedance interaction between the electromagnetic interference (EMI) filter and the noise propagation path, and its influences on the filter's design. It proves that the impedance resonance in the propagation path decreases the filter's high-frequency in-circuit attenuation. This paper proposes a method to improve the filter's high-frequency performance using an impedance-mismatching filter. The impedance-mismatching filter damps the resonance in the common mode (CM) noise propagation path and eliminates the high-frequency noise spike. By applying this method in the filter design, the CM inductor of the EMI filter can be significantly reduced, since overdesign of the EMI filter—caused by its high-frequency performance degradation—is avoided, and the filter can potentially achieve high power density. This paper also proposes a design procedure for this impedance-mismatching filter, as well as an improved EMI filter design method taking impedance mismatching into account.

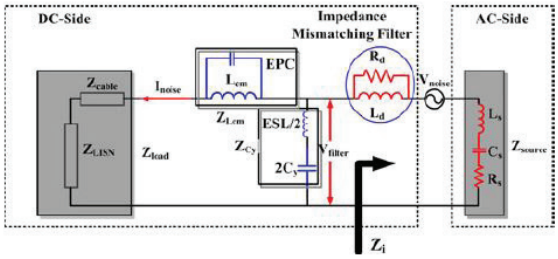


Fig. 1. Motor drive system with an EMI Filter.

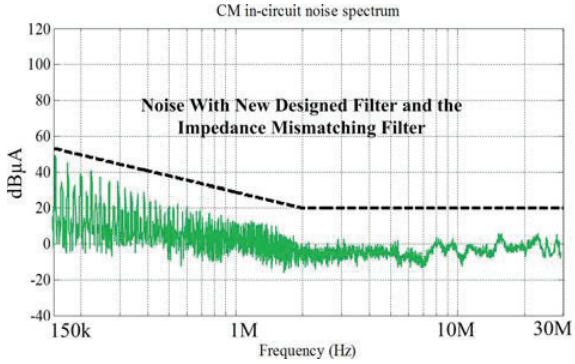


Fig. 2. Noise spectrum with the improved filter and the impedance mismatching filter.

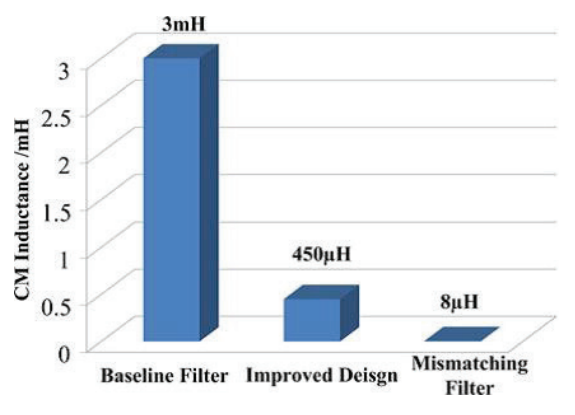


Fig. 3. Comparison of the CM inductances.

EMI Behavioral Models of DC-Fed Three-Phase Motor Drive Systems

Behavioral electromagnetic interference (EMI) models based on Thevenin equivalents are proposed for a dc-fed three-phase motor drive system. Both common-mode (CM) and differen-tial-mode (DM) noise models are developed to accurately predict the total EMI noise in accord-ance with the DO-160 standards for aerospace applications. Beyond the switching frequency of the drive, the CM noise model is found to behave like a two-port linear network and is shown to predict changes in the input-side EMI due to any changes in the load-side parameters, or vice versa. Simplified one-port behavioral models for DM noise are then used to predict the total noise at both the input and output sides of the motor drive. Such models can be very useful in system-level EMI analysis and also in understanding how EMI filters and harnesses affect the overall EMI in a motor drive system. The models run in the frequency domain and are validated with experiments up to 30MHz.

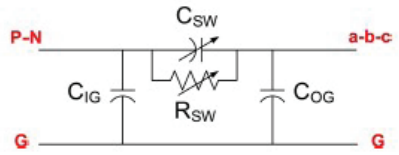


Fig. 1. Approximate CM equivalent circuit of the model impedances in motor drive.

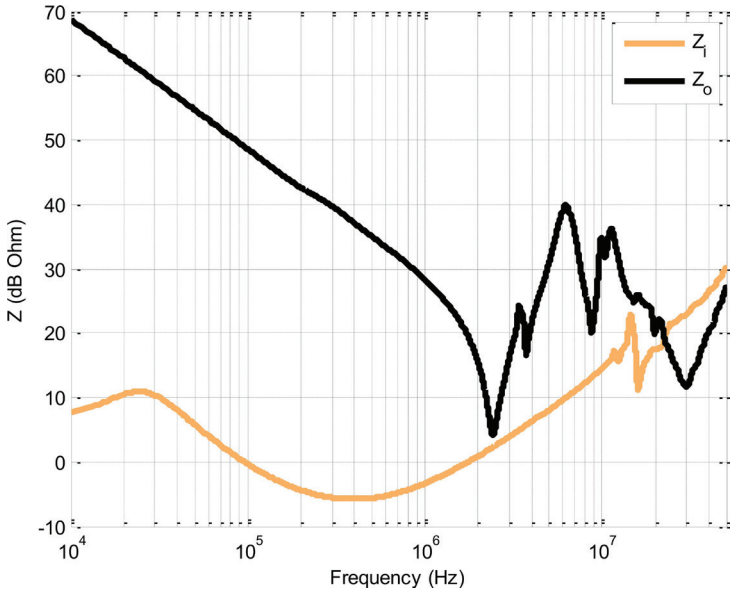


Fig. 2. CM impedance of the external network after implementation of RC shunt (shunt condition).

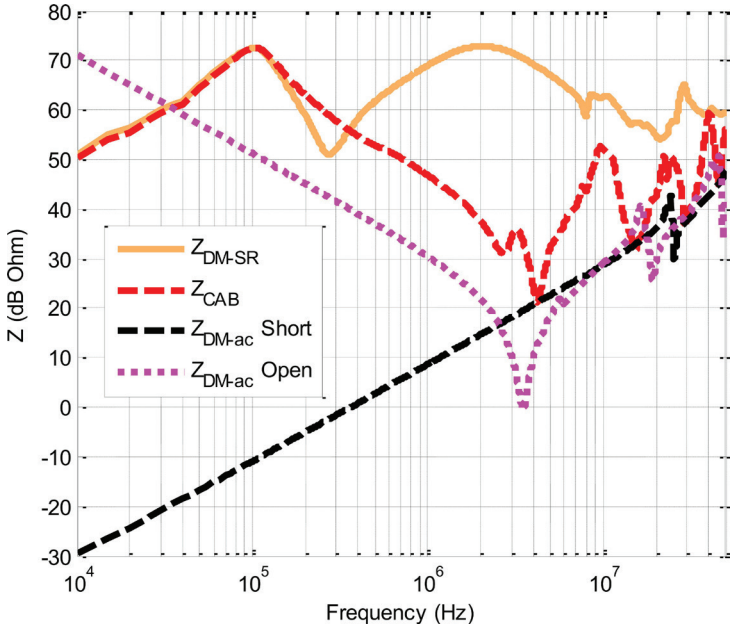


Fig. 3. Output DM impedance of the motor drive and the DM impedance of the network at the output side.

Improving the Efficiency and Dynamics of 3D Integrated POL

The three-dimensional (3D) integrated non-uniform flux inductor has shown good performance in achieving high power density and high efficiency in Point of Load (POL) module design. In this work, both single-phase and two-phase coupled non-uniform flux inductors are designed to build an 18A POL module with a QFN package, as shown in Fig. 1. The non-uniform flux inductor's unique property of varying core loss at different load conditions is analyzed, and the two-phase coupled inductor design that considers both efficiency and dynamics is demonstrated. The module evaluation shows improvement in efficiency and power density in comparison to conventional design.

One unique property of the non-uniform flux inductor is its variable core loss at different load conditions. Although the total flux is clamped by the voltage-second applied on the core, and independent to the load current, the flux density (B_{AC}) distribution changes a great deal at different load conditions. At heavy load conditions, B_{AC} is pushed out by the strong H_{DC} near the vias; while at light load conditions, the major portion of B_{AC} is concentrated in a small volume around the vias. As a result, the core loss density (P_v) distribution has a similar pattern as B_{AC}: at light load conditions, the large P_v value is located in a small core volume near the vias, which diminishes its core loss production (the product of P_v and core volume). This special property, along with the smaller H_{DC} at light load conditions, means a smaller core loss at light load than at heavy load conditions.

For the two-phase coupled inductor, a structure with a slot between two phases and low permeability filling material is proposed (as shown in Fig. 2). By controlling the permeability of the filling material, the non-linearity of L_{ss} and L_{tr} can be controlled to achieve a balanced trade-off between the efficiency and dynamics of the POL module. The low permeability filling material is characterized, and the extra core loss it induces is analyzed, showing that the low permeability material contributes only a very small portion of the total inductor core loss due to its small volume portion.

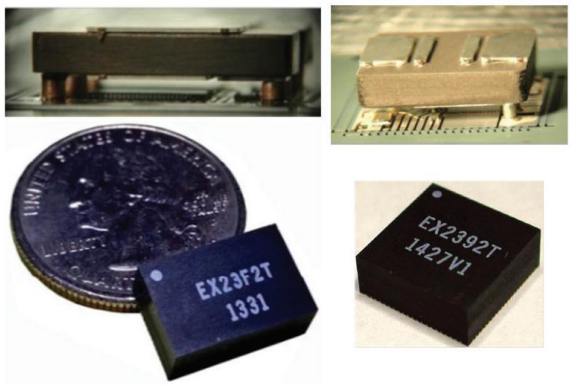


Fig. 1. 3D integrated POL modules in QFN package (left: single-phase module; right: two-phase coupled module).

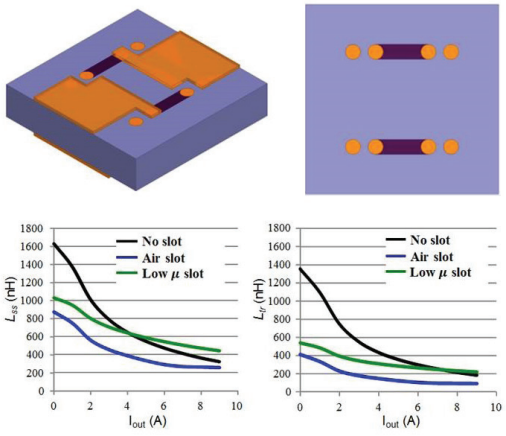


Fig. 2. Coupled inductor with low permeability slot structure (top figures) and its inductance comparison with no slot and air slot structure (bottom figures).

Evaluation of Thermal-Cycling Reliability of Sintered-Nanosilver Versus Soldered Joints by Curvature Measurement

In this work, the thermomechanical reliability of sintered-silver joints was studied in comparison with the soldered joints of two lead-free solders: SN100C and SAC305. Die-attach samples were fabricated by bonding 10 mm × 10 mm silicon "mechanical" chips to silver-metallized copper blocks and direct bond copper (DBC) substrates according to the respective heating profiles of a nanosilver paste and the two solders. The die-attach samples were thermally cycled between -40˚C and +125˚C. Bonding reliability was evaluated by measuring the bending curvatures of the cycled samples and examining the cross sections of the samples under an electron microscope. Bending of the bonded structures, which is the result of mismatched coefficients of thermal expansion between silicon and copper or DBC, offered a non-destructive method for monitoring the integrity of the bond line. The bending curvatures of all of the die-attach samples decreased rapidly after they were thermally cycled. Most of the drop in curvature can be attributed to stress relaxation in the bonding materials without bond-line cracking. However, in the samples on copper blocks, after 800 cycles, the curvatures of the soldered samples decreased to near zero m^{-1}, whereas those of the silver-sintered samples retained approximately 30% of the original curvatures. Scanning electron microscopy images showed that the joints of the soldered samples with near zero m^{-1} curvature had been cracked almost all the way through, whereas the joints of the sintered samples were still intact. These results demonstrate that sintered-silver joints are more reliable than soldered joints.

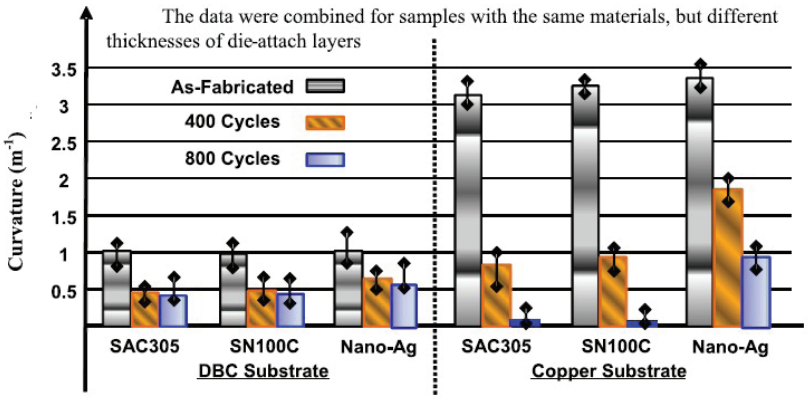


Fig. 1. Curvatures decrease with thermal cycling for samples with different substrates and different die-attach layers.

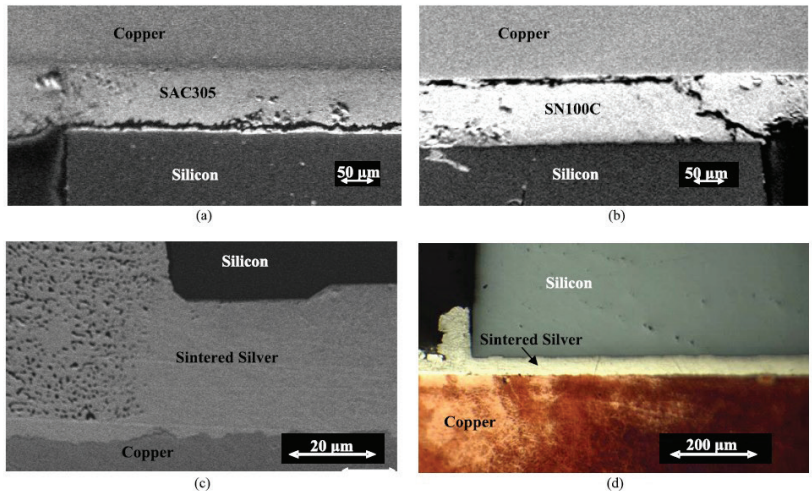


Fig. 2. Cross sections of copper samples after 800 cycles for (a) cracked SAC305 soldered joints, (b) cracked SN100C sol-dered joints, and (c) intact sintered-silver joints, and (d) intact sintered-silver joints under low magnification.

Effect of Sintering Temperature on Magnetic Core-loss Properties of a NiCuZn Ferrite for High-Frequency Power Converters

In an effort to find a magnetic material for making low-loss magnetic components for high power-density converters, we investigated the effect of sintering temperature of a commercial NiCuZn ferrite powder doped with Bi_2O_3 on the magnetic core-loss characteristics, both the complex permeability and core-loss density at high magnetic flux density and 5MHz. For comparison, we characterized a custom-made NiZn ferrite (4F1) toroid core from Elna Magnetics (Saugerties, NY), which had the same dimensions as our sintered toroid cores with sintering temperature higher than 850°C.

Fig. 1 shows plots of the frequency dispersions of the complex permeabilities obtained on the sintered LSF 50 cores and the custom-m ade NiZn ferrite (4F1) core. From the figure, the LSF 50 cores, except the one sintered at 850° C, had stable real parts of permeability beyond 10 MHz; the real parts began to show the relaxation resonance phenomenon at around 30MHz. The real part (μ') of the permeability of the LSF 50 core sintered at 850°C was about 28, significantly lower than the others; however it remained stable over 70MHz. The imaginary parts (μ") of the permeabilities of all the sintered LSF 50 cores increased with sintering temperature and also had the resonance phenomenon at about 30MHz. Comparing the μ'and μ" traces of the NiZn ferrite (4F1) and those of the NiCuZn ferrites, we see that the NiZn ferrite had a μ' trace similar to that of the LSF 50 sintered at 950°C; however, the μ" of the NiZn ferrite was significantly higher than that of the 950°C sintered LSF 50 ferrite over megahertz frequency regime. Fig. 2 shows the core-loss density plots measured at 5MHz of all the sintered LSF 50 cores and NiZn ferrite (4F1) core that were submerged in a 100°C oil bath. The figure clearly shows that the sintered LSF 50 cores, except the one sintered at 850°C, outperformed the 4F1 core. The cores sintered at 950°C and 1000°C had about the same core-loss densities that were the lowest and were nearly two to three times lower than that of the NiZn ferrite.

A commercial NiCuZn ferrite powder doped with Bi_2O_3 was used to study the effect of sintering temperature on the magnetic properties of both the complex permeability and core-loss density, for applications in high-frequency power converters. The ferrite powder was sintered into toroid cores at 850°, 900°, 950°, 1000° and 1050°C for two hours. We found that the sintering condition at 850°C for two hours was not sufficient to densify the powder, resulting in low relative permeability and high core-loss density. All the other sintered cores had relative permeabilities in the range of 60–115, which followed the trend of higher permeability with increasing temperature. The core-loss densities measured at 5MHz and several to over 10 mT of B-field strength were the lowest from the cores sintered at 950°C and 1000°C. Comparing with the core-loss density of a commercial NiZn ferrite (4F1) toroid core, the loss densities of all of the sintered LSF 50 cores, except the one sintered at 850°C, were two to three times lower than that of the NiZn core. We believe that a combination of high density, large grain size, and high electrical resistivity of the sintered LSF 50 core contributed to lowering the eddy current loss and hysteresis loss under the 5MHz alternating magnetic field excitation.

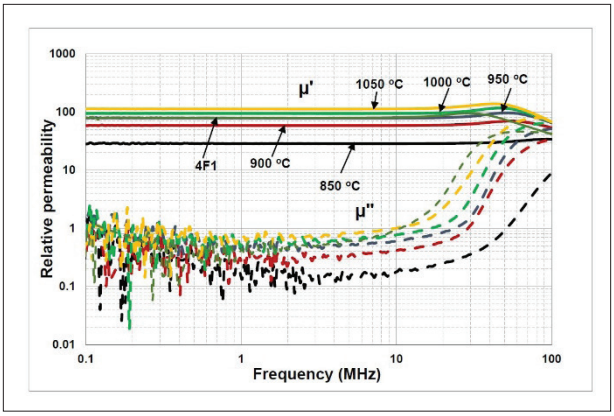


Fig. 1. Complex permeability dispersion spectra of the sintered LSF 50 toroid cores and the NiZn ferrite (4F1) core.

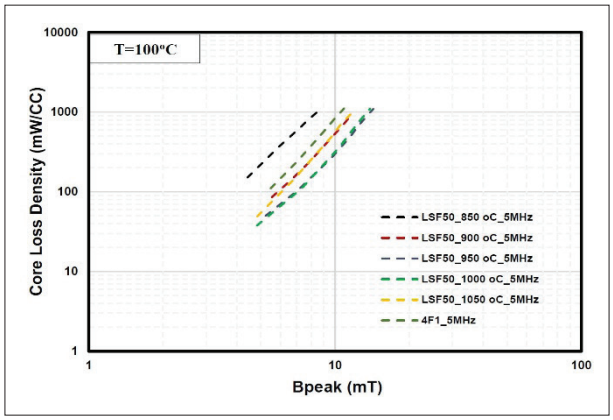


Fig. 2. Core loss density of sintered LSF 50 toroid cores and NiZn ferrite (4f1) core at frequency of 5MHz

Design and Evaluation of the Constant-Flux Inductor with Enclosed Winding

The recently introduced "constant-flux" concept is leveraged to distribute magnetic flux in order to improve energy density, lowering the profile of an inductor. The optimal flux distribution with normalized parameters is identified mathematically, and verified by simulation. It is then applied to reduce the dcresistance of a commercial inductor by a factor of two, keeping the outer dimensions and inductance the same. Thermal-limited current rating is improved by 50%, where-as saturation-limited current rating is improved by 20%, thanks to the suppression of flux crowding. The simulation result is verified by measurement results of a prototype under high current bias.

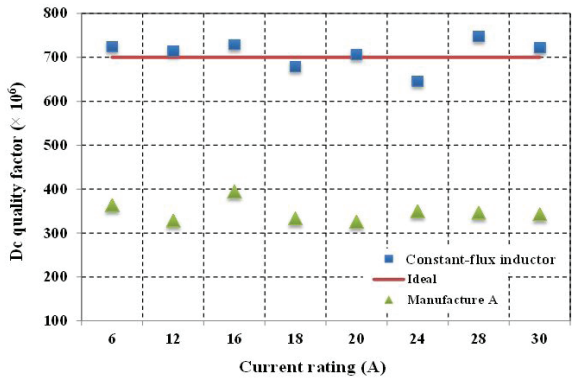


Fig. 1. Comparison of dc quality factor between a series of commercial inductors with a package size of 10 × 10 × 4 mm³ and constant-flux inductors with same inductance and package size for different current ratings.

For this paper, a behavioral model of a constant-flux inductor was constructed. With given specifications, a winding configuration with uniform flux distribution can be achieved by following the design equations and procedures. In order to generalize the design procedure and to analyze the impacts of design parameters systematically, the constructed model with normalized parameters is discussed herein. As shown in Fig. 1, by using normalized parameters for an optimal design, an improvement factor of two on the Q_{dc} is obtained for the whole series of inductors thanks to the constant-flux distribution.

In this paper, the optimal design of a constant-flux inductor that maximizes the inductor's performance is discussed. The design procedure of the constant-flux inductor is normalized so that the results are more general. In addition, the normalization decouples geometrical dimensions and magnetic material properties in design and evaluation. The heat rating current is improved by 50% because the dc quality factor of the constant-flux inductor is two times larger in comparison to a commercial product with the same volume and inductance. The saturation rating current is also improved by 20% as a result of the uniform flux distribution inside the core. The simulation result of the saturation current is verified by the measurement results on the fabricated inductor prototype under different dc currents.

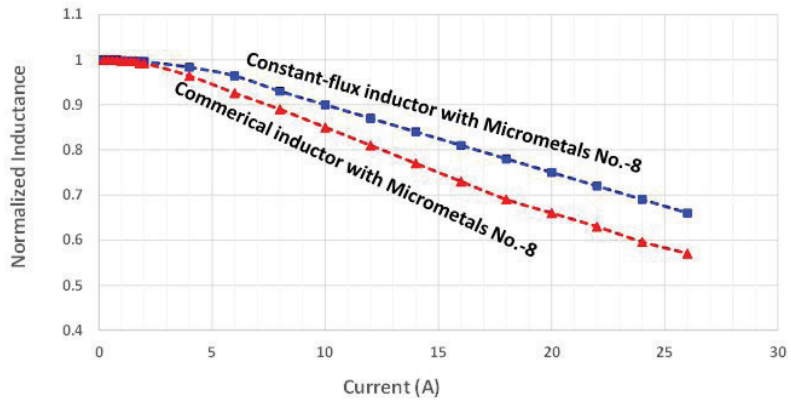


Fig. 2. Comparisons of normalized inductance under different current excitation with Micrometals Mix No. -8 material for commercial inductor and constant-flux in-ductor.

Gap Design for Nonlinear Ferrite Cores to Maximize Inductance

This paper demonstrates that in the presence of nonlinearity, inductive energy may be partially stored in the core, leading to a higher inductance. The objective is to find the optimal gap length to store the highest energy and reach the maximum inductance for a given dc current. Fig. 1(a) illustrates simulated inductance versus gap length, parametric with dc (bias) ampere-turns AT. When dc current is high, e.g., 30 A-Turns, there is one peak point on each curve. The maximum points of each curve constitute the line "Peaking AL" plotted as the solid line Fig. 1(a), which can also be plotted in the graph of AL versus AT, parametric with gap length in Fig. 1(b). For a fixed gap length, AL decreases with AT and is tangential to the curve of peaking AL. If the objective is to improve the inductance at heavy load, the "peaking AL" should be employed. The design for the swinging inductor needs a series of curves of AL versus AT plotted as dash lines in Fig. 1 (b).

From the specified L and I, the load curve $AL = LI^2 / AT^2$ is plotted as the dotted curve in Fig. 2 (a). The load curve intersects the curves of maximum AL at the solution points P1, P2, and P3. Those points determine operation points for maximum inductance. From the specified nonlinear inductance, the heavy-load curve $AL = L_{min}I_{max}^2/AT^2$ and light-load curve $AL = L_{max1}I_{min}^2/AT^2$ are also plotted in Fig. 2 (b). Not all the intersection points are valid to determine effective operating statuses. Valid intersection points should satisfy $AT_{max}/AT_{min} = I_{max}/I_{min}$.

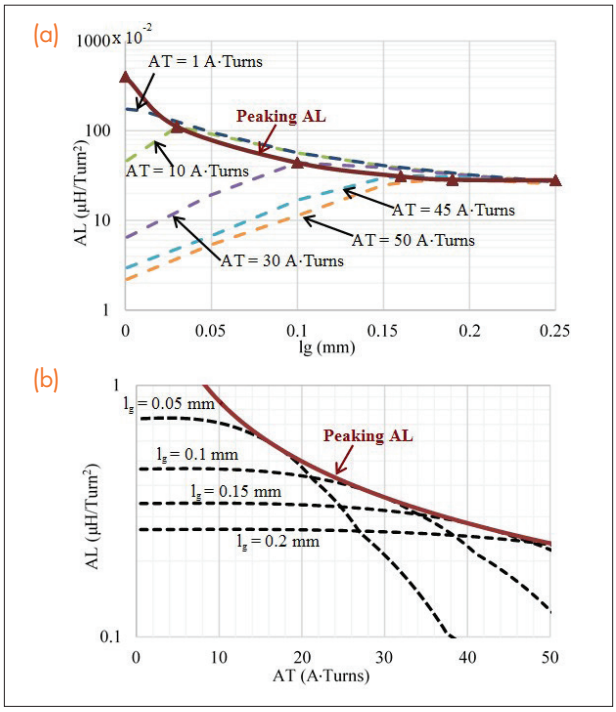


Fig. 1. (a) Simulated AL vs. gap length (l_g), parametric with AT, and (b) simulated AL vs. AT, parametric with l_g.

The only solution is the pair (M_4,M_3) since $AT_{@M3}/AT_{@M4} = 50/10 = I_{max}/I_{min}$. Both gap length and intersection points should be correct to determine the operating AT.

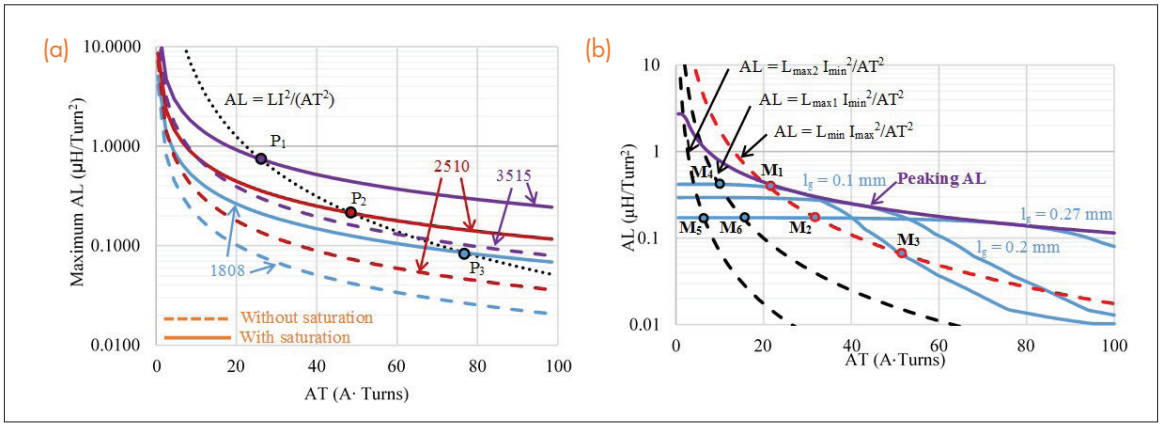


Fig. 2. (a) Maximum AL vs. AT calculated by conventional model without saturation and by model with saturation for core size 2510 and P-ferrite, intersecting $AL = LI^2/AT^2$ for L = 5 uH and I = 5 A. (b) Modeled AL vs. AT, parametric with gap length (l_g) for core size 2510 and P-ferrite, intersecting $AL = LI^2/AT^2$ for L_{max1} = 40 uH, L_{max2} = 7 uH, L_{min} = 7 uH, I_{min} = 1 A, and I_{max} = 5 A.

Compressive-Post Packaging of Double-Sided Die

A double-sided module exhibits electrical and thermal characteristics that are superior to thos of a wire-bonded counterpart. Such structure, however, induces more than twice the thermo-mechanical stress in a single-layer structure. Compressive posts have been developed and integrated into the double-sided module to reduce the stress to a level acceptable by silicon dice. For a 14 mm x 21 mm module carrying a 6.6 mm x 6.6 mm die, a finite-element simulation suggested an optimal design having four posts located 1 mm from the die; the z-direction stress at the chip was reduced from 17 MPa to 0.6 MPa.

For the 6.6 mm x 6.6 mm die studied, the optimal arrangement would place four posts symmetrically around the chip, each post at a distance between 0.75 mm and 1 mm from the chip's edges. The bonded chips no longer detached, and the module fully functioned after being sandwiched between a DBC substrate and a copper lead frame. The Von-Mises plastic strain at the die-attach layer was reduced to 87.69% of the strain without compressive posts, implying enhanced fatigue for the lifetime of the joint.

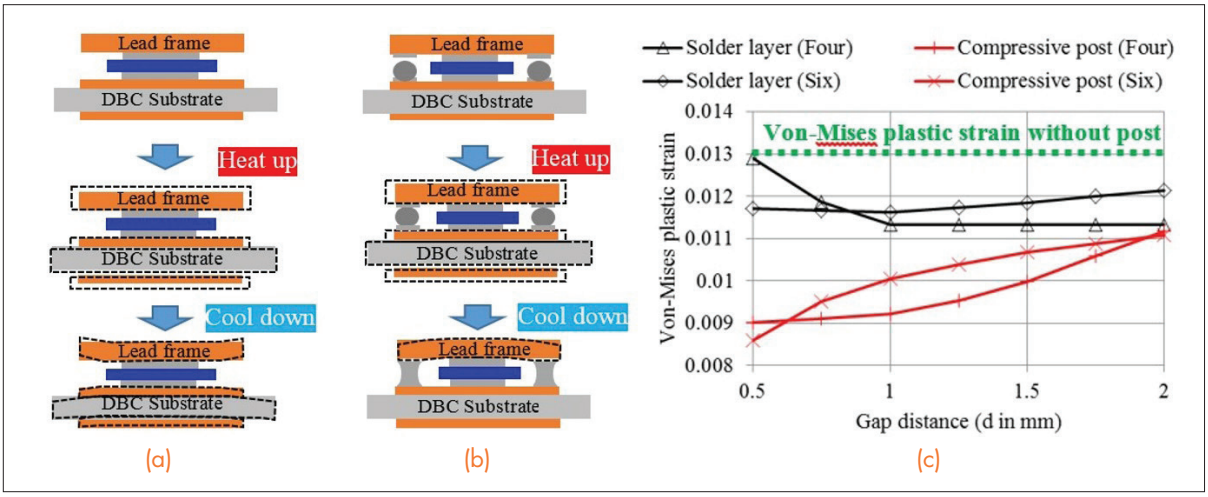


Fig. 1. Deformation (dashed line) in double-sided module (a) without and (b) with compressive posts; (c) simulated Von-Mises plastic strains at the top solder layer and compressive post.

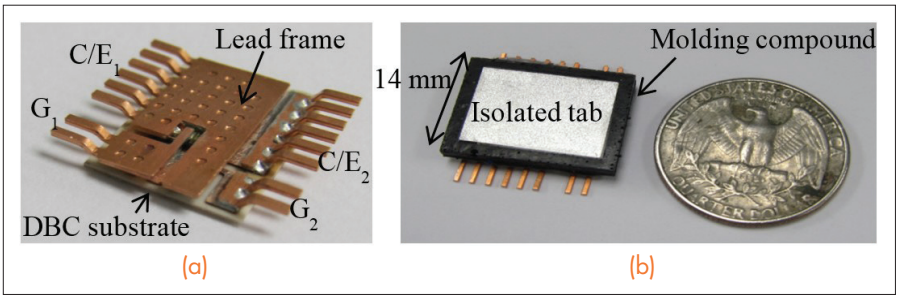


Fig. 2. Developed double-sided module with compressive posts (a) before and (b) after encapsulation.

DBC Switch Module for Management of Temperature and Noise in 220W/in^3 Power Assembly

Achieving high power density is a challenge in the presence of stringent specifications on temperature rise and switching noise. Integration of the DBC module with the PCB mother board was found to be the right approach in order to achieve a 220W/in^3 power density, a 2kW output power, and a 48.9°C junction-temperature rise. The reduced layout inductance (2.89-nH) at the source, and the negative coupling between source and drain layout inductances suppressed the turn-off noise. The prototyped dc-dc boost converter switched between 400kHz to 1MHz without self-turn-on problems.

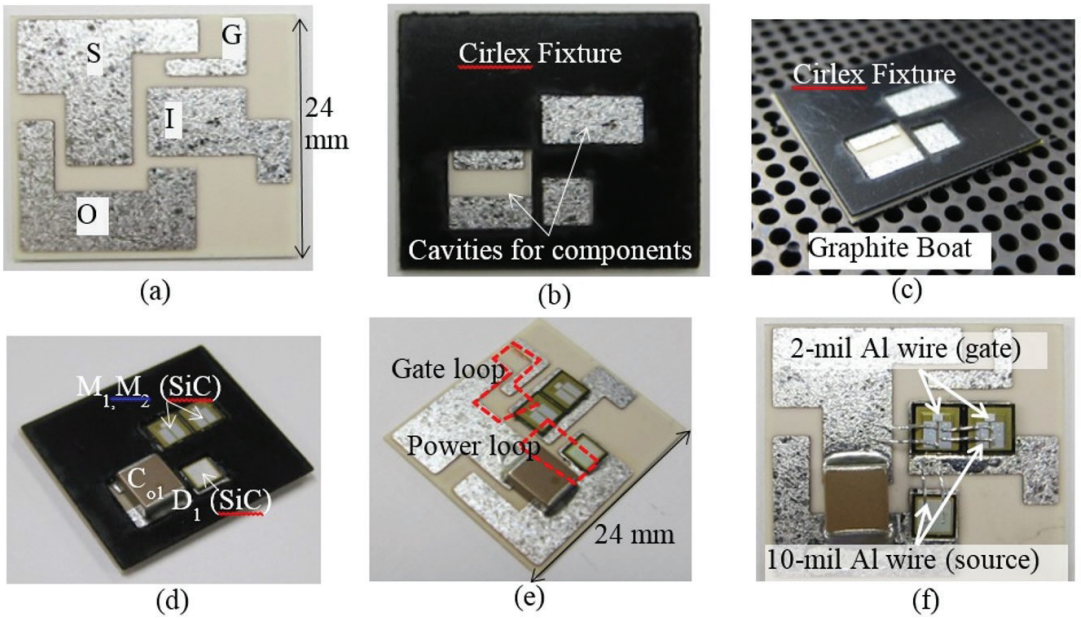


Fig. 1. Fabrication process of the DBC module: (a) chemical etching, (b) fixture design, (c) masking, (d) assembly, (e) vacuum reflow, and (f) wire-bonding.

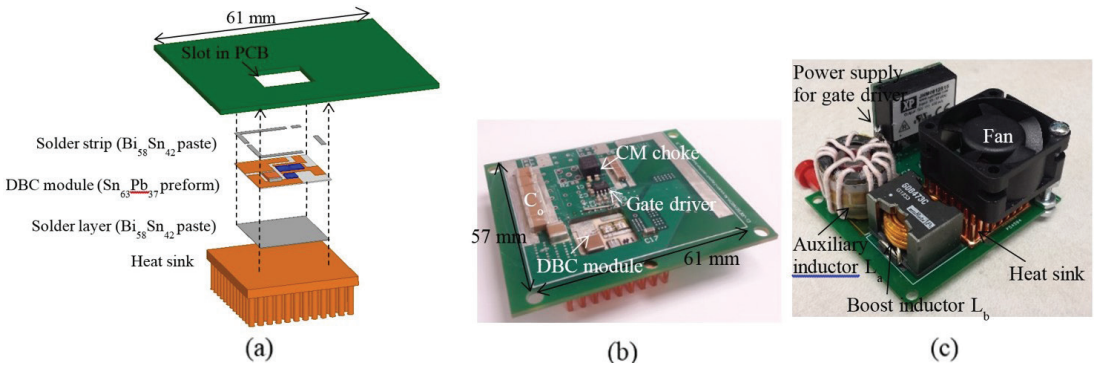


Fig. 2. (a) Assembly of packaged DBC substrate with PCB and heat sink. (b) Top side of the PCB mother board with the switch module integrated. (c) Bottom side of the mother board with magnetic and cooling components.

Loss Minimization for Coupled Inductors with Significant AC Flux

In this paper, a design methodology (Kgac) for coupled inductors (and one-winding inductor) with dominant core loss is described to identify the core volume that yields the lowest total loss. The excitation frequency is assumed as sufficiently low so that eddy-current effects in the winding can be neglected. Compared to conventional methods, the core loss density of the coupled inductor designed by the Kgac method can be 9.3 times smaller with the same core volume, which is demonstrated for coupled inductors of a 30W flyback converter switched at 200kHz. The total loss of the coupled inductors has also been evaluated by experiments, which is matched with the theoretical analysis.

The procedure of core selection is demonstrated for the coupled inductors shown in Fig. 1(a). The definition of mean length per turn (MLT), window area (W_A), effective length (l_e), and effective area A_c for the toroid core used in the analysis are shown in Fig. 1(b). The Kgac method is an extension of the Kg method. With the "Kgac" method, a designer can select the magnetic flux density based on the thermal constraint. An empirical relationship among the effective area (A_c), the mean length per turn (MLT), the window area (W_A), and the volume (V_e) is suggested for the derivation of the core volume that minimizes the total loss. Under the constraints of ac flux density, inductance and window area utilization, the optimal core volume is derived by

$$V_e = \left(\frac{K_1 a_1 a_2}{K_2}\right)^{\frac{1}{a_2+1}}$$

where

$$K_1 = \left[\frac{i_{dc}^2}{n^2 D'^2} + \frac{1}{12}\left(\frac{V_{in} D}{L_m f}\right)^2\right]\frac{\rho}{K_u}\left(\frac{V_{in} D}{2 f \Delta B}\right)^2\left(\sqrt{D}+\sqrt{D'}\right)^2$$

$$K_2 = K_{fe} f^{\alpha} (\Delta B)^{\beta}$$

a_1, and a_2 are constants depending on the core shape.

Table I shows the comparison of losses and volumes for Kgac, Ap and Kg methods based on the 30W flyback converter at 200kHz. If core loss is neglected in the Ap and Kg methods, the core-loss density of the Ap and Kg methods are 9.3 times as high when compared to the Kgac method, which means the temperature of the core will be unacceptably high at the normal cooling condition. The measurement results are consistent with the theoretical calculations shown in Fig. 2.

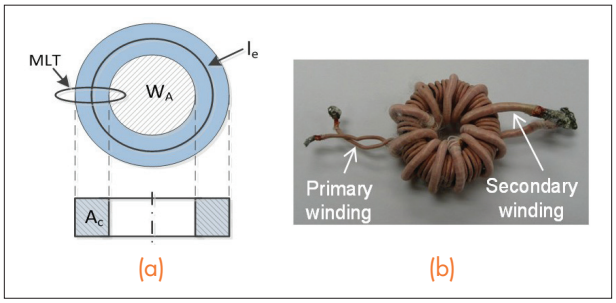


Fig. 1 (a) Prototype of coupled inductors and (b) definition of MLT, W_A, L_e, and A_c for toroid core used in the analysis.

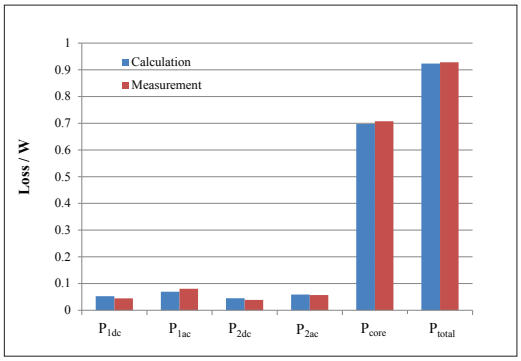


Fig. 2. Comparison of losses between calculation and measurement.

	Kgac method	Ap method (Normalized)		Kg method (Normalized)	
ΔB	1	2.74	1	3.05	1
Core loss density	1	7.5	1.04	9.33	1.02
Volume V_e	1	1	1.19	0.45	1.48
Core loss P_{core}	1	7.5	1.24	4.22	1.51
Winding loss $P_{winding}$	1	0.13	0.7	0.44	0.46
Total loss P_{total}	1	5.7	1.11	3.3	1.25

Table I. Comparison of losses and volumes for Kgac, Ap and Kg methods.

Package Influence on Switching Performance of SiC Modules

The SiC device parameter variations cause current and power unbalances during device parallel operation in a module. The unbalances introduce additional power losses, temperature rise, localized overcurrent, and even failure of the device. Since the package parasitics impact the performance of the module, and the number of parasitics in the module is usually large (more than 50), an accurate model should be built in order to analyze the performance by simulation. An internal view of a commercial module is shown in Fig. 1. Conventionally, there are two ways to model the parasitics. The first is to model the parasitic as a dc resistance in series

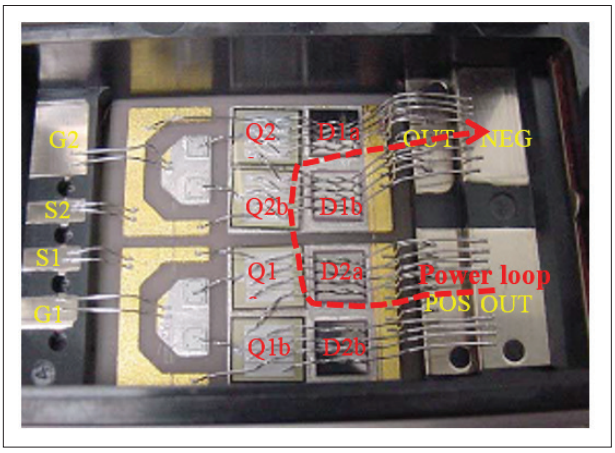


Fig. 1. Internal view of 1.2kV 100A SiC module showing two 80A SiC MOSFETs and two 50A SiC JBS diode per switch

with the ac inductance; another way is to model the parasitic as an ac resistance in series with the ac inductance. In addition, the simulation frequency is usually set the same as the switching frequency. In this paper, the model is changed to be an ac resistance parallel with the combination of a dc resistance in series with the ac inductance. This model should present accurate dynamics for both low frequency and high frequency. Choosing the simulation frequency is also further discussed in the paper. The maximum element length of the mesh should be set to no larger than the skin depth of the simulated conductor. A tradeoff has to be made between the simulation time and the switching frequency for practical use. Simulation results using the conventional modeling method and the proposed modeling method are compared with the experimental results. The proposed modeling method agrees with the experimental results. Once the accurate modeling method is concluded, the parasitics of five 1200V SiC commercial modules are extracted to build the simulation schematic in LTspice. Fig. 2 shows three different half-bridge configurations. The same MOSFET and diode dice are used to fairly evaluate the switching performance of each module affected mainly by the package parasitics. The layout characteristics of each module are summarized and compared. Among them, the largest gate inductance is 101nH. Current unbalance and self-turn-on issues are noticed and analyzed by looking into the internal switching performance.

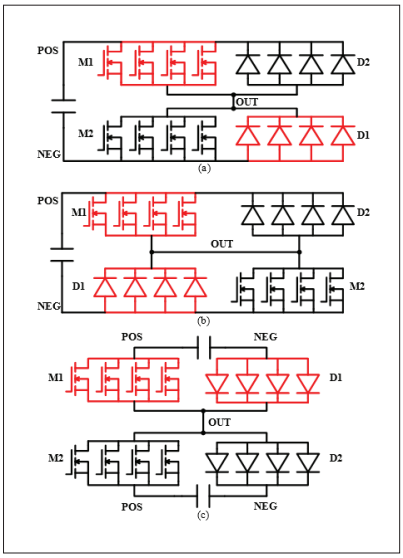


Fig. 2. Different half-bridge configurations

Design and Implementation of Integrated Common Mode Capacitors for SiC-JFET Inverters

This paper discusses the issue of electromagnetic interference (EMI) in SiC-JFET inverter power modules, and proposes a solution to limit conducted emissions at high frequencies. SiC-JFET inverters can achieve very fast switching, thereby reducing commutation losses, at the cost of a high level of EMI. To limit conducted EMI emissions, this paper proposes to integrate small-value common-mode (CM) capacitors directly into the power module. High-frequency noise, which is usually difficult to filter, is then contained within the module, thus keeping it far from the external network. This approach is in line with the current trend toward the integration of various functions (such as protection, sensors or drivers) around power devices in modern power modules. To demonstrate this concept, the resulting CM noise was investigated, and compared with a standard configuration. Simulations were used to design the integrated capacitors, and measurements were carried out on an experimental SiC-JFET half-bridge structure. A significant reduction was achieved in the experimentally observed CM conducted emissions, with a very minor influence on the switching waveforms, losses, and overall size of the system. The benefits and limitations of this design are discussed in the case of mid-power range inverters for aircraft applications.

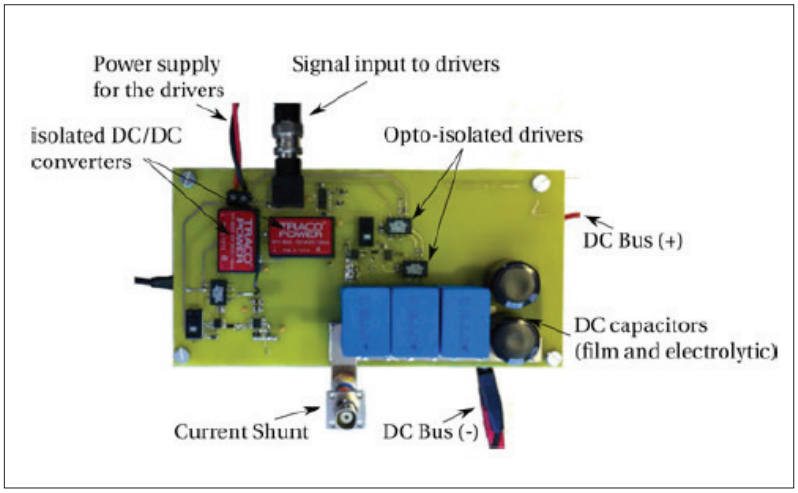


Fig. 1. SiC-JFET power module test board. The power module terminals were soldered directly onto the bottom layer of this board.

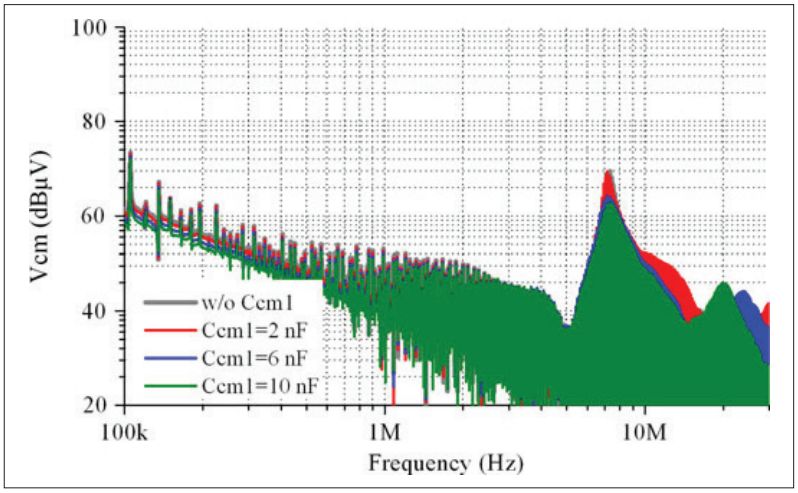


Fig. 2. Simulated EMI spectra for different values of the integrated CM capacitors.

A 50 kW SiC Three-Phase AC-DC Converter Design for High Temperature Operation

This work seeks to demonstrate the feasibility of developing a complete high-temperature, high-power-density, 50-kW bidirectional three-phase ac-dc power converter unit for operation in 200 °C environments. The unit, which utilizes custom SiC power modules, will enable high power generation, increased efficiency, and compact size suitable for embedded generators in more electric aircraft applications. This endeavor required the development of high-temperature pack-aging for both active and passive devices, cooling techniques, and EMI tolerant capability.

One of the core contributions of this work was the design and development of a completely high-temperature (200 °C), high-power (1200 V, ≥ 100 A), phase-leg power module utilizing SiC MOSFETs and SiC Schottky diodes. The power module was fabricated in the CPES packaging lab, and was fully characterized and tested up to 200 °C.

The system-level work includes the integration of the high-temperature power modules, gate drivers, sensors, and protection. In the design and implementation of this system, surveys on high temperature passive and active components, such as capacitors for the dc-link, magnetics for the EMI filter, and SOI technologies for the control electronics, were carried out. Noise coupling was minimized through the use of an improved laminated bus bar design and power module layout structure, implementing chokes and shields, and introducing redundancy protection.

Double-pulse tests (DPTs) were performed on the final high-temperature, 50-kW unit at 200 °C ambient, 540 V, and 100 A. Fig. 2 shows the turn on and turn off switching waveforms from this testing. The ringing in the waveforms is from the measurements, and is not actually seen on the modules. Due to a lack of high temperature probes, long high temperature wire was extended from the module (inside the thermal chamber) to outside of the high temperature envi-ronment where the probes could be connected. This long wire added parasitics and noise to the measurements. Overall, these tests revealed good performance of the unit at high-temperature, even after soaking for more than an hour.

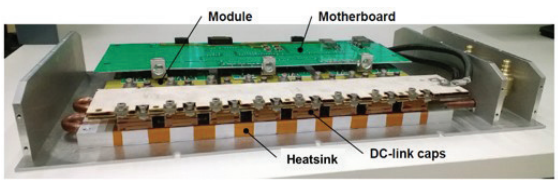
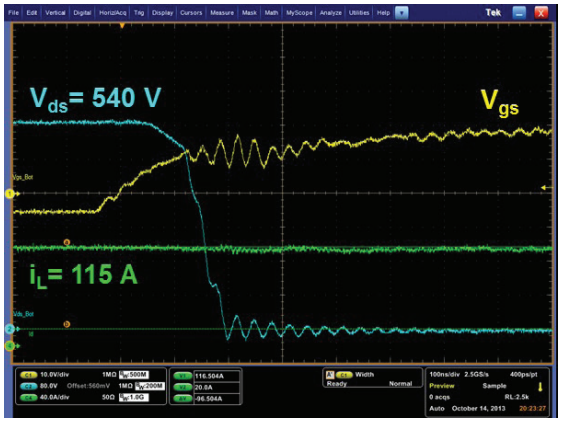


Fig. 1. High temperature 50 kW converter.



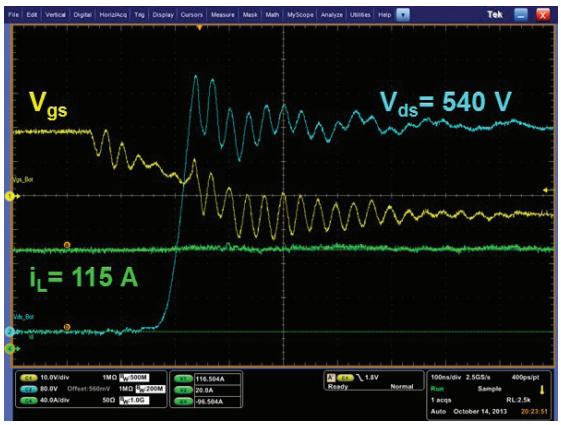


Fig. 2. Converter DPT waveforms at 200 °C, 540 V, and 100 A.

A 1200V, 60A SiC MOSFET Multichip Phase-Leg Module for High-Temperature, High-Frequency Applications

In this paper, a high-temperature, high-frequency, wire-bond-based multichip phase-leg module was designed, fabricated, and fully tested. Using paralleled Silicon Carbide (SiC) MOSFETs, the module was rated at 1200V and 60A, and was designed for aircraft applications using a 25kW three-phase inverter operating at a switching frequency of 70kHz in a harsh environment of up to 200ºC,. To this end, the temperature-dependent characteristics of the SiC MOSFET were first evaluated. The results demonstrated the superiority of the SiC MOSFET in both static and switching performances as compared to the Si devices, all the while revealing the design tradeoff in terms of the device's gate oxide stability. Various high-temperature packaging materials were then extensively surveyed and carefully selected for the module to sustain the harsh environment. The electrical layout of the module was also optimized using a modeling and simulation approach, in order to minimize the device parasitic ringing during high-speed switching. Finally, the static and switching performances of the fabricated module were tested, and the 200ºC continuous operation of the SiC MOSFETs was verified.

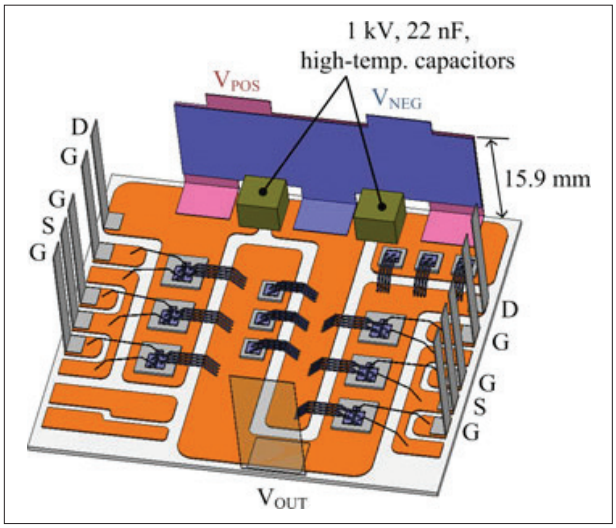


Fig. 1. 3-D package model of the power module.

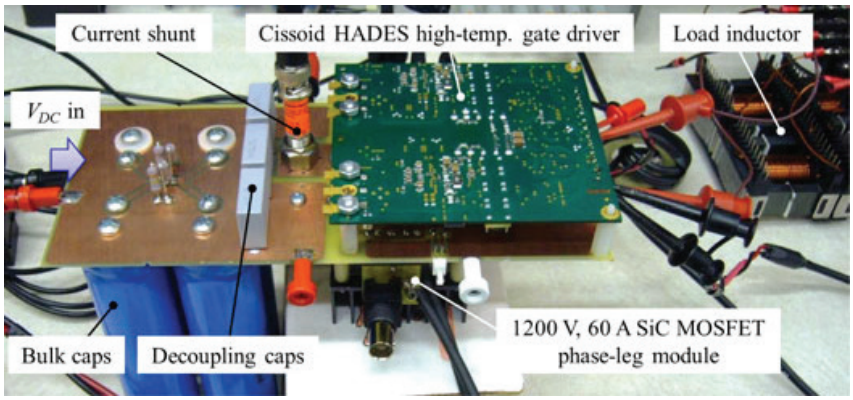


Fig. 2. Switching test setup for the module.

Sensitivity Analysis of a Modular Multilevel Converter

The modular multilevel converter (MMC), shown in Fig. 1, is one of the next generation high/medium-voltage converters intended to achieve a high-power conversion without line-frequency transformers. While the MMC has the advantages of easy assembly and flexible converter design, it still requires a reliable design like any other system. The design criteria in this case are a function of a large number of variables, due to the large number of submodules that are usually used in MMCs. Most papers so far have focused on the modeling and control of the MMC, but not on the design. This paper employs a sensitivity analysis technique to develop a detailed switching model to design the most compact power converter possible with the minimum required safety margins.

The many design criteria in an MMC include output power and line-to-line voltage, maximum temperature, peak value of submodule voltage, and power quality. These design criteria are selected based on the intended application. Each of these criteria is a function of a large number of variables, which require equivalent and simplified models. There is a distinction between models used to understand a law and models used to predict the behavior of a system given a presumably understood law. The latter requires more precision; the model used for designing a converter falls within this group.

This paper uses the sensitivity analysis technique to determine the main variables required for consideration in a specific design criterion. The uncertainties associated with these main variables can be propagated through the model via nondeterministic simulations to calculate the required safety margins in the design. Using this technique, one can develop a precise model from a design standpoint, with the minimum number of variables required, in order to have a realistic design without requiring large safety margins.

In the first section, the main concept of the sensitivity analysis is described and the most popular methods are discussed. In the second section, the peak voltage of a power cell and the resonance behavior of a circulating current are selected as the design criteria, which are generally used to select the minimum required capacitance and arm inductance. Sensitivity analysis is performed at three different levels, based on the hierarchical structure of the MMC, in order to develop a model to accurately predict the effects of parametric uncertainties on these design criteria with a minimum number of uncertain variables.

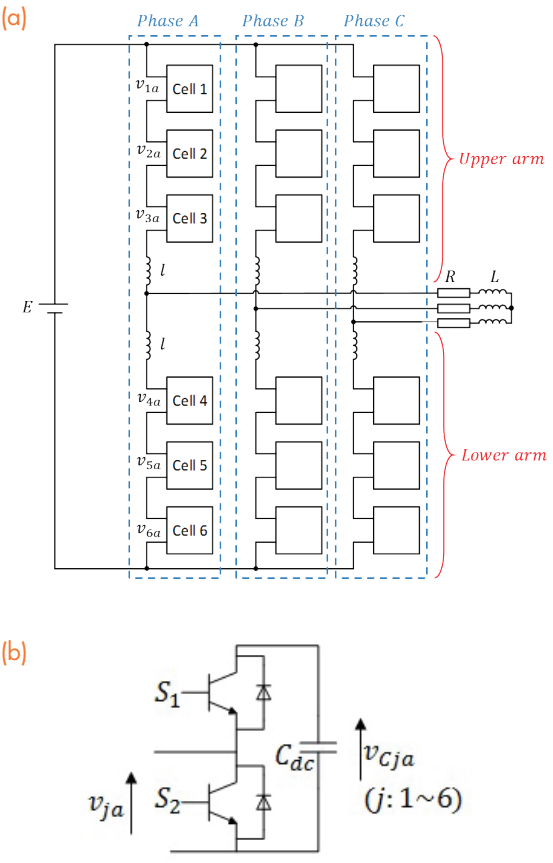


Fig. 1. Circuit configuration of a modular multilevel inverter: (a) three phase MMC, and (b) Single power cell.

Stress Analysis and Minimization for a Modular Multilevel Converter to enhance the Reliability of the Converter

The Modular Multilevel Converter (MMC) is becoming a well-known topology for use in high- and medium-voltage industrial applications. In Fig. 1, each sub-module structure of the Modular Multilevel Converter (MMC) topology is demonstrated. To achieve high-reliability power converters, the methodology of reliability-oriented design for the modular converters is summarized in Fig. 2.

In step F, as shown in Fig. 2, stress control and minimization are applied to the power module to further improve its reliability and complete its electrothermal design. Here it specifically shows how the amplitude of the converter (phase-leg) circulating current, and the switching frequency of the power modules influence the reliability of the latter. This figure also shows that reducing the circulating current by using an appropriate control system can adversely affect the two components of the IGBT failure rate, namely the thermal and cosmic-ray dependent failures, which also affects the capacitor failure rate that was successfully reduced. The switching frequency range is investigated to ensure the compliance of the grid THD codes, where the switching frequency reduction also adversely affected the two components of the IGBT failure rate, and was shown to increase the failure rate of capacitors. Similar to previous analyses, the Markov Chain models were used extensively (step D, as shown in Fig. 2) to aid in the investigation and comparison of alternative circulating current controllers and the switching frequency selection, seeking the best possible solution.

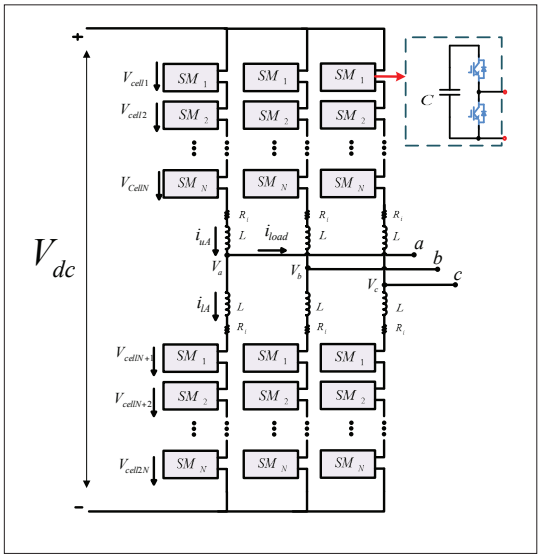


Fig. 1. Modular Multilevel Converter topology with each sub-module structure.

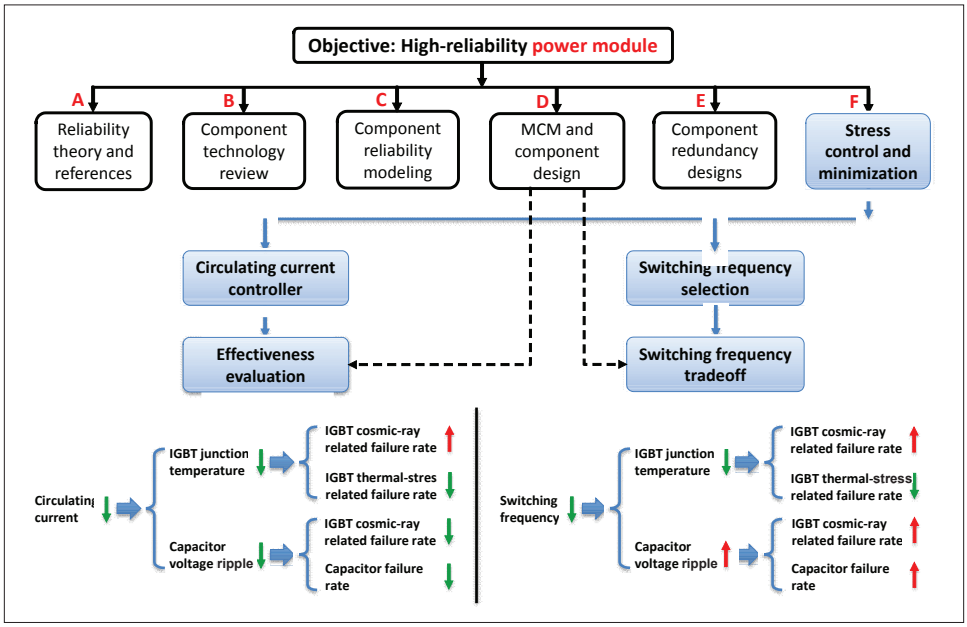


Fig. 2. Stress control and minimization for MMC.

Reliability-Oriented Switching Frequency Analysis for Modular Multilevel Converter

Fig. 1 shows the Modular Multilevel Converter (MMC) topology with each power module structure. In order to reduce the switching loss of the converter in high- and medium-voltage applications, it is preferable to operate at a low switching frequency. The consequence of this is an increase in the circulating current magnitude and harmonic distortion. In Fig. 2, the switching frequency effect on the arm current and the voltage ripple of the capacitor are shown. As seen in this plot, the switching ripple of the arm current and the capacitor voltage increase significantly at a lower switching frequency. Therefore, choosing the switching frequency for the MMC is effectively a tradeoff between the IGBT power loss and the maximum allowable voltage, and the current ripple through the module capacitor and the phase arm inductor. To obtain the optimum switching frequency for the MMC, the reliability of the converter is selected as the objective function.

Fig. 3 shows a plot of the probability to fail over time for the MMC operating at a switching frequency of 300 Hz, 420Hz and 540Hz with circulating current supressor controller (CCSC). The 420Hz case achieves the best reliability performance, although only a minor overall impact is determined. Nonetheless, this result points out that although fewer semiconductor losses are incurred when operating at lower switching frequencies, the increase of the voltage ripple across the capacitors and IGBTs can detrimentally affect the reliability of the converter. This illustrates one of the key tradeoffs when designing the MMC.

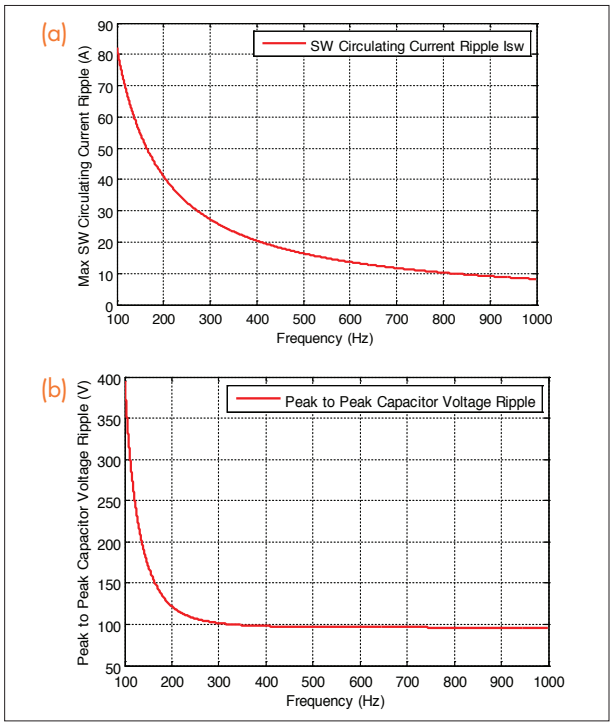


Fig. 2. With respect to frequency, (a) switching ripple of the arm current and (b) capacitor voltage.

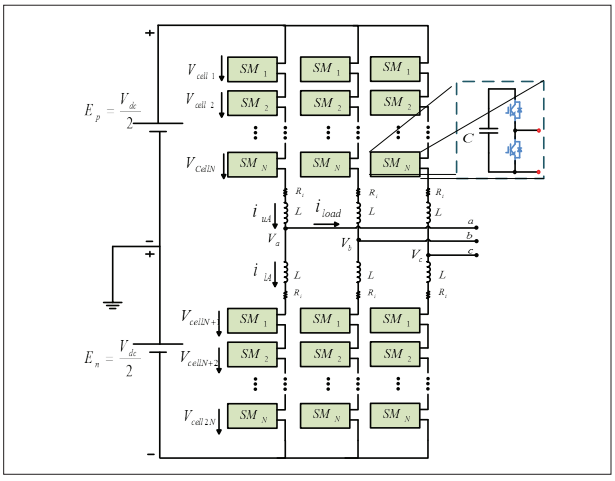


Fig.1 Modular Multilevel Converter (MMC) topology with each power module structure.

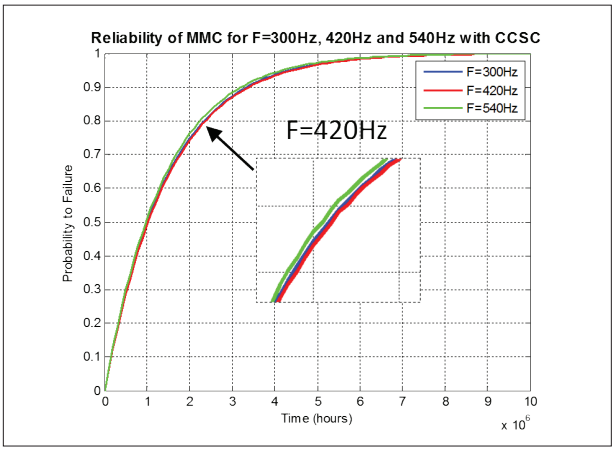


Fig.3 Markov reliability model of the MMC with circulating current suppressing controller at different frequencies.

DC Fault Ride-Through Capability of Modular Multilevel Converters

Modular Multilevel Converters (MMC) become attractive topology in high- and medium-voltage applications because of their interesting features such as modularity, scalability and reliability, excellent harmonic performance, transformer-less structure, distributed location of capacitive energy storages, filter-less Configuration, high resulting switching frequency and so on. One of the main issues surrounding the conventional MMC half-bridge power cell structure is the inability to block current during dc side faults causing the conventional MMC to suffer from poor dc fault performance, which requires fast circuit breakers to disconnect the converter by opening from the ac side.

Fig.1 (a) shows the conventional MMC with half bridge modules during the dc fault. The dc fault occurrence analysis is carried out in the MMC with half bridge power cells and the uncontrollable current path during the dc terminal short circuit. Fig. 1 (b) depicts the MMC as it contains full-bridge power cells during the dc short circuit. To have a sequential and coherent analysis, the operation of the MMC with full-bridge modules, should be demonstrated during the short circuit of the dc link and then, the dc-fault-blocking capability of the MMC with full-bridge power cells should be presented.

The recently published Alternate Arm Converter (AAC), which is from the family of the hybrid multilevel voltage source converter, is shown during the dc fault in Fig. 1. (c). AAC has nearly the same number of semiconductor devices in its topology, and it requires less arm-inductor and power cell capacitor size. The main benefit of the AAC is the excellent performance and ride-through capability in a local terminal-to-terminal short circuit of the dc-link and three different possible modes of STATCOM operation during the dc fault. In this paper, the dc-fault blocking of the AAC will mainly be considered for medium-voltage dc applications and the dc-fault current during the fault will be analyzed.

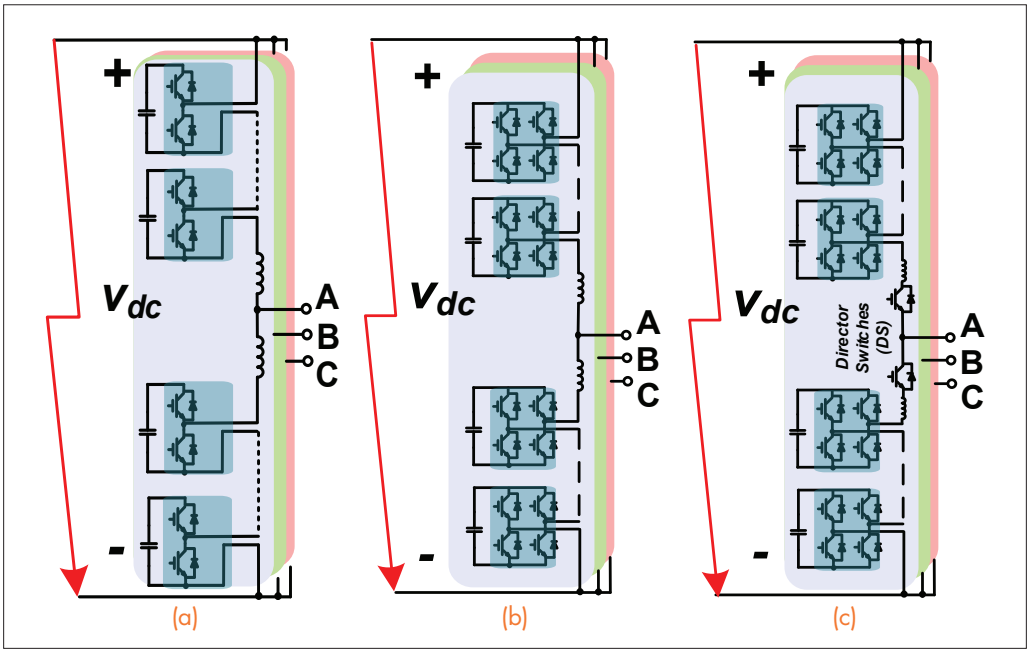


Fig. 1. dc Fault Occurrence in (a) Modular Multilevel Converter (MMC) with half-bridge power cells (b) MMC with full-bridge power cells, and (c) Alternate Arm Converter (AAC).

Compensation of DC-Link Oscillation in Single-Phase to Single-Phase VSC/CSC and Power Density Comparison

This paper proposes a technique to reduce low frequency dc-link energy oscillation caused by the pulsating single-phase energy flow in a single-phase to single-phase Voltage Source Converter (VSC) and Current Source Converter (CSC), which operate connected to the grid. That pulsating energy is the main reason for the increase in size of the passive components and power losses in the converter. Pulsation reduction is achieved by incorporating two auxiliary active switches and one passive energy storage element to the rectifier and inverter side. Additionally, this paper presents a comparison of these converters with regard to their efficiency and power density. A detailed control strategy is presented, and a simulation is provided, along with experimental results (See Fig. 1 and Fig. 2), in order to validate the theoretical approach.

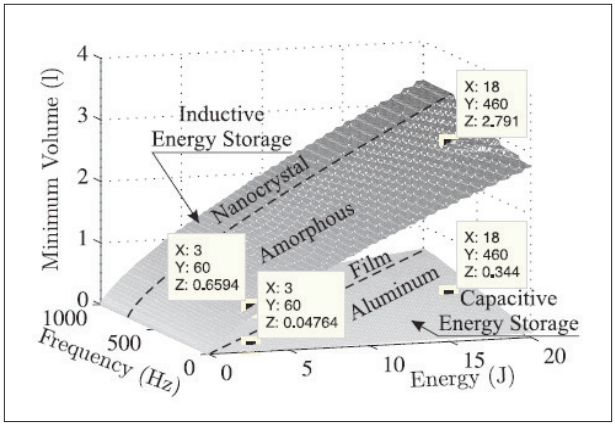


Fig. 1. Inductive and capacitive energy storage comparison results.

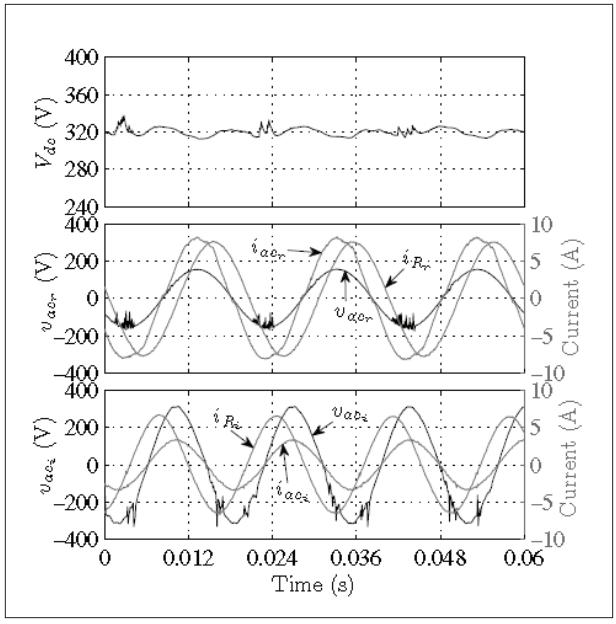


Fig. 2. Experimental results for the VSC, where the top figure is the dc voltage, the middle figure is for the ac rectifier side, and the bottom figure is for the ac inverter side.

Hybrid Modulation for Neutral Point Voltage Reduction in DC-Fed Three-Level Motor Drive Systems

In a dc-fed motor drive system, a three-level VSI, as shown in Fig. 1, can provide better performance on noise reduction and system efficiency. However, it also introduces neutral point voltage control problems. In the conventional nearest three space vector (NTSV) modulation method, there are fundamental frequency related harmonics on the dc voltage and large dc capacitor that is needed during the startup process when the motor speed is low. In order to reduce the dc-link capacitors and improve system power density, a hybrid modulation method is proposed to limit the neutral point (NP) voltage ripple during the startup process for three-level motor drive systems.

In NPC 3L inverters, since each phase leg has three output voltage levels: $+V_{dc}/2$ (P), 0 (O), $-V_{dc}/2$ (N), there are a total of 27 switching states and 18 output voltage vectors for the three phases, as shown in Fig. 2. There have been many publications about the modulation methods for NPC 3L inverters. Different optimization goals, such as minimum loss or harmonic distortion can be achieved by using the redundant switching states. The neutral point voltage calculation model is presented to study the large NP voltage ripple for three-level modulation during the startup process. Moreover, the possible overvoltage issue on the semiconductors, considering the different switching speed of the devices for two-level modulation in three-level NPC converters, is analyzed in detail. A zero neutral point voltage ripple modulation (ZNPVR) method is proposed to limit the NP voltage ripple and avoid overvoltage on the devices when the output fundamental frequency is low. When the output fundamental frequency is high, the modulation can smoothly transit to normal NTSV modulation for lower ripple and higher efficiency. Fig. 3 shows the modulation method transition from the ZNPVR method to the NTSV method, which shows the effectiveness of the ZNPVR modulation method.

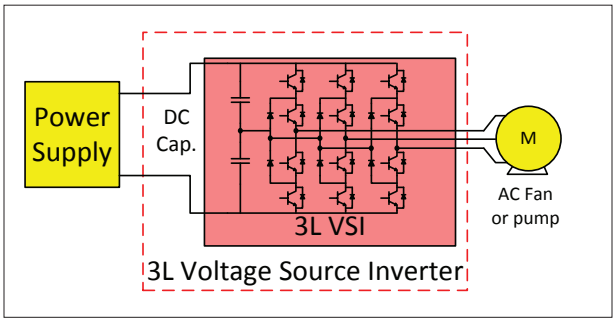


Fig. 1. 3L VSI motor drive system with fan load.

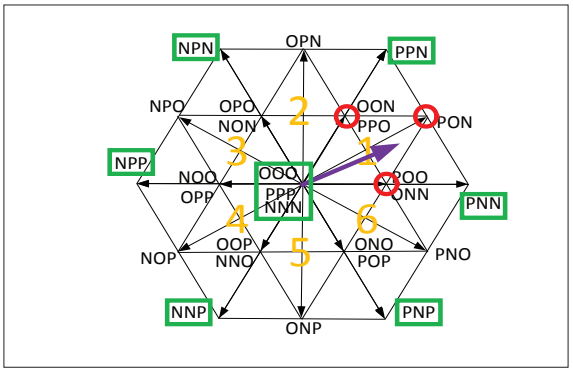


Fig. 2: Switching states of an NPC inverter: red states the switching states in NTSV modualtion, and green states are used in ZNPVR Modulation.

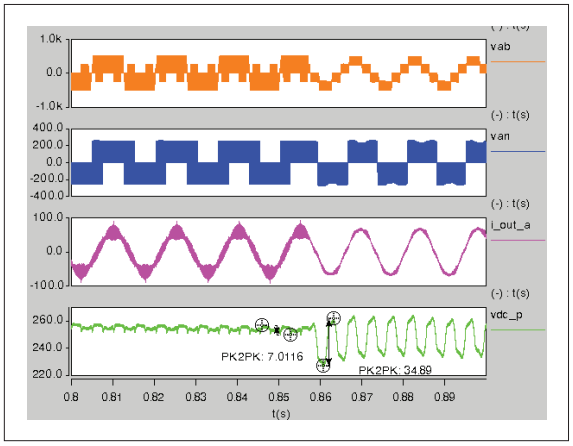


Fig. 3. Time domain simulation results: line to line voltage (V_{ab}): orange; phase voltage (V_{an}):blue; output current (I_{out}):pink; NP voltage ripple (V_{np}):green.

Discontinuous Pulse Width Modulation Methods with Neutral Point Voltage Balancing For Three-Phase Vienna Rectifiers

PWM converters have made a significant contribution when it comes to achieving energy conservation, and improving system performance and productivity in many applications, such as transportation systems and renewable energy systems. Vienna-type rectifiers as shown in Fig. 1 have been widely used for their higher reliability and more important, their potential advantage to achieve higher efficiency. With the use of a SiC diode, the reverse recovery loss from diodes in Vienna rectifiers can be nearly eliminated, which further makes the Vienna rectifier a promising topology in achieving high efficiency.

In two-level three-phase PWM converters, discontinuous modulation methods are widely used to reduce the switching loss by maintaining one phase leg unswitched during each switching period. A similar modulation technique can also be applied to Vienna rectifiers. This research presents two DPWM methods for three-phase Vienna rectifiers. One for switching loss minimization, as shown in Fig. 3(b) and one for switching loss reduction with the neutral point voltage controllability, as shown in Fig. 3(c). The detailed implementation of the two modulation methods are presented. System performance with the proposed two modulation methods are compared with the commonly used discontinuous PWM modulation method as shown in Fig. 3(a), in reference to semiconductor loss and neutral point voltage. The analysis is verified through both simulation and experimental verification based on a 3kW Vienna rectifier with 99.08% efficiency at nominal load.

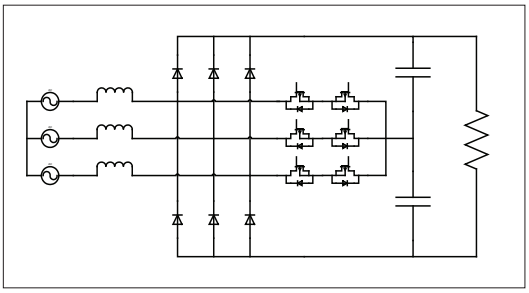


Fig. 1. Three-phase Vienna rectifier.

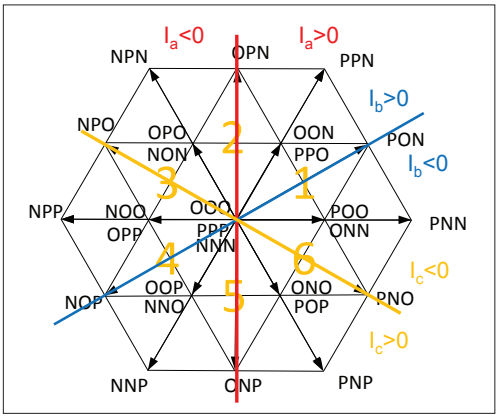


Fig. 2. Switching states in Vienna rectifier with unified power factor.

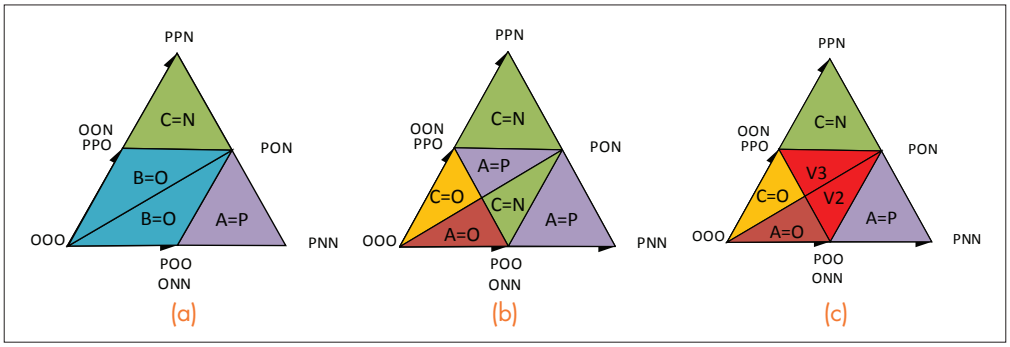


Fig. 3. Different Discontinuous PWM Methods. (a) Method 1; (b) Method 2; and (c) Method 3.

Modular Multilevel Alternate-Arm Converter (AAC): Modeling, Design, and Control

This paper will discuss the operation of the Alternative Arm Converter (AAC), and investigate the workings of the AAC mainly under RL loads. By examining the converter, it becomes obvious that the operation of the director switches (DS) under reactive load power will be an issue since the switches will be turned off in the non-zero current. In this study, the operation of the DS in the AAC to achieve ZCS will be investigated, and as a consequence the design procedure of the arm inductor as an imperative component of the AAC, which provides ZCS operation of the DS, will be provided. Next, the mathematical analysis will be performed to calculate the capacitor voltage ripple waveform in different load power factors. The waveforms are then compared with the simulation result. At the end, a design and switching losses comparison sample case study is done between the AAC and the MMC half-bridge to achieve a better understanding of the pros of the AAC, as well as its drawbacks.

In Fig. 1, the hard switching vs. soft switching of the DS in the AAC is shown. It can be seen from Fig. 1, by using the overlap time between the upper and lower arm director switches, that the current through the resonant LC circuit can go to a negative value and the ZCS can be achieved. During the overlap time, all the cell's capacitors will be inserted positively to the arm, and the difference voltage of the dc link and arm voltage, which is negative will be put over the arm inductor. This voltage makes the current through the arm become negative and provides a ZCS condition for the DS.

The simulation analysis has been done through Simulink/Matlab to verify the proposed scheme for ZCS, and the analytical analysis of the capacitor voltage ripple, as well as the operation of the AAC in the RL loads. The simulation has been performed for the load power factor φ=37° resistive and the inductive load RL. The upper and lower arm currents waveforms as well as the upper and lower arm capacitor voltage, the phase and DC line current is shown in Fig. 2. The results show that the AAC, despite having a higher number of switches, will have smallerswitching power losses. This is mainly due to the lack of circulating current, the alternating of the load power, and also the use of the demonstrated ZCS scheme for the director switches.

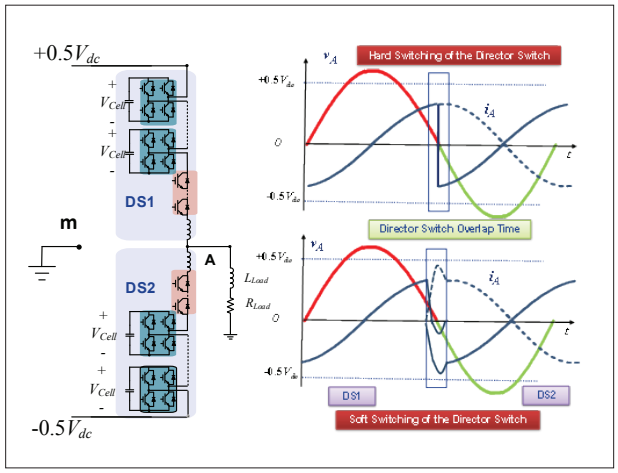


Fig. 1. Zero-Current Switching Realization in AAC vs. Hard Switching.

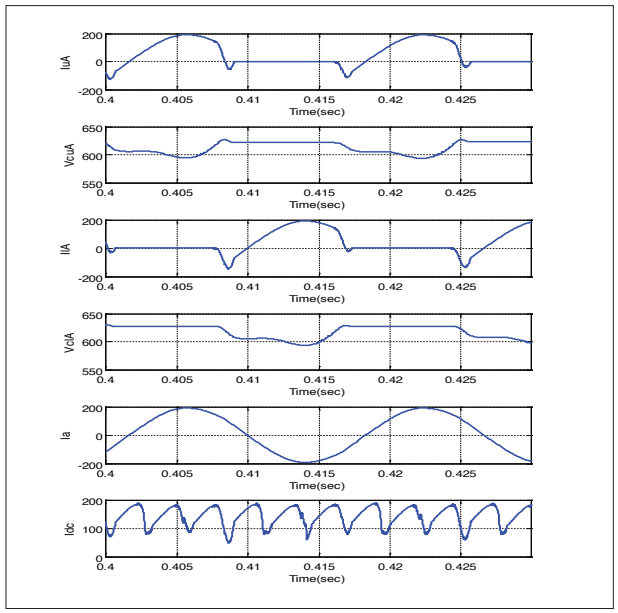


Fig. 2. Arm, DC and Phase Current and cap voltages of AAC with ZCS of DS for load power factor φ=37°.

Resistance Compression T-Networks with Active-Switch Compensation in the Input Branch for Constant-Frequency Resonant Power Conversion

Performance of resonant power converters is often plagued by wide-load variation. Resistance compression networks can reduce the variation while keeping the converters' efficiency high. A practical case of a two-port, voltage-driven, resistance compression T-network (RCN-T) is examined here (Fig. 1).

Active compensation is required in the input branch of the T-type network in order to create an effective RCN-T circuit. The compensator consists of a four-quadrant switch and a parallel capacitor (Fig. 2(a-c)). This configuration ensures ZVS turn-on of the switch and near-zero switching losses.

Depending on the voltage ratio between the input and the output of the RCN-T, three classes of circuits are possible: buck, buck-boost, and boost. Buck RCN-T is associated with the compensated LLC resonant tank in Fig. 2(a). Buck-boost functionality is obtained with the compensated LCL tank (Fig. 2(b)). Compensated LCC tank in Fig. 2(c) has boost functionality. Filtering capability of the RCN-T network is necessary to reduce the component count and cost, and to improve the simplicity of the system. Fig. 3 shows typical bode plots of the input impedance for each class of RCN. The buck class has only a limited capability to filter the higher frequency component, necessitating additional filtering to ensure proper operation at the operating frequency (Fig. 3(a)).

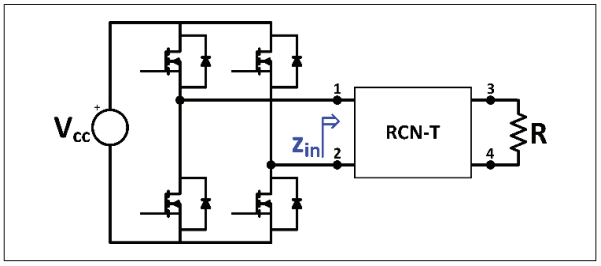


Fig. 1. Resonant inverter equipped with an RCN-T.

The buck-boost class does not have any filtering capability (Fig. 3(b)), and it is as disadvantageous as the buck class. The boost class (Fig. 3(c)), on the other hand, has intrinsic filtering capabilities. For this reason, boost topology is most attractive for the design's implementation.

The full paper includes the design procedure of the RCN-T boost system. Conduction losses of the active switch are further minimized by the properties of the boost class and compensator used, ensuring that RCN-T efficiency will be in the high 90% range.

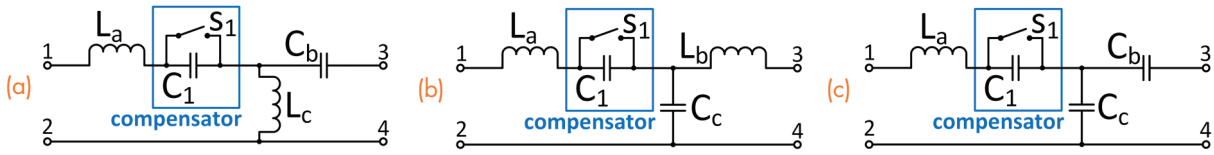


Fig 2. Capacitive compensator at the input branch of the T-networks: (a) LLC; (b) LCL; (c) LCC.

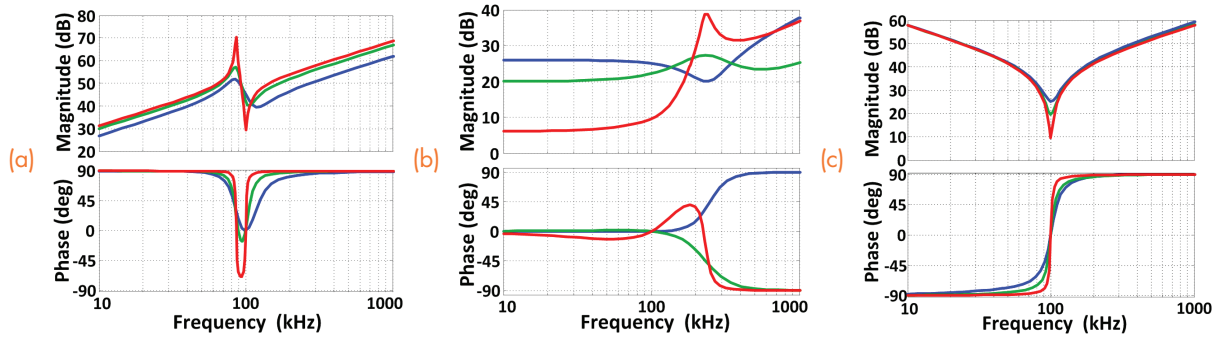


Fig 3. Typical Bode plots of the RCN-T's input impedance z_{in} for each class: (a) buck; (b) buck-boost; (c) boost.

A Unified Control for the Combined Permanent Magnet Generator and Active Rectifier System

This paper presents a unified control method for the combined permanent magnet generator (PMG) and active rectifier that can be used in autonomous power systems such as more electric aircraft requiring high power density and efficiency. With the proposed control, the system can function well without additional boost inductors and rotor position sensors. The design procedure for the control is presented, including current loops, a voltage loop, and a rotor position estimator loop. Simulation and experimental results show that both the dc-link voltage and the reactive power can be controlled effectively. A system efficiency optimization technique is proposed by selecting the permanent magnet flux linkage and determining the operating points at various load and speed conditions. The power density and efficiency of the PMG and active rectifier system are improved with the unified control.

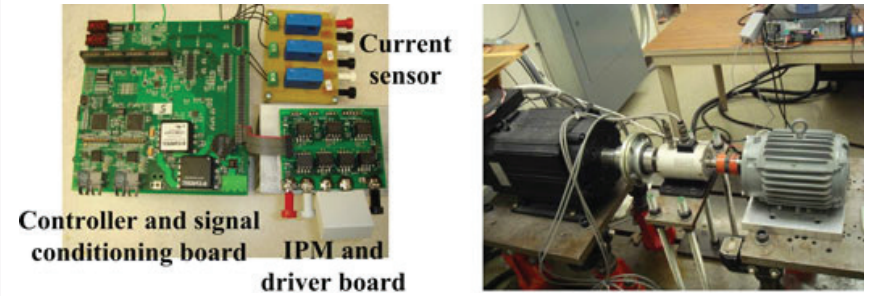


Fig. 1. Hardware setup. (a) Power stage and control unit. (b) Permanent magnet generator.

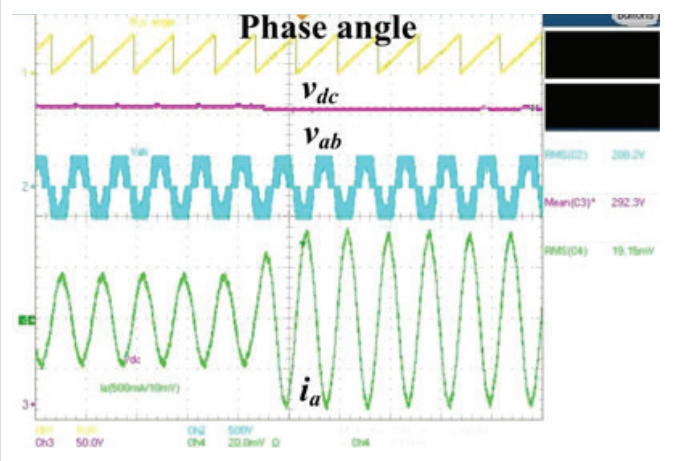


Fig. 2. Waveforms in the PMG and active front-end rectifier system after applying a load change from 200 to 400W (time: 20 ms/div).

Verification, Validation and Uncertainty Quantification (VV&UQ) Framework Applicable to Power Electronics Systems

Today, most engineering design projects are based on modeling and simulation. Critical decisions are being made based on simulation results. Increasing roles of computational modeling leads to the need for evaluating and comparing the models that are already being used, choosing the most efficient model for the intended use to minimize costs, and evaluating the predictive capability of the model where there is no experimental data available to verify and validate the model. All mentioned issues are discussed in Verification, Validation, and Uncertainty Quantification, known as VV&UQ. Planning and Prioritization (P&P), the modeling process, the verification process, the validation process, uncertainty quantification, and, finally, documentation of modeling and simulation activities are the main steps one needs to go through to complete the VV&UQ process. The uncertainty quantification step incorporates the concepts and results from previous steps to estimate the total uncertainty in modeling and simulation. Identifying and characterizing uncertainties provides guidance on how to reduce or manage uncertainty in modeling and simulation in the most efficient and cost-effective manner. Moreover, the proposed framework has the potential to assess and improve the model predictive capability.

In this paper, the contribution of different VV&UQ guidelines from the American Institute of Aeronautics and Astronautics (AIAA), the American Society of Mechanical Engineers (ASME), and the Department of Defense (DoD) have been used in order to propose a VV&UQ framework (shown in Fig. 1) with an emphasis on steps which are more important in the field of power electronics. The ultimate goal of this framework is to decrease dependency on experimental results, and to empower the role of modeling and simulation results in decision-making. In the end, accuracy of a switching model with a three phase voltage source inverter (shown in Fig. 2) in predicting total harmonic distortion of the output voltage is assessed. Although the VV&UQ approach is capable of building confidence in any system response quantity of a simple or complicated model, in this paper, a simple case has been chosen not to veil the description of the VV&UQ methodology since this approach is quite complicated, and requires a statistics background.

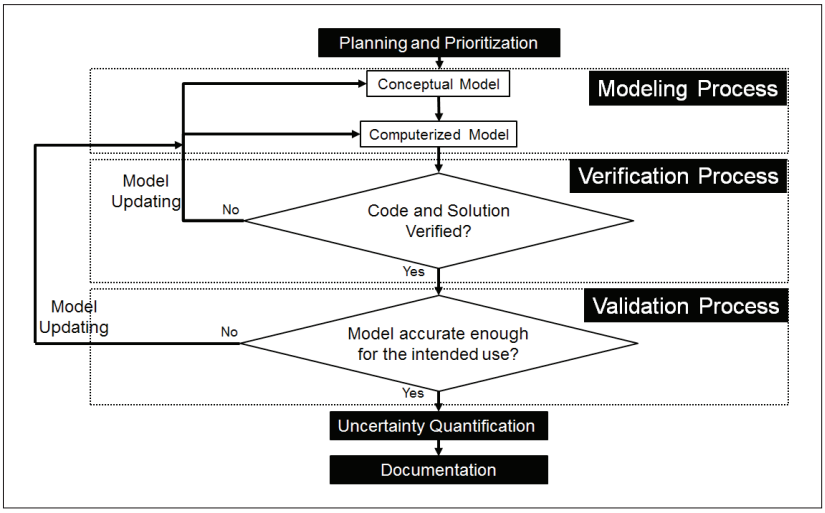


Fig. 1. Overview of Verification, Validation, and Uncertainty Quantification (VV&UQ).

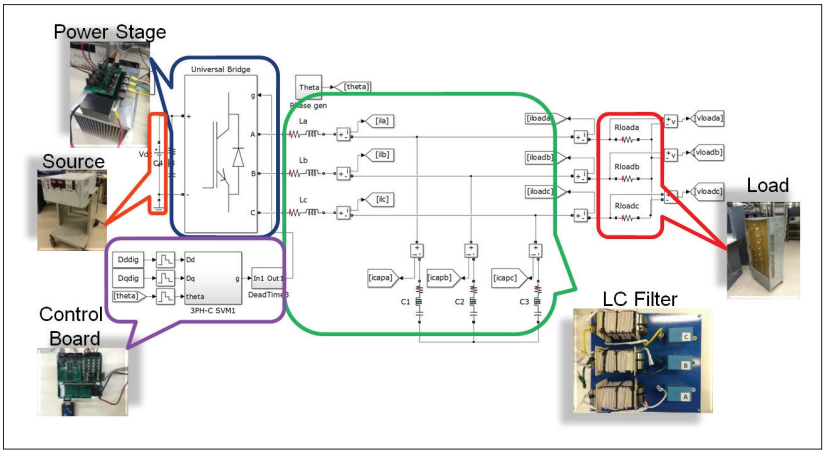


Fig. 2. Switching model of three-phase voltage-source inverter (VSI).

Determination of "Resonant Frequency" for Current-Fed Power Amplifier Using Multifrequency Modeling Technique

The current-fed power amplifier (PA) is used to generate high frequency alternating current (ac) driving the antenna L_r. It consists of two filter inductors L_f, two MOSFETs, and a parallel resonant tank with high quality factor (Q). Inductor L_f emulates a constant current source and supplies power to the tank. The PWM signals of the two MOSFETs are complementary with each other and have a 50% duty ratio. The switching frequency of MOSFETs may be as high as several megahertz with a several kilowatt power rating. Thus, zero-voltage switching (ZVS) is an important factor in decreasing the switching loss. While a large L_f could be employed to emulate a nearly ideal current source and realize ZVS when switching at natural frequency f_n, it introduces a large footprint and decreases the power density. On the other hand, small L_f introduces a large current ripple, and if still switching at natural frequency, a large current spike will flow through the MOSFETs at switching instant increasing the conduction loss of the MOSFETs and introducing extra stress (as shown in Fig. 1). The large current spike is originally caused by the phase shift between the PWM signal and the tank voltage, i.e. switching frequency deviates from the "resonant frequency". Thus, the resonant capacitor needs to be designed carefully in order to operate at the resonant frequency and achieve high efficiency with small L_f.(as shown in Fig. 1)

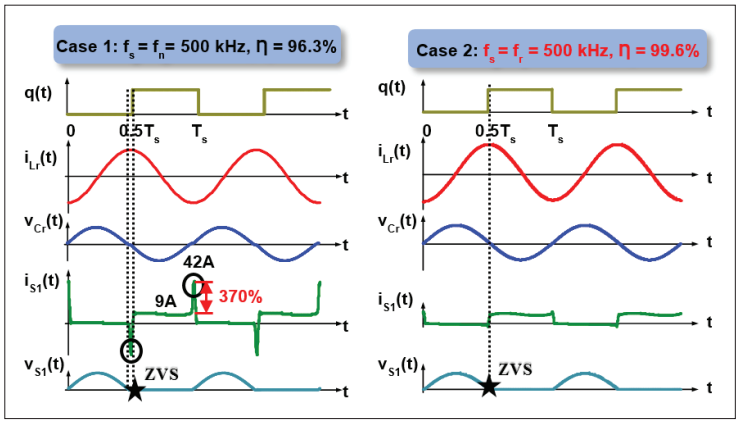


Fig. 1. Simulation waveforms of power amplifier operating at natural frequency and resonant frequency.

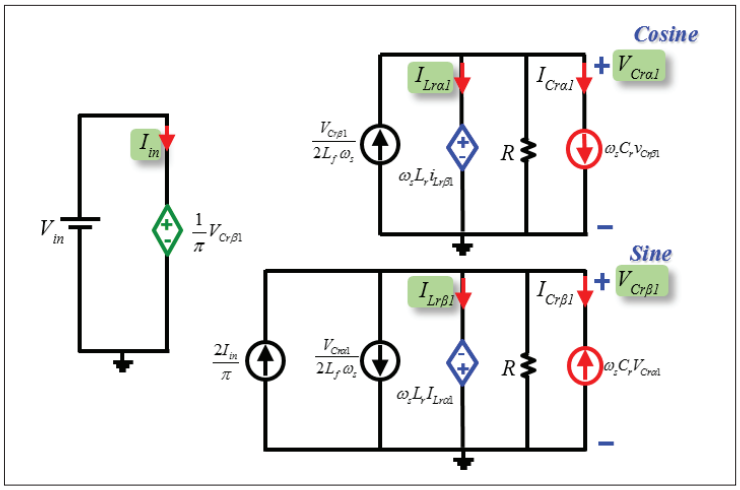


Fig. 2. Steady-state circuit model of power amplifier.

The Time-Invariant Multifrequency (TIMF) Modeling technique is utilized to account for the DC and first harmonic of the power amplifier. The corresponding steady-state circuit model is also derived for easier comprehension and use (as shown in Fig. 2). Based on the circuit model, the sine and cosine coefficients of the currents and voltages can be determined. When switching at resonant frequency, tank voltage is purely sine wave (see Fig 1) and the cosine part of $V_{Cr}(t)$ should be zero. Based on the modeling results, the resonant frequency is determined (ω_r=sqrt($1/L_rC_r+1/2L_fC_r$)). Such frequency depends not only on the tank's inductor and capacitor, but also on the filter inductors. With sufficiently large L_f, the resonant frequency can be approximated by natural frequency. Whereas, with decreasing L_f, the deviation of the resonant frequency from natural frequency will increase. If still switching at natural frequency, the effective resonant tank is inductive and causes a large current spike.

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655 Whittemore Hall
Virginia Tech
Blacksburg, VA 24061