CPES

Center for Power Electronics Systems

Annual Report 2019

VIRGINIA TECH

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Table of Contents

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CPES Research Retreat Participants (from left to right): Igor Cvetkovic, Peter Barbosa (IAB, Delta Electronics), Christina DiMarino, Rolando Burgos, Fred Lee, Johan Enslin (SAB), Tom Lipo (SAB), John Kassakian (SAB), Bob Steigerwald (SAB), Richard Zhang (IAB, GE Grid Solutions), Brian Carpenter (IAB, Texas Instruments), Al Tucker (SAB), Guo-Quan Lu, Dushan Boroyevich, Bo Wen, Ralph Cavin (SAB), Dong Dong, Dianbo Fu (IAB, Huawei Technologies), Yuhao Zhang, Qiang Li

Introduction

The power electronics program began in 1977 under the name Power Electronics Research Group (PERG). Later, in 1983, the program was renamed Virginia Power Electronics Center (VPEC) when it became a university center. In 1987, VPEC became a Technology Development Center (TDC) of Virginia's Center for Innovative Technology (CIT). The Center for Power Electronics Systems (CPES) became a National Science Foundation Engineering Research Center (ERC) in 1998, and since then has become world-renowned for its research and education/outreach programs.

The CPES mission is to provide leadership through global collaborative research and education in creating advanced electric power processing systems of the highest value to society. Specifically, CPES is dedicated to improving electrical power processing and distribution that affect systems of all sizes—from battery-operated electronics to vehicles to regional and national electrical distribution systems.

On the lower-power side, CPES has continued to make notable technological advancements. Many of these new technologies have arisen through the CPES Power Management Consortium (PMC), which has experienced immense growth over the years. Through the High Density Integration (HDI) consortium, CPES continues to explore cutting-edge materials and components, as well as packaging and integration of active and passive devices and converters. Additionally, CPES has a keen interest in supporting and growing the development and integration of higher power electronics at the power grid level. CPES intends to continue exploring these technologies by increasing its research efforts in this area under the Wide Bandgap High Power Converters and Systems (WBG-HPCS) consortium.

In early 2017, Virginia Tech announced the creation of the Electronic Energy Systems Institute (EESI), which will significantly expand its interdisciplinary research and education programs focused on power electronics and power systems. EESI will facilitate the move towards power electronics-based innovations in all forms of generation, transmission, distribution, and consumption of electrical energy. Virginia Tech and its partners are investing $15 million and have appointed CPES to lead this broad effort.

Over the past year, CPES has seen tremendous growth, in part from the EESI initiative. The next pages describe the growth in capabilities and activities enabled by our new research faculty, staff, and facilities in both Blacksburg and Virginia Tech's National Capital Region. CPES has constructed a new lab at the Virginia Tech Research Center in Arlington, Virginia, and has hired new faculty in power electronics to expand our scope of research.

Through the many years and evolutions, CPES has strongly relied on our Industry Advisory Board (IAB) and Scientific Advisory Boards (SAB) for guidance and advice on long-term strategies. Over three days in October 2018, CPES held a retreat attended by all faculty and members of the IAB, Executive Committee, and the SAB. Discussion focused on future research directions of the center, the progress and plans of the EESI, and achieving an appropriate balance between near-term applied research and long-term disruptive research. The CPES Executive Board has dedicated considerable time to discussing how best to implement the outcomes from the retreat and use them to form a near- and long-term disruptive research roadmap.

Despite ever-changing times, the CPES Industry Consortium has continued to thrive, and government funding has been strong and even growing amidst the shifting political climate. In order to keep up with increasing research demands, CPES has been growing its graduate student population. With more students and new research endeavors, CPES's prospects are bright and alive with excitement.

What will never change, however, is the service CPES provides to our members. Everything we do aims to increase the value and capabilities we offer to them. We are proud of the accomplishments detailed in this annual report and thank you for your continuing support.

TWO LOCATIONS, ONE LAB

CPES expands into the greater Washington D.C. region

The School of Architecture + Design helped CPES create a space that showcases the hands-on work being done from the benches.

For the uninitiated, "power electronics laboratory" may evoke a drab scene: A basement workspace. Flickering fluorescents. Wires piled haphazardly and trailing on the floor.

That vision dissolves with one peek into the Center for Power Electronics Systems' new lab in the greater Washington D.C. region at the Virginia Tech Research Center — Arlington.

"The work we do is incredibly exciting and cutting-edge," says Igor Cvetkovic, CPES technical director. The new lab, he explains, embraces those attributes. "This space is different from a conventional engineering lab."

The lab is sleek: floor-to-ceiling windows on three sides, custom benches with stainless steel frames and glass tops.

"We want to show the energy – teamwork energy, creative energy," says Cvetkovic. "We want passersby to see what we're doing here and rethink any preconceived notions about power electronics."

The modern, open lab environment is yielding new collaborations and wide-ranging interest even before reaching its full capacity (10 graduate students, five faculty and staff members).

Virginia Tech's School of Architecture + Design helped design the space to showcase the hands-on work being done from the benches. In another studio project, architecture students and the Washington-Alexandria Architecture Center are working to design something grander.

"They've developed master plans for a campus dedicated to transdisciplinary energy research and outreach for the 21st-century world, equipped with high voltage labs several stories high, design studios, energy museums, and housing for students and faculty," says Christina DiMarino, CPES assistant director.

Electronics Energy Systems Initiative

CPES and the School of Architecture + Design have a successful history of collaborations, the most recent being Virginia Tech's FutureHAUS Dubai, which took first place in the international 2018 Solar Decathlon Middle East competition. FutureHAUS Dubai was

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among the first efforts of the Electronics Energy Systems Initiative (EESI), a cross-college cooperation with the goal of envisioning and enacting a carbonless future.

EESI's mission is to create sustainable and enjoyable energy systems that meet current and future demands, according to University Distinguished Professor Dushan Boroyevich, CPES director and associate vice president for research and innovation. The new CPES lab is mobilizing to carry out this mission.

In the thick of it

One perk of the lab is its proximity to the new Amazon headquarters and the nation's capital with its federal agencies and international embassies.

"Part of the land-grant mission is to be a global land-grant university," says Boroyevich. "We're working to fulfill this mission by increasing our visibility with federal agencies, foreign sponsors, and other potential partners."

In addition to increasing visibility and encouraging collaboration, the new lab is well-situated to boost recruitment.

"We can now offer graduate students, visiting scholars, and professors an urban environment," says Boroyevich.

But the CPES metropolitan offshoot will maintain and strengthen ties with the Blacksburg lab.

In addition to a constant flow of new students and visits from faculty members who have offices in both locations or are taking sabbatical, "technology is here to help," says Cvetkovic.

More and more courses will be offered in-person in the Virginia Tech Research Center — Arlington, with many others offered online, and the day-to-day activities of the labs in both locations will be livestreamed.

"We're planning on having a large screen on one wall that's running a constant real-time livestream of the activities in the Blacksburg CPES labs," says DiMarino. "They will have the same on their side, and it will be one lab with a virtual window between us. That way we know we're a part of the same team." ●

CPES technical director Igor Cvetovic (above, talking with a student) says the open format of the lab exudes the Center's "teamwork energy".

FutureHAUS Dubai: Your next home

Last summer, a neighborhood of the future sprang up on a strip of Dubai desert. It was the site of the 2018 Solar Decathlon Middle East competition, which included one small solar home that produced more energy than it used overall.

That house was designed and built by the FutureHAUS Dubai team, an interdisciplinary collaboration that involved students and researchers from Virginia Tech's College of Architecture and Urban Studies who led the project, College of Engineering, Myers-Lawson School of Construction, Pamplin College of Business, College of Liberal Arts and Human Sciences, and College of Science. "We won!" said Igor Cvetkovic, technical director of the Center for Power Electronics (CPES) and the power electronics lead on the project.

"This project demonstrated how, if we trust each other and work together, interdisciplinary teams can achieve incredible things," said Cvetkovic. "We created something completely new that ended up being the best of its kind in the world."

The competition was the result of a joint effort by the United States Department of Energy and the United Arab Emirates' Dubai Electricity & Water Authority. Of the 15 international university teams competing, Virginia Tech was the only one based in the United States.

Virginia Tech's win follows almost two decades of research, two years of focused design and development, and more than a month in Dubai—where two dozen students and faculty members erected, tested, debugged, adjusted, and perfected their solar house.

Made of prefabricated structures and modular-cartridge designs, FutureHAUS can be snapped together "like LEGO® blocks" in just a few hours.

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LEFT: FutureHAUS brilliantly displays CPES's innovative power electronics technology. RIGHT: Undergraduate Elif Patton proudly shows CPES's work.

Practicing new power perspectives

Cvetkovic, three ECE undergraduate students—Matt Erwin (CPE senior), Elif Patton (EE senior), Michaela Goldammer (EE senior)— and four CPES graduate students—Vladimir Mitrovic, Joshua Stewart, Hao Xue, and Sarah El-Helw —worked closely with team members from the School of Architecture + Design. Together they interlaced FutureHAUS Dubai with a state-of-the-art electronics infrastructure that demonstrated the transformative capabilities of advanced power electronics in the home.

The FutureHAUS power infrastructure included 14-kilowatt solar arrays and a 14-kilowatt-hour energy storage system. The solar array and batteries fed excess energy into the grid via an 8-kilowatt bidirectional power inverter.

For safety reasons, all teams used standard power electronics technology—converters, batteries, charger, and solar panels. But the Virginia Tech team had their own spin on implementation; they developed an energy management system to maintain a net-positive energy balance throughout the day and designed a system that used commercial technology in unconventional ways.

"We disabled standard modes of operation in the equipment we used and implemented our own controls—that's how we went beyond other teams," explained Cvetkovic. "The competition rules did not allow for the use of power electronics prototypes and, although that would have been an ideal fit for CPES, we still pushed boundaries further than anyone else."

FutureHAUS challenged the building industry by demonstrating the use of advanced manufacturing concepts, prefabricated structures, and modular-cartridge design to redefine conventional practices of modern energy-efficient building with plug-and-play capability.

"You could literally snap house cartridges together like LEGO® blocks, and have a home put together in a few hours, with all electrical, mechanical, and plumbing infrastructure interconnected," said Cvetkovic. "You would just step inside and enjoy."

DC-powered wall

FutureHAUS is a 900-square-foot house, and the Virginia Tech team looked beyond their immediate goals by engineering some elbow room. They installed a moving wall powered by direct current (dc) that transformed one room into two.

The wall, which moved along a hidden rail, was outfitted with an entertainment system. By using dc to power it, the team was able to seamlessly and efficiently deliver low voltage to what they called "flex-space".

"Moving toward dc for domestic applications is slowly becoming an industry-wide trend, and we were able to show how this form of power distribution can be safely implemented in a home and work great," said Cvetkovic. "This was innovation executed safely."

The Solar Decathlon committee evidently appreciated the demonstration. In addition to winning first place overall, the team made a strong showing in the subcontests: first place in architecture, first place in creative solutions, second place in energy efficiency, second place in interior design, third place in sustainability, and third place in engineering and construction.

But the work didn't stop with the competition. CPES researchers have continued to improve upon and expand the power electronics technology on brilliant display in FutureHAUS Dubai.

"It was an amazing and very gratifying experience, and that's what university is about. Opening new doors and learning from each other in a great interdisciplinary atmosphere," said Cvetkovic. "But stay tuned. There's more coming." ●

> "*It was an amazing experience and that's what university is about. Opening new doors [and] learning from each other.*"
>
> —Igor Cvetkovik

New Faculty Members

Modularity and electrification:

meeting current and future demands

From the power grid to public transportation to the family car—we're due for an electronics upgrade.

Dong Dong, an assistant professor in ECE, is developing high-power high-frequency power electronics components, controls, and systems to enable a sprawling multi-decade, multi-industry infrastructure upgrade.

Many components on the power grid, for instance, have been deployed for almost a century, and Dong foresees "a huge opportunity for us to replace aging assets with our research outcomes."

Integrating, managing, and storing renewable energy resources across every sector of the grid is a formidable challenge, said Dong. Power conversion systems connect renewable resources to the grid, and Dong is working closely with power systems experts to combine cutting-edge technologies in both fields. They are developing new tools to help accelerate the transition from the traditional grid to a new grid that could be composed almost entirely of renewable assets.

Dong is also working on systems that can take full advantage of energy from renewable assets. For example, microgrids, electronic energy routers, and solid-state power substations—which are composed of innovative power electronics, sensors, and cyber solutions—can reduce complexity, increase efficiency, and add functionality and security.

The trend of electrification is lighting up applications in many other sectors of society, notably electric vehicles—cars, planes, trains, and boats. By replacing the mechanical components with power electronics systems, we can distribute propulsion components, shrink engine size, and cut carbon dioxide emissions, said Dong.

Modular high-frequency power electronics

According to Dong, industry engineers have traditionally used high-voltage devices with slower switching speeds to build the large power conversion system for high-power applications. His research on new wide bandgap semiconductors and their applications is pushing the boundaries on high-power applications.

"These devices make your system respond faster and react to load demand quickly and precisely," said Dong. "Wide bandgap devices have a much lower switching loss, so efficiency improves, and will ultimately help reduce cooling system cost, size, and complexity."

In his work, Dong uses a modular approach. He steers clear of designing "gigantic systems," and focuses on breaking the system down into modular pieces.

"With the modular approach, we can move on to medium- to high-voltage high-power conversion applications with what we learned from high-frequency switching power supplies.

We can optimize submodules and build larger high-power high-voltage systems—like LEGO® blocks," said Dong. And this modularity will make system design easier.

"It allows us to decouple system complexities and improve development cycles."

The risks and costs associated with each project are also reduced, and "we can apply the same modules for various applications with different requirements for frequencies and power levels," said Dong. "We can even populate the entire electric power system in the future with such an approach." ●

Introducing Dong Dong

Joined ECE
August 2018

Research scientist, GE Global Research Center, 2012-2018

Research assistant, Center for Power Electronics Systems, 2007-2012

Ph.D., electrical engineering, Virginia Tech, 2012

M.S., electrical engineering, Virginia Tech, 2007

B.S., electrical engineering, Tsinghua University, Beijing, 2007

Dong's modular approach allows researchers to "decouple system complexities".

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Emerging power electronics

Zhang heeds industry calls for smaller, more efficient electronic devices. SHAWN SPROUSE

The clamor for smaller, more-efficient electronic devices is so constant that many consider it background noise. Yuhao Zhang, an assistant professor in the Center for Power Electronics Systems (CPES), and his colleagues hear the cries and are examining the most fundamental building blocks of power electronics devices in order to meet the demand.

Zhang works at the intersection of three research areas: semiconductor devices, materials, and power electronics. His work bridges the gap between new materials and applications, and spurs momentum in both directions.

"We're creating devices that can't be purchased on the market or obtained from other companies, and advancing their practical applications in real-world power systems in data centers, electric vehicles and consumer electronics" he said.

Emerging materials for emerging devices

The majority of today's commercial power devices are made of silicon (Si). Many emerging power devices in research and development are based on a group of materials called wide bandgap semiconductors or ultra-wide bandgap semiconductors. These devices use materials such as silicon carbide (SiC), gallium nitride (GaN), and the less-studied gallium oxide (Ga_2O_3) and diamond. With a much larger bandgap, these materials can sustain at least 10 times the voltage of silicon with less power loss, explained Zhang.

"Overall, these materials can achieve 1,000 times higher performance compared to silicon devices—and they allow for switching at a higher frequency," said Zhang. If the system's switching frequency is higher, then the capacitors and inductors—which take up the majority of the volume of these devices—can also be smaller, significantly reducing the system's volume.

"For example, power electronics devices based on wide bandgap semiconductors can shrink the size of a laptop charger to one cubic centimeter," said Zhang. "These devices can significantly increase the efficiency and decrease the size of the overall system."

Zhang is trying to expand the application space of these materials in power electronics. He has already begun fabricating novel GaN and Ga_2O_3 devices in the clean room.

Emerging devices for emerging applications

Zhang's work isn't just on the small side.

According to Zhang, when data centers step down electricity from the grid (480 V in alternate current to 1 V in direct current), approximately one third of the total energy is lost in the conversion. By incorporating new devices like the ones CPES researchers are developing, Zhang expects the overall efficiency of power delivery to increase by at least 10 percent, which would pack a punch.

"Recent estimates claim that if we can increase overall power conversion efficiency by just 1 percent, the amount of energy we would save every year is equivalent to five nuclear power plants," said Zhang.

Whatever the physical size of the devices that will use Zhang's technology, the energy and space savings will be huge. ●

Introducing Yuhao Zhang

Joined ECE
August 2018

Postdoctoral associate, Massachusetts Institute of Technology (MIT), 2017-2018

Ph.D., electrical engineering, MIT, 2017

M.S., electrical engineering and computer science, MIT, 2013

B.S., physics, Peking University, China, 2011

CPES: it's electric

DiMarino is leading the way to developing game-changing high-speed 10 kV devices.

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The power industry is bracing for a tidal wave of demand for electrification—electric vehicles, data centers, heat pumps, motor drives, renewable energy, and grid applications.

"To meet the needs of our drastically changing landscape, a flexible, reliable, resilient, and secure power system is essential," says Christina DiMarino. "Power electronics and advanced materials can make this happen."

With a new lab in the greater Washington D.C. area, the Center for Power Electronics Systems (CPES) is set to serve as a linchpin as we pivot toward electrification worldwide; DiMarino is set to steer it.

Her first weeks as an assistant professor involved coordinating with government and industry contacts in Arlington, advancing high-density, high-speed, silicon-carbide (SiC) power module packaging, developing a hands-on course on electronics packaging, and helping to get the new hardware-focused lab up and running.

With natural light streaming in, and almost every wall a window, "the lab is an open book," said DiMarino. "Anyone can walk by and see what we're doing. It's an opportunity to interact with other centers, labs, departments, and colleges."

Module packaging research

As a doctoral student and research faculty in the ECE department, DiMarino worked alongside other researchers from Virginia Tech and the University of Nottingham on the packaging of high-voltage silicon carbide (SiC) transistors. Now, as an assistant professor, she is pushing this research further.

Wide bandgap power semiconductors—specifically SiC power devices with voltage ratings exceeding 10 kV—can switch higher voltages faster and with lower losses than existing semiconductor technologies, explained DiMarino. This drastically reduces the size, weight, and complexity of medium-voltage systems. However, these devices also bring new challenges.

"Current power module packaging is limiting the performance of these unique switches," said DiMarino.

She is leading a transdisciplinary project to address the electrical, thermal, and reliability challenges as well as electrostatic and electromagnetic interference issues associated with a high-speed 10 kV device.

"By pooling our knowledge in packaging, materials, thermal, semiconductor devices, power electronics, electromagnetics, and high voltage, we can overcome these barriers and hasten the adoption of these game-changing devices," said DiMarino.

Power electronics building blocks

DiMarino is also part of a team developing modular power electronics units, which "thanks to the flexibility of their connection, can be used in a variety of applications," she explained.

The goal of the project, sponsored by the Office of Naval Research, is to quintuple the power density of power electronics building blocks by increasing integration at the package level.

As the only full-time tenure-track faculty member permanently stationed at the new CPES lab, which officially opened in January, DiMarino says that she enjoys being able to easily and regularly meet with stakeholders for these and other CPES projects.

"We're getting our foot in the door and seeing what the opportunities are," said DiMarino. "This is just the start." ●

Introducing Christina DiMarino

Joined ECE
January 2019

Assistant director, Center for Power Electronics Systems, 2017-present

Rolls-Royce Graduate Fellow, 2016-2017

Webber Fellow, 2012-2015

Ph.D., electrical engineering, Virginia Tech, 2018

M.S., electrical engineering, Virginia Tech, 2014

B.S., engineering, James Madison University, 2012

New Staff Builds on CPES Foundation

CPES has welcomed a new cohort of staff members this past year as dedicated colleagues retired or left to pursue new opportunities.

CPES leadership is confident our new colleagues will strengthen the organization's commitment to serving our members.

Welcome

Na Ren has assumed the role of business director. During the interview process, it was apparent she was a perfect fit for CPES. Ren brings expertise in financial management with 15 years of wide-ranging experience in the private sector and in higher-education at the University of North Carolina at Chapel Hill and Virginia Tech. Ren started her financial career by earning a master's degree in economics from Northeastern University. She comes to CPES from Virginia Tech's Department of Aerospace and Ocean Engineering where she worked with 35 researchers to manage more than $5 million annually in sponsored projects funding. Prior to that, she led proposal management (more than 150 per year) for researchers at CPES and several other units while at Virginia Tech's Office of Sponsored Research.

Dennis Grove has assumed the role of industry program director. Grove brings more than 15 years of financial and project management experience. He has served in roles with increasing responsibility at top research and academic institutions including Ames National Laboratory at Iowa State University, Yale University, and Virginia Tech. Before joining CPES, Grove was a program manager for Virginia Tech's Institute for Critical Science and Technology, where he managed more than $1 million annually in university investment in interdisciplinary research in sustainable energy and sustainable water science and technologies. Grove earned master's degrees in business administration and organic chemistry at Iowa State University.

Audri Cunningham has become Boroyevich's executive assistant. Cunningham joins CPES after providing support for 12 generals and executive service staff at the U.S. Department of Defense. Cunningham's language skills — she speaks German, French, and some Arabic — will be an asset for multicultural members, researchers, and staff.

Yan Sun, Fiscal and Accounting Associate, has joined CPES after 12 years as a financial service representative with SunTrust where she won multiple awards for outstanding customer service. She coordinates all payroll, travel, wage employee timecards and other departmental accounting assignments.

Saying good-bye

Linda Long, longtime CPES business manager, retired in summer 2018 after 20 years with CPES. Long successfully managed CPES through the National Science Foundation ERC times into a fully self-sustaining organization. Since retiring, she has built a house in Raleigh, N.C., and is enjoying spending time with family.

Teresa Shaw, industry program director, retired this past winter. Shaw seamlessly helped guide researchers, students, visiting scholars, and industry members as they interacted with CPES during the past 29 years. Shaw, who plans to travel the world to see the many friends she made during her professional career, has already visited Brazil and Hong Kong.

Marianne Hawthorne, who served as Dushan Boroyevich's executive assistant for 17 years, has moved to a new role within Virginia Tech at the Hume Center for Cybersecurity.

Lauren Shutt, the CPES webmaster for three years, left Virginia Tech to pursue an advanced degree in anthropology.

Celebrating continuity

CPES is also enjoying some noteworthy continuity.

Trish Rose, procurement officer, continues in her role enabling the acquisition of all materials and supplies required to run a world-class power electronics lab.

David Gilham, who earned his master's degree with CPES, is now a research faculty member who serves as operation director for the CPES laboratories.

Long and **Shaw** also have continued as consultants to help ease the transition for Ren and Grove.

2018 CPES Student Council Report

Over the past year, the student council worked to build a stronger state of inclusion throughout the CPES community. In an effort to bolster the connection between students, visiting scholars, staff, and faculty, additional and more diverse engagement efforts were implemented. Some of these events and initiatives include CPES bowling night, the annual summer picnic, Lunar New Year potluck, and a new map depicting the origins of the current students. The council would like to thank all of the volunteers, staff, faculty, and alumni for their time and effort supporting the CPES family in the past year.

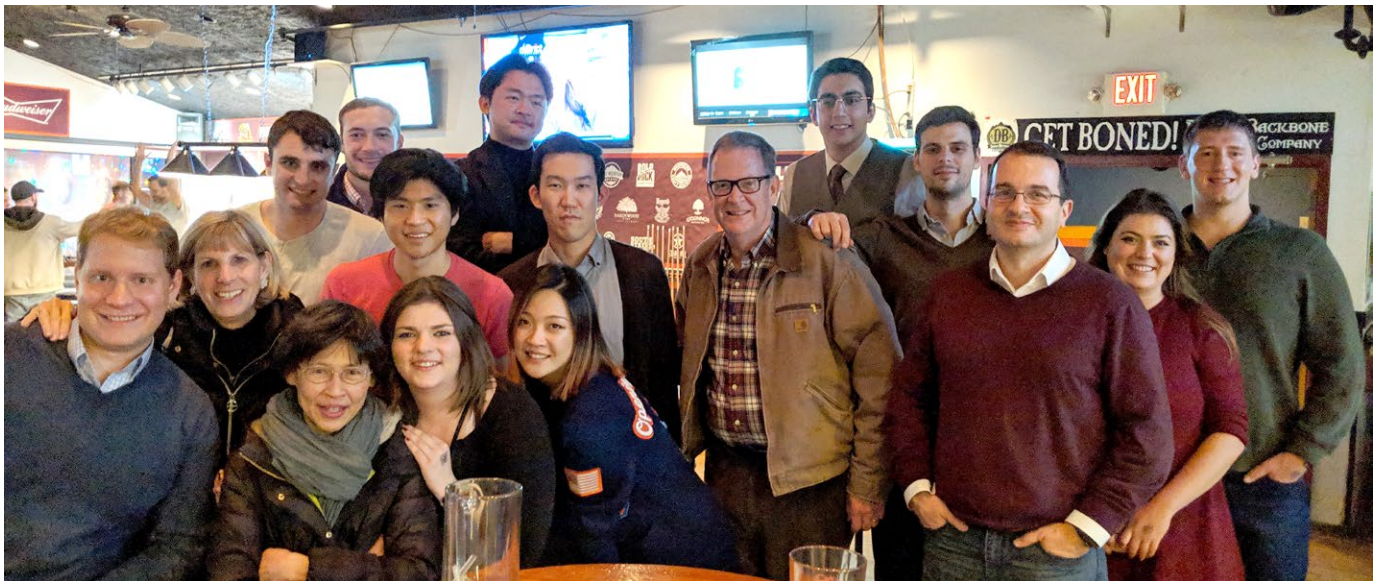
CPES group picture at the 2018 Summer Picnic at Chateau Morrisette

CPES students attend a lecture by Huang-Jen Chiu of the National Taiwan University of Science and Technology which was sponsored by the IEEE PELS Student Chapter at VT.

CPES students host a tour for undergraduate students in support of IEEE PELS Student Chapter at VT.

CPES Bowling Night, January 2019

CPES students from around the world!



CPES students thank Linda and Teresa for their years of service.

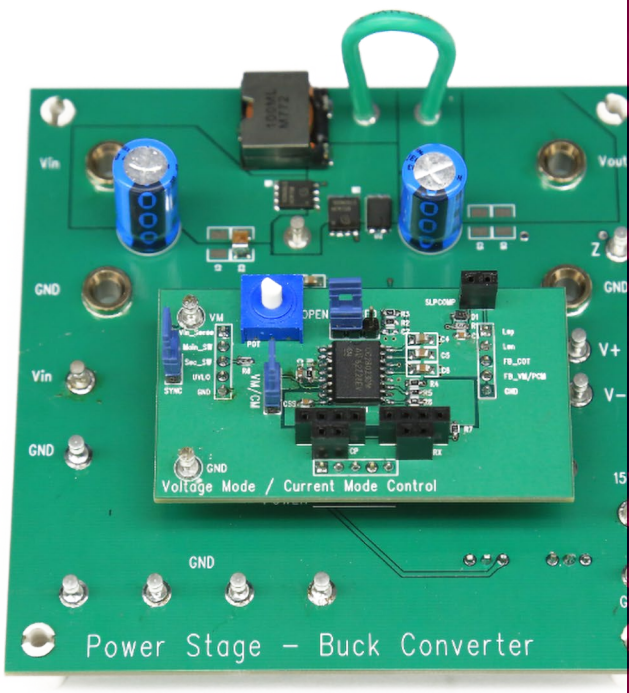
Short Course

One of the missions of CPES is to provide the opportunity for practicing engineers to broaden their knowledge base and stay updated on new technologies by offering professional short courses that will provide a clear understanding of the fundamental principles and a working knowledge of cutting-edge technology and applications. CPES is currently offering a professional short course on the topic "Modeling & Control Design of DC/DC Converters". This course will engage engineers in a combined lecture/laboratory instructional format, providing hands-on experience in the dc-dc converter analysis, modeling, simulation, control design and frequency domain measurement techniques.

With individual step-by-step guidance in the lab, participants will learn through simulation and measurements how to solve design problems using peak current-mode control, voltage-mode control, constant on-time current-mode control and constant on-time V2 control for both Buck and Boost converters. Participants will see the impact of loop-gain design on closed-loop performances such as stability margins, small-signal and large-signal dynamics, output impedance and audio susceptibility. Attendees will gain a clear understanding of power converter control through exercises such as determining dc and ac characteristics of power stages.

Below are the key contents of the course:

- DC and steady-state analysis of PWM converters
- Modeling and analysis of PWM converters
- Single-loop (voltage-mode) control for PWM converters
- Peak current-mode control systems
- Average current-mode control systems
- Constant on-time current-mode control
- Constant on-time V2 control



The Buck converter is one type of converter featured in this course.

Leading the Way

Cutting-edge advancements

Leading the Way

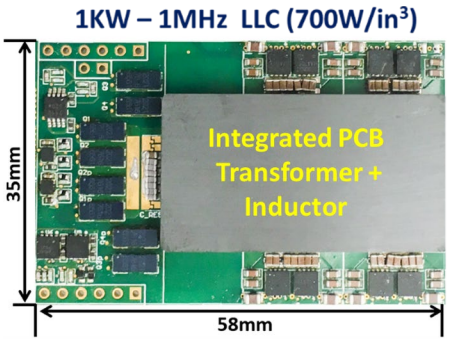
Cutting-edge advancements

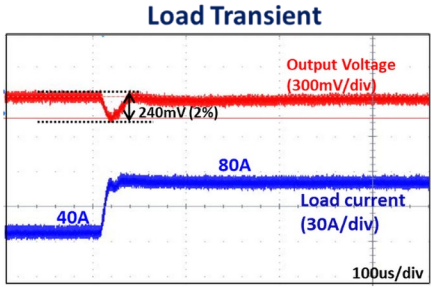
High-Frequency High-Density 1 kW 48 V LLC Bus Converter with Optimal Trajectory Control

The 48 V bus converter is a fundamental block in the power architecture of many applications such as network and telecom data-centers. Here, we propose a 1 MHz, 1 kW full-bridge LLC resonant converter as a high-efficiency, high power density solution for 48 V bus converter. The converter can achieve peak efficiency of 97.8 percent, and fits in the standard quarter brick size with power density of 700 W/in^3. The LLC features soft switching, which allows us to operate at high switching frequency and minimize the magnetic components' size while maintaining high efficiency. The converter is designed with a novel PCB winding matrix transformer. Here we integrate four elemental transformers with a resonant inductor using the same winding and a single core structure. This magnetic integration approach enables a very high-efficiency and power-density operation.

The designed LLC converter provides a 12 V output regulation from a wide input voltage range of 40 V to 60 V. Thus, the converter covers a gain range of 0.8 to 1.2 that corresponds to a switching frequency range of 0.8 MHz: 1.8 MHz. The converter is controlled with Simplified Optimal Trajectory Control (SOTC) to achieve fast transient response. Digital implementation of 2-step SOTC is proposed in this work for the high frequency LLC using a low-speed microcontroller.

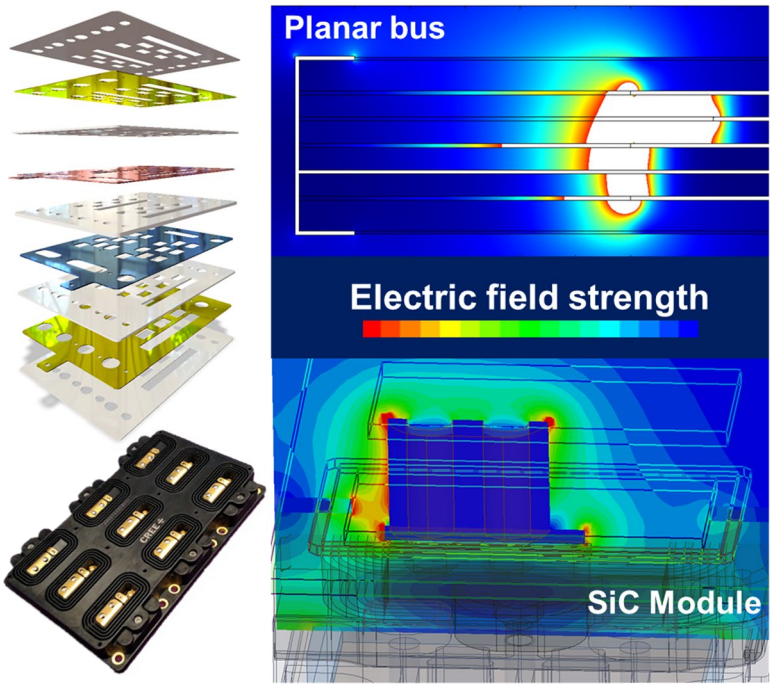
SOTC can achieve optimum transient response for an LLC operating at resonant frequency, but it has limited impact at wide-gain range. A feedforward compensation is proposed in conjunction with SOTC to achieve optimum transient response at wide input voltage range. With this control approach, we have been able to achieve very fast load transient response at wide switching frequency range with settling time less than 40 µs for 50 percent to 100 percent load transient.





High-Voltage, Partial Discharge-Free Power Electronic Design

Achieving a high power density high-voltage power electronics converter design is highly dependant on how well electric fields are controlled within the internal converter structure and inside its components. CPES has started a serious research effort in the domain of the insulation systems, electric field shaping, and partial discharge prevention for modular power electronics converters operating at several kilovolts and processing megawatt-level power. The mitigation of partial discharge phenomena will consequently reduce the occurrence of voltage breakdowns, prevent premature failure of components, and minimize degradation of the insulation material, significantly extending the lifetime of converters operating at very high switching frequencies, a capability enabled by fast SiC devices. The figure on the right illustrates a multilayer planar dc bus under design to effectively restrain electric fields, especially near the power module terminals susceptible to partial discharge phenomena. The use of shields and field shaping terminations, as well as dielectric coating will allow an unseen power density of modular power converters to boost operation to very high voltages while converter enclosure stays at a safe-to-touch voltage-level.

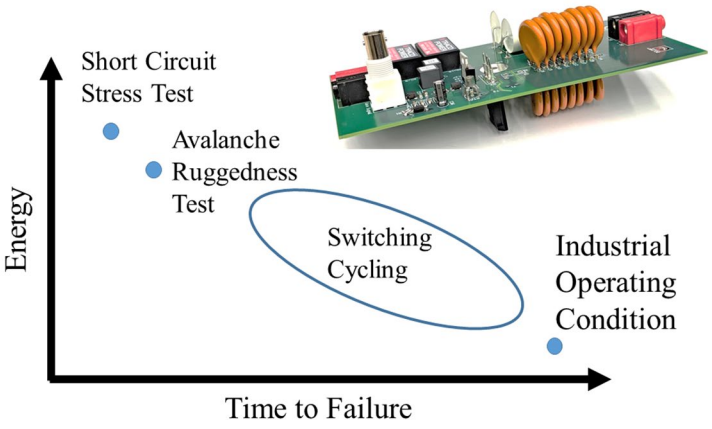


Leading the Way

Cutting-edge advancements

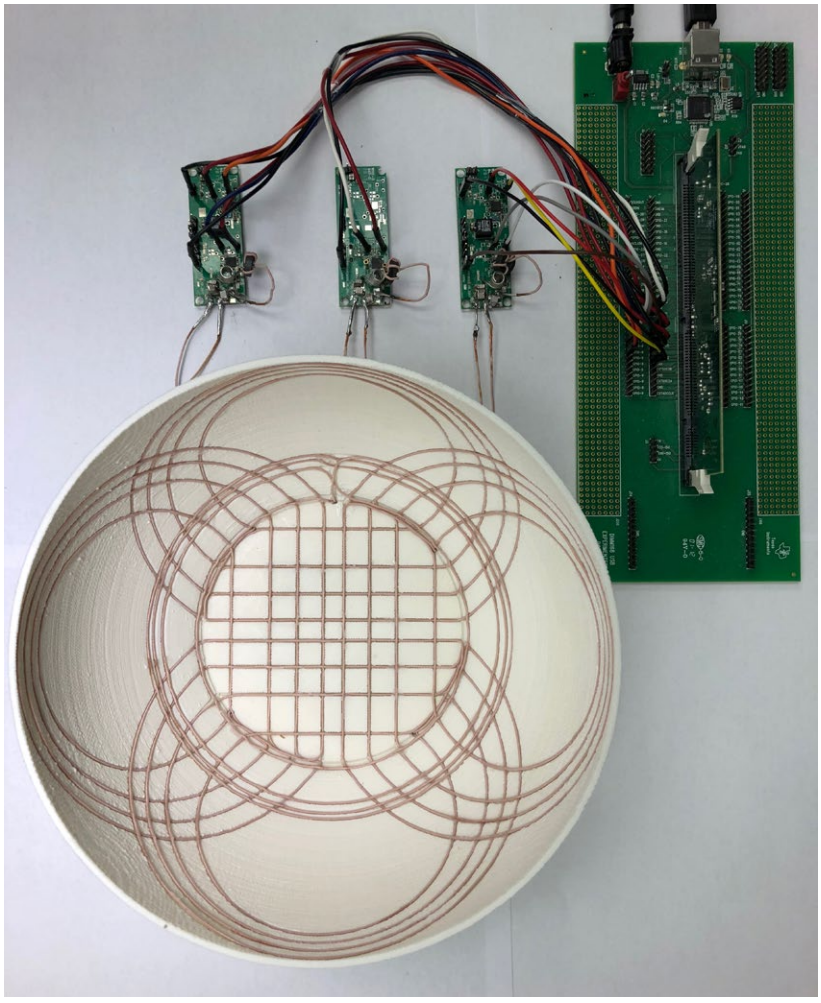
Switching Cycling— A Dynamic Accelerated Lifetime Test

Silicon carbide (SiC) MOSFETs are emerging as the new leading power semiconductor device for medium-power electronic systems. While these devices have been commercialized and proven in prototype systems, their long-term reliability under various operating conditions is still uncertain. Traditional dynamic ruggedness tests include short circuit, or avalanche ruggedness tests which imposes great stress to the semiconductor and package. Switching cycling is introduced to stress the device under a high electric field and high peak current; however, this is done at energy levels much lower than traditional tests. A 1.2 kV, TO-247 SiC MOSFET undergoes continuous pulses in a standard clamped, inductive switching circuit. The ambient temperature is held to 25 °C. The system, designed to be completely automated, switches the device with an on-time to reach the desired peak current while minimizing conduction losses and self-heating effects. Device electrical parameters are periodically monitored; threshold voltage, on-resistance, gate leakage current, and drain leakage current are the focal precursor parameters being observed. Preliminary results have shown changes in semiconductor-focused parameters over package-focused parameters.



A 6.78 MHz Omnidirectional Wireless Power Transfer System for Portable Devices

A novel wireless charging bowl with multiple transmitter coils is proposed to power portable devices. The bowl-shaped transmitter coil is optimized to provide sufficiently strong and nearly uniform omnidirectional field distribution. The magnetic field can rotate in different directions and, therefore, a planar receiver coil can be charged with arbitrary orientation inside the bowl. The alignment between the transmitter and receiver unit is not needed and portable devices can simply be dropped in and get charged efficiently. Compared with a planar charging pad in which exact alignment is needed, the proposed charging bowl is a promising charging solution for consumer electronics. The overall system efficiency varies within a range of 68 percent to 80 percent when charging a 5 W smartphone receiver with arbitrary positioning.

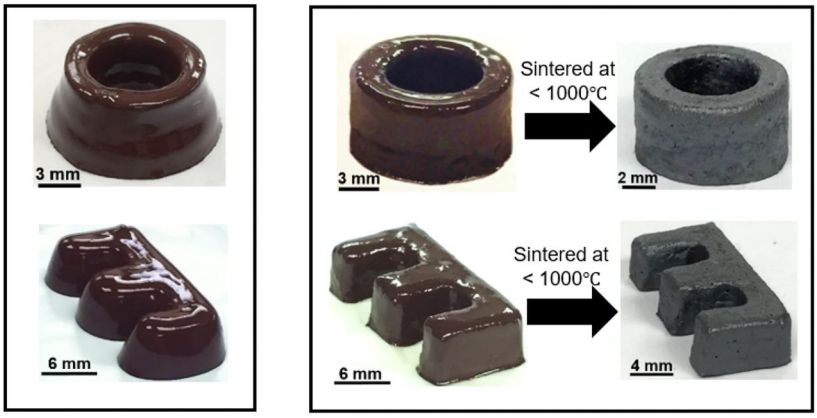


Leading the Way

Cutting-edge advancements

UV-Curable Ferrite Paste for 3D Printing of Power Magnetics

Additive manufacturing (AM) has the potential to rapidly prototype innovative designs of magnetic components aimed at improving power density and efficiency of switch-mode power converters. However, only a few magnetic feedstocks are available for AM, and the fabricated parts have significantly poorer magnetic properties. Our previous studies showed the promise of an extrusion-based AM platform for making high-performance power magnetics. However, the magnetic paste feedstock developed in these studies suffered from a "slumping" problem; they were not suitable for building large or tall core structures. To improve the AM capability, a UV-curable ferrite paste was developed that "solidified" upon UV illumination. Core structures with large aspect ratios were fabricated by retrofitting the printer with a UV-LED module. By varying the magnetic composition of the paste and sintering the printed parts at and below 1,000° C, we made tall (greater than 4 mm) ferrite cores with relative permeability ranging from 63 to 103 and resonance frequency higher than 30 MHz.



(a) Slumping feedstock printed without UV illumination. (b) UV-assisted 3D printed toroid and E cores.

A Class-E Inverter with Zero-Voltage Turn-On and Fixed Voltage Gain Under Load Variation

The Class-E topology was presented as a single switch power amplifier with high efficiency at the optimum condition, where the switch enjoys zero-voltage (ZV) and zero-voltage-derivative (ZD) turn-on (TO). It is also used in MHz dc-dc converters, and inverters for wireless power transfer, induction heating, and plasma pulsing. However, non-ZVTO and varying voltage gain occur when the operating point is not the optimum condition.

Traditional design also relies on solving differential equations numerically. The calculation error and the difference between real component value and the calculation result will induce unexpected performance in the circuit, which is difficult to be corrected without knowledge of the circuit.

A sequential design methodology of a fixed-gain Class-E inverter is proposed without adding components or using closed-loop controls. The revealed operating principle simplifies both the design and the debug. Fixed voltage gain and ZVTO are kept with load variation, and ZV + ZDTO is realized under full load condition. The schematic and the designed Class-E inverter are shown in Fig. 1; it is switched at 6.78 MHz with 11 V input voltage, 16 V output voltage, and 25 W maximum output power. The waveforms in Fig. 2 show that ZVTO is kept with 9 percent output voltage increase over 10:1 output power range; the derivative of drain-to-source voltage at turn-on moment is 0.16 V/ns under the full load condition.

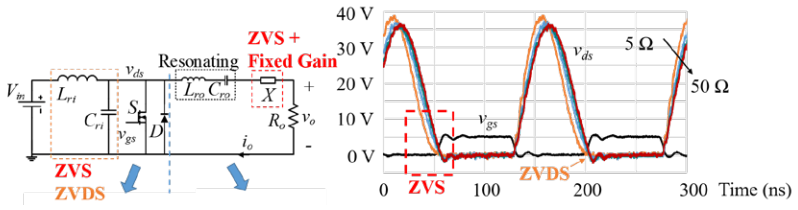


Fig.1. The designed Class-E inverter with its schematic.

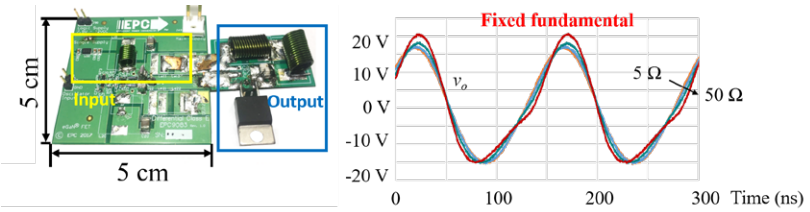


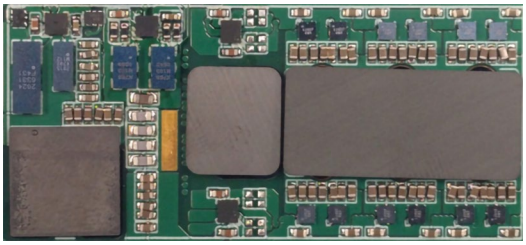
Fig. 2. Tested waveforms under load variation.

Leading the Way

Cutting-edge advancements

Wide Voltage Range High-Efficiency 48 V/CPU Voltage Regulator

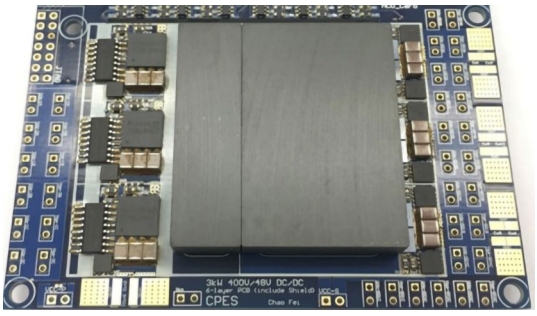
As U.S. data centers' power demands increase, it is imperative that more efficient power conversion solutions with higher power density be developed. This can be accomplished using a one-stage quasi-parallel power architecture known as the Sigma converter. The proposed power delivery architecture shares the power between two converters connected in series from the input side and parallel connected from the output side. As opposed to well-established two-stage solutions, higher conversion efficiency is always obtained with the Sigma converter. A variable-controlled gain LLC converter with novel magnetic integration is utilized in the Sigma converter architecture powering the CPU.



This enables efficient wide voltage range operation. A converter prototype has been built that meets Intel's VR specifications; the converter can provide a maximum output current of 100 A, while achieving maximum efficiency of 95 percent and power density of 700 W/in^3.

3 kW Three-phase Interleaved LLC Converter with Integrated Magnetics for 48 V Output

The LLC converter is deemed the most efficient topology in server and telecom applications. It has been demonstrated that the three-phase interleaved LLC converter can achieve further efficiency improvement at the 3 KW power level. However, the magnetic components for multi-phase LLC are complex, bulky, and difficult to manufacture in a cost-effective manner. A high-frequency GaN-based three-phase LLC converter is being used to attempt to address these aforementioned challenges. With GaN operating at 1 MHz, all magnetic components–namely, 3 inductors and 3 transformers–can be integrated into one common structure, while all magnetic windings implemented are in a compact 4-layer PCB with 3 oz. copper. The proposed structure can be easily and cost effectively manufactured in high quantity. Furthermore, up to a 25 db reduction of common-mode noises, from 150 KHz up to 30 MHz, can be realized if two additional PCB layers are employed for a proposed CM noise shielding. A 3 kW 400 V/48 V 3-phase prototype has been built with estimated peak efficiency greater than 97.5 percent and power density greater than 600 W/in^3 (15 kW/L).



Hetero-Magnetic Swinging Inductor (HMSI) for CRM PFC Converter

A traditional swinging inductor with discretely varying gap length is used for total harmonic distortion (THD) reduction in passive PFC converters. However, it has step-wise L-I curve which cannot match well with the desired L-I curve (Fig. 1). The gap also introduces fringing flux and significantly increases AC winding loss at high frequency. In order to have a matched L-I curve and reduce fringing field, we introduce a swinging inductor (Fig. 2) consisting of a core with simple, constant-length gaps that are filled by materials whose magnetic properties are tailored for desired L-I curves. We call this swinging inductor a hetero-magnetic swinging inductor (HMSI).

The HMSI concept builds on our materials processing expertise in formulating filler materials with wide-ranging magnetic properties. Combining with selection of gap length(s) and the core magnetic material, an HMSI offers greater flexibility for wider L-I swinging characteristics with low core loss and minimal fringe effect. We applied the HMSI concept in a critical conduction mode (CRM) PFC boost converter aimed at reducing the range of switching frequency range. In a conventional CRM PFC boost converter, the switching frequency variation comes from the changing of the input line voltage with a constant value boost inductor throughout the whole line. By implementing HMSI whose inductance follows a designed function to attenuate the influence of the changing input line voltage, switching frequency variation can be reduced compared to a converter using a linear inductor (Fig. 3).

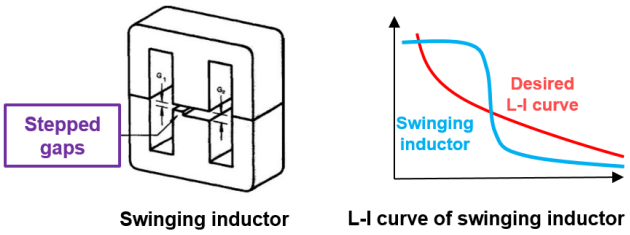


Fig. 1. Swinging inductor and its L-I curve

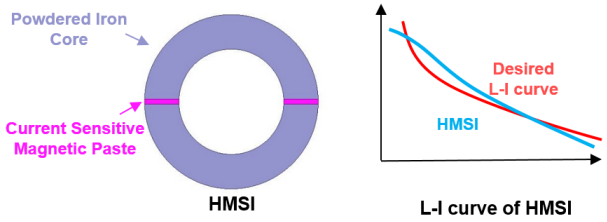


Fig. 2. HMSI and its L-I curve

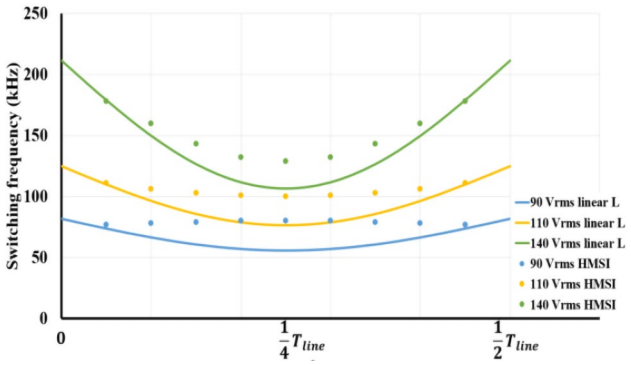


Fig. 3. Switching frequency variation comparison in CRM PFC converter.

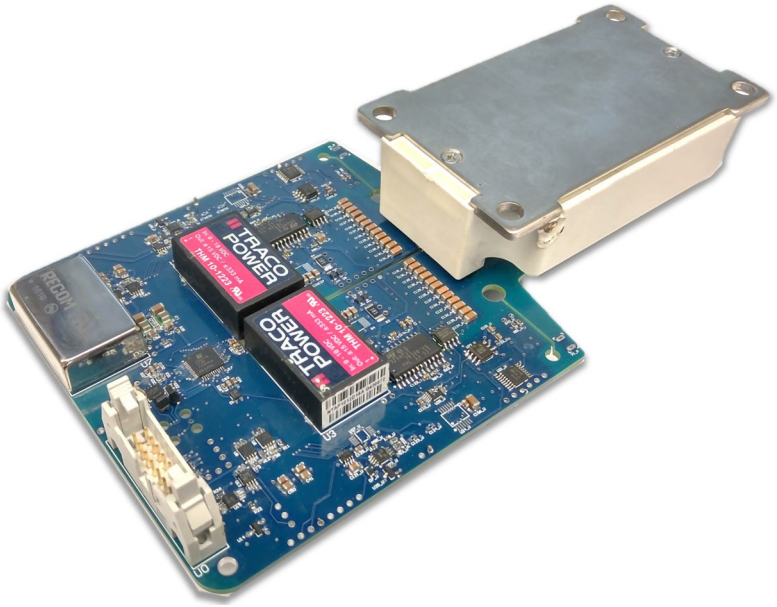
Leading the Way

Cutting-edge advancements

Enhanced Gate-Driver for 1.2 kV SiC MOSFET High-Current Modules

Due to advantages over conventional Si IGBT devices, integrating silicon-carbide (SiC) MOSFETs has become an attractive solution in power electronics converter design owing to their ability to meet the demands of higher power density, high efficiency conversion, and lower system cost. To further utilize the benefits of this new technology, an enhanced gate-driver has been developed, and benefits that a gate-driver-level intelligence can contribute to SiC-based power inverters have been explored.

The intelligence is brought by PCB-embedded Rogowski switch-current sensors (RSCS) integrated on the gate driver of a 1.2 kV, 300 A SiC MOSFET half-bridge module. They collect two MOSFET switch currents in a manner of high-magnitude, high-bandwidth, and solid signal isolation. The switch-current signals are used for short-circuit detection under various fault impedances. Experimental results show short-circuit detection times of only 80 ns, keeping the SiC MOSFET in the safe operating zone and far away from the breakdown point. Compared to a conventional desaturation protection for high-current modules, it exhibits superior performance in all relevant aspects such as detection and protection times, voltage and current overshoots, and dissipated energy. Moreover, switch-current signal are being utilized for phase-current reconstruction by digitally subtracting one switch current from another on the gate-driver's FPGA. This manipulation enables the gate-driver to directly communicate the phase-current information to the main controller, thus eliminating the necessity of



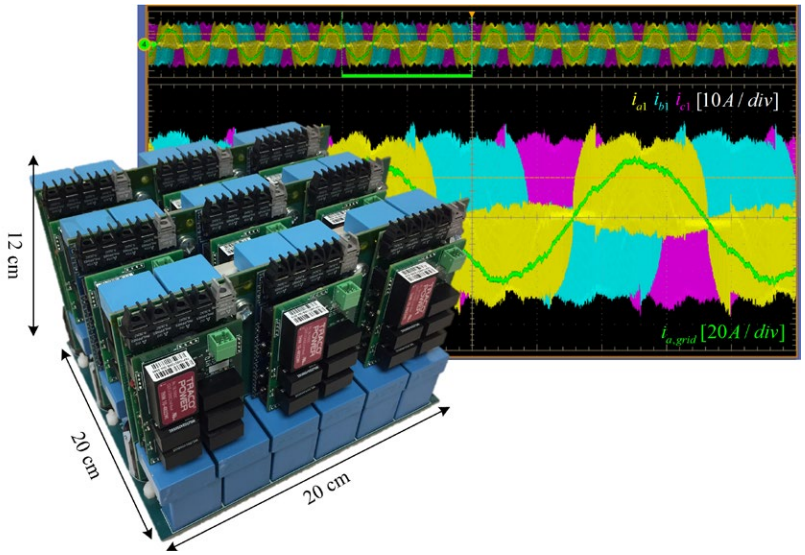
using additional current sensors, further increasing the systems reliability and power density. Phase current sensor performance is satisfactory, exhibiting greater than 98 percent accuracy, 1.6 µs delay, and 2.5 percent non-linearity error during continuous PWM schemes. During discontinuous PWM schemes, the phase current sensor exhibits similar performance. However, an additional processing aid from a main controller is needed in order to successfully obtain phase current during clamped periods of these modulation schemes for three-phase inverter applications. Reconstruction principles employed on the developed gate-driver can be applied to any half-bridge power module.

High Power Density, High-Efficiency, Three-Channel, Three-Level Commercial Photovoltaic Inverter Operating in Interleaved Triangular Conduction Mode

For tens to hundreds kW-level PV farms, the PV inverters may directly be connected to the grid without any transformer to improve power density and efficiency. Leakage current through parasitic capacitors of PV panels is required to be limited below 300 mA by standards. 3-level topologies such as neutral point clamped (NPC) or T-type are widely adopted to limit the leakage current. However, the switching frequencies of hard-switching SiC inverters are limited below 70 kHz due to the EMI and efficiency concern.

To improve the power-density of SiC inverters, zero-voltage switching (ZVS) schemes have been investigated. Triangular conduction-mode (TCM) delays turn-off time to generate reverse current, and achieves ZVS. Such a scheme has been extended to three-phase applications by operating the other two phases with two different conduction-modes: discontinuous conduction-mode (DCM) and clamped-mode, which is similar to a discontinuous PWM (DPWM) scheme. The variation of switching frequency is narrow and modulation index can go over 1 while the switching frequency can go up to hundreds of kHz with efficiency near 99 percent.

In this work, it has been demonstrated that a three-level three-phase full-SiC PV inverter can operate at TCM for ZVS with a 40 kW prototype hardware. First, a decoupled modeling approach has been presented to understand three-phase coupling. The three-phase inverter can be interpreted into a single-phase TCM, and DCM inverter and techniques for a single-phase TCM inverter can be directly applied. Second, a closed-loop current-control based on a digital controller has been presented. Without any look-up-tables,



current control and closed-loop interleaving of three-channels can be achieved within 27 µs by TMS320F28343. Finally, a comparison between optimized CCM inverter has been performed. The result shows -36 percent reduction on weight of filter inductors. A common-mode EMI filter highly benefits by high switching frequency with the closed-loop interleaving. High differential-mode EMI from TCM operation can be handled relatively easily from additional filter capacitors. Projected power density is 98.8 percent at full load with 4.06 kW/kg power density.

Statistics

$158M+
Research expenditures

240
Companies have belonged
to the CPES Industry Consortium

175
PhD degrees awarded

126
Patents awarded

27
Startup companies founded
by CPES alumni

332
Visiting professors, students,
and industry engineers

2
National Academy
of Engineering members

24,000
Square feet of space

910
Research projects sponsored by government and industry

3,028
Conference and journal papers

185
Master's degrees awarded

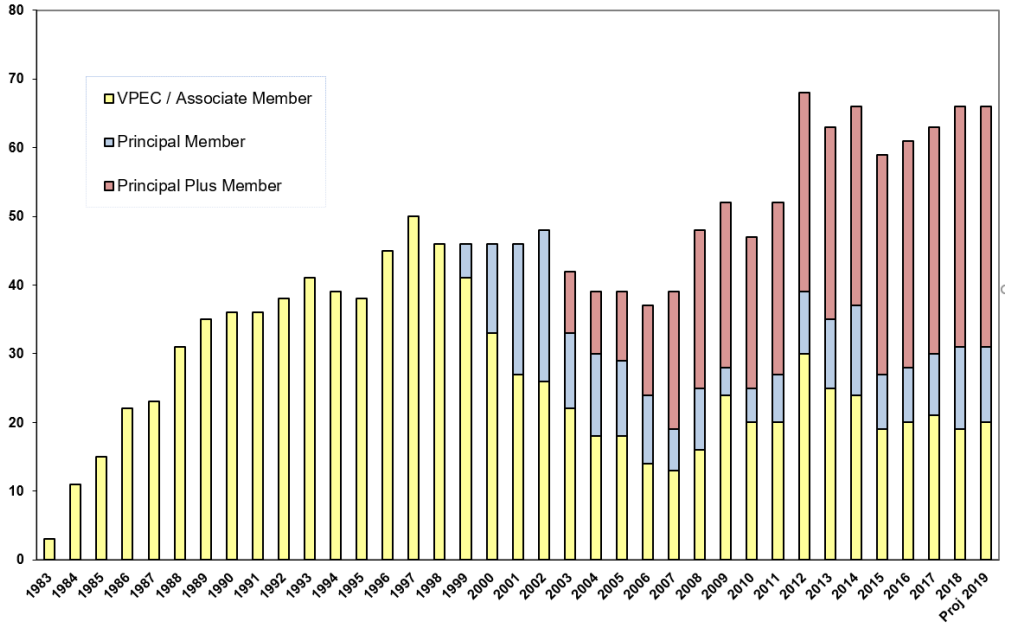
298
Invention disclosures filed

19
CPES alumni in academia

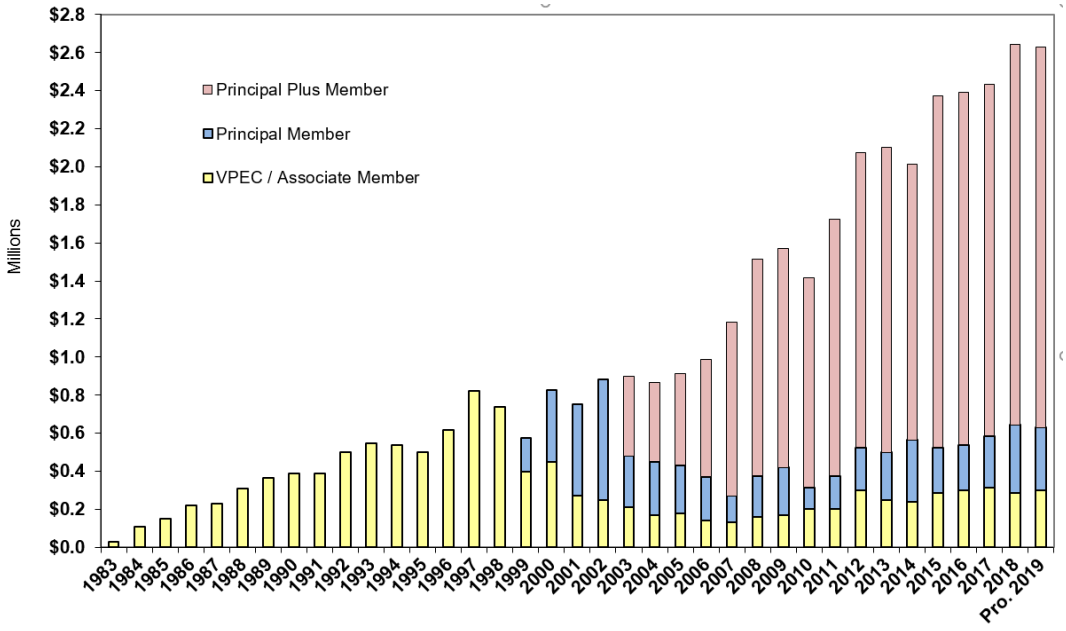
41
Countries with technical exchange

4
IEEE Fellows

CPES Membership Company Growth



Industry Membership Funding Growth



Overview

CPES Industry Consortium

The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members.

The CPES connection provides the competitive edge to industry members via:

- Complimentary registration for CPES Annual Conference
- Access to state-of-the-art facilities, faculty expertise, and top-tier students
- Leveraged research funding of more than $5 million per year
- Industry influence via CPES's Industry Advisory Board
- Intellectual properties with early access for Principal Plus and Principal members via the CPES IPPF (Intellectual Property Protection Fund)
- Technology transfer made possible via special access to CPES's multidisciplinary team of researchers, and their publications, presentations, and intellectual properties
- Continuing education via professional short courses offered at a significant discount
- Opportunities to send engineers to work with CPES researchers on campus via the Industry Residence Program

The CPES industrial consortium offers the ideal forum for networking with leading-edge companies and top-notch researchers, and provides the best mechanism to stay abreast of technological developments in power electronics.

MEMBERSHIP STRUCTURE

Principal Plus Members

Annual contribution - $50,000

Principal Plus Members gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research—PMC (Power Management Consortium), HDI (High Density Integration), or WBG-HPCS (Wide Bandgap High-Power Converters & Systems). Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each. In addition to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting-edge IPs via the CPES IPPF (Intellectual Property Protection Fund), as well as interactive opportunities with CPES researchers via designated student contacts and mini-consortium reviews.

Principal Members

Annual contribution - $30,000

Principal Members are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund) membership, in addition to all the benefits offered to Associate Members.

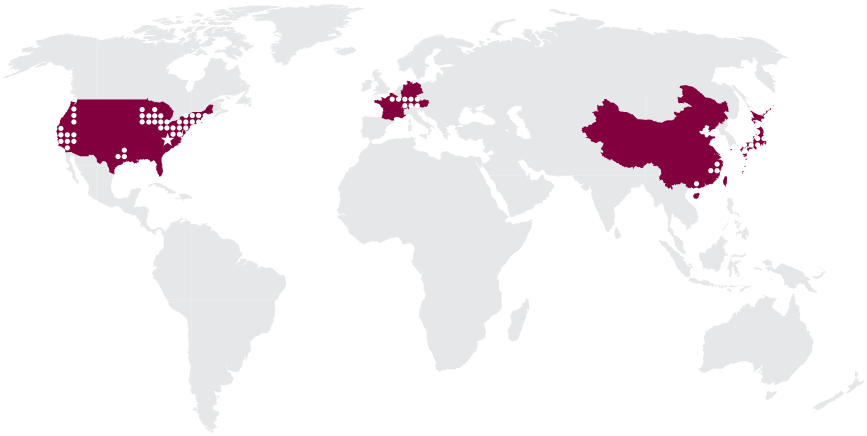
Associate Members

Annual contribution - $15,000

Associate Members gain a competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also through opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short courses to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the Center in technical areas that are of mutual interest, to be determined jointly with the CPES faculty host.

Affiliate Members make in-kind hardware/software donations to CPES equivalent to $10,000 per year. Their contributions must be relevant to CPES research. Membership participation at this level requires approval of the Center Director.

CPES



Industry Members
February 2018–February 2019

Principal Plus Members

3M Company
ABB Inc.
Analog Devices
Chicony Power Technology Co. Ltd.
CRRC Zhuzhou Institute Co. Ltd.
Delta Electronics
Dowa Metaltech Co. Ltd.
East China Research Institute of Microelectronics (ECRIM)
Efficient Power Conversion
Eltek
Ford Motor Company
FSP-Powerland Technology Inc.
GaN Systems
GE Global Research/GE Aviation
GE Grid Solutions
General Motors Company
Groupe SAFRAN
Huawei/Futurewei Technologies Co. Ltd.
Infineon +IR
Intel
Inventronics (Hangzhou) Inc.
Jiangsu Wanbang Dehe New Energy Co., Ltd.
Komatsu
Lite-On Technology Corporation
Lockheed Martin Corporation
Moog Inc.
Murata Manufacturing Co. Ltd.
Navitas Semiconductor
Nissan Motor Co. Ltd.
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Microsoft Corporation
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Robert Bosch GmbH
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Sumitomo Electric Industries
Suzhou Inovance Technology Co. Ltd.
TDK-Lambda Corporation
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CISSOID
EGSTON Power Electronics GmbH
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Mentor Graphics Corporation
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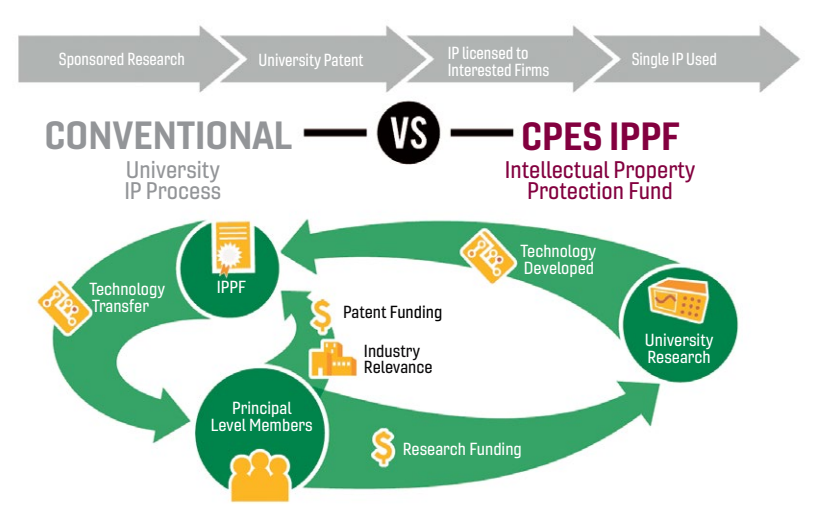
Plexim GmbH
Powersim Inc.
Simplis Technologies Inc.
Synopsys Inc.
Taiyo Yuden Co. Ltd.
Tektronix Inc.
TOKIN Corporation
Transphorm Inc.

Intellectual Property Protection Fund (IPPF)

IPPF is a unique IP access mechanism that provides extraordinary IP advantage to all Principal-level members. IPPF is available automatically, at no additional cost, to Principal Plus and Principal members. IPPF members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by IPPF.

Once a technology is protected, IPPF members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IPPF is applicable only to technologies developed by CPES-VT researchers under the CPES industry consortium.




Industry
Academia
Government
CPES
Mini-Consortiums
WBG-HPCS
HDI
PMC

Mini-Consortium Program

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing precompetitive technologies to address common challenges, and share the research results among mini-consortium members.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contributions of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- **PMC** (Power Management Consortium)
- **HDI** (High Density Integration)
- **WBG-HPCS** (Wide Bandgap High Power Converters and Systems)

Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

Power Management Consortium (PMC)

In 1997, at the request of Intel, CPES established a voltage regulator module (VRM) mini-consortium to address the issue of power management for future generations of microprocessors, targeting sub-1 volt and 100-200 amps current. As a result of this focused research, the CPES team developed a multi-phased VRM. Instead of paralleling power semiconductor devices to meet the current demand and efficiency requirements, the research team proposed to parallel a number of mini-converters. By paralleling the mini-converters and phase-shifting the clock signal, the team was able to both cancel the significant part of the output current ripple and increase the ripple frequency by N times, where N is the number of channels paralleled. This resulted in significant demonstrated improvement, specifically:

- 4 times improvement in transient response
- 10 times reduction in output filter inductors
- 6 times reduction in output capacitors
- 6 times improvement in power density

The new generation of Intel's microprocessor is operating at a much lower voltage and higher current, with a fast dynamic response in order to implement the sleep/power mode of operation. This mode of operation is necessary to conserve energy, and to extend the operation time for battery-operated equipment. The challenge for the VRM in this case is to provide a precisely regulated output with fast dynamic response in order to transfer energy as quickly as possible to the microprocessor. Today, every Intel processor is powered by such multiphase VRMs developed by CPES.

The Power Management Consortium (PMC) is an outgrowth of the early VRM mini-consortium initiated in 1997. The goal is to extend its research scope with a focus on developing precompetitive technologies in the areas of power management for distributed power system architectures, EMI/EMC, power quality, ac-dc converters, dc-dc converters, POL converters in applications including microprocessors, tablets, notebooks, desktops, servers, data centers, networking products, telecom equipment, solid state lighting, battery chargers, transportation, renewable energy, and other industrial and consumer electronic applications.

The PMC mini-consortium has accumulated a wealth of knowledge and made significant contributions to the power management industry. Since its inception, the program has been supported by more than 50 major semiconductor and power supply companies. PMC currently has 24 members. In the past year, FSP-Powerland Technology, GaN Systems, Jiangsu Wanbang Dehe New Energy, and Lite-On Technology Corporation have joined PMC.

The PMC places a significant emphasis on developing high efficiency, high-power density switch-mode power supplies based on recent developments in wide bandgap (WBG) power devices such as gallium nitride (GaN) devices and silicon carbide (SiC) devices. This emphasis is highly leveraged with the recent DOE award of "PowerAmerica." CPES is a partner in this multi-industry, multi-university collaborative program for a period of five years. The role of CPES is to work with the wide bandgap (WBG) manufacturing industry to explore potential applications and impacts of GaN and SiC devices on power conversion technologies.

Below are some highlights of our WBG-based research:

- High-frequency adapter with 40 W/in^3 power density and above 94 percent efficiency
- High-frequency 1 kW single phase PFC with 700 W/in^3 power density and 99 percent efficiency
- High-frequency 1 kW 400 V/12 V unregulated LLC converter with 900 W/in^3 power density and 98 percent efficiency
- High-frequency 3 kW 400 V/48 V isolated dc-dc converter with above 98 percent efficiency and 300 W/in^3 power density
- 48 V/12 V bus converter for telecom and server application with above 98 percent efficiency and 1600 W/in^3 power density
- High-frequency 48 V/1 V voltage regulator for server application with above 94 percent efficiency and 800 W/in^3 power density
- High-frequency 6.6 kW bidirectional on-board charger for plug-in electric vehicles with above 96 percent efficiency and 50 W/in^3 power density
- 25 kW battery charger with above 97 percent efficiency and 60 W/in^3 power density
- 25 kW PV inverter module with 99 percent efficiency and 120 W/in^3 power density

WORK SCOPE

- High performance VRM/POL converters
- High efficiency power architectures for laptops, desktops, and servers
- High frequency magnetics characterization and design
- High-efficiency and high-power density power supplies with wide bandgap power devices
- Digital control
- Power management for PV systems
- Power management for battery systems
- Power management for automotive applications
- Solid-state lighting
- EMI

PARTICIPANTS

PMC Members

3M Company
Analog Devices
Chicony Power Technology Co. Ltd.
CRRC Zhuzhou Institute Co. Ltd.
Delta Electronics
East China Research Institute of Microelectronics (ECRIM)
Efficient Power Conversion
Eltek
FSP-Powerland Technology Inc.
GaN Systems
Huawei / Futurewei Technologies Co. Ltd.
Infineon + International Rectifier
Intel
Inventronics (Hangzhou) Inc.
Jiangsu Wanbang Dehe New Energy Co. Ltd.
Lite-On Technology Corporation
Lockheed Martin Corporation
Murata Manufacturing Co. Ltd.
Navitas Semiconductor
NXP Semiconductors
ON Semiconductor
Panasonic Corporation
Silergy Corporation
Texas Instruments
Valeo
VERTIV

Research Team *February 2018 – February 2019*

Faculty

Fred C. Lee
Qiang Li

Graduate Students

Mohamed Ahmed
Syed Bari
Yinsong Cai
Chao Fei
Junjie Feng
Rimon Gadelrab
Yi-Hsun (Eric) Hsieh
Zhengrong Huang
Feng Jin
Owen Jong
Bin Li
Virginia Li
Zheqing Li
Xin Lou
Ahmed Salah Nabih
Tam Nguyen
Gibong Son
Qiong Wang
Shuo Wang
Hao Xue
Yuchen Yang
Chunyang Zhao
Feiyang Zhu

Visiting Scholars

Shaoling An
Minfan Fu
Ryo Kajitani
Lei Li
Phu Hieu Pham
Wei Qin
Hongfei Wu

Leveraged with Government Funding from:

PowerAmerica
DOE
NSF

High Density Integration (HDI)

HDI was created in 2011 as a mechanism for CPES and industry members to address emerging and long-term challenges in power electronic integration. While it is supported primarily by CPES membership, it also leverages sponsored research with major industries such as Delta, Dowa, GE, GM, Group Safran, Lockheed Martin, MKS, Nissan, Raytheon, Rolls-Royce, TI, Toyota, and UTRC, as well as with government agencies including the ARPA-E, NSF, DARPA, DOE, ONR, and the U.S. Army and Air Force. The tradeoffs among reliability, efficiency, cost, electromagnetic compatibility, power density, and speed are explored as new materials, components, circuits, and applications emerge.

The commercialization of wide bandgap semiconductor devices such as silicon carbide (SiC) and gallium nitride (GaN) has shifted switching frequency beyond tens of megahertz, power rating beyond megawatts, and junction temperature beyond 250° C. Ancillaries, characterization metrology, modeling method, packaging process, and manufacturing paradigm need to be transformed.

Unique high-temperature packaging technology is an example of CPES fulfillment of these critical needs to the future power electronics industry. HDI developed die-attach materials which can be processed at low temperatures, yet are reliable at the temperature of the wide bandgap junction. Processes were developed to encapsulate ultra-thin planar packages with polymer having high glass transition temperature and dielectric strength.

Magnetic materials with low core loss-density were synthesized from magnetic metals for additive manufacturing of high-frequency magnetic components. Inductors were fabricated from heterogeneous magnetic composites to shape the EMI spectrum. Over-molding magnetic materials have been synthesized for integrating energy storage and protection functions.

Techniques to decouple the noise loops have been identified to enable high dv/dt commutation in wide-bandgap switches. Design methodologies have been documented for high-temperature capacitors, power buses, protection, sensing, digital control, etc. New breeds of gate drivers, sensors, active filters, and passive filters have been demonstrated in a wide range of products, from power adapters to power electronic building blocks. Significant improvement in power density, efficiency, and signal integrity are expected thanks to the adoption of the technological advances. HDI tasks are scoped to advance wide bandgap systems, magnetic components, and module integration.

This current scope of work includes the following topics:

Wide Bandgap Systems

- Reliability study of failure mechanisms of GaN and SiC MOSFETs
- High-voltage high-temperature gallium-oxide diode
- Characterization of wide bandgap semiconductor switches up to highest voltage and temperature
- Short circuit protection design for paralleled GaN module high-density laptop adaptor
- High frequency, low loss soft-switched converters
- Insulation coordination study for high voltage high power density converter design

Magnetic Components

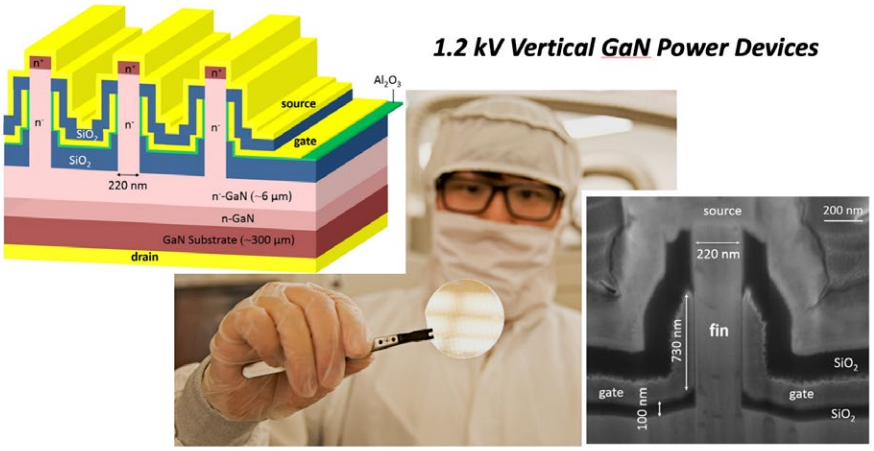
- Additive manufacturing of magnetic components
- Swinging and coupled inductors with heterogeneous magnetic cores
- Magnetic structures with high energy density
- Over-molding of encapsulating magnetics
- Low profile magnetic substrate
- Weakly coupled coils with low stray field for wireless power
- Integration of and field interaction in common-mode and differential-mode filters
- Integrated multi-phase inductor for voltage regulator for small portables
- PCB-integrated magnetics for high-efficiency, high-density front-end power supply
- Characterization of high-power inductors and materials
- High-frequency magnetic integration

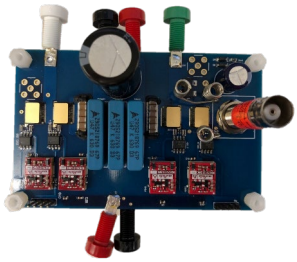
Module Integration

- Large-area substrate-to-substrate bonding by silver sintering
- Reliability evaluation of module interconnect
- Current sensor integrated with SiC MOSFET module
- High-voltage SiC module packaging
- Integration of magnetic dice into power module

WORK SCOPE

- Wide-bandgap devices
- Material and component characterization
- Active module integration
- High-frequency magnetic integration
- Converter integration
- Wide power range (10 W - 100 kW)
- High frequency (100 kHz - 10 MHz)
- High temperature ≥250° C





Dynamic R_{ds_on} Measurement

Overcurrent Protection Scheme Based on Parasitic Inductance of SiC MOSFET Power Module

PARTICIPANTS

HDI Members

Delta Electronics
Dowa Metaltech Co. Ltd.
Ford Motor Company
GE Global Research / GE Aviation
General Motors Company
Groupe SAFRAN
Huawei / Futurewei Technologies Co. Ltd.
Komatsu Ltd.
Lockheed Martin Corporation
Moog, Inc.
Nissan Motor Co. Ltd.
Texas Instruments
United Technologies Research Center

Leveraged with Gifts from:

ABB Inc.
LG Electronics
UTRC

Leveraged with Government Funding from:

PowerAmerica
ONR
ARPA-E
DOE

Research Team *February 2018 – February 2019*

Faculty

Dushan Boroyevich
Rolando Burgos
Christina DiMarino
Dong Dong
Mona Ghassemi
Fred C. Lee
Qiang Li
Guo-Quan Lu
Khai Ngo
Yuhao Zhang

Research Faculty

Igor Cvetkovic
Jun Wang

Graduate Students

Mohamed Ahmed
Chao Ding
Sarah El-Helw
Michael Emanuel
Chao Fei
Junjie Feng
Rimon Gadelrab
Shan Gao
Ting Ge
Nidhi Haryani
Joseph Kozak
Bo Li
Qian Li
Shengchang Lu
Zichen Miao
Ahmed Salah Nabih
Keyao Sun
Boyan Wang
Le Wang
Qiong Wang
Shuo Wang
Yue Xu
Yuchen Yang
Ruizhe Zhang
Tianyu Zhao

Visiting Scholars

Takashi Hirota
Takayuki Ikari
Toshihiro Kai

Wide Bandgap High Power Converters & Systems (WBG-HPCS)

Since its inception in 2011, this CPES mini-consortium program has provided a unique, open and collaborative forum for the power industry to explore, jointly with CPES researchers, new and emerging power conversion technologies to meet what are the ever-increasing energy demands of our modern society: WBG-HPCS looks at everything from power semiconductors, to gate drivers, to converters, down to the impact they can have on power systems.

As a mini-consortium, WBG-HPCS allows CPES to pool various resources seeking to develop the above pre-competitive technology. CPES is then able to address common industry challenges, and effectively share research results among its members while leveraging CPES's expertise in WBG-based power conversion and its vast knowledge of electronic power systems it has accrued over the past 30 years working with the transportation and IT industries. As a result, the WBG-HPCS mini-consortium has moved decisively into high-power medium-voltage applications for grid, industrial, and transportation applications.

In addition, CPES has continued to support research activities within the WBG-HPCS mini-consortium by securing funding, at the basic research level, from several government agencies, including the Office of Naval Research (ONR), the U.S. Department of Energy (DOE), DARPA, and ARPA-E. These agencies have been instrumental in the development of key enabling technology presently in use in WBG-based high power electronics applications, representing ideal partners that generate invaluable synergy within CPES in pursuit of the mini-consortium goals. As a result of this effort, CPES presently leverages strongly the WBG-HPCS funds, effectively quadrupling the research activity and the results that are shared with its members.

The WBG-HPCS current research thrusts are:

High-Power WBG-Based Power Converters

- High-frequency control of modular multilevel converters in ac-dc and dc-dc mode
- Design of SiC-based modular multilevel converters with 1.7 kV, 3.3 kV, and 10 kV devices (package, gate-drive, PEBB, converter, system)

WBG-Based Power Electronics Technology

- Characterization of MV SiC and LV GaN devices
- Development of EMI containment and suppression strategies for power converters, modular converters, and electronic systems
- Development of enhanced gate drivers and sensors for harsh dV/dt and electromagnetic interference (EMI) environments with advanced control capabilities

Renewable Energy Integration

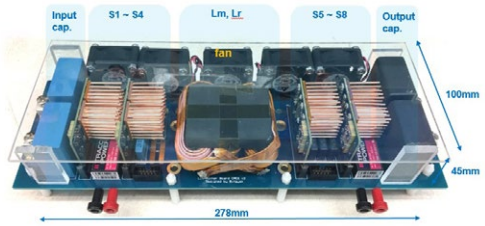
- Design of high-efficiency SiC-based grid-tied inverters for commercial PV applications
- Design of high-efficiency GaN-based grid-tied inverters for residential PV applications
- Static and dynamic impact of PV inverters in MV distribution systems

Stability and Dynamic Interactions in Power Converter Systems

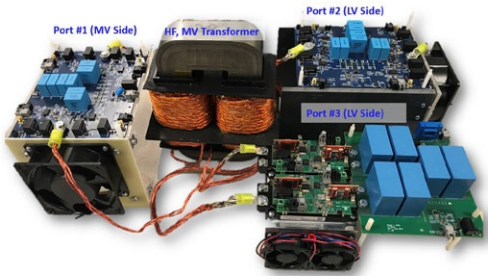
- SiC-based impedance measurement unit (IMU) for ac and dc LV and MV distributions systems
- Analysis of dynamic interactions between multiple STATCOM operating in proximity in HV transmission systems
- Stability assessment and interactions of utility-scale PV inverters in medium-voltage distribution systems
- Stability analysis in three-phase unbalanced systems and single-phase distribution systems
- Virtual synchronous machine modeling and converter control for grid-tied inverters

WORK SCOPE

- High-power WBG-based power converters
- WBG-based power electronics technology
- Renewable energy integration
- Stability and dynamic interactions in power converter systems



All-GaN-based 10 kW resonant converter



Triple active bridge hardware setup

PARTICIPANTS

WBG-HPCS Members

ABB Inc.
Delta Electronics
GE Grid Solutions
Huawei / Futurewei Technologies Co. Ltd.
Rockwell Automation
Siemens Corporate Technology

Leveraged with Gifts from:

ABB Inc.
Dominion Energy
United Technologies Research Center

Leveraged with Government Funding from:

ARPA-E (Advanced Research Projects Agency – Energy)
Office of Naval Research (ONR)
PowerAmerica Institute
U.S. Department of Energy

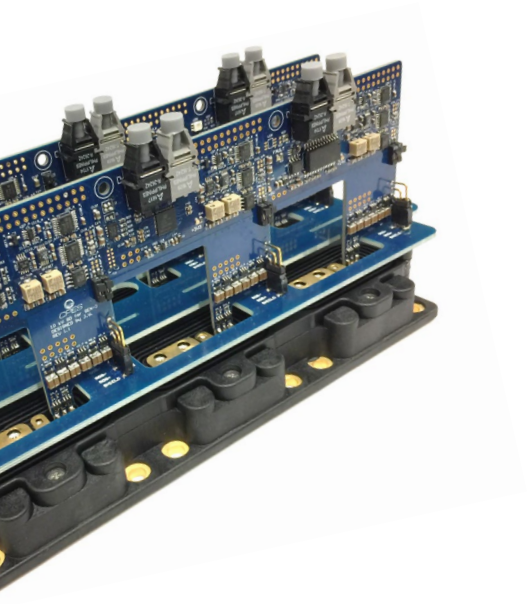
Research Team *February 2018 – February 2019*

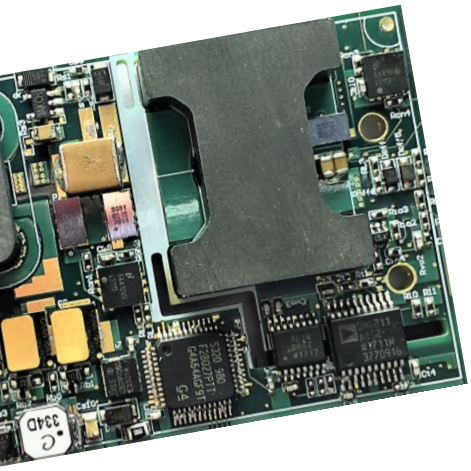
Faculty
Dushan Boroyevich
Rolando Burgos
Fred C. Lee
Qiang Li
Dong Dong

Research Faculty
Igor Cvetkovic
Jun Wang
Bo Wen

Graduate Students
Alexander Freeman
Nidhi Haryani
Yi-Hsun (Eric) Hsieh
Zhengrong Huang
Jiewen Hu
Chi Li
Slavko Mocevic
Tam Nguyen
Sungjae Ohn
Paul Rankin
Yu Rong
Rebecca Rye
Joshua Stewart
Bingyao Sun
Keyao Sun
Ye Tang
Qiong Wang
Jianghui Yu

Visiting Scholar
Boran Fan
Takahide Tanaka
Sizhan Zhou





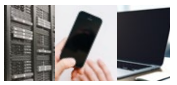
Research

In its effort to develop power processing systems to take electricity to the next step, CPES has cultivated research expertise encompassing five technology areas: (1) power conversion technologies and architectures; (2) power electronics components; (3) modeling and control; (4) EMI and power quality; and (5) high-density integration.

These technology areas target applications that include: (1) power management for information and communications technology; (2) point-of-load conversion for power supplies; (3) vehicular power converter systems; and (4) high-power conversion systems.

In 2018, CPES sponsored research totaled approximately $3.5 million. The following abstracts provide a quick insight to the current research efforts

Application Areas



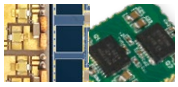
Power Management for Computers, Telecommunications, & Others

Vehicular Power Converter Systems

Point-of-Load Conversion

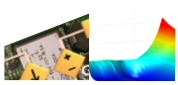
High-Power Conversion Systems

Technology Areas

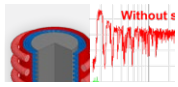


Power Conversion Topologies & Architectures

Power Electronics Components



Modeling and Control



EMI and Power Quality

High Density Integration

Sponsored Research

NSF Career—High Frequency Integrated Voltage Regulator to Support Dynamic Voltage and Frequency Scaling for Mobile Devices

Sponsored by: National Science Foundation

February 15, 2017–January 31, 2022

Voltage regulators have been widely used in computing systems to deliver power from energy sources from batteries to microprocessors. Today's voltage regulator is usually constructed using discrete components and assembled on a motherboard. Discrete passive components such as inductors and capacitors are bulky and occupy a considerable footprint on the motherboard. Furthermore, the power delivery path from the voltage regulators to the microprocessors is relatively long.

Recently there has been great demand for a very high-frequency integrated voltage regulator that can be placed very close to the microprocessor to support dynamic voltage and frequency scaling, which is a very effective power consumption reduction technique for microprocessors. This enables the supply voltage to change dynamically according to the microprocessor workload (decreased workload leads to a lower supply voltage; and a lower supply voltage also leads to a lower clock frequency). As a result, both the dynamic and static power consumption of the microprocessor can be greatly reduced. However, the traditional discrete voltage regulators are not able to realize the full potential of dynamic voltage and frequency scaling since they are not able to modulate the supply voltage fast enough due to the high parasitic interconnect impedance between the voltage regulators and the microprocessors.

This project focuses on developing a 20–50 MHz, three-dimensional integrated voltage regulator for mobile devices, such as the smartphone. The proposed research will have a significant impact on power management solutions for smartphones as well as other mobile applications. It will help make the integrated voltage regulator a feasible approach to significantly reduce mobile device power consumption, which will greatly extend battery life and reduce electricity consumption.

Education activities include outreach to K–12 and underrepresented groups to increase the attractiveness of power electronics.

High-Efficiency, Medium-Voltage-Input, Solid-State-Transformer-Based 400 kW/1000 V/400 A Extreme Fast Charger for Electric Vehicles

Sponsored by: Department of Energy, Sub-awardee of Delta Products Corporation

July 20, 2018 – November 30, 2021

CPES will work with Delta Products Corporation, General Motors, DTE Energy, Next Energy, Michigan State Energy Office, City of Detroit Sustainability office to deliver a novel, efficient, compact, and scalable SST-based 400 kW XFC. It will also provide a user-friendly dc interface for renewable energy generation systems (e.g. PV) and energy storage systems (ESS), resulting in less disturbance to the existing grid. This technology will enable large-scale XFC deployment. It will also accelerate EV market penetration and promote renewable energy usage.

The proposed 400 kW/1000 V/400 A Extreme Fast Charger (XFC) consists of two main function blocks: a solid-state transformer (SST) and a charger converter. The SST takes a 13.2 kV ac medium-voltage (line-to-line) and converts into a 1 kV intermediate dc bus voltage. The charger converter converts the 1 kV dc bus into the controllable dc-output voltage needed to charge an EV. The 1 kV intermediate dc bus is designed to interface with external renewable energy generation systems (e.g. PV) and ESS for load shaving and minimizing the demand charge. The bulky line frequency transformer (LFT) is eliminated in the proposed SST-based XFC system.

Developing the Future of Wide Bandgap Power Electronics Engineering Workforce – Wide Bandgap Generation (WBGen) Fellowship Program

Sponsored by: Department of Energy

January 1, 2015–July 31, 2021

The goals of the Wide Bandgap Generation (WBGen) fellowship program sponsored by the U.S. Department of Energy (DOE) are:

- To train the next generation of U.S. citizen power engineers with wide bandgap (WBG) power semiconductor expertise in anticipation of future workforce needs in this field
- To broaden the range of WBG-based power electronics by conducting research and development on high-efficiency grid apparatus and high-efficiency electrical power systems
- To enhance the power engineering curriculum by formalizing WBG-oriented design procedures for power electronics components and systems that can effectively integrate the inherent, challenging material characteristics of these devices, which have effectively rendered design procedures for silicon-based power electronics obsolete

The WBGen fellowship funded 6 fellows during its first year, and 11 students during its second year. It is expected that, over its 5-year tenure, the program will graduate 10 M.S. students and partially fund 6 to 8 Ph.D. students. This will not only have an immense impact on the success of the WBG research programs at Virginia Tech, but will consequently have immeasurably positive effects on the power engineering workforce over the next 5 to 10 years. Furthermore, the DOE and U.S. Department of Defense (DOD) laboratory and industrial partnership established in the traineeship will also benefit significantly from interaction with the participating graduate students, cementing what are already strong relationships

between the partners and CPES, and creating a solid network of power engineering training, research, and development.

So far, 12 WBGen fellows have joined the program, establishing partnerships with ABB Inc., General Motors (GM), United Technologies Aerospace Systems (UTAS), HRL Laboratories, the National Renewable Energy Laboratory (NREL), and VPT. Amy Romero, the first WBGen fellow who joined in January, 2016, graduated in February, 2017, earning her M.S. She is currently employed at Wolfspeed in Raleigh, North Carolina.

Power Conversion through a Novel Current Source Matrix Converter (PCTMXC)

Sponsored by: Advanced Research Projects Agency–Energy (ARPA-E), Sub-Awardee of United Technologies Research Center (UTRC)

May 14, 2018-April 6, 2021

UTRC proposed the novel solution of a matrix converter (MxC) with voltage boost capability that enables operation above 86.6 percent of input voltage and, thus, overcomes the main limitation of the traditional MxC. Specifically, the proposed MxC operates in a current control mode (CCM) in contrast to the traditional voltage control mode (VCM). UTRC's task is centered around the development of model-predictive control schemes for the MxC, which will further increase the benefits of the CCM MxC by improving its dynamic response. CPES has been tasked with the design, construction and testing of the MxC, three-phase to three-phase hardware, and control unit. The goal is to adapt its operation to the use of silicon-carbide (SiC) devices for fast switching frequency and commutation speeds. This is crucial given that the bulk of the work conducted in matrix-converter type solutions has been using IGBTs, and, hence, were not subject to the high-frequency operation challenges inherent to high-power SiC-based converters.

In the first year of this project, CPES has successfully demonstrated a modular power converter concept that maximizes power density while minimizing all critical parasitic inductances. It has also developed the digital control platform that will control the converter. The second year's effort will focus on the development of novel circuit assemblies to further reduce the impact of parasitic components, as well as on electromagnetic interference (EMI) suppression, mitigation, and containment.

Although the target applications of this proposal are aircraft power systems, the results will be applicable to the traditional VCM-MxC that is well suited for a broad range of industrial applications. Thus, the proposed program will facilitate wide penetration of MxC technology and WBG devices in the fields of energy generation, transportation and industrial applications.

High Power Density 10 kV SiC-MOSFET-based Modular, Scalable Power Converters for Medium Voltage Applications

Sponsored by: Advanced Research Projects Agency–Energy (ARPA-E)

February 26, 2018–February 25, 2021

The nearly ideal material properties of silicon-carbide (SiC) are transforming the design and manufacturing paradigm of power electronics. Specifically, pervasive dv/dt and di/dt rates, augmented electromagnetic interference (EMI) emissions, higher operating voltages and switching frequencies, and junction temperatures greater than 200° C have made apparent the need for the reformulation of design procedures developed for silicon (Si)-based power electronics, as well as for the materials, packaging and integration, and manufacturing technologies used. More so, the adequacy of existent circuit topologies is under scrutiny now, as their Si-optimized operation may impede the exploitation of the capabilities offered by SiC.

This last point is of special interest in medium-voltage (MV) and high-voltage (HV) applications, where multilevel converters and modular multilevel converters (MMC) have been developed to overcome the limitations of Si in terms of breakdown voltage, switching frequency, and efficiency. Expectedly, the use of SiC in these Si-optimized converters would yield minor gains, for which simpler two-level topologies have been pursued so far for 10 kV SiC MOSFETs. The latter promise direct connection to 4,160 V ac busses and increased power density by switching at 20–40 kHz. This is a glimpse of the potential offered by SiC.

Addressing the above, this is pursuing the development of modular power converters for MV applications optimized for SiC devices capable of achieving:

- Power density greater than 10 kW/l;
- Efficiency greater than 99 percent;
- Specific power greater than 10 kW/kg;
- Unrestricted current and voltage scaling; and
- Operation in both ac and dc power conversion modes.

Such flexibility can be attained by adopting an MMC-type circuit, but using previously untapped topological states of this converter. Two unique circuit operating modes are unveiled in this way: one enabling the switching-cycle control of the power-cell voltages, which effectively eliminates their line-frequency dependence; and one that inverts their operating mode allowing for the direct power flow between the converter input and output terminals without having to transiently store energy in the power cells. Both concepts have been extensively tested through simulations in applications of up to 120 power cells, but have yet to be demonstrated experimentally. This constitutes the main objective of the project that targets the development of 5 MW, 20 kV modular ac-dc and dc-dc power converters.

AMEBA Inverter

Sponsored by: Defense Advanced Research Projects Agency, Sub-Awardee of Rockwell Collins

September 1, 2017–June 30, 2018

Under the A Mechanically Based Antenna (AMEBA) Defense Advanced Research Projects Agency (DARPA) program, CPES sought to develop high power density, extreme efficiency GaN-based inverters to drive the motor used to move the mechanical antenna (magnet) in charge of generating electromagnetic fields. This type of antenna will enable mobile, low frequency, digital transmissions in radio-frequency-denied environments, such as underwater and underground, in addition to long-range communication. To this end, wide-bandgap power semiconductors, specifically gallium-nitride (GaN) semiconductors, were used to implement the power electronics inverter. These devices, with their superb material properties, enable switching frequencies of 1 to 2 higher order of magnitude when compared to state-of-the-art silicon (Si) devices. This allows power density to be maximized while still increas-

ing efficiency. Their higher operating temperature also minimizes the cooling system requirements, and their smaller footprint mitigates conducted electromagnetic interference (EMI) emissions. Accordingly, this project proposed an integrated power modulator unit achieving 98 percent
efficiency and a power density of 8 W/cm^3 (131 W/in^3), while switching at 100–300 kHz and operating at a semiconductor junction temperature of 150° C

Development of a P-HIL System Emulator for Aerospace Electrical Systems

Sponsored by: EGSTON Power Electronics GmbH

December 1, 2018-November 30, 2019

EGSTON has approached CPES seeking to develop a system simulation platform for aerospace electrical systems using the EGSTON COMPISO System Unit (CSU) CSU200-6AMP P-HIL that is currently in the CPES laboratory at the Virginia Tech Blacksburg campus. The goal is to implement the components and system models of a number of test scenarios that have been previously defined by EGSTON in collaboration with the aerospace industry, seeking to demonstrate the capabilities of the CSU to perform power hardware-in-the-loop (P-HIL) simulations in these environments. The objectives of this project are to develop the necessary models to demonstrate the CSU capability to simulate, in P-HIL mode, components and electrical systems in aerospace applications. The specific models and test scenarios will be defined in collaboration with EGSTON, Boeing, and potentially other aerospace industry members.

Soft-Switched Series-Capacitor Buck Converter (SCBC) for 48 V-54 V Power Delivery

Sponsored by: Texas Instruments Incorporated

November 1, 2018 – October 31, 2019

The fellowship program is established to support research in power delivery for data centers. As current requirement exceeds 200 A, the 12 V architecture for power delivery incurs excessive loss. A voltage regulator module with 48 V bus voltage is introduced as a candidate to achieve high efficiency and high power density for datacenter applications. A soft-switched Series Capacitor Buck Converter (SCBC) is proposed for a two-stage architecture for 48 V – 1 V power delivery with high efficiency, high power density and low noise. Compared with series capacitor buck converter (SCB), it achieves soft-switch with a wide and variable gain range. The solution is evaluated as the front end of the two-stage solution.

Development of Impedance Measurement Unit for 1 kV DC and 800 V AC Systems

Sponsored by: Newport News Shipbuilding

August 31, 2017 – September 30, 2019

Newport News Shipbuilding (NNS) has approached CPES with the purpose of developing two medium-voltage (MV) impedance measurement units (IMU) for three-phase ac and dc electrical systems. NNS engineers have worked jointly with the team at CPES to ensure an expedient technology and knowledge transfer for the project. Phase I will develop a new IMU rated at 1 kV dc, 800 V ac, with an injection capacity of 200 kW and an impedance measurement bandwidth spanning from 10 Hz to 1 kHz. Phase II, to be conducted later, would develop a higher power IMU rated for 12 kV dc, 6.9 kV ac, with an injection capacity of 1 MW in the same frequency range. The main measurement and operating mode under consideration is shunt IMU connected in parallel to the system, but the units will also be capable of series operation.

In response to the Phase I specifications, this project proposes to develop a single-phase, modular IMU with 1 kV, 200 kW capability, based on the CPES-developed IMU for 4,160 V ac networks that used 10 kV silicon-carbide (SiC) devices, and the power electronics building block unit PEBB 1000, a 50 kW, 1 kV dc power module with a switching frequency of 100 kHz built with 1.7 kV SiC MOSFET devices. The single-phase, modular IMU architecture will require the least number of modules to conduct measurements in both three-phase ac and dc systems, enabling the measurement of three-phase ac impedances under unbalanced conditions, as well as the measurement of zero-sequence and ground impedances.

The project has successfully demonstrated a newly-designed PEBB 1000 unit rated at 200 kW and is currently constructing three additional units. A new distributed control system has been developed, as well, featuring nanosecond-range synchronous communications over a fiberoptic network, which will be expandable to enable the control of the prospective medium-voltage 1 MW IMU unit. A new PEBB unit with active energy storage has also been conceived, demonstrating a nearly 50 percent reduction in the volume of capacitors needed per PEBB.

Direct-to-Line Central Inverter for Utility-Scale PV Plants Using 10 kV SiC MOSFET Devices

Sponsored by: Department of Energy through PowerAmerica Institute

July 1, 2018-June 30, 2019

This project is developing a direct-to-line central inverter block for photovoltaic (PV) applications using 10 kV silicon-carbide (SiC) MOSFET devices, rated for 200 kW, 11 kV ac, 16 kV dc, and a ±0.8 power factor. Targeting a California Energy Commission (CEC) efficiency of 99 percent, and a specific power of 5 kW/kg, the proposed project will seek to minimize the system complexity by adopting the simplest three-phase topology to realize the inverter. To this end, a two-level and a three-level active neutral-point-clamped (A-NPC) inverter have been considered and evaluated at the design stage in terms of efficiency, common-mode (CM) and differential-mode (DM) electromagnetic interference (EMI) emissions, size of EMI and power quality filters, specific power, leakage current, and fault handling capability.

To attain the medium-voltage rating, two series-connected MOSFET devices will be used in the main phase-leg construct of the two-level converter in what is an equivalent 20 kV SiC "switch". To demonstrate the proposed central inverter concept, the project will carry out the electro-thermal design, building and testing the inverter under laboratory conditions. In order to disclose and potentially transfer the proposed technology to the U.S. power industry, this project will specifically collaborate with ABB, conducting a design review of the proposed converter and demonstrating its performance to ABB scientists, as well as to other power industry partners, including General Electric and Rockwell Automation, with whom the principal investigators are conducting similar research.

Power Integration by Multifunctional Molding

Sponsored by: National Science Foundation

August 1, 2015–June 30, 2019

A process called "over-molding" was demonstrated for fabricating/integrating the inductor in a power module. The winding was first attached to the substrate already carrying the semiconductor and capacitor chips. Magnetic paste was then injected into the unused space that is normally occupied by the encapsulant and is cured under atmospheric pressure below 250° C to realize the core, achieving a permeability above 20. A power converter with input of 12 V, output of 1.2 V at 5 A, and switching frequency of 500 kHz was constructed to check the operation with a 1.1 μH over-molded inductor. The over-molded magnetic material did not adversely interfere with converter operation; switching noise was low. The maximum temperature of 48.3° C and full-load efficiency of 82 percent are similar to those of the same circuit using a discrete inductor. Effort is under way to replace the molding process by 3D printing to improve controllability and repeatability. One challenge is to keep the walls of tall structures from slumping. Another challenge is to print multiple layers of magnetic, conductive, and insulating materials, all of which should incur minimal loss at high frequency. Feedstocks are being developed along with control algorithms and settings for 3D printers of a commercial partner.

Medium Voltage AC to Low Voltage DC Power Conversion for Data Center

Sponsored by: Department of Energy through PowerAmerica Institute

July 1, 2018–June 30, 2019

Due to the increasing use of cloud computing and bag data, the power consumption of data centers alone will reach 10 percent of the total electrical power consumption in the world by 2020. The conventional ac data center power architecture has too many stages, which cause excessive power loss in power distribution. Furthermore, in current ac data center power architectures, a line frequency transformer is employed to step down medium voltage ac to 480 V ac and distribute 480 V throughout the facilities. With ever-increasing power consumption of mega-data centers, presently, the 480 V ac lines carry thousands of amperes of current. This leads to very bulky and costly transmission bus and large conduction losses within the data center.

In this work, we will develop a SiC and GaN based high frequency rectifier to directly step down 4.8 kV ac to 380 V dc. The 380 V dc bus is distributed directly to server cabinets. Inside the server cabinet, the 380 V dc will be further step down to 48 V dc. The 48 V dc will be used as distribution bus inside the server cabinet. The proposed system will not only eliminate the use of a bulky 60 Hz transformer, but also eliminate several series connected power stages in current data center architecture, greatly reducing power conversion loss. Furthermore, the 4.8 kV ac can be used as distribution bus within data centers instead of 480 V ac. By doing so, the use of copper (an increasingly more expensive commodity) will be reduced by 90 percent. At the same time, distribution-related conduction loss will also be reduced by a factor of 10. In total, the proposed system can save more than 15 percent of the energy consumption in the data centers. Also, by eliminating the bulky 60 Hz transformer, the proposed architecture is easily scalable.

The proposed MV ac to 380 V dc rectifier has cascade H-bridge with high-frequency isolated dc-dc converters. The inputs of H-bridges are in series and the outputs of the dc-dc stages are connected in parallel. The proposed 380 V to 48 V converter will be built with GaN devices and operated at MHz range with soft-switching. Transformers and inductors of this converter will be integrated and built with PCB winding to enable automatic manufacturing.

Small Motionless Antenna with Reconfigurable Transmission

Sponsored by: National Science Foundation

May 15, 2018-April 30, 2019

Search and detection in the wake of a hurricane has been hindered by the absence of a compact means for underwater communication. The very-low frequency (VLF) band between 1 and 30 kHz can be utilized for transmission of electromagnetic wave in this and other challenging environments. The transmitter is usually large and heavy owing to the long VLF wavelength. The small motionless antenna with reconfigurable transmission (SMART) is envisioned to be a portable transmitter emitting a rotating/pulsating/swirling magnetic cloud. It relies on "variable material" realized by current-driven saturable magnetism. It enables a new type of communication named "spin modulation" (SM) that complements the well-known frequency modulation (FM) and amplitude modulation (AM).

The basic SMART cell is a loop comprising a permanent magnet, a yoke with relative permeability of 20, and a current-controlled flux "shutter." As the control current increases from zero, the shutter's relative permeability decreases from 20 toward 2 to let more flux emit from the magnet. An array of basic cells and the associated control currents will generate a spinning magnetic cloud. Simulation suggests that 100 fT (femto-Teslas) at 1 kHz would be detected at 100 m away from a demonstrative prototype using commercial materials with dimensions of 150 x 95 x 30 mm^3.

Tunable Energy Efficient Electronics (TE3)

Sponsored by: Defense Advanced Research Projects Agency

December 1, 2015–March 31, 2019

Power passives realized from magnetic and dielectric materials are an integral part of power processing with high performance, light weight, and high efficiency. A majority of applications often require power processors to operate with a fluctuating source, load, or environment. Passive components with added tunability are sought to provide adaptability to different circuit conditions. Inductance in point-of-load power supplies can be increased by an input voltage to reduce switching loss at light load, or decreased to supply load transient in the absence of a large capacitive filter. Compensating capacitance in wireless power transfer can be varied to flatten the efficiency curve with the coils' separation or misalignment. The input impedance of a transformer driving a light-emitting diode can be tuned to be resistive to maintain the unity power factor, without a separate boost converter. The new components revolutionize not only the power passives themselves, but also power conversion systems and the education of electrical engineers.

Highly Integrated Wide-Bandgap Power Module for Next Generation Plug-In Vehicles

Sponsored by: Department of Energy, Sub–Awardee of General Motors Corporation

March 1, 2016–March 31, 2020

The main objective of the project is to research, develop, and demonstrate a highly integrated wide-bandgap (WBG) power module targeting the next generation plug-in vehicles, optimized for General Motors (GM)'s traction inverter architecture, meeting or exceeding U.S Department of Energy (DOE)'s specific power, power density, and cost targets of 14.1 kW/kg, 13.4 kW/L, and 3.3 USD/kW, respectively. To this end, CPES has conducted the static and dynamic characterization of silicon-carbide (SiC) devices from numerous vendors, focusing primarily on the 10 mΩ Gen 3 900 V SiC MOSFET from Wolfspeed and 10 mΩ 1.2 kV SiC MOSFET from Monolith, evaluating the inherent performance of these devices to support the development of high-current 900 V power modules.

Specifically, CPES has conducted an exhaustive short circuit characterization that showed the significant withstand time that these devices have (4-5 μs). CPES has also developed an enhanced gate-driver for the SiC power module using its advanced electromagnetic interference (EMI)-suppression and sensing and protection technology. This new gate driver uses integrated Rogowski current sensors to measure the current through the switches of the half-bridge module, reconstructing in its local field-programmable gate array (FPGA) the phase current of the module to eliminate the need for external sensors. The switch-level measurement is also used for short-circuit protection purposes, where CPES demonstrated the advantages of using current-based protection to replace traditional desaturation-detection-based schemes developed for Si-insulated gate bipolar transistor (IGBT) devices. Further, in support of the full-current module, CPES has evaluated several Ag pastes and preforms for large area sintering as well as alternative direct-bonded copper (DBC) and direct-bonded aluminum (DBA) ceramic substrates with Ag and Au coating, developing sintering profiles in order to attain a die shear strength in excess of 30 MPa. Temperature cycling tests have been conducted, as well, to assess the reliability of the methods and materials in question, which so far have exceeded 2,000 cycles without exhibiting any degradation. Furthermore, CPES has developed a 5 mΩ SiC MOSFET package in half-bridge configuration, rated at 900 V and 200 A, featuring ultra-low parasitic inductances in the module power and gate loops, for which flexible printed circuit board (Flex-PCB) circuits have been adopted for the latter. The power module will, in addition, be used to assess the current sharing capability of the Gen3 SiC MOSFET devices from Wolfspeed, and to conduct power cycling reliability testing.

Next Generation Electric Machines Program

Sponsored by: Department of Energy, Sub-Awardee of General Electric Global Research

October 6, 2016–April 30, 2019

In this project, CPES has been tasked with the development of gate-driving solutions to enable the direct stacking, or series-connection, of high-current 1.7 kV SiC MOSFET power modules from General Electric (GE) in support of the development of a medium voltage silicon-carbide (SiC)-based motor drive under the U.S Department of Energy (DOE) next-generation electrical machine (NGEM) program. GE has already completed comparative analysis of SiC switches in series connection, demonstrating the potential advantages of adopting such configuration as opposed to using a single, higher blocking voltage device. In its first year of execution, CPES developed a successful active-control mechanism to achieve the unrestricted series connection of SiC MOSFET power devices, demonstrating the operation of a 400 A 1.7 kV power module as a single 400 A 3.4 kV SiC MOSFET. The mechanism in question uses closed-loop control to regulate the turn-off speed of the devices to ensure the perfect balancing and dynamic voltage sharing between the stacked devices. CPES also investigated the numerous mechanisms that govern the inherent unbalanced operation of SiC MOSFET devices, identifying the parasitic capacitances to ground and the high dV/dt voltage slew rates (greater than 20 V/ns) as the main culprit. This is as opposed to the unbalance exhibited by stacked Si IGBT devices, which are primarily affected by gating signal offsets and the tolerance between device parameters. CPES is currently testing the connection of four modules, totaling eight series-connected or stacked MOSFET devices, in what would be an equivalent 10–12 kV "switch".

Highly Integrated Innovative Power Converters

Sponsored by: Carrier Corporation

August 15, 2017–April 30, 2019

Carrier, from United Technologies Corporation (UTC), approached CPES to investigate new inverter power conversion solutions in high-speed compressor motor drives for compact air conditioning systems (ACS), with the goal to attain high power density and high efficiency using new advanced integration technologies. Specifically, the high-speed inverter targeted 5 kW three-phase permanent magnet (PM) motor drives rated at 230 V rms line voltage and 2.5 kHz. To this end, CPES proposed the use of silicon-carbide (SiC) devices and the adoption of novel 5-level voltage-source inverter topologies seeking to, in addition, reduce the dv/dt stress on the electrical motor and mitigate electromagnetic interference (EMI) emissions. As a result, operating frequencies of up to 3 kHz have been achieved, with a switching frequency in the 40–70 kHz range, and an efficiency of 99 percent. New design methodologies for the 5-level topologies have been developed, as well, transforming these formerly medium-voltage circuits into ones favoring fast switching frequency and fast commutation speeds. This make feasible the adoption of SiC maximizing the benefits offered by this power conversion technology. A design and physical layout pursuing ease of manufacturing for the inverter prototype was also conducted.

Highly Integrated Innovative Power Converters

Sponsored by: Otis Elevator Corporation

August 15, 2017–April 30, 2019

OTIS, from United Technologies Corporation (UTC), approached CPES to express its interest in developing new power conversion solutions for commercial elevators. Specifically, three-phase active front-end (AFE) converters for elevator motor drives were investigated in the 5–10 kW range, rated at 480 V ac, 800 V dc. To achieve the desired performance, UTC wanted to explore the use of wide bandgap (WBG) power semiconductors, which — in this power and

voltage range — would imply the adoption of silicon-carbide (SiC), as well as the use of planar printed-circuit-board- (PCB) based magnetics, functionally integrated magnetics, and multichannel power conversion. CPES proposed the use of a new interleaved triangular conduction mode (iTCM) PWM technique for three-phase power converters, achieving zero-voltage switching (ZVS) at turn-on for all SiC MOSFETs, while effectively decoupling the operation of converter phase-legs without sacrificing voltage-gain, and minimizing the control system complexity. Achieving a switching frequency in the 200–300 kHz range, the converter efficiency exceeded 99 percent, and reduced the size of boost inductors, enabling the use of planar PCB-based magnetics to implement them. The adoption of an integrated high-bandwidth current transformer sensor and the use of a dual-mode analog-digital control platform v was critical to achieve the goals. In addition, a design and physical layout pursuing ease of manufacturing for the AFE converter prototype was conducted.

Electric Ship Research and Development Consortium

Sponsored by: Office of Naval Research, Sub-Awardee of Florida State University

August 1, 2016–July 31, 2021

CPES will continue supporting Office of Naval Research (ONR)'s mission by participating as a member of the Electric Ship Research and Development Consortium (ESRDC), a multi-university consortium led by Florida State University. Within this framework, CPES will work on the demonstration of power electronics building block (PEBB) 1,000-based power converters and systems, for which it is currently developing an updated version of the PEBB 1000 unit built with 1.7 kV SiC MOSFET devices. It will continue working on the impedance measurement unit (IMU) previously developed for ONR using 10 kV SiC MOSFET devices and a multi-megawatt converter capable of operating from 4,160 V ac and 6,000 V dc networks, to measure the terminal impedances at interfaces of interest, with the purpose of assessing the stability conditions of the electrical system. The focus of this work will be to improve its electromagnetic compatibility (EMC), necessary to operate with the fast-switching 10 kV devices in place.

CPES is also supporting the electric ship design, modeling, and simulation effort within ESRDC by integrating the modeling of power electronics systems, taking into consideration parametric and model-form uncertainties during the process with which improved and optimum designs will become feasible using the PEBB models developed. Finally, based on its past experience on PEBB plug-and-play converter systems, CPES has started working on the development of an advanced controls and communication network with nanosecond synchronization capacity based on the White Rabbit project. This network will allow for a large number of PEBB to operate in unison under a distributed control architecture, which is a fundamental requirement for medium-voltage and high-voltage applications that could encompass several, or as many as hundreds, of PEBB devices in one converter station.

High Frequency GaN Power Converter

Sponsored by: Department of Energy through PowerAmerica Institute, Sub-Awardee of Lockheed Martin

July 1, 2017–June 30, 2018

The demands for 48 V/12 V intermediate bus converters have grown rapidly in recent years, including but not limited to telecommunications, data centers, automotive, industrial, and aerospace applications. Today's most intermediate bus converters are running at relatively low frequency and are built with discrete magnetic components. Manufacturing and assembling this power supply is labor intensive. Forty percent of the components are manually inserted; thus, the manufacturing of switching power supplies are largely moved off shore to countries with low labor costs. This trend will not reverse unless there is a paradigm shift in the way we design and manufacture these power supplies.

In this project, we propose to develop a high-efficiency high-density 1 kW gallium nitride (GaN) based MHz 48 V/12V intermediate bus converter, which also can be manufactured automatically. We will consider two system architectures: variable frequency single-stage architecture and fixed frequency two-stage architecture. It is anticipated that the single-stage can achieve peak 97 percent efficiency with 700 W/in^3 power density, and the two-stage architecture can achieve peak 95 percent efficiency with 550 W/in^3 power density. The potential benefit of the two stage solution is that it may have better electromagnetic interference (EMI) performance and a simpler filter design due to fixed switching frequency.

48 V/12 V Module

Sponsored by: Valeo

May 1, 2017–April 30, 2018

The power system inside next-generation vehicles is moving from 12 V to 48 V for the purpose of larger energy storage and higher output power. The implementation of such a power system requires a high efficiency and high power density 48 V-12 V bidirectional dc-dc converter to efficiently transfer power between the two voltage levels.

By adopting gallium nitride (GaN) devices, a 3.5 kW dc-dc converter using a multiphase structure operating at several hundred kHz will be built for the target application. In addition, printed circuit board (PCB) winding-based coupled inductors will be implemented to further reduce the loss and shrink the volume of the whole converter. As a result, 98 perent peak efficiency with 120 W/in^3 power density is expected.

High-Efficiency Modular SiC-based Power-Converter for Flexible-CHP Systems with Stability-Enhanced Grid-Support Functions

Sponsored by: Advanced Research Projects Agency–Energy (ARPA-E)

October 1, 2018–December 31, 2019

This project proposes to develop a modular, scalable MV power converter featuring stability-enhanced grid-support functions for future F-CHP systems operating in small- to mid-size U.S. manufacturing plants being fully compliant with the IEEE Std 1547 and IEEE Std 2030.7. To this end, a modular circuit topology will be adopted based on 10 kV SiC MOSFET devices, achieving an effi-

ciency greater than 98 percent, and a power density greater than 10 kW/l. As such, the proposed converter will not just profit from the high blocking voltage capability of these devices, but also from their inherent high efficiency and from their high switching frequency capacity. The latter will be enabled by a control scheme developed at CPES that can balance the converter capacitor voltages on a switching-cycle basis. Further, the voltage and current scalable capacity of the proposed converter will render it an appropriate solution for 1–20 MWe F-CHP systems, which typically operate in the 2–13.8 kV voltage range.

For demonstration purposes, a scaled-down modular power converter based on 1.7 kV SiC MOSFET devices, and rated at 480 V ac, 60 Hz, 200 kW, and 150 kVAr (±0.8 power factor), will be used to evaluate the converter operation and key performance metrics. These will be extrapolated to the MV solution using the ongoing work at CPES on the development of 10 kV SiC MOSFET-based modular power converters for MV grid applications. The converter prototype will be evaluated using an Egston P-HIL test bed rated at 480 V and 250 kW, which will emulate both the CHP generator and the microgrid environment for the F-CHP. A Siemens SICAM A8000 microgrid controller will be connected to the P-HIL unit and to the converter prototype, and will be used to direct the operation of the emulated microgrid and to demonstrate the grid-support functionality of the converter in compliance with the IEEE standards in question.

The proposed converter and control system will be able to measure the grid and its own terminal impedance, which will allow it to implement the stability-enhanced grid support functions. Accordingly, the converter will be able to:

- Operate in over-excited and under-excited reactive power generation mode;
- Participate in voltage regulation under constant power factor, voltage-reactive power, active power-reactive power, and constant reactive power modes, and also by adjusting its active power generation as a function of voltage;
- Respond to abnormal conditions;
- Participate in frequency regulation;
- Operate in and detect both unintentional and intentional islanding conditions;
- Monitor grid stability conditions;
- Use grid-forming controls; and
- Monitor the microgrid with a GPS-synchronized integral μPMU module.

Dominion Energy Fellowship

This fellowship program has been established to investigate the dynamic interactions that can arise when multiple static synchronous compensator (STATCOM) units operate in proximity in the transmission grid (200–500 kV ac lines), as well as to investigate the impact that photovoltaic (PV) inverters in utility-scale PV generation farms can have on the distribution grid. The results obtained so far have demonstrated the possibility of dynamic interactions leading to voltage instability phenomena in the case of the multiple STATCOMs when these units operate within 100 miles of each other. The main trigger of these interactions has been shown to be the ac voltage loop of the STATCOMs, yet their current and synchronization loops play a similar role, too. It was also shown that the higher the number of STATCOM operating in proximity, the easier it is for the interactions to ensue. Regarding PV inverters, the work conducted has demonstrated the significant impact that the specific control scheme of these units can have in triggering interactions within the distribution grid. Specifically, it has been shown the detrimental effect that reactive power compensation schemes directly regulating the terminal voltage of the inverters can have, which illustrates how compliance with the IEEE Std. 1547 must not only consider the static requirements imposed by it, but also take into consideration the dynamic response of PV inverter units. This is crucial to maximizing active power generation within the physical limits of the distribution grid operating conditions. To this end, a CPES-developed impedance measurement unit (IMU) has been used to validate all theoretical findings thus far.

ABB Fellowship

This fellowship program has been established to investigate the high-power handling capability of gallium-nitride (GaN) power semiconductors (650 V, 25 mΩ), for which a 10 kW test bed was developed. Specifically, an LLC-type resonant converter with variable switching frequency (200–500 kHz) and rated at 500 V dc has been successfully demonstrated. To this end, CPES has explored the design of high-current half-bridge modules with multiple GaN enhancement mode high electron mobility transistors (e-HEMT) in parallel, demonstrating a 650 V, 200 A capability so far. CPES is currently focused on characterizing the dynamic R_{dson} impact on the design of the power converter, as well developing new packaging concepts to test 12 m, 650 V GaN dies from GaN systems.

LG Electronics Fellowship

This fellowship program was established to investigate alternative short-circuit protection mechanisms for high-current 1.2 kV silicon-carbine (SiC) power modules operating in high ambient temperature conditions, given the distinct saturation characteristics and temperature dependence that SiC MOSFETs exhibit when compared to silicon (Si) insulated gate bipolar transistors (IGBTs). The approach pursued was to use the parasitic loop inductance of the package to detect both short-circuit events and over-current conditions. The methods developed have been successfully demonstrated in a 60 kW inverter operating in 100° C ambient conditions.

United Technologies Research Center Fellowship

This fellowship program sought during its first year to develop multi-objective design optimization methodologies for power electronics converters, taking into consideration parametric and model-form uncertainties. The design techniques developed have built on CPES's previous efforts designing high-power density and extreme efficiency power converters. The quantification of these uncertainties has been essential to achieve a robust optimum design accounting for the errors introduced naturally by parametric tolerances and by the inherent accuracy of the numerous electromagnetic and mechanical models used in the optimization process. Results obtained on a three-phase Vienna-type rectifier have been successfully used to validate the theoretical findings. During the fellowship's second year, research efforts have been redirected toward the development of 1.2 kV SiC MOSFET power modules capable of operating in 250° C ambient temperature,

reaching junction temperatures of up to 300° C.

PowerHub Fellowship

This fellowship program was established with the purpose of investigating extreme efficiency dc-dc power conversion solutions for renewable energy applications requiring galvanic isolation to meet safety regulations. To this end, a 25 kW CLLC fully bidirectional power converter with a high-frequency transformer operating at 250 kHz was developed, demonstrating a record 98.5 percent efficiency, a power density of 78 W/in^3, and using 900 V and 1.2 kV discrete SiC MOSFET devices.

100 kW Commercial PV Inverter with Efficiency > 99 % Operating in Interleaved Triangular Conduction Mode (iTCM)

PowerAmerica Institute

July 1, 2017-June 30, 2018

The development of three-level 1.2 kV semiconductor power modules in Si, hybrid Si-SiC, and SiC has made possible the adoption of three-level power converter topologies in a broad range of applications. These applications readily benefit from the inherent advantages that three-level converters offer when compared to their two-level counterparts: namely, higher efficiency, improved power quality, and lower EMI emissions. Similarly, the use of triangular current or triangular conduction mode (TCM), originally developed for low-power dc-dc and single-phase power factor correction (PFC) converters as a more effective extension of critical conduction mode, has been increasingly adopted in higher power single-phase and three-phase applications, seeking the efficiency gains attained by eliminating the turn-on losses of power devices. SiC MOSFET devices, with their capacitive nature, are a natural fit for this type of zero-voltage switching (ZVS) resonant operation, which has been the main driver behind the adoption of TCM in higher power applications.

To this end, this project developed a high-efficiency 40 kW, three-phase PV inverter capable of operating in direct-to-line or transformer-less mode for commercial applications, featuring an average efficiency greater than 98 percent, a power density greater than 100 W/in^3, and a specific power greater than 10 kW/kg, while limiting the ground-leakage current to less than 300 mA. It used 1.2 kV SiC MOSFET modules in neutral-point-clamped (NPC) configuration, configured in a triple-channel three-level circuit topology, operating in interleaved triangular conduction mode (iTCM). The use of the newly-developed iTCM scheme provided a significant boost in efficiency and power density by enabling the inverter operation to delve into switching frequencies exceeding 100 kHz, as well as by the effective elimination of its turn-on switching losses. Further, the use of the three-channel interleaved topology helped constrain the conduction loss increase due to the higher ripple content of its output currents.

Development of an Integrated Power Supply with PCB-Embedded Transformer for SiC Gate-Driving Applications

LG Electronics

June 4, 2018-July 31, 2019

LG Electronics approached CPES to develop a dual-output 10 W gate-driver power supply for wide-bandgap- (WBG) based three-phase inverters for automotive applications capable of operating at ambient temperatures from –40° to 125° C. To this end, CPES proposed to develop a high-power density, high-efficiency power supply with PCB-embedded high-frequency transformer, using GaN power devices operating at 1 MHz, featuring a minimized input-output capacitance targeting less than 3 pF. The latter is essential to operate in WBG converter environments and effectively block the conduction of common-mode EMI currents to ground that are generated by the fast dv/dt switching transients. This power supply will be built and tested demonstrating its capability to meet the objectives set forth and its compliance with all applicable standards.

Development of the PEBB 6000 Using Gen3 10 kV, 240 A SiC MOSFET Modules in Full-Bridge Configuration

Sponsored by: Office of Naval Research

December 1, 2017-31 December 2019

After many years of sustained support from the U.S. Department of Defense, especially the Office of Naval Research (ONR), a revolutionary new silicon-carbide (SiC) power semiconductor device was developed by Wolfspeed (formerly Cree), currently under production in 10 kV, 240 A SiC MOSFET half-bridge modules. As such, for the first time in history, a fully qualified, properly packaged, megawatt-scale semiconductor device capable of switching at frequencies above 20 kHz, with very high efficiency, is available. Coupled with new developments in modular multi-cell power converters, this device is expected to completely transform the world of medium voltage (MV) high-power electronics.

Under the sponsorship of ONR, CPES has developed and demonstrated the operation of the first SiC-based PEBB rated at 6 kV, utilizing the second generation 10 kV, 120 A, SiC MOSFET half-bridge modules from Cree/Powerex/GE. More recently, CPES has also developed an advanced gate-driver for these modules with enhanced functionality and EMC capabilities. In addition, CPES has recently completed the initial development of the SiC-based PEBB 1000, based on 1.7 kV SiC power modules from Wolfspeed. Utilizing the knowledge from these three efforts, this new project has sought to demonstrate for the first time a full-bridge, self-contained, SiC-based least replaceable unit (LRU) rated at 1 MW, 6 kV and 20 kHz. Dubbed the PEBB 6000, this unit will feature a power density of 10 MW/m^3, 99 percent efficiency, zero conducted EMI emissions, a 30 kV partial discharge inception voltage, and a 0 V enclosure potential. The proposed program will develop two PEBB 6000 units over a time span of 36 months, formulating the high-power density design methodology to achieve the set targets, evaluating its electrothermal performance, and assessing the impact of their operation in PEBB-based power converters and systems.

Intellectual Property

U.S. Patents Awarded

VTIP 12-044
Energy Storage for Power Factor Correction in Battery Charger for Electric-Powered Vehicles
Khai Ngo, Hui Wang
U.S. PATENT: 9,914,362
Issued: March 13, 2018

VTIP 16-110
Method and Apparatus for Current/Power Balancing
Chi-ming Wang, Yincan Mao, Zichen Miao, Khai Ngo
U.S. PATENT: 9,923,560
Issued: March 20, 2018

VTIP 14-053 (combined with 14-147)
Power-Cell Switching-Cycle Capacitor Voltage Control for Modular Multi-Level Converters
Jun Wang, Rolando Burgos, Dushan Boroyevich, Bo Wen
U.S. PATENT: 9,966,874
Issued: May 8, 2018

VTIP 16-005
Power Switch Drivers with Equalizers for Paralleled Switches
Lujie Zhang, Zichen Miao, Khai Ngo
U.S. PATENT: 9,998,111
Issued: June 12, 2018

VTIP 14-066
Hybrid Interleaving Structure with Adaptive Phase locked Loop for Variable Frequency Controlled Switching Converter
Pei-Hsin Liu, Qiang Li, Fred C. Lee
U.S. PATENT: 10,013,007
Issued: July 3, 2018

VTIP 17-072
Semiconductor Module Arrangement
Christina DiMarino, Mark Johnson, Dushan Boroyevich, Rolando Burgos
U.S. PATENT: 10,032,732
Issued: July 24, 2018

VTIP 15-071 (includes 15-070)
Multi-Step Simplified Optimal Trajectory Control (SOTC) Based on Only V_o and I_{load}
Chao Fei, Fred C. Lee, Weiyi Feng, Qiang Li
U.S. PATENT: 10,075,083
Issued: September 11, 2018

VTIP 14-144 (CIP to 13-169)
Low Profile Coupled Inductor Substrate with Transient Speed Improvement
Yipeng Su, Dongbin Hou, Fred C. Lee, Qiang Li
U.S. PATENT: 10,109,404
Issued: October 23, 2018

VTIP 14-101
Transient Performance Improvement for Constant On-Time Power Converters
Syed Bari, Fred C. Lee, Qiang Li, Pei-Hsin Liu
U.S. PATENT: 10,110,122
Issued: October 23, 2018

VTIP 16-030
Parallel Devices Having Balanced Switching Current and Power
Yincan Mao, Zichen Miao, Khai Ngo, Chi-Ming Wang
U.S. PATENT: 10,116,303
Issued: October 30, 2018

VTIP 16-094
High-Frequency Circulating Current Injection Control for High-Speed Switch-Based MMC
Jun Wang, Rolando Burgos, Dushan Boroyevich
U.S. PATENT: 10,153,712
Issued: December 11, 2018

VTIP 17-059
Method and Apparatus for Balancing Current and Power
Yincan Mao, Chi-Ming Wang, Khai Ngo
U.S. PATENT: 10,187,050
Issued: January 22, 2019

Patents Pending

All pending patent applications sponsored by IPPF, unless otherwise noted.

VTIP 18-048
11/8/2017
Soft-Switching ZVS Turn-on Triangular Current Mode (TCM) Control for Three-Phase 2-level Converters with Power Factor Control
Nidhi Haryani, Rolando Burgos
Utility Application: 16/053,378
Filed: August 2, 2018

VTIP 17-108 (Combined with 18-089)
5/2/2017
3-phase Interleaved LLC Converter with Integrated Magnetics
Chao Fei, Bin Li, Fred C. Lee, Qiang Li
Utility Application: 16/006,117
Filed: June 12, 2018

VTIP 17-016
8/26/2016
Soft-Switching Techniques for Three-Phase AC/DC Converters
Zhengrong Huang, Zhengyang Liu, Fred C. Lee, Qiang Li, Furong Xiao
Utility Application: 15/868,486
Filed: January 11, 2018

VTIP 17-015
8/26/2016
A Novel Bi-Directional Two-Stage AC/DC Converter with Variable DC-link Voltage and Integrated PCB Winding Transformer for Wide Output Voltage Range Applications
Bin Li, Zhengyang Liu, Fred C. Lee, Qiang Li
Utility Application: 15/693,930
Filed: September 1, 2017

VTIP 17-004
7/11/2016
Cooler with EMI-Limiting Inductor
Khai Ngo, Han Cui, Chi-Ming Wang
Utility Application: 15/622,802
Filed: June 14, 2017
[Patent application sponsored by TEMA]

VTIP 16-115
4/12/2016
Multiphase Coupled and Integrated Inductors with PCB Winding for PFC Converters
Yuchen Yang, Mingkai Mu, Fred C. Lee, Qiang Li
Utility Application: 15/484,641
Filed: April 11, 2017

VTIP 16-109
4/1/2016
Matrix Transformer and the Winding Structure
Chao Fei, Fred C. Lee, Qiang Li
Utility Application: 15/656,198
Filed: July 21, 2017

VTIP 16-062
1/28/2016
Interface Converter Common Mode Voltage Control
Fang Chen, Rolando Burgos, Dushan Boroyevich
Utility Application: 15/242,683
Filed: August 22, 2016

VTIP 16-057 (Combined with 17-062)
12/11/2015
Omni-Directional Wireless Power Transfer System
Junjie Feng, Qiang Li, Fred C. Lee, Minfan Fu
Utility Application: 15/417,353
Filed: January 27, 2017

VTIP 16-022
9/15/2015
Non-Linear Droop Control
Fang Chen, Rolando Burgos, Dushan Boroyevich
Utility Application: 15/296,564
Filed: October 18, 2016

VTIP 16-008
8/6/2015
Method and Apparatus for Driving a Power Device
Jongwon Shin, Khai D.T. Ngo
[Patent application sponsored by TEMA]

VTIP 16-007
7/27/2015
Modular Multilevel Converter Capacitor Voltage Ripple Reduction
Yadong Lyu, Yi-Hsun Hsieh, Fred C. Lee, Qiang Li
Utility Application: 15/239,165
Filed: August 17, 2016

Invention Disclosures

VTIP 15-067
1/26/2015
Inverse Charge Current Mode (IQCM) Control for Power Converter
Syed Bari, Fred C. Lee, Qiang Li
Utility Application: 15/089,744
Filed: April 4, 2016

VTIP 15-064
1/21/2015
Current Mode Control DC-DC Converter with Single-Step Load Transient Response
Virginia Li, Pei-Hsin Liu, Qiang Li, Fred C. Lee
Utility Application: 15/075,553
Filed: March 21, 2016

VTIP 15-053
12/1/2014
Optimal Battery Current Waveform for Bidirectional PHEV Battery Charger
Lingxiao Xue, Paolo Mattavelli, Dushan Boroyevich
Utility Application: 14/971,611
Filed: December 16, 2015

VTIP 15-049 (expanded from 14-091)
11/12/2014
Coupled Inductor for Interleaved Multi-Phase Three-Level DC-DC Converters
Mingkai Mu, Sizhao Lu, Yang Jiao, Fred C. Lee
Utility Application: 14/957,743
Filed: December 3, 2015

VTIP 14-075
1/6/2014
Compact Inductor Employing Redistributed Magnetic Flux
Khai Ngo, Han Cui
Utility Application: 14/675,653
Filed: March 31, 2015

VTIP 18-089
2/23/2018
Three-phase Interleaved LLC and CLLC Resonant Converter with Integrated Magnetics
Bin Li, Chao Fei, Fred C. Lee, Qiang Li, Hongfei Wu

VTIP 18-113
4/20/2018
Switched-Capacitor Converters with Multi Resonant Frequencies
Owen Jong, Qiang Li, Fred C. Lee

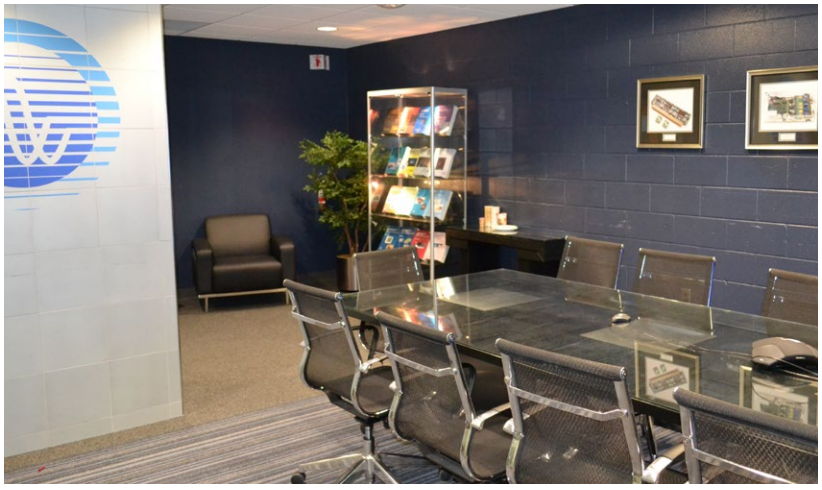
VTIP 18-123
5/15/2018
Soft Switching ZVS Turn-on Triangular Current Mode (TCM) Control with Phase Synchronization and Reduced Common Mode Voltage (CMV) for Three-Phase Three-Level Converters
Nidhi Haryani, Sungjae Ohn, Rolando Burgos, Dushan Boroyevich

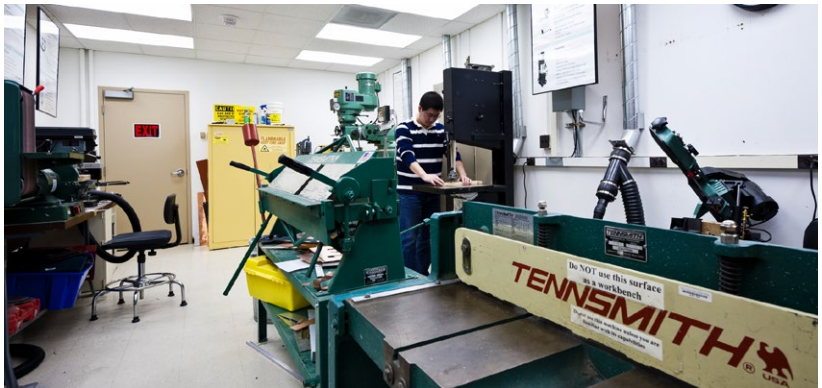
VTIP 19-022
9/18/2018
Three-Phase Interleaved Bi-Directional CLLC Resonant Converter
Hao Xue, Bin Li, Qiang Li, Fred C. Lee

Virginia Tech Facilities

Introduction

The Center headquarters are located at Virginia Tech, occupying office and lab facilities encompassing more than 20,000 square feet of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab, and a computer lab. In addition to the headquarters labs and offices, a large conference room with voice and video conferencing capabilities supporting remote site course instruction as well as interaction among CPES collaborators is maintained. Interactive collaboration is routinely facilitated through conference calls, GoToMeeting and Zoom online conferencing, student and faculty exchanges, and face-to-face research project review meetings.

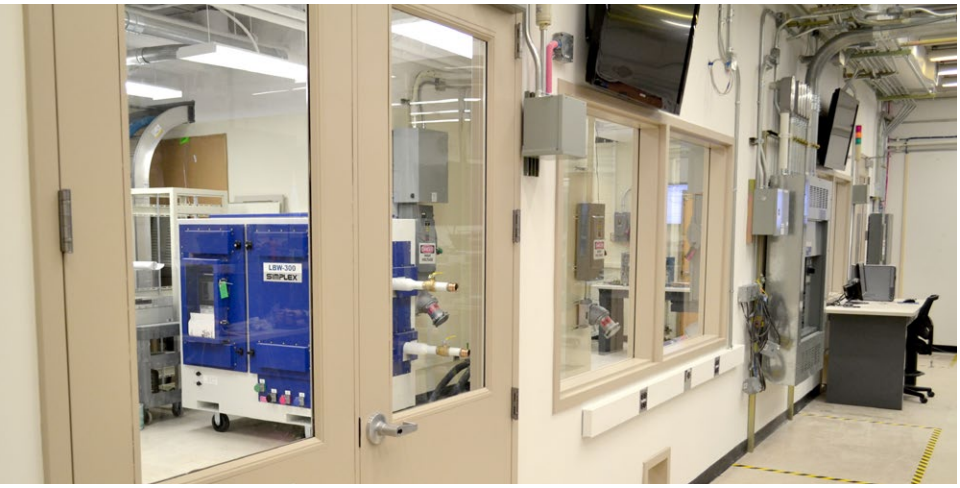




National Capital Region Laboratory

The CPES lab in Northern Virginia represents a state-of-the-art power electronics laboratory well-suited to continue building upon the CPES worldwide recognized expertise in developing groundbreaking power electronics technology ranging from watts to megawatts of power. This lab opened for the spring semester of 2019, and is located on the fourth floor of the Virginia Tech Research Center in Arlington, VA, occupying more than 1,800 square feet of space. Equipped with the latest testing and measurement equipment capable of achieving several hundreds of kilowatts of power, it is run by two faculty and two research faculty, providing an environment for unparalleled hands-on experience for a dozen graduate students and visiting scholars.

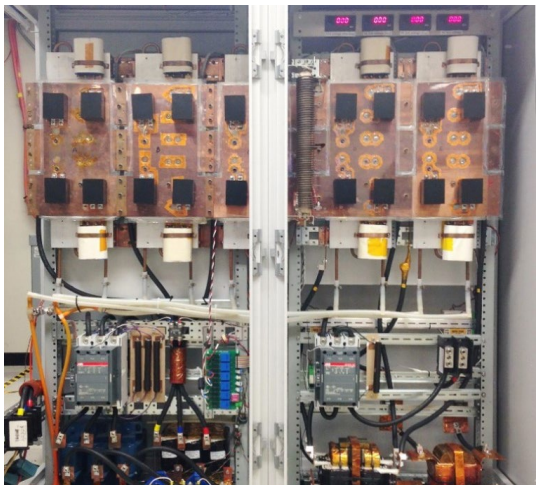
This lab will continue to deliver high quality research in an unmatched collaborative atmosphere with enormous teamwork energy, creating a family-like environment quite natural for CPES. Furthermore, as a part of the VT Electronic Energy Systems Initiative, this new lab expands Virginia Tech's presence in Northern Virginia, and in a joint effort with its main lab located in Blacksburg, stays dedicated to the improvement of electronic power processing that impacts systems of all sizes, from battery-operated to large distribution systems.



Electrical Research Laboratory

The electrical research laboratory is equipped with state-of-the-art tools and equipment for development of power electronic circuits and systems of all sizes from sub-volts, sub-watts to 6 kV, 1 MW. It also includes PWB manufacturing equipment, an EMI chamber, a clean room and a mechanical shop. A state-of-the-art curve tracer is capable of characterizing up to 10 kV and 1500 A. New this year is the addition of a 10kV probing station that will be integrated with the curve tracer. This will allow characterization of materials at the die level. Each student bench is equipped with Dell computers with up to 32 GB of RAM for running complex simulations.

Standard instrumentation includes GHz oscilloscopes, multi-channel function generators, electronic loads, low- and high-voltage passive and differential probes, network, spectrum, impedance, logic, and power analyzers, thermal sensors, and ac-dc bench supplies of all sizes. Specialized test room equipment includes thermal imaging, a Hi-Pot tester, a 3D magnetic field scanner, an EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, magnetic core loss testing, programmable and variable loads, and liquid-cooled heat exchanger.



Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculty, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab was established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 cleanroom space, and the addition of a dark room for photolithography processing. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro/electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing.

The IP lab also has the ability to mount bare dies and SMT components using a high precision pick-n-place machine, a solder reflow belt furnace, and a convection reflow oven. The advanced vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapuslants, an automated precision dispensing system and a spin coater have been added in the lab.

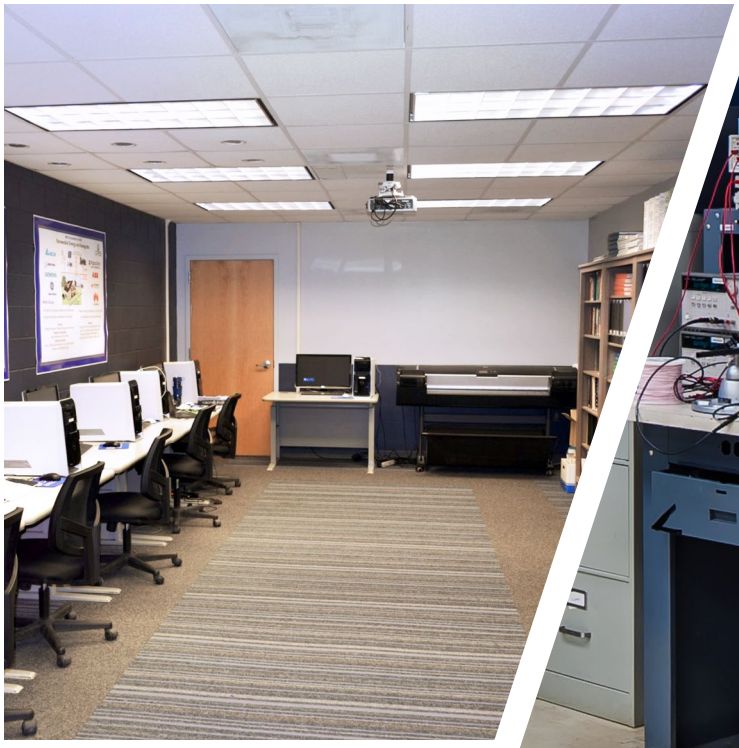
In addition, the IP lab has the full capability for low temperature co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The components and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Thermal performance evaluation can be made by the setup of thermo-couples, optic-fiber sensors, IR imaging, and the thermal diffusivity test system. Reliability analysis is performed using multi-purpose bond tester on as-made modules and ones after certain numbers of temperature/humidity cycling. An array of cross-sectioning and grinding/polishing equipment has been used to better understand the microstructure of electronic packaging materials.

High Power Lab

High power, high voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost-sharing of more than $250,000 for renovations, the electrical research lab area at Virginia Tech has been renovated and upfitted to accommodate medium voltage, megawatts power capability. The facility has two medium voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. A 1 MW Innovation Series medium voltage IGBT drive donated by GE is installed as a programmable load. The complete set-up is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4160 V level. The unique installation distinguishes Virginia Tech as one of a few universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

Library and Computer Lab

The computer lab supports all major software used in power electronics design, including SPICE, Saber, Simplis, PowerSim, Code Composer, Math products—Matlab and Mathcad, Ansys Products—Workbench and Mechanical, Ansys Electromagnetics—Maxwell, Electronics Desktop (Q3D, HFSS), Simplorer, SIWave, Mentor Graphics Flowtherm, PLECS, and Altium Designer.



Spotlight on Alumni

ChihYi Lin

Affiliation:
Delta Electronics Inc.

Position title:
Senior Design Manager

Last degree
from Virginia Tech:
Ph.D.

Year Graduated:
1997

CAREER HIGHLIGHTS

1997 Graduated from VPEC and researched applications of piezoelectric transformer; joined Delta Electronic Inc. in August

1998 Principal Engineer, completed a first server project with current sharing optional

1999 R&D Manager, worked on networking power and high-density DC converters

2005 Senior Design Manager; product development of CCFL/LED TV power supplies

2010 Built an R&D team in WuJian/Wuhu, China

2013 Transferred to system validation on high-power lithium battery charger

2015 Leading the 2nd generation DC converters and high-end server power, and planning for platform design of power supply products

2018 Leading the advanced research on power electronics and traction inverter of battery electric vehicles

PERSONAL REFLECTIONS

From 1991 to 1997, regular research hours and a wonderful living environment helped me recover my health and develop excellent family relationships.

Various successful research tasks during my VPEC days helped me manage product development very well, especially developing WBG device applications in EV power trains recently.

Hengchun Mao

Affiliation:
Quanten Technologies Inc.

Position title:
President & Founder

Last degree
from Virginia Tech:
Ph. D.

Year Graduated:
1996

CAREER HIGHLIGHTS

1996 Joined Bell Labs, Lucent Technologies. Conducted high-frequency and high efficiency power conversion research

2000 Cofounded NetPower Technologies. As its CTO and General Manager, grew NetPower into a technology leader in dc-dc power converter industry

2010 Joined Huawei as its Principal Architect in embedded power business, responsible for technology and platform development. Invented and developed BEMRD power architecture and key blocks adopted in high-performance and high-density telecom/network equipment

2013 Joined BCD Semi/Diodes Inc as General Manager of ACDC BU. Managed the low power ac-dc controllers and smart phone charger solutions

2014 Cofounded NuVolta Technologies Inc. Invented controlled resonance power architecture for flexible wireless power transfer, and developed industry's first integrated transmitter power IC for 6.78 MHz MR solutions

2017 Founded Quanten Technologies Inc., a startup company working on integrated drive systems and power solutions for HEVs, robots and other mobility applications

PERSONAL REFLECTIONS

Dr. Lee and VPEC taught me to maintain intellectual curiosity and positive attitude and to focus on solving real problems when facing tough challenges. This helped trigger a long and rewarding self-growing process.

Shuo Wang

Affiliation:
University of Florida

Position title:
Associate Professor

Last degree
from Virginia Tech:
Ph.D.

Year Graduated:
2005

CAREER HIGHLIGHTS

2001 Ph.D. student of Fred C. Lee

2005 Earned Ph.D. from CPES, Virginia Tech

2005 Research Assistant Professor, CPES, Virginia Tech

2009 Senior Design Engineer, GE Aviation Systems

2010 Assistant Professor, University of Texas at San Antonio

2012 Established Power Electronics and Electrical Power Research Lab (PEEPRL)

2012 NSF CAREER Award

2014 Associate Professor, University of Texas at San Antonio

2015 Associate Professor, University of Florida

2017 Radiated EMI research for Power Electronics with 3m anechoic chamber

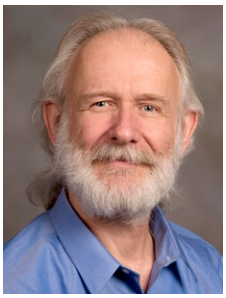
2019 IEEE Fellow for contributions to reduction of EMI in electronic systems

PERSONAL REFLECTIONS

CPES's research and student advising methodology greatly shaped my career.

People

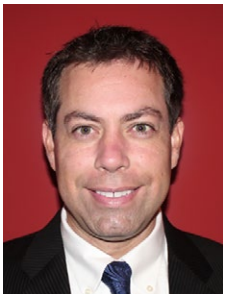
Tenure-Track Faculty



Dushan Boroyevich

CPES Director
University Distinguished Professor
Associate Vice President for Research and Innovation

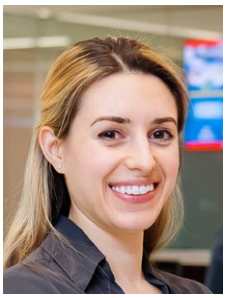
Dushan Boroyevich was born in 1952 in Zagreb, Croatia, in what was then Yugoslavia. In the same country, he earned a Dipl. Ing. from the University of Belgrade in 1976, and an M.S. from the University of Novi Sad in 1982, both in electrical engineering. He obtained a Ph.D. in power electronics in 1986 from Virginia Tech. His research interests include multiphase power conversion, electronic power distribution systems, modeling and control, and multidisciplinary design optimization. As CPES Director, Boroyevich leads a program which encompasses research, technology development, educational outreach, industry collaboration, and technology transfer.



Rolando Burgos

Associate Professor

Rolando Burgos (S'96–M'03) was born in Concepcion, Chile, where he attended the University of Concepcion, earning his B.S. in electronics engineering in 1995 and a professional engineering certificate in electronics engineering in 1997, graduating with honors. At the same institution he later earned his M.S. and Ph.D. degrees in electrical engineering in 1999 and 2002, respectively.



Christina DiMarino

Assistant Professor

Christina DiMarino is an assistant professor in the Bradley Department of Electrical and Computer Engineering at Virginia Tech. She has been the assistant director of the Center for Power Electronics Systems (CPES) since 2017. She received her M.S. and Ph.D. in electrical engineering from Virginia Tech in 2014 and 2018, respectively. She was a Webber Fellow from 2012 to 2015, and a Rolls-Royce Graduate Fellow from 2016 to 2017.

Her research interests include power electronics, electronics packaging, high density integration, wide-bandgap power semiconductors, high voltage, and high temperature.

Dong Dong

Assistant Professor

Dong Dong received a Bachelor of Science in 2007 from Tsinghua University in China and a Ph.D. in 2012 from Virginia Tech. Before joining CPES in 2018, he worked with GE's global research center for over five years on various power electronics and power system-related technologies. His research interests include high-frequency high-power conversion, application of wide bandgap-based power electronics, power conversion systems for renewable energy systems, electric grids, and transportation applications.

Mona Ghassemi

Assistant Professor

Mona Ghassemi received her M.S. and Ph.D. from the University of Tehran in 2007 and 2012, respectively. She was a postdoctoral fellow at NSERC/Hydro-Quebec/ UQAC from 2013 to 2015, and at the Electrical Insulation Research Center (EIRC) of the Institute of Materials Science (IMS) at the University of Connecticut from 2015 to 2017. Her research interests include dielectrics and electrical insulation materials and systems containing those in power electronics modules and systems, high-voltage technology, multiphysics modeling, plasma science, electromagnetic transients in power systems, and power system modeling.

Qiang Li

Associate Professor

Qiang Li received his B.S. in 2003 and M.S. in 2006 from Zhejiang University. Then in 2011 he received his Ph.D. from Virginia Tech. He started at Virginia Tech as a Research Assistant Professor in 2011 and was promoted to Assistant Professor in 2012. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, high-frequency power conversion, distributed power systems, and renewable energy.

Guo-Quan Lu

Professor (Affiliate Faculty)

G.Q. Lu received a double-major B.S. in physics and materials science and engineering from Carnegie-Mellon University in 1984. He then went on to Harvard University, where he earned an M.S. and Ph.D. in applied physics by 1990. Since 2003, Lu has been a professor in both the MSE and Electrical and Computer Engineering departments.

Khai Ngo

Professor

Khai Ngo received his B.S. from California State Polytechnic University, Pomona, in 1979, and his M.S. and Ph.D. from the California Institute of Technology, Pasadena, in 1980 and 1984, respectively, all in electrical and electronics engineering. At CPES, he pursues technologies for integration and packaging of power passive and active components to realize building blocks for power electronic systems. He also coordinates CPES's outreach activities and the Consortium for High-Density Integration

Yuhao Zhang

Assistant Professor

Yuhao Zhang studied physics at Peking University in China, where he received a B.S. in 2011. He went on to study electrical engineering at Massachusetts Institute of Technology in the United States, earning his M.S. in 2013 and his Ph.D. in 2017. His research interest is at the intersection of power electronics, micro/nano-electronic devices and advanced semiconductor materials, and the energy applications for data centers, electric vehicles, photovoltaics, and mobile applications, as well as the energy-related applications in extremely harsh environments.

Research Faculty

Igor Cvetkovic
Technical Director

David Gilham
Lab Operations Director

Fred C. Lee
Director Emeritus

Jun Wang
Research Assistant Professor

Bo Wen
Visiting Research Faculty

Staff

Audriana Cunningham
Executive Assistant

Dennis Grove
Industry Program Director

Na Ren
Business Director

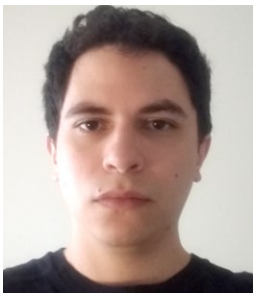
Trish Rose
Procurement Officer

Yan Sun
Accounting and Fiscal Associate

Visiting Scholars

Shaoliang An
PROFESSOR
Xi'an University of Technology, China

Guoen Cao
PROFESSOR
Institute of Electrical Engineering, Chinese Academy of Sciences (IEE CAS), China



Louelson Costa
PH.D. STUDENT
Federal University of Campina Grande (UFCG), Brazil

Nayara Brandao de Freitas
PH.D. STUDENT
Federal University of Campina Grande (UFCG), Brazil

Boran Fan
PH.D. STUDENT
Tsinghua University, China

Emilie Feick
VISITING ENGINEER
Newport News Shipbuilding, USA

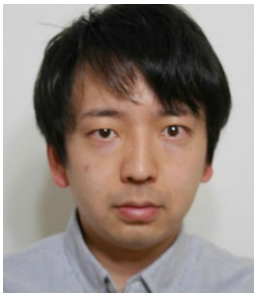
Darlan Fernandes
PROFESSOR
Federal University of Paraiba, Brazil

Minfan Fu
PH.D. STUDENT
University of Michigan and Shanghai Jiao Tong University Joint Institute, China

Chaofei Gao
PH.D. STUDENT
North China Electric Power University, China

Takashi Hirota
VISITING ENGINEER
Komatsu Ltd., Japan

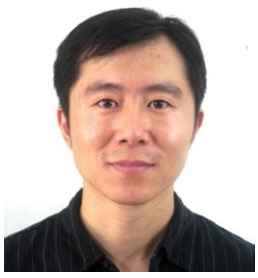
Mark Hoffman
VISITING ENGINEER
Newport News Shipbuilding, USA



Takayuki Ikari
VISITING ENGINEER
Nissan Motor Co. Ltd., Japan

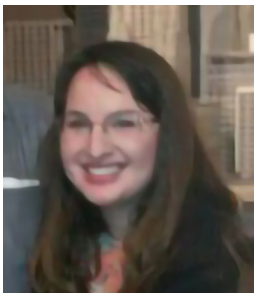
Toshihiro Kai
VISITING ENGINEER
Nissan Motor Co. Ltd., Japan

Ryo Kajitani
VISITING ENGINEER
Panasonic Corporation, Japan



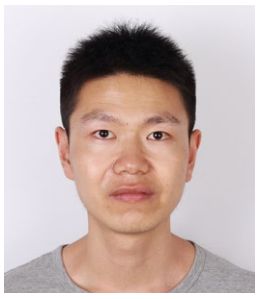
Lei Li
PROFESSOR
Nanjing University of Science and Technology, China

Vladimir Mitrovic
GRADUATE STUDENT
School of Electrical & Computer Engineering of Applied Studies, Serbia



Cassandra Pagels
VISITING ENGINEER
Newport News Shipbuilding, USA

Phu Hieu Pham
POSTDOC
National Taiwan University of Science and Technology, Vietnam



Wei Qin
PH.D. STUDENT
Zhejiang University, China

Javier Samanes
PH.D. STUDENT
Public University of Navarre, Spain

Xingguo Tan
PROFESSOR
Henan Polytechnic University, China

Takahide Tanaka
VISITING ENGINEER
Fuji Electric Co. Ltd., Japan

David Vrtachnik
VISITING ENGINEER
Newport News Shipbuilding, USA

Ke Wang
VISITING ENGINEER
East China Research Institute of Microelectronics (ECRIM), China

Leping Wang
STUDENT INTERN
Tsinghua University, China

Hongfei Wu
PROFESSOR
Nanjing University of Aeronautics and Astronautics, China

Ming Xiao
POSTDOC
Xidian University, China

Fan Yang
PH.D. STUDENT
Nanjing University of Aeronautics and Astronautics, China

Zhichang Yuan
PROFESSOR
Tsinghua University, China

Chongxing Zhang
PH.D. STUDENT
Xi'an Jiaotong University, China

Dong Zheng
VISITING ENGINEER
East China Research Institute of Microelectronics (ECRIM), China

Songlin Zheng
STUDENT INTERN
Tsinghua University, China

Sizhan Zhou
POSTDOC
Xi'an Jiaotong University, China

Graduate Students

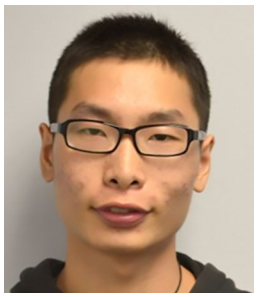

Mohamed Ahmed


Yinsong Cai


Chien-An Chen

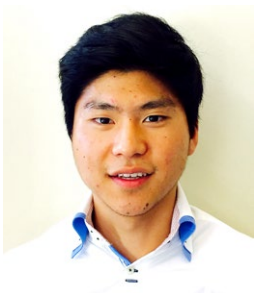

Chao Ding

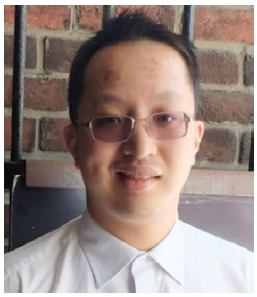

Michael Emanuel

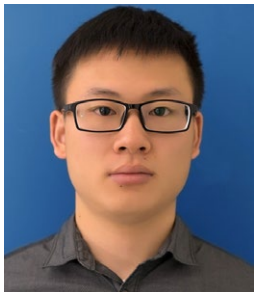

Junjie Feng


Alex Freeman

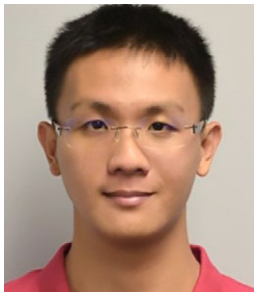

Rimon Gadelrab


Lee Gill


Patrick Gu


Yu Guo


Nidhi Haryani


Yi-Hsun Hsieh


Jiewen Hu


Zhengrong Huang


Feng Jin


Daniel Kellett


Joseph Kozak


Bo Li


Qian Li

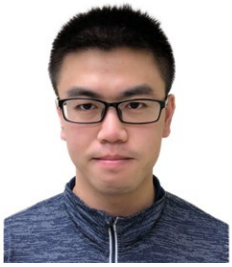

Virginia Li

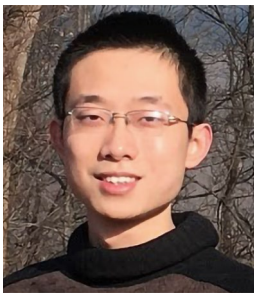

Zheqing Li


Xiang Lin


Lanbing (Leona) Liu

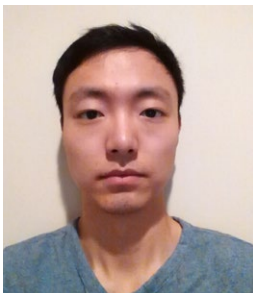

Xin Lou


Shengchang Lu


Yunwei Ma


Slavko Mocevic


Ahmed Nabih


David Nam


Tam Khanh Tu Nguyen


John Noon


Ripunjoy Phukan


Pranav Raj Prakash


Emma Raszmann


Lakshmi Ravi


Seyyed Moein Razavi Borghei

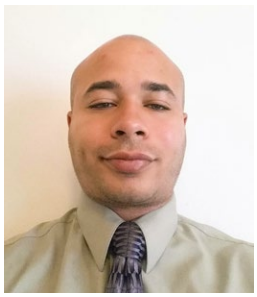

Yu Rong


Rebecca Rye

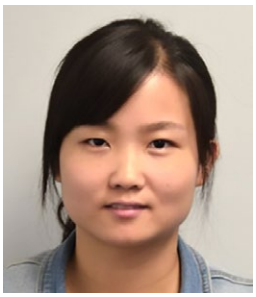

Chris Salvo


Gibong Son


He Song


Joshua Stewart


Keyao Sun


Ye Tang


Maryam Tousi


Cong Tu


Boyan Wang


Le Wang


Shuo Wang


Grace Watt


Yue Xu

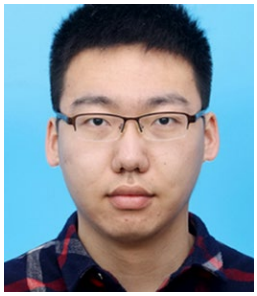

Hao Xue


Ning Yan


Jianghui Yu


Lujie Zhang


Ruizhe Zhang


Chunyang Zhao


Tianyu Zhao


Feiyang Zhu

Undergraduate Students

Benjamin Alden

Yijie Bai

Matthew Erwin

Michaela Goldammer

William Alan Lu

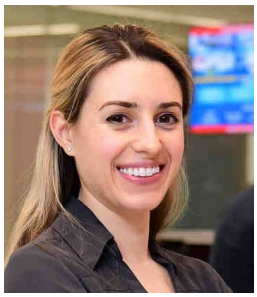
Paul Mourges

Elif Patton

Mina Shawky

Neil Edwin Slinde

Graduates



Christina DiMarino
Virginia Tech

Chao Fei
Google

Ting Ge
Monolithic Power Systems

Yingying Gui
Delta Electronics

Owen Jong
Analog Devices

Bin Li
Navitas Semiconductor

Chi Li
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Zichen Miao
Monolithic Power Systems

Sungjae Ohn
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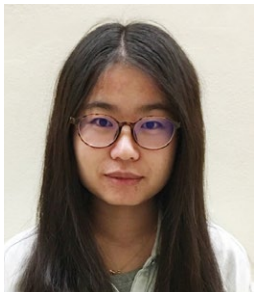
Paul Rankin
Raytheon Company



Bingyao Sun
Texas Instruments

Victor Turriate
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Yuchen Yang
Analog Devices

Advisory Boards

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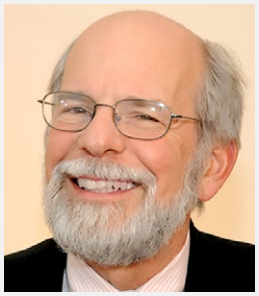
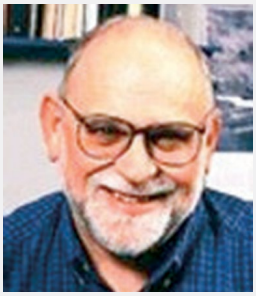


John Kassakian
Massachusetts Institute of Technology



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Bob Steigerwald
GE Global Research (retired)

Al Tucker
Office of Naval Research (retired)

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Jian Li	VERTIV
Jianping Zhou	ZTE Corporation

Honors & Achievements

National and International Honors

Christina DiMarino—Awarded Best Presentation/ Paper: ECPE Young Engineer Award, International Conference on Integrated Power Electronics

Dushan Boroyevich—Organizing Committee Member and HVDC and FACTS Session Chair for IEEE eGrid 2018

Dushan Boroyevich—Inducted into Virginia Tech College of Engineering Academy of Engineering Excellence, Virginia Tech

Guo-Quan Lu—Elected IEEE Fellow, Class of 2018 (officially recognized at ECCE 2018 Conference)

Guo-Quan Lu—Technical Program Chair for 3D Power Electronics Integration and Manufacturing Symposium (3D-PEIM) held in June, 2018, University of Maryland

Igor Cvetkovic—Led the electrical and power management team of FutureHAUS to 1st place finish at the Solar Decathlon Middle East, sponsored by the Dubai Electricity and Water Authority and the U.S. Department of Energy

Qiang Li—General Co-Chair for IEEE International Future Energy Challenge (IFEC) 2018

Rolando Burgos—Technical Program Co-Chair, IEEE ECCE 2018, September 2018

Rolando Burgos—Re-elected Chair of IEEE PELS Technical Committee on Power and Control Core Technologies for 2019-2020

Rolando Burgos—Technical Committee Member for IEEE COMPEL 2018

Fred C. Lee—2018 National Academy of Inventors (NAI) Fellow

Fred C. Lee—2018 Honorary Chair Professor, Tsinghua University, China

Fred C. Lee—2018 Honorary Professor, Huazhong University of Science and Technology, China

Fred C. Lee—Honorary General Chair, IEEE Power Electronics Applications Conference (PEAC), November 4-7, 2018, Shenzhen, China

Dong Dong—Vice Chair of IEEE Industry Application Society's Schenectady Chapter

Dong Dong—Organizing and Technical Committee Member of IEEE Energy Conversion Congress and Expo Conference

Keynote Addresses

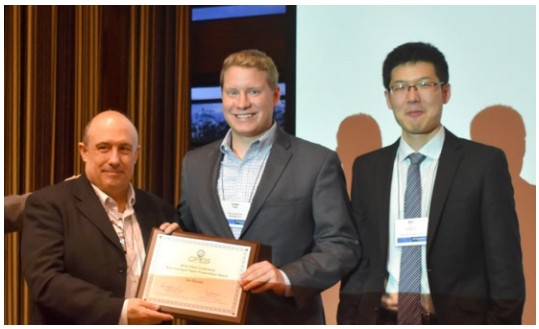
Guo-Quan Lu—"Advanced Die-Attach by Metal-Powder Sintering: The Science and Practice," 10th International Conference on Integrated Power Electronics Systems (CIPS 2018), March 20-22, 2018, Stuttgart, Germany

Dushan Boroyevich—"Future Electronic Energy Systems," IECON 2018, October 21-23, 2018, Washington, D.C.

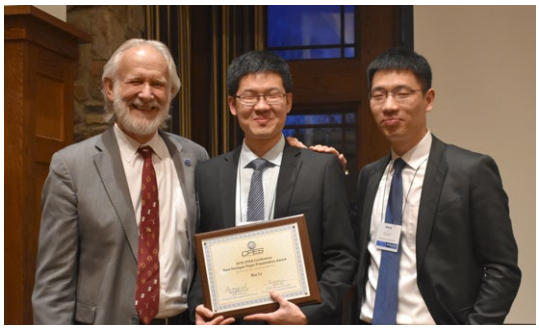
Fred C. Lee—"Is GaN a Game Changer," IEEE WiPDA, May 16-18, 2018, Xi'an, China

Fred C. Lee—"Leading the Technology Trends," Wuhan Power Supply Association Innovation Workshop, October 27, 2018, Wuhan, China

Fred C. Lee—"Design for Manufacturability – a New Paradigm," IEEE Power Electronics Applications Conference (PEAC), November 4-7, 2018, Shenzhen, China



Joseph Kozak (center), 2018 CPES Annual Conference, Best Dialogue Presentation, sponsored by General Electric



Bin Li (center), 2018 CPES Annual Conference, Best Dialogue Presentation, sponsored by Lockheed Martin Corporation

Christina DiMarino (left), ECPE Young Engineer Award, International Conference on Integrated Power Electronics

Invited Talks

Dushan Boroyevich, Rolando Burgos, Jinjun Liu, & Paolo Mattavelli—Invited Tutorial: **"Small-Signal Stability and Subsystem Interactions in Distributed Power Systems with Multiple Converters (II): 3-Phase AC Systems,"** IEEE APEC 2018, San Antonio, TX, March 2018

Fred C. Lee—**"Evolution of Power Electronics Technologies,"** Tsinghua University, Beijing, China, April 23, 2018

Rolando Burgos—**"100 kW PV Inverter with Efficiency > 99 % Operating in Interleaved Triangular Conduction Mode,"** PowerAmerica Webinar, April 2018

Khai Ngo—**"Integration of Energy Storage into Power Module by Magnetic Molding,"** 3D-PEIM, June 27, 2018

Rolando Burgos—**"100 kW PV Inverter with Efficiency > 99 % Operating in Interleaved Triangular Conduction Mode,"** PowerAmerica DOE Peer Review, Raleigh, NC, June 2018

Dushan Boroyevich, Rolando Burgos, Igor Cvetkovic, & Bo Wen—Invited Tutorial: **"Modeling and Control of Three-Phase AC High-Power High-Frequency Converters,"** IEEE COMPEL 2018, Padova, Italy, June 2018

Christina DiMarino—**Centre for Power Electronics (CPE) Annual Conference,** July 2018

Rolando Burgos—**"Wide-Bandgap Generation (WBGen) Fellowship Program at Virginia Tech,"** DOE Advanced Manufacturing Office Peer Review, Washington, D.C., July 2018

Qiang Li—**"Impacts of GaN Devices on Power Converter Design,"** PowerAmerica 2018 WBG Summer Workshop, Raleigh, NC, August 22-24, 2018

Dong Dong—**"Power Electronics with WBG Devices in Industrial Applications,"** GENESiC, September, 2018

Fred C. Lee—**"Next Generation of Power Supplies,"** IEEE Wuhan Chapter Inauguration, Wuhan, China, October 26, 2018

Fred C. Lee—**"New Generation of Power Supplies,"** Zhejiang University, Hangzhou, China, October 31, 2018

X. Wang & Rolando Burgos—Tutorial Presentation: **"Small-Signal Modeling and Stability Analysis of Grid-Connected Power Converters,"** IEEE eGrid 2018, Charleston, SC, November, 2018

Rolando Burgos—**"Power Converters Based on Wide-Bandgap Power Semiconductors (SiC, GaN),"** Universidad de Concepcion, Chile, December, 2018

2018 Prize Paper Awards

IEEE TRANSACTIONS ON POWER ELECTRONICS

Second Place: **"Design of Inductors with Significant AC Flux,"** **Zhemin Zhang, Khai Ngo & Jeff Nilles,** IEEE Transactions on Power Electronics, Vol. 32, No. 1, January 2017, pp. 529 - 539

IEEE ENERGY CONVERSION CONGRESS & EXPOSITION (ECCE)

First Place: **"Analytical Method to Calculate Winding Resistance of Litz Wire for Planar Coil with Ferrite Plate in Inductive Power Transfer,"** **Ming Lu & Khai Ngo,** IEEE Industry Applications Society, Transportation Systems Committee, Industrial Power Conversion Systems Department, pp. 111-117

WILLIAM M. PORTNOY AWARD:

Best Paper Award: **"Design of a Novel, High-Density, High-Speed 10 kV SiC MOSFET Module,"** **Christina DiMarino, Mark Johnson, Bassem Mouawad, Jianfeng Li, Dushan Boroyevich, Rolando Burgos, Guo-Quan Lu & Meiyu Wang,** 2017 IEEE Energy Conversion Congress & Expo (ECCE), Duke Energy Convention Center, Cincinnati, OH, October 1–5, 2017, pp. 4003–4010, received September 2018

IEEE INTERNATIONAL CONFERENCE ON ELECTRONIC PACKAGING

Outstanding Technical Paper Award: **"Effect of Substrate Surface Finish on Bonding Strength of Pressure-less Sintered Silver Die-Attach,"** **Yunhui Mei, Rolando Burgos, Dushan Boroyevich & Guo-Quan Lu,** IEEE ICEP 2018, April 2018

2018 CPES Annual Conference Best Student Presentation Awards

Best Technical Presentation Awards
Yi-Hsun Hsieh (Sponsored by Texas Instruments)
Keyao Sun (Sponsored by Delta Electronics)

Best Dialogue Presentation Awards
Bin Li (Sponsored by Lockheed Martin Corporation)
Bingyao Sun (Sponsored by Huawei Technologies)
Joseph Kozak (Sponsored by General Electric)

Publications

Transactions Papers

Power Quality Characteristics of a Multilevel Current Source With Optimal Predictive Scheme From More-Electric-Aircraft Perspective
Hamed Nademi, Rolando Burgos, Zareh Soghomonian
IEEE Transactions on Vehicular Technology, Volume 67, Issue 1, January 2018, pp. 160–170

Design, Fabrication, and Characterization of a Low-Temperature Curable Magnetic Composite for Power Electronics Integration
Yi Yan, Weizhen Sun, Shan Gao, Ting Ge, Khai Ngo, Guo-Quan Lu
IEEE Transactions on Magnetics, Volume 54, Issue 1, January 2018, Article Sequence Number: 2800106

A New Fast Adaptive On-Time Control for Transient Response Improvement in Constant On-Time Control
Syed Bari, Qiang Li, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 33, No. 3, March 2018, pp. 2680–2689

Design and Comparison of Cascaded H-Bridge, Modular Multilevel Converter, and 5-L Active Neutral Point Clamped Topologies for Motor Drive Applications
Ali Marzoughi, Rolando Burgos, Dushan Boroyevich, Yaosuo Xue
IEEE Transactions on Industry Applications, Vol. 54, No. 2, March/April 2018, pp. 1404–1413

Beat Frequency Oscillation Analysis for Power Electronic Converters in DC Nanogrid Based on Crossed Frequency Output Impedance Matrix Model
Xiaolong Yue, Dushan Boroyevich, Fred C. Lee, Fang Chen, Rolando Burgos, Fang Zhuo
IEEE Transactions on Power Electronics, Vol. 33, No. 4, April 2018, pp. 3052–3064

A Fast Method to Optimize Efficiency and Stray Magnetic Field for Inductive-Power-Transfer Coils Using Lumped-Loops Model
Ming Lu, Khai Ngo
IEEE Transactions on Power Electronics, Vol. 33, No. 4, April 2018, pp. 3065–3075

Systematic Design of Coils in Series–Series Inductive Power Transfer for Power Transferability and Efficiency
Ming Lu, Khai Ngo
IEEE Transactions on Power Electronics, Vol. 33, No. 4, April 2018, pp. 3333–3345

Robust Stability Analysis of a DC/DC Buck Converter Under Multiple Parametric Uncertainties
Sharmila Sumsurooah, Milijana Odavic, Serhiy Bozhko, Dushan Boroyevich
IEEE Transactions on Power Electronics, Vol. 33, No. 6, June 2018, pp. 5426–5441

Digital Implementation of Adaptive Synchronous Rectifier (SR) Driving Scheme for High-Frequency LLC Converters with Microcontroller
Chao Fei, Qiang Li, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 33, No. 6, June 2018, pp. 5351–5361

IEEE ITRW: International Technology Roadmap for Wide-Bandgap Power Semiconductors: An Overview
Peter R. Wilson, Braham Ferreira, Jing Zhang, Christina DiMarino
IEEE Power Electronics Magazine, Volume 5, Issue 2, June 2018, pp. 22–25

Optimum Design Guidelines for the Modular Multilevel Converter in Active Front-End Applications: Considerations for Passive Component Reduction
Alinaghi Marzoughi; Rolando Burgos; Dushan Boroyevich
IEEE Power Electronics Magazine, Volume 5, Issue 2, June 2018, pp. 56–65

Effect of Surface Roughening of Temperature-Cycled Ceramic-Metal-Bonded Substrates on Thermomechanical Reliability of Sintered-Silver Joints
Shan Gao, Seiya Yuki, Hideyo Osanai, Weizhen Sun, Khai Ngo, Guo-Quan Lu
IEEE Transactions on Device and Materials Reliability, Volume 18, Issue 2, June 2018, pp. 291–297

How to Determine Surface Roughness of Copper Substrate for Robust Pressureless Sintered Silver in Air
Meiyu Wang, Yunhui Mei, Xin Li, Rolando Burgos, Dushan Boroyevich, Guo-Quan Lu
Materials Letters, Volume 228, June 2018, pp. 327–330

Modeling and Design Optimization of Capacitor Current Ramp Compensated Constant On-Time V2 Control
Yingyi Yan, Fred C. Lee, Shuilin Tian, Pei-Hsin Liu
IEEE Transactions on Power Electronics, Vol. 33, No. 8, August 2018, pp. 7288–7296

Partial Discharge Measurements, Failure Analysis and Control in High Power Insulated Gate Bipolar Transistor Modules
Mona Ghaseemi
IET High Voltage, Vol. 3, No. 3, September 2018, pp. 170–178

High-Frequency Transformer Design for Modular Power Conversion From Medium-Voltage AC to 400 VDC
Shishuo Zhao, Qiang Li, Fred C. Lee, Bin Li
IEEE Transactions on Power Electronics, Vol. 33, No. 9, September 2018, pp. 7545–7557

A High Efficiency High Density Wide-Band-Gap Device Based Bi-Directional On-Board Charger
Bin Li, Qiang Li, Fred C. Lee, Zhengyang Liu, Yuchen Yang
IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 6, No. 3, September 2018, pp. 1627–1636

Low-Frequency Stability Analysis of Single-Phase System with *dq*-Frame Impedance Approach – Part I: Impedance Modeling and Verification
Yicheng Liao, Zhigang Liu, Han Zhang, Bo Wen
IEEE Transactions on Industry Applications, Vol. 54 , No. 5, September/October 2018, pp. 4999–5011

Low-Frequency Stability Analysis of Single-Phase System with *dq*-Frame Impedance Approach – Part II: Stability and Frequency Analysis
Yicheng Liao, Zhigang Liu, Han Zhang, Bo Wen
IEEE Transactions on Industry Applications, Vol. 54 , No. 5, September/October 2018, pp. 5012-5024

Steady-State Analysis of Resonant Cross-Commutated Buck Converter under Continuous Voltage Mode
Ting Ge, Brian Carpenter, Khai Ngo
IEEE Transactions on Industrial Electronics, Vol. 65, No. 10, October 2018, pp. 7782–7792

Digital Constant On-time V2 Control With Hybrid Capacitor Current Ramp Compensation
Pei-Hsin Liu, Yingyi Yan, Paolo Mattavelli, Fred C. Lee
IEEE Transactions on Power Electronics, Vol. 33, No. 10, October 2018, pp. 8818–8826

Electrical Insulation Weaknesses in Wide Bandgap Devices
Mona Ghassemi
Simulation and Modelling of Electrical Insulation Weaknesses in Electrical Equipment, R. A. Sánchez (Ed), IntechOpen, UK, November 2018, Chapter 6, pp. 129–149

Digital Implementation of Light-Load Efficiency Improvement for High-Frequency LLC Converters with Simplified Optimal Trajectory Control (SOTC)
Chao Fei, Qiang Li, Fred C. Lee
IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 6, No. 4, December 2018, Special Section pp. 1850–1859

Ferrite Paste Cured With Ultraviolet Light for Additive Manufacturing of Magnetic Components for Power Electronics
Lanbing Liu, Ting Ge, Khai Ngo, Yunhui Mei, Guo-Quan Lu
IEEE Magnetics Letters, Volume 9 (2018), Article Sequence Number: 5102705

Transient Core-Loss Simulation for Ferrites With Nonuniform Field in SPICE
Han Cui, Khai Ngo
IEEE Transactions on Power Electronics, Vol. 34, No. 1, January 2019, pp. 659–667

Characterization and Performance Evaluation of the State-of-the-Art 3.3 kV 30 A Full-SiC MOSFETs
Alinaghi Marzoughi, Rolando Burgos, Dushan Boroyevich
IEEE Transactions on Industry Applications, Vol. 55, No. 1, January/February 2019, pp. 575–583

A Bidirectional High-Efficiency Transformerless Converter with Common-Mode Decoupling for the Interconnection of AC and DC Grids
Fang Chen, Rolando Burgos, Dushan Boroyevich
IEEE Transactions on Power Electronics, Vol. 34, No. 2, February 2019, pp. 1317–1333

Ultralow Input-Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges
Bingyao Sun, Rolando Burgos, Dushan Boroyevich
IEEE Transactions on Power Electronics, Vol. 34, No. 2, February 2019, pp. 1382–1393

Conference Papers

Critical-Mode-Based Soft-Switching Modulation for Three-Phase Rectifiers
Zhengrong Huang, Zhengyang Liu, Fred C. Lee, Qiang Li, Furong Xiao
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 16–23

A Novel Soft Switching ZVS, Sinusoidal Input Boundary Current Mode Control of 6-Switch Three Phase 2-Level Boost Rectifier for Active and Active + Reactive Power Generation
Nidhi Haryani, Bingyao Sun, Rolando Burgos
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 8–15

A WBG Based Three Phase 12.5 Kw 500 Khz CLLC Resonant Converter with Integrated PCB Winding Transformer
Bin Li, Qiang Li, Fred C. Lee.
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 469–475

Comparison Between Desaturation Sensing and Rogowski Coil Current Sensing for Protection of 1.2 kV, 300 a SiC MOSFET Module
Slavko Mocevic, Jun Wang, Rolando Burgos, Dushan Boroyevich
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 2666–2672

Analysis and Design of an Overcurrent Protection Scheme Based on Parasitic Inductance of SiC MOSFET Power Module
Keyao Sun, Jun Wang, Rolando Burgos, Dushan Boroyevich, Yonghan Kang
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 2806–2812

Modeling and Control of Sigma Converter for 48V Voltage Regulator Application
Virginia Li, Mohamed Ahmed, Qiang Li, Fred C. Lee
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 1199–1204

Modeling Resonant Converters in a Rotating Polar Coordinate
Yi-Hsun Hsieh, Fred C. Lee
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 938–943

Magnetic Paste As Feedstock for Additive Manufacturing of Power Magnetics
Chao Ding, Lanbing Liu, Yunhui Mei, Khai Ngo, Guo-Quan Lu
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 615–618

Harmonic Current Analysis of the Active Front End System in the Presence of Grid Voltage Disturbance
Bo Wen, Paolo Mattavelli
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 499–504

Analysis and Control of a Transformerless Series Injector Based on Paralleled H-Bridge Converters for Measuring Impedance of Three-Phase AC Power Systems
Zeng Liu, Igor Cvetkovic, Zhiyu Shen, Dushan Boroyevich, Rolando Burgos
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 1841–1845

Wideband Small-Signal Input dq Admittance Modeling of Six-Pulse Diode Rectifiers
Xiaolong Yue, Xiongfei Wang, Frede Blaabjerg, Dushan Boroyevich, Rolando Burgos
2018 APEC (IEEE Applied Power Electronics Conference & Exposition), San Antonio, TX, March 4–8, 2018, pp. 1981–1988

Trends in SiC MOSFET Threshold Voltage and ON-Resistance Measurements from Thermal Cycling and Electrical Switching Stresses
Joseph P. Kozak, Douglas J. DeVoto, Joshua J. Major, Khai Ngo
10th International Conference on Integrated Power Electronics (CIPS 2018), Stuttgart, Germany, March 20–22, 2018, pp. 1–6

Effect of Substrate Surface Finish on Bonding Strength of Pressure-Less Sintered Silver Die-Attach
Meiyu Wang, Yunhui Mei, Rolando Burgos, Dushan Boroyevich, Guo-Quan Lu
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Development of a Highly Integrated 10-kV SiC MOSFET Power Module with a Direct Jet Impingement Cooling System
Bassem Mouawad, Robert Skuriat, Jianfeng Li, C Mark Johnson, Christina DiMarino
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High-Frequency High-Density Bidirectional EV Charger
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Qiong Wang, Rolando Burgos
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Modeling and Optimization of High-Frequency Litz-Wire Transformer for 10 kW LLC Resonant Converter
Bingyao Sun, Rolando Burgos
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EMI Study on Control Implementation in PEBB-based Converter
Jianghui Yu, Rolando Burgos, Dushan Boroyevich
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Hierarchical Weight Optimization Design of Aircraft Power Electronics Systems Using Metaheuristic Optimization Methods
Qian Li, Rolando Burgos, Dushan Boroyevich
2018 AIAA/IEEE Electric Aircraft Technologies Symposium (EATS) Cincinnati, OH, July 12–14, 2018, pp. 1–10

Modeling of the Modular Multilevel Converters Based on the State-Plane Analysis and ΣΔ Coordinate Transformation
Yi-Hsun Hsieh, Fred C. Lee
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ZVS Turn-on Triangular Current Mode (TCM) Control for Three Phase 2-Level Inverters with Reactive Power Control
Nidhi Haryani, Bingyao Sun, Rolando Burgos
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 4940–4947

10 kW High Efficiency Compact GaN-Based DC/DC Converter Design
Bingyao Sun, Rolando Burgos, Sandeep Bala, Jing Xu
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 6307–6313

A High-Speed Gate Driver with PCB-Embedded Rogowski Switch Current Sensor for a 10 kV, 240 A, SiC MOSFET Module
Jun Wang, Slavko Mocevic, Christina DiMarino, Rolando Burgos, Dushan Boroyevich
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 5489–5494

A Novel ZVS Turn-On Triangular Current Mode Control with Phase Synchronization for Three Level Inverters
Nidhi Haryani, Sung Jae Ohn, Jiewen Hu, Paul Rankin, Rolando Burgos, Dushan Boroyevich
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 2207–2214

Accurate Small-Signal Modeling of Resonant Converter Based on Perturbation on the State Plane
Yi-Hsun Hsieh, Fred C. Lee
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 6809–6816

Assessment of Switching Frequency Effect on a Compact Three-Phase GaN-Based Inverter Design
Bingyao Sun, Rolando Burgos
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 868–875

Coil and Circuit Design of Omnidirectional Wireless Power Transfer System for Portable Device Application
Junjie Feng, Qiang Li, Fred C. Lee
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 914–920

Desaturation Detection for Paralleled GaN E-HEMT Phase Leg
Yingying Gui, Bingyao Sun, Rolando Burgos, Jing Xu, Sandeep Bala
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 3503–3509

A Voltage-Controlled Capacitor with Wide Capacitance Range
Lujie Zhang, Khai Ngo
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 7050–7054

Design and Control of Tunable Piezoelectric Transformer Based DC/DC Converter
Le Wang, Qiong Wang, Mudit Khanna, Rolando Burgos, Khai Ngo, Alfredo Vazquez Carazo
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 5987–5993

Digital-Based Soft-Switching Modulation for High-Frequency Three-Phase Inverters with Reactive Power Transfer Capability
Zhengrong Huang, Qiang Li, Fred C. Lee
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 6751–6758

High Frequency Small Signal Model for Inverse Charge Constant On-Time (IQCOT) Control
Syed Bari, Qiang Li, Fred C. Lee
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 6000–6007

Current-Transformer Based Gate-Drive Power Supply with Reinforced Isolation
Jiewen Hu, Jun Wang, Rolando Burgos, Dushan Boroyevich
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 6328–6335

Loss Model and Optimization Method of Switched-Capacitor Divider for POL Application
Owen Jong, Qiang Li, Fred C. Lee, Brian Carpenter
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 3844–3850

Magnetic Integration into SiC Power Module for Current Balancing
Zichen Miao, Khai Ngo
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 5839–5846

Phase Current Sensor and Short-Circuit Detection based on Rogowski Coils Integrated on Gate Driver for 1.2 kV SiC MOSFET Half-Bridge Module
Slavko Mocevic, Jun Wang, Rolando Burgos, Dushan Boroyevich, Marko Jaksic, Mehrdad Teimor, Brian Peaslee
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 393–400

Resonant Cross-Commutated Point-of-Load Converter
Ting Ge, Brian Carpenter, Khai Ngo
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 162–167

Three Terminal Common-Mode EMI Model and EMI Mitigation Strategy for Full SiC UPS
Sungjae Ohn, Jianghui Yu, Paul Rankin, Rolando Burgos, Dushan Boroyeivch, Harish Suryanarayana, Christopher Belcastro
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23-27, 2018, pp. 2094–2101

Electrical Field Analysis and Insulation Evaluation of a 6 kV H-bridge Power Electronics Building Block (PEBB) using 10 kV SiC MOSFET Devices
Yue Xu, Mona Ghessemi, Jun Wang, Rolando Burgos, Dushan Boroyevich
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 2428–2435

Utility-Scale PV Generator Impedances in DQ Frame under Different Q Control Modes
Ye Tang, Rolando Burgos, Chi Li, Dushan Boroyevich
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 3725–3731

Zero Common-Mode Voltage Three-Level Buck DC-DC Converter Using 1.2 kV SiC MOSFET Neutral-Point-Clamped (NPC) Modules for UPS Applications
Paul Rankin, Sungjae Ohn, Jianghui Yu, Rolando Burgos, Dushan Boroyevich, Harish Suryanarayana, Christopher Belcastro
2018 IEEE Energy Conversion Congress & Expo (ECCE), Oregan Convention Center, Portland, OR, September 23–27, 2018, pp. 2086–2093

Control of Modular Multilevel Converters Based on the State-Plane Analysis and Coordinate Transformation
Yi-Hsun Hsieh, Fred C. Lee
44th Annual Conference of the IEEE Industrial Electronics Society (IECON 2018), Washington, DC, October 21–23, 2018, pp. 3932–3937

A High Frequency High Efficiency GaN-Based Bi-Directional 48V/12V Converter with PCB Coupled Inductor for Mild Hybrid Vehicle
Bin Li, Wei Qin, Yuchen Yang, Qiang Li, Fred C. Lee, Dong Liu
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Yuchen Yang
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Jiewen Hu
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Slavko Mocevic
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Paul Rankin
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Qiong Wang
Dissertation, May 9, 2018

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Yingying Gui
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Resonant Cross-Commutated DC-DC Regulators with Omni-Coupled Inductors
Ting Ge
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Impedance-Based Stability Analysis in Power Systems with Multiple STATCOMs in Proximity
Chi Li
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Bingyao Sun
Dissertation, August 10, 2018

High Frequency Bi-Directional DC/DC Converter with Integrated Magnetics for Battery Charger Application
Bin Li
Dissertation, September 10, 2018

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Victor Turriate
Thesis, September 20, 2018

Design and Validation of a High-Density 10 kV Silicon Carbide MOSFET Power Module with Reduced Electric Field Strength and Integrated Common-Mode Screen
Christina DiMarino
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Owen Jong
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Sungjae Ohn
Dissertation, February 22, 2019

CPES Research Volumes

Each volume below is a collection of papers organized by technology topic generated by CPES researchers over the years.

Volume I: High-Frequency Resonant, Quasi-Resonant, and Multi-Resonant Converters
1989

Volume II: Modeling, Analysis, and Design of PWM Converters
1990

Volume III: Power Devices and their Applications
1991

Volume IV: High-Frequency Resonant and Soft-Switching PWM Converters
1992

Volume V: Switching Rectifiers for Power Factor Correction
1994

Volume VI: Power Electronics Components and Circuit Modeling and Analysis
1995

Volume VII: Advanced Power Conversion Techniques
1995

Volume VIII: Converters and Distributed Power Systems
1995

Volume IX: Low Voltage Power Conversion and Distributed Power Systems
2000

Volume X: Integrated Power Electronics Module -- a Building Block Concept for System Integration
2000

Volume XI: Advanced Soft-Switching Techniques, Device and Circuit Applications
2000

Volume XII: Conducted EMI and Power Electronics: Characterization and Mitigation
2008

Volume XIII-Book 1: Systems-Based Power Electronics Integration Technology
2008

Volume XIII-Book 2: Systems-Based Power Electronics Integration Technology
2008

Volume XIV: Distributed Power Systems Front-End Converters: Power Factor Correction and Isolated Converters
2008

Volume XV: Distributed Power Systems: Point-of-Load Converters
2008

Volume XVI: Distributed Power Systems: Front-End Converters (Part II)
2016

Volume XVII: Distributed Power Systems: Point-of-Load Converters (Part II)
2016

Volume XVIII: Wide-Bandgap Power Devices and Applications
2016

2018 Charter

Short-Term/Long-Term Goals

Over the past four decades, CPES has developed promising new power electronics technologies, including new types of power semiconductor devices, high-frequency magnetics, soft-switching technologies that significantly reduce switching losses and electromagnetic interference (EMI), advanced materials and packaging technologies with planar interconnect processes, integrated sensors, and thermomechanical integration. These technologies collectively serve as the mainstay for the successful integration of modular building blocks into power electronics.

Industry adoption of the integrated power electronic module (IPEM) approach began in earnest in the early 2000s for applications such as power management solutions for the new generation of microprocessors, power supplies for the IT industry, electric/hybrid vehicles, and photovoltaic inverters, as well as variable speed motor drives for applications ranging from industry automation and process control to home appliances. These core technologies offer the promise of higher performance at a lower cost with improved reliability. CPES is poised to extend these core competencies to a wide range of new and emerging applications.

We expect the emergence of wide bandgap semiconductors to make it possible to operate converters at significantly higher switching frequencies, efficiency, and power density, and to operate at elevated temperatures. This new generation of wide bandgap devices is poised to make a significant impact on the marketplace currently dominated by silicon power devices. These high-frequency and higher-temperature devices require advanced packaging technologies, together with high-temperature interface materials, passive components, and improved thermal management. CPES has unique strengths in these areas, and is a member of the PowerAmerica Institute led by North Carolina State University. This institute has been established as an alliance of eighteen corporations, five universities and two government labs. The program was initiated in early 2015 with a total budget of $140 million over five years aimed at developing wide bandgap power services and associated system applications.

As the new generation of devices operate at significantly higher switching frequencies, power quality and electromagnetic interference and compatibility (EMI/EMC) have become increasingly important. CPES has pioneered a number of innovative technologies leading to significant improvements in power quality and EMI/EMC performance, and we plan to integrate these features directly into the next generation of power conversion systems. CPES researchers are well-positioned to play a leading role in helping industry and government agencies find high-performance, cost-effective solutions.

With ever-increasing current consumption and clock frequencies, today's microprocessors are operating at very low voltages

(one volt or less) and continuously switching between "sleep mode" and "wake-up mode" to conserve energy. This imposes a significant challenge to power delivery and management. Over the past 15 years, with the steady support of over 20 corporations, CPES developed a multi-phase voltage regulator (VR) module to power new generations of Intel microprocessors. This research project generated more than 30 U.S. patents, covering such areas as power delivery architecture; modularity and scalability; control and sensing; current sharing; integrated magnetics; and advanced packaging and integration. Today, every PC and server microprocessor in the world is powered with this multiphase VR.

These technologies have been further extended to high-performance graphical processors, server chipsets and memory devices, networks, telecommunications, and all forms of mobile electronics, including smartphones. This research is structured as the Power Management Consortium (PMC) within the Center's Industry Consortium Program, which has over 80 participating members. The research scope of this mini-consortium has expanded in recent years to include power architecture and the management of data centers, telecommunications equipment, LED lighting, and PV converter/inverters.

Following the success of the PMC, CPES built upon its core strengths and launched two new mini-consortia in 2011: the mini-consortium on High Density Integration (HDI) and the mini-consortium on Renewable Energy and Nanogrids (REN). HDI evolved as an extension of the early work supported under the NSF-ERC years to further develop IPEMs and system integration technology based on the new generation of wide bandgap power semiconductors that were emerging. This research leverages the availability of wide bandgap power semiconductors, as well as high-temperature passive components and ancillary functions. The switching frequency is pushed as high as component technologies, thermal management, and reliability permit. At the same time, the maximum component temperatures are pushed as high as component technologies, thermal management, and reliability permit.

REN on the other hand was created with the intent to consolidate the steady growth that CPES had in high power applications, focusing on high-power and medium-voltage power conversion technologies to facilitate the integration of renewable energy sources, such as offshore wind farms, PV farms, and energy storage systems into the existing electrical grid. Later, due to the strong focus on the adoption of WBG devices in higher power applications, REN was relaunched as the Wide Bandgap High Power Converters and Systems (WBG-HPCS) mini-consortium to better reflect the expanded scope of work. Under this new name, WBG-HPCS aims at consolidating and furthering the Center's strength surrounding WBG-based modular, multilevel power converters and high-power density high-power converters for grid, industrial, and transportation applications. It continues to strengthen and grow expertise on electronic power systems—defined as electrical systems with a high penetration of power converters. CPES continues to lead investigations on the dynamic impact these converters have on power systems, targeting ac and dc low-voltage and medium-voltage distribution systems, up to high-voltage transmission systems.

CPES has established one of the largest university/industry partnership programs in the US and has developed an innovative process for moving technology and intellectual property out of academic laboratories and into the marketplace. This process enables critical technologies developed by the Center to permeate all forms of power electronics equipment and systems, and has profoundly affected the design and manufacturing process of the industry. With an increasing level of industry participation, more than 42 industry-funded graduate fellowships are made available to CPES students annually, with industry members serving as mentors in the students' research. This unique industry/university collaboration was cited by the National Science Foundation (NSF) as a model ERC for its education/outreach program, industry collaboration, and technology transfer program. This program has continued to flourish since CPES graduated from the NSF ERC in 2008.

Resource Needs and Funding

CPES is a long-standing center, originally established in 1983 as VPEC (Virginia Power Electronics Center). Its continued support is expected to be consistent with the present sources of funding. The Center is supported by both sponsored research, presently at about $2.9 million per year, and industry member support, presently an additional $2.6 million annually. Returned overhead is an additional source of support.

CPES has a Memorandum of Understanding (MOU) for the distribution of overhead. This agreement is reviewed periodically as new opportunities arise. The last MOU was signed by all parties in 2014.

Participation and Governance

CPES is made up of the highest level of faculty in the area of power electronics and power electronics systems. Top-caliber students from electrical engineering programs worldwide pursue their masters and doctorate degrees at CPES-Virginia Tech, and in turn are heavily recruited after graduation, many by our industry partners.

CPES is administratively established as a suborganization under the College of Engineering. The Center director, Dushan Boroyevich, reports to the Dean, and together they identify initiatives to enhance the position and contributions of the Center within the university, industry, and the world.

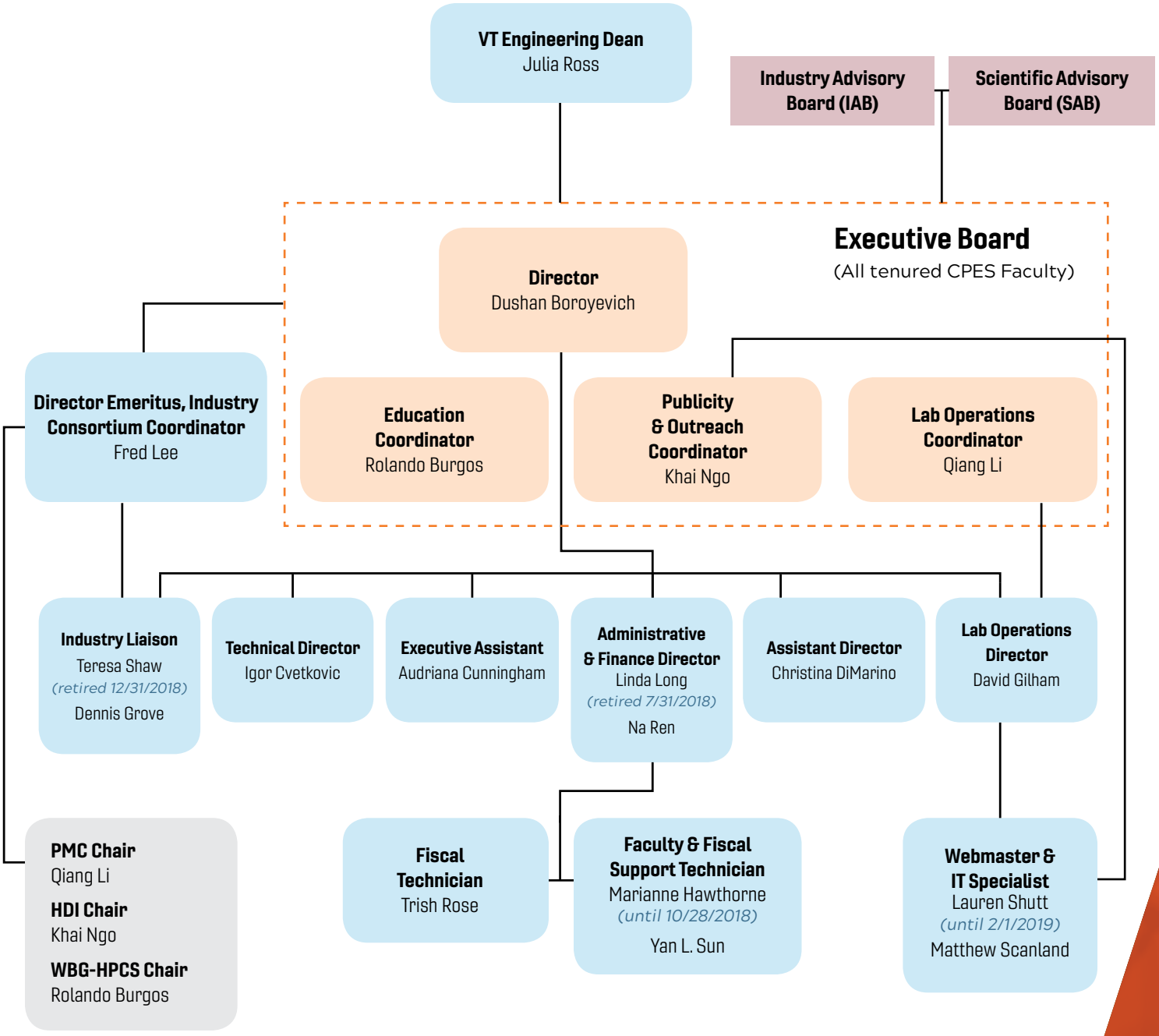
Boroyevich is supported in his role by Director Emeritus Fred C. Lee. For daily operations of the Center, Boroyevich is assisted by an executive board comprised of tenured faculty within CPES. Each faculty member plays a role as coordinator of one of four areas: Industry Consortium, Education, Publicity and Outreach and Lab Operations.

For long-term strategies, Boroyevich and Lee receive counsel from the CPES Industry Advisory Board (IAB) and the CPES Scientific Advisory Board (SAB).

The Industry Advisory Board represents industry interests and advises the CPES Director on programmatic matters. The board is made up of an elected Chair and Co-Chair, representatives from all Principal Plus and Principal Members, and Associate Member representation equal to 20% of the total number of Associate Members, or one less than the total number of Principal-level Members.

The Scientific Advisory Board reviews the Center's vision and strategic research plan, and offers critiques and guidance regarding the Center's research vision and its programmatic approach to ensure that the Center's research program maintains a focus on its long-term goals.

CPES Management Structure



Research Nuggets

Power Management Consortium (PMC) Nuggets

GaN-Based High-Density Unregulated LLC Converters for Two-Stage 48 V VRM

Sigma Converter 48 V VRM With Wide Voltage Range

Optimized Design of Integrated PCB-Winding Transformer for MHz LLC Converter

Shielding Study of a 6.78 MHz Omnidirectional Wireless Power Transfer System

Soft Switching Realization of LCCL-LC Resonant Converter for Wireless Power Transfer Application

3 kW Three-Phase Interleaved LLC Converter with Integrated Magnetics for 48 V Output

Accurate Small-Signal Equivalent Circuit Model for Resonant Converters

Critical-Mode-Based Soft-Switching Modulation for High-Frequency Three-Phase Bidirectional AC-DC Converters

Leakage Current Suppression with Critical-Mode-Based Soft-Switching Modulation for Three-Phase Inverters in PV Application

Resonant Switched-Capacitor Converter with Multi-Resonant Frequencies

Improved V^2 Constant On-Time Control with State-Trajectory Control

Simplified Optimal Trajectory Control for 1 MHz LLC Converter with Wide Input Voltage Range

Magnetic Integration of 3 kW LLC Converter for Front-end Power Supply in 48 V Power Architecture

Digital Implementation of Light-Load Efficiency Improvement for High-Frequency LLC Converters With Simplified Optimal Trajectory Control

Digital Implementation of Adaptive Synchronous Rectifier Driving Scheme for High-Frequency LLC Converters with Microcontroller

Single-Stage EMI Filter for Server Power Supply

High-Efficiency High-Power-Density 3 kW LLC Converter with Integrated PCB Winding Matrix Transformer

Shielding Technique for Planar Matrix Transformers to Suppress Common-Mode EMI Noise and Improve Efficiency

Improved Magnetic Design for 12.5 kW CLLC Resonant DC/DC On-Board Charger

A Wide Bandgap-Based Three-Phase 12.5 kW 500 kHz CLLC Resonant Converter with Integrated PCB Winding Transformer

20 MHz, Three-Via 2 Phase Inverse Coupled Inductor Design for Integrated Voltage Regulator for Smartphone Applications

Improved Partial Cancellation Method for High-Frequency Core Loss Measurement

GaN-Based High-Density Unregulated LLC Converters for Two-Stage 48 V VRM

With the rapid increase of power consumption at data centers, efficient power management solutions and architectures are gaining more attention. While telecom applications have used 48 V voltage regulator modules (VRMs) for years, a recent study indicates 48 V VRMs may be more efficient and cost-effective for data center applications, compared to the 12 V VRMs typically used.

Two-stage 48 V VRM architecture can help achieve the required efficiency and power density for the targeted application with a quicker integration to the existing data centers. As shown in Fig.1, the first stage is an unregulated dc-dc (DCX) converter stepping down the input voltage to an intermediate bus voltage and is followed by the mature technology of a multi-phase buck converter. The soft switching capabilities of the first stage, combined with the simplicity and scalability of the second stage, promote this solution as a suitable candidate for future data centers to achieve the required efficiency and power density. One key element to achieve these goals is the first stage unregulated converter design.

In this work, a LLC converter with matrix transformer structure is proposed for the first-stage converter. Two DCX converters are designed with different transformation ratios to evaluate the overall efficiency of the two stages with different intermediate bus voltages. With GaN devices and integrated magnetic structure, the two converter prototypes shown in Fig. 2 are designed, and can achieve very high efficiency (>98 percent) and power density (>1200 W/in^3). The efficiency of the two stages is then evaluated with the conclusion that 6 V for the intermediate bus will help achieve higher efficiency for the two-stage architecture.

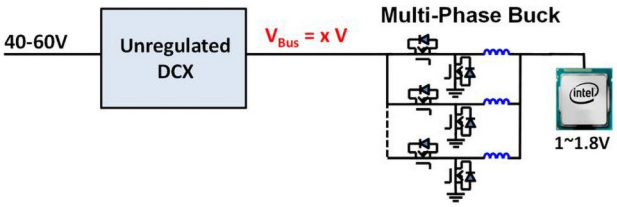


Fig. 1. Two-stage 48 V VRM Solution.

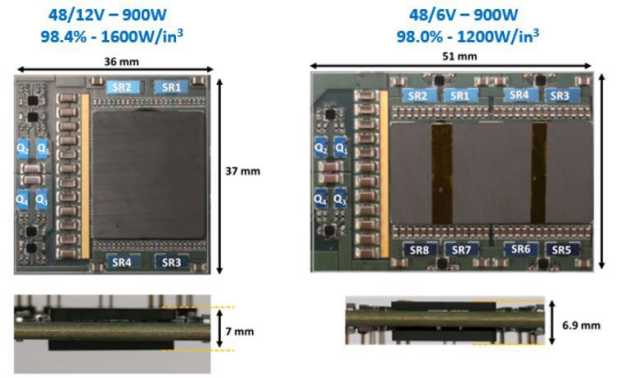


Fig. 2. High efficiency and density GaN-based 48/x V prototypes.

Sigma Converter 48 V VRM With Wide Voltage Range

With the ever-increasing demands of cloud computing, big data processing, and cryptocurrency mining, by the year 2020 a 10 percent share of the total power consumption will be required by U.S. data centers and telecommunication applications. Replacing 12 V bus distribution with a 48 V bus distribution system in data centers has been proposed and later adopted by Google. This architecture creates a challenge for voltage regulator module (VRM) design being placed near the CPU. The designed VRM must operate at very high efficiency with high power density.

In this work, a magnetic integration method is proposed for regulated LLC converters where a printed circuit board (PCB) winding matrix transformer and resonant inductor are integrated using a single core structure with minimum winding requirements. The proposed LLC converter with integrated magnetic structure is utilized in the Sigma converter architecture shown in Fig. 1 for VRM powering the CPU. By realizing a variable gain LLC converter, the Sigma converter is able to operate efficiently with wide input and output voltage ranges to meet the CPU requirements. Comparing with two stage solutions, the power flow in the Sigma converter is shared between two converters with ratio determined with the input voltage across each converter resulting in higher conversion efficiency.

The Sigma converter prototype shown in Fig. 2 is built to operate with an input voltage range of 40-60 V with an output voltage range of 1.3-1.85 V. The LLC converter with matrix transformer structure integrates six transformers and a resonant inductor using a single-core structure and PCB winding. The buck converter used for regulating the output voltage is built using GaN devices and a PCB winding inductor. The designed converter provides a maximum output current of 100 A, while achieving a maximum efficiency of 95 percent and power density of 650 W/in^3.

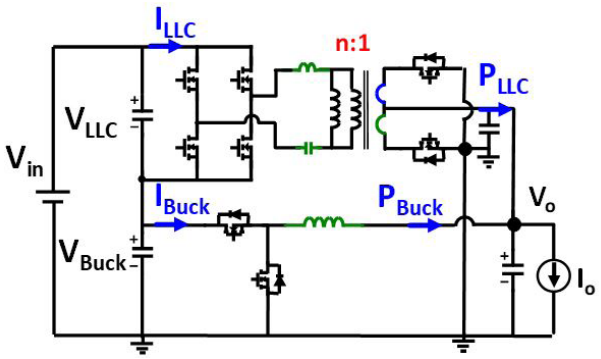


Fig. 1. One stage 48/1 V sigma converter power architecture.

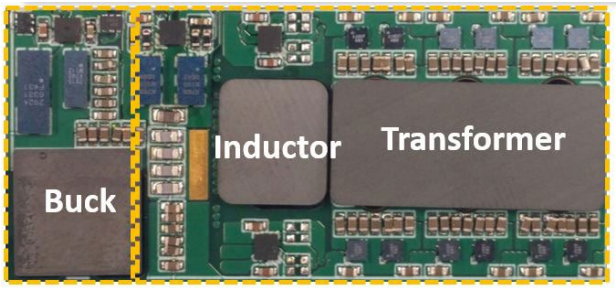


Fig. 2. Sigma converter prototype.

Optimized Design of Integrated PCB-Winding Transformer for MHz LLC Converter

Intermediate bus architecture employing 48 V bus converters is widely used in power supply applications. With the rapid increase of demanded power by these loads, higher effi-ciency and power density are sought-after for better performance power management solu-tions. In this paper, a Gallium Nitride (GaN) based design of a two-stage solution is proposed. The first stage is a multi-phase buck applied for regulation. The second stage is an LLC con-verter with fixed switching frequency applied for isolation. The design and optimization of an LLC matrix transformer are studied. Fig. 1 shows the circuit diagram of the studied LLC.

First, a novel termination and via structure of the primary windings is proposed resulting in significant loss reduction. In this structure, both terminations and vias are interleaved. The leakage flux is reduced and, as a result, the ac losses caused by an eddy current are reduced. Second, to minimize the winding loss, an overlapped winding structure is proposed. The new structure achieves improved interleaving and less current crowding. The loss reduction is verified by finite element analysis simulation results. Third, the traditional structure with parallel windings also suffers from poor current sharing between layers. To address this issue, a symmetrical winding layer arrangement with alternating magnetomotive force is proposed. Better current sharing is achieved and proven in the simulation.

In summary, the design and optimization of a high-frequency, high-current bus converter is developed. The hardware prototype is built with a 14 layer-PCB board and a customized planar transformer. The prototype is shown in Fig. 2, with the LLC part populated. The efficiency curve of the second-stage LLC is shown in Fig.2 with 97.8 percent peak efficiency. Finally, the two-stage converter is developed and tested. It achieves a high peak efficiency of 96 percent and a power density of 615 W/in^3.

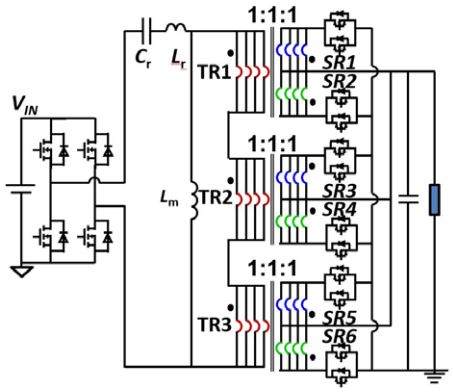


Fig. 1. Circuit diagram of the second-stage LLC.

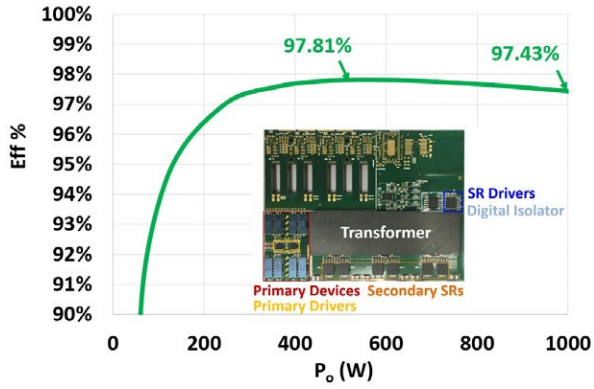


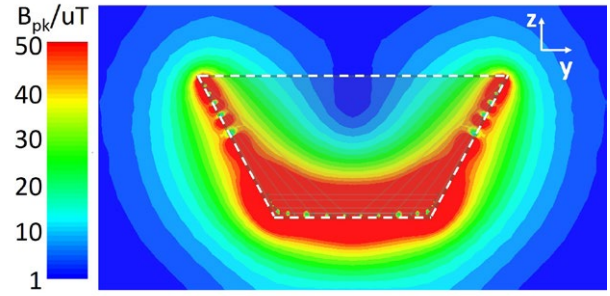
Fig. 2. Two-stage converter prototype and LLC efficiency.

Shielding Study of a 6.78 MHz Omnidirectional Wireless Power Transfer System

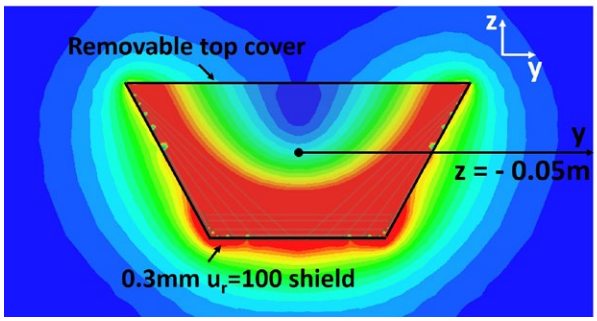
Wireless power transfer (WPT) is a promising solution to deliver power to a battery in a variety of applications and the near field inductive power transfer technology has been widely adopted in consumer electronics applications. A three-dimensional WPT system with omnidirectional power transfer capability is preferred due to the spatial charging freedom. In this nugget, a square-shaped wireless charging bowl is proposed and the transmitter coils structure is shown in Fig. 1.

An important design concern of the inductive power transfer system is the safety issue related to human exposure to electromagnetic fields (EMF). Several guiding regulation documents have been established to prevent adverse health effects due to the EMF. To comply with the regulation standards, a ferrite shield is added to reduce the stray field level. In the proposed setup, the ferrite shield layer is wrapped around the charging bowl to confine the magnetic field. The field distribution on the yz plane cases, with a ferrite shield and without a ferrite shield, are shown in Fig. 2(a) and (b), respectively. It is important to note, the stray field outside the charging bowl decreases but the attenuation is not enough due to the small permeability of the available high frequency (6.78 MHz) ferrite material.

To further reduce the stray field level, a conductive layer is added in addition to the ferrite layer. The field distribution on the yz plane after this addition is shown in Fig. 3. The stray field outside the bowl is effectively attenuated through the induction of eddy-current within the conductive layer. Thanks to the help of the ferrite layer, the magnetic field inside the bowl does not change much. Therefore, the power transfer capability will not suffer even with the conductive layer. Finally, according to the Finite Element Analysis simulation, the eddy current loss in the conductive layer is around 1 mW. However, the ferrite loss is around 0.3 W at 5 W output and the system efficiency drops from 82 percent to 78 percent after adding the double-layer shield.



(a)



(b)

Fig. 2. The field distribution on yz plane (a) without shield case, and (b) with a 0.3 mm ferrite (u_r = 100) shield.

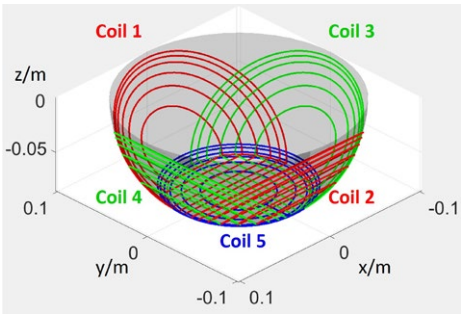


Fig. 1. The proposed square shaped charging bowl.

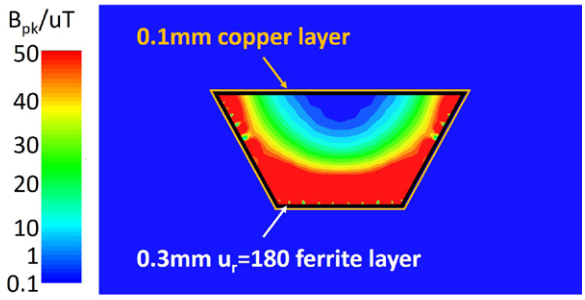


Fig. 3. Field distribution with the double layer shield.

Soft Switching Realization of LCCL-LC Resonant Converter for Wireless Power Transfer Application

Wireless power transfer (WPT) with loosely coupled coils is a promising solution to deliver power to a battery in consumer electronics application. The LCCL-LC resonant converter, as shown in Fig. 1, is a promising topology due to the current source characteristics of the transmitter coil current.

Soft-switching is essential to reduce the switching related loss and electromagnetic interference noise for a 6.78 MHz system. To achieve zero voltage switching (ZVS) for the LCCL-LC converter, the turnoff current of the primary devices must be high enough to discharge the junction capacitor (C_{oss}) of the devices during the dead-time period. In this nugget, a newly-derived analytical model to calculate the turnoff current of the LCCL-LC resonant converter reveals that the turnoff current is independent of the load and coupling condition in single-phase operation. Therefore, the ZVS condition is satisfied by careful design in different operating conditions.

In an omnidirectional WPT system, there are multiple transmitter coils and the ZVS condition for the LCCL-LC resonant converter in multiple phase operation is analyzed. It is found that the ZVS condition is related to the phase relationship among different transmitter coils current. If the excitation current of different transmitter coils is in the same phase, the turnoff current equation is the same as the single-phase case and the ZVS condition is independent of the load and coupling condition. However, the turnoff current is related to the load and coupling condition if there is some phase difference among different transmitter coils current. The schematic of a two-phase LCCL-LC circuit is shown in Fig. 2 and the experimental input voltage and current waveforms for different phase relationships is shown in Fig. 3. As shown here, ZVS is achieved in the first case but not in the second.

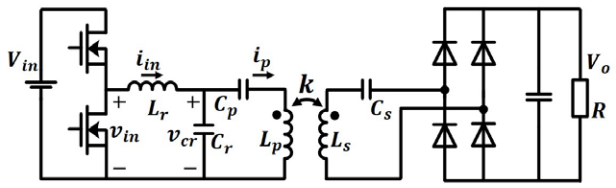


Fig. 1. The LCCL-LC resonant converter.

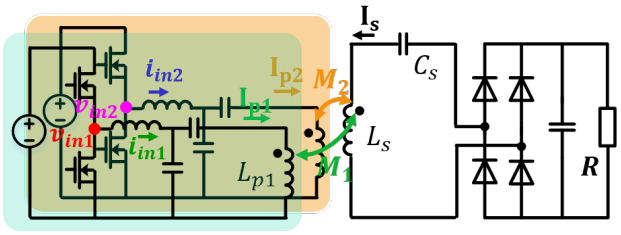
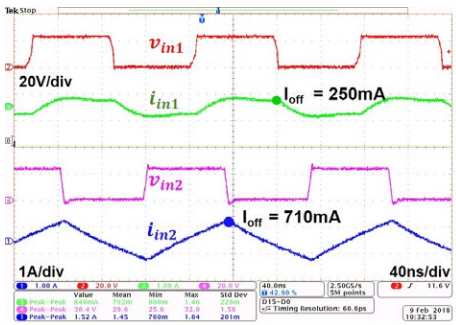
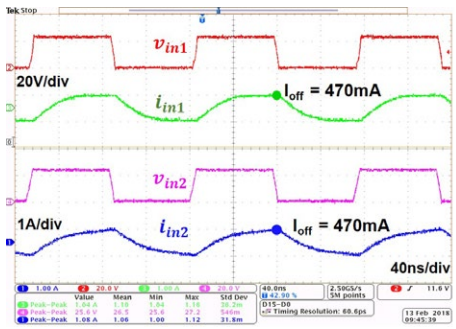


Fig. 2. The LCCL-LC converter in two-phase operation.



(a)



(b)

Fig. 3. The experimental waveforms of the input voltage and current in two-phase operation with (a) no phase difference between I_{p1} and I_{p2}, and (b) 90° phase difference between I_{p1} and I_{p2}.

3 kW Three-Phase Interleaved LLC Converter with Integrated Magnetics for 48 V Output

The LLC converter is the most suitable topology for dc-dc converters in server and telecom applications. In order to increase the output power and reduce the input and output current ripples, the three-phase interleaved LLC converter is becoming more and more popular. By conecting the three phases of the converter in a certain way, the three-phase LLC converter has the benefit of automatic current sharing. Different topologies of three-phase LLC converters are surveyed. A new topology suitable for high-frequency operation is proposed, as shown in Fig. 1. The proposed LLC converter employs a delta-connected resonant capacitor network in the primary side to achieve automatic current sharing, full-bridge secondary side due to high-frequency operation, and shielding technique to reduce common mode (CM) noise.

The three-phase LLC converter suffers the drawback of numerous and bulky magnetics. A novel magnetic structure is proposed to integrate three inductors and three transformers into one magnetic core. 600 V GaN devices from Panasonic Corporation and 80 V GaN devices from Efficient Power Conversion Corporation will be employed for the primary and secondary, respectively. By pushing the switching frequency up to 1MHz, all the windings for the magnetic structure can be implemented with 4-layer PCB winding. Additional 2-layer shielding is integrated in the PCB windings to reduce CM noise. A 1 MHz, 3 kW, 400 V/48 V, three-phase LLC converter with the proposed magnetic structure is designed with an estimated peak efficiency >98 percent, as shown in Fig. 2, and a power density of > 200 W/in^3.

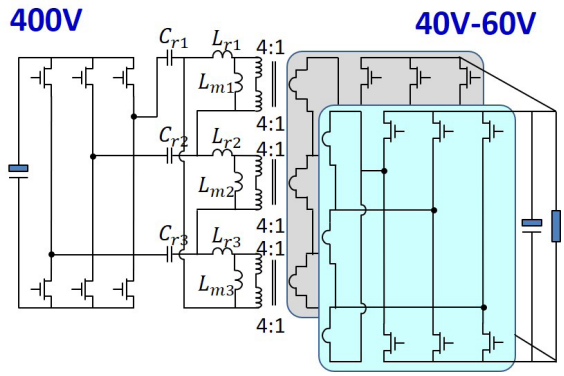


Fig. 1. Schematics.

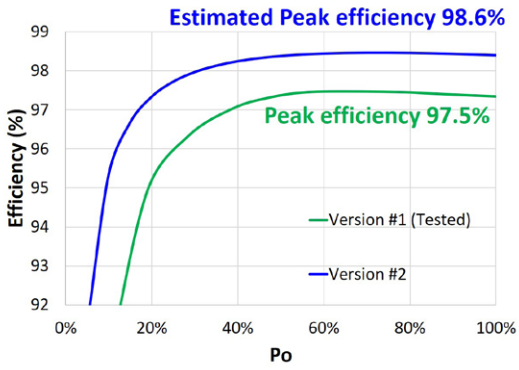


Fig. 2. Estimated efficiency.

Accurate Small-Signal Equivalent Circuit Model for Resonant Converters

Resonant converters, as shown in Fig. 1, are the preferred topologies of a wide range of applications. The major benefits of resonant converters, especially for LLC converters, are zero-voltage switching (ZVS) from zero to full load, low turn-off current of primary-side devices, zero-current switching (ZCS) of rectifiers, and circuit simplicity. Therefore, a power converter can be made efficient and compact. Despite decades of popularity, no simple and accurate small-signal model is available. One modeling approach is the discrete-time model. However, the result is overly complicated and often numerically solved. Moreover, there is no extension to an LLC converter using this method. The other approach is based on fundamental approximation in which the resonant tank operates as a good band-pass filter, which is normally not the case especially for LLC converters. As a result, the existing small-signal models work to a certain extent for SRCs but not LLC converters.

A new modeling approach is proposed based on an extended describing function. Referring to Fig. 1, the non-linear part of the resonant converter, which consists of an inverter, resonant tank, rectifier, and voltage-controlled oscillator (VCO), is first identified. Using superposition theory, the describing functions of the non-linear part subject to control, input voltage, and output voltage excitations are derived. Combining the non-linear part to the rest of the linear circuit, a simple equivalent circuit model is proposed and shown in Fig. 2. Without any assumption, the proposed small-signal model is accurate beyond switching frequency.

The proposed equivalent circuit model indicates, not surprisingly, a resonant converter is an infinite-pole system. For controller design and dynamic analysis, the frequency of interest is lower than the switching frequency in most cases. Ignoring high frequency poles, a simplified equivalent circuit model is proposed and shown in Fig 3. The small-signal behavior is well-explained with the simplified equivalent circuit model, including the beat-frequency double pole (from resonance between L_e and C_e) and the energy stored in the resonant tank (L_e). Furthermore, the right-half-plane (RHP) zero (caused by negative R_z) is predicted and explained for the first time for resonant converters. The prediction of the RHP zero is a significant contribution for an optimal controller design.

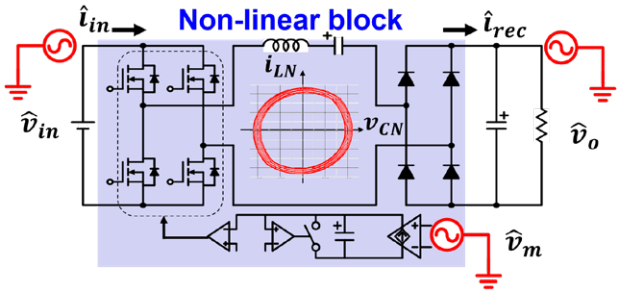


Fig. 1. Perturbation to a series resonant converter.

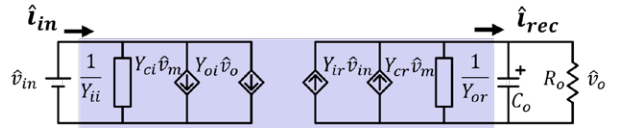


Fig. 2. Proposed small-signal model.

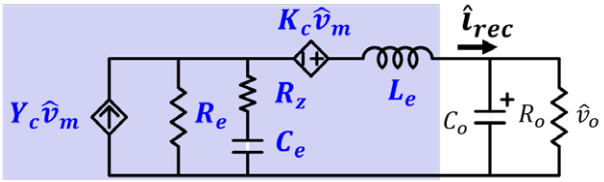


Fig. 3. Simplified small-signal equivalent circuit model observed from output side.

Critical-Mode-Based Soft-Switching Modulation for High-Frequency Three-Phase Bidirectional AC-DC Converters

For wide-bandgap (WBG) semiconductor device-based high-frequency power conversion systems, the high power density is achieved through size reduction of filters made up of passive components. Since WBG devices show negligible turn-off energy when compared with the turn-on energy, critical conduction mode (CRM) operation zero voltage switch (ZVS) soft switching is preferred to achieve high efficiency.

According to the literature, however, in order to achieve independent CRM control and therefore ZVS soft switching in three-phase ac-dc systems, extra components and connections are required. This requirement adds to system complexity and leads to some limitations under high modulation index conditions, showing extremely wide switching frequency variation and the associated high switching related loss. Therefore, a novel CRM-based soft-switching modulation is proposed for a bidirectional three-phase ac-dc converter. In this modulation, CRM operation with ZVS soft switching is still the foundation. With two total control freedoms among three phases, discontinuous pulse width modulation (DPWM) is adopted by clamping one phase to enable independent control in the other two phases. Switching frequency synchronization implemented by discontinuous conduction mode (DCM) operation is applied to limit switching frequency variation. With the proposed modulation, the switching frequency range is 300 kHz ~ 500 kHz at full load.

With the proposed modulation technique, at any line cycle operating point, the first phase is clamped and uncontrolled, the second phase operates at CRM, while the third phase operates at DCM. Under a high modulation index (>0.8) for each phase, ZVS turn-on of the control switch in each switching cycle is naturally achieved during CRM operation in the inverter mode. At the same time, the conclusion is totally opposite in the rectifier mode and therefore off-time extension is always required in the rectifier mode during CRM operation. The lower modulation index introduces the tendency of losing the capability of natural ZVS for the inverter mode operation during CRM, while introducing the tendency of gaining the capability of natural ZVS for the rectifier mode operation during CRM. For each phase during DCM operation, for both inverter and rectifier modes, valley switching (in most cases ZVS) turn-on is always achieved by applying a slight turn-on delay to the control switch.

A 25 kW SiC (WBG) based three-phase bidirecitonal ac-dc converter prototype is built, as shown in Fig. 1. This prototype is designed to operate at above 300 kHz switching frequency with the proposed modulation, achieving 127 W/in^3 power density. Fig. 2 shows the efficiency of the converter prototype, and approximately 99 percent peak efficiency is achieved for bidirectional operation even with above 300 kHz switching frequency.

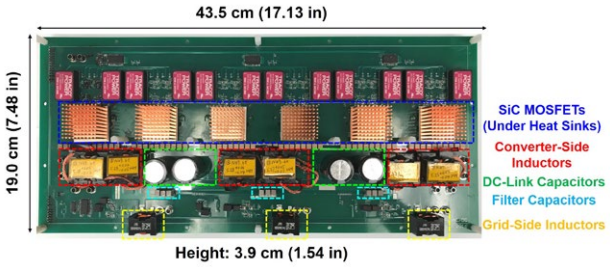


Fig. 1. Prototype of 25-kW SiC-based three-phase ac-dc converter.

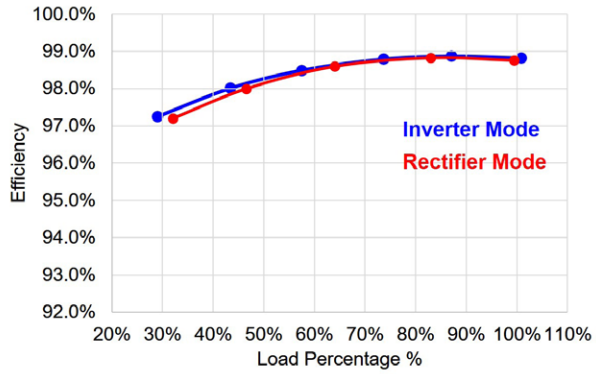


Fig. 2. Tested efficiency of the converter prototype.

Leakage Current Suppression with Critical-Mode-Based Soft-Switching Modulation for Three-Phase Inverters in PV Application

In photovoltaic (PV) system applications, large parasitic capacitance exists between the PV panel and the earth due to the relatively large area of the PV panel. This parasitic capacitance, combined with the power converter, the grounded power grid, and the earth, forms a closed electrical loop. Therefore, there is current flowing through this parasitic capacitance, which is called leakage current in PV system applications. For safety considerations, the root mean square value of the leakage current should be limited within 300 mA according to related standards in leakage current for PV system applications, otherwise protection will be triggered.

With the novel critical conduction mode (CRM)-based soft switching modulation technique applied into a wide-bandgap (WBG) semiconductor device-based high-frequency three-phase bidirectional ac-dc converter system, both high power density and high efficiency are achieved. A 25 kW silicon carbide (SiC)-based three-phase ac-dc converter prototype is built with greater than 300 kHz switching frequency operation under the novel CRM-based soft switching modulation. Approximately 99 percent peak efficiency and 127 W/in^3 power density are achieved. However, the limitation of high leakage current under the above soft switching modulation prevents its use in PV system applications.

Therefore, as shown in Fig. 1, the system topology is modified by adding two additional switches. The basic concept with these two additional switches is that isolation is provided by turning off the two switches during the freewheeling period in each switching cycle and therefore, the path for the leakage current is cut off in each switching cycle. Since the voltage across the parasitic capacitance cannot be suddenly changed, the accumulation of the leakage current is avoided so the much lower leakage current is achieved. In addition, adding a three-phase common mode (CM) choke is also beneficial for the suppression of leakage current. The simulation results of the leakage current before and after adding two additional switches under the CRM-based soft switching modulation is shown in Fig. 2.

With this modulation concept for the additional two switches, the independent control, narrow switching frequency variation range, and zero voltage switch (ZVS) or valley switching turn-on for all the switches can still be achieved. The only tradeoff due to the two additional switches is the slightly increased system conduction loss.

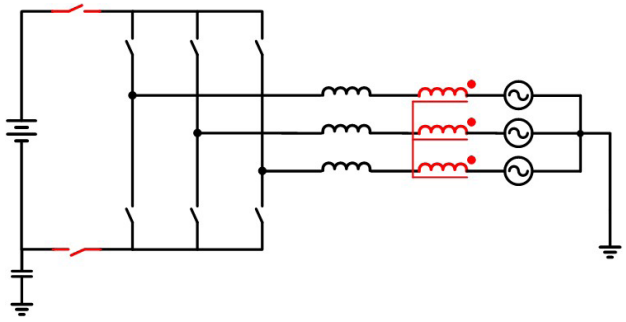


Fig. 1.. 8-switch topology for leakage current suppression.

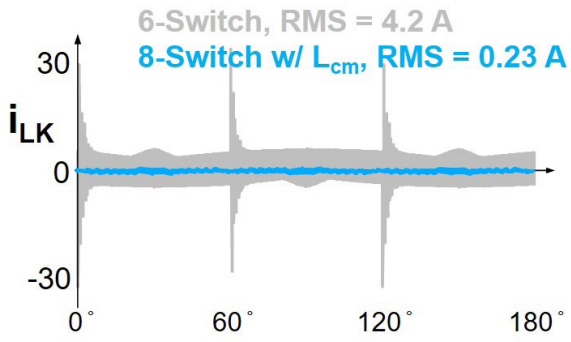


Fig. 2. Simulation result comparison before and after topology modification.

Resonant Switched-Capacitor Converter with Multi-Resonant Frequencies

Due to the increase in data processing, data center servers require high performance multi-core CPU and GPU installations that increase power consumption. This higher power consumption induces higher conduction loss along the bus and degrades whole system efficiency. Many leaders have proposed intermediate bus architecture using a 48 V distribution system to reduce conduction loss along the bus.

Google and North Dakota University expanded the concept of a resonant switched-capacitor converter (RSCC) introduced by Shoyama in 2004 into a higher voltage conversion ratio (VCR) DC transformer termed a switched-tank converter (STC). By operating switching frequency (f_{sw}) at an exact resonant frequency (f_o), a STC utilizes a zero-current switching (ZCS) soft-charging mechanism to achieve high efficiency. Regardless of ZCS, drain to source capacitance (C_{oss}) loss persists. ZCS operations of a STC requires stable resonant frequency. Consequently, class I ceramic capacitors, such as U2J dielectric capacitors, are appropriate. However, any component comes with tolerance which will affect the performance of STC un-less the component utilizes zero current detection control.

$$f_{sw} > f_o = \frac{1}{2\pi\sqrt{L_r C_2}} \quad \text{Eq. 1.}$$

$$C_r = (t_d/\pi)^2/L_r \quad \text{Eq. 2.}$$

Derived from a resonant switched-capacitor converter (RSCC), a multi-resonant switched-capacitor converter (MRSCC) adds a small capacitor (C_r) in parallel to the resonant inductor (L_r) to form a high frequency resonant tank. By operating at $f_{sw} > f_o$, the MRSCC provides immunity towards resonant frequency variation of the tank. L_r resonates with C_r for half-period during dead-time (t_d) to reverse the current direction of L_r before the next conduction state starts, as shown in Eq.2. By doing so, the MRSCC reshapes the inductor current to more like a square-wave and further reduces conduction loss. Although losing ZCS, the MRSCC expe-riences similar switching loss as a RSCC as determined by C_{oss} charging and discharging loss. By achieving high immunity tolerance towards component variation, the MRSCC allows utiliza-tion of a class II capacitor, such as an X7R capacitor, in order to reduce cost.

Similar to a RSCC, the MRSCC is expandable to higher VCR topology, such as Dickson star topology. As a result of having two resonant tanks, a STC must always have two exact resonant tanks. But due to operating a non-ZCS mechanism, the MRSCC need not have the exact same resonant tanks. In conclusion, due to immunity towards variation, the MRSCC reduces production cost by using class II capacitors and a simple control mechanism (no zero current detection).

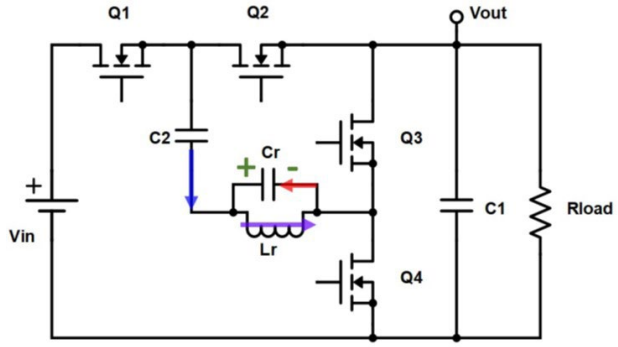


Fig. 1. 2 to 1 Multi-resonant switched-capacitor converter.

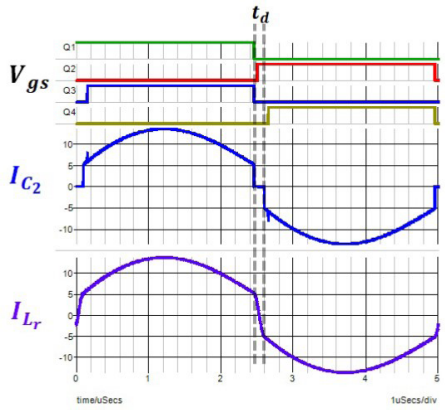


Fig. 2. MRSCC operational waveform.

Improved V² Constant On-Time Control with State-Trajectory Control

Voltage regulator (VR) for smartphone CPU application needs to meet fast dynamic voltage scaling (DVS) and load transient requirements. Constant On-Time (COT) control is a popular variable-frequency control due to high light-load efficiency and high-bandwidth design to achieve fast transient. In addition, the V^2 variation of COT is able to achieve fast DVS tracking due to direct output voltage (V_o) feedback.

Under fast load-transient conditions, it is possible for COT to lose control for a period of time. As a result, V_o not only has a large undershoot but also a ringback before control is regained. To analyze the converter behavior when control is lost, the state-plane trajectory of the buck converter is used. The trajectory of the buck converter for a given operating stage, on or off, is represented as a circle in the normalized state-plane, as shown in Fig. 1. Initial condition and circle center information are necessary to determine the state-plane trajectory.

When a load step-up transient occurs, the trajectory center moves due to the change in load current (I_o). To achieve the fastest transient possible, which is a single-cycle response, the converter should be operating in the on-stage during transient until an optimal switching point is reached. By switching from the on-stage to the off-stage at the optimal switching point, the off-stage trajectory brings the system to the new steady-state in one switching cycle. Using the state-plane trajectory, the optimal switching point (t_E) is determined as the intersection point of two circles, as shown in Fig. 2. In order to calculate the intersection of the two circles, I_o and circle radii need to be determined. This work presents a method to estimate the optimal switching point as an inductor current (i_L) limiting function using reference voltage (V_{ref}) and i_L.

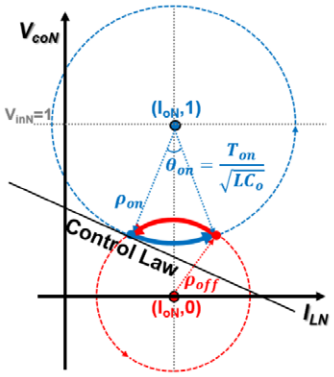


Fig. 1. State-plane trajectory paths of the on-stage (blue) and the off-stage (red) of the buck converter in the normalized state-plane.

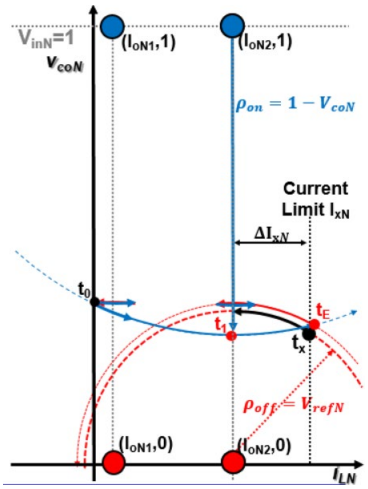


Fig. 2. Proposed state-plane trajectory control to achieve the fastest load step-up transient response.

Simplified Optimal Trajectory Control for 1 MHz LLC Converter with Wide Input Voltage Range

The LLC resonant converter has been trending as a high-efficiency dc-dc converter. LLC features soft switching for primary and secondary devices and can operate at high switching frequency with high efficiency and power density. In some applications, like bus converters, the dc-dc converter is required to provide regulation over the range of input voltage, typically 40 V:60 V for datacenter applications and 35 V:75 V for telecom use. LLC converters can provide regulation using frequency modulation, but controlling an LLC with fast transient re-sponse is challenging. Simplified Optimal Trajectory Control (SOTC) can achieve very fast load transient response by simple measurement of output voltage and load current signals. However, SOTC assumes operating at $f_s=f_o$ where the LLC converter runs at resonant frequency for all loading conditions.

This work presents a digital implementation of SOTC for a 1 MHz LLC with a low-cost low-speed 90 MHz MCU. Here, we propose the implementation of a two-step SOTC for fast tran-sient response. The delay between transient instant and settling point in the proposed implementation is reduced to only 6 cycles, hence a faster transient response can be achieved. Moreover, since the calculation time is reduced, the maximum switching frequency can be pushed from 1.6 MHz to 2 MHz and wider gain ranges can be obtained.

This work also discusses the challenges of controlling LLC converters operating at wide gain and frequency range. The SOTC control scheme assumes the operation at resonant frequency and unity gain. However, when the switching frequency drifts far from the resonant frequency, the transient performance is highly degraded. A feedforward compensation is proposed in conjunction with the SOTC control as shown in Fig. 1 to obtain fast transient performance over the whole frequency range.

Furthermore, trajectory control is used for soft startup of the LLC with limited current stress. The LLC starts with a fixed switching frequency profile where the switching frequency is calculated as a function in output voltage to a soft start-up under predetermined current band limit (+/-I_{LMAX}). However, with fixed switching frequency profiles, a higher input voltage than nominal value causes extra current stress that could damage the converter, and a lower input voltage leads to insufficient energy transfer to the output capacitor for start-up. For an LLC operating at wide input voltage range, the switching frequency at start-up is adapted with V_{in} to make sure the same current stress is applied, and guarantee successful start-up at all input voltage ranges.

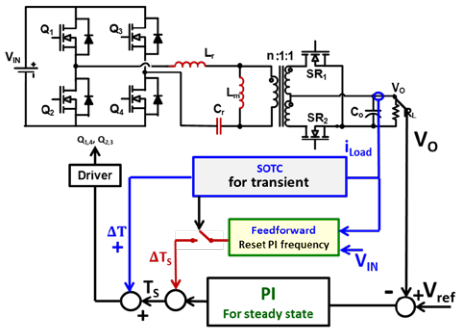


Fig. 1. Block diagram of a simplified trajectory control with a feedforward compensator for an LLC operating at a wide switching frequency range.

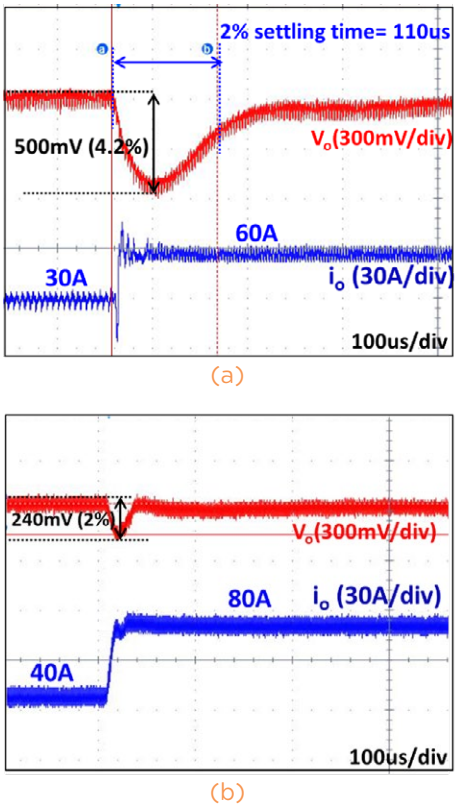


Fig. 2. 50% to 100% load transient response at 48 V (a) 130 kHz commercial 800 W full-bridge phase-shift converter, and (b) proposed 1 MHz -1 kW LLC resonant converter using SOTC control.

Magnetic Integration of 3 kW LLC Converter for Front-end Power Supply in 48 V Power Architecture

Power consumption of datacenters has been increasing rapidly. Recently, 48 V power architecture has attracted more interest for datacenters, as it offers a more efficient power architecture and fits in the telecom ecosystem. This paper focuses on the implementation of the dc-dc stage of a 3 kW power supply unit. Single phase LLC topology (Fig. 1) is chosen, as it can achieve soft-switching; giving us the opportunity to push the switching frequency and increase the power density. This paper focuses on the magnetic integration of the transformer and resonant inductor of the LLC converter.

The paper discusses the design and magnetic integration of matrix transformer. Three candidates of matrix transformer have been discussed and evaluated as shown in Fig. 2. A PCB matrix transformer of four elemental transformers is selected to handle the high power efficiently while keeping high power density. The matrix transformer is integrated in one core along with resonant inductor. The paper also addresses the transformer winding layout to reduce leakage flux and current crowding in the windings. The secondary winding layout is modified to reduce current crowding in transformer. Careful layout of primary side vias is also discussed to obtain good current shaing between vias, and reduce the current crowding around vias.

For the 48 V power architcture, the dc-dc stage controls the output voltage within a range of 40 V to 60 V. A high resonant inductance value needs to be implemented to gain voltage gain controllability. A resonant inductor is integrated with the transformer strucure in one core to achieve compact design.

Optimization of the transformer core loss and winding loss is also discussed to minimize total loss while achieving high power density. The proposed converter has estimated efficiency high than 98.8 percent with power density higher than 400 W/in^3.

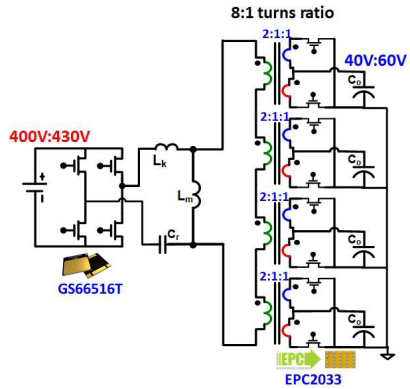


Fig. 1. Single-phase LLC with matrix transformer for 3 kW 48 V power architecture.

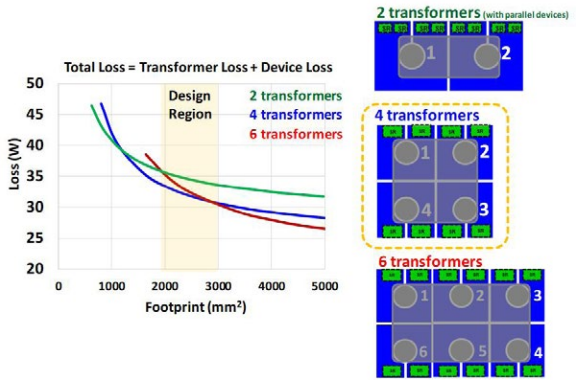


Fig. 2. Transformer loss vs. transformer footprint for three candidates of matrix transformer.

Digital Implementation of Light-Load Efficiency Improvement for High-Frequency LLC Converters With Simplified Optimal Trajectory Control

The light load efficiency of an LLC converter with frequency control cannot meet the increasing efficiency requirements, such as 80 Plus and Energy Star. In recent years, a high frequency LLC converter has emerged, due to its high power density and integrated magnetics, which reduce the total cost. Digital controllers, especially cost-effective microcontrollers (MCUs), are gradually replacing analog controllers for controlling the LLC resonant converter. Hence, it is desirable to extend burst mode to the high frequency LLC converter with a low-cost microcontroller (MCU).

Due to the dynamics of the resonant tank, a conventional burst control for an LLC converter has a problem; the resonant tank cannot keep to the efficiency-optimal state trajectory. The optimal trajectory control (OTC) for burst mode with a fixed 3-pulse pattern can solve this problem, based on state-plane analysis. However, when the OTC for burst mode is applied to a high frequency LLC converter with an MCU, the burst mode operation range is limited. This is because in burst off-time, the digital controller must leave enough time to blank sensing noise, sample, and update the control signal. With minimum off-time T_{off_min}, the maximum average power delivered to the secondary side is limited, as shown in Fig. 1(a).

To extend the burst operation range for a high frequency LLC converter, a simplified optimal trajectory control (SOTC) for burst mode, with adaptive burst on-power and adaptive multi-step, are proposed in this paper. The first step in the process is to increase the burst on-power, but the desired trajectory is not fixed to the efficiency-optimal trajectory. The next step is to increase the burst pulses, as shown in Fig. 1(b). The principles are as follows: Assuming the load increases from an empty load, initially a 3-pulse pattern is applied. When the load increases to the limit of the 3-pulse pattern, then a 5-pulse pattern is applied.

The SOTC for burst mode with an adaptive multi-step is verified on a 500 kHz LLC converter controlled by a 60 MHz MCU. The efficiency curve is shown in Fig. 2. The light efficiency improvement is significant, compared with conventional burst mode.

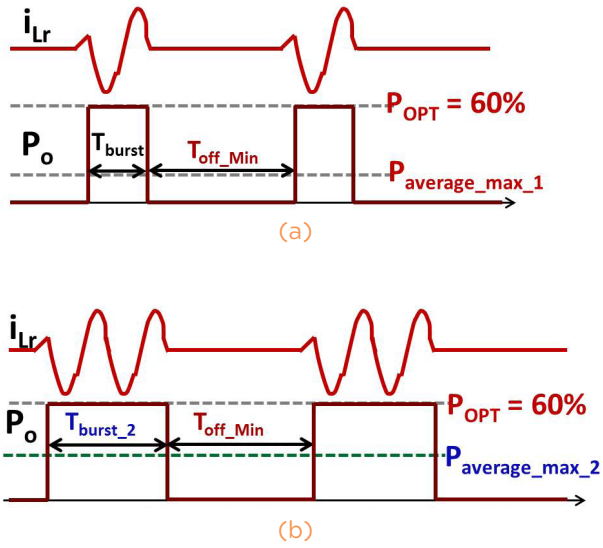


Fig. 1. (a) OTC for burst mode with fixed 3-pulse pattern and (b) proposed SOTC for burst mode with multi-step.

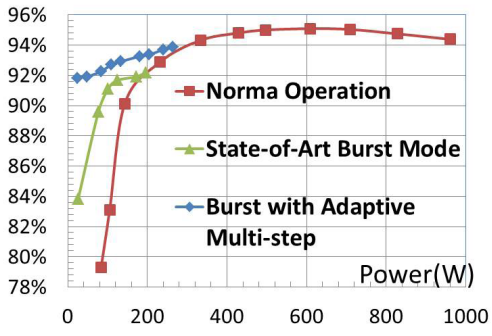


Fig. 2. Efficiency of proposed burst mode for high frequency LLC converter.

Digital Implementation of Adaptive Synchronous Rectifier Driving Scheme for High-Frequency LLC Converters with Microcontroller

To improve the overall efficiency of an LLC resonant converter, synchronous rectifiers (SRs) should be employed. The SR gate driving signals are important to the efficiency of LLC resonant converters, due to the discrepancy between the driving of primary switches and the driving of secondary switches. Digital controllers have superior advantages over analog controllers. Among digital controllers, cost-effective microcontrollers (MCUs) are preferred in industrial applications. Also, it is important to implement adaptive SR driving by the MCU, instead of using additional SR control chips.

The drain to source voltage of the SR is sensed and compared with the threshold voltage to detect the paralleled body diode conduction. For a conventional LLC converter, the SR turn-ON time is synchronized with the primary side switches. The SR turn-OFF time is tuned to eliminate the body diode conduction, based on the output of the comparator, which is connected to the external interrupt of the MCU. This is shown in Fig. 1.

For a high frequency LLC converter, if the SR turn-OFF time is tuned every switching cycle, the CPU of the MCU will be occupied most of the time. To release the burden off of the MCU, the output of the comparator is connected to a ripple counter, instead of the external interrupt of the MCU. This is shown in Fig. 2. The SR turn-ON time is still synchronized with the primary side switches, but the SR turn-OFF time is tuned based on the status of the counter output. The counter is cleared every 3rd switching cycle for a 500 kHz LLC converter.

The adaptive SR driving for a conventional LLC converter is verified on a 130 kHz LLC converter with a TMS320F2808 MCU. The adaptive SR driving for a high frequency LLC converter is verified on a 500 kHz LLC converter with a TMS320F28027 MCU. Desired performance is achieved in both cases.

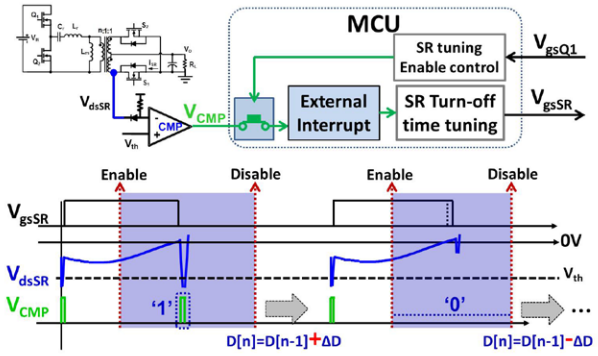


Fig. 1. MCU based implementation of adaptive SR driving for conventional LLC converter.

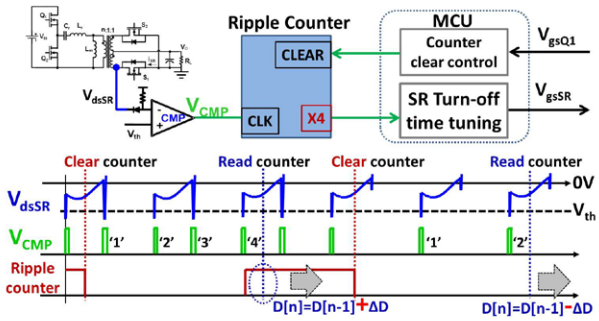


Fig. 2. MCU-based implementation of adaptive SR driving for high frequency LLC converter.

Single-Stage EMI Filter for Server Power Supply

Electromagnetic interference (EMI) filters are required in switching power converters to attenuate conductive noise. With low frequency noise, the current path is easier to identify and therefore easier to block. However, with high frequency noise, the current path will flow through parasitics, such as equivalent parallel capacitance (EPC) of inductors and equivalent series inductance (ESL) of capacitors. Therefore, the current path is hard to identify. Also, the near-field coupling between the inductor and capacitor (M1, M2 coupling), and the coupling between the capacitors (M3 coupling), will induce another mutual inductor in the capacitor branch and deteriorate the high frequency performance of the filter. Accordingly, the general practice in conventional server power supply is the two-stage or multi-stage EMI filter, with one of the stages intentionally designed to attenuate the high frequency noise. However, with more stages added to the EMI filter, the size and cost are increased and the power density is reduced.

Several approaches for self-parasitics and mutual-parasitics cancellation have been proposed, but not demonstrated in converters. The reason is that the near-field effect has submerged in the strong magnetic field of inductors in conventional two-stage or multi-stage EMI filters. Therefore, a single-stage filter is desired in order to have better self- and mutual-parasitics cancellation.

In this nugget, PCB winding magnetics, balance and shielding technique demonstrate good performance for common mode (CM) noise reduction. At the same time, phase interleaving for power factor correction (PFC) rectifier reduces differential mode (DM) noise. As a result, a single-stage EMI filter will easily meet the low-frequency EMI noise standard limit.

To improve the high frequency performance for the single stage EMI filter, High Frequency Structure Simulator software from ANSYS Inc. is used to analyze the flux distribution for the DM inductor from low frequency to high frequency. Then flux distribution is further verified by near field measurement with near field probe. By drawing the flux distribution, the change of the flux pattern from low frequency to high frequency is observed, and this provides useful information for adjusting the positions of the inductor and capacitors to reduce M1 and M2 coupling. Next, the X-cap is built up to reduce the ESL of the capacitor branch. Finally, a flux cancellation loop is introduced to reduce the M3 coupling. A single-stage EMI filter is demonstrated based on a 1 kW server power supply. The proposed single-stage filter demonstrates better high frequency performance compared to a conventional single-stage EMI filter.

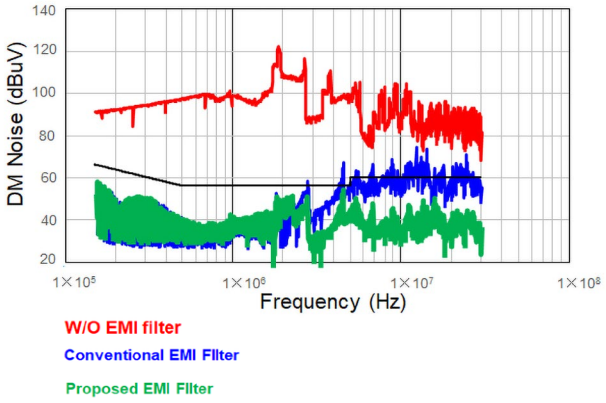


Fig. 1. DM noise testing result under different conditions.

High-Efficiency High-Power-Density 3 kW LLC Converter with Integrated PCB Winding Matrix Transformer

The 3 kW, 48 V output voltage power supply is promoted to replace the 12 V power supply for mitigating heavy bus bar loss and reducing energy conversion stages. The conventional Si-based 48 V front-end converter has fixed dc-link voltage, thus the output voltage is regulated with an LLC dc-dc (D2D) converter by modulating the switching frequency. With the output voltage varied in 40-60 V, the switching frequency range of the LLC D2D converter is wide, from 0.7 fr to >3.0 fr. Therefore, the switching loss is increased especially in light load, and the efficiency of the LLC D2D converter is comparatively low.

In order to increase the efficiency of the LLC converter, a variable dc-link voltage solution is proposed. By running the LLC converter as a dc transformer (DCX), the LLC converter can always work at resonant frequency to achieve high efficiency. Accordingly, the output voltage is actually regulated by a power factor converter (PFC). With SiC and GaN devices in the primary and secondary side respectively, the switching frequency of the LLC DCX converter is pushed to 500 kHz.

The main challenge for high power density and high efficiency is the transformer winding and core design. The total transformer ratio for the LLC converter is 12:1. With four elemental transformers, the turns ratio for each elemental transformer is 3:1. A four-layer printed circuit board (PCB) winding structure, with two layers for secondary side winding and another two layers for primary side winding, is the general practice in PCB winding matrix transformer design. In the case with an even number of turns on the primary side, half of the turns are arranged in each layer. However, with an odd number of turns on the primary side, it is physically impossible to accomplish half of one turn.

This work proposes a novel winding structure that allows an odd number of turns for the primary side winding. The proposed structure has a simple winding structure and low winding loss. Four elemental transformers are integrated into a single planar magnetic core by flux cancellation. The winding width and core radius are optimized to achieve lower winding loss and a smaller footprint. Moreover, shielding technique is applied by simply inserting two layers into the PCB winding to reduce the common mode electromagnetic interference noise.

A 3 kW PCB winding matrix transformer is demonstrated based on a 500 kHz LLC resonant converter with wide-bandgap device. A turns ratio of 3:1 is achieved in each elemental transformer. The prototype achieves a peak efficiency of almost 98.5 percent and a power density of 400 W/in^3.

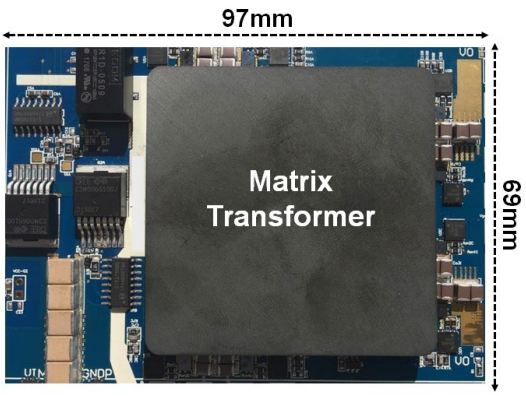


Fig. 1. The 500 kHz 3 kW LLC converter prototype with integrated PCB winding matrix transformer.

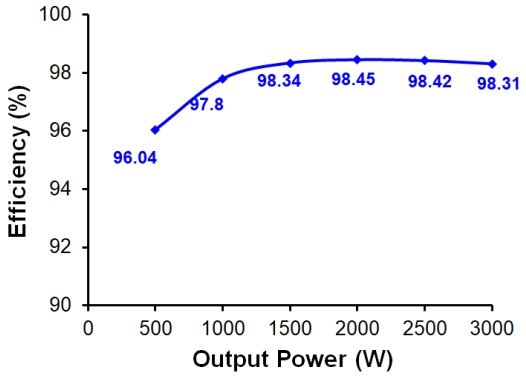


Fig. 2. The tested efficiency versus output power for the 3 kW LLC converter.

Shielding Technique for Planar Matrix Transformers to Suppress Common-Mode EMI Noise and Improve Efficiency

For high output current LLC converters, the planar matrix transformers with PCB windings are advantageous over the conventional transformer designs because of their high efficiency and high power density. However, they suffer from a large interwinding capacitance of the PCB windings, which causes a large common-mode (CM) noise. This is more severe when a gallium nitride (GaN) device is applied because it has a higher dv/dt than its silicon (Si) coun-terpart. To predict the CM noise spectrum for the matrix transformers, a model for the inter-winding capacitance was developed. Shielding is an effective method to attenuate the CM noise in all frequency spectrums of interest, and it is more suitable for PCB windings since it can automatically be embedded in the fabrication process. However, shielding will cause extra losses and decrease efficiency.

In this paper, a novel shielding structure is proposed, which utilizes half of the shielding as the primary winding while still maintaining the benefit of the CM noise attenuation. The shielding layer is identical to the secondary windings. It was proven in this paper that the proposed shielding layer can be rotated to simplify the PCB traces for connection and minimize interference between the primary traces and the output terminals. The proposed shielding was verified by experiments on 1-MHz, 800-W, 400 V/12 V LLC converters. The proposed shielding can attenuate the CM noise by around 30 dB and is effective in the whole frequency range. It improves the full-load efficiency from 97.2 percent to 97.4 percent and improves the peak efficiency from 97.6 percent to 97.7 percent.

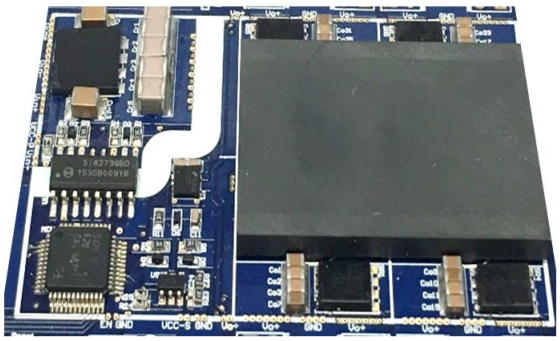


Fig. 1. A 1 MHz 800 W 400 V/12 V LLC converter prototype with proposed shielding.

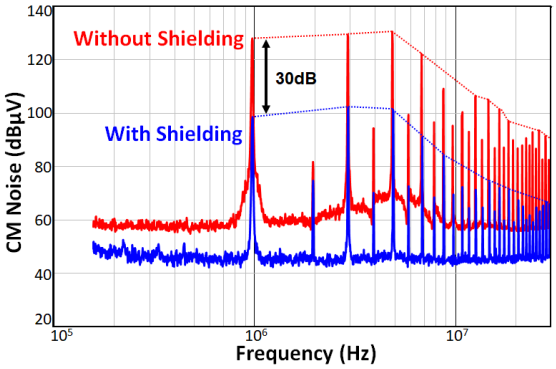


Fig. 2. Comparison of measured CM noise spectrums for the designs without and with proposed shielding.

Improved Magnetic Design for 12.5 kW CLLC Resonant DC/DC On-Board Charger

High-power and high-density battery charging converters have gained popularity in recent years thanks to the advantages of reduced size and improved efficiency. The three-phase dc-dc converter has the added benefit of reduced current stress on switching devices. Few applications, however, take advantage of integrating magnetics components. Implementing wide-bandgap devices provides the opportunity for increased switching frequency. The higher frequency makes printed circuit board (PCB) transformers a possibility.

In this work, an improved magnetic design is introduced for the 12.5 kW conventional LLC resonant converter. The improved magnetic structure has lower loss for both the transformer winding and the soft ferret core. Shielding technique is implemented to enhance common mode (CM) noise rejection performance and additional design considerations are given to thermal management of the transformer structure for improved reliability. By improving the magnetic structure, the PCB-based transformer can reach a higher power capacity without additional thermal constraints, enabling the converter to achieve a higher power level and higher power density.

The three-phase bidirectional dc-dc converter, shown in Fig. 2, is designed to operate with a 550-800 V variable dc bus. The bidirectional operation of the converter is achieved with the help of a resonant component on both the primary and secondary side of the converter. With magnetics integration, the converter is able to operate with six core legs. The primary and secondary side mirrors ensure identical gain characteristics for both forward and reverse operation.

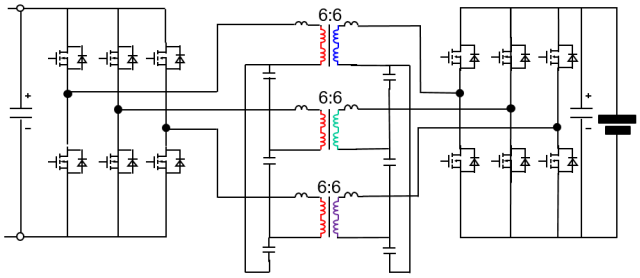


Fig. 1. Three-phase bidirectional converter.

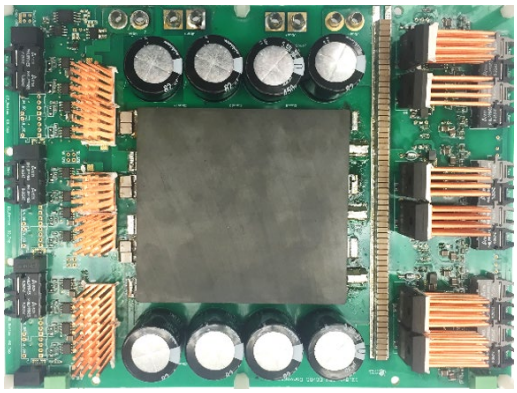


Fig. 2. Hardware prototype for 12.5 kW bi-directional CLLC converter.

A Wide Bandgap-Based Three-Phase 12.5 kW 500 kHz CLLC Resonant Converter with Integrated PCB Winding Transformer

The three phase dc-dc resonant converter offers an attractive solution to high-power applications due to the reduction in component stresses, when compared to a single-phase resonant converter of the same power rating. A three-phase CLLC bidirectional resonant converter is adopted for a 12.5 kW off-board charge, as shown in Fig. 1. The Δ-connection on the primary side is used to take advantage of the good current sharing and fast start up. In addition, wide-band-gap devices, including both silicon carbide (SiC) and gallium nitride (GaN) devices, are adopted to push the switching frequency to over 500 kHz. With the help of high switching frequency, a six-layer PCB winding transformer is proposed. Not only are all the resonant inductors integrated into the transformer, but also the three phase transformer is integrated to further reduce the size. As a result, only one magnetic component is needed for the whole three phase CLLC resonant converter.

By redistributing the primary and secondary windings on the outer posts and adding an additional center post, the leakage inductance of the transformer can be increased, and serve as primary and secondary side resonant inductors. Compared with other integration methods, the interleaved winding structure is maintained, and thus smaller ac winding loss is achieved. Also, with the additional center post serving as the leakage flux path, the leakage inductance (resonant inductors) can be controlled by adjusting the center post air gap length. In addition, all the leakage flux is confined in the center post, having no impact on surrounding components. If we investigate the flux in the core, due to the 120° phase shift between each phase, the flux in the three center posts also have a 120° phase shift. As a result, the total flux in the center posts is cancelled out. This can be verified through 3D finite element analysis (FEA) simulation. One can see that the flux in the three center posts is almost zero; therefore, the transformer structure can be simplified by removing the three center posts.

Using the designed three-phase integrated transformer, a 12.5 kW hardware prototype with 500 kHz switching frequency is developed, as shown in Fig. 2. The resulted power density including the heatsink is 155 W/in^3. The power density is much higher than the single-phase version due to the three phase transformer integration. The efficiency of the three phase CLLC resonant converter is also tested, and the peak efficiency of 97.3 percent is achieved.

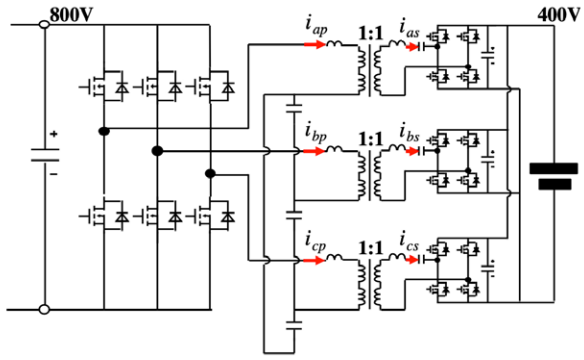


Fig. 1. Proposed three-phase CLLC resonant converter.

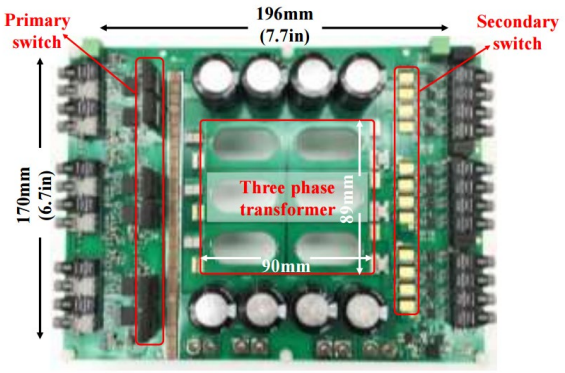


Fig. 2. 12.5 kW 500 kHz three-phase CLLC resonant converter with integrated magnetics.

20 MHz, Three-Via 2 Phase Inverse Coupled Inductor Design for Integrated Voltage Regulator for Smartphone Applications

For the magnetic integration in integrated voltage regulator (IVR), the on-chip inductor for wafer level integration and the package-embedded integration are two mainstreams. The on-chip inductor achieves ultra-high inductance density and small inductor size with a multi-turn structure. However, large dc resistance (DCR) limits current handling ability to <1 A load current per phase. In mobile applications, the peak current demand for system-on-chip (SoC) load is 20 A or more. Increasing the phase number to supply enough power increases cost and control complexity. To solve this issue, package-embedded inductor integration with a larger current handling ability is selected.

At the same time, in order to support dynamic voltage and frequency scaling (DVFS) and further shorten the power delivery path, a three-dimensional integration structure is proposed by CPES and shown in Fig.1, where an inductor is put underneath the processors rather than on the motherboard. To realize this, a unique inductor structure with a small footprint and low profile is required. In this paper, a unique, 20 MHz three-via two-phase inverse coupled inductor structure is proposed, as shown in Fig. 2. This special structure combines the benefits of multi-via with boosted inductance density and inverse coupling with dc flux cancellation effect. First, different high frequency magnetic materials are compared with our high frequency magnetic material characterization method. Metal-flake composite manufactured by TOKIN Corp.is selected for its high permeability and low loss property. Then, the impact of the design parameters of this structure is carefully examined and the whole inductor design flow is proposed for optimization with the help of ANSYS Maxwell simulation software. Finally, the inductance and coupling are measured by hardware to verify the accuracy of the simulation models. The final results show the total loss of inductor is as small as 100 mW at 3 A load current with a 2 mm^2 footprint and 0.5 mm height per phase. Compared with our previous single-via five-phase inductor design, this new three-via two-phase inverse coupled inductor achieves a 50 percent loss reduction and 30 percent size reduction. The comparison results with state-of-art inductor designs for IVR for mobile applications also indicates this new structure is promising due to larger current handling capability and smaller size.

To develop a 20-50 MHz IVR, for smartphone applications, this paper proposes a 20MHz, three-via two-phase inverse coupled inductor structure. The design flow is developed for optimization and experiments verify the accuracy of the simulation model. Compared with state-of-art inductor design for mobile applications, this new structure has larger current handling capability, a smaller footprint, and low loss and profile.

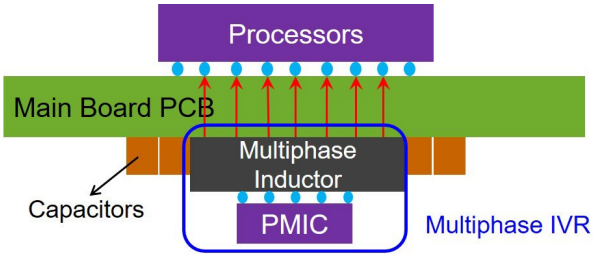


Fig. 1. Three-dimensional magnetic integration for mobile application.

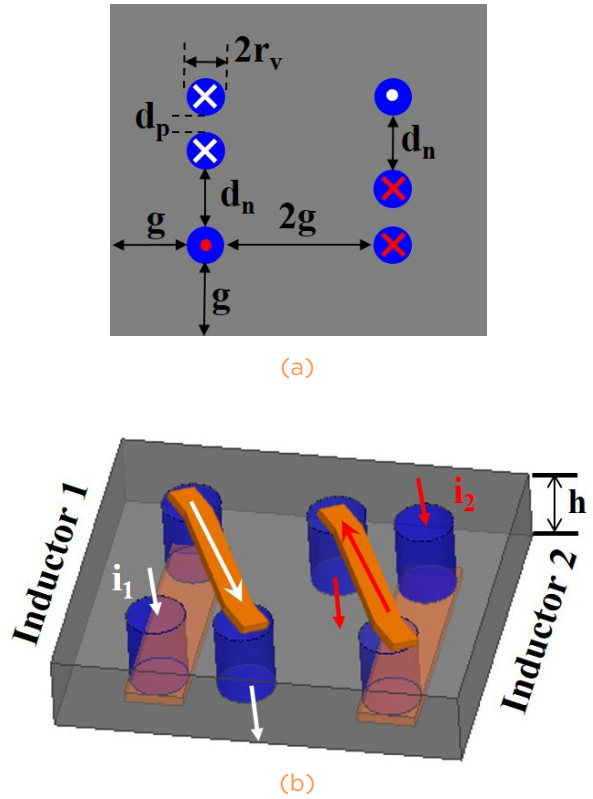


Fig. 2. (a) 2D view of three-via 2 phase inverse coupled inductor structure and (b) 3D view.

Improved Partial Cancellation Method for High-Frequency Core Loss Measurement

Accurate high-frequency core loss measurement is critical for power converter design, especially for integrated voltage regulator application. Partial cancellation method is a promising candidate, which is designed to cancel out loss error caused by phase discrepancy without finely tuning cancellation component values. Fig. 1 shows the equivalent circuit of Hou's inductive partial cancellation method. The voltage of the core sample, the voltage of air core transformer, and the current flowing through the core sample are measured. The basic idea of this method is utilizing the loss error in measured air core transformer loss to cancel out loss error in measured core loss. However, it assumes a small value of phase discrepancy caused by probe delay between voltage probe and current probe, which is not valid for high frequency. A detailed error analysis under this case shows the probe delay between voltage probe and current probe must be limited within a range to obtain the accuracy.

An initial compensation method by using a simple circuit with a high Q capacitor is proposed to solve this problem. Fig. 2 shows the circuit for initial compensation. By measuring capacitor voltage and its current under sinusoidal excitation, the high Q capacitor loss is ob-tained by integrating the product of its voltage and current in a cycle. By extracting the equivalent series resistance (ESR) loss, the probe delay between voltage probe and current probe is calculated out from the rest of the measured loss. It shows the probe delay changes with frequencies and a little difference will induce measurement error for higher frequencies (>20 MHz). Therefore, it is necessary to initially compensate the probe delay before using partial cancellation method. Finally, experimental results verify the proposed method. The core loss of metal flake composite manufactured by TOKIN Corp. is measured three times at 60 MHz with sinusoidal frequencies. The results with initial compensation are constant and stable compared with results using delay values from the probe datasheet.

As a promising method for high frequency core loss measurement, partial cancellation method assumes phase discrepancy as a small value, which is not valid for high frequency. This paper first performs the error analysis under high frequency test conditions. The result shows large phase discrepancy will introduce non-negligible error and phase discrepancy needs to be controlled in a small range to limit measured loss error. An initial compensation method is proposed to effectively control phase discrepancy in a small range by using a high Q capacitor. Finally, experiments verify the measurement accuracy of the improved partial cancellation method.

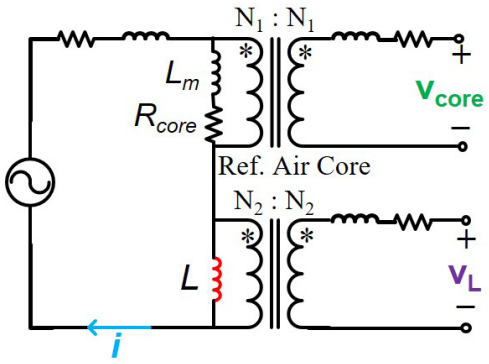


Fig. 1. The equivalent circuit of inductive partial cancellation method.

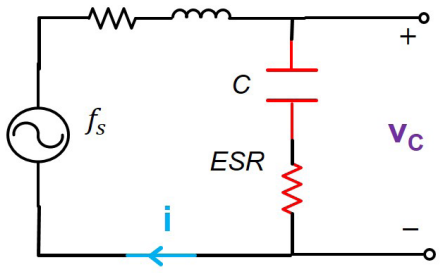


Fig. 2. Initial compensation circuit with high Q capacitor.

High Density Integration (HDI) Consortium Nuggets

A Wire-Bond-Less 10 kV SiC MOSFET Power Module with Reduced Common-mode Noise and Electric Field

Effect of Surface Roughening of Temperature-cycled Ceramic-metal-bonded Substrates on Thermomechanical Reliability of Sintered-silver Joints

A Novel ZVS Turn-on Triangular Current Mode Control with Phase Synchronization for Three Level Inverters

Trends in SiC MOSFET Parameters from Accelerated Lifetime Tests

Optimized Coil Design for EV Charging with Medium Voltage Input

Hierarchical Weight Optimization Design of Aircraft Power Electronics Systems Using Metaheuristic Optimization Methods

Hetero-Magnetic Swinging Inductor (HMSI) and Its Application for Power Factor Correction Converters

A Wire-Bond-Less 10 kV SiC MOSFET Power Module with Reduced Common-mode Noise and Electric Field

A 10 kV silicon carbide (SiC) MOSFET can switch higher voltages faster and with lower losses than silicon devices while also being smaller in size. However, these features can result in premature dielectric breakdown, higher voltage overshoots, high-frequency current and voltage oscillations, and greater electromagnetic interference. To mitigate these side effects, and fully utilize the benefits of these unique devices, advanced module packaging is needed. This work proposes a power module package with a small footprint (68 mm × 83 mm), low gate- and power-loop inductances (4 nH), increased partial discharge inception voltage (53 percent), and reduced common-mode (CM) current (10 times).

The module uses molybdenum posts and direct bonded aluminum (DBA) substrate for the interconnections instead of wire bonds. This 3D structure reduces the parasitic inductances and capacitances, and allows decoupling capacitors to be integrated inside the module without increasing the footprint.

To reduce the electric field strength at the ceramic-metal-encapsulant interface (i.e., the triple point) and the CM current generated by the fast voltage transients (up to 200 V/ns), it is proposed to stack two DBA substrates, and connect the middle metal to half of the dc bus (the midpoint of the series embedded decoupling capacitors in this case). With this connection, the partial discharge inception voltage (PDIV) is increased by 53 percent.

This connection also forms a screen that contains the CM current within the power module. Fig. 1a and Fig. 1b show the schematics of the module double-pulse test without and with the middle metal layer of the substrate stack connected to the capacitor midpoint, respectively. C_{P1} and C_{P2} are the parasitic capacitances across the two DBA substrates. Fig. 2 shows the resulting experimental waveforms. The current flowing through the ground path (shown in Fig. 1) is reduced by ten times when the proposed screen is connected. This method is thus effective at both increasing the PDIV and reducing the CM current and does not add significant size or complexity to the power module. The lower CM noise can reduce the external filtering requirements and enable WBG devices to switch at faster switching speeds, thus reducing size, weight, cost, and losses at the system-level.

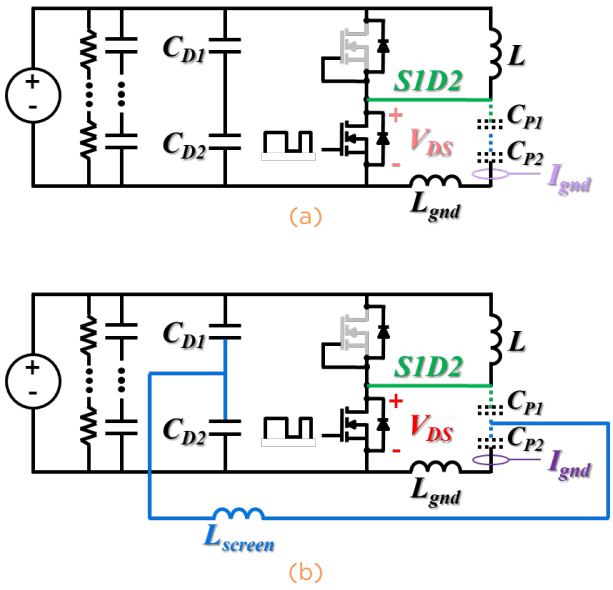


Fig. 1. Schematic of the testing setup (a) without and (b) with the CM screen connected.

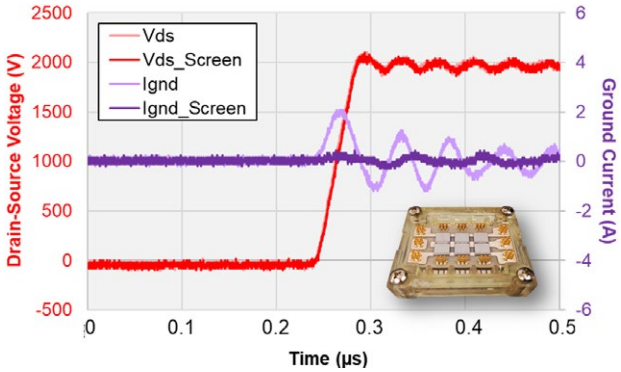
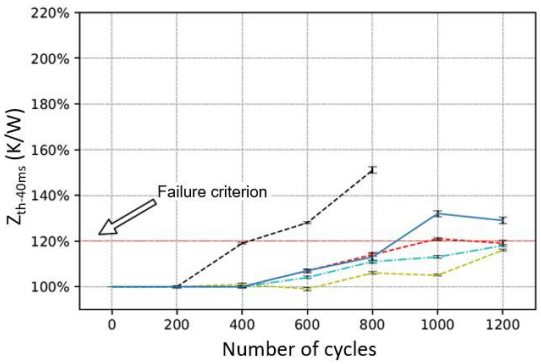


Fig. 2. Drain-source (red, left axis) and ground current (purple, right axis) waveforms with and without the CM screen.

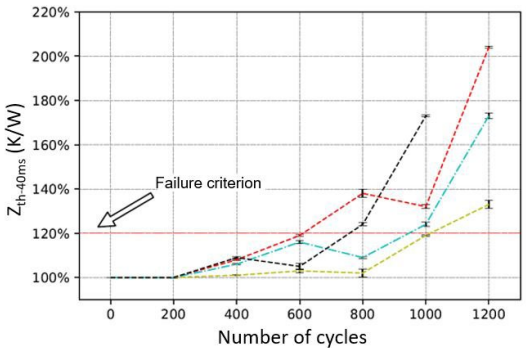
Effect of Surface Roughening of Temperature-cycled Ceramic-metal-bonded Substrates on Thermomechanical Reliability of Sintered-silver Joints

Higher power density and reliability demands on power electronics systems are driving the need for the development of high-temperature packaging solutions. Existing power module packaging technologies, that rely on lead-tin or lead-free die-attach solders and alumina direct-bond-copper (DBC) insulated substrates, are limited to 125°C junction temperature for reliable module operation. Recently, die-attach by silver sintering or the low-temperature joining technique (LTJT), has been shown to significantly improve chip-bonding reliability at higher junction temperatures. Also, direct-bond-aluminum (DBA) substrates with aluminum nitride (AlN) ceramic, and AMB substrates using high-toughness silicon nitride (Si_3N_4) ceramic, are shown to be significantly more reliable than alumina DBC substrates, especially over large temperature swings. However, it is reported that the surface roughness on both substrates grew with the number of temperature cycles. The roughening rate on the DBA substrate was two times faster than that on the AMB substrate. This may cause reliability issues. To evaluate the effect of surface roughening on the sintered-silver joint reliability, the transient thermal impedance of the bonded power chips was measured. As shown in Fig. 1, despite the higher roughening rate, the sintered-silver bond on the DBA substrate had a longer lifetime than that on the AMB substrate.

Fig. 2 is the cross-sectional scanning electron microscopy view. It shows the formation of vertical cracks in the sintered bond-line on the DBA substrate, as opposed to horizontal cracks on the AMB substrate. Formation of the vertical cracks in the bond-line relieved stresses without significantly impacting the thermal performance.

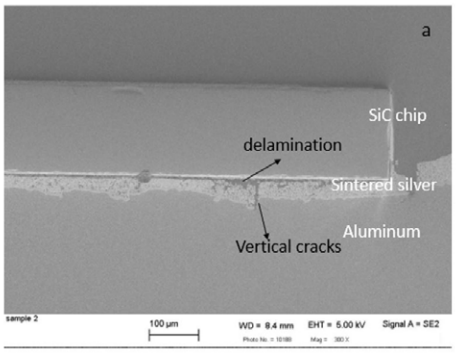


(a)

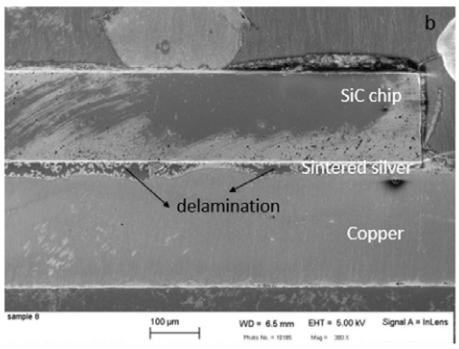


(b)

Fig. 1. Percentage change of thermal impedance for AlN DBA samples (a) and AMB Si_3N_4-copper samples (b) under the temperature (-55° C to 250° C) cycling.



(a)



(b)

Fig. 2. SEM cross-sectional images of bonded MOSFETs on the two different types of substrates after 1200 temperature cycles: (a) on AlN-DBA; and (b) on AMB Si_3N_4.

A Novel ZVS Turn-on Triangular Current Mode Control with Phase Synchronization for Three Level Inverters

The drive for higher power densities is pushing power converters to high switching frequencies due to their significantly smaller filters that account for the bulk of the volume in power converter systems. Critical conduction mode (CRM)/ Triangular current mode (TCM) control with ZVS turn-on for single phase converters has led to improved efficiency at high switching frequencies (>300 kHz). In addition, recent advancements in wide bandgap device technology, it is possible to operate at high switching frequencies with very low turn-off losses. However, turn-on losses in hard switching continuous conduction mode (CCM) are still significant, thus making it necessary to operate the inverter with zero voltage switching (ZVS) turn-on. A simple way of achieving soft switching in a three phase inverter is by connecting the dc bus midpoint to ac neutral, thus operating it as three single phase inverters in parallel.

However, this configuration results in phase desynchronization and very high switching frequency variation. Switching frequency variation is minimized in TCM for a two-level converter by clamping one of the phases. This work shows how to extend this method to three level inverters. Three-level converters offer several advantages over two-level converters, such as reduced common mode voltage (CMV). The same benefit is extracted in proposed 3-level TCM by making use of reduced CMV switching states. Two switching schemes are thus proposed that are applicable for any 3-level inverter topology. A 3-level NPC inverter is also considered. The modulation presented is compared with sinusoidal pulse width modulation (SPWM), it has lower losses as well as lower CMV. It is also shown that a huge reduction in inductor size is achieved by high switching frequency operation.

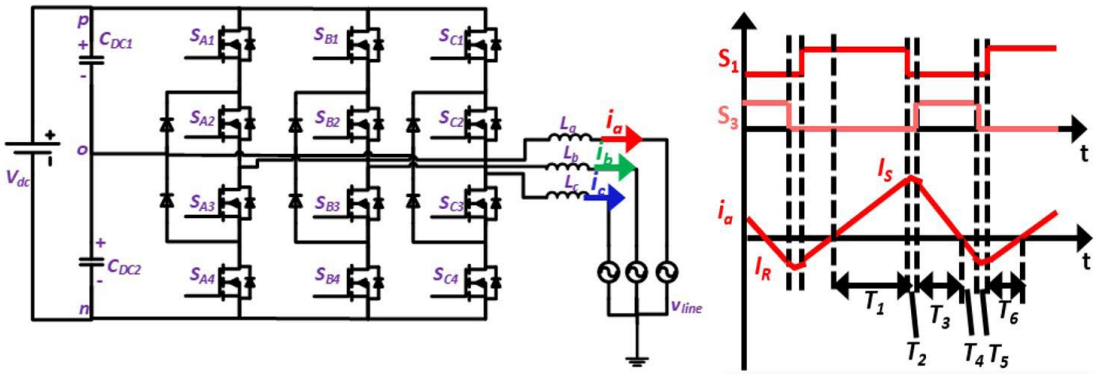


Fig. 1. 3-Level NPC Inverter with basic principle of ZVS turn-on with TCM when AC mid-point is connected to neutral.

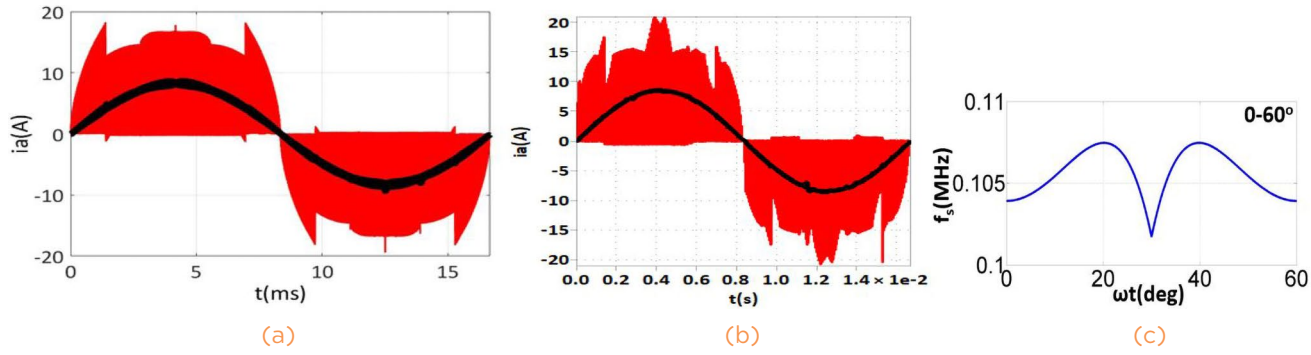


Fig. 2. Phase A current for a 5 kW, 900 V_{dc}, 480 V V_{acl-l}, L= 18 μH for (a) Scheme I and (b) Scheme II. (c) Switching frequency variation for both the schemes.

Trends in SiC MOSFET Parameters from Accelerated Lifetime Tests

Integrating SiC power MOSFETs is very attractive for advancing power electronic systems, yet system reliability remains in question. This work presents a newer accelerated lifetime test (ALT) that further investigates the packaging and semiconductor failures of a TO-247 SiC MOSFET. This ALT, entitled Switching Cycling, utilizes the transient turn-on and turn-off of a device to stress the semiconductor under high drain-source voltage (V_{DS}), and high pulsed drain-source current (I_{DS}). The device is pulsed on to reach the desired stress current. The short pulse time minimizes conduction losses, therefore minimizing self-heating effects. The clamped inductive circuit and initial VDS and IDS pulse waveforms are shown in Fig. 1.

The objective of Switching Cycling is to observe the degradation of the semiconductor through repetitive switching events. In this way, the degradation caused by switching events can be identified. Initial experiments are conducted at the rated pulse-current rating, and at 90 percent of the breakdown voltage. Device characteristics are recorded every six hours to monitor the degradation of key precursor parameters. Main parameters include threshold voltage, on-resistance, and gate leakage current. Shifts in the threshold voltage and on-resistance can be seen in Fig. 2.

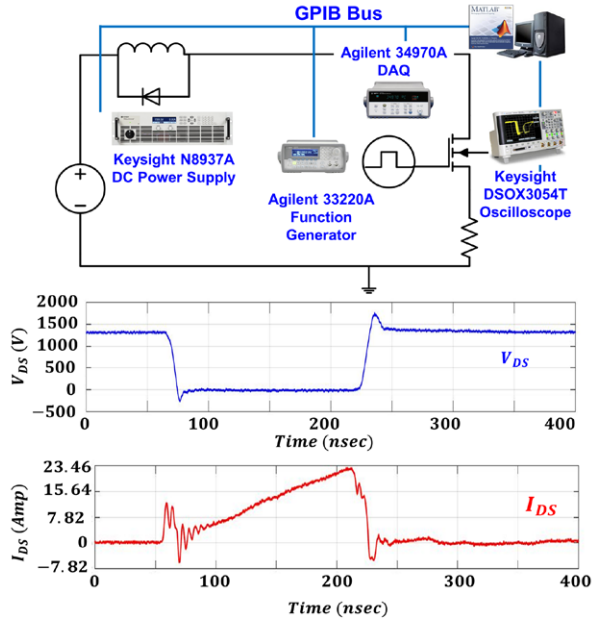


Fig. 1. Experimental test bed and experimental voltage and current waveforms.

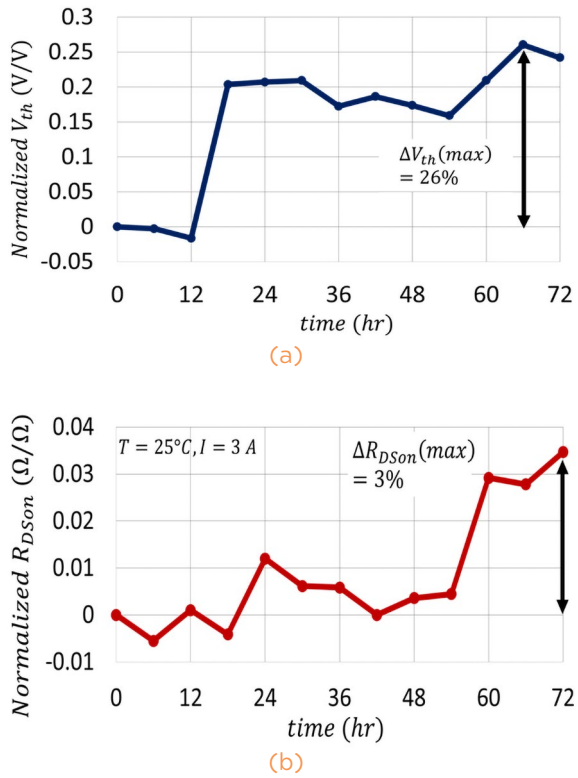


Fig. 2. Changes in threshold voltage (a) and ON-resistance (b) from switching cycling.

Optimized Coil Design for EV Charging with Medium Voltage Input

Inductive power transfer (IPT) is an appealing solution for charging electric vehicles (EVs) with its low maintenance requirement. The large volume for installation and the high power loss can limit the power level for high-speed charging. An optimization method was investigated to minimize the receiver coil of a 50 kW system with medium voltage (MV) input, enabling the integration of the receiver coil into the vehicle.

Coil inductances and resistances in conventional transformer are designed to minimize transformer loss while achieving desired system efficiency. This is then followed by mechanical and magnetic realizations. The main objective is to minimize receiver coil size while satisfying desired system efficiency. The basic idea for the optimization is to increase the transmitter size to enable a smaller receiver size, which is shown in Fig. 1.

The value of mutual inductance needs to be at certain value in IPT systems with series-series compensation for desired power level and fixed input and output voltage. Appropriate coil size is then designed to achieve the desired mutual inductance. Coil current increases with the power level, which will need larger wire gauge to have reasonable current density in the wire for thermal consideration so that coil size becomes larger at higher power level. In this work, smaller receiver coil size is enabled by increasing the number of turns at a larger transmitter coil to keep the mutual inductance at a certain range.

In the optimization, the receiver loss and transformer loss were calculated by sweeping for fixed receiver coil size and variable transmitter coil size. For each transmitter coil size, receiver loss and total transformer loss is calculated by sweeping turns number and turns pitch at transmitter and receiver. Pareto front is then utilized to show the trade-off between receiver loss and total transformer loss. Fig. 2 shows such pareto fronts for different transmitter sizes. For specific receiver size, maximum allowed loss can be determined with the thermal requirement under specific cooling conditions. An appropriate transmitter size that satisfies both the transformer efficiency and the receiver loss limit can be finally selected. An example of the design point is shown in Fig. 2 with receiver loss limited within 50 W and transformer loss limited below 200 W.

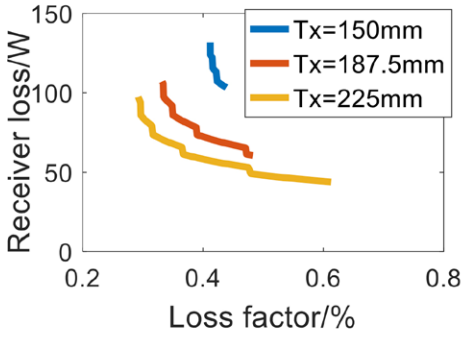


Fig. 1. Trade-off between receiver coil loss and transformer loss factor.

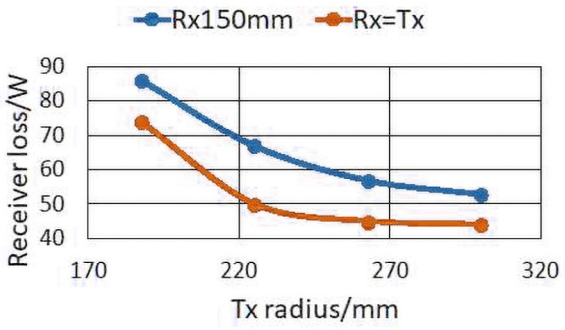


Fig. 2. Receiver coil loss decreases with increased transmitter coil radius.

Hierarchical Weight Optimization Design of Aircraft Power Electronics Systems Using Metaheuristic Optimization Methods

The more electric aircraft (MEA) concept has gained popularity in recent years. For traditional aircraft, the secondary power supplies on board are divided into three categories; the hydraulic power sources, the pneumatic power sources and the electric power sources. Unlike this case, on a more electric aircraft, the electric power sources will provide a majority of the power to the aircraft subsystems. As the main building blocks of the power distribution system, power electronics converters are doing their jobs in a complimentary way; highly efficient, reliable and lightweight compared to their conventional counterparts.

It is always desired to achieve optimized design for large-scale systems. In order to simply the optimization design process, the system-level design problem is broken into subsystem-level design problems. However, as optimized subsystems do not simply add up to optimized system, due to the interaction among them, multidisciplinary design optimization is proposed for this purpose, as shown in Figure 1. A comprehensive survey of the multidisciplinary design optimization architectures with single objective function and continuous design variables are given. In the field of power electronics, however, due to its nonlinear and discrete nature, in order to achieve system-level optimization design, for example, to minimize the weight of the aircraft power electronics system, hierarchical optimization structure is preferred. In this structure, a system-level design is divided into subsystem-level designs and subsystem-level designs are further broken into component-level designs by handling the interactions in the targeted system carefully.

To accommodate the above optimization process, as well as to improve its efficiency, metaheuristic optimization methods are used to speed up the design iterations. The metaheuristic optimization methods are motivated by natural selection and a social adaptation process and have two main categories; the population-based algorithms (e.g. generic algorithm (GA) and particle swarm optimization (PSO)) and the trajectory-based algorithms (e.g. simulated annealing (SA)). Compared with the classical optimization methods such as Newton's method, these metaheuristic optimization methods have demonstrated their ability to solve complex, highly nonlinear, and mixed integer optimization problems effectively.

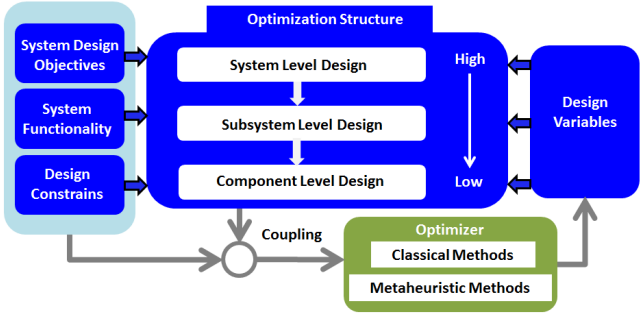


Fig. 1. Hierarchical optimization design flowchart.

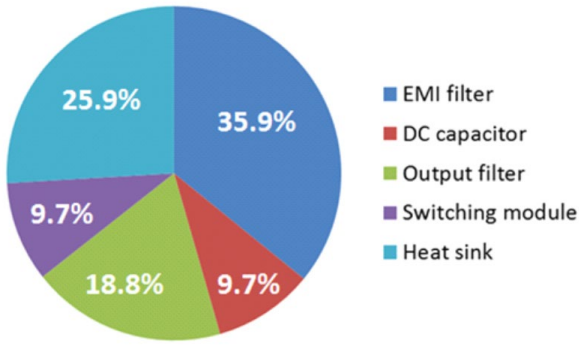


Fig. 2. Weight optimization result (compo-nent weight breakdown) of a 2 kW VSI.

Hetero-Magnetic Swinging Inductor (HMSI) and Its Application for Power Factor Correction Converters

Variable inductors with current dependent inductances are found in various power electronics applications. Swinging inductors with discretely varying gap lengths have step-wise L-I curves. A sloped air gap (SAG) inductor is a swinging inductor that has a smooth L-I curve. But, its maximum inductance is limited by the thinnest gap length and by the thickest gap edge. This fringing field can cause significant increase in winding loss at high frequency. This work introduces a swinging inductor (Fig.1) consisting of a core with simple, constant-length gap(s) that is (are) filled by materials whose magnetic properties are tailored for desired L-I curves. We call this configuration the hetero-magnetic swinging inductor (HMSI). The HMSI concept builds on our materials processing expertise in formulating filler materials with wide ranging magnetic properties. Together with the selection of gap length(s) and the core magnetic material, a HMSI offers greater flexibility for wider L-I swinging characteristics with low core loss and minimal fringe effect.

In this study, we applied the HMSI concept in a critical conduction mode (CRM) CRM power factor correction (PFC) boost converter (shown in Fig. 2) aimed at reducing the range of switching frequency range. CRM PFC converters have been widely used for ac-dc regulation to obtain good power quality due to their simple controller structure and no diode reverse recovery. However, large switching frequency variations of the converters increase the complexity of EMI filter designs. In a conventional CRM PFC boost converter, the switching frequency variation comes from the changing of the input line voltage with a constant value boost inductor throughout the whole line. By implementing a variable inductor whose inductance follows a designed function to attenuate the influence of the changing input line voltage, the switching frequency variation range can be reduced.

By combining different magnetic materials in one core to make a flexible swinging inductor and thereby reduce fringing effect, an HMSI targets reducing the switching frequency variation range for PFC converters. This simplifies the EMI filter design and improves the whole converter's power density. For application, a specific L-I function needed to limit the switching frequency range of a 150 W CRM PFC boost converter was calculated and a HMSI is designed and fabricated to meet this L-I function requirement. Testing results of a 150 W CRM PFC boost converter with HMSI and a linear inductor are compared.

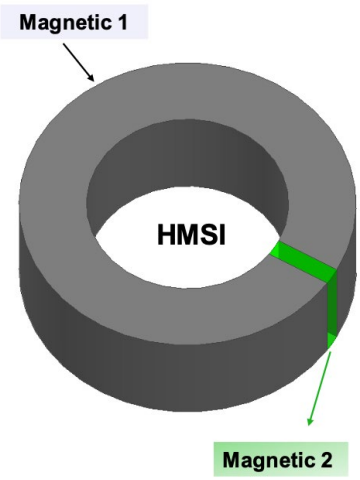


Fig. 1. Concept of hetero-magnetic swinging in-ductor (HMSI).

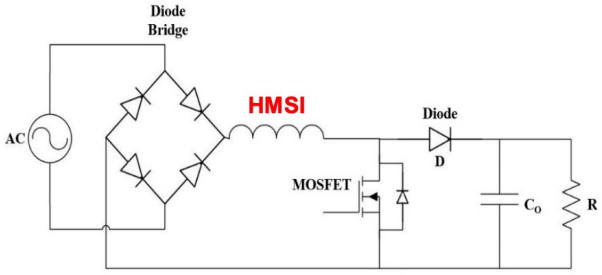


Fig. 2. Schematic of CRM PFC converter.

Wide Bandgap High Power Converters and Systems (WBG-HPCS) Consortium Nuggets

STATCOM-Based Transient Frequency Regulation in a Transmission System

Ultra-Wide Input Auxiliary Power Supply Using 3.3 kV SiC MOSFETs

Dual Active Bridge Converter for Medium Voltage Grid Connected Electric Vehicle Charging Application

ZVS Turn-On Triangular Current Mode (TCM) Control for Three Phase 2-Level Inverters with Reactive Power Control

Evaluation of Alternative Active Capacitor Banks for Floating H-Bridge Power Modules

Optimization of Modular Filter for Multi-Channel Three-Phase Interleaved AC-DC Converters

Startup Synchronization Analysis in PV Inverters with Virtual-Synchronous-Machine-Based Controls

High Power Density GaN-Based Interleaved Buck DC-DC Converter for 1 kW Brick Modules with 98.5% Efficiency

Design of a Multilayer Planar Bus for Medium-Voltage DC Converters

10 kW High Efficiency Compact GaN-Based DC/DC Converter Design

Stability Impact of PV Inverter Generation on Medium-Voltage Distribution Systems

Utility-Scale PV inverter Impedances in D-Q Frame Under Different Q-Control Modes

STATCOM-Based Transient Frequency Regulation in a Transmission System

With the increasing usage of renewable energy sources throughout the world, transient regulation is becoming a growing research area. Using a 200 MVA synchronous generator in a simple generator-STATCOM-load configuration, transient regulation with a 100 MVA STAT-COM reduces grid frequency perturbations.

Simulink is used as a simulation environment, having a 200 MVA synchronous generator connected to a 60 Hz simple transmission system through a 210 MVA, 13.8 kV/230 kV transformer. A 5 MW load is also connected directly to the synchronous generator to roughly approximate generation losses. The transformer is then connected to a lossless transmission line. Connected in parallel to the generator is a 100 MVA STATCOM. The transmission line then connects the generation and STATCOM side to a 50 MW, 50 MVar load.

Additionally, a governor is included to control and regulate the frequency of the generator. For the STATCOM, a DG controller is created and simulated, seeking to provide both constant point-of-common-coupling (PCC) output voltage control and constant grid frequency control. A phase-locked loop (PLL) is simulated with a 5 Hz bandwidth to obtain grid frequency information. The frequency controller has a bandwidth of 200 Hz to increase transient regulation speed. In addition, the STATCOM is also simulated with a controller designed to maintain constant grid frequency and to provide constant output power to the grid. These two STATCOM control schemes are simulated in the simple system, with the load having a step between +5 percent and -5 percent, and are then compared to the results of the system simulated with just the governor-controlled generator.

STATCOM-based transient frequency regulation is shown to improve frequency perturbations in a simple system simulation. Frequency takes less time with either STATCOM controller turned on than with just the generator regulating the frequency. Furthermore, overshoot and undershoot of frequency from 60 Hz is decreased with the STATCOM controller. These results provide preliminary optimism that STATCOMs can be used as an effective frequency controller, thus contributing to the stability of renewable power generation.

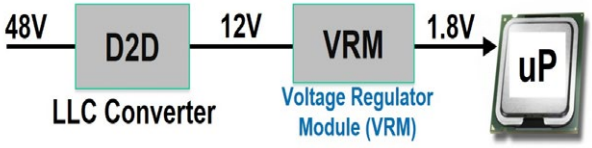


Fig. 1. Two-stage 48V-12V-1.8V VRM structure.

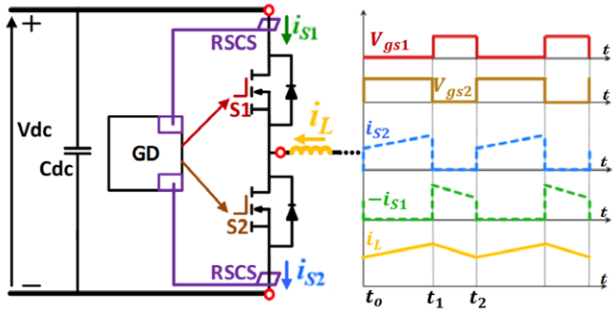


Fig. 2. Phase current reconstruction principle.

Ultra-Wide Input Auxiliary Power Supply Using 3.3 kV SiC MOSFETs

Modular multilelvel converters (MMCs) are widely used for various applications, including high voltage direct current transmission, motor drives, and renewable energy applications, such as 1.5kV photovoltaic inverters. MMCs are made up of multiple submodules connected in series. In order to enable a seamless operation of MMCs, an auxiliary power supply is needed to provide power to the control unit (see Fig. 1). This auxiliary power supply should accept a wide input range of voltage as the voltage of the submodule (SM) dc-link capacitor fluctuates from several hundred to several thousand volts. Therefore, there are many challenges to designing and developing a converter that can realize the output voltage and the load regulation of the auxiliary power supply for a wide input voltage range.

Currently, there are two stage cascaded options to designing an auxiliary power supply that can meet the requirements of the MMCs. In this work, a single stage flyback converter is used to provide a regulated 48 V at the output from a wide input voltage range. This topology is scalable in terms of input blocking voltage and output power when input is series connected and the output is parallel connected. For this to work, the flyback-based auxiliary power supply incorporates a single 3.3 kV, 30 A discrete device. A prototype is being designed to enable a regulated output from a wide-range high-voltage input.

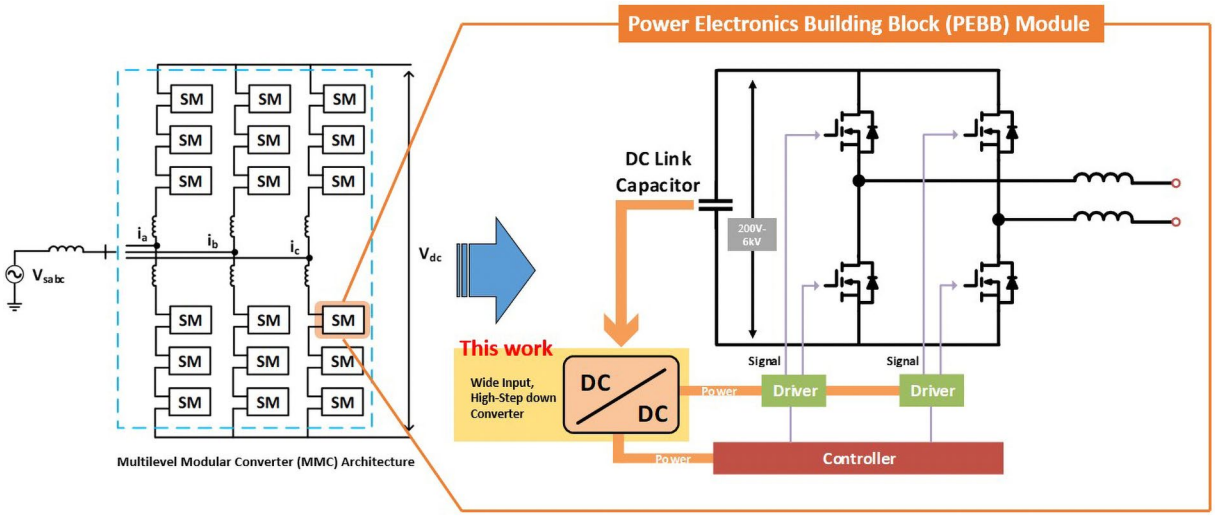


Fig. 1. Wide input, high-step-down ratio converter for auxiliary power supply.

Dual Active Bridge Converter for Medium Voltage Grid Connected Electric Vehicle Charging Application

Dc fast charging stations are becoming more prevalent as the numbers of electric vehicles (EV) on the road have increased significantly. In order to shorten the charging time and extend the driving range of EVs, the development of high-power, off-board charging stations is necessary. The conventional architecture of a dc fast charger incorporates either a local or a centralized front-end converter that interfaces with the medium-voltage (MV) grid via a low-voltage (LV) line frequency transformer. Fig. 1 shows an example architecture of the conventional dc charging station. This type of architecture is limited, due to the large size and installation costs of the line-frequency transformer.

There has been extensive research conducted in order to eliminate this bulky line frequency transformer. One example structure that allows a direct interface between the charging stations and the medium-voltage grid is shown in Fig. 2. A modular system architecture is used to connect multiple converters in series. This type of architecture can provide benefits to reducing the size requirement for the service transformer and it allows a high-power charging of the EV battery from the direct interface to the medium-voltage grid.

In this work, a dual active bridge converter is explored for the MV grid connected EV charging architecture. Furthermore, for the development of the medium-voltage dual active bridge converter, 3.3 kV SiC MOSFETs are used.

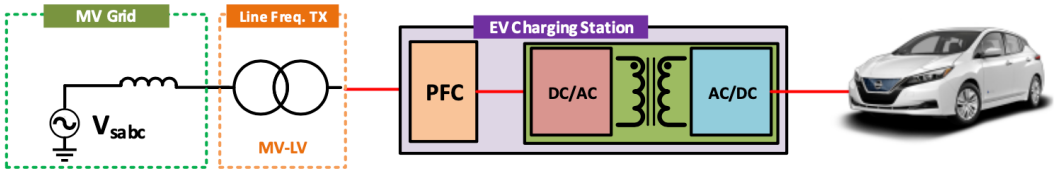


Fig. 1. Conventional Electric Vehicle Charging Station Architecture.

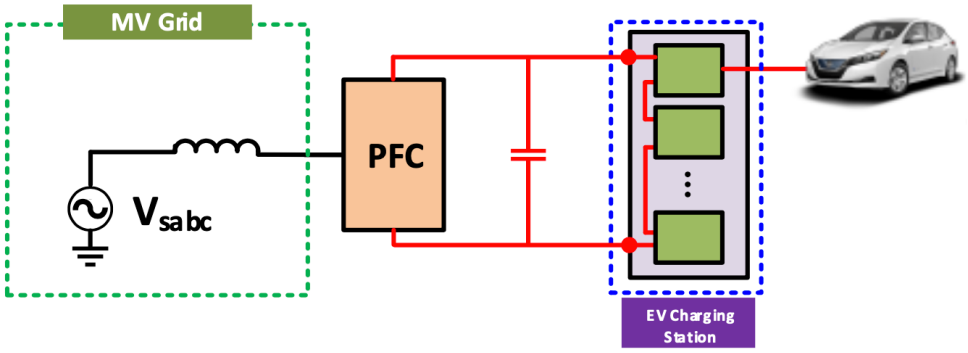


Fig. 2. Medium Voltage Grid Connected Electric Vehicle Charging Station Architecture.

ZVS Turn-On Triangular Current Mode (TCM) Control for Three Phase 2-Level Inverters with Reactive Power Control

Critical conduction mode (CRM)/Triangular current mode (TCM) control with ZVS turn-on for single phase inverters has led to significant improvements in efficiency at high switching frequencies (>300 kHz). The need to push power converters to high switching frequencies results from the drive to achieve higher power density. High-frequency operation helps to achieve higher power density as it leads to a significant decrease in filter volume which consumes most of the space in power converter systems. With recent advancements in wide bandgap device technology, it is possible to operate at high switching frequencies with very low turn-off losses (<5 W for a 1.2 kW three phase 2-level GaN inverter at 1 MHz switching frequency). A huge increase in power density (from 30 W/in^3 to 80 W/in^3) is achieved by pushing the switching frequency to 1 MHz. The turn-on losses in hard switching continuous conduction mode (CCM) though are still significant (>40 W for the above specified operating conditions). Thus, it is necessary to operate the inverter with zero voltage switching (ZVS) turn-on.

However, as the switching frequency in TCM is voltage dependent, a synchronized operation in all three phases can be achieved by operating in a combination of TCM + DCM operations. This new control scheme for inverters is proposed, however this technique should not be limited to just unity power factor operation. In fact, reactive power control becomes all the more necessary for inverters as the grid can have reactive loads or reactive power requirements. Additionally, TCM control, with ZVS turn-on in inverter mode for full range of power factor, is presented in this work. It is also shown that, even with higher ripple, TCM maintains similar efficiency at 1 MHz as CCM in 50 KHz while achieving 3× power density.

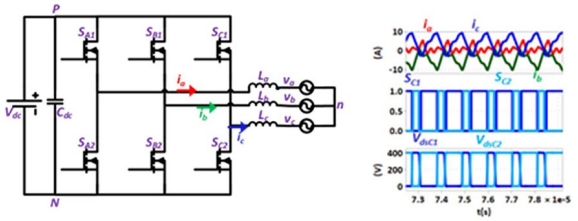


Fig. 1. Circuit schematic of three phase 2-level inverter with basic principle of ZVS turn-on with TCM.

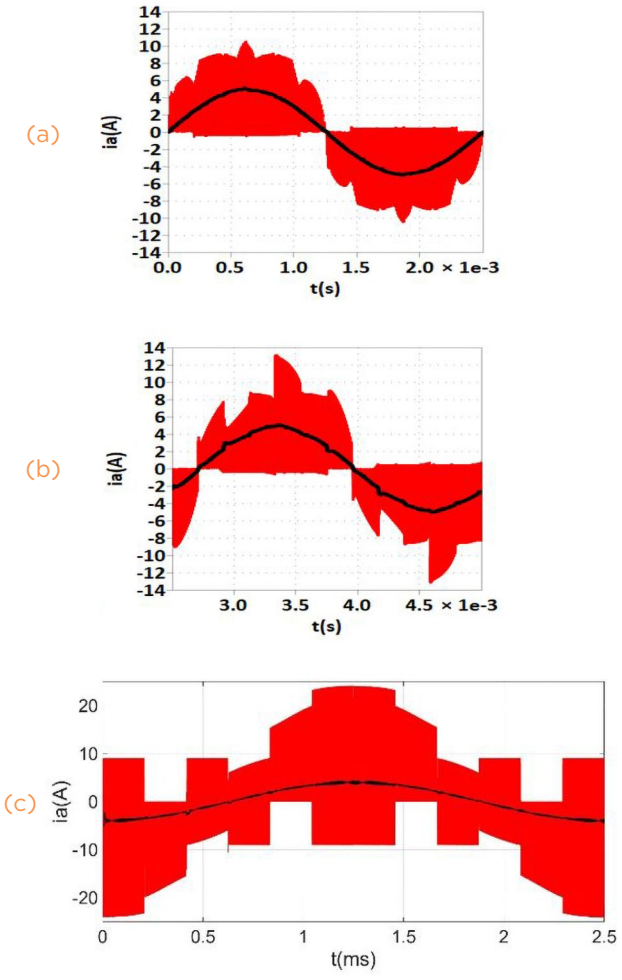


Fig. 2. Phase A current for 1.2 kW, 400 V Vdc, 115 V Vacrms for (a) unity power factor, (b) 30° lagging, and (c) 90° lagging.

Evaluation of Alternative Active Capacitor Banks for Floating H-Bridge Power Modules

Although single-phase power converters have begun to be widely used, one of the main concerns with this topology is that high-order harmonics exist in the system, including second-order harmonics in single-phase voltage inverters and rectifiers. Traditionally, a large aluminum electrolytic capacitor is used to suppress the voltage fluctuation caused by those harmonics. However, this considerably increases the system's volume, and thus reduces the power density.

To cope with these disadvantages, methods utilizing alternative active capacitor banks (AACBs) have been applied. The AACB is an additional circuit connected to the system to absorb the fluctuating power and maintain a constant dc-link voltage. Since the fluctuating voltage allowed on the auxiliary circuit is large, the AACB's capacitance is much smaller than that of the traditional capacitor bank. Moreover, the longer lifetime of the AACB's film capacitors, compared to aluminum electrolytic capacitors, helps to increase the system's reliability.

In this paper, the AACB is applied to a floating H-bridge, which is a popular configuration in power converter systems. The floating H-bridge is used as a perturbation injection unit (PIU), which can generate a single-tone frequency current for measuring the impedance. The AACB consists of one full bridge, one inductor, and three film capacitors, and is connected in parallel with the floating H-bridge, as illustrated in Fig.1. Due to the interaction between the injection current and the voltage source in the ac side of the floating H-bridge, multiple harmonic components appear on its dc side. The injection frequency, which is nearest to the grid frequency, causes the largest ripple on the dc-link voltage.

The AACB's full bridge is regulated so that its output voltage v_{ab} satisfies:

$$v_{ab} = -v_{C1} \ (\text{AC}). \qquad \text{Eq. 1}$$

Simulation waveforms obtained from the average model of the AACB with total capacitance value of 3.1 mF interfaced with a PIU are illustrated in Fig. 2.

The current with multiple harmonics on the dc side of the floating H-bridge causes an ac voltage fluctuation across the capacitor C1, with peak magnitude of 345 V. From the magnified waveform shown in Fig. 2, the peak-to-peak ripple on the dc-link voltage is around 30 V. Under the same operating condition, the required value of the capacitor bank using the traditional method is 75 mF. This indicates that the AACB can help reduce the capacitance by more than 20 times compared to the traditional method.

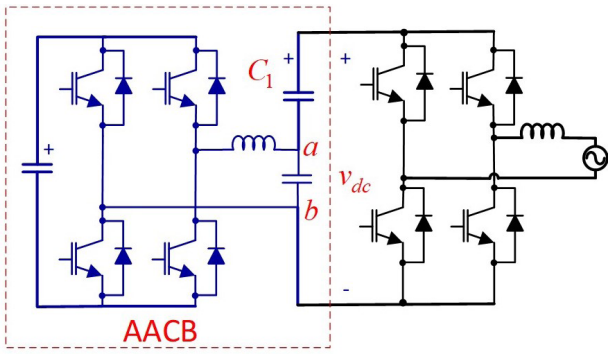


Fig. 1. AACB connected to the floating H-bridge in a perturbation injection unit.

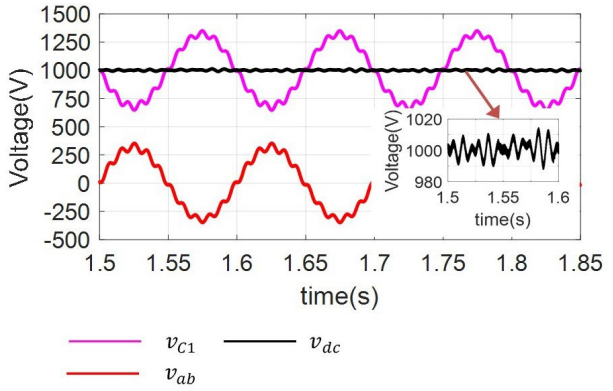


Fig. 2. Voltage waveforms v_{C1}, v_{ab}, and v_{dc} of the AACB-PIU system.

Optimization of Modular Filter for Multi-Channel Three-Phase Interleaved AC-DC Converters

The concept of a decoupled modular filter is introduced to handle EMI, power quality (PQ), THD and circulating current between channels for three-phase interleaved ac-dc converters. A modular filter should be fault tolerant, scalable, and easily replacable in the field and should operate for single- and multi-channel converter systems. For an interleaved converter, the DM and CM circulating current is attenuated through either three-phase boost or DM (E core) inductors and CM choke respectively. This increases the size of the ac side filter components compared to parallel converters. Also, due to phase cancellation of switching frequency harmonics on the grid side, the THD limit is easily met. This leads to an overdesign of the passive components for N channel interleaved converters.

Keeping this in mind, an N channel optimization procedure is developed to meet EMI, THD specification and individual current harmonic levels. However, no general guideline exists for peak circulating current limits, so the device conduction loss is used as the design criteria.

Several decoupled topologies are proposed based on filter location such as dc-side, ac-side and grid-side filter building blocks (FBB) as shown in Fig. 1. A comparison between the topologies is done using the optimization tool. Also, a comparison between 2L and 3L converter topology itself is made. Resonant frequency, reactive power limits, leakage current requirements and fixed grid-side impedance are considered in the filter design process. A basic terminal model with heat-sink capacitance to ground and ac capacitance to ground is used to represent EMI behavior.

The final design is verified with simulation studies to meet EMI PQ and circulating current limit criteria. The paper includes the optimization algorithm and comparison between decoupled topologies in detail. The analysis is simplified by creating a harmonic decomposition between phases and converters.

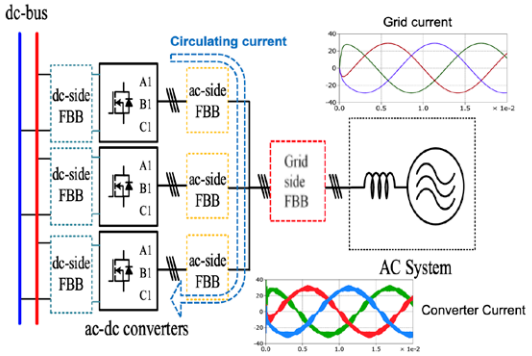


Fig. 1. N channel interleaved modular filter topology.

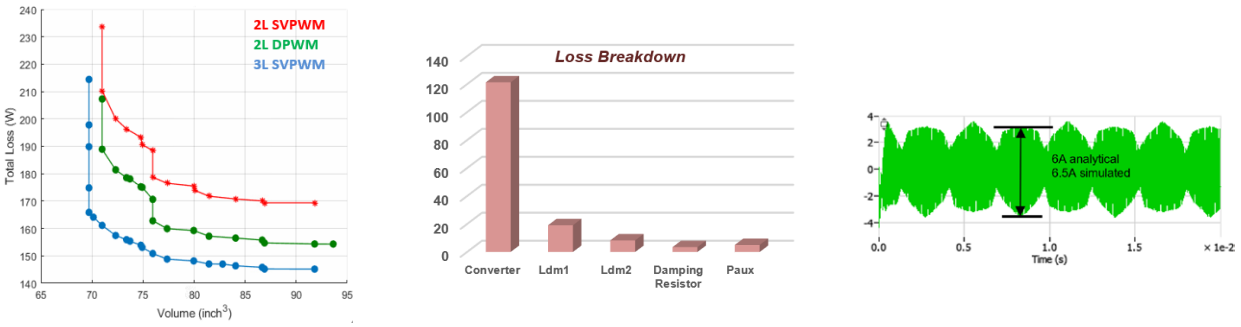


Fig. 2. Comparison between converter topologies and loss, loss breakdown, circulating current check.

Startup Synchronization Analysis in PV Inverters with Virtual-Synchronous-Machine-Based Controls

The proliferation of grid-tied inverters is redefining the profile of power generation sources in utility-scale power systems. As a result, it is necessary to ensure the continued nominal operation of the power system. A 250 kW grid-tied photovoltaic (PV) inverter with virtual-synchronous-machine- (VSM) based control, shown in Fig. 1, is studied. In contrast to a conventional control scheme that utilizes a phase-locked loop (PLL) for synchronization, VSM-based control emulates the characteristics of a synchronous machine, including its inertia, by using a swing equation. As a result, this method can synchronize via the power-balance method. However, with the variability introduced by PV generation sources, continued stability of the altered system should be ensured.

A system of equations is derived to describe an average model of the grid-tied PV inverter. The small-signal model of this system is obtained through linearization around an operating point. The linearized system allows for stability analysis via parametric sensitivity.

Parametric sensitivity is used to observe the sensitivity of a system's eigenvalues that occur due to variations in parameters. Fig. 2 demonstrates the movement of the dominant eigenvalues as the inertia Jspc, H, in the inertia-emulation portion of the VSM control increases: the complex conjugate pair of eigenvalues draws near the real axis, thus indicating that an increase in this parameter could lead to instability in the studied system.

This work implements this method of analysis in order to parameterize control variables in the VSM block of the control scheme prior to and after synchronization to ensure system stability.

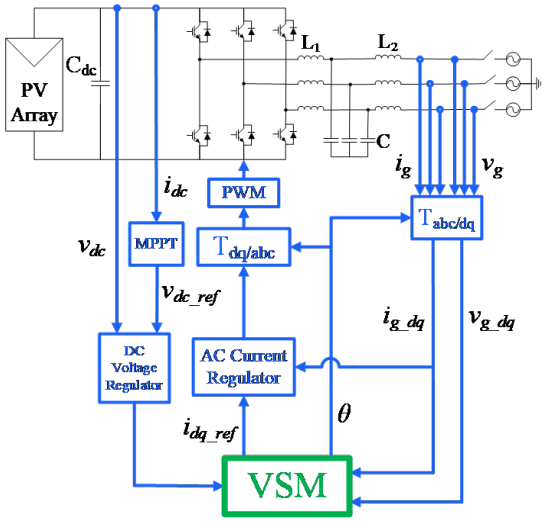


Fig. 1. 250 kW inverter with VSM-based control.

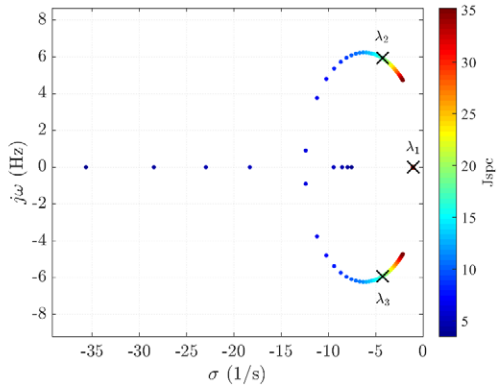


Fig. 2. Movement of eigenvalues as Jspc increases.

High Power Density GaN-Based Interleaved Buck DC-DC Converter for 1 kW Brick Modules with 98.5% Efficiency

The 48 V intermediate bus converter (IBC) is widely used in telecom, wireless, and aerospace applications. With increasing demand in power by the load, there is a need for higher-power converters with high power densities and high efficiencies. The use of gallium nitride (GaN) devices allows the converter to run at higher switching frequencies with lower loss. At higher switching frequencies, the magnetics are smaller; if planar magnetics are used, the power density and efficiency can be increased.

The buck converter provides regulation, and the LLC-DCX provides isolation for the two-stage converter. The buck converter regulates a variable input from 40 V–60 V to 36 V at the bus at 1 kW. By using an interleaved buck converter, the conduction and switching losses can be decreased. The overall two-stage converter needs to have both high efficiency and power density, so the area of the buck converter is limited to 30x35x7 mm. Based upon the footprint limitations and preliminary size of the inductor, the most optimal topology for the buck converter is a four-phase interleaved buck converter with two separate coupled inductors.

The efficiency and power density of the buck converter will be determined by the design of the coupled inductor. By starting with the footprint and inductance, all of the losses for the entire buck converter can be calculated. The estimated efficiency versus the power density can be plotted, and then a design point can be chosen.

A prototype buck converter has been built, which is shown in Fig. 1, and can achieve 98.5 percent efficiency. Fig. 2 shows the buck converter operation in steady state. The current waveform shows the inverse coupling of the inductor. The two-stage converter was able to achieve 96 percent efficiency with a power density of 680 W/in^3, which is higher than the current state-of-the-art two-stage 48 V IBC.

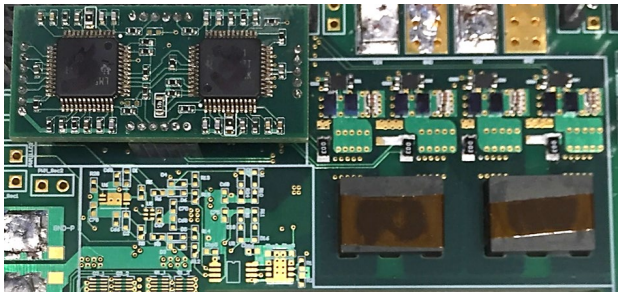


Fig. 1. Four-Phase Buck Converter and LM5170 Controllers.

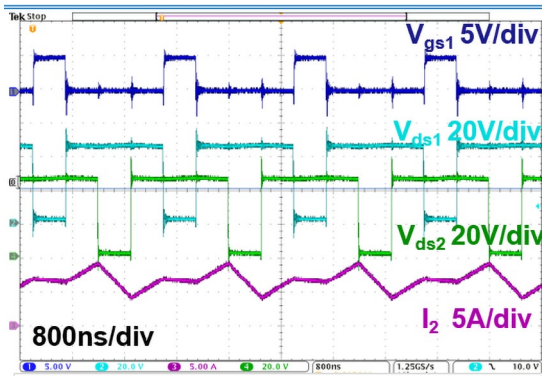


Fig. 2. Experimental Waveforms of Buck Converter In Steady State.

Design of a Multilayer Planar Bus for Medium-Voltage DC Converters

Silicon carbide (SiC) allows wide-bandgap (WBG) devices to operate at higher voltages and switching frequencies. The adoption of these WBG devices means medium-voltage power electronic converters can now advance rapidly. To fully leverage these SiC attributes, power loop inductance must be minimized. The dc-link bus is an area of opportunity for improvement. Reducing conductor spacing not only provides a smaller parasitic inductance, it can also decrease the converter's overall size and weight; however, higher voltage actually requires an increase in conductor spacing. The manufacturing process for a traditional laminated bus increases the likelihood for internal defects. These defects coupled with a high electric field (E-field) intensity increase the likelihood of partial discharge (PD) within the insulator. PD can cause premature system failure due to insulation degradation. This leaves designers with the tradeoff of increasing the bus thickness for reliability, or decreasing the thickness for improved switching performance.

In this work, a low-inductance printed circuit board- (PCB) based bus is designed to support Wolfspeed's XHV series 10 kV SiC MOSFET module. The construction process of a PCB exacerbates challenges seen in a traditional laminated bus. A custom dielectric has been selected for PCB construction to further reduce the likelihood of voids, thus further reducing the likelihood of PD.

The E-field was analyzed in high-intensity regions using COMSOL for finite-element analysis (FEA). A midpoint layer separating the +/- dc layers was implemented to reduce the peak intensity near the insulator/connector interface. Geometric techniques for field control along the surface and within the PCB were implemented using the design flow shown in Fig. 1. The results for the final E-field intensity after completion of the design flow are shown in Fig. 2. It should be noted that the field in air is of interest in the bottom image shown in Fig. 2; therefore, data above 2 kV/mm has been restricted and appears white.

Simulation results show that the peak E-field intensity can be reduced by adding a slight offset between conductors at different potentials. Due to the voltages of interest, the E-field intensity in air was most efficiently controlled by forcing the field into an additional dielectric layer placed on the outside of what would normally be the outermost power plane. A prototype has been fabricated and tested to verify a PD free bus at voltages greater than 10 kV.

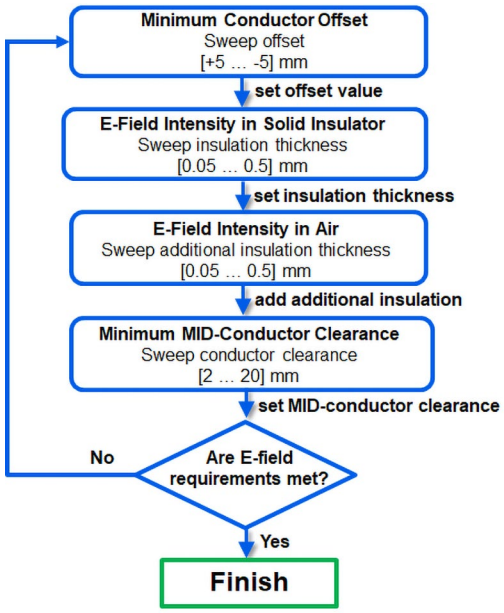


Fig.1. PCB design flow for electric field control.

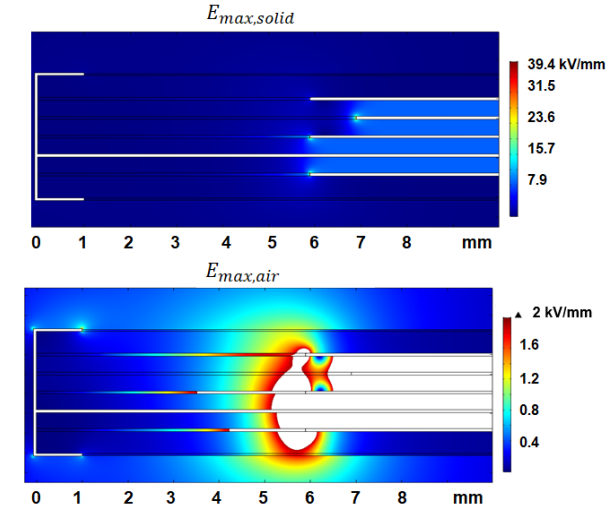


Fig. 2. Electric field strength (top) in dielectric (bottom) air.

10 kW High Efficiency Compact GaN-Based DC/DC Converter Design

The LLC resonant converter has been widely adopted in telecom and transportation applications for its high efficiency performance, as well as its ability to achieve zero-voltage switching (ZVS) for all switches under different load conditions. In the LLC resonant converter design, the adoption of wide-bandgap (WBG) devices, especially gallium nitride (GaN) devices, contributes to a significant improvement of efficiency and power density, due to high switching speed, low switching loss, no reverse recovery loss, and small package. This paper presents a 10 kW LLC converter design using 650 V 60 A e-mode GaN HEMTs with wide regulation, achieving high efficiency and high power density simultaneously.

To conduct high current and further reduce the on-resistance, the switching cell of a half bridge with paralleled GaN HEMTs is introduced. Fig. 1 shows the PCB design with four devices in the half bridge located on the top layer of the PCB, and the bus decoupling ceramic capacitor at the back side, which achieves 0.814 nH power loop inductance based on Q3D simulation. A universal connector employed for the switching cell, enables easy replacement and debug capabilities. The heat sink dedicated to the GaN-based switching cell, is designed according to the requirements of device loss, room temperature, and device operating temperature. For verification, a complete procedure in which conducting reverse current with negative gate voltage to measure the thermal resistance is developed, and can be generalized to other converter thermal management applications.

In order to achieve high efficiency and high power density, the transformer and the resonant inductor are integrated together on an 'E' 'I' core with litz-wire. A large resonant inductor, which can be controlled by a center leg width, helps to achieve wide regulation range. The transformer dimensions and inductances are optimized based on the Pareto front between converter volume and frequency. Using the selective design above, a compact structure is achieved, as shown in Fig. 2. Vertical space within the converter can be fully utilized with the same height of the switching cell, the fan, the transformer, and the input and output capacitor. Furthermore, the air flow from the fan can be effectively used for the heat dissipation of the transformer and the devices.

This paper presents a complete and detailed design procedure for a 10 kW GaN-based LLC resonant converter with a paralleled 650 V 60 A e-mode GaN. The work includes both layout consideration and thermal management. The integrated transformer design with a Pereto front is introduced. The final LLC resonant converter features a dimension of 278 x100 x 45 mm, achieving a 97.9 percent peak efficiency, and a 131 W/in^3 (8 kW/l) power density.

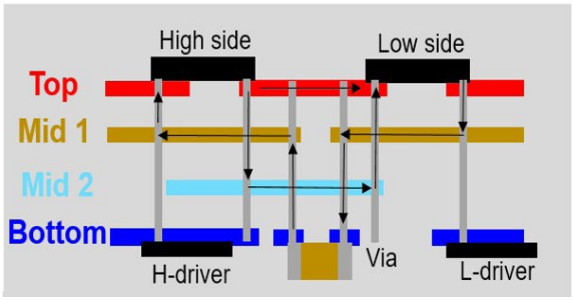


Fig.1. Power loop design using 4-layer PCB.

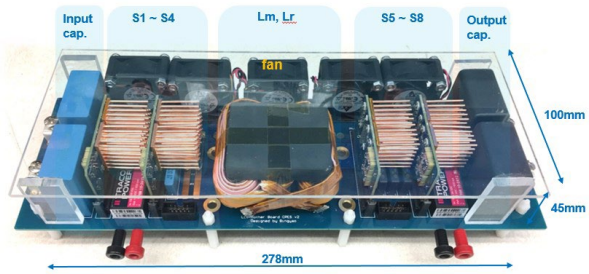


Fig. 2. All-GaN-based 10 kW LLC resonant converter.

Stability Impact of PV Inverter Generation on Medium-Voltage Distribution Systems

Renewable energy generators in distribution systems have recently increased in proliferation. Due to their high impedances, distribution systems are weaker than transmission systems. In addition, the impact of photovoltaic (PV) generators on the voltage profile impels the requirement of PV reactive power regulation from grid code. In the near future, PV generators will have more complicated reactive-power control strategies instead of working under unity power factor. This raises the question whether PV generators in the distribution system will cause any stability problems.

To assess small-signal stability, this paper employs the Generalized Nyquist Criteria (GNC) method based on measured impedances in DQ frames at connection interfaces. The GNC method has the advantage that interconnection stability can be judged without knowing details about the grid and PV generator model. Based on a distribution system that has 56 buses, a comparison is done among PV inverters at different physical locations and with different reactive-power control modes and operation states to determine their impact on the system's operation and stability.

The PV farms connected to different branches of a complicated radial distribution system may have interactions with each other when they are under volt-var droop-mode control. So the control strategy and parameters of the PV generator should be designed with consideration given to the impact of other PV generators. If models of other generators are not accessible, the GNC method based on impedance measurement should be used for stability assessment.

Higher capacity of PV penetration makes this stability problem worse. Moving any of the PV farm closer to the substation reduces the possibility of instability. Volt-var droop mode is more flexible and beneficial for grid voltage regulation compared to unity power factor or constant Q control modes, but raise the possibility of unstable PV connection, especially when PV is working in inductive zone in droop curve. There is a tradeoff between grid voltage regulation and stability.

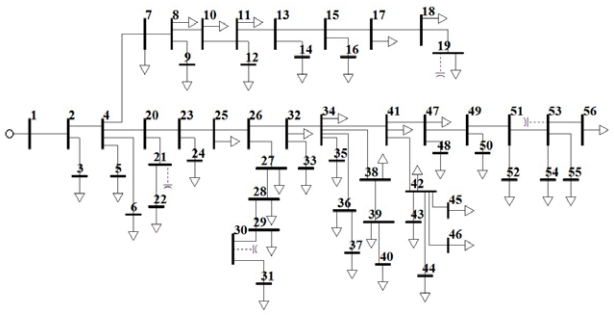


Fig.1. One line diagram of the distribution system.

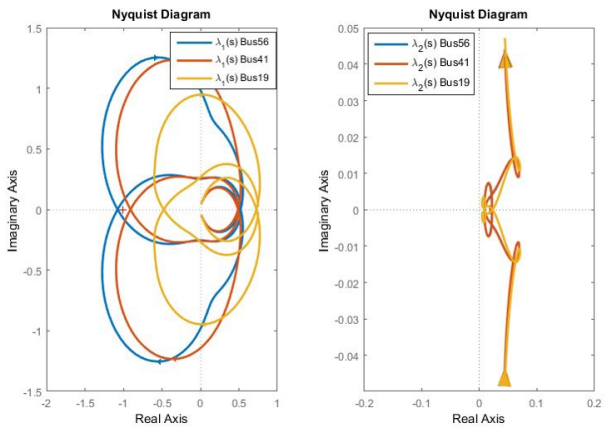


Fig. 2. Nyquist plots of eigenvalues of return ratio matrix L when the second PV farm is at a different location.

Utility-Scale PV inverter Impedances in D-Q Frame Under Different Q-Control Modes

With the worldwide development of renewable energies, power systems are seeing higher proliferation at the distribution and transmission levels. Since the negative incremental resistance caused by the constant-power behavior of power converters may cause stability problems, the stability of photovoltaic (PV) integration with the distribution system has begun to attract greater attention. Different from real-time simulations or the character root method, both of which require full models of all components in the distribution system, the generalized Nyquist stability criterion (GNC) for stability analysis of a three-phase ac power system uses only the measured D-Q frame impedances. Compared to the positive sequence impedance method, the D-Q frame impedance matrix method is more accurate for stability assessment of a system with a PV inverter that has non-symmetrical control in the D-Q frame, including dc voltage-loop and phase-locked-loop (PLL) controls. This work derives the D-Q frame impedances of utility-scale PV inverters under five reactive power modes, compares different Q control modes, shows the GNC application result based on impedances, and validates the impedance model using hardware experiments. Instability may occur when PV inverters are under reactive-power control mode of the volt-var (reactive power is a droop function of ac voltage), as a result of interactions among the voltage control of multiple PV inverters in parallel.

The terminal impedances in DQ frame are derived from utility-scale PV farm based on small signal model of PV inverters. A comparison is done among impedances of PV inverters under five different reactive power control modes, based on which GNC is used to assess the grid-PV connection stability. The volt-var control mode changes PV terminal impedance signs and magnitudes significantly and may cause unstable connection to the grid. The stability assessment is proved by time domain simulation and the derived impedances are validated by scaled-down hardware experiments.

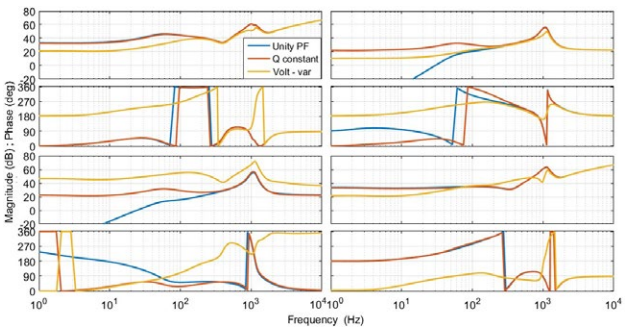


Fig.1. PV impedances under mode 1 unity power factor, mode 2 constant Q, and mode 5 volt-var droop control.

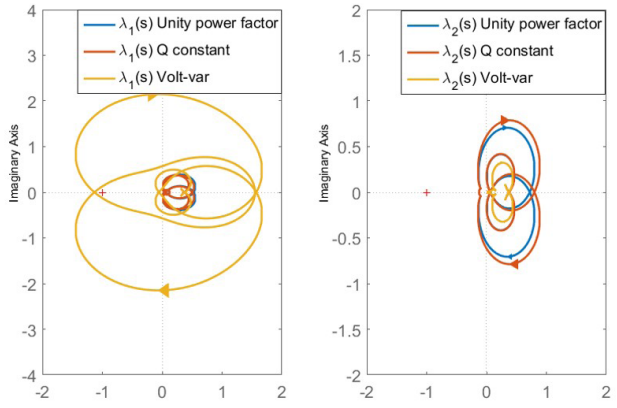


Fig. 2. Characteristic loci of PV connection to the grid.

Sponsored Research Nuggets

Non-Ideal Power Take-Off Modeling with Equivalent Circuit for Multi-Physics Simulation in Wave Energy Harvesting

Method for Increasing AC-DC Voltage Gain of Three-Phase Critical Conduction Mode Converter

A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger

Electric Field Control in Wide Bandgap Power Electronics Modules Via Geometrical Techniques

The Optimal Design of GaN HEMTs Active-Clamp Flyback Converter with Wide-Input Range

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Triangular Current Mode Boost Inductor Optimization Using 2-D Finite Element Analysis and the Improved Generalized Steinmetz Equation

High-Frequency Transformer Design for Modular Power Conversion from Medium-Voltage AC to 400 V DC

UV-Curable Ferrite Paste for Additive Manufacturing of Power Magnetics

Analytical Models for Superjunction Power Transistors with Interface Charges

Phase Current Sensor and Short-Circuit Detection Based on Rogowski Coils Integrated on Gate Driver for 1.2 kV SiC MOSFET Half-Bridge Module

Phase Current Reconstruction Based on Rogowski Coils Integrated on Gate Driver of SiC MOSFET Half-Bridge Module for Continuous and Discontinuous PWM Inverter Applications

SiC MOSFET Characterization and Reliability at 300° C

Single Pulse Common-Mode Voltage PWM Scheme to Achieve High Power Density for Full-SiC Three-Level Uninterruptible Power Supply

Design Comparison of Three-Level, Three-Phase Photovoltaic Inverter Operating in Continuous Conduction Mode and Triangular Conduction Mode

Decoupled Modeling of Three-Phase TCM Inverters Utilizing Three Different Conduction-Modes for ZVS Operation

A Simplified Digital Closed-Loop Current Control of Three-Phase PV Inverter Operating in Triangular Conduction Mode

Design of 20 kW Full-SiC, Three-Level Three-Phase Uninterruptible Power Supply

Voltage Balancing of Series-Connected Silicon Carbide MOSFET Modules Using Active DV/DT Control

Distributed Control and Communication System for SiC-Based Modular Power Converters

Short-Circuit and Overload Gate-Driver Protection Schemes for 1.2 kV, 400 A SiC MOSFET Modules

Analysis and Control of a Transformerless Series Injector Based on Paralleled H-Bridge Converters for Measuring Impedance of Three-Phase AC Power Systems

Model of Hysteresis and Magnetoelectric Effect for a Voltage-Controllable Inductor

Design and Testing of 1 kV H-Bridge Power Electronics Building Block Based on 1.7 kV SiC MOSFET Module

Design and Testing of 6 kV H-Bridge Power Electronics Building Block Based on 10 kV SiC MOSFET Module

A High-Speed Gate Driver with PCB-Embedded Rogowski Switch-Current Sensor for a 10 kV, 240 A, SiC MOSFET Module

Design and Control of Tunable Piezoelectric Transformer Based DC-DC Converter

Design of a Compact, Low Inductance 1200 V, 6.5 mΩ SiC Half-Bridge Power Module with Flexible PCB Gate Loop Connection

Design Space of Vertical GaN Superjunction Power Transistors for 1.2-10 kV Applications

Medium Voltage SiC Based Converter Laminated Bus Insulation Design and Assessment

Electrical Field Analysis and Insulation Evaluation of a 6 kV H-Bridge Power Electronics Building Block (PEBB) Using 10 kV SiC MOSFET Devices

Design of a SiC-Based 5-Level Stacked Multicell Converter for High-Speed Motor Drives

Design of a Zero Voltage Switching Class-E Inverter with Fixed Gain

Non-Ideal Power Take-Off Modeling with Equivalent Circuit for Multi-Physics Simulation in Wave Energy Harvesting

This work provides a methodology to build a high fidelity equivalent circuit for nonlinear power take-off (PTO) and simplifies the mathematical model with an equivalent circuit model. The parameters in the circuit model are extracted through multiple testing conditions, and the resulting model with extracted parameters is validated under time domain with multiple test conditions.

A mechanical-type PTO column in a wave energy conversion (WEC) system consists of components including a ball screw, a mechanical motion rectifier (MMR) gearbox, mechanical couplings, one-way clutches, and a generator. Circuit models for the dry frictions, viscous dampings, and the compliances in these components are described, so the non-ideal efficiency and nonlinear force of the PTO are predicted in an electrical simulation by integration of these sub-circuit models. This is accomplished through a nonlinear system identification method that compares the results from the simulation circuit model and the experimental results. The equivalent circuit model of the overall mechanical system is built as shown in Fig. 1.

The system test setup is shown Fig. 2(a). The validation results in Fig. 2 (b) and (c) show that the equivalent circuit can be used to predict the mechanical input force of the nonlinear PTO time domain in the time domain, and the mechanical efficiency of the system, under various operating modes. The multiphysics circuit-based model can accurately predict the characteristics of PTO. Compared to a mathematical only model, it can simplify the modeling and parameter extraction process.

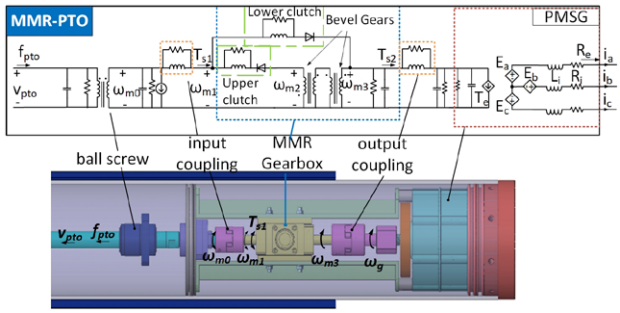
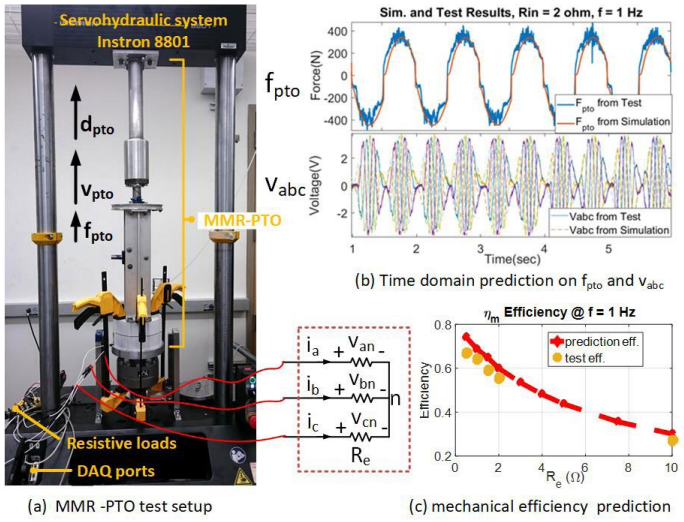


Fig. 1. Design of the PTO and its equivalent circuit including the ball-screw, MMR gearbox, mechanical couplings, shafts, and generator.



(a) MMR -PTO test setup

(b) Time domain prediction on f_{pto} and v_{abc}

(c) mechanical efficiency prediction

Fig. 2. Time domain results of PTO input force F_{pto} and output voltage V_{abc} from the bench test and simulation.

Method for Increasing AC-DC Voltage Gain of Three-Phase Critical Conduction Mode Converter

Increasing power density as well as efficiency, has always been the major concern in power electronics technology development. With the use of wide bandgap power semiconductors, operating a capacitive decoupled three-phase converter (shown in Fig. 1) in critical conduction mode, could largely boost converter power density and efficiency. However, due to the decoupled three phases, the ac-dc voltage gain is reduced by at least 15 percent. An example of this is shown in Fig. 1, where a dc-ac converter is shown; the gain is defined as VAN', rms / VDC. Compared to conventional pulse width modulation (PWM) modulated three phase converters, this largely limits the adoption of this type of converter.

This work provides a way for the capacitive coupled three-phase converter to maintain similar ac-dc voltage gain comparable to conventional PWM modulated three-phase converters. A controlled triplen order harmonic current is injected into the decoupling capacitors (Cf in Fig. 1). This induces triplen order harmonic voltage to be superimposed on the fundamental frequency voltage, which allows for increasing ac-dc voltage gain in a similar manner as a space vector modulated three-phase converter. The triplen order harmonics currents in the filter inductor Lf flows entirely through the decoupling capacitors Cf, as shown in Fig. 1. By controlling the triplen order harmonics in Lf, the triplen order harmonic current injected into Cf is directly controlled, and the triplen voltage superimposed on the capacitor fundamental voltage is controlled according to (Eq. 1.).

Eq. 1. $$C_f \frac{dV_{3rd}}{dt} = I_{3rd}$$

With properly superimposed triplen order harmonics, peak capacitor voltage can be reduced to 85 percent of the non-superimposed voltage, as shown in Fig. 2. This allows higher ac-dc gain to be achieved (which may also refer to dc voltage utilization).

A detailed theoretical derivation for this concept can be found in the slides submitted along with this document. Using this technique, the capacitive decoupled three phase converters, which achieve higher power density and efficiency, become good replacements for conventional PWM modulated three-phase converters. The target applications of this type of converter include telecom power supplies, server power supplies, aircraft power supplies, uninterrupted power supplies, motor drives, and other applications where three-phase ac-dc or dc-ac power conversion in kW range is required.

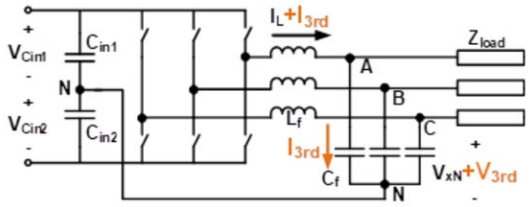


Fig. 1. Converter schematics and triplen harmonics injection concept of a three-phase critical conduction mode dc-ac converter with decoupling capacitors.

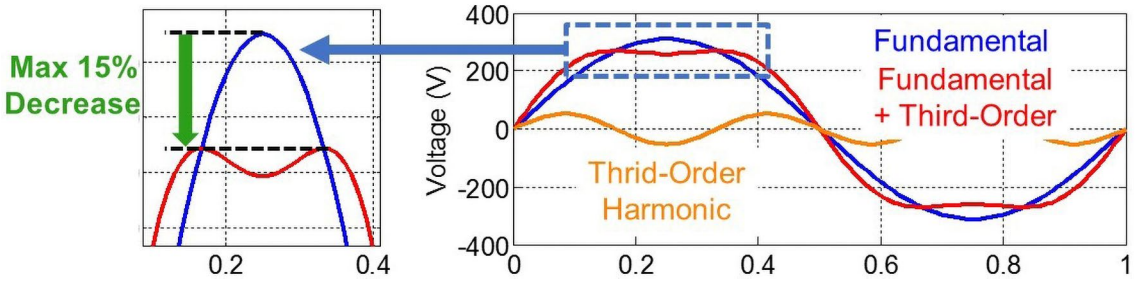


Fig. 2. Capacitor voltage waveforms with and without superimposed triplen order harmonics. With properly superimposed triplen order harmonics, an increase of 15 percent ac-dc voltage gain could be achieved.

A High-Efficiency High-Density Wide-Bandgap Device-Based Bidirectional On-Board Charger

Due to increasing fuel cost and air pollution concerns, plug-in electric vehicles (PEVs), are drawing more and more attention. PEVs have a rechargeable battery that can be restored to full charge by plugging into an external electrical source. However, the commercialization of the PEV is impeded by the demands of a lightweight, compact, yet efficient on-board charger system. Since the state-of-the-art level 2 on-board charger products are largely silicon (Si)-based, they operate at less than 100 kHz switching frequency. This results in a low power density at 3–12 W/in3, as well as an efficiency not more than 92-94 percent. Compared with Si devices, the absence of a reverse recovery charge in wide-bandgap (WBG) devices (gallium nitride (GaN) and SiC) enables bidirectional operation with a single converter. In addition, WBG devices have a much better figure of merit than Si devices. For a given ON-resistance and breakdown voltage, WBG devices require a much smaller die size, which can translate into a smaller gate charge and junction capacitance. Both of these characteristics are able to shorten the current and voltage transition interval, and thus reduce the switching loss. Therefore, by moving to WBG devices, the system switching frequency is increased to 100–300 kHz, and 95–96 percent efficiency is achieved.

For the ac-dc stage, a bridgeless totem-pole converter with critical conduction mode (CRM) operation is adopted. Zero voltage switching (ZVS) is achieved for all fast switches, making it a promising candidate for high-frequency operation. Also, the symmetrical structure guarantees easy bidirectional operation. For the isolated dc/dc stage, the CLLC resonant converter, featuring the same soft-switching technique as the LLC resonant converter, is selected. It achieves ZVS for all switches under all load conditions. In addition, the symmetrical resonant tank makes it much more suitable for bidirectional operation. To optimize the converter over a wide output voltage range, a variable dc-link voltage structure is used utilizing 1.2 kV SiC devices, so that the second stage CLLC resonant converter is always working around its optimized point for all output voltages. As a result, very high efficiency is achieved during the whole charging cycle from low battery voltage to high battery voltage. Also, a two-stage combined control strategy is proposed for both charging and discharging operations. The proposed control guarantees that the dc-dc stage switching frequency stays around resonant frequency and also eliminates the secondary order line-frequency ripple generated by the ac/dc stage. A 6.6 kW, 500 kHz (300 kHz for ac-dc) bidirectional on-board charger prototype with 37 W/in3 power density and higher than 96 percent efficiency is demonstrated to verify the proposed structure.

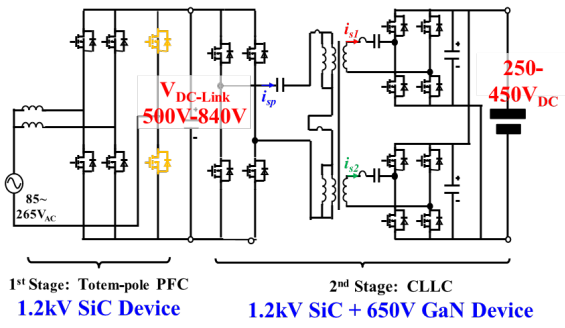


Fig. 1. Variable dc-link voltage structure without split capacitors.

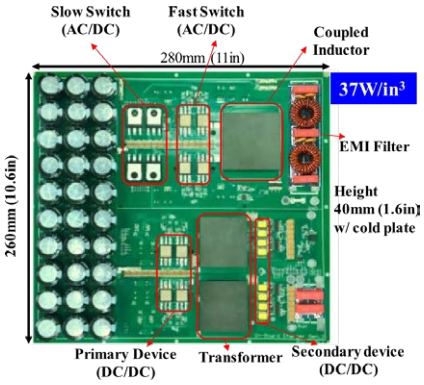


Fig. 2. Hardware prototype.

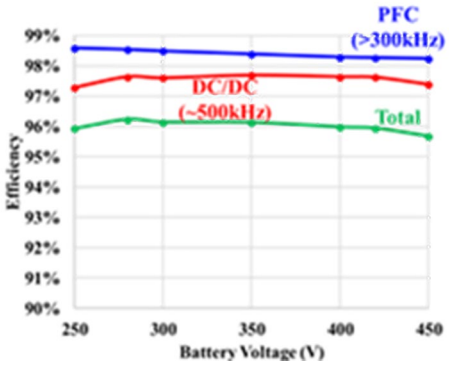


Fig. 3. Tested efficiency.

Electric Field Control in Wide Bandgap Power Electronics Modules Via Geometrical Techniques

Silicon carbide (SiC) and gallium nitride (GaN), which have a relatively large bandgap of 3.3 eV and 3.4 eV, respectively, are the more promising semiconductor materials known as wide bandgap (WBG) semiconductors. This is due to their outstanding properties such as commercial availability of starting material and maturity of the technological processes. WBG semiconductors, which are expected to have better efficiency, higher temperature tolerance, and higher voltage blocking capability than their silicon (Si) counterparts having a bandgap of 1.1 eV, are changing the landscape of the power electronics industry. Moreover, a new class of semiconductor materials called ultrawide-bandgap (UWBG) semiconductors, with bandgaps higher than that of GaN, including currently investigated diamond (C), gallium oxide (Ga_2O_3), and aluminum nitride (AlN), will be the generation-after-next power electronics. However, new packaging technologies are needed to realize the expected superior system performance with WBG and UWBG devices. Among the various factors needing to be addressed for high-density packaging designs of high voltage WBG and UWBG devices, are the high electric fields, especially at the edges of the substrate metallization. These can lead to unacceptable levels of partial discharges in the silicone gel, commonly used as encapsulations. In this paper, geometrical techniques for electric field control inside WBG power electronics modules are studied by finite element method models (FEM), developed in COMSOL Multiphysics.

Fig. 1 shows the geometry considered for modeling in COMSOL Multiphysics. The upper and lower copper metallization thickness is 300 μm which is a common value for ceramic substrates. The following were considered: the relative permittivity values of 8.9 and 2.7 for AlN and silicone gel, respectively; and the voltages of 10 kV addressing the blocking voltage of a WBG device for the upper metal layer, and 0 for the lower metal layers.

As shown in Fig. 1, an offset of the two metallization layers is defined as $r_{off}=r_u-r_l$ for r_u and r_l. Fig. 2 shows the electric field magnitude values at a distance of 20 μm from the edge along the dashed line L1, shown in Fig. 1, for different values of r_{off} for a 630 μm ceramic layer. It is apparent that with decreasing the offset, the electric field magnitude reduces. Stated simply, an increase in the length of the upper metal layer, relieves the worst high field region. This is due to the influence of the grounded based plate; the longer the upper metal layer, the less nonuniform the electric field. Changing r_{off} from 0.35 mm to -0.5 mm reduces the electric field intensity up to 57 percent and becomes an efficient electric field control technique.

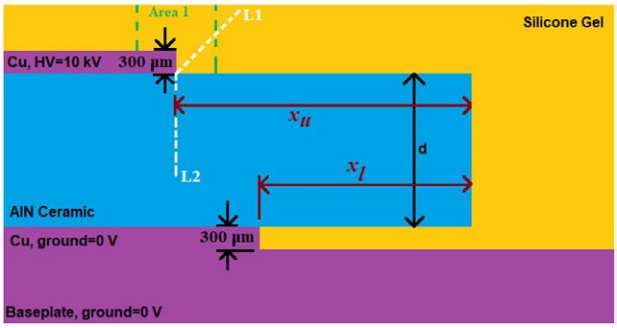


Fig. 1. Geometries considered for simulations.

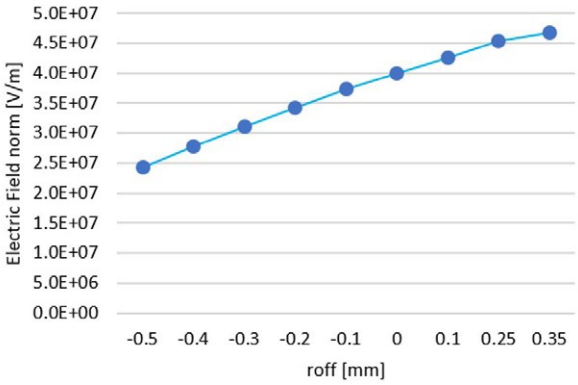


Fig. 2. Influence of r_{off} on electric field intensity.

The Optimal Design of GaN HEMTs Active-Clamp Flyback Converter with Wide-Input Range

Compared with traditional flyback topology, active-clamp flyback (ACF) topology is appealing to universities and industry due to its zero-voltage switching mechanism, relative simplicity, and lower switch voltage stress compared with other topologies used in low-power applications. Fig. 1 shows the schematic circuit of the ACF. This topology is a variant of the flyback converter with the additional active-clamp circuit consisting of an auxiliary switch S_2 and the clamping capacitor C_r. C_r collects the leakage energy stored in the transformer and the primary switches can achieve zero-voltage switching (ZVS), reducing the turn-on swithcing loss. Two methods have been proposed to achieve ZVS. One method runs in the critical conduction mode (CRM); the other runs in the continuous conduction mode (CCM). The former operates with bidirectional magnetizing current, which means that the transformer magnetizing current ripple current is allowed to become negative for a portion of each switching cycle. The main waveforms of hte two operation modes are shown in Fig. 2. The zero-current switching (ZCS) of the output rectifiers is satisfied when the secondary-side current I_s reaches zero before the end of the switching cycle, which is marked in Fig. 2 (a). In the CCM operation, the magnetizing current never reaches zero and there is no ZCS in the output rectifiers, which is illustrated in Fig. 2 (b). The CRM is preferred when the loss in diodes are more dominating compared with the loss in the primary switches. In the case when the losses in the primary switches are dominating, it is more desirable to design the ACF running in CCM operation to restrict the transformer ripple current. The selection between the CRM and the CCM becomes difficult when accompanied with a wide input voltage range, as both the losses of the switches and diodes vary with the change in the input voltage, leading to the difficulty in addressing the optimized point.

Loss simulations with different inductances at different input voltages are done to evaluate the performance of the two operation modes. CCM is selected due to its lower total device and diode loss. Additional capacitors are added in parallel with the rectier diodes to reduce their reverse-recovery loss.

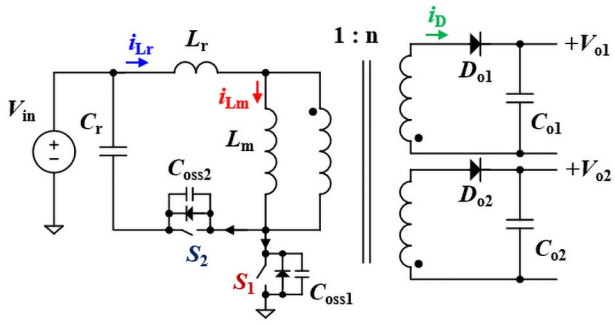


Fig. 1. Dual-output active-clamp flyback converter.

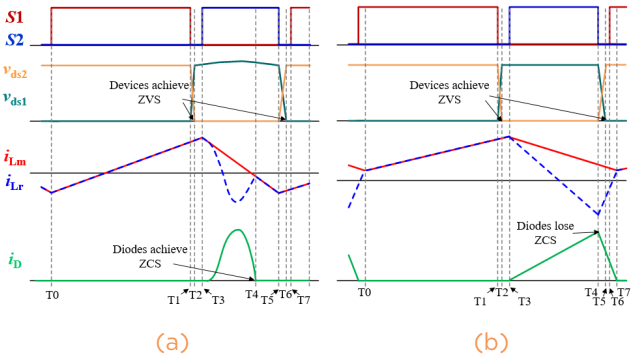


Fig. 2. Main waveforms of (a) the CRM and (b) the CCM in steady state.

Ultralow Input-Output Capacitance PCB-Embedded Dual-Output Gate-Drive Power Supply for 650 V GaN-Based Half-Bridges

With features such as high switching frequency and high blocking voltage, wide-bandgap (WBG) devices, such as silicon carbide (SiC) metal-oxide semiconductor field-effect transistors (MOSFET) and gallium nitride (GaN) high-electron-mobility transistors (HEMTs), are being used more in power converters to boost the efficiency and power density. A key trade-off of these gains is the increasing electromagnetic inference (EMI) noise. To attenuate the EMI noise from the power loop into the auxiliary sources, the isolation capacitance in the isolated gate drive power supply is expected to be as small as possible. In this nugget, a gate drive power supply dedicated to drive two 650 V GaN devices in a phase leg, is presented. It has a PCB-embedded transformer as a substrate, achieving an ultra-low inter-capacitance of 1.6 pF, high efficiency of 83 percent, and high power density of 72 W/in^3. The input of the power supply is 15 V. There are two isolated outputs; each has output voltage of 7 V and output power of 1 W.

To reduce the inter-capacitance (isolation capacitance) from the primary to the secondary side in the transformer, the primary and secondary windings should be located as far away as possible, which increases the volume accordingly. In addition to the above trade-off, efficiency is also a key design variable affected by the power supply volume. The challenge of the work is to find an appropriate design approach, aiming at small converter volume, small inter-capacitance, and high efficiency.

To design the targeted gate driver power supply, the paper first presents the circuit design, followed by the transformer optimization. The PCB-embedded transformer structure is then illustrated in Fig. 1, and the core and PCB material selections are addressed. To find a compromise among a low inter-capacitance, low transformer loss, and a small volume, an optimization of the transformer dimensions is performed, based on the transformer models. With the optimized dimensions, the transformer is built and shown in Fig. 2, and the fabrication procedures, including a standard lamination process, are introduced. The transformer and the converter hardware are shown and characterized with experimental waveforms, efficiency, isolation voltage, inter-capacitance, and total volume.

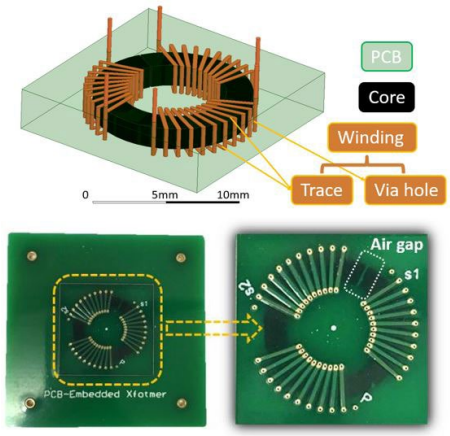


Fig. 1. PCB-embedded transformer structure illustration.

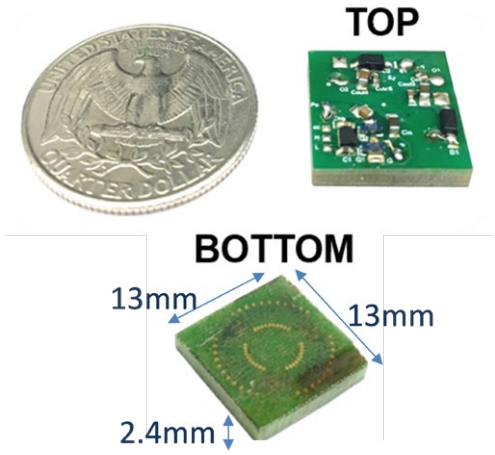


Fig. 2. Active-clamp flyback with the PCB-embedded transformer substrate.

Triangular Current Mode Boost Inductor Optimization Using 2-D Finite Element Analysis and the Improved Generalized Steinmetz Equation

In recent years, the emergence of wide bandgap semiconductors has fueled a renewed push towards faster, more efficient, and higher density power converters. The low turn-off energy of these devices makes them ideal for zero voltage switching (ZVS), and numerous techniques have been developed to take advantage of this fact. However, the performance of a power converter is not determined by switching speeds and efficiency alone. The design for the passive components and filters included in power converters to accommodate these higher switching speeds, is a must for maximum efficiency.

We look specifically at the optimization of the boost inductor in a triangular current mode (TCM) controlled boost inverter. This method of achieving ZVS uses hysteresis control with switching frequencies, ranging from 100s of kHz to around 1 MHz. This, in addition to the high harmonic content of triangular waveforms compared to sinusoidal waveforms, presents a challenging design problem for the boost inductor. While the improved generalized Steinmetz equation (iGSE) can be used to approximate core losses of an inductor, there is no generally used model for winding loss estimates. Instead, finite element analysis (FEA) is often used extensively to verify inductor designs in the early stages. However, 3D models are very costly in computational space and time requirements, and the TCM waveform requires both a small time step and long simulation time to accurately capture both the relatively fast switching frequency and slow fundamental.

Therefore, a 2D model of two similar core types is created and used for optimization of the boost inductor. Some points of optimization were neglected—namely in core dimensions—to avoid the need for custom core orders. Based on the results of the 2D FEA simulation models using ER and EI core types, commercially available cores were selected close to the optimal point and tested. The power loss from these tests and the simulation were compared for both cores to see how different geometries perform in 2D FEA vs. reality.

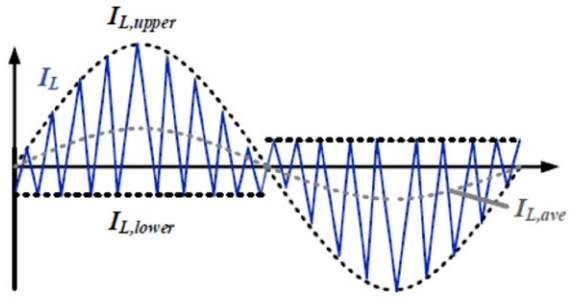


Fig. 1. Inductor current waveform of TCM boost inverter.

Qiong, W.; Turriate, V.; Burgos, R.; Boroyevich, D.; Sagona, J.; Kheraluwala, M., "Towards a high performance motor drive for aerospace applications: Topology evaluation, converter optimization and hardware verification," in IEEE Industrial Electronics Society, 2017. IE-CON'17., vol.1, no., pp.1622-1628 vol.1, Oct. 29 - Nov. 1, 2017

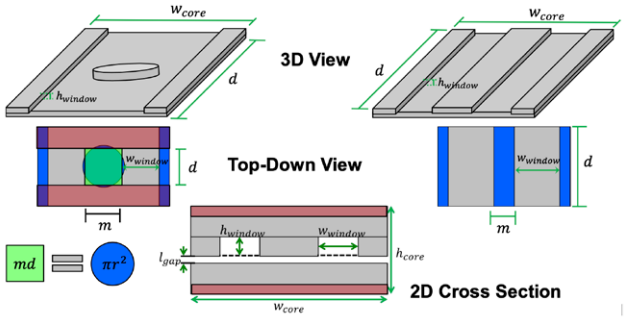


Fig. 2. 2D FEA modeling of ER (left) and EI (right) cores.

High-Frequency Transformer Design for Modular Power Conversion from Medium-Voltage AC to 400 V DC

As a result of the increasing use of cloud computing and big data, the power consumption of the data center alone, will reach 10 percent of the total electrical power consumption in the world by the year 2020. Considering such a booming data center load development, high copper cost and conduction loss, due to low voltage (480 VAC) power distribution outside the server hall, needs to be solved.

In the proposed system, medium-voltage ac is used as the distribution voltage in the data center, and the proposed power conditioning system block (PCSB), is used to convert medium-voltage ac directly to 400 V dc inside each server hall. This system can eliminate line frequency bulky transformers, reduce front end conduction cable costs, and save conduction loss. The proposed high-frequency modular medium-voltage ac, (4160 V ac and 13.8 kV ac), to low-voltage dc, (400 V dc) PCSB, is shown in Fig. 1. Each system block consists of ac-dc H-bridge converters, together with high-frequency isolated dc-dc converters. A total of five cascaded PCSBs are employed to convert 4160 V ac directly into 400 V dc. The inputs of the ac-dc H-bridges are in series, and the outputs of the dc-dc stages are connected in parallel.

In this work, a high-frequency isolated CLLC resonant converter is proposed for a next generation DC data center. The medium-voltage high-frequency transformer is the most crucial component in terms of insulation and power density. A novel UU core with a sectionalized winding structure is chosen to enhance insulation capability, restrict leakage inductance, and reduce magnetic loss. Transformer insulation parameters are calculated based on the IEEE standard requirements. The transformer turns number is determined based on the transformer loss and volume tradeoff. Different working frequency impacts on transformer design are also analyzed based on a similar method; 400 kHz is found to be the best working frequency for 3F36 material. Various material's optimal working frequency is also different. A 15 kW/500 kHz transformer prototype is developed, as shown in Fig. 2. The transformer is tested to pass three insulation tests according to the IEEE Std. C57.12.01 standard. Based on the transformer prototype, a 15 kW 500 kHz CLLC resonant converter is built. Experiment results of 98 percent peak efficiency and 2.9 kW/L power density are presented.

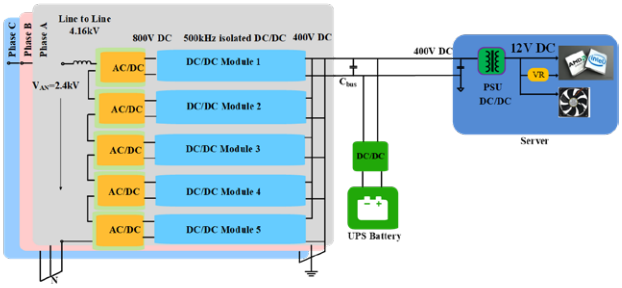


Fig. 1. Proposed medium voltage to 400 V dc PCSB for dc data center.

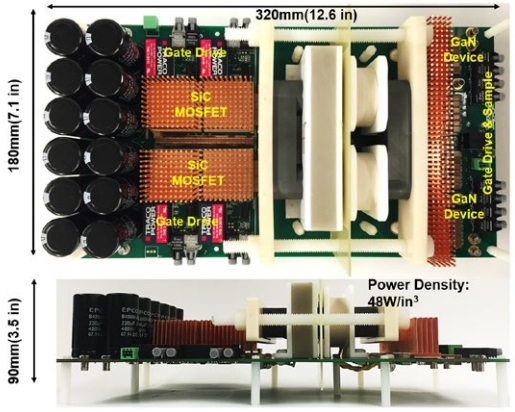


Fig. 2. 500 kHz 15 kW CLLC resonant converter prototype hardware.

UV-Curable Ferrite Paste for Additive Manufacturing of Power Magnetics

Magnetic components are necessary elements in power electronics converters for storing and converting energies, but they are often the bulkiest. Novel structures of magnetic components can be designed, but making them is difficult using current available materials and fabrication processes. Additive manufacturing (AM) has the potential to instigate a paradigm shift in how power magnetics are designed and made. Among the many 3D-printing platforms, the direct-extrusion type can print multiple materials into a single structure. This capability enables one-step shaping of a whole magnetic component; in other words, core, winding, and/or dielectric insulation, together. However, it was recently reported that magnetic paste feedstock for extrusion-based AM suffered from a "slumping" problem and, therefore, was not suitable for building tall core structures. In this study, a NiZn ferrite paste feedstock is formulated that develops deformation resistance under UV illumination.

Deformation resistance of an ink or paste feedstock is usually characterized by its complex shear modulus, both the storage and loss modulus, as a function of shear stress. For a paste feedstock to resist deformation after deposition (or called "solidified"), it usually has a storage modulus higher than 3 x 10^4 Pa, and a yield stress (crossover between the storage and loss moduli) higher than 60 Pa. Shown in Fig. 1 are the modulus plots of the UV-cured pastes with different solid loadings after 1 minute and 1.5 minutes UV curing time, respectively. 94 and 95 percent pastes solidified after only 1 minute illumination; 95 percent had to be illuminated for 1.5 minutes; 97 and 98 percent pastes may need more than 1.5 minutes illumination to solidify.

To demonstrate the feasibility of 3D-printing tall core structures using UV-curable ferrite paste, 6 mm-tall toroid cores and 5 mm-tall E cores were made using the UV-assisted 3D printer. Shown in Fig. 2 (a) to (d) are the as-printed parts. The structures shown in Fig. 2 (a) and (b) were made without UV exposure. As expected, the parts slumped and kept slumping with time. The structures in Fig. 2 (c) and (d) were made with UV exposure for 1.5 minutes and 1 minute, respectively. After the UV-cured structures were formed in the printer, they were heated to 1,000° C to remove all organic compounds and sinter. The sintered toroid core (Fig. 2 (e)) and E core (Fig. 2 (f)) had no cracks or warpage. The pictured cores were as-sintered without any polish.

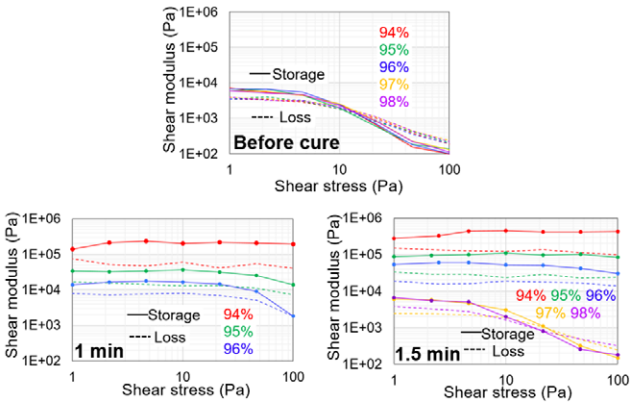


Fig. 1. Complex shear moduli versus shear stress of as-prepared pastes, pastes after 1 minute UV illumination, and pastes after 1.5 minutes UV illumination.

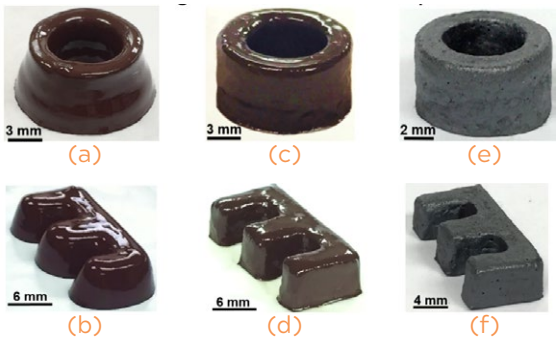


Fig. 2. 3D-printed cores (a-b) without UV illumination, (c) made with 96 percent paste with 1.5 minutes UV illumination after each layer, (d) made with 95 percent paste with 1 minute UV illumination after each layer, and (e-f) after sintering at 1,000° C for 2 hours.

Analytical Models for Superjunction Power Transistors with Interface Charges

Achieving high breakdown voltage with low specific-on resistance is one of the main objectives for power devices. Vertical superjunction devices could break the theoretical limit of unipolar power devices, by allowing linear design dependence of specificon resistance with breakdown voltage. Si superjunction devices have achieved huge commercial success. The presence of interface charges at the regrown surface is a key roadblock for experimental realization of GaN superjunction devices. However, analytical modeling for superjunctions with interface charges remains undone. This work studies the numerical model for superjunctions with interface charges, including GaN superjunctions as a case study. The specific-on resistance vs. breakdown voltage relationship is assessed together with the optimizing strategy for doping and geometry.

The interface charge that exists between n-pillar and p-pillar is shown in Fig.1. The existence of an interface charge will affect the charge equilibrium and electric field continuity on the interface, thus affecting the depletion width inside n-pillar. Since on-state current only flows in n-pillar, the minimum depletion width will give maximum conductivity. This means on resistance R_{on} is a function of the interface charge. Another crucial parameter is the breakdown voltage V_B. At breakdown, the lateral electric field amplitude is dependent on interface charge. Assuming the total critical electric field is constant, then the vertical electric field at breakdown will also be affected by interface charge. This vertical electric field will directly contribute to the breakdown voltage. Both the analytical equations are given for specific-on resistance $R_{on,sp}$ and breakdown voltage V_B. The figure of merit, $R_{on,sp}/V_B$, can be deduced and its minimum point can be achieved by optimizing doping concentration N_D and n-pillar width w_n, as shown in Fig. 2. The material properties of GaN are considered in this model for design optimization, and are compared with the no-interface charge case. The optimized result shows similar behavior compared with no-interface charge results. In fact, the difference is almost negligible when the width is not too small (>1 μm). All of them show advantage over unipolar devices at high voltage (>1000 V).

In conclusion, this work provides the first analytical model for understanding superjunction devices with interface charges. The case study of GaN superjunctions reveals promising features of vertical GaN superjunction devices. Though not as ideal as no-interface charge cases, problems can be greatly compensated for by optimizing doping concentration and pillar width. This work will remove the roadblocks of experimental demonstration of vertical GaN superjunctions.

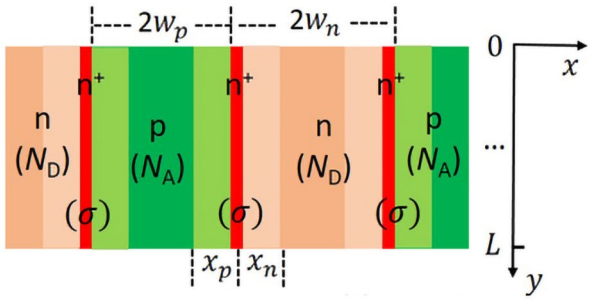


Fig. 1. Schematics of superjunction with interface charges.

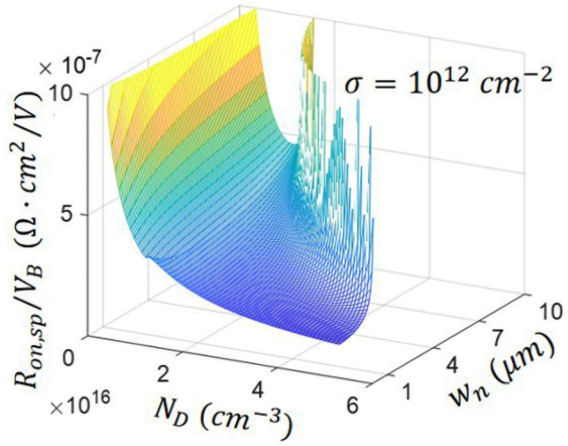


Fig. 2. Optimization of $R_{on,sp}/V_B$ for variable doping concentration and width.

Phase Current Sensor and Short-Circuit Detection Based on Rogowski Coils Integrated on Gate Driver for 1.2 kV SiC MOSFET Half-Bridge Module

The necessity of having a new, fast, and reliable short-circuit protection method for SiC applications, and the emergence of high density, high efficiency trends, drove the introduction of the gate driver (GD) with an integrated Rogowski switch-current sensor (RSCS). In the newly designed GD, switch currents are measured and used for protection, while the same information is used for obtaining the phase current with a simple manipulation on the GD itself (shown on Fig. 1). Outputting the phase current from the GD is possible by knowing the switch currents in the complete switching cycle and simply subtracting these two currents.

The chosen GD architecture is one where an RSCS for the top and bottom device is placed on the controller (common) ground. A digital reconstruction of the phase current is chosen, as shown in Fig. 2. The di/dt information, scaled with a factor of mutual inductance, is being constantly integrated by an active integrator. The output voltage of an integrator linearly represents current in the system. After the buffer, there is a two-stage analog-to-digital converter (ADC) filter with a cutoff frequency of 3.3 MHz. Its main role is to filter out any high frequency ringing in the current information during switching instances. The OpAmp level shifter is employed to adjust the signal to the proper values for ADC sampling. The chosen sample rate of the ADC is 2.5 MHz in order to reduce delay of the current measurement. Two ADCs for the top and bottom switch currents are synchronized and send data in the field-programmable gate array (FPGA) at the same time instances. Immediately after successful subtraction, the FPGA starts placing that information on the digital-to-analog converter (DAC). A 2.5 Msps DAC with a small settling time, is chosen to convert information back to analog, without minimizing delay.

The gate driver is able to successfully reconstruct the phase current under a dv/dt of 15 V/ns. The delay between the reconstructed phase current and the current in the system is 1.61 µs. The absolute error of the RSCS for both high and low currents is a maximum of 3 A for frequencies above 10 kHz. This is promising for applications with intended switching frequencies above 10 kHz and are within the silicon carbide (SiC) MOSFET domain. The recon-struction error is a maximum of 3 A for both high and low currents. The linearity error is 2.5 percent. A fast detection time of 80 ns for short-circuit events, and a reaction time of 200 ns are achieved; both limit overheating and stresses in the module. The total time spent in protecting the short-circuit is around 1.2 µs, minimizing overshoot and thermal stresses.

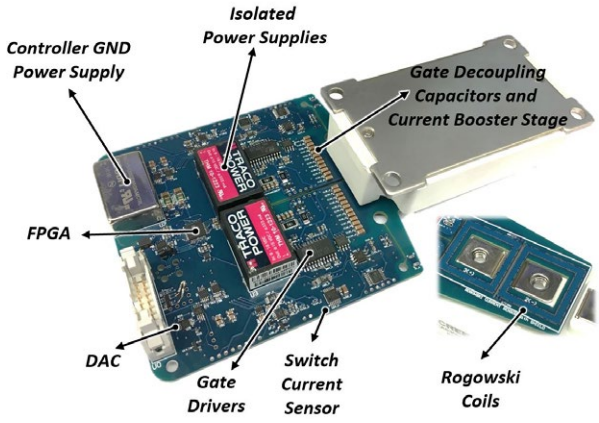


Fig. 1. Gate driver prototype.

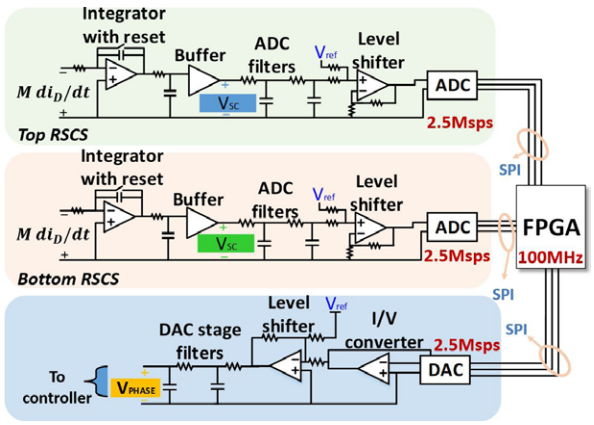


Fig. 2. Digital phase current reconstruction principle.

Phase Current Reconstruction Based on Rogowski Coils Integrated on Gate Driver of SiC MOSFET Half-Bridge Module for Continuous and Discontinuous PWM Inverter Applications

Silicon carbide (SiC) MOSFET power devices are becoming global solutions in applica-tions such as inverters, due to their fast switching speed, low on-state resistance, and high working temperature, making them a replacement for conventional Si solutions. In the past, and out of necessity, a fast and reliable short-circuit (SC) protection method for SIC MOSFET devices was introduced and developed, which consisted of a PCB-embedded Rogowski switch current sensor (RSCS) integrated on the gate driver (GD). To increase power density and reduce cost and weight, other sensors, such as a Hall sensor, can possibly be substituted in SiC applications, and use the developed RSCSs to generate phase current on the GD.

Outputting the phase current from the GD is possible by knowing the switch currents in the complete switching cycle and simply subtracting them. In order to subtract information be-tween two currents in some types of digital signal processors, two analog-to-digital converters are employed. A field programmable gate array (FPGA) is used for digital subtraction. A digital-to-analog converter is necessary to convert phase current information back to analog. Phase current information from the GD for a continuous pulse width modulation (CPWM) inverter can be sent back to the main controller for control purposes. This is shown in Fig. 1. Furthermore, the reconstructed waveform is compared with the commercially measured one and has a minimal delay of 1.6 μs, an error less than 3 A, and a linearity error of 2.5 percent.

During clamped periods of discontinuous pulse width modulation (DPWM), the developed sensor will be inaccurate due to a severe integration error. This is because there is no reset signal. The problem of the inaccurate phase current during the clamped period can be overcome on the controller level. The sum of the currents in each instance is zero in motor control applications, indicating that one of the phases can be calculated as the negative sum of the currents in the two other phases. According to DPWM fundamentals, while one phase is clamped, the other two will be switching, signifying that the current coming from their GD is valid. Based on that, whenever one phase is clamped, current in that phase can be extracted from the other two phases on the controller, as shown in Fig. 2. This simple manipulation makes the on-board phase current sensor valid for both CPWM and DPWM.

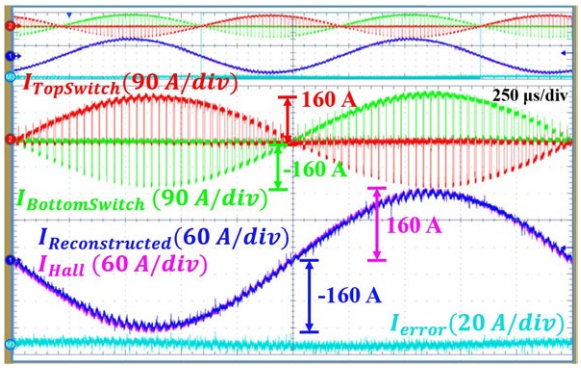


Fig. 1. Sensor performance during continuous PWM.

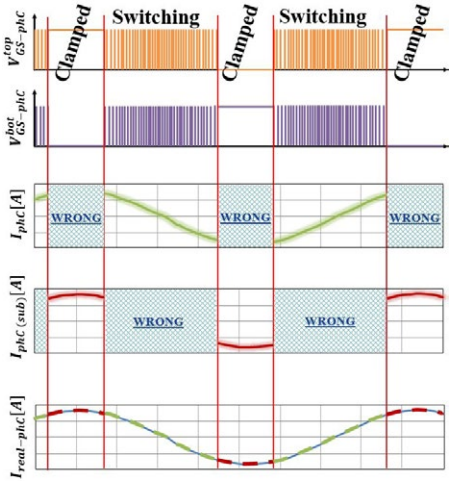


Fig. 2. Sensor performance during discontinuous PWM.

SiC MOSFET Characterization and Reliability at 300° C

Silicon carbide (SiC) MOSFETs are wide bandgap devices capable of achieving higher voltage and higher temperature operation, compared to their silicon IGBT counterparts. This is due to their high electric breakdown field and high thermal conductivity. In theory, high-temperature operation is feasible; however, the industry is limited by several factors. Those factors include the temperature rating for the packaging, as well as the MOSFET gate oxide instability at higher temperatures. Standard TO-247 packages for SiC MOSFETs are typically only rated to around 150-175°C maximum junction temperature. Even though SiC is mechanically stable up to extremely high temperatures, the SiC/SiO_2 interface mismatch at the MOS layer causes undesirable shifts of electrical properties at higher temperatures for SiC MOSFETs. To ensure reliability and operation of SiC MOSFETs at extremely high temperatures, there are two major steps to be addressed. Firstly, the package of the device must be able to withstand the heat and be reliable. Secondly, the electrical characteristics of the SiC MOSFET must not vary significantly from nominal datasheet values at said temperatures. This work focuses mainly on the latter point.

To determine the extent of the shift in electrical properties in SiC at junction temperatures of 300°C, standard 1.2 kV, 36 A SiC MOSFETs in TO-247 packaging are taken to 300°C, where the static electrical characteristics were analyzed. To detect any abnormalities in SiC MOSFETs due to a package or device failure, two main points are analyzed: threshold voltage, V_{th}, and on-resistance, $R_{DS(ON)}$. Other characteristics measured include the output characteristic, reverse output characteristic, transfer curve, avalanche breakdown voltage, and gate leakage current measurements. Outside of abnormalities, the expected behavior in V_{th} and $R_{DS(ON)}$ with increasing temperature are a gradual shift downwards and upwards, respectively. Although the exact reason of the threshold voltage shift is unknown, it is suspected to be the temperature-dependent introduction of hole traps within the gate oxide layer. $R_{DS(ON)}$ increases due to the drift layer's resistance being strongly proportional with increasing temperature, due to the electron mobility decreasing. As shown in Fig. 1, SiC MOSFETs perform as expected up to 300°C without any package or device failure under short-term conditions.

Reliability must also be tested for the same devices under similar temperatures. Industry standards for testing for MOSFET reliability include stressing the device and stressing the package—as shown in Fig. 2. To ensure that current generation SiC MOSFETs are suitable for reliable 300°C operation, high temperature gate bias (HTGB) and high temperature reverse bias (HTRB) tests are chosen.

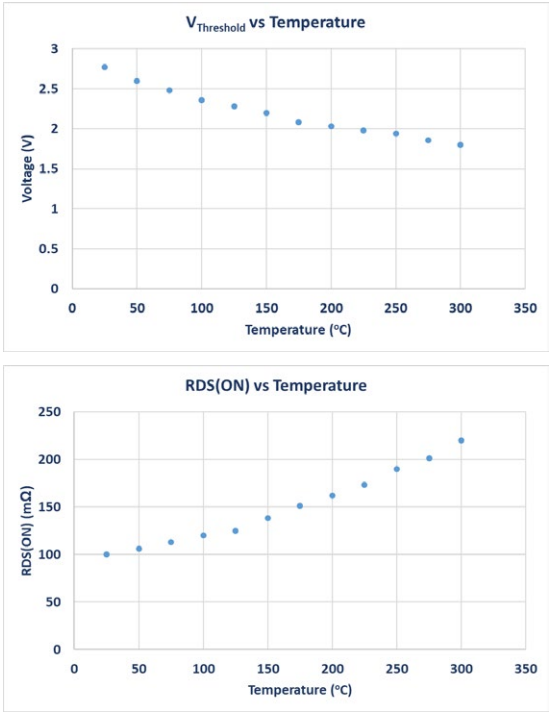


Fig. 1. V_{th} (top) and $R_{DS(ON)}$ (bottom) behavior with increasing temperature.

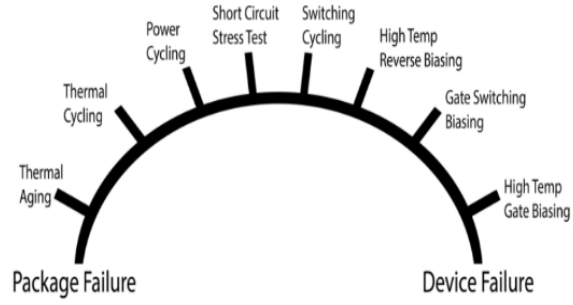


Fig. 2. Summary of reliability testing methods.

Kozak, Joseph, P, et al. "Impact of Accelerated Stress-Tests on SiC MOSFET Precursor Parameters." 3DPEIM, June 2018.

Single Pulse Common-Mode Voltage PWM Scheme to Achieve High Power Density for Full-SiC Three-Level Uninterruptible Power Supply

Superior loss characteristics of wide-bandgap (WBG) devices are improving both the power density and efficiency of power electronics. As shown in Fig. 1, uninterruptible power supplies (UPSs), are one of the applications that may highly benefit from the low-loss charac-teristic of silicon carbide (SiC) MOSFETs. A double conversion efficiency can be as high as 98 percent, while the power density of the power electronics system can be significantly im-proved, compared to silicon (Si)-based UPSs.

An increase in switching frequency brings a change in the contributions of passive components on total volume. Firstly, the portion of EMI filters on the total volume increases, especially the common-mode (CM) part. Secondly, the contribution of dc-link capacitors may increase in the three-level topologies, since the size of these capacitors is not relevant to the switching frequency.

A pulse-width modulation (PWM) scheme for the three-level full-SiC UPSs was developed to achieve a high power density. Two key passive components were selected for size reduction of the full-SiC UPS: a CM EMI filter and dc-link capacitors. To reduce the CM noise and perform neutral point voltage balancing, LMZ, MMS1, and MMS2 vector combinations were proposed based on a synchronous switching of the three phases. As shown in Fig. 2. The proposed combinations align CM voltage (CMV) to be a single pulse per a switching period. In this way, CMV cancellation between a three-level rectifier and inverter in the CM equivalent circuit, shown in Fig. 1 (b), can be maximally utilized, while a drift of neutral point voltage can be prevented by a transition among the three combinations. Secondly, to reduce the dc-link capacitors, a simple algorithm to compensate neutral point voltage (NPV) fluctuation was proposed. When the small film capacitors are used for the dc-link, the fluctuation of NPV creates a low-frequency distortion on the output current. The amount of the distortion can be more severe in a case of full-SiC multi-level inverters, compared to Si-IGBT based ones. Such a distortion can be easily compensated by modifying the carrier slope. The synchronous switching to reduce CMV can be maintained by a correction on the zero-sequence voltage. The proposed PWM scheme was verified with a 20 kW full-SiC UPS.

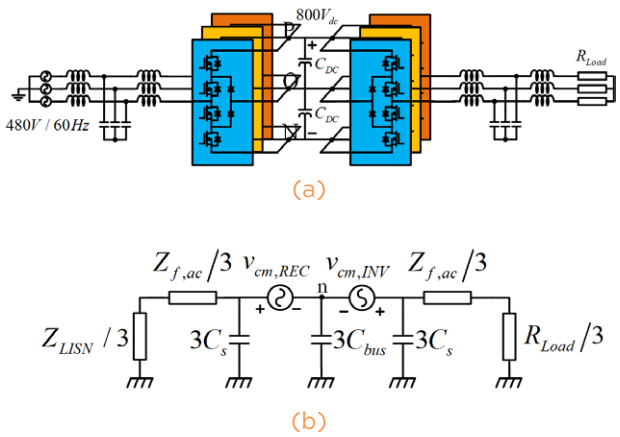


Fig. 1. (a) An ac-ac stage circuit diagram of full-SiC three-level UPS and (b) a common-mode equivalent model.

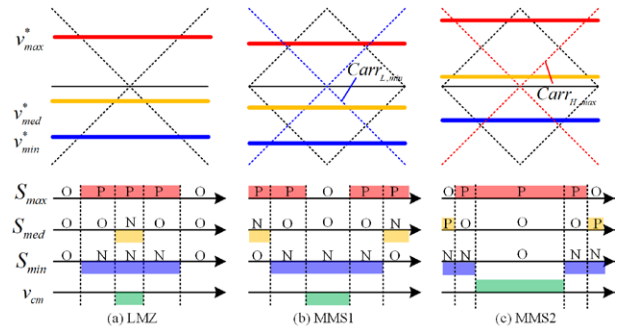


Fig. 2. Carrier-based implementation for LMZ and MMS vector combinations.

Design Comparison of Three-Level, Three-Phase Photovoltaic Inverter Operating in Continuous Conduction Mode and Triangular Conduction Mode

For photovoltaic (PV) applications, it is possible for three-phase inverters to interface a grid without a transformer. To limit a leakage current through the parasitic capacitance of PV panels, three-level topologies have been widely adopted, as shown in Fig. 1. In cases of power converter based wide bandgap (WBG) devices, switching-loss is reported to be concentrated on turn-on instants. To increase switching frequency, thus power density, zero-voltage switching (ZVS) schemes are widely investigated. Through ZVS, the switching frequency of the silicon carbide (SiC) three-phase inverter can reach a few hundreds of kHz with an efficiency >98.5 percent, which leads to a significant increase in power density.

In this paper, a detailed comparison in hardware design for a full-SiC 3-level inverter, operating in continuous conduction-mode (CCM) and triangular conduction-mode (TCM). With an identical full-SiC three-level phase leg, the switching frequencies for two cases were designed to achieve 99 percent efficiency. To achieve 40 kW output with full-SiC three-level phase-legs, two 20 kW channels are paralleled in the CCM case and three for the TCM case. With the designed switching frequency, a design guideline for an LCL filter of a three-phase TCM inverter was presented. Design criteria for each component of the LCL filter, and common-mode choke to block zero-sequence circulating current, were proposed. An analytic solution to calculate core-loss of the inductors with three-phase TCM operation was revealed. An optimization procedure for the LCL filter and CM choke of the TCM inverter was performed, based on the loss model. The final LCL filter design was compared between the CCM inverter and TCM inverter, as shown in Fig. 2. The benefit on EMI was also compared in the CCM inverter case.

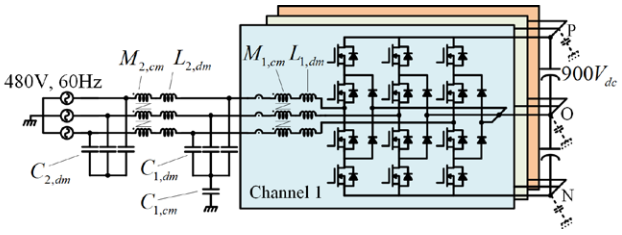


Fig. 1. Paralleled three-phase three-level inverters for PV application.

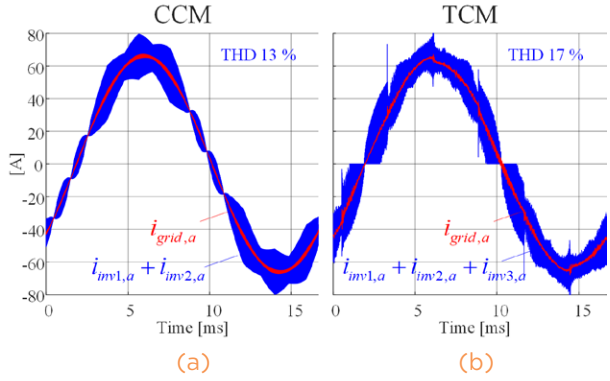


Fig. 2. Simulation waveform showing the summation of phase-A current for paralleled inverters and grid-side current in cases (a) CCM and (b) TCM.

Decoupled Modeling of Three-Phase TCM Inverters Utilizing Three Different Conduction-Modes for ZVS Operation

To improve the power density of ac-dc converters, zero-voltage switching (ZVS) schemes have been widely investigated. Triangular conduction-mode (TCM) delays turn-off time to generate reverse current. The reverse current discharges the junction capacitance before a MOSFET turns on, thus achieving ZVS. This method has been extended to three-phase applications by operating the other two phases with two different conduction-modes: discontin-uous conduction-mode (DCM) and clamp-mode which is similar to a discontinuous pulse-width modulation (DPWM) scheme. The variation of the switching frequency is narrow, while the switching frequency can go up to hundreds of kHz with an efficiency near 99 percent.

However, the presence of three-phase coupling, and transitions of the conduction-modes along the line-cycle introduce complexity in the modeling and control. While one phase is clamped to negative or positive dc-rail, the other two phases operate as two dc-dc buck converters in TCM and DCM within a switching period. The principle of TCM and DCM highly depends on the current slope, and through three-phase coupling, the operation of one phase affects the slope and trajectory of the other phase's current. This complicates the operation.

A decoupled modeling approach is proposed for the three-phase TCM inverters utilizing three different conduction-modes for ZVS operation. If DCM-phase current goes back to zero before the zero-crossing of clamp phase current, the switching frequency is irrelevant to the operation of DCM phase. It is only determined by TCM phase and clamp phase. Under such a condition, the current waveform can be decomposed into two equivalent single-phase TCM and DCM inverters. The current waveform of the three-phase coupled case, shown in Fig. 1 (a), is a superposition of the two single-phase inverter waveforms, shown in Fig. 2 (b). By this simplification, the behavior of the circuit can be easily interpreted, and techniques for a single-phase TCM inverter can be directly applied to the three-phase TCM inverter. The proposed modeling has been verified through Simplis simulation. Analytic solutions of small-signal gains for average current along 30° are compared with the simulation result in Fig. 2, as an example.

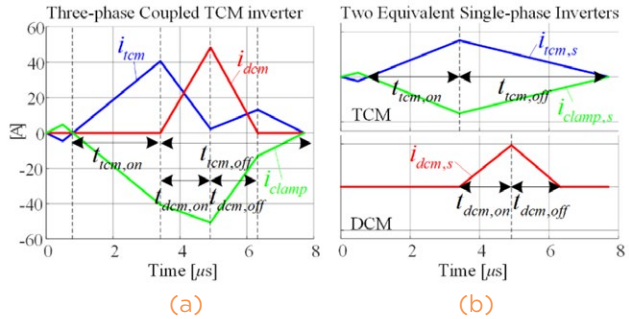


Fig. 1. Decomposition of current waveforms (a) by three-phase TCM inverter and (b) by two equivalent single-phase inverters.

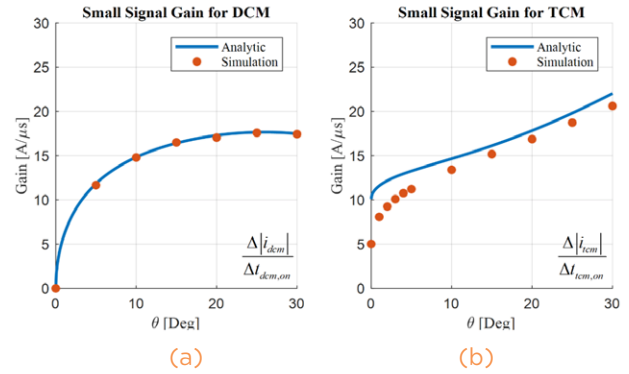


Fig. 2. Comparison of modeling and simulation results showing variation of small signal gain for (a) DCM phase and (b) TCM phase.

A Simplified Digital Closed-Loop Current Control of Three-Phase PV Inverter Operating in Triangular Conduction Mode

The adoption of a silicon carbide (SiC) device brings performance benefits to three-phase photovoltaic (PV) inverters. Since the switching loss of SiC devices is concentrated at a turn-on instant, triangular conduction mode (TCM) can be utilized to achieve zero-voltage switching (ZVS) for SiC-MOSFETs, thus minimizing the switching energy.

TCM modulation is used mostly in single-phase applications. When three-phases are coupled through a neutral point of the load to maximize MI range, the dynamics of the three-phases current interact with each other. Such a coupling makes it hard to apply the conventional current-control methods based on single-phase TCM inverters. In literature, a modulation scheme that combines three conduction-modes was proposed for ZVS operation, namely TCM, discontinuous conduction-modes, and clamping similar to discontinuous pulse width modulation (DPWM). However, the control aspect of this modulation was not investigated in detail.

In this paper, a simple digital scheme for a closed-loop current control is proposed for a three-phase inverter operating in TCM. A simple conduction-mode decision method is presented, based on the three-phase symmetry. A new reference domain based on the conduction-modes is proposed to simplify the closed-loop current control. Three hurdles are identified, namely the tracking of ramp-shaped reference, mode-transition every 30°, and variation of small-signal gain along the line-cycle. An architecture for the closed-loop controller is proposed to overcome these hurdles. The proposed closed-loop control is implemented with a control board with TMS320F28343 and a complex programmable logic device (CPLD). The tracking performance on the current reference in the proposed reference domain, is experimentally verified with a 30 kW three-phase three-level inverter, as shown in Fig. 1.

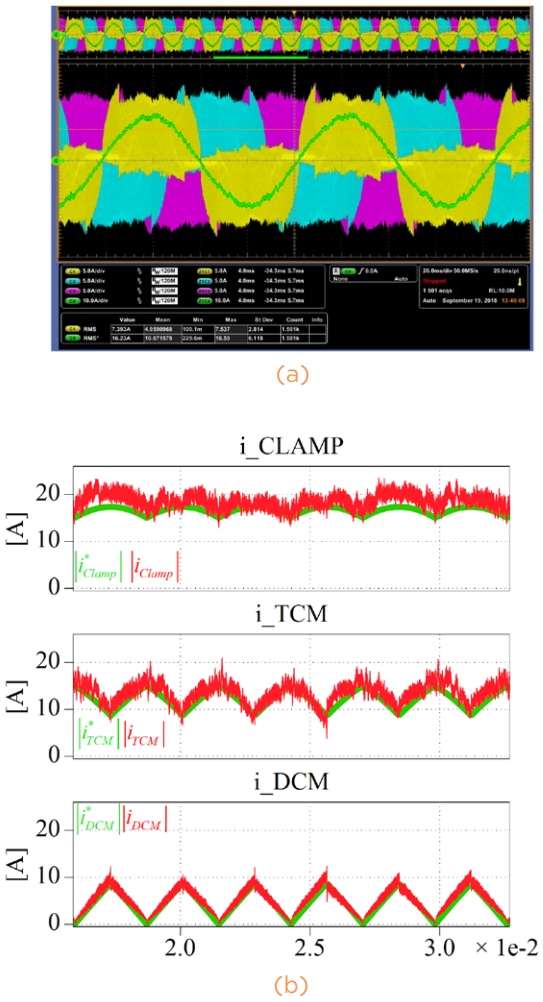


Fig. 1. Tracking performance of proposed current control scheme (a) time-domain waveforms and (b) tracking performance on the proposed reference frame.

Design of 20 kW Full-SiC, Three-Level Three-Phase Uninterruptible Power Supply

An uninterruptible power supply (UPS) is an application in which low conduction loss and switching loss from silicon carbide (SiC) devices, can largely improve the system efficiency. UPSs comprise multiple power-conversion stages and an energy storage. Due to the superior loss characteristic of SiC devices, the efficiency of a single stage can be up to 99 percent, which leads to 98 percent double conversion efficiency. With high efficiency, the operation costs of a UPS can be reduced. Also, the increase in the switching frequency leads to higher power density.

In this paper, the design and implementation for a high efficiency 20 kW, 480 V_{ac}, 800 V_{dc} full-SiC based UPS is presented. Loss of commercial 2-level and 3-level modules are compared, based on the datasheet values. Based on the result, a 3-level NPC topology was selected, which showed higher efficiency for a high switching frequency range over 30 kHz, compared to a 2-level case. A gate driver was designed for the NPC module. A double-pulse test was conducted to extract switching-loss with the designed gate driver. Maximum dv/dt is 26.4 V/ns, while di/dt is 4.14 A/ns when an extrernal gate resistor is 0.05 Ω. Based on the experimental switching-loss data, efficiency simulation was performed. Since the on-drop of the MOSFETs and neutral point clamping diodes are highly dependent on the junction temperature, a lumped parameter thermal simulation was performed to estimate the temperature rise. With a given heatsink and fan design, the junction temperature of the rectifier-side heatsink reaches 65°C, while the inverter side reaches 81°C at switching frequency of 60 kHz. An LCL filter was designed to meet a THD requirement, while the loss and power-density are optimized.

A prototype full-SiC 3-level UPS was built and shown in Fig. 1. The size of the assembly is 280 mm x 254 mm x 178 mm. A thermal rise of heatsink is measured with a thermal camera when it reached the equilibrium. In the experiment, the highest temperature on the inverter-side heatsink is measured to be 71°C. The temperature of the LCL filter is measured, and with small core-loss of nanocrystalline, the temperature of the converter-side inductor is measured to be lower than 55°C. An efficiency curve was extracted from 30 percent load to 100 percent load and shown in Fig. 2. It is compared with the Si-insulated gate bipolar transistor (IGBT) solution and the Si and SiC hybrid solution, which also are comprised of 3-level phase legs and have similar power ratings. It can be seen that the full-SiC prototype could achieve 1 percent increase in the double conversion efficiency at the full load.

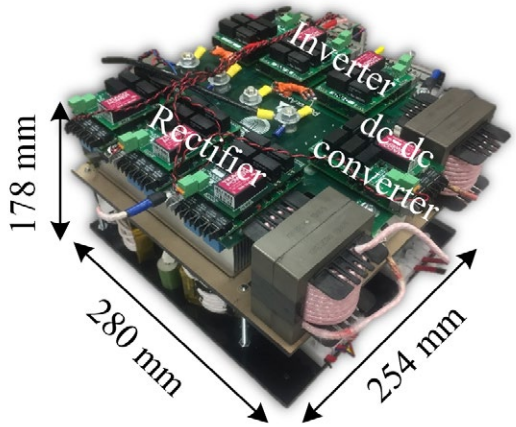


Fig. 1. Prototype full-SiC 20 kW UPS.

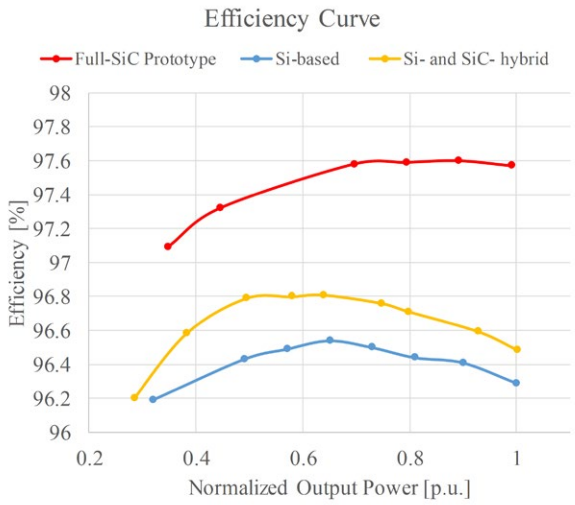


Fig. 2. Efficiency comparison with Si-based or Si- and SiC hybrid three-level UPSs.

Voltage Balancing of Series-Connected Silicon Carbide MOSFET Modules using Active DV/DT Control

Silicon carbide (SiC) MOSFET devices are gradually supplanting Silicon (Si) insulated gate bipolar transistors (IGBTs). This is due to their ability to operate at higher switching frequencies and higher voltages, and with higher thermal conductivity. Due to these advantages, it is worthwhile to study the use of SiC MOSFETs in the design of higher-power systems. By stacking SiC MOSFETs in series, converters can achieve even higher blocking voltages. Additionally, two-level switching topologies are of interest due to less complex circuitry, higher density, and simpler control techniques, when compared to conventional multilevel topologies, which typically requrie additional flying capacitors or isolated voltage sources. The main challenge of stacking devices in series is unbalanced voltages across devices, which can be caused by tolerance in device parameters, package and layout parasitic componenets, and gate signal timing delays.

To compensate unbalanced voltages across stacked switches, active dv/dt control can be used with feedback control of each device's drain-to-source voltage (V_{DS}), as shown in Fig. 1. Compared to other voltage balancing methods, active dv/dt control is preferable due to its small footprint and low losses. In Fig. 1, Q_1 through Q_4 constitute a bipolar junction transistor (BJT) current mirror network that controls the direction of the current generated by the external Miller capacitor C_M. The capacitor C_M induces a current at the drain of each device, based on the dv/dt at each drain. This induced current is distributed through the BJT network in Fig. 1. The magnitude of the voltage signal V_{CTRL} determines the magnitude of the Miller current directed to the device gate and the speed of the device at turn-off. The BJT device Q_5 acts as a freewheeling loop for the induced current to circulate and discharge C_M during each turn-on transition.

In this paper, the development of a stacked switch with active dv/dt control is detailed. Experimental results for closed-loop voltage balancing of four stacked SiC MOSFETs are evaluated, as shown in Fig. 2. Finally, scalability considerations when stacking more devices in series are discussed.

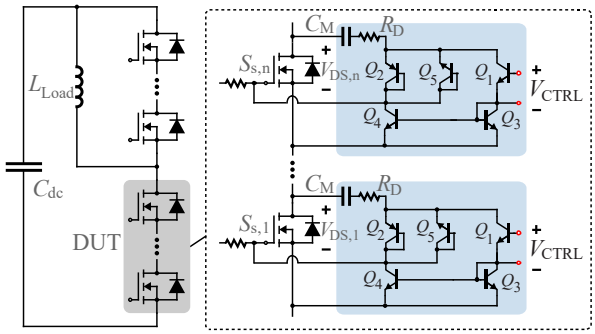


Fig. 1. Active dv/dt controller for stacked SiC MOSFETs.

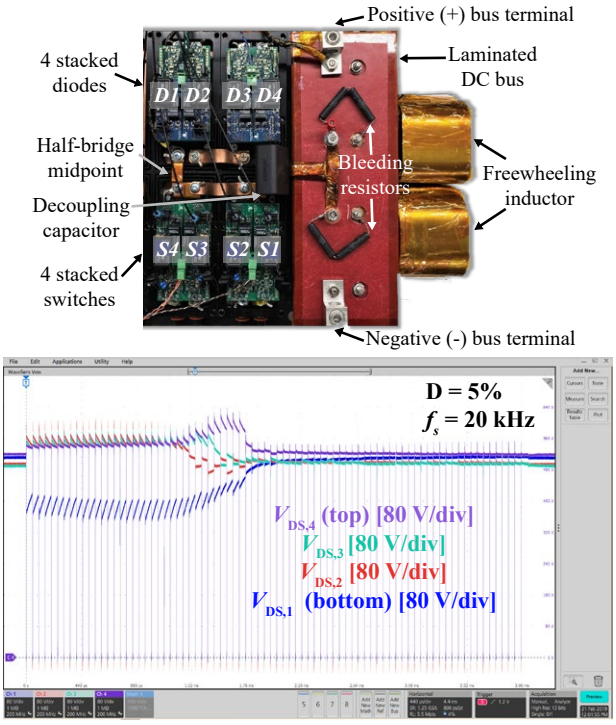


Fig. 2. Closed-loop dv/dt control of four stacked SiC MOSFETs with a 2 kV dc bus in a half-bridge configuration.

Distributed Control and Communication System for SiC-Based Modular Power Converters

A distributed control and communication protocol has been designed and verified for a power electronics building block (PEBB)-based converter, with a new synchronization method. The master-slave communication mode with bidirectional line topology is shown in Fig. 1. There are three main steps to run the system. The first step is the start-up address distribution to arrange the address number for each slave. The second step is the start-up synchronization to synchronize all of the slaves with the master. The third step is normal communication. During every cycle time, slaves send voltage and current to the master and generate gate signals, based on the calculated pulse width modulation (PWM) references received from the master. Some non-periodic information, such as the synchronization command, temperature, and fault signal, should also be transmitted during the normal com-munication step.

For synchronizing the communication system, the oversampling method is used in the clock and data recovery block to make the offset between nodes constant. Synchronization based on the precision time protocol (PTP) compensates the offset.

The protocol design was verified using four controllers: one the master, and the other three slaves. Successful synchronization among the four nodes is shown in Fig. 2. The square wave based on the local time counter of each node is observed. In the communication network, the clock frequency of the FPGA controller is 200 MHz, and the data rate is 40 Mbps. Zooming in, the maximum jitter of three slaves is 25 ns, as shown in Fig. 2.

In summary, a distributed control and communication protocol has been designed and verified for a PEBB-based converter, and a new synchronization method is implemented in the system. Compared with commercial chips, the forward delay per node can be reduced, and a communication frequency of 120 kHz is realized. The synchronization accuracy can be well controlled with the maximum jitter of 25 ns among four nodes.

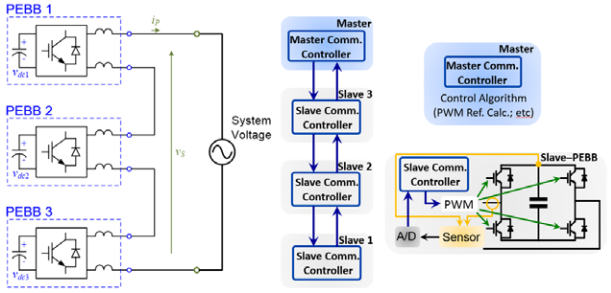


Fig. 1. System configuration of the converter.

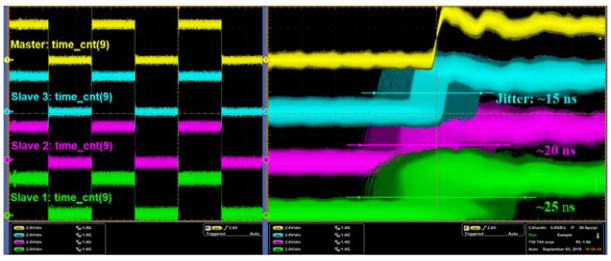


Fig. 2. Synchronization among four nodes.

Short-Circuit and Overload Gate-Driver Protection Schemes for 1.2 kV, 400 A SiC MOSFET Modules

This paper proposes short-circuit and overload gate-driver protection schemes, based on the parasitic inductance between the Kelvin- and power-source terminals of high-current silicon carbide (SiC) MOSFET modules. A comprehensive analysis of the two schemes is presented. It includes the worst-case analysis used to assess their parametric dependence due to manufacturing tolerance and temperature variations. Also included is the in-depth design procedure that can be generally applied to any power module containing a Kelvin source. For verification purposes, a compact 1.2 kV, 400 A half-bridge module, integrating the two protection circuits, is developed. The results demonstrated a response time within tens of nanoseconds, and effectively validated their functionality under fault and overload scenarios. As shown in Fig. 1, two overcurrent-detection-schemes are presented, based on parasitic inductance between the power source and the Kelvin source of SiC MOSFET power modules. A compact 1.2 kV SiC MOSFET gate driver prototype that integrates the two overcurrent detection circuits is developed, to validate their functionalities under conditions of different ambient temperatures.

For the short-circuit (SC) protection circuit, this paper provides a comprehensive analysis and detailed in-depth design procedure that is universally applicable to any power module with a Kelvin source. A novel circuit is then developed to realize an overload (OL) protection circuit, based on the same principle. This circuit helps to detect overload current conditions and to prevent the system from exceeding its thermal design limit. The OL detection circuit is designed to trigger with high flexibility, avoiding the generation of false trigger events. The parametric dependence of both SC and OL circuits is thoroughly studied by means of a worst-case analysis. This analysis shows the relatively small impact on the fault detection schemes proposed, when selecting low tolerance components with reduced thermal drift characteristics. Both SC and OL circuits were shown to exhibit a fast response with a delay within tens of nanoseconds and a high current range with no specific limitations. Fig. 2 shows the short-circuit protection procedure. The SC detector demonstrated a wide bandwidth up to hundreds of MHz, featuring low power loss. It is easily integrated on the gate-driver PCB using low-cost basic R, L, C components and comparators. A gate-driver prototype integrating the proposed overcurrent detection scheme, was built and demonstrated, under short-circuit faults and overload conditions. The full qualification of the proposed protection system was conducted in a 100 kW, 400 V three-phase voltage-source inverter, operating under 105° C ambient temperature conditions.

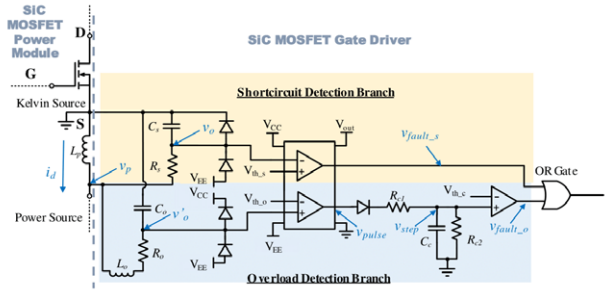


Fig. 1. Short-circuit and overload detection scheme.

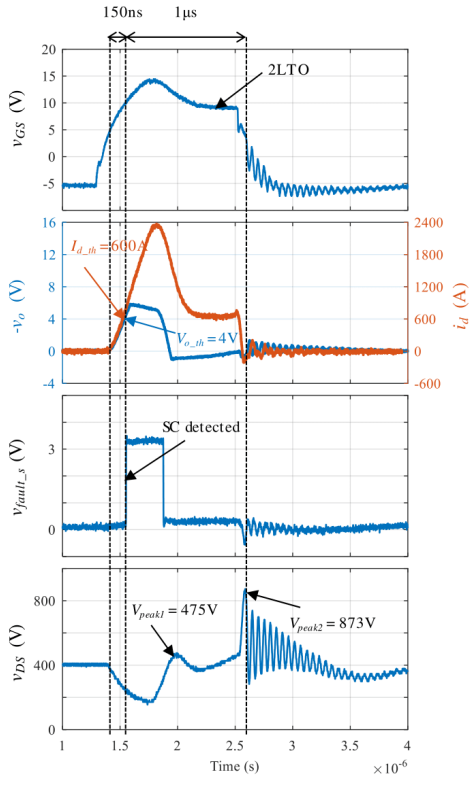


Fig. 2. Short-circuit protection procedure.

Analysis and Control of a Transformerless Series Injector Based on Paralleled H-Bridge Converters for Measuring Impedance of Three-Phase AC Power Systems

Three-phase ac power systems are prone to small-signal instability due to the dynamic behaviors of individual power equipment, such as a power electronics converter. The basic principle of extracting small-signal impedances of three-phase ac systems has been well established. Small perturbation signal at various selected frequencies under synchronous reference frequency (SRF) are injected into the system. Corresponding responses of current and voltage at the terminal of the subsystems are measured and then processed to compute the impedance. In the series injector paralleling H-bridge converters, the system current should be shared among H-bridge converters, while their dc voltages must be balanced and equal to the reference, since their dc links are isolated and floating. However, it is interesting to find that the dc voltages of H-bridge converters are not balanced anymore when the magnitude of system current reaches and exceeds a certain point.

To tackle the problem, this paper presents a deep analysis of the mechanism behind dc voltages being unbalanced. It is revealed that a positive feedback appears in the dc voltages balancing loop when system current is larger than a certain point. Furthermore, an enhanced control scheme is proposed for the transformerless series injector, where reactive circulating currents among the H-bridge converters are introduced to balance dc voltages. The series injector is able to operate in full system current range. Finally, the theoretical analysis is verified by experimental results.

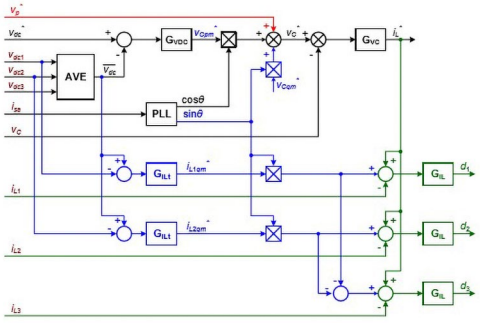
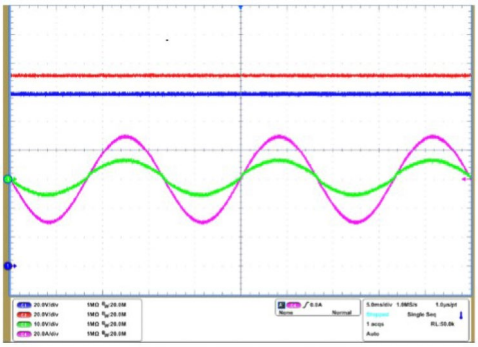
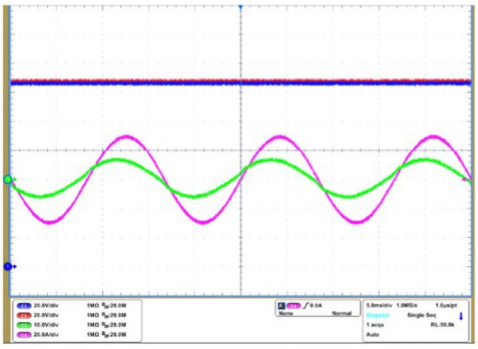


Fig. 1. Block diagram of proposed control scheme for the transformerless series injector.



(a)



(b)

Fig. 2. Experimental waveforms under (a) existing control scheme and (b) proposed control scheme CH1, vdc1, 20 V/div; CH2, vdc2, 20 V/div; CH3, vC, 10 V/div; CH4, iSa, 20 A/div.

Model of Hysteresis and Magnetoelectric Effect for a Voltage-Controllable Inductor

The voltage-controllable inductor (VCI) is one of the magneto-electric components. Such devices help achieve efficient energy conversion with the coupling effect of electric and magnetic fields. By actively changing the hysteresis loop, VCI changes its effective inductance, thus improving the circuit performance. The structure of the voltage-controllable inductor is shown in Fig. 1(a). It is comprised of two types of material: magnetostrictive material made from nick-zinc ferrite, and piezoelectric material made from lead zirconate titanate (PZT). For conventional inductors, there are only two terminals (a+ and a-), connecting with the circuit. With a VCI, there are two extra terminals (c+ and c-), connecting to a control voltage Vc, ranging from 0 V to 500 V.

Fig. 1(b) shows the control mechanism. When a control voltage is applied to the control port, an electric field is generated in the inductor. This causes the piezoelectric layer to generate mechanical strain, compressing the magnetostrictive layer. With the strain, a magnetic field generated by the magnetoelectric effect, is superimposed on the original magnetic field. Thus, the inductance L(Vc) is controlled by the control voltage.

To model the hysteresis and magnetoelectric effect of the VCI, the magnetic hysteresis loop under magnetoelectric effect is measured. The measurement method is introduced and explained for the modeling. Fig. 2 shows the experimental setup for the measurement. The modeling approach and measurement error analysis are presented, based on the experimental results.

Finally, this work presents a model that considers the magnetic hysteresis and magnetoelectric effect for the voltage-controllable inductor. The new model shows good accuracy compared with the test results, as shown in Fig. 3. An equivalent SPICE model is provided for the inductor performance evaluation in the circuit level.

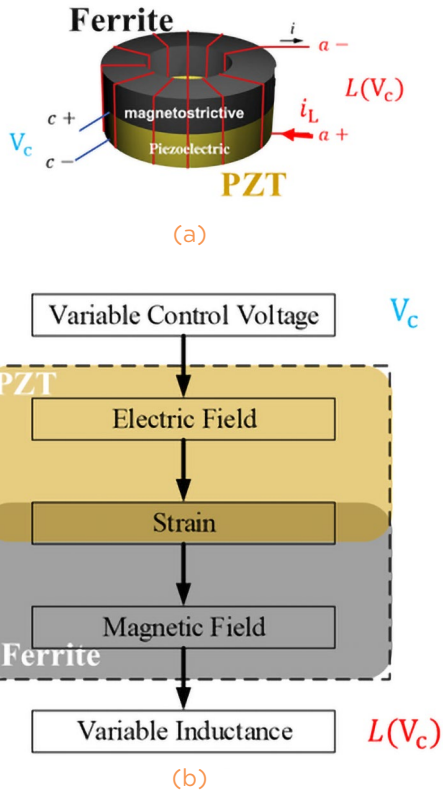


Fig. 1. (a) Schematic. (b) Control mechanism of a voltage-controllable inductor.

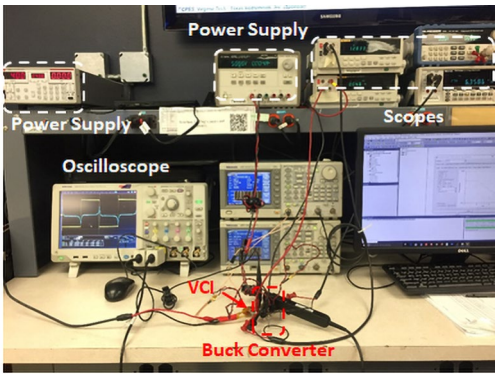


Fig. 2. Experimental setup for measuring hysteresis loop.

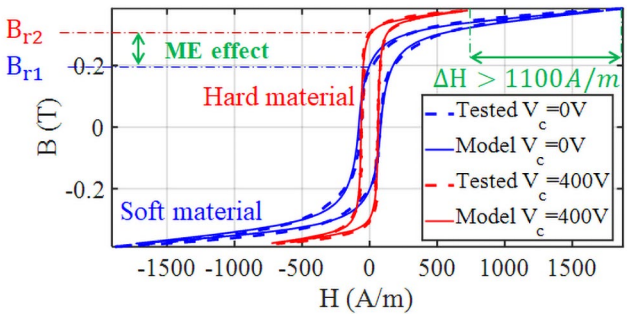


Fig. 3. Model verification with experiment.

Design and Testing of 1 kV H-Bridge Power Electronics Building Block Based on 1.7 kV SiC MOSFET Module

The Power Electronics Building Block (PEBB), as a concept to construct modular converters, was originally proposed by the Office of Naval Research in 1997. A PEBB is defined as a universal power processor that uses a systematic approach and has features of modular configurations, scalable voltage, and current ratings, as well as low inventory and maintenance cost.

As a result of the booming technology associated with wide-bandgap semiconductor devices and packaging, silicon carbide (SiC) MOSFETs have demonstrated their superior performance to silicon (Si) insulated-gate bipolar transistors (IGBTs) in terms of higher breakdown voltage, faster switching speed, lower switching loss, and higher operating temperature. Historically, in power electronics, high switching frequency and low switching loss have been the driving forces for reducing the size of passive and thermal management components. It is highly likely that SiC MOSFETs will change the game of developing high-density medium voltage (MV) PEBBs and power converters. However, SiC MOSFETs bring harsh challenges to power stage, gate driving, protection, and control circuitry designs for a SiC-MOSFET-based PEBB, as shown in Fig. 1. This paper tackles those challenges and ensures the best performance for the SiC PEBB.

Fig. 2 shows the PEBB1000. All of the parts are integrated to build the modular converters, including the controller, smart gate driver, busbar, inductors, dc-link capacitors, switches, different sensors, etc. A novel switching-cycle control (SCC) is proposed to minimize capacitor size and to enable the dc-dc operation of the modular multilevel converter (MMC). The basic modular multilevel buck converter (MMBC) was built with the PEBB1000 to validate the SCC approach. The PEBB DC capacitance was Cdc = 58 μF, and the PEBB inductance was Ldm = 4 μH, which is a significant reduction in size, compared to the conventional MMC and conventional MMC control schemes.

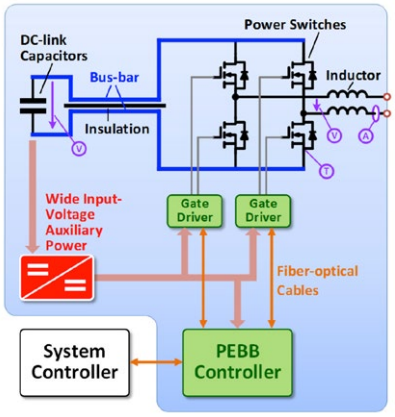


Fig. 1. PEBB with dc-fed auxiliary power supply.

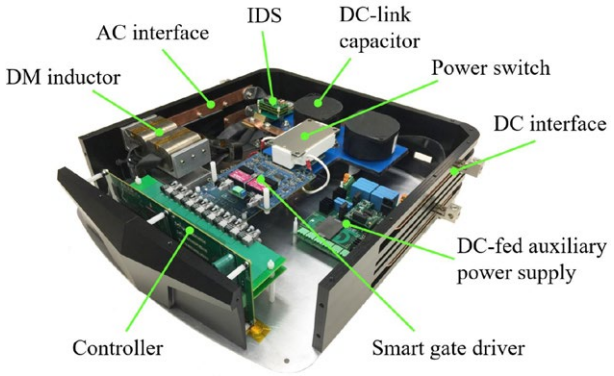


Fig. 2. PEBB1000 prototype assembly.

Design and Testing of 6 kV H-Bridge Power Electronics Building Block Based on 10 kV SiC MOSFET Module

A power electronics building block (PEBB) has been defined as a universal power processor, featuring modular configurations, scalable voltage, and current ratings, as well as low inventory and maintenance cost. In the past two decades, nearly all of the commercial high-power converters took advantage of the PEBB concept in medium voltage (MV) and high-voltage (HV) applications. Those PEBBs are connected in series, parallel, or multiple-phase configurations to scale up the voltage and current ratings of PEBB-based converters, breaking through the constraints of the semiconductor device ratings. In recent years, as a result of the booming technology of wide-bandgap semiconductor devices and packaging, silicon carbide (SiC) MOSFETs have demonstrated their superior performance to silicon (Si) IGBTs in terms of higher breakdown voltage, faster switching speed, lower switching loss, and higher operating temperature. The high blocking voltage of SiC MOSFETs simplifies the PEBB power stage, (shown in Fig. 1), by using uncomplicated topologies. Their high switching frequency preserves the overall harmonic performance, despite a reduced number of voltage levels.

The design and testing of smart gate drivers, gate driver power supplies, and the laminated dc bus-bar were explored, and all of them showed excellent performance. The H-bridge power stage and gate drivers were integrated into a plastic enclosure, shown in Fig. 2, a test plat-form for further assessment. The remaining parts of the PEBB6000 design will be published in the future. The gate driver is the critical interface between the power semiconductor devices and control signals. It serves to provide galvanic isolation and to supply driving current, while maintaining signal integrity under a high-noise environment. In addition to those basic tasks, it provides quick, reliable, and configurable protection, as well as advanced switch-current signal sensing and data processing for control purposes, which define a “smart” gate driver. The gate driver power supply must withstand the voltage stress between its primary and secondary sides, as well as having a low input-output parasitic capacitance to reduce the CM noise current. In this design, a resonant converter that offers a resonant current bus (RCB) to drive multiple isolated load is proposed, and achieves 20 kV isolation and only 1.56 pF of input-to-output parasitic capacitance. For the laminated busbar design, three different possibilities are evaluated. The option with the midpoint on top of the positive and negative busbar performed the best in terms of losses and fringing flux.

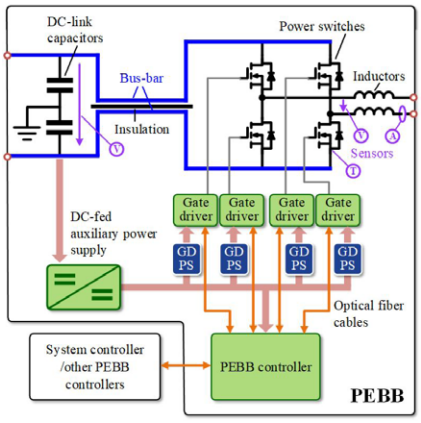


Fig. 1. PEBB6000 system architecture diagram.

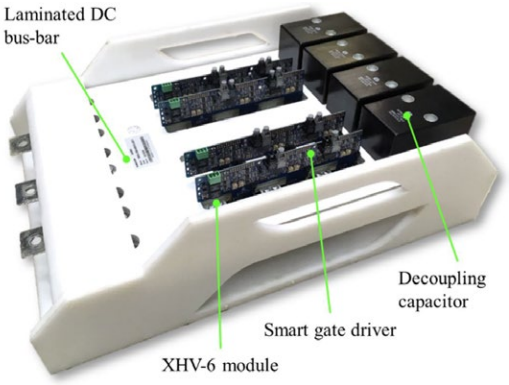


Fig. 2. PEBB6000 prototype integrating XHV-6 modules, gate drivers, and the laminated DC bus-bar.

A High-Speed Gate Driver with PCB-Embedded Rogowski Switch-Current Sensor for a 10 kV, 240 A, SiC MOSFET Module

As a result of the booming technology of wide-bandgap (WBG) semiconductor devices and packaging, silicon carbide (SiC) MOSFETs have demonstrated their superior performance to silicon (Si) IGBTs. Wolfspeed has developed a 10 kV, 240 A SiC MOSFET, module XHV-6, which uses their 3rd generation 10 kV, 350 m SiC MOSFETs with an improved package layout. This device is suitable to construct converters such as a 6.7 kV dc, 3.3 kV ac motor drive, by using a simple three-phase two-level topology. For the XHV-6 module, three submodules that contain 18 10 kV, 350 m SiC MOSFET dies need to be driven simultaneously. The driving current magnitude, driving signal synchronization, driving loop parasitics, and common-mode noises become big challenges. A gate driver can provide quick, reliable, and configurable protections, as well as advanced switch-current signal sensing, digital data processing, and active gate controllability; all of which define a "smart" gate driver. A prototype gate driver is shown on Fig. 1.

A well-planned gate driver architecture design is able to keep common-mode (CM) noise current away from sensitive components. This is even more critical for a smart gate driver, as a large amount of analog and digital signals are processed on the board. A field-programmable gate array (FPGA) manages gate driver IC programming, Rogowski switch-current sensor (RSCS) reset, analog/digital conversion (ADC), and communication to other units. External current boosters are designed to supply almost 90 A peak current to sustain the fastest switching transient and to fully enable the benefits of the SIC MOSFET device. A current booster solution with nine paralleled bipolar junction transistors (BJTs) has been proposed and designed. An RSCS has been proposed to work effectively together with the SiC MOSFET modules. The high bandwidth, wide measurement range, good accuracy, and solid signal isolation make it an excellent short-circuit current detector and current control for SiC devices. Fig. 2 shows the 6 kV double pulse test result at 120 A, achieving 50 V/ns transient switching.

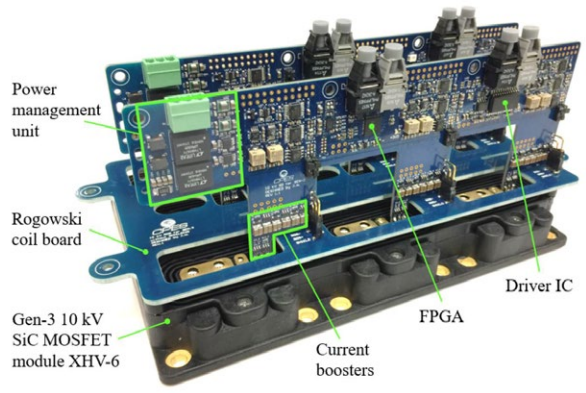


Fig. 1. Prototype gate driver mounted on a XHV-6 module.

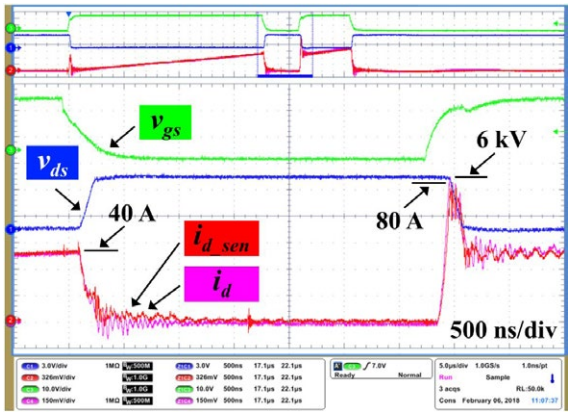


Fig. 2. 6 kV experimental switching results.

Design and Control of Tunable Piezoelectric Transformer Based DC-DC Converter

The piezoelectric transformer (PT) is an alternative for magnetic transformers in power converters. Compared to the magnetic transformer, the PT exchanges electric potential with the mechanical force instead of the magnetic flux. Specifically, the tunable piezoelectric transformer (TPT) is a recently developed device that has input, output, and control ports. When connected with different impedance at the control port, the TPT has different input-to-output voltage gain characteristics.

The proposed TPT-based converter is shown in Fig. 1. A half-bridge voltage inverter is used to generate an ac voltage with frequency. An input inductor is utilized to filter out the high frequency harmonics entering the TPT. A bridge rectifier is applied at the output port of the TPT. Following the rectifier, an LC filter is used to reduce the ripple of output voltage. A variable capacitor, realized by a duty cycle controlled switched capacitor, is used at the control port to achieve the output voltage regulation at different load and/or input conditions.

Fig. 2 shows the experimental waveforms of output voltage V_o (blue curve), duty cycle D of the control switch S_{Ctrl} (yellow curve), and its drain-to-source voltage of V_{dsCtrl} (green curve) under different test conditions. When either the input line voltage or the output load resistance increases, D increases so that V_o is regulated, and vice versa. It is also verified that zero voltage switching is achieved for the control switch, since S_{Ctrl} is always turned on when V_{dsCtrl}=0.

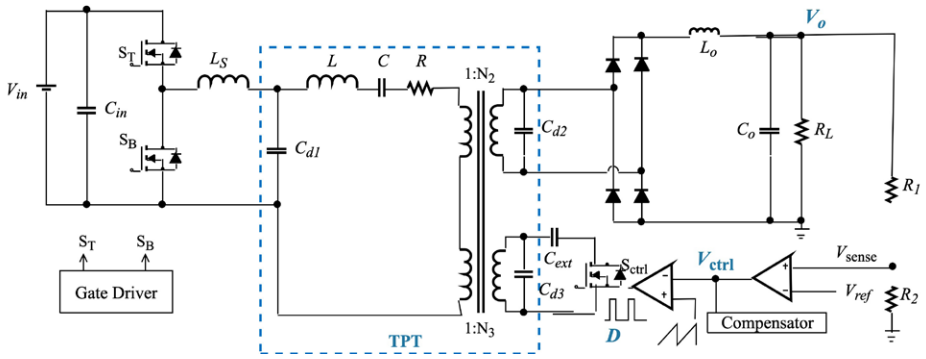


Fig. 1. Proposed TPT based dc/dc converter.

100% Load, V_{in} = 160 V | 30% Load, V_{in} = 160 V | 30% Load, V_{in} = 55 V

Fig. 2. Experimental waveforms.

Design of a Compact, Low Inductance 1200 V, 6.5 mΩ SiC Half-Bridge Power Module with Flexible PCB Gate Loop Connection

The properties of silicon carbide (SiC) devices make them desirable for use in power modules due to their high-power density capabilities, robust operation at higher temperatures, and low losses. SiC can be switched at higher frequencies than silicon (Si), enabling passive components to be smaller, thus reducing the size of fabricated modules. With these advantages comes the need for updated packaging techniques.

The design of this power module includes new methods in order to obtain low inductance, compact size, and reliable performance using Wolfspeed's 1200 V, 13 mΩ SiC MOSFET. Using the MOSFET body diodes increases the potential power density by eliminating the need for external antiparallel diodes. Reduction of the gate loop inductance is achieved with a flexible PCB serving as the gate, desaturation point, and kelvin source interconnection. Lastly, a balanced/symmetrical direct bonded copper (DBC) layout increases the likelihood of current balance in the commutation loop. The final design is shown in Fig. 1 with the patterned DBC and the die on top, the base plate, and the housing.

One of the more novel and challenging elements of the module fabrication process is attaching the flexible circuit on the bare die. This is due to the small area available for attachment, heat sensitivity of the die, and incompatibility of some attachment materials to the die. The flexible PCB is attached using a nanosilver sinter paste which can bond with the specialized nickel/gold top coat die.

To test the functionality of the half-bridge SiC power module, a static and dynamic characterization will be performed. The static characterization will include output and transfer curves. A clamped inductive load tester allows for dynamic characterization under different load currents. The tester was designed with vias to easily attach to pins coming out of the flexible PCBs (Fig. 2).

New techniques used in the design of this power module take advantage of SIC properties. Two power modules are designed to compare current sharing behavior: 1) the control sample with balanced die, and 2) the other with unbalanced die. The individual die currents are measured with Rogowski coils (Fig. 1) to determine the effects of the unbalanced die on power module performance.

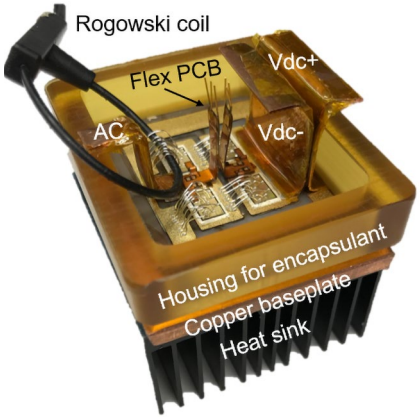


Fig. 1. Half-bridge power module with Rogowski coil around bottom side wire bonds.

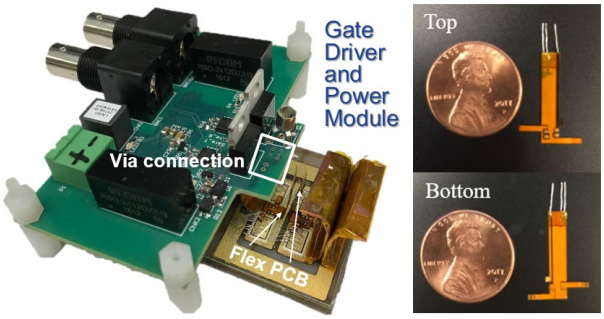


Fig. 2. Flexible PCB attach to gate driver PCB; size of PCB against a penny; pins for gate, kelvin, and desat shown from left to right from the top view.

Design Space of Vertical GaN Superjunction Power Transistors for 1.2-10 kV Applications

Vertical superjunction devices could break the theoretical limits of on-resistance (R_{on}) and breakdown voltage (BV) in unipolar power devices and allow a linear dependence of R_{on} on BV. While no experimental demonstration of vertical gallium nitride (GaN) superjunction devices have been reported so far, Si superjunction devices have achieved huge commercial success.

Our work explores the design space of vertical GaN superjunction field effect transistors (SJ-FETs) for 1.2 kV to 10 kV voltage classes, based on theoretical analysis and TCAD simulation. To obtain the best trade-off between R_{on} and BV, we identified and optimized key device designs, including the pillar width, doping concentration, superjunction thickness, etc. Based on the analysis, two novel vertical GaN SJ-FET with 2DEG and fin channels, i.e. a GaN superjunction current-aperture vertical electron transistor (SJ-CAVET) and a GaN superjunction fin field-effect-transistor (SJ-FinFET), were proposed and simulated. Fig. 1 shows the device structure schematics of two kinds of GaN superjunction devices.

In addition, a well-calibrated physics-based TCAD simulation was used to design 1.7 kV, 50 A normally-off GaN SJ-CAVETs and SJ-FinFETs. Following, a device-circuit mixed-mode simulation was utilized for their switching performance. The device on-resistance (0.35 mΩ·cm^2) and chip area (0.2 mm^2) are at least 25-fold smaller than today's best 1.7 kV, 50 A power transistors. Due to the smaller device area, the device junction capacitances and switching charges are also significantly smaller. A practical switching frequency of ~MHz was determined from the trade-offs between switching and conduction losses.

The simulation of higher-voltage GaN SJ-CAVETs and SJ-FinFETs up to 10 kV reveal consistent advantages over their commercial counterparts. Fig. 2 shows $R_{on,sp}$~V_B trade-offs for GaN SJ-CAVETs and SJ-FinFETs designed for 1.2 kV~10 kV power applications. Our simulation revealed at least 10-to-100-fold smaller Ron in 1.2 kV-10 kV vertical GaN SJ-FETs, compared to unipolar vertical GaN power transistors with the same BV classes. These results show the great potential of GaN SJ-CAVETs and SJ-FinFETs for future medium-to-high-voltage high-frequency power applications.

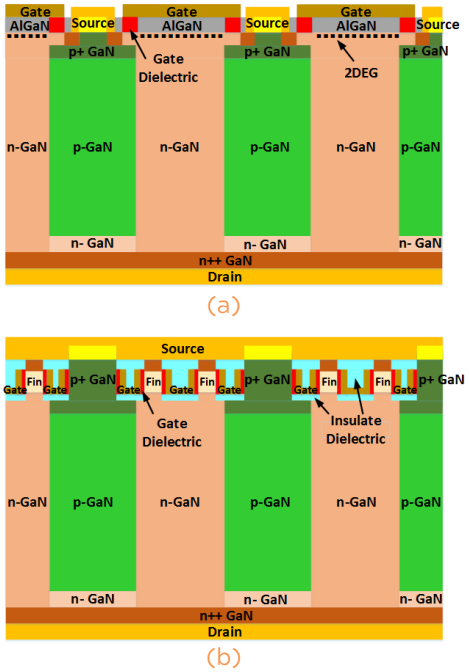


Fig. 1. Schematic structures of the (a) GaN SJ-CAVET and (b) GaN SJ-FinFET proposed in this work.

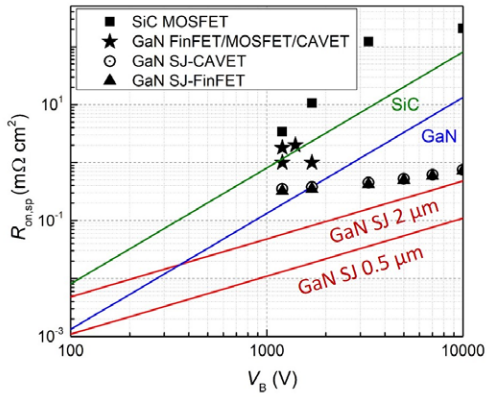


Fig. 2. $R_{on,sp}$~V_B trade-offs for GaN SJ-CAVETs and SJ-FinFETs designed for 1.2 kV~10 kV power applications. Theoretical limits for SiC and GaN unipolar devices as well GaN superjunction devices, the experimental data for state-the-art GaN vertical transistors with unipolar drift regions and SiC MOSFETs are included.

Medium Voltage SiC Based Converter Laminated Bus Insulation Design and Assessment

The laminated bus has been widely used in power electronics for decades. By arbitrarily sweeping the bus insulation thickness, its parasitic inductance increases significantly with the insulation. The bus's weight, size, and cooling performance suffer from the increase of insulation; therefore, the thinner the insulation is, the better overall performance the bus can have. The insulation thickness should have the lowest boundary, which can guarantee to block certain voltage across it with enough lifetime. Since the insulation design and an assessment of the laminated bus have not been fully studied, currently, a large security margin has to be applied. This results in very thick insulation, especially for the medium and high voltage converters. Then again, excessive partial discharge (PD) inside the defects of the adhesive layers or along surfaces can still degrade the insulation; thus, an over-designed insulation may not help a great deal.

Focusing on insulation design and assessment, two major representative structures in the bus are analyzed in this paper, as shown in Fig. 1. Based on the electric field simulation results along various ideal insulation systems, some basic guidelines can be concluded. There is one dominant difference between the ideal insulation systems and the real ones; defects in the adhesive layer are the main reason for accelerated insulation degradation. Therefore, these defects are fully estimated via PD tests among coupons with different material and fabrication processes. Part of these PD test results are shown in Fig. 2.

Finally, comprehensive guidelines on both the design and experimental evaluation of the laminated bus insulation system will be provided in this paper, with a combined consideration on the electric field management, material selection, and fabrication process.

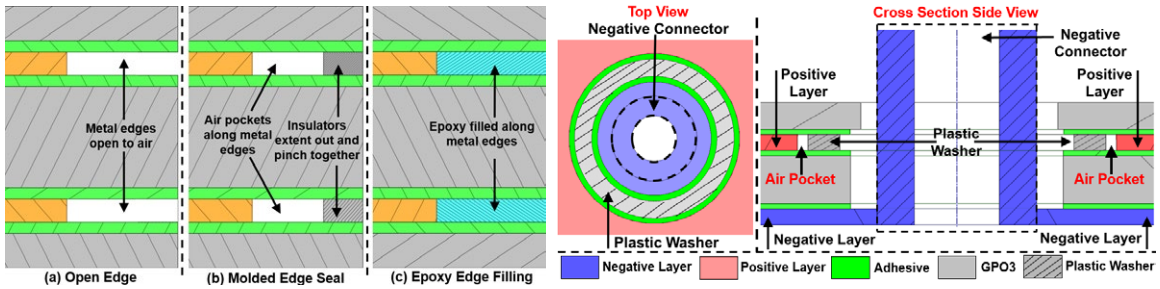


Fig. 1. Two major representative structures in the laminated bus: parallel-plate structure with edge treatment options and coaxial cylinder structure along the connection areas.

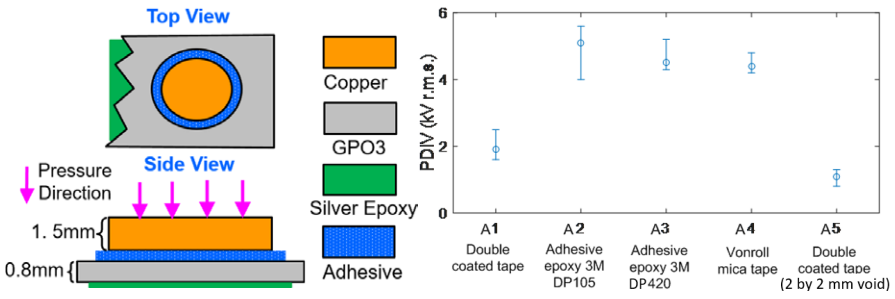


Fig. 2. Parallel plate test coupon general structure and dimensions with PD inception voltage comparison for different test coupons.

Electrical Field Analysis and Insulation Evaluation of a 6 kV H-Bridge Power Electronics Building Block (PEBB) Using 10 kV SiC MOSFET Devices

The main parts of the PEBB analyzed in this work are shown in Fig. 1. It contains two 10 kV MOSFET half-bridge power modules with a self-designed laminated bus, smart gate drivers, sensing boards, etc. The power module connects to the laminated bus via a spacer-hole structure. There is a self-designed embedded Rogowski coil PCB between the module and the bus, which measures the current going in and out from the dc power terminals of the module. Gate driver boards go through the holes from the top surface of the bus, all the way down, to be connected to the driving terminals of the power module beneath. Focusing on the insulation design and assessment, two kinds of insulation issues exist in the assembly. For example, internal defects in the adhesive layer of the laminated bus can introduce excessive partial discharge internally, and thus significantly decrease the lifetime of the material around it. Meanwhile, the high electric stress on the exposed metal surfaces of the interconnectors, may cause partial breakdown of air and generate significant surface discharge. These two kinds of issues are demonstrated, as shown by Fig. 2.

For the internal discharge issue, the insulation of a real laminated bus is evaluated. Some representative coupons are tested to demonstrate possible design issues for the existing bus and provide clues for further improvement. For the surface discharge issue along the interconnectors, a three-dimensional electric field model, taking into account different switching status, is developed, and results of electric field intensity distributions are analyzed. Geometry-based modifications are then proposed to relieve the electric stress on the critical regions. The insulation performance of one type of interconnector mentioned in this paper, is tested and verified. Afterwards, three kinds of surface treatment are individually applied on the exposed metal surface of the connector. The evaluation of the original structure, together with the comparison after applying different surface treatment material, is shown. A summary and some design guidelines are given at the end of the paper.

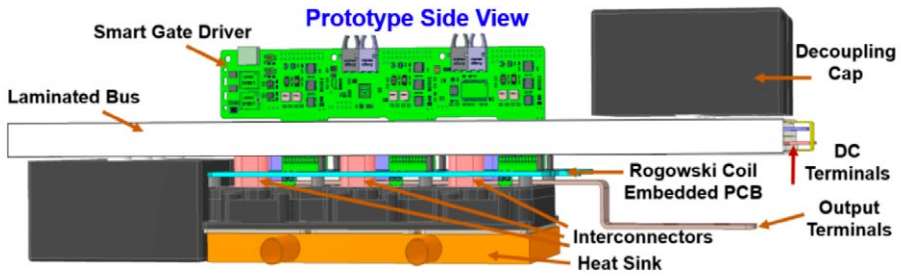


Fig. 1. Side view of the 10 kV power MOSFET half-bridge power module based H-bridge converter assembly.

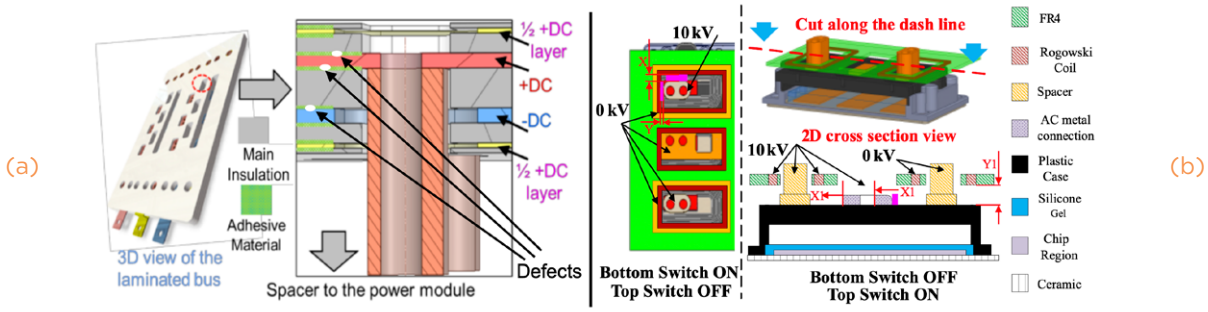


Fig. 2. Examples of internal and surfaces insulation issues inside the PEBB 6000 assembly. (a) 2D cross-section view of the laminated bus with internal defects in the adhesive layer. (b)Electric field crowding regions on the exposed metal surfaces under varied switching status.

Design of a SiC-Based 5-Level Stacked Multicell Converter for High-Speed Motor Drives

High-speed motor drives are valued in industrial applications for their low weight and volume. A major design challenge is generating high quality output voltages at high output frequency and maintaining high efficiency at the same time, as a high switching frequency is typically required by the former, but may lead to more losses. The wide-bandgap (WBG) devices, such as SiC MOSFETs, are suitable for high-speed motor drives due to their lower losses and higher switching speed compared to traditional silicon (Si) devices. On the other hand, multilevel converters can achieve high quality output voltages while maintaining low device switching frequency.

Another key challenge is restraining the over-voltage along the motor cable caused by the voltage reflection. The two-level inverter, three-level T-type inverter, and five-level Stacked Multicell Converter (SMC) are compared through simulation with the same modelled motor cable, modelled motor, device switching frequency, and switching speed. As the output voltage level increases, the output voltage quality increases, and the maximum voltage at the end of the motor cable reduces. In the five-level SMC case, the maximum voltage value is only 73 percent higher than the dc bus voltage, eliminating the need of an over-voltage mitigation filter; thus, reducing the total loss and weight of the system.

The configuration of one phase leg of a five-level SMC is shown in Fig. 1. There are two split dc capacitors and two flying capacitors per phase. One phase leg is the equivalent of two series-connected three-level T-type cells, each of which has two pairs of complementary switching devices. A phase-shifted PWM is applied to the two cells to achieve five output voltage levels.

As the three phase legs are identical and the two T-type cells in one phase leg are similar, the PCB design can be focused on the design of one cell. Fig. 2 shows the top view of one cell. The four switching devices (marked in blue) are placed in the middle of the cell. The two middle devices, located in the lower half, are placed next to each other because the source terminals of these two devices have to be close and connected together. The top and bottom devices, located in the upper half, have heat-sinks mounted on the top because they are estimated to have higher losses than middle devices. Each switching device has its own driving circuit (marked in purple). Decoupling capacitors (marked in red) are placed around and near the switching devices. The main power is transferred from left to right through the switching devices in the middle of the cell, while the auxiliary power and signals are transferred from right to left either at the top or bottom of the cell. There is no overlap be-tween the power circuits and auxiliary circuits.

In this study, a three-phase five-level stacked multicell converter (SMC) using SiC MOSFETs is designed for high-speed motor drives. The properties and the advantages of the selected topology are explored. The converter design is finished, including switching device selection, passive component selection, and PCB layout design, and is validated by experimental results.

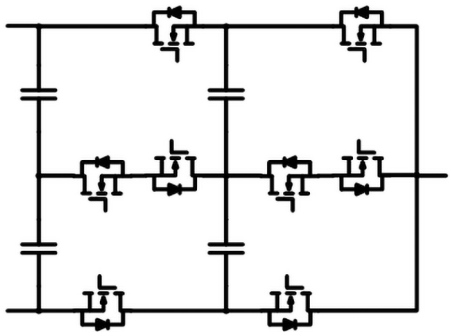


Fig. 1. One phase leg of a 5-level SMC.

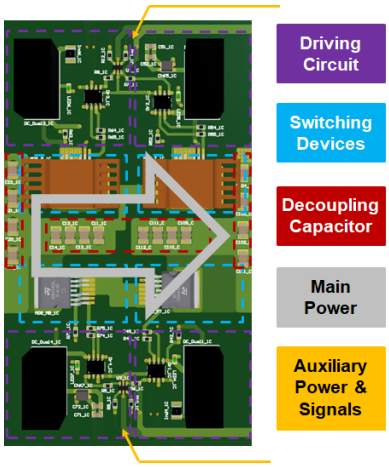


Fig. 2. Top view of one T-type cell.

Design of a Zero Voltage Switching Class-E Inverter with Fixed Gain

It is difficult for Class-E inverters to maintain fixed gain or zero-voltage-switching (ZVS) over a wide load range. A sequential design methodology of a fixed-gain Class-E inverter is presented without adding components or using closed-loop controls. Zero-voltage turn-on with zero-voltage-derivative under full load condition, and zero-voltage turn-on and fixed voltage gain is kept with load variation. The expectations were validated by a Class-E inverter switched at 6.78 MHz with 11 V input voltage and 25 W maximum output power over 10:1 output power range.

The topology of a Class-E inverter is shown in Fig. 1. The performance of the three designs are compared in Fig. 2 to summarize the contribution of this work.

The traditional design offers ZVDS and ZVS under optimum condition, but non-ZVS occurs with load variation. Some researchers propose that ZVS and the output voltage be kept under light load, but the cost is high current stress and small power-output capability. The design methodology in this work keeps ZVDS and ZVS under nominal load condition and realizes ZVS and regulation at low-load condition with reduced current stress.

The operating principle and sequential design of the ZVS Class-E with fixed gain is introduced. The detailed design steps are listed with 11 V input voltage, 16 V output voltage, and 25 W maximum output power over 10:1 output power range.

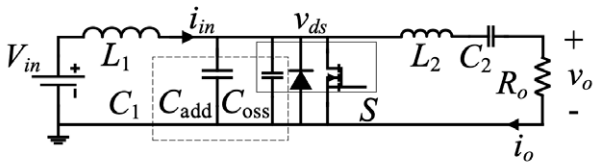


Fig. 1. Topology of a Class-E Inverter.

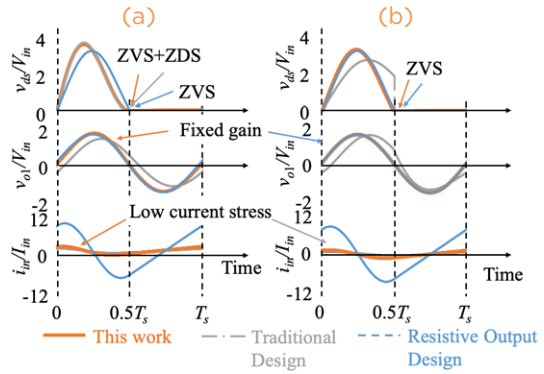


Fig. 2. Waveforms under (a) nominal load and (b) 10 percent load condition of three designs of Class-E inverter.

VIRGINIA TECH

Center for Power Electronics Systems

Blacksburg
1185 Perry Street
655 Whittemore Hall
Blacksburg, VA 24061

National Capital Region
900 N. Glebe Road
Arlington, VA 22203

cpes.vt.edu