

**Gigahertz-Range Multiplier Architectures Using
MOS Current Mode Logic (MCML)**

Venkataramanujam Srinivasan

Thesis submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science
in
Electrical Engineering

Dr. Dong S. Ha, Chairman

Dr. Joseph G. Tront

Dr. James R. Armstrong

December 2003

Blacksburg, Virginia

Keywords: MCML, High-speed multipliers, High-speed circuit design, VLSI Design

Copyright 2003, Venkat Srinivasan

Gigahertz-Range Multiplier Architectures Using MOS Current Mode Logic (MCML)

Venkataramanujam Srinivasan

Dr. Dong S. Ha, Chairman

The Bradley Department of Electrical and Computer Engineering

ABSTRACT

The tremendous advancement in VLSI technologies in the past decade has fueled the need for intricate tradeoffs among speed, power dissipation and area. With gigahertz range microprocessors becoming commonplace, it is a typical design requirement to push the speed to its extreme while minimizing power dissipation and die area. Multipliers are critical components of many computational intensive circuits such as real time signal processing and arithmetic systems. The increasing demand in speed for floating-point co-processors, graphic processing units, CDMA systems and DSP chips has shaped the need for high-speed multipliers.

The focus of our research for modern digital systems is two fold. The first one is to analyze a relatively unexplored logic style called MOS Current Mode Logic (MCML), which is a promising logic technique for the design of high performance arithmetic circuits with minimal power dissipation. The second one is to design high-speed arithmetic circuits, in particular, gigahertz-range multipliers that exploit the many attractive features of the MCML logic style. A small library of MCML gates that form the core components of the multiplier were designed and optimized for high-speed operation. The three 8-bit MCML multiplier architectures designed and simulated in

TSMC 0.18 μm CMOS technology are: 3-2-tree architecture with ripple carry adder (Architecture I), 4-2-tree design with ripple carry adder (Architecture II) and 4-2-tree architecture with carry look-ahead adders (Architecture III). Architecture I operates with a maximum throughput of 4.76 GHz (4.76 Billion multiplications per second) and a latency of 3.78 ns. Architecture II has a maximum throughput of 3.3 GHz and a latency of 3 ns and Architecture III has a maximum throughput of 2 GHz and a latency of 3 ns. Architecture I achieves the highest throughput among the three multipliers, but it incurs the largest area and latency, in terms of clock cycle count as well as absolute delay. Although it is difficult to compare the speed of our multipliers with existing ones, due to the use of different technologies and different optimization goals, we believe our multipliers are among the fastest found in contemporary literature.

Acknowledgements

First, I would like to express my sincere thanks to my advisor, Dr. Dong S. Ha for his support, advice and guidance throughout my stint at Virginia Tech. But for his patience, understanding and invaluable guidance, none of this work would have been possible. I would also like to express my gratitude to Dr. Joseph G. Tront for serving on my thesis committee and for providing me the opportunity to work with him. My thanks are due to Dr. James R. Armstrong for serving as my thesis committee member and commenting on this work.

I am extremely grateful to VTVT colleague, Jos Sulisty for all his help in realizing this work. But for his inordinate patience in answering my trivial and non-trivial queries, none of this work would have been possible. I affectionately appreciate all VTVT members for their cheerful company during those long hours in the lab.