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Data Acquisition and Control System for the OLYMPUS Propagation Experiments

by

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Abstract

A data acquisition and control system (DACS) has been designed and constructed for use during propagation experiments with the OLYMPUS satellite. OLYMPUS is a European Space Agency experimental satellite that broadcasts coherent beacons at 12, 20 and 30 GHz and is viewed from Blacksburg, Virginia at an elevation angle of 13.9°. This low elevation angle yields a relatively long atmospheric path which serves to accentuate propagation effects.

The DACS is a custom design which collects propagation, environmental and status information and periodically calibrates external equipment. Beacon signal strength is measured via a hybrid analog/digital receiver. The analog portion of the receiver utilizes the coherency of the satellite beacons to track the 20 and 30 GHz signals to the noise floor. The digital portion of the receiver is contained within the DACS and consists of a stand-alone microprocessor which filters the beacon signal to determine the power in a 3 Hz bandwidth. Additional DACS circuitry collects analog and digital input channels and controls external devices through digital output channels. Digital outputs are used to reference the collected data to known levels by performing periodic calibrations on external equipment. Analog input channels are used to measure quantities including external temperature, wind speed and wind direction, while digital inputs monitor alarm conditions.

The VIEW program utility permits an operator to graphically view data in real time. In addition, collected data is stored to tape without an interruption in data collection. DACS operation has been virtually continuous since data collection was started on August 3, 1990.

Acknowledgements

First and foremost, I am indebted to my parents for their love, understanding and encouragement.

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I would also like to thank all of the Satellite Communications Group members associated with the OLYMPUS project. In particular, Dennis Sweeney for his help in implementing the I and Q detector and William Sylvester for writing VIEW, the real time graphical display program used with the data acquisition and control system.

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Chapter 1

OLYMPUS Propagation Experiments

Transferring wideband information between distant locations on the earth can be accomplished by either a physical connection or by radio. Physical connections include fiber optic cable, coaxial transmission line and submarine cable. Radio based links typically operate in the microwave frequency range and include relays between telephone exchanges and communications satellites. Microwave frequencies are utilized in radio links because the communications spectrum below about 900 MHz has been allocated for other uses. An additional advantage of microwaves is that a relatively small, and therefore inexpensive, antenna can transmit or receive a directional signal which allows multiple users to operate within one geographic area without interference.

Microwave signals require a line-of-sight path between transmitter and receiver. Therefore, the maximum transmission distance for a terrestrial link is physically limited by the earth's curvature. As an example, transmit and receive antenna located 150 feet above average terrain yield a maximum distance between transmitter and receiver of 30 miles. Hilly terrain can increase the distance to several hundred miles yet it is not possible to fulfill transcontinental communications needs. A physical connection is one solution for transcontinental communications.

Physical connections can cover a virtually unlimited distance provided that repeaters are placed in the link to periodically boost the signal. Maintaining a physical

link is relatively simple since a technician can locate the faulty section and repair it. However, if a physical link is required to pass under an ocean, maintenance costs increase tremendously because accessing the cable is more difficult. Another caveat of physical links is that adding another site to the network requires the placement of new cable. One must consider the cost of the additional cable as well as labor and right-of-way costs for the passage of cable through property owned by others. Radio communications offers an attractive alternative: locate a transmitter at one point and a receiver at a second and communications can be established. There are, however, additional problems associated with radio link design. Radio communications is inherently less reliable than a physical link because of signal attenuation from ever changing atmospheric propagation characteristics. However through careful link design, the reliability of a radio link can approach that of a physical link.

Since a microwave link requires a line-of-sight path, geosynchronous communications satellites offer an attractive alternative to overseas and some intracontinental communications. In general, a communications satellite receives a signal from an earth station at an uplink frequency, mixes the received signal to a downlink frequency and retransmits an amplified version of this signal toward the earth. The most common uplink and downlink frequency pairs are 6/4 GHz (C band) and 14/11 GHz (K_u band). To simplify earth station design and to provide continuous availability, communications satellites are placed in geosynchronous orbit. This places the satellite in an orbit approximately 35,780 km above the equator. Viewed from the earth, the ensemble of geosynchronous satellites takes the form of an arc. The number of satellites that can be placed in geosynchronous orbit and which utilize a given set of frequencies is primarily limited by antenna design constraints. A signal transmitted from an earth to a particular satellite must not interfere with adjacent satellites. Presently, the portion of the geostationary arc visible from the United States is virtually saturated with satellites operating at C band while K_u band is becoming increasing utilized. As such, future communications satellites will need to use other frequency allocations, namely

the 30/20 GHz K_a band. Unfortunately, atmospheric propagation effects which are minimal at C band and tolerable at K_u band become very significant at K_a band.

1.1 Atmospheric Effects

A signal transmitted to or received from a satellite travels roughly 40,000 km. Yet only the 20 km of the path directly above the surface of the earth significantly affects the signal[1]. The received signal level varies because of atmospheric phenomena such as stratified layering, gaseous absorption, and rain. Figure 1.1 illustrates several of these effects.

Stratified layering of the atmosphere is responsible for rapid signal fluctuations known as scintillations. As shown in Figure 1.1 scintillations result in both signal enhancement and attenuation. Scintillation amplitude tends to increase with frequency and is also affected by weather conditions. During the early afternoon hours, atmospheric heating causes instabilities within the atmosphere. The subsequent changes in the atmospheric refractive index and effective path length give rise to high scintillation activity. In contrast to scintillations, gaseous absorption is always present.

Gaseous absorption is caused by the interaction of the microwave signal and atmospheric gases and generally results in 1-2 dB of attenuation in the 10-30 GHz frequency range[2]. The primary attenuating mechanism in the frequency range of interest is water vapor resonating at 22.235 GHz. Excluding a 0.25 dB peak at this frequency, gaseous absorption increases from about 0.05 dB at 10 GHz to 0.20 dB at 30 GHz[1]. High levels of humidity and clouds present on the signal path may add an additional 1-2 dB of attenuation. Very high levels of signal attenuation result from the absorption and scattering of microwave signals by rain.

During periods of heavy rain microwave signals can become attenuated to the point where reception is no longer possible. For example, during the rain fade shown in the received signal data of Figure 1.1 the 20 GHz and 30 GHz signals are attenuated by more than 30 dB for longer than 10 minutes during an afternoon thunderstorm.

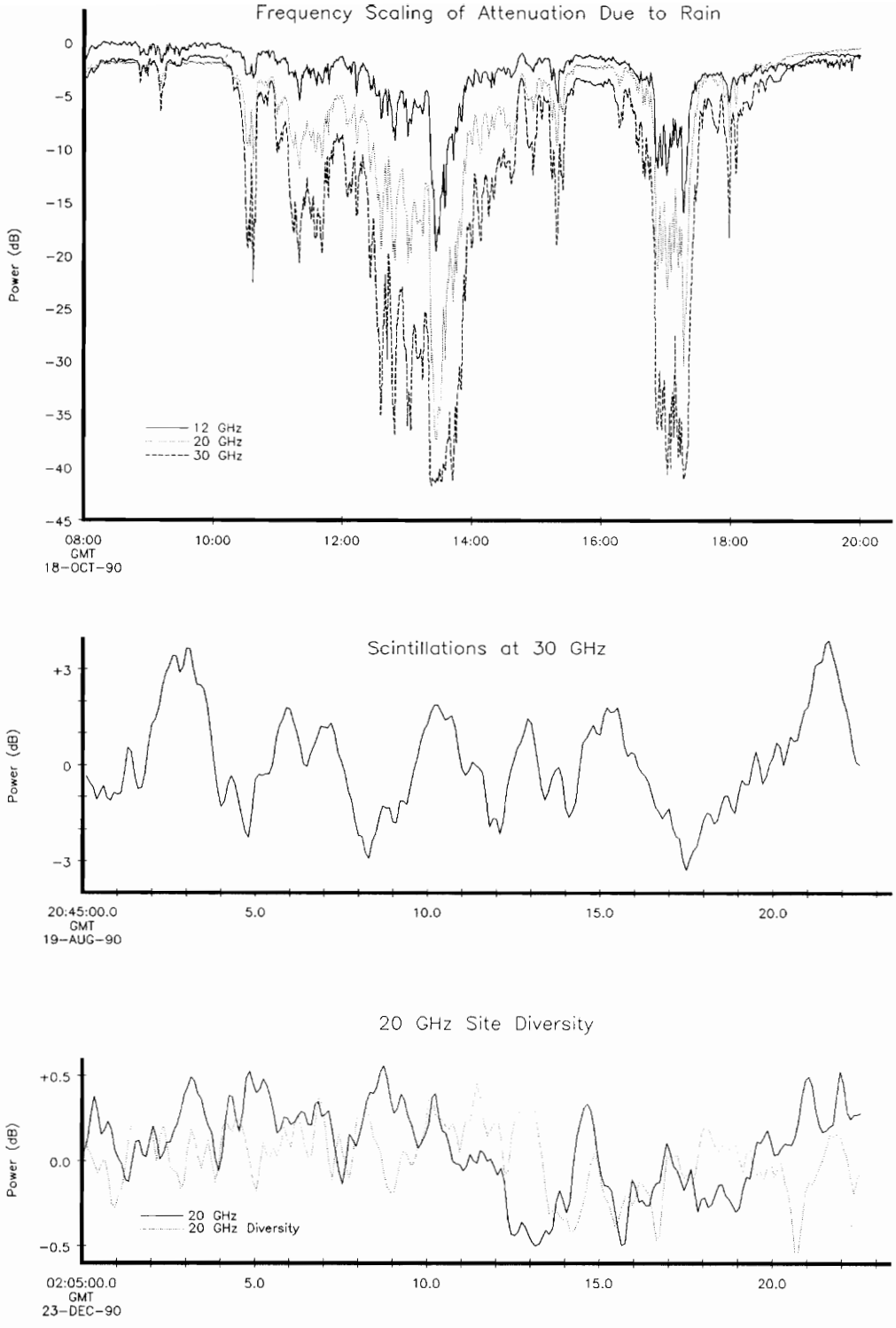

Figure 1.1. Several atmospheric signal attenuation effects observed during the OLYMPUS propagation experiments. Displays were generated from unprocessed raw data. Top graph consists of one minute averages; bottom two show all collected data points.

While this may seem to be a short period of time, downtime on a commercial data link during business hours is at best highly inconvenient and possibly quite costly. Moreover, Very Small Aperture Terminals (VSATs) – which are earth stations with relatively small dish antennas and low cost electronics with minimal reserve power – are gaining acceptance as an inexpensive method of communications for low data rate users. Most VSATs operate at K_u or K_a band with perhaps only a 3 dB margin. Thus, 3 dB of atmospheric attenuation can render a VSAT link useless. Figure 1.1 illustrates an event of this magnitude from a hot and humid August afternoon. Since scintillations can produce short term fades of more than 3 dB, and because almost no statistical data are available for short term fades, additional research is necessary.

The third graph in Figure 1.1 demonstrates site diversity. Site diversity relies on the fact that the atmosphere is non-uniform. Thus two separated terminals each receive a slightly different signal from the satellite. The data shown in Figure 1.1 was collected on an overcast day with two 20 GHz terminals separated by approximately 190 feet. Note that short term differences of 1 dB are clearly visible. The difference between the two signal levels is known as diversity gain. Characterization of diversity gain versus terminal baseline separation for distances of less than several hundred feet is an area requiring study.

Most of the previous work at K_u and K_a band is not suitable for modeling short term fade statistics[3]. Observations were performed at high elevation angles where the atmospheric path is relatively short. Additionally, the time resolution of the data from previous experiments is not adequate for the generation of accurate fade depth and fade duration statistics. A satellite with K_u and K_a band beacons viewed from a low elevation angle would provide the signals needed to generate the statistics mentioned above. The OLYMPUS satellite provides just such an opportunity.

1.2 OLYMPUS Satellite

The OLYMPUS satellite is a European Space Agency (ESA) three-axis stabilized experimental satellite that was launched on July 12, 1989 and placed in geosynchronous orbit at 19° West longitude. In this orbital slot, the satellite is viewed from Blacksburg, Virginia at an elevation angle of 13.9°. This low elevation angle increases the magnitude of atmospheric propagation effects since the signal travels through a large volume of atmosphere.

Four payloads are carried on OLYMPUS. A 12/14 GHz specialized services payload is provided for advanced communications experiments between small earth terminals (VSATs). A television direct broadcast payload with two channels, one for Italian use and one for European use is also carried on-board. Another package, a 20/30 GHz communications payload, is used for point-to-point and multipoint teleconferences and other experimental applications. The final payload is a 12/20/30 GHz propagation package to aid propagation research in the higher frequency ranges[4]. Of these payloads, the 12/20/30 GHz propagation package provides a unique opportunity to study atmospheric propagation effects.

As shown in Figure 1.2 the three beacons provided by the propagation package have the property of being coherent by virtue of a common frequency source. This coherency is extremely valuable for researching the 20 GHz and 30 GHz frequency bands during periods of heavy rain. Since the beacons are coherent, the receiving earth station hardware can be designed to lock to the less fade prone 12 GHz signal and track the 20 GHz and 30 GHz signals down to the noise floor of their respective receivers.

1.3 Desired Experimental Results

The Virginia Tech Satellite Communications Group has identified numerous statistics to be generated from collected data[5]. Of primary importance are fade duration, fade

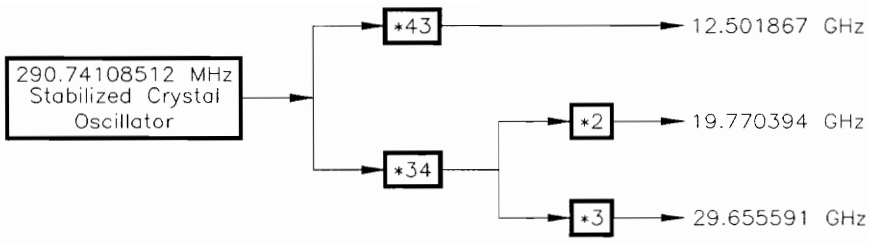

Figure 1.2. OLYMPUS satellite 12/20/30 GHz propagation package frequency plan.

interval, fade slope, and frequency scaling of attenuation. In addition, site diversity, scintillation effects, and uplink power control studies will also be conducted. Even though many analyses will be performed, relatively few data channels need to be collected to generate these statistics. Received beacon signal strength, sky noise temperature and rain rate are the primary data channels needed for analysis.

The major components of the Virginia Tech OLYMPUS experiment are shown in Figure 1.3. The experimental configuration consists primarily of four beacon receivers, four radiometers and two tipping bucket rain gauges. Each receiver outputs a signal representative of the received beacon signal strength. Because the beacon phase noise is quite low, the signal is only several Hertz wide[4]. Therefore, to maximize the signal to noise ratio, the output power is measured in a 3 Hz bandwidth. Under clear air conditions, the output of the beacon receiver is at a nominal level of 0 dB. Signal enhancement, such as that resulting from scintillations, increases the receiver output while rain decreases the output. Even though the receiver outputs a level of 0 dB in clear air, there is still some atmospheric attenuation. This attenuation is measured through the use of a radiometer.

The radiometers chosen for the OLYMPUS experiments are total power radiometers. The radiometer measures the noise power in a frequency band slightly removed from the beacon signal. The noise is assumed to be generated by radiation from molecules in the atmosphere and provides a measure of the absorption by atmospheric gases and water vapor, and hence the attenuation along the signal path. Using calibration information, the noise power is converted to attenuation. This attenuation is then used to calibrate the beacon signal such that 0 dB corresponds to zero atmospheric attenuation. Both the radiometers and the front end RF equipment are highly sensitive to temperature changes and were therefore placed in temperature controlled cabinets. Periodic recording of cabinet temperatures and weather conditions is helpful during data analysis.

Environmental information such as wind speed, wind direction, temperature, rain

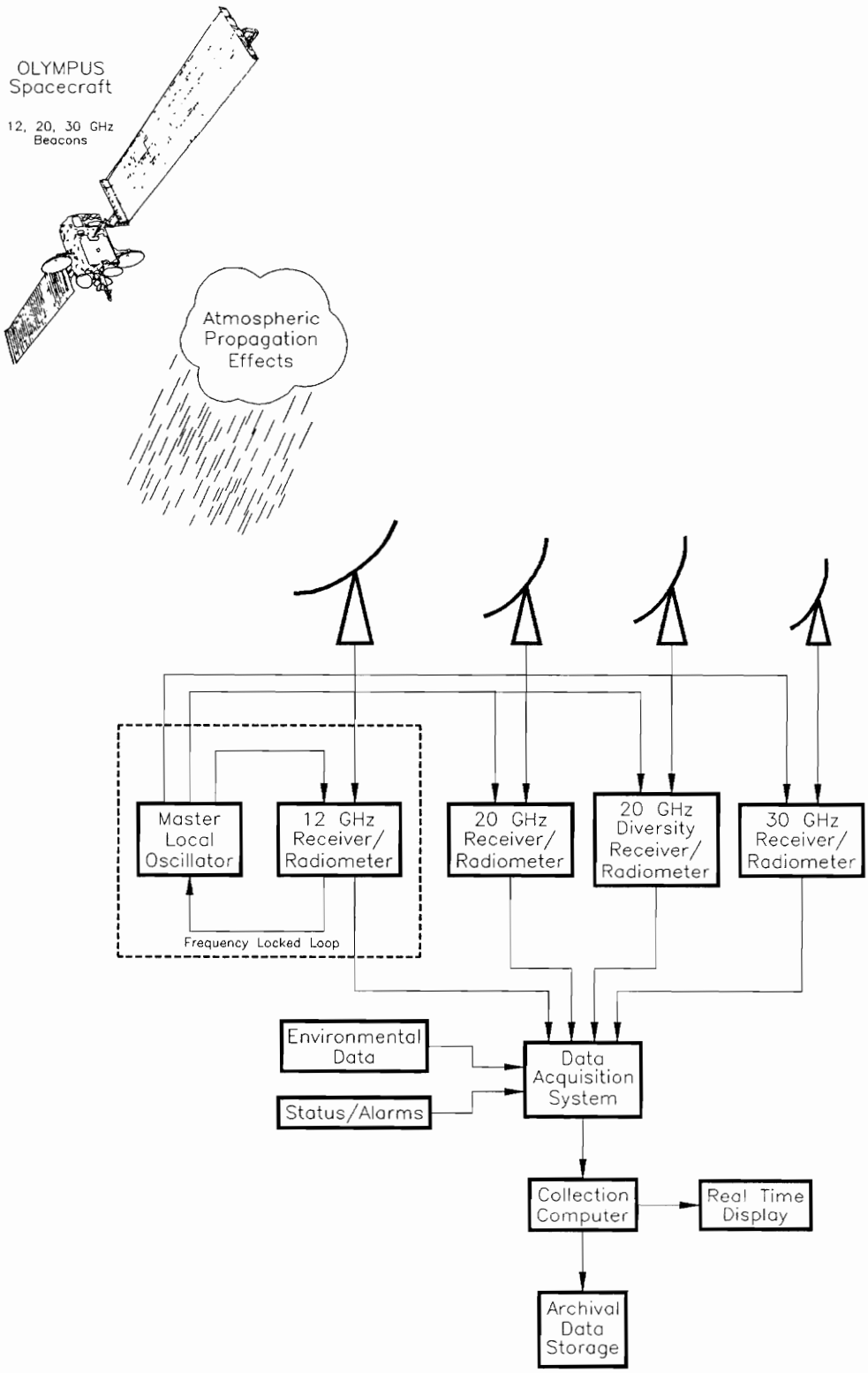

Figure 1.3. Overview of the Virginia Tech OLYMPUS propagation experiment hardware.

temperature, barometric pressure, and humidity is monitored primarily to indicate the passage of storms. Through the synchronous collection of signal and weather information, an expected correlation between scintillation amplitude and weather conditions can be examined. System health is verified by monitoring temperature controlled cabinets, PLO alarms and other status signals. Collection of the data channels described above for future analysis and for control of automated calibration procedures is the responsibility of the data acquisition and control system (DACS).

Figure 1.4 is an overview of data flow in the Virginia Tech OLYMPUS propagation experiments. Experimental data is collected by the DACS and may be displayed in real time. Archived data is input to the preprocessing software which applies calibration information to and locates and flags irregularities in the data. Analysis software then generates numerous statisitical graphs and displays.

1.4 Data Acquisition System

This thesis is primarily concerned with the design, construction, testing, and operation of the DACS for the OLYMPUS propagation experiments. Two tasks are assigned to the DACS: collection of data and execution of timed events. The data collection task continuously acquires and stores beacon strength, radiometer output, system status, and environmental conditions. To reference the collected data to known levels, periodic calibrations are required. These calibrations are considered timed events and are controlled by the DACS. The history of the DACS from its initial design to its present operational state is examined in the remainder of this thesis.

1.5 Overview

This chapter has provided a brief overview of atmospheric effects on satellite communications systems. Rain was shown to be the primary concern in link design for most geosynchronous earth stations. Scintillations are a primary concern for VSAT

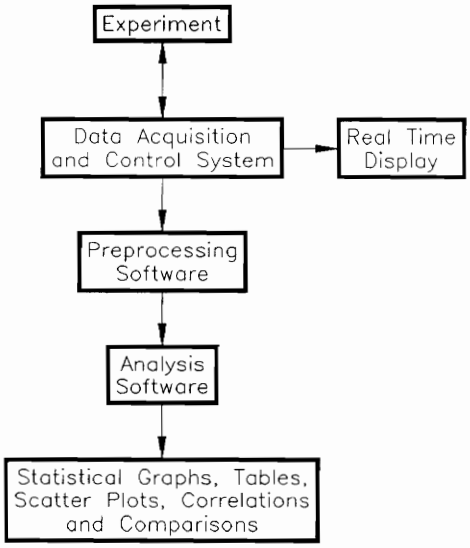

Figure 1.4. Overview of data flow in the Virginia Tech OLYMPUS propagation experiment.

terminals. As a result, future communications links at K_a band will require accurate modeling of short term signal behavior to allow link designers to take appropriate steps to ensure adequate link availability. ESA's OLYMPUS satellite has been chosen as a signal source for Virginia Tech's propagation experiments at 12/20/30 GHz. The OLYMPUS satellite's beacon coherency is used in Virginia Tech's receiver system to keep the 20 GHz and 30 GHz channels locked when their signal level drops into the noise.

Accurately characterizing the effects of rain and scintillations on K_a band signals requires a precise and stable data collection system. The second chapter in this thesis examines the system requirements for the DACS. Initially a list of data channels is presented as well as their respective sampling rates and resolutions. A method of acquisition is then determined for these data. System reliability concerns are addressed and specific design criteria are established. The chapter concludes with a comparison between commercially available data acquisition products and a custom design. The comparison indicates that a custom design is required to obtain accurate beacon signal strength measurements.

Chapter three provides an in-depth description of the DACS hardware beginning with a short history of the hardware development. System-wide design criteria are then established. In addition to the criteria established at the beginning of this project, design techniques subsequently incorporated into the system are presented. A detailed examination of each circuit board and the electrical systems in the DACS is then presented. For each item the complete design requirements are presented. These requirements include functionality, physical size, interface specifications and overvoltage protection. A functional block diagram is then presented. From this diagram and the given requirements, a suitable circuit was derived to meet the design criteria and it is presented in schematic form. An operational description of the circuit is then presented. The discussion of each card concludes with recommendations for future designs.

Software development for the DACS is examined in the fourth chapter. The C programming language along with a minimal amount of 80286 assembly code was chosen for all programs. Functional requirements for each program are then presented. Programming techniques are chosen for each program subfunction and a diagram depicting software flow is presented.

Chapter 5 begins with an operational history of the DACS. Dates when subsystems and functions were added are given with the hope that they may be useful in determining development and construction times for future projects. Uptime statistics are then presented as a measure of system reliability. The thesis concludes by providing recommendations for both improvement to the current design and the design of future data acquisition and control systems.

Chapter 2

System Requirements

Modeling atmospheric effects on 30/20 GHz (K_a band) signals is an area of intense research. Presently, OLYMPUS is the only spacecraft broadcasting coherent beacons both at K_u and K_a band. NASA, however, is scheduled to launch the Advanced Communications Technology Satellite (ACTS) in the second quarter of 1992. ACTS will allow research at K_a band as it carries beacons at nominal frequencies of 20 and 27 GHz[3]. When the satellite becomes operational, NASA intends to fund a number of experimental sites across the U.S. to collect K_a propagation data. To correlate the data measured between experimenters, the experimental sites will be configured identically and maintain accurate time reference by using WWV receivers. Since there will be many sites monitoring the ACTS beacons, distribution of incorrect hardware designs to ACTS experimenters would be costly in terms of time and money. To avoid problems such as these, the Jet Propulsion Lab (JPL), with NASA funding, contracted Virginia Tech to design, construct and operate a propagation measurement system for use with OLYMPUS. Once fully operational, the hardware from the OLYMPUS experiment will be modified for use with ACTS. This system will be replicated and distributed to ACTS experimenters throughout the U.S.

In its OLYMPUS experiment, Virginia Tech is contractually obligated to[6]:

- Measure attenuation of the OLYMPUS 12, 20 and 30 GHz beacons with sufficient accuracy for testing uplink power control algorithms proposed for the ACTS program.

- Measure and characterize site-diversity reception at 20 GHz.
- Collect rain rate information from two tipping bucket rain gauges.
- Operate continuously for one calendar year.

From these requirements, one might assume that only received signal strength and rain rate need to be monitored. However, a number of additional measurements are required to reference the collected data to known levels and to monitor system health and environmental conditions. The next section identifies each of the data channels to be interfaced to the DACS.

2.1 Original Proposal

The Virginia Tech OLYMPUS experiment began in January of 1989 with a contract to produce a system design for a propagation measurement system. The system description which resulted from this contract is different than the presently operational system[7]. The original system specification and the present system are described in this section.

Initially, Virginia Tech proposed to monitor the OLYMPUS propagation beacons with five terminals: 12 GHz, 20 GHz, 30 GHz, 20 GHz diversity and 30 GHz sidescatter. Each terminal was to include an analog receiver and a radiometer. Additionally, a prototype digital receiver designed by Virginia Tech was to be connected to the 12 GHz, 20 GHz and 30 GHz terminals. Digital receivers manufactured by Signal Processors Limited (SPL) were to be connected to the 20 GHz and 30 GHz terminals. Included in the system were instruments to monitor rain, wind velocity, and barometric pressure. Because of budget cuts at JPL, the sidescatter experiment and the purchase of the SPL receivers were deleted from the contract. During 1989 and the beginning of 1990 several system configurations were evaluated. A number of design/redesign cycles were required and in some cases operational circuit boards were scrapped. By the Spring of 1990 a stable system configuration was reached. This thesis examines the design and construction of this final configuration.

The DACS is presently operational and collecting data. Spare I/O channels allocated during the design phase provide additional inputs and outputs for the experiments. All of the data channels are presently recorded by the DACS; unconnected channels are ignored when processing the collected data. Since additional changes will be made to the DACS all future references in this thesis to DACS hardware and software are for the system as of April 1, 1991. Prior to discussing the interface between the DACS and external equipment, system reliability concerns must be addressed.

2.2 Reliability

Reliable day-to-day operation of measurement and control equipment is vital to any long term experiment; the OLYMPUS DACS is no exception. While the primary data of interest has signal variations of a few dB, high attenuation events are also important. These high attenuation events occur during heavy thunderstorms where lightning is present. The data from these events must be collected when the electrical environment for the DACS is worst. Therefore great significance is placed on the uninterrupted collection of data. DACS failures resulting from unstressed component failures are inevitable, however component failures and the degradation of analog signals resulting from external phenomena such as loss of AC power, nearby or direct lightning strikes, and ground loops can be reduced through proper design techniques. Each of these problems will now be examined.

Data collection during a power failure is possible by powering the DACS and the collection computer with an Uninterruptable Power Supply (UPS). The UPS slowly charges a rechargeable battery during normal operating conditions. When the AC line voltage drops below a predetermined level, the UPS disconnects the load from the failing AC line and substitutes a 120 VAC signal generated from the battery. After the AC line voltage returns, the UPS returns to charging the battery. The length of time that the UPS can supply power is dependent on the capacity of the battery and the load connected to the UPS.

Heavy rain, such as that experienced during thunderstorms, yields some of the best high signal attenuation data. The elevated and open location of Virginia Tech's Satellite Tracking Station, makes it a prime target for direct and nearby lightning strikes. Moreover, some of the cables which connect the DACS to outdoor equipment are over 150 feet long. These long cable runs act as antennas and can develop relatively high differential voltages in the presence of lightning. Additionally, incorrect grounding procedures may create ground loops resulting in ground voltage differentials between system units. To reduce the potential for ground loops, the individual grounds for each system unit should be connected together at a common point. In addition to reducing differential ground voltages, a system-wide grounding network provides a low impedance path for energy in the event of a lightning strike. While a direct strike will probably destroy most electronic equipment, the designer should provide protection to limit the extent of damage. In designing a DACS this involves optically isolating digital signal lines and clamping analog signal lines to ground with Zener diodes and MOV varistors. These devices cannot absorb the energy of a direct lightning strike but they may reduce the damage to other components in the DACS.

2.3 Data Channels

Figure 2.1 depicts all channels connected to or planned for interface to the DACS. These signals are categorized as either acquisition or control and analog or digital. Signals observed by the DACS are shown in the left hand side of the figure and DACS generated control signals are on the right. Before proceeding with the acquisition method, resolution, and sampling rate for each channel, some discussion is necessary to describe the signal categories:

- **Beacon:** A bipolar analog 10 kHz sine wave amplitude modulated by the signal strength of the beacon. The signal is bandlimited to a bandwidth of 200 Hz. While the 12 GHz frequency locked loop remains locked, all beacon signals maintain a relatively constant phase relationship with the sample clock.

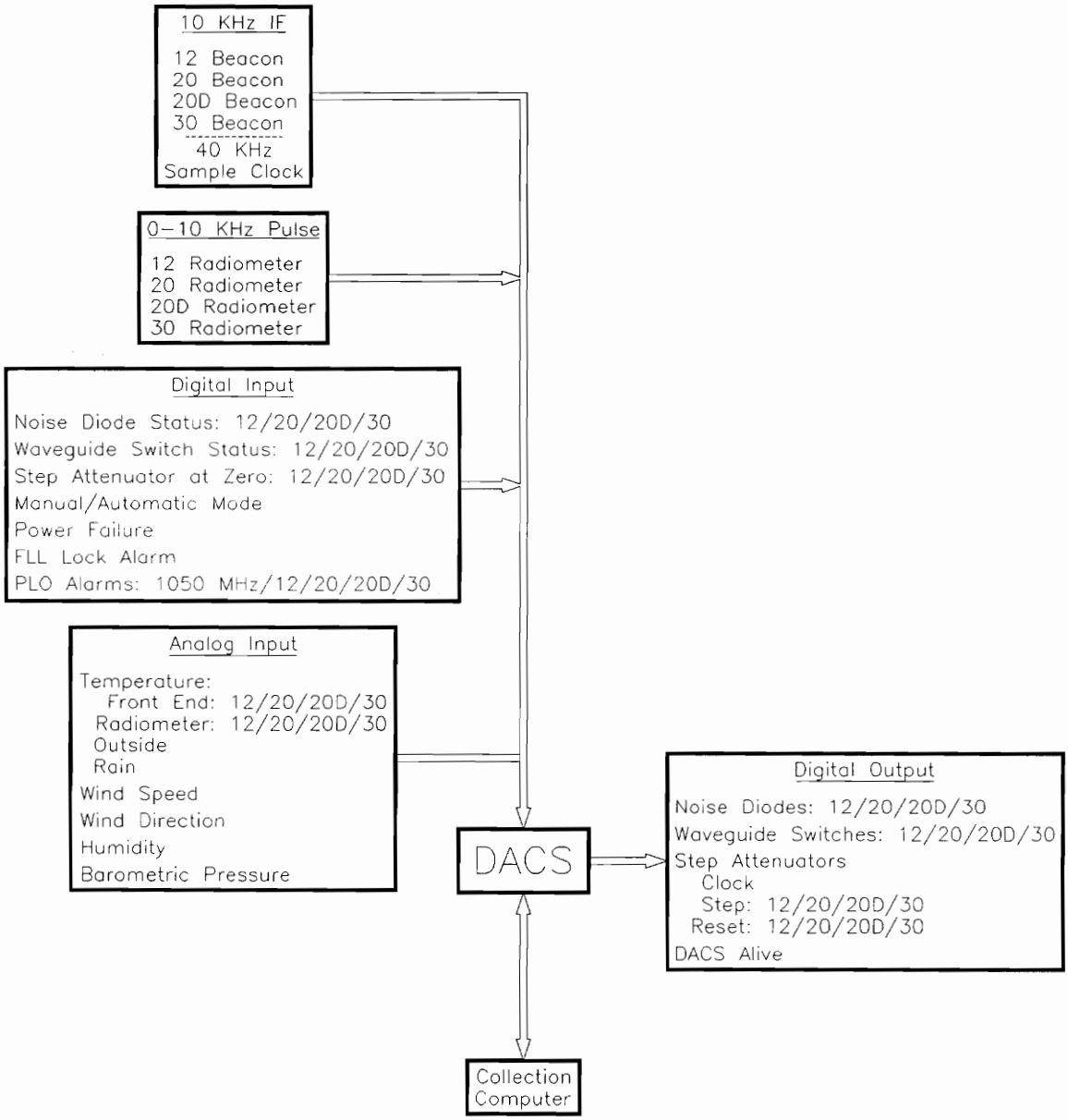

Figure 2.1. Interface connections to the OLYMPUS data acquisition and control system.

- **Radiometer:** A TTL level 0-10 kHz square wave signal proportional to the noise power observed in a 25 MHz bandwidth which is located close to the beacon frequency.
- **Sample Clock:** A TTL 40 kHz clock reference used for detecting the beacon signals.
- **Analog Inputs:** A 0-5 volt analog signal.
- **Digital Inputs:** A continuity sensor.
- **Digital Outputs:** A contact closure.
- **DACS Interface:** Bidirectional digital interface between the DACS and the collection computer.

The DACS interface is not required if the DACS can be located within the collection computer. Prior to locating either off-the-shelf DACS components or pursuing a custom design, the sampling rate for each of the channels was determined.

2.4 Sampling Rates and Resolution

The Nyquist criteria states that to reconstruct a sampled version of a continuous time signal, the sampling rate must be at least twice the highest frequency present in the input signal. If an input signal is undersampled, aliasing will be present in a reconstructed version of the signal[8]. Signals that will not be reconstructed, such as temperature, can be sampled at a convenient rate with the understanding that some input excursions may not be recorded. In contrast, beacon fade rate is a primary statistic which must be measured accurately and must conform to the Nyquist criteria.

2.4.1 Beacons

Measurement of fade rate during sudden attenuation events and scintillation spectra of is primary importance. The beacon channel bandwidth is filtered to one-half of the sampling rate, thus reducing the possibility of aliasing. An extensive review of fade

rate literature and a derivation of the theoretical maximum fade rate is presented in [3]. Sweeney indicates that a sampling rate of 7 Hz is required to accurately characterize fade rate. In practice, 7 Hz is not a convenient sampling rate, therefore for the OLYMPUS experiments the rate is fixed at 10 Hz. There are several reasons for sampling at 10 Hz. First, 10 Hz data can be resampled to rates such as 5, 2, 1 Hz, ... without the need for interpolation. Resampling to one of these rates involves filtering the original data so that it meets the Nyquist criteria and then discarding an appropriate number of samples. Another advantage of the 10 Hz sample rate is that timestamped data can be displayed with a finite number of decimal digits.

ESA recommends sampling beacon power with a resolution of 0.05 dB over the range of -40 to +8 dB. Because most analog-to-digital converters have a linear output, there will always be greater resolution for large input voltages. The number of bits, n, required for the analog-to-digital converter to meet ESA's specification is calculated as

$$n = \left\lceil \log_2 \left[10^{\frac{-\mathrm{SPAN}+\Delta}{20}} - 10^{\frac{-\mathrm{SPAN}}{20}} \right]^{-1} \right\rceil. \tag{2.1}$$

Here, SPAN is the input signal range in dB and Δ is the required measurement precision in dB. Evaluating with SPAN = 48 and $\Delta = 0.05$ yields

$$n = \left\lceil \log_2 \left[10^{\frac{-47.95}{20}} - 10^{\frac{-48.00}{20}} \right]^{-1} \right\rceil = \lceil 15.41 \rceil = 16 \text{ bits}. \tag{2.2}$$

While this derivation indicates that the output data must possess a resolution of 16 bits, beacon power may actually be sampled with less than 16 bits (c.f. Section 4.2.1).

In-phase and quadrature (I-Q) sampling is required to determine the amplitude and thus the power contained in a sinusoidal signal. This is because if a single sample of a sinusoidal signal is taken to determine the power, the sample must occur at the peak of the sine wave. In contrast, two samples separated by 90 degrees constitute an I and a Q sample, the power is formed by $I^2 + Q^2$. Because of design constraints in performing I-Q detection using analog components; namely, long term

stability and dynamic range, the I-Q detection is performed using digital signal processing techniques[9]. For the OLYMPUS experiment, I-Q sampling required uneven sampling points and Virginia Tech chose to build the I-Q detector system in-house.

2.4.2 Radiometers

Total path attenuation is indirectly measured with an instrument known as a radiometer. The operation of a radiometer relies on the conservation of energy: if a medium, i.e. the sky, absorbs energy then it must also radiate energy. The radiated energy takes the form of white noise. By measuring the received power P in a bandwidth B the medium temperature is determined to be[10].

$$T_m = \frac{P}{kB} \quad \text{Kelvin}, \tag{2.3}$$

where k is Boltzmann's constant. However, other sources of noise are also present and thus the apparent sky brightness temperature, T_b, is actually measured. If an appropriate value for T_m can be determined, the total path attenuation is

$$A = 10 \log_{10} \left(1 - \frac{T_b}{T_m}\right) \quad \text{dB}. \tag{2.4}$$

The Virginia Tech design utilizes total power radiometers. This type of radiometer measures the noise present in a frequency band slightly removed from the beacon frequency to avoid including energy from the beacon. Noise power is detected via a square law detector and then amplified to drive a voltage-to-frequency converter (VFC). The pulse train output from the VFC is then counted for a period of T_t seconds and recorded. The RMS resolution of the sky temperature measurement is[10]

$$T_r = \frac{T_s}{\sqrt{BT_t}} \quad \text{Kelvin}. \tag{2.5}$$

Because the system noise temperature, T_s, is different for each of the four systems (12, 20, 20D, 30), different integration times are required to achieve the desired measurement accuracy. To accomplish this requires a DACS while can acquire samples with varying integration intervals.

Since the beacons are sampled at 10 Hz, a data record is generated every 0.1 second. Adding radiometer samples to this data record does not create logistical problems. Therefore, the sampling interval for the radiometers was chosen to be adjustable in steps of 0.1 second.

The VFC 0-10 V input range combined with an output range of 1 kHz/V results in a maximum output frequency of 10 kHz. Allowing for integration periods of up to five seconds requires accumulating a maximum of approximately $5 \times 10^4 = 50000$ counts. The number of bits required to store this count is $\lceil \log_2(50000) \rceil = 16$.

2.4.3 Analog Inputs

Analog input channels are used in the system to collect environmental data and monitor the temperature within controlled cabinets. This information is secondary to the experiment and reconstruction to obtain the actual time varying signal will not be performed. The OLYMPUS research proposal [7] specifies a measurement rate of 0.1 Hz for the analog channels.

The resolution for the analog-to-digital converter (ADC) is determined by examining the input voltage range of each channel, the corresponding range of the physical parameter being measured and the required resolution of the physical parameter. Table 2.1 lists the resolutions for weather data as proposed by ESA[11]. Note that all signals have an input range of 0-5 volts. Therefore, a card configured with an ADC which has a 0-5 volt input span and is preceded by a multiplexer is probably the best design. Recording temperatures with a resolution of 0.1° C requires the most resolution. To resolve temperature differences of 0.1° C requires $\log_2\lceil 5/0.001 \rceil = 13$ bits of resolution. The LM135 temperature sensors used in the OLYMPUS experiment exhibit a calibrated accuracy of 0.3° C[12]. Therefore, sampling temperatures with 12 bits of accuracy yields a slight loss of accuracy.

Table 2.1: Summary of Analog Input Signal Resolutions.

Channel Type	Physical			Voltage	
	Units	Range	Resolution	Range	Resolution
Wind speed	knots	$0 - 50$	0.5 m/s $\approx$ 1 kn	$0 - 5$	0.100
Wind direction	degrees	$0 - 360$	$1°$	$0 - 4$	0.011
Humidity	relative (%)	$0 - 100$	1 %	$0 - 5$	0.050
Temperature	degrees C	$-30 - 50$	0.1° C	10 mV/K	0.001
Barometric pressure	millibars	$950 - 1050$	1 mb	$0 - 1$	0.010

2.4.4 Digital Inputs

Signals such as PLO alarms, waveguide switches and rain gauge tips are digital in nature. The position of the waveguide switch, for example, is indicated by a contact closure located within the waveguide switch. Since some of these input sources are located 150 feet from the DACS, electrical noise and inductive pickup are significant. To avoid damage to the DACS, all digital inputs are optically isolated. Since some error conditions may exist for less than one second, all digital inputs are sampled at 10 Hz. Thirty-two input channels are provided to fulfill present requirements and allow for expansion. Those inputs connected to rain gauges require latches to guarantee that all tips are recorded.

2.4.5 Digital Outputs

The DACS must provide a method to automatically perform system calibration by controlling noise diodes, waveguide switches and step attenuators. Noise diodes and waveguide switches, which are used to calibrate the radiometers, are easily controlled since they are either on or off. Step attenuators used for determining system linearity are configured such that digital control is possible. A step attenuator consists of a stepping motor which controls a rotary waveguide attenuator. To change the attenuator setting, a common step clock is used to drive the stepper motors for all systems (12, 20, 20D and 30). When the clock is active, an enable line causes the stepping motor to advance. Motion and hence attenuation is halted by either removing the clock source or the enable signal. No provision exists for stepping the attenuator in the reverse direction; a reset line that returns the attenuation level to 0 dB is provided. The clock must be present while the stepping motor controller is returning the attenuation level to 0 dB. As with the digital inputs, the digital outputs are optically isolated for noise immunity. Thirty-two channels are provided to fulfill system requirements and allow future expansion.

2.4.6 DACS Interface

The DACS interface may assume a number of different forms. If the acquisition and control system is directly compatible with the control computer bus, a DACS interface is not required. However, a standalone DACS requires some type of interface. If an interface is required, it should electrically isolate the DACS from the control computer. This can be done in a number of ways. Differential drivers would provide a measure of noise immunity and ground isolation while optoisolators result in several thousand volts of isolation. The ideal solution, a fiber optic link, would completely isolate the DACS from the collection computer.

2.4.7 Requirements Summary

The preceding discussion determined the sample rate, resolution, and type of interface for each of the DACS channels. Table 2.2 presents this in summary form. Using this information a comparison can now be performed between purchasing an off-the-shelf system, building a custom system, or perhaps a hybrid of the two.

2.5 System Components

Cost, performance and reliability specifications must be made prior to purchasing the control computer and equipment for use in the DACS. Selection of a control computer is the first component examined. Price comparisons are then presented for commercial products suitable for a DACS. A short description follows which details a custom DACS proposed by Virginia Tech.

2.5.1 Collection Computer

Since propagation data is collected continuously, the control computer must be able to operate for weeks at a time without error. IBM computers have consistently exhibited reliability unsurpassed by most of the clones in the marketplace. Coupling this with

Table 2.2: Summary of DACS Interface Signals.

Channel Type	Quantity	Characteristics	Rate (Hz)	Output Resolution
Beacon	4	Bipolar Analog	10	16 bits
Analog Input	32	0-5V Analog	0.1	12 bits
Radiometer	4	TTL Pulse Train	10/n	65536 counts
Digital Input	32	Optoisolated	10	—
Digital Output	32	Optoisolated	10	—
DACS Interface	1	Isolated	—	—

the future end of maintenance on IBM AT computers, the control computer chosen for this project is an IBM PS/2 Model 60-041. The Model 60-041 is a 10 MHz 80286 based system with a 41 MB hard disk. The system was chosen because it provides eight expansion slots and operates with a relatively high level of performance. Two megabytes of extended memory was purchased to allow the use of the OS/2 operating system. Subsequently, the choice of operating system has reverted back to DOS. While DOS does not require the extra memory for operation, the 2 MB is now used to buffer data during operation. Additionally, in the Fall of 1987 Virginia Tech required freshman engineering students to purchase IBM PS/2 computers for use with classwork. Because of this, a PC maintenance shop has been established at Virginia Tech and it can effect repairs to IBM PS/2 computers within several days.

2.5.2 DACS

Many factors influenced the decision between purchasing a commercial system and pursuing an inhouse custom design for the DACS. A commercial system can be assembled within a short period of time and will give predictable reliability. The cost of commercial products may appear high at first. However, the nonrecurring cost of an engineers time to design, build and test a custom design will most likely exceed that of a commercial product. For this research project, labor costs are to some extent fixed.

Labor Costs

Graduate students are usually funded for the length of a research project. During this time, each student is expected to research, design, build, maintain and document their portion of the project. While many hours of labor may be required to perform these tasks, the student is paid a fixed salary and expected to complete their task on schedule. Therefore, if only one student is funded for each area of the project, such as the DACS, the labor costs can be considered a fixed expense.

Commercial vs. Custom

One aspect of Virginia Tech's design – the hybrid analog/digital receiver – is inherently a custom circuit and was designed to interface with the DACS chosen. As this circuit represents a large portion of the DACS effort, design and construction of a custom DACS may be feasible. Before the decision to pursue a custom design could be made, components from several vendors were examined.

Ideally, several interface cards which provide the necessary data and control channels are desired. However, after examining product catalogs from several manufacturers (Burr-Brown, CyberResearch, Data Translation, Keithley MetraByte/Asyst/DAC, Octagon Systems), it became clear that five or more interface cards would be required to satisfy the DACS channel requirements. This applies both to PC and PS/2 type cards. Thus the choice to use an IBM PS/2 for the control computer did not solely eliminate the ability to place the DACS within the control computer.

The PS/2 Model 60 has eight expansion slots, of these one is used for the hard drive controller, one for the tape controller and a third for a memory expansion card. Of the five remaining slots, two should be left free for future expansion. Since this leaves only three slots free, the DACS must be external. An external DACS interfaces to the control computer through either a parallel or serial data port. DACS control and sampling can be performed either by the PS/2 or by a microprocessor contained within the DACS. PS/2 based control is inadvisable because of difficulties in using interrupts to generate precise sampling intervals. Additionally, foreground applications executing on the PS/2 exhibit slower performance because of the sampling and control process executing in the background.

Keithley MetraByte/Asyst/DAC and Octagon Systems Corporation are two producers of standalone DACS systems. Price comparisons for DACS systems from these two companies will now be presented. In the following comparisons, only those components of significant cost are included since the cost of small items such as mounting hardware and miscellaneous connectors remains relatively constant between different

systems.

Keithley produces several different types of standalone control and measurement system components. The three product lines are the Series 500, WorkHorse, and MetraBus[13]. The least costly MetraBus components are used for this price comparison. Prices for a suitable system are shown in Table 2.3.

Octagon Systems manufactures cards which interface to the STDBUS. Assembling a DACS system requires a CPU card, an interface to the PS/2, and interface cards for the data and control channels. Table 2.4 lists the components and costs for a DACS from Octagon Systems.

A custom DACS has advantages and disadvantages. One of the primary concerns is cost. In an industrial situation labor costs and the time required to design, build and debug a custom system is usually prohibitive. This is especially true if short deadlines are present and a system which can be configured to perform the task is available using off-the-shelf components. If, however, the required acquisition and control functions are not available, a custom system is the only solution. Virginia Tech's propagation experiments include a hybrid analog/digital receiver (I-Q detector) that is inherently custom.

The I-Q detector digitally filters data sampled at a non-uniform rate. Commercial digital signal processing systems which can perform this task cost approximately $2000. Since there are four beacon channels, the cost of the I-Q detectors approaches $8000. A preliminary analysis indicates that the hardware cost for a single channel custom unit is about $300. Therefore, the I-Q detector was chosen to be a custom design.

A custom design matches the needs of the user and reduces costs by eliminating unneeded functions. However, the reliability of a custom system is usually less than that of a commercial product. Virginia Tech's preliminary design for a custom system involves the use of STDBUS type cards which plug into a backplane. Since only one of each type of card, i.e. analog input, digital output, is required, the cards

Table 2.3: Metrabyte DACS Components and Costs.

Model Number	Description	Quantity	Unit	Total
INTMDB-64	Standalone Controller	1	450.00	450.00
MIO-32	Digital Output Card	1	295.00	295.00
MII-32	Digital Input Card	1	265.00	265.00
MCN-8	Counter/Timer Card	1	575.00	575.00
MAI-16	Analog Input Card	2	695.00	1390.00
MBB-32	Prototype Board	1	295.00	295.00
PWR100/115	Power Supply	1	595.00	595.00
RMT-04	Rack Mount Enclosure	2	295.00	295.00
	MetraBus Cable	1	75.00	75.00
	Connectors			250.00
				4485.00

Table 2.4: Octagon Systems DACS Components and Costs.

Model Number	Description	Quantity	Unit	Total
7308	Counter/Timer Card	2	225.00	450.00
9510-1	CPU Card	1	645.00	645.00
860	Analog Input Card	1	550.00	550.00
832	TTL I/O Card	1	225.00	225.00
920	Extender Card	1	68.00	68.00
CMA-26-24	I/O Rack Adapter	3	18.00	56.00
G4-IDC5D	DC Input Optoisolator	32	8.99	287.68
G4-ODC5	DC Output Optoisolator	32	8.50	272.00
RM-24	Rack Mount Card Cage	1	190.00	190.00
MB-12	12 Position Motherboard	1	150.00	150.00
PS-110-R	110W Power Supply	1	295.00	295.00
OM-X	Hardware Manuals	1	70.00	70.00
	Rack Mount Chassis			200.00
	Connectors			250.00
				3708.68

were wirewrapped instead of fabricated on circuit boards. The decision to wirewrap decreases development time by eliminating the time required to layout a circuit board. However, a wirewrapped card generally exhibits more electrical noise than a circuit board designed with full power and ground planes. Through careful wiring and layout of parts, the noise present on a wirewrap card can be reduced to acceptable levels.

Virginia Tech's custom DACS design includes six types of cards: one 32 channel analog input, one 32 channel digital input, one 32 channel digital output, one radiometer input, two I-Q detectors and one control microprocessor. Because development tools and an emulator for the Intel 80286 microprocessor are owned by the research group, the control computer was chosen to be 80286 based. The microprocessor samples data channels and generates control signals at appropriate intervals and sends the data samples to the collection computer for storage to disk. The estimated total cost of the Virginia Tech custom DACS is $6000[6].

2.6 Pursue Custom DACS

Based on the cost estimates presented above, experience with commercial data acquisition products, and the consent of our contract monitor, Virginia Tech chose to pursue a custom DACS. Recall that from the time this decision was made to the completion of the DACS, numerous changes were made to several of the interfaces. Because the DACS is custom, it was easy to conform to the changing interface specifications. The custom DACS has proven itself capable of reliable operation and relatively easy to service for the occasional failed component.

Specifications and designs for each subsystem of the DACS are presented in detail in Chapter 3. Software development for the I-Q detectors, control microprocessor and collection computer is presented in Chapter 4. Chapter 5 concludes this thesis by presenting reliability statistics for the DACS, examples of collected data and recommendations for the construction of future data acquisition and control systems.

Chapter 3

Hardware Development

The system definition and method of implementation discussed in Chapter 2 showed that the DACS should be a custom built unit which is external to the PS/2 data collection computer (CC). The DACS will autonomously sample and control selected channels at prespecified intervals. Once the system requirements were determined a hardware architecture and design methodology was chosen. Each component of the DACS is presented in this chapter first in block diagram form and then discussed in detail.

3.1 DACS Architecture

Virginia Tech's DACS design is centered around the Intel 80286 microprocessor and loosely based on the STD interface bus. The 80286 microprocessor was chosen for the control computer, hereafter known as the backplane control computer or BCC. The I-Q detector card was also designed with an 80286 because development tools for the 80286 were available within the research group. Additionally, the 80286 is the same processor used in IBM AT class computers thus allowing software to be developed with the same assemblers and compilers that are used with IBM PC computers.

From a hardware standpoint, the DACS is divided into two sections: the collection computer and a rack mounted unit. Figure 3.1 shows the location of components within the system. The following sections examine the design and operation of these

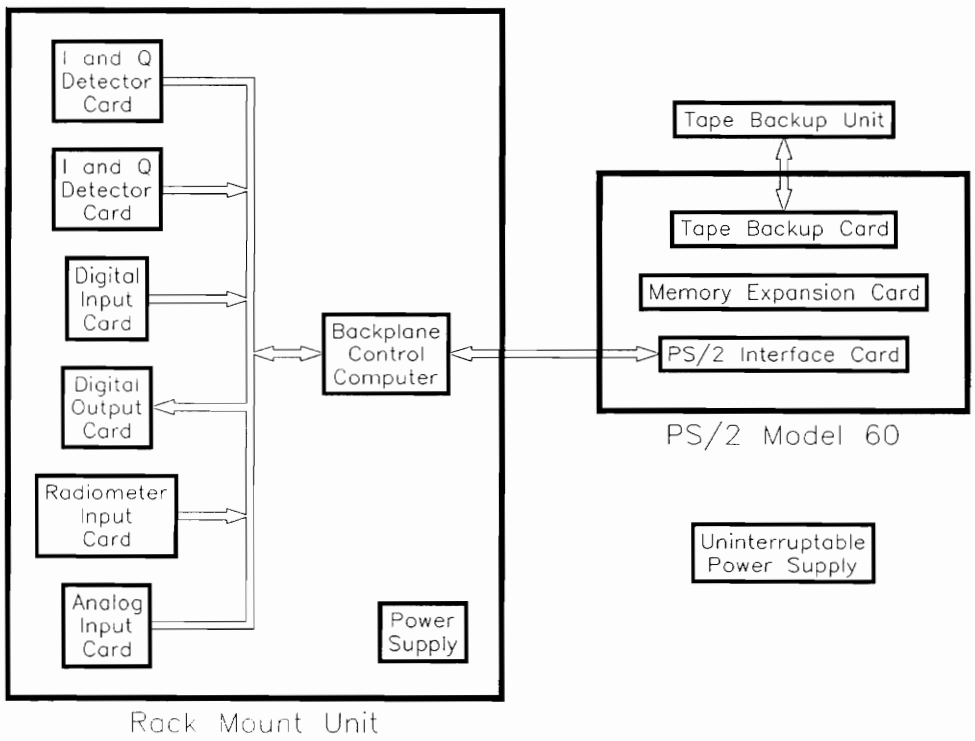

Figure 3.1. DACS subsystems.

DACS components.

3.2 Design Methodology

In designing and constructing the DACS a number of circuit techniques were utilized to improve reliability and ease construction and maintenance. Each subsystem was designed as an independent unit to allow maintenance of a portion of the DACS while data collection and control continued on the remaining data channels. Physically, each subsystem was either fabricated on a circuit board or wirewrapped in a uniform manner. Steps were taken to ensure that electrical noise and lightning induced voltages would cause the least possible degradation of measurements and/or circuit damage. Input and output connections were designed to allow easy removal of subsystems for servicing, testing or calibration. All I/O lines were either optically isolated or utilize breakdown devices to prevent excessive voltages from damaging the remainder of the DACS.

3.2.1 Independence

The DACS was constructed in a manner that allows the system to operate when a subsystem, i.e. a radiometer input card, is temporarily removed for maintenance. As result, each subsystem must function independently except for, of course, the backplane control computer (BCC). Therefore, internal signals derived in one of the subsystems should not be required for operation of another subsystem. The repetition of circuitry added some incremental cost, yet savings will be realized through simpler maintenance and less DACS downtime.

3.2.2 Card Construction

All circuit boards were designed to fit into a common backplane interface. For economic reasons it is not feasible to fabricate circuit boards for each of the unique units.

Those cards of which only one was required were wirewrapped in a manner that allowed easy debugging, maintenance and if necessary modification. All components other than those used to reduce electrical noise and provide circuit protection from lightning were socketed. On the wire side of the wirewrap boards, each of the sockets has a wirewrap ID which uniquely identifies the component. Wirewrap wiring was performed using four colors of wire: red, blue, yellow and white. Red and blue were used for power and ground respectively. Digital signal lines were implemented using yellow wire whereas white was used for analog lines. Because STDBUS type cards with ground and power planes were not readily available, those cards which are either analog or exhibit excessive electrical noise required the inclusion of heavy ground connections between components. Most importantly, zener diodes were placed on each card at the point where power enters the card and after all on-card voltage regulators. These diodes attempt to shunt excess voltage to ground in the event of power supply failure or a lightning strike. As the STDBUS is not inherently polarized, the edge connectors on all of the cards are keyed to prevent incorrect installation.

3.2.3 I/O Connections

The DACS is connected to both analog and digital devices. Isolating digital signals is easily performed through the use of optical isolators. These devices provide over 1500 V of isolation and can also provide translation between different voltage levels. Differential drivers provide some measure of isolation and are particularly effective when using twisted pair transmission line between systems with isolated grounds. Isolating analog signals requires techniques such coupled transformers and voltage-to-frequency conversion followed by an optical isolator and then frequency-to-voltage conversion[14]. Moreover, for these methods to work there must be electrical isolation between the power and ground of the information source and the DACS. Since all electrical systems within the OLYMPUS experiment are connected through a grounding network, true isolation is not possible. For the purposes of constructing the DACS,

analog signals are protected through the use of zener diodes. Unipolar signals have a single zener diode across the signal line to ground. The bipolar beacon signals require two back-to-back zener diodes which are shorted to ground. Using two diodes allows negative signal excursions and provides clamping for both excessive positive and negative transients.

3.3 DACS Subsystems

The following sections provide an in-depth description of the requirements, design, construction and testing of the DACS hardware components. For each of the electrical systems, the requirements as determined in Chapter 2 are presented. A functional block diagram for the subsystem is then shown. A specific method of implementing the design in hardware is then determined. Block diagrams are given in this chapter, while schematics are contained in Appendix A. From these schematics, each of the circuits was then wirewrapped or fabricated on a circuit board.

Since the DACS is an external unit, an interface between the DACS and the collection computer must be utilized. The interface must provide error free bidirectional data transfer. Additionally, collection computer resources should not be heavily loaded in operating the data link. Most significantly, the DACS should be electrically isolated from the collection computer. Isolation prevents transients, such as those resulting from lightning and ground loops, from creating differential voltages between system components.

Electrical

To reduce the possibility of ground loops and to provide a measure of noise immunity, differential line drivers and receivers are used for the data link. Signal lines are driven to RS-422 levels (0 V and 5 V) using 26LS31 line drivers. 26LS32 line receivers provide a hysteresis of 200 mV and can operate with a common mode or differential input voltage of ± 7 V[15]. During the DACS preliminary design and testing, no direct

connection between the BCC system ground and the CC ground existed. This was done with the incorrect assumption that the differential drivers could handle the large differential and common mode voltages present during a thunderstorm. A nearby or direct lightning strike on June 22, 1990 destroyed a large portion of the DACS and CC. This strike demonstrated that differential drivers could not handle the large differential voltages. As a result, a heavy gauge grounding strap was added which connects the DACS ground directly to the CC ground. Since this modification, no components failures have resulted from lightning.

Initial calculations indicated that the data rate between the DACS and the CC would exceed 10000 bits/second[6]. Since serial communications are most reliable below 9600 baud, the decision was made to employ a sixteen bit wide parallel data link. Sixteen bit wide data transfers decrease loading on the CC by requiring half as many interrupts as an eight bit link. By reducing the number of interrupts, more time is available for foreground processes such as real time data display and data archiving.

Figure 3.2 illustrates the sequence of signals between the DACS and the control computer. Note that the data flow is in both directions. The DACS to collection computer interface requires 22 signal lines. Since the data link is differential, a total of 44 physical lines are used. In the following discussion of the data link operation, reference to a signal also includes its complement. A signal without a bar over its name, X, is active high and those with a bar, i.e. $\overline{X}$ are active low.

Theory of Operation

When the data acquisition and control system is first started, configuration information must be sent to the BCC. Specifically, the time and date are required to ensure that timed events occur at the correct time. Prior to transmitting this data, a hardware reset should be performed for the BCC. Under normal operating conditions this is not necessary as the BCC will automatically reset when power is first applied. If

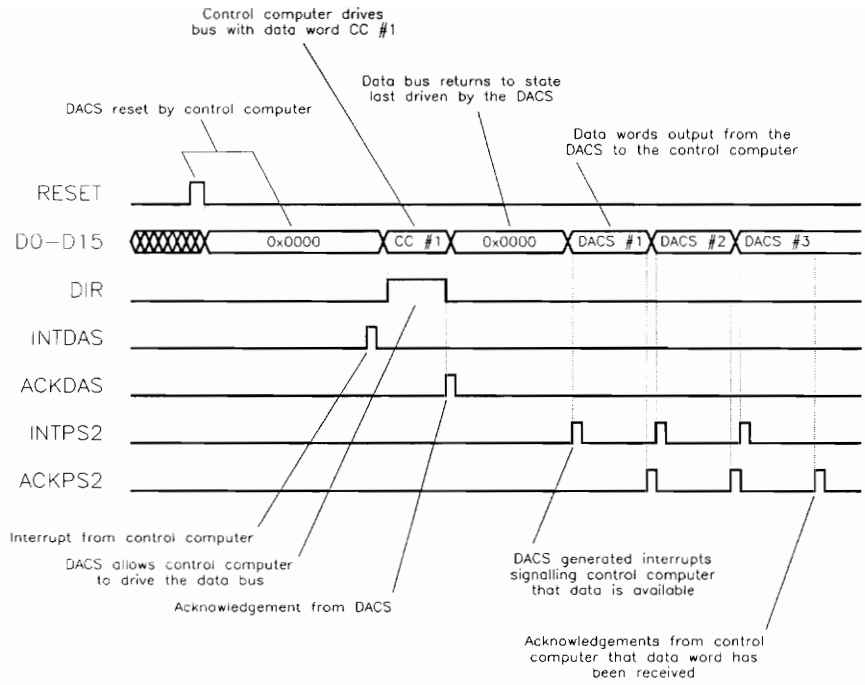

Figure 3.2. Sequence of DACS to BCC interface signals.

however, the CC is collecting data and the flow of data from the BCC ceases for more than 10 seconds, the CC infers that the BCC has crashed. The CC then forces a hardware reset on the BCC, downloads the appropriate configuration information and resumes data collection. The hardware reset is forced by the CC pulsing RESET.

A hardware reset causes the BCC to initialize internal data structures and wait for the CC to transmit the current time and date. At this time, the BCC writes a value of 0x0000 to the DACS data link drivers. D0 through D15 carry bidirectional data where D0 is defined as the least significant bit. DIR is a DACS generated signal which determines whether the BCC or the CC is permitted to drive the data bus. When DIR=1, the CC is permitted to drive the data bus. When the DACS is not receiving data from the collection computer, DIR=0 which allows the BCC to send data samples to the CC. Since DIR is used to enable both the CC and BCC data link drivers, bus contention is not possible.

As shown in Figure 3.2, the CC sends data to the BCC by latching the desired word into the CC data link latches and pulsing INTDAS. Upon receiving this interrupt, the BCC sets DIR=1, reads the word from the data link, returns DIR to 0 and buffers the data word for parsing and command execution. Data transmission from the BCC to the CC occurs in a similar fashion. The BCC places the data word onto the link and pulses INTPS2. The CC then reads and buffers the word and pulses ACKPS2 to signal that the data has been received.

To ensure that incorrect commands or data are not received, all data that is transmitted between the two computers is sent in packet form followed by a checksum. Presently, data received by either computer that is not a legal packet or has an incorrect checksum is discarded and no retransmission is attempted. Because of time constraints in bringing the system online, insufficient development time was available to fully implement a packetized data transfer algorithm. Additionally, the interrupt service routine (ISR) executing on the CC is unable to determine whether a received packet is correct. Data validity checks are performed by a parser which

reads the contents of a buffer written by the interrupt service routine. Since there may be a delay of several minutes from the time a packet enters the buffer until its validity is determined, some method of requesting a retransmission of a previous packet is required. An algorithm to perform this task is not complicated and could be integrated into the present DACS. However, an analysis of data collected since the DACS became operational indicates that fewer than 100 packets have been lost for undetermined reasons. This, coupled with an expected downtime of several days, suggests that modifying the BCC and CC software to perform retransmissions is not cost effective.

Hardware

The differential data link connecting the BCC to the CC uses fifty conductor flat ribbon cable, DB50 connectors and fifty pin circuit board headers. The signal assignments for the ribbon cable are such that differential signal pairs are adjacent. This adjacency helps to reduce coupling between signal lines.

3.3.1 PS/2 Interface Card

The PS/2 interface card is responsible for communications between the collection computer and the backplane control computer. The design for this card is based on the previous discussion of the DACS to PS/2 interface and the requirements for interfacing to the PS/2's Microchannel interface bus.

Microchannel Architecture Considerations

Unlike most personal microcomputers, the IBM Microchannel interface bus timing is asynchronous[16]. As a result, the relationship between data, control and status signals is variable. Another feature of the Microchannel bus is the use of shared interrupts. When using shared interrupts, multiple devices may generate an interrupt on a common channel. The interrupt service routines associated with the particular

interrupt are then called in sequence until one claims ownership of the interrupt. This is usually performed by having a status bit on the card which indicates that an interrupt is pending. Address mapping and configuration of interface cards on the Microchannel bus is performed differently than most PC bus cards.

Cards for use with the Microchannel bus are configured through software rather than with hardware jumpers. This configuration process occurs when the system is reset and relies on the fact that cards for use with the Microchannel bus are each assigned a unique identification code. By checking each slot for the existence of a card and then downloading to the card previously stored configuration data, system setup is simplified. However, designing an interface card which meets the requirements set forth by IBM is non-trivial. Fortunately, commercial prototyping cards are available that provide latched data, address and the necessary control signals.

Design

There are several design requirements for this card. First, the data path between the PS/2 and the DACS should sixteen bit wide differential data to facilitate rapid data transfer. Data transfer is differential to provide a level of noise immunity and isolation. In addition to data, bidirectional control signals are required to allow for resetting the BCC and for data handshaking. To reduce loading on both the CC and the BCC, all communications should be interrupt driven. Using interrupts is the only viable method to perform communications in a realtime application.

For the DACS interface, a prototype card from JDR Microdevices (part number JDR-PR16) was chosen. This card isolates the user from the Microchannel interface bus and provides a limited amount of configuration through software control. One important difference between the JDR card and IBM's requirements is that JDR's card does not respond with an adapter ID during system configuration. Because of this, the card does not exist as far the system is concerned and user written software must configure the card prior to operation.

A block diagram for the card is shown in Figure 3.3. Eight bits of data, programmable option select, the microchannel interface control and status logic and some address decoding is provided on the JDR prototype card[17]. The remainder of the circuitry implied by the block diagram must be designed and added to the prototype card.

Circuit Description

The DACS to PS/2 interface card is logically divided into three sections: interface, receive and transmit. The receive and transmit sections convert differential RS422 data into TTL levels and vice versa. TTL level data and the necessary control and status signals are connected to the Microchannel interface bus through the interface section of the card. The schematic for the interface card is shown in Figure A.1. It may be helpful to refer to this schematic during the following description.

Interface The DACS to PS/2 interface card facilitates the transfer of 16 bit data between the DACS and the PS/2. Interfacing to the Microchannel bus of the PS/2 is the most complicated portion of the card. While much of the necessary logic is provided by the JDR prototype card, some additional circuitry and several modifications to the prototype card are necessary.

Because the prototype card supports only eight bit data transfers, the data path must be increased to 16 bits. Octal buffer U25 was added to supplement the eight bits of buffering provided by U1. The logic generated by gates U14F, U24B and U14E and the modification stated in the note on the schematic prevents U1 and U25 from driving the PS/2 data bus during power-on configuration. Without this gating, the PS/2 frequently detects the card, is unable to locate the appropriate configuration information and halts with a system configuration error. U14B and U27B enable the data buffers between the Microchannel data bus and the on-card data bus and drive $\overline{\text{CDDS16}}$ low indicating to the PS/2 that a 16 bit port is selected for a read or write

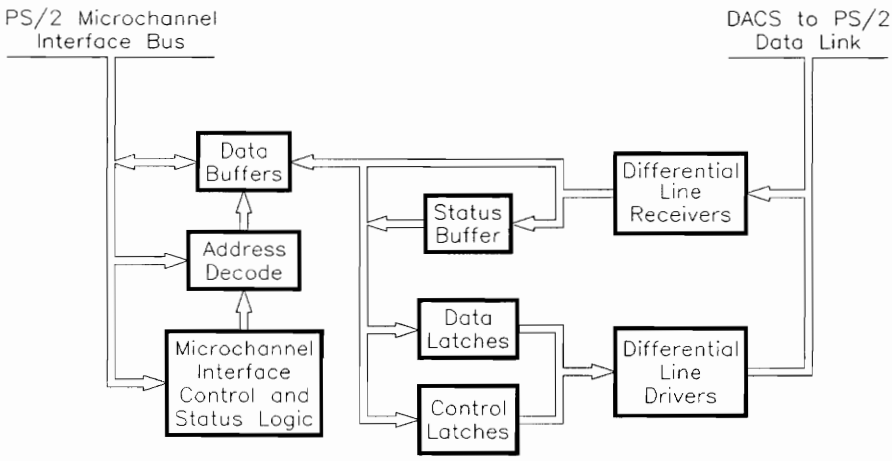

Figure 3.3. Block diagram of the PS/2 interface card.

operation. U13 is a three bit demultiplexer that allows access to various read and write registers and resets interrupt and acknowledge flip-flops.

Receive 26LS32 line receivers convert the differential signals present on the data link into TTL levels. The status signals from the DACS: DIR, ACKDAS and INTPS2 are received via U19 which is always enabled. DIR controls ownership of the data link. When DIR=1, transfers from the PS/2 to the DACS are allowed, otherwise data flows from the DACS to the PS/2. U21A and U21B latch INTPS2 and ACKDAS respectively and are cleared through a read operation to the card. In addition, INTPS2 is also cleared by CHRESET during system reset. U20 is enabled by a word read to address 0x7F2 and places DIR and the latched versions of ACKDAS and INTPS2 in the low order bits of the data word. Data from the DACS is read through address 0x7F4 by enabling the output of U15-U18.

Transmit The PS/2 generated control signals INTDAS, ACKPS2 and RESET are latched by U23 upon detected a write command to address 0x7F2. To prevent the control signals, especially RESET, from having glitches during writes to the control port, a non-transparent 74LS374 latch is used for U23. The output of U23 drives a permanently enabled 26LS31 differential line driver. Data for transmission to the DACS is latched into U22 and U26 by a write to address 0x7F4. The output of U22 and U26 is controlled by DIR and prevents the on-card data bus from being driven when data is being read from the DACS. This is necessary because the line drivers and receivers are located on a common data bus. Failure to disable U22 and U26 will result in bus contention and an inability to receive data from the DACS.

Results

The PS/2 interface card is one of the most modified cards in the DACS. Most of these changes were performed in an attempt to prevent the PS/2 from detecting the presence of the card during power-on selftest. If the card is detected, the card ID

number read by the PS/2 is meaningless since no configuration information exists for the card. As a result, a configuration error is displayed and the system halts. Presently, this type of error occurs infrequently. Simply turning the system off and then back on removes the error condition.

Another problem involves the bidirectional transfer of data. Initially, the DACS was to have been programmable for setting the channels to sample, sample rate, etc. Additionally, data transfer between the PS/2 and DACS was to be performed using packetized data and checksums. Hence errant data would be detected and a retransmission would be possible. However, the use of a common local data bus on the PS/2 interface card coupled with DACS control of data flow, has made reliable bidirectional data transfer virtually impossible. Since errant data packets are virtually non-existent the incorrect data is discarded and no retransmission is attempted. To solve this problem, and to simplify the design, debugging and maintenance of future data acquisition and control systems, a serial data link is highly recommended. A serial link requires only three wires between CC and DACS, can provide electrical isolation through the use of fiber optic cable, and can be implemented using several commercially available integrated circuits, e.g. 8251, baud rate generator, line driver and line receiver.

3.3.2 Backplane Architecture

To provide for expansion capabilities and simplify maintenance, interfacing external equipment to the DACS is accomplished through individual circuit boards which have a specific function. All cards interface to the BCC using a common backplane interface. By common, it is meant that an interface card may be placed in any slot and it will function correctly. The bus specification chosen for the DACS is loosely based on the STDBUS.

Electrical

The STD interface bus specification consists of signal assignments for a passive backplane. The definition provides for an 8-bit data bus and a 16-bit data bus[18]. As the number of channels foreseen for the DACS is less than 256 and 16-bit wide data transfers are more efficient, Virginia Tech has chosen to modify the STD bus specification. Table 3.1 shows the differences between the STD bus backplane configuration and the Virginia Tech implementation. The major difference between the STD bus specification and the Virginia Tech implementation is the reversal of the data and address buses. Additionally, careful inspection shows that the Virginia Tech specification differs in that some of the pins pairs, i.e. A7/A3, are reversed as compared to the STD bus specification. This is because the backplane interface connector on the I-Q detector card was specified incorrectly when the circuit board was fabricated. Since only the backplane control computer existed when the I-Q detector was being tested, the specification for the bus was modified to avoid cutting and rewiring approximately 20 traces on the I-Q detector cards. These modifications have not affected the system design other than slightly complicating the debugging process.

Excluding the address and data buses, ten signal lines are present on the backplane. READ and WRITE are driven by the BCC and either request that data be placed on the data bus or signify to an interface card that the data on the bus is valid. $\overline{\text{STATUS}}$ is an open collector signal driven by an interface card when its address is present on the address bus. TYPE is a three bit binary word that is also driven when that card is selected and indicates to the BCC the type of card which is present. Initially, it was envisioned that some form of error checking would be performed to prevent sampling or controlling an interface card of the wrong type. Error checking is not presently implemented, but each type of interface card does output a unique card type. Presently assigned card types are listed in Table 3.2.

All interface cards other than the I-Q detectors, are able to provide data virtually instantly. The I-Q detector cards, however, must execute an interrupt service routine

Table 3.1: Virginia Tech Backplane Interface Bus Specification.

Pin	STDBUS	Virginia Tech	Pin	STDBUS	Virginia Tech
1	Vcc	+5	29	A0	D8
2	Vcc	+5	30	A8	D0
3	GND	GND	31	$\overline{\text{WR}}$	READ
4	GND	GND	32	$\overline{\text{RD}}$	WRITE
5	VBB #1		33	$\overline{\text{IORQ}}$	
6	VBB #2		34	$\overline{\text{MEMRQ}}$	
7	D3	A7	35	IOEXP	
8	D7	A3	36	MEMEX	
9	D2	A2	37	$\overline{\text{REFRESH}}$	$\overline{\text{STATUS}}$
10	D6	A6	38	$\overline{\text{MCSYNC}}$	
11	D1	A1	39	$\overline{\text{STATUS1}}$	TYPE2
12	D5	A5	40	$\overline{\text{STATUS0}}$	TYPE1
13	D0	A4	41	$\overline{\text{BUSAK}}$	TYPE0
14	D4	A0	42	$\overline{\text{BUSRQ}}$	
15	A7	D15	43	$\overline{\text{INTAK}}$	
16	A15	D7	44	$\overline{\text{INTRQ}}$	
17	A6	D6	45	$\overline{\text{WAITRQ}}$	
18	A14	D14	46	$\overline{\text{NMIRQ}}$	$\overline{\text{WAIT}}$
19	A5	D13	47	$\overline{\text{SYSTRESET}}$	$\overline{\text{RESET}}$
20	A13	D5	48	$\overline{\text{PBRESET}}$	
21	A4	D12	49	$\overline{\text{CLOCK}}$	SCLK
22	A12	D4	50	$\overline{\text{CNTRL}}$	RCLK
23	A3	D3	51	PCO	
24	A11	D11	52	PCI	
25	A2	D2	53	AUX GND	GND
26	A10	D10	54	AUX GND	GND
27	A1	D9	55	AUX +V	+15
28	A9	D1	56	AUX -V	-15

Table 3.2: DACS Interface Card Types

TYPE	Card Type
000	Radiometer Input
001	Digital Input
010	Analog Input
011	Digital Output
100	I-Q Detector
101	unused
110	unused
111	unused

to place the requested filter output onto the data bus. Since the delay from requesting data to it being placed on the bus is variable, a feedback signal is required to indicate to the BCC that the data on the bus is valid. This is accomplished with the $\overline{\text{WAIT}}$ signal. $\overline{\text{WAIT}}$ is an open collector signal that causes the BCC to wait whenever it is active. Therefore, if an interface card requires extra time to supply data, it should drive $\overline{\text{WAIT}}$ low when the card is first selected and then release $\overline{\text{WAIT}}$ when data is available.

$\overline{\text{RESET}}$ is output by the BCC during power-on or a PS/2 initiated reset and may be used by interface cards to reset their state to a known value. The final two signals on the interface bus are SCLK and RCLK. RCLK is the 40 kHz sample clock which the 10 kHz analog IF signals are locked to. This source is extremely stable by virtue of the reference oscillator from which it is derived. RCLK is available on the bus and allows the I-Q detectors to receive their sample clock reference from a single source. SCLK is the system-wide 10 Hz sample clock and is presently derived from the 12 MHz clock crystal on the BCC. Through software control, SCLK may also be derived from RCLK. This is not presently done as the loss of RCLK would immediately cause sampling to halt. While the 12 MHz crystal on the BCC is not as accurate as the 40 kHz sample clock, the observed error is only slightly more than 1 second/day. Since Virginia Tech is not correlating measurements with other institutions, this slight error in sampling rate is insignificant.

Theory of Operation

The theory of operation for the backplane does not refer to a physical device, but to the sequence of operations required to move information between the BCC and the interface cards. As previous discussed, the backplane consists of an address bus and a data bus, and several control and status signals. The signaling sequence for a DACS consisting solely of a multiplexed analog input card is shown in Figure 3.4. In the actual system, control and sampling requires less than 10 ms of the allowable 100 ms

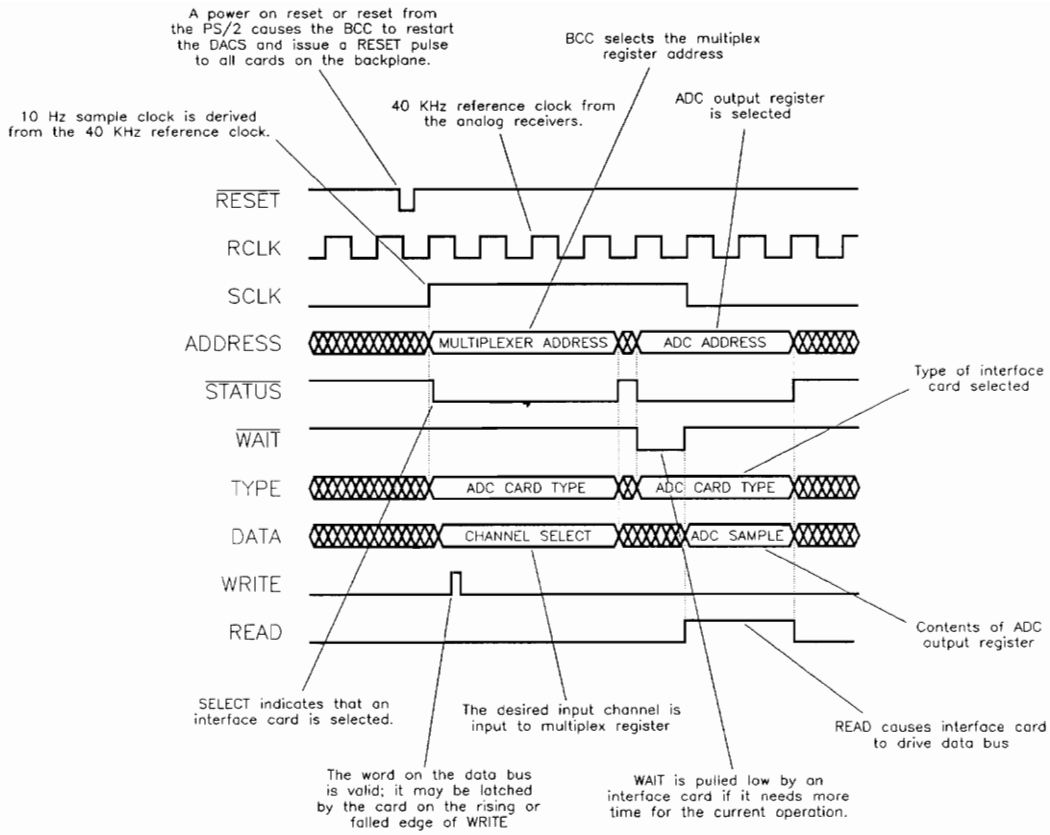

Figure 3.4. Sequence of operations required to transfer data between the BCC and an interface card.

sample clock period. Since this is a small percentage of the sample clock period, the timing sequence is not drawn to scale to provide legibility. While the timing relationship between signals is correct, the timing axis is nonuniform. A description of the events in this figure will now be given.

First, $\overline{\text{RESET}}$ is pulsed by the BCC in response to either a power-on reset or a hardware reset forced by the PS/2 control computer. SCLK is then started and produces a 10 Hz waveform. An opportunity to sample or control external signals begins with each rising edge of SCLK. Depending on the system configuration, a particular channel may be referenced at any multiple of the fundamental 10 Hz sample rate. For this simplistic system, the output of a multiplexed analog to digital converter is recorded at each sample clock transition. As shown in Figure 3.4, the address of the ADC multiplex register is driven onto ADDRESS by the BCC. Upon detecting an address which matches that associated with a register on the analog input card, $\overline{\text{STATUS}}$ is driven low and the card type is output on TYPE. The BCC then places the desired multiplex channel setting onto the DATA bus and pulses WRITE to latch the data into the multiplex register. The contents of ADDRESS are then changed to select the ADC output register and hence start the ADC conversion process. Since the ADC on this fictitious card is slow, $\overline{\text{WAIT}}$ is driven low to prevent the BCC from attempting to read incorrect information from the card. After the ADC conversion is complete, $\overline{\text{WAIT}}$ is released and the BCC sets READ=1 to cause the output of the ADC to be placed on DATA. The BCC then reads DATA and releases READ. This completes the sequence of backplane interface operations required for sampling a single channel. The next section describes the backplane control computer.

3.3.3 Backplane Control Computer

Data channel sampling, timed event control and transmission of collected data to the collection computer (CC) is performed by the backplane control computer (BCC). When collection begins on the DACS, the CC sends the time and date to the BCC.

After receiving this information, the BCC uses internally stored configuration information to sample and control channels at preselected intervals.

Design

The BCC can be divided into the three major components: the BCC to CC interface, the backplane to BCC interface and the 80286 microprocessor and associated support devices. Data transfer between the BCC and the CC is differential and utilizes several control and status lines. These have been thoroughly examined in Section 3.3.1. Likewise, the signaling required for backplane operation was just described in Section 3.3.3. The only remaining section of the BCC is the 80286 microprocessor and the generation of the DACS 10 Hz sample clock.

The 40 kHz sample clock from the analog portion of the digital receiver is extremely stable and precise and is a good candidate for a frequency reference. However, removal of either the I and Q detector cards or receiver maintenance would stop all data collection. Therefore, the 6.000 MHz system clock is divided in hardware to a obtain the 10 Hz DACS sample clock. The observed error using this method is slightly more than 1 second per day.

Two hardware interrupts are used in the BCC; the 10 Hz sample clock and data word sent from the CC. Since the 80286 directly supports only one hardware interrupt, an 8259 interrupt controller is used. Timely sampling of data channels is more important that a slight delay in reading a word from the CC, thus the sample clock is given higher priority.

16 KB of EPROM is provided to store the BCC software and 16 KB of RAM is used to store variables and collected data prior to transmission to the CC. Both EPROM and RAM are less than 25% utilized. The 80286 microprocessor is estimated to be idle approximately 95% of the time it is operational.

Circuit Description

Figure 3.5 is a high level block diagram of the BCC. Because of limitations in the size of a STDBUS card, the BCC occupies two cards. These cards are connected through a forty conductor ribbon cable. One card, with integrated circuits prefixed with an A contains the 80286 microprocessor, support circuitry, RAM and EPROM. The other card contains the backplane and CC interface logic and all integrated circuits on this card are prefixed with a B on the schematic.

Differential line receivers UB10-UB13 and line drivers UB3-UB6 are used to receive and transmit 16-bit data between the BCC and the CC. Control signals to the CC are transmitted by UB7 and status from the CC is received through UB14. As with the PS/2 interface card, the acknowledge signal from the CC is latched via UB24A to ensure that the BCC does not miss a response. Data latches UB22 and UB23 hold the data word that is input to the differential line drivers. Buffers UB1 and UB2 allow the BCC to read the word present on the line receivers. Address decoding on card B is performed with OR gates U20 and U26.

The interface to the backplane is a collection of data latches and buffers. The backplane address bus is driven by latch UB8. Backplane data is read through buffers UB15 and UB16 whereas data output to the backplane is held in latches UB25 and UB27. All status information required by the BCC, both backplane and CC interface related, is buffered by UB9. Similarly, control bits are output via UB17.

16-bit data, partially decoded addressing, interrupt request lines, $\overline{\text{RD}}$, $\overline{\text{WR}}$ and several other control and status lines pass on the forty pin connector between card A and B. Card A contain the 80286 microprocessor (UA1) and the necessary support chips; an 82284 clock generator (UA5) and an 82288 bus controller (UA6). Address latches UB7-UB9 and data buffers UA2-UA3 provide isolation and drive capability. A 74LS93 divide by sixteen counter (UA10) and an 8254 counter/timer (UA4) divide the 6.000 MHz output from UA5 to obtain the 10 Hz sample clock. Note that the 40 kHz I and Q detector sample clock is input to the 8254 and through software control, may

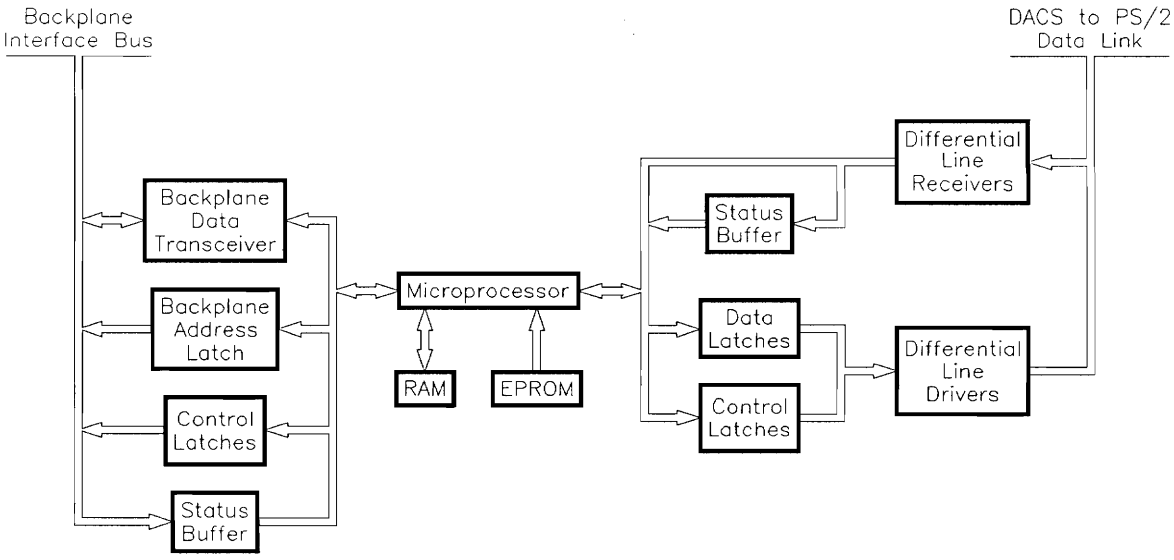

Figure 3.5. Backplane control computer block diagram.

be selected as the reference for the 10 Hz system clock. This is presently not in use for the reasons stated above. The 10 Hz clock is input together with INTDAS to the 8259 interrupt controller (UA15). Address decoding for the 8254, 8259 and logic on card B is implemented with UA11, a 3-to-8 line demultiplexer. EPROMs UB18 and UB19 store the BCC software and RAMs UB16 and UB17 contain sample data and internal variables.

3.3.4 I and Q Detector Card

Measurement of the received beacon power from a satellite must be performed in a narrow bandwidth to achieve a reasonable signal to noise ratio. Virginia Tech has chosen to digitally filter the beacon to a 3 Hz bandwidth prior to calculating the beacon power[9]. The input signal to the I and Q detector is a 10 kHz IF frequency locked to the 40 kHz sample clock. In-phase (I) and quadrature (Q) samples are taken at a pair (I-Q) rate of 1000 Hz. Note that since the IF signal is bandlimited to 200 Hz, the 1000 Hz pair rate does not violate the Nyquist criteria. The FIR filter executes 10 times a second and operates on the most recent 1116 data pairs.

Design

Two stages of design were used in constructing the I and Q detector. A prototype I and Q detector was wirewrapped and tested during the Summer of 1989. The test unit had a single input channel and output all results to a two digit LED display. Measurement of the test units' frequency response verified correct operation. Additionally, the prototype unit required only 20% of the available processing time to implement the filter. As a result, the production I and Q detector card filters two input channels in parallel. While four channels can probably be filtered with one unit, CPU loading could prevent future modifications to the software.

Dual 12-bit AD7870 analog-to-digital converters (ADC) are used to sample the IF input channels on the present unit. The AD7870 is a complete unit with integral

sample and hold and a voltage reference[19]. The criteria for selecting a 12-bit ADC is examined in Section 2.4.1. To date, the exact resolution of the unit is unknown. Figure 3.6 is a histogram of the output data from one of operational I and Q detectors. The data is binned to 0.01 dB and does not shown any obvious quantization effects to -30 dB; the estimated noise floor of the receiver chains.

Generation of the offset sample points is performed by two counters in an Intel 8254 counter/timer and several gates. The 40 kHz sample clock is directly input to both counters. External logic ensures that only one counter is enabled at a time. One counter is configured to count to 19 and generate an output pulse. The other counts to 21 and outputs a pulse. The output pulse from one counter changes the state of a flip-flop which disables that counter and enables the other one. Likewise, when the other counter outputs a pulse the first one is again enabled. By combining the output of both counters, ADC sample pulses are generated on the 19th and 40th transitions of the 40 kHz sample clock.

Because both ADCs sample input signals simultaneously, the end of conversion signals from the two ADCs are combined into a single interrupt signal. This signal, as well as card select which has been ANDed with READ, and the 10 Hz DACS sample clock are input to an 8259 interrupt controller. ADC end of conversion is given the highest priority, sample clock second and card read the lowest. Prioritization of interrupts is used to ensure that time critical operations are performed while the data is still valid. For example, the ADC conversion rate is 2000 samples per second. Failure to read the ADC output within 500 uS of the end of conversion interrupt will cause a loss of data.

The I and Q detector software is stored in 16 KB of EPROM and the sampled data in 16 KB of RAM. Less than 20% of the ROM is used to store the present software while 80% the RAM is utilized to hold sampled data. Operational status is indicated through an LED on the front of the card. The LED is active only during FIR filter operations.

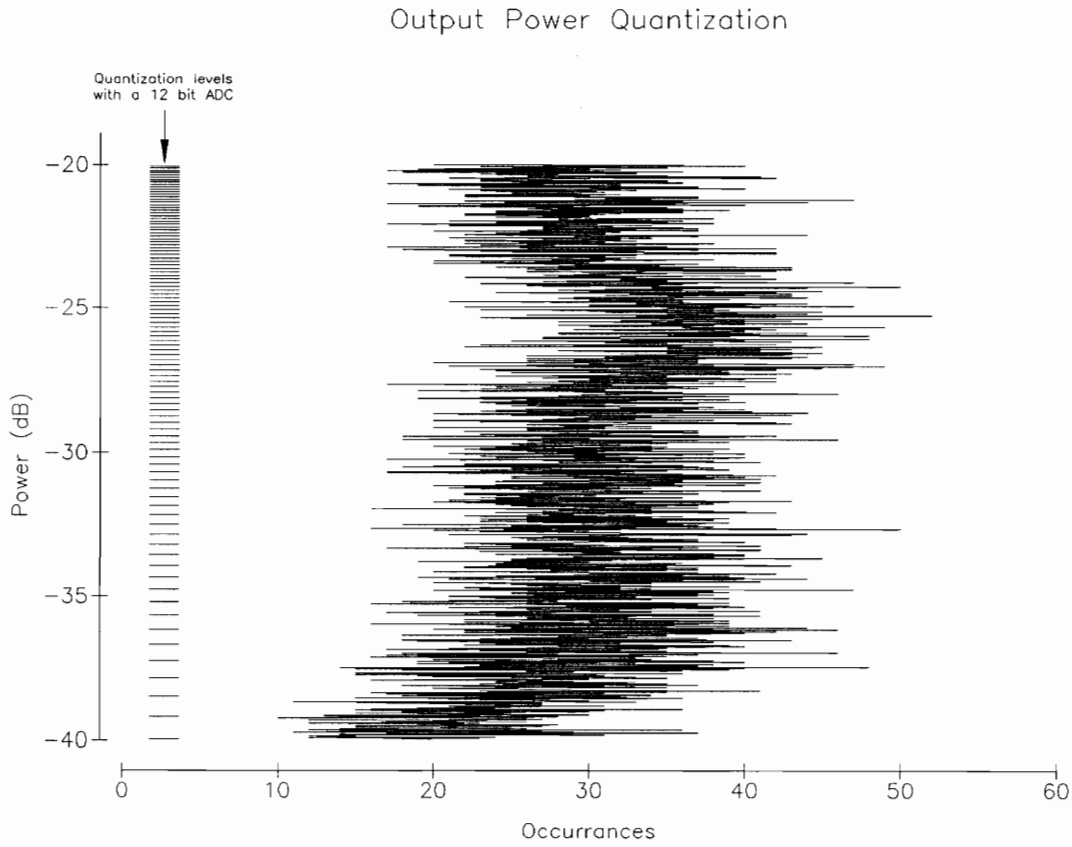

Figure 3.6. Histogram of the output power from an I and Q detector. Data shown is unpreprocessed 30 GHz channel information binned to 0.01 dB from a thunderstorm on October 18, 1990.

Circuit Description

Figure 3.7 is a simplified block diagram of the I and Q detector. Because of spacing constraints, the I and Q detector is divided into two circuit boards. These boards are physically mounted on top of one another with a thirty-two pin connector between the two. Integrated circuits on the schematic prefixed with B are on the bottom card which plugs into the backplane. Those integrated circuits marked with an A are on the daughter card.

Four consecutive backplane addresses are used by the card (c.f. Section 4.4.2). Address decoding is performed by UB1 and UB5. When the card is selected, UB4A sends an interrupt to UB11, the 8254 interrupt controller. At the same time, flip-flop UB17A through UB8 drives $\overline{\text{WAIT}}$ low. UB8 also places the card type and status onto the backplane. The I and Q detectors are only cards in the DACS that cannot provide information within 100 ns of a read pulse. Time is required to service the interrupt, get the requested data and place it in latches UB6 and UB7. The operation of latching data into UB6 and UB7 resets $\overline{\text{WAIT}}$ and allows the BCC to read the data.

The 80286 microprocessor (UA1) requires a clock generator (UA5), bus controller (UA4) and address latches (UA6, UA2, UA14A) for operation. Data bus buffers UA12 and UA11 provide isolation and additional drive capability. EPROM is used for non-volatile program storage and RAM for data storage. Since the 80286 is a 16-bit machine, memory must be divided into a high and a low byte. UA7 and UA8 are 8 KB by 8-bit RAM memories and UA10 and UA11 are 8 KB by 8-bit EPROM memories. The ROM is mapped into memory space by UA14A and UA3B so that it appears both in low memory (for the interrupt vector table) and high memory (for the reset vectors). Address decoding for input and output devices is accomplished with UB4D and UB15.

The 40 kHz sample clock from the analog receiver is transmitted using differential data. UB14 receives this signal and converts it to TTL levels for the 8254 counter/timer (UB2). As described above, gating (UB3 and UB9A) is used to imple-

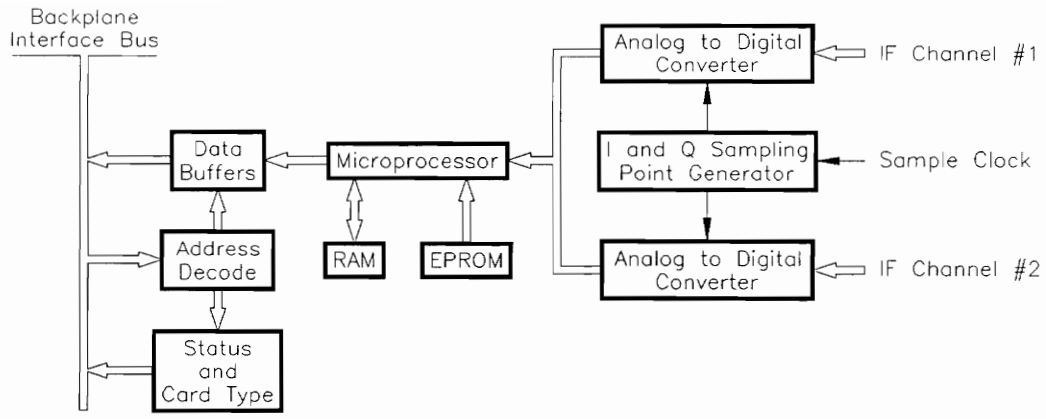

Figure 3.7. I and Q detector block diagram.

mented the offset sampling required for I and Q detection. Because TTL logic is fast, when one of the 8254 counters outputs a pulse, it is disabled within less than 20 ns. The resulting pulse from UB9A is too short for the ADC start of conversion input. UB3B takes the sample pulse output from UB9A and stretches it by one period of the sample clock to a length of 25 uS. This output then simultaneously starts both ADC (UB16 and UB10) conversions. When both ADCs end their conversions, an interrupt is generated via UB9B. The microprocessor then reads the data from both ADCs and stores it for processing.

3.3.5 Radiometer Input Card

Radiometers are used to measure sky noise temperature, from which attenuation along the signal path can be calculated. Virginia Tech uses four radiometers: one each at 12, 20 and 30 GHz and a 20 GHz diversity unit. The output of each radiometer is a TTL pulse train that varies in frequency from zero to 10 kHz. By counting the number of pulses within a given period of time, the radiometer output level can be easily sampled and recorded.

Design

Electrical isolation and variable integration times are the two requirements for the radiometer input card. Isolation is not necessarily required as the radiometer output and DACS are both indoors and separated by less than forty feet. However, the use of optoisolators nullifies the effect of common mode voltage on the signal lines. Variable integration times can be provided in one of two ways. First, the BCC can read the number of pulses accumulated every 0.1 second and output a sum after every N samples. The second technique is to let the radiometer input card count pulses for $0.1N$ seconds after which the BCC reads the result. A modified version of the former is used in the present system.

Until March 1991, the radiometer input card operated in a count, read and reset

fashion. This method was highly susceptible to error, as accidentally reading one of the radiometer counts would reset that count to zero. These spurious reads are not the result of software error, but electrical noise within the DACS. Rather than attempt to reduce the amount of noise, the circuitry on the card and the BCC software were slightly modified. The card was changed so that the counters are never reset. Instead, the BCC reads the value for a radiometer channel and subtracts the previous value to obtain the number of counts in the last time period. While variable integration times are easily implemented, all channels are presently sampled at a 1 Hz rate.

Circuit Description

Figure 3.8 is a block diagram of the radiometer input card. The radiometer input card occupies four consecutive backplane addresses. Address decoding is performed by U15 and U19. When the card is selected data buffers U16 and U17 provide a data path from the on-card data bus to the backplane data bus. U18 is also enabled during card select and outputs the card type and status to the backplane. U9/U13, U8/U12, U7/U11 and U6/U10 are 8-bit counters are cascaded to form four nonresetable 16-bit counters. When the backplane READ line is activated, data is read from the selected counter pair. Each counter pair is driven by the output of an optoisolator: U4, U3, U2 or U1. Electrical noise is reduced by the use of bypass capacitors spaced evenly about the card. Excessive power supply voltage or external transients are clamped by zener diodes placed between the logic supply rail and ground.

3.3.6 Digital Input Card

Alarms, waveguide switch position and rain gauge tips are signals monitored via the digital input card. This card is sampled at a 10 Hz rate and its output is directly integrated into the DACS data stream.

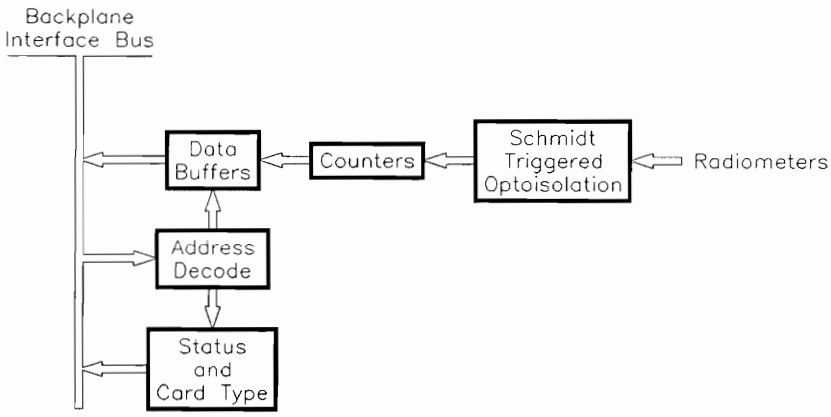

Figure 3.8. Radiometer input card block diagram.

Design

This card provides thirty-two channels of optically isolated digital inputs. Several different external voltages (5, 12, 24) are input to the optoisolators. Series resistors are necessary to limit the input current to less than 10 mA. The output from each optoisolator is then Schmidt triggered to reduce the effects of noise. Four of the channels are designated for use with rain gauges and latch input transitions until the card is read by the BCC. This is necessary because the digital input card is sampled at a 10 Hz rate. Without latches, a rain gauge trip occurring between two samples would be overlooked.

Circuit Description

A block diagram of the digital input card is shown in Figure 3.9. This card requires two consecutive backplane addresses. Address decoding is performed by U27 and U22. When the card is selected by the BCC, U28 outputs the card type and status to the backplane. Data is driven on the backplane data bus by U29-U32. These components are 74LS257 quad 2-to-1 multiplexers and are used to select one of the two 16-bit banks of input channels. When an input signal enters the board from an external source it first passes through a current limiting resistor and then one of the optoisolators (U5, U6, U8-U13). The value of the current limiting resistor is dependent on the external voltage applied to the input. After passing through an optoisolator, an input signal is Schmidt triggered (U19-U21, U23-U25) to provide a measure of hysteresis and noise reduction. All but four of the signals are then wired to the 74LS257 bus drivers. Each of the remaining four bits is connected to the preset input of a 74LS74 flip-flop (U15-U16). These lines are used for the rain gauges and therefore it is not possible to miss a rain gauge trip. The flip-flops are automatically reset following a read operation. After examining collected data, the rain gauge trips were found to be approximately 0.3 seconds long. As a result, the 74LS74 flip-flops are superfluous.

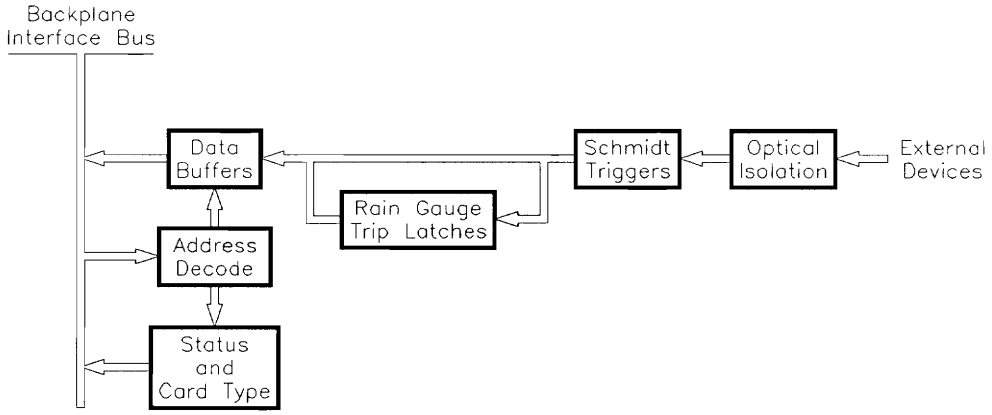

Figure 3.9. Digital input card block diagram.

3.3.7 Digital Output Card

Timed event control of external devices is performed using the digital output card. Devices presently controlled by the DACS include noise diodes, waveguide switches and a DACS alive bit. Each of these is binary.

Design

To allow future expansion, thirty-two output channels are provided by the DACS. Each channel's output is optically isolated to provide electrical isolation and allow translation between DACS TTL levels and external voltages. Each channel must also be glitch-free. That is, when the output changes values there may be at most one transition on each bit.

Circuit Description

A block diagram of the digital output card is shown in Figure 3.10. The digital output card occupies two consecutive backplane addresses. Address selection is performed by U13 and U19. Data buffers U21 and U22 are continually enabled and isolate the oncard data bus from the backplane. When the card is enabled U20 outputs the card type and status onto the backplane. Pulsing the backplane signal WRITE causes the data word on the backplane to be latched into either latch pair U17/U15 or U16/U14. These latches are non-transparent 74LS374s, therefore glitches appearing on the data bus will not appear on the outputs. The latch outputs are connected to a bank of optoisolators (U2-U4 and U8-U11). Within reason, any external voltage may be connected to the non-grounded side of an optoisolator output. The only requirement is that less than 10 mA of current should flow through the transistor when the optoisolator grounds the output.

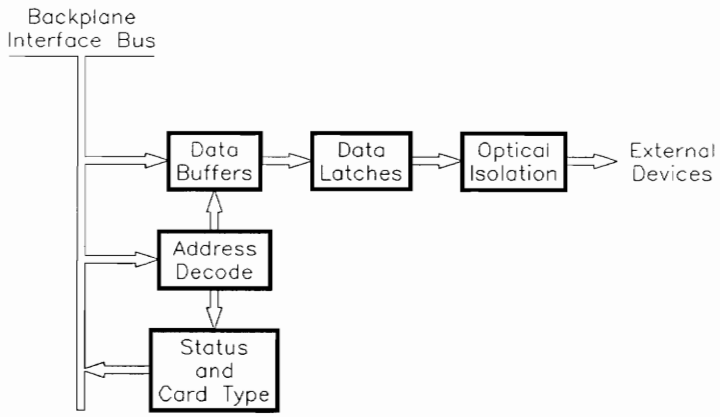

Figure 3.10. Digital output card block diagram.

3.3.8 Analog Input Card

Wind speed, temperature and humidity are measured using analog sensors. The input voltage range and resolution of each input was examined in Chapter 2. In that section the number of analog inputs was determined to be somewhat less than 32.

Design

Figure 3.11 is a block diagram of the analog input card. Thirty-two analog input channels are provided on the analog input card. Analog signals are sampled at a rate of one sample every 0.1 second. The resolution for each channel is 12 bits. The component used for the analog input card is an AD7870 because it contains an on-chip microprocessor interrupt which greatly simplifies interfacing.

The AD7870 is a single input analog-to-digital converter. Multiple input channels are added by using five 8-input multiplexers. Four of the multiplexers decimate the thirty-two input channels to four channels. The fifth multiplexer then selects the specific channel for measurement by the ADC. An opamp buffer stage follows the last multiplexer to allow accurate measurement of the input voltage. Without the buffer stage, several hundredths of a volt are dropped across the multiplexers. The exact method of interconnecting the multiplexers and opamps is shown in the schematic on page 97.

Each of the input channels is bypassed to ground with a 0.1 uF capacitor to reduce the effects of noise. Additionally, all inputs are clamped to ground through a 6.8 V zener diode. Channels which are connected to temperature sensors are biased toward +10.000 VDC with a current of 1 mA. This bias voltage is necessary for the LM135 temperature sensor to function correctly.

Circuit Description

U9 maps the analog input card into one address on the backplane. Writing to that address latches the contents of the data bus into the select registers for the analog

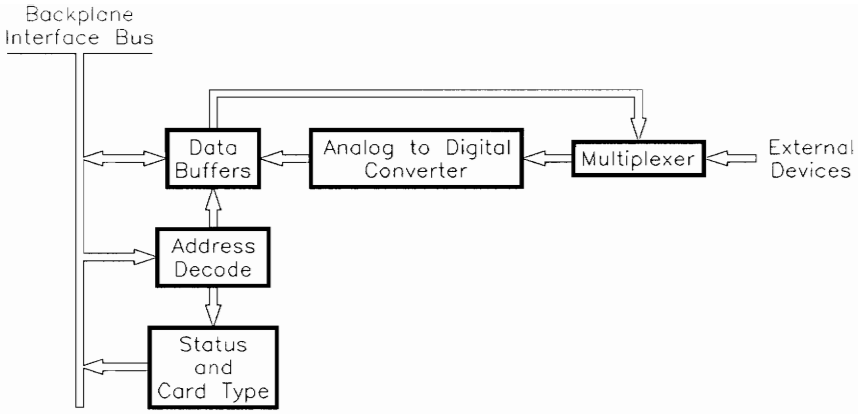

Figure 3.11. Analog input card block diagram.

multiplexers (U1-U4, U7). During DACS operation, the multiplex setting for the next sample period is written to the card. Immediately thereafter, the present output of the ADC is read and inserted into a timestamped data record. Recall that the BCC samples interface cards on the rising edge of SCLK. To minimize the effect of digital noise, and to allow the selected input channel to stabilize after the multiplexers are switched, the ADC is sampled on the falling edge of SCLK. The output from the multiplexers is buffered through U7 and the gain and offset of that signal are modified to match the -3 V to +3 V input range of the ADC (U12) by U6. ADC output data and the card type and status are driven onto the data bus via U10 and U11.

3.3.9 DACS Rack Enclosure

The components examined above are interface cards that plug into the backplane. The DACS also requires a power supply for the system and a chassis to contain everything. A 12" high by 15" deep rack mount enclosure is used as a chassis. This chassis provides sufficient space for the backplane, power supply and fan cooling. A linear power supply was chosen over a switching type unit because fewer high frequency noise components are present in the output.

Chapter 4

Support Software

The hardware necessary for DACS operation was detailed in Chapter 2. Of the cards located in the backplane, the I and Q detector and the backplane control card are microprocessor based and require software for operation. Similarly, a program for the collection computer is needed to store collected data onto disk. These three programs are the topic of this chapter. The next section examines the choice of a programming language for the software. Following that, each of the three computer programs is considered in turn. Software block diagrams are given and key points in the operation of each piece of code are examined.

4.1 Environment

All of the computer program useds in the DACS are data driven processes. By data driven, it is meant that if there is no data to process then the program waits in an idle loop. Two methods are available for controlling data driven processes: polled and interrupt driven I/O. Polled I/O requires the CPU to constantly check the status of an input port to determine whether information is present and should be processed. There are problems which this method. In the case of the I and Q detector card, the FIR filter requires much more time to execute than the time between A/D samples. This implies that a polled approach will not work without requiring polling within the filtering process and thus increasing system loading. A better solution is the

use of interrupts. Interrupt driven systems respond to external requests without the need for modifications to the user's software. Moreover, provided that interrupts are enabled an interrupt may occur at any point in program execution. Thus while the polled approach can only process external data at discrete points in program execution, interrupt driven I/O is asynchronous to program execution. Because of the simplicity and performance advantages of interrupt driven I/O it was used in all software for the DACS.

The choice to use interrupt driven I/O restricts the selection of programming languages to those that support interrupt service routines. 80286 assembly, of course, fulfills this requirement as does Microsoft C. Microsoft C has another advantage in that it may be linked with assembly code. Linking of C and assembly is required for the standalone I and Q detector and backplane control cards. C alone cannot be used because the routines required during system reset and the interrupt vector jump table must be placed at specific locations within memory.

4.2 I and Q Detector

The I and Q detector card accepts two 10 kHz IF signals and a 40 kHz sample clock. Output from the I and Q detector are the filtered in-phase and quadrature components of the measured signal strength within a 3 Hz bandwidth. An extensive discussion of the sampling technique and filtering algorithm is presented in [9] and will not be repeated here. The section of Chapter 3 devoted to the I and Q detector described the hardware associated with the card.

4.2.1 FIR Filtering

FIR filtering is essentially a vector dot product operation[8]. One vector is the sampled data and the other vector the filter coefficients. Through the use the appropriate filter coefficients, a sampled signal may be digitally filtered. One of the benefits of linear phase FIR filters is that the filter coefficients are symmetric about the cen-

ter point. This simplifies the filtering algorithm and allows processing of a greater number of data points.

The output from the analog portion of the receiver is a 10 kHz IF frequency locked to a 40 kHz sample clock. The signal output from the analog receiver is bandlimited to 200 Hz by an antialiasing filter. Therefore, it is possible to sample this signal at 400 Hz and satisfy the Nyquist criteria. A pair (I-Q) sampling rate of 1000 Hz has been specified as the rate for IF sampling. Since the IF signal is known to be frequency locked to 10 kHz, the in-phase and quadrature components can easily be obtained. Given the basic sampling rate is 1000 pairs per second, 40 transitions of the sample clock occur in each sample period. With the 10 kHz IF frequency locked to the 40 kHz clock, I and Q detection is performed in the present system by sampling on rising edge of the 19th and 40th sample clocks within a sample period. The I and Q samples are then filtered through the use of a finite impulse response (FIR) filter.

The resolution for the ADC chosen to sample the bipolar IF signal is 12 bits. Because of the bipolar nature of the IF signal, only 11 bits of resolutions are actually provided; the amplitude of the signal is being measured and thus the negative portion of the input provides redundant information. If phase information is not necessary, the 12th bit of resolution can be regained be offsetting the IF signal such that only the positive half of the sinewave falls within the input span of the ADC. Virginia Tech has chosen to retain phase information and thus only 11 bits of resolution are available. With eleven bits of resolution, ESA's standard of measuring -40 to +8 dB to within 0.05 dB cannot be fulfilled since 16 bits are needed (c.f. Section 2.4.1). However, the method by which the signal is filtered combined with the presence of electrical noise yields an effective increase in resolution.

The precise measurement of beacon power is possible only if a minimal quantity of noise is included in the post-detection bandwidth. The bandwidth chosen for measurements is 3 Hz. By separating the I-Q sample pairs into an I sample stream and a Q sample stream an in-phase and quadrature time history is obtained. A finite

impulse response (FIR) digital filter is applied to these two signals to lowpass filter them to 3 Hz. By filtering to 3 Hz the 10 Hz sample rate easily satisfies the Nyquist criteria. The output of an N-point FIR filter is[8]

$$y(n) = \sum_{i=0}^{N-1} c_i x(n-i). \tag{4.1}$$

Where the c_i are constant filter coefficients and the $x(i)$ are past sample values. The output of the filter can thus be viewed as a weighted average of the most recent N samples. This averaging of sample values effectively increases the resolution of the ADC through a process known as dithering[14]. The maximum increase in resolution obtained by averaging N samples is $\log_2 N$ bits. The 1116 point filter chosen for the I and Q detector can increase the resolution by at most 10.12 bits. Since only 5 additional bits of resolution are necessary, this system fulfills ESAs measurement requirement of 0.05 dB from +8 to -40 dB. If noise of a known amplitude and frequency were added to the input signal it would be possible to determine the exact resolution increase. However, to simplify system design, only the noise already present on the 10 kHz IF and that associated with the ADC converter board will be present. Therefore, it is not possible to calculate the exact increase in resolution.

4.2.2 Software Implementation

Figure 4.1 is a high level software block diagram of the I and Q detector software. Note that two I and Q channels are actually implemented on one I and Q detector card. As shown in the diagram, the software is comprised of an initialization routine and three interrupt service routines. Upon receiving a reset signal from the BCC, the I and Q detector resets all internal variables and pointers. During this process, the onboard 8254 timer/counter is configured to generate the necessary sampling scheme to extract I and Q from the 10 kHz IF.

The ADC then begins to generate interrupts at the end of conversion. Both of the ADCs start on the same sample clock and the interrupt is generated when both

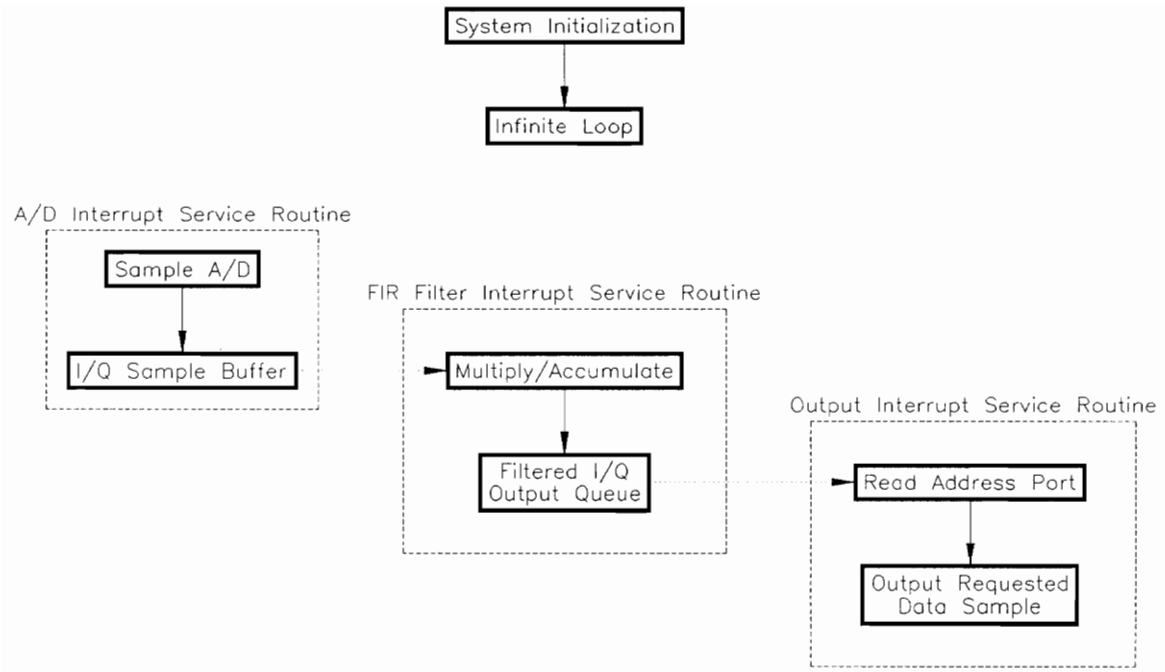

Figure 4.1. I and Q detector software block diagram.

ADCs have results. The sample interrupt service routine is then called via a hardware interrupt. Within the I and Q detector software, interrupts are never disabled for more than one or two lines of C source code. In doing this, interrupts will not be missed and data lost. Both of the ADC input values are then read and stored in either the I buffer or Q buffer for the appropriate channel. Data sampling continues in this manner and is not interrupted for any reason.

Buffering a continuous stream of data is most easily implemented with a circular buffer. A circular buffer has a pointer to the first element in the buffer and a pointer to the last element. The assumption is made that reaching the physical end of the array implies that the next element is at position zero. For example, given a 5 element array $X[0..4]$ the first element could be $X[3]$ while the last element is $X[1]$. In this case, the data consists of elements $X[3]$, $X[4]$, $X[0]$ and $X[1]$. The advantage of a circular buffer is that it is not necessary to physically move the data when a new sample is added. Circular buffers are used for the I and Q data streams and the filter output queue.

FIR filtering occurs asynchronous to the I and Q collection process. The I and Q buffer are sized such that a filtering operation will be complete before old I and Q data is overwritten. With the 10 Hz output rate, and the 1116 point FIR filter, I and Q buffer lengths of $1116 + 0.1 * 1116 = 1228$ are sufficient. Filtering begins upon receipt of an SCLK sample pulse from the BCC. At that time, the most recent 1116 points of I and Q data from both channels are filtered and the result placed in a 16 element output queue. The filtering algorithm utilizes the symmetry of the FIR coefficients to decrease the number of multiplications by half. Additionally, the FIR coefficients are stored as integers instead of floating point numbers and the answer is scaled by an appropriate amount. This enables all of the calculation to be performed in integer math and removes the need to place an 80287 math processor on-board. No loss in accuracy results from the use of integer math.

The I and Q detector card is mapped into four consecutive read only backplane

addresses through which filtered I and Q data may be accessed. Reading from the first address retrieves I for the first channel, the second address Q for the first channel and the next two addresses I and Q for the second channel. Filtered data is stored in such a manner as to prevent accidentally reading an I and a Q sample from different filtering passes. After reading Q for the second channel, the output buffer is shifted to provide access to the next set of filtered data.

This completes the operational description of the I and Q detector software. Output data from the I and Q detector is read by the backplane control computer, timestamped and assembled into data records along with environmental and status information and sent to the PS/2 for data archiving. The software which performs this task will now be examined.

4.3 Backplane Control Software

The backplane control computer (BCC) is primarily responsible for collecting data from input cards and sending it to the PS/2 for archiving. Additionally, timed event support allows periodic calibration of external equipment, namely the radiometers. Figure 4.2 illustrates the major program functions of the BCC software.

When data collection is started, the PS/2 pulses the BCC RESET line. At this point, the BCC executes an initialization routine. Within this routine, program status is reset, the 10 Hz backplane interrupt is started and channel sampling information is loaded. The initial system design envisioned downloading the sampling configuration from the PS/2. For various reasons, including conditional timed events such as avoiding waveguide calibrations during rain, the configuration data cannot be downloaded. At present, the BCC samples four beacon channels, four radiometers, thirty-two analog channels and two sixteen bit digital status words. Because of the massive quantity of data and the difference in sampling rates between beacons, radiometers, and analog input channels, each data record contains a column of time multiplexed data. Radiometers are sampled at a 1 Hz rate and thus only 40% of the column space is

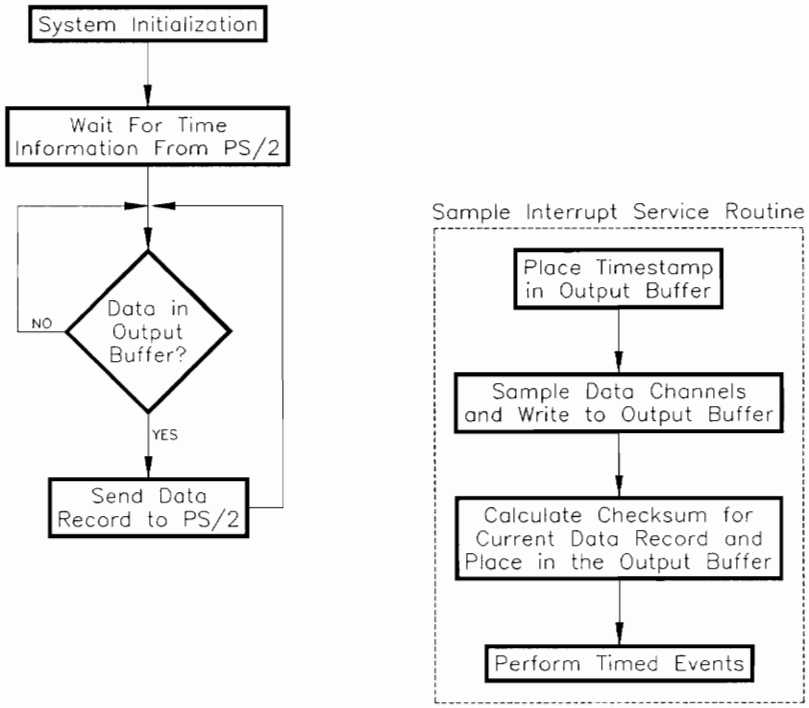

Figure 4.2. Backplane control computer software block diagram.

utilized. Rather than use a separate column for analog data, the samples are placed in the unused radiometer column space.

To provide a measure of security, each data record includes a timestamp with 0.1 second resolution. By timestamping each record, time gaps within stored data are easily located and data stored out of time sequence can be salvaged. Indeed, during the first several months of DACS operation, the collection software on the PS/2 had a programming error that infrequently caused the loss of several data records and storage of data out of time sequence. The standard C timestamp has a resolution of 1 second with time zero assigned to midnight January 1, 1970. Because we require 0.1 second resolution another method is required. The DACS time format counts tenths of a second since 00:00:00.0 GMT January 1, 1990. Note that since DACS time is represented with 32 bits of resolution, this format cannot be used after 00:38:49.5 12-AUG-2003 GMT.

After executing the BCC initialization routine, the BCC waits until the PS/2 sends the current time. Time is required both for timestamping records and to ensure that timed events always occur at the same time of the day. Transferring time and sampled data information between the DACS and the PS/2 is generally error free. However, errors will occasionally occur on any data channel. To reduce the possibility of undetected errors, all data transfers are packetized. Each packet contains a header indicating the size of the packet in words and a trailing 16-bit CRC checksum. By using a 16-bit checksum all single bit errors are detected along with many multiple bit errors. System hardware does not presently allow retransmission for incorrectly received data. This is not a problem as errors are extremely infrequent.

After the BCC receives the present time from the PS/2, the sample interrupt service routine is enabled and is invoked at a 10 Hz rate by the sample clock (backplane signal SCLK). The main program then waits in an infinite loop until data is detected in the output buffer. When data is present in the output buffer, all data in the buffer is sent to the PS/2 for archiving to disk. During the transmission of data to the PS/2,

it is necessary to temporarily disable interrupts on the BCC. To minimize jitter in the 10 Hz sample rate of the inputs channels, interrupts are never disabled for more than one line of C source code. By leaving interrupts enabled, the sample interrupt service routine can temporarily halt transmission of data to the PS/2 and sample the necessary data channels and perform timed events without significant delay. When the output buffer is clear, the main program once again waits until data is present.

The sample interrupt subroutine is responsible for performing all time critical tasks. Of primary importance is the sampling of data channels. Upon entry to this routine, time is incremented and enqueued as a timestamp into an intermediate buffer. Then, the required data for each column of the output record is sampled and queued into the buffer. If a specific column is unused, a value of zero is inserted. After all columns have been processed, the intermediate buffer is converted into a data packet by adding the proper header and trailing checksum and then placed into the output buffer. Within the BCC, the most recent value of a data channel is not saved except for the radiometers. Radiometric levels are necessary to determine whether waveguide calibrations should be performed.

After sampling all of the data channels, timed events are performed. Presently, there are three events: noise diode calibration, waveguide switch calibration and a DACS alive output bit. The alive output bit is a 5 Hz square wave output through a bit on the digital output card. The square wave is generated in software and will cease to exist if the BCC software malfunctions. This signal, among others, indirectly triggers a telephone dialer alerting the operator on-call to investigate a problem at the tracking station. Failure of the BCC is also detected by the PS/2 and will cause a hardware reset of the PS/2 and thus automatically cold start the entire DACS.

The other two timed events are required to obtain calibration information for the radiometers. Because excess noise injected into the system does not affect the beacon level, noise diode calibrations occur every thirty minutes regardless of weather conditions. Waveguide switch calibrations, however cause the loss of twenty seconds

of data and are not performed during periods of rain. The line of sight path to OLYMPUS is 13.9° above the horizon. This low elevation angle causes the signal to pass through a large volume of atmosphere prior to reception at Virginia Tech. Because rain along any portion of the path will attenuate the beacon, the output from the rain gauges does not necessarily indicate the presence of rain on the path. Moreover, analyzing the beacon signal strength is not feasible because scintillations can cause short term signal changes of ±5 dB. Therefore, the criteria for performing waveguide calibrations is the output from the 20 GHz radiometer just prior to the scheduled calibration time. If the radiometer does not show excessive attenuation along the path, the calibration occurs. Presently, waveguide calibrations occur every six hours.

4.4 PS/2 Data Collection Software

Data sent from the BCC to the PS/2 follows a rather lengthy path before being stored on disk. A software block diagram of the PS/2 data collection software is shown in Figure 4.3. The collection code is different from most computer applications in that it executes in the background. Background execution allows the user to perform DOS commands or execute other programs while data collection continues. Successfully writing a background, or Terminate and Stay Resident (TSR) program, is difficult because DOS does not provide the necessary features. Fortunately, software packages are available that allow a standard C program to execute as a TSR.

When started by the system operator, the PS/2 collection code (named DAS), determines if data collection is currently active. If this is the case, the operator can either request the status of the collection process or halt data collection. Program status provides information such as data buffer usage, number of data packets received and the time and date when the collection process was started. If collection was not active, DAS terminates the foreground portion of the program and continues executing as a TSR program. After DAS becomes a TSR, it is configured to receive

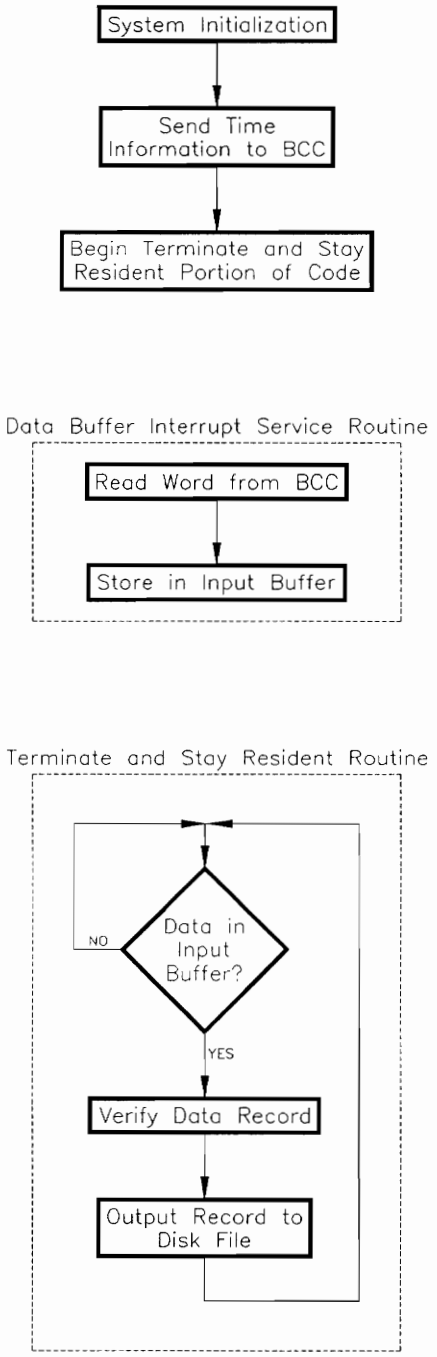

Figure 4.3. PS/2 Collection computer software block diagram.

data from the BCC. DAS then resets the BCC and sends the current time and date to the BCC. Upon receiving the time information, the BCC begins sampling data channels, performing timed events and sending packetized data to the PS/2.

One of the problems with DOS is that it is not reentrant. Hence, if DOS is active when the BCC interrupts the PS/2 to send a data word, DAS cannot receive the word and immediately write it to disk. The interrupt service routine (ISR) therefore places all data words in a shared buffer. The buffer is shared between the ISR and the packet parser. Only the ISR may place data in the buffer and only the parser may remove data. The size of the buffer required is highly dependent on system loading. A TSR program allows the user to perform a task in the background, however system loading may cause that task to suspend for perhaps several minutes. Operations such as graphically displaying an hour of data or performing system backup result in continual use of DOS services for up to four minutes. During this time the ISR continues execution but the TSR does not. Choosing a sufficiently large data buffer for use between the ISR and the parser is necessary for correct operation.

Tape backup is the most time consuming task and requires at least five minutes and perhaps as many as thirty. The packetized data rate from the BCC to the PS/2 is 300 bytes per second. Over a period of half an hour, 540 KB of data will amass. The tape backup program requires approximately 300 KB of memory, DOS uses 100 KB and DAS 16 KB. With only 640 KB of conventional memory, only 224 KB remains for buffering data. A solution is to use the 2 MB of eXtended Memory (XM) that the collection computer has for the buffer. XM is controlled by an extended memory manager (XMM) and is most easily accessed through C library functions provided by Microsoft. Accessing XM is slower than conventional memory because the 80286 microprocessor must first be placed in protected mode. Next the data transfer is performed and the 80286 is returned to real mode. System performance improves when data transfers to and from XM are performed with large blocks of memory; DAS uses 3000 byte blocks.

When DOS is idle, the TSR is permitted to execute. The primary task of the TSR is parsing data packets and logging the data record portion to disk. During parsing, the length of the packet is checked as is the checksum. If either of these items is incorrect, a message is written to the system log file and the errant packet is discarded. Data records from correct packets are written directly to disk without any processing. Because 22 MB of data is collected each day, raw data is placed in files that are one hour long. The resulting files are 936,000 bytes long and, if necessary, can be stored on a high density diskette.

After accounting for system files, approximately 40 MB of free disk space is available on the collection computer. Reserving several MB for temporary usage, yields storage for 36 hours of raw data. To allow the user to view data from previous hours, the most recent 36 hours are always on disk. When a file becomes older than 36 hours it is automatically deleted. Immediately before a file is deleted its archive bit is checked to determine whether it has been archived to tape. If the file was not archived, a message is placed in the system log. It is the operator's responsibility to ensure that files are backed up to tape at least every 36 hours.

As stated above, an operational log is maintained to provide a history of DACS system operation. The log, which is generated by DAS, is an ASCII file containing a timestamp and a textual message. Collection start and stop times are logged as well as the time of arrival and contents of any errant packets. The PS/2 system resets which occur as the result of an interruption in the flow of data from the BCC to the PS/2 are also recorded.

Chapter 5

Conclusions and Recommendations

This thesis has examined the specification, design and construction of a data acquisition and control system for the OLYMPUS propagation experiments. Chapter one detailed the need for additional measurement research at K_a band. Previous research efforts at K_a band were performed using relatively slow sampling rates with emphasis on short term deep fading. With the shift toward low power VSAT terminals, signal attenuation on the order of 3 dB is a more significant concern. Accurate measurement of both received beacon signal strength and radiometer predicted attenuation are necessary to statistically characterize these low level fading events.

In addition to beacon strength and radiometer level, environmental data and system status must also be collected and periodic calibrations performed. These additional measurements are used to verify the validity of the measured beacon and radiometer levels while calibrations serve to calibrate the radiometers. Chapter 2 examined all of the data channels in terms of resolution, collection rate and isolation characteristics. These system specifications were then used in a cost/performance comparison between commercially available data acquisition and control systems and a custom unit. Selection criteria including cost, flexibility and the inherently custom hybrid receiver chosen for measuring beacon strength indicated that a custom DACS was optimal. The design and construction of the circuit boards for the custom DACS was detailed in Chapter 3.

For each of the electrical subsystems, a block diagram was first presented along with specific requirement for the circuit. The reader was then instructed to view the associated schematic. An overview of the physical circuit operation was then given to verify that all requirements had been observed. For those cases where the final circuit deviates from the design requirements a rationale for noncompliance is provided. Following the hardware description, software required for system operation was outlined in Chapter 4.

The operation of the three computer programs required for the DACS was presented in chapter four. Because these programs are somewhat complex and subject to change, detailed flowcharts and program listings were not provided. Instead, high level block diagrams were given along with a description of program operation. Since the DACS is a data driven process, the operational descriptions were presented by examining the flow and processing of data.

Chapters 3 and 4 cover the hardware and software at a level suitable for thesis work but lack sufficient detail for system upgrades, maintenance and future design work. The information exists and may be obtained from

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5.1 DACS System Status

The DACS has been operational and collecting data since August 3, 1990. During the first month of data collection, only beacon signal strength, radiometer levels and rain gauge tips were collected. The digital input and output cards were added to the DACS in the middle of September, while the analog input card was not complete until the end of October. From August 3rd until January 6, 1991 DACS operations had to be suspending daily in order to archive collected data to tape. Nine track tape

was used as the storage medium until the first week of October at which time the change was made to high density data cassette. Average downtime for backup with the 9-track tape unit was twenty minutes while roughly five minutes were required for the cassette unit.

On January 6th the data collection software executing on the PS/2 was replaced with a new version (DAS) which allowed data backups during DACS operations. Since that time, no DACS failures have occurred and data collection has been continuous except for operator initiated shutdowns for system maintenance. To date, the longest period of uninterrupted collection is almost three weeks.

5.2 Recommendations for Future DACS

While the DACS performs the task for which is was designed, there are changes which should be incorporated into any new DACS. These modifications could be made to the OLYMPUS DACS, but the cost in terms of labor and lost data could not justify the incremental benefit. However, for a new design the increase in system reliability and in some cases, decreased cost are very attractive. Following are the recommendations for future design and the reasons for each.

Optical Isolation

Isolation by means of optical fiber or optoisolator is the simplest method of electrically isolating two components. For the OLYMPUS DACS, all digital inputs and outputs are optoisolated except for the differential 40 KHz sample clock and the differential data link between the PS/2 and the BCC. While differential line receivers will sustain a small common mode voltage, large transients can easily cause damage.

PALs and EPLDs

All DACS circuits make use of discrete logic to perform various operations. While TTL gates are a proven method of implementing logic, simplified circuit design and

wiring is possible through the use of programmable array logic (PAL) and erasable programmable logic devices (EPLDs).

Printed Circuit Boards

All circuit boards in the Virginia Tech DACS are wirewrapped except for the I and Q detectors. As would be expected, electrical noise has proven to be a problem on several of the wirewrapped cards. This is at least partially due to the absence of power and ground planes on the wirewrap cards. The other factor to consider is the bundling of wirewrap wires between components. While point-to-point wiring is recommended for reducing electrical noise, it makes debugging more difficult and gives the circuit card a less professional appearance. The best solution is to wirewrap for debugging purposes and then fabricate circuit boards. The cost of fabricating three STDBUS size (4.5" by 6") circuit boards is approximately $400. This number may appear high when compared to the $30 cost of a blank wirewrap card, yet the labor savings in both construction and debugging noise related problems is significantly higher. An additional benefit of printed circuit boards is that spares can be easily constructed.

The PS/2 Microchannel Bus

IBM's Microchannel interface bus is radically different than the standard PC-AT interface bus. Microchannel bus operations occur asychronously and interface cards are configured under software control. The Microchannel bus has advantages in terms of data transfer rate, shared interrupts and the ability to support multiple bus masters. However, the added complexity of the Microchannel bus, coupled with sparse documentation makes interfacing difficult. While a commercial interface card was used for the DACS, modifications were necessary to achieve reliable operation. Presently, a problem remains which the author has been unable to resolve. Since DACS operations are not affected a solution has not be sought. Future designs should either use a computer with the well documented PC-AT interface bus or a Microchannel interface

card which more strictly adheres to IBM's specification.

Data Storage

When the control computer was specified, a storage of capacity of at least one day was specified. The present DACS has sufficient disk space to retain 36 hours of data before transfer to tape is required. Because of the number of students and faculty members associated with the OLYMPUS project, there is usually someone in Blacksburg that can perform daily backups. It is possible, for example, to lose data if a backup is performed at 8:00 A.M. Saturday and the next one occurs at 11:00 P.M. Sunday. This is not a problem because presently, one person performs all backups.

One method to resolve the backup problem is to write the collected data directly to tape. This is not done for two reasons: the tape backup could fail and the present software does not support direct tape writes. Increasing the disk space on the collection computer is the best remedy. As a minimum, three days of storage should be provided. This would allow the tracking station engineer to backup data Friday afternoon after which no backups need be done until Monday afternoon. If funding permits, one week of storage should suffice for all holidays.

Appendix A

Schematics

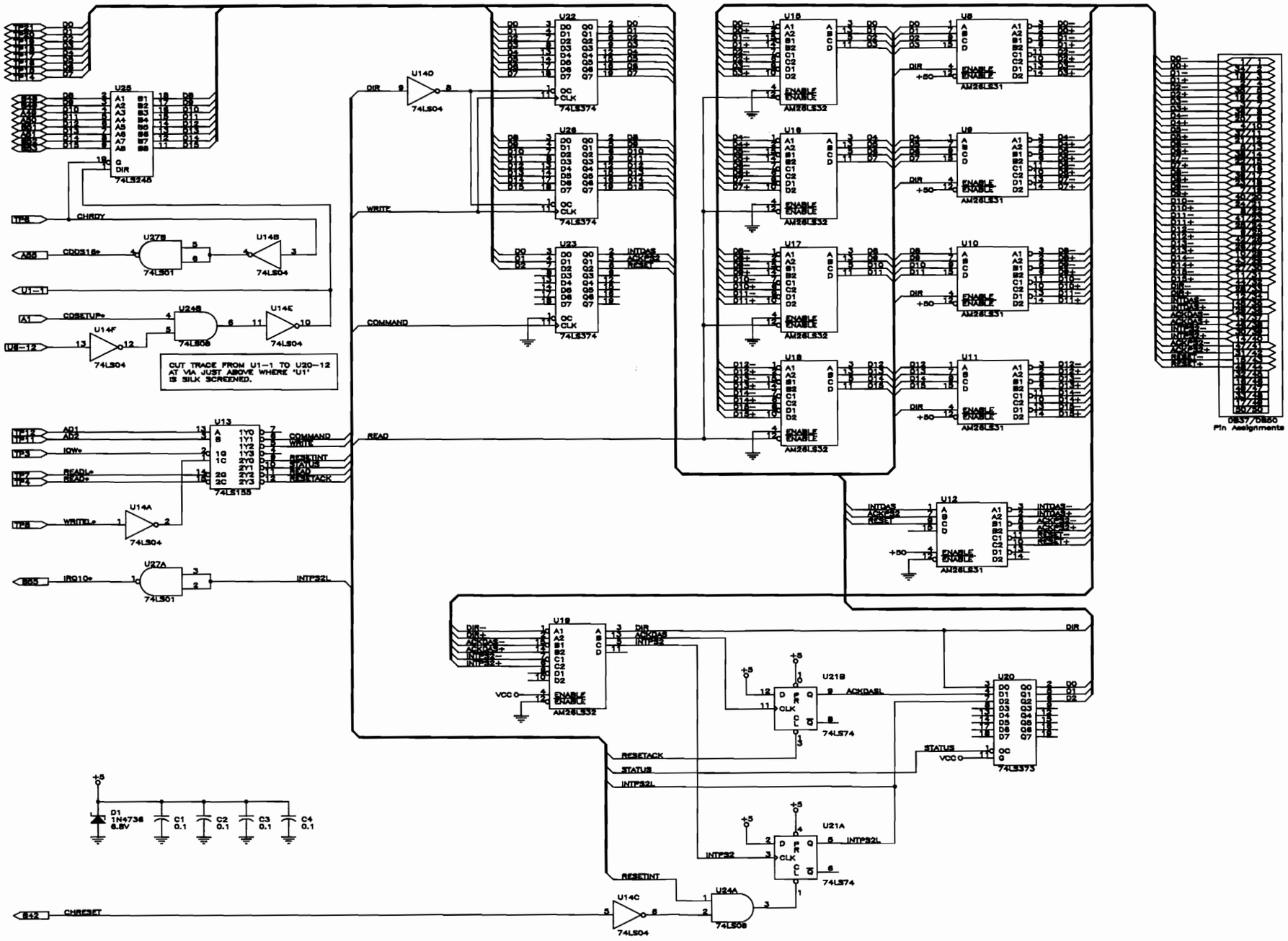

Figure A.1. PS/2 interface card schematic.

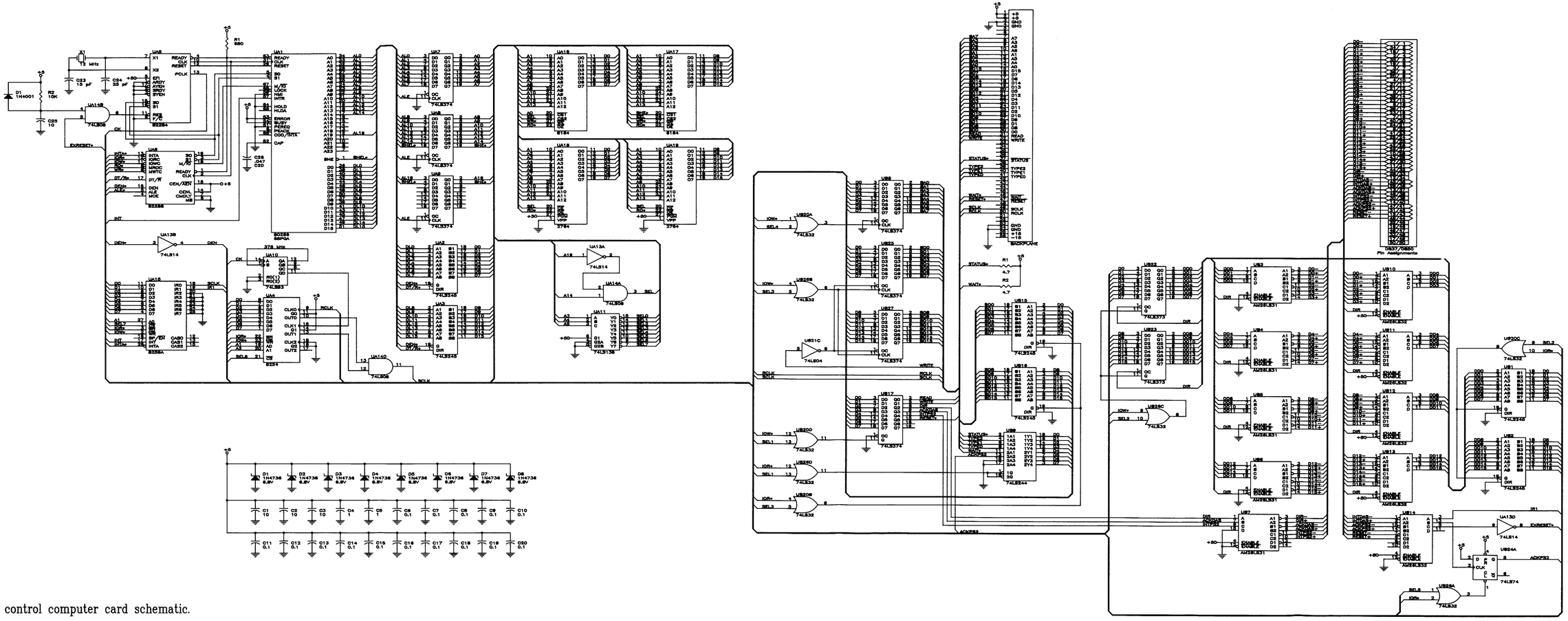

Figure A.2. Backplane control computer card schematic.

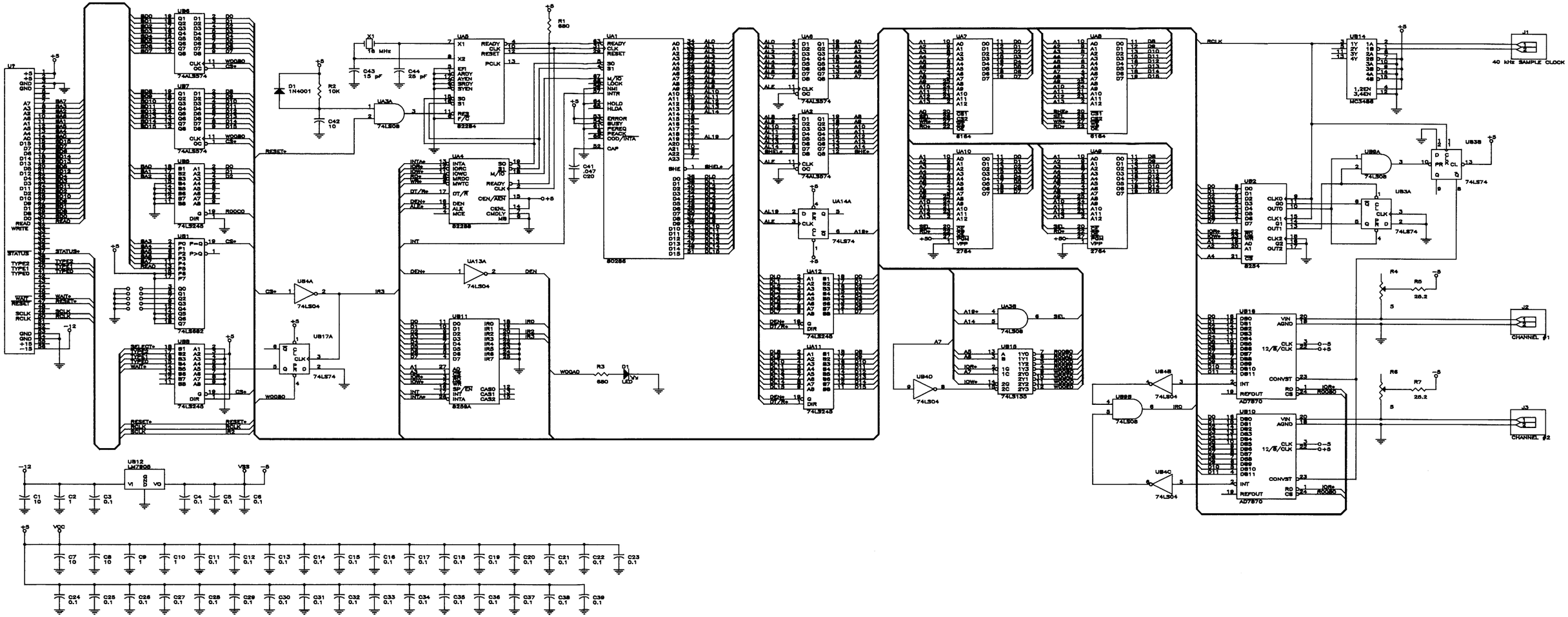

Figure A.3. I and Q detector card schematic.

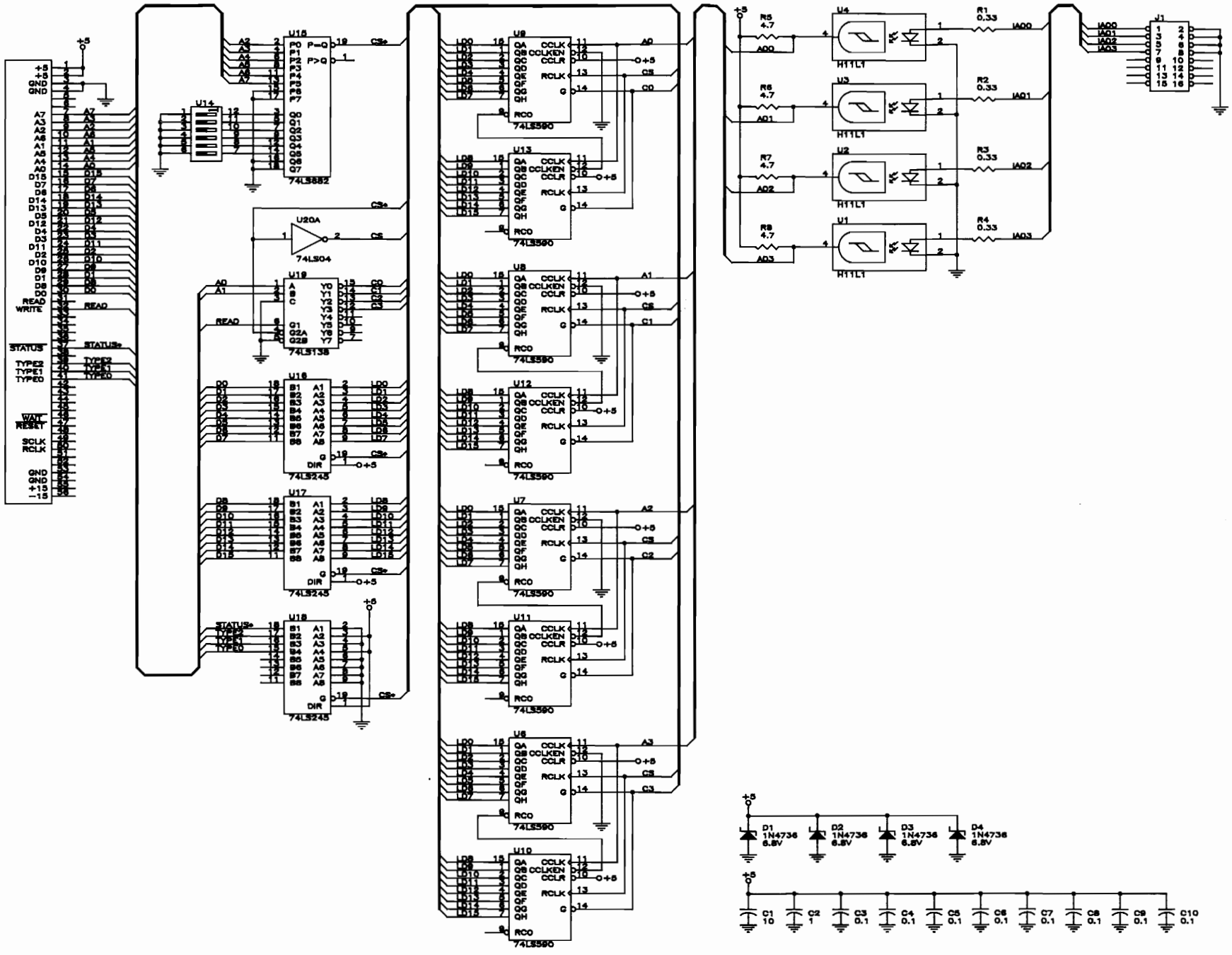

Figure A.4. Radiometer interface card schematic.

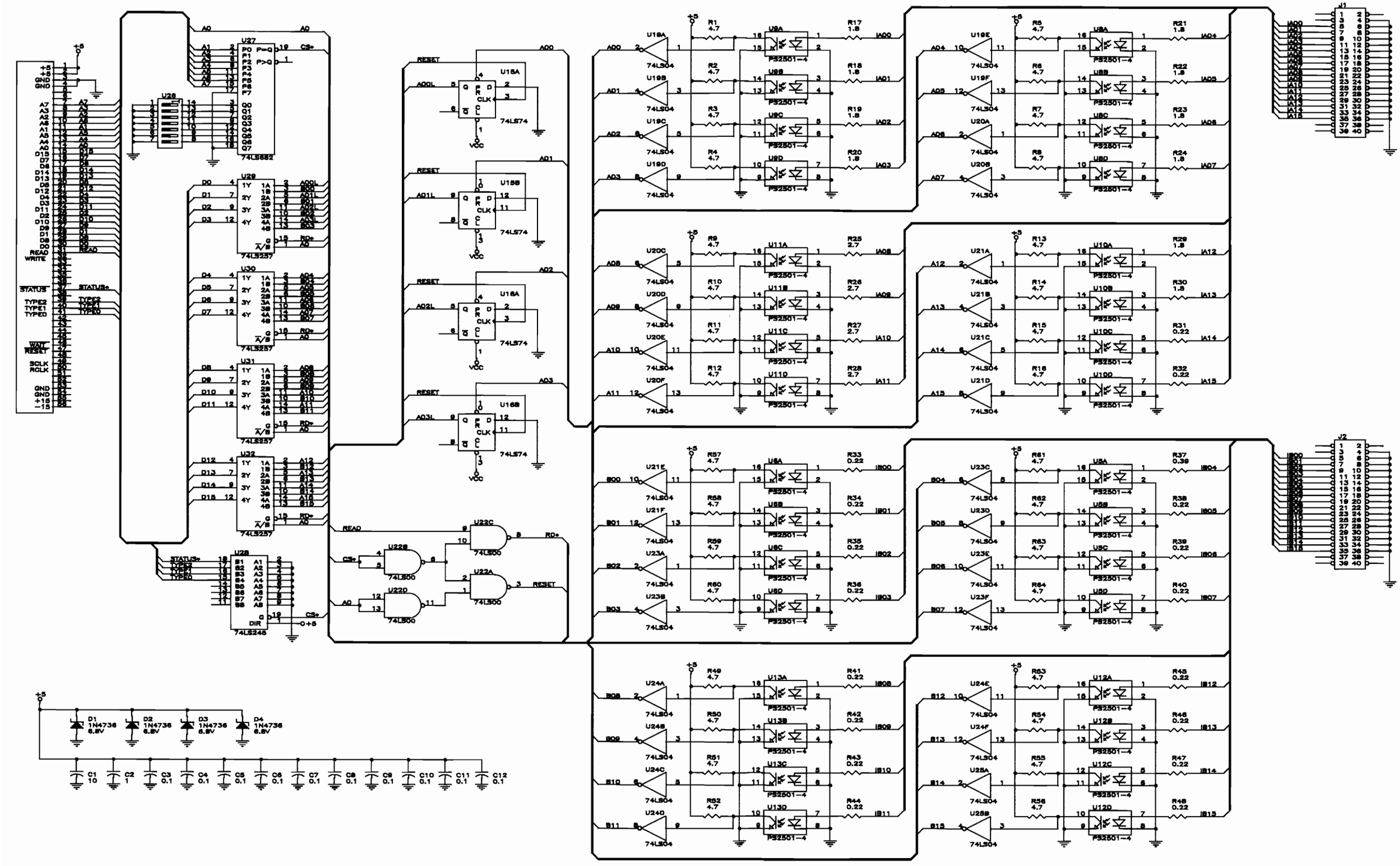

Figure A.5. Digital input card schematic.

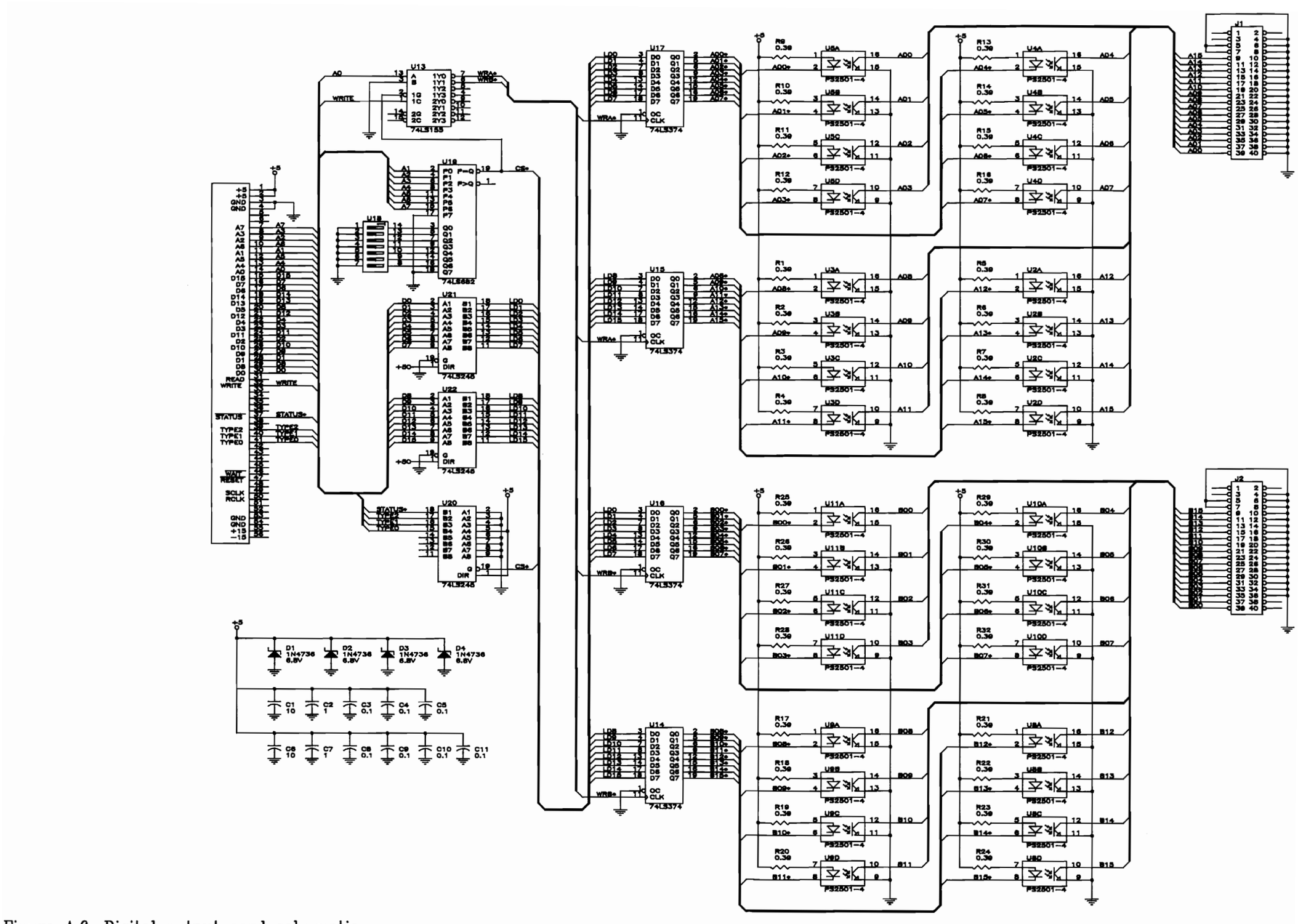

Figure A.6. Digital output card schematic.

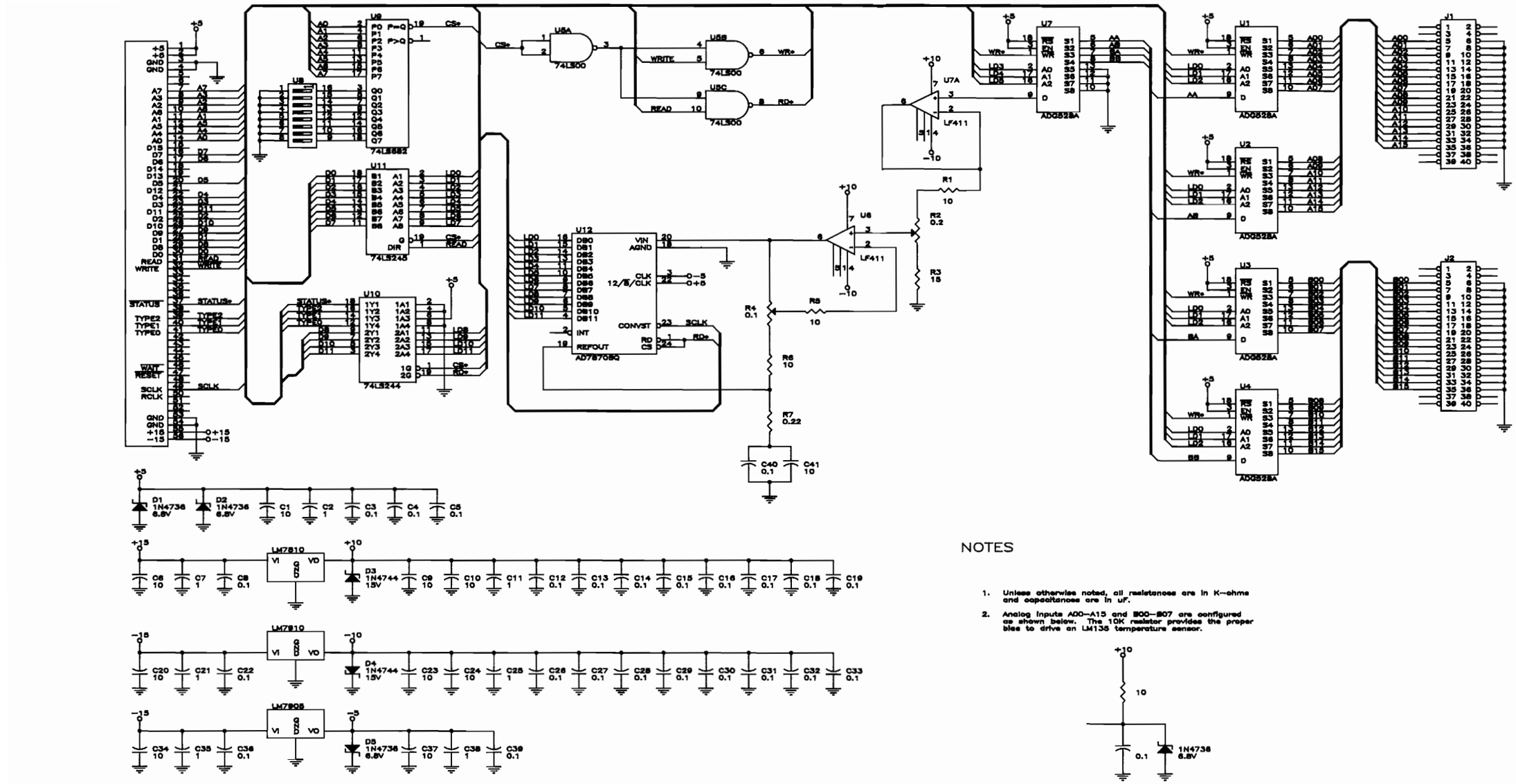

Figure A.7. Analog input card schematic.

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Vita

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