ELECTROMAGNETIC MODELING OF PACKAGING LAYOUT IN POWER ELECTRONIC MODULES

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Electromagnetic modeling of packaging layout in Power Electronic Modules

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(Abstract)

This thesis presents the modeling approaches and the challenges involved in electromagnetic modeling of packaging layout. It discusses the methodologies that are being used today. It then applies these methodologies to analyze, model and characterize three packaging technologies: (i) the wirebond technology, (ii) The Metal Post Interconnected Parallel Plate Structure, and the (iii) Multi Layer Structure. The model developed is validated through experimentation. These models are then used in simulation in order to compare the electrical performance of the packaging technologies.

Finally some problems with the existing designs are pointed out, and suggestions (both local and generic) are given to improve the layout design.

Acknowledgements

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Kalyan Siddabattula.

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1. INTRODUCTION

1.1 Background in Packaging and Power Electronic Building Blocks:

Over the past decade, packaging has become a thrust area of research in power electronics. With the semiconductor industry making rapid strides and developing faster, better performing devices, the onus has shifted to the packaging to derive maximum benefits from these devices. The conventional packaging technology (wirebond technology), which has been the standard in the industry, has been found to be inadequate to handle these high performance, high-speed devices. In fact poor packaging technology and layout may mitigate the advantages that these devices may have to offer, and may even reduce the reliability of these packages. Therefore the need to investigate new, alternative packaging technologies has been felt. This thesis is an attempt to analyze and model two of these new packaging technologies that are being investigated at the Center for Power Electronics Research.

The size and design of a packaging layout and the kind of packaging technology used are determined by a lot of factors. Some important factors include, but are not limited to:

Material properties: The thermal capacity of the materials, the mismatch in Coefficient of Thermal Expansion (CTE) among different layers, and their insulation properties, and the dependence of the properties of the material on temperature, and humidity are some of the factors that effect the layout.

Device properties: The losses in the device, like switching losses, conduction losses, and the reverse recovery of the diode, effect the ratio of the size of the die footprint to the size of the module footprint.

Application: The kind of application that the device has been manufactured for, plays a crucial role in determining the layout. Some applications involve constraints on space, size, and ambient temperature. Constraints also come in the form of type of cooling that is used. All these factors go a long way in determining the layout design and the kind of packaging technology that can be used.

Once the packaging technology and the layout have been determined, these then influence to a great deal the performance of the module. In order to understand the

electrical performance, and to predict the electrical performance of a certain layout and packaging technology, the module needs to be electrically modeled.

Electrical modeling involves characterizing the parasitic inductance and capacitance of the layout and then predicting the electrical performance of this layout. This prediction helps the design cycle because now the designer need not really fabricate the layout to understand performance, reliability, and issues relating to compliance or safety (such as EMI issues) and also allows the designer to optimize the layout design subject to some constraints.

The research effort reported on the methods of extracting parasitic elements in a layout, and interconnects, shows the degradation in the performance of the circuit under the influence of these parasitic elements. There are primarily two approaches that can be used in modeling and characterizing these parasitic elements within the layout. Firstly, there are mathematical tools such as those based on finite element analysis, and tools based on Partial Element Equivalent Circuit (PEEC) [4] methods. A second option would be to use a measurement-based modeling technique such as Time Domain Reflectometry [17].

These techniques, mathematical tools [13]-[16] and measurement [17], have been applied to the problem of identifying the parasitic elements in power electronic modules. There are certain advantages in each of these tools.

The mathematical tools are design oriented and so the designer is able to check the parasitic elements, and then modify the design accordingly. It also lets the designer come up with rules of the thumb, in order to reduce the design cycle time in future designs.

The measurement tools on the other hand is more accurate, since it can account for the shapes and material properties after the module has been packaged, overcoming the problem of having to make assumptions about them. It can also account for non-uniform media in the packaged module. The deformations that take place due to the processing are also accounted for in a measurement-based technique.

This thesis will concentrate on using mathematical tools to model the Power Electronic Modules also referred to as Power Electronic Building Blocks. Power Electronic Building Blocks is a generic term used for modules that are fabricated in the

Office of Naval Research's program to develop modular and integrated power electronic structures that would be used in building converters/inverters with the ability to "plug and play" technology. These are also referred to as Integrated Power Electronic Modules (IPEM) in the power electronics community.

For high power applications, there are primarily two structures into which most of today's power electronic converters can be divided. These are called the basic switching cells (Fig 1). They consist of either a switch with a diode in anti-parallel or switch with diode in series. The former referred to as the Voltage Source Inverter (VSI), and the latter also known as the Current Source Inverter (CSI). Most PEBB structures in this thesis are based on the VSI (Fig. 1.1).

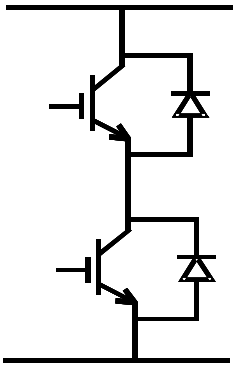

Figure 1.1. The basic switching cell – Voltage Source Inverter

1.2 Motivation and Objectives

The Fig. 1.2 shows the VSI in the form of an electrical circuit and the packaging layout. There is usually a DC voltage source/load on one side of the module and an AC current source/load on the other side. Either of these can be a load, and the other would then be the source. In packaging the above structure into a module, the designer has to consider a lot of factors. The most important of these concerns is thermal. In order to keep the junction temperature of the devices under operable limits, the heat producing devices should be placed far enough, so that the thermal interactions are minimized. In the VSI, it is the two IGBTs (represented by Q_1 and Q_2 in the Fig. 1.2). The corresponding diodes D_1 and D_2 are placed in proximity to the IGBTs. The bottom surface of the devices is the collector in the case of the IGBT and the cathode in the case of the diode. The top surface of the die is the emitter of the IGBT and the anode of the

diode. Once the tracks have been etched on a copper substrate, forming the layout, the devices are then placed in their corresponding positions on the substrate. These tracks connect the bottom surfaces of the dies. In Fig. 1.2, the track T_1 that connects the top half to the bottom half can be seen.

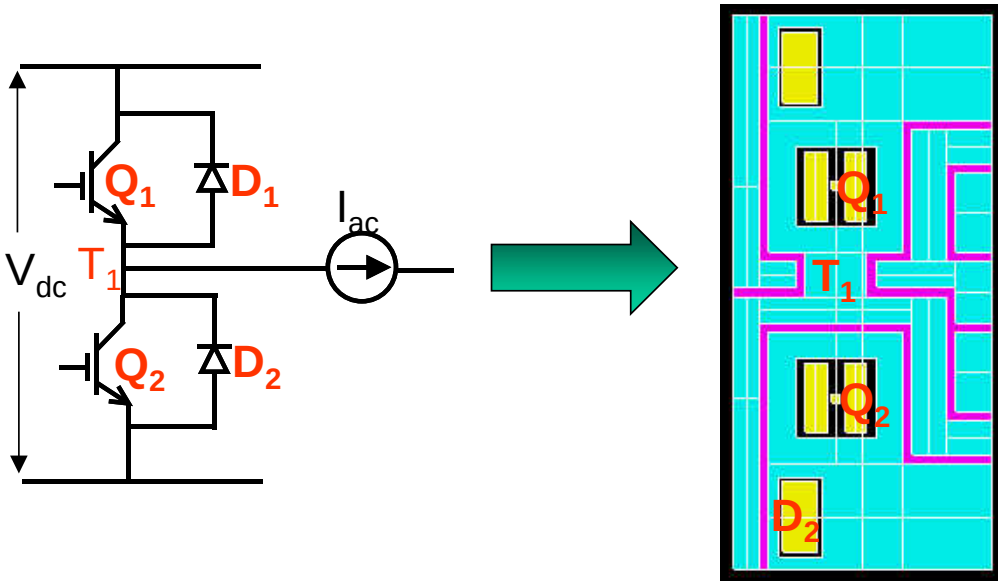

Figure 1.2. The layout and electrical circuit of a VSI power module

The problem now is to connect the top surface of the IGBT to various points on the layout. In order to do this, and thereby complete the circuit, wirebonds are used. Wirebonds are aluminum wires usually 10-20 mil in diameter, and the connection is made by a combination of pressure and ultrasonic energy. These wirebonds are referred to as interconnects throughout the length of this thesis. This is referred to as the wirebond technology or the two-dimensional packaging. Another approach may be to use another substrate on which some part of the layout that is seen in Fig. 1.2 is etched, and the devices are sandwiched between the two substrates. The interconnects are then in the form of copper vias or posts. This technology of using two or more layers of copper for the tracks is known as three-dimensional packaging.

There are some immediate advantages with a three-dimensional packaging approach. Because of the additional degree of freedom that this offers, the design may be optimized for the best possible performance. Also the three dimensional structure means shorter interconnects (as shall be seen later).

Another advantage that three-dimensional packaging offers is that unlike the two-dimensional packaging, an additional path for heat flow exists. Hence the thermal capability of the module for the same footprint size is higher and so the module may be operated safely at a higher temperature or at higher frequency or both.

There are two major structures being developed as a part of this research thrust:

(1) Metal Post Interconnected Parallel Plate Structure (MPIPPS): The MPIPPS structure uses direct bonding copper posts (dimensions: 1.1 mm, 1.1 mm, 3.5 mm), as interconnects. Since the current carrying capability of the copper posts is much higher than the current capability of the wirebonds, a single post may replace two or three wirebonds. The switch and diode are attached to the bottom DBC substrate. The copper posts are then soldered onto the pads on the device, which have been made solderable. Any other devices, active or passive, such as those in the gate driver may be attached to the top DBC substrate with the required pattern etched on it. This DBC substrate is then attached to the posts in order to complete the structure.

(2) Multi Layer Structure (MLS): The Multi Layer Structure (MLS). This is often referred to as the Multi Layer Integration Technology (MLIT). This structure uses multiple layers, in this case four, to create the VSI. The copper vias between the layers serve as interconnects.

The packaging layout, and the nature of the interconnects then affects the electrical performance of the module. There are parasitic elements (inductance, resistance and capacitance), which may degrade the electrical performance of the module.

In order to evaluate the electrical performance of a packaging technology under the influence of these parasitic elements, certain indices have been picked.In power electronics, the most common action is that of turning off and turning on of a switch. Therefore the turn on and turn off characteristic have been chosen to identify the indices. In this thesis, when evaluating any packaging technology, the following performance indices will be considered:

(1) Voltage Overshoot during Turn-Off

(2) Rise and Fall times

(3) Settling time during Turn-Off

(4) Current distribution between interconnects

The voltage overshoot is determined by loop inductance and fall time of the current. By improving the layout and choosing thermally superior material such as Aluminum Nitride ceramic substrate [10] and also by adjusting the ratio between the chip and module footprint, the loop inductance is reduced, which results in lower voltage overshoot. This is turn enables shorter rise and fall times. The inductance of interconnects, appropriately termed parasitic inductance, stores energy when the switch is on and this energy is then discharged when the switch turns off. This appears as voltage overshoot in the turn-off characteristic. Good layout and better packaging technologies only help to reduce the overshoot but do not eliminate it. Hence a snubber (typically RCD) is often needed to overcome this problem**.**

The objective of this thesis is to understand and critique the packaging layout and technologies from an electrical performance stand point, based on the indices that have been picked. In order to do this, the packaging technologies have been modeled using mathematical modeling techniques, and performance (based on these models) has been used to understand the packaging technology.

1.2.1 Methodologies of Electrical Modeling – a discussion

Electrical modeling of a layout primarily consists of understanding the parasitic elements that lie in the circuit. These parasitic elements store energy during certain operations and discharge this energy during other operations, and may cause degradation in performance. Electrical modeling can be done by using Finite Element based software such as Maxwell.

Once the geometry and the materials have been defined, Maxwell then finds the required parameters and fields in the geometry. Since there is no single analytical expression that describes the entire geometry, Maxwell divides the entire problem region into many smaller regions and represents the field in each small region with a simple polynomial or polynomial expression term using Maxwell's Equations. This collection of smaller regions (each smaller region is called an element) is referred to as a mesh. The user may also choose Adaptive Analysis to instruct Maxwell to perform an adaptive

solution. During this process, the system iteratively refines the starting mesh in order to reduce the size of the elements in regions of high error. The parameter “Percentage Refinement Per Pass” determines the increase in the number of elements in the problem region. The iterative process ends when the required percentage error has been obtained, or when the specified number of passes has been completed, whichever occurs earlier. In addition to the approximate solution of Maxwell’s equations, Maxwell can extract equivalent lumped parameter parasitic components using the utility called Quick 3D parameter extractor.

Internally, Maxwell Q3D computes the inductance of good conductors as if they were perfect conductors (perfect conductors have current flowing only on the surface of the conductor). However, it computes resistance as if the conductors were made of copper and assumes that they carry a 100 MHz signal. The user may then calculate the resistance at any other frequency by changing the frequency. Then Maxwell uses an approximate formula to calculate the resistance at the desired frequency [1].

$$\frac{R_{acnew}}{R_{acold}} \approx \sqrt{\frac{f_{new}}{f_{old}}} \tag{1.1}$$

In order to calculate the Capacitance Matrix that is associated with the 3-D geometry, the Maxwell Q3D performs the following steps;

- It computes the charge Q, on each object using a multipole expansion [1], [2]
- From charge calculated, it computes the capacitance matrix.

To compute the charge, the Maxwell Q3D extractor uses the boundary-element technique.

However, any finite element based analysis is CPU intensive and extremely time consuming. Therefore it is not suited to changing certain parameters, and then observing the effect of these changes on performance. A finite element analysis is therefore not conducive to an iterative design procedure. In order to quickly extract the parasitic inductance of a layout and to design a layout, another software known as INCA has been used.

INCA (Inductance Calculation) is software, which allows different types of coupling within a layout to be characterized, such as resistance, inductance and/or mutual

inductance between conductors. It uses the PEEC method (Partial element Equivalent Circuit) developed by A. E. Ruehli [4]. This method is based on closed form analytic formulae, which for low frequencies result from very complex calculation [5].

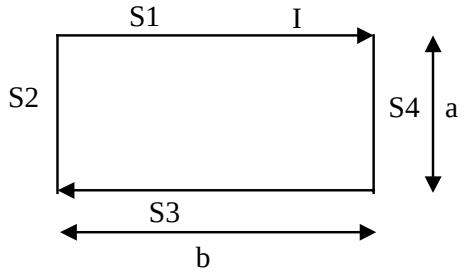

Figure 1.3. Rectangular Loop

In order to illustrate this concept we may use the following current loop shown in Fig 1.3

The inductance of the current loop thus built is:

$$L_b = \frac{1}{I}\int\oint \vec{B}.d\vec{s} \tag{1.2}$$

where $\vec{B}$ is the field created by the current I and $d\vec{s}$ is the vector along the normal oriented out of the paper.

Inductance can also be written according to magnetic vector potential $\vec{A}$, so that $\vec{B} = rot\vec{A}$. Using Stokes theorem

$$L_b = \frac{1}{I}\int_c \vec{A}.d\vec{l} \tag{1.3}$$

L_b is therefore the result of the vector potential circulation along the contour C of the current loop. However, this circulation can be split up over each of the four segments of the circuit where

$$L_b = \frac{1}{I}\left[\int_{segment1} \vec{A}.d\vec{l} + \int_{segment2} \vec{A}.d\vec{l} + \int_{segment3} \vec{A}.d\vec{l} + \int_{segment4} \vec{A}.d\vec{l}\right] \tag{1.4}$$

Since the vector potential at any point is the sum of the vector potentials contributed by each segment,

$$L_b = \frac{1}{I}\sum_{m=1}^{4}\sum_{n=1}^{4}\int_{sm}\vec{A}_{segmentn}.d\vec{l} \tag{1.5}$$

Partial and mutual inductance is defined by

$$M_{pnm} = \frac{1}{I}\int_{sm}\vec{A}_{sn}d\vec{l} \tag{1.6}$$

$$L_b = \sum_{n=1}^{4}\sum_{m=1}^{4}M_{pnm} \tag{1.7}$$

If m=n: L_b is partial inductance,

Otherwise, L_b is mutual inductance [5].

However the formulae derived here assume that the current density in the conductor is uniform. These therefore are not applicable to power electronics, where a rich harmonic content causes uneven distribution of the current. At higher frequencies, current crowds at the periphery of the conductor. This is known as *skin effect.* A neighboring conductor also affects the current distribution in the conductor. This is referred to as *proximity effect.* INCA models these effects by subdividing the conductor into several filaments in which the current density may be assumed uniform. Usually the number of filaments at the periphery of the conductor is higher since the current density is higher. Figure 1.3 shows these subdivisions in a typical conductor.

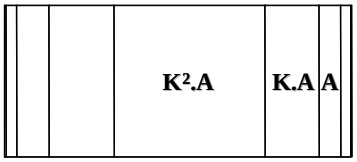

Figure 1.4. Subdivisions within a conductor

By appropriately choosing the number of subdivisions, and the ratio between adjacent subdivisions, a very accurate estimate of the parasitic inductance may be obtained. The ratio between areas of adjacent squares is shown as K in Fig. 1.4. This is very important in the analysis of a given conductor. The only subdivided objects are polylines. Subdivisions are automatically performed once the ratio **K** has been defined. In order to do this, each polyline needs to be modified with respect to ***concentration of subdivisions*** on X and Y-axes and ***number of subdivisions*** on the X and Y axes.

1.3 Summary and outline

In this chapter we presented the necessary background in packaging and modeling, the aims and the objectives in packaging, and the scope of this thesis. A brief introduction to the conventional two-dimensional packaging (wirebond technology) and its inherent defects was given, and the reasons for its wide usage were listed. We then explored the possible solutions to the problems that the two-dimensional technology and in this process briefly introduced two concepts:

(1) Metal Post Interconnected Parallel Plate Structure (MPIPPS)

(2) Multi Layer Structure (MLS) or Multi Layer Integration Technology (MLIT)

The advantages and disadvantages of each approach were then discussed. An early introduction into the methodologies of electrical modeling was given, and the issues associated with each approach were discussed. A simple analytical approach was also presented. With these in mind we may proceed to the following chapters.

This thesis is divided into two broad parts. The first part will analyze the conventional wire-bond technology which is primarily a two dimensional technology and the alternative packaging technologies. The second part compares the different packaging technologies, and then discusses the advantages and drawbacks of each technology and the reasons for them. Finally some design ideas and suggestions for the alternative forms of packaging are presented.

2. CONVENTIONAL TWO-DIMENSIONAL PACKAGING

WIREBOND TECHNOLOGY

2.1 Introduction

Wirebond technology is the most widely used packaging technology in the electronics industry, primarily due to its cost effectiveness and simplicity. In power electronics, it is used to connect the semiconductor die to some other part of the substrate or to connect two semiconductor dice together. Ultrasonic Aluminum wirebonding is the most widely used form of wirebonding in the industry today. In this process stitch bonds are formed at both ends of the interconnect by a combination of pressure and ultrasonic energy (60,000 times per second at the tool). As the wire softens, freshly exposed metal in the wire comes in contact with the freshly exposed metal on the pad and a metallurgical bond is formed. Aluminum wire is typically doped with 1% silicon to more closely match the hardness of the wire with that of the bond pad material. Both gold and aluminum wire are used extensively today in packaging [9]. A figure showing a typical wirebond is shown in Fig. 2.1.

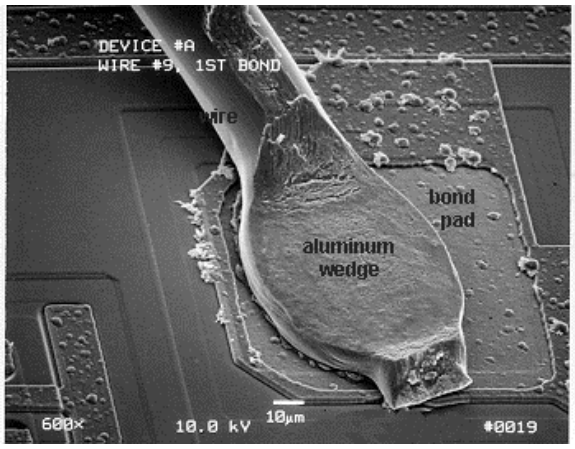

Figure 2.1. SEM photograph (400X) of an aluminum ultrasonic wedge bond [9]

The objective of the wire bonding operation is to develop a low cost, high yield interconnect process with a sufficient long-term reliability. There are many aspects of the wire bonding process that must be considered, besides the physical placement of the bonded wire. The wire metallurgy and aging effects, the wire diameter and elongation, surface cleanliness of the bond pad, potential failure mechanisms, the degrading effects

of temperature, the materials and morphology of the bond pad metallization can all adversely affect bond quality [9].

High reliability and long term stability are essential in high power applications. For example electronics used in traction purposes, in a 30-year lifetime, are exposed to 33800 long-term cycles and 12 million short-term temperature changes. There are serious reliability problems associated with wire bond technology due to proximity effects resulting from coupling effects in bonding wires, uneven current distribution among IGBT cells in one chip and paralleled IGBT chips, and mechanical forces that cause the peeling of the aluminum coating [6].

In this chapter, we will investigate the wirebond technology from the electrical characteristics and performance point of view. In order to do this, a commercially available wirebond module (MII 75-12A3 manufactured by IXYS) was chosen and modeled along the lines described in Chapter 1. First the INCA model of the module was developed, to gain insight into the parasitic inductance of the interconnects and the tracks and leads in the layout. Then a model in Maxwell parameter extractor and field simulator was developed. These models give insight into the parasitic capacitance (especially to the ground), and an idea about the current distribution among the interconnects. It was found that there are problems associated with this technology and some of the results obtained may explain the common problems that are associated with wirebonds.

2.2 INCA Model of the wirebond module

In order to develop an accurate electrical model of the module, the inductance and the AC resistance of the conductors have to be accurately determined. To calculate resistance and the inductance of conductors, two effects need to be accounted for (1) skin effect, which is the crowding of the current at the periphery of the conductor, and (2) proximity effect, which is the uneven distribution of current due to the magnetic field of the adjoining conductors. The methods to account for these effects have been described in the earlier chapter.

The parasitic capacitance in the module also has to be modeled. It will be shown later that the parasitic capacitance is very low compared to the output capacitance and the gate capacitance of the devices. The only important parasitic capacitance will turn out to

be the capacitance from the drain of the device to the ground, which influences the conducted EMI levels to a great degree.

In developing the INCA model of the module, the geometry of the module first needs to be drawn in INCA. In order to account for the direction of current flow the geometry needs to be divided into an optimum number of elements (each of which is a polyline). The direction in which the polyline is developed (polylines are developed by sweeping a cross-section profile along a line) gives the direction of the current flow. Therefore it is very necessary to understand the direction of the current flow and the elements through which it flows. In order to get a rudimentary understanding of how the current flows, it is a good idea to model the geometry first in Maxwell, understand the current flow and the model accordingly in INCA. The electrical conductivity for the materials used in the model (like copper, ceramic) needs to be defined. Once this has been done, then the polylines within the model will have to be subdivided to account for skin effect and proximity effect.

Once the critical polylines have been identified and finely subdivided, the frequency of the sources of excitation need to be defined. These are the frequencies at which the analysis will be performed. The parameters may then be extracted in the form of a PSPICE/SABER netlist or in a matrix form.

The inductance matrix consists of self-inductance of each element as well as the mutual inductance of each element with all the other elements in the model. In order to simplify the model we may omit the more insignificant terms by inspection and develop the PSPICE/SABER model. Throughout this thesis, this is the procedure that has been followed. This PSPICE/SABER model then is used with the corresponding simulator to evaluate the performance of a packaging technology.

2.2.1 Examination of the parasitic inductance in the wirebond module

The Fig 2.2 shows the INCA model (see Appendix I) of the wirebond module MII 75-12A3. This module is rated for 1200 Volts and 75 Amps. This is the rating of the other modules in this thesis. The model of the wirebond itself has been developed as a rectangular loop. The actual shape of the wirebond is very random and difficult to predict once the module has been sealed. Therefore the rectangular shape was chosen. This shape

makes the analysis in INCA easier. Once the parameters of all the elements have been extracted (at a frequency of 20 KHz), they are then mapped onto their corresponding elements. An equivalent circuit has been drawn to show the self-inductance of each element. The mutual inductance has not been shown in the figure in order to maintain the clarity of the figure. The AC resistance of each element has also been omitted in the figure.

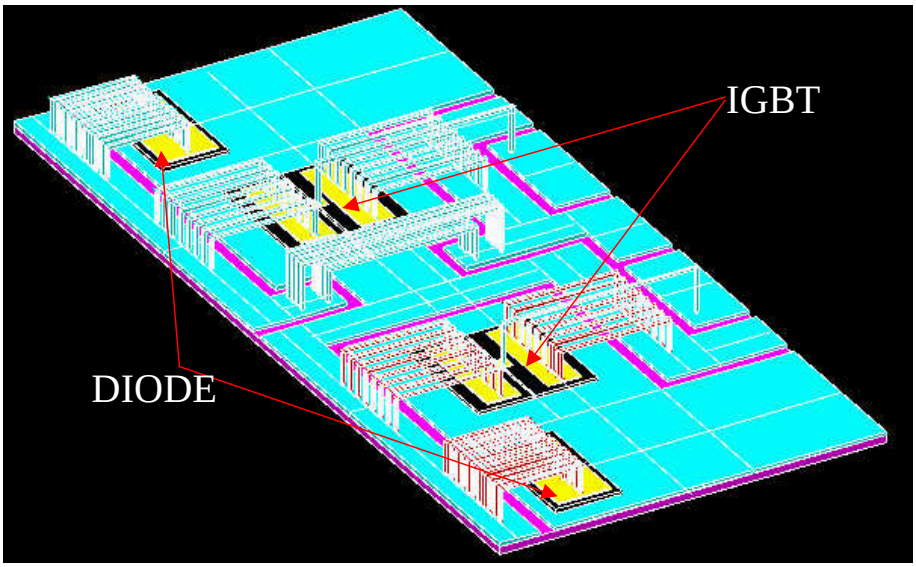

Figure 2.2. The INCA model of the wirebond module MII 75-12A3

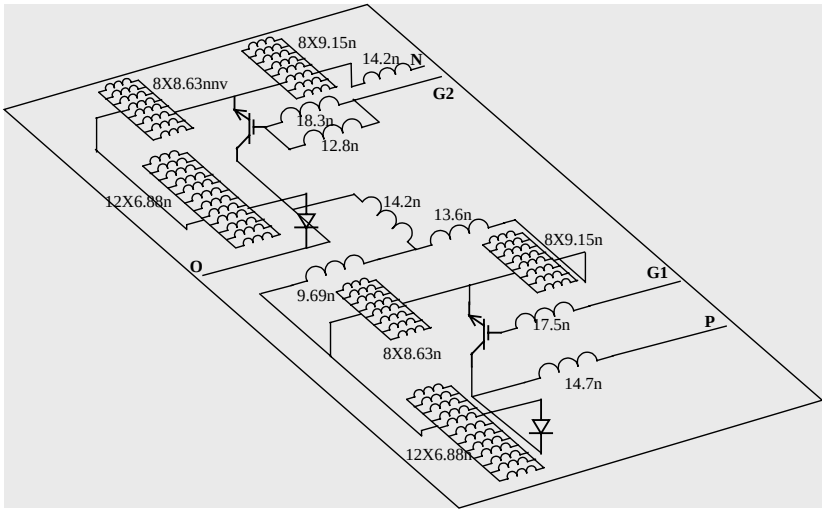

Figure 2.3. The equivalent parasitic inductance model for module MII 75-12A3

As can be seen from the Fig 2.3, the parasitic self-inductance of the wirebonds is quite significant. This added to the inductance of the tracks and leads themselves is quite

large and can cause considerable degradation in the performance of the module. In order to get a better idea of the inductance of each element a closer look at the INCA and the equivalent model have been shown below [18].

As mentioned before, the mutual inductance has not been shown here. In order to gain a better understanding of the model a tabular form of values is presented below.

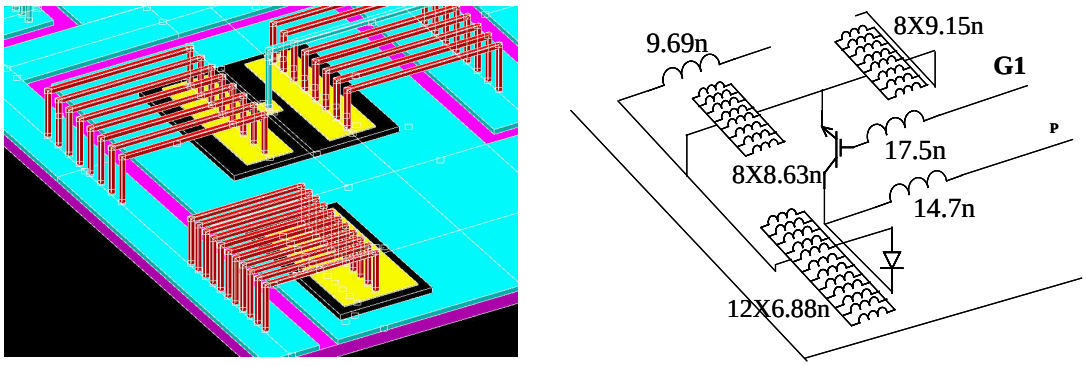

Figure 2.4. A closer look at the INCA model and the equivalent inductance model

Table I. The inductance values of the wirebond module

No.	Name of the element	Self-inductance	Comment
1.	Wirebond for IGBT Emitter	8.63nH	Mutual inductance between wirebonds is 4nH
2.	Wirebond for diode	6.88nH	Mutual inductance between adjacent wirebonds is 5nH
3.	Wirebond for gate lead	17nH	Causes excessive ringing.
4.	Track to IGBT Collector	14nH	Causes larger overshoots
5.	Loop inductance	28nH*	This is debatable

*The loop (from the top switch to the bottom diode or vice versa) inductance is difficult to determine since the path taken by the current is not very clear. Therefore the elements that will influence the inductance are difficult to determine. This is at best an astute guess. The Maxwell software can give the loop inductance if the loop is defined, since it accounts for the current flow in the elements. Before any conclusions can be

drawn about the model and the effects that these significant inductance have on the performance, the model needs to be verified. In order to verify any analytical model the results from the analytic procedure must be correlated to the experimental results.

2.2.2 Verification of the INCA model

A test setup was chosen to evaluate the performance of the chosen module on the indices that were decided upon. Once this was done, the test setup was simulated as closely as possible along with the model that was developed. The performance indices were then compared. A close correlation between the indices would mean a more accurate model. The test setup and the testing procedure are described below.

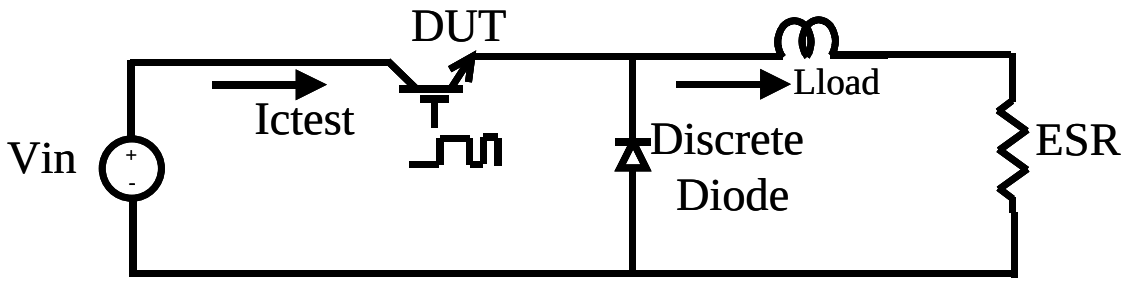

Figure 2.5. The Test Setup

The test setup consists of the Device Under Test (DUT), a discrete freewheeling diode, and an Inductive load. The DUT is first turned on letting the current in the inductor build up to the desired value. Then the DUT is turned off and then after a very short interval (compared to the initial turn on time) is turned on again. It is then finally turned off. The turn off of the first pulse and the turn on of the second pulse are considered for the turn off and turn on characteristics (Fig. 2.5).

These characteristics are used to determine the indices (Voltage overshoot, Rise and Fall times, and the settling time) are determined. These indices are used to compare experimental results to the simulation results and after the model has been validated, they can be used to compare different packaging technologies.

A good correlation between the indices obtained through the experiments and the indices obtained by simulating the experiment in PSPICE would validate the model and also indirectly validate the modeling procedure.

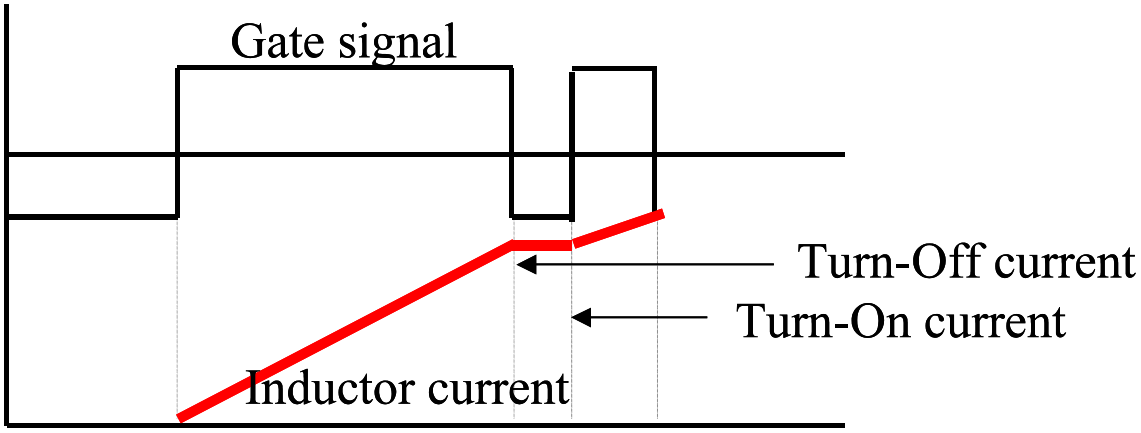

Figure 2.6. The turn on and turn off waveforms in the test setup

2.2.2.1 Experimental results

The experimental results for the module in the test circuit described above are shown below in Fig. 2.7. The simulation results from PSPICE are shown in the Fig. 2.8. The tabular form Table II given after the figures compares between the experimental and the simulation results.

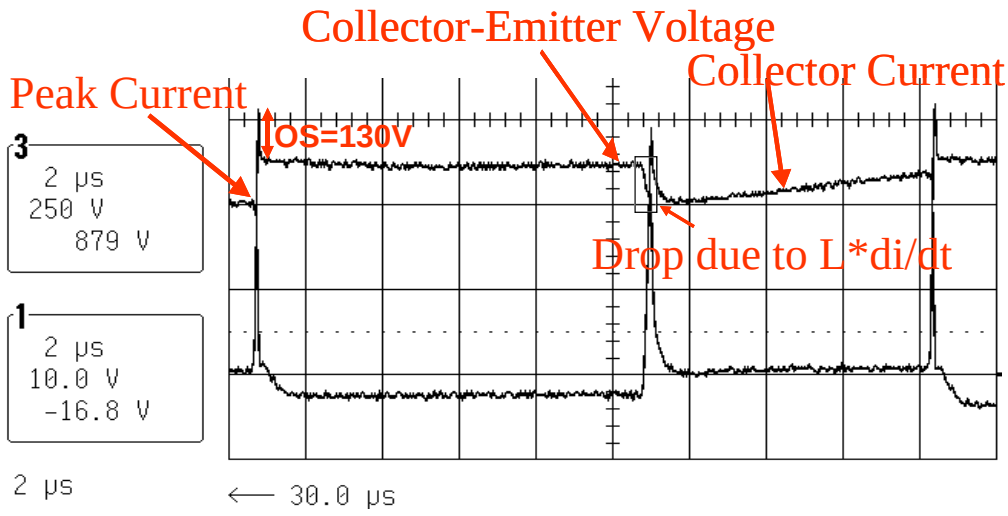

Figure 2.7. The experimental results for a wirebond

The experiment was performed on a 630 V bus voltage and by using 200µH inductor with a very low ESR. The inductor current is allowed to ramp up to 90A and then the switch is turned off for the first time. Then the switch is turned on after 5 µsec. This is where the turn on is observed. Then the switch is turned off when the inductor current

reaches the peak value of 100A. This test provides no thermal stress to the device of the package but shows the electrical performance of the module.

2.2.2.2 Simulation results of the model in PSPICE

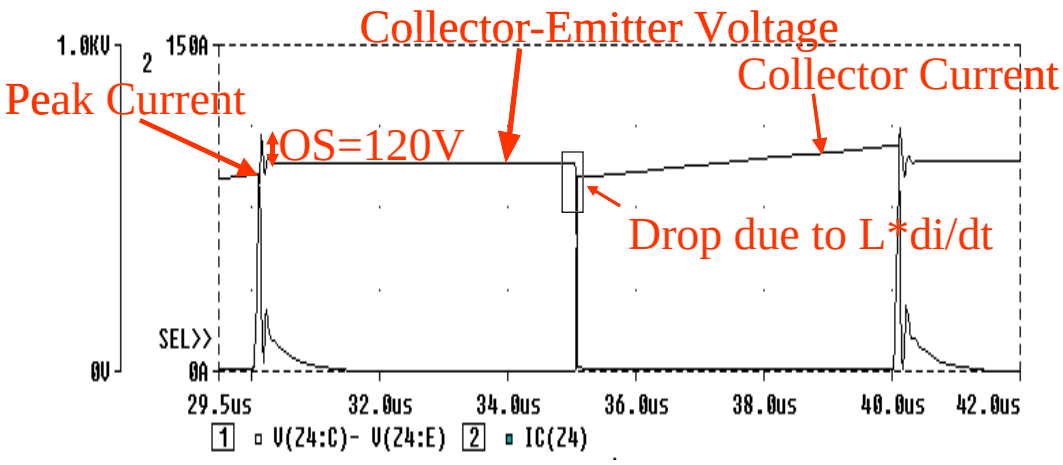

Figure 2.8. The simulation results of the wirebond module

The Fig. 2.8 shows the performance of the model in the simulation of the tester. In order to do this, the model developed from INCA is taken and the device model is added to the circuit model. Then the netlist is simulated in PSPICE.

2.2.2.3 Comparison

Table II. Comparison between experimental and simulation results

Performance Index	Experimental	Simulation
Voltage Overshoot	130V	120V
Rise time	0.4µsec	0.6µsec
Fall Time	1.2µsec	1µsec
Settling Time	0.6µsec	0.4µsec

The above table and the waveforms show that the model is accurate within the realm of experimental and modeling errors. This means that this model can now be used in future simulation and also in comparison with other technologies.

2.3 Maxwell model of the wirebond module

This section presents the extraction of the parasitic capacitance, its effects and implications and methods to reduce the adverse effects of the parasitic capacitance. It also shows analysis of the current distribution in interconnects. EMI is closely related to the parasitic elements. Although the EMI regulation specifications target the total EMI emission, the noise can be divided into differential mode and common mode. Generally, the magnetic coupling causes the differential mode noise when the loop inductance experiences large slew rate currents. These also cause radiated EMI. On the other hand the common mode EMI is due to the capacitive coupling, when exposed to large slew rate voltages. In this section though we do not present any EMI analysis, we study the elements that largely determine this common mode EMI.

The common mode capacitance consists of the capacitance between the electric nodes that experience voltage change and chassis ground is the case of PEBBs. The chassis ground is often the heat sink. Therefore, the parasitic capacitance between the collector of the IGBT and the chassis ground (in this case the heat sink) needs to be studied.

2.3.1 Examination of the parasitic capacitance in the wirebond module

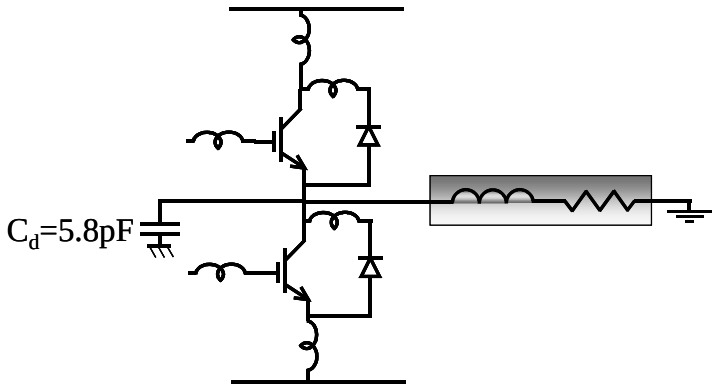

Figure 2.9. The parasitic capacitance from the collector to the chassis ground

After the model has been developed in Maxwell and the materials assigned to each element, in order to calculate the capacitance of the conductors the voltage on each conductor needs to be defined. Finally the conductors that are to be included in the capacitance matrix are chosen. The conductors that are not chosen are known as passive

conductors and are assumed to be the ground conductors. In the case of the wirebond module, the bottom of the DBC substrate is made the ground. Then the matrix is extracted based on the geometry and the materials. Our primary concern in this case is the capacitance from the collector of the IGBT to the ground. This is shown in Fig.2.9.

This capacitance is used in EMI modeling. Although no EMI modeling is being done in this thesis, this value will be useful in comparing with capacitance in the case of three-dimensional technologies.

2.3.2 Current distribution in the interconnects in the wirebond module

A major concern about the wirebonds is their proximity, and therefore the large coupling that exists between wirebonds. The high levels of flux linkage cause significant mutual inductance, which means that when several wirebonds are in parallel, the current distribution among the wire bonds is never uniform. The mutual inductance between the wires induces the current in the opposite direction in the wires in the center, thus making the effective current lower in the wirebonds in the center; this is referred to as *proximity effect*. This effect causes increased losses and since this effect is accentuated during transients, it puts stress on the wirebonds and may reduce the lifetime of wirebonds.

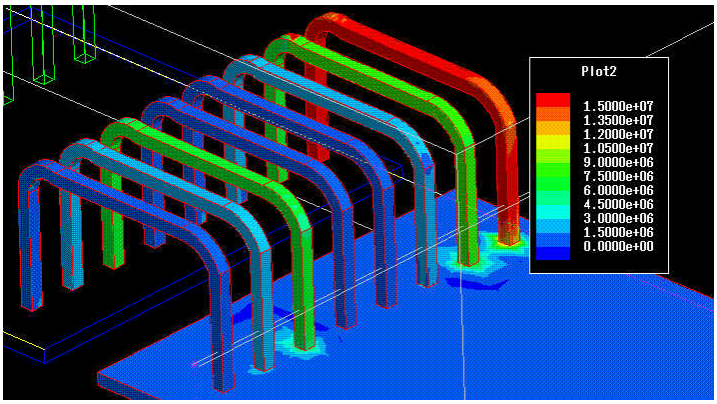

Figure 2.10. The wirebond model to study the proximity effects

In order to study this effect the module was modeled in Maxwell 3-D field simulator. Once again, the geometry is defined and then the materials defined, the current sources are defined. Maxwell will now calculate the fields at every point. Then the current distribution at each point may be studied. It must be remembered that the currents here

are sinusoidal in nature and all interfaces and materials are assumed to be uniform. This however is not the case in reality and a short discussion about this will be presented later.

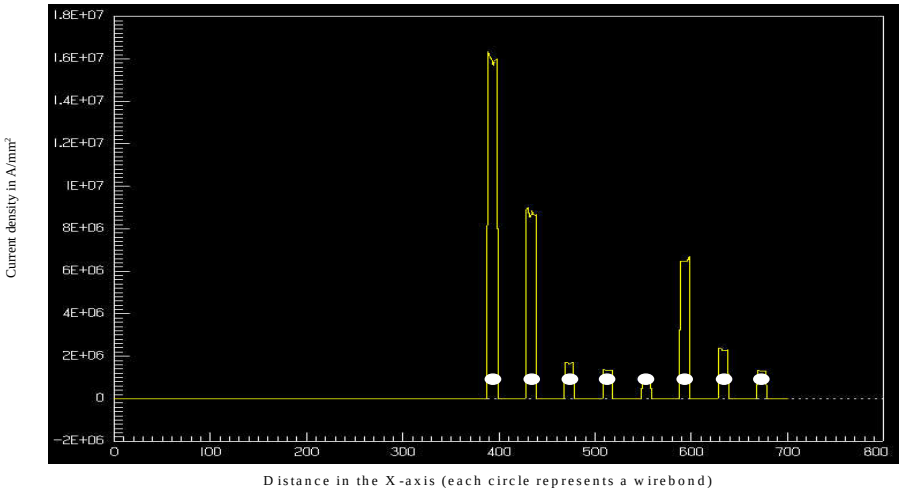

Figure 2.11. The current distribution among wirebonds

Fig. 2.10 shows the current distribution among the wirebonds. It can be seen that wirebond on the extreme right carries the most current. The wirebonds in the middle carry almost no current. On the other hand, the wirebond third from left also carries significant current. The above figure shows a graph where the current distribution among wirebonds has been mapped along a straight line running through the wirebonds. This corresponds to Fig. 2.10. The wirebond on the extreme right in Fig. 2.10 has the highest current density. This is the highest peak in Fig, 2.11. It can be seen that the current in the extremes is about eight times the current in the center wirebonds. The higher peak occurring in the third wirebond from the extreme may be due to the fact that there are additional tracks present in close proximity to the wirebond in the extreme right in the Fig. 2.10 and therefore the mutual inductance between the track and the wirebond may cause more current to flow through the third wirebond from the right in the Fig. 2.11.

This causes stress, electrical as well as mechanical, on the wirebond. This may lead to the wirebond peeling off the Aluminum coating on the top [6]. This analysis was performed with a unit Ampere current and at 10KHz frequency. This analysis at higher frequencies is very CPU intensive and also very time consuming. This however gives an idea of the current is distributed among wirebonds in parallel.

Since this effect primarily depends on the mutual inductance of wirebonds, it is safe to assume that this effect will be more accentuated at higher frequencies. Most power electronics involves quick rising and falling edges, which contain harmonics. The losses in the wirebonds due to this effect are much higher than in interconnects in the three-dimensional packaging.

2.4 Drawbacks of two-dimensional packaging

There are very serious drawbacks associated with two-dimensional packaging. Firstly the self-inductance of the tracks and the wirebonds is very significant. This has been shown to cause a overshoot of 130V on a 630V bus. This inductance is not only detrimental to the turn off process but also because of the high inductance, it may be safely assumed that the differential EMI and radiated EMI levels are much higher. In order to reduce the overshoot, the switch must be slowed down, leading to higher switching losses.

There is also the issue of the high mutual inductance between wirebonds causing the uneven current distribution, and this effect is again a reason for higher losses, and may be the cause of the reducing the reliability of wirebonds.

In order to overcome these drawbacks, a radical approach is needed. Three-dimensional packaging may be the answer.

3.Three-dimensional Packaging

Metal Post Interconnected Parallel Plate Structure

3.1 Introduction

In an attempt to reduce the length of the interconnects, tracks, and leads, another degree of freedom is added to packaging. Three-dimensional packaging allows an additional degree of freedom that lets the design engineer to reduce and optimize the track and lead length. An analogy comparing two-dimensional packaging to conventional one layer PCBs and the MPIPPS to the two layer PCB makes the point. The two layer PCB will have a more optimized layout.

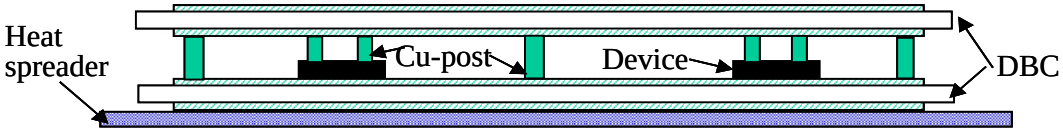

Figure 3.1. The cross sectional view of the MPIPPS module

The MPIPPS structure [7] (Fig. 3.1) is based on the use of direct bonding copper posts (dimensions: 1.1 mm, 1.1 mm, 3.5 mm), as interconnects. Since the current carrying capability of the copper posts is much higher than the wirebonds, each copper post may replace two or three wirebonds. The copper layer on the Aluminum Nitride Direct Bonded Copper (DBC) substrate is etched to give the desired pattern. In this case, the desired pattern is the circuit known as VSI. The switch and diode are attached to the bottom DBC substrate. The copper posts are then soldered onto the pads on the device, which have been made solderable. Any other devices, active or passive, such as those in the gate driver may be attached to the top DBC substrate. This DBC substrate is then attached to the posts to complete the structure.

A major thrust in this research effort is the integration of the passives and active elements associated with the gate driver and controller into the module. This makes the modules self-sufficient.

Fig. 3.2 shows the different levels of integration that this project aims at. Each succeeding phase of the project, the level of integration goes up. In the Fig. 3.2, there are three balloons, each of different color, which include the elements to be integrated in each phase of the project

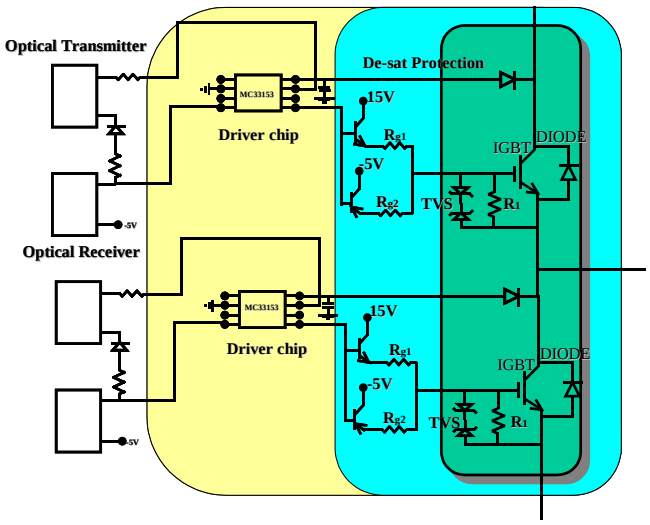

Figure 3.2. The Gate Driver and integration of the driver elements

The pattern etched on the top DBC substrate is used as the circuit for the gate driver elements that are shown in the Fig. 3.2. In the analysis of the MPIPPS module however, only the power layout has been used. Owing to the compact nature of this structure, interconnects are much shorter in length. Also, since one post replaces three or more wirebonds, the posts are further apart resulting in lower mutual inductance, which means more even current distribution.

As mentioned in the introduction, there are problems associated with three-dimensional packaging. These problems need to be addressed before it can become a viable alternative

3.2 INCA model of the MPIPPS module

The process described before, in Chapter 1 and Chapter 2, is followed in order to develop the INCA model of the MPIPPS module. The geometry and the material properties such as the resistivity are defined in INCA, and the equivalent inductance of each element is extracted. The INCA model and the equivalent inductance circuit of the MPIPPS module are shown in Fig. 3.3and Fig.3.4 [18].

In the model developed in INCA (see Appendix II), appropriate subdivision, to account for the proximity effects (the uneven distribution of current in parallel conductors) due to the mutual inductance and the skin effect, is done.

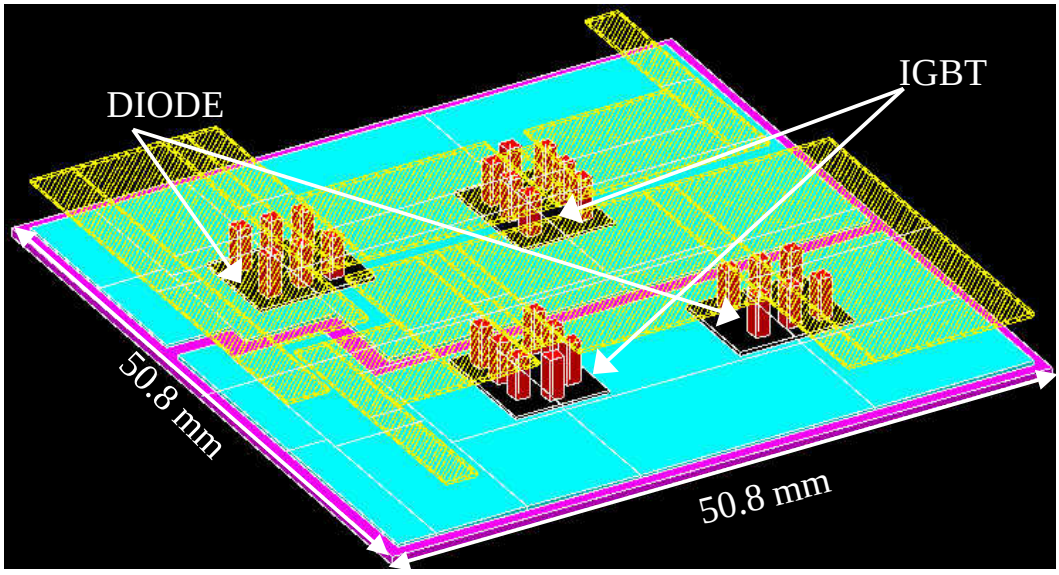

Figure 3.3. The INCA model of the MPIPPS module

This equivalent inductance circuit includes only the self-inductance of each element. In order to make the figures more lucid, the mutual inductance between the elements is ignored, and the AC resistances are not shown. These are however, included in the simulation.

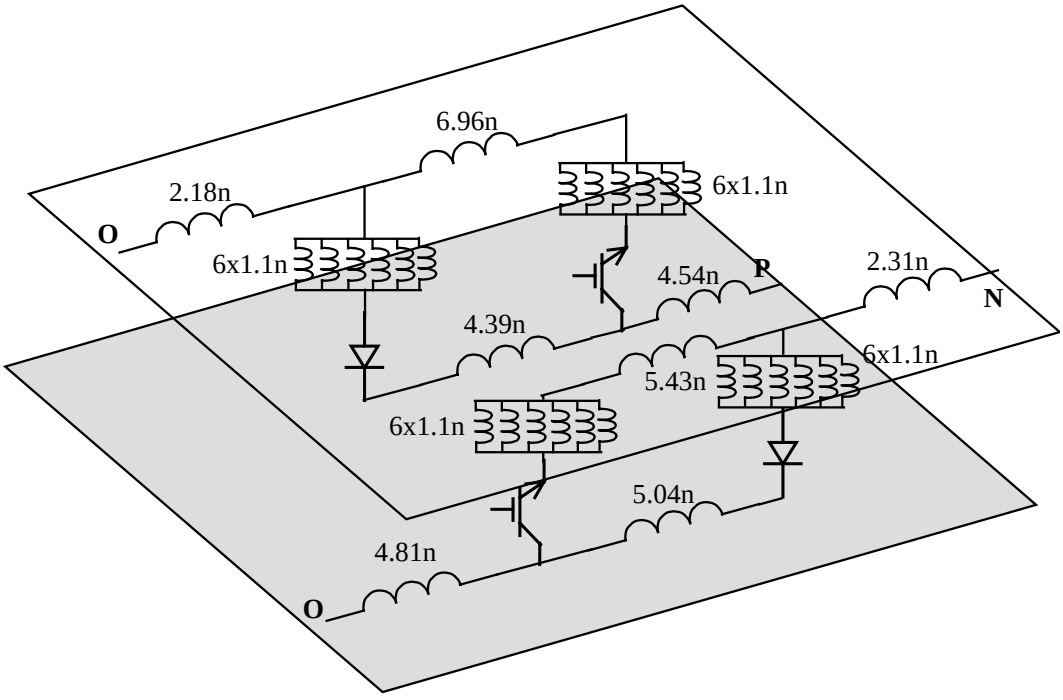

Figure 3.4. The equivalent inductance model of the MPIPPS module

3.2.1 Analysis of the MPIPPS structure

In order to get a better idea of the layout and the parasitic inductance associated with it, a closer look at the MPIPPS module and the equivalent inductance model is shown in Fig.3.5

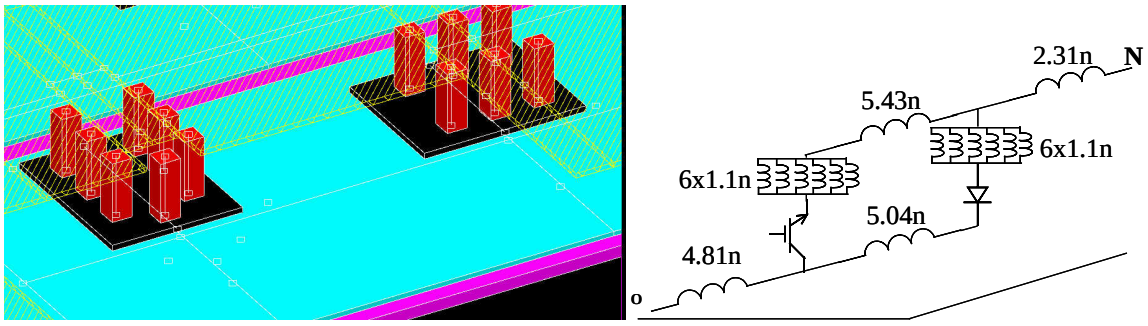

Figure 3.5 Closer look at the MPIPPS module and the equivalent circuit

Table III. The inductance values of the MPIPPS module

No.	Name of the element	Self-inductance	Comment
1.	Post for IGBT Emitter	1.1nH	Low inductance
2.	Post for diode	1.1nH	Mutual inductance between adjacent posts is 0.8nH
3.	Lead for gate	2nH	Will give good performance.
4.	Track to IGBT Collector	4.81nH	Lower overshoots
5.	Loop inductance	13nH	Lower overshoot

It can be seen that the parasitic inductance in the MPIPPS structure is low and therefore the degradation in performance is expected to be low too. Since the MPIPPS module requires that the pads be made solderable, a thin layer (100 Å) of tin followed by chromium and then a layer of copper is sputtered onto the aluminum pads. This processing of the pads of the device has posed problems. There are traces of organic materials on the pads, which reduce the adhesive strength between the metal layers and the pads. Therefore the resisistivity of the thin films increased, beyond acceptable norms rendering the devices unusable. These problems associated with processing need to be addressed before this technology can be implemented on a large scale with significant

yield. Because of these problems, modules with satisfactory performance could not be fabricated. Thus in comparing MPIPPS with the wirebond technology, only simulation is used. The validity of the models generated has already been verified in the case of the wirebond module. Therefore, the results from simulation of the MPIPPS module may be compared with the wirebond simulation.

3.2.2 Simulation of the performance of the MPIPPS module

In order to compare the packaging technologies, the MPIPPS module is also simulated in the same test circuit that the wirebond module was simulated and tested in.

3.2.2.1 Results from PSPICE simulation

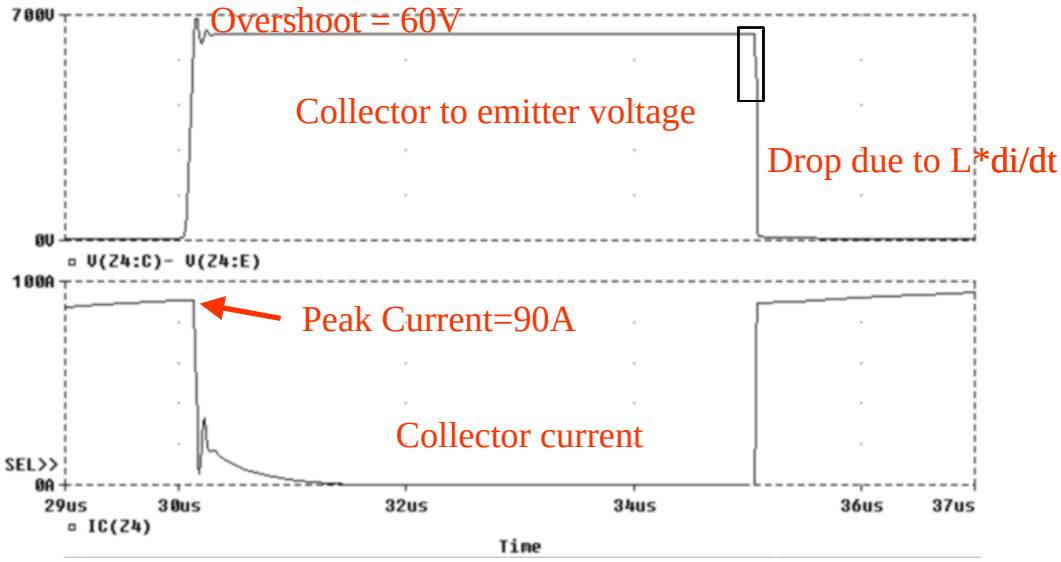

Figure 3.6. The simulation results for the MPIPPS module

The simulation of the tester described in section 2.2.2.1. The simulation results are shown in Fig. 3.6 (See Appendix III for the mpipps.cir file used in PSPICE simulation).

3.2.3 Maxwell model of the MPIPPS module

As with any design process, there is always a tradeoff involved. In this case, in order to reduce the inductance of the interconnects, the structure was made three-dimensional. In order to reduce the inductance of the tracks, the tracks were made with larger areas. All these changes increase the parasitic capacitance, because of the larger copper areas, and because the structure is now three-dimensional.

In order to model these effects, Maxwell Quick 3-D parameter extractor was used. Once again, the geometry and the materials are defined and then the parameters are extracted.

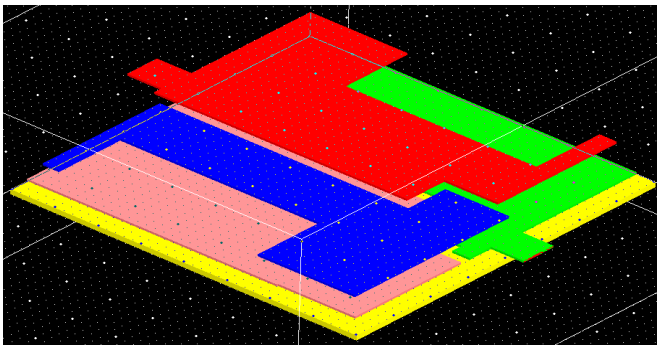

Figure 3.7. MPIPPS model in Maxwell

From the parameters extracted, it becomes obvious that the parasitic capacitance between the top and bottom substrates is very small due to the large distance that exists between substrates. Thus the output capacitance of the IGBT overshadows the parasitic capacitance. There is however, the parasitic capacitance to the chassis ground to consider. As described before, the capacitance to the ground affects the common mode EMI of the module. In this module, the gate driver has been integrated. The parasitic capacitance between the power and the gate lead will also need to be considered. This may cause adverse performance of the device.

3.2.3.1 Parasitic Capacitance of the MPIPPS module

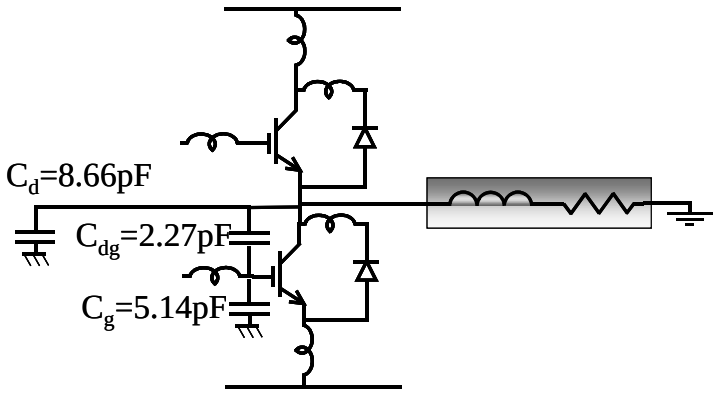

Figure3.8. The parasitic capacitance in the MPIPPS case

3.2.3.2 Comparison of the Maxwell and INCA models

Since the MPIPPS was analyzed both in INCA and Maxwell, a comparison of the models developed in both is made so that the software may be evaluated for their accuracy. The parasitic inductance and resistance extracted from Maxwell is compared to the values extracted in INCA. The comparison shows that both methods give results that are concurrent. The results in both cases closely match each other. Since the INCA model was already validated in the case of the wirebond module, and the INCA and Maxwell models are fairly similar, the Maxwell model can also be now used in further analysis. This is important because in the case of the Multi Layer Structure, the dielectric layers prevent us from modeling it in INCA. This is because INCA cannot analyze the materials used in MLS.

Table IV. The comparison of the Maxwell and INCA models of MPIPPS

No.	**Name of the element**	**Self-inductance**		**Resistance**	
		INCA	Maxwell	INCA	Maxwell
1.	Post for IGBT Emitter	1.09nH	1.1nH	0.046m	0.05m
2.	Post for diode	1.09nH	1.1nH	0.046m	0.05m
3.	Gate track	1.9nH	2nH.	0.052m	0.055m
4.	Track to Collector	4.7nH	4.81nH	0.066m	0.068m

3.2.3.3 Current distribution in the MPIPPS module

The lower mutual inductance in the copper posts means the current distribution is more uniform in the case of the MPIPPS module. In order to verify this, the model for the copper post interconnects is developed in Maxwell 3-D field simulator.

Our conjecture is verified in Fig. 3.9. The current is distributed more uniformly between all the three posts. The reason for this has already been explained. In order to study the exact current distribution, the current distribution along a line running through the posts was taken

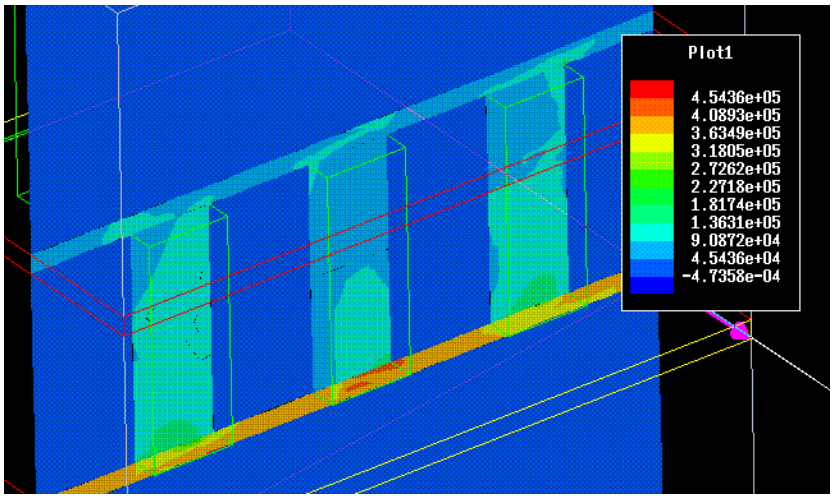

Figure 3.9. The current distribution in the posts

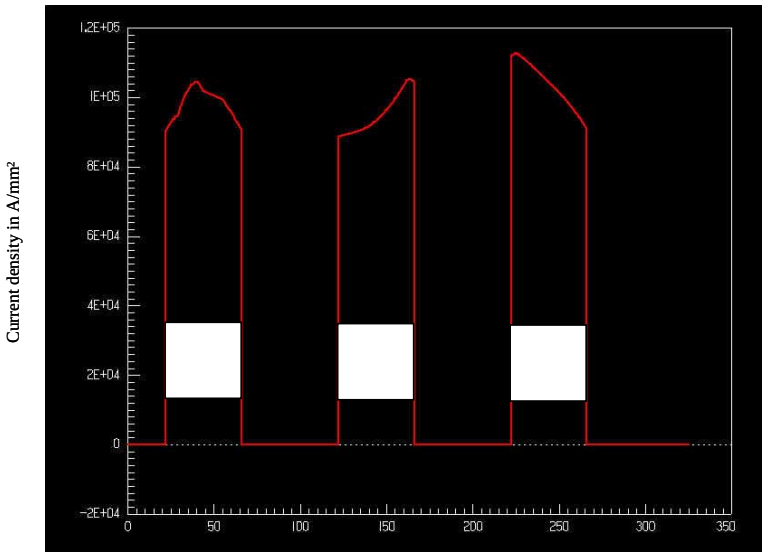

Figure 3.10. The current distribution along a straight line through the posts

More uniform current distribution means lower losses in the conductors. Also since the current distribution is uniform there is no unnecessary stressing of the interconnects since no one interconnect bears the entire burden. It is a well-known fact that lots of failures occur due to the failure of the packaging mechanism. The failures are due the current constriction and local heating.

It must be remembered that the since the copper posts have larger surface area, the skin effect (which is the crowding of the current to the periphery of the conductor) causes losses in the conductor.

3.3 Conclusions

In this chapter we have shown the performance of the Three-Dimensional packaging. This is however, only a part of the picture. When evaluating a packaging technology, many other factors need to be accounted for. These include the thermal capability of the module, the thermal spreading ability of the technology, the mechanical strength of the interfaces, the interfacial resistance, and reliability. Only after a thorough study in all these areas can we draw a conclusion about whether a certain packaging technology is worth pursuing or not.

4. Multi Layer Integration Technology

A Novel Three Dimensional technology

4.1 Introduction and advantages

In order to realize the integration that the future of power electronics demands, three-dimensional packaging technology is required. Many such packaging technologies have been developed [11]-[12]. Various high-density interconnection approaches have been taken. However, the technology needed to build reliable, compact and compatible 3-D power electronic modules has not been established.

Figure 4.1 shows the cross-section of the Multi Layer Structure (MLS). This is also referred to as the Multi Layer Integration Technology (MLIT).

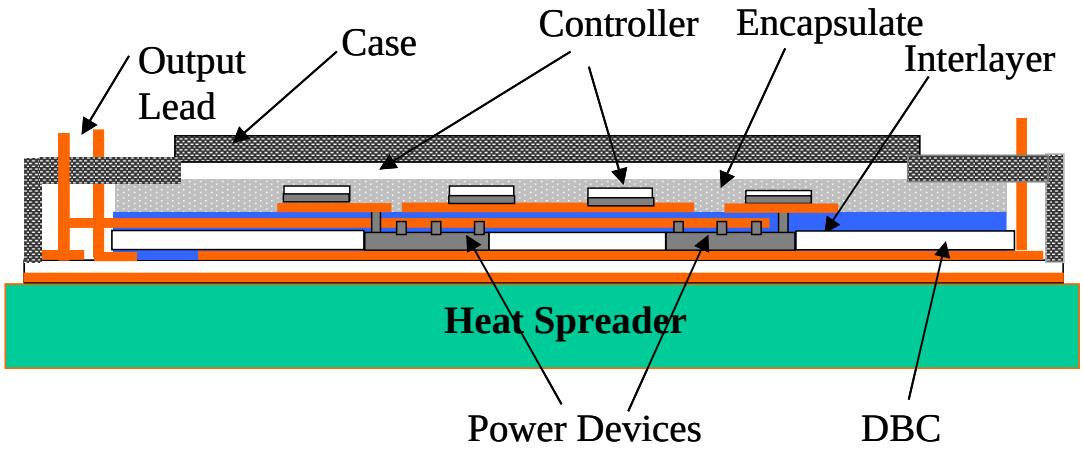

Figure 4.1 The Cross Section of the Multi Layer Structure

This structure can be divided into four layers, an aluminum nitride DBC substrate, a layer containing power devices and tracks, a dielectric layer, a conductive layer with tracks for signal and drive/control in that order from bottom to top. Most power devices are built in a vertical fashion. This means that two metal layers can complete their connections with any other part of the circuit. Once again, the AlN DBC substrate is employed as the base substrate. The power devices are directly soldered onto the substrate. To get a flat, embedded power layer, a machined Alumina plate with openings is bonded onto the other areas of the substrate to fill up the space between the chips. A

dielectric layer is then coated onto the power layer, and vias for the pads of the device are opened [8].

Since this technology makes use of a wide variety of materials, the materials and the layers used in the development of this technology have to be well matched in order to reduce the stress on the module, and thereby increase the reliability of the module. The most important concern in matching materials from a stress perspective is to reduce the Coefficient of Thermal Expansion (CTE) mismatch. The feasibility, and the process compatibility of the materials are also important. The fabrication order depends on the process property of the material. Once the surface metallization is done, the surface mount devices can be readily attached to the top surface.

It must be mentioned however, that this technology too would require that the semiconductor dice be topside solderable in order to attach the interconnects through vias. As mentioned before, this effort has met an obstacle in the form of poor adhesion, which is being addressed.

4.2 Maxwell model of the Multi Layer Structure

In order to extract the parasitic elements in this module, INCA was not used. The major drawback INCA faces (owing to the fact that INCA uses PEEC method to calculate the inductance based on the geometry) is that it cannot account for materials within the geometry, other than vacuum. Since this Multi Layer Structure uses layers of dielectric, adhesive and the ceramic substrate, Maxwell was chosen to extract the parasitics elements within the module. As we have shown before, through an example comparison between INCA and Maxwell, the parameters extracted by both tools are close enough to facilitate the comparison of the Multi Layer Structure to the wirebond technology.

The model was therefore developed in Maxwell. In order to do this, the geometry of the module has to be carefully defined. Then the material associated with each element needs to be described. Each material is described with its permitivity in case of dielectrics, and the permeability in the case of magnetic materials. Then the solver parameters are set and Maxwell is able to extract the parameters requested for.

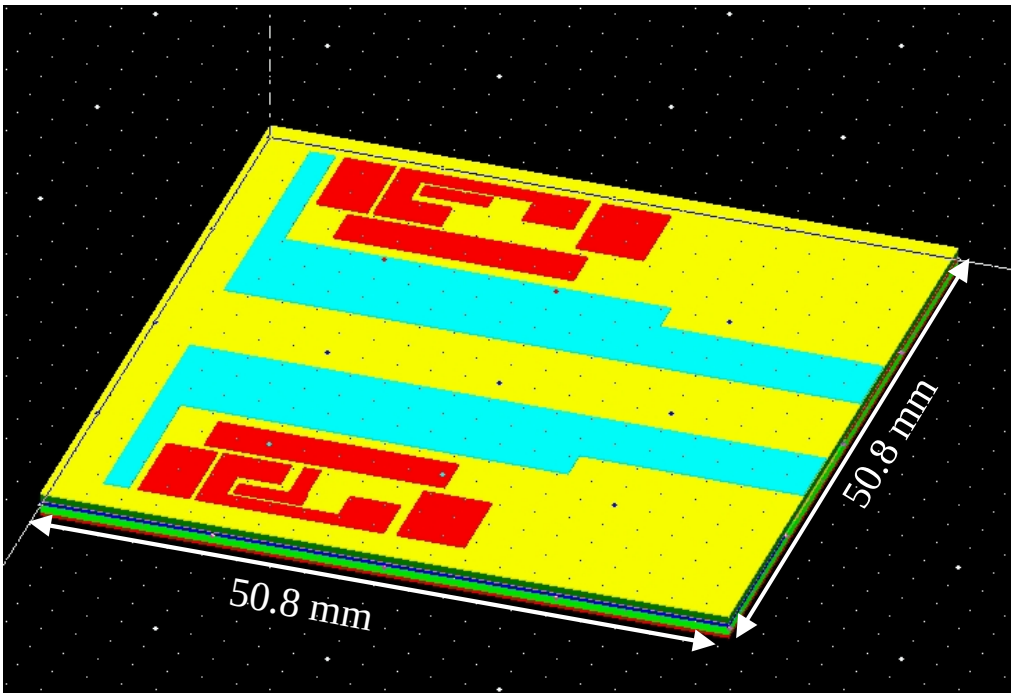

Figure 4.2. The MLS module in Maxwell Q3D extractor

In Fig. 4.2, the top metallization on the dielectric chosen can be seen. This is the gate drive circuitry. Surface mount devices are used on this pattern to build the gate driver.

The layout in this case is very similar to the MPIPPS module. Because of this reason, the self-inductance in this case is very close to the self-inductance of the MPIPPS module. However, because of the proximity of the conductors, the mutual inductance in this case much higher than the mutual inductance in the case of the MPIPPS module.

The cross-section of this Multi Layer Structure is shown below. Because the conductor and the dielectric layers alternate, the parasitic capacitance will play a major role in the performance of the module. The parasitic capacitance is also extracted and included in the model. As discussed before, the parasitic capacitance to the chassis ground will determine the common mode EMI levels.

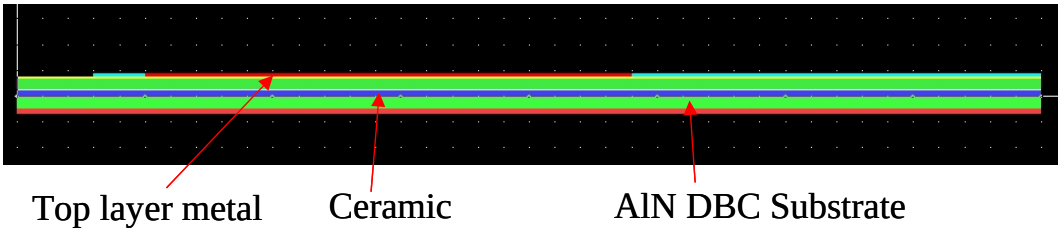

Figure 4.3. The cross-section of the Multi Layer Structure

4.2.1 Parasitic elements in the MLS

The parasitic inductance and capacitance, after being extracted, are sorted and then matched to the corresponding element in the geometry. The Fig. 4.4 shows the parasitic self-inductance of the elements in the module. Since showing the mutual inductance of the elements and the parasitic capacitance only reduces the lucidity of the figure, they have been omitted.

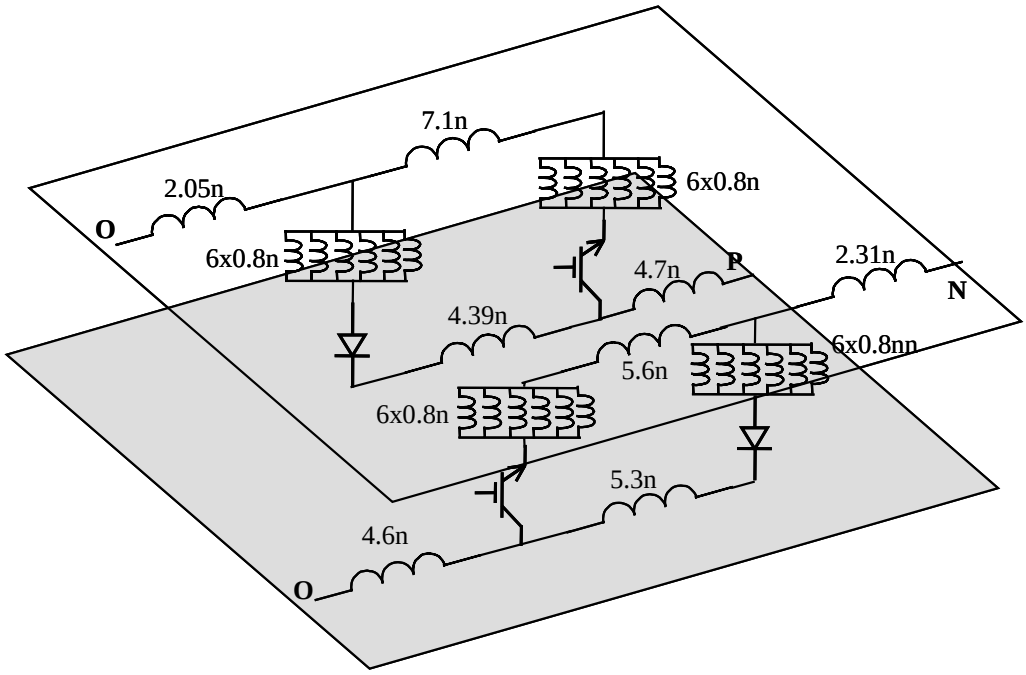

Figure 4.4. The equivalent inductance model of the Multi Layer Structure

As will be shown later in Chapter 6, the proximity of the layers causes higher mutual inductance between the layers than in the case of the MPIPPS module. The effects of this proximity are studied in Chapter 6.

The mutual inductance between the interconnects is very small. The effect of the larger mutual inductance between tracks can be seen in the simulation results.

4.2.1.1 Simulation of the performance of the MLS

The equivalent electrical model of the MLS was used in the test circuit in order to evaluate the performance of the packaging technology.

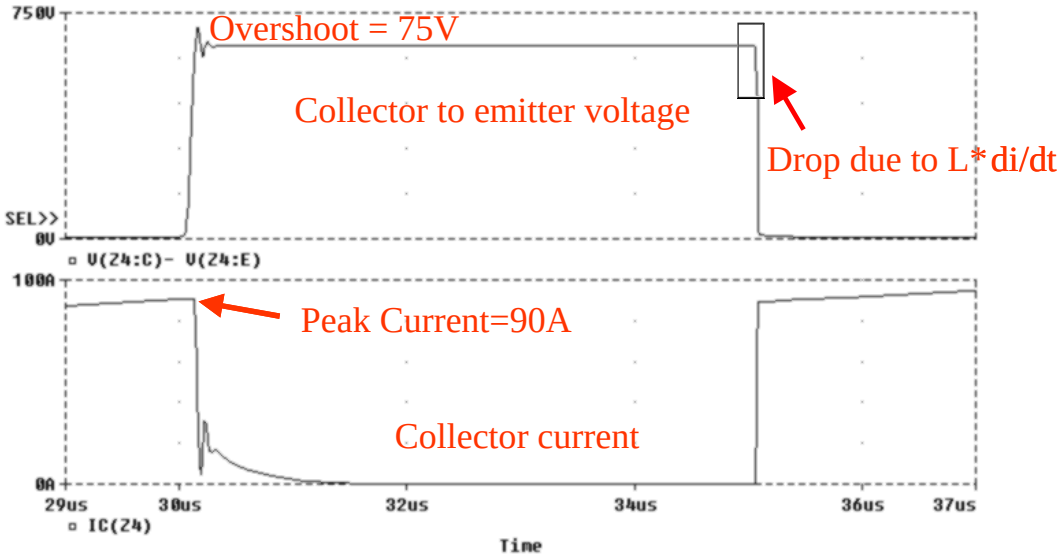

Figure 4.5. The simulation results for the MLS model

The simulation of the tester described in section 2.2.2.1. The simulation results are given in Fig. 4.5.

4.2.2 Examination of the parasitic capacitance of the MLS

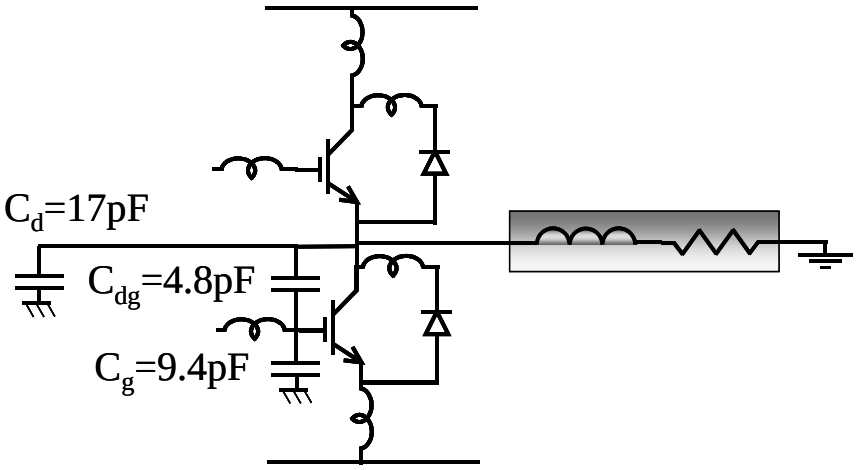

Figure 4.6. The parasitic capacitance model of the MLS nodule

Since Maxwell enables us to characterize the parasitic capacitance, the parasitic capacitance model is also drawn. It can be seen from the Fig. 4.6 that the capacitance to the ground is very high in this case. This would be very detrimental with respect to the EMI standards.

4.3 Conclusions

In this chapter, the Multi Layer Structure was presented. The equivalent electrical model of the Multi Layer Structure was developed using Maxwell Q3D parameter extractor. The model thus developed was then evaluated on the performance indices that were defined.

5. Comparison of the Packaging Technologies

5.1 Comparison of the parasitic inductance from the INCA model

In this section the results that the analyses have presented in the earlier sections will be compared and discussed. Table V presents the results from the INCA and Maxwell models, in terms of the parasitic inductance in the layout.

Table V. The comparison of wirebond, MPIPPS, and MLS module

No.	Name of the element	Self-inductance of wirebond	Self-inductance MPIPPS module	Self-inductance MLS module
1.	Interconnect for IGBT Emitter	8.63nH	1.1nH	0.8nH
2.	Interconnect for diode	6.88nH	1.1nH	0.8nH
3.	Lead for gate lead	17nH	2nH.	2nH
4.	Track to IGBT Collector	14nH	4.81nH	4.6nH
5.	Loop inductance	28nH	13nH	12nH

The most noticeable difference between the wirebond module and the MPIPPS module is that the MPIPPS module has lower parasitic inductance in the layout. The tracks and the leads in the MPIPPS module have lower inductance than their counterparts in the wirebond module. The parasitic inductance of the copper post is lower than that of the wirebond.

The self-inductance of the posts is much reduced because of the much larger cross-sectional area of the posts. They are also much shorter in length compared to the wirebond. The tracks are much wider and shorter in length, resulting in lower self-inductance. Because the posts are larger and can replace two or three wirebonds, they have larger distance between them. The larger distance means lower mutual inductance between posts.

This lower self-inductance and the lower mutual inductance are reflected in the better performance in terms of overshoot and also the more uniform current distribution. This is the case for the Multi-Layer Structure too.

This is because of the three dimensional nature of the layout where interconnects are much shorter. It is similar to the usage of a two layer PCB. The design is definitely more optimized in the case of the two-layer board. There is no necessity to have large tracks, leads or interconnects. The three-dimensional structure also means that the external laminated bus can be seamlessly integrated into the MPIPPS module. This would be a dramatic improvement, because of the absence of the long leads that are ubiquitous in a wirebond module. The self-inductance of the elements in the case of the MLS is very similar to that of the MPIPPS. In fact, the inductance of each element turns out to be very close to its counterpart in the MPIPPS case.

The mutual inductance however is higher in the case of the MLS than the MPIPPS module, since the tracks are closer. This is reflected in the performance of the MLS module. The Table V shows the better layout design of the MPIPPS module. The better layout design of the MPIPPS and the MLS modules will show up as better electrical performance when compared to the performance of the wirebond module.

5.2 Comparison of the performance of the technologies

The performance of all the packaging technologies and the layouts, in the simulation of the tester developed, was seen in the earlier chapters. The Table VI summarizes these results.

Table VI Simulation results for wirebond, MPIPPS and MLS

Performance Index	**WIREBOND**	**MPIPPS**	**MLS**
Voltage Overshoot	120V	60V	75V
Rise time	0.6µsec	0.4µsec	0.4µsec
Fall Time	1µsec	0.8µsec	1µsec
Settling Time	0.5µsec	0.2µsec	~0.3µsec

The MPIPPS module has the lowest overshoot. Although the MLS has lower self-inductance, as compared to the MPIPPS structure, the high mutual inductance (because of the proximity of the tracks) is detrimental to the performance of the module. Therefore, for a similar gate signal, the MLS has a higher overshoot than the MPIPPS module. Both the MPIPPS and the MLS have lower settling times, as compared to the wirebond, because of the lower inductance. This means that for the same switching frequency and speed the MPIPPS module would have lower switching losses than the wirebond module. This would augur well for miniaturization of the module.

The next chapter will present ideas that can be used in order to minimize this inductance in a three-dimensional structure so as to improve the performance of the modules.

5.3 Comparison of the parasitic capacitance from Maxwell models

As with any design process, in an effort to reduce the parasitic capacitance of the layout we increased the surface area of metal and reduced the gap between layers. This would increase the parasitic capacitance of the layout. A comparison of the parasitic capacitance of the layouts is presented in Table VII.

Table VII. The comparison of parasitic capacitance in the layout

Parasitic Capacitance	**WIREBOND**	**MPIPPS**	**MLS**
Collector to ground	5.8pF	8.86pF	17pF
Gate to Ground	Negligible	5.14pF	9.4pF
Collector to Gate	Negligible	2.27pF	4.8pF

It can be seen that the parasitic capacitance of the MPIPPS module is higher than the wirebond module. This is to be expected, as explained before, because of the larger copper areas and the three-dimensional nature of the packaging. The capacitance to the ground from the collector of the IGBT to the chassis ground is 8.66pF. This is almost double the capacitance to the ground in the case of the wirebond module. This is corroborated by the fact that the area of copper in case of the MPIPPS is almost double that in the case of the wirebond module. The MLS has a much higher parasitic

capacitance than the MPIPPS module. This is because the dielectric, which has a relative permitivity larger than unity, increases the parasitic capacitance. The larger area in the case of the MLS also contributes to the higher parasitic capacitance. It can also be noticed that there is a parasitic capacitance from the gate lead to the ground and between the collector and the gate lead in the case of the MLS and the MPIPPS module. This does not exist in the case of the wirebond module because the gate lead in the case of the wirebond module is a single wirebond, which does not have high parasitic capacitance.

By themselves the numbers do not signify much. The capacitance from the midpoint to the ground (if the module is attached to a heatsink) usually is the cause of common-mode EMI. A higher parasitic capacitance would usually indicate a higher level of common-mode EMI. This means that for the same slew rate of the voltages, the conducted EMI levels would be much higher. However, it must be pointed out that since the differential mode EMI and radiated EMI actually depend on the parasitic inductance as well. A more comprehensive study will be needed before any conclusion can be drawn about the EMI performance of the models.

Moreover, some capacitances, such as between the positive and negative rails of the DC buses are actually beneficial. It is a challenge for the layout designer to try to maximize the beneficial parasitic effects, while minimizing the detrimental ones.

5.4 Conclusions

We have in this chapter compared the different packaging technologies along the indices that were picked in the beginning of the thesis. The MPIPPS and the MLS have a significantly better electrical performance, compared to the wirebond structure. This better performance is expected because of the larger parasitic elements that exist in the layout and interconnects in the wirebond module. The three-dimensional packaging has also been shown to have a more uniform current distribution in the interconnects. There is a disadvantage however, in using three-dimensional packaging and that is the larger parasitic capacitance that the three-dimensional packaging layout has. This may prove to be detrimental in terms of conducted EMI. A more in depth analysis of how the three-dimensional packaging is better than the two-dimensional packaging is reserved for the next chapter.

6. Conclusions and Design Ideas

6.1. Packaging technologies – merits and demerits

We have now discussed, as a broad generalization, the demerits of the two-dimensional packaging, and the advantages of three-dimensional packaging. As an example of two-dimensional packaging, we analyzed a commercially available wirebond module (the MII75-12A3) manufactured by IXYS. The parasitic inductance and the parasitic capacitance of this module were extracted and then the models thus developed were verified by comparing the performance indices in the experimental case with the simulation results. After validating the model, and therefore the modeling process, the three-dimensional packaging technology was suggested as a possible means of overcoming the problems that the wirebond module posed.

In this effort, two new packaging technologies namely the Metal Post Interconnected Parallel Plate Structure, and the Multi Layer Structure were introduced. For each of these technologies, the same evaluation methodologies were applied and the performance indices of each packaging technology were compared. The MPIPPS and the MLS have better electrical performance thus making the case for three-dimensional packaging. This was attributed to the lower parasitic inductance of the interconnects, tracks, and leads. The three dimensional packaging was shown on the whole to perform better than the two-dimensional packaging. In this chapter we look at some design ideas for three-dimensional packaging. The effect of varying certain parameters on the parasitics in the module is studied.

6.2 Design ideas for Three-Dimensional Packaging

Through the length of this thesis, it has been well established that the MPIPPS and the MLS module have a better electrical performance than the wirebond module. This definitely establishes three-dimensional packaging, as the choice for the evolutionary pattern that packaging should take. But what actually makes the three-dimensional packaging better than the conventional two-dimensional wirebond packaging? It is the shorter interconnects? Is it due to the shorter tracks? Is it due to the usage of the

laminated bus (negative mutual inductance)? These questions need to be answered very clearly before any conclusions can be made.

On examining the equivalent inductance models of the MPIPPS and the wirebond module, it becomes obvious that the track inductance in the case of the wirebond module is much higher than the track inductance in the case of the MPIIPPS. The interconnects have much higher inductance too, but since the wirebonds are eight in parallel, their effect becomes insignificant. Therefore it is suspected that the major degradation in the performance of the module occurs due to the parasitic elements in the tracks and leads, rather than the interconnects themselves.

In order to verify this intuition, a simple simulation was performed. The wirebond module and the MPIPPS module were simulated in the test circuit, used for evaluating the packaging technologies, with only the inductance of the interconnects (i.e. the inductance of the wirebonds and copper posts only) affecting the performance of the module. These simulation results and the performance indices in these cases are compared.

When these simulation results are compared, it becomes clear as to what influences the performance of the module.

6.2.1 Generic comparison of two and three-dimensional interconnects

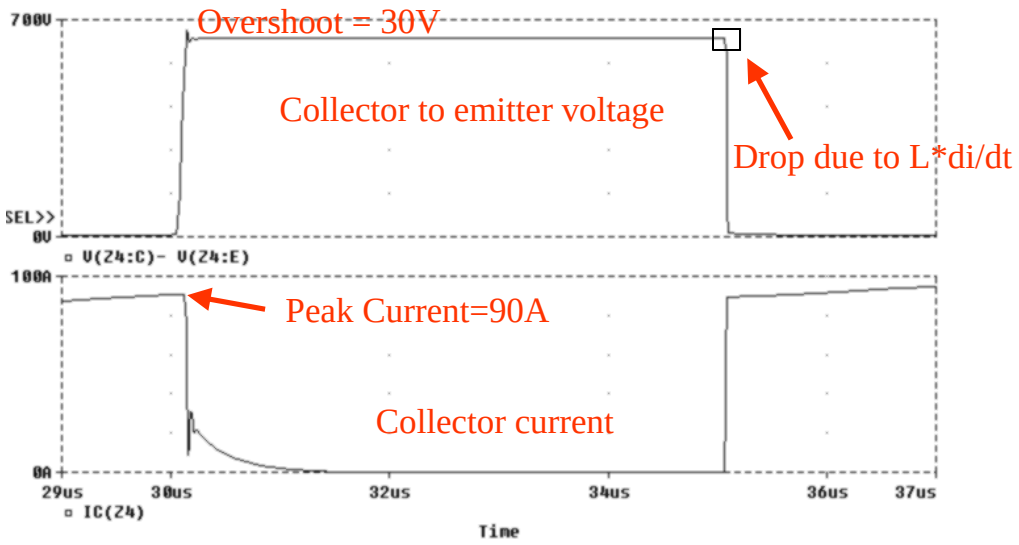

Figure 6.1. The simulation results for the wirebond module without track and lead inductance

The wirebond module was simulated with only the interconnects (in this case the wirebonds) affecting the performance of the module. They were simulated in the same test circuit that was used in testing the wirebond module and in the simulation of the MPIPPS and the MLS modules. The simulation results for the wirebond case are shown in Fig. 6.1, and the simulation results in the case of the MPIPPS module are shown in Fig. 6.2.

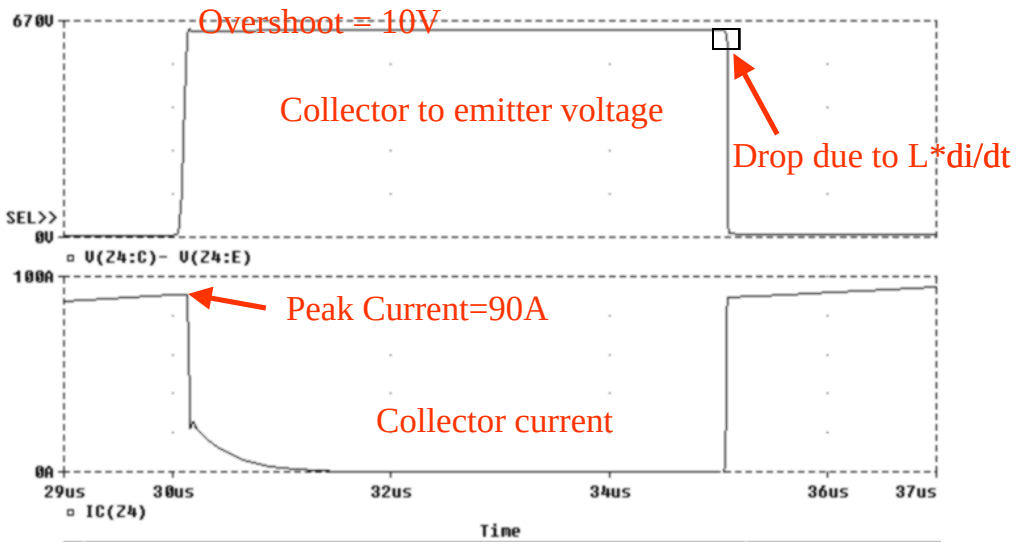

Figure 6.2.The simulation results for the MPIPPS module without tracks and leads

It can be seen that the voltage overshoot in the case of the wirebond module is very low, compared to the overshoot in the case of the wirebond module with the leads and the tracks. It is also much lower than the overshoot in the case of the MPIPPS module with the inductance of the tracks and leads included. The MPIPPS module was then simulated in the same test circuit, this time without the inductance of the tracks and leads. The results are shown Fig. 6.2. By looking at the two simulation results, it can be observed that there is almost zero or no degradation in the performance of the module due to the inductance of the interconnects. Since the voltage overshoot is on the order of 10V on a 630V bus, it is almost negligible. The settling time is non-existent.

Comparison of the two simulations shows that the MPIPPS structure is better than the wirebond structure. There is over 200% more degradation in the wirebond module, with only the inductance of the wirebonds being considered. But this is only 25% of the total degradation in the performance of the entire module when the inductance of the

tracks and the leads is considered. And therefore, we may conclude that the degradation in the voltage overshoot is primarily caused by inductance of the layout and only a small part of it is caused by the inductance of interconnects (copper posts and wirebonds). There are other effects such as the proximity effects, which are still predominant in the case of the wirebond and these may affect the reliability of the module. These conclusions apply to the modules analyzed. The conclusions may be extended to the generic class of two-dimensional and three-dimensional packaging with caution.

At this point a comparison between the results obtained in this thesis and the results in the previous literature, obtained through both the mathematical tools and the measurement techniques [6] [17] is made. Both the papers refer to the analysis on different layout and structure. The results in this thesis correlate very closely to the measurement results that are obtained in [17]. The parasitic inductance of the wirebonds is very close to the analysis performed in [6]; the inductance of the tracks is higher in the thesis than the in [6]. Even in the analysis that was performed, in the paper [6], the degradation is mostly caused by to the track and lead inductance, which is on the order of 10nH, as opposed to the total self-inductance of the wirebonds (12 wirebonds, each of 10nH). The total inductance in the path from the positive bus to the output of the midpoint (which is what influences the overshoot in the simulation) corresponds very closely to the results obtained through the measurement (in the same range).

Therefore in the modules analyzed, the improvement in performance (in terms of lower overshoot) for the MPIPPS and the MLS is not mainly due to the posts or interconnects vias, but due to better track and lead layout design. However, it must be remembered that the better track layout and design is enabled by the three-dimensional nature of the package, and the interconnects help in creating the three-dimensional layout. The interconnects do cause the improvement in performance – though not directly.

6.2.2 Further inductance reduction in three-dimensional packaging

We have already seen how three-dimensional packaging reduces the track length and therefore reduces the parasitic inductance. However, in order to derive maximum benefit from a three-dimensional package, the concept of the internal laminated bus structure could be used.

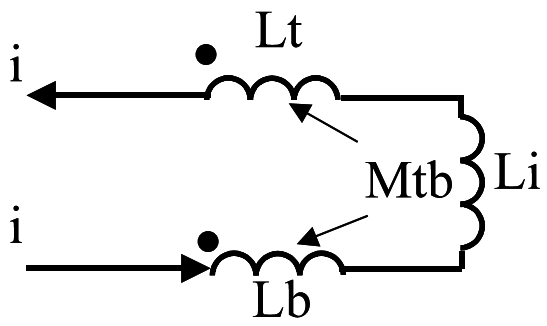

Figure 6.3. The circuit of a laminated bus

The equivalent inductance (Fig. 6.3) of the bus that the current sees would be given by equation. 6.1.

$$L_{eq} = Lt + Lb + Lp + 2Mtb \tag{6.1}$$

In 6.1,Lt is the self-inductance of the top conductor, Lb the self inductance of the bottom conductor and the Mtb the mutual inductance between the two conductors. If the mutual inductance is negative, which means that the current flows in opposite directions in the two conductors, the equivalent inductance of the structure is lower than the sum of their self-inductance. This effect may be used to great effect in three-dimensional packaging. This is especially true in the case of the Multi Layer Structure wherein the distances are so small that mutual inductance will play a significant role.

The designs in this thesis however, do not really use this concept. The current does not flow in opposite directions in the positive and negative DC buses at the same time. Instead, if the modules were built with the positive and the midpoint of the half-bridge, and the negative and the midpoint of the half bridge were to be made as a laminated bus, we may further reduce the inductance.

As an example if we consider the MPIPPS structure, as the Fig 6.4 below will show, the concept of the internal laminated bus is never utilized.

The advantages that can be derived by using the three-dimensional technology are reduced if this effect is not utilized. In order to provide some measure of the advantage of using the laminated bus structure, a simple study was performed on a single IGBT.

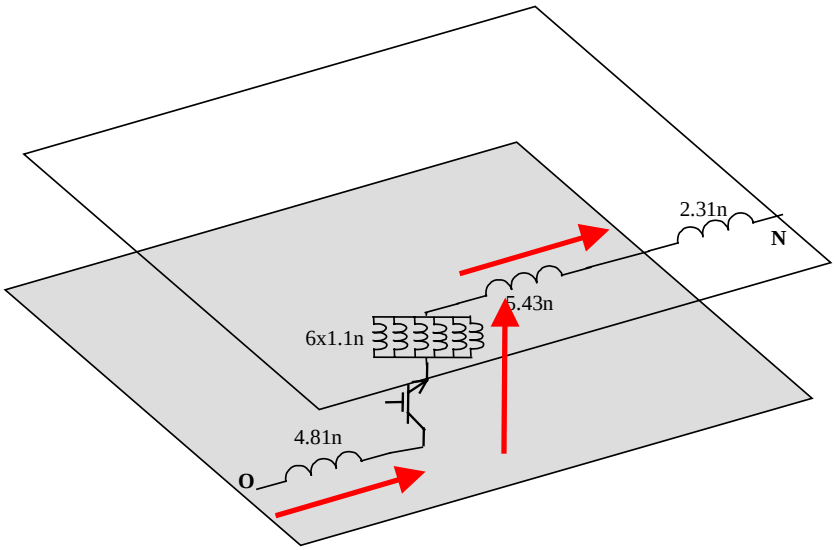

Figure 6.4. The laminated bus structure is never used

A single IGBT with copper posts is chosen. The top and bottom substrates are built in such a way that they carry the same current but in opposite directions at the same time as would happen in a real laminated bus. By varying the size of the post, the inductance of the laminated bus is varied. Varying the length of the post changes the mutual inductance between the top and the bottom substrates.

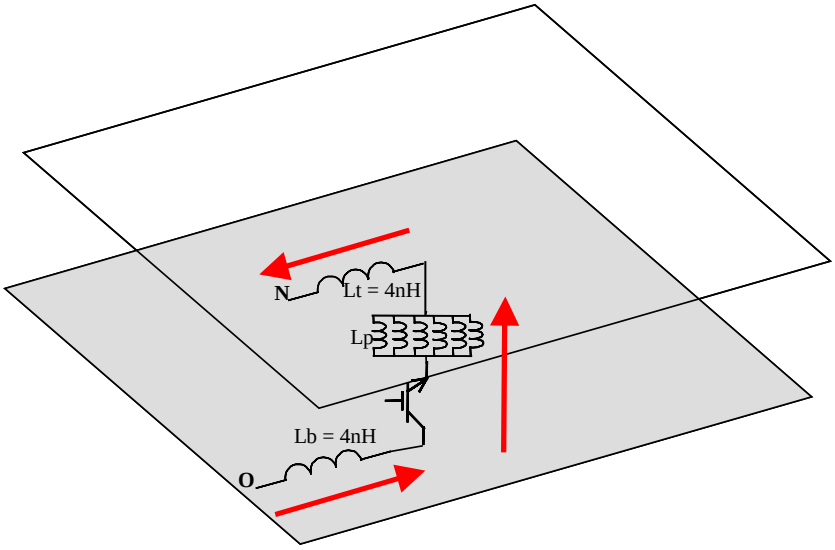

Figure 6.5. The usage of a laminated bus structure reduces equivalent inductance

Since their self-inductance remains the same, the equivalent inductance given by Eqn. (6.1) reduces in the case of a laminated bus. On the other hand, if the structure is built as in Fig.6.4, then the equivalent inductance actually increases.

The analysis of this problem is presented in Fig. 6.6.Since this shows the gain that can be achieved by reducing the post size; this graph may give a design idea about the appropriate size of the post to be chosen.

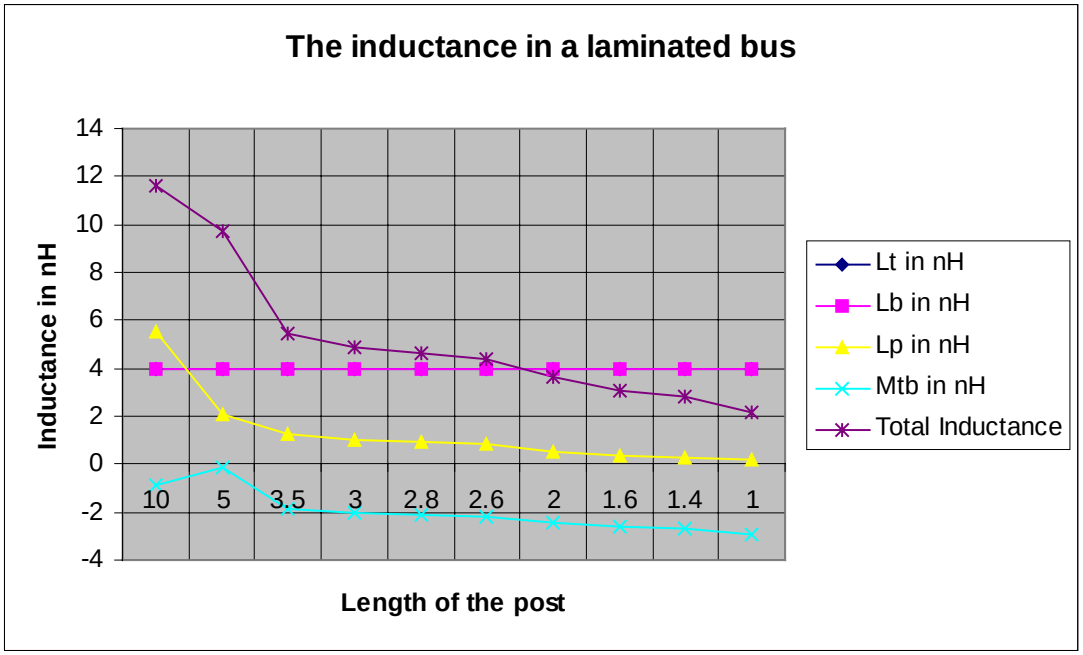

Figure 6.6. The equivalent inductance varies with post size

It must be remembered that by reducing the post size the unwanted inductance may increase. Also as the layers are brought together, the capacitance to the ground increases and as indicated before, this will affect the EMI levels. In the Fig. 6.6, Lt refers to the inductance of the top bus, Lb to the inductance of the bottom bus, Lp the inductance of the post, and Mtb the mutual inductance, as shown in Fig. 6.5.

Apart from varying the length of the post, the cross-section of the post itself may be varied. A study showing how the inductance of the post is affected by increasing the area of the post is given below.

The self-inductance of the post as expected falls with the increase in the area of the cross-section of the post. By using this curve in Fig. 6.7 and the curve in Fig. 6.6, the packaging engineer may find optimum post dimensions in order to fabricate the three-dimensional MPIPPS structure.

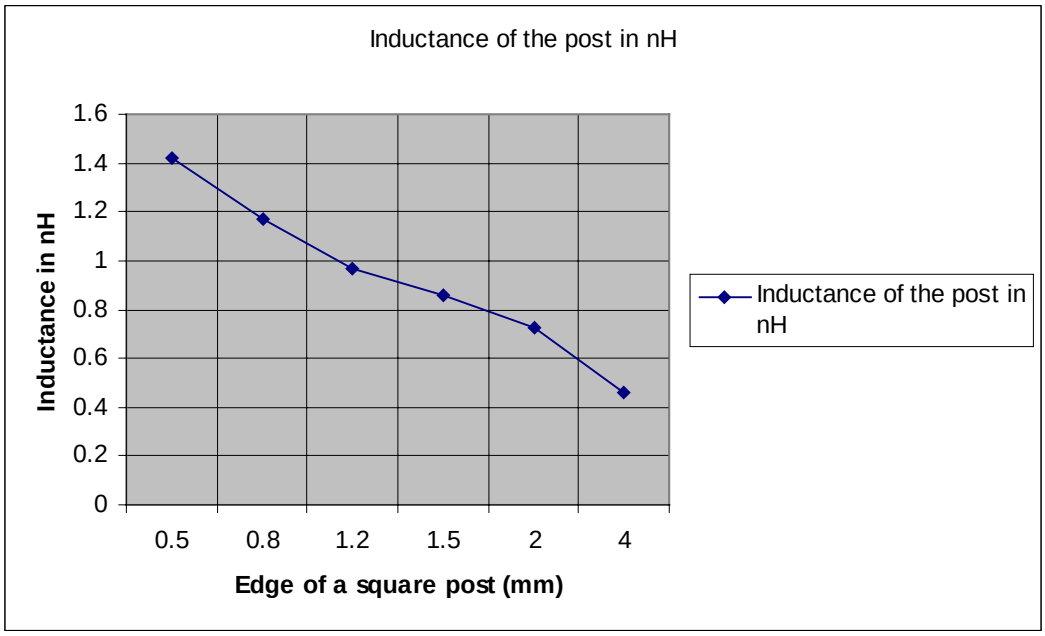

Figure 6.7. The effect of varying the cross-section area of the post

6.3 Issues that need to be addressed in Packaging

Power Electronics is a rapidly growing field. The devices are getting faster, More topologies are being developed and the applications and usage of power electronics has increased manifold over the last twenty years. The packaging of the power semiconductors however, has not kept pace with the industry. Power Packaging still lags far behind the IC industry in terms of performance, optimization, and miniaturization. The issues that need addressed in power packaging are more challenging than the IC industry, especially the thermal aspects.

However, now more than ever the onus is on packaging to come up with novel and unique solutions to solve the many problems that the packaging engineers face in power packaging. In this thesis, two such technologies were presented and they were analyzed from an electrical performance point of view. Although a technology maybe very promising from an electrical point of view, it may not be suitable from thermal, reliability, processing point of view. In order to complete the study on any packaging technology, it must be characterized from all these points of view. There is however the fact that processes may improve or better materials maybe synthesized, that would enable something that is not possible with the present technology.

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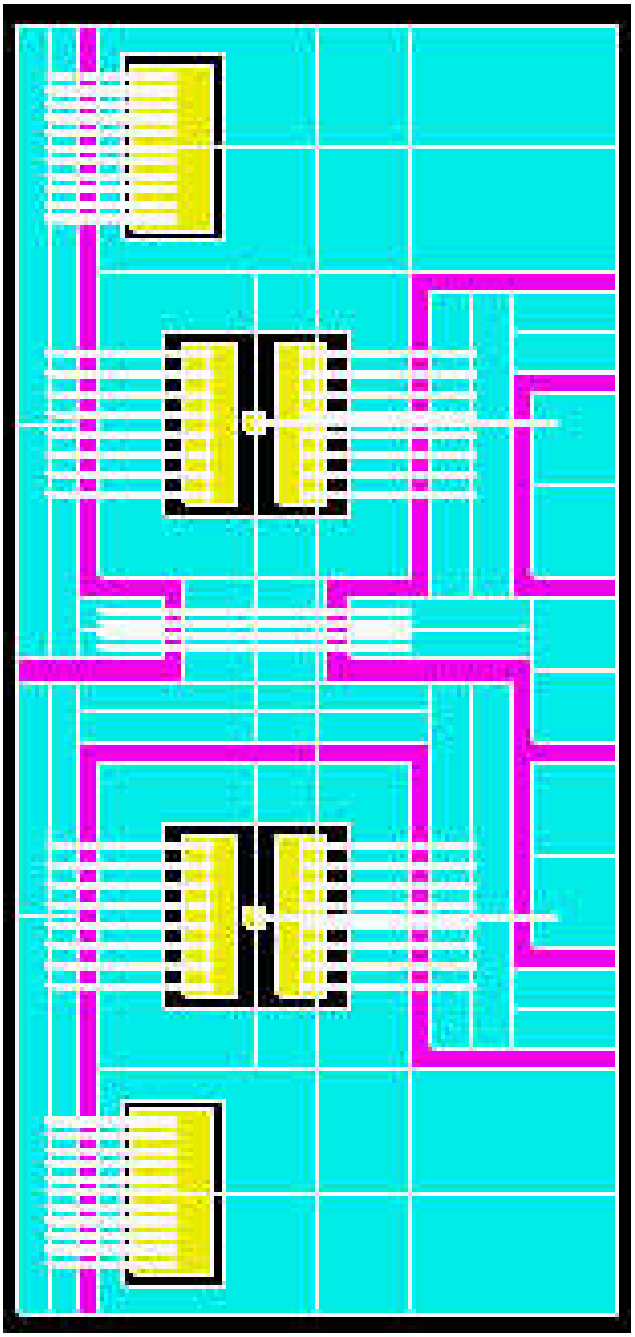
APPENDIX I – WIREBOND MODEL IN INCA

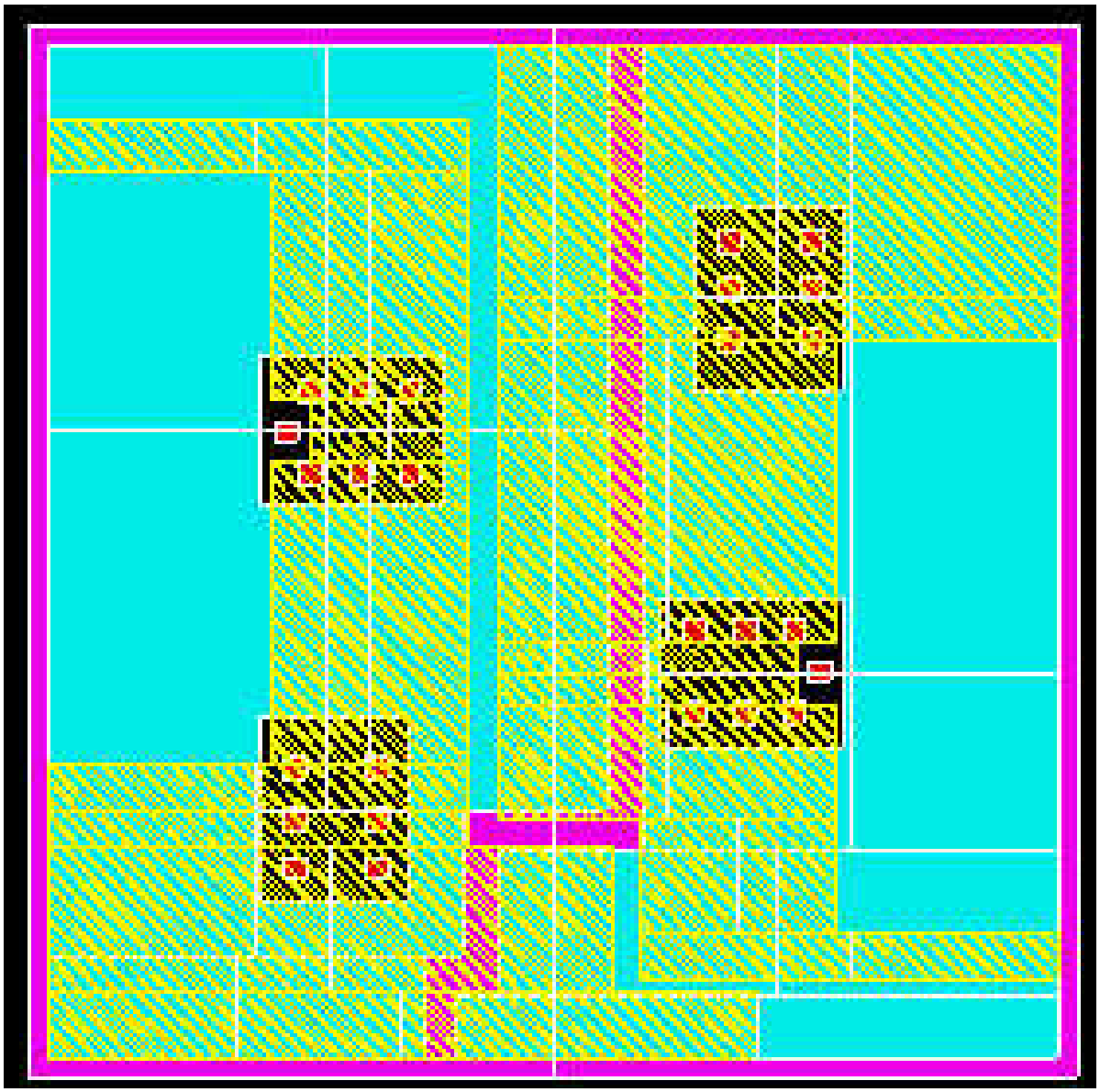


Scale 1 mm on paper = 0.37 mm real size

Frequency at which parameters were extracted: 20 KHz

Top view of the INCA model of the MII 75-12A3 manufactured by IXYS

APPENDIX II – MPIPPS MODEL IN INCA



Scale 1 mm on paper = 0.33 mm real size

Frequency at which parameters were extracted: 20 KHz

Top view of the INCA model of the MPIPPS module designed at Center for Power Electronics Research

APPENDIX III- MPIPPS.CIR FILE

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* Schematics Version 8.0 - July 1997
* Thu Nov 18 14:37:03 1999

.LIB MAGNETIC.LIB
.LIB DIODE.LIB
.LIB PWRMOS.LIB
.LIB THYRISTR.LIB
.PROBE
.TRAN  .20ns 45u UIC

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KLOOPP3-LOOPP6 LPLOOPP3 LPLOOPP6 .536E+00
KLOOPP3-LOOPTE LPLOOPP3 LPLOOPTE .137E+00
KLOOPP3-LOOPO1 LPLOOPP3 LPLOOPO1 .134E+00
KLOOPP3-LOOPO2 LPLOOPP3 LPLOOPO2 .922E-01
KLOOPP3-LOOPO3 LPLOOPP3 LPLOOPO3 .884E-01
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LPLOOPP4 P82 P82P89 .866E-09
RPLOOPP4 P82P89 P89 .232E-04
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KLOOPP4-LOOPP6 LPLOOPP4 LPLOOPP6 .283E+00
KLOOPP4-LOOPTE LPLOOPP4 LPLOOPTE .462E+00
KLOOPP4-LOOPO1 LPLOOPP4 LPLOOPO1 .301E+00
KLOOPP4-LOOPO2 LPLOOPP4 LPLOOPO2 .144E+00
KLOOPP4-LOOPO3 LPLOOPP4 LPLOOPO3 .928E-01
LPLOOPP5 P81 P81P88 .119E-08
RPLOOPP5 P81P88 P88 .401E-04
KLOOPP5-LOOPP6 LPLOOPP5 LPLOOPP6 .229E+00
KLOOPP5-LOOPTE LPLOOPP5 LPLOOPTE .386E+00
KLOOPP5-LOOPO1 LPLOOPP5 LPLOOPO1 .208E+00
KLOOPP5-LOOPO2 LPLOOPP5 LPLOOPO2 .107E+00
KLOOPP5-LOOPO3 LPLOOPP5 LPLOOPO3 .670E-01
LPLOOPP6 P78 P78P85 .933E-09
RPLOOPP6 P78P85 P85 .178E-04
KLOOPP6-LOOPTE LPLOOPP6 LPLOOPTE .212E+00
KLOOPP6-LOOPO1 LPLOOPP6 LPLOOPO1 .184E+00
KLOOPP6-LOOPO2 LPLOOPP6 LPLOOPO2 .121E+00
KLOOPP6-LOOPO3 LPLOOPP6 LPLOOPO3 .106E+00
LPLOOPTE P135 P135P34 .161E-08
RPLOOPTE P135P34 P34 .298E-04
KLOOPTE-LOOPO1 LPLOOPTE LPLOOPO1 .424E+00
KLOOPTE-LOOPO2 LPLOOPTE LPLOOPO2 .174E+00
KLOOPTE-LOOPO3 LPLOOPTE LPLOOPO3 .936E-01
LPLOOPO1 P37 P37P38 .504E-08
RPLOOPO1 P37P38 P38 .621E-04
KLOOPO1-LOOPO2 LPLOOPO1 LPLOOPO2 .411E+00
KLOOPO1-LOOPO3 LPLOOPO1 LPLOOPO3 .141E+00
KLOOPO1-LOOPC LPLOOPO1 LPLOOPC .648E+00
LPLOOPO2 P38 P38P39 .274E-08
RPLOOPO2 P38P39 P39 .418E-04
KLOOPO2-LOOPO3 LPLOOPO2 LPLOOPO3 .154E+00
KLOOPO2-LOOPC LPLOOPO2 LPLOOPC .521E+00
LPLOOPO3 P42 P42P43 .199E-09
RPLOOPO3 P42P43 P43 .853E-05
KLOOPO3-LOOPC LPLOOPO3 LPLOOPC .339E+00
LPLOOPU1 P32 P32P134 .936E-09
RPLOOPU1 P32P134 P134 .178E-04
LPLOOPU2 P137 P137P138 .400E-08
RPLOOPU2 P137P138 P138 .613E-04
LPLOOPC P2 P2P3 .150E-07
RPLOOPC P2P3 P3 .472E+01
LPLOOPU3 P138 P138P139 .119E-09
RPLOOPU3 P138P139 P139 .535E-05
LPLOOPU4 P64 P64P66 .519E-08
RPLOOPU4 P64P66 P66 .106E-03
LPLOOPU5 P29 P29P30 .211E-09
RPLOOPU5 P29P30 P30 .712E-05
LPLOOPU6 P10 P10P11 .693E-09
RPLOOPU6 P10P11 P11 .190E-04
LPLOOPU7 P8 P8P9 .113E-08
RPLOOPU7 P8P9 P9 .240E-04
KLOOPU7-LOOPU8 LPLOOPU7 LPLOOPU8 .432E+00
KLOOPU7-LOOPU9 LPLOOPU7 LPLOOPU9 .131E+00
KLOOPU7-LOOPU10 LPLOOPU7 LPLOOPU10 .433E+00
LPLOOPU8 P6 P6P7 .439E-08
RPLOOPU8 P6P7 P7 .466E-04
LPLOOPU9 P44 P44P45 .346E-08
RPLOOPU9 P44P45 P45 .802E-04
KLOOPU9-LOOPU10 LPLOOPU9 LPLOOPU10 .131E+00
LPLOOPU10 P76 P76P83 .172E-09
RPLOOPU10 P76P83 P83 .785E-05
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Rmasse P45 0 100MEG
.END

created using parts release 6.3 on 12/18/95 at 13:17
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+ AGD=12.500E-6 WB=117.00E-6 VT=4.9910 KF=.5005 CGS=32.809E-9
COXD=31.596E-9
+ VTD=2.621
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*ST: Vce=10
*LN: Vge=15
*CP: Qge=75.000E-9 Qgc=275.00E-9 Qg=450.00E-9 Vg=15 Vcc=300 Ic=150
*EndSpec

*BeginTrace
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*ST: 0,0,0,13,1,3,0,0,-1 (27)
*LN: 0,0,1.0000E-3,300,1,3,0,0,-1 (27)
*CP: 0,0,0,900.00E-9,1,3,0,0,-1 (27)
*EndTrace

*BeginParam
*TAU=309.77E-9 (1.0000E-9,100.00E-6,0)
*KP=1.8526 (.12,100,0)
*AREA=75.000E-6 (1.0000E-12,1.0000E-3,0)
*AGD=30.000E-6 (100.00E-9,1.0000E-3,0)
*WB=90.000E-6 (1.0000E-9,1.0000E-3,0)
*VT=5.0418 (.8,100,0)
*MUN=1.5000E3 (100.00E-6,1.0000E6,0)
*MUP=450 (100.00E-6,1.0000E6,0)
*BVF=2 (100.00E-6,10,0)
*NB=200.00E12 (1,1.0000E30,0)
*JSNE=650.00E-15 (1.0000E-15,1.0000E-3,0)
*BVN=4 (.1,100,0)
*KF=.5 (.5,1.0000E3,0)
*THETA=20.000E-3 (100.00E-6,10,0)
*CGS=10.934E-9 (1.0000E-15,1.0000E-3,0)
*COXD=1.0000E-3 (1.0000E-15,1.0000E-3,0)
*VTD=-5 (-100,100,0)
*EndParam

*DEVICE=IXGH10N100A-X,NIGBT

* IXGH10N100A-X NIGBT model
* created using Parts release 8.0 on 07/08/99 at 23:11
* Parts is a MicroSim product.
.MODEL IXGH10N100A-X NIGBT
+ TAU=309.77E-9
+ KP=1.8526
+ AREA=75.000E-6
+ AGD=30.000E-6
+ VT=5.0418
+ BVF=2
+ KF=.5
+ CGS=10.934E-9
+ COXD=1.0000E-3
+ VTD=-5
*$
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VITA

Kalyan Siddabattula was born on the 21st May 1976 in Visakhapatnam, India. His schooling was done in Visakhapatnam. He completed his Bachelor of Engineering degree in Electrical and Electronics Engineering, from Andhra University, Visakhapatnam, India (1993-1997). He then joined the Center for Power Electronics Systems in 1997, for his Masters degree in Electrical Engineering. His primary interests are power packaging, modeling of layout in packaging, and control systems. He will be pursuing a professional career in Advanced Energy inc., Fort Collins, Colorado as a power supply design engineer.