High Temperature Microwave Frequency Voltage-Controlled Oscillator

Nathan Isaac Turner

Thesis submitted to the faculty of the Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Master of Science

In

Electrical Engineering

Dong S. Ha

William T. Baumann

Yang Yi

July 5, 2018

Blacksburg, VA

Keywords: high temperature, downhole communication, GaN on SiC, extreme environment, VCO

High Temperature Microwave Frequency Voltage Controlled Oscillator

Nathan Turner

ABSTRACT

As the oil and gas industry continues to explore higher temperature environments, electronics that operate at those temperatures without additional cooling become critical. Additionally, current communications systems cannot support the higher data-rates being offered by advancements in sensor technology. An RF modem would be capable of supplying the necessary bandwidth to support the higher data-rate. A voltage-controlled oscillator is an essential part of an RF modem. This thesis presents a 2.336-2.402 GHz voltage-controlled oscillator constructed with 0.25 μm GaN-on-SiC technology high electron mobility transistor (HEMTs). The measured operating temperature range was from $25°C$ to $225°C$. A minimum tuning range of 66 MHz, less than 20% variation in output power, and harmonics more than 20 dB down from the fundamental is observed. The phase noise is between -88 and -101 dBc/Hz at 100 kHz offset at $225°C$. This is the highest frequency oscillator that operates simultaneously at high temperatures reported in literature.

High Temperature Microwave Frequency Voltage Controlled Oscillator

Nathan Isaac Turner

GENERAL AUDIENCE ABSTRACT

The oil and gas industry require communications systems to transmit data collected from sensors in deep wells to the surface. However, the temperatures of these wells can be more than 210 $°C$. Traditional Silicon based circuits are unable to operate at these temperatures for a prolonged period. Advancements in wide bandgap (WBG) semiconductor devices enable entrance into this realm of high temperature electronics. One such WBG technology is Gallium Nitride (GaN) which offers simultaneous high temperature and high frequency performance. These properties make GaN an ideal technology for a high temperature RF modem. A voltage-controlled oscillator is an essential part of a RF modem. This thesis demonstrates a GaN-based 2.36 GHz voltage-controlled oscillator (VCO) whose performance has been measured over a temperature range of $25°C$-$225°C$. This is the highest frequency oscillator that operates simultaneously at high temperatures reported in literature.

Acknowledgements

I would like to thank my advisor Dr. Dong S Ha for allowing me to work on this project. Along the way I learned a lot and am grateful to have been a part of this work. I would also like to thank Dr. Cindy Yi and Dr. William Baumann for serving on my defense committee.

Without the support and help from my colleagues this work would not have been possible. I would like to extend thanks to Jebreel Salem, Brannon Kerrigan, Alante Dancy, Keyvan Ramezanpour, and many more.

Finally, I would like to extend thanks to my girlfriend Laura, my family, and my friends who supported me through this degree. Without their continued support, I would not have been able to go to graduate school and earn this degree.

Table of Contents

List of Figures

List of Tables

Chapter 1

1 Introduction

There has been a large demand in industry for electronics capable of operating in harsh environments and more specifically high-temperature environments [1]. In this work high temperature refers to temperatures greater than 200 °C. Advances in semiconductor technologies enable cost effective solutions for high-temperature electronics (HTE) that have historically required bulky and expensive cooling systems. This in turn enables industries to explore previously inaccessible areas such as deep oil wells and high temperature environments in space [2].

Several different industries such as automotive, aerospace, and oil and gas exist that have a need for HTEs. This work will focus primarily on the oil and gas industry.

1.1 Motivation

The oil and gas industries are the oldest users of HTEs. As the industry continues to drill deeper temperatures in the hotter wells can exceed $200\ °C$. This exceeds the ambient temperature rating of traditional CMOS technologies. Passive cooling is not an option in this type of environment because over time the passive heatsink has the same temperature as the surrounding area. Active cooling is typically not practical due to the inefficiencies, added weight, and cost. For these reasons, electronics that can operate in these environments without additional cooling are valuable to the well-drilling industry.

Most of the research in this area has been focused on power electronics and low frequency circuits and sensors. The data rate of telemetry systems needs to be increased to account for higher resolution sensors, faster logging speeds, and additional tools. Current telemetry systems operate at a low data rate < 4 Mb/s [3, 4]. The system proposed by Tran et al. [4] is based on multi-conductor transmission from the well to the surface and has only two telemetry channels of relatively low bandwidth. Radio over fiber (ROF) presents a potential solution to the problem of low bandwidth. ROF takes an analog RF signal modulated with the data and then in turn modulates the light wave being transmitted over the fiber optic cable. ROF would be able to utilize the existing sensors that have electrical signals being transmitted over coaxial cable, and interface them with a single optical link. This enables high bandwidth capable of supporting high data rates and a large number of tools [5].

For ROF, an RF Modem capable of operating at high temperatures must be created. A typical single heterodyne RF transceiver is shown in Figure 1-1. The building blocks in Figure 1-1 must be capable of operating at high temperatures without any additional cooling. In general, the active circuits will present a larger challenge than the passive components such as the bandpass filters. This work will focus on the application and design of the VCO block.

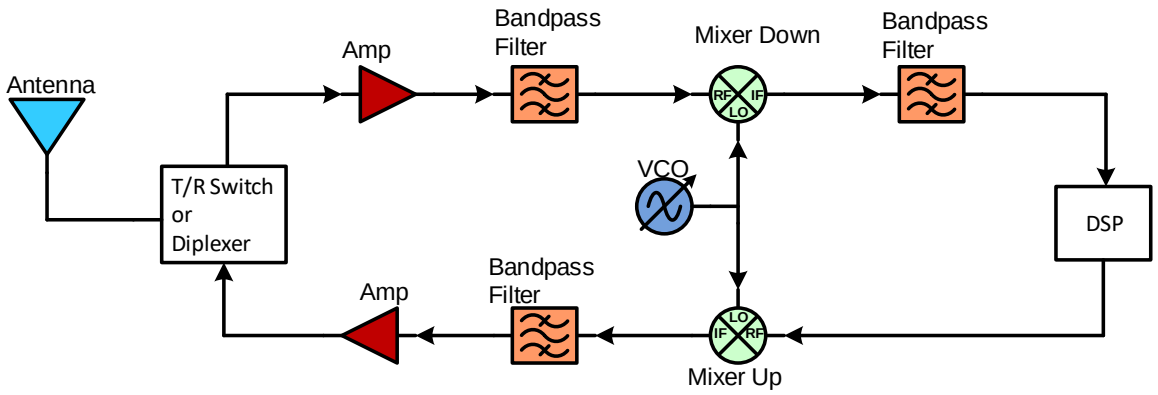


Figure 1-1 Typical single heterodyne transceiver architecture [6]

1.1.1 Technology

Silicon based devices are by far the most common in the field of electronics, however, certain fundamental properties make it nonviable for temperatures greater than 200 $°C$. Advancements in device technology are what make extreme temperature electronics a possibility. In particular, wide-bandgap (WBG) devices have emerged as a favored candidate for high temperature applications [7]. Although much of the market share for WBG devices has been for high power – and a correspondingly high junction temperature – they have also been shown to perform well for low power, high ambient temperature electronics that do not require cooling [1, 8-10]. The two most common WBG semiconductors are Silicon Carbide (SiC) and Gallium Nitride (GaN). Both have energy bandgaps greater than 3 eV which will later be shown to be a critical component in reducing leakage current at high temperatures. GaN High Electron Mobility Transistors (HEMTs) have been widely used in the field of microwave power amplifiers due to their high-power handling capability coupled with a high transition frequency (f_T) [9]. These reasons make GaN a more suitable candidate for high temperature RF/Microwave circuits than SiC.

1.1.2 Summary

The Voltage Controlled Oscillator (VCO) demonstrated in this work is designed and prototyped using commercial-off-the-shelf (COTS) GaN-on-SiC transistors, chosen for their high junction temperature and frequency capability. Reactive elements are realized using microstrip segments to reduce temperature variation. The VCO is intended to function as the local oscillator for a downhole communication system. To the author's best knowledge, this VCO represents the highest temperature implementation of a 2.336-2.402 GHz VCO. The VCO demonstrates an output power variation less than 20% over a temperature range of 25 $°C$-225$°C$, and a minimum phase noise of -114 dBc/Hz and -101 dBc/Hz at 100 kHz offset for 25 $°C$ and 225 $°C$ respectively. Harmonic content is 20 dB or more below the fundamental.

This work demonstrates the feasibility of GaN-on-SiC HEMTs for frequency synthesis at high temperatures and frequencies > 2 GHz.

1.1.3 Thesis Organization

This thesis is organized as follows: Chapter 2 will present background information necessary to understand high temperature microwave oscillator design. A review of different microwave engineering principals is covered followed by a review of negative resistance oscillator fundamentals. Thermal effects in semiconductors is also discussed. The end of the chapter presents a literature review on existing high temperature oscillators.

Chapter 3 will cover the full design process for the VCO. This chapter will start with active device selection, and then discuss the biasing network. A design procedure

for selecting the reactive elements is then discussed along with how to realize these reactive elements through microstrip. The chapter concludes with the full schematic and layout of the VCO. Chapter 4 covers the measurement setup and measured results of the VCO. This is followed by analysis of the measured results. Chapter 5 concludes this thesis.

Chapter 2

2 Background

This chapter will give a brief overview of necessary concepts to understand microwave oscillator design. This includes: scattering parameters, stability, microstrip transmission lines, oscillator fundamentals, and negative resistance oscillators. Additionally, this chapter will discuss temperature effects in semiconductors with an emphasis on WBG devices. The chapter will conclude with a literature review of existing high temperature oscillators.

2.1 Definitions and Concepts

2.1.1 S-Parameters

Typical low frequency systems can be characterized by their immittance parameters, that is by measuring the impedance (Z) or admittance (Y) parameters. This is done by driving a port with a voltage (current) while open (short) circuiting all other ports and measuring the voltage (current) at the port to get the respective Z (Y) parameter. This method of measurement becomes less feasible at higher frequencies because it becomes difficult to realize an open or short circuit and these types of terminations can sometimes result in large reflections or instabilities that can damage the device under test (DUT) [11].

Scattering parameters (S-Parameters) avoid the problems mentioned by relating the forward and backward traveling waves on a transmission line. For a one port the forward and backward traveling waves can be related with a reflection coefficient. Referring to Figure 2-1, the reflection coefficient at z = 0 i.e. at the load can be calculated as shown in Eq. 2.1.

$$\Gamma(x) = \frac{V^+(x)}{V^-(x)} \rightarrow \Gamma_L = \frac{V^+(0)}{V^-(0)} = \frac{Z_L - Z_o}{Z_L + Z_o} \qquad (2.1)$$

Where $V^+(0)$ is the incident voltage wave at z=0, and $V^-(0)$ is the reflected voltage wave at z=0. From this we can see that the reflection relates the incident and reflected voltage waves in terms of impedance terminations. Also, it is evident that if Z_L=Z_o meaning the load is *matched* to the input impedance -- in this case the characteristic impedance of the transmission line -- that there is no reflection.

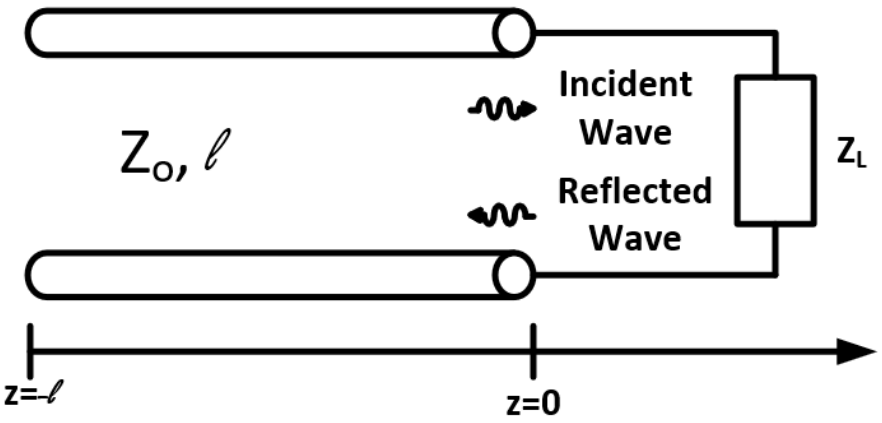


Figure 2-1 Transmission line with characteristic impedance Z_o, and length l terminated in a load impedance of Z_L [12]

A two-port network is shown in Figure 2-2 where V_n^+ represents an incident voltage traveling wave, and V_n^- is a reflected voltage traveling wave. The relationship

between the reflected waves and the incident waves can be written in terms of the S-parameters as shown in Eq. 2.2 and 2.3.

$$V_1^- = s_{11}V_1^+ + s_{12}V_2^+ \tag{2.2}$$

$$V_2^- = s_{21}V_1^+ + s_{22}V_2^+ \tag{2.3}$$

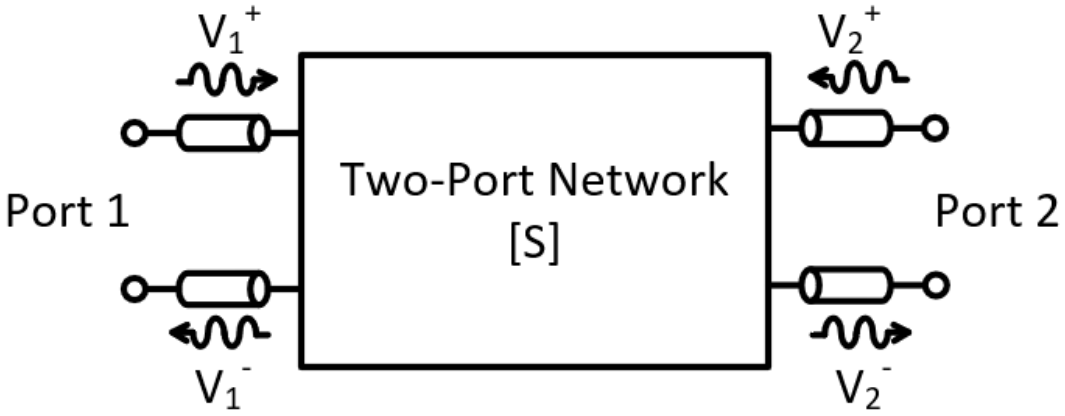


Figure 2-2 Two-Port Network with transmission lines on ports

From Eq. 2.2 and 2.3, the S-parameters are found by terminating a certain port in a matched load to eliminate reflections at that port and measuring the incident and reflected voltage traveling waves. This is shown in Eqs 2.4-2.7.

$$s_{11} = \left.\frac{V_1^-}{V_1^+}\right|_{V_2^+=0} \tag{2.4}$$

$$s_{12} = \left.\frac{V_1^-}{V_2^+}\right|_{V_1^+=0} \tag{2.5}$$

$$s_{21} = \left.\frac{V_2^-}{V_1^+}\right|_{V_2^+=0} \tag{2.6}$$

$$s_{22} = \left.\frac{V_2^-}{V_2^+}\right|_{V_1^+=0} \tag{2.7}$$

S-parameters provide a linear set of variables to characterize any network at microwave frequencies. They are essentially measures of the reflected and incident power and lend themselves well to RF/microwave circuits where power transfer is a critical concern.

2.1.2 Stability

There are many different measures of stability in microwave circuits. The Rollet Stability Criterion states a circuit is unconditionally stable – meaning any combination of load and source impedances will result in a stable circuit – if the conditions in Eq. 2.8-10 are satisfied [13].

$$k > 1 \;\&\; |\Delta| < 1 \tag{2.8}$$

where

$$k = \frac{1 - |s_{11}|^2 - |s_{22}|^2 + |\Delta|^2}{2|s_{12}||s_{21}|} \tag{2.9}$$

$$\Delta = s_{11}s_{22} - s_{12}s_{21} \tag{2.10}$$

Another measure of stability is the Edwards-Sinsky stability Criterion and given in Eq. 2.11-2.12 [13].

$$\mu = \frac{1 - |s_{11}|^2}{|s_{22} - s_{11}^* \Delta| + |s_{21} s_{12}|} > 1 \tag{2.11}$$

or

$$\mu' = \frac{1 - |s_{22}|^2}{|s_{11} - s_{22}^* \Delta| + |s_{21} s_{12}|} > 1 \tag{2.12}$$

The μ-Factor stability is popular due to a single parameter being used to determine unconditional stability. The Rollet stability criterion or the Edwards-Sinsky criterion are generally enough of a measure for stability for single stage active device designs, however the most complete measure of stability is the Nyquist stability criterion. The Nyquist stability criterion states that if the open-loop transfer function plotted in the complex plain encircles the -1 point in a clockwise rotation with increasing frequency the system is unstable [13].

2.1.3 Microstrip

At higher frequencies, the electrical size of the interconnects between two points become a significant portion or larger than the wavelength of the signal. These interconnects are called *transmission lines* and are referred to as *distributed structures,* where the voltage and current can vary at different points along the line. In other words the spatial change in the signal can no longer be ignored when the length of the interconnects becomes long with regards to the wavelength of the signal [14].

A lossless line with a characteristic impedance Z_o, of length l, and terminated in a load impedance of Z_L is shown in Figure 2-3.

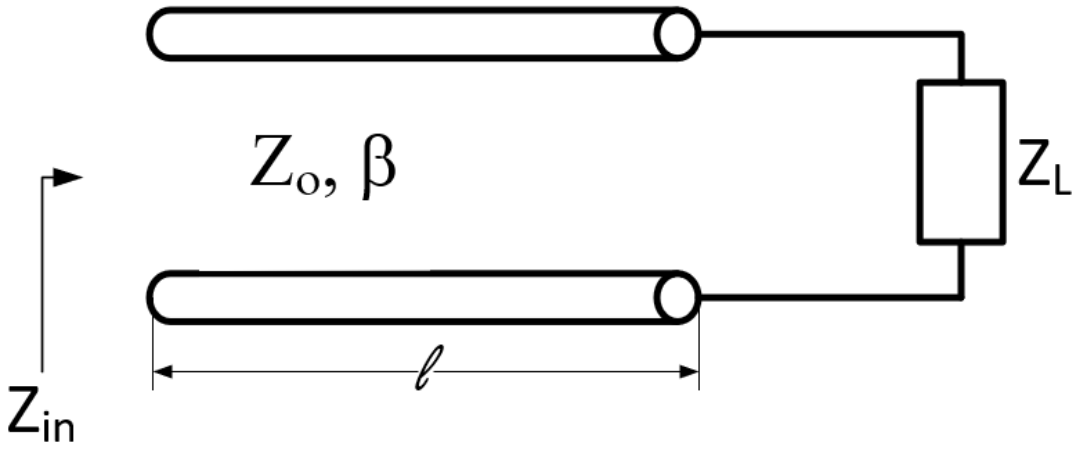


Figure 2-3 Lossless, terminated transmission line

The input impedance is given by

$$Z_{in} = Z_o \frac{Z_L + jZ_o \tan(\beta l)}{Z_o + jZ_L \tan(\beta l)} \tag{2.13}$$

Where

$$\beta = 2\pi/\lambda \tag{2.14}$$

It should be noted that Eq. 2.13-14 implies that the impedance is periodic with frequency and length. A line of length $\lambda/2$ at a frequency f_o appears as a line of length λ at a frequency $2f_o$. It is also apparent from Eq. 2.13 that if the line is terminated in a short-circuit the line acts inductive for $l < \lambda/4$. This relationship is shown in Eq. 2.15. Similarly, a line terminated in an open circuit acts capacitive for $l < \lambda/4$, shown in Eq. 2.16.

$$Z_{in}(Z_L = 0) = jZ_o \tan(\beta l) \tag{2.15}$$

$$Z_{in}(Z_L \to \infty) = jZ_o \cot(\beta l) \tag{2.16}$$

This means that open circuit and short circuit transmission lines can be used to realize reactive elements for resonators or matching elements in matching networks which will be discussed later in the chapter. It should also be noted that an impedance transformation occurs at $l = \lambda/4$, where a quarter-wavelength short-circuited transmission line looks like an open-circuit at f_o, and a quarter-wave open-circuit transmission line looks like a short-circuit at f_o.

Microstrip is a one type of transmission line that is easily manufacturable with commercial Printed Circuit Board (PCB) processes. It is a planar transmission line that supports quasi-TEM wave propagation. The design formulas for microstrip are summarized below [15].

The effective dielectric constant is approximated by

$$\epsilon_e = \frac{\epsilon_R + 1}{2} + \frac{\frac{\epsilon_R - 1}{2} 1}{\sqrt{1 + \frac{12d}{w}}} \tag{2.17}$$

For a given characteristic impedance Z_o and dielectric constant ϵ_r, the w/h ratio can be found as

$$w/h = \begin{cases} \dfrac{8e^A}{e^{2A} - 2}, & w/h < 2 \\ \dfrac{2}{\pi}\left[B - 1 - \ln(2B - 1) + \dfrac{\epsilon_R - 1}{2\epsilon_r}\left\{\ln(B - 1) + 0.39 - \dfrac{0.61}{\epsilon_R}\right\}\right], & w, h \geq 2 \end{cases} \tag{2.18}$$

Where

$$A = \frac{Z_o}{60}\sqrt{\frac{\epsilon_R + 1}{2}} + \frac{\epsilon_R - 1}{\epsilon_R + 1}\left(0.23 + \frac{0.11}{\epsilon_R}\right) \tag{2.19}$$

$$B = \frac{377\pi}{2Z_o\sqrt{\epsilon_R}} \tag{2.20}$$

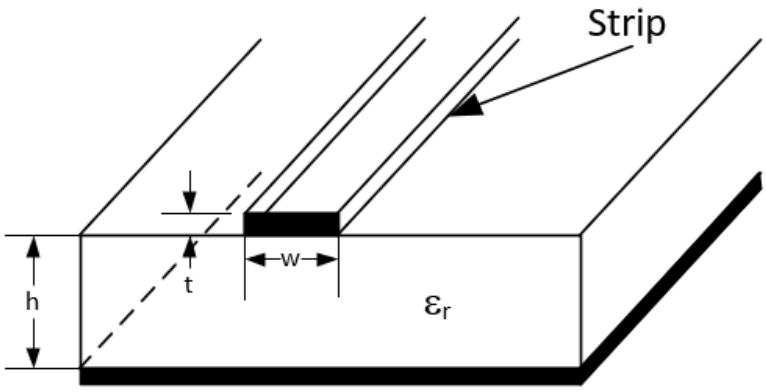


Figure 2-4 Microstrip line structure [6]

Using Eq. 2.17-20, the width of microstrip lines can be determined given the height of the substrate which is determined by the PCB process.

2.1.4 Matching Network

A matching network transforms the impedance of the source to achieve a certain type result such as

1) Maximum power transfer
2) Noise matching
3) Reflection-less matching

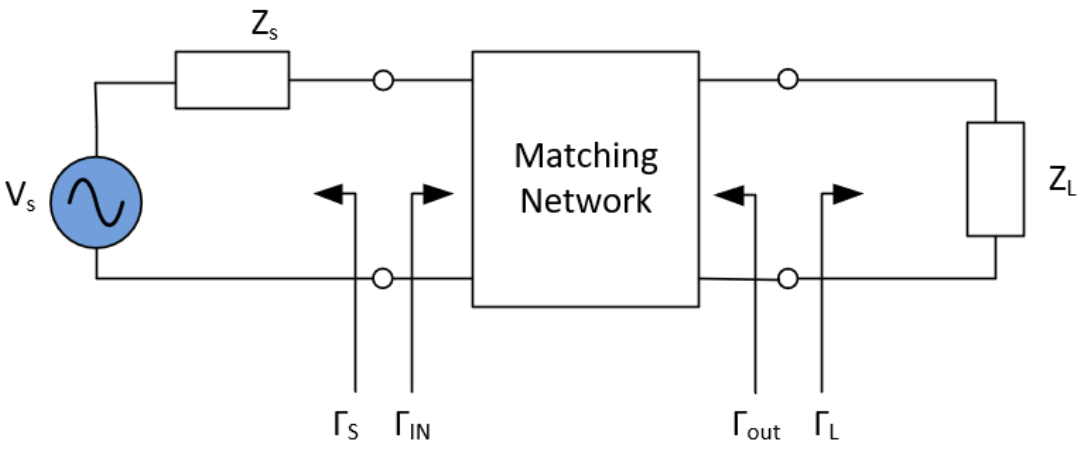


Figure 2-5 Source Impedance being transformed by matching network

Referring to Figure 2-5, for maximum power transfer

$$\Gamma_{in} = \Gamma_s^* \tag{2.21}$$

and

$$\Gamma_{out} = \Gamma_L^* \tag{2.22}$$

The matching network should be composed of purely reactive elements so that there is little or no loss in the matching network. Using distributed elements, a single frequency 2-element matching network can be synthesized using either the Smith Chart or analytical solutions. The general schematic for single stub matching networks are shown in Figure 2-6.

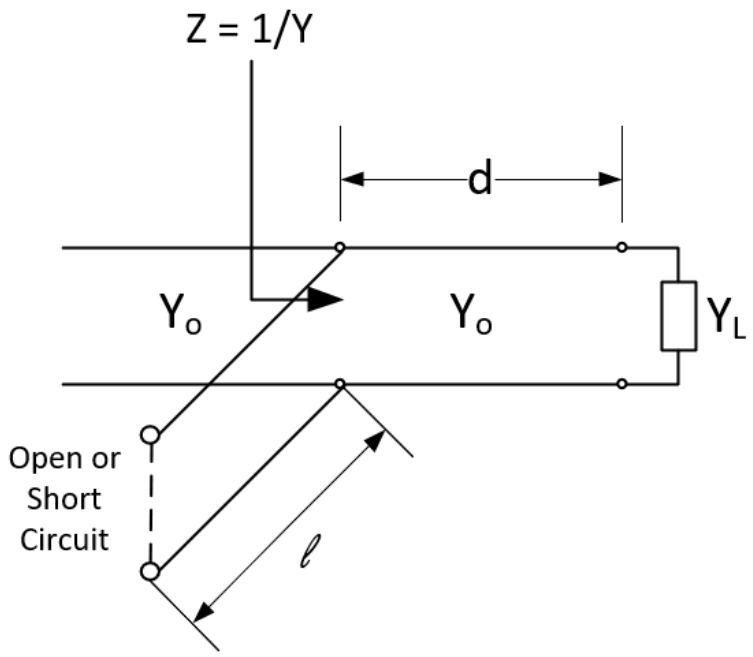


Figure 2-6 Single-Stub Matching

Analytical formulas for determining *l* and *d* are shown below [16]. First let $Z_L = \frac{1}{Y_L} = R_L + jX_L$. The impedance Z looking at the start of the line of length *d* from Eq. 2.13 is

$$Z = Z_o \frac{(R_L + jX_L) + jZ_o t}{Z_o + j(R_L + jX_L)t} \tag{2.23}$$

Where $t = \tan(\beta d)$. The admittance at this point is

$$Y = \frac{1}{Z} = G + jB \tag{2.24}$$

Where

$$G = \frac{R_L(1 + t^2)}{R_L^2 + (X_L + Z_o t)^2} \tag{2.25}$$

$$B = \frac{\left(R_L^2 t - (Z_o - X_L t)(X_L + Z_o t)\right)}{Z_o(R_L^2 + (X_L + Z_o t)^2)} \tag{2.26}$$

t can then be chosen to match the real part of the admittance i.e. $G = G_o = Y_o = 1/Z_o$

$$t = \frac{X_L \pm \sqrt{\frac{R_L[(Z_o - R_L)^2 + X_L^2]}{Z_o}}}{R_L - Z_o} \; for\; R_L \neq Z_o \tag{2.27}$$

If $R_L = Z_o$, then $t = -\frac{X_L}{2Z_o}$. If $R_L \neq Z_o$, then the solutions for *d* are as follows

$$\frac{d}{\lambda} = \begin{cases} \frac{1}{2\pi}\tan^{-1} t\,, & t \geq 0 \\ \frac{1}{2\pi}(\pi + \tan^{-1} t)\,, & t < 0 \end{cases} \tag{2.28}$$

Then, the value of t can be used in Eq. 2.26 to find the susceptance B that the open or short circuit stub needs to cancel.

For an open-circuit stub

$$\frac{l_o}{\lambda} = \frac{1}{2\pi}\tan^{-1}\frac{B_s}{Y_o} = -\frac{1}{2\pi}\tan^{-1} - \frac{B}{Y_o} \tag{2.29}$$

And for a short-circuit stub

$$\frac{l_s}{\lambda} = -\frac{1}{2\pi}\tan^{-1}\frac{Y_o}{B_s} = \frac{1}{2\pi}\tan^{-1}\frac{Y_o}{B} \tag{2.30}$$

And if the solutions for Eq 2.29-30 are negative, then $\frac{\lambda}{2}$ can be added to the length.

2.2 Oscillator Fundamentals

There are a large variety of oscillators, and the fundamental goal of oscillator design is to synthesize a circuit whose output is a periodic signal of some frequency when there is no input signal. The type of signal output depends on the application, and could range from a triangular waveform, a square wave, and the most common: a sinusoid. This section will discuss classic feedback oscillator theory, as well as give explanation of some of the important parameters of an oscillator.

2.2.1 Oscillation Conditions

First, consider the basic feedback system of Figure 2-7. The closed loop voltage gain is given as

$$H(s) = \frac{V_o(s)}{V_i(s)} = \frac{A(j\omega)}{1 - A(j\omega)\beta(j\omega)} \tag{2.31}$$

Where $A(j\omega)\beta(j\omega)$, is the loop gain. An oscillator must oscillate without an input signal. The only way this condition is satisfied is if the voltage gain approaches infinity. This condition is known as the Barkhausen Criteria and is written as

$$A(j\omega)\beta(j\omega) = 1\angle 0^{\circ} \tag{2.32}$$

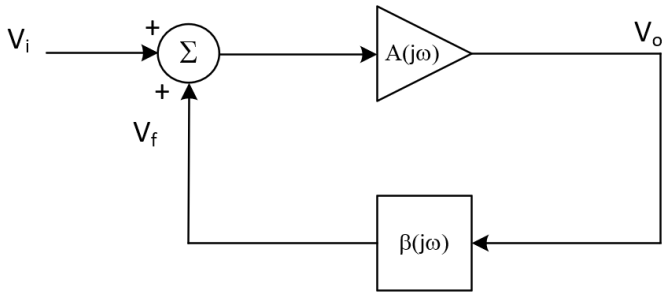


Figure 2-7 Basic Feedback System

The feedback system is then a frequency selective system that ensures that

1) The loop gain is equal to one at the frequency of interest
2) The total phase shift around the loop is 0° at the frequency of interest

Obviously, this condition applies to steady-state oscillations. In other words, oscillations occur when a pair of complex-conjugate poles are located on the imaginary axis of a complex plot [17]. In an electronic oscillator, there must be some form of start-up that ensures build-up of oscillations. The initial input voltage could be thermal noise or switching noise from the power supply. For oscillations to build up, the complex-conjugate poles are initially located in the Right-Half-Plane (RHP) of the complex plot. Nonlinear effects shift these RHP poles to the imaginary axis. The most common method of doing so in sinusoidal oscillators is to use a saturation limited amplifier i.e. an amplifier whose gain drops with increasing amplitude [17]. Fortunately, this is true for virtually all non-ideal amplifiers.

2.2.2 Frequency Stability

Frequency stability refers to an oscillators ability to maintain a single oscillation frequency. Long-term stability refers to frequency change due to aging, or thermal effects over time. Short term stability refers to oscillation frequency variation over a short amount of time, normally due to noise, mechanical vibrations, or thermal variations [18]. The frequency stability factor is defined as the change in phase divided by the normalized frequency [18], given by

$$SF = \frac{\Delta\phi}{\frac{\Delta\omega}{\omega_o}} = \omega_o \frac{d\phi}{d\omega}\Big|_{\omega=\omega_o} \tag{2.33}$$

Therefore, the larger the value of SF, the smaller the frequency variation.

2.2.3 Quality Factor

Reactive elements have a certain loss associated with them, and as such any type of resonator has a finite *Quality Factor*. The quality factor is defined as [19]

$$Q = \omega \frac{average\ energy\ stored}{energy\ loss/second} \tag{2.34}$$

Parallel and series resonant circuits with the loss modeled as a resistor R are shown in Figure 2-8.

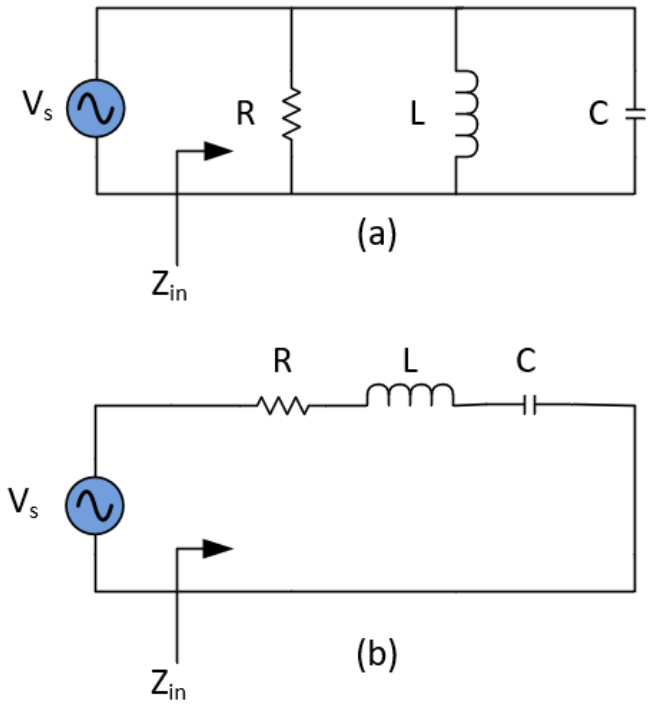


Figure 2-8 (a) Parallel RLC circuit (b) Series RLC circuit

For the parallel RLC circuit, the unloaded Q is

$$Q_u = \frac{R}{\omega_o L} = \omega_o RC \tag{2.35}$$

For the series RLC circuit, the unloaded Q is

$$Q_u = \frac{\omega_o L}{R} = \frac{1}{\omega_o RC} \tag{2.36}$$

Where ω_o is the angular resonant frequency

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{2.37}$$

An external Q can be defined to represent the quality factor of the circuit with the reactive elements and a load R_L, which is placed in series for the series LC network, and in parallel for the parallel LC network. The external Q is then defined as [19]

$$Q_e = \begin{cases} \frac{R_L}{\omega_o L}, & parallel \\ \frac{\omega_o L}{R_L}, & series \end{cases} \tag{2.38}$$

And then the loaded Q can be expressed as the

$$\frac{1}{Q_L} = \frac{1}{Q_e} + \frac{1}{Q_u} \tag{2.39}$$

This expression can be used to determine the bandwidth of the circuit using the following relationship

$$Q = \frac{f_o}{BW} \tag{2.40}$$

Meaning that the narrower the bandwidth the higher the Q.

2.2.4 Phase Noise

Noise in oscillators ultimately contribute to a phase and amplitude variation in the output signal of the oscillator. However, the self-limiting nature of most oscillators heavily reduces the amplitude variation and makes the phase variation a more serious concern [20]. The difference between an ideal sinusoidal oscillator and a noisy oscillator is shown in Figure 2-9.

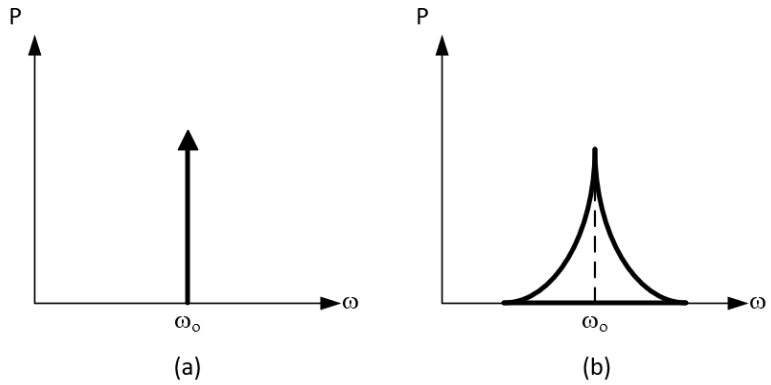


Figure 2-9 (a) Ideal oscillator spectrum (b) Noisy oscillator spectrum

To demonstrate the important of noise in oscillators, referring to Figure 1-1, if the LO spectrum is too wide, when the up or down conversion occurs the oscillator amplitude at offsets from the center frequency could be larger than the signal amplitude in an adjacent channel.

The single-sideband (SSB) phase noise is calculated at some frequency offset from the center frequency $\Delta\omega$, where the noise power in a 1 Hz bandwidth is divided by the signal power at the center frequency. This can be seen in Figure 2-10 and Eq. 2.41.

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{P_{noise}(\omega_o + \Delta\omega)}{P_{signal}}\right)\left[\frac{dBc}{Hz}\right] \qquad (2.41)$$

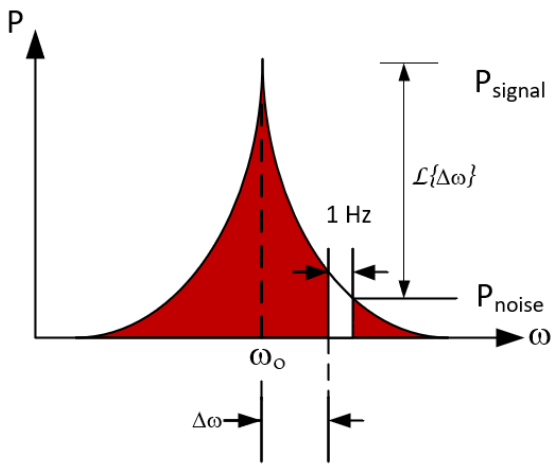


Figure 2-10 Frequency spectrum of noisy oscillator, with phase noise variables labeled

Phase noise arises from thermal noise, shot noise, and flicker noise in transistor based oscillators [18]. Leeson's phase noise model accounts for this in the following expression [20]

$$\mathcal{L}(\Delta\omega) = 10\log\left[\frac{2FkT}{P_{sig}}\left\{1+\left(\frac{\omega_o}{2Q\Delta\omega}\right)^2\right\}\left(1+\frac{\Delta\omega_{\frac{1}{f^3}}}{|\Delta\omega|}\right)\right] \quad (2.42)$$

Where F is an empirical parameter, k is Boltzmann's constant, T is the temperature, P_{sig} is the average power delivered to the load, Q is the loaded quality factor, ω_o is the angular oscillation frequency, $\Delta\omega$ is the offset from the oscillation frequency, and $\Delta\omega_{\frac{1}{f^3}}$ is the frequency corner between the $1/f^2$ and $1/f^3$ regions labeled in Figure 2-11.

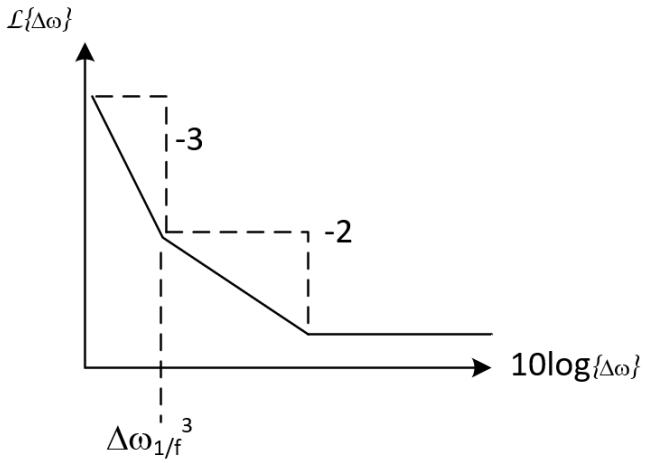


Figure 2-11 Leeson's phase noise model behavior

Leeson's model is based on a time invariant system and suggests that by increasing the signal power and the loaded quality factor that the phase noise will decrease. Unfortunately, there are no analytical expressions for F, and $\Delta\omega_{\frac{1}{f^3}}$ which means that simply increasing signal power and quality factor does not necessarily decrease phase noise due to how that would affect F and $\Delta\omega_{\frac{1}{f^3}}$ [20].

Lee and Hajimiri offer a linear time varying (LTV) model based on the observation that introducing an impulse into a free running oscillator results in a frequency change in that oscillator, but that the effect of the impulse on the frequency change depends on the *time* at which it is injected into the oscillator [20]. They introduce an impulse sensitivity function (ISF) given by

$$\Gamma(\omega_o, \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0\tau) \tag{2.43}$$

The SSB phase noise in the $1/f^2$ region written in terms of the ISF is

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}\Gamma_{rms}^2}{2q_{Max}^2\Delta\omega^2}\right) \tag{2.44}$$

And in the $1/f^3$ region

$$\mathcal{L}(\Delta\omega) = 10\log\left(\frac{\frac{\overline{i_n^2}}{\Delta f}c_0^2}{8q_{Max}^2\Delta\omega^2}\frac{\omega_{\frac{1}{f}}}{\Delta\omega}\right) \tag{2.45}$$

Where $\overline{i_n^2}$ is the mean-square noise spectral density for the current, Δf is the noise bandwidth, q_{Max} is the maximum charge stored in the resonator capacitor which corresponds to the peak voltage swing on the output node and the equivalent capacitance at that node, $\omega_{\frac{1}{f}}$ is the noise corner frequency of the active device, and Γ_{rms} is the root-mean-square value of the ISF.

2.3 Negative Resistance Oscillators

At microwave frequencies the transistor's internal capacitance plays a large role in the oscillator feedback path, making the simple feedback analysis of the previous sections difficult. At these higher frequencies, it is easier to use s-parameters and reflection coefficients to synthesize oscillators.

2.3.1 Two-Port Negative Resistance Oscillator

Figure 2-12 shows a block diagram of a typical microwave oscillator. It consists of a terminating network, an active device, and a load network.

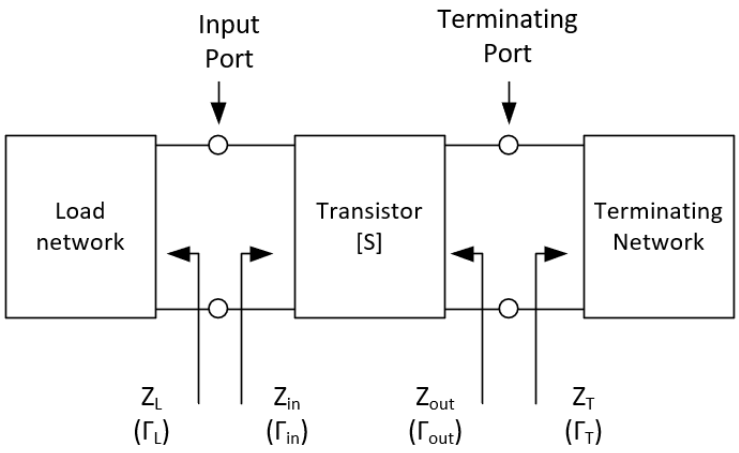


Figure 2-12 Typical microwave oscillator diagram [21]

For there to be oscillations on the input port the following condition must be satisfied [21]

$$Z_{in}(A_o, j\omega_o) + Z_L(A_o, j\omega_o) = 0 \qquad (2.46)$$

This is equivalent to saying that the real part of Z_{in} must be negative to cancel the real part of Z_L and the reactive parts of both must be resonant. The condition of Eq. 2.46 can be written in terms of the load and input reflection coefficients as

$$\Gamma_{in}\Gamma_L = 1 \qquad (2.47)$$

If the input port is oscillating the terminating port also oscillates. This means that to design a negative resistance oscillator, you can choose a potentially unstable transistor, which referring to section 2.1.2 can be done by ensuring that k<1 (from Eq. 2.9). A terminating network can then be designed to present a negative resistance at the input port by exploiting the following relationship [21]

$$\Gamma_{in} = s_{11} + \frac{s_{12}s_{21}\Gamma_T}{1 - s_{22}\Gamma_T} \tag{2.48}$$

Then the load network will be designed to satisfy Eq. 2.46 for *steady-state* operation. At small signal levels the condition $real(Z_L) < real(Z_{in})$ must be satisfied to ensure start-up. A typical value to ensure start-up is to choose

$$R_L = -\frac{R_{in}}{3} \tag{2.49}$$

where R_L is the real part of Z_L and R_{in} is the negative real part of Z_{in}. A more accurate way is to use load-line characterization which utilizes the non-linear device model and will be shown in Chapter 3.

2.4 Thermal Effects in Semiconductors

Temperature impacts several different parameters in semiconductors devices such as: intrinsic carrier density, energy band gap, mobility, velocity saturation, threshold voltage, and leakage current.

2.4.1 Energy Bandgap

The relationship between temperature and the energy band gap can be expressed approximately as [22]

$$E_g(T) \approx E_g(0) - \frac{\alpha_E T^2}{T + \beta_E} \tag{2.50}$$

Where $E_g(0)$ is the band gap energy at absolute zero, and α_E, β_E are material specific constants. It can be seen from Eq. 2.49 that as the temperature increases that the band gap will decrease.

2.4.2 Intrinsic Carrier Density

Intrinsic carrier density is essential in the operation of semiconductor devices in that by doping regions as either n (conduction) or p (valence) type, the fundamental goal is that the intrinsic carriers are small compared to the doped regions. However, the intrinsic carrier density has a strong dependence on temperature expressed as [22]

$$n_i = \sqrt{N_C N_V} e^{-\frac{E_g}{2kT}} \tag{2.51}$$

Where k is Boltzmann's constant, E_g is the energy band gap at absolute zero, and N_C and N_V are the electron and hole density of states respectively. The density of states is affected by temperature, but it is a small variation in comparison to the exponential term in Eq. 2.50. A key take-away from Eq. 2.50 is that the larger the band gap of the device the smaller the intrinsic carrier density is which effectively extends the operating temperature range of the device.

2.4.3 Mobility

The effect of temperature on mobility is a function of four different scattering parameters: phonon scattering μ_{ph}, surface roughness scattering μ_{sr}, bulk charge Coulombic scattering μ_{cb}, and interface charge Coulombic scattering μ_{int}. All these parameters are a function of the effective transverse electric field E_{eff} and temperature T. The scattering parameters can be combined using Matthiessen's rule [23]

$$\frac{1}{\mu_{eff}(E_{eff},T)} \propto \frac{1}{\mu_{ph}(E_{eff},T)} + \frac{1}{\mu_{sr}(E_{eff},T)} + \frac{1}{\mu_{cb}(E_{eff},T)} + \frac{1}{\mu_{int}(E_{eff},T)} \tag{2.52}$$

As temperature increases, the phonon scattering begins to dominate with its dependence of approximately $\mu_{ph} \propto T^{-3/2}$, which causes the effective mobility to decrease as temperature increases.

2.4.4 Velocity Saturation

Velocity saturation refers to the point where increases in energy no longer cause carrier velocity to increase, and this energy is instead lost to phonon scattering. The temperature dependence can be modeled as [23]

$$v_{sat} = v_{sat0}\left[1 - \alpha_{v_{sat}}(T - T_o)\right] \tag{2.53}$$

Where v_{sat0} is the saturation velocity at some nominal temperature T_o.

2.4.5 Threshold Voltage

The threshold voltage for a FET is given by [22]

$$V_T = V_{FB} + 2\Phi_F + \gamma\sqrt{2\Phi_F} \tag{2.54}$$

where

$$V_{FB} = \phi_{gs} - \left(\frac{Q_{ss}}{C_{ox}}\right) \tag{2.55}$$

And the gate-substrate potential is $\phi_{gs} = \frac{kT}{q}\ln\left(\frac{N_A N_G}{n_i^2}\right)$, with N_A and N_G being the substrate and gate doping concentrations. Q_{ss} is the surface charge density, C_{ox} is the gate oxide capacitance, γ is the body effect parameter, and

$$\Phi_F = \frac{kT}{q}\ln\left(\frac{N_A}{n_i}\right) \tag{2.56}$$

is the fermi potential. The two parameters that are affected by temperature in Eq. 2.53 are the fermi potential Φ_F and the gate-substrate potential ϕ_{gs} with their dependence on the intrinsic carrier level n_i which was shown to vary exponentially with temperature in Eq. 2.50, and the thermal voltage dependence $\frac{kT}{q}$. The threshold voltage dependence on temperature can then be written as [23]

$$\frac{\partial V_T}{\partial T} = \frac{\partial \phi_{gs}}{\partial T} + 2\frac{\partial \Phi_F}{\partial T} + \frac{\gamma}{\sqrt{2\Phi_F}}\frac{\partial \Phi_F}{\partial T} \tag{2.57}$$

where the temperature dependences of ϕ_{gs} and Φ_F are

$$\frac{\partial \phi_{gs}}{\partial T} = \frac{1}{T}\left(\phi_{gs} + \left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right)\right) \tag{2.58}$$

$$\frac{\partial \Phi_F}{\partial T} = \frac{1}{T}\left(\Phi_F - \frac{1}{2}\left(\frac{E_{G0}}{q} + \frac{3kT}{q}\right)\right) \tag{2.59}$$

When using typical parameters, the threshold voltage is shown to decrease with increasing temperature

2.4.6 Leakage Current

There are two major types of leakage current, the first kind is p-n junction leakage which refers to how much current goes through the p-n junction when a reverse bias is applied, and the second is thermionic leakage. The I-V behavior of a p-n junction diode is approximately

$$I \approx qAn_i \left[\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} \left(e^{\frac{qV_A}{kT}} - 1 \right) + \frac{W}{2\tau} \left(e^{\frac{qV_A}{2kT}} - 1 \right) \right] \tag{2.60}$$

where A is the area of the p-n junction, V_A is the voltage applied to the diode, N_D is the n-type doping density, W is the width of the junction depletion region at applied voltage V_A, D_p is the hole diffusion constant, and τ is the effective minority carrier lifetime [7]. The first exponential term is due to the diffusion current, and the second exponential term is due to the thermal generation of carriers that occurs in the depletion region of a biased diode. For a negative V_A greater than the thermal voltage the exponential term becomes insignificant compared to -1, and Eq. 2.59 can be reduced to [7]

$$I \approx -qAn_i \left[\frac{n_i}{N_D} \sqrt{\frac{D_P}{\tau}} + \frac{W}{2\tau} \right] \tag{2.61}$$

which demonstrates the heavy dependence of p-n junction leakage current on the intrinsic carrier density. As was noted previously, a device with a larger band gap results in exponentially smaller intrinsic carrier density.

Another type of leakage current is thermionic leakage, which refers to when carriers gain sufficient energy from the environment to go over or tunnel through the energy barrier in a device [7]. This process is called emission and is a function of temperature and the I-V relationship is

$$I \approx AK^* T^2 e^{-\frac{q\Phi_B}{kT}} \left(e^{\frac{qV_A}{kT}} - 1 \right) \tag{2.62}$$

where K^* is the effective Richardson constant of the semiconductor and Φ_B is the Schottky barrier height. For $V_A < \sim -0.2\ V$, Eq. 2.61 reduces to [7]

$$I \approx -AK^{*}T^{2}e^{-\frac{q\Phi_B}{kT}} \tag{2.63}$$

Φ_B is closely related the energy band gap for the device and therefore larger device band gaps cause the leakage current due to thermal emission decreases exponentially.

2.5 Wide Bandgap Devices

As was pointed out in Section 2.4, devices with a large energy band gap allow for higher temperature operation due to their exponentially lower n_i -- which in turn reduces the p-n junction leakage -- and from Eq. 2.62, it is evident that the thermionic leakage also decreases exponentially with increasing band gap. Silicon Carbide (SiC) and Gallium Nitride (GaN) are the two most popular Wide Band Gap (WBG) devices. A comparison of the intrinsic carrier concentration of SiC, GaN, and Silicon are shown in Figure 2-13.

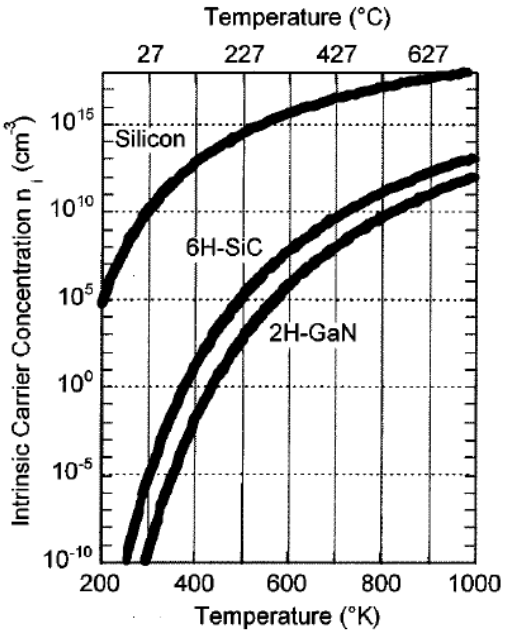


Figure 2-13 Intrinsic carrier concentration for different technologies [7]

A comparison of several parameters is shown in Table 2-1, where Diamond shows the best performance in almost every category. Unfortunately, Diamond semiconductor technology is still in its infancy and is not commercially available. SiC has the highest thermal conductivity of all of them – excluding Diamond -- which is a measure of how much the junction temperature raises with increasing power dissipation. GaN has a much higher mobility than SiC enabling its use at microwave frequencies. SiC and GaN see most of their use in high-power applications. These same devices can instead be operated at low-power for use at higher ambient temperatures than their commercial rating.

Table 2-1 Comparison of different technologies [9]

	Si	*GaAs*	*4H − SiC*	*GaN*	*Diamond*
$E_g\ (eV)$	1.1	1.42	3.26	3.39	5.45
$n_i(cm^{-3})$	$1.5x10^{10}$	$1.5x10^{6}$	$8.2x10^{-9}$	$1.9x10^{-10}$	$1.6x10^{-27}$
ϵ_r	11.8	13.1	10	9.0	5.5
$\mu_n\left(\frac{cm^2}{Vs}\right)$	1350	8500	700	1200 (bulk) 2000 (2DEG)	1900
$v_{sat}\left(10^7\frac{cm}{s}\right)$	1	1	2	2.5	2.7
$\Theta\left(\frac{W}{cmK}\right)$	1.5	0.43	3.3-4.5	1.3	20
$E_{br}\left(\frac{MV}{cm}\right)$	0.3	0.4	3.0	3.3	5.6

For temperatures above $200\ °C$ Silicon-on-Insulator technology is also a viable technology but as the temperature begins to increase past $300\ °C$ the intrinsic carrier density issue evidenced in Figure 2-13, becomes the limiting factor.

2.6 Literature Review

There has been little research concerning high temperature oscillators [24-27], and even less research regarding high temperature VCOs [28, 29].

Schwartz et al. demonstrate [25] a Silicon Carbide (SiC) MESFET based cross-coupled oscillator shown to be able to operate up to 125 °C at a frequency of 515 MHz, and then as the temperature increases the load and bias need to be adjusted which allows them to achieve an oscillation frequency of 610 MHz and 435 MHz at 200 °C and 475 °C respectively. The same group was able to demonstrate a SiC MESFET Clapp oscillator at 1 GHz operating at 200 °C [26]. A group at the NASA Glenn Research Center characterized two oscillators – one at 720 MHz, another at 940 MHz – from room temperature to 200 °C and 250 °C [27]. Both oscillators were hybrid implementations

using SiC MESFETs. Lu et al. presented a GaN-on-Si-Based Lamb-Wave oscillator operating at 58 MHz up to 250 °C [24] .

These oscillators are all Fixed-Frequency Oscillators (FFOs), that suffered from either relatively large variation in frequency, or output power with temperature. A monolithic VCO in Silicon-on-Sapphire is presented in [28] operating from 270 MHz to 370 MHz up to 200 °C albeit with relatively large close in phase noise. A discrete GaN High Electron Mobility Transistor (HEMT) based VCO is presented in [29] that demonstrates a 350 MHz center frequency oscillator with a 40 MHz tuning range operating up to 230 °C.

All the oscillators mentioned in this section used passive components that experienced large variations in quality factor with temperature. This work presents a High Temperature GaN HEMT VCO operating at 2.38 GHz with a tuning range of 66 MHz at 225 °C utilizing microstrip for the reactive elements. The above works are compared to the design presented in this work in Table 2-2.

Table 2-2 Comparison to past works

Parameter	[28]	[24]	[26]	[29]	This work
Temperature (°C)	25-200	25-250	30-200	25-230	**25-225**
Technology	SOS CMOS	GaN HEMT	SiC	GaN HEMT	**GaN HEMT**
Frequency (MHz)	300	58	1000	350	**2357**
Output Power (dBm)	4.9-2.2	11	21.8	18	**17.4**
Output power variation with T (%)	-	62.5	19	8.3	**15.2**
Tuning Range (MHz)	100	0	0	40	**66**
Power Dissipation (mW)	-	-	1010	127.5	**400**
Phase Noise @ 100 kHz (dBc)	-70	-120	-	-121	**-101**

Chapter 3

3 Proposed VCO Design

This chapter details the design process for the VCO presented in this work. The oscillator topology is a reflection-type negative resistance oscillator as seen in Figure 2-12. Device selection, sub-network identification and synthetization, and simulation results are shown in the following sections.

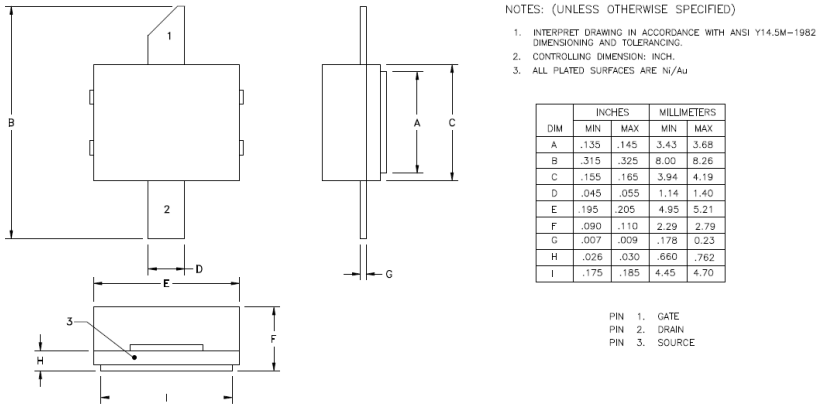
3.1 Device and Materials Selection

3.1.1 Active Device Selection

GaN offers a wide band gap, which was shown in Section 2.4 to be a critical parameter for high temperature designs, and a high electron mobility seen in Table 2-1 that makes GaN an ideal candidate for high temperature RF/Microwave circuits.

The VCO is designed using Commercial-off-the-shelf (COTS) transistors. The active device used for the design of the VCO is a 6W RF Power Transistor from Cree Wolfspeed part number CGH40006P [30]. It is a GaN HEMT device chosen due to its listed maximum operating junction temperature of 225 °C, frequency characteristics, and the availability of a nonlinear model. The listed max T_j can be extended with decreased lifetime. A picture of the device and its dimensions are shown in Figure 3-1 and Figure 3-2.

Figure 3-1 CGH40006P 6W, RF Power GaN HEMT Transistor [30] [fair use]



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.135	.145	3.43	3.68
B	.315	.325	8.00	8.26
C	.155	.165	3.94	4.19
D	.045	.055	1.14	1.40
E	.195	.205	4.95	5.21
F	.090	.110	2.29	2.79
G	.007	.009	.178	0.23
H	.026	.030	.660	.762
I	.175	.185	4.45	4.70

Figure 3-2 CGH40006P Dimensions [30] [fair use]

The varactor is constructed from the same transistor, but with the source and drain shorted thereby using the PN junction of the transistor as the tunable capacitance. This is done due to the lack of availability of high temperature varactors. The varactor will be discussed in more detail in Section 3.3.

3.1.2 Board Selection

The PCB material used for the design is 1.57 mm, 2 oz copper plated Rogers 4003C. Rogers 4003C offers a glass transition temperature $T_g > 280\ °C$, and negligible change in dielectric constant and board expansion making it ideal for high temperature circuits using microstrip lines [31].

3.1.3 Solder

Solder with a higher liquidous temperature than $250\ °C$ is requried. Indalloy 151 is used which is an alloy composed of 92.5 % Pb, 2.5 % Ag, and 5% Sn. The liquidous temperature is $296\ °C$, which is sufficient for the application target temperature.

3.2 Bias Network

A bias network sets the DC current through the device, and to a large degree it will set the average power dissipation. For high temperature designs it is critical to have a power dissipation that does not dramatically exceed the maximum junction temperature rating for the active device, as this will decrease the Mean Time To Failure (MTTF).

3.2.1 Bias Selection

The relationship between the device junction temperature, the ambient temperature, and the power dissipation can be linked using the *junction-to-ambient* thermal resistance θ_{JA} ($°C$/W) as shown below

$$T_j = P_{diss} + \theta_{JA} T_A \tag{3.1}$$

where P_{diss} is the dissipated power, T_j is the junction temperature, and T_A is the ambient temperature. The identification of the dominant heat flow path can be used to get an estimate for θ_{JA}. Referring to Figure 3-2, where the dimensions of the active device are shown, the device needs to be attached to the Rogers4003C substrate by the solder paste onto copper pads. The dominant heat flow path can be seen visually in Figure 3-3.

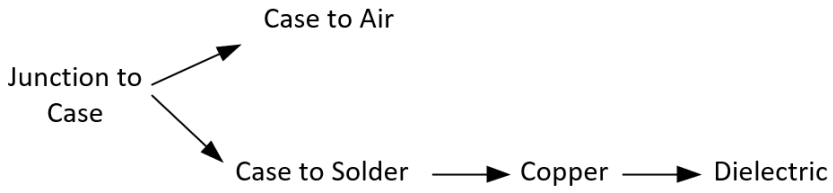


Figure 3-3 Heat flow path for calculating thermal resistance

By using the thermal conductivities of the materials [30-33], the thermal resistance representation can be synthesized as shown in Figure 3-4.

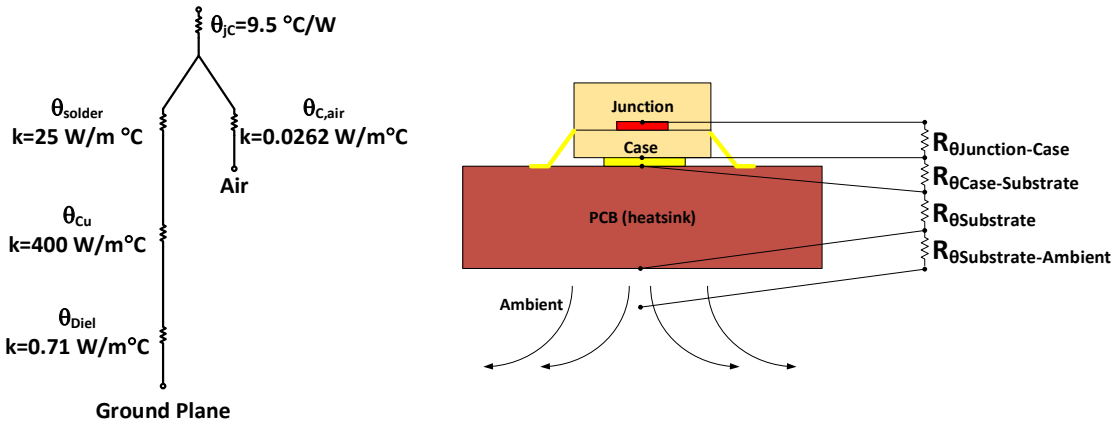


Figure 3-4 Thermal resistance representation of heat flow path

The dimensions to determine h and A for each part of the chain and therefore the thermal resistance is as follows:

- Transistor to Solder/Cu/Substrate area: 3.5 mm x 4.6 mm
- Copper thickness: 35 μm
- Solder thickness estimate: 35 μm
- PCB thickness: 1.57 mm
- Transistor to air has five sides
    - Top: 4 mm x 5.1 mm
    - 1st pair of sides: 2.5 mm x 5.1 mm
    - 2nd pair of sides: 2.5 mm x 4 mm

The thermal resistances can then be calculated:

$$\theta_{Solder} = \left(\frac{35\mu m}{3.5mm\ x\ 4.6\ mm}\right)\left(\frac{1}{\frac{25W}{m°C}}\right) = 0.087\ °C/W \tag{3.2}$$

$$\theta_{Cu} = \left(\frac{35\mu m}{3.5mm\ x\ 4.6\ mm}\right)\left(\frac{1}{\frac{400W}{m°C}}\right) = 0.0054\ °C/W \tag{3.3}$$

$$\theta_{diel} = \left(\frac{1.57mm}{3.5mm\ x\ 4.6mm}\right)\left(\frac{1}{\frac{0.71W}{m°C}}\right) = 137.35\ °C/W \tag{3.4}$$

$$\theta_{C,air} = \left(\frac{2.5mm}{4mm\ x\ 5.1mm}\right)\left(\frac{1}{\frac{0.0262W}{m°C}}\right) = 4655\ °C/W \tag{3.5}$$

From Eq. 3.2-5, θ_{JA} can be calculated as

$$\theta_{JA} = \theta_{JC} + (\theta_{C,air}||(\theta_{diel} + \theta_{Cu} + \theta_{solder})) = 143.1\ °C/W \tag{3.6}$$

And then by rearranging Eq. 3.1, the maximum power dissipation for a junction temperature of 275 $°C$, and an ambient temperature of 225 $°C$ is

$$P_{Max} = \frac{T_j - T_A}{\theta_{JA}} = \frac{275 - 225}{143.1} = 0.35\ W \tag{3.7}$$

Based on this estimate for the maximum power dissipation, a bias point can be chosen for the VCO.

Using the non-linear model provided by Cree Wolfspeed for the CGH4000P transistor, the I-V curves can be plotted using Advanced Design System (ADS). A schematic of the testbench for the sweep is shown in Figure 3-5.

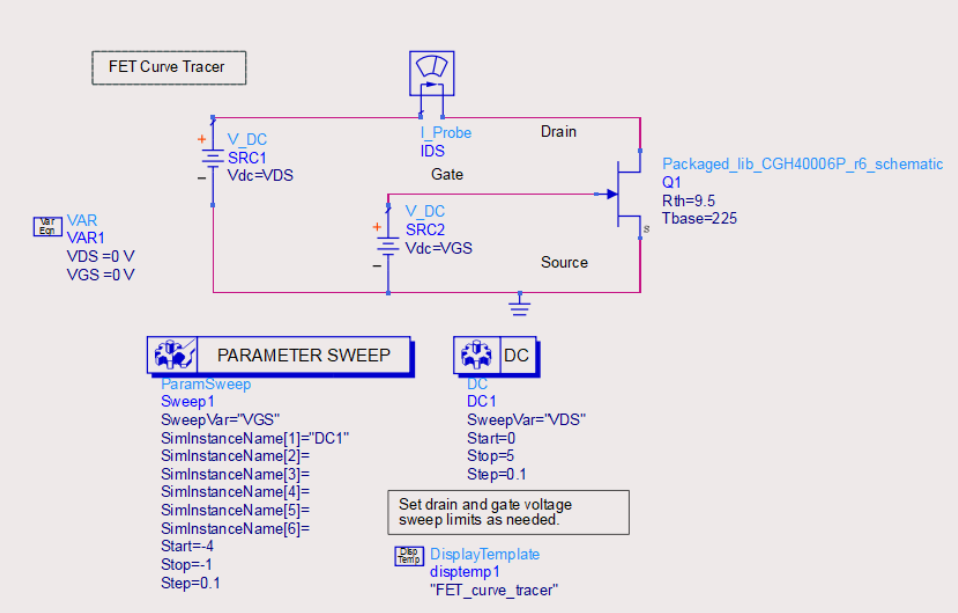


Figure 3-5 DC I-V curve tracer testbench

The model has a self-heating variable shown as Tbase in the schematic of Figure 3-5. By setting Tbase equal to the maximum ambient temperature the model will account for the change in current with temperature. A plot of the I-V curves for testbench of Figure 3-5 is shown in Figure 3-6. The bias point is initially chosen as $V_{GS} = -2.5\ V$, and $V_{DS} = 2.5\ V$ for a conservative DC power dissipation of 0.233 W based on Eq. 3.7.

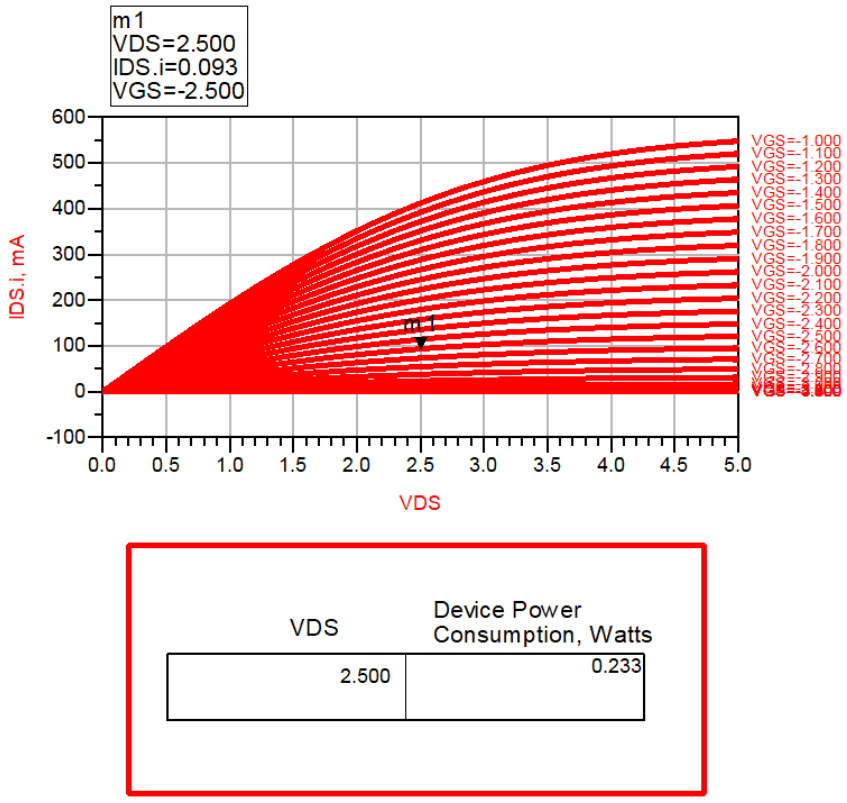


Figure 3-6 I-V curves for CGH4000P transistor model

3.2.2 RF Choke

To keep the RF power out of the DC supply a RF Choke needs to be used. From a qualitative standpoint the choke needs to look like a short circuit at DC and a high impedance path at RF. The most obvious solution is to use an inductor. However, at microwave frequencies inductors are difficult to realize because they start to resonant with their parasitic capacitance. Therefore, instead of using an inductor, quarter-wave transmission lines can be used to realize a large impedance at the frequency of interest.

As was mentioned in Section 2.1.3, a short-circuited quarter-wave transmission line appears as an open circuit at the frequency of interest and vice-versa for an open-circuit transmission line. By using two quarter-wave transmission lines an RF choke can be

realized as seen in Figure 3-7. Normally, the first quarter-wave line at the RF-Port is a high-characteristic impedance line, and the shunt quarter-wave line is a low-characteristic impedance line.

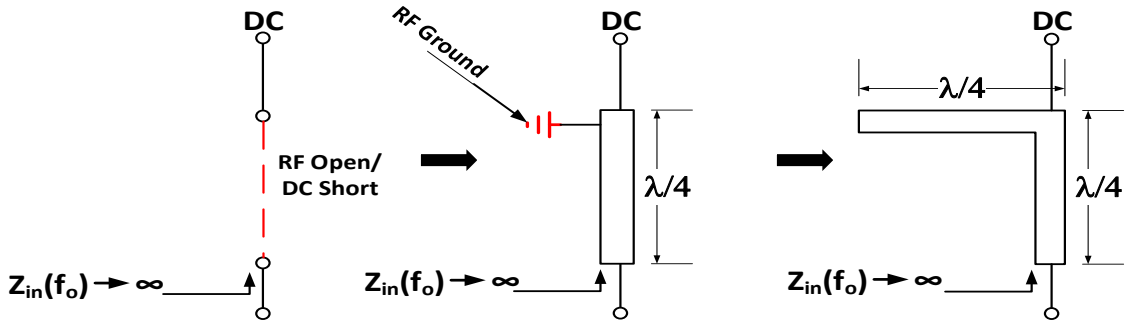


Figure 3-7 RF Choke with transmission lines

To determine the dimensions of the lines needed, the LineCalc tool in ADS is used. At 2.4 GHz, on the Rogers 4003C substrate, a $\lambda/4$ line is 19.57 mm. A line width of 3.5 mm is used for the low characteristic impedance line, and a line width of 1 mm is used for the high characteristic impedance line. After accounting for the discontinuities between the lines with the MTEE object in ADS, the length is varied until the performance is optimized for 2.4 GHz. The length for the lines then becomes 17.34 mm after tuning. The testbench for this is shown in Figure 3-8, the corresponding frequency response is shown in Figure 3-9

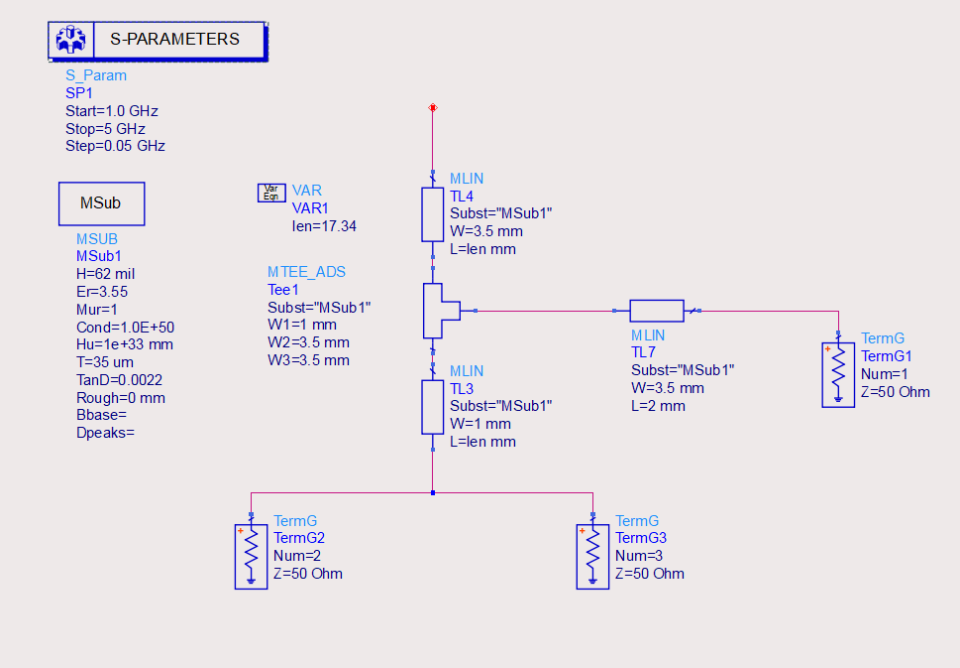


Figure 3-8 Testbench for RF Choke

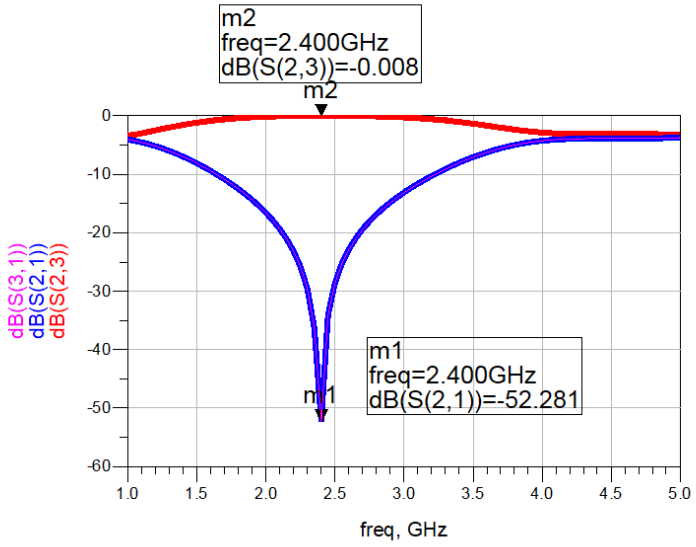


Figure 3-9 Frequency response of RF Choke

The schematic in Figure 3-8 and the corresponding results in Figure 3-9 are from approximate models. A more accurate response can be obtained through Electromagnetic

(EM) simulations. ADS momentum uses the Method-of-Moments to solve for the fields in planar structures. A layout of the RF Choke is shown in Figure 3-10.

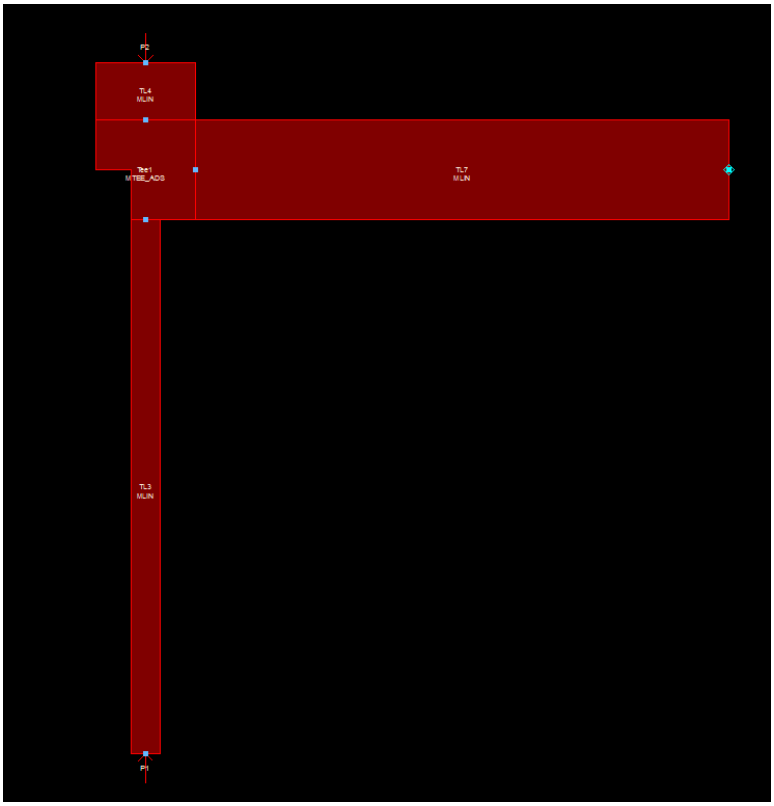


Figure 3-10 Layout of RF Choke

The EM simulated results will provide a more accurate solution. The transmission coefficient of the EM simulated layout is plotted on the same plot as the transmission coefficient from the schematic simulation in Figure 3-11. There is a difference of around 7 dB between the nulls, with a 22 MHz difference in the location of the nulls.

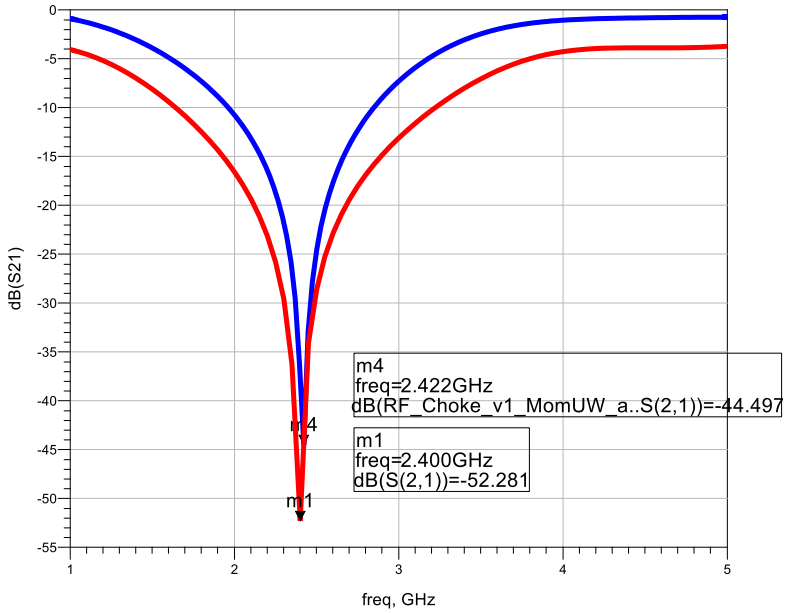


Figure 3-11 EM simulated response (blue) overlaid on schematic response (red)

3.3 Varactor

To the best of the author's knowledge there are no commercial available varactors that are rated over 175 $°C$ operating temperature. The decision was then made to utilize the Schottky diode inherit in a GaN HEMT transistor. This can be done by connecting the drain and the source together. The gate contact is then the anode, and the source/drain contact is the cathode. By applying a reverse bias voltage, a change in capacitance can be observed. The testbench is shown in Figure 3-12, where the source and drain are connected to ground and a one port simulation is ran by sweeping the tuning voltage from -30 to -2 V at 2.4 GHz. DC_Block and DC_Feed components are used to isolate the measurement port from the DC Source.

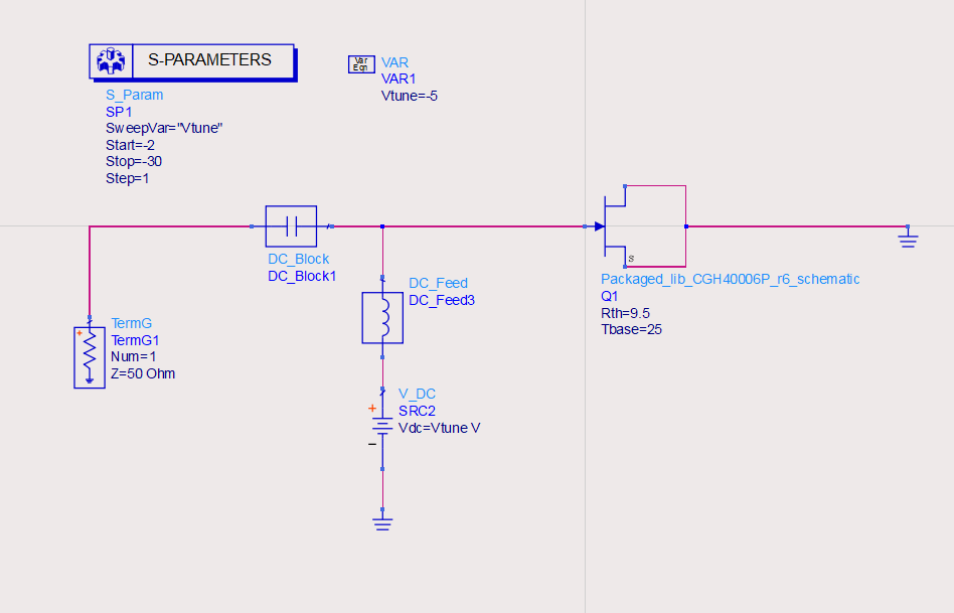


Figure 3-12 Testbench for varactor

From the one-port admittance (Y) parameters the capacitance can be calculated as

$$C = \frac{imag(Y_{11})}{2\pi f} \tag{3.8}$$

The quality factor can be calculated as

$$Q = \frac{imag(Y_{11})}{real(Y_{11})} \tag{3.9}$$

The results of the simulation are shown in Figure 3-13, where at a reverse bias voltage of -4V the Q drops very quickly due to the forward biasing of the transistor. This sets the usable tuning voltage range from -30 V – limited by the DC power supply – to -4 V.

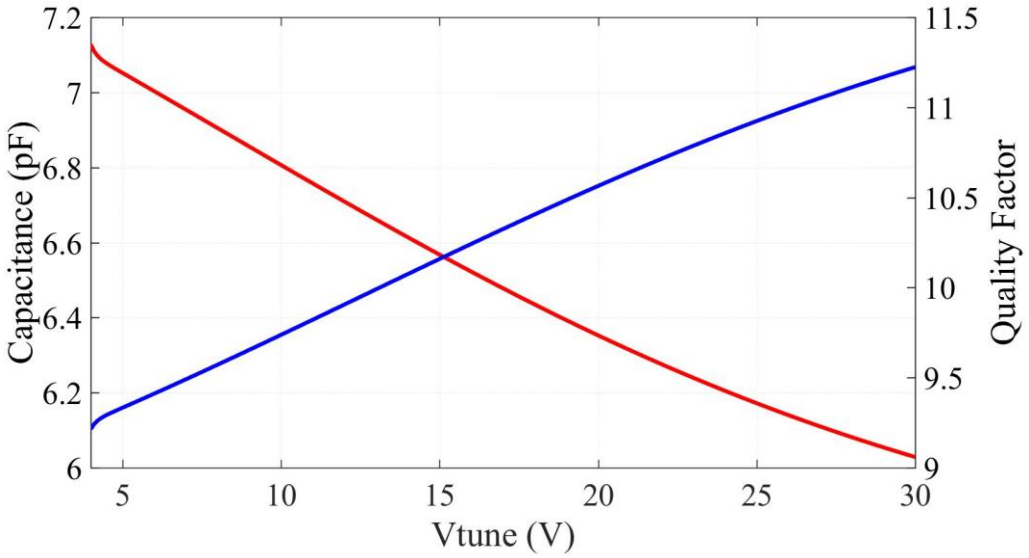


Figure 3-13 Capacitance (red) and Quality Factor (blue) versus reverse bias voltage (Vtune)

3.4 Series Feedback Network

As was mentioned in Section 2.3, negative resistance oscillators require unstable transistors. To ensure this instability, a common-gate topology with series feedback is used. In Section 2.1.2 the Rollet stability factor k was introduced. The smaller k gets, in general, the more unstable the device is. To determine a value for the series feedback, an inductor is placed on the gate, and the value of the inductance is swept to determine the minimum value of k. A testbench for this is shown in Figure 3-14 where the RF_Choke components are the chokes from Section 3.2.2.

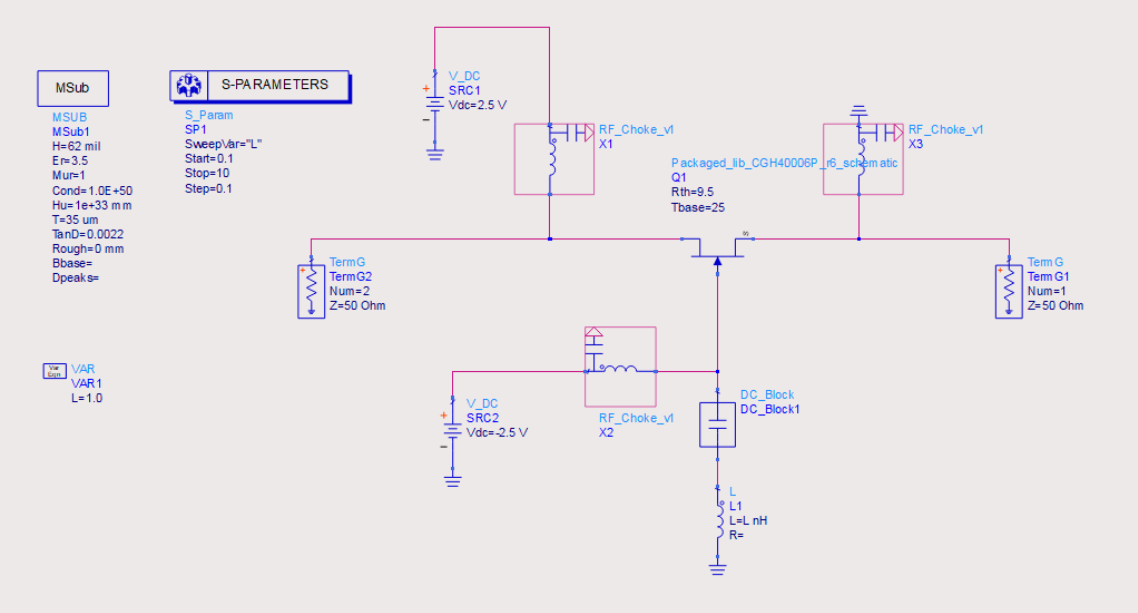


Figure 3-14 Testbench for series feedback

The results of the simulation from Figure 3-14 are shown in Figure 3-15. A value of L = 0.8 nH is shown to give the minimum value of k.

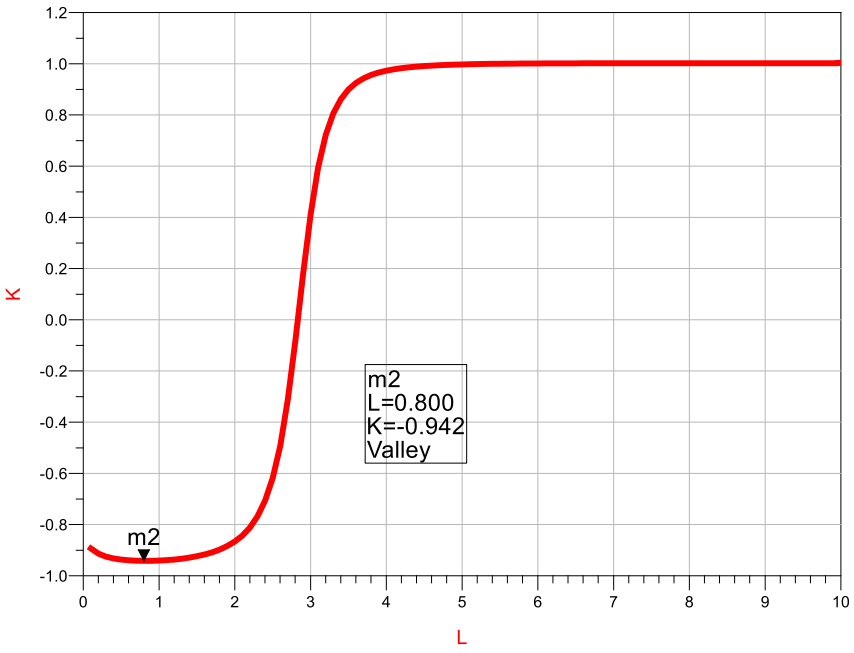


Figure 3-15 Rollet stability factor plotted versus feedback inductance

The inductor can be realized as the varactor in series with an open-circuit transmission line. The length of the transmission line can then be varied until the overall impedance equals that of the 0.8 nH inductor. The test bench for this is shown in Figure 3-16. Two one port circuits are being simulated: the one of the left is the varactor with an open circuit transmission line in series, the one on the right is the 0.8 nH inductor. The transmission line width is set to 3.48 mm, because this corresponds to a 50 Ω characteristic impedance for this substrate. The length is swept, and the reflection coefficient is converted to an impedance from Eq. 2.1.

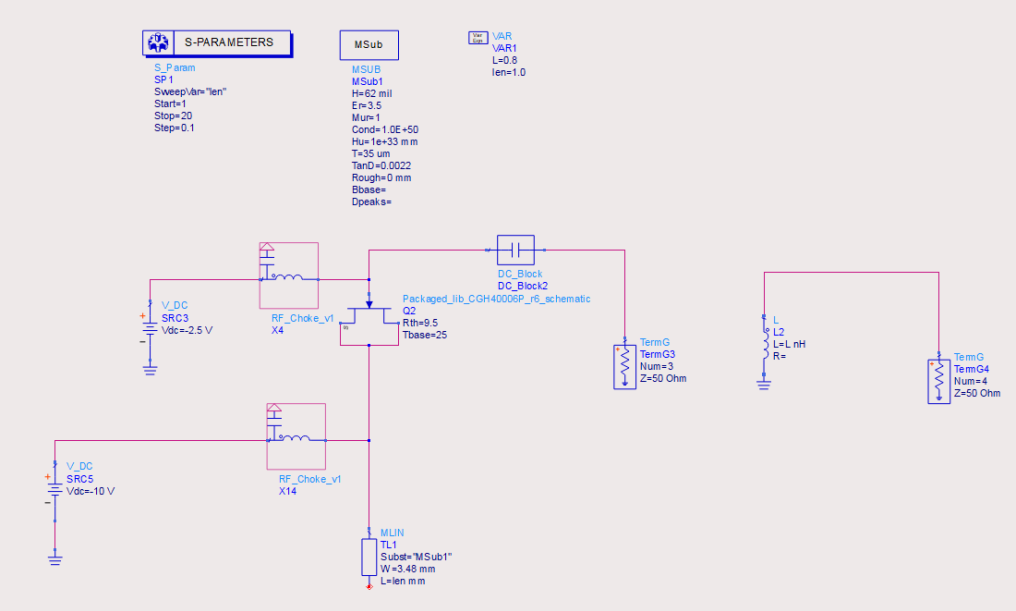


Figure 3-16 Testbench for tunable series feedback

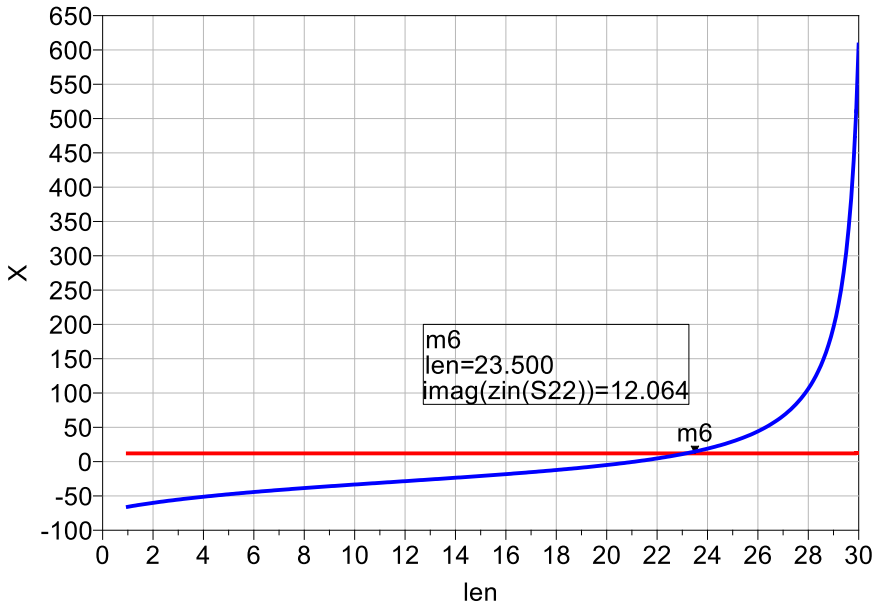


Figure 3-17 Reactance for varactor in series with open-circuit transmission line (blue) and 0.8 nH inductor (red)

It can be seen from Figure 3-17 that a length of 23.5 mm for the open-circuit transmission line gives the same reactance as the 0.8 nH inductor.

3.5 Load and Terminating Network

The topology shown in Figure 2-12 is modified to include the series feedback network -- which consists of an open-circuit transmission line and the varactor -- and is shown in Figure 3-18. As was mentioned in the previous section, this topology is a common-gate with series feedback. The terminating network needs to be chosen to present a negative resistance at the input port (real(Z_{in})<0), and then the load network needs to satisfy the conditions in Eq. 2.46 to oscillate at steady-state. Eq. 2.46 is repeated here for convenience as Eq. 3.10.

$$Z_L + Z_{in} = 0 \qquad (3.10)$$

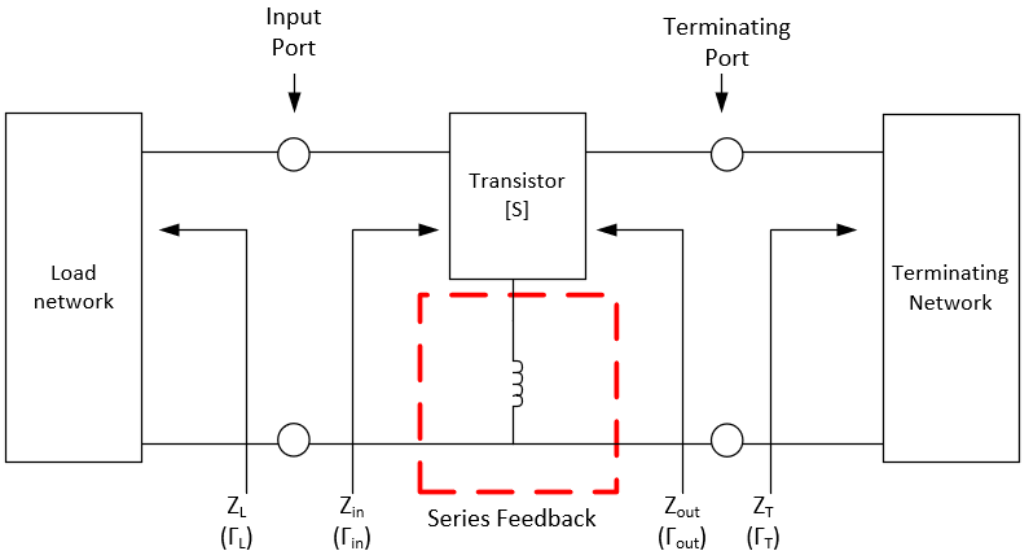


Figure 3-18 Negative resistance oscillator with feedback

3.5.1 Terminating Network

The terminating network has some restrictions for this application, in that this is an attempt at making an oscillator using only microstrip for its passive components. For this reason, the terminating network must be purely reactive. The terminating network can be on either the drain or the source of the device, however it was determined through iteration that a purely reactive terminating network on the source does not present as large of a negative resistance at the other port. Therefore, the terminating network is to be placed on the drain. For ease of implementation, this will be implemented as an open-circuit transmission line.

A sweep of the length of an open-circuit transmission line on the drain can be performed as shown in Figure 3-19, where the RGnd component is a large resistor to

ground to provide a DC path to ground for the simulator and is not a representation of an actual component that will be placed in the final layout.

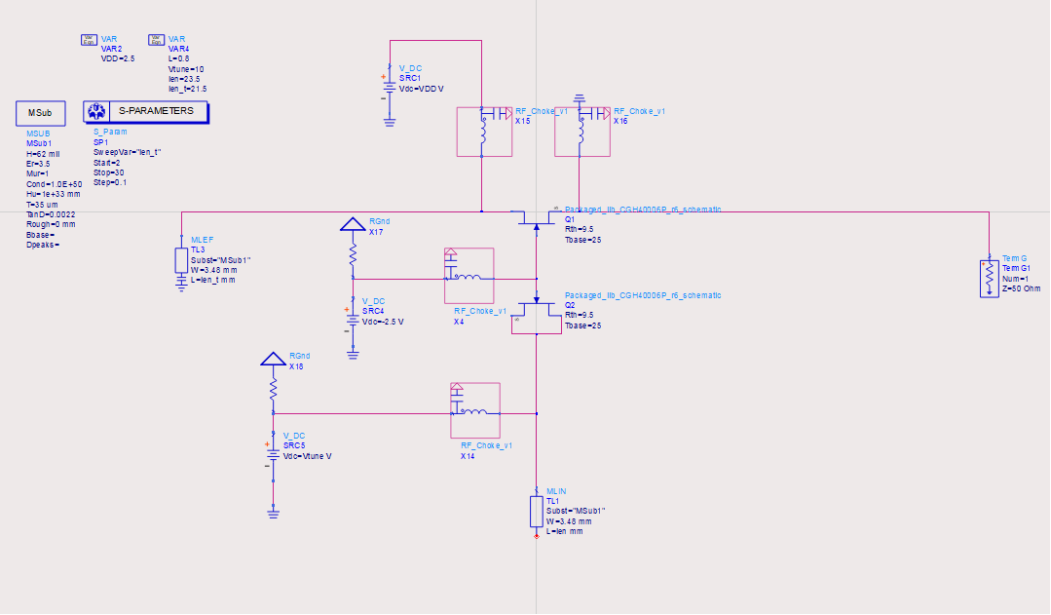


Figure 3-19 Testbench for determining Terminating Network

The resistance and reactance looking into the source is plotted versus the length of the open-circuit line on the drain in Figure 3-20. Looking at the plot, the impedance begins to change in a non-linear fashion after around 19 mm. This is because the impedance of a transmission line a function of the tangent of the length, meaning it changes quickly around a quarter-wavelength. A length of 18 mm is chosen initially as a compromise between ensuring there is enough negative resistance, but also not ensuring that the impedance does not have a steep slope with regards to the transmission line length.

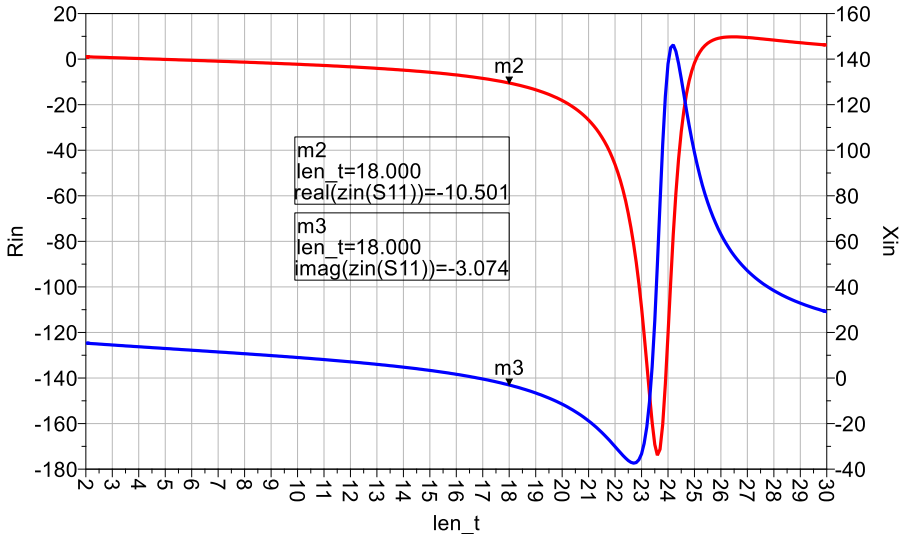


Figure 3-20 Input impedance looking into the source of the transistor vs. length of open-circuit transmission line on drain

3.5.2 Load Matching Network

The impedance shown in Figure 3-20 is the input impedance for small-signal oscillations i.e. this is the impedance being presented during the start-up regime. A more accurate measure of the input impedance can be done through load-line analysis, where a large signal is applied at the input port and the impedance is measured by taking the ratio of the voltage to current at that port. A schematic to determine the large signal input impedance is shown in Figure 3-21, where the input power is swept from 0 to 30 dBm and the current and voltage are measured to calculate the input impedance.

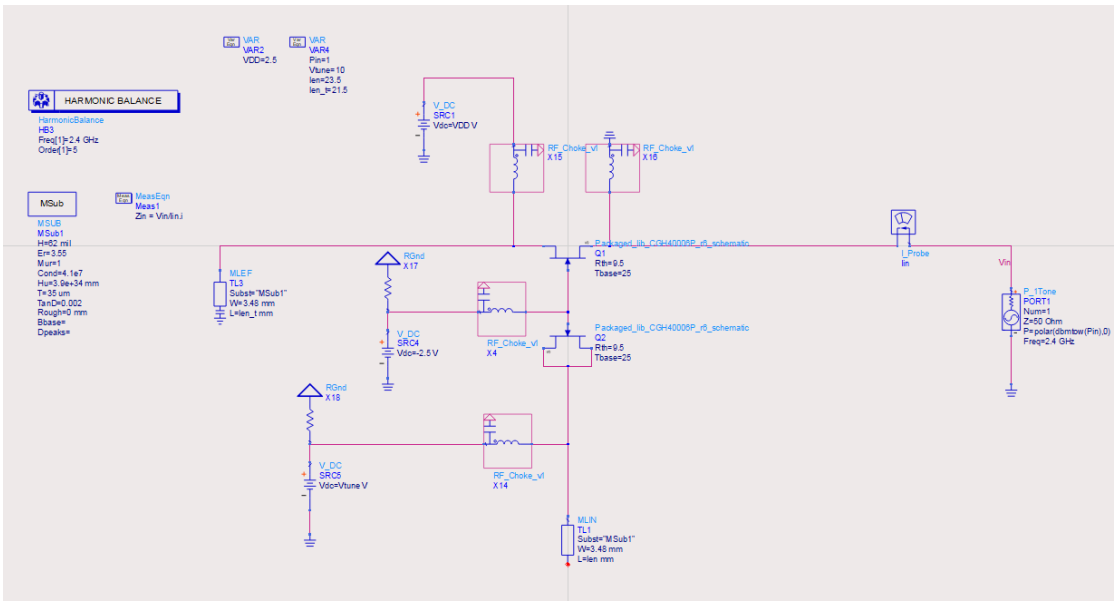


Figure 3-21 Testbench for determining large signal input impedance

The input impedance is shown in Figure 3-22, where it can be seen around 14.5 dBm the impedance starts to change rapidly due to the change in device impedances under large input power.

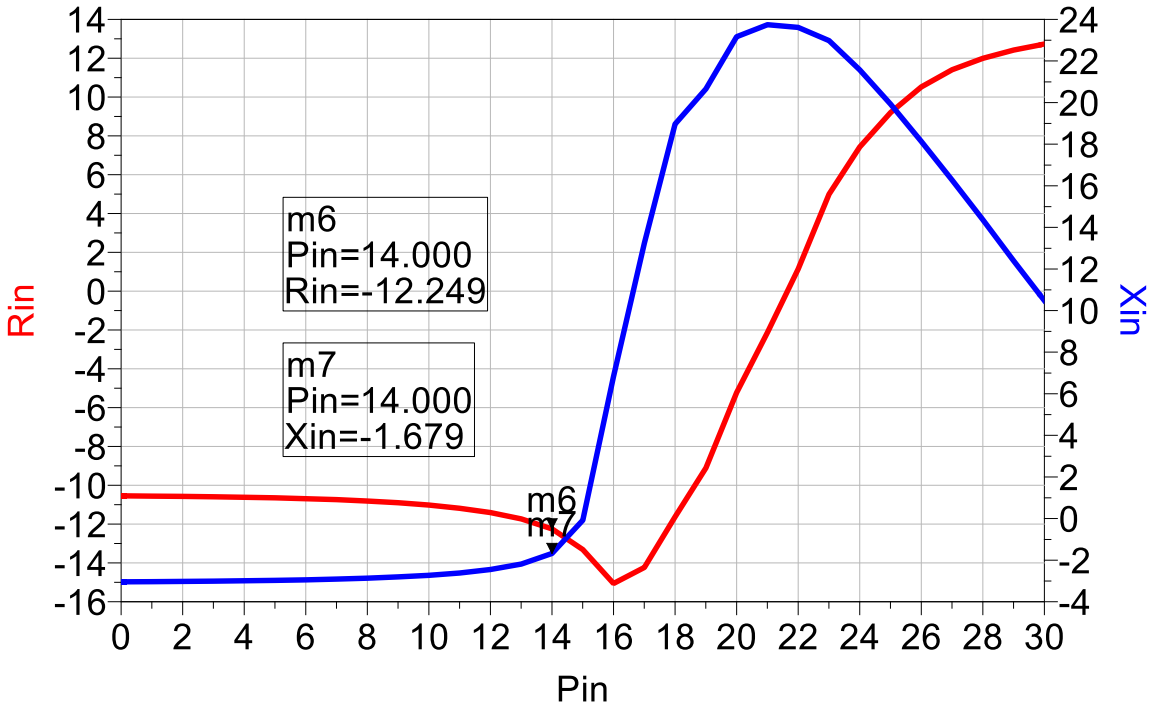


Figure 3-22 Input impedance for power-sweep

From Figure 3-22 for an input power of 14 dBm the input impedance is $Z_{in} = -12.2 - j1.68$. A matching network can then be synthesized to satisfy Eq. 3.10.

The matching network can be synthesized by using the Smith Chart. The Smith Chart is a polar mapping of the voltage reflection coefficient, where normalized constant resistance and reactance circles are overlaid on one another. More information on the mathematical principles behind the Smith Chart can be found in [34]. Normalizing in the input impedance gives

$$z_{in} = \frac{Z_{in}}{Z_o} = -0.244 - j0.0336 \tag{3.11}$$

And therefore, the matching network must present a normalized impedance of

$$z_L = 0.244 + j0.0336 \qquad (3.12)$$

which can be plotted on the Smith Chart. A series stub is then added to rotate z_L to the G=1 constant conductance circle, shown by point B in Figure 3-24. A shunt open-circuit stub is then used to rotate from point B to the center of the Smith Chart. The electrical lengths of the lines are read from the Smith Chart and are 24.24° for the series stub and 57.23° for the shunt open-circuit stub.

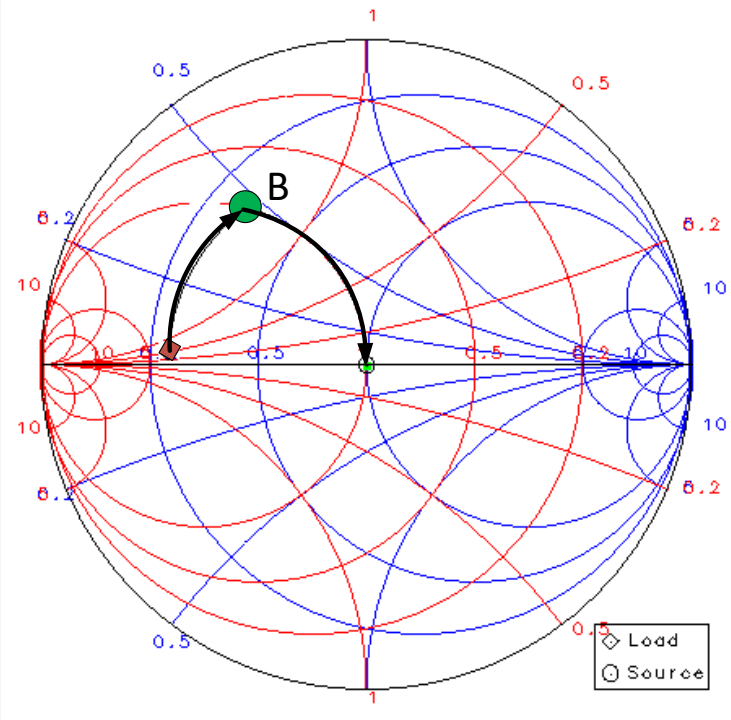


Figure 3-23 Single-stub matching on Smith Chart

The single-stub matching network is shown in Figure 3-24 with the lengths calculated using the LineCalc tool to convert from electrical length to mm, and then the tuning tool is used to further refine the match. A one-port s-parameter simulation is performed to determine the impedance looking into the matching network with a 50 Ω load.

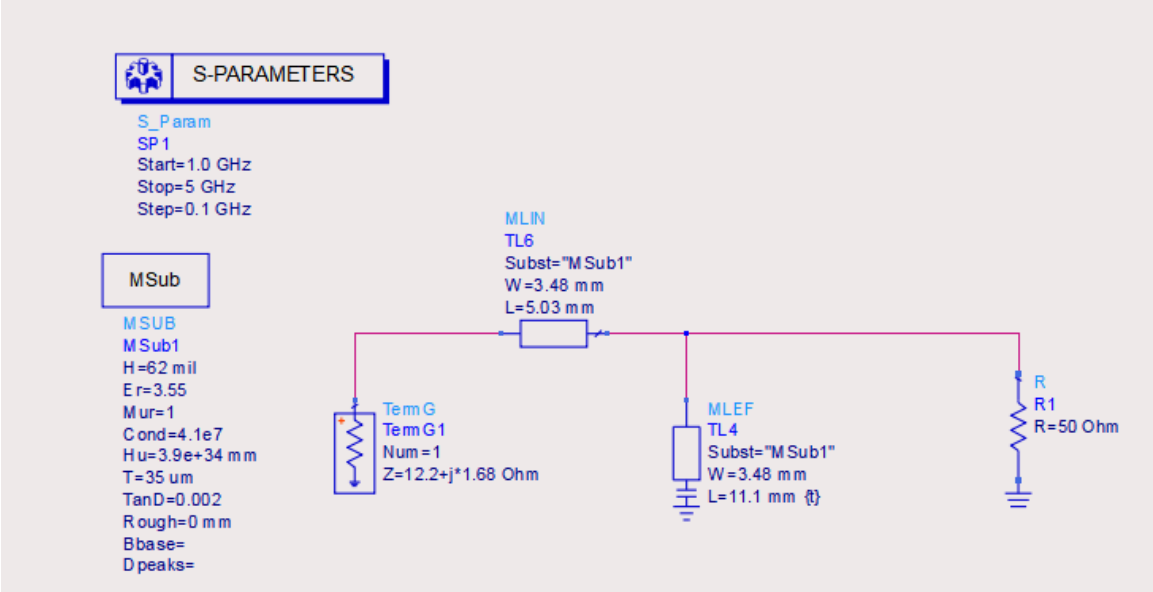


Figure 3-24 Single-stub matching network

The results of the match are shown in Figure 3-25, where the network shows a close match at 2.4 GHz, which is the design frequency.

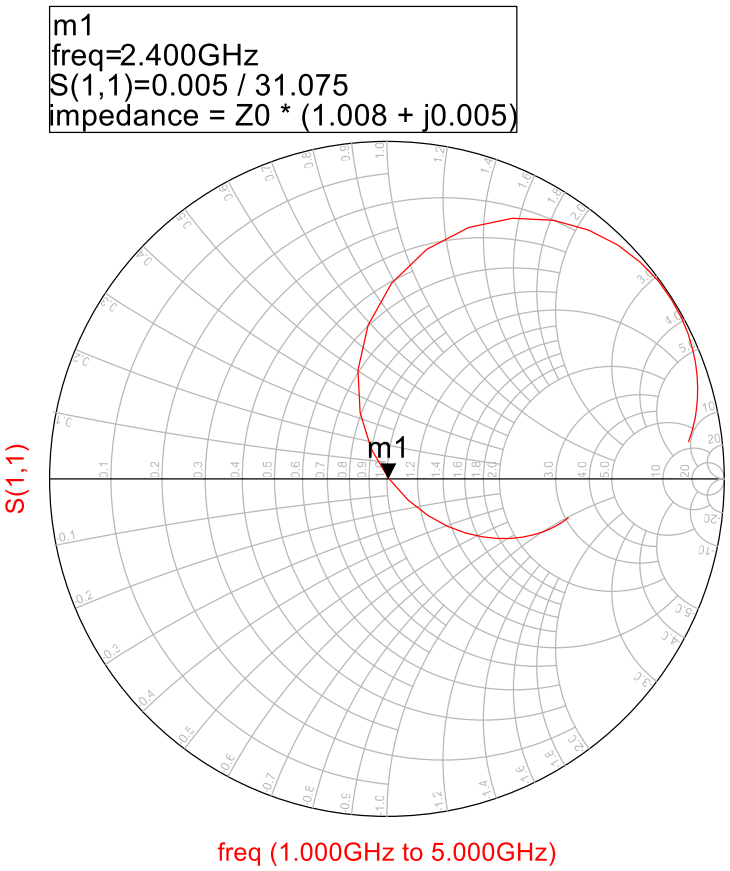


Figure 3-25 Results of single-stub matching, showing a match at 2.4 GHz

3.6 Final Schematic

Combining the pieces from the previous sections, a full schematic of the VCO is shown in Figure 3-26, with the relevant blocks from the previous sections labeled.

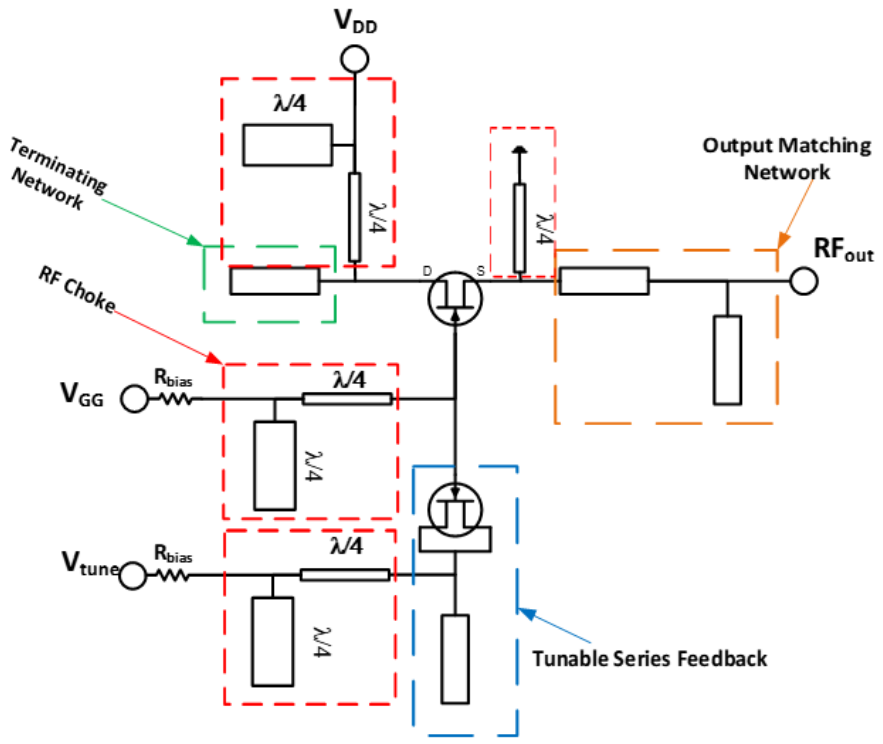


Figure 3-26 Schematic of VCO

A testbench schematic with the OscTest component placed in the loop to measure the loop-gain to determine whether the circuit will oscillate is shown in Figure 3-27.

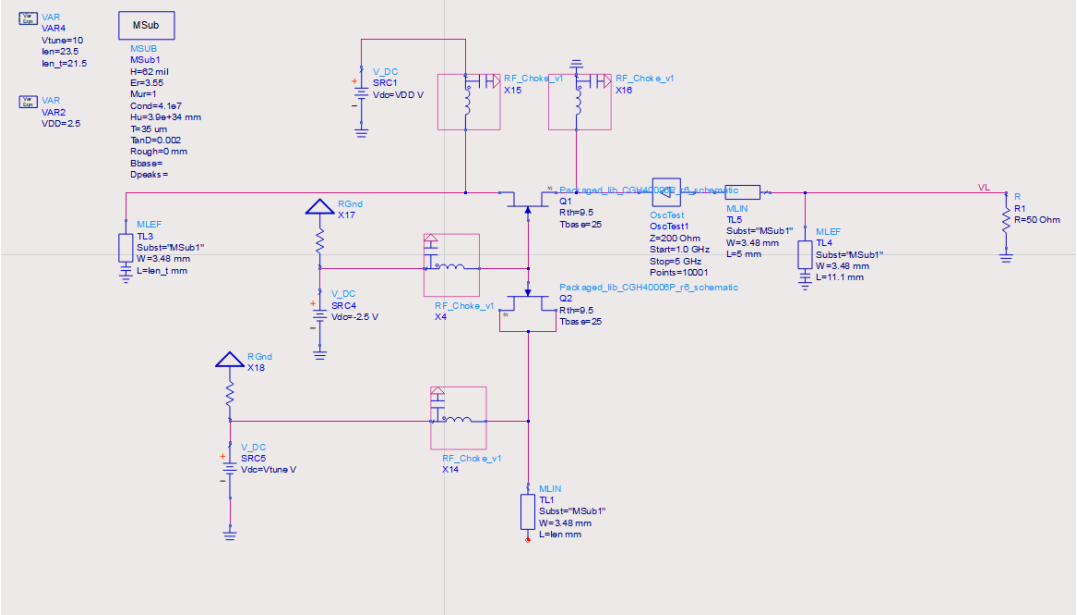


Figure 3-27 Schematic to test whether the circuit will oscillate

The polar plot of S(1,1) – which is the loop gain -- is shown in Figure 3-28. The circuit will oscillate if there is a zero-phase crossing with a loop gain > 1. It can be seen from Figure 3-28, that this is case where there is a loop gain of approximately 6.4 for a phase of zero.

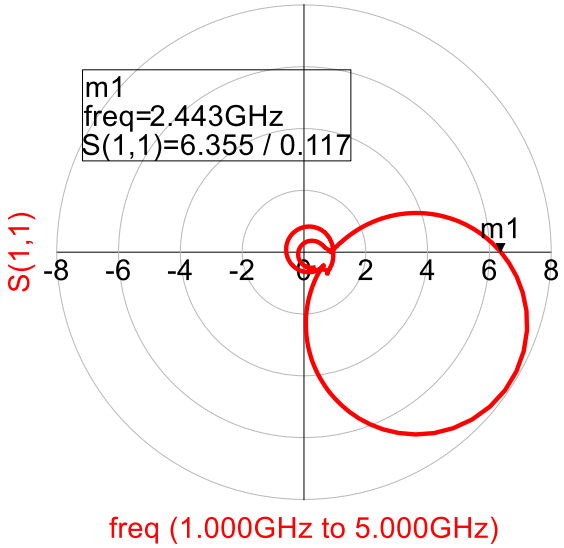


Figure 3-28 Polar Plot of loop gain

The OscTest component is used to determine if the circuit will oscillate, however it is a small-signal measure of the oscillation frequency. A Harmonic Balance simulation, which is a non-linear simulation will be able to more accurately predict the output power and oscillation frequency. The results for the output power versus tuning voltage of the Harmonic Balance simulation using the OscPort component are shown in Figure 3-29, where the fundamental output power is shown on the same plot as the 2nd and 3rd harmonics.

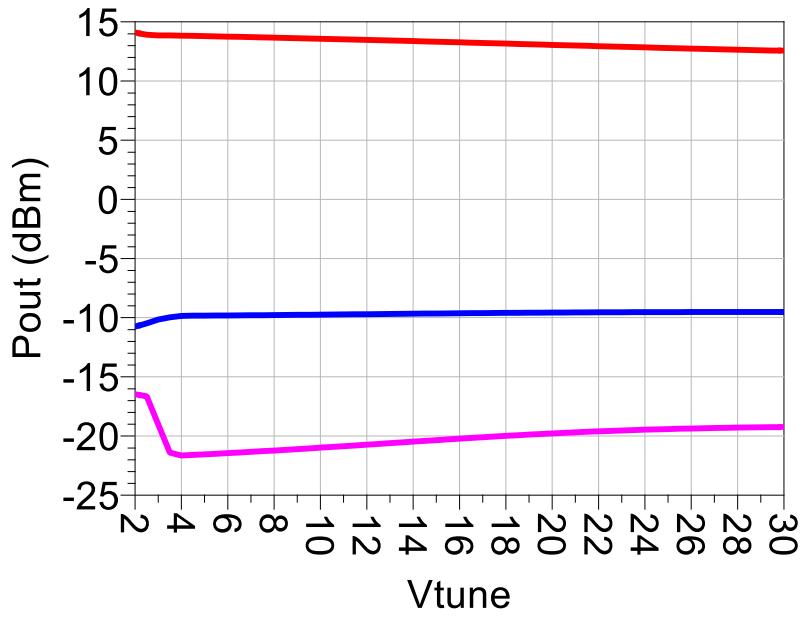


Figure 3-29 Output power versus tuning voltage. Fundamental (red), 2nd Harmonic (blue), 3rd Harmonic (purple)

The oscillation frequency versus the tuning voltage is shown in Figure 3-30. The tuning range is small – only 7 MHz. Tuning the terminating network or series feedback can extend the tuning range.

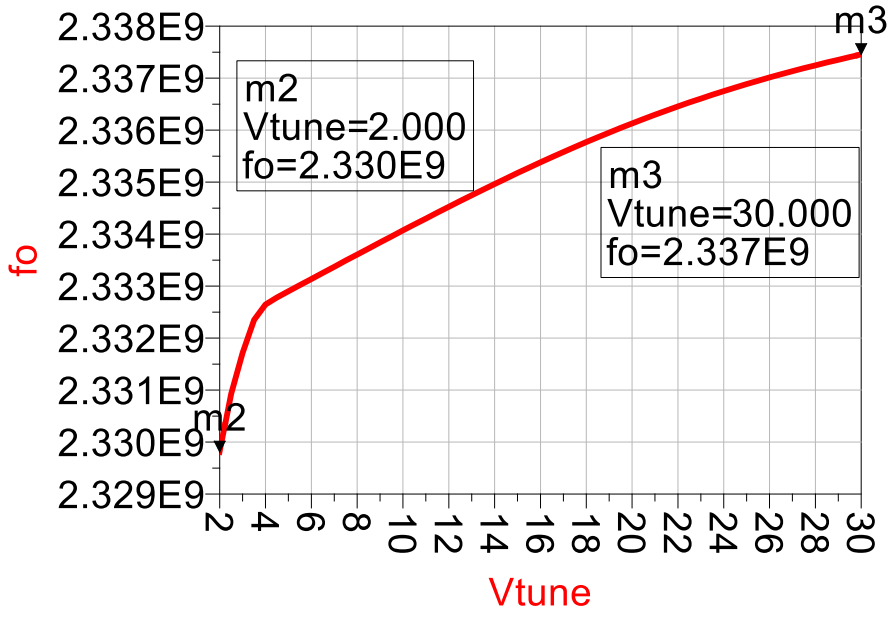


Figure 3-30 Output frequency vs. tuning voltage

After accounting for the discontinuities of transmission line junction using MTEE and MTAPER components, as well as replacing the GND symbol with a model of a via to ground, and tuning the terminating network and series network the final schematic is shown in Figure 3-31.

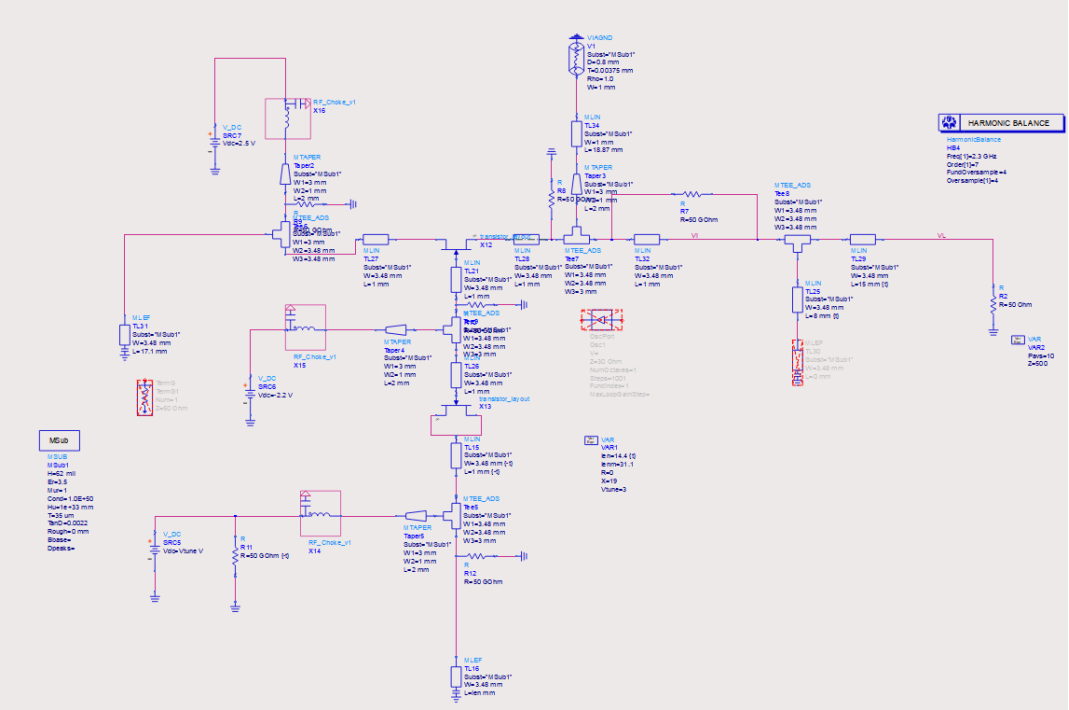


Figure 3-31 Final schematic of VCO

The output power versus tuning voltage and oscillation frequency versus tuning voltage is shown in Figure 3-32 and Figure 3-33 respectively. The output power ranges from 15.7 dBm to 16.53 dBm. The frequency range is from 2.374 GHz to 2.424 GHz.

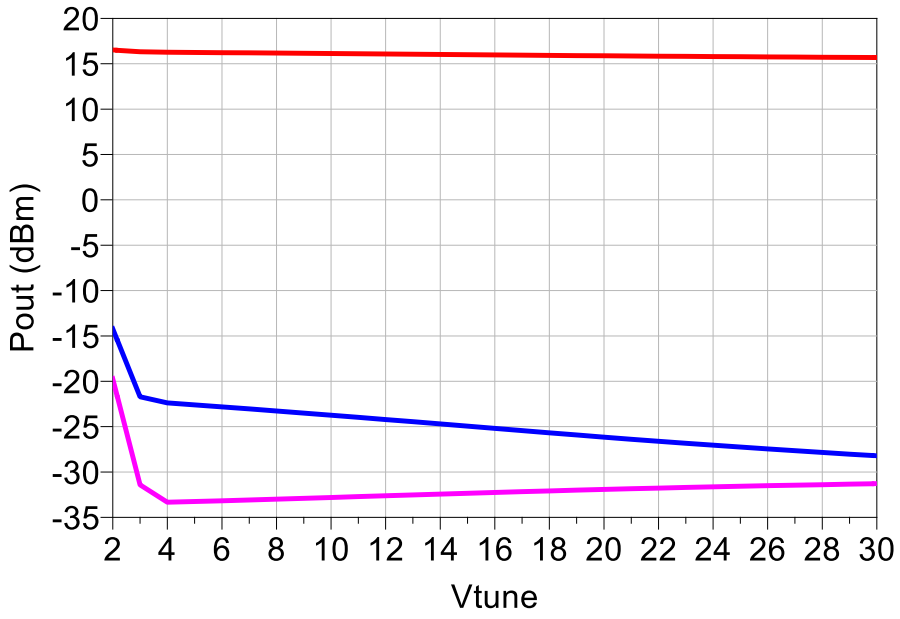


Figure 3-32 Output power versus tuning voltage. Fundamental (red), 2nd Harmonic (blue), 3rd Harmonic (purple)

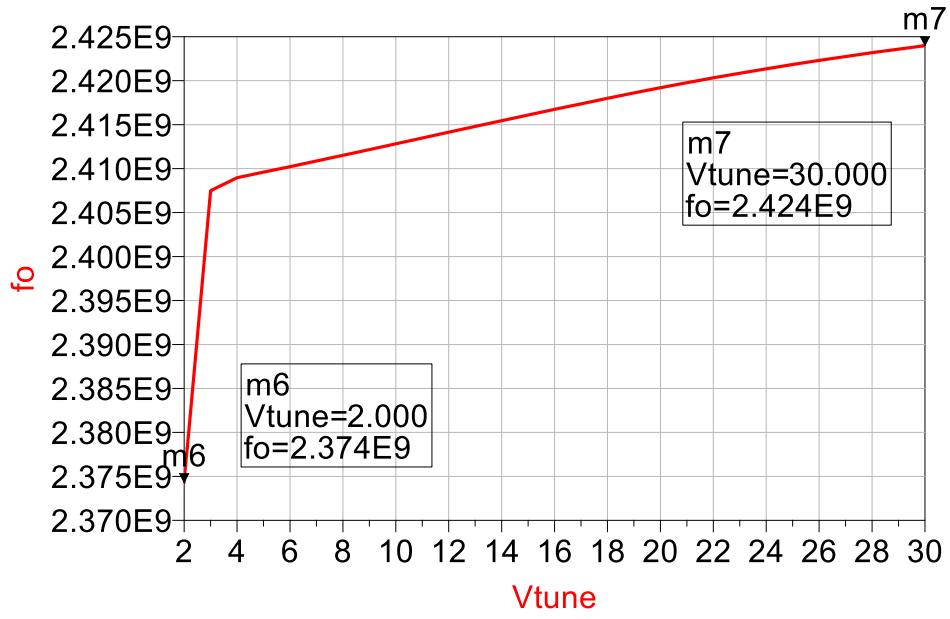


Figure 3-33 Oscillation frequency versus tuning voltage

3.7 Final Layout

The simulation results from Seciton 3.6 are a good estimate of the behavior, however a fully EM simulated layout is needed to further refine the design. After

iteration on transmission line lengths, the final layout for manufacturing is shown in Figure 3-34. There are additional stubs unconnected to the transmission lines to enable lengthening of the lines after manufacturing – lines can be shorted by using a knife to trim off length.

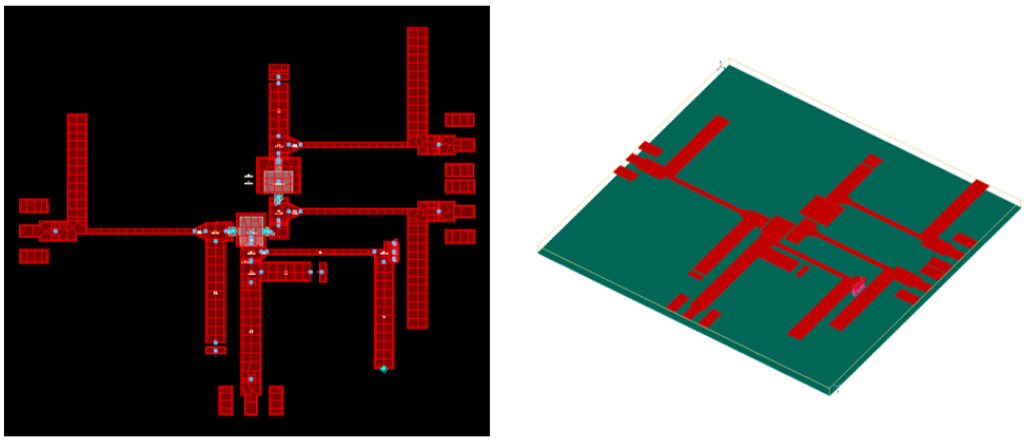


Figure 3-34 Layout view: (a) Planar (b) 3-D

3.8 Manufactured Board

A photograph of the manufactured board with soldered parts and port labels is shown in Figure 3-35. The board dimensions are 7.9 cm x 7.2 cm.

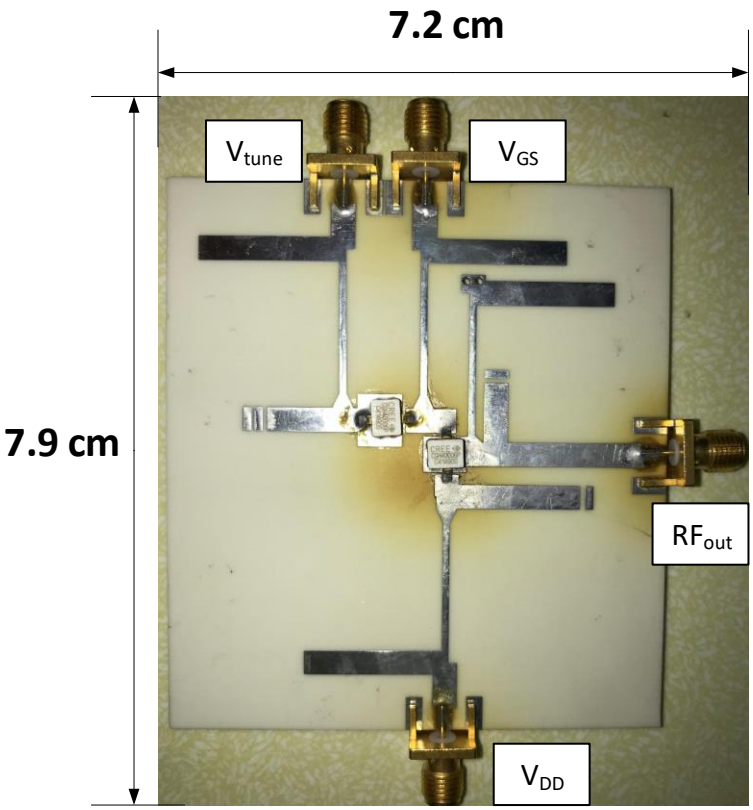


Figure 3-35 VCO Printed Circuit Board with ports labeled

Chapter 4

4 Measured Results

This chapter discusses the setup and results of measurements on output power, tuning range, and phase noise across a temperature range of $25°C$-$225°C$ for the VCO discussed in Chapter 3. The measurement setup along with a description of the associated instruments is discussed first. The results are discussed next and a comparison of these results is shown in a table at the end.

4.1 Measurement Setup

The measurement setup consists of a spectrum analyzer, a DC supply, and an oven. The oven is used to control the ambient temperature of the board. A visual representation of this is shown in Figure 4-1. The DC Supply supplies power to the drain and gate of the active device as well as control the tuning voltage on the varactors. The spectrum analyzer is used to measure the output power, frequency, and phase noise of the oscillator.

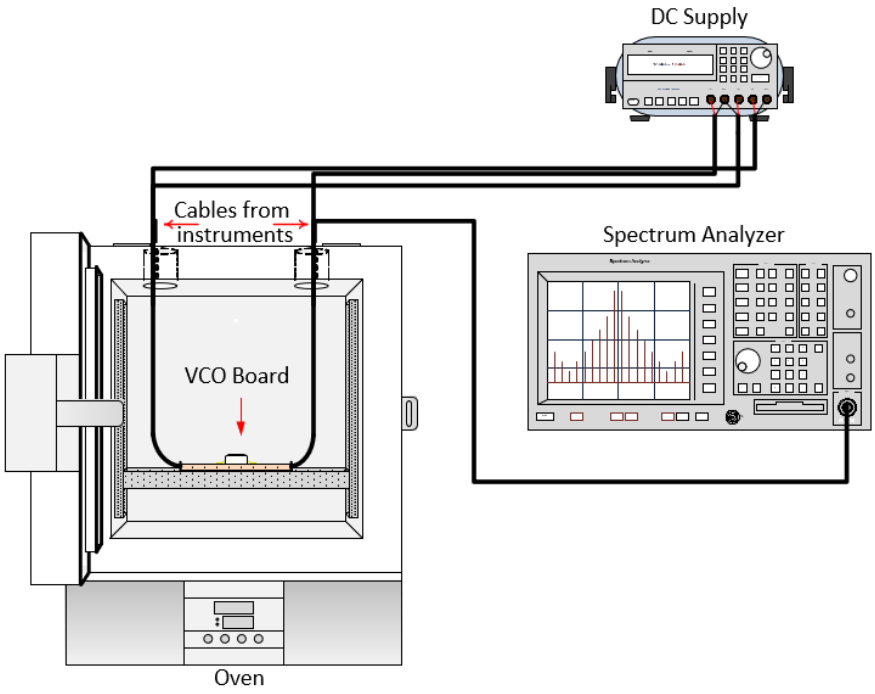


Figure 4-1 Measurement Setup

4.1.1 Instruments

4.1.1.1 Spectrum Analyzer

The spectrum analyzer used for the measurements is a Rohde and Schwarz FSW Signal and Spectrum Analyzer. It can measure signals up to 67 GHz, and has a SSB phase noise of <-145 dBc/Hz at 1 MHz offset which is well below the expected phase noise of the VCO presented in this work [35].

Figure 4-2 R&S FSW Signal and Spectrum Analyzer [36] [fair use]

4.1.1.2 Power Supply

A Rigol DP832A Programmable DC Power Supply is used to supply to gate and drain bias and the tuning voltage to the VCO board. The power supply has three channels. CH1 and CH2 can operate up to 30V and 3A. CH3 can operate up to 5V and 3A [37]. CH2 and CH3 are not isolated, therefore the voltages need to share the same polarity. CH2 was used for the tuning voltage and CH3 was used for the drain bias because they are both positive voltages. There is no negative voltage generator, so the positive lead for the gate bias is plugged into the negative terminal of CH1, and the negative lead is plugged into the positive terminal of CH1 to ensure a negative voltage.

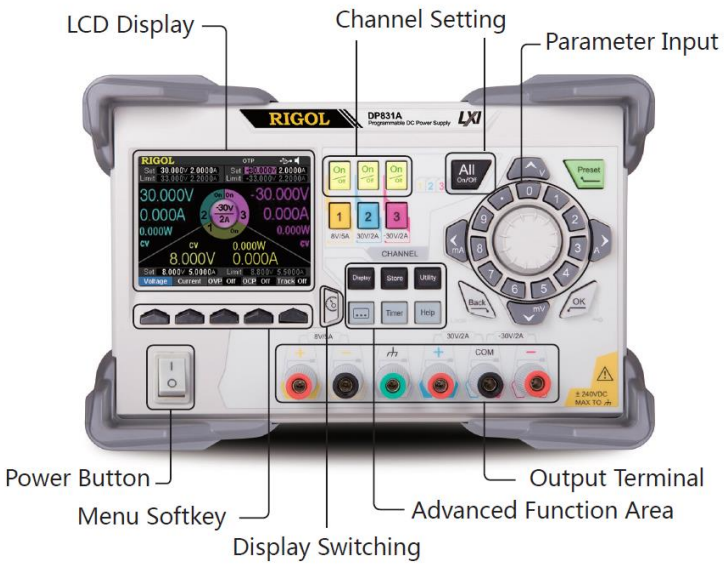


Figure 4-3 Rigol DP832A Programmable DC Power Supply [37] [fair use]

4.1.1.3 Oven

To control the ambient temperature of the board, the board is placed in a Yamato DX302 Convection Drying Oven, which has a temperature range of +10 °C - 300 °C [38].

Figure 4-4 Yamato DX302 Convection Drying Oven [38] [fair use]

4.1.2 Procedure

The board is measured at 5 different temperatures: 25 $°C$, 100 $°C$, 150 $°C$, 200 $°C$, and 225 $°C$. At each temperature the Fundamental, 2nd Harmonic, 3rd Harmonic, phase noise at 100 kHz and 1 MHz offset, and the center frequency is measured for tuning voltages from 2-30V in steps of 2V.

4.2 Measurement Results

Initial measurements at room temperature showed a significant deviation from the simulated center frequency. The results presented in this section are after trimming the terminating network and series feedback network transmission lines with a knife and adjusting the gate bias to be $V_{GG} = -2.3\ V$, which was found to give better tuning performance than $V_{GG} = -2.5\ V$.

4.2.1 Tuning Range

The VCO is biased at V_{GG}=-2.3 V, V_{DD}=2.5V, and is measured with V_{tune} ranging from 2 to 30 V. At room temperature -- 25 $°C$ -- this corresponds to a full tuning range of 2.333 – 2.42 GHz. At 225 $°C$ the tuning range deteriorates to 2.336 – 2.402 GHz which corresponds to a decrease of 21 MHz in tuning range over the full temperature range. A plot of output frequency versus tuning range at different temperatures is shown in Figure 4-5. The change is tuning range and frequency indicates a change in the quality factor of the resonator. This is due to the change in the quality factor in the active device and the

varactor. Past work has shown that the quality factor of the GaN varactor decreases with increasing temperature [29].

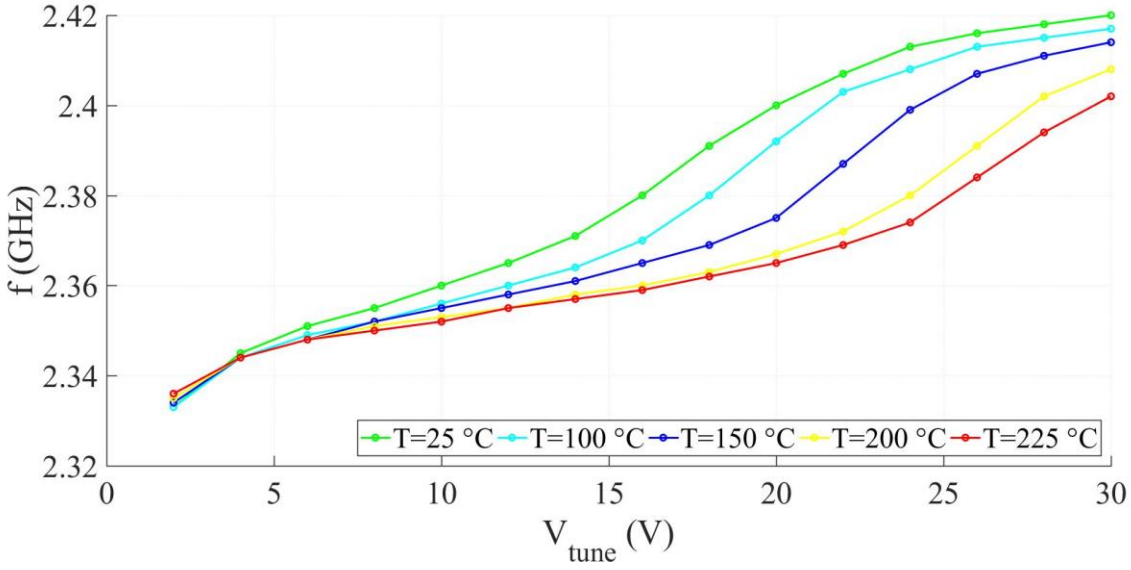


Figure 4-5 Measured output frequency versus tuning range at different temperatures

4.2.2 Output Power

The fundamental and harmonic signal power is seen to fluctuate with temperature, with a general trend of reduction in the amplitude.

4.2.2.1 Fundamental

The fundamental output power versus tuning voltage at different temperatures is shown in Figure 4-6. The range of output power is from 16.5 dBm to 20.79 dBm across all tuning voltages and temperatures. The general trend is for the output power to reduce with increasing temperature. This is consistent with the reduction in mobility and therefore current with an increase in temperature.

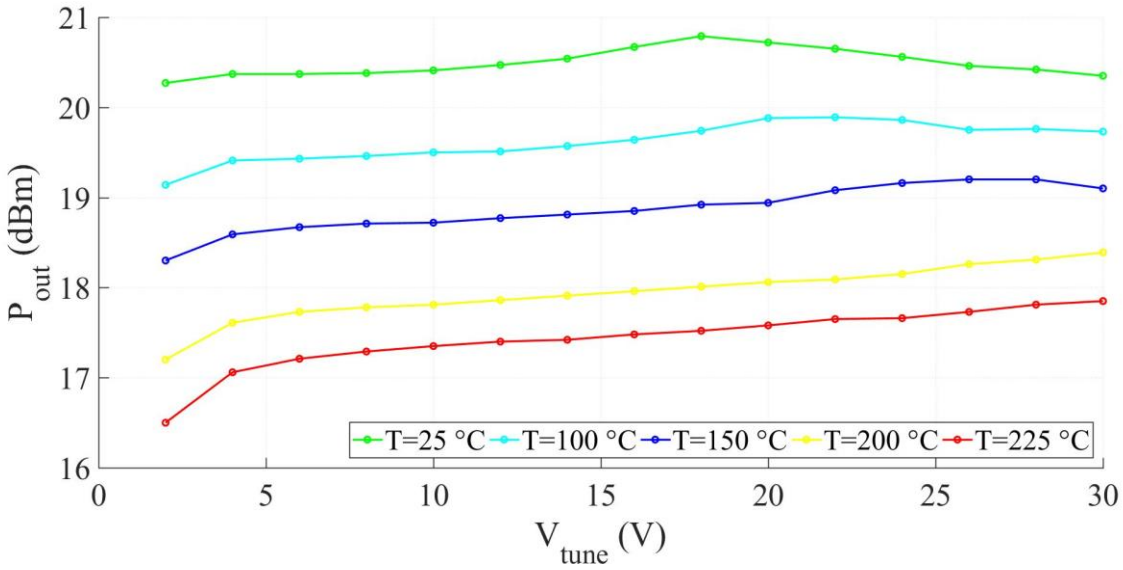


Figure 4-6 Fundamental output power versus tuning voltage for different temperatures

4.2.2.2 2nd and 3rd Harmonic

The fundamental power and 2nd Harmonic are plotted on the same graph versus tuning voltage at different temperatures in Figure 4-7. The 2nd Harmonic is more than 30 dB down from the fundamental at all temperatures and tuning voltages.

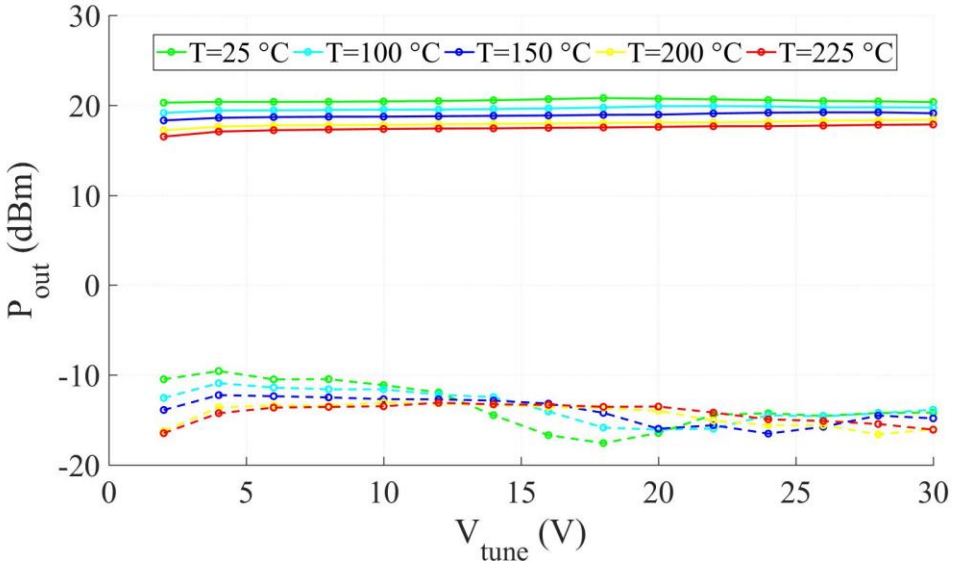


Figure 4-7 Fundamental (solid) and 2nd Harmonic (dashed) power versus tuning voltage for different temperatures

The 3rd Harmonic and fundamental power are plotted on the same graph versus tuning voltage at different temperatures in Figure 4-8. In comparing Figure 4-7 and Figure 4-8 the 3rd Harmonic is much higher than the 2nd Harmonic. However, the 3rd Harmonic is still more than 21 dB from the fundamental at all tuning voltages and temperatures.

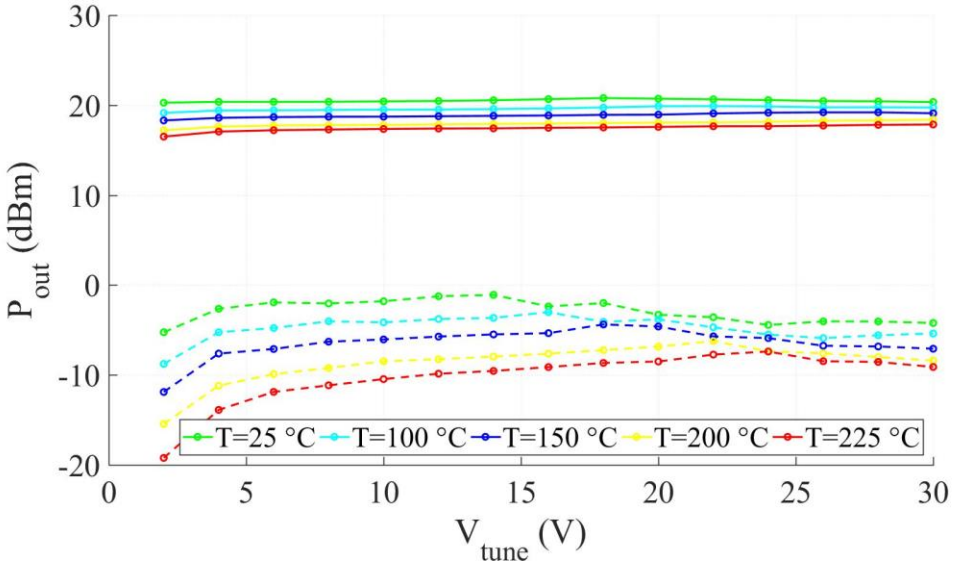


Figure 4-8 Fundamental (solid) and 3rd Harmonic (dashed) power versus tuning voltage at different temperatures

4.2.3 Phase Noise

The phase noise at a 100 kHz offset across tuning voltages and different temperatures is shown in Figure 4-9. The maximum phase noise at 100 kHz offset is -88 dBc/Hz and the minimum is -114 dBc/Hz across all temperatures and tuning voltages.

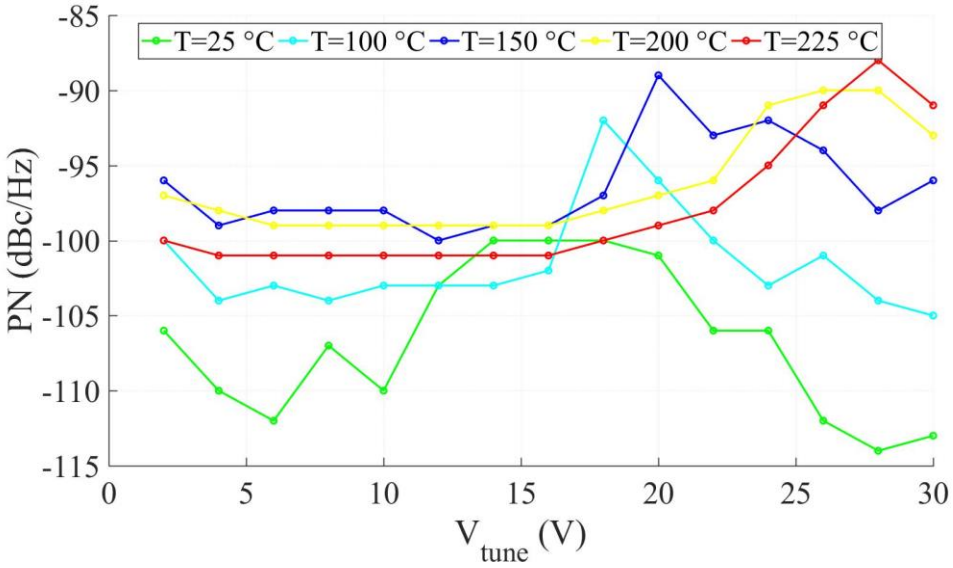


Figure 4-9 Phase noise at 100 kHz offset versus tuning voltage at different temperatures

The phase noise at 1 MHz offset across tuning voltages and different temperatures is shown in Figure 4-10. The maximum phase noise at 1 MHz offset is -113 dBc/Hz, and the minimum is -129 dBc/Hz.

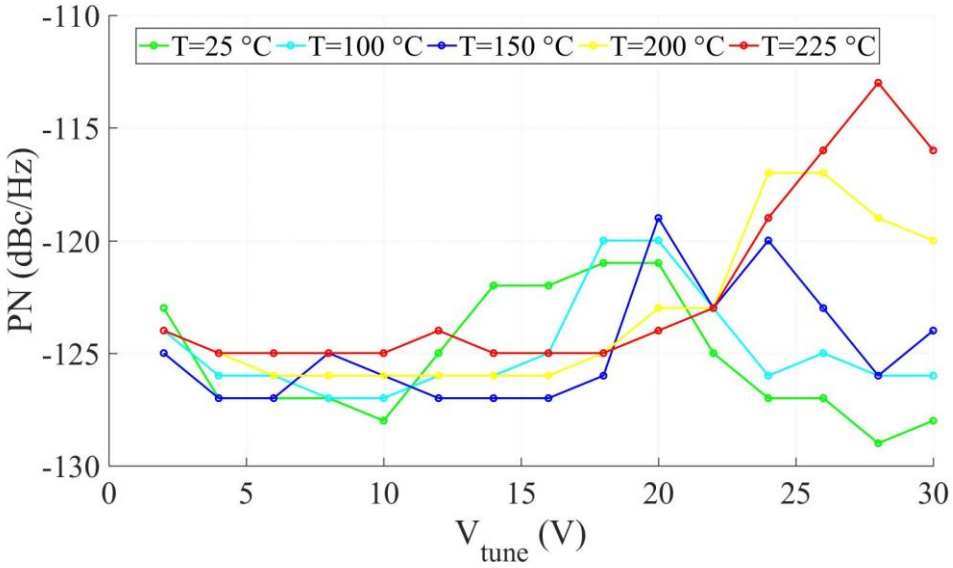


Figure 4-10 Phase noise at 1 MHz offset versus tuning voltage at different temperatures

A plot of the phase noise from 10 kHz to 10 MHz at a single tuning voltage $V_{tune} = 12V$ is shown in Figure 4-11.

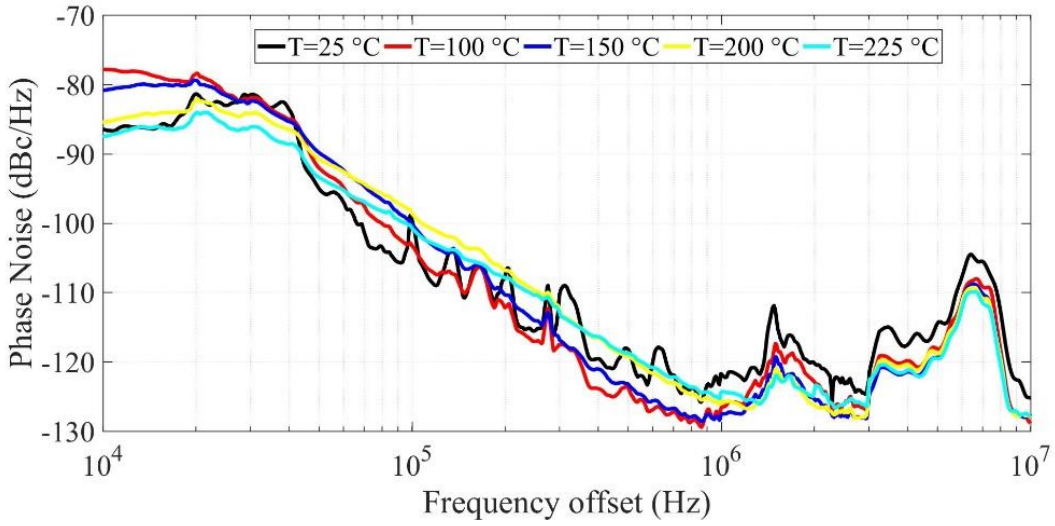


Figure 4-11 Phase noise plot at V_{tune} = 12V for different temperatures

Referring to the phase noise plots for the 1 MHz and 100 kHz offsets there exists points where the phase noise increases sharply and then decreases. This indicates that there is some sort of resonance near that frequency/capacitance. The reason the spike does not appear at the same tuning voltage over frequencies is because the capacitance of the varactor drops with increasing temperature [29]. Additionally, Lai et al. showed that for GaN HEMT oscillators the flicker noise corner and therefore the phase noise is heavily dependent on the DC bias [39]. The change in current with a large increase in temperature then affects the flicker noise corner and phase noise in a not necessarily linear manner.

4.2.4 Comparison

Comparison of oscillators is generally difficult as technology, application, and frequency range differ. A relationship between the frequency of the oscillator and the

phase noise exists as seen in Leeson's model in Eq. 2.42. This relationship can be summarized as

$$\mathcal{L} \propto 10\log\{f_o^2\} \tag{4.1}$$

And, assuming everything about the oscillators are the same except for the frequencies the the phase noise of oscillators can be related by the ratio of the frequencies

$$\mathcal{L}_{Hi} - \mathcal{L}_{Low} = 20\log(\frac{f_{Hi}}{f_{Low}}) \tag{4.2}$$

Therefore, the lower frequency phase-noise can be scaled up to the higher frequency by

$$\mathcal{L}_{low,adj} = \mathcal{L}_{Low} + 20\log\left(\frac{f_{Hi}}{f_{Low}}\right) \tag{4.3}$$

Table 4-1 shows a comparison between the VCO presented in this work and past works. After adjusting the phase noise for the change in frequency, the VCO presented in this work shows good performance with regards to tuning range, output power, and phase noise.

Table 4-1 Comparison to past works

Parameter	[28]	[24]	[26]	[29]	This work
Temperature (°C)	25-200	25-250	30-200	25-230	**25-225**
Technology	SOS CMOS	GaN HEMT	SiC	GaN HEMT	**GaN HEMT**
Frequency (MHz)	300	58	1000	350	**2357**
Output Power (dBm)	4.9-2.2	11	21.8	18	**17.4**
Output power variation with T (%)	-	62.5	19	8.3	**15.2**
Tuning Range (MHz)	100	0	0	40	**66**
Power Dissipation (mW)	-	-	1010	127.5	**400**
Phase Noise @ 100 kHz (dBc/Hz)	-70	-120	-	-121	**-101**
Adjusted Phase Noise @ 100 kHz (dBc/Hz)	-52	-88		-105	**-101**

Chapter 5

5 Conclusion

5.1 Summary

A high temperature, 2.36 GHz center frequency at 225 $°C$, VCO for a RF Modem for downhole communications is designed and prototyped using the commercially available 0.25 μm GaN-on-SiC Cree CGH40006P transistor on a Rogers 4003 C board. The output varies less than 20% over nearly a decade of temperature change. A minimum phase noise of -114 dBc/Hz at 100 kHz offset is achieved at room temperature, and a minimum phase noise of -101 dBc/Hz at 100 kHz offset is achieved at 225 $°C$. Harmonic content is better than 20 dB below the fundamental.

5.2 Conclusions

This work demonstrates the feasibility of using GaN-on-SiC HEMT, and microstrip circuits to create a functioning tunable oscillator at high temperatures. It is mainly a proof of concept demonstrating that cost effective solutions exist for high temperature oscillators available in the form of commercial transistors and cheap PCB processes.

5.3 Future Work

Several improvements can be made on this oscillator design. The first is to fully characterize the transistors across temperature and frequency and use that measured data to design the oscillator rather than trimming the transmission lines after it is manufactured. Improvements in the phase noise could be made by designing a Dielectric

Resonator Oscillator (DRO), however this will likely present a limit on the tuning range. Better varactors with higher quality factors would also improve the performance of the oscillator. Adjustable bias would be beneficial in keeping the frequency drift low across temperatures. Finally, implementation in a commercial GaN-on-SiC process could be explored to miniaturize the project and have on-chip temperature dependent biasing however, this would be costly for a university.

References

[1] J. Watson and G. Castro, "A review of high-temperature electronics technology and applications," *Journal of Materials Science: Materials in Electronics,* journal article vol. 26, no. 12, pp. 9226-9235, December 01 2015.

[2] J. D. Cressler and H. A. Mantooth, *Extreme environment electronics*. CRC Press, 2017.

[3] Schlumberger, "Wireline Services Catalog," ed. Houston, Texas, 2015, pp. 12-13.

[4] T. Tran, W. Sun, J. Zeng, and B. Wiecek, "High-bitrate downhole telemetry system," in *Power Line Communications and its Applications (ISPLC), 2015 International Symposium on*, 2015, pp. 280-284: IEEE.

[5] D. Wake, A. Nkansah, and N. J. Gomes, "Radio Over Fiber Link Design for Next Generation Wireless Systems," *Journal of Lightwave Technology,* vol. 28, no. 16, pp. 2456-2464, 2010.

[6] M. Steer, *Microwave and RF Design: A Systems Approach*, 2nd ed. Edison, NJ: SciTech Publishing, 2013.

[7] P. G. Neudeck, R. S. Okojie, and C. Liang-Yu, "High-temperature electronics - a role for wide bandgap semiconductors?," *Proceedings of the IEEE,* vol. 90, no. 6, pp. 1065-1076, 2002.

[8] C. Buttay *et al.*, "State of the art of high temperature power electronics," *Materials Science and Engineering: B,* vol. 176, no. 4, pp. 283-288, 2011/03/15/ 2011.

[9] U. K. Mishra, L. Shen, T. E. Kazior, and Y. F. Wu, "GaN-Based RF Power Devices and Amplifiers," *Proceedings of the IEEE,* vol. 96, no. 2, pp. 287-305, 2008.

[10] S. C. Binari, K. Doverspike, G. Kelner, H. Dietrich, and A. Wickenden, "GaN FETs for microwave and high-temperature applications," *Solid-State Electronics,* vol. 41, no. 2, pp. 177-180, 1997.

[11] C. Poole and I. Darwazeh, "S-parameters," in *Microwave Active Circuit Analysis and Design*: Elsevier, 2015, pp. 167-181.

[12] M. Steer, "Microwave Network Analysis," in *Microwave and RF Design: A Systems Approach*2nd ed. Edison, NJ: SciTech Publishing, 2013, pp. 407-445.

[13] M. Steer, "Linear Amplifiers," in *Microwave and RF Design: A Systems Approach*2nd ed. Edison, NJ: SciTech Publishing, 2013, pp. 817-872.

[14] M. Steer, "Transmission Lines," in *Microwave and RF Design: A Systems Approach*2nd ed. Edison, NJ: SciTech Publishing, 2013, pp. 199-266.

[15] D. M. Pozar, "Transmission Lines and Waveguides," in *Microwave Engineering*

4th ed.: John Wiley & Sons, Inc., 2012, pp. 95-164.

[16] D. M. Pozar, "Impedance Matching and Tuning," in *Microwave Engineering*

4th ed.: John Wiley & Sons, Inc., 2012, pp. 228-271.

[17] G. Gonzalez, "Theory of Oscillators," in *Foundations of Oscillator Circuit Design*: Artech House, 2007, pp. 5-51.

[18] G. Gonzalez, "Oscillator Characterisitics," in *Foundations of Oscillator Circuit Design*: Artech House, 2007, pp. 53-102.

[19] D. M. Pozar, "Microwave Resonators," in *Microwave Engineering*

4th ed.: John Wiley & Sons, Inc., 2012, pp. 272-316.
[20] T. H. Lee and A. Hajimiri, "Oscillator phase noise: A tutorial," *IEEE journal of solid-state circuits,* vol. 35, no. 3, pp. 326-336, 2000.
[21] G. Gonzalez, "Negative-Resistance Oscillators," in *Foundations of Oscillator Circuit Design*: Artech House, 2007, pp. 251-350.
[22] S. M. Sze, "Physics and Properties of Semiconductors - A Review," in *Physics of Semiconductor Devices*3rd ed.: John Wiley & Sons, Inc., 2007, pp. 7-68.
[23] D. Wolpert and P. Ampadu, "Temperature Effects in Semiconductors," in *Managing Temperature Effects in Nanoscale Adaptive Systems*New York, NY: Springer New York, 2012, pp. 15-33.
[24] X. Lu, J. Ma, C. P. Yue, and K. M. Lau, "A GaN-Based Lamb-Wave Oscillator on Silicon for High-Temperature Integrated Sensors," *IEEE Microwave and Wireless Components Letters,* vol. 23, no. 6, pp. 318-320, 2013.
[25] Z. D. Schwartz and G. E. Ponchak, "High temperature performance of a SiC MESFET based oscillator," in *Microwave Symposium Digest, 2005 IEEE MTT-S International*, 2005, pp. 1179-1182: IEEE.
[26] Z. D. Schwartz and G. E. Ponchak, "1-GHz, 200/spl deg/C, SiC MESFET Clapp oscillator," *IEEE microwave and wireless components letters,* vol. 15, no. 11, pp. 730-732, 2005.
[27] M. C. Scardelletti and G. E. Ponchak, "Characterization of 720 and 940 MHz oscillators with chip antenna for wireless sensors from room temperature to 200 and 250 °C," in *2011 IEEE Topical Conference on Wireless Sensors and Sensor Networks*, 2011, pp. 49-52.
[28] A. Moor, J. Rochelle, C. Britton, J. Moore, M. Emery, and R. Schultz, "A voltage-controlled oscillator for a 300 MHz high-temperature transceiver realized in 0.5/spl mu/m SOS technology," in *Circuits and Systems, 2001. MWSCAS 2001. Proceedings of the 44th IEEE 2001 Midwest Symposium on*, 2001, vol. 2, pp. 614-617: IEEE.
[29] T. Feng, J. M. Salem, and D. S. Ha, "High temperature VCO based on GaN devices for downhole communications," in *2017 IEEE International Symposium on Circuits and Systems (ISCAS)*, 2017, pp. 1-4.
[30] Cree, "6 W, RF Power GaN HEMT," CGH40006P Datasheet, May 2015, 2015.
[31] R. Corp., " RO4000 Series High Frequency Circuit Materials," Rogers Datasheet, 2018.
[32] Matweb. *Indium Corp. Indalloy 151 Pb-Sn-Ag Solder Alloy*.
[33] E. Toolbox. (2003). *Thermal Conductiviy of common Materials and Gases* [online].
[34] D. M. Pozar, "Transmission Line Theory," in *Microwave Engineering*

4th ed.: John Wiley & Sons, Inc., 2012, pp. 48-94.
[35] R. Schwarz, "R&S FSW Signal and Spectrum Analyzer Specifications," R&S FSW Datasheet, May 2018, 2018.
[36] R. a. Schwarz. (2018). [Online]. Available: https://www.rohde-schwarz.com/us/product/fsw-productstartpage_63493-11793.html
[37] Rigol, "DP800 Series Programmable Linear DC Power Supply," Datasheet, June 2016, 2016.

[38] Yamato. *Laboratory Drying Ovens, Constant Temperature DX302/402/602* [Online]. Available: http://www.yamato-scientific.com/product/ovens/dx302402602.htm
[39] S. Lai *et al.*, "Low Phase Noise GaN HEMT Oscillators With Excellent Figures of Merit," *IEEE Microwave and Wireless Components Letters*, vol. 24, no. 6, pp. 412-414, 2014.