Advanced Single-Stage Power Factor Correction Techniques

by

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(ABSTRACT)

Five new single-stage power factor correction (PFC) techniques are developed for single-phase applications. These converters are: Integrated single-stage PFC converters, voltage source charge pump power factor correction (VS-CPPFC) converters, current source CPPFC converters, combined voltage source current source (VSCS) CPPFC converters, and continuous input current (CIC) CPPFC converters.

Integrated single-stage PFC converters are first developed, which combine the PFC converter with a DC/DC converter into a single-stage converter. DC bus voltage stress at light load for the single-stage PFC converters are analyzed. DC bus voltage feedback concept is proposed to reduce the DC bus voltage stress at light load. The principle of operations of proposed converters are presented, implemented and evaluated. The experimental results verify the theoretical analysis.

VS-CPPFC technique use a capacitor in series with a high frequency voltage source to achieve the PFC function. In this way, the input inductor is eliminated. VS-CPPFC AC/DC converters are developed, and their performance is evaluated. VS-CPPFC electronic ballasts with and without dimming function are also presented. The average lamp current control with duty ratio modulation is developed so that the lamp operates in constant power with a low crest factor over the line variation. The experimental results verify the CPPFC concept.

CS-CPPFC technique employs a capacitor in parallel with a high frequency current source to obtain the PFC function. The unity power factor condition and principle of operation are analyzed. By doing so, the switch has less switching current stress, and deals only with the

resonant inductor current. Design considerations and experimental results of the CS-CPPFC electronic ballast are presented.

VSCS-CPPFC technique integrates the VS-CPPFC with the CS-CPPFC converters. The circuit derivation, unity power factor condition and design considerations are presented. The developed VSCS-CPPFC converters has constant lamp operation, low crest factor with a high power factor even without any feedback control.

CIC-CPPFC technique is developed by inserting a small inductor in series with the line rectifier for the conceptual VS-CPPFC, CS-CPPFC and VSCS-CPPFC circuits. The circuit derivation and its unity power factor condition are discussed. The input current can be designed to be continuous, and a small line input filter can be used. The circulating current in the resonant tank and the switching current stress are minimized. The average lamp current control with switching frequency modulation is developed, so the developed electronic ballast operates in constant power, low crest factor. The developed CIC-CPPFC electronic ballast has features of low line input current harmonics, constant lamp power, low crest factor, continuous input current, low DC bus voltage stress, small circulating current and switching current stress over a wide range of line input voltage.

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CHAPTER 1

INTRODUCTION

1.1 Background

Most electronic equipment is supplied by 60 Hz utility power, and more than 50% of this power is processed through some kind of power converter. Usually power converters use a diode rectifier followed by a bulk capacitor to convert AC voltage to DC voltage. Since these power converters absorb energy from the AC line only when the line voltage is higher than the DC bus voltage, the input line current contains rich harmonics, which pollute the power system and interfere with other electric equipment. These converters usually have a low power factor of 0.65 [A1, A2]. More stringent international requirements to limit the line input current harmonics, such as IEC 1000, have been effected recently. Because the conventional simple diode rectifier followed by a bulk capacitor cannot meet the requirements, which have stimulated the research of power factor correction techniques.

The power factor is defined as the ratio of the average power to the apparent power at an AC terminal [A3]. Assuming an ideal sinusoidal input voltage source, the power factor can be expressed as the product of two factors, the distortion factor and the displacement factor, as given in Eq. (1.1). The distortion factor k_d is the ratio of the fundamental root-mean-square (RMS) current to the total RMS current. The displacement factor k_θ is the cosine of the displacement angle between the fundamental input current and the input voltage.

$$\begin{aligned} PF &= K_d\, K_q \\ K_d &= \frac{I_{rms(1)}}{I_{rms}} \\ K_q &= \cos q \end{aligned} \tag{1.1}$$

When a converter has less than unity power factor, it means that the converter absorbs apparent power higher than the real power it consumes. This implies that the power source should be rated with higher VA ratings than the load needs. In addition, the current harmonics the converter produces deteriorate the power source quality, which eventually affect the other equipment. The simple solution to improve the power factor is to add a passive filter, which is usually composed of a capacitor and an inductor. However, this passive filter is bulky and inefficient since it operates at the line frequency. Therefore, a power factor correction stage has to be inserted to the existing equipment to achieve a good power factor. Usually, two types of power factor correction methods are used: the VAR/harmonics compensation method [A1-A4] and the off-line PFC method [A5-A34]. The VAR/harmonics compensation method employs a switch-mode power converter in parallel with the nonlinear load to supply a reactive power and/or line current harmonics to cancel the displacement and the line current harmonics created by the nonlinear load. This method cannot cancel all the line current harmonics, however, and this additional line current harmonics compensator cannot regulate the output to the load. The high frequency switch mode power factor correction converter [A5-A34], called a PFC stage, is usually inserted in the equipment to shape the line input current into a sinusoidal waveform and its line current is in phase with the line voltage.

This dissertation will focus on the development of the advanced power factor correction techniques. In the following section, the current power factor correction techniques will be briefly reviewed. Next, the excepted contribution of this dissertation will be introduced.

1.2 Review of present power factor correction techniques

Among three basic power converter topologies (boost, buck and buck-boost), the boost converter shown in Fig. 1.1 [A7-A26] is the one most suitable for power factor correction applications. This is because the inductor is in series with the line input terminal through the diode rectifier, which gives lower line current ripple and continuous input current can be obtained with an average current mode control chip like UC3854. As a result, a small line input filter can be used. Furthermore, the power switch is in shunt with the main power flow so that the converter operates efficiently. However, the output voltage has to be higher than the line input

voltage for a boost converter. The buck converter is seldom used as a power factor correction application [A5-A6], since the input current is discontinuous and it loses control when the line input voltage is lower than the output voltage. The buck-boost and flyback converters are able to control the average line input current [A27-A29]. However, the power handling capability is smaller because of its higher voltage and current stresses. Therefore, the boost converter is currently the most popular PFC topology. To achieve unity power factor, the input power is the squared sine waveform while the output power is usually constant for most applications. Thus, the power is unbalanced between the input and the output over half the line cycle. This unbalanced power has to be stored in an energy storage element, like the bulk capacitor. For a boost converter, the output filter capacitor, which is the only bulk capacitor, can deal with this unbalanced power. Therefore, the output voltage has 2nd order line ripple, which is undesirable for many applications. Furthermore, the output voltage is higher than the input

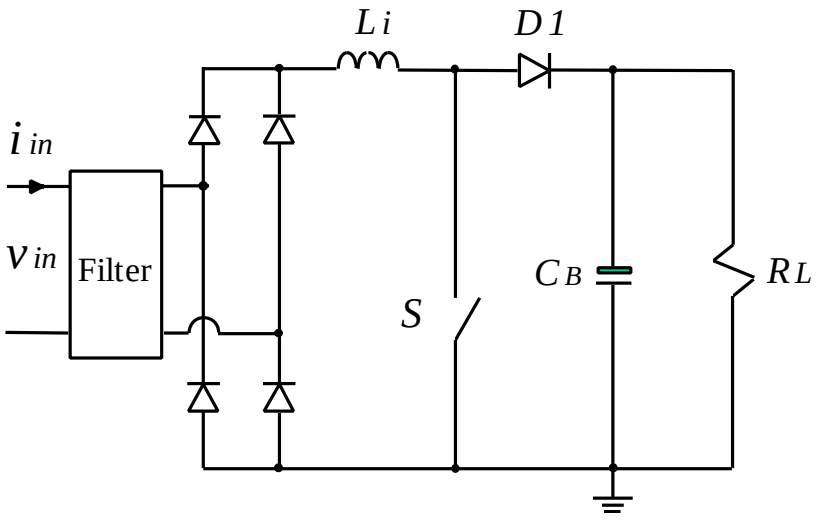


Fig. 1.1 Power factor correction boost converter

voltage, which is unsuitable for step-down applications. Therefore, another DC/DC converter has to be cascaded with this PFC converter to obtain the desired output voltage and tightly regulate the output voltage. Consequently, the power has to be processed twice, which is inefficient. In addition, the cost increases because the component count increases. This is the main disadvantage for the two-stage approach.

In order to reduce the cost, many single-stage PFC converters, which integrate the PFC stage with the DC/DC stage into a single stage, have been proposed recently [B1-B26]. The main idea is that the PFC stage and DC/DC stage share a common switch so that one main switch and its controller can be saved. However, the control freedom has been reduced and only one control variable can be controlled. For most applications, the output voltage has to be tightly regulated, while the power factor cannot be controlled. Thus, it requires that the PFC stage have inherent power factor correction. A good power factor can be obtained if the boost converter is operated in the discontinuous current mode (DCM) [B1-B9], so a DCM boost converter integrated with another converter can achieve power factor correction and tight output voltage. BIFRED and BIBRED, shown in Fig. 1.2 [B1], are examples of these single-stage PFC converters. The main disadvantage is that high DC bus voltage stress exists at light load, if the PFC stage operates in DCM and the DC/DC converter operates in CCM. The duty ratio does not change with a reduced load. Power is unbalanced between the input and the output. This unbalanced power has to be stored in the DC bulk capacitor. As a result, the DC bus voltage increases, which decreases the duty ratio. The reduced duty ratio decreases the input power until a new power balance is reached. Therefore, a high DC bus voltage exists at light load, which requires the use of high voltage-rating devices. Usually, the higher the voltage rating, the higher the conduction loss. To suppress the DC bus voltage, the variable switching frequency scheme was developed in [B2, B5]. However, the efficiency is still lower than the two-stage approach, mainly because of the wide range switching frequency operation. In addition, it is difficult to optimally design inductive components, like inductors and EMI filter, for wide range switching frequency operation.

For power factor correction electronic ballasts, the two-stage approach, shown in Fig. 1.3(a), is usually used. The first stage is a power factor correction stage such as a DCM boost converter, while the second stage is a DC/AC inverter to provide high frequency energy to the lamp. However, the cost increases because the component count increases. To reduce the component count, a DCM boost converter integrated with a DC/AC inverter was proposed [B10- B16].

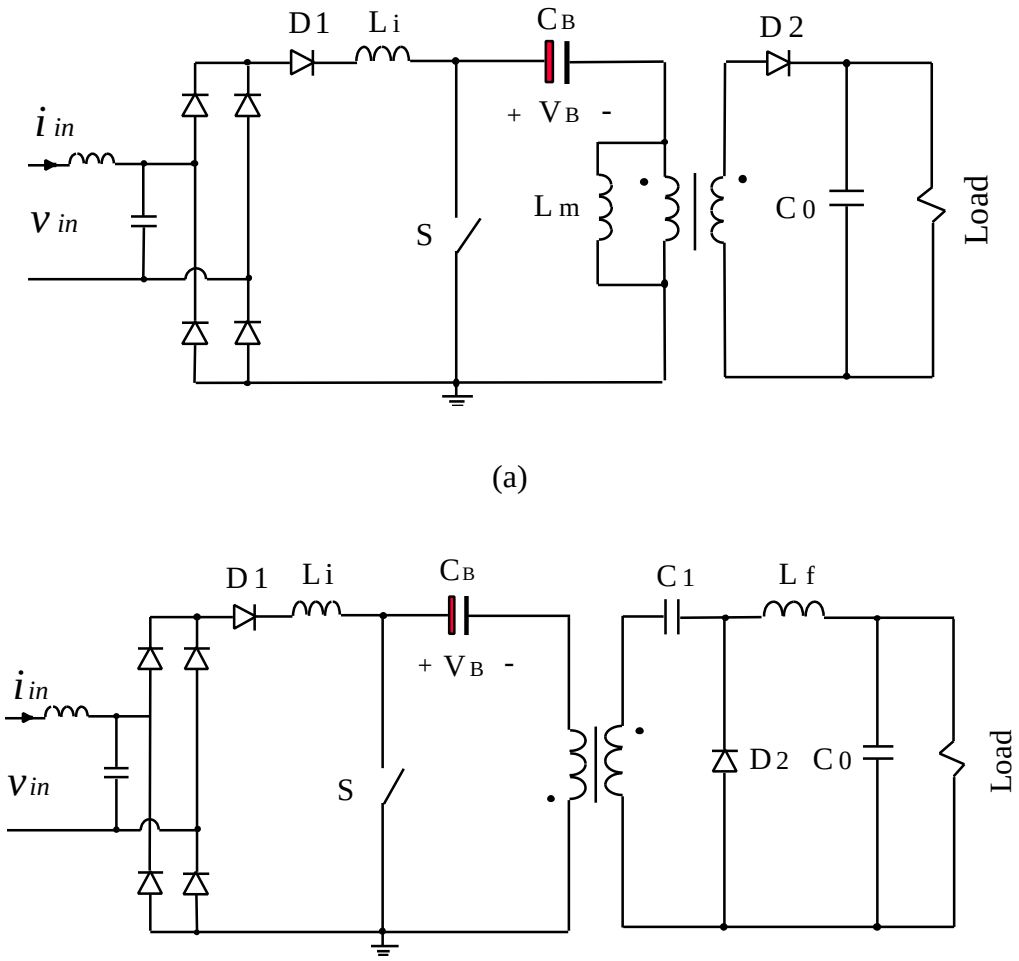
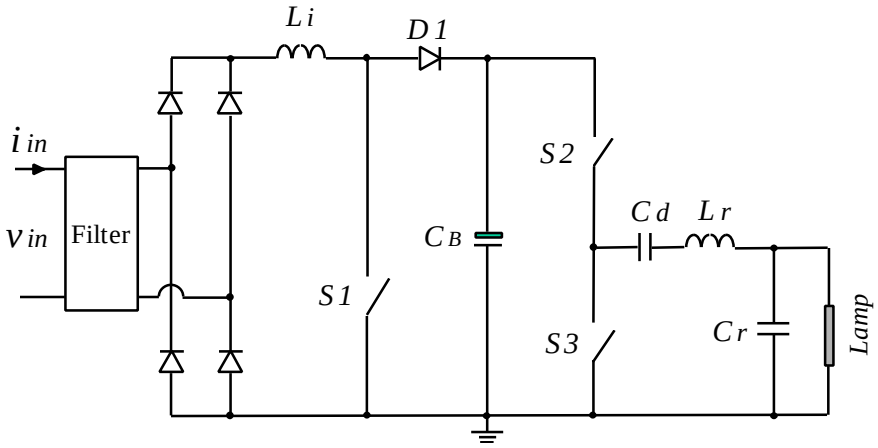


Fig. 1.2 Integrated single-stage PFC converters: (a) BIFRED, (b) BIBRED

The PFC stage and the DC/AC inverter share a common power switch. Therefore, the boost switch and its controller can be saved, consequently reducing the cost. Fig. 1.3(b) shows one example of the integrated PFC electronic ballast. The shared switch, however, has to take the current not only from the power factor correction stage but also from the resonant tank. This switch must have a higher current rating than that in the two-stage approach. Another of the



(a)

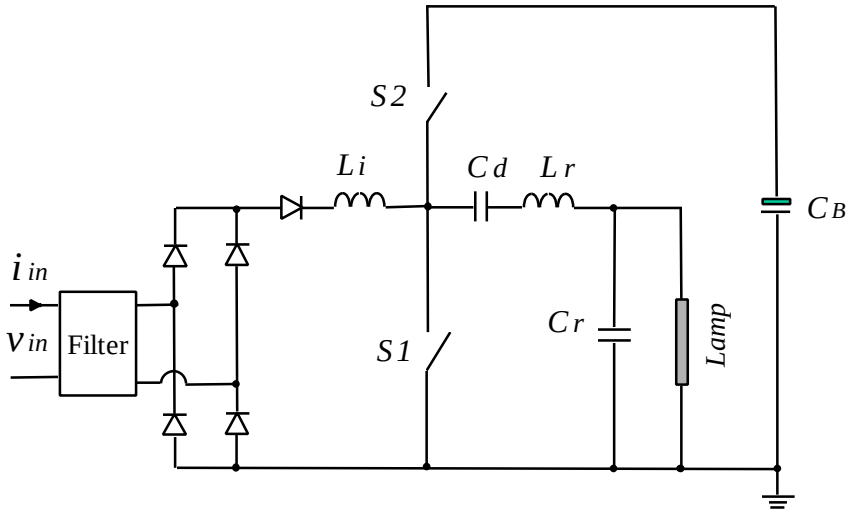


Fig. 1.3 (a) Two-stage power factor correction electronic ballast

(b) Integrated single-stage power factor correction electronic ballast

main drawbacks is that there is high DC bus voltage stress at the lamp start-up, so a high voltage rating bulk capacitor and power switches have to be used. Furthermore, least one boost choke and one resonant inductor have to be used to achieve power factor correction and provide high frequency energy to the lamp.

Charge pump power factor correction (CPPFC) techniques have become attractive. they use capacitors instead of an inductor to achieve power factor correction [C1-C13, D1-D7, E1-E5, F1-F6]. It is the capacitor that integrates with the DC/DC converter or the DC/AC inverter to achieve power factor correction. Figure 1.4 shows the basic charge pump power factor correction electronic ballast [C3]. C_{in} is used to integrate the PFC stage with the DC/AC inverter to achieve power factor correction. This circuit has a potentially low cost compared with the circuit in Fig. 1.3. However, the main problems of this circuit are high DC bus voltage stress at start-up mode, high lamp crest factor, and a little high Total Harmonic Distortion (THD).

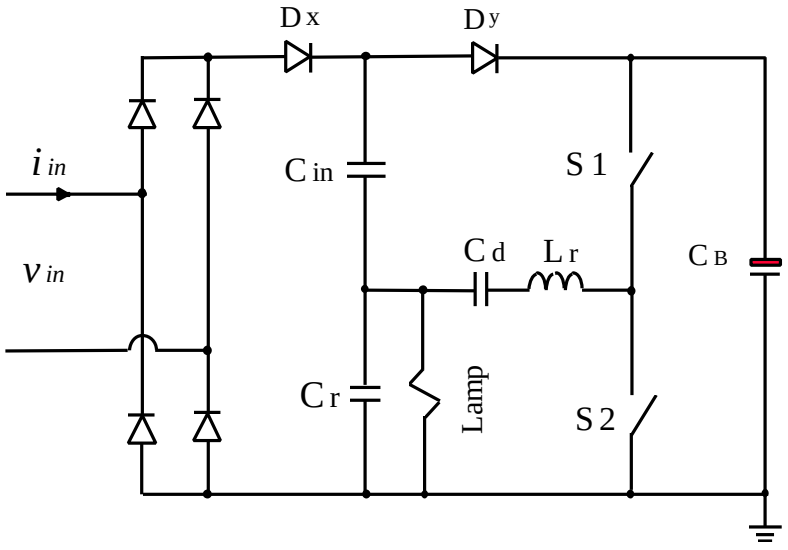


Fig. 1.4 Basic charge pump power factor correction electronic ballast

1.3 Motivation and Objectives

The preceding discussion of the current status of power factor conversion techniques demonstrates the need for further research in this area. Specifically, four areas need to be addressed.

1 When the output voltage is required to be tightly regulated, the two-stage approach is used for most applications. A two-stage converter costs more, because it uses more components. An important research objective, therefore, is to develop new single-stage PFC converters with low DC bus voltage stress.

2 Current electronic equipment has to satisfy IEC 1000 requirements to limit the line input current harmonics. To meet this regulation, however, unity power factor is not required; 0.8 power factor is enough to meet the line current harmonics limitation. It is important, therefore, to discover and evaluate new PFC techniques with fair power factor, high efficiency, and low cost.

3 The most commonly used PFC topology for low power applications is the DCM boost converter, since the DCM boost has an inherent PFC function. However, the boost inductor is bulky, heavy, and expensive. Another objective, therefore, is to develop new power factor correction converters employing a capacitor for achieving power factor correction, because the capacitor is usually cheaper and more reliable than the inductor.

4 Because the DCM boost converter has a discontinuous input current, it requires a relatively large input filter to suppress the high frequency input line current harmonics. It would be important, therefore, to develop continuous input current power factor correction techniques that use a capacitor in place of an inductor.

The overall objective of this dissertation is to develop advanced single-stage PFC techniques that incorporates these four objectives. This would result in new converter topologies that would cost less while performing better.

1.4 Dissertation Outline

This dissertation is composed of seven chapters.

Chapter 1 briefly reviews the present power factor correction techniques. It then lists the research objectives and provides this outlines of the research.

Chapter 2 covers the integrated single-stage PFC technique. First, DC bus voltage stress at light load will be analyzed for different integrations of the PFC converter and the DC/DC converter. A single-stage PFC converter, consisting of a DCM flyback integrated with another DCM DC/DC converter is proposed and implemented. The DC bus voltage feedback concept to reduce the DC bus voltage is proposed. One single-stage PFC converter using this concept is analyzed and developed.

Chapter 3 proposes the charge pump concept to achieve unity power. The voltage source charge pump power factor correction (VS-CPPFC) converter is first derived. The conditions for achieving the unity power factor are then analyzed and derived. A VS-CPPFC AC/DC converter is proposed and the unity power factor condition is automatically satisfied by using a clamping technique. Single-stage CPPFC AC/DC converters are proposed. Circuit derivation and steady state analysis are discussed. One prototype is implemented to evaluate its electrical performance.

The VS-CPPFC electronic ballast with second resonance is also analyzed, designed and implemented. A continuous dimming VS-CPPFC electronic ballast with average lamp current control and duty ratio modulation is developed. The developed dimming electronic ballast has constant lamp operation over the line input voltage variation. A family of VS-CPPFC electronic ballasts are presented.

In Chapter 4, the current source charge pump power factor correction (CS-CPPFC) technique is presented. The CS-CPPFC converter and unity power factor condition are derived and analyzed. A CS-CPPFC electronic ballast is analyzed, designed, and implemented as an

example. A family of CS-CPPFC electronic ballasts is derived, based on the high frequency capacitor shift rule and the circuit symmetry concept.

Chapter 5 deals with integrating the VS-CPPFC and CS-CPPFC techniques. The voltage source current source charge pump power factor correction (VSCS-CPPFC) technique is developed. One VSCS-CPPFC electronic ballast is proposed, analyzed, designed and implemented to evaluate its performance.

Chapter 6 develops the continuous input current charge pump power factor correction (CIC-CPPFC) technique. A basic CIC-CPPFC converter is derived. Based on the derived CIC-CPPFC converter, one CIC-CPPFC electronic ballast is proposed, analyzed, and implemented. Another CIC-VSCS-CPPFC electronic ballast is also developed. It has extremely low DC bus voltage stress at start-up, small switching current stress, constant lamp power, and low crest factor, with continuous line input current over a wide range of line input voltage. A family of CIC-CPPFC electronic ballasts is derived and presented.

Conclusions are given in Chapter 7.

CHAPTER 2

INTEGRATED SINGLE-STAGE SINGLE-SWITCH POWER FACTOR CORRECTION (S^4-PFC) CONVERTERS

2.1 Introduction

As mentioned in Chapter 1, a boost converter can be used as a power factor correction converter either in CCM operation with average current mode control or DCM operation with constant on-time control [A7-A26]. However, the output voltage is not tightly regulated, and it suffers from 2nd order line frequency ripple. Furthermore, the output voltage cannot step down for a boost PFC converter. So another DC/DC converter has to cascade this PFC converter to achieve the desired tightly regulated output voltage, as shown in Fig. 2.1. Two converters are in series to meet IEC 1000 harmonics requirements and achieve tight regulation of output voltage. Therefore, the component count increases, which increases the cost. To overcome this disadvantage, several integrated single-stage power factor correction AC/DC converters, which combine the PFC stage with the DC/DC stage into a single-stage, have been previously proposed [B1-B27]. These converters achieve power factor correction and regulate output voltage by using

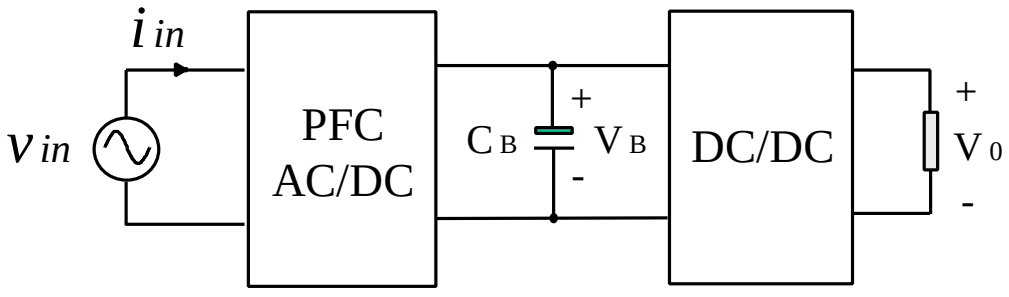


Fig. 2.1 Two-stage power factor correction AC/DC converter block diagram

only one switch, such as the Boost Integrated with Flyback Rectifier Energy storage DC/DC (BIFRED), Boost Integrated with Buck Rectifier Energy storage DC/DC (BIBRED) [B1]. Generally, these PFC converters operate in discontinuous current mode (DCM) to obtain power factor correction with constant on-time control. In order to tightly regulate the output voltage, an internal bulk capacitor is needed to balance the power between the input and the output. This bulk capacitor voltage is not regulated, and is determined by the power balance between the input and output. It usually suffers from relatively higher voltage stress at light load if the DC/DC stage, the second stage, operates in continuous current mode (CCM). Therefore, the variable switching frequency control technique is used to avoid this higher voltage stress [B2, B5]. However, it is difficult to optimally design the inductive components, like the inductor and transformer, for a wide-range switching frequency operation. Furthermore, it still cannot operate without a load.

This chapter will present integrated single-stage single-switch power factor correction (S^4-PFC) converters with fast output voltage regulation. First, DC bus voltage stress at light load for S^4-PFC converters is discussed. Next, the integrated DCM PFC with DCM DC/DC converter is investigated, implemented, and tested. The experimental results verify the proposed converter operation. Finally, DC bus voltage feedback concept to reduce the DC bus voltage at light load is proposed, and one S^4-PFC AC/DC converter with universal line input is analyzed, implemented, and tested, as an example. It will be shown that the DC bus voltage feedback scheme not only can suppress the DC bus voltage stress, but also can reduce the current stress through the power switch, improve the conversion efficiency, and enable the line input current to meet IEC 1000-3-2 Class D requirements.

2.2 DC Bus Voltage Stress for S^4-PFC Converters

The main disadvantage of two-stage PFC AC/DC converters is their high cost, because an additional power converter is cascaded in the AC/DC converter, and the component count increases. These two-stage PFC AC/DC converters usually increase the cost about 15%, compared with that of a DC/DC converter without a PFC function. In order to reduce the cost, it is desirable to integrate the two-stage converter into a single-stage PFC converter, where both the

PFC stage and the DC/DC stage share a common switch so that at least one switch and its control can be saved. As a result, the integrated PFC converter has a potentially low cost. The single-stage PFC converter block diagram is shown in Fig. 2.2. Both the PFC stage and DC/DC stage share a common switch. So, only one control variable can be controlled. Generally, the output voltage is needed to be tightly regulated by the voltage loop, as shown in Fig. 2.2, while the PFC stage cannot be controlled to achieve perfect power factor correction. Therefore, the PFC stage must have an inherent PFC function without active control. It is well known that the DCM boost converter has an inherent PFC with constant duty cycle. So, a DCM boost converter integrated with another DC/DC converter is able to achieve PFC and tight output regulation simultaneously. BIFRED and BIBRED are two of these converters [B1], and are shown in Fig. 2.3. In order to reduce power losses, CCM operation of the DC/DC stage is preferred, while the PFC stage operates in DCM to achieve PFC. One of the major problems is the high DC bus voltage at light load. It will be analyzed in more detail in the following.

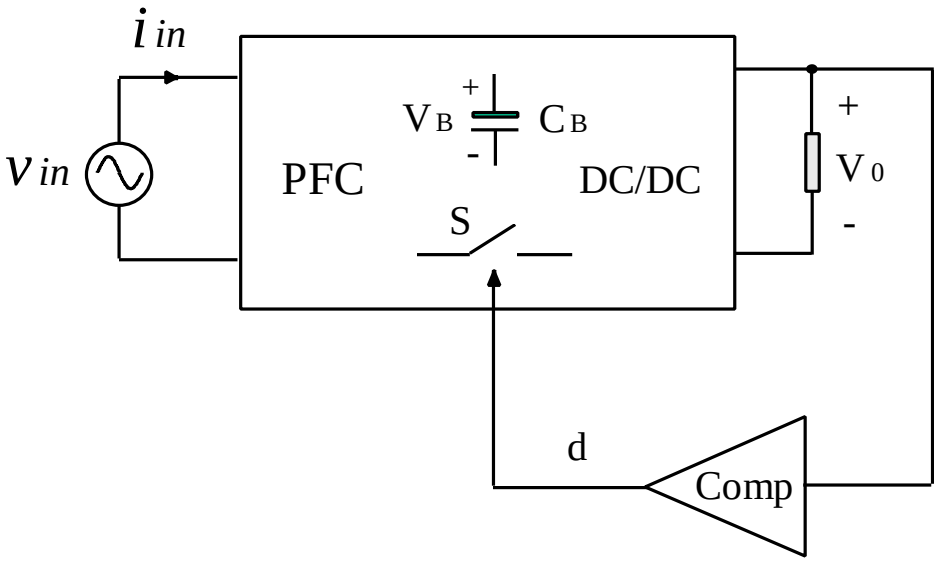


Fig 2.2 Single-stage PFC AC/DC converter block diagram

Figures 2.4 shows the relationship between the input power and the duty cycle in the PFC stage, and between the output power and the duty cycle in the DC/DC stage. The typical inherent PFC converter is the DCM boost converter, while the DC/DC stage can operate in either DCM or CCM. There are two practical combinations:

- DCM PFC + CCM DC/DC
- DCM PFC + DCM DC/DC

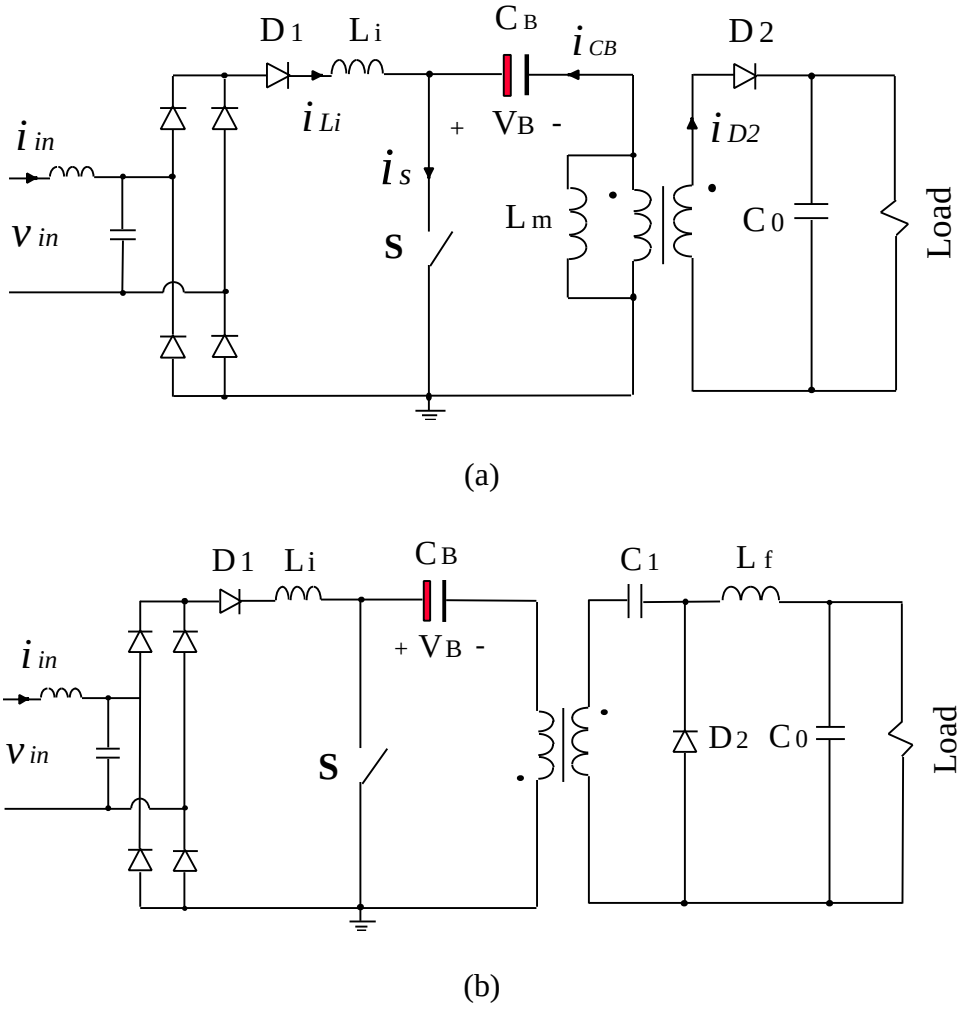


Fig. 2.3 (a) PFC BIFRED AC/DC converter
(b) PFC BIBRED AC/DC converter

2.2.1 DCM PFC + CCM DC/DC

Since the DC/DC stage operates in CCM, the duty cycle does not change with the load variation according to Fig. 2.4(a). When the load becomes light, which means the output power decreases. The duty cycle doesn't change immediately, because of the CCM operation in the DC/DC stage. Thus, the input power remains the same as that of the heavy load. There exists an unbalanced power between the input and the output. This unbalanced power has to be stored in the bulk capacitor C_B, causing the DC bus voltage to increase. As a result, the output voltage will increase too. To compensate for the output voltage increase due to the increase of the bus voltage, the voltage feedback loop is operated to regulate the output voltage as a constant. So the duty ratio has to decrease, and the input power also decreases correspondingly. This dynamic

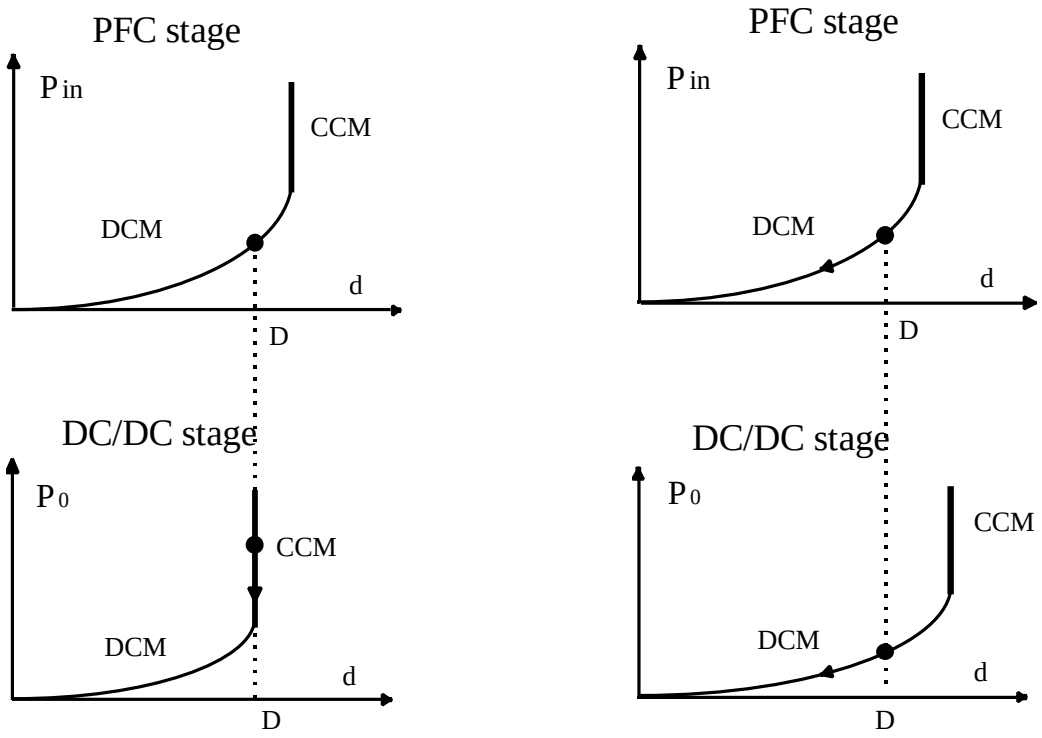


Fig. 2.4 The relationship between the input power, output power, and duty cycle
(a) DCM PFC + CCM DC/DC
(b) DCM PFC + DCM DC/DC

process will not stop until the input power equals the output power, and a new power equilibrium is reached. It is obvious that the power balance at light load is reached at the penalty of significant bus voltage stress. Variable switching frequency control for the DCM PFC + CCM DC/DC converter was proposed in [B2, B5]. The switching frequency can be controlled in such a way that the switching frequency increases when the load becomes light. It was shown that a wide switching frequency variation range is needed to suppress the DC bus voltage stress. If the load varies from 10% to full load, the switching frequency at light load should be 10 times as high as that of the heavy load. Therefore, it is difficult to optimize inductive components such as transformers and inductors.

2.2.2 DCM PFC + DCM DC/DC

If both the PFC and DC/DC stages operate in DCM, then the duty cycle has to decrease when the load becomes light, based on Fig. 2.4(b). It can be seen that the input power also decreases because the duty ratio decreases. Therefore, the input power decreases when the output power is reduced. There is no unbalanced power between the input and the output. It is concluded that there is no DC bus voltage issue for single-stage DCM PFC+DCM DC/DC converters. This statement will be verified in the next section.

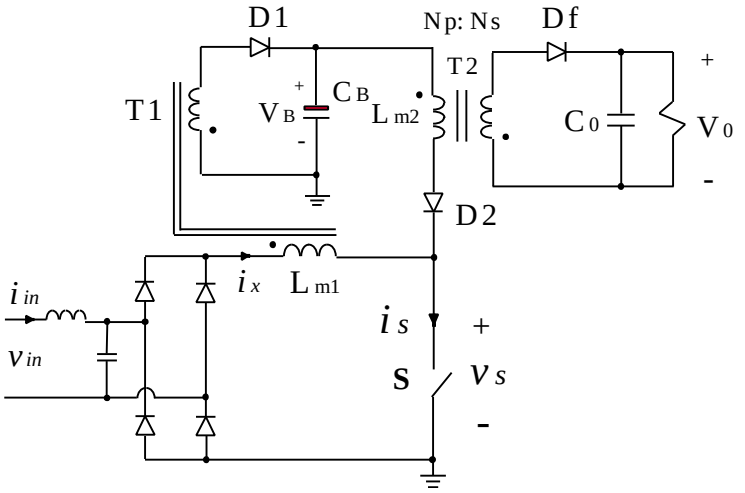
2.3 Integrated Single-Stage Power Factor Correction AC/DC Converter

2.3.1 Principle of Operation

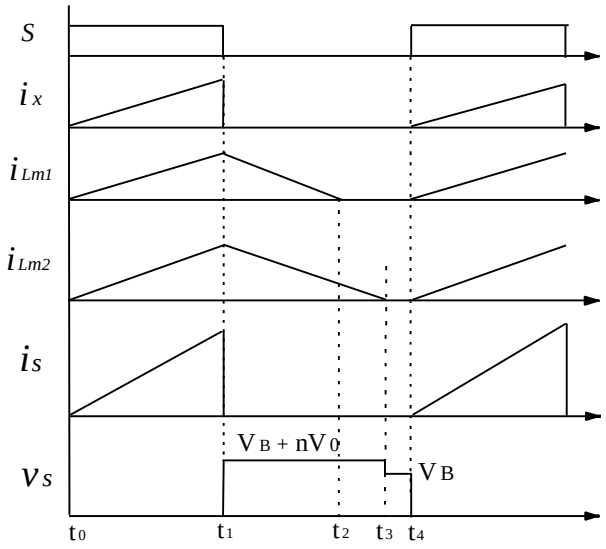
As discussed in the last section, the integrated single-stage DCM PFC + DCM DC/DC converter has no DC bus voltage stress. This feature is very attractive because low voltage rating devices and a 450V bulk capacitor can be used. However, the conduction loss and switching loss in the main switch increase, so the conversion efficiency may become low. In order to evaluate the performance of the integrated single-stage DCM PFC + DCM DC/DC converter, one DCM PFC + DCM DC/DC converter is analyzed, implemented and evaluated in the following.

Figure 2.5(a) shows the proposed integrated single-stage PFC rectifier. The power factor correction stage is composed of the input rectifier, coupled inductor T_1, diode D_1, and main switch S. The DC/DC conversion stage consists of D_2, main switch S, isolation transformer T_2,

output rectifier D_f, output filter C_0, and load. L_{m1} and L_{m2} are the magnetizing inductance of T_1 and T_2 respectively. The two stages share a common switch S to achieve power factor correction and tight output voltage. From its circuit structure, it is actually a flyback integrated with another flyback converter. The key waveforms of Fig. 2.5(a) are shown in Fig. 2.5(b). In the



(a)



(b)

Fig. 2.5 (a) The proposed integrated single-stage power factor correction rectifier

(b) The key switching waveforms

steady-state analysis, the rectified line input voltage is assumed constant in one switching cycle because the switching frequency is much higher than the line frequency. C_B is large enough that the voltage across C_B is constant. Four operation modes exist over one switching cycle.

M1 [t_0, t_1]: Switch S is turned on at t_0. Diode D_1 is reverse biased, and its reverse voltage is the sum of the voltage across the bulk capacitor C_B and the reflected line input voltage in the secondary winding of T_1. D_f is also in the off-state during this time interval. Both inductors L_{m1} and L_{m2} are linearly charged and begin to store energy. The current i_x is given by

$$\left| i_x(t) \right| = \frac{\left| v_{in} \right|}{L_{m1}} (t - t_0). \tag{2.1}$$

This mode terminates at t_1, where S is turned off.

M2 [t_1, t_3]: S is turned off at t_1, and L_{m2} first charges the parasitic capacitor of the MOSFET S until D_f is forward biased. The energy stored in L_{m2} then is delivered to the load while the energy stored in L_{m1} is transferred to the bulk capacitor C_B since i_{Lm1} cannot flow through the primary winding of T_2. At t_2, i_{Lm1} becomes zero and D_1 is naturally turned off, while i_{Lm2} continues to deliver its energy to the load, and its current linearly decreases until t_3, where i_{Lm2} reduces to zero, and D_f is naturally turned off.

M3 [t_3, t_4]: There is no current flow in the converter during this time period, until S is turned on again at t_4, where a new switching cycle starts.

From the above analysis, it can be seen that the rectified line current i_x is a right triangular waveform, and its average current over a switching period is given by

$$\left| i_{in} \right| = i_{x,ave} = \frac{\left| v_{in} \right| D^2}{2 L_{m1} f_s}, \tag{2.2}$$

where D and f_s are the duty ratio and the switching frequency, and $v_{in} = V_{in} \sin \omega_l t$, respectively. The duty ratio is almost constant over one line cycle since the input voltage V_B of the DC/DC stage only contains 2nd order line harmonics. Therefore, the average line input current automatically follows the line input voltage in a line cycle. Therefore, unity power factor can be automatically obtained.

2.3.2 Voltage Stress across the Bulk Capacitor C_B

If the DC/DC converter operates at CCM, the duty ratio doesn't change for a reduced load. The PFC stage still provides the same power as that of the heavy load because the duty ratio is the same. Therefore, the unbalanced power between the input and the output charges the bulk capacitor C_B, which causes the voltage of the bulk capacitor C_B to increase. To keep constant output voltage, the duty ratio is reduced, and the input power is also reduced until the input power equals the output power. Therefore, the new power balance is caused by the duty ratio reduction and the high DC bus voltage. Although this voltage stress can be controlled by using a variable switching operation, it is hard to optimize the EMI filter and the inductive components.

For this proposed converter, if the DC/DC stage operates in CCM, the bulk capacitor voltage can be calculated from

$$V_B = n\left(V_{in}\sqrt{\frac{V_0}{4\ f_s\ L_{m1}\ I_0}} - V_0 \right), \tag{2.3}$$

where I_0 and n are the load current and the turns ratio of N_p to N_s, respectively. It can be seen that V_B will be infinite at no load operation.

Figure 2.6 shows the voltage stress as a function of the load current. As is shown, the bus voltage is significantly dependent upon the load current. The bus voltage reaches nearly 1000V and a 2 kv device has to be used. In order to limit this voltage stress, switching frequency has to increase to compensate for the decrease of the load current from the equation (2.3). A wide switching frequency range is needed, however, and it is very difficult to optimally design the inductive components.

Now both the PFC stage and DC/DC stage operate in DCM, so the duty ratio D decreases when the load becomes light. As a result, the input power also decreases. There is no unbalanced power between the input and the output. There is no DC bus voltage stress at light load. In the following, the DC bus voltage will be mathematically calculated.

The bus voltage V_B can be calculated, based on equating the absorbed power from the ac line to the delivered power to the load in a half line cycle instead of in a switching cycle. The instantaneous input power over a switching period is given by

$$p_{in}(t) = \frac{v_{in}^2(t)\, D^2}{2\, L_{m1}\, f_s}. \tag{2.4}$$

The absorbed average power from the line input over a half line cycle is equal to averaging (2.4), which is

$$P_{in} = \frac{2}{T_L}\int_0^{T_L/2} p_{in}(t)\, dt\,, \tag{2.5}$$

where T_L is the line period. Substituting (2.4) into (2.5) yields

$$P_{in} = \frac{V_{in}^2\, D^2}{4\, L_{m1}\, f_s}. \tag{2.6}$$

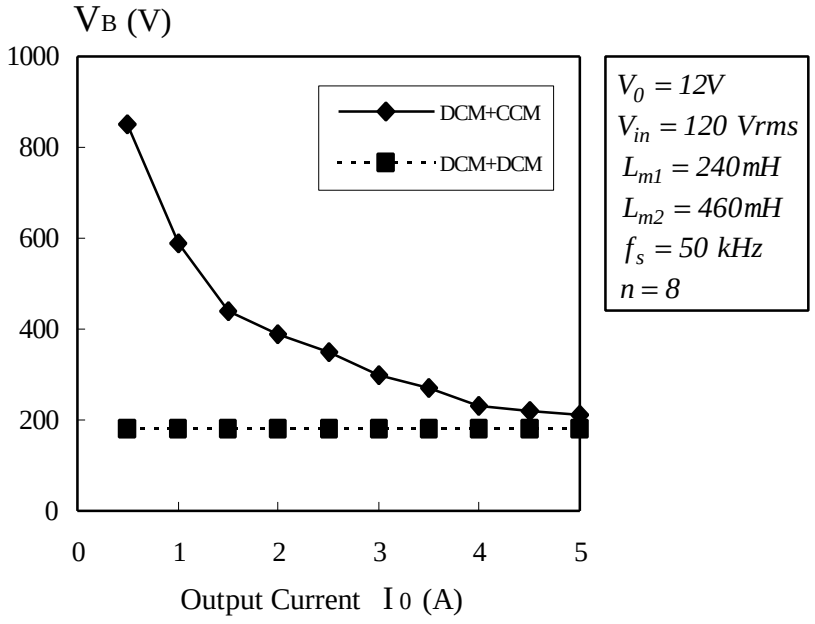


Fig. 2.6 The voltage stress across the bulk capacitor C_B

where V_{in} is the line peak voltage. The output power is the product of the average current through D_2 and the storage capacitor voltage. The average current through D_2 is given by

$$I_{d2} = \frac{D^2 V_B}{2 L_{m2} f_s}. \tag{2.7}$$

So the output power is

$$P_0 = \frac{D^2 V_B^2}{2 L_{m2} f_s}. \tag{2.8}$$

By equating (2.8) to (2.6), the bulk capacitor voltage V_B is determined by

$$V_B = V_{in}\sqrt{\frac{L_{m2}}{2 L_{m1}}}. \tag{2.9}$$

It can be seen that the voltage stress across the bulk capacitor C_B is dependent only on the ratio of two magnetizing inductors and is proportional to the input peak voltage. It is independent of the load condition. Therefore, by properly designing the ratio of two inductors, high voltage stress can be avoided. Figure 2.6 shows the voltage stress for this single-stage DCM PFC + DCM DC/DC converter. Compared with a DCM PFC + CCM DC/DC converter, this operation is very attractive.

2.3.3 Current Stress across the Main Switch

The peak switch current occurs with heavy load at the peak input voltage. The switch carries both input current i_{Lm1} and inductor current i_{Lm2} during its on-time period. So the peak switch current is given by

$$I_{s,peak} = \left(\frac{V_{in}}{L_{m1}} + \frac{V_B}{L_{m2}}\right)\frac{D}{f_s}. \tag{2.10}$$

The rms current is determined by averaging the rms switch current in one switching period over a half line period. The switch rms current in one switching cycle is

$$I_{s,rms}^{sw}(t) = \left(\frac{V_{in}|sinw\ t|}{L_{m1}} + \frac{V_B}{L_{m2}}\right)\frac{D}{f_s}. \tag{2.11}$$

Averaging (2.11) yields

$$I_{s,rms} = \left(\frac{2\,V_{in}}{p\,L_{m1}} + \frac{V_B}{L_{m2}} \right) \sqrt{\frac{D^3}{3\,f_s^2}}\,. \tag{2.12}$$

For the circuit parameters L_{m1} = 240 μH and L_{m2} = 460 μH, with the line input voltage from 90 V rms to 260 Vrms, the rms current of S is from 3A to 1.2A.

The conduction loss of S (MOSFET) is

$$P_{cond} = \left(\frac{2\,V_{in}}{p\,L_{m1}} + \frac{V_B}{L_{m2}} \right)^2 \frac{D^3 R_{on}}{3\,f_s^2}, \tag{2.13}$$

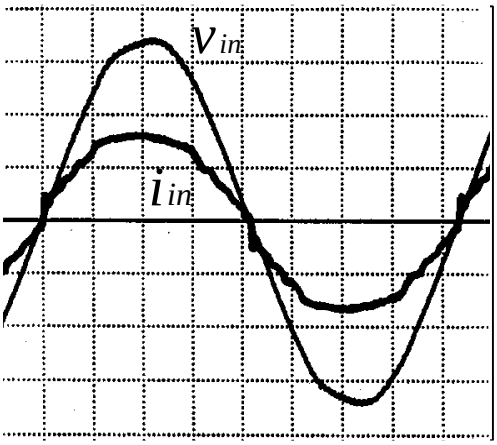
where R_{on} is the on-resistance of the MOSFET, which is obtained for its operating conditions from the data book.

2.3.4 Experimental Verification

In order to verify the circuit operation, a 60-watt, 12V output voltage prototype was implemented at the constant frequency of 53.5 kHz with universal line input. The designed circuit parameters are

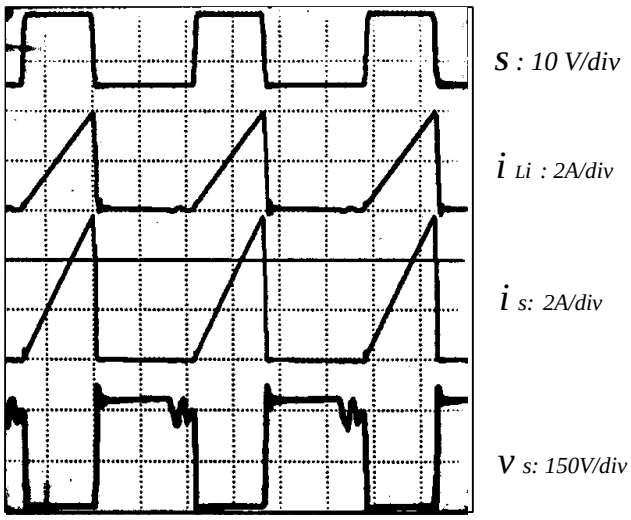
L_{m1}=240 μH	L_{m2} = 460 μH	C_B=100 μF/450V
n = 8	f_s = 53.5 kHz	V_{in} = 90 V- 260 V rms

The measured line input current waveforms and switching current waveforms are shown in Fig. 2.7. It can be seen that the input current follows the line input voltage. The power factor, total harmonic distortion (THD), efficiency over universal input line voltages, and the DC bus voltage over load variation with high line input are shown in Fig. 2.8. It can be seen that 0.99 power factor and low THD can be achieved over universal line input. The measured harmonic components of the line input current are much lower than those of IEC1000-3-2 Class D requirement. The efficiency is about 75% with 60-watt and 12V output for the input voltages from 90 to 260V. The measured bulk capacitor voltage V_B over load variation at high line input is always less 380V, so a 450V bulk capacitor can be used. It can be seen that this DC bus voltage is almost independent of the load, which verifies the theoretical analysis. Besides, this converter can operate even without load and still get regulated output voltage without any bus



t: 2 ms /div v_{in}*: 50 V/div* i_{in}*: 0.5 A/div*

(a)



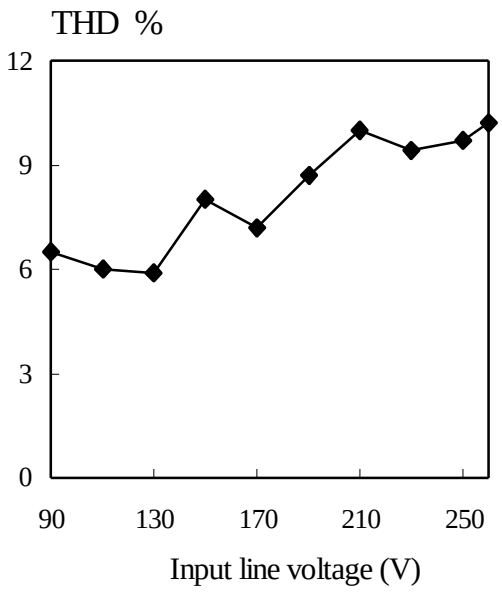
5 ms/div

(b)

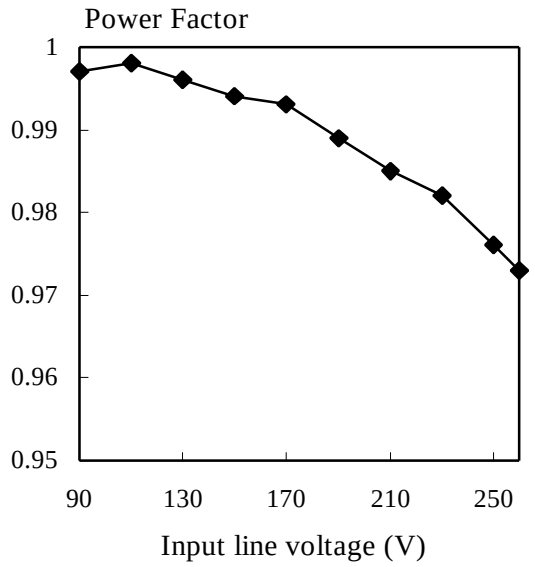
Fig. 2.7 Experimental waveforms

(a) The measured line input current waveform

(b) The measured switching waveforms



(a)



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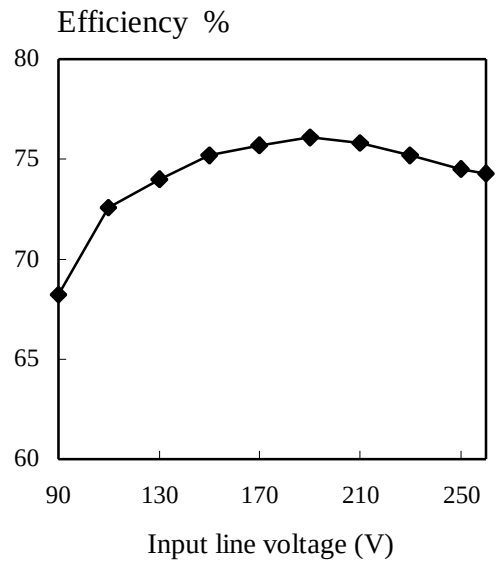
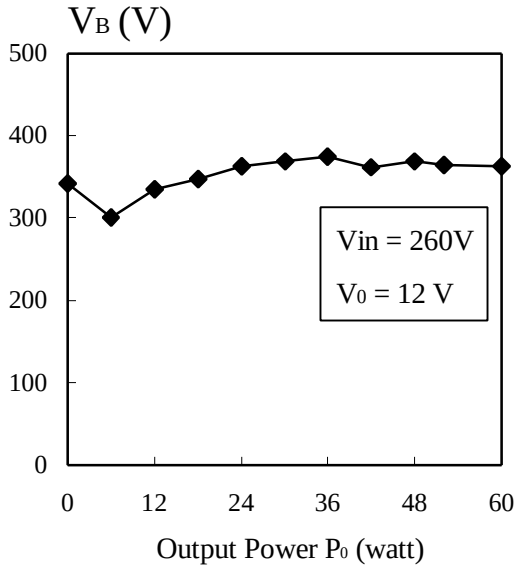


(c)



(d)

Fig. 2.8 The experimental results

(a) Total harmonic distortion

(b) Power factor over universal line input

(c) Efficiency over universal line input

(d) DC bus voltage over load variation

voltage stress. Figure 2.9 shows the predicted efficiency with 60-watt, 5V output. It can be seen that the efficiency is still higher than that of a DCM PFC + CCM DC/DC converter with switching frequency control. But the efficiency is lower than 70% due to the high conduction loss of DCM operation, which is the main disadvantage of this converter. In the following section, a new method, DC bus voltage feedback to suppress the DC bus voltage, will be proposed to improve the efficiency.

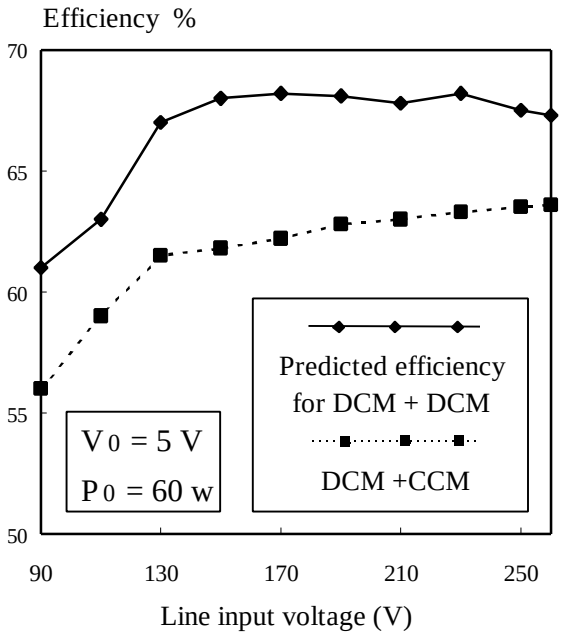


Fig. 2.9 Efficiency for a DCM PFC + DCM DC/DC converter with 60-watt and 5V output

2.4 Single-Stage Single-Switch Power Factor Correction (S^4-PFC) Converter with DC Bus Voltage Feedback

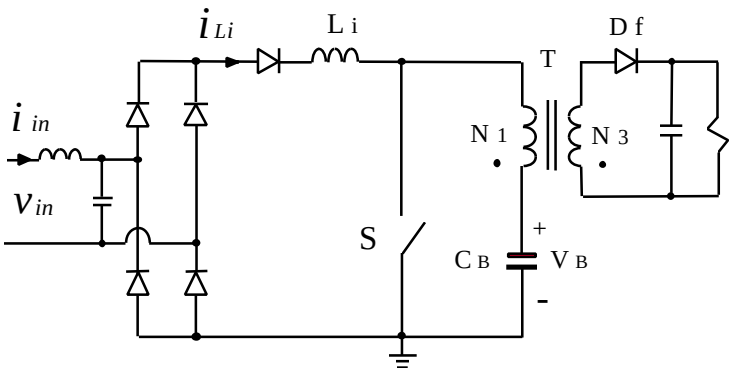
2.4.1 DC Bus Voltage Feedback Concept

Figure 2.10 (a) shows the BIFRED converter [B1]. It actually integrates a DCM boost converter with a DC/DC converter. When S is turned on, the rectified line input voltage is applied to $L_{i,}$ and the inductor current i_{Li} linearly increases. The magnetizing current of the flyback

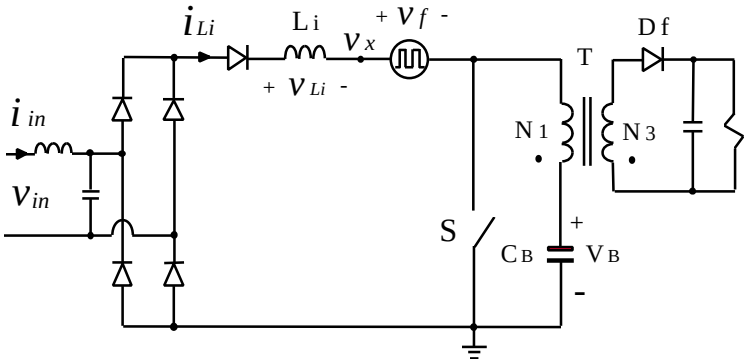
converter linearly increases too. Therefore, both input choke L_i and magnetizing inductor L_m store their energy independently during the switch on-time interval. When the switch is turned off, the energy stored in L_i and L_m is delivered to C_B and the load, respectively. From its operation principle, the input power is controlled only by the duty cycle and L_i. Although it is a single-stage PFC converter, the PFC stage really does not know whether the load is low or high. So, as discussed before, the high DC bus voltage exists for this integrated DCM boost with a CCM flyback converter. If the PFC stage is inherently able to reduce the input power automatically when the load becomes light, then the DC bus voltage can be suppressed. One way is to reduce the voltage across L_i during the switch on-time period at light load so that the energy absorbed from the line input is also reduced. One implementation is to insert a voltage source v_f in series with the inductor L_i, as shown in Fig. 2.10(b). The amplitude of v_f should be proportional to the DC bus voltage. The v_f waveform is shown in Fig. 2.10(c). It is shown that the applied voltage in L_i is the rectified line voltage minus the feedback DC bus voltage during the S on-time period. The inductor current is given by

$$i_{Li} = \frac{|v_{in}| - nV_B}{L_i}(t - t_0) \qquad t_0 < t < t_1 . \tag{2.14}$$

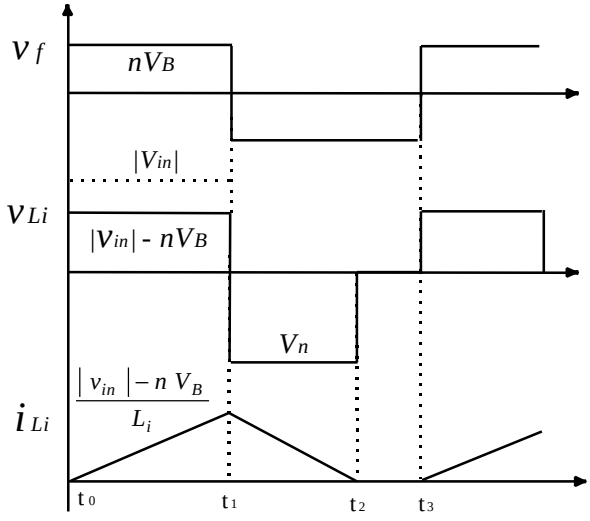
Thus, the input rectified line current decreases when the DC bus voltage increases at light load. The input power can be reduced through this negative feedback, so as to reduce the bus voltage stress. The negative feedback signal can be easily obtained by employing a feedback winding coupled with the isolated transformer, because the DC bus voltage is applied to the primary winding when the switch is on. Figure 2.11 shows the proposed S^4-PFC converter using the negative DC bus voltage feedback concept to limit the DC bus voltage at light load. By properly designing the turns ratio between the primary winding N_1 and the feedback winding N_2, a suitable feedback DC bus voltage can be obtained.



(a)



(b)



(c)

Fig. 2.10 (a) Integrated DCM boost with flyback converter

(b) The integrated PFC converter with DC bus voltage negative feedback

(c) Switching waveforms of (b)

2.4.2 S^4-PFC BIFRED AC/DC converter with DC bus voltage feedback

Figure 2.12(a) shows the proposed S^4-PFC BIFRED converter with DC bus voltage feedback as an example. The proposed converter is actually a BIFRED converter with an added feedback winding N_2. The feedback winding N_2 is used to detect the DC bus voltage as a feedback signal. The PFC stage is actually a boost converter operating in discontinuous current mode (DCM) to achieve power factor correction while the DC/DC stage operates in CCM. When the load becomes light, as discussed in the last section, the duty ratio does not change. As a result, the PFC stage provides more power than the load needs. This unbalanced power between the input and the output will be stored in the bulk capacitor, which increases the DC bus voltagevoltage. This DC bus voltage increase will decrease the duty ratio. Furthermore, the absorbed energy in the input inductor becomes small since the charging voltage across the inductor is the rectified line input voltage minus the partial DC bus voltage. This negative feedback helps reduce the DC bus voltage stress at light load. Another major advantage is that

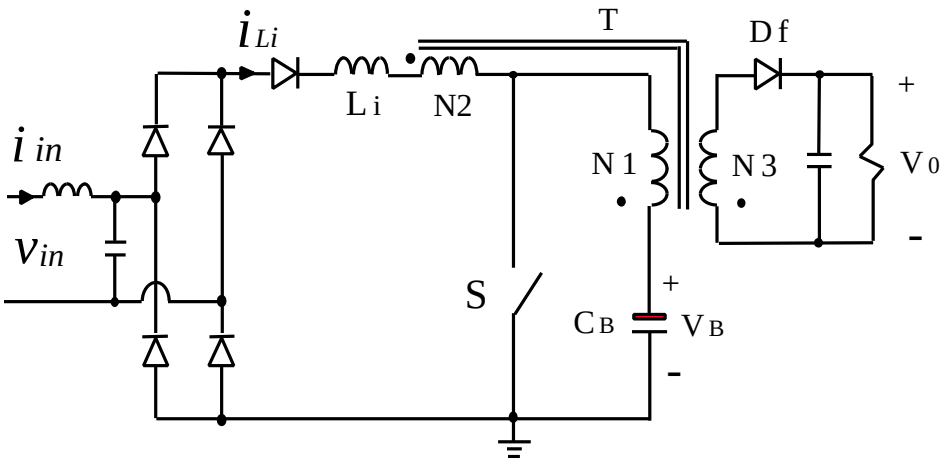
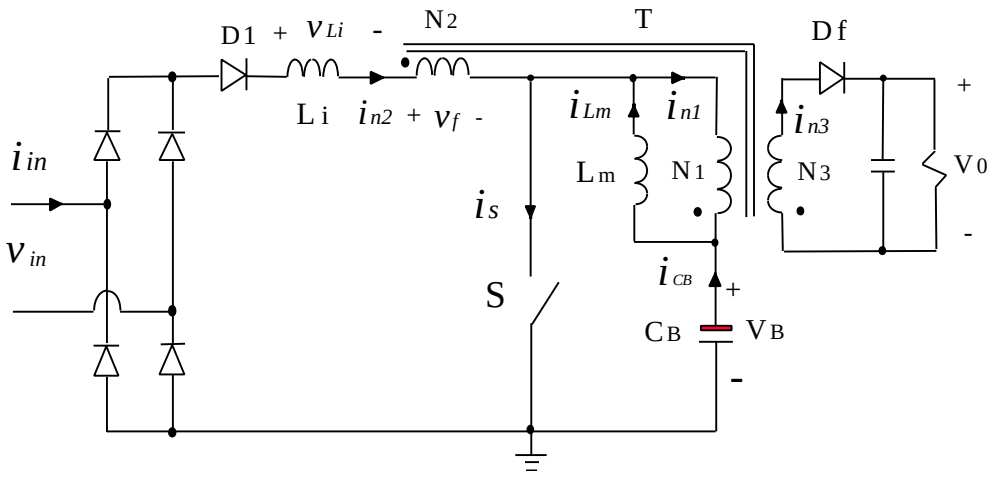
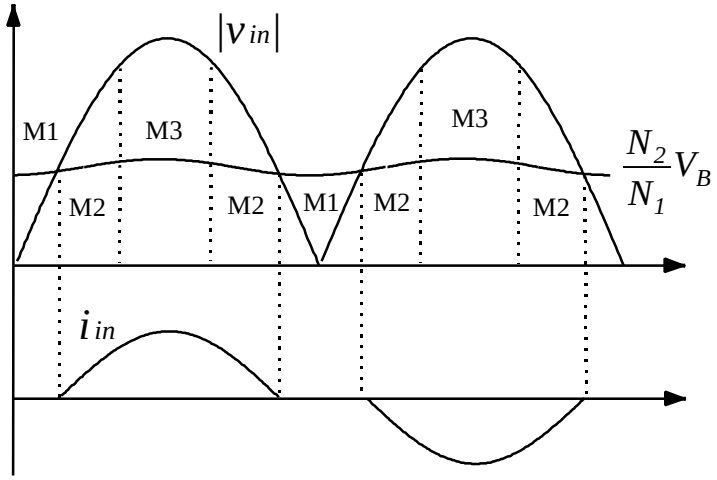


Fig. 2.11 The proposed S^4-PFC AC/DC converter with DC bus voltage feedback



(a)



(b)

Fig. 2.12 (a) S^4-BIFRED PFC converter with DC bus voltage feedback

(b) Line input current waveform and operation mode regions

the feedback winding can reduce the switching current stress. The feedback winding provides the input power directly to the load without being processed by the switch so that the designed PFC converter has potential high efficiency. This function will be analyzed in the following. In order to fully understand the circuit, the converter operation will be analyzed according to its possible three operational modes, M1, M2, and M3, as shown in Fig. 2.12(b).

M1: This mode happens near the zero crossing of the line voltage, where the DC bus feedback signal v_f is higher than the rectified voltage, $|v_{in}| < v_f = \frac{N_2}{N_1} V_B$. D_1 is reverse biased, and there is no line input current. The equivalent circuit is just the simple DC/DC flyback converter. During the switch on-time period, the magnetizing current linearly increases while the energy stored in L_m will be delivered to the load during the switch off-time interval. Therefore, the load power is solely provided by C_B.

M2: When the rectified line voltage is higher than the feedback voltage v_f, $|v_{in}| > v_f = \frac{N_2}{N_1} V_B$, the converter enters mode 2 operation. During this mode, the load power is provided not only by the bulk capacitor C_B but also by the line input. The switching waveforms are shown in Fig. 2.13. Here, the isolation transformer T is modeled as an ideal transformer with an external magnetizing inductor L_m.

When the switch S is turned on at t_0, the DC bus voltage is applied to the magnetizing inductor L_m, which causes the magnetizing current i_{Lm} to linearly increase. Assume the DC/DC converter operates in CCM. This magnetizing current is given by

$$i_{Lm} = \frac{V_B}{L_m}(t - t_0) + I_{Lm}(t_0). \tag{2.15}$$

The voltage v_{Li} across L_i is the rectified line voltage minus the feedback voltage across N_2, which is given by

$$v_{Li} = |v_{in}| - \frac{N_2}{N_1} V_B. \tag{2.16}$$

So the rectified line current, also the winding current i_{n2}, linearly increases from zero since the PFC stage operates in DCM. This current can be expressed as

$$i_{n2} = \frac{|v_{in}| - nV_B}{L_i}(t - t_0), \tag{2.17}$$

where $n = \frac{N_2}{N_1}$. On the other hand, D_f is reverse biased, and there is no current flow through the winding N_3, $i_{n3} = 0$. Since N_1, N_2, and N_3 are composed of an ideal transformer, based on Amper's law, it has

$$N_1 i_{n1} - N_2 i_{n2} - N_3 i_{n3} = 0 \tag{2.18}$$

Substituting i_{n2} and i_{n3} into (2.18) gives

$$i_{n1} = \frac{N_2}{N_1} i_{n2} \tag{2.19}$$

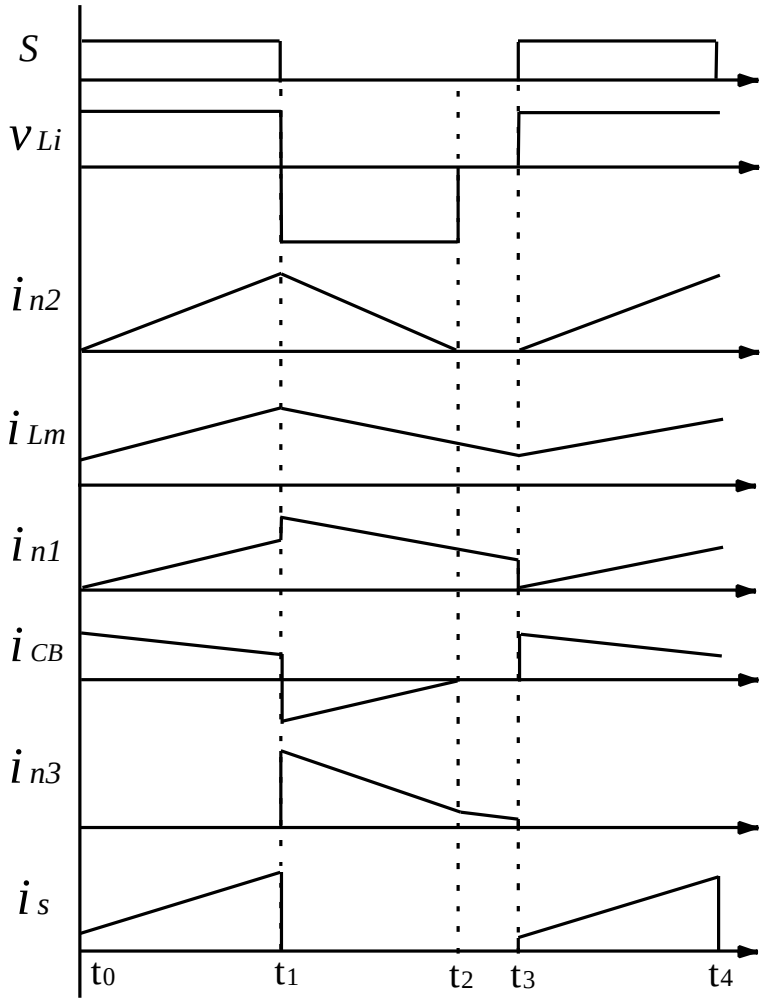


Fig. 2.13 Switching waveforms of M2

Thus, the magnetizing current i_{Lm} is given by

$$i_{Lm} = \frac{N_2}{N_1}\, i_{n2} + i_{CB}. \tag{2.20}$$

From (2.20), it can be seen that the magnetizing current i_{Lm} is provided by the discharging current from C_B and the line input current, which means that the stored magnetizing energy is not only from C_B but also from the line input. Both i_{CB} and i_{n1} contribute to the magnetizing current. Here $\frac{N_2}{N_1} i_{n2}$ is assumed to be always smaller than i_{Lm} since the rectified line input current is not enough higher.

The current through the main switch is

$$i_s = i_{n2} + i_{CB}. \tag{2.21}$$

Substituting i_{n2} and i_{CB} into (2.21) yields

$$i_s = \frac{N_1 - N_2}{N_1} i_{n2} + i_{Lm}. \tag{2.22}$$

This switching current stress is smaller than that of the BIFRED converter, where $N_2 = 0$. Therefore, the conduction loss and switching losses are minimized, and the efficiency is improved correspondingly.

When S is turned off at t_1, D_f begins to be forward biased. The voltage across L_i is

$$v_{Li} = \mid v_{in} \mid - \frac{N_1 - N_2}{N_3} V_0 - V_B. \tag{2.23}$$

This negative voltage resets the choke current i_{n2} to zero at t_2, and this current i_{n2} also charges the bulk capacitor C_B. The magnetizing current i_{Lm} linearly decreases because a reflected negative output voltage is applied to N_1. This magnetizing current is given by

$$i_{Lm} = -\frac{kV_0}{L_m}(t - t_1) + I_{Lm}(t_1), \tag{2.24}$$

where $k = \frac{N_1}{N_3}$. During this time period, i_{n1} is equal to the sum of i_{Lm} and i_{n2}. Again based on Amper's law, i_{n3} is given by

$$i_{n3} = \frac{N_1 - N_2}{N_3} i_{n2} + \frac{N_1}{N_3} i_{Lm}. \tag{2.25}$$

Equation (2.25) shows that the load absorbs energy not only from the magnetizing inductor but also from the line input. Therefore, there is direct power transfer from the line input to the load during the switch off-time interval. As a result, the efficiency can be improved.

At t_3, the choke current i_{n2} decreases to zero, and only the magnetizing energy is transferred to the load until the switch is turned on again at t_4.

As the line voltage further increases, the third mode may occur, depending upon the selection of the inductance L_i. M2 operation terminates when i_{n1} exceeds the magnetizing current i_{Lm} during the switch on-time period.

M3: This mode may occur near the line peak voltage, where the rectified line current is high enough that the line voltage provides most of the energy to the load, and the bulk capacitor C_B is in the charge mode. The switching waveforms are shown in Fig. 2.14. In this mode, the current i_{n1} through N_1 exceeds the magnetizing current i_{Lm} during the on-time interval of S. The current difference between i_{n1} and i_{Lm}, which is given by

$$D\, i = \frac{N_2}{N_1} i_{n2} - i_{Lm}, \tag{2.26}$$

will charge the bulk capacitor C_B. It is shown that i_{n1} reaches the magnetizing current i_{Lm} at t_{01}. Thus, both C_B and the line input provide energy to the magnetizing inductor during the time period from t_0 to t_{01}. However, the line input current totally supplies the magnetizing current and also charges the bulk capacitor C_B during the time interval from t_{01} to t_1. Therefore, the line input not only provides the energy to the load but also charges the bulk capacitor C_B as well. When the line voltage passes the line peak voltage, this mode ends and the converter enters Mode M2 operation. If the line voltage decreases further, then the converter will operate in Mode M1.

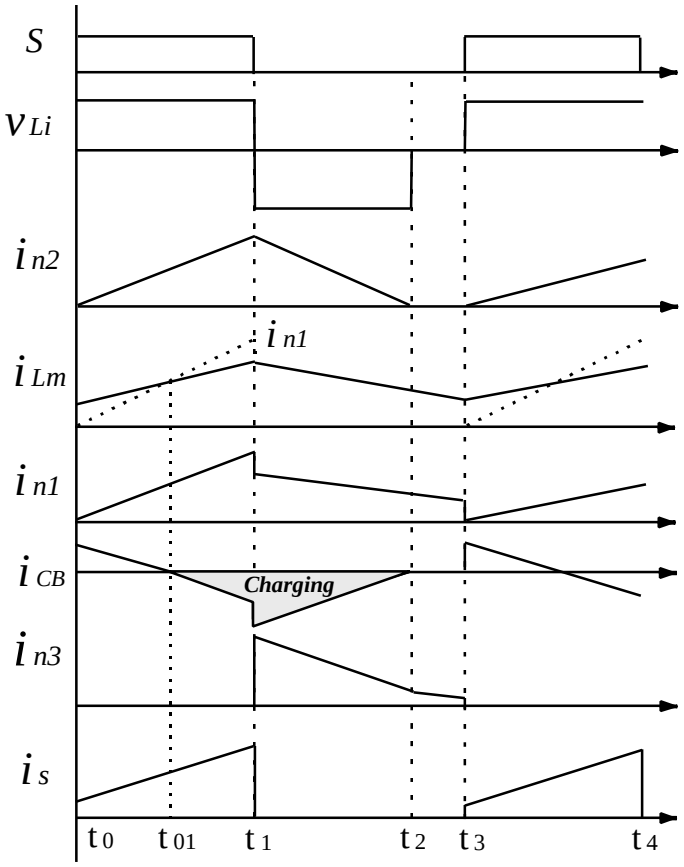


Fig. 2.14 Switching waveforms of Mode M3

Based upon the above analysis, it can be seen that there is no input current near the zero crossing of the line input voltage, because the feedback voltage is higher than the rectified line input voltage. As a result, the input current waveform distortion increases. The higher the feedback voltage v_{n2} (high turns ratio of N_2 and N_1), the higher the distortion. If $N_2 = N_1$, there is no power factor correction function; the converter simply becomes a conventional AC/DC converter, and there is no DC bus voltage stress at any load operation. Besides, the main switch deals only with the current from the DC/DC stage, and it has less current stress. If $N_2 = 0$, the converter becomes the BIFRED converter and very low THD and good power factor can be achieved. All line input harmonics are much lower than IEC 1000-3-2 Class D requirements. However, it suffers from high DC bus voltage at light load, and the main switch suffers from high current stress not only from the PFC stage but also from the DC/DC stage. It has maximum

current stress. Therefore, there is a trade-off among the input current distortion (THD), DC bus voltage, and switch current stress. By properly choosing the turns ratio of N_1 and N_2, the designed S^4-PFC AC/DC converter can satisfy the IEC1000-3-2 Class D requirement and have low DC bus voltage with less current stress.

2.4.3 Topology Variation

Several topologies can be derived, based on the concept of using DC bus voltage negative feedback to control the DC bus voltage stress. Actually, this concept could be extended to any S^4-PFC converter, as long as the PFC function is based on the DCM boost converter. It can be implemented by simply inserting a feedback winding in series with the input inductor, while its voltage polarity is against the rectified line voltage when the switch is on. Figures 2.15 (a) [B20] and (b) [B21] are two implementations using the DC bus voltage feedback concept. Figure 2.15 (c) shows the magnetic switch PFC AC/DC converter [B18]. However, if $N_2 < N_1$, then there is a DC bus voltage feedback mechanism to suppress the DC bus voltage at light load, and power is transferred directly to the load without being processed by the switch. The original magnetic switch PFC converter suffered from high DC bus voltage at light load because $N_1 = N_2$. This converter has no DC bus voltage stress at light load if $N_2 < N_1$ and their turns ratio is properly designed. They are significant different although the topologies are the same. Figure 2.15 (d) is another topology using the same concept. The forward versions of these topologies also have the PFC function, low DC bus voltage, and tight output voltage.

2.4.4 Experimental Verification

In order to verify the proposed concept and circuit operation, The circuit shown in Fig. 2.12(a) was designed and implemented with 5V, 12A output for universal line applications. The designed parameters are

L_i = 125 μH, N_1 = 34 T, N_2 = 12 T, N_3 = 2 T,

S: IRFPE50 (800V), T: TDK PC40 PQ25/26, D_f: 30CPQ40 (30A/40V).

The measured line current waveforms for 110V, 200V, and 260V line input voltage are shown in Fig. 2.16. It can be seen that there is no line current near the zero crossing of the line voltage due to the bus voltage feedback. Fig. 2.17(a) shows the measured line input current harmonic

components at different line inputs. All the line current harmonics are below the IEC 1000-3-2 Class D requirement for universal line input. The measured efficiency, as shown in Fig. 2.17(b), is about 71% over universal line input. The measured THD and power factor over universal line input voltages are shown in Fig. 2.17 (c) and (d), respectively. It can be seen that THD and power factor are almost independent of the line voltage. This feature is very desirable.

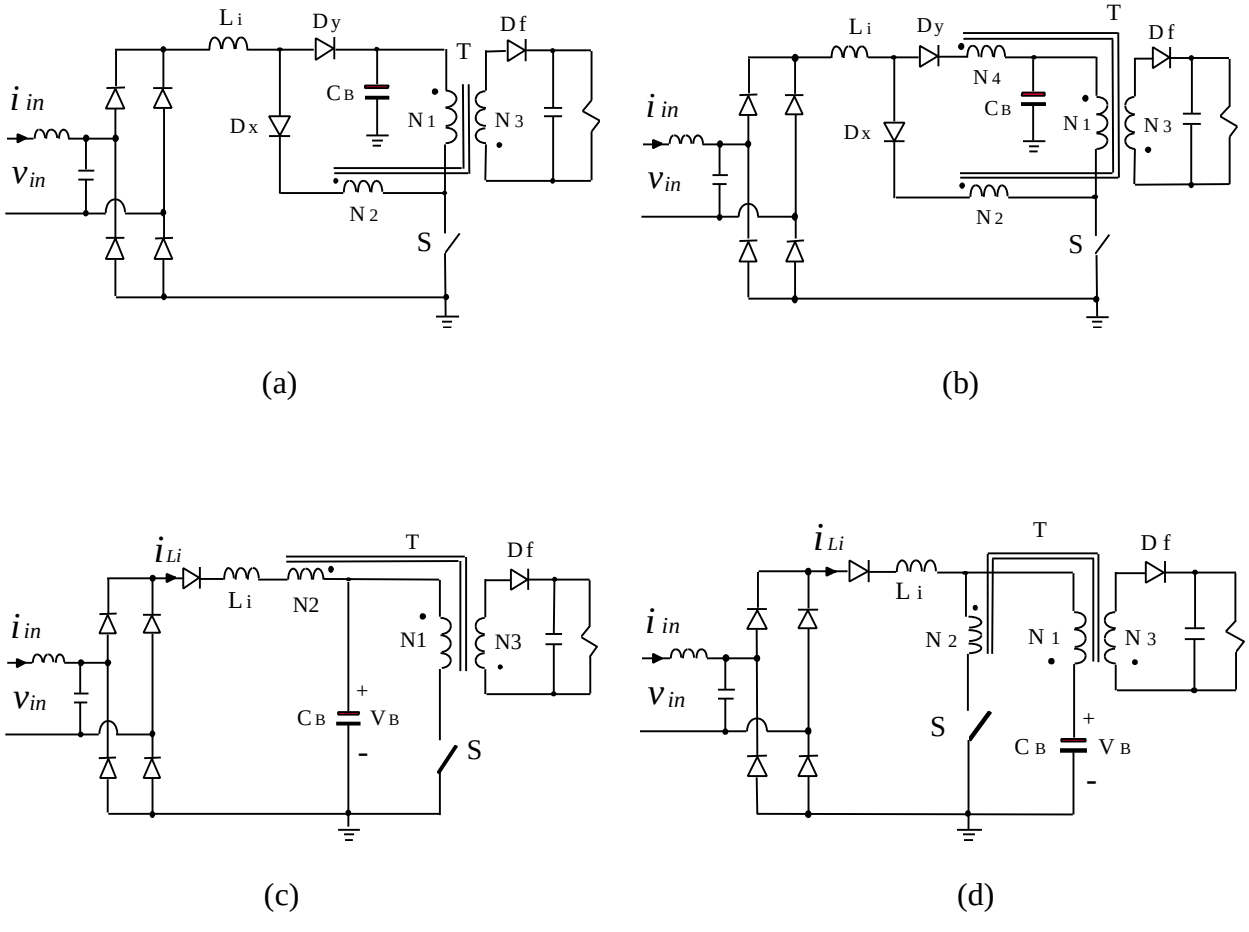
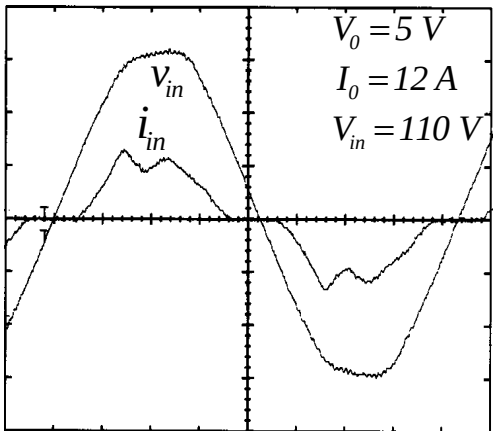


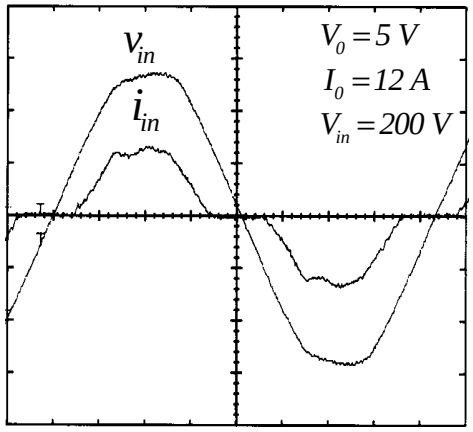
Fig. 2.15 Single-stage single-switch PFC AC/DC converters with DC bus voltage feedback

Figure 2.18(a) shows the DC bus voltage with load variation for 260V input. It is shown that the maximum DC bus voltage is 405V, so a 450V rated bulk capacitor can be used. Figure 2.18(b) shows the efficiency with 5V, 12A output over universal line input. It can be seen that the DCM PFC + CCM DC/DC converter has the lowest efficiency due to its wide range switching frequency operation [B2, B5]. The predicted efficiency is around 67% for the DCM PFC + DCM DC/DC converter [B17] because it has higher conduction loss and switching loss.



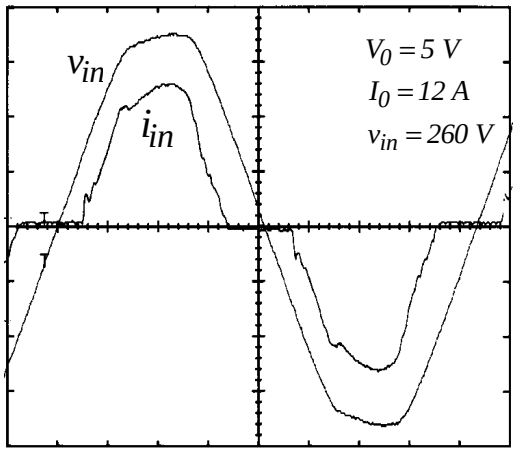
v_{in}: 50 V/div i_{in}: 1 A/div

(a) V_{in} = 100 V



v_{in}: 100 V/div i_{in}: 0.5 A/div

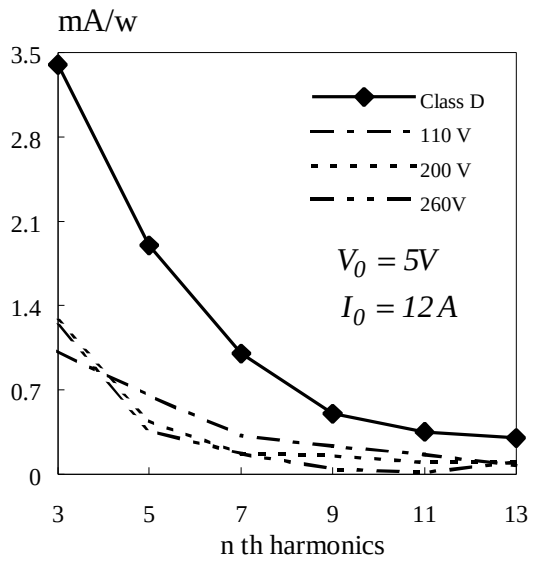
(b) V_{in} = 200V



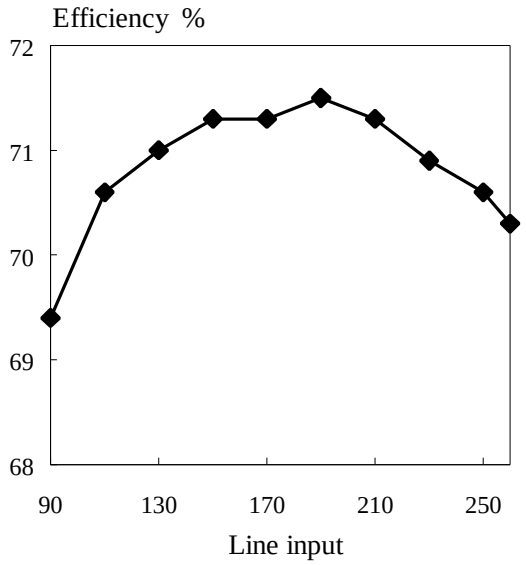
v_{in}: 100 V/div i_{in}: 0.2 A/div

(c) V_{in} = 260 V

Fig. 2.16 The measured line input current waveforms



(a)



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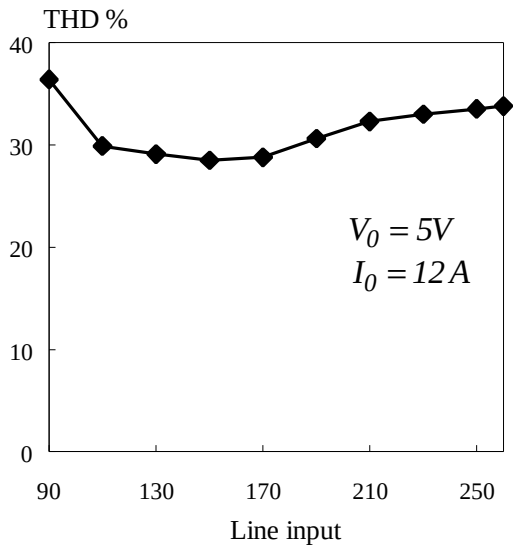
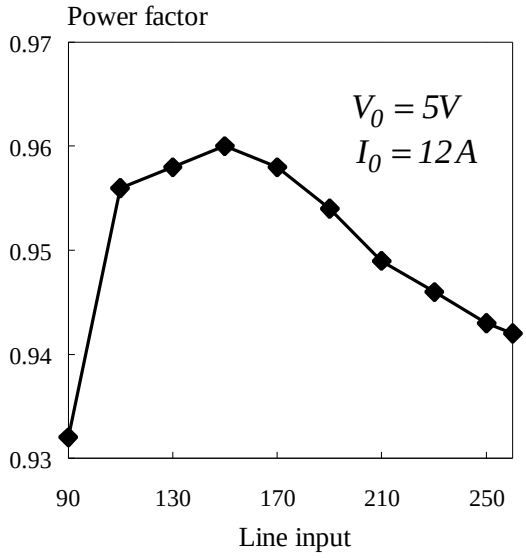


(c)



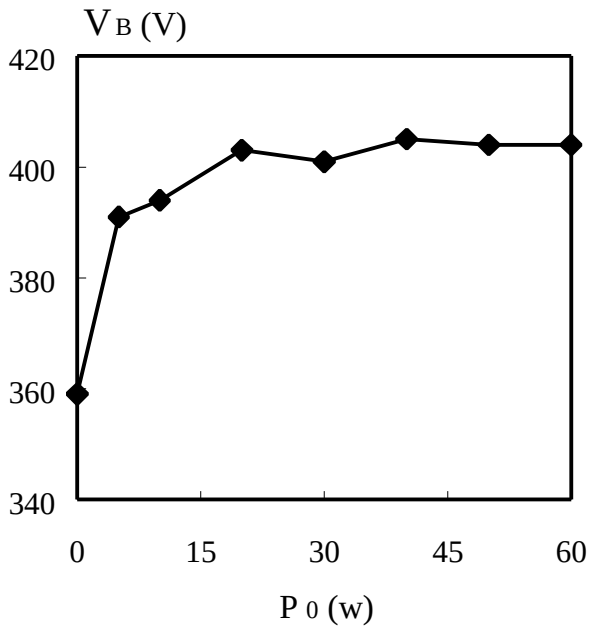
(d)

Fig. 2.17 (a) The measured input line current harmonics

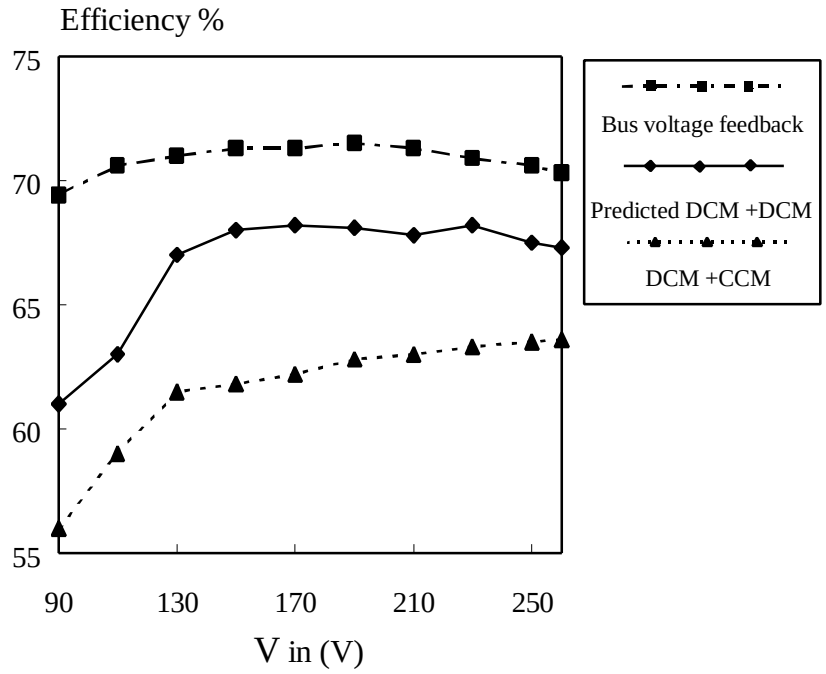
(b) The measured efficiency

(c) The measured Total Harmonic Distortion (THD)

(d) The measured power factor



(a)



(b)

Fig. 2.18 (a) DC bus voltage stress over load variation with 260V line input

(b) Efficiency comparison

It has very good power factor and extremely low THD. The measured harmonics of line input current are far below the IEC1000-3-2 Class D requirement. Also, it has no DC bus voltage stress at light load, so low voltage rating devices can still be used. The main disadvantage of the DCM PFC + DCM DC/DC converter is high conduction loss, which decreases the overall efficiency. The DCM PFC + CCM DC/DC converter with DC bus voltage feedback has the highest efficiency. The main reason is that there is a direct power transfer from the line input to the load through the feedback winding, and this direct transferred power is not processed by the main switch. Thus, the switching current stress is reduced, which reduces the loss in the main switch. The DC bus voltage stress can be suppressed within 410V, so low voltage rating devices can be used. However, the input current harmonic components are bigger than those of the DCM PFC + DCM DC/DC converter due to the distortion near the zero crossing of the line voltage. The DC bus voltage feedback both suppresses the DC bus voltage and deteriorates the input current harmonics. There is a trade-off between the DC bus voltage and THD. The design goal is tokeep the DC bus voltage as low as possible while ensuring that the line input current satisfies the IEC 1000-3-2 requirement. Therefore, the proposed DCM PFC + CCM DC/DC converter with DC bus voltage feedback has a potentially low cost and better performance.

2.5 Summary

For S^4-PFC AC/DC converters, the DC bus voltage is one of the most important issues. It is determined by the power balance between the input and the output. Usually, S^4-PFC AC/DC converters suffer from high DC bus voltage stress at light load. The DC bus voltage stress was analyzed for different PFC stage and DC/DC stage operations. It was shown that DCM PFC + CCM DC/DC converters have the highest voltage stress across the bulk capacitor, but they have very good THD. The DCM PFC + DCM DC/DC converters have no DC bus voltage stress, since the PFC stage and DC/DC stage are able to balance the input power and the output power. However, they suffer from high conduction loss, and the efficiency is still lower than that of DCM PFC + CCM DC/DC converter with DC bus voltage feedback. The CCM PFC + CCM DC/DC converter has no voltage stress, but it is difficult to find a converter that has an inherent power factor correction function.

Another way to suppress the DC bus voltage stress is to use DC bus voltage feedback in the power stage. The DC bus voltage feedback concept was proposed. One S^4-PFC AC/DC converter was analyzed, implemented, and tested. The analysis showed that there is a trade-off between the DC bus voltage stress and THD. The design criterion is to suppress the DC bus voltage as low as possible while keeping the input current harmonics below IEC1000-3-2 Class D requirements. Using DC bus voltage feedback concept, power is transferred directly from the line input to the load without being processed by the main switch. As a result, the current stress is minimized, and efficiency is improved. Therefore, S^4-PFC AC/DC converters with DC bus voltage feedback perform well, providing low DC bus voltage stress at light load, reasonable input current harmonics, and high efficiency with universal line input.

CHAPTER 3

VOLTAGE SOURCE CHARGE PUMP POWER FACTOR CORRECTION (VS-CPPFC) CONVERTERS

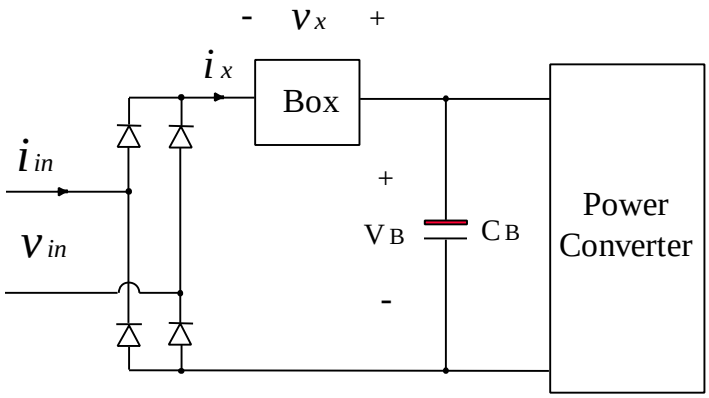
3.1 Introduction

The typical power factor correction converter uses an inductor in series with the line diode rectifier to shape the line input waveform to achieve power factor correction. For single-stage PFC converters, the boost inductor operates in DCM, So the inductor is usually bulky, heavy, inefficient, and expensive. It is attractive to investigate new PFC techniques employing a capacitor, since a capacitor is usually cheaper than an inductor. Intuitively, the comparable network of an inductor in series with a line rectifier is a capacitor in parallel with the line rectifier. This chapter presents a voltage source charge pump power factor correction (VS-CPPFC) technique using a charge pump capacitor. First, the basic charge pump power factor correction (CPPFC) converter is derived. Then, the condition for achieving unity power factor is analyzed and derived. The clamping technique is used to satisfy the unity power factor condition. Two types of VS-CPPFC converters -AC/DC converters and electronic ballasts- are proposed, analyzed, designed, and implemented. A family of VS-CPPFC converters is also presented.

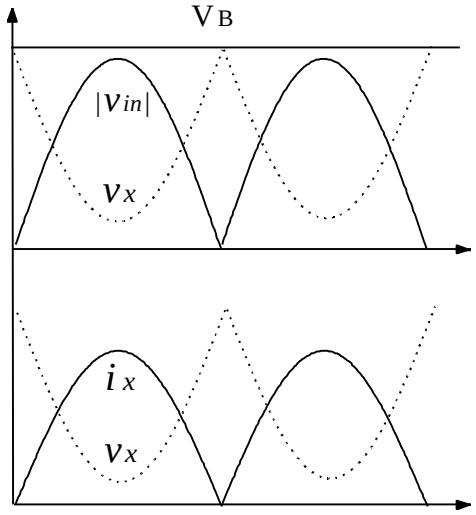
3.2 Derivation of the Voltage Source Charge Pump Power Factor Correction Converter

Figure 3.1(a) shows the power factor correction AC/DC converter block diagram. Usually, the DC bus voltage V_B is designed to be higher than the line peak voltage, so, the output voltage of the box is equal to the DC bus voltage minus the ac rectified line voltage. In order to achieve power factor correction, the rectified line current i_x should be a rectified sinusoidal waveform in phase with the rectified line voltage. The output characteristics of the box that are therefore required as shown in Fig. 3.1(b). To achieve unity power factor, the box should have high output voltage near the zero crossing of the line voltage, which corresponds to the light load

of the box, and low output voltage near the peak line voltage, which corresponds to the heavy load for the box. The question is what type of converter has these particular output characteristics to match the required curves ? Of the many topologies examined, the resonant converters have the required output characteristics for v_x and i_x. Figure 3.2(a) shows the power factor correction AC/DC converter [B24], where the box was replaced by a series resonant converter. Based upon the DC voltage gain characteristics of the series resonant converter, shown in Fig. 3.2(b), it can be seen that the series resonant converter has higher output voltage at



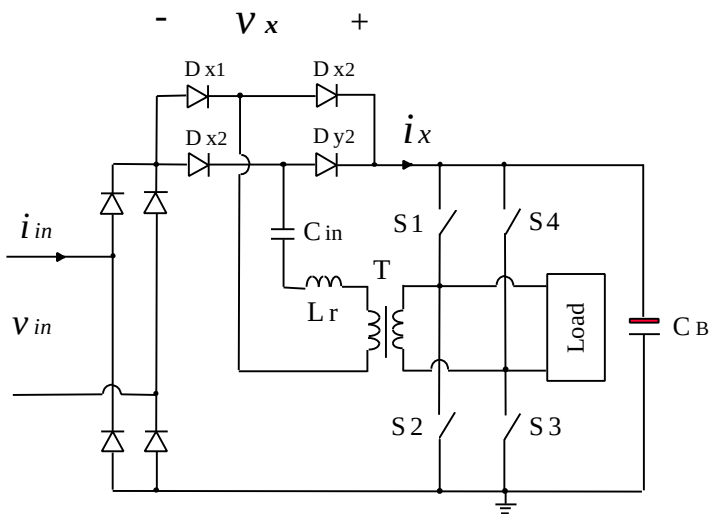
(a)



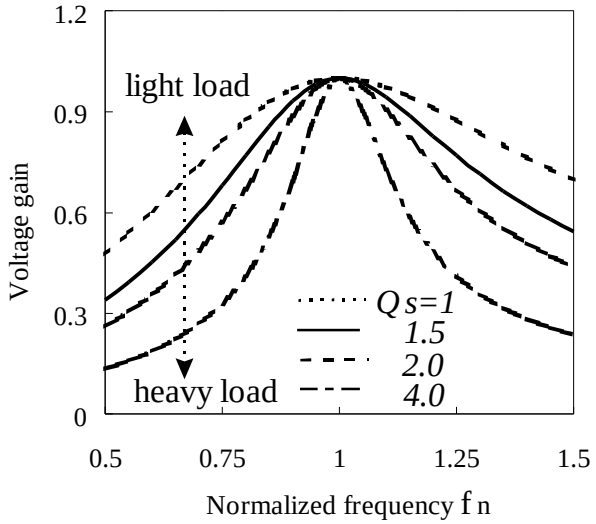
(b)

Fig. 3.1 (a) The power factor correction converter block diagram

(b) The required output characteristics to achieve power factor correction



(a)



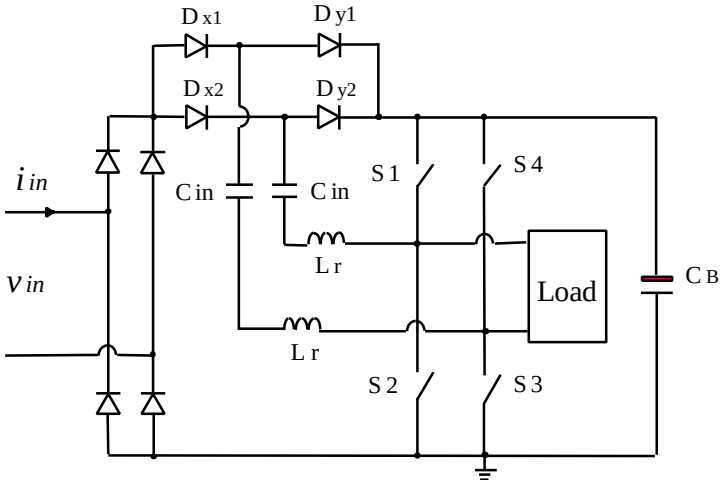
(b)

Fig. 3.2 (a) Power factor correction AC/DC converter

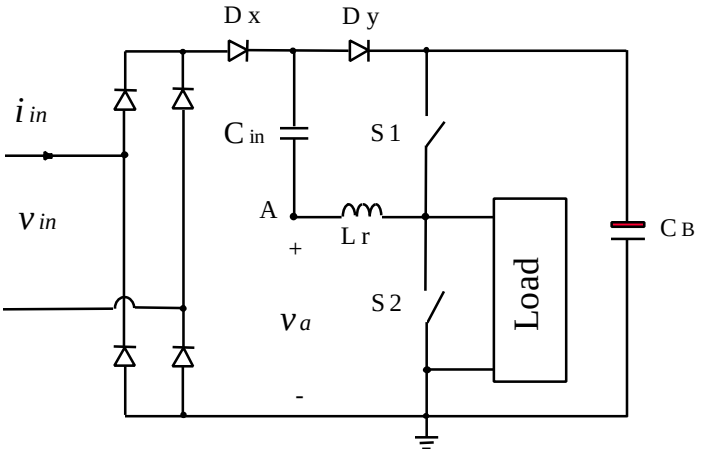
(b) The DC gain characteristics of the series resonant converter

light load near the zero crossing of the line voltage, while it provides low output voltage at heavy load near the peak line voltage. These output characteristics roughly match the required curves of Fig. 3.1(b). Therefore, this converter has an inherent power factor correction function. If the resonant inductor L_r and capacitor C_{in} are split into two series inductors and capacitors, then the isolated transformer can be eliminated, as shown in Fig. 3.3(a). This circuit is good for high-

power applications because of the full-bridge configuration. However, a half-bridge converter is preferred for low-power applications, so, one resonant tank, one switch leg (S_3, S_4), and a pair of of output rectifiers (D_{x1}, D_{y1}) can be eliminated. The simplified half-bridge power factor correction AC/DC converter is shown in Fig. 3.3(b). This is the basic charge pump power factor correction AC/DC converter. However, this converter does not have a perfect power factor. It is necessary to analyze the unity power factor condition so that this type of charge pump power factor correction AC/DC converter can be improved. In the following section, the unity power factor condition for this CPPFC converter is analyzed.



(a)



(b)

Fig. 3.3 (a) Power factor correction AC/DC converter

(b) The basic CPPFC converter

3.3 Unity Power Factor Condition

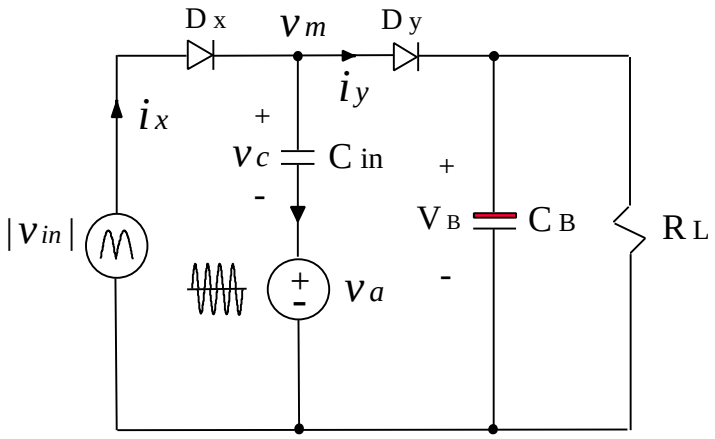
Due to the series resonance between the resonant inductor L_r and the resonant capacitor C_{in}, the voltage waveform v_a is a sinusoidal waveform. Alternative voltage v_a charges C_{in} through the line input to absorb energy from the line, and discharges energy to the bulk capacitor C_B. Because the absorbed energy of C_{in} is only related to the capacitor voltage variation, the waveshape of v_a is not so important. For further simplicity, v_a can be considered a high frequency voltage source. The generalized circuit is shown in Fig. 3.4(a). Because the charge capacitor C_{in} is in series with a high frequency voltage source to pump energy from the AC line and discharge its stored energy to the bulk capacitor C_B, this converter is usually called a *Voltage Source Charge Pump Power Factor Correction (VS-CPPFC) Converter*. In the steady-state analysis, four topological stages exist over one switching cycle. The switching waveforms are shown in Fig. 3.4(b).

M1 [t_0, t_1]: Before t_0, v_m is clamped to V_B, and D_y is on. After t_0, v_a decreases with a sinusoidal waveform. Because the charge capacitor voltage v_c cannot change abruptly, D_y is reverse biased. v_m also decreases with the same form. v_c keeps constant because there is no current through C_{in}; both D_x and D_y are off. This mode ends at t_1, where the voltage v_m is equal to the rectified line voltage, and D_x becomes forward biased and begins to conduct.

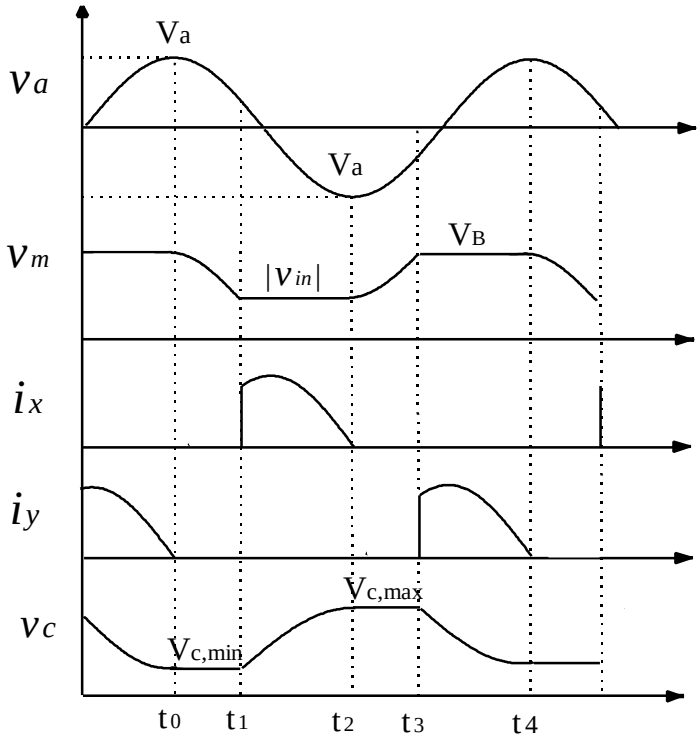
M2 [t_1, t_2]: At t_1, D_x is turned on, and v_m is clamped to the rectified line voltage. Because v_a continues to decrease, the charge capacitor voltage v_c increases up to $V_a + |v_{in}|$ at t_2. During this time interval, the charge capacitor absorbs energy from the line input. Its voltage and charging current are given by

$$\begin{aligned} v_c &= |v_{in}| - V_a \cos w_s (t - t_0) \\ i_c &= C_{in} V_a w_s \sin w_s (t - t_0) \qquad t_0 < t < t_1 \end{aligned} \tag{3.1}$$

where w_s and V_a are the frequency and the peak voltage of the voltage source v_a, respectively. At t_2, i_c becomes zero, and D_x is naturally turned off. The maximum charge capacitor voltage $V_{c,max}$ is expressed as



(a)



(b)

Fig. 3.4 (a) The generalized VS-CPPFC converter

(b) The switching waveforms of the VS-CPPFC converter

$$V_{c,max} = V_a + \left| v_{in} \right|. \tag{3.2}$$

M3 [t_2, t_3]: At t_2, D_x is turned off. Because v_m is lower than the DC bus voltage, D_y is in the reverse bias. No current flows through the charge capacitor, and v_c keeps constant. On the other hand, v_m continuously increases with the increase of v_a until t_3, where v_m reaches the DC bus voltage, and D_y is turned on.

M4 [t_3, t_4]: At t_3, v_m is clamped to the DC bus voltage, and D_y is turned on. Charge capacitor C_{in} discharges, and its stored energy is pumped to C_B due to the continuous increase of v_a. The charge capacitor voltage and its charging current are

$$\begin{aligned} v_c &= V_B - V_a \cos w_s(t - t_0) \\ i_c &= C_{in}\, V_a\, w_s \sin w_s(t - t_0) \qquad t_3 < t < t_4 \end{aligned} \tag{3.3}$$

v_c reaches its minimum value at t_4, which is given by

$$V_{c,min} = V_B - V_a. \tag{3.4}$$

At t_4, v_a increases up to its peak voltage. D_y will be turned off, and the next switching cycle begins.

From the above analysis, it can be seen that the rectified AC line current equals the capacitor charging current during the time period from t_1 to t_2. Therefore, the average AC line current over one switching cycle equals the average capacitor charging current, which is the total charge variation from t_1 to t_2. The charge variation is

$$D\,Q = C_{in} \left(V_{c,\,max} - V_{c,min} \right). \tag{3.5}$$

By substituting $V_{c,max}$ and $V_{c,min}$ into the above equation, the average rectified line current in a switching cycle is given by

$$\left| i_{in} \right| = i_{x,ave} = \frac{D\,Q}{T_s} = C_{in}\, f_s \left(\left| v_{in} \right| + 2\, V_a - V_B \right). \tag{3.6}$$

In order to achieve unity power factor, it is required that the line input current follow the line input voltage. From (3.6), if the converter is designed so that

$$2\, V_a = V_B, \tag{3.7}$$

then the rectified line current is

$$\left| i_{in} \right| = C_{in} f_s \left| v_{in} \right| \propto \left| v_{in} \right| . \tag{3.8}$$

Thus, the line input current is proportional to the line voltage, so unity power factor can be obtained if the condition of (3.7) can be satisfied. From (3.6), if $2V_a < V_B$, there is no input current when $| v_{in} | < | 2V_a - V_B |$.

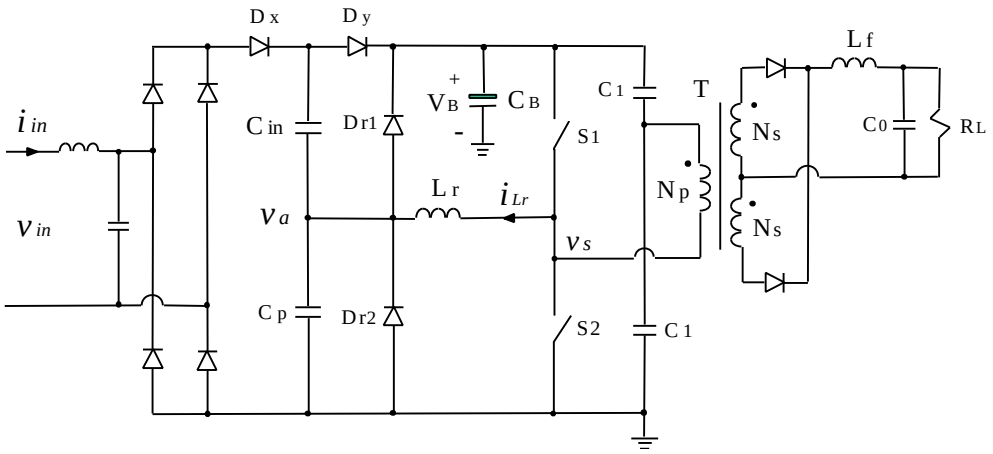
Under the unity power factor condition, the peak-peak voltage of the high frequency voltage source should equal the DC bus voltage. Therefore, it is natural to use the clamping technique to satisfy the unity power factor condition. If two clamping diodes are used to clamp v_a with the maximum voltage of V_B and the minimum voltage of zero, then (3.7) is automatically satisfied. Unity power factor can be achieved.

3.4 VS-CPPFC AC/DC Converters

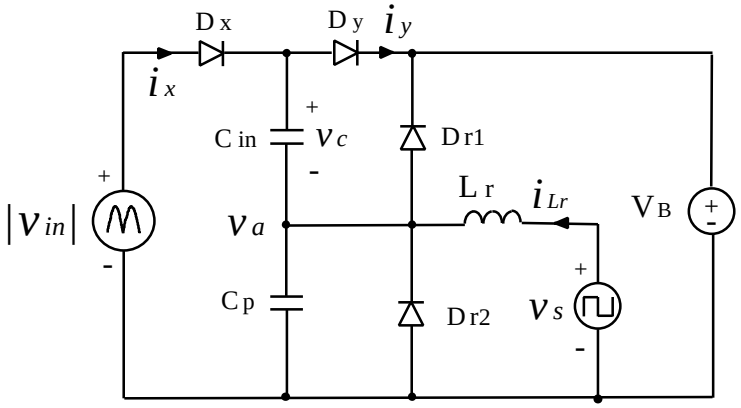
3.4.1 Principle of Operation

Simply adding two clamping diodes D_{r1} and D_{r2} to the circuit in Fig. 3.3(b) and replacing the load with a PWM converter creates the proposed VS-CPPFC AC/DC converter shown in Fig. 3.5(a). Here, the high frequency voltage source v_a can be obtained through a series resonant tank L_r and C_{in}. Two clamping diodes D_{r1} and D_{r2} are used to satisfy the unity power factor condition. Capacitor C_p is used to smooth the high frequency voltage source. Here, a half-bridge converter is employed as an example to achieve the desired output voltage. Because the half-bridge DC/DC converter is well known, only the PFC stage is analyzed to obtain the values of the charge pump capacitor C_{in} and resonant inductor L_r. The equivalent circuit of Fig. 3.5(a) is shown in Fig. 3.5(b), where a square waveform v_s is used to represent on and off switch positions. In the steady state, eight equivalent topological stages exist over one switching cycle, as shown in Fig. 3.6(a), and the switching waveforms are shown in Fig. 3.6(b)

M1 [t_0, t_1]: S_2 is turned on when S_1 is turned off at t_0. The equivalent circuit is shown in Fig. 3.6(a). Because C_{in} is much larger than C_p, the impedance of C_p is much higher than that of C_{in}. The current through C_p can be neglected.



(a)

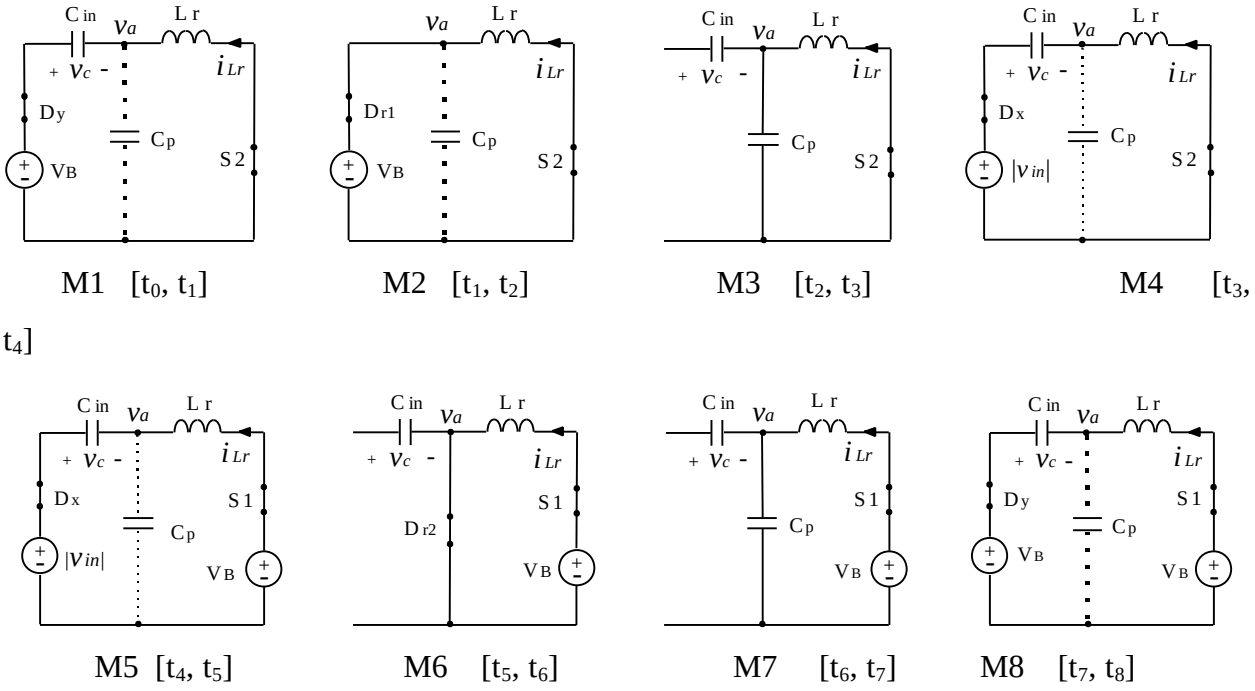


(b)

Fig. 3.5 The proposed converter and its equivalent circuit

(a) The proposed VS-CPPFC AC/DC converter

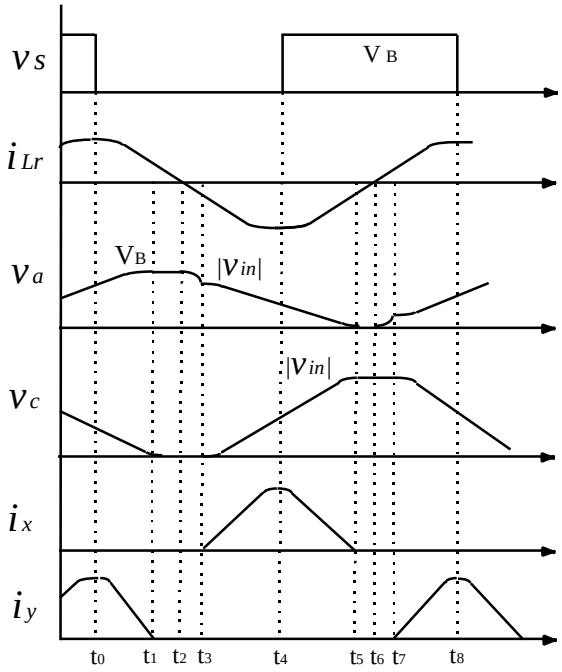
(b) Equivalent circuit of Fig. 3.5(a)



M1 [t_0, t_1] M2 [t_1, t_2] M3 [t_2, t_3] M4 [t_3, t_4]

M5 [t_4, t_5] M6 [t_5, t_6] M7 [t_6, t_7] M8 [t_7, t_8]

(a)



(b)

Fig. 3.6 Equivalent circuit and its switching waveforms

(a) Eight equivalent topological stages

(b) Switching waveforms

$$v_c(t) = V_B - \left[V_B - V_c(t_0)\right] cosw_0(t-t_0) - Z_0 I_{Lr}(t_0)\ sinw_0(t-t_0), \tag{3.9}$$

$$v_a(t) = \left[V_B - V_c(t_0)\right] cosw_0(t-t_0) - Z_0 I_{Lr}(t_0)\ sinw_0(t-t_0), \tag{3.10}$$

where $I_{Lr}(t_0)$ *and* $V_c(t_0)$ are initial conditions, Z_0 is the characteristic impedance $Z_0 = \sqrt{\frac{L_r}{C_{in}}}$, and w_0 is the resonant frequency $w_0 = \frac{1}{\sqrt{L_r C_{in}}}$. The capacitor voltage across C_{in} decreases to zero, while v_a increases to V_B at t_1, where the clamping diode D_r begins to conduct. All energy stored in C_{in} is discharged to the bulk capacitor C_B.

M2 [t_1, t_2]: The clamping diode D_{r1} is conducting, and v_a is clamped to V_B. The resonant inductor current i_{Lr} linearly decreases until it reduces to zero at t_2, where D_{r1} is naturally turned off. During this time period, v_c doesn't change, since there is not current through C_{in}.

M3 [t_2, t_3]: At t_2, D_{r1} is turned off and C_p is shown to form a resonant tank with L_r. The equivalent circuit is shown in Fig. 3.6(a). The resonant current and voltage are expressed as

$$i_{Lr}(t) = \frac{V_B}{Z_1} cosw_1(t-t_2) \tag{3.11}$$

$$v_a(t) = V_B\, cosw_1(t-t_2) \tag{3.12}$$

where Z_1 is the characteristic impedance $Z_1 = \sqrt{\frac{L_r}{C_p}}$ and w_1 is the resonant frequency $w_1 = \frac{1}{\sqrt{L_r C_p}}$. D_x begins to conduct when v_a is equal to the input voltage $|v_{in}|$ at t_3. This time interval is very short because the resonant frequency w_1 is very high.

M4 [t_3, t_4]: D_x is conducting. Its equivalent circuit is shown in Fig. 3.6(a). The charge pump capacitor is charged by the line input current. Actually L_r and C_{in} form a series resonant circuit, and v_s decreases in a sinusoidal form. The resonant inductor current is given by

$$i_{Lr}(t) = -\frac{|v_{in}|}{Z_0} sinw_0(t-t_3) - \frac{V_B}{Z_1}\sqrt{1-\frac{v_{in}^2}{V_B^2}}\, cosw_0(t-t_3), \tag{3.13}$$

where $I_{Lr}(t_3) = -\frac{V_B}{Z_1}\sqrt{1-\frac{v_{in}^2}{V_B^2}}$. This mode terminates at t_4, when S_2 is turned off.

M5 [t_4, t_5]: S_2 is turned off, while S_1 is turned on at t_4. The resonant inductor current i_{Lr} first charges and discharges the output capacitance of S_1 and S_2, respectively. Then, it flows through the anti-parallel diode of S_1. Therefore, S_1 can be turned on at zero voltage. D_x continues to conduct until the capacitor C_{in} is charged to the input voltage, where v_a decreases to zero, and the clamping diode D_{r2} starts to turn on at t_5. The corresponding equivalent circuit is shown in Fig. 3.6(a). i_{Lr} is expressed as

$$i_{Lr}(t) = I_{Lr}(t_3)\cos w_0(t-t_4) + \frac{V_B - |v_{in}| + v_c(t_3)}{Z_0}\sin w_0(t-t_4). \tag{3.14}$$

The line input current is equal to the resonant inductor current during this time period.

M6 [t_5, t_6]: The clamping diode D_{r2} is conducting, and i_{Lr} linearly increases because a positive voltage of V_B is applied to L_r. This mode stops at t_6, where the resonant inductor current i_{Lr} becomes zero and D_{r2} is naturally turned off.

M7 [t_6, t_7]: Once D_{r2} is turned off at t_6, C_p resonates with L_r, which makes v_s increase. The equivalent circuit is shown in Fig. 3.6(a). Since no current flows through C_{in}, v_c does not change. During this time period, i_{Lr} and v_a are given by

$$i_{Lr}(t) = \frac{V_B}{Z_1}\sin w_1(t-t_6) \tag{3.15}$$

$$v_a(t) = V_B\left[1-\cos w_0(t-t_6)\right]. \tag{3.16}$$

D_y conducts at t_7, where the summation of v_c and v_a equals V_B.

M8 [t_7, t_8]: The equivalent circuit is given in Fig. 3.6(a). In this time interval, the energy stored in the resonant tank L_r and C_{in} is delivered to the bulk capacitor C_B. At t_8, S_1 is turned off, and the next switching cycle begins.

From the above analysis, it can be seen that the input line current is approximately equal to the resonant inductor current from t_3 to t_5. The average input current equals half the average current of $|i_{Lr}|$ over one switching cycle:

$$|i_{in}| = i_{x,ave} = \frac{1}{T_s}\int_{t3}^{t5} |i_{Lr}(t)|\,dt. \tag{3.17}$$

For simplicity, i_{Lr} can be considered as a triangular waveform. Substituting i_{Lr} into the above equation yields

$$\left| i_{in} \right| = \frac{1}{4}\left(\frac{\left| v_{in} \right|}{Z_0} sin\frac{w_0 T_s}{4} - \frac{V_B}{Z_1}\sqrt{1-\frac{v_{in}^2}{V_B^2}}\, cos\frac{w_0 T_s}{4} \right). \tag{3.18}$$

Because $Z_1 >> Z_0$, and if the designed resonant frequency ω_0 is close to the switching frequency, the second term of the above equation can be omitted. Therefore, the rectified line input current $|i_{in}|$ can be given by

$$\left| i_{in} \right| \approx \frac{\left| v_{in} \right|}{4\, Z_0} \propto \left| v_{in} \right|. \tag{3.19}$$

The equation (3.19) shows that the rectified line current follows the line input voltage, so high power factor can be obtained.

Based on the power balance between the input and the output, the desired rectified input current is

$$\left| i_{in} \right| = \frac{2\, P_0}{V_{in}^2} \left| v_{in} \right|, \tag{3.20}$$

where V_{in} and P_0 are the peak line voltage and output power, respectively. From Eqs. (3.8), (3.19), and (3.20), two independent equations can be obtained to solve two unknowns, L_r and C_{in}. These two resonant component values of L_r and C_{in} are given by

$$L_r = \frac{h\, V_{in}^2}{32\, P_0\, f_s} \tag{3.21}$$

$$C_{in} = \frac{2\, P_0}{h\, f_s\, V_{in}^2}, \tag{3.22}$$

where h is the conversion efficiency. For a given output power, input voltage, and switching frequency, the resonant inductor L_r and charge capacitor C_{in} can be determined.

Single-stage power factor correction converters usually suffer from relatively high voltage stress across the bulk capacitor C_B. This converter also has this disadvantage. To solve this problem, variable switching frequency operation is needed. For this particular circuit, if v_a can be reduced at light load, higher voltage stress could be avoided. One method to reduce this voltage

stress employs another LC network [ ] and changing the switching frequency close to the resonant frequency of this extra LC network. The circuit is shown in Fig. 3.7. In that case, the variable switching frequency range can be significantly reduced.

3.4.2 Extended VS-CPPFC AC/DC Converters

Figure 3.8(a) shows the symmetrical charge pump power factor correction AC/DC converter, where two charge pump capacitors C_{in1} and C_{in2} are used to obtain a symmetrical input current. When one charge capacitor C_{in1} is in charge mode, the other capacitor C_{in2} is in discharge mode. Therefore, the input line current has twice the switching frequency, so a small line input filter can be used. Figure 3.8(b) shows a full-bridge two-parallel charge pump VS-CPPFC AC/DC converter for high power applications. These two converters can operate at zero-voltage switching so that switching losses can be reduced. However, the conduction loss may increase since the PFC stage is actually a resonant converter, and the rms current of a resonant converter is higher than that of a PWM converter.

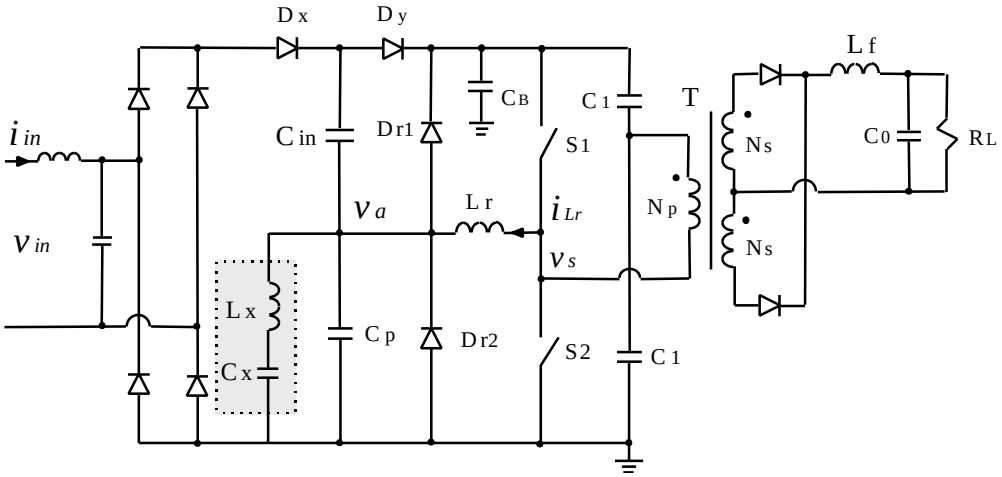
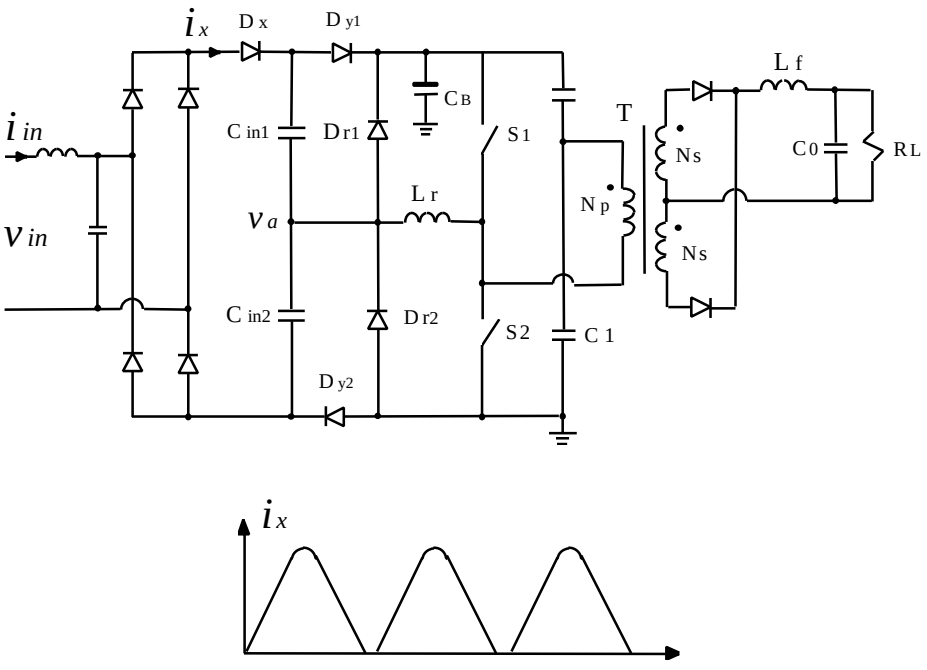
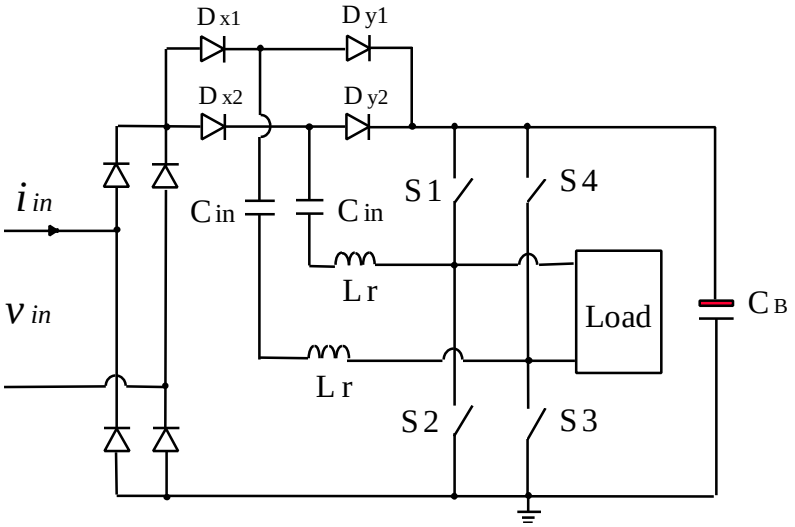


Fig. 3.7 The VS-CPPFC AC/DC converter with narrow switching frequency variation range



(a)



(b)

Fig. 3.8 (a) Symmetrical charge pump power factor correction AC/DC converter

(b) Two-parallel charge pump power factor correction AC/DC converter

3.4.3 Experimental Results

The charge pump power factor correction AC/DC converter of Fig. 3.7 was implemented to verify circuit operation with 250-watt, 12V output and 220V input. The circuit parameters are

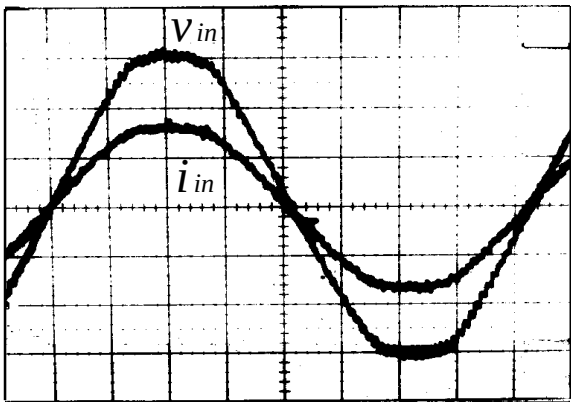
L_r = 125 μH C_{in} = 72 nF L_x = 670 μH

C_x = 5.6 nF C_p = 3.3 nF f_s = 68-80 kHz

In order to control the DC bus voltage stress at light load, a variable switching control scheme was used. When the load becomes light, the switching frequency changes in such a way that it is close to the resonant frequency of L_x and C_x so that the input power also decreases. The measured input line current waveform is shown in Fig. 3.9(a). The experimental results show that 0.996 power factor and 5% THD can be achieved at full load. The measured efficiency is about 83.5%. Fig. 3.9(b) shows the DC bus voltage across C_B and the switching frequency variation as a function of the load variation. As Fig. 3.9(c) shows, the required switching frequency variation range is only from 68 to 80 kHz to keep the DC bus voltage below 350V when the load varies from 100% to 10%.

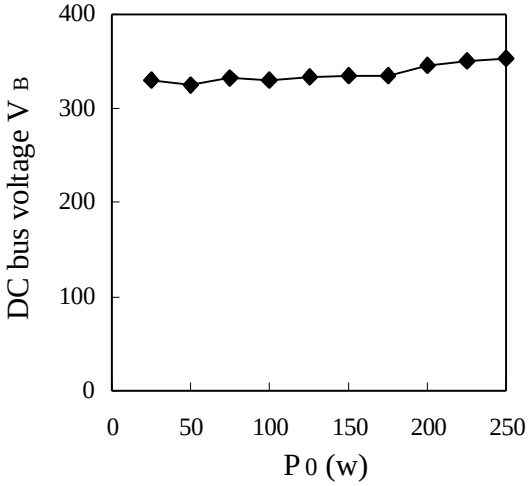
3.5 Single-Switch Charge Pump Power Factor Correction AC/DC Converter

The charge pump power factor correction converters developed in the last section have good power factor. These converters have to use two power switches, which are suitable for medium-power applications. To reduce the cost, however, a single switch is preferred for output power less than 150-watt. Besides, perfect power factor is not necessary to meet IEC 1000-3-2 class D requirements. It is estimated that 0.9 power factor is enough to meet this regulation. For low power application, low cost is one of the main issues. Usually, the power switch is one of the most expensive components in the circuit. In addition, a capacitor is usually cheaper than the inductor for low-power applications. Thus, it is attractive to develop a single-stage single-switch CPPFC converter, since a capacitor is used to achieve power factor correction. In this section, the single-stage single-switch CPPFC converter is first derived. The developed single-stage power factor correction AC/DC converter operates with continuous input current (CIC). The power factor correction stage does not increase the switching current stress and has no DC bus

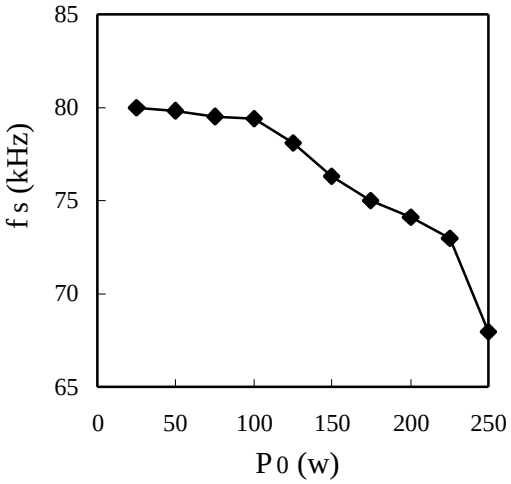


t: 2 ms/div v_{in} 100 V/div i_{in}: 1 A/div

(a)



(b)



(c)

Fig. 3.9 Experimental results

(a) Measured line input voltage and current waveforms

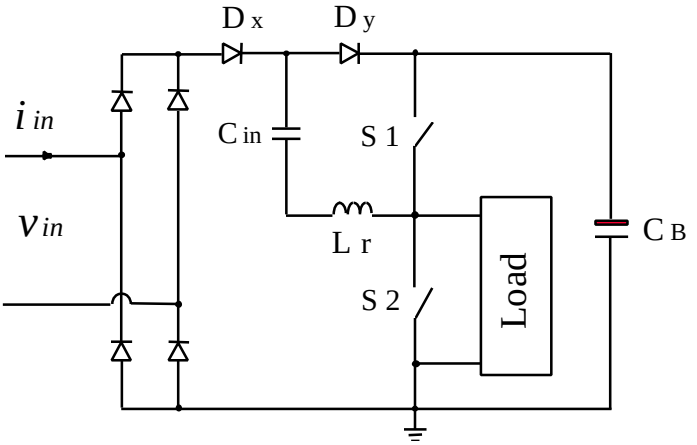
(b) DC bus voltage with load variation

(c) Switching frequency variation range

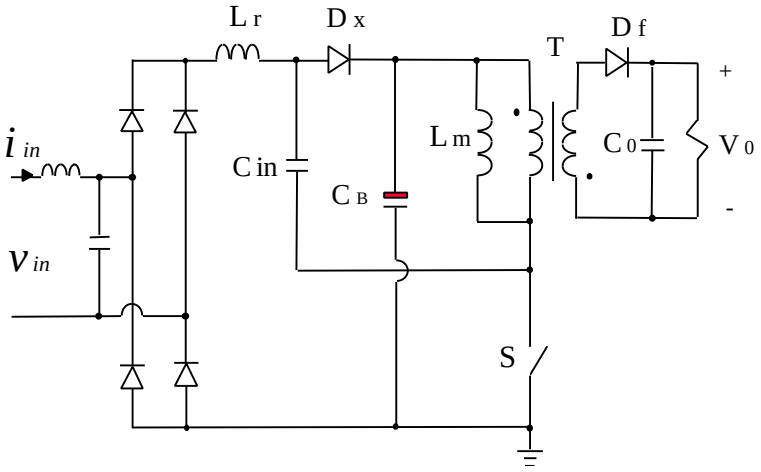
voltage stress at light load since both the PFC stage and DC/DC stage operate in CCM according to the analysis in Section 2.1. The developed converter can operate from 0.5% to 100% load with universal line input. These characteristics are very attractive.

3.5.1 Circuit Derivation

The basic voltage source charge pump power factor correction converter derived earlier, is shown in Fig. 3.10(a). The charge capacitor C_{in} is charged through the resonance with L_r to absorb energy from the line input in one-half of the switch period, while its energy is pumped to



(a)



(b)

Fig. 3.10 (a) Basic charge pump power factor correction (CPPFC) converter
(b) Single-switch resonant CPPFC AC/DC converter

the bulk capacitor C_B in the other half of the switching cycle. The key point is that the resonant inductor L_r serves to charging and discharge C_{in}. However, for low-power PFC AC/DC applications, it is desirable to use only one power switch to reduce the cost. If only one switch can be used, usually the upper switch S_1 is replaced by an isolated transformer and load. Figure 3.10(b) shows the single-stage single-switch charge pump power factor correction AC/DC converter [C13]. The input choke L_r serves as the resonant inductor, so that C_{in} absorbs energy from the AC line through the resonance between C_{in} and L_r during the switch S on-time period, while the magnetizing inductor serves as the resonant inductor to deliver C_{in}'s energy to the load through the resonance between C_{in} and L_m during the switch off-time period. Thus, the circuit in Fig. 3.10(b) inherently has a power factor correction function. This converter is actually a resonant charge pump PFC stage integrated with a PWM flyback converter. Both the PFC stage and DC/DC stage can operate at CCM for Fig. 3.10(b).

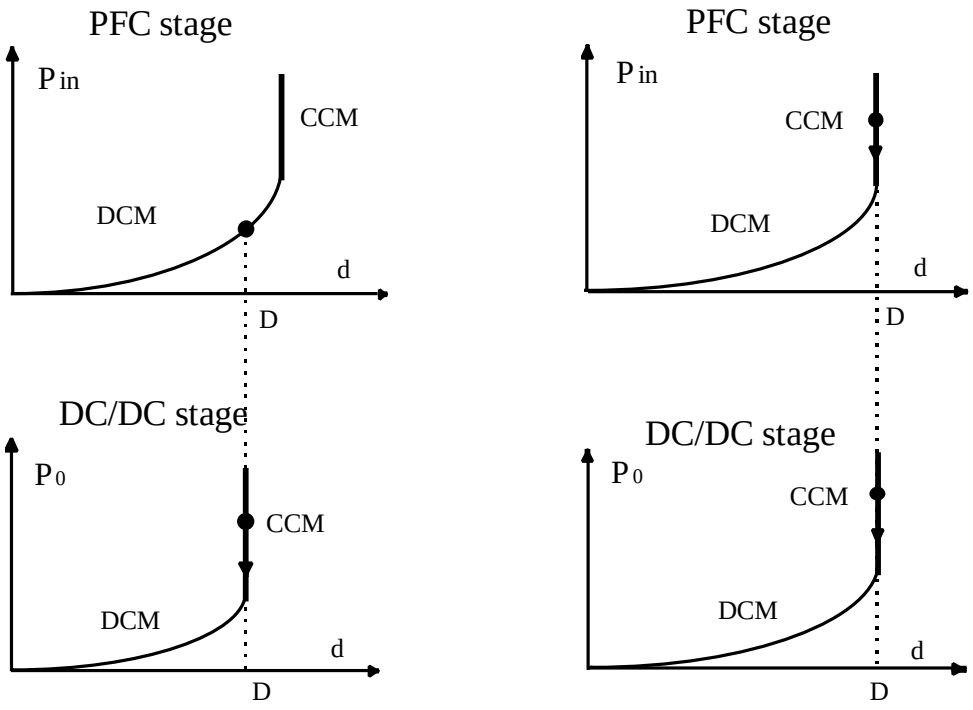


Fig. 3.11 The relationship between the input power, output power, and duty cycle

(a) DCM PFC + CCM DC/DC

(b) DCM PFC + DCM DC/DC

If both the PFC stage and DC/DC stage operate in CCM, the input power and output power can be automatically balanced according to Fig. 3.11(b). The duty cycle always remains the same even when the load becomes light. The input power could be either small or high, depending on the load. Therefore, This CCM PFC + CCM DC/DC converter has inherent properties to balance the input power and the output power so that no bus voltage problem exists. Therefore, There is no DC bus voltage stress at light load for the circuit in Fig. 3.10(b).

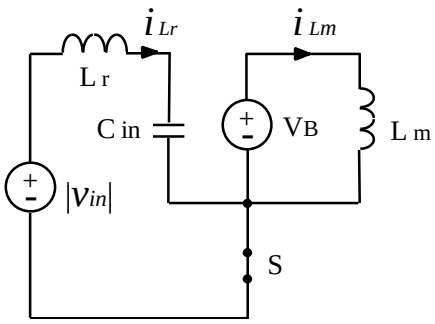
3.5.2 Steady-State Analysis

In the steady state analysis, four topological stages exist within one switching cycle as shown in Fig 3.12(a). The switching waveforms are shown in Fig 3.12(b). The operation principle is as follows.

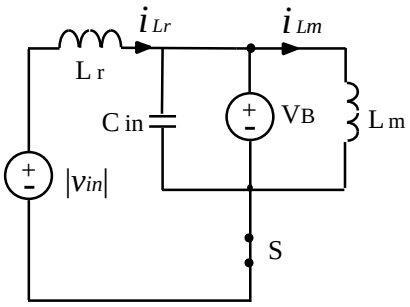
M1, [t_0, t_1]: Switch S is turned on at t_0. Bus voltage V_B is applied to the primary winding of the transformer. The magnetizing current linearly increases. Diode D_x is off since a negative voltage of $V_B+|v_c|$ is applied to D_x. The equivalent circuit is shown in Fig 3.12(a). The resonant inductor L_r and capacitor C_{in} form a series resonance to absorb energy from the AC line. The inductor current i_{Lr} increases in a resonant form. During this time period, the switch conducts the currents from both the resonant stage and the DC/DC converter. This stage ends when the resonant capacitor voltage reaches the bus voltage, where D_x begins to conduct at t_1.

M2, [t_1, t_2]: The voltage across the capacitor C_{in} is clamped when D_x is turned on at t_2. The energy stored in the inductor L_r is transferred to the bulk capacitor and its current linearly decreases since the bus voltage is always higher than the peak line input voltage. Switch S carries only the current from the DC/DC stage. The equivalent circuit is shown in Fig 3.12(a). This stage ends at t_2 when switch is turned off.

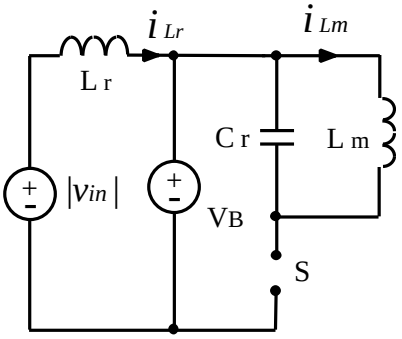
M3, [t_2, t_4]: Switch S is turned off at t_2. The current difference between the magnetizing inductor and the input inductor is to discharge the resonant capacitor. The magnetizing current continues to increase until the voltage across the resonant capacitor reverse at t_3. After t_3, the magnetizing current keeps charging the C_{in} until the voltage across C_{in} equals the reflected output voltage, where the output rectifier D_f becomes forward biased at t_4. During this time interval, the



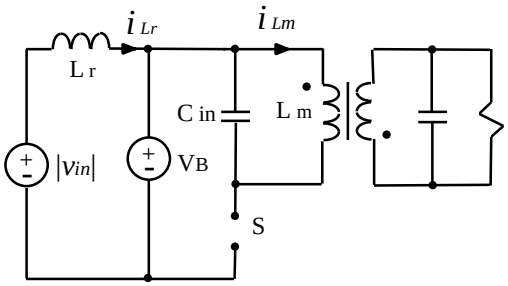
M1 $[t_0, t_1]$



M2 $[t_1, t_2]$

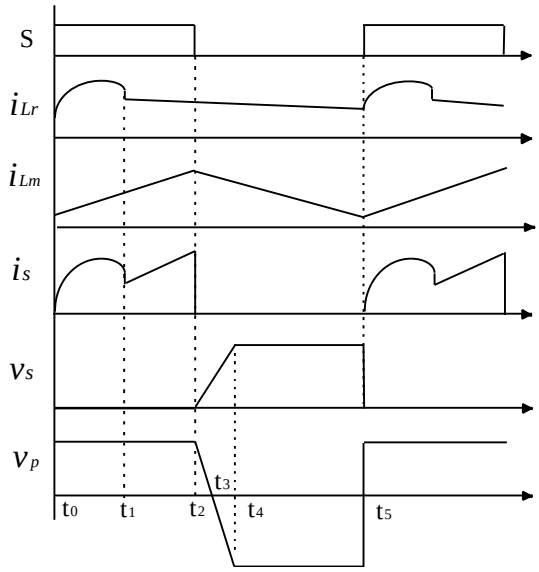


M3 $[t_2, t_4]$



M4 $[t_4, t_5]$

(a)



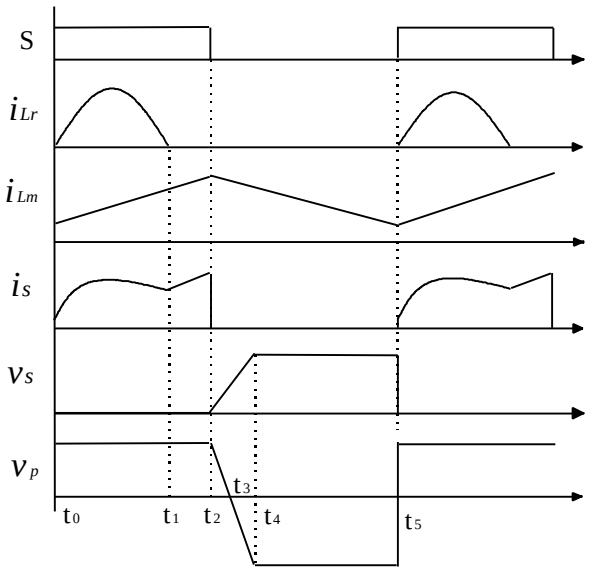


Fig 3.12 Topological stages and switching waveforms

(a) Four topological stages (b) The switching waveforms near the line peak voltage

(c) The switching waveforms near the zero crossing of the line voltage

magnetizing current is assumed to be constant so that the voltage across the switch linearly increases. The input current continues to decrease during this stage.

M4, [t_4, t_5]: The output diode D_f is turned on at t_4. The magnetizing energy is now delivered to the load and its current decreases linearly. The voltage across C_{in} is clamp to the reflected output voltage.

When the input voltage is low near the zero crossing of the line input voltage, the input current becomes discontinuous because the maximum resonant voltage across C_{in} is less than the bus voltage, as shown in Fig 3.12(c). The resonant stage terminates at its half resonant cycle.

The above analysis shows that the current waveform through the switch is similar to that of a PWM boost converter operating in continuous current mode. Thus, the conduction loss is relatively small, since the rms current of the switch is reduced, compared with that of DCM operation. Furthermore, the switching turn-off current is only from the DC/DC stage because the current from the power factor correction stage equals zero. Therefore, the current stress is reduced to almost the same level as that of the DC/DC converter. In other words, the PFC stage does not increase the conduction and switching losses. Thus, this converter operates efficiently. This is one of the main advantages of this converter. When the line voltage is high, for example, 260 V rms, the duty ratio becomes small. The switch has to take the currents both from the PFC stage and DC/DC converter. However, the input current is relatively small at high line voltage for constant power operation. Therefore, the efficiency still could be high.

The resonant capacitor C_{in} has several functions. First, it is used as the resonant element to form a resonant tank with L_r to obtain power factor correction. Second, it also serves as the snubber capacitor. When the switch is turned off, the leakage and magnetizing currents charge this resonant capacitor C_{in}, and the rate of the voltage change across the switch is limited by this capacitor. Thus, S can be turned off at zero voltage, which further reduces the switching loss. This snubber capacitor energy is transferred to the magnetizing energy during this transient period from t_2 to t_4, and then is charged in the reverse direction. So, this capacitor could be called either a resonant capacitor or snubber capacitor. Therefore, the voltage stress across the switch is clamped by C_{in}.

In general, the single stage PFC AC/DC converter suffers from high DC bus voltage stress at light load when the DC/DC stage operates in CCM and the PFC stage operates in DCM. The resonant capacitor has the function of helping reduce this voltage stress. The magnetizing inductor is the energy storage element, and its current is related to the load current. When the load becomes light, the magnetizing current will diminish so that the discharging time interval of C_{in} from t_2 to t_4 becomes longer. If the duty ratio remains constant, based on the volt-second balance of the primary winding of the transformer, the output voltage has to increase, which in turn automatically decreases the duty cycle. The decrease of the duty ratio certainly decreases the input power to keep the power balance between the input and the output. This duty ratio decrease is not due to the bus voltage increase, but to the characteristic of this DC/DC converter. However, this capacitor is not big enough, usually about several tens of nF. This feature is not very pronounced, but this capacitor tends to reduce the voltage stress. For this converter, there is no DC bus voltage stress at light load since both the PFC stage and DC/DC stage operate in CCM, according to the analysis in Chapter 2. Thus. the input power and the output power can be automatically balanced. This feature is very attractive.

3.5.3 Experimental Verification

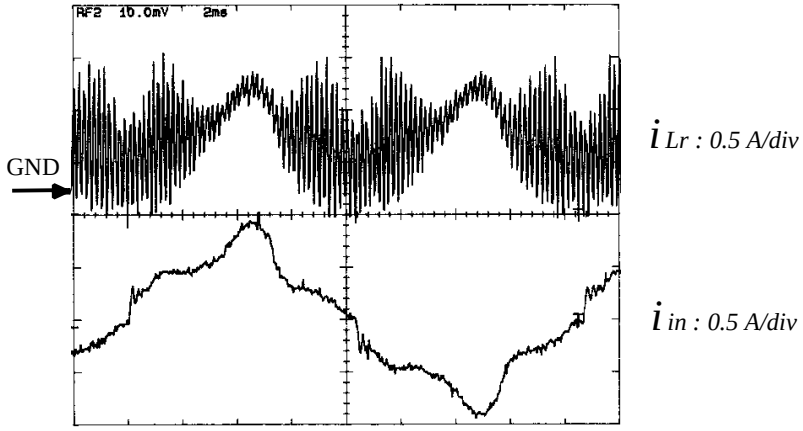
The single-switch CPPFC AC/DC converter was implemented to demonstrate the principle of operation. The converter is designed to operate at 70-watt, 5-volt DC output with universal line input. The circuit parameters are:

L_r = 580 μH L_m = 300 μH C_{in} = 4.7 nF

f_s = 90 kHz N_p = 34 T N_s = 2 T

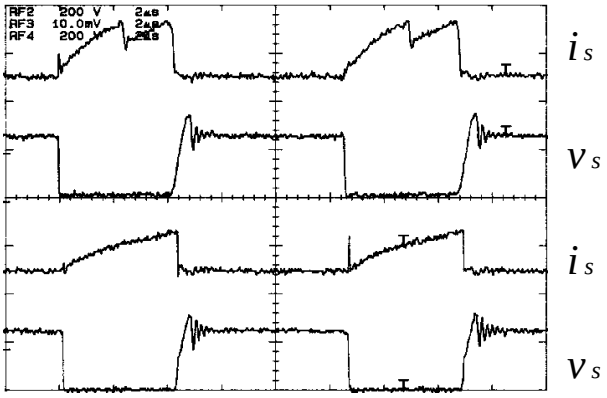
One prototype was implemented to operate at the universal input from 90 V rms to 260 V rms to verify its operation. Figures 3.13(a) shows the experimental waveforms of the input ac line current at 150V input with 70-watt, 5V output. It can be seen that the converter has continuous input line current near the peak line voltage. Fig. 3.13(b) shows the switching waveforms. It shows that the DC/DC stage operates in CCM at full load with low line input, and in DCM at light load to reduce the DC bus voltage stress. The measured line current harmonic components under universal line input voltage are shown in Fig. 3.14(a). It can be seen that the line current harmonics satisfy the IEC 1000-3-2 Class D requirements. The measured THD is shown in Fig.

3.14(b). It is shown that 70% THD still can satisfy the Class D requirements. Figure 3.14(c) shows the measured efficiency over the universal input voltage range. The lowest efficiency occurs at low line input, because at low line input the circuit has higher current stress and higher conduction loss, compared with those of high line. However, the efficiency also decreases at higher line input. This is mainly because the switching loss is dominant due to the



t: 2 ms/div

(a)



t: 2 ms/div, i_s: 2 A/div, v_s: 200 V/div

(b)

Fig. 3.13 Measured experimental waveforms

(a) The measured rectified line current at V_{in} = 150 V rms

(b) The measured switching waveforms for V_{in} = 110 V rms, P_0 = 70-watt

Top two waveforms: Near the peak line voltage

Bottom two waveforms: Near zero crossing of line voltage

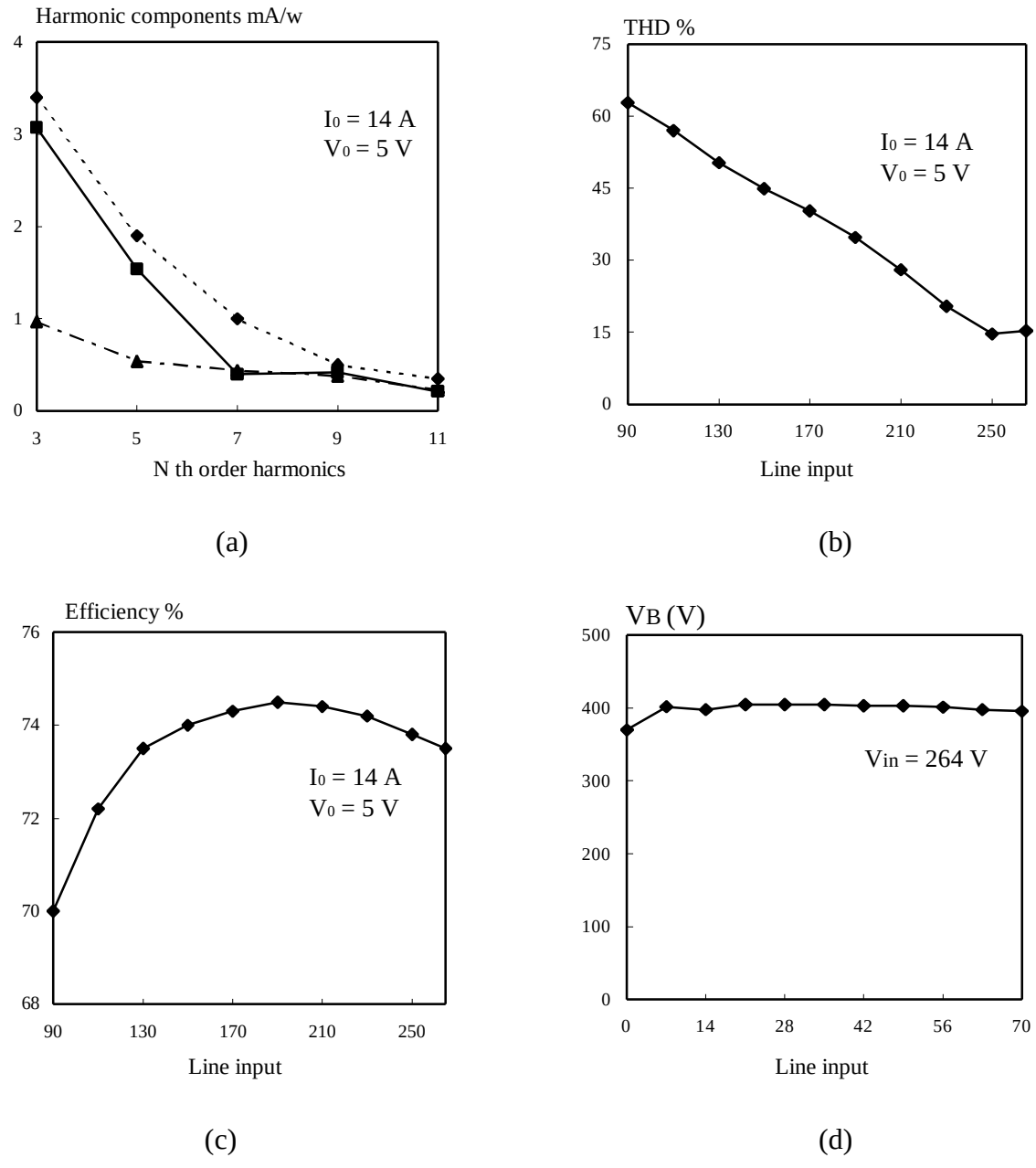


Fig. 3.14 The experimental results

(a) Measured line current harmonic components

(b) Measured THD

(c) Efficiency over line input voltage at full load

(d) DC bus voltage over load variation

high voltage. This overall efficiency corresponds to 92.7% or higher efficiency of each stage for the two-stage approach. The experimental switching waveforms show a voltage spike of the

switch after it is turned on. This is mainly due to the leakage inductance of the transformer, and finally was clamped. The rate of increase of the switch voltage is limited by the snubber capacitor C_s. The bus voltage stress across C_B over the load variation is shown in Fig. 3.14(d). It can be seen that the highest voltage stress is less than 400 volts for the converter operating from 1% to full load, so, a 450V bulk capacitor can be used. Figure 3.15 shows the efficiency for different circuits. It can be seen that this CCM PFC + CCM DC/DC converter has highest efficiency. So, it is very attractive to develop a single-stage PFC circuit with CCM operation.

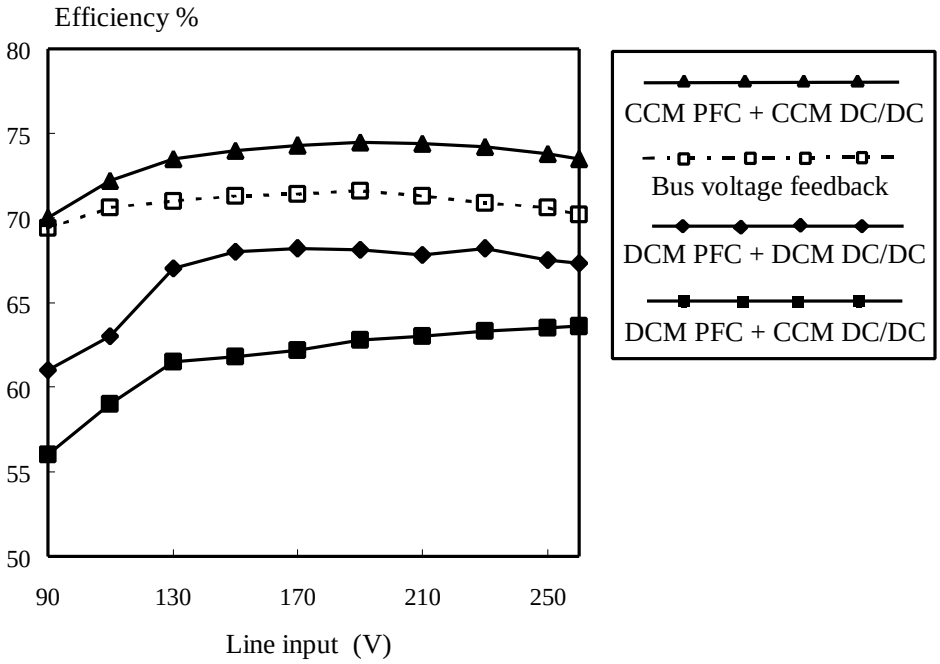


Fig. 3.15 The efficiency comparison

The advantages of the developed single-stage single-switch charge pump power factor correction AC/DC converter are summarized as follows:

- It is free from DC bus voltage stress over a wide range of load variation with universal line input. This voltage stress is suppressed within 400 V so that a 450 V rated bulk capacitor can be used. Furthermore, a low voltage rating device can be used as the main power switch.
- Continuous input current can be obtained, so a smaller line input filter can be employed, compared with the DCM operation.
- The charge pump capacitor not only serves as a resonant capacitor, but also as the snubber capacitor. The leakage energy of the isolated transformer can be recovered. Also, the charge capacitor helps suppress the DC bus voltage stress.
- The developed single-switch single-stage converter has a potentially low cost.

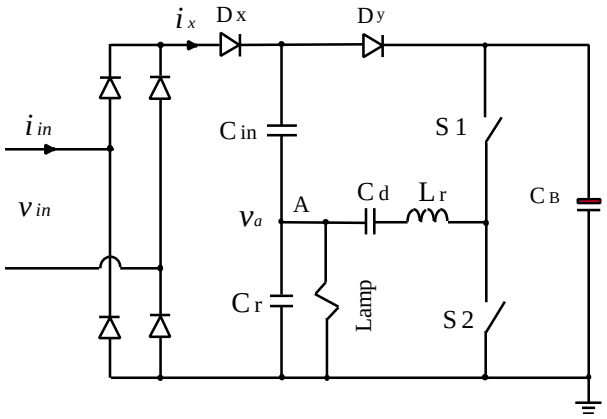
3.6 Voltage Source Charge Pump Power Factor Correction (VS-CPPFC) Electronic Ballast

3.6.1 Basic VS-CPPFC Electronic Ballast

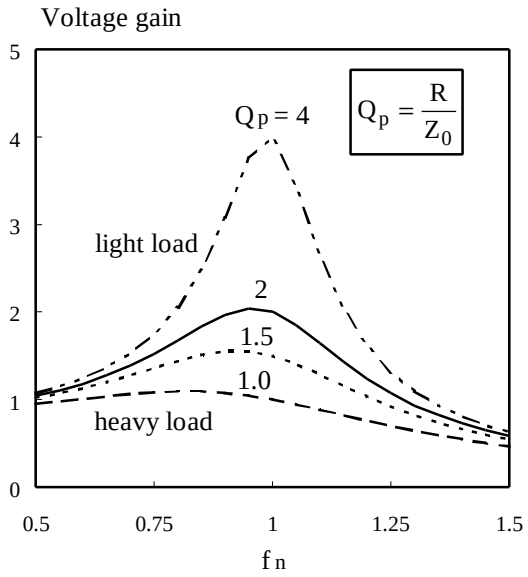
From the basic VS-CPPFC converter, shown in Fig. 3.3(b), if the load is shifted to the terminal A and ground, then the resulting topology becomes the VS-CPPFC electronic ballast shown in Fig. 3.16(a). The resonant components L_r and C_r form a series resonant parallel-loaded tank to provide high frequency energy to the lamp. A plot of the voltage gain of the series resonant parallel-loaded converter, shown in Fig. 3.15(b), shows that the ballast has high voltage gain at light load while it provides low output voltage at heavy load. On the other hand, from the lamp characteristics, it appears to have very high impedance during the preheat and start-up modes, which correspond to the light load operation of the electronic ballast. Thus, high lamp voltage can be obtained, which is desirable to ignite the fluorescent lamp. Usually, the lamp ignition voltage is about 3 times the normal operating voltage. Once the lamp is ignited, the lamp can be considered a pure resistance with a negative dynamic impedance. If the lamp voltage is modeled as a voltage source with constant amplitude, based on the analysis in Section 3.3, the average line input current in one switching cycle is given by

$$i_x = \frac{D\,Q}{T_s} = C_{in}\,f_s\left(\left|v_{in}\right| + 2\,V_a - V_B\right) \tag{3.23}$$

where V_a and V_B are the lamp peak voltage and DC bus voltage across C_B, respectively. From Eq. (3.23), the unity power factor condition is achieved when the lamp peak to peak voltage equals the DC bus voltage. However, this condition cannot be automatically satisfied. Therefore, the



(a)



(b)

Fig. 3.16 (a) The basic VS-CPPFC electronic ballast

(b) Voltage gain characteristics of series resonant parallel-loaded tank

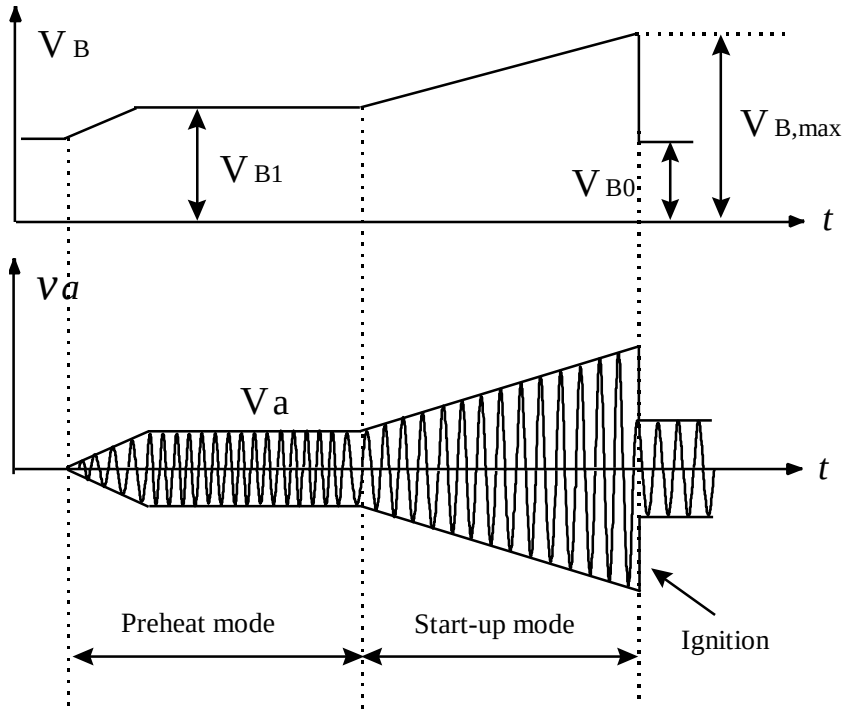


Fig. 3.17 The DC bus voltage across bulk capacitor C_B and the lamp voltage during the preheat and start-up modes

circuit in Fig. 3.16(a) suffers from input current harmonics that are a little high. Intuitively, this electronic ballast has no power factor correction without C_{in}. It is C_{in} that integrates the PFC stage and DC/AC inverter to achieve power factor correction.

The instantaneous input power is

$$p_{in}(t) = C_{in} f_s \left[v_{in}^2 + \left(2 V_a - V_B\right) \left| v_{in}(t) \right| \right]. \tag{3.24}$$

Averaging Eq. (3.24) over one line cycle yields

$$P_{in} = C_{in} f_s \left(\frac{V_{in}^2}{2} + \frac{2 V_{in}}{p} \left(2 V_a - V_B\right) \right). \tag{3.25}$$

At light load, such as preheat and start-up modes, where the lamp is off, and only filaments are being heated, the output power is very low. Figure 3.17 shows the voltage across C_B and the lamp

voltage waveforms during the preheat and start-up modes. During the preheat mode, the frequency is higher than normal operation, and V_B has to increase to keep low input power. Also, in order to ignite the lamp, the peak lamp voltage V_a has to be 2-3 times normal operating voltage. From Eq. (3.25), V_B has to increase to maintain this equality due to the light load operation. Therefore, high DC bus voltage stress exists during the preheat and start-up mode operations. High DC bus voltage requires high voltage rating bulk capacitor and power devices, which definitely increase the cost.

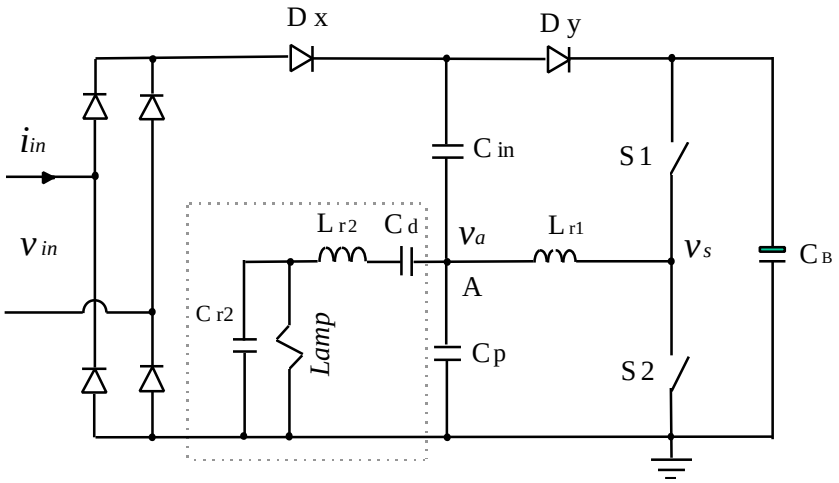
Another disadvantage of the circuit in Fig. 3.16(a) is its high lamp crest factor. This high crest factor is mainly due to the charge capacitor C_{in} modulation with the resonant tank. It can be seen that C_{in} is in parallel with the resonant capacitor C_r when either D_x or D_y is on. As a result, the equivalent resonant capacitor is a function of the line voltage. The higher the line voltage, the larger the equivalent resonant capacitance. Since C_{in} is much higher than C_r, the equivalent resonant capacitor is $C_{in} + C_r$ near the line peak voltage and C_r near the zero crossing of the line voltage. Therefore, the equivalent resonant capacitor significantly changes over one line cycle, which deteriorates the lamp crest factor. Therefore, the main disadvantages of the circuit are:

1. Inability to automatically achieve unity power factor, and resultant high line current harmonics.
2. High DC bus voltage stress across C_B during the preheat and start-up modes.
3. High crest factor due to C_{in} modulation.

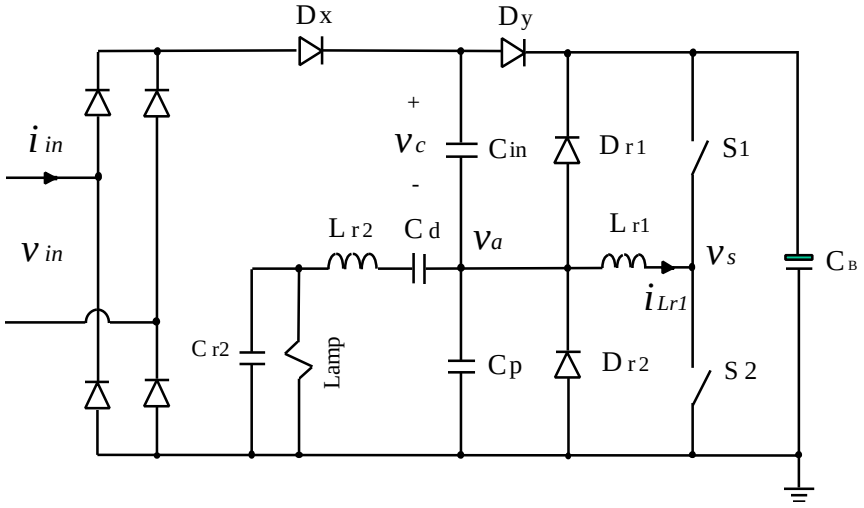
3.6.2 VS-CPPFC Electronic Ballast with Second Resonance

From Eq. (3.25), it can be seen that the DC bus voltage stress can be suppressed as long as voltage v_a is small at light load. However, v_a cannot be small since the lamp voltage has to be high enough to ignite the lamp. Therefore, to overcome this contradiction, the lamp voltage and v_a must be separate. To reduce v_a at light load, a low impedance path is connected to the terminals A and ground at light load. It is well known that the series resonant parallel-loaded tank has a low impedance at its resonant frequency. This suggests simply adding a series resonant parallel-loaded tank between node A and ground. The derived VS-CPPFC electronic ballast is shown in Fig. 3.18(a) [C7, C8]. At preheat and start-up modes, the switching frequency is set to

around the resonant frequency of L_{r2} and C_{r2} so that low v_a can be achieved to reduce the DC bus voltage. High lamp voltage still can be obtained because of the high voltage gain of the



(a)



(b)

Fig. 3.18 (a) The VS-CPPFC electronic ballast with second resonance

(b) The VS-CPPFC electronic ballast with unity power factor

series resonant parallel-loaded tank at light load, even though v_a is small. As discussed in Section 3.2, the unity power factor condition for Fig. 3.18(a) is that the peak-peak voltage of v_a is equal to the DC bus voltage. Therefore, adding two clamping diodes D_{r1} and D_{r2} automatically satisfies the unity power factor condition, as shown in Fig. 3.18(b). In the next section, circuit operation will be analyzed, and design equations are derived so that the electronic ballast can operate at optimum conditions, low DC bus voltage stress at abnormal conditions, unity power factor and low lamp crest factor.

3.6.2.1 Steady State Analysis and Design Considerations

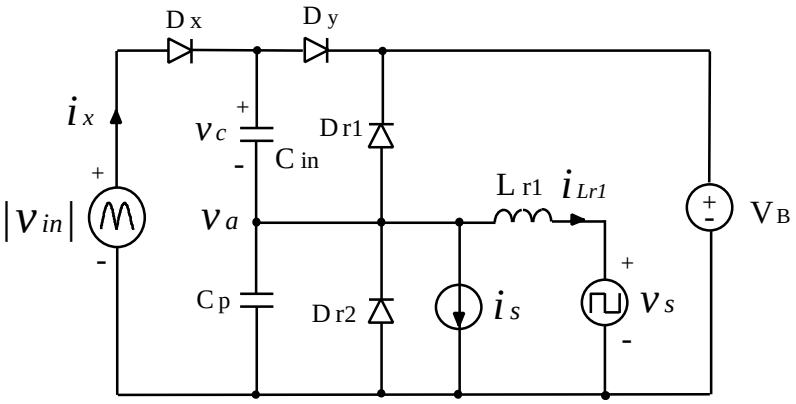
Figure 3.18(b) shows the VS-CPPFC electronic ballast with second resonance. L_{r1}, C_{in}, and C_p are composed of the first resonant circuit to achieve power factor correction, while the second resonant stage consists of L_{r2}, C_{r2}, and lamp to provide high frequency energy to the lamp. The clamping diodes D_{r1} and D_{r2} are used to satisfy the unity power factor condition. In order to analyze this circuit, the second resonant stage, comprising of L_{r2}, C_{r2}, and lamp, is a series resonant parallel-loaded tank, which can be considered a high frequency current source if the lamp voltage is constant. The equivalent circuit is shown in Fig. 3.19(a). Since two switches are turned on and off with 50% duty cycle, the high frequency square waveform v_s is represented as these two switches in the on and off positions. In the steady state analysis, eight topological stages exist over one switching cycle, as shown in Fig. 3.19(b). The key waveforms are shown in Fig. 3.20.

M1 [t_0, t_1]: S_1 is turned off when S_2 is turned on at t_0. The voltage v_a at node A is V_B before S_2 is turned on. During this time period, the clamping diode D_{r1} is still conducting if the resonant current i_{Lr1} is higher than i_s. Therefore, the inductor current i_{Lr1} linearly decreases until the inductor current equals the load current i_s, when the clamping diode is turned off.

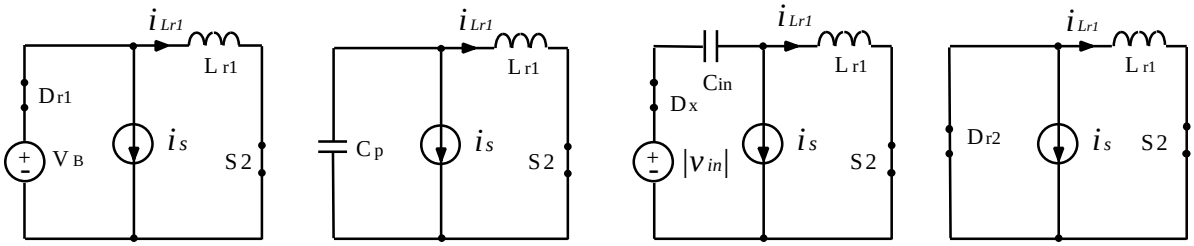
M2 [t_1, t_2]: During this time interval, both D_x and D_y are off. The capacitor C_{in} is neither charged nor discharged, and its voltage keeps constant. The equivalent circuit is shown in Fig. 3.19(b). C_p and L_{r1} form a parallel resonant tank. The load current i_s is

$$i_s(t) = I_s \cos w_s(t - t_0), \tag{3.26}$$

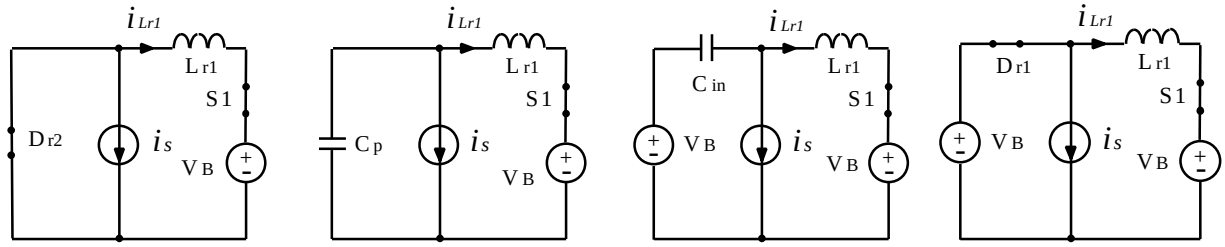
where ω_s is the switching frequency. Current i_s can be assumed to be constant during this stage, since the resonant frequency of C_p and L_{r1} is much higher than the switching frequency. When the voltage v_a decreases to the line input voltage at t_2, D_x starts to conduct.



(a)



M1 $[t_0, t_1]$ M2 $[t_1, t_2]$ M3 $[t_2, t_3]$ M4 $[t_3, t_4]$



M5 $[t_4, t_5]$ M6 $[t_5, t_6]$ M7 $[t_6, t_7]$ M8 $[t_7, t_8]$

(b)

Fig. 3.19 (a) The equivalent circuit of Fig. 3.18(b)

(b) Eight topological stages

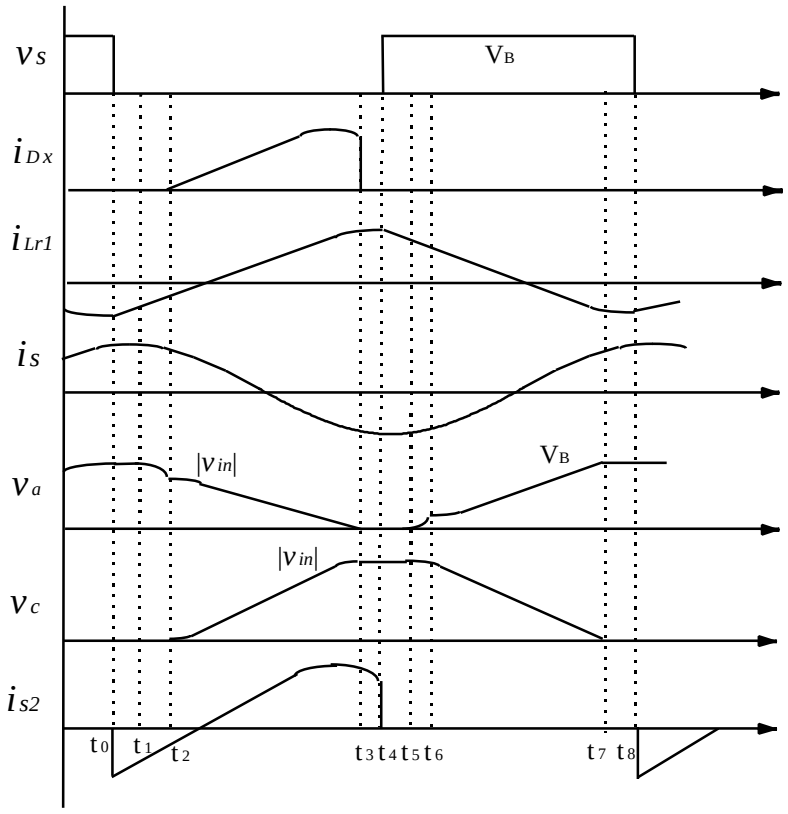


Fig. 3.20 Key waveforms of the electronic ballast

M3 [t_2, t_3]: When v_a decreases to the input line voltage, C_{in} is connected to the line to be charged, as shown in Fig. 3.19(c). Due to the resonance between L_{r1} and C_{in}, v_a decreases in the resonant form, and in turn the line input voltage charges the capacitor C_{in}. Therefore L_{r1} and C_{in} absorb energy from the ac line. Solving the equivalent circuit, the resonant inductor current i_{Lr1} which is the input current through D_x, is given by

$$i_{Lr1}(t) = \frac{|v_{in}|}{Z_0} \sin w_0(t-t_2) - \frac{I_s w_s^2}{w_s^2 - w_0^2} \cos w_0(t-t_2) + \frac{I_s w_0^2}{w_s^2 - w_0^2} \cos w_s(t-t_2) \qquad (3.27)$$

$$i_{Dx}(t) = i_{Lr1}(t) + I_s \cos w_s\left(t - t_0\right) \tag{3.28}$$

where $w_0 = \frac{1}{\sqrt{L_{r1}C_{in}}}$ and $Z_0 = \sqrt{\frac{L_{r1}}{C_{in}}}$. At t_3, v_a decreases to zero voltage, and C_{in} is charged to the rectified line input voltage, where the clamping diode D_{r2} begins to conduct.

M4 [t_3, t_4]: During this period, the inductor current i_{Lr1} remains constant, since L_{r1} is shorted through D_{r2} and S_2. The current difference between i_s and i_{Lr1} flows through the clamping diode. The equivalent circuit is shown in Fig. 3.19(d). At t_4, S_2 is turned off and this mode ends.

M5 [t_4, t_5]: When S_2 is turned off, i_{Lr1} flows through the body diode of S_1. Therefore, S_1 can be turned on at zero voltage. From the equivalent circuit of Fig. 3.19(e), it can be seen that the inductor current linearly decreases until the load current i_s is equal to i_{Lr1}, where the clamping diode D_{r2} is naturally turned off at t_5. During this time interval, the voltage across the charge capacitor C_{in} does not change.

M6 [t_5, t_6]: Because the clamping diode D_{r2} is off, the capacitor C_p resonates with L_{r1}. The equivalent circuit is shown in Fig. 3.19(f). At t_6, v_a increases to the value of V_B-$|v_{in}|$, and D_y begins to conduct. This time period is very short because the resonant frequency is much higher than the switching frequency.

M7 [t_6, t_7]: During this time interval, the energy stored in the capacitor C_{in} is discharged to the bulk capacitor through D_y due to the voltage increase of v_a. As shown in the equivalent circuit of Fig. 3.19(g), L_{r1} and C_{in} form a resonant circuit to deliver the resonant tank to the bulk capacitor. At t_7, v_a increases to the bulk capacitor voltage V_B, and all the energy stored in C_{in} is transferred to C_B, where the clamping diode D_{r1} begins to carry the current difference between i_s and i_{Lr1}.

M8 [t_7, t_8]: L_{r1} is shorted through S_1 and D_{r1}. So the current through L_{r1} remains constant, and the clamping diode D_{r1} carries the current difference between i_s and i_{Lr1} until the next switching cycle starts at t_8.

The above analysis shows that the capacitor C_{in} is charged by the line input through the resonance between L_{r1} and C_{in} during the time period from t_2 to t_3, while its energy is discharged to the bulk capacitor C_B, through the same resonance during the time interval from t_6 to t_7. The

instantaneous rectified line input current is equal to the average current of i_{Dx} over one switching cycle. However, the current through the diode D_x only exists during the charging period of C_{in} from t_2 to t_3. The average current of i_{Dx} over one switching cycle is given by

$$i_{Dx,ave} = \frac{1}{T_s}\int_{t_2}^{t_3} i_{Dx}\, dt\,. \tag{3.29}$$

It should be noted that the duty ratio is 50% for low line input (180 V rms) to have the lamp operate at full power. For 200 V rms line input, the required duty ratio of S_1 is about 0.39 (the duty cycle of S_2 is 0.63). Substituting (3.28) into (3.29) gives

$$\left| i_{in} \right| = i_{Dx,ave} \approx \frac{\left(D - \frac{D_c}{2}\right)\left| v_{in} \right|}{2\, Z_0}, \tag{3.30}$$

where D and D_c are the duty ratio of S_1 and the clamping diode, respectively. From (3.30), it can be seen that the average rectified input current is proportional to the line input voltage. Therefore, power factor correction can be achieved.

Based on the power balance between the input and the output under the unity power factor condition, the rectified input current is expressed as

$$\left| i_{in} \right| = \frac{2\, P_0}{h\, V_{in}^2}\left| v_{in} \right|. \tag{3.31}$$

From equations (3.8), (3.30), and (3.31), the resonant inductor L_{r1} and charge capacitor C_{in} are given by

$$C_{in} = \frac{2\, P_0}{h\ f_s\, V_{in}^2}, \tag{3.32}$$

`
$$L_{r1} = \frac{h\left(D - \frac{D_c}{2}\right)^2 V_{in}^2}{8\, f_s\, P_0}. \tag{3.33}$$

By substituting P_0 = 90 watts, η = 83%, V_{in} = 280 V (V_{in} = 200 V rms), f_s = 52 kHz, D = 0.39, D_c = 5% into (3.32) and (3.33), L_{r1} = 232 μH and C_{in} = 53 nF. The resonant capacitor C_p is chosen to be much smaller than C_{in}. Usually it can be selected at about 5%-10% of C_{in}.

For the second resonant stage of L_{r2} and C_{r2}, the excitation voltage v_a is close to a clamped sine waveform with a peak-to-peak voltage of V_B. In order to avoid high voltage stress across C_B

during the preheat and start-up modes, the resonant frequency of L_{r2} and C_{r2} is set to be close to the switching frequency in the preheat mode. Therefore, two equations are obtained by analyzing the second resonant stage, i.e.,

$$f_{s2} = f_0 = \frac{1}{2p\sqrt{L_{r2}C_{r2}}}, \tag{3.34}$$

$$V_0 = \frac{V_B}{2\sqrt{2}} \frac{1}{\sqrt{\left(1-\frac{f_{s1}^2}{f_0^2}\right)^2 + \left(2p\frac{f_{s1}L_{r2}}{R_L}\right)^2}}, \tag{3.35}$$

where V_0 is the lamp rms value, and f_{s1} and f_{s2} are the switching frequencies at normal operation (full load) and preheat mode, respectively. The lamp impedance R_L is calculated from

$$R_L = \frac{V_0^2}{P_0}. \tag{3.36}$$

If the ballast operates at 200 V rms input, and lamp power is about 90 watts with lamp voltage of 210 V rms, then the lamp impedance is 490 ohms. Substituting f_0 = 58.5 kHz, V_B = 300 V, V_0 = 210 V rms and R_L = 490 ohms into equations (3.34) and (3.35) yields

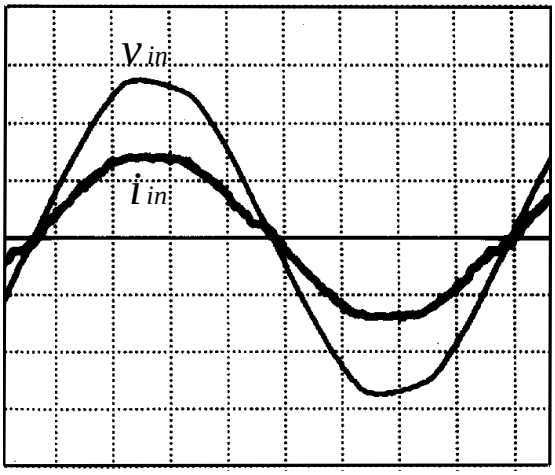
$$L_{r2} = 670\ \mu H \qquad C_{r2} = 11.2\ nF.$$

3.6.2.2 Experimental Verification

In order to verify the steady-state analysis and design procedures, the VS-VPPFC electronic ballast with second resonance was implemented with the following design parameters,

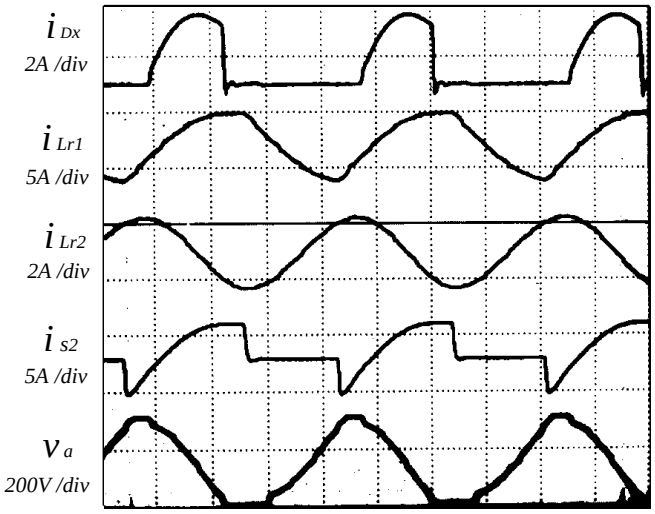
$$L_{r1} = 232\ \mu H \qquad C_{in} = 53\ nF \qquad L_{r2} = 670\ \mu H \qquad C_{r2} = 11.2\ nF.$$

The electronic ballast operates at 200V line input with two 45-watt lamp in series. The filaments are coupled with the second resonant inductor L_{r2}. The preheat and normal switching frequencies are 57.5 kHz and 52 kHz, respectively. The measured line input current waveform is shown in Fig. 3.21(a). The experimental results show that 0.995 power factor, 5% THD, and 1.5 crest factor can be achieved. The experimental switching waveforms are shown in Fig. 3.21(b). It can be seen that the experimental results verified the circuit operation and design.



t: 2 ms/div v_{in}: 100 V/div i_{in}: 0.5 A/div

(a)



t: 5 ms/div

(b)

Fig. 3.21 Experimental wveforms

(a) The measured input line current waveform

(b) The measured switching waveforms

3.6.2.3 A Family of VS-CPPFC Electronic Ballasts

Based on the circuit symmetry concept, if another charge pump is added to Fig. 3.18(b), the resulting VS-CPPFC electronic ballast is shown in Fig. 3.22(a). Two charge capacitors C_{in1} and C_{in2} are symmetrically operated in such a way that one charge capacitor is in the charge mode while the other is in the discharge mode. Thus, there are two input current pulses in one switching cycle, and the rectified line input current has twice the switching frequency. Therefore, a small size line input filter can be used. These two charge pump capacitors are designed to have the same value, which is given by

$$C_{in1} = C_{in2} = \frac{P_0}{h f_s V_p^2}. \tag{3.37}$$

The second resonant tank in Fig. 3.22(a) can be connected in the middle of two power switches S_1 and S_2. The derived VS-CPPFC electronic ballast is shown in Fig. 3.22(b). Since the excitation voltage of the resonant tank is a pure square waveform, the lamp voltage has constant amplitude with low crest factor. However, it may suffer from high voltage stress at preheat and start-up modes. Therefore, this circuit is suitable for instant start applications, where preheat is not needed.

On the other hand, the charge pump capacitor can be connected to the middle of the switch leg. The derived circuit is shown in Fig. 3.22(c) [C6, C12]. This electronic ballast has unity power factor since the body diodes of S_1 and S_2 can be used as the clamping diodes so that the unity power factor can be automatically satisfied. Figure 3.22(d) shows its symmetrical input current VS-CPPFC electronic ballast, where the rectified line current has twice the switching frequency, so a small line input filter can be used. It suffers, however, from high DC bus voltage stress during preheat and start-up mode operation. Therefore, this circuit is also only suitable for instant start application. Also, enough dead time is required for two power switches because of C_{in}, so this circuit cannot be used in dimming applications.

One symmetrical VS-CPPFC electronic ballast of Fig. 3.22(a) was implemented to verify the circuit operation, as an example. Fig. 3.23 shows the measured switching waveforms. It is shown that rectified line input current has twice the switching frequency, and a small line input filter can be used.

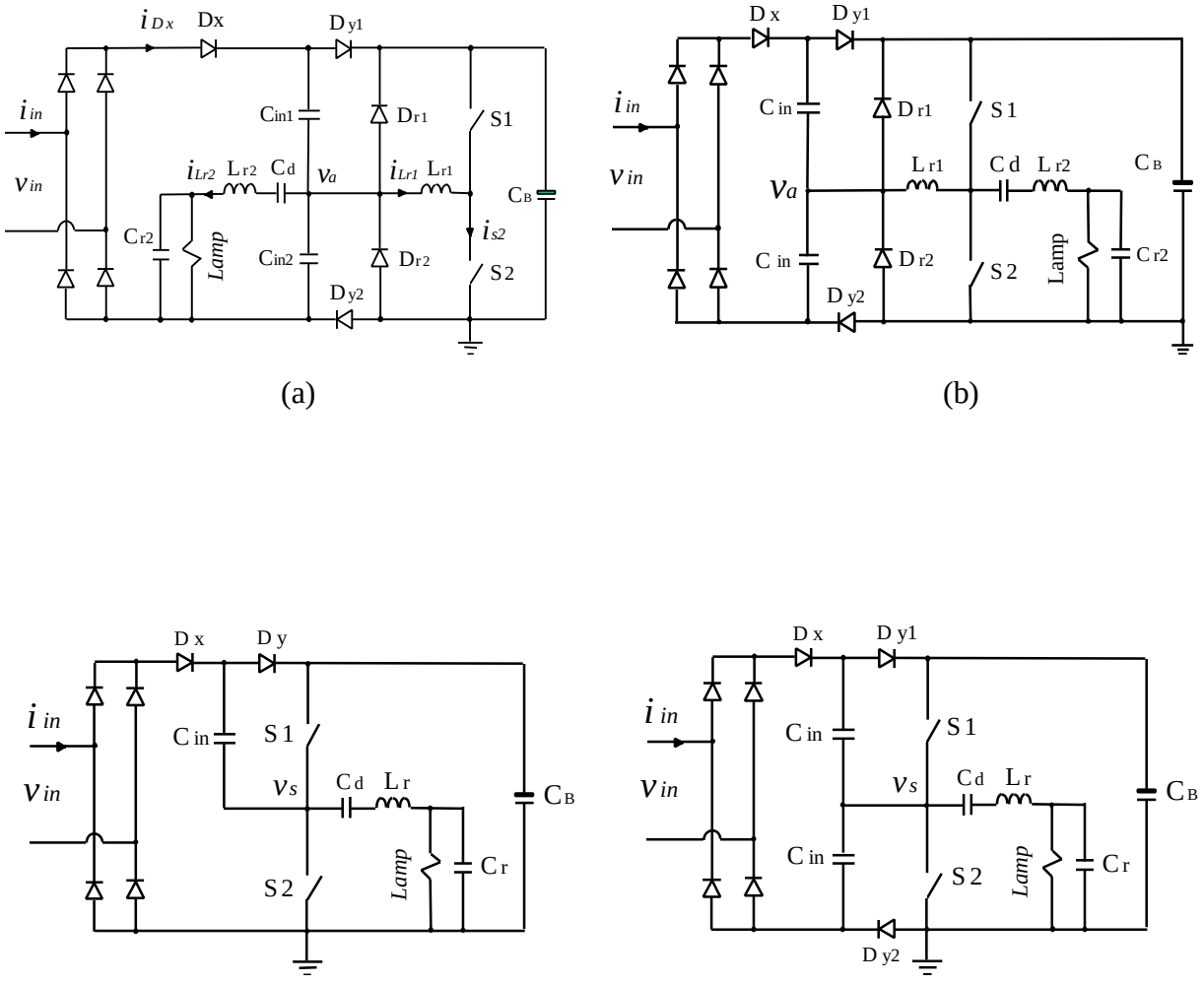


Fig. 3.22 A Family of VS-CPPFC electronic ballasts

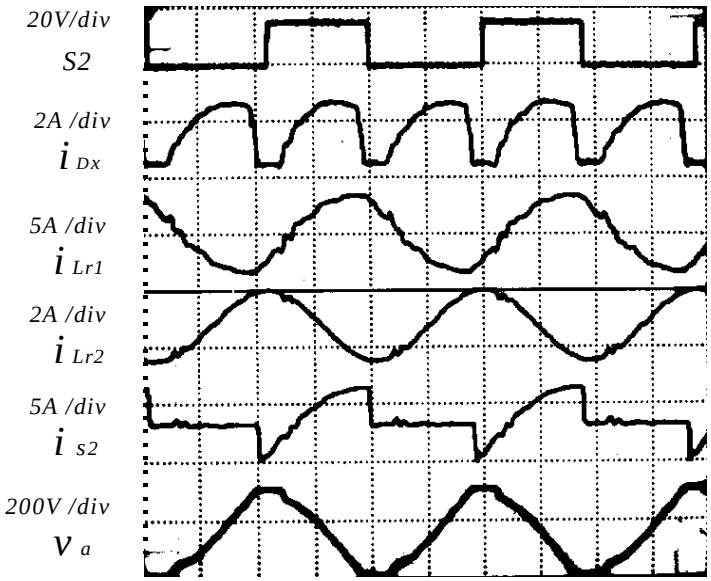


Fig. 3.23 The switching waveforms of the symmetrical CPPFC ballast

3.7 VS-CPPFC Continuous Dimming Electronic Ballast

The dimming electronic ballast is preferred in many areas such as offices, residential areas, theaters and gymnasiums. The existing dimming electronic ballasts are usually designed without any feedback control. They suffer from luminous output variation due to the lamp aging effect, variation of the circuit parameters, and especially line voltage variation. The major factor bothering the electronic ballast engineers is that the lamp characteristics are nonlinear, usually with negative dynamic impedance for a fluorescent lamp. Besides, the lamp is generally operated at the high frequency, though it behaves mostly as a pure resistance and presents a time delay because of the hysteresis phenomenon of the gas discharge ionization in the tube. These lamp characteristics affect the lamp crest factor, which is one of the important factors for lamp life time. For a single-stage CPPFC electronic ballast, DC bus voltage, crest factor and constant lamp power operation are the greatest challenges.

The lamp can generally be dimmed by using either switching frequency control, duty ratio control, or both. Here, an unbalanced duty cycle (duty ratios of S_1 and S_2 are 1-D and D, respectively) control scheme is used to dim the lamp for Fig. 3.18(b). If the duty ratios of the switches S_1 and S_2 are changed, then the output voltage v_a of the first resonant stage, composed of L_{r1} and C_p, is reduced. This decreases the excitation voltage of the second resonant stage L_{r2} and C_{r2}, which causes the output lamp power to decrease. Therefore, the lamp power can be controlled by changing the duty ratio.

On the other hand, from the analysis in 3.6.2.1, the average rectified line current over one switching cycle is given by

$$\left| i_{in} \right| \approx \frac{\left(D - \frac{D_C}{2} \right) \left| v_{in} \right|}{2 Z_0}, \tag{3.38}$$

where D is the duty ratio of power switch S_1, D_c is duty ratio of the clamping diode, and Z_0 is the characteristic impedance $Z_0 = \sqrt{\frac{L_{r1}}{C_{r1}}}$. It can be seen that the input line current decreases when the duty ratio D decreases. This means that the input power also decreases when the lamp power decreases. Therefore, this electronic ballast may not have voltage stress at the dimming mode.

To ensure that the dimming electronic ballast perform well, i.e., constant lamp power, low crest factor, and low DC bus voltage requires that I first investigate the lamp power variation with respect to the line voltage variation. The lamp current modulation scheme is used to regulate the lamp power so that the lamp operates at constant power and low crest factor.

The next section presents the development and implementation of the continuous dimming control schemes. The developed dimming electronic ballast has constant lamp power operation over a certain line voltage variation, low DC bus voltage stress, and good power factor. Finally, the experimental results will be provided to show that the developed dimming electronic ballast has good performance.

3.7.1 Constant Lamp Power Control

It is necessary to limit the lamp power variation for the line input voltage variation because the lamp may be too bright at the high line and may be too dark or even extinguished at the low

line. To maintain good light quality and make people comfortable, the lamp power variation at the same dimming level should be limited within a certain range for the line variation. Generally, the lamp power variation is a common issue for the single-stage electronic ballast, since the bus voltage is not regulated, and it depends on the line voltage. However, in the two-stage approach, the bus voltage is regulated to a fixed voltage for the input line variation through the feedback control of the power factor correction stage. As a result, the lamp power is independent of the line variation.

It should be noted that the lamp power is a function of the line input voltage with constant duty cycle control. Usually, the higher the line input, the higher the lamp power. Under the unity power factor operation, the lamp power P_L is given by

$$P_0 = \frac{1}{2}h \quad f_s \, C_{in} \, V_{in}^2, \tag{3.39}$$

where V_{in} and h are the peak line input voltage and efficiency, respectively. Equation (3.39) shows that the lamp power is proportional to the square of the line peak voltage. Therefore, there is at least ±21% lamp power variation when the line changes only ±10%. This lamp power change is contradictory to the dimming electronic ballast requirement, according to which the maximum lamp power variation is usually limited to ±15% when the line voltage changes ±10%. Figure 3.24 shows the lamp power variation and crest factor at different dimming level without any feedback control for Fig. 3.18(b). It can be seen that the lamp power variation is from +78% to -45%. This tremendous power variation range is not acceptable. Thus, it is necessary to develop a new control technique to limit this lamp power variation so that the developed dimming electronic ballast can meet the lamp power variation requirement.

3.7.1.1 Feed-Forward Lamp Power Control

It is natural to use the line voltage feed-forward loop to compensate for the lamp power variation. The feed-forward loop operates in such a way that it can adjust the duty ratio of the power switch so that the lamp power variation keeps at the minimum. When the line input voltage is high, the duty cycle is smaller than that of the normal input through the feed-forward loop. When the line input voltage becomes low, the duty ratio is adjusted to be larger so that the lamp power cannot drop too much. The experiments show that the duty ratio variation range is

required to vary from 0.3 to 0.5 at full lamp power operation when the input voltage changes from 110 V to 90 V. Because the duty ratio modulation is a function only of the line peak voltage at low dimming level operation, the duty ratio variation range is from 0.1 to 0.3. However, the lamp power is only about 5 watts with 0.1 duty ratio operation at high line, while the lamp power is about 28 watts with a duty ratio of 0.3 at 90 V input. Therefore, the problem occurs at high line, where the lamp may extinguish because lamp power is too low. It is impossible to keep the lamp power variation within ±15% for all dimming levels. Therefore, this approach cannot meet the requirement over all dimming levels.

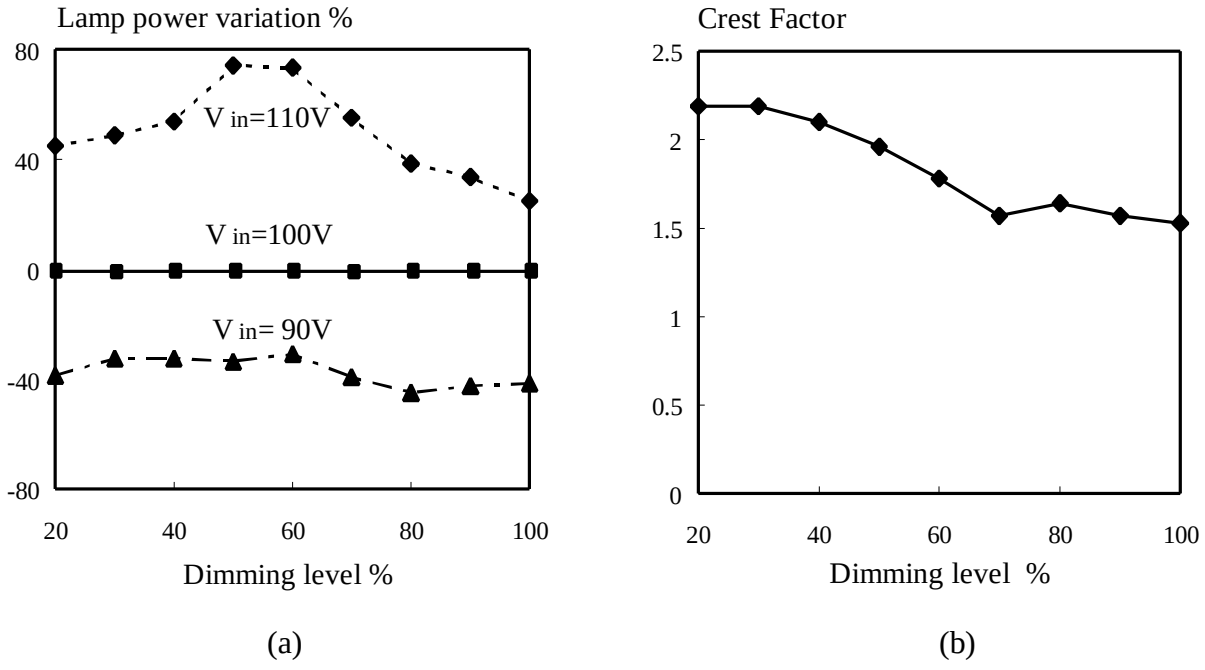


Fig. 3.24 (a) Lamp power variation without feedback control

(b) Crest factor at dimming levels without feedback control

3.7.1.2 Average Lamp Current Control with Duty Ratio Modulation

The lamp current waveform has large low frequency ripple which deteriorates the lamp crest factor especially at high dimming level, where the lamp crest factor is high either from using feed-forward control or without feedback control. This large crest factor may shorten the lamp life and cause flicker in a low temperature environment. Thus, it is necessary to control the lamp crest factor. Basically, the lamp power is the function of the lamp current and voltage. If the lamp current can be controlled in such a way that the lamp has a constant amplitude for different input voltages at a certain dimming level, then the lamp operates in constant power and has low crest factor. Therefore, as long as the lamp current has constant amplitude, constant lamp power operation and low crest factor can be simultaneously obtained. Besides, the lamp current control method is more accurate than the peak line voltage modulation method, since lamp current control is direct, while the peak line voltage modulation is indirect. In the following, average lamp current control method will be developed to evaluate the performance of the dimming function.

Figure 3.25 shows the developed average lamp current control with duty ratio modulation to improve the crest factor and keep constant lamp power operation. A current sensor CT is used to detect the lamp current. R_1 is a sampling resistor to convert the lamp current signal into the voltage signal. R_4 and C_1 are composed of a low pass filter to block the high frequency

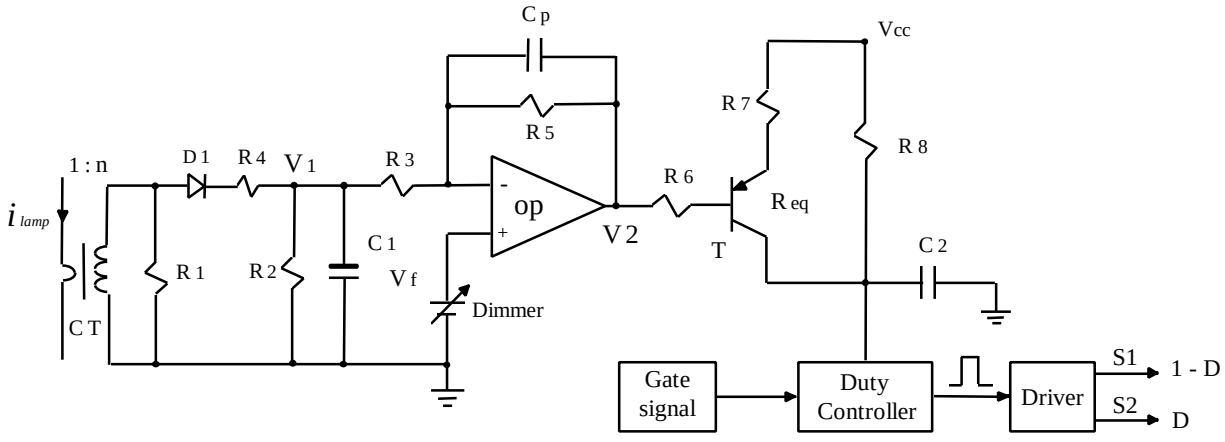


Fig. 3.25 The average lamp current controller with duty ratio modulation

component as high as the switching frequency, while allowing the low frequency component as low as the line frequency so that a DC voltage signal V_1, including the line frequency ripple seen in the lamp current, is fed to the error amplifier. The feedback compensator consists of R_3, R_5, C_p and error amplifier OP. The output signal V_2 of the error amplifier controls the variable of resistance transistor T so that finally the equivalent timing resistance is modulated. As a result, the duty ratio is modulated in such a way that the lamp current follows the reference lamp current v_f through this closed loop control. In other words, the duty controller determines the on-time ratio in such a manner as to decrease the lamp current when the input voltage V_1 to the error amplifier increases, and to increase the lamp a current as the voltage V_1 to the error amplifier decreases. With this control, the ballast is made to feed the lamp current of substantially constant level with reduced crest factor at normal or rated lighting operation. For an example, when the detected lamp current is higher than the reference, the output voltage of the error amplifier also decreases, which increases the base current of the transistor T. As a result, the output resistance across the collector and emitter path of T is reduced, and the equivalent timing resistance becomes small. Therefore, the duty ratio decreases, which makes the ballast provide less lamp current. When the lamp current is lower than the reference, through the same operation mechanism, the duty ratio increases, and the ballast supplies higher lamp current. Therefore, the lamp current can be regulated to a constant amplitude so that a low crest factor can be obtained in dimming mode.

The dimmer signal V_f controls the lamp power. When a higher dimming level is needed, the dimmer signal V_f decreases so that the lamp current follows the setting lamp current V_f through this dimming control. While a lower dimming level is required, the dimmer signal voltage V_f simply increases. Therefore, it is easy to dim the lamp by adjusting only the dimming reference voltage V_f. By properly designing the compensator parameters, the system is stable and the lamp power variation range with respect to the line variation is reduced to a minimum.

3.7.2 Experimental Verification

In order to verify the proposed continuous dimming average lamp current controller with duty ratio modulation, the CPPFC continuous dimming electronic ballast of Fig. 3.17(b) is developed. For 100 V line input, the designed electronic ballast parameters are:

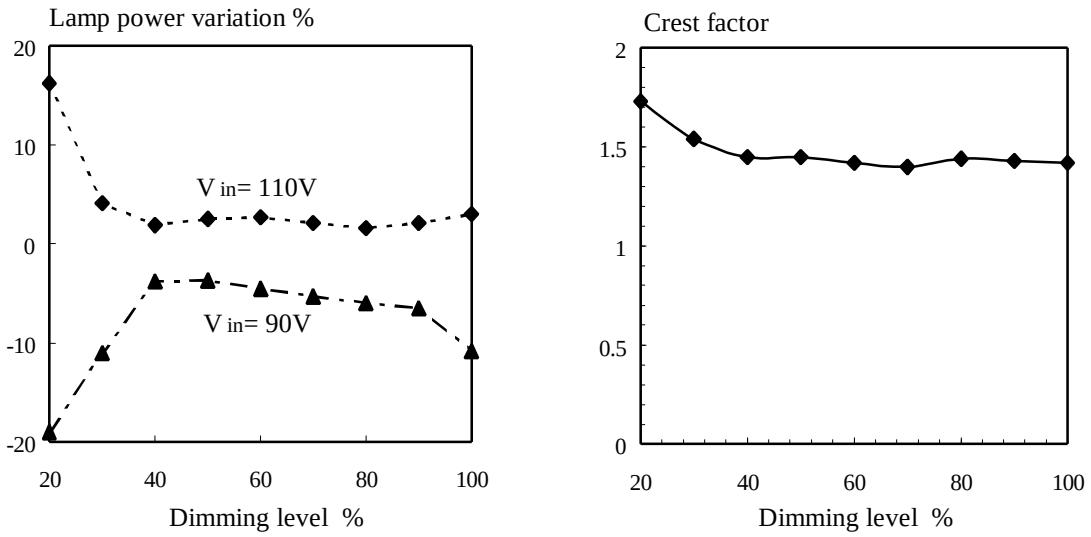
L_{r1} = 60 μH C_p = 33 nF C_{in} = 220 nF L_{r2} = 290 μH C_{r2} = 28 nF

The circuit parameters of the dimming controller of Fig. 3.4 are designed as follows:

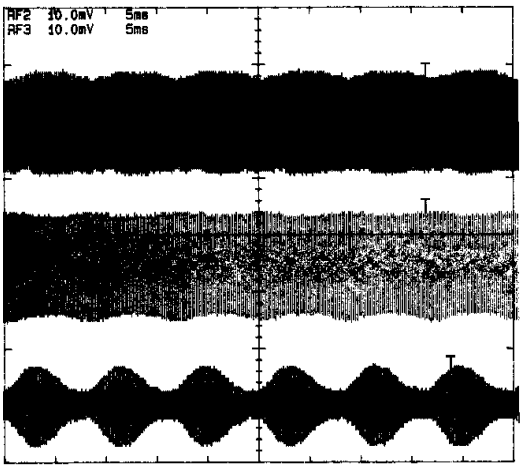
CT: n = 40 R_1 = 820 Ω R_3 = 10 kΩ R_5 = 30 kΩ C_p = 15 nF C_1 = 22 nF

T: 2N3906 OP: LM358 R_7 = 5.1 kΩ R_8 = 51 kΩ C_2 = 120 pF

Based on the developed average lamp current control with switching frequency modulation, the continuous dimming CPPFC electronic ballast was implemented and tested with two 40-w lamps in series. If the lamp power at 100 V rms input is used as a reference, the measured lamp power variation at 90 V rms and 110 V rms at different dimming levels is that shown in Fig. 3.26(a) (full power P_0 = 80-w at 100% dimming). It is shown that the lamp power variation range is limited within ±15% from 20% to 100% dimming at room temperature. Figures 3.26(b) and 3.26(c) show crest factor and the measured lamp current waveforms, respectively, at different dimming levels. It can be seen that the lamp current waveform has less low frequency ripple, so the crest factor is improved. The measured crest factor is as low as 1.9 even at 20% dimming. Therefore, the lamp have potentially long life. The measured THD, power fcator, line current with 100%, 50%, and 20% dimming levels with 100 V rms input are shown in Figs. 3.27(a), (b), and (c), respectively. It is shown that higher than 0.99 power factor can be obtained, and the measured line current harmonics meet the IEC 1000-3-2 Class C requirements from 20% to 100% dimming levels. Figure 3.27(d) shows the switching current waveforms through S_1 at 100%, 50%, and 20% dimming. It can be seen that zero voltage switching operation can be always obtained, so the electronic ballast operates efficiently. Figure 3.28(a) shows the measured overall efficiency of the electronic ballast (the total losses include filament loss and power loss of the electronic ballast). The measured maximum DC bus voltage stress from 20% to 100% dimming is shown in Fig. 3.28(b). The maximum DC bus voltage is only about 215 V, so a 250 V rated bulk capacitor and power MOSFETs can be used. The developed continuous dimming electronic ballast was also tested at low environmental temperature. It was found that it has no flicker at all, and the lamp operates in constant power and low crest factor by using the developed average lamp current control with duty ratio modulation.



(a) (b)



t: 5 ms/div

(c)

Fig. 3.26 (a) Lamp power at different dimming level

(b) Lamp crest factor at different dimming level

(c) Top waveform: Lamp current at 100% dimming, 0.5 A/div

Middle waveform: Lamp current waveform at 50% dimming, 0.2 A/div

Bottom waveform: Lamp current waveform at 20% dimming, 0.2 A/div

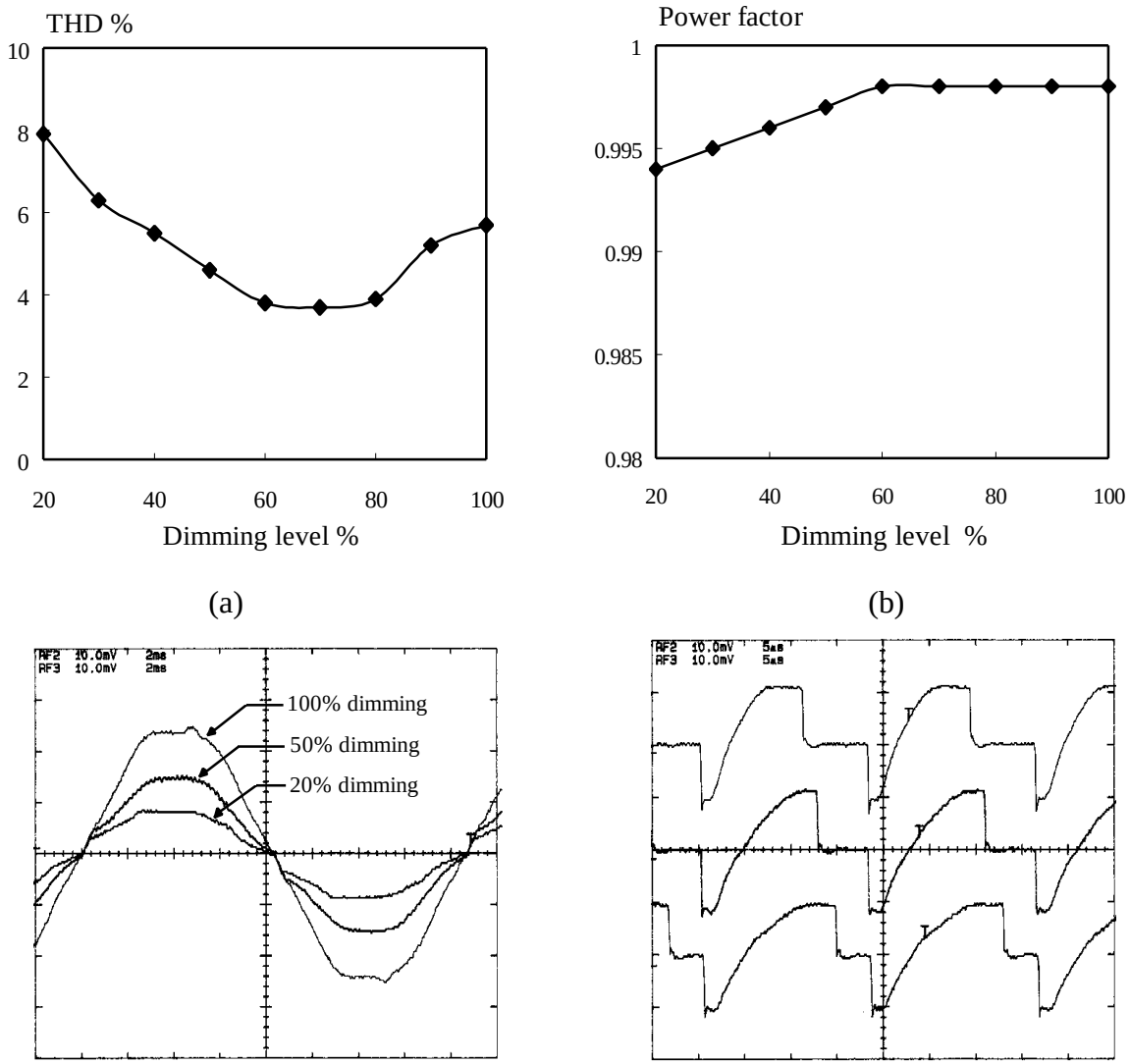
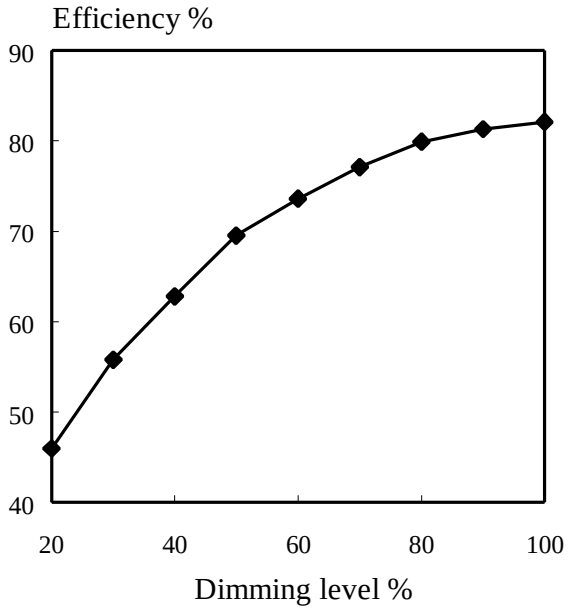


Fig. 3.27 (a) THD at different dimming levels

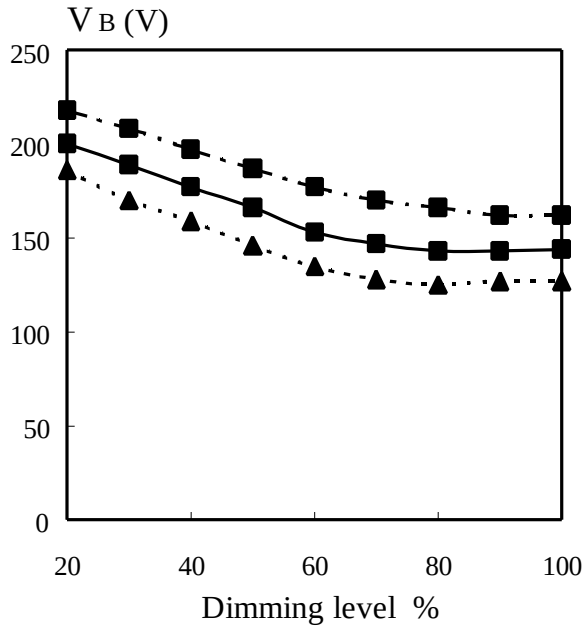
(b) Power factor at different dimming levels

(c) Measured line input current waveforms at 100%, 50%, and 20% dimming

(d) Measured switching current waveforms at 100%, 50%, and 20% dimming



(a)



(b)

Fig. 3.28 (a) Overall efficiency at different dimming level

(b) DC bus voltage at different dimming level

3.7 Summary

The charge pump power factor correction technique is very attractive because a capacitor is used to shape the line input current waveform, and a capacitor is cheaper than an inductor. In this chapter, the CPPFC concept was proposed and established. A VS-CPPFC converter and its unity power factor condition were derived. Based on the derived VS-CPPFC converter, VS-CPPFC AC/DC converters were proposed, analyzed, and implemented. The experimental results showed that unity power factor can be obtained and DC bus voltage stress can be limited.

One VS-CPPFC electronic ballast was presented and analyzed. Design guidelines are provided so that the electronic ballast operates at optimum conditions. A family of VS-CPPFC electronic ballasts was derived, and it was shown that the rectified line input current of the symmetrical VS-CPPFC converter has twice the switching frequency so that a small line input filter can be used.

One continuous dimming electronic ballast was also proposed. Constant lamp power control with duty ratio modulation was developed so that the lamp power variation is limited within 15% with respect to a 10% line voltage variation. Low crest factor and THD can be achieved over a wide dimming range from 20% to 100% dimming levels.

CHAPTER 4

CURRENT SOURCE CHARGE PUMP POWER FACTOR CORRECTION (CS-CPPFC) CONVERTERS

4.1 Introduction

The integrated single-stage power factor correction converters suffer from high current stresses in the power switches; they tackle the current not only from the reflected load but also from the power factor correction stage. Their current stresses are almost twice as much as those of the two-stage approach. These high stresses are undesirable simply because high current rating devices have to be used, and as a result, the cost cannot decrease much, compared with the two-stage approach. Unfortunately, the presented VS-CPPFC converters also have this disadvantage. So it is very attractive to develop a new single-stage power factor correction converter with small current and voltage stresses. Theoretically, the minimum switching current stress in power switches for the electronic ballast application is the resonant inductor current in a DC/AC stage. In other words, the switches only take the reflected load current, and the switching current is minimized so that a low cost device can be used.

In this chapter, current source charge pump power factor correction (CS-CPPFC) converters are presented. In these converters, the power switches deal only with the reflected load current, which is the same as that of the two-stage approach. The presented single-stage CS-CPPFC converter can use devices with the same current rating as those of two-stage approach. Also, a capacitor is employed to obtain the power factor correction function, and magnetic components are minimized. Therefore, the developed single-stage CPPFC perform well and are extremely low cost. The next section presents the basic CS-CPPFC converter, followed by the

analysis and derivation of its unity power factor condition. A CS-CPPFC electronic ballast based on the CS-CPPFC converter is presented, and its steady state analysis and design considerations are provided. A family of CS-CPPFC electronic ballasts are derived. Finally, the experimental results are provided to verify the proposed CS-CPPFC technique.

4.2 Circuit Derivation

Figure 4.1(a) shows the charge pump power factor correction converter block diagram. The signal S, either a high frequency voltage source or a high frequency current source, charges and discharges capacitor C_{in} to achieve power factor correction. Series-resonant parallel-loaded inverters are commonly used in electronic ballasts. It is easy to obtain this high frequency signal. The VS-CPPFC converter shown in Fig. 4.1(b) was derived and analyzed in Chapter 3. The high frequency voltage source v_a in series with a capacitor C_{in} charges and discharges the capacitor C_{in} to absorb energy from the ac line and pump its stored energy to the bulk capacitor C_B. This voltage source in series with a capacitor can be represented as a high frequency current source i_s in parallel with a capacitor C_{in} as a Norton form, shown in Fig. 4.1(c). Thus, C_{in} can be either charged or discharged by the high frequency current source i_s. Therefore, this converter can be called a Current Source Charge Pump Converter. The charge pump capacitor C_{in} can be shifted to parallel with D_y, based on the capacitor shift rule. Figure 4.1(d) shows another CS-CPPFC converter. In the next section, the unity power factor condition will be analyzed.

4.3 Unity Power Factor Condition

In order to fully understand this CS-CPPFC converter, it is necessary to analyze its unity power factor condition. Four topological stages exist over one switching cycle, and their switching waveforms are shown in Fig. 4.2.

M1 $[t_0, t_1]$: Before t_0, the current source i_s has a negative value, and it flows through the diode D_y. The voltage at node *m* is clamped to the bus voltage V_B. At t_0, i_s becomes positive and begins to charge C_{in}. The charge capacitor voltage v_c begins to rise while v_m decreases. So, the charge capacitor C_{in} accumulates energy from the DC bus. This mode terminates at t_1, where the voltage at node *m* decreases to the line input voltage, and D_x starts to conduct. The time interval t_1 is determined by

$$t_1 = \frac{1}{w_s} arc^{-1} cos\left[1 - \frac{w_s C_{in}}{I_s}\left(V_B - |v_{in}|\right)\right], \tag{4.1}$$

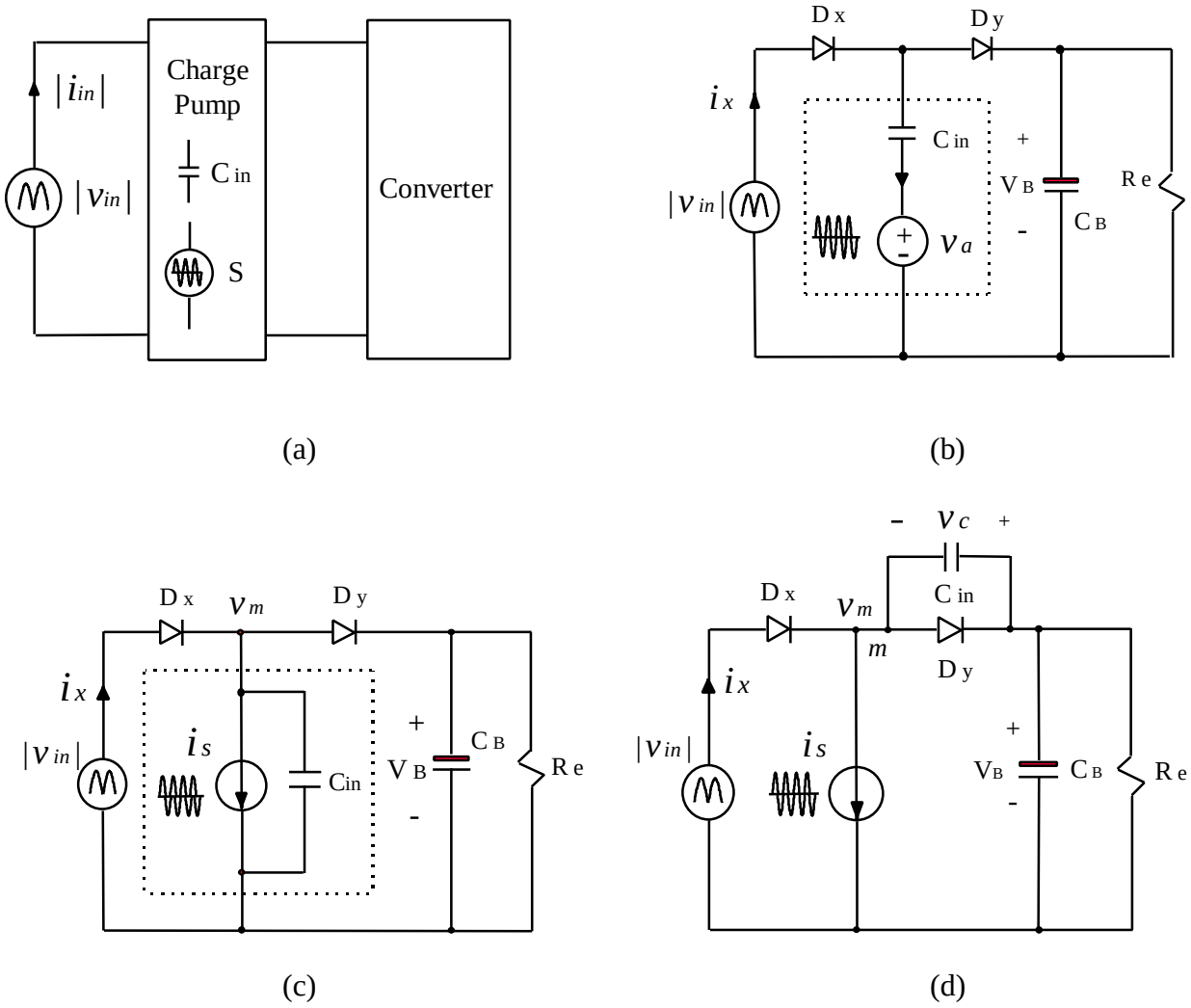
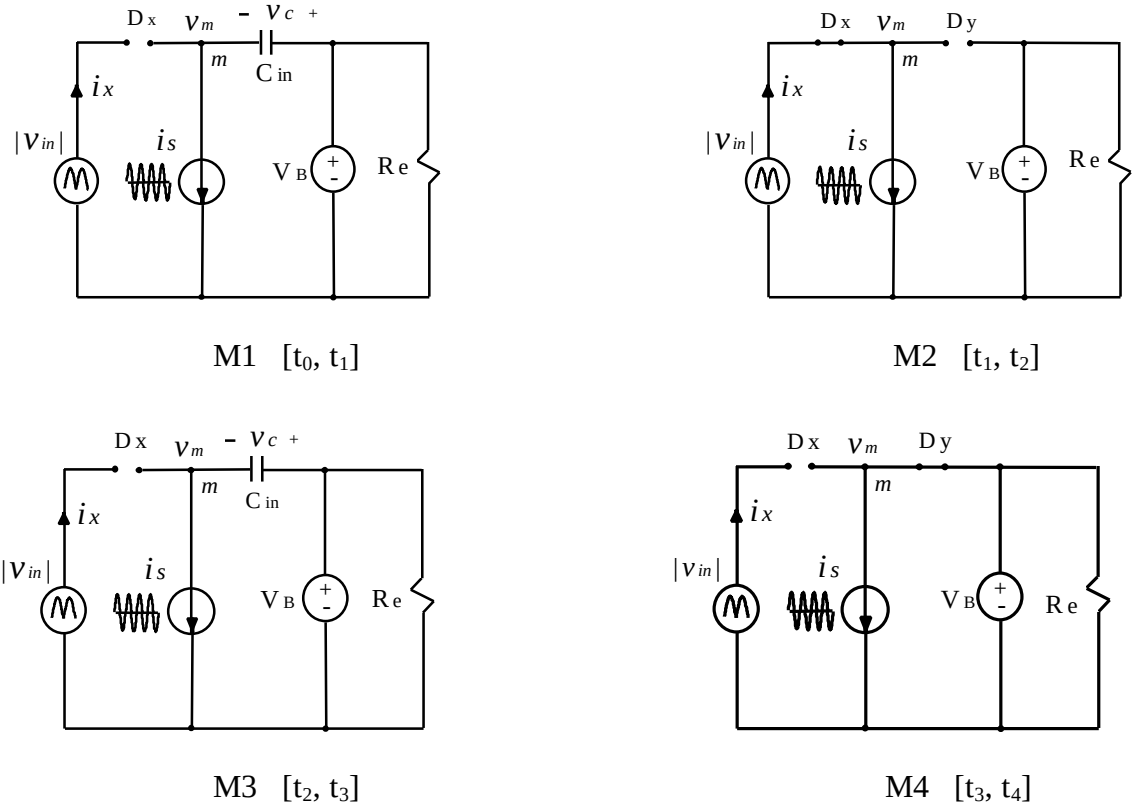


Fig. 4.1 (a) The CPPFC converter block diagram

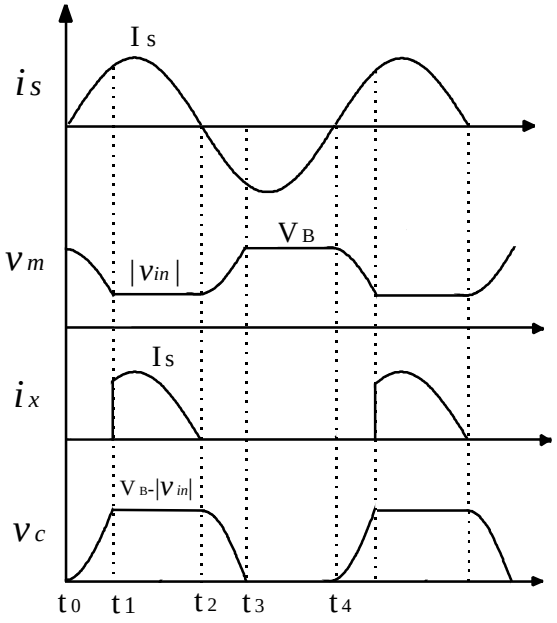
(b) VS-CPPFC converter

(c) CS-CPPFC converter

(d) Another CS-CPPFC converter



(a)



(b)

Fig. 4.2 Four equivalent topological stages and switching waveforms

where w_s is the frequency of current source i_s, and V_B is the voltage across the bulk capacitor C_B. The total charge variation in C_{in} is given by

$$D\,Q = C_{in}\left(V_B - \left| v_{in} \right| \right). \tag{4.2}$$

There is no input line current during this stage.

M2 [t_1, t_2]: At t_1, diode D_x begins to turn on, and v_m is clamped to the rectified line input voltage. Current source i_s flows through the line input and D_x. Therefore, the high frequency current source i_s absorbs energy directly from the ac line. At $t_2 = T_s/2$, current i_s becomes negative, while D_x is naturally turned off, and this mode ends. During this time interval, the rectified line current i_x is given by

$$i_x = i_s = I_s \sin w_s t \qquad t_1 < t < t_2 . \tag{4.3}$$

M3 [t_2, t_3]: At t_2, current source i_s becomes negative and D_x is naturally off. Since v_m is still lower than the DC bus voltage V_B, D_y cannot be turned on at this time. Current source i_s is discharging C_{in}, and the voltage at node *m* increases. v_m rises to the DC bus voltage, where D_y starts to conduct at t_3.

M4 [t_3, t_4]: At t_3, D_y begins to flow the source current i_s, and the voltage at node *m* is clamped to the DC bus voltage until i_s becomes positive, and D_y is naturally turned off at $t_4 = T_s$.

The average rectified input line current equals the average diode current i_x over one switching cycle, which is given by

$$\left| i_{in} \right| = i_{x,ave} = \frac{1}{T_s} \int_{t_0}^{t_4} i_x \, dt = \frac{1}{T_s} \int_{t_1}^{t_2} i_s \, dt , \tag{4.4}$$

where T_s is the switching period. After substituting i_s into the above equation, we have

$$\left| i_{in} \right| = \frac{I_s}{p} - \frac{D\,Q}{T_s} , \tag{4.5}$$

where $D\,Q$ is the charge variation of C_{in} and $D\,Q = C_{in}\,(V_B - | v_{in} |)$. Therefore, the average rectified line current i_x in one switching period is

$$\left| i_{in} \right| = \left(\frac{I_s}{p} - C_{in}\, f_s\, V_B \right) + C_{in}\, f_s \left| v_{in} \right|. \tag{4.6}$$

In order to achieve the unity power factor, the average input current should be proportional to the line input voltage. The first term of the above equation should be zero, which is given by

$$I_s = p\ C_{in}\ f_s\, V_B. \tag{4.7}$$

This equation (4.7) is the unity power factor condition. Then (4.6) becomes

$$\left| i_{in} \right| = C_{in}\, f_s \left| v_{in} \right|. \tag{4.8}$$

Eq. (4.8) shows that the unity power factor can be obtained as long as eq. (4.7) can be satisfied.

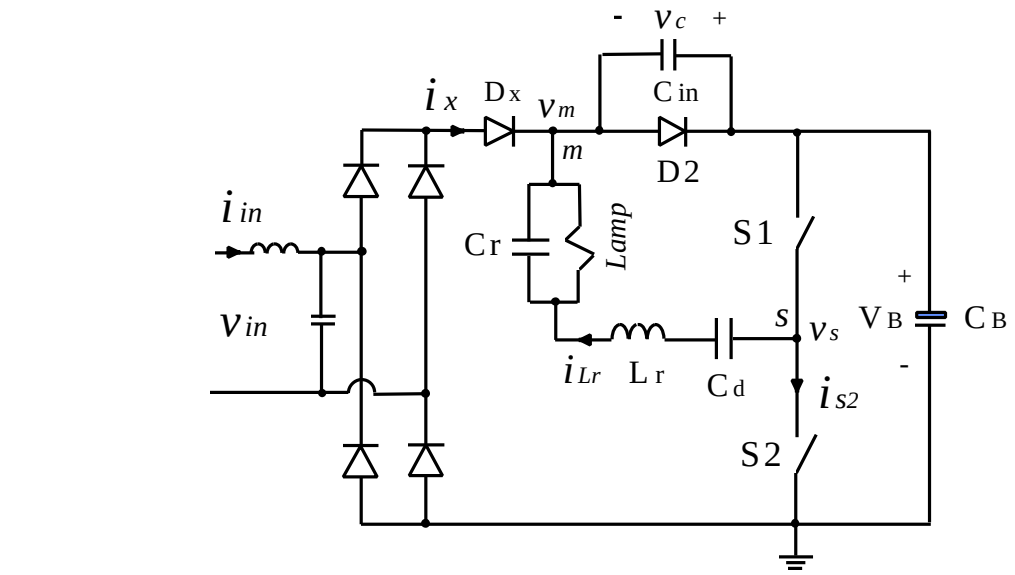
4.4 Current Source Charge Pump Power Factor Correction Electronic Ballast

4.4.1 Principle of Operation

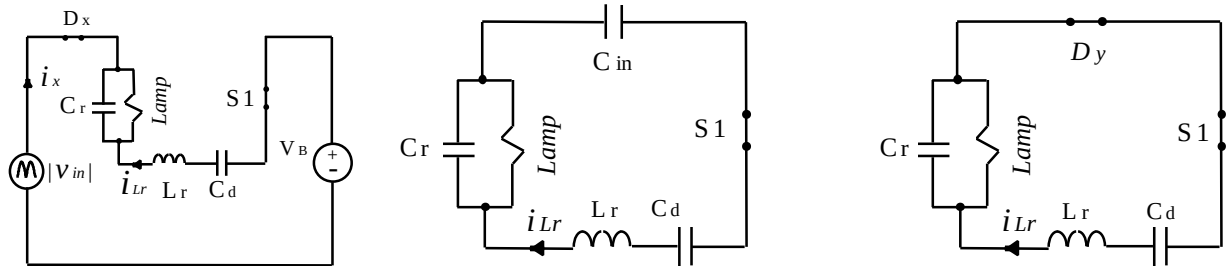
Since the series resonant parallel-loaded tank can be considered a high frequency current source if the load voltage is constant, current source i_s in Fig. 4.1(d) can be replaced by a series resonant parallel-loaded tank. The resulting circuit is shown in Fig. 4.3(a). This tank consists of a DC blocking capacitor C_d, resonant inductor L_r, capacitor C_r, and a lamp which is in parallel with the resonant capacitor C_r to absorb high frequency energy. C_{in} serves as the charge pump capacitor. In steady state, six topological stages exist over one switching cycle, as shown in Fig. 4.3(b). The switching waveforms are shown in Fig. 4.4.

M1 [t_0, t_1]: At t_0, S_2 is turned off and S_1 is turned on. Since i_{Lr} is still negative, this resonant current continues to flow through D_x and the ac line to absorb energy from the line input. From the equivalent circuit of Fig. 4.3(b), this resonant current is also charging C_B. D_x is naturally turned off at t_1, where the resonant inductor current equals zero.

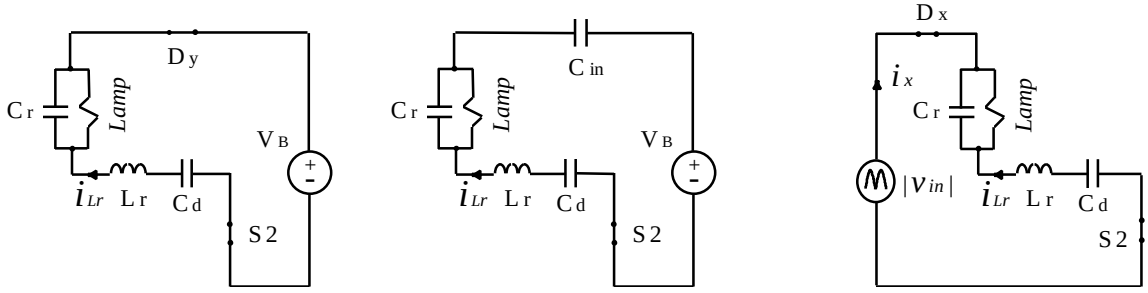
M2 [t_1, t_2]: The resonant inductor current reverses at t_1. Because v_m is now higher than the rectified line voltage and lower than the DC bus voltage V_B, both D_x and D_y are off. i_{Lr} discharges C_{in}. C_{in} is actually a part of the resonant element during this time period. C_{in} is totally discharged



(a)



M1 $[t_0, t_1]$ M2 $[t_1, t_2]$ M3 $[t_2, t_3]$



M4 $[t_3, t_4]$ M5 $[t_4, t_5]$ M6 $[t_5, t_6]$

(b)

Fig. 4.3 CS-CPPFC electronic ballast and its six topological stages

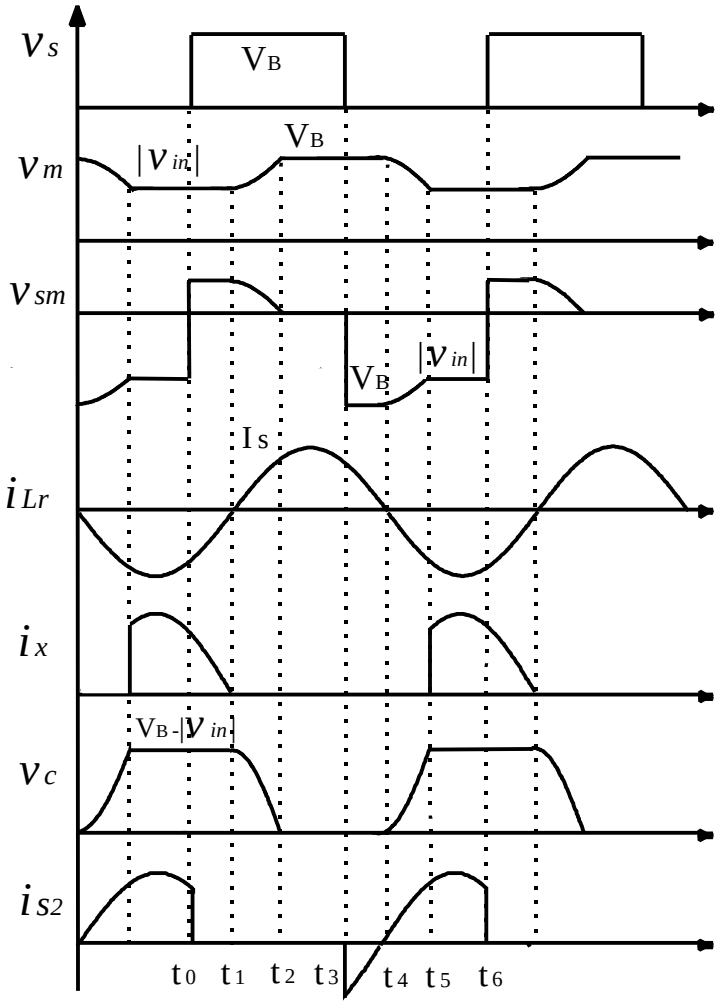


Fig. 4.4 Switching waveforms of Fig. 4.3

at t_2, where D_y becomes forward-biased and begins to conduct the resonant inductor current. The equivalent circuit is shown in Fig. 4.3(b).

M3 [t_2, t_3]: The lamp energy is provided by the DC blocking capacitor, and the converter simply becomes a series resonant parallel-loaded tank. This mode lasts until t_3, when S_1 is turned off.

M4 [t_3, t_4]: S_2 is turned on when S_1 is turned off at t_3. D_y is still conducting the resonant inductor current. i_{Lr} becomes negative at t_4, where D_y is naturally turned off. The equivalent circuit is shown in Fig. 4.3(b).

M5 [t_4, t_5]: v_m cannot change abruptly because C_{in} is connected in parallel with D_y. The negative resonant inductor current is charging C_{in}, and v_m decreases until t_5, where v_m equals the rectified line voltage and D_x starts to conduct.

M6 [t_5, t_6]: v_m is clamped by the rectified line input voltage, and the resonant tank is excited by the line input. The resonant tank absorbs energy from the line input. This mode ends at t_6 when S_2 is turned off.

The equivalent circuit shows that the time intervals [t_1, t_2] and [t_4, t_5] during which C_{in} is connected in the resonant tank are the maximum near the zero crossing line input voltage, since the total stored charge in C_{in} has to be discharged during these time intervals. However, the total charge stored in C_{in} is given by

$$D\,Q = C_{in}\left(\,V_B - \left|\,v_{in}\,\right|\right). \tag{4.9}$$

DQ reaches its maximum value when $v_{in} = 0$, where it takes the longest time to fully charge and discharge C_{in}. To maintain zero voltage switching operation, the switching frequency has to be higher than the resonant frequency, that is:

$$f_s > \frac{1}{2\,p\sqrt{\dfrac{C_{in}C_r}{C_{in}+C_r}\;L_r}}. \tag{4.10}$$

Since there are six resonant mode operations, and each resonant mode has a different excitation tank voltage, the current i_{Lr} may not have constant amplitude, which causes the lamp current waveform to have low frequency ripple and deteriorates the lamp crest factor. In order to improve the crest factor, suitable modulation is needed. This will be discussed in the next section.

4.4.2 Design Considerations

The design objective is to find the charge capacitor value C_{in}, and the resonant components L_r and C_r. To optimally design this CS-CPPFC electronic ballast, the following should be taken into account.

- Minimum DC bus voltage, $V_B = V_{in}$, where V_{in} is the line peak voltage.
- Satisfying the unity power factor condition

$$I_s = p \ f_s \ C_{in} \ V_B . \tag{4.11}$$

- Maintaining ZVS, that is

$$f_s > \frac{1}{2 \ p \sqrt{\frac{C_{in} C_r}{C_{in} + C_r} \ L_r}} . \tag{4.12}$$

The input power over one switching cycle is the product of the instantaneous input voltage and the average rectified input current over one switching cycle, which is given by

$$p_i(t) = \left(\ \frac{I_s}{p} - C_{in} \ f_s \ V_B \right) \left| \ v_{in}(t) \ \right| \ + \ C_{in} \ f_s \left| \ v_{in}(t) \ \right|^2 . \tag{4.13}$$

By averaging the above equation in a line cycle if $v_{in}(t) = V_{in} \ sin w_L t$, where w_L is the line frequency, the average input power P_i is

$$P_i = \frac{2 \ V_{in}}{p} \left(\ \frac{I_s}{p} - C_{in} \ f_s \ V_B \right) + \ \frac{1}{2} \ C_{in} \ f_s \ V_{in}^2 . \tag{4.14}$$

Under the unity power factor condition operation, the first term of (4.14) is zero, and (4.14) can be expressed as

$$P_i = \frac{1}{2} \ C_{in} \ f_s \ V_{in}^2 . \tag{4.15}$$

Based on the power balance between the input and the output,

$$P_0 = h \ P_i , \tag{4.16}$$

where P_o and h are the output power and the conversion efficiency, respectively. The charge capacitor C_{in} can be determined by

$$C_{in} = \frac{2\,P_0}{h\,f_s\,V_{in}^2}. \tag{4.17}$$

For a given peak line voltage V_{in}, switching frequency f_s, and lamp power P_0, the charge capacitance C_{in} can be calculated from (4.17).

Figure 4.5 shows the series resonant parallel-loaded tank and its excitation voltage waveform. It can be seen that the excitation voltage v_{sm} is actually not pure square waveform, and is modulated by the rectified line voltage. To simplify this resonant tank design, the converter is designed near the peak line voltage, where the excitation voltage is close to a pure square waveform. The peak-peak voltage of v_{sm} is the DC bus voltage. If only the fundamental component is taken into account, the output voltage v_0 and the resonant inductor peak current are given by

$$V_{0,rms} = \frac{\sqrt{2}\,V_B}{p}\frac{1}{\sqrt{\left(1-\frac{w_s^2}{w_0^2}\right)^2+\left(\frac{w_s\,L_r}{R_L}\right)^2}}, \tag{4.18}$$

$$I_{Lr,p} = \frac{2\,V_B}{p}\frac{\sqrt{\left(w_s C_r\right)^2+\frac{1}{R_L^2}}}{\sqrt{\left(1-\frac{w_s^2}{w_0^2}\right)^2+\left(\frac{w_s\,L_r}{R_L}\right)^2}}, \tag{4.19}$$

where $w_s = 2p\,f_s$, and $w_0 = \frac{1}{\sqrt{L_r C_r}}$. In order to achieve unity power factor, (4.19) should equal (4.17).

The lamp can be considered a pure resistance with a negative dynamic impedance at normal operation. So R_L can be determined by

$$R_L = \frac{V_{0,rms}^2}{P_0}. \tag{4.20}$$

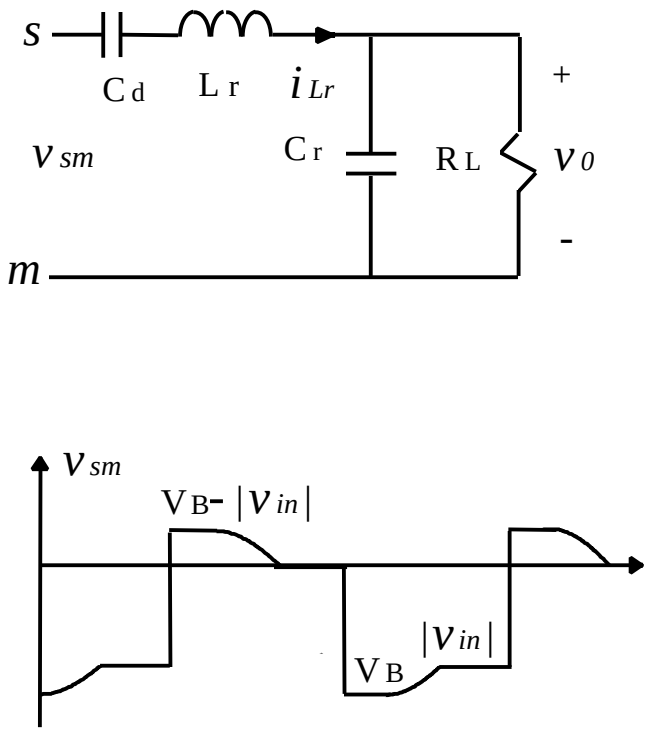


Fig. 4.5 The series resonant tank and its excitation voltage

For a given lamp power P_0 = 85 watts, the lamp voltage for two lamps in series is about 230 V rms, and lamp resistance is 620 Ω. If f_s = 52 kHz, V_B = 280 V, V_{in} = 280 V and η = 85%, charge capacitor C_{in}, the required resonant peak inductor current and resonant components L_r, C_r can be calculated through Mathcad software,

C_{in} = 46 nF $I_{Lr,p} = I_s$ = 2 A L_r = 680 μH C_r = 19.6 nF.

After checking the zero voltage condition, (4.12) is satisfied.

4.4.3 A Family of CS-CPPFC Electronic Ballasts

Several CS-CPPFC electronic ballasts can be derived, based on the high frequency capacitor shift rule and symmetrical circuit concept. The high frequency capacitor can be shifted

through any DC voltage or low impedance path like the DC bulk capacitor. C_{in} can be shifted through C_B to the ground in Fig. 4.3(a), and the derived CS-CPPFC electronic ballast is shown in Fig. 4.6(a) [D6]. If C_{in} of Fig. 4.3(a) is separated into two capacitors, C_x and C_y, then the circuit will become the one in Fig. 4.6(b) [D1]. If C_y is shifted through C_B to the ground from Fig. 4.6(b), then the resulting circuit becomes the one in Fig. 4.6(c) [D1]. If a symmetrical charge pump tank is added to Fig. 4.6(b), then the resulting CS-CPPFC electronic ballast becomes the one shown in Fig. 4.6(d) [D1]. This circuit is symmetrical and two input current pulses exist over one switching cycle. As a result, current stress in the line rectifier is reduced and a small input line filter can be used. On the other hand, in Fig. 4.6(d) if both capacitors C_{y1} and C_{y2} are shifted through C_{x1} and C_{x2}, respectively, then the derived circuit becomes another symmetrical CPPFC electronic ballast, shown in Fig. 4.6(e) [D1]. From Fig. 4.6(e), C_{y1} can be considered the equivalent of C_{x1}, C_{x2}, and C_{y2} because these capacitors form a loop, C_{y1} can be saved. The derived electronic ballast is shown in Fig. 4.6(f). Both Figures 4.6(d) and (e) have symmetrical input current with which a small line filter can be employed. The expenses include the cost of adding extra diodes and high frequency capacitors. These derived CS-CPPFC electronic ballasts have similar performance to that of Fig. 4.3(a).

4.4.4 Experimental Verifications

Based on the above analysis and design parameters, the CS-CPPFC electronic ballast of Fig. 4.3(a) was implemented to verify its operation. The electronic ballast operates two 45-watt lamps in series with 200 V rms line input. The switching frequencies at normal operation and preheat mode are about 56 kHz and 90 kHz, respectively. If the electronic ballast operates in constant switching frequency and duty cycle without any modulation, the lamp current waveform is shown in Fig. 4.7. The measured lamp crest factor is 1.85. It can be seen that the lamp current waveform is modulated by twice the line frequency, which means that the lamp current has large low frequency ripple. This is mainly because there are six resonant mode operations, shown in

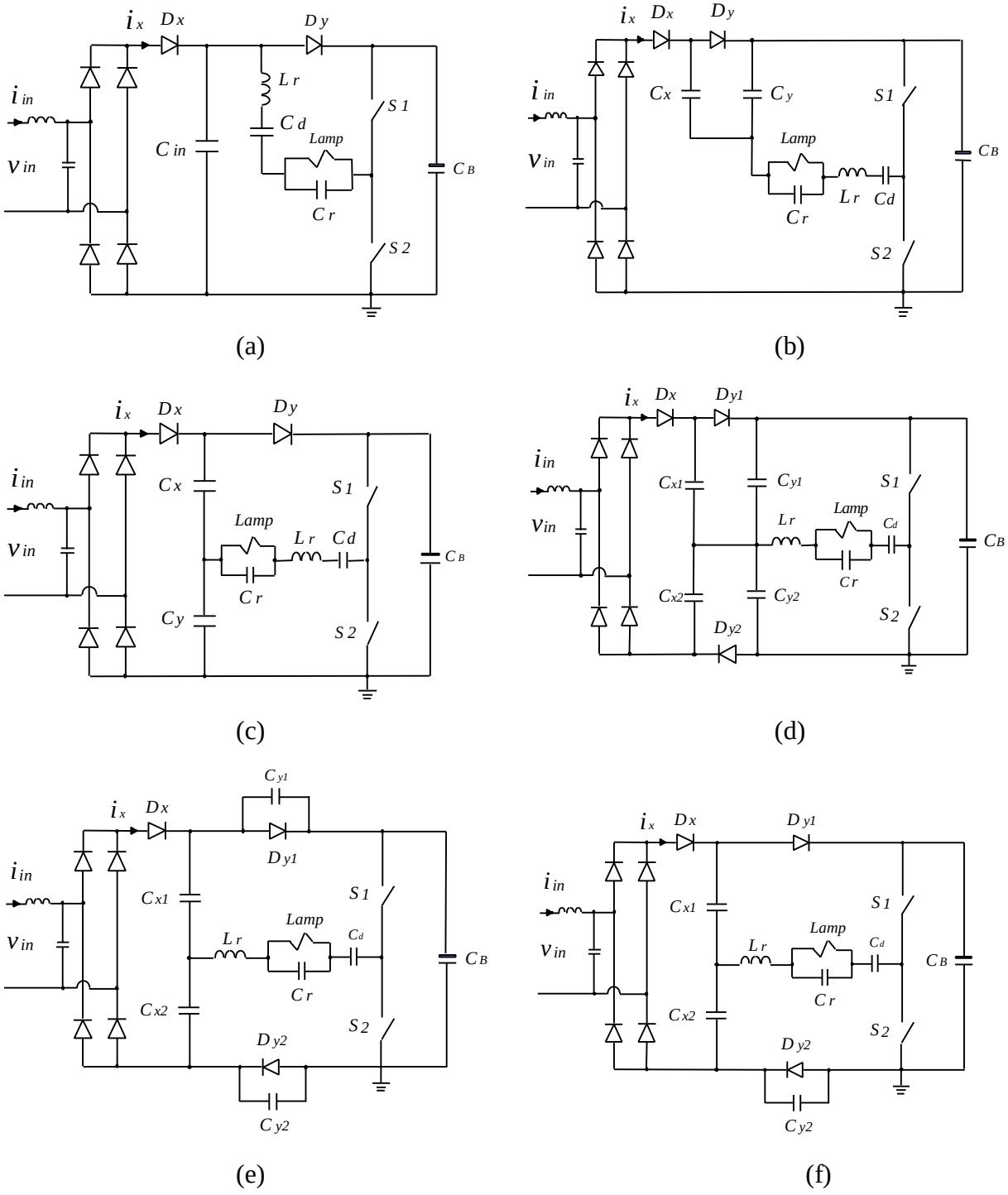
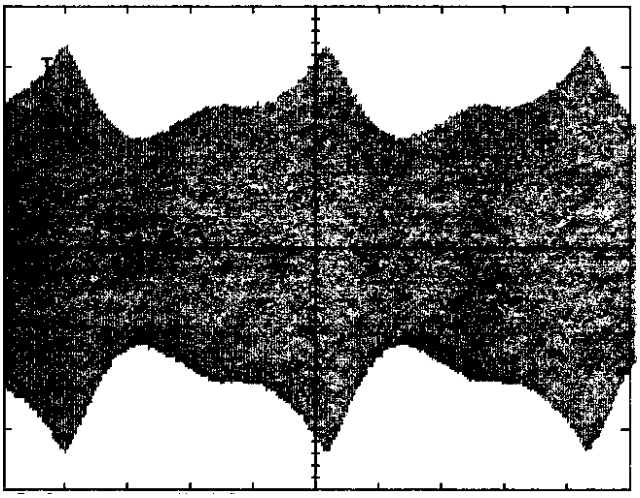


Fig. 4.6 A family of CS-CPPFC electronic ballasts

Fig. 4.3, over one switching cycle, and each resonant mode time interval is related to the line input voltage. Thus, the lamp current has of twice the line frequency ripple which deteriorates the crest factor. This high crest factor may shorten the lamp life. In order to reduce the low frequency lamp current ripple and improve the lamp crest factor, the switching frequency modulation scheme is used. Fig. 4.7 shows that the lamp has high current near the zero crossing of the line voltage and small lamp current near the line peak voltage. The controller should operate in such a way that the switching frequency is high near the zero crossing of the line input voltage and the switching frequency is low near the line peak voltage, so that the lamp current waveform has constant amplitude. Figure 4.8(a) shows the average lamp current control with switching frequency modulation to improve the crest factor. This modulation scheme consists of a lamp current sensor, error amplifier, and timing resistor. When the lamp current is high near the zero crossing of the line voltage, the sensed lamp current signal V_i increases. The output of the error amplifier becomes low so that more base current flows through transistor T, and the output resistance of transistor T becomes small, which increases the switching frequency. Therefore, the lamp current does not increase, and it is regulated to a fixed value. The lamp current waveform with switching frequency modulation is shown in Fig. 4.8(b). Its measured



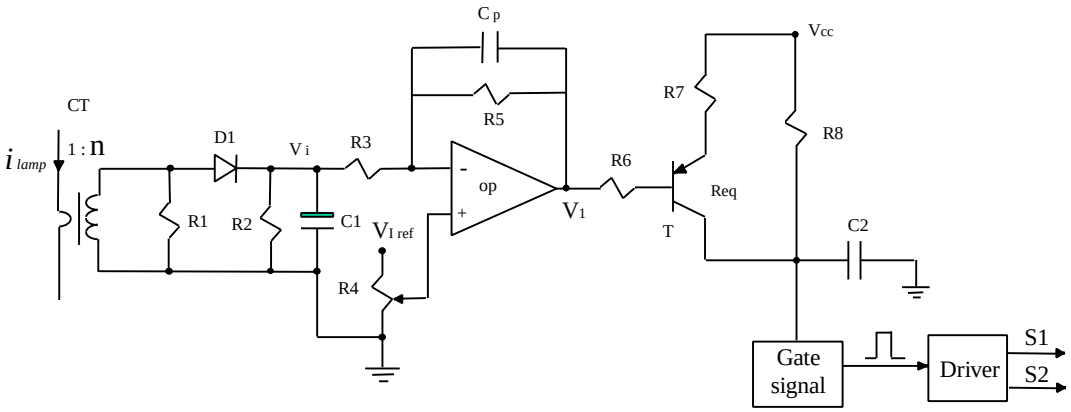
t: 2 ms/div *i_{lamp}: 0.2 A/div*

Fig. 4.7 The lamp current waveform with constant frequency and duty ratio control

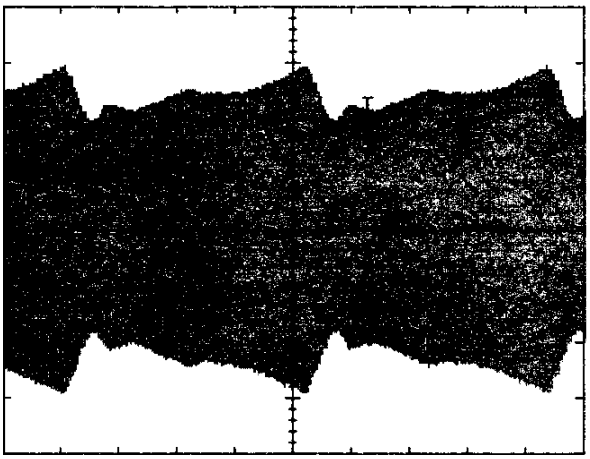
crest factor is 1.54. Of course, a line voltage feed-forward scheme also can be used to improve the crest factor [D6]. However, the developed average lamp current control with switching frequency modulation is able to keep the lamp's power constant even for a certain line voltage variation. Figure 4.9(a) shows the switching current waveform near the zero crossing of the line voltage and near the peak line voltage. It can be seen that the switching frequencies are 59.5 kHz and 56.8 kHz near the zero crossing of the line voltage and line peak voltage, respectively. The maximum switching current is about 2.1A. The measured line input current waveform is shown in Fig. 4.9(b). The measured total harmonic distortion is 11.3%, and each harmonic component satisfies IEC1000-3-2 Class C requirements. Therefore, both high power factor and low crest factor can be simultaneously achieved by using switching frequency modulation. Table 4.1 shows the performance of the developed CPPFC electronic ballasts. The maximum DC bus voltage V_{bmax} in parenthesis stands for the measured maximum voltage by slowly reducing the switching frequency instead of one second preheat and then fast sweeping frequency to ignite the lamp. It is shown that the CS-CPPFC electronic ballast has lower switching current stress and only one inductor is used. The VS-CPPFC electronic ballast with LFSR has lowest DC bus voltage stress, but it suffers from highest current stress.

Table 4.1 Comparison of the CPPFC electronic ballasts

Type	THD	V_{Bmax}	I_s (A)	CF	I_{in}	Inductor	Efficiency	Vin (V)
VS-CPPFC	12%	800	2.4	2.6	DCM	1		
VS-CPPFC with LFSR	5.0%	310 (410)	3.4	1.50	DCM	2	82.0 %	180-220 V
CS-CPPFC	11.0%	(470)	2.2	1.54	DCM	1	82.5 %	180-220V



(a)

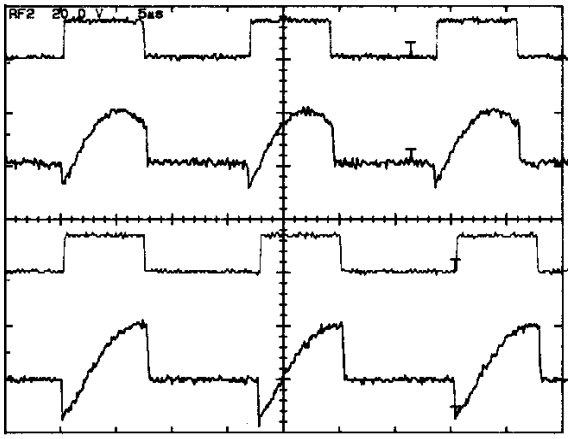


t: 2 ms/div, i_{lamp}*: 0.2 A/div*

(b)

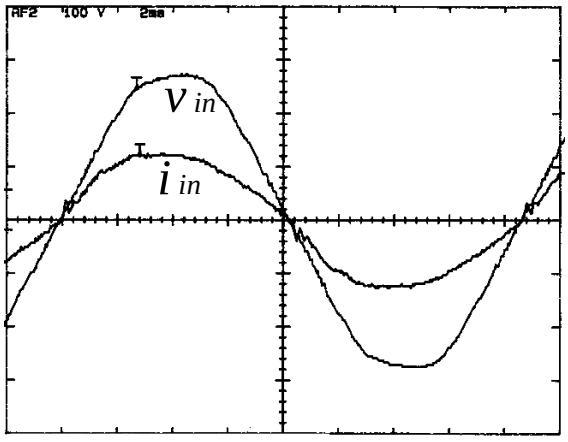
Fig. 4.8 (a) Average lamp current control with switching frequency modulation

(b) Measured lamp current with switching frequency modulation



t: 5 μs/div

(a)



t: 2 ms/div v_{in}*: 100 V/div* i_{in}*: 0.5 A/div*

(b)

Fig. 4.9 (a) Top two waveforms: Near the zero crossing of the line voltage
Bottom two waveforms: Near the line peak voltage
(b) Measured line input current and voltage waveforms

4.5 Summary

The CS-CPPFC technique is actually similar to the VS-CPPFC technique because they are equivalent. Simply the VS-CPPFC converter is the Thevinin version and the CS-CPPFC converter is a Norton version. This chapter developed the current source charge pump power factor correction (CS-CPPFC) technique and derived the generalized CS-CPPFC converter. The conditions for achieving unity power factor were analyzed and derived, and the principles of the CS-CPPFC electronic ballast was also provided. This chapter also presented a family of CS-CPPFC electronic ballasts. The experimental results verify the theoretical analysis and circuit operation.

The main advantages for the CS-CPPFC electronic ballast are:

1. The power switches deal only with the reflected load current, which is the resonant inductor current. This switching current stress is much smaller than that of a VS-CPPFC electronic ballast with second resonance, where the power switches have to take almost twice the resonant inductor current. Thus, small current rating devices can be used.
2. By properly using the modulation scheme, low THD, high power factor and low lamp crest factor can be simultaneously achieved.
3. Only one inductor is used for the CS-CPPFC electronic ballast while the VS-CPPFC electronic ballast with second resonance has to use two resonant inductors. The integrated single-stage PFC electronic ballast also uses two inductors. One is the DCM boost inductor and the other is the resonant inductor. Therefore, the inductive components are minimized.
4. The developed CS-CPPFC converter has a potentially low cost, which is very attractive.
5. The main disadvantage is that the DC bus voltage stress is a little high, about 470V at start-up mode with 200V line input voltage. The VS-CPPFC electronic ballast with second resonance has low DC bus voltage stress, about 410V at start-up mode. So, the CS-CPPFC electronic ballast is suitable for instant start-up application.

CHAPTER 5

VOLTAGE SOURCE CURRENT SOURCE CHARGE PUMP POWER FACTOR CORRECTION (VSCS-CPPFC) CONVERTER

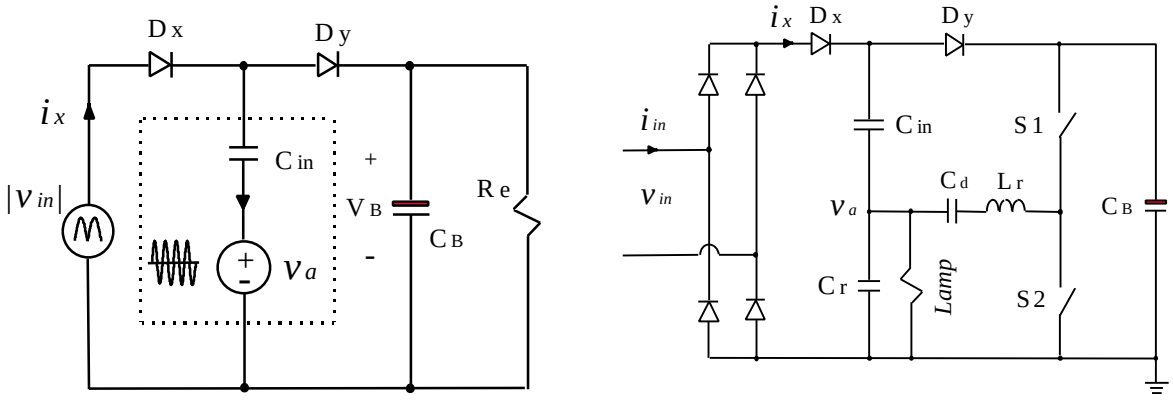
5.1 Introduction

VS-CPPFC and CS-CPPFC techniques were developed in Chapters 3 and 4, respectively. VS-CPPFC and CS-CPPFC electronic ballasts were proposed, analyzed, and developed, as examples. It was shown that crest factor is high for the basic VS-CPPFC and CS-CPPFC electronic ballasts without feedback control. This chapter develops the voltage source current source charge pump power factor correction (VSCS-CPPFC) technique, which actually integrates voltage source charge pump power factor correction with the current source charge pump power factor correction technique is developed. The conduction angle of the line rectifier becomes bigger for the VSCS-CPPFC converter. As a result, the circulating current in the resonant tank can be reduced, compared with the basic VS-CPPFC and CS-CPPFC converters. One electronic ballast using the developed VSCS-CPPFC technique is analyzed and implemented. It will be shown that low crest factor and good power factor can be simultaneously obtained without feedback control.

5.2 Circuit derivation

The VS-CPPFC converter was derived and analyzed in Chapter 3, as shown in Fig. 5.1(a). The voltage source v_a charges and discharges the capacitor C_{in} to absorb energy from the ac line and pump its stored energy to the bulk capacitor C_B. Figure 5.1(b) shows the basic VS-CPPFC electronic ballast, where the lamp voltage is considered a high frequency voltage source with a constant amplitude. One disadvantage of the circuit in Fig. 5.1(b) is its high lamp crest factor. This high crest factor is mainly due to the charge capacitor C_{in} modulated with the resonant tank. It can be seen that C_{in} is in parallel with the resonant capacitor C_r when either D_x or D_y is on. As a result, the equivalent resonant capacitor is a function of the line voltage. The higher the line

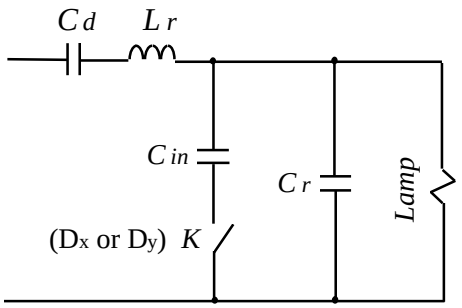
voltage, the larger the equivalent resonant capacitance. The equivalent resonant tank is shown in Fig. 5.2(a). Since C_{in} is much bigger than C_r, the equivalent resonant capacitor is $C_{in} + C_r$ near the line peak voltage and C_r near the zero crossing of the line voltage. Therefore, the equivalent resonant capacitor significantly changes over one line cycle, which deteriorates the lamp crest factor. To improve the crest factor, the possible way is to minimize C_{in} effect. Figure 5.3(a) shows the proposed equivalent resonant tank to minimize the C_{in} effect, where C_y is in parallel with K. Before K is turned on, C_y has to be discharged. The conduction angle of K is reduced so as to minimize C_{in}'s effect. Besides, C_y is in series with C_{in}, and the equivalent capacitance of C_y and C_{in} is less than either C_y or C_{in}. Thus, the effect of C_{in} is much less than in the circuit of Fig. 5.1(b). The VS-CPPFC electronic ballast with improved crest factor is shown in Fig. 5.3(b).



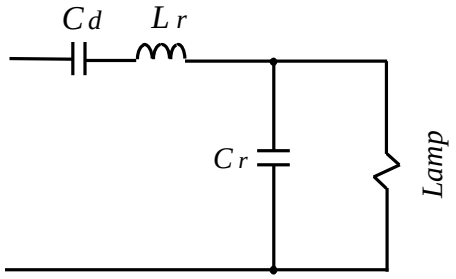
(a) (b)

Fig. 5.1 (a) The VS-CPPFC converter

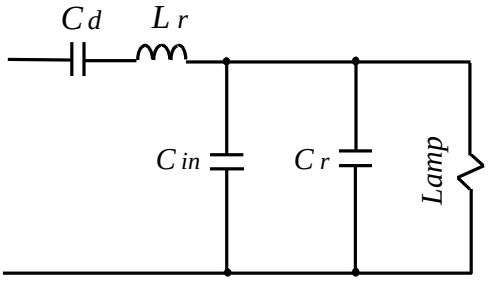
(b) The basic VS-CPPFC electronic ballast



(a)



(b)

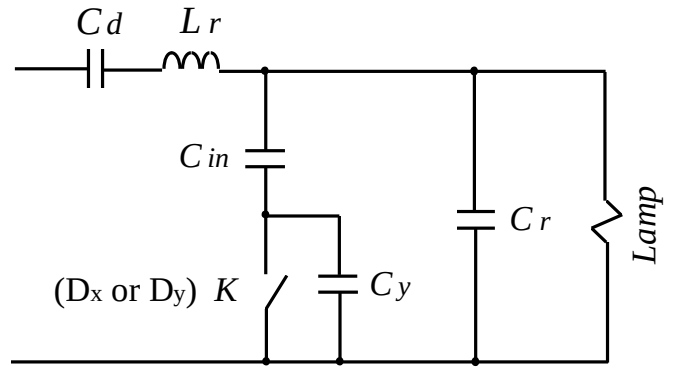


(c)

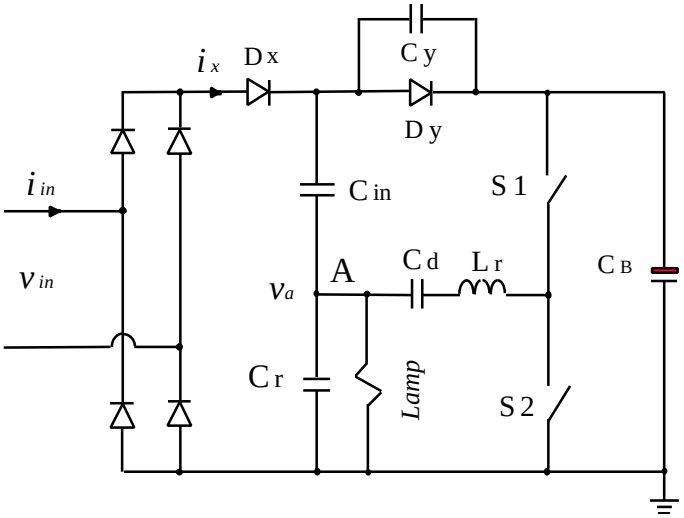
Fig. 5.2 (a) Equivalent resonant tank of Fig. 5.1(b) (K on when D_x or D_y is on)

(b) The equivalent resonant tank near the zero crossing of the line voltage

(c) The equivalent resonant tank near the line peak voltage



(a)

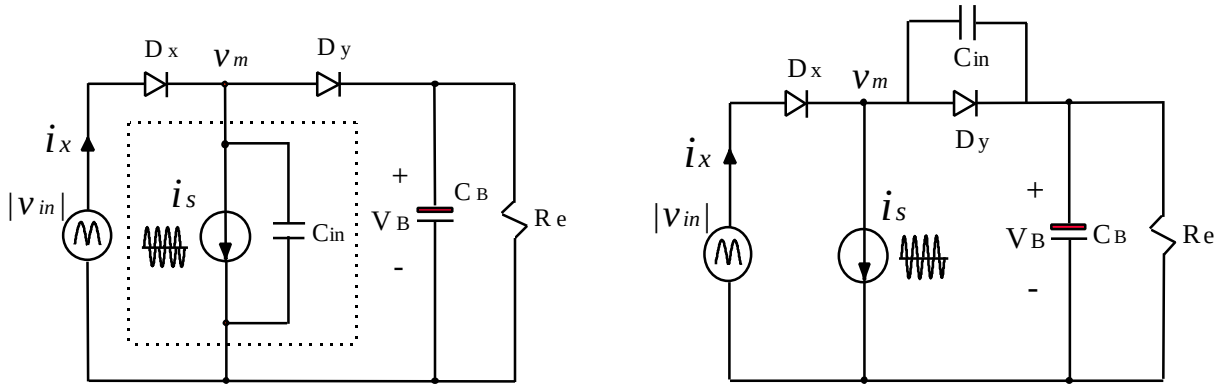


(b)

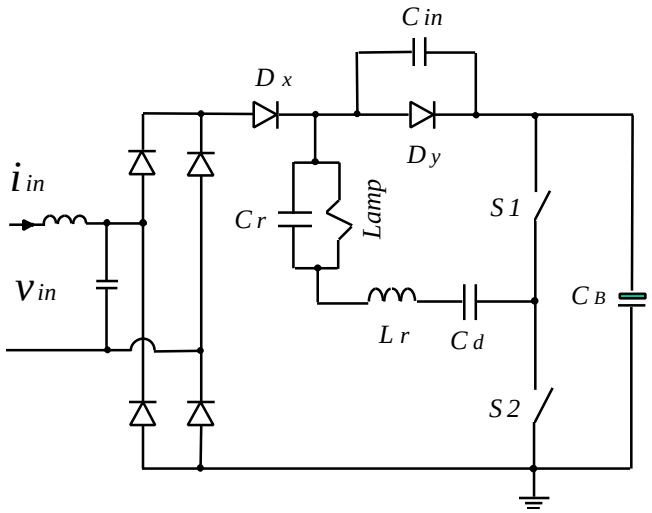
Fig. 5.3 (a) Equivalent resonant tank with improved crest factor

(b) The VS-CPPFC electronic ballast with improved crest factor

The voltage source v_a in series with a capacitor can be represented as a high frequency current source i_s in parallel with a capacitor C_{in} as a Norton form, as shown in Fig. 5.4(a). The charge pump capacitor C_{in} can be shifted to parallel with D_y, based on the capacitor shift rule, as shown in Fig. 5.4(a). Because the series resonant parallel-loaded tank can be considered a high frequency current source if the output voltage is constant, the basic current source charge pump power factor correction (CS-CPPFC) electronic ballast is shown in Fig. 5.4(b).



(a)



(b)

Fig. 5.4 (a) The basic CS-CPPFC converter

(b) CS-CPPFC electronic ballast

If we integrate the VS-CPPFC electronic ballast with improved crest factor of Fig. 5.3(b) with the CS-CPPFC electronic ballast of Fig. 5.4(c), the derived voltage source current source charge pump power factor correction (VSCS-CPPFC) electronic ballast is the circuit shown in Fig. 5.5(c). The VS-CPPFC circuit is composed of charge capacitors C_{in} and C_{y1}, resonant inductor L_r, resonant capacitor C_r, and the lamp, while the CS-CPPFC circuit consists of charge capacitor C_{y2}, resonant inductor L_r, resonant capacitor C_r, and the lamp. It can be seen that both the VS-CPPFC and CS-CPPFC circuits share the same resonant tank of L_r and C_r. There is a phase difference between the voltage source v_a and current source i_s. Here the lamp voltage and resonant inductor current are considered high frequency voltage source and current source, respectively, if the lamp voltage is constant. So combining the VS-CPPFC electronic ballast and CS-CPPFC electronic ballast reduces the circulating current, the current stress in the switching devices, and the resonant inductor current, because the conduction angle of the line rectifier can be extended during which time the input current is drawn by the difference of each phase. In the next section, the steady state and unity power factor condition will be analyzed.

5.3 Steady State Analysis and Unity Power Factor Condition

To further explain the VSCS-CPPFC electronic ballast, it is necessary to analyze the steady-state performance and its unity power factor condition so that it can be optimally designed. In the following steady state analysis, the following assumptions are made:

1. The lamp voltage and resonant inductor current are considered a high frequency voltage source and a high frequency current source, respectively.
2. The bulk capacitor C_B is large enough so that its voltage V_B can be considered a constant voltage source.

The rectified line voltage is assumed a constant over one switching cycle since the switching frequency f_s is much higher than the line frequency.

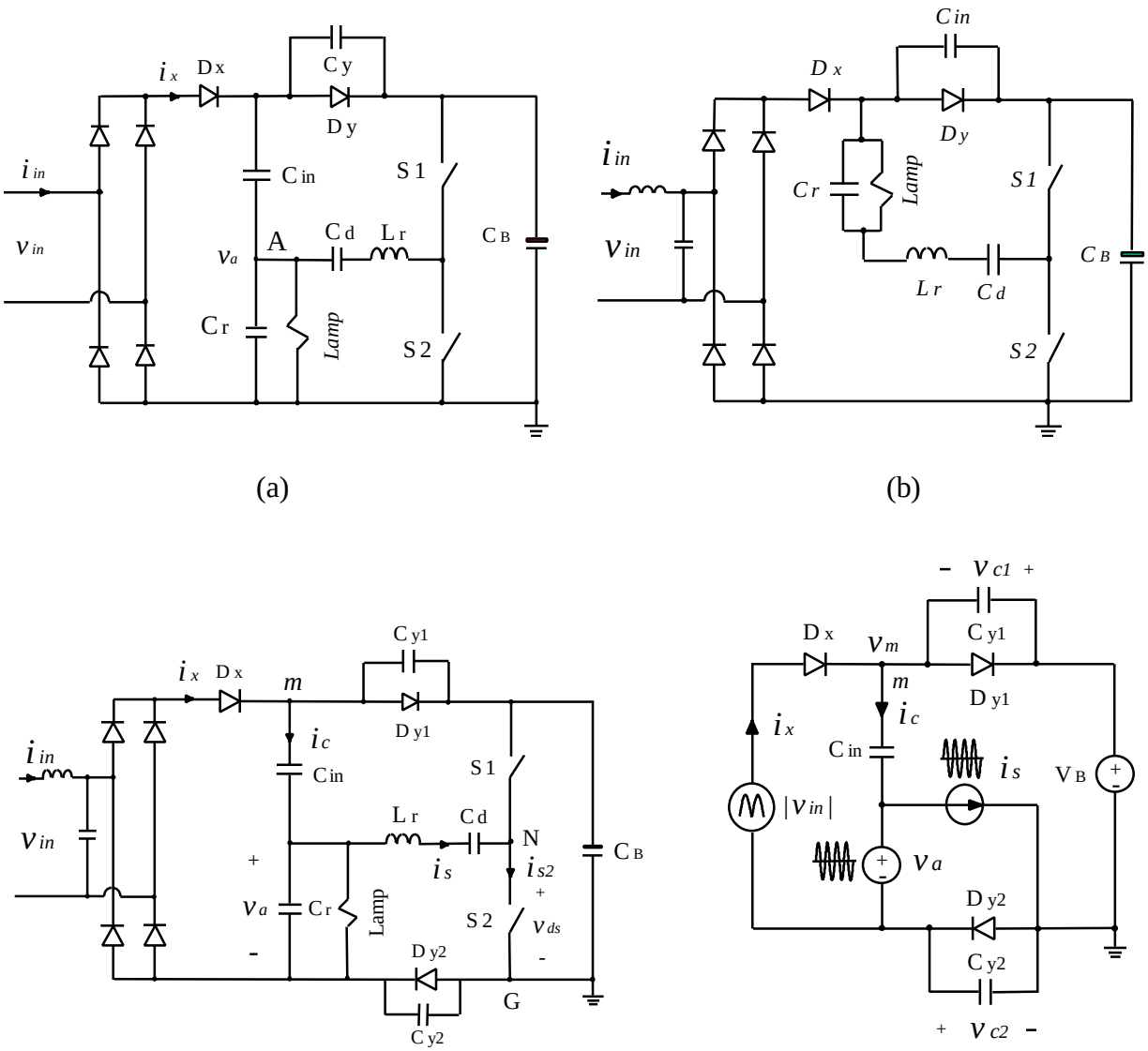


Fig. 5.5 (a) VS-CPPFC electronic ballast

(b) CS-CPPFC electronic ballast

(c) The proposed VSCS-CPPFC electronic ballast

(d) Equivalent circuit of Fig. 5.5(c)

The simplified equivalent circuit of Fig. 5.5(c) is shown in Fig. 5.5(d). Four topological stages, shown in Fig. 5.6, exist in one switching cycle. The switching waveforms are shown in Fig. 5.7.

M1 [t_0 - t_1]: Before t_0, both D_x and D_{y1} are conducting, while D_{y2} is off. After t_0, v_a decreases in a sine waveform, and v_m also decreases in the same form since the voltage across C_{in} cannot change abruptly. v_m becomes lower than the DC bus voltage, and D_{y1} becomes reverse biased. The equivalent circuit is shown in Fig. 5.6(a). During this time interval, C_{y1} is charged while C_{y2} is discharged. Assume the high frequency current $i_s = I_s \sin w_s t$, and the high frequency voltage $v_a = V_a \sin(w_s t + 90^0)$. The two charge capacitor currents i_{cy1} and i_{cy2} and rectified line current i_x are given by

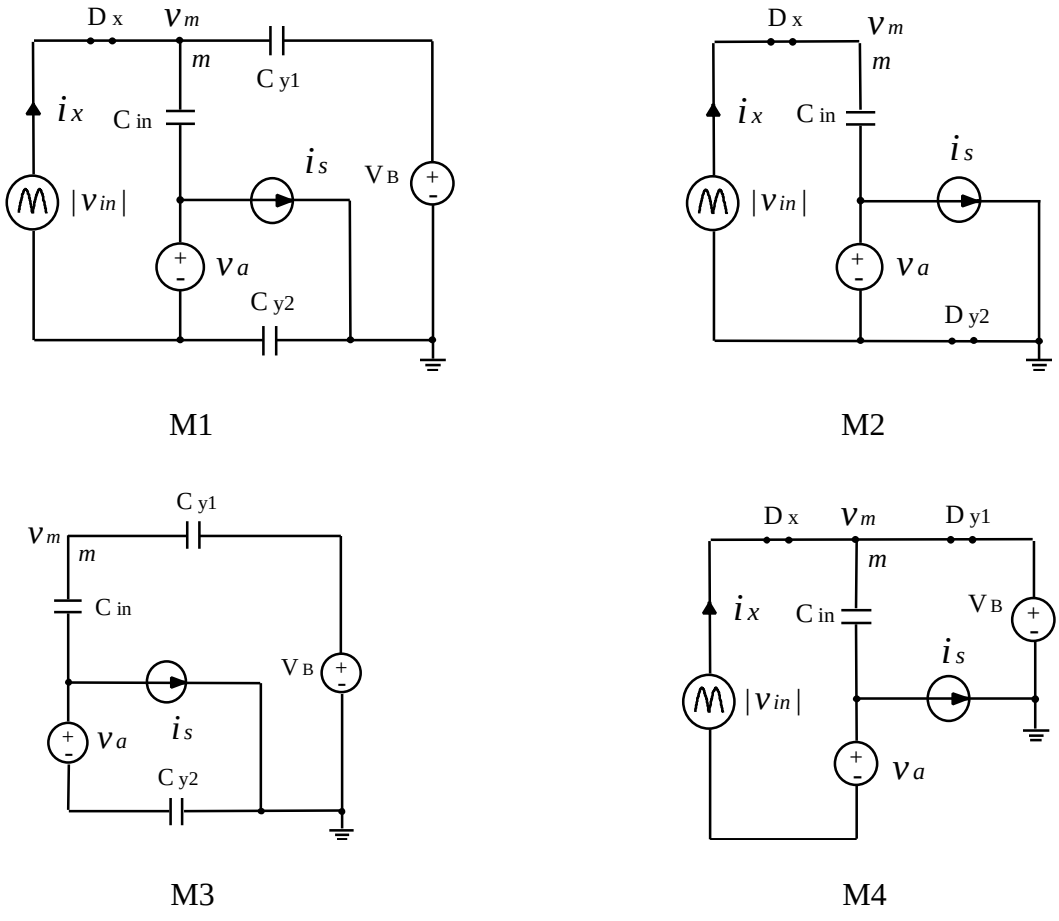


Fig. 5.6 Four topological stages

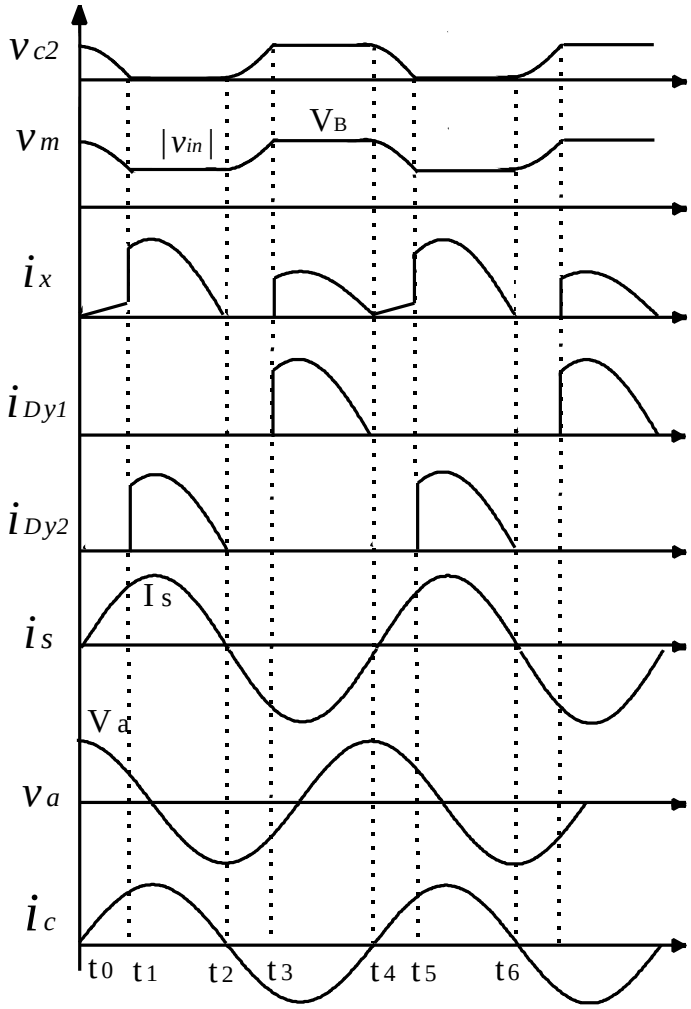


Fig. 5.7 The key switching waveforms

$$i_{cy1} = \frac{C_{y1} I_s}{C_{y1} + C_{y2}} sinw_s t\,, \tag{5.1}$$

$$i_{cy2} = -\frac{C_{cy2} I_s}{C_{y1} + C_{y2}} sinw_s t\,, \tag{5.2}$$

$$i_x = \left(2p\ f_s\ C_{in}\ V_a - \frac{C_{y1} I_s}{C_{y1} + C_{y2}} \right) sinw_s t \quad t_0 < t < t_1\,. \tag{5.3}$$

C_{y2} is totally discharged and v_m decreases to the rectified line voltage at t_1, where D_{y2} begins to conduct.

M2 [t_1, t_2]: At t_1, D_{y2} is on, and the equivalent circuit is shown in Fig. 5.6(b). During this time period, v_a continuously decreases and C_{in} is being charged to absorb energy through the line input and D_x. This rectified line current can be determined by

$$i_x = 2\ p\ f_s\ C_{in} V_a\ sinw_s t \qquad t_1 < t < t_2 . \tag{5.4}$$

At t_2, i_s becomes zero and D_{y2} is naturally turned off, while v_a reaches its minimum value and D_x is also naturally turned off.

M3 [t_2, t_3]: During this time interval, v_a continuously increases and i_s becomes negative, which discharges C_{in} and C_{y1} and charges C_{y2}. As a result, C_{y1} is totally discharged and the voltage v_m-v_{c2} is equal to the rectified line voltage at t_3, where D_x starts to conduct. The equivalent circuit is shown in Fig. 5.6(c). C_{y1} is being discharged while C_{y2} is being charged. The charging and discharging current for these capacitors can be determined by

$$i_{cy1} = \frac{C_{y1}}{C_{y1} + C_{y2} + \dfrac{C_{y1} C_{y2}}{C_{in}}} \left(I_s + w_s C_{y2} V_a \right) sinw_s t , \tag{5.5}$$

$$i_{cy2} = \frac{w_s C_{y2} V_a - \left(\dfrac{C_{y2}}{C_{y1}} + \dfrac{C_{y2}}{C_{in}} \right) I_s}{1 + \dfrac{C_{y2}}{C_{y1}} + \dfrac{C_{y2}}{C_{in}}}\ sinw_s\ t \qquad t_2 < t < t_3 . \tag{5.6}$$

There is no line input current in this time interval.

M4 [t_3, t_4]: Both D_x and D_{y1} are on, and D_{y2} is off. D_x conducts the current difference of i_x and i_c. During this time period, the energy stored in C_{in} is pumped to the DC bus, while the high frequency voltage source v_a also absorbs energy from the ac line. The rectified input line current is given by

$$i_x = \left(2p\ f_s\ C_{in}\ V_a - I_s \right) sinw_s\ t \qquad t_3 < t < t_4 . \tag{5.7}$$

This mode ends at t_4, where i_s becomes positive and v_a reaches its maximum value. The average rectified input line current is

$$\left| i_{in} \right| = i_x^{ave} = \frac{1}{T_s} \int_{t_0}^{t_4} i_x \, dt \, . \tag{5.8}$$

Substituting (5.3), (5.4), and (5.7) into (5.8) gives

$$\left| i_{in} \right| = \frac{I_s}{p} - \left(C_{y1} + C_{y2} \right) f_s \, V_B + f_s \left(C_{y1} + C_{y2} \right) \left| v_{in} \right| . \tag{5.9}$$

In order to achieve unity power factor, it is required that the average input current follow the line input voltage. From (5.9), the first two terms have to be zero. That is

$$I_s = p \, f_s \left(C_{y1} + C_{y2} \right) V_B \, . \tag{5.10}$$

Thus, (3.9) becomes

$$\left| i_{in} \right| = f_s \left(C_{y1} + C_{y2} \right) \left| v_{in} \right| . \tag{5.11}$$

Equation (5.11) shows that the average line input current is proportional to the line input voltage so that unity power factor can be obtained.

To obtain unity power factor, it is required that the resonant inductor peak current has to satisfy Eq. (5.10). The resonant inductor is related to the resonant tank parameters. C_{in} is the part of the resonant capacitor when either D_x or D_{y1} is turned on. Usually, the larger the capacitor C_{in}, the bigger the resonant inductor current. Thus, according to (5.9), the input power also increases with larger resonant inductor current.

5.4 Design Considerations

The design objective is to find the charge capacitor values C_{y1}, C_{y2}, and C_{in} and the resonant components L_r and C_r. To optimally design this VSCS-CPPFC electronic ballast, the following should be taken into account.

- Minimum DC bus voltage, $V_B = | v_{in} |_{max}$
- Satisfying unity power factor condition

$$I_s = p \;\; f_s \left(C_{y1} + C_{y2} \right) V_B \, . \tag{5.12}$$

5.4.1 Selection of Charge Pump Capacitors C_{y1} and C_{y2}

The instant input power is the product of the instantaneous input voltage and average rectified input current over one switching cycle, which is given by

$$p_i(t) = \left(\frac{I_s}{p} - \left(C_{y1} + C_{y2}\right) f_s \, V_B \right) \left| v_{in}(t) \right| + \left(C_{y1} + C_{y2}\right) f_s \left| v_{in}(t) \right|^2 . \tag{5.13}$$

By averaging the above equation in a line cycle, the average input power P_i is

$$P_i = \frac{2\,V_{in}}{p} \left(\frac{I_s}{p} - \left(C_{y1} + C_{y2}\right) f_s \, V_B \right) + \frac{1}{2}\left(C_{y1} + C_{y2}\right) f_s \, V_{in}^2 , \tag{5.14}$$

where V_{in} is the line peak voltage. Under the unity power factor condition operation, the first term of (5.14) is zero, and (5.14) can be expressed as

$$P_i = \frac{1}{2} \left(C_{y1} + C_{y2}\right) f_s \, V_{in}^2 . \tag{5.15}$$

Based on the power balance between the input and the output,

$$P_0 = h \, P_i , \tag{5.16}$$

where P_0 and h are the output power and the conversion efficiency, respectively. The charge capacitors can be determined by

$$C_{y1} + C_{y2} = \frac{2\,P_0}{h \, f_s \, V_{in}^2} . \tag{5.17}$$

For a given peak line voltage V_{in}, switching frequency f_s and lamp power, the charge capacitors can be calculated from (5.17).

5.4.2 Selection of Resonant Components L_r, C_r and C_{in}

Since D_x conducts throughout almost the whole switching cycle except Mode 3, from a high frequency sense, C_{in} is in parallel with C_r as long as D_x is on. For simplicity, it is reasonable to consider C_{in} as part of the resonant capacitor, which is parallel with the lamp. The excitation voltage of this resonant tank is approximately a square waveform near the line peak voltage. If only fundamental component is taken into account, the lamp voltage is given by

$$V_{0,rms} = \frac{\sqrt{2}\,V_B}{p} \frac{1}{\sqrt{\left(1-\frac{w_s^2}{w_0^2}\right)^2 + \left(\frac{w_s L_r}{R_L}\right)^2}}. \tag{5.18}$$

The lamp impedance R_L can be assumed to be a pure resistance in the steady state operation, although it has a negative dynamic impedance. R_L is calculated from

$$R_L = \frac{V_{0,rms}^2}{P_0}. \tag{5.19}$$

The resonant frequency ω_0 is

$$w_0 = \frac{1}{\sqrt{L_r\left(C_r + C_{in}\right)}}. \tag{5.20}$$

To achieve zero-voltage switching operation, the switching frequency has to be higher than the resonant frequency. For P_o = 80 watts, $V_{0,rms}$ = 230 V rms, V_B = 280 VDC, f_s = 53 kHz, and $f_0 = 0.9\, f_s$, the resonant components are given by

L_r = 710 μH, $C_r + C_{in}$ = 16 nF.

For further determining C_r and C_{in}, it is necessary to simulate this electronic ballast so that unity power factor and low lamp crest factor can be obtained.

5.5 Experimental Verification

The proposed VSCS-CPPFC electronic ballast was implemented and tested to verify the circuit operation. Based on the above design guidelines and Pspice simulation, the designed parameters are chosen as follows:

C_{in} = 12 nF C_r = 3.9 nF C_{y1} = 8.2 nF C_{y2} = 22 nF L_r = 700 μH

The start-up and steady-state characteristics of the designed electronic ballast were tested and investigated. The main results are described in the following.

5.5.1 Preheat and Start-up Characteristics

Normally the electronic ballast operation consists of three parts: preheat, start-up, and steady-state operations. The preheat and start-up operations correspond to the light load,

because the lamps are not fully turned on. Because DC bus voltage stress across the bulk capacitor may exist during these operation modes, it is important to investigate the circuit characteristics during the preheat and start-up modes.

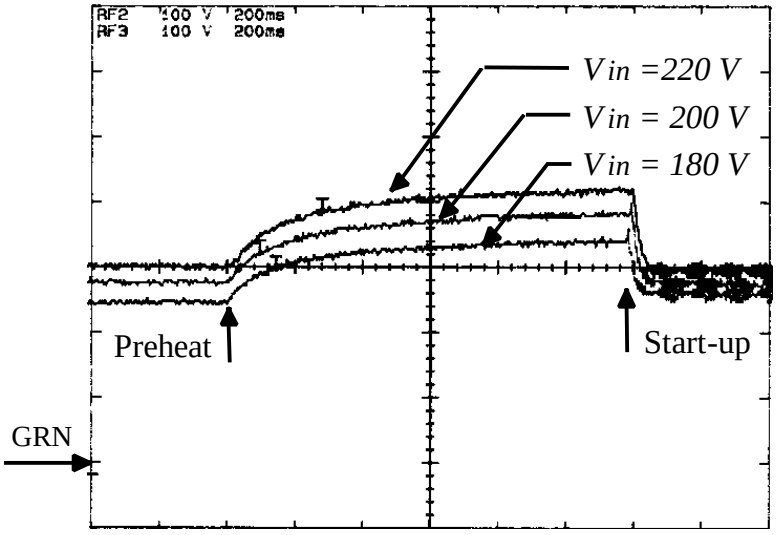
Usually, preheat mode is needed to prolong lamp life, where the lamp is frequently turned on and off. If the lamp filaments are preheated before the lamp is ignited, the lamp ignition voltage will be lower than without preheat. Thus, it is easy to ignite the lamp after lamp preheating. Usually, it takes one second to preheat the filaments at the fixed switching frequency. Then the switching frequency is reduced so that a high lamp voltage is obtained to ignite the lamp. Since these operation modes correspond to the light load of the circuit, the bulk capacitor voltage is one of the most important issues. Figure 5.8 shows the DC bus voltage across the bulk capacitor C_B during the preheat and start-up modes. It can be seen that the highest DC bus voltage occurs at the instant of start-up with high line input voltage. The highest measured DC bus voltages are about 360V, 385V, and 415V for 180V, 200V, and 220V line input voltages, respectively. It is also shown that the DC bus voltage suddenly drops to around the line peak voltage when the lamp is on. Therefore, a 450V bulk capacitor and 500V power MOSFET can be used. However, the DC bus voltage stress will be about 495V for slowly reducing the switching to ignite the lamp.

5.5.2 Steady-State Characteristics

The steady-state characteristics of the electronic ballast include the input characteristics, namely, power factor and total line input current harmonics, and output characteristics, namely, lamp crest factor and lamp power variation over the line input voltage variation. The designed electronic ballast operates at the switching frequency of 53 kHz with 200 V rms line input. Two 40-watt lamps in series were tested. Figure 5.9(a) shows the measured line input current waveform. It is shown that 0.987 power factor and 13% THD can be obtained. The measured line current harmonics are shown in Table 5.1. It can be seen that the developed VSCS-CPPFC electronic ballast can satisfy the IEC1000-3-2 Class C requirement.

Table 5.1 Measured line current harmonic components

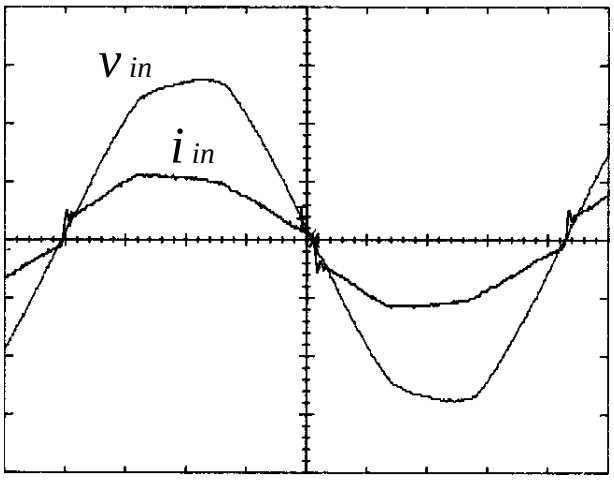
Harmonics	3rd	5th	7th	9th	11th	13th
Class C	29%	10%	7%	5%	3%	3%
Measurement	5.6%	3.6%	1.5%	3.9%	1.2%	2.2%



t: 200 ms/div *V_B: 100 V/div*

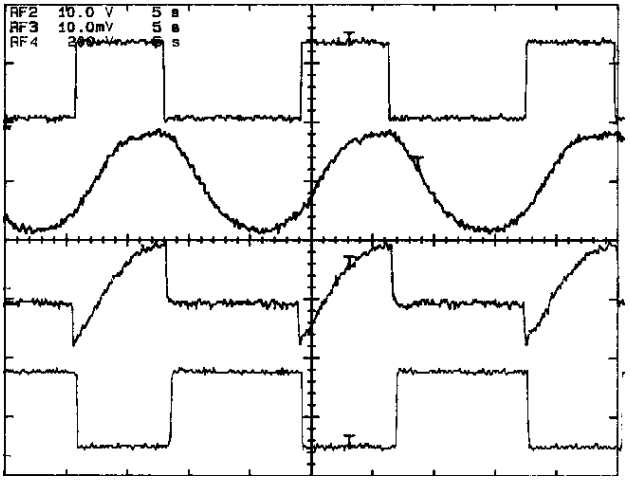
Fig. 5.8 DC bus voltage across C_B during the preheat and start-up modes

The measured switching waveforms are shown in Fig. 5.9(b). It can be seen that the switch takes only 1.9A switching current. This switching current is much smaller than that of the VS-CPPFC electronic ballast with second resonance, so that lower current rating devices can be used. The measured lamp current waveform is shown in Fig. 5.10. The designed electronic ballast was also tested for ±10% line variation. The lamp power was 72W, 82W, and 92W, and the lamp crest factor was 1.66, 1.60, and 1.68 for 180V, 200V, and 220 V line input voltages, respectively. The lamp power variation was less than ±15% for ±10% line voltage variation without any feedback control.



t: 2 ms/div v_{in}: 100 V/div i_{in}: 0.5A/div

(a)

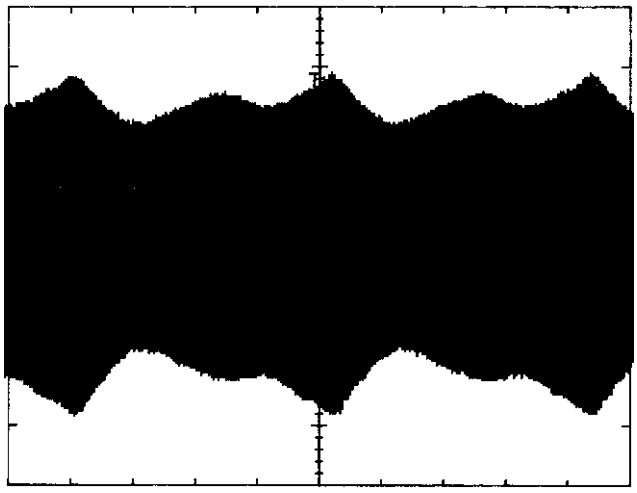


t: 5 ms/div

(b)

Fig. 5.9 (a) Measured line input voltage and current waveforms

(b) Measured switching waveforms



t: 2 ms/div i_{lamp}: 0.2 A/div

Fig. 5.10 Measured lamp current waveform

5.6 Summary

The main merits of the developed VSCS-CPPFC electronic ballast are:

1. By simply adding an additional capacitor in parallel with the diode, the charge pump capacitor effect on the resonant tank is minimized so that the lamp crest factor is significantly improved over ±10% line input voltage variation without using any feedback control.
2. The lamp power variation is automatically limited within ±15% when the line input changes ±10%. This is mainly because the lamp crest factor is improved.
3. The conduction angle of the line rectifier is extended so that the circulating current in the tank can be reduced. As a result, the switching current stress is reduced and the conversion efficiency is improved.

4. DC bus voltage across the bulk capacitor C_B during the preheat and start-up modes is reduced, compared with the basic VS-CPPFC and basic CS-CPPFC electronic ballasts. The maximum DC bus voltage is limited within 415V so that a 450V bulk capacitor can be used.

5. Only one resonant inductor is used, while charge capacitors are used to achieve power factor correction to satisfy the IEC 1000-3-2 Class C harmonics requirements. Therefore, the inductive components are minimized, and the developed VSCS-CPPFC electronic ballast has a potential low cost.

The disadvantage is that the rectified line current is discontinuous so that a relatively large line input filter can be used. This is a common problem for the known PFC converters, such as the DCM PFC, VS-CPPFC, and CS-CPPFC converters.

Table 5.2 shows the main characteristics of the developed VS-CPPFC, VS-CPPFC with second resonance, CS-CPPFC and VSCS-CPPFC electronic ballasts. It can be seen that the developed VSCS-CPPFC electronic ballast has minimum switching current stress with low DC bus voltage. It also uses only one resonant inductor. Thus, the VSCS-CPPFC technique is very attractive.

Table 5.2 The performance of Charge pump power factor correction electronic ballast

Type	THD	V_{Bmax} (V)	I_s (A)	CF	Iin	Inductor	Efficiency	Vin (V)
VS-CPPFC	12%	800	2.4	2.6	DCM	1		
VS-CPPFC with LFSR	5.0%	310 (410)	3.4	1.50	DCM	2	82.0 %	180-220 V
CS-CPPFC	11.0%	(470)	2.2	1.54	DCM	1	82.5 %	180-220 V
VSCS-CPPFC	13.0%	385 (495)	1.9	1.60	DCM	1	81.0 %	180-220 V

CHAPTER 6

CONTINUOUS INPUT CURRENT CHARGE PUMP POWER FACTOR CORRECTION (CIC-CPPFC) CONVERTERS

6.1 Introduction

Both the integrated single-stage power factor correction converters and the previously developed CPPFC converters have discontinuous input current. This requires a relatively large EMI filter. The integrated single-stage PFC converters and the VS-CPPFC converters also suffer from high current stresses in the power switches, because they carry the current not only from the reflected load but also from the PFC stage. Their current stresses are almost twice those found in the two-stage approach. These are undesirable for manufacturers simply because high current rating devices have to be used. The CS-CPPFC electronic ballast suffers from a relatively high voltage stress. The VSCS-CPPFC electronic ballast has low THD and crest factor even without feedback control. It also has low switching current stress and reasonable DC bus voltage stress with 200V line input. But, it is not suitable for wide range line input application because the DC bus voltage will be too high at start-up for 265 V line input. Besides, constant lamp power, low crest factor and THD are all the main issues for a wide range line input application. Therefore, the best electronic ballast should have the following features:

(1). Low THD and high power factor to satisfy IEC 1000-3-2 Class C requirement.

(2). Constant lamp power operation and low crest factor over wide range line input voltage.

(3). Low DC bus voltage across the bulk capacitor C_B at preheat, start-up, dimming and normal operations.

(4). Small switching current stress.

(5). A minimum of inductive components as possible. Only one resonant inductor is preferred or one resonant inductor plus an additional small inductor.

(6). Continuous input line current so that a small line input filter can be used.

Table 6.1 shows that the developed CPPFC electronic ballasts cannot satisfy the above requirements. Therefore, it is attractive to develop a new single-stage power factor correction electronic ballast with the above features, so that the developed electronic ballast has the best possible performance and lowest cost.

Table 6.1 Performance of the CPPFC electronic ballast

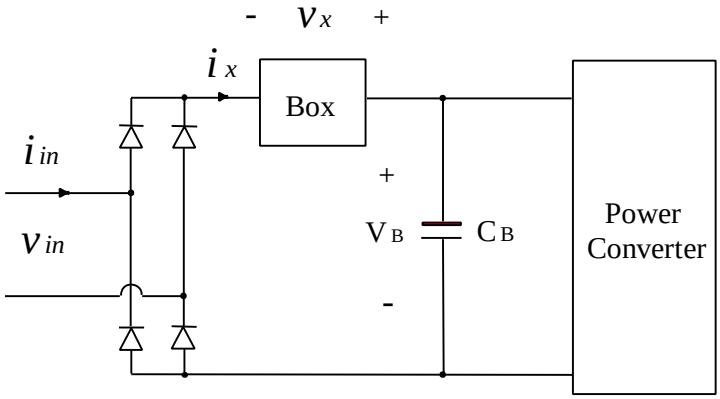
Type	Class C	Constant P_0	CF <1.7	Control	V_B	Is	Wide Vin	CCM I_{in}
VS-CPPFC	Yes	Yes	No	f_s	High	Medium	No	No
VS-CPPFC with LFSR	Yes	Yes	Yes	Duty	Low	High	No	No
CS-CPPFC	Yes	Yes	Yes	f_s	Medium	Medium	No	No
VSCS-CPPFC	Yes	Yes	Yes	No	Medium	Low	No	No

In this Chapter, the continuous input current charge pump power factor correction (CIC - CPPFC) technique is first developed. The power switches only deal with the resonant load current, which is the same as that of the two-stage approach. The developed CIC-CPPFC electronic ballast has low DC bus voltage stress, constant lamp power operation, low crest factor and continuous line input current over a wide range line input voltage. In the next section, the CIC - CPFC converter is derived, and then the principle of operation is analyzed. A family of CIC-CPPFC electronic ballasts are derived. Finally, two CIC-CPPFC electronic ballasts are implemented. The experimental results show that the CIC-CPPFC electronic ballast is very attractive.

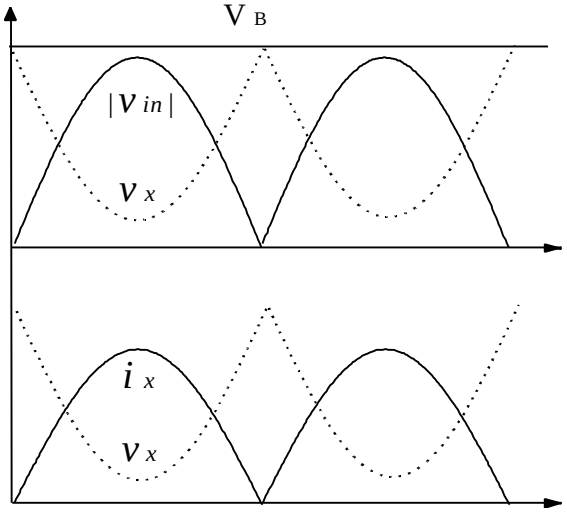
6.2 Circuit Derivation

Figure 6.1 shows the power factor correction converter block diagram. Usually, the DC bus voltage V_B is designed to be higher than the line peak voltage. The box stands for a power converter, and the output voltage of the box is equal to DC bus voltage minus the rectified line voltage. In order to achieve high power factor, the rectified line current i_x should be rectified

sinusoidal waveform. Therefore, the required output characteristics of the box are as shown in Fig. 6.1(b). To achieve high power factor, the box features a high output voltage near the zero crossing of the line voltage, which corresponds to the light load for the box, and low output voltage near the peak line voltage, which corresponds to the heavy load for the box. The question is what kind of converter has these particular output characteristics so that high power factor can be obtained. After examining many topologies, it was found that a resonant converter has these kinds of output characteristics of v_x and i_x. Figure 6.2(a) shows the power factor correction converter [B25], where the box was replaced by a LCC type resonant converter. Based on the voltage gain characteristics of the LCC type resonant converter, shown in Fig. 6.2(b), it is seen that it will provide high output voltage at light load near the zero crossing of the line input voltage, and have low output voltage at heavy load near the line peak voltage. These output characteristics roughly match the required curves of Fig. 6.1(b). Therefore, Figure 6.2(a) has an inherent power factor correction function. If the resonant inductor L_s and capacitor C_s are split into two series inductors and capacitors, and C_{in} is shifted to the output rectifier, then the isolated transformer can be eliminated, which is shown in Fig. 6.3(a). This circuit is good for high power applications due to the full bridge configuration. However, a half-bridge converter is preferred for low power applications. Therefore, one switch leg (S_3 and S_4) associated with its resonant tank and a pair of output diodes can be saved. The simplified power factor correction converter is shown in Fig. 6.3(b). The series resonant tank, composed of L_s and C_s, can be considered a high frequency current source. The generalized circuit of Fig. 6.3(b) is shown in Fig. 6.4(a). The input current can be continuous due to the inductor L_x. This converter can be called basic CIC-CPPFC converter. It can be seen that the CIC-CPPFC converter can be developed by simply adding an inductor to the basic CS-CPPFC converter. In the next section, unity power factor condition will be analyzed to further explain the power factor correction function.



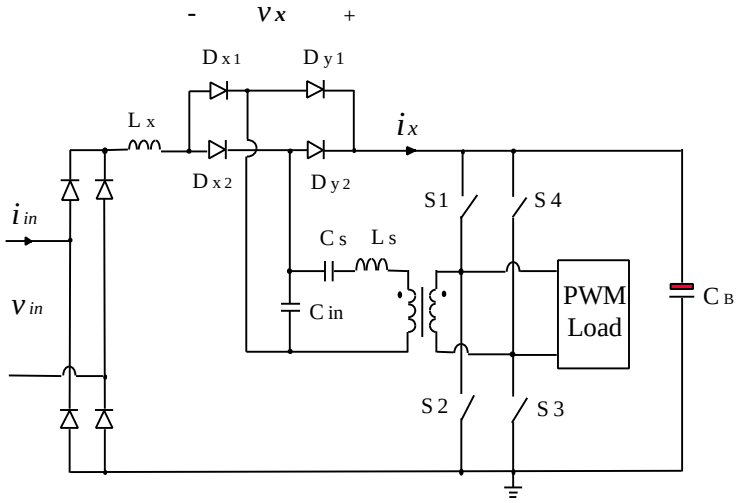
(a)



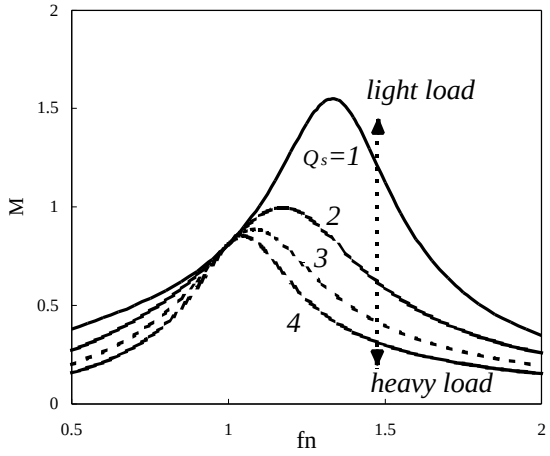
(b)

Fig. 6.1 (a) The power factor correction converter block diagram

(b) The required output characteristics to achieve the power factor correction



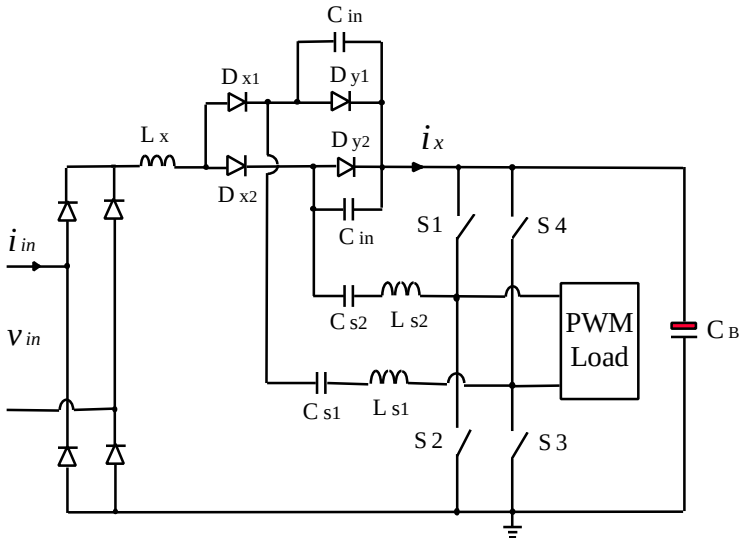
(a)



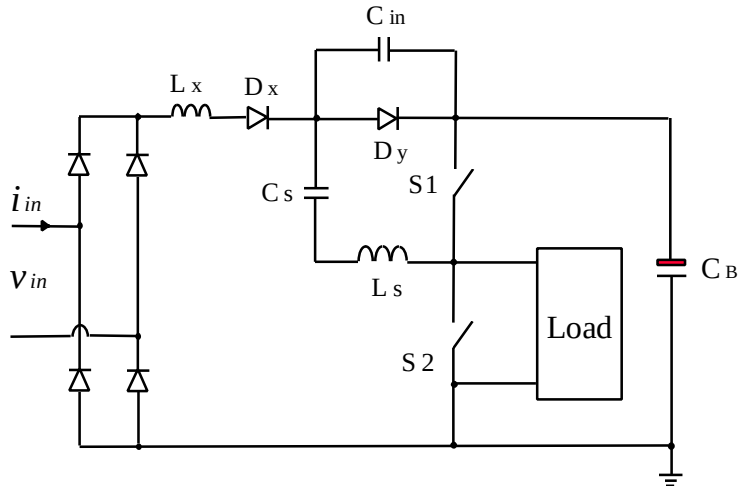
(b)

Fig. 6.2 (a) LCC type power factor correction converter

(b) Output characteristics of LCC type resonant converter



(a)



(b)

Fig. 6.3 (a) Power factor correction AC/DC converter

(b) Simplified continuous input current CPPFC converter

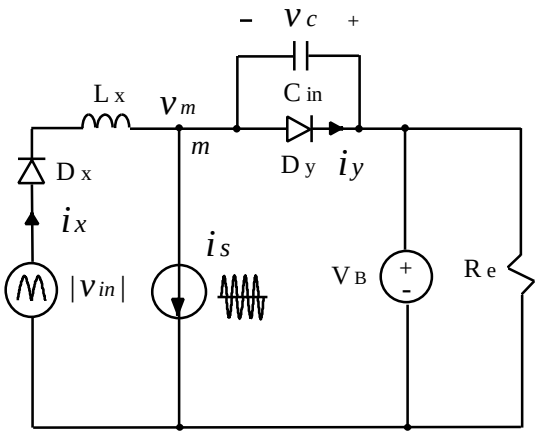
6.3 Unity Power Factor Condition

It is necessary to derive the unity power factor condition so that the converter can be optimally designed to minimize the line input current harmonics. In the steady state analysis, three assumptions are made:

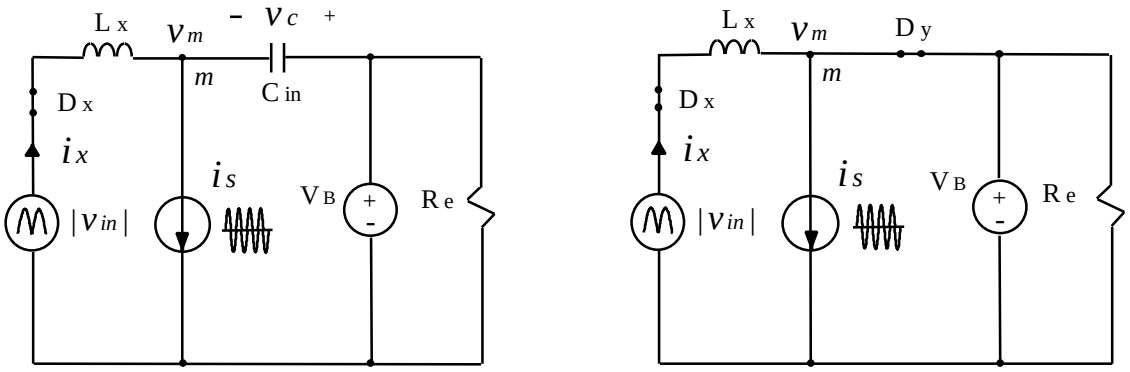
- The DC bulk capacitor C_B is sufficiently large, and its voltage is assumed as a constant.

- Due to the input inductor L_x, the input line current is continuous.
- The switching frequency is much higher than the line frequency so that the rectified line voltage can be assumed to be constant over one switching cycle.

In steady state, two topological stages exist in a switching cycle as shown in Fig. 6.4(b). The switching waveforms are shown in Fig. 6.5.



(a)



M1 M2

(b)

Fig. 6.4 (a) The generalized CIC-CPPFC converter

(b) Two topological stages of Fig. 6.4(a)

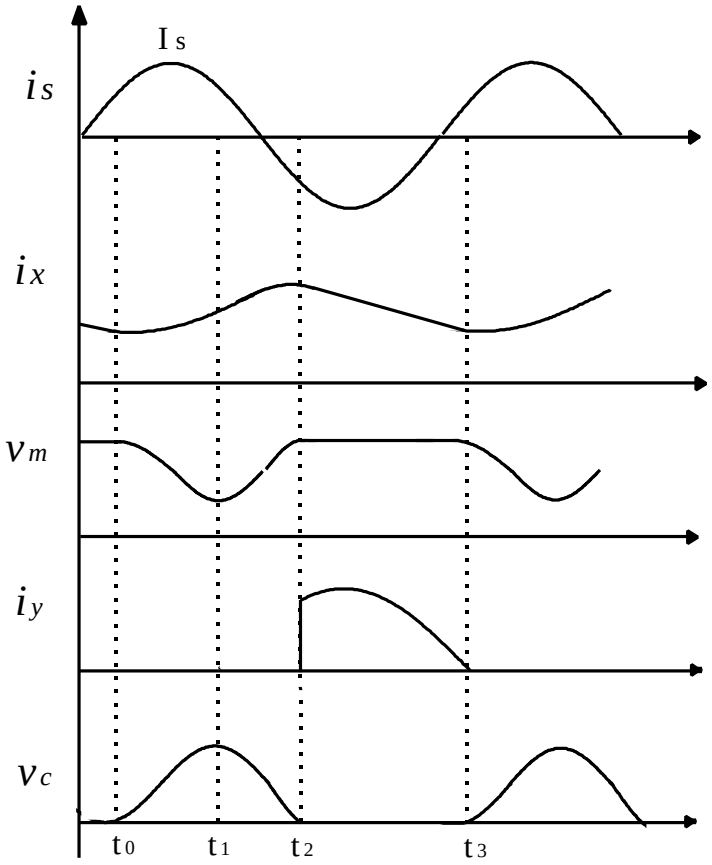


Fig. 6.5 Key switching waveforms of Fig. 6.4(a)

M1, [t_0, t_2]: Before t_0, the rectified line input current is higher than the source current value i_s. D_y was conducting the current difference between i_x and i_s. At t_0, i_x equals i_s, and D_y is naturally turned off with zero voltage, since C_{in} is in parallel with D_y. After t_0, the current difference of i_x and i_s charges C_{in} and voltage v_c increases. v_m decreases, which causes the input line current i_x to increase. The capacitor voltage v_c reaches its maximum value when i_x is equal to i_s at t_1. After t_1, i_x is higher than i_s, and this difference current discharges C_{in}. C_{in} is totally discharged at t_2, where D_y begins to conduct, and this mode ends. Based on the charge balance,

$$C_{in} V_{cmax} = \int_{t_0}^{t_1} (i_s - i_x)\, dt = \int_{t_1}^{t_2} (i_x - i_s)\, dt \ . \tag{6.1}$$

According to KVL and KCL,

$$L_x \frac{d\, i_x}{d\, t} = \left| v_{in} \right| - V_B + v_c , \tag{6.2}$$

$$C_{in} \frac{d\, v_c}{d\, t} = i_s - i_x , \tag{6.3}$$

$$i_s = I_s \sin\left[w_s \left(t - t_0 \right) + q \right]. \tag{6.4}$$

The initial conditions are:

$$i_x (t_0) = I_s \sin q , \qquad v_c(t_0) = 0, \qquad w t_0 = q .$$

After solving the above differential equations, we have

$$i_x = \frac{\left| v_{in} \right| - V_B}{Z_0} \sin w_0 t + I_s \sin q \cos w_0 t + K \qquad t_0 < t < t_2, \tag{6.5}$$

where $w_0 = \frac{1}{\sqrt{L_x C_{in}}}$, $Z_0 = \sqrt{\frac{L_x}{C_{in}}}$ and

$$K = \frac{I_s}{\frac{w_s^2}{w_0^2} - 1} \left(\sin q \cos w_0 t + \frac{w_s}{w_0} \cos q \sin w_s t - \sin\left(w_s t + q \right) \right) .$$

M2 [t_2, t_3]: D_y is conducting, and its equivalent circuit is shown in Fig. 6.4(b). v_m is clamped to the DC bus voltage, while i_x decreases linearly. Since i_x is higher than i_s, these two current differences charge the bulk capacitor C_B. The rectified input line current is

$$i_x = \frac{\left| v_{in} \right| - V_B}{L_x} \left(t - t_2 \right) + i_x \left(t_2 \right) \qquad t_2 < t < t_3, \tag{6.6}$$

with the boundary conditions, $i_x(t_0) = i_x (t_3)$.

The average rectified line input current is equal to the average inductor current i_x over one switching cycle ,and is given by

$$\left| i_{in} \right| = i_{x,ave} = \frac{1}{T_s} \int_{t_0}^{t_3} i_x \, dt = \frac{1}{T_s} \left(\int_{t_0}^{t_2} i_x \, dt + \int_{t_2}^{t_3} i_x \, dt \right). \tag{6.7}$$

Substituting (6.5) and (6.6) into (6.7) yields

$$\left| i_{in} \right| = \frac{2}{Z_0 w_0 T_s} \left| v_{in} \right| + \frac{2 I_s w_0 \cos q}{w_s + w_0} - \frac{2 V_B}{Z_0 w_0 T_s} + \frac{P_0}{V_{in}}, \tag{6.8}$$

where P_0 and V_{in} are the output power and the line peak voltage, respectively. To achieve unity power factor, the second term of Eq. (6.8) should equal zero, which is

$$I_s = \frac{w_s + w_0}{2 w_0 \cos q} \left(\frac{2 V_B}{Z_0 w_0 T_s} - \frac{P_0}{V_p} \right), \tag{6.9}$$

then (6.8) becomes

$$\left| i_{in} \right| = \frac{2}{Z_0 w_0 T_s} \left| v_{in} \right|. \tag{6.10}$$

This shows that the rectified line input current is proportional to the line input voltage so that unity power factor can be obtained under the condition of (6.9). However, the unity power factor condition formula is more complicated than those of the voltage source and current source CPPFC converters. So, Pspice or Saber simulation is usually used to adjust the circuit parameters to achieve unity power factor.

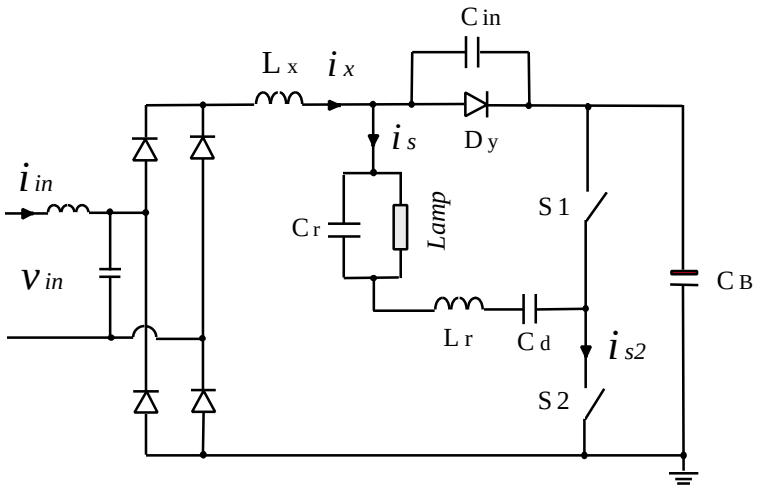
6.4 Basic CIC-CPPFC Electronic Ballast

6.4.1 Principle of Operation

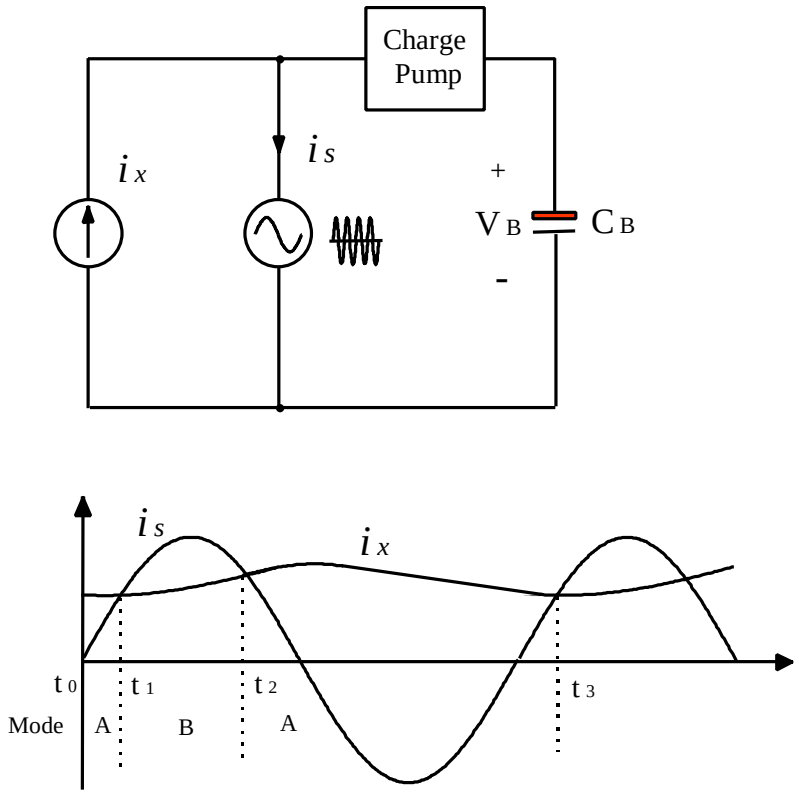
The series resonant parallel-loaded tank can be considered a high frequency current source if the lamp voltage is constant; the proposed basic CIC-CPPFC electronic ballast is shown in Fig. 6.6(a). Its operation also can be explained through its block diagram and its waveforms shown in Fig. 6.6(b).

Mode A [t_0, t_1]: The rectified input line current i_x is higher than the load current i_s, and the unbalanced current flows through the charge pump to the bulk capacitor C_B. That means the line input directly provides the power that the load needs, and the extra energy is then delivered to the bulky capacitor C_B.

Mode B [t_1, t_2]: The rectified input line current is smaller than the load current. That means the line input cannot provide enough power for the load. Therefore, the bulk capacitor C_B has to supply energy with the load through the charge pump so that the load can absorb constant power.



(a)



(b)

Fig. 6.6 (a) Basic continuous input current CPPFC electronic ballast

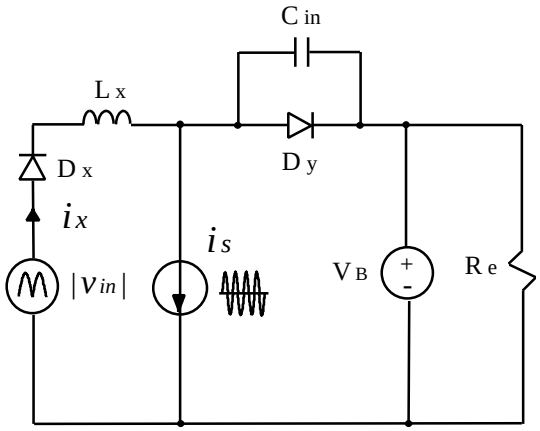
(b) The CIC-CPPFC converter diagram and its waveforms

From this converter, the input current is continuous and a small input filter can be used. Furthermore, the resonant inductor current can be minimized since the line rectifier is always on, and the conduction angle is 360^0 while the line rectifier of the basic CS-CPPFC electronic ballast has a maximum conduction angle of 180^0. Besides, the resonant peak current has a limitation to meet the unity power factor condition for CS-CPPFC converter. Therefore, the power devices can deal with less resonant inductor current. Thus, this electronic ballast has less switching current stress.

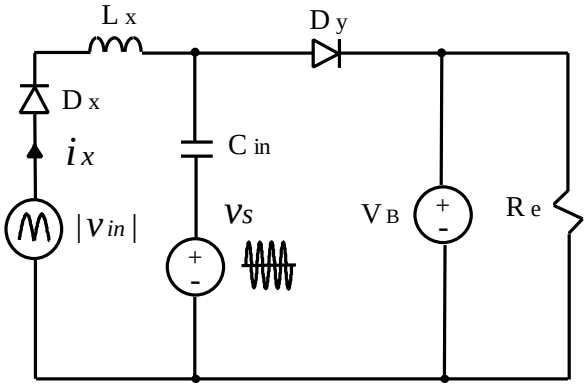
6.4.2 A Family of CIC-CPPFC Electronic Ballasts

A family of CIC-CPPFC electronic ballasts are derived, based on the generalized concept circuit of Fig.6.4(a) and high frequency capacitor shift rule. The Thevenin circuit of i_s and C_{in} of Fig. 6.4(a) is shown in Fig. 6.7. This shows that by simply adding an inductor to the basic VS-CPPFC converter and the basic CS-CPPFC converters, these converters then become the CIC-VS-CPPFC and the basic CIC-CS-CPPFC converter, as shown in Fig. 6.7.

If C_{in} is shifted through the bulk capacitor in Fig. 6.6(a), then the resulting electronic ballast is shown in Fig. 6.8(a). If C_{in} is split into two capacitors, then the resulting circuit becomes the one shown in Fig. 6.8(b). Moreover, if C_{in2} is shifted through C_B, the resulting circuit becomes the one shown in Fig. 6.8(c). By using the symmetry circuit concept and adding another charge pump to Fig. 6.8(b), Figure 6.8(d) shows the symmetrical CIC-CPPFC version, where small input current ripple can be obtained. If both capacitor C_{y1} and C_{y2} are shifted through C_{in1} and C_{y2} in Fig. 6.8(d), respectively, then the converter becomes Fig. 6.8(e). C_{y1} can be saved since the equivalent C_{eq} of C_{in1}, C_{in2} and C_{y1} is in parallel with D_{y1}, therefore, the electronic ballast becomes Fig. 6.8 (f). From the basic CIC-CPPFC converter shown in Fig. 6.3(b), the load can be replaced by the series resonant parallel-load for electronic ballast application. The resulting circuit becomes the one shown in Fig. 6.8(g). Figure 6.8 (h) and (i) are two CIC-VS-CPPFC electronic ballasts. By combining the CIC-VS-CPPFC converter and the CIC-CS-CPPFC converter, Fig. 6.8(j) shows CIC-VSCS-CPPFC electronic ballast. This electronic ballast is very attractive, and will be analyzed in the next section.



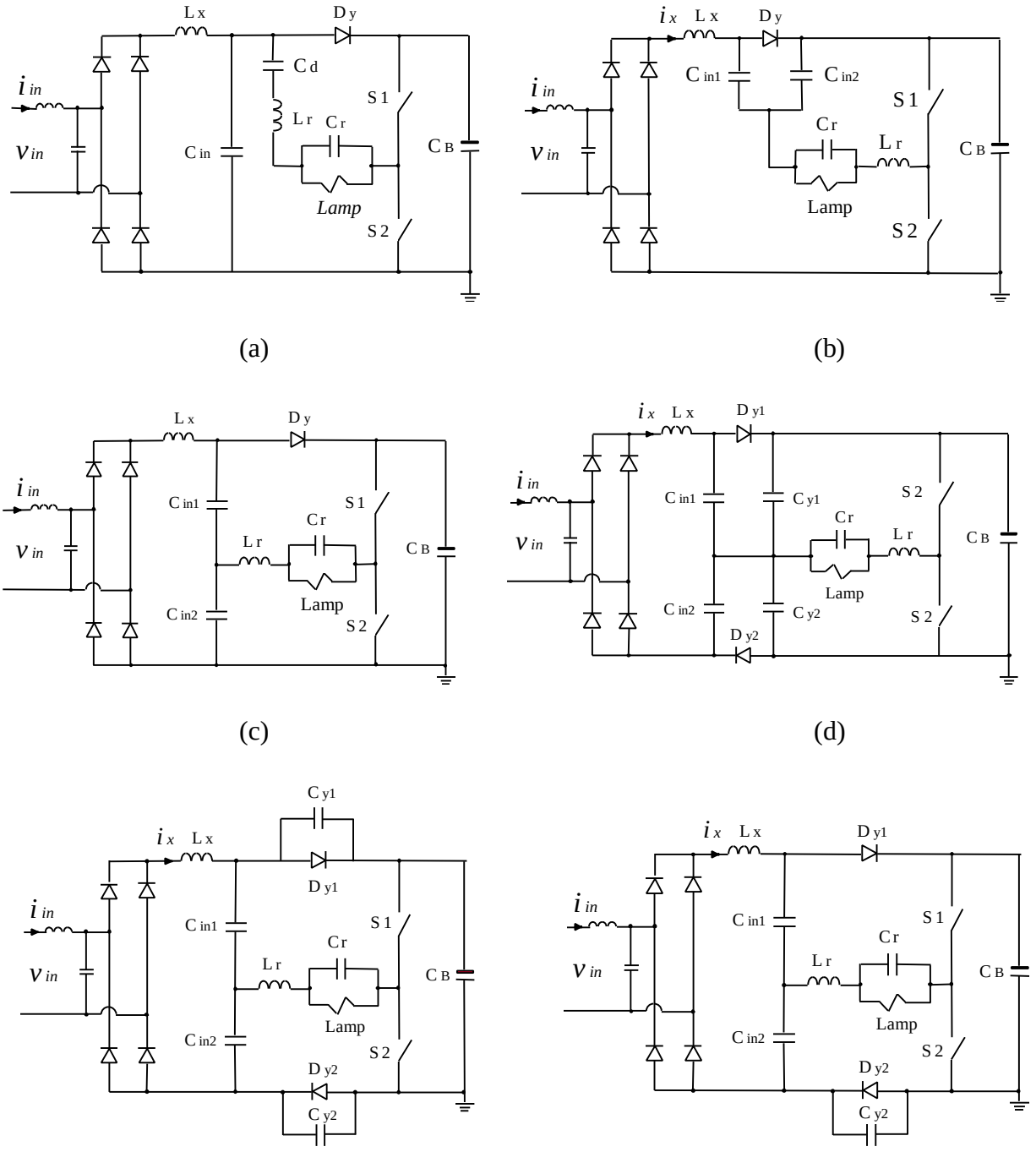
(a)



(b)

Fig. 6.7 (a) Thevenin circuit of CIC-CPPFC converter

(b) Norton circuit of CIC-CPPFC converter

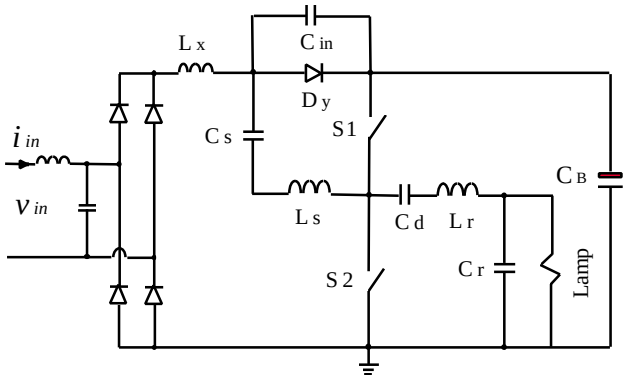


(a) (b)

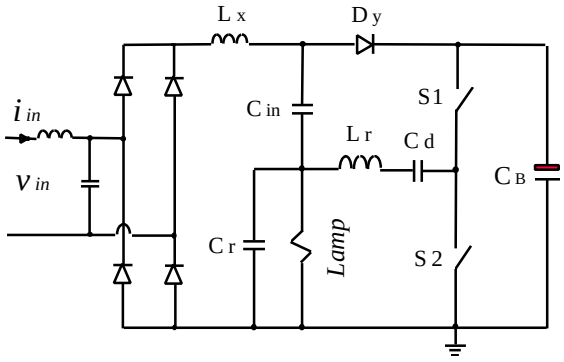
(c) (d)

(e) (f)

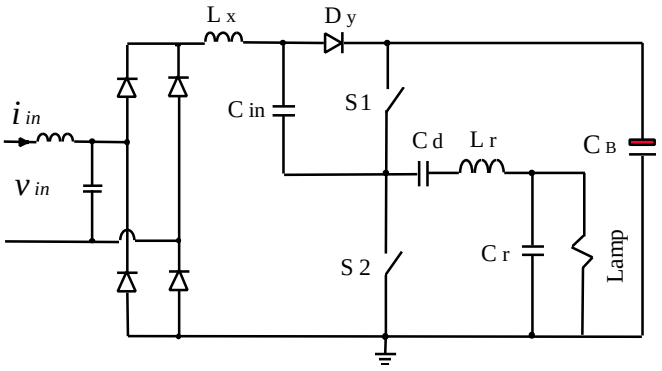
Fig. 6.8 A family of CIC-CPPFC electronic ballasts



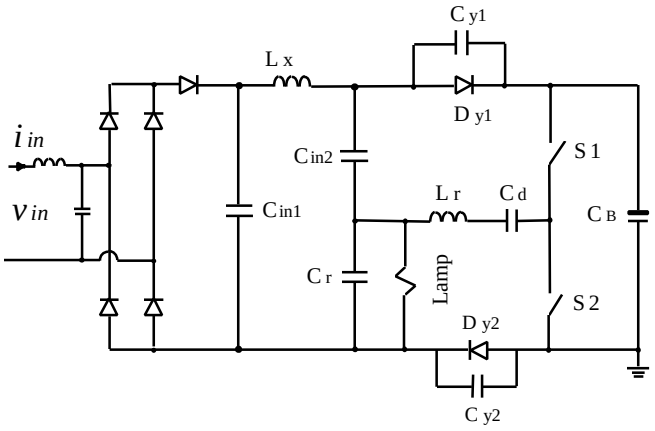
(g)



(h)



(i)



(j)

Fig. 6.8 Continued a family of CIC-CPPFC electronic ballasts

(a) ~ (g): CIC-CS-CPPFC electronic ballast

(h) ~ (j): CIC-VS-CPPFC electronic ballast

6.4.3 Design Considerations

The design objective of the proposed CIC-CPPFC electronic ballast is to get the values of the charge pump capacitor C_{in}, input inductor L_x, and the resonant components L_r and C_r. Under the unity power factor condition, the instantaneous input power is

$$p_{in}(t) = \frac{2 f_s}{w_0 Z_0} \left| v_{in}(t) \right|^2 . \tag{6.11}$$

Averaging Eq. (6.11) over one half line cycle yields

$$P_{in} = \frac{f_s V_{in}^2}{w_0 Z_0}, \tag{6.12}$$

where V_{in} is the line peak voltage. According to the power balance between the input and the output,

$$P_0 = h P_{in}, \tag{6.13}$$

where h is the conversion efficiency. Substituting Eq. (6.12), $w_0 = \frac{1}{\sqrt{L_x C_{in}}}$ and $Z_0 = \sqrt{\frac{L_x}{C_{in}}}$ into (6.13) yields

$$C_{in} = \frac{P_0}{h f_s V_{in}^2} . \tag{6.14}$$

According to the simulation results, if the resonant frequency ω_0 is about two-thirds of the switching frequency, then unity power factor can be achieved. The input inductor is given by

$$L_x = \frac{9 h V_{in}^2}{16 p^2 f_s P_0} . \tag{6.15}$$

The excitation voltage of the series resonant parallel-loaded tank is not actually a pure square waveform, and is modulated by the rectified line voltage. To simplify this resonant tank design, the converter is designed near the peak line voltage, where the excitation voltage is close to a pure square waveform. If only the fundamental component is taken into account, the lamp voltage v_o is given by

$$V_{0,rms} = \frac{\sqrt{2} V_B}{p} \frac{1}{\sqrt{\left(1 - \frac{w_s^2}{w_p^2}\right)^2 + \left(\frac{w_s L_r}{R_L}\right)^2}}, \tag{6.16}$$

where $w_s = 2p f_s$, and $w_p = \frac{1}{\sqrt{L_r C_r}}$. Here the load resistance R_L, which is the lamp impedance, is assumed to be a pure resistor in the steady state, and is given by

$$R_L = \frac{V_{0,rms}^2}{P_0}. \tag{6.17}$$

Given the lamp voltage $V_{0,rms}$ = 230 V, resonant frequency f_0 = 54 kHz ($\omega_p = 2\pi f_0$), f_s = 58 kHz, V_B = 320 V, lamp power P_0 = 85 watts, line peak voltage V_{in} = 280 V and the efficiency η = 83%, then L_x, C_{in}, L_r and C_r are

L_x = 750 μH, C_{in} = 22.5 nF L_r = 820 μH C_r = 11 nF.

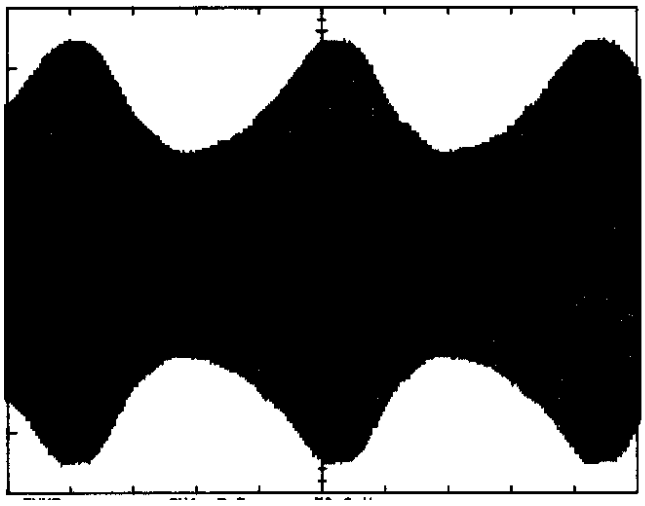
6.4.4 Experimental Verifications

To verify the proposed power factor correction electronic ballast, an 85-watt CIC-CPPFC electronic ballast of Fig. 6.6(a) for two 45-watt lamps in series was built. The circuit parameters are as follows:

L_x = 760 μH, L_r = 850 μH, C_r = 10.7 nF, C_d = 0.47 μF, C_{in} = 23.2 nF, C_B = 47 μF/450 V.

The switching frequency at normal operation is about 64 kHz with 200V line input. If the electronic ballast operates in constant switching frequency and duty cycle without any modulation, the lamp current waveform is shown in Fig. 6.9. The measured lamp crest factor is 1.77. It can be seen that the lamp current waveform is modulated by twice of the line frequency. This is mainly because the resonant tank is modulated by C_{in}. The resonant capacitor is $C_{in} + C_r$ near the line peak voltage and C_r near the zero-crossing of the line voltage. So, the lamp current has twice line frequency ripple, which deteriorates the crest factor. This high crest factor may shorten the lamp life. In order to reduce the low frequency lamp current ripple, and improve the lamp crest factor, the switching frequency modulation scheme is used. From the measured lamp current waveform shown in Fig. 6.9, it is shown that the lamp has high current near the zero crossing of the line voltage and small lamp current near the line peak voltage. It is required that the controller operate in such a way that the switching frequency is high near the zero crossing of the line input voltage, and the switching frequency is low near the line peak voltage so that the lamp current waveform has constant amplitude. Figure 6.10 shows the average lamp current control with switching frequency modulation to improve the crest factor. This modulation scheme consists of

a lamp current sensor, error amplifier and timing resistor. When the lamp current is high near the zero crossing of the line voltage, the sensed lamp current signal V_1 increases. The output voltage V_2 of the error amplifier becomes low so that more base current flows through transistor T, and the output resistance of transistor T becomes small, which increases the switching frequency. Therefore, the lamp current does not increase, and it is regulated to a fixed value. The lamp current waveform with switching frequency modulation is



t: 2 ms/div i_{lamp}*: 0.2 A/div*

Fig. 6.9 Measured lamp current waveform with constant switching frequency

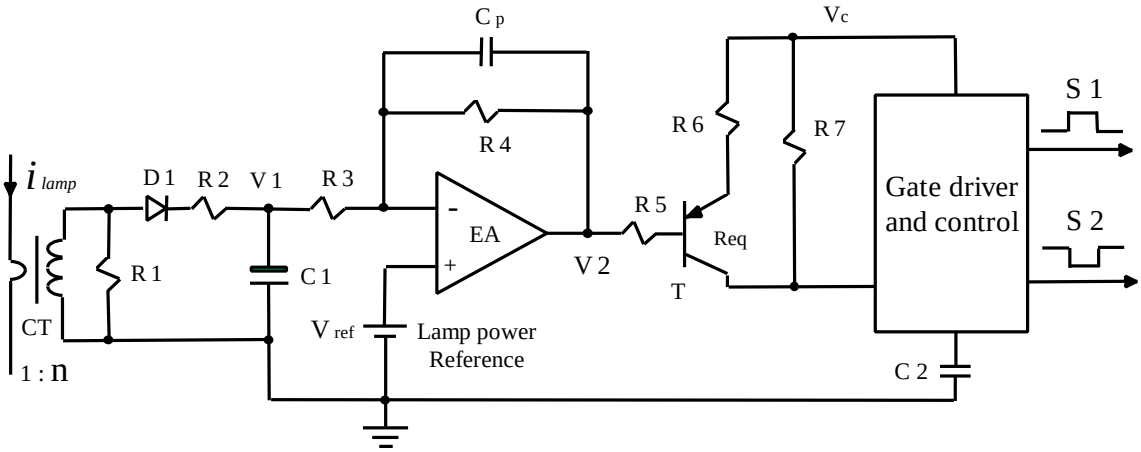
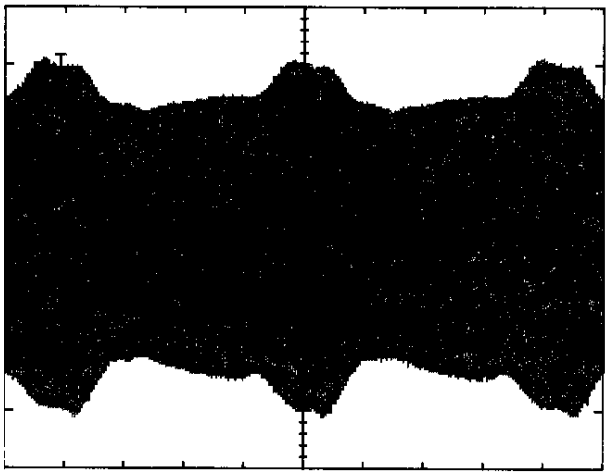


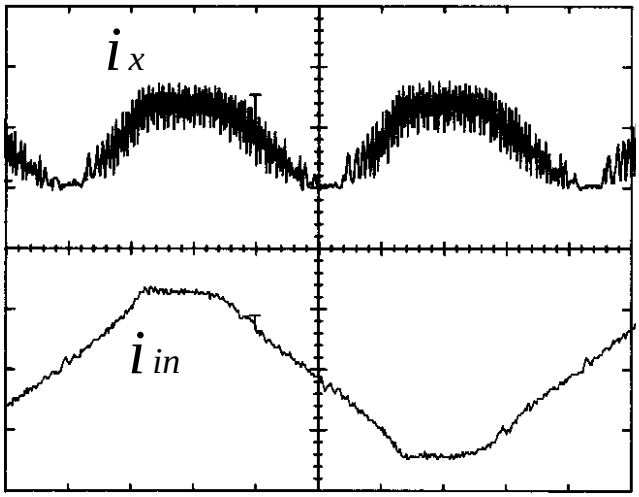
Fig. 6.10 Average lamp current control with switching frequency modulation

shown in Fig. 6.11. The measured crest factor is 1.54. Of course, line voltage feed-forward scheme also can be used to improve the crest factor. However, the developed average lamp current control with switching frequency modulation is able to keep lamp constant power operation even for a certain line voltage variation. The input inductor current i_x and the line input current waveform are shown in Fig. 6.12(a). It is shown that the inductor current i_x is continuous, so a small line input filter can be utilized. The measured total harmonic distortion (THD) is 10.6% and each harmonic component satisfies the IEC 1000-3-2 Class C requirements. Figure 6.12(b) shows the switching current waveform near the zero crossing of the line voltage and near the peak line voltage. The switching frequencies are 72 kHz and 64 kHz near the zero crossing of the line voltage and the line peak voltage, respectively. Zero voltage switching is always maintained, so the switching loss is minimized. The measured maximum switching current is only 1.3A. This switching current is only 40% of the voltage source CPPFC electronic ballast with low frequency second resonance [C10], and 65% of the current source CPPFC electronic ballast [D5]. Thus, small current rating power devices and a small size resonant inductor can be utilized, which reduces the cost. The DC bus voltage across the bulk capacitor C_B is also tested at preheat, start-up and dimming mode operations with 200 V rms input by slowly reducing the switching frequency from 85kHz to 65 kHz instead of fast sweeping the switching frequency. The measured maximum DC bus voltage is 420 V, which occurs at the



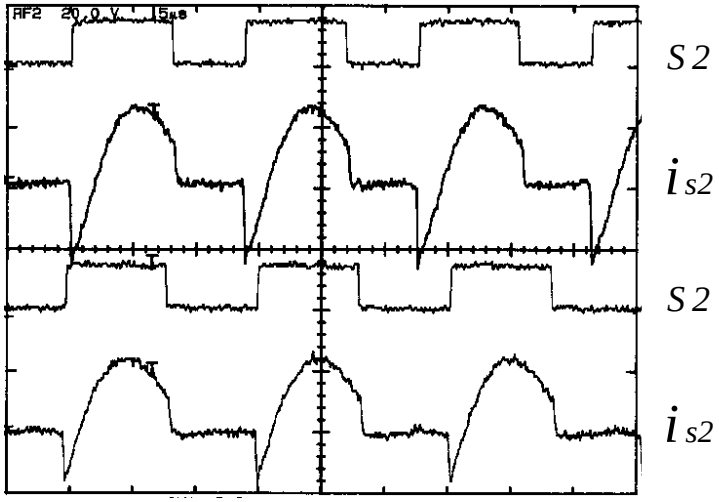
t: 2 ms/div *i_{lamp}: 0.2 A/div*

Fig. 6.11 Measured lamp current with switching frequency modulation



t: 2 ms/div i_x and i_{in}: 0.5 A/div

(a)



t: 5 ms/div S2: 20 V/div i_{s2}: 1 A/div

(b)

Fig. 6.12 Measured line current and switching waveforms

(a) Measured line input current and voltage

(b) Measured switching waveforms

Top two waveforms: Near the zero crossing of the line voltage

Bottom two waveforms: Near the peak line voltage

lamp start-up mode with 5-watt output. This low DC bus voltage stress is mainly because the circulating current is very small at light load. It should be noted that the DC bus voltage stress at start-up for 1 second preheat and then quickly sweeping the switching frequency to ignite the lamp is much lower than that of slowly reducing the switching frequency to ignite the lamp. At the normal lighting operation, the DC bus voltage across C_B is about the line peak voltage. The input inductor L_x carries continuous current with a small ripple. So the size and volume are much smaller that the resonant inductor.

6.5 CIC-VSCS-CPPFC Electronic Ballast with a Wide Range of Line Input Voltage

6.5.1 Principle of Operation

The conventional single-stage PFC electronic ballasts suffer from high crest factor, big lamp power variation and high THD with a wide range of line input voltages. They have a good performance with ±10% line variation, and have to be individually designed for the different line input voltages. One disadvantage is that the electronic ballasts use different components, which increases the cost. Another issue is that companies may suffer from market vibration if the designed products are suitable for only one country's line input. Therefore, it is important that the electronic ballasts are able to operate with different line input voltages so that they can be sold in many areas. The designed single-stage PFC electronic ballasts will have a high cost if they operates over universal line input. But, it is possible to have the electronic ballast operate with a wide range line input using the same design and low cost components.

In this section, a single-stage CIC-VSCS-CPPFC electronic ballast with a wide range input voltage from 180 V to 265 V is proposed and implemented. It has extremely low DC bus voltage at preheat, start-up, dimming modes and normal operation. In addition, it has constant lamp power operation, low crest factor and THD over a wide range line input. The input current is continuous so that a small line input filter can be used.

DC bus voltage stress at light load is a common issue for single-stage PFC circuit. One way to reduce the DC bus voltage is to adjust the input impedance in such a way that the input impedance is high near the switching frequencies at preheat and start-up modes so that the input current can be reduced at light load. Usually, the frequencies during the preheat and start-up modes are higher than that of normal operation. An inductive component appears high impedance

at high frequency. Therefore, the inductive component is preferred to connect with the line rectifier. Figure 6.13 shows one implementation using this concept, where an inductor is inserted after the line rectifier. This circuit is actually a CIC-VSCS-CPPFC electronic ballast. By properly designing the circuit parameters, the input impedance could be higher due to L_x. However, adding an inductor increases the cost. Here, L_x is much smaller than L_r. Besides, the current through L_x is much smaller than that of L_r, since it conducts almost DC current. Therefore, the volume and size of L_x are much smaller than those of L_r. If a high frequency capacitor C_{in1} is connected in parallel with the line rectifier, then it may be possible to form a resonant tank, composed of C_{in1}, L_x, C_{in2} and C_r, near the switching frequencies during the preheat and start-up operation. This also helps reduce the DC bus voltage stress at light load. The resonant circulating current can be designed to be small since the rectified line current is continuous. Capacitors C_{y1} and C_{y2} are charged and discharged by this resonant current. At preheat and start-up modes, they cannot be totally discharged because the resonant inductor current is small. The conduction angle of diodes D_{y1} and D_{y2} becomes small. So, the input power delivered to the bulk capacitor C_B is reduced, and the voltage stress across C_B is suppressed. This low DC bus voltage at start-up is mainly due to the small circulating current at light load.

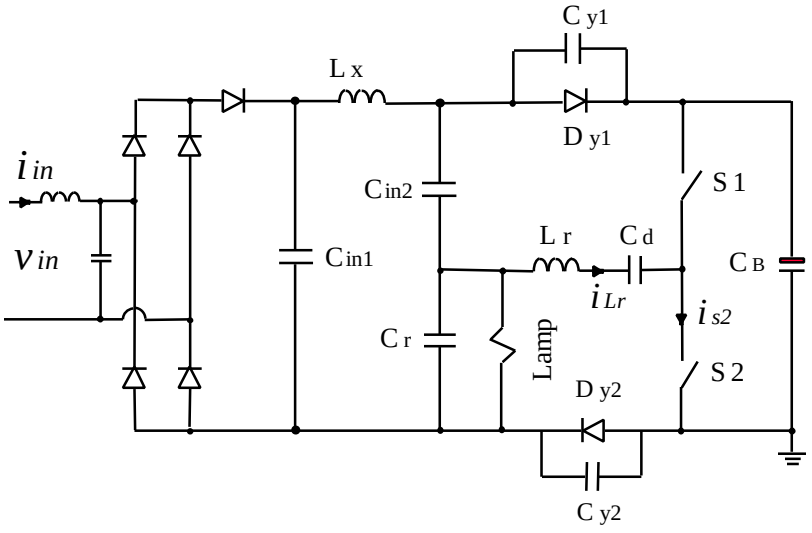


Fig. 6.13 The proposed CIC-VSCS-CPPFC electronic ballast with a wide range line input

6.5.2 Experimental Results

The developed CIC-VSCS-CPPFC electronic ballast with average lamp current control with switching frequency modulation was implemented and tested. The circuit parameters are

L_x = 215 μH L_r = 665 μH C_r = 3.9 nF C_{in1} = 10 nF

C_{in2} = 8.2 nF C_{y1} = 20.6 nF C_{y2} = 10 nF.

The characteristics of the preheat, start-up modes and normal lighting operation are tested.

6.5.2.1 Preheat and Start-up Characteristics

The most concern is the DC bus voltage stress during the preheat and start-up mode operations, which correspond to the light load operation. Usually, this DC bus voltage is higher than that of the normal lighting operation. So, the highest DC bus voltage occurs during the lamp preheat and start-up modes, which determines the voltage rating of the bulk capacitor and power switches. In general, the electronic ballast has one second at preheat mode, and then quickly sweeping the switching frequency to the normal lighting frequency to ignite the lamp. Thus, there is no enough time to charge the bulk capacitor during this transient period if the lamp is ignited. However, the DC bus voltage will further increase if the lamp does not ignite, especially at a low temperature. So, it is better to measure the DC bus voltage by slowing reducing the switching frequency from preheat mode to ignite the lamp so that there is enough time to charge the bulk capacitor, and we can see how high the DC bus voltage will be. Continuously slowly reducing the switching frequency, the circuit enters to the dimming operation and finally operates in normal lighting. Actually, the DC bus voltage reaches maximum at the lamp start-up. After the lamp is ignited, this DC bus voltage decreases with increasing the lamp power, and reaches minimum at normal lighting operation. This DC bus voltage reflects the real maximum voltage for all mode operations. Figure 6.14 shows the measured maximum DC bus voltage stress by slowing reducing the switching frequency to ignite the lamp. The DC bus voltage stress is 380 V and 480V with 200 V rms and 265 V rms, respectively. So 500 V bulk capacitor and 500 V rating power switch can be used. It should be noted that the DC bus voltage will much lower for the case of 1 second preheat and then quickly sweeping the switching frequency to ignite the lamp. The measured input current and input inductor current waveforms at start-up mode are shown in

Fig. 6.15. It can be seen that the conduction angle of the line input current is very small because the capacitors cannot be totally discharged by a small resonant inductor current.

6.5.2.2 Steady-State Characteristics

By using average lamp current control with switching frequency modulation, constant lamp power operation and low crest factor can be achieved. The measured line input current waveforms at different line input voltages are shown in Fig. 6.16. It can be seen that the high line current distortion occurs near the zero crossing of the line input voltage especially at high line. This is because the charge pump capacitors have highest voltage and they are discharged by the same resonant inductor current. Thus, these capacitors cannot be totally discharged near the zero crossing of the line input voltage, where the capacitor voltage is maximum. The input inductor current is shown in Fig. 6.17. It can be seen that the line input current i_x is continuous,

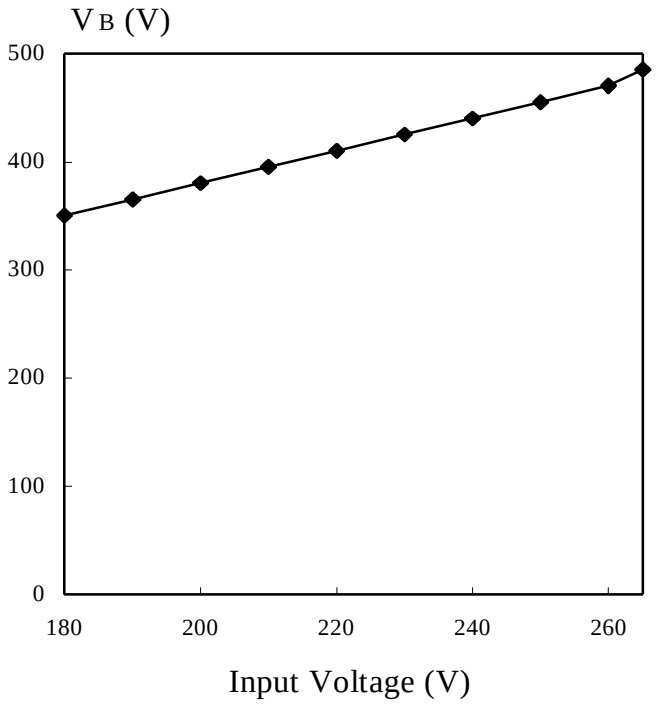
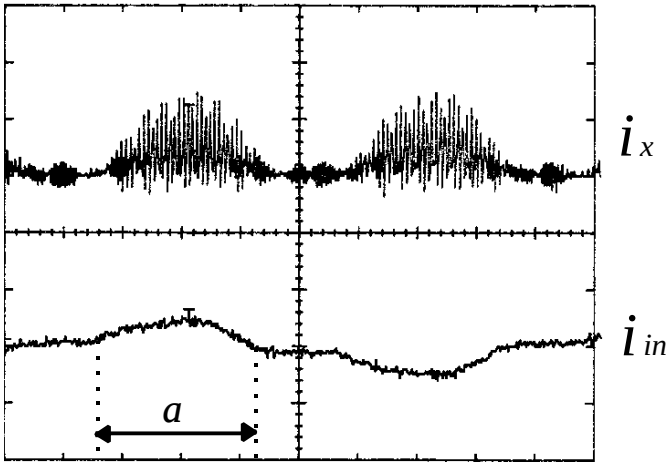
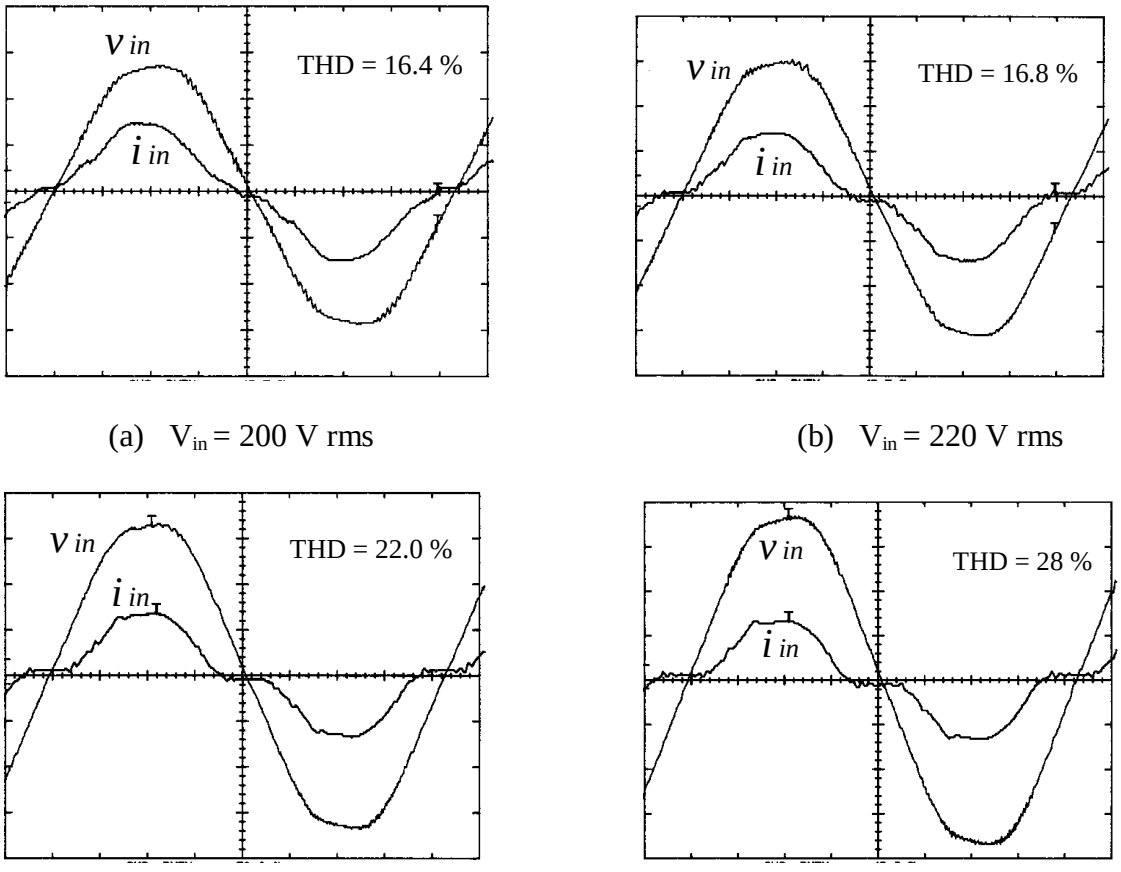


Fig. 6.14 Measured maximum DC bus voltage during start-up mode



t: 2 ms/div i: 0.5 A/div

Fig. 6.15 Measured line input current and input inductor current waveforms at start-up mode



(a) V_{in} = 200 V rms (b) V_{in} = 220 V rms

(c) V_{in} = 240 V rms (d) V_{in} = 265 V rms

t: 2 ms/div v_{in}: 100 V/div i_{in}: 0.5 A/div

Fig. 6.16 The measured line input current waveforms at different line input voltages

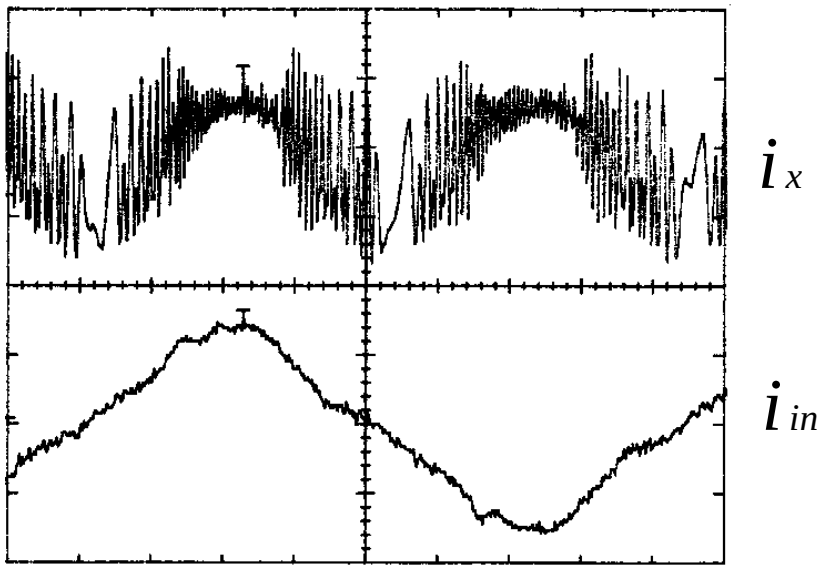


Fig. 6.17 Measured input inductor current and line input current

so a small line input filter can be used. The measured lamp THD is shown in Fig. 6.18. Although THD is a little high, each harmonic component still satisfies the IEC 1000-3-2 Class C requirements. The measured lamp current waveforms are shown in Fig. 6.19, and the measured lamp crest factor is shown in Fig. 6.20. It is shown that the lamp current waveform has almost constant amplitude so that low crest factor can be achieved. The measured crest factor is always less than 1.7 for the line voltages from 180 V to 265 V. Fig. 6.21 shows the measured lamp power at different line input voltages. It can be seen that the lamp power variation range is within 10%. It is very important to maintain zero voltage switching (ZVS) operation over a wide line input range. The average lamp current control with switching frequency modulation operates in a such a way that the switching frequency is high when the line input voltage is high. Therefore, as long as the developed electronic ballast can achieve ZVS at low line input, the circuit maintains ZVS at high line. Figure 6.22 shows the switching current waveforms at the different line input voltages. It can be seen that the circuit always operates in ZVS. The measured switching frequencies vary from 66.6 kHz to 76.9 kHz for the line voltages from 180 V to 265V. The maximum switching current is only 1.6 A. This switching current stress is only 45% of VS-

CPPFC electronic ballast with second resonance [C10] and 75% of CS-CPPFC electronic ballast [D5]. The measured overall efficiency include the filament loss is shown in Fig. 6.23. It can be seen that 80% overall efficiency can be obtained. If the filament loss is excluded, 91% efficiency can be achieved.

Table 6.2 shows performance of developed CPPFC electronic ballast. It can be seen that CIC-VSCS-CPPFC electronic ballast has best performance, low DC bus voltage stress, less switching current stress, continuous line input current, low crest factor with constant lamp power operation over a wide range of line input voltage.

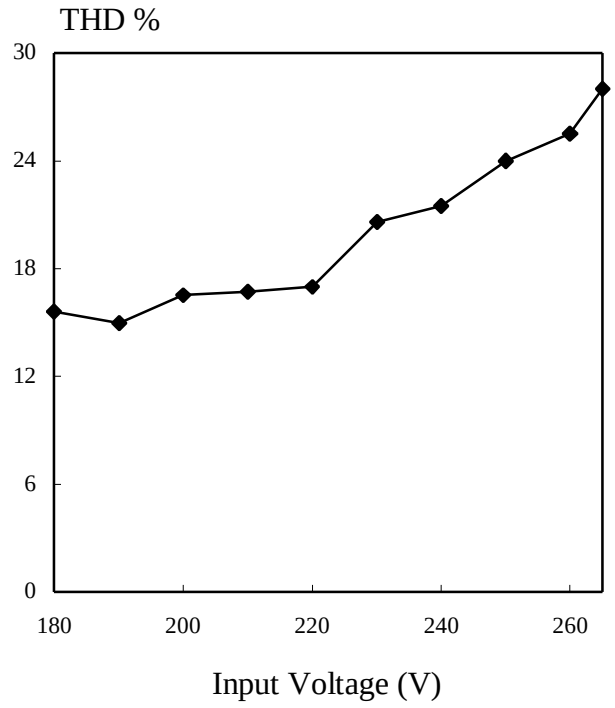
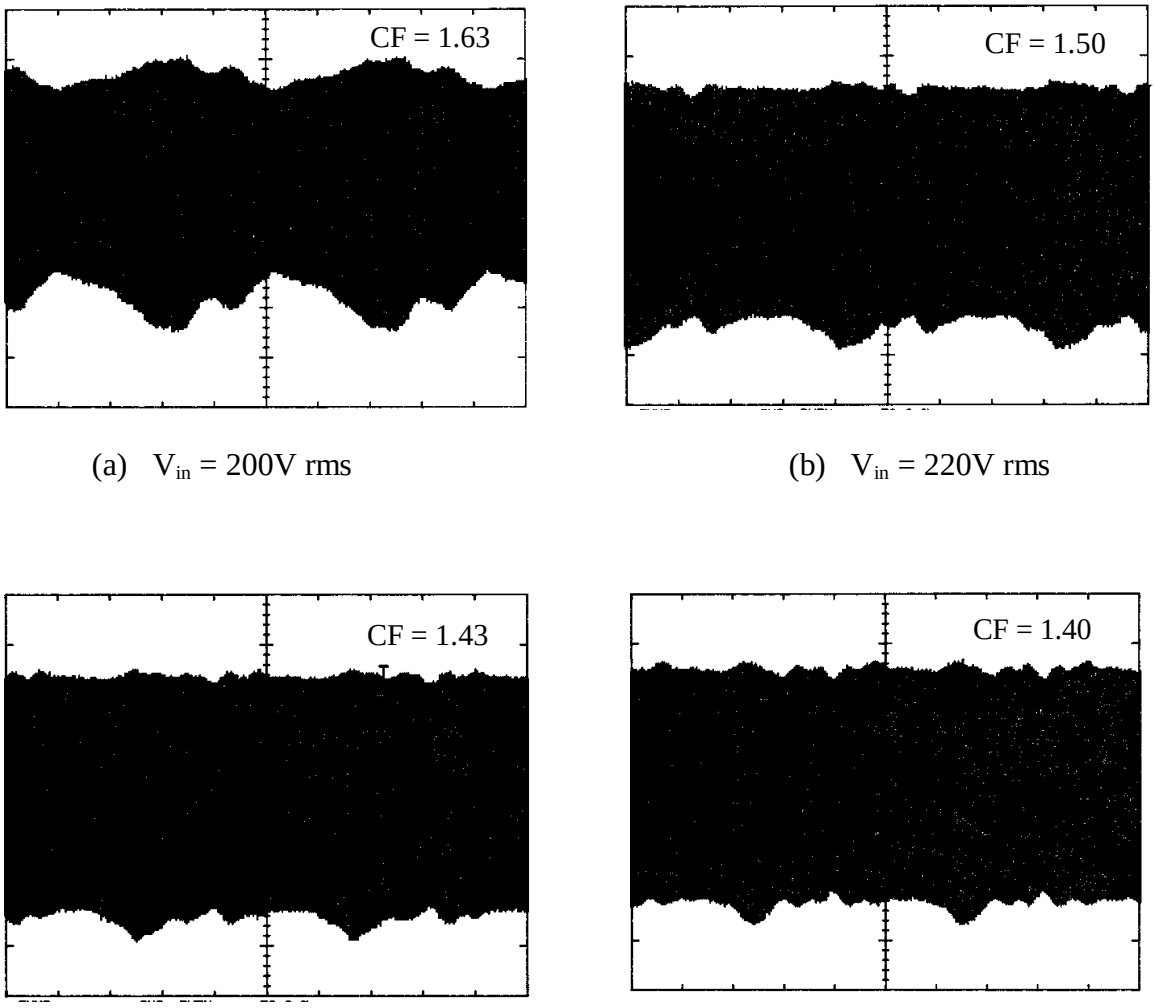


Fig. 6.18 Measured THD of the line input current



(a) V_{in} = 200V rms (b) V_{in} = 220V rms

(c) V_{in} = 240V rms (d) V_{in} = 265V rms

t: 2 ms/div i_{lamp}*: 200 mA/div*

Fig. 6.19 Measured lamp current waveforms at different line input voltages

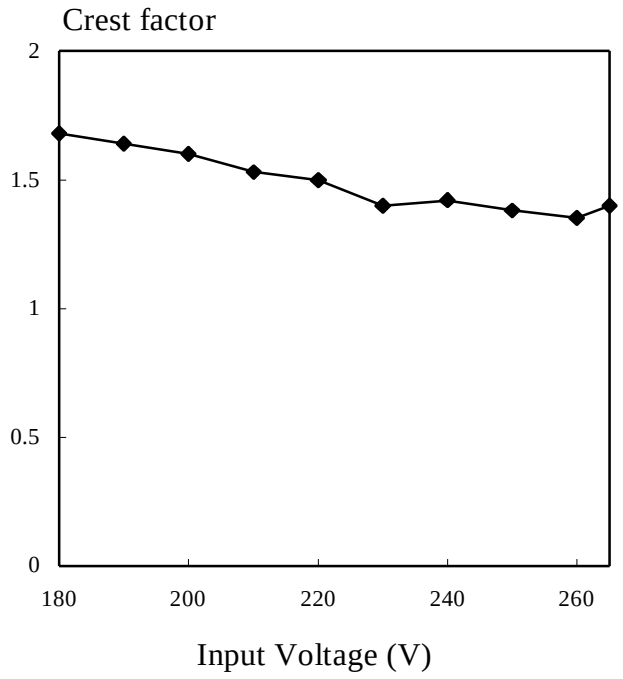


Fig. 6.20 Crest factor at different line input voltages

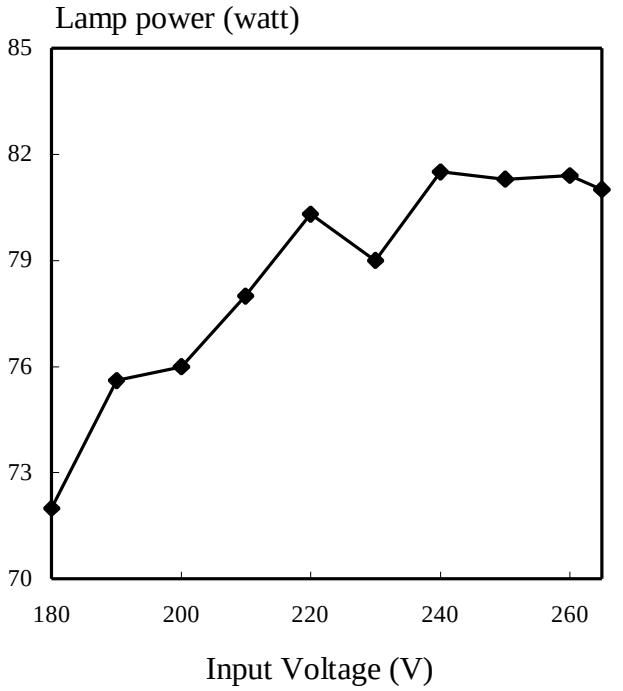
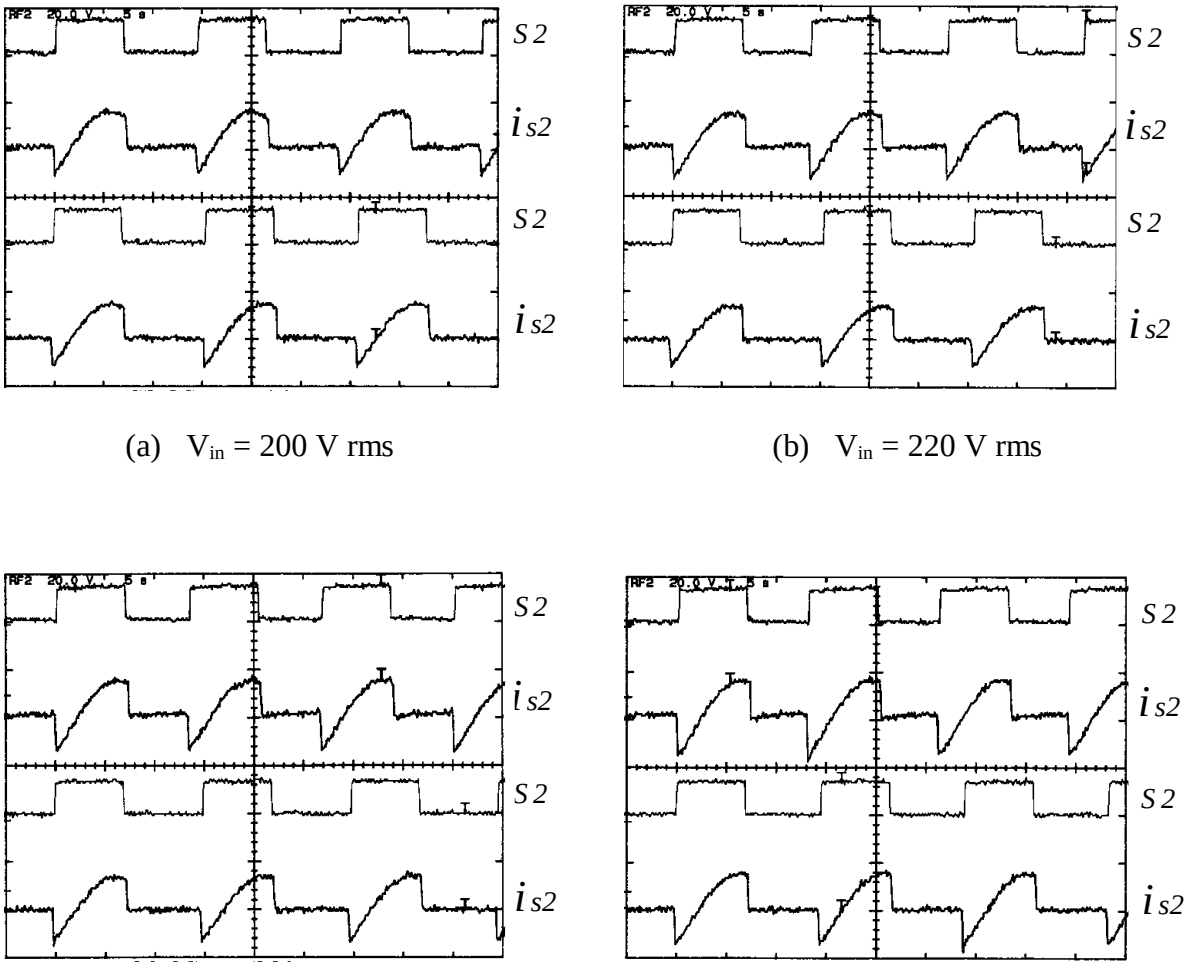


Fig. 6.21 Measured lamp power over different line input voltages



(a) V_{in} = 200 V rms (b) V_{in} = 220 V rms

(c) V_{in} = 240 V rms (d) V_{in} = 265 V rms

t: 5 ms/div *S 2: 20 V/div* i_{s2}*: 2 A/div*

Fig. 6.22 Measured switching current waveforms

Top two waveforms: Near the zero crossing of the line voltage

Bottom Two waveforms: Near the peak line voltage

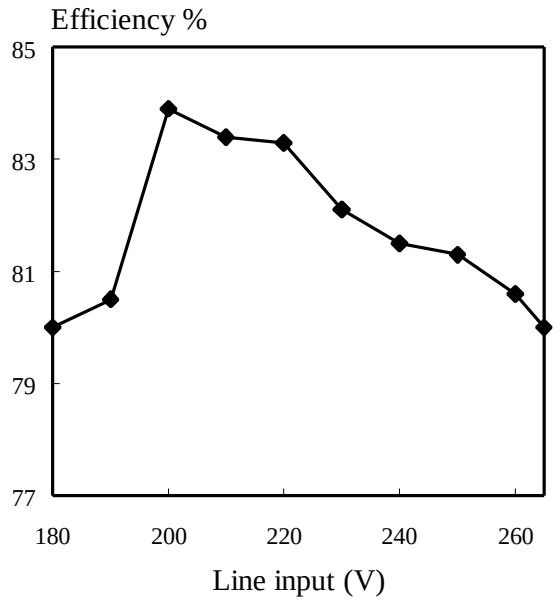


Fig. 6.23 Measured overall efficiency

Table 6.2 Performance of developed CPPFC electronic ballast

Type	THD	V_{Bmax} (V)	I_s (A)	CF	I_{in}	Inductor	Efficiency	V_{in}
VS-CPPFC	12%	800	2.4	2.60	DCM	1		180-220 V
VS-CPPFC with LFSR	5.0%	310 (410)	3.4	1.50	DCM	2	82.0 %	180-220 V
CS-CPPFC	11.0%	(470)	2.2	1.54	DCM	1	82.5 %	180-220 V
VSCS-CPPFC	13.0%	385 (495)	1.9	1.60	DCM	1	81.0 %	180-220 V
CIC-VSCS CPPFC	16.0%	(380)	1.6	1.50	CCM	2	80-84.0 %	180-265 V

6.6 Summary

The previously developed CPPFC converters have discontinuous line input current, which require a relatively large line input filter. The continuous input current charge pump power factor correction technique was developed and analyzed in this Chapter. It can be seen that all VS-CPPFC, CS-CPPFC and VSCS-CPPFC converters are able to operate in continuous line input current mode by simply inserting a small inductor in series with the line rectifier. The principle of operation of the CIC-CPPFC converters was also discussed. A family of CIC- CPPFC electronic ballasts are derived. Two CIC-CPPFC electronic ballasts were implemented and tested. It can be seen that the power switches only carry the resonant inductor current so that low current rating devices can be used. The developed CIC-VSCS-CPPFC electronic ballast has the best performance.

The main advantages of the developed CIC-VSCS-CPPFC electronic ballast are:

1. Extremely low DC bus voltage stress during the preheat, start-up, dimming modes and normal operation so that low voltage rating bulk capacitor and power switches can be used.
2. High power factor and low THD. The measured line current harmonics satisfy the IEC 1000-3-2 Class C requirements.
3. Constant lamp power operation over a wide range of line input voltages.
4. ZVS is maintained over a wide range of line input and at any operation mode.
5. Less switching current stress.
6. Only one resonant inductor and an additional small inductor are used. The developed electronic ballast has a low cost.

CHAPTER 7

CONCLUSIONS

Power converters in common use today produce a poor power factor and rich harmonic current, which deteriorates the power line quality and may interfere with other power electronic equipment. To clear the power lines, stringent requirements such as IEC 1000 have recently been enacted. Power factor correction techniques have therefore become very attractive. Adding a power factor correction function to existing power converters increases the cost about 10% to 15%, however, which is undesirable. In order to reduce the cost, it is attractive to integrate the power factor stage with the power converter so that at least one power switch and its control can be eliminated.

This dissertation developed several power factor correction techniques: the integrated PWM single-stage PFC, VS-CPPFC, CS-CPPFC, VSCS-CPPFC, and CIC-CPPFC.

The integrated single-stage PFC converter actually combines the PFC stage with the PWM DC/DC converter. The DC bus voltage across the bulk capacitor is the main issue at light load. This DC bus voltage stress is usually determined by the power balance between the input and the output. High DC bus voltage exists at light load for the integrated PWM DCM PFC with CCM DC/DC converter so that a high voltage rating bulk capacitor and power switch have to be used. The integrated PWM DCM PFC with DCM DC/DC converter was developed. It is free from the DC bus voltage stress at any load operation, but it suffers from high current stress because of DCM operation. As a result, the conduction loss, copper loss of the inductive components, and switching loss increase, which decreases the conversion efficiency. The DC bus voltage feedback concept was proposed to reduce the DC bus voltage stress at light load. It simply inserts a feedback winding coupled with the isolated transformer, which is in series with the input choke. When the DC bus voltage increases, the PFC stage automatically reduces the input power from the line input so that the unbalanced power between the input and the output is reduced. As a

consequence, the DC bus voltage is suppressed by this negative feedback in the power stage. Also, power is transferred directly from the line input to the load without being processed by the power switch. This reduces the switching current stress and consequently improves the efficiency. The integrated CCM PFC with CCM DC/DC converter has no DC bus voltage stress, because the input power and the output power can be automatically balanced. The conduction loss and switching loss can be minimized so that it has high efficiency. One CCM PFC integrated with a CCM DC/DC converter was implemented to show that it has good PFC and is free from DC bus voltage stress at light load.

The VS-CPPFC concept was derived and proposed. A capacitor, instead of an inductor, is used to achieve power factor correction. It is very attractive since the capacitor is usually cheaper and more reliable than an inductor. It is simply a high frequency voltage source in series with a capacitor to charge the capacitor from the line input and discharge its stored energy to the bulk capacitor to achieve power factor correction. The condition for achieving a unity power factor was derived. As long as the peak to peak voltage of the high frequency voltage source is equal to the DC bus voltage, unity power factor can be achieved no matter how the waveshape of the high frequency voltage source. One VS-CPPFC AC/DC converter was proposed, analyzed and implemented. It was shown that unity power factor can be achieved and the DC bus voltage is limited. The electronic ballast using the charge pump PFC concept is attractive since it is easy to obtain the high frequency voltage source. It is capacitor that integrates with the DC/AC inverter to achieve power factor correction. A VS-CPPFC electronic ballast with low frequency second resonance was analyzed, designed and tested. Unity power factor, low crest factor, and low DC bus voltage can be achieved. A continuous dimming VS-CPPFC electronic ballast was proposed and developed. The average lamp current control with duty ratio modulation was developed so that the lamp could operate at constant power and low crest factor over ±10% line input voltage variation. The lamp can be dimmed from 20% to 100% with low crest factor and low DC bus voltage. The main disadvantage is that the switch has to take the current not only from the PFC stage, but also from the DC/AC inverter.

The CS-CPPFC technique was presented. It uses a high frequency current source in parallel with a capacitor to achieve power factor correction. The derived unity power factor condition is equivalent to that of the VS-CPPFC converter. Actually the CS-CPPFC converter is

a Norton equivalent circuit of the VS-CPPFC converter. The main advantage of the CS-CPPFC converter is that the line input is able to directly provide energy to the load without being processed by the power switch. Thus, the switching current stress is less than that of the VS-CPPFC electronic ballast with second resonance.

The VSCS-CPPFC technique was developed. It integrates the VS-CPPFC converter with the CS-CPPFC converter. VSCS-CPPFC electronic ballast was proposed. The charge capacitor effect on the resonant tank is minimized so that the lamp crest factor is improved. The conduction angle is extended, since there is a phase difference between the voltage source and current source. The circulating current in the resonant tank is reduced, So is the switching current. This VSCS-CPPFC electronic ballast has features of constant lamp operation, low crest factor, and low DC bus voltage stress without any feedback control. The drawback of these CPPFC techniques is that the line input current is discontinuous, so a relatively large input filter has to be used.

The CIC-CPPFC technique was developed. It simply inserts an inductor in series with the line rectifier for all charge pump power factor correction converters, and the converters have continuous line input current. The circulating current and switching current can be further reduced. One CIC-VSCS-CPPFC electronic ballast with a wide range line input voltage was proposed and developed. The DC bus voltage stress at start-up mode was significantly reduced. The main reason is that the charge capacitor cannot be fully discharged by the resonant inductor current, which is much small compared with other CPPFC electronic ballasts. The conduction angle of the line rectifier becomes smaller so that the input power is small at light load. The CIC-VSCS-CPPFC electronic ballast has the promised features of constant lamp power, low crest factor, small switching current stress over a wide range line input voltage from 180 V to 265 V with developed average lamp current control and switching frequency modulation.

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