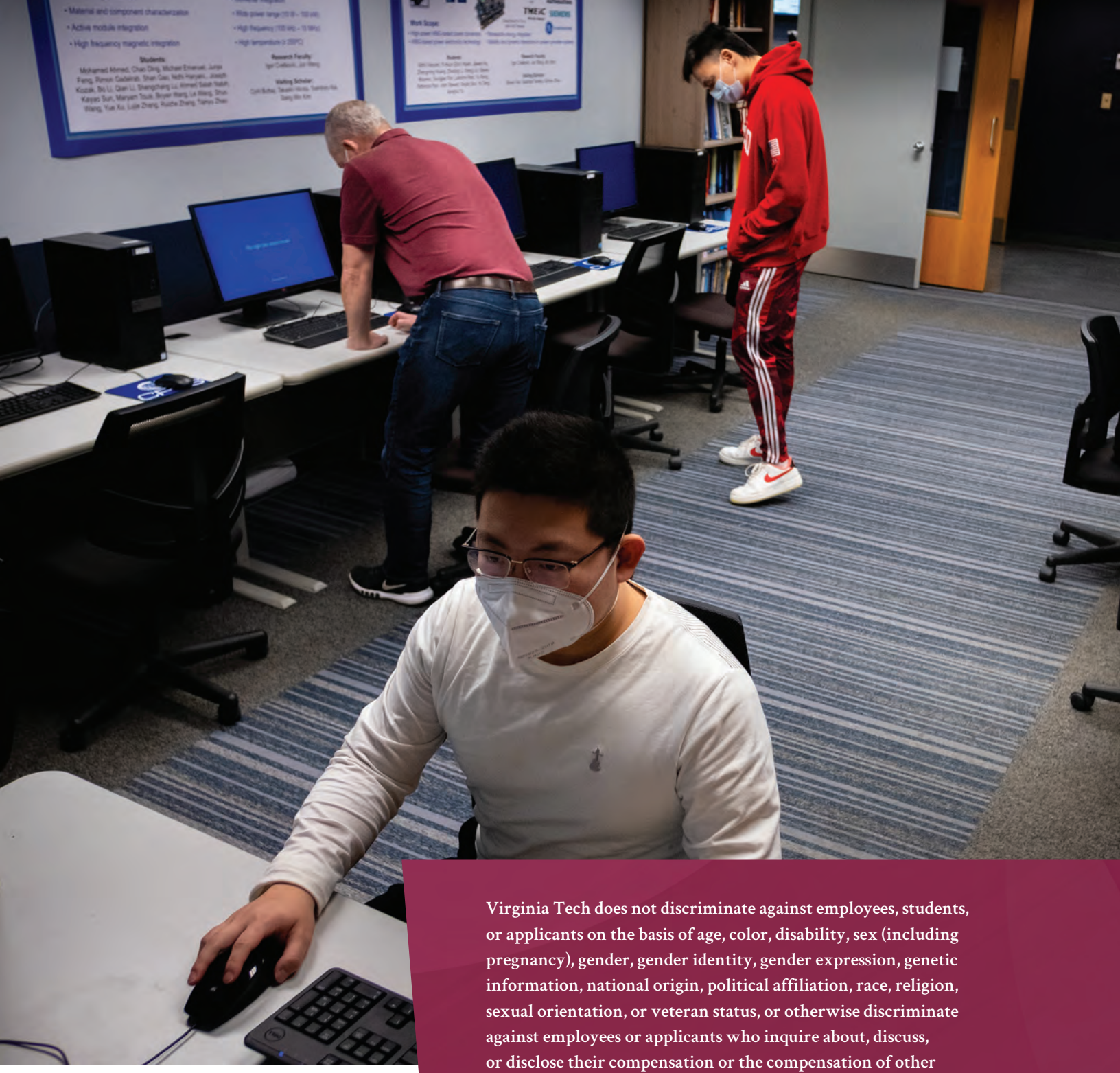
INNOVATION
Watts to Megawatts

2022 ANNUAL REPORT

CPES
Center for Power Electronics Systems



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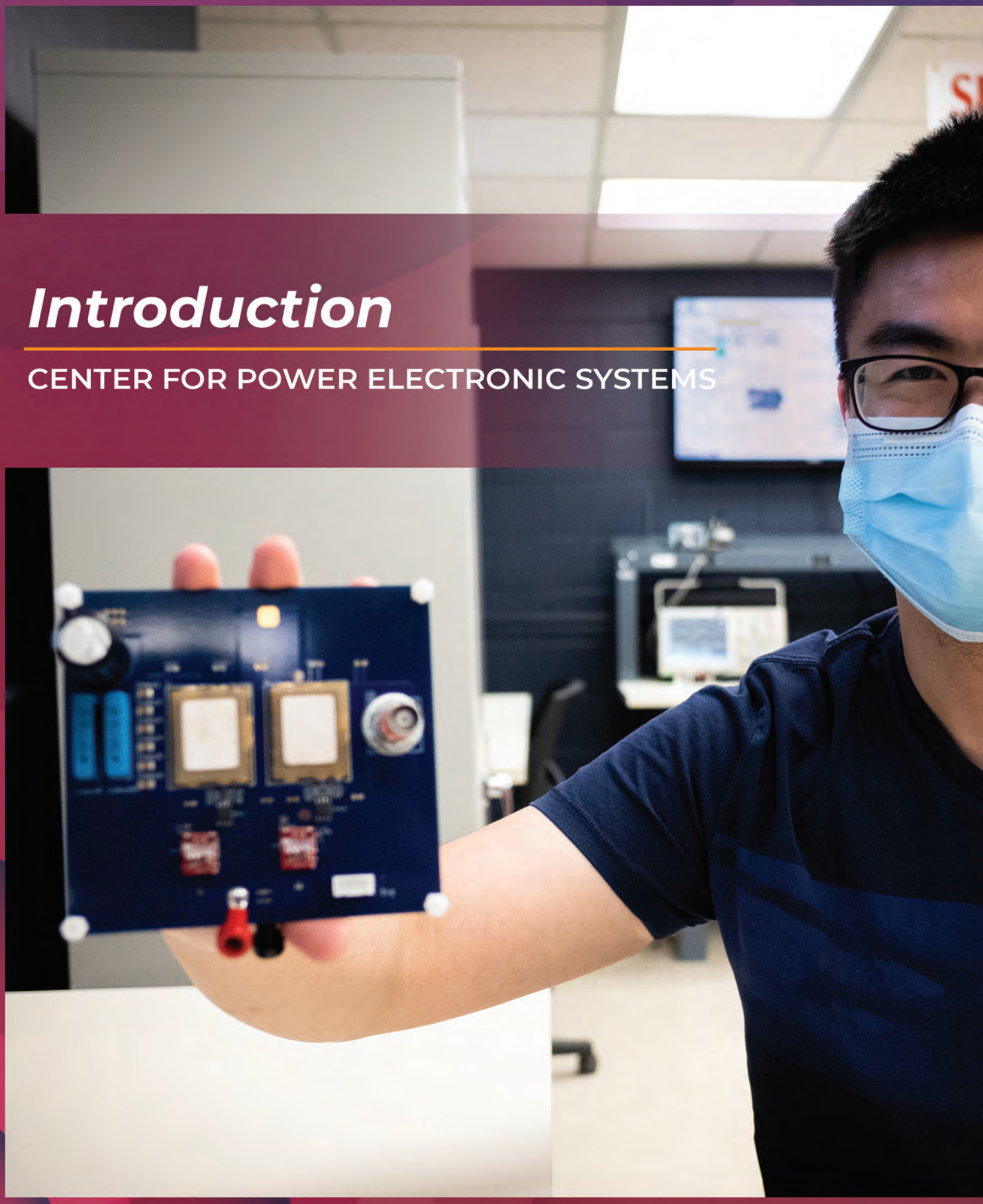
Introduction

CENTER FOR POWER ELECTRONIC SYSTEMS



Innovation has always been at the core of the Center for Power Electronics Systems (CPES). Professor Fred. C. Lee began the program at Virginia Tech more than 40 years ago with the mission to provide leadership through global collaborative research and education in creating advanced electric power processing systems of the highest value to society. Dr. Lee's vision and hard work, combined with tireless efforts from faculty, students, and staff, has resulted in an academic research center that is among the largest and most renowned in the world.

Over the past years, the Center was fortunate enough to continue building on its success under the leadership of Professor Dushan Boroyevich, who is not just a CPES alumnus, but who helped shape and co-direct the Center since the early 1990s. Under his guidance, CPES continued to expand delving into new frontiers driven by societal needs that call for increasingly more efficient power and energy processing technologies.

And so CPES stands today, growing and propelling its current iteration into the future, fully dedicated to our efforts to continue improving the electrical power processing technology that affects an ever larger and diverse number of systems that span a broad range of power levels and myriad applications from consumer electronics to electrified transportation, from industrial applications to renewable energy integration, from powering the telecommunications industry to the development of future electronic energy processing distribution and transmission grids. In all, CPES remains steadfastly committed to ***innovation from watts to megawatts!***

This book aims to be a comprehensive record of the Center's accomplishments during the year 2021. In addition to copious research project summaries and results (see Sponsored Research and Research Nuggets), one can learn more about the world-class Facilities and People necessary for these achievements. Research outputs, like Intellectual Property and Publications, are detailed as well.

The most visible change was in Center leadership. Rolando Burgos, professor, who originally joined CPES in 2002, assumed the role of Director from Dushan Boroyevich in July 2021. Under his leadership, the Center continues along its innermost tradition of training the best students in the field and researching the cutting-edge power electronics solutions that our members and sponsors expect.

Furthermore, Richard Zhang, CPES alumnus, returned as the Hugh P. and Ethel C. Kelly Professor of Electrical and Computer Engineering, bringing with him more than 20 years of technology and business leadership at GE. His technical experience includes research and development of the most advanced high-voltage DC transmission (HVDC) solution in the industry, including power electronics and revolutionary control platform, enabling bulk power transmission beyond 2 gigawatts for applications such as offshore wind parks.

As we reflect back on 2021, we offer our sincere gratitude to our members, sponsors, and colleagues from around the world. We look forward to another year of fruitful partnership where we can push the boundaries of power electronics together!

Features

A YEAR OF BREAKTHROUGHS

Change in CPES Leadership

On July 1st, CPES welcomed Rolando Burgos as its third center director. Dushan Boroyevich, who served as deputy director from 1995 to 2017, returned to his previous role.

The weight of leadership in such an esteemed organization is considerable, but Burgos is certainly up to the task. Says Boroyevich, "Rolando has been with CPES since 2002, except for a three-year stint at ABB U.S. Corporate Research Center, Raleigh, NC. He is now the most productive professor in CPES in terms of projects, graduate students, publications, etc." Boroyevich will remain active as Deputy Director, a role with which he is intimately familiar.

Dushan's leadership accomplishments are extraordinary. Assuring continuity of one of the world's foremost academic research centers was the first challenge he faced after assuming CPES directorship four years ago. Several long-serving staff members followed CPES founder Fred Lee into retirement. Boroyevich was hands-on in evaluating organizational needs, reorganizing CPES roles and hiring personnel to address them, and encouraging all the new faces to work together seamlessly.

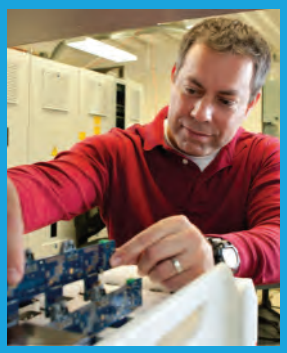
Another accomplishment has been successful in expanding and strengthening CPES with new faculty, facilities, research directions, and funding. Since 2018, Dong Dong, Yuhao Zhang, and Christina DiMarino joined the Center as tenure-track faculty, while Igor Cvetkovic, Bo Wen, Ming Xiao, Eric Hsieh, and Boran Fan, are new research faculty. In terms of facilities, the CPES Arlington lab is now an impressive 1,800-square-foot showcase for power electronics research, including a new packaging lab that completes CPES capabilities in the National Capitol Region. Lab space in Blacksburg increased as well with new facilities on the 6th floor of Whittemore Hall, improved equipment, and new expanded experimental resources. As a result of these gains in researchers and facilities, the number of research proposals submitted annually has doubled and the amount of sponsored research funding increased dramatically.

But, what Boroyevich considers his proudest achievement as CPES director was successfully navigating CPES through the COVID 19 pandemic. His leadership enabled the industrious, creative, and collaborative spirit of CPES faculty, staff, students, and scholars to overcome epochal adversities. Not only was the Center's world-leading research and education in power electronics maintained, but research output actually increased by many measures.

In assuming his new role as CPES director, Burgos knows he has large shoes to fill. "It is with great honor and an immense sense of responsibility that I humbly assume the directorship of CPES. I will try my very best to follow in the footsteps of Drs. Fred Lee and Dushan Boroyevich, who have set us on a path of excellence and success matched by few, with an unparalleled record of accomplishments, an unstoppable work ethic, and an absolute full commitment to the Center."

Rolando Burgos

2002 Ph.D., Chile
2002 Res. Assistant Professor, CPES
2009 Principal Scientist, ABB
2012 Associate Professor, CPES
2019 Professor, CPES
2021 Deputy Director, CPES



Dushan Boroyevich

1986 Ph.D., Virginia Tech
1986 Assistant Professor, Yugoslavia
1990 Associate Professor, CPES
1995 Deputy Director, CPES
2017 Director, CPES

Richard Zhang Returns to CPES

Richard Zhang, the Hugh P. and Ethel C. Kelly Professor of Electrical and Computer Engineering.

After a highly successful and influential 22 years at GE, Richard Zhang returned to CPES and Virginia Tech as the Hugh P. and Ethel C. Kelly Professor of Electrical and Computer Engineering.

CPES Director Rolando Burgos expressed the Center's collective excitement: "Richard brings high-voltage power electronics experience that only a handful of people in the world have. He immediately strengthens CPES's place as one of the leading power electronics centers in the world conducting research and education on power technologies ranging from mW to GW."

Dr. Zhang officially joined Virginia Tech in August and is located in the CPES lab in Arlington, located in the Greater Washington, DC, Metro Area.

Highlights of his illustrious career follow:

Education and Experience

Dr. Zhang received his Ph.D. in Electrical Engineering from Virginia Tech in 1998. From 1998 to 2008, he was with General Electric (GE) Global Research Center in Niskayuna, New York, leading power electronics research serving all GE industrial businesses, including GE Renewable Energy, Healthcare, Aviation, Oil and Gas, Power, Transportation, Lighting and Industrial Systems. Subsequently, between 2008 and 2016, he held several executive technology and business leadership positions at GE Oil & Gas and GE Power Conversion based in Paris, France, and in Shanghai, China. In 2017, he joined GE's Grid Integration Solutions business based in Stafford, UK, as the Chief Technology Officer.

Business and R&D Leadership

Over the years, Dr. Zhang has led wins of many large government research programs from DARPA, DOD, and DOE (exceeding $35 million); created major business initiatives, and defined and led large research and development (R&D) portfolios. He managed R&D teams with sizes ranging from 50+ to 500+ in nine different countries: US, France, Germany, UK, Finland, Canada, China, India, and Brazil. The technologies and products created by Richard's teams have been deployed in a cumulative capacity of 60+ GW in multiple industries, such as wind, solar, oil and gas, healthcare, marine, mining, power generation, and metal processing, enabling over $10 billion GE businesses and making extraordinary contributions and impact on society. In his most recent position, Dr. Zhang led research and development of the most advanced high-voltage DC transmission (HVDC) solution in the industry, including power electronics and revolutionary control platform in the industry, enabling bulk power transmission beyond 2 gigawatts for applications such as offshore wind tie-back. The resulting revolutionary HVDC solutions enabled Dr. Zhang's team to win the production and construction of the world's largest 1.4 gigawatts offshore wind-farm HVDC tie-back project in the North Sea, United Kingdom. He also guided research in the Supergrid Institute in Lyon, France.

Scholarly Impact

Additionally impressive is Dr. Zhang's scholarly dissemination of knowledge and mentoring of younger colleagues. He has co-authored 35 papers in peer-reviewed conferences and journals and has over 100 patents or patents-pending. He has won four best paper awards from his publications in IEEE journals and conferences. Dr. Zhang taught numerous courses in the GE Edison Engineering Development Program, GE Six-Sigma Training, and European Ph.D. School. He started the internal GE education programs: New Product Introduction Leadership Academy at GE Power Conversion and GE HVDC University at GE Grid Integration Solutions. Three of his GE advisees are now professors at US universities, and two are CEOs. He delivered numerous invited lectures at many professional meetings, including tutorials at *IEEE Energy Conversion Congress and Expo*, Milwaukee, US, in 2016, *Biannual Postgraduate Conference*, Cambridge University, UK, in 2018, *IEEE eGrid Workshop*, Charleston, SC, US, in 2018, and *IEEE Workshop on Power Electronics for Grid Dynamics*, Imperial College, London, UK, in 2019.

Professional Service

Dr. Zhang was Associate Editor for *IEEE Transactions on Power Electronics*, an AdCom member of the IEEE Power Electronics Society; has been a reviewer and session organizer for multiple journals and conferences; and has been a member of several IEEE and non-IEEE standardization working groups. He is a Fellow of IEEE for his technical leadership in the development of high-power electronics. He served as Chairman of the Board of Directors for Powerex – a US power semiconductor company, and served as Chair and Co-Chair on the Industrial Advisory Board for CPES for the last 16 years.

Next – Power Conversion for Electrified Green Infrastructure

Written by Richard Zhang

"What's Next?" – that's probably the most critical and most difficult question that every engineer/researcher and every technology and business leader ask themselves at least once a year in their strategic and operational planning sessions. After 22 years in the industry, what lured me back to CPES is the chance to face this question almost every single day and the unique position that CPES is in to answer it. And THAT IS EXCITING!

Before talking about "What's Next?", it helps to first understand where we are. The growth of power electronics technologies has been truly amazing – in its scale, permeating every aspect of our lives and every corner of our society; in its capabilities, reaching 100 MW in medium-voltage solutions and beyond 2-10 GW in high-voltage solutions; in its performance and intelligence, reaching unprecedented switching speed and power density, more intelligent control and fast communication delivering sophisticated functionalities and reliability. On top of all that, those have been achieved with a steady and fast cost-reduction curve.

When one tries to figure out "What's Next?," there is no better place than standing at the forefront of the challenges that the industry and society face. CPES has earned its world-renowned reputation of research eminence as the result of solving the toughest technical challenges that the industries faced – for example, the innovative circuits and controls that enabled the IT industry and More-Electric-Aircraft/Ship. It is ingrained in CPES's genes to step up to the upcoming technology challenges that need to be overcome to transform the industries.

From time to time, many of us may feel that the room for innovation became limited – all switching devices, circuit topologies, and control methods have been invented, the rest is for the industries to reduce cost. Fortunately, we are living in a time that couldn't be more diametrically opposed to that. We are besieged by needs for technology disruption – and that is GREAT for researchers and companies seeking opportunities for disruption in the marketplace.

Electrified Green Infrastructure!

If I need to pick one phrase to capture the tsunami of demands for technology disruptions, that's probably it. What's at the center stage of that tsunami of demands is Power Conversion – as researchers in the field of power electronics, we love it! You don't need to look far …

- Net zero-carbon emission goals set by governments around the world
- Penetration of renewable energy such as wind and solar in the past 20 years has reached a point that they are no longer a small niche player on the grid, but a critical energy source that provides double-digits of total electricity that we consume today
- Plans are being studied to provide 70 % of total electric energy and instantaneously 100 % of power level by clean energy on the grid. A revolutionary change is on the horizon at the power transmission level
- The fast growth of EV calls for another transformational change on the power distribution network

The grid will move from the current Grid 2.0 with augmented intelligence, where modern computing, sensing, and monitoring technologies were added to the 140-years-old, passive-components-dominated grid, to a new phase of Grid 3.0 with embedded intelligence through power electronics and ML/AI technologies. Unprecedented controllability and functionalities can be made possible to enable the increasingly complex grid with higher reliability and resilience. The Electrified Green Infrastructure is not just about the grid, but also innovations involving power conversion for EV fast-charging stations, H2 production, and utility-scale energy storage integration.

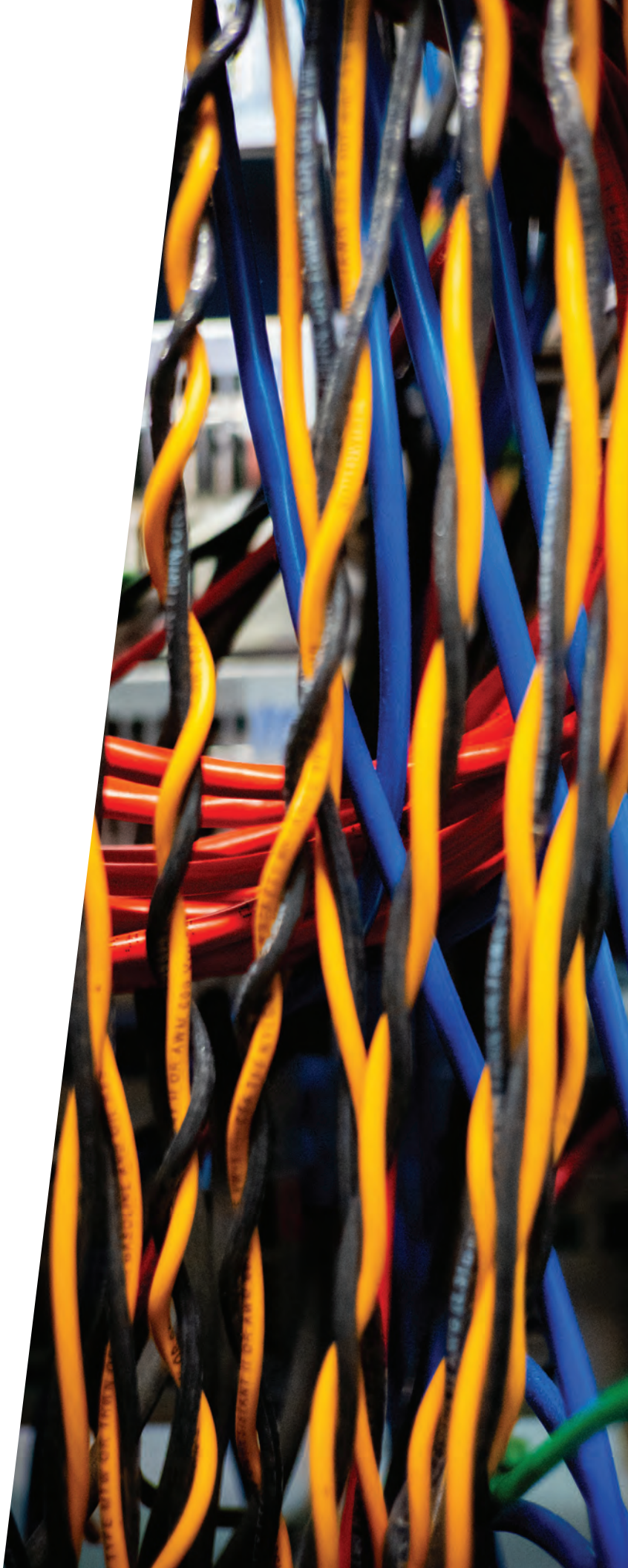
It's not like we just see this coming now. However, never before have we seen the scale and urgency of the technology challenges being felt so strongly by so many industries and countries. Jointly they start to scream the same needs – Power Conversion for the Electrified Green Infrastructure.

We have seen the dynamics for a while. And for a good reason, we have treated those challenges with the "making new look like old" approach – power electronics-enabled renewables were felt almost like a beast to be tamed and tolerated; yes, they provide clean energy we like, but they are also fluctuating in nature and could be a risky source to destabilize the grid. The concerns are real, especially when we insist on those new energy resources and loads to behave like 140-years-old components that we are familiar with. Facing the ever-accelerated penetration of renewables and EV, no wonder a consistent and loud voice from CEOs in the industry has been "we are operating now beyond science." Well, I believe we are still within the realm of science, but I do resonate strongly with the feeling that craves for new solutions and new approaches.

We have played the game of "making new look like old" long enough. To move forward, perhaps it helps to take a different approach and thinking. Edison and Tesla built the grid that we have today based on what they knew 140 years ago. It's probably a safe bet that if they were alive today and knew about the modern power electronics technologies, they would build a totally different grid and other infrastructure to go with it.

When I worked in the industry, I always asked my teams to have "Feet on the Ground, and Eyes into the Sky." Feet-on-the-ground to keep a sharp focus on execution to deliver market-winning products, Eyes-into-the Sky to never stop dreaming and building the future for the business. Coming to academia, I'd like to flip that statement as "Eyes into the Sky, and Feet on the Ground" – constantly looking out for new and disruptive approaches to solve the technical challenges that truly matter to the industry.

As always in CPES, I hope there are plenty of partners in industry and government resonating with the direction and are interested in creating the solutions together to build the Electrified Green Infrastructure with Power Conversion.



Yuhao Zhang Receives NSF CAREER Award to Develop New Generation of Power Devices for Electric Vehicles, Data Centers, and Renewable Energy Processing

Written by Barbara L. Micale

Yuhao Zhang, assistant professor at the Center for Power Electronics Systems (CPES) in the Bradley Department of Electrical and Computer Engineering, has received a National Science Foundation CAREER Award to develop a new generation of medium-voltage power devices that will enable advancement in the performance, frequency, efficiency, and form factor of the power electronic systems in electric vehicles, among other applications.

"Currently, many medium-voltage power electronics systems provide only about 70 percent efficiency; 30 percent of energy is lost in power conversion," Zhang said. "By monolithically integrating a power device and an integrated circuit into the same chip, we will be able to significantly increase efficiency."

Zhang's research is particularly timely in support of an auto industry striving to meet the challenges of climate change. In August, President Joe Biden signed an executive order to encourage more sales of electric cars, and some automakers announced their shared aspiration to achieve sales of 40 to 50 percent of annual US volumes of electric vehicles (battery electric, fuel cell, and plug-in hybrid vehicles) by 2030 in order to move the nation closer to a zero-emissions future consistent with Paris climate goals.

As consumers move to electric cars, the demand for smaller, lighter-weight, and higher-efficiency powertrain systems will increase, Zhang said, and these new powertrain systems will make improved energy efficiency possible in electric vehicles. Zhang estimates that the power devices he is developing can ultimately enable a significantly higher range in electric cars like the Tesla.

"We also believe that we can increase performance at a lower cost – a benefit to automakers, and, ultimately, the consumer," Zhang said.

"From an academic perspective, the interdisciplinary nature of this project allows significant intellectual merits in materials, devices, processing technologies, and power modules," he said.

Data centers in Google, Facebook, and Amazon as well as other entities like solar and wind power plants that rely on how electricity is converted will also benefit from these new power electronic devices.

To create a new generation of medium-voltage power devices, Zhang and his team will focus on understanding the fundamental leakage current and breakdown physics in vertical gallium nitride devices on silicon substrates; probe new device designs and functional structures for vertical and lateral gallium nitride FinFETs; develop innovative epitaxial structure and processing technologies for monolithic integration; and explore advanced device simulation and modeling that account for material non-idealities (defects and traps), and circuit dynamics.

> *"In all of these undertakings, we are putting particular emphasis on advising under-represented and minority students"*
>
> *Yuaho Zang, Assistant Professor, CPES*

The CAREER award is the National Science Foundation's most prestigious award for early-career faculty with the potential to serve as academic role models in research and education, and to lead advances in the mission of their organization, as stated by NSF.

CAREER awardees are also required to find ways to integrate education and research, and to conduct outreach.

Assistant Professor Yuhao Zhang and his graduate students.

To address these components, Zhang is establishing a unique research program in collaboration with the Major Design Experience program that will train undergraduate students in technical, research, and professional skills and allow them the opportunity to tackle interdisciplinary problems in the fields of materials, devices, and power electronics.

"Mentoring is an important part of the program," he said. "Leveraging the substantial resources at the Center for Power Electronics Systems, we will facilitate student interactions with our collaborators in the power semiconductor industries."

Results of Zhang's research will also be integrated into graduate-level course curriculum. "One of our goals is to develop and promote power semiconductor education materials to help maintain the U. S. power semiconductor workforce," he said.

Outreach efforts will also include involvement in pre-college summer camps and provide summer research opportunities to K-12 students and teachers that encourage their participation in microelectronics and power electronics research.

"In all of these undertakings, we are putting particular emphasis on advising under-represented and minority students," Zhang said.

TechGirls' Power Electronics Experience

Every day, for two weeks in July, 27 young women from around the world came together virtually to learn about power electronics.

CPES Assistant Professor Christina DiMarino organized the course, which included classroom-style lectures and technology demonstrations with help from many CPES students and faculty, facilitated by the Student Council.

Dr. DiMarino's course, "Power Electronics for a Sustainable Future," highlighted power electronics as a key enabling technology for the electrical and electronics industry, with applications ranging from consumer and portable electronics and electric vehicles to renewable energy and electrification of rural and developing regions. TechGirls participants learned about electrical circuits, power electronics converters, and circuit simulation tools.

CPES was the perfect organization to provide this experience, with its focus on hands-on learning and creating innovative power electronics solutions for society.

"TechGirls is supposed to be an in-person experience," said DiMarino. "To provide an engaging virtual experience, we developed a series of pre-recorded videos with lectures, simulation exercises, and hardware demonstrations, and live group design challenges that enabled students to apply what they learned."

Dr. Christina DiMarino

TECH Girls

TechGirls is a U.S. Department of State initiative and exchange program designed to inspire young women from the Middle East, North Africa, Central Asia, and the U.S. to pursue higher education and careers in technology through hands-on skills development. It is administered by Legacy International in partnership with Virginia Tech's Center for Enhancement of Engineering Diversity.

In less than 10 years, the TechGirls program has helped 238 young women prepare to be the next generation of women leaders in science, technology, engineering, and mathematics. The TechGirls program offers a rich cultural immersion experience, improves the participants' ability to enter tech fields, and encourages them to pursue higher education in fields where women are under-represented.

Overall program goals include:

- Improving participants' ability to enter tech fields and gain access to higher education
- Increasing participants' skills and knowledge in current technologies
- Connecting and supporting the next generation of women STEM leaders

Rolando Burgos, CPES Director, states, "CPES strongly supports efforts to make STEM education available around the world, and we strive to increase underrepresented groups in power electronics. TechGirls is important because it helps on both counts, and we hope it will help continue strong female participation within CPES."

"This has been a tremendous experience," says DiMarino. "These young women were truly inspiring – so positive, excited, and motivated to learn."

Vladimir Mitrovic, on guitar, and Marija Grove, vocals, entertain at the CPES Summer Party.

CPES Student Council Report

The past year saw a variety of changes to the CPES student experience, resulting from the continued growth of CPES and the lingering impacts of the pandemic. The Student Council also took steps to add back fun events and bring enhanced learning opportunities to the students.

To better serve students in the growing CPES lab in the National Capital Region (NCR), the CPES Student Council expanded to a total of ten members with two located in Arlington, Virginia. The larger CPES Student Council focused on facilitating collaborative efforts between the two CPES campuses in regards to research and improving overall quality of life.

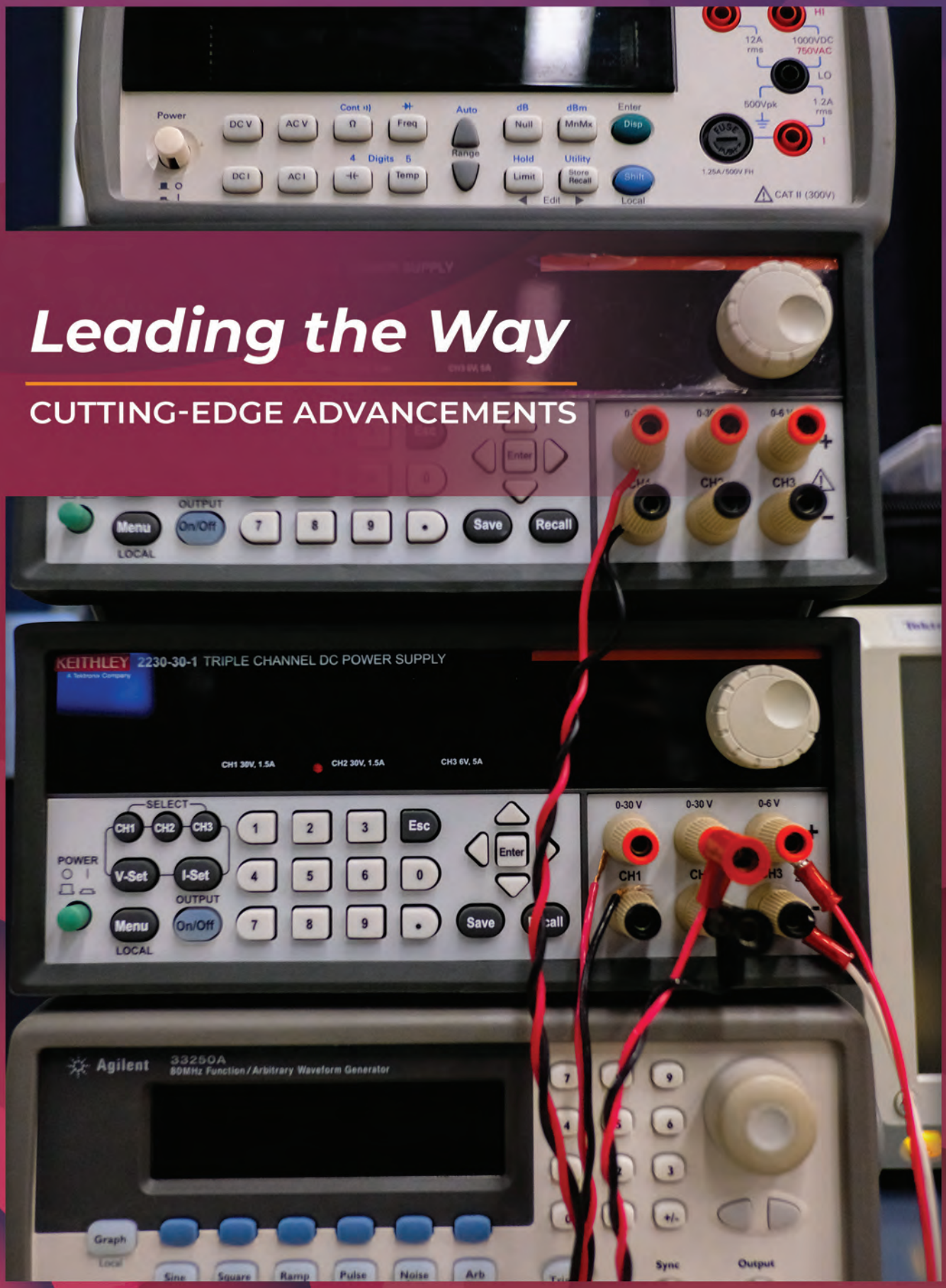
Throughout 2021, the Student Council worked closely with CPES faculty to communicate, quickly and accurately, information on pandemic developments, e.g., Virginia Tech guidelines on COVID testing and vaccinations. Through these efforts, CPES researchers were able to safely return to work in a manner reminiscent of the pre-COVID days. As the pandemic evolves, the CPES Student Council continues its work in keeping the student body up to date with the latest information.

In July 2021 the Student Council planned and hosted the CPES Summer Party – a day of fun and relaxation at the Beliveau Farm Winery to celebrate the Center's commitment to high-level research while navigating the challenges of the global pandemic safely.

The Student Council also organized student involvement in the TechGirls program. Led by Dr. Christina DiMarino, CPES students helped develop course material, lead lectures, and virtually interact with high school women from the U.S., Middle East, North Africa, and Central Asia as they learned about power electronics and the energy needs of the 21st century.

The CPES Student Council continues to organize a weekly seminar for students where they present and discuss research with their peers. Over the last year, we added presentations from industry partners with the goal of broadening students' view of the power electronics industry and educating ourselves on the needs and challenges of our partners. Dr. Sungjae Ohn from Tesla detailed his company's product ecosystem while Dr. Mona Ebish from the Navy Research Laboratory shared new advances in the semiconductor industry.

The CPES Student Council are looking forward to even more opportunities to build comraderie among our colleagues in the upcoming year.



Leading the Way

CUTTING-EDGE ADVANCEMENTS

A Phone-Sized 3 kW DC-DC LLC Module With Low Loss PCB-Based Matrix Inductor for 48 V Power Architecture for Data Centers

The use of cloud computing services is surging at a rapid rate. These trends are a motivation to improve the cost efficiencies of building data centers, either by reducing initial construction cost or increasing Power Usage Effectiveness (PUE) to reduce running costs. In this work, the proposed DC-DC module is targeting the latest new narrow range 48 V bus architecture as shown in Fig. 1. The interest in 48 V architecture is building up recently to leverage the high efficiency in power delivery. Multiple state-of-art solutions have been introduced for the 3 kW datacenter power supplies. The efficiency is ranging from 96%-98% and power density less than 50 W/in^3 as shown in Figure. 2. A common in challenge in the available high-efficiency solutions is the high cost dure to high design complexity.

In this work, high efficiency and low-profile design are proposed for the 48 V LLC converter for the data center. The converter utilizes PCB magnetics for better thermal management, easy assembly, and lower cost. However, there are three main challenges to PCB magnetics: 1. High AC Loss in the transformer, 2. high thermal stress in PCB specially in PCB-based inductor, and 3. EMI due to high interwinding capacitance. The matrix transformer is optimized through multiple aspects like number of elemental transformers, transformer turns number, and operating frequency.

The matrix inductor concept is presented to reduce PCB inductor winding loss and reduce thermal stress on PCB. The matrix inductor concept helps to avoid the extreme increase in ac resistance due to the MMF build-up by lateral distribution of the stacked layers. Finally, the converter is integrated on 6-layer PCB, featuring two shielding layers to block EMI noise from input to output.

The converter achieves **98.8 % efficiency and 600 W/in^3 power density**. The converter has an extremely low profile of < 11 mm and can fit within a smart phone size. The low-profile design reduces the PCB-to-air thermal resistance and facilitates thermal management.

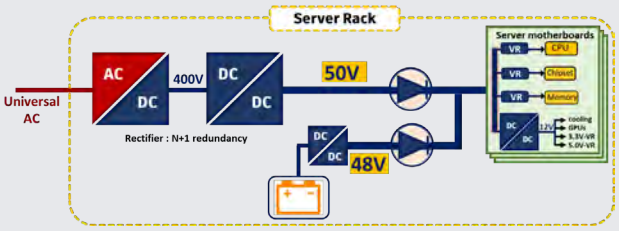


Fig. 1. Narrow range 48 V bus for efficient data centers' power delivery.

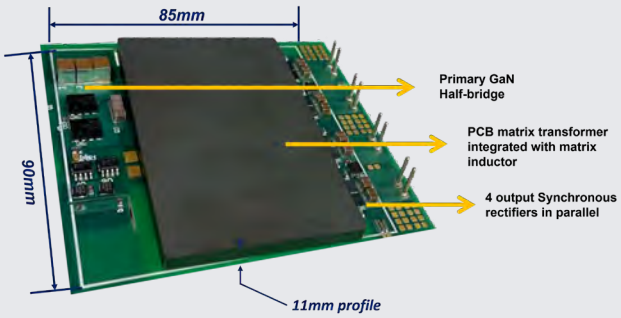


Fig. 3. Hardware prototype of 400 V- 48 V 300 kHz LLC with integrated PCB magnetics. The converter features low profile and is about the same size as iPhone 13.

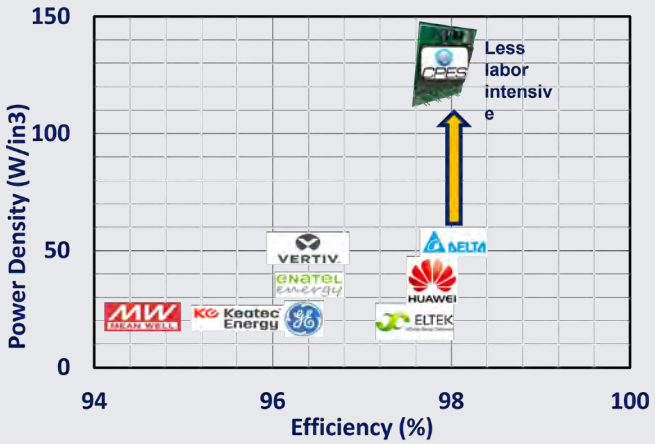


Fig. 2. Road map of 3 kW datacenter power supply units. CPES All-PCB solution presents 3x higher power density with less cost and same efficiency.

Closing the Gap Between High-Density and High-Voltage in Multi-Die Power Modules With 10 kV SiC MOSFETs

The longstanding trend of miniaturization in low-power converters prompted by the commoditization of consumer electronics has extended into the kilovolt level over the past decade. The broadening focus is motivated by new applications for dense, medium-voltage power conversion such as rugged dc microgrids aboard military and commercial vessels, efficient grid-tie converters for renewable energy sources, and reliable supplies for high-voltage ion thrusters used in deep space exploration. These applications require high-density, high-voltage power conversion that extends beyond the capabilities of conventional silicon technologies, with a need for ruggedness and efficiency, without compromising on cost.

Medium-voltage silicon-carbide (SiC) MOSFETs have emerged to meet this need, promising lower losses, higher operating temperatures, and faster switching speeds as a means to improving the density of power converters for these cutting-edge applications. To take advantage of SiC devices, packaging technology must evolve as well. Innovative, high-voltage packages, such as the 10 kV, 50 A SiC MOSFET package in Fig. 1, are developed to unlock the potential of medium-voltage SiC devices and broaden their appeal to designers of state-of-the-art conversion systems.

A range of innovative electrical, material, and manufacturing technologies are required to meet this goal. Nano-silver sintering replaces conventional solder bonds, reducing thermal resistance and improving thermomechanical ruggedness, allowing for higher device temperatures and larger temperature swings during operation. Molybdenum posts make the electrical connection to the SiC MOSFET in lieu of wirebonds, lowering stray inductance and providing an additional heat path from the die to the top of the package. To improve power density, beryllium-copper spring-pins replace bulky bolt-on terminals. The module housing and a PCB busbar fully enclose the pins, breaking the in-air path between the terminals, and enabling 7 mm spacing without violating creepage requirements. The result is an innovative, 10 kV SiC MOSFET package that provides the thermomechanical ruggedness, high-temperature operation, and compact form factor required by modern applications (Fig. 2) while preserving the advantages of medium-voltage SiC over conventional silicon technology.

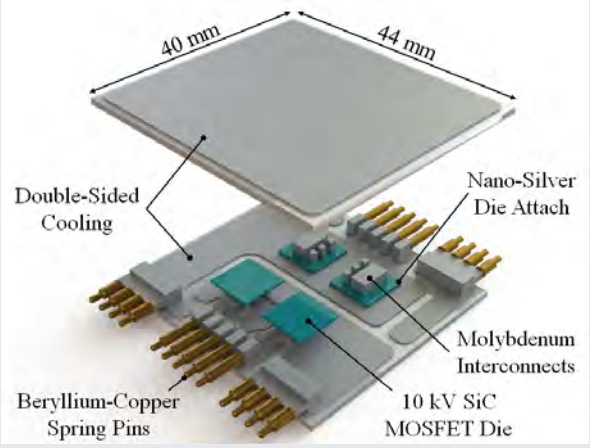


Fig. 1. 10 kV, 50 A SiC MOSFET phase-leg package with double-sided cooling, molybdenum post interconnects, and lateral spring-pin terminals.

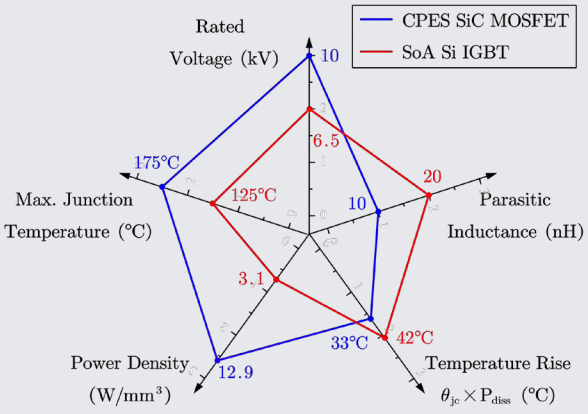


Fig. 2. Comparison between the proposed 10 kV SiC MOSFET package and state-of-the-art 6.5 kV silicon IGBT technology.

10 kV GaN Diodes and Transistors Beyond SiC Limit

Power semiconductor devices with low on-resistance (R_{ON}), high-switching speed, and high-breakdown voltage (BV) are central to improving the efficiency of electrical energy processing in many applications. Medium-voltage (MV) power devices (also referred to high-voltage in many contexts) are ubiquitously used in electricity grid, renewable energy processing, industrial motor drives, and electrified transportation. Today's MV power device market is dominated by bipolar Si IGBTs and p-n diodes up to 6.5 kV. However, they suffer from a slow-switching speed due to the poor reverse recovery. A set of superior alternatives that allow fast switching is the unipolar SiC MOSFET and junction Schottky barrier (JBS) diode. These SiC devices have been recently pre-commercialized up to 10 kV by a few vendors and used in R&D power applications.

GaN has superior power semiconductor properties over SiC and Si. Lateral GaN high-electron mobility transistors (HEMTs) have been commercialized up to 650 V, and industrial vertical GaN transistors have been demonstrated at the 1.2 kV class. A few GaN devices have been demonstrated with BV close to 10 kV, but their specific R_{ON} are higher than SiC counterparts. This has led to a common belief that GaN is only advantageous in the low-voltage range.

Recently, the Zhang group at CPES has developed a new generation of MV devices based on the multi-channel AlGaN/GaN platform with performance superior to the SiC and Si counterparts. The multi-channel GaN device offers the combination of a high mobility in a two-dimensional electron gas (2DEG) channel and a high-power handling capability enabled by the stacked channels. The multi-channel lateral device also leverages some benefits of vertical devices, e.g., spatially distributed current. To fully exploit these material properties, a series of new device designs has been proposed to enable robust termination, distributed electric field (E-field), and normally-OFF operation. These designs have enabled demonstration of 10 kV GaN Schottky barrier diodes (SBDs) and normally-OFF HEMTs with a R_{ON}~BV trade-off beyond the 1-D SiC unipolar limit.

These works have achieved wide impacts, as they can potentially change the landscape of high-voltage power semiconductors and power electronics. They have been covered by media globally including *Nature Electronics* and *Semiconductor Today*. The PI has been invited to deliver over seven talks to introduce these works.

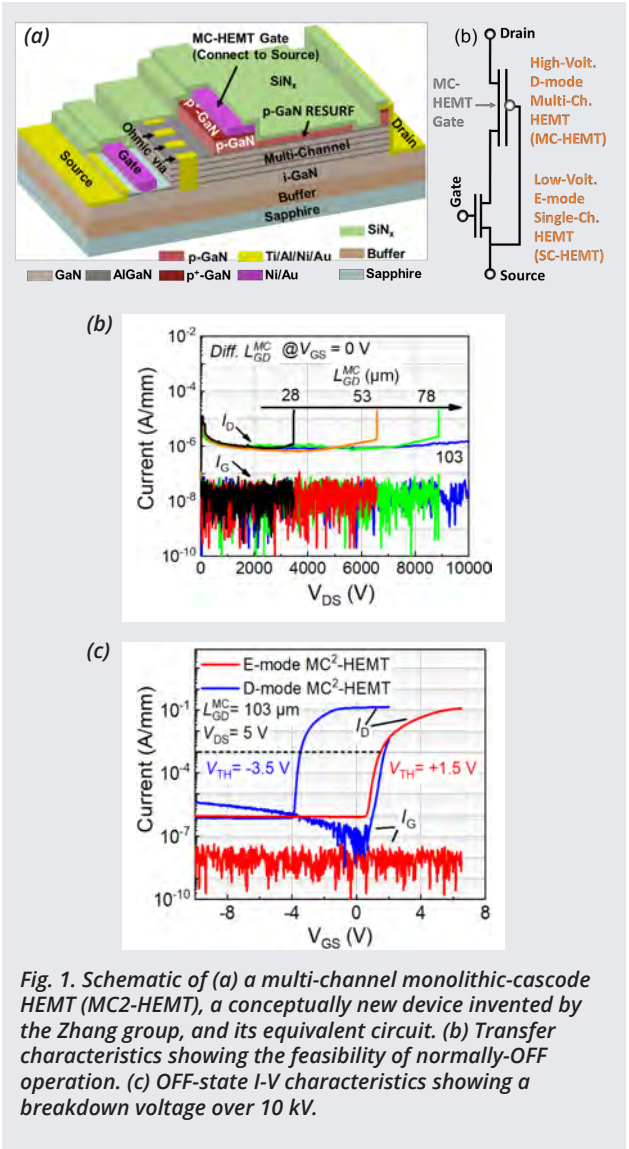


Fig. 1. Schematic of (a) a multi-channel monolithic-cascode HEMT (MC2-HEMT), a conceptually new device invented by the Zhang group, and its equivalent circuit. (b) Transfer characteristics showing the feasibility of normally-OFF operation. (c) OFF-state I-V characteristics showing a breakdown voltage over 10 kV.

10 kV SiC MOSFET-Based Modular, Scalable, High-Power Density, Converter for Medium-Voltage Applications

Medium-voltage (MV) Si-based converters are widely used in MV applications such as motor drives, renewable energy integration, ship-to-shore connections, and uninterrupted power supplies, among others. These converters, however, exhibit low-power density (< 1 MW/m^3) and efficiencies in the 97–98 % range, which limits their applicability and power-processing capacity. The development of 10 kV SiC MOSFETs, with the advanced properties of this type of wide-bandgap (WBG) semiconductor, has revolutionized the possibilities that power electronics bring in these MV applications, primarily thanks to the vastly improved design space that they offer.

CPES, under the sponsorship of ARPA-E, the Office of Naval Research (ONR), and its WBG high-power converters and systems (WBG-HPCS) mini-consortium, has worked over the past several years in the development of circuit topologies, advanced controls, and several fundamental technologies, to make possible the development of MV converters based on 10 kV SiC MOSFET devices. Its main effort has targeted modular multi-level converter (MMC)-type circuits that can fully exploit the properties of these devices by adopting switching-cycle controls. The MMC is comprised of phase-arms and phase-legs that use series-connected power cells to scale the dc-bus voltage, operating in voltage-source converter (VSC) mode. Fig. 1 shows the half-bridge power cell developed at CPES using 10 kV SiC MOSFETs, rated at 6 kV dc and 84 A rms, while Fig. 2 shows an MMC in full-bridge configuration built with these power cells. This converter is rated at 18 kV, 1.5 MW, uses 6 power cells per phase-leg (three per arm), and is capable of operating in both dc-ac and dc-dc power conversion modes.

The power-cell developed attained a power density of 12 kW/l and an efficiency of 99.4 % switching at 10 kHz. To attain this performance CPES had to develop several key technologies, including: 1) FPGA-controlled enhanced gate drivers designed to have high driving currents (90 A), low gate-loop inductances (< 5 nH), high common mode (CM) transient immunity (>100 V/ns), a Rogowski coil current sensor used for short-circuit protection and high-bandwidth current control, and a fiberoptic communication link to the local digital controller; 2) PCB-based planar dc-bus with a loop inductance of 12.1 nH, and a partial discharge inception voltage (PDIV) > 10 kV; 3) auxiliary power network architecture built around a wireless power transfer unit rated at 120 W, 30 kV insulation, and a coupling capacitance of 2.8 pF, and a current-transformer (CT) based secondary unit rated at 100 W, 5 kV insulation, and a coupling capacitance of 1.86 pF to distribute power to all ancillary circuitry; 4) digital-interface sensors with fiber-optic communications; and 5) a local FPGA-controlled digital controller running an internal power cell communication network (gate drivers, sensors, ancillary circuitry), and a converter-level communication network, both featuring sub-nanosecond synchronization among all components and a 5 Gbps data rate.

To date, the converter has been tested using two novel control methods; namely Switching Cycle Control (SCC) that shapes the arm currents to achieve switching cycle

Fig. 1. Half-bridge power cell based on 10 kV SiC MOSFET devices.

balance of the power cell capacitor voltages, and the Integrated-Capacitor-Blocked-Transistor (ICBT), which reverses the power flow in a power cell so that most of the power is transferred directly from the input to the output without affecting its capacitor voltages. Both control methods eliminate the line frequency dependence on the power cell capacitor voltage, and decrease the capacitive energy storage needed by an order of magnitude compared to state-of-the-art MMC converters. This unit is currently undergoing tests, and has demonstrated an efficiency of 99.2 % while limiting the power cell voltage ripple to 1.2 % of the rated voltage, and using a 32.5 μF MV capacitor. Over the coming months, CPES will increase the operating voltage to 24 kV using four power cells per arm (8 per phase-leg).

Fig. 2. Full-bridge 18 kV, 1.5 MW converter setup with 12 power cells.

Terminal Behavioral Modeling of Electric Machines for Real-Time Emulation, System-Level Analyses, and Stability Studies

According to the International Energy Agency, around half of the electricity used globally is consumed by electric motors. Moreover, the growth in the electrical vehicle industry will increase their application even further. The development of high-fidelity models of electric machines for real-time emulation, system-level analyses, and stability studies together stand out as an important and needed research focus. New modeling concepts that go beyond the standard industry practice can aid with this effort.

Aligned with this trend, CPES is currently assessing a possibility to model electric machines, namely permanent magnet synchronous machines (PMSM) using small-signal, terminal-behavioral, three-port networks. Having such behavioral models of the machine available provides many opportunities for system integrators, and even enables an *in-situ* system observation and stability assessment at both the machine's electrical and mechanical interfaces. This capability can undoubtedly be of high importance in practice, as it is offering new insights into dynamic interactions of the mechanical system, the governor/turbine control design in ships, aircrafts, and even large synchronous machines in power plants.

To obtain a terminal behavioral model of an electric machine, it is required to introduce small-signal perturbations – current or voltage at the electrical interface, and torque or speed at the mechanical interface. This procedure would characterize the machine at one operating point since this is a small-signal characterization that leads to a small-signal model; however, the machine can be characterized at numerous operating points where non-linear effects like saturation can be captured assuming the Wiener-Hammerstein model structure that combines non-linear static and linear dynamic.

This modeling methodology has been under development for a 3 HP permanent magnet machine, which is mechanically coupled with an induction machine of the same power level, the latter serving as a perturbation source at the mechanical interface. The methodology requires accurate torque, position, voltage, and current sensors. A so-called characterization testbed has been built that combines hardware-in-the-loop (HIL) and power-hardware-in-the-loop (PHIL) environment, together with sensor-interface boards that are used to properly scale measured signals for machine control. The frequency-response analyzer is used to sweep the machine at different operating points by perturbing the reference signal within machine control running in PHIL and reading *d-q* currents, voltages, torque, and speed variables whose dynamic ratios are then obtained in-situ. The developed procedure further allows standard machine parameters to be calculated out from the measured frequency responses at all operating points of interest, enabling higher-fidelity models than those obtained using standstill IEEE test procedures commonly used in practice today.

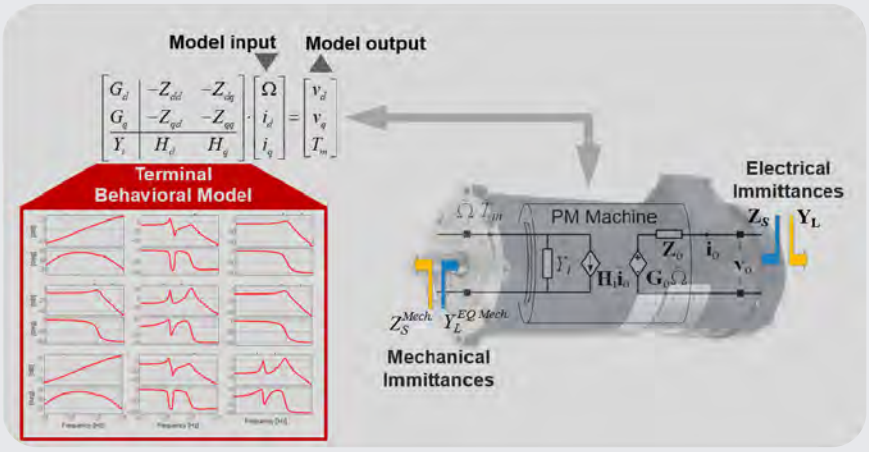


Fig. 1. TBM study for a permanent magnet synchronous machine.

Modular Ultra-High-Density Power Electronics Interrupter With 12 kV 1 kA Breaking Capability for MVDC Hybrid DC Circuit Breaker

MVDC Circuit Breaker is a crucial component in the imminent MVDC system for various applications, like MV charging station, dc power delivery in aircraft and ships. Both solid-state and hybrid DC circuit breakers need a power electronic interrupter (PEI) to interrupt the fast-rising dc fault current while containing the inductive energy to secure arc-less breaking operation. For instance, the hybrid circuit breaker (HCB) in Fig. 1(a) shows the location of PEI.

The conventional customized PEI solution suffers a very bulky volume and high cost to house MV IGBT modules as shown in Fig. 1(a), gate-drivers, energy absorption component. In addition, the existent PEI has a limited breaking voltage due to lack of robust MV-insulated aux-power solutions. CPES proposed a modular-based PEI concept that MV is achieved by stacking identical LV PEI-cells using large-volume, low-cost discrete IGBT devices. Paralleled discrete IGBTs in each PEI-cell are capable of breaking over 1 kA current. As shown in Fig. 1(b), the integration of nine modules with 12 kV 1 kA breaking capability demonstrates a very high-power density of 7.4 kW/cm^3, much higher than the module-based design. The proposed cascaded gate-driver power supply and single 20 kV-insulated MHz auxiliary power supply architecture enables flexible MV voltage ratings to tens of kV.

In addition, a staged turn-off strategy is proposed, which not only reduces the total MOV energy and clearing time, but also improves the MOV energy balance and average lifetime. The experimental results shown in Fig. 2 validate the current interruption function of designed PEI. With the good scalability, the PEI concept and the HCB architecture show great potential in the MV dc distribution system and even higher voltage applications.

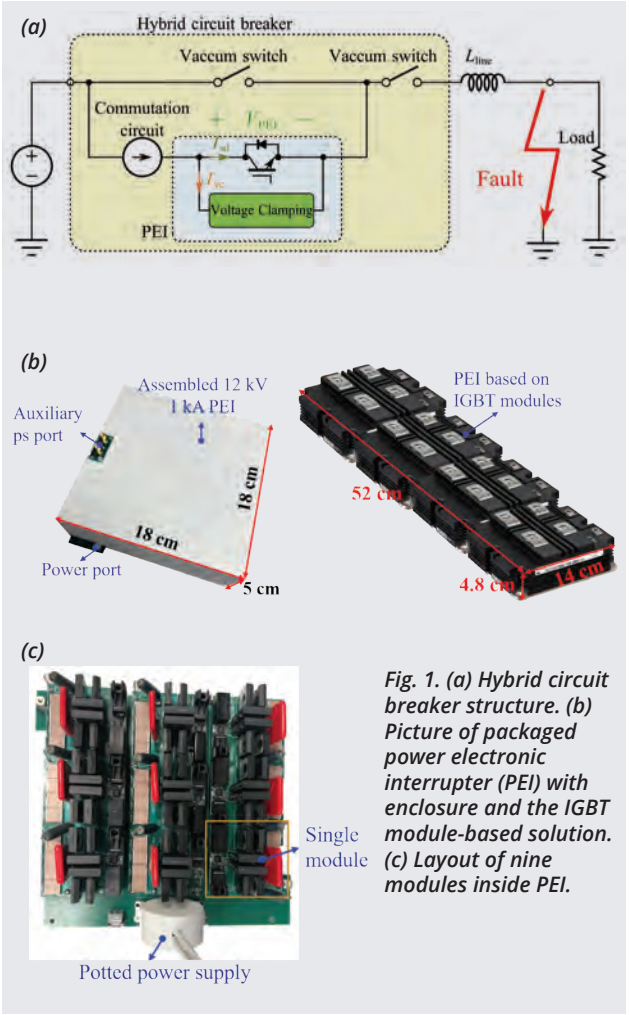


Fig. 1. (a) Hybrid circuit breaker structure. (b) Picture of packaged power electronic interrupter (PEI) with enclosure and the IGBT module-based solution. (c) Layout of nine modules inside PEI.

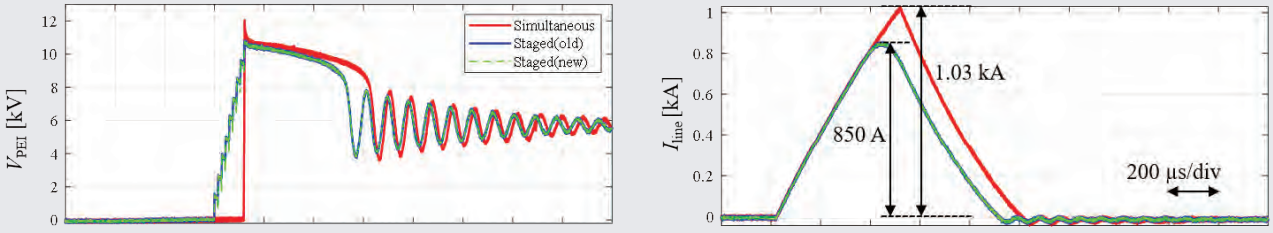


Fig. 2. Waveforms of PEI breaking 12 kV 1 kA with three turn-off strategies.

Center Overview

2021 DASHBOARD

Research

48
New Sponsored Research Projects

$7.1M
Research Expenditures

Industry Consortium

84 Consortium Members

$2.3M
Consortium Value

Education

191 Total
Since 1977

6 Ph.D. Degrees Awarded

198 Total
Since 1977

4 Master's Degrees Awarded

Intellectual Property

146 Total
Since 1977

3 U.S. Patents Awarded

12 U.S. Patent Applications Filed

Leading With Distinction

2

National Academy of Engineering Members

Dushan Boroyevich

Fred C. Lee

Election to National Academy of Engineering membership is one of the highest professional honors accorded an engineer.

5

IEEE Fellows

Dushan Boroyevich

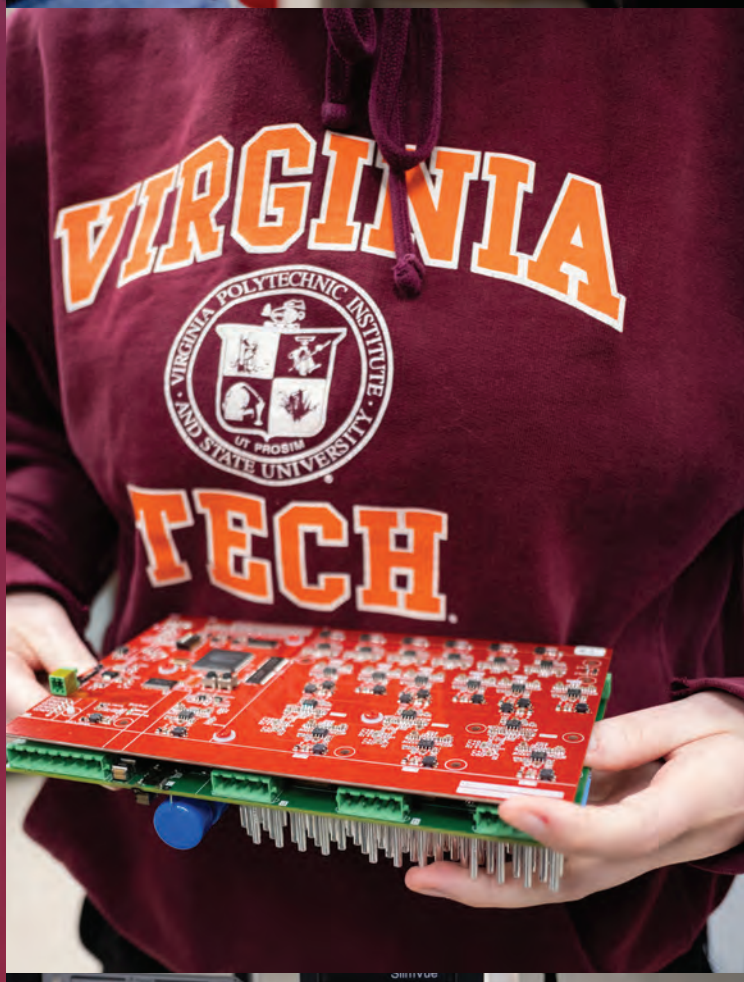
Fred C. Lee

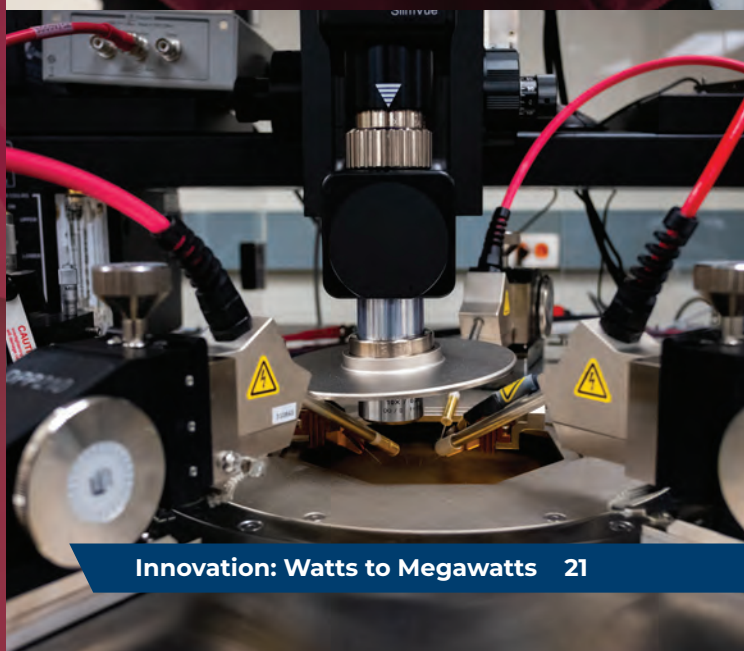
Guo-Quan Lu

Khai Ngo

Richard Zhang

IEEE Fellow is a distinction reserved for select members who have demonstrated extraordinary accomplishments in their field.





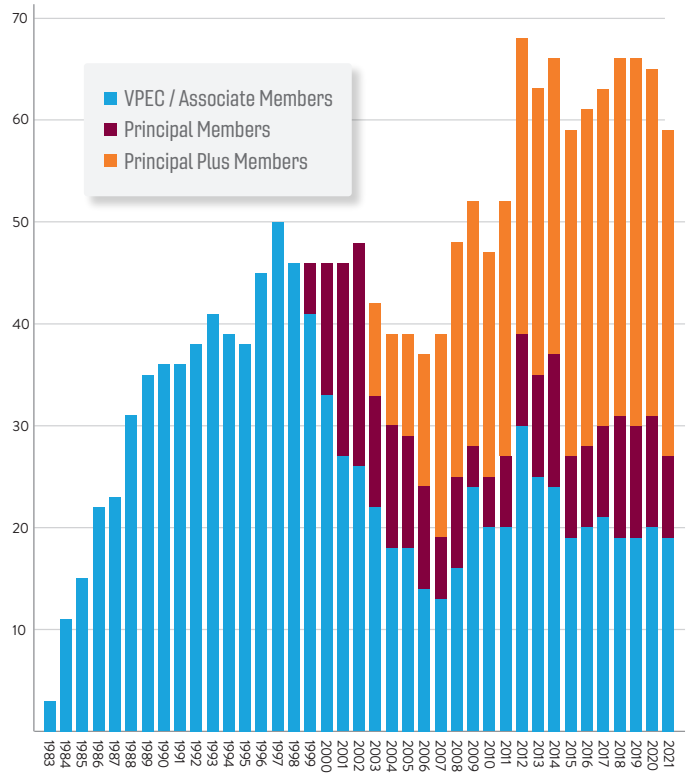
CPES Industry Consortium

The CPES industrial consortium is designed to cultivate connectivity among researchers in academia and industry, as well as create synergy within the network of industry members. It offers the ideal forum for networking with leading-edge companies and top-notch researchers and provides the best mechanism to stay abreast of technological developments in power electronics.

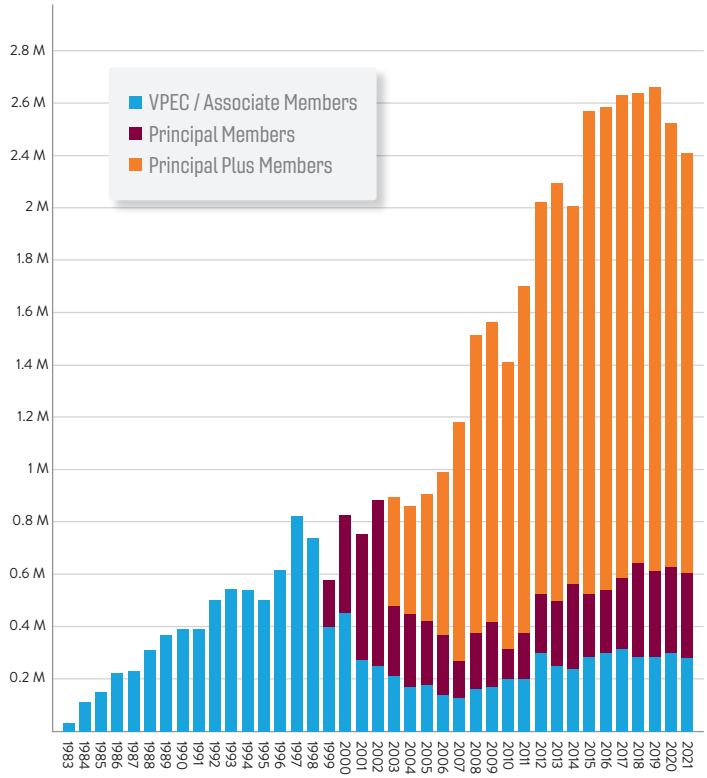
The CPES connection provides a competitive edge to industry members via:

- Complimentary registration for CPES Annual Conference
- Access to state-of-the-art facilities, faculty expertise, and top-notch students
- Leveraged research funding of more than $6 million per year
- Industry influence via Industry Advisory Board
- Intellectual properties with early access for Principal Plus and Principal members via CPES Intellectual Property Sharing Program
- Technology transfer made possible via special access to the Center's multidisciplinary team of researchers, and resulting publications, presentations, and intellectual properties
- Continuing education opportunities via professional short courses offered at a significant discount
- Option to send engineers to work with CPES researchers on campus via the Industry Residence Program

CPES Membership Company Growth



Industry Membership Funding Growth



Membership Structure

Principal Plus Members
Annual Contribution $50,000

Principal Plus Members gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research—PMC (Power Management Consortium), HDI (High Density Integration), or WBG-HPCS (Wide Bandgap High Power Converters & Systems). Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each. In addition to all the benefits offered to Principal and Associate Members, Principal Plus Members have easy access to cutting- edge IPs via the CPES IPPF (Intellectual Property Protection Fund), as well as interactive opportunities with CPES researchers via designated student contacts and mini-consortium reviews.

Principal Members
Annual Contribution $30,000

Principal Members are well positioned to influence and guide CPES as Industry Advisory Board (IAB) members. Principal Members also have cutting-edge IP advantage via automatic IPPF (Intellectual Property Protection Fund) membership, in addition to all the benefits offered to Associate Members.

Associate Members
Annual Contribution $15,000

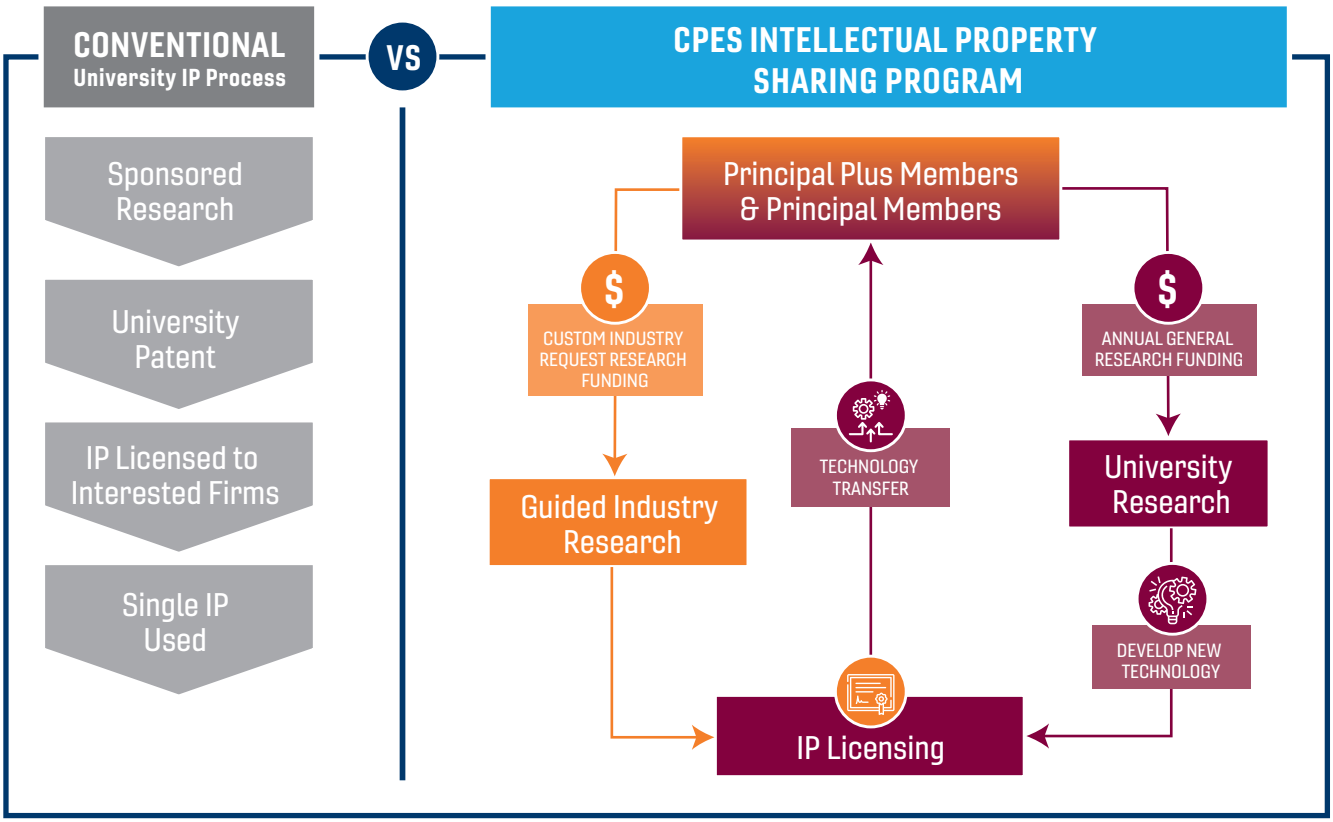
Associate Members gain a competitive edge, not only through easy access to CPES research results, researchers, and state-of-the-art facilities, but also opportunities for technical exchanges via the Industry Residence Program and continuing education via CPES short courses to stay abreast of new technologies. Companies participating in the Industry Residence Program must be actively engaged in collaborative research with the Center in technical areas that are of mutual interest, to be determined jointly with CPES faculty host.

Affiliate Members
Annual In-Kind Hardware/Software Donations Equal to or Less Than $15,000

Their contributions must be relevant to CPES research. Membership participation at this level requires approval of the Center Director.

Intellectual Property Sharing Program

CPES offers a unique IP access mechanism that provides extraordinary advantage, automatically and at no additional cost, to Principal Plus and Principal members. Members meet quarterly with inventors to discuss invention disclosures and jointly decide which technologies to protect, with patenting costs covered by the consortium. Once a technology is protected, current Principal and Principal Plus Members are granted a royalty-free, non-exclusive, non-transferable license to use the technology. IP Sharing is applicable only to technologies developed under the industry consortium by CPES/VT researchers.



CPES Members

Principal Plus Members

ABB Inc.
Analog Devices Inc.
Aurora Flight Sciences
Crane Aerospace & Electronics
CRRC Zhuzhou Institute Co., Ltd.
Delta Electronics Inc.
EnerSys
Ford Motor Company
GE Global Research / GE Aviation
GE Grid Solutions
Infineon Technologies AG
Innoscience (Zhuhai) Technology Co., Ltd.
Jiangsu Wanbang Dehe New Energy Technology Co., Ltd.
Joulwatt Technology
Lite-On Technology Corporation
Lockheed Martin Corporation
Moog Inc.
Murata Manufacturing Co., Ltd.
Navitas Semiconductor
NexGen Power Systems
Nissan Motor Co., Ltd.
NXP Semiconductors N.V.
Onsemi
OPPO
Panasonic Corporation
Powerland Technology Inc.
Raytheon Technologies
Rockwell Automation Inc.
Siemens Corporate Technology
Silergy Corporation
Texas Instruments
TMEIC Corporation
Vertiv
VisIC Technologies
Würth Elektronics
ZF Friedrichshafen AG

Principal Members

Carrier Corporation
Eaton Corporation
Flextronics
Mercedes-Benz R&D North America Inc.
NR Electric Co., Ltd.
Schneider Electric
SolarEdge Technologies, Inc.
Toshiba Corporation
ZTE Corporation

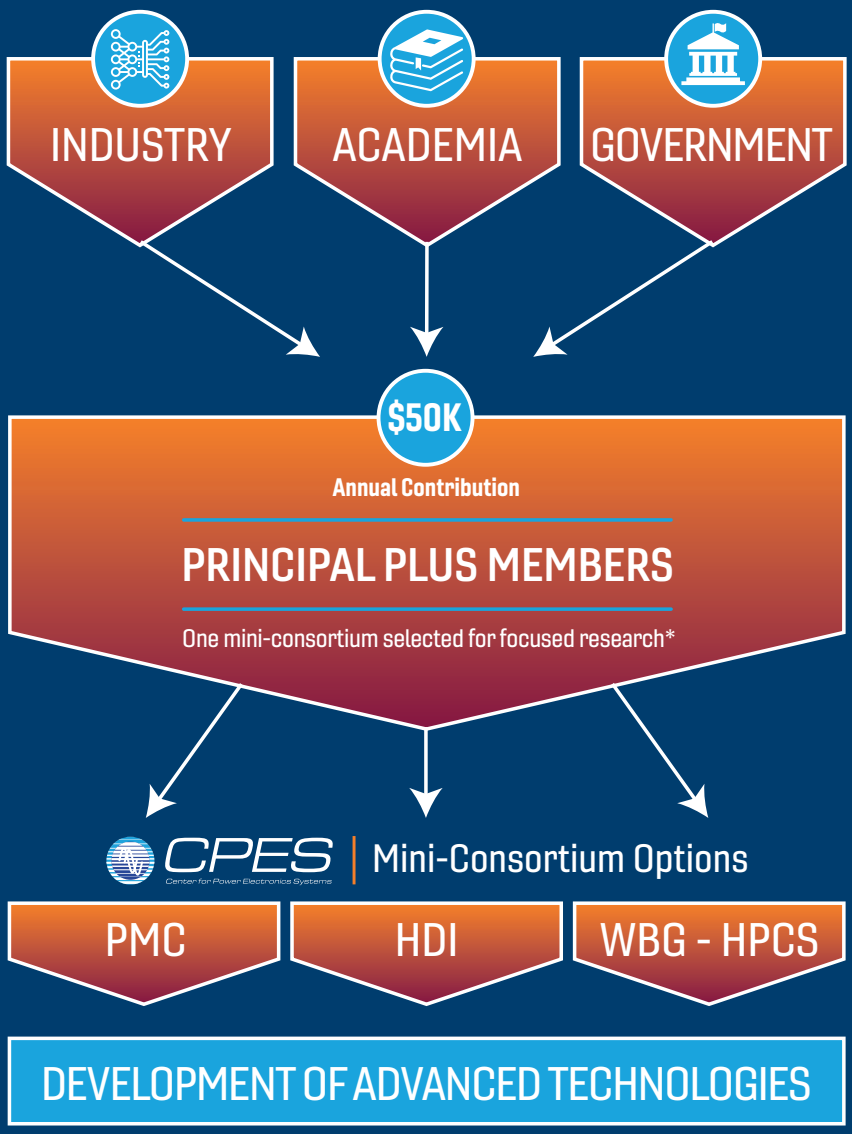
Associate Members

AcBel Polytech Inc.
Cummins Inc.
General Motors
Inventronics (Hangzhou) Inc.
Johnson Controls Inc.
Maxim Integrated
NuVolta Technologies
Richtek Technology Corporation
Robert Bosch GmbH
Safran
Shindengen Electric Mfg. Co., Ltd.
Sumitomo Electric Industries, Ltd.
Suzhou Inovance Technology Co., Ltd.
TBEA Xi'an Electric Technology Co., Ltd.
TDK-Lambda Corporation
Tesla Motors
Valeo

Affiliate Members

ANSYS Inc.
AT & S
Chicony Power Technology Co., Ltd.
Cissoid
Dowa Metaltech Co., Ltd.
Efficient Power Conversion
Egston Power Electronics GmbH
Electronic Concepts Inc.
Hitachi Metals
Mentor Graphics Corporation
Novel Crystal Technology
OPAL-RT Technologies
Plexim GmbH
Powersim Inc.
Silvaco
Simplis Technologies Inc.
Synopsys Inc.
Taiyo Yuden Co. Ltd.
Tektronix Inc.
Tokin Corporation
Transphorm Inc.
VPT Inc.

Mini-Consortium Program



*Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

The CPES mini-consortium program provides a unique forum for creating synergy among industries and defining new research directions to meet future industry needs. The formation of the mini-consortium allows CPES to pool resources and focus on developing pre-competitive technologies to address common challenges, and share the research results among mini-consortium members. Companies also benefit from enhanced opportunities to engage regularly and directly with CPES faculty and students through quarterly reviews.

Mini-consortium members are enrolled in CPES as Principal Plus Members, with annual contributions of $50,000. They gain tangible benefits via research collaboration with CPES as a member of one of the mini-consortia on focused research:

- Power Management Consortium (PMC)
- High Density Integration (HDI)
- Wide Bandgap High Power Converters and Systems (WBG-HPCS)

Companies interested in more than one focused research area may join another mini-consortium for an additional annual contribution of $50,000 each.

Power Management Consortium (PMC)

With ever-increasing current consumption and clock frequency, today's microprocessors are operating at very low voltage and continuously switching between the "sleep-mode" and "wake-up mode" up to tens of megahertz in order to conserve energy. This imposes a significant challenge to the power delivery and management and was perceived as a road block for further processor development.

In 1997, at the request of Intel, CPES established a voltage regulator module (VRM) mini-consortium to address the issue of power management for the next generation of Pentium processors. The CPES the team developed a multi-phase voltage regulator (VR) module architecture and implementation and it was immediately adopted by industry. The scope of VRM research encompasses power delivery architecture, modularity and scalability, control and sensing, current sharing, integrated magnetics, advanced packaging and integration. In these respects, over 30 US patents awarded. The developed power architecture is easily scalable to meet ever-increasing current consumption, clock rate, and stringent voltage regulation requirements. Today, every computer and server microprocessor in the world is powered with this multi-phase VR. These technologies have been further extended to high performance graphical processors, AI, chipset, and memory devices, and used in all forms of mobile electronics, networks products and telecommunications. The impacts are fundamental and span multiple industries worldwide.

The Power Management Consortium (PMC) is an outgrowth of the early VRM mini-consortium initiated in 1997, with much expansive research scope and with a focus on developing precompetitive technologies for wide range of applications. The current scope of research encompasses power architecture and management for computer and communication equipment, all forms of mobile devices, date centers, and network products, automotive electronics, EV charger, solid-state lighting, PV inverters, and industrial and consumer electronics. R&D emphases include such key issues as efficiency, power density, cost, power quality, EMI mitigation, and manufacturability.

Since its inception, the PMC program has been supported by more than 50 major global enterprises, and with wealth of knowledge generated, including over 75 US patents, over 650 technical papers, and more than 80 PhD/ MS students who are playing key leadership roles in various industry sectors.

With recent advances in wide-band-gap (WBG) power semiconductor devices, namely, SiC and GaN, we have witnessed significant improvements in efficiency and power density while operating at an order of magnitude higher frequency than the current practice using silicon counterparts. With this dramatic increased operating frequency, current design practices are challenged. Design trade off previously inconceivable or deemed impractical can be realized not only with significant gain in efficiency and power density, but also drastic improvement of EMI/ EMC, manufacturability and cost.

This potential paradigm shift has been one of our major research activities. A number of demonstrations were developed to illustrate the performance improvements and ease of manufacturability, including:

- 48 V /1.8 V Point of Load converter with 160 A continue current and 300 A peak current achieves 95% efficiency and 1100 W/in^3 power density
- 1 kW 400 V /12 V unregulated LLC converter with PCB Based integrated inductors and transformers while achieving 98% efficiency and 960 W/in^3 power density with much improved EMI performance
- 3 kW 400 V /48 V 300 kHz regulated LLC with PCB-based matrix resonant inductor achieves 99% efficiency and 600 W/in^3 power density
- 11 kW 800 V three-phase CLLC converter at 500kHz with 98.6% peak efficiency and 180 W/in^3 power density
- 25 kW soft-switching three-phase inverter/rectifier with PCB based integrated inductors with 98.6% efficiency and 176 W/in^3 power density

With the recent recruitment of Prof. Yuhao Zhang, PMC also established full-stack capabilities for power device research, including device design, simulation, cleanroom fabrication, small-scale process development, device characterization, as well as reliability and robustness studies. Current PMC device research includes the design and fabrication of novel GaN power devices beyond the commercial voltage range (15-650 V), development of p-channel GaN devices and "CMOS"-type GaN ICs, as well as the reliability and robustness studies of commercial GaN power devices under switching conditions and a variety of mission profiles. Below are some on-going device research:

- New GaN power transistors allow multi-megahertz switching at 5 V to 50 V
- New GaN lateral and vertical devices with a voltage class of 650 V to 3300 V with superior performance and low cost
- Single-event and repetitive avalanche and short-circuit robustness testing platform for WBG power devices

Work Scope of PMC

- Wide-bandgap power device design and its reliability study
- High-efficiency and high-power density power supplies using WBG power devices
- High-performance VRM/POL converters with integrated magnetics
- Power architectures and management for servers and data center, PV system, EV charger/charging station
- High-frequency magnetics characterization and integration
- Modeling and control
- Digital control
- EMI mitigation
- Wireless power transfer system for portable electronics

PMC Member Companies

PMC currently has 17 member companies. In 2021, Joulwatt Technology joined as a new member and Navitas Semiconductor upgraded their membership to PMC from Principal level.

Analog Devices Inc.
CRRC Zhuzhou Institute Co., Ltd.
Delta Electronics Inc.
Infineon Technologies AG
Innoscience (Zhuhai) Technology Co., Ltd.
Jiangsu Wanbang Dehe New Energy Technology Co., Ltd.
Joulwatt Technology
Lite-On Technology Corporation
Lockheed Martin Corporation
Murata Manufacturing Co., Ltd.
Navitas Semiconductor
NexGen Power Systems
NXP Semiconductors
Onsemi
OPPO
Panasonic Corporation
Powerland Technology Inc.
Silergy Corporation
Vertiv

Research Team

Faculty

Fred C. Lee
Qiang Li
Yuhao Zhang

Research Faculty

Yi-Hsun (Eric) Hsieh
Ming Xiao

Graduate Students

Ahmed Salah Nabih Ahmed
Xingyu Chen
Rimon Gadelrab
Md Abdul Gaffar
Feng Jin
Zheqing Li
Jingcun Liu
Xin Lou
Yunwei Ma
Tyler McGrew
Adhistira Naradhipa
Pranav Raj Prakash
Gibong Son
Shuo Wang
Xinmiao Xu
Qiuzhe Yang
Xipei Yu
Tianlong Yuan
Ruizhe Zhang
Chunyang Zhao
Feiyang Zhu

Visiting Scholars

Phu Hieu Pham

Leveraged With Government Funding From

Department of Energy (DOE)
National Science Foundation (NSF)
Office of Naval Research (ONR)
PowerAmerica Institute

High-Density Integration (HDI)

HDI was created in 2011 as a mechanism for CPES and industry members to address emerging and long-term challenges in power electronic integration. While it is supported primarily by CPES membership, it also leverages sponsored research with major industries such as Delta, Dowa, GE, GM, Group Safran, Lockheed Martin, MKS, Nissan, Raytheon, Rolls-Royce, TI, Toyota, and UTRC, as well as with government agencies including the U.S. Department of Energy (ARPA-E), U.S. Department of Defense (DARPA, ONR, Army, and Air Force), and National Science Foundation. The tradeoffs among reliability, efficiency, cost, fields, electromagnetic compatibility, power density, and speed are explored as new materials, components, circuits, and applications emerge.

Wide-bandgap and ultra-wide-bandgap semiconductor devices have been designed, fabricated, and characterized for applications with switching frequency in the tens of megahertz, power rating in the megawatts, and junction temperature beyond 250° C. Ancillaries, characterization metrology, modeling method, packaging process, and manufacturing paradigm need to be transformed. Robustness measures such as unclamped inductive switching and short-circuit withstand time have been investigated. Reliability has been characterized using realistic mission profiles.

Unique high-temperature packaging technology is an example of CPES fulfillment of these critical needs to the future power electronics industry. HDI developed die-attach materials that can be processed at low temperatures, yet are reliable at the temperature of the wide bandgap junction. Processes and materials were developed to reduce electric field intensity and improve partial-discharge inception voltage.

Magnetic materials with low core loss-density were synthesized from magnetic metals for additive manufacturing of high-frequency magnetic components. Inductors were fabricated from heterogeneous magnetic composites to shape the EMI spectrum. Over-molding magnetic materials have been synthesized for integrating energy storage and protection functions.

Techniques to decouple the noise loops have been identified to enable high dv/dt commutation in wide-bandgap switches. Design methodologies have been documented for high-temperature capacitors, power buses, protection, sensing, digital control, etc. New breeds of gate drivers, sensors, active filters, and passive filters have been demonstrated in a wide range of products, from power adapters to power electronic building blocks. Significant improvements in power density, efficiency, and signal integrity are expected thanks to the adoption of technological advances. HDI tasks are scoped to advance wide-bandgap systems, magnetic components, and module integration.

This current scope of work includes the following topics:

Wide-Bandgap Systems

- Reliability study of failure mechanisms of wide- and ultra-wide-bandgap switches
- High-voltage high-temperature gallium oxide diode
- Characterization of wide-bandgap semiconductor switches up to highest voltage and temperature
- Short circuit protection design for paralleled GaN module high-density laptop adaptor
- High-frequency, low loss soft-switched converters
- Insulation coordination study for high-voltage high-power density converter design
- Wireless charging

Magnetic Components

- Swinging and coupled inductors with heterogeneous magnetic cores
- Magnetic structures with high-energy density
- Over-molding of encapsulating magnetics
- Low profile magnetic substrate
- Weakly coupled coils with a low stray field for wireless power

- Integration of and field interaction in common-mode and differential-mode filters
- Integrated multi-phase inductor for a voltage regulator for small portables
- PCB-integrated magnetics for high-efficiency, high-density front-end power supply
- Characterization of high-power inductors and materials
- High-frequency magnetic integration

Module Integration

- Large-area substrate-to-substrate bonding by silver sintering
- Reliability evaluation of module interconnects
- Current sensor integrated with SiC MOSFET module
- High-voltage SiC module packaging
- Integration of magnetic dice into the power module
- Electromagnetic interference (EMI)

Work Scope

- Wide-bandgap devices
- Material and component characterization
- Active module integration
- High-frequency magnetic integration
- Converter integration
- Wide power range (10 W – 100 kW)
- High frequency (100 kHz – 10 MHz)
- High temperature ≥ 250° C

HDI Member Companies

There are currently 10 companies participating in HDI. In 2021, HDI was pleased to welcome Crane Aerospace & Electronics as a new member and Raytheon Technologies who upgraded their membership from the Principal level.

Crane Aerospace & Electronics
Delta Electronics Inc.
Ford Motor Company
GE Global Research/GE Aviation
Lockheed Martin Corporation
Moog Inc.
Nissan Motor Co., Ltd.
Raytheon Technologies
Texas Instruments
VisIC Technologies
Würth Elektronics
ZF Friedrichshafen AG

Research Team

Faculty

Dushan Boroyevich
Rolando Burgos
Christina DiMarino
Dong Dong
Mona Ghassemi
Fred C. Lee
Qiang Li
Guo-Quan Lu
Khai Ngo
Yuhao Zhang

Research Faculty

Ming Xiao

Graduate Students

Ahmed Salah Nabih Ahmed
Filip Boshkovski
Mark Cairnie
Yuliang Cao
Md Abdul Gaffar
Jacob Gersh
Jack Knoll
Joseph Kozak
Bo Li
Shengchang Lu
Pranav Raj Prakash
Qihao Song
Joshua Stewart
Cong Tu
Boyan Wang
Le Wang
Shuo Wang
Yue Xu
Zichen Zhang

Leveraged With Gifts From

ABB Inc.

Leveraged With Government Funding From

Department of Energy (DOE)
Advanced Research Project Agency - Energy (ARPA-E)
PowerAmerica
Office of Naval Research (ONR)

Wide-Bandgap High-Power Converters and Systems (WBG-HPCS)

This CPES mini-consortium has provided since 2011 a most unique, open, and collaborative forum for the power industry to explore new and emerging power conversion technology and applications. WBG-HPCS looks at everything from power semiconductors, to gate drivers and ancillary circuitry, to converters, all the way to the impact that they have on electrical power systems, and features a research scope that has successfully expanded into high-power medium-voltage (MV) applications for grid, industrial, and transportation applications.

As a mini-consortium, WBG-HPCS allows CPES to pool various resources seeking to develop the above pre-competitive technology. The program is strongly leveraged by CPES's vast expertise in WBG-based power conversion and its in-depth knowledge of electronic power systems accrued by working closely with the space, transportation, and IT industries. In addition, CPES has continued to support research activities within the WBG-HPCS mini-consortium by securing funding—at the basic research level—from several government agencies, including the Office of Naval Research (ONR), the U.S. Department of Energy (DOE), and ARPA-E.

The above agencies have been instrumental in developing key enabling technology presently used in WBG-based high power electronics applications, and as such represent ideal partners for CPES. Their collaboration over the past years has generated invaluable synergy within CPES aiding in the pursuit of the mini-consortium goals. From a funding standpoint, CPES has been able to effectively quadruple the research activity in this area thanks to their support, ultimately quadrupling too the results and technological advancement that are shared with its members.

Present research thrusts:

High-Power WBG-Based Power Conversion Technology

- Design and development of high power density SiC-based modular multilevel converters based on 1.7 kV, 3.3 kV, and 10 kV devices
- High-frequency PWM and control of modular multilevel converters in ac-dc and dc-dc mode
- Development of EMI containment and suppression strategies for power converters, modular converters, and electronic distribution systems

- Formulation of electric-field constrained design methodologies for power components subject to high-frequency excitation and fast dv/dt transients
- Design of electric-field constrained power converters and components for high-altitude (30,000 – 60,000 ft) aerospace applications
- Development of enhanced gate drivers, auxiliary power supplies and sensors for harsh dv/dt and EMI environments
- Characterization of MV SiC and LV GaN devices

Stability and Dynamic Interactions

- Stability impact of grid-forming control schemes
- Stability assessment and interactions in MV Distribution Systems in the presence of utility-scale PV inverters
- Stability assessment and interactions in HV Transmission Systems in the presence of multiple STATCOM units operating in proximity
- Stability analysis in three-phase unbalanced and single-phase distribution grids, including generator-fed systems
- SiC-based impedance measurement unit (IMU) for ac and dc LV and MV distributions systems
- Self-impedance-measurement-based stability monitoring in grid-tied inverters

Renewable Energy Integration

- Development of grid-forming controls under grid-connected and islanded conditions
- Dynamic impact of PV inverters in MV distribution systems
- Protection system operation under high penetration of PV inverters in MV distribution grid
- Design of high-efficiency SiC-based grid-tied PV inverters for MV and LV applications
- Design of high-efficiency GaN-based grid-tied inverters for residential PV applications

WBG-HPCS Member Companies

ABB Inc.
Aurora Flight Sciences
Delta Electronics
EnerSys
GE Grid Solutions
Rockwell Automation
Siemens Corporate Technology
TMEIC Corporation

Research Team

Faculty

Dushan Boroyevich
Rolando Burgos
Dong Dong
Fred C. Lee
Qiang Li

Research Faculty

Igor Cvetkovic
Boran Fan
Bo Wen
Eric Hsieh

Graduate Students

Victoria Baker
Yuliang Cao
Che-Wei Chang
Yugal Gupta
Qian Li
Zheqing Li
Qing Lin
Xiang Lin
Jian Liu
Vladimir Mitrovic
Slavko Mocevic
Jayesh Motwani
Vinay Mutyala
Minh Ngo
Lakshmi Ravi
Yu Rong
He Song
Matthias Spieler
Joshua Stewart
Keyao Sun
Ye Tang
Ning Yan
Jianghui Yu

Leveraged With Gifts From

ABB Inc.
Dominion Energy

Leveraged With Government Funding From

Department of Energy (DOE)
Advanced Research Project Agency-Energy (ARPA-E)
Office of Naval Research (ONR)

Sponsored Research

POWER PROCESSING SYSTEMS DEVELOPMENT

In synergy with industry consortium research, CPES also has numerous sponsored research projects, funded by state and federal government and companies around the world. In 2021, there were almost 50 sponsored projects totaling approximately $5M.

These projects cover the breadth of CPES expertise across six technology areas and focus on four application areas:

Technology Areas

- Power conversion technologies and architectures
- Power electronics components
- Modeling and control
- EMI and power quality
- High-density integration
- High-power high-voltage converters

Application Areas

- Power management for information and communications technology
- Point-of-load conversion for power supplies
- Vehicular power converter systems
- Sustainable and distributed electronic energy systems

ABB Fellowship

Project Lead: Rolando Burgos

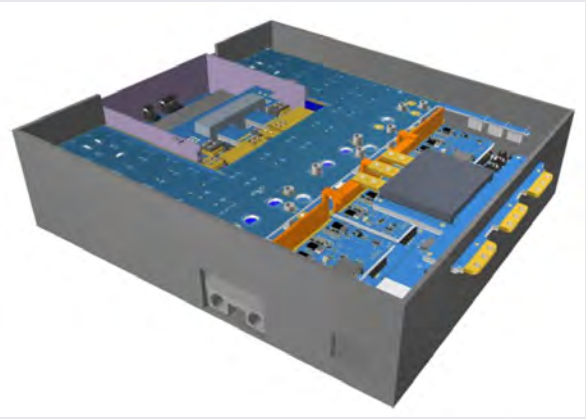
This fellowship program was originally established to investigate the capabilities of wide-bandgap power semiconductors. Although the first year concentrated on the evaluation of gate-driver circuitry for silicon carbide (SiC) 1.7 kV and 10 kV MOSFET devices, the following years were fully devoted to the evaluation and assessment of the high-power handling capability of gallium nitride (GaN) power semiconductors. The effort concluded in 2020 with the development of a packaging solution for the latest generation of 10 mΩ GaN 650 V dies from GaN systems, for which a ceramic substrate module with PCB interposer was built and successfully demonstrated in both single-and half-bridge module configurations. A parallel effort explored the impact of the dynamic RDS(on) effect on the design of GaN-based power converters. In 2020, the fellowship direction returned once again to SiC devices, and specifically to the evaluation of SiC MOSFET devices as a viable power semiconductor for solid-state circuit breaker (SSCB) applications. Specifically, the work conducted developed a design methodology for SiC-MOSFET-based SSCB, focusing on the design and breaking capabilities of MOSFETs and the companion MOV devices used. While the design methodology investigations were conducted using 1.2 kV SiC MOSFETs, a final prototype was built using 3.3 kV SiC MOSFET modules from Mitsubishi, which were tested at dc voltages of up to 13 kV and fault currents of up to 5 kA operating in series- and parallel-connection modes.

High-Density, High-Altitude, High-Voltage, High-Speed Motor Control Unit (MCU) for Aviation Electric Propulsion

Sponsor: Airbus

Project Lead: Dong Dong

Airbus, one of the leading aerospace and defense solution providers, partnered with CPES to investigate power conversion solutions for high-altitude-ready, liquid-cooled, high-speed motor control unit (MCU) systems. The goal is to attain high-power density and high efficiency by profiting from new, advanced power conversion topology, sensing, and integration technologies in 200 kW applications.



Rendering of the proposed power conversion solution featuring advanced topology, sensing, and integration for 200 kW applications.

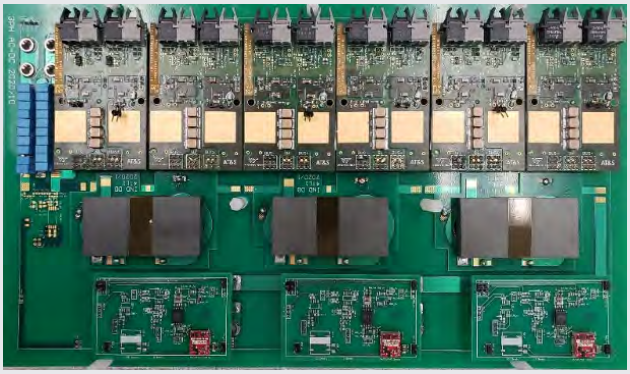
Design, Evaluation, and Demonstration of an Embedded SiC Power Module for Electric Vehicle On-Boarder Charger

Sponsor: AT & S

Project Lead: Christina DiMarino

Embedding power semiconductors using PCB manufacturing processes can enable automated, flexible, low-cost, high-volume production of power electronic converters, while offering improved performance and reduced system size and weight. This is especially desirable for the electric vehicle industry due to the increasing needs for greater manufacturing throughput, improved cost competitiveness, and better performance and power density.

This work will demonstrate a high-power-density 800 V, 22 kW on-board charger system (OBC) with PCB-embedded 1.2 kV SiC MOSFETs and PCB-winding magnetics. Compared to state-of-the-art 1.2 kV half-bridge modules, the PCB-embedded half-bridge module in this work has eight-times lower power loop inductance, twelve-times smaller volume, and two-times lighter weight. The ac-dc stage of the OBC system achieves 98.2 % efficiency and 160 W/in^3 power density. The dc-dc stage will be developed using the PCB-embedded SiC half-bridges and PCB-winding inductors and the full 22 kW OBC system will be tested.



22 kW ac-dc converter with PCB-embedded SiC MOSFETs and PCB-winding inductors.

DC-DC Converter for Electrocaloric Air Conditioning Systems

Sponsor: Carrier Corporation

Project Lead: Rolando Burgos

CPES worked jointly with Carrier to characterize the static and dynamic behavior of new electrical films with electrocaloric properties, seeking to develop a suitable model of these devices and to conduct simulations to improve the understanding of their properties and capabilities. In addition, CPES successfully developed a new dc-dc power converter topology capable of driving these types of films, achieving maximum efficiency, power density, and minimum control and system complexity. A final 1 kW, 1 kV dc-dc converter prototype was built and demonstrated.

USB Type-C Power Delivery: Charger Development

Sponsor: Collins Aerospace

Project Lead: Rolando Burgos

The objectives of this project are to develop an integrated, highly compact USB Type-C power delivery charger targeting low cost and high efficiency, and seeking to demonstrate a TRL 3 single-output prototype, including both single-phase PFC ac-dc and high-frequency isolated dc-dc stages, with the following specifications: 100 W, 115 V, 360–800 Hz input, 5, 9, 15 and 20 V dc output. The project will specifically target: power density > 50 W/in^3, nominal power efficiency > 90 %, 10 % load efficiency > 80 %, and 15 mW of standby power consumption. The proposed converter will use commercial-off-the-shelf (COTS) units as benchmark. The charger will encompass the power stage, electromagnetic interference (EMI) filters, and use available integrated-circuit (IC)-based controls, allowing the project to hone in on the performance and integration aspects of the unit. The main challenge at hand will be the design optimization of the ac-dc-dc powertrain to satisfy the wide-output voltage range of the USC-C type charge specifications.

High-Frequency, Three-Phase Inverter

Sponsor: CSR Zhuzhou Institute Co., Ltd.

Project Lead: Qiang Li

This project focused on a high-frequency, high-density, frequency isolated, three-phase inverter module with wide-input voltage range. A two-stage solution is used to provide isolation and accommodate wide-input voltage range. Soft-switching techniques and integrated-magnetic solutions are used to improve the efficiency and power density for the proposed system. The targeted power level and efficiency are 20-30 kW and 95-97 %.

Dominion Energy Fellowship

Project Lead: Rolando Burgos

This fellowship program was originally established to investigate the dynamic interactions that can arise when

multiple static synchronous compensator (STATCOM) units operate in proximity to transmission systems (200–500 kV ac lines). In the following years the fellowship continued by exploring the impact that utility-scale photovoltaic (PV) inverters have in medium-voltage (MV) distribution grids; especially in the case that these units are complying with the new voltage and frequency compensation requirements of the IEEE Std 1547. In 2019, the fellowship specifically addressed stability concerns in unbalanced MV grids, where a new stability assessment theory and approach were developed and validated experimentally, overcoming a limitation of the conventional impedance-based stability assessment approach and a technical and theoretical challenge that CPES had pursued for more than 15 years. Since 2020, the fellowship program has continued expanding the breadth of the analysis conducted to determine the impact that PV inverters can have on the protection coordination of distribution grids. Specifically, on identifying the increase or decrease of short-circuit currents throughout the distribution grid when increasing amounts and distributed PV inverter generation is present in the system, quantifying as well the advantages and disadvantages that PV inverters with grid-forming controls can have in this respect.

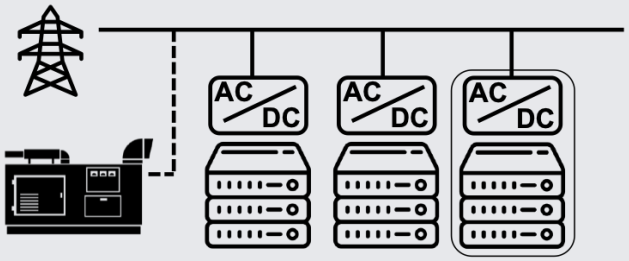
Small-Signal Stability Analysis in Data Centers With Unbalanced Power Factor Correction Loads

Sponsor: Google

Project Lead: Bo Wen

Google has approached CPES to investigate the stability and dynamic interactions in data center distribution systems with multiple single-phase power factor correction (PFC) loads. The objective of this project is to analyze the small-signal stability in three-phase, four-wire data center distribution systems with multiple PFC loads, with the intent to formulate an analysis methodology and a test procedure capable of predicting the occurrence of dynamic interactions, having as a goal the reduction in the number of field tests during the construction and commissioning of data centers.

CPES will expand on its recently developed stability analysis methods for three-phase unbalanced networks, developing the corresponding models to study the above system, and building a testbed to verify the methods to be developed. The latter will employ both a Google power supply unit, and CPES-developed PFC loads given the expected need to have full knowledge of the PFC operation and controls in the formulation of the methods in question. Lastly, CPES will make use of its low-voltage impedance measurement unit to extract the synchronous d-q frame, small-signal impedances seen at the points of interest.



Schematic for a data center power system.

Undergraduate Student Research, Major Design Experience

Sponsor: Office of Naval Research and Lockheed Martin

Project Lead: Dushan Boroyevich

The Major Design Experience in the Bradley Electrical and Computer Engineering (ECE) Department provides hands-on project development towards solving industry challenges for teams of undergraduate students.

Program benefits include:

1. Supporting the undergraduate education mission of ECE.
2. Providing CPES teaching and research faculty and PhD students expanded teaching and advising experience.
3. Increasing undergraduate recruiting opportunities for CPES Industry Consortium Members and the CPES graduate program.
4. Providing engineering and research personnel for CPES-sponsored research projects.

All CPES faculty are participating in the MDE.

High-Density, High-Frequency, Bi-Directional Battery Charger Converter

Sponsor: Moog Inc.

Project Lead: Dong Dong

The objective of this project is to develop a highly-integrated, high-power-density, and high-efficiency energy management converter system for stationary battery systems seeking to demonstrate the size reduction that is possible when operating at high-switching frequency using WBG devices. The project will develop the novel partial power processing architecture, flexible PCB technology, and soft-switching bi-directional topology to significantly enhance the durability, reliability, and flexibility for harsh environments. The technology intends to be modular in nature, seeking to address a wide-range of energy storage, bi-directional, onboard, and stationary applications.

Terminal Behavioral Modeling of Electric Machines for Real-Time Emulation, System-Level Analyses, and Stability Studies

Sponsor: Newport News Shipbuilding, Huntington Ingalls Industries

Project Lead: Igor Cvetkovic

In order to support "Next Generation Power Architecture & Power Management" independent research and development within Huntington Ingalls Industries, CPES is working jointly with Newport News Shipbuilding engineers on the development of component and system models with a high-level of fidelity to assess system performance in architecture trade studies. Hence, this project is focused on the development of a terminal behavioral model of permanent magnet synchronous machines for real-time emulation, system-level analyses, and stability studies. Machine model is obtained in-situ with electric machine undergoing frequency-domain characterization at different operating points. System dynamics is then removed from the measurements leaving only bare machine dynamics ready to be used in different simulation scenarios, both on the non-real-time and real-time platforms. Having machine dynamics fully characterized in the desired frequency range, this methodology further offers an opportunity to perform a small-signal stability assessment of the machine under test at both mechanical and electrical interfaces.

High-Efficiency, High-Density, Automotive DC-DC Converters

Sponsor: Panasonic Automotive Systems Company of Americas

Project Lead: Qiang Li

This project focuses on the design of automotive dc-dc converters: 400 V/48 V converter and 400 V/12 V converter. The two converters are implemented based on the two-stage approach. The 48 V converter uses an LLC with a 3:1 step-down matrix transformer, whereas the 12 V converter uses an LLC with an 8:1 step-down matrix transformer. The 48 V converter achieves 96.6 % efficiency at nominal condition (350 V/44 V) with 3 kW/L power density (including heat sink). The 12 V converter achieves 96 % efficiency at nominal conditions (350 V/14 V) with 2.5 kW/L power density (including heat sink).The designed converters feature feedback digital control for soft startup and transient response. Both converters can achieve fast transient response with overshoot and undershoot below 10 %.

AC Filters for Back-to-Back Wide-Bandgap-Based, Three-Phase Power Converters

Sponsor: Siemens Corporation

Project Lead: Rolando Burgos

Siemens AG has approached CPES with the purpose of developing new, optimized filter topologies for three-phase, back-to-back (B2B), grid-to-motor converter systems rated for 25 kW, 400 V ac, 50/60 Hz line frequency, 650 V dc, 0-60 Hz motor-side frequency, and a switching frequency in the 40-100 kHz range. The filters in question should meet power quality and conducted electromagnetic interference (EMI)-applicable standards, and feature minimized parasitic resistances, inductances, and capacitances both at the component and filter-level. A key aspect of the investigation should be the identification of limits and development of processes, in terms of parasitic components, materials, form factors, and manufacturing, which could lead to the formulation of design guidelines for filter components with reduced magnitude and sensitivity to parasitic components. In addition, the impact of unshielded motor cables should be evaluated. The project will focus on three-level, B2B converter topologies given the inherent advantages of this circuit configuration.

Series-Resonator Buck Converter for 48 V-54 V Power Delivery

Sponsor: Texas Instruments

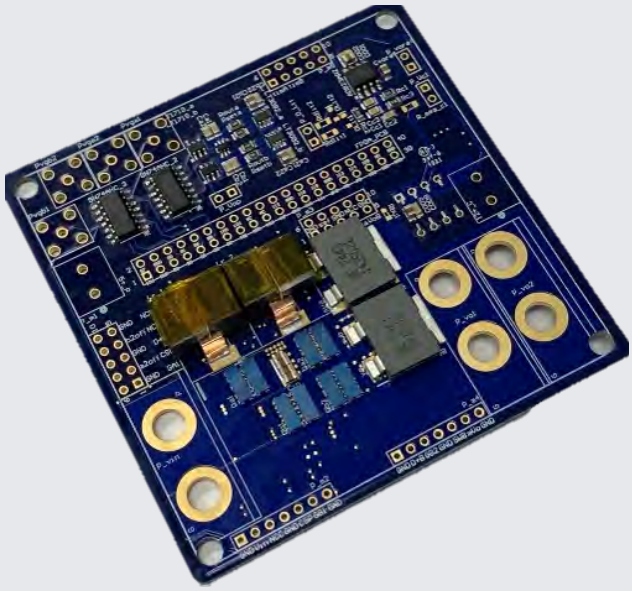
Project Lead: Khai Ngo

This fellowship program was established to support research in power delivery for data centers. As the current requirement exceeds 200 A, the 12 V architecture for power delivery incurs an excessive loss. A voltage regulator module with 48 V bus voltage is introduced as a candidate to achieve high efficiency and high-power-density for data center applications.

A series-resonator buck (SRB) converter is proposed for a two-stage architecture for 48 V-1 V power delivery with high efficiency, high-power-density, and low noise. Compared with a series-capacitor buck (SCB) converter, it achieves soft-switching with a wide and variable gain range. The solution is evaluated as the front end of the two-stage solution.

A high-frequency, high-current stress resonant inductor enables soft-switching in the SRB converter. Fringing-induced loss, eddy-current loss, and core loss hinder efforts to reduce size via increasing switching frequency. The

winding area is redesigned for balancing winding loss and core loss. The new design has been demonstrated in a 200 W SRB converter.



Series-Resonator Buck (SRB).

Machine Learning-Enhanced Material-Device Co-Design for Power Electronics

Sponsor: Thomas F. & Kate Miller Jeffress Memorial Trust

July 2020 – December 2021

This project aims to develop a novel and computationally efficient framework comprising advanced machine learning (ML) models and a data-generation scheme that utilizes technology computer-aided design (TCAD) simulations to augment the experimental data. The proposed framework will be used to design and analyze power devices based on emerging wide-bandgap (WBG) semiconductors, which hold great promise for next-generation power electronics applications in electric vehicles, data centers, and smart grids. This project also highlights research training opportunities for undergraduate students.

20 kV GaN Switch Technology Demonstrated in High-Efficiency, Medium-Voltage Building Block

Sponsor: Advanced Research Projects Agency-Energy

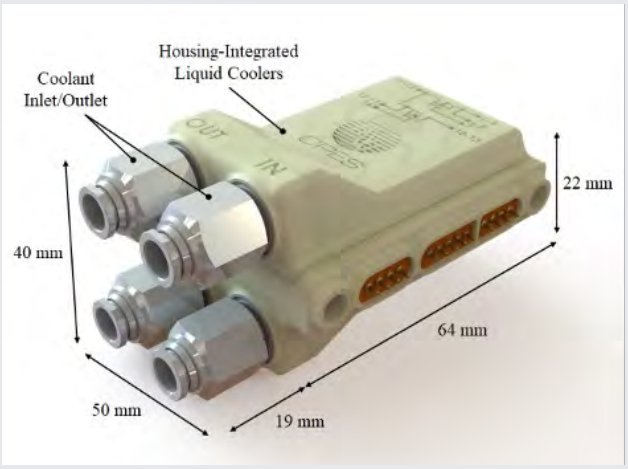
Project Lead: Khai Ngo

Gallium-nitride's (GaN) 6x lower specific on-resistance compared to SiC makes it an ideal candidate for widespread deployment in grid-scale applications. The primary focus of this program is to demonstrate lateral GaN devices with blocking voltage >10 kV along with the required packaging techniques to make the technology feasible in grid-scale power conversion.

At the semiconductor level, the goal is to utilize metal organic chemical vapor deposition (MOCVD) to grow GaN drift layers with carbon contamination ≤1E15 cm^{-3} and residual oxygen content ≤7E14 cm^{-3} with controllable electron densities below 1.5E15 cm^{-3}. Such drift layers enable the delivery of 5 kV, 10 A diodes useful for grid applications. In conjunction with the material characterization efforts, fabrication of lateral GaN diodes with blocking voltages >10 kV using commercial wafers is underway for eventual demonstration in a 10 kV GaN package.

To ensure reliable insulation performance of the package, a resistive field grading coating is developed to manage the electric field crowding around critical triple-points in the package. The resistive coating assists in electric field reduction, allowing for thinner insulating substrates and improving thermal performance while providing >50 % improvement in PDIV compared to the state-of-the-art.

All these technologies will be demonstrated in a 10 kV GaN diode package with double-sided cooling. Currently, the package utilizes 10 kV SiC devices but will later be used with 10 kV lateral GaN diodes. The module leverages the resistive field grading coating to achieve a compact footprint of 64 x 50 x 22 mm^3 while maintaining a safe partial discharge inception voltage and achieving >50 % improvement in power density over the state-of-the-art.



A 10 kV, 50 A phase-leg package utilizing resistive field grading coating to enable a >50 % improvement in power density compared to the state-of-the-art.

An integrated isolated gate power supply for a planar three-phase SiC power module is also being developed as part of the program.

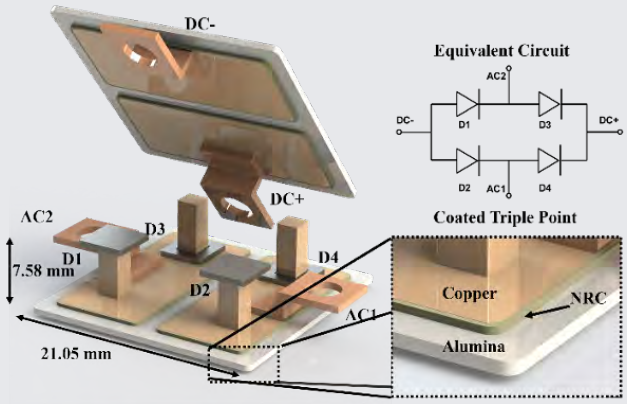
The rated junction temperature of the SiC die is 200 °C. The nearness to the high-temperature junction greatly increases the operating temperature of the power supply to above 125 °C. The lack of magnetic cores at such a temperature led to the use of an air-core transformer with PCB winding for the isolation stage.

To accommodate the 6 cm^2 per package device area, the switching frequency is increased to 7 MHz to minimize the footprint of the air-core transformer. A class-e converter topology is designed to eliminate turn-on loss of the switching device. Air-core inductors and transformers are designed to achieve a load-independent output current with ZVS.

A 20 W six-output isolated transformer has been designed. Extra compensation was added to eliminate cross-coupling between secondary windings. A sandwich winding structure was applied to minimize transformer footprint and isolation capacitance between windings.

Finally, the program includes the development of a material coating or shielding technology for reducing the electric field intensities inside medium-voltage power modules. A nonlinear nanoparticle-polymer composite (NPC) is developed and evaluated. It exhibits an electric-field-dependent electrical conductivity. The composite was coated and cured at the electrodes' edges of medium-voltage power module insulated-metal substrates. The measured partial discharge inception voltage increases up to 100% more than those substrates without the coating. To demonstrate the coating technology, a double-side, cooled, 10 kV SiC diode module with sintered-silver joints was designed, analyzed, fabricated, and characterized.

We are currently improving the formulation and the processing procedures of the composite. This new material could offer a cost-effective insulation solution for packaging MV power modules without compromising their thermal performance.



Exploded view of the 10 kV SiC full-wave diode module with coated 0.5 mm alumina DBC substrates. The four 10 kV SiC JBS diodes and the connection terminals are labeled corresponding to those in the equivalent circuit.

Ultra-Efficient Intelligent MVDC Hybrid Circuit Breaker

Sponsor: U.S. Department of Energy, Sub-Awardee of Eaton Corporation

Project Lead: Dong Dong

DC power provides numerous benefits at low (<1 kV), medium (1-100 kV), and high (>100 kV) levels. Both low-voltage dc (LVDC) and high-voltage dc (HVDC) markets are maturing. MVDC markets, comparatively, are still in the early phases of development. Currently, MVDC is primarily used in rail, with voltages up to 3 kV; however, MVDC benefits extend to a variety of potential markets, including distribution networks (e.g., conversion of existing ac lines to dc), distributed energy resources (DERs), and integrated renewable energy. One of the main difficulties preventing the growth of dc markets is a lack of reliable hardware protection against faults (e.g., short circuit and overload faults). Circuit breakers, current limiters, and fault detection mechanisms are essential to grid resiliency in a number of ways: sectioning the grid during a fault; preventing damage to wiring, power electronics, and other important assets; and restoring power to the grid after a fault is cleared.

In this program, CPES will work with Eaton Corporation and the Illinois Institute of Technology to develop an ultra-fast, ultra-efficient, intelligent, MVDC hybrid circuit breaker. The main objective of the program is to achieve 6 kV dc operating voltage, 200 A rated current, <500 μs active interruption time, and >99.99 % efficiency and <0.064 m^3 form factor. The technology to be developed

Eaton team visiting CPES researchers for project discussions.

in the program is an ultra-fast vacuum switch, novel transient commutation current injector, and MV electronic interrupter, as well as system integration and intelligent switching operation.

Power Conversion Through a Novel Current Source Matrix Converter

Sponsor: Advanced Research Projects Agency-Energy, Sub-Awardee of Raytheon Technologies Research Center

Project Lead: Rolando Burgos

Raytheon Technologies Research Center (RTRC), formerly United Technologies Research Center (UTRC), proposed a novel solution of a Matrix Converter (MxC), with voltage boost capability as a response to the ARPA-E SWITCHES program. The proposed solution enables operation above 86.6 % of input voltage and thus overcomes limitations of traditional MxC. Accordingly, the proposed MxC operates in "boost" current control mode (CCM) in contrast to the traditional voltage control mode (VCM). The concept is applicable to the broad range of systems where the source is an electrical generator. CPES has supported this effort by developing two hardware prototype demonstrators of the MxC, rated at 380 V ac, 60 Hz, and 15 kW, with a 1-min overload capacity of 25 kW, using 1.2 kV Silicon-Carbide (SiC) MOSFET devices.

The first-generation prototype used a modular per-phase PCB-based structure and through-hole discrete SiC MOSFETs packaged in 4-pin To-247, successfully demonstrating the boost current-mode operation of the MxC while also achieving a power density of 10 kW/L. The second generation, improved prototype adopted surface-mount devices to improve the switching performance and manufacturability of the unit, and used instead a single PCB-based design with aluminum nitride ceramic inserts to minimize the thermal impedance from the device packages to the bottom-side mounted heatsink. The full three-phase implementation of the MxC on a single PCB was further exploited by designing an optimized physical layout, which minimized and balanced the parasitic inductances for the three commutation paths per switching pole. This resulted in an improved switching performance and reduced EMI, which helped counteract the main tradeoff of adopting surface-mount devices; namely the increased

parasitic capacitance to ground. With these significant improvements, the second-generation MxC achieved a power density of 15 kW/L, an efficiency of 98.5 %, and a 1-minute 25 kW overload capacity.

ULTRA-COMPACT: Ultra-Light, inTegrated, Reliable, Aviation-Class, Co-Optimized Motor & Power Converter With Advanced Cooling Technology

Sponsor: Advanced Research Projects Agency-Energy, Sub-Awardee of Raytheon Technologies Research Center

Project Lead: Rolando Burgos

ARPA-E seeks to decrease aviation greenhouse gas emissions through the implementation of high-performance hybrid electric propulsion systems. One piece of a vision system includes high-performance (12 kW/kg at 96 % efficiency) electric-to-shaft power systems to be developed in the ASCEND program. The electric-to-shaft power system includes the motor, motor drive, cooling system and gearbox (if needed) required to convert dc power to 5000 rpm shaft power.

To meet this need, Raytheon Technologies Research Center (RTRC), with its partners Collins Aerospace, CPES at Virginia Tech (VT), Purdue University, University of Buffalo, and Ames National Lab, propose to develop the Ultra-Light, inTegrated, Reliable, Aviation-Class, and Co-Optimized Motor & Power Converter With Advanced Cooling Technology (ULTRA-COMPACT) system. The ULTRA-COMPACT includes:

1. Stator with simplified winding architecture (utilizing ~90 % of the coil to produce torque), U-shaped PM rotor (formed with interior, exterior, and one side axial) spinning at high speed (~15000 RPM)
2. SiC-based series-parallel, multi-level circuit topology with electromagnetic-interleaving
3. Integrated and actively controlled thermal management solutions (TMS) using two-phase, liquid-vapor loop with a dielectric refrigerant
4. High-density gear box, made with light-weight composite/hybrid materials

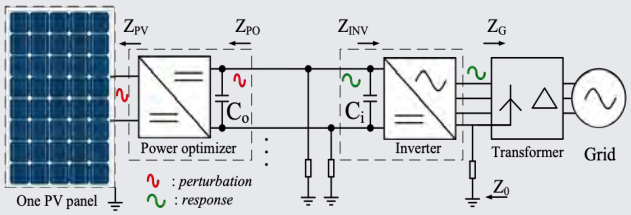
Combined, these four technology elements along with advanced materials pave a path to achieving PD (12.2 kW/kg) and efficiency (96.6 %).

Power Electronics-Based Self-Monitoring and Diagnosing for Photovoltaic Systems

Sponsor: U.S. Department of Energy

Project Lead: Bo Wen

U.S. Department of Energy has supported the development of a prototype self-monitoring and diagnosing technology for photovoltaic (PV) systems to reduce energy production losses. The proposed technology will enable existing panel-level power optimizers and inverters in a PV system to actively perturb the system, measure its response to these small-signal perturbations, and detect any changes in the small-signal impedances. Through computer algorithms to be developed in this project, these impedance changes will be used to identify specific faults and power degradation trends of the associated components. This information can be used to instantly alert operations and maintenance personnel of the need for corrective action, thereby reducing energy production losses earlier relative to standard PV systems.



Power electronics-based self-monitoring and diagnosing for PV systems.

Heterogeneous Integration Technologies for High-Temperature, High-Density, Low-Profile Power Modules of Wide-Bandgap Devices in Electric Drive Applications

Sponsor: U.S. Department of Energy

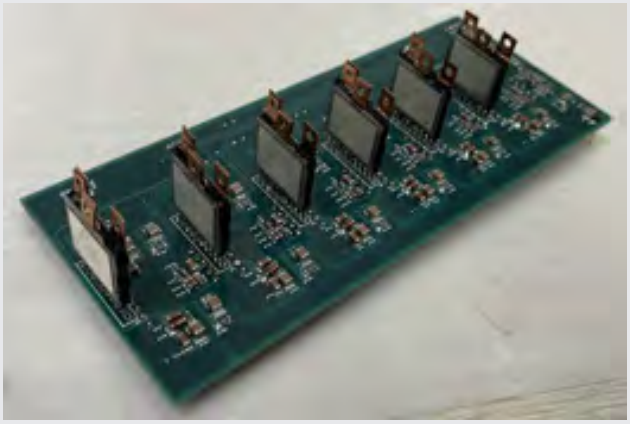
Project Lead: GQ Lu

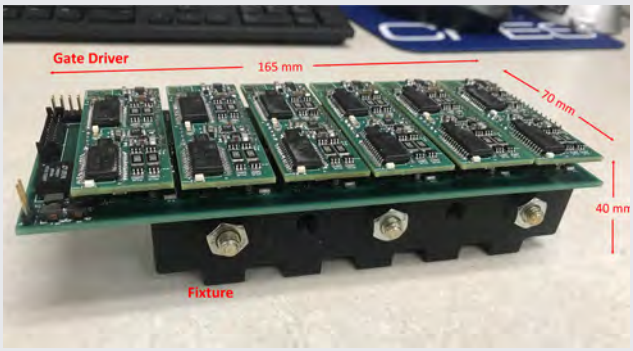
The goal of this project is to develop packaging technologies for making high-temperature, high-density, and low-profile wide-bandgap (WBG) power electronics modules for electric drives. These modules are aimed at enabling the DOE's University Consortium to reach its 2025 inverter targets of ≥ 100 kW/L and ≤ 2.7 $/kW. The specific objectives are to:

1. Design and fabricate double-side cooled SiC half-bridge power modules with parasitic inductances < 5 nH, heat flux density > 400 W/cm^2, and working junction temperature > 200 °C

2. Design and fabricate gate drivers capable of working over 200 °C
3. Design and prototype intelligent gate drivers with integrated current sensor and protection for 200 °C module

The state-of-the-art silicon carbide devices rated at 1.2 kV and 147 A are packaged by sintered-silver bonding on an aluminum nitride direct-bond-copper substrate for high-thermal conductivity, high-working temperature, and high-joint reliability. Porous silver posts are used to interconnect the device's source pads to the other direct-bond-copper substrate for low mechanical stresses, ease of manufacturing, and double-sided cooling. Gate driver and power supply are integrated into the low-profile SiC power module. A constant-current, class-e, dc-dc converter with air-core transformer is designed. The air-core transformer is used due to the unavailability of magnetic core above 200 °C. A current sensor based on package parasitic inductance is developed to measure switching current. A dynamic feedback scheme is developed to compensate the temperature effect on the current measurement.





Six double-side cooled SiC phase-leg modules and their gate-driver board delivered to Oak Ridge National Laboratory for constructing a 100 kW/L inverter.

13.8 kV Grid-Interface Power-Conditioning Converter with AC and DC Microgrid Ports for Dispatchable and Resilient Manufacturing Facilities

Sponsor: U.S. Department of Energy

Project Lead: Rolando Burgos

CPES, in partnership with Siemens, is working to demonstrate a 13.8 kV medium-voltage (MV), power-conditioning system (PCS) for flexible manufacturing plants, rated at 1.1 MVA (1 MW, 450 kVAr), with accessible 22 kV (MVDC) dc ports, using 10 kV silicon carbide (SiC) MOSFET modules and a back-to-back, ac-dc-ac, 5-level, 'multi-cell' power converter topology. The converter system will be designed with the following targets per each three-phase, ac-dc building-block:

1. 99.7 % peak efficiency
2. A volume of 0.2 m3 per MVA (power density = 5 kW/L)
3. Manufacturing costs without SiC devices of 13.6 $/kW
4. A service lifetime > 10 years

To show the scalability of the proposed converter up to 3.3 MVA, the project will also demonstrate a phase-leg (ac-dc building block) with threefold power rating using a CPES-developed, triple-output gate-driver and force-paralleled 10 kV SiC modules that will triple the number of SiC dies per switch position. This higher-power configuration will greatly simplify the PCS architecture for applications of up to 10 MVA (3 x 3.3 MVA).

High-Power-Density, 10 kV SiC-MOSFET-Based Modular, Scalable Power Converters for Medium-Voltage Applications

Sponsor: Advanced Research Projects Agency-Energy

Project Lead: Rolando Burgos

The nearly ideal material properties of silicon carbide (SiC) are transforming the design and manufacturing paradigm of power electronics. Specifically, pervasive dv/dt and di/dt rates, augmented electromagnetic interference (EMI) emissions, higher operating voltages and switching frequencies, and junction temperatures greater than 200 °C, have made apparent the need for the reformulation of design procedures developed for Silicon (Si)-based power electronics, as well as for the materials, packaging and integration, and manufacturing technologies used. More so, the adequacy of existent circuit topologies is under scrutiny now, as their Si-optimized operation may impede the exploitation of the capabilities offered by SiC.

The last point is of special interest in medium-voltage (MV) and high-voltage (HV) applications, where multilevel converters and modular multilevel converters (MMC) have been developed to overcome the limitations of Si in terms of breakdown voltage, switching frequency, and efficiency. Expectedly, the use of SiC in these Si-optimized converters would yield minor gains, for which simpler two-level topologies have been pursued so far for 10 kV SiC MOSFETs. The latter promise direct connection to 4, 160 V ac busses and increased power density by switching at 20–40 kHz, in what is a glimpse of the potential offered by SiC.

Addressing the above, this project proposed the development of modular power converters for MV applications optimized for SiC devices capable of achieving:

1. Power density greater than 10 kW/L
2. Efficiency greater than 99 %
3. Specific power greater than 10 kW/kg
4. Unrestricted current and voltage scaling
5. Operation in both ac and dc power conversion modes

Such flexibility can be attained by adopting an MMC-type circuit, but using previously untapped topological states of this converter. Two unique circuit operating modes are unveiled in this way, one enabling the switching-cycle control of the power-cell voltages, which effectively eliminates their line-frequency dependence, and one that inverts their operating mode allowing for the direct power flow between the converter input and output terminals without having to transiently store energy in the power-cells. Both concepts have been extensively tested through simulations in applications of up to 120 power-cells, but have yet to be demonstrated experimentally. This constitutes the main objective of the project that targets the development of 5 MW, 20 kV modular ac-dc, and dc-dc power converters.

During 2019, CPES successfully demonstrated two power-cells rated at 6 kV dc, 84 A rms, switching at 10 kHz, operating in a circulating power scheme, and processing 250 kW at an exceedingly high 99.3 % power conversion efficiency. The power-cell building-blocks in question also demonstrated the effective use of PCB technology to realize 6 kV dc planar dc bus structures featuring partial-discharge-free operation at 6 kV. The program has also successfully demonstrated auxiliary power supplies with insulation ratings of up to 30 kV, and input-output capacitances in the 2–3 pF range, which are necessary to effectively suppress the propagation of conducted EMI through the power-cells. The project has also made effective use of the electric-field constrained design methodologies developed within the project, and also in leveraging efforts funded by the Office of Naval Research and the U.S. Department of Energy.

In 2020, the project devoted itself to the revision of the power-cell design, which had as its main task and goal the methodic design of its insulation system to achieve partial-discharge (PD)-free operation up to 30 kV. This was successfully demonstrated in the final prototype of the power-cell, which was used to create a manufacturing line that so far has produced 8 of the 16 total units that are needed. In conjunction with the ONR project developing the PEBB 6000, and the CPES mini-consortium on wide-bandgap, high-power converters and systems (WBG-HPCS), the project also concentrated in the development of a highly-synchronized digital communication and control network that achieved a sub-nanosecond synchronization accuracy. This control network is used to establish all communications between power-cells, which are hence fully isolated over the associated high-speed optical network. Similarly, an optical tightly-synchronized communication and control network was developed to establish all communications within the power-cells, including the main controller, enhanced gate-drivers and sensors. Lastly, the project developed the digital control architecture and also reduced to practice the digital control algorithms to implement the two novel fast-switching control schemes under evaluation in the project; namely the integrated capacitor-blocked transistor (ICBT) concept, and the CPES-developed switching cycle control (SCC).

In 2021 the project devoted itself to converter level testing, which by the end of the year had attained the operation in ICBT and SCC modes from an 18 kV dc bus using three power-cells per arm. In 2022 the project is expected to conclude its work by achieving 24 kV operation with four power-cells per arm.

High-Efficiency, SiC-Based, Flexible-CHP Interface-Converter With Advanced Grid-Support Functions

Sponsor: U.S. Department of Energy

Project Lead: Rolando Burgos

In this project, CPES in collaboration with Siemens, proposed to develop a modular, scalable MV power converter featuring stability-enhanced, grid-support functions for future F-CHP systems operating in small- to mid-size U.S. manufacturing plants being fully compliant with the IEEE Std 1547 and IEEE Std 2030.7. To this end, a modular circuit topology was adopted based on 10 kV SiC MOSFET devices, achieving an efficiency greater than 98 %, and a power density greater than 10 kW/L. As

such, the proposed converter will not just profit from the high-blocking voltage capability of these devices, but also from their inherent high efficiency and from their high-switching-frequency capacity. The latter will be enabled by a control scheme developed at CPES that can balance the converter capacitor voltages on a switching-cycle basis. Further, the voltage and current scalable capacity of the proposed converter will render it an appropriate solution for 1–20 MWe F-CHP systems, which typically operate in the 2–13.8 kV voltage range.

Modular, scalable MV power converter featuring stability-enhanced, grid-support functions for future F-CHP systems.

For demonstration purposes, a scaled-down modular power converter based on 1.7 kV SiC MOSFET devices, and rated at 480 V ac, 60 Hz, 200 kW, and 150 kVAr (±0.8 power factor), has been built and used to evaluate the converter operation and key performance metrics. The converter prototype will be evaluated using an Egston P-HIL test bed rated at 480 V and 250 kW, which will emulate both the CHP generator and the microgrid environment for the F-CHP. A Siemens SICAM A8000 microgrid controller will be connected to the P-HIL unit and to the converter prototype, and will be used to direct the operation of the emulated microgrid and to demonstrate the grid-support functionality of the converter in compliance with the IEEE standards in question.

The proposed converter and control system will be able to measure the grid and its own terminal impedance, which will allow it to implement the stability-enhanced grid support functions. Accordingly, the converter will be able to:

1. Operate in over-excited and under-excited reactive power generation mode
2. Participate in voltage regulation under constant power factor, voltage-reactive power, active power-reactive power, and constant reactive power modes, and also by adjusting its active power generation as a function of voltage
3. Respond to abnormal conditions
4. Participate in frequency regulation
5. Operate in and detect both unintentional and intentional islanding conditions
6. Monitor the grid stability conditions
7. Use grid-forming controls
8. Monitor the microgrid with the GPS-synchronized integral μPMU module

Prototyping and Evaluation of High-Speed 10 kV SiC MOSFET Power Modules With High Scalability and System-Integration Solutions

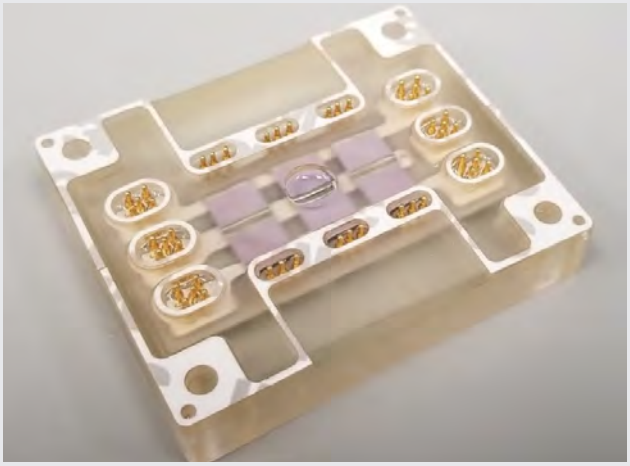
Sponsor: U.S. Department of Energy through PowerAmerica

Project Lead: Christina DiMarino

Wide-bandgap (WBG) power devices with voltage ratings exceeding 10 kV have the potential to revolutionize medium- and high-voltage systems due to their high-speed switching and lower on-state losses. However, present power module packages are limiting the performance of these unique switches. A high-density package for 10 kV silicon carbide (SiC) power MOSFETs has been proposed that achieves low and balanced parasitic inductances, resulting in a fast switching speed of 140 V/ns with negligible ringing and voltage overshoot.

The objective of this work is to evaluate the scalability, system integration, and reliability of the proposed 10 kV SiC power module. Power modules with multiple 10 kV die in parallel will be prototyped and tested to evaluate the current scalability of the proposed design. A compact system interfacing solution between the module and the

gate driver and bus bar that enables high-density, 10 kV-SiC-based power converters will be prototyped and undergo partial discharge testing. Accelerated testing will be employed to understand the failure mechanisms of the proposed 10 kV power module. Understanding these failure mechanisms will enable improved designs for use in high-reliability applications.



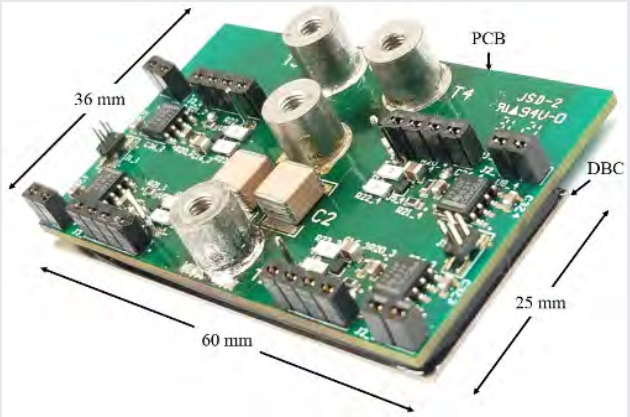
10 kV, 100 mΩ SiC MOSFET module with dimensions of 80 x 70 x 15 mm³.

SiC-Based Module Building Block With Integrated Coupled Inductor and Gate Driver

Sponsor: U.S. Department of Energy through PowerAmerica

Project Lead: Christina DiMarino

This work proposes to develop a 7–10 kW integrated power module building block (IMBB) consisting of a 1.2 kV SiC MOSFET full-bridge, PCB-winding coupled inductor, decoupling capacitors, and gate drivers. The IMBB can be flexibly arranged to form different power converter systems, such as dc-dc converters, and single- and three-phase rectifiers/inverters. To address the common-mode noise coming from the power stage, the balance technique will be implemented by integrating two additional inductors with the coupled inductor using a single core. Advanced packaging design will be used to minimize the parasitic inductance of the power and driving loops, enabling operating switching frequencies of 500 kHz–1 MHz, and to provide seamless integration with the coupled inductor, gate driver circuitry, and cooler. With interleaving control, the equivalent switching frequency at the input terminal will be 1–2 MHz. This high-switching frequency shrinks the size of the magnetics, thereby increasing the power density. State-of-the-art heat-spreading materials and cooling techniques will be used to effectively dissipate the heat from the SiC MOSFETs. Team members include Lockheed Martin and Infineon Technologies.



1.2 kV SiC MOSFET full-bridge with integrate gate driver.

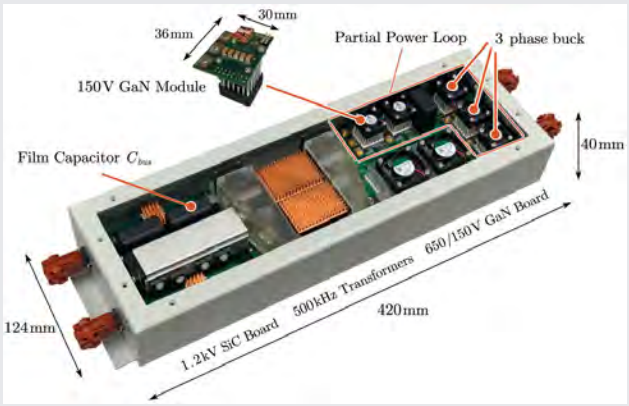
High-Efficiency Multiport Power Conversion for an All-Electric Transportation Refrigeration Unit

Sponsor: U.S. Department of Energy through PowerAmerica

Project Lead: Dong Dong

Partnered with Raytheon Technologies Research Center, CPES developed a high-power-density (>100 W/in³) and high-efficiency (>98.8 %) 20 kW bi-directional onboard dc-dc isolated converter for battery charging and bus-interface applications using SiC and GaN power semiconductors. The operating frequency is 500 kHz in order to minimize the isolation transformer. The project will adopt a new circuit topology using partial power processing to reduce the total device kVA rating and improve the efficiency. The solution adopted in the project will also provide fast and precise current and voltage regulation for pulse power applications.

The solution is considered an advanced technology insertion for next-generation battery chargers and bus-tie converter/breaker systems for future hybrid electric propulsion systems. The CLLC-type bi-directional resonant converter will be adopted to achieve zero voltage-switching (ZVS) throughout the complete operating range.



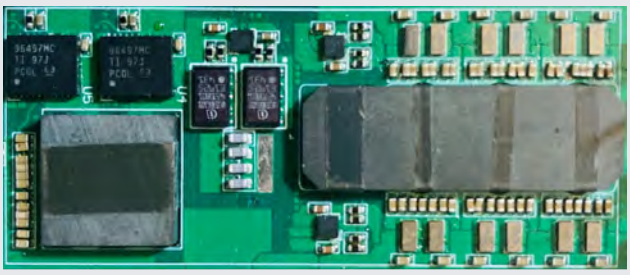
High-power-density (>100 W/in³) and high-efficiency (>98.8 %) 20 kW bi-directional onboard dc-dc isolated converter for battery charging and bus-interface applications.

High-Power-Density, High-Efficiency, and Wide-Range, GaN-Based 48 V-1 V, 300 A Single-Stage Converter

Sponsor: U.S. Department of Energy through PowerAmerica, Sub-Awardee of ABB

Project Lead: Qiang Li

The objective of this project is to demonstrate an efficient GaN-based, single-stage 48 V to processor point of load (POL) converter that occupies less than half the board space occupied by equivalent solutions today. The outcome of the project is a technical demonstrator that supports high-current CPU processors of a data center. The proposed system can provide more than 1000 W/in³ power density and 94.9 % peak efficiency. With high-power-density and efficiency, the proposed Sigma converter minimizes conversion and conduction loss, showing great potential for data center applications. In addition, a control method for the Sigma converter is proposed and verified through simulation and experiment. Results show that under wide input (40-60 V) and output (1.3-2.0 V) voltage ranges, a fast transient response can be achieved to meet VR13 transient response specifications.



160 A, 48 V/1.8 V converter with 95 % efficiency and 1100 W/in³ power density

100 kW SiC-Based Generator Rectifier Unit for Variable-Frequency Airborne Applications

Sponsor: U.S. Department of Energy through PowerAmerica

Project Lead: Rolando Burgos

CPES, in partnership with Raytheon and GE Aviation, developed a full SiC-based generator rectifier unit (GRU) rated at 100 kW and 600 V dc, designed to operate from a 200 V rms line-to-neutral, 400-900 Hz VFG, at an altitude of 50,000 ft. The GRU targeted a peak efficiency of 99 %, and a power density of 120 W/in³ (without accounting for electromagnetic interference filters), and sought to displace a Si-IGBT-based GRU rated at 85 kW, 600 V dc, with a 20 kHz switching frequency, and featuring a peak efficiency of 97 % and a power density of 80 W/in³. The GRU used SiC MOSFET devices from GE Aviation rated for 200 °C junction temperature operation, and packaged using GE's power-overlay technology. It employed liquid-cooling, operating at nominal power with a coolant temperature of 50 °C, and derated to 50 % with a coolant temperature of 75 °C. Its switching frequency was 70 kHz, allowing for a 3.5-times higher output voltage regulation bandwidth compared to the state-of-the-art unit. This increase in switching frequency allowed too for the reduction in the number of dc bus capacitors needed, further improving power density. A key design challenge was the high altitude requirement, as it affected both the insulation design of the inverter unit and its ancillary systems as well as the cooling systems due to the thin air constraints. To this end, CPES conducted an electric-field-oriented design of all the GRU components, finally qualifying its operation in a high-altitude chamber. The GRU was extensively tested at nominal power conditions and delivered to Raytheon for additional testing.

High-Efficiency, Medium-Voltage-Input, Solid-State-Transformer-Based 400 kW/1000 V/400 A, Extreme Fast Charger for Electric Vehicles

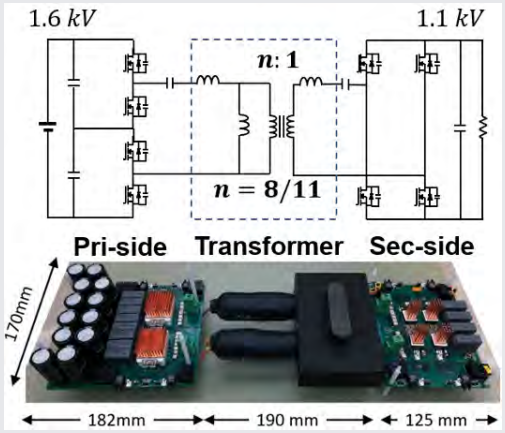
Sponsor: U.S. Department of Energy, Sub-Awardee of Delta Products Corporation

Project Lead: Qiang Li

CPES is working with Delta Products Corporation, General Motors, DTE Energy, Next Energy, Michigan State Energy Office, and the City of Detroit Sustainability Office to deliver a novel, efficient, compact, and scalable solid-state-transformer (SST)-based 400 kW extreme fast charger (XFC). The proposed system will also provide a user-friendly dc interface to renewable energy generation systems (e.g,. PV) and energy storage systems (ESS),

resulting in less disturbance to the existing grid. This is the enabling technology for large-scale XFC deployment. It will also accelerate electric vehicle (EV) market penetration and promote renewable energy usage.

The proposed 400 kW/1000 V/400 A XFC consists of two main function blocks: an SST and a charger converter. The SST takes a 13.2 kV ac medium-voltage (line-to-line) and converts it to a 1 kV-intermediate dc bus voltage. The charger converter converts the 1 kV dc bus into the controllable dc-output voltage to charge an EV. The 1 kV intermediate dc bus is designed to interface with external renewable energy generation systems (e.g., PV) and ESS for load shaving and minimizing demand charges. The bulky line frequency transformer (LFT) is eliminated in the proposed SST-based XFC system.



15 kW dc-dc building block with 99 % efficiency for 13.2 kV solid-state transformer system.

Low-Cost, Rare-Earth-Free Electric Drivetrain Enabled by Novel Permanent Magnets, Inverter, Integrated Design and Advanced Thermal Management

Sponsor: U.S. Department of Energy, Sub-Awardee of Marquette University

Project Lead: Dong Dong

To achieve significant EV market penetration, e.g., 10 percent by 2025 and 35 percent by 2040, electric propulsion drive system cost and size will need to be reduced in addition to a continued reduction in energy storage costs. This will in turn allow for easier integration of electric traction drive systems and favorable economics, resulting in a greater number of both passenger and light truck EVs.

Using GM's commercial Bolt™ light-weight EV IGBT-based traction drive system as the benchmark and demonstration platform, this project seeks to demonstrate a liquid-cooled, 200 kW, three-phase, highly integrated, full-SiC high-speed electric propulsion drive, with 800 V operating dc-voltage, and a minimum of 20 kHz switching-frequency. The proposed solution will adopt the heavy-duty, bus-bar-embedded printed-circuit board (PCB) with integrated digital gate-driver, double-sided cooling, embedded current sensing, and PCB EMI filters solution to significantly reduce the OEM component count, which simplifies the mechanical structure and assembly process, as well as leverages low-cost electronics components. The power density target is >30 kW/L, almost twice the number of the 2025 U.S. Department of Energy target, and peak power efficiency target is >98.5%. The cost savings are driven by overall mechanical and integration platform cost reduction thanks to high-power-density, hydraulic system and heat-exchanger reduction due to high efficiency, more automated assembly, and component savings by the highly-integrated, multi-functional heavy copper PCB bus solution.

Resiliency Enhancement of Cyber-Microgrids and Microgrid Building Blocks

Sponsor: U.S. Department of Energy, Sub-Awardee of Pacific Northwest National Laboratory

Project Lead: Igor Cvetkovic

In close collaboration with the Power and Energy Center at VT, CPES has been conducting a conceptual study of a microgrid building block (MBB) – a bi-directional power electronics converter serving as a main tie between a microgrid and a utility. The microgrid example resembling the existing Virginia Tech Electric Service power plant is modeled and simulated to demonstrate the functionality enhancement achieved with the addition of a bi-directional power electronics converter named a microgrid building block, cyber-physical system, which features standardized power, control, and communication interfaces. This concept significantly simplifies (and standardizes) microgrid nesting, while providing dynamic decoupling from the utility. It further enables multiple microgrids to operate independently and coordinate operation even when the main grid is not present, thus enhancing the resiliency. Not only can MBB interfaced microgrid operate an islanded mode for a given time determined by available power from local energy generation and storage, but it also brings an advanced protection, black-start capability, fast resynchronization, low-voltage ride-through, and a sub-millisecond response functionality. Additionally, the concept of a MBB is important toward modularization of microgrids for wide deployment in the power grid. The VT

team involved in this project will also study a broader set of cyber system events and their impact on the resiliency of the microgrid system.

Intelligent Power Stages

Sponsor: Oak Ridge National Laboratory

Project Lead: Rolando Burgos

Supporting Oak Ridge National Laboratory's (ORNL) effort to develop future solid-state transformers by building and demonstrating their building blocks, namely intelligent power stages (IPSs) featuring advanced power conversion and control functionalities, CPES is developing a three-phase, ac-dc-dc IPS unit rated at 50 kW and 75 kVAr (75 kVA), utilizing SiC devices to achieve an efficiency >98 %, and a power density > 10 kW/L.

The proposed IPS topology has a three-phase, ac-dc input terminal and a dc-dc output stage using a three-level, buck-boost, dc-dc converter for minimized electromagnetic interference (EMI) emissions. The IPS will in addition demonstrate: interoperability, grid and fault monitoring capacity, integrated modular filter building blocks (FBB), operational diagnostics and prognostics, electromagnetic compatibility (EMC)-enhanced intelligent gate-driving with integrated sensors, EMC-enhanced intelligent sensors, EMC-enhanced auxiliary power supply network, and fiberoptic-based control, sensor, and communication networks.

Modeling, Analysis, and Simulation of Large-Scale Power Electronics-Based Power Grids

Sponsor: Oak Ridge National Laboratory

Project Lead: Dong Dong

Oak Ridge National Lab is partnering with the Center for Power Electronics Systems (CPES) to investigate system modeling and simulation and stability analysis of a new power-electronics based-power system architecture, namely resilient all-power electronics grid (APEG). The goal of the program is to explore a new modeling and simulation approach, which can provide significantly better simulation speed and accuracy than state-of-the-art EMT-based simulation software used in the power system community.

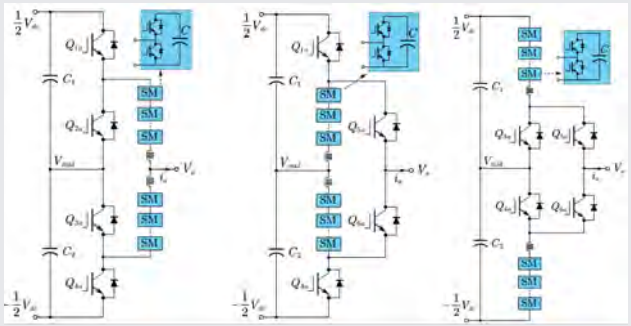
SiC Three-Level Hybrid Modular Multilevel Converter (THMMC) for Medium-Voltage Power Conversion Applications

Sponsor: National Science Foundation

Project Lead: Dong Dong

Accessing renewable energy and energy storage from the grid, e.g., solar, wind, and batteries, inevitably requires high-efficiency, solid-state power conversion solutions. The industry is moving toward medium-voltage (MV) solutions, which can directly access the MV grid, to reduce bulky transformers, cables, and cost/kVA of the converters. First published in 2003, the modular multilevel converter (MMC) technology immediately gained in popularity and became a de-facto benchmark system in MV to HV voltage-source converters (VSC). However, MMC still has many limitations.

This work explores a new family of modular-oriented MV multilevel converters, "hybrid modular multilevel converter (HMMC)". The proposed concept leads to important topology variations. For instance, the diode-based HMMC (DHMMC) rectifier provides a significant cost and total system size saving and efficiency improvement. SiC devices can be used in the proposed solutions to synthesize high-fidelity ac output. This NSF funding will support the PIs to perform detailed fundamental research on this family of solutions and to develop a set of fundamental modeling, control, and design solutions, paving the path for industry adoption as well as train students in MV power electronics and MMC systems.



Schematics of three hybrid modular multilevel converter (HMMC) topologies being studied.

Faculty Early Career Development Program (CAREER) Award

Career Award: High-Frequency Integrated Voltage Regulator to Support Dynamic Voltage and Frequency Scaling for Mobile Devices

Sponsor: National Science Foundation

Project Lead: Qiang Li

Voltage regulators have been widely used in computing systems to deliver power from energy sources such as batteries to microprocessors. Today's voltage regulator is usually constructed using discrete components and assembled on the motherboard. Discrete passive components such as inductors and capacitors are bulky and occupy a considerable footprint on the motherboard. Furthermore, the power delivery path from the voltage regulators to the microprocessors is relatively long. Recently there has been great demand for a very high-frequency integrated voltage regulator that can be placed very close to the microprocessor to support dynamic voltage and frequency scaling, which is a very effective power consumption reduction technique for microprocessors. This enables the supply voltage to change dynamically according to the microprocessor workload (decreased workload leads to a lower supply voltage; and a lower supply voltage also leads to a lower clock frequency). As a result, both the dynamic and static power consumption of the microprocessor can be greatly reduced. However, the traditional discrete voltage regulators are not able to realize the full potential of dynamic voltage and frequency scaling since they are not able to modulate the supply voltage fast enough, due to the high parasitic interconnect impedance between the voltage regulators and the microprocessors.

This project focuses on developing a 20-50 MHz, three-dimensional, integrated voltage regulator for mobile devices, such as the smartphone. The proposed research will have a significant impact on power management solutions for smartphones as well as other mobile applications. It will help make the integrated voltage regulator a feasible approach to significantly reduce mobile device power consumption, which will greatly extend battery life and reduce electricity consumption. Proposed education activities also include outreach to K–12 and underrepresented groups to increase the attractiveness of power electronics.

Career Award: Nitride FinFET on Silicon for Medium-Voltage Monolithically-Integrated Power Electronics

Sponsor: National Science Foundation

Project Lead: Yuhao Zhang

Medium-voltage (600-1700 V) power devices are key for efficient power conversion in electric vehicles, solar farms, and power grids among other applications. They are among the fastest-growing sectors in the $40 billion power semiconductor market. Today's medium-voltage devices are mainly made of silicon (Si) and silicon carbide (SiC), while gallium nitride (GaN) has superior physical properties over Si and SiC for power applications. Recently, the vertical GaN power FinFET, a new power transistor utilizing sub-micron-meter fin channels, has demonstrated one of the best performances in all medium-voltage transistors. However, all existing vertical GaN FinFETs employ small-diameter and high-cost GaN substrates, which hinders their commercialization.

This proposal aims to develop a new generation of medium-voltage vertical GaN power FinFETs on low-cost, large-diameter Si substrates with high performance, and fabricating them on the same wafer with the low-voltage lateral GaN FinFETs or tri-gate transistors, such to allow the monolithic integration of the driving circuitry and medium-voltage power devices for the first time. This project, if successful, will enable an unprecedented advancement in the performance, frequency, efficiency, and form factor of the medium-voltage power electronic systems.

This project also provides wide opportunities for student education and outreach, with an emphasis on the advising of underrepresented and minority students:

1. Establishing an integrated undergraduate research program that tackles interdisciplinary problems in the fields of materials, devices, and power electronics
2. Mentoring the participating students with the industrial collaborators and promoting the student interactions with the power semiconductor industries
3. Contributing to the pre-college summer camps and providing summer research opportunities to K-12 students and teachers, to promote their participation in microelectronics and power electronics research

Cybermanufacturing of Wide-Bandgap Semiconductor Devices Enabled by Simulation-Augmented Machine Learning

Sponsor: National Science Foundation

Project Lead: Yuhao Zhang

The semiconductor industry is one of the largest manufacturing sectors with annual revenue approaching $500 billion. Semiconductor devices are manufactured on large-diameter wafers through multiple process steps. Yield is a key metric determining the success in semiconductor manufacturing. The current practice of yield management relies on minimizing the wafer material non-uniformity, maximizing the process control in every step, and applying necessary process adaptions to the entire wafer-based on domain expertise. However, the manufacturing yield of emerging semiconductor devices, e.g., wide-bandgap (WBG) devices, is merely 50-80 % in the foundry, due to less mature materials and processes. While WBG devices are gaining quick adoption in applications like electric vehicles, data centers, 5G communications, and power grids, the limited yield of their manufacturing has become an increasingly serious concern.

This project proposes the self-predictive and self-adaptive cybermanufacturing of semiconductor devices implemented through die- or device-based (instead of wafer-based) adaptions in each process step guided by a physical simulation-augmented machine-learning (ML) framework. In this semiconductor cybermanufacturing, which does not exist today, device-to-device adaptions in geometrics and designs are applied in each process step to intelligently compensate for the variability in inherent material properties and historical process steps. This seed grant will use the small-scale fabrication of WBG power diodes as a demonstration vehicle to establish the knowledge base related to the integration of ML in adaptive semiconductor manufacturing. The new manufacturing paradigm can potentially lead to the formation of new industries at the intersection of ML and semiconductors. This project also presents a unique venue to train future technicians with the capabilities of tackling interdisciplinary problems in ML-guided semiconductor manufacturing. This interdisciplinary project will be utilized to support undergraduate research activities and outreach activities for K-12 students.

Nitride Super-Junction HEMTs for Robust, Efficient, Fast Power Switching

Sponsor: National Science Foundation

Project Lead: Yuhao Zhang

Power semiconductor devices are utilized as solid-state switches in power electronic systems that are ubiquitous in consumer electronics, data centers, electric vehicles, electricity grid, and renewable energy systems. The global power device market exceeded $15 billion in 2019 and is fast growing. Gallium nitride (GaN) high-electron-mobility transistors (HEMTs) are widely perceived as the next generation of power devices. Despite their initial commercialization recently, their wide adoption in industrial applications is hindered by the limited reliability and robustness, which in turn, requires considerable overdesign, rendering device performance far below the material limit.

This project will develop a new generation of robust, charge-balanced GaN HEMTs through innovation in the semiconductor materials and device structure. Interdisciplinary research will be carried out in materials, devices, processing technologies, and circuit-level tests through a collaboration between Virginia Tech and the University of Southern California. The research activities will also involve collaboration with Cambridge University in the United Kingdom. This US-UK collaborative project provides wide opportunities for student education and international exchange, development of cross-university teaching modules, and industrial collaboration for potential technology transfer. This interdisciplinary, cross-continent project will also be utilized to support outreach activities for K-12 students and teachers and promote the educational activities related to microelectronics and power electronics technologies.

High-Temperature Ultrawide-Bandgap Gallium Oxide Power Module

Sponsor: National Science Foundation

Project Lead: Christina DiMarino

There is a compelling need for power electronic components and systems capable of operation at ambient temperatures exceeding 250 °C. However, these extreme temperatures challenge the fundamental limit of silicon devices, and wide-bandgap power semiconductors show diminished performance benefits at high temperatures. Gallium oxide (Ga_2O_3), an ultrawide-bandgap semiconductor, is emerging as a viable candidate for high-temperature power electronics. While Ga_2O_3 power devices

have shown promising high-temperature stability, package advancements at temperatures above 200 °C are limited.

This work has four main research goals:

1. To develop an electro-thermal, device-package co-design framework that will enable physical insights into the device-package interdependencies, and accelerate the design of power modules optimized for emerging power semiconductors
2. To evaluate and apply new dielectric materials for use as the high-temperature power module encapsulant
3. To explore innovative heat dissipation strategies at the device and package levels for improved thermal performance of Ga_2O_3-based power modules
4. To demonstrate the first 300 °C, 1.2 kV, 20 A Ga_2O_3 fin power field-effect-transistor (FinFET) half-bridge module, and assess its electrical, thermal, and reliability characteristics

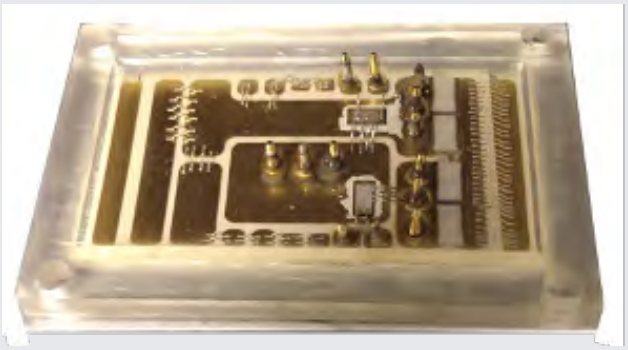
The knowledge gained from this work will showcase the potential of Ga_2O_3 power devices, and enable significant advancements in high-temperature packaging, which could enable more efficient and higher-density electric transportation and harsh-environment systems.

Evaluation of Electromagnetic Interference Mitigation Strategies for High-Voltage, Wide-Bandgap Power Modules

Sponsor: Army Research Laboratory

Project Lead: Christina DiMarino

Wide-bandgap (WBG) power devices with voltage ratings exceeding 10 kV have the potential to revolutionize medium- and high-voltage systems due to their high operating voltage and high-speed switching. However, the benefits of these unique switches are also their main barriers to adoption. In particular, the high-switching speed can cause significant electromagnetic interference (EMI), voltage overshoot, and ringing. While it has been shown that the latter can be mitigated by low-inductance packaging, the former remains a major challenge. Current EMI mitigation solutions involve adding common-mode (CM) chokes and EMI filters at the converter and system levels. To reduce these external filtering requirements, CPES has demonstrated a 10-kV SiC power module with an integrated screen, which reduces the CM current that is generated by the fast voltage transients, while simultaneously increasing the partial discharge inception voltage by more than 50 %. Through systematic experimentation, a better understanding of how to design packages to mitigate EMI effects on the system can be achieved. The knowledge gained from this work will contribute to new design criteria for low-EMI WBG packages. Reducing the negative impacts of high-speed switching on the system is essential to mitigating the risk of high-voltage WBG devices without sacrificing performance.



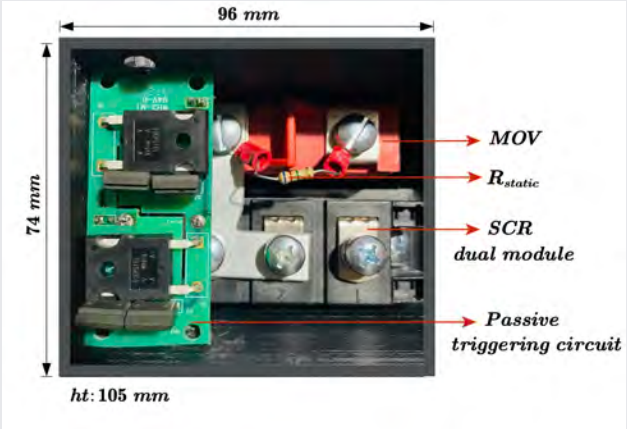
1.2 kV SiC MOSFET module with integrated common-mode screen.

Modeling and Design of a Solid-State Circuit Breaker

Sponsor: Naval Postgraduate School

Project Lead: Dong Dong

CPES will investigate the design trade-off of the energy dissipation circuit (EDC) used for a modular, bi-directional, solid-state-based circuit breaker. The project will design and implement a novel EDC concept, namely "electronic-MOV (eMOV)" to address the drawbacks of the traditional MOV-based EDC, such as ratio between clamping voltage and operation voltage. The proposed eMOV technology can help reduce the conduction loss by up to 30 % in a 2 kV dc-system.



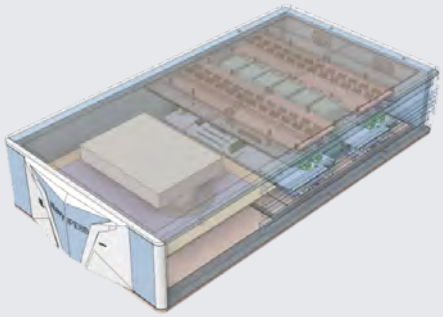
Modular, bi-directional, solid-state-based circuit breaker with electronic-MOV (eMOV).

Development of the iPEBB 1000, a 1.7 kV SiC MOSFET-Based Integrated Power Electronics Building Block

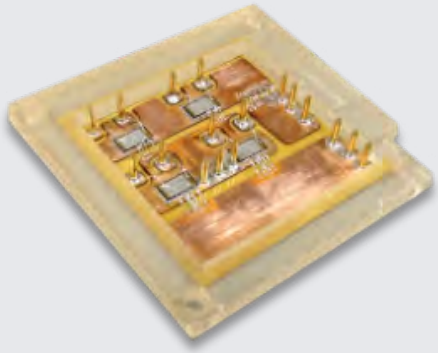
Sponsor: Office of Naval Research

Project Lead: Christina DiMarino

The advancement of SiC power semiconductor devices allows for higher-power and faster-switching converters. This work aims to design a 250 kW integrated power electronics building block (iPEBB) for shipboard power systems. The galvanically-isolated iPEBB can be stacked in series and parallel to scale the voltage and power and can be used for ac or dc operation. At the core of the iPEBB is a common substrate that provides the power distribution, circuit interconnections, mechanical support, heat spreading, and interface to the cooling system. State-of-the-art organic, direct, bonded copper (ODBC) substrates are evaluated in this work. Multi-domain simulations are used to design the integrated SiC bridges to achieve the optimal tradeoff between power-loop inductance, device junction temperature, and converter weight. For the galvanic isolation, a 500 kHz transformer with 20 kV isolation has been developed using a unique insulating design. This work will help advance the development of a lightweight, flexible iPEBB to serve as the backbone for shipboard power systems.



250 kW, 500 kHz integrated power electronics building block (iPEBB).



1.7 kV SiC MOSFET module with organic DBC substrate.

Electric Ship Research and Development Consortium

Sponsor: Office of Naval Research

Project Lead: Igor Cvetkovic

CPES continues to be a part of a multi-university consortium with the goal of supporting the Office of Naval Research work in the domain of fundamental research that can consequently advance electric ship concepts. Going beyond initial CPES-developed solutions in the area of EMI suppression and containment strategy for power electronics building blocks (PEBBs) featuring high dv/dt-SiC MOSFET devices, this program will continue the development of a more systematic approach to understand and accurately model high-frequency behavior of PEBBs and PEBB-based converters. Furthermore, CPES will continue focus on development of ultra-fast distributed control addressing not only inter-PEBB communication and synchronization strategy, but also intra-PEBB-distributed control utilizing White Rabbit precision-time protocol (PTP). Focus will also continue on the development of hierarchical modeling and multidisciplinary set-based design methodology for shipboard-distributed power systems focusing on electromechanical and thermal models that can effectively capture the interrelationships and interdependencies of the electrical, mechanical, and thermal domains. Finally, a development of a PEBB-based Energy Magazine Testbed for System-Level Demonstration will be carried out to aid system-level studies and provide a validation platform for the above-described research tasks. The testbed will be designed to include PEBBs under development at CPES, including multiple passive and electronic dc and ac electronic loads.

Power Electronics Power Distribution Systems (PEPDS) for Future Navy Ships

Sponsor: Office of Naval Research (ONR)

Project Lead: Igor Cvetkovic

In order to support new power, energy, and control power-electronics, power-distribution systems (PEPDS) distribution concept enabled by ONR-developed technology, CPES has been putting an effort into the modeling and simulation of PEBB-based converters for system-level PEPDS architecture studies, performance evaluation, and stability enhancement. Both PEBB concepts, an isolated topology called Navy iPEBB featuring all bridges on a common substrate, and non-isolated H-bridge with 6000 V dc link will be modeled with a different level of details to allow multiple levels of abstraction from a detailed switching model, via average to simplified system-level

terminal behavioral models. These models will enable study and analysis of power electronics-dominated distribution system architectures, and additionally "set the ground for" energy transfer protocols for future Navy ships utilizing PEBB and Navy iPEBB-based Electronic Energy Routers. This work will further support technology advances and developments in the domain of fast SiC-based converters and provide the modeling capabilities needed to employ them in system-level studies as well as to demonstrate enhanced operation of modern Navy shipboard electrical systems.

Development of the PEBB 6000 Using Gen3 10 kV, 240 A SiC MOSFET Modules in Full-Bridge Configuration

Sponsor: Office of Naval Research (ONR)

Project Lead: Rolando Burgos

Under the sponsorship of ONR, CPES developed and demonstrated the operation of the first SiC-based power electronics building block (PEBB) rated at 6 kV in 2015, utilizing the second generation 10 kV, 120 A, SiC MOSFET half-bridge modules from Cree/Powerex/GE. Later, CPES initiated the development of the critical ancillary circuitry needed to operate medium-voltage (MV) power converters at high-switching frequencies, efforts started by the ONR-funded development of enhanced gate-drivers for these 10 kV devices, and for the auxiliary power system needed to power controllers, sensors, and the gate-drivers themselves. In 2018, CPES commenced the development of the full-bridge PEBB 6000, using Gen 3 10 kV SiC MOSFET modules from Wolfspeed 240 A, rated at 1 MW, 6 kV and 20 kHz, targeting a power density of 10 MW/m^3, 99 % efficiency, minimum EMI emissions, a 30 kV partial discharge inception voltage (PDIV), and a 0 V enclosure potential. This program has approached its end and is readying to test the final PEBB 6000 prototype that achieved a power density of 20 MW/m^3, 99.5 % efficiency, with minimized EMI emissions, and 30 kV PDIV rating. These tests are expected to be conducted by March 2022.

Medium-Voltage Nitride Power Switches Enabled by Vertical Superjunction Technology

Sponsor: Office of Naval Research

Project Lead: Yuhao Zhang

One of the main objectives in the design of power devices is to obtain a high off-state breakdown voltage (VB) while minimizing the on-state resistance (Ron). Power devices are limited by the trade-off between VB and Ron. A vertical superjunction (SJ) device, which consists of alternative p-type and n-type pillars, could break the theoretical limit of conventional 1-D power devices, and achieve over 10-fold lower Ron than conventional power devices for the same VB at the same time that the capacitances and charges are significantly reduced, allowing for a megahertz switching frequency in kilovolts switching. The material cost can be also reduced.

In this five-year project, Virginia Tech, working with Qorvo, will pursue coordinated efforts to realize the medium-voltage vertical GaN superjunction technologies. This will initially focus on the demonstration of 1.2-1.7 kV prototypes, then scaling to 3.3-10 kV. Two technical approaches will be pursued to fabricate vertical GaN superjunction. This team will also participate in the GaN Superjunction working group established by the U.S. Naval Research Laboratory (NRL). Specific collaborations will include:

1. A joint effort with NRL to develop the approach utilizing their expertise in p-type dopant activation and epitaxial regrowth, as well as obtain thick drift layers with low background impurity utilizing their state-of-the-art GaN metal organic chemical vapor deposition (MOCVD) reactors
2. Joint studies with Penn State University (PSU) to understand processes, defects, and interfaces that are common to both the lateral and vertical GaN superjunction structures

Southwest Virginia Node Research Funding

Sponsor: Virginia Commonwealth Cyber Initiative

Project Lead: Igor Cvetkovic

In an effort to support positioning Virginia as a global center of excellence at the intersection of security, autonomous systems, and data CPES started a study on deployment of 5G networks within electronic power systems that can provide advanced communication capabilities and enhance operation of electrical systems in nanogrids and microgrids. Special emphasis will be put on real-time clock synchronization between system nodes at a microsecond accuracy, enabling network transfer of time-stamped, addressed variables with a millisecond latency. CPES's initial focus has been use of a White Rabbit precision time protocol (PTP) over a 5G network to synchronize clocks in the all-power-electronics systems that could potentially eliminate phase-locked loops in the converter control. This concept also has promising advantages for protection coordination, which will be explored later in the project.

Developing the Future of Wide-Bandgap Power Electronics Engineering Workforce – Wide-Bandgap Generation (WBGen) Fellowship Program

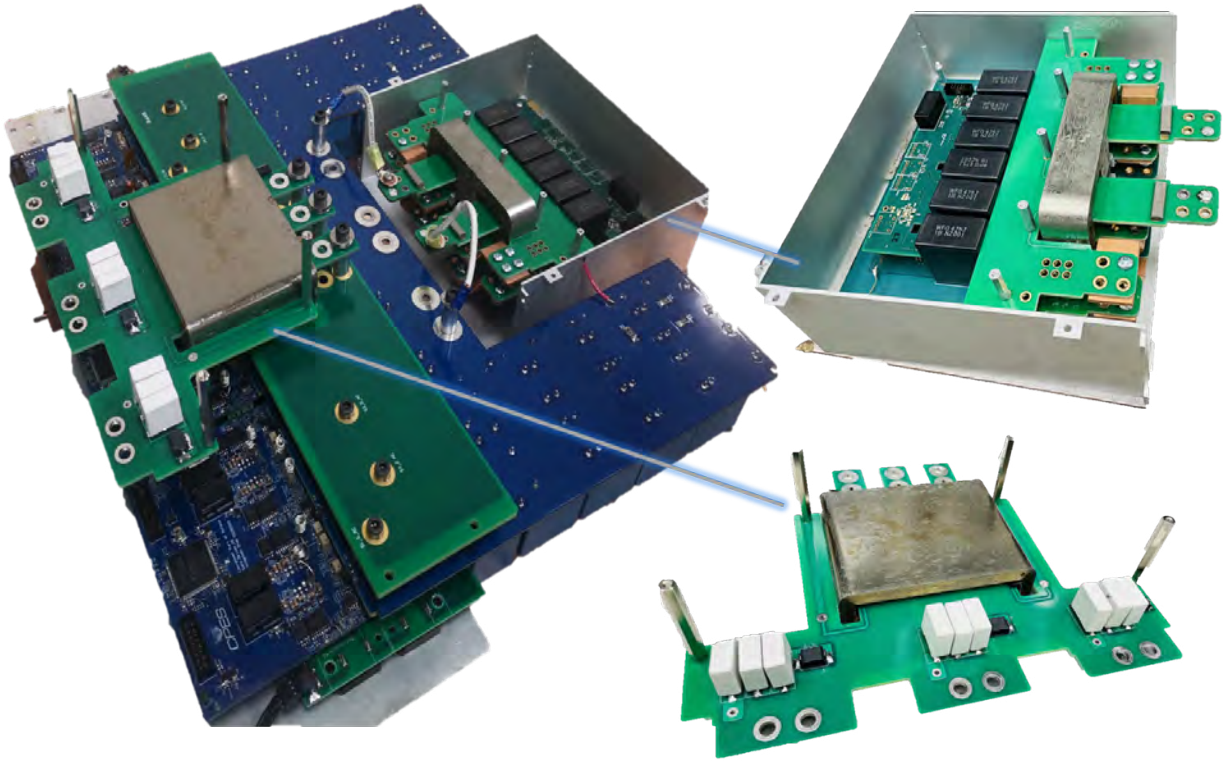
Sponsor: U.S. Department of Energy

Project Lead: Rolando Burgos

The goals of the Wide-Bandgap Generation (WBGen) fellowship program sponsored by the U.S. Department of Energy (DOE) are:

1. To train the next generation of U.S. citizen power engineers with wide-bandgap (WBG) power semiconductor expertise aiding in fulfilling future workforce needs in this field
2. To broaden the range of WBG-based power electronics by conducting research and development on high-efficiency grid apparatus and high-efficiency electrical power systems
3. Enhance the power engineering curriculum by formalizing WBG-oriented design procedures for power electronics components and systems that can effectively integrate the inherent, challenging material characteristics of these devices, which have effectively rendered design procedures for silicon-based power electronics obsolete

The WBGen fellowship has funded a total of 24 fellows since its inception in January 2016, of which 2 PhD students have transitioned into other CPES programs, and 15 MS students have joined industry so far. 2022 should see 3 more MS students successfully graduate from the program. This has had an immense impact on the success of the WBG research programs at Virginia Tech, and is already having measurable positive effects on the power engineering workforce in the U.S. Furthermore, DOE laboratories and numerous CPES industrial partners have also benefited significantly from the interaction with the participating graduate students, cementing what are already strong relationships between the partners and CPES, and creating a solid network of power engineering training, research, and development. These partnerships have involved ABB Inc., General Motors, United Technologies Aerospace Systems, United Technologies Research Center, Raytheon Technologies Research Center, HRL Laboratories, National Renewable Energy Laboratory, Oak Ridge National Laboratory, Dominion Energy, Rockwell Collins, General Electric, Synopsys, Otis, Lockheed Martin, Newport News Shipbuilding, Nissan, Office of Naval Research, VPT, Egston, Carrier, and the PowerAmerica Institute.



Intellectual Property

INNOVATIONS SHARED

U.S. Patents Awarded (All patents awarded available to IP Sharing.)

VTIP 18-123 | US PATENT 10,886,860
Issued January 5, 2021

Three-Phase, Three-Level Inverters and Methods for Performing Soft-Switching With Phase Synchronization
Nidhi Haryani, Sungjae Ohn, Rolando Burgos, Dushan Boroyevich

VTIP 16-109 | US PATENT 10,910,140
Issued February 2, 2021

Matrix Transformer and Winding Structure
Chao Fei, Fred C. Lee, Qiang Li

VTIP 19-114 | US PATENT 11,171,203
Issued November 9, 2021

High-Electron Mobility Transistors With Charge Compensation
Yuhao Zhang

U.S. Patents Filed (All pending patent applications available to IP Sharing.)

VTIP 20-108 | Filed January 21, 2021

Soft-Switched, Series Capacitor, Buck Converter
Cong Tu, Khai Ngo, Ting Ge, Rengang Chen (Texas Instruments)

VTIP 21-056 | Filed March 12, 2021

Multiphase, Integrated, Coupled Inductor Structure
Feiyang Zhu, Qiang Li, Fred C. Lee

VTIP 21-054 | Filed March 24, 2021

Planar Omnidirectional Wireless Power Transfer System
Junjie Feng, Qiang Li, Fred C. Lee

VTIP 21-067 | Filed March 25, 2021

Coupled Inductor Winding Structure for Common-Mode Noise
Shuo Wang, Fred C. Lee, Qiang Li

VTIP 21-058 | Filed April 29, 2021

Power Schottky Barrier Diodes With High-Breakdown Voltage and Low-Leakage Current
Yuhao Zhang, Ming Xiao

VTIP 21-094 | Filed July 19, 2021

Hybrid, Modular, Multilevel Converter Topologies Using Half-Bridge Submodules
Jian Liu, Dong Dong, Rolando Burgos

VTIP 21-090 | Filed August 19, 2021

Sealed Interface Power Module Housing
Christina DiMarino, Dushan Boroyevich, Rolando Burgos, Christopher Mark Johnson (University of Nottingham), Mark Carnie

VTIP 21-115 | Filed September 17, 2021

Line Frequency, Commutated, Voltage Source Converters for Multiphase, Modular, Multilevel Converters
Jian Liu, Dong Dong

VTIP 22-033 | Filed October 21, 2021

Three-Phase LLC Converters With Integrated Magnetics
Rimon Gadelrab, Fred C. Lee

VTIP 21-129 | Filed October 27, 2021

High-Current DC-DC Converter With Integrated Matrix Transformer and Multiphase Current Doubler Rectifier
Xin Lou, Qiang Li, Fred C. Lee

VTIP 21-122 | Filed November 5, 2021

Charge-Balanced Power Schottky Barrier Diodes
Yuhao Zhang, Ming Xiao

VTIP 22-040 | Filed November 19, 2021

Scalable Voltage-Balancing, Circuit-Based, Non-Isolated, High-Step-Down-Ratio Auxiliary Power Supply
Keyao Sun, Rolando Burgos, Dushan Boroyevich

Facilities

WORLD-CLASS INFRASTRUCTURE

The Center headquarters are located at Virginia Tech, occupying office and lab facilities encompassing more than 20,000 square feet of space in one building. Research space at CPES-VT includes an electrical research lab, an integrated packaging lab, and a computer lab. In addition to the headquarters labs and offices, a large conference room with voice- and video-conferencing capabilities supporting remote site course instruction, as well as interaction among CPES collaborators, is maintained. Interactive collaboration is routinely facilitated through conference calls, GoToMeeting and Zoom online conferencing, student and faculty exchanges, and face-to-face research project review meetings.

National Capital Region Laboratory

CPES's expansion into Northern Virginia includes state-of-the-art power electronics and packaging laboratories that are well-suited to continue building upon CPES's internationally-recognized expertise in developing groundbreaking power electronics technologies. The power electronics lab opened for the spring semester of 2019, and is located on the fourth floor of the Virginia Tech Research Center in Arlington, Virginia, occupying more than 1,800 square feet of space. Equipped with the latest testing and measurement equipment capable of achieving several hundreds of kilowatts of power, the lab provides an environment for unparalleled hands-on experience for graduate students and visiting scholars. The packaging laboratory is equipped with state-of-the-art equipment for designing, building, characterizing, and testing advanced power electronics packages. These new labs contribute to Virginia Tech's expanding presence in Northern Virginia.

Electrical Research Laboratory

The Electrical Research Laboratory is equipped with state-of-the-art tools and equipment for development of power electronic circuits and systems of all sizes, from sub-volts, sub-watts to 6 kV, 1 MW. It also includes PWB manufacturing equipment, an EMI chamber, a clean room, and a mechanical shop. Each student bench is equipped with Dell computers with up to 32 GB of RAM for running complex simulations.

Standard instrumentation includes GHz oscilloscopes, multi-channel function generators, electronic loads, low- and high-voltage passive and differential probes, network, spectrum, impedance, logic, and power analyzers, thermal sensors, and ac-dc bench supplies of all sizes. Specialized test room equipment includes thermal imaging, a Hi-Pot tester, a 3D magnetic field scanner, an EMI/EMC analyzer, large and small dynamometers, automatic circuit board routing equipment, magnetic core loss testing, programmable and variable loads, and a liquid-cooled heat exchanger.

National Capital Region Laboratory

Integrated Packaging Lab

Integrated Packaging Lab

The Integrated Packaging (IP) Lab supports all CPES students, faculty, visiting scholars, and sponsors for their advanced needs in power electronics packaging research. The lab was established to create and evaluate alternative approaches to the design and manufacture of Integrated Power Electronics Modules (IPEMs) and provide state-of-the-art electronic manufacturing and assembly equipment. The IP lab itself has installed a sealed ceiling and HEPA filtration to create over 1,600 square feet of class 10,000 clean room space. It has the capability to produce FR4, DBC, and thick film hybrid substrates, perform metallization using RF sputtering thin film deposition and electro- and electro-less plating, and develop substrate patterns by virtue of laser ablation machining, chemical metal etching, and screen printing. New this year is a chamber for high-altitude testing.

The IP lab also has the ability to mount bare dies and SMT components using a high-precision pick-n-place machine, a solder reflow belt furnace, and a convection reflow oven. The vacuum solder reflow system provides another technical solution for die-attachment in a flux-less, void-less process. Device attachment reliability is tested with the Dage 4000 Die shear equipment.

State-of-the-art device characterization equipment can also be found in the IP lab. This includes a Keysight B1505A curve tracer that is rated at 10 kV and 1500 A, a Form Factor probe station with a gold thermal chuck, and ATT system's thermal controller/chiller to give the ability to test bare die from -30 °C to 300 °C. The thermal chiller runs solely on air, which is provided by a 7.5 hp Ingersoll Rand air compressor.

The wire bonding machines equipped in the IP lab provide interconnect options of heavy aluminum wire bonding, gold wire ball bonding, and aluminum/gold ribbon bonding for manufacturing IPEMs. For accurate and controlled dispensing of adhesives and encapsulants, an automated precision dispensing system is in the lab. In addition, the IP lab has full capability for low-temperature, co-fired ceramic (LTCC) processing from tape cutting, via drilling, screen printing, laminating, to co-firing. The components and module-level test and evaluation of electrical, thermal, and reliability performance for the assembled IPEMs are also available in the IP lab. Thermal performance evaluation can be made by the setup of thermo-couples, optic-fiber sensors, IR imaging, and the thermal diffusivity test system. Reliability analysis is performed using a multi-purpose bond tester on as-made modules and ones after certain numbers of temperature/humidity cycling.

High-Power Lab

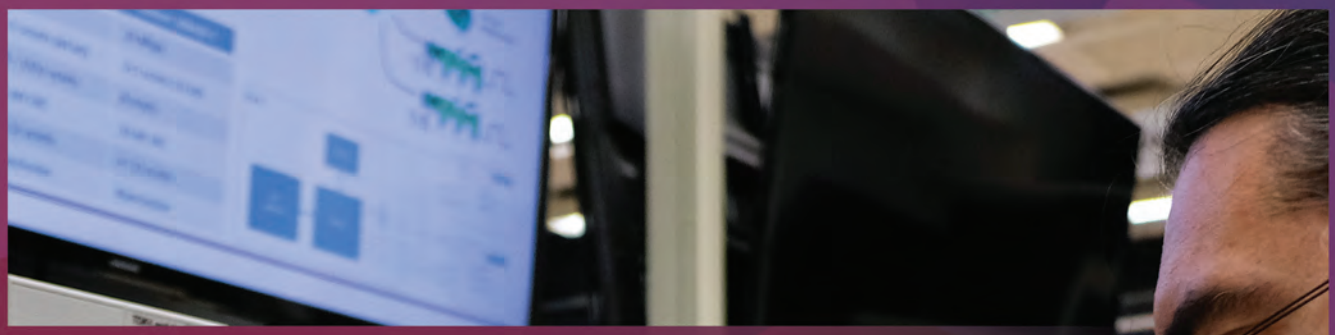
High-power, high-voltage power conversion technologies are attracting increasing attention in academia as well as industry in response to a need for more emerging power electronics applications, including alternative energy and power conversion such as wind power generations, fuel cells, hybrid electric vehicles, and all-electric ships. Enabled by a 2002 award of $839,337 from the Defense University Research Instrumentation Program (DURIP) paired with CPES cost-sharing of more than $250,000 for renovations, the electrical research lab area at Virginia Tech has been renovated and upfitted to accommodate medium-voltage, megawatts power capability. The facility has two medium-voltage 1 MVA reconfigurable transformers, corresponding reactors, capacitors, switchgears, and controllers. The complete setup is capable of testing power converters in various active and reactive operation modes continuously at 1 MVA, 4,160 V level. The unique installation distinguishes Virginia Tech as one of a few universities in the nation with this capability and enhances its position as a leader in power electronics research well beyond the NSF ERC life expectancy.

CPES also has the ability to test at 1 kV/100 A, 2 kV/ 50 A, and 3 kV/33 A with Magna dc Power Supplies along with 400 V/45 kVA/30 kVA ac-dc at various frequencies using the California Instruments MX-45 and MX-30. The High-Power Lab has also added a TDK-Lambda 30 kV/ 3.3 A supply. Partial Discharge testing is being done with a Phenix 50 kV Hi-Pot tester.

Software Support

CPES supports all major software used in power electronics design, including SPICE, Saber, Simplis, PowerSim, Code Composer, Math products—Matlab and Mathcad, Ansys Products—Workbench and Mechanical, Ansys Electromagnetics—Maxwell, Electronics Desktop (Q3D, HFSS), Simplorer, SIWave, PLECS, and Altium Designer.

High-Power Lab



Spotlight on Alumni

TOGETHER WE LEAD

At CPES, I was very fortunate to have Dushan Boroyevich as my advisor, Dr. Fred Lee as my co-advisor and very talented colleagues. CPES gave me a solid technical foundation in Power Management. But more importantly, at CPES, I learned that where there is a problem, there is an opportunity!

Ravi Ambatipudi

Affiliation
Analog Devices

Position Title
Vice President, Industrial Multi-Markets Business Unit

Last Degree from Virginia Tech
Master of Science

Year
1995

Career Highlights

Graduated from Virginia Tech in 1995 and joined National Semiconductor (acquired by Texas Instruments in 2011) as an applications engineer. Soon progressed through various engineering and business unit leadership roles. Ran several small and mid-size power management product lines and business units in the consumer, cloud and automotive markets. Joined Maxim Integrated (acquired by Analog Devices in 2021) in 2016 and transformed the Battery Power Solutions business unit. Now in-charge of the largest Power Management business unit in Analog Devices, Industrial Multi-Markets Business unit.

l landed in CPES quite by chance. My background was electromagnetic compatibility and I had interest in pursuing further expertise in RF/Antenna design. Due to lack of funding at VT and application season over, I decided to stay in electromagnetic compatibility and expressed willingness work for CPES instead. What seemed like a gamble at the time, both for me and Dushan, has now come to define my career. Guess it was destiny. I still remember the first question Dushan asked me, "who are you and why haven't I seen your application", and I replied, "Oh! because I never applied here".

Hemant Bishnoi

Affiliation
ABB Corporate Research Center

Position Title
Senior Scientist, Power Electronics Converters

Last Degree from Virginia Tech
Ph.D.

Year
2013

Career Highlights

Hemant has been working as a scientist in ABB's Corporate Research Center in Switzerland since 2013. Since joining, he has worked on several projects spanning over a wide application area including isolated MVDC converters and high power density inverters for UPS, marine, datacenters, traction, photovoltaic and electric vehicle charging applications. He is currently holding a position of senior scientist in ABB corporate research and been the project lead since 2019. His interests includes Electromagnetic compatibility, power conversion topology optimization and power stage design.

CPES is well known for its technical excellence and visionary leadership. Uniquely, CPES was also a window on the industry with a comprehensive view. By engaging broadly with companies and their engineers, CPES enabled it's researchers to have immediate impact and build skills for the real world. We understood the context of our technical work... why it was important and where it would make a difference. This prepared us to enter the industry and continue to grow and innovate throughout our careers.

Vlatko Vlatkovic

Affiliation
VM Vlatkovic Technology and Business Consulting

GE (formerly)

Position Title
Founder and Principal Advisor

Last Degree from Virginia Tech
Ph.D.

Year
1994

Career Highlights

Built a career dedicated to driving electrification through the industry, serving as a catalyst for change towards cleaner technologies like wind, solar PV, fuel cells, and hybrid electric propulsion.

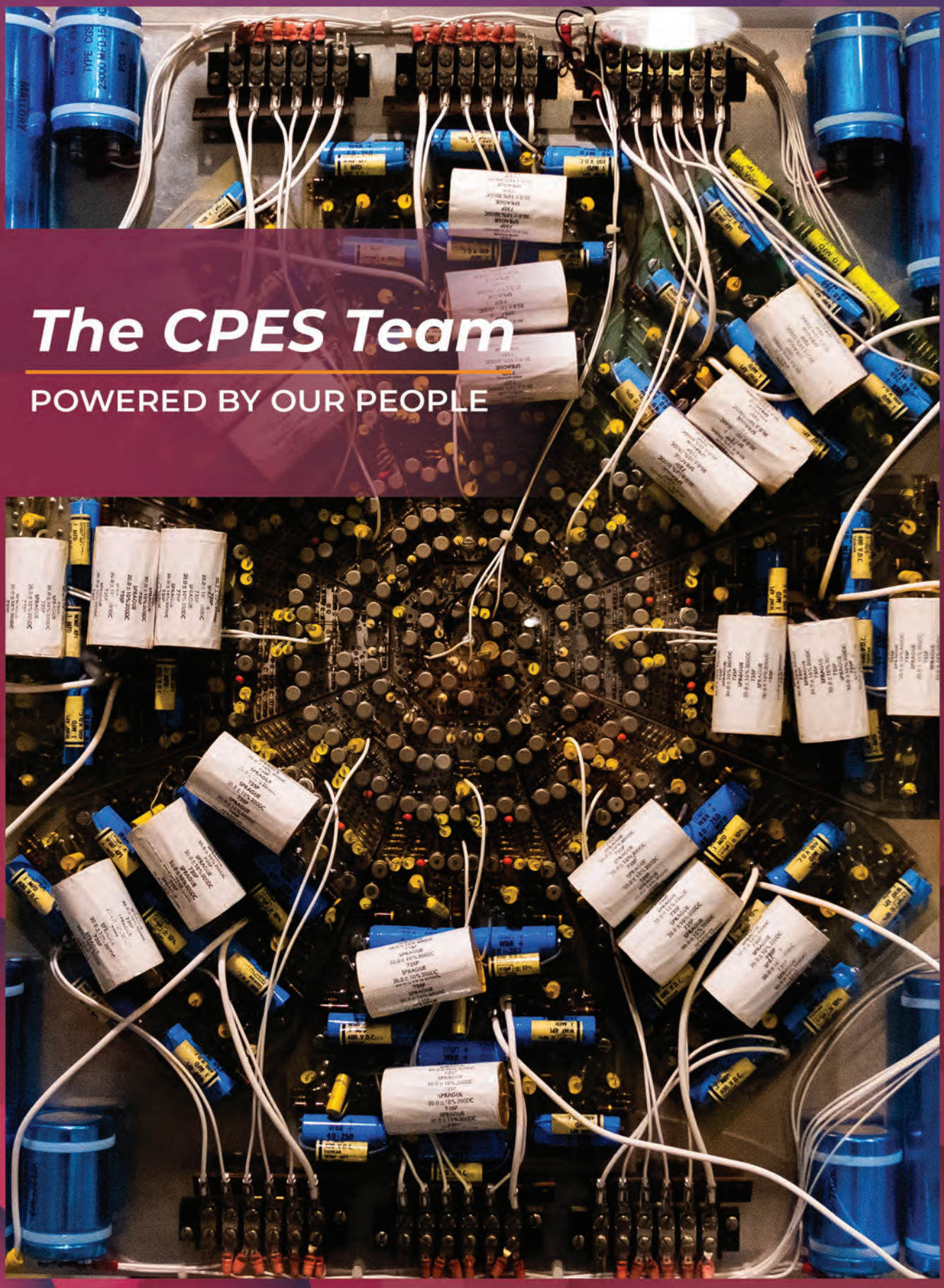
Joined GE Global Research as a scientist. Progressed to various leadership positions including leading the Electronics and Electrical Systems Labs at GE Global Research.

Served as CTO of the ~$3B GE Power Conversion business, driving electrification to transform traditionally mechanical drive oriented industries like Oil and Gas, Marine, and Power Generation.

As CTO and General Director of GEIQ in Mexico, the largest global engineering center of GE, was responsible for delivering hundreds of projects to customers across a business portfolio of Aviation Engines, Aviation Systems, Gas Power, and Renewables.

Founded an Energy Technology Investment Consultancy to continue driving innovation and growth through electrification of industry throughout transition of economy towards a sustainable future.

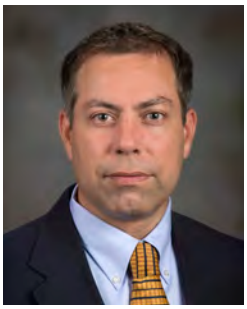

NOTICE
THIS UNIT IS
OUT OF SERVICE



The CPES Team

POWERED BY OUR PEOPLE

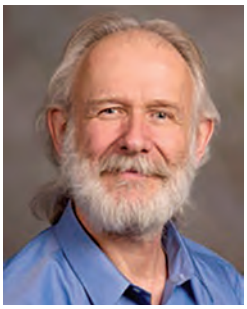
Faculty



Rolando Burgos

CPES Director and Professor

Dr. Burgos received the B.S. in Electronics Engineering, the Electronics Engineering Professional Degree, and the M.S. and Ph.D. degrees in Electrical Engineering from the University of Concepción, Chile, in 1995, 1997, 1999, and 2002, respectively. He then joined CPES as Postdoctoral Fellow, becoming Research Scientist in 2003 and Research Assistant Professor in 2005. In 2009, he joined ABB Corporate Research in Raleigh, NC. In 2012, he returned to Virginia Tech as Associate Professor, earning an early-decision tenure in 2017, and being promoted to Professor in 2020. In July 2021, he assumed the role of CPES Director. His research interests include high-power-density, wide-bandgap, semiconductor-based power conversion, packaging and integration, electromagnetic interference (EMI) and electromagnetic compatibility (EMC), multiphase multilevel power converters, modeling and control, grid power electronics systems, and the stability of ac and dc power grids.



Dushan Boroyevich

CPES Deputy Director and University Distinguished Professor

Dushan received Dipl. Ing. from the University of Belgrade in 1976 and an M.S. from the University of Novi Sad in 1982, in what used to be Yugoslavia, and a Ph.D. from Virginia Tech in 1986, all in electrical engineering. Between 1986 and 1990 he was an assistant professor at the University of Novi Sad. Since then he has been with CPES at Virginia Tech leading the research, education, industry collaboration, and global outreach in the areas of electronic power distribution systems, multiphase power conversion, power electronics systems modeling and control, and integrated design of power converters. He graduated almost 50 Ph.D. and 50 M.S. students, and co-authored with them around 1,000 technical publications. Prof. Boroyevich is a member of the US National Academy of Engineering and is the recipient of four honorary professorships in China and Taiwan, as well as numerous other awards.

Christina DiMarino

Assistant Professor

Christina DiMarino received her M.S. and Ph.D. degrees in electrical engineering from Virginia Tech in 2014 and 2018, respectively. She was a Webber Fellow from 2012 to 2015, and a Rolls-Royce Graduate Fellow from 2016 to 2017. She has been an assistant professor in the ECE department at Virginia Tech since 2019. She is located in the Virginia Tech Research Center in Arlington, VA, where she helped establish and manage two new CPES laboratories. Her research interests include power electronics packaging, high-density integration, medium-voltage power modules, and wide-bandgap power semiconductors.

Dong Dong

Assistant Professor

Dong Dong received a Bachelor of Science in 2007 from Tsinghua University in China and a Ph.D. in 2012 from Virginia Tech. Before joining CPES in 2018, he worked with GE's global research center for over five years on various power electronics and power system-related technologies. His research interests include high-frequency high-power conversion; driving, sensing, and protection of wide-band-gap power semiconductor devices; high-frequency high-power magnetics and resonant converters; board-level to system-level EMI modeling and mitigation; power delivery and distribution systems for renewable energy systems and transportation applications. He received multiple prize paper awards from IEEE, IAS and PELS, new technology and innovation awards at GE, and the NSF Career Award.

Mona Ghassemi

Assistant Professor (Affiliate Faculty)

Mona Ghassemi received her M.S. and Ph.D. from the University of Tehran in 2007 and 2012, respectively. She was a Postdoctoral Fellow at NSERC/Hydro-Quebec/UQac from 2013 to 2015, and at the Electrical Insulation Research Center (EIRC) of the Institute of Materials Science (IMS) at the University of Connecticut from 2015 to 2017. Her research interests include dielectrics and electrical insulation materials and systems containing those in power electronics modules and systems, high-voltage technology, multiphysics modeling, plasma science, electromagnetic transients in power systems, and power system modeling.

Qiang Li

Associate Professor

Qiang Li received his B.S. in 2003 and M.S. in 2006 from Zhejiang University. Then in 2011, he received his Ph.D. from Virginia Tech. He started at Virginia Tech as Research Assistant Professor in 2011 and was promoted to Assistant Professor in 2012. His research interests include high-density electronics packaging and integration, high-frequency magnetic components, high-frequency power conversion, distributed power systems, and renewable energy.

Guo-Quan Lu

Professor (Affiliate Faculty)

Guo-Quan Lu received a double-major B.S. in physics and materials science and engineering from Carnegie Mellon University in 1984, and a Ph.D. in applied physics from Harvard University in 1990. He then worked at Alcoa Technical Center for two years before joining Virginia Tech. Since 2003, Lu has been a professor in both the MSE and ECE departments. Lu's research activities and interests include packaging materials and assembly process development for interconnect, insulation, and magnetics of power electronics modules and converters.

Khai Ngo

Professor

Khai Ngo received his B.S. from California State Polytechnic University, Pomona, in 1979, and his M.S. and Ph.D. from the California Institute of Technology, Pasadena, in 1980 and 1984, respectively, all in electrical and electronics engineering. At CPES, he pursues technologies for reliable, efficient, affordable, and dense integration of high-field and high-temperature power and electronic components. He also coordinates CPES's outreach activities and the Consortium for High-Density Integration.

Richard Zhang

Professor

Richard Zhang earned B.S. and M.S. degrees from Tsinghua University in 1989 and 1993, respectively, and his Ph.D. degree from Virginia Tech in 1998. He joined GE's Global Research Center in 1998. In the following 22 years with various GE businesses, he held a number of executive-level technology and business leadership positions. Prior to joining CPES, he was CTO of GE Grid Integration Solutions. Prof. Zhang was named the Hugh P. and Ethel C. Kelly Chair upon joining Virginia Tech. His research interests include MVDC/HVDC, EV fast-charging stations, grid integration of renewables, H2 production, utility-scale energy storage, WBG device applications, DC Circuit Breaker, and ML/AI in high-power electronics systems. He has over 105 global patents granted or pending and has 4 IEEE Transaction Paper Awards. Prof. Zhang is a Fellow of IEEE.

Yuhao Zhang
Assistant Professor

Yuhao Zhang studied physics at Peking University in China, where he received a B.S. in 2011. He went on to study electrical engineering at Massachusetts Institute of Technology in the United States, earning his M.S. in 2013 and his Ph.D. in 2017. He received the MIT Microsystems Technology Laboratories Doctoral Dissertation Seminar Award, the IEEE George E. Smith Award, and a NSF CAREER Award. His research interest is at the intersection of power electronics, micro/nano-electronic devices and advanced semiconductor materials, and the energy applications for data centers, electric vehicles, photovoltaics, and mobile applications, as well as the energy-related applications in extremely harsh environments. He has published over 100 journal publications and juried conference proceedings, and has five patents.

Research Faculty

Igor Cvetkovic
Research Scientist and Technical Director

Igor Cvetkovic received a Dipl. Ing. Degree from University of Belgrade, Serbia in 2004. After working several years for the Electric Power Industry of Serbia, Igor joined the Center for Power Electronics Systems at Virginia Tech where he completed his M.S and Ph.D. degrees in 2010 and 2017, respectively. Igor is now Research Scientist and Technical Director at CPES, and his research interests include electronic power distribution systems design and stability, as well as system-level modeling and control. Igor participated in numerous sponsored projects at CPES including Boeing, Newport News Shipbuilding, U.S. Department of Energy, and Office of Naval Research.

Boran Fan
Research Scientist

Boran Fan received the B.S. and Ph.D. degrees in electrical engineering from Tsinghua University in 2013 and 2018, respectively. In 2018 he joined, CPES as a Postdoctoral Fellow, becoming Research Scientist in 2021. His research interests include MV power conversion topology, auxiliary circuitry, insulation technique, advanced control and intelligent communication and control systems, aircraft powertrain power converters and HV electrification covering multiphase drive architecture, EMI filter mitigation, high-density drive system integration, thermal management systems, and high-voltage (>1 kV), high-altitude (>30,000 ft) insulation techniques.

David Gilham
Lab Operations Director

David was born and raised in Southern California. He moved with his wife to Virginia in 2003 to pursue his B.S. degree in Electrical Engineering from Virginia Tech. Soon after graduation in 2007, he began as a staff researcher under the guidance of Dr. Fred Lee at CPES. In 2010 he was promoted to research faculty and began his M.S. study with concentration on packaging of POL converters using ceramic substrates and WBG devices. In 2012, David was promoted to Lab Operations Director and also graduated with his M.S. degree that same year.

Yi-Hsun Hsieh
Research Associate

Yi-Hsun (Eric) Hsieh received his B.S. and M.S. degrees in electrical engineering from the National Cheng Kung University in Taiwan in 2011 and 2013, respectively. He joined CPES as a Ph.D. student in 2014 and worked with Dr. Fred C. Lee. After receiving his Ph.D. degree in 2020, he continues working in CPES as a research associate. Yi-Hsun Hsieh's research interests include resonant converter modeling, solid-state transformer, and modular multilevel converter. He holds one U.S. patent, and has published two journal papers and 18 conference papers.

Fred C. Lee

CPES Director Emeritus

University Distinguished Professor Emeritus

Fred C. Lee received his B.S. Degree in electrical engineering from the National Cheng Kung University in Taiwan in 1968, and his M.S. and Ph.D. degrees in electrical engineering from Duke University in 1972 and 1974, respectively. He has been Founder and Director of VPEC/CPES since 1983. His research interests include high-frequency power conversion, magnetics and EMI, distributed power systems, renewable energy, power quality, high-density electronics packaging and integration, and modeling and control.

Bo Wen

Research Assistant Professor

Bo Wen received his B.S. degree from Xi'an Jiaotong University, China, and M.S. and Ph.D. degrees from Virginia Tech, USA, in 2006, 2011, and 2014, all in electrical engineering. He was Research Associate with the University of Cambridge, Cambridge, and a Lecturer with the School of Electrical and Electronic Engineering, the University of Manchester, Manchester, U.K. Dr. Wen is currently Research Assistant Professor at CPES. He received the 2017 Prize Paper Award in the IEEE Transactions on Power Electronics and the 2019 Outstanding Reviewer Award from the same journal. His current research interests include power conversion, power electronics systems modeling, and integration.

Ming Xiao

Research Scientist

Ming Xiao received all his B.S., M.S., and Ph.D. degrees in electrical and electronics engineering from Xidian University in 2012, 2015, and 2018, respectively. He won the honor of an Excellent Ph.D. Dissertation of Shaanxi Province for his Ph.D. works. He joined CPES as Postdoctoral Associate in 2018 and was promoted to Research Scientist in 2021. His research interest is at the intersection of power electronics, micro/nano-electronic devices, advanced semiconductor materials and their energy applications.

Staff

Neil Croy
Lab Operations Associate

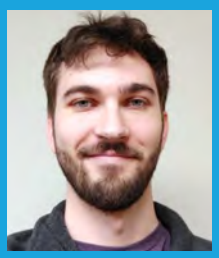
Audri Cunningham
Executive Assistant

Dennis Grove
Industry Program Director

Brandy Grim
Procurement Officer

Emmet Howard
Lab Assistant

Ling Li
Business Director

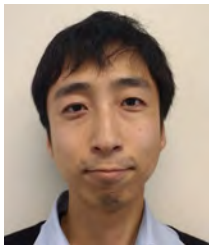


Matthew Scanland
Webmaster & Digital Content Specialist

Yan Sun
Accounting & Fiscal Associate

Visiting Scholars

Fabiano Costa
Professor
Federal University of Bahia



Takeya Okuno
Visiting Engineer
Panasonic Corporation

Phu Hieu Pham
Ph.D. Student
National Taiwan University of Science and Technology

Ryota Tanaka
Visiting Engineer
Nissan Motor Company

Chuanyun Wang
Visiting Engineer
Powerland Technology Inc.

2021 Graduates

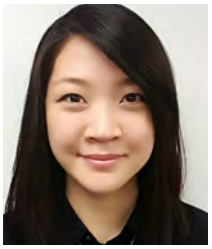
Victoria Baker
Johns Hopkins University Applied Physics Laboratory

Md Abdul Gaffar

Jacob Gersh
Rivian

Jiewen Hu
Apple Inc.

Joseph Kozak
Johns Hopkins University Applied Physics Laboratory



Virginia Li
Analog Devices, Inc.

Slavko Mocevic
ABB

Sri Naga Vinay Mutyala
Lam Research Corporation

Keyao Sun
Empower Semiconductor

Yue Xu
University of Texas, Austin

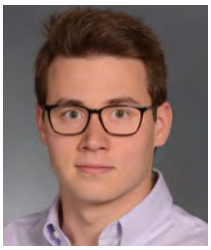
Graduate Students


Benjamin Alden

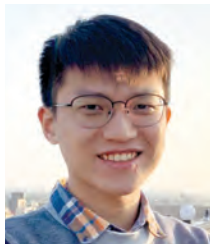

Haris Bin Ashraf


Yijie Bai


Filip Boshkovski


Mark Cairnie


Yuliang Cao


Che-Wei Chang


Xingyu Chen


Rimon Gadelrab


Yugal Gupta


Feng Jin


Matthew Kallicharran


Jack Knoll


Marie Lawson


Danielle Lester


Bo Li


Qian Li


Zheqing Li


Junming Liang

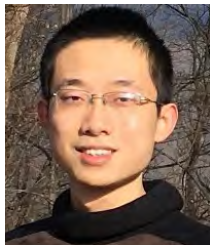

Qing Lin


Xiang Lin


Jian Liu


Xin Lou


Shengchang Lu


Yunwei Ma


Abdelrahman Mahgoub

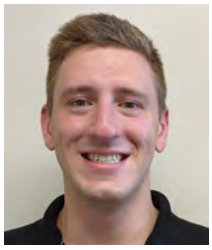

Tyler McGrew


Jesi Miranda

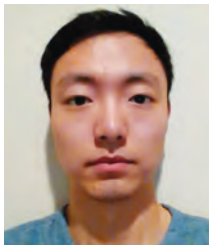

Vladimir Mitrovic


Taha Moaz


Jayesh Motwani


Paul Mourges


Ahmed Nabih


David Nam


Adhistira Naradhipa


Arash Nazari


Minh Ngo


Tam Nguyen


Carl Nicholas


Jeet Panchal


Ripunjoy Phukan


Pranav Raj Prakash


Narayanan Rajagopal


Lakshmi Ravi


Yu Rong


Aishworya Roy


Yizhi Ruan


Keyue Shan


Sharifa Sharfeldden

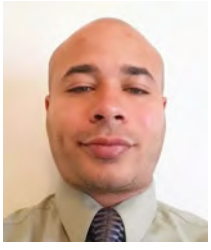

Gibong Son


He Song


Qihao Song


Joseph Spencer


Matthias Spieler


Joshua Stewart


Kenneth Test


Cong Tu


Sunbo Wang


Biqi Wang


Boyan Wang


Le Wang


Shuo Wang


Yifan Wang


Xinmiao Xu


Ning Yan


Qiuzhe Yang


Jianghui Yu


Xipei Yu


Tianlong Yuan


Ruizhe Zhang


Zichen Zhang

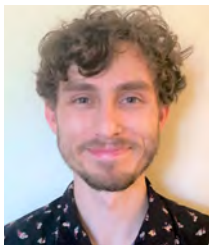

Chunyang Zhao


Tianyu Zhao


Xinchen Zhao


Feiyang Zhu

Undergraduate Students


Benjamin Albano

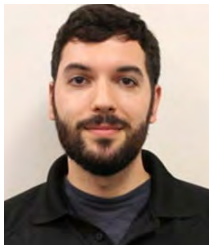

John Alcantara

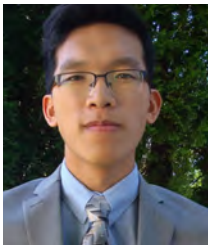

Ankit Bhardwaj


Jonathan Borghese


Rutvik Chavda


Bhavin Jain


Matthew Sclafani


Matthew Trang


Ruiqi Zhang

Advisory Boards

Scientific Advisory Board (SAB)

The CPES SAB is a critical part of the governing structure, providing key insights on the technological direction of the center.

Consisting of leading global researchers and managers of research programs in areas related to power electronics, these experts observe the status of CPES research and education programs and provide critical feedback to CPES leadership.

Anant Agarwal
Ohio State University

Johan Enslin
Clemson University

Leo Lorenz
European Center for Power Electronics

Dragan Maksimovic
University of Colorado, Boulder

Industry Advisory Board (IAB)

The primary role of the IAB is to represent the interests of Industry Members in the CPES research programs as well as advise the CPES director and faculty members on industry trends, key challenges, and programmatic matters.

Pietro Cairoli
ABB, Inc.

Henry Zhang
Analog Devices, Inc.

Kevin Rhatigan
Aurora Flight Sciences

Ismail Agirman
Carrier Corporation

Ernie Parker
Crane Aerospace & Electronics

Shengli (Catherine) Huang
CRRC Zhuzhou Institute Co., Ltd.

Jaroslaw (Jarek) Leonarski
Cummins*

Peter Barbosa, IAB Chair
Delta Electronic

Hongrae Kim
Eaton

Peter Xu
Flextronics

Zhuxian (Nicole) Xu
Ford Motor Company*

Xiaochuan Jia
GE Aviation

Juan Sabate
GE Global Research

Eric Persson
Infineon Technologies

Chunhua (David) Zhou
Innoscience (Zhuhai) Technology

Qiuyan Huang
Jiangsu Wanbang Dehe New Energy Technology Co. Ltd.

Pit-Leong Wong
Joulwatt Technology

Sam Ye
LITE-ON Technology

Thomas Byrd
Lockheed Martin Corporation

Agasthya Ayachit
Mercedes-Benz R&D North America, Inc.

Heath Kouns
Moog, Inc.

Alex Yang
Murata Manufacturing Co., Ltd.

Gene Sheridan
Navitas Semiconductor

Dinesh Ramanathan
NexGen Power Systems

Yasuaki Hayami
Nissan Motor Co., Ltd.

Zhenxia Shao
NR Electric, Ltd.

Hatsuda Tsuguyasu
Panasonic Corporation

Ming Xu
Powerland Technology, Inc.

Sriram Chandrasekaran
Raytheon Technologies

Navid Zargari
Rockwell Automation

Anurag Jivanani
Schneider Electric IT Corporation

Arturo Pizano
Siemens Corporate Technology

Issac Chen
Silergy Corporation

Udi Levy
SolarEdge Technologies, Inc.

Colin Campbell
Tesla*

Laszlo Balogh
Texas Instruments

Thomas Tainer
TMEIC Corporation

Jian Li
Vertiv

Tamara Baksht
VisIC Technologies

Florian Wilhelmi
ZF Friedrichshafen AG

Jianping Zhou
ZTE Corporation

**Associate Member Representative*

Honors & Achievements

CELEBRATING TRANSFORMATION & MOMENTUM

National and International Honors

Dushan Boroyevich

Technical Co-Chair, 2021 FERC EnVision Forum, April 26-27

Session Chairman, "Converter Modeling, Design and Low-Level Control," 23rd European Conference on Power Electronics and Applications, EPE'21 ECCE Europe, September 6-10

Steering Committee, 2021 6th IEEE Workshop on the Electronic Grid (eGRID), November 8-10

Advisory Board, *Journal of Power Electronics*, The Korean Institute of Power Electronics

Co-Author, "Building Blocks for Microgrids," Microgrid R&D Program Strategy, Office of Electricity, Department of Energy, USA

Co-Design Advisory Board, *Ultra Materials for a Resilient, Smart Electricity Grid (ULTRA)*, DoE Energy Frontier Research Center, Arizona State University, USA

Editorial Board, *Chinese Journal of Electrical Engineering,* China Machinery Industry Information Institute

Inaugural Advisory Board, *Inaugural Advisory Board,* iEnergy journal, Tsinghua University Press, China

Dong Dong

Conference General Chair, IEEE International Conference on DC Microgrids, July 18-21

Qiang Li

Faculty Fellow, 2021 College of Engineering Dean's Awards for Excellence

Richard Zhang

Steering Committee and Session Chair, 2021 FERC EnVision Forum, April 26-27

Technical Program Chair, 2021 6th IEEE Workshop on the Electronic Grid (eGRID), November 8-10

IEEE Fellow Evaluation Technical Committee, Power Electronics Society

Appointed the Hugh P. and Ethel C. Kelly Professor of Electrical and Computer Engineering, by the Virginia Tech Board of Visitors

Yuhao Zhang

CAREER Award, *"Nitride FinFET on Silicon for Medium-Voltage Monolithically Integrated Power Electronics,"* National Science Foundation

Outstanding Assistant Professor, 2021 College of Engineering Dean's Awards for Excellence

Dong Dong and Yuhao Zhang

Special Session Co-Chairs, *"Medium- and High-Voltage Gallium Nitride Power Devices,"* Energy Conversion Congress and Expo (ECCE), October 10-14

Keynote Addresses

Christina DiMarino

Wide-Bandgap Power Semiconductor Packaging for Electrified Transportation, 2021 IEEE Students and Young Professionals Symposium (SYPS), March 27-29

Fred C. Lee

History of IEEE PELS and Power Electronics, IEEE Power Electronics Society, PELS Day, June 20

Data Center Power Architecture and Design, 2021 5th IEEE International Future Energy Electronics Conference, November 16-19

PCB-Based Magnetics Integration: Benefits and Limitations, 24th China Power Supply Society Conference & Exhibition, CPSSC 2021, November 12-15

A Planar Omni-Directional Power Transfer System for Portable Devices Application, 2021 International Conference on Electric and Intelligent Vehicles, June 25-28

Invited Talks

Dushan Boroyevich

Lessons Learned and Future Vision for NSF and DOE Research Centers in Power and Energy Research, 2021 IEEE Power and Energy Society General Meeting, July 26-29

High-Density High-Frequency Power Conversion for Future Electronic Power Systems, Ultra Materials for a Resilient, Smart Electricity Grid (ULTRA), DoE Energy Frontier Research Center, September 20

Global Intergrid for Sustainable Energy Abundance, Global Innovation Hub, 2021 UN Climate Change Conference (COP 26), Glasgow, UK, October 31-November 13

Fred C. Lee

Power Electronics-The Earlier Days, IEEE PEL Lecture Series, June 22

EV Bi-Directional On-Board Charger, Tutorial, IEEE Wide-Bandgap Power Devices and Applications in Asia (WiPDA-Asia), August 25-27

Next Generation of Power Supplies, 2021 IEEE Asian PhD School on Advanced Power Electronics, August 28-September 4

Yuhao Zhang

(Ultra-) Wide-Bandgap Devices: Reshaping the Power Electronics Landscape, University of Utah, Department of Computer and Electrical Engineering Seminar, February 22

Surge Energy Robustness of GaN Power Devices and Modules, PowerAmerica Annual Conference 2021, February 23-25

Exploring New Application Space of GaN Power HEMTs, Analog Devices, Inc., February

Exploring New Application Spaces of GaN Power Devices, Mitsubishi, May

Exploring New Application Spaces of GaN Power Devices, Applied Power Electronics Conference (APEC), June 14-17

Exploring New Application Spaces of GaN Power Devices, Taiwan Semiconductor Manufacturing Company (TSMC), August

Multi-Channel GaN Power Rectifiers: Breakthrough Performance up to 10 kV, 240th Electrochemical Society (ECS) Meeting, October 10-14

How to Achieve Low Thermal Resistance and High Electrothermal Ruggedness in Ga_2O_3 devices?, 240st Electrochemical Society (ECS) Meeting, October 10-14

GaN Power Devices: Physics and Reliability, Murata Power Solutions, November

Dushan Boroyevich and Igor Cevtkovic

Center for Power Electronics Systems at Virginia Tech in Arlington, 2021 IEEE Power and Energy Society General Meeting, July 26-29

Dushan Boroyevich, Jun Wang, Yu Rong, Vladimir Mitrovic, and Boran Fan

PESNet 3.0: a Next-Generation-Distributed Communication and Control Network for Modular Power Converters, 2021 IEEE Electric Ship Technologies Symposium (ESTS), July 27-30

Dushan Boroyevich, Dong Dong, Christina DiMarino, Jun Wang, Igor Cvetkovic, Slavko Mocevic, Yu Rong, Jian Liu, Keyao Sun, Yue Xu, Joshua Stewart, Jianghui Yu, Ning Yan, He Song, Mark Cairnie, and Ye Tang

High-Power-Density High-Frequency Modular Power Converters for High-Voltage Applications, Video Tutorial, 2021 IEEE Asian PhD School on Advanced Power Electronics, August 28-September 4

Dushan Boroyevich, Igor Cevtkovic, and Dong Dong

An Electronized Future Power System for Sustainable Energy Abundance, International Forum on Electronized Future Energy Systems, Tsinghua University, Beijing, China, September 4

Urban Living Labs inspiring Global Intergrid for Sustainable Energy Abundance, The Transformative Power of Urban Living Labs, 2021 UN Climate Change Conference (COP 26), Glasgow, UK, October 31-November 13

Fred C. Lee and Qiang Li

Integrated PCB Winding Magnetic Components for High-Frequency Power Converters, Tuorial, 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), June 14-17

Prize Paper Awards

Xiang Lin, Lakshmi Ravi, Dong Dong, and Rolando Burgos

William M. Portnoy Award, 2020 IEEE Energy Conversion Congress and Exposition (ECCE), October 11-15, 2020. *Hybrid Voltage Balancing Approach for Series-Connected 10 kV SiC MOSFETs for DC-AC Medium-Voltage Power Conversion Applications,* pp3769-3775

Slavko Mocevic, Vladimir Mitrovic, Jun Wang, Rolando Burgos, Dushan Boroyevich, Marko Jaksic, and Mehrdad Teimor

William M. Portnoy Award, 2020 IEEE Energy Conversion Congress and Exposition (ECCE), October 11-15, 2020. *Gate-Driver Integrated Junction Temperature Estimation of SiC MOSFET Modules,* pp3761-3768

Slavko Mocevic, Vladimir Mitrovic, Jun Wang, Rolando Burgos, and Dushan Boroyevich

Best Paper Award, 21st International Symposium on Power Electronics Ee2021. *SiC MOSFET Junction Temperature Estimation Based on Output Characteristics Integrated on Gate-driver, October 27-30*

Ming Xiao, Yunwei Ma, Zhonghao Du, Vasantha Pathirana, Kai Cheng, Andy Xie, Edward Beam, Yu Cao, Florin Udrea, Han Wang, and Yuhao Zhang

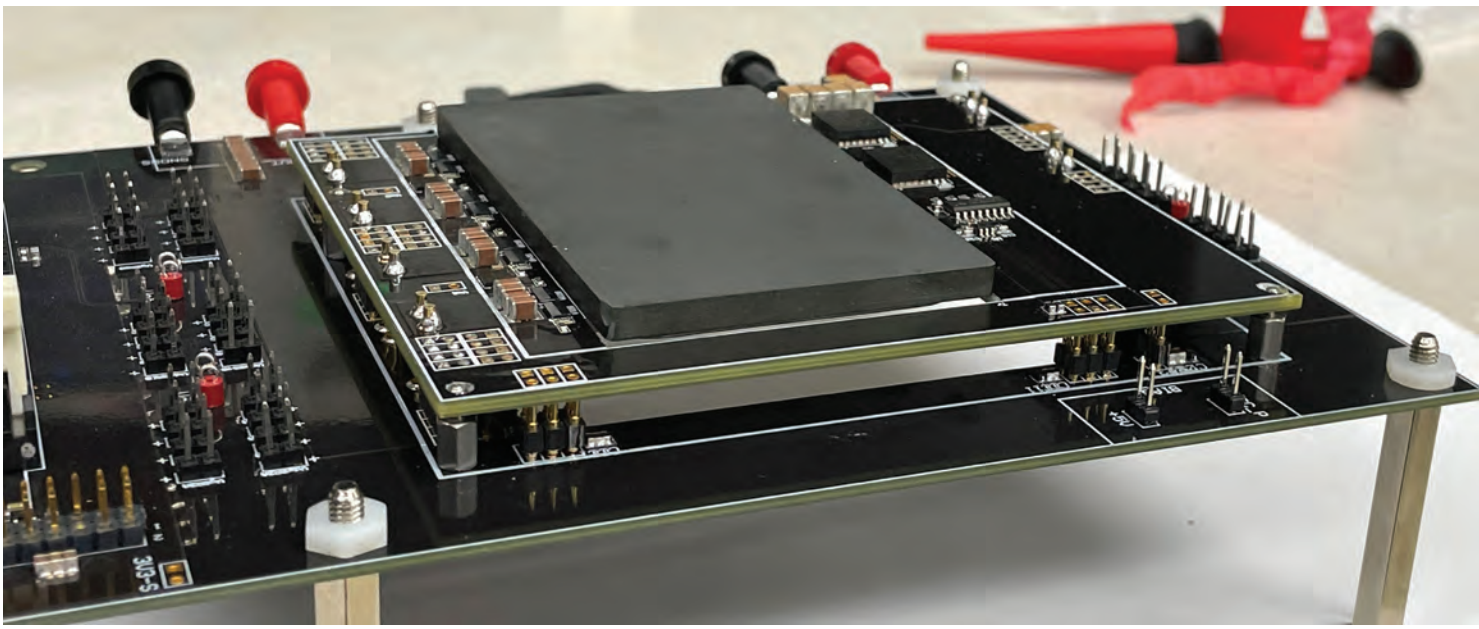
Technical Tipsheet Award, 67th IEEE International Electron Devices Meeting (IEDM), December 11-15. *Multi-Channel Monolithic-Cascode HEMT (MC2-HEMT): A New GaN Power Switch up to 10 kV.*

Shike Wang, Zeng Liu, Jinjun Liu, Dushan Boroyevich, and Rolando Burgos

2020 First Place Prize Paper Award, IEEE Transactions on Power Electronics, *Small-Signal Modeling and Stability Prediction of Parallel Droop-Controlled Inverters Based on Terminal Characteristics of Individual Inverters,* Vol. 35, No. 1, pp1045-1063

Ramanuja Panigrahi, Santanu K. Mishra, Avinash Joshi, and Khai D. T. Ngo

2020 First Place Prize Paper Award, IEEE Power Electronics Letters, *DC-DC Converter Synthesis: An Inverse Problem,* Vol. 35, No. 12, pp12633-12638



Student Awards and Achievements

Jian Liu, Lakshmi Ravi, Dong Dong, Rolando Burgos, Cyril Buttay, and Steve Schmalz

Technical Lecture Best Presentation Award Winner, 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), June 14-17. *High-Power-Density Design of Power Electronic Interrupter in Hybrid DC Circuit Breaker,* pp33-38

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Technical Lecture Best Presentation Award Winner, 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), June 14-17. *High-Power-Density 1 MHz 3 kW 400 V-48 V LLC Converter for Data Centers With Improved Core Loss and Termination Loss,* pp304-309

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Yuliang Cao, Minh Ngo, Ning Yan, Yijie Bai, Dong Dong, Rolando Burgos, and Ismail Agirman

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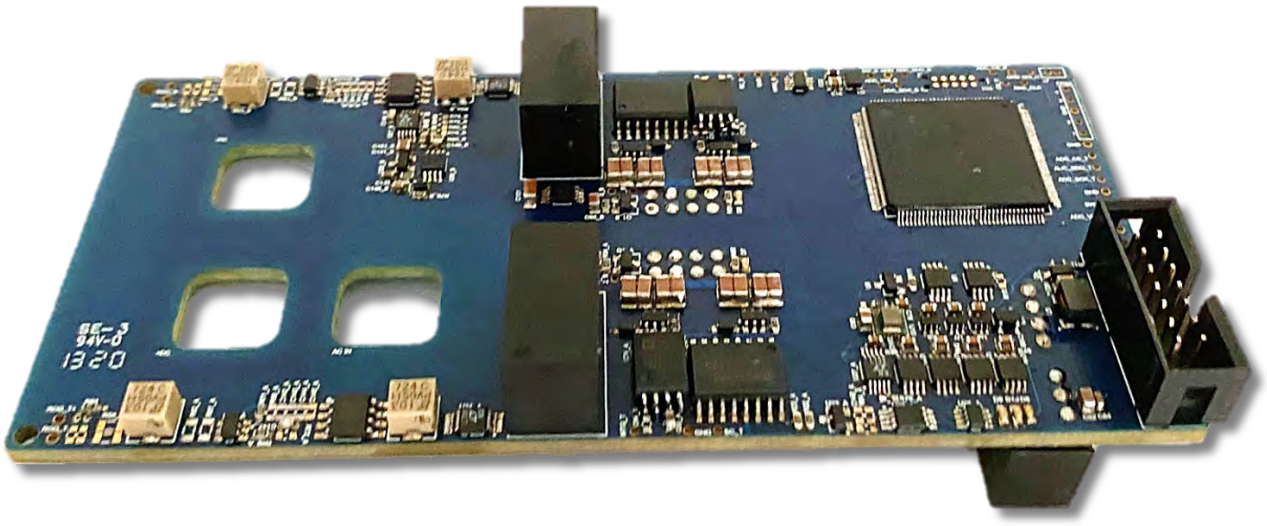
Technical Lecture Best Presentation Award Winner, 2021 IEEE Applied Power Electronics Conference and Exposition (APEC), June 14-17. *Computational Fluid Dynamic Analysis and Design of an Air Duct Cooling System for 18 kW, 500 kHz Planar Transformers,* pp1496-1504

Joseph Kozak

IEEE PELS Ph.D. Thesis Talk Award. *Hard-Switched Robustness of Wide-Bandgap Power Semiconductor Devices*

2nd Prize, Virginia Tech Engineering Ph.D. Poster Presentation Torgersen Award. *Hard-Switched Robustness of Wide-Bandgap Power Semiconductor Devices*

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Publications

WORKING TOWARDS TOMORROW

Transactions Papers

Adaptive Hysteresis Current Based ZVS Modulation and Voltage Gain Compensation for High-Frequency Three-Phase Converters

Boran Fan; Qiong Wang; Rolando Burgos; Agirman Ismail; Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 36, No. 1, pp. 1143-1156

Multi-Objective Design and Optimization of Power Electronics Converters With Uncertainty Quantification – Part I: Parametric Uncertainty

Niloofar Rashidi; Qiong Wang; Rolando Burgos; Chris Roy; Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 36, No. 2, pp. 1463-1474

Multi-Objective Design and Optimization of Power Electronics Converters With Uncertainty Quantification – Part II: Model-Form Uncertainty

Niloofar Rashidi; Qiong Wang; Rolando Burgos; Chris Roy; Dushan Boroyevich

IEEE Transactions on Power Electronics, Vol. 36, No. 2, pp. 1441-1450

Third Quadrant Conduction Loss of 1.2 – 10 kV SiC MOSFETs: Impact of Gate Bias Control

Ruizhe Zhang; Xiang Lin; Jingcun Liu; Slavko Mocevic; Dong Dong; Yuhao Zhang

IEEE Transactions on Power Electronics, Vol. 36, No. 2, pp. 2033-2043

LCCL-LC Resonant Converter and Its Soft-Switching Realization for Omnidirectional Wireless Power Transfer Systems

Junjie Feng; Qiang Li; Fred C. Lee; Minfan Fu

IEEE Transactions on Power Electronics, Vol. 36, No. 4, pp. 3828-3839

Circuit Modeling of the Mechanical-Motion Rectifier for Electrical Simulation of Ocean Wave Power Takeoff

Chien-An Chen; Xiaofan Li; Lei Zuo; Khai D. T. Ngo

IEEE Transactions on Industrial Electronics, Vol. 68, No. 4, pp. 3262-3272

High-Frequency Resonant Converters: An Overview on the Magnetic Design and Control Methods

Fred C. Lee; Qiang Li; Ahmed Nabih

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 1, pp. 11-23

Transient Control and Soft Start-Up for 1 MHz LLC Converter With Wide Input Voltage Range Using Simplified Optimal Trajectory Control

Ahmed Nabih; Mohamed H. Ahmed; Qiang Li; Fred C. Lee

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 1, pp. 24-37

Inverse Charge Constant On-Time Control With Ultrafast Transient Performance

Syed Bari; Qiang Li; Fred C. Lee

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 1, pp. 68-78

Two-Stage 48 V VRM With Intermediate Bus Voltage Optimization for Data Centers

Mohamed H. Ahmed; Fred C. Lee; Qiang Li

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 1, pp. 702-715

Modeling of N-Parallel Full-SiC AC–DC Converters by Four Per-Phase Circuits

Sungjae Ohn; Ripun Phukan; Dong Dong; Rolando Burgos; Dushan Boroyevich; Mondal Gopal; Sebastian Nielebock

IEEE Transactions on Power Electronics, Vol. 36, No. 6, pp. 6142-6146

Neutral-Point Voltage Balancing Methods of Series-Half-Bridge LLC Converter for Solid-State Transformer

Cheng Lu; Wenfei Hu; Fred C. Lee

IEEE Transactions on Power Electronics, Vol. 36, No. 6, pp. 7060-7073

Two-Dimensional Mapping of Interface Thermal Resistance by Transient Thermal Measurement

Shan Gao; Khai D. T. Ngo; Guo-Quan Lu

IEEE Transactions on Industrial Electronics, Vol. 68, No. 5, pp. 4448-4456

A Soft Magnetic Moldable Composite With Tri-Modal Size Distribution for Power Electronics Applications

Chao Ding; Khai D. T. Ngo; Guo-Quan Lu

IEEE Transactions on Magnetics, Vol. 57, No. 3, pp. 1-6

Omnicoupled Inductors (OCI) Applied in a Resonant Cross-Commutated Buck Converter

Ting Ge; Khai D. T. Ngo

IEEE Transactions on Industrial Electronics, Vol. 68, No. 6, pp. 4894-4902

High-Power Magnetoelectric Voltage Tunable Inductors

Yongke Yan; Liwei D. Geng; Lujie Zhang; Cong Tu; Rammohan Sriramdas; Hairui Liu; Xiaotian Li; Mohan Sanghadasa; Khai D. T. Ngo; Yu U. Wang; Shashank Priya

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Analysis of Voltage Sharing of Series-Connected SiC MOSFETs and Body-Diodes

Xiang Lin; Lakshmi Ravi; Yuhao Zhang; Rolando Burgos; Dong Dong

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Switching Performance Analysis of Vertical GaN FinFETs: Impact of Interfin Designs

Hengyu Wang; Ming Xiao; Kuang Sheng; Tomás Palacios; Yuhao Zhang

IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 2, pp. 2235-2246

True Breakdown Voltage and Overvoltage Margin of GaN Power HEMTs in Hard Switching

Joseph P. Kozak; Ruizhe Zhang; Qihao Song; Jingcun Liu; Wataru Saito; Yuhao Zhang

IEEE Electron Device Letters, Vol. 42, No. 4, pp. 505-508

1.2 kV Vertical GaN Fin-JFETs: High-Temperature Characteristics and Avalanche Capability

Jingcun Liu; Ming Xiao; Ruizhe Zhang; Subhash Pidaparthi; Hao Cui; Andrew Edwards; Michael Craven; Lek Baubutr; Cliff Drowley; Yuhao Zhang

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A Constant-Current ZVS Class-E Inverter With Finite Input Inductance

Lujie Zhang; Khai Ngo

IEEE Transactions on Industrial Electronics, Vol. 68, No. 8, pp. 7693-7696

Packaged Ga_2O_3 Schottky Rectifiers With Over 60 A Surge Current Capability

Ming Xiao; Boyan Wang; Jingcun Liu; Ruizhe Zhang; Zichen Zhang; Chao Ding; Shengchang Lu; Kohei Sasaki; Guo-Quan Lu; Cyril Buttay; Yuhao Zhang

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A Hybrid Modular Multilevel Converter Family With Higher Power Density and Efficiency

Jian Liu; Dong Dong; Di Zhang

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10 kV, 39 mΩ·cm² Multi-Channel AlGaN/GaN Schottky Barrier Diodes

Ming Xiao; Yunwei Ma; Kai Liu; Kai Cheng; Yuhao Zhang

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Glass for Encapsulating High-Temperature Power Modules

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Series-Resonator Buck Converter – Viability Demonstration

Cong Tu; Rengang Chen; Khai D. T. Ngo

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Design of a Wide-Input-Voltage PCB-Embedded Transformer Based Active-Clamp Flyback Converter Considering Permeability Degradation

Jiewen Hu; Bo Wen; Rolando Burgos; Yonghan Kang

IEEE Transactions on Power Electronics, Vol. 36, No. 9, pp. 10355-10365

Additive Manufacturing of Hetero-Magnetic Coupled Inductors

Chao Ding; Shengchang Lu; Lanbing Liu; Khai D. T. Ngo; Guo-Quan Lu

IIEEE Transactions on Components, Packaging and Manufacturing Technology, Vol. 11, No. 6, pp. 1028-1034

Surge Current and Avalanche Ruggedness of 1.2 kV Vertical GaN p-n Diodes

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A Single Passive Gate-Driver for Series-Connected Power Devices in DC Circuit Breaker Applications

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A Double-Side Cooled SiC MOSFET Power Module With Sintered-Silver Interposers: I-Design, Simulation, Fabrication, and Performance Characterization

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Quasi-Two-Level Bridgeless PFC Rectifier for Cascaded Unidirectional Solid-State Transformer

Cheng Lu; Wenfei Hu; Hongyang Wu; Fred C. Lee

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Low-Thermal Resistance (0.5 kW) Ga_2O_3 Schottky Rectifiers With Double-Side Packaging

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IEEE Electron Device Letters, Vol. 42, No. 8, pp. 1132-1135

Analysis and Control of Critical Conduction Mode High-Frequency Single-Phase Transformerless PV Inverter

Gibong Son; Zhengrong Huang; Qiang Li; Fred C. Lee

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Power Cell Design and Assessment Methodology Based on a High-Current 10 kV SiC MOSFET Half-Bridge Module

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IEEE Journal of Emerging and Selected Topics in Power Electronics, Vol. 9, No. 4, pp. 3916-3935

Insulation Design of Wireless Auxiliary Power Supply for Medium-Voltage Converters

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Synthesis of DC-DC Converters From Voltage Conversion Ratio and Prescribed Requirements

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Tri-Gate GaN Junction HEMTs: Physics and Performance Space

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IEEE Transactions on Electron Devices, Vol. 68, No. 10, pp. 4854-4861

New Way of Generating Electromagnetic Waves

Ali Hosseini-Fahraji; Majid Manteghi; Khai D. T. Ngo

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Desired Properties of a Nonlinear Resistive Coating for Shielding Triple Point in a Medium-Voltage Power Module

Jiayu Xu; Zichen Zhang; Khai D. T. Ngo; Guo-Quan Lu

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The Fast Overvoltage Protection Consideration and Design for SiC-Based Matrix Converters

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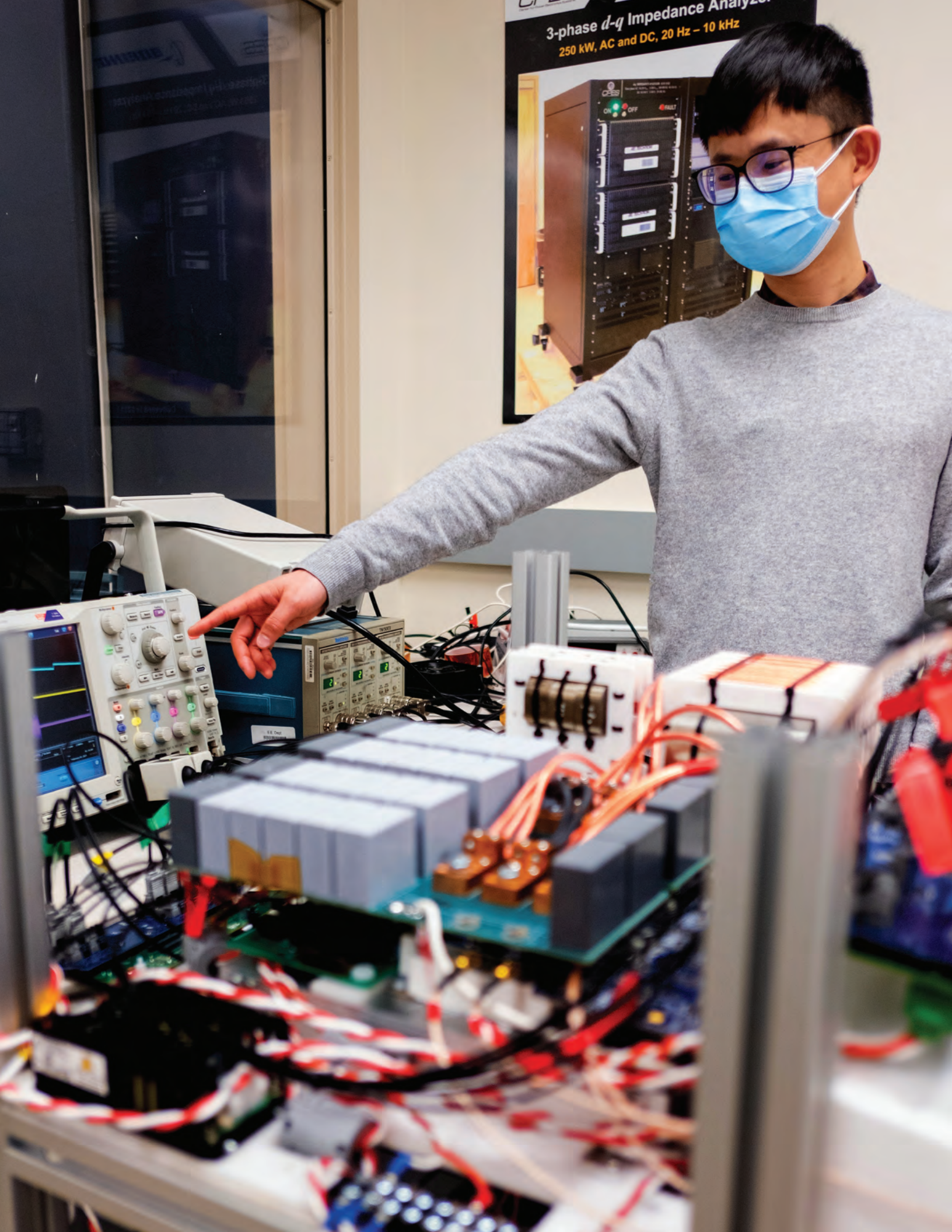
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Research Nuggets

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Reduced-Order Analysis and Circuit-Level Cost Function for the Numerical Optimization of Power Electronics Modules

The fast switching times and higher operating temperatures enabled by medium-voltage, wide-bandgap power devices have forced package designers to employ innovative technologies to improve power densities, lower stray parasitics, and increase cooling capability. These new technologies ultimately require new simulation tools to allow for fast, efficient, and accurate computation of the multi-physics phenomena that govern package performance. To that end, this work proposes a multi-physics optimization workflow (Fig. 1) that uses reduced-order partial element equivalent circuit (PEEC) modelling to efficiently model the electromagnetic and thermal performance of power electronics packages.

Employing reduced-order PEEC as the forward solver, as opposed to more conventional finite element techniques, provides both decreased simulation time (up to 100x) as well as access to time domain simulation outputs of the package operating in a converter. This enables the designer to efficiently model the voltage and current transient stresses on the package during continuous operation of the device and relate these stresses to the material and geometric design decisions. The addition of time-domain simulation results in the optimization allows for a wide range of possible cost functions that prioritize performance of the package in a converter.

One such cost function is proposed in the work and demonstrated on a 10 kV/25 A discrete SiC MOSFET package with double-sided cooling (Fig. 2). The proposed cost function utilizes the time domain outputs of the reduced-order PEEC to optimize the position of the die in the package, based on the power noise spectrum emitted by the package during 100 kHz hard-switching. On standard desktop hardware, the optimal die position is determined in ~30 iterations of the optimizer at a rate of 15 min/iteration. During each iteration, a time-domain simulation electrical simulation (10 μs duration and 100,000 time steps) and a steady-state thermal simulation are completed. This work demonstrates both the reduction in computational time and the improved flexibility of power electronics package optimization enabled by reduced-order PEEC.

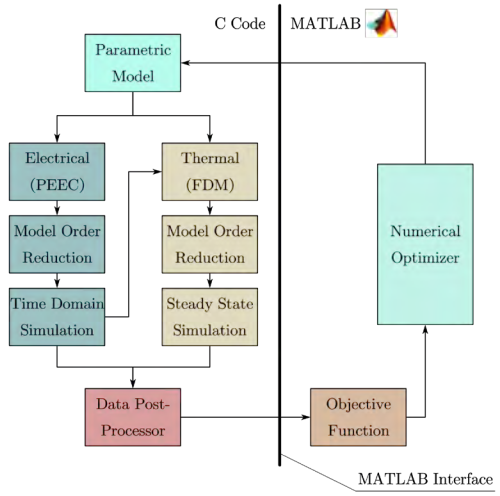


Fig. 1. Reduced-order PEEC workflow for EM and thermal optimization.

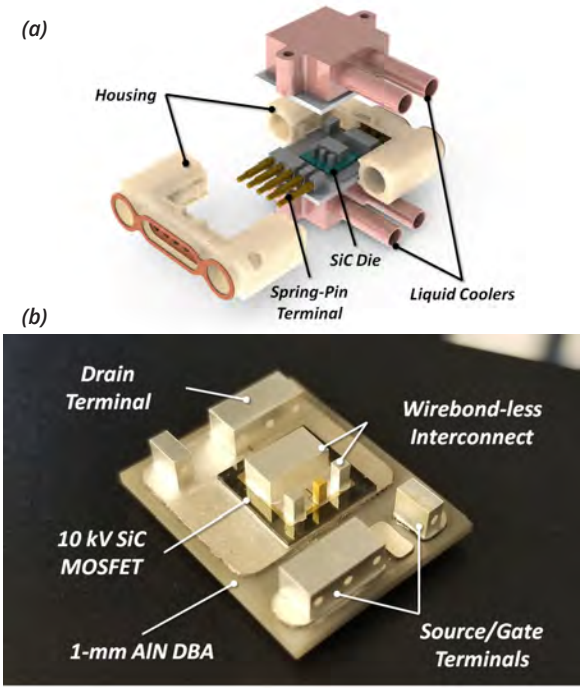


Fig. 2. Optimized 10 kV/25 A discrete SiC MOSFET package. (a) Exploded rendering of the package showcasing the lateral spring-pin terminals and double-sided cooling. (b) Package during assembly process.

PCB-Based Inductor Design – Benefits and Limitations

With recent advances in wide-band-gap (WBG) power semiconductor devices, namely, SiC and GaN, there have been significant improvements in efficiency and power density in power electronic circuits, as compared to the current practice using silicon counterparts. Furthermore, with substantial higher operating frequency, the integration of magnetic components with embedded windings in the printed circuit board (PCB) is feasible. In certain isolated areas, design paradigms integrate transformers with embedded PCB windings to improve the power density, manufacturability, and electromagnetic interference (EMI). The PCB winding-based transformer is able to maintain a similar winding loss compared to the litz wire version by using perfect winding interleaving. On the other hand, in certain power supplies where PCB winding-based inductors are implemented, a dramatic increase in losses has been observed in an extended power range.

In this paper, the fundamental limitation of the PCB winding-based inductor is identified: the increased winding losses due to the cumulative effect of the magnetomotive force. Based on the understanding of the loss mechanism, an approach to reduce the PCB winding loss is presented by breaking down one inductor into several elemental inductors with a fewer number of winding layers. The feasible power range of each elemental inductor unit is studied. Furthermore, a modular approach to extend the power range of PCB-based inductors while maintaining a similar efficiency as the litz wire inductor is discussed. As shown in Fig. 1, the balance technique is incorporated into the inductor design to suppress the common mode noise emission of non-isolated converters, such as the totem-pole PFC circuit. A PCB-based inductor example for a 3 kW datacenter server power supply is given to illustrate the benefits of the proposed approach, as shown in Fig. 2.

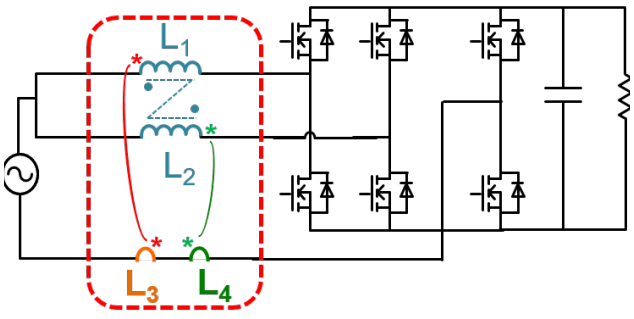


Fig.1. Two-phase interleaved totem-pole PFC converter.

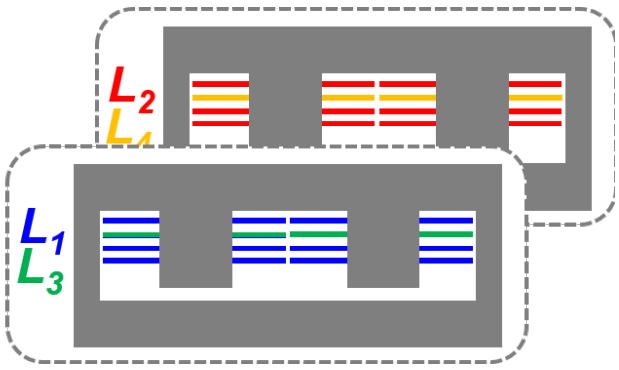


Fig. 2. Proposed inductor with embedded PCB winding.

Improved Measurement Accuracy for Junction-to-Case Thermal Resistance of GaN HEMT Packages by Gate-to-Gate Electrical Resistance and Stacking Thermal Interface Materials

The application of gallium nitride high-electron mobility transistors (GaN HEMTs) in power converters has the potential to further increase efficiency and power density due to their low conduction loss, low switching loss, and high temperature capability. However, packaging these fast-switching devices is challenging because of the requirement for low parasitics and low junction-to-case thermal resistance, R_{thJC}. One of the first steps in developing a device or module package is to design the package structure and select the materials. This is followed by running electrical and thermal simulations to determine package parasitics and thermal resistances. Experimental verification of the electrical and thermal simulations is key to ensure the success of a package development. Of the two, thermal measurements are more difficult and generally less accurate. This is especially true for GaN packages, thus hampering the development of GaN packaging. The main challenge of measuring R_{thJC} of a GaN package is the lack of accurate temperature-sensitive electrical parameters (TSEPs) to determine the device's junction temperature.

The common TSEPs of a GaN HEMT lack sufficient sensitivity or stability due to the charge-trapping effect from the device-switching action. Recently, researchers fabricated GaN HEMT devices with two gate pads. This research showed that the gate end-to-end or gate-to-gate electrical resistance, R_{g2g}, can be used as a reliable TSEP; however, because they did not fabricate packages for their devices, they did not apply the technique to measure R_{thJC}.

In this work, a commercial (650 V, 150 A) eGaN device with two gate pads is packaged for the purpose of accurately measuring R_{thJC} of the GaN package, as shown in Fig. 1. Two techniques are combined to improve the accuracy: 1) using R_{g2g} as the TSEP, and 2) making multiple thermal resistance measurements with stacked layers of a thermal interface material (TIM). The stacked-TIM technique is employed to reduce inaccuracy in determining the package case temperature. The measurement procedure is tested using two different types of the TIM on a custom package of an eGaN (650 V, 150 A) HEMT. In Fig. 2, the two measured R_{thJC} are found to be within 24 % of each other.

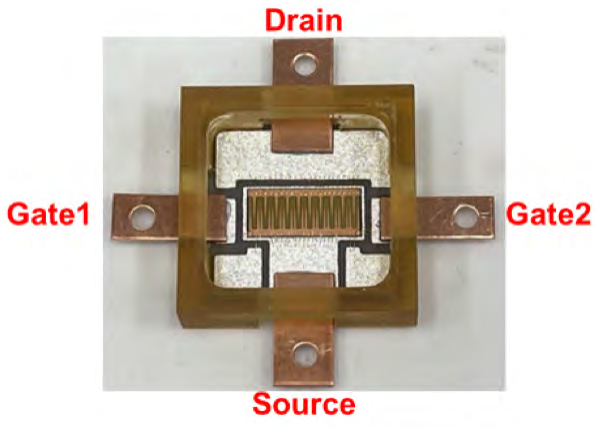


Fig. 1. Top view of a completed eGaN package.

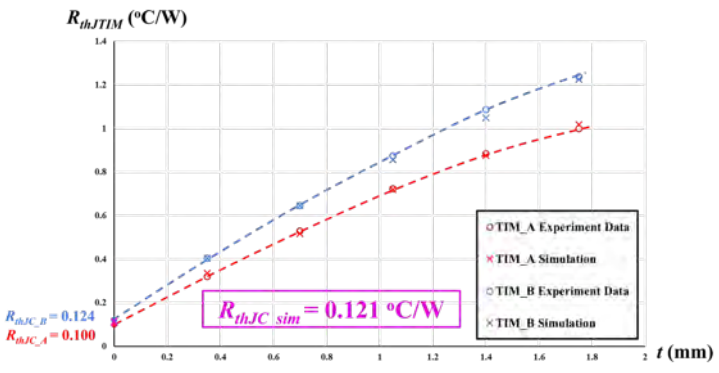


Fig. 2. Plots of the measured (red and blue circles) and simulated (red and blue crosses) junction-to-TIM thermal resistances with each TIM type. The dash lines are the fitted curves. The intercepts of the fitting curves on the y-axis are the experimentally determined R_{thJC}.

Characterization of a Nonlinear Resistive Polymer-Nanoparticle Composite Coating for Electric Field Reduction in a Medium-Voltage Power Module

Emerging medium-voltage (MV) silicon carbide (SiC) device technologies offer the opportunity to reduce the complexity and increase the efficiency of power electronics in various power-grid applications. However, before the MV devices can be widely adopted, innovative solutions for their packaging, especially their insulation, are needed. With their reduced size and increased voltage rating, the insulation materials in the power modules, such as the insulated metal substrate and the encapsulant, are under much higher electric field (E-field) intensities. This can lead to dielectric failure or partial discharge (PD) that reduces the lifetime of the module. Given that the MV wide-bandgap devices are expected to handle higher heat fluxes because of their higher-rated current densities (as compared to their silicon counterparts), an insulation solution that trades off thermal performance for meeting the insulation requirement is not ideal.

Previously, a simulation study was completed to find the desired properties of a nonlinear resistive material for reducing the E-field intensities at the triple-point (TP) edges on a direct-bonded copper (DBC) substrate. The study was aimed at providing a guideline for materials engineers to develop effective field-reduction materials.

In this work, a polymer-nanoparticle composite material is characterized as a field-reduction coating of the triple point on a medium-voltage power module substrate. The electrical conductivity of the material shows nonlinear dependence on the E-field intensity with a switching field at around 15 kV/mm. Patterned DBC substrates, as shown in Fig. 1, with their triple points along the edges of the electrodes, are coated with about 20 μm thick of the material; their PDIVs are measured in a silicone gel. The coating increases the PDIVs of the substrates by over 85 % in the gel, as shown is Fig. 2. The significant increases in PDIVs of the coated substrates obtained in the gel are found to be in good agreement with the simulated reduction of the maximum E-field intensity in the gel. These findings offer an experimental validation of a practical nonlinear resistive material for E-field grading in MV power modules.

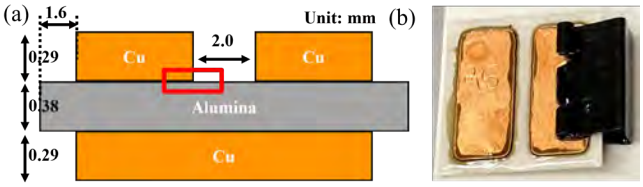


Fig. 1. (a) Schematic of the DBC test coupon, and (b) photo of a coated DBC sample after silicone encapsulation.

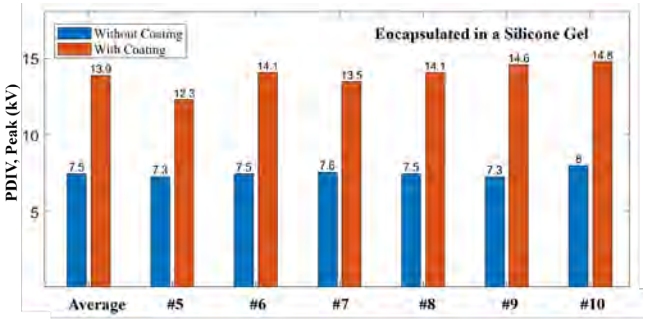


Fig. 2. PDIVs of the DBC samples with and without the coating measured with the silicone gel encapsulation.

Effects of Underfill Properties on the Thermo-Mechanical Reliability of Double-Side Cooled (DSC) Power Modules

Double-side cooled (DSC) or "sandwich type" power modules are packages of power semiconductor devices that can be cooled from both sides of the devices, thus offering lower junction-to-case thermal resistance and higher power density. DSC power modules also have lower parasitic inductances. However, they are structurally more rigid than the traditional single-side cooled (SSC), wire-bonded modules, raising concerns about their thermomechanical reliability.

This work aims to gain a better understanding of the thermomechanical reliability of DSC power modules. More specifically, it focuses on understanding the effects of various material properties of the encapsulation or underfill used for packaging the devices, on the module reliability.

A series of finite element analysis (FEA) simulations is designed to investigate the thermo-mechanically induced stresses and strains inside a typical DSC package, as modeled in Fig. 1. The model package consists of two parallel direct-bonded copper (DBC) substrates: one device bonded on one substrate, two metal posts connecting the device to the other substrate, and an underfill filling the empty space in between. The package is assumed to undergo accelerated tests, such as temperature-cycling and power-cycling. Isotropic elastic and isotropic viscoelastic (such as Anand) models are used to describe the mechanical behaviors of the materials.

Anticipated results of the FEA simulations will help elucidate 1) the locations where inside the package the thermal stresses and strains are concentrated, 2) the effects of underfill on those stresses and strains, and 3) which material property or properties of the underfill is or are more effective for improving the reliability of the module.

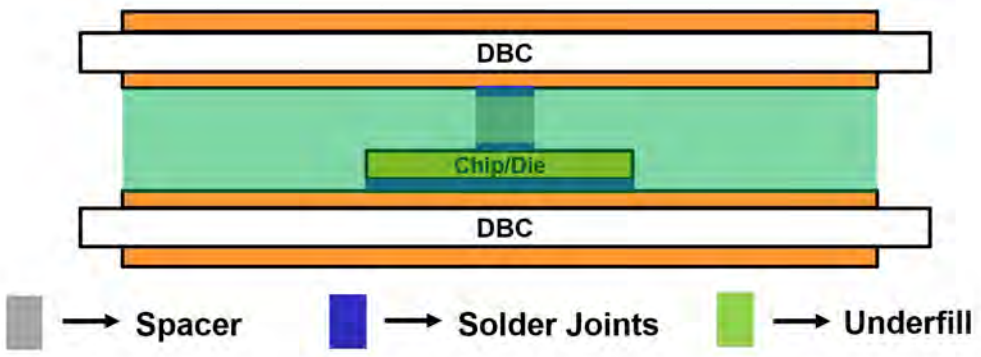


Fig. 1. DSC package layout with labels utilized in the FEA simulations.

Steady-State Analysis of Series-Resonator Buck Converter

Interleaved multiphase buck converters have been adopted for point-of-load regulation below 3.3 V and above 10 A from input voltage exceeding 12 V. The Series-Capacitor Buck (SCB) converter is synthesized by adding a series capacitor in a two-phase buck converter to reduce voltage stresses under steady state. Side benefits include doubling of the duty cycle, reduction of the switching loss, and equalization of the phase currents. Hard switching hinders efforts to reduce volume through increasing the switching frequency, although a monolithically integrated SCB converter boosts current density exceeding 60 A/cm^3 in. The efficiency drops by 5 %, owing to the switching loss, as the frequency increases from 1 MHz to 3 MHz.

The Series-Resonator Buck (SRB) converter is synthesized by adding a parallel resonant tank next to the series-capacitor C_s, as demonstrated in Fig. 1. All switches turn on into zero-voltage (ZVOn), and low-side switches turn off from zero-current (ZCOff). No snubber is needed to keep the switches' stresses within the input voltage. A 2 MHz prototype with 48 V at the input, and 7 V, 20 A at the output, is built to verify the design.

The peak efficiency of the RSCB prototype is 98.5 %, and the full load efficiency is 97.3 %, as shown in Fig. 2. The measured drain-source voltages of all switches at nominal condition are shown. All switches turn on into zero-voltage.

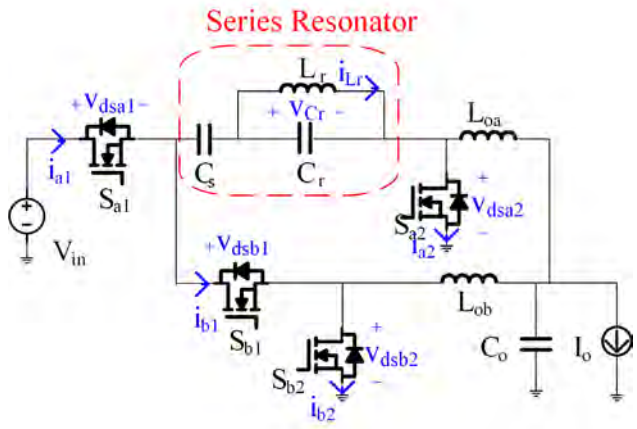


Fig. 1. Series-Resonator Buck (SRB) converter.

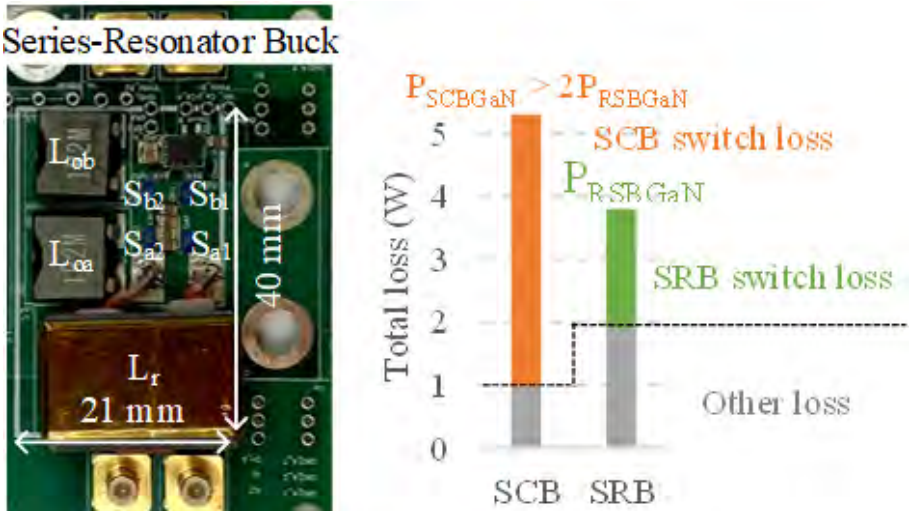


Fig. 2. Prototype and loss reduction compared with a conventional SCB converter.

A Constant-Current Class-E with Air-Core Transformer

Current source is used in gate drivers, battery chargers, and wireless power transfer. The Class-E converter is a good candidate for the application because only one switch is required and ZVS is achieved. This work proposed an isolated Class-E, dc-dc converter with constant-current (CC) output and ZVS over a wide load range with finite input inductance. An air-core transformer is used for the isolation stage for a lower profile and elimination of core loss. The air-core transformer with PCB winding has two planar layers. The radius is 5 mm. The drawing of the air-core transformer and the hardware is shown in Fig. 1.

The converter can be separated with a Class-E inverter and a compensation network. The Class-E inverter can be equalized with a voltage source in series with a capacitor. The fundamental output voltage can be constant if the capacitor is compensated at a certain switching frequency and the load is resistive. The CC output is realized by adding a CLC network to the Class-E inverter. Capacitor C1 and C2 compensate the self-inductance at the primary side and secondary side to realize a resistive load. For duty ratio (D) equal to 0.5, the switching frequency needs to be 1.29 of the resonant frequency of L_{in} and C_{in}. The leakage inductances L_{l1} and L_{l2} need to be large enough to suppress high-order harmonics. In this work, the self-inductance is 600 nH and the mutual inductance is 360 nH. The switching frequency is 6.78 MHz and the output current is 700 mA.

Fig. 2. shows the testing results with 10 V input and different load resistances. ZVS is always maintained within the load range and output voltage increases linearly with the load resistance, which is the characteristic of CC output. The peak efficiency of the converter is 80%.

In summary, this work demonstrated the principle of realizing CC output on the Class-E, dc-dc converter with an air-core transformer. The work can be a good candidate for high-temperature and low-profile applications with the elimination of magnetic cores. The efficiency can be further improved by optimizing the air-core transformer and will be discussed in the future.

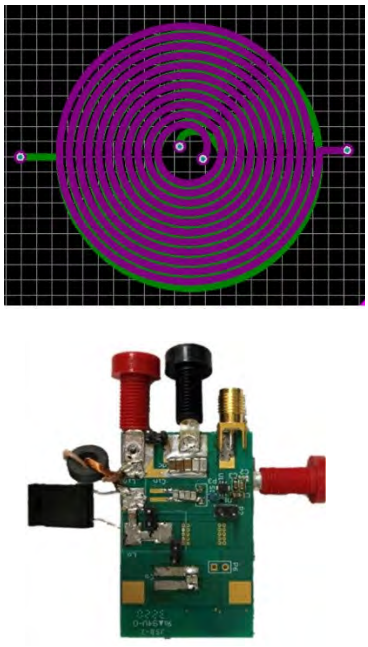


Fig. 1. Drawing of the air-core transformer and actual hardware.

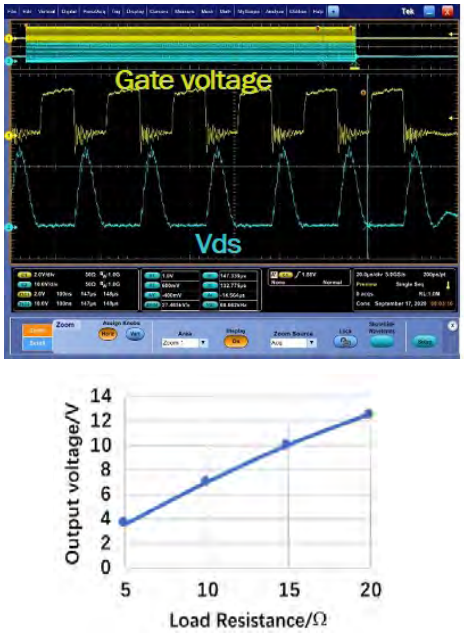


Fig. 2. Testing waveforms and output characteristic of the converter.

Low Thermal Resistance (0.5 K/W) Ga_2O_3 Schottky Rectifiers With Double-Side Packaging

The low thermal conductivity of Ga_2O_3 has arguably been the most serious concern for Ga_2O_3 power and RF devices. Despite many simulation studies, there is no experimental report on the thermal resistance of a large-area, packaged Ga_2O_3 device. This work satisfies this need by demonstrating a 15-A double-side packaged Ga_2O_3 Schottky barrier diode (SBD) and measuring its junction-to-case thermal resistance (R_{0JC}) in the bottom-side- and junction-side-cooling configurations. The R_{0JC} characterization is based on the transient dual interface method, i.e., JEDEC 51-14 standard, and the test setup is shown in Fig. 1. Fig. 2 shows the R_{0JC} of the junction- and bottom-cooled Ga_2O_3 SBD is measured to be 0.5 K/W and 1.43 K/W, respectively, with the former lower than that of similarly-rated commercial SiC SBDs. This low R_{0JC} is attributable to the heat extraction directly from the Schottky junction instead of through the Ga_2O_3 chip. The R_{0JC} lower than that of commercial SiC devices proves the viability of Ga_2O_3 devices for high-power applications and manifests the significance of proper packaging for their thermal management.

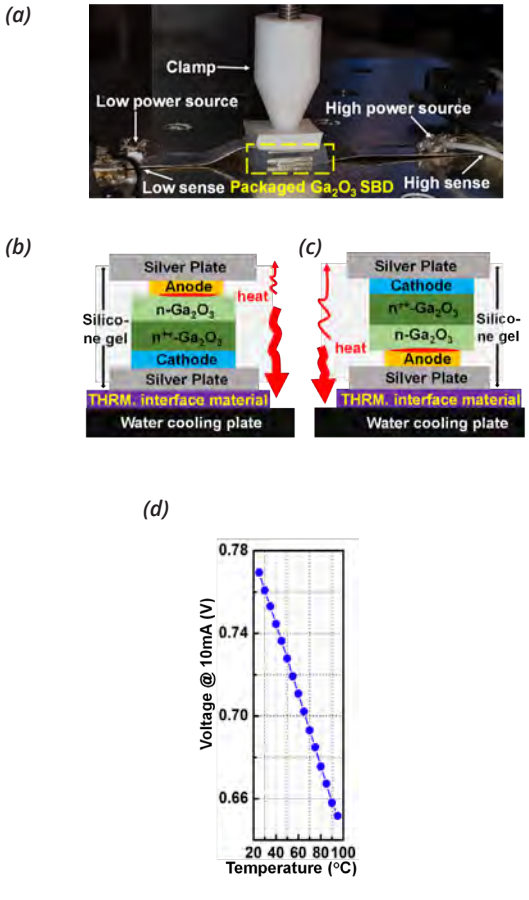


Fig. 1. (a) Photo of the test setup. Schematic of R_θ measurements under (b) bottom-side cooling and (c) junction-side cooling. (d) The forward voltage at 10 mA current as a function of temperature of the packaged Ga_2O_3 SBD.

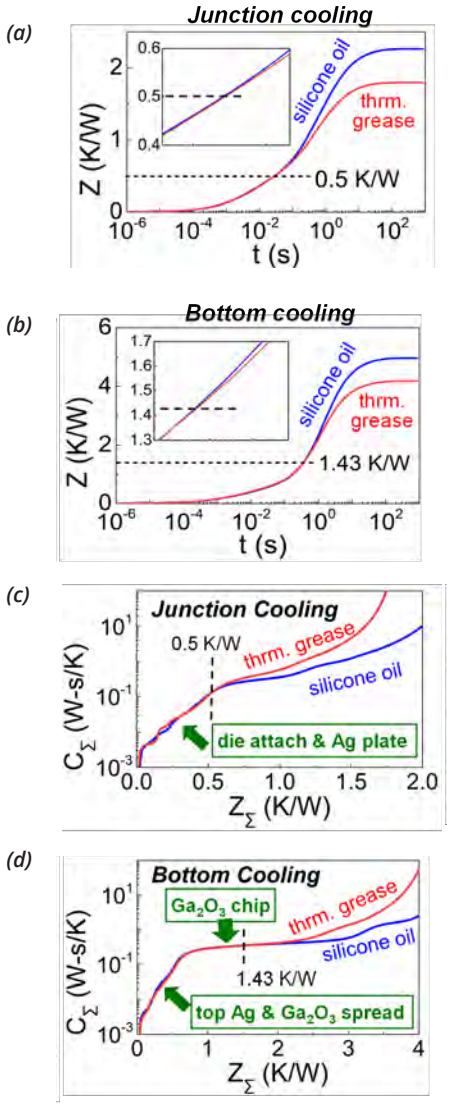


Fig. 2. Transient thermal impedance curves of the Ga_2O_3 SBD measured with two TIMs under the (a) junction- and (b) bottom-side cooling. The insets show the zoom-in plot of the separation point. Calculated structure function with two TIMs in the (c) junction - and (d) bottom-side cooling.

10 kV, 39 mΩ·cm² Multi-Channel AlGaN/GaN Schottky Barrier Diodes

High-voltage (HV, >1.7 kV) power rectifiers are needed in various power electronics applications, e.g., renewable-energy generation, industrial motor drives, electricity grids, and transportation. Bipolar Si diodes are commercially available up to 6.5 kV, but they suffer from slow switching speed. Unipolar SiC junction barrier Schottky (JBS) diodes up to 10 kV have been recently pre-commercialized by Cree. Commercial 3.3 kV+ SiC diodes are barely available due to high cost; their market penetration is still slow. This work demonstrates multi-channel AlGaN/GaN Schottky barrier diodes (SBDs) with a breakdown voltage (BV) over 10 kV, the highest BV reported in GaN devices to date.

The epitaxial structure consists of a p-GaN cap layer and five AlGaN/GaN channels continuously grown on a low-cost 4-inch sapphire substrate. Fig. 1(a) shows a reference sample with the p-GaN termination. A novel device design is proposed for electric field management, i.e., the p-GaN reduced surface field (RESURF) structure, which balances the net charges in the multi-channel at reverse biases (Fig. 1(b)). Fig. 2 benchmarks the $R_{ON,SP}$ *vs. BV* of the GaN SBDs with the state-of-the-art HV (BV > 2 kV) GaN SBDs, SiC JBS/SBDs, and Ga_2O_3 SBDs. The SBD with a 98-μm anode-to-cathode length (L_{AC}) shows a BV of 9.15 kV and a specific on resistance (R_{ON}) of 29.5 mΩ·cm², rendering a Baliga's figure of merit (FOM) of 2.84 GW/cm². The SBD with a 123-μm L_{AC} shows a BV over 10 kV and a R_{ON} of 39 mΩ·cm², which is 2.5-fold lower than the R_{ON} of the state-of-the-art 10 kV SiC junction barrier Schottky diodes. The Baliga's FOMs of the proposed 4.6-10 kV GaN SBDs well exceed the SiC unipolar limit. These results show the great promise of GaN for medium- and high-voltage power electronics.

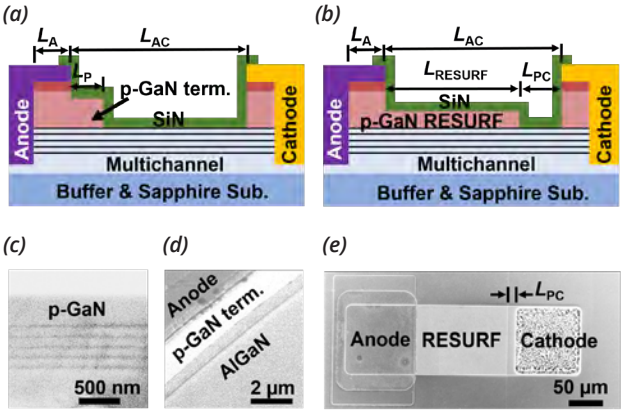


Fig. 1. Schematics of the multi-channel AlGaN/GaN SBD with (a) p-GaN edge termination, and (b) p-GaN RESURF. (c) Cross-sectional SEM images of the p-GaN/multi-channel region. (d) SEM image of the p-GaN edge termination region. (e) Top-view SEM image of p-GaN RESURF SBD.

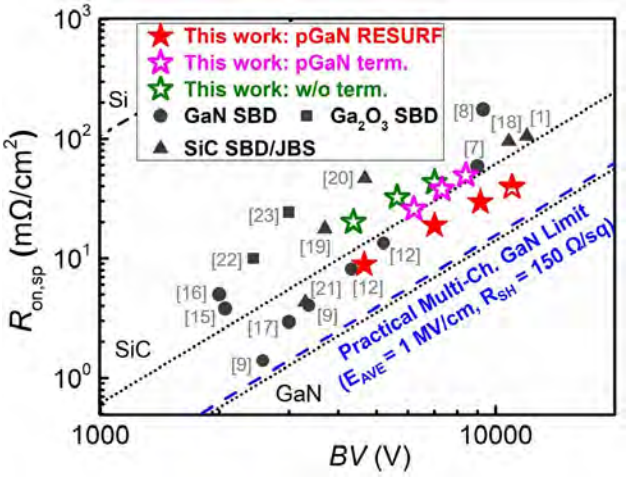


Fig. 2. Differential $R_{ON,SP}$ vs. BV benchmark for proposed SBDs and the state-of-the-art GaN, SiC, and Ga_2O_3 HV SBDs. Si, SiC, GaN bulk limits and the multi-channel lateral AlGaN/GaN limit are also plotted.

Power Management Consortium (PMC) Nuggets

High-Efficiency High-Density 6 kW 400/48 V Power Supply for Data Centers

The LLC converter is considered the most efficient topology in server and telecom applications. Additionally, it has been demonstrated that three interleaved LLC converters can achieve further efficiency improvement at several kilowatts power level. However, the magnetic components for multiphase LLC converters are complex, bulky, and difficult to manufacture in a cost-effective manner. In this work, a high-frequency GaN-based, three-phase LLC converter is utilized, attempting to address these challenges. With GaN operating at 500 kilohertz, all magnetic components, namely three inductors and six transformers, can be integrated in one common structure while all magnetic windings are contained in a compact 4-layer PCB with 3 oz. copper. The proposed structure can be easily and cost-effectively manufactured in high quantities. Furthermore, up to a 20 db reduction of common-mode noise, from 150 KHz up to 30 MHz, can be realized if 2 additional PCB layers are employed for proposed CM noise shielding. A 6 kW 400 V/48 V 3-phase prototype will be implemented, with an expected peak efficiency of 99 % and a power density of 900 W/in^3 (56 kW/L).

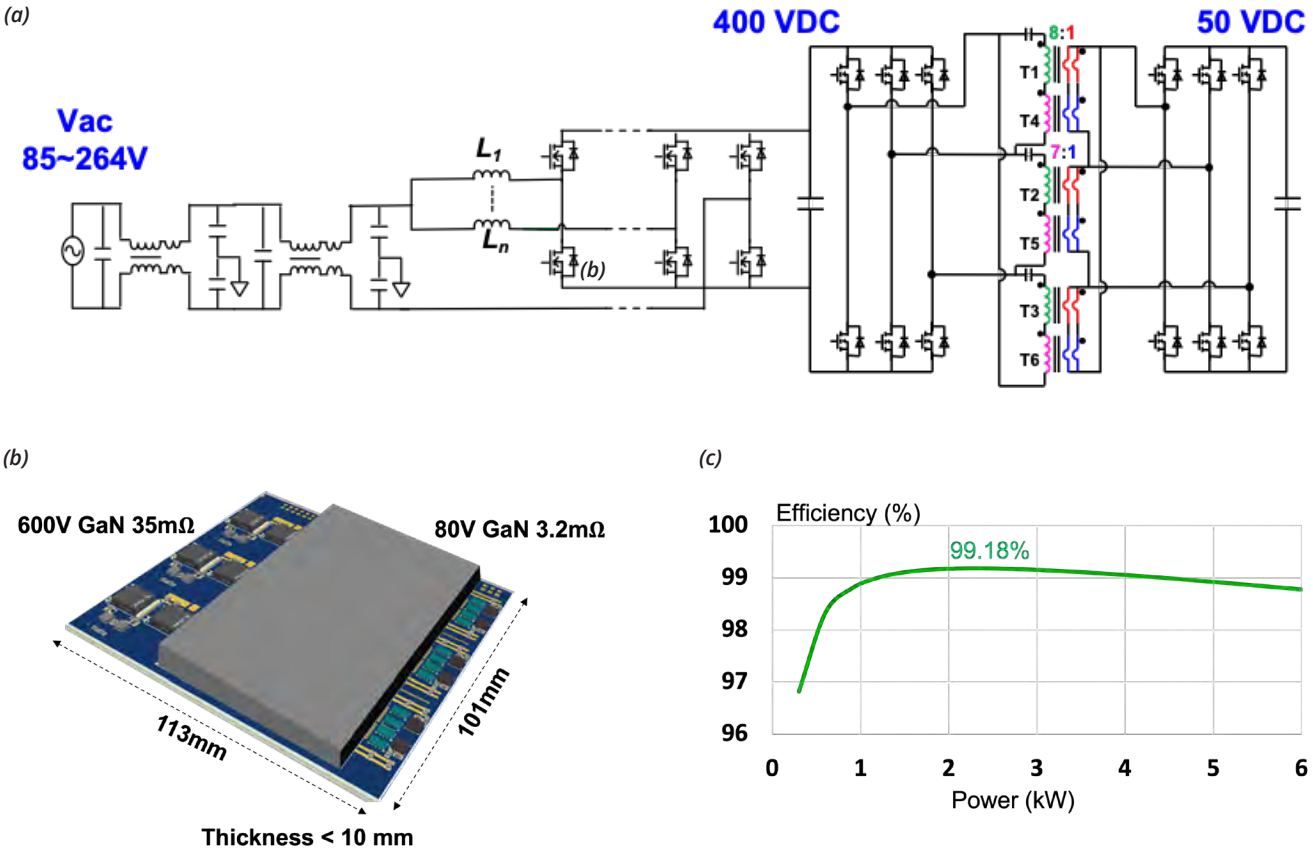


Fig. 1. (a) Circuit. (b) Hardware prototype. (c) Tested efficiency.

Light-Load Efficiency Improvement of Three-Phase CLLC Resonant Converter for On-Board Charger Applications

The three-phase CLLC (3PCLLC) resonant converter, as shown in Fig. 1, is a good candidate for the on-board-charger application due to the low-current stress it incurs on the device, its automatic current-balancing among phases, and its good interleaving. However, the efficiency at light load is sacrificed as a result of its higher number of switching devices, driving circuits, and magnetics. To improve the efficiency and achieve bi-directional energy transfer, synchronous rectifiers (SRs) can be adopted. The conduction time of the SR will impact the operation of circuits, gain characteristics, and efficiency. In this work, the SR ON-time is extended to achieve negative current for better regulation capability and light-load efficiency improvement. A new phase-shedding method for the 3PCLLC converter is proposed and analyzed. By shutting down one or two bridges as the load current decreases, the light-load efficiency increases significantly. Experiments are implemented on an 11 kW 3PCLLC converter with 500 kHz operation frequency to verify the extended SR ON-time control and the phase shedding method. These results show an improvement of more than 9 % under 20 % load output conditions, as shown in Fig. 2.

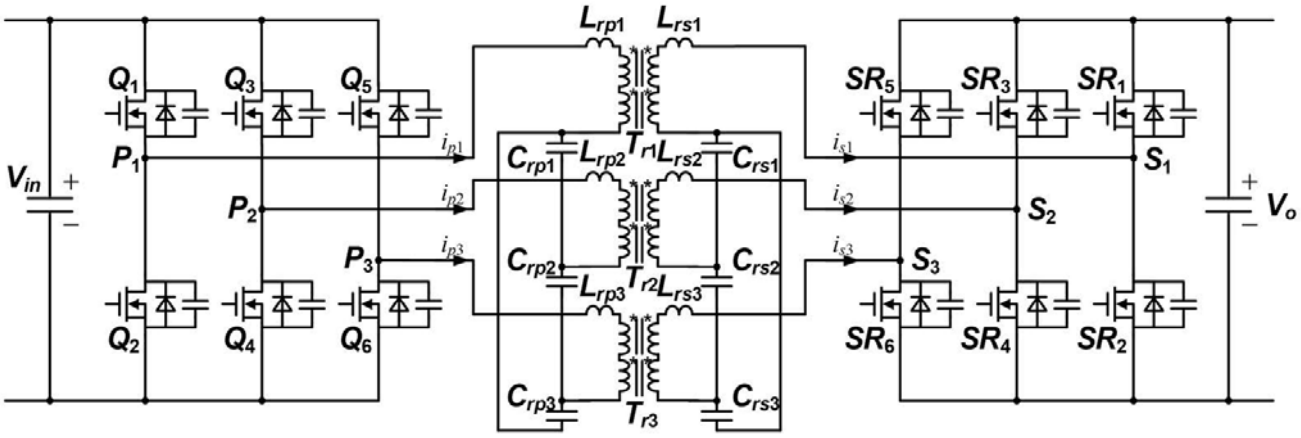


Fig. 1. Diagram of the three-phase CLLC resonant converter.

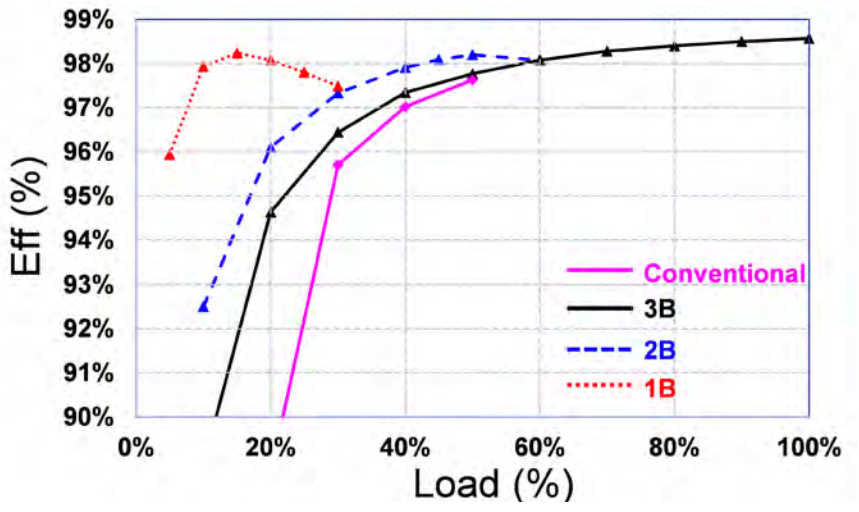


Fig. 2. Efficiency curves of 3PCLLC converter with light-load efficiency improvement control strategy.

Adaptive-Coupled Inductors for Multiphase Voltage Regulators

As modern microprocessors continuously advance, a high-efficiency, high-power-density voltage regulator design with fast transient response is a must. Compared with the non-coupled-inductor-based solution, a multiphase buck converter with an indirect-coupled inductor (also named TLVR) can dramatically improve the circuit transient response without increasing the inductor current ripple and sacrificing the efficiency. However, a design conflict between the steady-state performance and transient response exists for the traditional indirect-coupled inductor structure with a given inductor size.

To solve this issue, this work proposes an adaptive-coupled inductor structure as shown in Fig. 1. This is realized by applying a variable inductor in the additional winding loop of an indirect-coupled inductor. By varying the coupling coefficient during the steady-state operation and load transients, the proposed inductor structure can help the multiphase buck converter achieve a faster transient speed while maintaining the same steady-state current ripple, as compared with the traditional indirect-coupled inductor. The coupling coefficient in the proposed structure is self-adjusted according to the circuit working conditions. Therefore, the proposed structure can be easily implemented without increasing the control complexity and cost. Furthermore, the inductor size of L_c can be dramatically reduced.

A four-phase buck converter with the proposed inductor structure is experimentally tested, and a 25.6 % output voltage overshoot reduction can be realized by the proposed coupled inductor structure, as shown in Fig. 2.

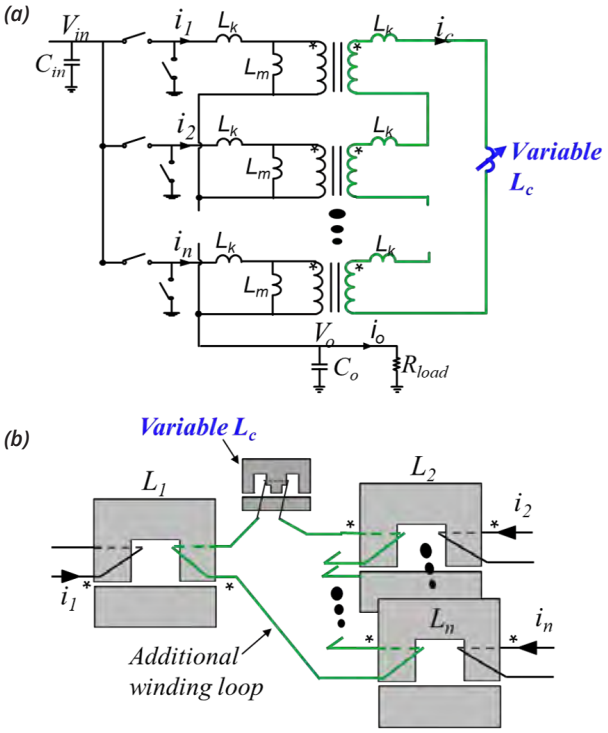


Fig. 1. Multiphase buck with an adaptive-coupled inductor. (a) Equivalent circuit. (b) Inductor structure.

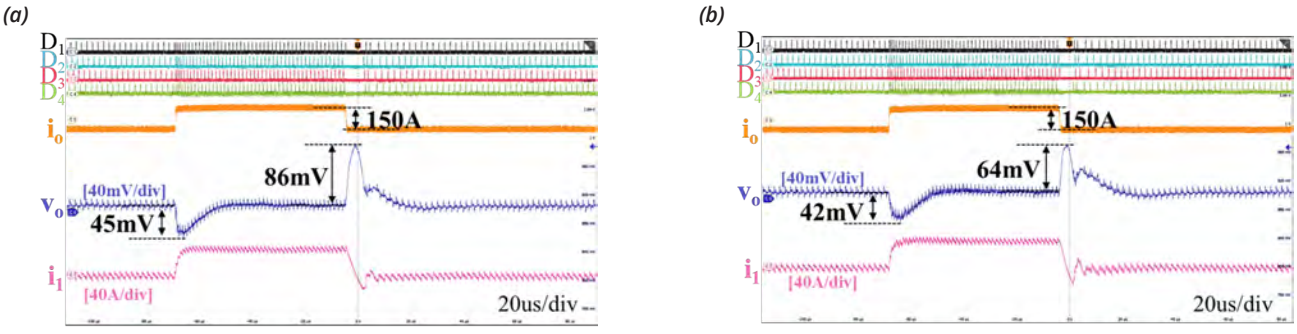


Fig. 2. Load transient response comparison. (a) Traditional coupled inductor. (b) Proposed coupled inductor.

Low-Profile and High-Efficiency 3 kW 400 V-48 V LLC Converter With a Matrix of Four Transformers and Inductors for 48 V Power Architecture for Data Centers

The use of cloud computing services is surging at a rapid rate. These trends serve as motivation to improve the cost efficiencies of building data centers, either by reducing initial construction cost or increasing Power Usage Effectiveness (PUE) to reduce running costs. In 2020, OCP V3 was released to modify the 48 V bus to a more efficient structure. A narrow range 48 V bus is proposed where the bus voltage is fixed to 50 V during normal power delivery conditions. In the case of an energy shortage, the power flow is switched naturally to the BBU when the bus voltage drops to 48 V. This solution offers multiple advantages such as enabling efficient 4:1 fixed ratio converters to downstream conventional 12 V PoL converters, thus eliminating oversized current/voltage designs.

In this work, a high-efficiency and low-profile design is proposed for the 48 V LLC converter for the data center. The converter utilizes PCB magnetics for better thermal management, easy assembly, and lower cost. The matrix transformer is optimized through multiple aspects. The number of elemental transformers is selected based on the required number of parallel SRs. The turns number of 2:2 per elemental transformer is found to achieve better light load efficiency compared to the 1:1 turns ratio, as the core loss reduces. The switching frequency is optimized, and 250 kHz is found to have the least total converter loss, given the selected devices and ferrite material. The matrix inductor concept is presented to reduce PCB inductor winding loss and reduce thermal stress on the PCB. The matrix inductor concept helps to avoid the extreme increase in ac resistance due to the MMF build-up. The ac resistance is found to be reduced by a factor of 1/7 in the case of a 4 turn inductor. The converter achieves 98.8 % efficiency and 600 W/in^3 power density. The converter has an extremely low profile of < 11 mm. This reduces the PCB-to-air thermal resistance and facilitates thermal management.

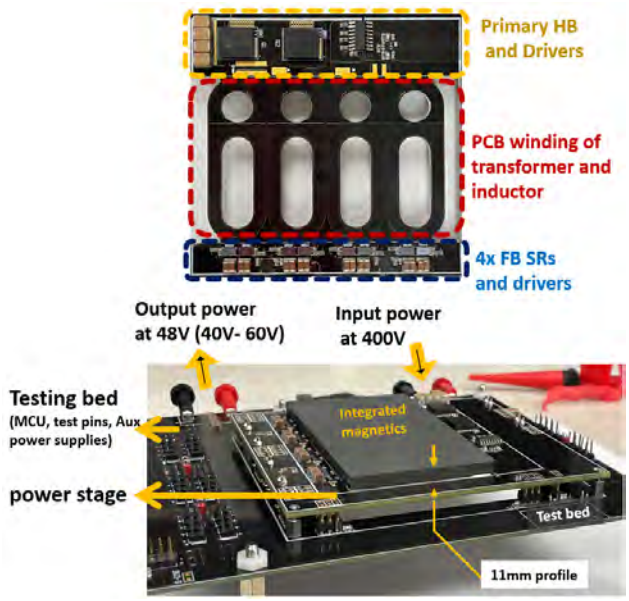


Fig. 2. Hardware prototype of 400 V- 48 V 300 kHz LLC with integrated PCB magnetics.

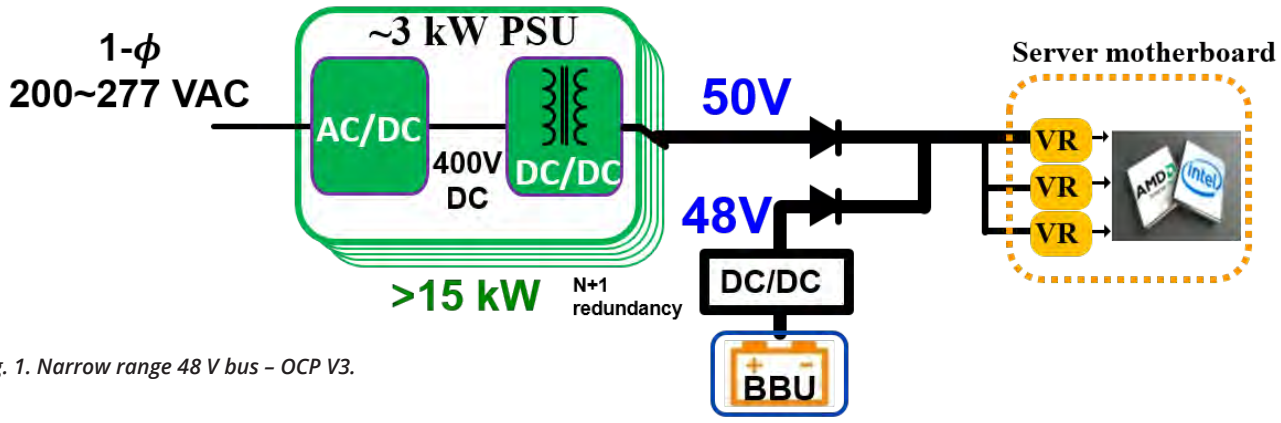


Fig. 1. Narrow range 48 V bus – OCP V3.

PCB Winding Coupled Inductor Design and Common-Mode EMI Noise Reduction for Soft-Switching Three-Phase AC-DC Converter

A critical conduction mode (CRM)-based soft-switching three-phase ac-dc converter with SiC power devices can achieve high-power density and high efficiency at hundreds of kHz switching frequency. One of the major concerns for the converter is the conducted electromagnetic interference (EMI) noise. Because of the fast-switching characteristic of SiC power devices, di/dt and dv/dt of the switches are much higher than those with Si power devices. In particular, the high dv/dt at the switching node of phase legs is seen over the parasitic capacitance between the power circuit and the ground, and generates substantial common mode (CM) EMI noise. A large CM filter is needed between the converter and the ac source in order to abide by electromagnetic compatibility (EMC) requirements. This depreciates the benefits from using SiC power devices with CRM at high-switching frequency, the small-size inductors for the power stage, and the small DM filter.

A balance technique can effectively lessen the CM noise. In Fig. 1, the two-channel interleaved three-phase ac-dc converter with the balance technique is presented.

The circuit topology requires the additional return path connecting from the middle point of the dc capacitors, *m*, to the neutral point of the ac filter capacitors, *n*. In the return path, additional inductors are placed to form a balanced structure. The inductors on the return path are coupled with the inductors in the main circuit for better balance at high frequency.

The converter is implemented with PCB winding magnetics. The PCB winding coupled inductor needs to be carefully designed by taking into account a variety of considerations: 1) winding configuration to minimize the winding loss, 2) placement of the return path to maximize the coupling between the main inductors and the additional inductors, 3) coupling coefficient between the main inductors to reduce switching frequency range, device loss, and core loss, 4) turns number of the main inductors to balance out the winding loss and the core loss. By properly designing the PCB winding inductor, CM Noise can be effectively reduced, up to almost 15 MHz, as shown in Fig. 2.

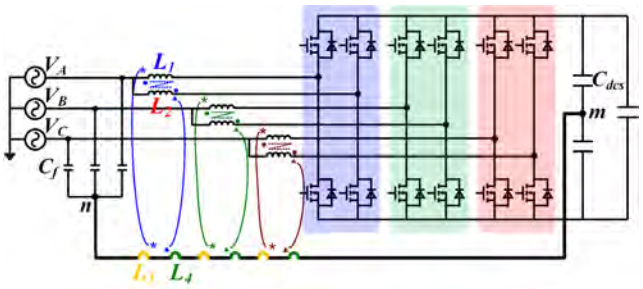


Fig. 1. Circuit topology for two-channel, interleaved, three-phase ac-dc converter with balance technique.

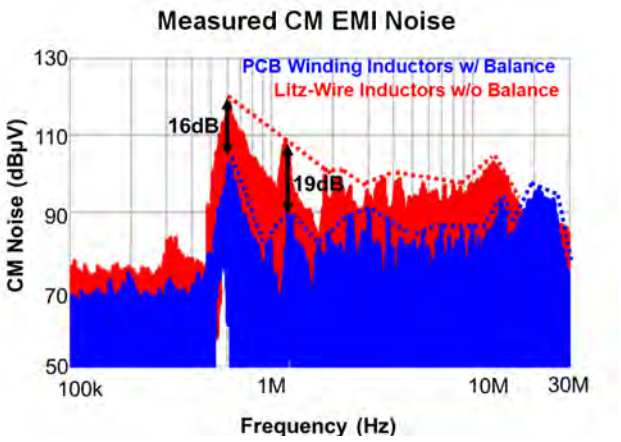


Fig. 2. Comparison of measured CM EMI Noise between litz-wire inductor without balance technique and PCB winding coupled inductor with balance technique.

300 A Single-Stage 48 V Voltage Regulator With Multiphase Current Doubler Rectifier and Integrated Transformer

High-current, high-power-density 48 V voltage regulator modules (VRMs) are critical for 48 V data center power architecture. In this work, a single-stage 48 V converter with multiphase current doubler rectifiers is proposed for CPUs in data center applications, as shown in Fig. 1. The magnetizing inductors of the matrix transformer are used as the output inductors of the multiphase current doubler rectifier. A magnetic integration structure for the matrix transformer is proposed and optimized, which creates negative coupling between multiphase current doubler rectifiers. With GaN devices as primary side devices and low-voltage silicon devices as secondary synchronous rectifiers (SRs), the proposed converter can achieve high-efficiency and high-power density. A 48/1.8 V 300 A converter is designed, which can reach a peak efficiency of 92.7 %.

The prototype of the multiphase current doubler rectifier is shown in Fig. 2. With the proposed integrated multiphase current doubler rectifier, the footprint is 21 mm × 50 mm, and the thickness is 4.45 mm. The compact prototype means the power density can reach 1.9 kW/in^3 and 332 W/in^2 under 300 A output current and 1.8 V output voltage. Even if the 160 A continuous current is considered, the power density can still be larger than 1 kW/in^3.

The footprint of the 48/1.8 V prototype is compared with the state-of-art 12/1.8 V multiphase buck converter with the same output current ability. Furthermore, in Fig. 2, it is observed that the secondary side gate drivers, which are highlighted with red boxes, take a great many footprints. If the gate drivers are integrated into the secondary SRs, which is a common practice for commercial products, the footprint can be further reduced to 21 mm × 42 mm. This means a smaller footprint than the state-of-art 12/1.8 V multiphase buck converter. The proposed 48/1.8 V converter sets a new record of power density for single-stage 48 V solutions.

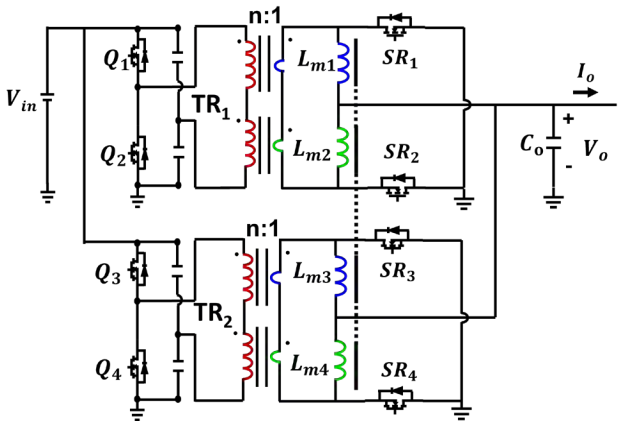


Fig. 1. Schematic of the proposed converter with integrated multiphase current doubler rectifier.

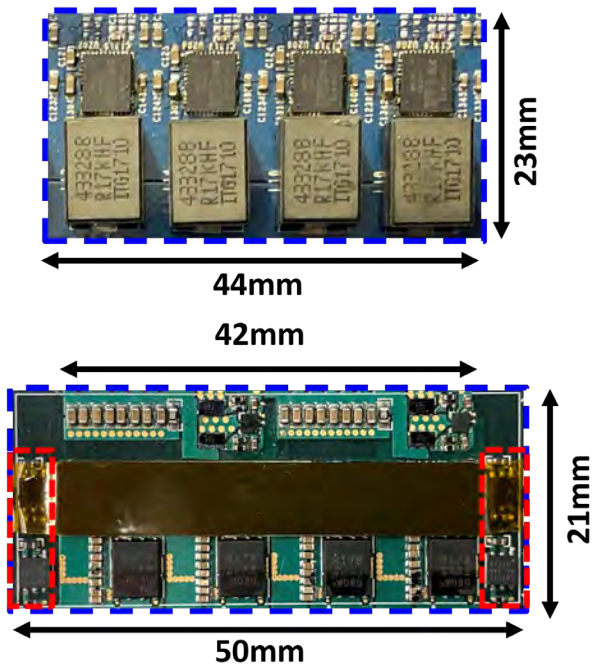


Fig. 2. Comparison between the 12/1 V multiphase buck converter and proposed 48/1 V converter.

A Microcontroller-Based High-Efficiency Critical Conduction Mode Control for GaN-Based Totem-Pole PFC

Power factor correction (PFC) rectifiers are widely used in electric vehicle (EV) chargers and in power supplies for telecommunication or data centers to achieve unity power factor (PF) and restrain total harmonic distortion (THD). The totem-pole PFC rectifier is well known for its simple topology. Recently, the totem-pole PFC rectifier has become popular again with the help of the high-voltage Gallium-Nitride (GaN), high-electron-mobility-transistor (HEMT).

In this work, a microcontroller-based control method for the GaN-based critical conduction mode (CRM) totem-pole PFC is proposed. A simple digital control method, based on synchronous rectifier (SR) on-time calculation, which ensures zero-voltage switching (ZVS) without zero current detection (ZCD), is proposed. Average current mode control is discussed and a compensator gain adjustment method is introduced to improve PF and restrain THD. Finally, all control functions are integrated in a microcontroller unit (MCU) and demonstrated on a 2.2 kW GaN-based, two-phase interleaved CRM totem-pole PFC prototype, as shown in Fig. 1. Fig. 2 shows the control diagram.

The prototype with the proposed control method can reach a peak efficiency of 98.96 % and full load efficiency of 98.55 %. The converter reaches a PF of 0.996 at full load.

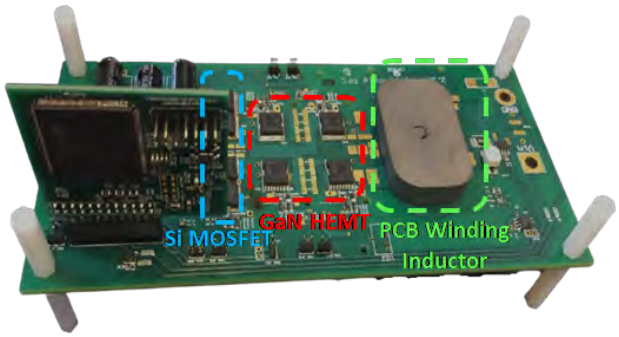


Fig. 1. 2.2 kW two-phase interleaving, GaN-based, CRM totem-pole PFC prototype.

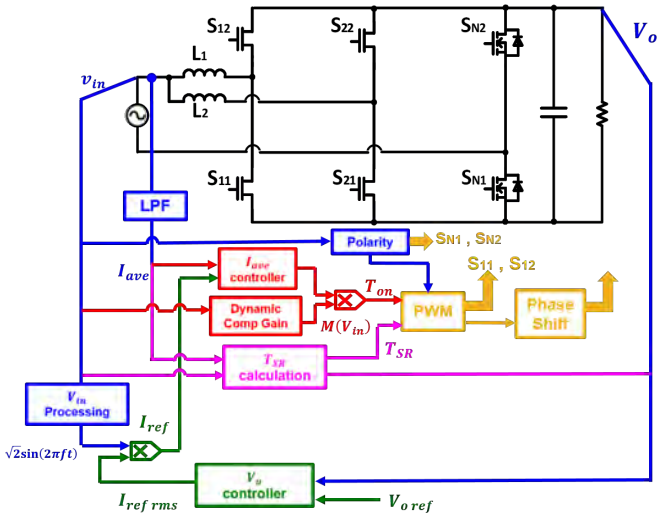


Fig. 2. Microcontroller-based average current mode control with SR on-time calculation in a GaN-based, two-phase interleaved CRM totem-pole CRM PFC.

Design of Integrated Transformer and Inductor for a High-Power High-Frequency Resonant Converter

LLC Resonant Converters are widely used for dc-dc converters. A resonant inductance embedded transformer is a critical component, as it provides the required isolation between the primary and secondary side and takes a large portion of the total volume of the whole converter. This work presents a comprehensive design procedure of a 100 kHz, medium-voltage transformer for a 30 kW Serial Half Bridge Converter with 45 kW overload condition. The design method of a high-power, high-frequency integrated transformer and inductor with perfect current sharing is presented in this work.

The transformer structure is shown in Fig. 1. Fig. 2 presents some cases with different leakage inductance and current-sharing waveforms. The leakage inductance between the winding on the same leg is more important for current sharing. A 13 % difference on the leakage inductance between Lk_pri1sec2 and Lk_pri2sec1 only causes a 2 % current difference, but a 30 % difference between Lk_pri1sec1 and Lk_pri2sec2 causes a 31 % current difference. The structure in Fig. 2(b) can be avoided by using a bobbin, and Fig. 2(c) is not mechanically stable, so both cases can be avoided.

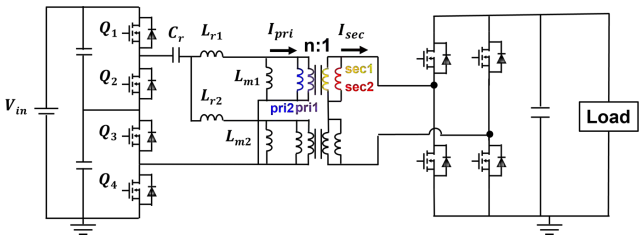


Fig.1. Serial half-bridge topology.

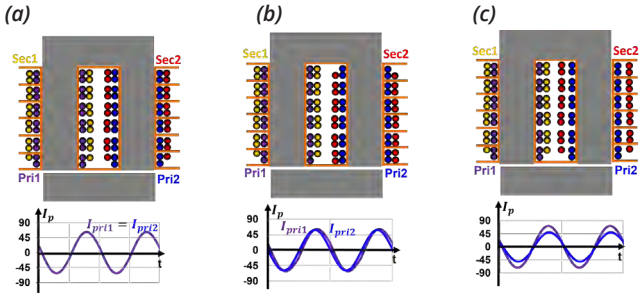


Fig. 2. Current sharing for different winding structures. (a) Normal. (b) Vertical misalignment. (c) Horizontal misalignment.

Fig. 3. Hardware prototype.

Investigation and Solutions for High Termination Losses in Planar Matrix Transformers With Full-Bridge Rectifiers

For high-frequency, high output-current isolated dc-dc applications, LLC resonant converters with PCB-winding-based planar matrix transformers with full-bridge rectifiers have shown superior efficiencies and power densities. However, in such transformers, the secondary-side termination design of the secondary-rectifiers (SRs) and the output filter capacitors is critical to minimize the termination losses. Various SR termination techniques have been studied, with the SR on-winding termination exhibiting the lowest leakage inductance and termination loss.

However, in this termination, the output filter capacitors must be split between the two secondary layers as C_{top} and C_{bot}, respectively, and must be paralleled using vias before connecting to the load. This results in a long paralleling path, which has its own parasitic leakage inductance L_s and resistance R_s, as shown in Fig. 1. Due to parallel resonance between the two parallel capacitor paths, there are high circulating currents at the resonant frequency, which depend on L_s and C_{top}. This results in high current through R_s, resulting in high termination ac resistance at the parallel resonant frequency. Hence, it must be moved to a higher frequency away from the converter-switching frequency to minimize its impact on the converter performance.

To achieve this, additional interleaving vias can be added directly under the capacitors to provide a much shorter path with lower L_s, hence higher parallel resonant frequency. This concept is experimentally verified by comprehensively modeling and measuring the transformer impedances with the different capacitor-paralleling via placements. Moreover, to verify its impact on the converter efficiency, a 2 kW 500 kHz unregulated 112 V/14 V LLC converter is developed, and full-load efficiency improvement of 0.56 % is obtained, as shown in Fig. 2.

Lastly, this work proposes a guideline to design the termination for PCB-winding-based planar matrix transformers with full-bridge rectifiers. The paralleling of the split output-filter capacitors in the SR on-winding termination results in parallel resonance, which could impact the transformer resistance, thus converter efficiency, if not designed properly. The improvement in transformer ac resistance and LLC converter efficiency is demonstrated with the improved termination design.

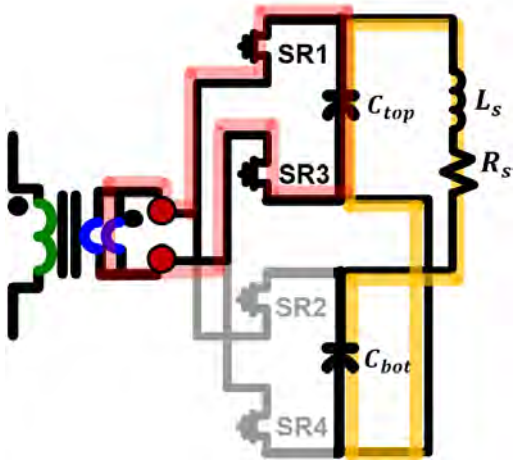


Fig. 1. Circulating current between parallel filter capacitors.

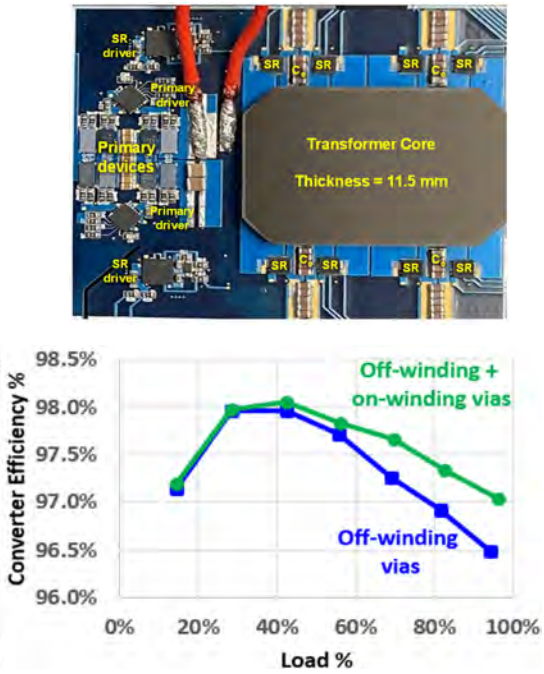


Fig. 2. Test hardware and converter efficiency.

Thermo-Mechanical Analysis of a Custom Package for a (650 V, 150 A) e-GaN HEMT

Gallium nitride (GaN) high electron mobility transistors (HEMTs) show great promise for high-frequency and high-temperature switching operations in power converters. However, to fully utilize their advantages, their packages must be designed to minimize the junction-to-case thermal resistance and parasitic electrical parameters. To achieve minimal package parasitic inductances, an example of previous efforts involved embedding bare transistor dice into printed circuit boards (PCBs). However, this packaging approach suffers from large junction-to-case thermal resistance because of PCB material's low thermal conductivity. It also suffers from low thermo-mechanical reliability because of the large coefficient of thermal expansion mismatch between the GaN device and PCB. To improve the thermal performance and reliability of the embedded packaging, CPES recently developed a PCB-Interposer-on-Direct Bonded Copper (DBC) packaging approach and applied it to packaging GaN System's 650 V, 120 A GaN HEMT die. As shown in Fig. 1, the die is sandwiched between an aluminum nitride (AlN) DBC substrate and a PCB. The DBC substrate provides electrical isolation and heat extraction, while gold-plated pins through the PCB connect the die terminals to the PCB circuit for low parasitic inductances.

To investigate the thermo-mechanical reliability of the PCB-Interposer-on-DBC package, a finite-element analysis tool, ANSYS Mechanical, is used to simulate the temperature-cycling test of the package and finds the stress and strain distributions at the package's interconnects. Shown in Fig. 2 is an FEA model of half of the package undergoing a temperature cycling test between -40 to 125 °C. One focus of the analysis is on the sintered silver joints connecting the PCB to the device. Results of the simulations include the shear and normal stresses at the joints and the volume-averaged strain energy density per thermal loading cycle (VA SED/cycle). The latter is a widely accepted metric for evaluating the reliability or predicting the lifetime of a bonded interconnect.

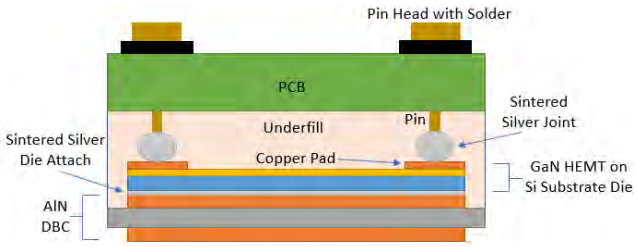


Fig. 1. Side view of the simplified active region of the PCB-Interposer-on-DBC structure.

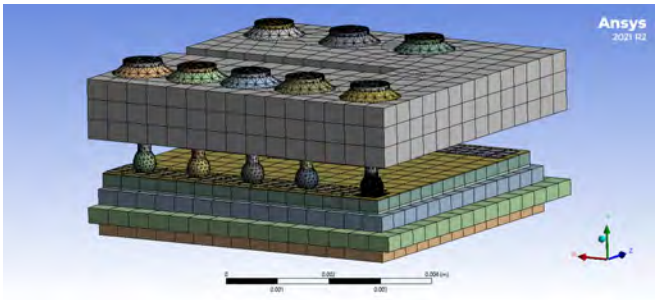


Fig. 2. Half model being simulated with the underfill removed for clarity.

Fast-Transient Control Scheme for 48 V-PoL Four-Phase Series Capacitor Buck Converter

This work presents the transient performance of a four-phase series capacitor buck (SCB) converter with the proposed improved constant on-time (COT) control scheme for a voltage regulator module (VRM) application. The four-phase SCB converter can work in either a four-phase interleaving or two-phase interleaving operation. Unlike a conventional multiphase buck converter, the SCB converter only allows a phase overlap between non-subsequent phases. Due to the phase overlap restriction, it is revealed that the two-phase operation has a better load step-up transient performance, whereas the four-phase operation has a better load step-down transient performance.

In order to achieve a good transient performance at both a load step-up and load step-down transient, a control strategy to use a four-phase operation at steady-state, allowing a phase-overlap between the non-subsequent phase at load step-up transient is proposed. A modification both in the phase manager and clock generator is done to enable a phase overlap between non-subsequent phases at the load step-up transient. With the proposed control scheme, the load step-up transient performance is improved while maintaining a good load step-down transient performance of a four-phase operation.

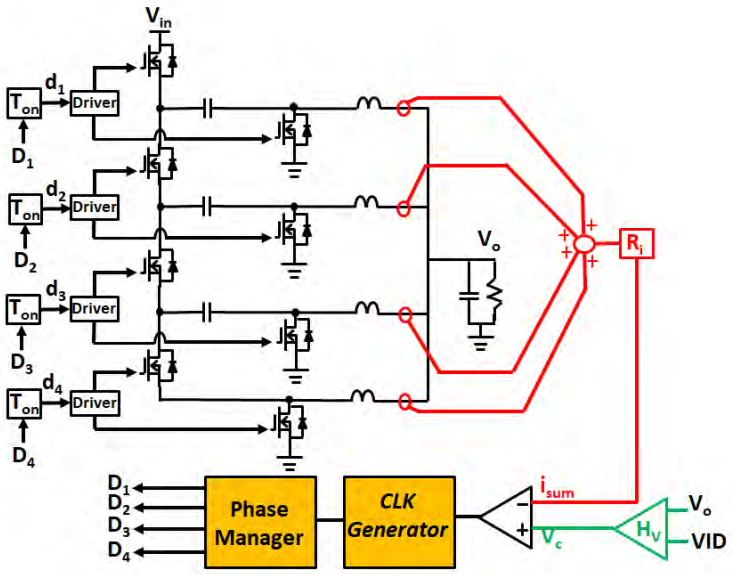


Fig. 1. Four-phase SCB converter with COT control.

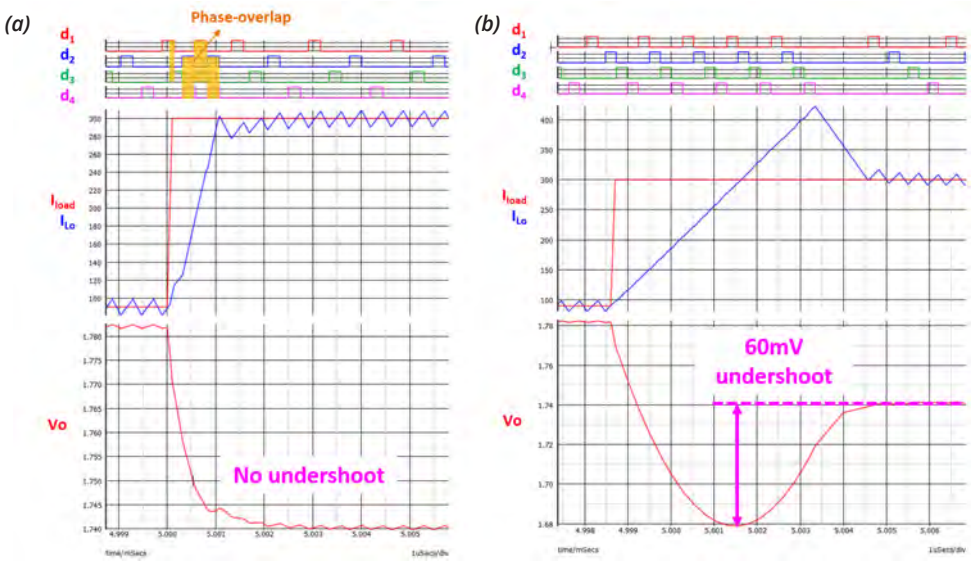


Fig. 2. Load step-up transient simulation results. (a) Four-phase interleaving operation with the proposed control scheme. (b) Conventional four-phase interleaving operation.

Tri-Gate GaN Junction HEMTs: Physics and Performance Space

The gallium nitride transistor (GaN HEMT) has shown great potential in high-efficiency power switches. The most commonly used GaN HEMT applies a planar pGaN as the gate stack. The tri-gate GaN junction HEMT (Tri-JHEMT) combines a 3D fin gate structure and junction gate design (Fig. 1), where preliminary results show that E-mode operation and low on-resistance can be achieved.

This work is a comprehensive study of the device physics and performance space of GaN Tri-JHEMTs, with the aim to probe their potential advantages over the commercial planar p-gate HEMTs at different voltage classes. 3-D TCAD simulation is employed to traverse a large design space for the pGaN-based Tri-JHEMT (e.g., fin width, 2DEG density). The simulation models are calibrated with the experimental characteristics of the fabricated p-NiO-based Tri-JHEMTs. The experimental characterizations also demonstrated the first kilovolt blocking capabilities at high temperatures (150 °C) in a GaN trigate HEMT. These high-temperature characteristics show the true variability of Tri-JHEMTs for industrial applications.

The pGaN-based Tri-JHEMT is simulated with a calibrated model from NiO Tri-JHEMT experimental results. As compared with the planar pGaN gate HEMT, the pGaN Tri-JHEMT allows E-mode with the highest wafer 2DEG concentration and lowest sheet resistance. As a result of its strong gate control capability, the Tri-JHEMT can reduce the fin length to ~100 nm level to reduce gate resistance. As compared with the Tri-MISHEMT, the junction depletion region of the Tri-JHEMT removes the parasitic capacitance and minimizes unnecessary gate charges. As shown in Fig. 2, there is more than a 40 % decrease in R_{on}, $R_{on}Q_G$, and $R_{on}Q_{oss}$ is achieved for the Tri-JHEMT at 600 V rating, as compared with the same gate length planar HEMT. By reducing the fin length to a 100 nm level, more than a 50 % decrease in the above parameters can be obtained for the 15 V rating.

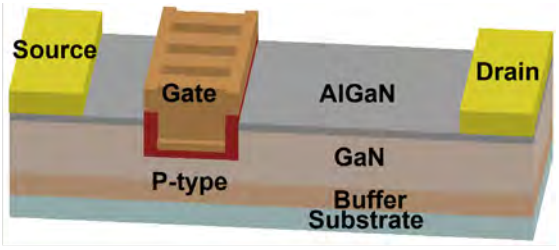


Fig. 1. Device diagram of Tri-gate GaN junction HEMT.

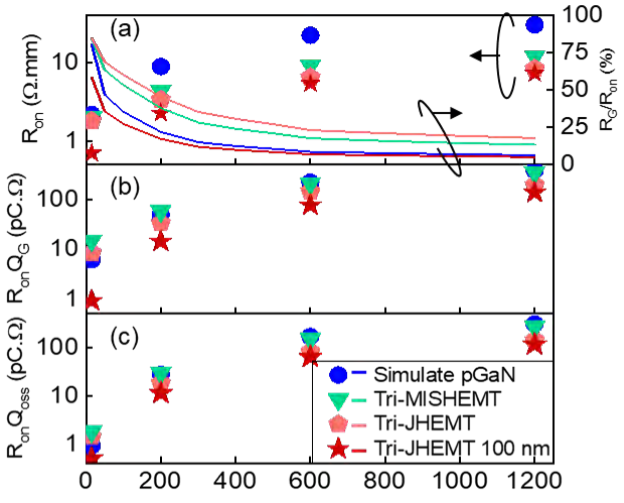


Fig. 2. (a) R_{on}, (b) $R_{on}Q_g$, and (c) $R_{on}Q_{oss}$ comparison for Tri-gate junction HEMT, Tri-gate MISHEMT, and planar pGaN HEMT.

Overvoltage Ruggedness and Dynamic Breakdown Voltage of P-Gate GaN HEMTs in High-Frequency Switching up to Megahertz

In this work, we designed and prototyped a novel overvoltage testbed based on a soft-switch buck converter, in which an air-core inductor produces transient overvoltage on the device under test (DUT) during its hard turn-OFF, and an active clamping circuit (ACC) subsequently clamps the inductor's surge energy and regulates the test waveforms. This testbed allows continuous kilovolt overvoltage switching up to 1 MHz with a peak dv/dt > 100 V/ns. Two types of commercially available 600/650 V p-gate GaN HEMTs were tested, namely a Hybrid-Drain Gate Injection Transistor (HD-GIT) and a Schottky-type P-gate GaN HEMT (SP-HEMT).

Fig. 1(a) & (b) show the test circuit and the test setup. Fig. 1(c) & (d) illustrates the working principle of the ACC via the LTspice simulation at a 400 V input voltage (V_{in}), 1 MHz F_{SW} and 0.5 duty cycle.The ACC works at the same F_{SW} as the converter. In each switching cycle, ACC turns ON at the end of the first V_{DS} overshoot, transferring the surge energy to the ACC loop and regulating the overvoltage waveform to contain only one high V_{DS} overshoot pulse. It turns OFF before the top switch turns ON. The energy stored in L_{air} is fully dissipated via the clamping circuit in each cycle, and a stable peak V_{DS} can be achieved.

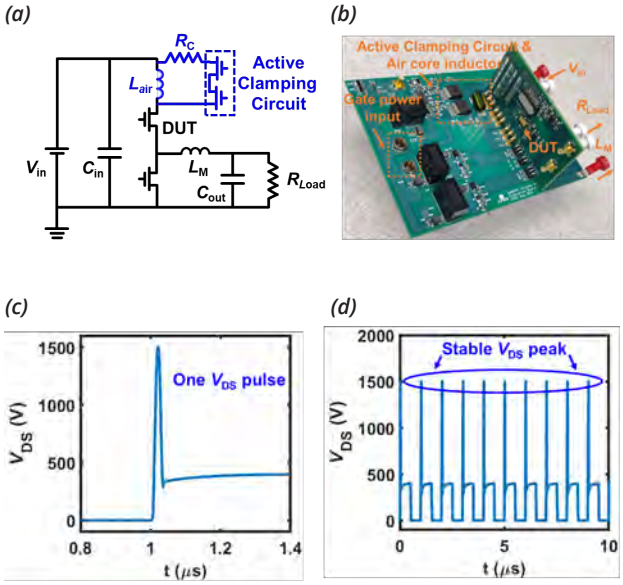
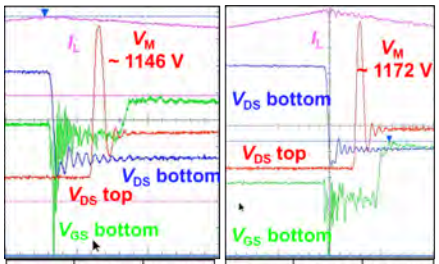


Fig. 1. (a) & (b) Test circuit schematic and setup. (c) & (d) Simulated waveforms with ACC activated.

Fig. 2 summarizes the testing results. While the HD-GIT shows a nearly F_{SW}-independent dynamic BV, the SP-HEMT shows a decreasing dynamic BV at higher F_{SW}, e.g., 270 V lower when F_{SW} increases from 2 kHz to 1 MHz. The change of BV with F_{SW} can be explained by the time-dependent electron trapping and the impacted dynamic BV of GaN HEMTs. In HD-GIT, an additional p-GaN is electrically connected to the drain metal, holes are injected from the drain under high V_{DS}, which neutralize the acceptor traps in the GaN buffer and alleviate the peak E-field at the drain side. On the contrary, in SP-HEMT the filling of acceptor traps in the GaN buffer results in a dynamic BV lower in higher F_{SW} test.

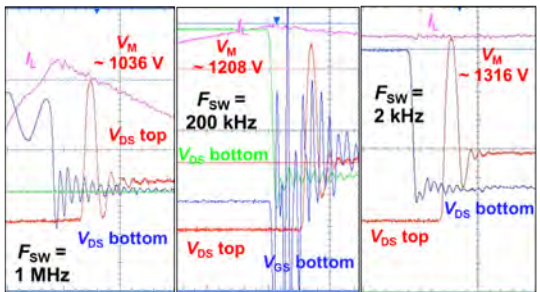
(a)



F_{SW}	DUT	V_M (V)
200 kHz	1	1146
	2	1171
	3	1163

F_{SW}	DUT	V_M (V)
1 MHz	1	1172
	2	1156
	3	1127

(b)



F_{SW}	DUT	V_M (V)
1 MHz	1	1036
	2	1060
	3	1040

F_{SW}	DUT	V_M (V)
200 kHz	1	1196
	2	1208
	3	1204

F_{SW}	DUT	V_M (V)
2 kHz	1	1316
	2	1316
	3	1324

Fig. 2. Summary of tested BV of (a) HD-GIT and (b) SP-HEMT.

Evaluation of 650 V,100 A Direct-Drive GaN Power Switch for Electric Vehicle Powertrain Applications

This work presents the evaluation of a 650 V, 100 A, 22 mΩ-rated D³GaN (Direct Drive Depletion-mode) power switch (V22TC65S1A) from VisIC Technologies, which is designed for electric vehicle (EV) powertrain inverter applications (Fig. 1). The static and dynamic performance, as well as the surge-energy and short-circuit robustness of the D³GaN, are evaluated in a top-cooled, surface-mount device package. Multiple customized test boards are employed to evaluate the switching loss, dynamic on-resistance, gate charge (Q_g), and robustness. The D³GaN switch shows a small total Q_g, high breakdown voltage, positive threshold voltage, small switching-energy loss, fast switching speed, and good robustness. These advantages make the D³GaN switch an attractive candidate for high-power EV powertrain inverter applications. Reportedly, this work presents the first comprehensive evaluation of a high-power GaN device targeted for EV inverter applications.

TABLE I provides a comparison of key parameters between the VisIC D³GaN tested in this work and its counterparts. The D³GaN device shows a higher V_{th}, a smaller Q_g, lower device capacitance, and a faster switching speed, as compared to the cascode GaN HEMT and SiC MOSFET. Also, it exhibits good surge-energy/short-circuit robustness, which indicates the D³GaN is an attractive candidate for high-power EV powertrain inverters and other power applications.

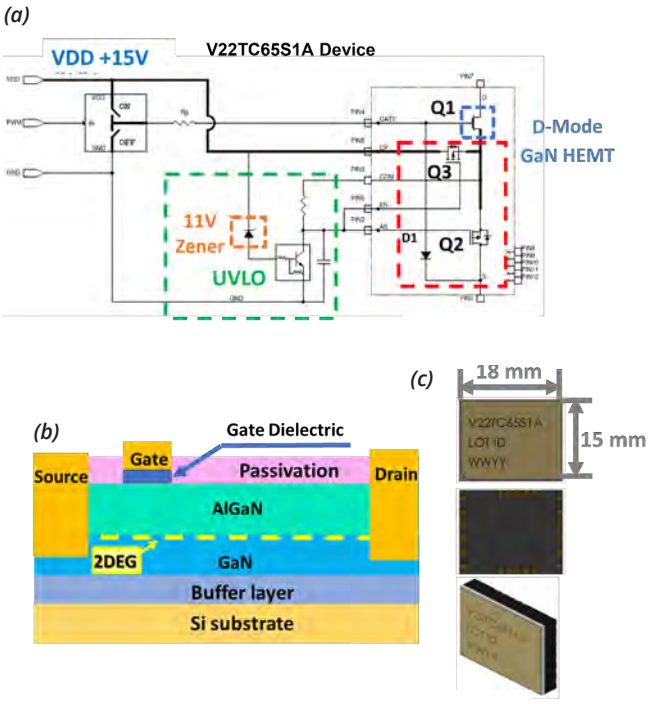


Fig.1. (a) Schematic of the D³GaN device. (b) Structure of the D-mode GaN HEMT. (c) Top-cooled SMT package with AlN ceramic substrate.

TABLE I

		VisIC V22TC65S1A		Transphorm TP65H015G5WS		Cree Wolfspeed C3M0025065K	
Symbol	**Parameter**	**Value**	**Test Conditions**	**Value**	**Test Conditions**	**Value**	**Test Conditions**
V_{DSS}	Drain to source voltage	650 V	V_{GS} = -15 V, I_D = 1mA	650 V	V_{GS} = 0 V	650 V	V_{GS} = 0 V, I_D = 100 µA
I_{DS}	Continuous drain current	100 A	T_c = 25 °C	95 A	T_c = 25 °C	97 A	T_c = 25 °C
$R_{DS\ (on)}$	Static on-resistance	22 mΩ	V_{GS} = 15 V, I_D = 35A, T_c = 25 °C	18 mΩ	V_{GS} = 10 V, I_D = 35A, T_c = 25 °C	25 mΩ	V_{GS} = 15 V, I_D = 33.5A, T_c = 25 °C
V_{th}	Gate threshold voltage	6.8 V	I_D = 1 mA, V_{DS} = 0.1 V	4 V	I_D = 2 mA, V_{DS} = V_{GS}	2.3 V	I_D = 9.22 mA, V_{DS} = V_{GS}
I_{DSS}	Drain source leakage current	20 µA (1)	V_{DS} = 650 V, V_{GS} = 0 V	7 µA	V_{DS} = 650 V, V_{GS} = 0 V	1 µA	V_{DS} = 650 V, V_{GS} = 0 V
I_{GSS}	GaN gate leakage current	9.5 nA	V_{DS} = 400 V, V_{GS} = -15 V	≤ 400 nA	V_{GS} = 20 V	10 nA	V_{DS} = 0 V, V_{GS} = 15 V
Q_G	Total gate charge	54 nC	V_{DS} =400V, V_{GS} = 0 V to 10 V, I_D= 60 A	68 nC	V_{DS} =400V, V_{GS} = 0 V to 10 V, I_D= 60 A	112 nC	V_{DS} =400V, V_{GS} = -4 V to 15 V, I_D= 33.5 A
C_{ISS}	Input capacitance	760 pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	5218 pF	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	2980 pF	V_{DS} = 600 V, V_{GS} = 0 V, f = 1 MHz
C_{OSS}	Output capacitance	212 pF		307 pF		178 pF	
C_{RSS}	Output capacitance	26 pF		26 pF		12 pF	
$T_{D\ (ON)}$	Turn-on delay	11 ns	V_{DS} = 400 V, R_G = 15 Ω, I_D = 60 A	78 ns	V_{DS} = 400 V, R_G = 15 Ω, I_D = 60 A	12 ns	V_{DS} = 400 V, $R_{G(ext)}$ = 2.5 Ω, I_D = 33.5 A
T_R	Rise time	10.92 ns		20 ns		18 ns	
$T_{D\ (OFF)}$	Turn-off delay	19.8 ns		132 ns		25 ns	
T_F	Fall time	3.81 ns		32 ns		8 ns	
E_{Surge}	Maximum UIS surge energy	0.77 mJ	$V_{DS(Peak)}$ = 1800 V	N/A	N/A	N/A	N/A
E_{Short}	Maximum short circuit energy	0.72 mJ	V_{DS} = 400 V, t_{short} = 5 µS (with built-in protection)	N/A	N/A	N/A	N/A

TABLE I
Summary of the key parameters of D³GaN Device, a similar rated commercial cascode GaN HEMT from Transphorm, and a similar rated commercial SiC MNMOSFET from Cree Wolfspeed.

Wide-Bandgap High-Power Converters & Systems (WBG-HPCS) Nuggets

Modeling and Control of Modular Multilevel Converter

In a Modular Multilevel Converter (MMC), a large capacitor bank is usually required to store line-frequency and its harmonics-related circulating energy. Even though several methods are proposed in literature to minimize the circulating energy, there is still no effective modeling tool that enables a more systemic approach to address the control strategies. In general, the nature of the circulating energy is rather ambiguous.

Recently, Dr. Hsieh (graduate of CPES) proposed a decoupled equivalent circuit model of an MMC, shown in Fig. 1, based on state trajectory analysis and coordinate transformation. This model clearly demonstrates the nature of circulating energy. Specifically, there are two orthogonal circulating energies flowing into the MMC: one is related to capacitor voltage v_Σ that represents energy exchanging between modules and input/output while the other circulating energy is related to v_Δ that represents energy merely swapping between the upper and lower arm. Due to the orthogonal nature of these two circulating energies, the capacitor voltages, v_Σ (dc,2ω,..) and v_Δ (ω,3ω,..) are decoupled from each other based on the frequency. Due to this decoupling nature, circulating energies can be easily controlled. From the circuit model, the following two "ideal" control laws, $d_{in}\, i_{in}=d_o\, i_o$ and $2d_o i_{in}=0.5d_{in}i_o$, can be established to make the circulating energy related to v_Σ and v_Δ zero, respectively.

The other control objectives in a grid-tied MMC are output current regulation and the capacitor's dc voltage regulation. Conventionally (in literature), to achieve the capacitor's dc voltage regulation, the generally accepted control is implemented in an indirect manner; instead of directly controlling the upper and lower arm capacitor voltages, the sum and difference of the upper and lower arm capacitor voltages are regulated. However, since the sum and difference of capacitor voltages do not physically exist in the original circuit of an MMC, the control implementation lacks in the physical interpretation. However, in the proposed circuit model, v_Σ (dc) and v_Δ (dc) can be directly regulated without affecting each other, owing to their decoupling nature. They can be regulated by controlling i_{in} through d_{in}, as shown in Fig. 1. Similarly, i_o current can be directly controlled through d_o.

Thus, the control of the MMC becomes evident under the proposed decoupled equivalent circuit model.

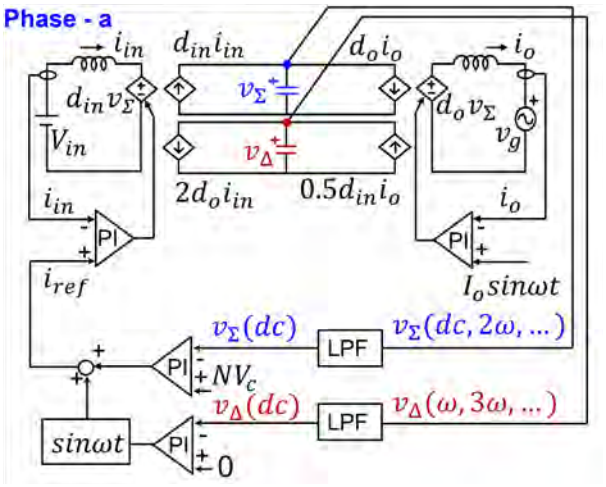


Fig. 1. Proposed decoupled equivalent circuit model and its basic control implementation.

Modeling of Power Electronic Systems With Harmonic State Space Modeling With Focus on Pulse Width Modulation

With the growing integration of power converters within the modern power grid, there is a recent challenge to observe how these distinct power converters interact among themselves. There have been several recent attempts to fill this research gap but most efforts in this area are either concentrated on the low-frequency harmonics arising from the Phase Locked Loop or in the high-frequency EMI region. Very little has been reported in the domain of switching harmonic interactions, and this work aims to bridge that gap.

This research work models the complex converter interactions using a harmonic domain modeling method: Harmonic State Space (HSS). The HSS simulation environment is further enhanced by the development of a fundamentally new pulse width modulator model based on multi-tone Bessel functions. The incorporation of the new modulator model paves the way for HSS to be about four times faster than the conventional time domain modeling method and much more accurate than conventional averaging models. To verify the proposed approach, a two-converter model (as shown in Fig. 1) is considered. Inverter A regulates the voltage across the ac link, whereas inverter B is designed to regulate the current at the ac link. The performance of the proposed modeling methods in comparison to its equivalent time domain counterparts is analyzed in MATLAB. This is presented in Fig. 2.

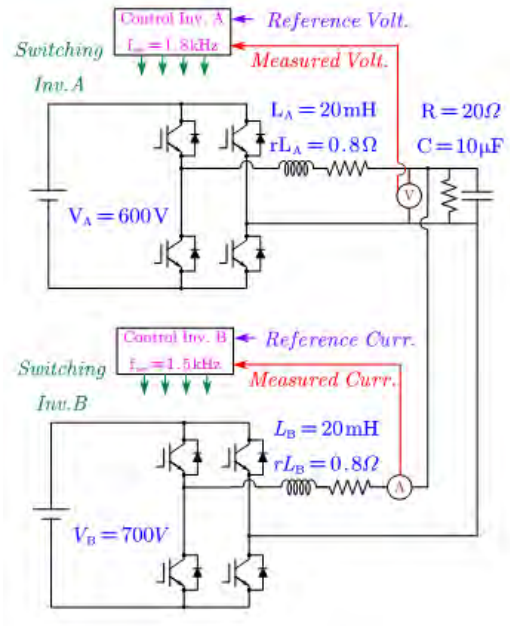


Fig. 1. Two-converter system under observation.

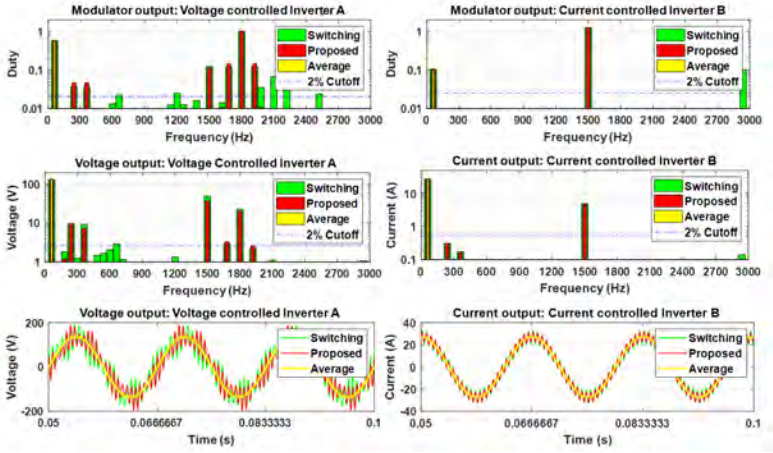


Fig. 2. Comparison of converter modeling results.

Modified Switching Cycle Control for Modular Multilevel Converters

Modular Multilevel Converters (MMC) have gained a great amount of traction in recent years due to their scalability and modularity. While extensively utilized for high-voltage applications, the MMCs have a major challenge in terms of the passive component sizing, in particular, capacitor sizing. This stems from their reliance on line frequency operation, hence restricting their utilization in power-dense operating situations, such as wind energy generation or ships.

Switching Cycle Control (SCC) has been proposed earlier, which transforms the line frequency operation of MMCs to switching frequency operation, greatly improving the power density of converter. To implement SCC, the converter must pass through several operating regions with different phase shift (PS), as shown in Fig. 1. This change in PS is necessary to maintain converter regulation. To demonstrate the idea, consider a two module per arm MMC, as shown in Fig. 2, and the results for the two operating modes shown in Fig. 3. Conventionally the transition has been abrupt, as shown in Fig. 1(a). This can lead to transients at transition points, as visible in Fig. 3(a) and Fig. 3(c). On the contrary, this work proposes a variable PS transition, as shown in Fig. 1(b). As observed from Fig. 3(b) and Fig. 3(d), the transient behavior can be eliminated.

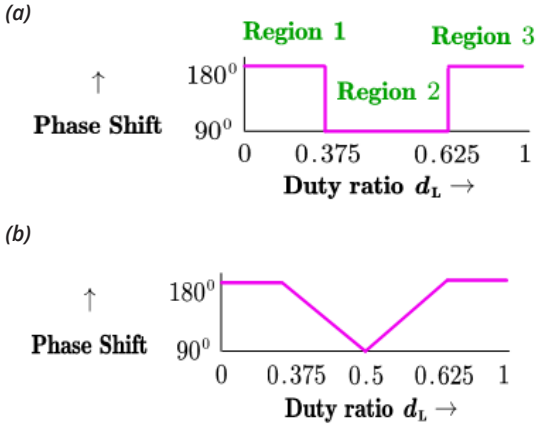


Fig. 1. Operating mode for two modules per arm MMC operating under SCC.

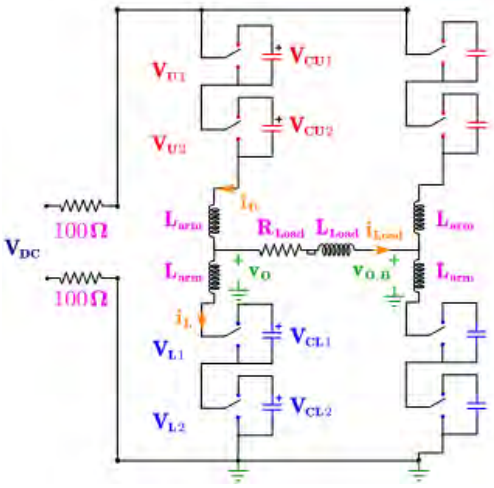


Fig. 2. Two modules per arm MMC setup.

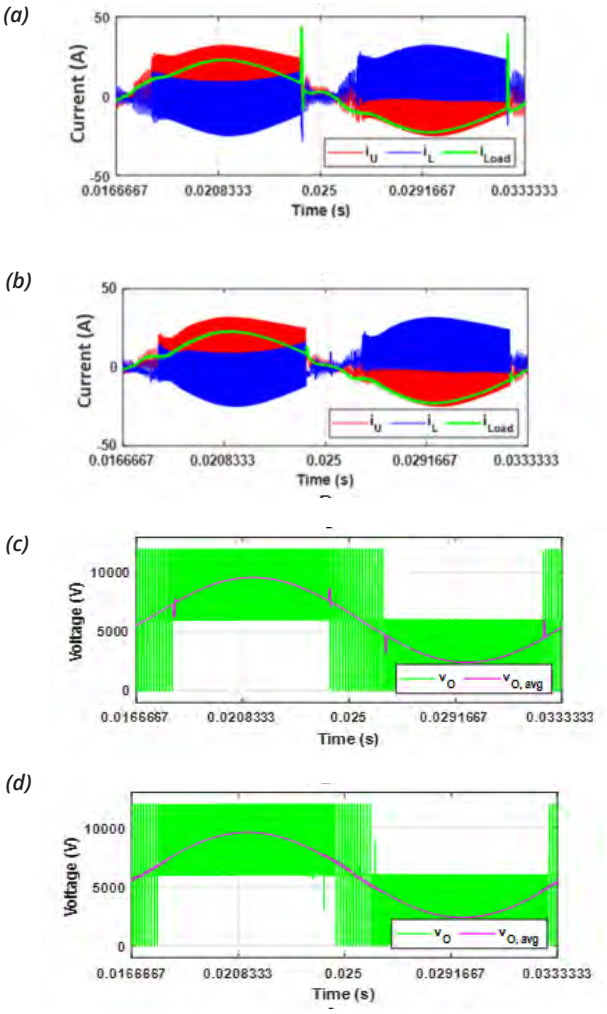


Fig. 3. Results for SCC dc-ac operation. (a) Conventional SCC currents. (b) Proposed SCC currents. (c) Conventional SCC Voltages. (d) Proposed SCC Voltage.

Gate Driver Switching Noise Propagation Study for Medium-Voltage SiC-Based Power Electronics Building Blocks

The emergence of the SiC MOSFET facilitates the development of power electronics; nevertheless, it gives rise to challenges, including electromagnetic interference (EMI), due to its fast dv/dt transient. The gate drivers that are used in power electronics building blocks (PEBBs) have complicated designs and can achieve comprehensive functionalities. However, the fast dv/dt rate during the switching transient generates switching noise. This can corrupt the critical signals on the gate driver PCB, in particular the high side gate driver, thus potentially causing false triggering issues and system malfunction.

This work aims to investigate the switching noise propagation on the gate driver PCB under fast dv/dt. First, the dv/dt generated by the power stage induces common-mode (CM) current flowing on the ground layers of the PCB due to the isolation barriers among different PCB grounds as shown in Fig. 1(a). Then, the CM noise flowing on the ground layers is coupled to the signal traces on other layers, which connect between different ICs. The noise at the IC that receives the signal matters; if it exceeds the threshold value of that IC, false triggering will happen.

In this work, an existing gate driver design for a 10 kV power module is used to study how the switching noise is propagated on the gate driver PCB. The study starts with selecting several critical signal traces. FEA simulation is done to find the parasitics of the ground layer and traces, as well as the mutual inductances between them. Experiments are done to comparatively verify the proposed models. It is proved that the noise at the signal receiving IC is strongly related to the trace location, orientation, length, and shape.

This work was supported by the Office of Naval Research (ONR), with grant number N00014-16-1-2956. DCN: 43-9069-22.

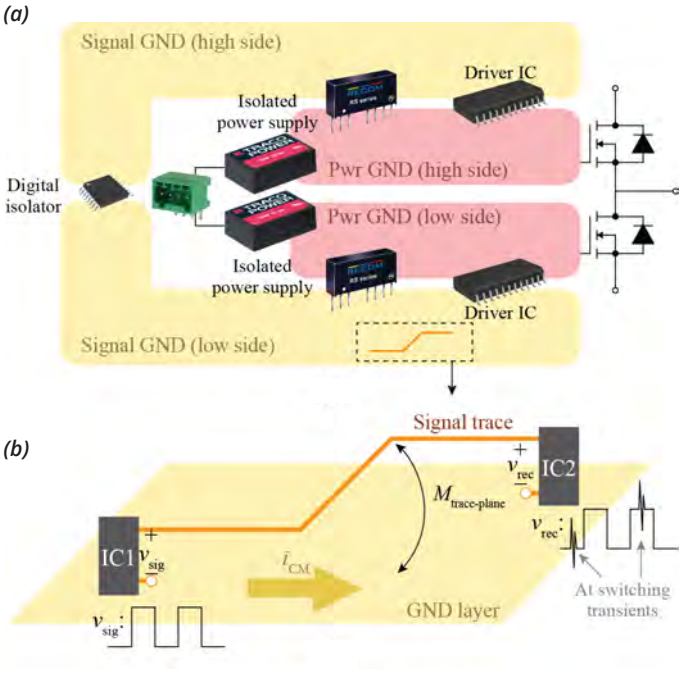


Fig. 1. Gate driver switching noise propagation models. (a) Exemplary CM noise propagation diagram showing different PCB grounds and isolation barriers. (b) Signal trace – ground plane model showing how the received signal is corrupted.

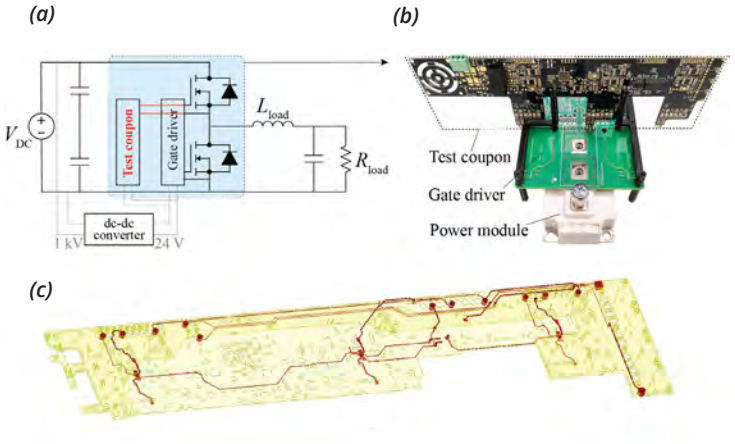


Fig. 2. Test setup and FEA simulation overview. (a) Test schematic. (b) Image of power module, gate driver, and test coupon. (c) 3D FEA simulation with selected critical traces.

Reduced Order Modeling of Power Converters for System-Level Studies

To support large-scale, system-level simulations of distributed point-of-load, three-terminal dc and ac power converters, it is desirable to develop reduced-order models for improved computational efficiency when higher order response is not a quantity of interest. For a notional 250 kW dc-dc buck converter having switching and current loop bandwidths of 10 kHz and 1 kHz, respectively, it is postulated the current loop bandwidth may be treated as infinite, and a reduced-order model is developed. The order of this simplified model is reduced by not only the order of the omitted current loop controller, but also by a simplification of removing the contribution of the output inductor from the model, leading to an ultimate reduction of at least two orders, or more likely three or more.

The challenge lies in analyzing the source-load impedance interactions. If a power converter's higher-order source impedance transfer function curve contains salient points not represented in the reduced-order model, there may be cases where the source-load impedance interaction appears stable for a reduced-order model but is revealed to be unstable by a higher-order average-value model. This may appear in the form of an insufficient phase margin where the Bode gain plots intersect and in the form of Nyquist encirclements of the -1 point. It is desirable to determine if a correction can be included in the simplified model.

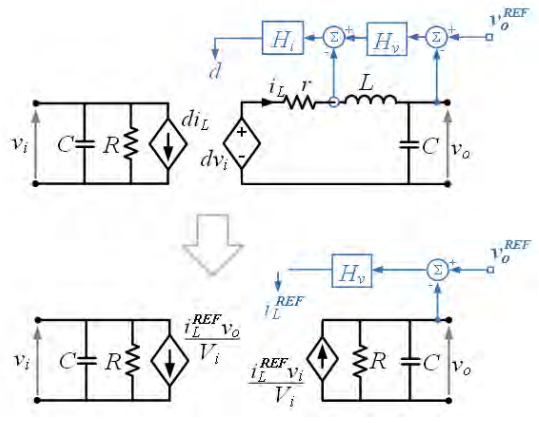


Fig. 1. Simplified model assumes infinite-bandwidth current control.

The simplified model of the characteristic 250 kW dc-dc buck converter is loaded with an identically structured converter representing a constant-power load of 15-30 kW. The source and load transfer functions are then extracted and manipulated to compare load-source impedance interactions for average versus simplified converter models. This is done with a focus on the impact of any salient points in the gain and phase curves, which are evident for the higher-order average model, but not for the lower-order simplified model.

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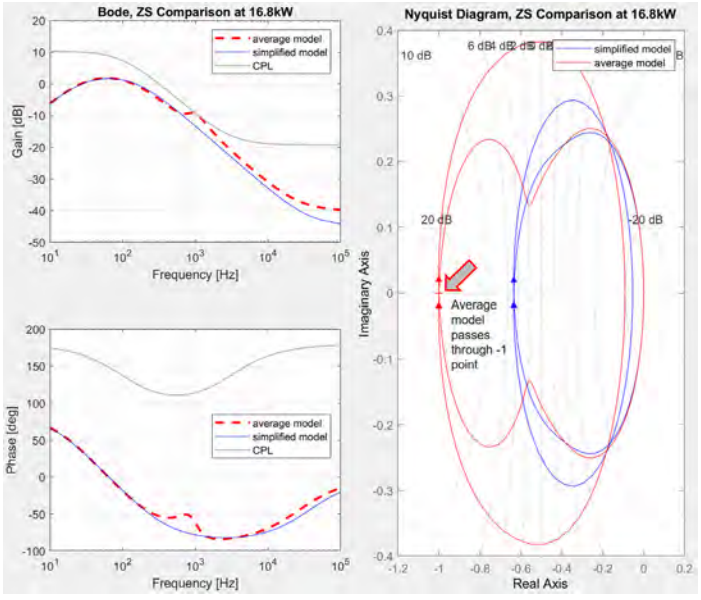

Fig. 2. Average model unstable while simplified model yet stable.

Experimental Verification of a Converter Having Integrated Capacitor Blocked Transistor Cells Using 10 kV SiC MOSFETs

Converters having Integrated Capacitor Blocked Transistor (ICBT) cells provide a new method of transferring high power in medium-voltage or high-voltage systems. ICBT-based converters have modularity and scalability similar to Modular Multilevel Converters (MMCs) but have much lower cell capacitor voltage ripples.

A medium-voltage modular converter was built to verify the ICBT operation, as shown in Fig. 1. There are 12 power cells in total. Three cells are connected in series vertically to form a converter arm, and two arms form a phase leg. The converter has two phase legs sharing the same converter dc bus, which sits on the top. The cells are rated at 6 kV and feature a 10 kV SiC MOSFETs. The cell capacitance is 32.5 μF. A high-voltage, low-current power supply connects to the converter dc bus; an inductor is connected between the outputs of the two phase legs. The rated load current flows through the load inductor, while the power supply only supplies the losses of the converter.

To ensure the cell capacitor voltage balance, a capacitor voltage control is proposed and implemented. The voltage difference is changed by applying delays to the gate signals of some of the cells, depending on the measured cell capacitor voltages and phase leg output current polarity.

Fig. 2 shows the experimental results at 12 kV dc bus voltage and 25 Arms output current. Three subfigures show the three cell capacitor voltages: in the upper arm of phase leg A, the three cell capacitor voltages in the lower arm of phase leg A, and the output current of phase leg A. Each cell capacitor voltage is around 4.0 kV, one-third of the dc bus voltage. The maximum peak-to-peak voltage ripple in a cell is around 34 V, which is 0.85 % of the rated voltage, verifying the low cell capacitor voltage ripple feature of the ICBT operation. The maximum instant voltage difference in an arm is around 28 V, which is 0.70 % of the rated voltage, verifying the effectiveness of the balancing control.

Fig. 1. Converter setup with three cells per arm.

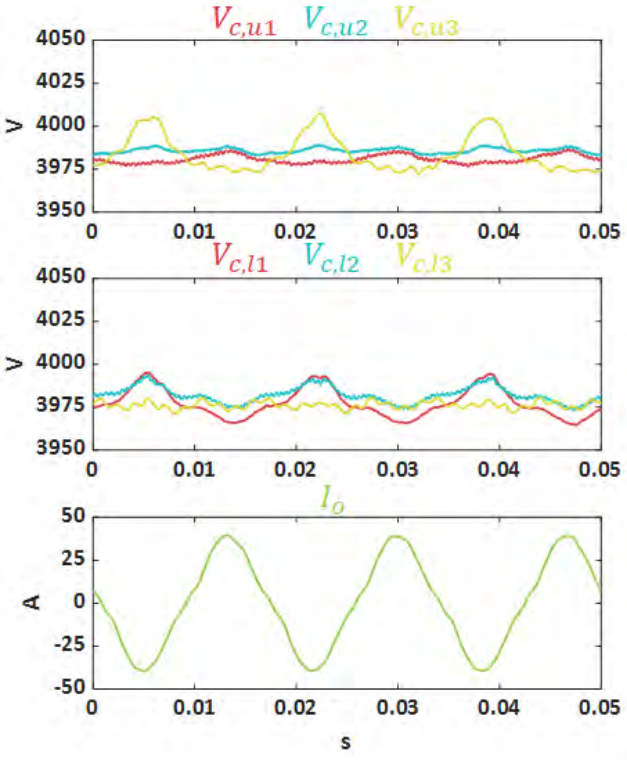

Fig. 2. Experimental results at 12 kV dc bus voltage and 25 Arms output current.

Design of a 24 kV PCB-Based DC Bus

In this work, an electric-field-constrained design of a 22 kV PCB-based dc bus is completed. A PCB-based dc bus allows high customization for high-density power electronics converters and minimizes parasitic inductance through deliberate design. To realize this goal, critical regions for high electric field intensity areas are defined within the board. Several steps are taken to mitigate the identified peak electric fields: increasing distance between layers and staggering conducting layers. An example of these techniques is illustrated in Fig. 1, where a cross-sectional view of a PCB that includes multiple layers at different potentials close to a through-hole via is shown. At increasing potentials, the x and y distances are increased to meet the critical peak electric field intensity requirements. Fig. 2 verifies this stack-up through finite element analysis (FEA); the white area is the peak field intensity value above the maximum allowable intensity in air. The final design of the PCB provides connections for a 22 kV-rated flying capacitor inverter phase leg, while maintaining internal electric fields below the dielectric strength of the insulating material and surface electric fields below the breakdown strength of air. This design hosts multiple buses for the flying capacitor banks within one PCB, thus providing a high-density structure that can be modular. To further expand on the modularity of each phase leg, auxiliary circuit power distribution is also integrated into the PCB. Additionally, layout selection is considered to minimize total loop inductance while minimizing volume.

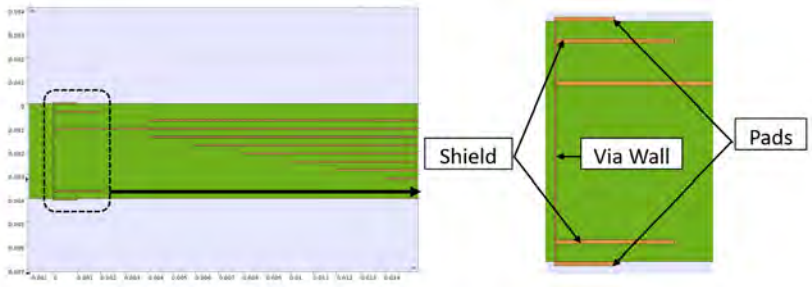

Fig. 1. Cross-sectional view of a PCB with a high-voltage layer stack-up.

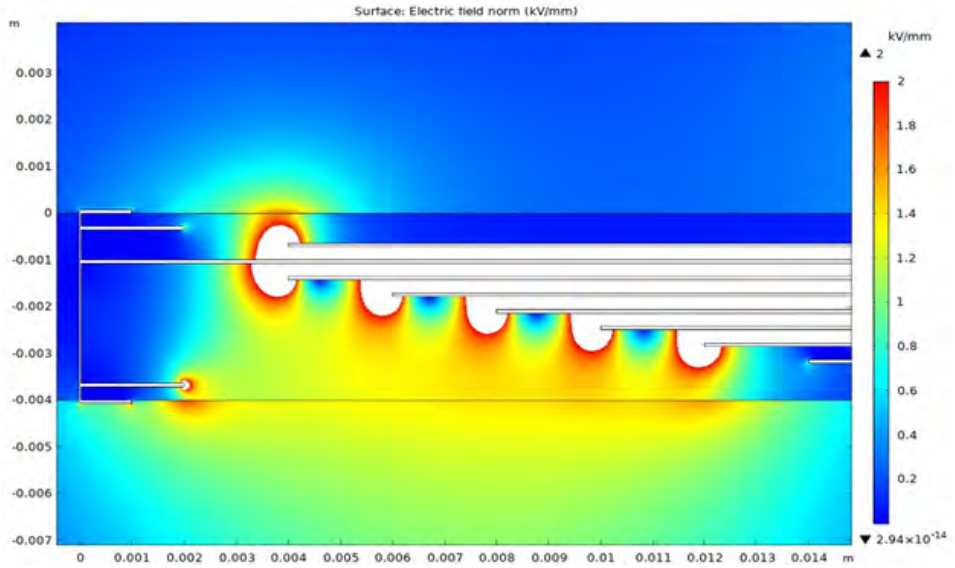

Fig. 2. Verification of high-voltage PCB design through FEA simulations.

PESNet 3.0 for Large-Scale SiC Modular Power Converters: A White-Rabbit-Based Communication Network With Sub-ns Synchronization Accuracy

Emerging large-scale modular power converters are pursuing high-performance distributed control systems (DCSs) that feature minimal synchronization accuracy, high data rate, and advanced control schemes. The power electronics system network (PESNet) 3.0 is a next-generation communication network designed and optimized for such DCSs. As an accompaniment to the growing availability of medium-voltage, wide-bandgap devices, fast-switching-enabled novel control schemes raise the high synchronization accuracy requirements for the PESNet 3.0. The PESNet 3.0 contains an inter-cell layer and an inside-cell layer. Sub-nanosecond (sub-ns) synchronization accuracy is achieved among all controller units.

White Rabbit technology (originally developed for the Large Hadron Collider accelerator chain at the European Organization for Nuclear Research), is embedded in the PESNet 3.0 inter-cell layer, achieving sub-ns synchronization accuracy for distributed power conversion systems for the first time. The PESNet 3.0 inter-cell layer contains the main controller and cell controllers. They share the same hardware, using the high-end Xilinx 7000 as the control device, and communicate in a tree topology with a 5 Gbps data rate. Sub-ns synchronization accuracy is achieved by utilizing a PLL on the controllers to lock both the frequency and phase of the local time with each other.

In order to verify the PESNet 3.0 inter-cell layer synchronization performance, a communication network is built, as shown in Fig.1 (a). A local time counter is generated based on each controller's own clock. A square wave based on the local time counter is utilized to measure the synchronization accuracy, as shown in Fig. 1(b). The channel-to-channel delay measurement data is further extracted from the oscilloscope, as shown in Fig. 1(c). Setting the main controller as the benchmark, all of the measurement data for the 16 cell controllers are within ±0.5 ns, which verifies the sub-ns synchronization accuracy.

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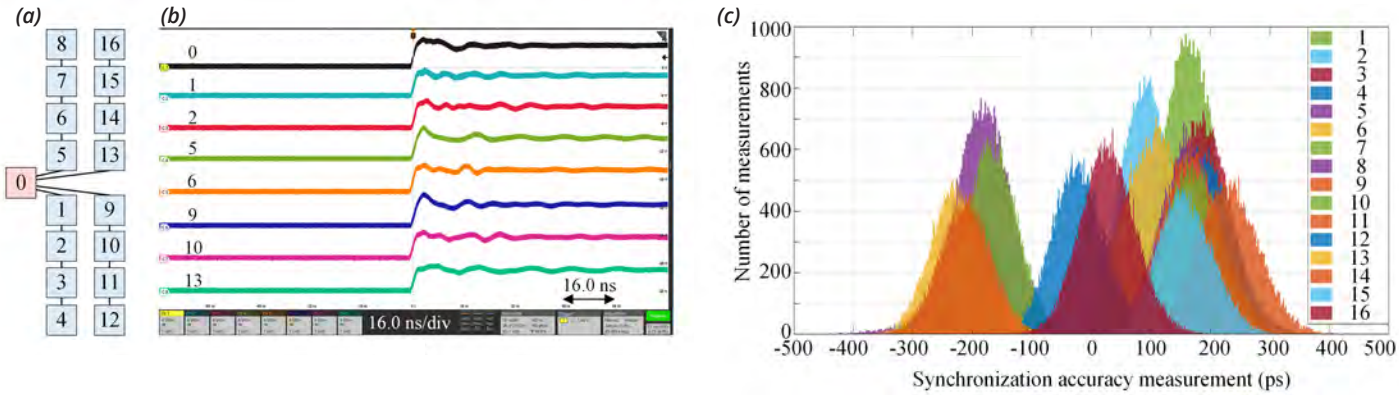

Fig. 1(a). PESNet 3.0 inter-cell layer with 17 controllers in a tree topology. Controller 0 is the main controller; Controllers 1 to 16 are the cell controllers. (b) Synchronization test wave-form of the main controller and 7 cell controllers obtained by an 8-channel oscilloscope. This test is repeated with the other 9 cell controllers. (c) Synchronization accuracy distribution referred to the benchmark main controller for all 16 cell controllers.

Design and Analysis of a 24 kV PCB-Bus for the Low Impedance Interconnect of a Multiphase PEBB-Based Converter

Medium-voltage (MV) SiC MOSFETs, such as Wolfspeed's 10 kV SiC MOSFET module, offer the ability to build megawatt level power electronics building blocks (PEBBs). A 24 kV PCB-bus motherboard is designed to serve as a low impedance interconnect between two phase legs of a 24 kV 2 MW PEBB-based converter. In order to achieve a partial discharge inception voltage (PDIV) >24 kV, internal copper layers are staggered with an offset to introduce a field grading that reduces the peak E-field intensity between layers. As the electric strength of FR4 is higher than the surrounding air, it is desirable to contain the highest fields inside of the PCB. In this work, "shield pads" are introduced to further reduce the peak E-field intensity in air. Shield pads are pads within the PCB dielectric that are the same shape, but slightly oversized, and connect to the same potential as pads directly above them on the surface of the PCB.

Custom 9 μF 3 kV capacitor daughtercards with integrated balancing resistors are designed using a series-parallel network of Commercial off-the-Shelf (COTS) film capacitors. These daughtercards mount directly to the motherboard to build a 1.13 μF 24 kV capacitor bank.

The motherboard PDIV is tested on a layer-to-layer basis and as a full assembly to ensure the system is PD-free under 24 kV operation. Fig. 1 shows the motherboard with daughtercards mounted. Here, the air insulation between the motherboard and daughtercards are tested by observing both PDIV and flashover voltage. Fig. 2 is the full bus assembly, including the container system and frame used to attach it to the converter.

This work demonstrates a 24 kV dc bus motherboard with 3 kV capacitor daughtercards serving as the low impedance interconnect of a 2 MW PEBB-based multiphase converter. The full paper details the design and analysis of the dc bus with shield pads, capacitor daughtercards, and the front end of the bus container, which is used to connect the external MVDC supply.

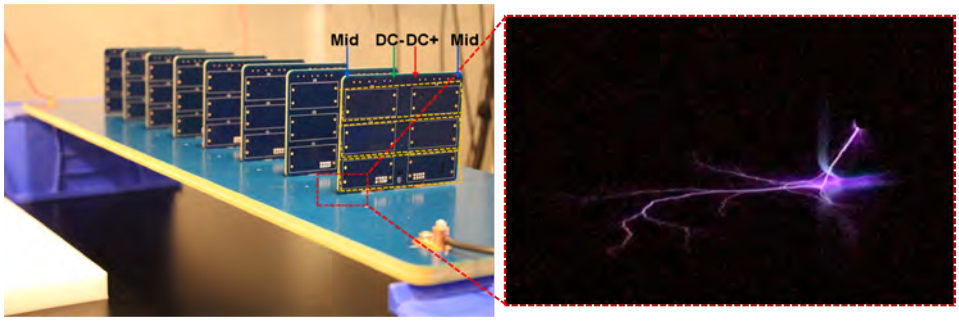

Fig. 1. Insulation test of 24 kV bus with capacitor daughtercards. Flashover >27 kV.

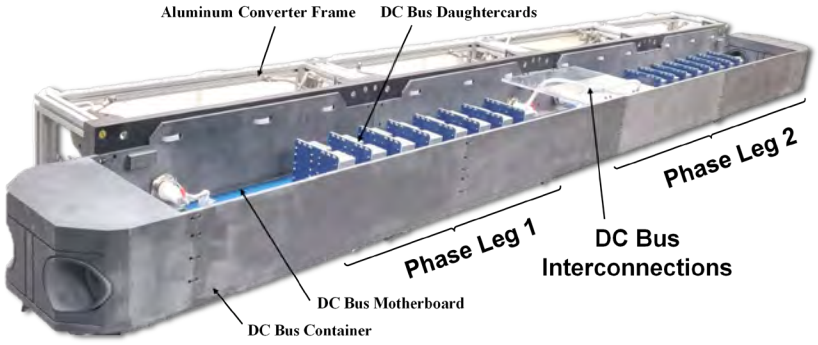

Fig. 2. Dual bus assembly configured for 2-phase converter.

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High-Frequency Transformer and 1.7 kV Switching-Cells for an Integrated Power Electronics Building Block (iPEBB)

This work presents the design of a 250 kW integrated power electronics building block (iP-EBB) for future electric ship applications. This work focuses on the motivation, design choices, and initial prototyping of a 500 kHz transformer, which forms the core of the converter. The transformer is designed for 13.8 kVAC and features a unique structure that meets insulation requirements while maintaining a compact and lightweight design. The prototype is designed with target ratings of 250 kVA, 1000 Vpri/1000 Vsec, 500 kHz with insulation suitable for operating in 20 kVDC or 13.8 kVAC systems. The size of the prototype is approximately 30 x 25 x 10 cm^3 and weighs less than 5 kg. To reduce the size of the transformer, the target-switching frequency for the inner bridges of the iPEBB is 500 kHz. The bi-directional topology of the iPEBB is shown in Fig. 1. To achieve this high-switching frequency, soft switching is employed for the inner bridges (blue). The outer bridges (grey) will be hard switching (10-20 kHz) and interface to the ac or dc line. The inner bridges interface with the transformer (green).

In conventional medium-voltage transformers, the insulation can become a sizeable fraction of the transformer weight and present a thermal barrier preventing effective cooling. To address this, the proposed transformer design uses an insulating sheet to separate the primary- and secondary-sides (Fig. 2(a)). The sheet is coated with conductive and semiconductive layers to reduce the electric field strength. Mica is used as the insulating sheet and has dimensions to meet the primary-to-secondary voltage insulation and creepage requirements. The insulating sheet is covered with a layer of conductive paint on the two surfaces where the primary and secondary coils and core sections are located. The conductive layers are referenced to the potentials of the two respective sides, thereby eliminating electric field stress in the air gaps around the windings (Fig. 2(b)). N49 ferrite is used for the core, and 6600/46 AWG litz wire is used for the windings. Based on initial test results, the transformer is expected to have core losses of 300 W and winding losses of 850 W at 250 kW, resulting in an efficiency of 99.5 %. Future work will involve testing the transformer with the rest of the iPEBB converter.

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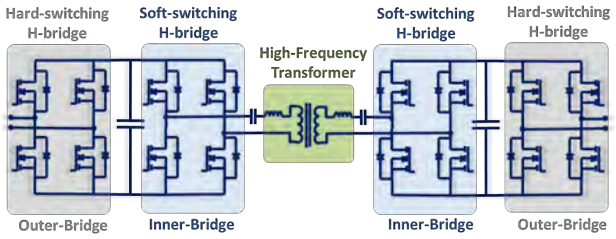


Fig. 1. iPEBB bi-directional topology with the transformer highlighted in green.

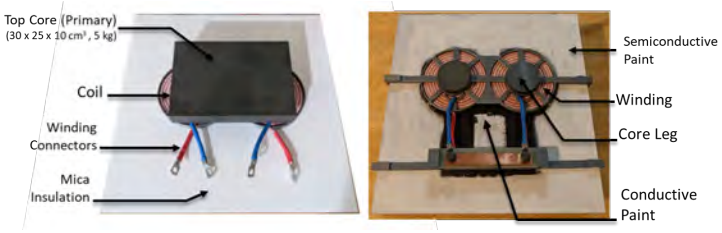


Fig. 2. Fastwatt transformer prototype (a) before the conductive and semiconductive paints are applied, (b) with the top core block removed to show the Litz wire coils and conductive (black) and semiconductive (white) paints.

1.7 kV SiC Switching-Cell for a High-Density Integrated Power Electronics Building Block (iPEBB)

This work focuses on the design, fabrication, and testing of 1.7 kV SiC MOSFET switching cells that form the 250 kW solid-state transformer-based integrated power electronics building block (iPEBB). The galvanically-isolated iPEBB can be stacked in series and parallel to scale the voltage and power, and can be used for ac or dc operation. Fig. 1 shows the iPEBB converter topology, which is made up of two H-bridges on both sides of a high-frequency transformer. The inner H-bridges are soft switching (blue), and the outer H-bridges are hard switching (red). A portion of the iPEBB's H-bridges, referred to as a switching cell, is fabricated to verify the layout and design of the power stage.

Fig. 2 shows the fabricated iPEBB switching cell. It is populated with two parallel 1.7 kV SiC MOSFETs per switch. State-of-the-art, multi-layer, silicon nitride, active metal brazed (AMB) substrates are used to develop a low inductance design for the iPEBB. The multi-layer design is made up of three copper layers divided by two silicon nitride dielectric layers. Vias connect the top copper layer to a middle copper layer, which enable a vertical power loop and negative mutual inductance cancellation. This cancellation allows for a reduced power-loop inductance of 3.5 nH. Furthermore, the multi-layer design creates an inherent screen that reduces the common-mode current through the cooling system. The multi-layer design uses thick copper layers, which enable good heat spreading. The copper layers of the switching cell are optimized to improve thermal performance while minimizing the weight increase of the iPEBB.

Initial electrical testing is completed on the switching cell to see its dynamic performance. Double pulse tests at 1 kV and 50 A are completed. The voltage fall time during turn-on is 20 ns and has a turn-on dv/dt of 40 V/ns with an overshoot of approximately 9 %. The voltage rise time during turn-off is 10.3 ns and gives a dv/dt of 77 V/ns. Furthermore, the switching cell is designed to maximize the heat-spreading capabilities while minimizing the weight of the iPEBB. The measured junction-to-case thermal resistance of the switching cell is 0.285 °C/W, which is comparable to single-layer ceramic substrates. The switching-cell design, fabrication, and testing will go into advancing -based PEBBs for future power systems.

This work was supported by the Office of Naval Research (ONR), with grant number N00014-16-1-2956. DCN: 43-9067-22.

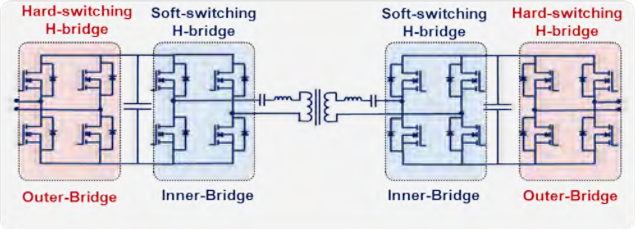


Fig. 1. Bi-directional topology for iPEBB with hard- and soft-switching H-bridges.

Fig. 2. Prototype of fabricated switching cell.

Bayesian Optimization of PCB-Integrated Field Grading for a High-Density 10 kV SiC Power Module Interface

High-voltage SiC MOSFETs have the potential to drastically improve the size and efficiency of power systems due to their higher operating voltages and faster switching speeds. To realize this potential, a 10 kV/75 A high-density (4 W/mm^2) SiC MOSFET package with low parasitic inductance (4.4 nH) is developed. The high-density design is enabled by minimal (6 mm) spacing between the terminals of the module. This is nearly six times closer than the terminals of the CREE XHV-9 10 kV SiC MOSFET module, which has a terminal spacing of 37 mm. The reduction in terminal spacing is made possible by fully enclosing the terminals, which circumvents the creepage and clearance distance requirements (Fig. 1).

To reduce the electric field strength in the air surrounding the interface, copper traces inside the PCB are used as field-grading plates that shift the peak electric field from the air to the FR4 dielectric, which has a higher breakdown field strength than air. The geometry and location of the field-grading plates is critical to their effectiveness. To design the geometry, a numerical optimization technique is used in conjunction with finite element analysis. The system is first decomposed into critical 2D design regions, which are then parameterized, and the locations of field crowding are identified. A weighted cost function is formulated using the breakdown strength of the materials and is optimized using an interior-point algorithm with finite difference derivatives.

One of these optimized cross-sections is shown in Fig. 2. The optimization results in copper conductors shaped such that the high-strength electric field is contained inside the FR4 dielectric, where the field can be supported without partial discharge. Meanwhile, the electric field in air is kept below the breakdown strength of air, resulting in a safe, reliable, partial-discharge-free operation. The optimized laminate bus bar and optimized module housing are built and experimentally demonstrate a partial discharge inception voltage of 11.6 kV rms under 60 Hz sinusoidal excitation.

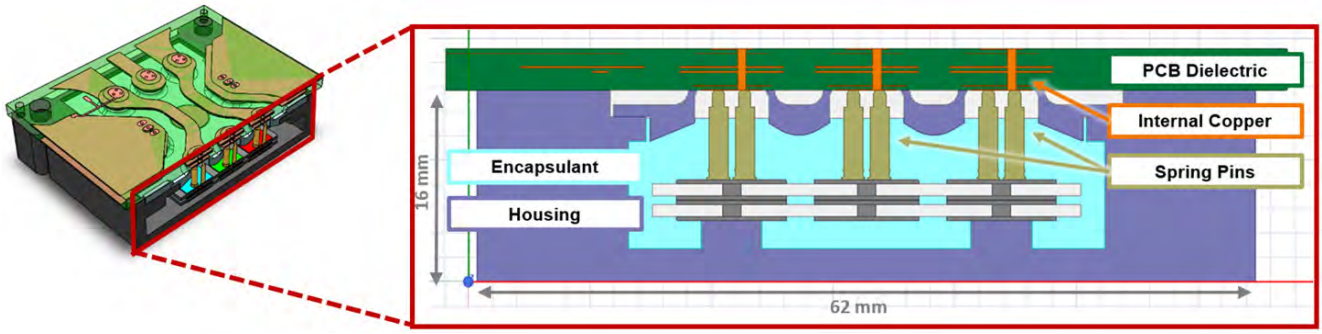


Fig. 1. SiC 10 kV power module cross-section.

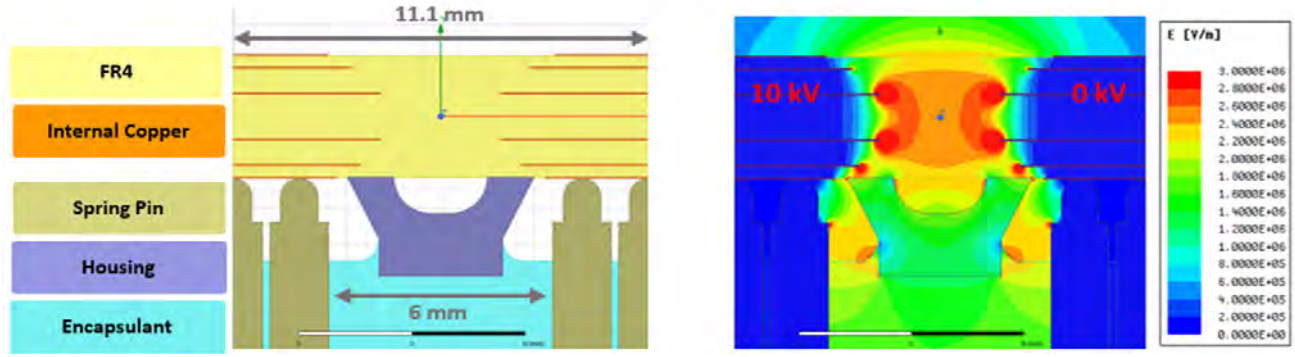


Fig. 2. Optimized cross-section supports 10 kV bus voltage without the electric field magnitude exceeding the 3 kV/mm breakdown strength of air.

Thermal and Thermomechanical Analysis of a 10 kV SiC MOSFET Package with Double-Sided Cooling

Medium-voltage wideband gap power devices such as silicon carbide (SiC) MOSFETs are an attractive alternative to traditional silicon IGBTs due to their reduced on-state losses, higher blocking voltages, and faster switching speeds. Packaging technology currently poses a significant hurdle towards the widespread adoption of medium-voltage SiC devices with existing standardized footprints limited in density and thermal performance. This work seeks to improve conventional medium-voltage packages by proposing a discrete 10 kV/25 A SiC MOSFET package (Fig. 1) that utilizes double-sided cooling to reduce junction-to-case thermal resistance (θ_{jc}) and improve power handling. The package footprint is 32 x 31 x 7 mm^3 and is built on 3rd generation 10 kV SiC MOSFETs from CREE with an on-state resistance of 300 mΩ.

Parallel heat flow paths are provided through the top and bottom of the die by means of wirebond-less molybdenum interconnects that serve as both the electrical connection to the die (replacing conventional wirebonds) and conduction of heat from the die to an upper substrate. High thermal conductivity materials such as aluminum-nitride ceramic and sintered silver die-and post-attach are used to reduce the junction-to-case (θ_{jc}) thermal impedance. Special care is taken to manage thermomechanical stress inside the package as materials with high-thermal conductivity generally tend toward larger Poisson's ratio, and can exhibit larger thermomechanical stresses due to mismatches in the coefficient of thermal expansion. This leads to a trade-off between low thermomechanical stress and low θ_{jc}. In this work, finite element simulation via ANSYS® and Abaqus® (Fig. 2) is used to evaluate this trade-off and select appropriate materials to ensure high thermal performance without sacrificing reliability.

The θ_{jc} of the assembled package is characterized on a JEDEC 51-14-compliant test bed and experimentally determined to be 0.17 °C/W overall, 0.25 °C/W and 0.57 °C/W on the lower and upper cooling surfaces, respectively. The package is run continuously with a dc channel current of 150 W to pin the junction temperature at a constant 150 °C for 30 minutes, after which no degradation of the silver sinter bond lines is observed. This work demonstrates the viability of double-sided cooling for packages up to 10 kV and the performance improvements that can be gained over the existing state-of-the-art.

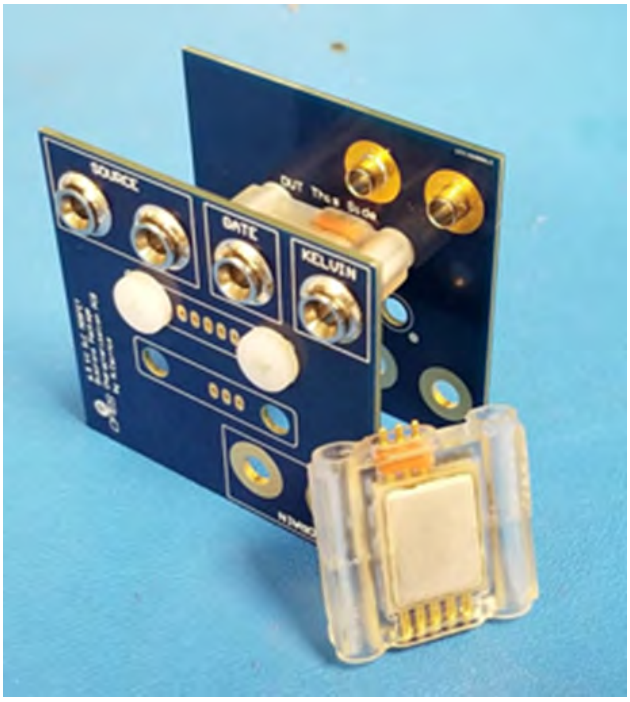


Fig. 1. 10 kV/25 A discrete SiC MOSFET package measuring 32 x 31 x 7 mm^3 shown mounted to two PCB busbars.

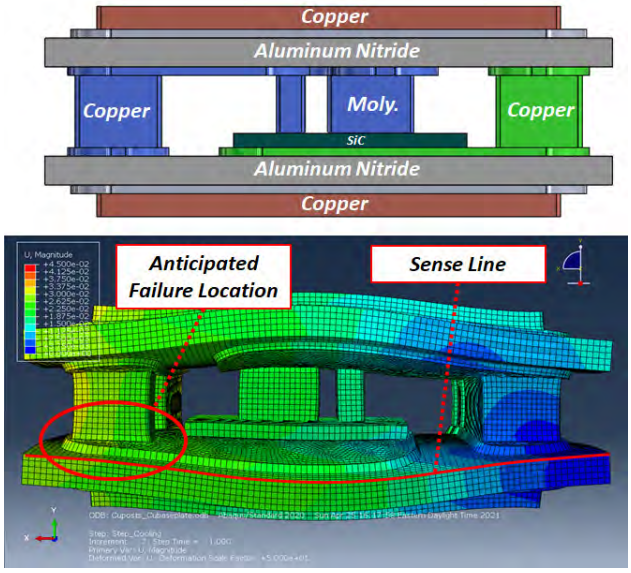


Fig. 2. Thermomechanical simulation showing vertical deformation during cooling after sintering.

A PCB-Embedded 1.2 kV SiC Half-Bridge Module for EV On-Board Charger Applications

In this work, the PCB-embedded 1.2 kV SiC MOSFET half-bridge module with integrated gate drive circuitry, shown in Fig. 1, is designed and analyzed for use in a 22 kW electric vehicle on-board charger (OBC). The die embedding is performed by AT&S using their PlAnaR Surface-Embedded Component (PARSEC) technique, which allows for gate and source electrical connections to be made with copper-filled microvias. The design methodology used to create this module is based on understanding the trade-offs between thermal and electrical performance in PCB-embedding and using that knowledge to achieve the performance required by this application. To minimize the thermal resistance of the FR4 layers, microvias are used to connect the source-side and drain-side inner layers to their outer layer counterparts. 4 oz and 3 oz copper layers are used for the inner and outer layers, respectively, to balance the trade-off between heat spreading and gate drive manufacturability. The gate drive circuitry is integrated to reduce loop inductances.

Following the design and manufacturing, the PCB-embedded half-bridge modules are experimentally tested to measure their performance. The source-side and drain-side junction-to-case thermal resistances are measured to be 0.41 K/W and 0.17 K/W, respectively, using the JEDEC51-14 standard and a Phase 12 B Thermal Analyzer. Under similar operating conditions, the PCB-embedded half-bridge module achieves 5.6 times lower voltage overshoot during turn-off and 0.5 % higher efficiency than a TO-247 package containing the same SiC MOSFET. With the help of soft switching and low loop inductances, the measured peak efficiency and power density of the 22 kW three-phase ac-dc converter prototype with six PCB-embedded half-bridge modules (seen in Fig. 2), are 98.2 % and 182 W/in^3, respectively.

The experimental results obtained in this work provide evidence that PCB-embedding is a viable packaging method for use in electric vehicle OBCs. The integrability, power density, and thermal and electrical performance afforded by PCB-embedding makes it a great candidate as a packaging method for SiC MOSFETs. The large-scale adoption of PCB-embedding in power converters hinges on reducing manufacturing costs and gaining a better understanding of the failure mechanisms seen in power and thermal cycling.

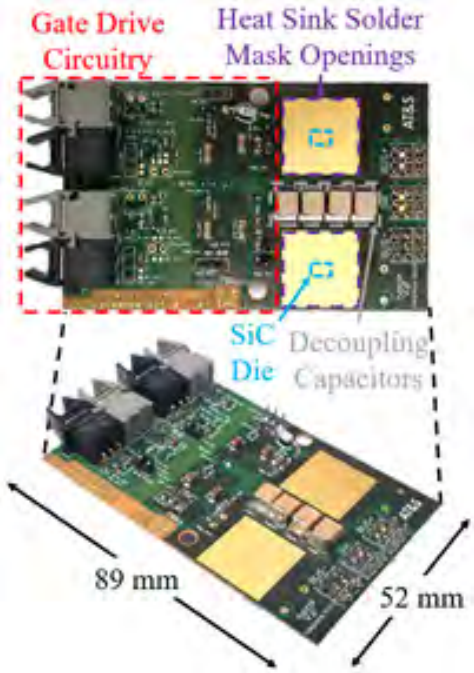


Fig. 1. The PCB-Embedded half-bridge module.

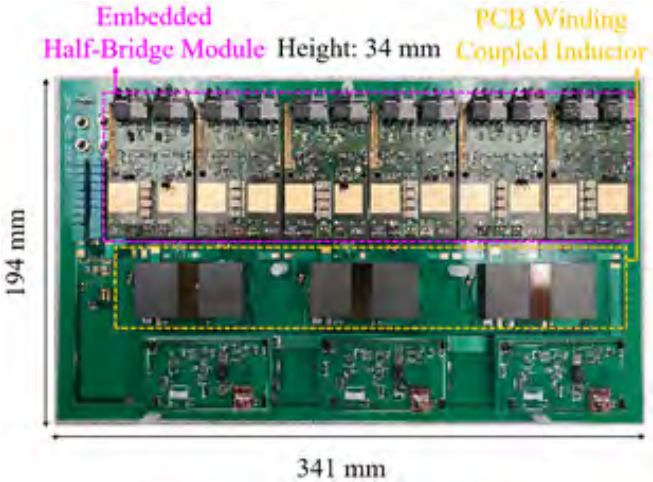


Fig. 2. A 22 kW three-phase, ac-dc converter prototype with six PCB-embedded half-bridge modules plugged into the motherboard containing the PCB winding coupled inductors.

Analysis of EMI Mitigation for SiC Power Modules Using an Integrated Common-Mode Screen

The high-frequency operation of wide-bandgap (WBG) power semiconductors, along with high-dv/dt transients during switching, results in significant electromagnetic interference (EMI). The EMI generated has become a critical roadblock in fully benefitting from the various advantages provided by WBG devices. This work investigates the influence of embedding a common-mode (CM) screen and decoupling capacitors into the power electronic module architecture on the EMI noise generated during switching transients. The aim is to inform EMI mitigation strategies that can be implemented at the power module design stage and result in modules with lower noise emissions in the conducted EMI frequency range.

The hardware implementation of the embedded CM screen module architecture explored is shown in Fig. 1. The CM screen is formed by using a two-layer substrate and connecting the middle layer to the power terminals. The current generated by the high dv/dt at the switching node of the half-bridge is then redirected, reducing the current flowing through the baseplate. The amount of current diverted will depend primarily on the impedance of the CM screen path to the connected terminal. In this work, the embedded CM screen is shorted to the midpoint of the bus voltage, which is formed by the series connection of embedded capacitors. The midpoint connection to the CM screen further helps by evenly distributing the electric field in the ceramic layers.

To evaluate the EMI noise generated, a baseline module with no embedded CM screen, decoupling capacitors, and the module, shown in Fig. 1, are switched in a buck converter topology with a switching frequency of 100 kHz, input/output voltage of 600 V/300 V, and an output current of 12 A. The EMI noise current flowing through the baseplate of the modules is measured and compared as shown in Fig. 2. Initial test results show that due to the introduction of the embedded CM screen and decoupling capacitors, noise mitigation of up to 25 dB is observed in the conducted EMI frequency range.

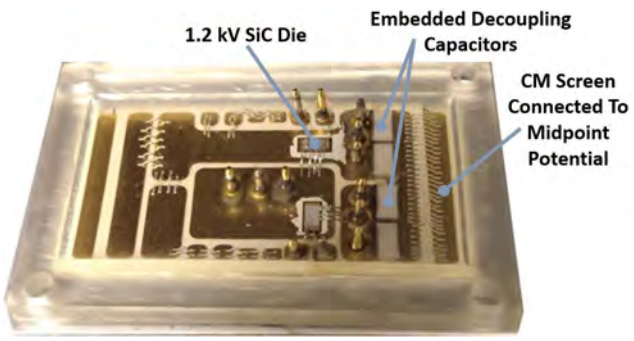


Fig. 1. 1.2 kV SiC half-bridge power module with embedded CM screen and decoupling capacitors.

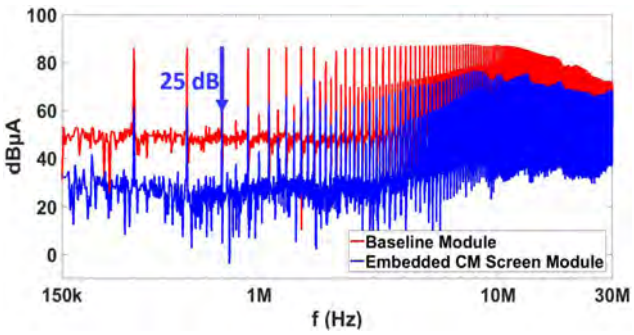


Fig. 2. Measured noise current through baseplate with and without the embedded common-mode screen.

A Multi-Channel High-Frequency Current Link-Based Isolated Auxiliary Power Supply for Medium-Voltage Applications

10 kV SiC MOSFETs enable a high-frequency power conversion solution in medium-voltage applications, offering a smaller converter size and better performance. However, as a consequence, the auxiliary power supply (APS) design becomes more challenging. To ensure the device's safe operation, it requires the APS to achieve a high isolation level, low coupling capacitance (C_{cm}), and small footprint. Since these three requirements are difficult to achieve at the same time, design balances exist in the APS design.

This work first presents the circuit design of a 1 MHz current-fed APS using LCCL-LC resonate topology with a single-turn transformer to reduce the overall size and realize multi-load driving ability. Then, based on the designed APS, eight insulation schemes using different dielectric materials and electric-field (E-field) stress control techniques are introduced. In the analysis, FEM and Q3D simulations are performed to evaluate the E-field distribution and C_{cm} value for each solution. Considering insulation capability, manufacturability, and C_{cm} values, as shown in Fig. 1, two designs using air and silicone as insulation materials are selected and evaluated by hardware experiments.

With a threshold discharge value of 10 pC, the air-insulated design achieves PD free of 5.8 kV with measured C_{cm} value of 1.25 pF. Due to higher dielectric strength, the silicone-insulated design achieves a higher partial discharge inception voltage of 16.4 kV with C_{cm} value of 3.9 pF. Both designs are able to drive a maximum power of 20 W without any thermal issues. Although in this work, only two solutions are built, all proposed insulation schemes can be applied to other APS system designs.

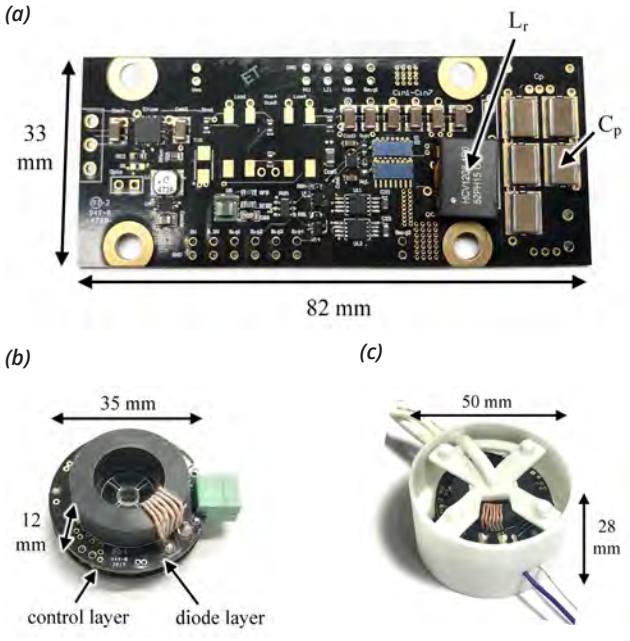


Fig. 1. Hardware prototypes of (a) sending side circuitry, (b) air-insulated receiving side circuitry, and (c) silicone-insulated receiving side circuitry.

Active Control and Gate-Driver Design for Voltage Balancing of Both MOSFETs and Body-Diodes in Series-Connected SiC MOSFETs

To further push the device operating voltage for applications beyond 10 kV, a series connection of 10 kV SiC MOSFETs is a cost-effective solution. However, a severe voltage imbalance issue exists among series-connected devices under higher switching speed conditions because of the difference in the parasitic capacitors and gate signals of different devices. Voltage balancing is required for series-connected SiC MOSFETs.

To guarantee the balance voltage sharing under both MOSFET and body diode conducting periods, this work proposes to apply different active voltage balance strategies in different periods: 1) In the body diode conducting period, to solve the voltage unbalance caused by the dv/dt difference, an extra short-pulse gate signal (SPGS) on the device with a higher turn-off voltage is proposed, which controls the MOSFET channel current to affect the voltage sharing. 2) In the MOSFET conducting period, to solve the impact of the gate signal mismatch, an active gate signal delay time (GSDT) control to mitigate the time mismatch on the gate signal is proposed. The SPGS with a fixed duration is also applied in the MOSFET conducting period to eliminate the impact of dv/dt difference on the GSDT control.

To implement the proposed voltage balancing method, a new gate driver (Fig. 1) is designed with improvements on the turn-off voltage sensing and gate signal control. Experiments with two series-connected 10 kV SiC MOSFETs under different conditions are conducted, and the results verify the proposed voltage balancing method. Fig. 2 shows the transient, and that the voltage sharing of diodes are balanced by the closed-loop control.

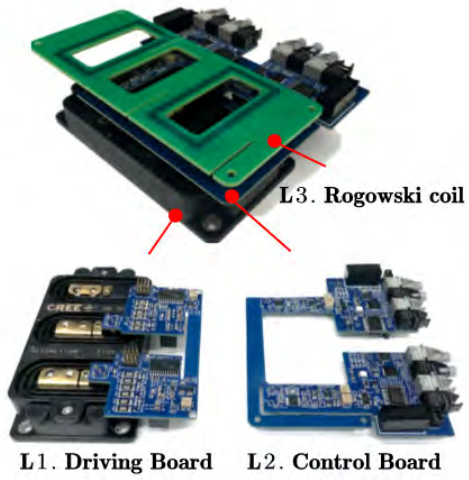


Fig. 1. Gate driver prototype with proposed control.

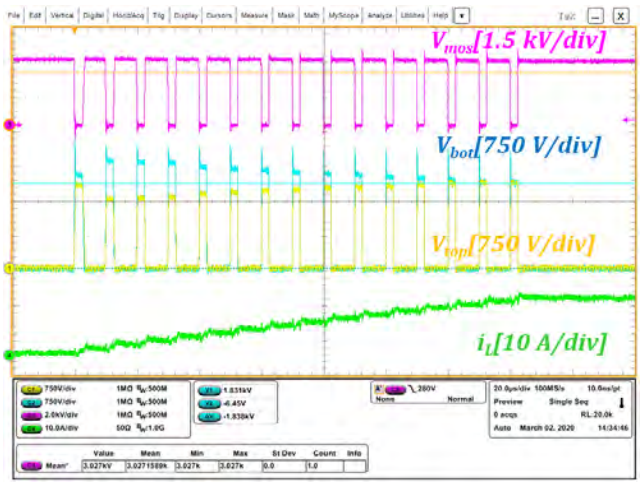


Fig. 2. Voltage sharing of body diodes with short pulse gate signal.

Magnetic and Thermal Design of Litz Wire 500 kHz High-Power Planar Transformers With Converging Cooling Duct for a DC Transformer Resonant Converter Application

This work presents the design and analysis of two Litz wire transformers for a 500 kHz, 18 kW partial-power-processing (PPP) converter. Because the two power paths in the PPP converter operate as "dc transformers" (DCX), both transformers are designed with the goal of leakage inductance minimization in order to reduce gain variation around the resonant frequency. The selected winding topology with the lowest leakage inductance results in an impedance mismatch among parallel secondaries used in the majority power path transformer, resulting in poor current sharing. In order to balance the goals of leakage inductance minimization and even current sharing, a new winding technique called "intra-leaving" is presented, which reduces the current sharing error from 50 % to 5 %. Due to increased loss per unit volume in power transformers when operating at higher frequencies, the increase in cooling system size can outweigh the transformer size reduction benefits.

Conventional air-cooling design simply adopts an over-sized high airflow fan to keep the transformer within a desired thermal limit, which reduces power density and efficiency. This work seeks to address this trade-off by presenting a high-density, low-profile, forced-air-cooling duct system for high-frequency transformers. Different cooling duct designs are presented and analyzed, considering the trade-offs between design complexity and cooling performance. A pair of 500 kHz planar transformers with 18 kW ratings are used to demonstrate the proposed cooling system and achieves a power density of 635 W/in^3, peak height of 43 mm, cooling power consumption of 6.8 W, and 8 % peak temperature reduction when compared to cooling the transformers with a 120 mm x 120 mm, 25 W fan. Peak winding temperature at 15 kW load was 106, and peak core temperature was 72. The proposed transformer with the cooling ducts also achieves four times higher power density than the setup using a 120 mm x 120 mm fan.

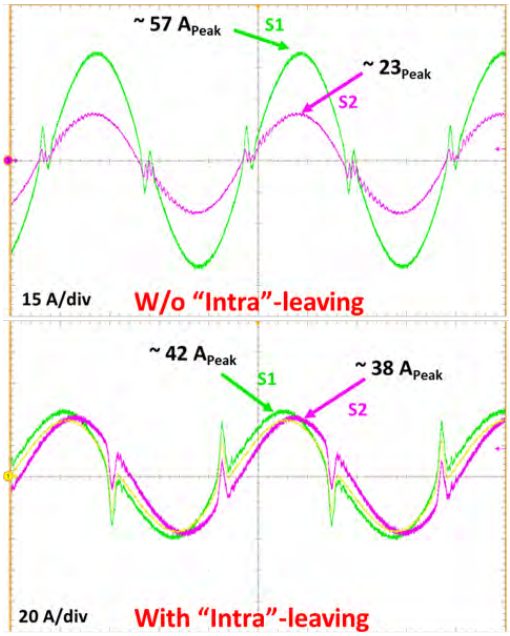


Fig. 1. Current sharing results with and without "Intra-leaving."

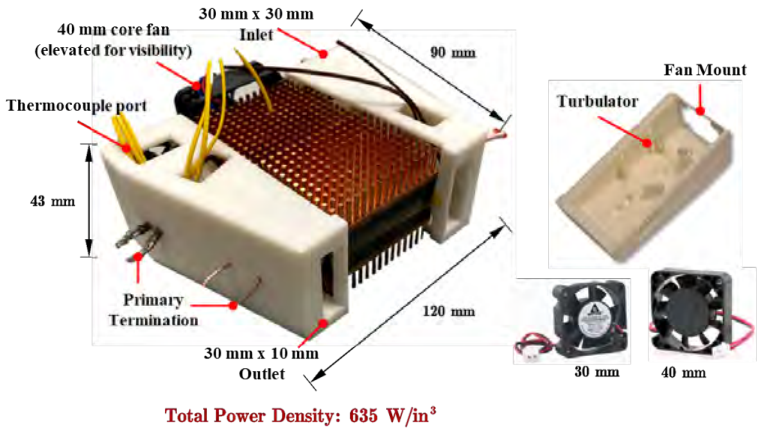


Fig. 2. Proposed cooling system with converging cooling ducts.

High-Power-Density Design of Power Electronic Interrupter in Medium-Voltage Hybrid DC Circuit Breaker

Circuit protection is a key enabler for future medium-voltage, direct-current (MVDC) distribution systems. The hybrid dc circuit breaker (HCB) offers low conduction losses and reasonably fast response times but suffers from large size. In this work, a high-power-density power electronic interrupter (PEI) design is introduced in terms of single module design, turn-off strategy, and whole system optimization.

As an important part of the HCB, the PEI plays an important role in the conduction and interruption of surge current. Although it is based on the series semiconductor devices, the design focus is quite different than that of the normal power converters. In this work, the design procedure based on a modular PEI concept is introduced and investigated. The surge current conduction and interruption tests are performed for the selected candidates. With two types of the voltage clamping circuit, the single module design can be determined. In addition, the proposed staged turn-off strategy can improve the MOV energy balance, and average its life span. The integration of nine modules demonstrates a very high-power density of 7.4 kW/cm^3. The experimental results validate the current interruption function the designed PEI and HCB achieve at a 6 kV dc bus.

With good scalability, the PEI concept and the HCB architecture show great potential in the MV dc distribution system and even higher voltage applications.

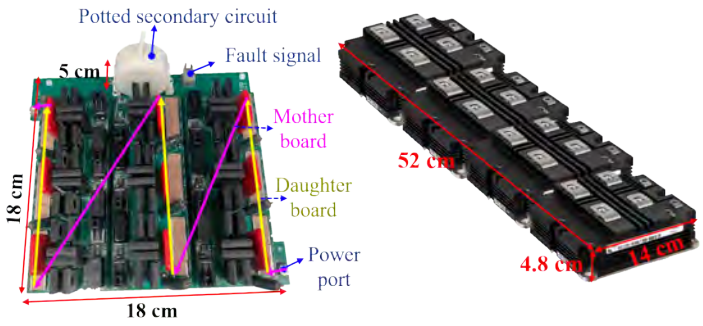


Fig. 1. Designed PEI and comparison with IGBT modules.

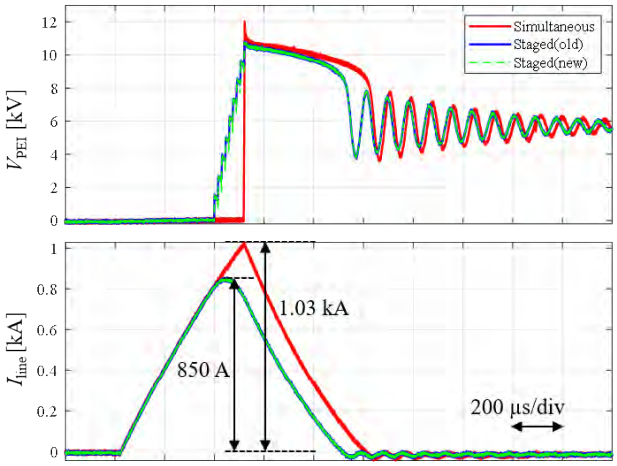


Fig. 2. Waveforms of PEI with three turn-off strategies.

Switching Transition Analysis and Optimization for Bi-Directional CLLC Resonant DC Transformer

In this work, a comprehensive switching transient analysis for an open-loop CLLC-DCX with DAS modulation is presented, as shown in Fig. 1. Among seven ZVS transition types, one desirable "Sync-ZVS" transition is identified with merits of minimum deadtime, load-independent voltage-gain, and no deadtime conduction loss, as shown in Fig. 2. In order to achieve this "Sync-ZVS" transition in the full load range, an ACS method is proposed based on currents decomposition. Following this method, an overall design procedure for an open-loop CLLC-DCX with DAS modulation is proposed to achieve high efficiency.

Finally, the proposed "Sync-ZVS" transition and "ACS" method are both verified by three 18 kW CLLC-DCX prototypes with DAS modulation, which all operate around 500 kHz and have 98.8 % peak efficiency, as shown in Fig. 3. The proposed method has great potential to improve the performance of DCX used in EV charging systems and solid-state transformers.

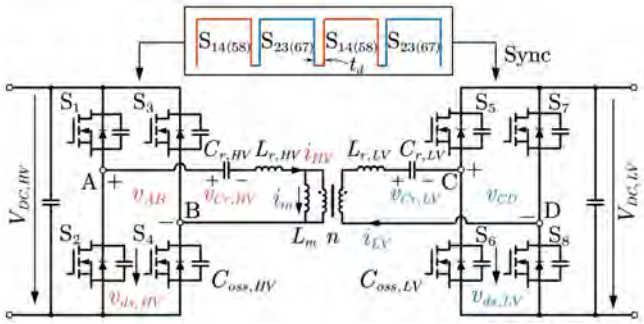


Fig. 1. CLLC-DCX topology.

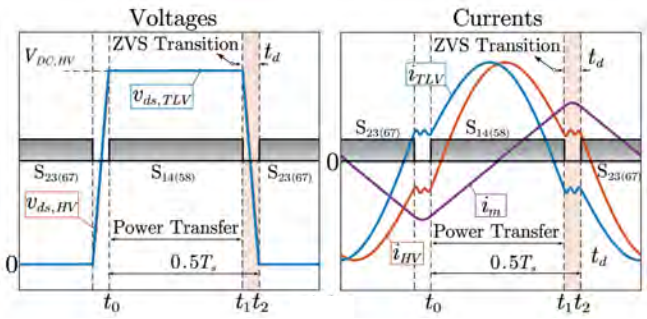


Fig. 2. "Sync-ZVS" transition.

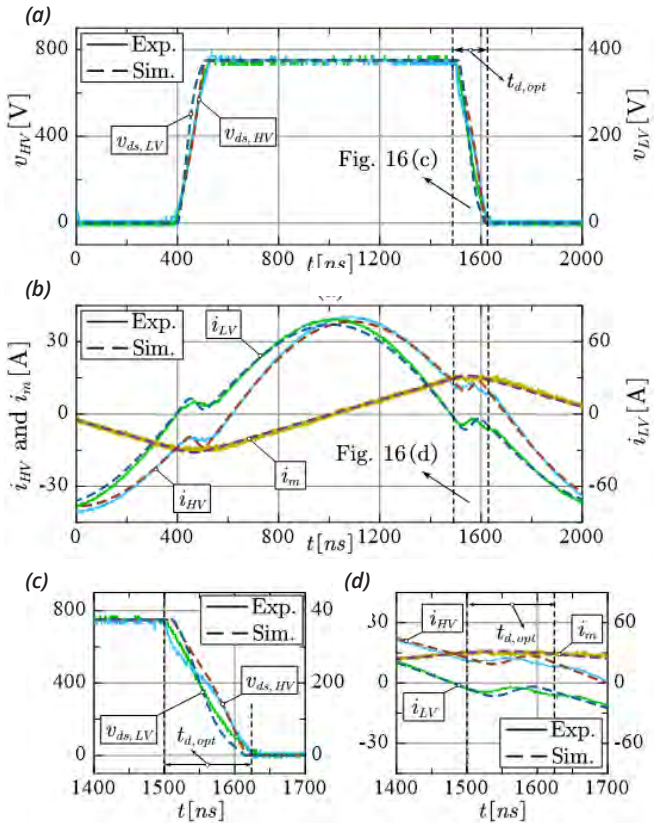


Fig. 3. Simulation and experimental results of CLLC-DCX with "Sync-ZVS" transition. (a) Voltage waveforms. (b) Current waveforms. (c) Zoomed-in voltage waveforms. (d) Zoomed-in current waveforms. The CLLC-DCX operates at 18 kW with fs,opt as 455 kHz.

Design of 2×211 kW High-Power-Density Aircraft Motor Drive System

Two 211 kW three-level T-Type inverters are designed for a dual-winding aircraft motor. The power density of the prototype is up to 19.7 kW/kg and efficiency is over 99 %. The three-level (3-L) T-Type inverter is selected because it reduces the weight of the EMI filters, and the switching loss is reduced effectively, compared to the 2-L inverter. A special busbar design is made for this project, and the high-frequency decoupling path and high-current path are separated to achieve a good thermal performance and low loop-inductance at the same time.

The Rogowski coil is used to realize the current sensing and short-circuit protection, which helps achieve a higher bandwidth and lower weight. The gate driver, decoupling path, and Rogowski coil are integrated in one PCB board. The device current can be reconstructed by the integrated Rogowski coil, and it matches the results with the commercial Rogowski coil well, as shown in Fig. 1.

A hybrid 3-L PWM scheme is developed to reduce the neutral point imbalance and reduce the THD at the same time. The prototype is shown in Fig. 2, and the full-power test waveforms are shown in Fig. 3.

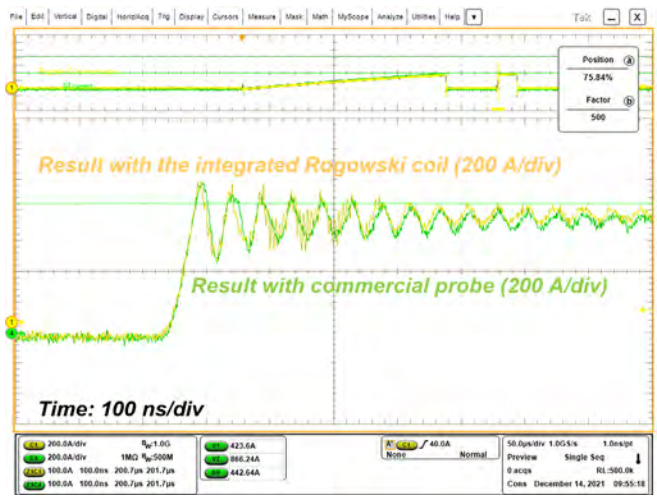


Fig. 1. The Rogowski coil embedded in the gate driver and busbar.

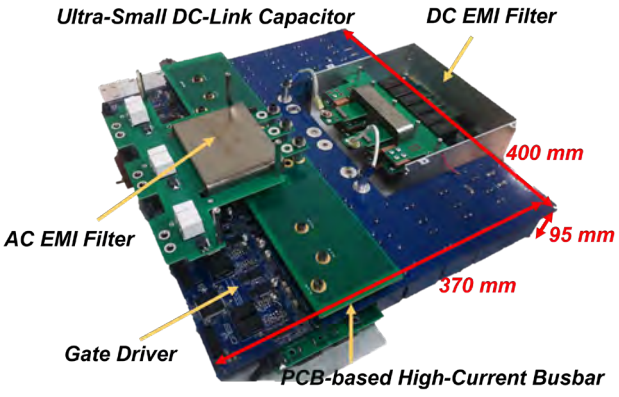


Fig. 2. Prototype of the 211 kW inverter.

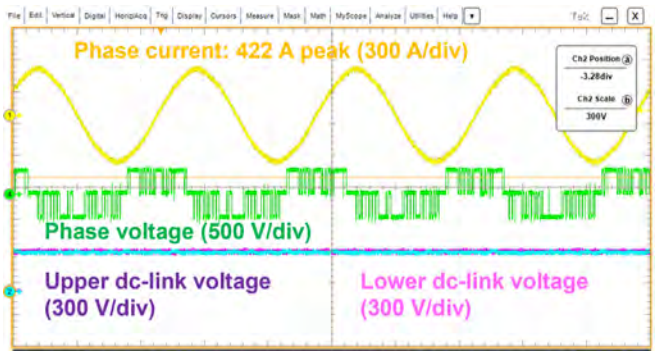


Fig. 3. Full-power test results.

Analysis and Assessment of Soft-Switching Inverters for a 200 kW Traction Drive in Electric Vehicles

Using a soft-switching inverter topology for a low-voltage, high-current traction drive inverter remains unclear. In this work, four widely accepted topology candidates, including the two-level inverter (2-L), three-level T-type inverter (T^2), auxiliary resonant commutation pole inverter (ARCP), and six-switch inverter with coupling inductor (6S), are selected and investigated for a 200 kW SiC-based traction inverter. Considering the voltage stress of switching positions, three SiC device candidates with different characteristics are chosen from the current market.

First, the system specifications, as well as the component candidates, are introduced. The power devices, including one from UnitedSiC (due to its high-switching energy but low conduction resistance for soft-switching), and another one from Microsemi (because of its overall performances for hard-switching), are chosen from the original 50+ devices on the market. Moreover, two capacitor candidates, which are CeraLink and film capacitors, are considered for the dc-link capacitor.

Next, the mechanism of the topology candidates is discussed in detail in order to identify key parameters for power loss calculations. Based on the different voltage stress of different switching positions and current components in the auxiliary branch, the loss distribution of soft-switching topologies are calculated and analyzed. Since the switching-on loss is greatly eliminated and the generated conduction loss is combined in the auxiliary branch, the conduction loss is dominant in soft-switching inverters. The conduction loss is directly proportional to the output current.

The final comparisons for the four topology candidates are shown under 20 kHz and 100 kHz, using CeraLink and Film capacitor as the dc-link capacitor. It is clear that the performance of the soft-switching inverters largely depends on the power device technology or characteristics. By using the latest device, such as Microsemi for the 2-L inverter, the efficiency improvement by using a soft-switching inverter is always less than 0.2 %, while having higher cost and volume.

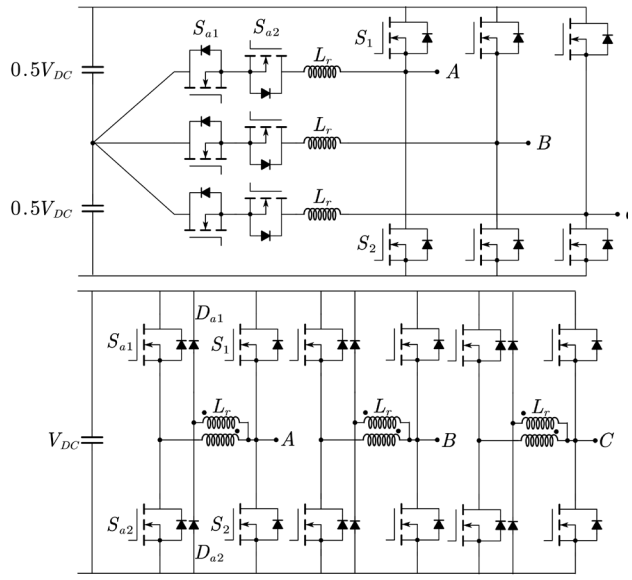


Fig. 1. Two soft-switching topology candidates, the ARCP and 6S with coupling inductor.

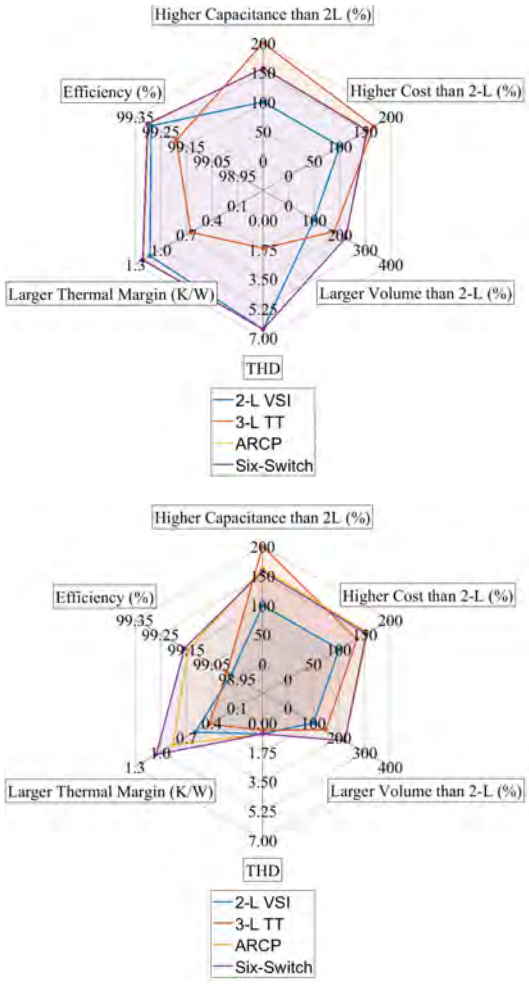


Fig. 2. Final comparisons for topology candidates, using CeraLink as dc-link capacitor, under (a) 20 kHz and (b) 100 kHz.

Weight-Minimizing Optimization of Microchannel Cold Plate for 200 kW SiC-Based Traction Inverters

In this work, a weight-minimizing optimization is adopted for a microchannel liquid cold plate to cool the SiC MOSFET in a 200 kW traction inverter. First, the mathematical model of the microchannel cold plate is derived in detail. Based on the derived mathematical model, by setting up desired geometry parameters of the microchannel cold plate, both thermal and pressure drop performance can be predicted in a short time without conducting time-consuming computational fluid dynamic (CFD) simulations. Moreover, the Pareto optimization can be conducted for the purpose of finding minimum weight points of the microchannel cold plate without exceeding the system's thermal and pressure drop limitations.

Also, two different liquid flow path configurations, which are series flow path (V1 Series) and parallel flow path (V2 Parallel) are designed based on geometry parameters from optimizations. Considering the footprint area of 360 cm^2, both versions of the cold plate have weight less than 810 g with cost lower than $300/Unit. Furthermore, the liquid cooling testing environment is set up in CPES to verify the accuracy of the derived mathematical, i.e., the thermal and pressure drop performances. Eventually, a trade-off analysis between the two flow path configurations is compared and discussed. To summarize, the V2 Parallel design is a more attractive candidate based on overall performances. The designed V2 Parallel has the thermal resistance around 0.008 °C/W and pressure drop lower than 0.4 bar at the system's maximum flow rate of 0.25 kg/s, while having 810 g for the footprint area of 360 cm^2.

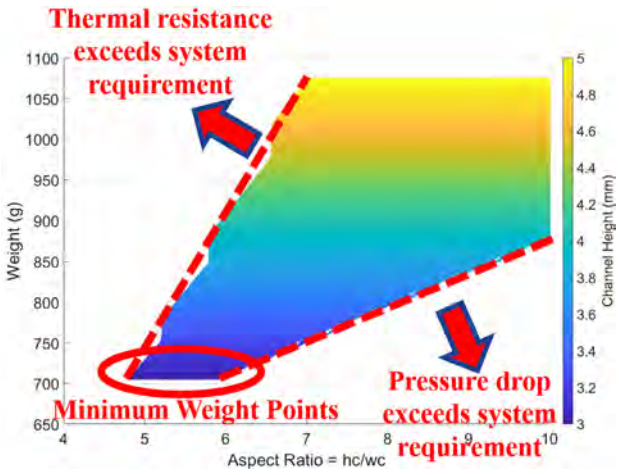


Fig. 1. Weight-minimizing Pareto optimization map for microchannel cold plate.

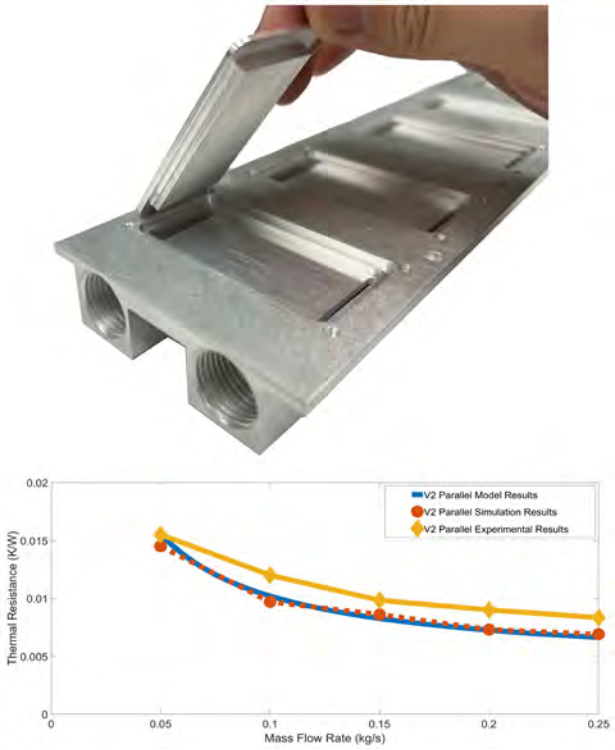


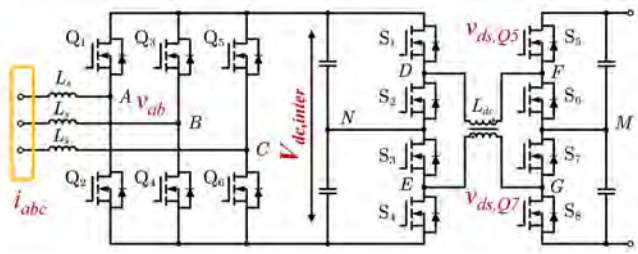
Fig. 2. Designed V2 parallel microchannel cold plate composed of base plate and fin plate, and its testing results comparisons.

Design and Implementation of Bi-Directional Three-Phase Two-Level Converter Cascaded With Stacked Non-Inverting Four-Switch Buck-Boost DC-DC Converter

In this work, a bidirectional, three-phase, two-level converter and a cascaded, bi-directional, dc-dc converter are shown in Fig. 1(a). The converter assembly is shown in Fig. 1(b). The converter is rated for 50 kW, 75 kVA with 480 V AC port, 900 V internal dc bus, and 500 V-1000 V external dc port. The three-level, dc-dc converter is a stacked, non-inverting, four-switch buck-boost (FSBB) converter with a coupled inductor, which reduces the blocking voltage of each switching device. With the quadrangle inductor current waveform control method, all switches of the dc-dc converter can achieve zero voltage switching (ZVS) conditions while minimizing inductor RMS current. The operation with the unit-gain of the dc-dc converter waveform is shown in Fig. 2 .

In order to achieve quadrangle control of the stacked FSBB converter, the intelligent gate driver is designed to integrate the sensing capabilities, including dedicated on-state and off-state voltage-sensing circuits and the non-intrusive current sensor for each switching device. With fiber optic communication with the local controller, close-loop control can be achieved. Together with the gate driver integrated temperature sensor, the device on-resistance Rds-on can be estimated, and the device operation health status can be monitored.

(a)



(b)

Fig. 1. Full converter (a) topology and (b) assembly.

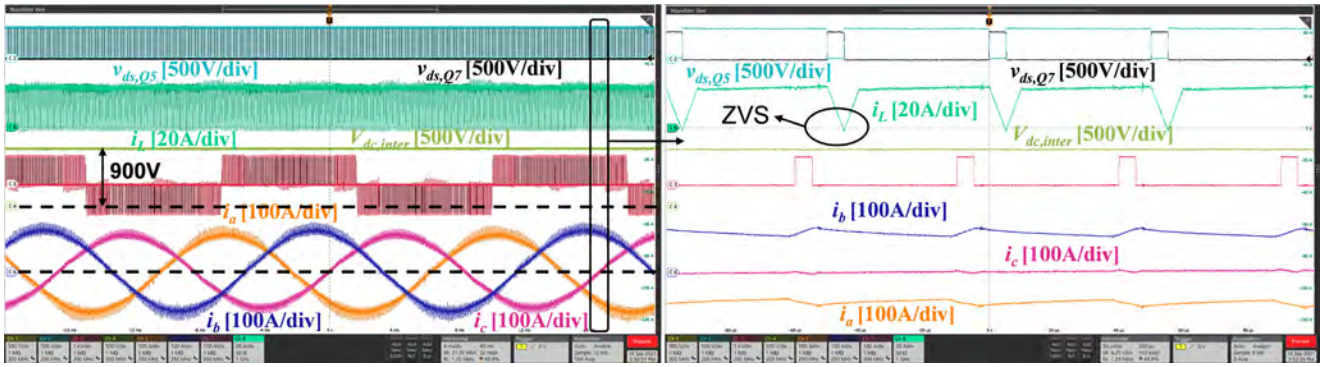


Fig. 2. Operation waveform of (a) ac-dc converter and (b) dc-dc converter with quadrangle control.

Real-Time Industrial Communication Protocols: A Comparative Study

Communication between different levels and nodes in power electronics systems allows the implementation of distributed control. An excellent example of that is Switching Cycle Control (SCC), where the main assumption is that the Gate Driver (GD) can run Peak Current Mode Control (PCMC) autonomously, and the only information it needs for running is the current reference. Flexibility is another important benefit of communication. As compared with the traditional approach of running power electronics systems where a Pulse Width Modulated (PWM) signal is sent from the controller to the GD, the communication allows different data to be exchanged between the GD and controller using the same or additional transmission line. Communication brings hardware simplification. For example, information collected from sensors used for gate driver protection can be implemented for control; therefore, fewer sensors are needed for the system. Hardware and software abstraction can be achieved using communication - an abstraction of power stage terminal behavior independent from hardware design, such as a hardware abstraction layer (HAL). Synchronization is the key aspect of reliable control. Communication allows synchronization protocols over communication lines such as SyncE, PTP, or state-of-the-art White Rabbit.

As shown by J. Hibbard in "5 Real-Time, Ethernet-Based Fieldbuses Compared", TABLE I compares several industrial real-time communication protocols in an application where 100 nodes need to be controlled synchronously. The two criteria analyzed in terms of performance measurement are the response time (cycle time) and the jitter (e.g., the variation in response time). It appears that most of the existing real-time communication protocols are based on Ethernet, and that the communication speed is 100 Mbps or faster. The latest version of EtherCAT supports speed up to 10 Gbps.

TABLE I

Real-Time Industrial Protocols Comparison

Protocol	Response Time	Jitter	Data Rate Mbps	Based on	Open Source
EtherCAT	**0.1 ms**	**< 0.1 ms**	**100**	**Ethernet**	**Yes**
Ethernet/IP	1 ms	< 1 ms	100	TCP/IP	Yes
Ethernet Powerlink	< 1 ms	< 1 ms	100	Ethernet	Yes
PROFINET IRT	< 1 ms	< 1 ms	100	Ethernet	Yes
SERCOS III	< 0.5 ms	< 0.1 ms	100	Ethernet	Yes

Dynamic Phasor Modeling of Multi-Converter Systems

With the increase in the deployment of distributed and renewable energy resources, the application of power electronics such as power processing units between sources, loads, and energy storage systems has also increased. To ensure better design, stability, and sustainability of the power grid in the future, simulations of large-scale interconnected power electronics units are essential. In this work a time-frequency domain approach, known as the dynamic phasor method, is represented. An application of this method, in a parallel combination of single-phase voltage source inverters, is expanded to a general form with any number of interconnected converters. For modeling this system, time-varying Fourier representations of the differential equations that represent all stated variables of individual VSIs in different load conditions are formed. Then, using the DP representation of components at the point of common coupling, all of the equations that describe any number of VSIs are coupled to represent the completed model for any number of parallel-connected converters. This methodology is then numerically validated by comparing it to the detailed switching modeling method and is used to model up to 100 parallel-connected converters. An approach for comparing the accuracy and computational efficiency of this method with the detailed switching model is presented. The computational efficiency of this modeling method is compared with the detailed switching model in terms of a time step comparison. In the experiment case, the DP modeling method can have 16.6 times larger time step in comparison to the switching model with a similar value of RMS error rate. Accuracy of this method is compared with the detailed switching model in time and frequency domain. Also, a test case is designed to model between 5 to 100 parallel-connected voltage source inverters to compare the computational efficiency of the model with the detailed switching model. Multiple time domain and frequency domain representation of the modulator, including multi-frequency modulation signal modulators is also used in this modeling method. It expands the capability of the conventional DP method in observing the instability cases that are invisible to average models but visible to switching and dynamic phasor-based models. That opens the space for applying this modeling method to large-scale converter networks while providing a better understanding of harmonic content and more reliable simulation results.

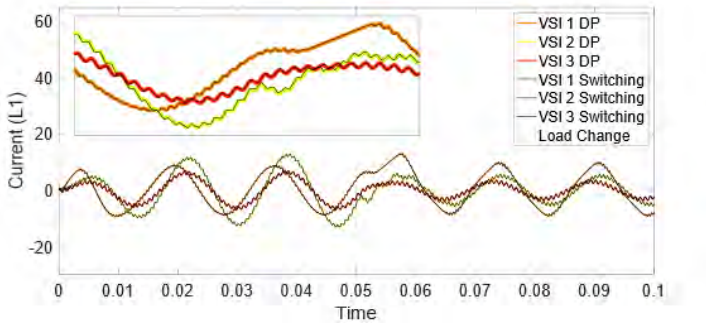


Fig. 1. Comparison of the output voltage of three voltage source inverters.

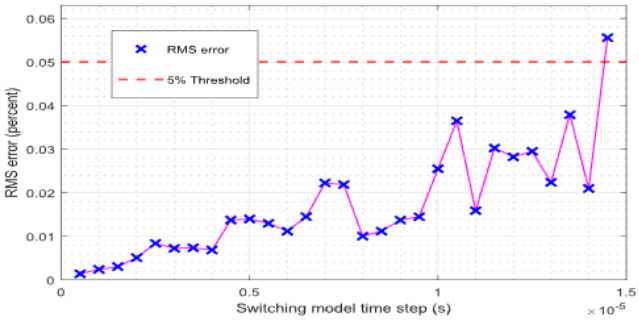


Fig. 2. Measurement of accuracy of detailed switching model.

Design Optimization of a Thermal Management System for Medium-Voltage Modular Converters

In this work, a weight-optimized thermal management system for the switching module is designed, considering all operating functions of a medium-voltage modular converter in a ship power conditioning system application. In the first step, a worst-case loss analysis is conducted for the switching device, covering all operating conditions of the medium-voltage modular converter. A thermal management system is then designed to dissipate the maximum loss. To embed the thermal management system design into the hierarchical power system optimization process, an analytical model is constructed for the cooling system with improved design efficiency and accuracy. In this analytical model, a heat transfer coefficient *h* is first calculated, considering the fan selection and the dimensions of the heat sink. Then, by assuming the Neumann boundary condition, a heat-spreading model is constructed for the heat sink base plate. From this model, the temperature distribution across the heat sink top surface is obtained, and the hot spot temperature under the heat source is calculated, which can be used to estimate the junction temperature of the switching device. Other applications of this analytical thermal model involve the optimum placement study of a power module and the thermal coupling study of multiple heat sources on a single cooling plate. The accuracy of this analytical thermal model has been verified by both simulations and experiments. Fig. 1 shows one of the application examples with this analytical thermal model. In this design example, as depicted in Fig. 1(a), two heat sources, which each dissipates a 200 W of loss, are placed on the top surface of the heat sink of known dimensions. Applying the analytical model, the temperature distribution across the top heat sink surface is calculated. The result is plotted and then compared with the FEA simulation, as shown in Fig. 1(b). From the comparison, it is observed that the thermal distribution under the heat sources is accurately predicted by the analytical model with a maximum error of 6 °C. The experiment validation process is also implemented and will be illustrated in the final paper. In summary, a maximum error of 15 % is achieved for all test points.

This work was supported by the Office of Naval Research (ONR), with grant number N00014-16-1-2956. DCN: 43-9044-22

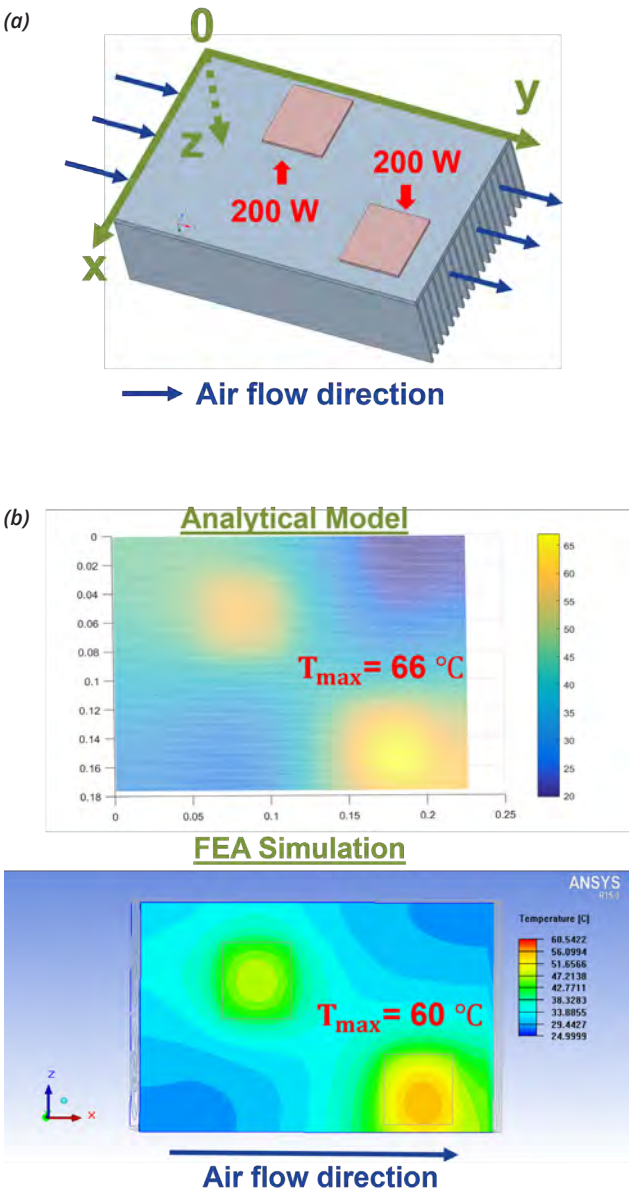


Fig. 1. Temperature distribution across heat sink top surface with two heat sources. (a) Heat sink model. (b) Compare temperature distribution prediction across heat sink top surface between analytical thermal model and FEA simulation.

A Novel Stray-Inductance-Based Current Sensor for Switching Current Measurement

Since the SiC MOSFET is designed with a small size, the thermal mass is much smaller compared to the Si-based MOSFET. Under the short-circuit condition, the temperature rise in the SiC MOSFET is much faster, which leads to damage of the power modules. Therefore, it is crucial to have fast current sensing to trigger the protection under the short-circuit fault. There have been several simple current sensor schemes, which are based on the stray inductance of the power module. These methods eliminate the need to use the Rogowski coil, which consumes a large space of the PCB circuit. However, due to the inaccuracy under temperature variation, the function of these current sensors is mostly limited to protection.

This work proposes a stray-inductance-based current sensor scheme, which provides much-improved output compared with existing methods. First, the impact of the parasitic resistance on the current sensor is thoroughly investigated. Then, a feedback method with a fixed pole placement is proposed. The current sensor's performance is further improved by a dynamic feedback loop, which constantly monitors the change in the parasitic resistance and updates the pole accordingly. As a result, the moving zero caused by the parasitic resistance variation is cancelled regardless of the temperature. The proposed method only requires information of the switching current, which helps simplify the design process.

The proposed current sensor scheme, which includes an integration circuit, a low-pass filter, and a dynamic feedback loop, is presented in Fig. 1. Based on the sensing current waveform, the change in the wire bond resistance between the Kelvin source and power source terminals is calculated. Then, the correction factor, denoted by β, is continuously updated to the feedback loop in Fig. 1 to mitigate the error in the current sensor's output caused by the temperature variation. Fig. 2 presents the switching current waveform with the proposed current sensor versus that measured by a commercial Rogowski coil probe, under a DPT test. There is good agreement between the two characteristics in the on-time interval of the switching device, including the short transient time shown in the magnified area. This indicates that the measurement current with the proposed sensor can be used for both protection and control purposes.

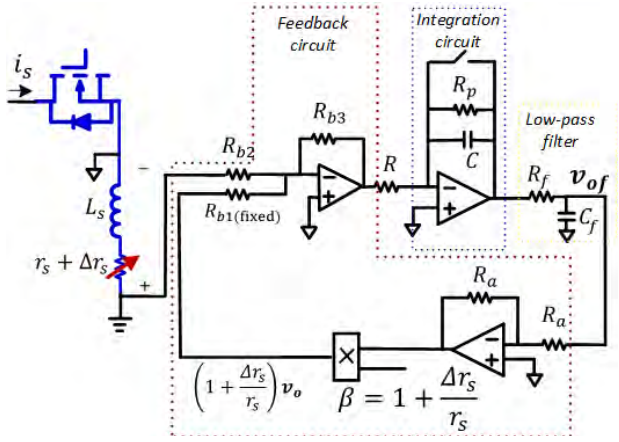


Fig. 1. Proposed current sensor scheme.

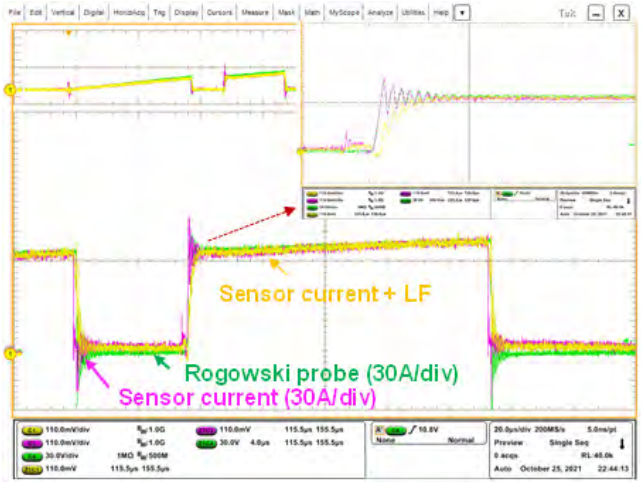


Fig. 2. Sensing current waveform with the proposed sensor and the Rogowski coil at steady state.

Three-Phase Multi-Level Inverter Topology Evaluation

To replace conventional non-electrical systems with electrical systems in the aircraft, the concept of More Electric Aircraft (MEA) has been raised. Most of these systems are power drives, normally composed of an inverter, EMC filters, and a motor. Increasing power density is one of the most important challenges and goals in power electronics applications in transportation. Multilevel topologies are identified as promising approaches in motor drive systems, owing to the decrease of switching frequency and the reduction of input and output filter size. However, the increased voltage level also requires more devices and floating capacitors. This work presents the comparison results based on a 1.1 kV/50 kVA three-phase, multi-level inverter, from the loss and volume point of view, seeking to evaluate the performance of different topologies and voltage levels.

Three topologies shown in Fig. 1 are selected. Flying capacitors (FC) are widely adopted in high-voltage and medium-voltage applications. Recently it is also proposed in lower PV applications and can achieve high efficiency due to the adoption of low-voltage GaN devices. However, the power density is sacrificed with the increasing number of floating capacitors. Therefore, some hybrid topologies seven-level stacked multi-cell (SMC) and active neutral-point converters (ANPC) can also be compared. Evaluation starts from three-level to nine-level. Loss evaluation includes the semiconductor and floating capacitors. Both GaN devices and SiC devices are considered to achieve the best performance. Volume evaluation includes the cooling system and floating capacitors. For the EMC filters, an initial comparison of noise spectrums of common-mode voltage and differential-mode current is simulated of each topology to avoid numerous filter designs and comparisons. All of these compared parameters are related to the carrier frequency and modulation method of each topology. For a fair comparison, carrier frequencies under the same THD values are extracted, as shown in Fig. 2. It can be observed that for FC, from three-level to five-level, the frequency decreases the most. While for the other two hybrid topologies, the frequency decreases the most from five-level to seven-level.

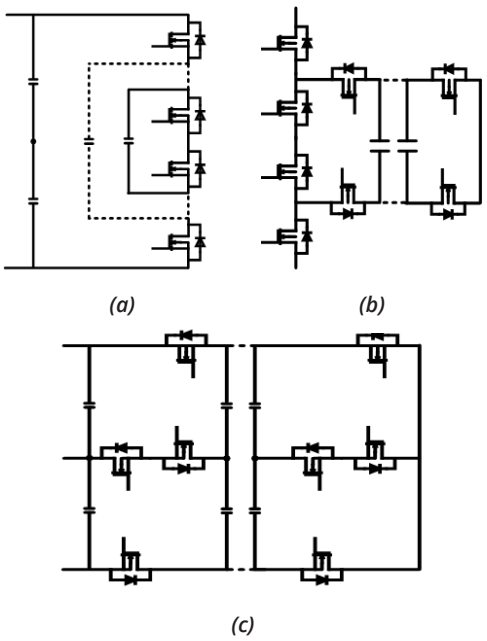


Fig. 1. Bridge leg topologies in evaluation, (a) FC, (b) ANPC, and (c) SMC.

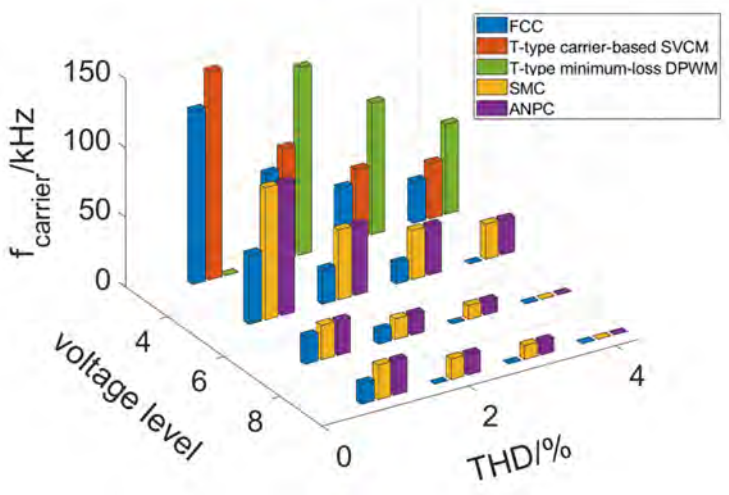


Fig. 2. Carrier frequency extracted based on same THD under different topologies and voltage level.

Electrical Insulation Design and Qualification of a SiC-Based Generator-Rectifier Unit (GRU) for High-Altitude Operation

The aerospace industry is in the process of moving towards a more electric aircraft by replacing the traditional hydraulic and mechanical systems with high-efficiency electrical systems to reduce system weight, cost, and fuel consumption. The main generator rectifier unit (GRU) forms the heart of the power processing system in the aircraft, feeding all downstream loads. The low air pressure environment associated with the cruising altitudes (up to 15,200 m) reduces the breakdown electric field (E-field) strength of air. This increases the risk of surface discharges within the GRU resulting in consequences ranging from insulation lifetime degradation to complete insulation breakdown and catastrophic system failures.

Printed circuit boards (PCBs) are ideal for integration of electronic components in low-profile, high-power density assemblies, where precise E-field control techniques can be easily implemented to achieve sufficient PD performance, even under the specified altitude conditions. With the knowledge of Paschen's curves for air, it is possible to deduce the breakdown E-field of air for varying conductor clearances at different altitude conditions to directly guide the GRU design.

In this work, the GRU in question is designed and qualified for PD-free operation at 15,200 m altitude (11.6 kPa). Finite element analysis simulations are used to optimize the design of the GRU PCBs and their assemblies to constrain the surface E-field (E_{air} in air) of the system under a predetermined limit ($E_{air\text{-}limit} \leq 300$ V/mm). This is chosen based on the Paschen curves to eliminate PD occurrences under nominal conditions. The three main GRU component assemblies, the dc bus, the CM choke, and the gate driver, are shown in Fig. 1. A high-altitude PD test bed is designed for GRU insulation qualification (Fig. 2(a)). PD experimental results of individual GRU components and their assemblies are presented in Fig. 2(b) showing satisfactory PDIV values (> 1.4 times the working voltage) at the specified air pressure conditions.

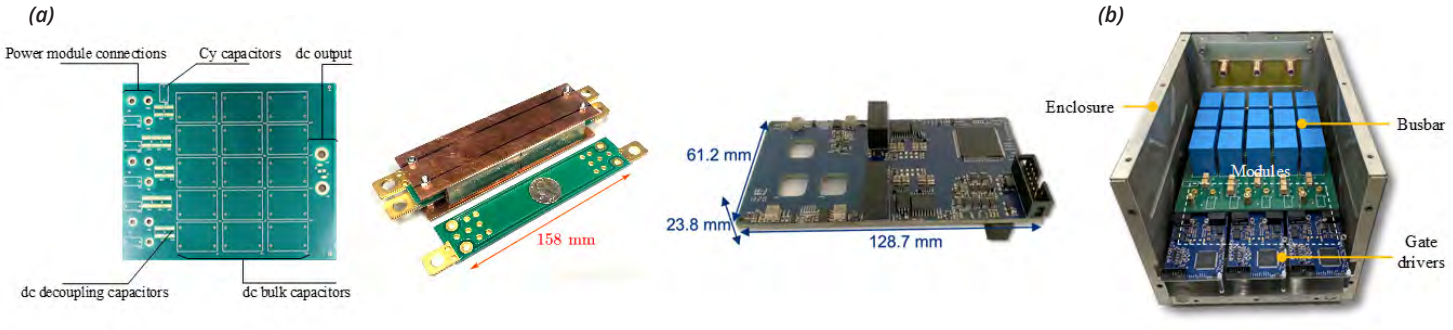


Fig. 1. (a) GRU components: dc bus (left), dc CM choke (middle), gate driver (right). (b) Full system assembly.

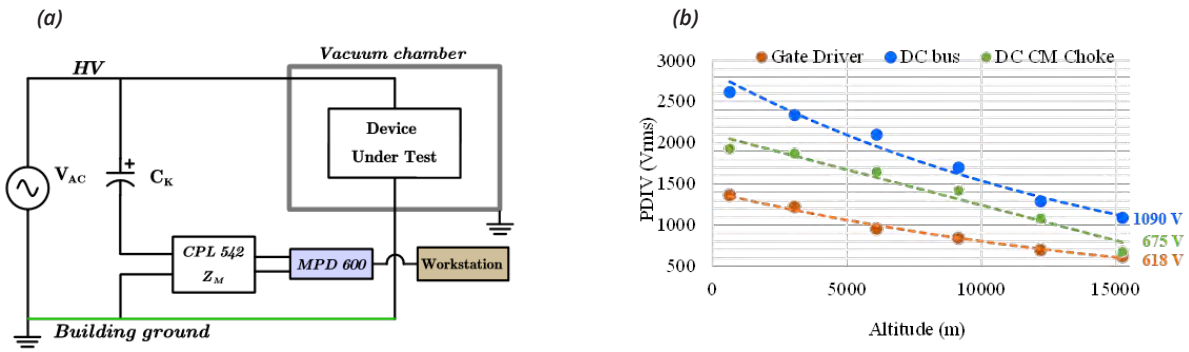


Fig. 2. (a) High-altitude PD test bed. (b) GRU components PDIV summary for different altitude settings.

High-Density EMI Filter for a More Electric Aircraft (MEA)-Based DC-Fed Motor Drive

This work presents a highly compact multi-turn integrated Differential Mode (DM) and Common Mode (CM) dc and common mode ac EMI filters for a high-power inverter (200 kW, 300 A) used in aerospace applications, as shown in Fig. 1. Design challenges pertaining to high-current, high-altitude, and strict weight requirement are tackled. Key aspects, such as the impact of load and converter multi-loop resonances, E-field, and form factor on the design are discussed. Consequently, a PCB-based multi-turn solution is adopted featuring an ultra-low EPC and low E-field. The design is based on a masked impedance approach. The ac CM Filter is used to damp/control resonance due to the motor CM impedance seen on the dc side, while the dc CM filter provides additional attenuation for mid- and high-frequency CM noise. The DM filter design follows a conventional design process while considering commutation loop RLC parameters for the three-level structure (derived from FEA simulations).

An additional feature includes an embedded AMR current sensor for dc side current sensing, which is useful for inverter prognostics. The specific weight of the proposed filters is 58.8 kW/kg, while for the converter (shown in Fig. 2), it is approximately 20 kW/kg. A 3L-T type inverter is used for the demonstration of the filter performance with DO-160 standard as the dc side EMI constraint.

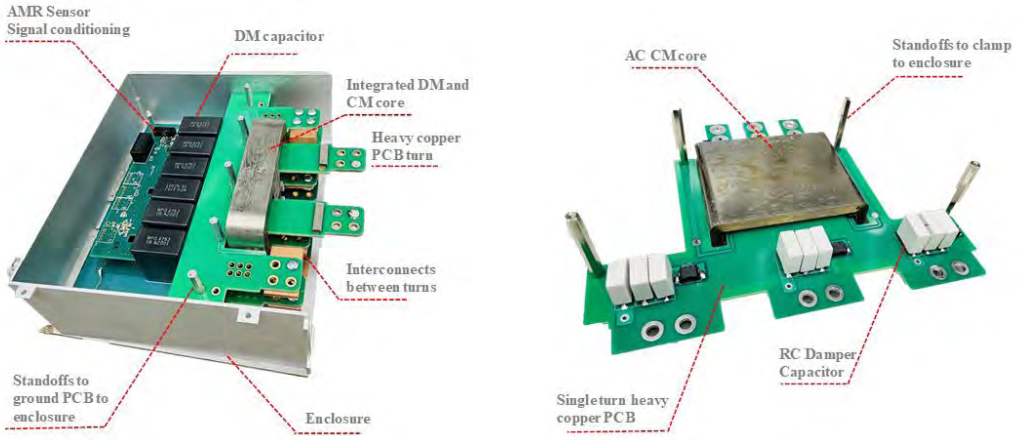


Fig. 1. Dc and ac EMI Filter.

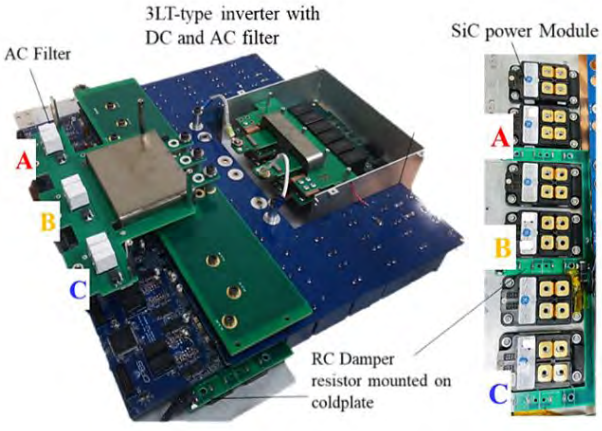


Fig. 2. 3LT-Type inverter with integrated filters (illustration of RC damper mounted next to module on the coldplate).

Input Impedance Characterization of a Single-Phase PFC in D-Q Frame

Small-signal stability analysis in a balanced three-phase system can be performed by extracting source and load impedance in a synchronous rotating frame (d-q) and using Generalized Nyquist Criterion (GNC). For a single-phase system or three-phase unbalance system, like a data center power system, the derivation of input impedance and stability analysis in the d-q frame is not straightforward because of the system's inherent time-variant condition due to the single-phase and unbalanced load. Existing approaches to analyze the stability of such a system are based on harmonics linearization in the stationary frame or by creating virtual frames and transforming the constructed three-phase system to another rotating frame. Inspired by the latter method, this work models and characterizes the input impedance of a single-phase, totem-pole, power-factor-correction (PFC) converter in d-q frame based on the virtual frames method, which is a vital step towards stability analysis of data power systems. This work also analyzes the different control loops' impact on the shaping of the PFC d-q impedance, which can provide insights for design-oriented stability analysis. The derived impedance model is verified with experimental measurement.

A totem-pole topology PFC is studied; the circuit of which is shown in Fig. 1. Its controller contains a proportional-resonant (PR)-based current controller, a proportional-integral (PI)-based dc voltage controller, and a phase tracking unit, by scaling the input voltage by a gain of 1/|Vac| and an ac voltage feedforward control.

Fig. 2 shows the measured impedance and the modeling results in the d-q frame in 1 Hz~1 kHz. The modeling results match well with the experimental results except for around 120 Hz. This is due to the presence of the dc-bus double line-frequency ripples that induce the ac side third harmonics through frequency coupling, thus mixing the small-signal response and operating point response. The mismatch in Z_{dq} and Z_{qd} mainly results from the system error because the off-diagonal terms are too small. Another important point is that this mismatch is also not critical because the PFC converter impedance is diagonally dominant, and the off-diagonal terms have a negligible effect on the minor loop gain construction.

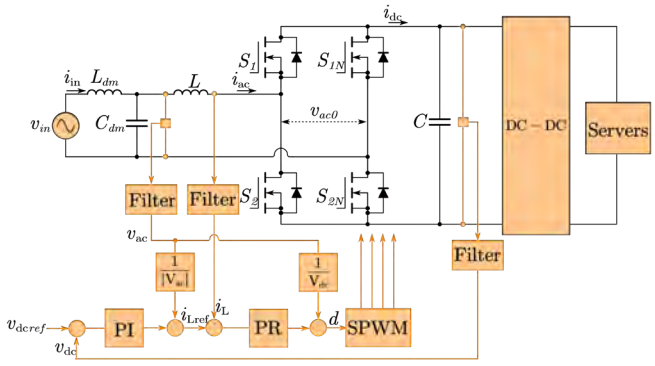


Fig. 1. Single-phase totem-pole PFC with current and voltage control.

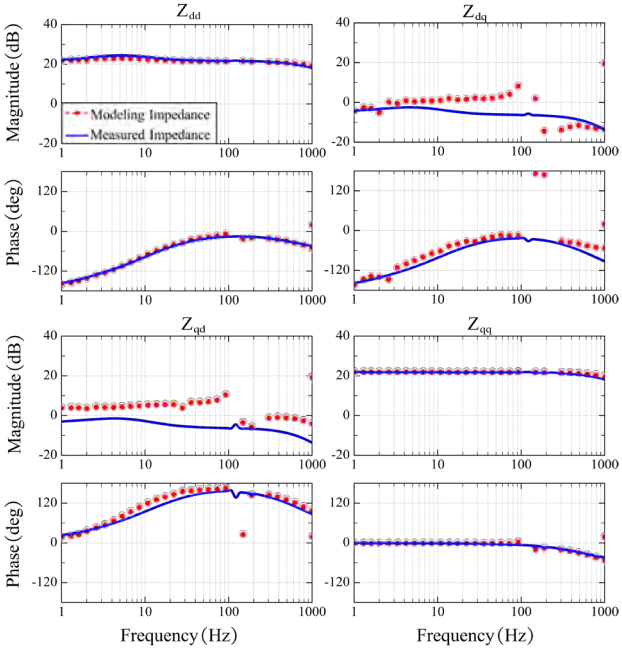


Fig. 2. PFC impedance measurement and modeling results.

Fault Characteristics Analysis on 56-Bus Distribution System With Penetration of Utility-Scale PV Generation

With distribution systems' dramatic transition from centralized fossil-based generations to distributed energy resources (DERs), system fault characteristics, especially the fault current profile, will experience some major changes. These changes will likely produce some undesirable technical issues in the area of system protective relay. The existing overcurrent relay scheme, which is designed to operate under radial power flow conditions, might fail to operate correctly under a high DER penetration level. To avoid DERs' negative impact on system safety, it is necessary to study fault characteristics changes and possible relay issues caused by the DER interconnection.

In recent years, a few literatures focused on the impact of large-scale inverter-based photovotaic (PV) generations to overcurrent relays, yet restricted to fault responses under the PV inverter grid following control. This work focuses on the fault analysis of a 56-bus distribution feeder interfacing with a utility-scale PV farm, with the inverter control strategy in compliance with the IEEE Standard 1547-2018. The feeder testbed, shown in Fig.1, is implemented in PLECS. The fault responses under both the inverter's grid-following and grid-forming control are discussed. The system fault current profile is analyzed under various scenarios, including both three-phase and single-phase faults, under different fault severity, and at different locations.

Under grid-following control, the PV inverter outer loops lose their effect. The current loop saturates, thus has a rather limited contribution on the system fault current. During a PV upstream fault, the PV farm current contribution causes an increase of the fault downstream current instead of a decrease; the fault downstream overcurrent relays are likely to trip mistakenly, as illustrated in Fig. 2. Under grid-forming control, the failure of the inverter drooping mechanism leads to current saturation under balanced faults and severe current signals distortion under unbalanced faults.

This work assesses the impacts of the utility-scale PV farm's interconnection to the system fault characteritics, as well as stated potential issues in overcurrent relay under high PV penetration. The fault current profile changes can lead to relay desensitization and false tripping, which will require revising the relay settings.

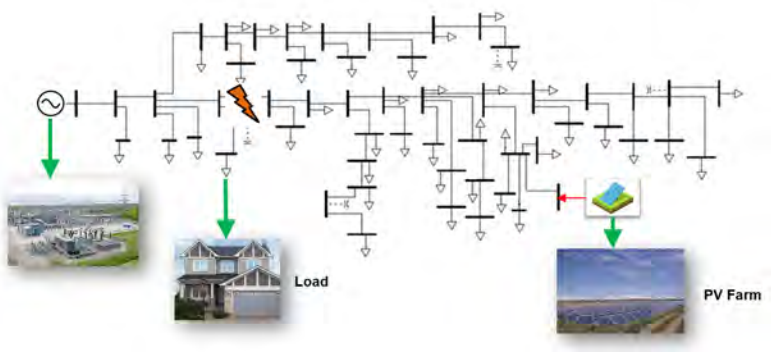


Fig. 1. Topology of 56 bus distribution system.

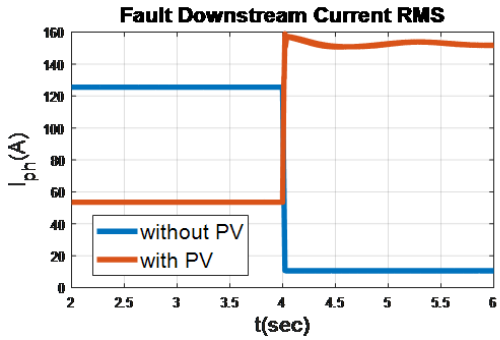


Fig. 2. Comparison of with/without PV integration at fault downstream location.

Active Gate Drivers for EMI and dv/dt Control

This work is a study on the impact of using active gate drivers, which provide a variable drive voltage to the switching device. This will give a better understanding of the advantages and drawbacks seen with the introduction of multiple drive voltage variations. The primary areas of focus are the control of the drain node dv/dt, switching loss, and gate terminal current. One benefit seen from controlling the drain node dv/dt is that with an active gate driver and lower gate resistance, the same slew rate can be achieved as with a conventional driver and much higher gate resistance. This is simultaneously achieved with a lower switching loss in the active gate driver. Fig. 1 depicts both the conventional gate driver voltage profile (in dashed red), and an approach used by active gate drivers for dv/dt control. This also illustrates the two separate control regions available for the active gate driver to impact.

When looking at reduction in dv/dt, simulations are performed using the C2M0080120D CREE SiC MOSFET. From these simulations the intermediate step voltage and duration of this voltage are adjusted. The results are plotted in Fig. 2, which shows the dv/dt being reduced from ~110 V/ns to ~ 30 V/ns (with an 8 V applied step).

This represents a reduction of almost 73 %. These results show a noticeable range in dv/dt reduction with an active driver. Through the introduction of additional intermediate voltage steps, the results do not show any noticeable improvement in this area.

From the perspective of loss, Fig. 2 shows a clear trend; as the step duration increases, the losses also increase until a point where the dv/dt no longer is reduced. Then, the loss remains constant.

A final improvement noted in initial simulations is with the peak gate current during the drain voltage fall region. With the introduction of additional voltage steps in the gate driver voltage that achieve the same dv/dt, the peak gate current in this region is reduced, and the current stayed at a more constant value.

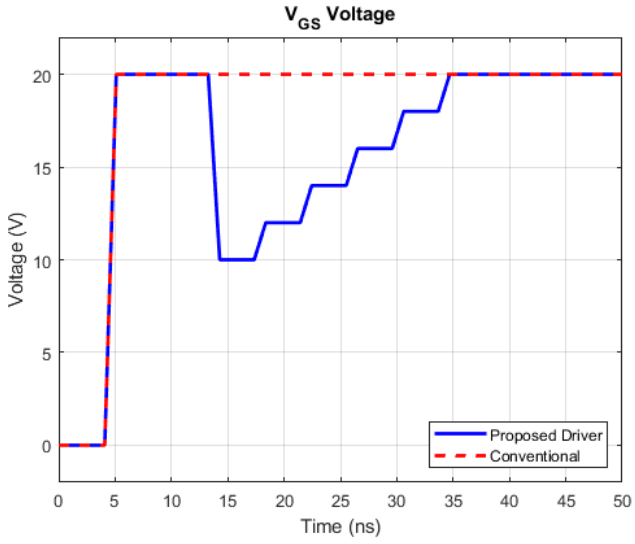


Fig. 1. Active gate driver turn-on waveform.

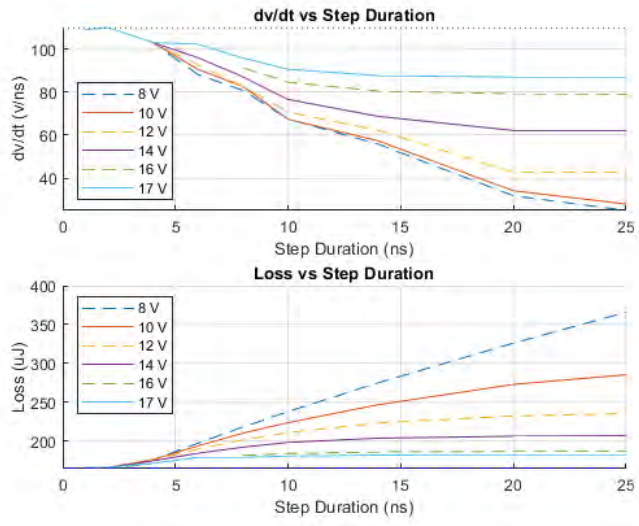


Fig. 2. Single-voltage step impact as step duration is increased.

PCB Technology Comparison Enabling a 900 V SiC MOSFET Half-Bridge Design for Automotive Traction Inverters

Conventional automotive traction inverters for 800 V systems are designed with 1.2 kV SiC MOSFETs. The 1.2 kV power devices allow for high overshoot voltages during switching transients but experience a high on-state resistance due to the die's thick drift layer region. This work proposes the usage of 900 V SiC MOSFETs for 800 V automotive traction inverter applications. The proposed half-bridge design combines discrete power semiconductors and the dc-link capacitor on one PCB. Three different PCB technologies are compared based on their suitability for the inverter application. An 800 V half-bridge prototype is designed and simulated. Simulation results are provided and show an overshoot voltage of 33 V at maximum load conditions.

The three PCB technologies compared are a heavy copper PCB with copper inlays for better thermal conductivity from junction to heat sink, a ceramic inlay PCB, and an embedded die PCB. The PCB technologies are compared based on the thermal conductivity path from junction to heat sink, the high current capability, and the switching transient overshoot voltage influenced by current commutation loop stray inductance.

Finite element analysis is carried out in Ansys Icepack to analyze the thermal resistance path from junction to heat sink. The junction temperature must not exceed 150 °C. The results indicate that the junction temperature exceeds the threshold for the copper inlay PCB. The ceramic inlay and embedded die PCB have a low thermal resistance, allowing the junction temperature to stay below 150 °C.

The current density should not exceed 5 A/mm^2 to allow for passive cooling of the dc-link capacitor. Finite element analysis shows a current density of 43.3 A/mm^2 due to thin copper layers. The embedded die PCB has a current density of 4.3 A/mm^2. Thus, switching transient overshoot voltage is further analyzed. The PCB parasitics are derived from Ansys Q3D simulations and imported into SPICE simulations. The resulting switching transient is depicted in Fig. 1. The overshoot voltage is 33 V at a current slope of 5.7 A/µs. Thus, the maximum drain-source voltage does not exceed the break down voltage of the 900 V SiC MOSFET.

The comparison shows that an embedded die PCB is suited for using 900 V SiC MOSFETs for 800 V automotive traction inverter applications. Further work includes testing the thermal conductivity and switching transients on a prototype.

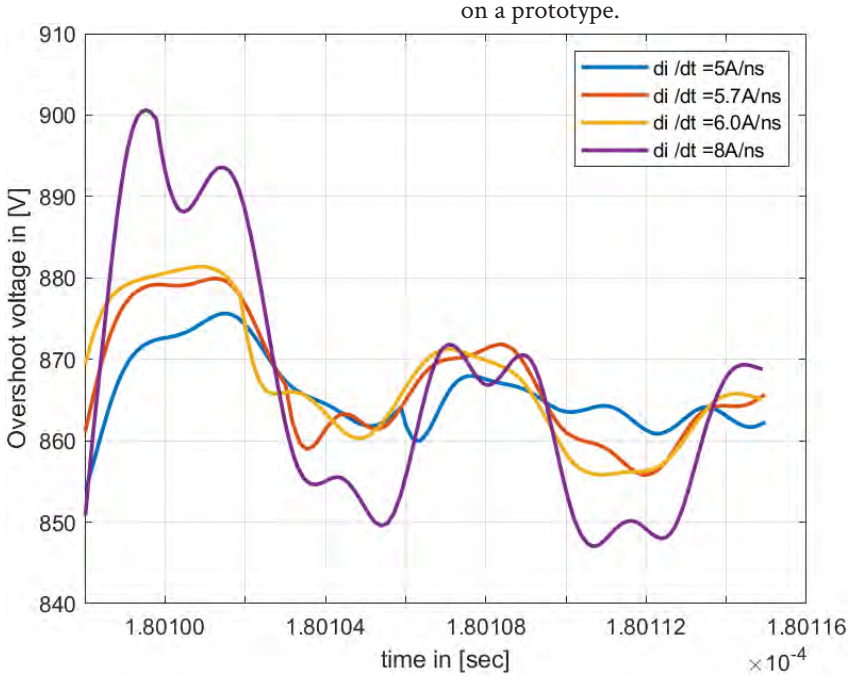


Fig.1. Turn-off switching transient overshoot voltage.

Fault Monitoring of Photovoltaics System Using Impedance Measurement

The solar photovoltaics (PV) panel has seen rapid growth for many years and is expected to grow further with the continuous decrease in the cost of technologies. Energy from the PV panel can be fetched and provided to the grid through a dc-dc converter and dc-ac inverter. PV panels are susceptible to a variety of faults, such as a hot spot fault, line to line fault, open circuit fault, diode fault, ground fault, and many more. The nature of the fault can be due to cabling, modules, converter, inverter, and protection. A PV panel comprises multiple PV cells; each PV cell has its series and parallel resistances and parallel capacitance. The PV system operation varies by changes in voltage biasing, illumination, and temperature.

Using power converters and inverters, a small signal is injected into the PV panel, as shown in Fig. 1, and the impedance of the PV panel is computed. Due to mismatching of electrical characteristics among PV cells, the PV string operates at a suboptimal point. The cause of mismatching can be manufacturing error, PV cell shading, or cell degradation. Partial shading of a PV cell can lead to the cell being operated in reverse bias condition. Thus, PV cells will be sinking power rather than the source, leading to an increase in cell temperature. High PV cell temperature will eventually lead to cell degradation and create a hot spot (HS) in a PV module. A Simulink-based model is simulated with 20 monocrystalline PV cells under standard illumination of 1000 W/m^2 and temperature of 25 °C. With fault conditions, the illumination on the faulty PV cell is 0 W/m^2 and temperature of 75 °C. The results are compared to experimental results. Under the low-frequency region, the magnitude of impedance for faulty PV cells is higher than the normal PV cells. For the mid-frequency region, the phase of impedance for the faulty PV cell is higher than the normal PV cell, as shown in Fig. 2.

With the impedance measurement tool, changes in impedance are seen for PV cells under fault scenarios. Equipment-based hardware results for impedance measurement of a PV cell matches well with the model, and the general trends are consistent.

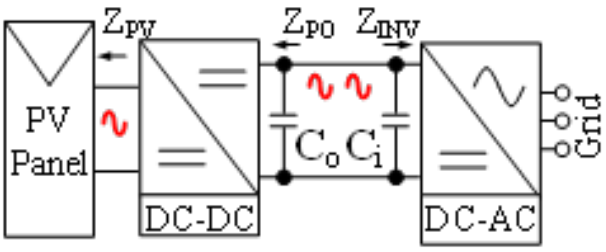


Fig. 1. Small signal Injection to PV panel.

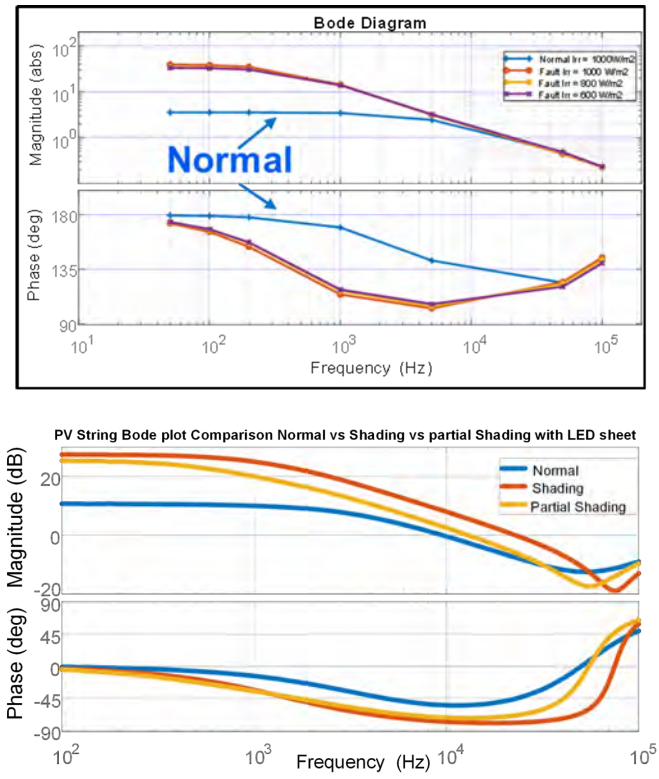


Fig. 2. Impedance plot comparison between simulation and experimental results.

Design and Control of a High-Power Wide-Gain-Range LLC Resonant Converter

In LLC converters with regulation requirements, usually there are two constraints that should be addressed in the design procedure: 1) select appropriate magnetizing inductance L_m and deadtime t_d according to selected power switches to realize zero voltage switching (ZVS) at DCX operation ($f_s \approx f_o$) to achieve high efficiency, and 2) to satisfy the gain requirement within a practical switching frequency range.

However, in high-power wide-gain-range applications, there is no ready solution to meet both constraints. Thus, multi-control methods are combined to solve the problem.

In general, the converter will operate in DCX mode when the input voltage is in the nominal voltage range to maximize the peak efficiency, operate in Boost mode when the input voltage is lower than nominal values to boost gain, and operate in PWM mode when the input voltage is higher than nominal values to reduce switching frequency and device losses.

Fig. 1 shows the topology and key waveforms of three-mode operations. 3D gain curves and operating path are shown in Fig. 2.

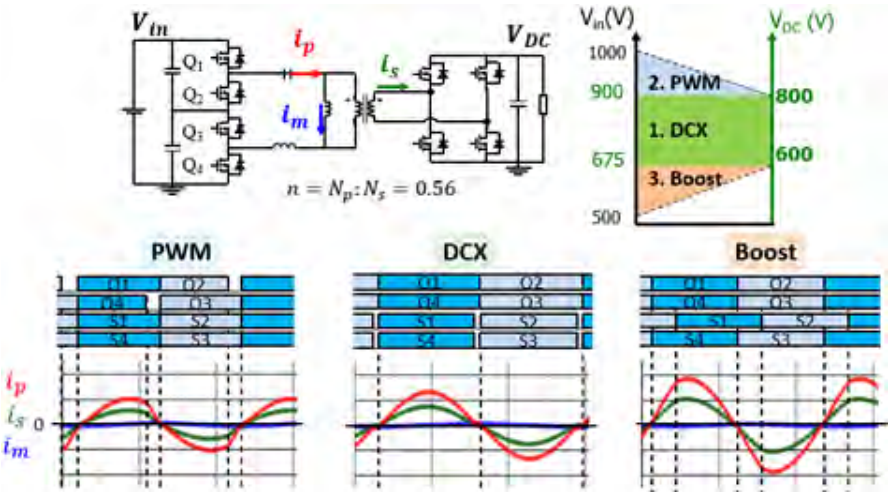


Fig. 1. Circuit topology and waveforms of three-mode operations.

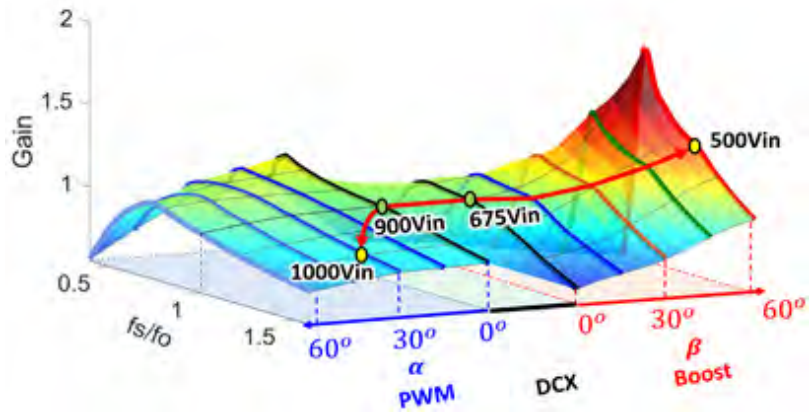


Fig. 2. 3D gain curves and operating path.

Partial Fluctuating Power Control of Resonant Converter for Solid-State Transformer

Solid-state transformers (SSTs) are becoming an exciting topic for their ability to directly step medium voltage down to low voltage (e.g., 400 V or 1 kV) with minimized power conversion stages, which allows for higher overall efficiency in the smart grid system. A two-stage SST system with a cascade H-bridge (CHB) as the first stage and dc-dc stage as the second stage is one of the most popular architectures. In the system, the CHB steps down the medium voltage while the dc-dc handles the isolation and high-voltage insulation. Due to the CHB characteristics, double-line-frequency power must be introduced into the SST system. To eliminate the impact of fluctuating power, two control methods — constant power control and fluctuating power control — are proposed by different researchers.

In this paper, the benefits and drawbacks of these two methods are compared under the same design parameters. The bus capacitor is found to be the most critical component in the system from the standpoint of loss and size trade-offs in the two control methods. Factors that impact the loss trade-off for partial fluctuating power control are evaluated.

A method is proposed for calculating the average loss over one cycle that utilizes the proposed fluctuating power flow to predict the loss distribution. A power fluctuation of 50 % is selected as an example to illustrate the loss comparison between the partial fluctuating power and the constant power. The total efficiency has a less than 0.1 % decrease with the same device; however, a 50 % reduction in bus capacitor volume and BOM can be saved. A 15 kW-rated, 200 kHz, 1.6 kV/1.1 kV CLLC converter is developed to verify the concept, which shows 98.9 % efficiency for constant fluctuating power flow and 98.8 % for partial fluctuating power flow.

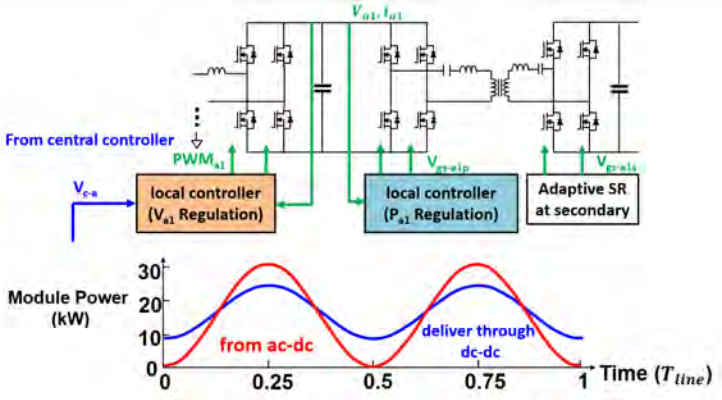


Fig. 1. Control diagram for partial fluctuating power control.

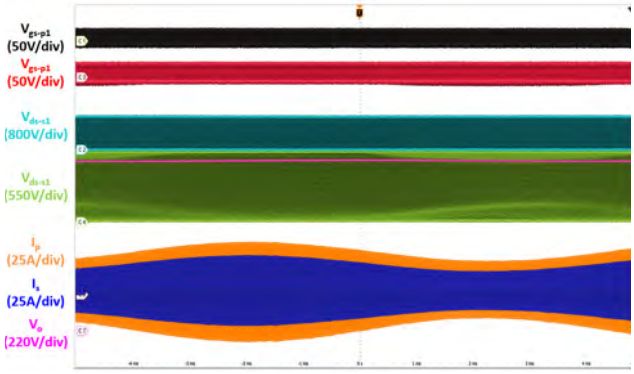


Fig. 2. Experimental waveform for fluctuating power control in a half-line cycle.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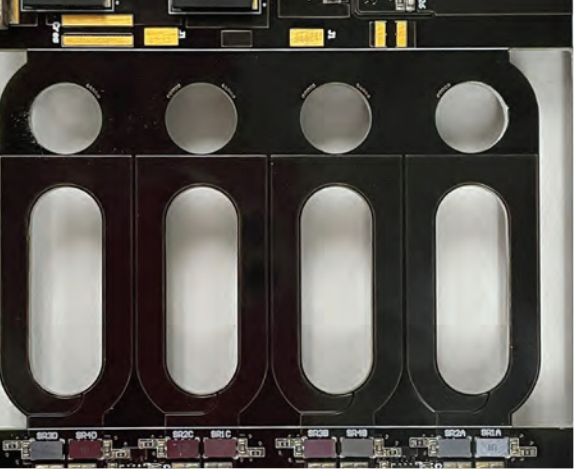

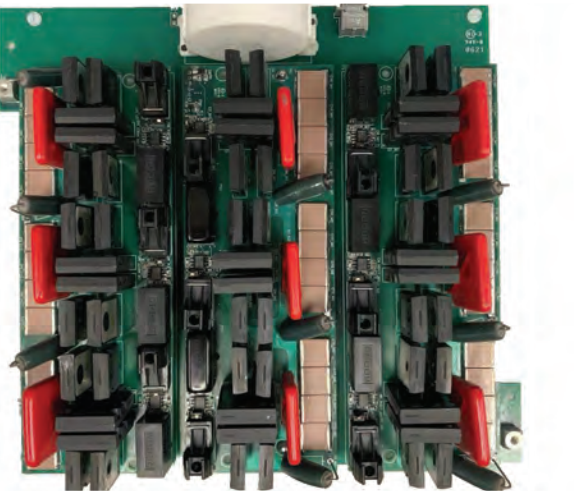

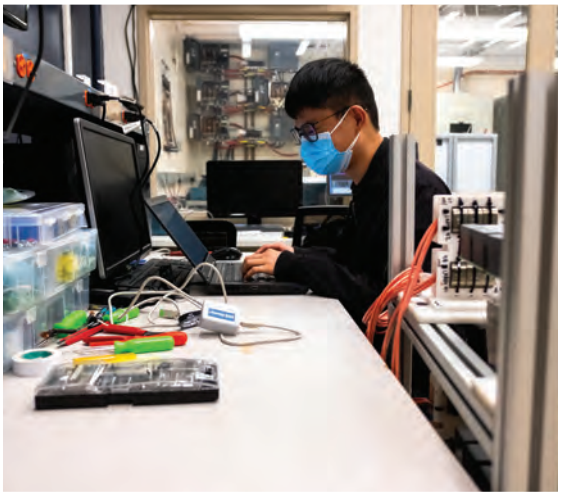

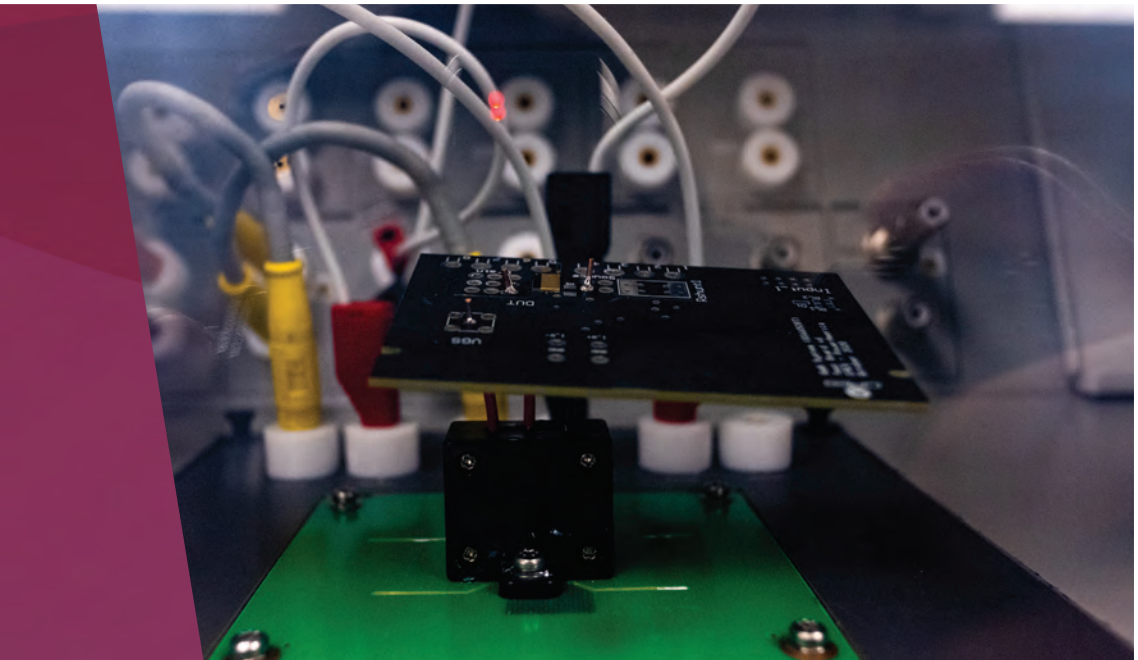

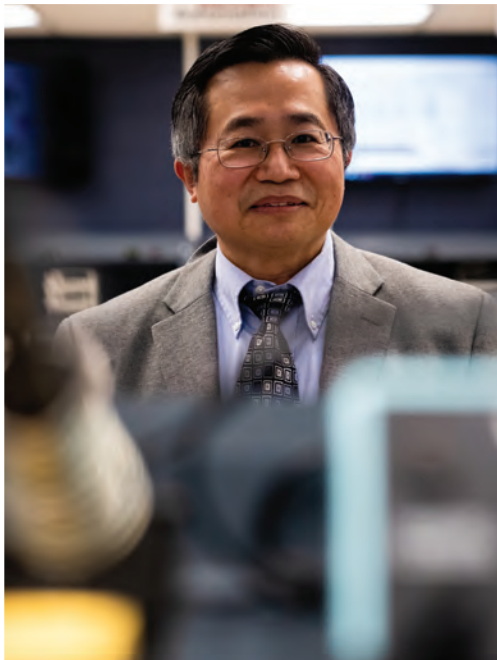

BLACKSBURG

1185 PERRY STREET
655 WHITTEMORE HALL
BLACKSBURG, VA 24061

NATIONAL CAPITAL REGION

900 N. GLEBE ROAD
ARLINGTON, VA 22203

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