Cascade Dual-Buck Inverters for Renewable Energy and Distributed Generation

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ABSTRACT

Renewable energy and distributed generation are getting more and more popular, including photovoltaic modules (PV), wind turbines, and fuel cells. The renewable energy sources need the power electronics interface to the utility grid because of different characteristics between the sources and the grid. No matter what renewable energy source is utilized, inverters are essential in the microgrid system. Thanks to flexible modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascade inverters are good candidates for utility interface of various renewable energy sources.

This dissertation proposes a new type of cascade inverters based on dual-buck topology and phase-shift control scheme. Compared to traditional cascade inverters, they have enhanced system reliability thanks to no shoot-through problems and lower switching loss with the help of using power MOSFETs. With phase-shift control, it theoretically eliminates the inherent current zero-crossing distortion of the single-unit dual-buck type inverter. In addition, phase-shift control can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency.

An asymmetrical half-cycle unipolar (AHCU) PWM technique is proposed for dual-buck full-bridge inverter. The proposed approach is to cut down the switching loss of power MOSFETs by half. At the same time, this AHCU PWM leads to current ripple

reduction, and thus reducing ripple-related loss in filter components. Therefore, the proposed PWM strategy results in significant efficiency improvement. Additionally, the AHCU PWM also compensates for the zero-crossing distortion problem of dual-buck full-bridge inverter. Several PWM techniques are analyzed and compared, including bipolar PWM, unipolar PWM and phase-shifted PWM, when applied to the proposed cascade dual-buck full-bridge inverter. It has been found out that a PWM combination technique with the use of two out of the three PWMs leads to better performance in terms of less output current ripple and harmonics, no zero-crossing distortion, and higher efficiency.

A grid-tie control system is proposed for cascade dual-buck inverter with both active and reactive power flow capability in a wide range under two types of renewable energy and distributed generation sources. Fuel cell power conditioning system (PCS) is Type I system with active power command generated by balance of plant (BOP) of each unit; and photovoltaic or wind PCS is Type II system with active power harvested by each front-end unit through maximum power point tracking (MPPT). Reactive power command is generated by distributed generation (DG) control site for both systems. Selective harmonic proportional resonant (PR) controller and admittance compensation controller are first introduced to cascade inverter grid-tie control to achieve better steady-state and dynamic performances.

To my parents

Enshu Sun and Xuehui Ren

To my sister

Penglin Sun

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Chapter 1

Introduction

1.1 Research Background

In the past two decades, renewable energy has gained tremendous attention thanks to its environmentally-friendly feature as well as its ability to offer more cost-effective options to meet the demand of electricity market. Distributed generation (DG) based on renewable energy provides power in the vicinity of loads, which reduces the loss through power transmission and improves the power quality to the loads. In addition, the DG can be utilized in a remote village or rural area where the grid is not available. It can also be used as a backup source when the grid is gone [1]-[4].

Solar power, wind power, and fuel cells [5]-[7] are widely used for distributed generation. Because the first two energy sources do not need extra fuel, the installation of photovoltaic modules (PV) and wind turbines increased at a rate of 20-40% per year in the last few years [8]-[9]. Though fuel cells have a higher fuel cost compared to solar and wind power, they are considered better for the system stability because they are not susceptible to the weather for power generation.

If DG units are powered only by intermittent energy sources, such as PV or wind, it is necessary for DG units to have the energy storage system to handle the transient

energy demands. The energy storage system can be composed of batteries, flywheels, super-capacitors, and so on [10]-[11].

Fig. 1.1 shows a renewable energy and distributed generation based microgrid configuration. The renewable energy sources need the power electronics interface to the utility grid due to the different characteristics between the sources and the grid [1], [10], [12]-[13]. For example, DG sources can be dc power (solar, fuel cell), or variable-frequency ac power (wind) while the utility grid is fixed ac 50/60Hz. From Fig. 1.1, we can see that no matter what renewable energy source is utilized, inverters are essential in this microgrid system.

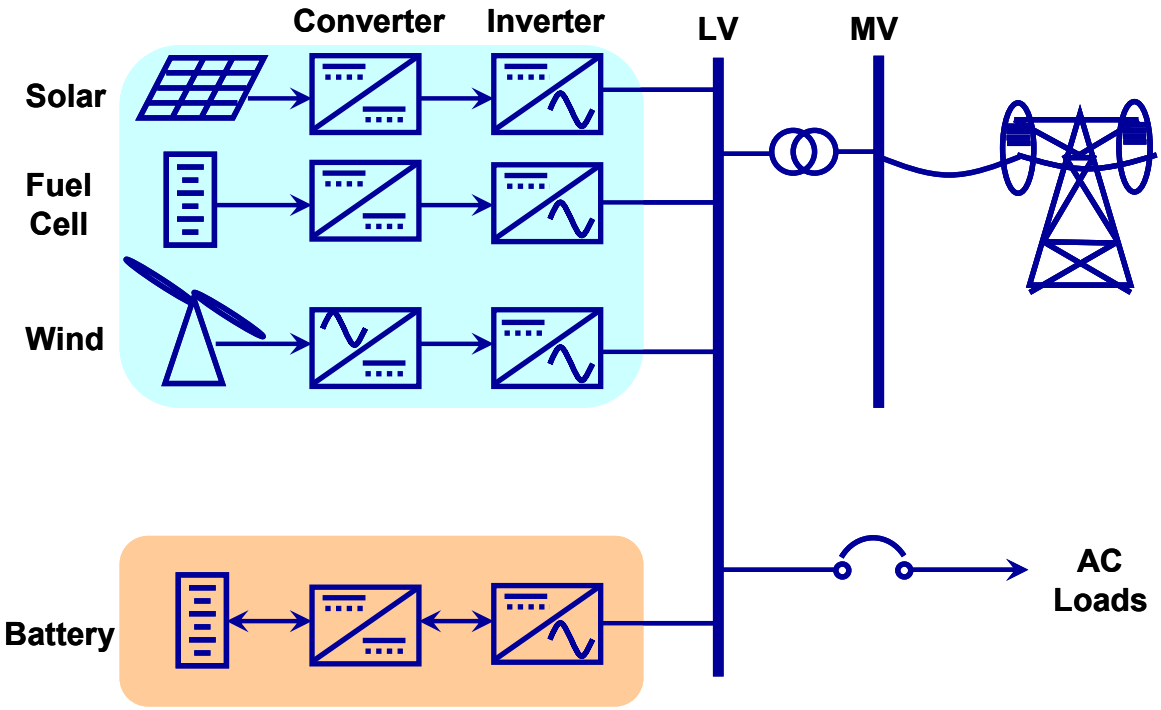


Fig. 1.1: Renewable energy and distributed generation based microgrid configuration.

Grid-tie control of renewable energy and DG systems, such as fuel cell, photovoltaics, and wind power, are important research topics nowadays. Various circuit topologies and control methods have been proposed to improve the efficiency and to enhance the performance and reliability. With flexible modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascade inverters are good candidates for low-cost utility interface of various renewable energy sources [14]-[24]. In this dissertation, a new type of cascade inverter utilizing the dual-buck type inverter cells to stack the multilevel ac output voltage is proposed for a highly reliable, high-efficiency, and potentially low cost inverter that can be used in different renewable energy and distributed generation applications.

1.2 Benefits and Limitations of Cascade H-Bridge Inverters

Among various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-clamped inverter, flying capacitor inverter and cascade H-bridge inverter [14]-[17]. Cascade inverters are with separate dc sources, and each dc source is associated with a single-phase inverter while the ac terminals of each inverter are connected in series. It was first invented by Richard H. Baker back in 1975 [77].

The cascade types of inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components, and it features the modular design concept which makes the maintenance less burdensome [14]-[20], [25]-[28]. In medium voltage AC drives application, Robicon Corporation promoted cascade H-bridge inverters and claimed numerous advantages of their products, including low voltage and current THD level and optional degrees of redundancy with electronic bypass [78]-[81]. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaics, fuel cells, battery energy storage, and electric vehicle drives, where separate dc sources naturally exist [29]-[37].

However, because most of current cascade inverters are based on a series connection of several single voltage source inverters (VSI) with two active devices in one leg, it still faces shoot-through problems, the most dominating failure of VSI.

In addition, for the hard-switched cascade inverters operating at higher dc bus voltage, it loses the benefit of using power MOSFETs as the active switching devices for

efficiency improvement and fast switching speed when they are available at certain voltage and power level.

For example, when the dc bus voltage goes up to 300V to 600V, one cannot simply adopt super-junction power MOSFETs that are rated from 600- to 950-V level, such as CoolMOS^{TM} or MDmesh^{TM} series to work at hard-switched situation like traditional cascade H-bridge inverter because of the reverse recovery issues of the body diode [38]-[42] unless soft-switching techniques are employed [43]-[45].

1.3 Characteristics of Single-Unit Dual-Buck Inverters

The standard half-bridge or full-bridge inverter is a typical voltage source inverter (VSI) with two active switches in one phase leg. It needs dead time to prevent shoot-through problems between the switches in one leg. Because of dead time effect, the output waveforms can be distorted and the equivalent transferred energy of pulse-width-modulation (PWM) is reduced. Even with added dead time, shoot-through is still the dominant failure of the circuit, especially at some fault conditions. In addition, with higher dc bus voltage operation, this standard inverter cannot simply employ power MOSFETs as the active switches due to the reverse recovery problem of the body diode of MOSFETs [38]-[42].

To utilize the benefits of power MOSFETs, such as lower switching loss, resistive conduction voltage drop, and fast switching speed that allows reduction of current ripple and the size of passive components, dual-buck half-bridge and full-bridge inverters had been proposed [46]-[50]. The dual-buck inverter typically has two buck inverters with one working at the positive half-cycle while the other one operating at the negative half-cycle. The dual-buck type inverters do not need dead time, and they totally eliminate the shoot-through concerns, thus leading to greatly enhanced system reliability. The body diode of MOSFET never conducts, and the external diodes can be independently selected to minimize switching losses.

However, one of the inherent drawbacks of single dual-buck inverters is the output current zero-crossing distortion, which will be explained in detail in chapter 2. To

overcome this disadvantage, new PWM methods need to be introduced. Even though the dual-buck inverters adopt MOSFET devices, they are still the hard-switching VSI. To further reduce the switching loss in power devices and passive filter components, new PWM schemes need to be explored. In this dissertation, several PWM methods that effectively eliminate the zero-crossing distortion and reduce the switching loss are proposed and implemented. Experimental results will be shown to prove the effectiveness of the proposed PWM methods.

1.4 Research Motivations and Objectives

Compared to cascade H-bridge inverter, the new cascade inverter should have the following several features. First of all, it should eliminate the possibility of shoot-through problems, which is the major failure of traditional voltage source inverters. It should avoid dead time to fully utilize the PWM output voltage and maximize the energy transfer to the load. In addition, the cascade inverter should employ the high-voltage power MOSFETs without the complexity of soft-switching assisting circuits to improve the system efficiency.

In order to use the promising single-unit dual-buck inverter as the building block for the cascade inverter, several issues also need to be addressed. First, the inherent zero-crossing distortion problems of the dual-buck inverters need to be solved. Second, to further cut down the switching loss and current ripple, new PWM schemes need to be explored.

The system control strategies, including standalone operation of the new cascade inverter as well as grid-tie operations for different renewable energy sources need to be developed.

With the above research motivations, the research objectives can be summarized:

1. To design and build a new cascade inverter that inherits the advantages and overcomes the disadvantages of traditional cascade H-bridge inverters.
2. To solve the zero-crossing distortion problems of single-unit dual-buck inverters.

3. To explore different PWM schemes for further reduction of the switching loss and current ripple.

4. To design and implement standalone controllers for the new cascade inverter.

5. To design and implement grid-tie control of the cascade inverter for different renewable energy and distributed generation sources with the wide-range power flow capability.

1.5 Dissertation Outline

Chapter 2 presents a new type of cascade inverter based on dual-buck topology and phase-shift control scheme. The proposed cascade dual-buck inverter with phase-shift control inherits all the merits of dual-buck type inverters and overcomes some of their drawbacks. Compared to traditional cascade inverters, it has much enhanced system reliability due to elimination of shoot-through mechanism and lower switching loss with the help of ultrafast reverse recovery diode during power MOSFETs turn-on condition. With phase-shift control, it can eliminate the inherent current zero-crossing distortion of the single-unit dual-buck type inverter. In addition, applied phase-shift control to cascade inverters can greatly reduce the ripple current and cut down the size of passive components with a higher equivalent switching frequency. A cascade dual-buck inverter has been designed and tested to demonstrate the feasibility and advantages of the system by comparing single-unit dual-buck inverter, 2-unit and 3-unit cascade dual-buck inverters at the same 1kW, 120V AC output conditions.

Chapter 3 presents an asymmetrical half-cycle unipolar (AHCU) PWM technique for dual-buck full-bridge inverter. The proposed approach is to cut down the switching loss of power MOSFETs to half by maintaining one active switch without switching during half-cycle of fundamental frequency of inverter output current. At the same time, this AHCU PWM leads to current ripple reduction, and thus reducing ripple-related loss in filter components of the inverter. Therefore, the proposed PWM strategy results in significant efficiency improvement. Additionally, the unipolar PWM also compensates for the zero-crossing distortion problem of dual-buck full-bridge inverter to a great degree,

practically eliminating the zero-crossing distortion found in the ordinary PWM operated dual-buck inverters. Detailed analysis and implementation of the AHCU PWM technique were performed. A 2kW, 240V ac output dual-buck full-bridge inverter prototype was designed and tested under both traditional bipolar SPWM and this unipolar PWM by using digital signal processor. Experimental results indicated that this AHCU PWM technique increased the inverter efficiency by 0.6% and greatly improved the zero-crossing distortion at wide load range conditions.

In chapter 3, several PWM techniques are analyzed and compared, including bipolar PWM, unipolar PWM and phase-shifted PWM that are applied to the proposed cascade dual-buck full-bridge inverter. It has been found out that a PWM combination technique with the use of two out of the three PWMs mentioned above leads to better performance of the cascade dual-buck full-bridge inverter in terms of less output current ripple and harmonics, no zero-crossing distortion, and higher efficiency. A prototype of the proposed inverter has been built and tested to verify the feasibility and effectiveness of the topology and different PWM techniques.

Chapter 4 presents a grid-tie control system for cascade dual-buck inverter with both active and reactive power flow capability in a wide range under two types of renewable energy and distributed generation sources. Fuel cell power conditioning system (PCS) is Type I system with active power command generated by balance of plant (BOP) of each unit; and photovoltaic or wind PCS is Type II system with active power harvested by each front-end unit through maximum power point tracking (MPPT). Reactive power command is generated by distributed generation (DG) control site for both systems. Selective harmonic proportional resonant (PR) controller and admittance compensation

controller are first introduced to cascade inverter grid-tie control to achieve better steady-state and dynamic performance. Detailed analysis and derivation of both control systems were conducted. A 1kVA cascade dual-buck inverter system was designed and interfaced to 120V, 60Hz grid to verify the control strategy. Pure active power, pure reactive power and mixed power flow with leading and lagging angles were fully tested under steady-state and command-dynamic conditions for both systems. The experimental results proved the effectiveness of the designed grid-tie control for both systems.

Chapter 5 comes to the conclusion, discusses the future work and lists the publications.

Chapter 2

Cascade Dual-Buck Inverter with Phase-Shift Control

2.1 Introduction

Among various multilevel voltage-source inverters, the most commonly used and commercially available ones are the neutral-point-clamped inverter, flying capacitor inverter and cascade H-bridge inverter [14]-[17]. The cascade types of inverters are capable of reaching higher output voltage level by using commercially standard lower voltage devices and components, and it features the modular design concept which makes the maintenance less burdensome [14]-[20], [25]-[28]. The cascade inverters are well suited for utility interface of various renewable energy sources, such as photovoltaics, fuel cells, battery energy storage, and electric vehicle drives, where separate dc sources naturally exist [29]-[37]. However, because most of current cascade inverters are based on a series connection of several single VSIs with two active devices in one leg, it still faces shoot-through problems, the most dominating failure of VSI. In addition, for the hard-switched cascade inverters operating at higher dc bus voltage, it loses the benefit of using

power MOSFETs as the active switching devices for efficiency improvement and fast switching speed when they are available at certain voltage and power level. For example, when the cell dc bus voltage goes up to 300V to 600V, one cannot simply adopt the super-junction power MOSFETs such as CoolMOS^{TM} and MDmesh^{TM} that are rated 600- to 900-V to work under hard-switched condition like the traditional cascade H-bridge inverter because of the reverse recovery issues of the body diode [38]-[42] unless soft-switching techniques are employed [43]-[45].

This chapter proposed a new cascade dual-buck inverter based on single dual-buck inverter topology to better address the issues mentioned above. The dual-buck type inverters are still VSI, but with the unique topology and operation, it does not have the shoot-through worries, which leads to greatly enhanced reliability [46]-[50]. Without shoot-through problem in each building block, the cascade dual-buck inverter much improved system reliability as compared to other cascade inverters. In addition, the cascade dual-buck inverter does not have the dead time related issues of conventional VSI based cascade inverters, which can easily push the duty cycle to the theoretical limit and fully transfers the energy to load through total PWM. In the meantime, the cascade dual-buck inverter can be hard-switched while utilizing the benefits of power MOSFETs at certain power level.

Phase-shift control is widely used for cascade inverters because it is easy to implement with digital controllers and it equivalently increases the switching frequency by the number of times of cascade units, which reduces the output voltage and current ripple [51]-[53]. For the proposed cascade dual-buck inverter, phase-shift control is adopted. Besides the common benefits, it solves the fundamental zero-crossing distortion problem

in the single dual-buck inverters. The detailed zero-crossing elimination mechanism will be explained in chapter 2.3.

The chapter first shows different topologies of the proposed cascade dual-buck inverters and their operation principles. This chapter takes single-phase cascade dual-buck half-bridge inverter as the analytical and design subject to demonstrate the feasibility and advantages of cascade dual-buck inverter. The phase-shift control scheme was analyzed by comparing single-unit dual-buck inverter and 2-unit cascade dual-buck inverter. The closed-loop control for cascade dual-buck inverter was designed and implemented. A 1kW, 120VAC output cascade dual-buck inverter system has been built to validate the proposed topology and control by comparative experimental tests of single-unit dual-buck inverter, 2-unit and 3-unit cascade dual-buck inverters.

2.2 Topology and Operation Principle

The single-unit dual-buck inverter has two basic forms, dual-buck half-bridge inverter [46], [48] and dual-buck full-bridge inverter [47]. The proposed cascade dual-buck inverter has two types accordingly: cascade dual-buck half-bridge inverter, shown in Fig. 2.1, and cascade dual-buck full-bridge inverter, shown in Fig. 2.3. This chapter will focus on the analysis, design and test of the cascade dual-buck half-bridge inverter to demonstrate the feasibility and advantages of cascade dual-buck inverter.

In [48], it proposed the control strategy for two dual-buck half-bridge inverters in series output to obtain higher voltage. However, the two dual-buck inverters shared the same dc power supply, had two sets of filter inductor and capacitor, and the connection was only effective for two units. The proposed inverter in this paper has different concept of series connection, the cascading, which has separate dc power supplies for each cell, and is extended to N unit connection, and shares the same filter components.

Fig. 2.1 shows the topology of the proposed cascade dual-buck half-bridge inverter. It consists of N units of single dual-buck half-bridge inverter. Each unit is composed of two power MOSFETs and two fast recovery diodes. Each unit has two output ports, *i*P and *i*N (i=1, 2, …, N). To realize the cascade topology, connect the *i*N port of the i^{th} unit with the (*i*+1)P port of the $(i+1)^{th}$ unit, and use port 1P and NN as the output ports.

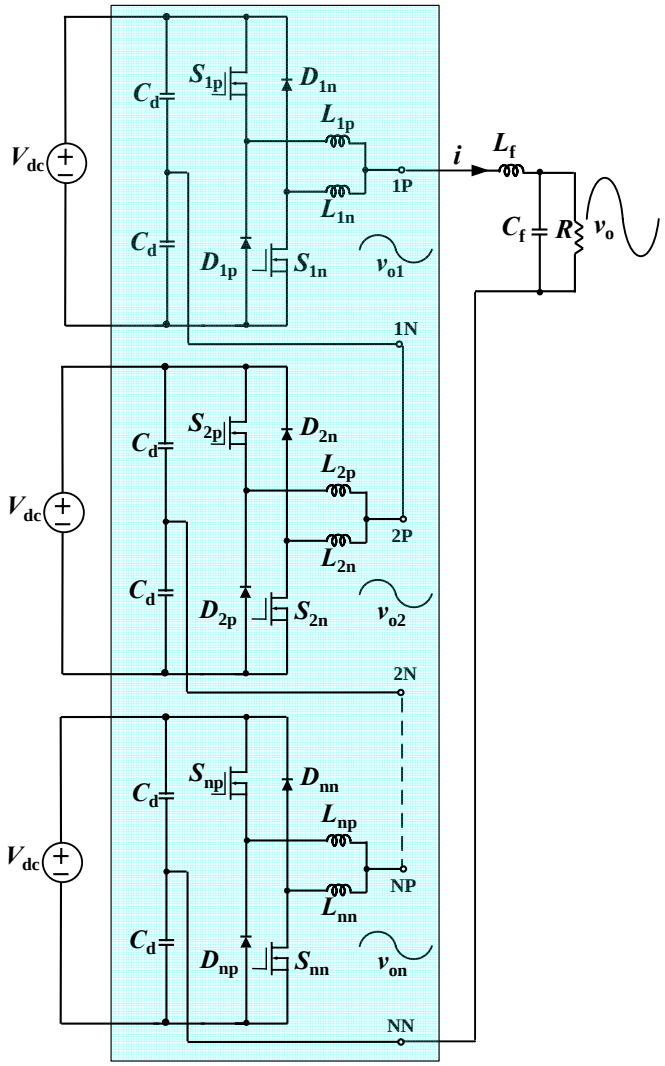
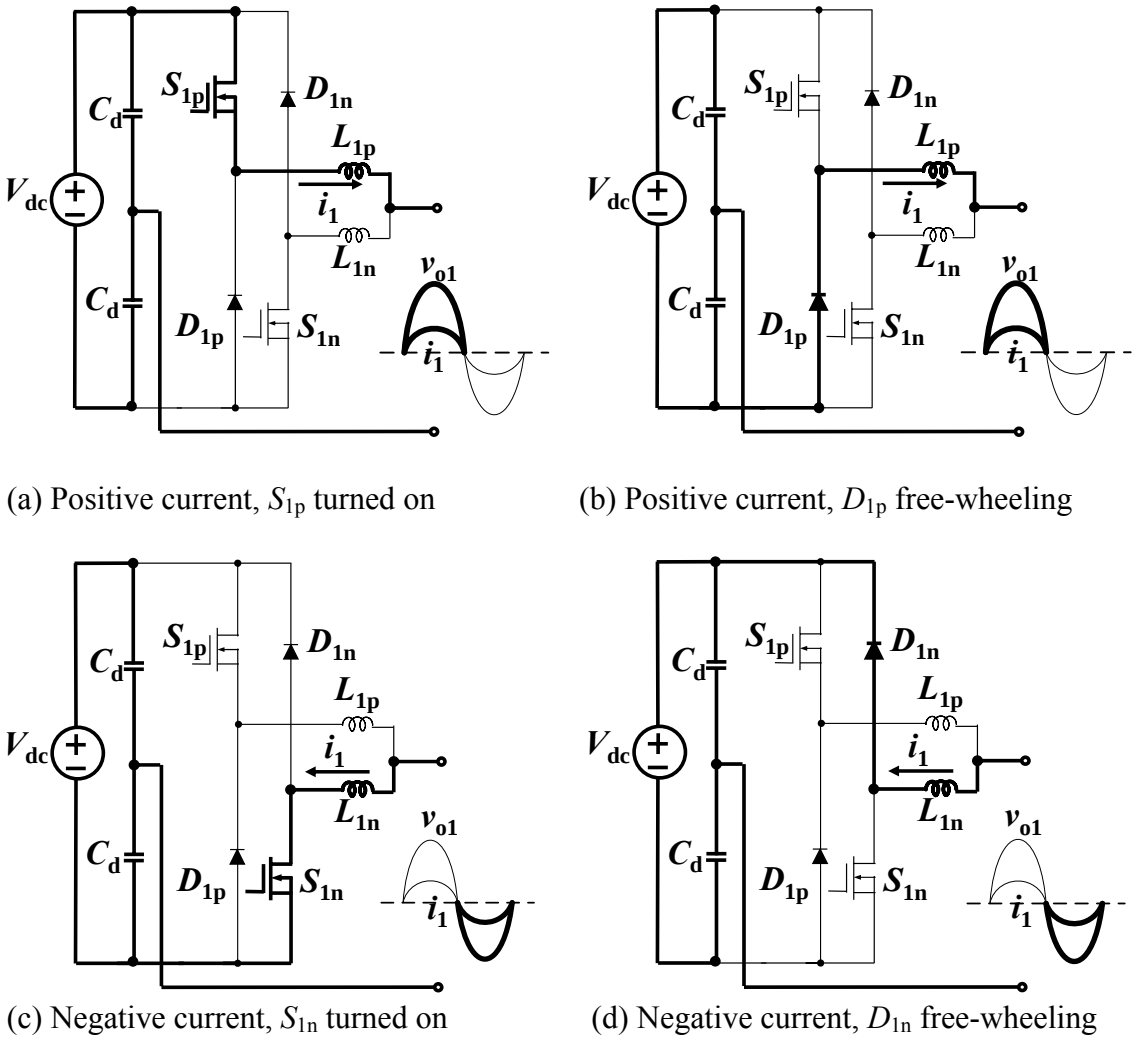


Fig. 2.1: Topology of cascade dual-buck half-bridge inverter.

S_{ip} and D_{ip} are a working pair, and operate at the positive half-cycle of output current i. S_{in} and D_{in} are another working pair, and operate at the negative half-cycle of output current i. The single unit operation modes are shown in Fig. 2.2 [46], [48]. For the cascade dual-buck inverter, if phase-shift control is not adopted, we can switch all the units exactly the same as single-unit inverter. It means the PWMs for S_{ip} and S_{in} are the same. However, this will bring in the zero-crossing distortion problem of single-unit dual-buck inverter into the cascade topology. In addition, without phase-shift control, the

cascade topology loses its benefits of increased equivalent switching frequency and reduced output current ripple. Therefore, the proposed cascade dual-buck inverter utilizes the phase-shift control technique to eliminate the zero-crossing distortion problem of single unit dual-buck inverter and at the same time achieve higher equivalent switching frequency thus cutting down output current ripple. The detailed analysis of phase-shift control of cascade dual-buck inverter will be presented in chapter 2.3.



(a) Positive current, S_{1p} turned on

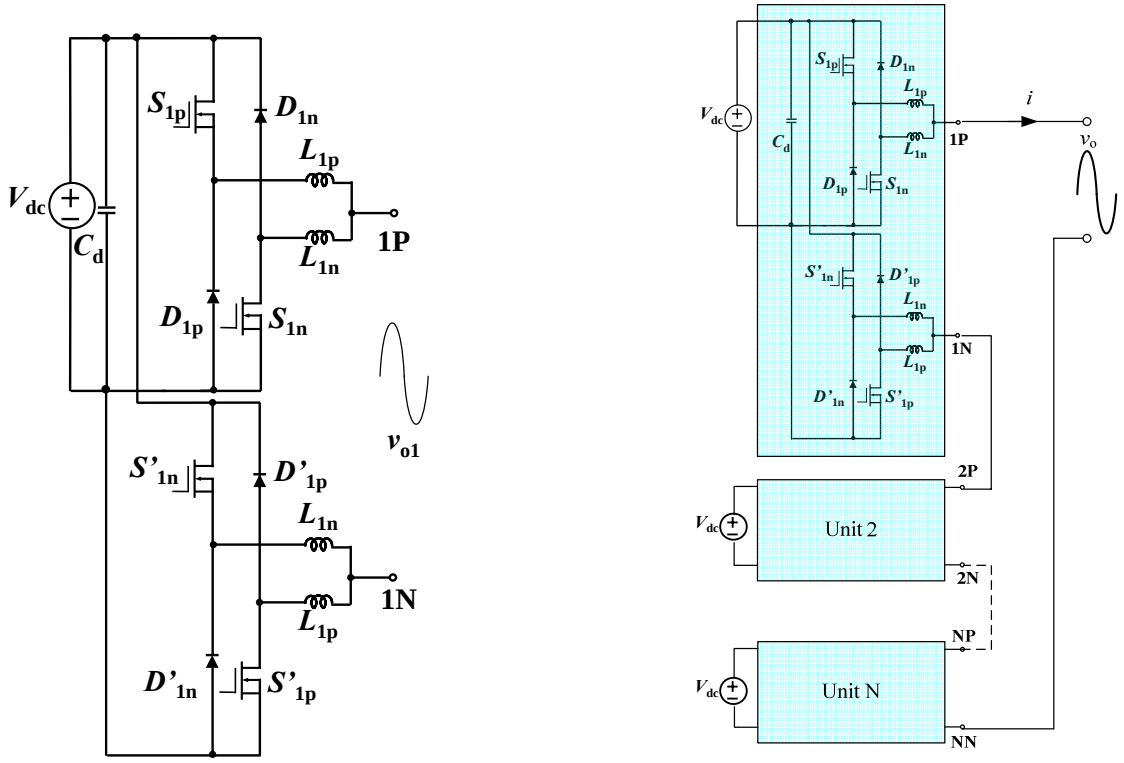
(b) Positive current, D_{1p} free-wheeling

(c) Negative current, S_{1n} turned on

(d) Negative current, D_{1n} free-wheeling

Fig. 2.2: Operation modes of single-unit dual-buck half-bridge inverter.

Fig. 2.3 (a) shows the topology of single-unit full-bridge dual-buck inverter [47]. For the cascade dual-buck full-bridge inverter shown in Fig. 2.3 (b), we can put N units of this single full bridge dual-buck inverter in series similar to cascade dual-buck half-bridge inverter in Fig. 2.1. The operation principle of cascade dual-buck full-bridge inverter with phase-shift control will be discussed in chapter 3.



(a) Single-unit dual-buck full-bridge inverter (b) Cascade dual-buck full-bridge inverter

Fig. 2.3: Single-unit dual-buck full-bridge inverter serving as one cell for cascade dual-buck full-bridge inverter.

2.3 Phase-Shift Control Analysis

One of the significant characteristics of single-unit dual-buck type inverter is that the switch is selectively working based on the direction of output current. From the operation modes of single-unit half-bridge dual-buck inverter in Fig. 2.2, we can clearly see that when i_1 is positive, S_{1p} and D_{1p} are the working pair, and when i_1 is negative, S_{1n} and D_{1n} are the working pair. This distinctive operation leads to its inherent drawback, current zero-crossing distortion, which will be explained in detail below. This issue can be passively mitigated by turning on both S_{1p} and S_{1n} near zero-crossing period. However, this remedy is against the operating principle and the best feature of dual-buck type inverter, high reliability by avoiding turning on both active switches at the same time. In addition, this passive measure results in higher switching losses because at zero-crossing period two switches are switching while the original goal of dual-buck inverter is only one switch operates at any given time.

Thanks to cascade topology, it opens the door to actively solving this current zero-crossing distortion by using phase-shift control scheme. With phase-shifted PWM fed to different cascade units, it theoretically eliminates the current zero-crossing distortion. In addition, the phase-shift control greatly increases the equivalent switching frequency by N times than that of single-unit inverter, which leads to significantly lower current ripple or smaller passive filter component selections.

In order to illustrate the phase-shift control, single-unit half-bridge dual-buck inverter and 2-unit cascade half-bridge dual-buck inverter are analyzed. Fig. 2.4

shows the equivalent circuit of single-unit half-bridge dual buck inverter when S_{1p} is on. Fig. 2.5 shows the gate signal of S_{1p} and the current through output inductor i_1. The shaded area of Fig. 2.5 corresponds to the operation mode shown by Fig. 2.4.

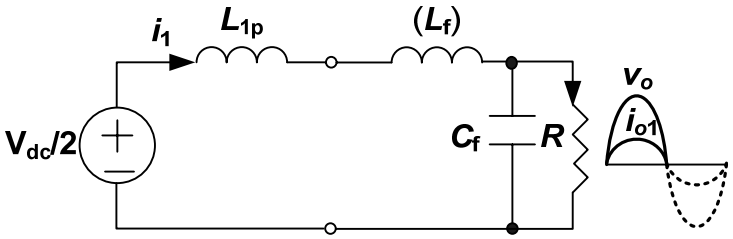


Fig. 2.4: Equivalent circuit of single-unit half-bridge dual-buck inverter when S_{1p} is on.

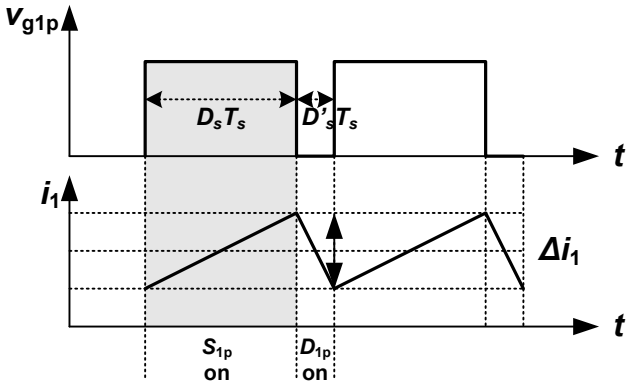


Fig. 2.5: Gate signal of S_{1p} and current i_1 through output inductor of single-unit half-bridge dual-buck inverter.

The current ripple of i_1 can be derived from Fig. 2.4 and Fig. 2.5 as follows:

$$\Delta i_1 = \frac{(0.5V_{dc} - v_o)D_s T_s}{L_{1p} + L_f} \tag{2.1}$$

where D_s is the duty cycle of the switch S_{1p}, $0.5 \le D_s \le 1$ (Bipolar SPWM); and $T_s = \frac{1}{f_s}$, f_s is the switching frequency of S_{1p}.

At zero-crossing period, D_s is approaching 0.5. Therefore, the current ripple of i_1 at

zero-crossing region is not zero. The same analysis applies to the negative half-cycle current. After the two half-cycle currents with switching frequency component are filtered by output capacitor C_f, the current i_{o1} gets its average component. It connects the averages of positive half-cycle current and negative half-cycle current at zero-crossing period. Because both half-cycle current averages at zero-crossing are not zero, there is a jump from the negative average to the positive average, which is the current zero-crossing distortion. Since the load is resistive, the output voltage v_o has the same shape as i_{o1}, and thus has the distortion. In light load condition, the resistance is much larger, so the zero-crossing distortion of the output voltage is amplified by the multiplication of the distorted current and the load resistance.

Fig. 2.6 shows the experimental result of output current i_1 and output voltage v_o across the load at zero-crossing period of single-unit dual-buck inverter.

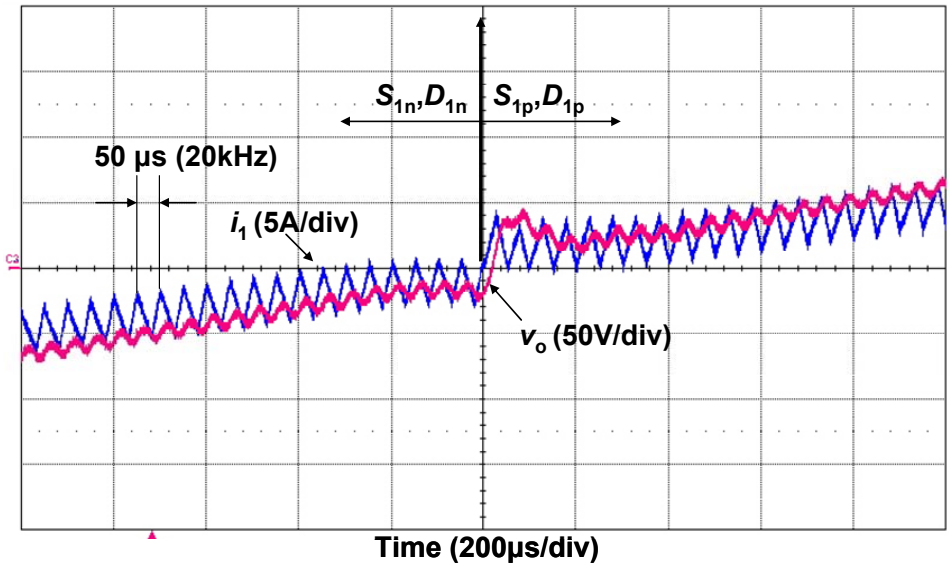


Fig. 2.6: Experimental result of single-unit half-bridge dual-buck inverter at zero-crossing period.

Fig. 2.7 shows the equivalent circuit of 2-unit cascade half-bridge dual-buck inverter when S_{1p} and S_{2p} are on. Fig. 2.8 shows the gate signals of S_{1p} and S_{2p}, and

the current through output inductor i_2. The shaded area of Fig. 2.8 corresponds to the operation mode shown by Fig. 2.7. The 2-unit phase-shift angle is 180^o (Phase-shift angle is 360^o/N). In order to generate the same output voltage v_o, the 2-unit cascade inverter needs 2 dc sources with $0.5V_{dc}$ each.

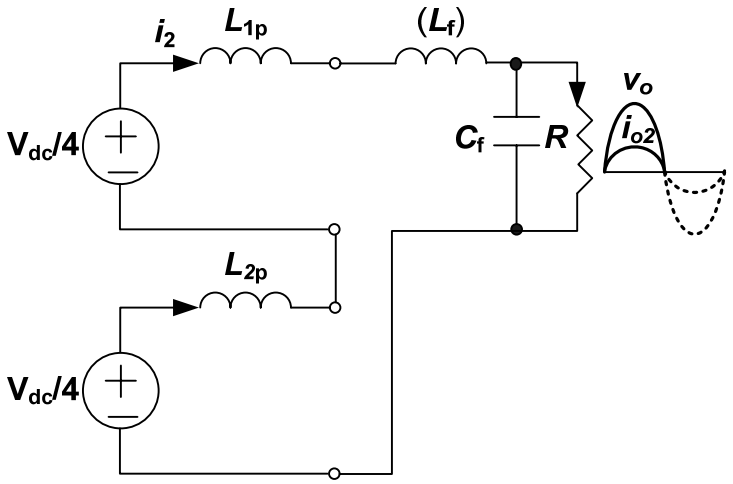


Fig. 2.7: Equivalent circuit of 2-unit cascade half-bridge dual-buck inverter when S_{1p} and S_{2p} are both on.

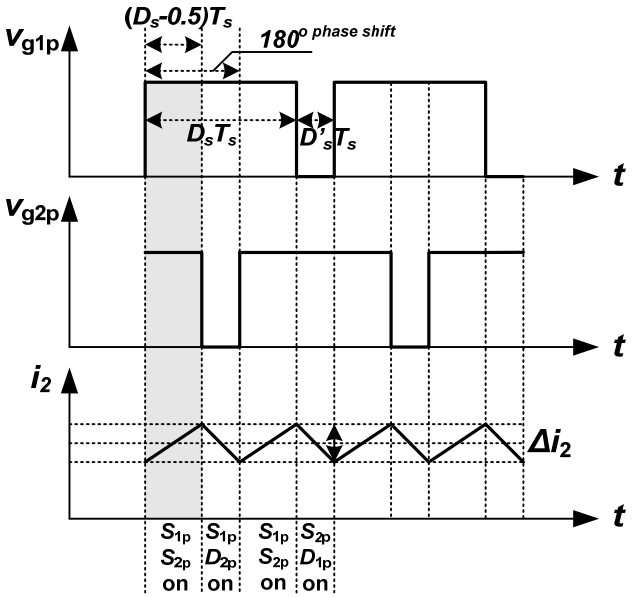


Fig. 2.8: Gate signals of S_{1p} , S_{2p} and current i_2 through output inductor of 2-unit cascade half-bridge dual-buck inverter.

The current ripple of i_2 can be derived from Fig. 2.7 and Fig. 2.8 as follows:

$$\Delta i_2 = \frac{(0.25V_{dc} + 0.25V_{dc} - v_o)(D_s - 0.5)T_s}{L_{1p} + L_{2p} + L_f} \tag{2.2}$$

If L_{1p}=L_{2p}, Eq. (2.2) can be rewritten as

$$\Delta i_2 = \frac{(0.5V_{dc} - v_o)(D_s - 0.5)T_s}{2L_{1p} + L_f} \tag{2.3}$$

In order to find out the generalized equation of current ripple with phase-shift control for n-unit cascade half-bridge dual-buck inverter, similar process of derivation has been conducted for enough samples, from 3-unit inverter up to 5-unit inverter. The results are shown in Table 2.1 as follows, and it is under the assumption that L_{1p}=L_{2p}=…=L_{np}.

Table 2.1: Current ripple derivation for 3, 4, and 5-unit cascade dual-buck inverters.

current ripple / unit	Δi_j
3	$\Delta i_3 = \frac{(\frac{2}{2\cdot 3}V_{dc} - v_o)(D_s - \frac{1}{3})T_s}{3L_{1p} + L_f}$
4	$\Delta i_4 = \frac{(\frac{3}{2\cdot 4}V_{dc} - v_o)(D_s - \frac{2}{4})T_s}{4L_{1p} + L_f}$
5	$\Delta i_5 = \frac{(\frac{3}{2\cdot 5}V_{dc} - v_o)(D_s - \frac{2}{5})T_s}{5L_{1p} + L_f}$

From Table 2.1, the generalized form of current ripple for n-unit cascade half-bridge dual-buck inverter can be derived in the following equation

$$\Delta i_n = \frac{(\frac{\left\lceil \frac{n+1}{2} \right\rceil}{2n}V_{dc} - v_o)(D_s - \frac{\left\lceil \frac{n-1}{2} \right\rceil}{n})T_s}{nL_{np} + L_f} \tag{2.4}$$

where $\lceil x \rceil$ is the ceiling function, and is defined as the smallest integer not less than x

$$\lceil x \rceil = \min\{m \in \mathbb{Z} \mid m \geq x\} \tag{2.5}$$

x is real number, m is integer, and $\mathbb{Z}$ is the set of integers.

As can be seen from (2.4), at zero-crossing period, D_s is very close to 0.5, and thus the current ripple at zero-crossing region is greatly reduced compared to single-unit inverter. Theoretically, when n is the even number, there is no current distortion at zero-crossing point because $\lceil (n-1)/2 \rceil / n$ is equal to 0.5. It is obvious with the increase of the number of cascade units, the current ripple becomes smaller and smaller.

Fig. 2.9 shows the experimental result of output current i_2 and output voltage v_o across the load at zero-crossing period of 2-unit dual-buck inverter with phase-shift control. There is practically no current distortion.

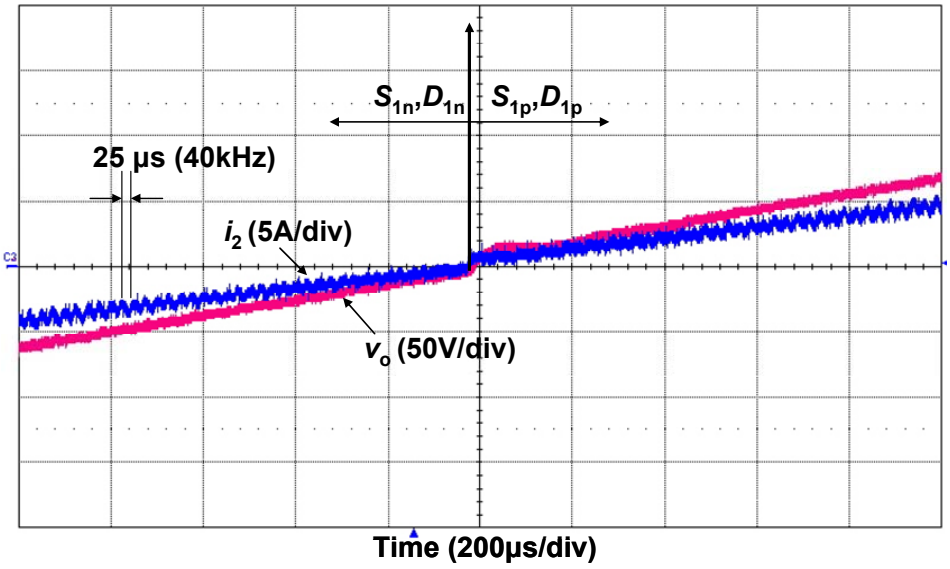


Fig. 2.9: Experimental result of 2-unit cascade half-bridge dual-buck inverter at zero-crossing period.

From Fig. 2.6 and Fig. 2.9, we can see that the equivalent switching frequency of 2-unit cascade inverter with phase-shift control is doubled, which leads to current ripple cut-down. From (2.1) and (2.3), the current ripple ratio is

$$\gamma = \frac{\Delta i_2}{\Delta i_1} = \frac{D_s - 0.5}{D_s} \cdot \frac{L_{1p} + L_f}{2L_{1p} + L_f} \tag{2.6}$$

Since L_{ip} is already serving as the filter inductor, and if L_f=0, (2.6) can be analyzed as

$$\gamma = (1 - \frac{0.5}{D_s}) \cdot 0.5 \le 25\% \tag{2.7}$$

Fig. 2.10 shows the current ripple ratio curve under different duty cycles. From Fig. 2.10 we can see that at zero-crossing, the ratio reaches the lowest, zero and climbs up when D_s increases. Even as D_s approaches 1, the maximum ratio is only 25%.

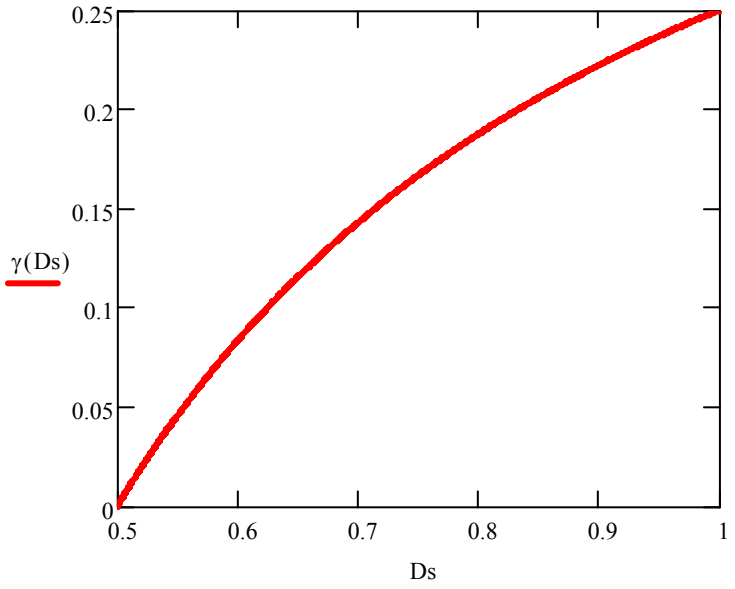


Fig. 2.10: Current ripple ratio between single-unit dual-buck inverter and 2-unit cascade dual-buck inverter.

2.4 Closed Loop System Control Design

In order to demonstrate the feasibility and advantages of cascade dual-buck inverter, the closed-loop control is derived and designed below for a 1kW, 120VAC standalone system shown in Fig. 2.1.

Fig. 2.11 shows the average model of N-unit cascade half-bridge dual-buck inverter. d_j (j=1, …, n) is the duty cycle of each corresponding unit, and L_j (j=1, …, n) is the output inductor of each unit

$$\begin{aligned} L_j &= L_{jp} \qquad i > 0 \\ L_j &= L_{jn} \qquad i < 0 \end{aligned} \tag{2.8}$$

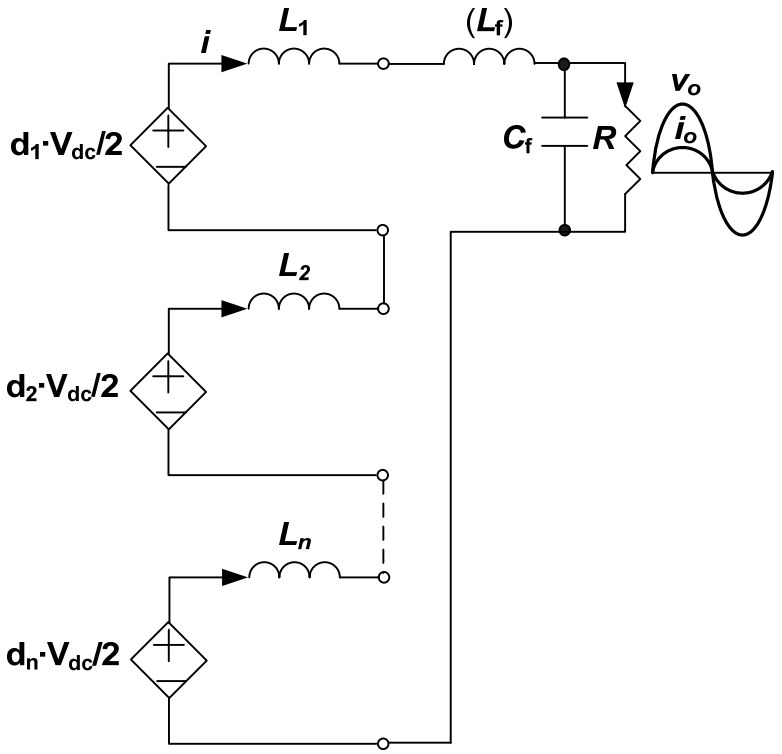


Fig. 2.11: The average model of N-unit cascade half-bridge dual-buck inverter.

From Fig. 2.11, we have the following relation

$$(d_1 + d_2 + \cdots + d_n) \cdot \frac{V_{dc}}{2} = \frac{d_1 + d_2 + \cdots + d_n}{N} \cdot \frac{NV_{dc}}{2} \tag{2.9}$$

d_j can be different from each other. However, to maintain the power balance of each cascade unit, it is desirable to have equal d_j. So if $d_1 = d_2 = \cdots = d_n = d$, (2.9) can be rewritten as

$$(d_1 + d_2 + \cdots + d_n) \cdot \frac{V_{dc}}{2} = d \cdot \frac{NV_{dc}}{2} \tag{2.10}$$

From (2.10) and Fig. 2.11, it is easy to derive the equivalent average model of N-unit cascade dual-buck inverter shown in Fig. 2.12, where $\Sigma L_j = L_1 + L_2 + \cdots + L_n$.

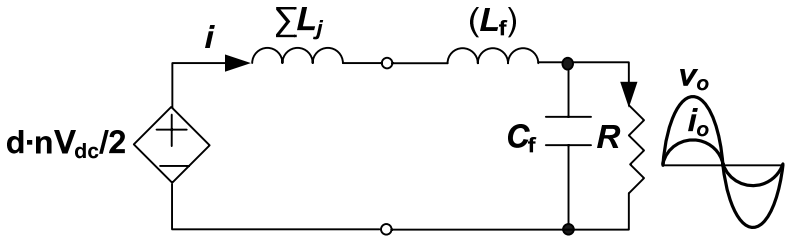


Fig. 2.12: The equivalent average model of N-unit cascade half-bridge dual buck inverter.

Define $L = \Sigma L_j + L_f$, and we have the following equation from Fig. 2.12.

$$d(t) \cdot \frac{NV_{dc}}{2} - v_o(t) = L \frac{di(t)}{dt} \tag{2.11}$$

Transform (2.11) to s domain, we have

$$i(s) = \frac{1}{sL}(d(s) \cdot \frac{NV_{dc}}{2} - v_o(s)) \tag{2.12}$$

So the transfer functions from duty cycle d to current i and voltage v_o to current i are as follows

$$G_{id}(s)=\frac{i(s)}{d(s)}=\frac{\frac{NV_{dc}}{2}}{sL} \tag{2.13}$$

$$G_{iv}(s)=\frac{i(s)}{v_o(s)}=\frac{1}{sL} \tag{2.14}$$

where $G_{id}(s)$ is the control-to-output transfer function and $G_{iv}(s)$ is an uncontrolled feed-forward term. By introducing admittance compensation controller $G_{AC}(s)$ shown in Fig. 2.13, the undesirable term can be cancelled out, which brings in a better smoothed zero-current start-up and reduced current steady-state error[54]-[55].

Fig. 2.13 shows the control block diagram of N-unit cascade half-bridge dual-buck inverter operating at standalone mode. The closed-loop design adopts dual-loop design, the inner current loop with a simple proportional controller $G_P(s)$ to achieve fast dynamic response with enough stability margin and the outer voltage loop with a PR controller $G_{PR}(s)$ to ensure a higher loop gain at fundamental frequency reducing the steady-state voltage error [56]-[58].

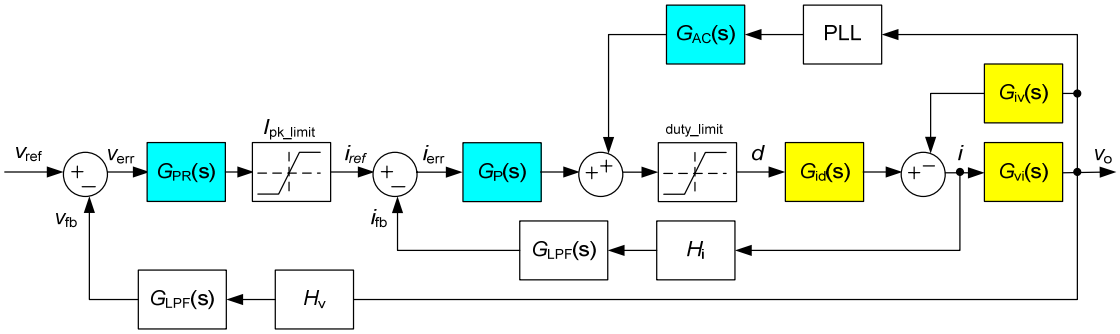


Fig. 2.13: Control block diagram of N-unit cascade half-bridge dual-buck inverter operating at standalone mode.

For this 1kW, 120VAC output cascade inverter system, the controllers are designed as follows.

For the PR controller in (2.15), k_p is the proportional gain, k_r is the resonant gain, and ω_c is the equivalent bandwidth of the resonant controller. In principle, the bandwidth ω_c needs to be as small as possible to obtain a highly selective bandwidth, but for digital implementation, it is quite difficult to realize a small ω_c. The controller gain at fundamental frequency can be increased by increasing either k_p or k_r. On the other hand, k_p and k_r can not be too high because it will impair the system stability [57]-[59]. With all the considerations above, the parameters for PR controller in this design have been chosen

$$G_{PR}(s) = k_p + \frac{2\omega_c k_r s}{s^2 + 2\omega_c s + \omega_1^2} \tag{2.15}$$

where $k_p = 0.02$, $k_r = 12$, $\omega_c = 10$

A current loop in a dual-loop system is designed to have a high loop bandwidth with enough stability margins rather than to reduce the current steady-state error by providing a high gain at fundamental frequency [59]. In this design, a simple proportional controller will meet the requirement.

$$G_P(s) = 0.05 \tag{2.16}$$

In [55], the equivalent dc bus voltage is V_{dc} for single unit inverter system, and thus the outcome of admittance compensation term is the reciprocal of V_{dc}. From Fig. 2.13, we can see clearly that the equivalent dc bus voltage for the cascade dual-buck inverter is $NV_{dc}/2$. Therefore, the admittance compensation transfer function is obtained as follows

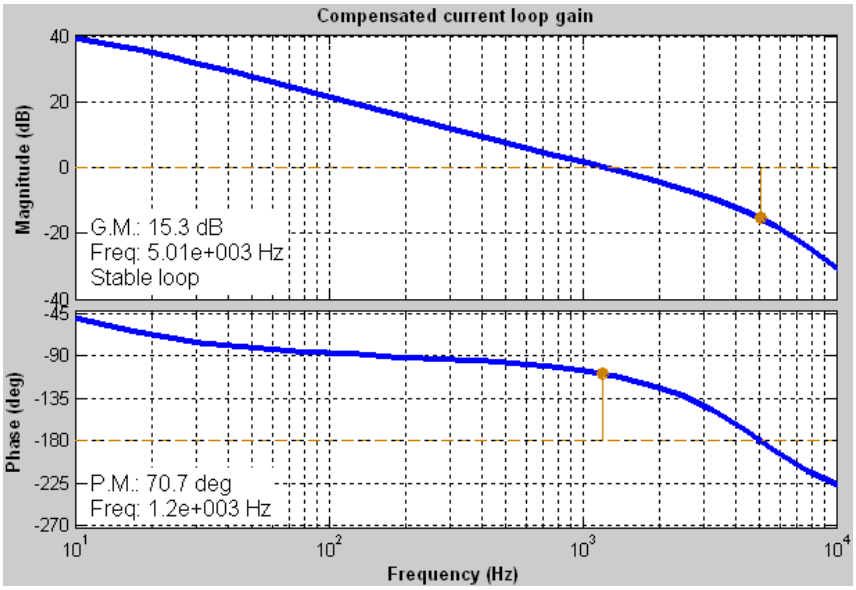
$$G_{AC}(s) = \frac{1}{\frac{NV_{dc}}{2}} \tag{2.17}$$

In order to close the outer voltage loop, shown in Fig. 2.13, $G_{vi}(s)$ is derived below based on the model in Fig. 2.12.

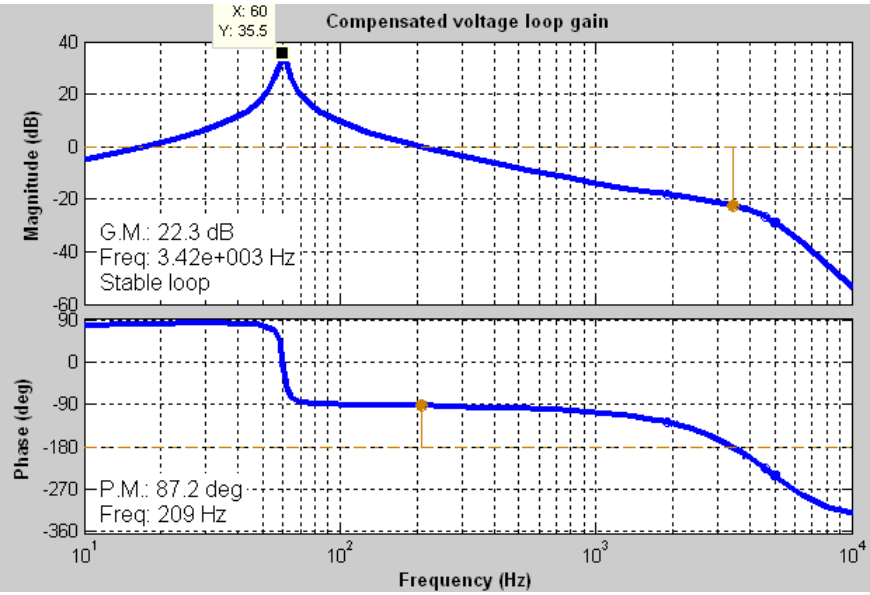
$$G_{vi}(s) = \frac{1}{sC_f + 1/R} \tag{2.18}$$

$G_{LPF}(s)$ is 2nd order low pass filter with cut-off frequency 5kHz and a damping ratio 0.7.

With the designed controllers above, the Bode plot of both compensated inner current loop gain and compensated outer voltage loop gain is shown in Fig. 2.14. As can be seen, the current loop has the cross-over frequency 1.2 kHz with gain margin 15.3dB and phase margin 70.7deg. The voltage loop has the cross-over frequency 209Hz with phase margin 87.2deg, and at 60Hz fundamental frequency it has a gain of 35.5dB to reject the steady state error.



(a) Bode plot of compensated current loop gain



(b) Bode plot of compensated voltage loop gain

Fig. 2.14: Bode plot of compensated inner current loop gain and outer voltage loop gain.

Fig. 2.15 shows the PWM generation flow chart based on the current reference signal from Fig. 2.13. Fig. 2.16 shows the experimental results for PWM generation based on the sequence from Fig. 2.15. It can be seen that the PWMs for S_{ip} and S_{in} never overlap together, which means this cascade dual-buck inverter is shoot-through free. The phase-shifted PWMs are simple to implement by digital controller by just adding an incremental angle to the adjacent cascade unit.

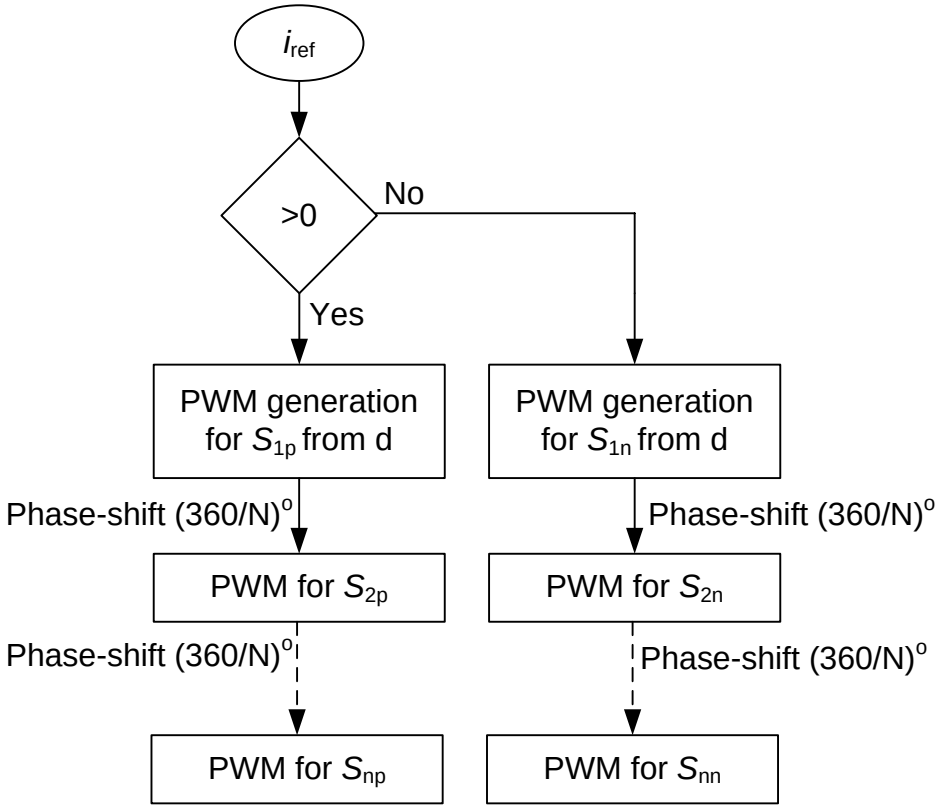
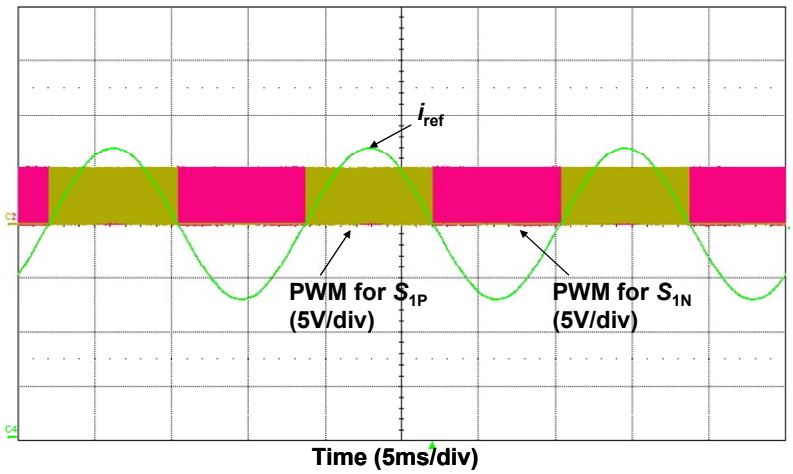
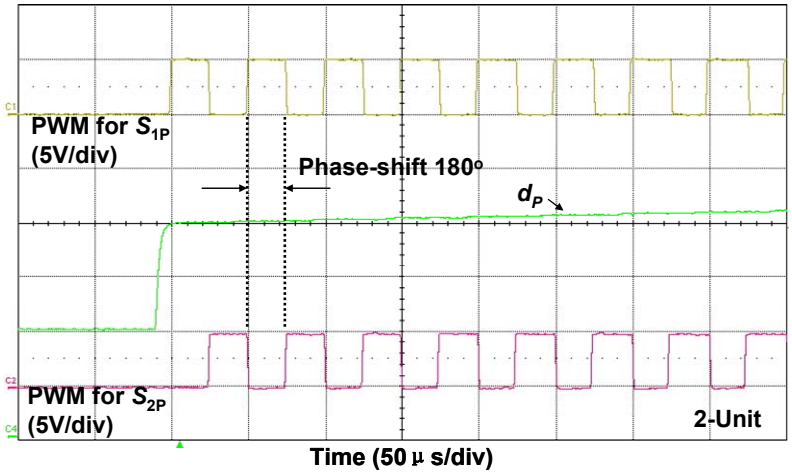


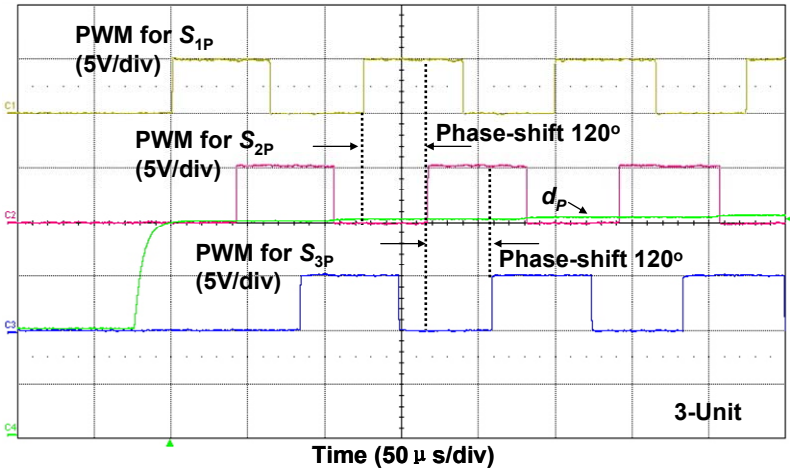
Fig. 2.15: PWM generation for all switches of N-unit cascade half-bridge dual-buck inverter with phase-shift control.



(a) PWM generation for S_{1p} and S_{1n} based on i_{ref} direction



(b) PWM phase-shift of S_{1p} and S_{2p} for 2-unit cascade dual buck inverter



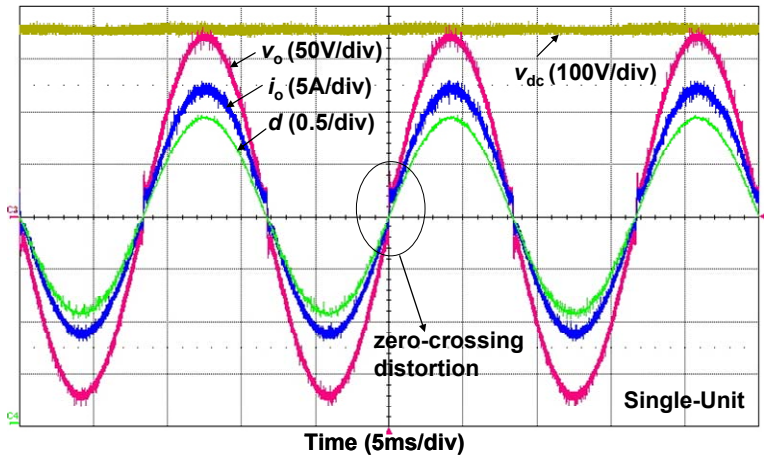
(c) PWM phase-shift of S_{1p}, S_{2p}, and S_{3p} for 3-unit cascade dual buck inverter

Fig. 2.16: Experimental results of PWM generation for N-unit cascade half-bridge dual-buck inverter with phase-shift control.

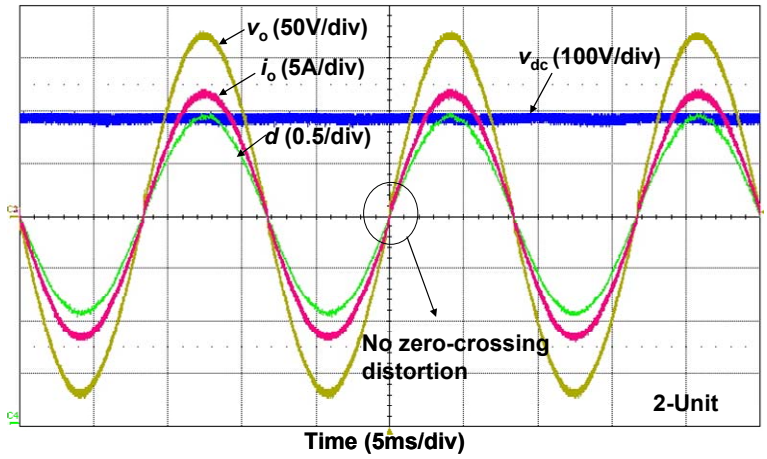
2.5 Comparative Experimental Results

To prove the viability and merits of the proposed cascade dual-buck inverter with phase-shift control, a 1 kW, 120VAC output cascade dual-buck half-bridge inverter system in standalone operation was designed and tested. The system structure of the experiment is the same as in Fig. 2.1, and the control scheme applied is shown in Fig. 2.13 and Fig. 2.15. The system controller and PWM generation are conducted by TI floating point DSP TMS320F28335. The switching frequency of the devices is set to be 20 kHz. Because the cascade dual-buck inverter adopts phase-shifted PWM control, the equivalent switching frequency of the inverter is 40 kHz for 2-unit and 60 kHz for 3-unit cascade inverters, respectively. The MOSFET is selected as STY80NM60N with on-resistance 35mΩ, and the diode is RURG3060 with reverse recovery time 55ns. The passive components are selected as follows: L_{jp}=L_{jn}=250μH, L_f=1mH, C_f=2.4μF, C_d=1.2mF. The system has the ability of serving as single-unit, 2-unit and 3-unit systems. For comparison, tests were conducted with single-unit, 2-unit, as well as 3-unit systems. All the output power of three tests is 1kW, and output AC voltage is 120V RMS. For single-unit system, V_{dc} is 360V, and for 2-unit cascade system, V_{dc} is 180V, and for 3-unit cascade system, V_{dc} is 120V.

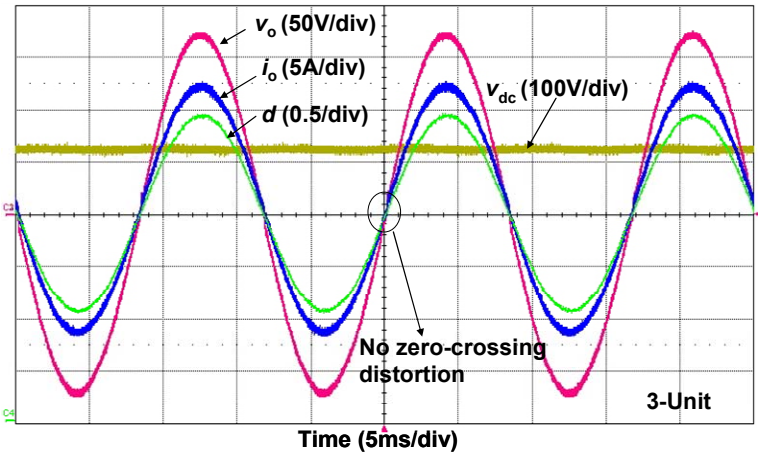
Fig. 2.17 shows the output current i_o through load and voltage waveforms of single-unit dual-buck inverter, 2-unit cascade dual-buck inverter and 3-unit cascade dual-buck inverter at 1kW output. It is clear that with phase-shift control for 2-unit system and 3-unit system, the current zero-crossing distortion was almost eliminated. However, the single-unit zero-crossing is severe.



(a) Single-unit inverter



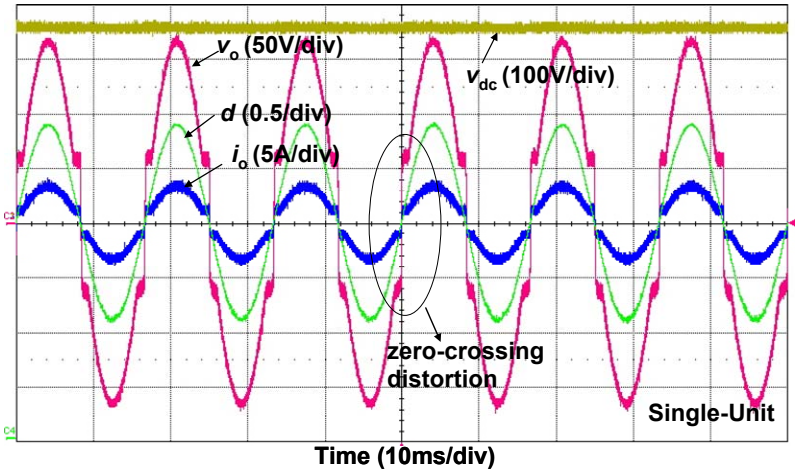
(b) 2-unit cascade inverter



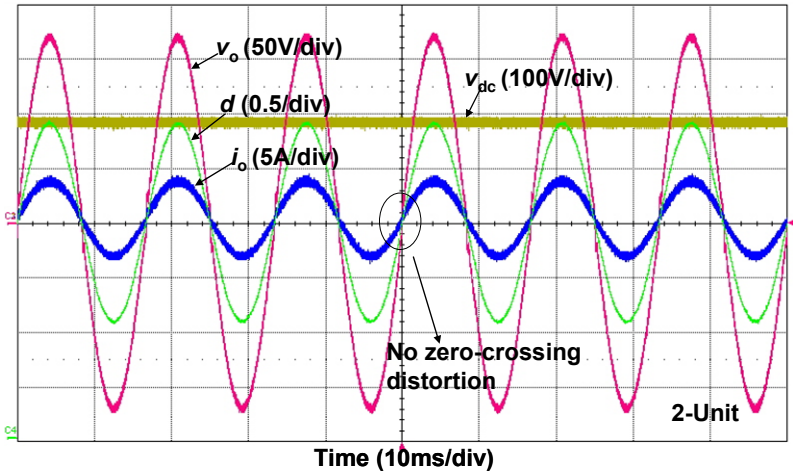
(c) 3-unit cascade inverter

Fig. 2.17: Output current i_o , AC and DC voltage waveforms for single-unit, 2-unit cascade, and 3-unit cascade inverter system at 1kW.

The distortion problem is more obvious in light load conditions for single-unit inverter. Fig. 2.18 shows the comparison between single-unit inverter and 2-unit cascade inverter at 300W output. The aggravated current and voltage distortion with very high THD will be intolerable and impose a risk for the load operation. In contrast, the cascade dual-buck inverter with phase-shift control does not have this distortion at light load either. The THD is measured for both single-unit inverter and cascade dual-buck inverter under full load and light load conditions. The result is shown in Table 2.2. As can be seen, the THD at 300W for single-unit inverter is 10% while for cascade dual-buck inverter it is only around 1%.



(a) Single-unit inverter



(b) 2-unit cascade inverter

Fig. 2.18: Output current i_o , AC and DC voltage waveforms for single-unit, 2-unit cascade inverter system at 300W.

Table 2.2: THD measurement for both single-unit and cascade dual-buck inverters.

	1kW		300W	
	v_o	i_o	v_o	i_o
1-unit	2.6%	2.4%	10.3%	10.0%
2-unit	0.9%	0.8%	1.7%	1.5%
3-unit	0.9%	0.8%	1.5%	1.2%

Fig. 2.19 shows the voltage v_{cd1} and v_{cd2} across the split capacitors from one cell of 3-unit cascade dual-buck half-bridge inverter. For the cascade dual-buck half-bridge inverter, the split capacitors are needed for each cascade unit. It can be seen that the voltage of the capacitors is naturally balanced. In some cases, if the voltage across the capacitors is unbalanced due to use of different types of capacitors, the different ESR or other factors, a voltage balance compensator might be considered [60] to solve the issue. The cascade dual-buck full-bridge inverter is a better alternative to save two split capacitors and totally avoid the issue.

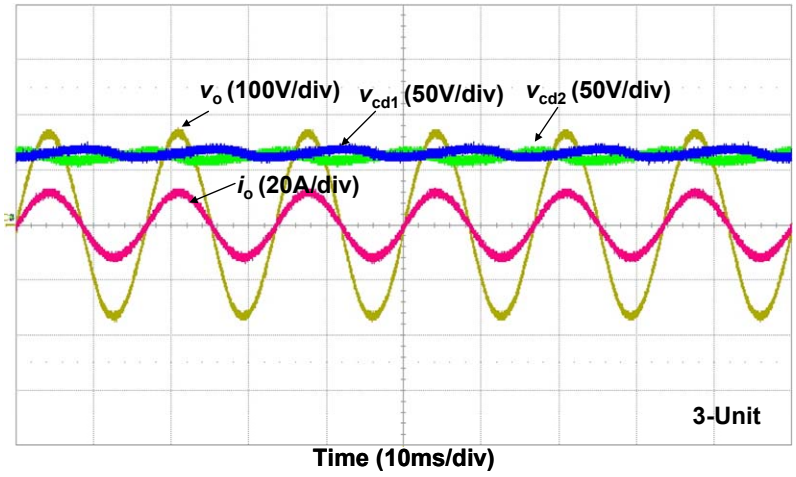
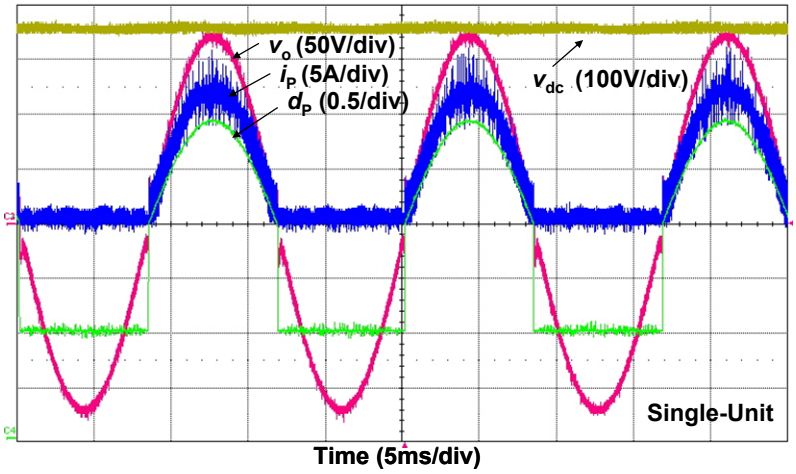
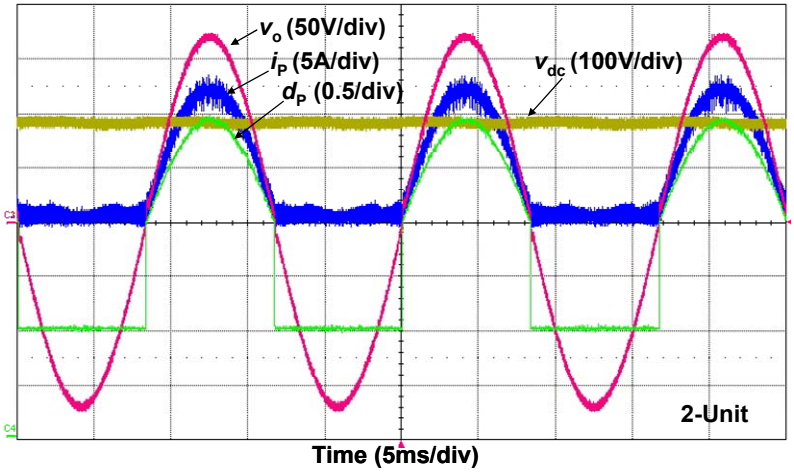


Fig. 2.19: Voltage waveforms across split capacitors for 3-unit cascade dual-buck half-bridge inverter system at 1kW.

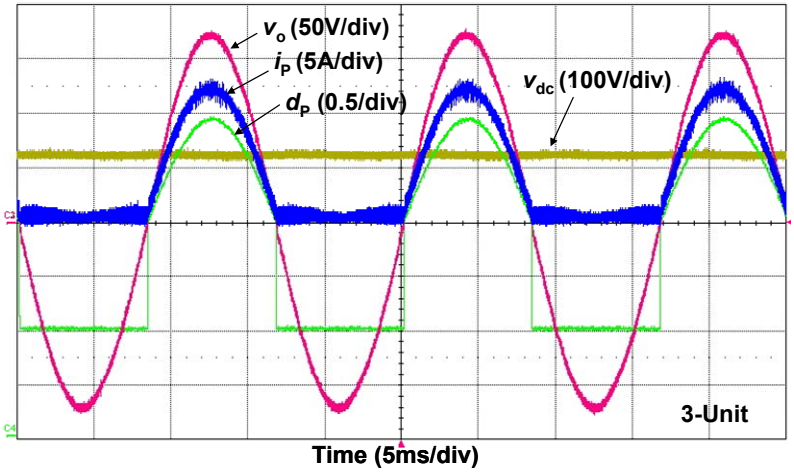
Fig. 2.20 shows the positive half cycle output current i_p through inductor and voltage waveforms of single-unit dual-buck inverter, 2-unit cascade dual-buck inverter and 3-unit cascade dual-buck inverter. d_p is the duty cycle for current positive half-cycle. This shows the unique operating feature of single-unit dual-buck inverter is inherited by cascade dual-buck inverter. Every dual-buck unit in the cascade system maintains the no shoot-through characteristic, and thus leads to a more robust and reliable cascade inverter system than traditional voltage source based cascade inverter.



(a) single-unit inverter



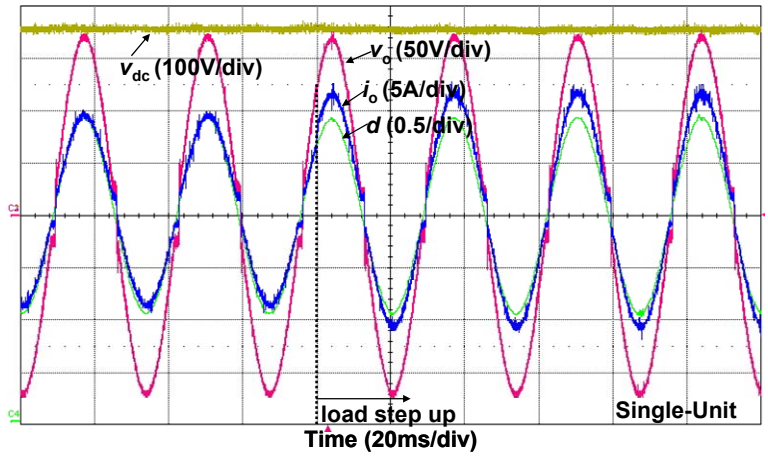
(b) 2-unit cascade inverter



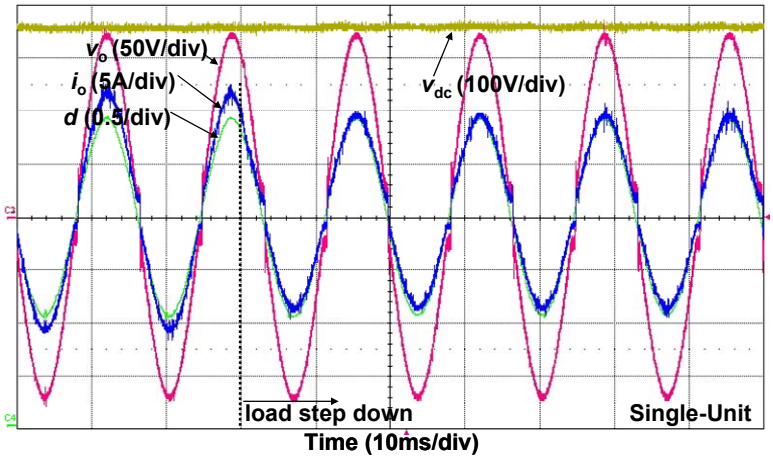
(c) 3-unit cascade inverter

Fig. 2.20: Output positive half-cycle current i_P, AC and DC voltage waveforms for single-unit, 2-unit cascade, and 3-unit cascade inverter system at 1kW.

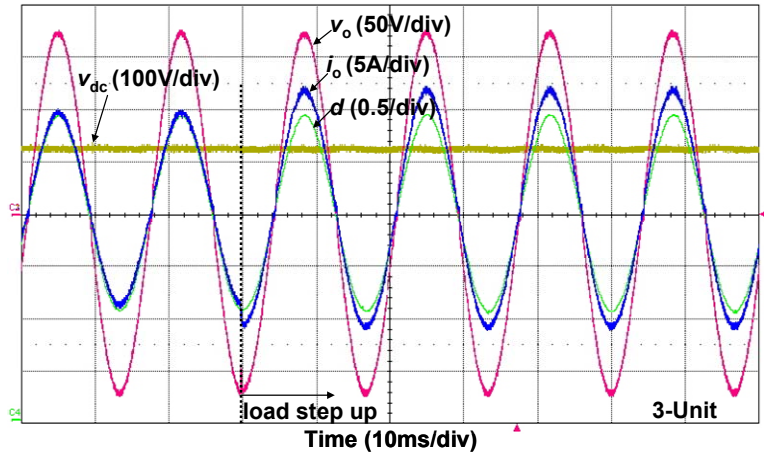
Fig. 2.21 shows the output current and voltage waveforms of single-unit inverter and 3-unit cascade dual-buck inverter under load step conditions. Load step-up and step-down tests were done to show the fast dynamics and good stability of the designed control system for cascade dual-buck inverter. Even though single-unit system can withstand load change, its inherent zero-crossing distortion will affect the control system and be harmful to the load.



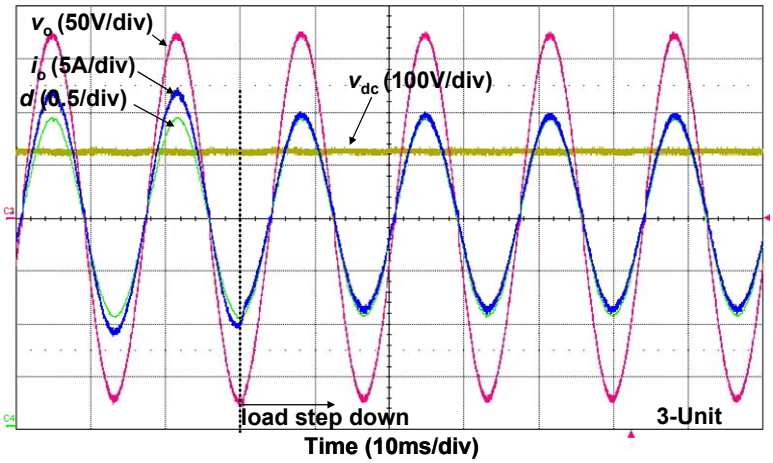
(a) Load step-up test for single-unit inverter



(b) Load step-down test for single-unit inverter



(c) Load step-up test for 3-unit cascade inverter



(d) Load step-down test for 3-unit cascade inverter

Fig. 2.21: Load step-up and step-down tests for single-unit inverter and 3-unit cascade inverter system.

Fig. 2.22 shows the measured efficiency curve under different power output conditions for cascade dual-buck half-bridge inverter.

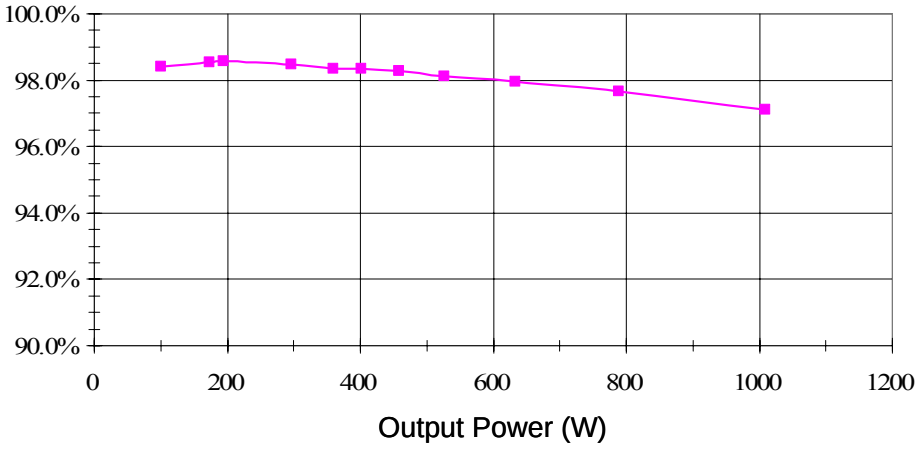


Fig. 2.22: Efficiency measurement under different power output conditions.

2.6 Summary

A new series of cascade dual-buck inverters has been proposed based on single-unit dual-buck inverters. The cascade dual-buck inverter has all the merits of traditional cascade inverters, and improves on its reliability by eliminating shoot-through worries and dead-time concerns. With the adoption of phase-shift control, the cascade dual-buck inverter solves the inherent current zero-crossing distortion problem of single-unit dual-buck inverter.

To prove the effectiveness of the proposed topology and control scheme, a cascade dual-buck half-bridge inverter system operating at standalone mode with 1kW, 120VAC output capability has been designed and tested. By comparison of experimental results of single-unit dual-buck inverter with 2-unit and 3-unit cascade dual-buck inverters, the viability and advantages of the cascade dual-buck inverter are validated.

Chapter 3

Cascade Dual-Buck Full-Bridge Inverter with Different PWM Techniques

3.1 Introduction

The standard full-bridge inverter is a typical voltage source inverter (VSI) with two active switches in one phase leg. It needs dead time to prevent shoot-through problems between the switches in one leg. Because of dead time effect, the output waveforms can be distorted and the equivalent transferred energy of PWM is reduced. Even though with added dead time, shoot-through is still the dominant failure of the circuit, especially at some fault conditions. In addition, with higher dc bus voltage operation, this standard full-bridge inverter can not simply employ power MOSFETs as the active switches due to the reverse recovery problem of the body diode of MOSFETs [38]-[42].

To utilize the benefits of power MOSFETs, such as lower switching loss, resistive conduction voltage drop, and fast switching speed that allows reduction of current ripple and the size of passive components, dual-buck full-bridge inverter had been proposed

[46]-[50]. The dual-buck full-bridge inverter, shown in Fig. 3.1, does not need dead time, and totally eliminates the shoot-through concerns, which leads to greatly enhanced system reliability. The body diode of MOSFET never conducts, and the external diodes D_1 to D_4 can be independently selected to minimize switching losses.

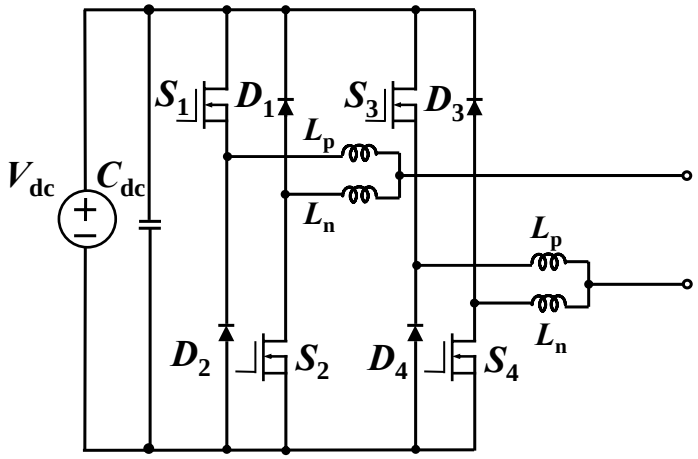


Fig. 3.1: Dual-buck full-bridge VSI with MOSFETs.

However, the traditional bipolar sinusoidal PWM (SPWM) [61]-[62] used on dual-buck full-bridge inverter results in zero-crossing distortion of the output voltage and current, which will be explained in chapter 3.2. Even though the topology adopts MOSFET, the dual-buck full-bridge inverter is still the hard-switching VSI. To further reduce the switching loss in power devices and passive filter components, and at the same time alleviate the zero-crossing distortion problem, an asymmetrical half-cycle unipolar (AHCU) PWM technique for dual-buck full-bridge inverter is proposed in this chapter. This AHCU PWM cuts down the switching loss of power MOSFETs to half by maintaining one active switch without switching during half-cycle of inverter output current. It also reduces the output current ripple, and therefore leads to less power loss in passive components of the inverter. It compensates for the zero-crossing distortion

problem found in ordinary PWM operated dual-buck inverters, and practically eliminates this drawback.

The chapter 3.2 first analyzes the traditional bipolar SPWM technique and points out its disadvantages when applied to dual-buck full-bridge inverters. Then the AHCU PWM method is proposed and elaborated on to solve the zero-crossing distortion problem and improve the system efficiency. In chapter 3.4, a 2kW, 240V ac output prototype has been built and tested to compare SPWM with the proposed novel PWM. Experimental results proved the significant output waveform improvement at zero-crossing under novel PWM. Efficiency of two modulation methods were measured and compared. With the help of the proposed PWM, the efficiency of the inverter is 0.6% higher than that of bipolar SPWM.

Fig. 3.2 shows the proposed topology of the cascade dual-buck full-bridge inverter. It consists of N units of single dual-buck full-bridge inverter. Each unit is composed of four power MOSFETs and four fast recovery diodes. Each unit has two output ports, *i*P and *i*N (i=1, 2, …, N). To realize the cascade topology, connect the *i*N port of the i^{th} unit with the (*i*+1)P port of the $(i+1)^{th}$ unit, and use port 1P and NN as the final output ports.

The chapter 3.3 evaluates several PWM methods, including bipolar PWM, unipolar PWM, and phase-shifted PWM for cascade dual-buck full-bridge inverter. Through analysis, it has been found out that the PWM combination technique, which means the use of two PWM methods at the same time, can lead to elimination of zero-crossing distortion, reduced current ripple, and increased system efficiency. In chapter 3.5, a 1kW, 240VAC output cascade dual-buck full-bridge inverter prototype has been designed and tested to validate the proposed topology and different PWMs control. The zero-crossing and current

ripple waveforms, and the current total harmonic distortion (THD) have been compared side by side under different PWMs.

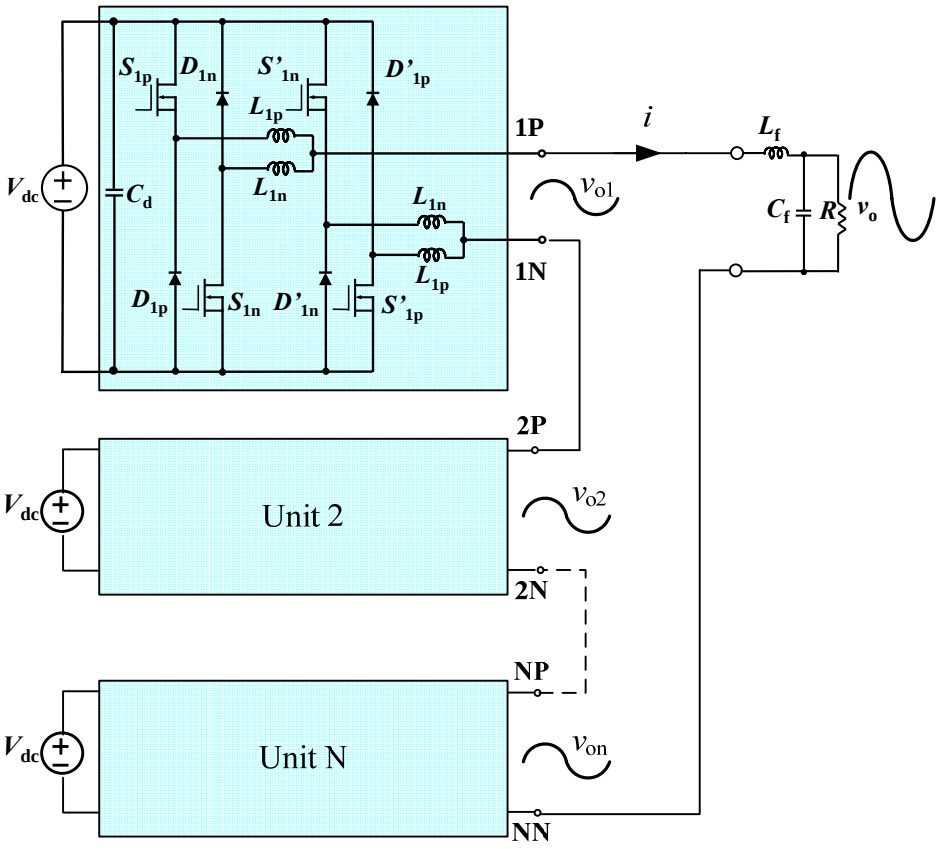
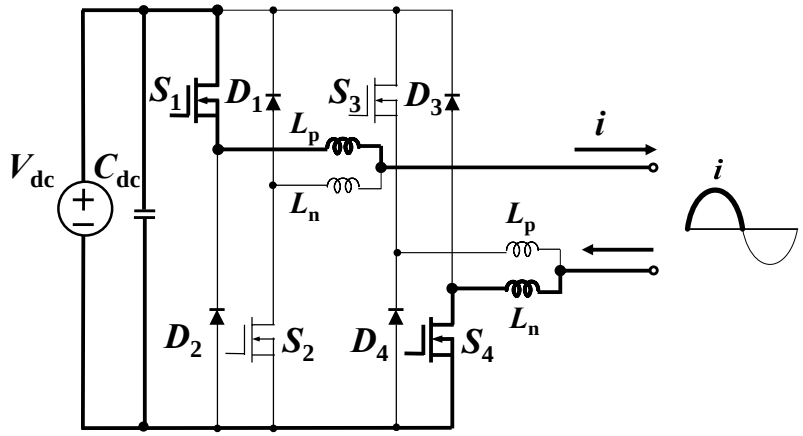


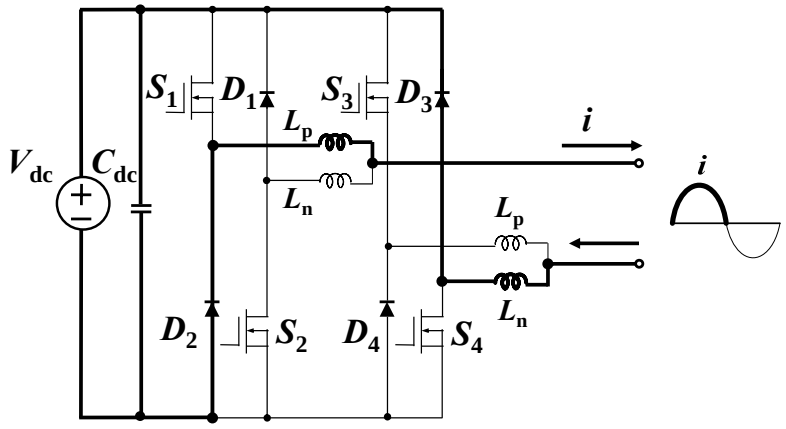
Fig. 3.2: Topology of cascade dual-buck full-bridge inverter.

3.2 PWM Analysis for Single-Unit Dual-Buck Full-Bridge Inverter

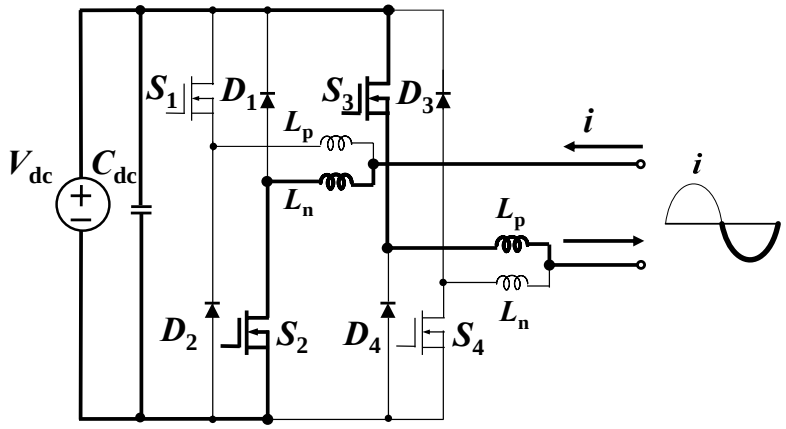
One of the significant features of a dual-buck full-bridge inverter is that the switch is selectively working based on the direction of output current. Fig. 3.3 shows the operation modes of dual-buck full-bridge inverter under traditional bipolar SPWM. When the output current i is in the positive half cycle, (S_1, D_2) and (S_4, D_3) are the two pairs of working devices. The energy is pumped out when S_1 and S_4 are turned on, shown in Fig. 3.3 (a). D_2 and D_3 are freewheeling when S_1 and S_4 are turned off, shown in Fig. 3.3 (b). Likewise, when the output current i is negative, the operation shifts to (S_2, D_1) and (S_3, D_4). The dc side energy is transferred to ac side by turning on S_2 and S_3, indicated in Fig. 3.3 (c). D_1 and D_4 start to conduct the current when S_2 and S_3 are off, shown in Fig. 3.3 (d).



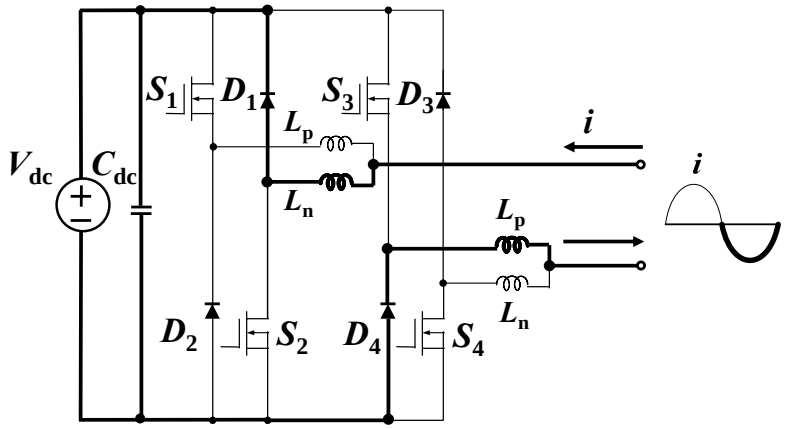
(a) Positive current, S_1 and S_4 turned on



(b) Positive current, D_2 and D_3 free-wheeling



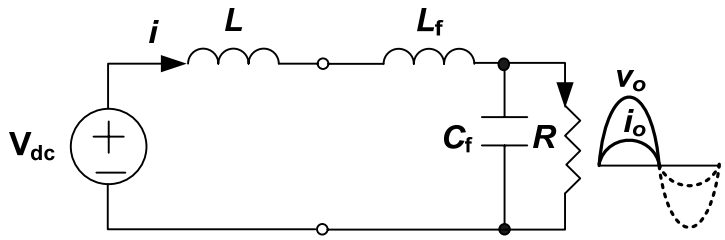
(c) Negative current, S_2 and S_3 turned on



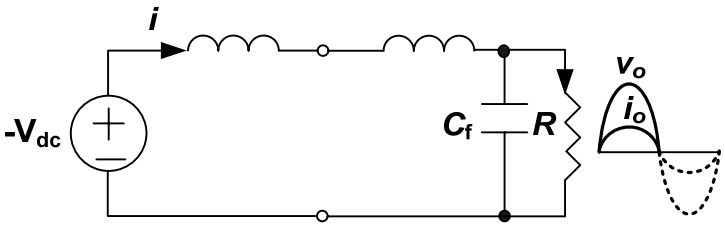
(d) Negative current, D_1 and D_4 free-wheeling

Fig. 3.3: Operation modes under traditional bipolar SPWM.

Fig. 3.4 shows the equivalent circuit of the dual-buck full-bridge inverter at the output current positive half cycle, which relates to the operation mode in Fig. 3.3 (a) and (b). L_f and C_f are the filter inductor and capacitor. L is the output inductor, and is equal to the sum of L_p and L_n. Fig. 3.5 shows the gate signal of S_1 and S_4, and the current through output inductor i. The shaded area of Fig. 3.5 corresponds to the operation mode shown in Fig. 3.4 (a). D_s is the duty cycle for the switch S_1 and S_4, and under traditional bipolar SPWM, $0.5 \le D_s \le 1$.



(a) S_1 and S_4 on



(b) D_2 and D_3 freewheeling

Fig. 3.4: Equivalent circuit of dual-buck full-bridge inverter when output current is positive.

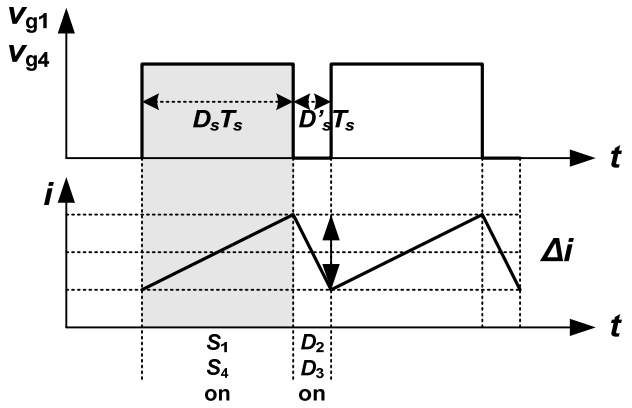


Fig. 3.5: Gate signal of S_1 and S_4 with current i through output inductor.

The current ripple of i can be derived from Fig. 3.4 and Fig. 3.5 as follows:

$$\Delta i = \frac{(V_{dc} - v_o)D_s T_s}{L + L_f} \tag{3.1}$$

where $T_s = \frac{1}{f_s}$, f_s is the switching frequency of S_1 and S_4.

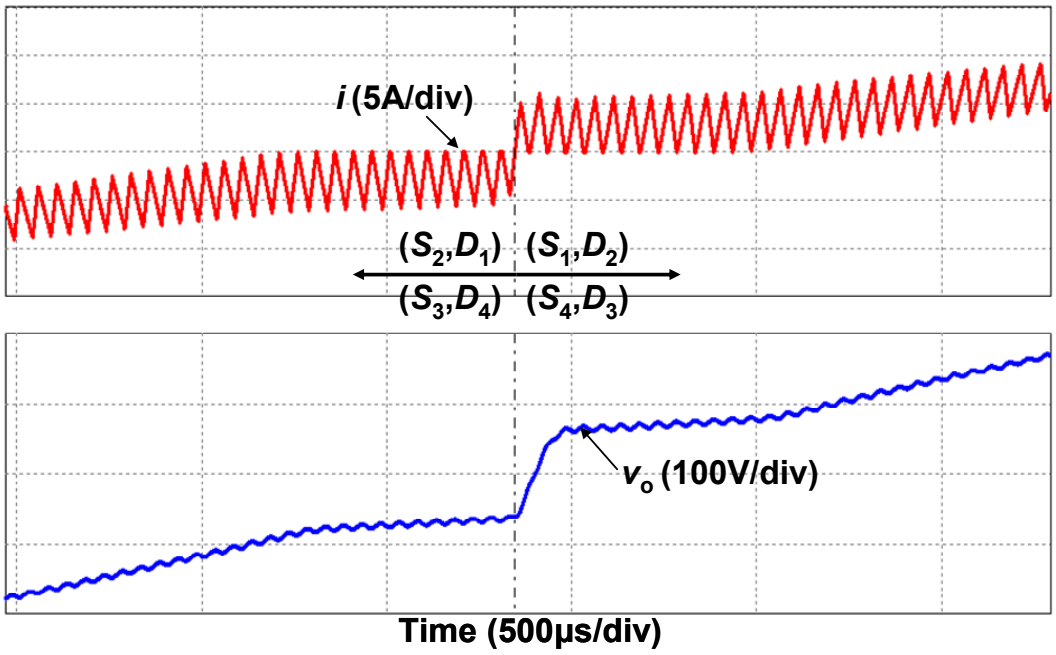
It can be seen that at the zero-crossing period, D_s is approaching 0.5. Therefore, the current ripple at zero-crossing region is not zero. The same analysis applies to the negative half-cycle current. When the positive half-cycle current connects with the negative half-cycle current, it will create a jump. The current jump at zero-crossing will reflect on a voltage jump on the output capacitor. At zero-crossing region, D_s is almost 0.5, and v_o is very small compared to V_{dc}. Therefore, (3.1) can be rewritten as (3.2) with consideration of both positive and negative half-cycles.

$$\Delta i \approx \text{sgn}(v_o)\frac{V_{dc} D_s T_s}{L + L_f} \tag{3.2}$$

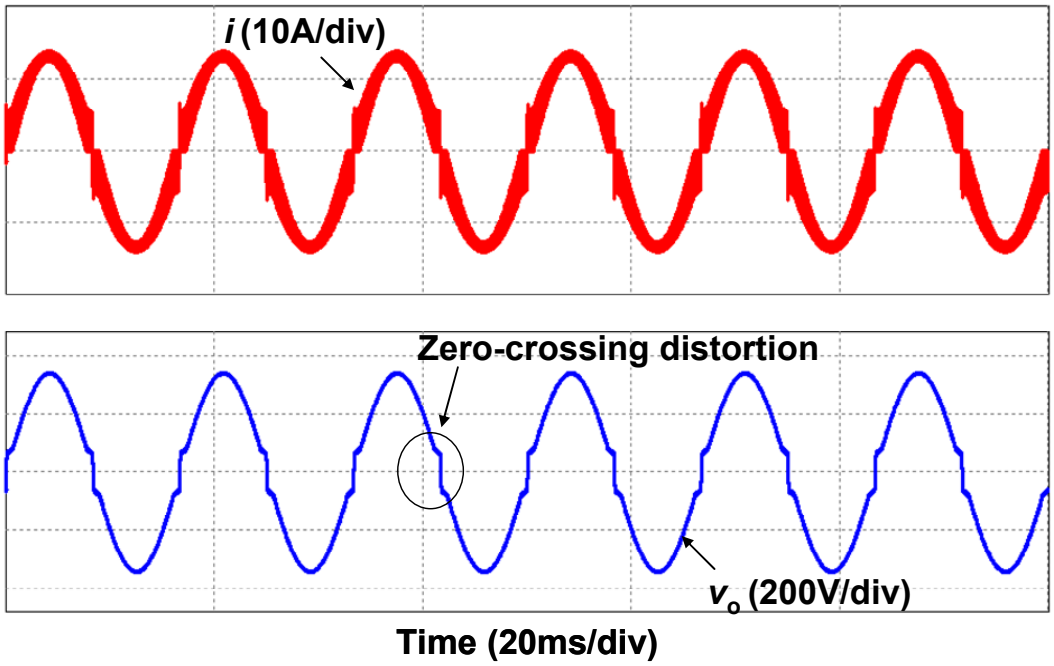
Where $\text{sgn}(v_o)$ is defined as

$$\text{sgn}(v_o) = \begin{cases} 1 & v_o > 0 \\ -1 & v_o < 0 \end{cases} \tag{3.3}$$

Fig. 3.6 shows the simulation result of output current i and output voltage v_o across the load under traditional bipolar SPWM. The dc bus voltage is 380V, and the output voltage is 240V. With larger V_{dc}, the current ripple is higher, which means the current zero-crossing distortion is worse at higher dc bus voltage. Since the load is resistor, the output current i_o through load has the same shape as v_o, and thus has the distortion.



(a) Output waveforms at zero-crossing period



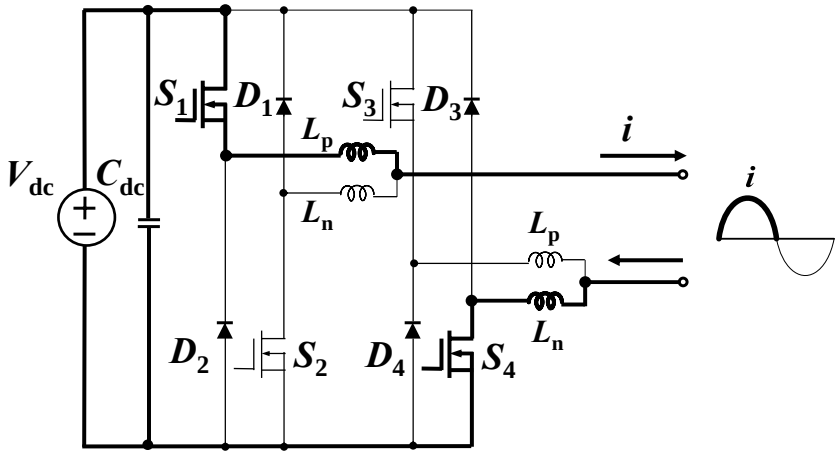
(b) Output current and voltage waveforms

Fig. 3.6: Simulation result of dual-buck full-bridge inverter under traditional bipolar SPWM.

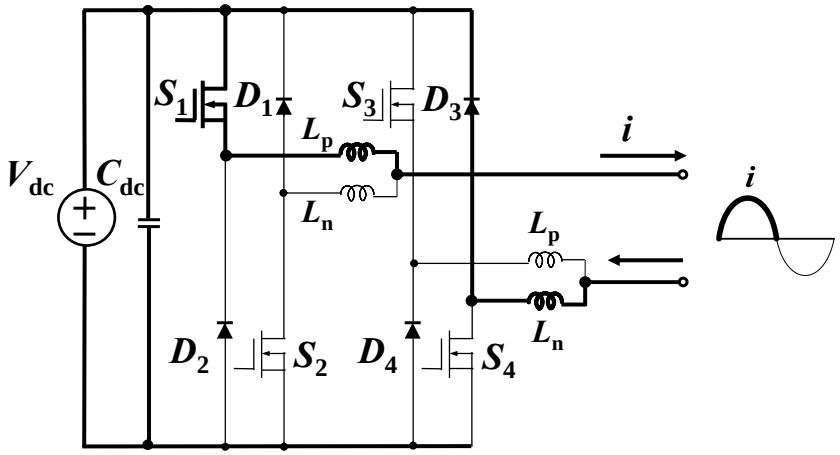
It is also clear that with traditional bipolar SPWM, all the active switches operate at high switching frequency. For example, at the positive half cycle, S_1 and S_4 are turned on and off at the same time within every switching period. This leads to higher switching losses. In addition, under this PWM scheme, the current ripple is higher, which results in higher losses in filter components as well.

To address the issues of zero-crossing distortion and higher switching losses caused by traditional bipolar PWM, an asymmetrical half-cycle unipolar (AHCU) PWM scheme is proposed for dual-buck full-bridge inverter. Fig. 3.7 shows the operation modes of dual-buck full-bridge inverter under this new PWM. When the output current is at the positive half cycle, S_1 is always turned on, shown in Fig. 3.7 (a) and (b). S_4 is the switching device

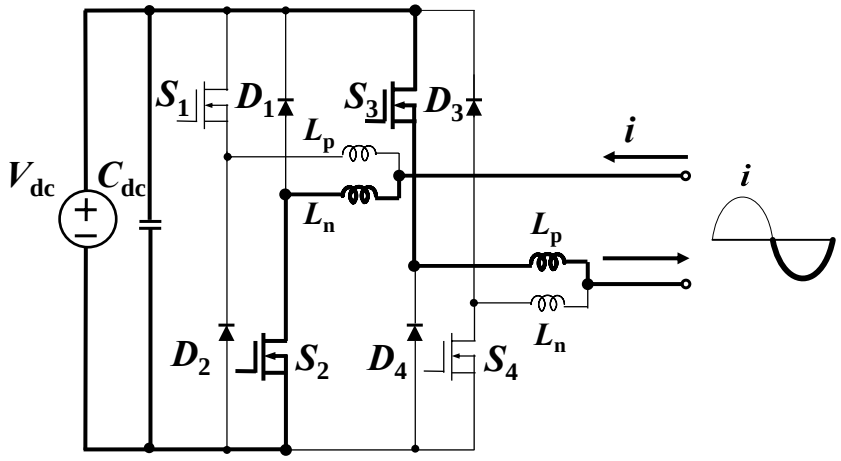
for this positive half cycle. When S_4 is on, the output voltage is V_{dc}, and when it is off, D_3 freewheels with output voltage equal to zero. Likewise, when the output current is at the negative half cycle, S_2 is kept on, with S_3 and D_4 working at the switching frequency, shown in Fig. 3.7 (c) and (d). The output PWM voltage is $-V_{dc}$ and zero.



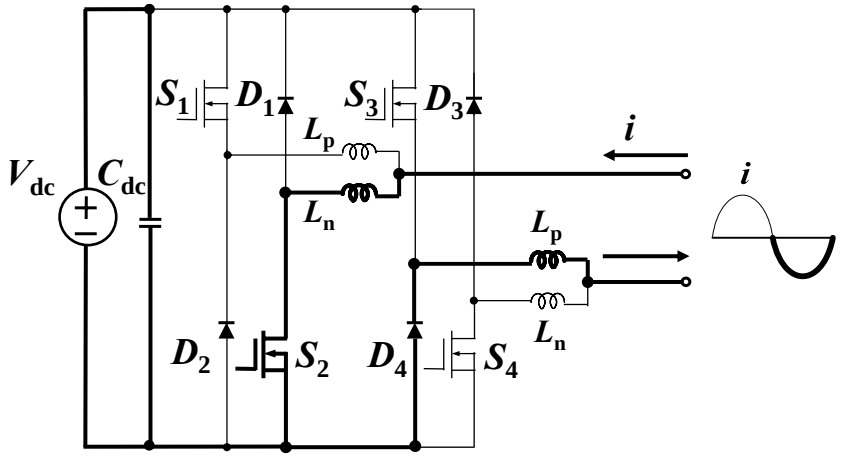
(a) Positive current, S_1 and S_4 turned on



(b) Positive current, S_1 on and D_3 free-wheeling



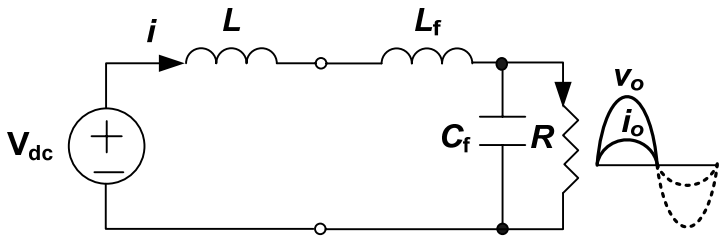
(c) Negative current, S_2 and S_3 turned on



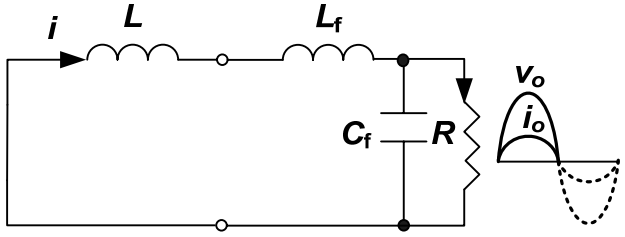
(d) Negative current, S_2 on and D_4 free-wheeling

Fig. 3.7: Operation modes under AHCU PWM.

Fig. 3.8 shows the equivalent circuit under this PWM at the output current positive half cycle, which relates to the operation mode in Fig. 3.7 (a) and (b). Fig. 3.8 shows the gate signal of S_1 and S_4, and the current through output inductor i. The shaded area of Fig. 3.9 corresponds to the operation mode shown in Fig. 3.7 (a). D_{sH} is the duty cycle for the switch S_4, and under this AHCU PWM, $0 \le D_{sH} \le 1$.



(a) S_1 and S_4 on



(b) S_1 on and D_3 freewheeling

Fig. 3.8: Equivalent circuit under AHCU PWM when output current is positive.

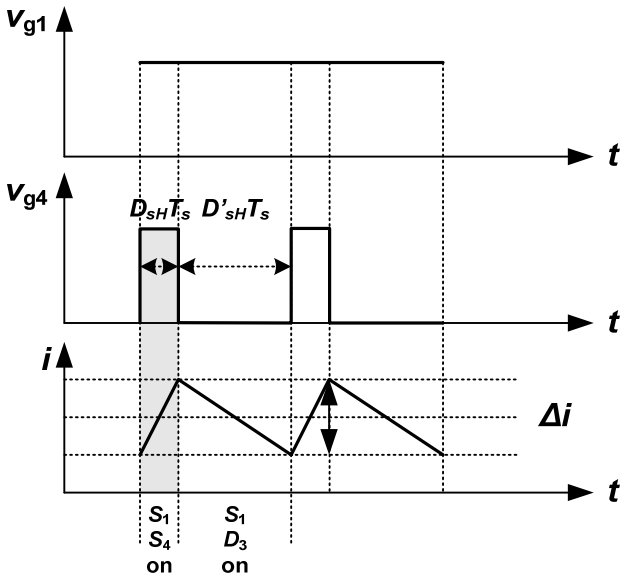


Fig. 3.9: Gate signal of S_1 and S_4 with current i through output inductor.

The current ripple of i can be derived from Fig. 3.8 and Fig. 3.9 as follows:

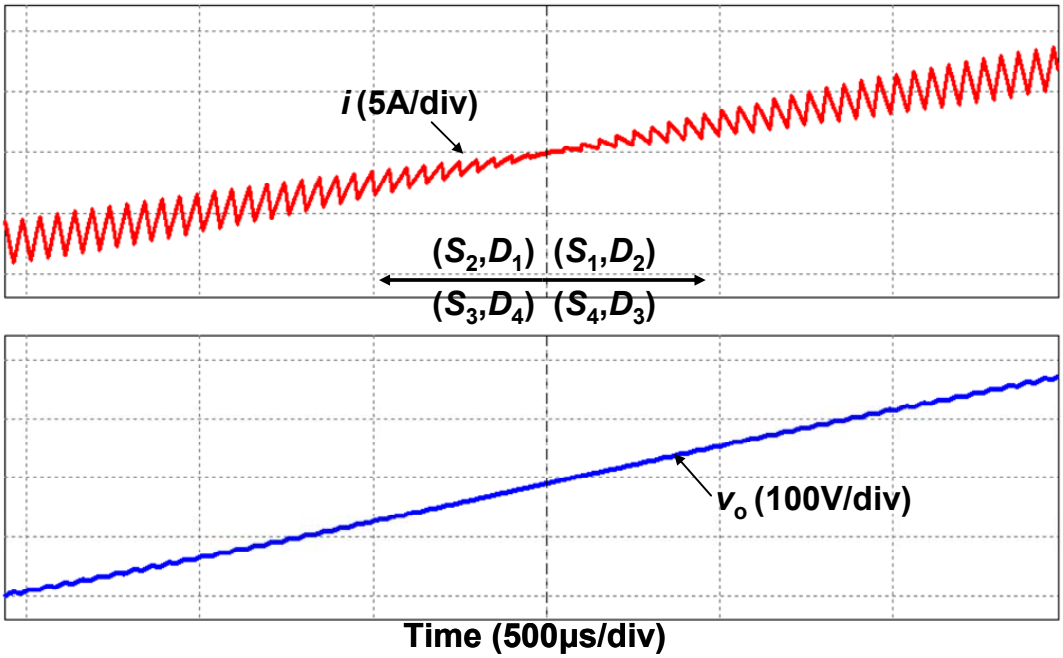
$$\Delta i = \frac{(V_{dc} - v_o) D_{sH} T_s}{L + L_f} \tag{3.4}$$

where $T_s = \frac{1}{f_s}$, f_s is the switching frequency of S_4.

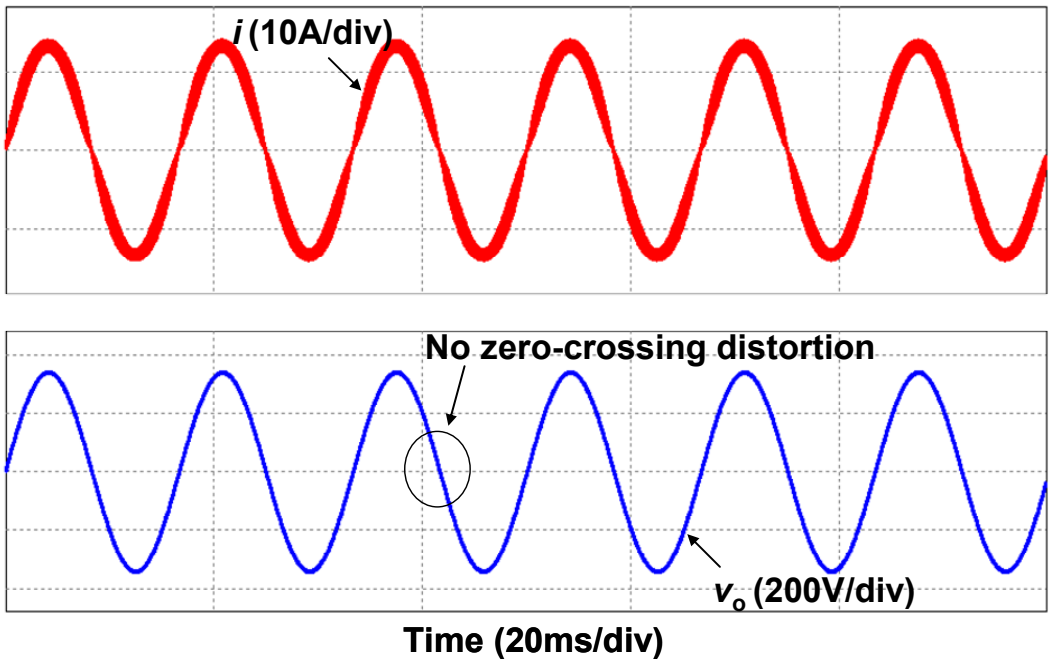
Compared to the current ripple equation (3.1) for traditional bipolar SPWM, it is clear that at zero-crossing period, the current ripple under this PWM is close to zero because D_{sH} is close to zero even though V_{dc} is high. Theoretically, when the positive half-cycle current connects with the negative half-cycle current, there is no current jump at all at zero-crossing region. At zero-crossing region, D_{sH} is almost 0, and v_o is very small compared to V_{dc}. Therefore, (3.4) can be reconstructed as (3.5) with consideration of both positive and negative half-cycles.

$$\Delta i \approx \text{sgn}(v_o)\frac{V_{dc}D_{sH}T_s}{L+L_f} \tag{3.5}$$

Fig. 3.10 shows the simulation result of output current i and output voltage v_o across the load under proposed PWM. All the simulation settings are the same with the one for Fig. 3.6 except the PWM. As can be seen, the zero-crossing distortion is practically eliminated.



(a) Output waveforms at zero-crossing period

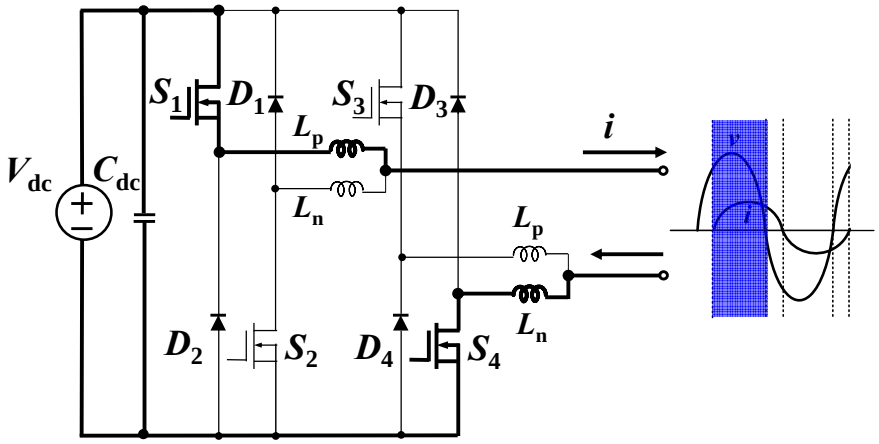


(b) Output current and voltage waveforms

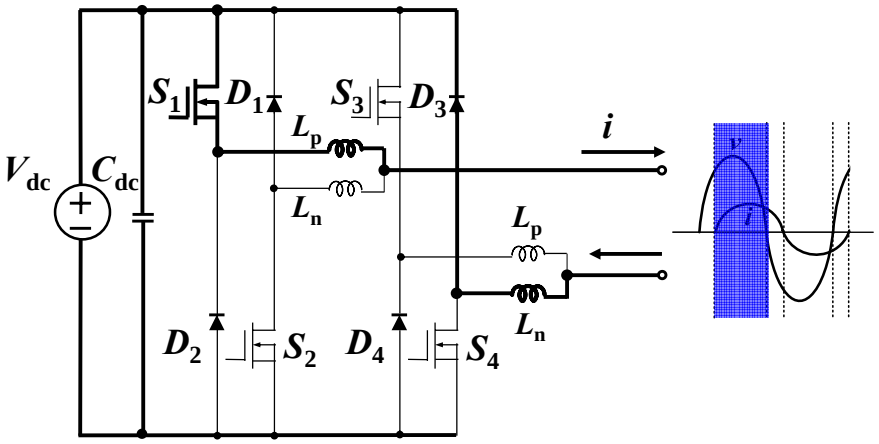
Fig. 3.10: Simulation result of dual-buck full-bridge inverter under AHCU PWM.

From Fig. 3.7 and Fig. 3.9, we can see that under this AHCU PWM scheme, only one active switch operates at switching frequency at any instant. Compared to the traditional bipolar SPWM where two active switches run at switching frequency, the switching loss of the devices is theoretically cut down by half.

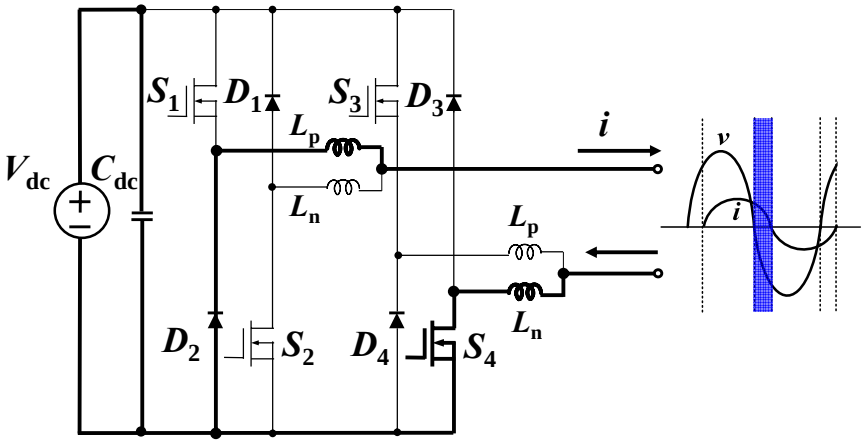
Fig. 3.7 describes the AHCU PWM operation when the load is resistive or in other words in unity power factor. Under this AHCU PWM technique, if the load is reactive, which means the output voltage is leading the output current, the operation modes will be different from Fig. 3.7. In order to adapt to reactive load, extra operation modes need to be included. Fig. 3.11 shows the operation modes under AHCU PWM with reactive loads. Compared to Fig. 3.7 with resistive load, S_1 and S_2 are still fundamental-line-frequency switches, while S_3 and S_4 are high-speed PWM switches. Because the polarity combination of the output current and voltage increases to four states, there are periods where S_1 and S_2 need to be turned off when the output current and voltage have opposite polarities. When both the output current and voltage are positive, S_1 is always turned on, shown in Fig. 3.11 (a) and (b). S_4 is the switching device for this period. When S_4 is on, the output voltage is V_{dc}, and when it is off, D_3 freewheels with output voltage equal to zero. When the output current is positive and the output voltage is negative, in order to generate the negative voltage, S_1 is turned off, and thus D_2 is always on during this period, shown in Fig. 3.11 (c) and (d). S_4 and D_3 are still the high speed switching devices. When S_4 is on, the output voltage is zero, and when it is off, D_3 freewheels with the output voltage equal to $-V_{dc}$. Similarly, when the output current is at the negative half cycle, S_2 and D_1 are either on or off depending on the voltage polarity, with S_3 and D_4 working at the switching frequency, shown in Fig. 3.11 (e) to (h).



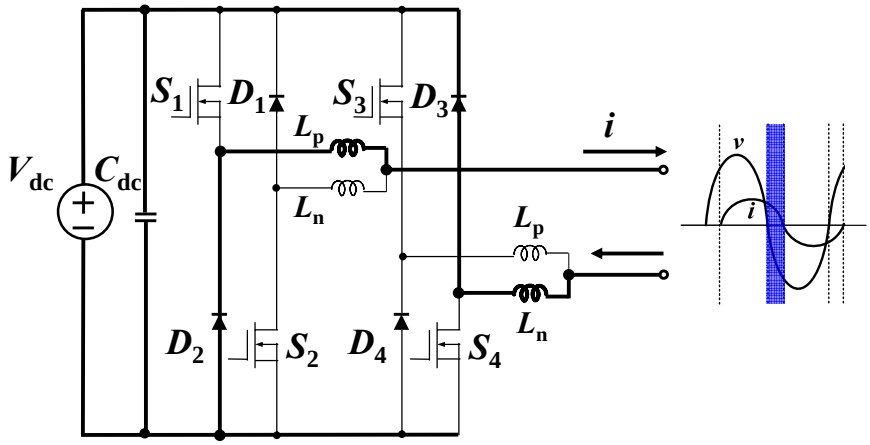
(a) Positive current, positive voltage, S_1 and S_4 turned on



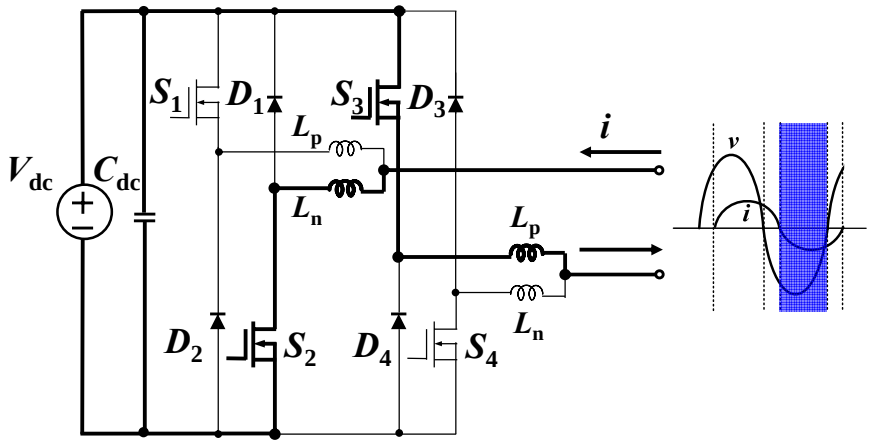
(b) Positive current, positive voltage, S_1 on and D_3 free-wheeling



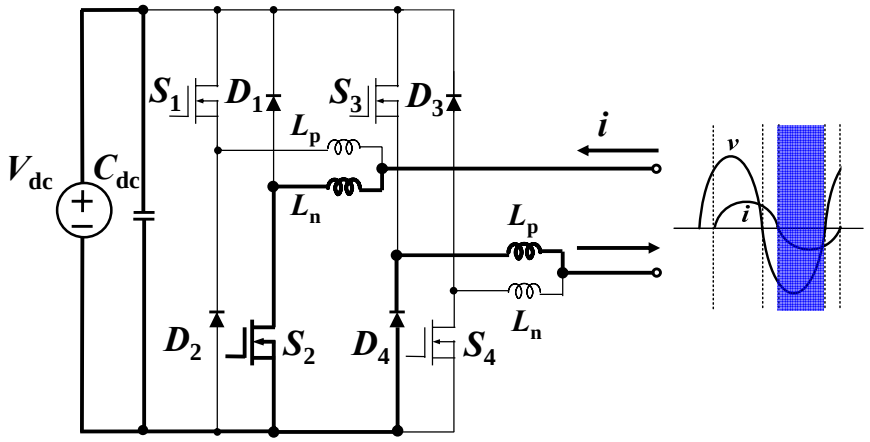
(c) Positive current, negative voltage, D_2 on and S_4 on



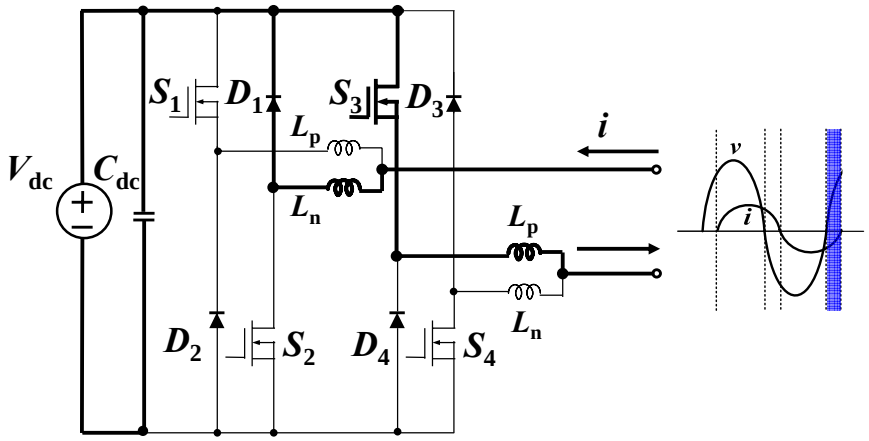
(d) Positive current, negative voltage, D_2 on and D_3 free-wheeling



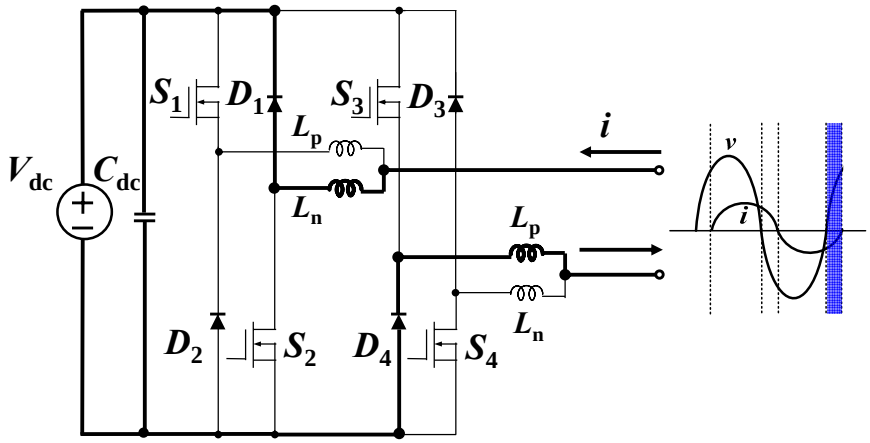
(e) Negative current, negative voltage, S_2 and S_3 turned on



(f) Negative current, negative voltage, S_2 on and D_4 free-wheeling



(g) Negative current, positive voltage, D_1 on and S_3 on

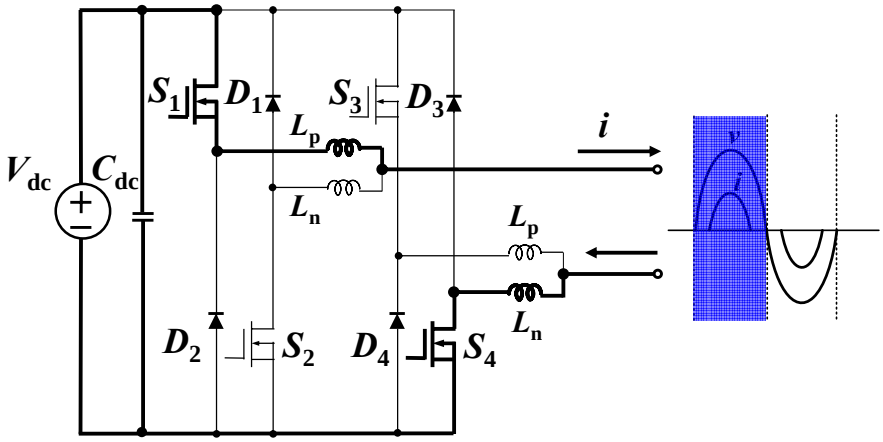


(h) Negative current, positive voltage, D_1 on and D_4 free-wheeling

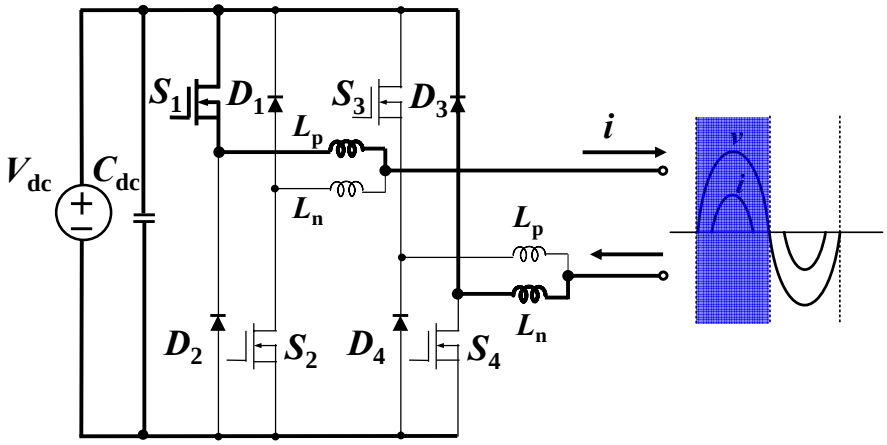
Fig. 3.11: Operation modes under AHCU PWM with reactive loads.

Fig. 3.12 describes the operation modes under AHCU PWM with non-linear loads. The rectifier non-linear load is used as an example here with current characteristics drawn in Fig. 3.12. When the output current is equal or greater than zero, and the output voltage is positive, S_1 is always turned on, and S_4 is the high-switching frequency device, shown in Fig. 3.12 (a) and (b). Similarly, when the output current is equal or less than zero, and the output voltage is negative, S2 is always turned on, and S3 is the high-switching frequency

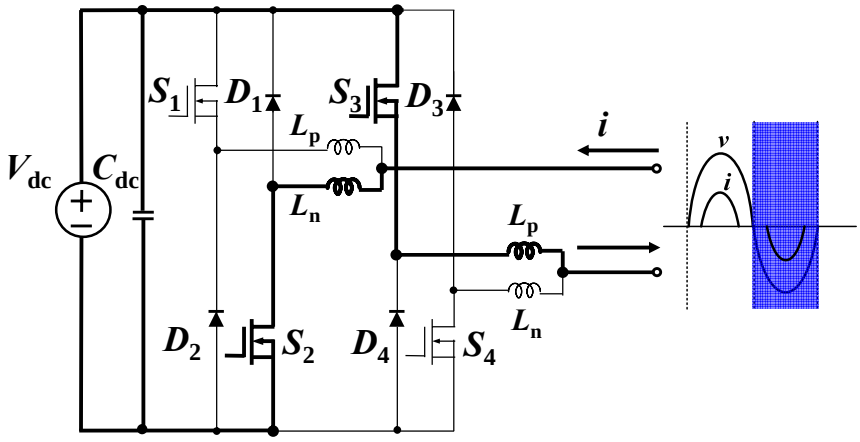
device, shown in Fig. 3.12 (c) and (d).



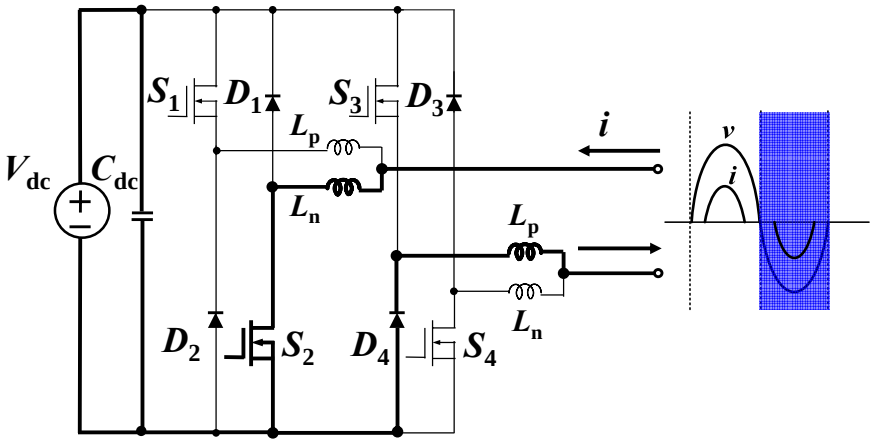
(a) $i \geq 0$, positive voltage, S_1 and S_4 turned on



(b) $i \geq 0$, positive voltage, S_1 on and D_3 free-wheeling



(c) $i \leq 0$, negative voltage, S_2 and S_3 turned on



(d) i≤0 , negative voltage, S_2 on and D_4 free-wheeling

Fig. 3.12: Operation modes under AHCU PWM with non-linear loads.

In terms of current ripple reduction, compare (3.1) and (3.4): if the switching frequency and filter components are the same, the current ripple ratio γ can be obtained as follows

$$\gamma = \frac{\Delta i_{HPWM}}{\Delta i_{SPWM}} = \frac{D_{sH}}{D_s} \tag{3.6}$$

The relationship between D_s and D_{sH} is established below

$$D_s = \frac{D_{sH} + 1}{2} \tag{3.7}$$

Therefore, from (3.6) and (3.7), we can derive

$$\gamma = \frac{2D_{sH}}{D_{sH} + 1} \tag{3.8}$$

Fig. 3.13 shows the current ripple ratio curve under different duty cycles. From Fig. 3.13 we can see that at zero-crossing, the ratio reaches the lowest, zero and climbs up when D_{sH} increases. At any given point below duty cycle 1, the current ripple of AHCU PWM is smaller than that of bipolar SPWM. This conclusion can also be verified by the simulation results from Fig. 3.6 and Fig. 3.10. This indicates that the proposed PWM can

reduce ripple related filter losses over the entire output current range.

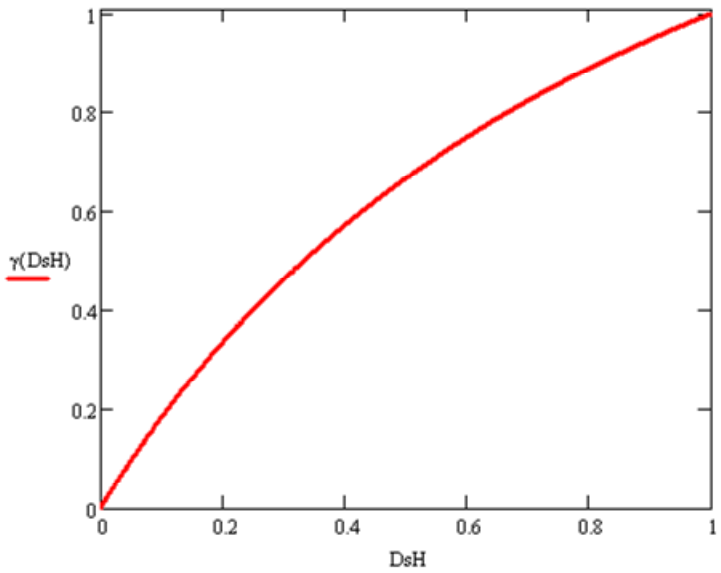


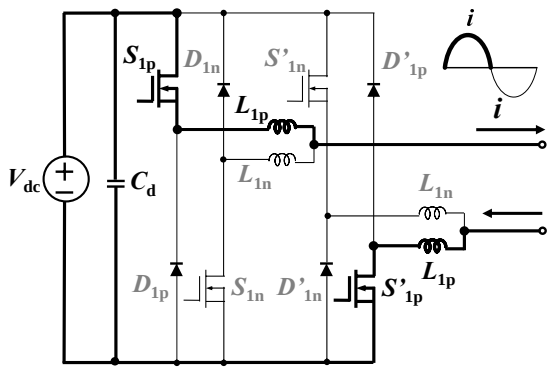
Fig. 3.13: Current ripple ratio between AHCU PWM and bipolar SPWM.

3.3 PWM Evaluation for Cascade Dual-Buck Full-Bridge Inverter

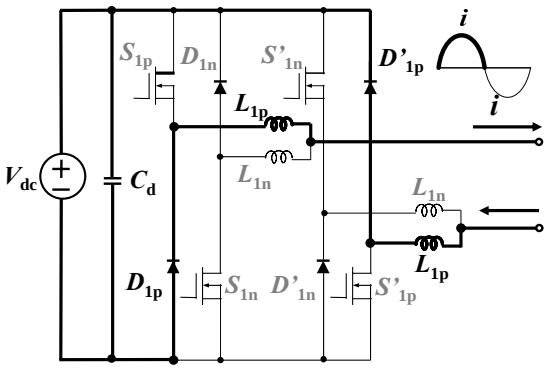
Fig. 3.14 shows the operation modes of a single unit of the cascade dual-buck full-bridge inverter under bipolar PWM. (S_{1p}, D_{1p}) and (S'_{1p}, D'_{1p}) are a working pair, and operate at current positive half-cycle. S_{1p} and S'_{1p} share the same gating signal, and when they are turned on, V_{dc} is applied to the output; when they are turned off, D_{1p} and D'_{1p} free-wheel together, and $-V_{dc}$ is applied to the output. Similarly, (S_{1n}, D_{1n}) and (S'_{1n}, D'_{1n}) are a working pair, and operate at current negative half-cycle.

Fig. 3.15 shows the operation modes of a single unit of the cascade dual-buck full-bridge inverter under the AHCU PWM proposed in the previous section. In the analysis of PWM schemes for cascade dual-buck full-bridge inverters, we use 'unipolar PWM' as the name for the AHCU PWM proposed in chapter 3.2. At current positive half-cycle, S_{1p} is always turned on, and (S'_{1p}, D'_{1p}) is the switching pair. When S'_{1p} is turned on, V_{dc} is applied to the output. When S'_{1p} is turned off, D'_{1p} free-wheels, and zero voltage is applied to the output. Similarly, S_{1n} and (S'_{1n}, D'_{1n}) operate at current negative half-cycle.

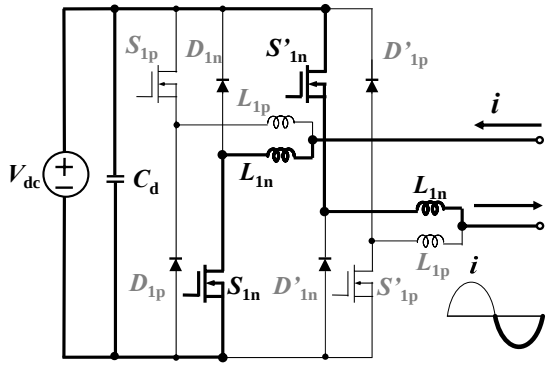
It can be noticed that no matter what PWM applied to the circuit, the body diode of the MOSFET never conducts, and the external diodes D_{1p}, D'_{1p}, D_{1n} and D'_{1n} can be independently selected with the features of fast reverse recovery to further minimize switching losses.



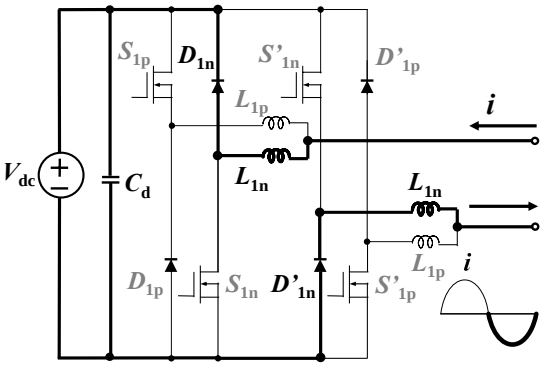
(a) Positive current, S_{1p} and S'_{1p} turned on



(b) Positive current, D_{1p} and D'_{1p} free-wheeling

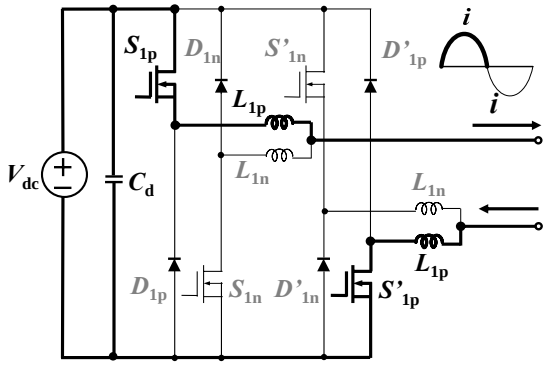


(c) Negative current, S_{1n} and S'_{1n} turned on

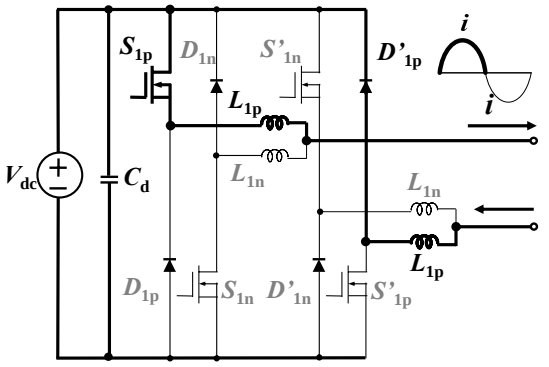


(d) Negative current, D_{1n} and D'_{1n} free-wheeling

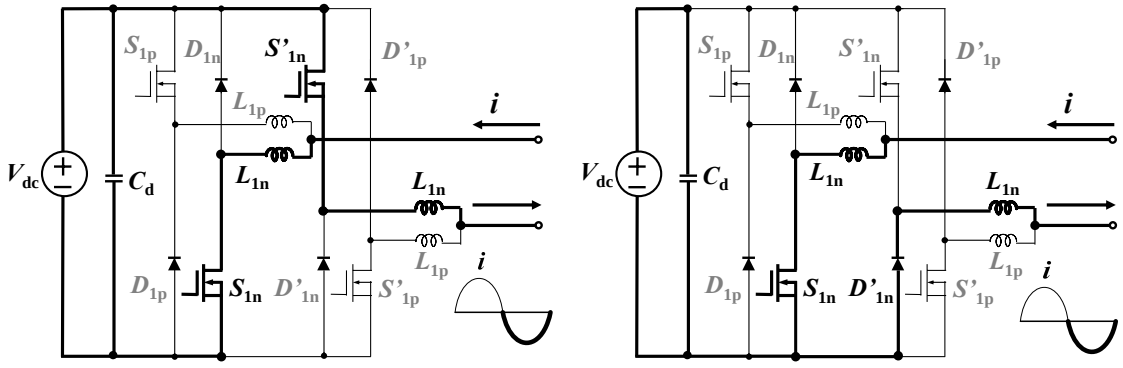
Fig. 3.14: Operation modes of single-unit dual-buck full-bridge inverter under bipolar PWM.



(a) Positive current, S_{1p} and S'_{1p} turned on



(b)Positive current, S_{1p} on and D'_{1p} free-wheeling

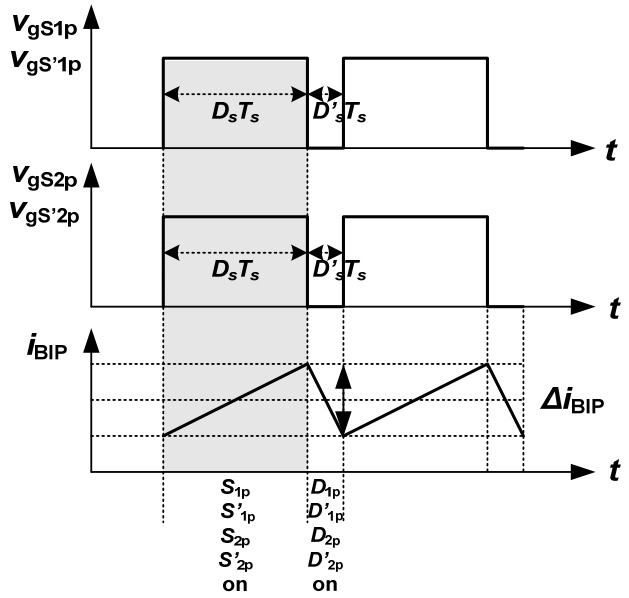


(c)Negative current, S_{1n} and S'_{1n} turned on (d)Negative current, S_{1n} on and D'_{1n} free-wheeling

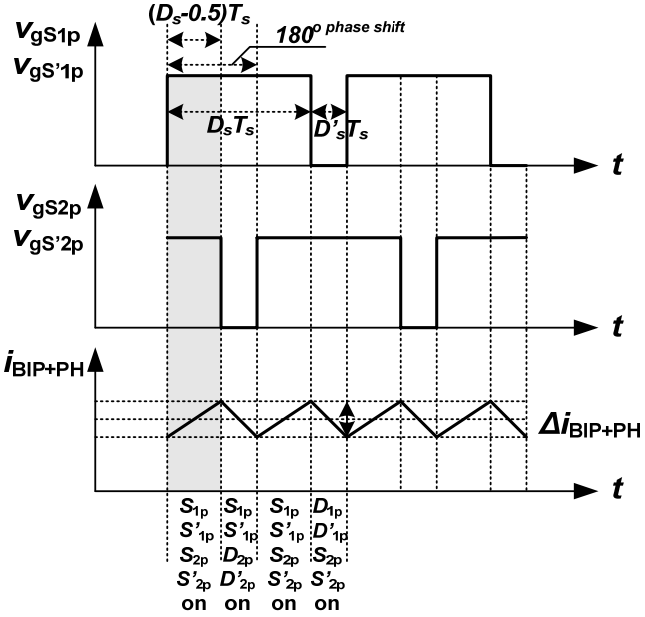
Fig. 3.15: Operation modes of single-unit dual-buck full-bridge inverter under unipolar PWM.

In this section, four different PWM schemes are analyzed for cascade dual-buck full-bridge inverter, including bipolar PWM, bipolar with phase-shifted PWM, unipolar PWM, and unipolar with phase-shifted PWM. The current ripple equations are derived and compared side by side.

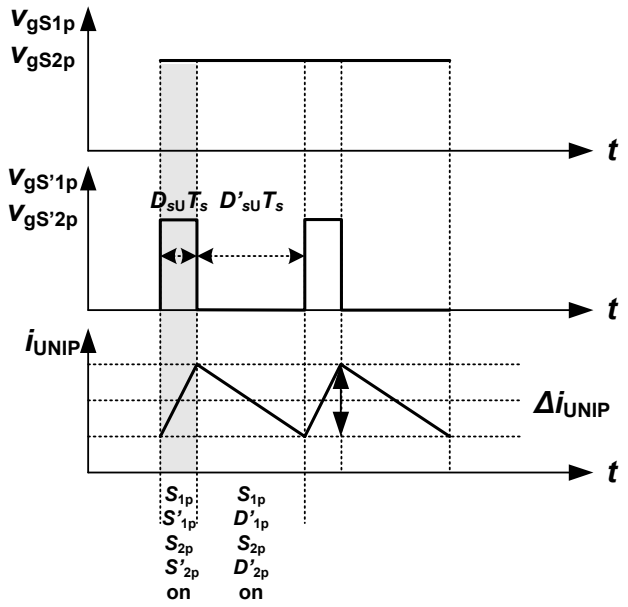
Fig. 3.16 shows the gating signals and the related current ripple information under different PWM schemes. The analysis is based on two dual-buck full-bridge units in cascade. D_s is the duty cycle for bipolar PWM ($0.5 \le D_s \le 1$), and at zero crossing, D_s is close to 0.5. D_{sU} is the duty cycle for unipolar PWM ($0 \le D_{sU} \le 1$), and at zero crossing, D_s is close to 0. All the states of the switches are provided underneath each output current figure. For two-unit cascade inverter, the phase shift angle is 180^o (360^o/N). The abbreviations BIP, BIP+PH, UNIP, UNIP+PH stand for bipolar, bipolar with phase-shift, unipolar and unipolar with phase-shift, respectively.



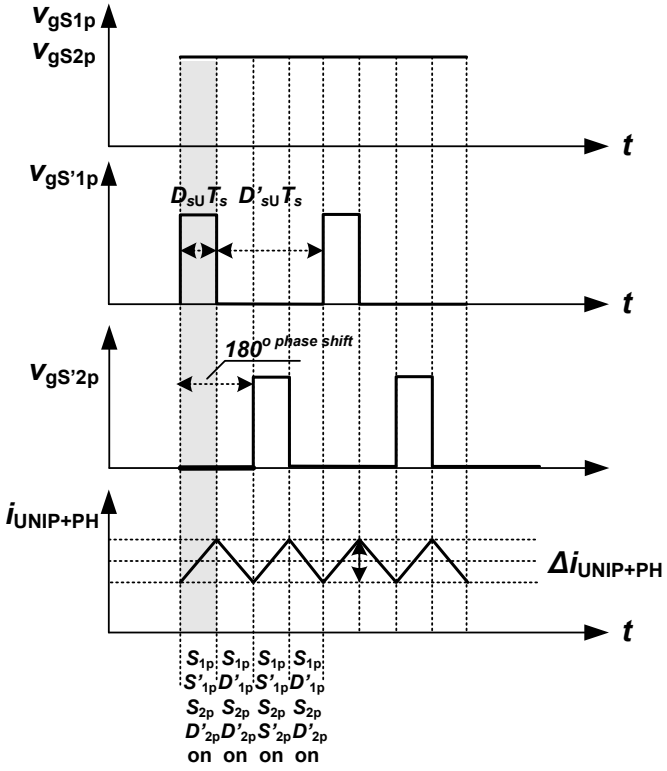
(a) Bipolar PWM



(b) Bipolar with phase-shifted PWM



(c) Unipolar PWM



(d) Unipolar with phase-shifted PWM

Fig. 3.16: Gating signals and current ripple under different PWM schemes.

Equations (3.9) to (3.12) provide the current ripple information for bipolar PWM, bipolar with phase-shifted PWM, unipolar PWM, and unipolar with phase-shifted PWM respectively under the assumption that L_{1p}=L_{2p}. As can be seen from (3.9), there will be current zero-crossing distortion for bipolar PWM because at zero-crossing D_s is 0.5. When bipolar PWM is phase-shifted for the second unit, as in (3.10), the current ripple will be zero at zero-crossing period. For unipolar PWM from (3.11), because D_{sU} is already zero at zero-crossing, there is no ripple current. The zero distortion is also true for unipolar phase-shifted PWM in (3.12). Besides zero-crossing improvement, the phase-shifted PWM also helps reduce the current ripple when it is applied to both bipolar and unipolar PWMs, which would lead to efficiency improvement.

$$\Delta i_{BIP} = \frac{(2V_{dc} - v_o)D_s T_s}{4L_{1p} + L_f} \tag{3.9}$$

$$\Delta i_{BIP+PH} = \frac{(2V_{dc} - v_o)(D_s - 0.5)T_s}{4L_{1p} + L_f} \tag{3.10}$$

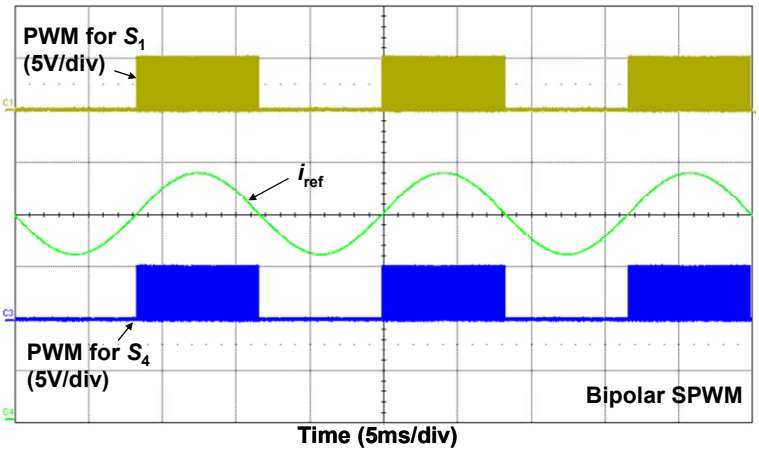
$$\Delta i_{UNIP} = \frac{(2V_{dc} - v_o)D_{sU} T_s}{4L_{1p} + L_f} \tag{3.11}$$

$$\Delta i_{UNIP+PH} = \frac{(V_{dc} - v_o)D_{sU} T_s}{4L_{1p} + L_f} \tag{3.12}$$

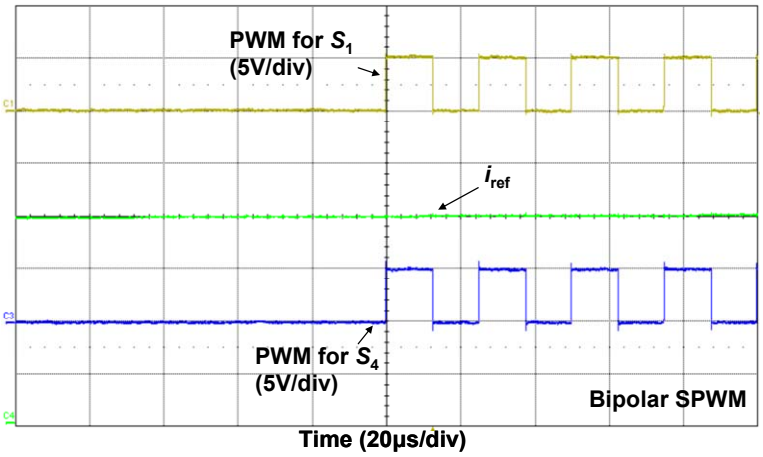
3.4 Comparative Experimental Results for Single-Unit Dual-Buck Full-Bridge Inverter

To prove the viability and merits of the proposed AHCU PWM, a 2kW, 240Vac output dual-buck full-bridge inverter system in standalone operation was designed and tested. For comparison, tests were conducted for both traditional bipolar SPWM and AHCU PWM. The dc bus voltage is 380V. The switching frequency is 40kHz. All the devices are rated 600V. The MOSFET is selected as STY80NM60N with on-resistance 35mΩ, and the diode is RURG3060 with reverse recovery time 55ns. The passive components are selected as follows: L_p=L_n=250μH, L_f=1mH, C_f=2.4μF. The load is a variable resistive load bank. The system controller and PWM generation are conducted by TI floating point DSP TMS320F28335.

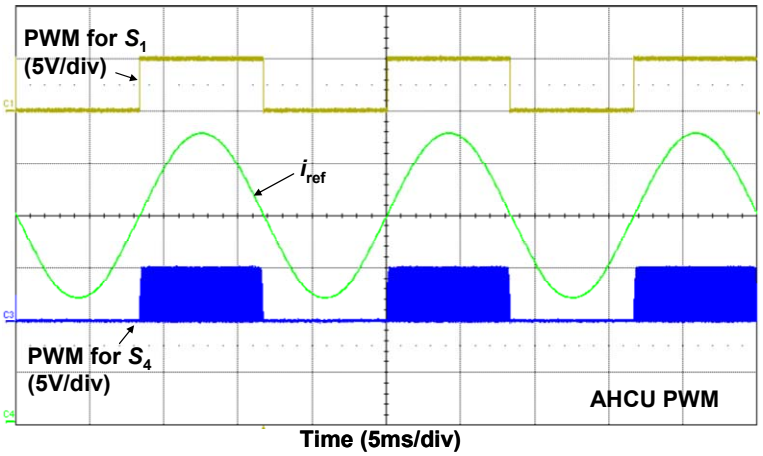
Fig. 3.17 shows the gate signals for both traditional bipolar SPWM and AHCU PWM operating at the positive half cycle of output current reference. It can be seen that at the positive half cycle, S_1 never switches under AHCU PWM, which saves the switching loss by half. In addition, the AHCU PWM for S_4 starts to increase from zero pulse width at zero-crossing, which leads to current ripple cut-down.



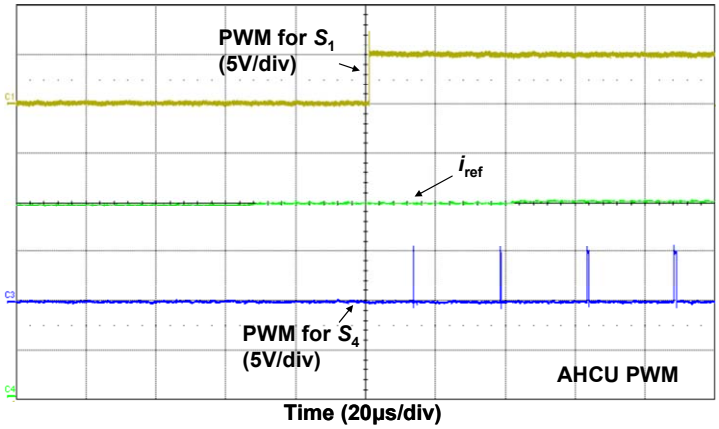
(a) Gate signals for bipolar SPWM



(b) Gate signals for bipolar SPWM at zero-crossing period



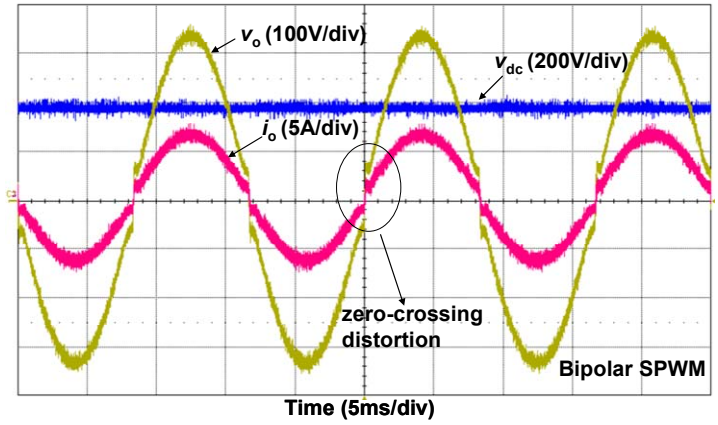
(c) Gate signals for AHCU PWM



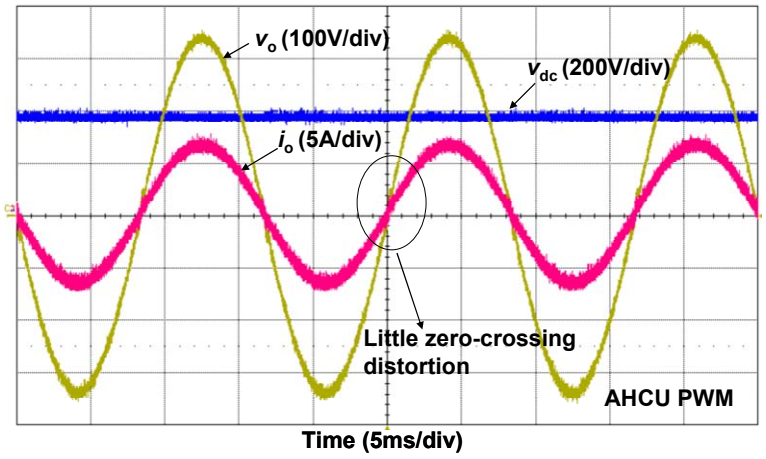
(d) Gate signals for AHCU PWM at zero-crossing period

Fig. 3.17: Gate signals with bipolar SPWM and AHCU PWM.

Fig. 3.18 shows the output voltage v_o and output current i_o waveforms for both bipolar SPWM and AHCU PWM. The zero-crossing distortion is obvious for bipolar SPWM, while AHCU PWM greatly compensates for this distortion. Fig. 3.19 shows the comparison at smaller load condition, 500W. It can be seen due to the reduced load, the zero-crossing distortion is quite severe and unacceptable for bipolar SPWM. On the other hand, by using AHCU PWM, the zero-crossing distortion is alleviated at light load conditions.

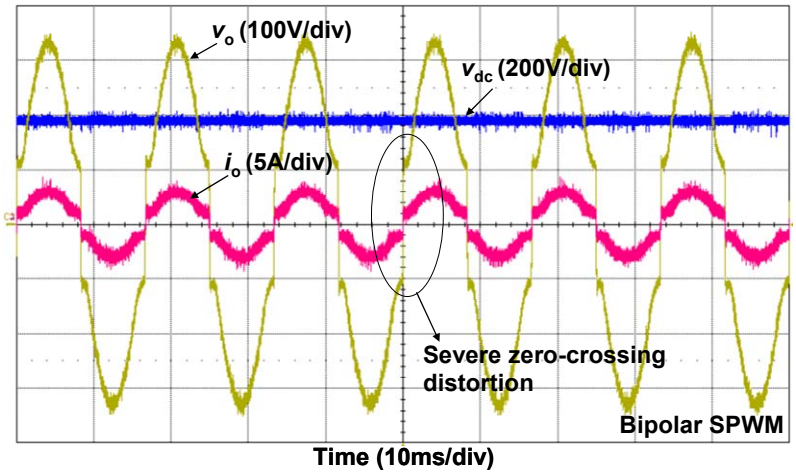


(a) Output waveforms under bipolar SPWM

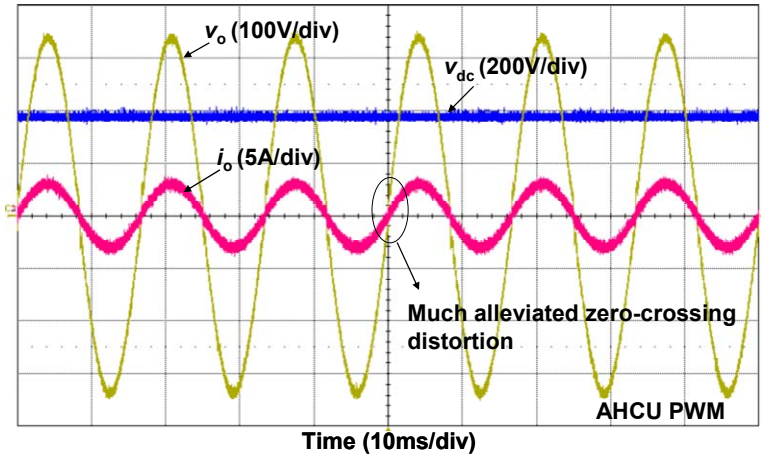


(b) Output waveforms under AHCU PWM

Fig. 3.18: Output current and voltage waveforms with bipolar SPWM and AHCU PWM.



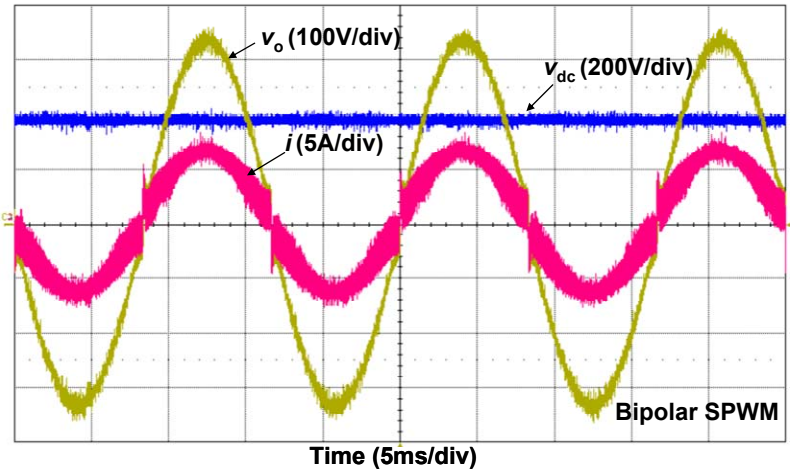
(a) Output waveforms under bipolar SPWM



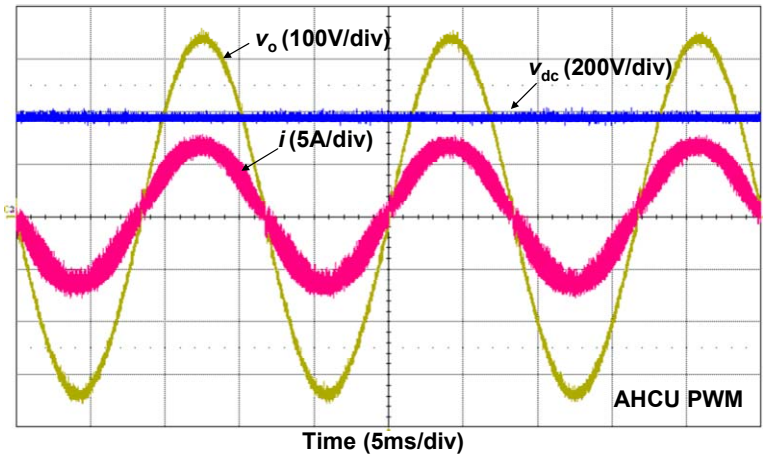
(b) Output waveforms under AHCU PWM

Fig. 3.19: Output current and voltage waveforms under light load condition.

Fig. 3.20 shows the output voltage v_o and the output current i before filtering for both bipolar SPWM and AHCU PWM. It can be seen that the current ripple under AHCU PWM is smaller than that of bipolar SPWM, which means less losses in filter components.



(a) Output waveforms under bipolar SPWM



(b) Output waveforms under AHCU PWM

Fig. 3.20: Output current i and voltage v_o under bipolar SPWM and AHCU PWM.

Another benefit for the AHCU PWM is efficiency improvement. In order to show the difference between two PWM schemes, efficiency experiments were conducted.

Fig. 3.21 shows measured efficiency curves under different power output conditions for bipolar SPWM and AHCU PWM. The switching frequency is 40kHz, and the output voltage is 240V for all test points. The efficiency measurement was performed through light load until full load 2.4 kW conditions. It can be seen that AHCU PWM improves the efficiency by an average of 0.6% compared to bipolar SPWM at the same test condition. The saving includes both switching loss in active devices and current ripple related loss in passive filter components. The peak efficiency of the inverter with AHCU PWM is 98.4%.

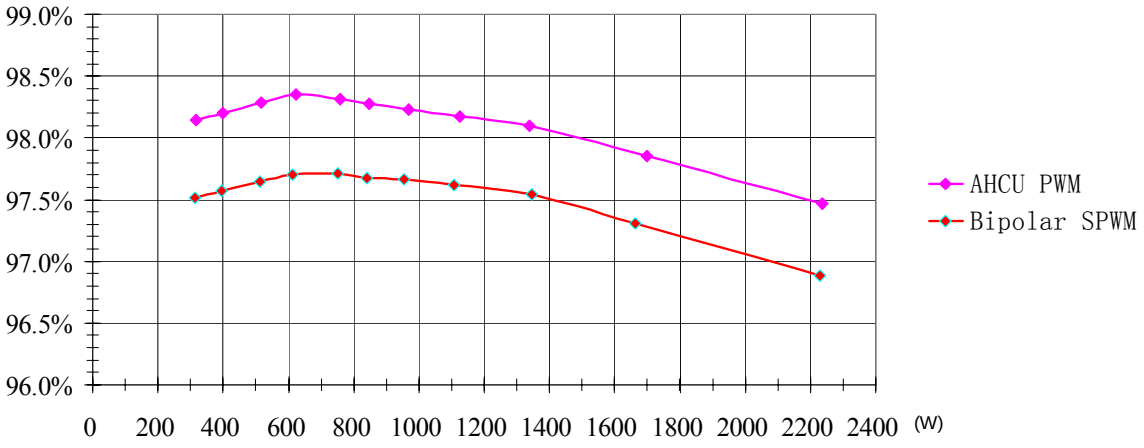
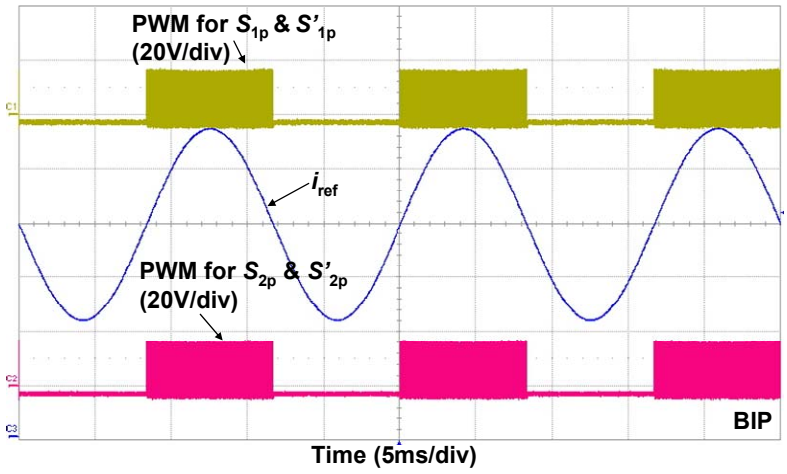


Fig. 3.21: Efficiency comparison between bipolar SPWM and AHCU PWM.

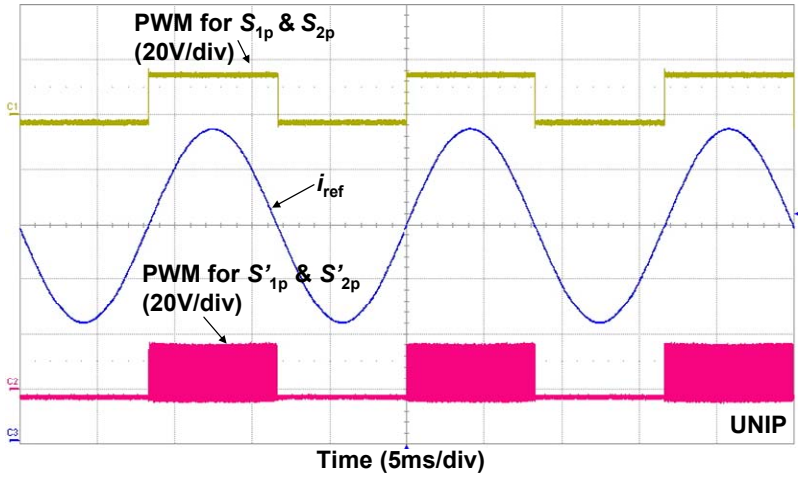
3.5 Comparative Experimental Results for Cascade Dual-Buck Full-Bridge Inverter

A 1kW, 240Vac output cascade dual-buck full-bridge inverter with two cascade units has been built and tested. The dc bus voltage for each cell is 190V, and the parameters of the passive components are as follows: L_{jp}=L_{jn}=250μH, L_f=1mH, C_f=2.4μF. The switching frequency is 20 kHz. The MOSFET is selected as IPW60R045CP with on-resistance 45mΩ, and the diode is APT30DQ60BG with reverse recovery time 30ns, and forward voltage drop 2V. The system control and PWM generation are conducted by TI floating point DSP TMS320F28335.

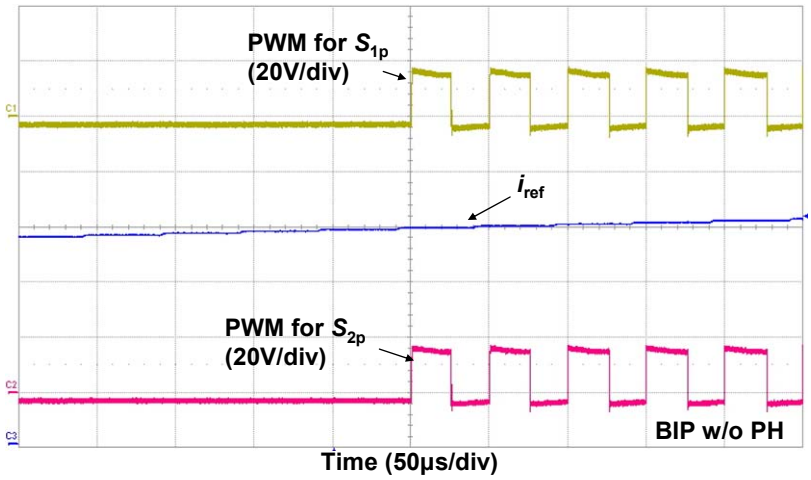
Fig. 3.22 shows the gate signals generated for different PWM methods. Only the positive half-cycle PWMs are shown, and the PWMs for negative half-cycle are symmetrical. Fig. 3.22 (c) to (f) are detailed PWMs at switching frequency time frame. For two-unit cascade inverter, the phase shift angle is 180°.



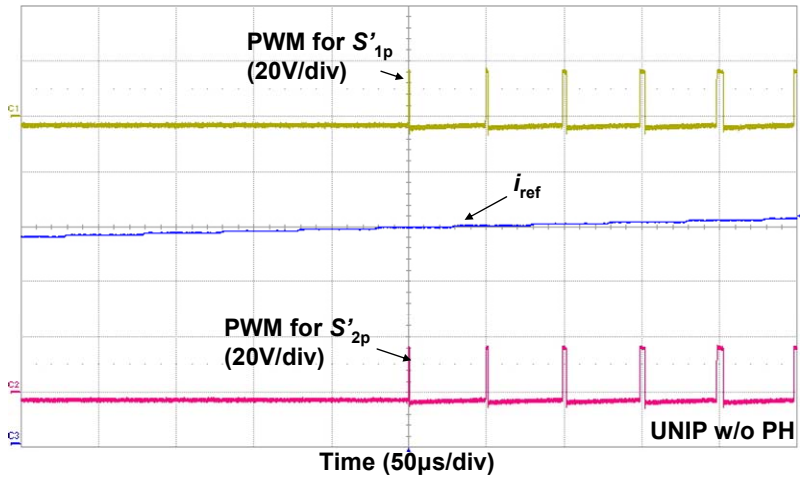
(a) Bipolar PWM



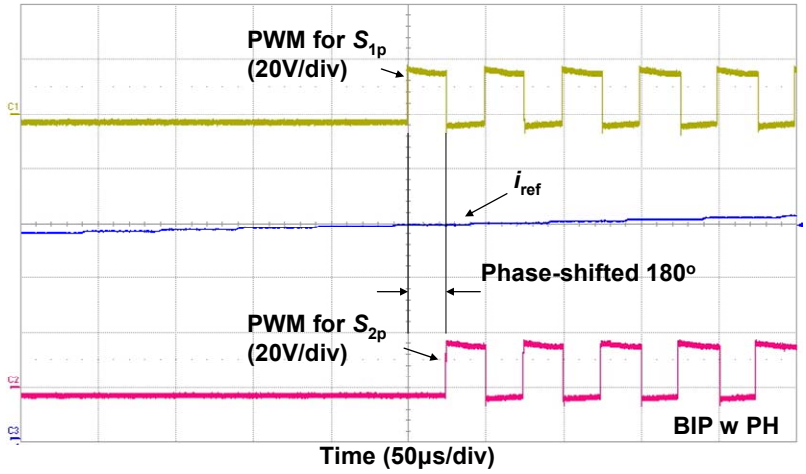
(b) Unipolar PWM



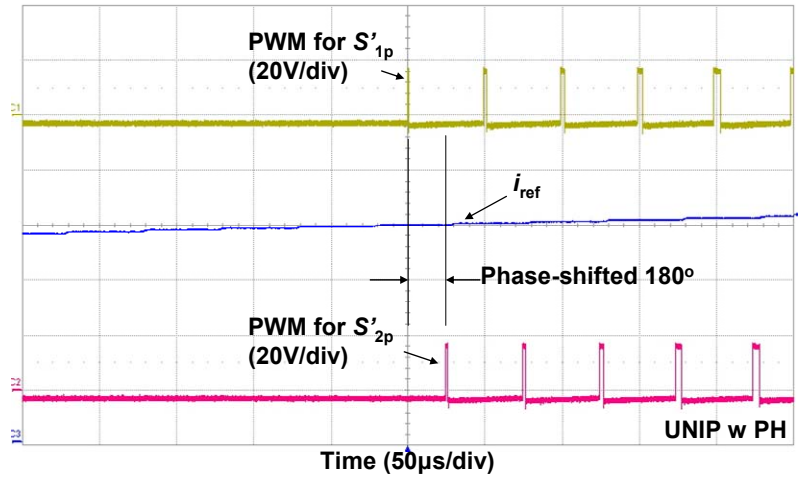
(c) Bipolar without phase-shifted PWM



(d) Unipolar without phase-shifted PWM



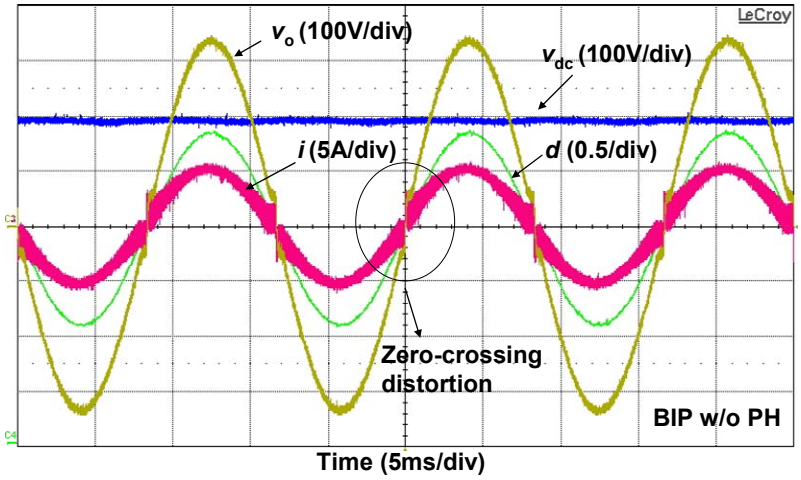
(e) Bipolar with phase-shifted PWM



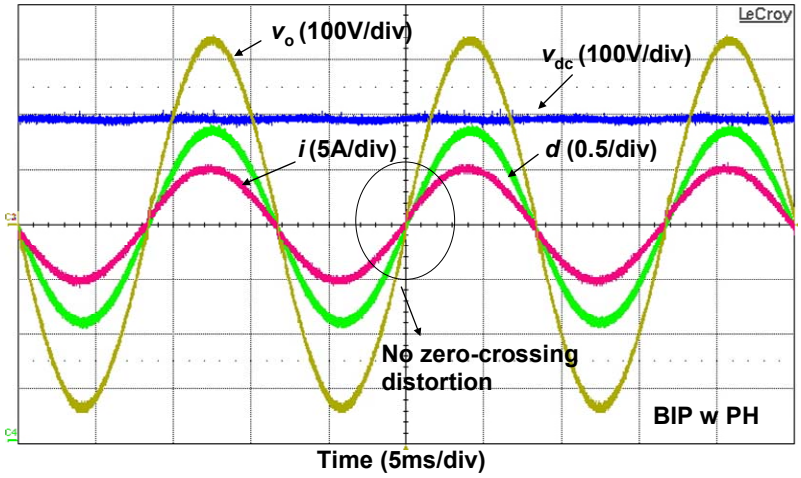
(f) Unipolar with phase-shifted PWM

Fig. 3.22: Different PWM generations for cascade dual-buck full-bridge inverter.

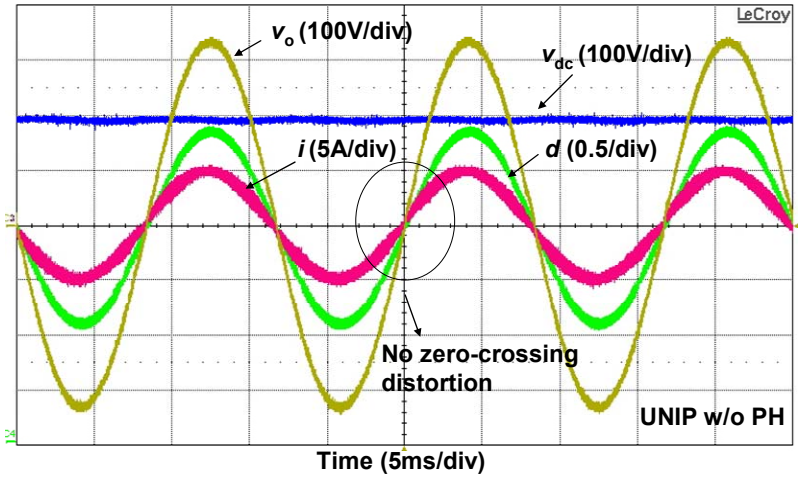
Fig. 3.23 shows the output current and voltage waveforms under different PWMs. It is clear to see that bipolar PWM creates severe zero-crossing distortion while all the other PWMs eliminate this issue, which meets the analysis in chapter 3.3. In addition, it is obvious to draw the conclusion that the phase-shifted PWM cuts down the current ripple to a great extent compared to PWM without the help of phase-shift.



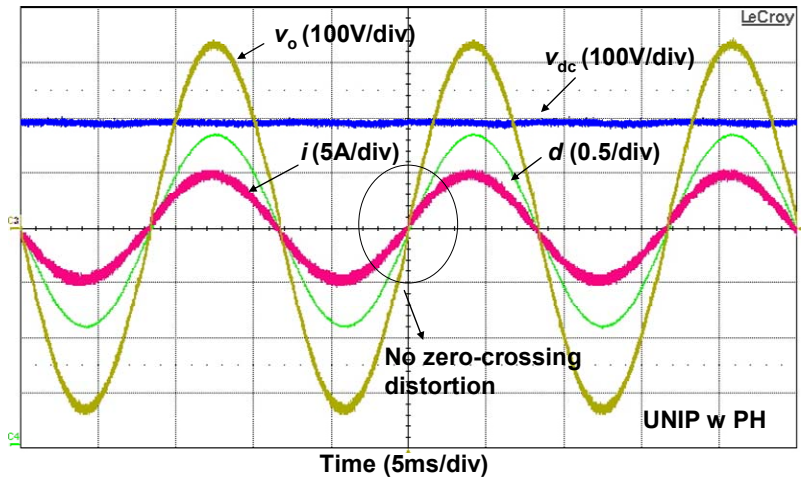
(a) Bipolar without phase-shifted PWM



(b) Bipolar with phase-shifted PWM



(c) Unipolar without phase-shifted PWM



(d) Unipolar with phase-shifted PWM

Fig. 3.23: Output current and voltage waveforms under different PWMs.

Fig. 3.24 shows the measured current THD for all four PWM methods. At light load condition, the zero-crossing problem is much more severe and that is why the THD for bipolar PWM at half load is up to 16%. All the other three PWMs can well restrain the THD below 2% at full load condition, which meets the limit of 5% of IEEE standard 519.

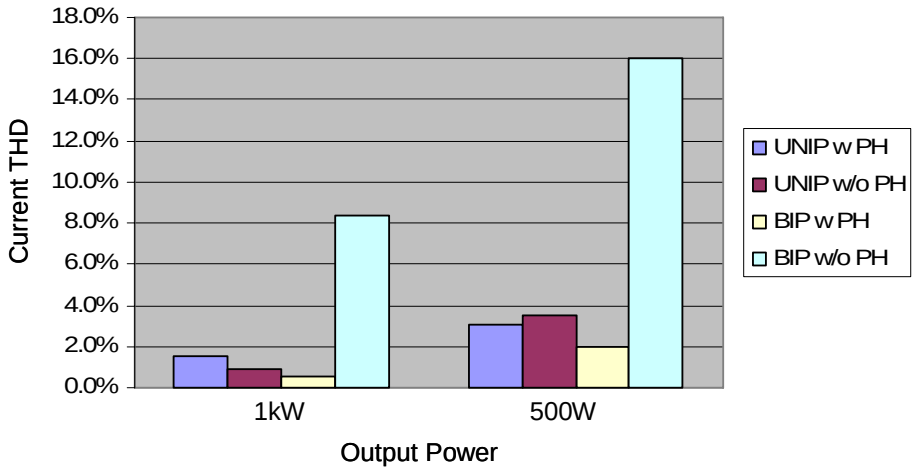


Fig. 3.24: Current THD comparison between different PWMs.

3.6 Summary

This chapter presents an AHCU PWM technique for a dual-buck full-bridge inverter to compensate for the zero-crossing distortion and improve the system efficiency. Traditional bipolar SPWM and the proposed PWM were comparatively analyzed in detail to demonstrate the advantages of the latter.

To prove the feasibility and effectiveness of this proposed PWM, a 2kW, 240V ac output dual-buck full-bridge inverter was built and tested with both bipolar SPWM and AHCU PWM. Experimental results indicated the adoption of AHCU PWM reduced the zero-crossing distortion to a great extent, especially at light load conditions. Efficiency measurement of the inverter system showed an average 0.6% improvement by using AHCU PWM compared to the traditional bipolar SPWM.

Following the AHCU PWM proposed for the single-unit dual-buck full-bridge inverter, this chapter further explores several PWM schemes for the cascade dual-buck full-bridge inverter. Different PWM schemes have been analyzed and the combinations are considered to be better choices when it comes to ripple reduction, zero-crossing distortion compensation and efficiency improvement. Experimental results proved the feasibility and effectiveness of the proposed topology and different PWM methods.

Chapter 4

Grid-Tie Control of Cascade Dual-Buck Inverter with Wide-Range Power Flow Capability

4.1 Introduction

Grid-tie control of distributed generation (DG) systems, such as fuel cell, photovoltaics, and wind power, are hot research topics nowadays with various circuit topologies and control methods proposed. Thanks to flexible modular design, transformerless connection, extended voltage and power output, less maintenance and higher fault tolerance, the cascade inverters are good candidates for utility interface of various renewable energy sources [14]-[24].

A new type of cascade inverters, cascade dual-buck inverter has been proposed in chapter 2. This newly proposed inverter inherits all the merits of cascade H-bridge inverter. Compared to cascade H-bridge inverter, it has several advantages. Most important of all, it eliminates the possibility of shoot-through problems, which is the major failure of traditional voltage source inverters. It does not need dead time, which fully utilizes the

pulse width modulated voltage and transfers total desired energy to the load. In addition, the cascade dual-buck inverter has the advantage to use high-voltage power MOSFETs without the complexity of soft-switching assisting circuits to improve the system efficiency.

In terms of cascade inverter grid-tie control, renewable energy and distributed generation sources can be classified into two types. Fuel cell power conditioning system (PCS) is Type I system with active power command generated by balance of plant (BOP) of each unit; and photovoltaic or wind PCS is Type II system with active power harvested by each front-end unit through maximum power point tracking (MPPT). Besides active power delivery, the DG systems are also requested to take the responsibility of sending reactive power to the grid within its design limit to help the grid maintain voltage and power demand. Reactive power command can be generated by distributed generation (DG) control site for both systems.

Several grid-tie control schemes have been proposed for cascade H-bridge inverter, mostly for photovoltaic applications [63]-[68]. Some used traditional PI controllers or repetitive controllers [63]-[65], others adopted advanced controllers like fuzzy logic, sliding mode, and ramptime ZACE [66]-[68]. However, few of them conducted reactive power delivery control, which is a requirement for future DG systems. In this chapter, a wide-range power delivery controller has been designed. For Type I system, the grid-tie control is designed to be current loop controller with both active and reactive power commands; for Type II system, the grid-tie control is structured to be dc bus voltage controllers for each cascade unit and an inner current loop controller with reactive power command combined with the active peak current reference generated by the dc bus mean

voltage controller**.**

Selective harmonic proportional resonant (PR) controller [56]-[57], [69] and admittance compensation controller [54]-[55], [70] have been reported to be effective in single inverter grid-tie control. In this paper, the two control techniques were first utilized in cascade inverter grid-tie control to achieve better steady-state and dynamic performance.

This chapter first presents the grid-tie system control block diagrams of both Type I and Type II systems. Second, the detailed analysis and design of controllers with wide-range power flow capability have been conducted. In order to verify the proposed control strategies, a 1kVA cascade dual-buck inverter grid-tie system has been designed. Various power flow conditions including pure active, pure reactive and mixed leading and lagging power factor cases have been tested under steady-state and dynamic conditions for both Type I and Type II systems. The experimental results proved the feasibility and effectiveness of the control system.

4.2 System Types and Block Diagrams

Fig. 2.1 shows the topology of newly proposed cascade dual-buck half-bridge inverter. The grid-tie control system discussed below will be based on this topology. The output port 1P and NN can be connected to the grid through commonly used inductor-capacitor-inductor (LCL) filter. The LCL filter has several benefits, including but not limited to higher high-frequency harmonics attenuation and operation flexibility for both standalone and grid-tie modes, which is a plus for DG systems such as PV and fuel cell PCS [69], [71]-[75].

As indicated in introduction, in terms of control, the grid-tie systems can be classified into two types. Type I system is fuel cell PCS, where each individual front-end unit acts as voltage source and the active power command generated by the BOP. Type II system is PV or wind PCS, where each individual front-end unit acts as current source when the maximum active power is provided by MPPT.

A. Type I System

Fig. 4.1 shows the Type I system structure. Each fuel cell energy source is connected to individual unit of cascade dual-buck inverter through dc-dc converter. The dc-dc converter boost ratio can be greatly reduced or the dc-dc converter is even not required if the cascade units are enough to generate the output grid voltage.

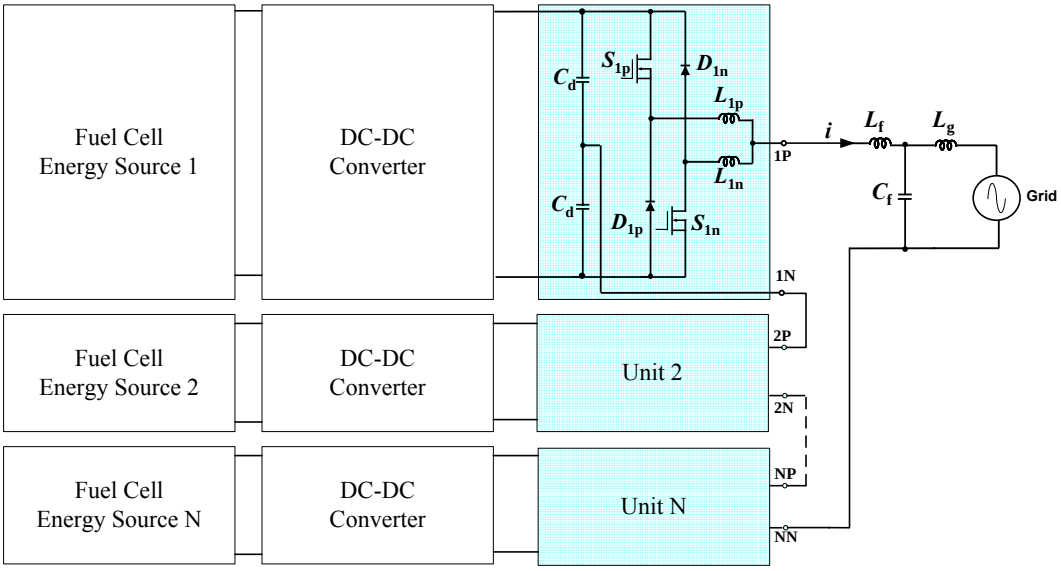


Fig. 4.1: System structure of Type I grid-tie PCS.

Fig. 4.2 shows the control block diagram of Type I system. By adopting LCL filter, the current feedback is sensed through L_f and the voltage feedback is obtained across C_f. The active power command P_{com} comes from the total BOP of fuel cell sources. The phase lock loop (PLL) will generate the magnitude and phase angle information of the grid and feed it to the current reference generation block. A current controller G_i with selective harmonic PR compensation is needed to produce the equivalent duty cycle d_{eq}. After obtaining each individual duty cycle for corresponding unit, the phase-shifted PWM will be made by DSP and then drives the active switches of the cascade dual-buck inverter. The detailed analysis of the control will be presented in chapter 4.3.

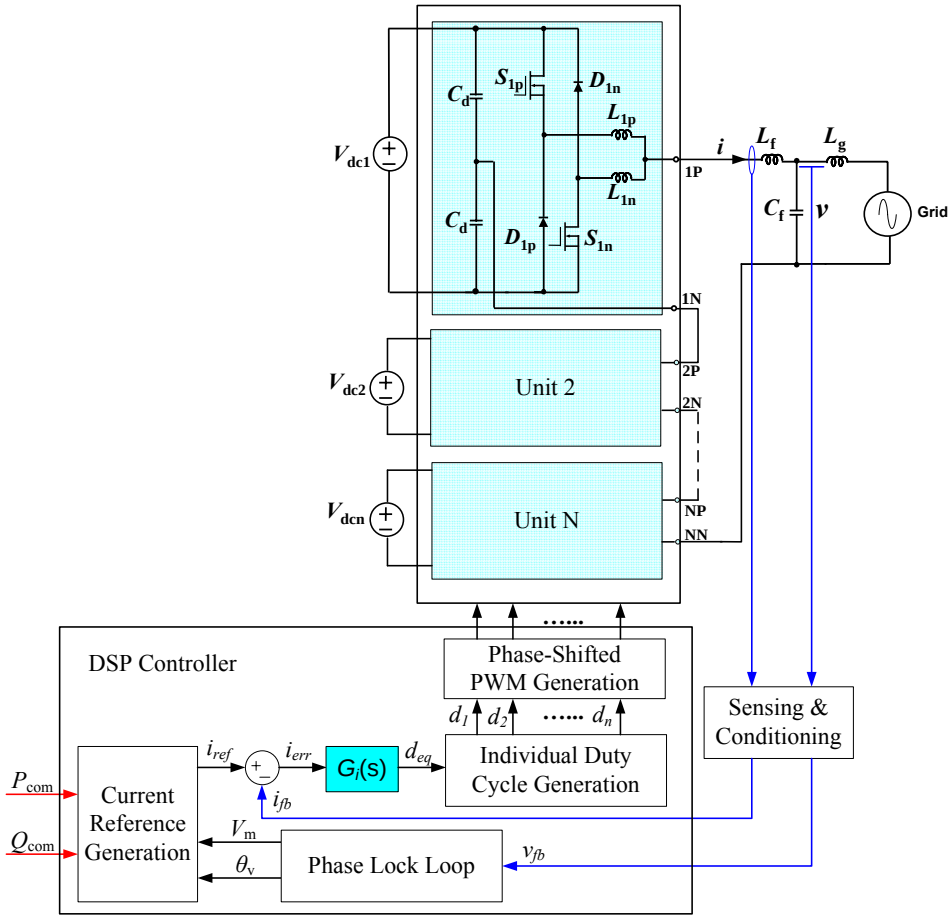


Fig. 4.2: Control block diagram of Type I grid-tie PCS.

B. Type II System

Fig. 4.3 shows the Type II system structure. Each PV or wind energy source is connected to individual unit of cascade dual-buck inverter through dc-dc converter or ac-dc converter. The front-end converter takes the responsibility of MPPT, and thus leaves the work of individual dc bus voltage control to cascade inverter. Similar to cascade H-bridge inverter, when used in PV grid-tie applications, in order to eliminate the leakage current caused by PV panel stray capacitance, the dc-dc converter needs to be designed with high-frequency transformer to solve the problem. If the front stage dc-dc converter is non-isolated, some measures [76] can be done with the cascade inverter unit to cut the

path of leakage current.

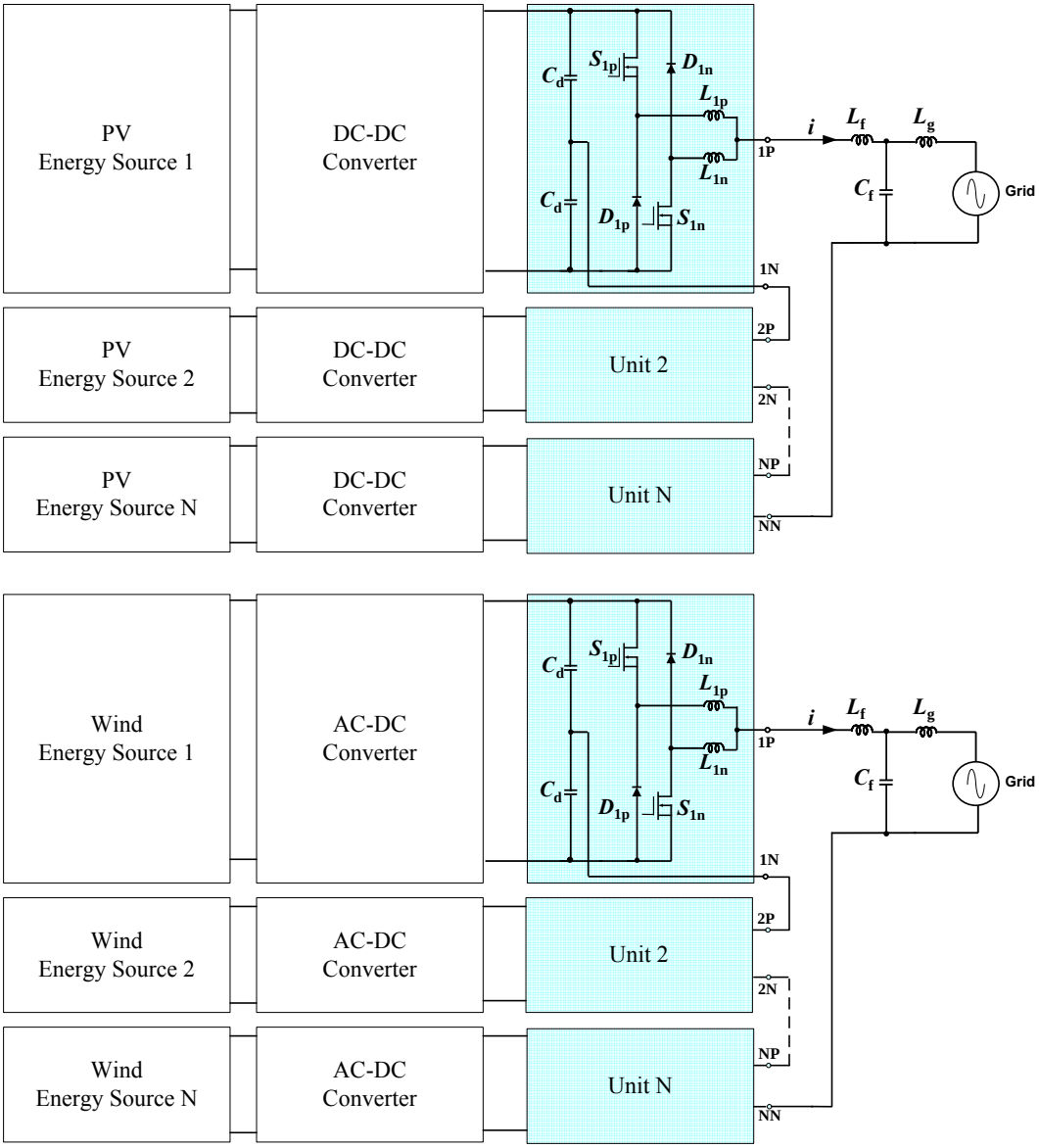


Fig. 4.3: System structure of Type II grid-tie PCS.

Fig. 4.4 shows the control block diagram of Type II system. Compared to Type I, the difference is the front-end stage acts as individual current source. Therefore, the cascade dual-buck inverter needs to control the dc bus voltage. The mean-value dc bus control loop with PI compensator G_v will generate the current reference for inner current loop, which produces the equivalent duty cycle d_{eq}. At the same time, each individual unit

has its own dc bus controller. The outputs of mean-value loop and individual loop are fed into individual duty cycle generation block for allocating unit duty cycle respectively. The detailed derivation will be discussed in the next section.

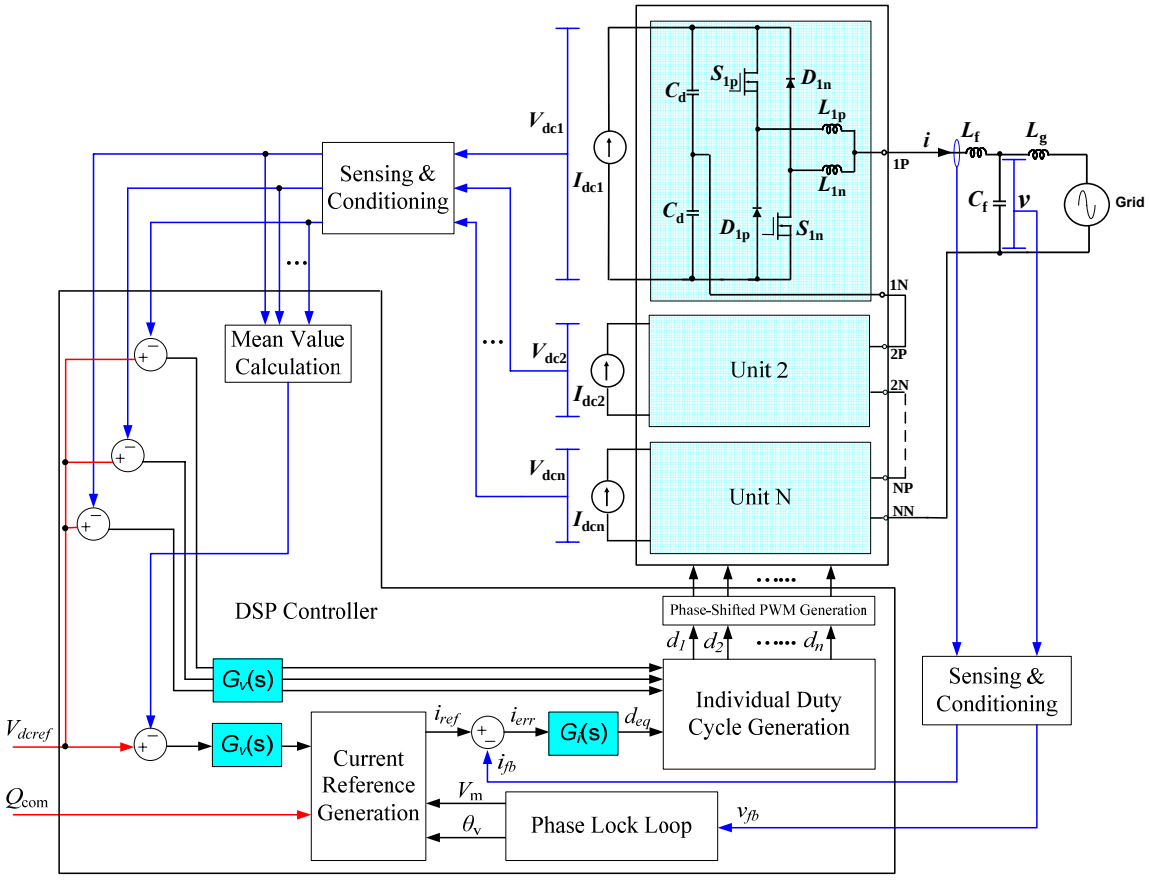


Fig. 4.4: Control block diagram of Type II grid-tie PCS.

4.3 Grid-Tie Control Design for Type I System

Fig. 4.5 shows the average model of cascade dual-buck half-bridge inverter in grid-tie system. d_j (j=1, …, n) is the duty cycle of each corresponding unit, and L_j (j=1, …, n) is the output inductor of each unit and

$$\begin{aligned} L_j &= L_{jp} \qquad i > 0 \\ L_j &= L_{jn} \qquad i < 0 \end{aligned} \tag{4.1}$$

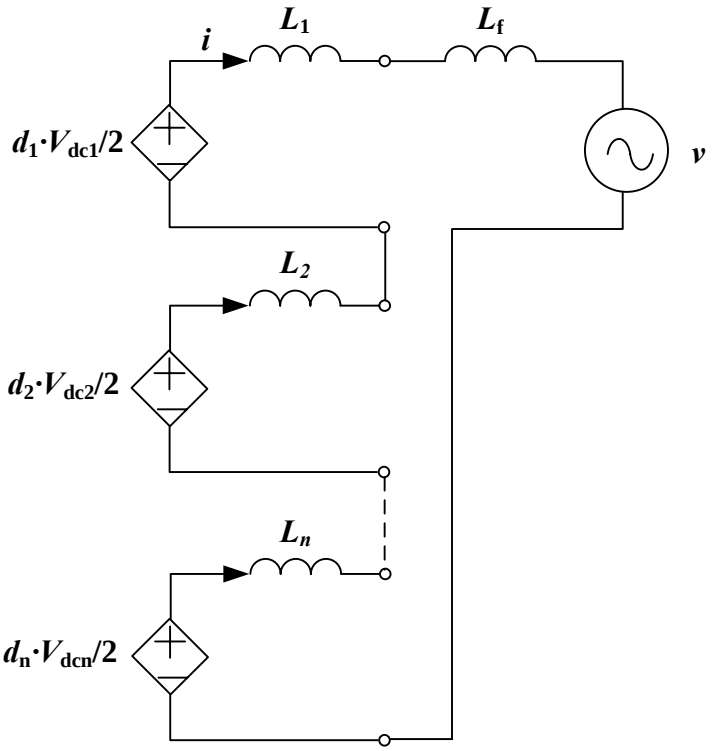


Fig. 4.5: The average model of cascade dual-buck half-bridge inverter in grid-tie PCS.

From Fig. 4.5, if the individual dc bus is not controlled by cascade inverter, which is the case in Type I system, we can assign

$$d_1 = d_2 = \cdots = d_n = d_{eq} \tag{4.2}$$

Then we have the following relation

$$d_1 \frac{V_{dc1}}{2} + d_2 \frac{V_{dc2}}{2} + \cdots + d_n \frac{V_{dcn}}{2} = d_{eq}(\frac{V_{dc1} + V_{dc2} + \cdots + V_{dcn}}{2}) = d_{eq} \frac{nV_{dc}}{2} \tag{4.3}$$

where V_{dc} is the mean value of the sum of each individual dc bus voltage. From (4.3) and Fig. 4.5, we can derive the equivalent average model of cascade dual-buck inverter shown in Fig. 4.6, where $\Sigma L_j = L_1 + L_2 + \cdots + L_n$

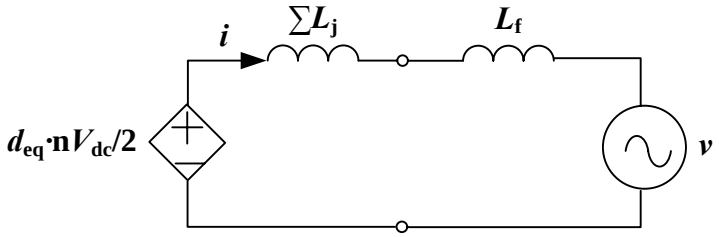


Fig. 4.6: The equivalent average model of cascade dual-buck inverter in grid-tie PCS.

Note that in the equivalent circuit above, we ignored the ESR in the inductance to derive the models below. Since the ESR in the inductors is very small, the omission of ESR will not affect the model and control. Define $L = \Sigma L_j + L_f$, and we have the following equation from Fig. 4.6

$$d_{eq}(t) \cdot \frac{nV_{dc}}{2} - v(t) = L \frac{di(t)}{dt} \tag{4.4}$$

Transfer (4.4) to s domain, we have

$$i(s) = \frac{1}{sL}(d_{eq}(s) \cdot \frac{nV_{dc}}{2} - v(s)) \tag{4.5}$$

So the transfer functions from d_{eq} to current i and voltage v to current i are as follows

$$G_{id}(s) = \frac{i(s)}{d_{eq}(s)} = \frac{\frac{nV_{dc}}{2}}{sL} \tag{4.6}$$

$$G_{iv}(s)=\frac{i(s)}{v(s)}=\frac{1}{sL} \tag{4.7}$$

where $G_{id}(s)$ is the control-to-output transfer function and $G_{iv}(s)$ is an uncontrolled feed-forward term. By introducing admittance compensation controller $G_{AC}(s)$, the undesirable term can be cancelled out, which brings in better smoothed zero-current start-up and reduced current steady-state error [54]-[55], [70]. In [55], the equivalent dc bus voltage is $V_{dc,}$ and thus the outcome of admittance compensation term is the reciprocal of V_{dc}. From Fig. 4.6, we can see clearly that the equivalent dc bus voltage for the cascade dual-buck inverter is $nV_{dc}/2$. Therefore, the admittance compensation transfer function is obtained as follows

$$G_{AC}(s)=\frac{1}{\frac{nV_{dc}}{2}} \tag{4.8}$$

Fig. 4.7 shows the control block diagram of Type I system.

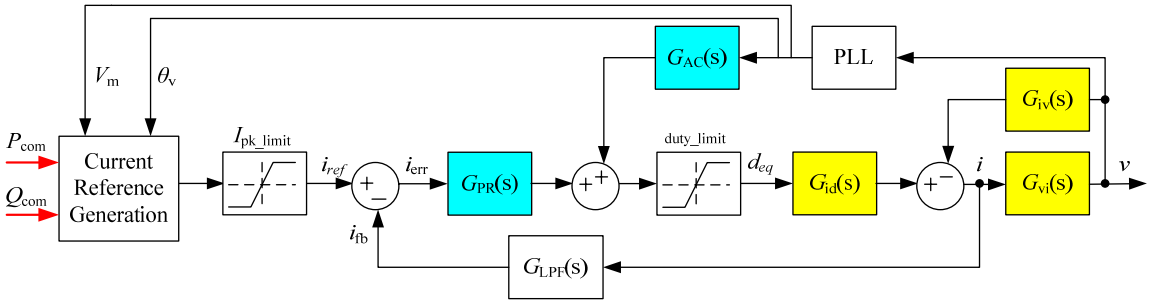


Fig. 4.7: Control block diagram of Type I system.

Through PLL, the grid voltage magnitude V_m and phase angle θ_v can be tracked down, and are used for admittance compensation and current reference generation. The active power and reactive power command can be used to calculate the apparent power command S_{com} and power factor angle φ as follows

$$S_{com} = \sqrt{P_{com}{}^2 + Q_{com}{}^2} \tag{4.9}$$

$$\varphi = \tan^{-1}(\frac{Q_{com}}{P_{com}}) \tag{4.10}$$

The current reference magnitude I_{m} can be obtained by

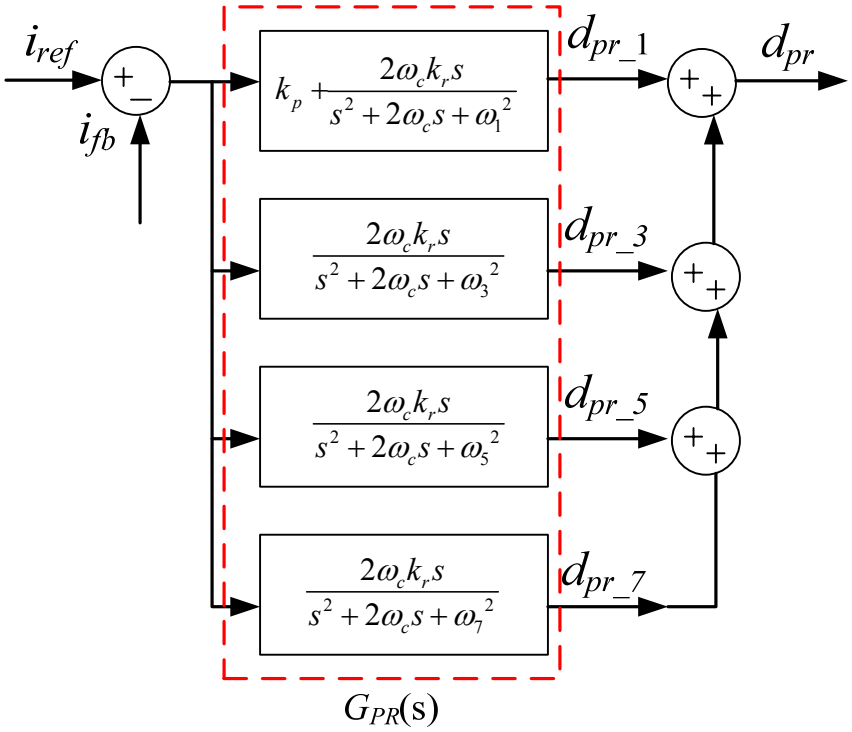
$$I_{\mathrm{m}} = \frac{S_{com}}{V_m / 2} \tag{4.11}$$

and the phase angle θ_i of the i_{ref} is

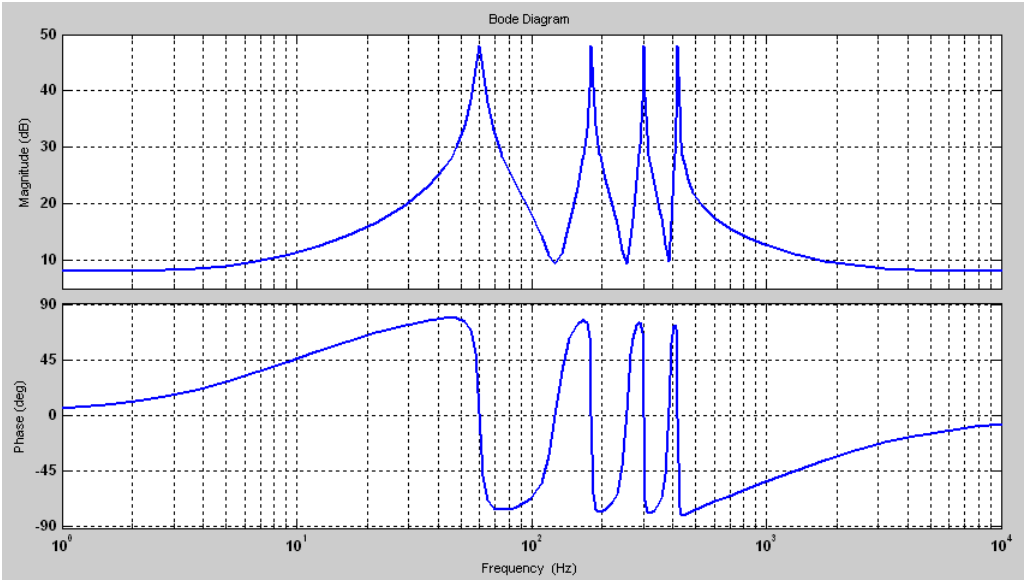
$$\theta_i = \theta_v - \varphi \tag{4.12}$$

For the current loop compensator $G_{\mathrm{PR}}(\mathrm{s})$, we choose a PR controller with capability of selective harmonics compensation [56]-[57], [69]. It proved to be a successful solution in DG grid-tie applications where high dynamics and lower harmonics compensation are required. Fig. 4.8 shows the PR controller we implemented with 3rd, 5th, and 7th harmonics compensation, where k_{p} is the proportional gain, k_{r} is the resonant gain, and ω_{c} is the equivalent bandwidth of the resonant controller. In principle, the bandwidth ω_{c} needs to be as small as possible, but for digital implementation, it is quite difficult to realize a small ω_{c}. Based on the comparison of different values in [55], it is appropriate to set ω_{c} as 10 to obtain a better highly selective bandwidth and at the same time practical for DSP implementation. From Fig. 4.8 (a), we can see that the controller gain at fundamental frequency can be increased by increasing either k_{p} or k_{r}, and the gain at harmonic frequencies can be maximized by boosting k_{r} values. For each individual harmonic compensation, it is possible to tune different k_{r} values to tackle different harmonics. However, for the real implementation, it is easier to set one k_{r} for all harmonic compensation as long as it meets the IEEE standard on current harmonics. On the other

hand, k_p and k_r can not be too high because it will impair the system stability. With $k_p = 2.5$, $k_r = 250$, $\omega_c = 10$ selection, the Bode plot of the PR controller is shown in Fig. 4.8 (b). It can be seen that at fundamental frequency and 3rd, 5th, and 7th harmonic frequency, the controller provides a large gain.



(a) PR controller $G_{PR}(s)$ with selective harmonic compensation



(b) Bode plot of PR controller $G_{PR}(s)$

Fig. 4.8: PR controller with selective harmonics compensation.

$G_{LPF}(s)$ is 2nd order low pass filter with cut-off frequency 5kHz and a damping ratio 0.7.

4.4 Grid-Tie Control Design for Type II System

For Type II system, the ac side model is still the same, as shown in Fig. 4.5. Because the cascade dual-buck inverter needs to control individual unit dc bus voltage to V_{dc}, which means

$$V_{dc1} = V_{dc2} = \cdots = V_{dcn} = V_{dc} \tag{4.13}$$

Then we have the following relation from Fig. 4.5

$$d_1 \frac{V_{dc1}}{2} + d_2 \frac{V_{dc2}}{2} + \cdots + d_n \frac{V_{dcn}}{2} = (d_1 + d_2 + \cdots + d_n) \frac{V_{dc}}{2} = d_{eq} \frac{nV_{dc}}{2} \tag{4.14}$$

where

$$d_{eq} = \frac{d_1 + d_2 + \cdots + d_n}{n} \tag{4.15}$$

Finally, from the derivation above, the equivalent average model at grid side does not change either in terms of formation, which is still Fig. 4.6. Therefore, (4.4) to (4.8) are correct for Type II system control except that the values of d_{eq} and V_{dc} comply with (4.13) and (4.15).

Fig. 4.9 shows the average model of each cascade unit at dc side. Therefore, we have the following equations

$$\begin{aligned} I_{dc1} &= \frac{1}{2} C_d \frac{dV_{dc1}}{dt} + d_1 i \\ I_{dc2} &= \frac{1}{2} C_d \frac{dV_{dc2}}{dt} + d_2 i \\ &\cdots \\ I_{dcn} &= \frac{1}{2} C_d \frac{dV_{dcn}}{dt} + d_n i \end{aligned} \tag{4.16}$$

From (4.16), further derivation can be made

$$I_{dc1} + I_{dc2} + \cdots + I_{dcn} = \frac{1}{2} C_d \frac{d(V_{dc1} + V_{dc2} + \cdots + V_{dcn})}{dt} + (d_1 + d_2 + \cdots + d_n) i \qquad (4.17)$$

Apply (4.13) and (4.15) to (4.17), we can obtain

$$I_{dc} = \frac{1}{2} C_d \frac{dV_{dc}}{dt} + d_{eq} i \qquad (4.18)$$

where $I_{dc} = (I_{dc1} + I_{dc2} + \cdots + I_{dcn})/n$. Fig. 4.10 shows the equivalent average model at dc side. From Fig. 4.10 and (4.18), we have the following s-domain equation

$$I_{dc}(s) = \frac{1}{2} C_d s V_{dc}(s) + d_{eq}(s) i(s) \qquad (4.19)$$

So the transfer function from i to V_{dc} is

$$G_{ivdcmean} = -\frac{2 d_{eq}(s)}{s C_d} \qquad (4.20)$$

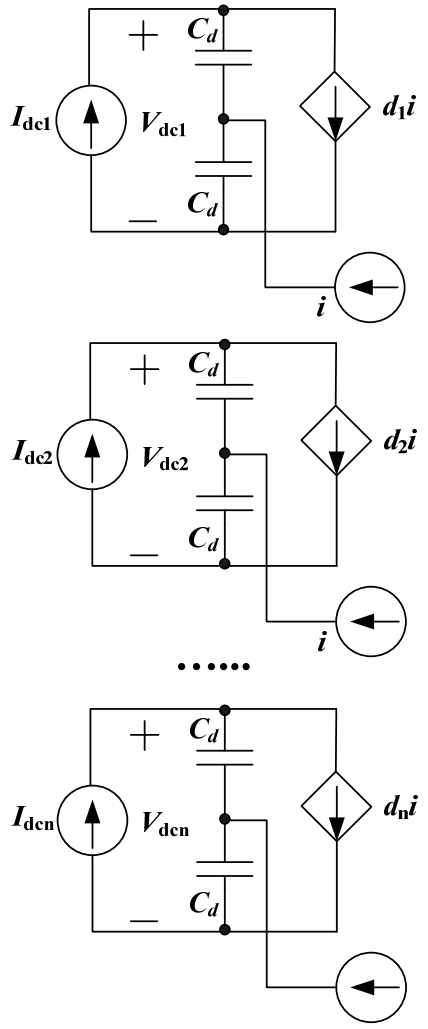


Fig. 4.9: The average model of individual cascade unit at dc side.

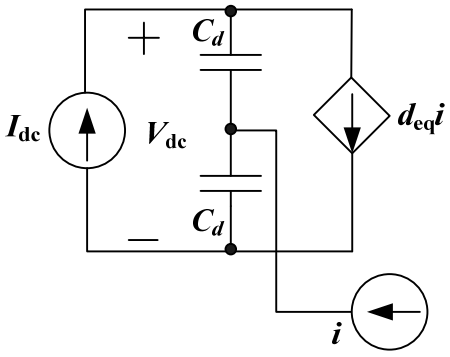
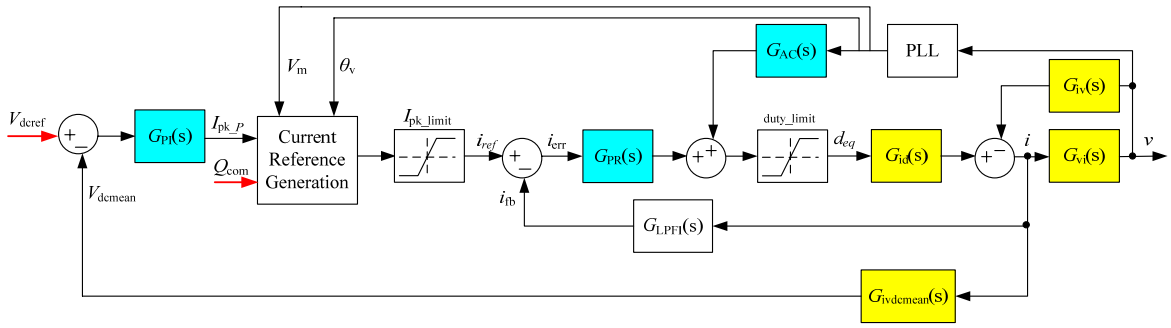
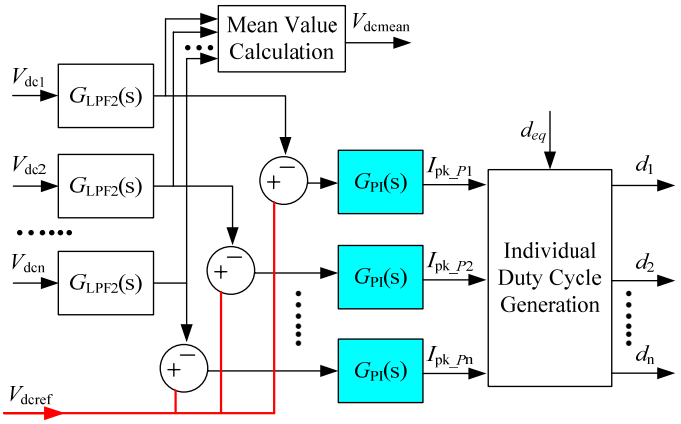


Fig. 4.10: The equivalent average model at dc side.

Fig. 4.11 shows the control block diagram of Type II system. Fig. 4.11 (a) is the control dual loops for generating equivalent duty cycle d_{eq}, (b) is the control loops to produce individual duty cycles.



(a) Equivalent duty cycle control loops



(b) individual duty cycle control loops

Fig. 4.11: Control block diagram of Type II system.

After having $G_{id}(s)$ from (4.6) and $G_{ivdcmean}(s)$ from (4.20), we can design the current-loop compensator $G_{PR}(s)$ and voltage-loop compensator $G_{PI}(s)$. $G_{PR}(s)$ follows the same design with Type I system shown in Fig. 4.8. $G_{PI}(s)$ is a PI controller with the following form

$$G_{PI}(s) = \frac{k(1+sT)}{sT} \tag{4.21}$$

where k=0.05, and T=0.05

The output of $G_{PI}(s)$ of the equivalent duty cycle loop is the peak current I_{pk_P} originated from the active power of the front-end of Type II system. So the active power command can be calculated as

$$P_{com} = \frac{1}{2} V_m I_{pk\_P} \tag{4.22}$$

After obtaining P_{com}, the following current reference calculation is the same with Type I system. Equations (4.9) to (4.12) hold.

For the individual voltage loops, $G_{PI}(s)$ can be the same, and the output is individual peak current I_{pk_Pj} (j=1, …, n) under the assumption that the cascade units are in parallel operation with the same active power generation. From Fig. 4.5 and 4.9, under cascade operation, the active power input and output should be the same if no loss considered.

$$I_{dc1}V_{dc1} + I_{dc2}V_{dc2} + \cdots + I_{dcn}V_{dcn} = \frac{1}{2} I_{pk\_P} V_m \tag{4.23}$$

If the cascade units are in parallel operation with the same active power generation, we can have

$$I_{dc1}V_{dc1} + I_{dc2}V_{dc2} + \cdots + I_{dcn}V_{dcn} = \frac{1}{2}(I_{pk\_P1} + I_{pk\_P2} + \cdots + I_{pk\_Pn})\frac{V_m}{n} \tag{4.24}$$

From (4.23) and (4.24), it is easy to see

$$I_{pk\_P} = \frac{I_{pk\_P1} + I_{pk\_P2} + \cdots + I_{pk\_Pn}}{n} \tag{4.25}$$

From (4.13) and (4.16), we can derive

$$\frac{I_{dcj}}{I_{dck}} = \frac{d_j}{d_k} \quad (j,k \in (1,2,\cdots n)) \tag{4.26}$$

From (4.13) and (4.24), we can obtain the relation

$$\frac{I_{dcj}}{I_{dck}} = \frac{I_{pk\_Pj}}{I_{pk\_Pk}} \quad (j,k \in (1,2,\cdots n)) \tag{4.27}$$

Therefore, from (4.26) and (4.27), it is easy to have the following individual duty cycle relation

$$\frac{d_j}{d_k} = \frac{I_{pk\_Pj}}{I_{pk\_Pk}} \quad (j,k \in (1,2,\cdots n)) \tag{4.28}$$

From (4.28), do the summation on both sides of the equations

$$\frac{d_1 + d_2 + \cdots + d_n}{d_j} = \frac{I_{pk\_P1} + I_{pk\_P2} + \cdots + I_{pk\_Pn}}{I_{pk\_Pj}} \quad j \in (1,2,\cdots n) \tag{4.29}$$

Apply (4.15), (4.25) to (4.29), finally we can generate the individual duty cycle by using the I_{pk_Pj} from individual voltage loops and I_{pk_P} and d_{eq} from equivalent duty cycle loop.

$$d_j = d_{eq} \frac{I_{pk\_Pj}}{I_{pk\_P}} \quad j \in (1,2,\cdots,n) \tag{4.30}$$

For the phase-shifted PWM generation, it is the same for Type I and Type II systems. Fig. 4.12 shows the flow chart of PWM generation based on current reference signal. For detailed analysis, refer to chapter 2.

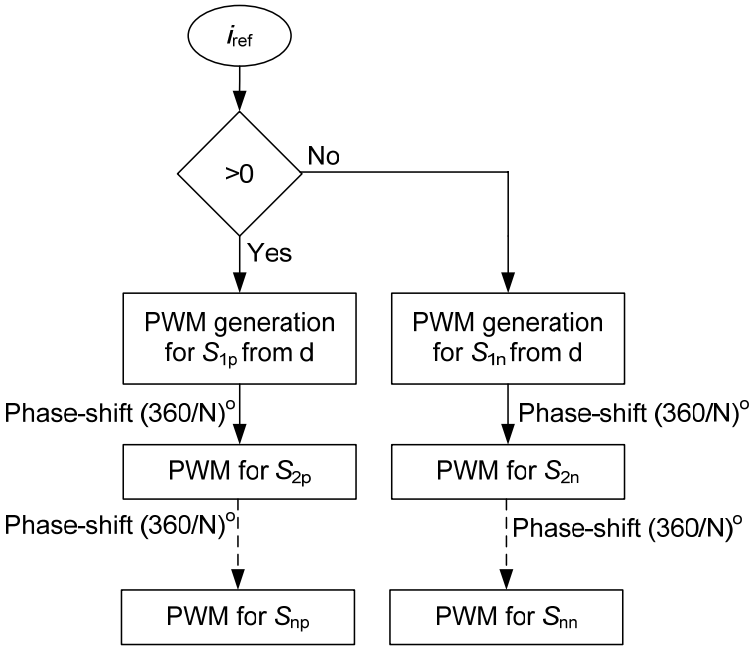


Fig. 4.12: Phase-shifted PWM generation.

4.5 Experimental Results

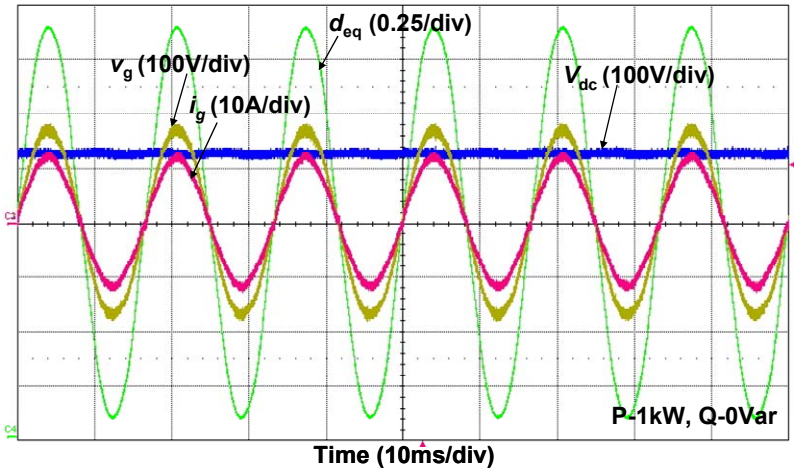
A 1kVA cascade dual-buck inverter grid-tie system has been designed to verify the effectiveness of the control for both Type I and Type II system. For Type I system, individual dc voltage sources are used to emulate the front-end units. For Type II system, individual dc current sources are used for the front-ends. Both 2-unit and 3-unit cascade dual-buck inverters have been tested under various power factor and command step conditions. For Type II system, tests of different power generation among different cascade units are also conducted.

The switching frequency of the devices is set to be 20 kHz. Because the cascade dual-buck inverter adopts phase-shifted PWM control, the equivalent switching frequency of the inverter is 40 kHz for 2-unit and 60 kHz for 3-unit cascade inverters, respectively. With more cascade units, the equivalent switching frequency will be higher, which leads to less output current ripple and possibility of smaller passive filter component selections. On the other hand, the system efficiency will suffer if the switching frequency is set too high because this topology is still hard-switching.

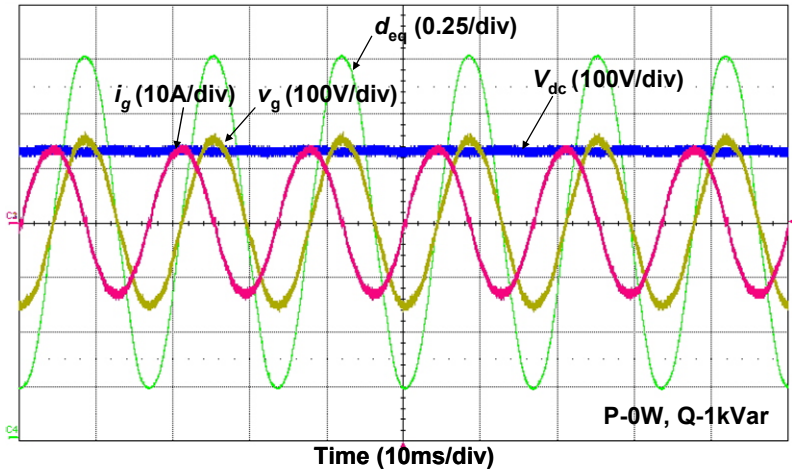
The grid voltage is 120V, 60Hz. The system controller and PWM generation are conducted by TI floating point DSP TMS320F28335. The MOSFET is selected as STY80NM60N with on-resistance 35mΩ, and the diode is RURG3060 with reverse recovery time 55ns. The passive components are selected as follows: L_{jp}=L_{jn}=250μH, L_f=1mH, C_f=2.4μF, L_g=0.5mH.

A. Type I system

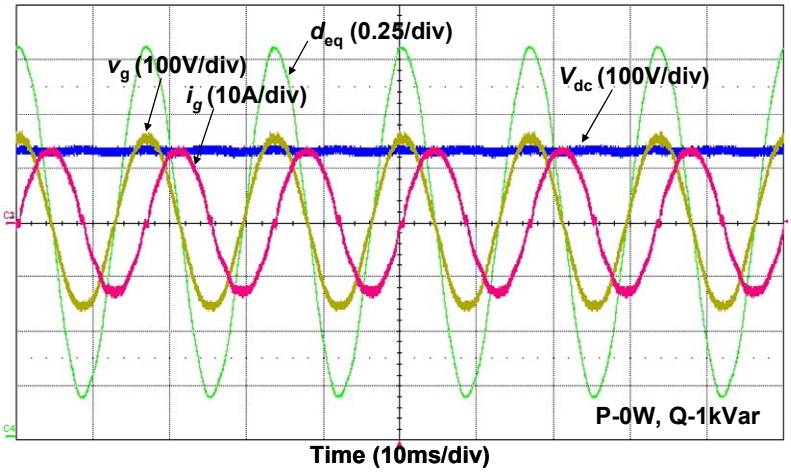
Fig. 4.13 shows the 3-unit cascade dual-buck inverter grid-tie control under pure active power, pure leading and lagging reactive power conditions. The output is either 1kW active power or 1kVar reactive power.



(a) 1kW active power



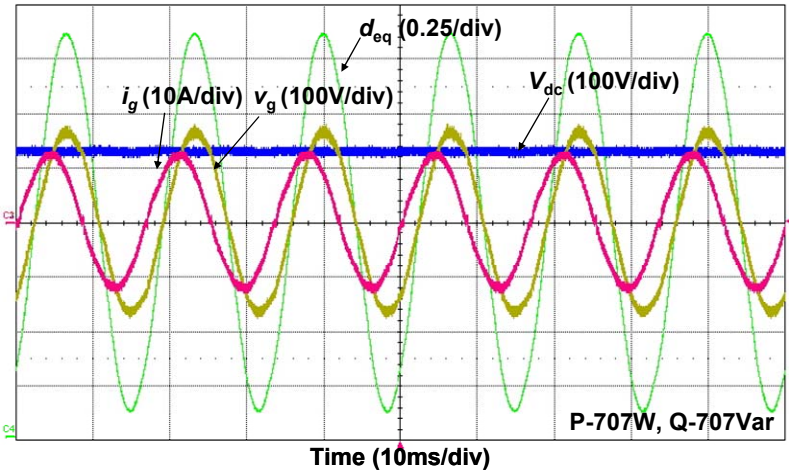
(b) 1kVar leading reactive power



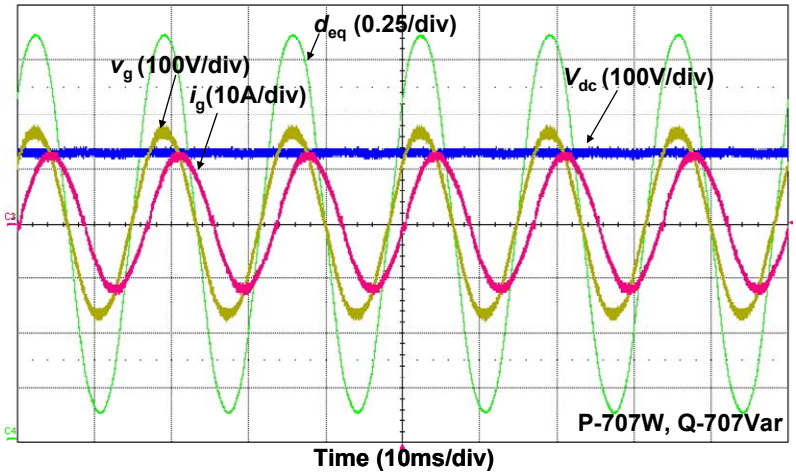
(c) 1kVar lagging reactive power

Fig. 4.13: Pure active and reactive power grid-tie test.

Fig. 4.14 shows the 3-unit cascade dual-buck inverter grid-tie control with equal active power and reactive power command. The total output is still 1kVA, and active power is 707W with either leading or lagging reactive power 707Var.



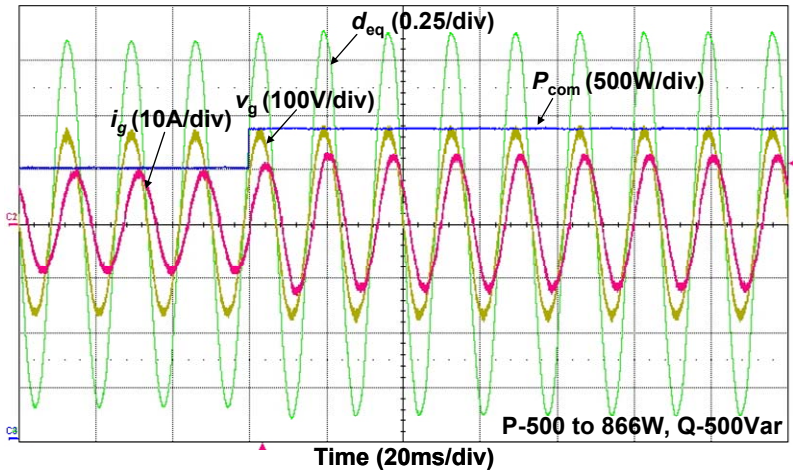
(a) 707W active power with 707Var leading reactive power



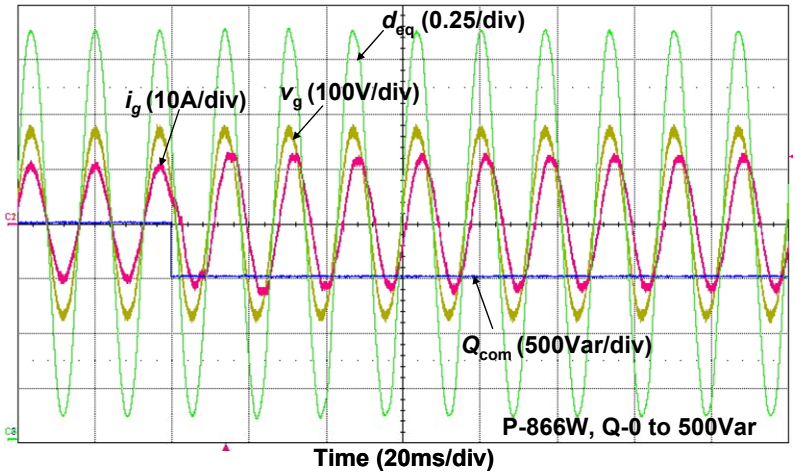
(b) 707W active power with 707Var lagging reactive power

Fig. 4.14: 1kVA output with equal active and reactive power grid-tie test.

Fig. 4.15 shows the 3-unit cascade dual-buck inverter grid-tie control with active power command and reactive power command step changes. The experimental results proved the control system has fast dynamics and good stability.



(a) Reactive power 500Var with active power step from 500W to 866W

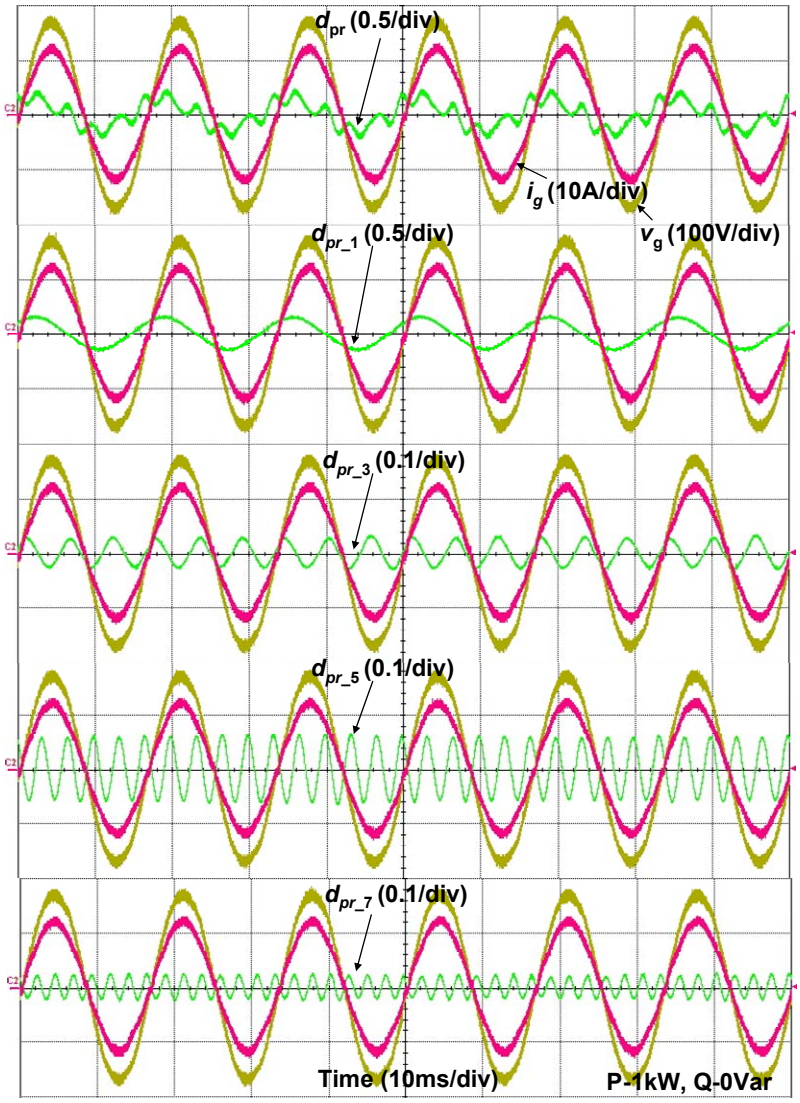


(b) Active power 866W with reactive power step from 0 to 500Var

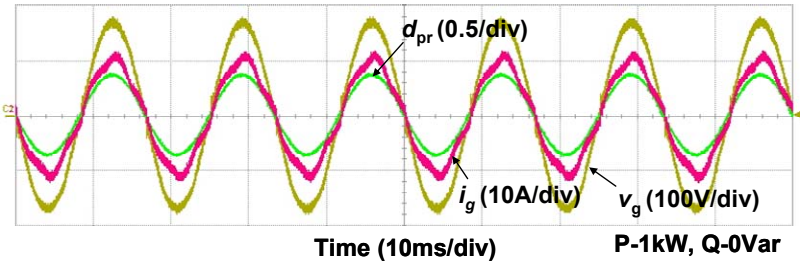
Fig. 4.15: 1kVA output with active and reactive power command step grid-tie test.

Fig. 4.16 (a) shows the output waveforms of selective harmonic PR compensator under 1kW condition. For comparison, the PR controller without harmonic compensation was also implemented and the results were shown in Fig. 4.16 (b). It is clear to see that with the help of selective harmonic PR compensator, the harmonics were minimized and thus the grid-tie current was sinusoidal. The IEEE 519 standard allows a limit of 5% for the current total harmonic distortion (THD) with individual limits of 4% for each odd harmonic from 3rd to 9th and 2% for 11th to 15th. In order to see the effectiveness of the control method, the measurement of current harmonics was conducted and the bar chart is illustrated in Fig. 4.16 (c), which indicates the compliance with the IEEE 519 standard. The measured grid voltage THD was 1.9%. As can be seen in the chart, the PR controller without harmonic compensation failed to comply with IEEE 519 standard with a THD of 7.5%, while the PR controller with harmonic compensation obtained noticeable improvement and satisfied the requirement of the standard with a THD of 2.7% and

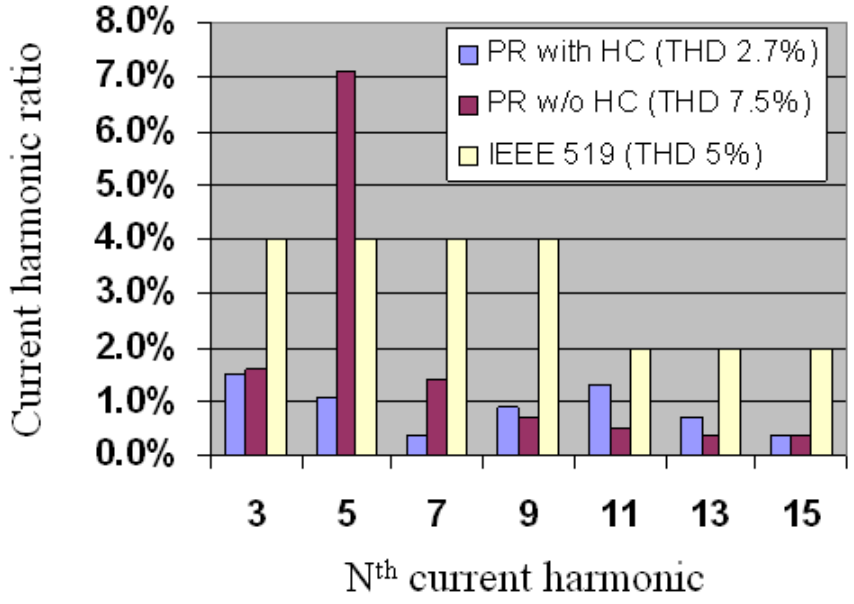
individual harmonic percentage within the limit.



(a) PR compensator with harmonic compensation



(b) PR compensator without harmonic compensation



(c) Current harmonic measurement

Fig. 4.16: PR controller output with 1kW output and current harmonics measurement.

B. Type II system

Fig. 4.17 shows the 3-unit cascade dual-buck inverter grid-tie control with different power generation from different cascade unit. The first unit has less power with small duty cycle while the other two units have the same power output. From the experimental results, we can see the ratio between d_1 and d_2 equals the ratio between I_{dc1} and I_{dc2}, and the relationship between the equivalent duty cycle and individual duty cycles satisfies the previous derivation.

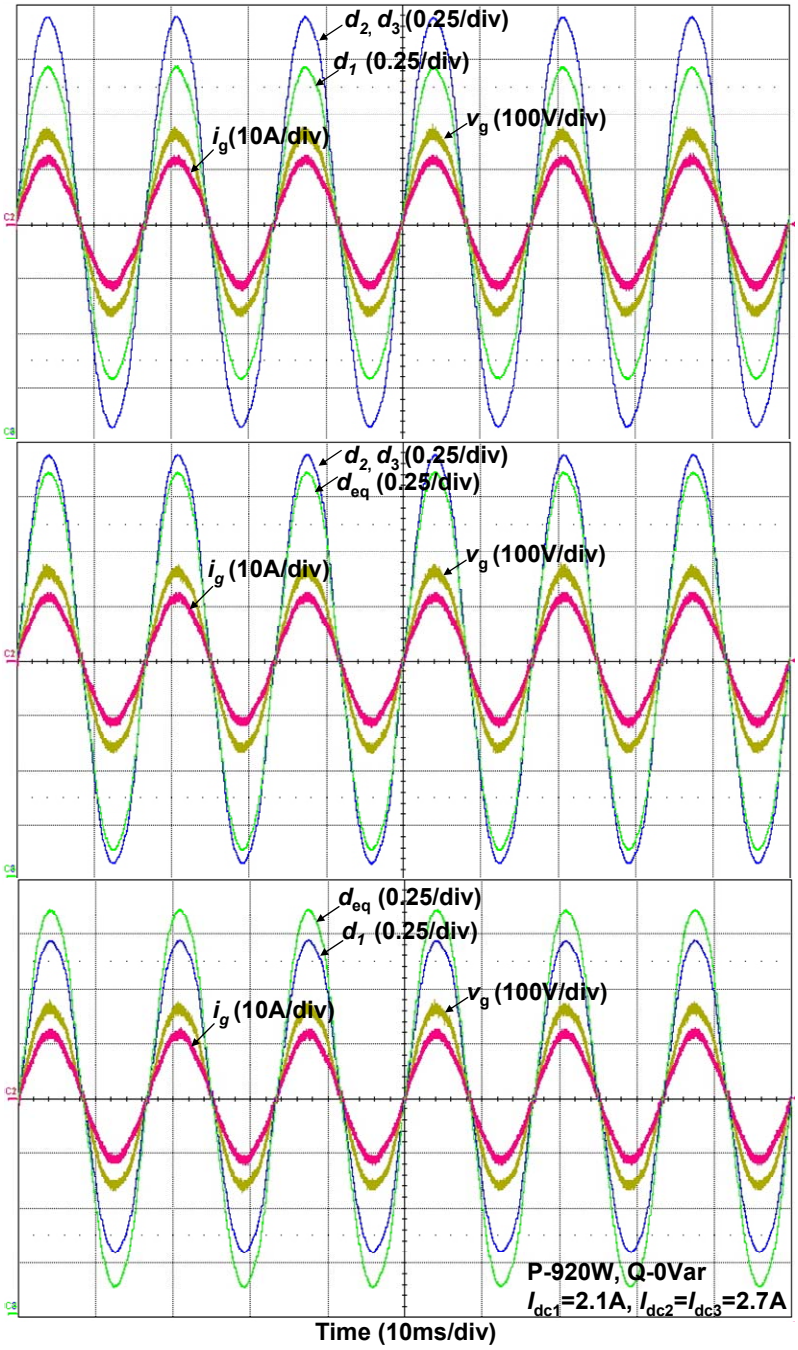


Fig. 4.17: Different individual duty cycles with different power generation.

Fig. 4.18 shows the positive half-cycle current of 2-unit cascade dual-buck inverter grid-tie control with equal active and reactive power output. This is the unique waveform of cascade dual-buck inverter, and only S_{ip} works at the positive half-cycle of output

current, which results in enhanced system reliability due to no shoot-through possibilities.

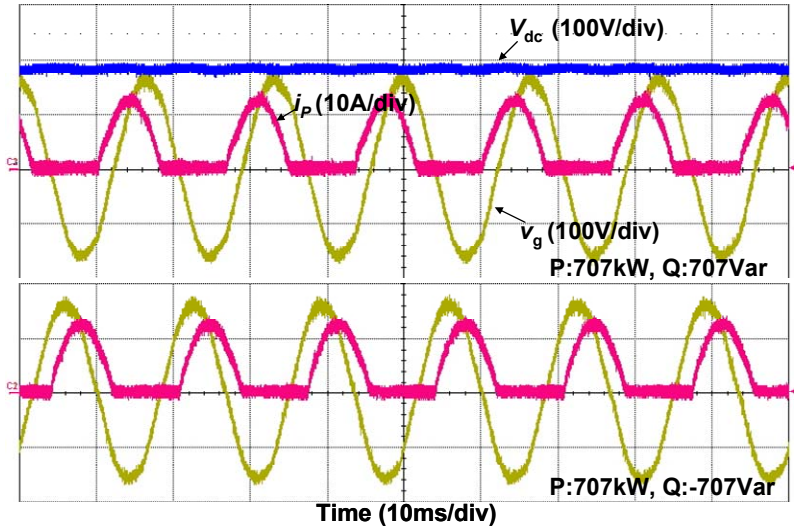


Fig. 4.18: Positive half-cycle current output under 707W and 707Var.

Fig. 4.19 shows the 2-unit cascade dual-buck inverter grid-tie control under reactive power command step conditions. The reactive power command was made on both leading and lagging directions. The results proved the control dynamics and stability.

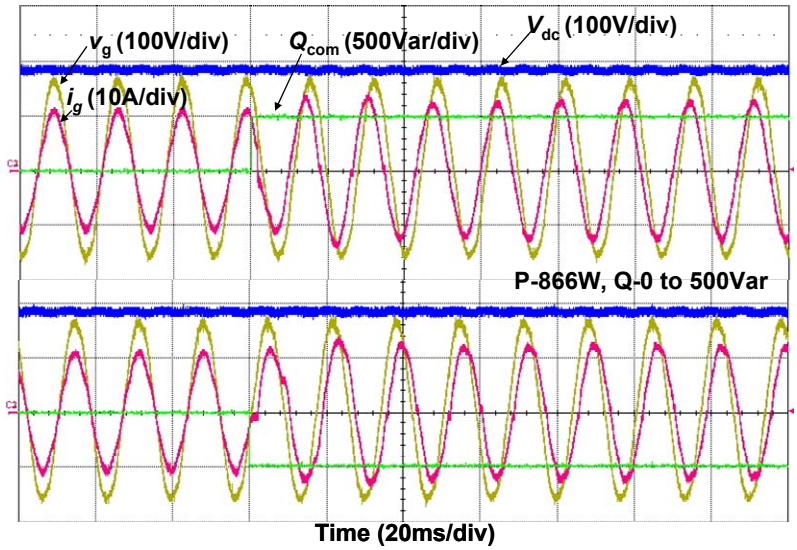


Fig. 4.19: Reactive power command step from 0 to 500Var.

4.6 Summary

The chapter presented grid-tie control of cascade dual-buck inverter for two types of renewable energy and distributed generation systems. The control system ensures wide-range power flow capability, from pure active power to pure reactive power delivery. Detailed analysis and design of the controllers were conducted for each system. Selective harmonic PR controller and admittance compensation controller were incorporated into the control loop to achieve better dynamic and steady-state performances. A 1kVA cascade dual-buck inverter grid-tie system was built and tested to verify the proposed control for both Type I and Type II systems. Wide-range power flow experimental results proved the feasibility and effectiveness of the designed control system.

Chapter 5

Conclusion and Future Work

5.1 Summary and Major Contributions

This dissertation presents the analysis, design and implementation of the cascade dual-buck inverters. Major contributions of the dissertation can be summarized as follows:

1. A new type of cascade inverters, cascade dual-buck inverters, is firstly proposed in the dissertation. Cascade dual-buck inverters are based on single-unit dual-buck inverters. Compared to traditional cascade inverters, they have enhanced system reliability thanks to no dead time and shoot-through concerns and they can achieve lower switching losses with the help of using power MOSFETs.

2. Phase-shift control is applied to cascade dual-buck inverters to solve the zero-crossing distortion problems. In addition, phase-shift control can greatly reduce the ripple current or cut down the size of passive components by increasing the equivalent switching frequency.

3. An asymmetrical half-cycle unipolar (AHCU) PWM technique is proposed for dual-buck full-bridge inverter for zero-crossing distortion compensation and

efficiency improvement. The proposed approach is to cut down the switching loss of power MOSFETs by half. At the same time, this AHCU PWM leads to current ripple reduction, and thus reducing ripple-related loss in filter components.

4. Evaluation of different PWM schemes is performed on cascade dual-buck full-bridge inverters. Several PWM techniques are analyzed and compared, including bipolar PWM, unipolar PWM and phase-shifted PWM. It has been found out that a PWM combination technique with the use of two out of the three PWMs leads to better performance in terms of less output current ripple and harmonics, no zero-crossing distortion, and higher efficiency.

6. A grid-tie control system is proposed for cascade dual-buck inverters with both active and reactive power flow capability in a wide range under two types of renewable energy and distributed generation sources. Fuel cell power conditioning system (PCS) is Type I system with active power command generated by balance of plant (BOP) of each unit; and photovoltaic or wind PCS is Type II system with active power harvested by each front-end unit through maximum power point tracking (MPPT). Reactive power command is generated by distributed generation (DG) control site for both systems. Selective harmonic proportional resonant (PR) controller and admittance compensation controller are first introduced to cascade inverter grid-tie control to achieve better steady-state and dynamic performances.

5.2 Future Work

1. Design and implement three-phase cascade dual-buck inverters for three-phase power loads and systems.
2. Explore the mode transfer between standalone and grid-tie control of cascade dual-buck inverters.
3. Add front-stage dc-dc converters to connect with renewable energy sources, such as PV panels or fuel cells, to perform system level control.

5.3 Publications

- **P.W. Sun**, C. Liu, J.-S. Lai, and C.-L. Chen, "Cascade Dual Buck Inverter with Phase-Shift Control", *IEEE Trans. Power Electron.,* vol. 27, no. 4, pp. 2067-2077, Apr. 2012.
- **P.W. Sun**, C. Liu, J.-S. Lai, and C.-L. Chen, "Grid-Tie Control of Cascade Dual-Buck Inverter with Wide-Range Power Flow Capability for Renewable Energy Applications", *IEEE Trans. Power Electron.,* vol. 27, no. 4, pp. 1839-1849, Apr. 2012.
- **P.W. Sun**, C. Liu, J.-S. Lai, C.-L. Chen, and N. Kees, "Three-Phase Dual-Buck Inverter with Unified Pulse Width Modulation", *IEEE Trans. Power Electron.,* vol. 27, no. 3, pp. 1159-1167, Mar. 2012.
- **P.W. Sun**, J.-S. Lai, C. Liu, W.S. Yu, "A 55kW Three-Phase Inverter Based on Hybrid-Switch Soft-Switching Modules for High Temperature Hybrid Electric Vehicle Drives Application", *IEEE Trans. Ind. Applicat.,* accepted for publication, 2012.
- C. Liu**, P.W. Sun**, J.-S. Lai, and et al., "Cascade Dual-Boost/Buck Active-Front-End Converter for Intelligent Universal Transformer", *IEEE Trans. Ind. Electron.,* accepted for publication, 2012.
- **P.W. Sun**, C. Liu, C.-L. Chen, and J.-S. Lai, "Cascade Dual-Buck Full-Bridge Inverter with Hybrid PWM Technique," in *Proc. 27th IEEE Applied Power Electron. Conf. and Expo.*, Feb. 2012, pp. 113-119.

- B.F. Chen, **P.W. Sun**, C. Liu, C.-L. Chen, and J.-S. Lai, "High Efficiency Transformerless Grid-Connected Photovoltaic Inverter with Wide-Range Power Factor Capability," in *Proc. 27th IEEE Applied Power Electron. Conf. and Expo.*, Feb. 2012, pp. 575-582.
- **P.W. Sun**, J.-S. Lai, H. Qian, W.S. Yu, and et al., "Efficiency evaluation of a 55kW soft-switching module based inverter for high temperature hybrid electric vehicle drives application," in *Proc. 25th IEEE Applied Power Electron. Conf. and Expo.*, 2010, pp. 474–479.
- S.-Y. Park, **P.W. Sun**, W. Yu and J.-S. Lai, "Performance evaluation of high voltage super junction MOSFETs for zero-voltage soft-switching inverter applications," in *Proc. 25th IEEE Applied Power Electron. Conf. and Expo.*, 2010, pp. 387–391.
- **P.W. Sun**, J.-S. Lai, H. Qian, W.S. Yu, C. Smith, and J. Bates, "High efficiency three-phase soft-switching inverter for electric vehicle drives," in *Proc. IEEE Vehicle Power and Propulsion Conf.*, 2009, pp. 761–766.
- J.-S. Lai, W.S. Yu, H. Qian, **P.W. Sun**, and et al., "High temperature device characterization for hybrid electric vehicle traction inverters," in *Proc. 24th IEEE Applied Power Electron. Conf. and Expo.*, 2009, pp. 665–670.

References

[1] F. Blaabjerg, Z. Chen, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Trans. Power Electron.*, vol. 19, no. 5, pp. 1184-1194, Sep. 2004.

[2] B. Maurhoff and G. Wood, "Dispersed generation to reduce power costs and improve service reliability," in *Proc. of IEEE REPC*, pp. C5/1-C5/7, 2000.

[3] J. Gutierrez-Vera, "Use of renewable sources of energy in Mexico," *IEEE Trans. Energy Conv.*, vol. 9, pp. 442-450, Sept. 1994.

[4] L. Philipson, "Distributed and dispersed generation: addressing the spectrum of consumer needs," in *Proc. of IEEE Power Engineering Society Summer Meeting*, vol. 3, pp.1663-1665, 2000.

[5] G. T. Chinery and J. M. Wood, "Tva's photovoltaic activities," *IEEE Trans. Power Appa. and Syst.*, vol. pas-104, pp. 1998-2005, Aug. 1985.

[6] *Wind Power in Power Systems*, Edited by Thomas Ackermann, J. Willy Press, 2003.

[7] *Fuel Cell Fundamentals*, R. P. O'Hayre, S.W. Cha, W. G. Colella, and F.B. Prinz, , New Jersey: Wiley, 2009.

[8] M. R. Khan, and M. F. Khan, "Energy cost calculations for a solar PV home system," in *Developments in Renewable Energy Technology Conference, ICDRET 07*, pp. 1-4, Dec. 2009.

[9] US Department of Energy*, Linkages for DOE's Wind Energy Program R&D to Commercial Renewable Power Generation,* Sep. 2009.

[10] J. M. Carrasco, L. G. Franquelo, J. T. Bialasiewicz, E. Galvan, R. C. P. Guisado, Ma.A.M. Prats, J.I. Leon, and N. Moreno-Alfonso, "Power-electronic systems for the grid integration of renewable energy sources: a survey," *IEEE Trans. Ind. Electron.*, vol. 53, no. 4, pp. 1002-1016, June 2006.

[11] P. F. Ribeiro, B. K. Johnson, M. L. Crow, A. Asroy, and Y. Lie, "Energy storage systems for advanced power applications," in *Proc. of IEEE*, vol. 89, pp. 1744-1765, Dec. 2001.

[12] J.-S. Lai, "Power conditioning systems for renewable energies," in *International Conference on Electrical Machines and Systems, ICEMS 07*, pp. 209-218, Oct. 2007.

[13] F. Blaabjerg, R. Teodorescu, M. Liserre, and A.V. Timbus, "Overview of control and grid synchronization for distributed power generation systems," *IEEE Trans. Ind. Electron.,* vol 53, pp. 1398-1409, Oct. 2006.

[14] J. S. Lai and F. Peng, "Multilevel converters—A new breed of power converter," *IEEE Trans. Ind. Electron.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[15] J. Rodriguez, J. S. Lai, and F. Peng, "Multilevel inverters: A survey of topologies, controls, and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.

[16] M. Malinowski, K. Gopakumar, J. Rodriguez, and M.A. Pérez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2196–2206, Jul. 2010.

[17] L. G. Franquelo, J. Rodriguez, J. I. Leon, S. Kouro, R. Portillo, and M. A. M. Prats, "The age of multilevel converters arrives," *IEEE Ind. Electron. Mag.*, vol. 2, no. 2, pp. 28–39, Jun. 2008.

[18] F. Z. Peng, J.W. McKeever, and D.J. Adams, "Cascade Multilevel Inverters for Utility Applications," in *Conf. Rec. IEEE-IECON Annu. Meeting*, New Orleans, LA, Nov. 9–14, 1997, pp. 437–442.

[19] P. Lezana and G. Ortiz, "Extended operation of cascade multicell converters under fault condition," *IEEE Trans. Ind. Electron.*, vol. 56, no. 7, pp. 2697–2703, Jul. 2009.

[20] H. Ertl, J. W. Kolar, and F. C. Zach, "A novel multicell DC–AC converter for applications in renewable energy systems," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1048–1057, Oct. 2002.

[21] F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power systems," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[22] L. Maharjan, S. Inoue, H. Akagi, J. Asakura, "A transformerless battery energy storage system based on a multilevel cascade PWM converter," in *Proc. IEEE Power Electron. Spec. Conf.*, 2008, pp. 4798–4804.

[23] F. Filho, Cao Yue, L.M. Tolbert, "11-Level cascaded H-bridge grid-tied inverter interface with solar panels," in *Proc. of IEEE APEC*, Palms Spring CA, Feb. 2010, pp. 968-972.

[24] M. Calais, and V.G. Agelidis, "Multilevel converters for single-phase grid connected photovoltaic systems-an overview," in *Proc. IEEE International Sympo. on Ind. Electron.*, 1998, pp. 224–229.

[25] F. Z. Peng and J. S. Lai, "A multilevel voltage-source inverter with separate DC sources for static var generation," in *Conf. Rec. IEEE-IAS Annu. Meeting*, Lake Buena Vista, FL, Oct. 8–12, 1995, pp. 2541–2548.

[26] F. Z. Peng and J. S. Lai, "Dynamic performance and control of a static var compensator using cascade multilevel inverters," in *Conf. Rec. IEEE-IAS Annu. Meeting*, San Diego, CA, Oct. 6–10, 1996, pp. 1009–1015.

[27] M. Hagiwara, K. Nishimura, and H. Akagi, "A Medium-Voltage Motor Drive With a Modular Multilevel PWM Inverter," *IEEE Trans. Power Electron.,* vol. 25, no. 7, pp. 1786–1799, Jul. 2010.

[28] R. Teodorescu, F. Blaabjerg, J. Pederson, E. Cengelci, and P. Enjeti, "Multilevel inverter by cascading industrial VSI," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 832–838, Aug. 2002.

[29] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. 34th IEEE Power Electron. Spec. Conf.*, 2003, vol. 2, pp. 731–735.

[30] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[31] F. S. Kang, S. J. Park, S. E. Cho, C. U. Kim, and T. Ise, "Multilevel PWM inverters suitable for the use of stand-alone photovoltaic power grid-connected inverters for photovoltaic modules," *IEEE Trans. Energy Convers.*, vol. 20, no. 4, pp. 906–915, Dec. 2005.

[32] L.M. Tolbert, F.Z. Peng, T.G. Habetler, "Multilevel converters for large electric drives," *IEEE Trans. Ind. Applicat.*, vol. 35, no. 1, pp. 36–44, Jan../Feb. 1999.

[33] L.M. Tolbert, F.Z. Peng, T. Cunnyngham, J.N. Chiasson, "Charge balance control schemes for cascade multilevel converter in hybrid electric vehicles," *IEEE Trans. Ind. Electron.*, vol. 49, no. 5, pp. 1058–1064, Oct. 2002.

[34] L. Maharjan, T. Yamagishi, H. Akagi, J. Asakura,;, "Fault-Tolerant Operation of a Battery-Energy-Storage System Based on a Multilevel Cascade PWM Converter With Star Configuration", *IEEE Trans. Power Electron.,* vol. 25, no. 9, pp. 2386–2396,Sep. 2010.

[35] Q. Song, and W.H. Liu, "Control of a Cascade STACOM with Star Configuration under Unbalanced Conditions ," *IEEE Trans. Power Electron.,* vol. 24, no. 1, pp. 45–58, Jan. 2009.

[36] L. Maharjan, S. Inoue, H. Akagi, and J. Asakura, "State-of-Charge (SOC)-Balancing Control of a Battery Energy Storage System Based on a Cascade PWM Converter ," *IEEE Trans. Power Electron.,* vol. 24, no. 6, pp. 1628–1636, Jun. 2009.

[37] Z. Du, L.M. Tolbert, B. Ozpineci, and J.N. Chiasson, "Fundamental Frequency Switching Strategies of a Seven-Level Hybrid Cascaded H-Bridge Multilevel Inverter ," *IEEE Trans. Power Electron.,* vol. 24, no. 1, pp. 25–33, Jan. 2009.

[38] S.-Y. Park, P.W. Sun, W. Yu and J.-S. Lai, "Performance evaluation of high voltage super junction MOSFETs for zero-voltage soft-switching inverter applications," in *Proc. 25th IEEE Applied Power Electron. Conf. and Expo.*, 2010, pp. 387–391.

[39] L. Saro, K. Dierberger, and R. Redl, "High-voltage MOSFET behavior in soft-switching converters: analysis and reliability improvements," in *Proc. 20th IEEE Telecom. Energy Conf.*, 1998, pp. 30–40.

[40] X.D. Huang, H.J. Yu, J.-S. Lai, A.R. Hefner, and D.W. Berning, "Characterization of paralleled super junction MOSFET devices under hard and soft-switching conditions," in *Proc. 32nd IEEE Power Electron. Spec. Conf.*, 2001, vol. 4, pp. 2145–2150.

[41] C.M. Johnson, and V. Pickert, "Three-phase soft-switching voltage source converters for motor drives. II. Fundamental limitations and critical assessment," *IEE Proceedings on Electric Power Applications*, vol. 146, no. 2, pp. 155–162, 1999.

[42] V. Pickert, and C.M. Johnson, "Three-phase soft-switching voltage source converters for motor drives. I. Overview and analysis," *IEE Proceedings on Electric Power Applications*, vol. 146, no. 2, pp. 147–154, 1999.

[43] P.W. Sun, J.-S. Lai, H. Qian, W.S. Yu, C. Smith, and J. Bates, "High efficiency three-phase soft-switching inverter for electric vehicle drives," in *Proc. IEEE Vehicle Power and Propulsion Conf.*, 2009, pp. 761–766.

[44] J.H. Zhang, and J.-S. Lai, "A synchronous rectification featured soft-switching inverter using CoolMOS," in *Proc. 21th IEEE Applied Power Electron. Conf. and Expo.*, 2006, pp. 810–815.

[45] J.-S. Lai, J.H. Zhang, H.J. Yu, and H. Kouns "Source and Load Adaptive Design for A High-Power Soft-Switching Inverter," *IEEE Trans. Power Electron.,* vol. 21, no. 6, pp. 1667–1675, Nov. 2006.

[46] J. Liu, and Y. Yan, "A Novel Hysteresis Current Controlled Dual Buck Half Bridge Inverter", in *Proc. IEEE PESC*, 2003, pp. 1615-1620.

[47] Z. Yao, L. Xiao, and Y. Yan, "Dual-Buck Full-Bridge Inverter With Hysteresis Current Control", *IEEE Trans. Ind. Electron.,* vol. 56, no. 8, pp. 3153–3160, Aug. 2009.

[48] Z. Yao, L. Xiao, and Y. Yan, "Control Strategy for Series and Parallel Output Dual-Buck Half Bridge Inverters Based on DSP Control", *IEEE Trans. Power Electron.,* vol. 24, no. 2, pp. 434– 444, Feb. 2009.

[49] H. Qian, J.H. Zhang, and J.-S. Lai, "A grid-tie battery energy storage system", in *Proc. of IEEE COMPEL*, 2010, pp. 1-5.

[50] H. Qian, J.-S. Lai , J.H. Zhang, and W.S. Yu, "High-efficiency bidirectional AC-DC converter for energy storage systems", in *Proc. of IEEE ECCE*, 2010, pp. 3224-3229.

[51] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," *IEEE Trans. Ind. Electron.*, vol. 55, no. 3, pp. 1047–1058, Mar. 2008.

[52] Y.-M. Park, H.-S. Yoo, H.-W. Lee, M.-G. Jung, S.-H. Lee, C.-D. Lee, S.-B. Lee, and J.-Y. Yoo, "A simple and reliable PWM synchronization and phase-shift method for cascaded H-bridge multilevel inverters based on a standard serial communication protocol," in *Conf. Rec. 41st IEEE IAS Annu. Meeting*, Oct. 2006, vol. 2, pp. 988–994.

[53] B. N. Mwinyiwiwa, Z.Wolanski, and B. T. Ooi, "Microprocessor implemented SPWM for multiconverters with phase-shifted triangle carriers," in *Conf. Rec. IEEE-IAS Annu. Meeting*, NewOrleans, LA, Oct. 1997, pp.1542–1549.

[54] K. P. Louganski, and J.-S. Lai, "Current Phase Lead Compensation in Single-Phase PFC Boost Converters With a Reduced Switching Frequency to Line Frequency Ratio" *IEEE Trans. Power Electron.,* vol. 22, pp. 113–119, Jan. 2007.

[55] S.-Y. Park, C.-L. Chen, J.-S. Lai, and S.-R. Moon, "Admittance Compensation in Current Loop Control for a Grid-Tie LCL Fuel Cell Inverter", *IEEE Trans. Power Electron.,* vol. 23, no. 4, pp. 1716–1723,Jul. 2008.

[56] F. Blaabjerg, R. Teodorescu, M. Liserre, and A. V. Timbus, "Overview of Control and Grid Synchronization for Distributed Power Generation Systems", *IEEE Trans. Ind. Electron.,* vol. 53, no. 5, pp. 1398–1409,Oct. 2006.

[57] R. Teodorescu and F. Blaabjerg, "Proportional-resonant controllers. A new breed of controllers suitable for grid-connected voltage-source converters," in *Proc. OPTIM*, 2004, vol. 3, pp. 9–14.

[58] C.-L. Chen, Y. Wang, J.-S. Lai, Y.-S. Lee, and D. Martin, "Design of Parallel Inverters for Smooth Mode Transfer Microgrid Applications", *IEEE Trans. Power Electron.,* vol. 25, no. 1, pp. 6–15, Jan. 2010.

[59] C.-L. Chen, J.-S. Lai, Y. Wang, S.-Y. Park, and H. Miwa "Design and Control for LCL-Based Inverters with Both Grid-Tie and Standalone Parallel Operations", in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 2008, pp.1–7.

[60] H. Qian, J.H. Zhang, J.-S. Lai, and W.S. Yu, "A High-Efficiency Grid-Tie Battery Energy Storage System", *IEEE Trans. Power Electron.,* vol. 26, no. 3, pp. 886–896, May. 2011.

[61] J. Holtz, "Pulsewidth modulation—A survey," *IEEE Trans. Ind. Electron.,*vol. 39, pp. 410–420, Oct. 1992.

[62] J.W. Kolar, H. Ertl, and F.C. Zach, "Influence of the modulation method on the conduction and switching losses of a PWM converter system", *IEEE Trans. Ind. Applicat.,* vol. 27, no. 6, pp. 1063–1075, Nov./Dec. 1991.

[63] O. Alonso, P. Sanchis, E. Gubia, and L. Marroyo, "Cascaded H-bridge multilevel converter for grid connected photovoltaic generators with independent maximum power point tracking of each solar array," in *Proc. 34th IEEE Power Electron. Spec. Conf.*, 2003, vol. 2, pp. 731–735.

[64] E. Villanueva, P. Correa, J. Rodriguez, and M. Pacas, "Control of a Single-Phase Cascaded H-Bridge Multilevel Inverter for Grid-Connected Photovoltaic Systems," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4399–4406, Nov. 2009.

[65] S. Vazquez, J.I. Leon, J.M. Carrasco, L.G. Franquelo, E. Galvan, J.A. Sanchez, E. Dominguez, "Controller design for a single-phase two-cell multilevel cascade H-bridge converter," in *Proc. IEEE International Sympo. on Ind. Electron.*, 2008, pp. 2342–2347.

[66] C. Caluisi, C. Cecati, A. Piccolo, P. Siano, and A. Sindona, "Multilevel inverters and fuzzy logic for fuel cells power conditioning and control," in *Proc. IEEE International Sympo. on Ind. Electron.*, 2010, pp. 2739–2744.

[67] J.J. Negroni, D. Biel, F. Guinjoan, and C. Meza, "Energy-balance and sliding mode control strategies of a cascade H-bridge multilevel converter for grid-connected PV systems," in *Proc. IEEE International Conf.. on Ind. Tech..*, 2010, pp. 1155–1160.

[68] M. Calais, V.G. Agelidis, L.J. Borle, M.S. Dymond, "A transformerless five level cascaded inverter based single phase photovoltaic system," in *Proc. 31th IEEE Power Electron. Spec. Conf.*, 2000, vol. 3, pp. 1173–1178.

[69] R. Teodorescu, F. Blaabjerg, U. Borup, and M. Liserre, "A new control structure for grid-connected LCL PV inverters with zero steady-state error and selective harmonic compensation," in *Proc. of IEEE APEC*, Anaheim CA, March 2004, pp. 580-586.

[70] S.-Y. Park, C.-L. Chen, and J.-S. Lai, “A Wide-Range Active and Reactive Power Flow Controller for a Solid Oxide Fuel Cell Power Conditioning System”, *IEEE Trans. Power Electron.,* vol. 23, no. 6, pp. 2703–2709, Nov. 2008.

[71] T. C. Wang, Z. H. Ye, G. Sinha, and X. M. Yuan, “Output filter design for a grid-interconnected three-phase inverter,” in *Proc. of IEEE PESC*, Acapulco, Mexico, June 2003, pp. 779-782.

[72] M. Liserre, F. Blaabjerg, and S. Hansen, “Design and control of an LCL filter-based three-phase active rectifier,” *IEEE Trans. Industry Applications*, vol. 41, pp. 1281-1291, Oct. 2005.

[73] F. Liu, Y. Zhou, S. Duan, J. Yin, B. Liu, and F. Liu, "Parameter design of a two-current-loop controller used in a grid-connected inverter system with LCL filter," *IEEE Trans. Ind. Electron.*, vol. 56, no. 11, pp. 4483-4491, Nov. 2009.

[74] J. Dannehl, F. W. Fuchs, S. Hansen, and P. B. Thogersen, "Investigation of active damping approaches for PI-based current control of grid-connected pulse width modulation converters with LCL filters," *IEEE Trans. Ind. Appl.*, vol. 46, no. 4, pp. 1509-1517, July-Aug. 2010.

[75] G. Shen, X. Zhu, J. Zhang, and D. Xu, "A new feedback method for PR current control of LCL-filter-based grid-connected inverter," *IEEE Trans. Ind. Electron.*, vol. 57, no. 6, pp. 2033-2041, June 2010.

[76] H.F. Xiao, and S.J. Xie, “Leakage Current Analytical Model and Application in Single-Phase Transformerless Photovoltaic Grid-Connected Inverter”, *IEEE Trans. Electromagnetic Compatibility.,* vol. 52, no. 4, pp. 902–913, Nov. 2010.

[77] R. H. Baker, “Electric Power Converter”, US Patent 3867643, Feb. 1975.

[78] P.W. Hammond, “Medium Voltage PWM Drive and Method”, US Patent 5625545, Apr. 1997.

[79] P.W. Hammond, “A New Approach to Enhance Power Quality of Medium Voltage AC Drives”, *IEEE Trans. Ind. Appl.*, vol. 33, no. 1, pp. 202-208, 1997.

[80] R. H. Osman, “A Medium Voltage Drive Utilizing Series-Cell Multilevel Topology for Outstanding Power Quality”, in *Conf. Rec. IEEE-IAS Annu. Meeting*, Oct. 1999, pp.2662–2669.

[81] B. Wu, and P. Song, “Current Status of Multi-Megawatt AC Drives”, in *Conf. Rec. IEEE-ICIT*, Dec. 2004, pp.438–443.