Analysis and Design of Paralleled Three-Phase Voltage Source Converters with Interleaving

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Abstract

Three-phase voltage source converters(VSCs) have become the converter of choice in many ac medium and high power applications due to their many advantages, including low harmonics, high power factor, and high efficiency. Modular VSCs have also been a popular choice as building blocks to achieve even higher power, primarily through converter paralleling. In addition to high power ratings, paralleling converters can also provide system redundancy through the so-called (N+1) configuration for improved availability, as well as allow easy implementation of converter power management. Interleaving can further improve the benefit of paralleling VSCs by reducing system harmonic currents, which potentially can increase system power density. There are many challenges to implement interleaving in paralleled VSCs system due to the complicated relationships in a three-phase power converter system. In addition, to maximize the benefit of interleaving, current knowledge of symmetric interleaving is not enough. More insightful understanding of this PWM technology is necessary before implement interleaving in a real paralleled VSCs system.

In this dissertation, a systematic methodology to analyze and design a paralleled three-phase voltage source converters with interleaving is developed. All the analysis and

proposed control methods are investigated with the goal of maximizing the benefit of interleaving based on system requirement.

The dissertation is divided into five sections. Firstly, a complete analysis studying the impact of interleaving on harmonic currents in ac and dc side passive components for paralleled VSCs is presented. The analysis performed considers the effects of modulation index, pulse-width-modulation (PWM) schemes, interleaving angle and displacement angle. Based on the analysis the method to optimize interleaving angle is proposed. Secondly, the control methods for the common mode (CM) circulating current of paralleled three-phase VSCs with discontinuous space-vector modulation (DPWM) and interleaving are proposed. With the control methods, DPWM and interleaving, which is a desirable combination, but not considered possible, can be implemented together. In addition, the total flux of integrated inter-phase inductor to limit circulating current can be minimized. Thirdly, a 15 kW three phase ac-dc rectifier is built with SiC devices. With the technologies presented in this dissertation, the specific power density can be pushed more than 2kW/lb. Fourthly, the converter system with low switching frequency is studied. Special issues such as beat phenomenon and system unbalance due to non-triplen carrier ratio is explained and solved by control methods. Other than that, an improved asymmetric space vector modulation is proposed, which can significantly reduce output current total harmonic distortion (THD) for single and interleaved VSCs system. Finally, the method to protect a system with paralleled VSCs under the occurrence of internal faults is studied. After the internal fault is detected and isolated, the paralleled VSCs system can continue work. So system reliability can be increased.

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Chapter 1 Introduction

This chapter first introduces the background of paralleled three-phase voltage source converters with interleaving. After that, the existing research activities in this area are reviewed, which helps to formulate the work in this dissertation and identify its originality. The challenges and the major results to solve the corresponding issues with interleaving are then presented, followed by an explanation of the structure of the dissertation.

1.1 Background and Motivations

Three-phase PWM voltage source converters (VSCs) have become the converter of choice in many ac medium and high power applications due to their many advantages, including low line harmonics, high power factor, and high efficiency.[1]

Parallel operation of VSCs has also become a popular choice recently because of the benefits it can provide, including the following major aspects:

(1) High power. Even though a single converter can handle more and more power with the development of semiconductor devices, it is still far from enough to meet the power rating requirement for all applications. To achieve a higher power rating, one possible way is to parallel several converters together. [2]-[6] Theoretically, an unlimited power rating can be achieved with a parallel operation. Even though paralleled devices can also increase the system power rating. Paralleled VSCs is a better choice, since it is easier to achieve power balance and current sharing, as well as the potential to apply interleaving technology. [7][8]

(2) High reliability. Through the so-called (N+1) configuration, paralleling converters can provide system redundancy.[9]-[12] Thus, system reliability can be drastically improved using a parallel structure instead of a single-converter solution. High reliability is critical for many applications, such as stand-alone distributed power systems on shipboard, aircraft and in aerospace, main-frame computers and servers, etc.

(3) High flexibility. In the paralleling operation of converters, modular VSCs have been a popular choice as building blocks. Paralleling modular VSCs can bring much flexibility to the system design and operation. On one side, the power rating of the whole system can be adjusted or expanded easily with the flexibility for a gradual scaling up of power demand. On the other side, the total power can be distributed to different converters to achieve an easy implementation of converter power management.[13]

Interleaving can further improve the benefits of paralleling VSCs. This PWM technique interleaves or phase-shifts the converter switching cycles, which is done by phase shifting the gate control signals of the converters.

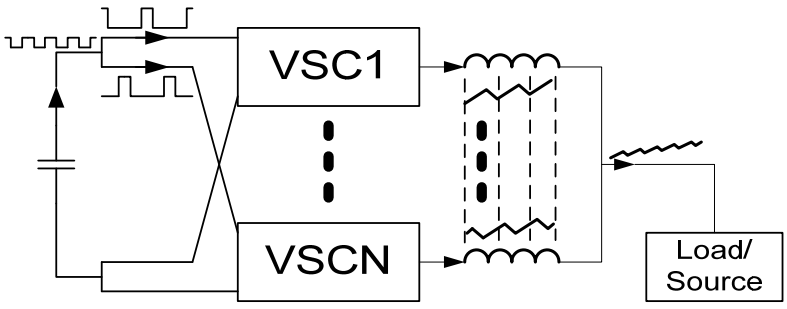

Figure 1-1. Harmonic reduction via interleaving.

As shown in **Error! Reference source not found.**, with interleaving, the total voltage ripple due to PWM switching at the ac terminal can be reduced [14][15]. Because

of the reduction of ripple voltage, the harmonic currents on the ac terminal can be reduced. In a similar way, the harmonics currents on the dc terminal can be reduced too [16] [17]. This brings many benefits to the converter system.

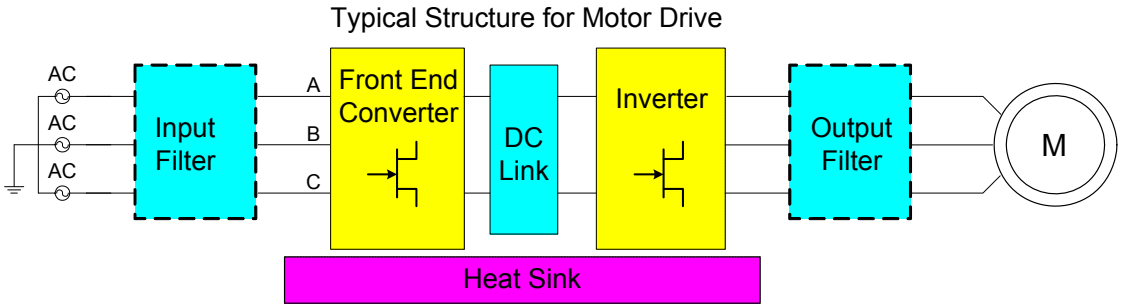

Figure 1-2. A typical structure for a motor drive with active front-end converter.

Error! Reference source not found. shows a typical structure for a motor drive. With the reduction of harmonic currents on the ac terminal, smaller filters and/or lower switching frequency can be used to meet the same harmonic currents limit. In addition, a lower switching frequency also means a lower power loss and smaller heat sink, causing the system power density and/or the system efficiency to improve. With the reduction of harmonic currents on the dc terminal, the power loss in the dc capacitor is reduced. Since dc capacitors, especially the aluminum electrolytic capacitors, are the weakest links in power electronic designs [18][19], interleaving can help to increase the system lifetime. In addition, if dc harmonic currents are limited by the number of paralleled dc capacitors, interleaving can help reduce the total volume of dc capacitors. In summary, interleaving has the potential to increase the system power density, efficiency and lifetime. This is very desirable for applications seeking to minimize the weight and volume of power electronics systems and for those that require a higher lifetime [20][21], e.g. aircraft application [22][23].

In order to realize the harmonic currents reduction on both the ac and dc terminal, there should not be any electrical isolation between a paralleled VSCS, such as a transformer. Such a directly (also called transformerless) paralleled three-phase converter system is also desirable in practice, because of the reduced cost and increased power density. [12][24] A directly paralleled three-phase converter system with interleaving presents very attractive characteristics, such as simplicity, easy expandability, high power density and high reliability.

Therefore there is a clear need for a systematic analysis and design approach for a paralleled three-phase voltage source converter system with interleaving, as well as a hardware implementation and verification. The literature review in the next section shows the state-of-the-art status of the research related to a paralleled three-phase voltage source converter system with interleaving, which helps to define the challenges and research topics of this work.

1.2 State-of-the-art Research

The use of paralleled three-phase PWM converters dates back to the late 1980s in motor drives [24] and uninterruptable power supply (UPS) applications[26][27]. Although almost 30 years have passed, paralleling with interleaving continues to have many benefits. However, most paralleling applications with interleaving are still for dc/dc converters only. Until recently, interleaving operation was not a common practice in paralleling three-phase power conversion. Instead, the paralleled three-phase VSCs are usually controlled in phase, avoiding any phase-shifting in carrier waveforms. This is because there are still some issues not resolved, prohibiting the widespread application of interleaving in the paralleling three phase power conversion.

1.2.1 Principle of Asymmetric Interleaving

To utilize the benefit of interleaving and maximize such benefit in different applications, it is necessary to, first comprehensively understand the principle of harmonic voltages or currents reduction via interleaving. After the analysis of interleaving in dc/dc applications [28][29], the impact of interleaving in a three-phase VSC system is usually analyzed in time domain [30][31]. It is easy to see a ripple current cancellation effect of interleaving in time domain, but the analysis in time domain lacks insight. For example, it is very difficult to study the impact of interleaving on the circulating current and the relationship between the harmonic currents reduction, especially if more than two VSCs are involved in the paralleling system. As a result, the conventional (also called symmetric) interleaving method is used, which means the carrier waves of each converter are phase-shifted by 1/N switching cycle for N paralleled VSCs system. This result is the same in the dc/dc converter.

Recently, people started to study the impact of interleaving on a paralleled three phase VSCs system in frequency domain [16][32][33][36]. Using the double Integral Fourier analysis method [37], the output ac harmonic currents cancellation effect of interleaving for N parallel three-phase VSCs system has theoretically been confirmed [16]. The impact of the non-conventional interleaving is also discussed in [33]-[35] and used in [36].

In summary, the previous work discussed above mainly focuses on symmetric interleaving and the impact of interleaving on system harmonic voltages and currents. There is no comprehensive analysis of how interleaving will impact system passive components design, especially when asymmetric interleaving is used. In-depth understanding of the correlations between system variables and interleaving impact is

still desired and the methodology to optimize unconventional interleaving based on different system requirement is still unknown.

1.2.2 Circulating Current Control

Circulating current is another issue that must be solved before paralleling operation of three phase VSCs with interleaving can be used for real applications. Circulating current always exists in paralleled VSCs because of the physical and control difference between each VSC. Direct parallel structure and interleaving can make this problem even worse, since there is no isolation between VSCs to block such circulating current and interleaving itself makes the operation of paralleled VSCS non-identical.

Circulating current among paralleled VSCs should be controlled to share power evenly and minimize additional loss. Basically, the circulating current can be classified into two groups by frequency. One's frequency is close to the fundamental frequency, which can be limited by control. The other one's frequency is comparable to switching frequency, which is usually out of the control bandwidth, so it can only be limited by passive components. Interleaving mainly affects the high frequency circulating current.

Much work has been done in solving the circulating current, both in control and passive component design.

Traditionally, an isolation method is used to block such circulating current. Separate ac or dc power supplies [26], [38]-[41], or a transformer-isolated ac-side[27], [42]-[45]is configured. With this approach, the overall paralleling system is bulky and expensive because of the additional power supplies or the ac line-frequency transformer.

Another choice of passive component is a high impedance reactor. Inter-phase inductor and CM inductor are often used to provide high impedance in the loop of

circulating current [45]-[50]. When interleaving is used, a high frequency CM circulating current will be introduced [31] which may increase the size of such reactor. Since those reactors are heavy and bulky compared with other components in the paralleling system, it is very important to design the structure of such a reactor carefully to limit the circulating current efficiently and make them as small and light as possible.

Even though the circulating current reactors have to be used, the design should not depend on them to limit low frequency circulating currents. Otherwise, they will be too heavy and bulky to bring the paralleling system into real application. Many works have dealt with the low frequency circulating currents. [51]-[56] and ref. [57] mainly focus on the control of circulating current on the DQ axis, which is also called load sharing. Although in some of these papers, isolated dc buses are used. Such a control method can still be used in the system with only a high impedance reactor. Ref. [57] and [59]-[61] mainly discussed the control of the CM circulating current on zero axis. Ref. [57] used a PI controller on zero axes in continuous central aligned space vector PWM (SVM) [62] to reduce the low frequency CM circulating significantly. Ref. [59] presented a hysteresis-control method for paralleling system with DPWM [63], but this method cannot limit the current small enough, especially when the system modulation index is low. However, none of these papers considered the impact of interleaving. Ref. [63] discussed the CM circulating current problem when interleaving is used with DPWM and claimed those two PWM techniques should not be used together.

In summary, in terms of circulating current control, previous work mainly focuses on the even distribution of power, which is done in a dq axis. The work to control low frequency CM circulating current is only suitable for continuous SVM, the

implementation of DPWM and interleaving is not considered possible. However, it is well known that DPWM can reduce the system switching loss, so it is very desirable to use those two techniques together to reduce the total power loss and increase power density. More work is needed to make this happen. In addition, to limit the high frequency circulating current, usually additional passive components are used, such as separate CM inductors and an inter-phase inductor. How to reduce the weight of such additional passive components either via physical design or control is an interesting and promising topic.

1.2.3 Interleaving in Systems with Low Carrier Ratio

In the literature survey above, the switching frequency is usually much higher than the fundamental frequency. However, very low carrier ratios, such as less than 15 are usually adopted in the applications with a very high power requirement where the performance of high voltage, high current devices limit the switching frequency. Especially, for applications involving a high-speed generator or motor, the carrier ratio will be extremely low, usually around 9. In many cases, even if the devices can operate at a higher switching frequency, it is also desirable to use a lower switching frequency, in order to reduce loss and increase power capability. It is usually very difficult, if not impossible, to build one converter to handle the total huge power, so a paralleling operation makes even more sense in these applications and it is really meaningful to apply the interleaving technique.

To avoid beat in this area, some studies show that the minimum ratio between switching frequency and fundamental frequency is 15–20. [64] Synchronization of PWM is necessary to eliminate beat when switching frequency is less than 15 times

fundamental frequency. [65] In addition, the patterns of synchronization PWM can affect the final output voltage. [66] Even for the selection of switching frequency, there is still argument. It is usually considered necessary to keep the ratio between switching frequency to be triplen [67][68], but [69] claims it is not necessary.

Some other papers have studied the performance of PWM with a low carrier ratio. Ref. [70] and [71]compared four kinds of space vector modulations, including the traditional asymmetric space vector modulation. Ref. [72] also investigated a synchronized space vector modulation for active front-end rectifiers in high-power current-source drive. However, these studies mainly focused on the impact of space vectors sequence on the performance of space vector modulation and the harmonic current performance of these space vector modulations are very similar. Ref. [73]-[75] proposed methods to optimize the harmonic performance of converters under space vector modulation control. But these methods cannot be used directly on the system with a very low carrier ratio. In addition, how to maximize the current THD reduction in a paralleled VSCs system with interleaving and ASVM is still unknown.

In summary, some special issues related to low switching frequency have not been explained well. There is still a lack of insight in designing a high power system with interleaving. In addition, the above-mentioned methods to reduce output current THD cannot be used directly for a low switching frequency case. It is desirable to develop some special PWM schemes for high power low switching frequency system to reduce output current THD. Also, how to maximize the benefits of interleaving in this area is still not clear.

1.2.4 Internal Fault Protection in Paralleled VSCs System

The last thing that should be mentioned is the protection of those directly paralleled systems. The downside of paralleling VSCs—as opposed to using a single converter rated at the total power—is the higher number of components, which reduces reliability as the possibility of faults in the system increases. [76] In consequence, only if the VSC under fault can be isolated from the system and replaced by a redundant VSC, can the reliability of the whole system be increased. This is the basis of the above-mentioned benefits of paralleling converters.

For external faults such as ac or dc side short circuits, the methods to protect VSCs are well known and have been discussed in [77]. But there are also internal faults including the short or open circuit of switches and diodes, which can be caused by the melting or lifting of wire bonds resulting from thermal cycling, gate-drive failure, or load over currents. The method to deal with an external fault cannot be applied to internal faults, since in this case not all switches can be controlled after an internal fault occurs. In this regard, [78]-[80] presented how to deal with the internal faults in a single VSC; however, the method and conclusions presented cannot be extended to a paralleled converter system as the fault effects between VSCs was not taken into consideration. These effects cannot be neglected as their impact can be catastrophic for the system, for instance, the result of the ensuing circulating current between VSCs after a fault. The occurrence of internal faults should then be studied in detail for systems with paralleled VSCs.

In summary, the existing work on protecting a system from external faults cannot be applied directly to internal faults. The internal fault detection, isolation and protection methods are not well studied.

1.3 Research Challenges and Objectives

From the survey above, the application of interleaving in a paralleled three phase VSCs system is still a new approach and there are many unsolved issues which obstruct the wide implementation of interleaving.

The main challenges include:

(1) Full understanding and explanation of interleaving impact on harmonic currents in three-phase power conversion applications, especially for asymmetric interleaving.

(2) Methodology to maximize the benefit of interleaving in a system passive components design to meet specific system requirements, such as ripple current or EMI standard.

(3) Use of DPWM in a paralleled VSCs system with interleaving.

(4) Weight minimization of additional passive components introduced by interleaving to increase power density.

(5) Extend the application of interleaving to systems with very low carrier ratio.

(6) Improvement of reliability for paralleled VSCs system under internal faults.

Corresponding to the challenges discussed above, the objective of this work is to develop a systematic methodology for the analysis and design of a paralleled three phase voltage source converter with interleaving and to verify the developed concepts with hardware. The dissertation accomplishes nine tasks:

(1)Performs a complete analysis studying the impact of interleaving on harmonic currents in ac and dc side passive components for multi-paralleled VSCs, considering all key variables.

(2)Provides a methodology to maximize the benefits of interleaving in passive components design to meet different system requirements.

(3)Develops the solution to implement DPWM and interleaving together, which is desirable, but not considered possible.

(4)Proposes two integrated inter-phase inductors to limit circulating current introduced by interleaving and the corresponding circulating current control method, which can minimize the total flux in such inductors when DPWM is used.

(5)Analyzes special issues for a system with very low switching frequency.

(6)Develops an improved asymmetric space vector modulation (ASVM) for a system with very low carrier ratio, which can significantly reduce output current THD for single and interleaved VSCs system.

(7)Analyzes the impact of a single device internal fault and proposes the fault detection and isolation methods.

(8)Builds a 2kW demo system to verify all the concepts and methodologies developed in this work.

(9)Designs and fabricates a high power density 15 kW three-phase ac/dc rectifier using SiC devices and the techniques developed in this work.

These nine items form the main content of this work. A review of the relevant literature is included within the introductory sections of each chapter.

1.4 Dissertation Organization

This work comprehensively deals with these issues mentioned above in paralleled three phase VSCs system with interleaving. The chapters are organized as follows.

Chapter 2 starts with a complete analysis studying the impact of interleaving on harmonic currents in ac and dc side passive components for paralleled VSCs. The analysis reveals the principle of asymmetric interleaving which is the theoretical basis for the dissertation. The analysis performed considers the effects of modulation index, pulse-width-modulation (PWM) schemes, interleaving angle and displacement angle. Based on the analysis the method to optimize interleaving angle is proposed.

Chapter 3 proposes the control methods for the CM circulating current of paralleled three-phase VSCs with DPWM and interleaving. With the control methods, DPWM and interleaving, which are desirable combinations, but not considered possible, can be implemented together. In addition, the total flux of the integrated inter-phase inductor to limit circulating current can be minimized.

Chapter 4 develops a 15 kW three phase ac-dc rectifier built with SiC devices. With the technologies presented in this dissertation, the specific power density can be pushed to more than 2kW/lb. In this chapter both the new digital controller named Nano, and the hardware architecture are described in detail. After that, the test results and system weight distribution are also presented.

Chapter 5 analyzes the converter system with low switching frequency. Special issues such as beat phenomenon and system unbalance due to non-triplen carrier ratio is explained and solved by control methods. Other than that, an improved asymmetric space vector modulation is proposed, which can significantly reduce output current total harmonic distortion (THD) for single and interleaved VSCs system.

Chapter 6 presents a systematic analysis of the impact of internal faults on paralleled VSCs system, and proposes methods to effectively detect and isolate the faulty devices

and converters. The impacts of four kinds of single device internal fault are analyzed in detail. Such internal faults can be detected and isolated. With the fault isolation, the paralleled VSCs system can continue to work, with increased system reliability.

Finally Chapter 7 summaries the entire dissertation and discusses some ideas for future work.

Chapter 2 Impact of Interleaving on System Ac and Dc Side Harmonic Currents

This chapter presents a complete analysis studying the impact of interleaving on harmonic currents in ac and dc side passive components for paralleled three-phase voltage-source converters (VSCs). The analysis considers the effects of the modulation index, different pulse-width-modulation (PWM) schemes, the interleaving angle and the power factor or displacement angle.

Based on the analysis, the impact of interleaving on the design of ac passive components such as ac line or boost inductor and electromagnetic interference (EMI) filter are discussed first. The results show that interleaving has the potential benefit to reduce the ac passive components. To maximize such benefit, interleaving angle should be optimized according to the system requirements including total harmonic distortion (THD) limit, ripple limit or EMI standards while considering operating conditions such as modulation index and PWM schemes.

Also interleaving can reduce the rms value of total ripple currents in the dc side passive components, which is used as the figure of merit. The results obtained show that all of the factors considered can strongly affect the rms value one way or another. The effect of circulating currents on the ripple currents in the dc side passive components is also taken into consideration to perform a more accurate analysis.

All the analysis is based on an example system containing two VSCs. However the proposed analysis method in frequency domain can be easily expandable for multiple paralleled VSCs. Experimental results are used to verify the analysis conducted.

2.1 *Introduction*

In ac medium and high power applications, three-phase PWM VSCs are very popular because of their many advantages, such as low harmonics, high power factor, and high efficiency [1]. The parallel operation of VSCs has also become a popular choice in order to achieve ever increasing power ratings [2-6]. In addition, parallel VSCs can also increase the system reliability through so-called N+1 configuration [7-10], as well as allow for the easy and flexible implementation of power management at the system level [11].

Interleaving can further improve the benefit of paralleling VSCs. This PWM technique interleaves or phase-shifts the converter switching cycles, which is done by phase shifting the gate control signals of the converters. [14] [17] To represent such phase-shifted switching cycles, the interleaving angle κ ($0 \le \kappa \le 2\pi$, or $0° \le \kappa \le 360°$) is defined in Figure 2-1. In the case of carrier-based PWM this is done by the actual phase shifting of the carrier signals for each converter, or in the case of space vector modulation (SVM) by interleaving their switching cycle clock. As a result, interleaving has as main benefit the reduction of harmonic currents at the input and output terminals of the converters, i.e., at the dc capacitor and ac boost inductors.

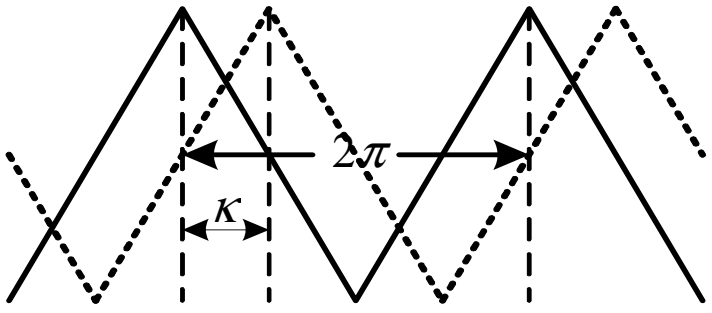

Figure 2-1. Definition of interleaving angle (κ).

As a result, the use of this PWM technique first has the potential to reduce the size of the converters ac passive components, increasing power density. This is very attractive for applications seeking to minimize the weight and volume of power electronics systems, e.g. aircraft application.

In addition, in a VSC system, the dc side passive components such as dc-link capacitors are usually the weakest points, as such determine the system reliability and lifetime [18]. This is mainly caused by thermal issues related to the ripple current flowing through the capacitors. To mitigate this problem, more capacitors can be paralleled to reduce the ripple current stress in them, at the expense of an increase system cost and volume. In fact, when the system current rating is increased by paralleling VSCs, the dc-link capacitors indeed become one of the most bulky components in the system. It is apparent then that the benefits of reducing the ripple current in a system of paralleled VSCs is threefold; namely increased lifetime, reliability, and power density.

There have been several papers studying the benefits of interleaving the paralleled three phase VSCs [30]-[35]. Ref. [30]and [31] show the reduction of ac line inductors and dc side ripple currents in two paralleled VSCs for an active power filter (APF) application. Using a time domain analysis method, it shows that interleaving reduced the ac line inductance to 70% while CM inductors are added to limit circulating current generated as a result of paralleling and interleaving. Ref. [32] [33], using double integral Fourier analysis method, theoretically proved the output ac harmonic current cancellation effect of interleaving for N paralleled three-phase VSCs system. In [30]-[32], symmetric interleaving angle was used, which means the interleaving angle κ was fixed to $2\pi/N$ for N paralleled ac three-phase VSCs system. Ref. [33] and [34]discussed the effect of

interleaving with asymmetric κ on ripple and an example was shown in [35]. However, there is still no discussion or analysis on κ selection criteria to fully utilize the benefit of interleaving in reducing the inductors and/or dc side ripple currents.

Furthering the past work, this chapter presents a systematic design method to reduce ac passive components and the dc side ripple currents through properly selecting the interleaving angle κ. Such method is based on a comprehensive analysis of the impact of interleaving on ac harmonics currents in paralleled three-phase VSCs with respect to a number of parameters: the modulation index (M, defined here as the ratio between the peak value of line-line voltage to dc bus voltage), the interleaving angle *(κ),* power factor or displacement angle between fundamental frequency currents and voltages (θ) and the PWM schemes. The methods to improve the benefit of interleaving by changing the interleaving angle under different operation conditions can be extended for N paralleled VSCs system.

All of these analyses are verified by experimental results based on a demo system.

2.2 Principle of Asymmetric Interleaving

The impact and benefit of interleaving are generally realized through selected harmonic current cancellation or reduction. Consequently, the analysis in this chapter will be mainly performed in frequency domain using the double integral Fourier analysis.[81] For clarity and simplicity, the analysis and discussion will be first carried out for the example system shown in Figure 2-2. The system consists of two paralleled VSCs fed from a common ac-bus and connected to a common dc bus, and the power flows from the ac source to the load represented by a dc link resistor. The naming conventions for

various currents and passive components are marked in the figure. There is no electrical isolation in the system such as transformer or isolated DC buses.

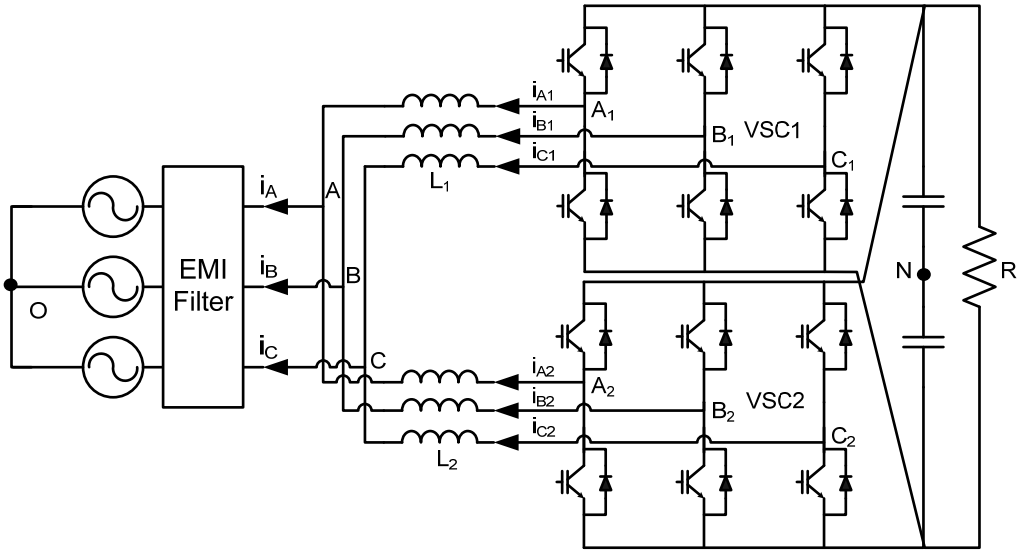

Figure 2-2. Sample converter system architecture under study.

From [81], the switched phase-leg output voltage between ac terminal (e.g. point A_1) and dc link mid-point (N), v_{A1N}, can be decomposed into different harmonics. The frequencies of harmonic voltage components can be expressed as ($m\omega_c$+ $n\omega_0$), where ω_c is the angular frequency of the carrier wave, ω_0 is the fundamental line frequency, and m and n are the carrier and baseband integer index respectively. Based on the double integral Fourier analysis approach, the harmonic component for voltage v_{A1N} corresponding to frequency ($m\omega_c$+ $n\omega_0$) can be expressed as in (2-1) [81]:

$$v_{A1N}(m,n)(t) = C_{mn}\cos\left[(m\omega_c + n\omega_0)t + m\theta_c + n\theta_0 + \theta_{mn}\right] \tag{2-1}$$

where C_{mn} is the harmonic amplitude, θ_c and θ_0 are the initial angles of the carrier and reference waves, and θ_{mn} is a constant value depending on PWM scheme and operation condition. C_{mn} and θ_{mn} can be obtained as in (2-2) from the double integral Fourier analysis. Note that C_{mn} is only function of PWM scheme and modulation index M. An

example for central aligned space vector modulation (SVM) is given in Table 2-1. Assuming the same carrier and symmetrical reference (with 120˚ apart) for the three phases for converter VSC1, its phase B and C voltage harmonic v_{B1N}(m,n), v_{C1N}(m,n) will be similar to (2-1) with identical C_{mn} and θ_{mn} but θ_0 will be displaced by 120˚.

$$C_{mn}e^{j\theta_{mn}} = \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{x_r}^{x_f} e^{j(mx+ny)}dxdy \tag{2-2}$$

Table 2-1 Double Fourier Integral Limits for SVM (Phase A)

y	x_r (rising edge)	x_f (falling edge)
$0<y<\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$
$\frac{\pi}{3}<y<\frac{2\pi}{3}$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$\frac{2\pi}{3}<y<\pi$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{\pi}{3}<y<0$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})]$
$-\frac{2}{3}\pi<y<-\frac{\pi}{3}$	$-\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$	$\frac{\pi}{2}[1+\frac{3}{2}M\cos y]$
$-\pi<y<-\frac{2}{3}\pi$	$-\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$	$\frac{\pi}{2}[1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})]$

For the group 2 converter VSC2, without interleaving (i.e., with identical carrier wave as group 1 converter), v_{A2N} will be identical to v_{A1N}. In general, for the example system in Figure 2-2, the harmonic currents in i_A are determined by the summation of harmonic currents in i_{A1} and i_{A2}, which are in turn determined by the harmonic voltages in v_{A1N} and v_{A2N} respectively, assuming the grid-side voltage source has no harmonic components. Also, assuming the inductances L_1 and L_2 are balanced and equal, the harmonic current in i_A corresponding to frequency ($m\omega_c + n\omega_0$) will be determined by the

average value of v_{A1N} (m,n) and v_{A2N} (m,n), or $v_{AN\text{-}avg}$ (m,n). Without interleaving, the amplitude of $v_{AN\text{-}avg}$ (m,n) remains the same as C_{mn}, i.e.

$$C_{mn\_ave} = 0.5\left(C_{mn1} + C_{mn2}\right) = C_{mn} \tag{2-3}$$

Interleaving phase shifts the carrier waves between VSC1 and VSC2. As a result, for the harmonic components at frequency ($m\omega_c + n\omega_0$) in v_{A1N} and v_{A2N}, their amplitudes will remain the same as C_{mn} in (2-2), but the angle will be different. Specifically, an angle shift of κ by the VSC2 carrier will result in $\Delta\theta_c = m\kappa$ angle shift for θ_c of v_{A2N} (m,n). Consequently, the amplitude of $v_{AN\text{-}avg}$ (m,n) with interleaving angle κ will become

$$C'_{mn\_ave} = 0.5\left|\left(C_{mn1} + C_{mn2}e^{jm\kappa}\right)\right| = C_{mn}\cos\left(m\kappa/2\right) \tag{2-4}$$

It can be seen that if κ is set to be π/m, i.e., interleaving the carrier wave of VSC2 by $1/m$ switching cycle and keeping the carrier wave of VSC1 unchanged, C'_{mn_avg} will be zero. In general, when certain κ is used, the relationship between the two vectors representing the two harmonic components at ($m\omega_c + n\omega_0$) in v_{A1N} and v_{A2N} can be shown as in Figure 2-3 and Figure 2-4. Especially, for the sample system shown in Figure 2-2, phase-shifting π can eliminate all odd order switching frequency harmonics and not affect the even order switching frequency harmonics. And phase-shifting $\pi/2$ will eliminate harmonics when m is (4k+2), such as 2, 6 and 10, reduce the harmonics by 30% (i.e. $1/\sqrt{2}$ of the original) when m is odd, and not affect other even order harmonics.

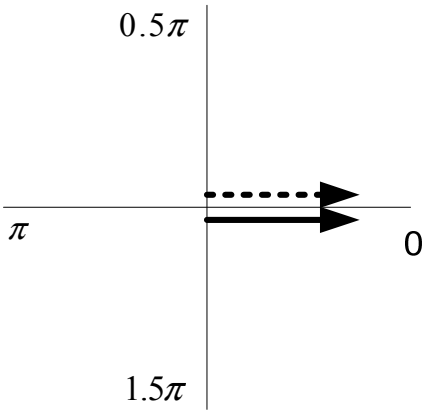

Figure 2-3. Relative phase angle of two VSCs harmonics without interleaving.

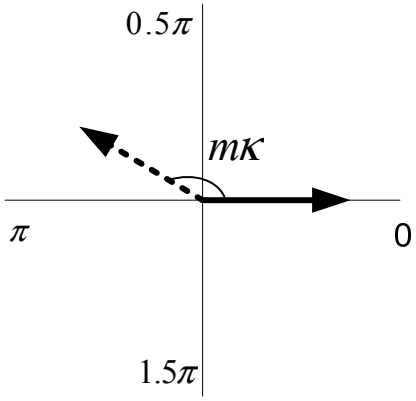

Figure 2-4. Relative phase angle of two VSCs harmonics with interleaving.

2.3 Impact of Interleaving on Ac Side Harmonic Currents

2.3.1 Principle of Ac side Harmonic Currents Reduction

The harmonic voltages, e.g. those in v_{A1N} and v_{A2N}, have both CM and differential mode (DM) components that can generally produce both CM and DM harmonic currents. Given that the converter system should have a high impedance CM path (e.g., high impedance between O and N in Figure 2-2), the current i_A is dominated by DM currents contributed from the DM components of i_{A1} and i_{A2}. Note that the impedance of the ac source is generally small compared with that of the VSC ac line inductor. Therefore, the DM harmonic voltage between A_1 and A is approximately the same as between A_1 and N, and the amplitudes of DM harmonic voltages across ac line inductor L_1 and L_2 cannot be changed by interleaving. Consequently, the amplitudes of corresponding DM harmonic currents in i_{A1} and i_{A2} will not be affected by interleaving. However, interleaving will reduce the amplitude of harmonic currents in i_A, because part of the DM harmonic currents in i_{A1} an i_{A2} are changed into circulating current not flowing into the ac source. Such circulating current can be determined by the difference of DM harmonic voltage in v_{A1N} and v_{A2N} as in (2-5):

$$C'_{mn\_diff} = C_{mn} \sin(m\kappa/2) \tag{2-5}$$

In fact, (2-5) can also be used to calculate the difference of CM harmonic voltages. Similar to DM harmonic voltages, the difference of CM harmonic voltages can generate CM harmonic currents, increasing the total harmonic currents in i_{A1} and i_{A2}. Without interleaving, such difference, theoretically, is zero. So no such CM circulating current exists in the system without interleaving.

Based on the analysis above, for each κ, current components in i_{A1} or i_{A2} can be classified into three groups shown in Figure 2-5 and Figure 2-6:

− Group A (I_{GA}): This current group is not affected by interleaving and always appears in i_{A1} and i_A. For example, when κ is π, I_{GA} includes the current components corresponding to even m^{th} and odd but non-triplen n^{th} order harmonics. It also always includes the fundamental current.

− Group B (I_{GB}): This current group always appear in i_{A1}, but will be changed into DM circulating current with interleaving, not appearing in i_A. For example, when κ is π, I_{GB} includes the current components corresponding to odd m^{th} and even but non-triplen n^{th} order harmonics.

− Group C (I_{GC}): This current group is CM circulating current, introduced as a result of interleaving. For example, when κ is π, I_{GC} includes the current components corresponding to odd m^{th} and triplen n^{th} order harmonics.

The other harmonic voltages corresponding to even m^{th} and triplen n^{th} order are CM harmonic voltages that are still in phase when κ is π. For other κ, such as $\pi/2$, the definition of I_{GA}, I_{GB} and I_{GC} remain the same but the harmonic currents in each group vary. And the harmonic currents at certain frequency will contain I_{GA} and I_{GB} at the same time, since it can only be partially changed into circulating current.

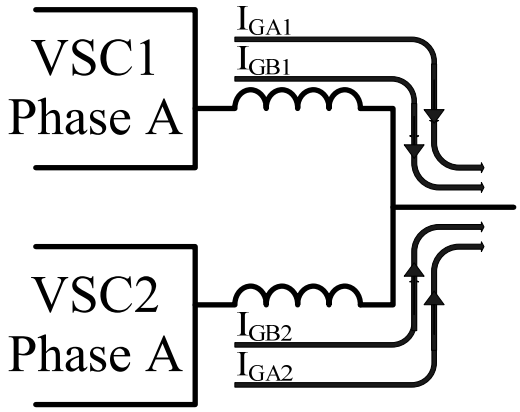

Figure 2-5. System harmonic currents without interleaving.

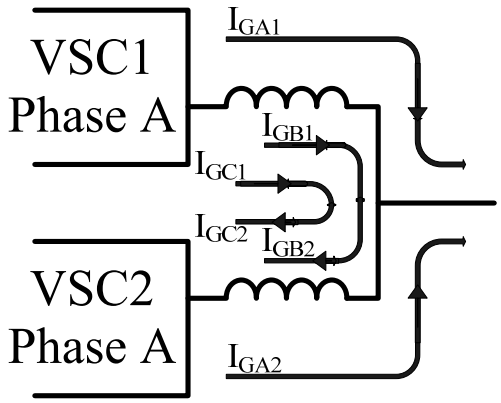

Figure 2-6. System harmonic currents with interleaving.

In summary, based on the above analysis, the following observations can be generally made on ac current harmonics:

1) The harmonic currents of i_A can be reduced by interleaving with the same source conditions (i.e. same ac line inductance) since I_{GB} has been converted into circulating current that will not appear in i_A.

2) Under the same conditions, the amplitude of i_{A1} or i_{A2} may actually be increased because of CM circulating current I_{GC} introduced by interleaving.

The above analysis already qualitatively showed the impact of interleaving angle κ on harmonic currents, which will in turn impact the ac passive components. The selection of interleaving angle κ should be based on the PWM schemes, operating conditions and design objectives. Every PWM strategy has its own unique harmonic spectrum, which will affect the result of interleaving. In practice, central aligned continuous SVM (simply called SVM in this dissertation) [62] and DPWM [63] are most often used. Thus, these two PWM schemes are used here to demonstrate the interleaving angle impact and selection. The operating conditions for VSC are characterized mainly by modulation index. Since the focus of this section is on ac passive components, the design objectives can be minimum output harmonic current and/or maximum corner frequency of EMI filter. And the analysis is based on the sample system in Figure 2-2. In the analysis, the nominal ac phase to neutral rms voltage is 230 V, the dc bus voltage is 650 V and the load power is 10 kW. A fundamental frequency of 400 Hz is used.

2.3.2 Harmonic Currents Reduction with SVM and THD Limit

In many applications, there are limits on ac harmonic or ripple currents for power quality. Often, the THD is used as a design constraint. When the switching frequency is not very high, e.g. 20 kHz for a 400 Hz fundamental frequency, such limit mainly determines the size of inductor. Since EMI filters are only designed to limit very high frequency harmonics (e.g. > 150 kHz for many conducted EMI standards), ac line inductor L1 and L2 are considered to be the only passive components limiting ripple currents. It can be shown that the THD of i_A in Figure 2-2 system can be strongly influenced by interleaving angle κ. In other words, κ can be selected to minimize the THD of i_A.

For the analysis in this section, the switching frequency is arbitrarily selected to be 20 kHz. However, since the fundamental frequency and switching frequency cannot affect the amplitude of harmonic components, which can be seen from (2-2), and in addition, the harmonic currents reduction of interleaving only relies on the order of switching frequency, such selected switching frequency will not affect the analysis method and conclusions.

The spectrum of output harmonic voltage without interleaving can be obtained using the double integral Fourier analysis, with (2-2). For SVM, the integral limits for the example system are given in Table 2-1. The frequency spectrum of harmonic components of PWM waves when modulation index M is 0.5 and 0.9 are shown in Figure 2-7 and Figure 2-8. The amplitudes of each harmonic component are normalized based on V_{dc}.

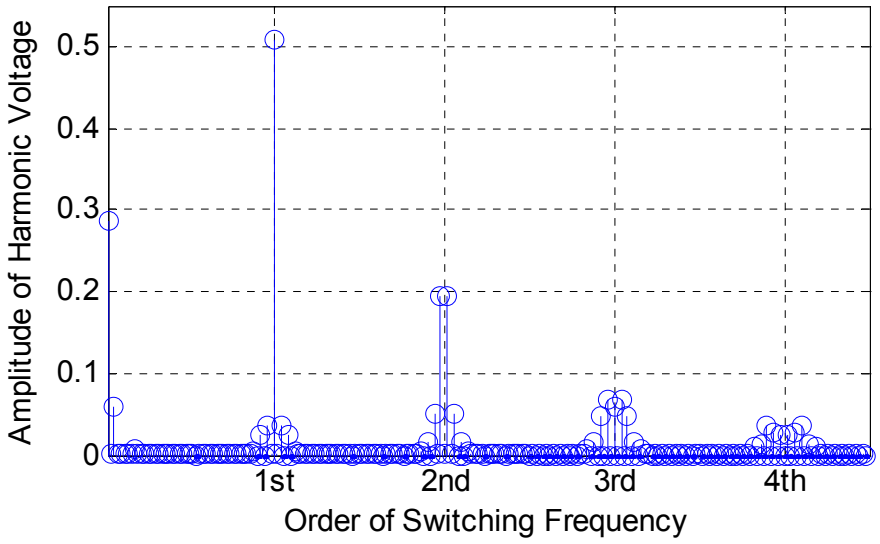

Figure 2-7. Spectrum of PWM for center aligned continuous SVM (M=0.5).

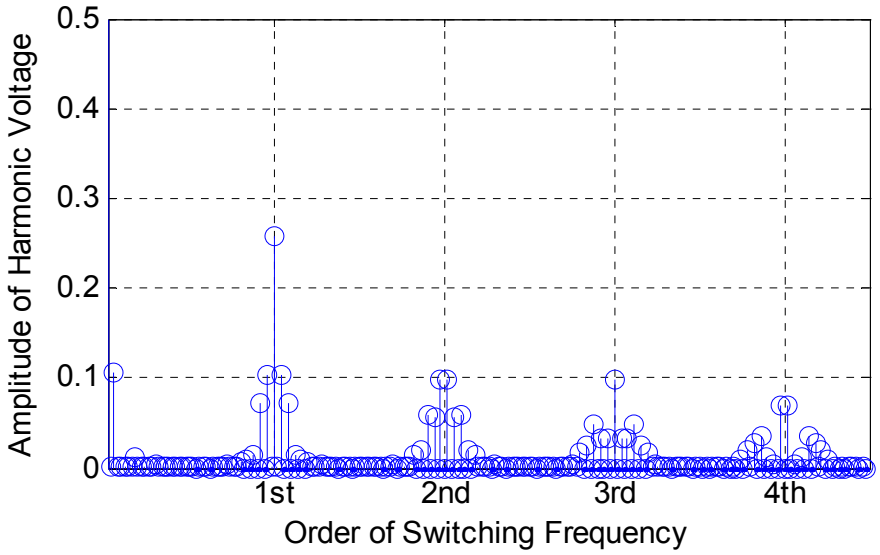

Figure 2-8. Spectrum of PWM for center aligned continuous SVM (M=0.9).

From Figure 2-7 and Figure 2-8, it can be seen that harmonic energy will concentrate more around switching frequency when *M* is high, On the contrary, more harmonic energy will concentrate around twice the switching frequency when *M* is low. The highest harmonic component at switching frequency is, as mentioned above, CM component which cannot create CM harmonic current in i_{A1} without interleaving.

Similarly, the frequency spectrum of harmonic components with DPWM when *M* is 0.5 and 0.9 are shown in Figure 2-9 and Figure 2-10. The fundamental and switching frequencies are kept the same as in SVM case. From Figure 2-9 and Figure 2-10, it can be seen that harmonic energy will concentrate more around switching frequency no matter whether *M* is high or low, which is an opposite result when compared to SVM. The spectrum of other PWM schemes can be obtained in a similar way.

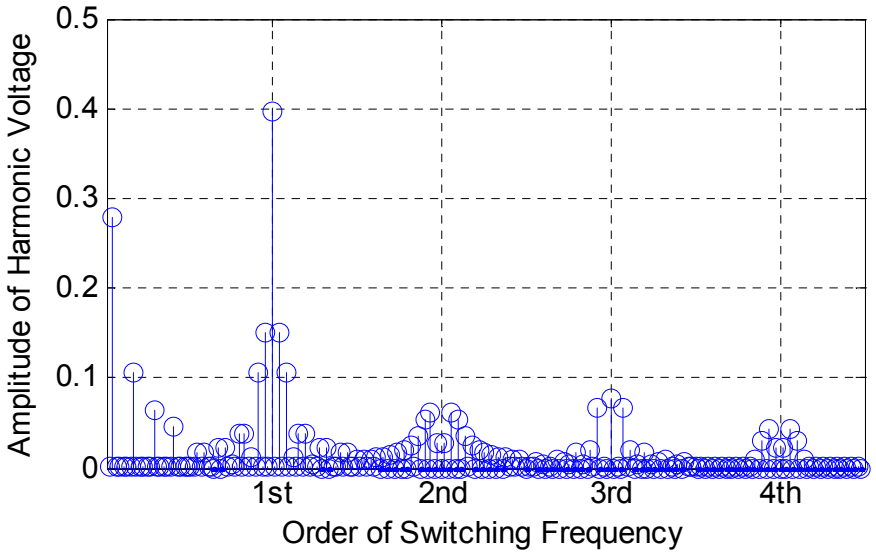

Figure 2-9. Spectrum of PWM DPWM (M=0.5).

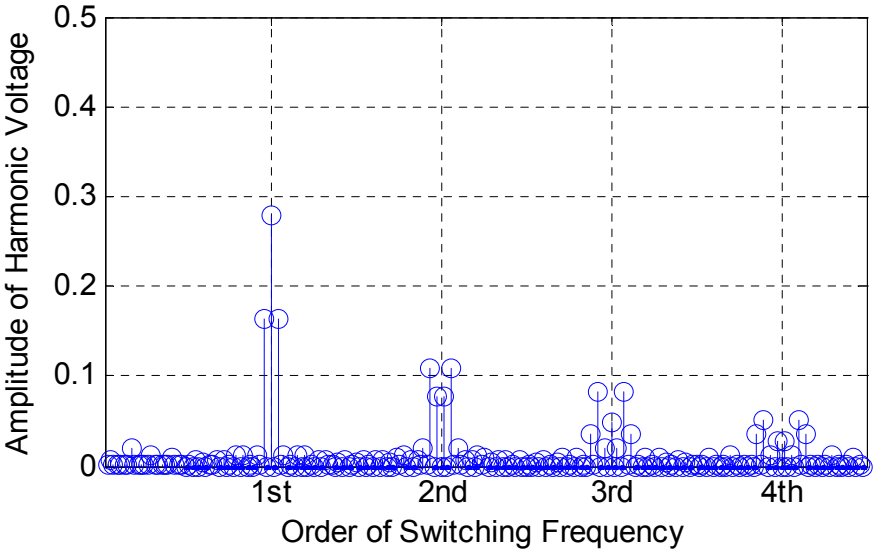

Figure 2-10. Spectrum of DPWM (M=0.9).

Based on the voltage spectrum, the harmonic current amplitude at the frequency $(m\omega_c + n\omega_0)$ for i_A can be calculated as

$$i_A(m,n) = \frac{2C_{mn}\cos(m\kappa/2)}{(m\omega_c + n\omega_0)L} \tag{2-6}$$

where L is the inductance for the ac line inductors L1 and L2, which are assumed identical. Then corresponding THD is

$$\mathrm{THD} = \frac{\sqrt{\sum_{m=0}^{\infty}\sum_{n=-\infty}^{\infty} i_A^{\,2}(m,n)}}{I_f} \tag{2-7}$$

where I_f is the rated peak current of the fundamental component in i_A. Figure 2-11 shows the normalized THD as function of modulation index M for two interleaving angles π and $\pi/2$ with SVM scheme, where THD without interleaving is assumed to be unity. The normalized THD reduction with interleaving is independent of inductance L. Figure 2-11 shows that $\kappa=\pi/2$ is better when M is low, since $\pi/2$ interleaving can reduce the 1st order switching harmonics while canceling the 2nd order switching harmonic, which is significant for SVM at low M as shown in Figure 2-11. When M is high and harmonic energy concentrates at the switching frequency (see Figure 2-8), $\kappa= \pi$ is better. An overall best interleaving angle between $\pi/2$ and π can be selected through a compromise between canceling the 1st order and 2nd order switching harmonics considering modulation index range. In principle, the interleaving angle may be varied under different modulation indexes to achieve the minimum value of THD dynamically. The theoretical minimum THD reduction corresponding to the "optimal" κ is also shown in Figure 2-11.

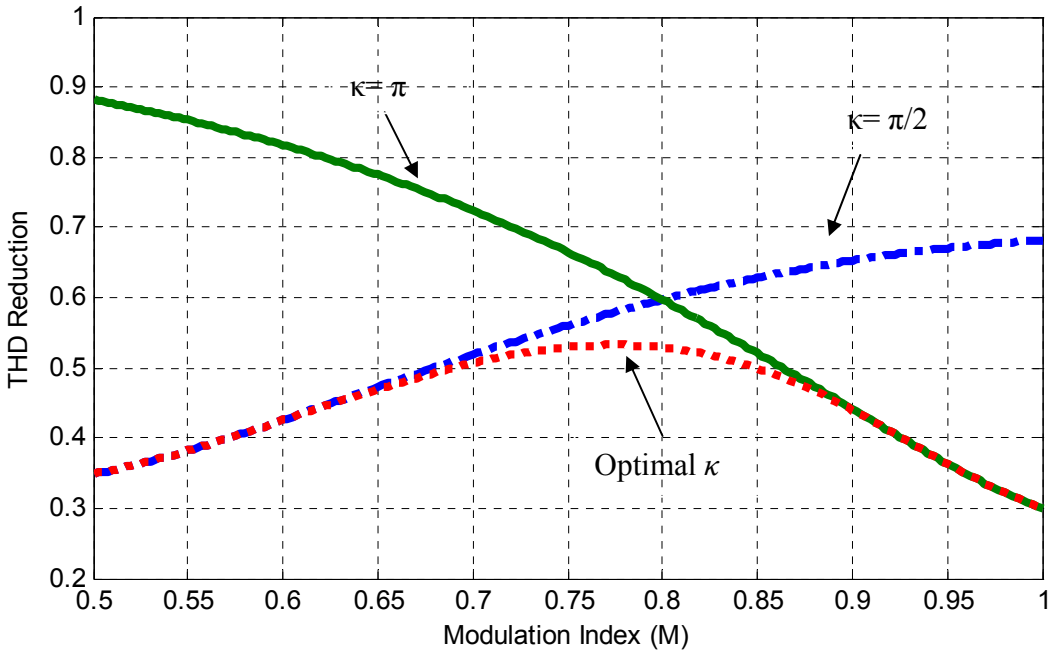

Figure 2-11. Impact of interleaving angle on THD reduction for central aligned SVM.

For DPWM, since the harmonic currents around 1st order switching frequency always dominate, $\kappa = \pi$ is overall better to minimize ac current THD.

2.3.3 Harmonic Currents Reduction with DPWM and EMI Limit

In some applications, EMI filter, usually made up with passive capacitors and inductors, is required and often contributes significantly to the size, weight, or cost of the overall converter. For a passive EMI filter, the corner frequency can determine the required capacitance and inductance values, and the corresponding component size [24]. A higher corner frequency generally indicates smaller passive components needed for EMI filter. Therefore, for a paralleled interleaved VSC system, the interleaving angle should be selected to increase such corner frequency. In practice, EMI filters are often designed separately for DM and CM noise. For illustration purpose, the impact of

interleaving angle is discussed here through a design example of the corner frequency for a DM EMI filter.

In the example design, the converter system as shown in Figure 2-12 has a two-stage LC EMI filter. The system parameters are the same as in section A except the switching frequency is 70 kHz. DPWM is assumed and the EMI standard in DO-160E as shown in Figure 2-13 should be met. For such high switching frequency, the ac line inductor L1 and L2 can be considered the first stage inductor (L_{1st}) of EMI filter [82].

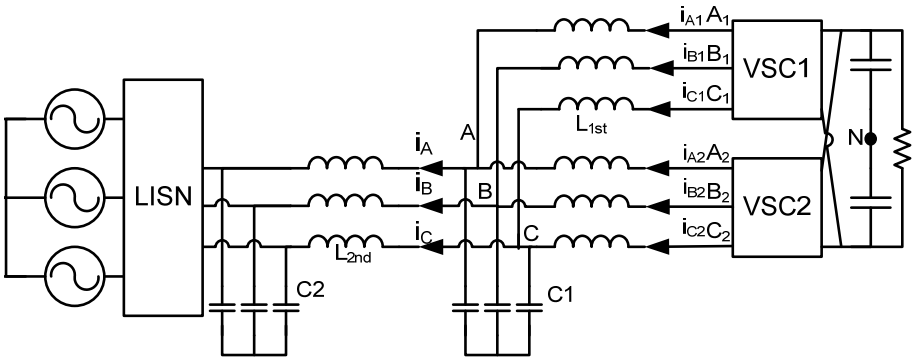

Figure 2-12. EMI filter topology under study.

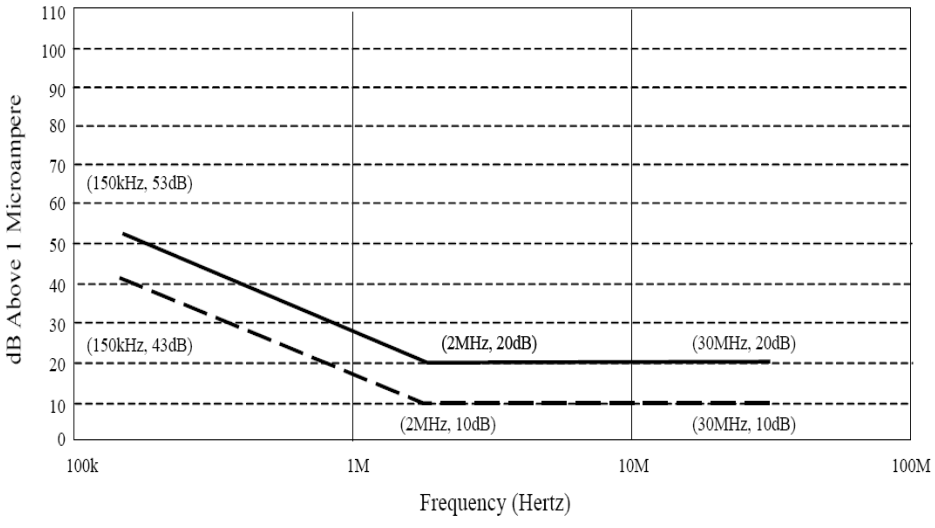

Figure 2-13. EMI standard based on DO-160E [82].

Assuming that the nominal modulation index M is 0.9, the spectrum of v_{AIN} is calculated and shown in Figure 2-14. The spectrum is shown from 150 kHz as in the case of the standard in Figure 2-13. Note that in Figure 2-14, voltage in dBμV is used instead of current in dBμA as in Figure 2-13 for easy comparison. The voltage requirement in Figure 2-14 is obtained by multiplying the current requirement in Figure 2-13 with the LISN impedance of 50Ω. In addition, since the EMI standard is for the total harmonic currents including both DM and CM, the EMI standard is reduced by 6dB for DM EMI filter design considering the margin needed for CM EMI filter.

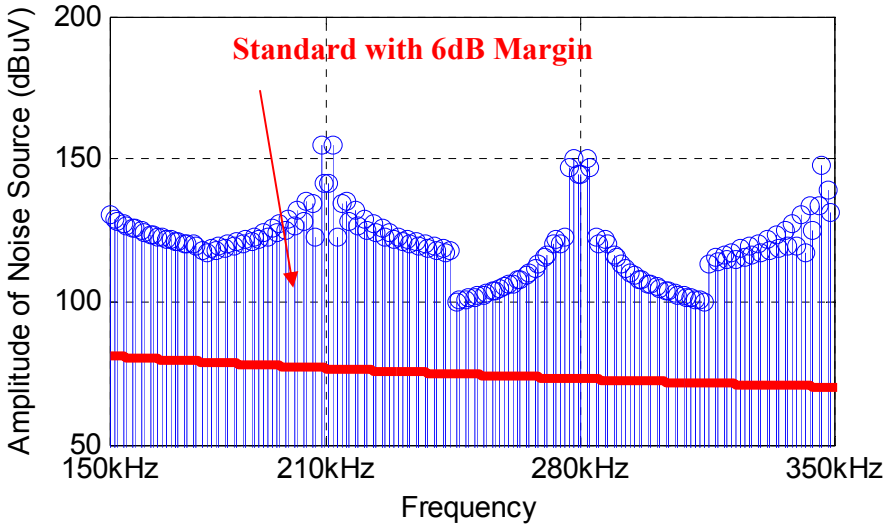

Figure 2-14. Spectrum of V_{AIN} without interleaving.

From Figure 2-14, the required attenuation can be obtained as shown in Figure 2-15. Considering the 80 dB/dec attenuation slope of the selected two-stage EMI filter, the dominant harmonic voltage is located at 208.4 kHz and the attenuation needed is 77.78 dB. Based on these values, the two-stage EMI filter corner frequency can be determined to be 22.2 kHz [83].

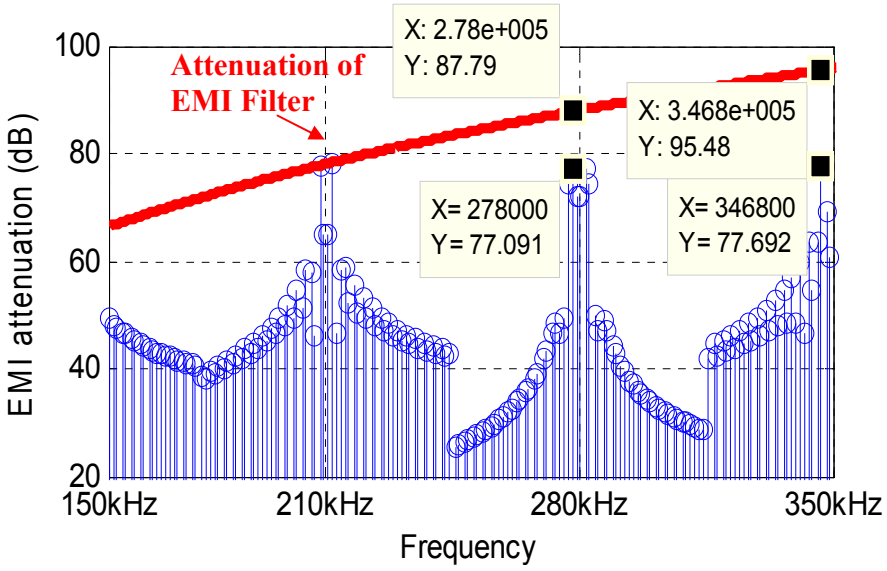

Figure 2-15. Attenuation required without interleaving.

Seen from (2-4), interleaving can reduce the amplitude of DM output harmonic voltages by a factor of $\cos(m\kappa/2)$. In this design example, the dominant harmonic voltage is around the 3rd order switching frequency where m=3. If symmetric interleaving is used, κ is π and the original dominant harmonic voltage at 210 kHz will be eliminated. The harmonic voltage close to 280 kHz (278 kHz) becomes the new dominant harmonic as shown in Figure 2-16.

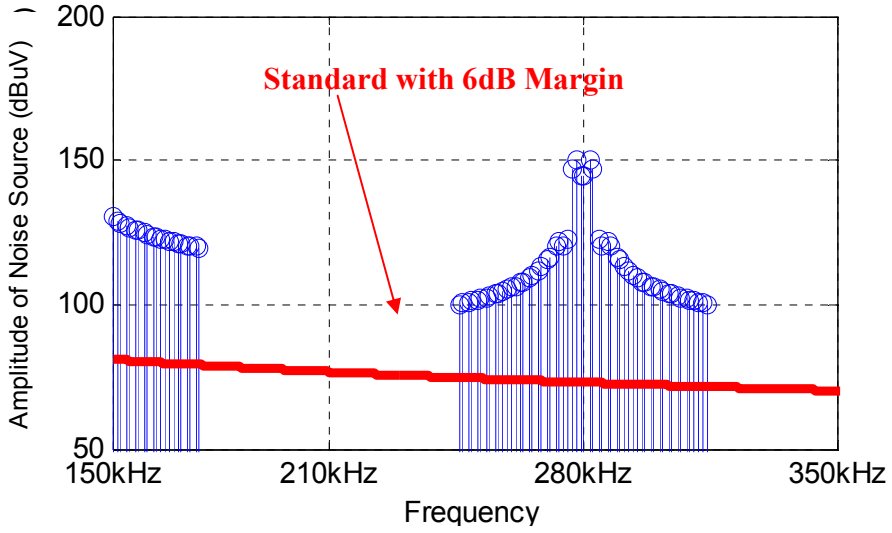

Figure 2-16. Spectrum of v_{AIN} with interleaving angle π.

From Figure 2-16, the required attenuation with interleaving angle κ =π, can be obtained as shown in Figure 2-17. It can be determined that 77.1 dB attenuation is needed at 278kHz and the two-stage EMI filter corner frequency will be increased to 30.4kHz.

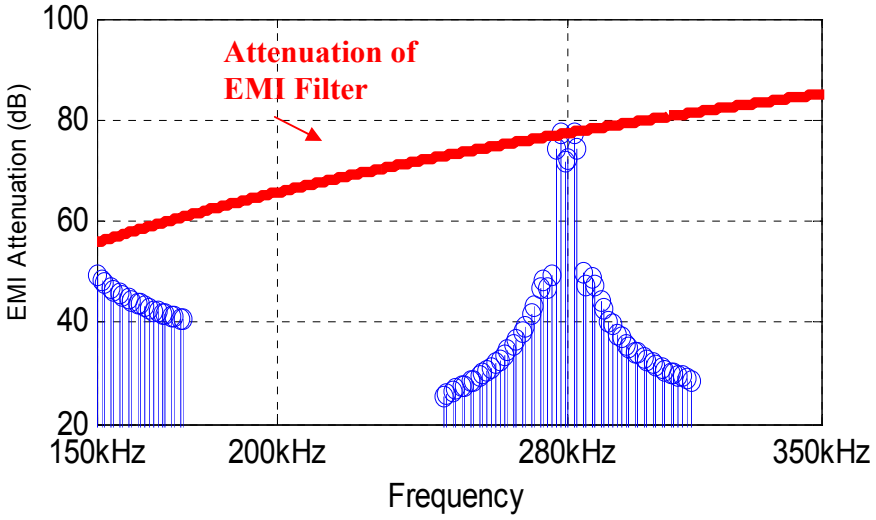

Figure 2-17. Attenuation required with interleaving π.

Note that in Figure 2-15, to maximize the benefit of interleaving, κ can be selected such that more than one harmonic can be "dominating" and the filter can attenuate all of them at the same time. In the design example, κ should be selected to reduce the amplitude of harmonics from 210 kHz to 350 kHz together. From Figure 2-15 the original margins for the 4th order and 5th order harmonic voltages when 3rd order harmonics hit the attenuation of EMI filter are 11 dB and 18 dB separately. For an interleaving angle κ, the margins for 3rd, 4th and 5th order harmonics can be generally calculated as

$$M3 = -20\log(\cos(1.5\kappa)) \tag{2-8}$$

$$M4 = 11 - 20\log(\cos(2\kappa)) \tag{2-9}$$

$$M5 = 18 - 20\log(\cos(2.5\kappa)) \tag{2-10}$$

Since the attenuation of EMI filter is determined by the minimum value among M3, M4 and M5, the optimized interleaving angle κ should maximize the minimum value among M3, M4 and M5. Finally κ can be calculated to be about 0.31π. New margins M3, M4 and M5 are 18.4 dB, 18.3 dB and 20.4 dB with such optimized κ. As a result, the third order and fourth order harmonics will become dominant together. New spectrum of DM harmonic voltages and the attenuation needed with interleaving are shown in Figure 2-18 and Figure 2-19.

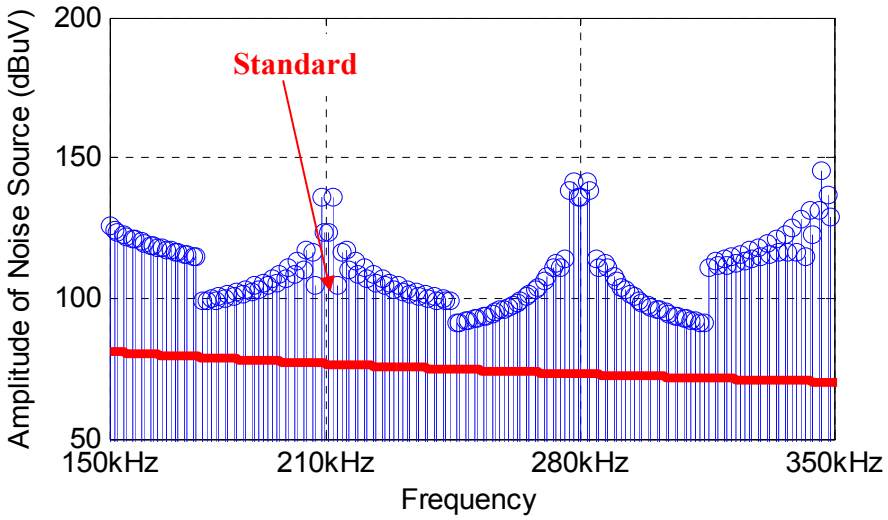

Figure 2-18. Spectrum of v_{AIN} with interleaving 0.31π.

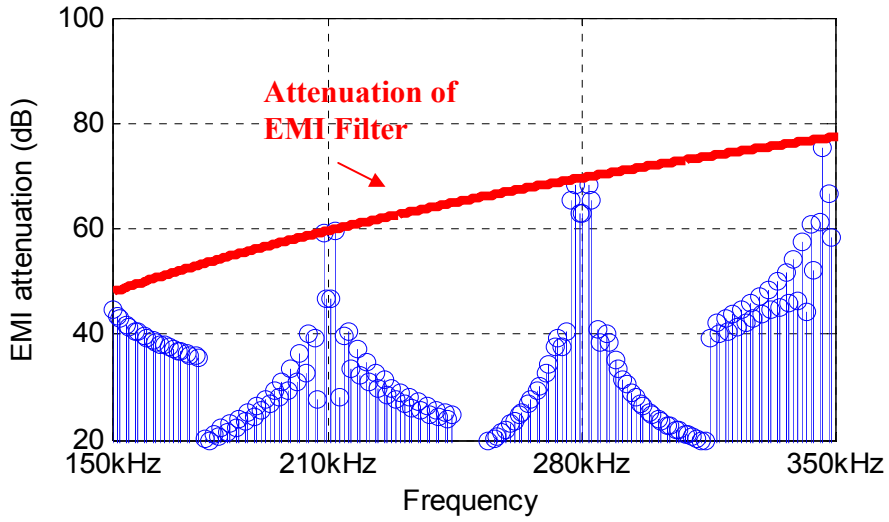

Figure 2-19. Attenuation required with interleaving 0.31π.

From Figure 2-19 the dominant harmonic voltage will be either at 208.4 kHz or 278 kHz as designed. And based on the attenuation needed, the two-stage EMI filter corner frequency is further increased to 37.8 kHz.

The same analysis method can be applied to CM EMI filter. And a trade-off may be necessary between CM and DM EMI filter reduction.

2.3.4 Experimental Results on Ac Side Harmonic Currents

The experiment is designed to verify three key points in the analysis above. First, the designed interleaving angle can reduce ac harmonic currents at each order of switching frequency to expected level. Second, inter-phase inductor can limit the circulating current, reducing the rms and peak values of the current through VSCs. Third, the ripple current in output harmonic currents can be reduced significantly.

To simplify the experiment, the inverter configuration in Figure 2-20 is used, whose voltage harmonic spectrum are the same as in the case of the rectifier configuration in Figure 2-2. The ac side now has a three phase resistor load in addition to inductors. Since

at switching frequency, the resistance is much smaller than the impedance of ac inductors, the harmonic currents are still determined by the inductors and harmonic voltages. Therefore, the analysis in previous sections applies to the experimental configuration of Figure 2-20. Also the function of L_{3ph} in Figure 2-20 is realized by the leakage inductance of inter-phase inductors.

The experimental setup comprises of two 6-pack IGBT intelligent power modules (IPMs) from Fuji (6MBP20RH060) for two VSCs power stage, one common DSP-FPGA digital controller, three inter-phase inductors as shown in Figure 2-21, and three 10Ω resistors as load. As discussed above, the leakage inductance of inter-phase inductor L_{leak} is used as ac line inductor which is 320μH and the main inductance L_{ip} is used to limit circulating current which is 3mH. The dc voltage is 200V, and the fundamental and switching frequency are chosen as 200Hz and 20 kHz respectively. The rms value of fundamental current in the resistor load is 8A with corresponding modulation index of 0.8. DPWM is used.

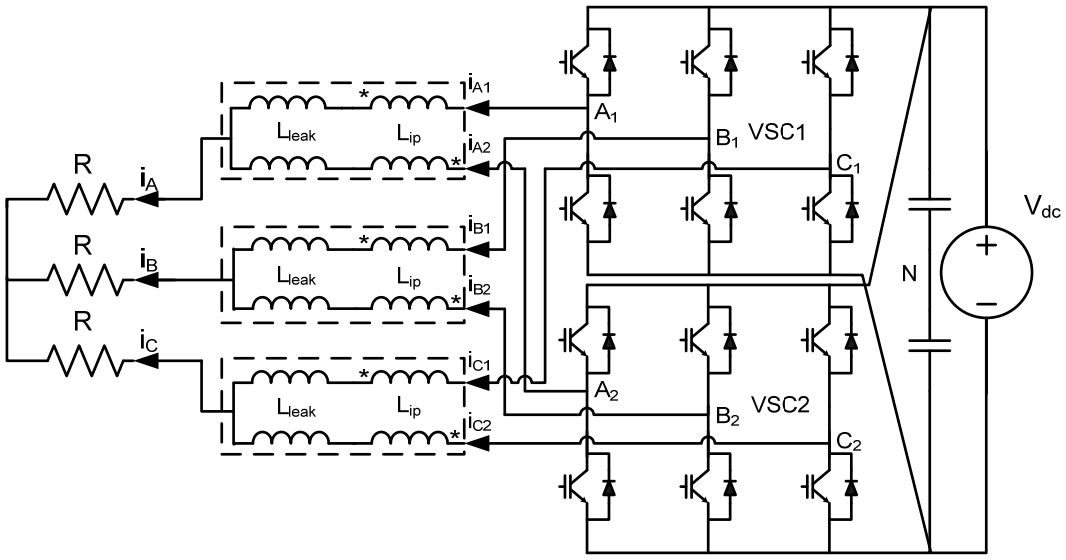

Figure 2-20. Schematic of the experimental setup.

Figure 2-21. Inter-phase inductor.

The experimental ac side waveforms for selected interleaving angles are shown in Figure 2-22 through Figure 2-27. The current THD value and rms value of fundamental components in all currents are summarized in Table 2-1.

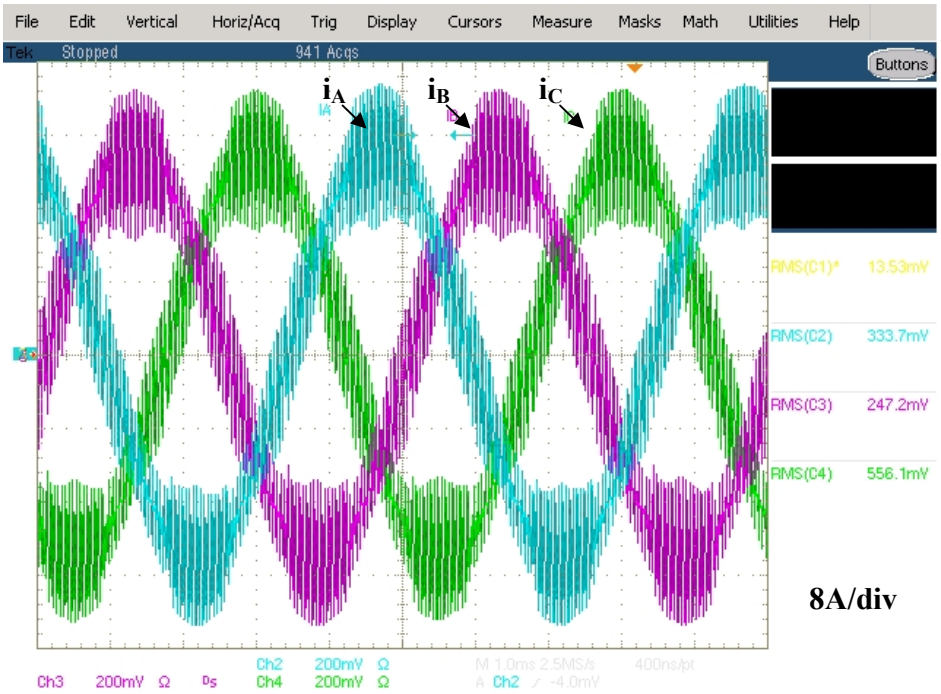

Figure 2-22. Waveforms of i_A, i_B and i_C when $\kappa = 0$.

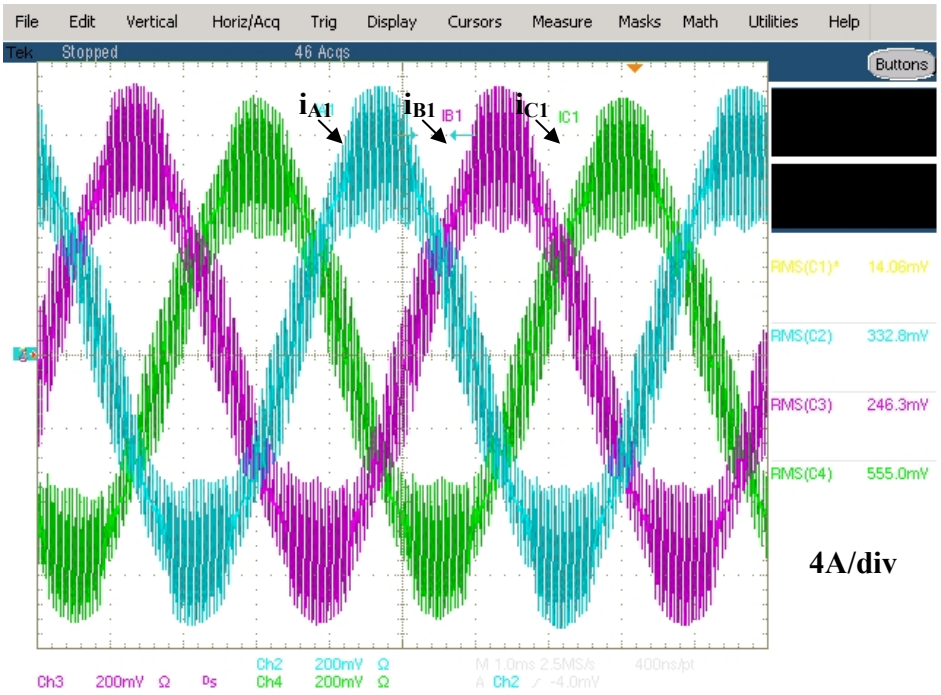

Figure 2-23. Waveforms of i_{A1}, i_{B1} and i_{C1} when $\kappa = 0$.

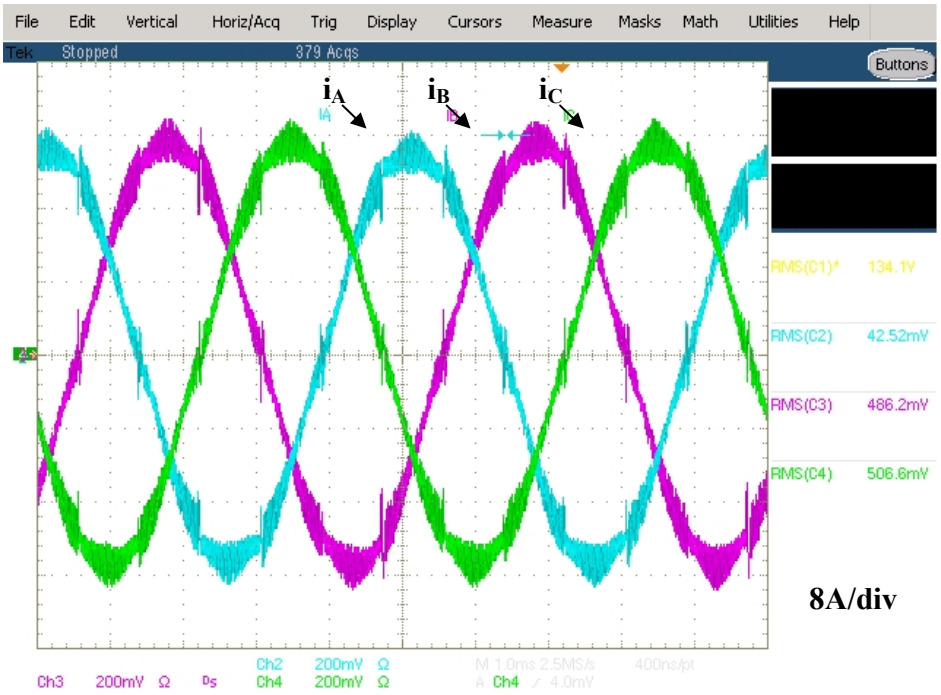

Figure 2-24. Waveforms of i_A, i_B and i_C when $\kappa = \pi$.

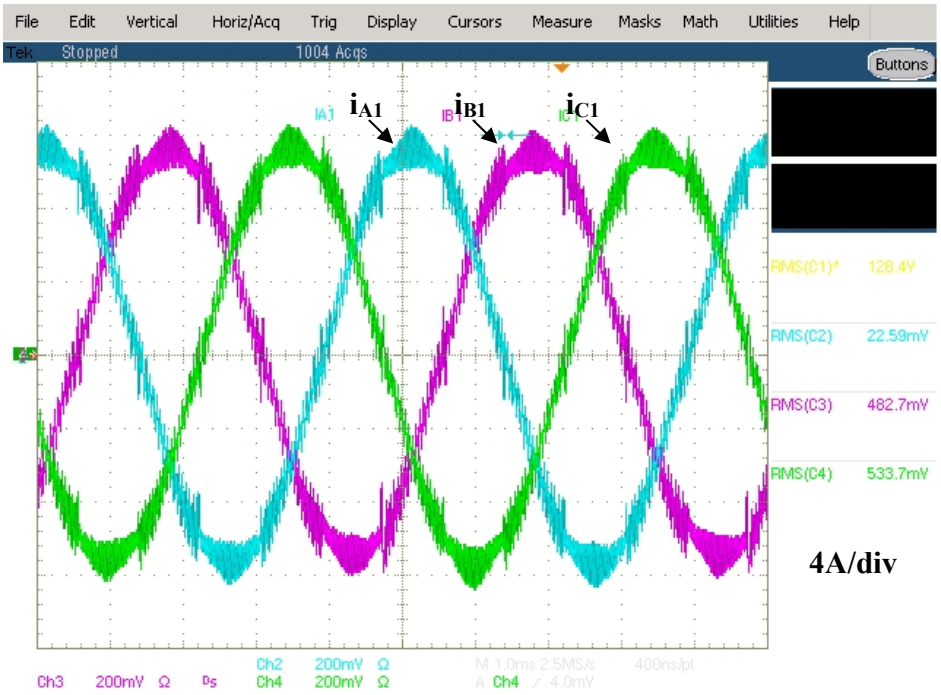

Figure 2-25. Waveforms of i_{A1}, i_{B1} and i_{C1} when $\kappa = \pi$.

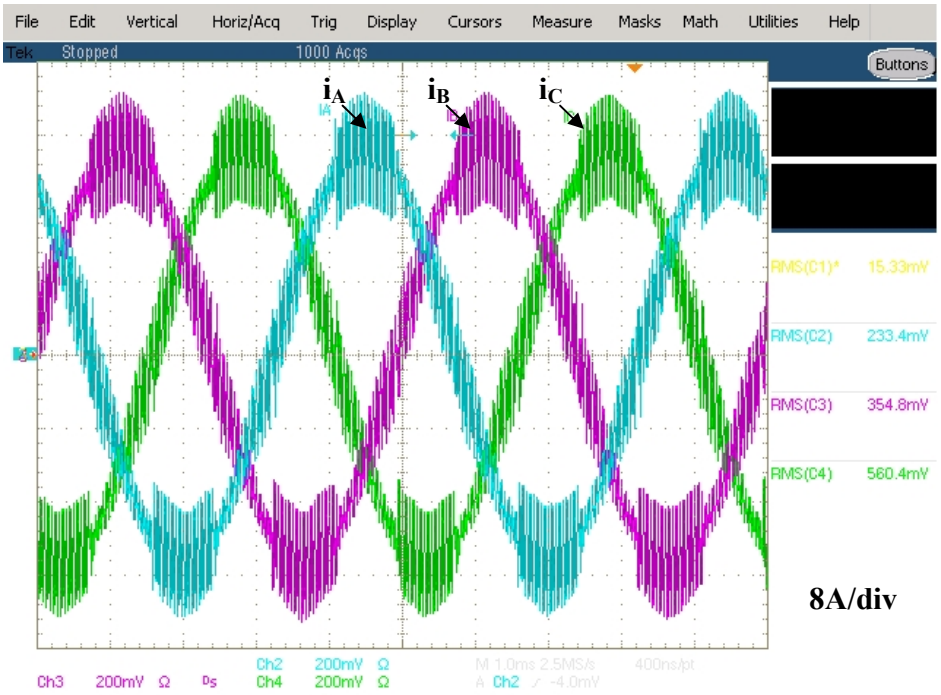

Figure 2-26. Waveforms of i_A, i_B and i_C when $\kappa = 0.31\pi$.

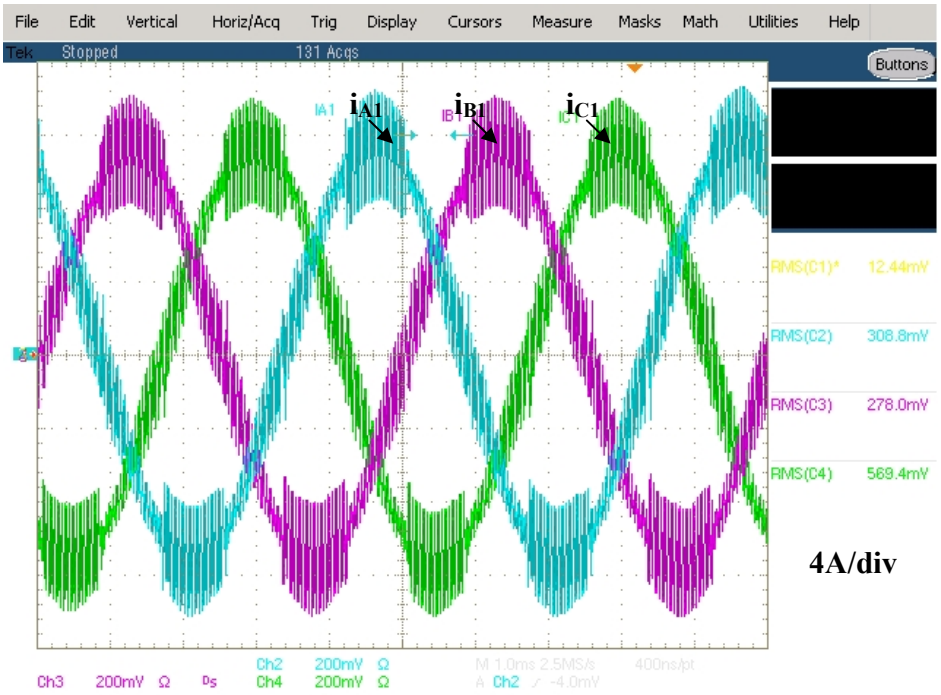

Figure 2-27. Waveforms of i_{A1}, i_{B1} and i_{C1} when $\kappa = 0.31\pi$.

Table 2-2 Summary of Experimental Results

		i_A	i_{A1}
κ=0°	THD	21.2%	21.0%
	RMS I_f	8.07A	4.04 A
κ=0.31π	THD	18.2%	17.8%
	RMS I_f	8.02 A	4.04 A
κ=π	THD	6.7%	7.3%
	RMS I_f	7.99 A	4.03 A

From Table 2-1, it can be seen that the rms fundamental currents for i_A and i_{A1} are controlled very close to the desired values of 8 A and 4 A in all cases, with or without interleaving. Given that i_{A1} is half of i_A, there is no unbalance between i_{A1} and i_{A2}. Interleaving can help to reduce the output harmonic currents significantly. Especially, when κ is π, the THD and the peak ripple current can both be reduced by about 70%, which can also be observed in Figure 2-24 and Figure 2-25. Since the circulating current is limited by inter-phase inductor, the THD of currents in each VSC (i_{A1}) and the total currents (i_A) are almost the same. However, inter-phase inductor cannot totally eliminate

the circulating current, so there are still circulating currents in each VSC as analyzed. As a result, the THD of current in each VSC (i_{A1}) is a little higher than the THD of output current (i_A), especially when π is used as interleaving angle, introducing more circulating currents than other cases.

The spectrum of harmonic currents in i_A with different interleaving angles are shown from Figure 2-28 to Figure 2-30.

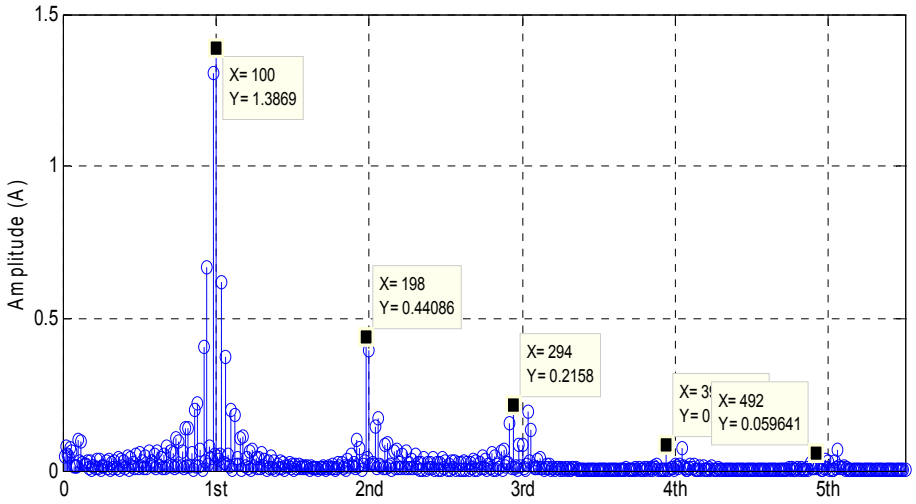

Figure 2-28. Spectrum of i_A (κ=0°).

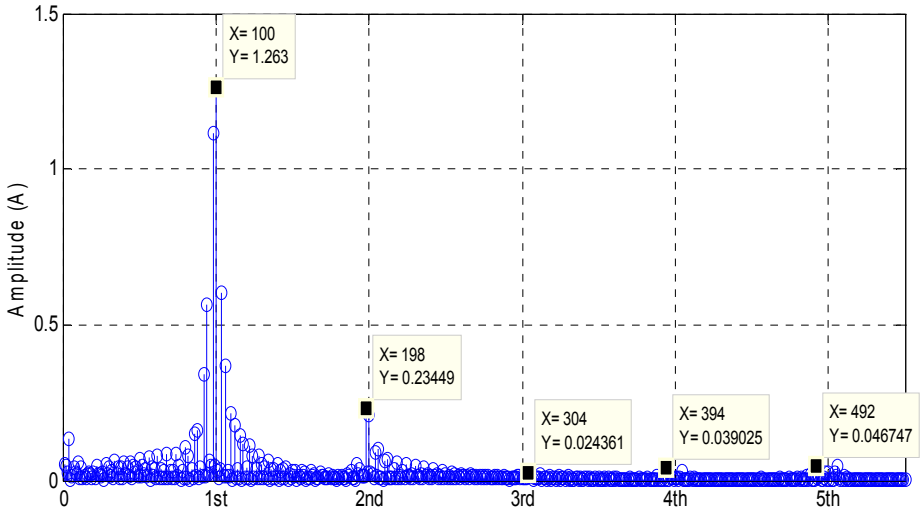

Figure 2-29. Spectrum of i_A (κ= 0.31π).

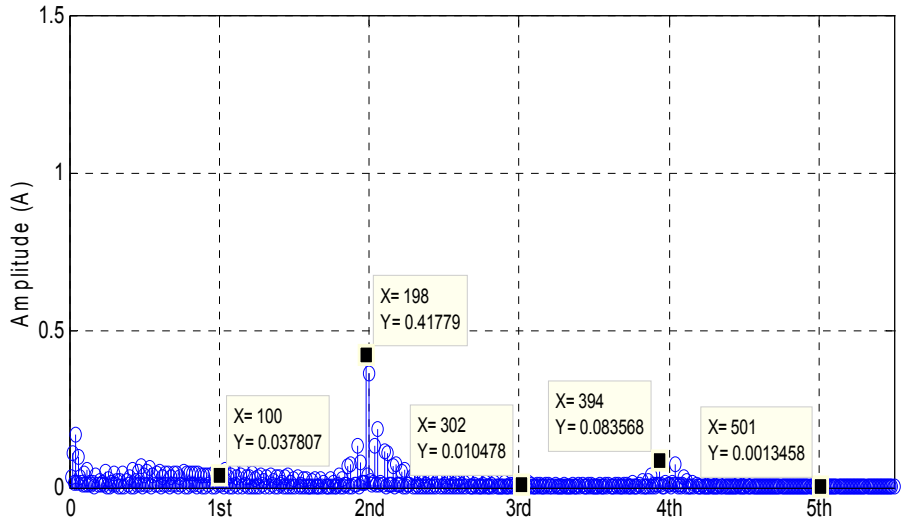

Figure 2-30. Spectrum of i_A (κ=π).

The amplitude reduction of up to 5th order switching frequency harmonic currents with different interleaving angles are summarized and compared with theoretical analysis results in Table 2-3.

Table 2-3 Summary of Experimental Results in Frequency Domain

	$\kappa = 0.31\pi$		$\kappa = \pi$	
	Theoretical Reduction	Experimental Reduction	Theoretical Reduction	Experimental Reduction
1st order	11%	9%	0%	3%
2nd order	43%	47%	100%	95%
3rd order	88%	89%	0%	5%
4th order	64%	55%	100%	98%
5th order	25%	22%	0%	2%

From Table 2-3, the experimental reduction is very close to the theoretical reduction. Since such reduction is only related to the order of harmonics and has no relationship with the actual switching frequencies. The impact of optimized interleaving angle on the attenuation of EMI filter is verified.

As predicted, interleaving can help reduce the ripple current in i_A much without increasing the ripple current flowing through converters.

2.3.5 Discussion

In the analysis above, a basic assumption is the carrier ratio (the ratio between the switching frequency and fundamental frequency) is sufficiently high, so that the difference between regular sampled PWM and naturally sampled PWM can be neglected. This is because the claim that interleaving only phase-shifts the harmonic components keeping the amplitudes not changed is only correct for naturally sampled PWM. This assumption is correct for many high power density applications that are the focus of the paper. However, there are some applications, esp. very high power applications, where the carrier ratio is very low (e.g., <10). In those cases such difference cannot be neglected and the analysis and conclusions here may not be used directly. This issue is partially studied in Chapter 5 and will be further studied in the future.

Another issue is the case with multi-paralleled VSCs (N>2). In the analysis above, we focused on the system involving only two two-level VSCs. Since the analysis is carried out in frequency domain, as long as if the current spectrum can be calculated, either by the double integral Fourier analysis or other methods, the impact of interleaving can be analyzed in the same way not related to the number and topology of the VSCs. For examples, based on (2-4) it is easy to conclude that for the N paralleled VSCs system, interleaving angle π/N can eliminate all of the m^{th} order harmonic components when m is not multiple of N. However, multi-paralleled VSCs system will make some issues more difficult such as the design of inter-phase inductor and circulating current control. These issues together with the optimization of interleaving angle will also be studied in the future.

2.4 Impact of Interleaving on Dc Side Ripple Currents

This chapter presents a complete analysis studying the impact of interleaving on the ripple current in the dc side passive components of paralleled three-phase voltage-source converters (VSCs). The analysis considers the effects of different PWM scheme, the modulation index, the interleaving angle, and the power factor or displacement angle. In the analysis, the rms value of the total ripple current in the dc side is used as figure of merit and calculated in the frequency domain. The results obtained show that all of the factors considered can strongly affect the rms value one way or another. Based on the analysis, the interleaving angle optimization method is shown to minimize the rms in different cases. The effect of circulating currents on the ripple currents in the dc side passive components is also taken into consideration to perform a more accurate analysis. All the analysis is based on an example system containing two VSCs, but the proposed analysis method in the frequency domain can be easily expandable for multiple paralleled VSCs. Experimental results are used to verify the analysis conducted.

2.4.1 Principle of Dc Side Ripple Currents Reduction

As mentioned above, the impact and benefit of interleaving are generally realized through selected harmonic current cancellation or reduction. Consequently, the analysis in this section will also be mainly performed in frequency domain using the double integral Fourier analysis. For clarity and simplicity, the analysis and discussion in this section will be also first carried out for the example system shown in Figure 2-2. The system consists of two paralleled VSCs fed from a common ac-bus and connected to a common dc bus, and the power flows from the ac source to the load represented by a dc link resistor. The naming conventions for various currents and passive components are

marked in the figure. There is no electrical isolation in the system such as transformer or isolated dc buses.

From [81], the switched phase-leg output voltage between ac terminal (e.g. point A_1) and dc link mid-point (N), v_{A1N}, can be decomposed into different harmonics. The frequencies of harmonic voltage components can be expressed as ($m\omega_c + n\omega_0$), where ω_c is the angular frequency of the carrier wave, ω_0 is the fundamental line frequency, and m and n are the carrier and baseband integer index respectively. Based on the double integral Fourier analysis approach, the harmonic component for voltage v_{A1N} corresponding to frequency ($m\omega_c + n\omega_0$) can be expressed as in (2-11):

$$v_{A1N}(m,n) = C_{mn} e^{m\theta_{c1} + n\theta_{01} + \theta_{mn}} \tag{2-11}$$

where C_{mn} is the harmonic amplitude, θ_{c1} and θ_{01} are the initial angles of the carrier and reference waves for VSC1, and θ_{mn} is a constant value depending on PWM scheme and operation condition.

For each phase leg, the switching function is defined as:

$$S_i = \begin{cases} 1, & (if\ top\ switch\ is\ turned\ on) \\ 0. & (if\ bottom\ switch\ is\ turned\ on) \end{cases} \tag{2-12}$$

Then from the spectrum of v_{A1N}, the spectrum of switching function of phase A in VSC1 can be expressed as:

$$S_{A1}(m,n) = v_{A1N}(m,n)/V_{dc} = C_{mn} e^{m\theta_{c1} + n\theta_{01} + \theta_{mn}} / V_{dc} \tag{2-13}$$

The spectrum of the switching functions of other phases can be calculated in a similar way as.

$$S_{B1}(m,n) = S_{A1}(m,n) e^{-\frac{2}{3}\pi m} \tag{2-14}$$

$$S_{C1}(m,n) = S_{A1}(m,n)e^{\frac{2}{3}\pi m} \tag{2-15}$$

Now, in time domain, the current on dc side for VSC1 can be expresses as:

$$i_{dc1} = i_{A1}S_{A1} + i_{B1}S_{B1} + i_{C1}S_{C1} \tag{2-16}$$

Correspondingly, the spectrum of i_{dc1} can be calculated as:

$$i_{dc1}(m,n) = F(i_{A1}) \otimes S_{A1}(m,n) + F(i_{B1}) \otimes S_{B1}(m,n) + F(i_{C1}) \otimes S_{C1}(m,n) \tag{2-17}$$

where F ( ) is Fourier transfer function and $\otimes$ is convolution operator.

The rms value of i_{dc1} can be calculated as:

$$RMS_{i_{dc1}} = \sqrt{\sum_{m=1}^{\infty}\sum_{n=-\infty}^{\infty} i_{idc1}^2(m,n)} \tag{2-18}$$

For VSC2, based on the similar analysis for VSC1,

$$v_{A2N}(m,n) = C_{mn}e^{m\theta_{c2}+n\theta_{02}+\theta_{mn}} \tag{2-19}$$

$$S_{A2}(m,n) = v_{A2N}(m,n)/V_{dc} = C_{mn}e^{m\theta_{c2}+n\theta_{02}+\theta_{mn}}/V_{dc} \tag{2-20}$$

$$S_{B2}(m,n) = S_{A2}(m,n)e^{-\frac{2}{3}\pi m} \tag{2-21}$$

$$S_{C2}(m,n) = S_{A2}(m,n)e^{\frac{2}{3}\pi m} \tag{2-22}$$

where θ_{c2} and θ_{02} are the initial angles of the carrier and reference waves for VSC2.

Since interleaving can only change the relative angle of carrier waveforms,

$$\begin{aligned} \theta_{c2} &= \theta_{c1} + \kappa \\ \theta_{02} &= \theta_{01} \end{aligned} \tag{2-23}$$

where κ is interleaving angle which is defined in Figure 2-1.

From (2-23) - (2-25) and (2-20) - (2-23),

$$
\begin{aligned}
S_{A2}(m,n) &= S_{A1}(m,n)e^{m\kappa} \\
S_{B2}(m,n) &= S_{B1}(m,n)e^{m\kappa} \\
S_{C2}(m,n) &= S_{C1}(m,n)e^{m\kappa}
\end{aligned} \tag{2-24}
$$

Considering the even distribution of output currents in VSC1 and VSC2,

$$F(i_{dc2})(m,n) = F(i_{dc1})(m,n)e^{m\kappa}$$

and

$$F(i_{dc})(m,n) = F(i_{dc1})(m,n) + F(i_{dc2})(m,n) = F(i_{dc1})(m,n)(1+e^{m\kappa}) \tag{2-25}$$

It follows that the amplitude of the harmonic current in i_{dc} is

$$\left|F(i_{dc})(m,n)\right| = 2\left|F(i_{dc1})\right|(m,n)\cos(m\kappa/2) \tag{2-26}$$

When κ is 0, which means without interleaving,

$$\left|F(i_{dc})(m,n)\right| = 2\left|F(i_{dc1})\right|(m,n) \tag{2-27}$$

By comparing (2-26) and (2-27), it is obvious that interleaving can reduce the amplitude of harmonic currents in i_{dc}.

By comparing (2-26) and (2-27), it is obvious that interleaving can reduce the amplitude of harmonic currents in i_{dc}. Also from (2-26), it can be seen that if κ is set to be π/m, i.e., interleaving the carrier wave of VSC2 by $1/m^{th}$ of the switching cycle keeping the carrier wave of VSC1 unchanged, $F(i_{dc})(m,n)$ will be zero. In general, when certain κ is used, the relationship between the two vectors representing the two harmonic components at $(m\omega_c + n\omega_0)$ in i_{dc1} and i_{dc2} can be shown illustrated as in Figure 2-31 and Figure 2-32. Especially, for the sample system shown in Figure 2-2, the phase-shifting π can eliminate all odd order switching frequency harmonics and not affect the even order switching frequency harmonics. And the phase-shifting by π/2 can eliminate harmonics when m is (4k+2), such as 2, 6 and 10, and reduce the harmonics by 30 % (i.e. $1/\sqrt{2}$ of

the original) when *m* is odd, and not affect other even order harmonics. The conclusion is similar as on ac side.

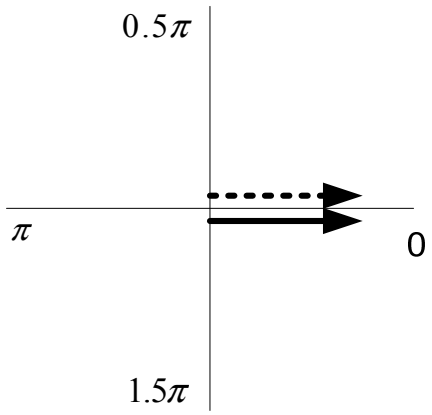

Figure 2-31. Relative phase angle of i_{dc1} and i_{dc2} without interleaving.

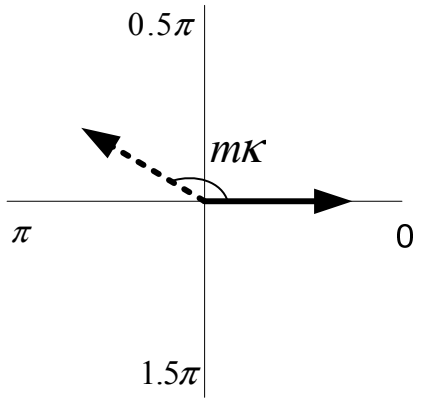

Figure 2-32. Relative phase angle of i_{dc1} and i_{dc2} with interleaving.

2.4.2 Interleaving Angle Selection for Ripple Current Reduction

The objective of the selection of the interleaving angle is to minimize the rms value of the total ripple current in i_{dc}, which is used as the figure of merit in this section. From Section 2.2, it follows that different interleaving angles can eliminate different harmonic currents. It is straightforward then that the interleaving angle should be selected to eliminate the dominant harmonic component. A tradeoff appears then in the case where several harmonic components are dominant. As a result, the interleaving angle should be

selected based on the spectrum of the harmonic currents in i_{dc} under different operating conditions, such as PWM schemes, power factor, modulation index, and the number of paralleled VSCS in the system.

To explain the effects of different variables in the selection of the interleaving angle, two examples are used. In the first one, an analytical analysis is used for simple sinusoidal PWM (SPWM), and numerical analysis is used for the more complex SVM scheme. In these two examples, the system shown in Figure 2-2 is used, which means that only two paralleled VSCs are considered. The method used can be extended and used for N paralleled VSCs system.

A. Analytical analysis for SPWM

To clearly explain the effect of different variables on the rms value of the total dc side ripple analytically, SPWM is assumed to be the PWM scheme first. For SPWM, the harmonic components of the switching functions can be calculated as follows **Error! Reference source not found.**

$$F(S_{A1})(m,n)=\frac{4}{\pi m}J_n\left(m\frac{\pi\sqrt{3}M}{4}\right)\sin\left[(m+n)\frac{\pi}{2}\right]e^{m\theta_{c1}+n\theta_0 1+\theta_{mn}} \tag{2-28}$$

where M is the modulation index($0<M<1$), m is the carrier index variable, n is the baseband index variable and $J_n(x)$ is a Bessel function.

To simplify the analysis, only the fundamental component in the ac side currents is considered first. In fact, even though the ac side currents contain fundamental and harmonic components, the contribution of the ac side harmonic currents on the dc side ripple current is negligible compared with that of the ac side fundamental current—if the THD of the ac side current is within reasonable levels. Experimental results will prove

this assumption. Some special ac harmonic currents, which are circulating currents related to interleaving, will be analyzed later in section 2.4.4 in order to focus the analysis hereinafter. For some special applications where the harmonic currents are high in magnitude compared to the fundamental current, the method to calculate the rms value of i_{dc1} is still correct, but the spectrum of the ac side currents cannot be simplified in that case and the analytical analysis will be more complex.

With that said, the spectrum of the fundamental component of the ac side currents can be expressed as:

$$\begin{aligned} F(i_{A1}) &= \left[\frac{i_{A1}}{2} e^{-j\theta} \quad 0 \quad \frac{i_{A1}}{2} e^{j\theta} \right], \\ F(i_{B1}) &= \left[\frac{i_{B1}}{2} e^{-j\left(\theta-\frac{2}{3}\pi\right)} \quad 0 \quad \frac{i_{B1}}{2} e^{j\left(\theta-\frac{2}{3}\pi\right)} \right] \\ F(i_{C1}) &= \left[\frac{i_{C1}}{2} e^{-j\left(\theta+\frac{2}{3}\pi\right)} \quad 0 \quad \frac{i_{C1}}{2} e^{j\left(\theta+\frac{2}{3}\pi\right)} \right] \end{aligned} \tag{2-29}$$

where θ is the displacement angle.

Together with (2-28), the spectrum of i_{dc1} can be calculated from (2-17), if the ac side currents are balanced:

$$\begin{aligned} F(i_{dc1})(m,n) = \frac{I_{peak}}{\pi m} e^{m\theta_{c1}+n\theta_{01}+\theta_{mn}} \left[1+2\cos\left(n\frac{2}{3}\pi \right) \right] \Bigg\{ & J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4} \right) \sin\left[(m+n-1)\frac{\pi}{2} \right] e^{-j\theta} \\ & + J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4} \right) \sin\left[(m+n+1)\frac{\pi}{2} \right] e^{j\theta} \Bigg\} \end{aligned} \tag{2-30}$$

where I_{peak} is the peak value of the fundamental component in ac side currents.

Since $\left|F(i_{dc})(m,n)\right| = 2\left|F(i_{dc1})\right|(m,n)\cos(m\kappa/2)$, so interleaving angle should be selected to reduce the amplitude of the dominant harmonic components.

From (2-30), only when n is triplen, the amplitude of such harmonic component is not zero. Further, the amplitude of the harmonic component of i_{dc1} at $m\omega_c+n\omega_0$ is determined by a pair of components $J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4}\right)$ and $J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4}\right)$, which also determine the amplitude of the harmonic components at $m\omega_c\pm n\omega_0$ as shown in (18). From [69], the highest harmonic components are located around the switching frequency (m = 1, n = ± 2) and twice its value (m = 2, n = ± 1), so the possible dominant harmonic components may be located at a given frequency represented as a pair of (m, n), e.g., as (1,-3), (1,-1). (1,1), (1,3), (2,-2), (2,0) and (2,2), which are related to the dominant components of the ac harmonic components. Since only when n is multiple of three the amplitude is not zero, (1,-3), (1, 3) and (2,0) may be the dominant components.

For unity power factor operation, θ is 0°, that is,

$$F(i_{dc1})(m,n)=\frac{3I_{peak}}{\pi m}e^{m\theta_{c1}+n\theta_{01}+\theta_{mn}}\left\{J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\sin\left[(m+n-1)\frac{\pi}{2}\right]+J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\sin\left[(m+n+1)\frac{\pi}{2}\right]\right\} \tag{2-31}$$

The amplitude of the harmonic components is then,

$$\left|F(i_{dc1})(m,n)\right|=\frac{3I_{peak}}{\pi m}\left|J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4}\right)-J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\right| \tag{2-32}$$

Since the Bessel function is an odd function,

$$\left|F(i_{dc1})(2,0)\right|=\frac{3I_{peak}}{\pi}\left|J_1\left(\frac{\pi\sqrt{3}M}{2}\right)\right| \tag{2-33}$$

$$\left|F(i_{dc1})(1,3)\right| = \left|F(i_{dc1})(1,-3)\right| = \frac{3I_{peak}}{\pi}\left|J_2\left(\frac{\pi\sqrt{3}M}{4}\right) - J_4\left(\frac{\pi\sqrt{3}M}{4}\right)\right| \tag{2-34}$$

and since J_2 () is very close to J_4(), the amplitude of $F(i_{dc1})(1,3)$ and $F(i_{dc1})(1,-3)$ are very small. So $F(i_{dc1})(2,0)$ is the dominant component and 90° interleaving angle should be used, which can eliminate the second order switching harmonic components as shown in Section 2.4.1.

For zero power factor operation, θ is 90°, and

$$F(i_{dc1})(m,n) = \frac{3I_{peak}}{\pi m} e^{m\theta_{c1}+n\theta_{01}+\theta_{mn}}\left\{J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\sin\left[(m+n-1)\frac{\pi}{2}\right] - J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\sin\left[(m+n+1)\frac{\pi}{2}\right]\right\} \tag{2-35}$$

The amplitude of the harmonic components are then,

$$\left|F(i_{dc1})(m,n)\right| = \frac{3I_{peak}}{\pi m}\left|J_{n-1}\left(m\frac{\pi\sqrt{3}M}{4}\right) + J_{n+1}\left(m\frac{\pi\sqrt{3}M}{4}\right)\right| \tag{2-36}$$

And since Bessel function is an odd function,

$$\left|F(i_{dc1})(2,0)\right| = 0 \tag{2-37}$$

$$\left|F(i_{dc1})(1,3)\right| = \left|F(i_{dc1})(1,-3)\right| = \frac{3I_{peak}}{\pi}\left|J_2\left(\frac{\pi\sqrt{3}M}{4}\right) + J_4\left(\frac{\pi\sqrt{3}M}{4}\right)\right| \tag{2-38}$$

As a result, $F(i_{dc1})(2,0)$ will be zero and $F(i_{dc1})(1,3)$ and $F(i_{dc2})(1,-3)$ become the dominant components, and 180° should be used as interleaving angle in order to eliminate the second order switching harmonic components.

When system power factor is increased from 0 to 1, the interleaving angle will also vary from 180° to 90° accordingly. In other words, a tradeoff in the reduction of the

harmonic components around the switching frequency and twice the switching frequency is expected. Also, from (2-34), M is always a key variable to determine the amplitude of the harmonic components, so M also affects the impact of interleaving.

B. numerical analysis for SVM

For more complex PWM schemes it is not easy to carry out the analytical analysis; but an alternative numerical approach can be used to conduct it. Specifically, C_{mn} and θ_{mn} can be obtained as in (2-39) from the double integral Fourier analysis. Note that C_{mn} is only a function of the PWM scheme and the modulation index M. An example for central aligned SVM is given in Table 2-1. Assuming the same carrier and symmetrical references (120˚ apart) for the three phases for the converter VSC1, its phase B and C voltage harmonic v_{B1N}(m,n), v_{C1N}(m,n) will be similar to (1), with identical C_{mn} and θ_{mn} but θ_0 will be displaced by 120˚.

$$C_{mn}e^{j\theta_{mn}} = \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{x_r}^{x_f} e^{j(mx+ny)}dxdy \tag{2-39}$$

The integral limits for the example SVM system are also given in Table 2-1.

Based on the same analysis method presented in Section 2.4.2, the spectrum of ripple currents on dc side under different conditions are shown from Figure 2-33 to Figure 2-36. In these figures, the amplitudes of the harmonic components are normalized based on the peak value of the ac side fundamental current. From Figure 2-33 and Figure 2-34, when the power factor is high, the dominant harmonic component is located at the 2nd and 6th order harmonic, which can be eliminated by phase shifting by 90˚. From Figure 2-35 and Figure 2-36, when the power factor is low, the dominant component is locate at the 1st

and 3rd order harmonics, which can be eliminated by phase shifting by 180˚. The conclusion then is similar to that of the SPWM case; a tradeoff.

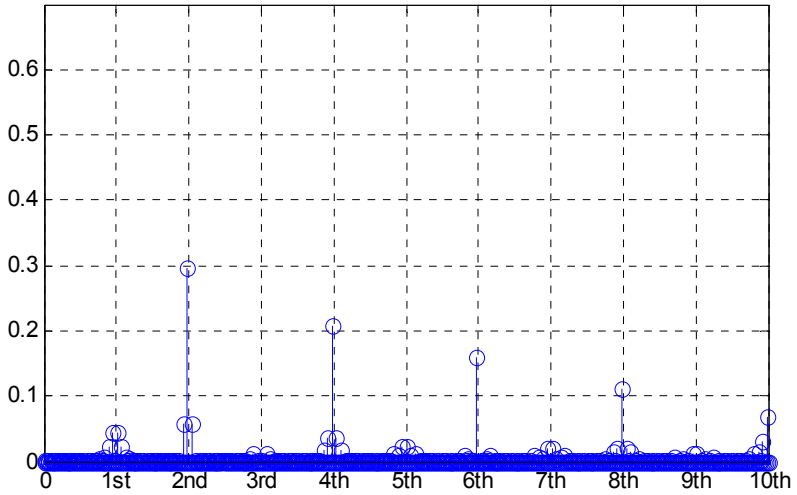

Figure 2-33. Spectrum of dc side ripple current when power factor is 1. (M=0.9).

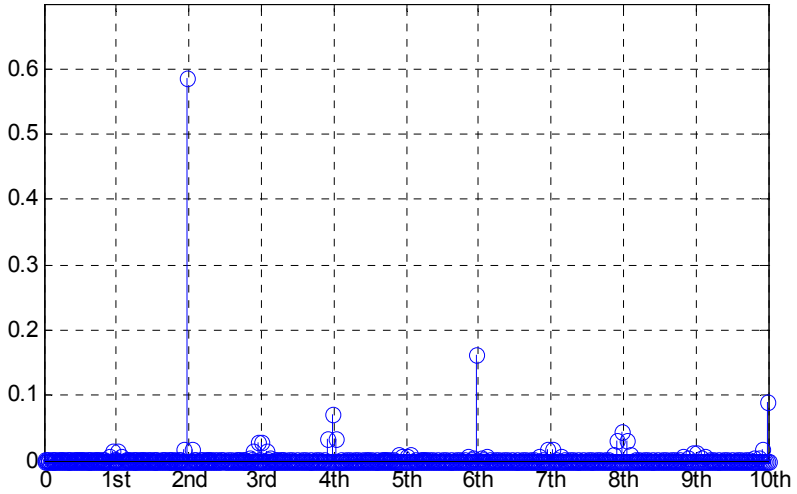

Figure 2-34. Spectrum of dc side ripple current when power factor is 1. (M=0.5).

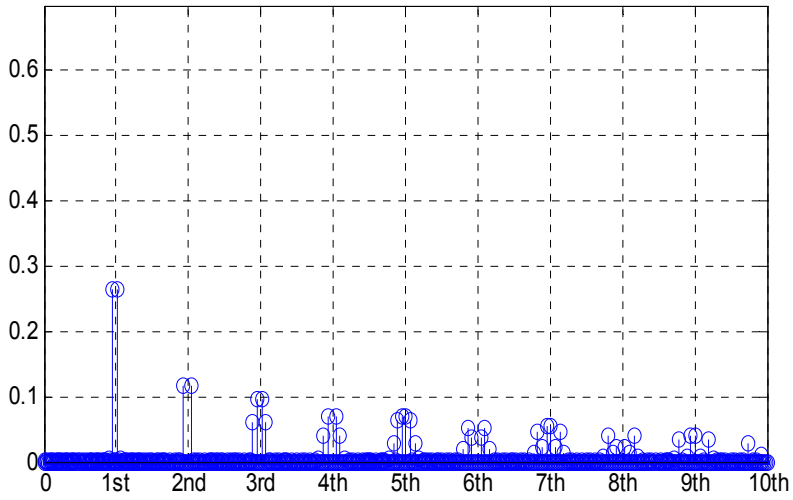

Figure 2-35. Spectrum of dc side ripple current when power factor is 0. (M=0.9).

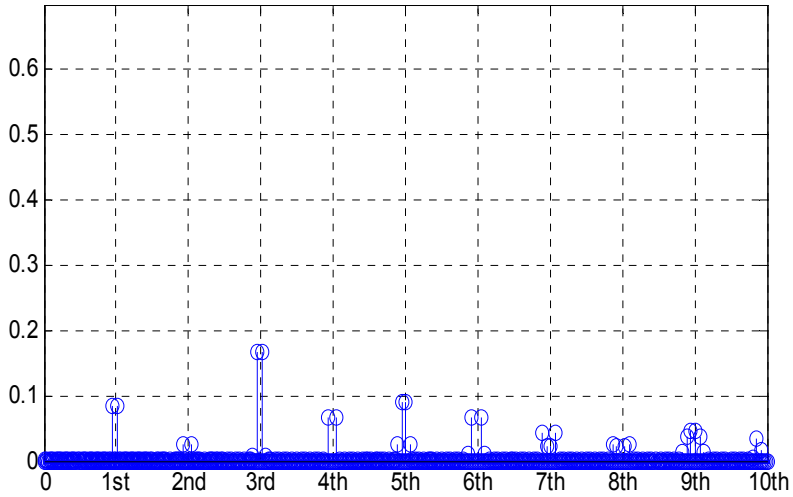

Figure 2-36. Spectrum of dc side ripple current when power factor is 0. (M=0.5).

The impact of the interleaving angle, modulation index, and displacement angle on the rms value of the total dc side ripple current are presented in Figure 2-37 and Figure 2-38. In these plots the rms value of the total dc side ripple currents is normalized based on the peak value of the ac side fundamental current. The impact of three interleaving angles (0˚, 90˚ and 180˚) is shown and compared in three different planes as illustrated.

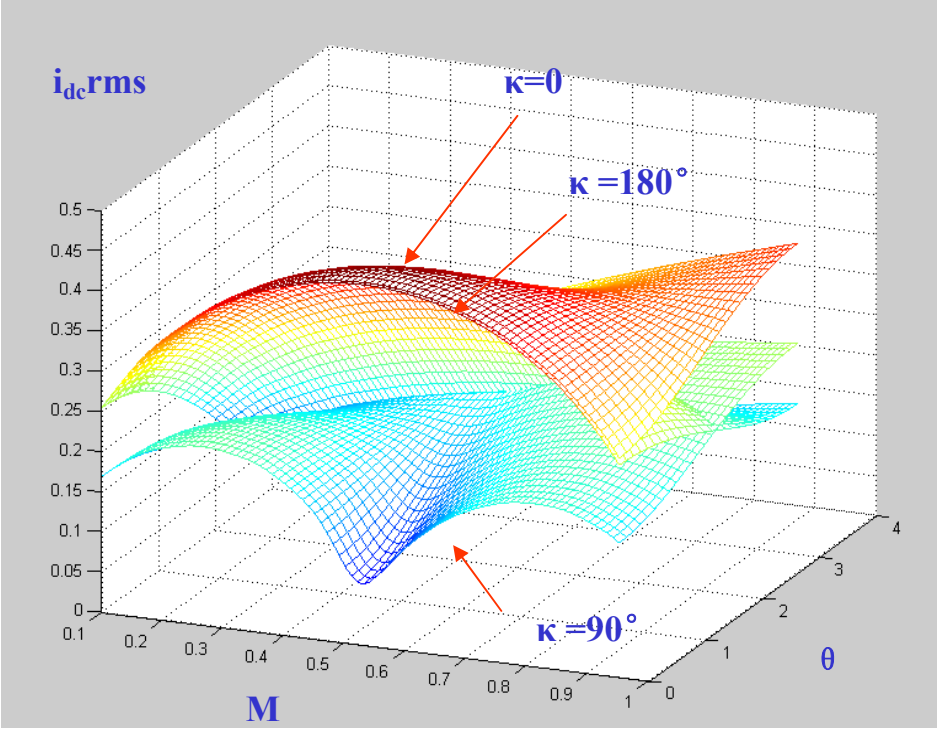

Figure 2-37. Impact of interleaving angle on dc side ripple current for SVM.

Figure 2-37 shows that when the power factor is high—θ is close to zero, 90˚ interleaving is much better than 180˚. In fact, 180˚ can barely reduce the rms value of dc side ripple currents. On the contrary, 90˚ can help especially when the modulation index is close to 0.5, which without interleaving is usually the worst case. Figure 2-38on the other hand depicts the same plot as Figure 2-37, but viewed from a different direction in order to see better the effect on cases with low power factor. As seen in this figure, when power factor is low, 180˚ phase-shifting is better than 90˚ phase-shifting, which also agrees with the analytical results.

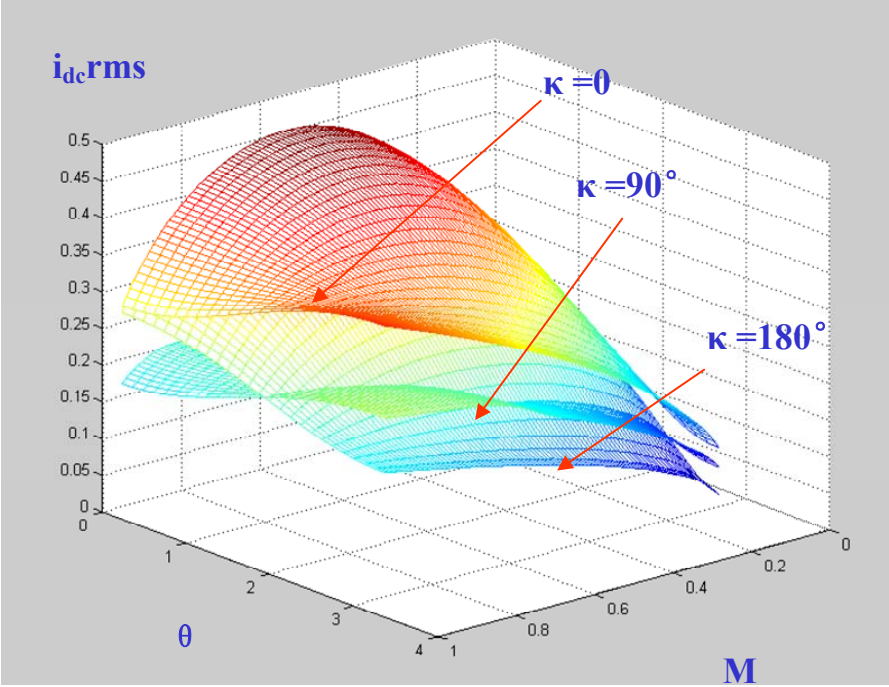

Figure 2-38. Impact of interleaving angle on dc side ripple current for SVM.

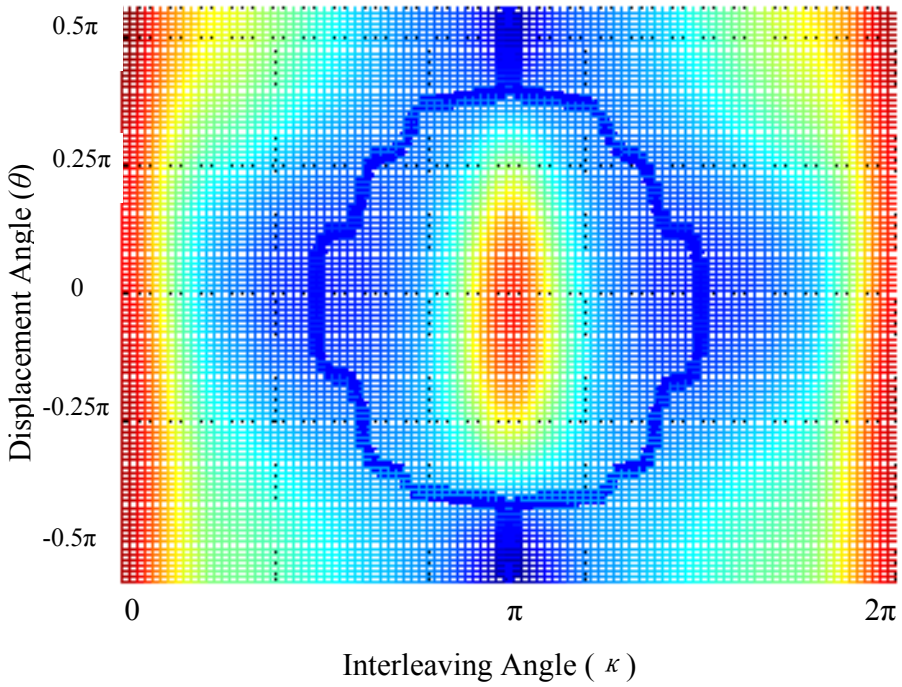

Figure 2-39. Interleaving angle for minimized dc side ripple current.

Another point of view is when the modulation index is fixed, as in rectifier operation. In this case the optimized interleaving angle to minimize the rms value of the dc side

ripple current can be determined, and it is highlighted by the thick curve in Figure 2-39. This figure shows how the optimized interleaving angle changes from 90˚ to 180˚ when the power factor decreases from 1 to 0, which is also similar for SPWM.

The impact of interleaving angle has a high dependency on the specific PWM scheme. For minimum loss or DPWM, the spectrum of i_{dc} can be calculated using (2-39). The double Fourier integral limits for DPWM are given in Table 2-4. In a similar way, for DPWM, the impact of the interleaving angle, modulation index, and the power factor angle on the rms value of the dc side ripple current can also be calculated numerically. Figure 2-40 and Figure 2-41 show the corresponding plots to Figure 2-37 and Figure 2-38, which show that 180˚ is better than 90˚ in most of the cases for DPWM, which is an opposite result when compared to SVM.

Table 2-4 Double Fourier Integral Limits for DPWM (Phase A)

y	x_r (rising edge)	x_f (falling edge)
$-\frac{\pi}{6}<y<\frac{\pi}{6}$	$-\pi$	π
$\frac{\pi}{6}<y<\frac{\pi}{2}$	$-\pi\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})$	$\pi\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6})$
$\frac{\pi}{2}<y<\frac{5\pi}{6}$	$-\pi(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$	$\pi(1+\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6}))$
$\frac{5\pi}{6}<y<\frac{7\pi}{6}$	0	0
$\frac{7\pi}{6}<y<\frac{3\pi}{2}$	$-\pi(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$	$\pi(1+\frac{\sqrt{3}}{2}M\cos(y-\frac{\pi}{6}))$
$\frac{3\pi}{2}<y<\frac{11\pi}{6}$	$-\pi\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})$	$\pi\frac{\sqrt{3}}{2}M\cos(y+\frac{\pi}{6})$

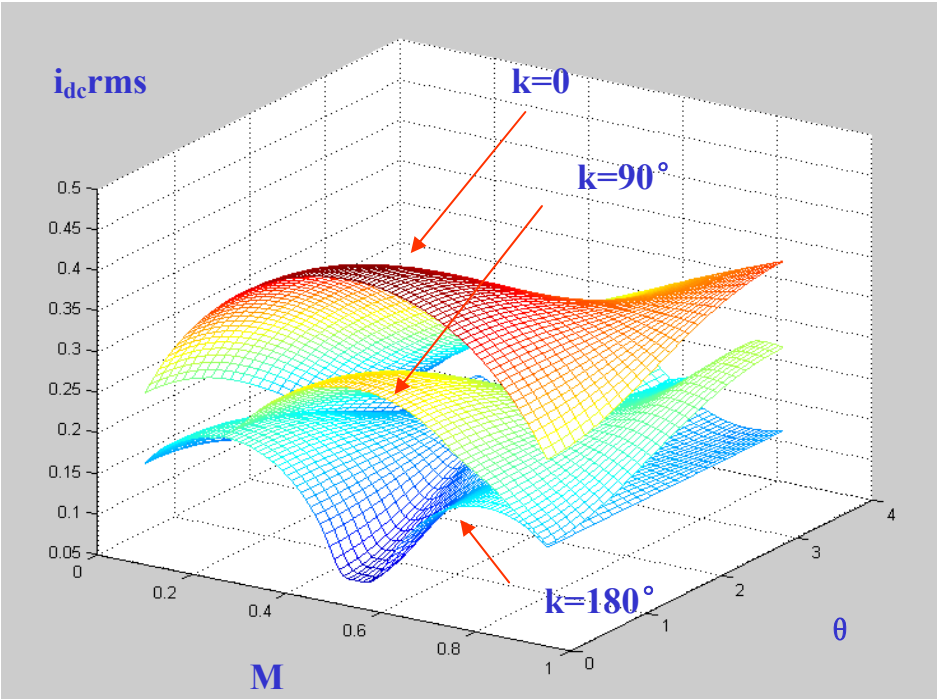

Figure 2-40. Impact of interleaving angle on dc side ripple current for DPWM.

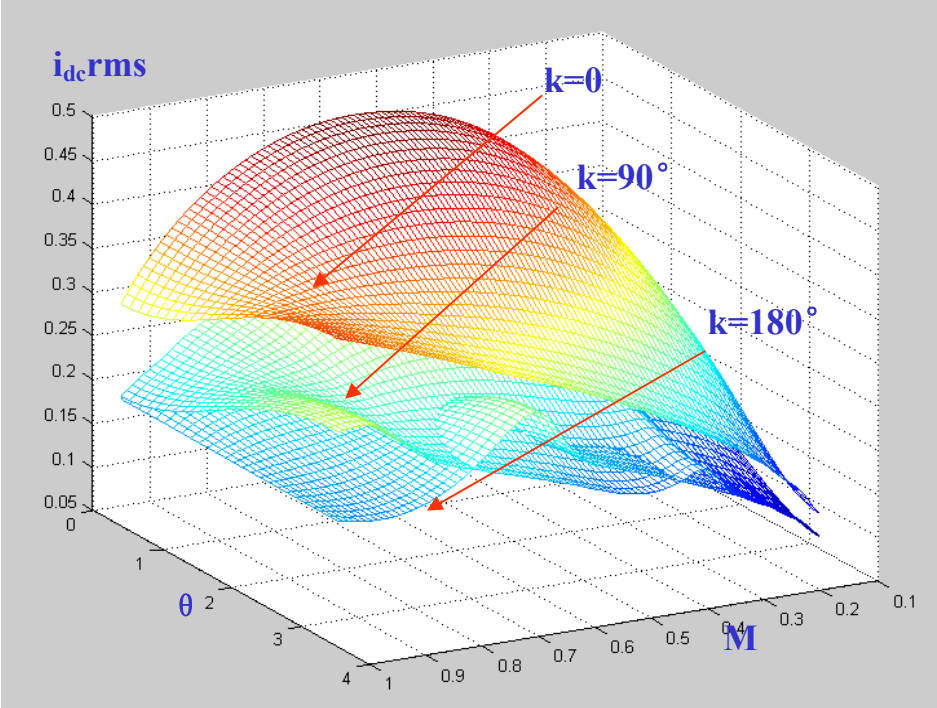

Figure 2-41. Impact of interleaving angle on dc side ripple current for DPWM.

2.4.3 Impact of Circulating Currents on Dc Side Ripple Currents

Other than the output ac side currents there are also circulating currents in the system that may also generate dc side ripple currents. Interleaving can make this problem worse if no precautions are taken since interleaving can introduce additional common-mode (CM) circulating current, which can be the dominant circulating current in the system.

In this paper, the circulating currents for VSC1 are defined as:

$$i_{cir\_A1} = 0.5(i_{A1} - i_{A2}) \tag{2-40}$$

$$i_{cir\_B1} = 0.5(i_{B1} - i_{B2}) \tag{2-41}$$

$$i_{cir\_C1} = 0.5(i_{C1} - i_{C2}) \tag{2-42}$$

And because of the character of circulating current,

$$i_{cir\_A2} = -i_{cir\_A1} \tag{2-43}$$

$$i_{cir\_B2} = -i_{cir\_B1} \tag{2-44}$$

$$i_{cir\_C2} = -i_{cir\_C1} \tag{2-45}$$

As a result, in time domain it follows that,

$$i_{dc\_cir} = i_{cir\_A1}S_{A1} + \left(-i_{cir\_A1}\right)S_{A2} + i_{cir\_B1}S_{B1} + \left(-i_{cir\_B1}\right)S_{B2} + i_{cir\_C1}S_{C1} + \left(-i_{cir\_C1}\right)S_{C2} \tag{2-46}$$

Without interleaving,

$$S_{A1} = S_{A2} \tag{2-47}$$

$$S_{B1} = S_{B2} \tag{2-48}$$

$$S_{C1} = S_{C2} \tag{2-49}$$

which replaced in (2-46) yields

$$i_{dc\_cir} = 0 \tag{2-50}$$

As a result, the system circulating current cannot generate any ripple current in the dc capacitor without interleaving. On the contrary, with interleaving, the ripple current

caused by the circulating current will be generated. Its spectrum can be calculated as shown below in the frequency domain.

$$\begin{aligned} F(i_{dc\_cir})(m,n) &= F(i_{cir\_A1}) \otimes F(S_{A1}) + F(i_{cir\_B1}) \otimes F(S_{B1}) + F(i_{cir\_C1}) \otimes F(S_{C1}) \\ &- F(i_{cir\_A2}) \otimes F(S_{A2}) - F(i_{cir\_B2}) \otimes F(S_{B2}) - F(i_{cir\_C2}) \otimes F(S_{C2}) \end{aligned} \quad (2\text{-}51)$$

From [69], the dominant component in *F(S)* is located at the switching frequency, which is a CM component, so that $S_{A1}(1,0) = S_{B1}(1,0) = S_{C1}(1,0)$. As a result, the convolution between the DM component in i_{cir_A1}, i_{cir_B1} and i_{cir_C1} and the CM harmonic components in (41) are zero. Only the CM components in i_{cir_A1}, i_{cir_B1} and i_{cir_C1} are therefore analyzed in this paper. And furthermore, only the dc component and the circulating current at the switching frequency are considered, since they are the dominant circulating currents in the system. The experimental results will verify the validity of such assumption.

The dc component in circulating current can be caused by the sampling error or other non-ideal experimental condition. For such dc component, (2-51) can be simplified to

$$F(i_{dc\_cir})(m,n) = 2\left(i_{cir\_A1} \times F(S_{A1}) + i_{cir\_B1} \times F(S_{B1}) + i_{cir\_C1} \times F(S_{C1})\right) \quad (2\text{-}52)$$

It is apparent then that the dominant harmonic current related to the dc circulating current is located at the switching frequency.

For CM circulating currents at the switching frequency, the spectrum contains two components located at $+\omega_c$ and $-\omega_c$. As a result, the convolution between such circulating current and the CM harmonic component at the switching frequency contains two components located at dc, and at twice the switching frequency.

Since it is hard to predict the amplitude of circulating current especially the dc circulating current, in the analysis in sections above, the effects of circulating is not

considered in the calculation of rms value of total dc side ripple current. Such simplification can introduce certain relative error between experimental results and analysis results. Even though the amplitude of such dc side harmonic current caused by the circulating current is much smaller than the harmonic currents at the same frequency caused by the fundamental current, the contribution of such harmonic current to the rms value of total dc side ripple currents can still be observed when the ripple currents related to the output fundamental current have been reduced significantly by interleaving. This can be seen in next section.

2.4.4 Experimental Results on Dc Side Ripple Currents

The experiment is designed to verify three key points in the analysis above. First, that the impact of the interleaving angle has a high relationship with the system power factor. Second, that the PWM scheme can also affect the selection of interleaving angle. And third, that the effect of the circulating current on dc side ripple current can be observed when interleaving is applied.

In the experiment, the rectifier configuration in Figure 2-42 was used, whose power factor can be controlled. To limit the circulating current on the ac side efficiently, an inter-phase inductor was used [34]. Also, the function of the boost inductor in Figure 2-42 was realized by the leakage inductance of the inter-phase inductors.

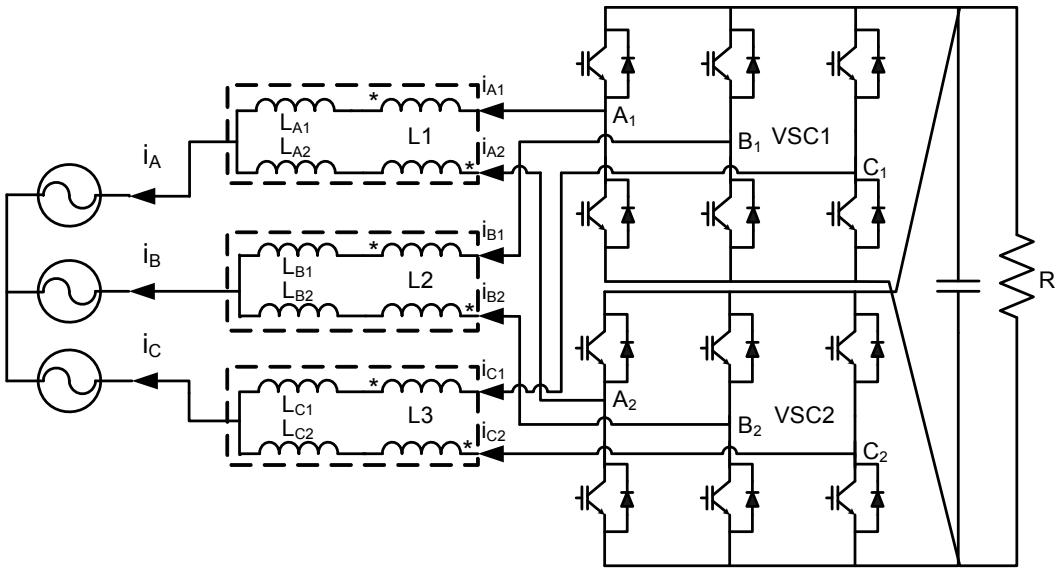

Figure 2-42. Schematic of the experimental setup.

The experimental setup was comprised of: two six-pack IGBT IPMs from Fuji (6MBP20RH060), implementing the power stage of the two VSCs; one common DSP-FPGA digital controller; three inter-phase inductors as shown in Figure 2-21; and a Helionetics three-phase AC power supply used as an ideal three-phase voltage source. As discussed above, the leakage inductance of the inter-phase inductor L_{leak} was used as ac boost inductor (320 μH), and the main inductance L_{ip} was used to limit the circulating current (3mH). The dc voltage was 250 V, and the fundamental and switching frequency were chosen as 60 Hz and 10 kHz respectively. The rms value of the fundamental current on the ac side was about 8 A. To verify the case with 0.9 modulation index, an ac line voltage of 90 V was used. A 50 V ac line voltage was used to verify the case with 0.5 modulation index. Two PWM schemes were used in the experiment, central aligned SVM and DPWM. When DPWM is used, the circulating current control methods proposed in [57] and [84] were used. For the unity power factor case, a 30 Ω and a 52 Ω loads were

used for the 0.9 and 0.5 modulation index cases separately in order to keep the ac side fundamental current constant.

Figure 2-43 and Figure 2-44 show the experimental results when central aligned SVM is used. In this case M is 0.5, the displacement angle is 0˚, and κ is 0˚ and 90˚. From these two figures, it is clear that 90˚ interleaving can reduce the dc side ripple currents significantly barely affecting i_{dc1} and i_{dc2}. The experimental data are summarized in Table 2-5.

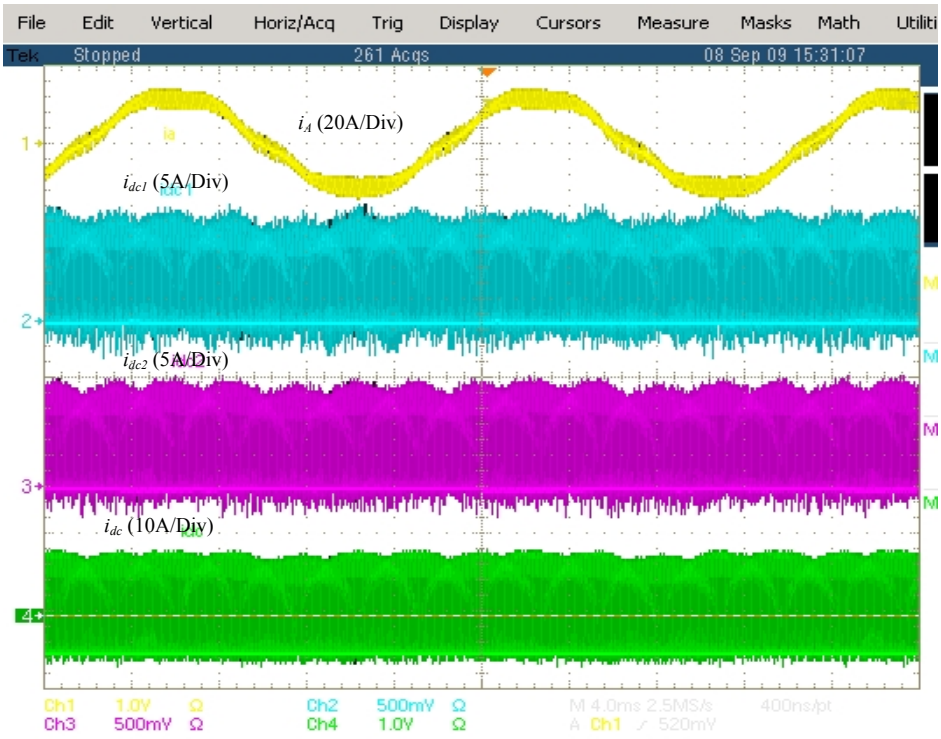

Figure 2-43. Dc side ripple currents when M=0.5, θ=0 and κ=0˚.

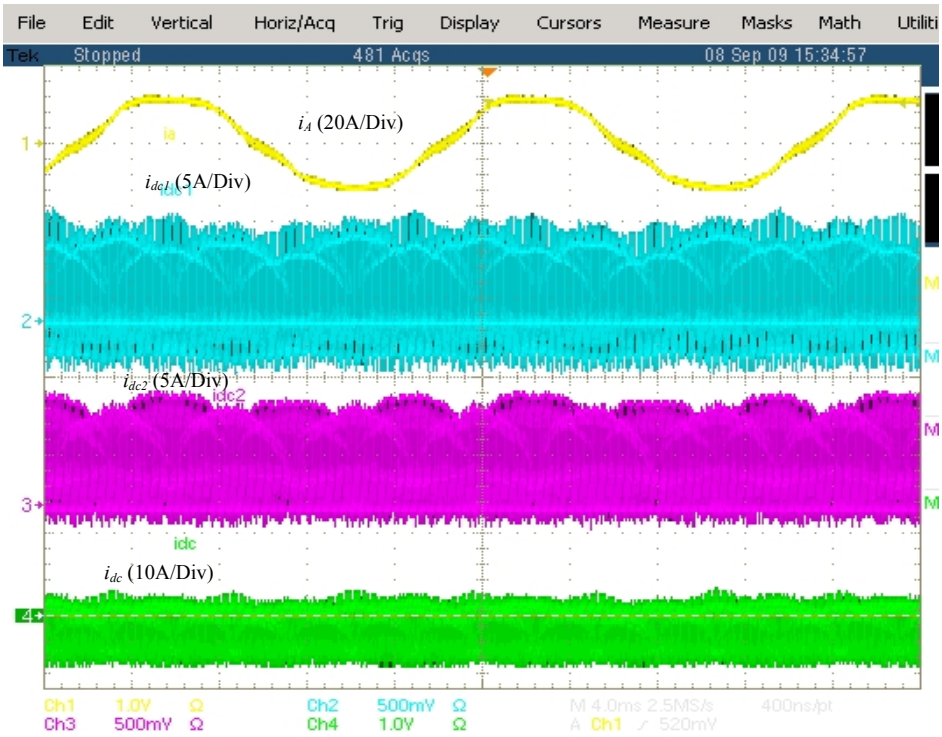

Figure 2-44. Dc side ripple currents when M=0.5, θ=0 and κ=0˚.

Table 2-5 Experiment results on dc side for SVM when M=0.5, θ=0˚

Interleaving Angle	EXPERIMENTAL RESULTS
κ= 0	5.33A (100%)
κ= 90˚	1.89A (35%)
κ= 180˚	5.42A (102%)

Figure 2-45 and Figure 2-46 show the experimental results when central aligned SVM is used, but M is 0.9, the displacement angle is 90˚, and κ is 0˚ and 180˚. These results summarized in Table 2-6 also show that 90˚ interleaving can reduce the dc side ripple current significantly without affecting i_{dc1} and i_{dc2}—reducing it to 72 %, but the interleaving angle of 180˚ is better as it can reduce the rms ripple to 45%, which matches the theoretical analysis.

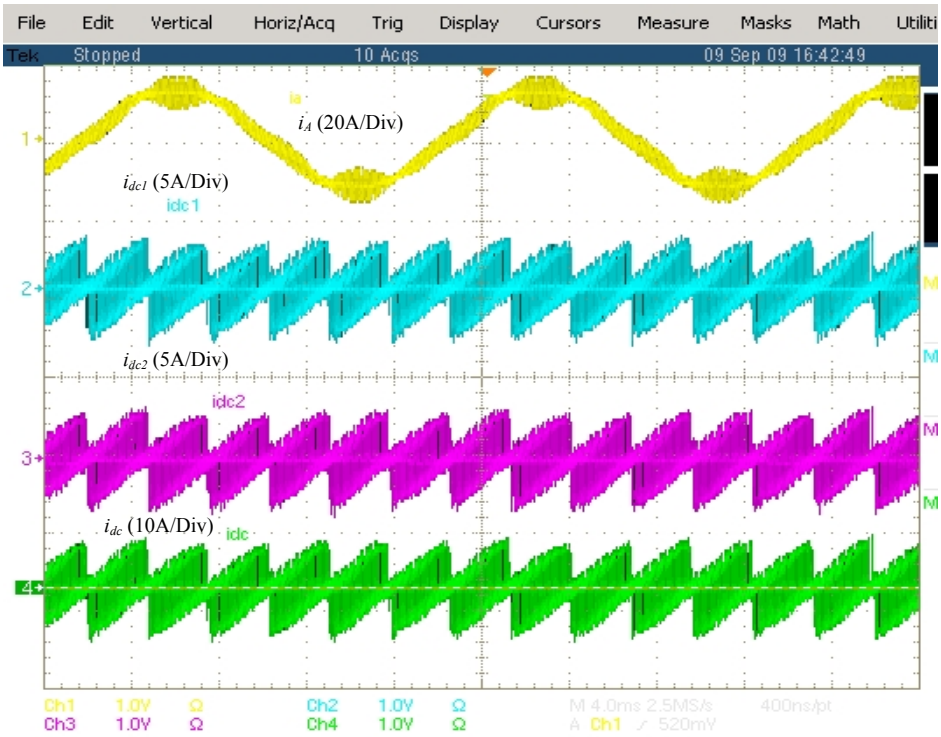

Figure 2-45. Dc side ripple currents when M=0.9, θ=90˚ and κ=0˚.

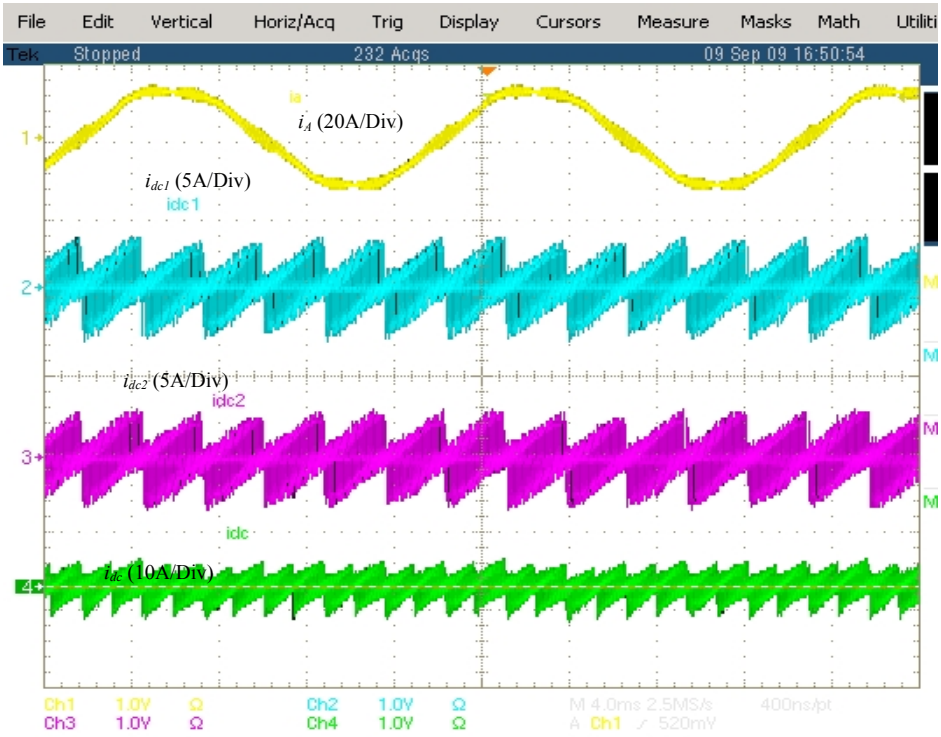

Figure 2-46. Dc side ripple currents when M=0.9, θ=90 and κ=180˚.

Table 2-6 Experiment results on dc side for SVM when M=0.9, θ=90˚

Interleaving Angle	EXPERIMENTAL RESULTS
κ= 0	4.9A (100%)
κ= 90˚	3.52A (72%)
κ= 180˚	2.21A (45%)

Finally, Figure 2-47 and Figure 2-48 show the experimental results using DPWM, with M equal to 0.9, a power factor angle of 0˚, and κ is 0˚ and 180˚. From the figures, it can be clearly observed how an interleaving angle of 180˚ can reduce the dc side ripple current significantly without affecting idc1 and idc2. In fact, as detailed in Table 2-7, κ = 180º provides a better dc ripple cancellation for both unity and zero power factor operation, reducing the ripple content by 54 % and 47 % respectively. This is in accordance with the analysis presented in Figure 2-40 and Figure 2-41.

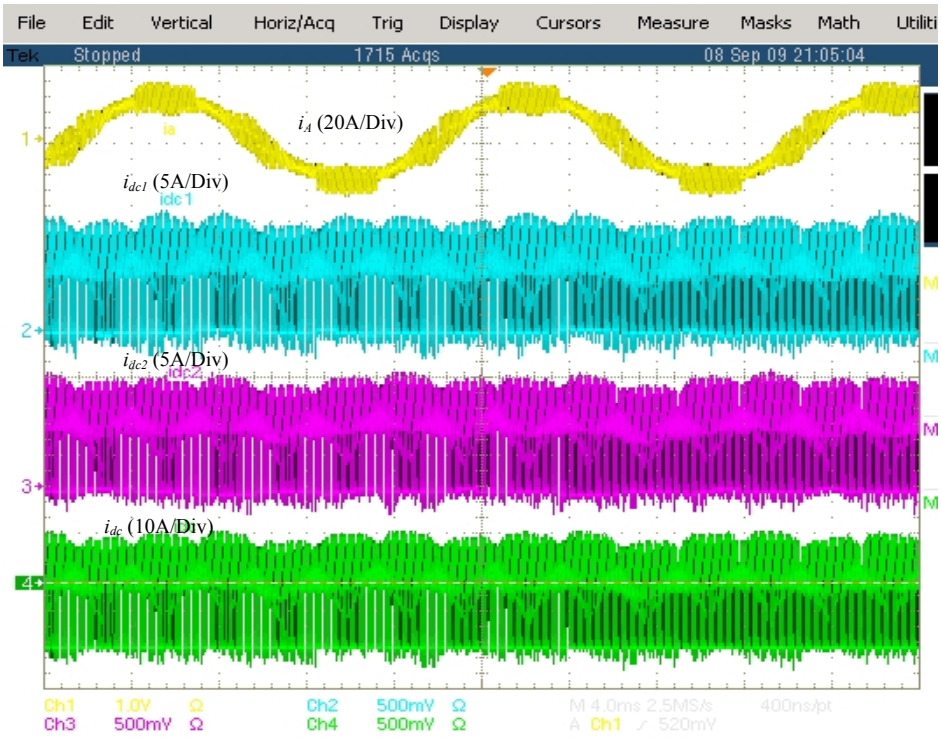

Figure 2-47. Dc side ripple currents when M=0.9, θ=90˚ and κ=0˚.

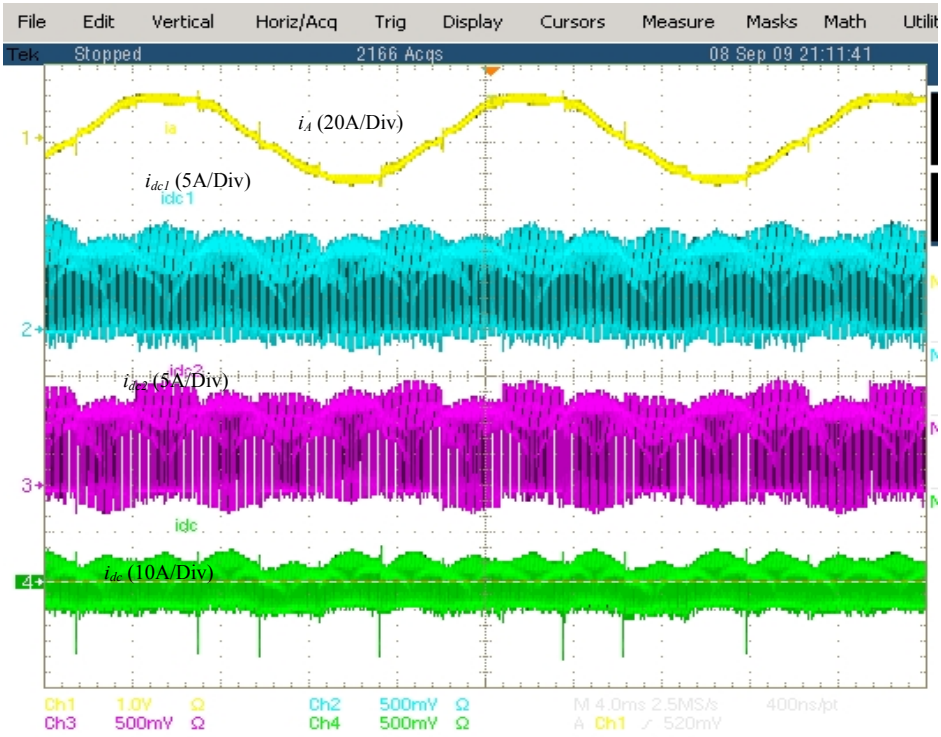

Figure 2-48. Dc side ripple currents when M=0.9, θ=90˚ and κ=180˚.

Table 2-7 Experiment results on dc side for DPWM when M=0.9, θ=90˚

Interleaving Angle	EXPERIMENTAL RESULTS	
	θ=0˚	θ=90˚
κ= 0	2.13A (100%)	2.48 A (100%)
κ= 90˚	1.35A (63%)	1.79A (72%)
κ= 180˚	1.15A (54%)	1.16A (47%)

Furthermore, as analyzed in Section 2.4.3, the circulating currents can generate dc side ripple currents when interleaving is used. This can be seen by comparing the experimental and calculated results without considering the effects of the circulating current shown in Table 2-8. The case with SVM, M = 0.5 and θ = 0˚ is used as an example. This table shows a relative error between 2 % and 14 %. As seen, the difference is high, especially when interleaving is used, as the ripple currents have been reduced significantly by interleaving as predicted in the previous section.

Dc circulating current and CM circulating current in switching frequency can be obtained from experimental data. After considering the effects of those two types of circulating currents, the recalculated results are also listed in Table 2-8. From Table 2-8, the relative error between the experimental results and calculated results can be reduced to reasonable level after the effects of circulating currents are considered. And since only dc and switching frequency CM circulating current are considered to reduce the relative error, the assumption in last section that these two types of circulating current are the main circulating has also been verified.

Table 2-8 Experiment results on dc side

rms of i_{dc}	M=0.5 , θ=0, central aligned SVM		
	EXPERIMENTAL RESULTS	ANALYSIS RESULTS WITHOUT EFFECTS OF CIRCULATING CURRNETS	ANALYSIS RESULTS WITH EFFECTS OF CIRCULATING CURRNETS
κ= 0	5.33A (100%)	5.21A (98%)	5.21A (98%)
κ= π/2	1.89A (100%)	1.63A (86%)	1.79A (95%)
κ= π	5.42A (100%)	5.20A (96%)	5.31A (98%)

2.5 Summary

This chapter presents a comprehensive analysis studying the impact of interleaving on harmonic voltages and currents on ac side of paralleled three-phase voltage-source converters. The analysis considers modulation schemes, interleaving angle, and operating conditions. The effects of CM and DM circulating harmonic currents caused by interleaving are discussed in detail, which is the basic principle of interleaving. Based on the analysis results, the method to calculate the optimized interleaving angle for minimum ac line inductor and EMI filter is presented. The analysis on the harmonic current reduction with designed interleaving angle is verified by experiment.

Other than that, this chapter also presents a comprehensive analysis studying the impact of interleaving on ripple currents in dc side passive components for paralleled three-phase voltage-source converters. The analysis considers modulation schemes, modulation index, displacement angle and the interleaving angle. The effects of interleaving on dc side ripple currents are analyzed in analytical way for simple SPWM and in a numerical way for more complex space vector modulations. The analysis results show that the operation conditions can highly affect the selection of interleaving angle to minimize the rms value of total dc side ripple current. The effects of system circulating currents are also presented to increase the accuracy of analysis. The analysis on the dc side ripple current reduction with designed interleaving angle is verified by experiment.

Chapter 3 Circulating Current Control with Discontinuous SVM

This chapter presents a control method for the CM circulating current of paralleled three-phase two-level voltage-source converters (VSCs) with DPWM and interleaving. CM circulating current can be separated into two parts based on frequency. The high frequency part close to switching frequency is analyzed first, which can be limited by passive components. The low frequency part close to fundamental frequency is the jumping of CM circulating current, which is the main reason why it is usually believed not possible to implement DPWM and interleaving together. The reason of such low frequency CM circulating current is analyzed in detail. Based on that the method to eliminate such low frequency CM circulating current by avoiding the coexistence between different zero vectors are proposed.

In addition, this chapter also presents a control method to minimize the total flux in integrated inter-phase inductor. By eliminating the circulating when fundamental current achieves the peak range, the total flux is minimized and only determined by output current.

Both of the control methods will only introduce very limited additional switching actions, which will not significantly affect the system thermal design. Experimental results verify the analysis and the feasibility of the control methods.

3.1 Introduction

Three-phase two-level PWM VSCs have many advantages such as low harmonics, high power factor, and high efficiency, which make them the converter of choice in many ac medium and high power applications. Paralleling VSCs can boost system power rating and system redundancy.

As shown in Chapter 2, Interleaving can bring more benefits to paralleling VSCs. By phase-shifting (i.e. interleaving) the PWM switching cycles of each converters at an appropriate angle, the total voltage ripple due to PWM switching at the ac terminal can be reduced [12-13]. Because of the reduction of ripple voltage, the use of this PWM technique has the potential to reduce the size of the converters ac and/or dc side passive components, increasing power density. [14]

Also, it is well-known that DPWM [15], which is also called minimum loss space-vector modulation (SVM) or 60° clamped SVM, can help to reduce the device switching loss up to 50%, which can increase the converter power handling capability or reduce the need for cooling, again increasing system power density.

As a result, it is very desirable to implement these two PWM techniques together for applications seeking to minimize the weight and volume of power electronics systems [16], e.g. aircraft application.

However, in order to implement DPWM and interleaving together in a paralleled VSCs system the critical issue of the circulating current must be solved. Because of the imperfect symmetry in hardware or control, circulating current can be generated among the paralleled VSCs, even if all of VSCs are of the same type. The circulating current may increase the power loss, saturate the inductors, and overstress or even damage power

semiconductor devices. Interleaving generally worsens the circulating current problem because the carrier phase-shifted switching between converters can introduce additional high frequency common-mode (CM) circulating current close to switching frequency [13]. The problem can further deteriorate if interleaving and DPWM are used together, because additional low frequency, close to fundamental frequency, CM circulating current is introduced [15]. This low frequency CM circulating current is the main reason why it is usually believed interleaving and DPWM should not be used together in paralleled VSC systems.

If DPWM and interleaving can be implemented together, to further increase the system power density, it is still desirable to minimize the flux in the passive components used to limit the circulating current, so the system weight can be reduced.

Some works have been done to control or limit CM circulating currents in paralleled VSC systems. Ref. [17] and [18] add CM inductor to limit the circulating current in the system. Additional inter-phase inductors are used in [19] and [20] for the same purpose. Although passive components are necessary especially for high frequency CM circulating current, active control methods are also desirable to reduce the requirement of passive components for high power density purpose. Ref. [21] employs a zero-sequence Proportional Integration (PI) regulator in continuous central aligned SVM [22] to significantly reduce the low frequency CM circulating current. However, this method can not be used for paralleled system with DPWM. Ref. [15] suggests the SVM without using zero vectors should be used instead of DPWM to mitigate CM circulating current problem, but the system current THD will be increased. Ref. [23] presents a hysteresis-control method for paralleling the system with DPWM, but this method cannot

sufficiently limit the CM circulating current, especially when the system modulation index is low. In addition, the impact of interleaving when DPWM is used is not considered. And none of this method can realize the flux minimization for integrated inter-phase inductor.

This paper first compared different inductor structure used to limit circulating current. Based on that two integrated inter-phase inductor structures explained in detail, which are lighter than separate inter-phase inductors.

After that, the method to implement interleaving and DPWM is proposed. In section 3.3.1, the high frequency CM circulating current is analyzed first, which can be limited by passive components. After that the reason to generate the low frequency CM circulating current related to DPWM and interleaving is explained and the method to eliminate such low frequency CM circulating current is proposed. This control method can be applied to the system involving any structure of circulating current limit inductor.

Finally, the control method to minimize the total flux in integrated inter-phase inductor is proposed for system with DPWM and interleaving. If the total flux can be minimized, the core size for integrated inter-phase inductor can be reduced to increase system power density.

All of the analysis are verified by simulation and experimental results.

3.2 Comparison of Circulating Current Limit Inductors

This chapter studies the paralleled VSCs with common dc and ac buses. For controlling circulating currents in such a system, inductors are usually added and should be integral part of the system. As explained in Chapter 2, interleaving the paralleled VSCs changes some of the output harmonic currents into circulating currents. In addition,

interleaving will introduce extra CM circulating currents. Given the various issues discussed in Section I, circulating currents should be limited in paralleled interleaved VSC systems.

There are two principal inductor configurations for limiting circulating current: the CM inductor, shown in Figure 3-1, and the inter-phase inductor, shown in Figure 3-2.

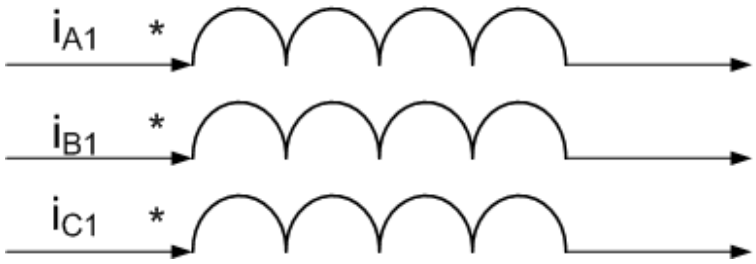

Figure 3-1. Structure of CM inductor.

Figure 3-2. Structure of inter-phase inductor.

Figure 3-3 shows the topology of a paralleled VSC system with a CM inductor, which can limit the CM circulating current in each VSC. Figure 3-4 shows the topology of a paralleled VSC system with additional inter-phase inductor, which can limit the difference between i_{A1} and i_{A2}. The inter-phase inductor can limit all circulating current in each phase, including CM and DM circulating currents. Note that in addition to the CM or inter-phase inductors, Figure 3-3 and Figure 3-4 also have three-phase inductors used as boost inductors in rectifier configuration. Three-phase inductors are assumed since they are usually smaller than corresponding single-phase inductors.

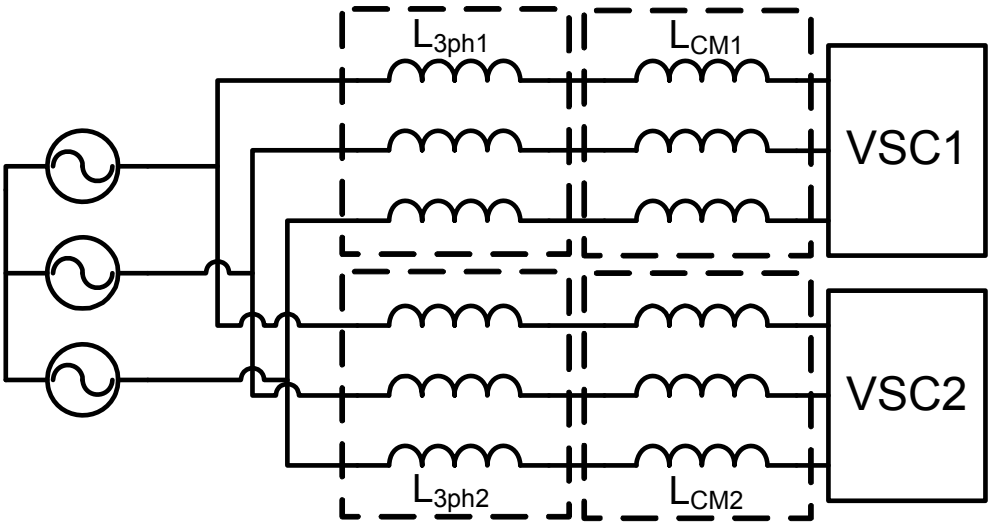

Figure 3-3. Topology of paralleled VSCs system with a CM inductor.

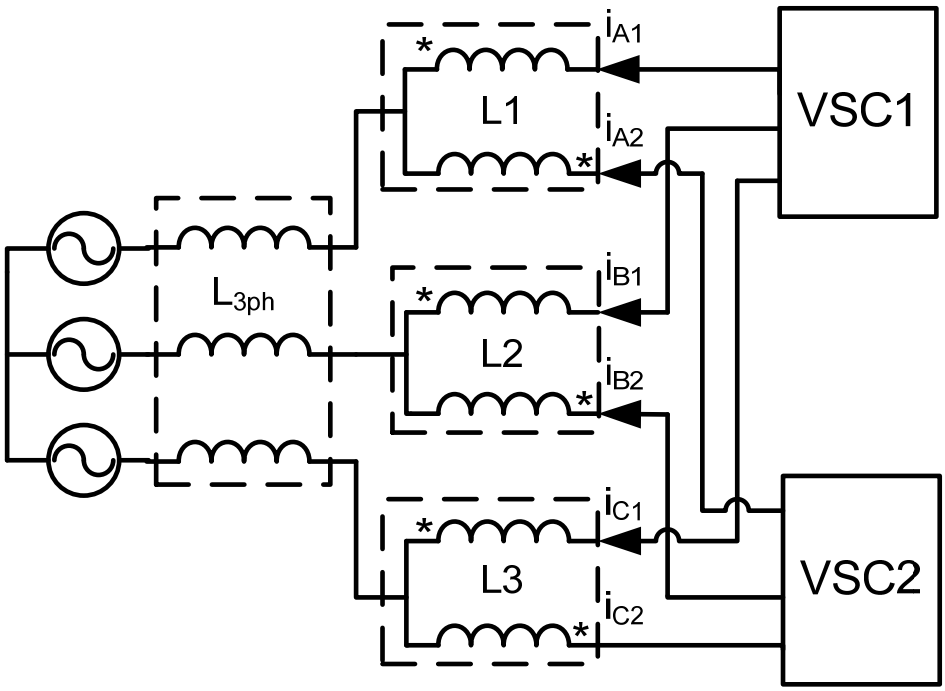

Figure 3-4. Topology of paralleled VSCs system with an inter-phase inductor.

Since the inter-phase inductor can limit both the CM and DM circulating current, it is a more effective approach. On the other hand, the inter-phase inductor couples the two

VSCs together, so each VSC cannot work by itself. The topology with CM inductors doesn't have this limitation, and therefore is more suitable for modular design

To facilitate the discussion in Figure 3-4, additional inter-phase inductors are used. This topology is easy to understand, but additional cores and wires are needed to build this type of inter-phase inductor, which increases the total weight of the inductor.

A better inductor structure is to integrate the boost inductor and inter-phase inductor together. One integrated structure of inter-phase inductor is shown in Figure 3-5. As Figure 3-5 shows, a set of CC cores is used. The main inductance is used as an inter-phase inductor, and the leakage inductor of the two windings are used as a boost inductor for two phase As in two VSCs. In contrast with the separate inter-phase inductor design, only one set of cores and two windings are used to realize the inter-phase inductor and boost inductors. In this way, the total weight of the inductors can be further reduced. Figure 3-6 shows the topology of a paralleled VSC system with integrated inter-phase inductor.

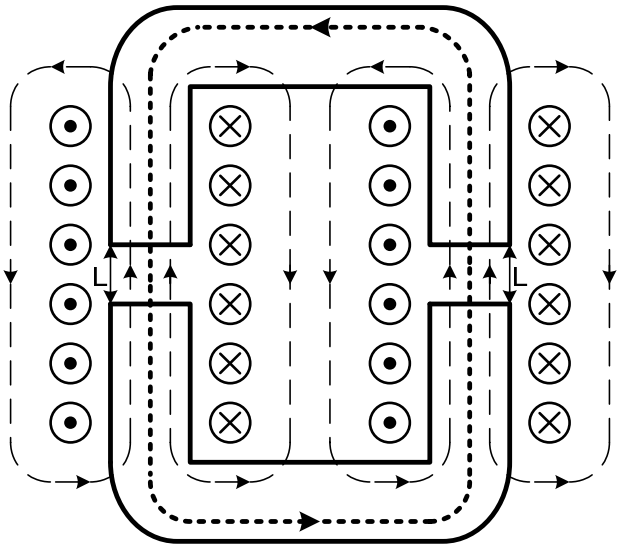

Figure 3-5 . Integrated inter-phase inductor (CC core).

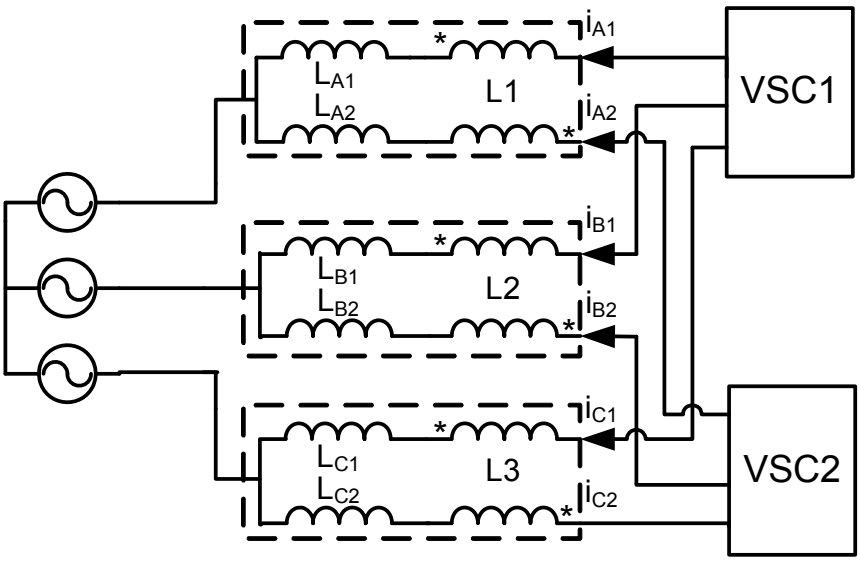

Figure 3-6. Topology of paralleled VSCs system with an inter-phase inductor.

However, in the structure shown in Figure 3-5, the leakage is utilized for boost inductor which is not easy to calculate and control accurately. In addition, flux of the leakage inductance will go through the air which may cause some EMI issues. To control the inductance for both inter-phase inductor and boost inductor accurately and constrain the flux, another integrated inductor may be used, as shown in Figure 3-7.

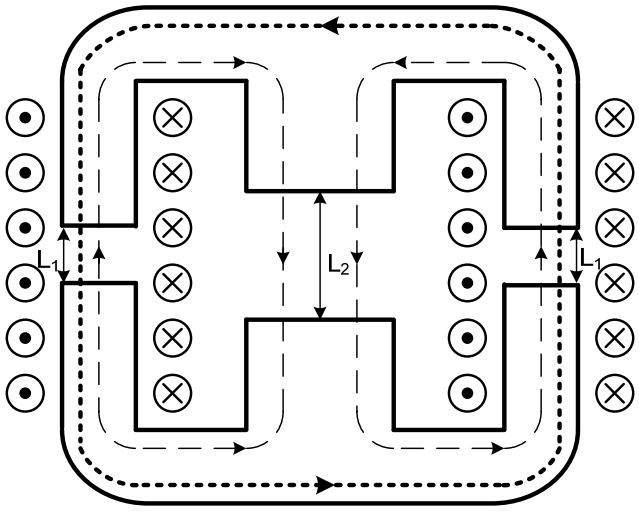

Figure 3-7. Inductor with integrated inter-phase inductor and boost inductor (EE core).

Compared with the structure shown in Figure 3-5, in Figure 3-7, two EE cores are used. The loop of main inductance used as inter-phase inductor is the same. But for the boost inductor, the flux is mainly constrained in L2 instead of in the air. As a result, the classic design methodology in [] can be used to design the boost inductor and inter-phase inductor. the inductance of boost inductor can be controlled by the length of air gap accurately. Since usually the designed inductance for inter-phase inductor is much higher than that of boost inductor, the design of the two types of inductors can be done separately. And since no leakage inductance is used, the EMI issue related to the flux in the air can be mitigated.

Figure 3-7, the middle leg in EE core is used to constrain the flux of boost inductor. Compared with the structure in Figure 3-5, such part of core is additional which will increase the weight of inductor. However, to achieve the desired value of boost inductance, some dimensions of the CC core in Figure 3-5 will be limited. For example, if high leakage inductance is needed, the height of the window cannot be high, so more layers of windings is necessary to achieve the needed turn number. As a result, the mean length per turn of winding will be increased which will increase the weight of total inductor. It is not easy to say which structure in Figure 3-5 and Figure 3-7 is light to build the same inductors until two optimized design based on these two structures are done.

3.3 Common Mode Circulating Current Control

3.3.1 High Frequency CM Circulating Current Caused by DPWM

This paper studies the paralleled VSCs with common dc and ac buses. There is no bulky transformer in the system to isolate the paralleled VSCs between each other, so the

system power density can be increased significantly. However, there will be paths in the system for CM circulating current.

Without loss of generality, the topology shown in Figure 3-8 is used for analysis first. The system consists of two paralleled VSCs fed from a common ac bus and connected to a common dc bus, and the power flows from the ac source to the load represented by a dc link resistor. The naming conventions for various currents and passive components are marked in the figure. There is no electrical isolation in the system such as transformer or isolated dc buses.

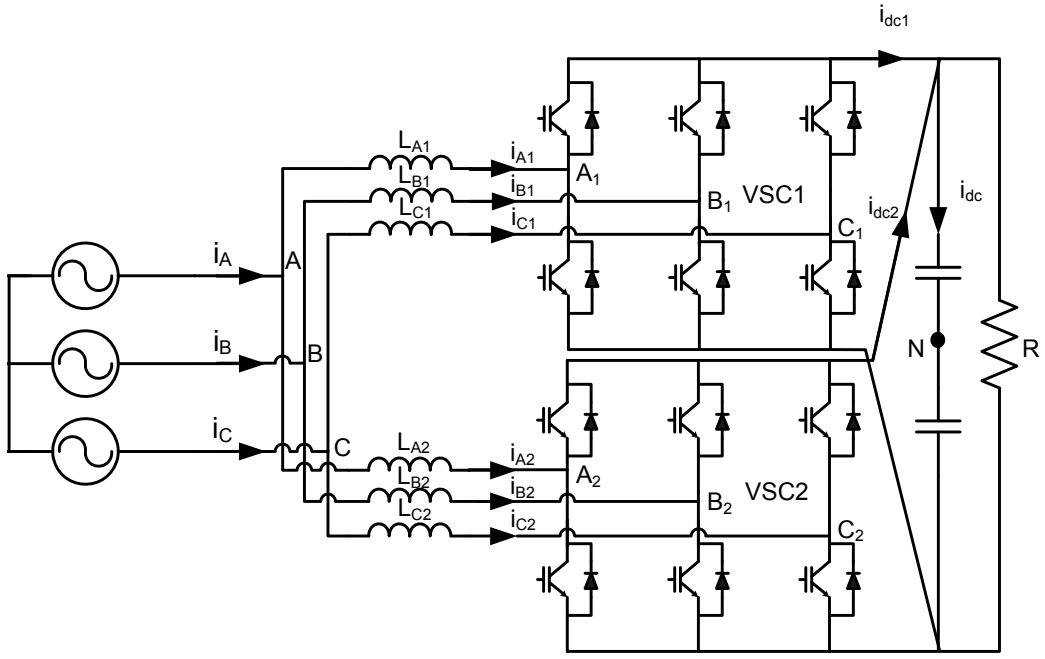

Figure 3-8. Sample converter system architecture under study.

As shown in last chapter, the switched phase-leg output voltage between ac terminal (e.g. point A_1) and dc link mid-point (N), v_{A1N}, can be decomposed into different harmonics. The frequencies of harmonic voltage components can be expressed as ($m\omega_c$+ $n\omega_0$), where ω_c is the angular frequency of the carrier wave, ω_0 is the fundamental line

frequency, and *m* and *n* are the carrier and baseband integer index respectively. Based on the double integral Fourier analysis approach, the harmonic component for voltage v_{A1N} corresponding to frequency ($m\omega_c + n\omega_0$) can be expressed as in (3-1) [24]:

$$v_{A1N}(m,n)(t) = C_{mn}\cos\left[(m\omega_c + n\omega_0)t + m\theta_c + n\theta_0 + \theta_{mn}\right] \tag{3-1}$$

where C_{mn} is the harmonic amplitude, θ_c and θ_0 are the initial angles of the carrier and reference waves, and θ_{mn} is a constant value depending on PWM scheme and operation condition. C_{mn} and θ_{mn} can be obtained as in (3-2) from the double integral Fourier analysis. Note that C_{mn} is only function of PWM scheme and modulation index *M*. For DPWM, the double Fourier integral limits are given in Table 2-4. Assuming the same carrier and symmetrical reference (with 120˚ apart) for the three phases for converter VSC1, its phase B and C voltage harmonic v_{B1N}(m,n), v_{C1N}(m,n) will be similar to (3-1) with identical C_{mn} and θ_{mn} but θ_0 will be displaced by 120˚. As a result, when n is triplen, v_{A1N}(m,n), v_{B1N}(m,n) and v_{C1N}(m,n) are the same. In other words, the harmonic voltages, when n is triplen, are CM harmonic voltages.

$$C_{mn}e^{j\theta_{mn}} = \frac{V_{dc}}{2\pi^2}\int_{-\pi}^{\pi}\int_{x_r}^{x_f} e^{j(mx+ny)}dxdy \tag{3-2}$$

For the group 2 converter VSC2, without interleaving (i.e., with identical carrier wave as group 1 converter), v_{A2N} will be identical to v_{A1N}. For three phase system, such CM harmonic voltages cannot generate any harmonic currents.

With interleaving, the carrier waves between VSC1 and VSC2 are phase shifted. As a result, for the harmonic components at frequency ($m\omega_c + n\omega_0$) in v_{A1N} and v_{A2N}, their amplitudes will remain the same as C_{mn} in (3-2), but the angle will be different. Specifically, an angle shift of κ by the VSC2 carrier will result in $\Delta\theta_c = m\kappa$ angle shift for

θ_c of v_{A2N} (m,n). As a result, even though the CM harmonic voltage still cannot produce output currents, they can produce CM circulating current. The amplitude of such CM circulating current is determined by the impedance of CM path and the difference between CM harmonic voltages v_{A1N} and v_{A2N} as in (3-3)

$$C'_{mn\_diff} = 2C_{mn}\sin(m\kappa/2) \tag{3-3}$$

Since the CM harmonic voltage at switching frequency is the dominant CM harmonic voltage [24], the CM harmonic currents at switching frequency is also the dominant CM harmonic circulating current. And such CM circulating current introduced in this section is called high frequency CM circulating current in this chapter.

To limit the amplitude of such high frequency CM circulating current, additional passive components are usually used to increase the impedance of CM circulating current path. All of the passive components compared in last section are useful to limit high frequency CM circulating current.

Since the switching frequency CM circulating current is the dominant CM circulating current, the amplitude can be used to estimate the amplitude of total high frequency CM circulating current, which can be calculated as:

$$i_{CM} = \frac{C'_{mn\_diff}(1,0)}{\omega_c L_{CM}} \tag{3-4}$$

where $C'_{mn\_diff}(1, 0)$ is the amplitude of CM harmonic voltage at switching frequency and L_{CM} is the impedance of CM path.

3.3.2 Low Frequency CM Circulating Current Caused by DPWM

In last section, the effect of DPWM and interleaving on circulating current are analyzed in frequency domain. To study the low frequency CM circulating current, the effect of DPWM and interleaving on CM circulating current is analyzed in time domain in this section.

DPWM scheme can significantly reduce the switching loss compared with the continuous SVM. Figure 3-9 illustrates the space vector DPWM scheme with only one zero vector used in each 60° sector separated by dashed lines. In Figure 3-9 “p” and “n” correspond to positive and negative states respectively. Thus the phase carrying the highest current can be clamped, theoretically reducing the switching loss by as much as 50% compared with continuous SVM.

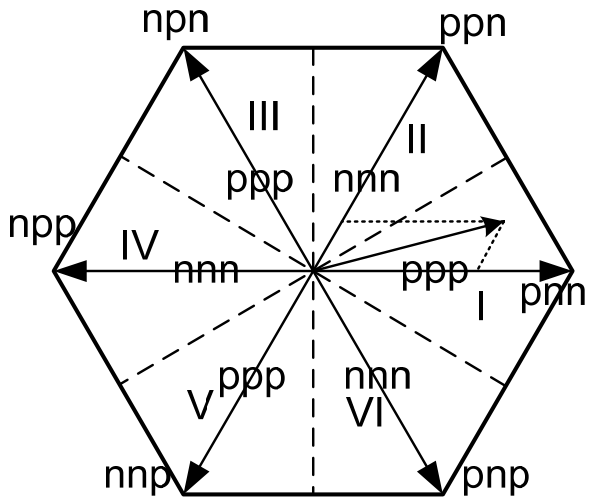

Figure 3-9. Principle of DPWM

With interleaving, the PWM waves of the two VSCs are phase-shifted. For a space-vector PWM, such a phase-shift means moving the position of the output voltage vectors relative to the space vectors. In DPWM, different zero vectors are used in adjacent

sectors. As a result, with interleaving, output voltage vectors for two VSCs, at the same time point, can be in different sectors.

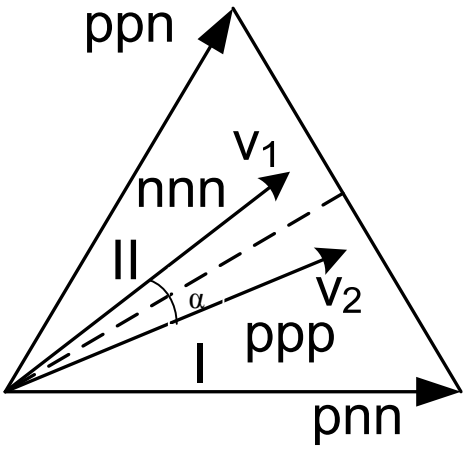

Figure 3-10 . Output vectors for two VSCs when zero vector is changed.

One example of output voltage vectors in different sectors is shown in Figure 3-10, where VSC1 voltage V_1 is in sector II and the VSC2 voltage V_2 will be in sector I. And the relative angle between V_1 and V_2 is defined as α which in ideal case is only determined by interleaving angle κ shown in Figure 2-1, as

$$\alpha = \kappa \frac{\omega_0}{\omega_c} \tag{3-5}$$

Take symmetric interleaving for example, where κ is π or 180˚ for two paralleled VSCs, the switching states of the phases in the two VSCs are shown in Figure 3-11, when the output vector crosses the boundary of sector I and sector II.

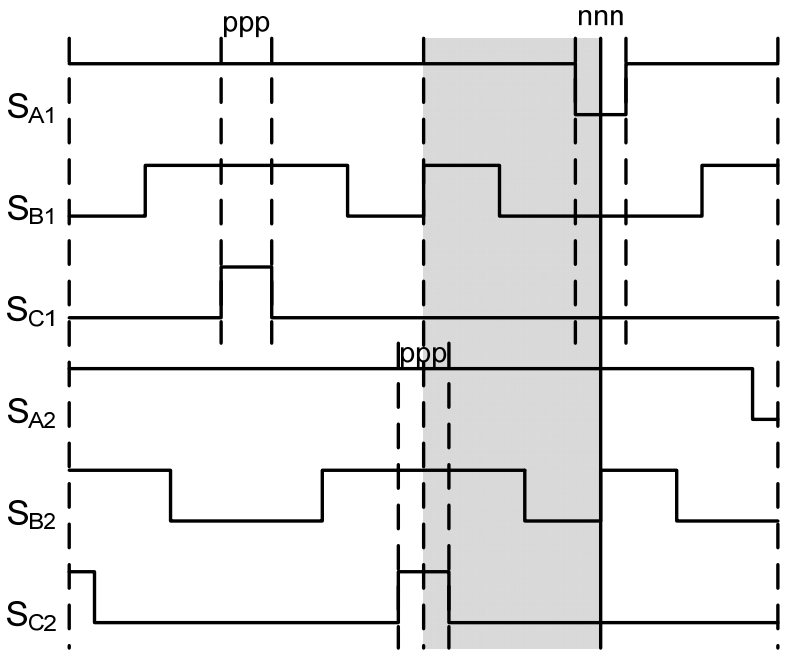

Figure 3-11. Switching states for two VSCs when zero vector is changed.

In Figure 3-11, because of interleaving and DPWM, there is half a switching cycle, highlighted in shade area, when the two different zero vectors (ppp) and (nnn) appear together. Because of this coexistence of different zero vectors in this period, the total zero sequence components of VSC1 and VSC2 are different. As a result, in addition to the high-frequency CM circulating current mentioned in Section II, a jumping of CM circulating current can be observed, and the amplitude of this jump can be estimated as:

$$\Delta i_0 = \frac{1}{2}\frac{V_{dc}T_0}{L_{cm}} \tag{3-6}$$

where T_0 is the duration of zero vector in the switching cycle.

Since all of these jumping happen when the vector cross the boundary of sectors, in other words, the positions of the vectors when the jumping happen are very close to the dashed line in Figure 3-10, T_0 in (3-6) can be estimated as

$$T_0 = (1 - M)T_s \tag{3-7}$$

where T_s is the duration of one switching cycle and M is the modulation index, defined as the ratio between line-to-line peak voltage and dc bus voltage ($0<M<1$).

From (3-6) and (3-7), the amplitude of CM circulating jumping can be written as,

$$\Delta i_0 = \frac{1}{2}\frac{V_{dc}(1-M)}{L_{cm}T_s} \tag{3-8}$$

Figure 3-12 shows the simulation results of the CM circulating current when switching frequency (f_s) is 20 kHz and fundamental frequency (f_0) is 400 Hz. In the simulation, open loop control is used so the positions of vectors can be controlled accurately and the effects of close loop control can be eliminated. Other than that, the parameters for two converters are exactly the same. However, the jumping of CM circulating current still cannot be avoided. In the simulation results, it is easy to observe the jumping of CM circulating current based on the high frequency CM circulating six times for each line cycle when the zero vector used is changed.

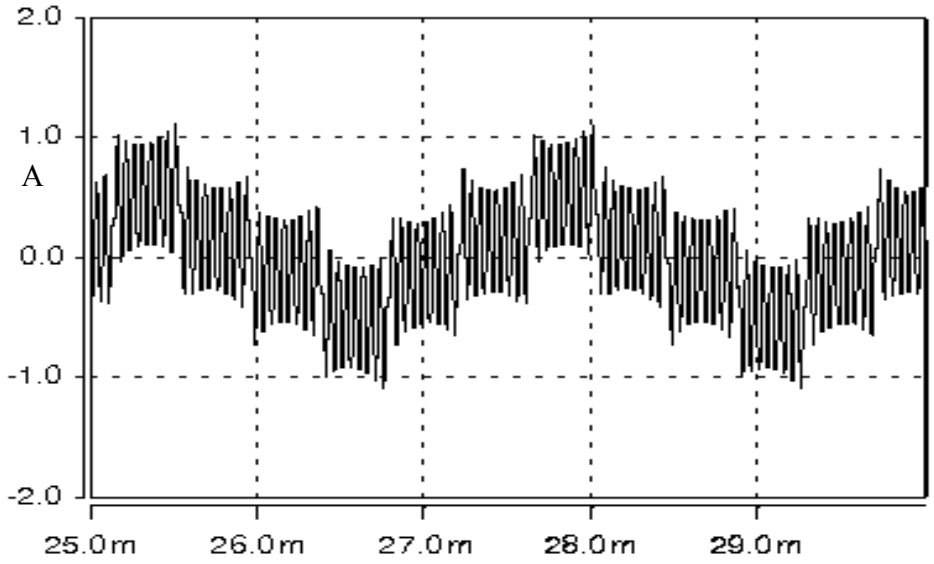

Figure 3-12. CM circulating current when f_s/f_0=50.

In the simulation, ideally CM circulating can jump up and down subsequently. But in the real system, with the effects of system asymmetric and close-loop control, the CM

circulating current, in this case, can continue increasing or decreasing. Even though high impedance of CM path can help reduce the amplitude of CM circulating jump, such passive components in the CM path still can be saturated if the low frequency CM circulating current is not controlled well and continues increasing or decreasing.

For asymmetric interleaving with interleaving angle κ other than π, the story is very similar, except the coexistence of different zero vectors is not half of T_0. However, it can be considered that VSC1 is leading VSC2 κ, or VSC2 is leading VSC1 (2π –κ). In the real system, both cases are possible for VSC1 or VSC2 to enter the new sector first. Even though κ is zero, the positions of VSC1 and VSC2 cannot always be the same. As a result, the coexistence of zero vectors can be $\kappa T_0/2\pi$ or $(1-\kappa/2\pi)\ T_0$. When $\kappa \leq \pi$, the maximum amplitude of the jump can be calculated as

$$\Delta i_0 = \frac{V_{dc}(1-M)}{L_{cm}T_s}(1-\frac{\kappa}{2\pi}) \tag{3-9}$$

Extremely, when interleaving is not used, κ is zero. If the relative angle α is very small but not zero, the only difference between V_1 and V_2 could be the zero vectors used. In this case, the coexistence of different zero vectors can happen for a whole switching cycle, which can be seen in the experimental results in Section 3.4.

3.3.3 CM circulating Current Control

Based on the analysis, we can conclude that the jumping of CM circulating current is caused by the coexistence of different zero vectors. If such coexistence is avoided, the jumping can be eliminated. This is the basic idea of the proposed CM circulating current control method.

To realize this control, the pattern of zero vectors should be changed temporarily when the coexistence of different zero vectors happens, which requires additional switching actions. Take the symmetric interleaving for example. With the proposed circulating current control scheme, one more switching action is added in phase C of VSC1, as shown in Figure 3-13.

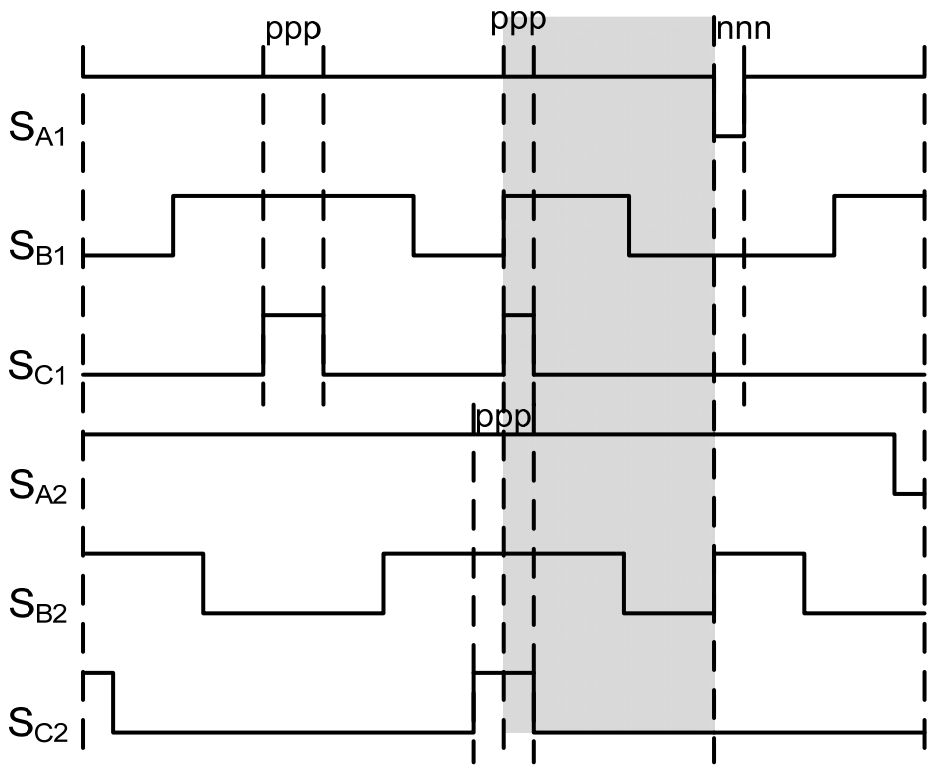

Figure 3-13. Switching states for two VSCs when zero vector is changed.

From Figure 3-13, one additional switching is added in phase C. The duration is half of the T_0. In this way, no coexistence of different zero vectors for each half switching cycle can be observed. And the jumping of CM circulating current can be eliminated. When the additional pulse is added, the pulse width of S_{A1} and S_{B1} is also adjusted consequently, so the duration of non zero vectors, which are (ppn) and (pnn) in Figure 3-11and Figure 3-13 are kept the same.

Since only when the vector cross the boundary of different sectors, the coexistence happens, six additional switching actions are needed in one line cycle for the whole system. Thus the penalty of increased switching loss is very limited.

From (3-9), lower modulation index means higher jumping of CM circulating current, so only the case of a low modulation index (M=0.5) is used to show the impact of this control method. The simulation results with and without the proposed CM circulating current control is shown in Figure 3-14 and Figure 3-15. By comparing those two simulation results, it is easy to see that the jumping of CM circulating current is significantly reduced. In the simulations, the switching frequency is 19.2 kHz which is 48 times of the fundamental frequency, 400Hz. As a result, the jumping up and down of CM circulating current happens consequently, when open loop control is used and the two VSCs are exactly the same. In real applications, it is very difficult to guarantee such condition, especially for rectifier application when the fundamental frequency is not constant. However, the feasibility of the proposed CM circulating current control method does not depend on specific carrier ratio, which can be seen from the experiment results shown in Section 3.5.

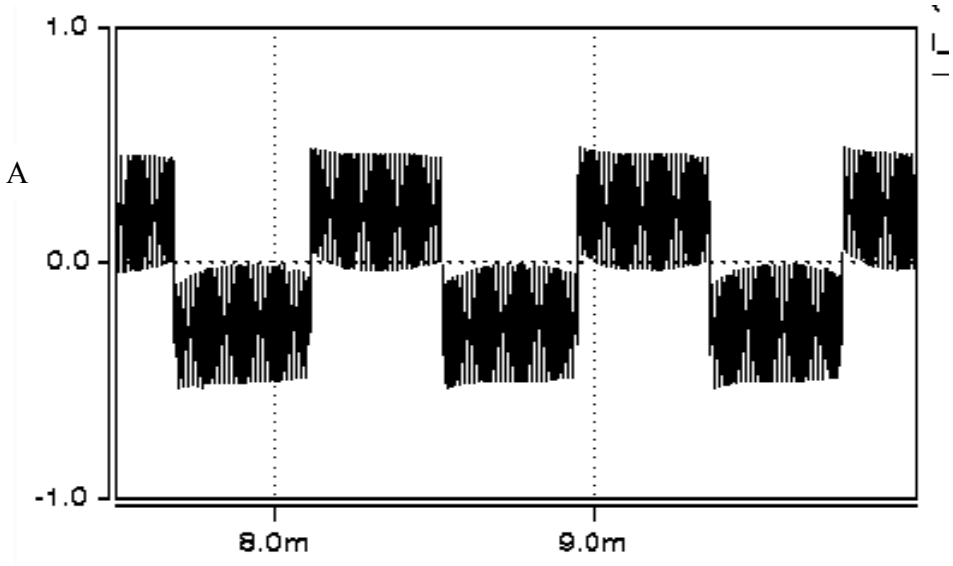

Figure 3-14. CM circulating current without control (M=0.5).

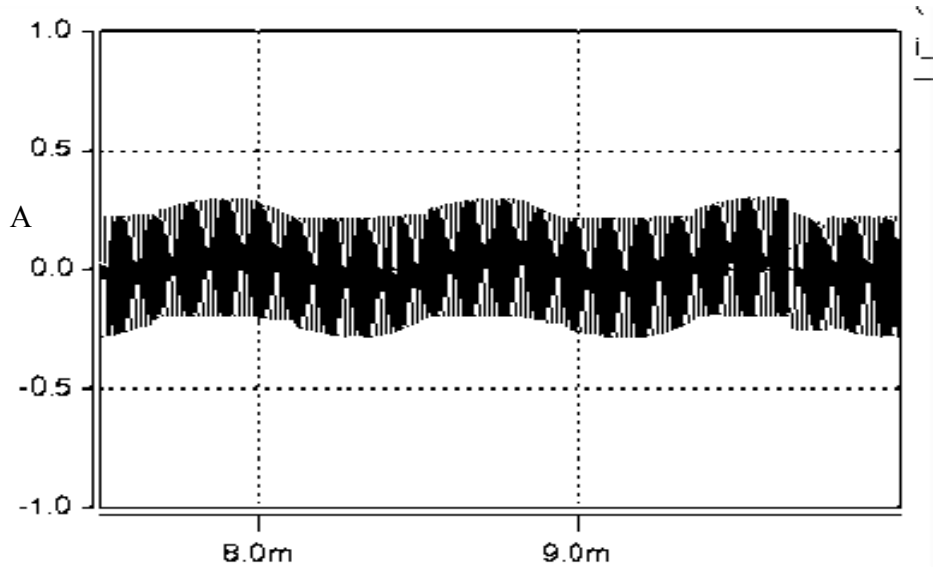

Figure 3-15. CM circulating current with control (M=0.5).

Figure 3-13, the additional pulse is place on the left side of the shaded area. However, if the duration of V_0 due to the additional switching in phase C is equal to half of T_0, the coexistence of different zero vectors can still be eliminated no matter where the additional pulse is placed within the shaded area. For example, if the pulse is place as shown in Figure 3-16, the coexistence of different zero vectors does not exist and the

duration of non zero vectors are kept the same, so the basic idea of this CM circulating control method can be realized.

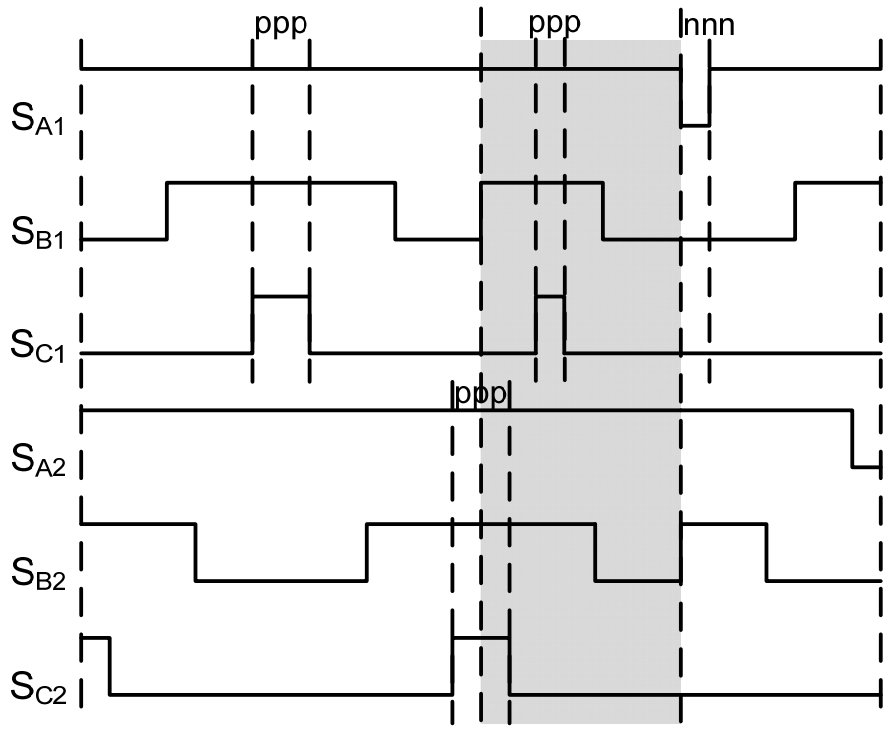

Figure 3-16. Switching states for two VSCs with one additional pulse.

Since the basic idea of output harmonic currents reduction by interleaving is to change output harmonic currents into circulating currents, which requires different vectors to be used by the paralleled VSCs, to maximize the benefit of interleaving, the same vector should be avoided using together by the paralleled VSCs simultaneously. From this point of view, the position of additional switching in Figure 3-16 is better than in Figure 3-13.

The same method can be applied to the system with asymmetric interleaving angle (κ is not π). When the duty cycle for one converter, e.g. VSC2, is under calculation, the type, position and duration of zero vector generated by VSC1 in previous case is already known. If the zero vector for VSC2 is the same as the zero vector generated by VSC1,

there will be no coexistence of different zero vectors in the system. So no additional switching is needed. If the zero vector for VSC2 is different from the zero vector generated by VSC1, considering the interleaving angle used in the system, the duration of additional pulses can be calculated to eliminate the possible coexistence of different zero vectors in the overlapped period such as the shaded area in Figure 3-16, and the position of additional pulse should be selected to minimize the period when the same vector are output by two VSCs together.

So far, the duration of additional switching action is calculated to eliminate the coexistence of different zero vectors. In fact the duration of additional switching action can also be controlled to limit the amplitude of total CM circulating current. From section 3.3.3, the amplitude of high frequency CM circulating can be calculated based on the impedance of CM path and dc bus voltage and switching frequency. The calculated results with certain margin can be used as a reference (e.g. I_{CM_max}) of the maximum I_{CM} allowed in the system. If the amplitude of the CM circulating current exceeds the preset level I_{CM_max} , when the additional switching is added, the duration of the additional switching can be adjusted to limit the CM circulating within allowed level. This idea is very similar to the method used in [21] for continuous SVM.

If the amplitude of the CM circulating current exceeds the preset level I_{CM_max} in normal operation, when no additional switching is used, DPWM can be interrupted and changed back to continuous SVM. Then the method to control the amplitude of CM circulating current mentioned in [21] can be used. But the switching loss will be increased accordingly.

3.4 Flux Minimization for Integrated Inter-phase Inductor

3.4.1 Principle of Total Flux Minimization

For both of the integrated inter-phase inductors, the flux of inter-phase inductor and boost inductor will share all, for CC core, or part, for EE core, of the core in integrated inter-phase inductors. In other words, when designing the core for such inter-phase inductors, the effects of boost inductor and inter-phase inductor flux should be considered together.

As shown in Figure 3-6, if the boost inductor for phase A is LA1 and the inter-phase inductor is L1, then the total flux in the core is

$$\Phi = L_{A1} i_{A1} + L_1 i_{cir} = L_{A1} i_{A1} + L_1 (i_{A1} - i_{A2})/2 \tag{3-10}$$

i_{A1} is output current which is determined by system power requirement. And the circulating currents, defined by half of the difference between i_{A1} and i_{A2}, are mainly high frequency circulating current, close to switching frequency, when interleaving and DPWM is used and the jumping of CM circulating current has been eliminated by CM circulating current control proposed in Section 3.3.

For simplicity, the output harmonic current is neglected, so the output current is purely sinusoidal waveforms. So the flux in boost inductor and inter-phase inductor can be expressed as in Figure 3-17. In the figures in this section to show the flux in the integrated inter-phase inductors, the peak value of the flux related to fundamental current is used as the unit.

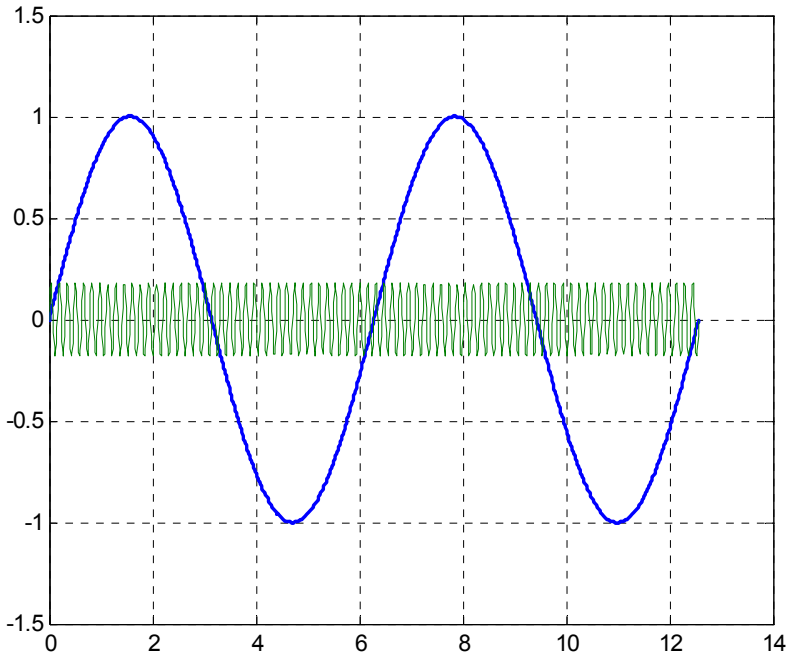

Figure 3-17. Inter-phase and boost inductor flux without flux minimization control.

So by adding these two types of flux together, in the sharing part of the core, the waveform of the total flux is as shown in Figure 3-18.

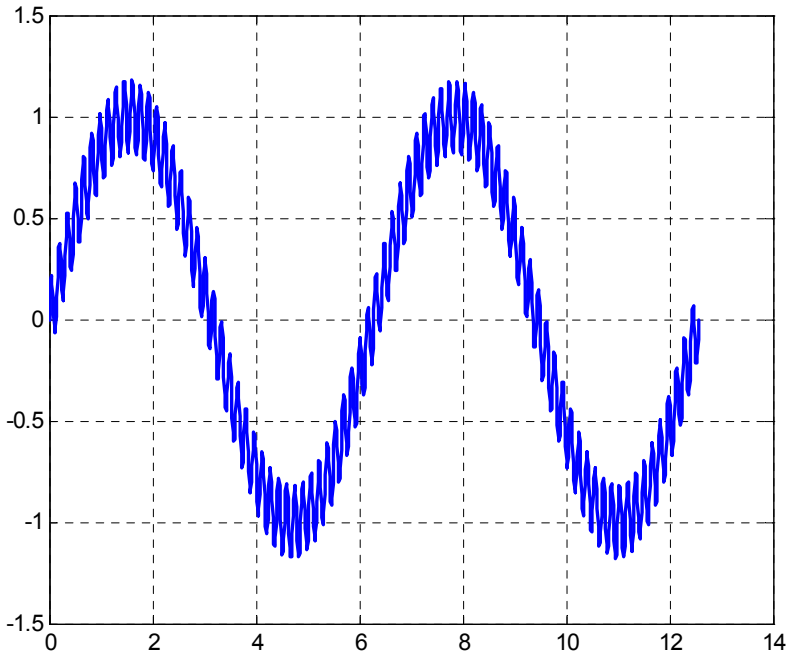

Figure 3-18. Total flux of integrated inter-phase inductor without flux minimization.

Since the output current is determined by system power requirement, which cannot be changed, only the flux related to circulating current can be reduced to minimize the total flux. Ideally, if the flux related to circulating current can be reduced to zero, then the total flux can be minimized and only determined by output current. However, this idea case cannot be realized, since it is impossible to reduce the circulating current to zero. Otherwise inter-phase inductor can be removed from the system directly.

However, even though the ideal case cannot be realized, the total flux can still be reduced to the same level, only determined by the output current, if the flux related to circulating current can be adjusted as shown in Figure 3-19.

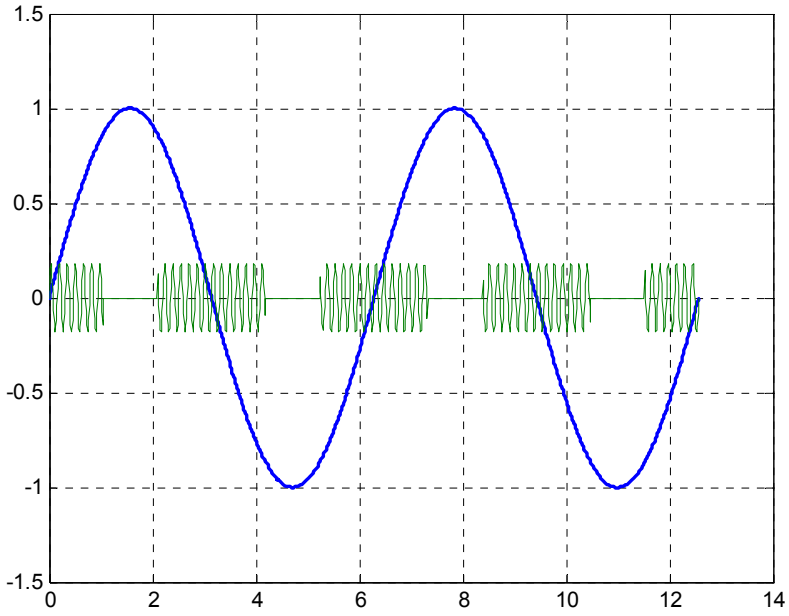

Figure 3-19. Inter-phase and boost inductor flux with flux minimization control.

In Figure 3-19, the circulating current is reduced to zero, when the fundamental current reaches the peak range (1/3 of the whole line cycle). Then the waveform of the total flux is as shown in Figure 3-20.

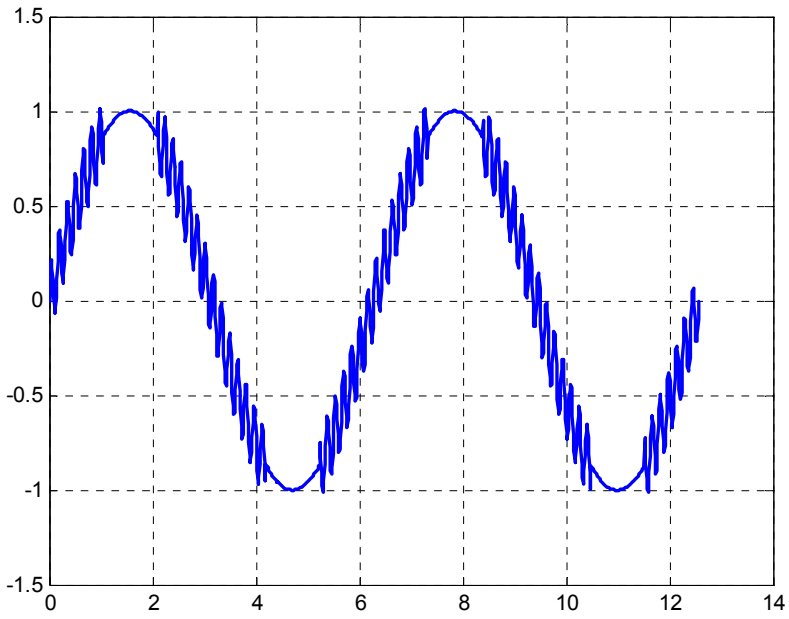

Figure 3-20. Total flux of integrated Inter-phase inductor with flux minimization.

From Figure 3-20 although the circulating current is not always zero, the total flux is still minimized, determined only by output current. This is the basic idea of the flux minimization control method.

If the amplitude of flux related to output current and circulating current is Φ1 and Φ2, the total flux Φ without minimization control is the sum of Φ1 and Φ2. From Figure 3-20 if Φ2 is less than 13.4% of Φ1, the total flux is always Φ1 with total flux minimization control. In other words, the total flux can be reduced as high as 13.4%. If Φ2 is more than 13.4% of Φ1, the total flux can be reduced by 13.4% of Φ2 with total flux minimization control. In either way, the core size can be reduced and the system power density can be increased.

3.4.2 Total Flux Minimization Control Method

When DPWM is used, the space vector DPWM scheme with only one zero vector used in each 60° sector separated by dashed lines as shown in Figure 3-9. Thus the phase carrying the highest current can be clamped, theoretically reducing the switching loss by as much as 50% compared with continuous SVM. At the same time, the integrated in the clamped phase will be shorted. One example is shown in Figure 3-21. In Figure 3-21, when i_{A1} and i_{A2} reach the positive peak range, the two phase Cs are clamped to the negative dc bus. As a result, the inter-phase inductor is shorted, as marked with dashed arrows.

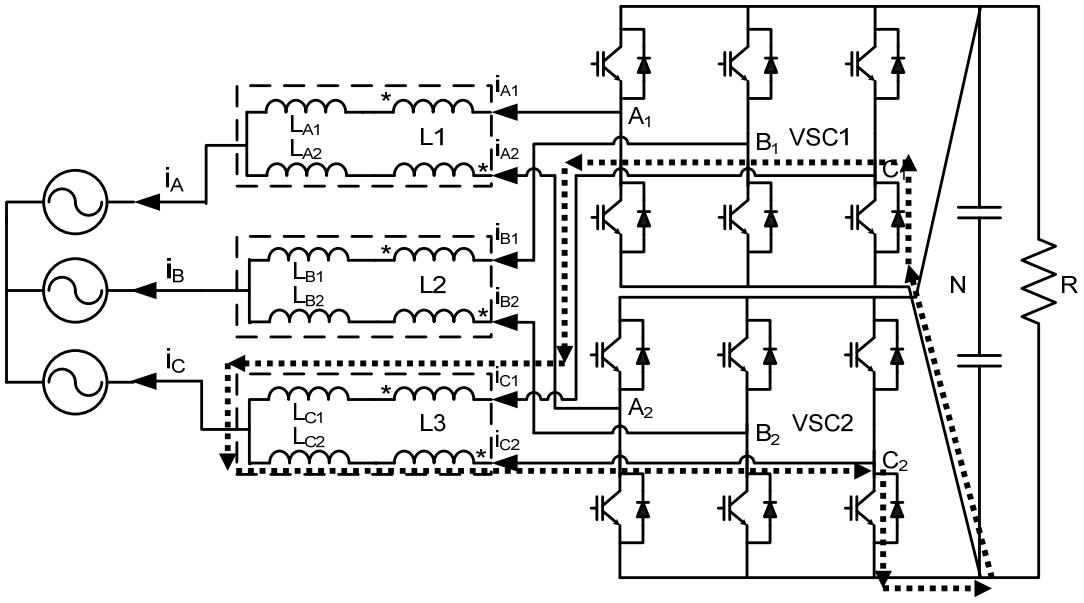

Figure 3-21. Two Phase Cs clamped in DPWM.

During this period, the circulating current in phase C will be nearly constant. Since in this period, the fundamental current in phase C is in the peak range, which is the operation principle of DPWM, if this circulating current in phase C can be corrected to zero before phase C is clamped, the circulating current will remain zero when the fundamental is in the peak range. In other words, the desired total flux minimization

shown in Figure 3-19 and Figure 3-20 can be realized. The same concept applies to other phases.

To correct the circulating current to zero, an idea is borrowed from [7]. As presented in [7] the amplitude of the CM circulating current can be adjusted by controlling the portion between ppp and nnn in the zero vector duration. Since CM circulating current is part of total circulating current, the amplitude of total circulating current can be also adjusted to zero by controlling the amplitude of the CM circulating current.

As presented in the last section, when the CM circulating current control method is used, six switching actions are added to the system in a line cycle. As shown in Figure 3-13, when each switching action is added, ppp and nnn can be used in the same switching cycle for one VSC. Thus there is additional penalty of switching loss when realizing the flux minimization control by changing the portion of ppp or nnn.

Taking the case in Figure 3-21 as an example, if there is a positive circulating current (defined by the direction show in dashed arrows) in phase C before phase C is clamped, longer nnn should be used. The switching states are shown in Figure 3-22. Compared with the switching states shown in Figure 3-21 when the durations of ppp and nnn are the same, the duration of ppp and nnn for VSC1 is adjusted to correct the circulating current in phase C to zero.

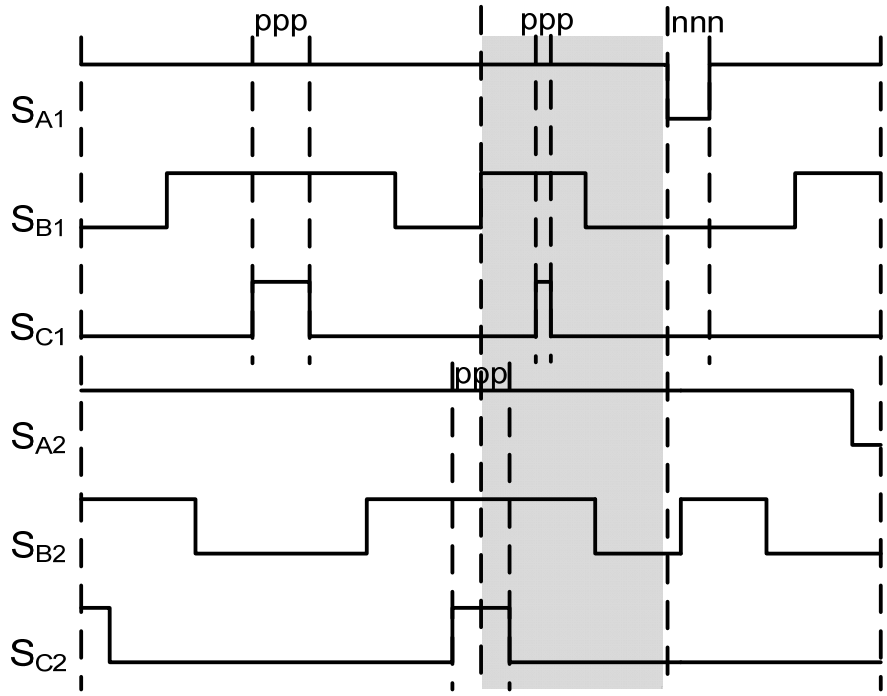

Figure 3-22. Switching states for two VSCs with one additional pulse.

Similarly, if there is a negative circulating current in phase C, a longer ppp should be used in Figure 3-22. The duration to change ppp to nnn to correct the circulating current i_{cir} to zero can be calculated as:

$$\Delta T = \frac{L_{CM} i_{cir}}{V_{dc}} \tag{3-11}$$

where the definitions of L_{CM} and V_{dc} are the same as in (3-4).

3.5 Experimental Results

The experiment is designed to verify three key points in the analysis above: 1) the existence of CM circulating current jumping due to interleaving and DPWM; 2) the feasibility of CM circulating current control method; 3) the feasibility of total flux minimization control method; 4) control method can work for cases with different modulation indexes and interleaving angles.

To simplify the experiment, the inverter configuration in Figure 3-23 is used, where the ac side now has a three-phase resistor load in addition to inductors. Since the amplitudes of harmonic currents are mostly limited by boost inductors, and the circulating currents are limited by inter-phase inductors that are the same as those in the rectifier configuration in Figure 3-6, the analysis and control methods are still suitable.

The experimental setup is comprised of two six-pack IGBT IPMs from Fuji (6MBP20RH060) for the two VSCs' power stages, one common DSP-FPGA digital controller, three integrated inter-phase inductors like those shown in Figure 2-21, and three 10 Ω resistors as the load. As discussed above, the leakage inductance of inter-phase inductor L_{leak}, which is 320μH, is used as the ac line inductor; and the main inductance L_{ip}, which is 3mH, is used to limit the circulating current. The dc voltage is 200V, and the fundamental and switching frequencies are chosen as 200Hz and 20 kHz, respectively. The rms value of fundamental current in the resistor load is 8A with a corresponding modulation index of 0.8. DPWM is used.

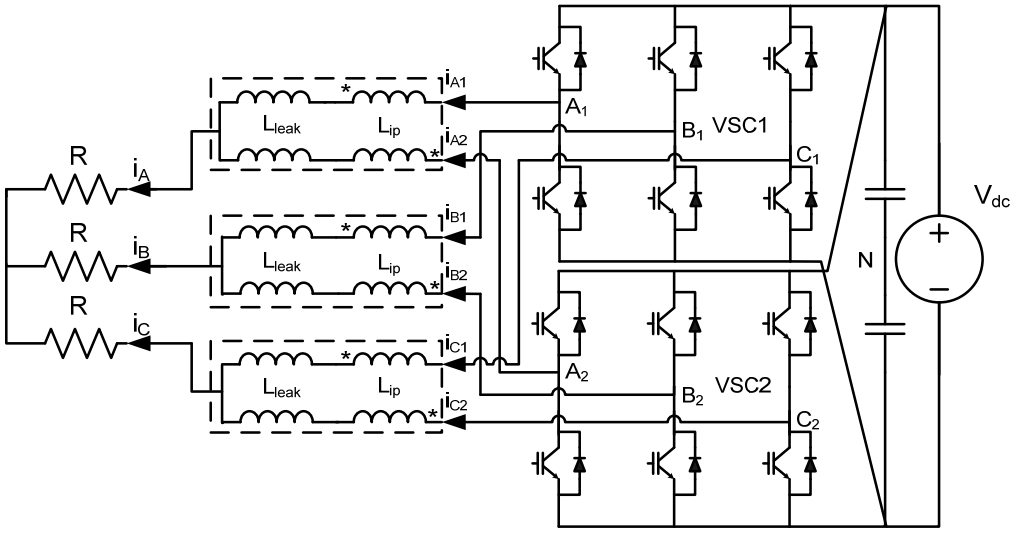

Figure 3-23. Schematic of the experimental setup.

Figure 3-24 shows the experiment results with symmetric interleaving or the interleaving angle π. In Figure 3-24 the switches are clamped every 60°, and the currents are controlled to the desired level.

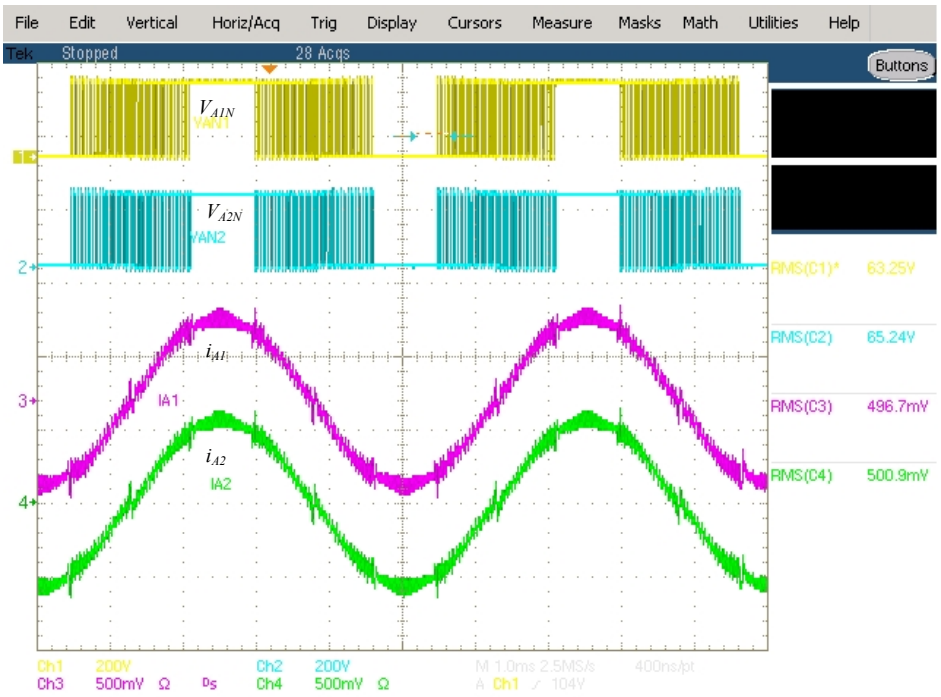

Figure 3-24. Experimental results waveforms (κ=180°).

To more clearly show the impact of circulating current control methods, waveforms are drawn in MATLAB based on the data obtained from experiment. The circulating current with and without the proposed circulating current control methods are shown and compared from Figure 3-25 to Figure 3-30.

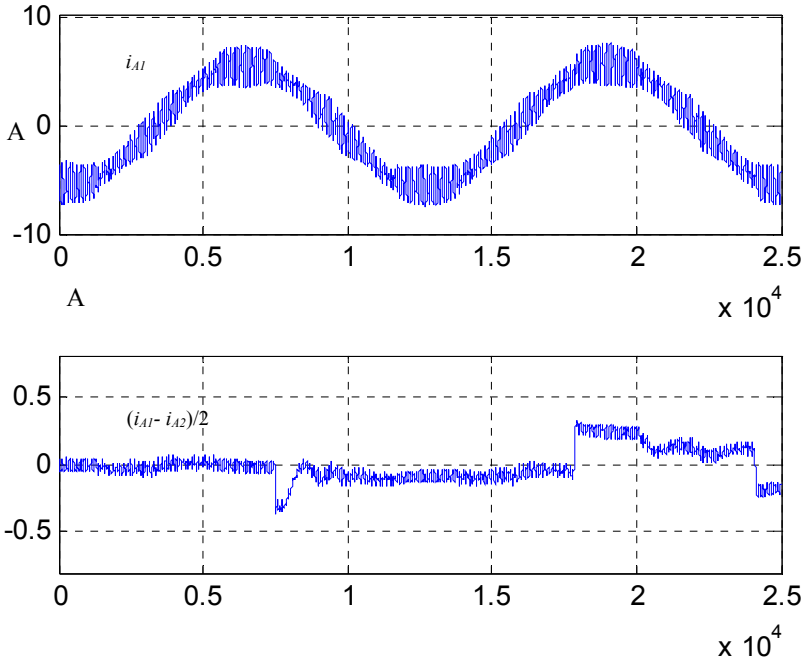

Figure 3-25. Experimental results without CM circulating current control (κ=0º, M=0.9).

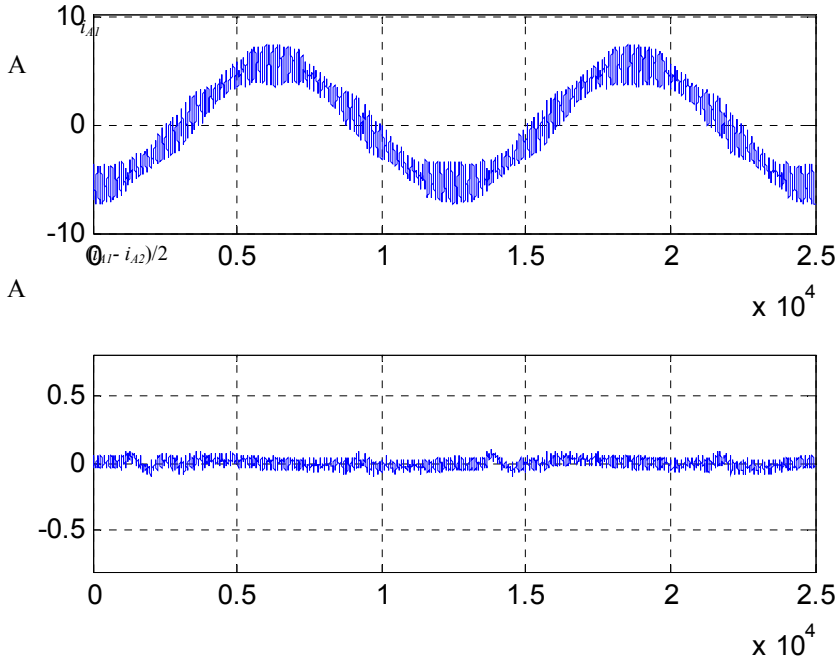

Figure 3-26. Experimental results with CM circulating current control (κ=180º, M=0.9).

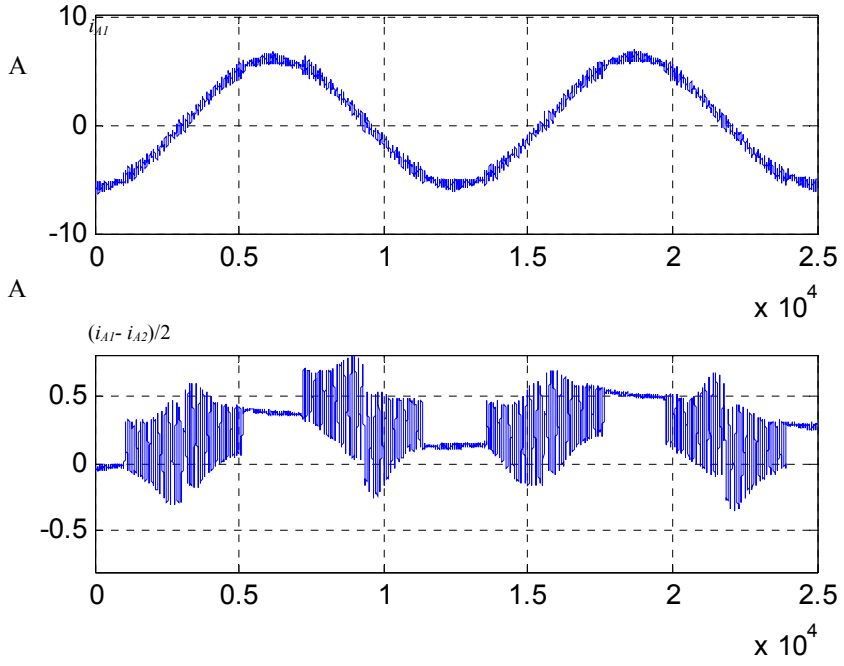

Figure 3-27. Experimental results without CM circulating current control (κ=180º, M=0.9).

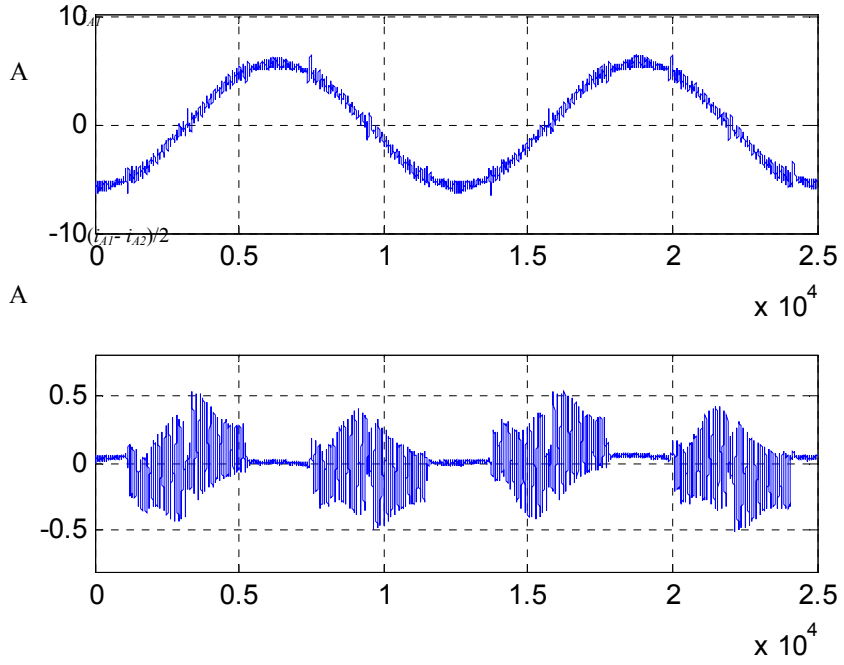

Figure 3-28. Experimental results with CM circulating current control (κ=180º, M=0.9).

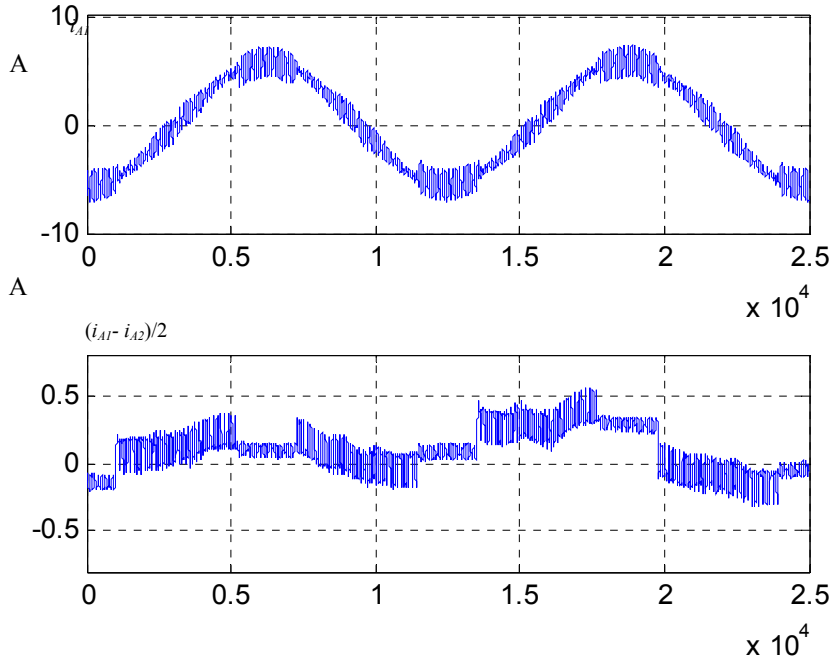

Figure 3-29. Experimental results without CM circulating current control (κ=55º, M=0.9).

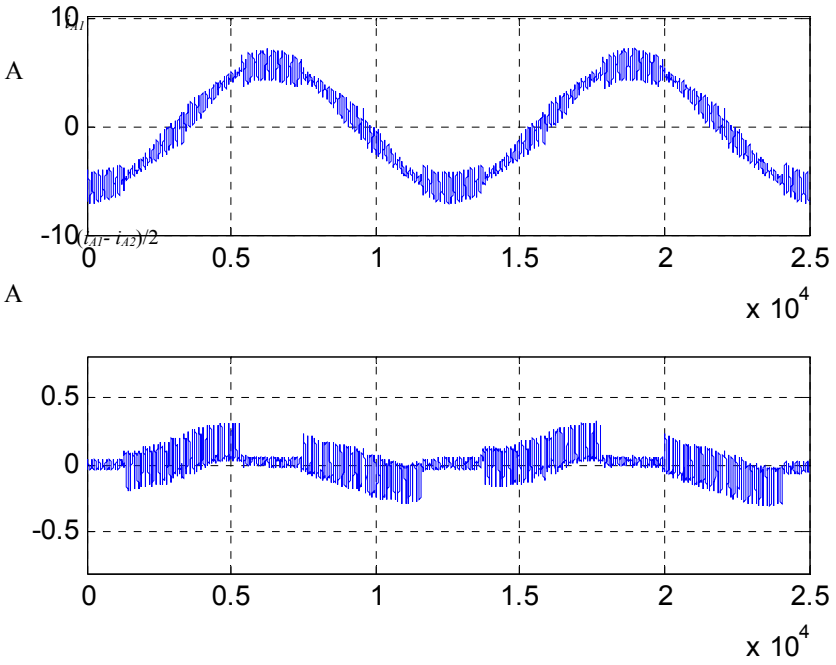

Figure 3-30. Experimental results with CM circulating current control (κ=55º, M=0.9).

From Figure 3-25 to Figure 3-30, the jumping of CM circulating current are very obvious without CM circulating current control. And the jumping are eliminated by the proposed circulating current control methods regardless of whether symmetric or asymmetric interleaving is used.

To further investigate the importance of using the circulating current control method, the experiment is repeated with a reduced modulation index of 40%. The experiment results are shown from Figure 3-31 to Figure 3-32. As the analysis in Section 3.3.3 predicts, lower modulation makes the circulating current problem even worse. In the experiment, when modulation is reduced, the jump in circulating current is greatly increased, and the output current waveform is distorted. When the circulating current methods are used, the circulating current can be controlled as well as it's controlled with a high modulation index. The feasibility of this CM control method is fully verified.

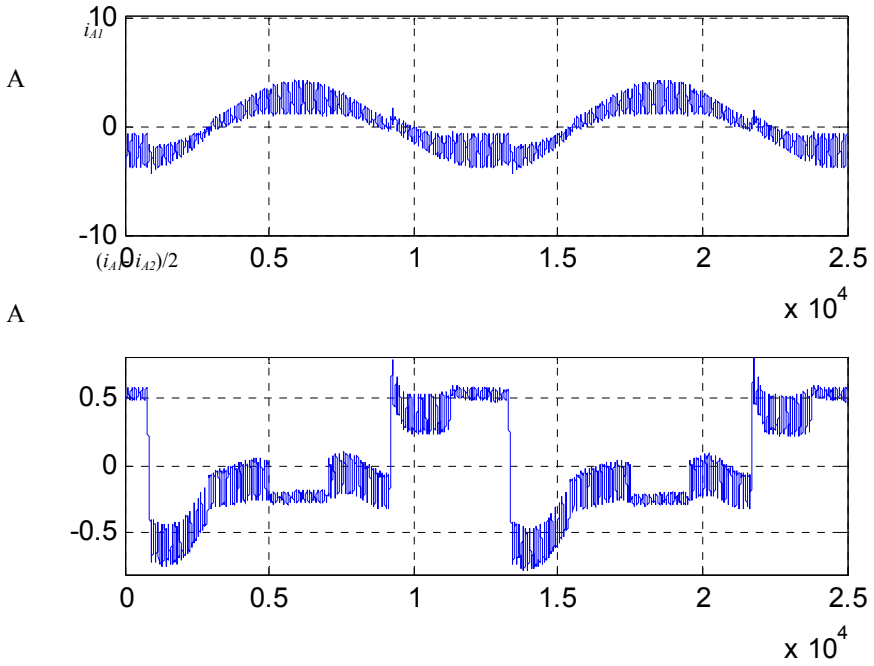

Figure 3-31. Experimental results without CM circulating current control (κ=55°, M=0.4).

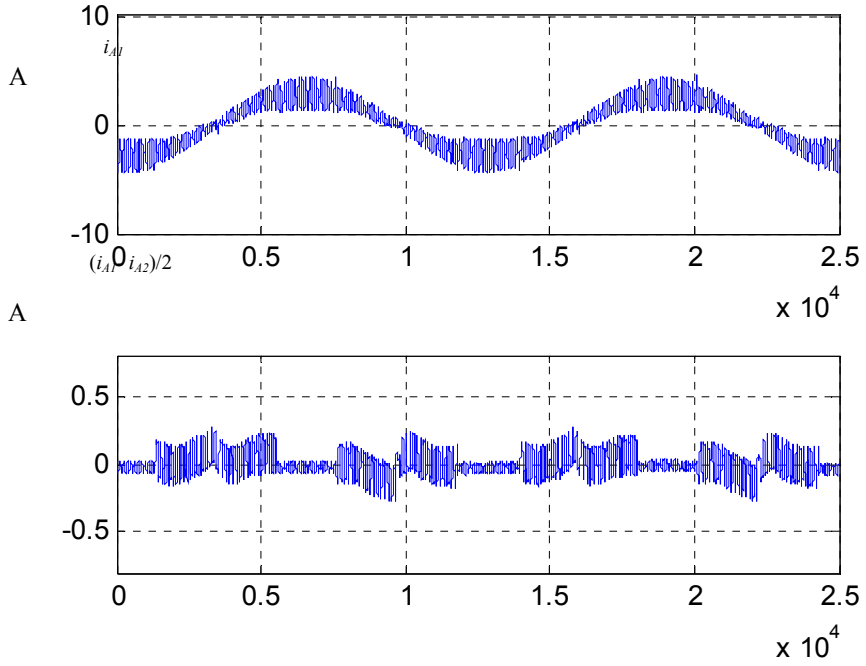

Figure 3-32. Experimental results with CM circulating current control (κ=55º, M=0.4).

From Figure 3-26, Figure 3-28, Figure 3-30 and Figure 3-32, the amplitude of circulating current has been limited very close to zero when the fundamental current reaches the peak range. The basic idea of total flux minimization has been realized. To demonstrate such control method more clear, the total flux is calculated as in (3-10) and shown in Figure 3-33 and Figure 3-34 when M is 0.8 and κ is 55º. By comparing the experimental results in Figure 3-33 and Figure 3-34, the total flux is minimized, only determined by output current. The feasibility of this total flux minimization control method is fully verified.

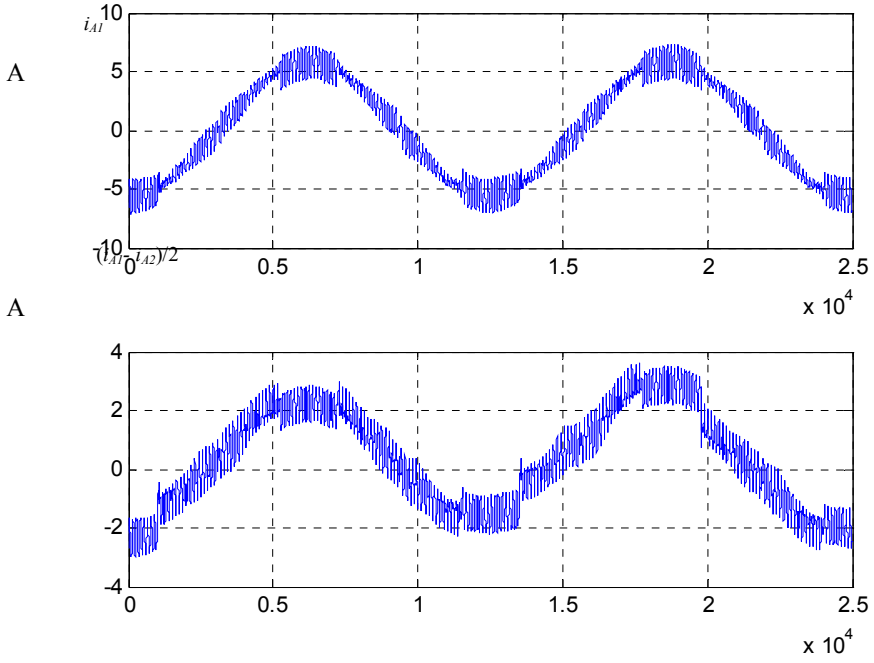

Figure 3-33. Experimental results without total flux minimization control (κ=55º, M=0.8).

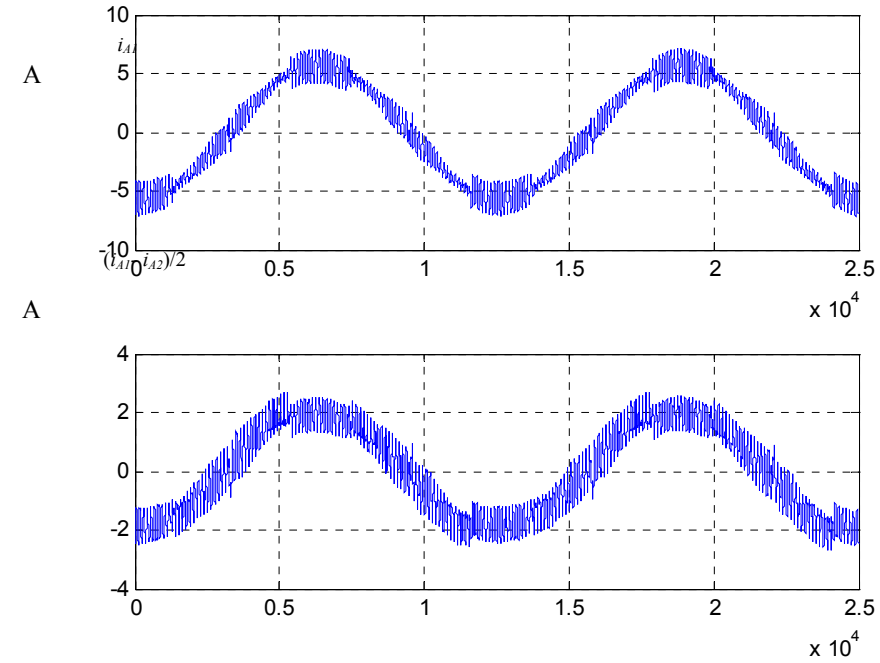

Figure 3-34. Experimental results with total flux minimization control (κ=55º, M=0.4).

3.6 Summary

This chapter first compared several different types of passive components to limit CM circulating current. After that two control methods are presented for CM circulating current in a paralleled VSCs system operated with DPWM and interleaving.

The first control method is used to help implement DPWM and interleaving together. There two kinds of CM circulating currents classified by the frequency. The high frequency part, close to switching frequency, can be limited by passive components. The low frequency part, close to fundamental frequency, is caused by coexistence of different zero vector, which can keep jumping up or down, finally saturating the passive components in CM path. Control method to eliminate the jumping of CM circulating is proposed. To realize the control method, six additional switching actions are added to the system, which will not increase the switching loss much. The feasibility of control methods are verified by simulation and experiment.

Based on that, the second control method is proposed to minimize the total flux in integrated inter-phase inductor for high power density purpose. With specified CM circulating current control and total flux minimization control, the core size in this kind of inductors is only determined by the flux related to output current. So the added system weight caused by interphase inductor can be minimized. To realize such controls, only very limited additional switching actions are needed. So the penalty of additional power loss is negligible. The feasibility of this inductor structure and the control methods are verified by simulation in this chapter and will be demonstrated in the next chapter.

Chapter 4 High Power Density System Design and Development

To show the benefits of proposed control methods and topology more clearly, the hardware development for a 15 kW three-phase ac-dc rectifier with the merit of high specific power density is presented in this chapter. SiC JFETs and SiC Schottky diodes are selected for the power stage in order to achieve high power and high switching frequency. Based on the analysis in Chapter 2 and 3, two paralleled three phase two-level VSCs are selected for the hardware system. All the concepts and methodologies developed and described in previous chapters, including interleaving angle optimization, integrated inter-phase phase inductor, CM circulating control method and integrated inter-phase inductor flux minimization control, are implemented in this hardware system. The hardware design and construction results are described in details. In addition, to meet the calculation speed requirement, a new digital controller, named Nano controller, is developed. The architecture and hardware are also presented in detail. At the end of this chapter, the weight distribution of the hardware system is analyzed and compared to the paper design.

4.1 System Configuration and Interface

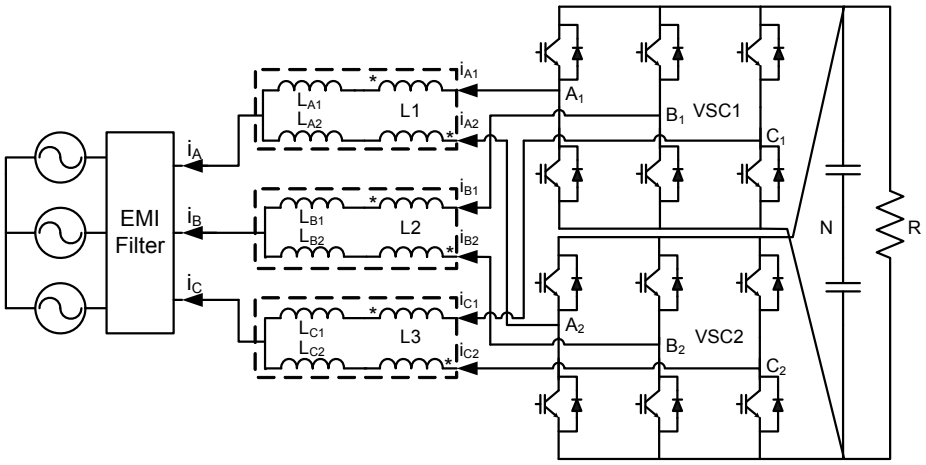

Figure 4-1. Hardware system circuit diagram.

Figure 4-1 shows the circuit diagram for the hardware system. The EMI filter block represents the multi-stage three-phase LC filter. Two three phase two-level VSCs are connected together through three inter-phase inductors to a common ac source, and connected to a common dc capacitor feeding the dc load.

The specification of this rectifier include: 230V rms ac side voltage, 650V dc side voltage, 15 kW power rating and DO160 EMI standard. The switching frequency is selected to be 70kHz following the design procedure in [91].

The hardware system is classified into the following sub-systems according to the functions and layout considerations:

(1)Digital controller, which consists of analog to digital conversion, DSP and FPGA for control implementation. Since two paralleled VSC are used and each converter operates at 70 kHz, the requirement of the calculation speed is very high. To meet such requirement, a new digital controller, named Nano controller is developed.

(2)Phase leg modules, which include all the switching devices and the corresponding gate drives, decoupling capacitors and heat-sinks. For the rectifier system, six power modules are fabricated.

(3)DC bus board, which provides the planar dc bus structure and the connection interface for the phase modules, filters, controller and protection circuits. The voltage and current sensors and the corresponding processing circuits are also included on this board.

(4)Input filter, which combines the functions of boost inductor and EMI suppression.

Figure 4-2 shows the interface of the system. Converter power stage represents the combination of the phase leg modules, dc bus board and the input filter. The hardware system terminals include a three-phase main power input, a 28 V control power input, a dc output, and three external control buttons. The interconnections between the controller and the converter power stage include the analog sensor signals (8 channels for the full system), the error signals generated by the shoot-through and other faults detection, and the power supplies (±15V, 28V, and 5V).

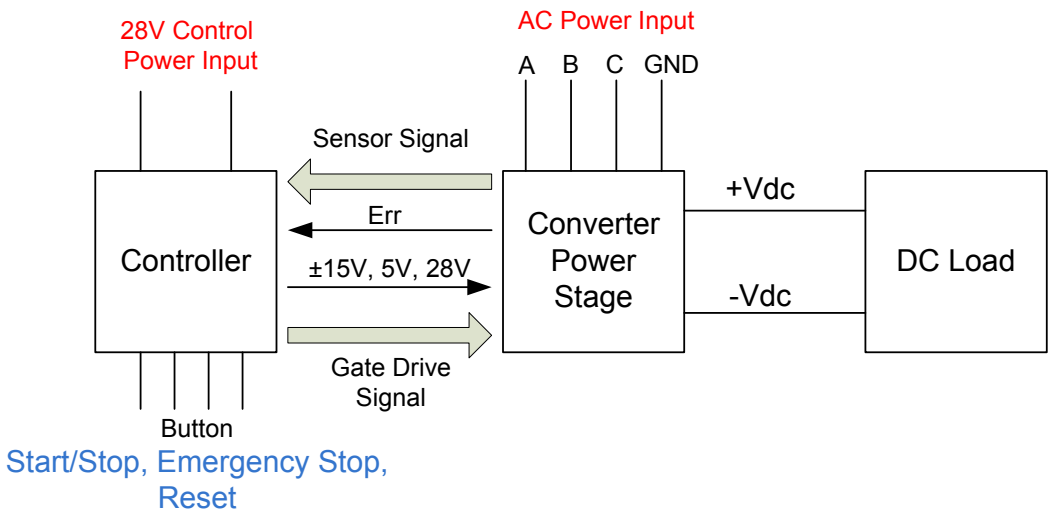

Figure 4-2. Hardware system interface.

4.2 Controller and Control Program Architecture

4.2.1 Nano Controller Architecture

As mentioned above, for the 15 kW three-phase rectifier, two converter are operated in parallel at 70 kHz. Since current universal converter in CPES which is developed about 10 years ago can only meet the control requirement for one converter operated at 35 kHz, it is necessary to develop a new digital controller to meet the calculation requirement. In additional, to further increase the system power density, the size of the new digital control should be small.

Also the functions of the new controller should be expandable, to meet the possible more strict requirements of more complex system in the future. In addition, to increase the power density of power electronics system, the size of the new controller should be small.

Considering these requirements, a multi-board stackable structure is used for the new digital controller. Because the size for each board is small and the distance between boards are also very limited, this new digital controller is named as Nano controller.

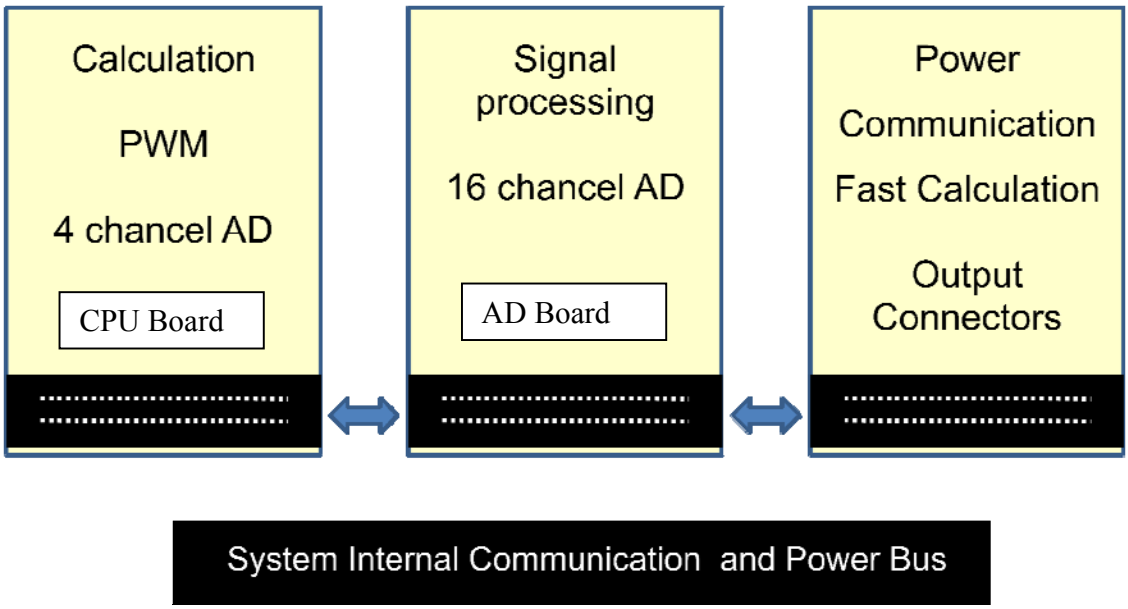

Figure 4-3. Nano controller architecture.

The architecture of Nano controller is shown in Figure 4-3. The functions of Nano controller can be divided into several boards, such as CPU board, AD board and other auxiliary boards. These boards can communicate with other boards by high speed system internal communication bus marked in Figure 4-3.

In the design, limited by the system cost and complexity, only 8 independent communication channels are provided in the communication bus. In other words, up to 8 boards in the Nano controller system can talk to each other. However, for a real complex system, if 8 boards cannot meet the requirement, one or more of the boards can work as communication boards to link two or more Nano controller systems together, so the function of Nano controller can be further expanded.

Even though different boards can be designed to implement different tasks, three boards are involved so far for this high power density rectifier project. As shown in Figure 4-3, the functions of Nano controller are separated into three boards: CPU board (shown in Figure 4-4), AD board and power supply board (shown in Figure 4-5). From

Figure 4-4, the size of CPU board is 9.5cm by 6.5cm which is a little larger than a credit card size. The other boards in Nano controller will be designed to be the same size. AD board can prepare the system data and transfer them to CPU board. And CPU board can use the data from AD board and local AD chips on CPU board for calculation and generate PWM signal to drive the power stage. Power supply board can provide power to the nano controller system and also provide buffer between the PWM signal in CPU board and mother board. More detailed description of Nano controller is shown in the Appendix.

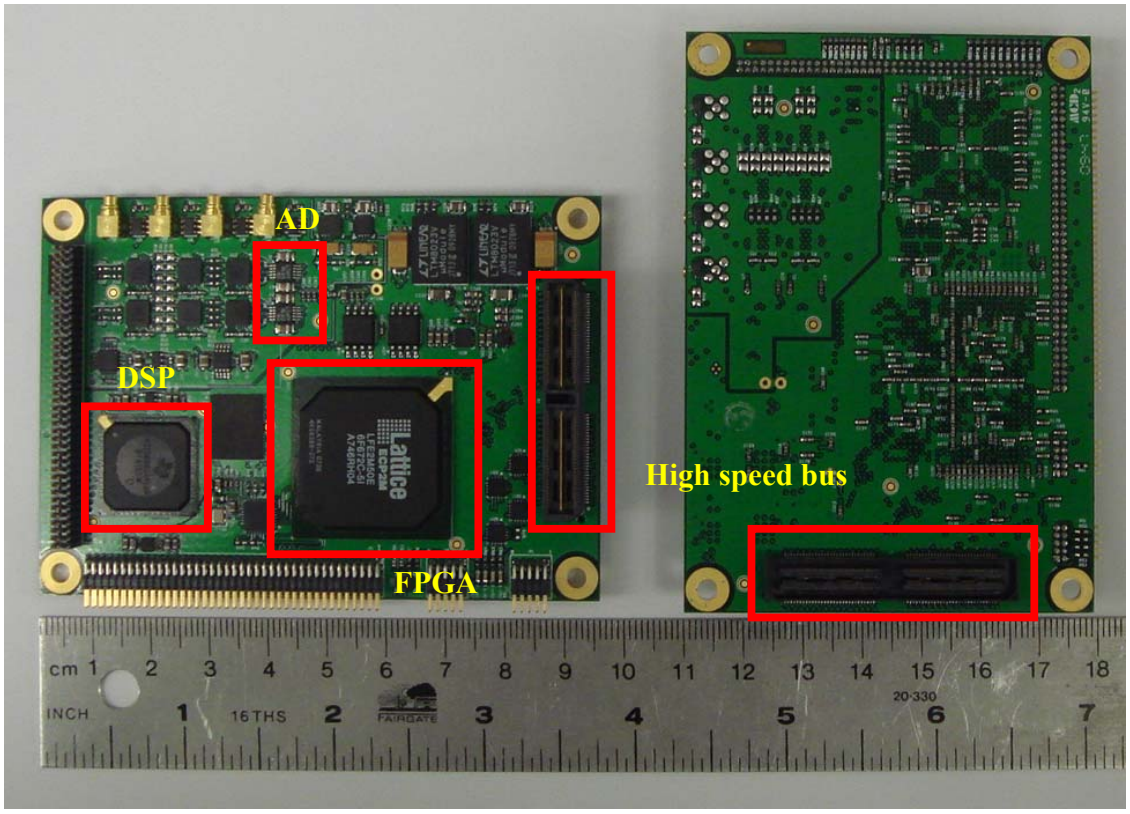

Figure 4-4. Top and bottom pictures of CPU board.

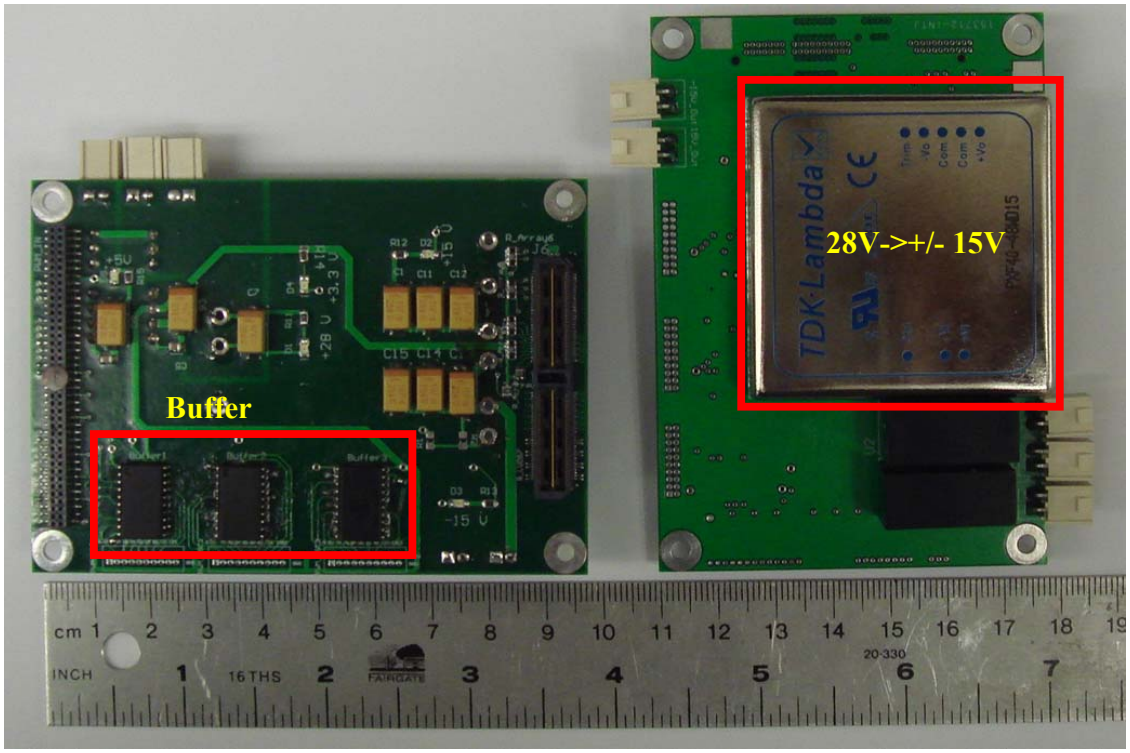

Figure 4-5. Top and bottom pictures of Power supply board.

Since the high power density rectifier only needs 8 channels AD and the AD board is still under fabrication, two CPU boards are used together. One is acting as a real CPU board, and the second one is acting as a 4 channels AD board. Actually, this is also an advantage of the architecture, since the resource on each board can be shared by the other boards in this system. The picture of the Nano controller used in this project is shown in Figure 4-6.

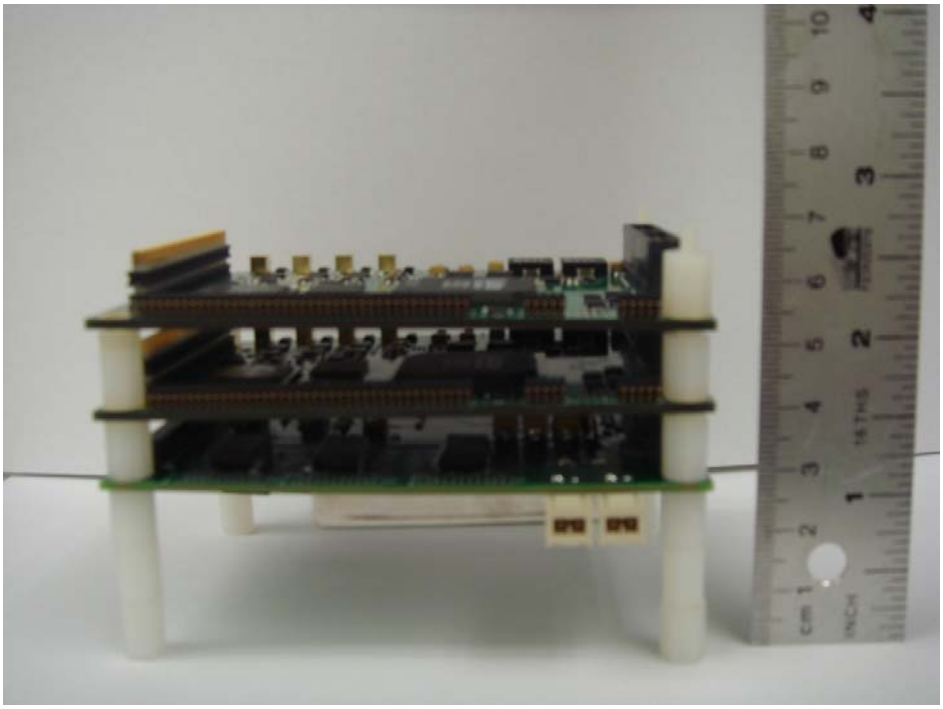

Figure 4-6. Picture of Nano controller system.

4.2.2 Control Program Architecture

The structure of the control program is shown in Figure 4-7. The analog signals are sampled and conversed to digital data by AD chips and copied to FPGA on AD board. This FPGA will transfer the data to series format and send them to the FPGA on DSP board through the high speed bus. The FPGA on DSP board will receive those data and transfer the data from series format to parallel format and send them to DSP. Finally, DSP can use those data to generate PWM signals used to control the power stage.

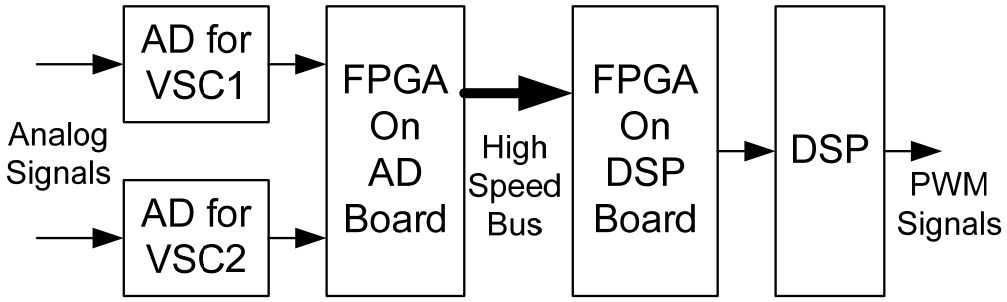

Figure 4-7. Structure of control system.

The time point to start a new AD conversion is controlled by FPGA. If oversampling is applied, since the sampling speed of the AD chips is over 20 times faster than the switching frequency in the project, the AD conversion for all of the channels can be synchronized. Otherwise, if only one point is sampled in each switching cycle, the AD conversion for VSC1 and VSC2 should be controlled with certain delay according to the interleaving angle selected.

The control diagram in DSP is shown in Figure 4-8.

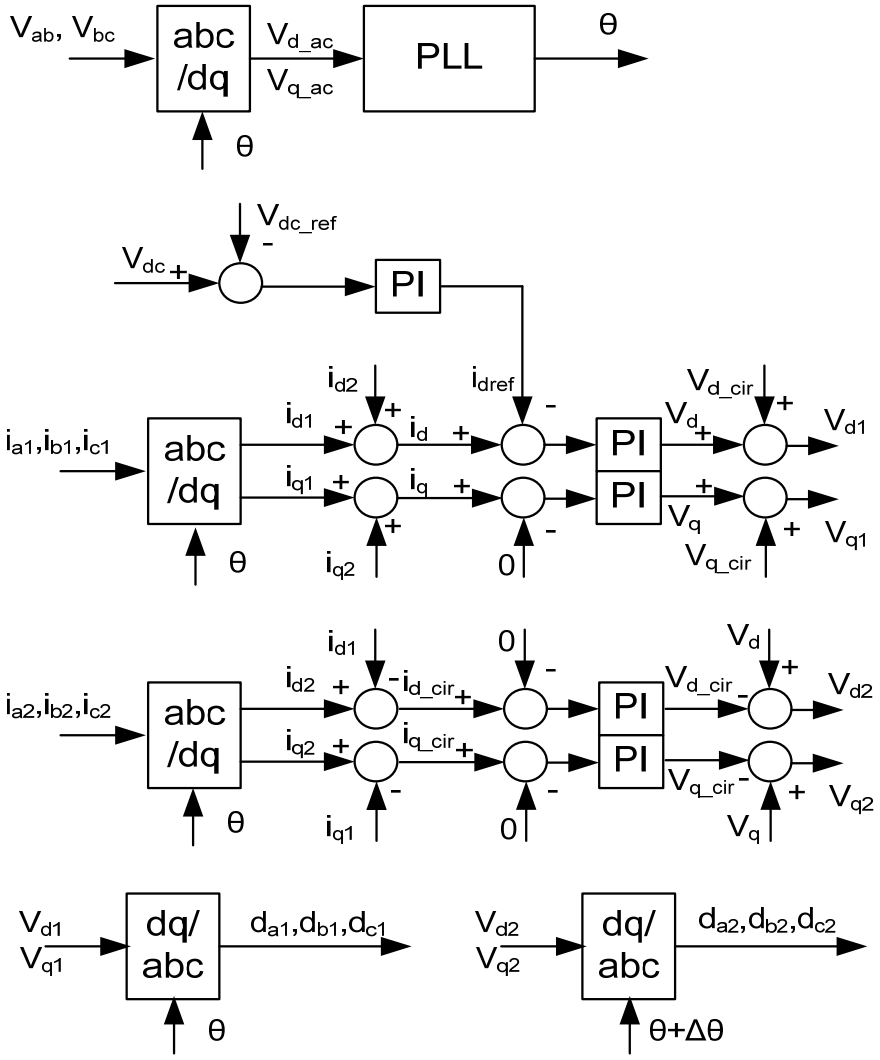

Figure 4-8. Control diagram in DSP.

As shown in Figure 4-8, there are six control loops in the control diagram: PLL or phase angle control loop, dc bus voltage control loop, output voltage control loop on d and q coordinates, and circulating current control loop on d and q coordinates. All of these control loops design are classic which will not be described in detail.

To implement interleaving in the paralleled VSCs system, $\Delta\theta$ is added for VSCs in the dq to abc transformation, so the output vectors for VSC1 and VSC2 are phase-shifted. And in time domain, the PWM signals for VSC2 should be delayed accordingly.

4.3 Power Stage Design and Construction

4.3.1 Phase Leg Module

The phase leg modules are designed and fabricated by another Ph.D student Puqi Ning. To keep the work complete, the phase leg modules are introduced briefly in this section.

As shown in Figure 1, the phase-leg module consists of two SiC JFETs. Based on a comprehensive survey [92] and lab evaluation, the materials for each part of the power module package are compared and selected. The finally selected materials for each part are listed in Table 4-1.

Table 4-1 Material selection list

Switch	1200 V, 4.18 mm × 4.18 mm from SiCED
Substrate	Aluminum Nitride (AlN) Direct Bond Copper (DBC) with 25 mils thick AlN, 8 mils thick Copper
Die-attachment	Au-Ge solder (360 ºC melting point)
Wirebond	5 mils Aluminum wire for gate pads on JFET dies; 10 mils Aluminum wire for other pads
Encapsulant	Nusil R-2188
Lead frame	8 mils thick copper stripe

As shown in Figure 4-9, the layout for wire bond module was designed by considering the reduction of parasitic parameters and the balance of the paralleled devices. Finally, case 5 is selected as the layout design.

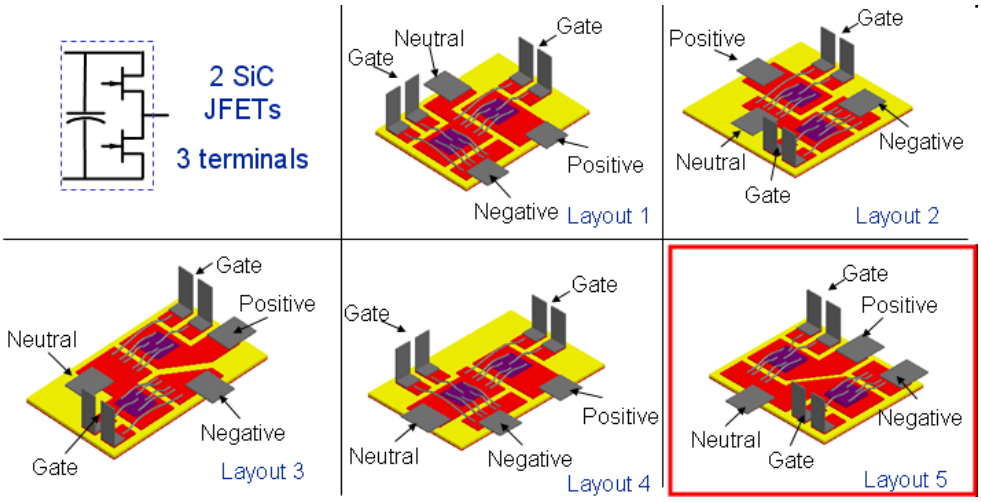

Figure 4-9. Layout design of phase leg modules.

The cooling system is designed by following the process presented in [93]. In 250ºC junction temperature operation, the power loss of each JFET is 46 W and the heatsink is selected as Z35-12.7B of AlphaNovaTech with 2m/s air flow.

The designed power module was then fabricated and amounted with gate drive PCB board, as shown in Figure 4-10.

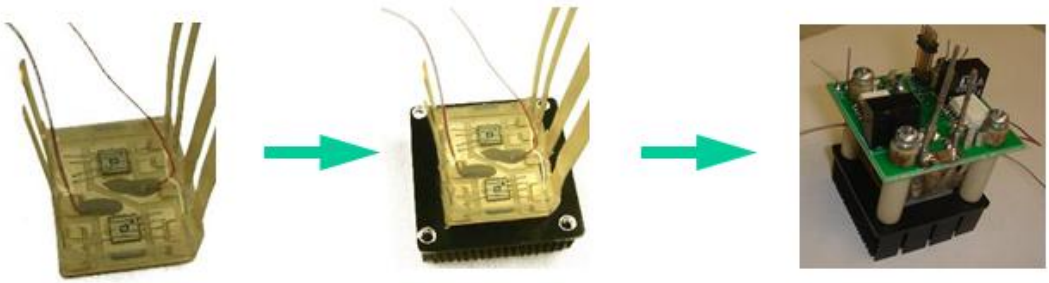

Figure 4-10. Picture of phase leg module.

With a simple buck converter circuit, the power module can be operated in rated voltage and current with 250ºC junction temperature. The testing results are shown in

Figure 4-14. Thus, the designed package enables the rating power at high temperature operation.

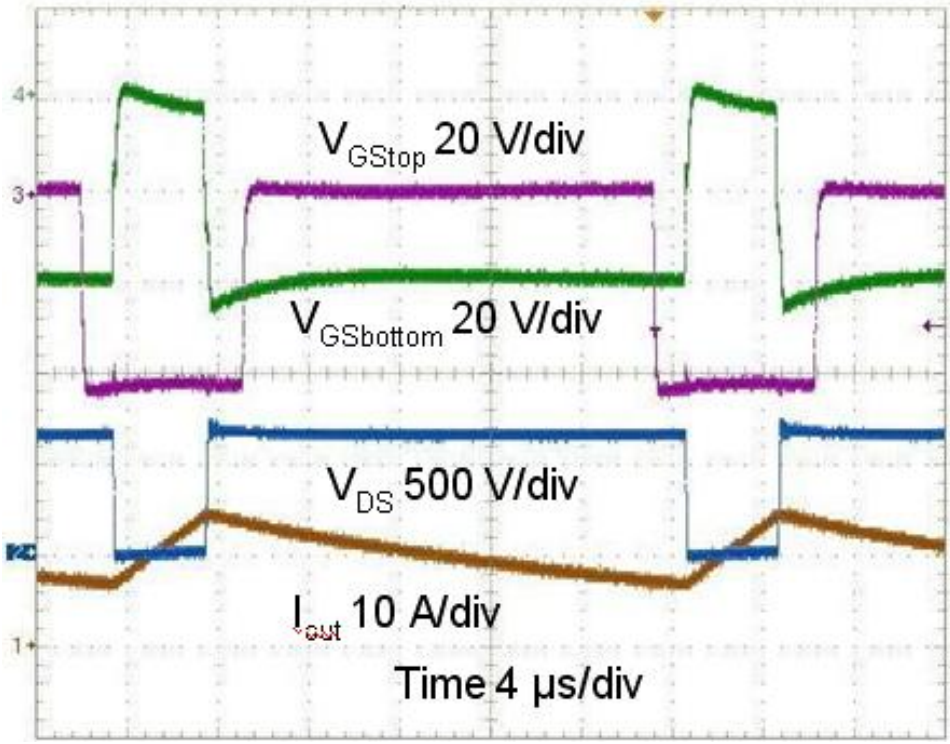

Figure 4-11. Test Results of phase leg module.

4.3.2 DC Bus Board

The dc bus board is the key interface for all the power components. The function is shown in Figure 4-12. As can be seen, the dc bus board includes the over current, over voltage protection, shoot-through protection and all the sensor circuits. And all of the phase leg modules, filter board and Nano controller are connected through dc bus board.

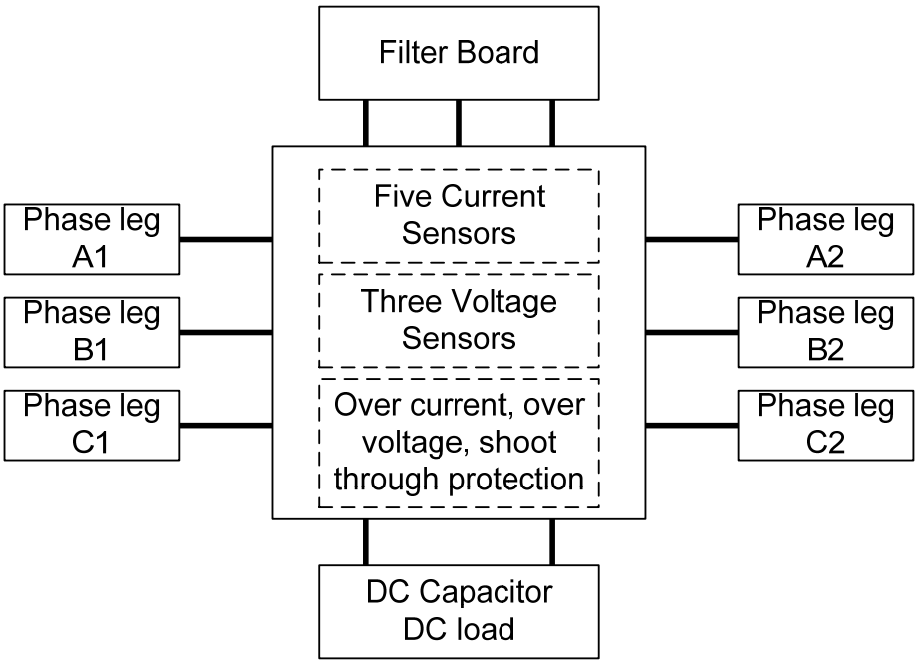

Figure 4-12. Diagram of the dc bus board.

The protection circuit proposed in [90] is borrowed and changed a little for shoot-through protection in this project, shown in Figure 4-13. The IGBT for the shoot-through detection is IRG4BC20SD from International Rectifier, which features a saturation current of 35 A at 10 V gate drive voltage. With the current level the JFET in the inverter phase leg should be safe even in a shoot-through condition if the fault only last for a short while.

In this design the dc-link capacitance is very small, therefore a film capacitor is utilized for energy storage instead of electrolytic capacitors in order to achieve better reliability and lifetime. The MKP series dc capacitors from EPCOS are selected with the rated value of 7 μF/1100 V. Three of them are connected in parallel to achieve 21 μF in total. In addition, some 10 nF/1000 V ceramic capacitors are also connected to the dc bus for decoupling purpose.

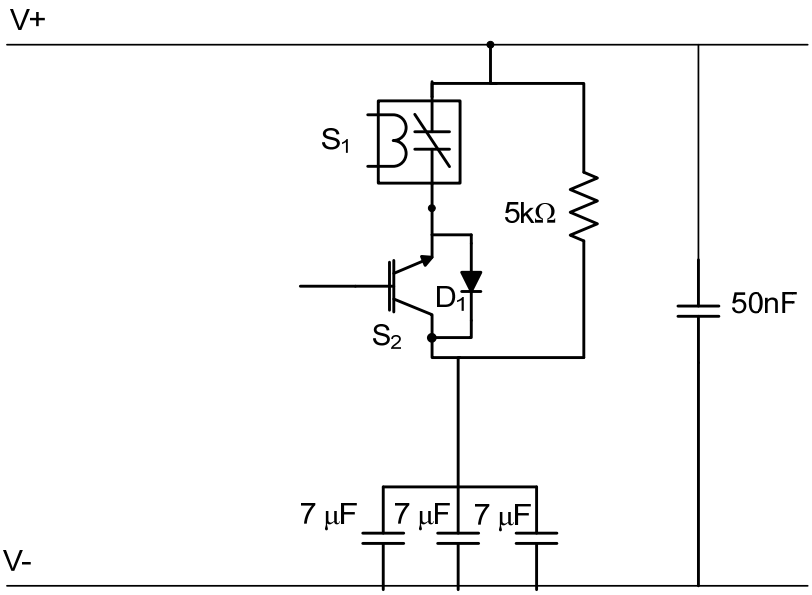

Figure 4-13. Circuit diagram of the dc bus including shoot through protection.

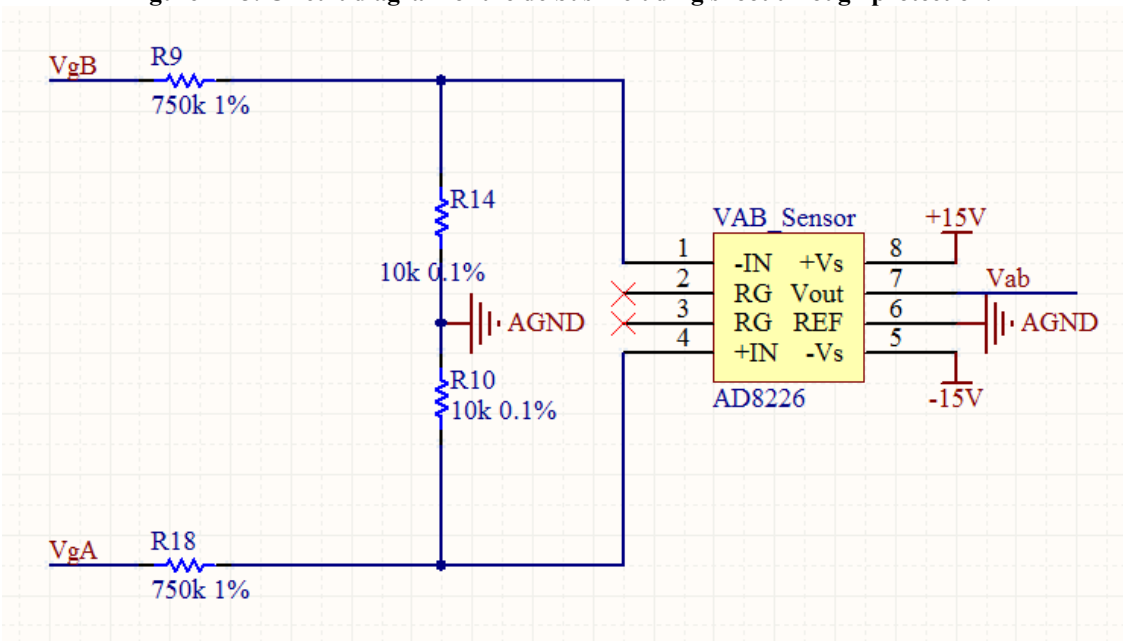

Figure 4-14. Voltage sensing circuit.

The dc bus board includes 8 sensing signals: 5 channels for currents, 2 for input voltage, and 1 for dc link voltage. Sensor HX 10-P from LEM Company is utilized for the current sensing. For the voltage measurement, non-isolated instrument amplifiers are

utilized to achieve low profile and good performance. Figure 4-14 shows the measurement circuit for inverter output voltage V_{ab}.

To increase the system power density, the size of the dc bus board is limited to match the total size of phase-leg power modules. Since each power module is 4cm by 4cm and the dc bus board need to connect to 6 power modules and dc bus capacitor, the board size is limited to 12 cm by 12cm, with some space for DC capacitor. To achieve that, small footprints are selected for all chips on dc bus board. For all of the chip resistors and capacitor except limited by creepage distance, 0603 footprint is used. For all ICs, the distance between adjacent two pins is 0.5mm.

The PCB layout of the dc bus board is shown in Figure 4-15. Since the board is sitting just above the power stage, the bottom layer is used as a shielding connected directly to earth ground, with all components only placed on the top layer. Also to reduce the impact of power stage on low voltage signal circuits such as protection circuit, mainly from the chopped dc side ripple current, there is no overlap between power stage dc bus and low voltage signal circuits on the dc bus board. As shown in Figure 4-15, only the area highlighted by dashed frame is connected to power stage. The picture of the dc bus board is shown in Figure 4-16.

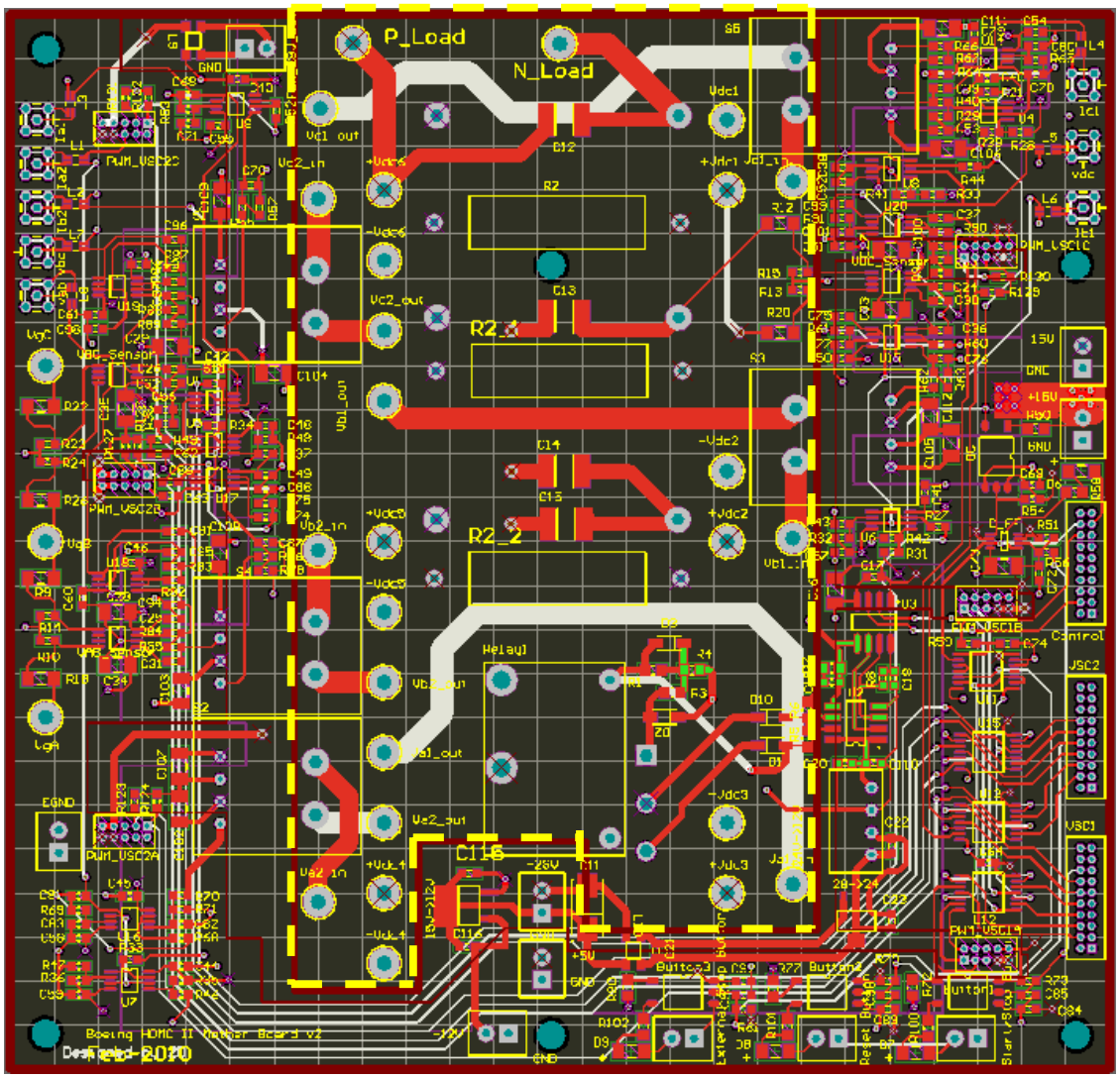

Figure 4-15. PCB layout of the dc bus board.

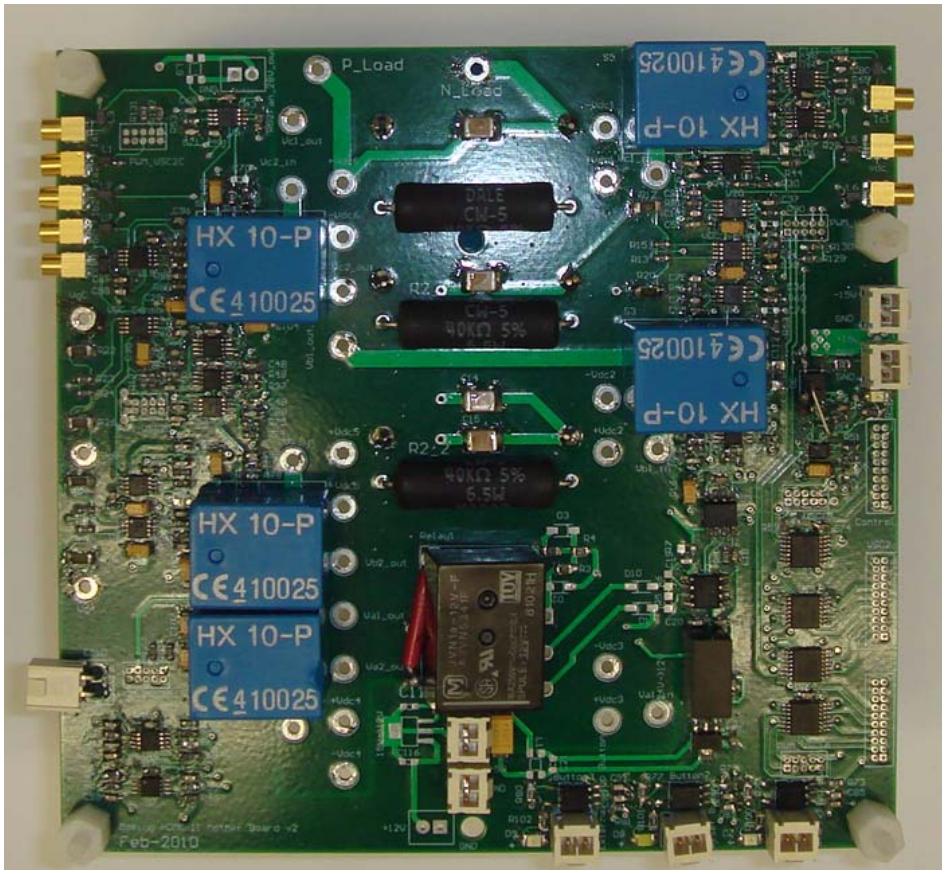

Figure 4-16. Picture of dc bus board.

4.3.3 Input Filter

The structure of three stage EMI filter is shown in Figure 4-17. The parameters of the passive components in each stage are also marked.

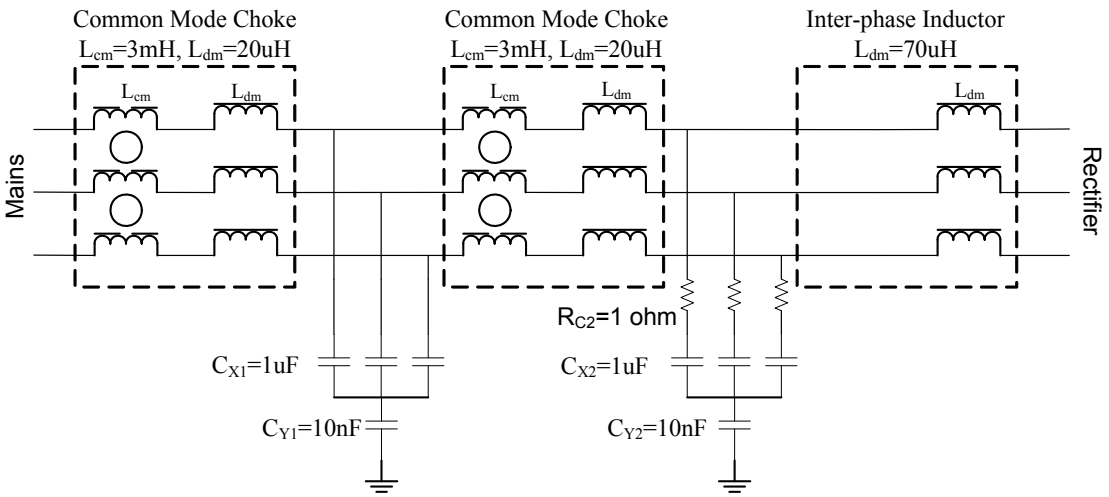

Figure 4-17. Structure and parameters of EMI filter.

From chapter 2, with optimized interleaving angle, the EMI filter needs to provide 53 db at 210kHz. Considering 14 dB margin and the ripple current limit in the first stage inductor, finally the three stage inductors are designed to be 70μH, 20 μH and 20 μH. The DM capacitor is 1.36uF and CM capacitor is 3.3nF each. To limit the resonant phenomenon, 1Ω resistors are connected in series with the first stage DM capacitors. The bode plot of the designed EMI filter is shown in Figure 4-18. From Figure 4-18, the required attenuation can be achieved.

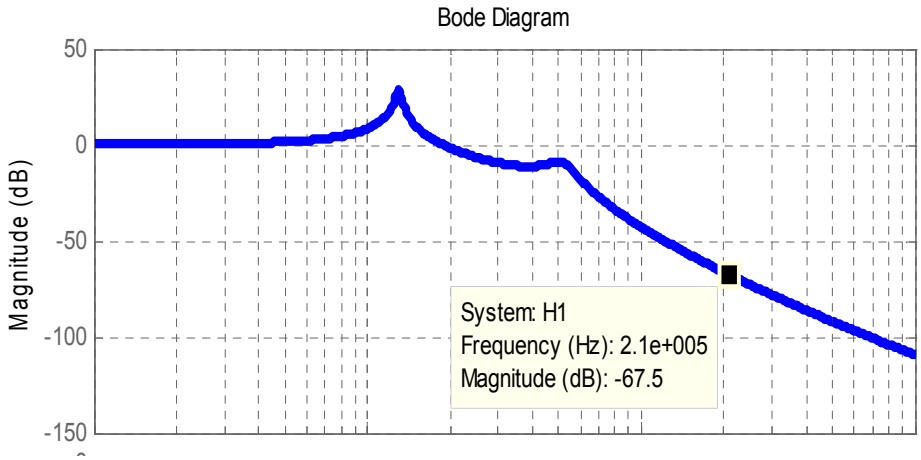

Figure 4-18. Bode plot of the designed EMI filter attenuation.

To build the first stage inductor, the two integrated inter-phase inductor structure based on CC core shown in Figure 3-5 and EE core shown in Figure 3-7 are both investigated and designed. Nano crystal material is used due to their high flux, high permeability and high temperature characteristics. The physical design results for both CC core and EE core based integrated inter-phase inductor are listed and compared in Table 4-2. Since Nano crystal core cannot be ordered with customized EE shape, two CC core are designed which together can act as one EE core as shown in Figure 4-19. And for each CC core the names of the dimension are listed as shown in Figure 4-20.

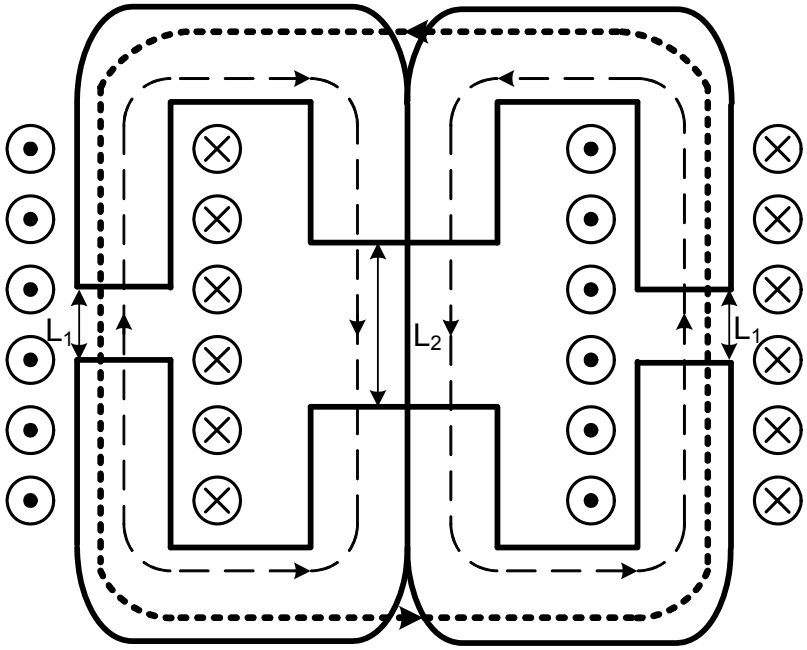

Figure 4-19. EE core realized by two CC core.

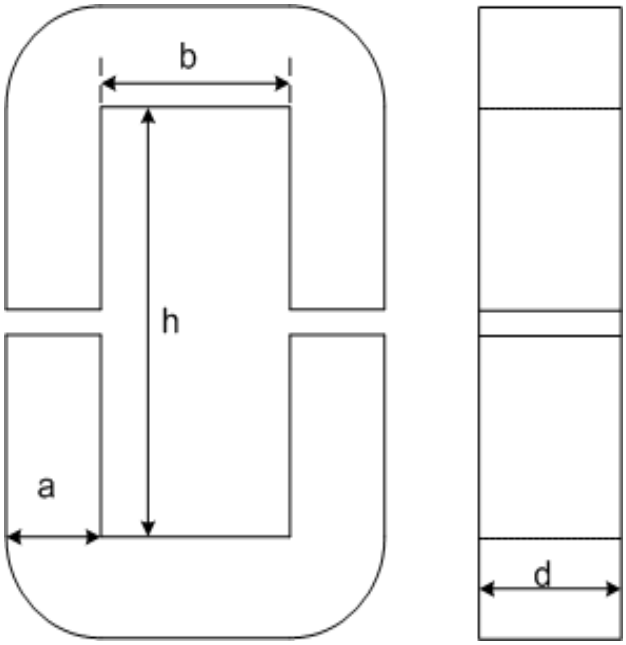

Figure 4-20. Name of dimensions for CC core.

Table 4-2 Design Results for the First Stage Inductor

	CC core	EE core
a	7mm	5mm
b	12mm	4mm
h	18mm	30mm
d	18mm	15mm
Turns Number	32	45
Core Weight	82g	Two 48g
Wire Weight	37g	Two 17g
Total Weight	119g	130g
Temperature Rise	120°C	139°C

In the inductor design, the leakage inductance is calculated as in [86]. And the thermal rise is estimated as in [91].

From Table 4-2, the EE core design is less than 10% heavier than CC core design. Considering the EMI issue with CC core and possible mismatch between designed and real leakage inductance, the design based on EE core is finally selected. The picture of one integrated inter-phase inductor is shown in Figure 4-21.

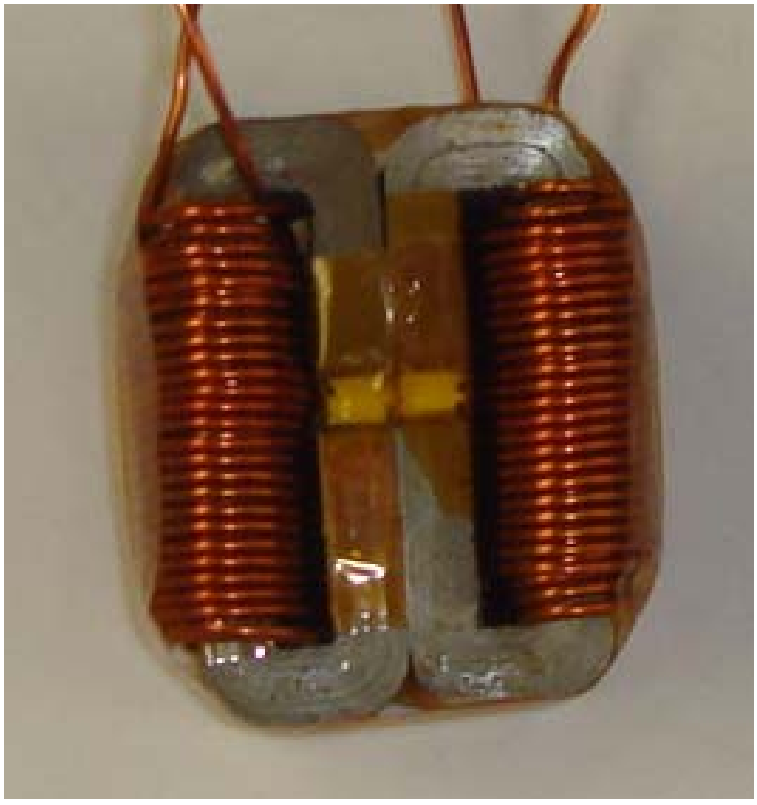

Figure 4-21. Picture of EE core based integrated inter-phase inductor.

And for the second stage inductor, toroid core is used. The leakage inductance is used as boost inductor and the main inductance is used as CM choke. [91] The design results are summarized in Table 4-3.

Table 4-3 Physical Parameters for the CM Choke

Outer Diameter	Inner Diameter	Height	Number of Turns	Weight	Temperature Rise
5.6 cm	4.4 cm	0.8 cm	20	86g	96°C

In the design, reduce the effect of EPC at high frequency range, single layer design is used. And picture of second stage inductor is shown in Figure 4-22.

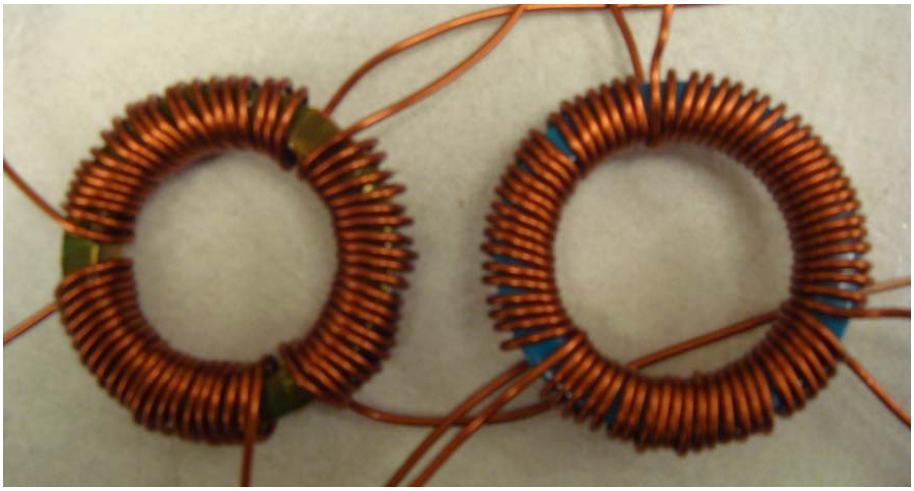

Figure 4-22. Picture of Toroid core based second and third stage inductors.

For the DM and CM capacitor, MKP series from EPCOS is selected.

Limited by the space in the system, the size of each filter board is limited to 6 cm by 12 cm. So the filters are mounted on two boards, as shown in Figure 4-23.

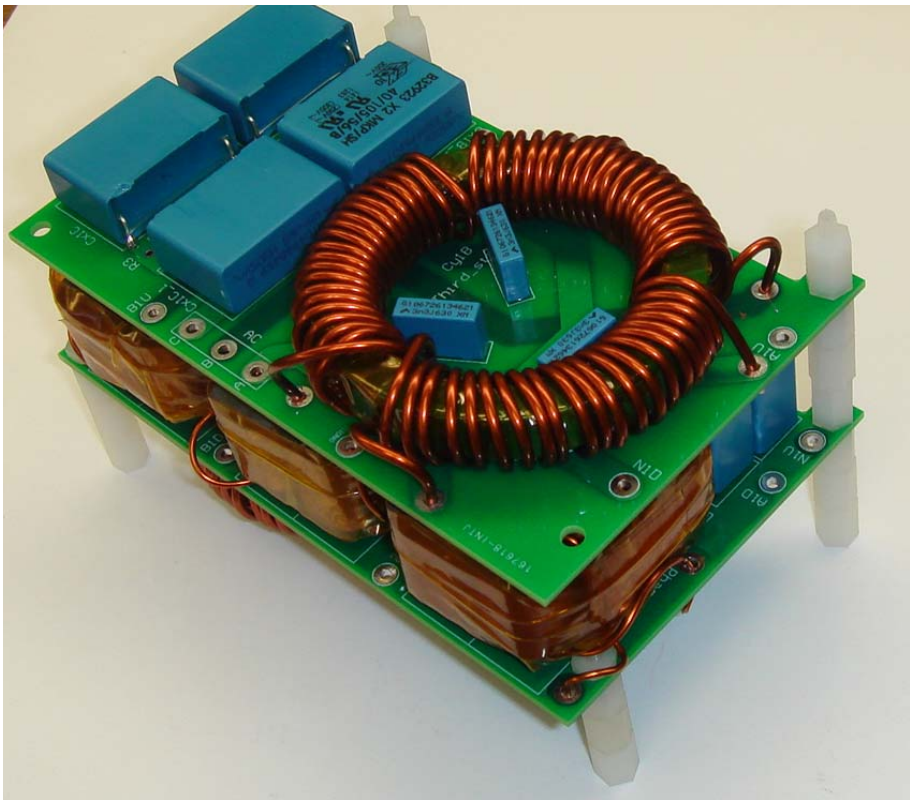

Figure 4-23. Picture of EMI filter boards.

As shown in Figure 4-23 the second and third stage inductors are place as far as possible to reduce the coupling and one layer in the filter boards are also connected directly to earth ground to provide shielding.

4.4 System Assembly and Weight Distribution

Finally the whole system is assembled as shown in Figure 4-24.

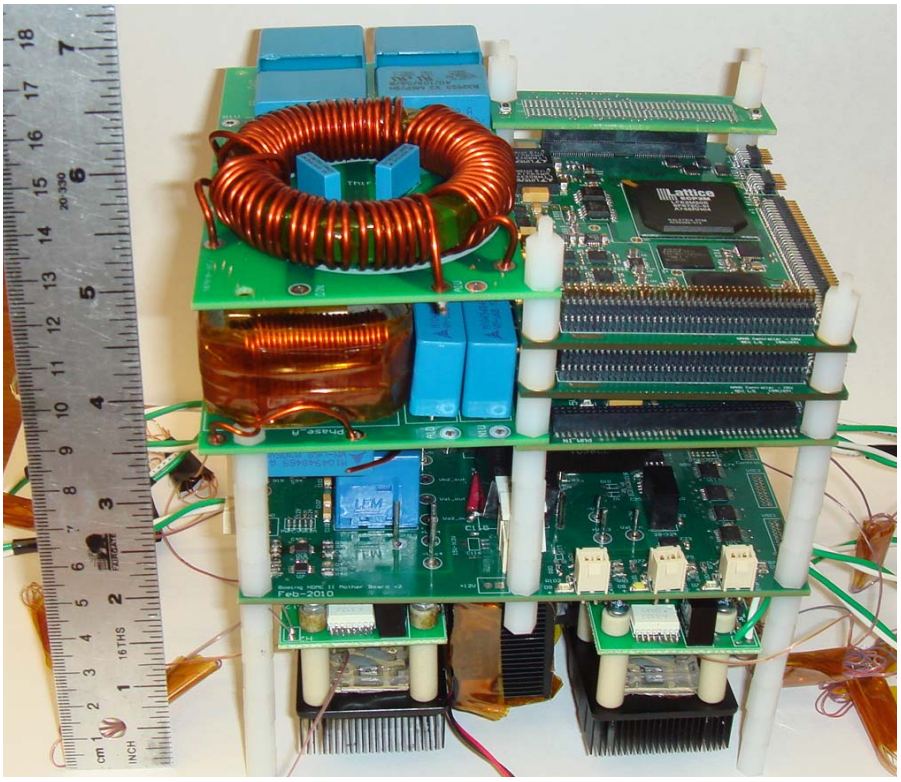

Figure 4-24. Picture of the whole rectifier hardware.

The size of the whole system is 2366cm^3. And the total weight is 2.45kg. Since the power rating of the converter is 15kW, the power density is 6.3kW/l and the specific power density is 2.78kW/lb.

The weight distribution in the system is listed in Table 4-4. In Table 4-4, the power weight of the power modules has included the weight of gate drive boards. And the

weight of the housing is estimated by the 3mm thickness aluminum box with the same volume as the rectifier.

Table 4-4 Weight Distribution in High Power Density Rectifier System

Power Modules (Devices + Heatsink)	Fan	DC Bus Board	Shoot-through Protection	EMI Filter				Nano Controller	Housing
				PCB Boards	L1	L2 and L3	Caps		
42.7g ×6	166g	217g	36g	49g	126g ×3	109g×2	70g	225g	850g

4.5 Simulation Verification

Since the rectifier power stage is still under test, only the simulation results are provided here to verify the function of designed rectifier.

The simulation results from start-up to steady state are shown in Figure 4-25. From Figure 4-25, it can be seen that the function of the converter have been realized. With the load step change from 1/3 load to 2/3 load and further to full load, the system can always operate stably and the system is always symmetric.

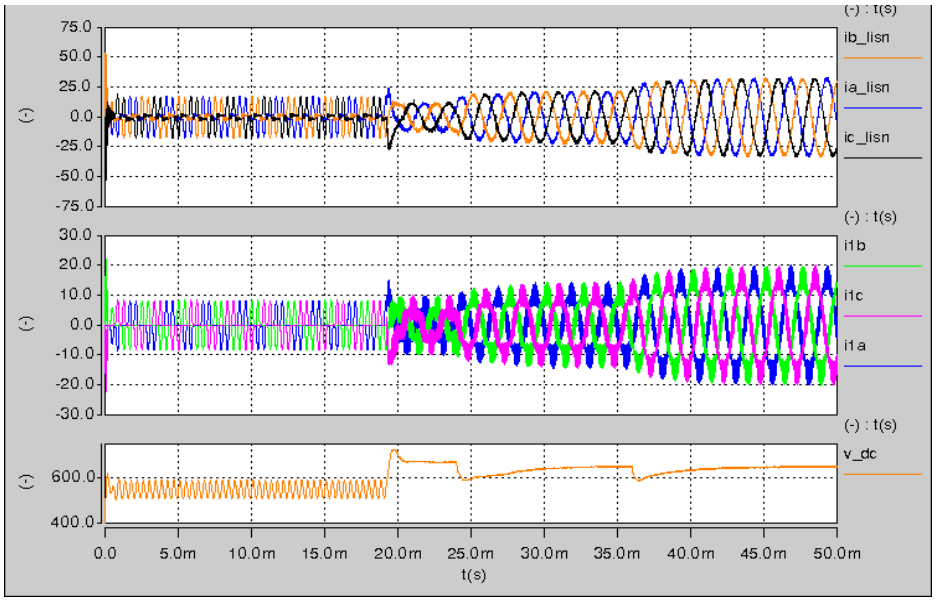

Figure 4-25. Simulation Results from Start-up to Steady State.

The performance of EMI filter is also verified by simulation. The spectrum of output current without interleaving and with optimized interleaving are shown in Figure 4-26 and Figure 4-27. In Figure 4-26 and Figure 4-27, the red line is the EMI standard.

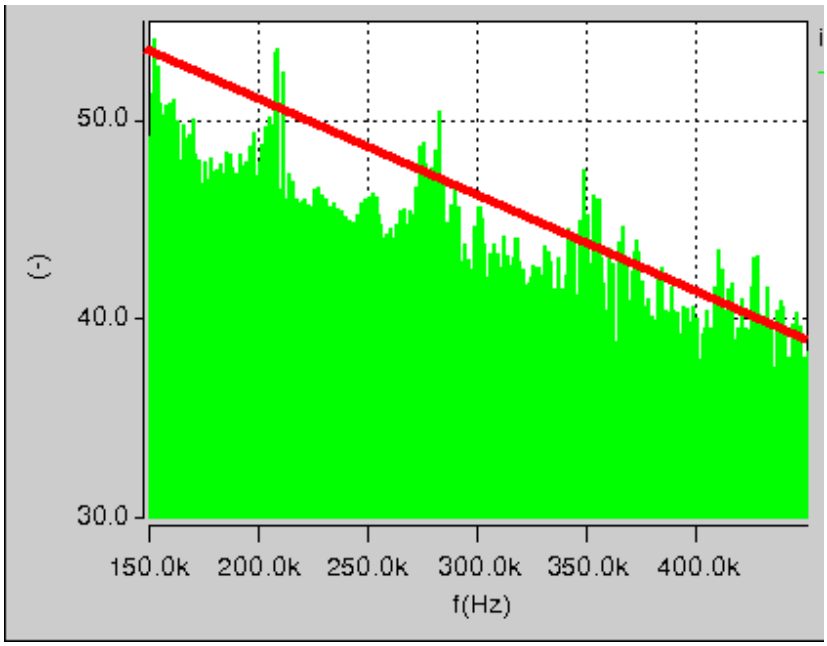

Figure 4-26. Spectrum of output current without interleaving.

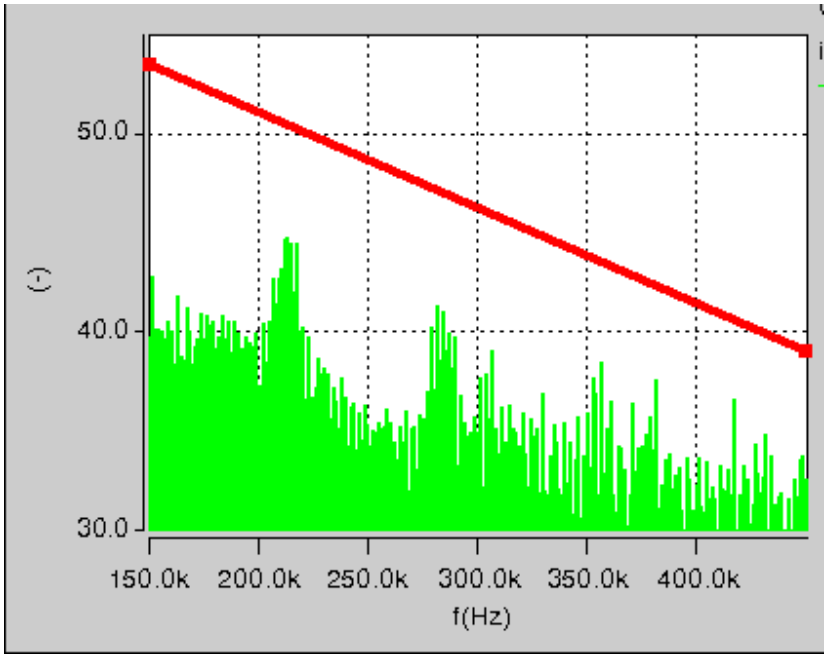

Figure 4-27. Spectrum of output current with optimized interleaving.

By comparing the simulation results in Figure 4-26 and Figure 4-27, the design of EMI filter can meet the EMI standard with optimized interleaving.

4.6 Summary

This chapter presents the hardware development for a 15 kW three-phase ac-dc rectifier with the merit of high specific power density.

First, system configuration and interface are presented. After that, the controller architecture and the hardware design are described in detail including the functions of main boards and main chips. Also the power stage design and construction are introduced including phase leg module, dc bus board input filters. Based on that, the system assembly and weight distribution are summarized. Simulation in Saber is used to verify the function of the designed high specific power density rectifier.

Chapter 5 Converter System with Low Switching Frequency

This chapter mainly focuses on the converter system with low carrier ratio (defined as the ratio between switching frequency and fundamental frequency). The analysis and conclusions are useful for very high power converter application, where system switching frequency cannot be high or very high speed motor drive, where the switching frequency is relatively low compared with the fundamental frequency.

First the special issues when switching frequency is low are analyzed. Based on the analysis, the beat phenomenon is explained and the method to avoid the beat phenomenon in system is presented. Also the method to eliminate system unbalance for non-triplen carrier ratio is proposed.

After that, this chapter also presents an improved asymmetric space vector modulation (ASVM) for two level VSCs when the switching frequency is only 9 times of fundamental frequency. By adding two pulses in each line cycle when the fundamental voltage crosses zero, the total harmonic distortion (THD) of output current can be reduced significantly. The penalty of additional switching loss is very limited especially for high power factor system. With optimization, the ac output current THD can be reduced to as low as 50% for single VSC and even lower to 20% for interleaved VSCs systems. Such THD reduction has close relationship with space vectors position, modulation index and interleaving angle. In addition, improved ASVM can also reduce the amplitude of circulating current which mainly determines the size of inter-phase inductors. Finally, the weights of total inductors needed to meet the same THD requirement are compared to demonstrate the benefits of improved ASVM when different

PWM schemes are used. The analysis results are verified by experiments on a demo system.

5.1 Introduction

Very low carrier ratios, such as less than 15 are usually adopted in the applications with very high power requirement where the performance of high voltage high current devices limits the switching frequency or with very high fundamental frequency such as high speed motor drive where the switching frequency is relatively low compared with the fundamental frequency. Especially, for applications involving high speed generator or motor, carrier ratio will be extremely low such as around 9. In many cases, even if the devices can operate at higher switching frequency, it is also desirable to use lower switching frequency, in order to reduce loss and increase power capability. However, since usually it is very difficult, if not impossible, to build one converter to handle the total huge power, paralleling operation even makes more sense in such applications. It is really meaningful to apply interleaving technique to those applications.

In the analysis in previous chapters, a basic assumption is the carrier ratio is high enough. When the carrier ratio is really low, several issues will appear. Such as the overlap between sidebands and difference between regular sampled PWM and naturally sampled PWM. Because of the overlap between sidebands, some phenomenon can be observed such as the beat and system unbalance, which may decrease the system performance.

In this area, some study showed that the minimum ratio between switching frequency and fundamental frequency to avoid beat is 15–20. [64] And synchronization PWM is necessary to eliminate beat when switching frequency is less than 15 times fundamental

frequency. [65] In addition, the patterns of synchronization PWM can affect the final output voltage. [66] Even for the selection of switching frequency, there is argument. It is usually considered necessary to keep the ratio between switching frequency to be triplen [67][68], but Ref. [69] claims it is not necessary. There is still no very clear explanation of such phenomenon. In this chapter, these problems will be studied and explained. Based on that, the solutions are also proposed.

The difference between regular sampled PWM and naturally sampled PWM has been mentioned in [69]. When the carrier ratio is really low such as less than 11, such difference will very obvious. This issue will be studied in detail in the future.

After that, Asymmetric space vector modulation (ASVM) is proposed, which can significantly reduce the THD of system currents.

Asymmetric space vector modulation (ASVM) is a popular pulse-width modulation (PWM) scheme used for VSCs operated with low carrier ratio (R_{fs}). When R_{fs} is very low, ASVM, compared with symmetric SVM, has many benefits such as keeping the PWM waveforms symmetric in a line cycle, avoiding even order harmonic currents and reducing the total harmonic distortion (THD) of output current. **Error! Reference source not found.**

Low carrier ratio results in higher harmonic currents. To limit current harmonics, large ac line inductors are generally necessary with the expense of higher cost and size. Therefore, it is very desirable to improve the ASVM algorithm for better harmonic performance, so smaller or lighter passive components can be used to meet the THD requirement for ac currents.

Some papers have studied the performance of PWM with low carrier ratio. Ref. [70] and [71] compared four kinds of space vector modulations, including traditional asymmetric space vector modulation. Ref. [72] also investigated the synchronized space vector modulation for active front-end rectifiers in high-power current-source drive. However, these studies mainly focused on the impact of space vectors sequence on the performance of space vector modulation and the harmonic current performance of these space vector modulations are very similar. Ref. [73] [74] [75] proposed methods to optimize the harmonic performance of converters under space vector modulation control. But these methods cannot be used directly to the system with very low carrier ratio. In addition, how to maximize the current THD reduction in a paralleled VSCs system with interleaving and ASVM is still unknown.

This chapter presents a method to improve the harmonic current performance of traditional ASVM which can reduce the output current THD significantly both for single VSC and paralleled VSCs system with interleaving. The corresponding penalty is very limited especially for high power factor system. In addition, the system circulating current in paralleled VSCs system can also be reduced, which can help further reduce system passive components weight.

5.2 Converter System Issues with Low Switching Frequency

5.2.1 Overlap of Sideband Harmonic Components

Overlap between harmonic component sidebands is an issue related to a very low carrier ratio. When the carrier ratio is very low, the sidebands related to each order of the switching frequency harmonics will overlap each other. Figure 5-1 shows the double integral Fourier analysis results for an asymmetrical SVM when the carrier ratio is 9. The

blue, red, green, yellow and black lines represent the baseband and sidebands for up to the 4th order of switching frequency harmonics.

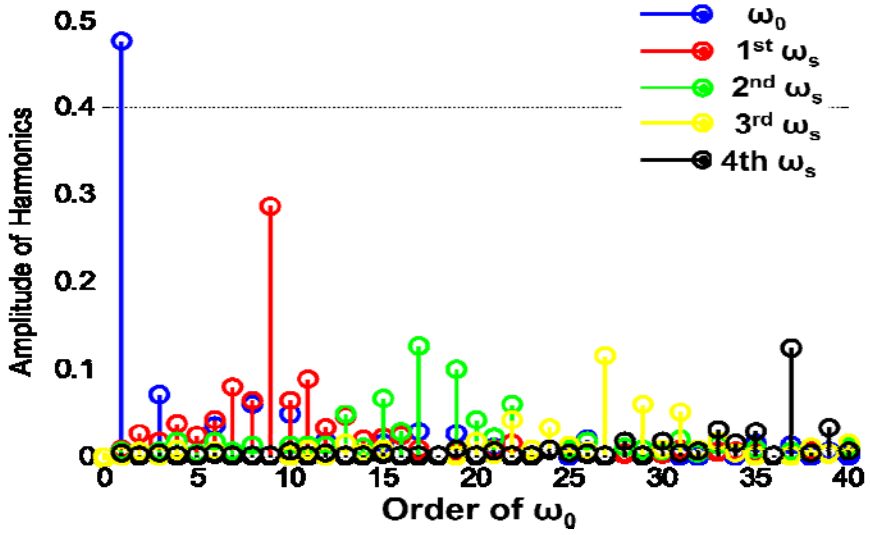

Figure 5-1. Sidebands of up to 4th order switching frequency harmonics.

From Figure 5-1, it is easy to see that, each harmonic component will be determined by many sidebands because of the overlap. As a result, interleaving cannot eliminate the harmonic at a certain frequency, since the impacts of interleaving on harmonics related to a different order of switching frequency are different.

An even more serious problem is that the final amplitude at a fundamental frequency is not only determined by the amplitude of the fundamental component, but also affected by some of the switching frequency's harmonic sidebands at fundamental frequency. This will cause a beat phenomenon and system unbalance which will be discussed later in this section.

5.2.2 Beat Phenomenon

The term beat phenomenon means that the system has a low frequency oscillation, which can affect the control performance of the whole system. As reported in [64], beat

phenomenon can be avoided when carrier ratio is at least 15-20 or the synchronized PWM is used. The reason why these conditions should be met to avoid beat has not been fully explained well.

The key point when explaining beat phenomenon is the effect of harmonic voltage sidebands at fundamental frequency (f_0). This effect is not negligible when R_{fs} is low and regular-sampled PWM (or asymmetrical space vector PWM - ASVM) is used as assumed in the paper.

To explain this effect, first take a two-level voltage source converter as an example with ASVM, a carrier ratio (R_{fs}) of 7 and modulation index (M) of 0.9. Assuming the first vector is located at 0° on the space vector diagram, the PWM waveforms and the corresponding spectrum are shown in Figure 5-2 and Figure 5-3. From Figure 5-3 the fundamental component amplitude is 0.5089 based on the dc link voltage of unity. When the first vector is moved from 0° to 10°, the PWM waveforms and the corresponding spectrum are shown in Figure 5-4 and Figure 5-5, where the fundamental component amplitude changes to 0.5203. This shows that the positions of the vector can affect the amplitude of the fundamental component, even with the same reference fundamental voltage.

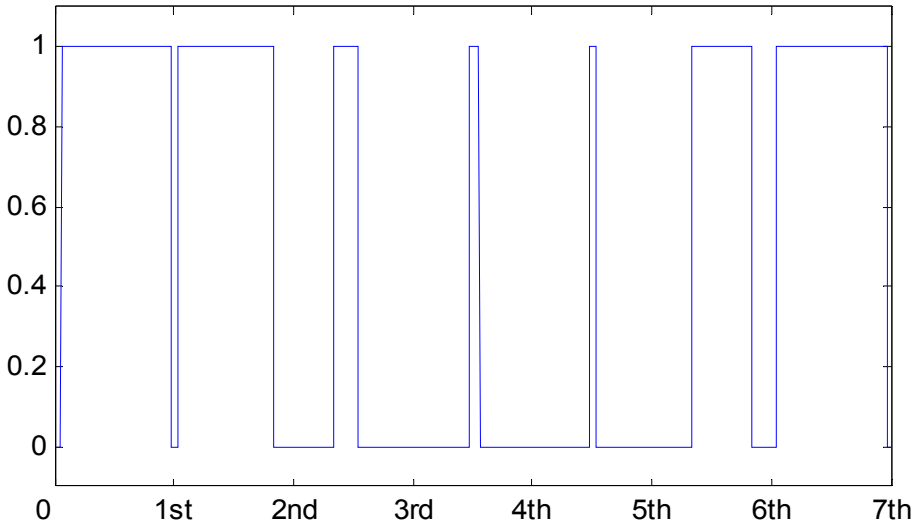

Figure 5-2. Time domain PWM waveforms of ASVM when R_{fs} = 7 , M=0.9 and the first vector is at 0°

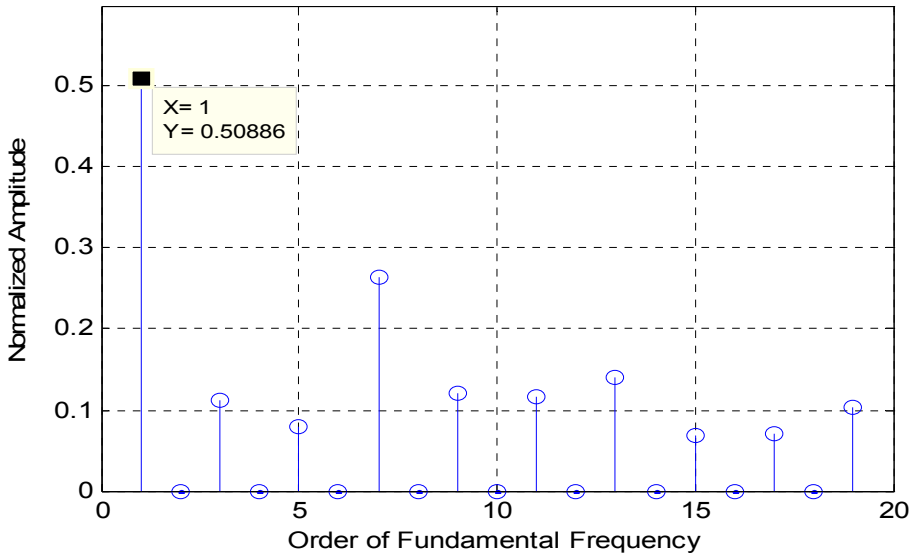

Figure 5-3. Spectra of PWM waveforms of ASVM when R_{fs} = 7 , M=0.9 and the first vector is at 0°

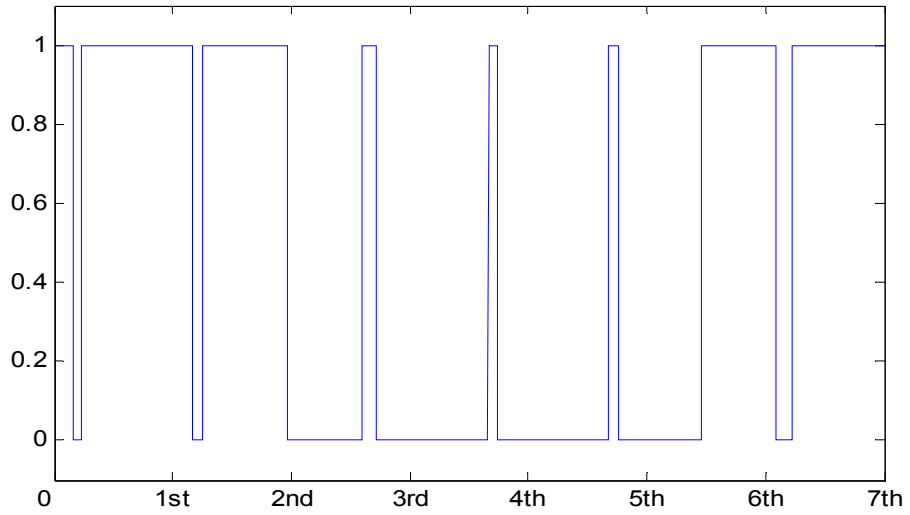

Figure 5-4. Time domain waveforms of ASVM when R_{fs} = 7 , M=0.9 and the first vector is at 10°.

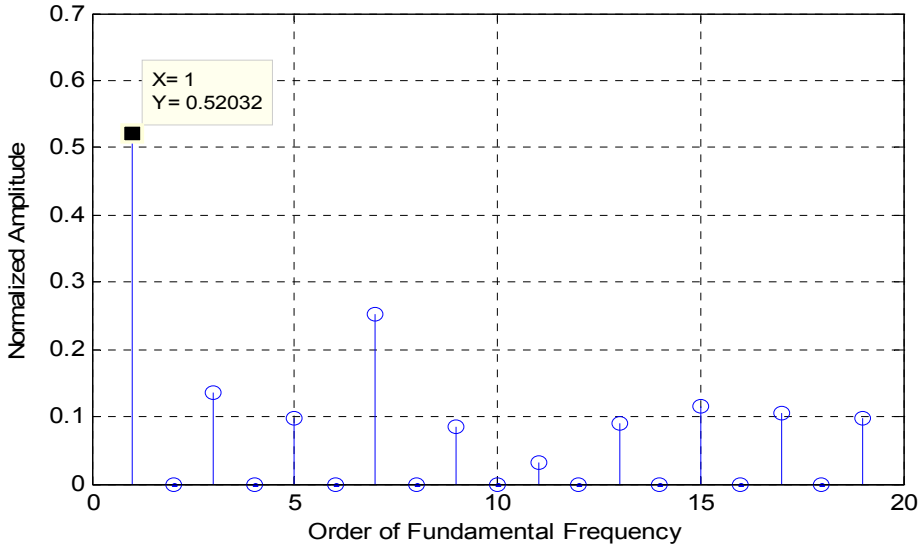

Figure 5-5. Spectra of PWM waveforms of ASVM when R_{fs} = 7 , M=0.9 and the first vector is at 0°

The above observation is explained more clearly by the double integral Fourier analysis results in Figure 5-6, where the sidebands of the fundamental components and up to the 3rd order of switching frequency harmonics are shown. From here we can see that the final amplitude at f_0 is not only determined by the amplitude of the fundamental

component, but is also affected by some of the switching frequency harmonic sidebands at f_0.

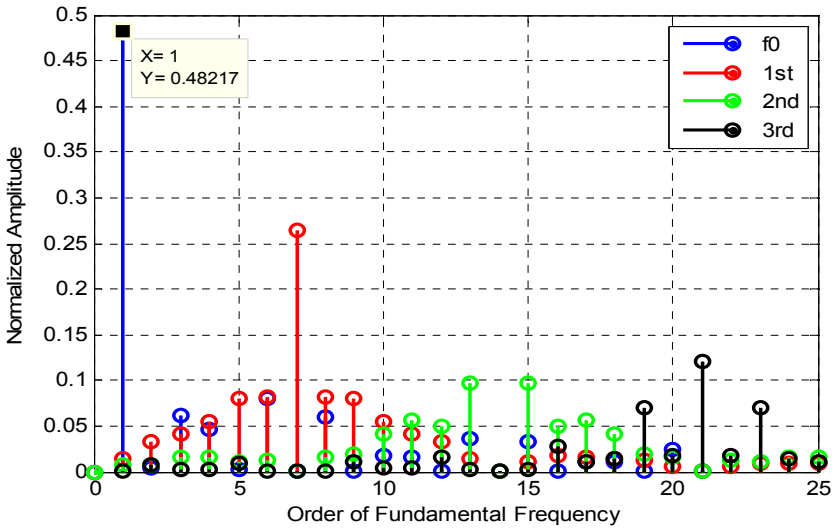

Figure 5-6. Double integral Fourier analysis results of ASVM when R_{fs} = 7 and M=0.9.

A relevant point that will help is the relationship between the space vector PWM and its equivalent carrier-based PWM. Based on the characteristic of space vector PWM, the vector positions determine the relative phase angles between the reference waveform and the equivalent carrier waveforms. If the positions of the vectors are changed, the equivalent carriers are phase-shifted, for the same reference waveform. The relative phase-angle between the reference waveform and the carrier waveforms also determine the sidebands of switching frequency harmonics, as the vector positions in the case of the space vector PWM.

If the carrier ratio is not a constant integer because of the grid-frequency variation or some other reasons, the vectors will not repeat on the space vector diagram every line cycle, which means the switching harmonic components are phase shifted. Based on the above discussion, the amplitude of the fundamental components will be affected. If the positions of the vectors are changed continuously, beat phenomenon can be observed.

This analysis is also valid for other types of voltage source converters.

For a three-level converter, the relationship between the modulation index (determined by the resultant amplitude of the fundamental components) and the position of the first vector is shown in Figure 5-9. In calculating this relationship, M is set to be 0.86 and *no* closed-loop control is used. When moving of the first vector, the real modulation index can beat between 0.85 and 0.865. The result matches well with the experimental result in [66].

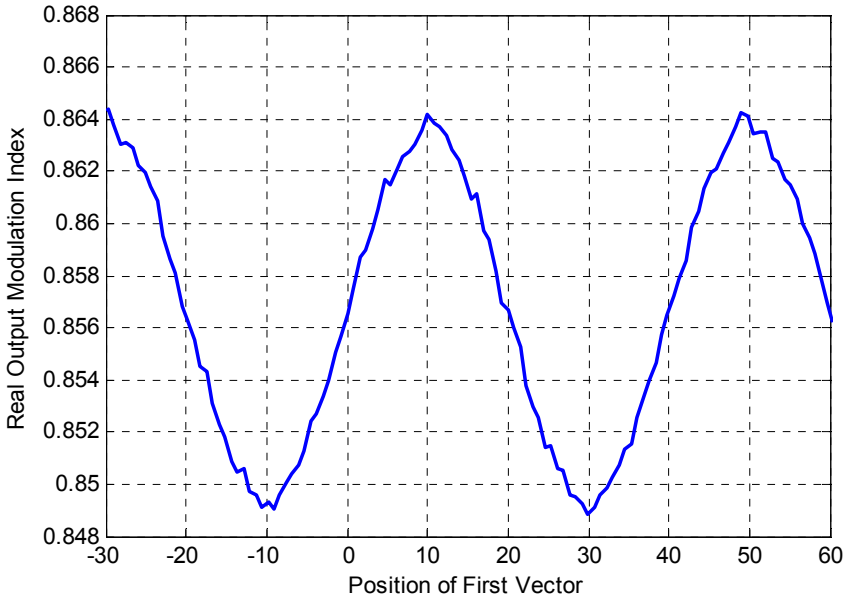

Figure 5-7. Relationship between the output modulation index and the position of first vector for ASVM in a three-level VSC when R_{fs} = 9 and M=0.86.

With synchronized PWM, the positions of the output vectors are fixed, thus eliminating the beat phenomenon, as claimed in [65]. However, the relative angle between the harmonic sideband at f_0 and the fundamental component can affect the final amplitude at f_0. The positions of the vectors can also affect the amplitude of the final output fundamental voltage which is also observed in [66].

5.2.3 System Unbalance with Non-triplen Carrier Ratio

When synchronized PWM is used, the carrier ratio is an integer and the positions of the output vectors are fixed. It is usually believed that a triplen carrier ratio is desired. As claimed in [66], when the carrier ratio is low, only the triplen carrier ratio can keep the system balance. This section proves it in a mathematical. However, when power is really high, sometimes a non-triplen carrier is the only choice such as 7. The method to avoid system unbalance is proposed and the penalty for using such method is also presented.

Take a two level voltage source converter for example. The harmonic voltages of line to line voltages V_{ab} and V_{bc} are expressed as [81]:

$$V_{ab}(t)=\frac{4V_{dc}}{\pi}\sum_{m=0}^{\infty}\sum_{\substack{n=1(m=0)\\ n=-\infty(m>0)}}^{\infty}\frac{1}{q}J_n\left(q\frac{\pi}{2}M\right)\sin\left(\left[m+n\right]\frac{\pi}{2}\right)\times\sin\left(n\frac{\pi}{3}\right)\cos\left(m\omega_c t+n\left[\omega_0 t-\frac{\pi}{3}\right]+\frac{\pi}{2}\right) \tag{5-1}$$

$$V_{bc}(t)=\frac{4V_{dc}}{\pi}\sum_{m=0}^{\infty}\sum_{\substack{n=1(m=0)\\ n=-\infty(m>0)}}^{\infty}\frac{1}{q}J_n\left(q\frac{\pi}{2}M\right)\sin\left(\left[m+n\right]\frac{\pi}{2}\right)\times\sin\left(n\frac{\pi}{3}\right)\cos\left(m\omega_c t+n\left[\omega_0 t-\pi\right]+\frac{\pi}{2}\right) \tag{5-2}$$

For the fundamental component in V_{ab}, the phase angle of $V_{ab}(0,1)$ is $\frac{1}{6}\pi$.

The sideband component around the first order switching frequency when $m=1$ and $n=-(\frac{\omega_{sw}}{\omega_0}-1)$ has the same frequency as fundamental components (f_0). The phase angles of those harmonic components are $\frac{1}{6}\pi+m\frac{R_{fs}}{3}\pi$.

So the relative phase angle between the fundamental component and the harmonic components at f_0 in V_{ab} are expressed as:

$$\Delta\theta_{Vab} = m\frac{R_{fs}}{3}\pi \tag{5-3}$$

For V_{bc}, in a similar way, the relative phase angle between the fundamental component and the harmonic components at f_0 in V_{bc} are expressed as:

$$\Delta\theta_{Vbc} = mR_{fs}\pi \tag{5-4}$$

Comparing (5-3) and (5-4), only when R_{fs} is triplen, the relative phase angle between the fundamental component and the harmonic components at f_0 for V_{ab} and V_{bc} is the same. In other words, the effects of the harmonic sidebands on the fundamental components are the same, so the system three phases can be balanced.

When the carrier ratio is not triplen, the system three phases will not be balanced with the effects of harmonic components. Take a system with a carrier ratio 7 for example. The positions of the output vector for ASVM when the carrier ratio is 7 are shown in Figure 5-8 and the corresponding three phase PWM waveforms are shown in Figure 5-9. From Figure 5-9, the three phase PWM waveforms are unbalanced. The spectrum of the three phase voltages are shown in Figure 5-10. From Figure 5-10 the amplitude of the fundamental components in three phases are not the same.

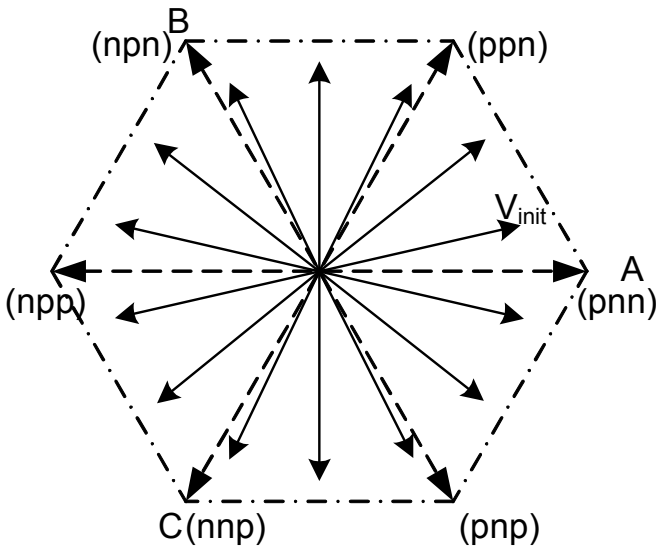

Figure 5-8. Output vectors of ASVM (R_{fs}=7)

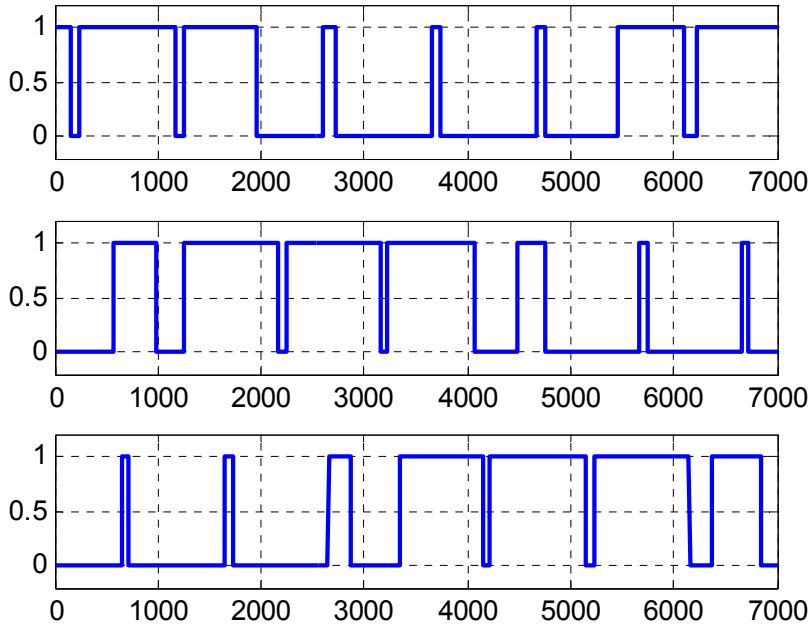

Figure 5-9. Three phase PWM waveforms for ASVM (R_{fs}=7).

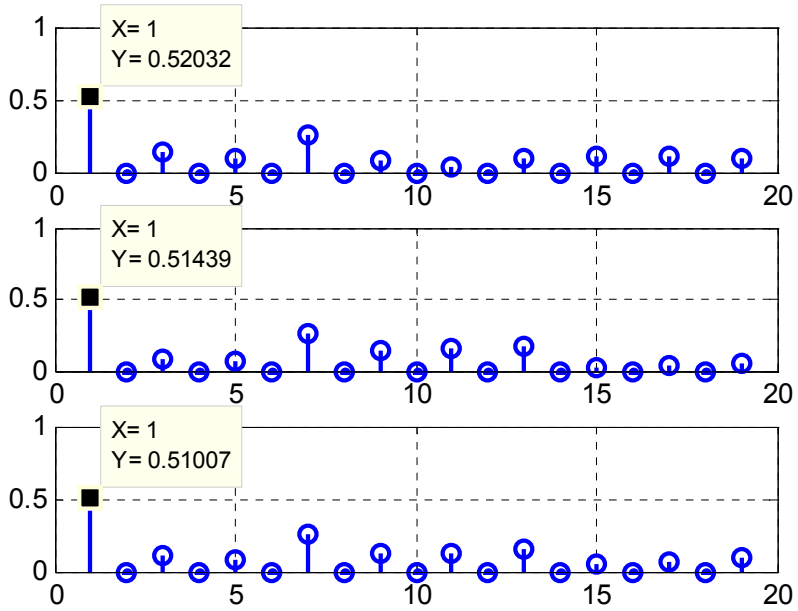

Figure 5-10. Spectra of three phase voltage for ASVM (kc=7).

Even though the system is only slightly out of unbalance, it is still desirable to correct it. This can be done by inter-phase interleaving.

As mentioned above, the sideband component around the first order switching frequency when $m=1$ and $n=-(\frac{\omega_{sw}}{\omega_0}-1)$ has the same frequency as the fundamental components. Assuming the angle of $V_a(0,1)$ is 0 and $V_a\ (1,\ -(\frac{\omega_{sw}}{\omega_0}-1))$ is β, then the relative angle between the fundamental and the harmonic components for phase A is β.

For V_b, if R_{fs} is 3k-1, then the angle for $V_b(1,0)$ is -2/3π and $V_b\ (1,\ -(\frac{\omega_{sw}}{\omega_0}-1))$ is β+(m R_{fs} -1) 2/3π, So the relative angles for phase B is θ+2k π –m(2/3π)

To make the two relative angles the same to keep the system balanced, the carrier waveform of V_b should be phase shifted by 2/3π which is 1/3 of switching cycle

Based on the same analysis, the carrier waveform of phase C should be phase-shifted -1/3 switching cycle.

By using this method, the carrier waveforms for phase A, B and C are phase shifted; it is called inter-phase interleaving. The method is similar to the carrier ratios which are 3k+1.

Take the system with the carrier ratio of 7 for example again. Based on the analysis, to keep the system balanced inter-phase interleaving is applied. Instead of using the same group output vectors, three phase-shifted group output vectors are used correspondingly for phase A, phase B and phase C, which are shown in Figure 5-11, Figure 5-12 and Figure 5-13. For example, to generate the PWM waveform of phase A, only the vectors in Figure 5-11 are used. The information in Figure 5-11, which is usually are usually used to generate the PWM waveforms of phase B and phase C, is neglected. It is the same story for phase B and phase C. Finally, the three phase time domain PWM waveforms are shown in Figure 5-16. With inter-phase interleaving, three phase PWM waveforms become symmetric, which can also be seen from the spectrum analysis results in Figure 5-15.

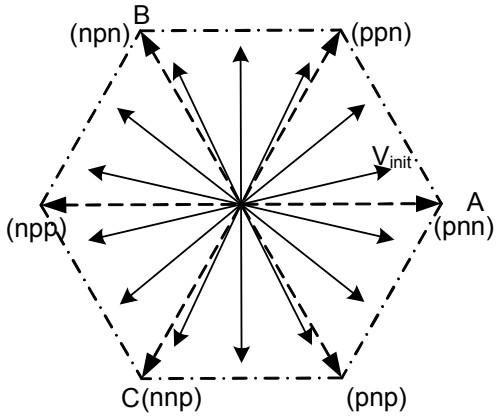

Figure 5-11. Output vectors of ASVM for phase A with inter-phase interleaving (R_{fs} =7).

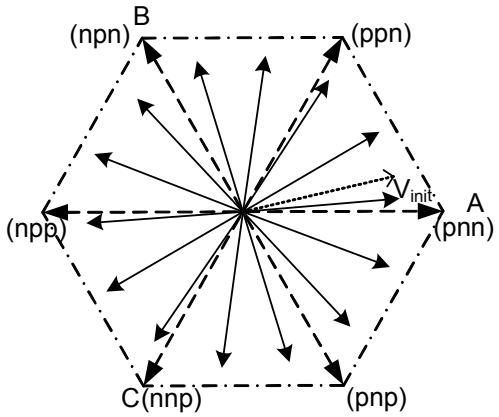

Figure 5-12. Output vectors of ASVM for phase B with inter-phase interleaving (R_{fs} =7).

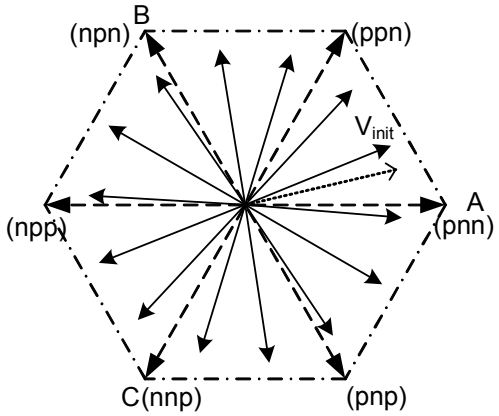

Figure 5-13. Output vectors of ASVM for phase C with inter-phase interleaving (R_{fs} =7).

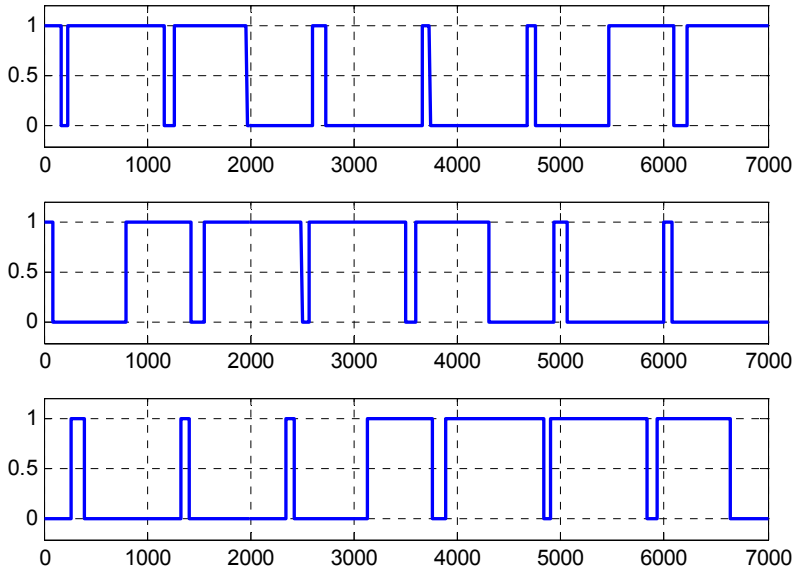

Figure 5-14. Three phase PWM waveforms for ASVM with inter-phase interleaving (R_{fs} =7).

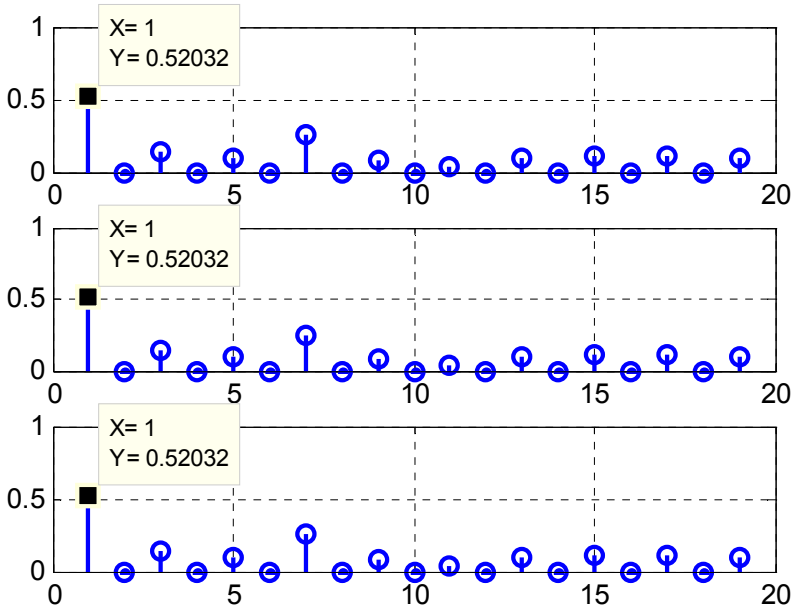

Figure 5-15. Spectra of three phase voltage for ASVM with inter-phase interleaving (kc=7).

Because of inter-phase interleaving, part of the DM harmonic components are changed into CM harmonic components and the original CM harmonic components are changed into DM harmonic components. This can be seen from the spectrum of DM and CM harmonic components with or without inter-phase interleaving.

Since the amplitude of the harmonic component at switching frequency is usually the highest which is CM harmonic component without inter-phase interleaving, the THD of harmonic currents after such a big harmonic component becomes a DM harmonic component.

To verify that, simulation is done and the results are shown in Figure 5-17 and Figure 5-18. In Figure 5-17 and Figure 5-18, the same simulation model is used. The only difference whether or not is inter-phase interleaving is applied. By comparing the simulation results in Figure 5-17 and Figure 5-18, the three phase current is not symmetric without inter-phase interleaving. However, the THD is increased from 35% to

74% by inter-phase interleaving, since the highest harmonic components are changed from CM to DM. Even though, lower CM harmonic components also offer benefit for the CM filter design, a trade-off may still be necessary for a real project. In addition, more study will be done in the future.

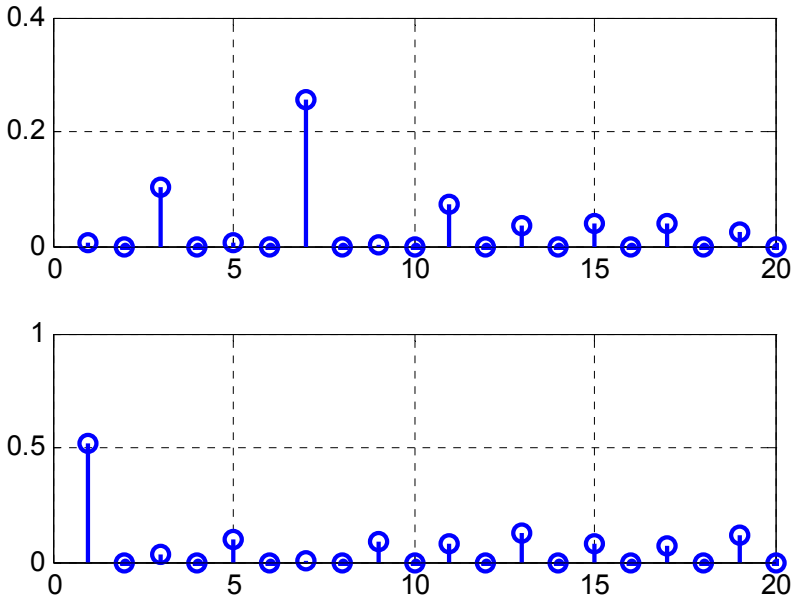

Figure 5-16. CM and DM harmonic components for ASVM without inter-phase interleaving (R_{fs} =7).

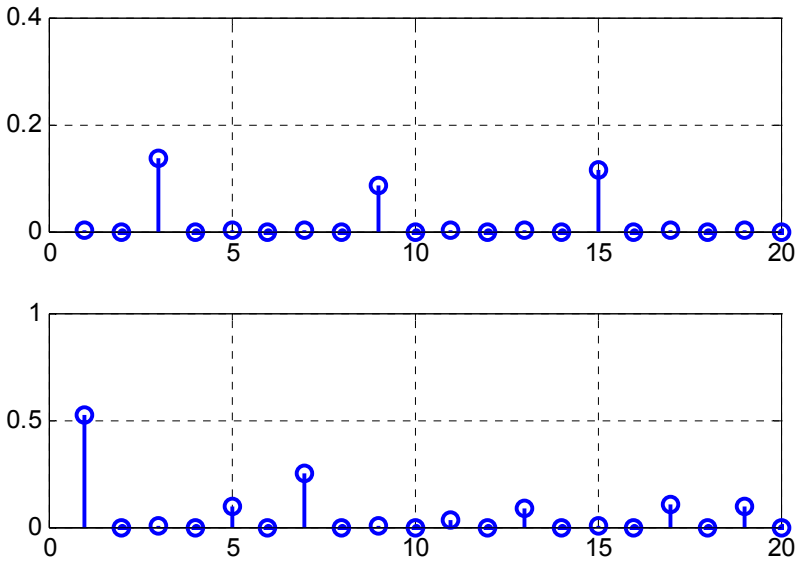

Figure 5-17. CM and DM harmonic components for ASVM with inter-phase interleaving (R_{fs} =7).

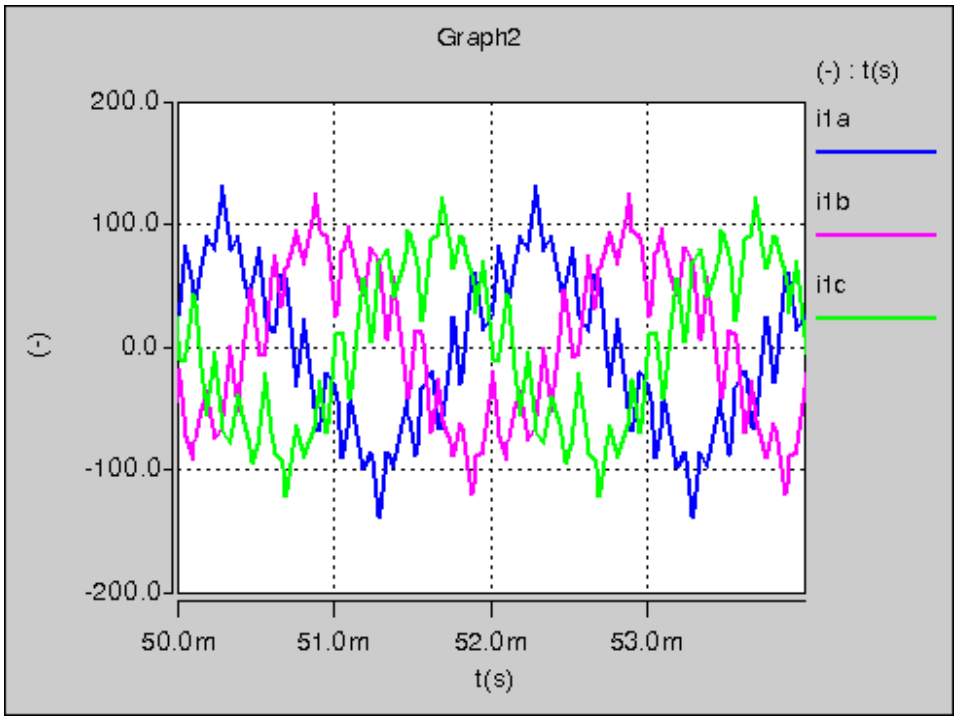

Figure 5-18. Three phase Current without inter-phase interleaving.

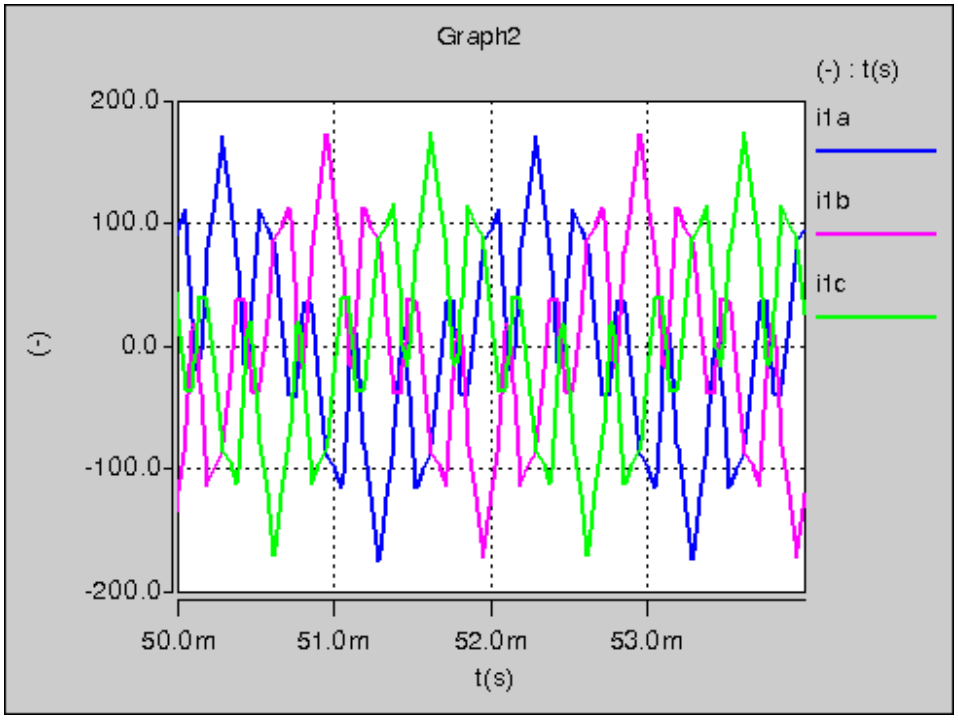

Figure 5-19. Three phase currents with inter-phase interleaving.

5.3 Improved Asymmetric Space Vector Modulation

5.3.1 Principle of Improved Asymmetric Space Vector Modulation

Even though synchronized PWM and triplen carrier ratio is used, the performance of ASVM can be further improved. Without loss of generality, the work in this chapter is based on the example system shown in Figure 5-20. In Figure 5-20, a simple two level VSC is operated as a rectifier. The power flows from the generator (modeled as a voltage source connected in series with a boost inductor) to the dc load (shown as a dc resistor). In the system under study, the ac line-to-neutral rms voltage is 230 V, the apparent power is 300 kVA, the dc bus voltage is 700V, the fundamental frequency varies between 500 Hz and 2 kHz, and ASVM is used.

Following the conventional wisdom, an odd triplen carrier ratio is preferred [9-10]. In this paper, R_{fs} is assumed to be 9. As a result, 18 vectors can be generated in one line cycle as shown in Figure 5-21. Since lower switching frequency usually means higher system harmonic currents, the lowest switching frequency 4.5 kHz is selected for study. The corresponding fundamental frequency is 500 kHz.

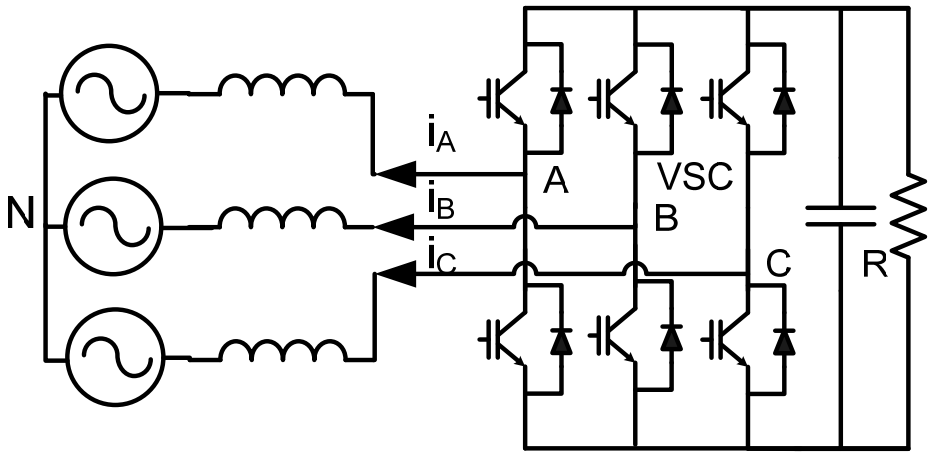

Figure 5-20. Single VSC system under study.

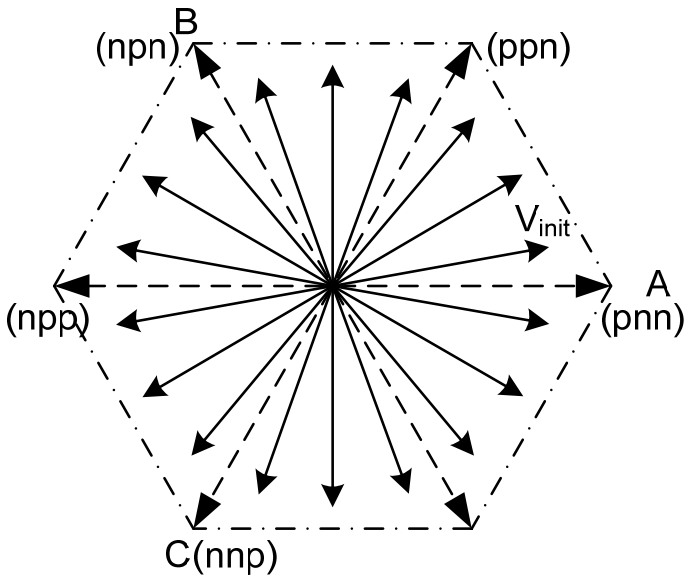

Figure 5-21. Output vectors of ASVM (R_{fs} =9)

The PWM waveform for phase A is shown in Figure 5-22 when the first vector (V_{init}) is located at 10° and modulation index (M) is 0.9. In this paper, M is defined as the ratio between the line-to-line peak voltage to dc bus voltage, which is between 0 and 1. In Figure 5-22, the green curve is the fundamental component of the PWM waveform.

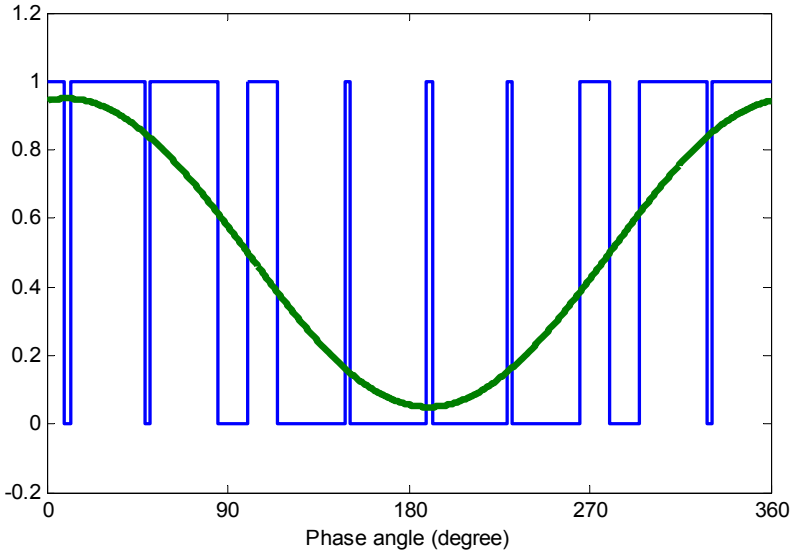

Figure 5-22. PWM wave for phase A (V_{init} at 10°and M=0.9)

As presented in [10-11], the integration of the error between PWM waves and fundamental component indicates the energy of harmonic components. The integration results of such error in each half switching period (period for each vector in Figure 5-21) is shown and compared in Figure 5-22. From Figure 5-22, it can be seen that the error is highest for the vectors located at 90° or 270°, where the fundamental component crosses zero.

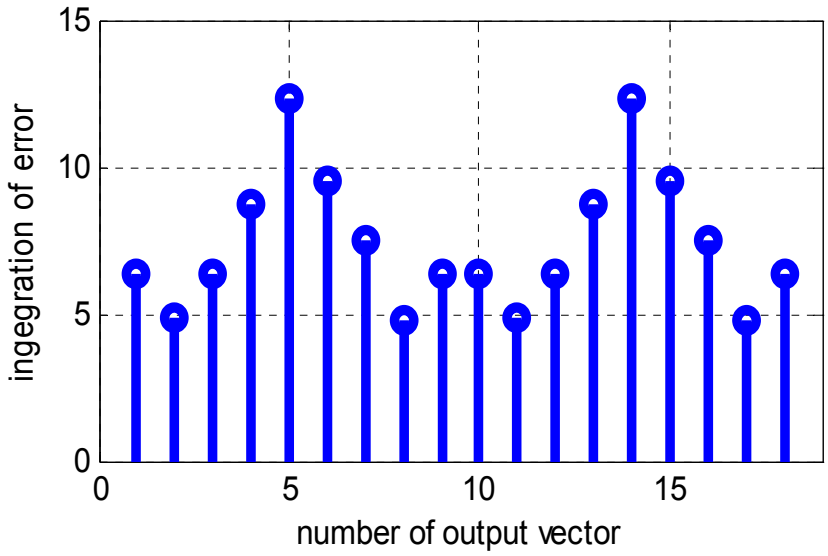

Figure 5-23. Energy of harmonic voltage for each vector

Even through the THD of harmonic voltage cannot be reduced, the THD of harmonic current can be reduced by increasing the system switching frequency. [1] This can be done by adding additional switching to the system. Since additional switching usually means higher switching loss, which is critical for high power application, the number of additional switching should be limited.

The basic idea of the improved ASVM proposed in this paper is to double the switching frequency to reduce the current THD only in specific switching cycles. From

Figure 5-23, it is obvious that the additional switching should be added in 5th (90°) and 14th (270°) vectors, when the fundamental voltage crosses zero.

For grid-connected rectifier, to maximize the power rating of a converter, usually unity power factor control is desirable. For unity power factor control, when fundamental voltage crosses zero, the fundamental current will also cross zero. Consequently, the penalty of additional switching loss is very limited.

For traditional ASVM, to generate each vector, two non-zero vectors (V_1 and V_2) and two zero vectors (V_0 and V_7) in each sector will be used as shown in Figure 5-24 to generate the vector at 90°. To increase the equivalent frequency in this switching cycle, part of V_1 and V_2 is swapped as shown in Figure 5-25. In the time domain, it means one additional pulse is added to the system in phase A when fundamental voltage of phase A reaches 90°. In the same way, another pulse will be also added when fundamental voltage of phase A reaches 270°. In a word, two pulses will be added to phase A when fundamental voltage of phase A crosses zero. The same method can be applied to phase B and phase C when the fundamental voltage component of each phase crosses zero. Finally, 11 pulses will be generated in one line cycle instead of 9 pulses used in traditional ASVM.

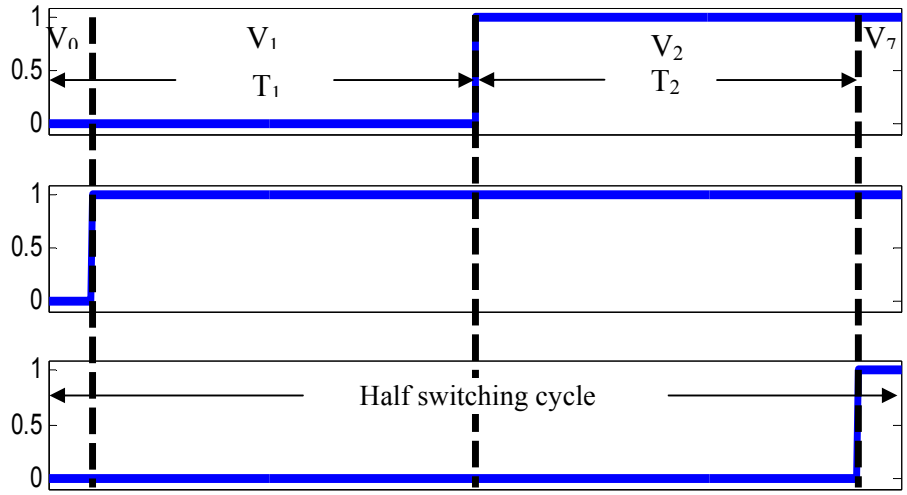

Figure 5-24. Three phase PWM waves when output vector is 90°

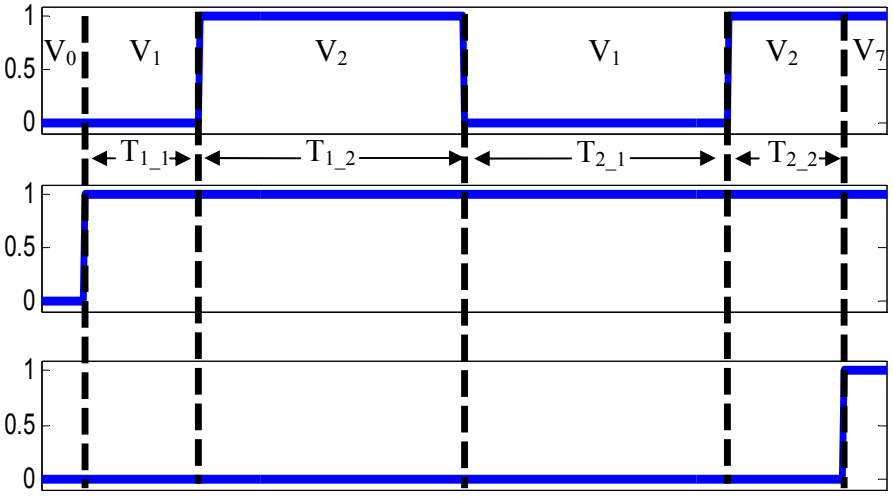

Figure 5-25. Basic idea of improved ASVM

From Figure 5-24, the duration of V_1 and V_2 are T_1 and T_2 for traditional ASVM. For improved ASVM shown in Figure 5-25, the duration of V_1 is separated into two parts T_{1_1} and T_{1_2} and the duration of V2 is also separated into two parts T_{2_1} and T_{2_2}. To describe the process of swapping part of V1 and V2, two variables are defined in this paper.

$$k1 = \frac{T_{1\_1}}{T_1} \tag{5-5}$$

$$k2 = \frac{T_{2\_1}}{T_2} \tag{5-6}$$

By selecting k_1 and k_2, the duration and position of the additional pulses can be controlled. And, to keep the PWM wave symmetric in a line cycle, the sum of two k_1's used in vector 90 ° and 270° should be 1. So should be the sum of k_2's.

5.3.2 Improved ASVM in a Single VSC

For the improved ASVM, k_1 and k_2 can be optimized to minimize the THD of output current in a single VSC system. In this chapter, the optimized k_1 and k_2 are obtained by exhaustive searching method. However, the optimized k_1 and k_2 are not sensitive to the system modulation index (defined as the ratio between peak line-to-line voltage and dc bus voltage), e.g. when M is between 0.5 and 1. The optimized k_1 is always around 0.2 and k_2 is always around 0.8 for vector 90 °. As a result, k_1 and k_2 are kept to be 0.2 and 0.8 for vector 90° and 0.8 and 0.2 for 270° in all simulations and experiments. And the modulation index is assumed to be 0.9 for the analysis in this section, which is reasonable for rectifier applications.

However, the optimized k_1 and k_2 and the corresponding minimized THD of output current has close relationship with the positions of vectors shown in Figure 5-21. The impacts of the initial vector V_{init}'s position on the THD of output current for traditional ASVM and improved ASVM with optimized k_1 and k_2 are shown and compared in Figure 5-26. In Figure 5-26, the THD in all cases are normalized to the value when traditional ASVM is used and V_{init} is at 1°. The cases when V_{init} is at 0° and 20° are not

analyzed, since in these cases the output vectors can be on the boundary of adjacent sectors which should be avoided.

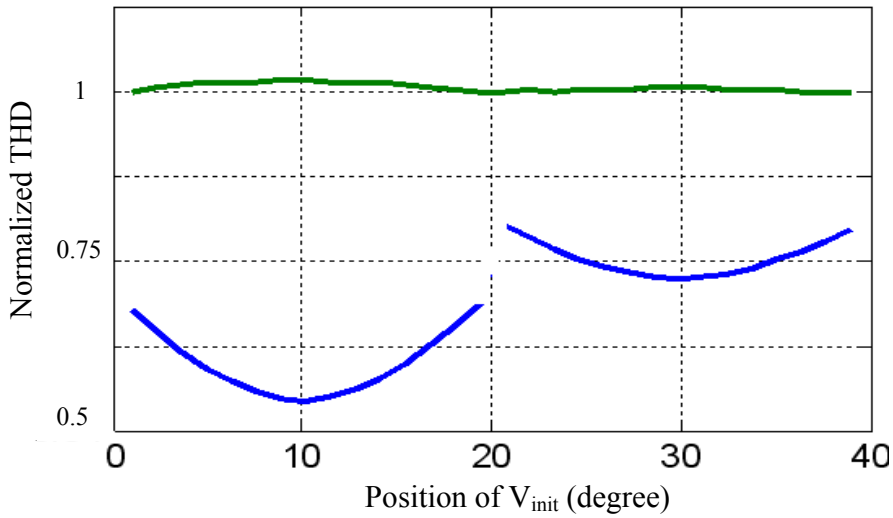

Figure 5-26. Relationship between normalized THD of i_A and V_{init} for traditional and improved ASVM

From Figure 5-26, the position of the first vector nearly cannot change the THD of output current for traditional ASVM. For improved ASVM, the THD of output current can be affected significantly by the position of the first vector. For the best case, when V_{init} is located at 10°, the THD of output current can be reduced by as much as about 50%. But for the worst cases, when V_{init} is located close to 20° and 40°, the THD reduction is very limited.

However, based on the study in [10] and [11], synchronized PWM should be used for the system with very low carrier ratio to avoid beat phenomenon. And synchronized ASVM can keep the positions of output vectors unchanged [12]. In other words, the position of V_{init}, practically, can be controlled to be at 10° to maximize the benefit of the improved ASVM. The simulation results with traditional and improved ASVM are shown in Figure 5-27 and Figure 5-28 under the operation condition described in last section.

From the simulation, the THD of output current is reduced from 8.1% to 4.1% by adding the two pulses with improved ASVM.

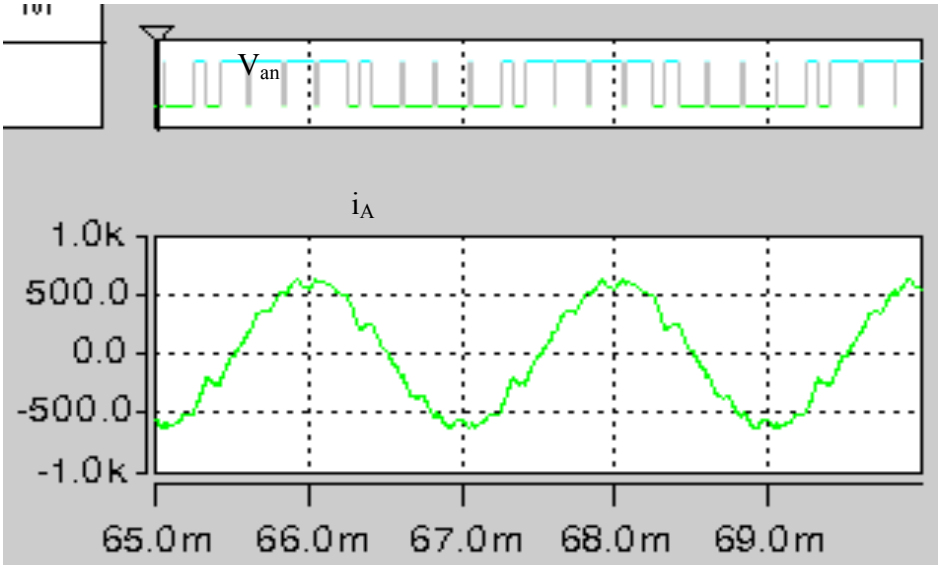

Figure 5-27. Simulated time domain waveforms of Van and i_A with traditional ASVM

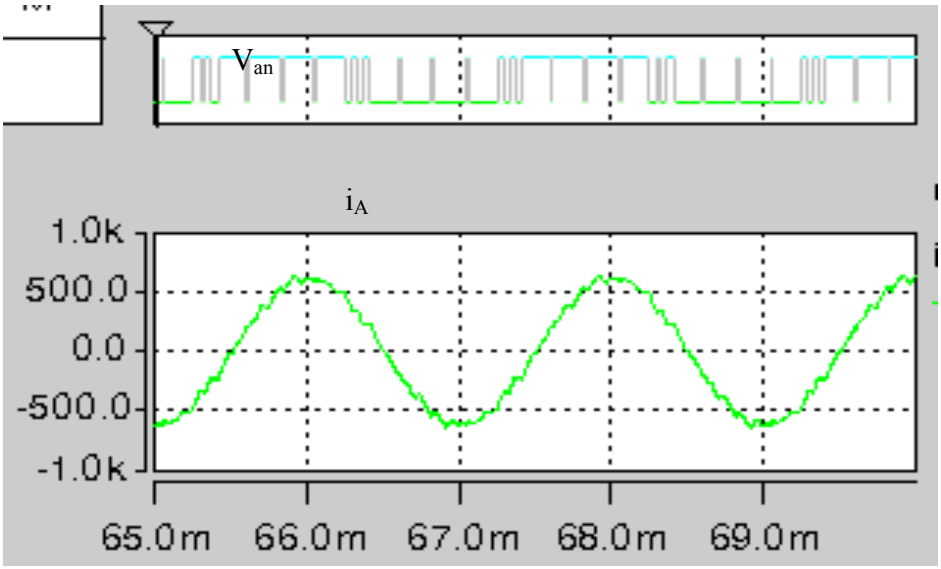

Figure 5-28. Simulated time domain waveforms of Van and i_A with improved ASVM

The benefit of improved ASVM can be explained clearly in frequency domain. The spectrum of output harmonic voltage for these two ASVM schemes are shown in Figure 5-29 and Figure 5-30 where half of dc bus voltage is used as unit.

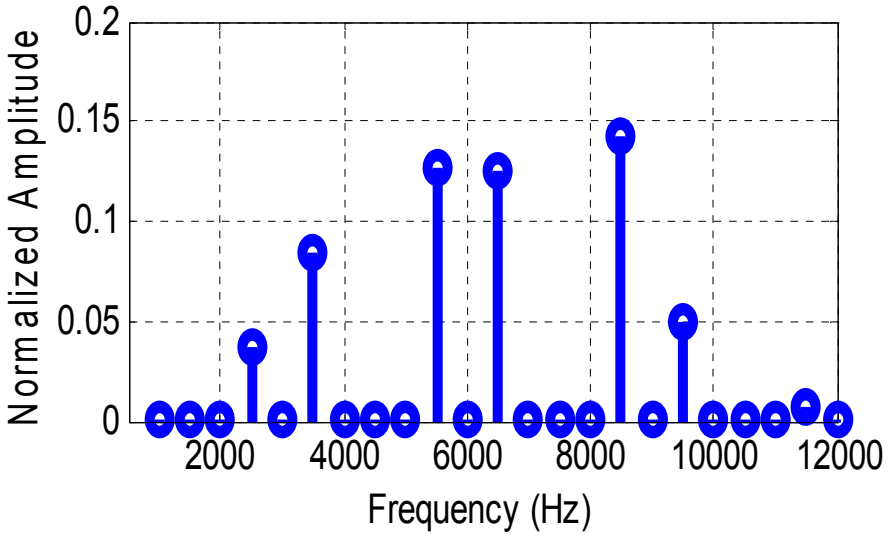

Figure 5-29. Spectra of V_{AN} for traditional ASVM.

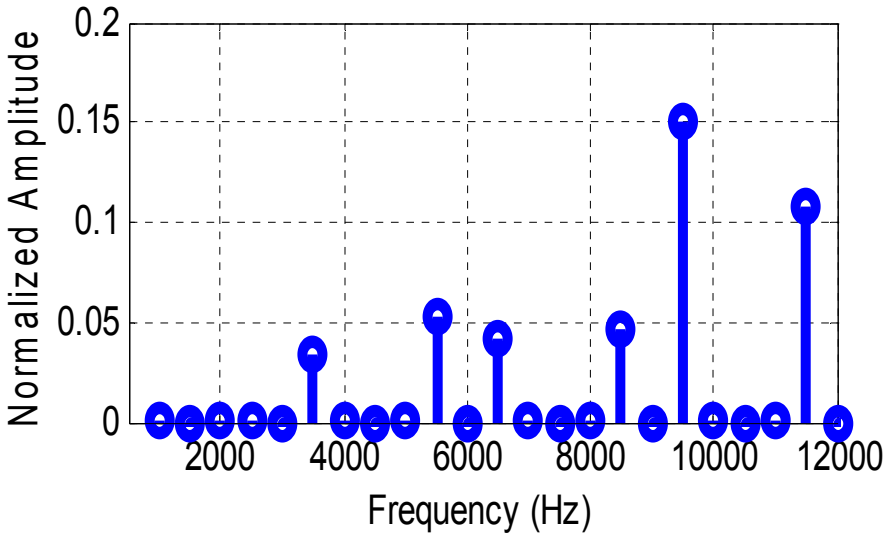

Figure 5-30. Spectra of V_{AN} for improved ASVM.

By comparing the voltage spectrum in Figure 5-29 and Figure 5-30, the energy of harmonic components is pushed from around switching frequency to around twice switching frequency by the additional two pulses in improved ASVM. As a result, the equivalent impedance of boost inductor is increased and the THD of output current is reduced.

Compared with traditional ASVM, the devices are switched two more times in each line cycle with improved ASVM. However, even if R_{fs} is increased to 11, traditional ASVM can only reduce the THD of output current to 82%, not mentioning the penalty of the unbalance between different phases due to non triplen R_{fs} [10].

Since the additional pulses for improved ASVM are added when fundamental voltage crosses zero, the corresponding additional switching loss has high relationship with power factor. However, for the traditional ASVM with 11 pulses, the switching actions are symmetric for the whole line cycle. So the total switching should be almost constant for different power factor system. The relationship between total switching loss and system power factor (presented by system displacement angle) for traditional ASVM with 9 or 11 pulses and improved ASVM with 11 pulses are summarized and compared in s. To simplify the analysis, the impact of ripple current is neglected and device turn-on and turn-off loss are assumed to be the same when the same current is switched. In Figure 5-31, the total switching loss for unity power factor system using traditional ASVM with 9 pulses is used as unit. The total switching loss in other cases are normalized based on such unit.

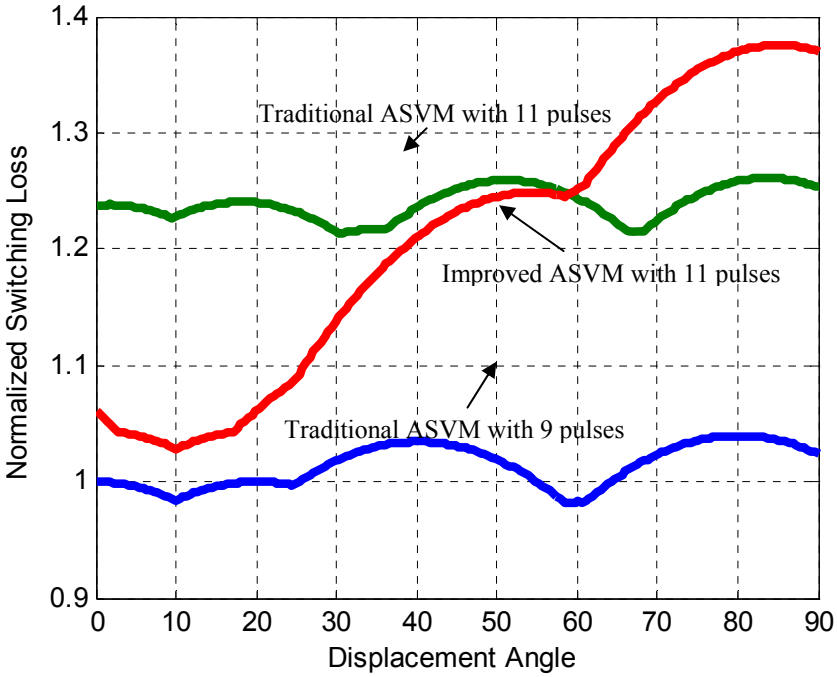

Figure 5-31. Relationship between normalized switching loss and system power factor.

From Figure 5-31, if the system power factor is high, e.g. the displacement angle is within 20°, the total switching loss will be increased by less than 5% for improved ASVM with 11 pulses and the THD of output current can be reduced by about 50%.

However, if traditional ASVM with 11 pulses is used, the total switching loss can be increased by 20%~25% and the THD of output current can only be reduced by less than 20%. The benefit of improved ASVM is very obvious compared with traditional ASVM for high power factor case. If the power factor is low, e.g. the displacement angle is between 20° and 60°, the additional switching loss related to improved ASVM with 11 pulses is still lower than the case with traditional ASVM, but the additional switching loss may not be neglected. When the power factor is very low, e.g. the displace angle is between 60° and 90°, even though the benefit of THD reduction related to improved

ASVM is the same, the penalty of additional switching loss will be very high, which is even higher than the case with traditional ASVM with 11 pulse. A trade-off may be necessary between the weight reduction of boost inductor due to low current THD and the weight increase of heat-sink due to higher switching loss.

5.3.3 Improved ASVM in Interleaved VSCs System

Interleaving can further reduce the THD of output current by changing part of the output harmonic currents into circulating currents between two paralleled VSCs and the interleaving angle (κ) should be designed to eliminate the dominant harmonic currents in output currents. [8]

In this paper, the topology used for paralleled VSCs system is shown in Figure 5-32 for high power density design [13]. In Figure 5-32, inter-phase inductors are involved to limit the circulating current in the system with interleaving. Since the size of the inter-phase inductor is mainly determined by the amplitude of circulating current, it would be very desirable if the amplitude of circulating current can be reduced together with the THD of output current.

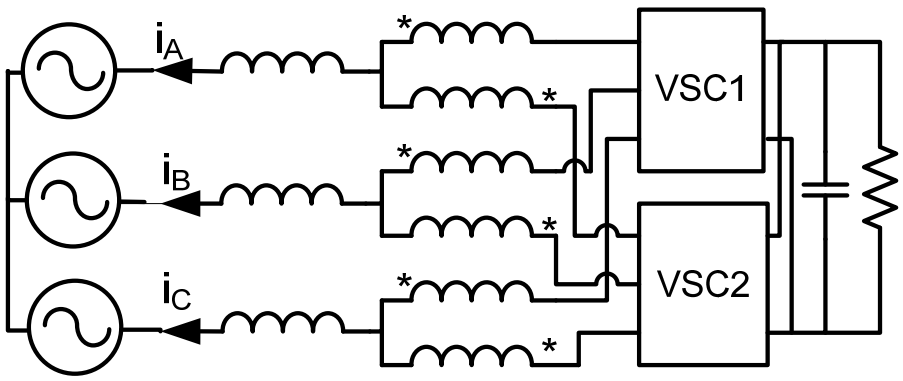

Figure 5-32. Paralleled VSCs system under study.

From Figure 5-29, the dominant harmonic currents are around switching frequency, so interleaving angle π should be used for traditional ASVM when M is high, e.g. 0.9. Based on Figure 5-30, interleaving angle $\pi/2$ should be used, since for improved ASVM the dominant harmonic currents are pushed to around twice switching frequency. Considering system symmetry, V_{init} for VSC1 and VSC2 are placed at 5° and 15°.

As a summary of the analysis, the normalized THD of output current in different cases are compared in Figure 5-33. In Figure 5-33, the THD of output current, when traditional ASVM is used and M is 0.87, is used as unity. From Figure 5-33, improved ASVM is only good when modulation index is high. When modulation index is close to 1, improved ASVM can reduce the THD almost by half. However, when modulation index is lower than 0.63, it may not be as good as traditional ASVM with 11 pulses per line cycle. For interleaved VSCs system with traditional ASVM, interleaving angle $\pi/2$ should be used for low modulation index case and interleaving angle π should be used for high modulation index case. This is similar to the case with high carrier ratio case [13]. But improved ASVM with $\pi/2$ interleaving is always the best PWM scheme no matter modulation index is low or high.

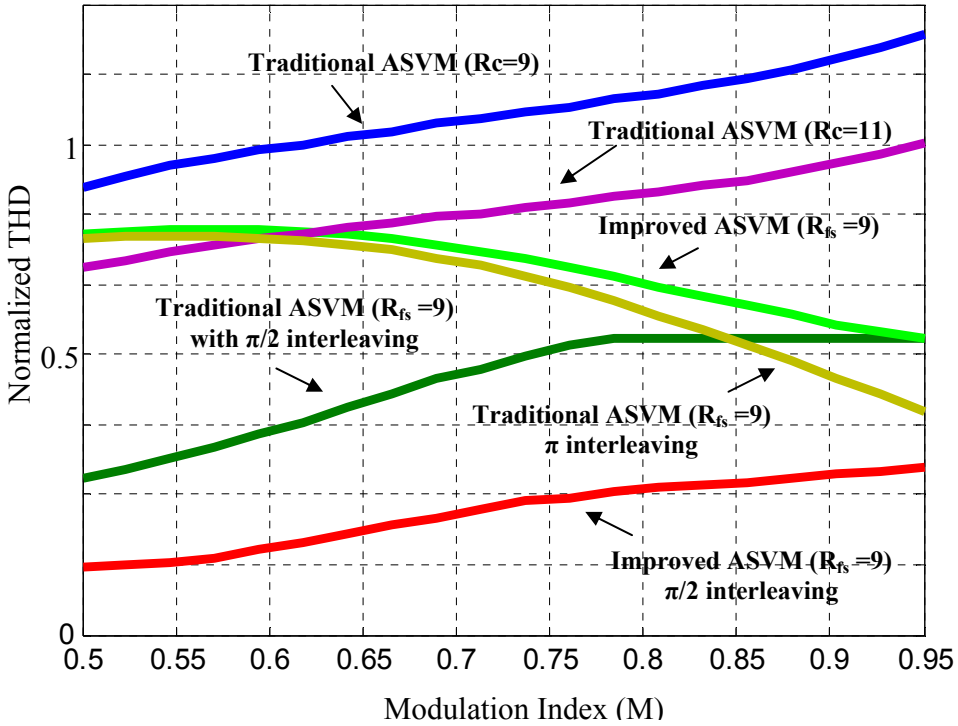

Figure 5-33. THD reduction comparison

For the example system shown in Figure 5-32, the simulations for paralleled VSCs topology are performed for traditional and improved ASVM. In the simulation, the inter-phase inductor is realized by two coupled 100 μH inductor. The simulation results are shown in Figure 5-34 and Figure 5-35. From the simulation results, the THD of output current, with optimized k_1 and k_2, can be reduced from 4.3% to 2.1% with interleaving and improved ASVM.

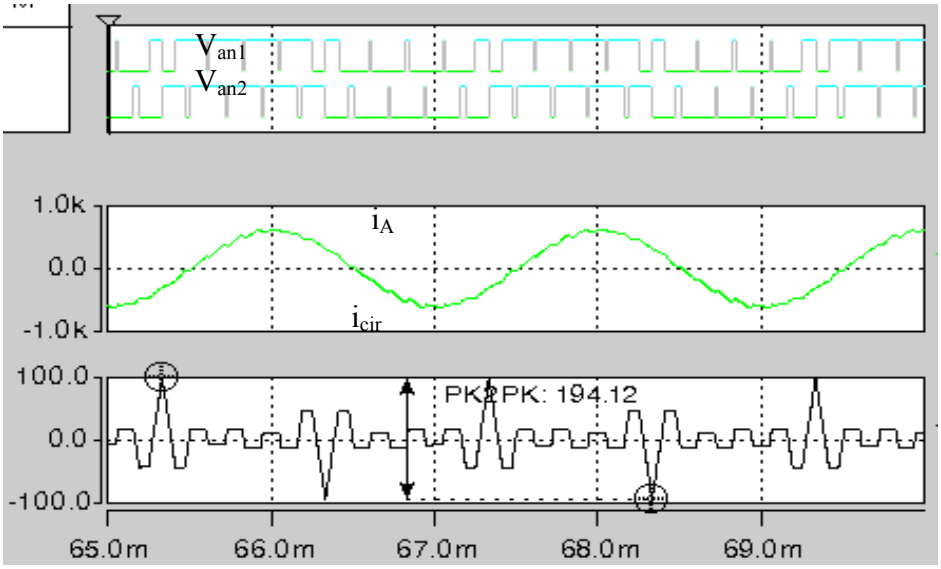

Figure 5-34. Simulation results for traditional ASVM (κ=π)

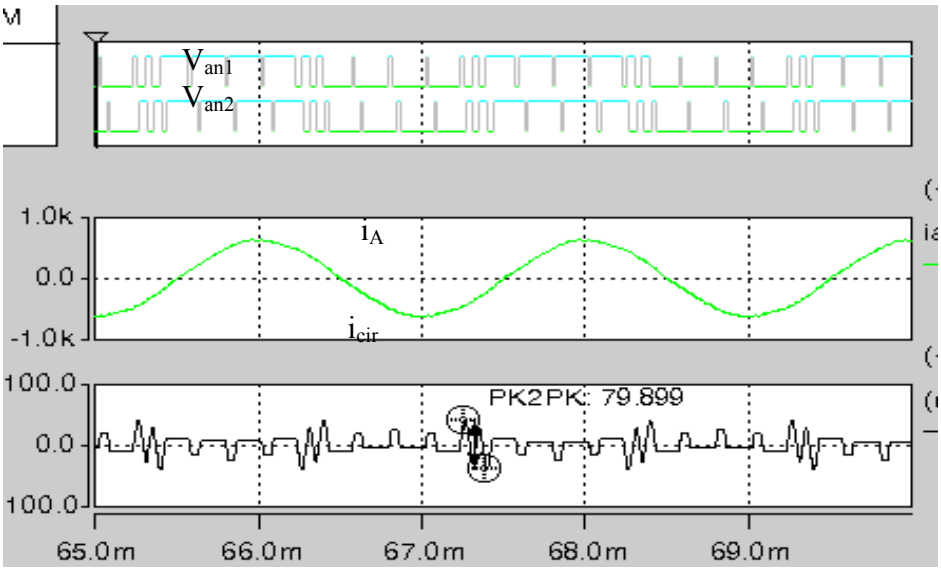

Figure 5-35. Simulation results for improved ASVM (κ=π/2)

In addition, the amplitude of circulating current is also reduced from 194A to 80A. This is because for traditional ASVM the peak of circulating current happens when the fundamental voltage crosses zero. After improved ASVM is used, the switching frequency is doubled within the switching cycles. So the voltage pulse applied on the inter-phase inductor is also split into two short pulses which can be seen from the

simulation results. Since the duration of voltage pulse mainly determined the peak of circulating current, improved ASVM can also help to reduce the peak value of circulating current.

As analyzed above, lower peak value of circulating current means lighter inter-phase inductor. Improved ASVM can further reduce the passive components weight for interleaved VSCs system.

5.3.4 Experimental Results and Inductor Weight Comparison

The experiment is designed to verify three key points in the analysis above. First, the improved ASVM can reduce the THD of output current dramatically. Second, interleaving with designed interleaving angle can further reduce the THD of output current. Third, the amplitude of circulating current in interleaved VSCs system can also be significantly reduced by the improved ASVM. After these key points are verified, inductor physical design is done for the example system described in section II with different PWM schemes. The weight comparison results are summarized in Table IV to show the benefit of improved ASVM.

To simplify the experiment, the inverter configuration in Figure 5-36 is used, whose voltage harmonic spectrum are the same as in the case of the rectifier configuration in Figure 5-32. The ac side now has a three phase resistor load in addition to inductors.

Since in the analysis, the harmonic current is assumed to be only determined by inductance and harmonic voltage, the resistor load may change the amplitude of harmonic currents especially when switching frequency is low and the power factor is high. However, the same setup is used for all PWM schemes, so the relative THD reduction of output current is still very close to the analysis results.

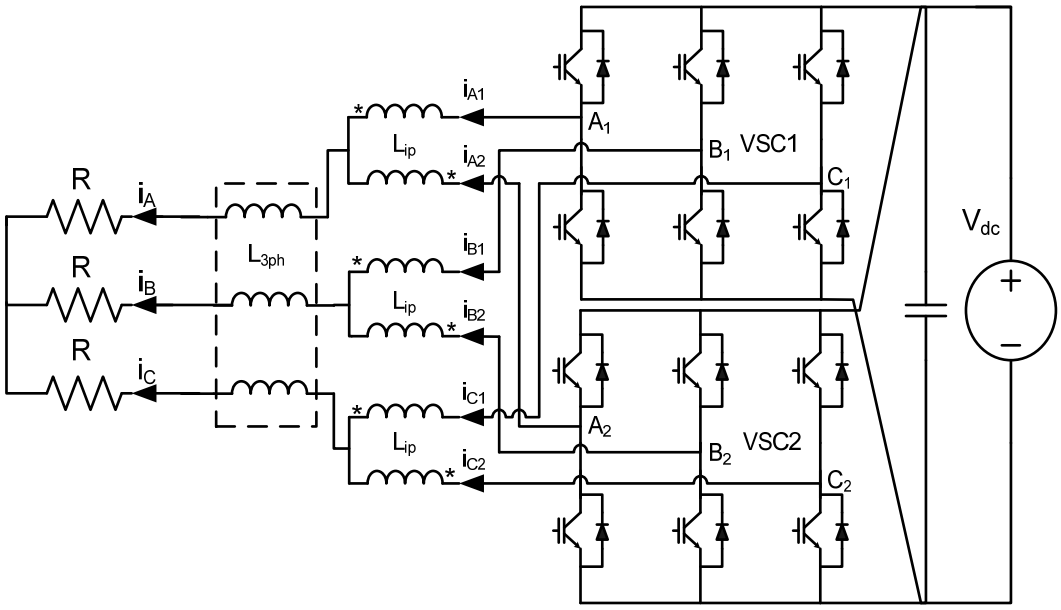

Figure 5-36. Schematic of the experimental setup.

The experimental setup comprises of two 6-pack IGBT IPMs from Fuji (6MBP20RH060) for two VSCs power stage, one common DSP-FPGA digital controller, three inter-phase inductors, one three phase inductor and three 6Ω resistors as load. The ac line inductor is 400μH and the inter-phase inductor used to limit circulating current is 3mH. The dc voltage is 100V, and the fundamental and switching frequency are chosen as 500Hz and 4.5 kHz respectively. Synchronized PWM and close loop control are used for all cases. The reference RMS value of fundamental current in the resistor load is 6A with corresponding modulation index of 0.9. To verify the analysis results in single VSC system, the two VSCs are controlled as one VSC without interleaving.

The experimental waveforms for single VSC case with traditional ASVM and improved ASVM are shown in Figure 5-37 and Figure 5-38. The current THD value and RMS value of fundamental components are summarized in Table 5-1.

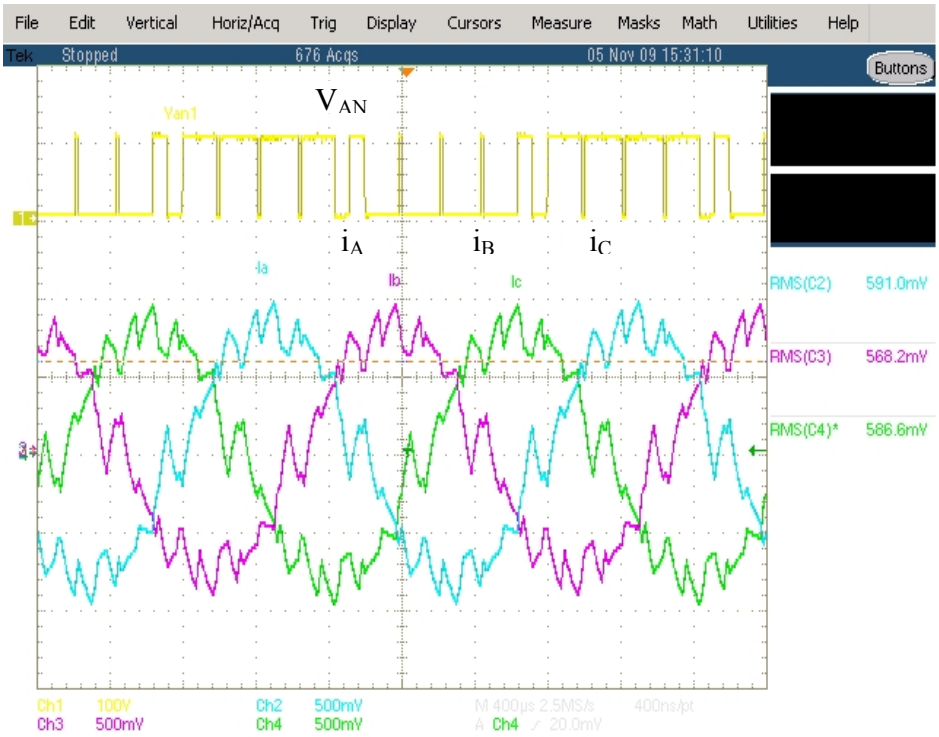

Figure 5-37. V_{AN}, i_A, i_B, i_C for traditional ASVM

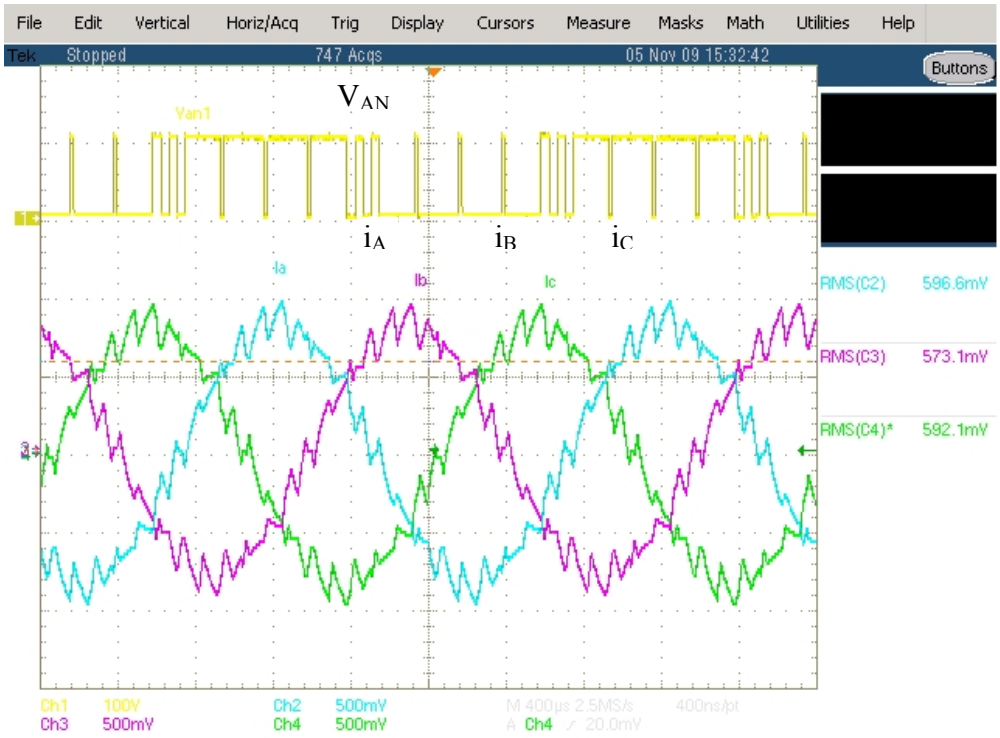

Figure 5-38. V_{AN}, i_A, i_B, i_C for traditional ASVM

Table 5-1. Experimental results for single VSC

		Experimental Results	Simulation Results
Traditional ASVM	RMS of i_A	5.82A	5.94A
	THD of i_A	17.8% (100%)	19.5%
Improved ASVM	RMS of i_A	5.93A	5.94A
	THD of i_A	10.7% (60%)	11.4%

Table 5-1, it can be seen that the rms value of output current is controlled very close to the reference value. And by adding two pulses when voltage fundamental component crosses zero, the THD of output current can be reduced by 40%. Since the power factor in this system is very close to 1, the current amplitude is almost zero during the added pulses, introducing very limited additional power loss. The difference of i_A rms value between experimental and simulation results is mainly caused by sampling issues. When current waveform is distorted, it is difficult to sample the real fundamental component. Such difference can be reduced by improved ASVM, since ripple current is reduced. The difference of THD of i_A between experimental and simulation results is mainly caused by the system parameters difference between simulation and experiment.

The experimental waveforms for interleaved VSCs case with traditional ASVM and improved ASVM are shown in Figure 5-39 and Figure 5-40. The current THD value and rms value of fundamental components are summarized in Table 5-2.

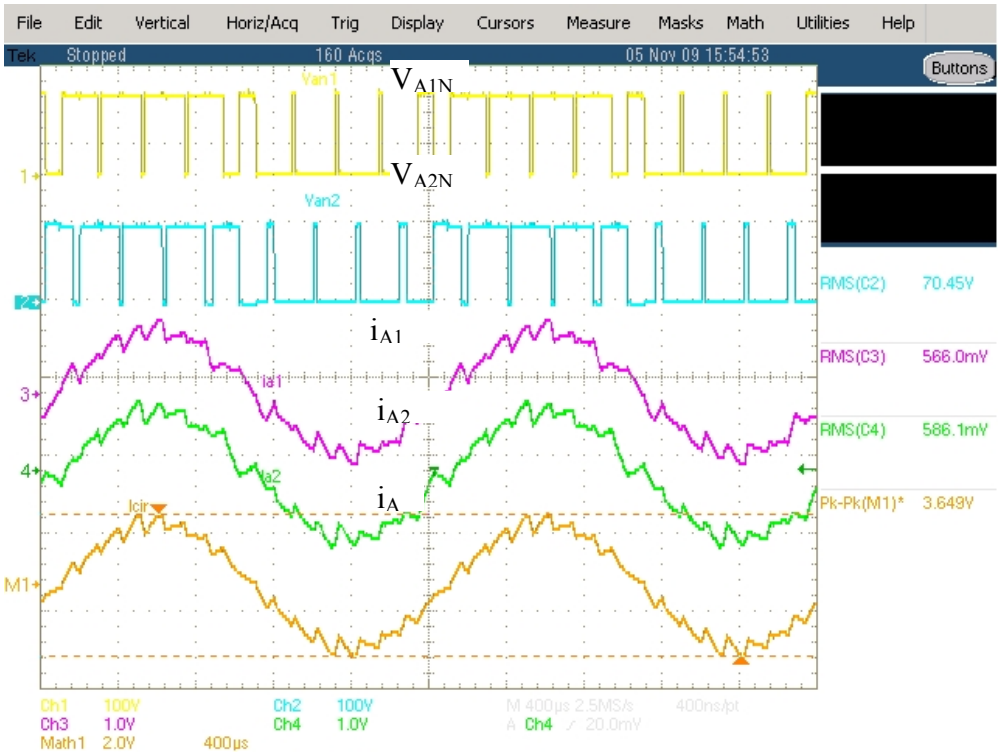

Figure 5-39. V_{A1N}, V_{A2N},i_{A1}, i_{A2}, i_A for traditional ASVM with interleaving.

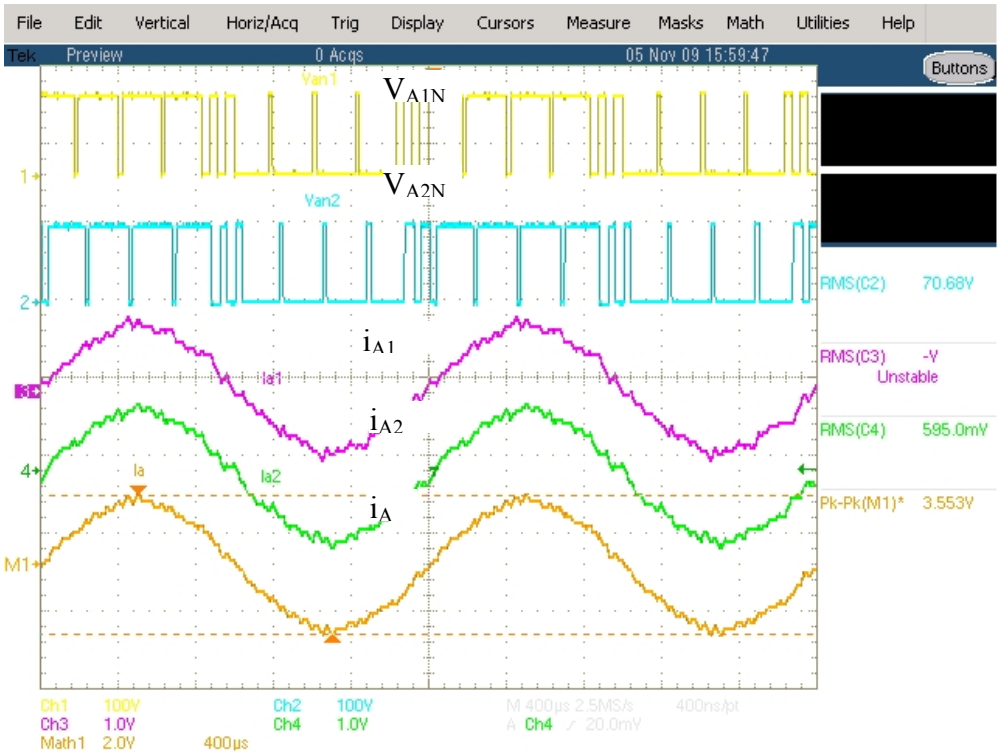

Figure 5-40. V_{A1N}, V_{A2N},i_{A1}, i_{A2}, i_A for improved ASVM with interleaving

Table 5-2. Experimental results for interleaved VSCs system

		Experimental Results	Simulation Results
Traditional ASVM (k=π)	RMS of i_A	5.82A	5.94A
	THD of i_A	9.5% (54%)	9.5%
Improved ASVM (k=π/2)	RMS of i_A	5.94A	5.94A
	THD of i_A	5.0% (28%)	5.5%

From Figure 5-39, Figure 5-40 and Table 5-2. Experimental results for interleaved VSCs systemTable 5-2, it can be seen that interleaving can also reduce the THD of output current to 54% compared with the traditional ASVM case without interleaving. And it can be further reduced to 28% with improved ASVM. Again, the additional switching is added when the output current crosses zero, introducing very limited additional power loss.

To verify the impact of improved ASVM on the circulating current, the experiment for interleaved VSCs cases are repeated. The experimental waveforms including circulating currents for interleaved VSCs case with traditional ASVM and improved ASVM are shown in Figure 5-41 and Figure 5-42.

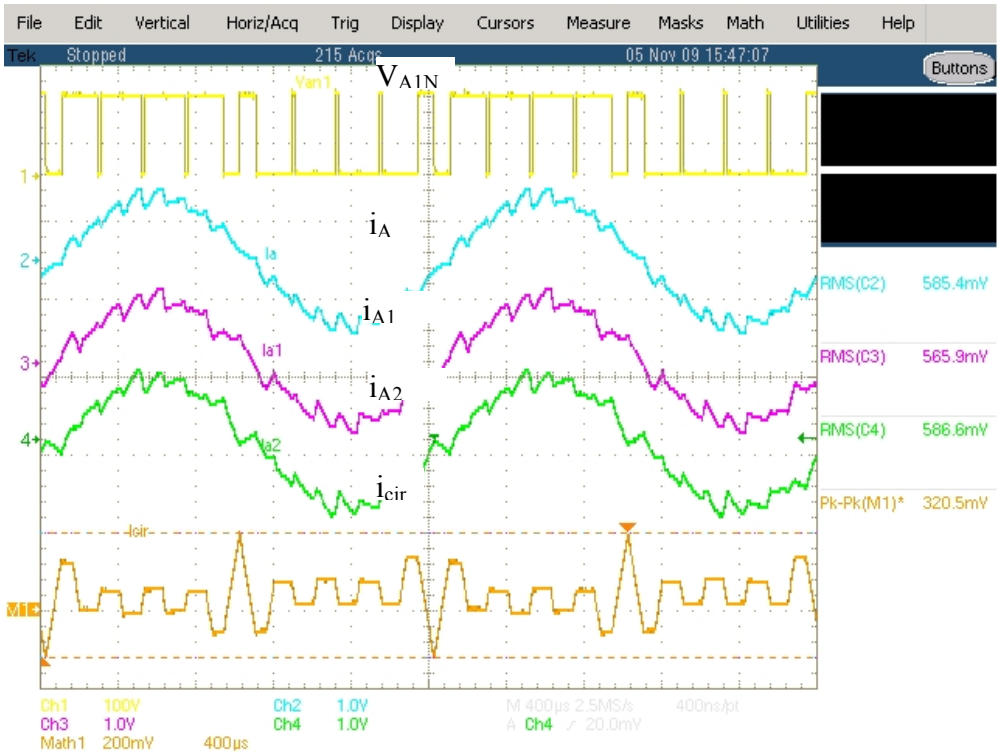

Figure 5-41. V_{A1N}, i_A, i_B, i_C, i_{cir} for improved ASVM.

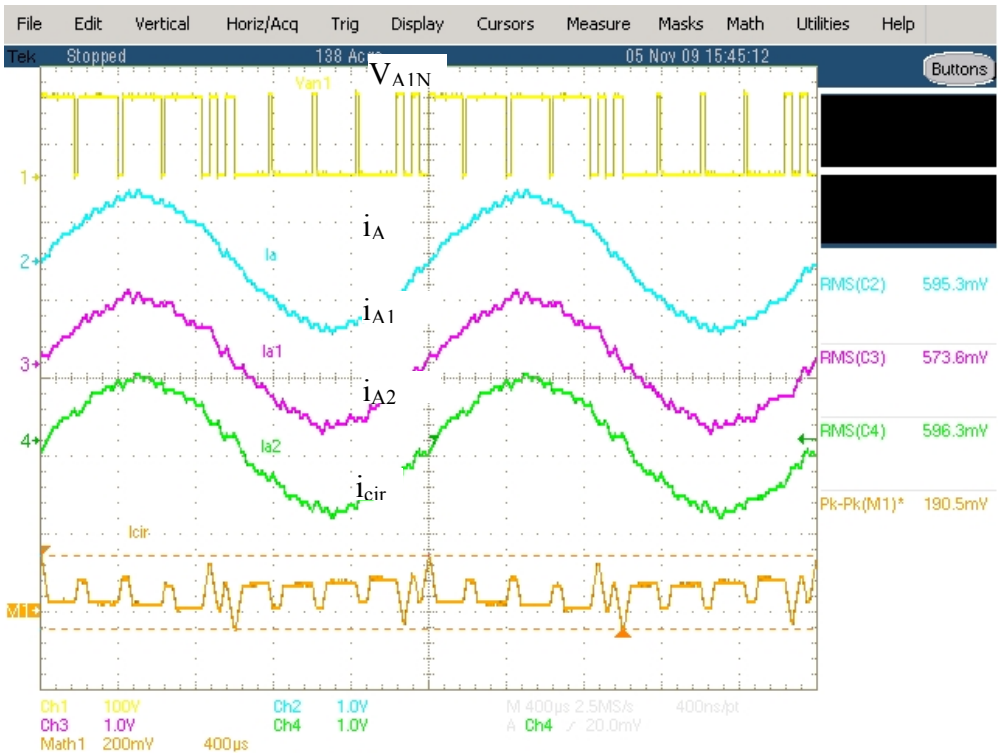

Figure 5-42. V_{A1N}, i_A, i_B, i_C, i_{cir} for improved ASVM.

From Figure 5-41 and Figure 5-42, it can be seen that the amplitude of circulating current is reduced from 1.6A to 0.9A with improved ASVM. The analysis and simulation results are verified.

To further verify the impact of modulation index on the THD reduction benefit of improved ASVM. The experiments are repeated with reduced modulation index (M=0.75) and the reference current is reduced from 6A to 5A. The experimental data are listed in Table 5-3.

Table 5-3. Summary of Experimental results (M=0.75 or M=0.9)

		M=0.9	M=0.75
Traditional ASVM	RMS of i_A	5.82A	5.0A
	THD of i_A	17.8% (100%)	20% (100%)
Improved ASVM	RMS of i_A	5.93A	4.95A
	THD of i_A	10.7% (60%)	14.9% (75%)
Traditional ASVM ($k=\pi$)	RMS of i_A	5.82A	4.91A
	THD of i_A	9.5% (53%)	13.9% (70%)
Improved ASVM ($k=\pi/2$)	RMS of i_A	5.94A	5.07A
	THD of i_A	5.0% (29%)	5.6% (28%)

From Table 5-3, higher modulation index is good for THD reduction in single VSC system with improved ASVM and interleaved VSCs with traditional ASVM. But improved ASVM with interleaving is always the best PWM scheme in THD reduction. These match the analysis results in Figure 5-33.

After the key conclusions are verified by experimental results, the inductor physical design is done based on the simulation results in last two sections. The design results are summarized in Table 5-4 for each case to reduce the THD of output current to the same level 2.1%. In the design, METGLAS amorphous Alloy 2605SA1 is used for core design,

the temperature rise is limited within 100 °C, EE core is used for three inductor design and CC core is used for inter-phase inductor design. From Table 5-4, improved ASVM with interleaving can reduce the weight of required inductor significantly.

Table 5-4. Inductor Weight Comparison

Case	Single VSC with traditional ASVM	Single VSC with Improved ASVM	Interleaved Two VSCs with traditional ASVM ($\kappa=\pi$)	Interleaved Two VSCs with improved ASVM($\kappa=\pi/2$)
Additional inductors needed	one 300uH three phase inductor	one 100uH three phase inductor	one 80 uH three phase and three 400 uH inter-phase inductors	three 400uH inter-phase inductors
Weight of total inductors	140kg (100%)	47kg (34%)	70kg (50%)	16kg (11.5%)

5.4 Summary

Low switching frequency can bring some special issues to the system compared with high switching frequency. The overlap of harmonic sidebands is explained, which can cause two problems: beat phenomenon and system three phase unbalance with non-triplen carrier ratio. The beat phenomenon can be eliminated by synchronized PWM which can fix the relative phase angle between harmonic side at f0 and the real fundamental component. The system unbalance can be solved by inter phase interleaving which has been verified by simulating results.

After that, this chapter also presented an improved asymmetric space vector modulation (ASVM) for two level VSCs operated with low carrier ratio. By adding two pulses for each phase in one fundamental cycle, the THD of output current can be reduced as much as 50%. The THD can be further reduced to 20% if improved ASVM is used together with interleaving in a paralleled VSC system. Among the four PWM

schemes analyzed, improved ASVM with 90° interleaving can always achieve the lowest THD no matter modulation index is high or low. In addition, improved interleaving can also reduce the amplitude of circulating current between the paralleled VSCs which can help reduce the size and weight of inter-phase inductor. Since the additional pulses are added when fundamental voltage crosses zero, the resulted extra power loss is very limited especially if system power factor is high. The benefit of improved ASVM is also demonstrated by inductor weight comparison in different PWM schemes and all of the analyses are verified by experimental results.

Chapter 6 Internal Fault Protection for Parallel VSCs System

This chapter studies how to protect a system with paralleled VSCs under the occurrence of internal faults. First, a sample system of paralleled VSCs used to study the impact of internal faults is described. Based on this system, the impacts of four kind of single device internal faults, including a short or open circuit of switches and diodes, are analyzed in detail. Then, by analyzing the characteristics of the system under fault, methods to detect and identify the faulty VSC, as well as fault isolation methods are presented. Experimental results using a prototype set up are presented to verify the analysis and proposed methods.

6.1 Introduction

As mentioned in the above chapters, parallel operation of VSCs has many benefits such as modularity, redundancy, flexibility for a gradual scaling up of power demand and higher power density. The downside of paralleling VSCs—as opposed to using a single converter rated at the total power—is the greater number of components, which reduces reliability as the possibility of faults in the system increases. In consequence, only if the VSC under fault can be isolated from the system and replaced by a redundant VSC can the reliability of the whole system be increased, which is the basis of the above-mentioned benefits of paralleling converters. This chapter mainly discussed four typical internal faults include the short or open circuit of switches and diodes, which can be caused by the melting or lifting of wire bonds as a result of thermal cycling, gate-drive failure, or load over currents.

For external faults such as ac or dc side short circuits, the methods of protecting VSCs are well known and have been discussed in [77]. But there are also internal faults such as short or open circuit of switches and diodes, which can be caused by the melting or lifting of wire bonds as a result of thermal cycling or load over currents. The method to deal with external faults cannot be applied to internal faults, since in this case not all switches can be controlled after an internal fault occurs. On this topic, [78]-[80] present methods to deal with the internal faults in a single VSC; however, the methods and conclusions presented cannot be extended to a paralleled converter system as the fault effects between VSCs was not taken into consideration. These effects cannot be neglected, as their impact can be catastrophic for the system; for instance, there may be ensuing circulating current between VSCs after a fault. The occurrence of internal faults should thus be studied in detail for systems with paralleled VSCs.

Addressing the above, this chapter studies in detail how to protect a system with paralleled VSCs when internal faults occur. Section 6.2 analyzes the impact of single device internal faults. Section 6.3 proposes internal fault detection methods, and Section 6.4 describes how to isolate the fault and recover the system. Finally, an experimental system is built to verify the analysis and feasibility of the proposed protection approach.

6.2 Impact of Single Device Internal Faults

There are basically two kinds of paralleled VSC systems. One topology involves an isolated dc bus for each VSC and the other use one common dc bus for all of the VSCs. In the first topology, no current can flow between the isolated dc buses, preventing the VSC under fault from affecting other healthy VSCs, as shown in the following analysis. However, since the equipment needed to create the isolated dc buses, such as

transformers are usually bulky and heavy, this topology has low power density, which is not desirable in applications such as aircraft. Furthermore, isolated dc buses will naturally prohibit the possibility of reducing the dc ripple current with interleaving as mentioned above, so this chapter mainly studies the internal faults of the paralleled VSC system with a common dc bus.

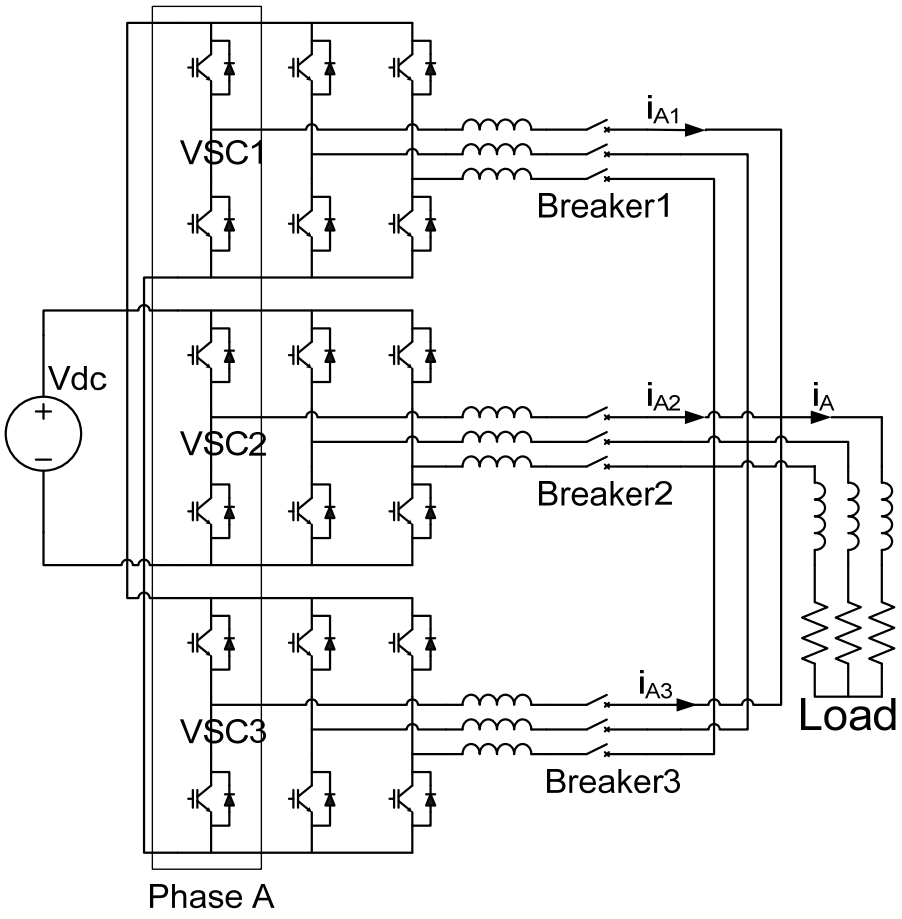

Figure 6-1. Sample system under study.

The sample system under study (shown in Figure 6-1) is comprised of three two-level VSCs, a common dc bus, and an R–L load. Two of the converters work together while the third is a redundant unit, creating a 2+1 system (N + 1 redundancy with N=2). Since the possibility of two devices having independent faults at the same time is very

low, this chapter considers only single-device faults, including short and open circuits. Also, because of the symmetry between phases, all faults are assumed to occur in phase A. The circuit diagram of this phase with all devices named is shown in Figure 6-2. Figure 6-3 through Figure 6-6 show the circuit diagrams of phase A under the four kinds of internal faults considered in this chapter. Figure 6-3 and Figure 6-4 show short-circuit faults, where the switch or diode short-circuit fault depends on whether the IGBT or diode was conducting when the fault occurred. As shown in Figure 6-5 and Figure 6-6, the open-circuit fault naming convention is self-explanatory.

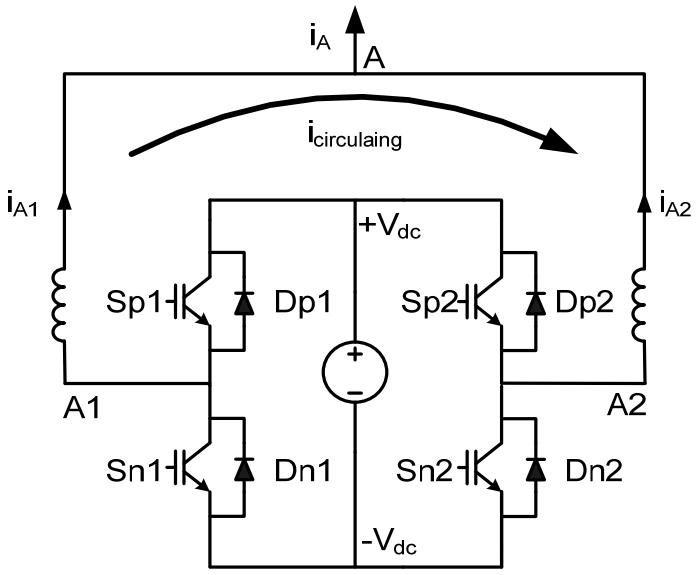

Figure 6-2. Phase A without fault.

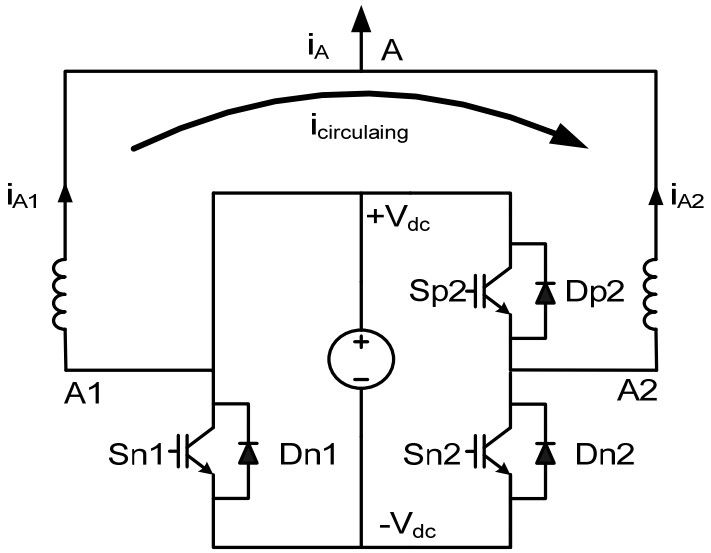

Figure 6-3. Phase A with switch short circuit fault.

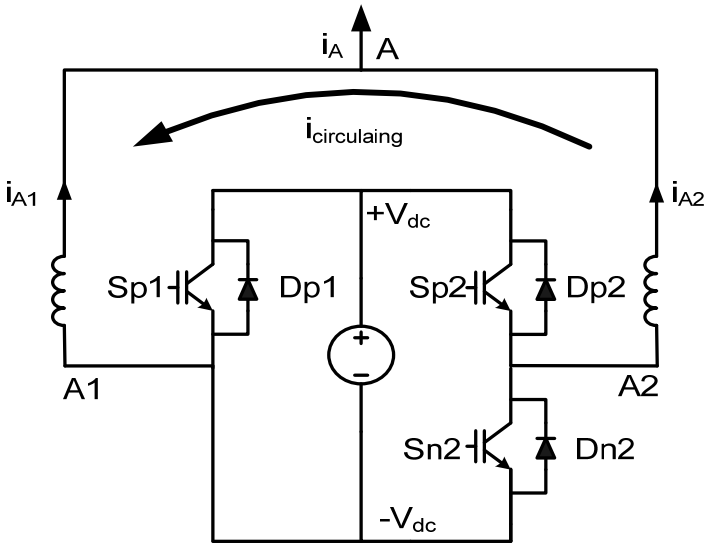

Figure 6-4. Phase A with diode short circuit fault.

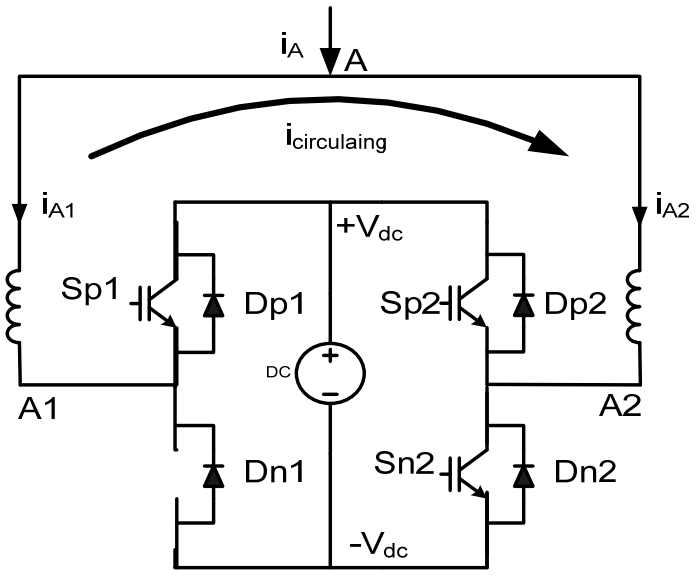

Figure 6-5. Phase A with switch open circuit fault.

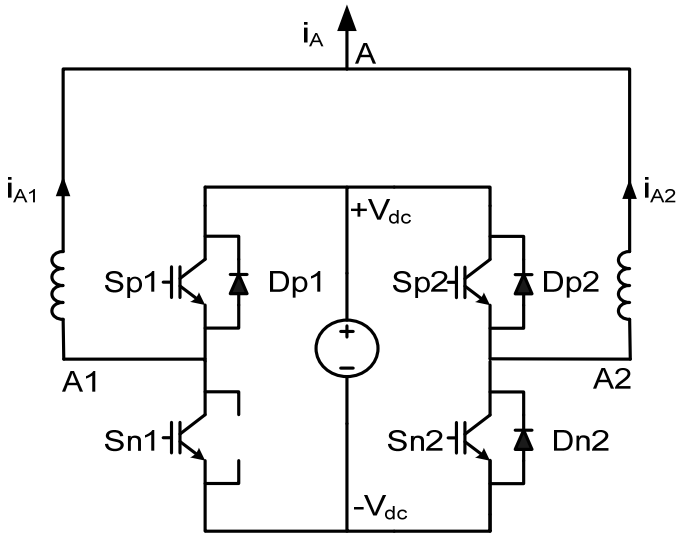

Figure 6-6. Phase A with switch open circuit fault.

For all four types of internal faults described, the ensuing circulating current induced by the actual fault can cause over-current or even damage to the remaining paralleled healthy phase-legs. This circulating current is defined in this chapter as the difference

between the current flowing through one phase-leg and the average current in all phase-legs. For example, if switch Sp1 is shorted while Sn2 is turned on, a loop is formed for the dc source to charge the ac line inductors, as shown in Figure 6-3, creating circulating current. This current continues to increase if Sn2 remains on, and it would eventually damage the healthy phase-leg due to over-current. The same failure occurs in a diode short-circuit fault. But for the switch open-circuit fault, since a diode is part of the circulating current loop, this current cannot increase after the current through the diode becomes zero. As a result, the circulating current is limited, and even considering the short period of the over-current capability of IGBTs, the switch open-circuit fault cannot damage the healthy phase-legs in the system and the output current will not be affected much, as long as a redundant VSC is activated quickly enough or the healthy VSC can work in current-limiting mode.

For the system with isolated dc buses, there is no such loop for circulating current, since current cannot flow between isolated dc buses. Taking a switch short-circuit fault as an example, if Sn1 is turned off to prevent shoot-through fault (as shown in Figure 6-7), the switch Sp1 short-circuit fault will be isolated and should not damage any other devices. Thus, the system with isolated dc buses will not be analyzed further in the later sections.

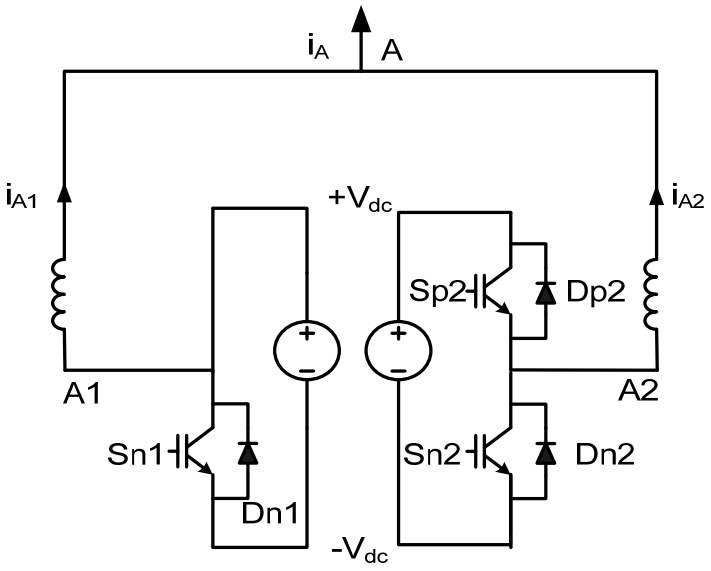

Figure 6-7. Phase A with switch short circuit fault with isolated DC bus.

For the system with a common dc bus, the switch and diode short circuit faults also affect the output ac voltage, since this type of fault connects the ac terminal point, e.g., A1 to either $+V_{dc}$ or $-V_{dc}$. As a result, the output voltage at point A is jeopardized and a dc current appears between phase A and the other two phases, until the fault VSC is isolated from the system. This dc current together with circulating current may in turn saturate the ac line inductors additionally causing over-current tripping and further faults.

Diode open faults, on the other hand, are different from the faults analyzed above. As Figure 6-6 shows, if Dn1 opens while Sp1 is turned off, current i_{A1} is interrupted, resulting in a transient overvoltage between points A and A1 with the capability to damage devices in other healthy VSCs. To mitigate this effect, a voltage limiter can be used in parallel with the inductor, such as a varistor dissipating the inductor energy in the fault VSC. However, considering that diode open-circuit faults are rare, and the effect is not unique for the paralleled converters, diode open-circuit faults will not be studied

further in this chapter. In addition, after the energy stored in the inductors is dissipated, the situation will be the same as the switch open circuit fault.

6.3 Detection of Internal Faults

The first step in protecting a paralleled VSC system from internal faults is to detect and locate the faulted VSC, which enables the fault isolation; the next step is system recovery. These converters normally have internal over-current detection schemes for switch protection, such as the de-saturation (or de-sat) function available in IGBT gate drives. This protection scheme acts upon the V_{CE} voltage and the gate signal of the device, turning off the gate signal in case the V_{CE} voltage is higher than the normal level, thus preventing the occurrence of over-currents. The de-sat function can also be used to detect internal faults. Specifically, when a switch or diode short-circuit fault occurs and the healthy switch in the faulty phase-leg is turned on, the dc source is shorted and the de-sat function is activated. Also, when a switch open-circuit fault occurs and the faulty switch is given a turn-on command, the V_{CE} voltage across the faulty switch rises to V_{dc}, which activates the de-sat protection, as its threshold voltage is clearly exceeded. In summary, in the presence of an internal fault, the de-sat protection of the faulted VSC is always activated. Furthermore, since the current increase in the healthy phase-leg is limited by the ac line inductor, only the faulty VSC de-sat protection can be activated, and thus the fault is detected.

In addition to the de-sat protection, the circulating current itself can be used to detect the faulty phase-leg when an internal fault occurs. This is useful if the controller cannot see the de-sat protection signal. For example, for the switch short circuit fault shown in Figure 6-3, if Sp1 and Sp2 are turned on together, the de-sat protection of Sp1 is activated,

turning off VSC1, and the closed state of Sp2 will increase the circulation. The same thing occurs during the other two internal faults; therefore, monitoring the circulating current can help to detect an internal fault. For instance, if N VSCs are connected in parallel, the faulty VSC can be easily detected, since the circulating current is N – 1 times larger than in a healthy VSC. However, if only two VSCs are paralleled, only the fault can be detected because the amplitudes of the circulating currents in each VSC are the same, impeding the location of the faulty VSC by the simple monitoring of the circulating current. However, this can be solved if the system is allowed to be shut down, enabling the identification of the faulty VSC, as presented in the next section.

6.4 Isolation of Internal Faults

6.4.1 Selection of Breakers for Faulty VSC Isolation

As mentioned in Section 6.2, the VSC with internal faults can damage the other healthy VSCs and affect the output voltage unless the VSC can be isolated. To isolate one VSC completely from the system, two methods can be used, as illustrated in Figure 6-8 and Figure 6-9. Compared with the method of placing three breakers on the ac side, only two breakers are needed to isolate the VSC from dc side, but the current rating of the two breakers should be 1.5 times that of the corresponding breakers on the ac side.

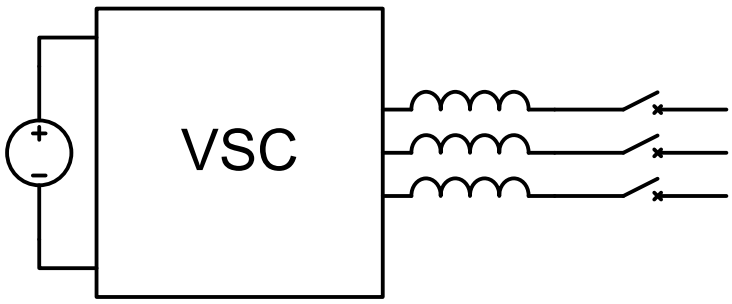

Figure 6-8. Isolate one VSC from system from ac side.

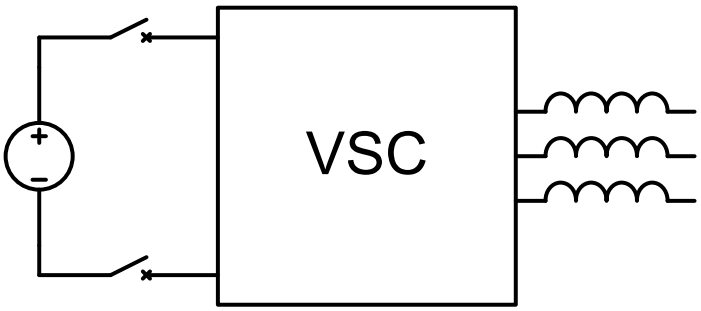

Figure 6-9. Isolate one VSC from system from ac side.

In this chapter, SCRs are adopted as solid-state breakers to isolate the fault VSC from the ac side. One reason for the choice is that the SCRs can be considered to be free, because even though the internal fault is not considered, the SCRs have usually already been involved in isolating the VSC from the ac side to protect the VSC from other faults, such as a dc bus short-circuit fault [12-13]. Another reason for using SCRs as solid-state breakers is that the SCR itself has advantages such as low conduction loss, low cost and light weight. Although the SCR cannot break the dc current, the mechanical dc current breakers are usually not fast enough to block the circulating current before any damage is done, because the current is generated by charging the ac line inductor directly with the dc bus voltage. Fast breakers, such as solid-state breakers, cause some other concerns such as cost and reliability.

6.4.2 System Behavior during Faulty VSC Isolation Procedure

When SCRs are used as breakers, the currents flowing through the SCRs must first be reduced to zero before the SCR is turned off, isolating the fault VSC from the system. However, this condition cannot always be met when the system continues to operate after the fault occurs. For a switch open-circuit fault (as shown in Figure 6-5), after the Sp1 is turned off, i_{A1} will be reduced to and remains at zero, so SCRs can easily isolate the fault

VSC. For a switch short-circuit fault (as shown in Figure 6-5), if the system continues to operate, Sn2 will be turned on, increasing the circulating current. Since the directions of circulating current and i_{A1} are the same in this case, i_{A1} cannot be reduced to zero when Sp2 is turned on. Furthermore, even if Sp2 is turned off, cutting off the circulating current, i_{A1} cannot also be reduced to zero because of the interaction between phase A and the other two phases. As a result, to reduce i_{A1} to zero, the whole system must be shut down.

For a diode short-circuit fault (shown in Figure 6-4), the directions of circulating current and i_{A1} are opposite, so i_{A1} can cross zero, at which point the fault VSC can be isolated using SCRs. However, if the SCR is not turned off before i_{A1} crosses zero, the direction of i_{A1} will be reversed, which means the fault becomes a switch short-circuit fault, and the system must be shut down. This can also be seen in the experiment in Section 6.5.

After the system is shut down, the currents in the ac line inductors decreases exponentially. Such currents can be decomposed into two parts. Taking i_{A1} and i_{A2} as an example, one part flowing to the load is the output current which is the sum of i_{A1} and i_{A2}. The other current flowing between the two phase As is the circulating current, which is the difference between i_{A1} and i_{A2}. The output current will decrease very fast no matter which internal fault occurs, since it is always damped by the load. For the circulating current, the damping loops are different for different internal faults, which are illustrated in Figure 6-10 to Figure 6-12. Figure 6-10 and Figure 6-12 depict switch and diode short-circuit faults, respectively, where the circulating current is damped mainly by the voltage drop across the diodes and the breakers. Therefore the decaying of the current takes a relatively long time, T_{short}, and can be estimated as (6-1), where i is the circulating current

through the faulted phase-leg when the system is shut down, L is the inductance of the output inductor, N is the number of paralleled VSCs, and V_{ave} is the average voltage drop on the diodes and SCRs during the current-damping period.

$$T_{short} = \left(1 + \frac{1}{N-1}\right)\frac{Li}{V_{ave}} \quad \textbf{(6-1)}$$

Figure 6-12, on the other hand, shows the switch open-circuit fault, where the circulating current is limited by the dc source, forcing a very fast current extinction. The time for the extinction, T_{open}, can be estimated as (6-2).

$$T_{open} = \frac{Li}{V_{DC}} \quad \textbf{(6-2)}$$

Since the dc bus voltage V_{DC} is much higher than V_{ave}, T_{open} should be much smaller than T_{short}. The open and short circuit faults can be easily distinguished, helping the identification of the faulty VSC described in Section 6.3.

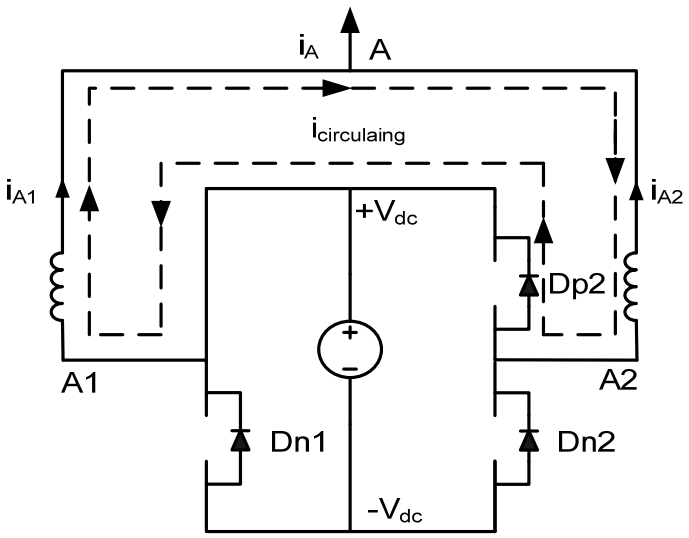

Figure 6-10. Damp of circulating current in switch short circuit fault.

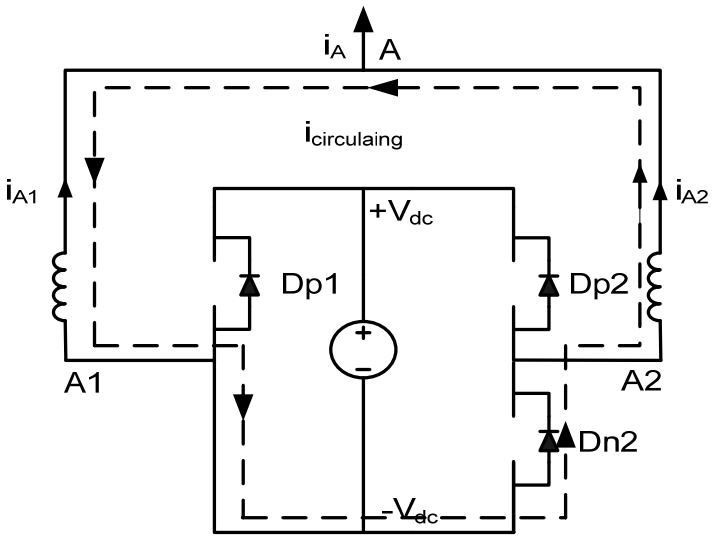

Figure 6-11. Damp of circulating current in switch short circuit fault.

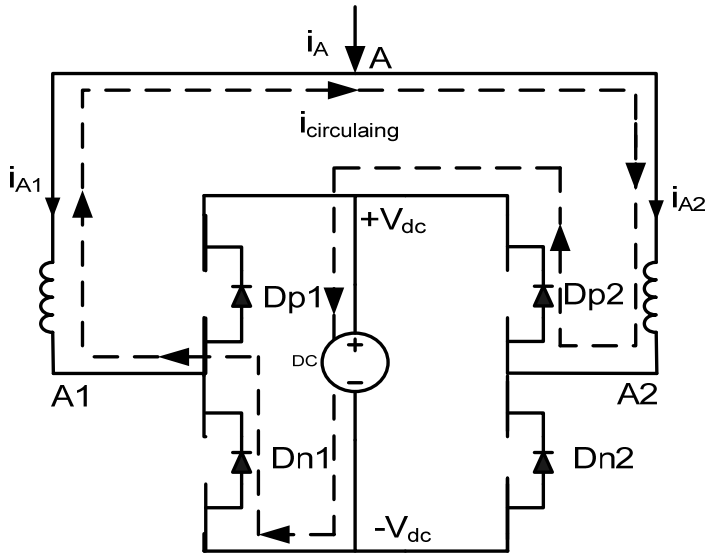

Figure 6-12. Damp of circulating current in switch open circuit fault.

6.4.3 Faulty VSC Isolation and System Recovery

When the amplitude of the circulating current hits the preset limit, the system is shut down. Based on the value of i_{A1} and i_{A2} when the system is shut down, the directions of

output current and circulating current can be obtained and the positive direction is defined in Figure 6-3. If more than two VSCs are used, the faulty VSC can be determined by comparing the amplitudes of circulating currents in each VSC. Assuming VSC1 is identified to be the faulty VSC, if circulating current is positive, Sn1 open circuit fault or Sp1/Dp1 short circuit fault is detected which can further be distinguished by checking the damping speed of such circulating current.

For the system with only two paralleled VSCs, if circulating current is positive and open circuit fault is detected, Sp2 or Sn1 may have open circuit fault. Those two possible faults can be identified by checking the direction of output current. When the output current is positive, Sp2 has open circuit fault. Otherwise, Sn1 has open circuit fault. If circulating current is positive and short circuit fault is detected, Sp1/Dp1 or Sn2/Dn2 short circuit fault may happen. To further identify those two possible faults, the output voltage at point A in the circulating current damping period needs be checked if possible. If the voltage of point A in such period was close to +Vdc, Sp1/Dp1 short circuit fault happened. Otherwise, it is close to –Vdc, showing Sn2/Dn2 short circuit fault happened. If the voltage at point A cannot be measured, some alternative methods can be used. One of them is to turn on the top switches in phase B and C at the same time. If there is current flowing between phase A and the other two phases, the voltage at point A is +Vdc, so Sn2/Dn2 short circuit fault happens. Otherwise, Sp1/Dp1 short circuit fault happens. In a similar way, other short or open circuit faults can be identified.

Based on the analysis, for the paralleled VSCs system with common dc bus and SCR as breakers, system must be shut down to isolate the fault VSC from the system. This is allowed in many applications, for example an aircraft system can be shut down for

as long as 7 seconds under fault conditions [14]. For the applications which are very critical in their operational requirements and do not allow any shut down action, such as a UPS system, the topology with isolated dc bus should be used or SCR should be replaced by other fast breaker with dc current break capability such as power electronics switches.

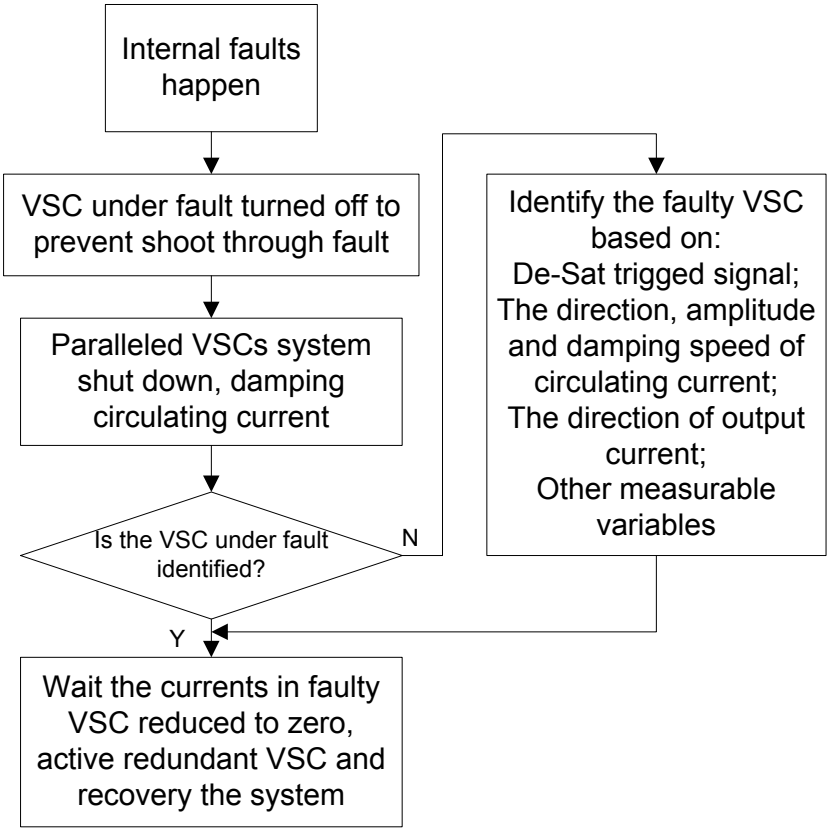

Figure 6-13. Flowchart of internal fault isolation and detection.

Finally, the internal fault detection and protection in this chapter can be summarized in Figure 6-13.

6.4.4 Effect of Coupling Inductors

Another issue worth mentioning is the effect of coupling inductors. To further increase the power density of the paralleled system, interleaving technology can be used and the ac line inductors in the system is designed to be coupled with each other to

maximize the benefit of interleaving [7]. If coupled inductors used as interphase inductors are used (shown in Figure 6-14), the analysis above is still valid, except that the inductance of the circulating current limiting inductor is not constant.

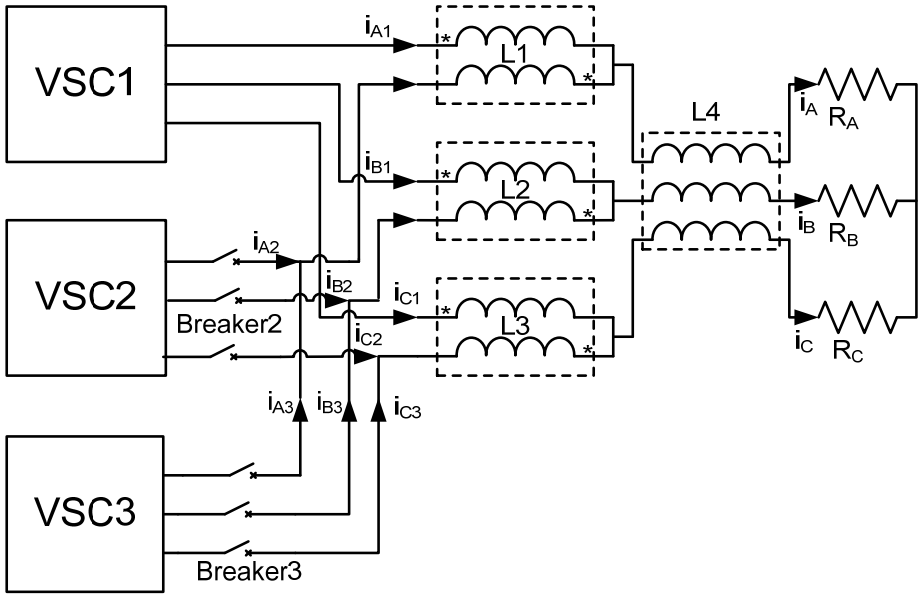

Figure 6-14. System topology with inter-phase inductor for experiment

The inductance of interphase inductors is high at the beginning, but will decrease very quickly after inductor saturation due to the high circulating current. As a result, after internal faults occur and the fault VSC is turned off to prevent a shoot-through fault, the rising slope of the circulating current is very small. But after the interphase inductors are saturated, the increase will be much faster. In fact, when the circulating current increases, the energy stored in interphase inductor is increased, and because the inductances of the interphase inductor (L1, L2 and L3) are much higher than the output inductor (L4), the output current in the phase will be reduced to keep the energy constant. For example, when a diode short-circuit fault occurs, as shown in Figure 6-4, i_{A1} will be reduced because of circulating current. If i_{A2} can be kept the same, the increase of circulating current and the reduction of i_A are the same. Since the inductance of L1 is much higher

than that of L4, the energy will not be constant unless i_{A2} is also reduced. Finally, because of the interphase inductors, i_{A1} and i_{A2} will both have been reduced when the fault occurs, and the interphase inductors are not saturated.

6.5 Experimental Results

To verify the fault analysis, experimental results have been obtained based on the topology shown in Figure 6-14. The experimental setup consists of three 6MBP30RH060 IGBT IPMs (30A 600V), a DSP-FPGA digital controller, three 1.6mH inter-phase inductors (coupling inductors), three 250μH single phase inductor and seven PF480D25 solid state relay(SSR) with SCR output. The ratings of the experiment study are: 160 V dc bus, 50 V and 60 Hz ac bus, 20 kHz switching frequency and 600 W resistor load.

The three IPMs marked as VSC1, VSC2 and VSC3 created a 2+1 paralleled VSC system as shown in Figure 6-14. Six of the SSRs acted as the breaker2 and breaker3 and the last SSR was used to short the output of phase A in VSC2 to negative dc bus as shown in Figure 6-15. In normal operation, breaker 3 is turned off, VSC1 and VSC2 operate together and the total current i_A is shared evenly between i_{A1} and i_{A2}. When the open or short circuit fault happened, VSC2 will be turned off 3μs later to prevent shoot through fault. Then VSC1and breaker2 are turned off to stop the increase of circulating current and damp i_{A2} 200us later. After the system is shut down and VSC2 is isolated from the system completely, VSC1, VSC3 and breaker3 will be turned on to recover the system with a 10 ms interruption.

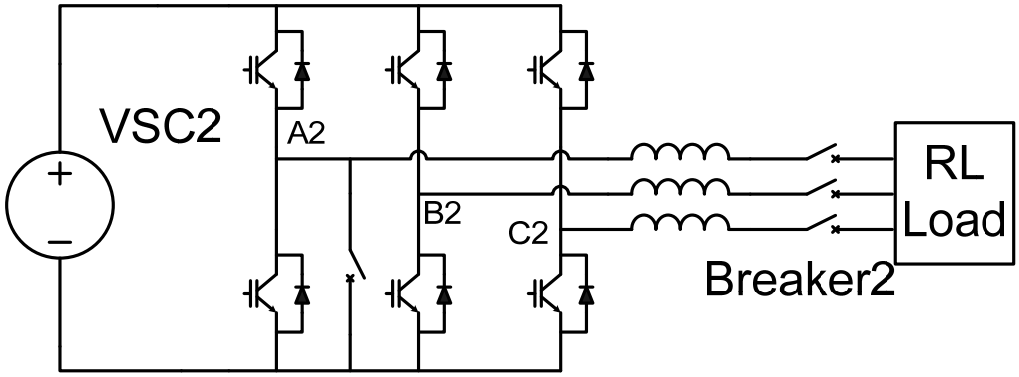

Figure 6-15. Short circuit fault generation for VSC2

The experimental results of Sn2 open circuit and Dn2 short circuit faults are shown from Figure 6-16 to Figure 6-19. Figure 6-17 and Figure 6-19 show the detailed waveforms when the fault happened. From top to bottom the waveforms depicted are: i_{A1}, i_{A2}, i_{A3} and i_A.

From Figure 6-17 and Figure 6-19, when VSC2 is turned off, i_{A1} and i_{A2} will reduce together because of interphase inductors and as analyzed in Section 6.4 the circulating current will increase very fast after a while when interphase inductor is saturated.

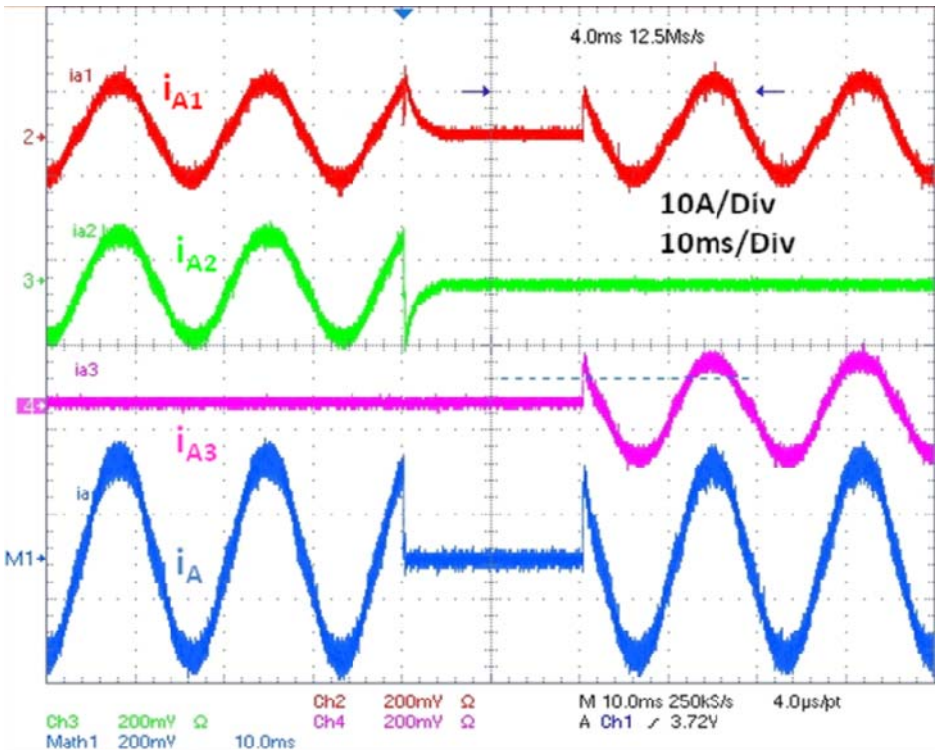

Figure 6-16. Currents in diode short circuit fault.

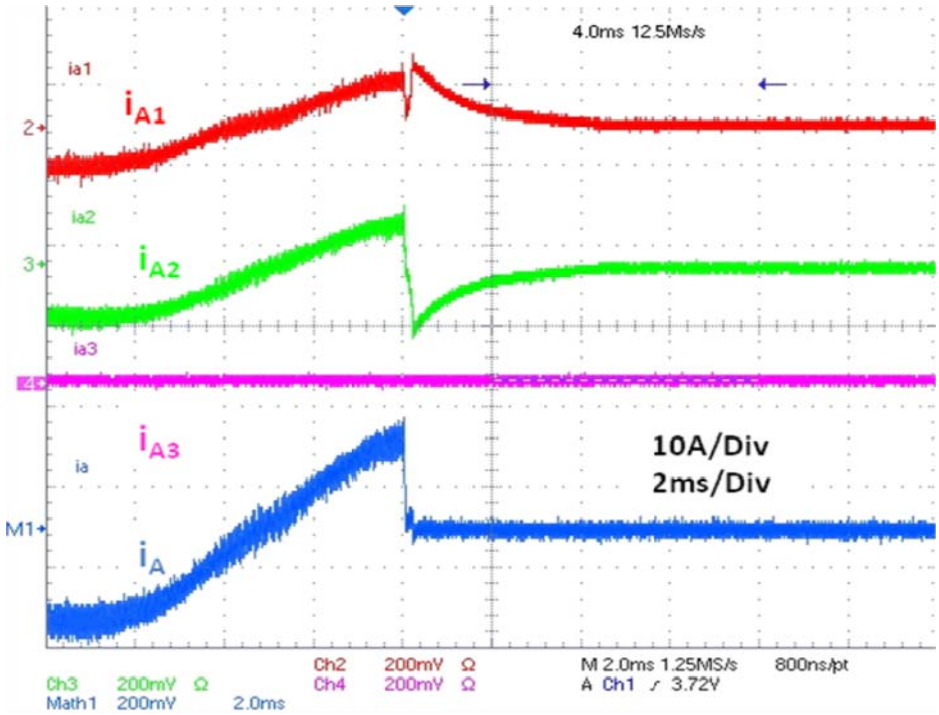

Figure 6-17. Detailed waveforms of currents in diode short circuit fault.

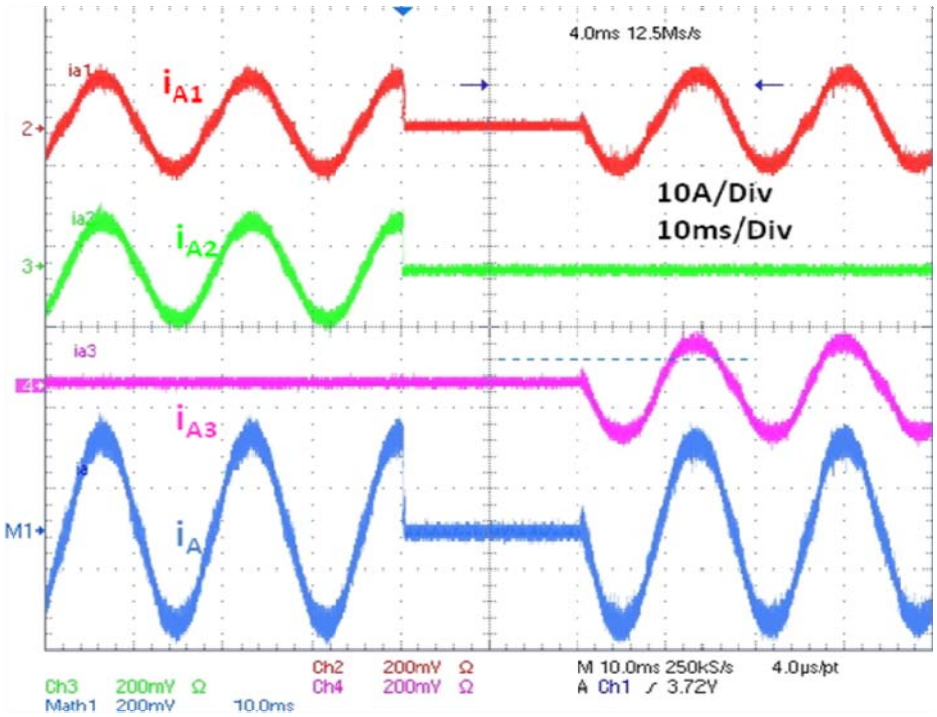

Figure 6-18. Currents in switch open circuit fault.

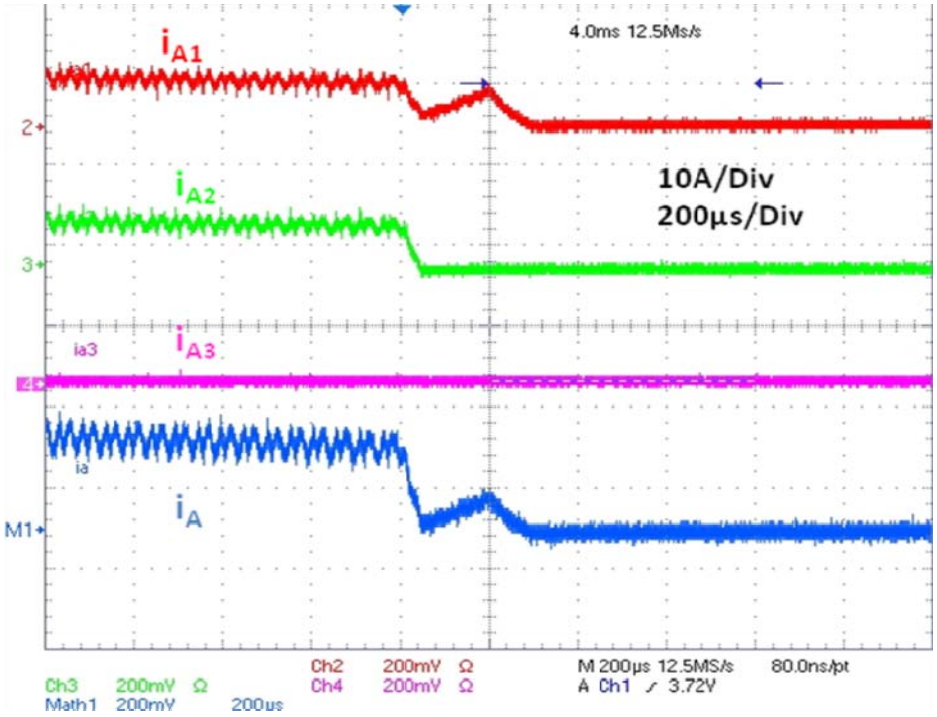

Figure 6-19. Detailed waveforms of currents in switch open circuit fault.

As analyzed above, when a diode short-circuit fault occurs, i_{A2} can cross zero since the directions of the output current and circulating are opposite to each other, which can been seen from Figure 6-17. However, if breaker2 is not turned off on time, as in the experiment, the direction of i_{A2} will be reversed, changing the fault from a diode short-circuit to a switch short-circuit. Because the circulating current in this case is damped by the voltage drop of the SSR and the diodes, a relatively long time (5ms) is needed to isolate VSC2 from the system. Since the circulating current is positive when the system is shut down and this is a short-circuit fault, the Sn2/Dn2 short-circuit fault can be identified, as presented in section 6.4.

When an open-circuit fault occurs, the time to damp the circulating current (100 μs in the experiment) is much shorter than the short-circuit fault case, as predicted. Since the circulating current is positive, based on the analysis, it should be caused by the Sp2 open-circuit fault.

In the experiment, the time delay to shut down and recover the whole system was preset to be a fixed value. The performance of the protection scheme can be improved if the time point of the recovery of the system can be determined by checking the amplitude of i_{A2}, significantly shortening the interruption of i_A.

6.6 Summary

This chapter presents a systematic analysis of the impact of internal faults on paralleled VSCs system, and proposes methods to effectively detect and isolate the faulty devices and converters.

In a system of paralleled VSCs with a common dc bus, internal faults can easily damage other healthy VSCs in the system by creating a circulating current between the

healthy and faulty VSCs. Such faults can be detected by measuring the resultant circulating current or by using the de-sat function of the IGBT gate drives, which also allows the identification of the actual VSC under fault. However, if a conventional breaker or SCR is used to isolate the faulty VSC, the system must be shut down for a short period, which is permissible for certain applications. If a short period of being shut down is not feasible, the topology with an isolated dc bus for each VSC or other breakers should be used, as these can cut off dc current fast enough. Finally, experimental results using a 2+1 VSCs system validate the analysis and protection schemes.

Chapter 7 Conclusions and Future Work

This chapter summarizes the entire dissertation and discusses some ideas for the future work.

7.1 Conclusions

In this dissertation, a systematic methodology to analyze and design a paralleled three-phase VSCs with interleaving is developed. All the analysis and proposed control methods are investigated with the goal of maximizing the benefit of interleaving based on system requirement.

Firstly, a complete analysis studying the impact of interleaving on harmonic currents in ac and dc side passive components for paralleled VSCs is presented. The analysis reveals the principle of asymmetric interleaving, including the impact of interleaving angle on harmonic voltage and currents. The analysis performed considers the effects of modulation index, pulse-width-modulation (PWM) schemes, interleaving angle and displacement angle. Based on the analysis the method to optimize interleaving angle is proposed.

Secondly, to implement interleaving and DPWM together so system power loss and output harmonic currents can be reduced together, the control methods for the CM circulating current of paralleled three-phase VSCs is proposed. With the control methods, DPWM and interleaving, which a desirable combination, but not considered possible, can work together. This method does not depend on the structure of circulating current limit inductor. However, if the integrated inter-phase inductor is used, the total flux in the

inductor can be minimized, by changing the CM circulating current control a little bit. Both of these control methods only introduce very limit additional switching loss.

Thirdly, the converter system with very low switching frequency is studied. Special issues such as beat phenomenon and system unbalance due to non-triplen carrier ratio are explained. And the solutions are proposed such as synchronized PWM and inter-phase interleaving. Other than that, an improved asymmetric space vector modulation (IASVM) is proposed, which can reduce output current total harmonic distortion (THD) as high as 50% for single VSC system especially when modulation is high. By applying such IASVM with interleaving, the THD can be further reduced by half, as well as the amplitude of circulating current. The additional power loss is very limit, especially when system power factor is high.

Fouthly, to increase the system reliability, the impact of internal faults on paralleled VSCs system is analyzed and the methods to effectively detect and isolate the faulty devices and converters are proposed. The impacts of four kinds of single device internal fault are analyzed in detail. Such internal faults can be detected and isolated. With the fault isolation, the paralleled VSCs system can continue work, with increased system reliability.

In addition, a 15 kW three phase ac-dc rectifier is designed and built with SiC devices. With the technologies presented in this dissertation, the specific power density can be pushed more than 2kW/lb. The hardware has been fabricated and under test. Other than that, to meet the calculation requirement, a new digital controller named Nano controller is designed.

7.2 Future Work

In order to further improve the benefit of interleaving, future work can be carried out in the following directions.

1) Even though the analysis about interleaving impact in this dissertation can be extended to N paralleled VSCs, more work are still needed in this areas. The methodology to optimize the interleaving angle for N paralleled VSCs is still not clear, especially if the interleaving angle can be different between each two VSCs. In addition, when more than two VSCs are interleaving, there are still many issues in designing the circulating current limit inductor and the corresponding control methods.

2) The impact of interleaving is mainly limited to the impact on harmonic voltages and currents. How would interleaving affect the system models, such as the control bandwidth and system stability is still not studied. And the impact of CM circulating current is also studied in time domain. The impacts of such control on system models are not clear.

3) The special issues in the system with very low carrier ratio need to be studied further. How to extend the idea of improved ASVM to non-triplen carrier ratio has not been done. And the method to optimize the duration and position of the additional pulses in the system is not so clear.

4) The scheme of internal fault detection and protection can be further improved, especially for diode open fault. And also more experiments are needed to fully verify the feasibility of the proposed protection methods.

APPENDIX

On all of the boards which need to receive or send data by high speed communication bus, one FPGA is used to take charge of the communication task. After considering the function requirement, chip footprint size and cost, the FPGA ECP2M50E-5F672C from Lattice Company is selected. Each FPGA features 8 channels of embedded SERDES which can transfer data between parallel format and series format and can support LVDS up to 3.125GHz. [87] Theses 8 channels of embedded SERDES can meet the requirement of high speed communication between boards in Nano controller. Other than that, each FPGA has 48k 4-input lookup table (LUT), 4Mbits embedded memory, 88 multipliers and 339 IOs, which is enough to meet the system requirement. Each FPGA has a 672 BGA footprint (2.7 cm by 2.7 cm), which is small enough.

For calculation, the TMS320C28346 high-performance floating-point DSP from TI Company is selected. The C28346 delivers 300 MHz of floating-point performance, 516KB of single-access RAM, and PWM modules with 65 picoseconds of resolution. [88] The embedded high resolution PWM generator is the main reason to select this DSP for Nano controller system. Each DSP can output 18 channels of 12bit resolution PWM waveform at 70 kHz. For the paralleled structure, only 12 channels PWM are needed and for the high power density rectifier 12 bit resolution PWM is good enough. If really high resolution PWM signals are needed, the DSP can alternately generate 4 channels PWM signals with 60ps which means 12 bit resolution at 4MHz or 14 bits resolution at 1MHz. Even though for future project, the calculation speed is not fast enough, this DSP can at

least be used a PWM generator in the Nano controller system. The footprint of each DSP chip is 256 BGA, which is only 1.7 cm by 1.7 cm.

High speed high resolution AD chips are also desirable to increase the system control accuracy. LTC1407 AD chip from LINEAR Technology company is selected. Each chip has 3Msps sampling ADC with two simultaneous differential inputs. [89] In other words, for each chip, one system analog signal can be sampled and converted into digital signal at the speed of up to 3Msps. Or two system analog signals can be sampled and converted into digital signal at the speed of up to 1.5Msps. The resolution is 14bits, which is high enough for most of the power electronics projects. In addition, this AD chip has 80dB CM rejection at 100 kHz and 14 mw low power dissipation, with the footprint size only 3.2mm by 5 mm. All of these outstanding features make this AD the choice in Nano controller.

The power supply board show in Figure 4-5 is designed to support up to four boards in the system. PFX40-48WD15 DC-DC converter from TDK-Lambda company is used which can output +/- 15V voltage with 40W. Since the pin density is too high to use the PWM signals from DSP board directly and buffer function is desired to increase the signal driving capability, the PWM signals are connected to the power supply board first and then sent to power stage through buffer chips.

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