Fully Distributed Control and Its Analog IC Design For Scalable Multiphase Voltage Regulators

Xin Zhang

Dissertation submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy

in

Electrical Engineering

Alex Q. Huang, Co-Chairman
James Thorp, Co-Chairman
Dong S.Ha
Robert W. Hendricks
Fred C. Lee
Douglas K Lindner
Jacobus Daniel van Wyk

November 1, 2005

Blacksburg, Virginia

Keywords: Distributed Control, Analog IC,

Scalable, Multiphase Voltage Regulator

Fully Distributed Control and Its Analog IC Design For Scalable Multiphase Voltage Regulators

Xin Zhang

(ABSTRACT)

Modern microprocessors require low supply voltage (about 1V), but very high current (maximum current is 300A in servers, 100A in desktop PCs and 70A in notebook PCs), and tighter voltage regulation. However, the size of a CPU Voltage Regulator (VR) needs to be reduced. To achieve much higher power density with decent efficiency in VR design is a major challenge. Moreover, the CPU current rating can vary from 40A to 300A for different kinds of computers, and CPU power supply specifications change quickly even for the same type of computers. Since the maximum power rating of one channel converter is limited, the VR channel number may vary over a large range to meet VR specifications. Traditionally, VR design with different channel numbers needs different types of VR controllers. To reduce the developing cost of different control ICs, and to maximize the market share of one design, scalable phase design based on the same type of IC is a new trend in VR design.

To achieve higher power density and at the same time to achieve scalable phase design, the concept of Monolithic Voltage Regulator Channel (MVRC) is introduced in this dissertation. MVRC is a power IC with one channel converter's power MOSFETs, drivers and control circuitries monolithically integrated based on lateral device technology and working at high frequency. It can be used alone to supply a POL (Point of Load). And without the need for a separate master controller, multiple MVRC chips can be paralleled together to supply a higher current load such as a CPU.

To make MVRC a reality, the key is to develop a fully distributed control scheme and its associated analog IC circuitry, so that it can provide control functions required by microprocessors and the performance must be equal or better than a traditional a centralized VRM controller. These functions includes: multiphase interleaving, Adaptive Voltage Position (AVP) and current sharing.

To achieve interleaving, this dissertation introduces a novel distributed interleaving scheme that can easily achieve scalable phase interleaving without channel number limitation. Each channel's interleaving circuitry can be monolithically integrated without any external components. The proposed scheme is verified by a hardware prototype. The key building block is a self-adjusting saw-tooth generator, which can produce accurate saw-tooth waveforms without trimming. The interleaving circuit for each channel has two self-adjusting saw-tooth generators. One behaves as a Phase Lock Loop to produce accurate phase delay, and the other produces carrier signals.

To achieve Adaptive Voltage Position and current sharing, a novel distributed control scheme adopting the active droop control for each channel is introduced. Verified by hardware testing and transient simulations, the proposed distributed AVP and current sharing control scheme meets the requirements of Intel's guidelines for today and future's VR design. Monte Carlo simulation and statistics analysis show that the proposed scheme has a better AVP tolerance band than the traditional centralized control if the same current sensing scheme is used, and its current sharing performance is as good as the traditional control.

It is critical for the current sensing to achieve a tight AVP regulation window and good current sharing in both the traditional centralized control scheme and the proposed

distributed control scheme. Inductor current sensing is widely adopted because of the acceptable accuracy and no extra power loss. However, the Signal-to-Noise Ratio (SNR) of the traditional inductor current sensing scheme may become too small to be acceptable in high frequency VR design where small inductor with small DCR is often adopted. To improve the SNR, a novel current sensing scheme with an accurate V/I converter is proposed. To reduce the complexity of building an accurate V/I converter with traditional Opamps, an accurate monolithic transconductance (Gm) amplifier with a large dynamic range is developed. The proposed Gm amplifier can achieve accurate V/I conversion without trimming.

To obtain further verification, above proposed control schemes are monolithically integrated in a dual channel synchronous BUCK controller using TSMC BiCMOS 0.5um process. Testing results show that all the proposed novel analog circuits work as expected. System testing results show good interleaving, current sharing and AVP performance. The silicon size of each channel is $1800\times1000um^2$.

With proposed current sensing, interleaving, AVP and current sharing, as well as their associated analog IC implementations, the technical barriers to develop a MVRC are overcome. MVRC has the potential to become a generic power IC solution for today and future POL and CPU power management.

The proposed distributed interleaving, AVP and current sharing schemes can also be used in any cellular converter system. The proposed analog building blocks like the self-adjusting saw-tooth generator and the accurate transconductance amplifier can be used as basic building blocks in any DC-DC controller.

TO MY WIFE

Ji Pan

ACKNOWLEDGMENTS

I would like to express my greatest appreciation to my advisor, Dr. Alex Huang, for his guidance and support throughout my graduate study and research. His extensive knowledge, broad vision and creative thinking have been a source of inspiration for me through my entire study and research work.

I am grateful to my committee members Dr. Dong S.Ha, Dr. Robert W. Hendricks, Dr. Fred C. Lee, Dr. Douglas K Lindner, Dr. Jacobus Daniel van Wyk and Dr. James Thorp for their valuable discussions, encouragement and comments on my research.

The first three-year of my PHD study was at CPES of Virginia Tech. Especially, I would like to thank Dr. Ming Xu and Dr. Gary Yao for their help and guidance. I have known them for more than 10 years since I entered the power electronics lab at Zhejiang University for my master degree study in 1994. They are the best in the field and I learned a lot from them. I also would like to thank my old friends Dr. Gang Chen, Dr. Peng Xu, Dr. Jingdong Zhang and Dr. Shuo Wang. I get help from them even before I came to America.

Special thanks also go to Mr. Maurice Chee, my intern advisor at HiPAC Semiconductor in Silicon Valley. He successfully transferred me from an application engineer to an IC designer, which could be my future career. Mr. George Chen, the CEO, is another good teacher for me. He teaches me not only analog IC design, but also his philosophy about career and life. Thank Ms. Wendy Lee very much. Without her excellent layout, I would not be able to get result from my testing chip. And thank to Mr. Raphael Liu, my living analog textbook and Mr. Tom Jiang, my living digital textbook.

My advisor transferred to North Carolina State University as the director of Semiconductor Power Electronics Center in the late 2004. Therefore, the last phase of my Ph.D. study is at SPEC of NCSU, where I work with a group of ambitious young people. The following is the list of this awesome individuals: Mr. Xiaoming Duan, Mr. Jinseok Park, Mr. Ding Li, Mr. Hongtao Mu, Mr. Ning Zhu and Ms. Xiaojun Xu.

I am indebted to all the faculty, staff, engineer and students at CPES, HiPAC and SPEC for their support and friendship, which made my Ph.D. study pleasant and enjoyable. I would like to thank Dr. Jinrong Qian, Mr. Dengming Peng, Mr. Mao Ye, Dr. Changrong Liu, Dr. Qun Zhao, Dr. Jianjun Liu, Dr. Yunfeng Liu, Dr. Peter Barbosa, Dr. Francisco Canales, Dr. John Tero, Dr. Bo Yang, Dr. Zhenxian Liang, Mr. Steve Chen, Mr. Dan Huff, Mr. Gary Kerr, Ms. Linda Gallagher, Dr. Linyin Zhao, Mr. Jingeng Qian, Dr. Zhengxue Xu, Dr.Yuming Bai, Dr. Bin Zhang, Mr. Yu Meng, Mr. Nick Sun, Dr. Xuening Li, Dr. Haifei Deng, Ms. Li Ma, Ms. Qian Liu, Ms. Huiyu Zhu, Mr.Julu Sun, Mr. Xiangfei Ma, …

My heartfelt appreciation goes toward my parents, who have always encouraged me to pursue higher education. With much love, I would like to thank my beautiful wife, who has always been there for me with her devoted love and encouragement.

TABLE OF CONTENTS

Chapter 1. Monolithic Voltage Regulator Channel…..……1

1.1. The Challenges of Microprocessor Power Management ……..1

1.2. The Technology Trend for Microprocessor Power Supply Design ……..9

1.3. The Concept of Monolithic Voltage Regulator Channel ..……..13

1.4. Research Scope and Dissertation Outlines …… 22

Chapter 2. Distributed Interleaving ...…….25

2.1. Interleaving ---- Benefits and Requirements ……..25

2.2. Issues of Centralized Interleaving Schemes ……...30

2.3. Issues of Reported Distributed Interleaving Schemes ..…….32

2.4. A Novel Distributed Interleaving Scheme ……..37

2.5. The Key Building Block ---- A Self-Adjusting Saw-tooth Generator …39

2.6. Hardware Verification of the Proposed Interleaving Scheme ……...43

2.7. Summary of Chapter 2…….46

Chapter 3. Distributed Adaptive Voltage Position and Current sharing……47

3.1. AVP and Current Sharing Design Specifications ..…….47

3.2. Investigation of Traditional AVP and Current Schemes ……53

3.3. Issues of Centralized AVP and Current Sharing Schemes…….…..…61

3.4. A Novel Distributed AVP and Current Sharing Scheme ..…….67

3.5. AVP and Current Sharing Tolerance Analysis ..……84

3.6. AVP and Current Sharing Monte Carlo Simulation ……111

3.7. Hardware Verification of the Proposed AVP and CS Schemes ..……116

3.8. Summary of Chapter 3……128

Chapter 4. Improved Inductor Current Sensing ..……..129

4.1. Reviews of Current Sensing Approaches in VR Applications ...……129

4.2. Issues of Traditional Inductor Current Sensing Schemes ……139

4.3. A Novel Current Sensing Scheme Adopting a V/I Converter ……..147

4.4. The Key Block ---- A Monolithic Accurate Gm Amplifier …….….152

4.5. Other Applications of the Gm Amplifier ……..160

4.6. The Concept of Power Stage Emulator ……..162

4.7. Summary of Chapter 4…….164

Chapter 5. Silicon Verification of Proposed Analog Blocks and Control Schemes……165

5.1. Proposed MVRC Chip ..…….165

5.2. Testing Chip Diagram ……168

5.3. Design Methodology ..……171

5.4. Layout and Die Photo …….……175

5.5. Block Testing Results ...……..177

5.6. System Testing Results ……...183

5.7. Summary of Chapter 5……..……188

Chapter 6. Summary and Future Work ……...189

6.1. Conclusion of the Dissertation ……189

6.2. Future Work ……...191

References…….……...193

Vita……...203

LIST OF FIGURES

Fig. 1-1. One channel synchronous BUCK converter……..…2
Fig. 1-2. Multi-channel interleaving BUCK converter……3
Fig. 1-3. VRs on the motherboard……...5
Fig. 1-4. A typical VR implementation……...6
Fig. 1-5. VR designs with different channel number……..7
Fig. 1-6. FOM values of VR devices..……..…9
Fig. 1-7. Volterra's VT1102 solution..……..10
Fig. 1-8. IR's Xphase solution……..…….11
Fig. 1-9. Traditional centralized control architecture..……..13
Fig. 1-10. Integration with the traditional centralized control architecture……...14
Fig. 1-11. Partially distributed control architecture……...15
Fig. 1-12. Integration with the partially distributed control architecture……...16
Fig. 1-13. Fully distributed control architecture……....18
Fig. 1-14. Integration with fully distributed control architecture ---- MVRC……...19
Fig. 1-15. Research purpose……...…21
Fig. 1-16. Research scopes…….22
Fig. 2-1. Topology of N-channel synchronous buck converter…….25
Fig. 2-2. Current ripple reduction in interleaving buck converter…….26
Fig.2-3. The impact of phase shift error……28
Fig. 2-4. The impact of un-ideal carrier signal……29, 30
Fig. 2-5. Traditional centralized interleaving scheme……...31
Fig.2-6. Distributed interleaving scheme proposed by Perreault's paper……..32
Fig.2-7. Distributed interleaving scheme proposed by Feng's paper……..33, 34
Fig. 2-8 distributed interleaving scheme proposed by Huang's paper……35, 36
Fig. 2-9. A novel distributed interleaving scheme…….37
Fig. 2-10. Implementation of the voltage controlled phase delay block……...38
Fig. 2-11. A self-adjusting saw-tooth generator……..……..39
Fig. 2-12. Simulated waveforms of the self-adjusting saw-tooth generator……..40
Fig. 2-13. Photo of the 3-channel interleaving hardware……..43

Fig. 2-14. Testing results of 2 phase interleaving……...43, 44
Fig. 2-15. Testing results of 3 phase interleaving…….44
Fig. 3-1. A lumped model for CPU power delivery……..49
Fig. 3-2.Transient with and without AVP……..50
Fig. 3-3. CPU die's AVP window and VRM AVP window……..51
Fig. 3-4. AVP transient at different locations of the power delivery loop……51
Fig. 3-5. Transient response when the processor runs a testing program……..51
Fig. 3-6. Generic VR architecture…….…54
Fig. 3-7. Classification of VR control approaches……55
Fig. 3-8. Peak current modulation……..…….…56
Fig. 3-9. Valley current modulation……....57
Fig. 3-10. Charge modulation……...57
Fig. 3-11. Voltage error signal adjustment for each channel……57
Fig. 3-12. Saw tooth signal adjustment for each channel…….58
Fig. 3-13. Enhanced V^2 modulation……..58
Fig. 3-14. Compensator implementation based on Opamp……...59
Fig. 3-15. Compensator implementation based on OTA……..59
Fig. 3-16. AVP approach 1……61
Fig. 3-17. AVP approach 2……63
Fig. 3-18. Current sharing approach 1……...64
Fig. 3-19 Current sharing approach 2……65
Fig. 3-20. Different AVP approaches……..67, 68
Fig. 3-21. One channel active droop control…….70
Fig. 3-22. The small signal model of VRM power plant……...70
Fig. 3-23. AVP design scheme……..72
Fig. 3-24. The simplified model with active droop control……..73
Fig. 3-25. Constant output impedance design with $\omega c = \omega\_cap$ ……74
Fig. 3-26. A practical AVP design strategy……..74
Fig. 3-27. Multi-channel active droop control…….76
Fig. 3-28. Redrawn Multi-channel active droop control……..77
Fig. 3-29. Current sharing with droop control……..78

Fig. 3-30. Impact of Vref tolerance on the current sharing……..79
Fig. 3-31. Tie each channel's Vref together to achieve better current sharing…….80
Fig. 3-32. Current sharing with scheme shown in Fig. 3-35…….80
Fig. 3-33. Impact of current sensing gain tolerance on the current sharing……..81
Fig. 3-34. Proposed MVRC solution for CPU power management……..82
Fig. 3-35. Transient simulation results……..83
Fig. 3-36. General steps to do worst case analysis……85
Fig. 3-37. General steps to do standard error analysis……..86
Fig. 3-38. Combination of worst case analysis and standard error analysis……..87
Fig. 3-39. Steady state model for the traditional AVP scheme……..88
Fig. 3-40. Steady state model for proposed AVP scheme…….92
Fig. 3-41. Monte Carlo simulation results: AVP at steady state…….114
Fig. 3-42. Monte Carlo simulation results: AVP transient……..115
Fig. 3-43. Monte Carlo simulation results: current sharing…….115
Fig. 3-44. Design specifications……..116
Fig. 3-45. Photo of hardware……...117
Fig. 3-46. Voltage regulation of 2 phase VR with the proposed control
and resistor current sensing…….118
Fig. 3-47. Load lines of 2 phase VR with the proposed control
and resistor current sensing……..118
Fig. 3-48. Current sharing of 2 phase VR with the proposed control
and resistor current sensing……..119
Fig. 3-49. AVP transient of 2 phase VR with the proposed control
and resistor current sensing……..120
Fig. 3-50. Voltage regulation of 2 phase VR with the proposed control
and inductor current sensing……120
Fig. 3-51. Load lines of 2 phase VR with the proposed control
and inductor current sensing……121
Fig. 3-52. Current sharing of 2 phase VR with the proposed control
and inductor current sensing……121, 122
Fig. 3-53. AVP transient of 2 phase VR with the proposed control

and inductor current sensing……122
Fig. 3-54. Voltage regulation of 3 phase VR with the proposed control
and resistor current sensing……..123
Fig. 3-55. Load lines of 3 phase VR with the proposed control
and resistor current sensing……..123
Fig. 3-56. Current sharing of 3 phase VR with the proposed control
and resistor current sensing……..124
Fig. 3-57. AVP transient of 3 phase VR with the proposed control
and resistor current sensing……..125
Fig. 3-58. Voltage regulation of 3 phase VR with the proposed control
and inductor current sensing……125
Fig. 3-59. Load lines of 3 phase VR with the proposed control
and inductor current sensing……126
Fig. 3-60. Current sharing of 3 phase VR with the proposed control
and inductor current sensing……126, 127
Fig. 3-61. AVP transient of 3 phase VR with the proposed control
and inductor current sensing……127
Fig. 4-1. Current sensing by sensing resistor……...129
Fig. 4-2. Current sensing by Inductor DCR……130
Fig. 4-3. Current sensing by power MOSFET on resistance……...131
Fig. 4-4. Current sensing by sensing FET……132
Fig. 4-5. A popular improved version of sensing FET scheme……...134
Fig. 4-6. Current sensing by sensing transformers……..134
Fig. 4-7. Current sensing by Midya's scheme……135
Fig. 4-8. Current sensing by Zhou's scheme……...135
Fig. 4-9. Current sensing by Forghani-zadeh's scheme……...137
Fig. 4-10. Inductor current sensing from signal processing point of view……..139
Fig. 4-11. Key waveforms of inductor current sensing……...140
Fig. 4-12. Impact of amplifier's input impedance on inductor current sensing……...140
Fig. 4-13. An improved version of differential amplifier……....141
Fig. 4-14. Major noise sources for the inductor current sensing……142

Fig. 4-15. Simplified noise model of inductor current sensing……143
Fig. 4-16. Semtech's current sensing scheme……..145
Fig. 4-17. Key waveforms of Semtech's current sensing scheme……...145
Fig. 4-18. Proposed current sensing scheme adopting a V/I converter……...147
Fig. 4-19. Simplified noise model of proposed current sensing scheme…….148
Fig. 4-20. Key waveforms of the proposed current sensing scheme……...149
Fig. 4-21. Simulation results with the proposed current sensing scheme……150
Fig. 4-22. Implementation of V/I converter with Opamps……..151
Fig. 4-23. Proposed current sensing scheme hardware testing results…….151
Fig. 4-24. Basic configuration of an OTA……...154
Fig. 4-25. Fixed Gm with the floating resister…….156
Fig. 4-26. Gain cell transconductor……..156
Fig. 4-27. Enhanced gain cell transconductor……..157
Fig. 4-28. Accurate enhanced gain cell transconductor……...158
Fig. 4-29. A Gm amplifier based on Opamp and current mirror…….158
Fig. 4-30. Simulation results with the proposed sensing scheme and Gm block…….159
Fig. 4-31. Resister current sensing with Gm amplifier……160
Fig. 4-32. Inductor current sensing with Gm amplifier……...160
Fig. 4-33. AVP configuration with Gm amplifier and resistor current sensing……...161
Fig. 4-34. AVP configuration with Gm and original inductor current sensing……...161
Fig. 4-35. AVP configuration with Gm amplifier and the proposed current sensing…..161
Fig. 4-36. Current sensing with a power stage emulator…….162
Fig. 5-1. Proposed MVRC solution for CPU power management……..166
Fig. 5-2. Proposed MVRC chip supplying a POL……...167
Fig. 5-3. Block diagram of the testing chip…….169
Fig. 5-4. A typical power management IC design flow in industry…….171
Fig. 5-5. The concept of partial tree design in HDL……172
Fig. 5-6. Generic hierarchy for dc-dc controller design……..173
Fig. 5-7. Proposed design approach for a DC-DC controller……..174
Fig. 5-8. The chip layout……..175
Fig. 5-9. The die photo…….176

Fig. 5-10. Die photo of the proposed analog blocks……176
Fig. 5-11. Testing chip in DIP28 package……...177
Fig. 5-12. Testing results of the distributed interleaving block……..178, 179
Fig. 5-13. Testing results of the proposed Gm amplifier…….180, 181
Fig. 5-14. Testing results of the voltage reference block…….182
Fig. 5-15. Testing chip in SOIC28 package…….183
Fig. 5-16. The application circuit for the testing chip……..183
Fig. 5-17. The photo of the demo board of the testing chip…….184
Fig. 5-18. Voltage regulation of the testing chip demo board…….185
Fig. 5-19. Load lines of the testing chip demo board……..185
Fig. 5-20. Current sharing of the testing chip demo board……..186
Fig. 5-21. AVP transient of the testing chip demo board……187

LIST OF TABLES

Table 1-1. Potential benefits of the MVRC approach for customers……20
Table 1-2. Potential benefits of the MVRC approach for manufacturers……..21
Table 2-1. Summary of the exist interleaving scheme……...36
Table 3-1. Summary of some popular VRM controllers……...60
Table 3-2. Transfer functions……71
Table 3-3. Parameters used in tolerance analysis……108
Table 3-4. Equations based on worst case analysis……109
Table 3-5. Equations based on stochastic analysis……..109
Table 3-6. Design examples based on the calculation in table 3-5……..110
Table 3-7. Monte Carlo simulation setup……113
Table 3-8. Summary of current sharing of 2 phase VR with the proposed control and resistor current sensing……..119
Table 3-9. Summary of current sharing of 2 phase VR with the proposed control and inductor current sensing……122
Table 3-10. Summary of current sharing of 3 phase VR with the proposed control and resistor current sensing……..124
Table 3-11. Summary of current sharing of 3 phase VR with the proposed control and inductor current sensing……127
Table 4-1. Summary of current sensing approaches……138
Table 5-1. Summary of the performance of the distributed interleaving block……..179
Table 5-2. Design parameters used in the demo board……....184
Table 5-3. Summary of current sharing of the testing chip demo board……187

Chapter 1. Monolithic Voltage Regulator Channel

1.1. The Challenges of Microprocessor Power Management

1.1.1. Power Requirements of Microprocessor

In 1965, just six years after the invention of the integrated circuit (IC), Gordon Moore predicted the annual doubling of the number of transistors integrated in integrated circuits [A1]. In the late 1980s, the doubling speed was adjusted to every 18 months for the expected increases in the complexity of semiconductors [A2]. Moore's Law has remained valid for 4 decades [A3]. It has been recognized as the vision, driving force and roadmap setter for the trillion-dollar semiconductor and electronics industry. Moore's Law will continue prevailing at least for the next decade, with continuous advancement in processing technologies for Very Large Scale Integration (VLSI) [A4].

Not only the device counts rising, nearly all the parameters of microprocessor technology improve as transistor counts climb according to Moore's law [A5].

For example, microprocessor speed and performance have ascended even more sharply than has the number of transistors. The i486 processor ran at 25 MHz, but today's Pentium IV processors run at 2.20 GHz, and the predicted billion-transistor processor in will likely run at speeds approaching 20 GHz.

The consequence of higher transistor counts and higher clock frequency is higher power consumption [A6]. For mainstream CPU in desktop PCs, although the core voltage is scaled down to 1V, the current rising quickly to 100A results the total power consumption up to 100W for the CPU in desktop PCs [A7]. And the power consumption of a server CPU is much larger than that of the desktop CPU.

1.1.2. Evolution of Microprocessor Power Management

For a 386 or 486 processor, the CPU uses standard 5V Vdd. The power directly comes from the silver box. Starting with Intel Pentium microprocessors, which were released in 1990, microprocessors begin to use a nonstandard supply of less than 5V. A dedicated non-isolated DC-DC converter called Voltage Regulator Module (VRM) is put beside the CPU socket to power the microprocessor. The original version of the VRM that accompanied the Pentium I and Pentium II was made up of a simple 5V input BUCK converter, as shown in Fig. 1-1.

The Pentium III processor was released in 1999. Compared to the Pentium II, the operating voltage was drastically reduced from 2.8V to 1.5V, and the current was increased from 10A to 30A, and the current slew rate was increased from 1A/ns to 8A/ns [A8]. The simple approach of one channel BUCK is not practical to power Pentium III processor [A9] [A10]. This is simply because that not enough real estates is available on the motherboard accommodate the increased bulk capacitors to meet Pentium III's tighter regulation window. Secondly, the cost increase due to the bulk capacitors is also not acceptable.

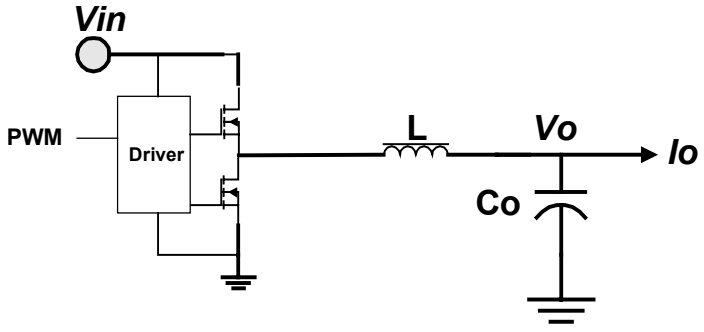


Fig. 1-1. One channel synchronous BUCK converter.

Fortunately, researchers in Center of Power Electronics System (CPES) at Virginia Tech proposed a better solution for the microprocessor power supply in early 1997.

Instead of paralleling a number of transistors to increase power rating, the team proposed paralleling circuits. The new solution is widely called as multi-channel interleaving synchronous BUCK converter [A11]. Fig. 1-2 shows such topology.

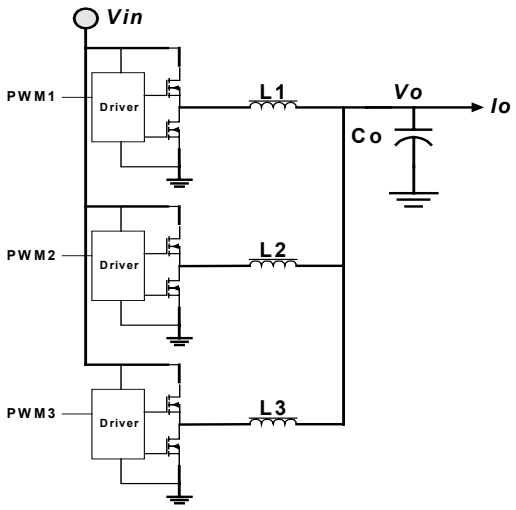


Fig. 1-2. Multi-channel interleaving BUCK converter.

With multi channels of synchronous BUCK cells in parallel, each cell can use an inductor that is about 1/10 smaller than the inductor used in the original one channel BUCK converter, and the minimum number of output capacitance to meet transient requirement is dramatically reduced without sacrificing the efficiency. Moreover, with the interleaving operation, the minimum number of output capacitance to meet steady-state voltage ripple requirement is also dramatically reduced because of current ripple cancellation effect. In the same way, the interleaving approach can also significantly reduce the input filter capacitor requirement.

Multi-channel approach can also benefit the thermal design because the power loss is more evenly distributed on the board. And its power scalability characteristic makes it very attractive in terms of its ability to keep up with the future microprocessor power management design.

As a result, industry quickly adopted this solution. A number of companies (National Semiconductor, Semtech, Intersil, Maxim, Linear Technology, Analog Device, Fairchild Semiconductor, Texas Instruments and ST Microelectronics) have developed their IC controllers to facilitate the implementation of the proposed multi channel approach [A12]. And today, multi-channel interleaving synchronous BUCK converters become an industry standard.

After the introduction of multi-channel interleaving synchronous BUCK converter, there is little new evolution on the VR power stage. The only major change was the input voltage of VR. The input bus voltage was changed from 5V to 12V in order to reduce the input bus conduction loss that run across the motherboard [A13]. After Pentium IV processor was released in 2004, all the VR products use multi-channel interleaving synchronous BUCK converters with 12V input voltage as the power stage.

However, there are a number of improvements in VR controllers. The first generation of multiphase VR controller only provided interleaving and pure voltage loop control, which is already enough to meet Intel's design guidelines. Active current sharing between each channel is introduced later, and then the Adaptive Voltage Position specifications are added [A14]. Adaptive Voltage Position means the dc output voltage of a converter is dependent on its load. It is set to the highest level within the specification window at no-load condition and to the lowest level at full load condition. This approach increases the output voltage dynamic tolerance by as much as twofold, which thus reduces the number of bulk capacitors required to meet the output voltage regulation. More importantly, it reduces the average power the microprocessor or DSP consumes, therefore reduces the cost on thermal design. Today, to meet newest Intel's design

guidelines, interleaving, current sharing and AVP are three basic functions the VR control chip needs to provide.

1.1.3. Challenge 1: to Achieve Higher Power Density

Microprocessor power management design is a tradeoff among efficiency, thermal, size, and costs under the constraint of required voltage regulation window [A15]. Today's VR products are the results of such tradeoff. Today's VRs use discrete 30V trench MOSFETs as power devices. The switching frequency is 300~500KHz. And a lot of electrolytic (Oscon) capacitors are adopted to meet the tight regulation window. [A16]

Driving by the customer and market, computers become more and more powerful while the computer size becomes smaller and smaller. However, the size of the VR changes in the opposite direction. The power consumption of today's mainstream microprocessor has already reached 1.6V/50A in laptops, 1.2V/80A in desktops and 1.0V/200A in severs. As shown in Fig. 1-3, to delivery enough power to the CPU, the VR occupies 12~15% area on the motherboard. To achieve higher power density is an immediate challenge in microprocessor power management.

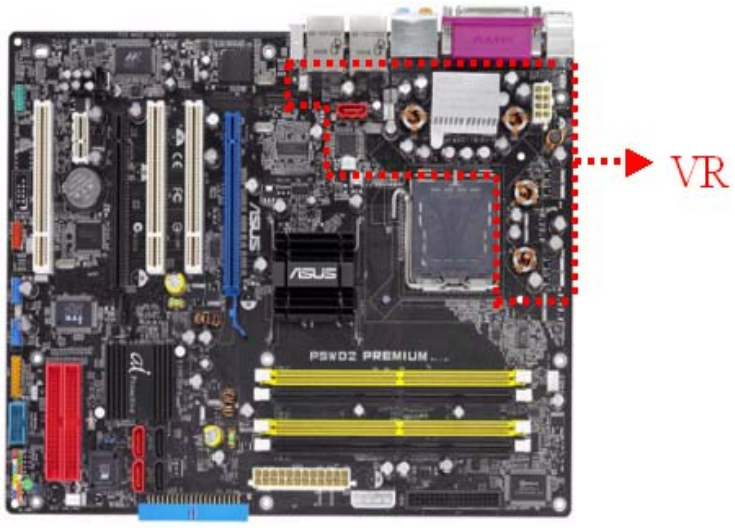
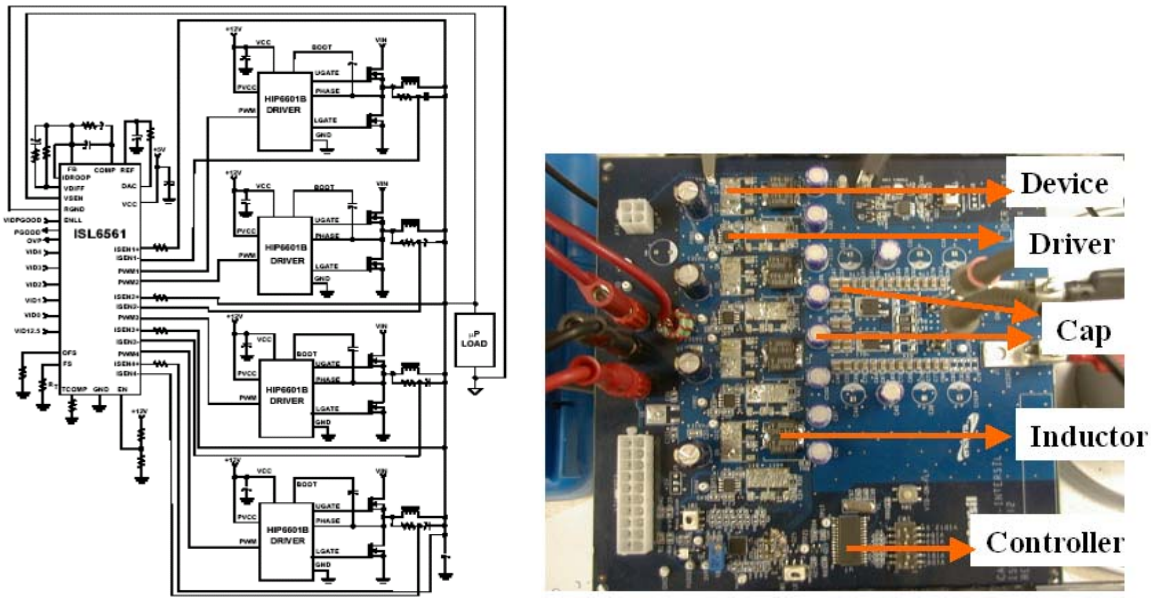


Fig. 1-3. VR on a typical motherboard.

This challenge may become prohibitive in the future. Following Intel's roadmap, in 2010 the processor will run at 20GHz clock frequency with over one-billon transistors. It will require more than 200A current at a voltage level of around 0.7 V [A17]. To build a 0.7V/200A VR with today's approach will occupy more than 30% motherboard area. It is not acceptable.

The introduction of multi-core technology in microprocessor may temporarily solve the issue and it is just for some certain types of microprocessors. In the long run, Moore's Law will continue prevailing for at least the next decade. To achieve higher power density in VR design will continue to be the main challenge.

1.1.3 Challenge 2: to Achieve Scalable Phase Design



a. Typical application of ISL6561

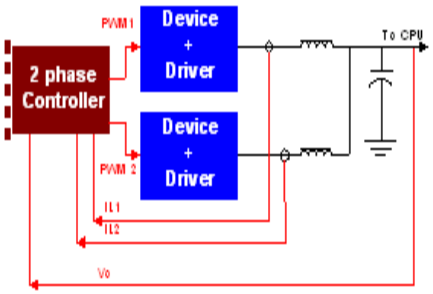
b. Picture of ISL6561 evaluation-board

Fig. 1-4. A typical VR implementation.

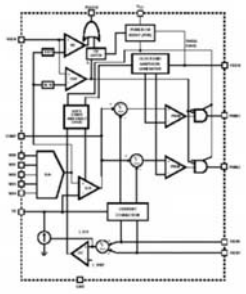
Fig. 1-4 shows today's typical VR implementation [A18]. As we can see, the power stage is a disturbed multiphase BUCK converter, which is controlled by a centralized VR controller. The output voltage information and current sensing information of each BUCK channel is fed back to the controller. The controller does the signal processing and sends out PWM signals to the driver.

This centralized VR control approach has the following limitations:

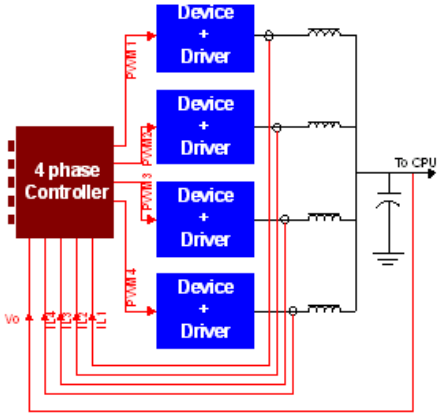
1) As shown in Fig. 1-5, VR design with different channel numbers needs different VR controllers. (The pin-out of the control IC is limited, but all the channels need to send back current information to the control IC and receive PWM signals from the control IC.)



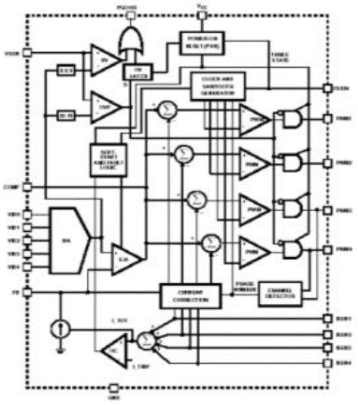
a. A two channel VR



b. Typical diagram of two channel VR controller



c. A four channel VR



d. Typical diagram of two channel VR controller

Fig. 1-5. VR designs with different channel number.

2) As shown in Fig. 1-5c, for the design with large phase number, long current sensing lines and PWM signal lines cannot be avoided, which is noise sensitive. (The controller can be physically put close to one or two channels, but cannot be close to all the channels.)
3) A control IC with channel number larger than 4 is not usually available in the market. (Second source is always one of the top priority for motherboard manufacturers to select VR control ICs.)
4) To design a controller with larger channel number to cover different channel numbers will waste package pins, waste silicon, and is only reasonable when the VR channel number is close to the controller channel number.

Basically, with traditional centralized controller, it is difficult for us to do flexible phase design (increase or reduce channel number). For future CPU power management, however, the CPU current rating will vary from 40A to 300A for different kinds of computers, and the CPU current rating will change even for the same type of computers, therefore the VR channel number can vary over a large range. To save the cost of developing different kinds of VR controllers, and to achieve more orders of design flexibility for better tradeoff of the system, and to maximize the market share of one design, how to achieve scalable phase design with the same type of IC is another major challenge in microprocessor power management.

1.2. The Technology Trend for Microprocessor Power Supply Design

1.2.1. Trend 1: Integration and High Frequency Operation

---- to Achieve High Power Density

Universities and industry researchers understand the limitation of traditional discrete and low frequency approach as described in 1.1.3. A lot of researches have been conducted to improve VR power density. The research shows that high frequency operation and integration with lateral device technology is the way to achieve higher power density [A19].

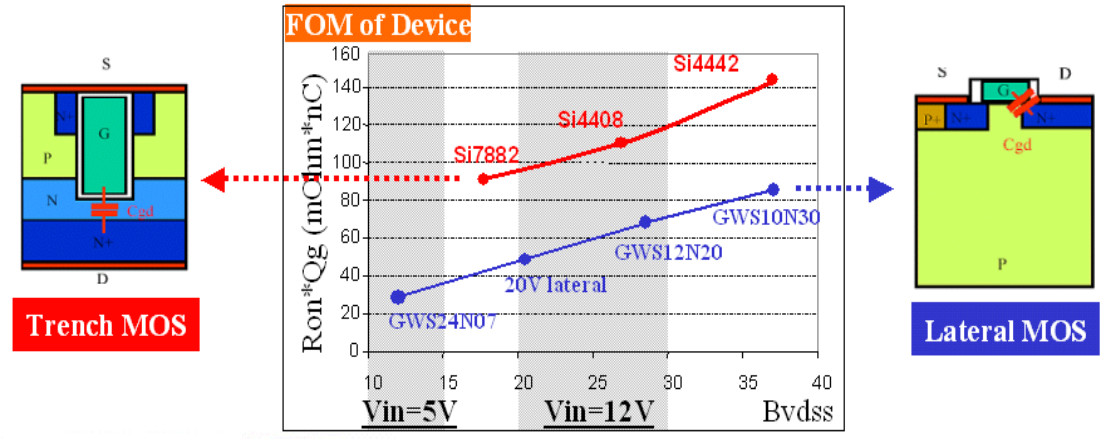


Fig. 1-6. FOM values of VR devices.

Traditional VRs use discrete trench MOSFETs as power devices. Fig. 1-6 shows the Figure of Merit (FOM) values of the state of the art trench MOSFETs. These values show that the trench MOSFET is not suitable to work at high switching frequency. Therefore today's VRs work just around 300KHz to avoid high power loss. The control bandwidth is also limited by the switch frequency, which results in the need for lots of OSCON caps to meet the transient requirement. Fig. 1-6 also shows that lateral MOSFET has much better FOM because lateral structure has much smaller Cgd [A20]. Using lateral MOSFET as power device will enable the high frequency operation so that the profile of

the converter can be reduced. More over, because the structure of the lateral power MOSFET is compatible with normal CMOS or BiCOMS process, the lateral power device can be integrated with the driver and control monolithically, which can further reduce the parasitic hence facilitating higher frequency operations.

For the Voltage Regulator, which is a multiphase BUCK converter with each phase of 15~25A, with the thermal constraint of today's IC package, the most straight forward way of integration is to integrate one channel device and driver together as a power IC. A company called Volterra takes this approach. Volterra released a 15A power IC "VT1102" that integrates one channel device and driver together and can work beyond 1MHz with 85% efficiency [A21]. Because of the high frequency, small inductor can be used. And only ceramic caps are used on motherboard, no OSCON needed. As you can see from Fig. 1-7, high frequency and integration dramatically improve the power density. Besides Volterra, other companies also introduce high power density VR solutions by integration and high frequency operation. They may be based on different advanced device technologies, for example Dr. MOS [A22], but the concept is the same ---- integration and high frequency operation.

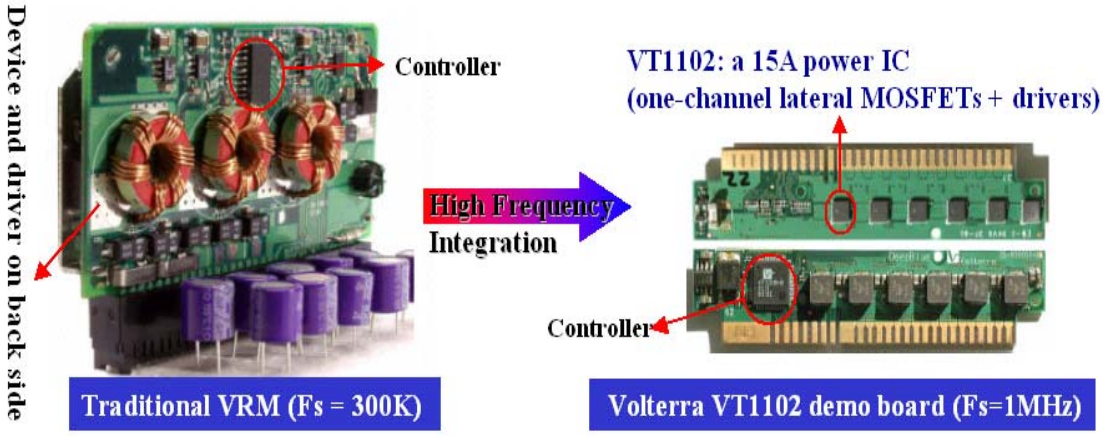


Fig. 1-7. Volterra's VT1102 solution.

1.2.2. Trend 2: Distributed Control ---- to Achieve Scalable Phase Design

Industry also realizes the limitation of the traditional centralized controller as described in 1.1.4. To save the cost of developing different control ICs for VR with different phase numbers, to cover different VR power ratings, and to achieve a better system tradeoff without channel number limitation, industry has begun to explore the scheme to achieve flexible phase design. Fig. 1-8 shows IR's Xphase solution [A23].

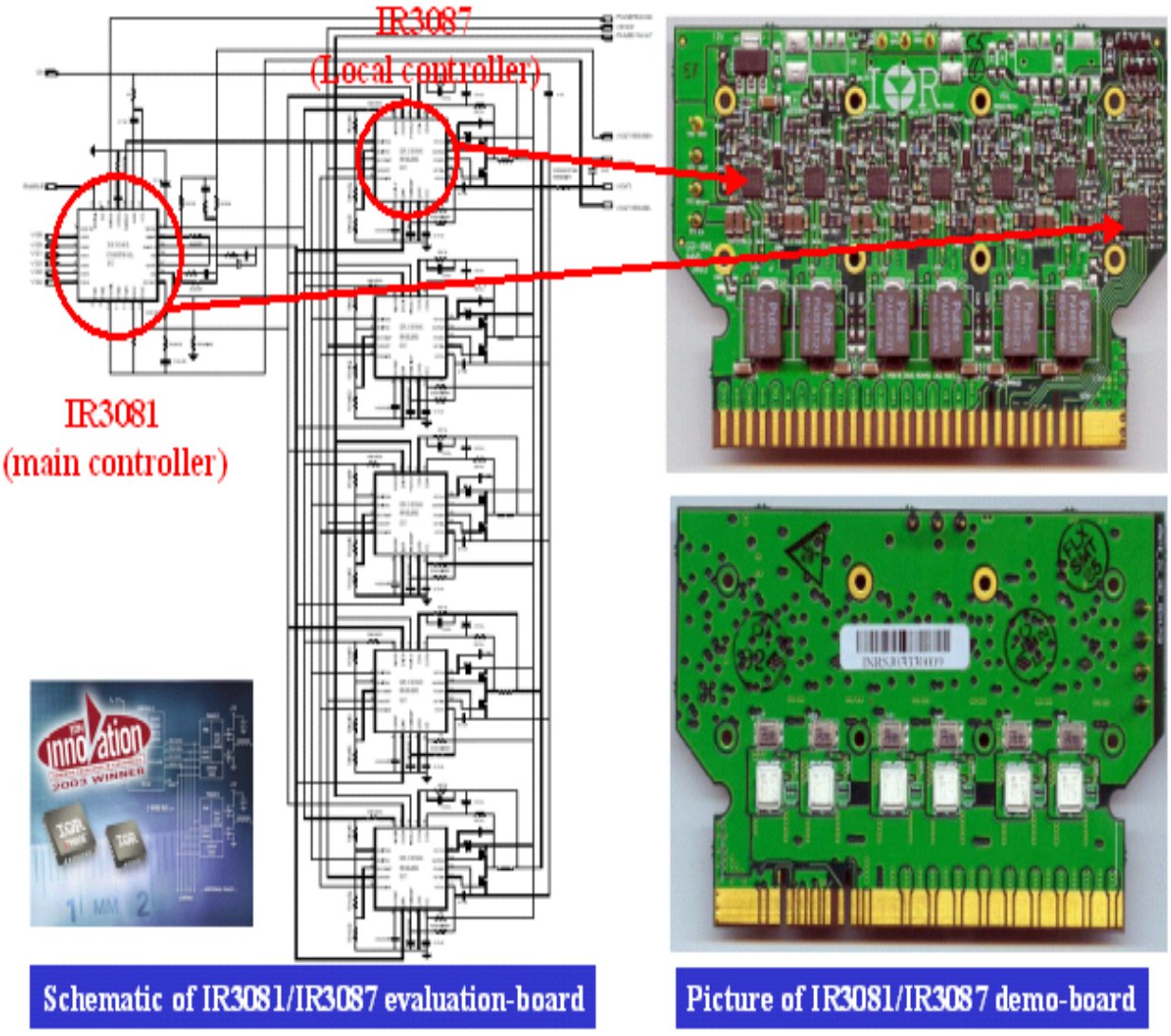


Fig. 1-8. IR's Xphase solution.

Developed specifically for multiphase, interleaved BUCK DC-DC converters, IR's XPhase chip set consists of the IR3081 Control IC (master) and the IR3086 Phase IC (local), and provides a high performance solution that exceeds the VRM or EVRD 10.x requirements. Unlike other multiphase solutions that are limited in the number of phases they drive, the IR XPhase architecture can support from 1 to "X" phases. Phases can be added or removed without changing the fundamental design.

The key of IR's chip set to achieve scalable phase design is the concept of distribution. The original VR control circuitries are distributed in "1+N" units. Each unit is integrated in different chips: 1 main controller chip, and N local controller chips. Each channel's PWM signals come from the local controller associated with this channel. Each channel's current information is only fed back to the local controller associated with this channel. The output voltage information is fed back to the main controller. The commutation between the main controller and local controllers depends on several bus lines. Because of the distributed architecture, a channel can be added or removed by adding or removing a local controller and one channel power stage without changing the fundamental design.

However, this solution is not perfect. A master controller is still needed because it is not a fully distributed system, too many external small resisters and capacitors are needed. Besides the 4 components in each channel for current sensing and the decoupling cap for the local control chip, there are still 7 components in each channel. They cannot be integrated because the absolute values of these resistors and capacitors need to be accurate, and they need to change if the channel number is changed. And too many analog bus lines and connections make the layout complex.

1.3. The Concept of Monolithic Voltage Regulator Channel

As described in sections 1.1 and 1.2, there are two major challenges for modern microprocessor power management: one is to achieve much higher power density, another is to achieve flexible phase design. To meet these challenges, a lot of explorations have been done and will be done in universities as well as in industry. However, the reported and published solutions need to be improved. For example, Volterra's solution can achieve much higher power density but it is difficult to achieve flexible phase design. IR's solution can achieve flexible phase design, but it has its drawbacks. The motivation of this research is to achieve both scalable phase deign and high power density for microprocessor power management. The following several paragraphs describe my train of thoughts.

1.3.1. Centralized Control Architecture and Its Integration

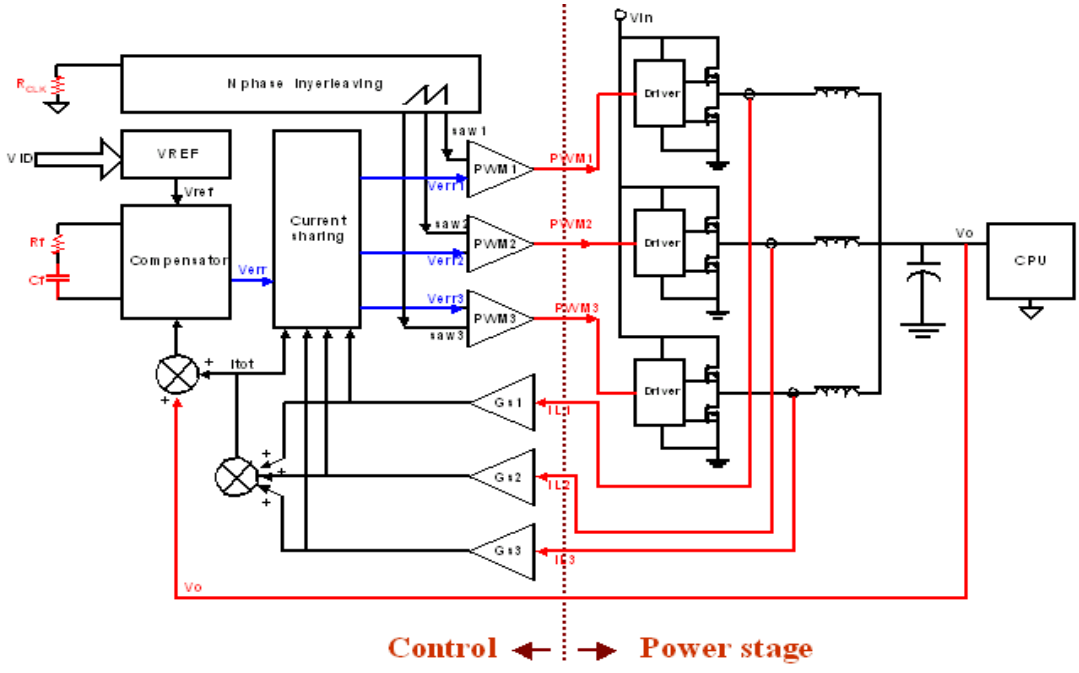


Fig. 1-9. Traditional centralized control architecture.

Fig. 1-9 is a simplified diagram of the traditional centralized control architecture for multiphase VRs [A18]. To achieve interleaving, a centralized interleaving block produces phase shifted clock pulse signals and saw-tooth signals according to the pre-decided VR phase number. To achieve current sharing, each channel's inductor current is fed back to a dedicated current sharing block (CS). The CS block produces error signals for each channel's PWM modulator by adjusting the voltage loop error signal according to each channel's current information. The CS block can be based on other current sharing mechanisms. To achieve AVP, the total current information and output voltage are fed back to the compensator, and the AVP performance is controlled by compensator design. Traditionally, the control part in Fig. 1-9 is integrated into a monolithic controller IC, and the driver for each channel's power devices is integrated as a separate driver IC. The power devices are discrete trench MOSFETs.

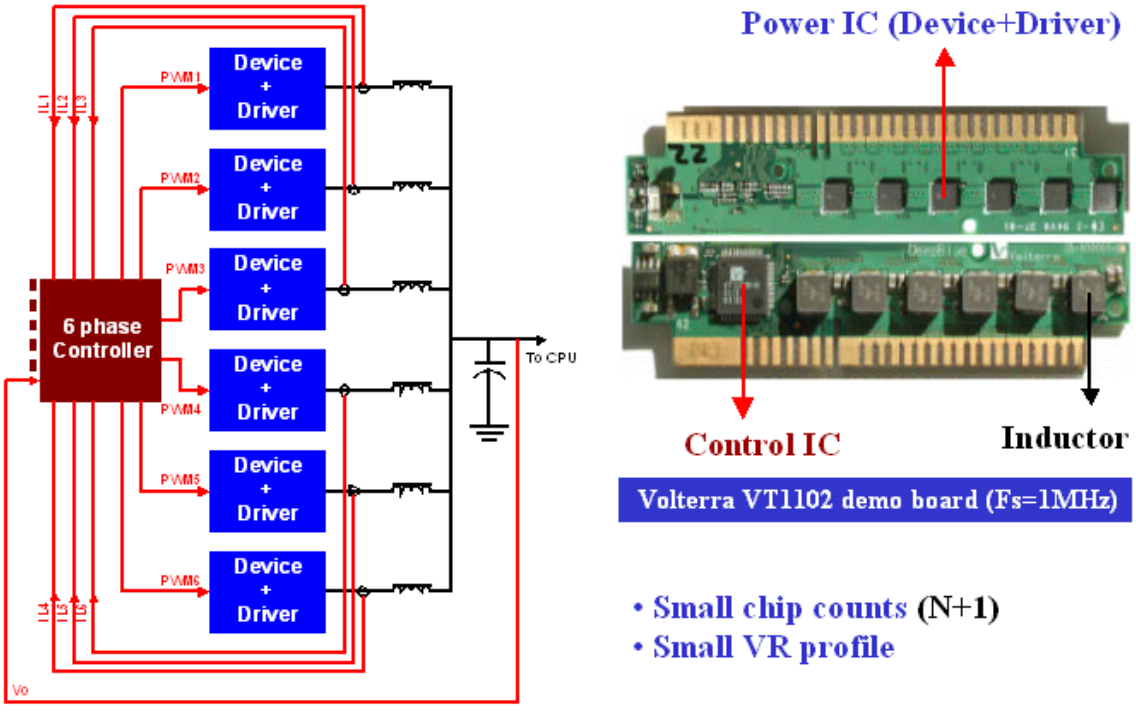


Fig. 1-10. Integration with the traditional centralized control architecture.

With the development of lateral power MOSFET, as discussed in section 1.2.1, each channel's driver and power devices can be monolithically integrated as a power IC and working at higher frequency to reduce chip count and to achieve much high power density. Fig. 1-10 shows the integration with the traditional centralized control architecture. However, even with this integration, there is still something that needs to be improved. Section 1.1.4 explained the need of scalable phase design and the challenge to realize it with the centralized controller. To achieve scalable phase design, new control architecture is explored in industry.

1.3.2. Partially Distributed Control Architecture and Its Integration

Fig. 1-11 shows the simplified diagram of IR's Xphase solution [A23]. Basically it is partially distributed control architecture.

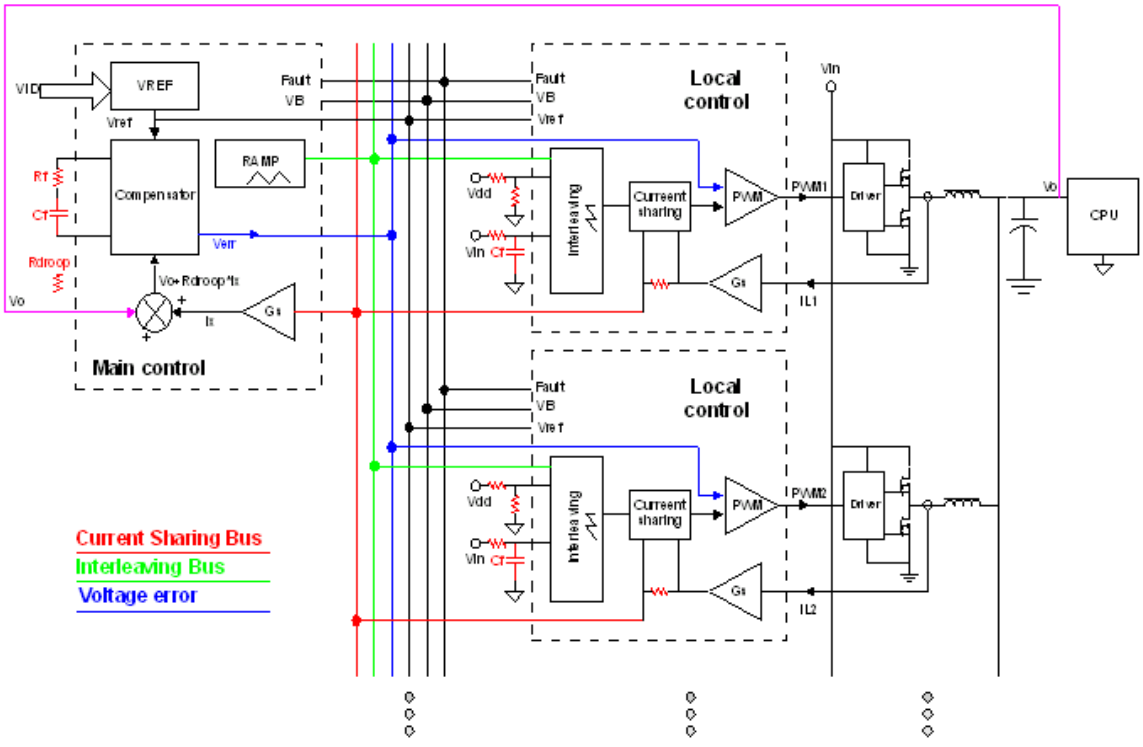


Fig. 1-11. Partially distributed control architecture.

In this partially distributed control, the block to achieve interleaving is distributed into N local control units and 1 main control unit. The block to achieve current sharing is distributed into N local control units. The block to achieve AVP, the compensator, is kept in the main control unit. By this way, each channel's current information is only fed back to the local control unit associated with this channel. And each channel's driver gets PWM signals from the associated local control unit. Therefore long current feedback lines and PWM signal lines are avoided. The main control gets information only from bus lines and sends information only to the bus lines. Therefore phases can be added or removed by adding or removing a local control without changing the fundamental design. To achieve high power density, each channel's driver and power devices and the local control unit can be monolithically integrated as a power IC. Fig. 1-12 shows the integration.

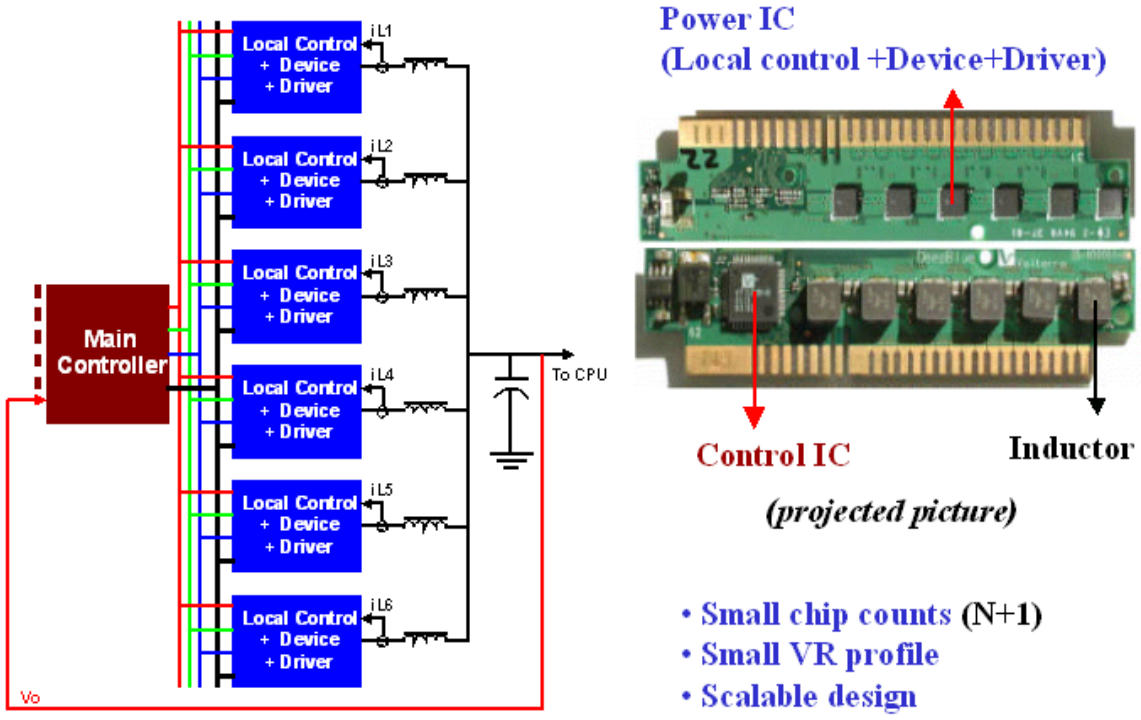


Fig. 1-12. Integration with the partially distributed control architecture.

However, the CPU power management solution shown in Fig. 1-12 still has some limitations. Some limitations are due to the partially distributed architecture and some are due to limitations in today's analog IC implementation.

Limitations due to the control architecture include:

- For manufacturer: The power IC has to work with a particular control IC. Both ICs have narrow application range, therefore small market.
- For customer: A main control is still needed. And the power IC cannot be used alone to supply a regular POL.

Limitations not due to the control architecture, but due to today's implementation:

- Too many analog bus lines, which may be sensitive to noise.
- Large control silicon size due to the required building blocks for driving the bus lines.
- Too many external components.

1.3.3. Fully Distributed Control Architecture and Its Integration ---- MVRC

Based on the observation of the centralized control architecture and partially distributed control architecture as well as their integration, a fully distributed control architecture is proposed.

Following Volterra's approach, we can integrate one channel device and driver together based on lateral device technology so it can work at high frequency, which will results in high power density. Then to achieve flexible phase design, instead of using partially distributed architecture such as IR's Xphase, the control circuitries are completely and evenly distributed into each individual channel. Each channel's current information is only fed back to the control associated to this channel. The output voltage

is fed back to each channel's control. The communication between different channel's control is not through a master controller, but through bus lines or other simple wire connections. With these connections, the control of each individual channel can work together to offer the control function for the whole voltage regulator. And of course each channel's control can also work alone to control just one channel. Fig. 1-13 visually shows this "fully distributed" idea.

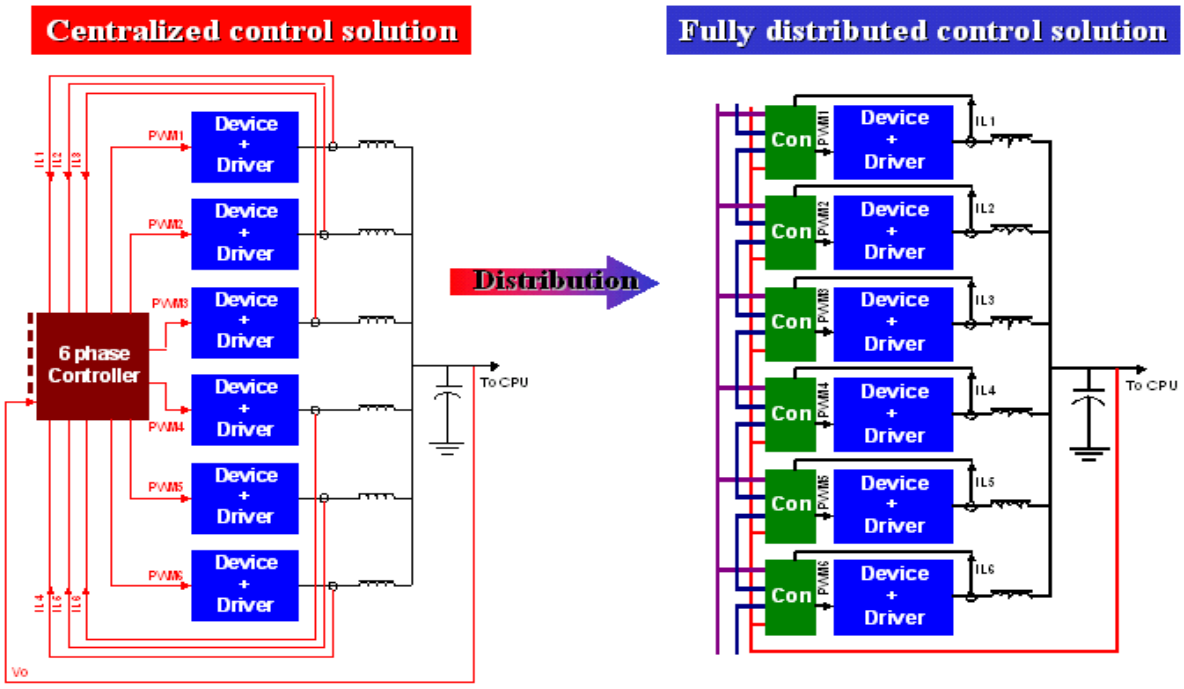


Fig. 1-13. Fully distributed control architecture.

However, if each channel's control part were built as a separate chip, the total chip counts of the voltage regulator would increase a lot. The power density would decrease. Then there is an interesting observation. The silicon size of each channel's control is normally much smaller than the power device and driver. If a very small piece of control silicon is added into the original power IC, the package will not change much or even

have no change. This is because the package of the power IC usually is thermally limited instead of die-size limited, and the power loss of the control part can be ignored when compared with the power MOSFET. By integrating the distributed control into the original power IC, we can eliminate the large size master controller, whose package is pin-out limited.

Then next step is to integration the distributed control into the original power IC. Fig. 1-14 shows the vision of this integration. The chip count is reduced and the power density increase further increases. The new power IC has control, driver and devices. It is a Monolithic Voltage Regulator Channel (MVRC), a generic IC that can be used alone to supply a regular POL load or multiple MVRCs can be used together to supply a CPU load. The MVRC is therefore a proposed solution for future CPU power management.

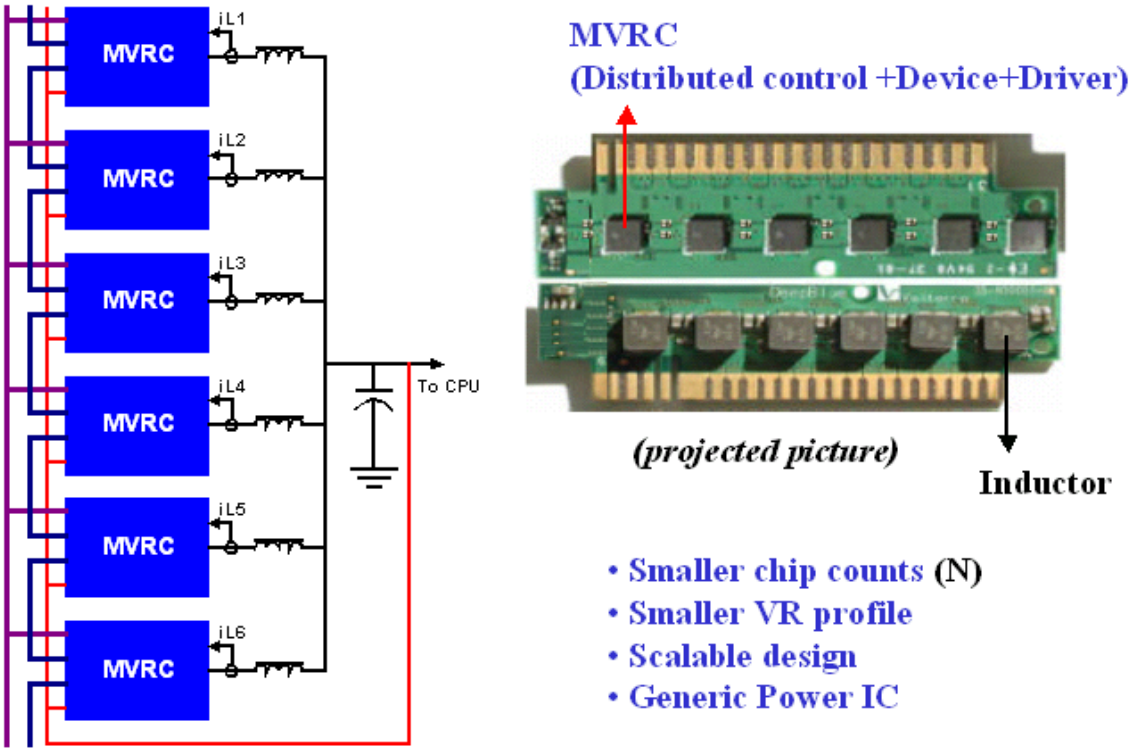


Fig. 1-14. Integration with the fully distributed control architecture ---- MVRC.

1.3.4. Potential Benefits of MVRC

Table 1-1 and Table 1-2 show the comparison of the integration based on three different control architectures ---- centralized, partially distributed and fully distributed (MVRC). The MVRC solution based on fully distributed control architecture shows potential benefits for both customers and manufacturers. Generally speaking, MVRC can achieve both high power density and scalable phase design. It is also a generic power IC for CPU and POL power management.

As shown in table 1-1 and 1-2, the benefits of MVRC solution depend on the particular control schemes and analog circuitries. The objective of this thesis research is to find out the suitable control schemes and analog circuitries for MVRC. Fig. 1-15 visually shows the research purpose of this dissertation.

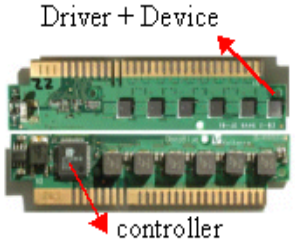
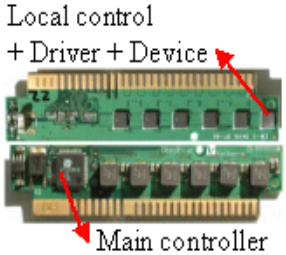
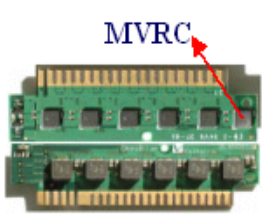
Customer's Concerns	Centralized control (Volterra' VT1102 demo) 	Partly distributed control ***(projected picture)*** 	Fully distributed control ***(projected picture)*** 
Scalable design	Difficult	**Easy**	**Easy**
Chip count	1 Controller +N Power IC	1 Controller +N Power IC	N Power IC **Smaller chip count**
VR power density	High	High	**Potentially Higher**
Layout difficulty	Difficult	**Easy**	**Easy**
Noise sensitive lines	1 Vo feedback lines N iL feedback lines	1 Vo feedback lines 3 analog BUS lines	**Depend on implementation**
Small component count	Few	Many (with IR's solution)	**Depend on implementation**

Table1-1. Potential benefits of the MVRC approach for customers (N is channel number).

Manufacturer's Concerns	Centralized (VT1102)	Partly distributed (IR xPHASE)	Fully distributed (MVRC)
Application range	CPU power	CPU power	CPU and POL power Potentially wider
Chip types	2	2	1
Chip complexity	Controller : ~ 8000 Power IC: ~300	Controller: ~ 2000 Power IC: ~1000	Depend on implementation
Overall developing cost	High	Fair	Potentially Lower
Mask sets	2	2	1
Chip Silicon size	Controller: 2N mm^2 Power IC: 25 mm^2	Controller : 2mm^2 Power IC : 26mm^2	Depend on implementation
Total Silicon size	27N mm^2 (2 run)	26N+2 mm^2 (2 run)	Depend on implementation
Total package needed	1*QFN + N*CSP	1*QFN + N*CSP	N*CSP
Trimmed needed per chip	Controller: 2 Power IC : 0	Controller: 2 Power IC : 1	Depend on implementation
Overall production cost	High	Fair	Potentially Lower

Table1-2. Potential benefits of the MVRC approach for manufacturers (N is channel number).

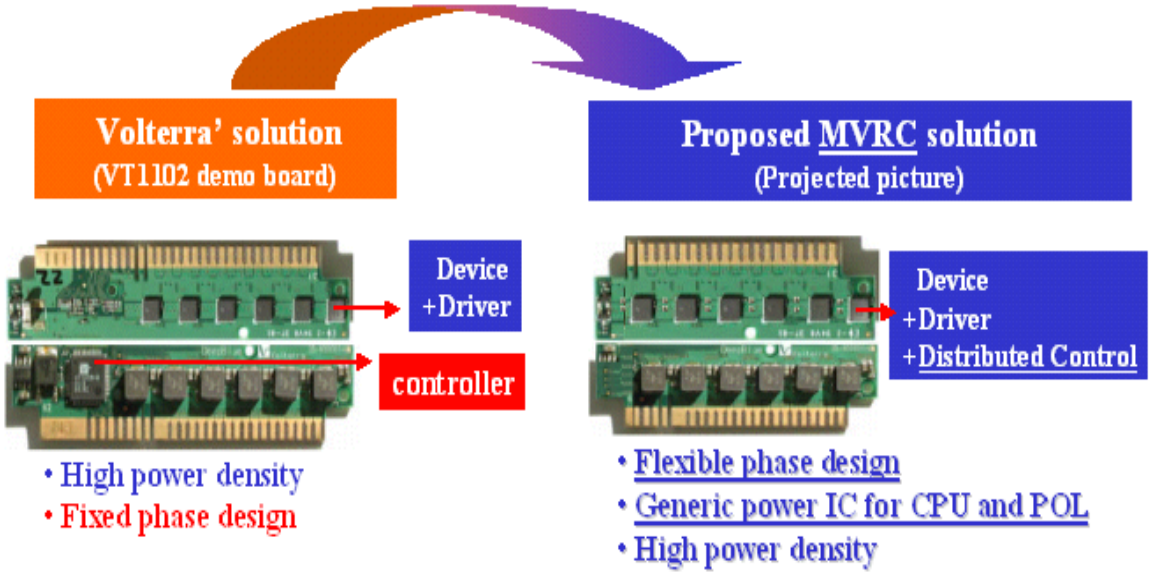


Fig. 1-15. Research purpose.

1.4. Research Scope and Dissertation Outlines

1.4.1. Research Scope

Inside the MVRC, there are power devices, drivers and control. For the integration of lateral MOSFET, CPES has developed a 5A power IC [A19]. The chip demonstrates the feasibility of multi-MHz operation with optimized lateral MOSFET. The result can be scaled up to higher current ratings provided new packaging techniques are used. Industry also has developed similar monolithic power ICs. Volterra's VT1102 power IC is an example.

To make MVRC a reality, the key is to define a fully distributed control and its associated analog IC designs to achieve all required functions that are originally provided by centralized VR controllers. These main functions include: interleaving, current sharing and Adaptive Voltage Position. And since MVRC works at high frequency, today's current sensing needs to be improved to meet the requirement of high frequency operation. Fig. 1-16 visually shows the research scopes of this dissertation.

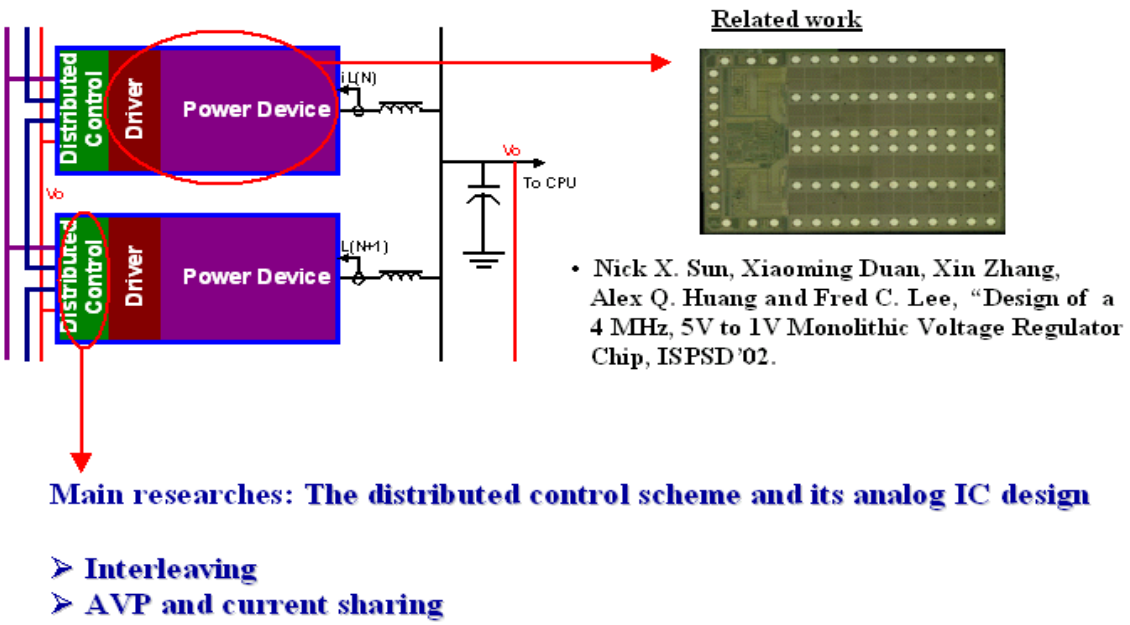


Fig. 1-16. Research scopes.

1.4.2. Dissertation Outlines

MVRC (Monolithic Voltage Regular Channel) is a generic power IC proposed for low voltage high current applications. MVRC chip has one channel power device, driver and control circuit monolithically integrated in a single silicon die and working at high switching frequency. It can be paralleled without a master control IC and without channel number limitation to support CPU power, or can be used alone to support regular POL. The objective of this research to find suitable control scheme and analog IC design solutions to overcome potential technology barriers in implementing the MVRC concept.

There are three major technology barriers in implementing the MVRC concept: 1) distributed interleaving; 2) distributed current and current sharing; 3) high frequency current sensing.

Chapter 2 addresses the distributed interleaving. Section 2.1 identifies the basic requirements to achieve good interleaving. Section 2.2 reviews the conventional centralized interleaving scheme and its limitations. Section 2.3 reviews existing distributed interleaving schemes. Issues of these approaches are also identified. In section 2.4, a novel distributed interleaving scheme is introduced, which can easily realize scalable phase interleaving without changing any component. The key building block of this scheme, a self-adjusting saw-tooth waveform generator is described in section 2.5. Section 2.6 is the hardware testing results of a 3 channel interleaving system with each channel working at 1MHz switching frequency. Section 2.7 is the conclusion of the chapter.

Chapter 3 addresses the distributed current sharing and AVP. Section 3.1 introduces Intel's design guidelines for microprocessor power management. Section 3.2 reviews the

conventional centralized current sharing and AVP schemes to meet the design specifications. The limitations in adopting these schemes for MVRC are also identified. In section 3.3, a novel distributed current sharing and AVP scheme are introduced. Section 3.4 presents the testing results of prototypes based on the proposed control schemes. Section 3.5 is the tolerance analysis of the proposed current sharing and AVP scheme. Monte-Carlo simulation results are also presented. Section 3.6 is the conclusion of the chapter.

Chapter 4 addresses the current sensing issues. Section 4.1 reviews the current sensing technologies currently used in VR applications. Section 4.2 identifies the issues of the traditional inductor current scheme in high frequency application. Section 4.3 introduces a novel inductor current sensing scheme that is suitable in high frequency application with small inductor DCR. The key building block of the proposed sensing scheme, an accurate transconduance (Gm) amplifier is described in Section 4.4. Section 4.5 presents a number of current sensing configurations with the proposed Gm amplifier. Section 4.6 discusses other applications of the novel Gm block. Section 4.7 is the conclusion of the chapter.

To obtain further verification, the proposed schemes and analog building blocks are integrated in a dual channel synchronous BUCK controller developed with TSMC 0.5um BiCMOS process. Chapter 5 presents the design of this chip, including the design objective, block diagram, design methodology, layout and die photo, as well as circuit testing results and system testing results. Section 5.7 is the summary of Chapter 5.

Chapter 6 is the conclusion of the whole dissertation and the list of future work.

Chapter 2. Distributed Interleaving

2.1. Interleaving ---- Benefits and Requirements

2.1.1. Interleaving Benefits

Verified by industry, paralleling circuits (power stages/ converters) are usually better than paralleling power devices to construct a supply with a large power rating [B1]. Especially for microprocessor power management, all the VRMs (Voltage Regulator Modules) or VRDs (Voltage Regulator Downs) [B2] use multiphase topology to get high current low voltage output with decent efficiency.

One of the primary benefits of multiphase converter is that the input and output ripple cancellation can be achieved by interleaving operation. For microprocessor power management, to meet the tight output voltage ripple specifications and voltage regulation window [B2], interleaving operation of the multi-cell power stage (which is usually a multi-channel synchronous BUCK converter, as shown in Fig. 2-1,) is mandatory.

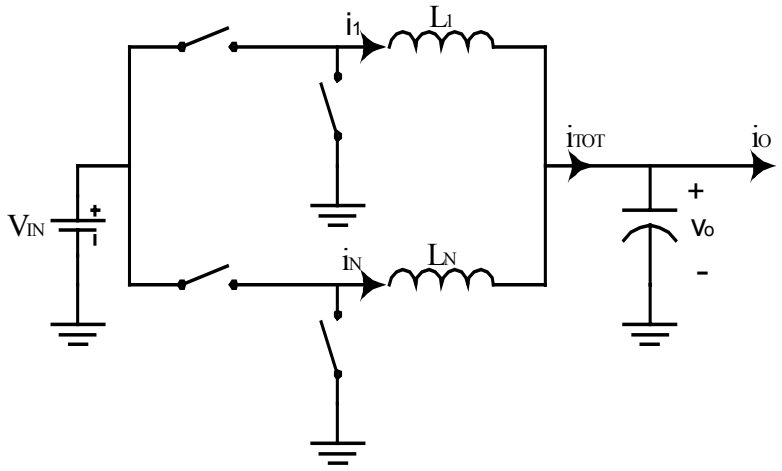


Fig. 2-1. Topology of N-channel synchronous BUCK converter.

Fig. 2-2 shows the steady state current ripple reduction effect of interleaving operation [B3]. The effect is defined as $K= \Delta i_{TOT} / \Delta i_{n,}$ where Δi_{TOT} is the peak-to-peak value of the total inductor current in Fig. 2-1, and Δi_n is the peak-to-peak value of the individual inductor current. The ripple cancellation effect is a function of the phase number and the steady state duty cycle. For a given input and output voltage, by proper selection of the phase number, the ripple of the total current going through output capacitors can be significantly reduced. Therefore, the output voltage ripple can be dramatically reduced. More advantages of interleaving can be found in [B3]. And more mathematic analysis can be found in [B4].

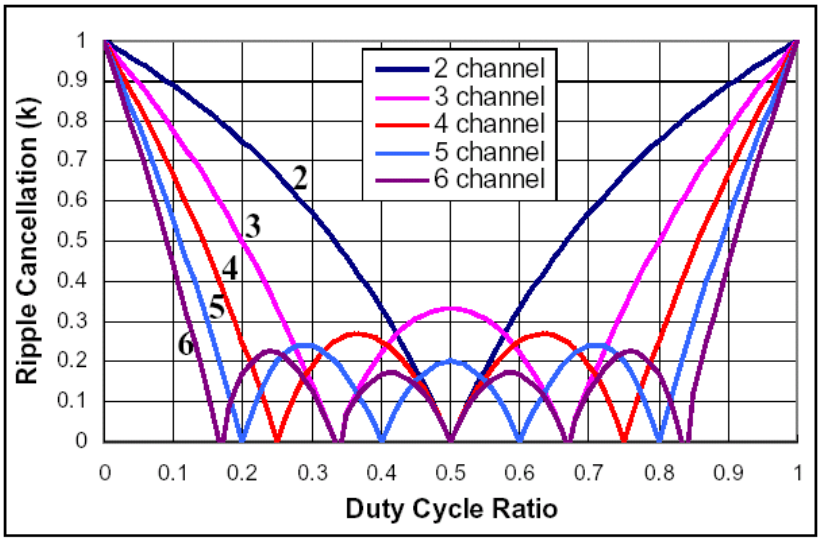


Fig. 2-2. Current ripple reduction in an interleaving BUCK converter.

According to Intel's roadmap [B5], future mainstream microprocessor needs lower voltage, higher current, and tighter voltage regulation window. Moreover, the CPU current rating can vary from 40A to 300A for different kinds of computers, and CPU power supply specifications can change fast for the same type of computer. VR channel number can vary in a very large range. As discussed in Chapter 1, to save the cost to

develop different kinds of VR controllers, and to achieve more orders of design flexibility for better tradeoff, scalable phase design with the same type of IC is the trend [B6].

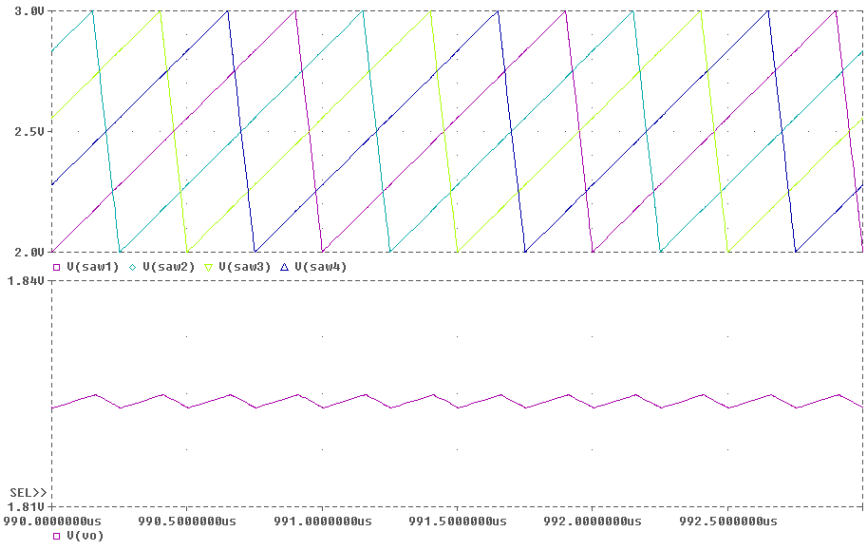
To achieve scalable phase design, the first task is to achieve interleaving with scalable phases. A conventional approach of interleaving is to use a centralized phase splitter circuit to supply a properly phased clock or synchronization pulses to each individual channel. This approach is not practical if there are a variable number of channels in the system. The objective of this chapter is to introduce a concise practical scheme that can achieve interleaving with scalable phases.

2.1.2. Requirements to Achieve Good Interleaving

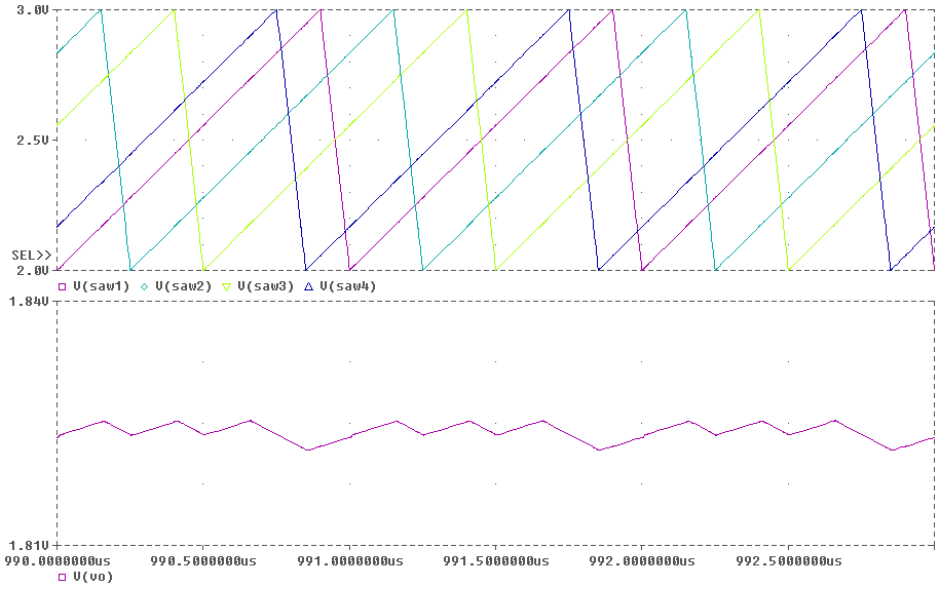
There are three requirements to achieve good interleaving operation: 1) Accurate phase shift; 2) Matched carrier signals; 3) Good layout for the output capacitor matrix. This chapter focuses on the task 1 and 2. The following is the detailed explanation of these requirements.

1) Accurate phase shift

To achieve interleaving operation of a N-channel power stage, each channel's switching clock must have the same frequency, and the phase of the clock should be displaced with respect to one another by 2p/N radians. Any error in phase shift can lead to large current ripple and voltage ripple at output capacitors. Fig. 2-3 shows the impact of phase shift error. Fig. 2-3a shows the simulated carrier waveforms and output voltage of a 4-channel BUCK converter with proper phase shift. Fig. 2-3b is simulation results with a 10-degree phase shift error in one of the 4 channels. The output ripple in Fig. 2-3b is about 2 times bigger than in Fig. 2-3a.



a. Simulation results with proper phase shift



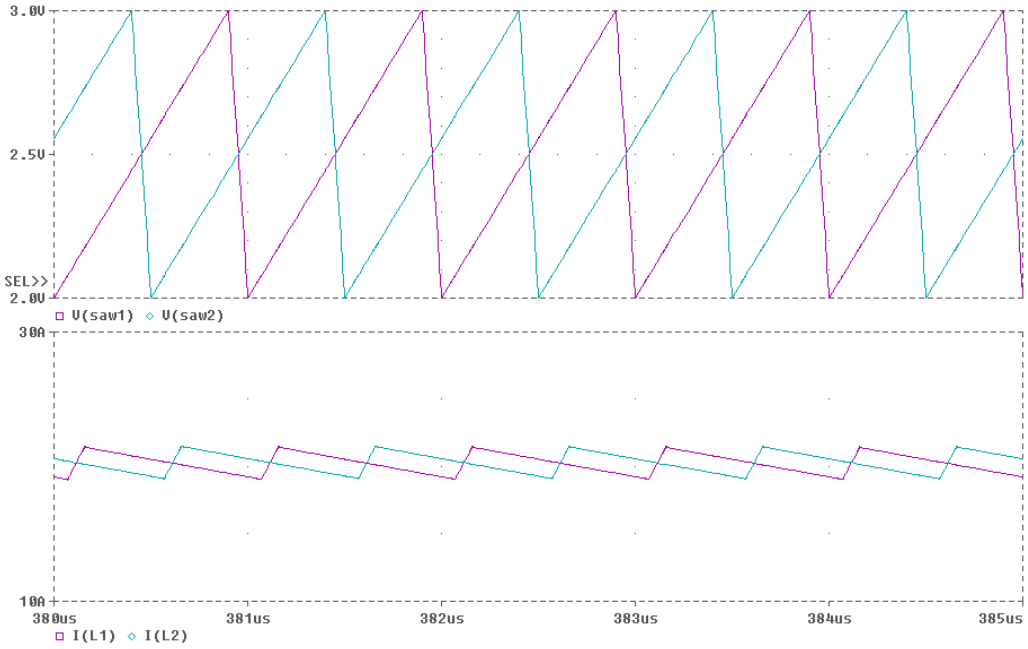
b. Simulation results with 10-degree phase shift error in V(saw4)

Fig.2-3. The impact of phase shift error.

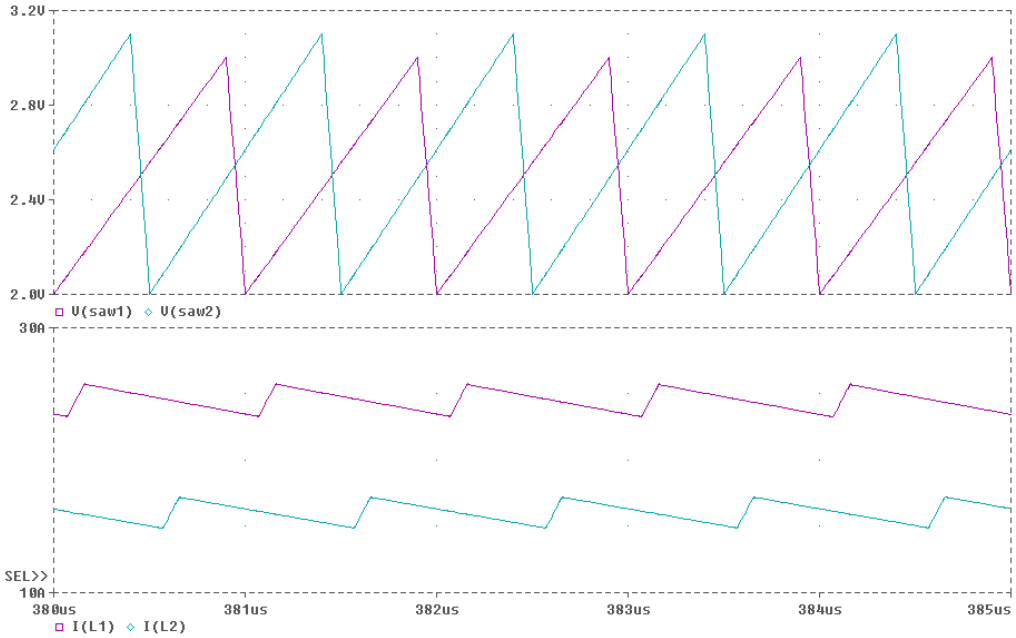
2) Matched carrier signal

For lots of VRM control schemes [B7], each channel also needs a carrier signal synchronizing the phased clock, which is usually in a format of trailing edge saw-tooth waveform. Any unmatching of the slopes and the valley or/and the peak values of the

carrier waveforms can cause the current sharing problem or even the stability problem. The impact of the nonideal carrier waveforms can be different and is dependent on the system control architecture. Therefore, besides the proper phase shift, carrier signal matching is another requirement to achieve proper interleaving operation for multi-channel DC-DC converter used for microprocessor power management. Fig. 2-4 shows the impact of nonideal carrier signals. Fig. 2-4a shows the simulation results of matched carrier waveforms and inductor currents of a 2-channel synchronous BUCK converter. Fig. 2-4b is the simulation results with 10% difference in each channel's carrier slope. Both simulations use a control scheme like HIP6301 [B8]. As shown in Fig. 2-4b, the current sharing is sacrificed by only small error in the matching of saw-tooth signals.



a. Inductor current with matched saw tooth



b. Inductor current with 10% difference in saw-tooth slope

Fig. 2-4. The impact of nonideal carrier signal.

2.2. Issues of Centralized Interleaving Schemes

To meet the requirements described in section 2.1.2, a conventional interleaving scheme uses a centralized phase splitter to produce a properly phased clock or synchronization pulses for the individual channels. Typical implementation is to use a shift register or a counter and decoder [9]. For a traditional VRM control scheme, a centralized multiphase saw-tooth generator is adopted to produce saw-tooth carrier waveforms for each individual channel, which synchronizes the associated pulses produced by phase splitter. Typical implementation of the multiphase saw-tooth generator is to use a series of matched current sources to charge a series of matched capacitors. Fig. 2-5 shows the traditional interleaving scheme for VRM application.

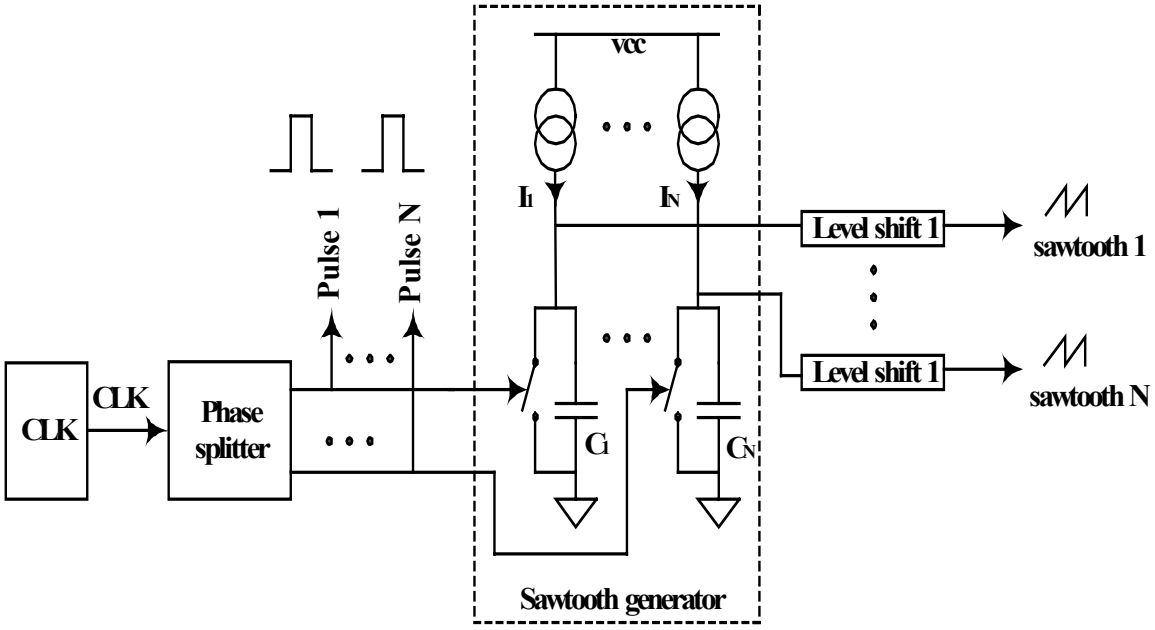


Fig. 2-5. Traditional centralized interleaving scheme.

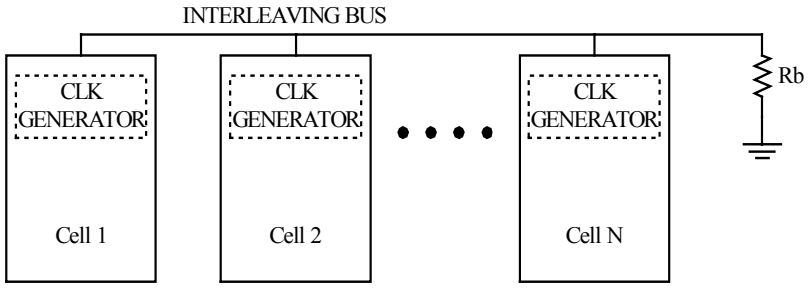
In the traditional centralized interleaving scheme, the phase splitter needs to know the channel number of the system. Circuitries and interconnections between phase splitter and saw-tooth generator need to be changed when the channel number is changed. A centralized interleaving scheme that can offer a programmable number of phases within a limited range is achievable but at the cost of unused or redundant die area. The complexity of circuit and interconnection limits the centralized interleaving scheme to produce properly shifted clock and carrier waveforms if the channel number of the system can vary in a large scope. And to guarantee the matching of each channel's saw tooth, layout matching of current mirrors I1~IN and capacitors C1~CN in Fig. 2-5 is mandatory. Therefore they usually occupy lots of silicon size and are put together using particular patterns. Even so, to guarantee the slopes, and peak and valley values of these saw-tooth waveforms are the same as specified, trimming is often needed for the current source or/and the capacitor inside silicon.

2.3. Issues of Reported Distributed Interleaving Schemes

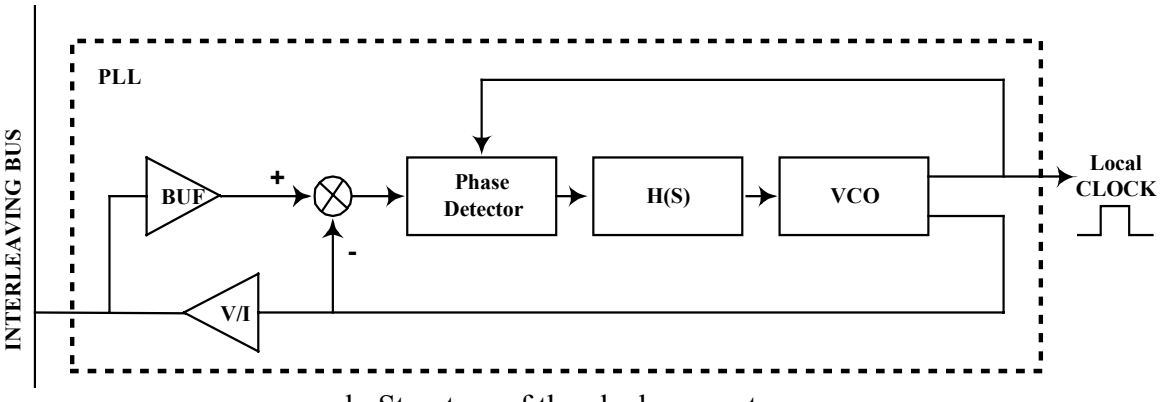
The limitations of the traditional centralized interleaving scheme have led to the exploration of distributed interleaving approach.

2.3.1. A Distributed Interleaving Scheme with Interleaving BUS [B10]

Fig. 2-6 shows the distributed interleaving scheme proposed in Perreault's paper [B10]. In this scheme, each cell (channel/converter) has its own clock generator. The frequency and phase information of each cell is aggregated on the interleaving bus. Using the analog signal on the interleaving bus, each cell adjusts the frequency and phase of its local clock to achieve the desired value for proper interleaving. The implementation of the clock generator in each cell is shown in Fig. 2-6b. Its basic building block is a Phase-Lock Loop (PLL).



a. Distributed interleaving architecture with an interleaving BUS



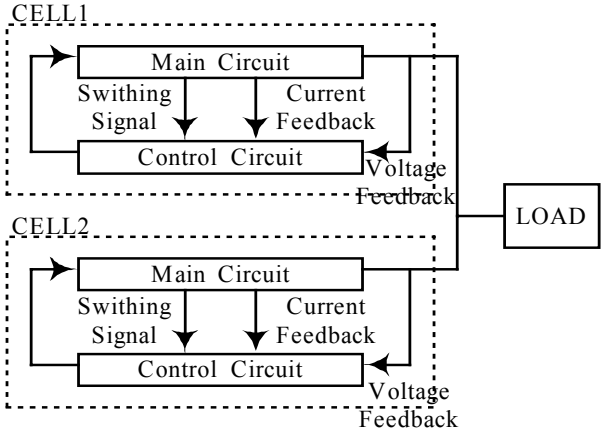
b. Structure of the clock generator

Fig. 2-6. Distributed interleaving scheme proposed by Perreault's paper.

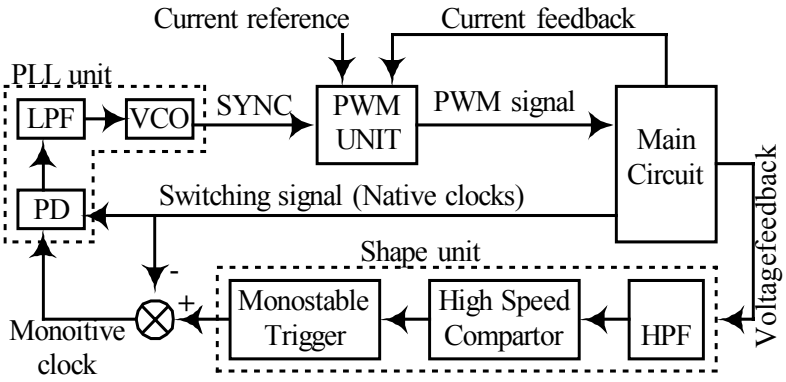
However, Perreault's scheme can only generates right clocks for up to 3 cell interleaving. The PLL may lock to a wrong phase state when there are more than 3 cells in the system. A low pass filter H(S) is necessary to compensate the PLL. Because the switching frequency for a regular converter is within a 10MHz range, the low pass filter needs large passive components and cannot be monolithically integrated. Perreault's paper did not address the issue of how to get carrier signals matched among each cell, which is very important in VRM application, as shown in Fig. 2-4.

2.3.2. A Distributed Interleaving without Interleaving BUS [B11]

Fig. 2-7 shows the distributed interleaving scheme proposed in Feng's paper [B11]. In each converter cell, switching signals of the power stage are fed back to each cell's control circuit to cancel the native pulses in the output voltage that are consistent in phase with the corresponding switch signals. The implementation of each cell's control circuit is shown in Fig. 2-7b. The basic building block includes a phase-lock loop and a "shape unit", which is composed of a High Pass Filter, a high-speed comparator and a mono-stable trigger.



a. Distributed interleaving architecture without interleaving BUS



b. Structure of the control circuit in each cell

Fig. 2-7. Distributed interleaving scheme proposed by Feng's paper.

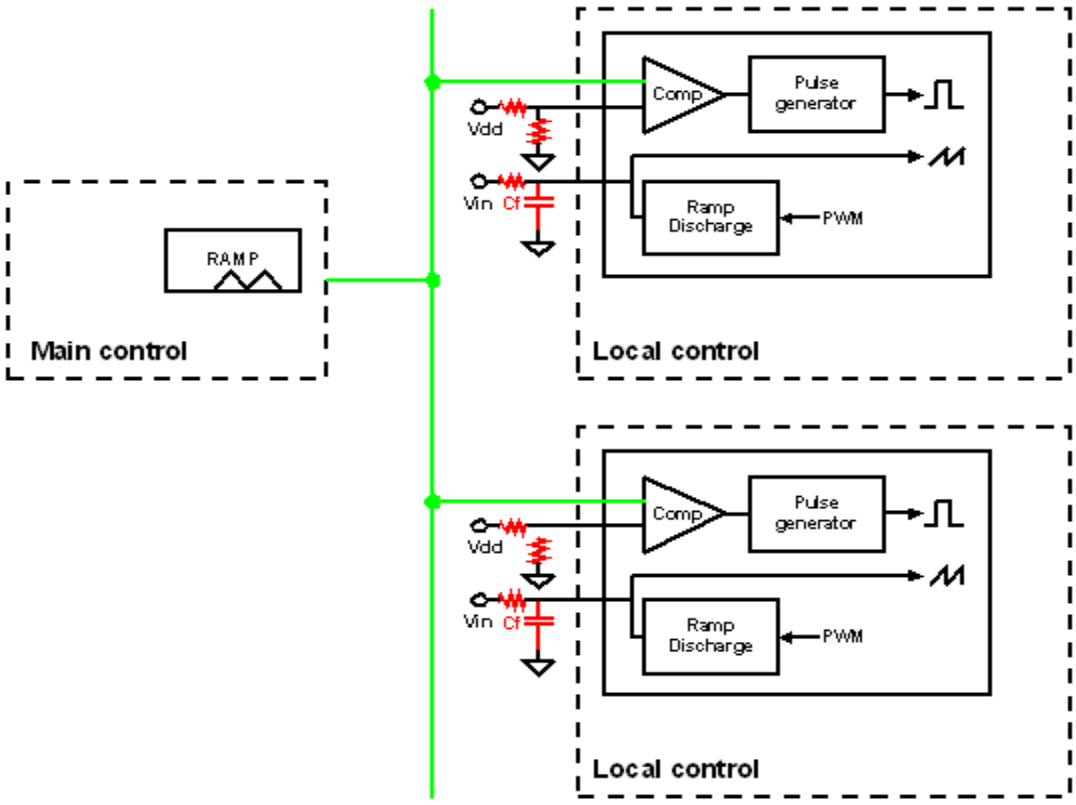
Feng's paper demonstrates the interleaving operation of a 2-cell system with switching frequency of about 100KHz. However, due to its approach to shaping output voltage, this scheme is noise sensitive and is very difficult to be adopted in VRM application, where the switching frequency can be beyond 1MHz, conduction time of power MOSFET within a cycle may be smaller than 200ns, and di/dt on the gnd plane is usually beyond 50A/us. From VRM cells to CPU, there is a complex decoupling loop composed of different types of capacitors [B12]. It is difficult to find a feedback point to get a signal contending the strong enough timing information of every switching event in the system. However, to be able to feed back such a signal is the pre-requisite of this scheme. The HPF in the shaping unit and LPF in the PLL need large passive components that cannot be monolithically integrated. Feng's paper did not address the carrier signal matching issue either.

2.3.3. Distributed Interleaving Based on Two-Chip Architect [B6]

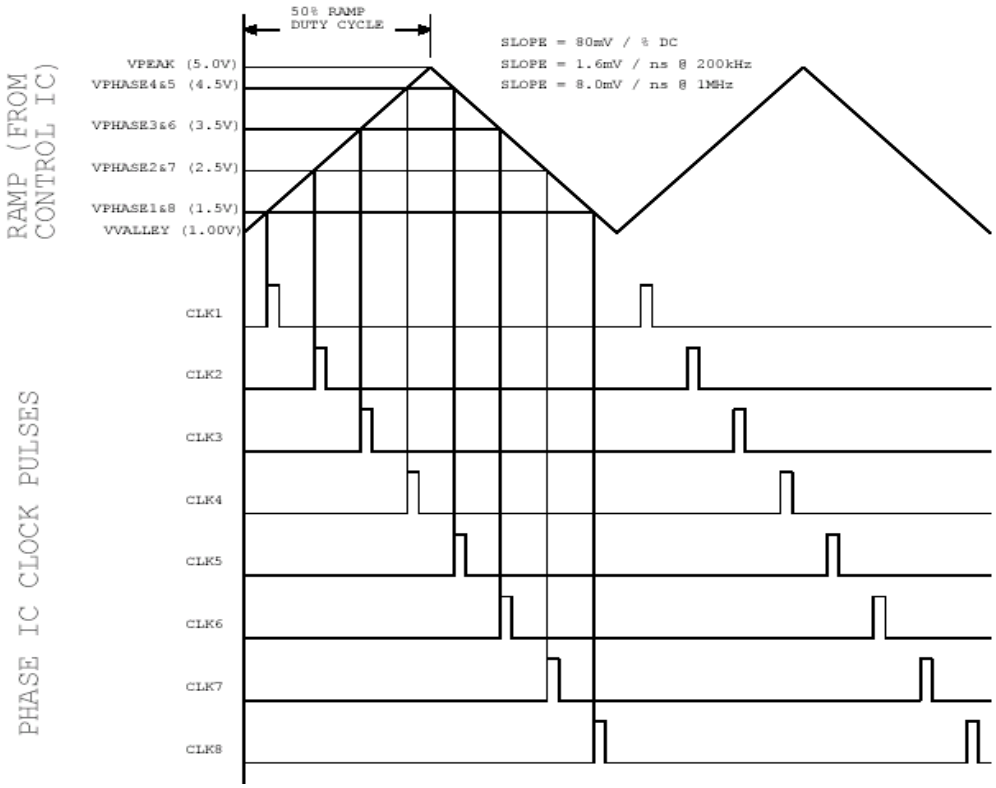
Fig. 2-8 shows the distributed interleaving scheme proposed by Huang's paper [B6]. This scheme uses a master control IC to produce a triangle waveform with the same

frequency as the switching clock. Each channel's phase IC uses an accurate divider to produce a DC voltage to tell the master controller which phase it has. As shown in Fig. 2-8b, this DC voltage is compared with a triangle waveform to produce a pulse working as the timing base for this channel's clock and carrier.

Verified by hardware testing, this scheme meets the tight requirements of VRM application up to 16 channels. However, this scheme is not perfect. Because each channel needs to produce an accurate DC voltage to program the phase delay, each channel needs 2 external resistors to build the accurate divider. And to guarantee the carrier signal matching, each channel needs 1 additional external resistor and 1 external capacitor. When the channel number is changed, all these components need to be changed.



a. Distributed interleaving based on two-chip architect



b. Phase delay programming of an eight phase interleaved converter

Fig. 2-8. Distributed interleaving scheme proposed by Huang's paper.

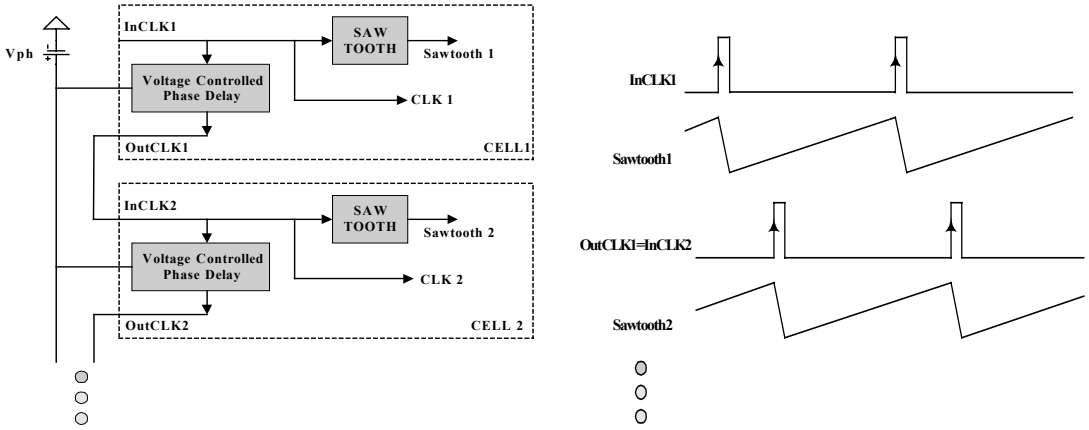
Table 2-1 shows the summary of the main limitations of the interleaving schemes mentioned above.

Interleaving scheme	Perreault's [B10]	Feng's [B11]	Huang's [B6]
Main limitations	Only works well up to 3 channels.	Noise sensitive, not suited for VRM application.	Too many external extra components needed. Two kinds of chip needed.

Table 2-1. Summary of existing interleaving schemes.

2.4. A Novel Distributed Interleaving Scheme

As shown in Table 2-1, the schemes reviewed in section 2.3 are not suitable or not convenient to achieve scalable phase design in VRM application. A Novel distributed interleaving scheme is developed to serve the purpose.



a. Scheme b. Waveforms

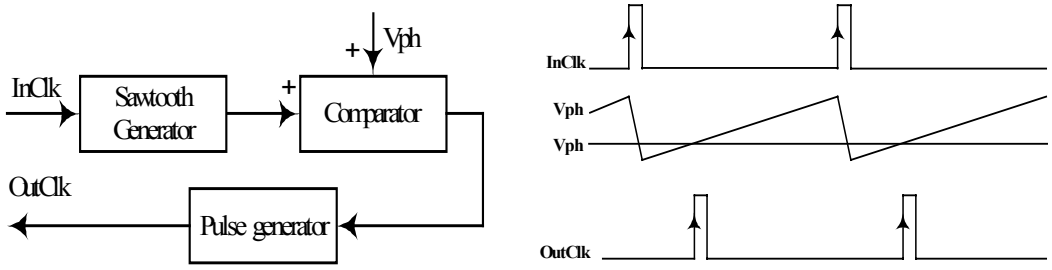
Fig. 2-9. A novel distributed interleaving scheme.

Fig. 2-9 shows the proposed interleaving scheme. For each cell, there is an InCLK and OutCLK. And there is a phase delay between these two clocks. The phase delay is controlled by Vph, which is set according to the phase number of the system. Each phase need not tell others which phase they have because the InCLK and OutCLK have already decided the relationship of each phase. If there is N phase, set up Vph to make phase delay 360/N degrees between InCLK and OutCLK. In each channel, a saw-tooth generator produces a saw-tooth waveform to synchronize the InCLK. By this way, Interleaving among each channel is achieved.

The DC voltage Vph can be produced by an adjustable voltage reference like TL431, or can be the output of a Digital-to-Analog Converter (DAC). For microprocessor power

management, this DAC can be integrated in the IC that supplies the VID power [B2], therefore no external chip/component needed for the proposed interleaving scheme.

The key of this scheme is how to generate an accurate phase delay according to Vph. The most popular approach is to use PLL to get the voltage controlled phase delay. But as mentioned in section 2.3, such PLL cannot usually be monolithically integrated since the large outside capacitor is needed for the low pass filter within the PLL. In the proposed interleaving scheme, as shown in Fig. 2-10, a monolithic saw-tooth generator and a comparator are adopted to produce the voltage control delay. A leading edge saw tooth is produced to synchronize the InCLK. Vph is compared with the leading edge saw tooth to get the timing signal. A pulse generator reshapes the comparison results as a pulse waveform, OutCLK, which is used as InCLK for next phase.



a. Scheme b. Waveforms

Fig. 2-10. Implementation of the voltage controlled phase delay block.

However, to get the accurate phase delay, we need to make sure the saw-tooth waveform accurate. And to achieve carrier matching between channels, and we also need an accurate saw-tooth generator that is layout and process insensitive. A monolithic self-adjusting saw-tooth generator that is accurate and layout/process insensitive will be presented in next section. The saw-tooth generator is used as the key building block of Figures. 2-9a and 2-10a.

2.5. The Key Building Block ---- A Self-Adjusting Saw-Tooth Generator

As mention in section 2.2, the traditional saw-tooth generator needs layout matching to match the saw-tooth of different channels, which cannot be done in scalable phase design since in the distributed interleaving scheme, each carrier waveform is generated in different silicon dies associated with each channel. The approach in section 2.3.3 is not convenient either, since a lot of external discrete components are needed.

Fig. 2-11 shows the proposed self-adjusting saw-tooth generator. The output saw-tooth waveform synchronizes the incoming CLK. The slope, amplitude, valley and peak values of the saw-tooth waveform are automatically self-adjusted to the specified values, and independent of the layout and process. No trimming is needed for this circuit. And it can be easily monolithically integrated using just typical digital CMOS process without any external component.

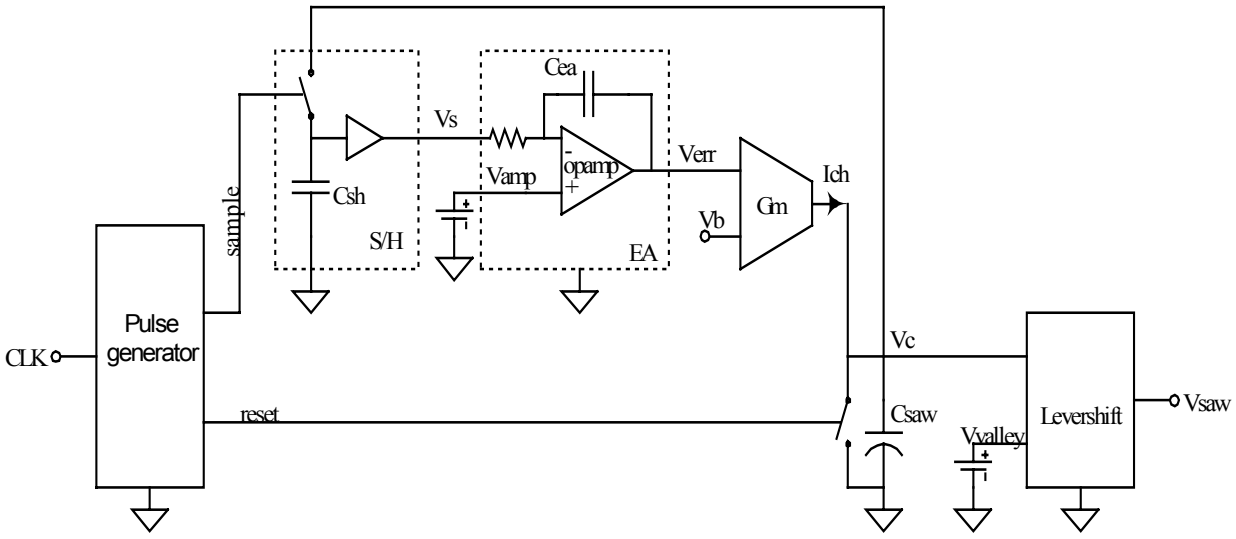
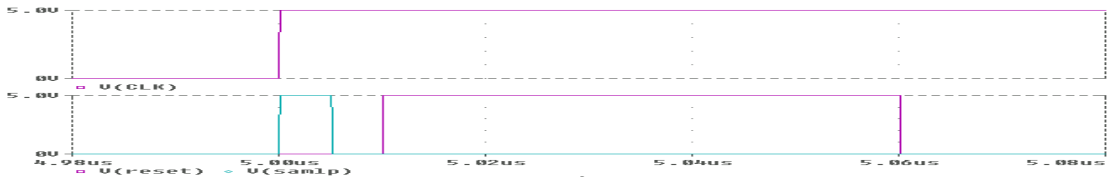
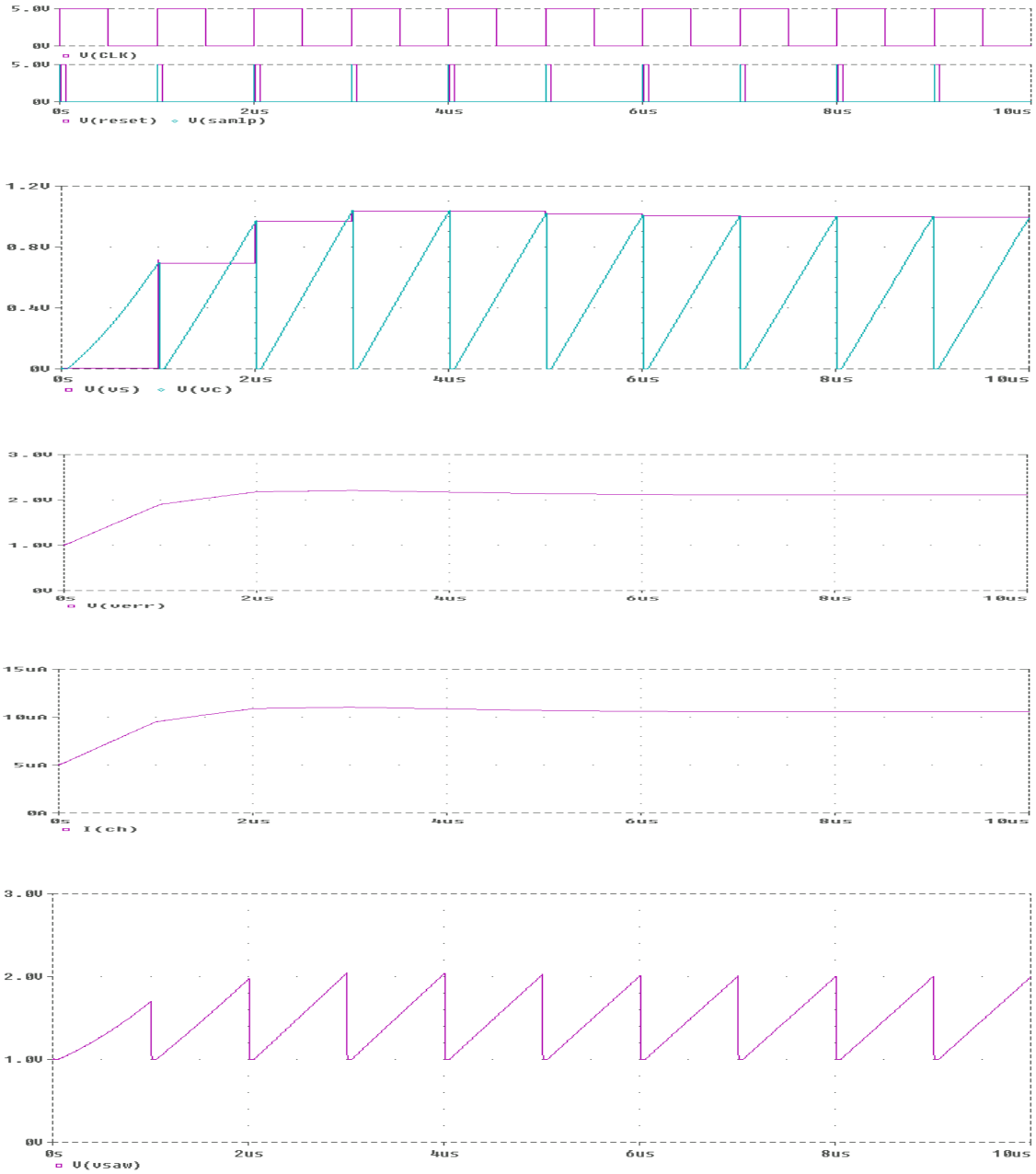


Fig. 2-11. A self-adjusting saw-tooth generator.

The basic concept of this circuit is to use a changeable current Ich instead of a fixed current to charge a capacitor to produce a saw-tooth waveform Vc. And Vc is lever-shifted (if necessary) to produce the finial output voltage Vsaw.



a. Detail of reset pulse and sample pulse



b. A self-adjusting process

Fig. 2-12. Simulated waveforms of the self-adjusting saw-tooth generator.

Fig. 2-12 shows the simulated waveforms that explain the work principle of this self-adjusting circuit. The CLK defines the switching frequency and has a period T. In Fig. 2-11, a pulse generator produces two narrow pulses synchronizing the incoming CLK. As shown in Fig. 2-12a, the sample pulse is triggered by the rising edge of the CLK and has a pulse width $\tau 1$. The reset pulse is triggered by the falling edge of the sample pulse but with a tiny delay $\tau 2$ to guarantee there is no overlap between the sample pulse and the reset pulse that has a pulse width $\tau 3$. The sample pulse controls a sample and holds the circuit to catch the value of Vc when sample = "1". The reset pulse controls a switch to reset the voltage across Csaw when reset = "1". The sampled Vc value ---Vs and a voltage reference Vamp are fed into an error amplifier to produce an error voltage Verr. This Verr is then transferred to a current Ich by a transconductance amplifier. Csaw is charged by Ich and reset by the switch controlled by the reset pulse to produce a saw-tooth signal Vc across the Csaw. Since the Error amplifier is basically an integrator that has an infinite DC gain, the amplitude of the Vc will be settled down to the value defined by Vamp after several switching cycle if the feedback loop is stable. Vc can be level-shifted to be on top of Vvalley using Opamp circuit if the designed valley of the output saw tooth is not GND. For the finial output saw-tooth signal Vsaw, the frequency is synchronized with CLK; the amplitude is defined by Vamp; the valley value is defined by Vvalley; the peak valley is defined by Vvalley + Vamp; the slope is defined by Vamp/(T-$\tau 3$). Vamp and Vvalley can come from Bandgap reference. T is the same for each channel, which is guaranteed by the connection shown in Fig. 2-9a and is usually set by an external resistor. Therefore, Vsaw can be produced by setting voltage Vamp and Vvalley. The accuracy of the slope, amplitude, valley and peak values, and the matching

of different saw-tooth waveforms produced by different silicon chips can be guaranteed by the schematic design and be insensitive to layout and process variations. The self-adjusting process does not affect the system because the PWM or other control actions of the system can be active only after the saw-tooth is settled down to the designed value, which only takes several switching CLK periods.

In the implementation, the tolerance of Vamp, Vvalley, τ1, τ2, and τ3 all are unavoidable. Assume

$Vamp\cdot(1-\varepsilon)<Vamp\_real<Vamp\cdot(1+\varepsilon)$, $Vvalley\cdot(1-\varepsilon)<Vvalley\_real<Vvalley\cdot(1+\varepsilon)$,

$\tau1\cdot(1-\theta)<\tau1\_real<\tau1\cdot(1+\theta)$, $\tau2\cdot(1-\theta)<\tau2\_real<\tau2\cdot(1+\theta)$,

$\tau3\cdot(1-\theta)<\tau3\_real<\tau3\cdot(1+\theta)$.

The phase shift error among different channels will be $\frac{(\tau1+\tau2+\tau3)\cdot\theta}{T}\bullet 360$ degree.

The slope difference among different channels will be $\left(\frac{(\tau1+\tau2+\tau3)\cdot\theta}{T}+\varepsilon\right)\bullet 100\%$.

For example, if $(\tau1+\tau2)<5ns$, $\tau3<10ns$, $T=1us$,

$\varepsilon=0.005$ (a typical Bandgap Reference tolerance),

$\theta=0.5$ (a typical delay tolerance due to process variation)

Then, the phase shift error among different channels will be <3.6 degrees and the slope difference among different channels will be 1.5%. This is good enough for the requirements described in section 2.1.

In Fig. 2-11, since no layout matching is needed, Csh, Cea, Csaw all can be <1pF, (in a traditional multi-channel saw-tooth generator, Csaw is usually larger than 10pF for layout matching.) and Rea can be <100KΩ. The silicon size of the self-adjusting saw-tooth generator can be much smaller than the traditional scheme.

2.6. Hardware Verification of the Proposed Interleaving Scheme

A 3 phase/1MHz prototype hardware is developed according the interleaving scheme shown in Fig. 2-11. Fig. 2-13 shows the photo of the 3-channel interleaving prototype hardware. Fig. 2-14 shows the testing results of 2-phase interleaving; Fig. 2-15 shows the testing results of 3-phase interleaving.

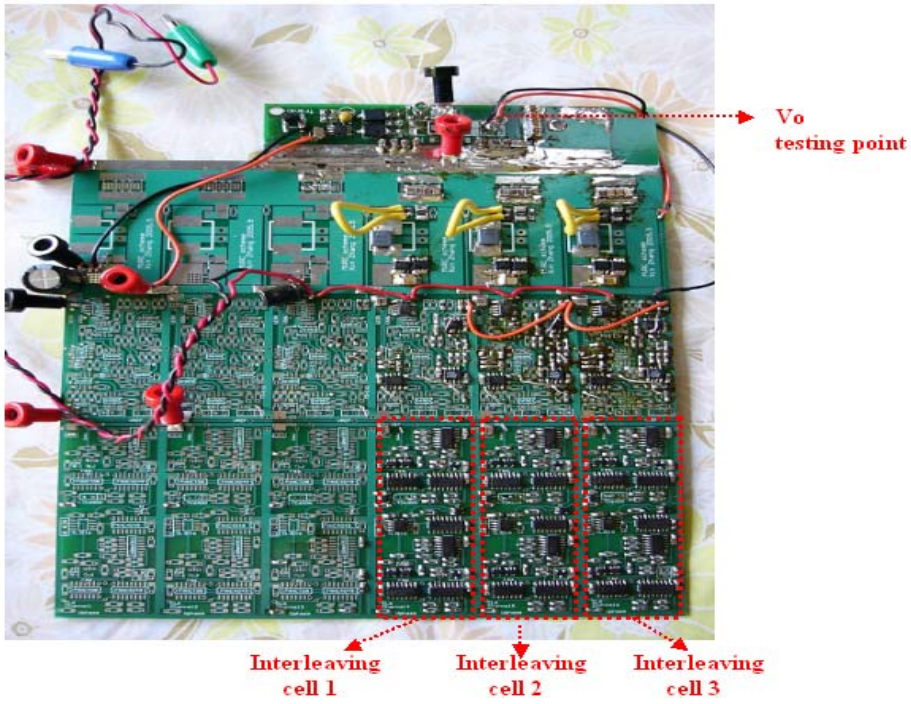
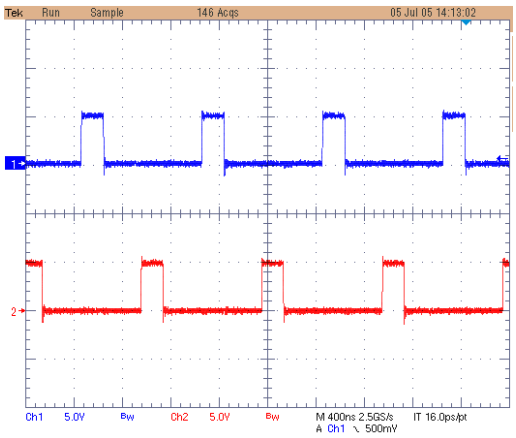
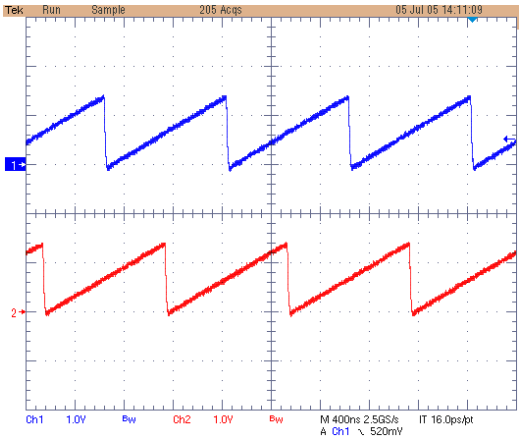


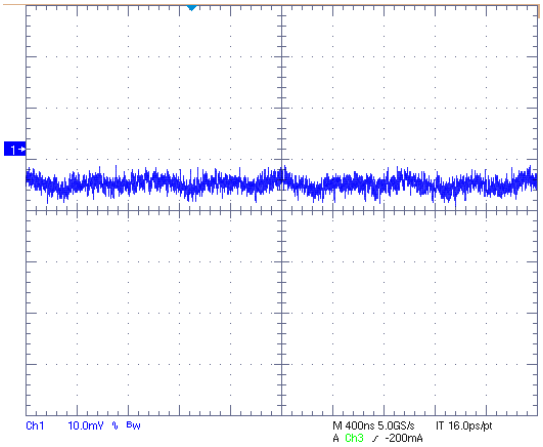
Fig. 2-13. Photo of the 3-channel interleaving hardware.



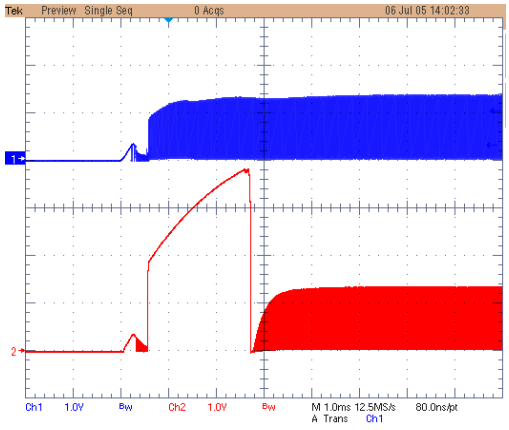
a. accurate shifted clock



b. matched saw-tooth

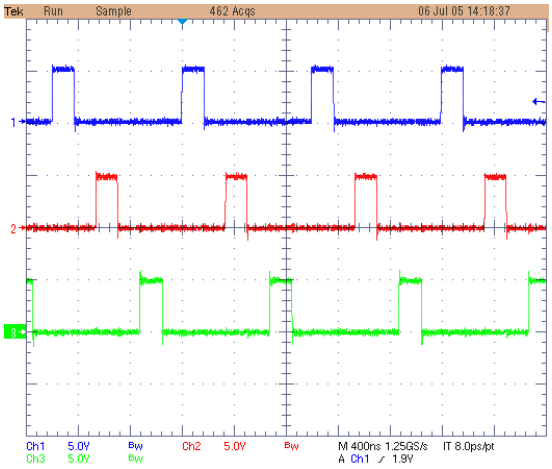


c. output voltage ripple

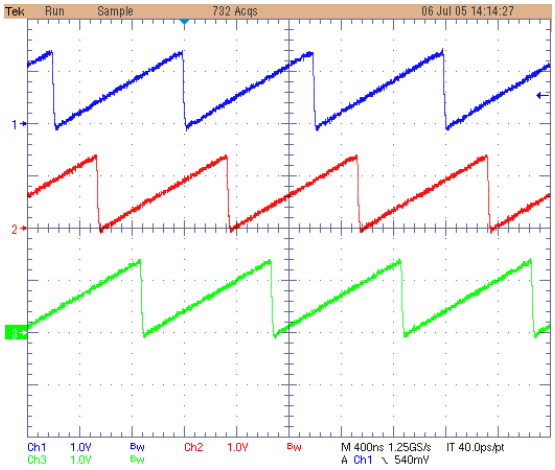


d. self-adjusting process

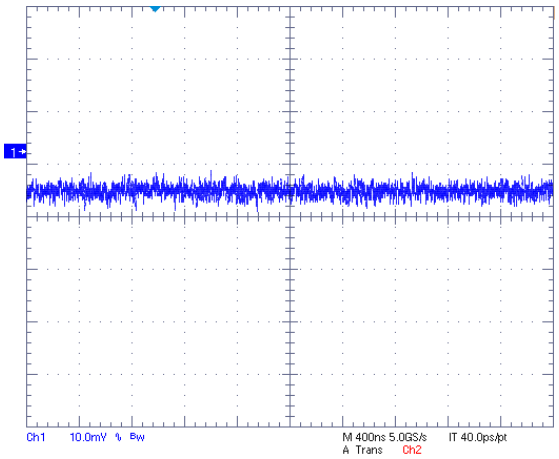
Fig. 2-14. Testing results of 2 phase interleaving.



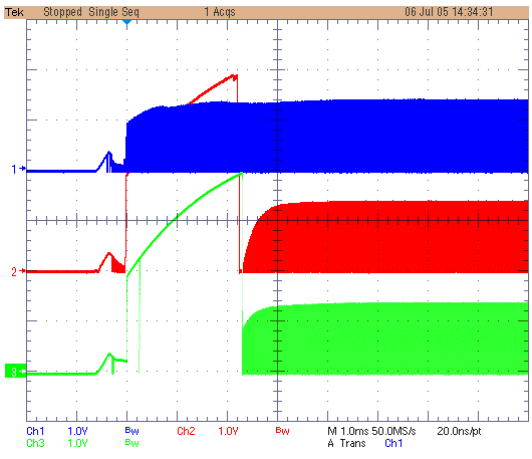
a. accurate shifted clock



b. matched saw-tooth



c. output voltage ripple



d. self-adjusting process

Fig. 2-15. Testing results of 3 phase interleaving.

As shown in Figures 2-14 and 2-15, the proposed interleaving blocks produce accurate shifted clock signals and matched saw-tooth signals to each channel. Figures. 2-14d and 2-15d show the "self-adjusting" process of the proposed saw-tooth generator. When the power of interleaving circuitry is just turned on, each channel's saw-tooth amplitude may have big difference. However, they settle down to the same value after hundreds of microseconds. The waveforms in Figures. 2-14 and 2-15 demonstrate the feasibility to use the proposed interleaving scheme for microprocessor power management.

As explained in section 2.4, key building block of the proposed interleaving scheme, a self-adjusting saw-tooth generator can be monolithic integrated without any external components. As shown in Fig. 2-11, other building blocks of this scheme are regular digital and analog circuitries whose monolithic integration has been verified by many commercial available products. Therefore, for each channel, the whole interleaving unit can be monolithically integrated without any external component. The monolithic integration of the proposed distributed interleaving scheme will be verified in Chapter 5.

2.7. Summary of Chapter 2

Interleaving is widely used in multi-cell converter systems especially for microprocessor power management. This application requires not only a very small phase shift error, but also strict carrier signal matching among different channels. Traditional centralized interleaving scheme depends on layout matching and trimming to meet the requirement and it is not practical for future's systems with a flexible channel number. The limitations of traditional centralized interleaving scheme have led to the exploration of distributed interleaving approach.

However, existing distributed interleaving schemes are not suitable or not convenient to achieve scalable phase design in microprocessor power management application. A novel distributed interleaving scheme is developed to serve the purpose. The proposed scheme can easily achieve scalable phase interleaving without changing many components. The scheme is verified by a 3 phase/1MHz prototype hardware. The key building block of the proposed interleaving scheme is a self-adjusting saw-tooth generator, which demonstrates the feasibility of monolithic integration without any external component. The proposed interleaving scheme can also be used in any cellular converter system.

Chapter 3. Distributed Adaptive Voltage Position And Current Sharing

3.1. AVP and Current Sharing Design Specifications

3.1.1. VRM-CPU Power Delivery Loop

To keep CPU working properly, the voltage of the CPU silicon die needs to be kept within a regulation window. However, the voltage across the CPU die cannot be directly accessed by the VRM controller because of the CPU packaging. Even though the VR controller can access the CPU die voltage directly, it cannot really control the voltage. Because the VR current slew rate is limited by VR inductor and control bandwidth [C1], it is an order lower than the current slew rate of the CPU die [C2]. The solution is to design a decoupling loop between the VR and the CPU die [C3]~[C5]. Instead of getting voltage feedback from the CPU die directly, the VRM gets voltage feedback from two of CPU package pins. The regulation window of CPU die voltage is mapped to the regulation window across these two package pins. The AVP specifications are defined at these two pins.

To understand the VR design specifications, we need to understand the power delivery loop from VRM to CPU first. From VR to CPU die, there is a long way to go. The decoupling elements are put on the motherboard inside the CPU package or even inside the CPU silicon die. The CPU packaging is no longer just a space transformer that bridges the gap between the fine silicon die features and the coarse features of the motherboard environment. It must be viewed as an integral part of the electrical solution [C6].

To design this complex power delivery loop, Intel developed a "3D distributed, integrated, lumped model" for the power delivery path [C6]. In this model, power distribution insider the CPU silicon die and the CPU package is modeled by a distributed 3D network in order to enhance prediction of the whole power system performance. This network is connected to the system motherboard through several inductive and resistive socket pin elements, which are terminated at one node on the motherboard. The motherboard, represented by its L, R, and C parasitics, in turn is connected to a simple VRM model consisting of the voltage regulator L, R, and C filters and input voltage source. Using the 3D model, we can get the voltage distribution inside the CPU package and even across the silicon die. We can also get the relationship between the voltage at different CPU package pins and the voltage across the CPU die. Therefore, a voltage budget can be done to meet the target regulation window on silicon die. And VR design specifications can be defined at CPU package pins based on the requirement of CPU silicon die.

The above 3D model can be simplified as a lumped model used for VR design verification. Fig. 3-1 is such a model of the power delivery loop of Pentium4 in a 478-pin socket. This lumped model does not provide the voltage distribution inside the CPU package. However, using this model in simulation, we can get typical values of the voltage across the decoupling elements at different locations on the power delivery loop. And the results agree with the simulation results using 3D model. Such a lumped model can be found in Intel's VR design guide.

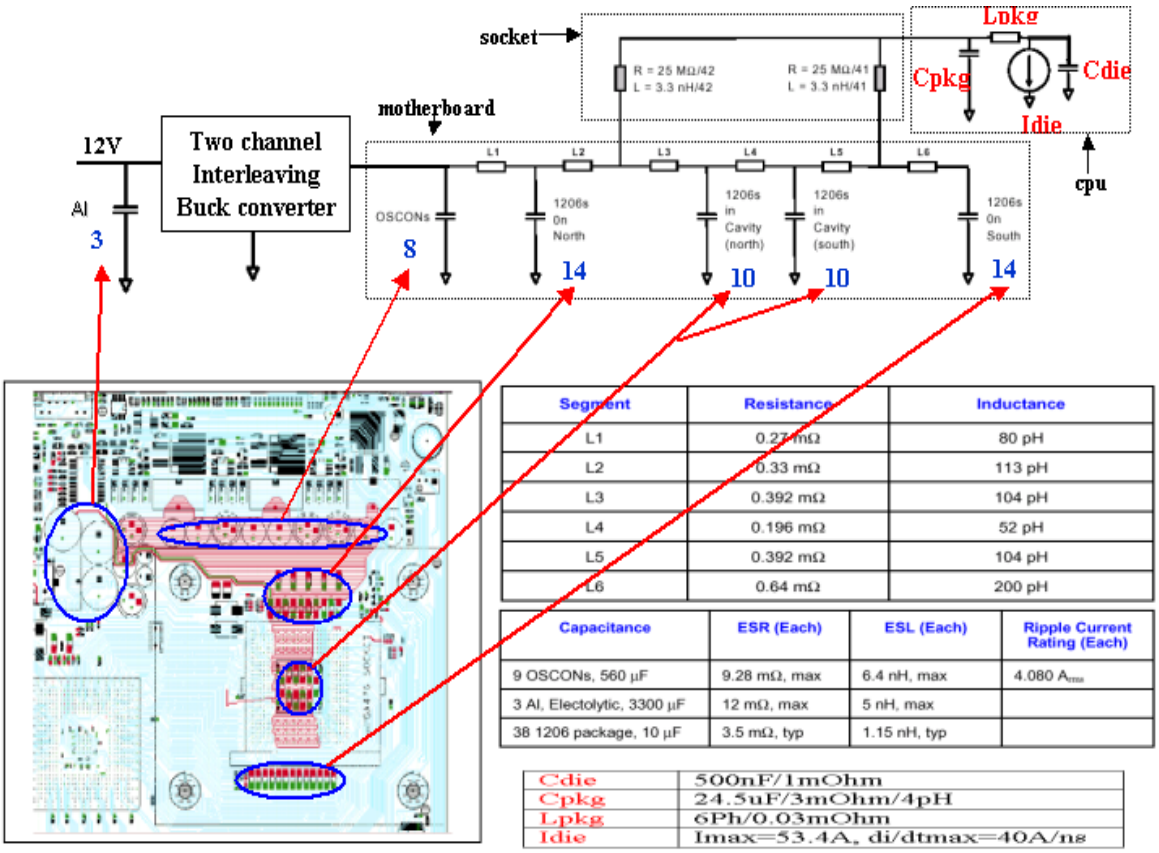


Fig. 3-1. A lumped model for CPU power delivery. [C7]

3.1.2. AVP Design Specifications

Adaptive Voltage Position was first proposed by Analog Device, a company producing VR controllers [C8]. As shown in Fig. 3-2, AVP means that the DC output voltage of a converter is dependent on its load. It is set to the highest level within the specification window at no-load condition and to the lowest level at full-load. This approach increases the output-voltage dynamic tolerance by as much as twofold, and thus reduces the number of bulk capacitors required to meet the output voltage regulation window. More importantly, it reduces the average power the microprocessor consumes, and therefore saves lots of cost of CPU packaging to deal with the heat. Now, AVP is widely adopted by Intel, AMD and other microprocessor manufacturers. The AVP load

line of CPU silicon die is optimized based on the tradeoff between CPU thermal cost and CPU performance [C9]. Today, the VR load line is defined based on the AVP of the CPU silicon die.

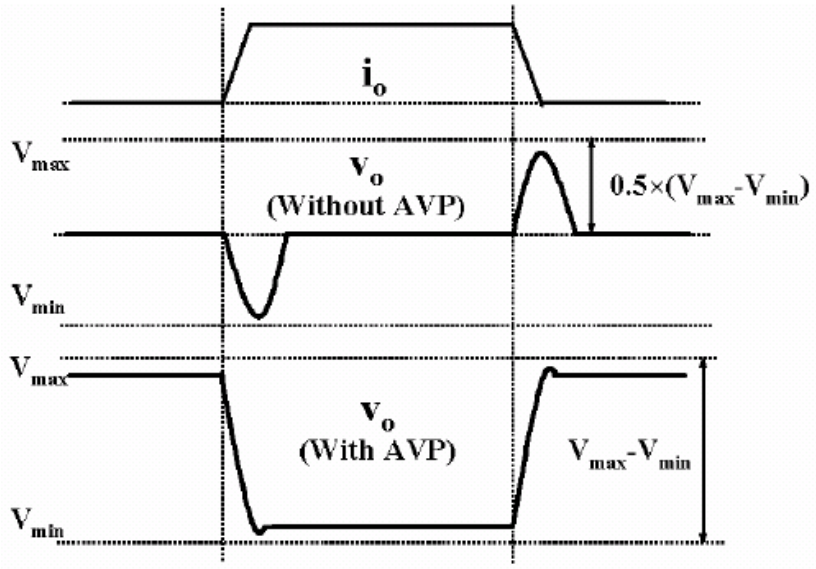


Fig. 3-2.Transient with and without AVP.

Fig. 3-3 shows the mapping of CPU die's AVP window that is defined at CPU die, and VRM AVP window that is defined at CPU package pin. The blue region is CPU die's AVP window. The green one is VR AVP window. Based on the Monte-Carlo simulation using the 3D model, to guarantee the voltage across CPU silicon die within the blue region, the voltage across two specifically selected package pins ("the worst case pins") should be kept within the green region. In other words, if the voltage across the specifically selected package pins can be controlled within the green region, in most of the cases, as shown in Fig. 3-4, the voltage across CPU silicon die will be kept within the blue region. But in some extreme case, as shown in Fig. 3-5, the voltage across CPU die can be beyond the blue range even when the voltage at CPU package pin is kept within the green range.

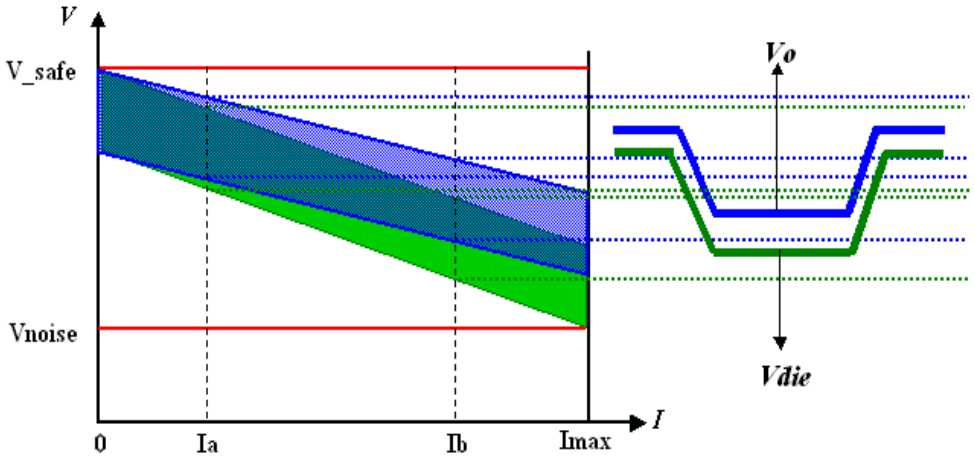
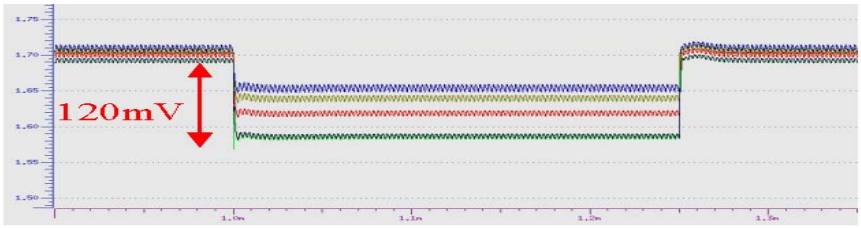
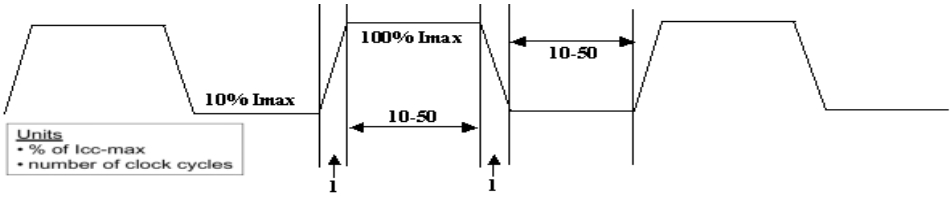


Fig. 3-3. CPU die's AVP window (blue) and VRM AVP window (green).

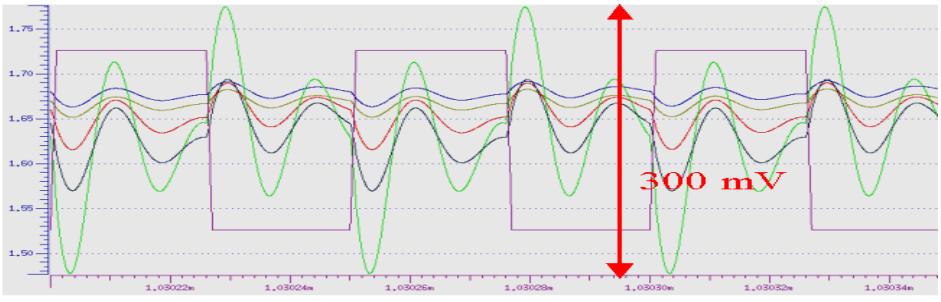


Blue: voltage @VRM output nodes; Green: voltage @ CPU die.

Fig. 3-4. AVP transient at different locations of the power delivery loop [C7].



(a) CPU load current waveforms



(b) Voltage waveforms at different points of the decoupling loops

Fig. 3-5. Transient response when the processor runs a testing program [C7].

Blue: voltage @VRM output nodes; Green: voltage @ CPU die.

Different CPUs may have different CPU AVP windows and VR AVP windows. Today's VR design guidelines from Intel provide the detailed description of VR AVP window [C10]~[C14]. To keep CPU working properly, VR needs to have a well-controlled load line defined by the line "R_{LL}" in the above picture. However, due to the tolerance of components, temperature variation, and output voltage ripples etc, a tolerance band is allowed. In high volume manufacturing, within 3σ, VR output voltage needs to be kept within MAXLL and MINLL in steady state. At transient, VR output voltage needs to be kept within the range between the maximum 0 load voltage and the minimum full load voltage. Many processors today allow the spike beyond the maximum 0 load voltage at current unloading step [C12]~[C14]. Today, VR AVP window specifications, VID is about 1.5V; R_{LL} is about 1.5mΩ; TOB is 25mV; in the future, VID would be 0.8V, R_{LL} be about 0.8V; TOB be 20mV. [C15]

3.1.3. Current Sharing Design Specifications

Today's VRs all adopt multi-cell converters as the power stage. Current sharing among each channel is required to get better thermal distribution across the board and to reduce the current stress of the components. However, the value of current sharing between two channels is not defined in Intel's VR design guidelines.

Based on industry's practice, current sharing index is define at full load condition:

CS=(Imaxchanne-Iminchannel)*N/Io,

where N is the channel number, and Io is the VR output current.

10% is a decent value of current sharing among each channel [C16].

3.2. Investigation of Traditional AVP and Current Schemes

3.2.1. Generic Architecture of VRM Controller

To meet the requirements of AVP and current sharing specifications, there are different control approaches. Because of the huge market, lots of companies join the competition of VRM controller design and fabrication. Wellknown names such as Intersil, Analog, Fairchild, Semtech, Onsemi, National, Maxim, Micrel, Ti, IR, ST and Linear Tech are in this list. Different companies have different control approaches. New designs appear each year in each company [A16].

It is difficult to have systemic comparison for all these controller architectures. Even classification of these controllers is not an easy task. To meet the specifications for desktop VRM9.X, VRD 10.X or to meet IMVP specifications for laptop, the controllers have many control loops mixed together. The big three are voltage loop, current sharing loop and AVP (Adaptive Voltage Position) loop. Some people think VR controllers can be classified as linear and nonlinear ones. But almost all the VR designs saturate the duty at large load step transient especially from heavy load to light load. The “linear” become “nonlinear” at that time.

However, thinking from IC design point of view, the architecture of a VR controller becomes clear. My research in this area does identify a generic VR architecture, as shown in Fig. 3-6. The state of the art energy processor is a multi-channel interleaving synchronous BUCK converter. The VR controller is the signal processor. The top-level building blocks of this signal processor were identified, namely the modulator, the compensator and the sensor. Together, they realize the three basic functions: active current sharing, Adaptive Voltage Position and interleaving.

To perform signal processing by electronic circuitry, signals (data/information) can be formatted with one of the four following templates: A. analog voltage waveforms; B. analog current waveforms; C. digital voltage waveforms; (e.g. “Smaller than 0.5V” = ‘0’ and “larger than 4.5V” = ‘1’.) D. digital current waveforms. (e.g. “Smaller than 0.5uA” = ‘0’ and “larger than 4.5uA” = ‘1’.)

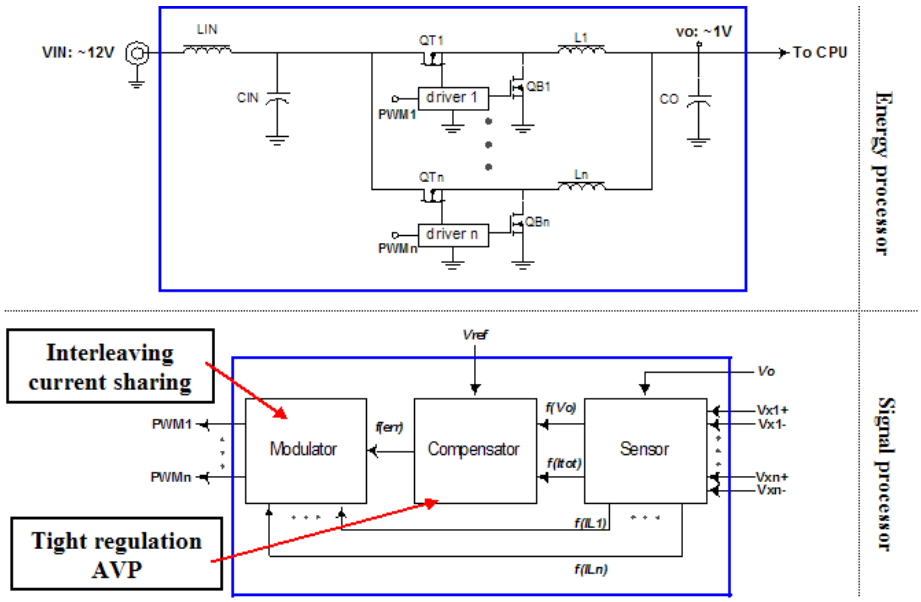


Fig. 3-6. Generic VR architecture.

PWM1~PWMn: Pulse Width Modulation signals;
f(err): VR voltage error signals;
f(Vo): sensed VR output voltage signals;
f(Itot): sensed VR output current signals;
f(IL1)~f(ILn): sensed inductor current signals for each channel;
Vo: VR output voltage;
Vx1+ ~Vxn-: voltage across current sensing element for each channel;
f(Itot) may not exist in some controller if f(IL1)~f(ILn)exist;
f(IL1)~f(ILn): may not exist in some controller if f(Itot) exists;

For the VR controller, the outputs of the signal processors (PWM1~PWMn in Fig. 3-6) have to be in format C. The sensor inputs of the controller (Vo, Vx1+, Vx1-, … Vxn+, Vxn- in Fig. 3-6) have to be in format A. (The controller gets inductor current

information from the voltage across the sensing element in the power stage.) And the reference input has to be in format C. (e.g. 6 bit VID in VRD 10.x)

Most of today's available commercial controllers only process signals in format A (often called analog VRM controller and usually f(vo) = Vo in Fig. 3-6). Some of them can process signals in format C (often called digital VRM controller and ADCs needed in the sensor block in Fig. 3-6). However, the signals inside the controller (e.g. f(Vo), f(Itot), f(err), f(iL1) ~ f(iLn) in Fig. 3-6) can be in any of the four formats mentioned above. For simplicity, in the following controller review sections, I only draw the scheme of analog voltage controller.

3.2.2. A short review of VRM controller

According to the generic VRM architecture in section 3.2.1, we can classify VR controllers by modulator, by compensator and by current sensor. Fig. 3-7 shows such a classification.

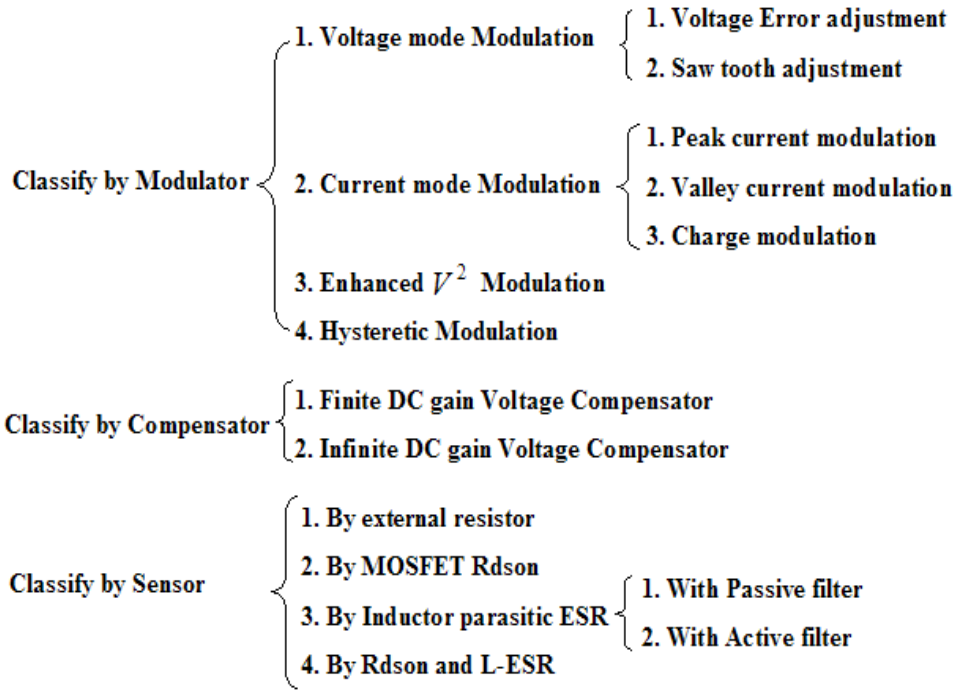


Fig. 3-7. Classification of VR control approaches.

A. Modulator

The modulator makes the comparison between the error signal and the carrier signal produce a digital PWM signal. For voltage mode modulation, the carrier signal is built in the controller chip and often in the format of a voltage saw-tooth waveform. For current mode modulation, the carrier signal comes from the power stage current information.

In today's VR controller products, current sharing performance is often decided by modulator design. Using current mode modulation, the current balance among each channel is guarantied. This includes peak current modulation [C17] as in Fig. 3-8, valley current modulation [C18] as in Fig. 3-9 and charge modulation [C19] as in Fig. 3-10. To achieve current sharing with voltage mode modulation, special techniques need to be adopted. The popular ways to do it are "voltage error adjustment" [C20] as in Fig. 3-11 and "saw-tooth adjustment" [C21] as in Fig. 3-12.

People also use nonlinear modulation to improve the transient performance of a converter. This includes enhanced V^2 modulation [C22] as in Fig. 3-13 and hysteretic modulation.

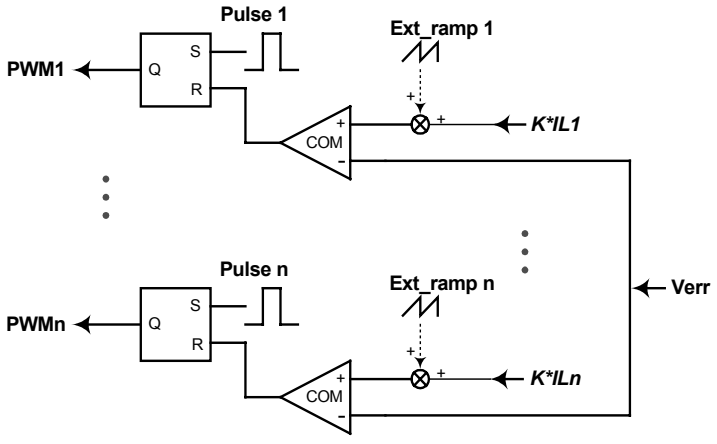


Fig. 3-8. Peak current modulation .

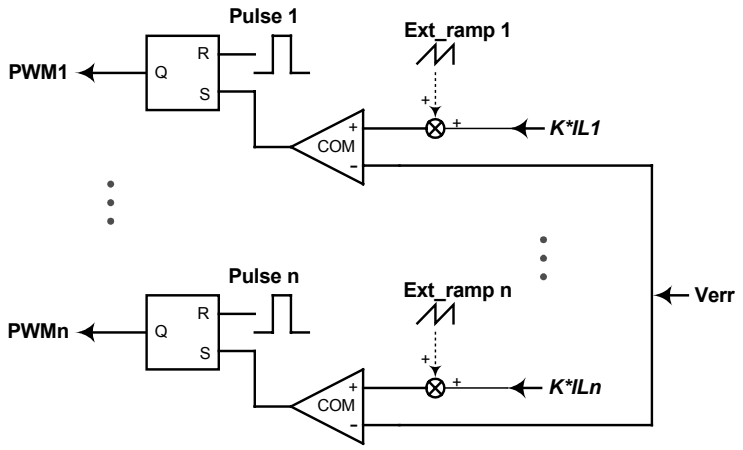


Fig. 3-9. Valley current modulation.

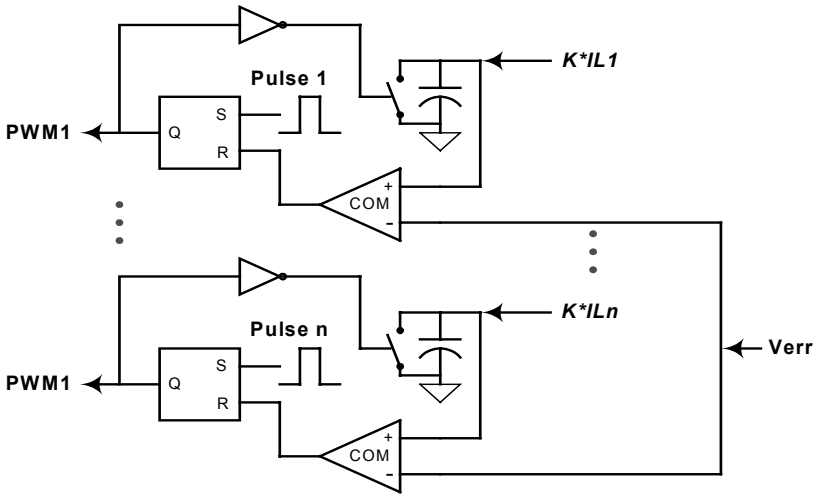


Fig. 3-10. Charge modulation.

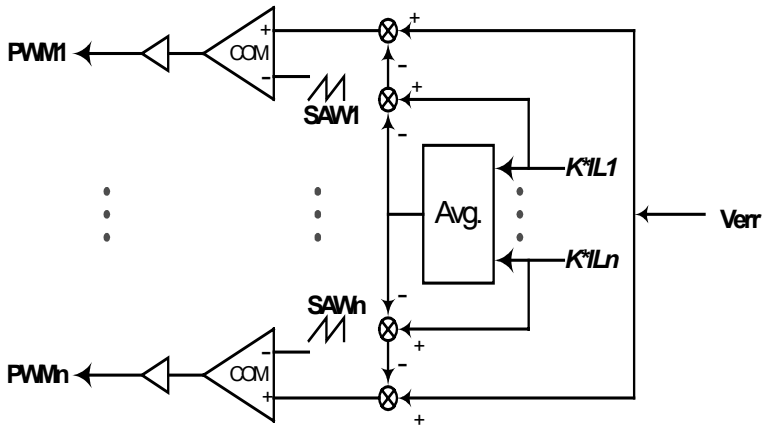


Fig. 3-11. Voltage error signal adjustment for each channel.

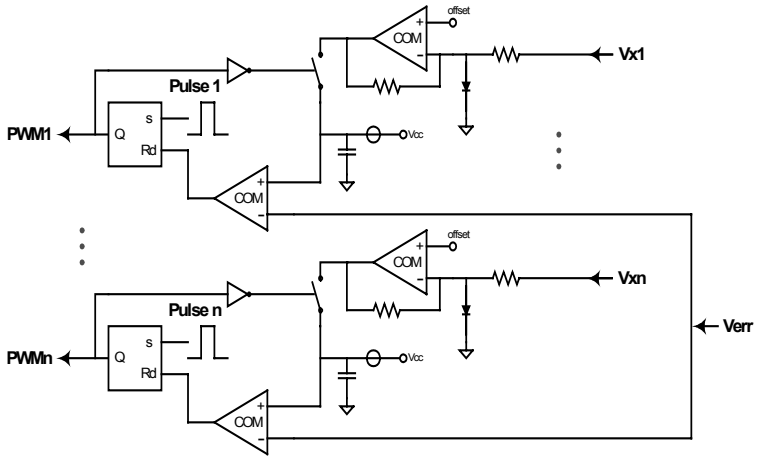


Fig. 3-12. Saw-tooth signal adjustment for each channel.

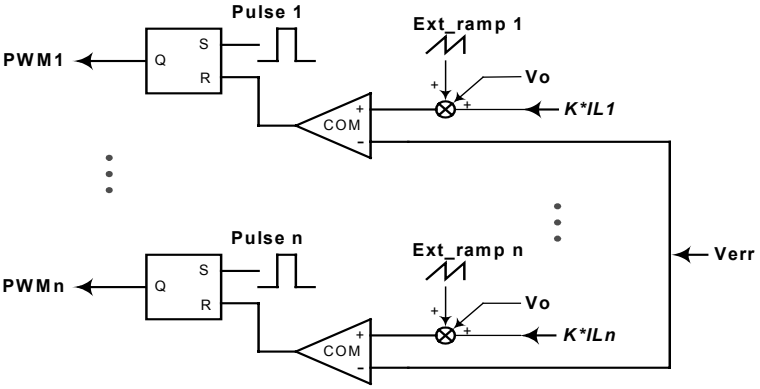


Fig. 3-13. Enhanced V^2 modulation.

B. Compensator

The compensator tries to add pole and zero and/or gain to the system. It could be a voltage Opamp surrounded by RC network, as shown in Fig. 3-14. Or it could be an operational transconduance amplifier (OTA/GM) with RC load, as shown in Fig. 3-15. Or it could be a digital filter implemented by DSP / FPGA/ ASIC if in digital VRM controller.

In today's VR controller products, AVP performance is decided by compensator design. A finite DC gain compensator is often used with current mode modulation to achieve AVP while an infinite DC gain compensator is often used with voltage mode

modulation to get AVP. The detailed design approach of the compensator can be found in [C23] and [C24]. The basic principle is the same: design a compensator to achieve constant close loop output impedance of the VR.

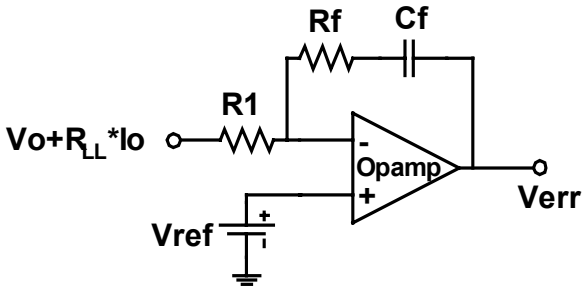


Fig. 3-14. Compensator implementation based on Opamp.

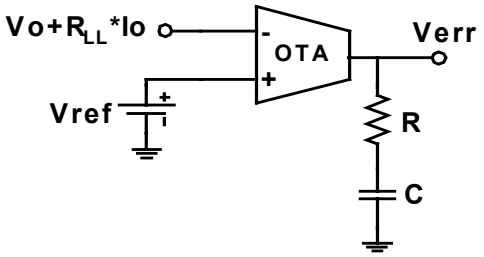


Fig. 3-15. Compensator implementation based on OTA.

C. Sensor

The sensor gets output voltage and inductor current and /or load current information of the power stage from the sensing elements and sends the information to modulator and compensator. The sensor also scales the information so that the signal can be in the operational range of the modulator and compensator.

Because large voltage drops on PCB trace, differential output voltage sensing is need in VRM controller.

For current sensing, we have resistor current sensing, Rdson current sensing, inductor current sensing [C25] and the combination of Rdson current sensing and inductor current

sensing [C26]. Resistor current sensing is most accurate, but it has huge power loss on the sensing resistor. Rdson current sensing adopts the on resistor of power MOSFET as sensing element, therefore no extra power loss. But the on resistor of power MOSFET has 30% variation due to the silicon process. Inductor current sensing adopts the DCR of each channel's inductor as sensing element, therefore no extra power loss. And the variation of the inductor DCR can be controlled within 5%. To meet the strict requirements of the tight VR AVP window, Intel only suggests resistor current sensing and inductor current sensing. And inductor current sensing is becoming more and more popular today due to the acceptable accuracy and 0 additional power loss. More detailed discuss of current sensing is provided in chapter 4.

Each company has its own combination of modulator, compensator and sensor. New controllers could be new combinations of the "old" blocks, or could be new designs of the blocks themselves. Table 3-1 is the summary of some popular VR controller products.

	Modulator					Compensator				Sensor				
	Voltage Mod.		Current Mod.		Enhanced V2 control	Finite DC gain	infinite DC gain			By Res	Rds CS	Ind. CS	Com CS	Int. CS
	Err	Saw	Peak	Valley			A	B	C					
HIP6301 (Intersil)	✓						✓				✓			
ADP3168 (Analog)		✓							✓					✓
SC2424 (Semtech)			✓			✓				✓				
Fan5091 (Fairchild)				✓		✓					✓			
CS5307 (Onsemi)					✓			✓				✓		
ADP3160 (Analog)			✓			✓				✓				
SC2643 (Semtech)			✓						✓				✓	

Table 3-1. Summary of some popular VRM controllers.

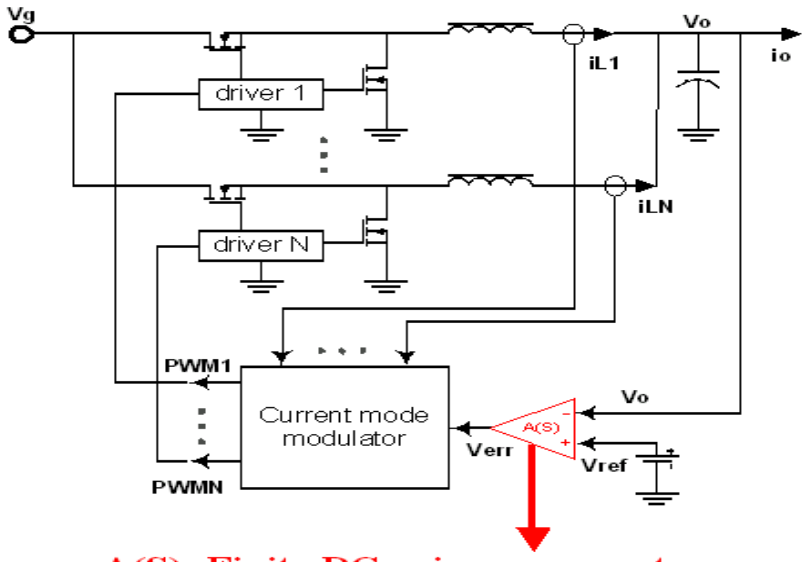
3.3. Issues of Centralized AVP and Current Sharing Schemes

Although all the commercial VRM controllers are acceptable for today's VRM application, they have limitations to achieve scalable phase design because of the centralized architecture. Section 2.2 has already identified the limitations of traditional interleaving scheme. The following will address the issues of the traditional AVP and Current sharing scheme.

3.3.1. Limitations of the Traditional AVP Scheme to Achieve Scalable Phase Design

To achieve AVP, traditional controls adopt a dedicated AVP loop. Two of the most popular AVP approaches are: 1) Current mode modulator with a finite DC gain compensator; 2) Voltage mode modulator with an infinite DC gain compensator.

3.3.1.1. AVP Approach 1



$$Io = ILtot = K \cdot A \cdot (Vref - Vo)$$

$$\Rightarrow \quad Vref = Vo + \frac{1}{K \cdot A} Io$$

Fig. 3-16. AVP approach 1

---- Current mode modulator with a finite DC gain compensator.

Fig. 3-16 shows AVP approach 1 ---- Current mode modulator with a finite DC gain compensator.

This approach adopts current mode modulator (including peak current modulation, as shown in Fig. 3-8, valley current modulation, as shown in Fig. 3-9, and charge modulation, as shown in Fig. 3-10) with a finite DC gain compensator to build the AVP loop. In steady state, seen from the input of this finite DC gain compensator, we have $Verr = A \cdot (Vref - Vo)$, where A is the finite DC gain. Because current mode modulation is adopted, *Verr* has its physical meaning and is proportional to the inductor current. The inductor current is equal to the output current within the control bandwidth. Then we have $Io = K \cdot Verr$, K is a constant value.

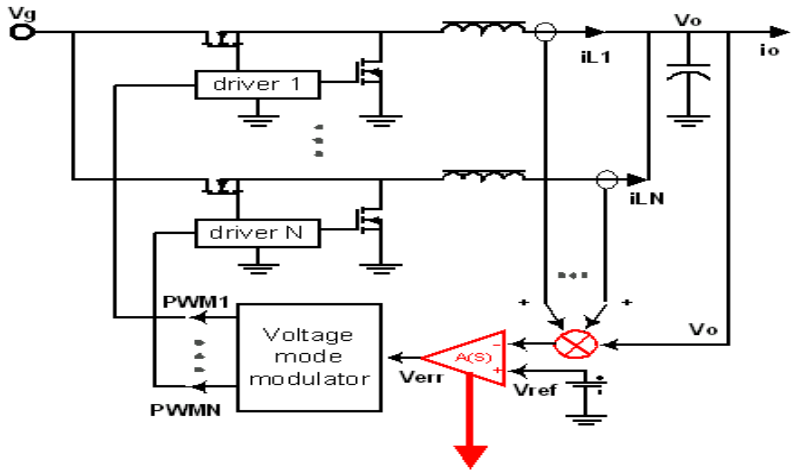
Based on the two equations: a. $Verr = A \cdot (Vref - Vo)$ b. $Io = K \cdot Verr$,

Then, we have $Vref = Vo + \left(\frac{1}{K \cdot A}\right) \cdot Io$. A well-controlled load line is achieved and the droop resistance is equal to $\left(\frac{1}{K \cdot A}\right)$. By proper compensator design according to [C27], good AVP transient performance can also be achieved.

However, this AVP scheme cannot be distributed according to Fig. 1-13 to achieve scalable phase design. This is simply because the *Verr* comes from a single compensator and cannot be distributed into each channel (although the multiphase current mode modulator can be evenly divided to N parts).

3.3.1.2. AVP approach 2

Fig. 3-17 shows AVP approach 2 ---- Voltage mode modulator with an in finite DC gain compensator.



A(S): Infinite DC gain compensator

$$Ri \cdot Io + Vo = Vref$$

$$\Rightarrow \quad Vref = Vo + Ri \cdot Io$$

Fig. 3-17. AVP approach 2

---- Voltage mode modulator with an infinite DC gain compensator.

This approach adopts a voltage mode modulator and an infinite DC gain compensator to build the AVP loop. In steady state, seen from the input of this infinite DC gain compensator, we have $Vref = Vo + Ri \cdot iLtot$, where *iLtot* is the total inductor current and *Ri* is the current sensing gain. The total inductor current is equal to the output current within the control bandwidth. Then we have $Vref = Vo + Ri \cdot Io$. A well-controlled load line is achieved. And the droop resistance is equal to *Ri*. By proper compensator design according to [C28], good AVP transient performance can also be achieved.

However, this AVP scheme cannot be distributed according to Fig. 1-13 to achieve scalable phase design. This is because *Verr* comes from a single compensator and it cannot be distributed into each channel. And the "adder block" needs to get current information from each channel.

There are other AVP schemes in today's VRM controller products. But they are similar to the approaches described above and cannot be distributed according to Fig. 1-13 to achieve scalable phase design.

3.3.2. Limitations of Traditional CS Schemes to Achieve Scalable Phase Design

To achieve current sharing among each channel, traditional controllers depend on modulators instead of using active current sharing buses. Two of the most popular current sharing approaches are: 1) Current mode modulation; 2) Improved voltage mode modulation with current balance function.

3.3.2.1. Current Sharing Approach 1

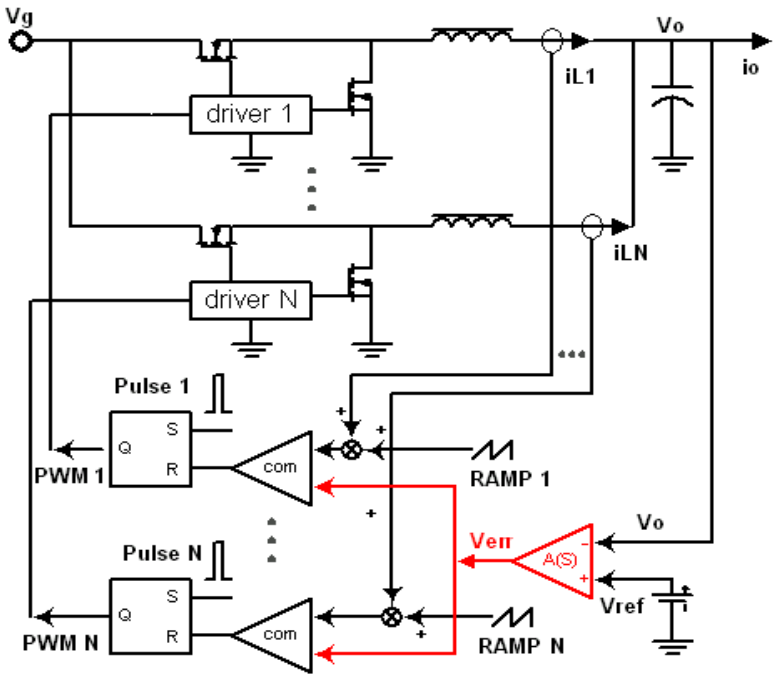


Fig. 3-18. Current sharing approach 1 ---- current mode modulation.

Fig. 3-18 shows current sharing approach 1 ---- Current mode modulation. Current mode modulation can provide the current sharing function if each channel has the same current reference [C29]. In Fig. 3-18, the output of the voltage loop compensator Verr works as this current reference for each channel.

However, this current sharing scheme cannot be distributed according to Fig. 1-13 to achieve scalable phase design. This is simply because Verr comes from a single compensator and cannot be distributed into each channel (although the multiphase current mode modulator can be evenly divided into N parts).

3.3.2.2. Current Sharing Approach 2

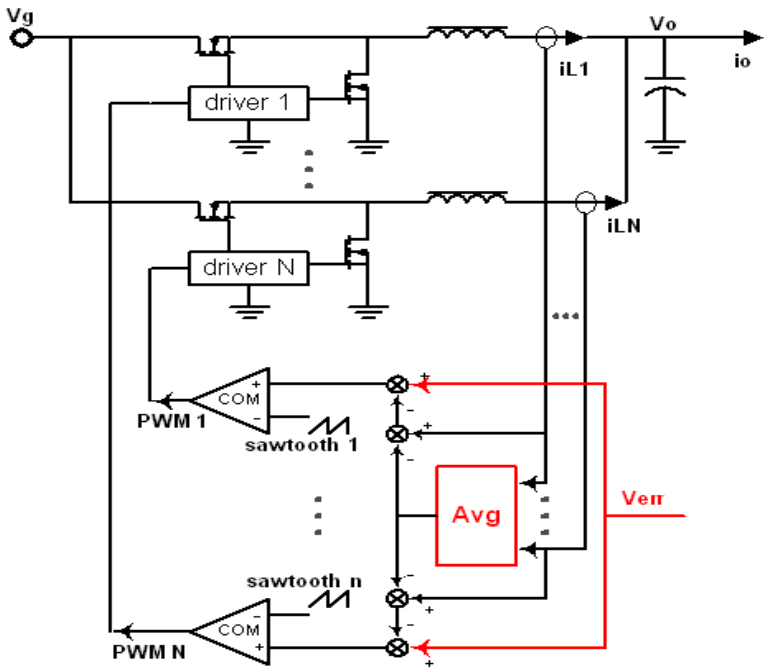


Fig. 3-19 Current sharing approach 2

---- Improved voltage mode modulation with current balance function.

Fig. 3-19 shows current sharing approach 2 ---- improved voltage mode modulation with current balance function. As described in section 3.2.2, there are many ways to improve original voltage mode modulation to achieve the current sharing function. Fig. 3-19 just shows the implementation with "error signal adjustments."

To achieve the current sharing function, this scheme adopts an "average" block to get average value of different channels' inductor current information, and then use the difference of each channel's current and this average value as an index to adjust the

original Verr signal. If each channel's inductor current is the same, this scheme is equal to the original voltage mode modulation. If there is current difference among different channels, this scheme can force current balance according to the above "error signal adjustments" mechanism.

However, this current sharing scheme cannot be distributed according to Fig. 1-13 to achieve scalable phase design. This is because Verr comes from a single compensator and it cannot be distributed into each channel. And the "average block" needs to get current information from each channel.

There are other current sharing schemes in today's VRM controller products. But they are similar to the approaches described above and cannot be distributed according to Fig. 1-13 to achieve scalable phase design.

As addressed in chapter 1, scalable phase design with the same type of ICs is the technology trend to meet the quickly changing specifications of CPU power requirements and to reduce the cost of developing different control ICs. It also provides engineers the flexibility to optimize the number of phase to achieve better system design tradeoff. However, as discussed in this section, today's VR control ICs have their limitation to achieve scalable phase design due to the centralized architecture. Some ICs may offer a programmable number of phases within a limited range (usually 2~4) at the cost of unused or redundant die area and package pins. Distributed control architecture needs to be developed to achieve scalable phase design for the microprocessor power management.

3.4. A Novel Distributed AVP and Current Sharing Scheme

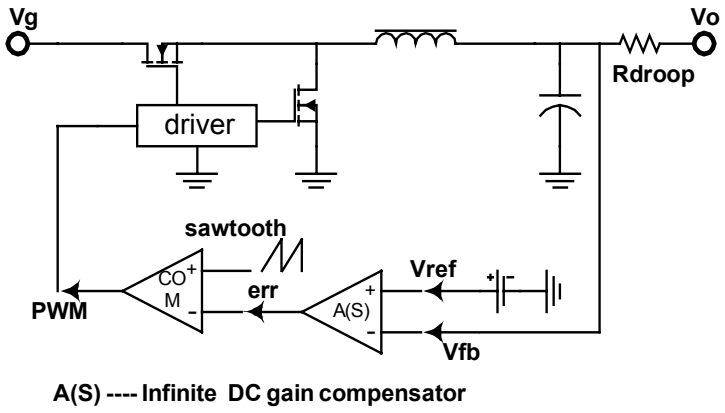
As addressed in section 3.3, traditional AVP and current sharing schemes cannot be evenly divided into N parts according to Fig. 1-13 to achieve scalable phase design. New schemes need to be developed to serve the purpose.

3.4.1. Distributed AVP Scheme Development

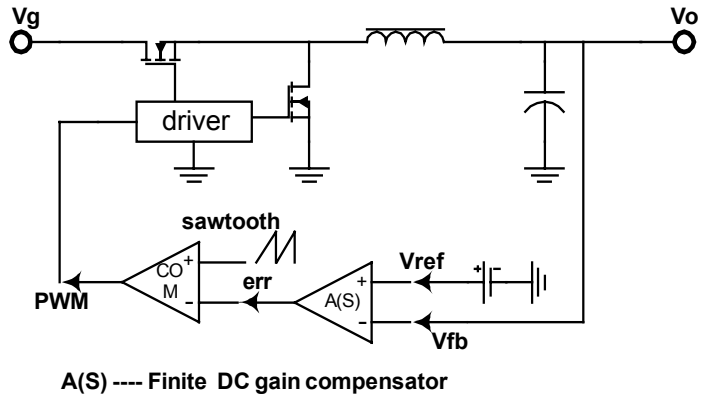
3.4.1.1. Build a Well-Controlled Load Line to One Channel

Since each MVRC chip described in section 1.3 can work alone as a POL power supply. The control part of the MVRC chip needs to have all the necessary building blocks to realize the one-channel control. Since AVP is adopted not only in CPU power management, but also widely in POL application, the MVRC chip needs to provide the AVP function even when used alone to supply a POL load.

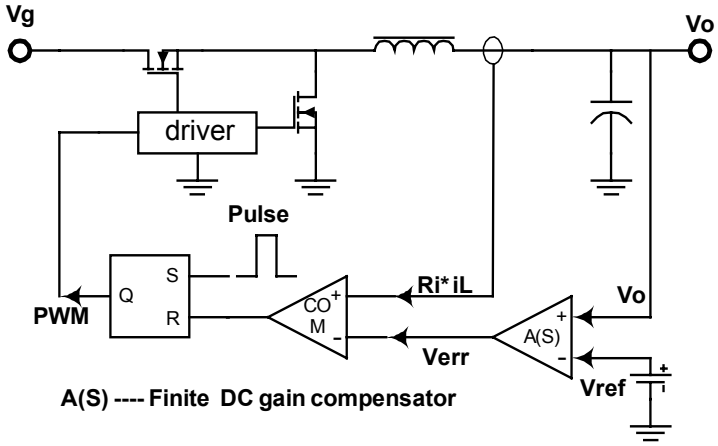
As shown in Fig. 3-20, there are basically 4 approaches to build a load line with a one-channel converter, that is, a. Voltage modulation + infinite DC gain compensator + droop resister; b. Voltage modulation + finite DC gain compensator; c. Current modulation + Finite DC gain compensator; d. Non-current modulation with load-dependent reference voltage + Infinite DC gain compensator.



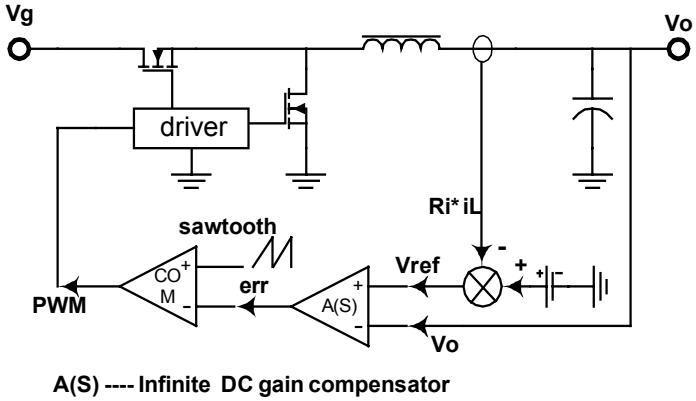
a. Voltage modulation + infinite DC gain compensator + droop resister



b. Voltage modulation + finite DC gain compensator



c. Current modulation + Finite DC gain compensator



d. Voltage mode modulation with load-dependent reference voltage

+ Infinite DC gain compensator

Fig. 3-20. Different AVP approaches.

However, not all of these four approaches meet the tight requirements of modern POL and CPU power management. Approach a has huge power loss because a resistor with the value equal to the specified VR load-line resistance is put in the power stage.

Approach b has huge load-line variation. The input voltage, the efficiency, and the compensator DC gain variation all have impact on the load line realized.

Approach c is widely used in VR controller products as described in section 3.2. This approach has no extra power loss but a good AVP window. The droop variation is only related to *Ri* variation and compensator DC variation. The challenge is cycle-by-cycle current sensing needed.

Approach d becomes more and more popular to achieve AVP in today's VR controller products. The benefit is no extra power loss but even better AVP window. The droop variation is only related to *Ri* variation. Although current sensing is needed, but cycle-by-cycle current sensing is not necessary, as long as the sensed signal can follow the large current transient within the control bandwidth.

Based on the discussion above, approach d is selected to build a well-controlled load line for a one channel BUCK converter. Instead of using a load-dependent reference voltage, I use the equivalent scheme, as shown in Fig. 3-21, in which a constant reference voltage is adopted. The sensed inductor current and output voltage are added together and sent to the compensator. With proper compensator design, we can get a well-controlled output impedance within the control bandwidth so that when we look from the output side, the one channel BUCK converter is equivalent to a voltage source in series with a resistor. The value of this voltage source is equal to the voltage reference and the

resistance is equal to current sensing gain *Ri*. Both Vref and Ri can be well controlled in IC design.

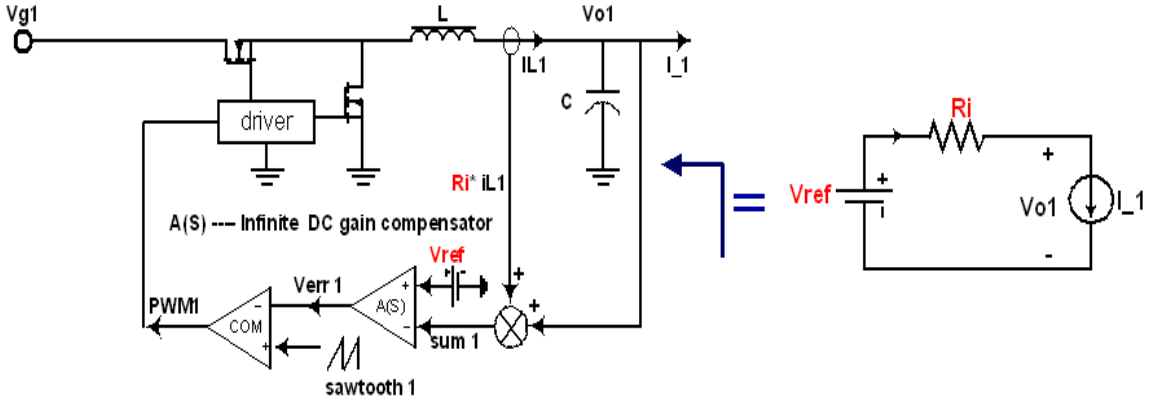


Fig. 3-21. One channel active droop control.

An infinite DC gain compensator is necessary in Fig. 3-21. The compensator design begins from the derivation of the small signal model of the power plant. Fig. 3-22 shows the small signal model of a synchronous BUCK converter. The top three perturbations of the power stage are output current, input voltage, and duty cycle. The state variables selected here are the inductor current and the output voltage. Table 3-2 shows the transfer functions used in Fig. 3-22.

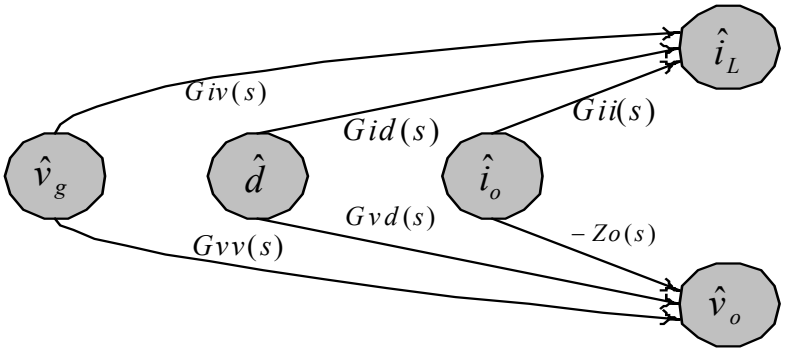


Fig. 3-22. The small signal model of VRM power plant.

Parameters	Transfer functions
$R_L' = R_L + Rdson$	$Gid(s) = Vg \cdot \frac{s \cdot C}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$
$\omega o = \frac{1}{\sqrt{L \cdot C}}$	$Gvd(s) = Vg \cdot \frac{1 + \frac{s}{\omega z\_cap}}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$
$Q = \sqrt{\frac{L}{C}} \cdot \frac{1}{(R_C + R_L')}$	$Giv(s) = D \cdot \frac{s \cdot C}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$
$\omega z\_ind = \frac{R_L}{L}$	$Gvv(s) = D \cdot \frac{1 + \frac{s}{\omega z\_cap}}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$
$\omega z\_cap = \frac{1}{R_C \cdot C}$	$Gii(s) = \frac{1 + \frac{s}{\omega z\_cap}}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$
	$zo(s) = R_L \cdot \frac{\left(1 + \frac{s}{\omega z\_cap}\right) \cdot \left(1 + \frac{s}{\omega z\_ind}\right)}{1 + \frac{s}{Q \cdot \omega o} + \frac{s^2}{\omega o^2}}$

Table 3-2. Transfer functions (Assume Rdson of all the devices is the same).

Fig. 3-23 shows the small signal model of AVP design with the scheme shown in Fig. 3-21. Vpp is peak-to-peak amplitude of the saw tooth inside the controller. *Rdroop* specifies the required AVP load line. *Rdroop* is also the current sensing gain in this scheme. And *A(s)* is the compensator needed to be designed. To analyze AVP design, the input voltage perturbation can be ignored.

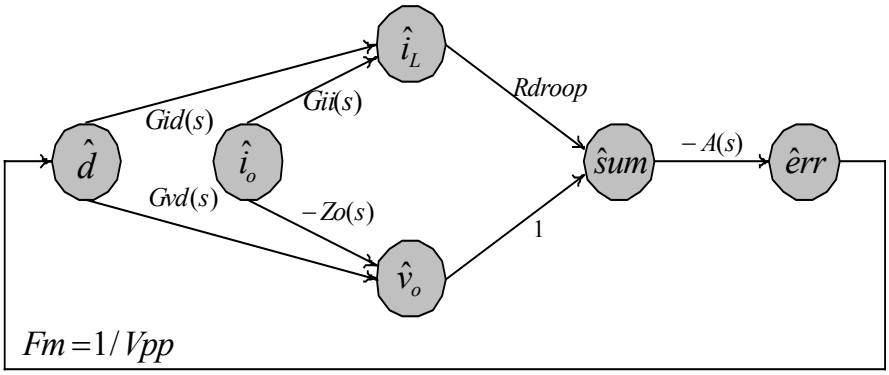


Fig. 3-23. AVP design scheme.

Using S.J.Mason's formula, we have:

$$zout(s) \equiv -\frac{\hat{vo}(s)}{\hat{io}(s)}$$
$$= \frac{zo(s)\cdot\left(1+Gid(s)\cdot Rdroop\cdot A(s)\cdot Fm\right)+Gii(s)\cdot Rdroop\cdot A(s)\cdot Fm\cdot Gvd(s)}{1+Gvd(s)\cdot A(s)\cdot Fm+Gid(s)\cdot Rdroop\cdot A(s)\cdot Fm}$$

If we define

Current loop gain $Ti(s) \equiv Gid(s)\cdot Rdroop\cdot A(s)\cdot Fm$,

Voltage loop gain $Tv(s) \equiv Gvd(s)\cdot A(s)\cdot Fm$, and

Out loop gain $T2(s) \equiv \frac{Tv(s)}{1+Ti(s)}$,

The close loop output impendence $zout(s) = \frac{zo(s)\cdot\left(1+Ti(s)\right)+Gii(s)\cdot Rdroop\cdot Tv(s)}{1+Ti(s)+Tv(s)}$.

To force $zout(s) = Rdroop$, the compensator needs to be:

$$A(s) = \frac{zo(s)-Rdroop}{Rdroop\cdot Fm\cdot\left(Gvd(s)+Rdroop\cdot Gid(s)-zo(s)\cdot Gid(s)-Gii(s)\cdot Gvd(s)\right)}$$

In practice, simplification of the above equations is achievable [C1] [C24] [C27] [C28].

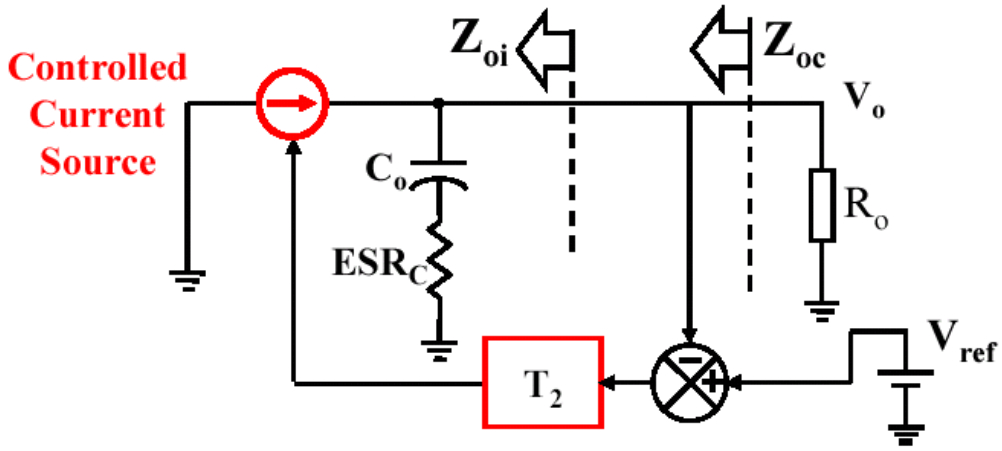


Fig. 3-24. The simplified model with active droop control.

Assume the system shown in Fig. 3-21 has a high bandwidth current-loop gain *Ti(s)*, and then when the current loop is closed and the voltage loop is open, the BUCK converter operates as an ideal current source, as shown in Fig. 3-24. Its output impedance can be approximately represented as:

$$Zoi(s) = \frac{1}{s \cdot C} + Rc = \frac{1 + \frac{s}{\omega\_cap}}{s \cdot C}$$

When the voltage loop is closed, the closed-loop output impedance is:

$$Zoc(s) = \frac{Zoi(s)}{1 + T2(s)}$$

With a logarithm union, the closed-loop output impedance is:

$$Zoc(s) = \begin{cases} Zoi(dB) - T2(dB) & (T2 >> 1) \\ Zoi(dB) & (T2 << 1) \end{cases}$$

Based on above equations, if the system loop *T2* is designed with a -20dB/dec slope and a bandwidth ωc equal to ω_cap, the close loop output impendence Zoc(s) will be equal to *Rc*.

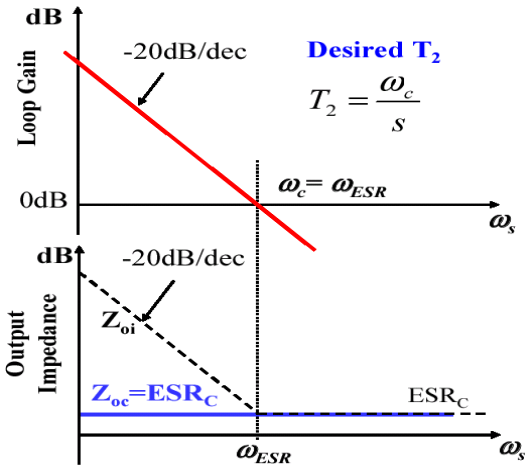


Fig. 3-25. Constant output impedance design with $\omega c = \omega\_cap$.

However, in practice, Zoc(s) needs to be designed according to specified VR load-line droop resistance R_{LL}. In many cases, it is not practical to design $\omega\_cap = R_{LL}$, and $\omega c = \omega\_cap$. For example, in high frequency application, ceramic capacitors are often adopted as output capacitors. The ESR zero of ceramic capacitor is beyond 1 MHz. It is not practical to achieve the 1MHz *T2* bandwidth.

Therefore a design strategy, as shown in Fig. 3-26, is often adopted for active droop control with ceramic output capacitors.

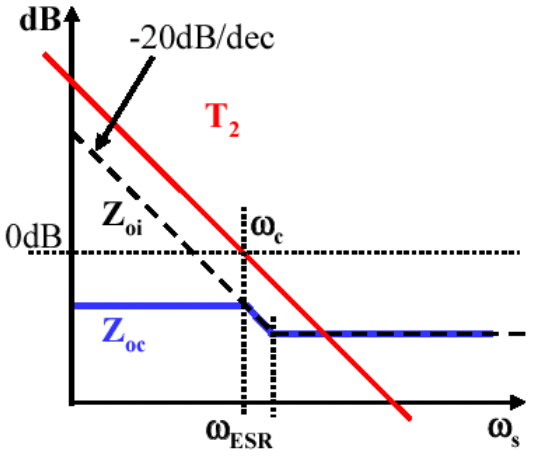


Fig. 3-26. A practical AVP design strategy.

According to Fig. 3-26, *T2* bandwidth is $\omega c < \omega\_cap$. The close loop output impedance is constant within the control bandwidth, and the impedance beyond the bandwidth is smaller than that in the lower frequency range. The phase margin at ωc needs to be beyond 60° to achieve a good AVP transient. For a system loop T2 designed with a -20dB/dec slope, there is no problem because the phase margin is about 90°.

The *T2* of the control scheme shown in Fig. 3-21 can be simplified as $T2(s) = \frac{1 + \frac{s}{\omega\_cap}}{Ri \cdot C \cdot S}$, which is just in the shape we want to achieve according to the above design strategy. If we design current sensing gain *Ri* equal to the specified load-line resistance R_{LL}, the close output impedance will be equal to R_{LL} within *T2* bandwidth.

Therefore, the compensator design becomes simple. Typically we can design

$$Av(s) = K \cdot \frac{1 + \frac{s}{\omega o}}{s \cdot (1 + \frac{s}{\omega p})}$$

An integrator is used to eliminate the steady state error. A zero is put to compensate the system double pole. A pole in the high frequency range can be used to further attenuate the switching noise, but it can be omitted to simplify the circuitry.

Based on the above discussion, by proper but not critical compensator design, within the control bandwidth, the converter with active droop control shown in Fig. 3-21 is equivalent to a voltage source *Vref* in series with a resistor *Ri*.

3.4.1.2. Build a Well-Controlled Load Line to Multi-Channels

If there are many channels and we do active droop control for each channel, as shown in Fig. 3-21, we can get the same equivalent circuit. Even the power stages between each channel have huge variation. If we design *Vref* and *Ri* the same, they would have the same equivalent circuits within the control bandwidth. As shown in Fig. 3-27, if all the channels share the same input and output, their equivalent circuits would be connected together.

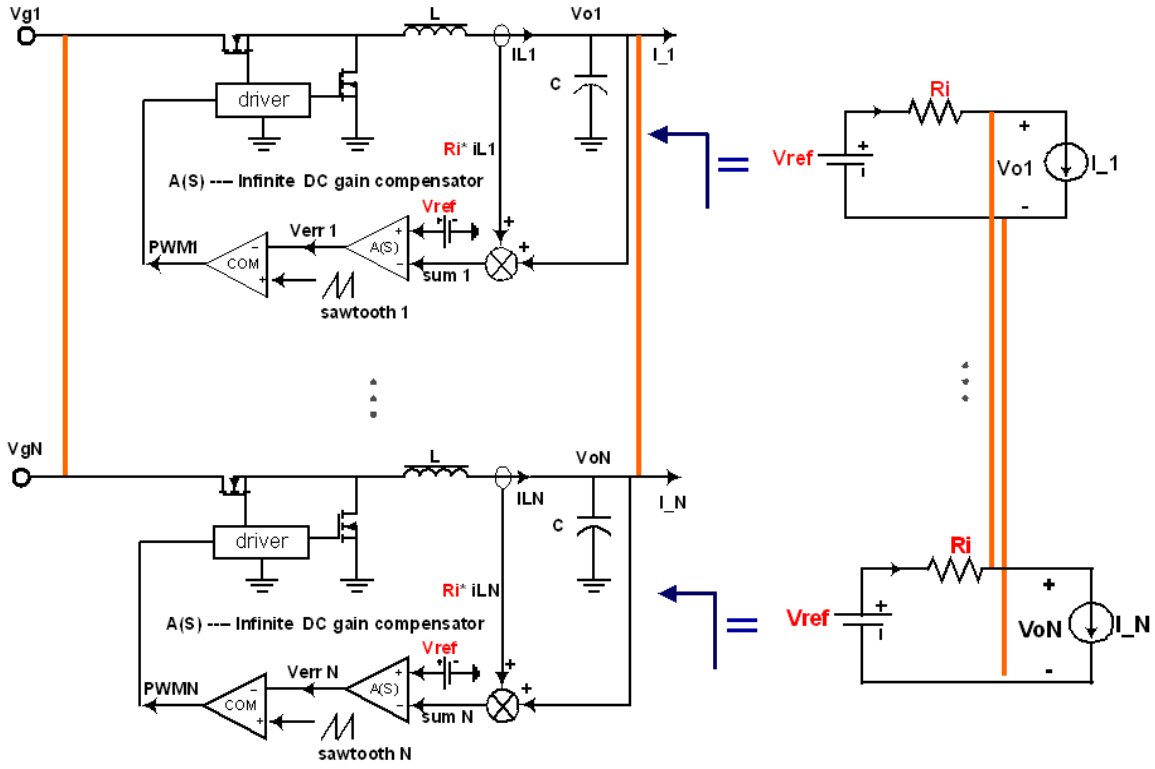


Fig. 3-27. Multi-channel active droop control.

Fig. 3-27 can be redrawn as Fig. 3-28. The overall equivalent circuit can be further simplified as a voltage source in series with a resistor. The value of the voltage source is *Vref*, and the value of the resistance is *Ri/N*. By this way, a well-controlled system load line is achieved. And this scheme can be fully distributed according to Fig. 1-13 to achieve scalable phase design.

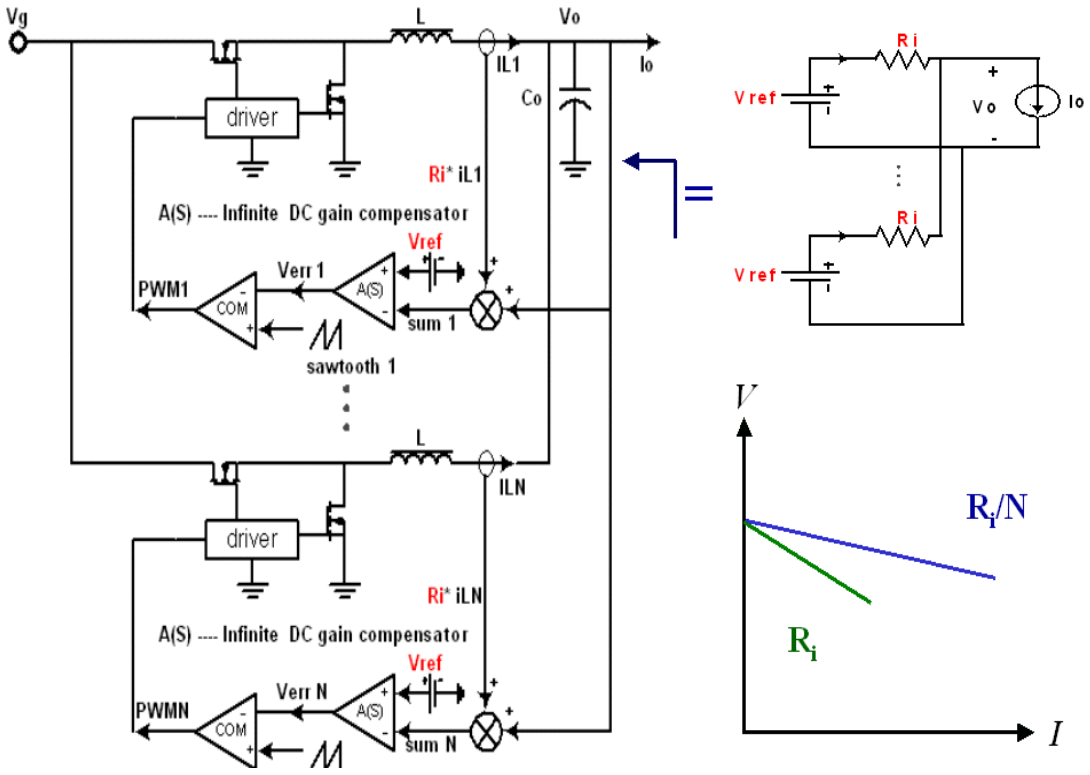


Fig. 3-28. Redrawn Multi-channel active droop control.

The key of this scheme is to build a well-controlled load line for each channel to realize a well-controlled system load line. If we need design a VR with ideal 0 load, output voltage=1V and R_{LL}=1mΩ, we just need to design *Vref=1V*, and each channel's current sensing gain = N mΩ if we have N channels.

Although each channel's Vref and sensing gain can be well controlled, in reality they still have some tolerance so that the load line of the whole system have a tolerance band (TOB). As we have already seen in section 3.1 that the TOB specifications for AVP is very strict. Tolerance analysis is needed to verify the ability of this control scheme to meet the specifications of today or even future's CPU voltage regulation window. Section 3.5 will provide the tolerance analysis.

3.4.2. Distributed Current Sharing Scheme Development

Now, we have already had a control scheme for AVP. According to [C30]~[C32], this kind of active droop scheme has the current sharing function. The reason is simple: if the load line of each channel is exactly the same, the current going through each channel should be the same because the outputs are tie together.

However, as shown in Fig. 3-29, if there are tolerances of each channel's *Vref* and *Ri*, the current in each channel will be different.

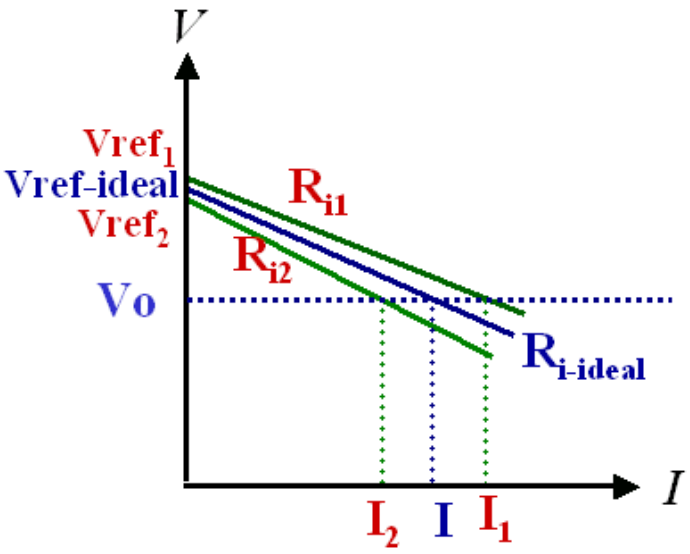


Fig. 3-29. Current sharing with droop control.

And for the case of VR, the total AVP droop is just about 10% of the normal output voltage; the impact of *Vref* tolerance is dominant. Fig. 3-30 shows the relation of current sharing and load current with different Vref tolerances assuming each channel's *Ri* is exactly the same. In Fig. 3-30, *Kvid* is the tolerance of each channel's voltage reference. The current sharing index is defined as $CS = \frac{Max\Delta I}{I}$, where ΔI is inductor current

difference between two channels, and *I* is the average value of all the channels' inductor current.

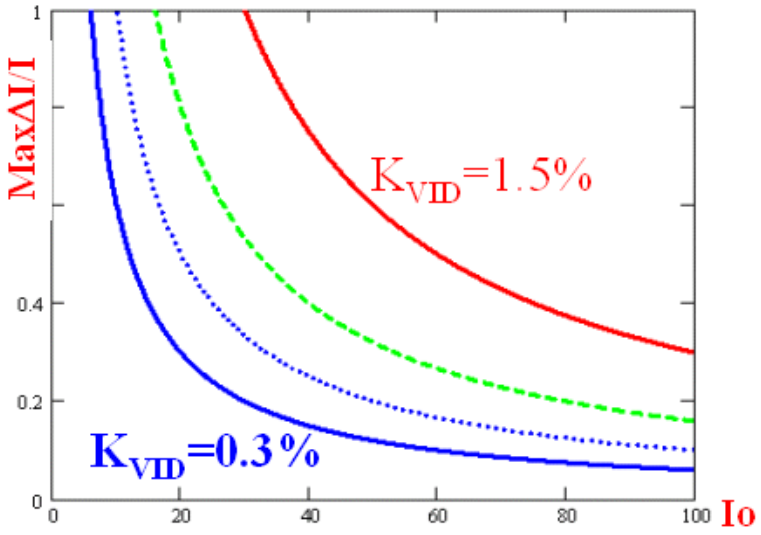


Fig. 3-30. Impact of Vref tolerance on the current sharing.

As we can see from Fig. 3-30, the current sharing becomes worse at light load and becomes better if *Vref* tolerance is smaller. Before the year 2001, VR controllers often use 1.5%, or 1% *Vref*, and the current sharing at half load is only 50% using the scheme of Fig. 3-28. Therefore people don't think the current sharing by this droop mode is a practical way to share current between two VRMs. However, today's VR controllers all use 0.5% voltage reference, and 0.35% is also easily achievable.

And we can do better. If we tie each channel's *Vref* together, we can completely bypass the impact of *Vref* tolerance on current sharing. And the current sharing will not change with load. It only depends on how well each channel's current sensing gain can be controlled. Fig. 3-31 shows the scheme with each channel's Vref tied together. Fig. 3-32 explains the improvement of current sharing. Fig. 3-33 shows the impact of current sensing gain tolerance on current sharing. Compared to the scheme in Fig. 3-28, the configuration in Fig. 3-31 will sacrifice AVP performance, and it has better current

sharing performance. More importantly, it can still be fully distributed according to Fig. 1-13 to achieve scalable phase design.

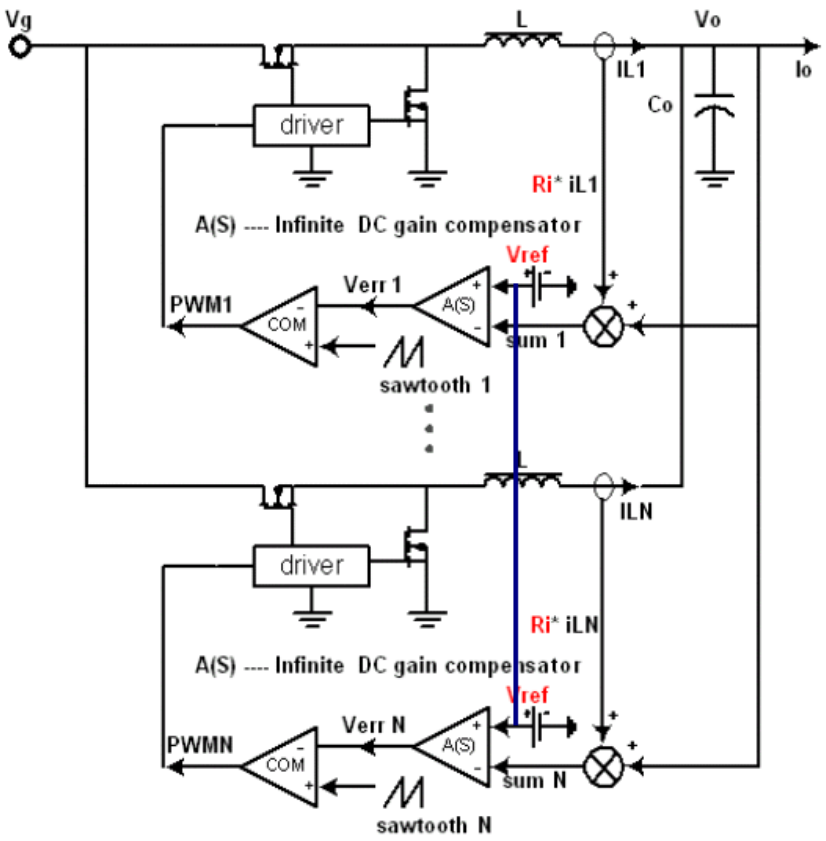


Fig. 3-31. Tie each channel's Vref together to achieve better current sharing.

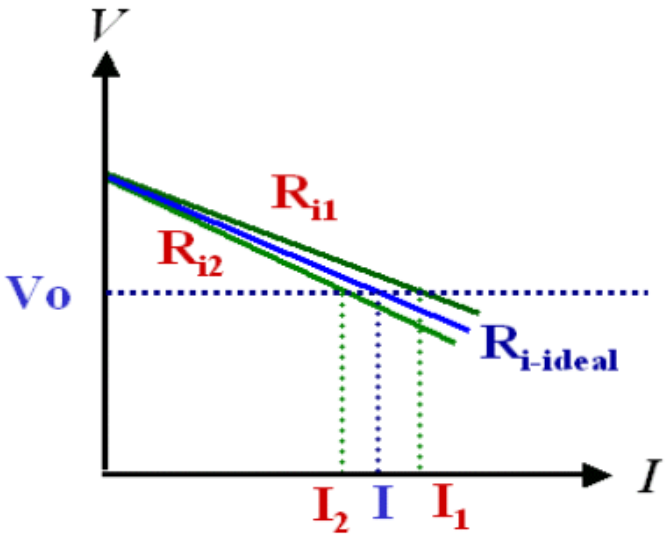


Fig. 3-32. Current sharing with scheme shown in Fig. 3-31.

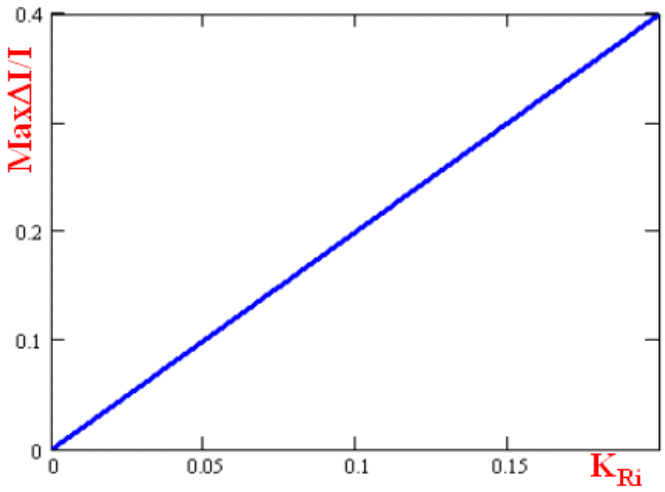


Fig. 3-33. Impact of current sensing gain tolerance on the current sharing.

Figures 3-32 and 3-33 just conceptually describe the impact of nonideal components on current sharing. In reality, the values of each channel's current sensing gain are not in a uniform distribution. Section 3.5 will provide more strict tolerance analysis.

3.4.3. Proposed MVRC Control Scheme

Until now, we have a scheme, as shown in Fig. 3-31, which can achieve AVP and current sharing, and can be fully distributed according to Fig. 1-13 to achieve scalable phase design. Combing Fig. 3-31 and Fig. 2-9 together, we have a fully distributed control scheme for scalable phase design with MVRC chips.

Fig. 3-34 shows the combined scheme. For AVP and current sharing, it uses droop in each channel with voltage references tied together. For interleaving, it uses voltage controlled phase delay with self-adjusted saw-tooth generators. It can realize unlimited phase design and no master controller needed. It is my proposed MVRC solution for CPU power management.

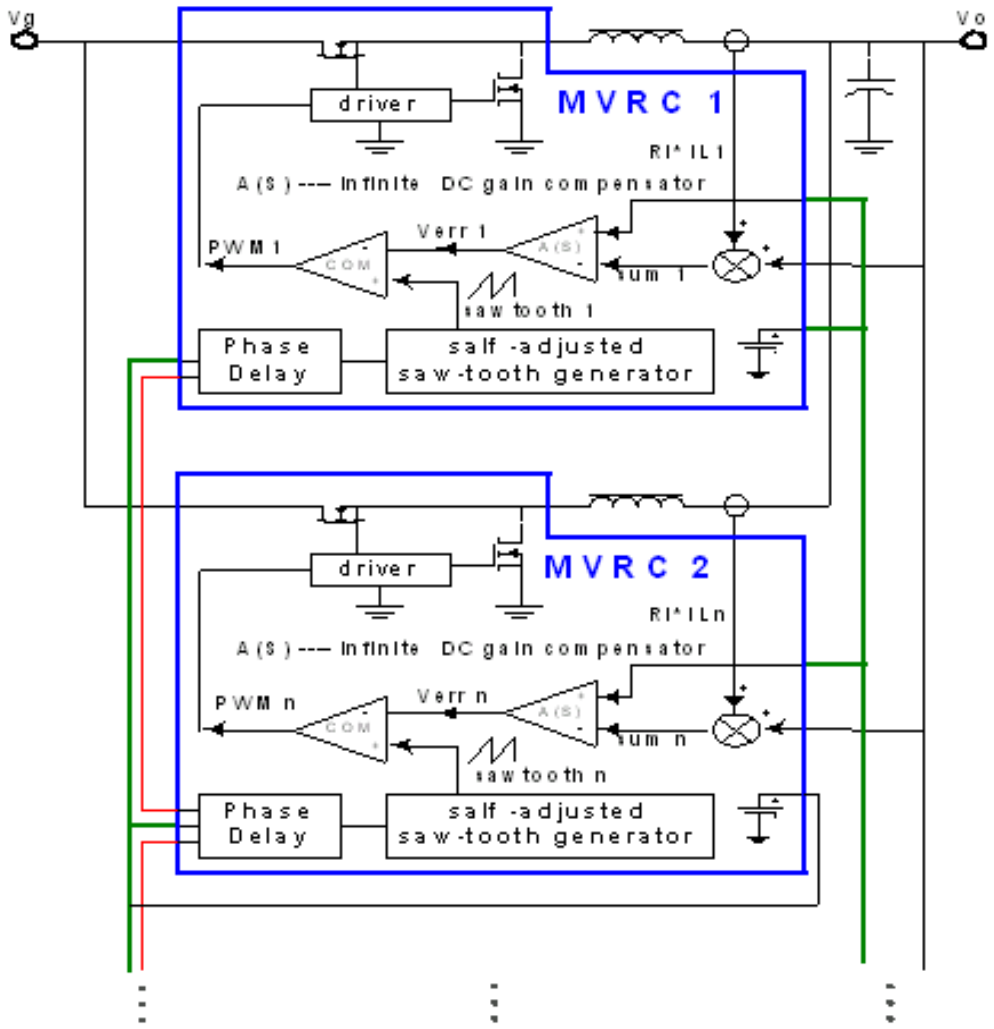


Fig. 3-34. Proposed MVRC solution for CPU power management.

3.4.4. Simulation Results

A lot of visional designs with the scheme in Fig. 3-34 are simulated to verify the distributed control. Fig. 3-35 shows the transient simulation results with a 4-phase design. The input voltage is 12V. The switching frequency is 1MHz. The specified VR load-line resistance is 1.5mΩ. Voltage reference is 1.5V. The inductor in each channel is about 200nH with 0.4mΩ DCR. The total output capacitor is 2000uF with 1mΩ ESR. The Rdson of power device is 5~8mΩ and unevenly distributed. The output current changes

from 0A to 100A at t =100us, and changes from 100A to 0A at 160us.The di/dt=100A/us at both loading step and unloading step. As shown in Fig. 3-35, the proposed control has good interleaving, AVP, current sharing performance. More tolerance simulation results will be provided in section 3.6.

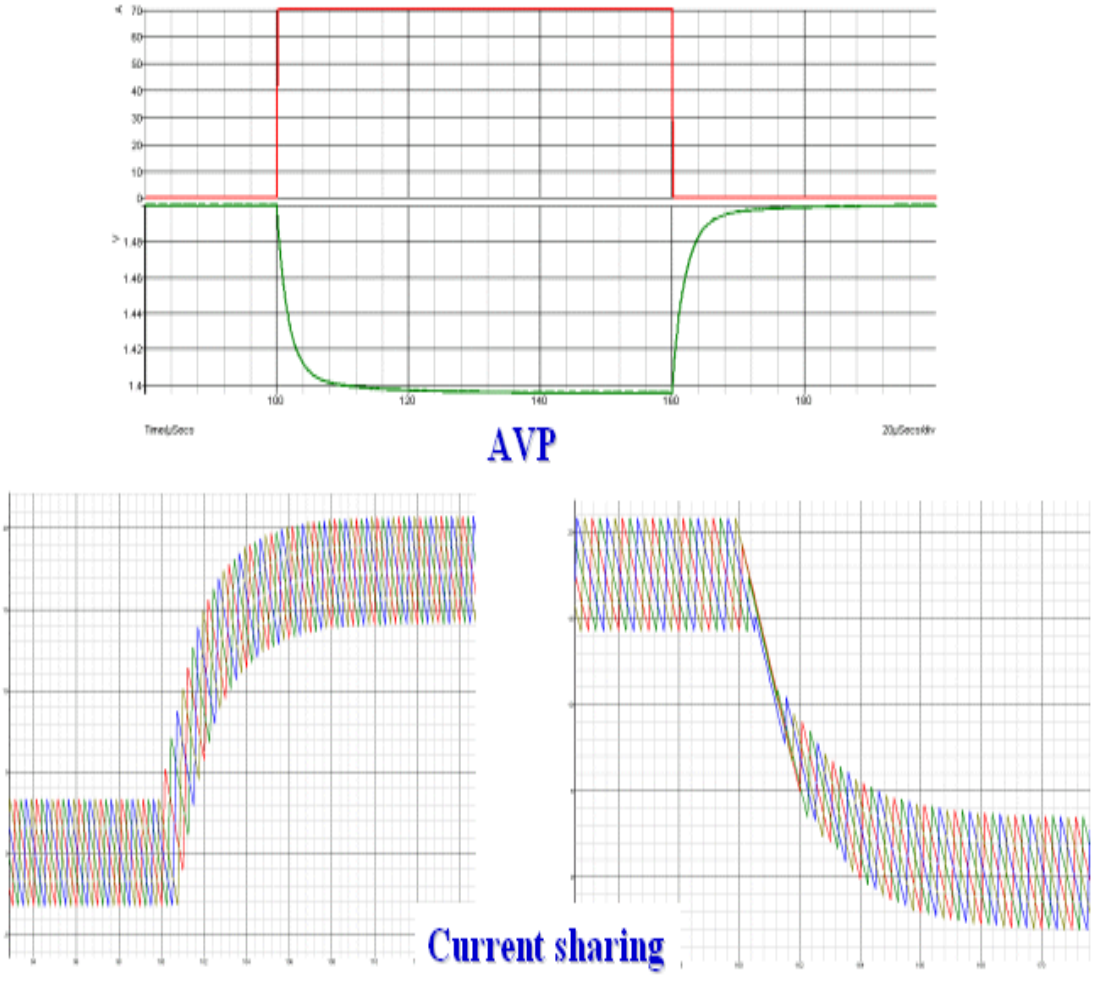


Fig. 3-35. Transient simulation results.

3.5. AVP and Current Sharing Tolerance Analysis

3.5.1. Tolerance Analysis Approaches [C33]

As mentioned in the above sections, tolerance analysis is necessary to verify the proposed AVP and current sharing schemes. To do the analysis, we need to know the procedure first. Basically, there are three popular ways to do mathematic tolerance analysis: 1) worst case analysis; 2) standard error analysis; 3) the combination of 1) and 2).

3.5.1.1. Worst Case Analysis

One appealing definition of how good a solution a hysteretic gets is to see how bad a hysteretic can possibly be. If we know that the hysteretic is never worst than, say, 1% above the optimal, we do not have to worry about which instances we have to solve.

Worst case analysis is to find the worst case impact due to the tolerance of parameters. It just uses each parameter's boundary values in the calculation and does not require the knowledge of parameter distribution. Due to the over simplification, the results of worst case analysis are usually too pessimistic. Quality control based on worst case analysis will lead to huge overdesign. However, because the worst case analysis is easy to implement and does not require the prior knowledge of parameter distribution, it is widely used in industry as a tool to roughly evaluate the design quality.

Fig. 3-36 shows the general steps to do worst case analysis. First, we need to do the modeling of the system so that the relationship of outputs and design parameters can be described by mathematic equations. Second, we need to identify stochastic variables and their *maximum tolerances*. Then, we derive the output function, whose tolerance is the objective of the study. Notice that **not** all the design parameters have big impacts on the

output function. Last, the maximum tolerance of the output function can be calculated using the general propagation equation for *maximum tolerance*.

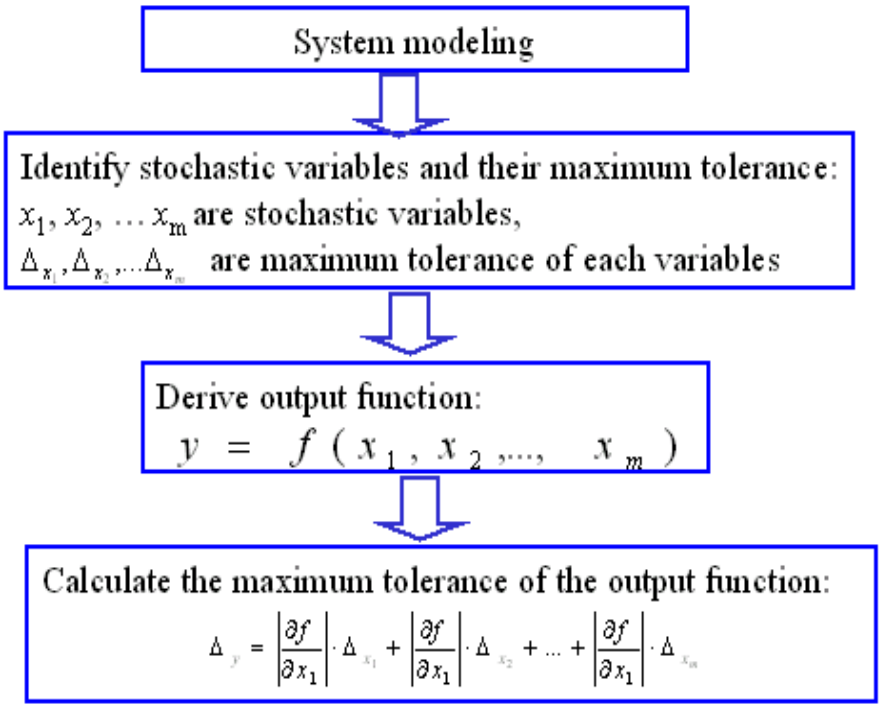


Fig. 3-36. General steps to do worst case analysis.

3.5.1.2. Standard Error Analysis

The calculation in the above worst case analysis is equivalent to that assuming each parameter of the system is in a uniform distribution. In manufacture, real values of most components are in Gussian distribution instead of uniform distribution. To analyze the impact of these stochastic variables, it is more accurate to calculate the overall manufacturing tolerance with standard error (mean-square deviation) instead of maximum error. Standard error analysis is a way to evaluate the design quality more accurately.

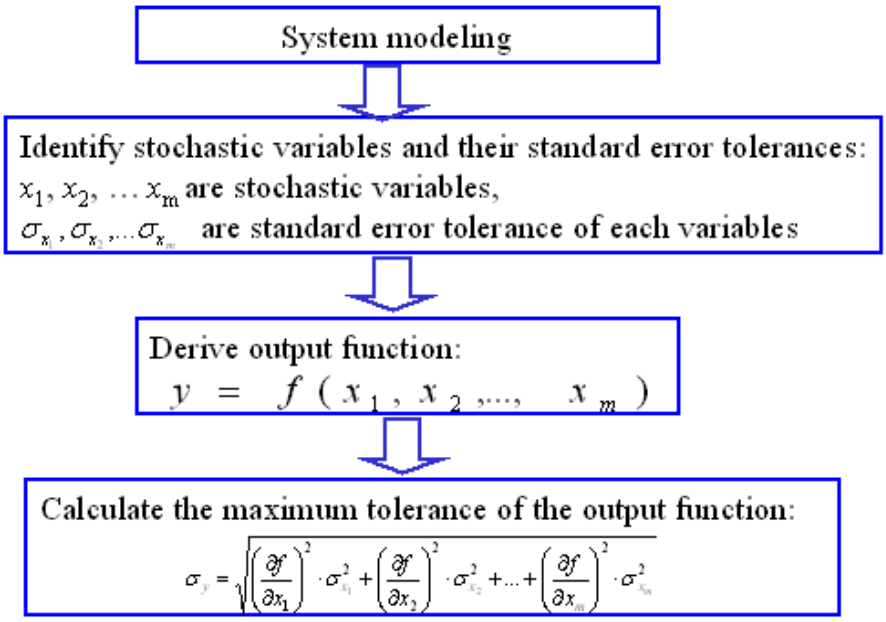


Fig. 3-37. General steps to do standard error analysis.

Fig. 3-37 shows general steps to do standard error analysis. First, we need to do the modeling of the system so that the relationship of outputs and design parameters can be described by mathematic equations. Second, we need to identify stochastic variables and their *standard error* tolerances. Then, we derive the output function, whose tolerance is the objective of the study. Notice that **not** all the design parameters have big impacts on the output function. Last, the tolerance of the output function can be calculated using the general propagation equation for *standard error* tolerance.

3.5.1.3. The Combination of Worst Case Analysis and Standard Error Tolerance

In reality, not all deign parameters are in Gussian distribution. And the distribution of some parameters is simply unknown. The combination of worst case analysis and standard error analysis is more practical to evaluate the design quality.

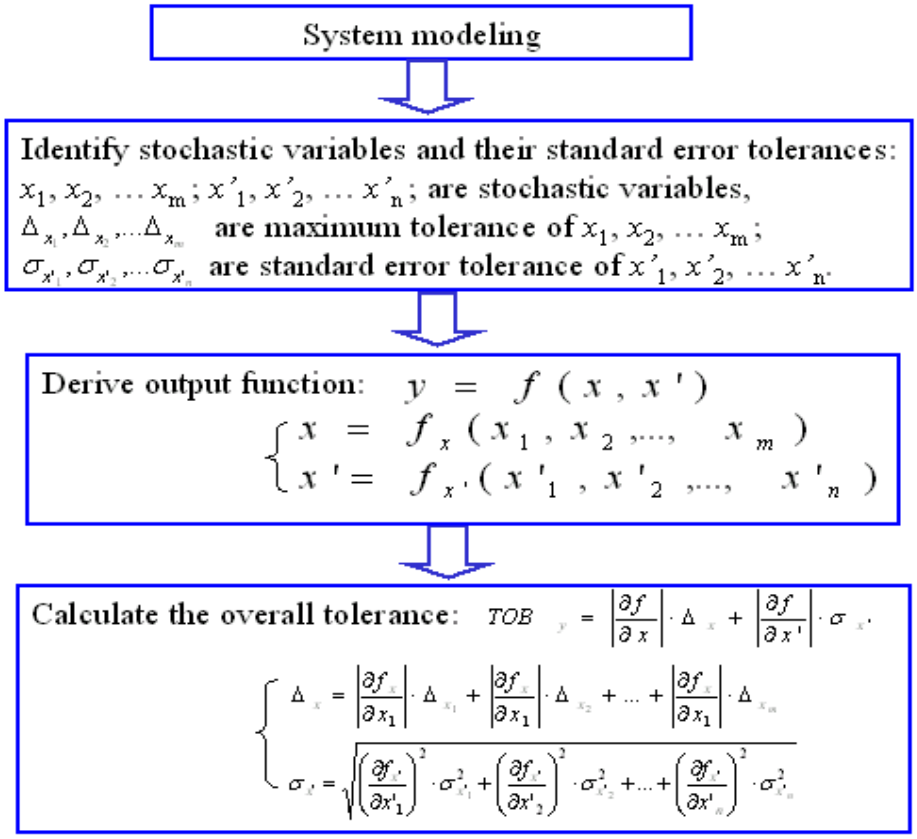


Fig. 3-38. Combination of worst case analysis and standard error analysis.

Fig. 3-38 shows such a procedure. First, we need to do the modeling of the system so that the relationship of outputs and design parameters can be described by mathematic equations. Second, we need to identify stochastic variables and their *maximum tolerances* or *standard error* tolerances. Then, we derive the output function, whose tolerance is the objective of the study. The function should be in a format $y = f(x, x')$. The function x contains and only contains stochastic variables, whose distribution are unknown or too complicated. The function x' contains and only contains stochastic variables in Gussian distribution. The overall tolerance of the output function y can be calculated using $TOB_y = \left|\frac{\partial f}{\partial x}\right| \cdot \Delta_x + \left|\frac{\partial f}{\partial x'}\right| \cdot \sigma_{x'}$, where Δ_x and $\sigma_{x'}$ are calculated using propagation equations for *maximum error* and *standard error* respectively.

3.5.2. AVP and Current Sharing Worst Case Analysis

3.5.2.1. AVP Worst Case Analysis

A. AVP with the traditional control scheme

In steady state, the traditional AVP scheme the adopting active droop control, as shown in Fig. 3-17, can be modeled with the signal flow diagram shown in Fig. 3-39.

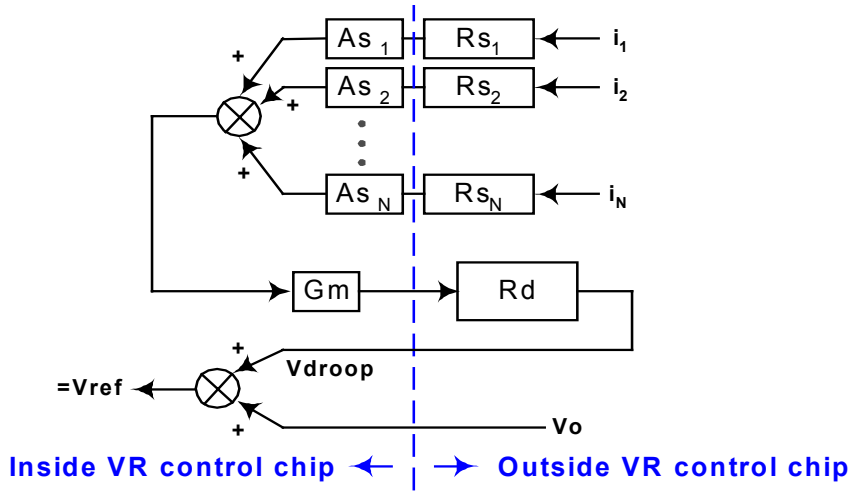


Fig. 3-39. Steady state model for the traditional AVP scheme.

In Fig. 3-39, *Vref* is the voltage reference inside the VR controller; *As1 ~ AsN* are the current scaling gain and *Rs1 ~ Rsn* are the effective sensing resistance of each channel's current sensing element. *Gm* is the transconduance gain. *Rd* is the droop resistor outside the VR controller, and *N* is channel number.

From Fig. 3-39, it is easy to get the output function:

$$Vo = Vref - Vdroop = Vref - Gm \cdot Rd \cdot \sum_{i=1}^{N} \left(Rs_i \cdot As_i \cdot i_i \right)$$

Since the current sharing function (not shown in Fig. 3-39) forces

$Rs_1 \cdot As_1 \cdot i_1 = Rs_2 \cdot As_2 \cdot i_2 = \ldots = Rs_N \cdot As_N \cdot i_N$, we have:

$\sum_{i=1}^{N} \left(Rs_i \cdot As_i \cdot i_i \right) = Rs_1 \cdot As_1 \cdot N \cdot i_1 = Rs_2 \cdot As_2 \cdot N \cdot i_2 = \ldots. = Rs_N \cdot As_N \cdot N \cdot i_N$. Therefore,

$$\begin{cases} Vo = Vref - Gm \cdot Rd \cdot Rs_1 \cdot As_1 \cdot N \cdot i_1 \Rightarrow i_1 = \dfrac{Vref - Vo}{Gm \cdot Rd \cdot Rs_1 \cdot As_1 \cdot N}, \\ Vo = Vref - Gm \cdot Rd \cdot Rs_2 \cdot As_2 \cdot N \cdot i_2 \Rightarrow i_2 = \dfrac{Vref - Vo}{Gm \cdot Rd \cdot Rs_2 \cdot As_2 \cdot N}, \\ \cdots \\ Vo = Vref - Gm \cdot Rd \cdot Rs_N \cdot As_N \cdot N \cdot i_N \Rightarrow i_N = \dfrac{Vref - Vo}{Gm \cdot Rd \cdot Rs_N \cdot As_N \cdot N} \end{cases}$$

$$i_1 + i_2 + \ldots + i_N = \frac{Vref - Vo}{Gm \cdot Rd \cdot N} \cdot \left(\frac{1}{Rs_1 \cdot As_1} + \frac{1}{Rs_2 \cdot As_2} + \ldots + \frac{1}{Rs_N \cdot As_N} \right) = Io$$

$$\Rightarrow \quad Vo = Vref - \frac{Gm \cdot Rd \cdot N \cdot Io}{\left(\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + \ldots + \dfrac{1}{Rs_N \cdot As_N} \right)} \qquad \textbf{(3-1)}$$

The partial derivatives of (3-1) are the following:

$$\frac{\partial Vo}{\partial Vref} = 1$$

$$\frac{\partial Vo}{\partial Gm} = \frac{-Rd \cdot N \cdot Io}{\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + \ldots + \dfrac{1}{Rs_N \cdot As_N}}$$

$$\frac{\partial Vo}{\partial Rd} = \frac{-Gm \cdot N \cdot Io}{\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + \ldots + \dfrac{1}{Rs_N \cdot As_N}}$$

$$\begin{cases} \dfrac{\partial Vo}{\partial Rs_1} = \dfrac{-Gm \cdot Rd \cdot N \cdot Io}{\left(\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + \ldots + \dfrac{1}{Rs_N \cdot As_N} \right)^2} \cdot \dfrac{1}{Rs_1^2 \cdot As_1} \\ \cdots \\ \dfrac{\partial Vo}{\partial Rs_N} = \dfrac{-Gm \cdot Rd \cdot N \cdot Io}{\left(\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + \ldots + \dfrac{1}{Rs_N \cdot As_N} \right)^2} \cdot \dfrac{1}{Rs_N^2 \cdot As_N} \end{cases}$$

$$\begin{cases} \dfrac{\partial Vo}{\partial As_1} = \dfrac{-Gm \cdot Rd \cdot N \cdot Io}{\left(\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + ... + \dfrac{1}{Rs_N \cdot As_N}\right)^2} \cdot \dfrac{1}{Rs_1 \cdot As_1^2} \\ \cdots \\ \dfrac{\partial Vo}{\partial As_N} = \dfrac{-Gm \cdot Rd \cdot N \cdot Io}{\left(\dfrac{1}{Rs_1 \cdot As_1} + \dfrac{1}{Rs_2 \cdot As_2} + ... + \dfrac{1}{Rs_N \cdot As_N}\right)^2} \cdot \dfrac{1}{Rs_1 \cdot As_N^2} \end{cases}$$

In most of the cases, we use the same specified values to design each channel's current sensing element ($Rs_1, Rs_2, ..., Rs_N$) and scaling gain. We have:

$$As_1\_ideal = As_2\_ideal = ... = As_N\_ideal = AS$$

$$Rs_1\_ideal = Rs_2\_ideal = ... = Rs_N\_ideal = RS$$

Defining $Gm\_ideal = GM$, $Rd\_ideal = RD$, $Vref\_ideal = VR$, and R_{LL} as the specified target load-line resistance of the system, then we have $R_{LL} = \dfrac{Vdroop}{Io} = AS \cdot RS \cdot GM \cdot RD$, and around the design point *Po*, we have:

$$\left|\frac{\partial Vo}{\partial Vref}\right|_{Po} = 1 \qquad \left|\frac{\partial Vo}{\partial Gm}\right|_{Po} = \frac{RD \cdot N \cdot Io}{\dfrac{N}{RS \cdot AS}} = RD \cdot RS \cdot AS \cdot Io = \frac{R_{LL}}{GM} \cdot Io$$

$$\left|\frac{\partial Vo}{\partial Rd}\right|_{Po} = \frac{GM \cdot N \cdot Io}{\dfrac{N}{RS \cdot AS}} = GM \cdot RS \cdot AS \cdot Io = \frac{R_{LL}}{RD} \cdot Io$$

$$\left|\frac{\partial Vo}{\partial Rs_1}\right|_{Po} = \left|\frac{\partial Vo}{\partial Rs_2}\right|_{Po} = ... = \left|\frac{\partial Vo}{\partial Rs_N}\right|_{Po}$$
$$= \frac{GM \cdot RD \cdot N \cdot Io}{\left(\dfrac{N}{RS \cdot AS}\right)^2} \cdot \frac{1}{RS^2 \cdot AS} = \frac{GM \cdot RD \cdot AS \cdot Io}{N} = \frac{1}{N} \cdot \frac{R_{LL}}{RS} \cdot Io$$

$$\left|\frac{\partial Vo}{\partial As_1}\right|_{Po} = \left|\frac{\partial Vo}{\partial As_2}\right|_{Po} = \ldots = \left|\frac{\partial Vo}{\partial As_N}\right|_{Po}$$

$$= \frac{GM \cdot RD \cdot N \cdot Io}{\left(\frac{N}{RS \cdot AS}\right)^2} \cdot \frac{1}{RS \cdot AS^2} = \frac{GM \cdot RD \cdot RS \cdot Io}{N} = \frac{1}{N} \cdot \frac{R_{LL}}{AS} \cdot Io$$

$$\Delta Vo = \left|\frac{\partial Vo}{\partial Vref}\right|_{Po} \cdot \Delta Vref + \left|\frac{\partial Vo}{\partial Gm}\right|_{Po} \cdot \Delta Gm + \left|\frac{\partial Vo}{\partial Rd}\right|_{Po} \cdot \Delta Rd$$

$$+ \left|\frac{\partial Vo}{\partial Rs_1}\right|_{Po} \cdot \Delta Rs_1 + \left|\frac{\partial Vo}{\partial As_1}\right|_{Po} \cdot \Delta As_1 + \ldots + \left|\frac{\partial Vo}{\partial Rs_N}\right|_{Po} \cdot \Delta Rs_N + \left|\frac{\partial Vo}{\partial As_N}\right|_{Po} \cdot \Delta As_N$$

$$= \Delta Vref + R_{LL} \cdot Io \cdot \left(\frac{\Delta Gm}{GM} + \frac{\Delta Rd}{RD} + \frac{\Delta Rs_1}{N \cdot RS} + \frac{\Delta As_1}{N \cdot AS} + \ldots + \frac{\Delta Rs_N}{N \cdot RS} + \frac{\Delta As_N}{N \cdot AS}\right)$$

Using the same maximum tolerance value for each channel's current sensing element, and for each channel's current scaling amplifier, we have:

$\Delta As_1 = \Delta As_2 = \ldots = \Delta As_N = \Delta As$, $\Delta Rs_1 = \Delta Rs_2 = \ldots = \Delta Rs_N = \Delta Rs$.

Then:

$$\Delta Vo = \Delta Vref + R_{LL} \cdot Io \cdot \left(\frac{\Delta Gm}{GM} + \frac{\Delta Rd}{RD} + \frac{\Delta Rs}{RS} + \frac{\Delta As}{AS}\right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining: $\varepsilon_{Gm} = \frac{\Delta Gm}{GM}, \varepsilon_{Rd} = \frac{\Delta Rd}{RD}, \varepsilon_{As} = \frac{\Delta As}{AS}, \varepsilon_{Rs} = \frac{\Delta Rs}{RS}, \varepsilon_{Vr} = \frac{\Delta Vref}{VR}$, then we have:

$$\Delta Vo = VR \cdot \varepsilon_{Vr} + R_{LL} \cdot Io \cdot \left(\varepsilon_{Gm} + \varepsilon_{Rd} + \varepsilon_{As} + \varepsilon_{Rs}\right) \qquad \textbf{(3-2)}$$

E.g., if $VR=1$, $Io = 100$, $\varepsilon_{Gm} = 1\%, \varepsilon_{Rd} = 1\%, \varepsilon_{As} = 1\%, \varepsilon_{Rs} = 5\%, \varepsilon_{Vr} = 0.5\%$,

$$\Delta Vo = 1 \cdot 0.5\% + 0.001 \cdot 100 \cdot (1\% + 1\% + 1\% + 5\%) = 0.005 + 0.1 \cdot 0.08 = 13(mV)$$

B. AVP with the proposed control scheme

In steady state, the proposed AVP scheme adopting the active droop control, as shown in Fig. 3-31, can be modeled with the signal flow diagram shown in Fig. 3-40.

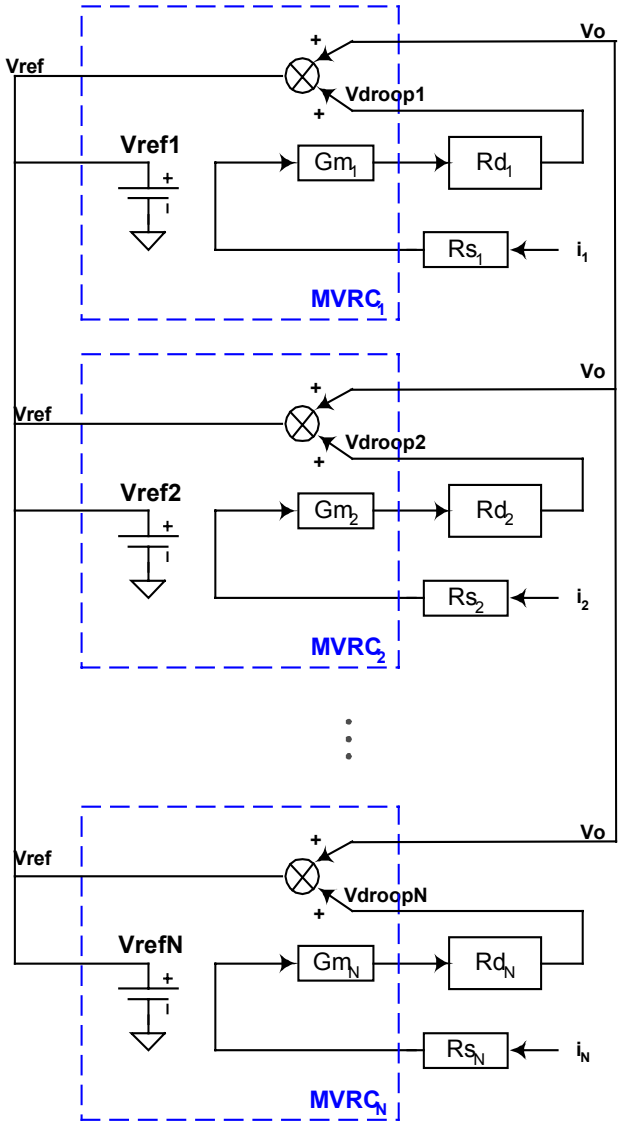


Fig. 3-40. Steady state model for proposed AVP scheme.

In Fig. 3-40, $Vref_1$~$Vreg_N$ are the voltage reference inside each MVRC chip; *Rs1~Rsn* are the effective sensing resistance of each channel's current sensing element. *Gm1~Gmn* are the transconduance gain in each MVRC chip, and *Rd1~Rdn* are each channel's droop resistor outside the MVRC chip.

It is easy to get the voltage of *Vref* in the above figure:

$$Vref = \frac{Vref_1 + Vref_2 + ... + Vref_N}{N}$$

$$\begin{cases} Vref = Vo + Vdroop1 = Vo + i_1 \cdot Rs_1 \cdot Gm_1 \cdot Rd_1 \Rightarrow i_1 = \dfrac{Vref - Vo}{Rs_1 \cdot Gm_1 \cdot Rd_1} \\ Vref = Vo + Vdroop2 = Vo + i_2 \cdot Rs_2 \cdot Gm_2 \cdot Rd_2 \Rightarrow i_2 = \dfrac{Vref - Vo}{Rs_2 \cdot Gm_2 \cdot Rd_2} \\ \cdots \\ Vref = Vo + VdroopN = Vo + i_N \cdot Rs_N \cdot Gm_N \cdot Rd_N \Rightarrow i_N = \dfrac{Vref - Vo}{Rs_N \cdot Gm_N \cdot Rd_N} \end{cases}$$

$$\begin{aligned} Io = i_1 + i_2 + ... + i_N &= \frac{Vref - Vo}{Rs_1 \cdot Gm_1 \cdot Rd_1} + \frac{Vref - Vo}{Rs_2 \cdot Gm_2 \cdot Rd_2} + ... + \frac{Vref - Vo}{Rs_N \cdot Gm_N \cdot Rd_N} \\ &= (Vref - Vo) \cdot \left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n} \right) \end{aligned}$$

$$\Rightarrow \quad Vo = Vref - \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}} \quad \textbf{(3-3)}$$

The partial derivatives of (3-3) are the following:

$$\frac{\partial Vo}{\partial Vref} = 1$$

$$\begin{cases} \dfrac{\partial Vo}{\partial Rs_1} = \dfrac{-1}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n} \right)^2} \cdot \frac{1}{Rs_1^2} \cdot \frac{1}{Gm_1} \cdot \frac{1}{Rd_1} \cdot Io \\ \cdots \\ \dfrac{\partial Vo}{\partial Rs_N} = \dfrac{-1}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n} \right)^2} \cdot \frac{1}{Rs_N^2} \cdot \frac{1}{Gm_N} \cdot \frac{1}{Rd_N} \cdot Io \end{cases}$$

$$\begin{cases} \dfrac{\partial Vo}{\partial Gm_1} = \dfrac{-1}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \cdot \dfrac{1}{Rs_1} \cdot \dfrac{1}{Gm_1^2} \cdot \dfrac{1}{Rd_1} \cdot Io \\ \cdots \\ \dfrac{\partial Vo}{\partial Gm_N} = \dfrac{-1}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \cdot \dfrac{1}{Rs_N} \cdot \dfrac{1}{Gm_N^2} \cdot \dfrac{1}{Rd_N} \cdot Io \end{cases}$$

$$\begin{cases} \dfrac{\partial Vo}{\partial Rd_1} = \dfrac{-1}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \cdot \dfrac{1}{Rs_1} \cdot \dfrac{1}{Gm_1} \cdot \dfrac{1}{Rd_1^2} \cdot Io \\ \cdots \\ \dfrac{\partial Vo}{\partial Rd_N} = \dfrac{-1}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \cdot \dfrac{1}{Rs_N} \cdot \dfrac{1}{Gm_N} \cdot \dfrac{1}{Rd_N^2} \cdot Io \end{cases}$$

In most of the cases, we use the same specified value to design each channel's current sensing element ($Rs_1, Rs_2, ..., Rs_N$), droop resistor ($Rd_1, Rd_2, ..., Rd_N$), and transconductance amplifier ($Gm_1, Gm_2, ..., Gm_N$). We have:

$$Rs_1\_ideal = Rs_2\_ideal = ... = Rs_N\_ideal = RS$$

$$Rd_1\_ideal = Rd_2\_ideal = ... = Rd_N\_ideal = RD$$

$$Gm_1\_ideal = Gm_2\_ideal = ... = Gm_N\_ideal = GM$$

Defining R_{LL} as the specified target load line resistance of the system, based on the working principle described in section 3.4.1, we have $R_{LL} = \dfrac{Vdroop}{Io} = \dfrac{RS \cdot GM \cdot RD}{N}$.

Around the design point *Po*, we have:

$$\left|\frac{\partial Vo}{\partial Vref}\right|_{Po}=1$$

$$\left|\frac{\partial Vo}{\partial Rs_1}\right|_{Po}=\left|\frac{\partial Vo}{\partial Rs_2}\right|_{Po}=...=\left|\frac{\partial Vo}{\partial Rs_N}\right|_{Po}$$
$$=\frac{1}{\left(\frac{N}{RS\cdot GM\cdot RD}\right)^2}\cdot\frac{1}{RS^2}\cdot\frac{1}{GM}\cdot\frac{1}{RD}\cdot Io=\frac{GM\cdot RD}{N^2}\cdot Io=\frac{1}{N}\cdot\frac{R_{LL}}{RS}\cdot Io$$

$$\left|\frac{\partial Vo}{\partial Gm_1}\right|_{Po}=\left|\frac{\partial Vo}{\partial Gm_2}\right|_{Po}=...=\left|\frac{\partial Vo}{\partial Gm_N}\right|_{Po}$$
$$=\frac{1}{\left(\frac{N}{RS\cdot GM\cdot RD}\right)^2}\cdot\frac{1}{RS}\cdot\frac{1}{GM^2}\cdot\frac{1}{RD}\cdot Io=\frac{RS\cdot RD}{N^2}\cdot Io=\frac{1}{N}\cdot\frac{R_{LL}}{GM}\cdot Io$$

$$\left|\frac{\partial Vo}{\partial Rd_1}\right|_{Po}=\left|\frac{\partial Vo}{\partial Rd_2}\right|_{Po}=...=\left|\frac{\partial Vo}{\partial Rd_N}\right|_{Po}$$
$$=\frac{1}{\left(\frac{N}{RS\cdot GM\cdot RD}\right)^2}\cdot\frac{1}{RS}\cdot\frac{1}{GM}\cdot\frac{1}{RD^2}\cdot Io=\frac{RS\cdot GM}{N^2}\cdot Io=\frac{1}{N}\cdot\frac{R_{LL}}{RD}\cdot Io$$

$$\Delta Vo=\left|\frac{\partial Vo}{\partial Vref}\right|_{Po}\cdot\Delta Vref+\left|\frac{\partial Vo}{\partial Rs_1}\right|_{Po}\cdot\Delta Rs_1+\left|\frac{\partial Vo}{\partial Gm_1}\right|_{Po}\cdot\Delta Gm_1+\left|\frac{\partial Vo}{\partial Rd_1}\right|_{Po}\cdot\Delta Rd_1$$
$$+....\left|\frac{\partial Vo}{\partial Rs_N}\right|_{Po}\cdot\Delta Rs_N+\left|\frac{\partial Vo}{\partial Gm_N}\right|_{Po}\cdot\Delta Gm_N+\left|\frac{\partial Vo}{\partial Rd_N}\right|_{Po}\cdot\Delta Rd_N$$
$$=\Delta Vref+R_{LL}\cdot Io\cdot\left(\frac{\Delta Rs_1}{N\cdot RS}+\frac{\Delta Gm_1}{N\cdot GM}+\frac{\Delta Rd_1}{N\cdot RD}+...+\frac{\Delta Rs_N}{N\cdot RS}+\frac{\Delta Gm_N}{N\cdot GM}+\frac{\Delta Rd_N}{N\cdot RD}\right)$$

Using the same maximum tolerance value for each channel's current sensing element, droop resistor, and transconduance amplifier, we have: $\Delta Rs_1=\Delta Rs_2=...=\Delta Rs_N=\Delta Rs$, $\Delta Gm_1=\Delta Gm_2=...=\Delta Gm_N=\Delta Gm$, and $\Delta Rd_1=\Delta Rd_2=...=\Delta Rd_N=\Delta Rd$. Then, we have:

$$\Delta Vo=\Delta Vref+R_{LL}\cdot Io\cdot\left(\frac{\Delta Rs}{RS}+\frac{\Delta Gm}{GM}+\frac{\Delta Rd}{RD}\right),$$

where $Vref = \frac{Vref_1 + Vref_2 + ... + Vref_N}{N}$,

$$\Delta Vref = \left|\frac{\partial Vo}{\partial Vref_1}\right|_{Po} \cdot \Delta Vref_1 + \left|\frac{\partial Vo}{\partial Vref_2}\right|_{Po} \cdot \Delta Vref_2 + ... + \left|\frac{\partial Vo}{\partial Vref_N}\right|_{Po} \cdot \Delta Vref_N$$
$$= \frac{1}{N} \cdot \Delta Vref_1 + \frac{1}{N} \cdot \Delta Vref_2 + ... + \frac{1}{N} \cdot \Delta Vref_N$$

Using the same maximum tolerance value for each channel's voltage reference, we have: $\Delta Vref_1 = \Delta Vref_2 = ... = \Delta Vref_N = \Delta Vr$, and then $\Delta Vref = \Delta Vr$

$$\Delta Vo = \Delta Vr + R_{LL} \cdot Io \cdot \left(\frac{\Delta Rs}{RS} + \frac{\Delta Gm}{GM} + \frac{\Delta Rd}{RD}\right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining: $\varepsilon_{Gm} = \frac{\Delta Gm}{GM}, \varepsilon_{Rd} = \frac{\Delta Rd}{RD}, \varepsilon_{Rs} = \frac{\Delta Rs}{RS}$, $\varepsilon_{Vr} = \frac{\Delta Vr}{VR}$, we have:

$$\Delta Vo = VR \cdot \varepsilon_{Vr} + R_{LL} \cdot Io \cdot \left(\varepsilon_{Gm} + \varepsilon_{Rd} + \varepsilon_{Rs}\right) \quad \textbf{(3.4)}$$

For example, if $\varepsilon_{Gm} = 1\%, \varepsilon_{Rd} = 1\%, \varepsilon_{Rs} = 5\%, \varepsilon_{Vr} = 0.5\%, VR = 1$, $Io = 100$,

$$\Delta Vo = 1 \cdot 0.5\% + 0.001 \cdot 100 \cdot (1\% + 1\% + 5\%) = 0.005 + 0.1 \cdot 0.07 = 12(mV)$$

3.5.2.2. Current Sharing Worst Case Analysis

A. Current sharing with the traditional control scheme

The traditional current balance scheme, as shown in Fig. 3-19, forces $Rs_1 \cdot As_1 \cdot i_1 = Rs_2 \cdot As_2 \cdot i_2 = ... = Rs_N \cdot As_N \cdot i_N$ in steady state. From section 3.5.2.1, we have:

$$i_1 = \frac{Vref - Vo}{Gm \cdot Rd \cdot Rs_1 \cdot As_1 \cdot N} \text{ and } Vo = Vref - \frac{Gm \cdot Rd \cdot N \cdot Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}}$$

$$\Rightarrow i_1 = \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}} \cdot \frac{1}{Rs_1 \cdot As_1} \quad \textbf{(3.5)}$$

The partial derivatives of (3-5) are the following:

$$\frac{\partial i_1}{\partial Rs_1} = \frac{Io \cdot \frac{1}{Rs_1^2 \cdot As_1}}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1 \cdot As_1} - \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}} \cdot \frac{1}{Rs_1^2 \cdot As_1}$$

$$= \frac{Io}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1^2 \cdot As_1} \cdot \left(\frac{1}{Rs_1 \cdot As_1} - \sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right) = -\frac{\left(\frac{Io}{Rs_1^2 \cdot As_1}\right) \cdot \left(\sum_{n=2}^{N} \frac{1}{Rs_n \cdot As_n}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2}$$

$$\begin{cases} \frac{\partial i_1}{\partial Rs_2} = \frac{Io \cdot \frac{1}{Rs_2^2 \cdot As_2}}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1 \cdot As_1} = \frac{\left(\frac{Io}{Rs_2^2 \cdot As_2}\right) \cdot \left(\frac{1}{Rs_1 \cdot As_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \\ \cdots \\ \frac{\partial i_1}{\partial Rs_N} = \frac{Io \cdot \frac{1}{Rs_N^2 \cdot As_N}}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1 \cdot As_1} = \frac{\left(\frac{Io}{Rs_N^2 \cdot As_N}\right) \cdot \left(\frac{1}{Rs_1 \cdot As_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \end{cases}$$

$$\frac{\partial i_1}{\partial As_1} = \frac{Io \cdot \frac{1}{Rs_1 \cdot As_1^2}}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1 \cdot As_1} - \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}} \cdot \frac{1}{Rs_1 \cdot As_1^2}$$

$$= \frac{Io}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2} \cdot \frac{1}{Rs_1 \cdot As_1^2} \cdot \left(\frac{1}{Rs_1 \cdot As_1} - \sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right) = -\frac{\left(\frac{Io}{Rs_1 \cdot As_1^2}\right) \cdot \left(\sum_{n=2}^{N} \frac{1}{Rs_n \cdot As_n}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}\right)^2}$$

$$\begin{cases} \dfrac{\partial i_1}{\partial As_2} = \dfrac{Io \cdot \dfrac{1}{Rs_2 \cdot As_2^2}}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot As_n}\right)^2} \cdot \dfrac{1}{Rs_1 \cdot As_1} = \dfrac{\left(\dfrac{Io}{Rs_2 \cdot As_2^2}\right) \cdot \left(\dfrac{1}{Rs_1 \cdot As_1}\right)}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot As_n}\right)^2} \\ \cdots \\ \dfrac{\partial i_1}{\partial As_N} = \dfrac{Io \cdot \dfrac{1}{Rs_2 \cdot As_N^2}}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot As_n}\right)^2} \cdot \dfrac{1}{Rs_1 \cdot As_1} = \dfrac{\left(\dfrac{Io}{Rs_2 \cdot As_N^2}\right) \cdot \left(\dfrac{1}{Rs_1 \cdot As_1}\right)}{\left(\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot As_n}\right)^2} \end{cases}$$

Around the design point *Po*, we have:

$$\left|\frac{\partial i_1}{\partial Rs_1}\right|_{Po} = \frac{\left(\dfrac{Io}{RS^2 \cdot AS}\right) \cdot \left(\dfrac{N-1}{RS \cdot AS}\right)}{\left(\dfrac{N}{RS \cdot AS}\right)^2} = \frac{N-1}{N^2} \cdot \frac{Io}{RS}$$

$$\left|\frac{\partial i_1}{\partial Rs_2}\right|_{Po} = \left|\frac{\partial i_1}{\partial Rs_3}\right|_{Po} = \ldots = \left|\frac{\partial i_1}{\partial Rs_N}\right|_{Po} = \frac{Io \cdot \dfrac{1}{RS^2 \cdot AS}}{\left(\dfrac{N}{RS \cdot AS}\right)^2} \cdot \frac{1}{RS \cdot AS} = \frac{1}{N^2} \cdot \frac{Io}{RS}$$

$$\left|\frac{\partial i_1}{\partial As_1}\right|_{Po} = \frac{\left(\dfrac{N \cdot Io}{RS \cdot AS^2}\right) \cdot \left(\dfrac{N-1}{RS \cdot AS}\right)}{\left(\dfrac{N}{RS \cdot AS}\right)^2} = \frac{N-1}{N^2} \cdot \frac{Io}{AS}$$

$$\left|\frac{\partial i_1}{\partial As_2}\right|_{Po} = \left|\frac{\partial i_1}{\partial As_3}\right|_{Po} = \ldots = \left|\frac{\partial i_1}{\partial As_N}\right|_{Po} = \frac{Io \cdot \dfrac{1}{RS \cdot AS^2}}{\left(\dfrac{N}{RS \cdot AS}\right)^2} \cdot \frac{1}{RS \cdot AS} = \frac{1}{N^2} \cdot \frac{Io}{AS}$$

$$\begin{aligned} \Delta i_1 = & \left|\frac{\partial i_1}{\partial Rs_1}\right|_{p0} \cdot \Delta Rs_1 + \left|\frac{\partial i_1}{\partial Rs_2}\right|_{p0} \cdot \Delta Rs_2 + \ldots + \left|\frac{\partial i_1}{\partial Rs_N}\right|_{p0} \cdot \Delta Rs_N \\ & + \left|\frac{\partial i_1}{\partial As_1}\right|_{p0} \cdot \Delta As_1 + \left|\frac{\partial i_1}{\partial As_2}\right|_{p0} \cdot \Delta As_2 + \ldots + \left|\frac{\partial i_1}{\partial As_N}\right|_{p0} \cdot \Delta As_N \end{aligned}$$

$$\Delta i_1 = \frac{N-1}{N^2}\cdot\frac{Io}{RS}\cdot\Delta Rs_1 + \frac{1}{N^2}\cdot\frac{Io}{RS}\cdot\left(\Delta Rs_2 + ... + \Delta Rs_N\right)$$
$$+\frac{N-1}{N^2}\cdot\frac{Io}{AS}\cdot\Delta As_1 + \frac{1}{N^2}\cdot\frac{Io}{AS}\cdot\left(\Delta As_2 + ... + \Delta As_N\right)$$

Using the same maximum tolerance value for each channel's current sensing element, and for each channel's current scaling amplifier, we have: $\Delta Rs_1 = \Delta Rs_2 = ... = \Delta Rs_N = \Delta Rs$, $\Delta Asm_1 = \Delta As_2 = ... = \Delta As_N = \Delta As$, and then:

$$\Delta i_1 = \frac{N-1}{N^2}\cdot\frac{Io}{RS}\cdot\Delta Rs + \frac{1}{N^2}\cdot\frac{Io}{RS}\cdot\Delta Rs\cdot(N-1) + \frac{N-1}{N^2}\cdot\frac{Io}{AS}\cdot\Delta As + \frac{1}{N^2}\cdot\frac{Io}{AS}\cdot\Delta As\cdot(N-1)$$
$$= 2\cdot\left(\frac{N-1}{N^2}\right)\cdot Io\cdot\left(\frac{\Delta Rs}{RS} + \frac{\Delta As}{AS}\right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining: $\varepsilon_{Rs} = \frac{\Delta Rs}{RS}$, $\varepsilon_{As} = \frac{\Delta As}{AS}$, then we have:

$$\Delta i_1 = 2\cdot\frac{Io}{N}\cdot\left(\frac{N-1}{N}\right)\cdot\left(\varepsilon_{Rs} + \varepsilon_{As}\right)$$

If defining current sharing index as $CS = \frac{\Delta i_1}{Io/N}$, we have:

$$\text{CS} = 2\cdot\left(\frac{N-1}{N}\right)\cdot\left(\varepsilon_{Rs} + \varepsilon_{As}\right) \quad \textbf{(3.6)}$$

For example, if $\varepsilon_{Rs} = 5\%$, $\varepsilon_{As} = 1\%$, $N = 4$, $CS = 2\cdot\frac{3}{4}\cdot(5\% + 1\%) = 9\%$

B. Current sharing with the proposed control scheme

From section 3.5.2B, we have:

$$i_1 = \frac{Vref - Vo}{Rs_1\cdot Gm_1\cdot Rd_1} \text{ and } \quad Vo = Vref - \frac{Io}{\sum_{n=1}^{N}\frac{1}{Rs_n\cdot Gm_n\cdot Rd_n}}$$

$$\Rightarrow i_1 = \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}} \cdot \frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1} \quad \textbf{(3.7)}$$

The partial derivatives of (3-7) are the following:

$$\frac{\partial i_1}{\partial Rs_1} = -\frac{\left(\frac{Io}{Rs_1^2 \cdot Gm_1 \cdot Rd_1}\right) \cdot \left(\sum_{n=2}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2}$$

$$\begin{cases} \frac{\partial i_1}{\partial Rs_2} = \frac{\left(\frac{Io}{Rs_2^2 \cdot Gm_2 \cdot Rd_2}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \\ \cdots \\ \frac{\partial i_1}{\partial Rs_N} = \frac{\left(\frac{Io}{Rs_N^2 \cdot Gm_N \cdot Rd_N}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \end{cases}$$

$$\frac{\partial i_1}{\partial Gm_1} = -\frac{\left(\frac{Io}{Rs_1 \cdot Gm_1^2 \cdot Rd_1}\right) \cdot \left(\sum_{n=2}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2}$$

$$\begin{cases} \frac{\partial i_1}{\partial Gm_2} = \frac{\left(\frac{Io}{Rs_2 \cdot Gm_2^2 \cdot Rd_2}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \\ \cdots \\ \frac{\partial i_1}{\partial Gm_N} = \frac{\left(\frac{Io}{Rs_N \cdot Gm_N^2 \cdot Rd_N}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \end{cases}$$

$$\frac{\partial i_1}{\partial Rd_1} = -\frac{\left(\frac{Io}{Rs_1 \cdot Gm_1 \cdot Rd_1^2}\right) \cdot \left(\sum_{n=2}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2}$$

$$\begin{cases} \dfrac{\partial i_1}{\partial Rd_2} = \dfrac{\left(\frac{Io}{Rs_2 \cdot Gm_2 \cdot Rd_2^2}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \\ \cdots\cdot \\ \dfrac{\partial i_1}{\partial Rd_N} = \dfrac{\left(\frac{Io}{Rs_N \cdot Gm_N \cdot Rd_N^2}\right) \cdot \left(\frac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}\right)}{\left(\sum_{n=1}^{N} \frac{1}{Rs_n \cdot Gm_n \cdot Rd_n}\right)^2} \end{cases}$$

Around the design point P_o, we have:

$$\left|\frac{\partial i_1}{\partial Rs_1}\right|_{Po} = \frac{N-1}{N^2} \cdot \frac{Io}{RS}$$

$$\left|\frac{\partial i_1}{\partial Rs_2}\right|_{Po} = \left|\frac{\partial i_1}{\partial Rs_3}\right|_{Po} = \ldots = \left|\frac{\partial i_1}{\partial Rs_N}\right|_{Po} = \frac{1}{N^2} \cdot \frac{Io}{RS}$$

$$\left|\frac{\partial i_1}{\partial Gm_1}\right|_{Po} = \frac{N-1}{N^2} \cdot \frac{Io}{GM}$$

$$\left|\frac{\partial i_1}{\partial Gm_2}\right|_{Po} = \left|\frac{\partial i_1}{\partial Gm_3}\right|_{Po} = \ldots = \left|\frac{\partial i_1}{\partial Gm_N}\right|_{Po} = \frac{1}{N^2} \cdot \frac{Io}{GM}$$

$$\left|\frac{\partial i_1}{\partial Rd_1}\right|_{Po} = \frac{N-1}{N^2} \cdot \frac{Io}{RD}$$

$$\left|\frac{\partial i_1}{\partial Rd_2}\right|_{Po} = \left|\frac{\partial i_1}{\partial Rd_3}\right|_{Po} = \ldots = \left|\frac{\partial i_1}{\partial Rd_N}\right|_{Po} = \frac{1}{N^2} \cdot \frac{Io}{RD}$$

$$\Delta i_1 = \frac{N-1}{N^2}\cdot\frac{Io}{RS}\cdot\Delta Rs_1 + \frac{1}{N^2}\cdot\frac{Io}{RS}\cdot\left(\Delta Rs_2 + ... + \Delta Rs_N\right)$$
$$+\frac{N-1}{N^2}\cdot\frac{Io}{GM}\cdot\Delta Gm_1 + \frac{1}{N^2}\cdot\frac{Io}{GM}\cdot\left(\Delta Gm_2 + ... + \Delta Gm_N\right)$$
$$+\frac{N-1}{N^2}\cdot\frac{Io}{RD}\cdot\Delta Rd_1 + \frac{1}{N^2}\cdot\frac{Io}{RD}\cdot\left(\Delta Rd_2 + ... + \Delta Rd_N\right)$$

Using the same maximum tolerance value for each channel's current sensing element, transcondance amplifier and droop resistor, we have: $\Delta Rs_1 = \Delta Rs_2 = ... = \Delta Rs_N = \Delta Rs$, $\Delta Gm_1 = \Delta Gm_2 = ... = \Delta Gm_N = \Delta Gm$, and $\Delta Rd_1 = \Delta Rd_2 = ... = \Delta Rd_N = \Delta Rd$. Then,

$$\Delta i_1 = 2\cdot\left(\frac{N-1}{N^2}\right)\cdot Io\cdot\left(\frac{\Delta Rs}{RS} + \frac{\Delta Gm}{GM} + \frac{\Delta Rd}{RD}\right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining: $\varepsilon_{Rs} = \frac{\Delta Rs}{RS}$, $\varepsilon_{Gm} = \frac{\Delta Gm}{AS}$, $\varepsilon_{Rd} = \frac{\Delta Rd}{RD}$, we have:

$$\Delta i_1 = 2\cdot\frac{Io}{N}\cdot\left(\frac{N-1}{N}\right)\cdot\left(\varepsilon_{Rs} + \varepsilon_{Gm} + \varepsilon_{Rd}\right)$$

If defining current sharing index as $CS = \frac{\Delta i_1}{Io/N}$, we have:

$$\text{CS} = 2\cdot\left(\frac{N-1}{N}\right)\cdot\left(\varepsilon_{Rs} + \varepsilon_{Gm} + \varepsilon_{Rd}\right) \quad \textbf{(3.8)}$$

E.g. if $\varepsilon_{Rs} = 5\%$, $\varepsilon_{Gm} = 1\%$, $\varepsilon_{Rd} = 1\%$, $N = 4$, $CS = 2\cdot\frac{3}{4}\cdot(5\% + 1\% + 1\%) = 10.5\%$.

3.5.3. AVP and Current Sharing Standard Error Analysis

3.5.3.1. AVP Standard Error Analysis

A. AVP with traditional control schemes

As discussed in section 3.5.1, worst case analysis is usually too pessimistic, but standard error analysis is much closer to the reality.

In section 3.5.2.1A, we get the traditional control scheme's Vo output function

$$Vo = Vref - \frac{Gm \cdot Rd \cdot N \cdot Io}{\left(\frac{1}{Rs_1 \cdot As_1} + \frac{1}{Rs_2 \cdot As_2} + ... + \frac{1}{Rs_N \cdot As_N} \right)}$$

According to the standard error propagation equation, we have:

$$\sigma_{Vo}^2 = \left| \frac{\partial Vo}{\partial Vref} \right|_{Po}^2 \cdot \sigma_{Vr}^2 + \left| \frac{\partial Vo}{\partial Gm} \right|_{Po}^2 \cdot \sigma_{Gm}^2 + \left| \frac{\partial Vo}{\partial Rd} \right|_{Po}^2 \cdot \sigma_{Rd}^2 + \left| \frac{\partial Vo}{\partial Rs_1} \right|_{Po}^2 \cdot \sigma_{Rs_1}^2 + \left| \frac{\partial Vo}{\partial As_1} \right|_{Po}^2 \cdot \sigma_{As_1}^2 + ... + \left| \frac{\partial Vo}{\partial Rs_N} \right|_{Po}^2 \cdot \sigma_{Rs_N}^2 + \left| \frac{\partial Vo}{\partial As_N} \right|_{Po}^2 \cdot \sigma_{As_N}^2$$

Put the partial derivatives of Vo at the design point, which we calculated in section3.5.2.1A, into the above equation, and then we can get:

$$\sigma_{Vo}^2 = \sigma_{Vr}^2 + R_{LL}^2 \cdot Io^2 \cdot \left(\frac{\sigma_{Gm}^2}{GM^2} + \frac{\sigma_{Rd}^2}{RD^2} + \frac{\sigma_{Rs_1}^2}{N^2 \cdot RS^2} + \frac{\sigma_{As_1}^2}{N^2 \cdot AS^2} + ... + \frac{\sigma_{Rs_N}^2}{N^2 \cdot RS^2} + \frac{\sigma_{As_N}^2}{N^2 \cdot AS^2} \right)$$

Using the same standard tolerance value for each channel's current sensing element and for each channel's current scaling amplifier, we have:

$\sigma_{Rs_1} = \sigma_{Rs_2} = ... = \sigma_{Rs_N} = \sigma_{Rs}$, and $\sigma_{As_1} = \sigma_{As_2} = ... = \sigma_{As_N} = \sigma_{As}$,

$$\sigma_{Vo}^2 = \sigma_{Vr}^2 + R_{LL}^2 \cdot Io^2 \cdot \left(\frac{\sigma_{Gm}^2}{GM^2} + \frac{\sigma_{Rd}^2}{RD^2} + \frac{\sigma_{Rs}^2}{N \cdot RS^2} + \frac{\sigma_{As}^2}{N \cdot AS^2} \right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Define: $k_{Gm} = \frac{\sigma_{Gm}}{GM}, k_{Rd} = \frac{\sigma_{Rd}}{RD}, k_{As} = \frac{\sigma_{As}}{AS}, k_{Rs} = \frac{\sigma_{Rs}}{RS}$, $k_{Vr} = \frac{\sigma_{Vr}}{VR}$, and then

$$\sigma_{Vo}^2 = VR^2 \cdot k_{Vr}^2 + R_{LL}^2 \cdot Io^2 \cdot \left(k_{Gm}^2 + k_{Rd}^2 + \frac{1}{N} \cdot k_{As}^2 + \frac{1}{N} \cdot k_{Rs}^2 \right)$$

$$\sigma_{Vo}=\sqrt{VR^2\cdot k_{Vr}^2+R_{LL}^2\cdot Io^2\cdot\left(k_{Gm}^2+k_{Rd}^2+\frac{1}{N}\cdot k_{As}^2+\frac{1}{N}\cdot k_{Rs}^2\right)}$$

E.g. if $k_{Gm}=1\%, k_{Rd}=1\%, k_{As}=1\%, k_{Rs}=5\%, k_{Vr}=0.5\%$, $VR=1, Io=100, N=4$,

$$\sigma_{Vo}=\sqrt{1^2\cdot 0.005^2+0.001^2\cdot 100^2\cdot\left(0.01^2+0.01^2+\frac{1}{4}\cdot 0.01^2+\frac{1}{4}\cdot 0.05^2\right)}=5.78(mV)$$

B. AVP with the proposed control scheme

In section 3.5.2.1B, we get $Vo=Vref-\dfrac{Io}{\sum_{n=1}^{N}\dfrac{1}{Rs_n\cdot Gm_n\cdot Rd_n}}$. We also get the partial derivatives of Vo at the design point. Then,

$$\begin{aligned}\sigma_{Vo}^2&=\left|\frac{\partial Vo}{\partial Vref}\right|_{Po}^2\cdot\sigma_{Vref}^2+\left|\frac{\partial Vo}{\partial Rs_1}\right|_{Po}^2\cdot\sigma_{Rs_1}^2+\left|\frac{\partial Vo}{\partial Gm_1}\right|_{Po}^2\cdot\sigma_{Gm_1}^2+\left|\frac{\partial Vo}{\partial Rd_1}\right|_{Po}^2\cdot\sigma_{Rd_1}^2\\&\quad+....\left|\frac{\partial Vo}{\partial Rs_N}\right|_{Po}^2\cdot\sigma_{Rs_N}^2+\left|\frac{\partial Vo}{\partial Gm_N}\right|_{Po}^2\cdot\sigma_{Gm_N}^2+\left|\frac{\partial Vo}{\partial Rd_N}\right|_{Po}^2\cdot\sigma_{Rd_N}^2\\&=\sigma_{Vref}^2+R_{LL}^2\cdot Io^2\cdot\left(\frac{\sigma_{Rs_1}^2}{N^2\cdot RS^2}+\frac{\sigma_{Gm_1}^2}{N^2\cdot GM^2}+\frac{\sigma_{Rd_1}^2}{N^2\cdot RD^2}+...+\frac{\sigma_{Rs_N}^2}{N^2\cdot RS^2}+\frac{\sigma_{Gm_N}^2}{N^2\cdot GM^2}+\frac{\sigma_{Rd_N}^2}{N^2\cdot RD^2}\right)\end{aligned}$$

Using the same standard tolerance value for each channel's current sensing element, transconductance amplifier and droop resistor, we have:

$\sigma_{Rs_1}=\sigma_{Rs_2}=...=\sigma_{Rs_N}=\sigma_{Rs}$, and $\sigma_{Gm_1}=\sigma_{Gm_2}=...=\sigma_{Gm_N}=\sigma_{Gm}$,

$\sigma_{Rd_1}=\sigma_{Rd_2}=...=\sigma_{Rd_N}=\sigma_{Rd}$.

Then, $\sigma_{Vo}^2=\sigma_{Vref}^2+R_{LL}^2\cdot Io^2\cdot\left(\dfrac{\sigma_{Rs}^2}{N\cdot RS^2}+\dfrac{\sigma_{Gm}^2}{N\cdot GM^2}+\dfrac{\sigma_{Rd}^2}{N\cdot RD^2}\right)$.

Since $Vref=\dfrac{Vref_1+Vref_2+...+Vref_N}{N}$,

$$\sigma_{Vref}^2 = \left|\frac{\partial Vo}{\partial Vref_1}\right|_{Po}^2 \cdot \sigma_{Vref1}^2 + \left|\frac{\partial Vo}{\partial Vref_2}\right|_{Po}^2 \cdot \sigma_{Vref2}^2 + ... + \left|\frac{\partial Vo}{\partial Vref_N}\right|_{Po}^2 \cdot \sigma_{VrefN}^2,$$
$$= \frac{1}{N^2} \cdot \sigma_{Vref1}^2 + \frac{1}{N^2} \cdot \sigma_{Vref2}^2 + ... + \frac{1}{N^2} \cdot \sigma_{VrefN}^2$$

and using the same standard tolerance value for each channel's voltage reference,

we have: $\sigma_{Vref_1} = \sigma_{Vref_2} = ... = \sigma_{Vref_N} = \sigma_{Vr}$, and then $\sigma_{Vref}^2 = \frac{\sigma_{Vr}^2}{N}$. Therefore,

$$\sigma_{Vo}^2 = \frac{\sigma_{Vr}^2}{N} + R_{LL}^2 \cdot Io^2 \cdot \left(\frac{\sigma_{Rs}^2}{N \cdot RS^2} + \frac{\sigma_{Gm}^2}{N \cdot GM^2} + \frac{\sigma_{Rd}^2}{N \cdot RD^2} \right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining: $k_{Gm} = \frac{\sigma_{Gm}}{GM}, k_{Rd} = \frac{\sigma_{Rd}}{RD}, k_{Rs} = \frac{\sigma_{Rs}}{RS}, k_{Vr} = \frac{\sigma_{Vr}}{VR}$, we have

$$\sigma_{Vo}^2 = \frac{VR^2 \cdot k_{Vr}^2}{N} + R_{LL}^2 \cdot Io^2 \cdot \frac{k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2}{N}$$

$$\sigma_{Vo} = \sqrt{\frac{VR^2 \cdot k_{Vr}^2}{N} + R_{LL}^2 \cdot Io^2 \cdot \frac{k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2}{N}} \quad \textbf{(3.10)}$$

For example, if $k_{Gm} = 1\%, k_{Rd} = 1\%, k_{Rs} = 5\%, k_{Vr} = 0.5\%$, $VR = 1, Io = 100, N = 4$,

$$\sigma_{Vo} = \sqrt{\frac{1^2 \cdot 0.005^2}{4} + 0.001^2 \cdot 100^2 \cdot \left(\frac{0.05^2 + 0.01^2 + 0.01^2}{4} \right)} = 3.606(mV)$$

3.5.3.2. Current Sharing Standard Error Analysis

A. Current sharing with traditional control schemes

In section 3.5.2.2A, we get $i_1 = \frac{Io}{\sum_{n=1}^{N} \frac{1}{Rs_n \cdot As_n}} \cdot \frac{1}{Rs_1 \cdot As_1}$. We also get the partial derivatives of i_1 at the design point. Then,

$$\sigma_{i_1}^2 = \left|\frac{\partial i_1}{\partial Rs_1}\right|_{Po}^2 \cdot \sigma_{Rs_1}^2 + \left|\frac{\partial i_1}{\partial Rs_2}\right|_{Po}^2 \cdot \sigma_{Rs_2}^2 + \ldots + \left|\frac{\partial i_1}{\partial Rs_N}\right|_{Po}^2 \cdot \sigma_{Rs_N}^2$$
$$+ \left|\frac{\partial i_1}{\partial As_1}\right|_{Po}^2 \cdot \sigma_{As_1}^2 + \left|\frac{\partial i_1}{\partial As_2}\right|_{Po}^2 \cdot \sigma_{As_2}^2 + \ldots + \left|\frac{\partial i_1}{\partial As_N}\right|_{Po}^2 \cdot \sigma_{As_N}^2$$

$$= \left(\frac{N-1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot \sigma_{Rs_1}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot \left(\sigma_{Rs_2}^2 + \ldots + \sigma_{Rs_N}^2\right)$$
$$+ \left(\frac{N-1}{N^2} \cdot \frac{Io}{AS}\right)^2 \cdot \sigma_{As_1}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{AS}\right)^2 \cdot \left(\sigma_{As_2}^2 + \ldots + \sigma_{As_N}^2\right)$$

Using the same standard tolerance value for each channel's current sensing element and for each channel's current scaling amplifier, we have:

$\sigma_{Rs_1} = \sigma_{Rs_2} = \ldots = \sigma_{Rs_N} = \sigma_{Rs}$, and $\sigma_{As_1} = \sigma_{As_2} = \ldots = \sigma_{As_N} = \sigma_{As}$. Then,

$$\sigma_{i_1}^2 = \left(\frac{N-1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot \sigma_{Rs}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot (N-1)\left(\sigma_{Rs}^2\right)$$
$$+ \left(\frac{N-1}{N^2} \cdot \frac{Io}{AS}\right)^2 \cdot \sigma_{As}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{AS}\right)^2 \cdot (N-1)\left(\sigma_{As}^2\right) = \frac{N-1}{N} \cdot \frac{Io^2}{N^2} \cdot \left(\frac{\sigma_{Rs}^2}{RS^2} + \frac{\sigma_{As}^2}{AS^2}\right)$$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Define: $k_{Rs} = \frac{\sigma_{Rs}}{RS}$, $k_{As} = \frac{\sigma_{As}}{AS}$, and then

$$\sigma_{i_1}^2 = \frac{N-1}{N} \cdot \frac{Io^2}{N^2} \cdot \left(k_{Rs}^2 + k_{As}^2\right) \Rightarrow \sigma_{i_1} = \frac{Io}{N}\sqrt{\frac{N-1}{N} \cdot \left(k_{Rs}^2 + k_{As}^2\right)}$$

If defining the current sharing index as $CS = \frac{\sigma_{i_1}}{Io/N}$, we have:

$$\text{CS} = \sqrt{\frac{N-1}{N} \cdot \left(k_{Rs}^2 + k_{As}^2\right)} \quad \textbf{(3.11)}$$

For example, if $k_{Rs} = 5\%$, $k_{As} = 1\%$, $N = 4$, $CS = \sqrt{\frac{3}{4} \cdot \left(0.05^2 + 0.01^2\right)} = 4.4\%$

B. Current sharing with the proposed control scheme

In section 3.5.2.2B, we get. $i_1 = \dfrac{Io}{\sum_{n=1}^{N} \dfrac{1}{Rs_n \cdot Gm_n \cdot Rd_n}} \cdot \dfrac{1}{Rs_1 \cdot Gm_1 \cdot Rd_1}$. We also get the

partial derivatives of i_1 at the design point. Then,

$$\sigma_{i_1}^2 = \left(\frac{N-1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot \sigma_{Rs}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{RS}\right)^2 \cdot (N-1) \cdot \sigma_{Rs_2}^2$$
$$+ \left(\frac{N-1}{N^2} \cdot \frac{Io}{GM}\right)^2 \cdot \sigma_{Gm_1}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{GM}\right)^2 \cdot \left(\sigma_{Gm_2}^2 + \ldots + \sigma_{Gm_N}^2\right)$$
$$+ \left(\frac{N-1}{N^2} \cdot \frac{Io}{RD}\right)^2 \cdot \sigma_{Rd_1}^2 + \left(\frac{1}{N^2} \cdot \frac{Io}{RD}\right)^2 \cdot \left(\sigma_{Rd_2}^2 + \ldots + \sigma_{Rd_N}^2\right)$$

Using the same standard tolerance value for each channel's current sensing element, transconductance amplifier and droop resistor, we have:

$\sigma_{Rs_1} = \sigma_{Rs_2} = \ldots = \sigma_{Rs_N} = \sigma_{Rs}$, $\sigma_{Gm_1} = \sigma_{Gm_2} = \ldots = \sigma_{Gm_N} = \sigma_{Gm}$, and

$\sigma_{Rd_1} = \sigma_{Rd_2} = \ldots = \sigma_{Rd_N} = \sigma_{Rd}$. Then, $\sigma_{i_1}^2 = \dfrac{N-1}{N} \cdot \dfrac{Io^2}{N^2} \cdot \left(\dfrac{\sigma_{Rs}^2}{RS^2} + \dfrac{\sigma_{Gm}^2}{GM^2} + \dfrac{\sigma_{Rd}^2}{RD^2}\right)$

In industry, the component tolerances are often formatted as relative value instead of absolute value. Defining $k_{Gm} = \dfrac{\sigma_{Gm}}{GM}$, $k_{Rd} = \dfrac{\sigma_{Rd}}{RD}$, $k_{Rs} = \dfrac{\sigma_{Rs}}{RS}$, we have:

$$\sigma_{i_1}^2 = \frac{N-1}{N} \cdot \frac{Io^2}{N^2} \cdot \left(k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2\right)$$

If defining current sharing index as $CS = \dfrac{\sigma_{i_1}}{Io/N}$, we have:

$$\text{CS} = \sqrt{\frac{N-1}{N} \cdot \left(k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2\right)} \quad \textbf{(3.12)}$$

E.g. if $k_{Rs} = 5\%$, $k_{Gm} = 1\%$, $k_{Rd} = 1\%$, $N = 4$, $CS = \sqrt{\dfrac{3}{4} \cdot \left(0.05^2 + 0.01^2 + 0.01^2\right)} = 4.5\%$

3.5.4. Summary of AVP and Current Sharing Tolerance Analysis

Parameters	Description	Typical values [C34]
R_{LL}	Specified VR Load line resistance	1mΩ
Io	The maximum VR output current	100 A
VR	Ideal VR voltage reference value	1 V
ε_{Vr}	Relative maximum tolerance of VR voltage reference	0.5%
k_{Vr}	Relative standard tolerance of VR voltage reference within 3σ	0.5%
ε_{Rs}	Relative maximum tolerance of VR current sensing elements	1% for resistor sensing; 5% for inductor sensing.
k_{Rs}	Relative standard tolerance of VR current sensing elements within 3σ	1% for resistor sensing; 5% for inductor sensing.
ε_{As}	Relative maximum tolerance of current sensing scaling amplifier	1%
k_{As}	Relative standard tolerance of current sensing scaling amplifier within 3σ	1%
ε_{Gm}	Relative maximum tolerance of V/I conversion amplifier	1%
k_{Gm}	Relative standard tolerance of V/I conversion amplifier within 3σ	1%
ε_{Rd}	Relative maximum tolerance of droop resistor	1%
k_{Rd}	Relative standard tolerance of droop resistor within 3σ	1%
V_{TC}	Maximum VR output voltage deviation due to the uncompensated temperature dependence of current sensing elements	0 for resistor sensing; 2mV for inductor sensing.
V_{ripple}	Maximum VR output voltage ripple	10 mV
TOB'	Maximum VR output voltage deviation including the tolerance due to voltage ripple and temperature dependence	< 20 mV
TOB	VR tolerance band ---- Maximum VR output voltage deviation within 3σ, including the tolerance due to voltage ripple and temperature dependence	< 20 mV
CS'	The ratio of each channel's maximum current deviation over each channel's ideal current,	< 10%
CS	Current sharing index ---- The ratio of each channel's maximum current deviation within 3σ over each channel's ideal current	< 10%

Table 3-3. Parameters used in tolerance analysis.

Table 3-3 shows the parameters and their typical values used in tolerance calculation. Table 3-4 shows the equations based on the worst case analysis in section 3.5.2. Table 3-5 shows the equations based on stochastic analysis in section 3.5.3.

AVP	$TOB'\_traditional = VR \cdot \varepsilon_{Vr} + R_{LL} \cdot Io \cdot \left(\varepsilon_{Gm} + \varepsilon_{Rd} + \varepsilon_{As} + \varepsilon_{Rs}\right) + V_{TC} + V_{ripple}$ $TOB'\_proposed = VR \cdot \varepsilon_{Vr} + R_{LL} \cdot Io \cdot \left(\varepsilon_{Gm} + \varepsilon_{Rd} + \varepsilon_{Rs}\right) + V_{TC} + V_{ripple}$
Current Sharing	$CS'\_traditional = 2 \cdot \left(\frac{N-1}{N}\right) \cdot \left(\varepsilon_{Rs} + \varepsilon_{As}\right)$ $CS'\_proposed = 2 \cdot \left(\frac{N-1}{N}\right) \cdot \left(\varepsilon_{Rs} + \varepsilon_{Gm} + \varepsilon_{Rd}\right)$

Table 3-4. Equations based on worst case analysis

AVP	$TOB\_traditional = \sqrt{VR^2 \cdot k_{Vr}^2 + R_{LL}^2 \cdot Io^2 \cdot \left(k_{Gm}^2 + k_{Rd}^2 + \frac{k_{As}^2 + k_{Rs}^2}{N}\right)} + V_{TC} + V_{ripple}$ $TOB\_proposed = \sqrt{\frac{VR^2 \cdot k_{Vr}^2}{N} + R_{LL}^2 \cdot Io^2 \cdot \frac{k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2}{N}} + V_{TC} + V_{ripple}$
Current Sharing	$CS\_traditional = \sqrt{\frac{N-1}{N} \cdot \left(k_{Rs}^2 + k_{As}^2\right)}$ $CS\_proposed = \sqrt{\frac{N-1}{N} \cdot \left(k_{Rs}^2 + k_{Gm}^2 + k_{Rd}^2\right)}$

Table 3-5. Equations based on stochastic analysis.

In tables 3-4 and 3-5, "TOB" means voltage tolerance band, which is defined in section 3.1. However, the analysis in section 3.5.2.1 and 3.5.3.1 does not consider the output voltage ripple and the temperature dependence. Based on industry's study [C16], the budget of voltage ripple is V_{ripple}=10mV, and the budget of voltage deviation V_{TC} due to the uncompensated temperature dependence of current sensing elements is 3mV. These items are added into the original tolerance analysis results based on the concept described in section 3.5.1.3 to calculate the VR output voltage tolerance band.

Table 3-6 shows some design examples based on the calculation in table 3-5 and using the typical technology parameter values shown in table 3-3. In table 3-6, "today's SPEC" is from Intel VRM9.1 design guidelines, and "future's SPEC" is based on the discussion in Chapter 1.

VREF=1.5V, R_{LL} = 1.5mΩ, Imax=70A, N=4		
TOB (mV)	Current Sensing by	
	Rext	R_L
Traditional	18	20
Proposed	14	17

a. TOB with today's SEPC

VREF=0.8V, R_{LL} = 0.8mΩ, Imax=150A, N=8		
TOB (mV)	Current Sensing by	
	Rext	R_L
Traditional	14	17
Proposed	12	15

b. TOB with future's SEPC

VREF=1.5V, R_{LL}=1.5mΩ, Imax=70A, N=4		
CS	Current Sensing by	
	Rext	R_L
Traditional	1.2%	4.4%
Proposed	1.5%	4.5%

c. CS with today's SEPC

VREF=0.8V, R_{LL} = 0.8mΩ, Imax=150A, N=8		
CS	Current Sensing by	
	Rext	R_L
Traditional	1.3%	4.7%
Proposed	1.6%	4.8%

d. CS with future's SEPC

Table 3-6. Design examples based on the calculation in table 3-5.

From tables 3-4, 3-5 and 3-6, it is easy to know that if the same current sensing approach is used, the proposed distributed control scheme has better output voltage tolorance band than the traditional centralized control scheme, and the current sharing performance is almost the same as the traditional scheme.

In reality, the current sharing of the proposed distributed control scheme could be better than the traditional scheme because in the traditional scheme, current sharing is sensitive to comparator delay and the matching of carrier signals while the proposed distributed control scheme does not have such a problem [C36].

3.6. AVP and Current Sharing Monte Carlo Simulation

3.6.1. Monte Carlo Simulation

Section 3.5 gives the tolerance analysis results of AVP and current sharing for the traditional VR control scheme and the proposed distributed control scheme. However, the analysis is only for the steady state. At transient, the model of the system becomes very complex; the error propagation approaches as in section 3.5 are too time consuming to be set up, and the equation derivations can be too complex to be handled by the designer. Luckily, there are simulation tools based on Monte Carlo analysis, which can handle such complex cases.

Monte Carlo analysis is a stochastic tool used to calculate the overall error of a model by varying simultaneously all relevant influence factors. It is especially useful in complex models with a great number of complex influence factors, where classical error propagation approaches are too time consuming to be set up while showing some validity limits. In Monte Carlo analysis, an algorithm generates stochastically distributed random sets of parameters, and each of them follows its own stochastic distribution with its own standard deviation.

Monte Carlo analysis is most famous for its use in the design of the atomic bomb during the Second World War. It has also been used in diverse applications, such as the analysis of traffic flow on superhighways, the development of models for the evolution of stars, and the attempts to predict fluctuations in the stock market. The scheme also finds applications in integrated circuit design, quantum mechanics, and communication engineering. Until now, Monte Carlo analysis is still the most accurate and flexible tool

for error calculation. Today, all the IC design software packages provide the simulation tool to do Monte Carlo analysis.

Since Monte Carlo simulation is a means of statistical evaluation of mathematical functions using random samples, it requires a good source of random numbers. There are always some errors involved in with this scheme, but the larger the number of random samples taken, the more accurate the result. Therefore, although Monte Carlo simulation is easy to be set up, it can be computationally expensive to be used. Monte Carlo simulation usually takes hours or even days to give meaningful results due to the large number of iterations with different parameter values.

Nevertheless, Monte Carlo simulation is the only tool available to do the tolerance analysis for the complex case like a multiphase VR's transient response. One case study is provided in next section with Monte Carlo simulation. The objective of this simulation is to see the impacts of nonideal components on the VR AVP transient performance, and to verify the steady state analysis results provided in section 3.5.

3.6.2 A Case Study of Monte Carlo Simulation

A four phase VR is designed according to VRM9.1 design guide with the traditional control scheme, as shown in Fig. 3-17 and Fig.3-19, and the proposed control scheme, as shown in Fig. 3-31. In the design, the input voltage is 12V. Each channel's switching frequency is 1MHz. For each component, the tolerance distribution function and its value are set up according to table 3-7.

Parameters	Description	Simulation setup
R_{LL}	Specified VR Load line resistance	1.5mΩ
Io	The maximum VR output current	70 A
VR	Ideal VR voltage reference value	1.5 V
k_{Vr}	Relative standard tolerance of VR voltage reference within 3σ	0.5%
RS	Specified value of current sensing elements	1.5mΩ
k_{Rs}	Relative standard tolerance of VR current sensing elements within 3σ	5%
AS	Specified value of current sensing scaling amplifier	1
k_{As}	Relative standard tolerance of current sensing scaling amplifier within 3σ	1%
GM	Specified value of V/I conversion amplifier	1mA/V
k_{Gm}	Relative standard tolerance of V/I conversion amplifier within 3σ	1%
RD	Specified value of droop resistor	1.5KΩ in traditional scheme; 6 KΩ in proposed scheme
k_{Rd}	Relative standard tolerance of droop resistor within 3σ	1%
L	Specified value of Each channel's inductor	100nH
k_L	Relative standard tolerance of each channel's inductor value within 3σ	20%
RON	Specified value of Each power MOSFET on resistance	5mΩ
k_{RON}	Relative standard tolerance of each power MOSFET on resistance within 3σ	30%
CO	Specified value of VR output cap within	2000 uF
k_{Co}	Relative standard tolerance of VR output cap within 3σ	30%
RC	Specified value of VR output cap ESR	1mΩ
k_{Rc}	Relative standard tolerance of VR output cap ESR within 3σ	30%
k_R	Relative standard tolerance of External small signal resistor within 3σ	1%
k_C	Relative standard tolerance of External small signal cap within 3σ	15%

Table 3-7. Monte Carlo simulation setup.

Fig. 3-41 shows the results of steady state simulation. There are 400 curves there, 200 green curves and 200 red curves respectively. The red are the curves of the traditional control; the green are the curves of the proposed control. And all the curves are inside the VRM 9.1 specified voltage regular window. And the distribution of green curves is within the band of red curves, which shows that the proposed control scheme has better tolerance band. This verifies the conclusion in section 3.5. Fig. 3-42 shows results of transient simulation. We can also get the same conclusion. Monte Carlo simulation results in Fig. 3-43 show that the current sharing of the proposed control is comparable with that of the traditional control.

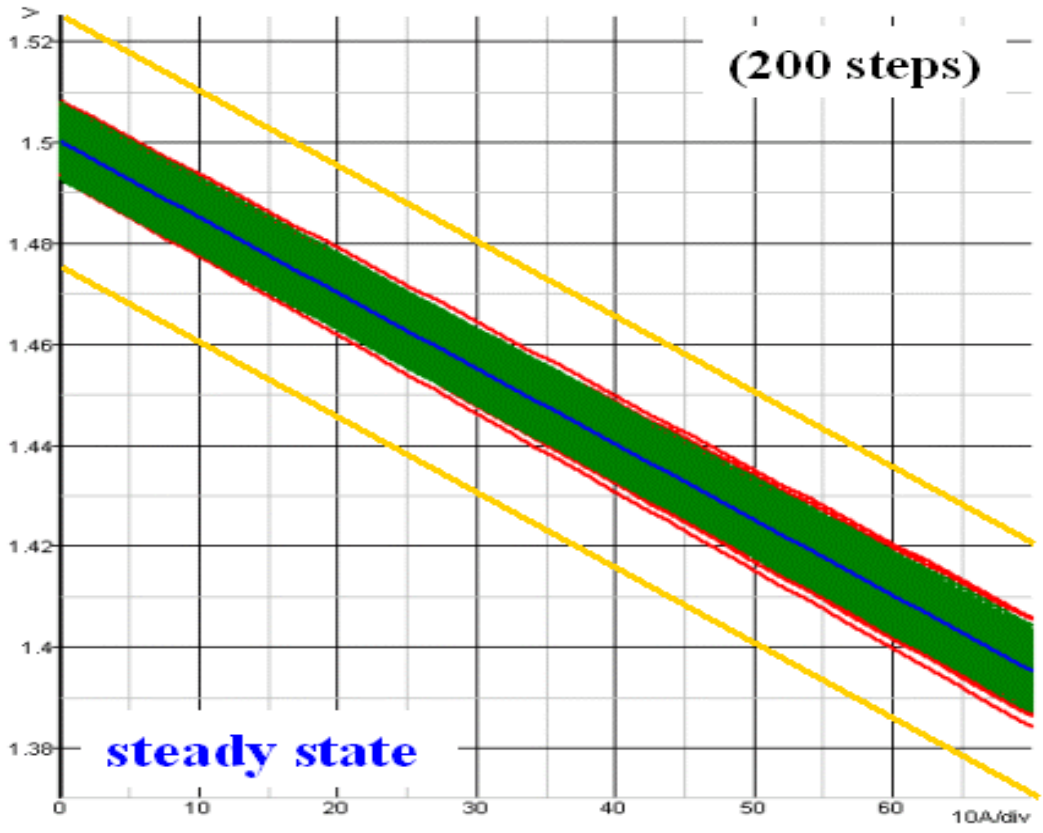


Fig. 3-41. Monte Carlo simulation results: AVP at steady state
(Green: proposed control, Red: traditional control).

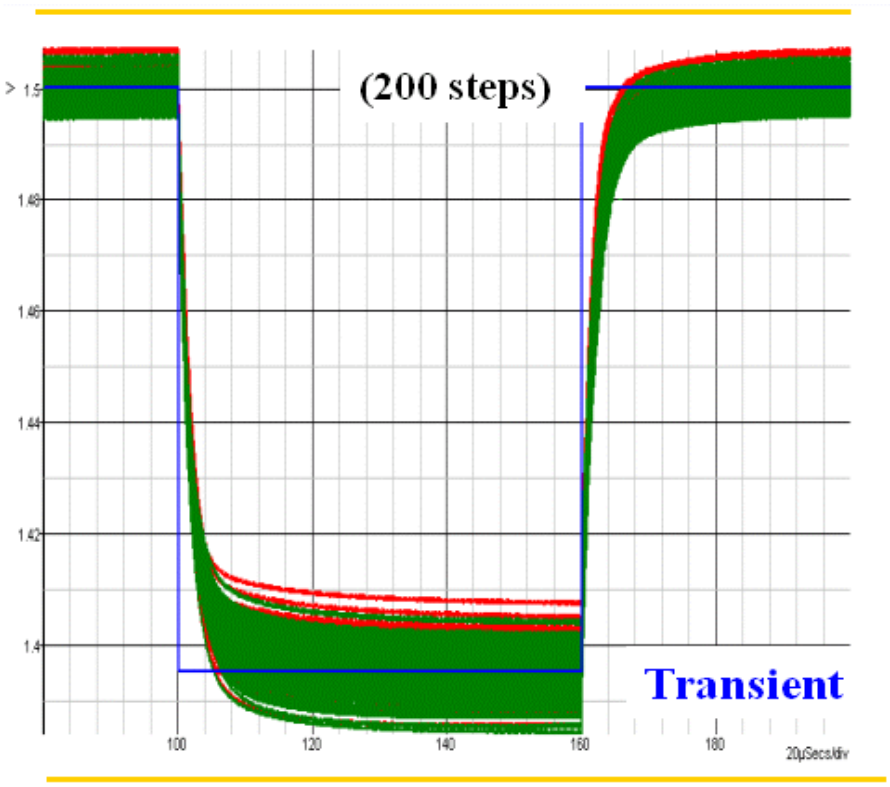


Fig. 3-42. Monte Carlo simulation results: AVP transient
(Green: proposed control, Red: traditional control).

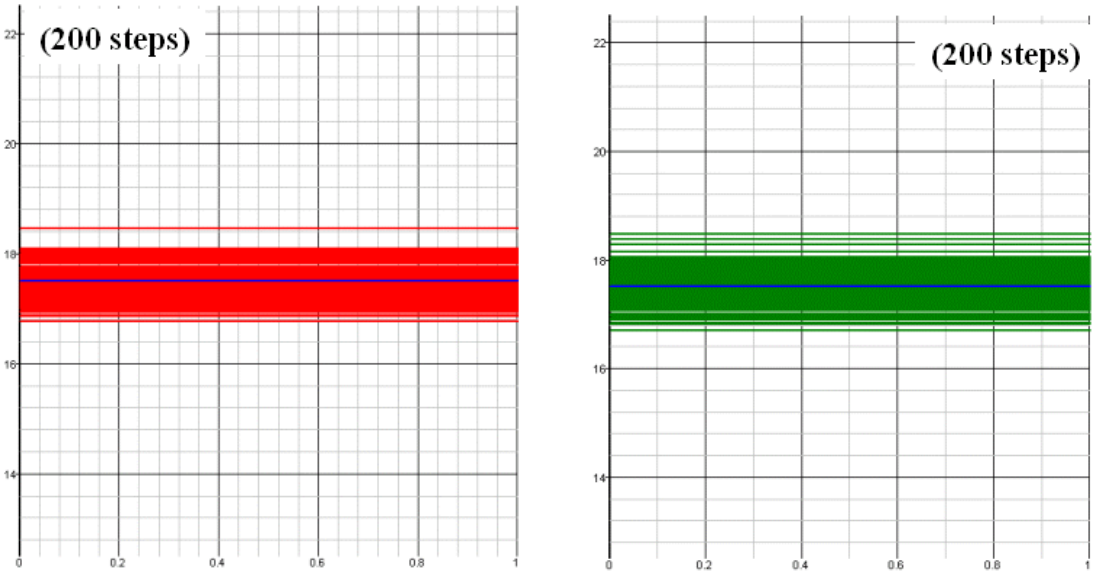


Fig. 3-43. Monte Carlo simulation results: current sharing
(Green: proposed control; Red: traditional control).

3.7. Hardware Verification of the Proposed AVP and CS Schemes

3.7.1. Design Specifications

Fig. 3-44 shows the design specifications for the hardware prototype based on the proposed control scheme. The specifications are a projection of future's CPU power requirements. The total current may vary from 40A to 120A, but the target load line always is 1mΩ. The TOB is 20mV and the 0 load output voltage is 1.000V.

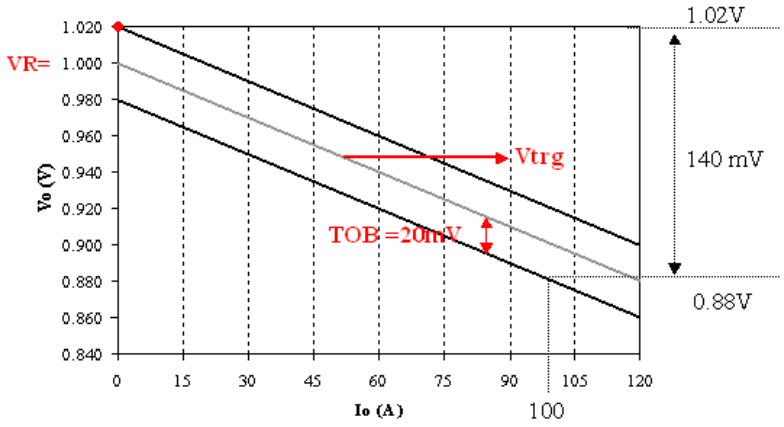


Fig. 3-44. Design specifications.

3.7.2. Hardware Description

A "discrete version" prototype using general Opamp, comparator, analog switch, digital gates as basic building components is developed according to the proposed interleaving, AVP and current sharing schemes. Fig. 3-45 identifies the location of the proposed interleaving circuit and AVP-CS circuit on the hardware prototype. The transient emulator is also identified. The transient emulator can produce large current pulse with 10A/ns di/dt. It is used to test voltage regulator's AVP transient performance.

In each channel's power stage, the top device is Vishay's Si4390; the bottom device is Vishay's Si4368; the driver is National's LM2726; and the inductor is 100nH/1.2mΩ. Each channel's switching frequency is 1MHz and current rating is about 20A. The 47uF

ceramic caps are adopted as output caps. The number of caps is 4×N (N is channel number).

With the four-layer PCB broad shown in Fig. 3-45, a 1~6 phase VR with the proposed control can be tested. Different current sensing schemes can also be selected with the specially designed jumper on the broad.

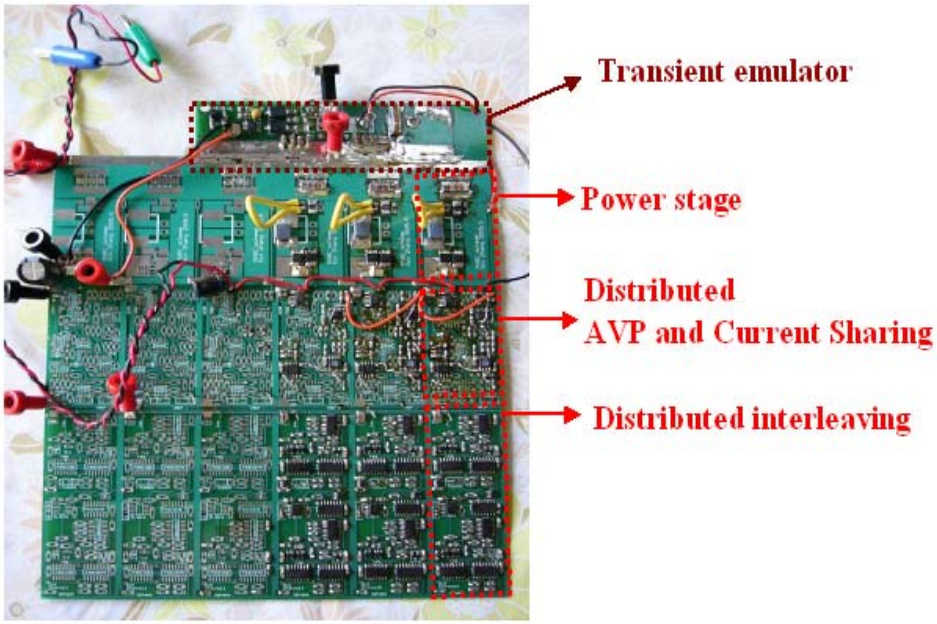
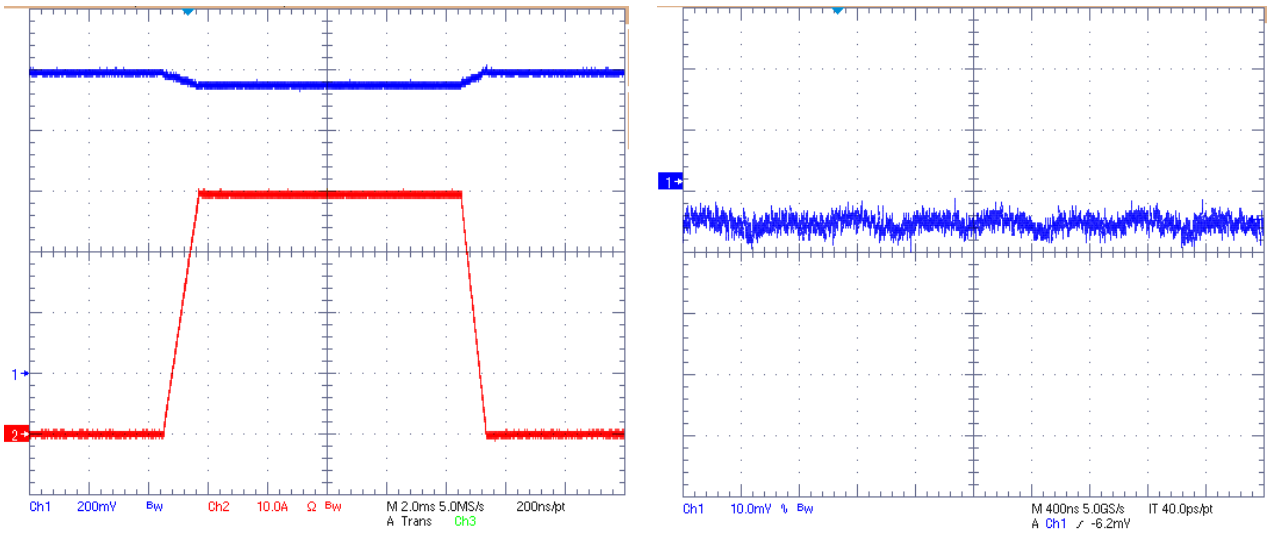


Fig. 3-45. Photo of hardware.

3.7.3. Testing Results

Exclusive experiments are conducted using the above board. AVP and current sharing waveforms are measured for the 2~6 phase VR circuit with different sets of components. To save the profile of this dissertation, only 2 phase and 3 phase testing results are reported in this section. Figures 3-46~3-61 and tables 3-8~3-11 demonstrate that the proposed control can meet future CPU power management's design specifications with resistor current sensing and inductor current sensing. Measurement with different sets of components further verifies the tolerance analysis in section 3.5 and 3.6.

3.7.3.1. 2 Phase 40A Design with Resistor Current Sensing



a. Adaptive voltage position b. Output voltage ripple

Fig. 3-46. Voltage regulation of 2 phase VR with the proposed control and resistor current sensing (Red: Io, Blue: Vo).

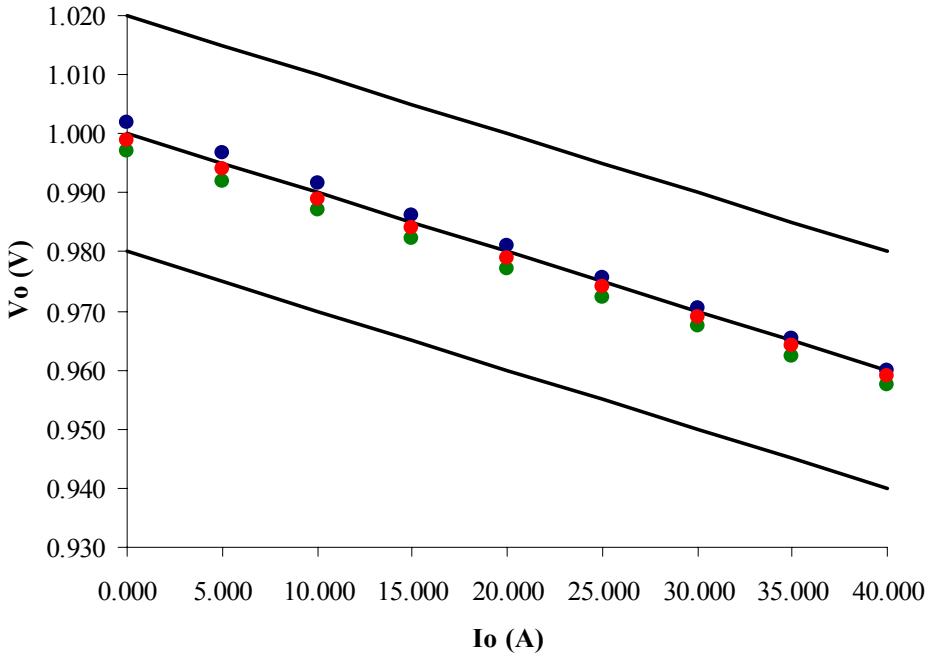
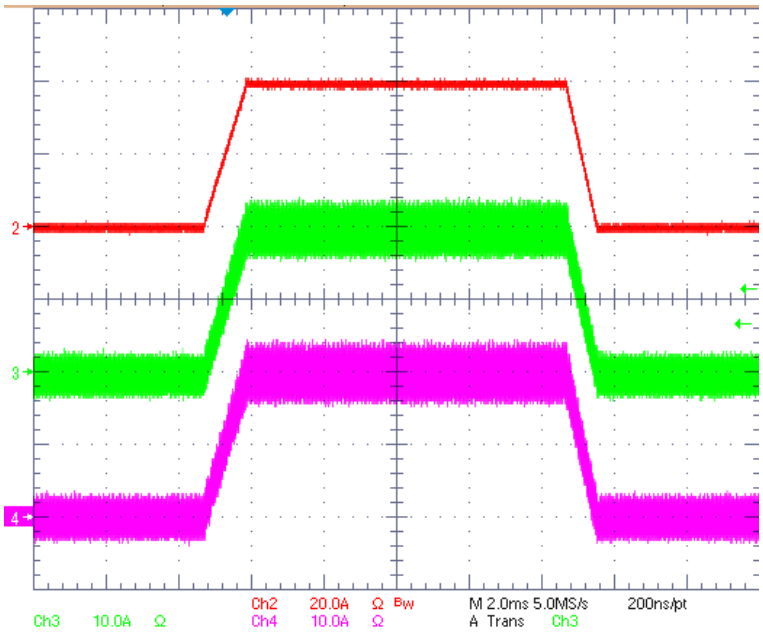
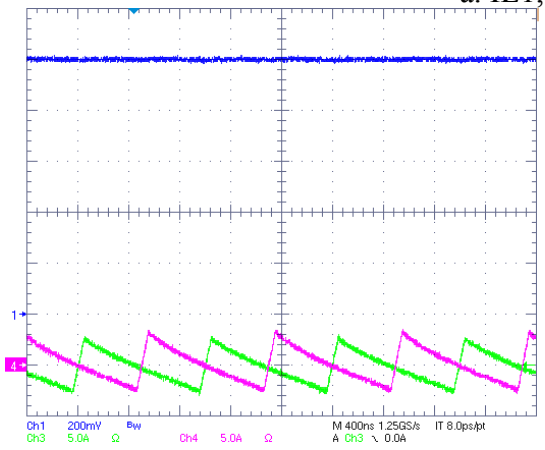


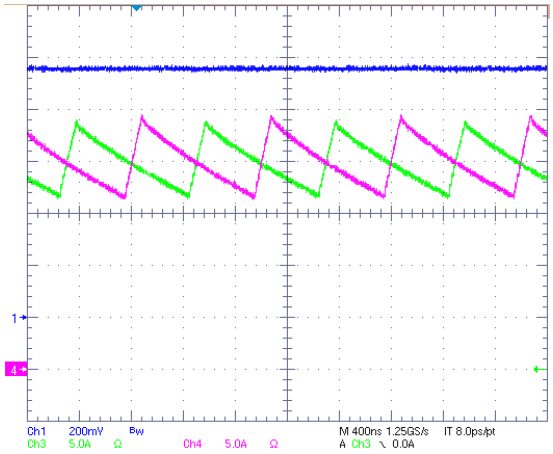
Fig. 3-47. Load lines of 2 phase VR with the proposed control and resistor current sensing (Red: DUT1, Blue: DUT1, Green: DUT3).



a. IL1, IL2 and Io



b. at light load



c. at full load

Fig. 3-48. Current sharing of 2 phase VR with the proposed control and resistor current sensing (Red: Io, Pink: IL1, Green:IL2, Blue: Vo).

	Io = 0A		Io ≈ 40A	
	IL1	IL2	IL1	IL2
DUT1	<0.1A	<0.1A	19.81A	19.92A
DUT2	<0.1A	<0.1A	20.29A	20.12A
DUT3	<0.1A	<0.1A	20.11A	19.97A

Table 3-8. Summary of current sharing of 2 phase VR with the proposed control and resistor current sensing.

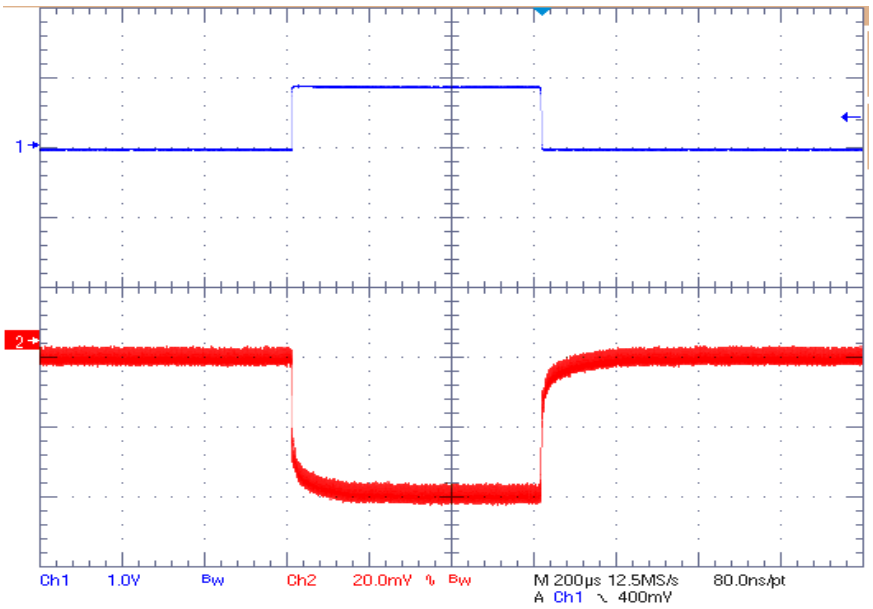
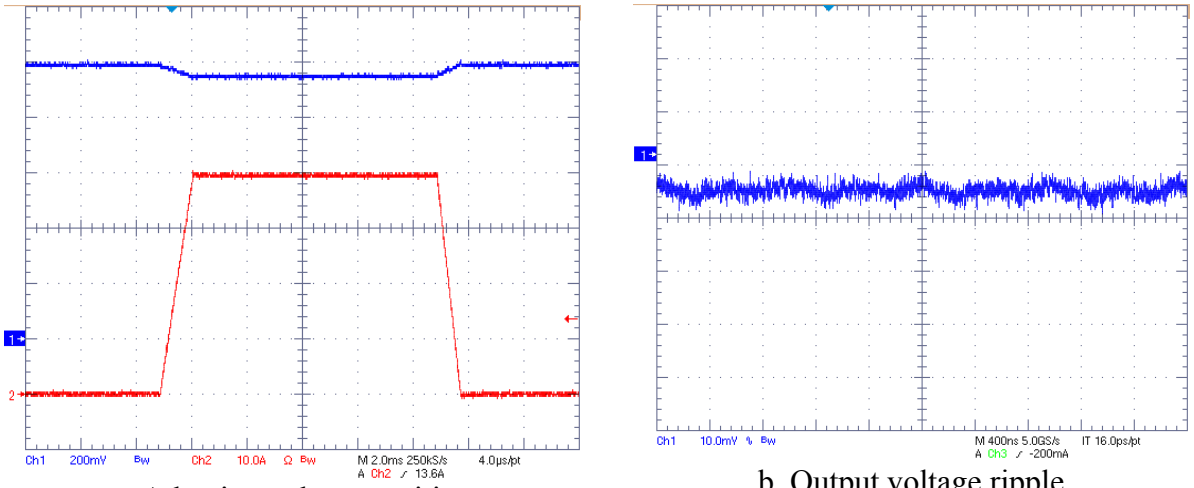


Fig. 3-49. AVP transient of 2 phase VR with the proposed control and resistor current sensing.

3.7.3.2. 2 Phase 40A Design with Inductor Current Sensing



a. Adaptive voltage position b. Output voltage ripple

Fig. 3-50. Voltage regulation of 2 phase VR with the proposed control and inductor current sensing (Red: Io, Blue: Vo).

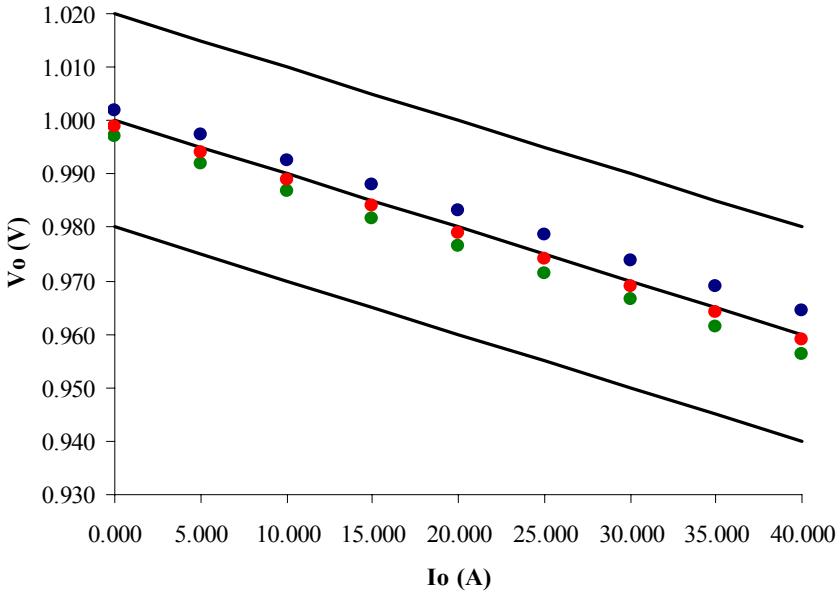
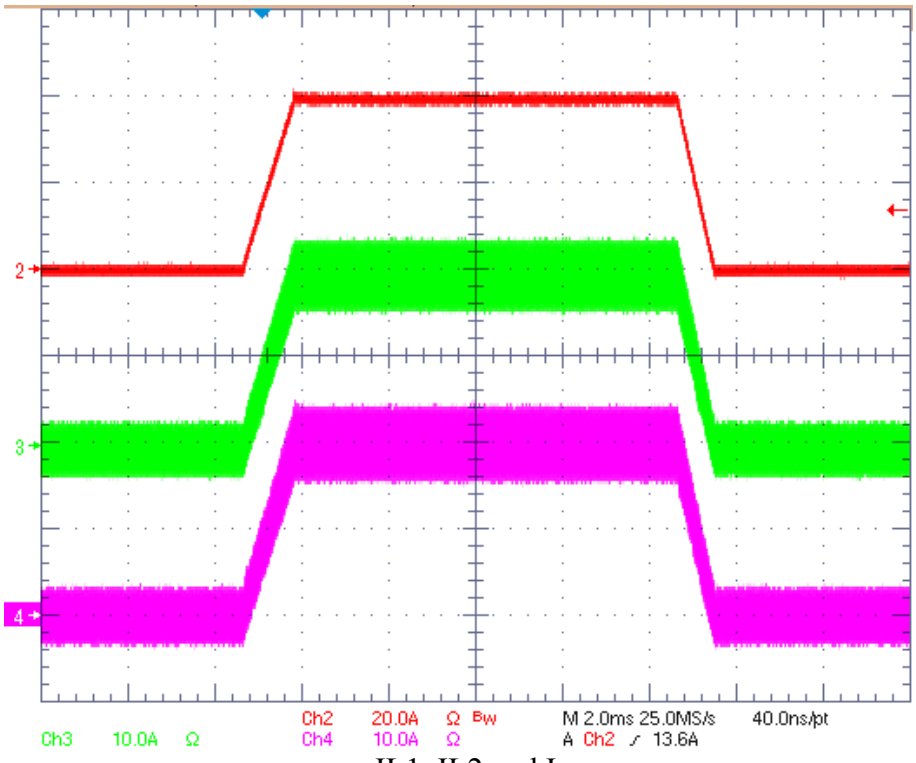
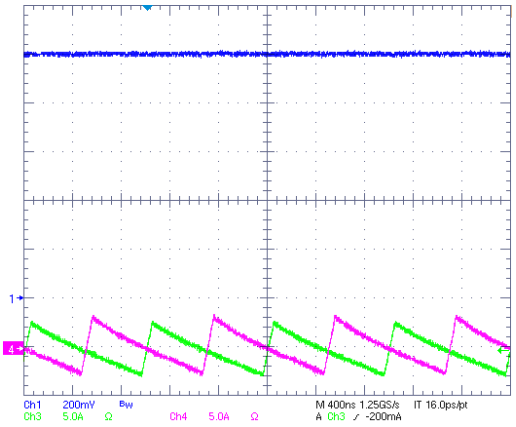


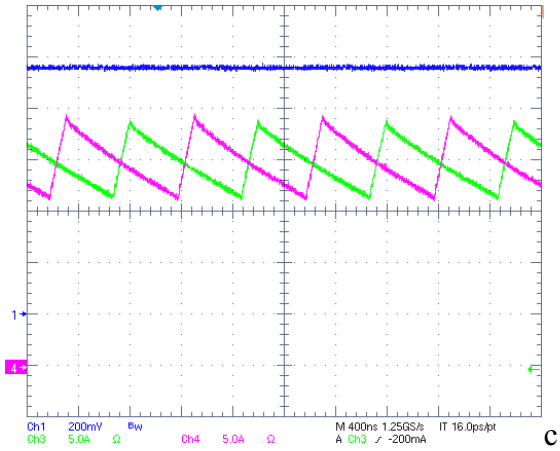
Fig. 3-51. Load lines of 2 phase VR with the proposed control and inductor current sensing (Red: DUT1, Blue: DUT1, Green: DUT3).



a. IL1, IL2 and Io



b. at light load



c. at full load

Fig. 3-52. Current sharing of 2 phase VR with the proposed control and inductor current sensing (Red: Io, Pink: IL1, Green:IL2, Blue: Vo).

	Io = 0A		Io ≈ 40A	
	IL1	IL2	IL1	IL2
DUT1	<0.1A	<0.1A	19.30A	20.08A
DUT2	<0.1A	<0.1A	20.43A	20.02A
DUT3	<0.1A	<0.1A	19.79A	20.33A

Table 3-9. Summary of current sharing of 2 phase VR with the proposed control and inductor current sensing.

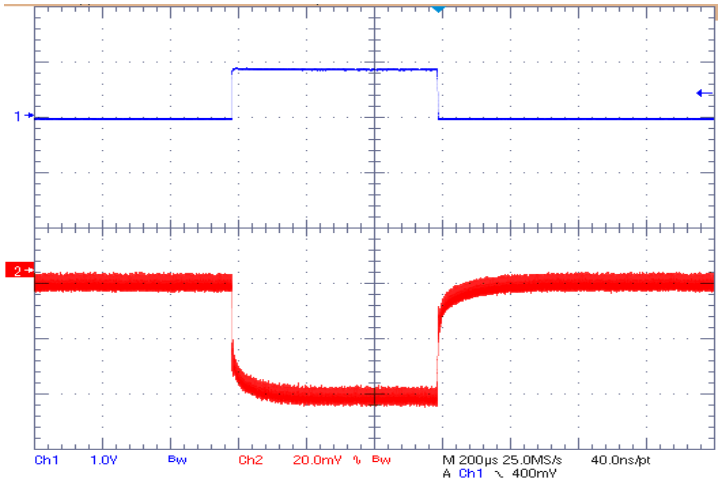
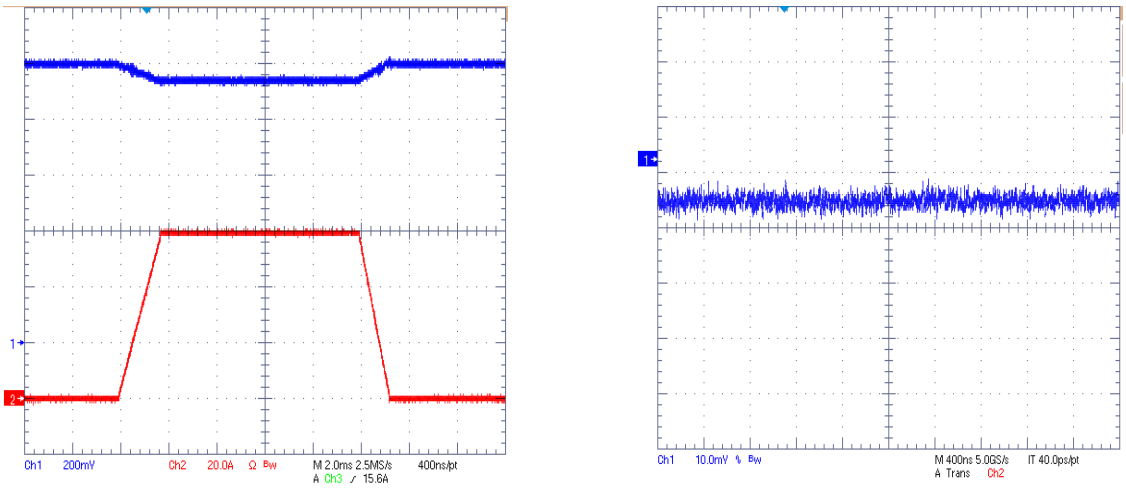


Fig. 3-53. AVP transient of 2 phase VR with the proposed control and inductor current sensing.

3.7.3.3. 3 Phase 60A Design with Resistor Current Sensing



a. Adaptive voltage position b. Output voltage ripple

Fig. 3-54. Voltage regulation of 3 phase VR with the proposed control and resistor current sensing (Red: Io, Blue: Vo).

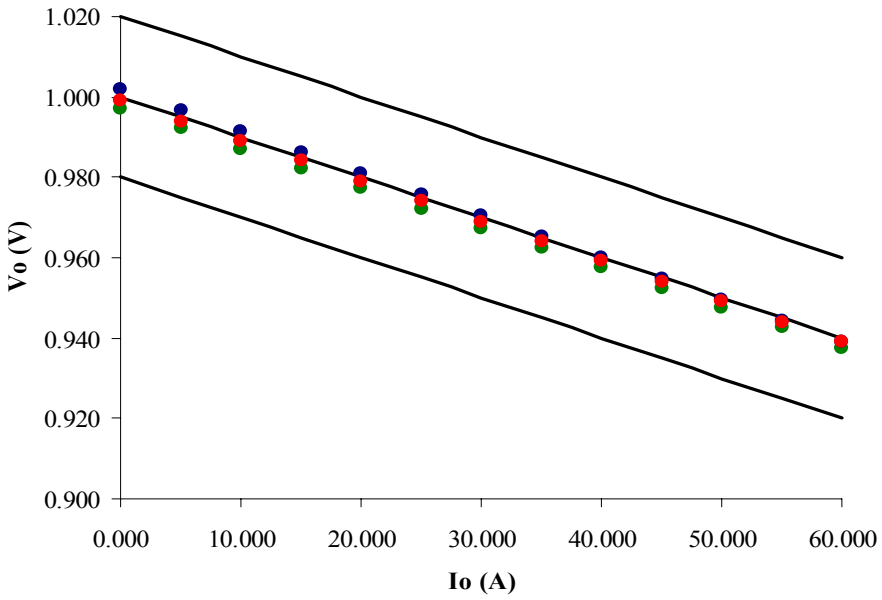
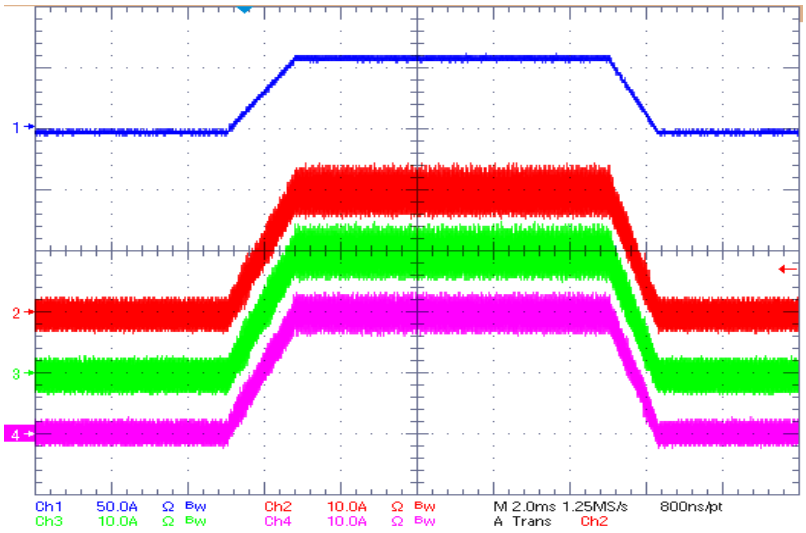
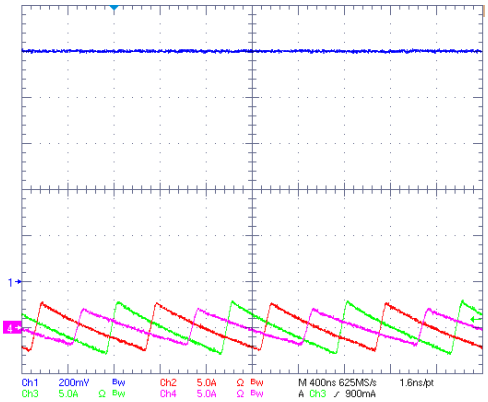


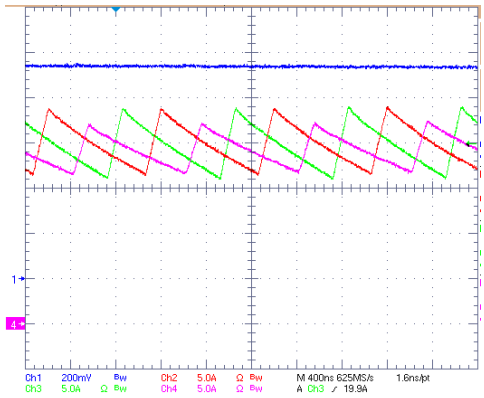
Fig. 3-55. Load lines of 3 phase VR with the proposed control and resistor current sensing (Red: DUT1, Blue: DUT1, Green: DUT3).



a. IL1, IL2 and Io



b. at light load



c. at full load

Fig. 3-56. Current sharing of 3 phase VR with the proposed control and resistor current sensing (Red: Io, Pink: IL1, Green:IL2, Blue: Vo).

	Io = 0A			Io ≈ 60A		
	IL1	IL2	IL3	IL1	IL2	IL2
DUT1	<0.1A	<0.1A	<0.1A	19.80A	19.97A	20.12A
DUT2	<0.1A	<0.1A	<0.1A	20.09A	20.41A	20.27A
DUT3	<0.1A	<0.1A	<0.1A	19.87A	19.81A	20.15A

Table 3-10. Summary of current sharing of 3 phase VR with the proposed control and resistor current sensing.

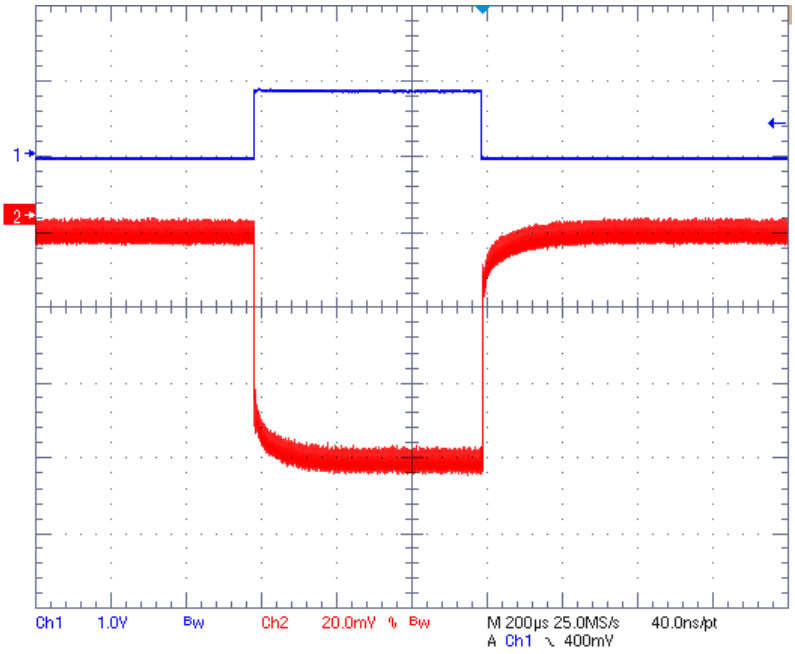
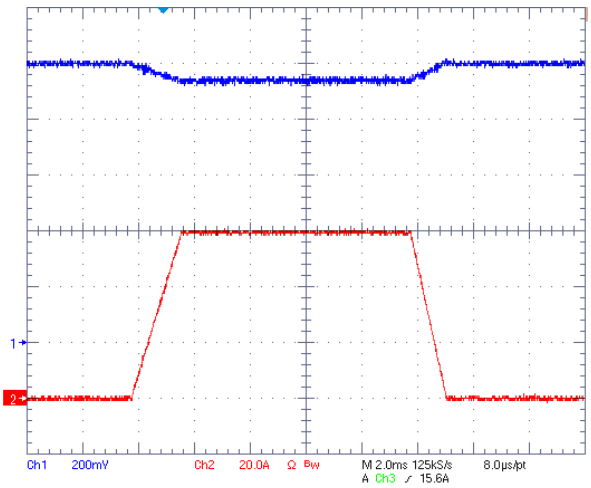
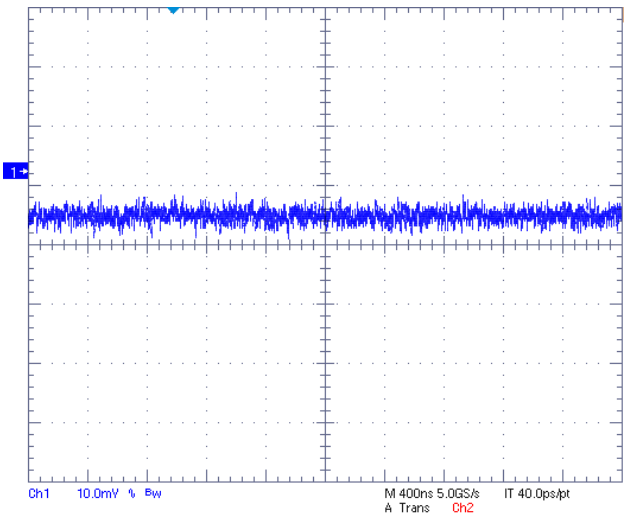


Fig. 3-57. AVP transient of 3 phase VR with the proposed control and resistor current sensing.

3.7.3.4. 3 Phase 60A Design with Inductor Current Sensing



a. Adaptive voltage position



b. Output voltage ripple

Fig. 3-58. Voltage regulation of 3 phase VR with the proposed control and inductor current sensing (Red: Io, Blue: Vo).

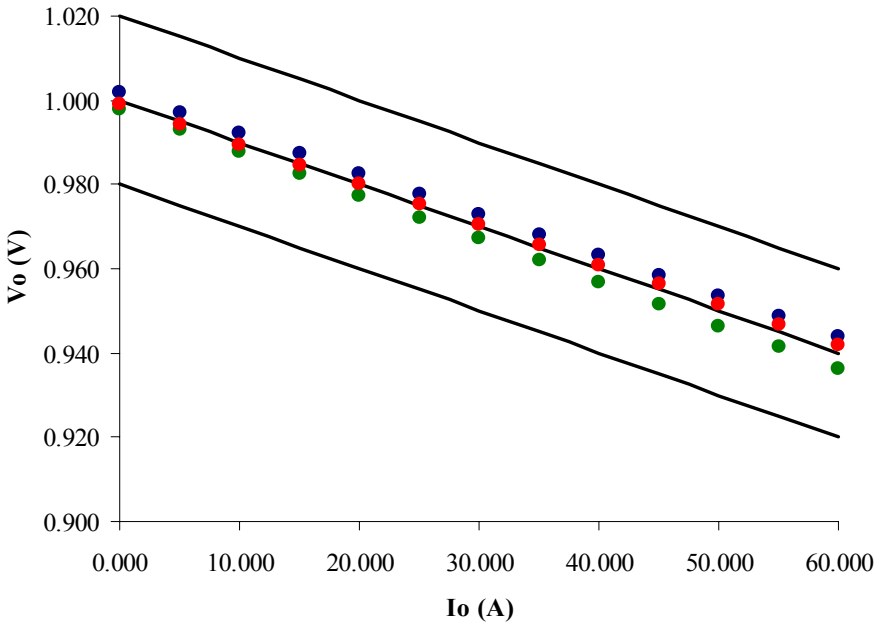
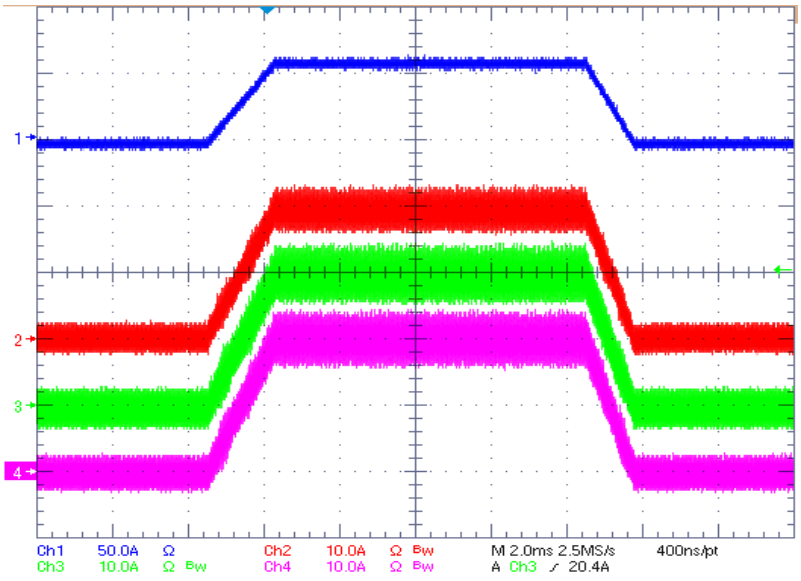
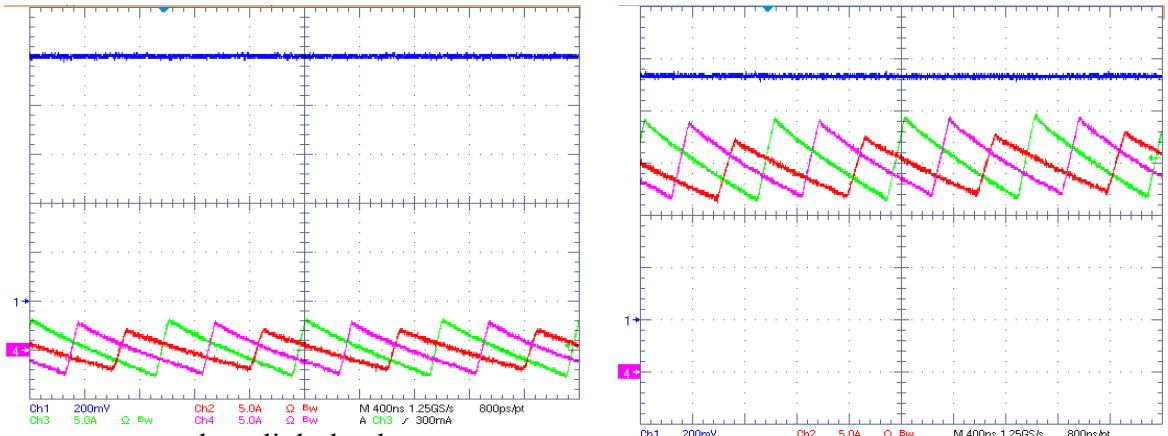


Fig. 3-59. Load lines of 3 phase VR with the proposed control and inductor current sensing (Red: DUT1, Blue: DUT1, Green: DUT3).



a. IL1, IL2 and Io



b. at light load

c. at full load

Fig. 3-60. Current sharing of 3 phase VR with the proposed control and inductor current sensing (Red: Io, Pink: IL1, Green:IL2, Blue: Vo).

	Io = 0A			Io ≈ 60A		
	IL1	IL2	IL3	IL1	IL2	IL2
DUT1	<0.1A	<0.1A	<0.1A	19.29A	20.08A	20.57A
DUT2	<0.1A	<0.1A	<0.1A	19.17A	20.99A	20.02A
DUT3	<0.1A	<0.1A	<0.1A	19.70A	19.01A	20.92A

Table 3-11. Summary of current sharing of 3 phase VR with the proposed control and inductor current sensing.

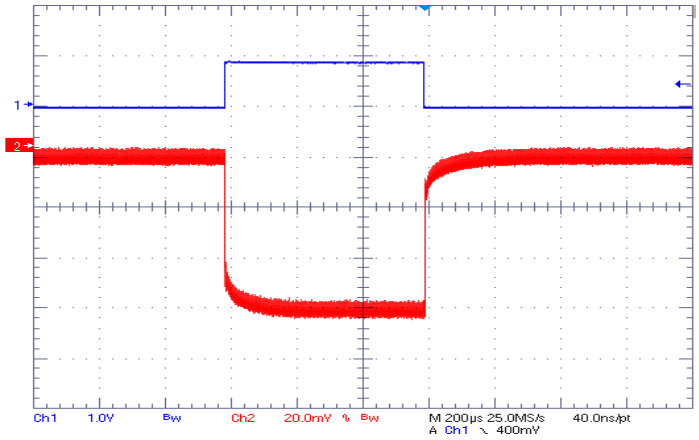


Fig. 3-61. AVP transient of 3 phase VR with the proposed control and inductor current sensing.

3.8. Summary of Chapter 3

This chapter first explains the objective of AVP and current sharing design specifications. Traditional AVP and current sharing schemes are systemically classified and reviewed. The limitation of traditional schemes to achieve scalable design leads to the exploration of the distributed control architecture.

Based on the active droop control for one channel converter, a "droop to each channel" scheme is developed to achieve scalable AVP and current sharing. The key concept of this scheme is to build a well-controlled system load line by a building well-controlled load line for each individual channel. By this way scalable AVP is achieved and current sharing is a free bonus. Current sharing performance can be further improved by tying each channel's voltage reference together.

The challenge is to prove it is not a challenge for this scheme to achieve good AVP and current sharing performance with nonideal components. Systemic tolerance analysis is provided in this chapter, which shows the proposed control scheme has better AVP tolerance band and comparable current sharing performance when compared with the traditional centralized control scheme. The tolerance formula derivation is verified by a case study with Monta-calco simulation.

A "discrete version" prototype using general Opamp, comparator, analog switch, digital gates as basic building components is developed according to the proposed control schemes and exclusive experiments are conducted. The first hand data demonstrate that the proposed control can meet future CPU power management's rigorous design specifications. Measurement with different sets of components further verifies the tolerance analysis.

Chapter 4. Improved Inductor Current Sensing

4.1. Reviews of Current Sensing Approaches in VR Applications

As mentioned in the above chapter, current sensing is necessary and important in the proposed control scheme as well as in the tradition control scheme. Accurate current sensing is a must to meet today's and future's rigorous VR design specifications. There are many current sensing approaches in VR products. And more are reported in academic papers. A short review of current sensing for VR applications is provided in this section.

4.4.1. By Resister

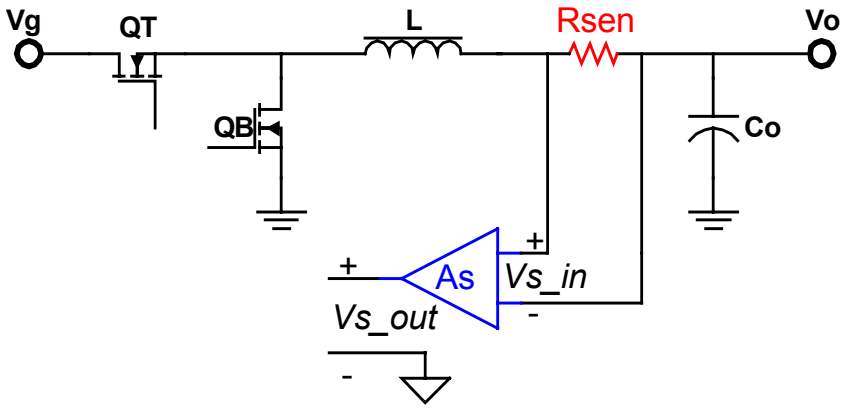


Fig. 4-1. Current sensing by sensing resistor.

Fig. 4-1 shows the resistor current sensing scheme. This technique is the most conventional way to sense current. The sensing element is a sensing resistor. Based on Ohm's low, if the value of the resistor is known, the voltage across the sensing resistor is determined by the current flowing through the resistor. Usually, this differential signal *Vs_in* is scaled and transferred to a single ended signal by an accurate gain block inside the VR controller.

This method obviously incurs a power loss in *Rsen*, which therefore reduces the efficiency of the DC-DC converter. To save the power loss, the sensing resistor can be put in series with the device QT to sense the current through the top device [D1]. However, this approach is prone to Signal-to-Noise issues due to the large switching voltage swing at the source side of the top device [D2].

The best place to put the sensing resistor from control point of view is in series with the output inductor on the load side, where the common mode voltage is minimum. This configuration provides the cleanest signal that can easily be processed with a differential amplifier, and be used to build well-controlled VR load line and to achieve accurate current sharing.

For accuracy, the voltage across the sensing resistor should be roughly 100mV at full load because of input inferred offsets and other practical limitations. If the full load current is 20A, 2W is dissipated in the sensing resistor.

4.4.2. By Inductor DCR

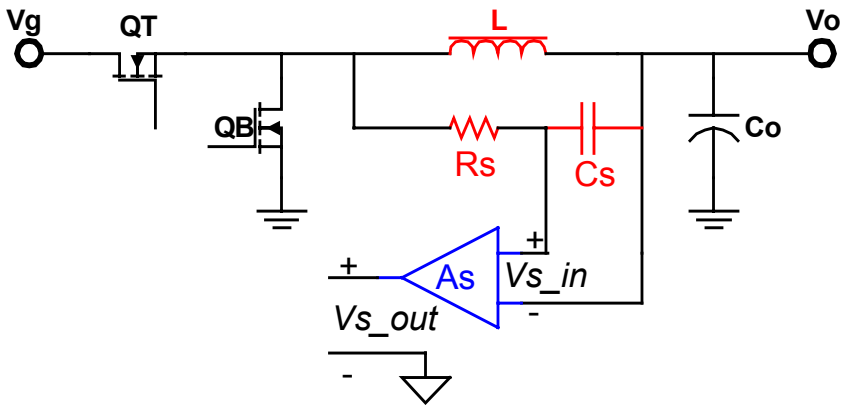


Fig. 4-2. Current sensing by Inductor DCR.

Fig. 4-2 shows the inductor current sensing scheme. This technique, reported in [D3] [D4], uses a simple low pass RC network to filter the voltage across the inductor and sense the current through the equivalent series resistance R_L of the inductor.

According to Fig. 4-2, we have

$$Vs\_in(s) = Vcs(s) = \frac{\frac{1}{s \cdot Cs}}{Rs + \frac{1}{s \cdot Cs}} \cdot (s \cdot L + R_L) \cdot i_L = R_L \cdot \frac{1 + s \cdot \frac{L}{R_L}}{1 + s \cdot Rs \cdot Cs} \cdot i_L$$

If we design $\frac{L}{R_L} = Rs \cdot Cs$, we have $Vs\_in = R_L \cdot i_L$. To use this technique, the values of L and R_L need to be known, and then Rs and Cs are chosen accordingly. The benefit of this scheme is no additional power loss due to the current sensing circuitry. And the accuracy of this scheme depends on the accuracy of inductor DCR and its temperature compensation.

4.4.3. By Power MOSFET On Resistance (Rdson)

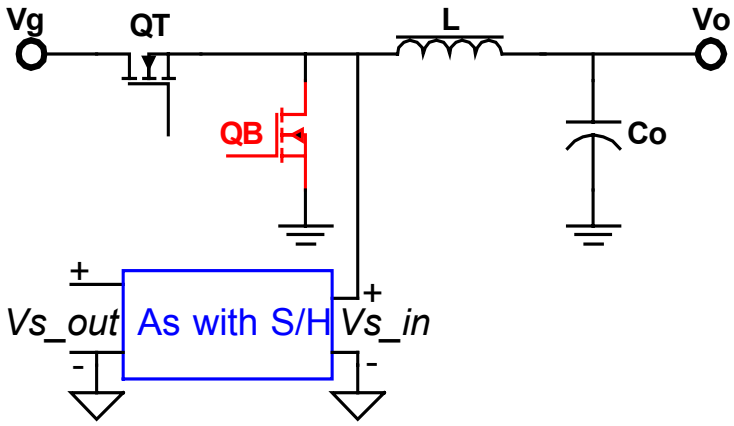


Fig. 4-3. Current sensing by power MOSFET on resistance.

Fig. 4-3 shows the Rdson current sensing scheme [D5]. MOSFETs act as resistors when they are "on" and are biased in the ohmic region. Assume small drain-source voltages are used, as is the case for MOSFETs when used as switches. Then the equivalent resistance of the device is $Rdson = \frac{1}{W \cdot \mu \cdot Cox \cdot (V_{GS} - V_T)}$, where μ is the mobility, Cox is the oxide capacitance, and V_T is the threshold voltage [D6]. Consequently, the switch current is determined by sensing the voltage across the drain and source of the MOSFET, provided that Rdson of the MOSFET is known. To sense this voltage, an accurate Gain stage with Sample & Hold is often adopted.

The benefit of this scheme is no additional power loss due to the current sensing circuitry. The main drawback of this technique is low accuracy. The MOSFET on resistance is inherently nonlinear. The Rdson of the MOSFET (on-chip or discrete) usually has significant variation because of μCox and V_T, not to mention how it varies with temperature.

4.4.4. By Sensing FET

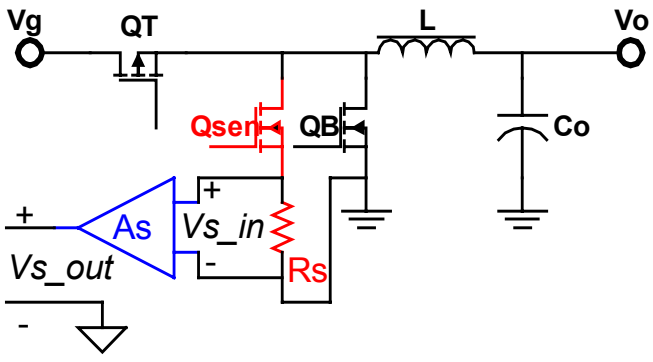


Fig. 4-4. Current sensing by sensing FET.

Fig. 4-4 shows the current sensing scheme by sensing MOSFET (sensing FET) [D7]~[D12]. Its operation is based on the matched device principle that is so commonly used in integrated circuits. Like integrated circuit transistors, the on resistance of individual source cells in a power MOSFET tends to be well matched. Therefore, if several out of several thousand cells are connected to a separate sensing pin, a ratio between sensing section on resistance and power section on resistance is developed. Then, when the sensing device is turned on, current flow splits inversely with respect to the resistance of these two sections, and a ratio between sensing current and source current is established. When a signal level resistor *Rs* is connected in series with the sensing FET, a known fraction of load current is sampled without the insertion loss that is associated with sensing resistors in Fig. 4-1. As long as the sensing resistor is less than 10% of the mirror section's on resistance Rdson, the current that is sampled is approximately load current divided by the current mirror ratio or I_{LOAD}/n (n is the area ratio of power FET and sensing FET).

In Fig. 4-4, the width of the power MOSFET should be at least 100 times larger than the width of the sensing FET to guarantee that the consumed power in the sensing FET is low and quasi-lossless. However, as the width ratio of the main MOSFET and sensing FET increases, the accuracy of the circuit decreases because the matching accuracy of the FETs degrades.

The bandwidth of this technique is not good due to the "transformer effect" [D13] [D14]. Because of the large current ratio of power FET and sensing FET, even a low degree of coupling between power FET circuits and sensing FET circuits can induce a significant error. Especially during periods of high di/dt, a large spike should be expected

in the sensing output. To reduce the "transformer effect", proper layout schemes should be chosen to minimize mutual inductance between sensing FET and main MOSFET circuits.

There are many improved versions of current sensing schemes adopting sensing FET [D15] [D16]. Fig. 4-5 shows a popular version. By adopting an Opamp, the drain voltage of sensing FET and power FET is forced to be equal, which eliminates the current mirror non-ideality resulting from channel length modulation.

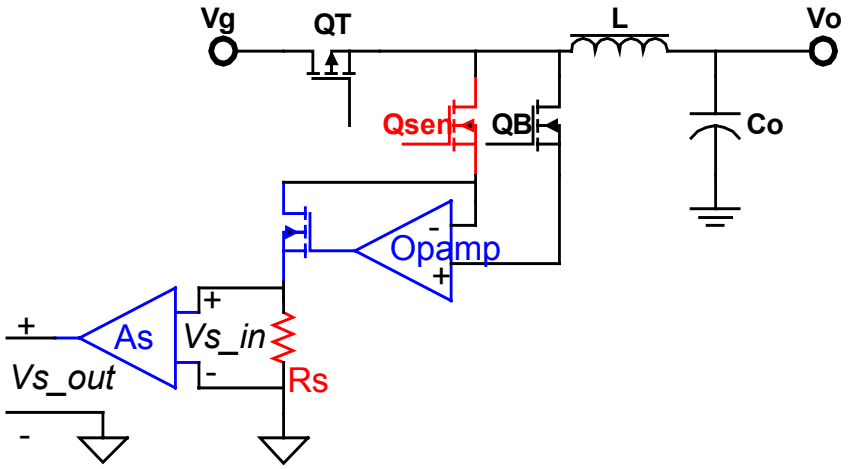


Fig. 4-5. A popular improved version of sensing FET scheme.

4.4.5. By Current Sensing Transformers

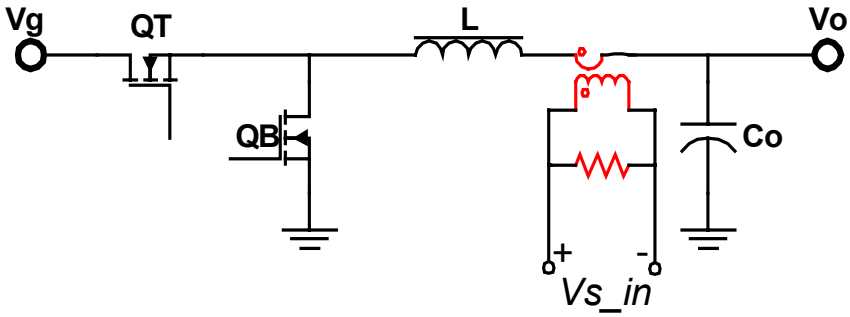


Fig. 4-6. Current sensing by sensing transformers.

Fig. 4-6 shows the current sensing scheme with current transformers. The use of current sensing transformers is common in high power systems. The idea is to sense a fraction of the high inductor current by using the mutual inductor properties of a transformer. The major drawbacks are increased cost and size and non-integrablity. The transformer cannot transfer the DC portion of current either, which makes this method inappropriate for over current protection.

4.4.6. By Midya's Scheme

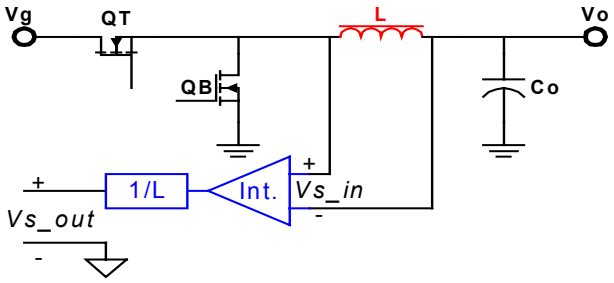


Fig. 4-7. Current sensing by Midya's scheme.

Fig. 4-7 shows Current sensing by Midya's scheme [D17]. It uses inductor voltage to measure inductor current. Since the voltage current relation of an inductor is $V_L=Ldi/dt$, the inductor current can be calculated by integrating the voltage over time. The value of L should also be known for this technique.

4.4.7. By Zhou's Scheme

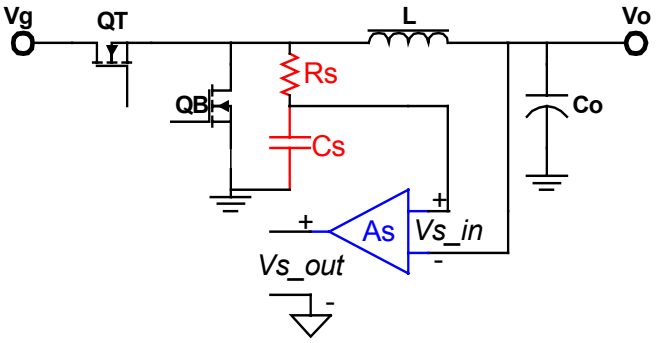


Fig. 4-8. Current sensing by Zhou's scheme.

Fig. 4-8 shows Current sensing by Zhou's scheme [D18]. This scheme uses a simple RC low pass filter at the junction of the switches of the converter. Since the average current through the resistor *R* is zero, the averaged value of *Vs_in* is:

$$\overline{Vs\_in} = \overline{Vo - Vcs} = R_L \cdot \overline{i_L}$$

If R_L is known, the output current can be determined. Sensing the current in this method depends only on R_L, and not on the switch parasitic resistor or the values of *Rs* and *Cs*. This scheme is used mainly for load sharing of different phases in multiphase DC-DC converters [D19].

4.4.8. By Forghani-zadeh's Scheme

All the discussed current sensing methods, except for the sensing FET technique, depend on knowing the values of discrete elements such as inductor, sensing resistor or MOSFET's Rdson. In a lossless current sensing technique, only node voltages are sensed and the value of the current in a branch is estimated using the values of passive elements (i.e., $V = R \cdot i, i = C \cdot dV/dt$ and $V = \left(\int CdV\right)/L$). In a custom discrete design, the values of external components are known and the current sensing technique can be adjusted before mass production. On the other hand, if a current sensing scheme is designed for a general purpose controller, where the end user can select inductors, capacitors, and switches from a specified range, the IC designer is incognizant of the values of the external components. Hence, current sensing techniques are best designed if they are independent of external component values. To solve this problem, the circuit shown in Fig. 4-9 is proposed in [D20], where the value of the inductor is measured and stored during startup and the voltages are sensed during normal operation to determine the

current. Just before startup, the power MOSFETs are forced off and switches S1 and S2 are “on”.

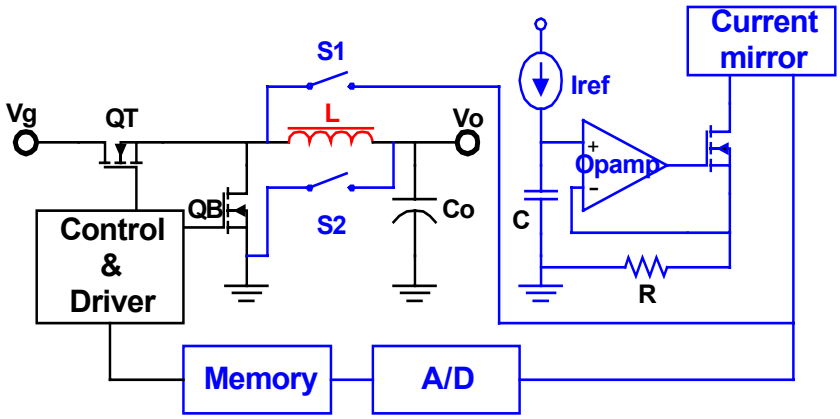


Fig. 4-9. Current sensing by Forghani-zadeh’s scheme.

Constant current source *Iref* charges capacitor C during that time, creating a linear voltage ramp, which is turned into a linear current ramp by the Opamp. The voltage at the positive port of the Opamp is $Vc(t) = \frac{1}{C}\int I_{ref}\,dt = \frac{I_{ref}\cdot t}{C}$, where t is time. The Opamp, along with the negative feedback, forces the negative port of the Opamp to be equal to the positive port; thus, the current forced is a ramp $i_L(t) = \frac{Vc}{R} = \frac{I_{ref}\cdot t}{R\cdot C}$. Therefore, the voltage across the inductor is $V_L(t) = L\cdot\frac{di_L}{dt} = \frac{L\cdot I_{ref}}{R\cdot C}$, where *Iref* is a function of the reference voltage and another integrated resistor. The voltage given by the above equation is a constant voltage across a 1μH inductor. This measurement technique boosts the observer technique accuracy especially when the inductor value is not known.

4.4.8. Summary of Current Sensing

Selecting a proper current sensing method depends on the DC-DC converter control scheme. If voltage mode control is used, current sensing is only needed for overload current protection. Therefore a simple, not very accurate but lossless method, like Rdson current sensing, is sufficient. If current mode control or mode hopping (for high efficiency) is used, more accurate algorithms may be necessary. The traditional series resistor with inductor technique can be used when power dissipation is not critical, which is hardly the case for portable applications. For application like desktop computers, decreasing the power efficiency by about 5% is not critical. The majority of commercial current mode controller solutions for desktop computers use a sensing resistor. Rdson sensing is the other dominant technique, which is used even in current-mode controllers in commercial products, but its accuracy is poor. Another widely used technique is inductor current sensing. Table 4-1 summarizes the advantages and disadvantages of the different current-sensing techniques explored.

Current sensing approaches	Advantages	Disadvantages
By sensing Resistor	High accuracy (1%)	High power loss
By Inductor DCR	Lossless High accuracy (5%)	Known L (roughly value) and R_L, High number of discrete elements
By Rdson	Lossless	Low accuracy
By sensing FET	Quasi-lossless Integratable High accuracy (2%)	Matching issues, Low bandwidth
By sensing transformer	Lossless	High cost, large size, High number of discrete elements
By Midya's scheme	Lossless	Known L (accurate value), Fast integrator needed
By Zhou's scheme	Lossless	Known R_L, Extreme low bandwidth
By Forghani-zadeh's scheme	Lossless No power stage information needed	Complex, expensive block like A/D, memory needed

Table 4-1. Summary of current sensing approaches.

4.2. Issues of Traditional Inductor Current Sensing Schemes

In table 4-1, resistor current sensing, inductor current sensing and Rdson current sensing are adopted in commercial VR products. Sensing FET approach can also be found in some VR power ICs [D21]. Other approaches are mainly reported in academic paper. Their applications in real VR products are limited due to the cost issues or implementation difficulties.

Because of the rigorous design specifications of VR load line, Intel does not suggest Rdson current sensing. Therefore, only resistor current sensing and inductor current sensing are widely used in VR products. And the inductor current sensing becomes more and more popular due to the 0 power loss and acceptable sensing accuracy.

The inductor current sensing scheme shown in Fig. 4-2 can be seen as a low pass filter composed of two cascaded stages. Fig. 4-10 shows such a view:

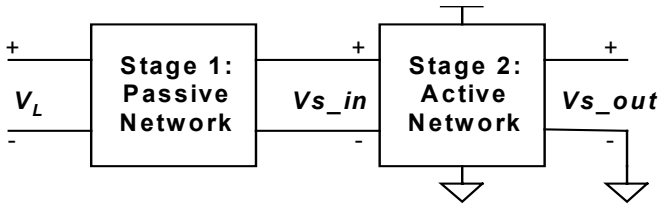


Fig. 4-10. Inductor current sensing from signal processing point of view.

The concept of inductor current sensing is to get inductor current information by processing inductor voltage signal V_L. To do the signal processing, the first stage is a passive RC network, which achieves a differential signal proportional to inductor current *Vs_in*. The second stage is an active network, which transfers the differential signal *Vs_in* to a single ended signal *Vs_out* used by other circuitry of the VR controller. Fig. 4-11 shows the key waveforms of this scheme.

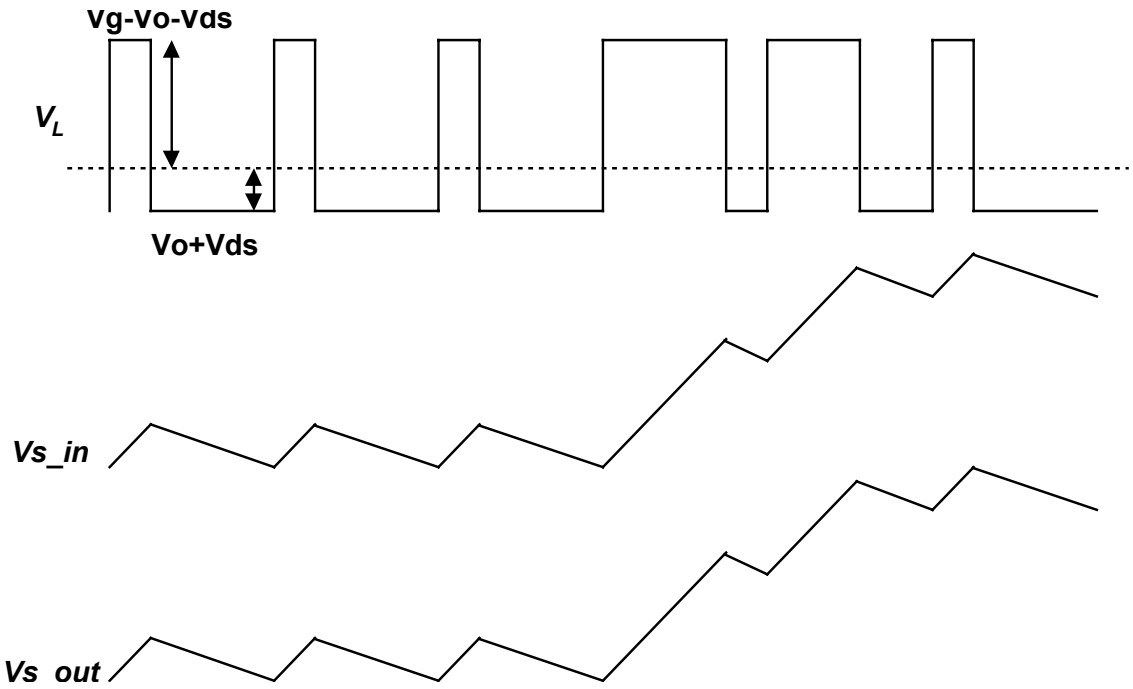


Fig. 4-11. Key waveforms of inductor current sensing.

The concept and waveforms seem clear and easy to be implemented, but there are still some issues of today's inductor current sensing approach.

4.2.1. Input Impedance of the Differential Amplifier

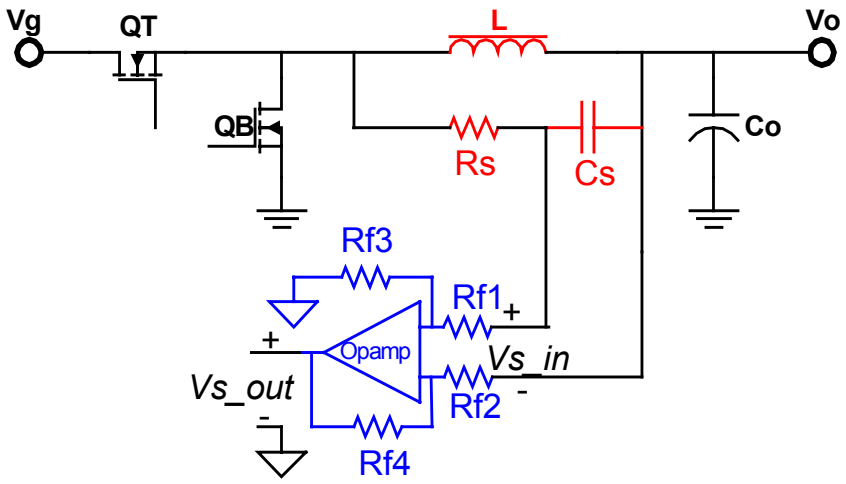


Fig. 4-12. Impact of differential amplifier's input impedance on inductor current sensing.

Fig. 4-12 is the redraw of Fig. 4-2, in which the differential amplifier block *As* is implemented by an Opamp and feedback resistors. Usually, design *Rf1=Rf2=R1* and *Rf3=Rf4=R2*. Then, the input impedance of the block *As* is $Rin = 2R1$. Then:

$$Vs\_in(s) = Vcs(s) = \frac{\frac{1}{s \cdot Cs} // Rin}{Rs + \left(\frac{1}{s \cdot Cs} // Rin\right)} \cdot (s \cdot L + R_L) \cdot i_L$$

$$= \left(\frac{Rs}{Rs + Rin}\right) \cdot R_L \cdot \frac{1 + s \cdot \frac{L}{R_L}}{1 + s \cdot (Rs // Rin) \cdot Cs} \cdot i_L$$

If we still design *Rs* and *Cs* according to $L / R_L = Rs \cdot Cs$, a large error will be introduced to the current sensing output. If we design according to $L / R_L = (Rs // Rin) \cdot Cs$, *Vin_in* will be $\left(\frac{Rs}{Rs + Rin}\right) \cdot R_L \cdot i_L$, which is even smaller than $R_L \cdot i_L$ and may cause Signal-to-Noise ratio issues as described in next section. In reality, even the matching of *Rf1~Rf4* can be guaranteed, the absolute values of *Rf1~Rf4* can vary as much as 30%. Therefore the value of *Rin* is difficult to be estimated. And it is impractical to design according to $L / R_L = (Rs // Rin) \cdot Cs$.

To achieve accurate current sensing, the input impedance of the *As* block should be maximized. Fig. 4-13 shows a popular improved version of the differential amplifier.

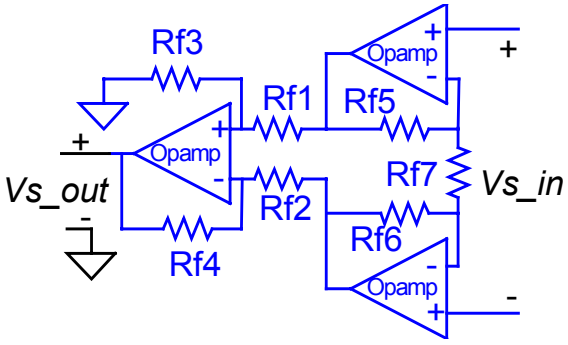


Fig. 4-13. An improved version of differential amplifier.

However, the above circuit is expensive for manufacture because of the number of operational amplifiers and resistors required. The silicon surface area for forming the circuit on integrated circuits is not negligible.

4.2.2. Signal-to-Noise Issues with Small Inductors

Even if the input impedance of the differential amplifier is large enough, there is another issue ----Noise.

For an analog signal processing circuitry, there are many noise sources. The noise can be caused by the small current and voltage fluctuations that are generated within the circuitry itself. Or it can be caused by unintentional pickup of extraneous signals. The noise produced by the semiconductor circuitry includes shot noise, thermal noise, flicker noise, burst noise and avalanche noise etc. [D22] The amplitude of these noise is in μV (rms) or nA (rms) range. They are the major concerns of RF analog circuits. However, in switching DC-DC converters, the noise pickup of extraneous signals is more serious, which may be several orders larger than the RF noise.

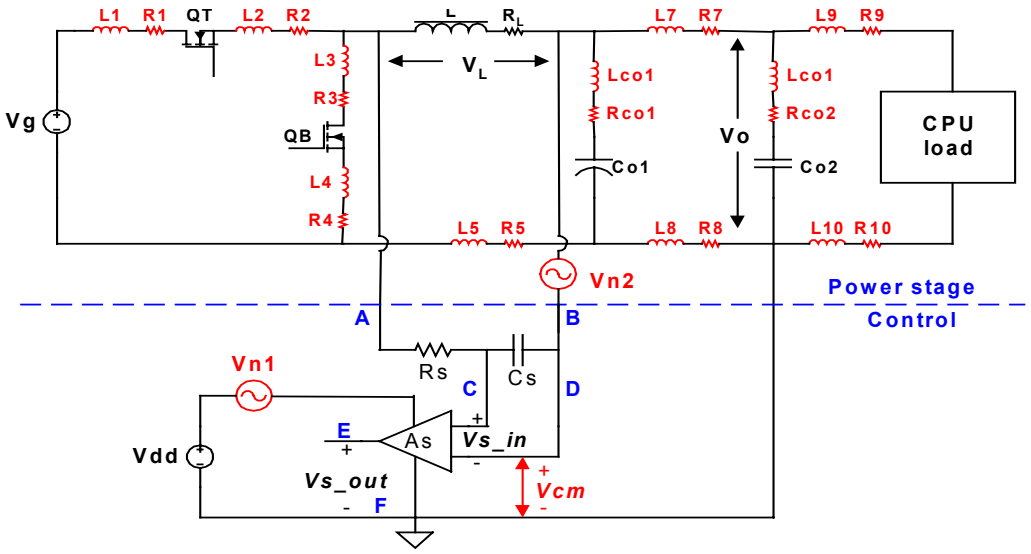


Fig. 4-14. Major noise sources for the inductor current sensing.

Fig. 4-14 tries to show the unintentional pickup of extraneous signals with the inductor current sensing scheme. There are three major sources for the inductor current sensing scheme. The first noise source is the common mode voltage of the differential amplifier *Vcm*. As shown in the above figure, *Vcm* equals to the sum of the output voltage *Vo* and the voltage across the parasitics *R7* and *L7*. As the instance when the switches are being turned on or off, the voltage across the parasitic may reach to volt level. For the active circuitry, the CMRR is limited. The voltage *Vcm* will not be attenuated close to 0 at the output, especially for the high frequency part of the common mode signal.

The second noise source is *Vn1*, the voltage fluctuation of power supply Vdd. The decoupling of Vdd is far from ideal in real implementation. Due to the limited PSRR of the active circuitry, the fluctuation of Vdd may introduce the fluctuation at output, especially for high frequency Vdd fluctuation.

The third noise source is Vn2, the differential signal pickup from the power inductor to the input port of the current sensing scheme. This noise pickup can be largely reduced by proper layout of the current sensing traces from the power inductor to the points A and B [D23]. The two sensing traces need to be close to each other to reduce the loop area.

Fig. 4-15 shows a simplified noise model of inductor current sensing. The noise source Vn2 is ignored in this figure.

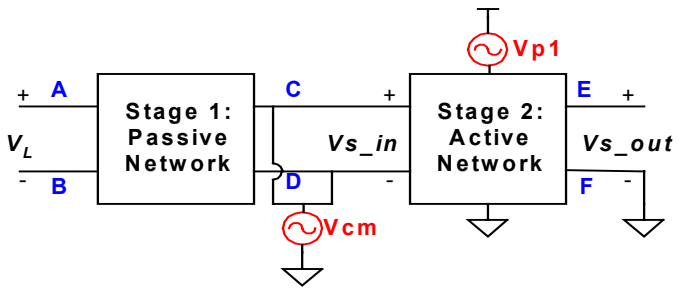


Fig. 4-15. Simplified noise model of inductor current sensing.

As shown above, the first stage of inductor current sensing is a passive network. The passive network has no PSRR issue because no power supply exists. And the CMRR of the passive network is close to ideal circuit. Therefore, the common mode voltage and the voltage fluctuation of Vdd do not cause output deviation of the first stage. However, these noise sources introduce output error in the second stage due to the limited CMRR and PSRR of the active circuitry. The input amplitude of the active circuit should be maintained beyond some value to guarantee an acceptable signal quality at output. It is difficult to calculate the noise floor, which is related to many parameters from component characteristics to their layout. However, based on industry practice, the input signal to the active circuitry *Vs_in* needs to be over 20mV at full load [D24].

As explained in section 4.1.2, for the current sensing scheme, as shown in Fig. 4-2, if we design the time constant of the RC network equal to the inductor time constant, we always have $Vs\_in = R_L \cdot i_L$. When R_L is too small, *Vs_in* can be too small to maintain a good enough Signal-to-Noise ratio for the active circuitry of the sensing scheme. Particularly in high frequency application, small inductors are often adopted to take advantage of the possible wide control bandwidth. Small inductor also means small winding DCR. For example, the typical value of R_L for a 50nH/20A inductor is about 0.5mΩ. The amplitude of *Vs_in* is just 10mV when the inductor current is 20A, which is too small to be handled by a normal active circuitry working under the noisy environment, as shown in Fig. 4-14. New sensing schemes need to be developed for the application with small inductors.

Fig. 4-16 shows an approach trying to increase the input signal amplitude for the active stage of the sensing scheme [D24]. Fig. 4-17 shows the key waveforms.

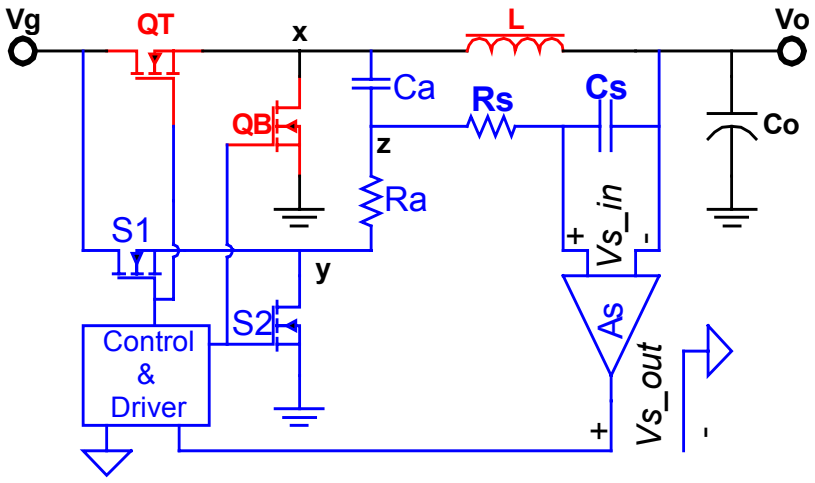


Fig. 4-16. Semtech's current sensing scheme.

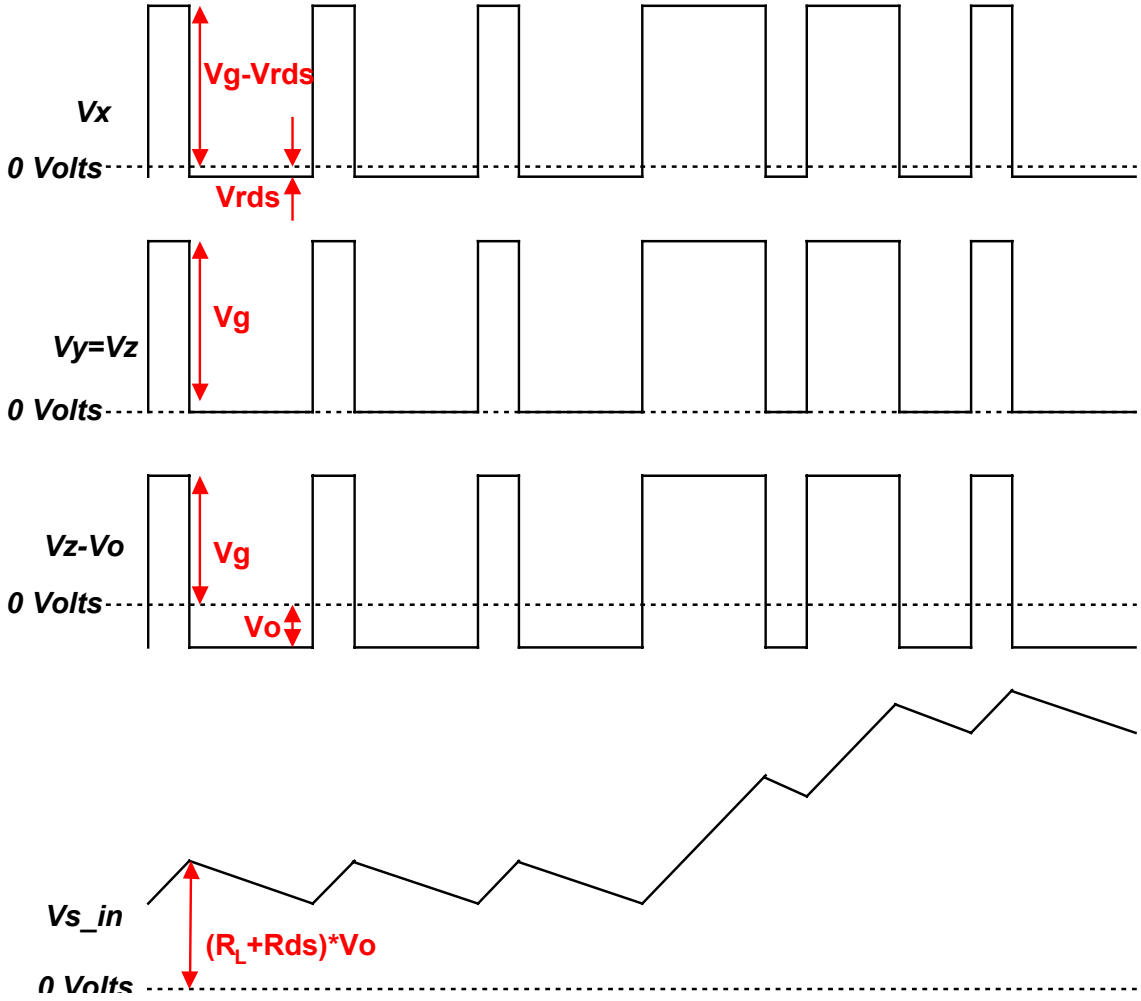


Fig. 4-17. Key waveforms of Semtech's current sensing scheme.

In the above scheme, S1 and S2 are signal level MOSFETs that are hundreds or thousands times smaller than the power MOSFETs QT and QB. S1 and QT turn on and off simultaneously; S2 and QB turn on and off simultaneously too. When S1 and QT turn on, $Vx = Vg - Vrds$, $Vy = Vg$, and $Vz = Vy$. When S2 and QB turn on, $Vx = -Vrds$, $Vy = 0$, and $Vz = Vy$. By this way, $Vz(s) - Vo(s) = i_L \cdot \left(R_L + R_{ds} + s \cdot L\right)$. Then,

$$Vs\_in(s) = \frac{\frac{1}{s \cdot Cs}}{Rs + \frac{1}{s \cdot Cs}} \cdot \left[Vz(s) - Vo(s)\right] = \left(R_L + R_{ds}\right) \cdot \frac{1 + s \cdot \frac{L}{R_L + R_{ds}}}{1 + s \cdot Rs \cdot Cs} \cdot i_L .$$

If we design $Rs \cdot Cs = \frac{L}{R_L + R_{ds}}$, we have $Vs\_in = \left(R_L + R_{ds}\right) \cdot i_L$, and the amplitude of *Vs_in* is much larger than that of the original inductor current sensing.

In Fig. 4-16, capacitor *Ca* and resistor *Ra* are operative during the dead time of the power cycle to provide a low pass filter to block any high frequency transient signal from affecting the current sensing signal and to synchronize operation of the power phase node x and signal phase node y.

However, this scheme assumes the on resistance of the top power MOSFET and the bottom power MOSFET is the same. In reality, Rds_bot is much smaller than Rds_top. The scheme is expensive for implementation. It needs specially designed driver, which integrates the S1 and S2. And more discrete external components are needed in the scheme than in the original inductor current sensing scheme. The bigger issue is that it introduces the tolerance of *Rdson* in the sensing output. According to the discussion in section 4.1, the *Rdson* of power MOSFET has as much as 30% variation. This scheme may not meet future's VR design specifications.

4.3. A Novel Current Sensing Scheme Adopting a V/I Converter

4.3.1 Scheme Development

As discussed above, inductor current sensing becomes more and more popular due to the 0 power loss and acceptable sensing accuracy. However, there are still some issues of today's inductor current sensing approach. One issue is the input impedance of the differential amplifier has big impact on the current sensing output. A more important issue is the input signal amplitude could be too small to be handled by normal analogy circuitry when the inductor DCR is small.

To overcome the above issues, a novel inductor current sensing scheme adopting a V/I converter is developed. Fig. 4-18 shows the proposed current sensing scheme. The noise source and the power stage parasitic are also shown. Fig. 4-19 shows the simplified noise model of the proposed current sensing scheme.

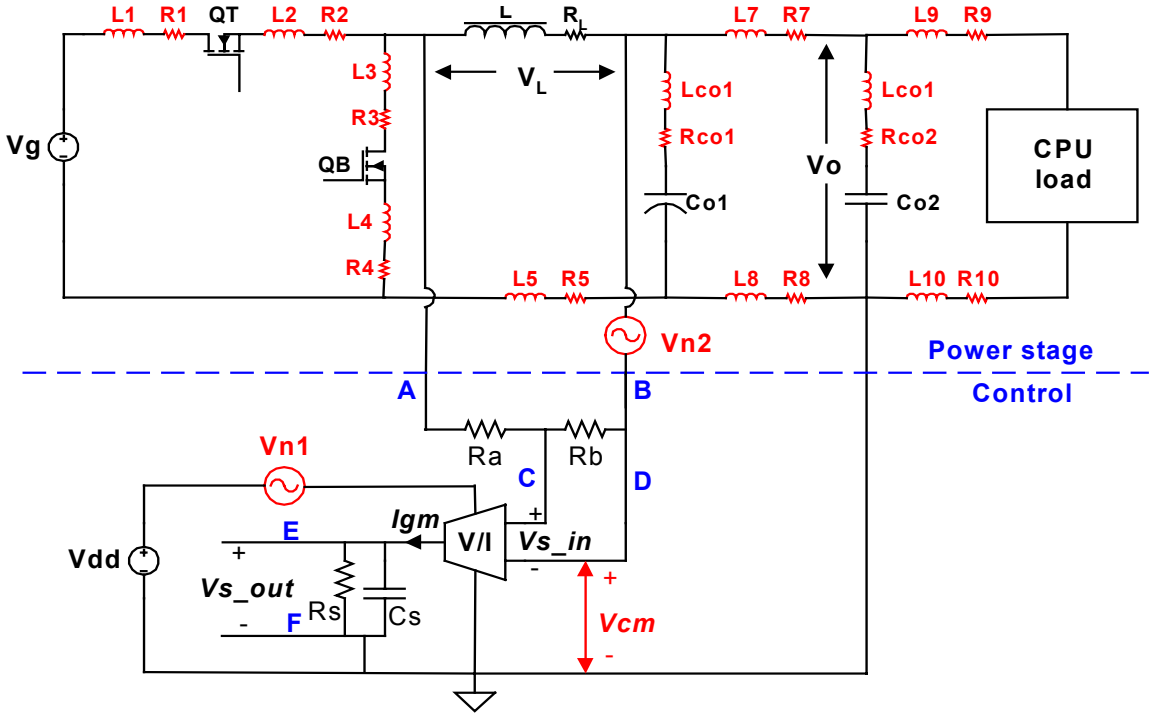


Fig. 4-18. Proposed current sensing scheme adopting a V/I converter.

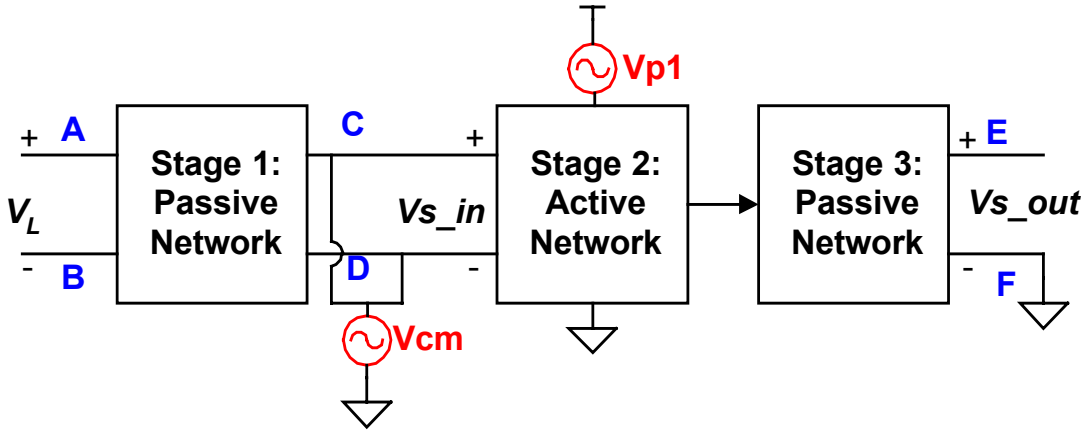


Fig. 4-19. Simplified noise model of proposed current sensing scheme.

The concept of this scheme is to put the active network before the passive RC network, so that the input of the active network *Vs_in* can be a large signal. Therefore, the Signal-to-Noise ratio of the active network stage can be dramatically improved.

As shown in Fig. 4-18, this scheme can be seen as three stages. The first stage is a voltage divider composed of two resistors *Ra* and *Rb*. The divider scales the V_L and makes it small enough to be processed by the active circuitry with 5V Vdd, and big enough to be noise insensitive. The second stage of the scheme is an accurate V/I converter, which transfers the scaled inductor voltage *Vs_in* to a current waveform *Igm*. The third stage is a passive RC network. The current *Igm* charges and discharges the RC network to restore the shape of inductor current waveform. By this way, we can handle a very small inductor as long as the DCR is well controlled. The key of this approach is the accurate V/I converter with a large dynamic range.

Fig. 4-20 shows the key waveforms of the proposed current sensing scheme. As we can see, the input signal to the active circuitry *Vs_in* can be an order larger than that of the original inductor current sensing scheme.

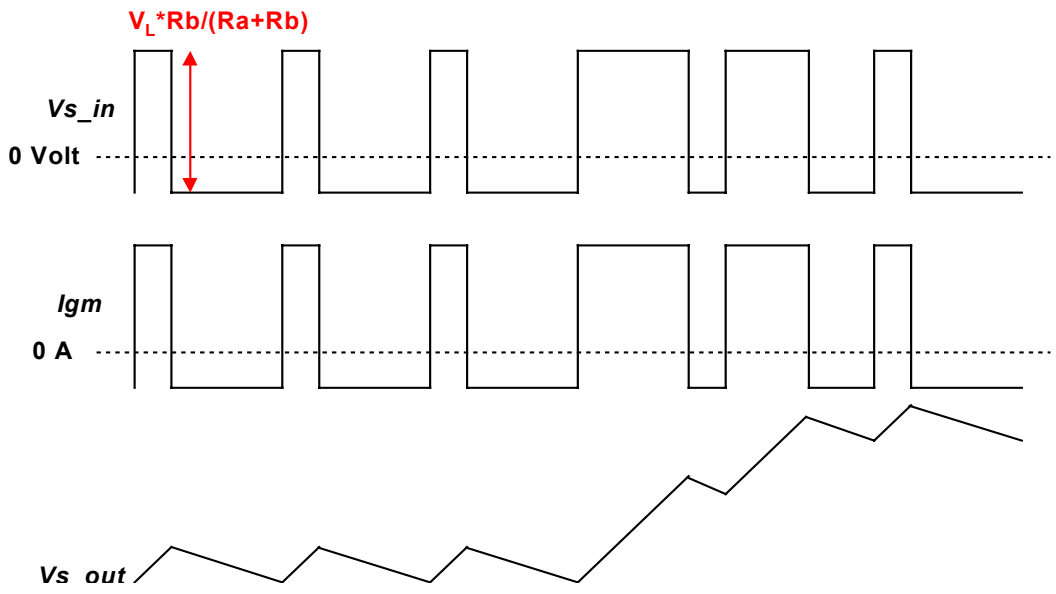


Fig. 4-20. Key waveforms of the proposed current sensing scheme.

From Figures 4-19 and 4-20, it is easy to derive

$$Vs\_out(s) = \frac{Rs \cdot \left(\frac{1}{s \cdot Cs}\right)}{Rs + \frac{1}{s \cdot Cs}} \cdot GM \cdot Vin\_in(s) = \frac{Rs}{1 + s \cdot Rs \cdot Cs} \cdot GM \cdot \frac{Rb}{Ra + Rb} \cdot \left(R_L + s \cdot L\right) \cdot i_L$$

$$= \frac{Rb}{Ra + Rb} \cdot Rs \cdot GM \cdot R_L \cdot \frac{1 + s \cdot \frac{L}{R_L}}{1 + s \cdot Rs \cdot Cs} \cdot i_L$$

where GM is the transconductance of the V/I converter. If we design $Rs \cdot Cs = \frac{L}{R_L}$, we'll have $Vs\_out(s) = \frac{Rb}{Ra + Rb} \cdot Rs \cdot GM \cdot R_L \cdot i_L$.

In the implementation, Ra and Rb can be integrated in the controller because only the ratio of their resistance needs to be accurate. After Ra, Rb, GM and R_L are fixed, the current sensing gain can be flexible by selection of Rs.

In the above derivation, the bandwidth of the V/I converter is infinite. The finite bandwidth of the V/I converter introduces a pole in Vs_out, which determines the bandwidth of the whole current sensing scheme.

4.3.2 Simulation Results

Fig. 4-21 shows the simulation results with the proposed current sensing scheme. The V/I converter in the simulation is a voltage controlled current source with 1MHzbandwidth.

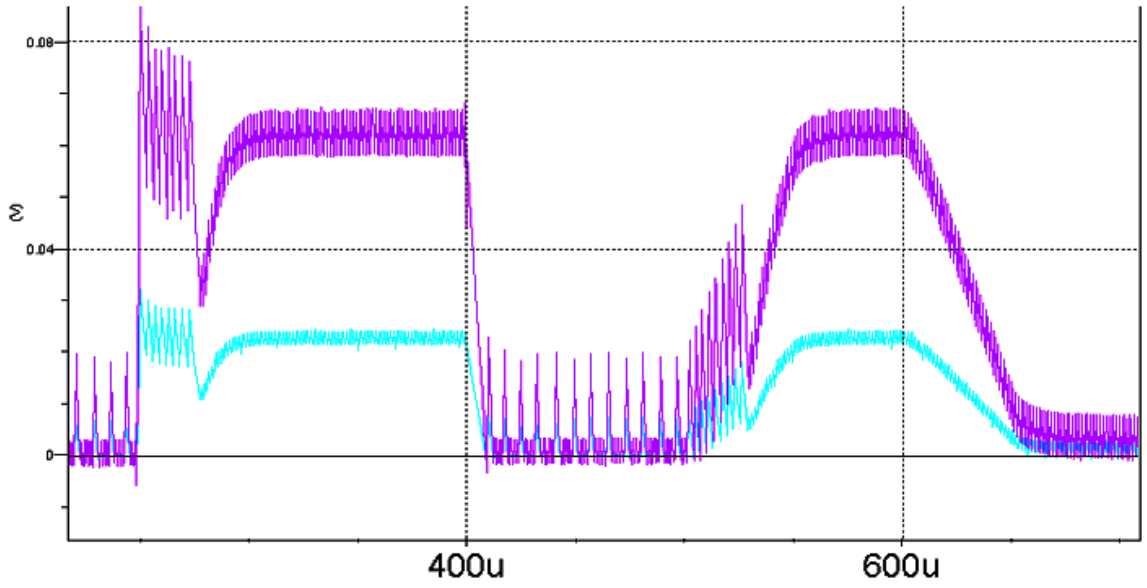


Fig. 4-21. Simulation results with the proposed current sensing scheme.

In Fig. 4-21, the purple curve is the inductor current, the bright blue curve is the output signal of the current sensing scheme. As we can see, the current sensing output follows the inductor current waveform very well, no matter whether the converter is in steady state or transient, at CCM or DCM.

4.3.3 Hardware Verification

To verify the proposed current sensing scheme in hardware, the V/I converter is implemented with available commercial operational amplifiers according to the circuit shown in Fig. 22. This circuit is based on the configuration of the improved Howland

current pump [D25]. Six Opamps and many resistors are used in this circuit. And a voltage bias *Vb* is produced to balance the offset of these Opamps.

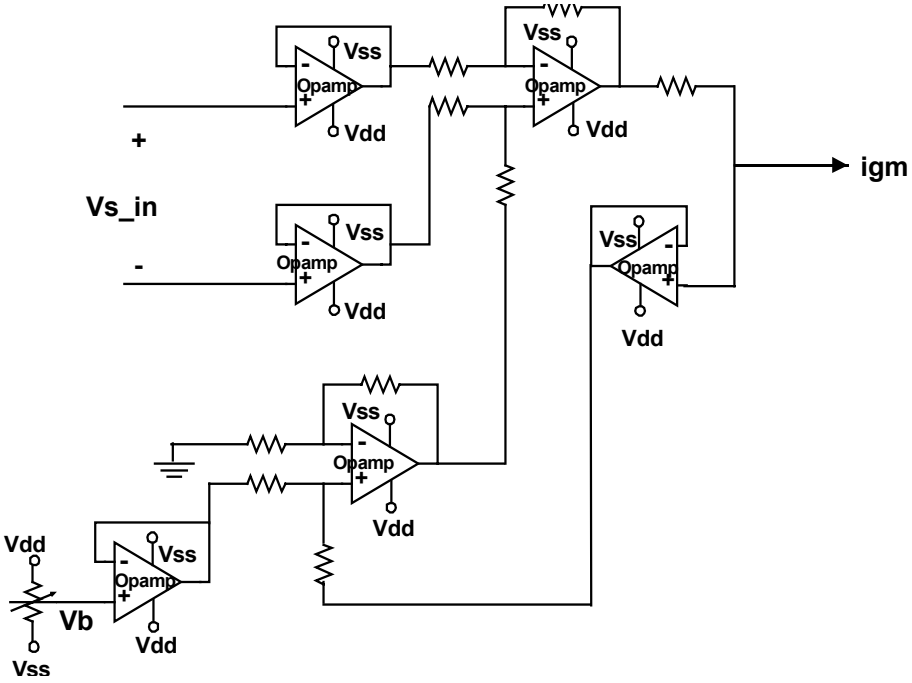
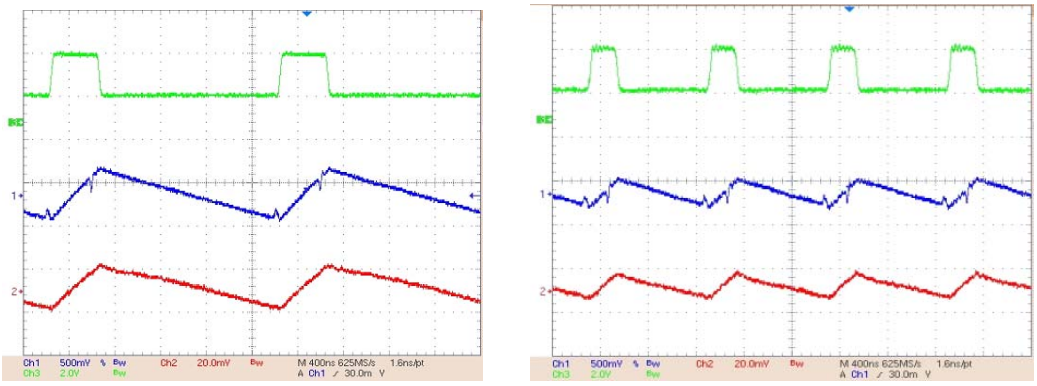


Fig. 4-22. Implementation of V/I converter with Opamps.

Fig. 4-23 shows the hardware measurements results.



a. Fs=500KHZ b. Fs=1MHz

Fig. 4-23. Proposed current sensing scheme hardware testing results.

* Green: switching clock; Blue: the output of proposed sensing scheme;
  Red: inductor current measurement with current probe.
  The inductor used is 200nH / 0.45 mΩ DCR.

4.4 The Key Block ---- A Monolithic Accurate Gm Amplifier

4.4.1 The Basic Design Requirements of the V/I Converter

An accurate V/I converter is the key building block of the proposed current sensing scheme. In section 4.3.3, the V/I converter is implemented using Opamps with the improved Howland current pump configuration. However, this circuit is expensive for manufacture because of the number of Opamps and resistors required. The silicon surface area for forming the circuit on integrated circuits is huge and special trimming is needed to get an accurate transconductance (Gm) value for the V/I conversion. The offset of Opamps also needs to be tuned using external components. More than that, the Howland current pump configuration has both positive and negative feedbacks, which may lead to oscillation under some operation conditions [D26]. A more concise implementation of the V/I converter is necessary to make the proposed current sensing scheme really practical.

Although an ideal V/I conversion cannot be achieved in real analog design, the V/I converter needs to meet the following requirements used in the proposed current sensing scheme.

1) Accurate and large Gm value (e.g. 1mA/V ±3%).

The accuracy of the V/I converter's Gm value has direct impact on the accuracy of the current sensing gain. As mentioned in section 3.3.3, the budget for the current scaling inside the chip is only 3%. The Gm value needs to be large, usually around mA/V, to facilitate the selection of resistor *Rs* and to achieve the target current sensing gain.

2) Large input dynamic range and common mode range.

(e.g. $-0.5V < Vdif < 0.5V$, $0.5V < Vcom < 3V$)

Since the V/I converter needs to process a large signal to overcome the noise issues, a large input dynamic range is a necessary. And the input of the V/I converter can be tied to very low voltage node, for example, the VR output node.

3) Small output offset current (e.g. < 0.1 μA).

The impact of the V/I converter's output offset current on the accuracy of current sensing depends on the load of the V/I converter. For example, if the load of the V/I converter is 10KΩ, a 1μA offset current may introduce 10mV current sensing output error. Usually the load of the V/I converter is small than 10KΩ, and the maximum acceptable current sensing output error is 1mV. Therefore, the output offset current of the V/I converter needs to be limited within ±0.1 μA.

4) High input impedance (e.g. > 1MΩ).

As discussed in section 4.2.1, the limited input impedance of the V/I converter also has effect on the current sensing output accuracy.

5) High bandwidth (e.g. > 1MHz).

The current sensing bandwidth is limited by the bandwidth of the V/I converter. To build a fast current loop for VR application, a large bandwidth V/I conversion is a must. However, super wide bandwidth is not necessary because the VR control bandwidth is limited by the switching frequency.

6) Low power consumption.

Power consumption is an important specification in today's analog market. Every *mA* counts. To make the V/I converter a general analog building block used in a DC-DC controller, low power consumption is an important design consideration.

4.4.2 The Limitations of the Basic OTA Configuration

The most common solution for the V/I converter people may think of is the Operational Transconductance Amplifier (OTA), which is widely used in RF circuit as a voltage controlled current source. Fig. 4-24 shows the its basic configuration [D27].

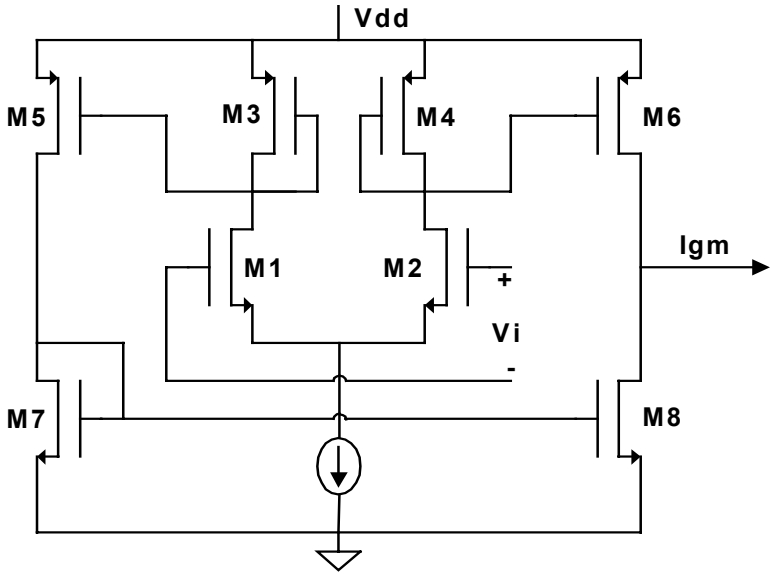


Fig. 4-24. Basic configuration of an OTA.

The OTA is basically an Opamp without an output buffer. Therefore the OTA can only drive capacitive loads. All nodes of the OTA have low impedance except the input and output nodes.

If the impedance of the load capacitor or the resistance of an external load is small compared to the output resistance *Ro6*//*Ro8*, the output current flows mainly in the external load. Assume $\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2$, $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, $\left(\frac{W}{L}\right)_6 = K \cdot \left(\frac{W}{L}\right)_4$ and $\left(\frac{W}{L}\right)_8 = K \cdot \left(\frac{W}{L}\right)_7$. Then the transconductance of the OTA is given by $GM = K \cdot Gm1$, where Gm1 is the transconductance of transistor M1.

However, the value of transconductance Gm can vary as much as 50% due to process, temperature, and layout. Moreover, the structures discussed above are nonlinear, which means that it has a very small input voltage range yielding say 1% Total Harmonic Distortion (THD). Therefore, the basic OTA configuration cannot achieve an accurate V/I conversion. A new topology needs to be developed to serve the purpose.

4.4.3 Topology Development for a Monolithic Accurate Gm Amplifier

To build an ideal V/I converter is always a dream for analog designers. Since 1975, hundreds of papers talking about V/I converters (or say, transconductor / Gm amplifier) have published in JSSC and other journals. Some authors even dedicated their PHD dissertations to addressing how to build and use a Gm amplifier [D28]. Most of these publications emphasize how to improve the linearity or/and bandwidth of a Gm amplifier. And the application focuses on analogue multipliers, arbitrary piecewise linear function generator, oscillators, and high performance filters.

However, there are still some papers trying to address the issues of V/I conversion accuracy and input dynamic range [D29]~[D35]. I develop my Gm topology based on the principles and concepts of these papers.

4.4.3.1 Topology 1: Accurate Enhanced Gain Cell Transconductor

According to Martin's book [D36], when we use current source as the load of an emitter coupled pair with Emitter degeneration, we can get a load independent linear Gm with a large dynamic range and the common mode voltage can be close to ground because of the floating resister configuration. When R_E is much larger than small signal

emitter resistance of the transistor given by V_T/I_E, this Gm equals to $1/R_E$. Fig. 4-25 shows such a configuration.

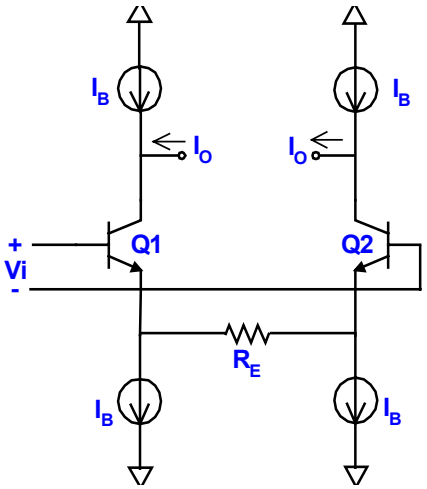


Fig. 4-25. Fixed Gm with the floating resister.

The Gm value in Fig. 4-25 is very small. To increase the Gm the first thing to do is to make Gm changeable. An important analog building block for bipolar circuits is the translinear gain cell proposed by Gilbert for analog multipliers [D37]. Cascading the Gilbert gain cell to a fixed Gm cell according to Fig. 4-26, we can get a changeable Gm. Now the Gm is $(1/R_E)\times(I_2/I_1)$. To enlarge Gm an order by bias current design ($I2/I1$) is not practical because of huge power consumption.

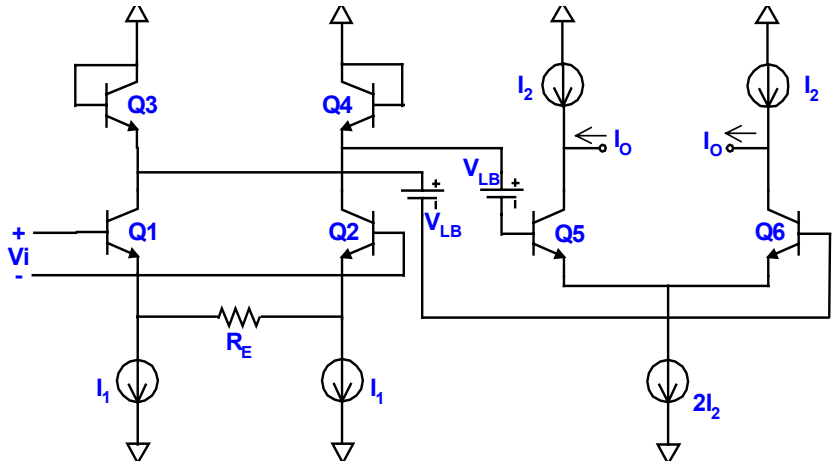


Fig. 4-26. Gain cell transconductor.

However, the gain cell configuration offers a current that can be copied. We can use a current mirror to enhance the Gm. By properly designing a cascade current mirror with a large dynamic range, we can have accurate amplification of the original output current. Now the Gm is $(1/R_E)\times(I_2/I_1)\times n$ (n is the ratio of current mirror).

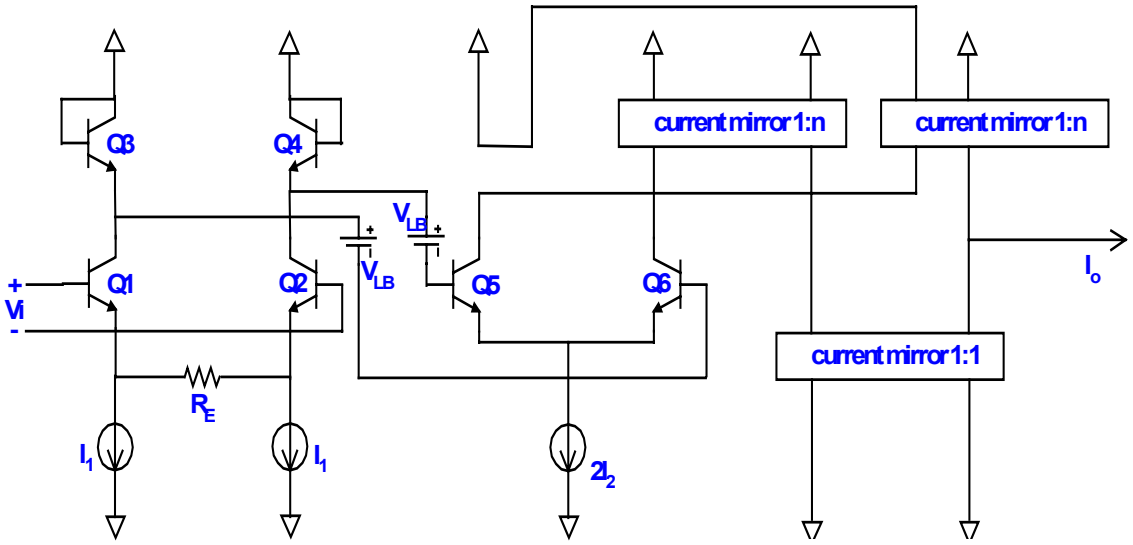


Fig. 4-27. Enhanced gain cell transconductor.

But to use this circuit to build a monolithic Gm, we need to tune R_E, which has 30% variation in typical process. To trim R_E we need an extremely large trimming range and its difficult to set the measure pad and trimming fuse pad in the layout with the floating resistor configuration.

The idea is to change absolute R value trimming to electrical bias trimming. As shown in Fig. 4-28, a very simple Opamp is used to transfer Bandgap Voltage Reference (BGR) to a current and copy it as the bias current of the first Gm stage. Another current I_B works as current bias for the gain cell. By this way, the total Gm is $(R_1/R_2)\times(I_B/V_B)\times(n/2)$. The inaccurate R_1 and R_2 can be matched to give an accurate ratio. If we get accurate I_B and V_B, we get the accurate Gm. Luckily, accurately trimmed V_B and

I_B are often available in power management IC. Therefore, no external trimming is needed for the Gm block.

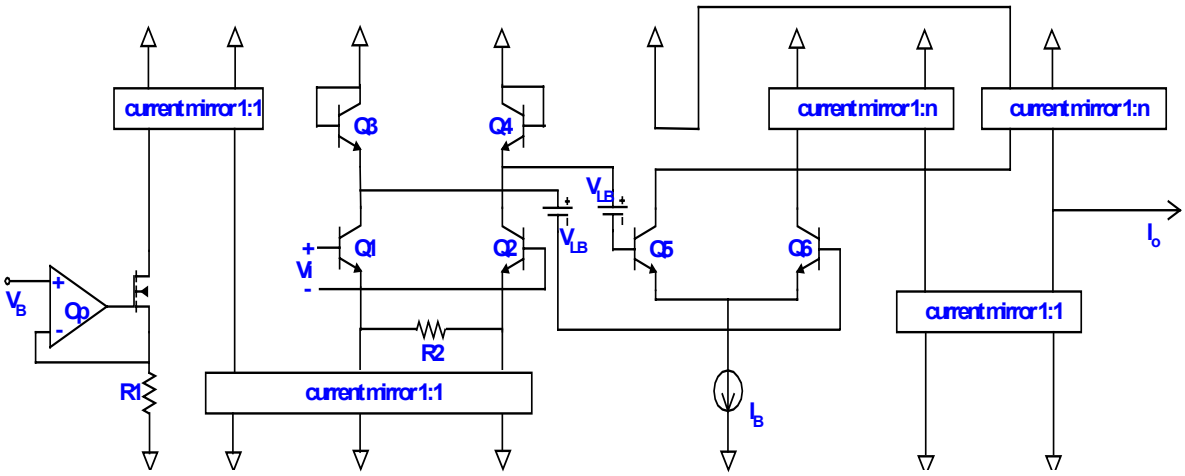


Fig. 4-28. Accurate enhanced gain cell transconductor.

4.4.3.2 Topology 2: A Gm Amplifier Based on Opamp and Current Mirror

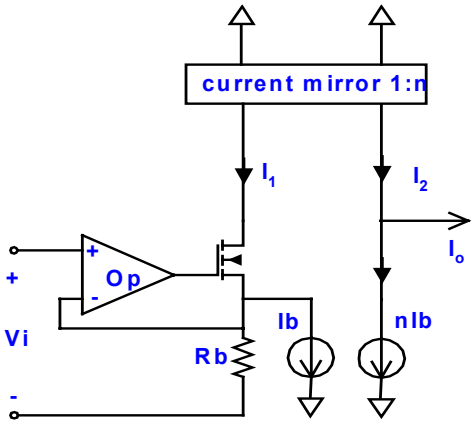


Fig. 4-29. A Gm amplifier based on Opamp and current mirror.

Fig. 4-29 shows another solution for the V/I converter. According to the above figure, it is easy to derive: $Io = I_2 - n \cdot Ib = n \cdot I_1 - n \cdot Ib = n \cdot \left(I_b + \frac{Vi}{Rb} \right) - n \cdot Ib = n \cdot \frac{Vi}{Rb}$. Therefore $Gm = \frac{Io}{Vi} = n \cdot \frac{1}{Rb}$. If Rb is trimmed to an accurate value, the Gm value can be accurate.

By proper Opamp design, the large input dynamic range and the common mode range is achievable.

Although the topology in Fig. 4-29 is more concise than in Fig. 4-28, it has some limitations. The first one is that *Rb* needs to be trimmed or has to be put outside the chip. The second is large quiescent current exiting. To achieve a 1mA maximum output current, the quiescent *nIb* needs to be equal or larger than 1mA. However, it is not the case in Fig. 4-28. Based on the comparison, topology 1 is selected to implement the V/I converter in the proposed current sensing scheme. Fig. 4-30 shows the simulation results with the proposed sensing scheme, in which the Gm block is implemented with the topology shown in Fig. 4-28.

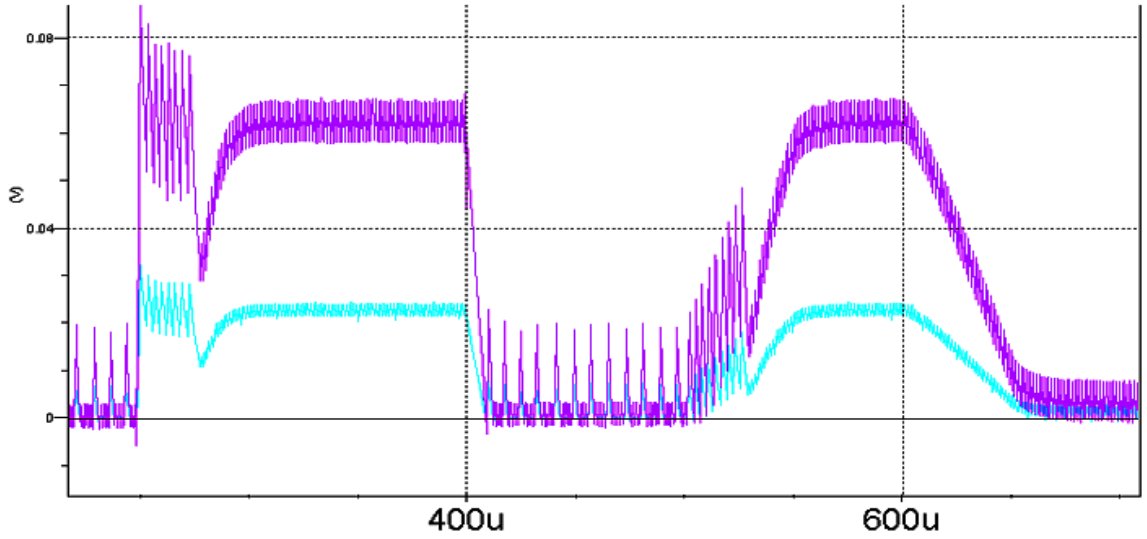


Fig. 4-30. Simulation results with the proposed sensing scheme and Gm block.

In Fig. 4-30, the purple curve is the inductor current, the bright blue curve is the output of the current sensing scheme. The results are almost the same as Fig. 4-21, which verifies the feasibility of the proposed Gm block. The silicon verification of the Gm block will be presented in Chapter 5.

4.5. Other Applications of the Gm Amplifier

4.5.1 Other Current Sensing Configurations with the Gm Amplifier

With the accurate Gm block integrated inside the chip, customers can not only configure it as the proposed current sensing scheme, but also have the flexibility to configure it as the original current sensing scheme and resister current sensing scheme, as shown in Figures 4-31 and 4-32. In Fig. 4-31, the current sensing gain $Ri = Rsen \cdot Gm \cdot Rg$. In Fig. 4-32, the current sensing gain is $Ri = R_L \cdot Gm \cdot Rg$.

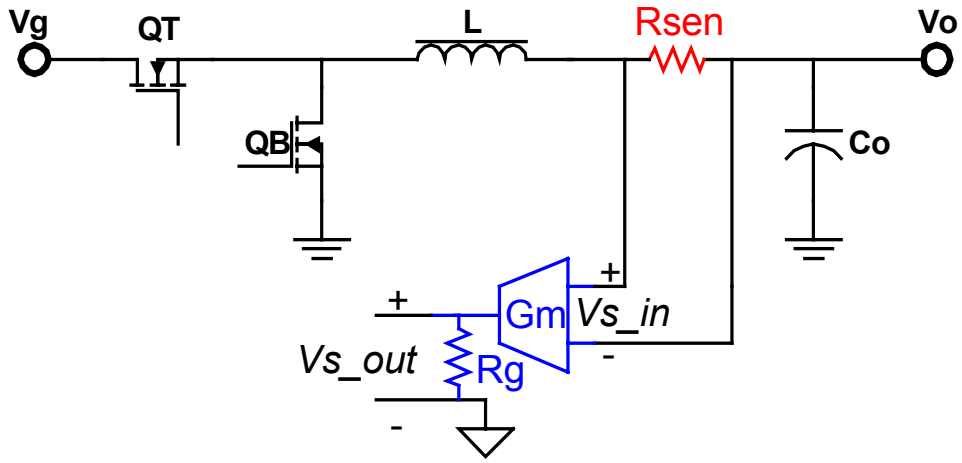


Fig. 4-31. Resister current sensing with Gm amplifier.

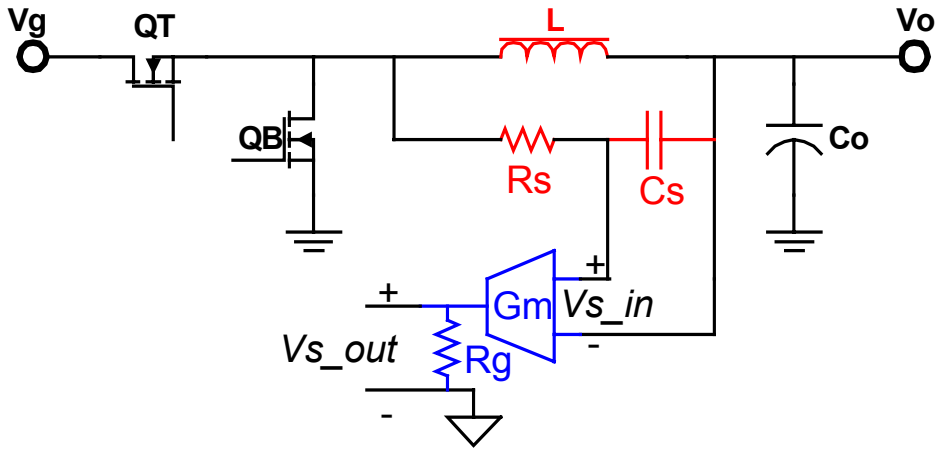


Fig. 4-32. Inductor current sensing with Gm amplifier.

4.5.2 AVP Without an Additional Adder

When AVP is needed, with the accurate Gm block integrated inside the chip, the output voltage signal can be added to the sensed inductor current signal without an adder. Figures 4-33 ~4-35 show such configurations.

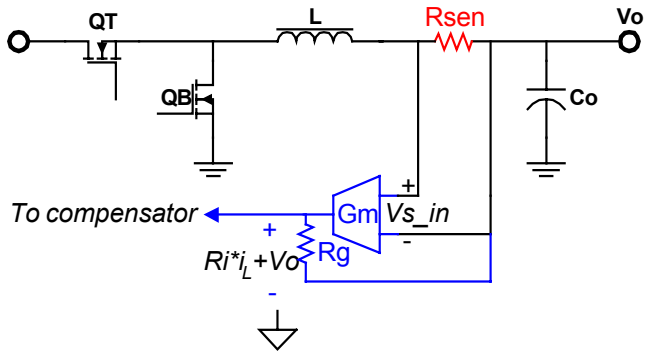


Fig. 4-33. AVP configuration with Gm amplifier and resistor current sensing.

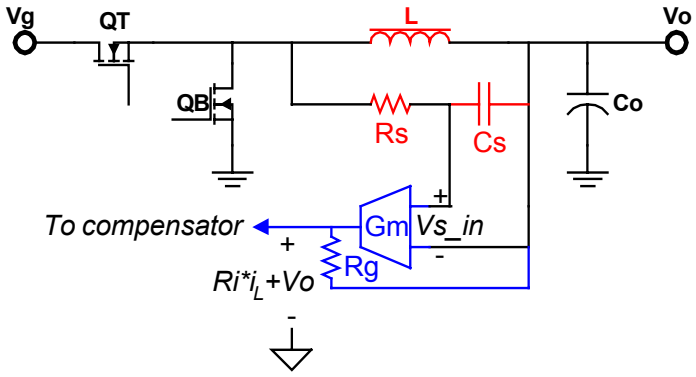


Fig. 4-34. AVP configuration with Gm amplifier and original inductor current sensing.

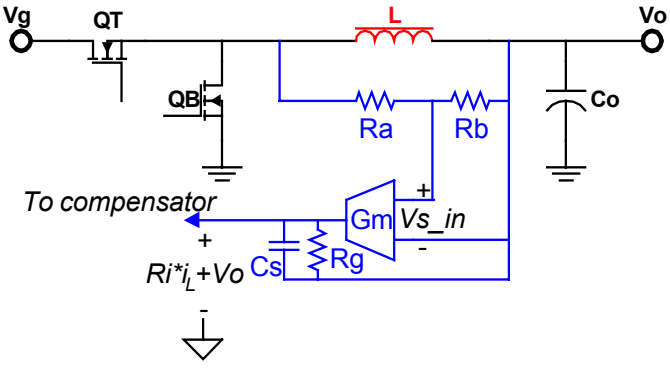


Fig. 4-35. AVP configuration with Gm amplifier and the proposed current sensing.

4.6. The Concept of Power Stage Emulator

The objective of current sensing in power electronics is to provide a signal proportional to the instantaneous current or average current going through a power stage loop. This signal needs to be scaled within a reasonable range and in a suitable format (analog or digital, voltage or current, differential or single ended) so that it can be understood by the other part of control circuitry.

To provide this signal, one approach is to get a signal proportional to the current from power stage and scale it and transfer it into the controller. Resistor current sensing, Rdson current sensing and sensing FET current sensing belong to this catalog.

Another approach to provide this current information is to sense a signal from the power stage having a known relationship with the current, and process this signal to restore the current information. Inductor current sensing and the proposed "Gm current sensing" belong to this catalog.

Following this train of thought, we can sense the current more indirectly. Fig. 4-36 shows a scheme adopting a power stage emulator, which emulates the relation of the inductor current and other power stage parameters using signal level circuitries.

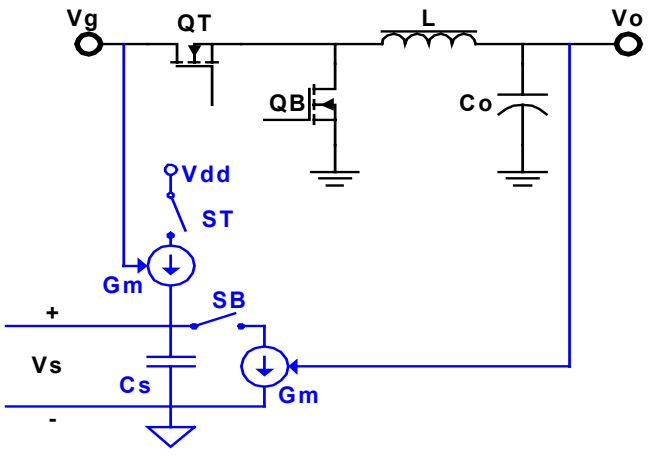


Fig. 4-36. Current sensing with a power stage emulator.

In Fig. 4-36, the power stage emulator is composed of two voltage controlled current sources, two analog switchers and one capacitor. ST and QT turn on and off simultaneously, so do SB and QB. If ignoring the second order tolerances, we can have $Vs = Gm \cdot Cs / L$. In reality, it is difficult to build an accurate Gm and to maintain the ratio of Cs and L. The scheme in Fig. 4-36 is not practical for implementation. However, it shows the concept of current sensing using power stage emulator.

Although resistor current sensing is accurate, indirect approaches like inductor current sensing or even power stage emulator may have their value to tradeoff among sensing accuracy, efficiency and bandwidth.

4.7. Summary of Chapter 4

Different current sensing schemes have different tradeoff on accuracy, efficiency and bandwidth, and suit for different applications. Inductor current sensing is becoming more and more popular in VR application because of its 0 power loss and acceptable sensing accuracy. However, the original inductor current scheme has its limitation in the application with small inductors, and the input impedance of a differential amplifier has great impact on sensing accuracy. To overcome these issues, a novel current sensing scheme adopting an accurate V/I converter is proposed. And a Gm amplifier topology is developed to implement the monolithic V/I converter without trimming. Hardware testing and software simulation verifies the feasibility of proposed current sensing scheme and the Gm amplifier. The proposed Gm block has other benefits. With the accurate Gm block integrated in the chip, a customer has the flexibility to choose different current sensing schemes according to different design requirements. And the AVP function can be achieved without an additional adder.

Chapter 5. Silicon Verification of the Proposed Analog Blocks and Control Schemes

5.1. Proposed MVRC Chip

In chapter 1, the Monolithic Voltage Regulator Channel is proposed as a generic power IC solution for CPU and POL power supply. To make MVRC a reality, three technology issues need to be overcome, which are: distributed interleaving, distributed AVP and current sharing, inductor current sensing with small inductors.

For interleaving, a scalable distributed interleaving scheme is proposed in chapter 2 and it is verified with a hardware prototype as shown in Fig. 2-13. Besides the unlimited phase interleaving, this scheme has another big advantage over other distributed interleaving schemes: each channel's interleaving circuitries can be monolithically integrated without any external components, which is because the key building block, a self-adjust saw-tooth generator is layout and process insensitive and the cap used this block can be smaller than 1pF.

For AVP and current sharing, a scalable distributed AVP and current scheme is proposed in chapter 3 and it is verified with a hardware prototype as shown in Fig. 3-49.

For current sensing with small inductors, an improved inductor current scheme with an accurate Gm amplifier is proposed in chapter 4 and it is verified with a hardware prototype. However, in that hardware prototype, the key building block, an accurate Gm amplifier, is built with 6 Opamps configurated as the Howland current pump. This implementation is not practical in MVRC solution due to the silicon size and offset

issues. A more concise topology based on gain cell configuration is developed to serve the purpose.

Following the concept of MVRC proposed in chapter 1, and based on the control schemes and analog blocks proposed in chapters 2~4, a block diagram of the MVRC chip is developed, as shown in Fig. 5-1.

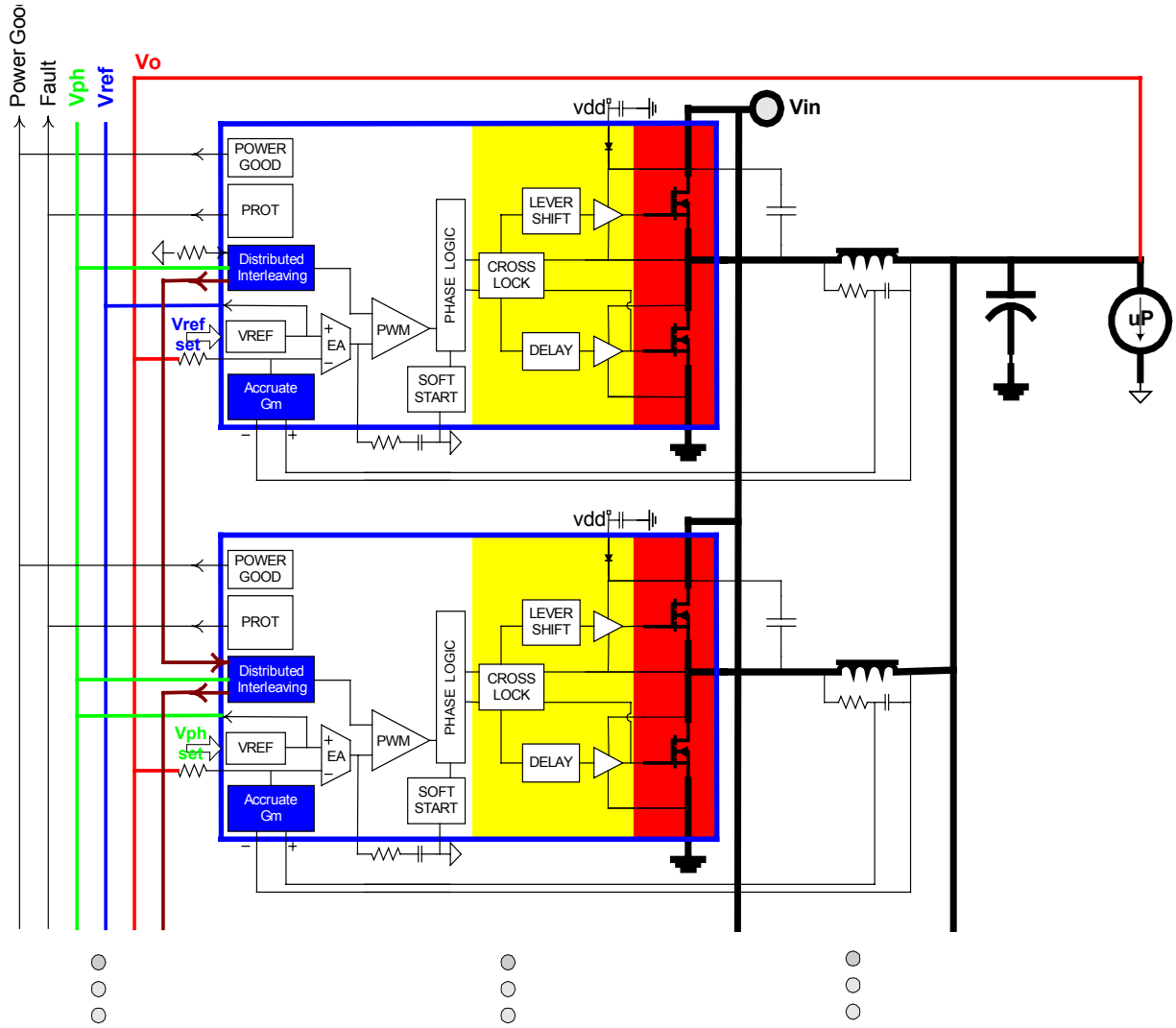


Fig. 5-1. Proposed MVRC solution for CPU power management.

As shown in Fig. 5-1, each MVRC chip has power MOSFET, driver, and control integrated in one die. The control schemes are developed in previous chapters. And the blue blocks are the proposed novel analog blocks, which include a “distributed

interleaving" block and an "accurate Gm" block. As described in previous chapters, they serve as the key building blocks of the control.

For the configuration, each channel's inductor current information only feedbacks to this channel's MVRC chip. Therefore there is no long current feedback line. The only long analog bus lines are the voltage reference line "Vref" and the phase delay setup voltage "Vph". They all are DC lines and insensitive to the noise. The voltage "Vref" is set by one MVRC's VREF block (a simple but accurate DAC) or can be set by all MVRC chips' VREF blocks tied together. The voltage "Vph" is set by one MVRC's VREF block or simply comes from a voltage divider. The external components for each channel (beside the power stage) are compensator resistors, capacitors, droop resistors, and decoupling caps for the chip's signal power. It is easy to see that compared with IR's Xphase solution, the proposed MVRC solution have smaller component counts and less noise sensitive lines. More importantly, the MVRC is a generic power IC that can also be used alone to supply a regular POL. Fig. 5-2 shows the configuration of the proposed MVRC chip as a regular POL power supply.

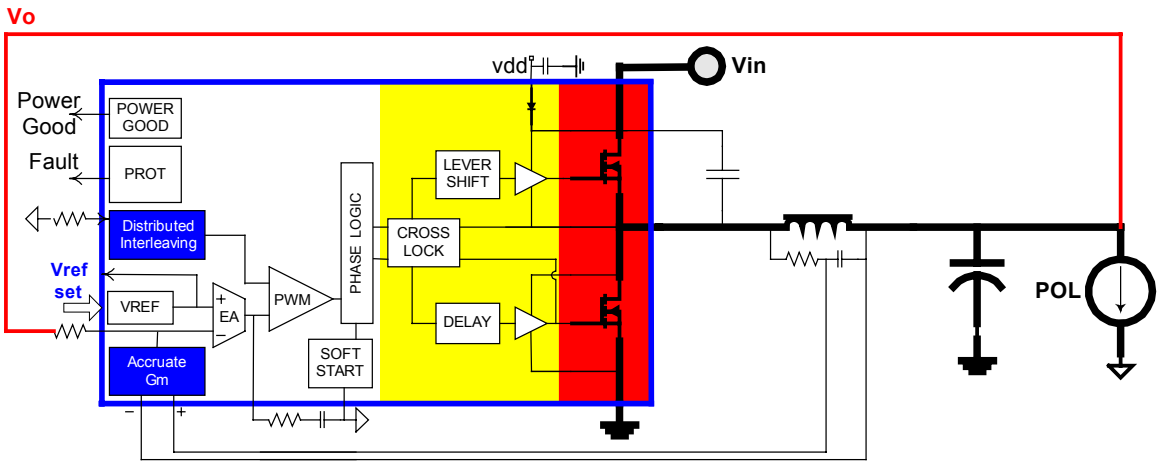


Fig. 5-2. Proposed MVRC chip supplying a POL.

5.2. Testing Chip Diagram

Although the proposed control schemes are verified by hardware prototype, silicon prototype is necessary to verify the proposed analog blocks and further verify the control schemes. In chapter 1, the MVRC concept is developed based on the assumption that the silicon size of the control circuitry is much smaller than that of the power devices, and the power loss of the control part can be ignored when compared with that of power devices. To verify this assumption, a silicon prototype is necessary and important.

The following is the summary of the objectives of the testing chip:

1) Verify the proposed analog building blocks. Including:
    A. A distributed interleaving block
    B. An accurate Gm amplifier without trimming.
2) Further verify the proposed control schemes in silicon. Including:
    A. A scalable distributed interleaving scheme;
    B. A scalable distributed AVP and current sharing scheme;
    C. An improved inductor current sensing scheme.
3) Verify the total silicon size and power consumption of each channel's control circuits.

The best way to demonstrate the MVRC concept is to develop a real MVRC chip, as shown in Figures 5-1 and 5-2, to show that it works and works well. However, because of the limited recourse, it is impossible for university to develop such a large chip.

However, to achieve the objectives mentioned above, a testing chip that integrates each channel's control part is enough. But even such a control chip is very difficult to be built in university without a sponsor.

Luckily, a sponsor supported me to build a two channel BUCK controller for Graph card and DDR power management application. I developed the chip in such a way so that the chip can satisfy the sponsor and at the same time can serve as a testing chip to achieve the objectives mentioned above.

Fig. 5-3 shows the block diagram of this testing chip.

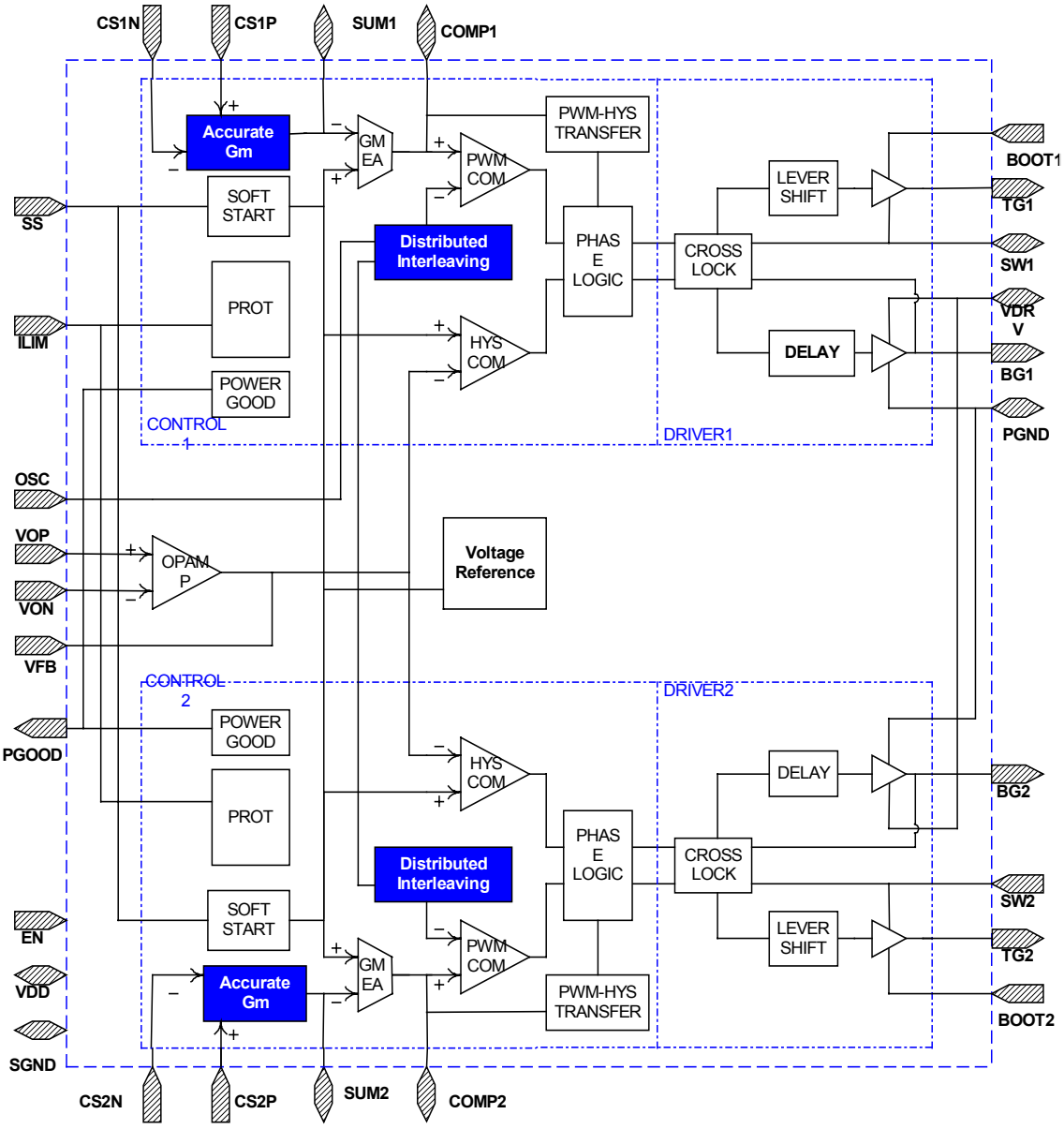


Fig. 5-3. Block diagram of the testing chip.

As shown in Fig. 5-3, there are two independent control units in this chip. Each control unit serves the function as the control portion in MVRC chip. Each control unit has exactly the same circuitry, which includes the control core (to realize distributed interleaving, Adaptive Voltage Position and current sharing), a driver and some general blocks like protection and soft-start. The control core is explained in chapter 2 , chapter 3 and chapter 4. The interleaving function is achieved by the novel "distributed interleaving" block. AVP and current sharing is achieved by active droop control, which is implemented by an error amplifier "GMEA" and a PWM comparator "PWMCOM". The transconductance amplifier "Accurate Gm" is used to get better current sensing and to work as one part of the AVP loop.

Each control unit in Fig. 5-3 has almost the same circuitry proposed to be used in the MVRC chip as shown in Figures 5-1 and 5-2. Other blocks like "PWM-HYS Transfer" are adopted as the requirement of the sponsor and are beyond the discussion of this dissertation. The only block shared between the two control units is the voltage reference and an Opamp used for a differential amplifier to do the remote voltage sense.

The power MOSFET drivers were also integrated in the testing chip. It is a regular bootstrap NMOS driver. The basic building blocks include a "top device deriver", a "bottom device driver", a "lever shift", a "delay" block, and a "cross lock" block. The drivers are designed to have 2A peak current and 1Ohm impedance.

This chip was internally configured as a 2 channel interleaving BUCK controller. The application is just as Fig. 5-1 when channel number is 2. Therefore, not only the proposed analog blocks but also the proposed distributed control scheme can be verified by testing this 2 channel control chip.

5.3. Design Methodology

Fig. 5-3 shows the typical approach to design DC-DC controller in industry. First, we do chip specifications, then architecture selection, then block schematic design, then top-level design and chip simulation, then floor plan, then layout, and then tape out. It seems straight forward, but long loop iteration would happen amogn block schematic design, top-level design and chip simulation. It is fully dependent on the skill and experience of the designer to decrease the number of iterations. And it is time consuming. The key issue is that we cannot verify a block in the system unless the other blocks all have been synthesized. We have to identify and find solutions for both circuit level and higher level issues with almost full chip simulation, which wastes a huge amount of simulation time and human resource.

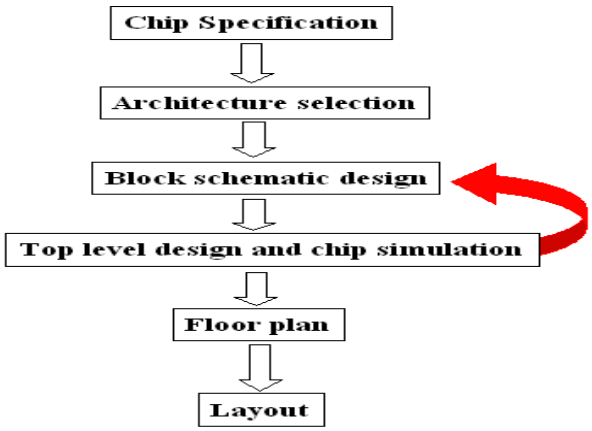


Fig. 5-4. A typical power management IC design flow in industry.

Other chip design, especially more complex digital VLSI chip design also meets the issue of block verification. The difference is that all today's complex digital circuits are designed with a powerful tool, HDL (Hardware Description Language). With the concept of HDL, the design becomes a series of transformations from one representation of a system to another until a representation exists that can be fabricated. And it is not

required that all system components be specified on the gate level in order to evaluate the gate level design of a specific component. As you can see in Fig. 5-5, the behavior modeling can be and should be used on different hierarchy levels to verify others in the system. By this way, in digital VLSI design, the long loop iteration can be avoided. Fig. 5-5 shows this "partial tree design" concept [E1].

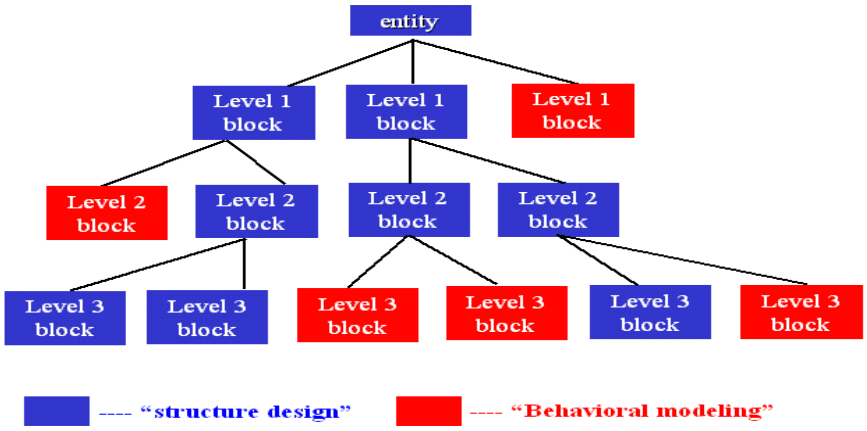


Fig. 5-5. The concept of partial tree design in HDL.

We can also adopt the "partial tree" design approach in analog power management IC design. One way is to use Analog HDL Language (AHDL). But AHDL is expensive and not mature and mostly unavailable in IC designer's CAD package. The other way is to develop the behavior modeling of each block without AHDL. Because of the characteristics of the DC-DC controller, the function of each block can be described simply with ideal voltage source, ideal current source, ideal switch, ideal resistor, ideal inductor, ideal capacitor, and ideal delay block. For example, a comparator can be modeled by a voltage controlled voltage source.

The "partial tree" design approach in Fig. 5-4 also needs a clear idea of the design hierarchy. Hierarchy is the most important concept in VLSI and it is the key to the DC-DC controller ASIC design. Analog designers have a tendency to use a brick in east wall

to fix a hole in west wall. Clear and proper hierarchy will avoid this problem. Fig. 5-5 is my proposed generic hierarchy for a DC-DC controller. This figure only shows the first 2 level of the hierarchy for the indispensable parts. My objective is to make each block not only a function block but also a physical circuitry block and layout block. The hierarchy is usable not only in schematic design but also in schematic library building. As you can see the control core design is only a small part of the whole chip.

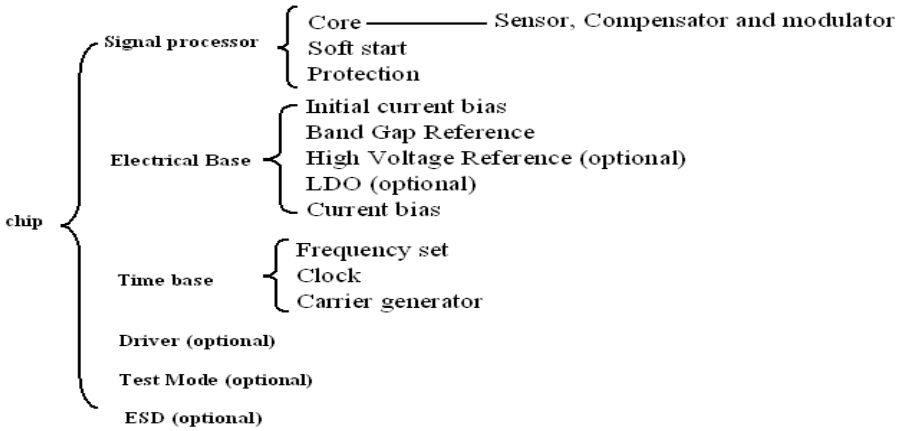


Fig. 5-6. Generic hierarchy for dc-dc controller design.

With the concept of "partial tree" design and with a clear idea of design hierarchy, we can design a DC-DC controller as the following steps.

Step 1--- Chip specifications. Make the overall function of the chip clear, including soft-start and protection parts. Make the I/O of the chip clear.

Step 2---- Testing bench setup. The testing bench for a DC-DC controller is a close loop test bench, which is usually the typical application circuit of the chip.

Step 3---- Hierarchy break down. Make sure each block is not only a function block but also a physical circuitry block and layout block.

Step 4---- Behavior modeling. The behavior modeling is not a traditional model for the whole system as a unit but for each individual hierarchy top two level blocks. The I/O

of these blocks should keep the same as the real implementation. After all the blocks are modeled, we get chip_A, which is built by behavior model blocks. Verify this chip with the prepared testing bench. This simulation usually takes several minutes.

Step 5---- Real core. The transistor level core control part is designed in this step. With the "real core", we get chip_B. This simulation usually takes tens of minutes to verify this chip_B.

Step 6 ---- Other part. After step 5, we can design the real driver; the first time chip simulation may take 1 hour. Then design the ESD; the chip simulation may take 2 hours. Then design the real electrical base; the chip simulation may take 4 hours. Then design the real time base; the chip simulation takes 8 hours. Then design the soft-start; the chip simulation may take 16 hours. Then design protection; the chip simulation may take 24 hours. Then design the real test mode circuitry; the chip simulation may take 48 hours.

Until now we get the finial transistor level chip schematic. By this way, no long loop iteration happens and we can do hundreds of system simulation before chip_C is synthesized, where usually most issues can happen. The crystal clear hierarchy and the order of implementation is the key of my approach. Fig. 5-6 summarizes this approach.

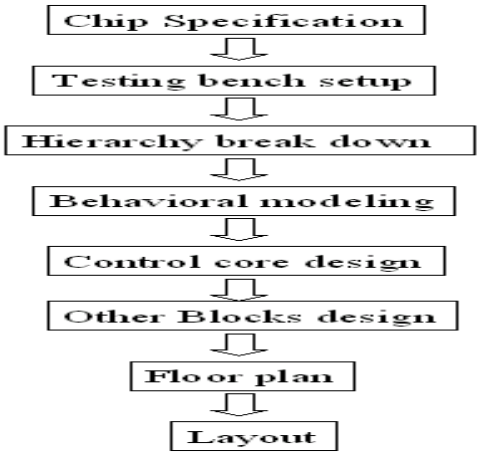
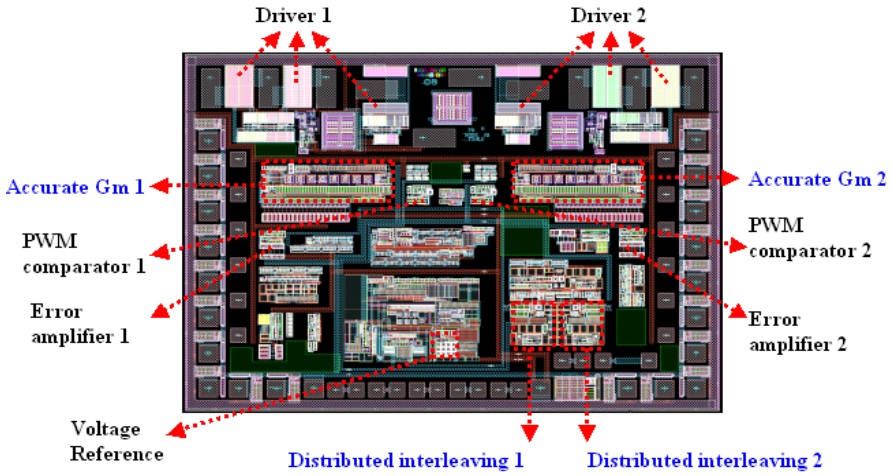


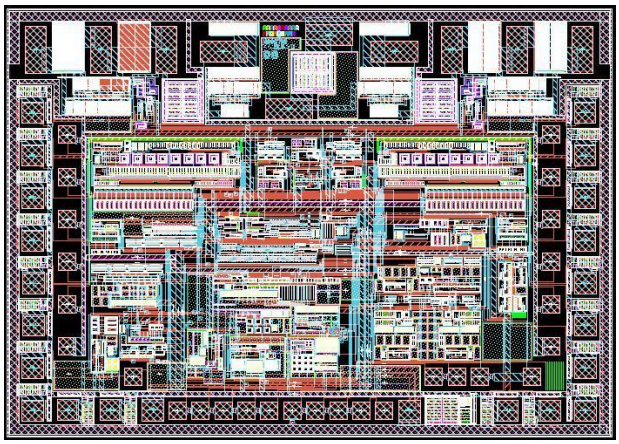
Fig. 5-7. Proposed design approach for a DC-DC controller.

5.4. Layout and Die Photo

According to the design approach in section 5.3, the testing chip, as shown in Fig. 5-3, is developed with TSMC0.5um BiCOMS process. Fig. 5-8a shows the layout of this chip before top level routing. The proposed analog block "Accurate Gm" and "distributed interleaving" and some other major analog building blocks are marked. Fig. 5-8b shows the completed layout of this chip. The layout floor plan follows the design guidelines described in [E2].



a. Before top level routing



b. After top level routing

Fig. 5-8. The chip layout.

Fig. 5-9 shows the chip die photo. The proposed analog blocks are marked. The total die size is 2200um×1800um. Fig. 5-10 shows more detailed photos of the proposed analog blocks.

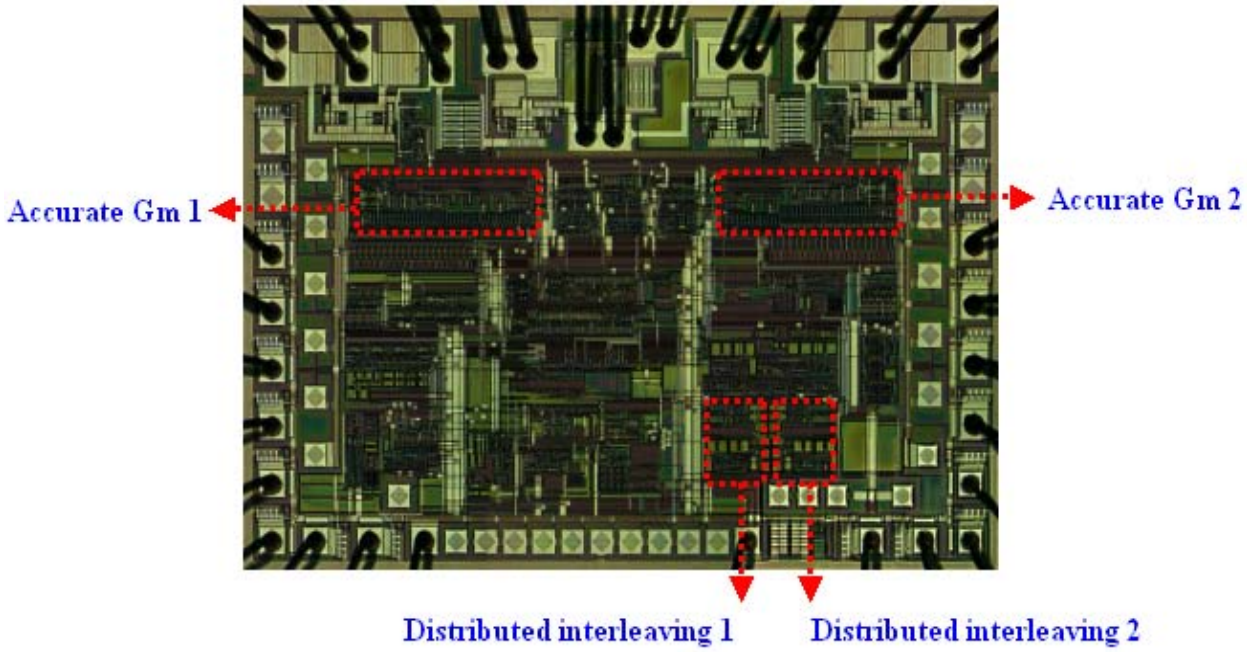
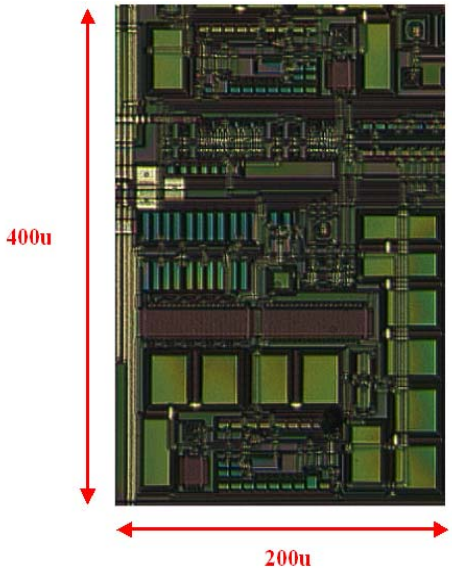
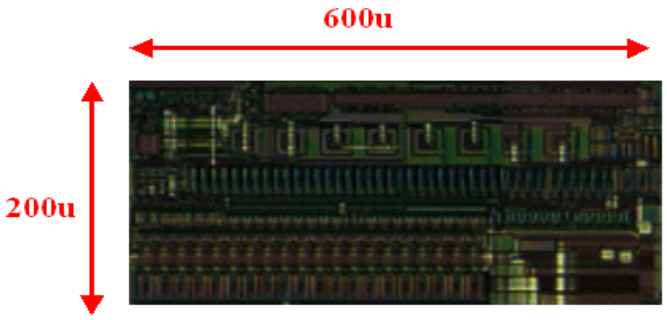


Fig. 5-9. The die photo (Die size 2200um×1800um).



a. Distributed interleaving

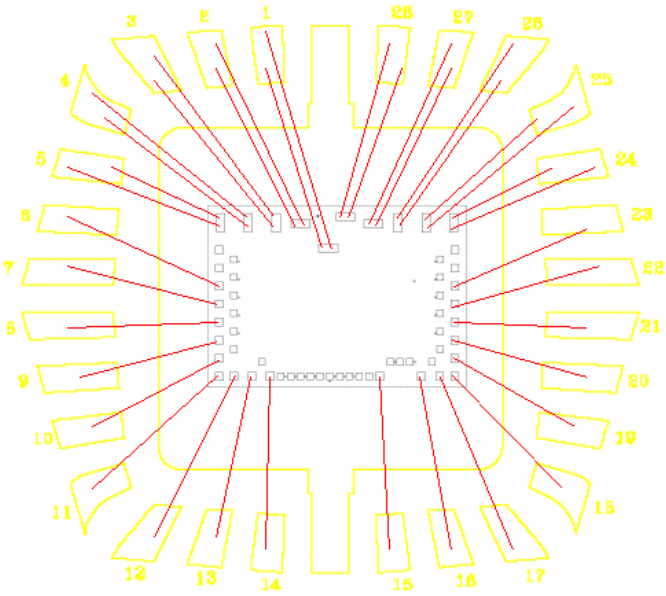


b. Accruate Gm

Fig. 5-10. Die photo of the proposed analog blocks.

5.5. Block Testing Results

The fabricated testing chip has been packaged in DIP28 package for silicon level and block level testing. The major blocks needed to be verified include the proposed "distributed interleaving" block, the proposed "accurate Gm" block and the voltage reference block. Fig. 5-11 shows the chip in DIP28 package.



a. Banding diagram

b. Chip photo

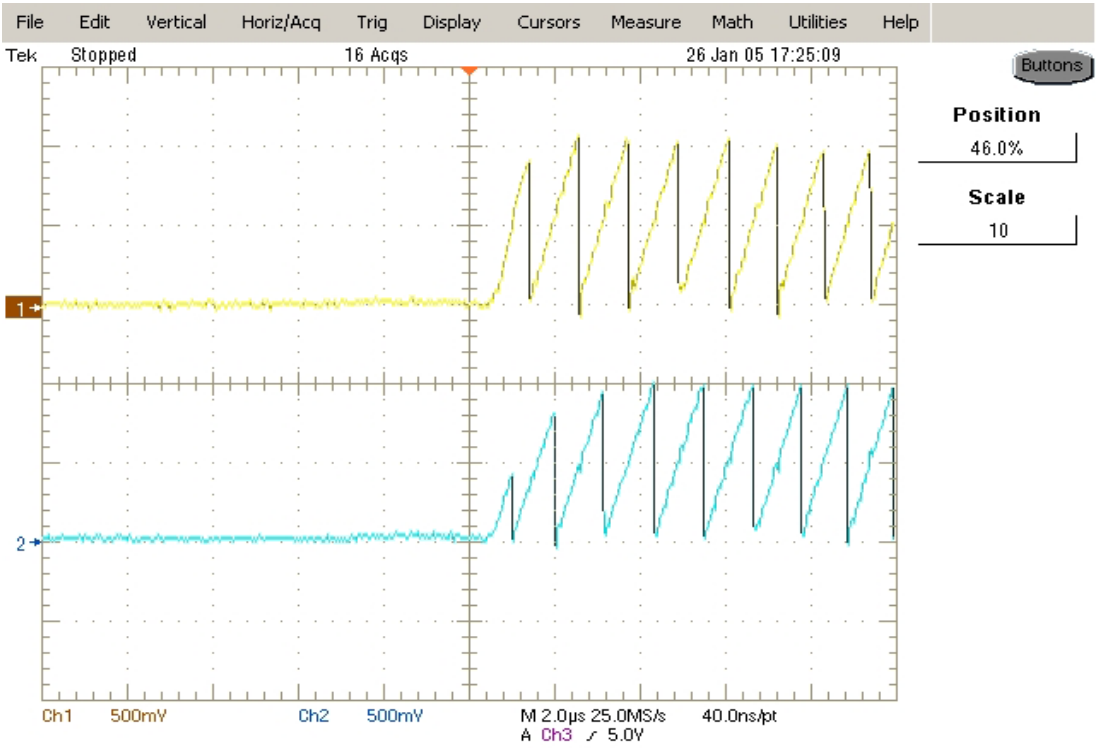
Fig. 5-11. Testing chip in DIP28 package.

5.5.1. Testing Results of the Distributed Interleaving Block

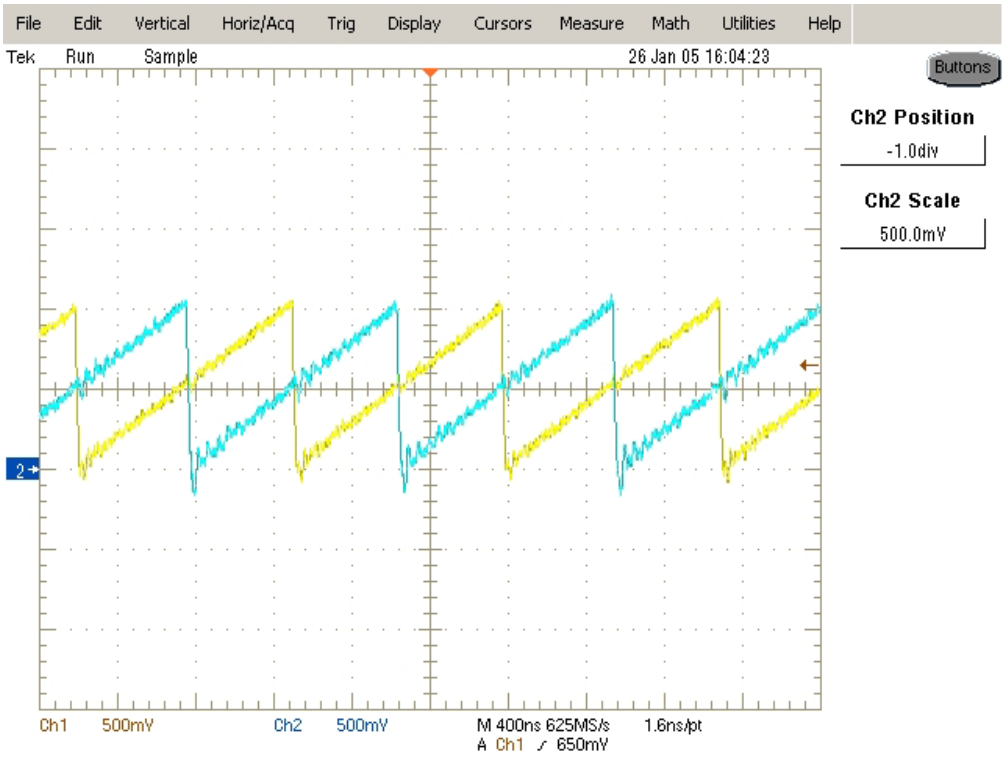
Chapter 2 proposed a distributed interleaving scheme. The automatic interleaving is achieved by each channel's "distributed interleaving" block, as shown in Fig. 2-9, which is composed by an accurate delay block and a self-adjust saw-tooth generator block. And the self-adjust saw-tooth generator block is also the key sub-block of the accurate delay block. As explained in chapter 2, the proposed distributed interleaving block can be monolithically integrated without any external component. Fig. 5-10a shows the silicon photo of the distributed interleaving block in the testing chip. The size is only 200μm ×

400μm. In the test chip, the cap in the self-adjust saw-tooth generator (Csaw in Fig. 2-11) can be intentionally trimmed to different values by breaking a fuse between two trim pads associated with the saw-tooth block of the testing chip.

In the testing experiment, the Csaw of channel 1 is 100μm×100μm (about 1pF). In channel 2, Csaw is changed to 100μm×50μm (about 0.5pF). Fig. 5-12 shows the measured waveforms of the output of the interleaving block: Vc1 and Vc2. Fig. 5-12a shows the waveforms when the Vcc 5V is just turned on. Fig. 5-12b shows the waveforms after settling down. Although the Csaw in one channel is about 2 times of the other, the output saw-tooth waveforms still settle down to the same amplitude defined by Vref (1V). And the slopes of the two saw-tooth waveforms are also the same after they settle down. The settling time of the two saw-tooth waveforms is just several switching cycles. These waveforms verify the idea of "self-adjust" is working.



a. Vc1 and Vc2 when the Vcc is just turned on



b. Vc1 and Vc2 after settling down

Fig. 5-12. Testing results of the distributed interleaving block.

Table 5-1 shows the summary of the performance of the distributed interleaving block in the testing chip.

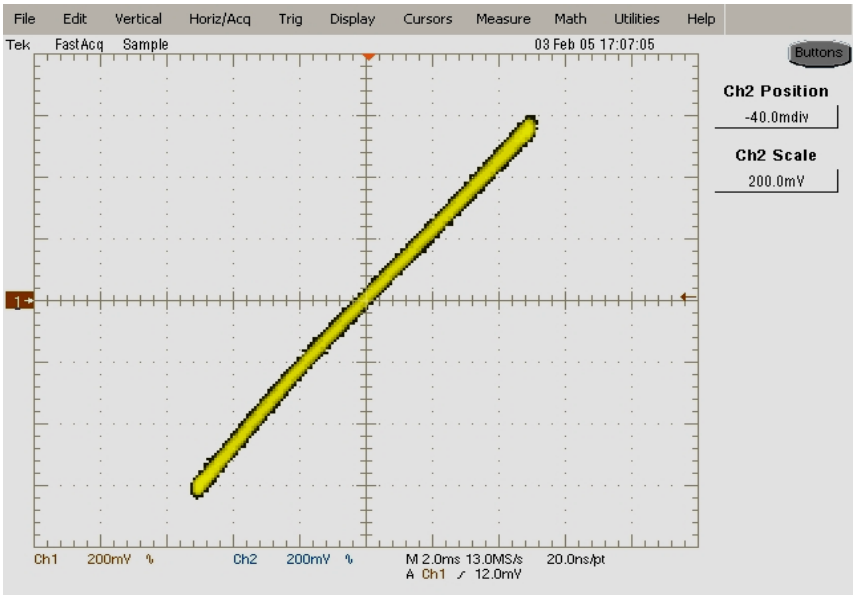
Maximum channel number allowed	Unlimited
Maximum switching frequency allowed	2MHz
Minimum switching frequency allowed	200KHz
Interleaving maximum phase error	< 2%
Maximum time from power on to output settling down	500uS
Saw-tooth peak value	1.2V
Saw-tooth valley value	0V
Die size	200um×400um
Power consumption	100uA @ 3.3V Vdd

Table 5-1. the summary of the performance of the distributed interleaving block.

5.5.2 Testing Results of the Accurate Gm Block

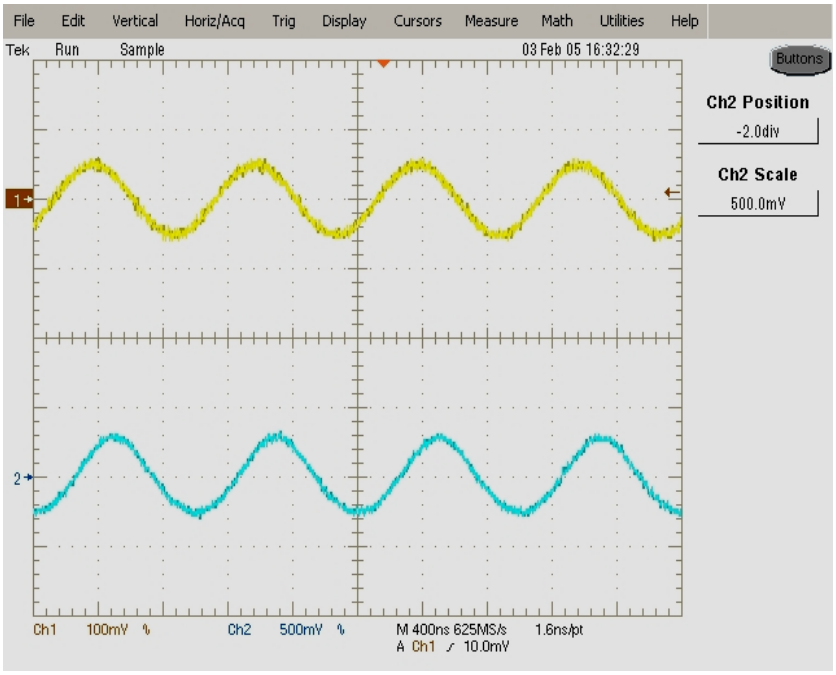
Chapter 3 proposes a distributed AVP and current sharing scheme. The current sensing is the most important part of this scheme. In chapter 4, a novel technique of inductor current sensing with an accurate transconduance amplifier is proposed. The analog topology of the accurate transconduance amplifier is also developed. Fig. 5-10b shows the silicon photo of the proposed Gm amplifier in the testing chip. The size is only 200um × 600um.

Fig. 5-13 is the testing results of the Gm amplifier. The results show that the proposed Gm amplifier has a large input linear dynamic range (about 1V), high -3dB bandwidth (about 3MHz), accurate Gm value (1mA/V ±2%) and very low output offset (<0.1uA). Measurement also shows that the proposed Gm amplifier has very low power consumption (100uA/5V Vdd).



a. Linearity (X axis: input differential voltage; Y axis: voltage across the load resistor.)

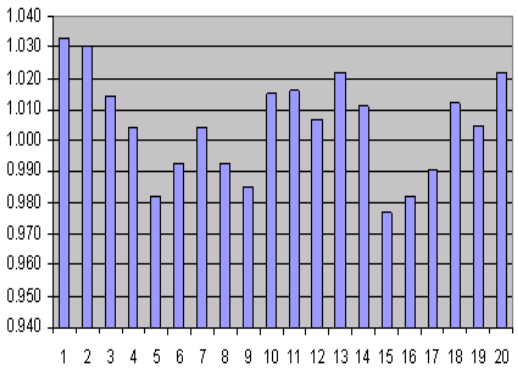
** Input differential signal: 500Hz sinusoid waveform; Input common mode voltage: 1V; Output common mode voltage: 1V. Load impendence: 1KΩ.*



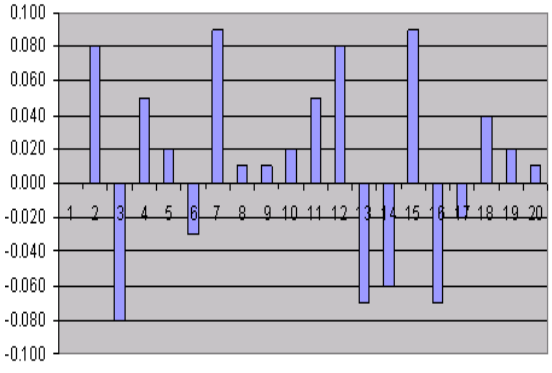
b. Frequency response

(Blue: input differential voltage; Yellow: voltage across the load resistor.)

* *Input differential signal: 1MHz sinusoid waveform; Input common mode voltage: 1V; Output common mode voltage: 1V; Load impendence: 1KΩ.*



c. Gm value distribution



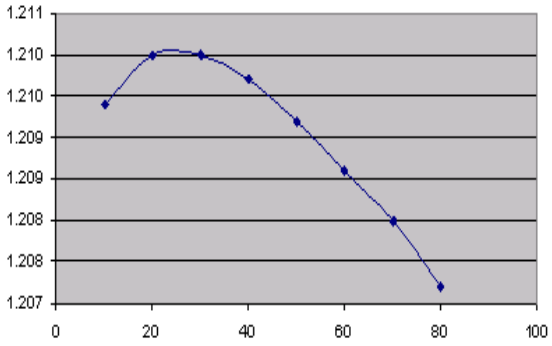
d. Gm output offset distribution

Fig. 5-13. Testing results of the proposed Gm amplifier.

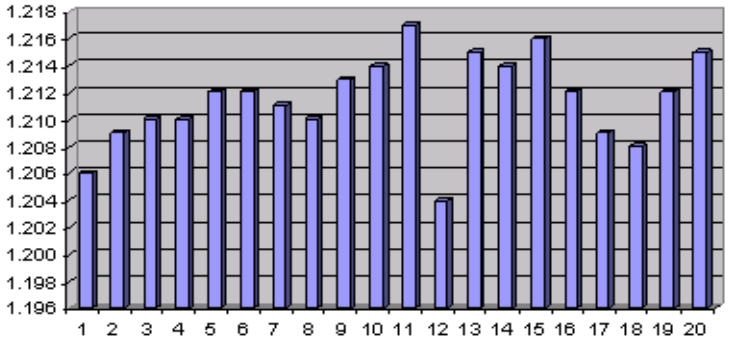
* *Sample number: 20.*

5.5.3 Testing Results of the Voltage Reference Block

Besides the proposed distributed interleaving block and the accurate Gm amplifier, the voltage reference is also the key building block of the proposed control scheme. An accurate voltage reference can be achieved with the traditional bandgap voltage reference topology with proper trimming [E3]. Fig. 5-14 shows the testing results of the voltage reference block used in the testing chip. These results show an accurate Vref (1.210±0.35%) can be achieved over a large temperature range (-40~80^{o}C).



a. Variation of Vref with temperature



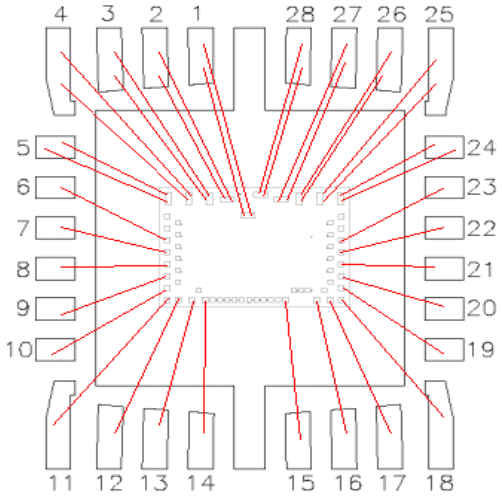
b. Distribution of Vref values (manually trimmed, sample number: 20)

Fig. 5-14. Testing results of the voltage reference block.

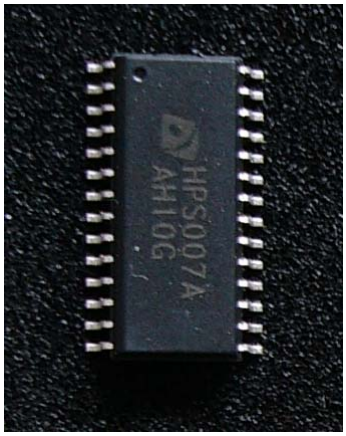
Besides the three blocks mentioned above, other analog blocks of the testing chip have also been tested. Since they are conventional DC-DC building blocks or unrelated to this dissertation, the testing results of these blocks are not included.

5.6. System Testing Results

The fabricated testing chip has also been packaged in SOIC28 package for system level testing to further verify the proposed analog blocks and control schemes. Fig. 5-15 shows the chip in SOIC28 package.



a. Banding diagram



b. Chip photo
("HPS007A" is the project code used in the sponsor company)

Fig. 5-15. Testing chip in SOIC28 package.

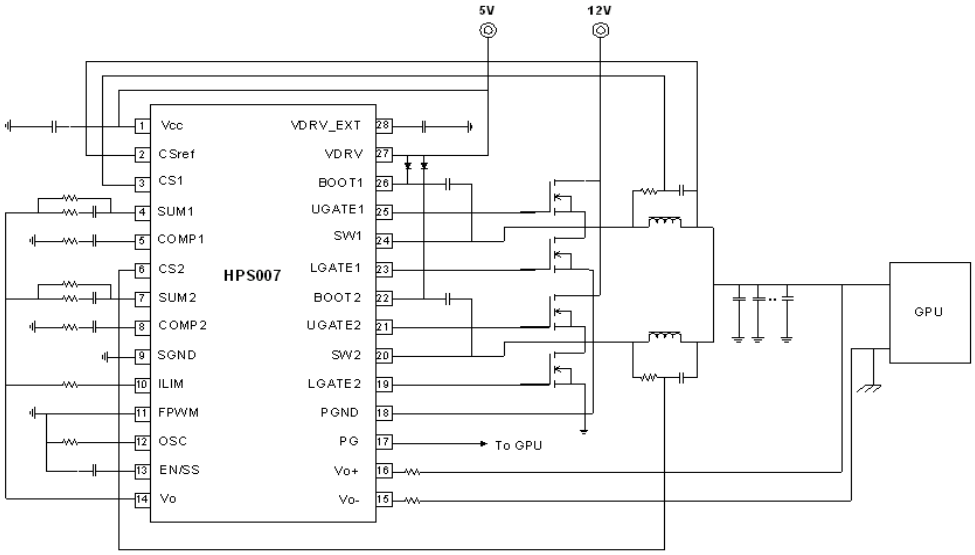


Fig. 5-16. The application circuit for the testing chip.

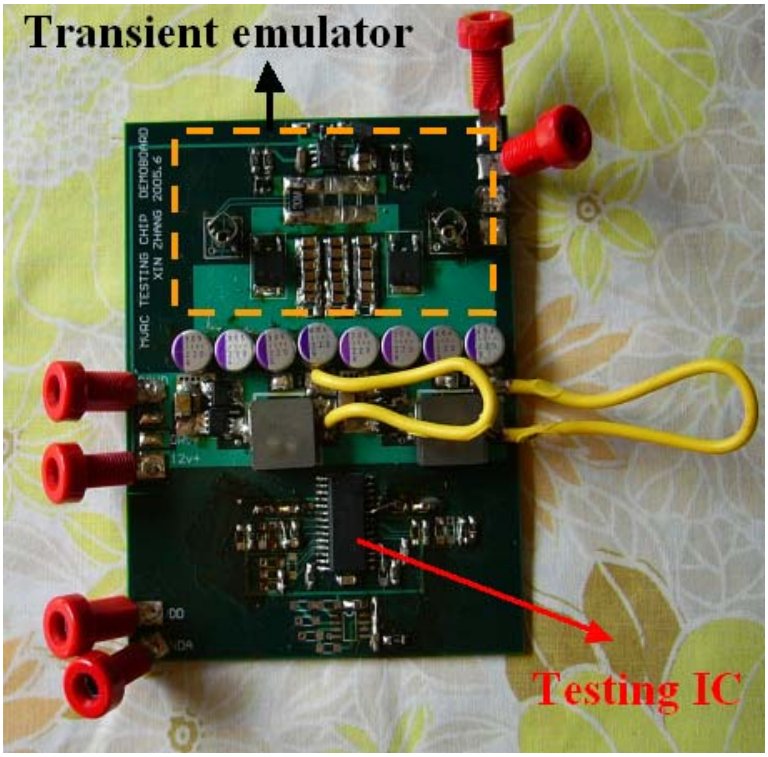
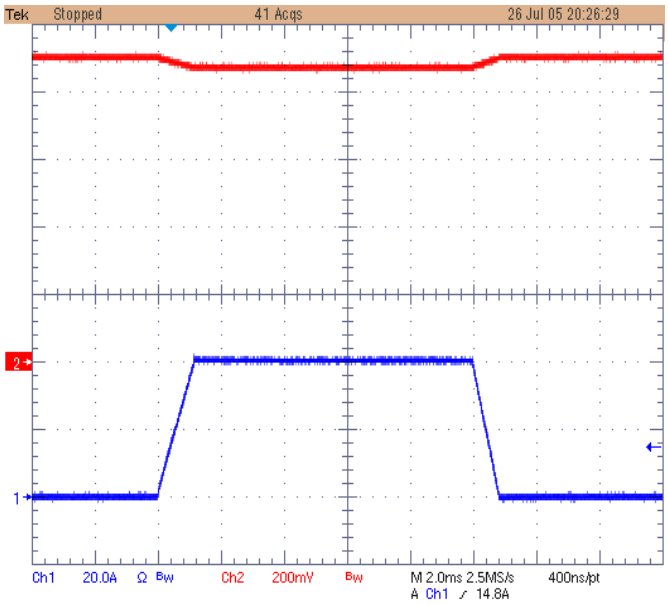


Fig. 5-17. The photo of the demo board of the testing chip.

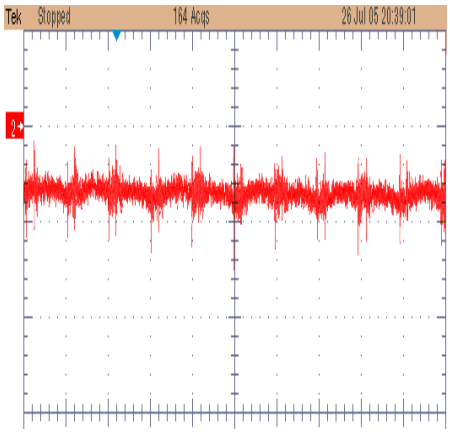
Fig. 5-16 shows the application circuit of the testing chip. Fig. 5-17 shows the photo of the testing chip demo board. Table 5-2 shows the design parameters used in the demo board. Figures 5-18~5-21 show the testing results of the demo board.

Controller	The testing chip
Channel number	2
Top device in each channel	Vishay Si4390
Bottom device in each channel	Vishay Si4368
Inductor in each channel	400nH/1mΩ ESR
Total bulk caps	8 OSCON, 220uF/5mΩ ESR
High frequency decoupling caps	18 Ceramic, 10uF/1mΩ ESR
Switching frequency	600KHz
Input voltage	12V
Target output voltage at 0 load	0.9V
Maximum output current	40A
Target Load line impedance	1 mΩ
Target output voltage tolerance band	± 20 mV
Transient emulator di/dt	10A/ns
Transient emulator pulse step	40A

Table 5-2. The design parameters used in the demo board.



a. Adaptive voltage position (Red: Vo, Blue: Io)



b. Output voltage ripple

Fig. 5-18. Voltage regulation of the testing chip demo board.

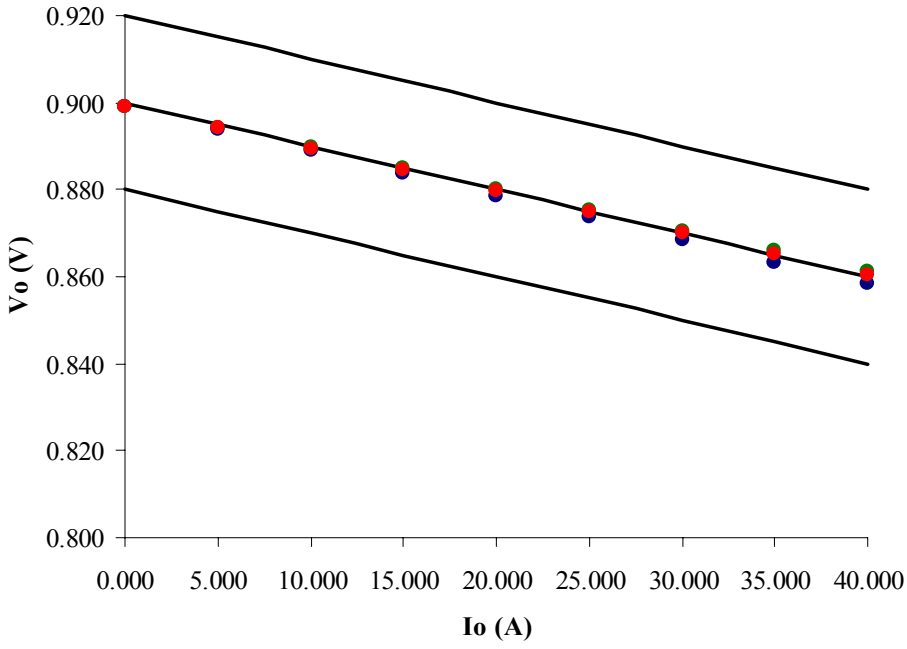
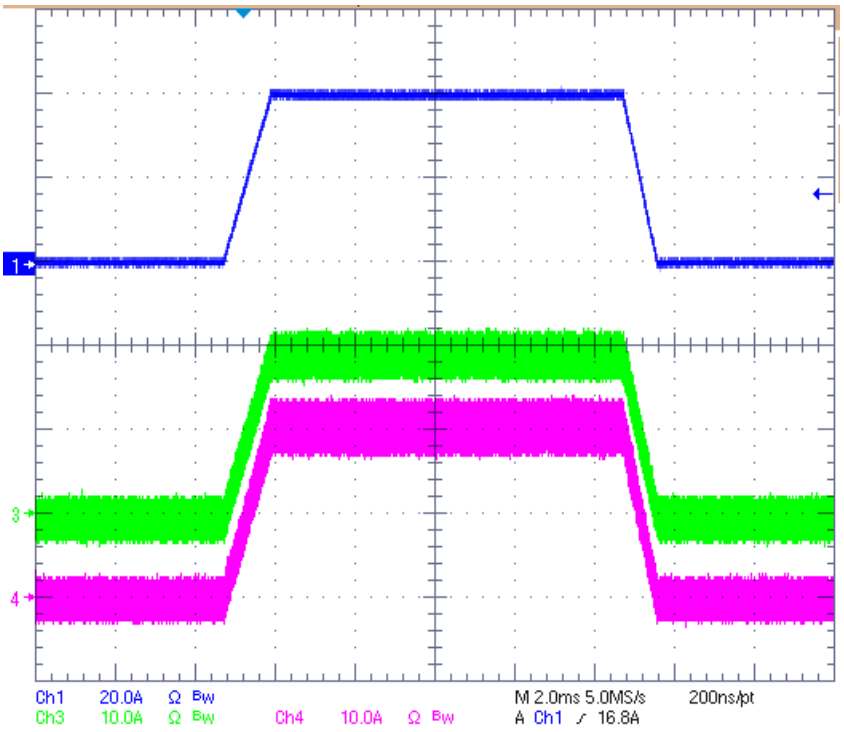
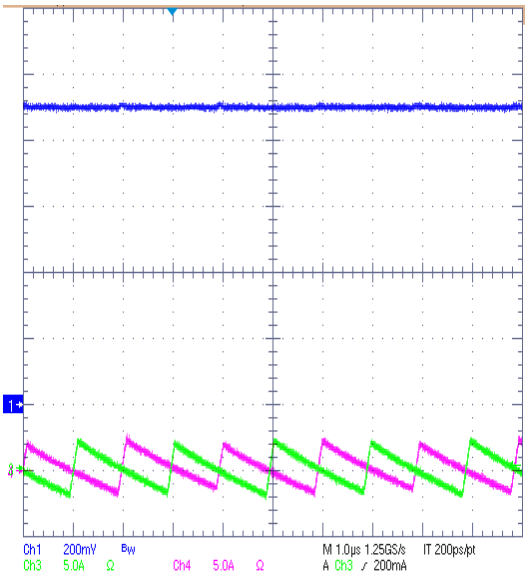


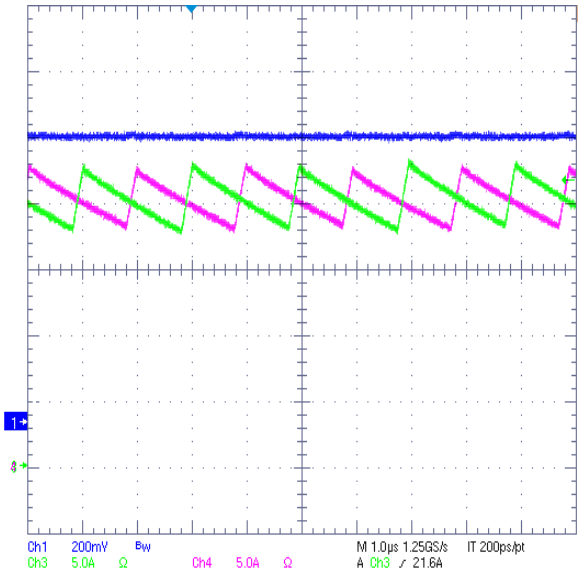
Fig. 5-19. Load lines of the testing chip demo board
(Red: DUT1, Blue: DUT1, Green: DUT3).



a. IL1, IL2 and Io
(Red: Io; Pink: IL1; Green:IL2; Blue: Io.)



b. at light load



c. at full load

(Red: Io; Pink: IL1; Green:IL2; Blue: Vo.)

Fig. 5-20. Current sharing of the testing chip demo board.

	Io = 0A		Io ≈ 40A	
	IL1	IL2	IL1	IL2
DUT1	<0.1A	<0.1A	19.89A	20.02A
DUT2	<0.1A	<0.1A	19.80A	20.11A
DUT3	<0.1A	<0.1A	20.28A	20.73A

Table 5-3. Summary of current sharing of the testing chip demo board.

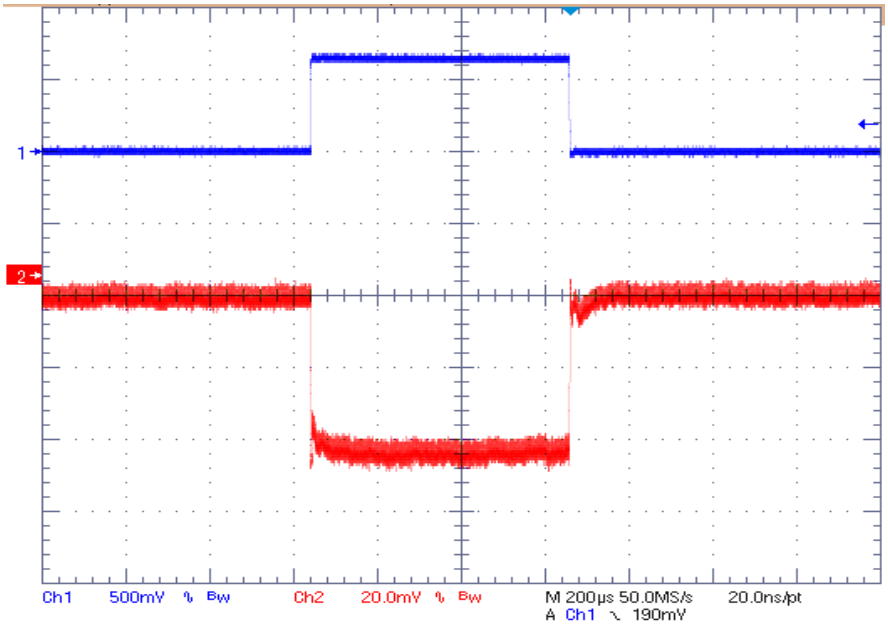


Fig. 5-21. AVP transient of the testing chip demo board.

(Red: Vo 20mV/div; Blue: Io 30A/div.)

From figures 5-18~5-12 we can see that the proposed interleaving scheme, AVP & current sharing scheme and current sensing scheme are working and the proposed analog blocks work well in the system. Even with the very low target load line impedance (1mΩ), the system achieves good interleaving, good current sharing and a well-controlled load line. The transient performance also meets today's voltage regulator design guidelines. With the technology verified by this testing chip, the real MVRC chip, as shown in Figures 5-1 and 5-2, is more than a potential.

5.7. Summary of Chapter 5

To verify the distributed control scheme and the novel analog blocks proposed in chapters 2~4, a testing chip is developed with TSMC0.5um process. The "partial tree" design approach with behavior modeling for blocks at different hierarchy levels is proposed and adopted in the development of the testing chip.

Each channel's control unit in the fabricated chip is only $1mm^2$. With the testing chip, the system achieves good interleaving, good current sharing and a well-controlled load line. The transient performance also today's voltage regulator design guidelines.

Chapter 6. Summary and Future Work

6.1. Conclusion of the Dissertation

To achieve higher power density and scalable phase design for microprocessor power management, the concept of Monolithic Voltage Regulator Channel (MVRC) is proposed in this dissertation. MVRC is a power IC with one channel converter's power MOSFETs, drivers and control circuitries monolithically integrated together based on lateral device technology and working at high frequency. It can be used alone to supply a POL (Point of Load). Without the need for a master controller, multiple MVRC chips can be used together to supply a CPU load.

To make MVRC a reality, the key is to develop a fully distributed control scheme and its analog IC circuitry to provide the control function required by microprocessor power management, which is traditionally offered by a centralized VRM controller. These functions include: interleaving, Adaptive Voltage Position (AVP) and current sharing.

To achieve interleaving, this dissertation introduces a novel distributed interleaving scheme that can easily achieve scalable phase interleaving without channel number limitation. Each channel's interleaving circuitry can be monolithically integrated without any external component. The scheme is verified by a 3-phase / 1MHz hardware prototype. The key building block is a self-adjusting saw-tooth generator, which can produce accurate saw-tooth waveforms without trimming. The interleaving circuit for each channel has two self-adjust saw-tooth generators. One behaves as a Phase Lock Loop to produce accurate phase delay, and the other produces carrier signal.

To achieve Adaptive Voltage Position and current sharing, a novel distributed control scheme adopting active droop control for each channel is introduced. Verified by hardware testing and transient simulations, the proposed distributed AVP and current sharing control scheme meets the requirements of Intel's guidelines for today and future's VR design. Monte-Carlo simulations and statistics analysis show that with the same current sensing approach, the proposed scheme has better AVP tolerance band than the traditional centralized control, and the current sharing performance is as good as traditional control.

Current sensing is critical for achieving tight AVP regulation window and good current sharing in both the traditional centralized control scheme and the proposed distributed control scheme. To improve the Signal-to-Noise Ratio, a novel current sensing scheme with an accurate V/I converter is proposed. To reduce the complexity of building an accurate V/I converter with Opamps, an accurate monolithic transconduance (Gm) amplifier with large dynamic range is developed. The proposed Gm block can achieve accurate V/I conversion without trimming.

To get further verification in silicon, the proposed schemes and analog blocks are integrated in a dual channel VR controller based on TSMC 0.5um BiCMOS process. Block testing results show that all the analog circuits proposed work as expected. System testing results show good interleaving, current sharing and AVP performance.

With the proposed schemes of current sensing, interleaving, AVP and current sharing, as well as the proposed analog circuitries, the technical barriers to build MVRC are overcome. MVRC has the potential to become a generic power IC solution for today and future POL (include CPU) power management.

6.2. Future Work

The exploration of the fully distributed control and its IC design for multiphase converter system is far from completed. Many other potential control schemes need to be addressed.

For example, to achieve AVP and current sharing, current mode control may be a good candidate. The current sharing can be achieved if all the channels share a voltage loop error signal, which comes from the voltage loop error amplifier. Where to put this error amplifier needs to be addressed. If the error amplifier is put into each MVRC chip, there will be N error amplifiers, and only one of them is working for the multiphase VR application. However, the complexity of each channel's control circuitry may be the same as the proposed "droop to each channel". The real issue of current mode control is the accuracy of current sharing. The current sharing performance of peak current control is dependent on the value of each channel's inductor, which could have 30% variation. Analog average circuits could be used to improve the current sharing performance of current mode control but the complexity of control circuitry is increased. Another issue of the peak current control is the cycle-by-cycle current sensing, which is difficult to be performed in high frequency application. However, improvement in analog design may change this conclusion. Hence high-speed analog current sensing circuit needs to be further developed.

Distributed AVP, current sharing and interleaving can also be achieved with digital control technology. The major issue of digital control is the cost of high-speed high resolution ADCs. Another issue is the die size and power consumption of the control circuitry. To reduce the die size and power consumption, digital control needs to be

implemented in deep sub-micro process, which may not be suitable for power MOSFETs. Therefore, MVRC could be a multi-die solution. All these issues need to be addressed to develop an optimal application for digital control.

This dissertation proposes the MVRC concept, which is a new chip definition based on the fully distributed control architecture. The design methodology of such generic power IC needs to be addressed. The optimal design is possible when the design methodology is clearly defined.

References

Chapter 1

[A1] G. Moore, “Cramming more components onto integrated circuits,” in Electronics, Volume 38, Number 8, April 19, 1965.

[A2] P.P. Gelsinger, P. Gargini, G. Parker and A. Yu, “Microprocessor circa 2000,” in IEEE Spectrum, Oct. 1989, pp. 43-47.

[A3] Chang Leland, Yang-Kyu Choi, J.Kedzierski, N. Lindert, Peiqi Xuan, J. Bokor, Chenming Hu, Tsu-Jae King, “Moore's law lives on,” in IEEE Circuits and Devices Magazine, Vol.19, Issue 1, Jan. 2003, pp: 35-42.

[A4] P.K. Bondyopadhyay, “ Moore's law governs the silicon revolution,” in IEEE proceedings of the Digital Object Identifier Vol.86, Issue 1, Jan. 1998 pp: 78 – 81.

[A5] “Extending and expanding Moore’s Law,” in Intel Developer Updated Magazine, April 2002, pp. 1-4.

[A6] Terrence J. McManus, “Moore’s Law & PC Power,” Presentation at Tulane Engineering Forum 2002 September 13, 2002.

[A7] Frank Kern, “Intel Desktop Power Delivery Desktop Power Delivery,” Presentation at Intel Technology Symposium 2004.

[A8] Ed Stanford, “Intel technology VR road map,” Intel Power Supply Technology Symposium, Sept. 2001.

[A9] J. Xu, X. Cao and Q. Luo, “The effects of control techniques on the transient response of switching DC-DC converters,” in Proc. IEEE PEDS, 1999, pp. 794-796.

[A10] P. Wong, F.C. Lee, X. Zhou and J. Chen, “VRM transient study and output filter design for future processors,” in Proc. IEEE IECON, 1998, pp. 410-415.

[A11] X. Zhou, X. Zhang, J. Liu, P. Wong, J. Chen, H. Wu, L. Amoroso, F. C. Lee and D. Y. Chen, "Investigation of candidate VRM topology for future microprocessors," in Proc. IEEE APEC, 1998, pp. 145-150.

[A12] Ashok Bindra , “Power-Supply ICs Go Multiphase To Take On 100-A Loads,” Electronic Design, March 4, 2002.

[A13] Intel, "VRM 9.0 DC-DC Converter Design Guidelines," available on: ftp://download.intel.com/design/Pentium4/guides/24920504.pdf
(The author visited the website on Oct.10, 2005).

[A14] R. Redl, B.P. Erisman, Z. Zansky, "Optimizing the load transient response of the buck converter," in proceeding of APEC1998, vol.1, pp. 170 – 176.

[A15] Peng Xu, "Multiphase Voltage Regulator Modules with Magnetic Integration to Power Microprocessors," Chapter 4, Ph.D dissertation of Virginia Tech, 2002

[A16] Y.Panov, M.M.Jovanovic,"Design considerations for 12-V/1.5-V, 50-A voltage regulator modules," in IEEE Transactions on Power Electronics, Vol.16, Issue 6, Nov. 2001, pp: 776-783.

[A17] S. Hamilton, " Intel research expands Moore's law," in Computer Vol.36, Issue 1, Jan. 2003, pp: 31-40.

[A18] Intersil, ISL6561 datasheet, available on:
http://www.intersil.com/data/fn/fn9098.pdf
(The author visited the website on Oct.10, 2005).

[A19] Nick X. Sun, Xiaoming Duan, Xin Zhang, Alex. Huang and Fred C. Lee, "Design of a 4 MHz, 5V to IV Monolithic Voltage Regulator Chip," ISPSD2002, pp.217-220.

[A20] Z. J. Shen, D. Okada1, F. Lin, A. Tintikakis, and S. Anderson, "Lateral Discrete Power MOSFET: Enabling Technology for Next-Generation, MHz-Frequency, High-Density DC/DC Converters," in proceeding of APEC2004, vol.1, pp. 225 – 229.

[A21] Andy Andy Burstein, "Volterra's 3 Volterra's 3rd rd Generation Generation Integrated Switching Regulators for Intel Microprocessor for Intel Microprocessor Power," Intel power Symposium 2002.

[A22] P. Rutter, "Design Challenges of Integrated Power Trains (DrMOS)," Presentation at Intel Technology Symposium 2004.

[A23] Wenkang Huang; Schuellein, G.; Clavette, D., "A scalable multiphase buck converter with average current share bus," in Proc. IEEE 18 th Annu. Applied Power Electronics Conference and Exposition (APEC'03), vol.1, 2003, pp. 438-443.

Chapter 2

[B1] Shiguo Luo, Zhihong Ye, Ray-lee Lin and Fred C.Lee, "A classification and evaluation of paralleling methods for power supply modules," in Proc. IEEE 30th Annu. Power Electronics Specialists Conf. (PESC'99), vol.2, 1999, pp. 901–908.

[B2] Intel design guideline "Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.0," Available: http://www.intel.com/design/xeon/guides/30273101.pdf (The author visited the website on Oct.10, 2005).

[B3] Pit-Leong Wong, "Performance Improvements of Multi-Channel Interleaving Voltage Regulator Modules with Integrated Coupling Inductors," Ph.D Dissertation, Dept. Elect. Eng., Virginia Tech, Blacksburg, VA, 2001.

[B4] Chang Chin, M. A Knights, "Interleaving technique in distributed power conversion systems", IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Regular Papers, vol.42, Issue 5, May 1995, pp.245 – 251.

[B5] Information from Intel roadmap Intel Developer Forum, Spring 2004.

[B6] Wenkang Huang; Schuellein, G.; Clavette, D., "A scalable multiphase buck converter with average current share bus," in Proc. IEEE 18 th Annu. Applied Power Electronics Conference and Exposition (APEC'03), vol.1, 2003, pp. 438-443.

[B7] Xin Zhang, Alex Q.Huang, "Investigation of VRM controllers", Proc. IEEE The 16th International Symposium on Power Semiconductor Devices and ICs, . (ISPSD'04), 2004, pp. 51-54.

[B8] Intersil Corporation, HIP6301 datasheet, Available on: Http://www.intersil.com/data/fn/fn4765.pdf (The author visited the website on Oct.10, 2005).

[B9] B. A. Miwa, "Interleaved conversion techniques for high density power supplies," Ph.D. dissertation, Dept. Elect. Eng. Comput. Sci., Mass. Inst. Technology, 1992.

[B10] D.J.Perreault, J.G Kassakian, "Distributed interleaving of paralleled power converters," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Regular Papers, vol.44, Issue 8, Aug. 1997, pp.728–734.

[B11] Liang Feng; Qu Wenlong, “Implementation of an automatic interleaving approach for parallel DC/DC converter without interleaving bus,” in Proc. IEEE Sixth International Conference on Electrical Machines and Systems, (ICEMS’03), vol.1, 2003, pp.368-371.

[B12] T. Rahal-Arabi, G. Taylor, M. Ma, C. Webb, “Design & Validation of the Pentium III and Pentium 4 Processors Power Delivery,” in Digest of Technical Papers of Circuits Digest of Symposium on VLSI, Jun. 2002, pp 220-223.

Chapter 3

[C1] Kaiwei Yao, Yuancheng Ren, F.C.Lee, “Critical bandwidth for the load transient response of voltage regulator modules,” IEEE Transactions on Power Electronics, Volume 19, Issue 6, Nov. 2004 Page(s): 1454 – 1461.

[C2] A..Waizman, Chee-Yee Chung, “Resonant free power network design using extended adaptive voltage positioning (EAVP) methodology,” IEEE Transactions on Advanced Packaging, Volume 24, Issue 3, Aug. 2001 Page(s):236 – 244.

[C3] A. Hasan, A. Sarangi, A. Sathe, G.Ji, “High Performance Mobile Pentium III Package Development and Design,” in Proceedings of Electronic Components and Technology Conference, 2002, pp:378 - 385.

[C4] T. R. Arabi, G. Taylor, M. Ma, C.Webb, “Design & Validation of the Pentium III and Pentium 4 Processors Power Delivery,” in Proceedings of Symposium on VLSI Circuits 2002, pp: 220-223.

[C5] Tawfik Rahal-Arabi, Greg Taylor, Matthew Ma, Jeff Jones and Clair Webb, "Design and Validation of the Core and IOs Decoupling of the Pentium® III and Pentium® 4 Processors," in Proceedings of Topical Meeting on Electrical Performance of Electronic Packaging, October 2002 pp.249-252.

[C6] Y. L. Li , David G. Figueroa, Shamala A. Chickamenahalli, Chee Yee Chung, Teong Guan Yew, Michael D. Cornelius, Huong T. Do, “Enhancing power distribution system through 3D integrated models, optimized designs, and

switching VRM model," Proceedings on Electronic Components and Technology Conference, 2000, pp:272 – 277.

[C7] Richard Redl, etc. , "Voltage Regulator Compensation Circuit and Method," US patent 6229292 B1.

[C8] "The AVP load line of CPU silicon die is optimized based on the tradeoff between CPU thermal cost and CPU performance."

[C9] Xin Zhang; A..Q. Huang, N.X. Sun, "Microprocessor power management integration by VRB-CPU approach," in proceeding of PESC2003, vol.2, pp:875 – 880.

[C10] Intel, "VRM 9.0 DC-DC Converter Design Guidelines," available on:
ftp://download.intel.com/design/Pentium4/guides/24920504.pdf
(The author visited the website on Oct.10,2005).

[C11] Intel, "VRM 9.1 DC-DC Converter Design Guidelines," available on:
ftp://download.intel.com/design/Xeon/guides/29864601.pdf
(The author visited the ftp website on Oct.10, 2005).

[C12] Intel, "Voltage Regulator-Down (VRD)10.0 Design Guide For Desktop Socket 478," available: ftp://download.intel.com/design/Pentium4/guides/25288503.pdf
(The author visited the ftp website on Oct.10, 2005).

[C13] Intel, "Voltage Regulator-Down (VRD) 10.1Design Guide For Desktop LGA775 Socket," available on:
ftp://download.intel.com/design/Pentium4/guides/30235604.pdf
(The author visited the ftp website on Oct.10, 2005).

[C14] Intel, "Voltage Regulator Module (VRM) and Enterprise Voltage Regulator-Down (EVRD) 10.0 Design Guidelines," available on:
ftp://download.intel.com/design/Xeon/guides/30273102.pdf
(The author visited the ftp website on Oct.10, 2005).

[C15] Information from Intel symsium 2005.

[C16] David Ricketts, "Current Sensing for Multi-phase CPU DC-DC converters," presentation at IBM power technology symposium 2002.

[C17] Analog Devices, Inc., ADP3160 datasheet. Available on:
http://www.analog.com/UploadedFiles/Data_Sheets/14824600ADP3160_67_b.pdf

(The author visited the website on Oct.10, 2005).

[C18] Fairchld Semiconductor, Inc., FAN5093 datasheet. Available on:
http://www.fairchildsemi.com/ds/FA/FAN5093.pdf
(The author visited the website on Oct.10, 2005).

[C19] Eric X. Yang etc. "High-speed Charge-mode Controller for a Multi-phase Switched-mode Power Converter", US patent 6462521 B1.

[C20] Intersil Corporation, HIP6301 datasheet. Available on:
http://www.intersil.com/data/fn/fn4765.pdf
(The author visited the website on Oct.10, 2005).

[C21] Analog Devices, Inc., ADP3180 datasheet. Available on:
http://www.analog.com/UploadedFiles/Data_Sheets/426634141ADP3180_a.pdf
(The author visited the website on Oct.10, 2005).

[C22] On Semiconductor, Inc, CS5307 datasheet. Available on:
http://www.onsemi.com/pub/Collateral/CS5307-D.PDF
(The author visited the website on Oct.10, 2005).

[C23] Xin Zhang, Gary Yao, Alex Q. Huang, " A Novel VRM control with direct load current feedback", in Proceeding of APEC 2004. Vol.1, pp: 267 – 271.

[C24] Kaiwei Yao etc, " Adaptive Voltage Position Design for Voltage Regulators", in Proceeding of IEEE APEC 2004, vol.1, pp:272 – 278.

[C25] Michael M. Walters etc., "DC-to-DC Converter with Inductor Current Sensing and Related Methods", US patent 5982160.

[C26] Patrice R. Lethellier etc. "Method and Apparatus for Sensing Output Inductor Current in a DC-to-DC Power Converter", US patent 6441597 B1.

[C27] Kaiwei Yao, Yu Meng, Peng Xu, F.C.Lee, "Design considerations for VRM transient response based on the output impedance," in Proceeding of APEC 2002, vol.1, pp:14-20.

[C28] K. Yao, K. Lee, M. Xu, F.C.Lee, "Optimal design of the active droop control method for the transient response," in proceeding of APEC 2003, Volume 2, pp:718 – 723.

[C29] R.Redl, N.O.Sokal, "Current-Mode Control, Five Different Types, Used with the Three Basic Classes of Power Converters: Small-signal AC and Large-signal DC

Characterization, Stability Requirements, and Implementation of Practical Circuits," in proceeding of PESC1985, pp: 771-785.

[C30] Jung-Won Kim, Hang-Seok Choi, Bo Hyung Cho , "A novel droop method for converter parallel operation," IEEE transactions on power electronics, Vol.17, Issue 1, Jan. 2002 pp:25 - 32 .

[C31] Brian T.Irving, Milan M. Jovanovic, "Analysis, design, and performance evaluation of droop current-sharing method," in proceding of APEC2000, Vol.1, pp: 235 – 241.

[C32] Enrico Dallago, "improvements in voltage regulation and current sharing with the droop function," EPE2001.

[C33] A. Papoulis, etc. "Probability, Random Variable, and Stochastic Processes", 4th Edition, 2002.

[C34] Frank Kern, etc. "Intel VRD processor Voltage and Circuit Specifications," presentation at Intel technology symposium 2003.

[C35] Frank Kern, etc. "Intel VRD processor Voltage and Circuit Specifications," presentation at Intel technology symposium 2003.

[C36] Xin Zhang, Alex Huang, "Fully distributed AVP and current sharing scheme for scalable multiphase Voltage regulator," will be published in APEC2006.

Chapter 4

[D1] Analog Device, ADP3160 datasheet, available on: http://www.analog.com/UploadedFiles/Data_Sheets/14824600ADP3160_67_b.pdf (The author visited the ftp website on Oct.10, 2005).

[D2] Ray Ridley, "VRM current sensing," Switching Power Magazine, 2002.

[D3] R. Lenk, "Application Bulletin AB-20 Optimum Current-Sensing Techniques in CPU Converters", Fairchild Semiconductor Application Notes, 1999.

[D4] E. Dallago, M. Passoni and G. Sassone, "Lossless Current Sensing in Low Voltage High Current DC/DC Modular Supplies", IEEET Trans. Industrial Electronics, vol. 47, pp. 1249-1252, Dec. 2000.

[D5] Rober H.Isham, etc., "Synchronous-Rectified DC to DC Converter with Improved Current Sensing," US patent 6246220 B1.

[D6] P. Gray, P. Hurst, S. Lewis and R. Meyer, Analysis and Design of Analog Integrated Circuits, Wiley, New York, 2001.

[D7] S. Yuvarajan, L. Wang, "Power conversion and control using a current sensing power MOSFET," in IEEE Proceedings of the 34th Midwest Symposium on Circuits and Systems, vol.1, May 1991, pp: 166-169.

[D8] B.Bryant, M.K. Kazimierczuk, "Effect of a current-sensing resistor on required MOSFET size," IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, Vol. 50, Issue 5, May 2003, pp: 708 – 711.

[D9] Y. Xiao, J. Cao, J.D.Chen, K.Spring, "Current sensing trench power MOSFET for automotive applications," in IEEE Proceedings of APEC 2005, Vol.2, pp: 766-770.

[D10] S.Yuvarajan, "Performance Analysis and Signal Processing in a Current Sensing MOSFET (SENSEFET)", in Proc. Industry Applications Society Annual Meeting, vol. 2, pp. 1445 – 1450, 1990.

[D11] P. Givelin, M. Bafleur, "On-Chip Over Current and Open Load Detection for a Power MOS High Side Switch: A CMOS Current Source Approach", in Proc. Fifth European Conference on Power Electronics and Applications, vol. 2, pp.197-200, 1993.

[D12] S. Yuvarajan and L. Wang, "Power Conversion and Control using a Current Sensing MOSFET", in Proc. 34th Midwest Symposium on Circuits and Systems, vol. 1, pp.166–169,1992.

[D13] D. Grant and R. Pearce, "Dynamic Performance of Current-Sensing Power MOSFETs", Electronic Letters, pp. 1129-1131, Sept. 1988.

[D14] D. Grant and R. Williams, "Current Sensing MOSFETs for Protection and Control", IEE Colloquium on Measurement Techniques for Power Electronics, pp. 8/1-8/5,1992.

[D15] Nobumasa Ueda, "Load Current Supply Circuit Having Current Sensing Function,"US patent 5877617.

[D16] Bruce Lee Inn, "Reference-Corrected Ratiometric MOS Current Sensing Circuit," US patent 6304108 B1.

[D17] P. Midya, M Greuel and P. Krein, “Sensorless Current Mode Control-An Observer Technique for DC- DC Converters”, IEEE Trans. Power Electronics, vol. 16, pp. 522 –526, July 2001.

[D18] Xunwei Zhou, etc. “Current sensing and current sharing,” US patent 6414469 B1.

[D19] X. Zhou and P. Xu, “A Novel Current-Sharing Control Technique for Low-Voltage High-Current Voltage Regulator Module Applications”, IEEE Trans. Power Electronics, vol. 15, pp. 1153-1162, Nov.2000.

[D20] Hassan Pooya Forghani-zadeh, Gabriel A. Rincón-Mora, “Current-Sensing Techniques for DC-DC Converters,” in Proc. 45th Midwest Symposium on Circuits and Systems, 2002. pp:577-580.

[D21] Andy Andy Burstein, “Volterra’s 3 Volterra’s 3rd rd Generation Generation Integrated Switching Regulators for Intel Microprocessor for Intel Microprocessor Power,” Intel power Symposium 2002.

[D22] Behzad Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill Higher Education, 2001, ISBN:0-07-238032-2.

[D23] Intersil ISL6566 datasheet, available: http://www.intersil.com/data/fn/fn9178.pdf (The author visited the website on Oct.10, 2005).

[D24] Patrice R. Lethellier, “Method and apparatus for sensing output inductor current in a DC-to-DC power converter,” US patent 6441597 B1.

[D25] Sergio Franco, Design with Operational Amplifiers, McGraw-Hill, 2001, ISBN: 0072320842.

[D26] Jerry Steele, Tim Green, “Tame Those Versatile Current-Source Circuits,” Electronic Design Magazine, Oct.15, 1992.

[D27] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, Wiley-IEEE, 1997, ISBN: 0780334167

[D28] H. Khorramabadi, “High frequency CMOS continuous time filters,” Ph.D. dissertation, University of California, Berkeley, 1985.

[D29] A.T. Van Zanten, J.H.Huusing, “An Accurate Integrated Voltage-to-Current Converter”, IEEE JOURNAL OF SOLID- STATE CIRCUITS, VOL. SC 10, NO. 6, DECEMBER 1975.

[D30] Katsuji Kimura, “A Linear Transconductance Amplifier Obtained by Realizing a Floating Resistor”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, VOL. 45, NO.1, JANUARY 1998.

[D31] Keng Leong Fong, “High-Frequency Nonlinearity Analysis of Common-Emitter and Differential-Pair Transconductance Stages”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 33, NO. 4, APRIL 1998.

[D32] E.Sanchez-Sinencio, J.Silva-Martinez, “CMOS transconductance amplifiers, architectures and active filters: a tutorial”, IEE Proc.-Circuits Devices Syst., Vol. 147, No. 1, February 2000.

[D33] H. Elwan, W. Gao, R. Sadkowski and M. Ismail, “CMOS low-voltage class-AB operational transconductance amplifier”, ELECTRONICS LETTERS Vol. 36 No. 17 August 2000.

[D34] Bahram Fotouhi,, “All-MOS Voltage-to-Current Converter”, IEEE JOURNAL OF SOLID- STATE CIRCUITS, VOL. 36, NO. 1, JANUARY 2001.

[D35] Uma Chilakapati, “A CMOS Transconductor With 80-dB SFDR up to 10 MHz”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 37, NO. 3, MARCH 2002.

[D36] David Johns, Ken Martin, Analog Integrated Circuit Design, Wiley,1996, ISBN: 0471144487.

[D37] “Current-mode circuit from a translinear viewpoint: a tutorial.” In C. Toumazou, F.J. Lidgey and D.G. Haigh (Eds.) Analog IC Design: the Current-mode Approach, Institution of Electrical Engineers; Repr. with Minor Corrections June 1990 edition, ISBN: 0863412157.

Chapter 5

[E1] James R. Armstrong, F. Gail Gray, VHDL Design Representation and Synthesis, Prentice-Hall, 2000, ISBN: 0130216704

[E2] Alan Hastings, The Art of Analog Layout, Prentice-Hall, 2001, ISBN: 0130870617.

[E3] Paul Brokaw, “A simple three-terminal IC bandgap reference”, IEEE JOURNAL OF SOLID-STATE CIRCUITS, vol.sc-9, no.6, 1974, pp.381-393.

Vita

The author, Xin Zhang, was born in Guiyang, China. He received his B.S. degree and M.S. degree in electrical engineering from Zhejinag University, Hangzhou, China, in 1994, and 1997 respectively.

From 1997 to 2000, he was an electrical engineer at Zhongxing telecom LTD. (ZTE) in Shenzhen, China. Begin from September 2000, Mr. Xin Zhang works as a research assistant in Center of Power Electronics System (CPES) of Virginia Tech to pursue his Ph.D. degree. His research forces on the Voltage Regulators and their analog IC design for microprocessor power management.