MICROPROCESSOR-BASED SYSTEM FOR THE DETECTION AND CHARACTERIZATION OF ACOUSTIC EMISSIONS FOR MATERIALS TESTING

by

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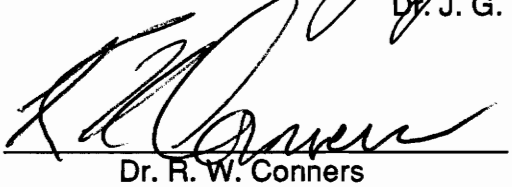
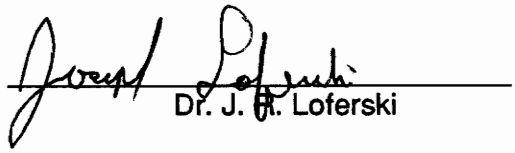
APPROVED:

Dr. J. G. Tront, Chairman



Dr. R. W. Conners



Dr. J. R. Loferski

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Abstract

This document explains the design of the Acoustic Emission Detection and Characterization System (AEDCS). The AEDCS is capable of recording several Acoustic Emmision (AE) characteristics including AE event peak amplitude, duration, frequency, and time of occurrence. The analog and digital circuits designed to implement these functions are monitored and controlled by a microprocessor system. The microprocessor system processes and records the AE event information, and passes it to a host computer for mass storage and further manipulation. The AEDCS is the first low cost, self-contained device that records these AE characteristics in real-time.

The AEDCS is designed to be used in the AE testing of materials. It is well-suited for non-destructive applications that produce a relatively low AE count rate, such as AE monitoring of wooden structures. The AEDCS is also capable of recording AE event characteristics in destructive test applications. The results of using the AEDCS in a mechanical loading test application on several different types of wood are given here as well.

Acknowledgements

I wish to express my sincere gratitude and appreciation to Dr. J. G. Tront for his guidance, suggestions, and encouragement which made this project a possibility. I would like to thank Dr. J. R. Loferski for his suggestions and encouragement, and Dr. Conners for his time and attention as a member of my graduate committee. I would like to thank Dr. C. Skaar for the opportunity to work on this project.

I wish to express my gratitude to Jai Keswani for all her constant support and encouragement and to my parents, to whom I dedicate this work.

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Chapter I

INTRODUCTION

1.1 Overview of Acoustic Emission

Acoustic Emission (AE) is defined as the "class of phenomena where by transient elastic waves are generated by the rapid release of energy from localized sources within material, or the transient elastic waves so generated" [1]. For a material such as wood under stress, an AE is generated at points of fracture or friction, causing an elastic stress or strain wave to be generated [2]. AE in wood can be caused by mechanical damage processes such as mechanical strains, or passive damage processes such as the tearing of cell walls during drying [3]. These AEs are typically bursts of high frequency sound waves in the ultrasonic range [4]. The acoustic waves can be transformed into an electrical signal for instrumentation purposes by a mechano-electro transducer such as a piezo-crystal sensor.

Figure 1-1 illustrates some of the characteristics used to describe an AE. Also labelled on the diagram is a constant voltage level, called the threshold, that is used to derive several of the characteristics. The number of threshold crossings by an AE event are called ring-down counts [5]. The duration of an AE event can be defined as the time between the initial rise of AE energy above the threshold and the time at which the AE energy decays below the threshold. The peak amplitude is the absolute value of the highest voltage obtained by a single AE event. The time between the initial crossing of the threshold and the time at which the peak amplitude occurs is called the rise time, and the rise time slope is the peak amplitude minus the threshold voltage divided by the rise time [5]. An actual AE signal may contain many frequency components, but the principle frequency is defined by the period of the AE wave as shown in figure 1-1. It should be noted that this period may not be constant throughout the AE wave, but may provide useful information if measured consistantly for all AE events. The frequency defined here is the inverse of the period of the first cycle measured following the peak amplitude, as shown in figure 1-1.

The DC envelope of the AE event is also shown in figure 1-1, and is derived by full-wave rectifying and low-pass filtering the AE signal. A more detailed description of this signal and its derivation is discussed in Chapter 2, but it should be noted here that several of the afore mentioned characteristics can also be derived from this DC signal. For example, the duration can be derived by a simple voltage comparator circuit that compares the DC envelope to the threshold voltage. Deriving the duration from the AC signal would entail a more complex circuit. Using the DC envelope to get the peak

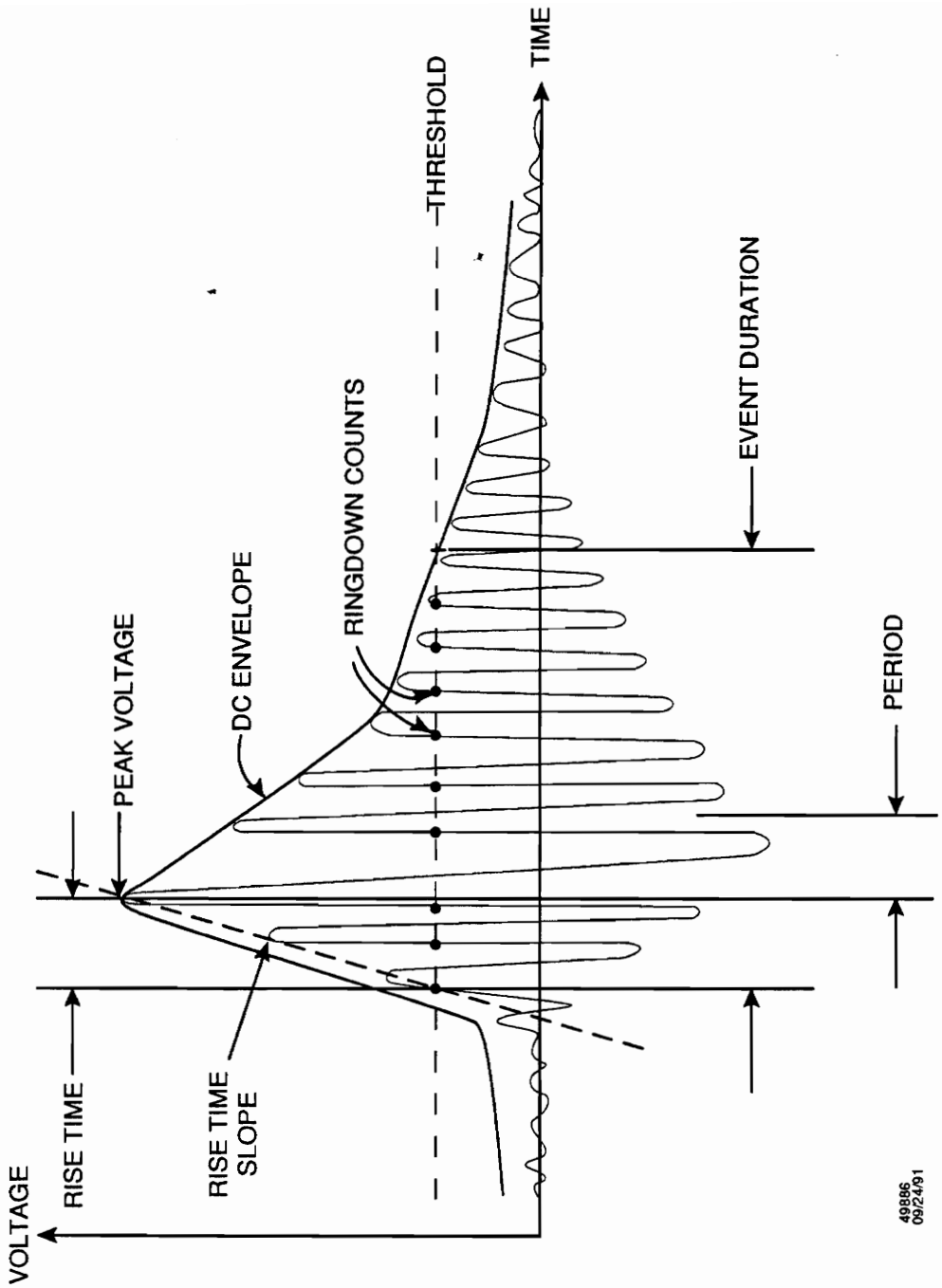

Figure 1-1. Diagram of an Acoustic Emission Event

amplitude also reduces the speed constraints of the peak detection circuit. This speed constraint reduction results from the elimination of high frequency content in the DC signal as compared to the AC signal.

Any number of these AE parameters can be used to characterize AEs for a given application. Some parameters may not prove to be useful for certain applications, while others may be impractical to obtain because of the prohibitive cost of the necessary instrumentation. Still other parameters that are not mentioned here may prove useful. Much research has been done with AEs, and the following section discusses some of the applications and AE characterization parameters that have been used.

1.2 Literature Review

Much of the current research utilizes counting techniques to characterize AEs. The rate of ring-down counts and the cumulative total counts have been the most widely used methods. AE count rate provides a good indication of AE occurences and a non-specific indication of AE energy content. This is due to the fact that a high energy AE event will have more ring-down counts than a lower energy AE, and therefore a high rate of ring-down counts indicates either the occurence of high energy AEs or the quick succession of many AE events, or a combination of both. The ringdown method does not differentiate between these two causes and provides no other AE

characteristic information. However, in instances where a high rate of AE events occur, this method has been sufficient.

Sato, et al. [6] used AE count rate to study the fracture mechanism of wood. They recorded AE count rate generated during several different types of mechanical loading and correlated the data with their predictions. The count rate method proved successful for them as they were able to observe different effects from each type of loading of the wood.

Ansell [7] used the count rate method to compare the effects of one type of mechanical loading on several different samples of wood and man-made composites. He was successfull in distinguishing between different species of wood by their AE count rate characteristics, and he concluded that AE testing provides an insight into the state of internal stress and processes of energy release in wood. [7]

Ogino, et al. [8] attempted to predict the mechanical damages in wood during drying by examining the intensity and frequency spectrum of AE events. Energy intensities were determined by classifying the peak voltages of AE events into six different ranges. They also recorded the AE events and analyzed them later on a spectrum analyzer. They were successfull in correlating their AE intensity data to mechanical damages in wood. They were also able to notice some trends from the frequency spectrum data, although not as conclusively as the intensity correlations.

Noguchi, et al. [9] also studied the characteristics of AE generated during wood

drying. They recorded AE cumulative event count, AE count rate, amplitude distribution of AE events, and the waveform and spectrum of AE signals for two species of wood during drying. Again, the count rate and cumulative count data showed good correlations for different species, but the amplitude data appeared constant irrespective of species and drying time. They confirmed that the AE signals were burst type waves but did not correlate the AE event duration and frequency spectrum to anything. They also suggested that their frequency spectrum data was related to the resonant frequency of the piezo-crystal used.

Skaar, et al. [10] and Kitayama, et al. [20] used AE count rate as a control parameter in the drying of wood. They used a microcomputer to control a dry kiln and monitor AE data, and used feedback schemes to optimize the drying process without causing mechanical damages usually associated with faster drying times. Both studies concluded that feedback control of the drying process using AE monitoring is possible.

Quarles [11] reported on his initial analysis of wood drying using several time domain parameters, including ring-down counts, count rate, peak amplitude, rise time, event duration, and a measure of AE energy, but he then limited his analysis to include only count rate and peak amplitude. He concluded that AE peak amplitude measurement provided useful information for monitoring mechanical damages in wood.

As stated above, much research has been done on AE testing, and most have used an AE count rate method for characterizing AE activity. Others have studied AE waveform and frequency spectrum data, all with varying methods and results. None

have reported on a single detection system that provides real-time measurement of the peak amplitude, event duration, and frequency of AE events.

1.3 Organization of the Thesis

This thesis will provide a detailed discussion of the hardware design, software design, and operation of the AE detection and characterization system. The results of implementing the system in a mechanical testing application on wood are also presented here, and a conclusion is given to summarize the thesis and to provide directions for future research.

Chapter 2 is a detailed discussion of the system's hardware. A list of functional requirements of the system is given, and the hardware implementation of these requirements is discussed by partitioning the hardware into several blocks and describing each block in detail. The results of the design verification tests are also given in this chapter.

Chapter 3 is a detailed discussion of the system's software. The sofware is also partitioned into several blocks, and a description of all of the routines associated with each block is given. Operation of the microprocessor's interface to the system hardware is provided in this chapter.

Chapter 4 is a users manual that describes the setup and use of the system in a typical AE test application. This chapter documents all of the system specifications.

Chapter 5 discusses the results of implementing the system in a mechanical test of wood. A description of the test setup and procedure is given, and the emperical results are discussed.

Finally, the conclusion is provided in Chapter 6. The conclusion summarizes the thesis and discusses possible directions for future research.

Chapter II

HARDWARE

2.1 Functional Requirements

The objective of this thesis is to design a system that will detect and characterize AE events. The system is designed to meet the following requirements:

1. Detect an AE event and record the following information:
    - Peak amplitude, in volts
    - Duration, in microseconds
    - Frequency, in kHz
    - Time of occurence, in seconds

    The above characteristics were all defined in section 1.1 except the time of occurence, which is measured relative to the start of the test. The system only records AE events of sufficient peak amplitude which is user specified.

2. Simultaneously record 7 A/D inputs when an AE event occurs. This provides the user with additional instrumentation capabilities.

3. User alterable D/A voltage outputs to set the minimum peak voltage for

system detection and to set the threshold voltage for the frequency detection circuit.

4. RS-232 serial interface. AE tests are initiated by commands sent through this interface, and all output is sent back to a controlling computer through this interface.

A description of the hardware implementation of these requirements follows, along with the hardware specifications and calibration results. A description of the software is in Chapter 3.

2.2 Implementation

Figure 2-1 is a block diagram of the system hardware. It shows that the hardware can be partitioned into the following sections:

1. Piezo-crystal transducer
2. Amplifier and filter
3. Signal derivation circuits
4. Microprocessor system

Each of these sections is described below in detail.

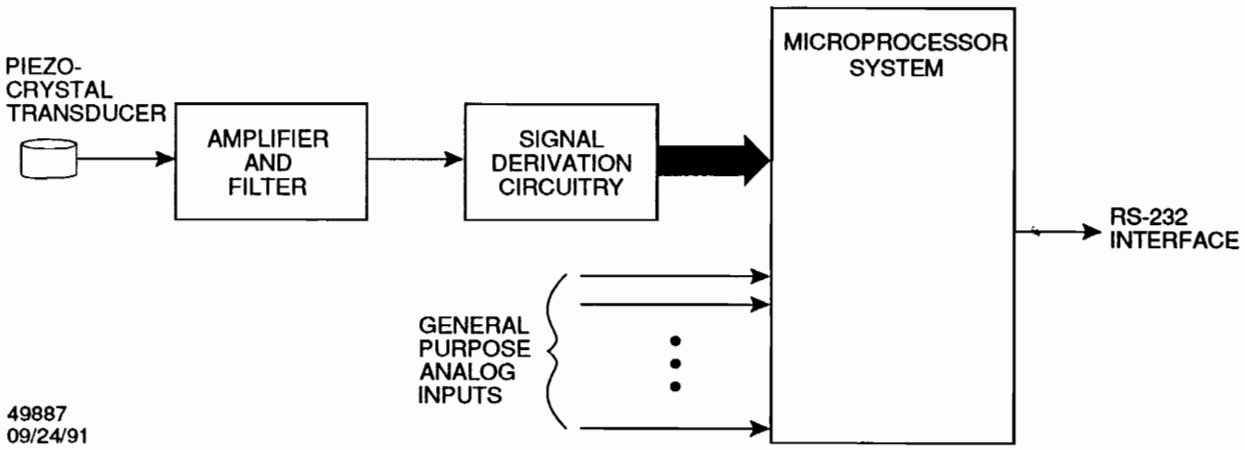

Figure 2-1. System Hardware Block Diagram

2.2.1 Piezo-Crystal Transducer

A piezo-electric transducer is used to convert the mechanical AE energy into an electrical voltage. The transducer used is a model AC175L from the Acoustic Emission Technology corporation in Sacramento, California. It has a sensitivity of -68 dB referred to 1 volt per µBar which means that 398 µvolts are produced for every µBar of pressure applied to the transducer at it's resonant frequency. The transducer has a resonant frequency of 175 kHz and a bandwidth of 100kHz to 300kHz. The bandwidth of the transducer is determined by measuring the frequencies above and below the resonant frequency at which the output voltage falls 3 dB below the output voltage measured at the resonant frequency.

2.2.2 Amplifier and Filter

The transducer output voltage is typically in the hundreds of microvolts range for a typical AE measured in wood. This signal requires considerable amplification and filtering before the signal derivation circuits can use it. Sheet 1 of the schematic diagram contained in Appendix B shows the amplifier and filter stages.

The output of the transducer is fed into the first stage of amplification, which consists of a passive RC high pass filter network and a non-inverting buffer/amplifier. The high pass filter network is a first-order resistor-capacitor (RC) circuit with a corner frequency at 25 kHz and a high-frequency attenuation (rolloff) of 20 dB per decade.

This filter helps to eliminate any low-frequency interference such as 60 Hz hum from AC power sources. The buffer/amplifier provides 40 dB of gain using an LH0032 op-amp in a non-inverting configuration. The input impedance of the LH0032 is on the order of $10^{12}\Omega$.

The second stage consists of another high pass filter and an inverting op-amp amplifier. The high pass filter has the same corner frequency and first-order rolloff characteristics as the first stage, providing a combined second-order rolloff of 40 dB per decade. This filter provides additional low-frequency interference rejection and also decouples any DC offset voltage from the first stage. The amplification of the second stage is 40 dB, and uses an LH0032 in an inverting configuration.

The LH0032 is used because of its high input impedance, high slew rate and wide bandwidth [13]. Both LH0032 op-amps have been compensated with a 5 pf capacitor for stabilization [14]. This compensation results in a high frequency rolloff at 500 kHz, which is well above the transducer's bandwidth.

2.2.3 Signal Derivation Circuits

The amplified and filtered AE signal is then used to derive the signals needed to characterize the AE event. A block diagram of these signal derivation circuits is shown in figure 2-2. From this diagram, the signal derivation circuits can be partitioned into the following sections:

1. AC to DC converter
2. Peak detector
3. Duration detector
4. Frequency detector

These sections are described in detail below.

2.2.3.1 AC to DC Converter

The AC to DC converter transforms the AC signal into a DC signal that resembles the envelope of the AE signal. As described in section 1.1, the DC signal is used in the peak and duration detection circuits. Sheet 2 of the schematic diagram in Appendix B shows the AC to DC converter. Figure 2-3 shows a sample waveform at the input to the AC to DC converter and at various points inside the circuit.

The converter consists of two stages. The first stage is a negative half-wave rectifier built around an LF353 op-amp. This stage inverts all of the positive peaks of the AE signal but does not pass any of the negative peaks, as shown in figure 2-3b. The second stage sums the original AE signal with twice the negative half-wave rectified signal, resulting in a negative full-wave rectified signal (figure 2-3c). The second stage then inverts the signal providing a positive full-wave rectified signal. The second stage is also a low-pass filter which reduces the AC peaks into a smoother DC voltage, as shown in the output signal in figure 2-3d. [15]

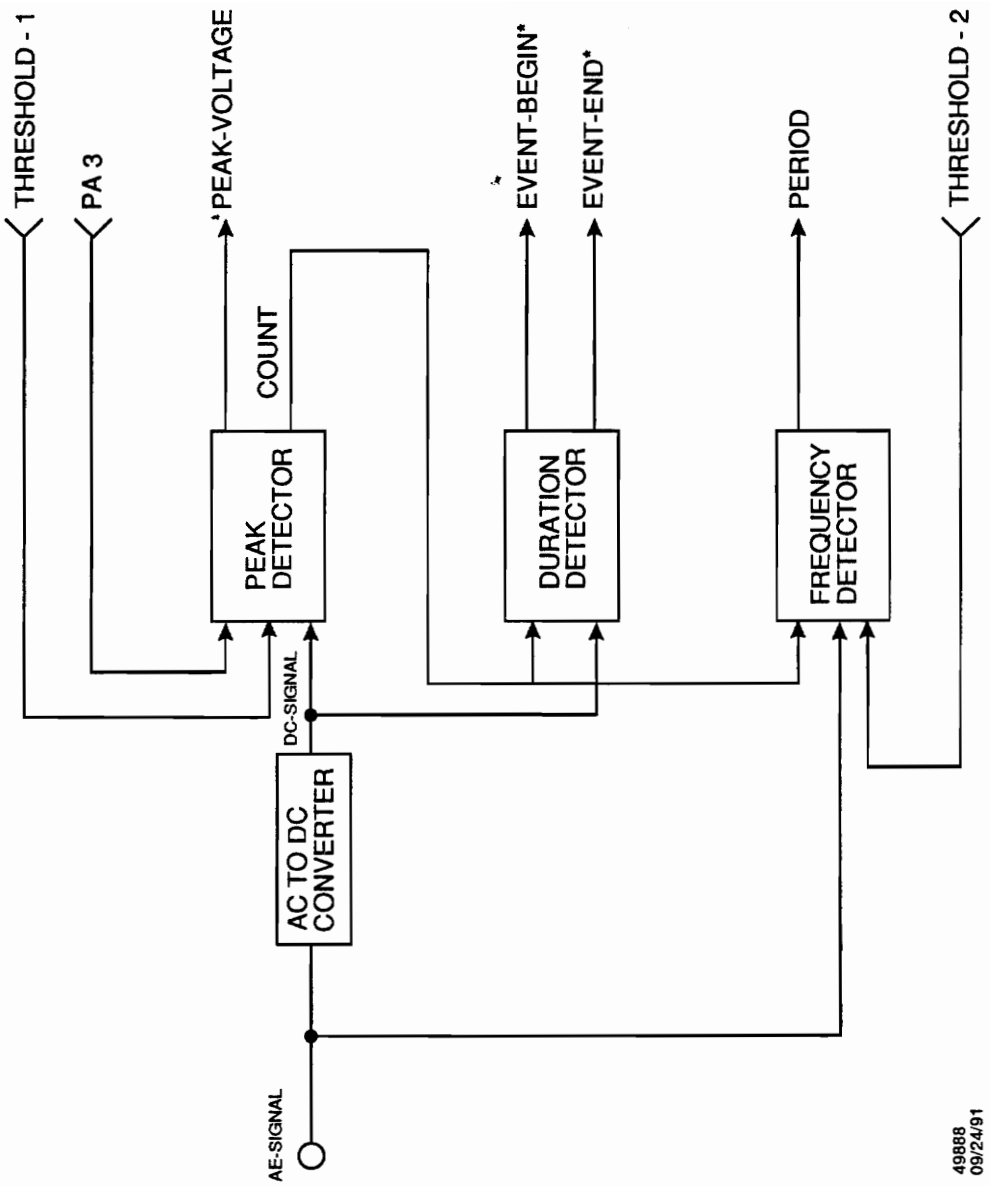

Figure 2-2. Signal Derivation Block Diagram

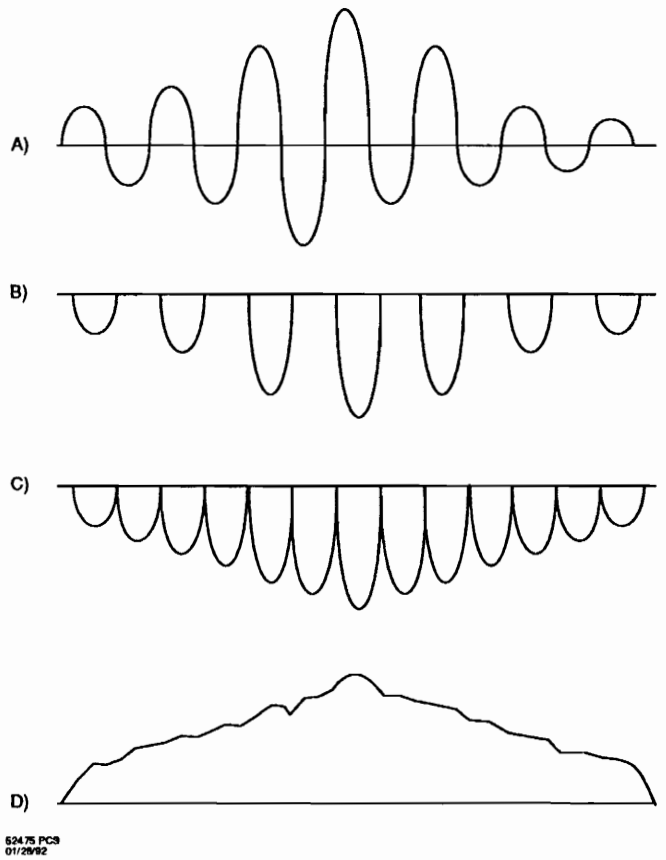

Figure 2-3. AC to DC Converter: (a) Sample input to the AC to DC converter. (b) signal at ouput of first op-amp. (c) summed signal at input of second op-amp. (d) output of converter.

2.2.3.2 Peak Detector

The peak detector provides two signal outputs: PEAK-VOLTAGE and the COUNT signal. The PEAK-VOLTAGE signal is sent to the microprocessor's A/D converter to be recorded, and the COUNT signal is used in the derivation of other signals. Sheet 3 of the schematic diagram shows the peak detector circuit.

The AE peak amplitude is detected by a PKD-01 integrated circuit (IC). The DC signal is fed into the input of the PKD-01. The DET* (the trailing asterisk on a signal name indicates an active-low signal) input is tied low, causing the IC to continuously detect the peak of the voltage on its input. The PKD-01 holds the peak voltage on its output until the RESET line goes high. The RESET line is tied to the microprocessor digital output PA3, which is pulsed high by the software to reset the peak voltage after it has been read by the A/D converter.

The output of the PKD-01 is then scaled down by a two stage op-amp circuit that divides the signal by 3. This allows the voltage to be read by the A/D converter which has an input voltage limitation of 5V max. The software rescales the conversion result by 3 to obtain the original peak voltage.

The output of the PKD-01 is also sent to a comparator circuit to derive the COUNT signal. COUNT is asserted high when the peak voltage rises above a threshold voltage which is set by the microprocessor's D/A converter. A high output on COUNT signifies that an AE event is of sufficient peak amplitude to be recorded. The duration and frequency detectors use the COUNT signal to derive their output signals.

2.2.3.3 Duration Detector

The duration detector provides two output signals: EVENT-BEGIN* and EVENT-END*. These signals are used to trigger input capture lines on the microprocessor timer. The duration detector circuit is shown on sheet 4 of the schematic diagram.

The duration detector consists of a comparator circuit and a NAND gate. The comparator is an LM339 used in an inverting configuration with hysteresis. The comparator output will go low when the DC-SIGNAL level rises above .5V, and the hysteresis will keep the output low until the AE level drops to 0V. Therefore, the output of the comparator is low for the duration of an AE event. This signal is fed directly to the IC1 pin on the MC68HC11 microprocessor and is called EVENT-BEGIN*. A high to low transition on EVENT-BEGIN* triggers an input capture on the microprocessor's timer, signalling the beginning of an AE event.

A high to low transition on EVENT-END* signifies that the end of an AE event has occurred, and that the event was of sufficient peak amplitude to be recorded. EVENT-END* is fed into the IC2 pin of the microprocessor which triggers an input capture and a processor interrupt. Therefore the processor is only interrupted at the end of an AE event that needs to be recorded. EVENT-END* is derived by NANDing the comparator output with the COUNT signal, which results in a high to low transition only when the COUNT signal is asserted and the comparator output changes from low to high.

2.2.3.4 Frequency Detector

The frequency detector generates the PERIOD signal. The PERIOD signal is a pulse that has a width equal to the time between the first two consecutive threshold crossings of the AE signal after the COUNT signal has been asserted. The frequency detector circuit is shown on sheet 5 of the schematic diagram.

The output of an LM339 comparator transitions from low to high every time the AE signal rises above a threshold voltage. The threshold voltage is set by the D/A converter. The time between any two rising edges of the comparator output is the period of one cycle of the AE signal.

The output of the comparator is fed into a sequential logic circuit that derives the PERIOD signal under the following constraints:

- A pulse is generated for the first cycle following the assertion of the COUNT signal.
- Only one pulse is generated per sufficient peak amplitude AE event. amplitude. Another pulse will not be generated until the processor resets the COUNT signal.

The sequential logic consists of two D flip-flops that generate the PERIOD signal. Figure 2-4 illustrates the timing of this circuit. The first flip-flop is clocked by the threshold crossing detector output. The D input to the first flip-flop is connected to the inverted Q output, providing a divide by two function on the clock input. This divide by two circuit will change state for every rising edge on the clock.

The second flip-flop is used to control the CLR* input of the first flip-flop. When the COUNT signal goes high, the CLR* input of the first flip-flop is set high, allowing the first flip-flop to change states at the next rising edge of the clock. When the Q* output of the first flip-flop goes from low to high, the second flip-flop is clocked, and the Q* output of the second flip-flop resets the CLR* input on the first flip-flop low, thus preventing it from changing states again. The result is a single pulse generated on the PERIOD line only when the COUNT signal is asserted.

The PERIOD signal is then used to control the GATE0 pin on the 8253 timer board of figure 2-5. Operation of the 8253 timer is described in section 3.3.3.

2.2.4 Microprocessor System

All of the AE characteristic signals that are derived are sent to the microprocessor system to be processed and recorded. Figure 2-5 is a block diagram of the microprocessor system components, which include:

- Microprocessor Board
- D/A Converter Board
- 8253 Timer Board
- Real-Time Clock Board

These components are discussed below.

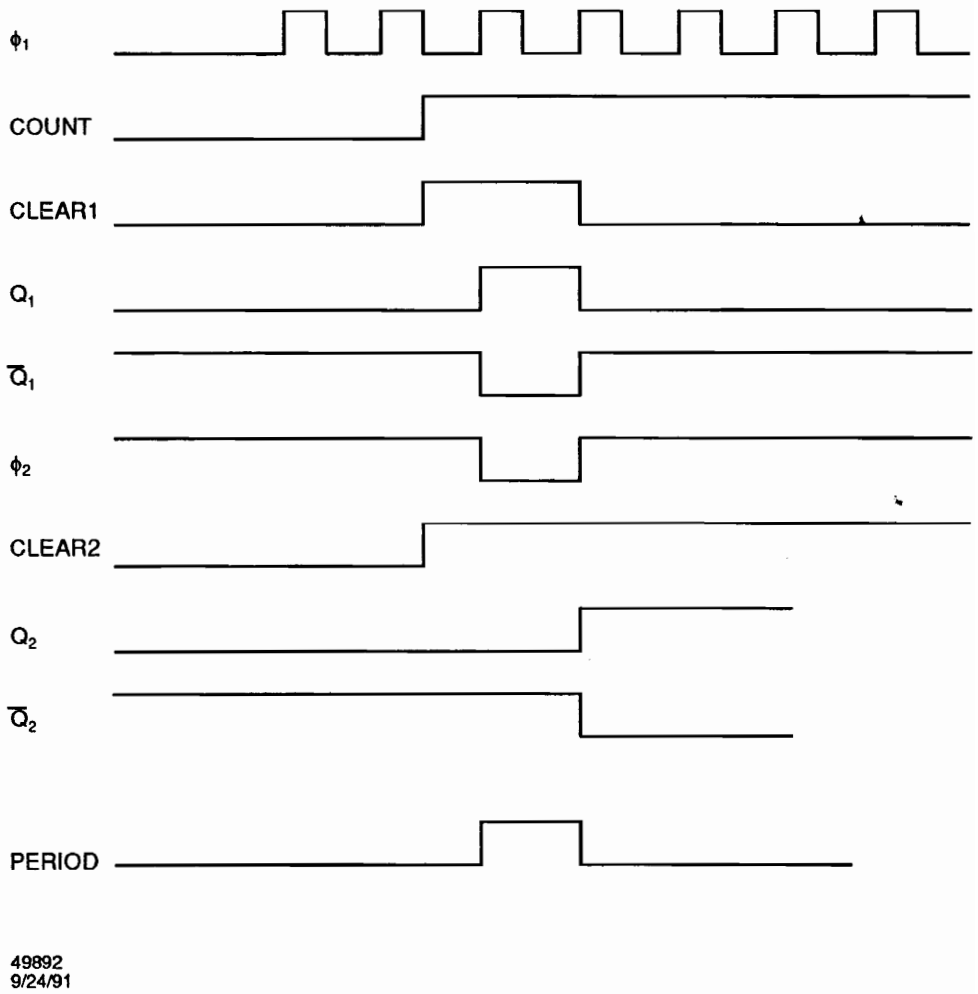

Figure 2-4. PERIOD Signal Derivation Timing Diagram

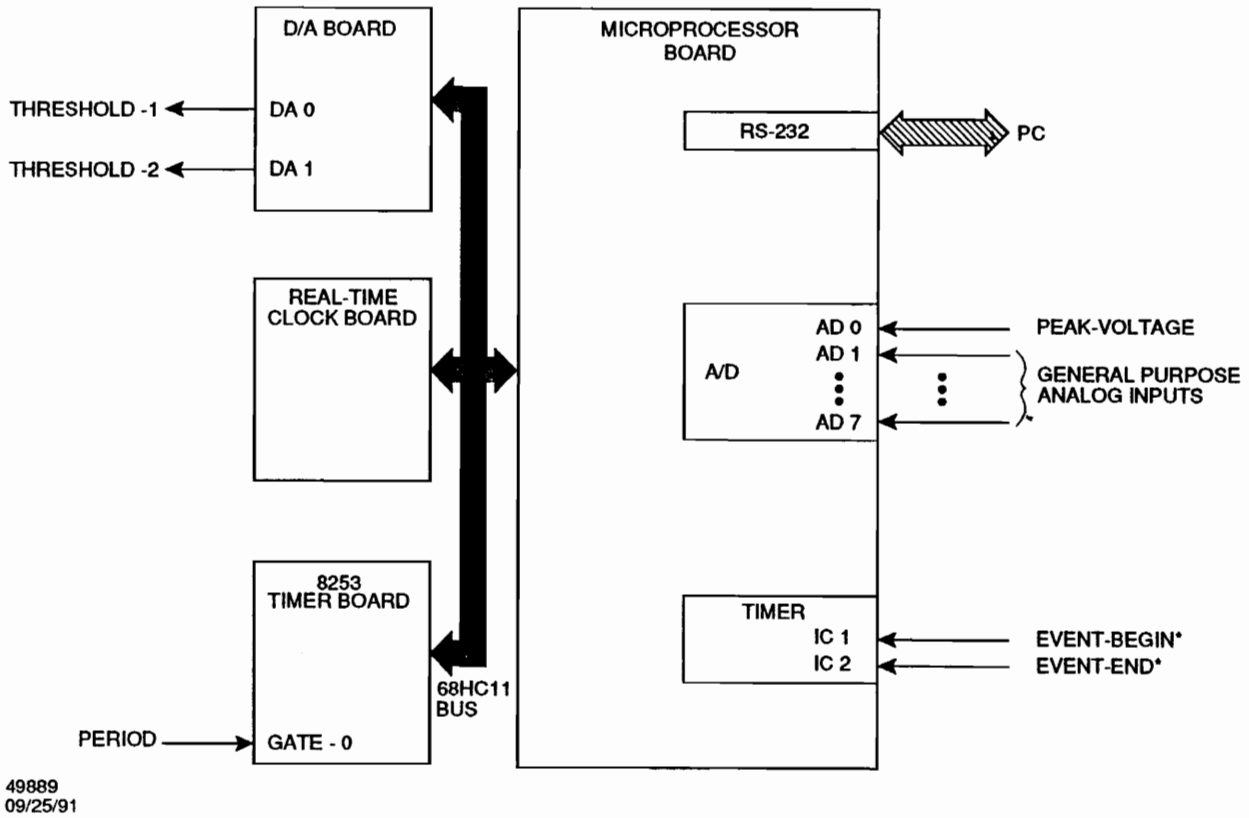

Figure 2-5. Microprocessor System Block Diagram

2.2.4.1 Microprocessor Board

The microprocessor board is a Model NMIX-0032 board from New Micros, Inc., in Dallas, Texas. The board is built around the Motorola 68HC11 single-chip computer. The NMIX-0032 board contains support circuitry for the 68HC11 to provide external RAM, EPROM, RS-232 interface, system clock, power, and an external bus. The features of the NMIX-0032 board that are pertinent to the AE system are:

- Timer - 16-bit free running timer with external triggers to capture the timer value into registers. It is used in the AE system for duration detection.
- A/D Converter - 8 channels, 8 bits per channel. It is used to record the PEAK-VOLTAGE signal and 7 external general purpose inputs.
- Digital I/O ports - general purpose 8 bit I/O ports. One output bit is used in the peak detector reset circuit.
- RS-232 Interface - All information is output through this port.
- EPROM based FORTH programming language - provides for ease of software development.
- 2 MHz System clock
- Operation from a single 5V supply
- On board memory expansion - up to 24K of RAM/ROM space for code and data.

The other system components are peripheral boards that connect to the 68HC11 via the system bus. These cards stack upon each other and the system board, thus providing interconnection to the bus.

2.2.4.2 D/A Converter Board

A New Micros NMIS - 4000 D/A converter board is used to supply the comparator threshold voltages THRESHOLD-1 and THRESHOLD-2. The board supplies 8 channels of 8-bit D/A conversion. Each channel is referenced from an external 12V supply to provide a 0-10V output range.

2.2.4.3 8253 Timer Board

A New Micros NMIS-9002 board is used to supply the system with an 8253 timer chip. One timer is used for frequency detection. The operation of the timer board is given in section 3.3.3.

2.2.4.4 Real-Time Clock Board

A New Micros NMIS-9003 board is used to supply the system with a real-time clock (RTC). The RTC is used to record the time of occurence of an AE event in an hours, minutes, and seconds format, which are reset to 00:00:00 at the beginning of an AE test. The RTC has a one second resolution.

Operation and programming of the above hardware and microprocessor system components is discussed in section 3.3. For a more detailed description of the

microprocessor system components, refer to the New Micros reference manuals [16, 17, 18, 19].

2.3 Hardware Verification

After the design and implementation was complete, it was necessary to calibrate the hardware and to verify correct operation. The results of these procedures are given here.

2.3.1 Amplifier and Filter

The amplifier and filter circuits consist of two gain stages and two passive filter networks. It was necessary to calibrate the gain of each stage to provide an overall gain of 80 dB. The input and feedback resistors were chosen carefully to provide 40 dB of gain for each stage.

Calibration of the filter networks was not necessary because the corner frequency of the low pass filter was not critical. It was only necessary to verify that the corner frequency was well below the low frequency cutoff of the sensor, which was 100kHz.

A frequency generator was connected to the input of the amplifier and filter circuit to provide the frequency source. The input and output of the amplifier and filter circuit

were monitored with a dual-trace oscilloscope so that amplitude differences could be seen. The output of the frequency generator was set to .1 mV peak-peak, and the frequency was swept from 1 kHz to 1 MHz.

Figure 2-6 is a plot of the amplifier and filter circuit gain measured for various frequencies. From this data, it is clear that the gain drops 3 dB below 80 dB at around 25 kHz and 500 kHz.

2.3.2 AC to DC Converter

The AC to DC converter was calibrated such that the output waveform amplitude was approximately the same as the peaks of the input waveform. This resulted in a DC waveform that resembled the envelope of a full-wave rectified input signal. The 43kΩ resistor in the feedback loop of the second stage of the converter was chosen to give this desired gain effect. Figure 2-7 is a digital oscilloscope output showing a sample AE signal input (figure 2-7a), and the corresponding AC to DC converter output (figure 2-7b).

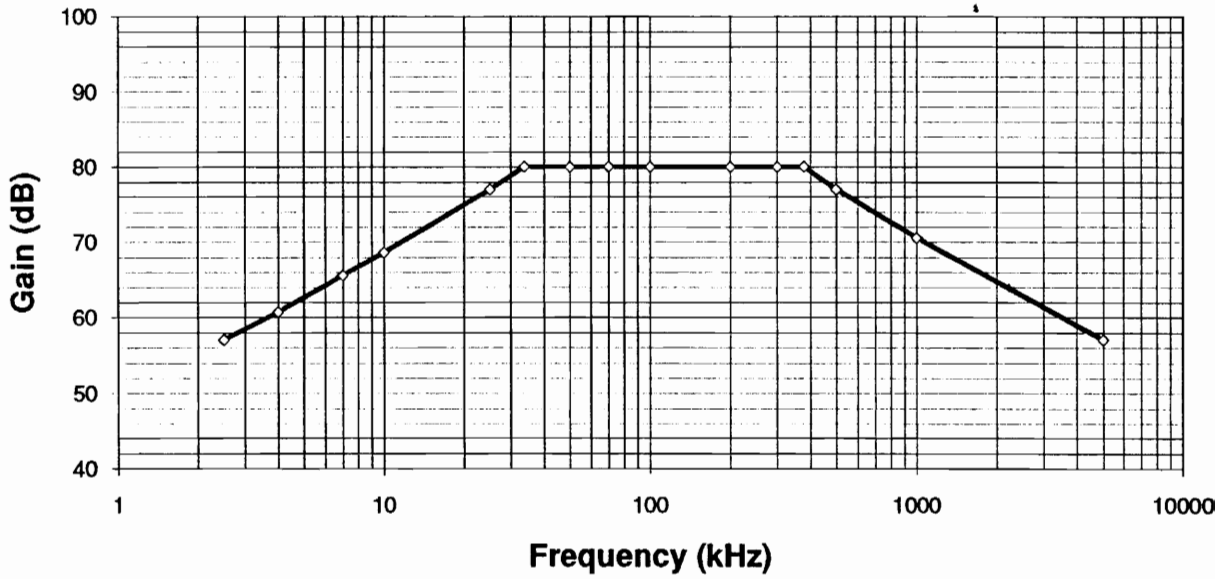

Figure 2-6. Amplifier and Filter Circuit Frequency Response

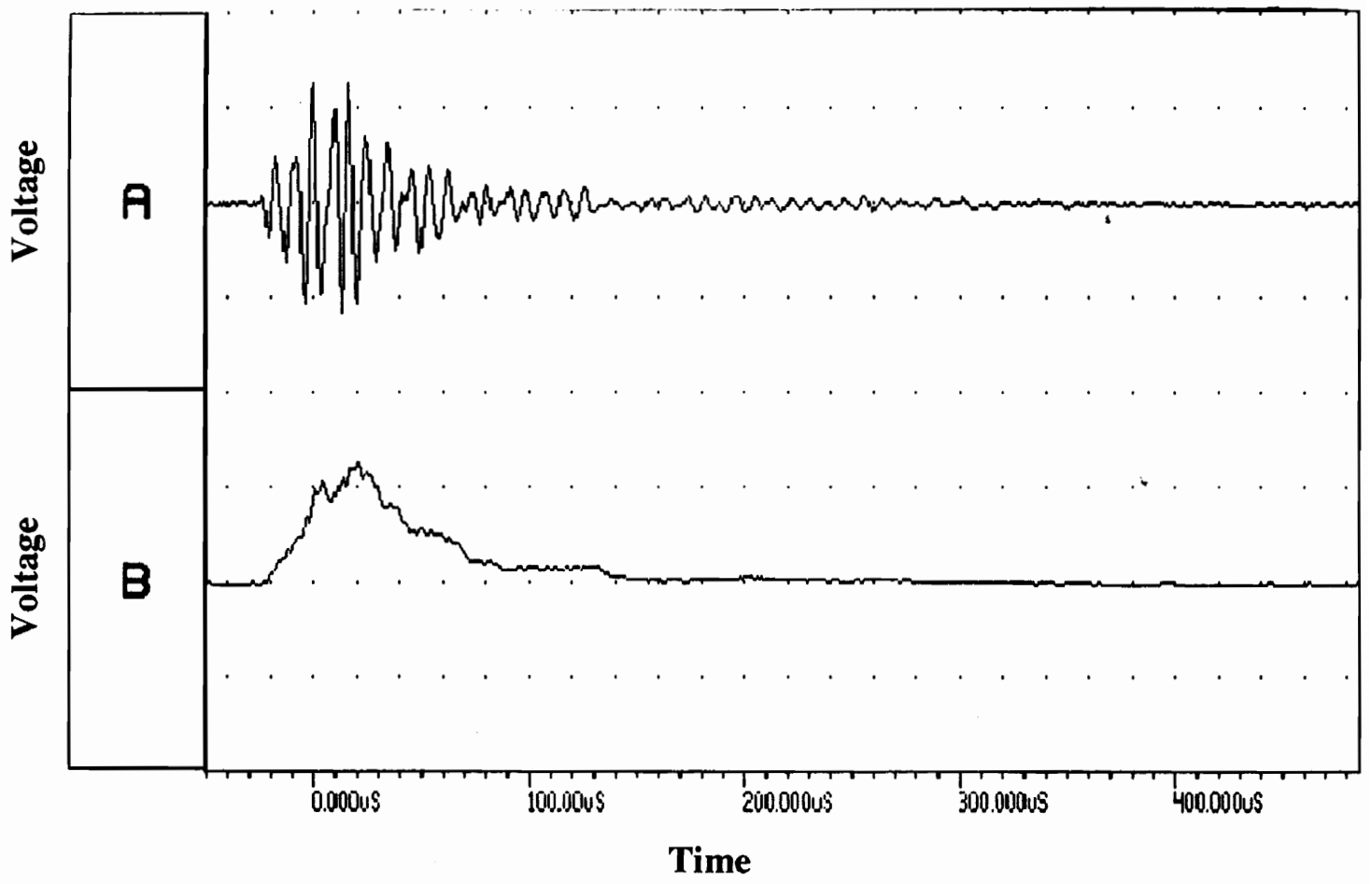

Figure 2-7. AC to DC Converter: (a) Sample AE input. (b) Converter output.

2.3.3 Peak Detector

The peak detector circuit required only the calibration of the output voltage scaler because the peak detection was handled by the PKD-01 integrated circuit. The voltage scaler circuit was calibrated such that the output voltage was exactly 1/3 of the input voltage. The 30kΩ input resistor and 10kΩ feedback resistor of the first stage of the scaler were chosen to acheive the gain of 1/3.

Figure 2-8 shows the output of the PKD-01 (before the scaler) for a sample DC AE input signal. The PKD-01 clearly holds the peak voltage of the input waveform.

The results of testing the A/D input that reads the peak voltage are given in section 2.3.6.

2.3.4 Duration Detector

The duration detector circuit required no calibration. Figure 2-9 shows the output waveform of the comparator for a sample DC AE input. It can be seen from this figure that the comparator switches low when the DC signal rises above .2 volts and does not switch back high until the DC signal drops to 0 volts, due to hysteresis.

The duration detector was tested with the microprocessor system to verify that the microprocessor was reading the correct duration. A storage oscilloscope was used to

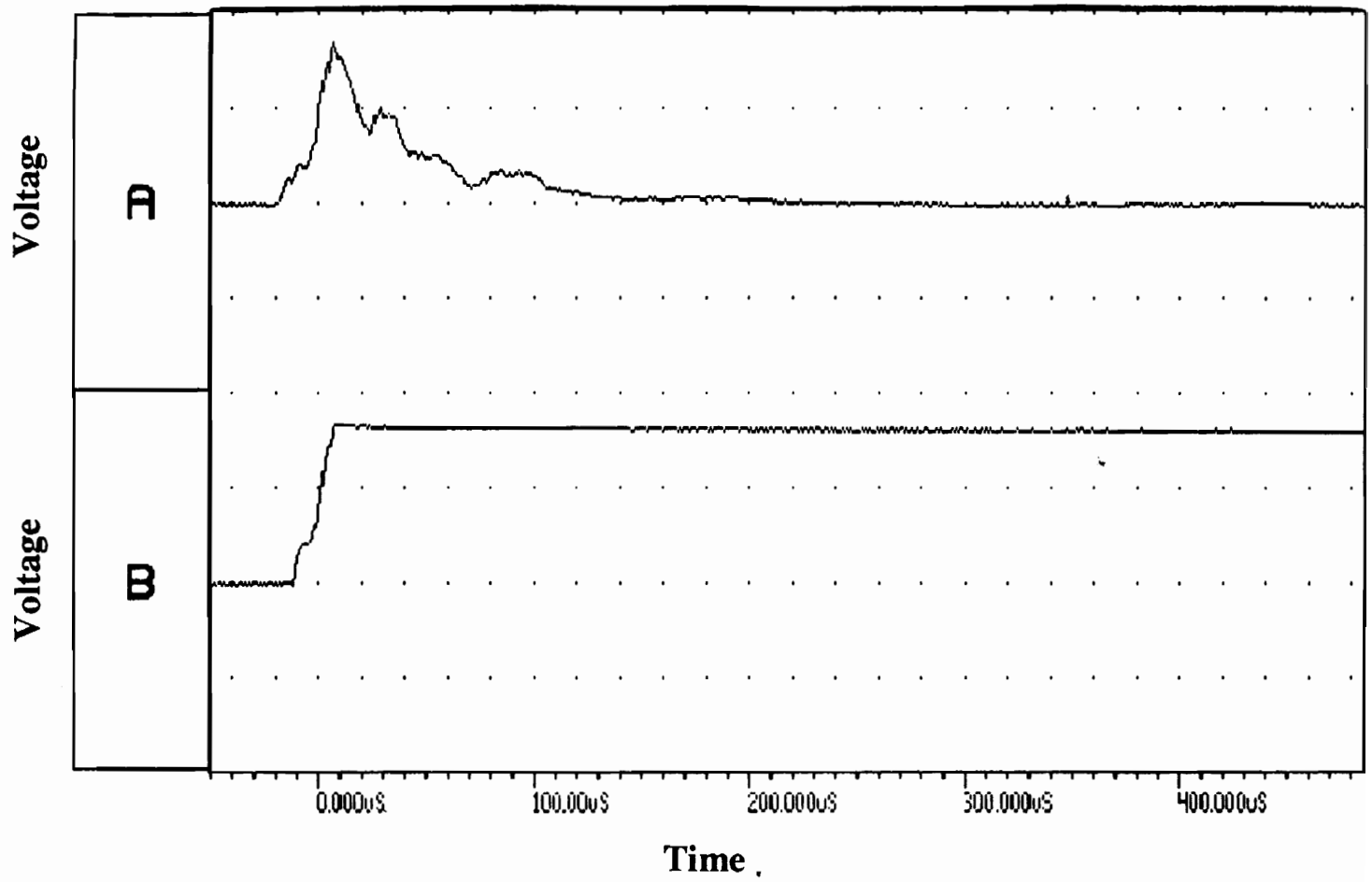

Figure 2-8. Peak Detector: (a) Sample DC AE input. (b) PKD-01 output.

capture the comparator output and the corresponding duration detected by the microprocessor system was verified as having the same value.

2.3.5 Frequency Detector

The frequency detector circuit was tested in two stages: first the PERIOD signal derivation circuit was tested, then the 8253 board was added and the complete section was verified. Figure 2-10 shows the comparator output for a sample AE signal input. It can be seen from these waveforms that a pulse is generated for every large peak of the AE signal.

Figure 2-11 also shows the pulses generated at the output of the comparator for a sample AE signal along with the PERIOD pulse generated from the same AE signal. Note that a couple of pulses appear in waveform A without a corresponding PERIOD pulse being generated. This occurred because the AE signal that caused these pulses was not of high enough amplitude to set the COUNT signal, and therefore no PERIOD signal was generated.

To test the frequency detector operation, a frequency generator was used to drive the AE-SIGNAL to the detector circuit. The corresponding frequencies measured by the microprocessor system through software were checked against the input frequency. The results were accurate and repeatable.

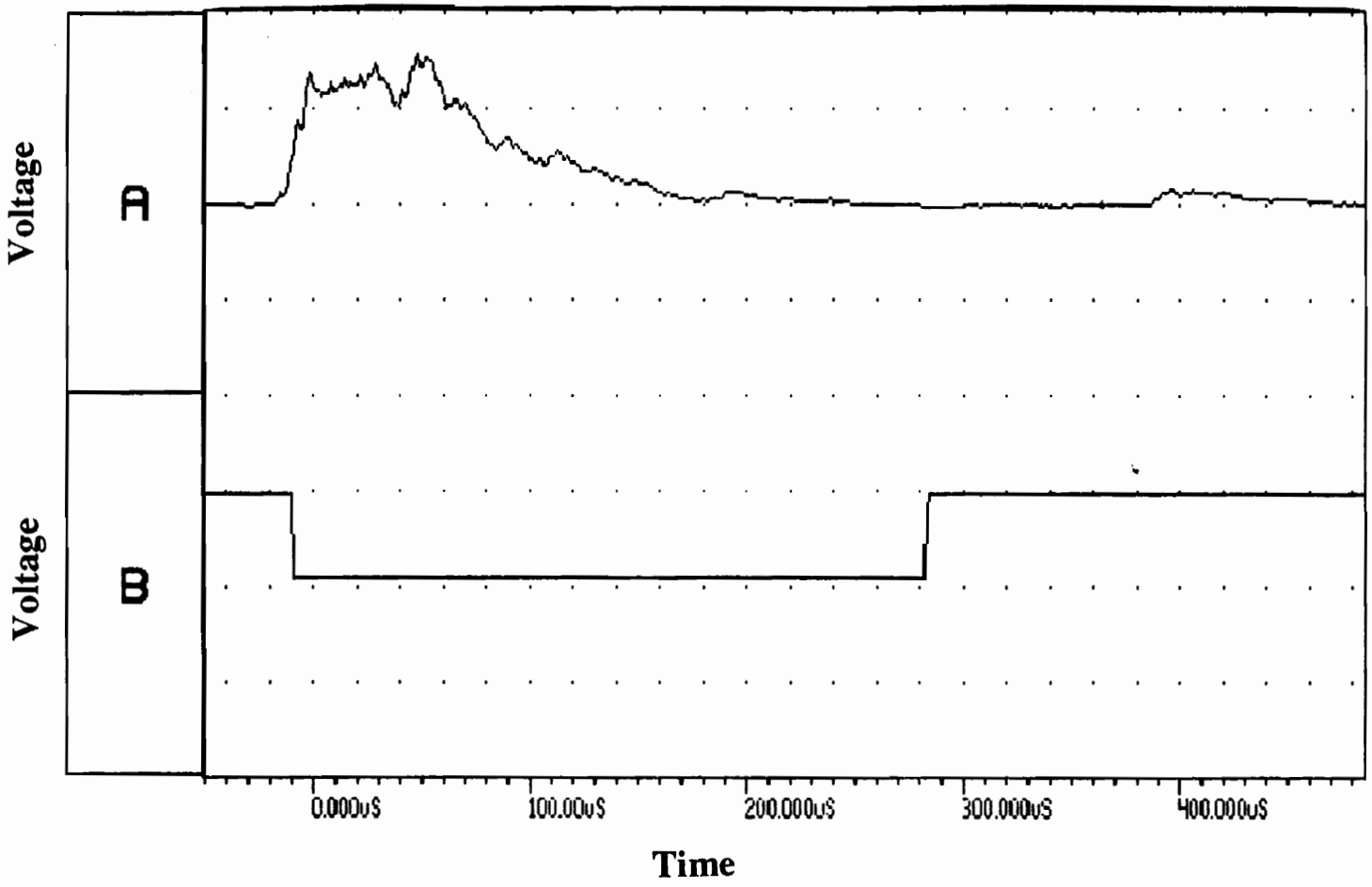

Figure 2-9. Duration Detector: (a) Sample DC AE input. (b) Comparator output.

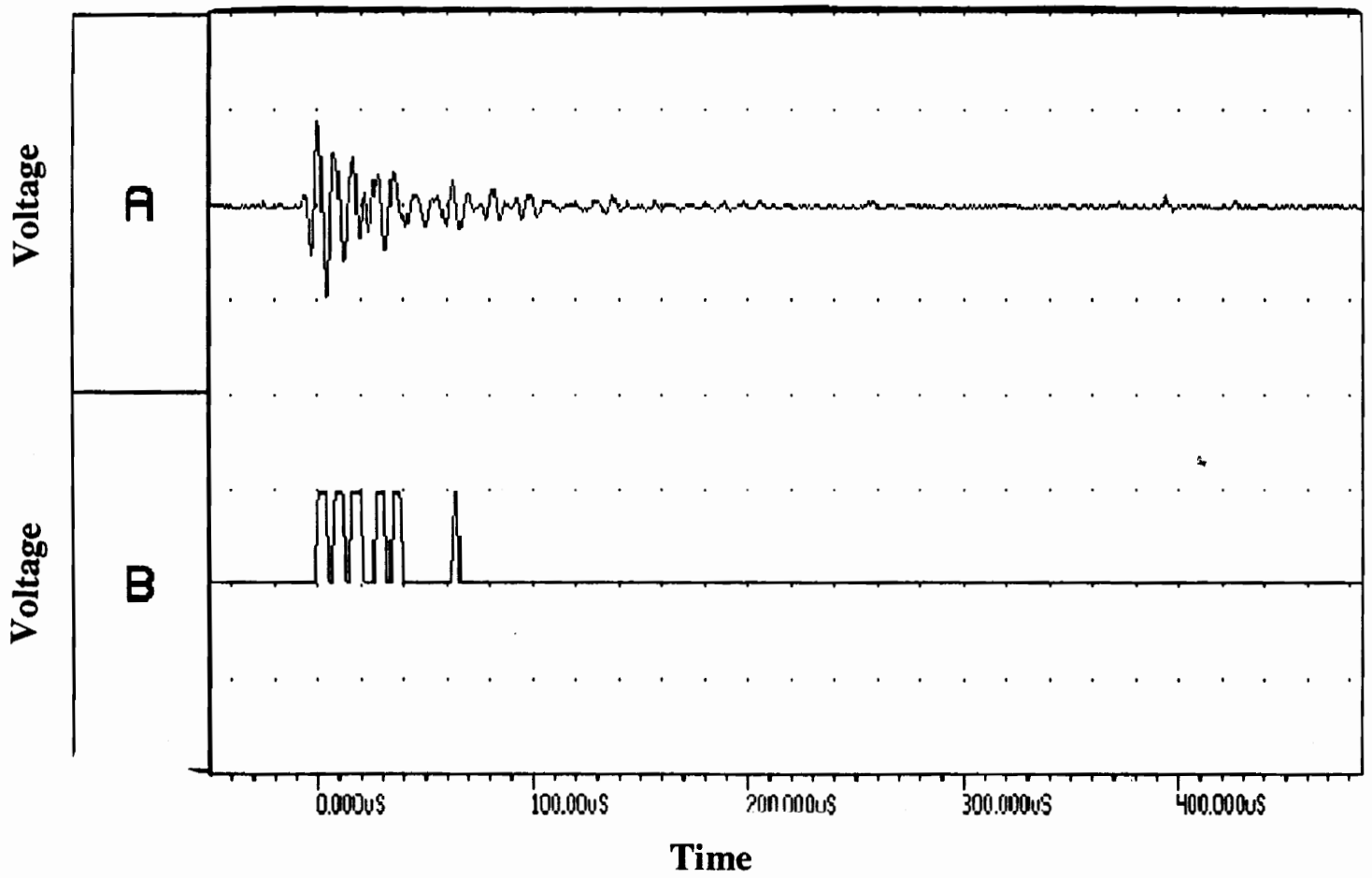

Figure 2-10. Frequency Detector: (a) Sample DC AE input. (b) Comparator output.

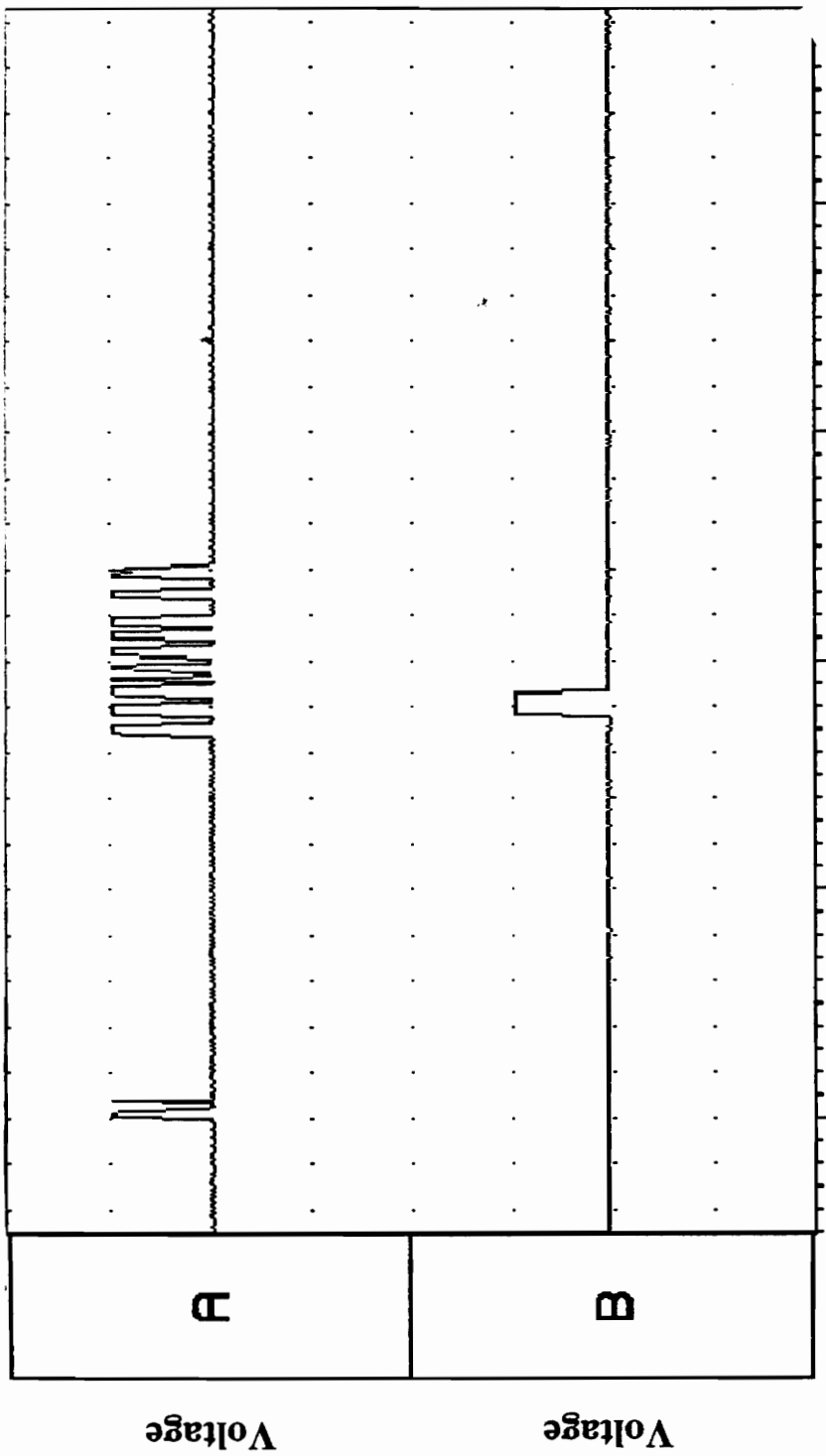

Figure 2-11. Frequency Detector: (a) Comparator output. (b) PERIOD signal.

2.3.6 A/D Inputs

The A/D inputs were verified by reading the A/D registers via software for various known voltages input on the A/D lines. All of the A/D readings were verifiable.

2.3.7 D/A outputs

The D/A lines were verified by measuring the voltage output for various settings of the D/A registers with software. All D/A voltages matched the values output to them.

Chapter III

SOFTWARE

The microprocessor system is responsible for the monitoring and control of the system hardware and all communications with the host computer. It is necessary to develop specialized software routines for the microprocessor to enable it to perform these functions. This chapter provides an overview of the operating system used by the microprocessor and a detailed discussion of the software written for the AE system.

3.1 Overview

The 68HC11 microprocessor provided with the NMIX-0032 board has a FORTH operating system embedded in internal ROM. When the 68HC11 is reset, FORTH takes control of the system allowing the user to communicate with the board via the

RS-232 port within the operating system. The user then defines program modules or "words" from previously defined words or words that are intrinsic to FORTH. FORTH compiles the words as they are defined, and no machine language or microprocessor register interaction is needed. Words can then be executed in four different ways: typed at the command line, upon reset, interrupt, or called by another word.

Figure 3-1 is a flow diagram that shows how the FORTH operating system is used with the software defined for the AE system. When the microprocessor is reset, the reset initialization routine MAIN is executed automatically. Upon completion of the initialization routine, control is returned to FORTH, which provides the user with a command line prompt via the RS-232 port.

The user may then execute several routines to configure the hardware or to start/stop an AE test. These routines are executed by the user by typing the routine name, along with any data that needs to be passed, and hitting return. After the routine is completed, control is again returned to FORTH. The interrupt service routine is executed if the interrupt has been enabled and an interrupt occurs, and it too returns control to FORTH.

Appendix A contains a listing of the software routines written for the AE system. The routines can be partitioned into the following categories:

1. Declaration Statements
2. Hardware Operation Routines
3. Reset Initialization Routine

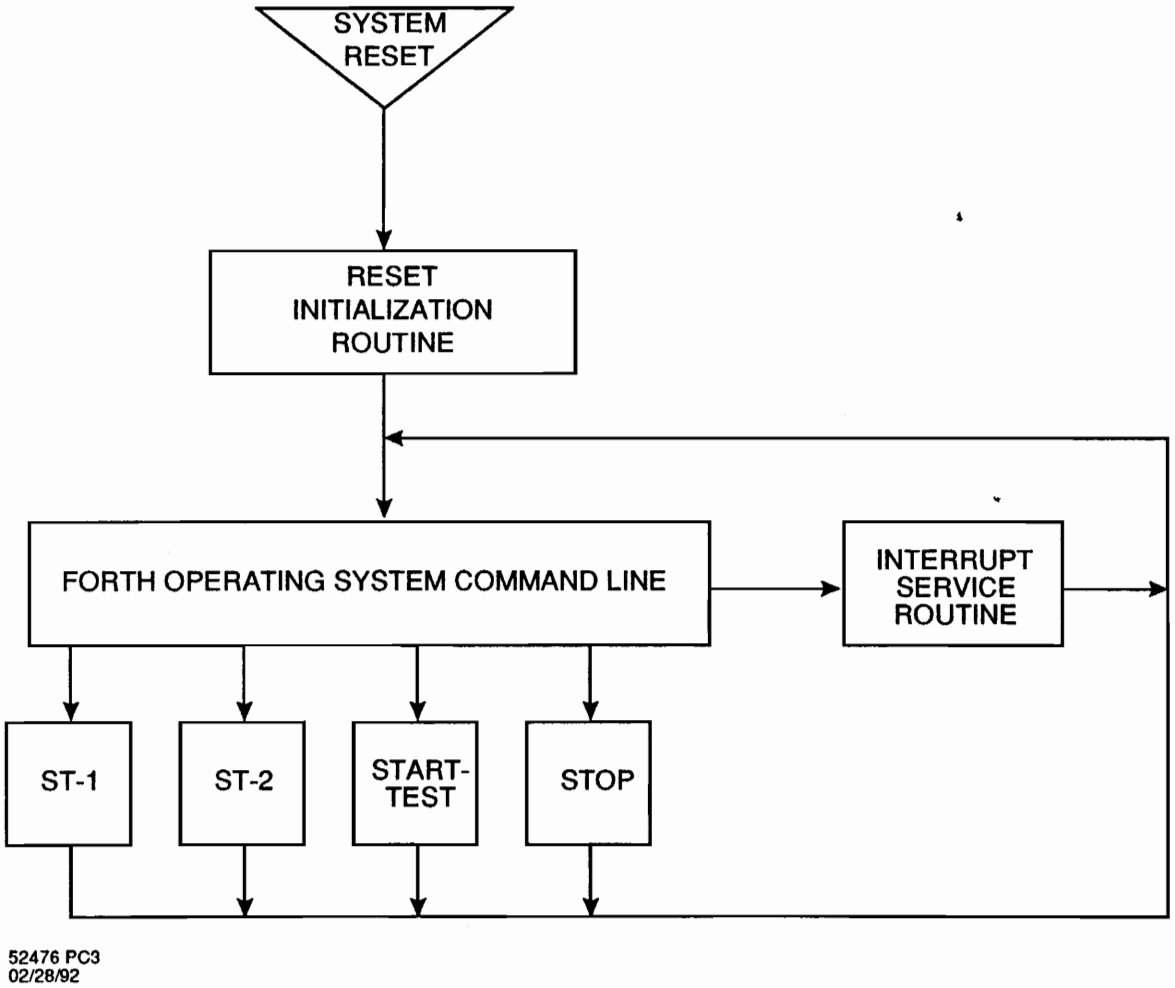

Figure 3-1. Software Flow Diagram

4. Command Line Routines

5. Interrupt Service Routines

These program segments are described in detail below.

3.2 Declaration Statements

3.2.1 Constants

System hardware registers are assigned logical names with the CONSTANT statement. The purpose of assigning logical names to the registers is to make the program listing easier to read by referring to registers by a name instead of a numerical address.

3.2.2 Variables

Variable names are assigned memory space with the VAR command. These variables are used by various program segments to store and pass information.

3.3 Hardware Operation Routines

Several program routines are defined to read and write to the system hardware. These might be termed hardware driver routines in larger systems. The hardware operation routines are self-contained and pass data to the routine that called them by pre-defined variables or via the system stack.

Hardware operation routines can be categorized to perform one or more of the following system functions:

1. Peak Detection and A/D Input
2. Duration Detection
3. Frequency Detection
4. Time of Occurrence

The following is a discussion on how each of these functions is performed, and the related software routines.

3.3.1 Peak Detection and A/D Input

Peak detection and analog voltage input require the use of the microprocessor's A/D converter. A/D channel 0 is used to read the peak detector voltage, and channels 1-7 are used to read 7 general purpose inputs.

The A/D converter is accessed via the control register ADCTL and four storage

registers AD0 through AD3. A/D conversion is performed on one bank of four channels at a time: channels 0-3 or channels 4-7. ADCTL is setup to read one of the two banks, and the results of the conversion are placed in the four storage registers. A flag is set in ADCTL when the conversion is complete.

Routine READ-AD1 shown in the software listings in Appendix A sets up the ADCTL register for conversion of the first bank and waits for the end of conversion flag to be set. READ-AD2 performs the same function for the second bank of A/D channels. The calling routine then reads the storage registers to get the results of the conversion.

After the peak voltage is read, the peak detector is reset by the RESET-PEAK routine. RESET-PEAK toggles the PA3 output pin high then low.

3.3.2 Duration Detection

Duration detection is performed by the 68HC11 on-chip timer. The timer consists of a free running 16-bit counter and several 16-bit timer registers. Timer register TCTL2 is set up to make the timer perform the following functions:

1. Capture the timer count in register TIC1 when a high to low transition occurs in input pin IC1.
2. Capture the timer count in register TIC2 when a high to low transition occurs on input pin IC2.

The EVENT-BEGIN* signal is connected to input pin IC1, so the timer is captured in

register TIC1 at the beginning of an AE event. EVENT-END* is connected to input pin IC2, so the timer count is captured in register TIC2 at the end of an AE event. The duration of the AE event is then calculated by subtracting TIC1 from TIC2 and converting the count difference into microseconds, knowing that the timer runs at 2 MHz. The timer has a resolution of .5 microseconds.

The timer is also responsible for interrupting the processor when the EVENT-END* signal is asserted, signifying the end of an AE event that was of sufficient peak amplitude to be recorded. The 68HC11 provides for interrupts on timer input captures, and the TMSK1 register controls these interrupts. TMSK1 is set up to enable an interrupt on input capture 2, which is triggered by the EVENT-END* signal. Register TFLG1 is a flag register that signifies input capture events. TFLG1 must be reset to re-enable an interrupt after an input capture has occurred [16].

3.3.3 Frequency Detection

Frequency detection is performed on the 8253 timer board. The 8253 timer-0 is placed in mode 0 and loaded with FFFFh (hex). The PERIOD signal is connected to the gate pin of timer-0, and the timer counts down whenever the gate pin is high. An 8 Mhz clock is connected to the clock pin of timer-0, causing it to count down at the rate of 125 ns/count. The frequency is calculated by reading the timer after an AE event has occurred, and subtracting that value from FFFFh. The period is then converted to a frequency in Mhz.

The routine RESET-COUNTER0 sets timer-0 to mode 0 and loads it with FFFFh. READ-COUNTER0 reads the timer-0 value, converts it to a frequency in Mhz, and places the result on the system stack.

3.3.4 AE Event Time of Occurence

The time of occurrence function is performed by reading the real-time clock. The real-time clock is set to 0 at the beginning of a test. Several declaration statements and program routines are used to control the real-time clock board, and these routines were taken from the New Micros NMIS-9003 reference manual [19]. The RESET-CLOCK routine resets the RTC to 0. The clock starts immediately after this routine is called. The CLK routine displays the number of hours, minutes, and seconds that have passed since the clock was reset.

3.4 Reset Initialization Routine

The routine MAIN is executed automatically upon system reset. The purpose of MAIN is to restore the system user area [16], output a system message to the RS-232 port, and to set the default D/A threshold output values. The system user area is a reserved section of RAM that is used by the FORTH operating system. It is necessary to restore this section of RAM so that FORTH knows that words have been defined and reside in ROM. The routine then returns control to the FORTH operating system which waits for a command line routine to be executed by the user.

3.5 Command Line Routines

The main program segment includes 4 routines that may be used to configure the system hardware or to start and stop an AE test. These routines are:

1. ST1
2. ST2
3. START-TEST
4. STOP

These routines are executed by the user at the FORTH command line. These routines do not interact with each other, but instead they perform a function and return control to the FORTH operating system. These routines are described below in detail.

3.5.1 ST1 and ST2

The user may execute the ST1 and/or ST2 routines to change the D/A voltage outputs THRESHOLD-1 and THRESHOLD-2. ST1 and ST2 remove a value from the system stack, convert the value to a binary representation of the voltage, and write the byte to the corresponding D/A channel register. The voltage value removed from the stack is in tenths of a volt, and no decimal points are allowed (Fixed point notation is used). No confirmations or handshakes are used in this routine.

3.5.2 START-TEST

The START-TEST routine may be executed by the user to begin an AE test. START-TEST performs the following functions:

1. Initialize the IC2 interrupt vector [16].
2. Set up the 68HC11 timer input captures.
3. Reset the following:
    - 68HC11 timer flag register (TFLG1)
    - Peak detector
    - 8253 timer
    - RTC board
4. Enable the IC2 interrupt.

These functions are described in section 3.3. The START-TEST routine returns control to the FORTH operating system with the IC2 interrupt enabled. The system will stay in test mode until the STOP command is executed.

3.5.3 STOP

The STOP routine performs only one function, which is to disable the IC2 interrupt. The user executes STOP to end an AE test. The hardware remains active even when the interrupt is disabled.

3.6 Interrupt Service Routine

The interrupt service routine is called IC2INT. This interrupt is caused by the end of an AE event that is of sufficient peak amplitude to be recorded. The IC2INT routine performs the following functions:

1. Temporarily disable the IC2 interrupt.
2. Calculate the following AE characteristic information and output it to the RS-232 port:
    - Peak voltage
    - Duration
    - Frequency
    - Time of Occurrence
3. Read the 7 general purpose analog voltage inputs and output the values to the RS-232 port.
4. Reset the following:
    - 68HC11 timer flag TFLG1
    - 8253 timer 0
    - Peak detector
5. Re-enable the IC2 interrupt.

IC2INT calls the DISPINFO routine to output the recorded information to the RS-232 port.

3.7 Summary

The software routines developed for the AE system are programmed into a ROM that is located on the microprocessor board, which allows the system to run without downloading code to the microprocessor. All of the FORTH routines developed reside in approximately 3k of ROM.

The interrupt service routine begins execution after an AE event has completed. Any AE events that occur while the interrupt routine is executing will go undetected. The execution time of the interrupt service routine is approximately 100 milliseconds and was measured with an oscilloscope by examining the time between the rising edge of the IC2 pin and the falling edge of the peak detector reset pin. The rising edge of the IC2 pin triggers the interrupt, and the interrupt routine resets the peak detector right before it re-enables the interrupt mask, so this measurement is a good indication of execution time.

Chapter IV

USERS MANUAL

This document explains the method for using the AE detection and characterization system (AEDCS). The AEDCS is a microprocessor controlled device that detects and records the following AE characteristics:

1. Peak Voltage
2. Duration
3. Frequency
4. Time of Occurence

The AEDCS also records seven analog voltages which can be used for additional instrumentation purposes. D/A outputs are provided for configuring the system hardware via commands sent from the host computer over the RS-232 serial port. AE events are picked up with a piezo-crystal transducer, and all recorded information is output through an RS-232 serial port.

4.1 System Specifications

RS-232 Serial Port
Baud: 9600
Data: 7 bits
Parity: None
Stop-bits: 1

Sensor
Type: Piezo-crystal transducer
Model: AC175L from AET, Inc.
Bandwidth: 100 kHz to 300 kHz @ 3 dB points
Sensitivity: -68 dB, referred to 1V/µbar

Amplifier and Filter
Gain: 80 dB, fixed
Bandwidth: 25 kHz to 500 kHz @ 3 dB points

Peak Detector
Range: 0 to 15V
Resolution: 60 mV
Threshold: 0 to 10V, settable in .1V steps

Duration Detector
Range: .5 µs to 20 ms
Resolution: .5 µs

Frequency Detector
Range: 8 MHz
Resolution: .125 µs of period

A/D Inputs
Range: 0 - 5V
Resolution: 8 bits (.0196 mV)

O-Scope Output
Ouptut Imped.: Low
Range: ±15V max.

4.2 Setup

The AEDCS consists of the following components:

1. AEDCS Box
2. Piezo-Crystal Transducer & Cable
3. Constant Force Spring
4. RS-232 Cable

Figure 4-1 is a diagram of the system components and their interconnection.

The AEDCS box has the following connectors, cables, and switches:

- Sensor Connector - A BNC type connector input for the piezo-crystal transducer cable.
- O-Scope Connector - A BNC type connector for monitoring the amplifier stage AE output.
- RS-232 Connector - A DB-25F type connector for the RS-232 cable.
- On/Off Switch - Main power.
- RESET Button - resets the microprocessor system.
- A/D Input Wires - Seven A/D inputs for additional instrumentation.
- 120VAC - Power Cord.

To set the AEDCS up for use, simply connect the system as shown in figure 4-1.

The transducer should be mounted with a thin coating of silicon vacuum grease between the face of the transducer and the specimen. The constant force spring holds the transducer in place and helps maintain a good acoustic interface between the specimen and the transducer. Mount the spring over the transducer as shown in the inset of figure 4-1.

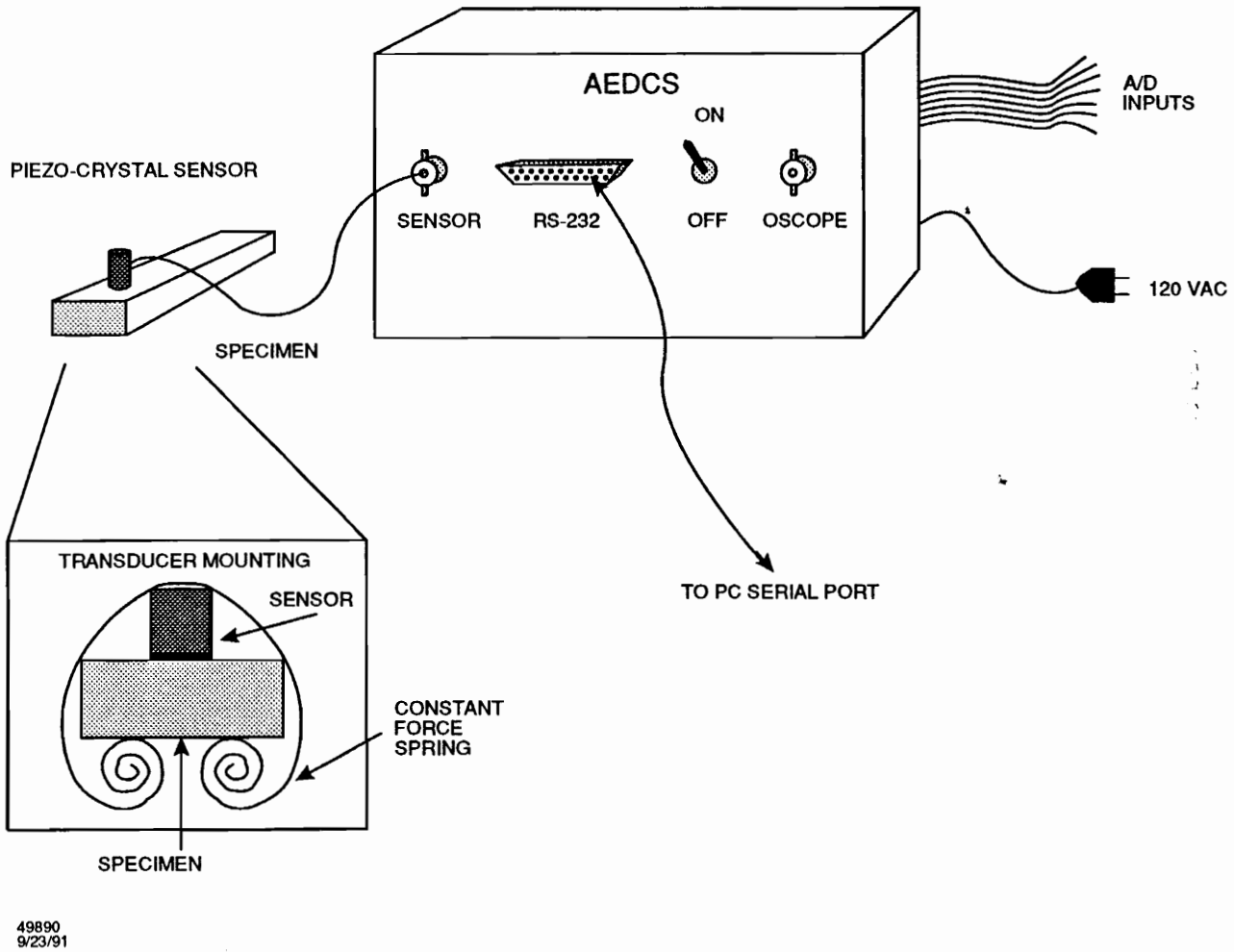

Figure 4-1. Setting Up the AEDCS

The RS-232 cable should be connected to the serial port of a computer - preferably a personal computer (PC). Any communications software that allows interaction with the PC's serial port should be run on the PC. This allows the user to send setup commands to the AEDCS and to view the AE data recorded during a test. A communications program that captures data on the serial port to disk is needed if the results of an experiment are to be stored. Because of the variety of needs that different researchers may have, development of the communication software for the PC is left to the user. An example of a particular data logging software is described in chapter 5.

The O-Scope output and A/D inputs are optional. The O-Scope output enables the user to view the amplified AE signal. The A/D inputs are general purpose, and can be used to record up to 7 analog voltages at the occurence of an AE event. Typical usage for these inputs might be temperature and humidity sensors, load cells, or position monitoring sensors.

Once the AEDCS is set up and the PC is ready for serial communications, the power to the AEDCS should be switched on. A message should appear on the PC that indicates that the AEDCS is ready to begin a test. If the message doesn't appear, press the reset button on the AEDCS box. The AEDCS is now ready for an AE test.

4.3 Operation

Operation of the AEDCS is very simple: there are only four commands that can be executed. These commands setup the comparator threshold voltages and start and stop an AE test.

The first command is ST1, and is used to set the threshold voltage for the COUNT detection comparator, THRESHOLD-1. THRESHOLD-1 determines the peak voltage that is necessary for an AE event to be recorded by the AEDCS. If the peak voltage of an AE event is less than THRESHOLD-1 the AEDCS will ignore it. If the peak voltage is greater than THRESHOLD-1 the AEDCS will record it. The default setting for THRESHOLD-1 is 2.0 volts upon reset. To change this setting, send a number to the 68HC11 serial port followed by a space and the command ST1, and then send a return character. The number should be the voltage setting in tenths of a volt, and a decimal point is not allowed. For example, to set the THRESHOLD-1 voltage to 4.3 volts, send the following:

43 ST1

The AEDCS will reply with an OK message. The setting is changed immediately. Any value from 0.1V to 10.0V can be set, and the setting depends on the application.

ST2 is the second command that is used to setup the AEDCS. ST2 sets the THRESHOLD-2 voltage, which sets the threshold crossing detector for the frequency detector circuit. This threshold should be set high enough to allow the detector to

ignore any noise on the AE signal line, and low enough to enable the detector to catch most of the peaks in an AE event. This setting should be kept below the THRESHOLD-1 setting. The default setting upon reset is 0.5V, and can be changed in the same way as the ST1 command.

The command START-TEST begins an AE test. The time of occurrence for an AE event is referenced to the execution of this command. Once this command is executed, the AEDCS will immediately begin recording AE events that are of sufficient peak amplitude.

The last command is STOP. The user types STOP to end an AE test. STOP disables the AEDCS from recording any AE events, and should be executed only after the test is completed. The user can then send configuration commands or start another test. If a test is started without re-configuring the D/A channels, the configuration of the previous test will remain.

Chapter V

RESULTS

Verification of the AEDCS's functions was discussed in chapter 2. These tests proved that each section of the system's hardware performed the functions outlined in the requirements. These tests did not, however, prove that the AEDCS could be used successfully in an AE testing application.

The AEDCS is well-suited for use in many AE testing applications. As a demonstration of the system's capabilities, the AEDCS was used to record AE event characteristics in a mechanical loading test application for several different types of wood. Ansell [7] conducted similar tests to compare the effects of tensile loading of several different types of wood. By recording the count rate of AE events, he was able to distinguish between different species of wood. He was also able to correlate AE activity with internal stresses and fractures within the wood samples.

The purpose of these tests was two-fold: to prove that the AEDCS could record actual AE events and to show that the data recorded could be used to characterize known properties of different types of wood. An explanation of the test setup and procedures is given here, as well as a discussion of the test results.

5.1 Test Setup and Procedures

As mentioned in section 1.1, an AE can be generated at points of fracture or friction in wood during mechanical strains. The object of this test was to record AE event characteristics for several types of wood during a 3-point mechanical load test. A diagram of the test setup is shown in figure 5-1.

The test fixture was constucted on the test bed of an MTS, Inc. hydraulic loading machine. The specimen, 2" wide by 24" long by 1/4" thick pieces of wood, were supported at two points that were placed 18" apart. The force of the hydraulic piston was centered between the supports. The AEDCS sensor was placed 2" away from the center of the loading point.

The force and displacement outputs of the MTS were connected to the analog inputs of a Data Translation, Inc. DT2805 data acquisition board that was in a PC system. The PC was running software that recorded these analog signals every 5 seconds, providing a continuous record of these test parameters. The AEDCS analog inputs

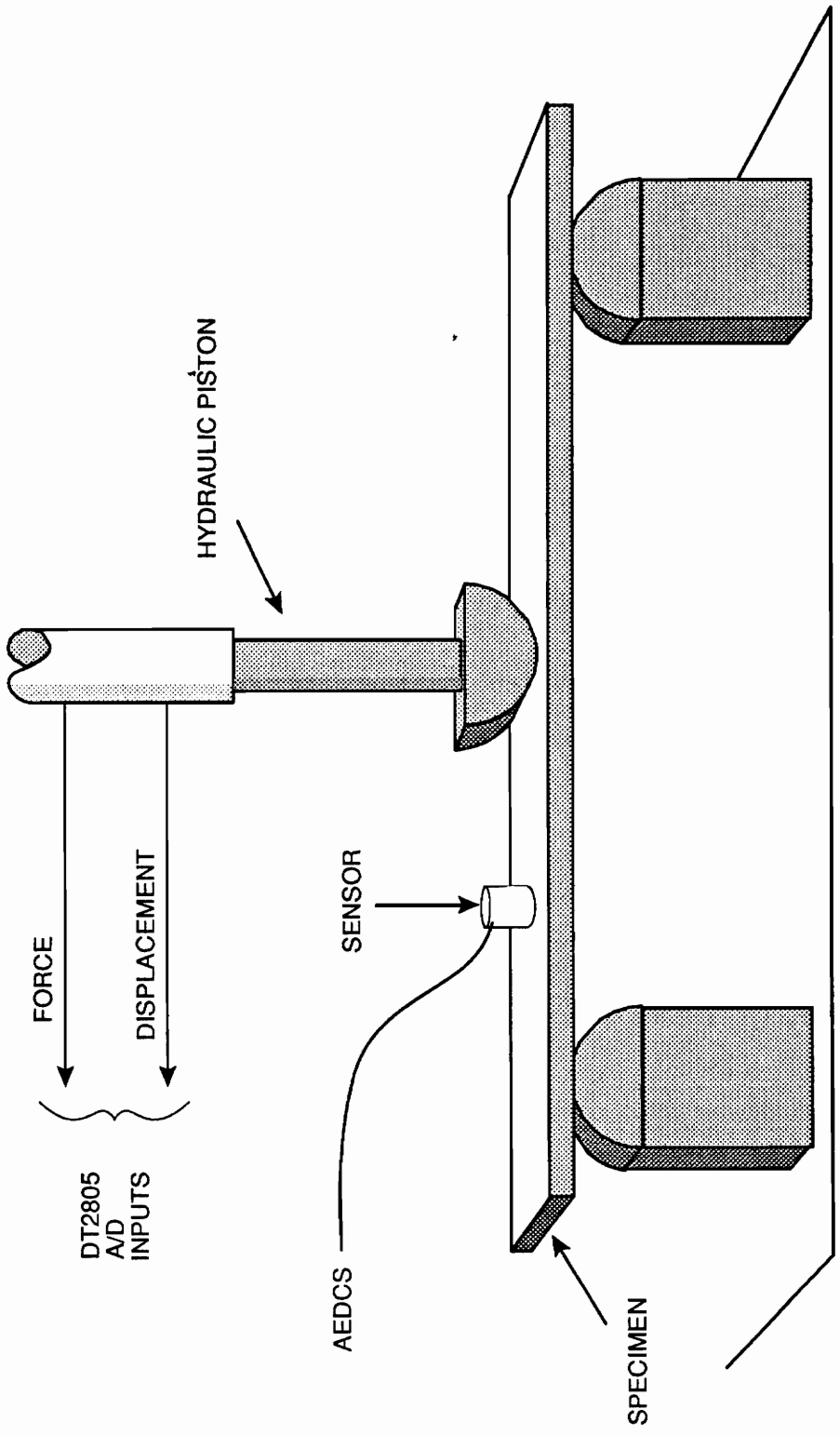

Figure 5-1. Diagram of the AE Test Setup

were not used because the AEDCS only records the analog voltage inputs when an AE event occurs, which is sporadic. The AEDCS does not provide any analog channels that are recorded at regular intervals because the real time clock interrupt needed to accomplish this might cause the system to miss an AE event. The timing of the recording of these inputs was synchronized to the beginning of the AE test.

The AEDCS was connected to the serial port of a second PC system. An Oscilloscope was connected to the O-Scope output of the AEDCS to monitor the AE signal.

The MTS was set to provide a constant rate of displacement of .0025"/sec. The AEDCS was setup with THRESHOLD-1 = 2.0 volts and THRESHOLD-2 = .5 volts. These thresholds were kept constant for all tests so that a comparison could be made between the sets of test data without adding a test variable.

The test procedure was done using the following steps:

1. A specimen was put in the test fixture and the hydraulic piston was lowered until it touched the specimen.
2. The data acquisition program on the first PC was started at the same time the START-TEST command was executed on the AEDCS with the second PC.
3. The constant displacement rate was then initiated on the MTS.
4. The test was stopped after the specimen failed (broke).

These same steps were repeated for all of the tests performed.

5.2 Test Results

Three pieces each of the following types of wood were tested: masonite, OSB, and plywood. These types of wood were chosen because of their different physical characteristics. Three pieces of each type were tested to verify the repeatability of the results.

Each of the following sections discusses the results of one of the types of wood tested. The results of only one test per wood type are given as a representation of that type due to the fact that the results were very similar.

The chart in figure 5-2 shows the actual data of displacement versus time for one of the tests. The displacement data is identical for all tests due to the constant displacement rate.

The results of each wood type are given as two separate charts: one plotting load and AE event energy versus time, and the other plotting AE event frequency versus time. The load data was taken from the ouput of the MTS load cell and represents the force placed on the specimen. The AE event energy is the product of the peak voltage and the duration of an AE event. This computation of the AE event energy is not an exact measurement of energy but is used here as an indication of energy relative to other AE events. The frequency data was taken directly from the AEDCS data.

Some obvious conclusions can be made from the load and AE energy graphs, but the AE frequency data produced no such conclusions. The lack of other research relating the frequency content of AE events to mechanical stresses adds to the inability to draw conclusions from the frequency data.

5.2.1 OSB

OSB is a wood product that is composed of small chips of wood held together by a resin compound and hot pressed. Due to the nature of this composition, OSB fractures at a much lower load than the other types of wood. Figure 5-3 shows the results of the OSB test.

It can be seen from figure 5-3 that the load line is not linear, and is in fact quite irregular. This load line shows that the specimen was constantly fracturing. The number of occurrences of AE events increased with the load, which is intuitive. The rate sharply increased while the board was failing due to the increased number of fractures that occurred.

The energy level of the AE events generally stayed low with twenty or so higher energy events occurring near the times of rapid fluctuations of load. Since a fluctuation of load usually indicates a fracture, the higher energy AE events measured should be expected.

5.2.2 Masonite

Masonite is another wood product composition. Masonite is made by hot pressing a fine sawdust and resin mixture. Since the wood fibers of masonite are already broken down as sawdust, it is expected that fewer AE events would occur due to fractures of these fibers. Figure 5-4 shows the test results for masonite.

As expected, figure 5-4 shows no AE events of sufficient energy until the board failed. It should be noted here that due to the composition of masonite it is not a good acoustic medium. AE events would therefore have to be louder to reach the sensor. AE events of smaller amplitude most likely did occur while the board was being loaded, but it was neccessary to keep the threshold the same in all of the tests for consistancy, and therefore the low energy events were not detected.

It is not unexpected to find the highest energy AE events while the board is failing, because the highest number and most severe fractures occur at this time. The highest rate of events occurred closest to the failure point, and the rate decreased as the board continued to fail and the number of fractures diminished.

5.2.3 Plywood

Two sets of plywood specimens were tested: one set was cut across the grain, and the other set was cut with the grain. Both sets of specimen showed similar test results. Figures 5-5 and 5-6 show the results of both plywood tests.

As expected, the plywood that was cut with the grain was more than three times as stiff as the other piece, and withstood a much greater force before failing. The rate of occurrence and the AE event energy dramatically increased in the piece that was cut with the grain after the board began to give and the stiffness dropped. This board, unlike any of the other specimens, endured a reduction in stiffness for a long while before failing. During this time, the highest number of severe failures occurred which led to the increased number of high energy AE events.

The cross-grain piece showed a steady increase in the rate of AE activity and event energy as the board was loaded, up until the first failure occurred. The highest energy events, however, occurred when the board underwent numerous fractures after the initial failure. These fractures can also be seen by the jagged edges on the load curve.

5.3 Summary

Several types of wood were mechanically loaded while being monitored with the AEDCS. These tests were conducted to show that the AEDCS is capable of recording several characteristics of AE events that provide usefull information in the study of AE behavior in wood materials.

The results of each test seemed to correlate well with the current beliefs on AE behavior. Increased rates of AE events and increased levels of event energy occurred when the greatest number and most severe fractures should be expected to occur. These results proved both that the AEDCS is capable of detecting AE characteristics and that the system may prove to be a useful tool in the study of AEs in wood.

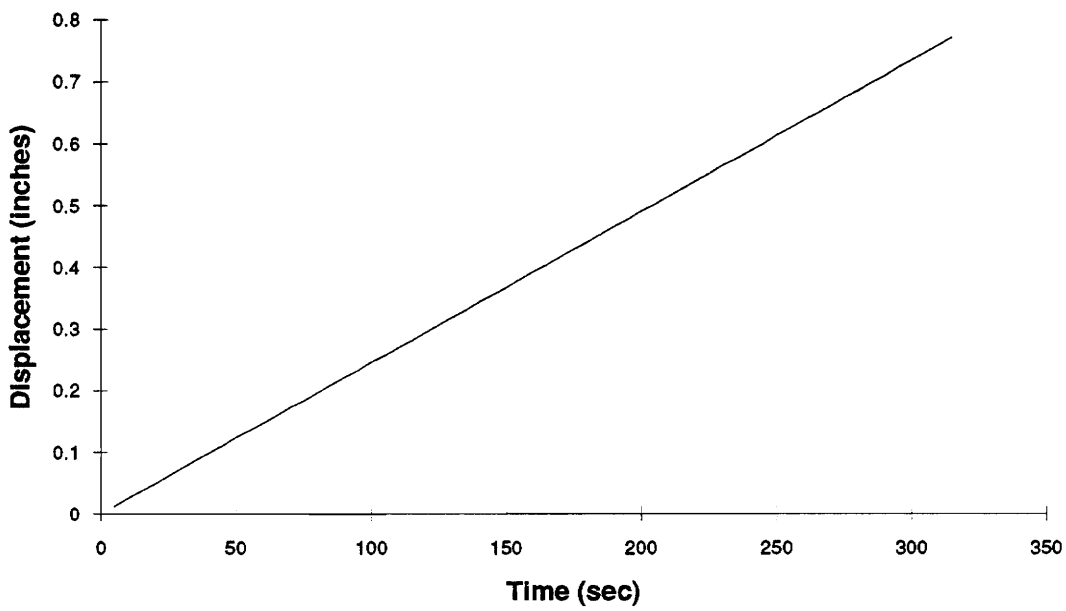

Figure 5-2. MTS Head Displacement for AE Tests

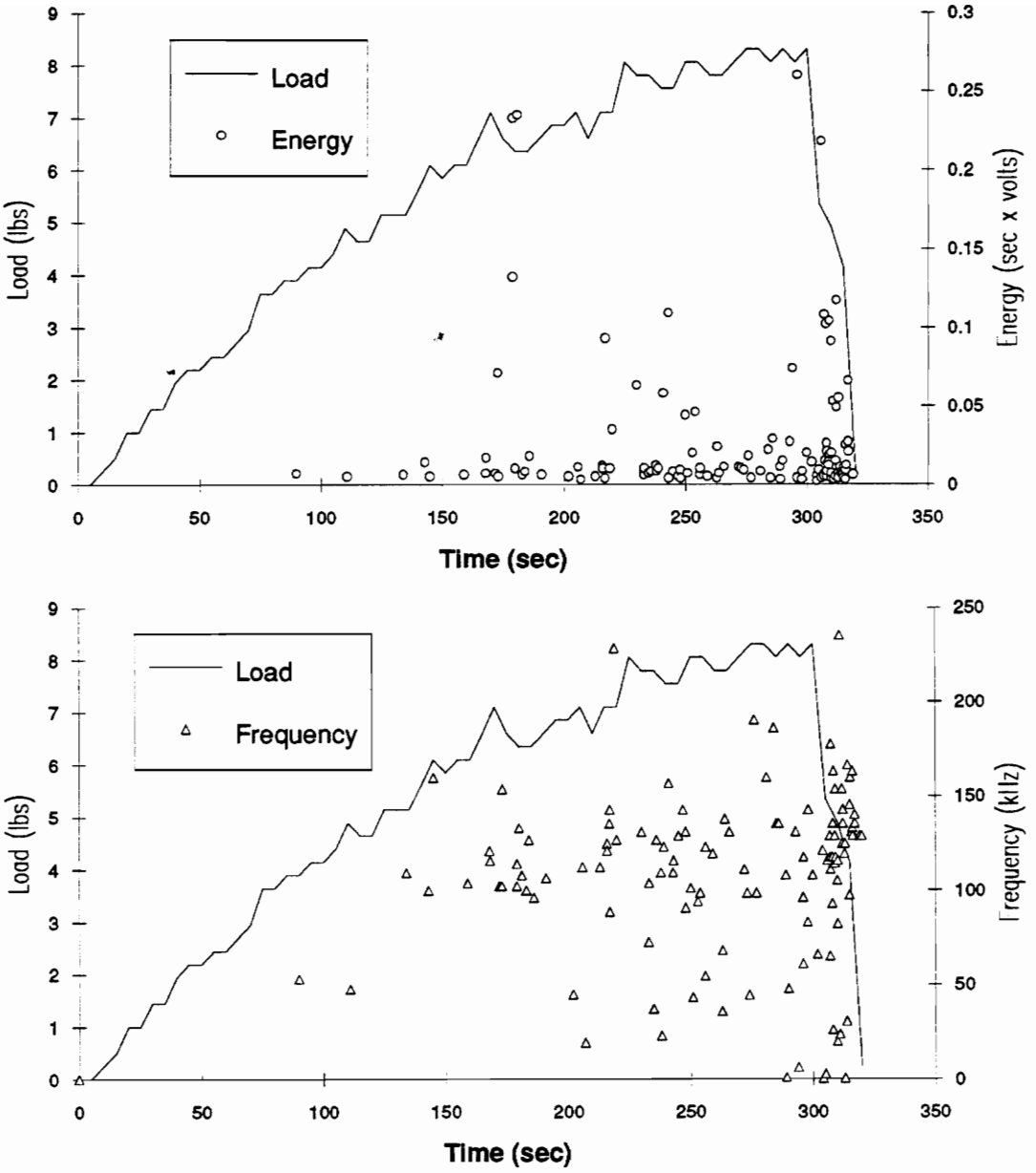

Figure 5-3. OSB Test Results

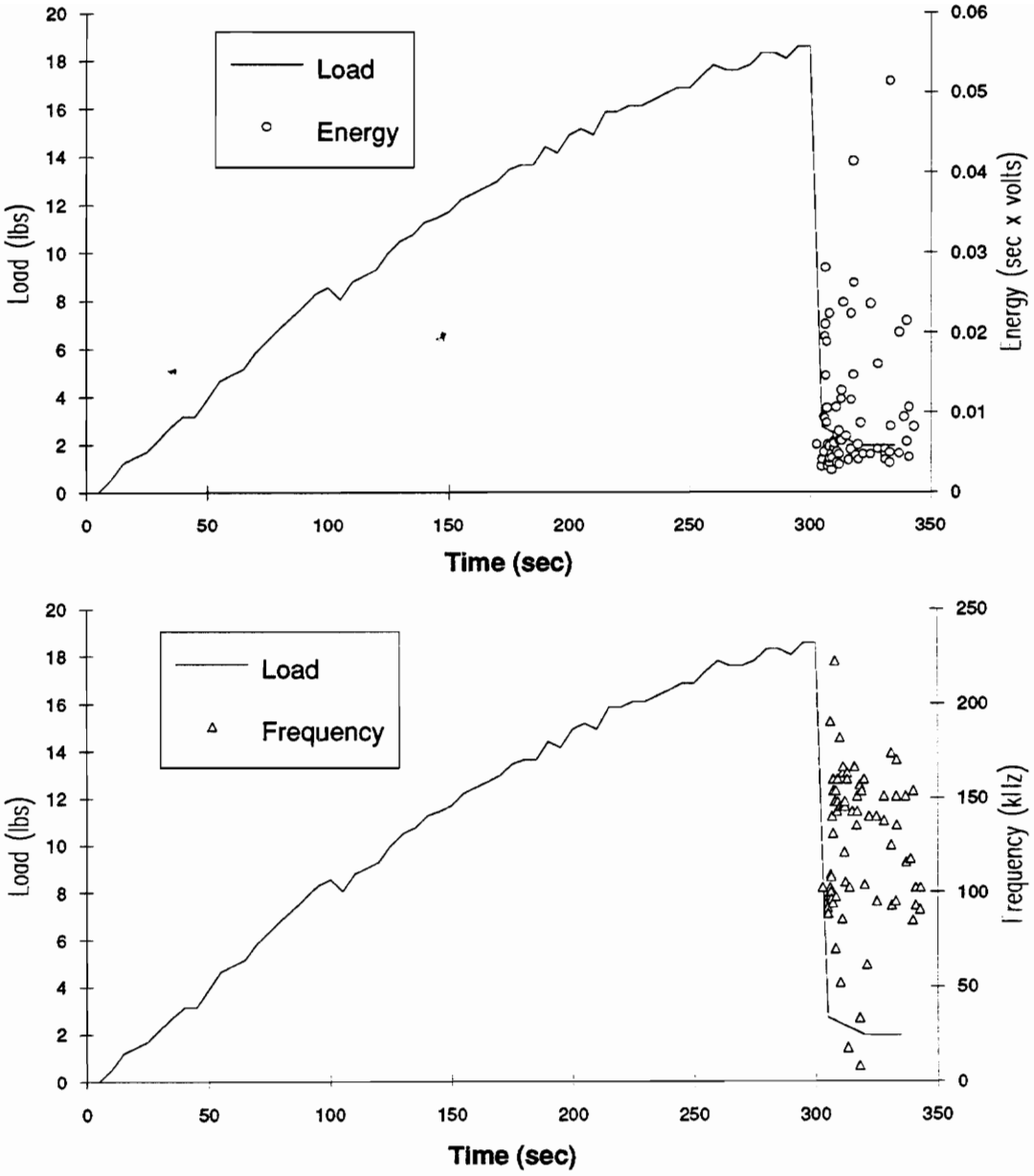

Figure 5-4. Masonite Test Results

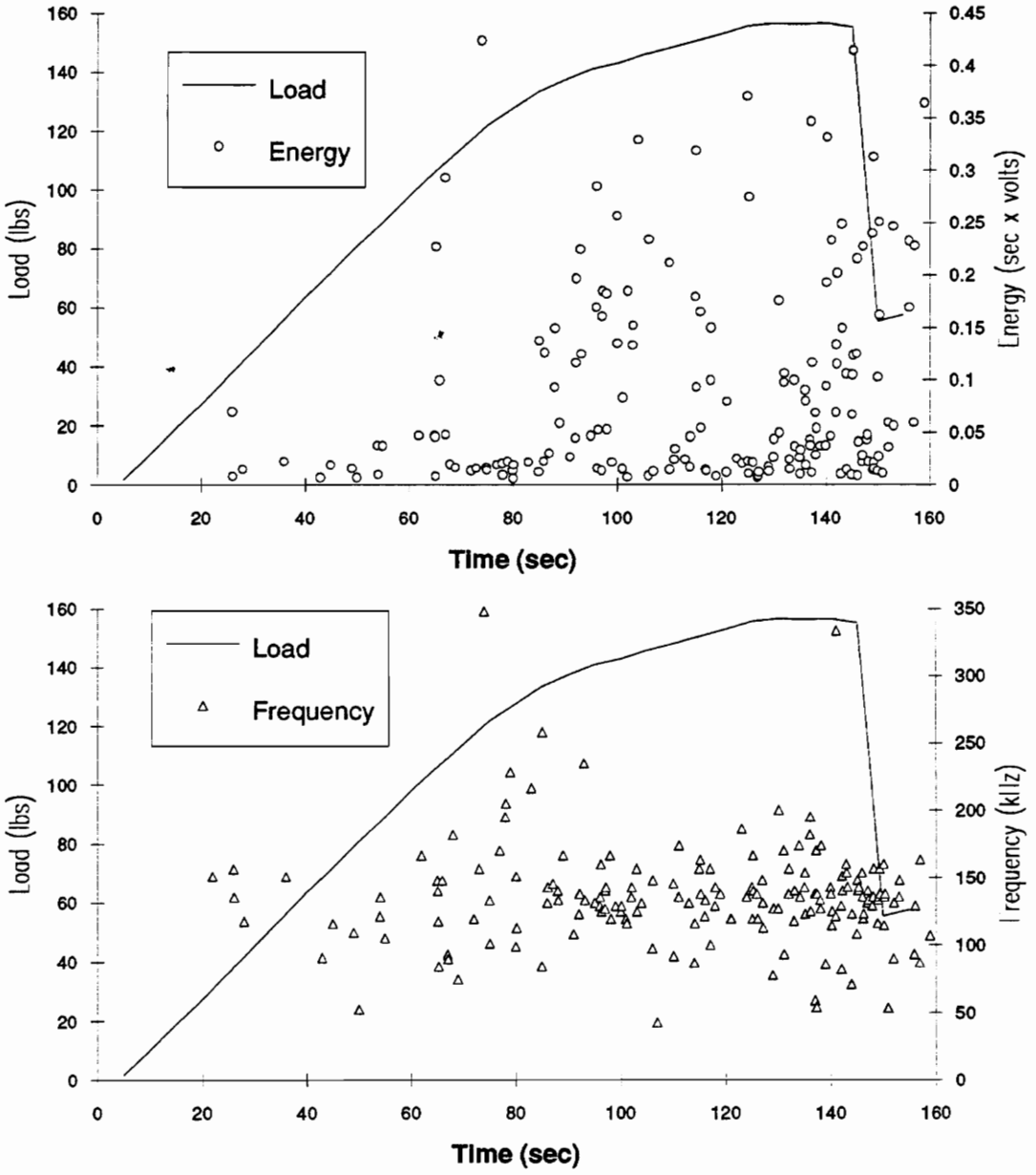

Figure 5-5. Plywood Test Results (cut with the grain)

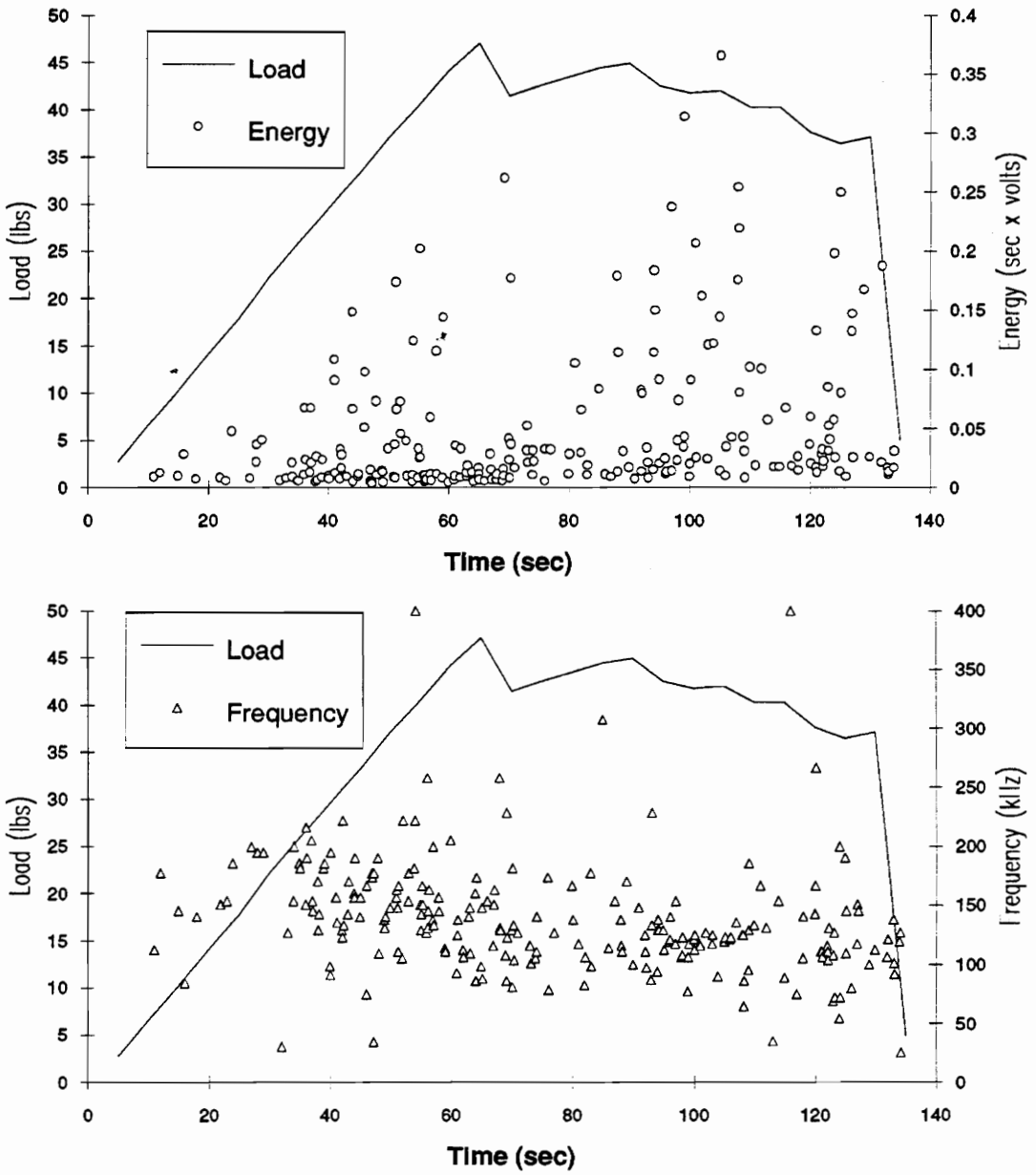

Figure 5-6. Plywood Test Results (cut across the grain)

Chapter VI

SUMMARY AND CONCLUSIONS

The purpose of this thesis was to design a system that will detect and characterize AE events. This device can be used in many applications that involve AE detection, such as destructive and non-destructive testing of wood.

The design process was started with the objective of achieving the functional requirements specified in section 2.1. The first step in this process was to determine how to derive the signals necessary to characterize an AE event. Next, the hardware needed to implement these signal derivations was designed. After the hardware was designed, it was necessary to interface the characteristic signals to the microprocessor system, which involved more hardware development. The software was then written to complete the implementation of all the design objectives. The system was then used in a mechanical testing application on wood to demonstrate the system's capabilities.

6.1 Performance

The overall performance of the system can be determined by examining how well the system performs the design objectives, keeping in mind that the objectives were functional requirements and not design specifications.

Most of the functions performed were constrained by the microprocessor system, such as the resolutions of the A/D and D/A converters. Some of the functions, on the other hand, have room for improvement. The performance of each function is discussed here separately.

6.1.1 Peak Detector

The purpose of the peak detector is to detect the greatest amplitude achieved by an AE event. The peak detector used in this system was not fast enough to detect the peak of a 150 kHz AE signal. This problem was bypassed by using the DC conversion of the AE signal, which closely resembled the envelope of the AE signal. The response time of the peak detector and AC to DC converter were not measured, but the hardware verification tests showed that these circuits were capable of handling frequencies within the detection range of the transducer used.

The resolution of the A/D converter used for peak voltage detection was 8 bits. This resulted in a peak voltage detection resolution of 60 mV for a 15 V detection range,

which was adequate for measuring AE event peak voltages in the tests conducted. The peak voltages measured varied throughout the 15 V detection range for most of the tests.

6.1.2 Duration Detector

The accuracy of the duration detector depends on how closely the output of the AC to DC converter resembles the AE signal and on the response time of the comparator used. As stated above, the AC to DC converter is adequate for the frequency range of the transducer used. The comparator used has a typical response time of around .4 μsec. Since these response times are nearly the same for negative and positive transitions, no error would be incurred when measuring the end of the event relative to the start of the event.

The resolution of the microprocessor timer is .5 μsec. This resolution is good for the types of AE events measured in the tests outlined in chapter 5 where event durations were typically in the hundreds of microseconds range.

6.1.3 Frequency Detector

The frequency detector used has several flaws. First, as stated in section 1.1, an AE event can contain many frequency components. The detector used can only determine the period of one cycle of an AE event, which may or may not be of significance. A more elaborate detection method, such as a fast fourier transform, would have required the AE signal to be sampled at a rate of almost 600 kHz and software to perform the needed algorithms. The microprocessor used was designed primarily as a microcontroller, and does not have the speed or processing power needed to implement a better frequency detection method.

The resolution of the period detector, which was .125 µsec, was limited by the rate of the clock used to gate the 8253 timer channel. An 8 MHz clock was used, which was the highest clock rate allowed for the 8253 timer chip. This resolution was poor because the typical AE events measured had periods less than 4 µsec.

6.1.4 Time of Occurence Detection

The microprocessor's real-time clock was used to record the time of occurence of an AE event. The RTC was only accurate to the second, which was inadequate for AE tests that produced many AE events within a one second interval. A higher resolution RTC should be used to increase the accuracy of measuring the exact time that events occur. A resolution of 1 millisecond would be addequate for most applications with a moderate rate of AE activity.

6.1.5 A/D and D/A Channels

The resolution of the A/D and D/A converters were fixed to 8 bits on the microprocessor board. This resolution was adequate for the D/A channels used to set the comparator threshold values because a higher resolution would not have affected the results of the AE tests conducted.

The resolution of the A/D channels provided for additional instrumentation can only be judged adequate by the application that they are being used for.

6.2 Project Evaluation

As a prototype piece of equipment, the AEDCS demonstrated that several characteristics of AEs could be recorded by a small, low-cost instrumentation device.

The device also proved that it could provide usefull data in a typical materials testing application. Correlations between AE event characteristics and stress/strain data were shown from data recorded by the AEDCS during these tests. It was also possible to distinguish between the different types of wood materials tested from the AE data recorded. These preliminary tests showed that the AEDCS could prove to be a valuable tool in the AE testing of materials field.

The device also had a coulple of short-comings that prohibited a complete success

rating. The real-time clock used proved to be inadequate in the measurement of event time of occurrence. This is a hardware shortfall that can be corrected by adding a more sophisticated RTC board.

The second short-coming was both hardware and design related. The method used to detect the frequency of a nearly random AE event wave was inadequate. The method used was capable of determining just one of the frequencies that were present during an AE event. It is unknown whether the frequency information that the AEDCS is capable of recording might provide usefull.

In addition to the shortfalls of the method, the resolution for detecting the period of AE events in the hundreds of kilo-hertz range was also inadequate. Hardware that can handle a much higher gate clock rate should be used if the method is shown worthwhile.

Aside from these short-comings, the goals of the project were achieved. All of the functional requirements outlined in section 2.1 were implemented. The device, as it stands, along with some of the modifications described in the next section, can be used as a valuable tool in the study of AE behavior in materials testing.

6.3 Future Modifications

The previous section detailed some areas of the system that have room for improvement. Many of these improvements may be necessary to achieve a high performance instrumentation device. The system as it stands, however, could be modified into a stand alone recording device that could be placed in a remote location. The recorded data could be downloaded from the system's memory at the operator's convenience. This would allow relatively inexpensive non-destructive testing of existing wooden structures, as well as numerous other non-laboratory AE testing applications. Modifications would have to be made to the system's software to allow the device to store all of the recorded information internally, and to allow the data to be extracted by a host computer at a later time.

Several hardware modifications may prove very useful. If a digital signal processing chip were to be added, for example, a fast fourier transform algorithm could be implemented that would give an accurate composition of an AE event's frequency content. As stated in previous sections, the required sampling rate and processing power required to implement an FFT algorithm is beyond the capabilities of the microprocessor system used in the AEDCS.

Also, the present system does not utilize very many of the microprocessor's interface capabilities. These capabilities could be used for more instrumentation, or to implement some of the other AE characterization methods mentioned in section 1.1.

Additional software routines, however, might cause the system to miss AE events that occur in rapid succession.

These software restrictions, along with some hardware restrictions, also prohibit the system from monitoring more that one transducer input. Ideally, many transducers would be used in an AE testing application to provide more data and to improve the reliability of the data. A microprocessor system with greater processing power would enable many different modifications and additions to the system, but cost would also increase.

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Appendix A

PROGRAM LISTING

```
HEX 0 2000 !
COLD


HEX

C000 TIB !
50 TIB 2+ !

2000 1FFF FF FILL
2004 DP !

B000 CONSTANT PORTA
B020 CONSTANT TCTL1
B021 CONSTANT TCTL2
B022 CONSTANT TMSK1
B023 CONSTANT TFLG1
B030 CONSTANT ADCTL
B031 CONSTANT AD0
B032 CONSTANT AD1
B033 CONSTANT AD2
B034 CONSTANT AD3
B031 CONSTANT AD4
B032 CONSTANT AD5
B033 CONSTANT AD6
B034 CONSTANT AD7
B040 CONSTANT CNTR0
B043 CONSTANT CNTLREG
BC40 CONSTANT DAC1
BC41 CONSTANT DAC2

VARIABLE VARADDRESS
C100 VARADDRESS !
: VAR
   VARADDRESS @ DUP 0
   2SWAP + VARADDRESS ! DROP
   CONSTANT ;

2 VAR VPEAK
4 VAR IC1TIME
4 VAR IC2TIME

2 VAR CR-AM/PM
2 VAR CR-MONTH
2 VAR CR-DAY
2 VAR CR-YEAR
2 VAR CR-HOUR
2 VAR CR-MINUTE
2 VAR CR-SECOND
2 VAR CR-DOW

BC00 CONSTANT BASE-ADDRESS
BASE-ADDRESS 0 + CONSTANT 1-SEC-DIG
```

```
BASE-ADDRESS 1 + CONSTANT 10-SEC-DIG
BASE-ADDRESS 2 + CONSTANT 1-MIN-DIG
BASE-ADDRESS 3 + CONSTANT 10-MIN-DIG
BASE-ADDRESS 4 + CONSTANT 1-HRS-DIG
BASE-ADDRESS 5 + CONSTANT 10-HRS-DIG
BASE-ADDRESS 6 + CONSTANT 1-DAY-DIG
BASE-ADDRESS 7 + CONSTANT 10-DAY-DIG
BASE-ADDRESS 8 + CONSTANT 1-MON-DIG
BASE-ADDRESS 9 + CONSTANT 10-MON-DIG
BASE-ADDRESS A + CONSTANT 1-YRS-DIG
BASE-ADDRESS B + CONSTANT 10-YRS-DIG
BASE-ADDRESS C + CONSTANT 1-DOW-DIG
BASE-ADDRESS D + CONSTANT REG-D
BASE-ADDRESS E + CONSTANT REG-E
BASE-ADDRESS F + CONSTANT REG-F

: TEN* A * ;

: TEN/MOD A /MOD ;

: HOLD-CLOCK
  5 REG-D C!
  BEGIN REG-D C@ 2 AND 0= UNTIL ;

: RELEASE-CLOCK
  0 REG-D C! ;

: READ-CLOCK
  HOLD-CLOCK
  10-SEC-DIG C@        TEN* 1-SEC-DIG C@ + CR-SECOND !
  10-MIN-DIG C@        TEN* 1-MIN-DIG C@ + CR-MINUTE !
  10-HRS-DIG C@ 4 AND                      CR-AM/PM  !
  10-HRS-DIG C@ 3 AND TEN* 1-HRS-DIG C@ + CR-HOUR   !
  10-DAY-DIG C@        TEN* 1-DAY-DIG C@ + CR-DAY    !
  10-MON-DIG C@        TEN* 1-MON-DIG C@ + CR-MONTH  !
  10-YRS-DIG C@        TEN* 1-YRS-DIG C@ + CR-YEAR   !
  1-DOW-DIG  C@                            CR-DOW    !
  RELEASE-CLOCK ;

: 2.R
  TEN/MOD 30 OR EMIT 30 OR EMIT ;

: SET-24-HR-MODE
  REG-F C@ F0 AND 4 = NOT
  IF
    1 REG-F C!
    5 REG-F C!
    4 REG-F C!
  THEN ;

: SET-CLOCK
  HOLD-CLOCK
  0 1-SEC-DIG 1+ C! 0 1-SEC-DIG C!
```

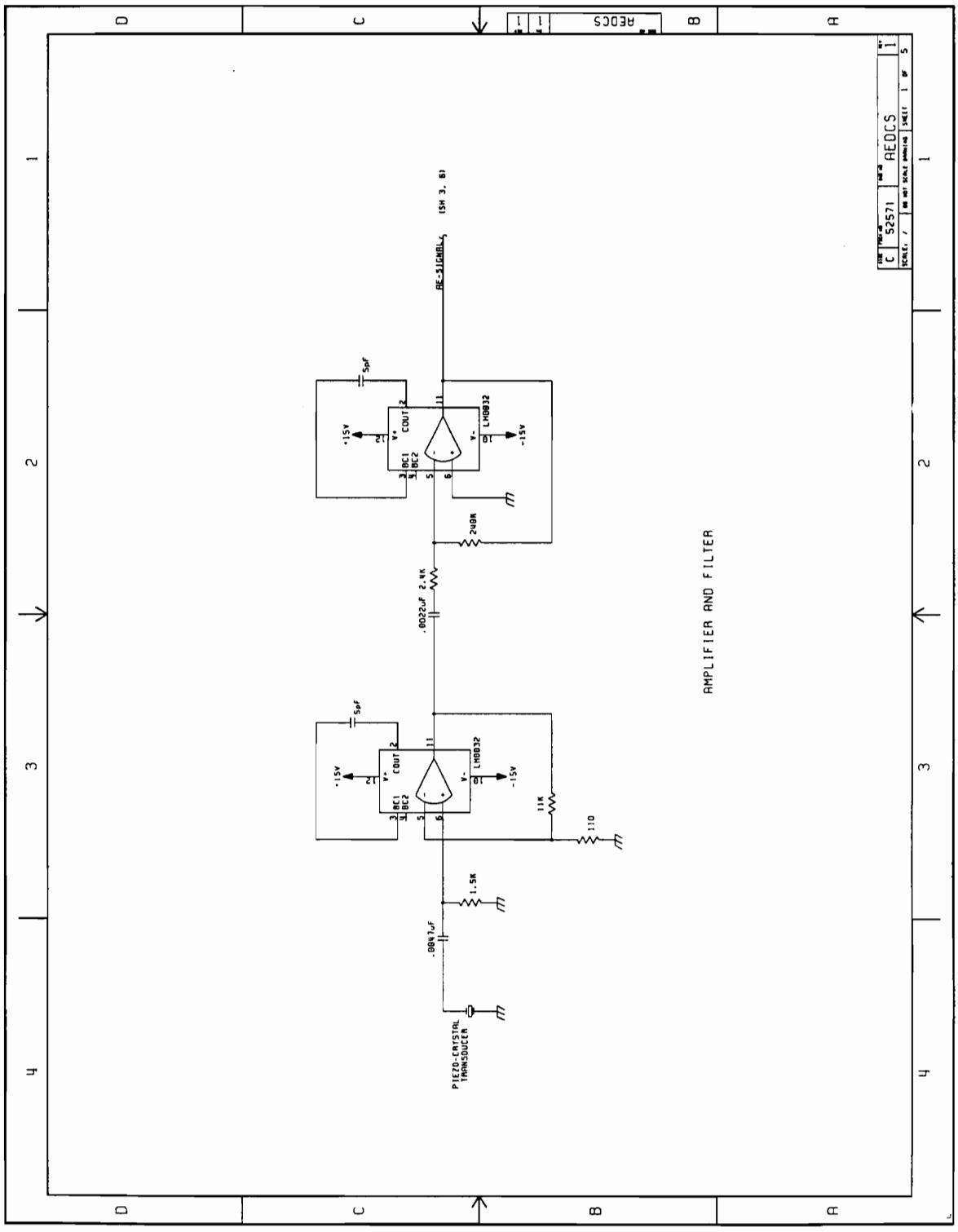
```
  CR-MINUTE @       TEN/MOD 10-MIN-DIG C! 1-MIN-DIG C!
  CR-HOUR   @       TEN/MOD 10-HRS-DIG C! 1-HRS-DIG C!
  CR-DAY    @       TEN/MOD 10-DAY-DIG C! 1-DAY-DIG C!
  CR-MONTH  @       TEN/MOD 10-MON-DIG C! 1-MON-DIG C!
  CR-YEAR   @       TEN/MOD 10-YRS-DIG C! 1-YRS-DIG C!
  CR-DOW    @                             1-DOW-DIG C!
  RELEASE-CLOCK ;

: RESET-CLOCK
    0 REG-D C!
    1 REG-E C!
    0 REG-F C!
    DECIMAL
    67 CR-YEAR !
    07 CR-DAY !
    06 CR-MONTH !
    00 CR-MINUTE !
    00 CR-HOUR !
    SET-24-HR-MODE
    SET-CLOCK ;

: CLK
  READ-CLOCK
  CR-HOUR @ 2.R ." ," CR-MINUTE @ 2.R ." ," CR-SECOND @ 2.R ;

: READ-AD1
    10 ADCTL C!
    BEGIN ADCTL C@ 80 AND UNTIL ;

: READ-AD2
    14 ADCTL C!
    BEGIN ADCTL C@ 80 AND UNTIL ;

: ST1
   102 UM* 64 UM/MOD SWAP DROP
   DAC1 C! ;

: ST2
   102 UM* 64 UM/MOD SWAP DROP
   DAC2 C! ;

: PA3LOW
   PORTA C@ F7 AND PORTA C! ;

: PA3HIGH
   PORTA C@ 08 OR PORTA C! ;

: RESET-PEAK
   PA3HIGH PA3LOW ;

: RESET-COUNTER0
   30 CNTLREG C!
   FF CNTR0 C!
```

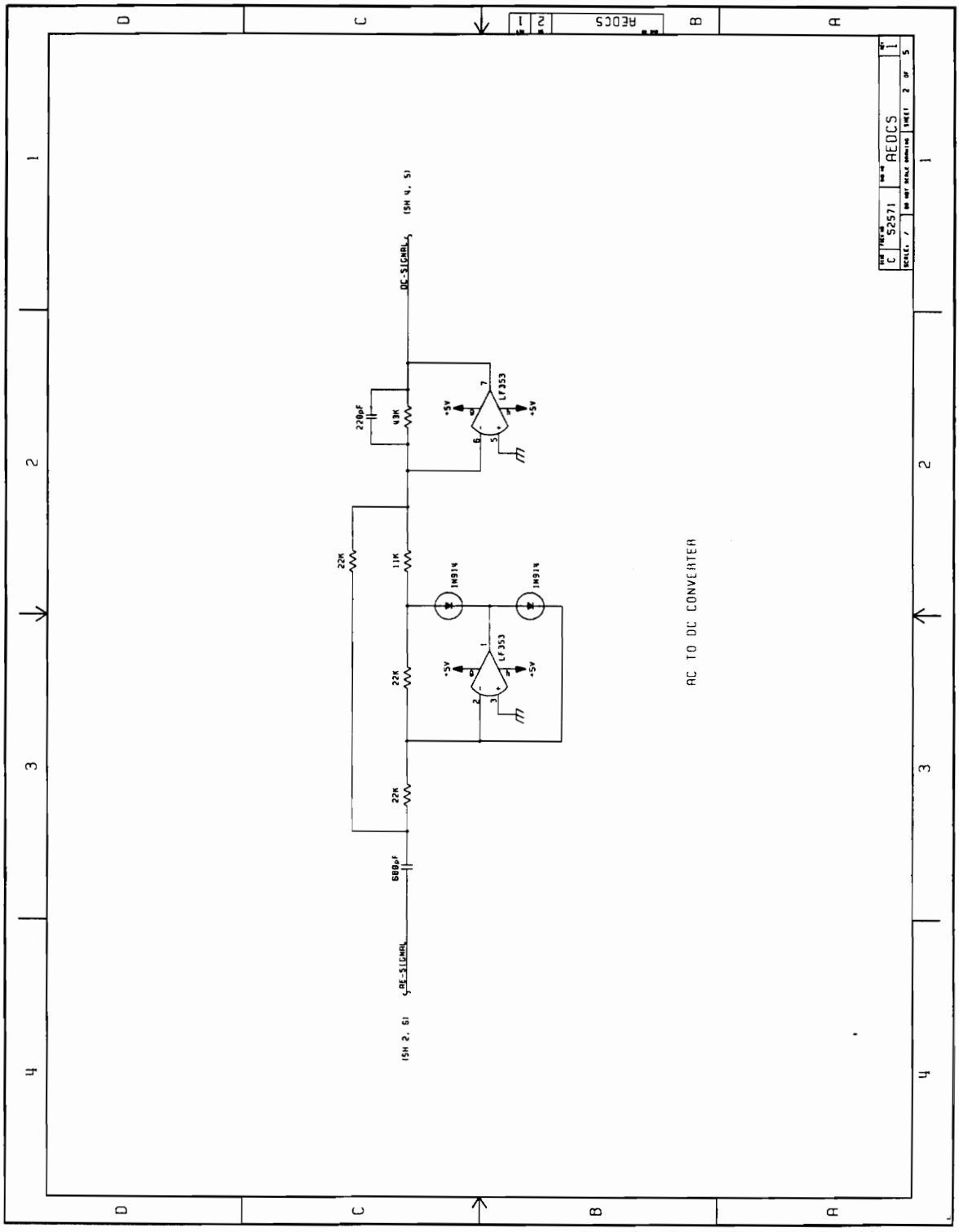
```
   FF CNTR0 C! ;

: READ-COUNTER0
   00 CNTLREG C!
   CNTR0 C@
   CNTR0 C@ 100 * +
   FFFF SWAP - DUP
   DUP 0 = IF DROP 4E20 THEN
   DUP 4E20 U< NOT IF DROP 4E20 THEN
   0 13880. 2SWAP DROP UM/MOD SWAP DROP ;

: A->V
    C@ C4 UM* 64 UM/MOD SWAP DROP S->D
    <# # # 2E HOLD #S #> TYPE ;

: DISPINFO
   CLK ." , "
   READ-COUNTER0 S->D <# # 2E HOLD #S #> TYPE ." , "
   IC2TIME @
   IC1TIME @
   -
   0A UM* 2 UM/MOD SWAP DROP S->D
   <# # 2E HOLD #S #> TYPE ." , "
   VPEAK C@ 5DC UM* FF UM/MOD SWAP DROP S->D
   <# # # 2E HOLD #S #> TYPE ." , "
   AD1 A->V ." , " AD2 A->V ." , " AD3 A->V ." , "
   READ-AD2
   AD4 A->V ." , " AD5 A->V ." , " AD6 A->V  CR ;

: IC2INT
   00 TMSK1 C!
   TIC1 @ IC1TIME !
   TIC2 @ IC2TIME !
   READ-AD1 AD0 C@ VPEAK C!
   DISPINFO
   RESET-COUNTER0
   RESET-PEAK
   FF TFLG1 C!
   02 TMSK1 C!
;

CODE LOWIC2
  CC C, ' IC2INT CFA ,
  BD C, ATO4 ,
  3B C,
END-CODE

CODE-SUB CLI
  0E C,
  39 C,
END-CODE

CODE-SUB SEI
```

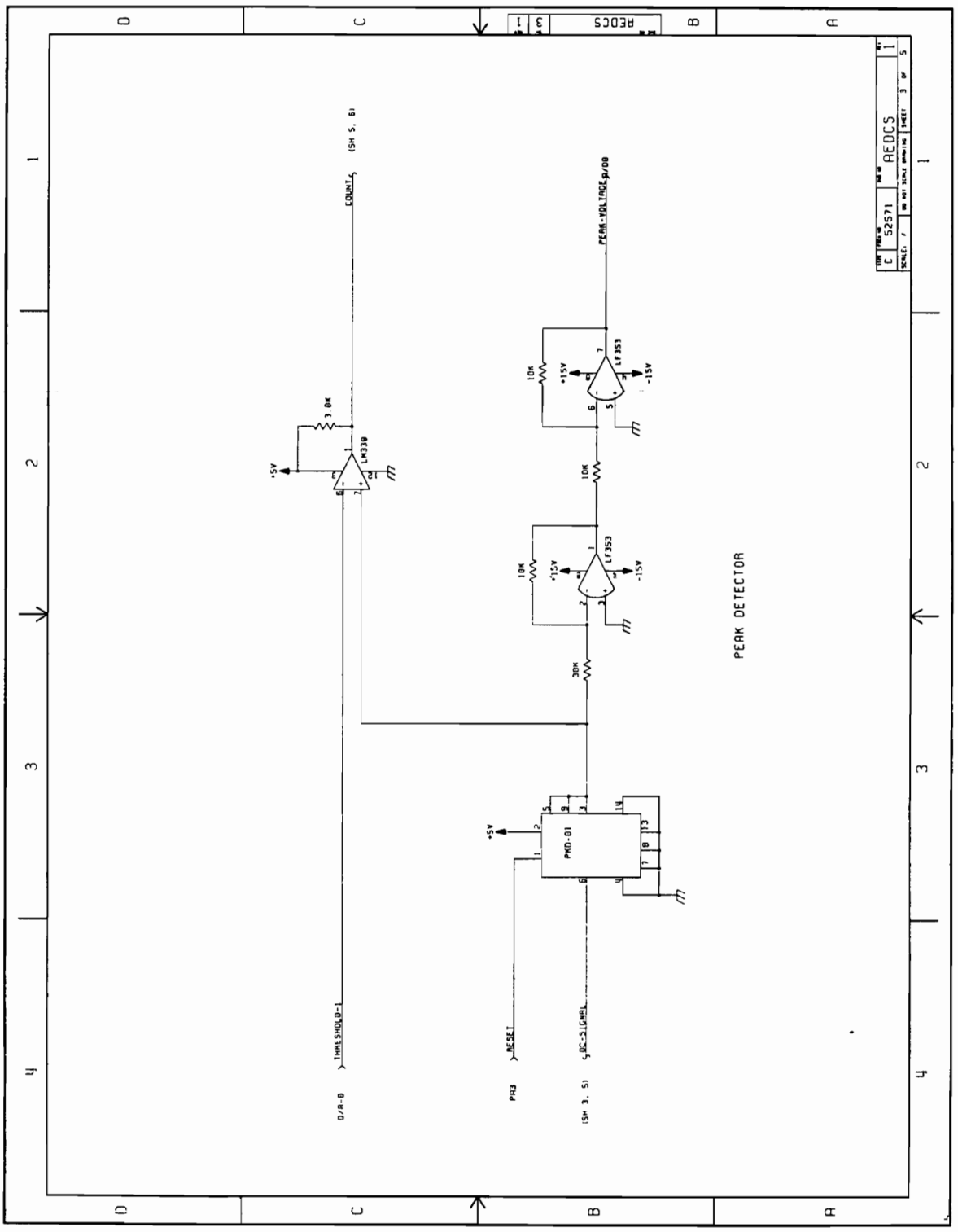
```
  0F C,
  39 C,
END-CODE

: VEC-INIT
  7E B7E0 EEC!
  [ ' LOWIC2 @ >< FF AND ] LITERAL B7E1 EEC!
  [ ' LOWIC2 @    FF AND ] LITERAL B7E2 EEC! ;

: START-TEST
  18 TCTL2 C!
  FF TFLG1 C!
  SEI
  VEC-INIT
  RESET-PEAK
  RESET-COUNTER0
  RESET-CLOCK
  02 TMSK1 C!
  CLI ;

: STOP
  00 TMSK1 C! ;

: RESTORE-USER-AREA
    3F96 06 6A CMOVE ;

: MAIN
    RESTORE-USER-AREA
    DECIMAL
    20 ST1
    05 ST2
    CR CR
    ."        Acoustic Emission Logging Device" CR CR
    ."             by David D. Bettinger" CR CR CR CR ;
```

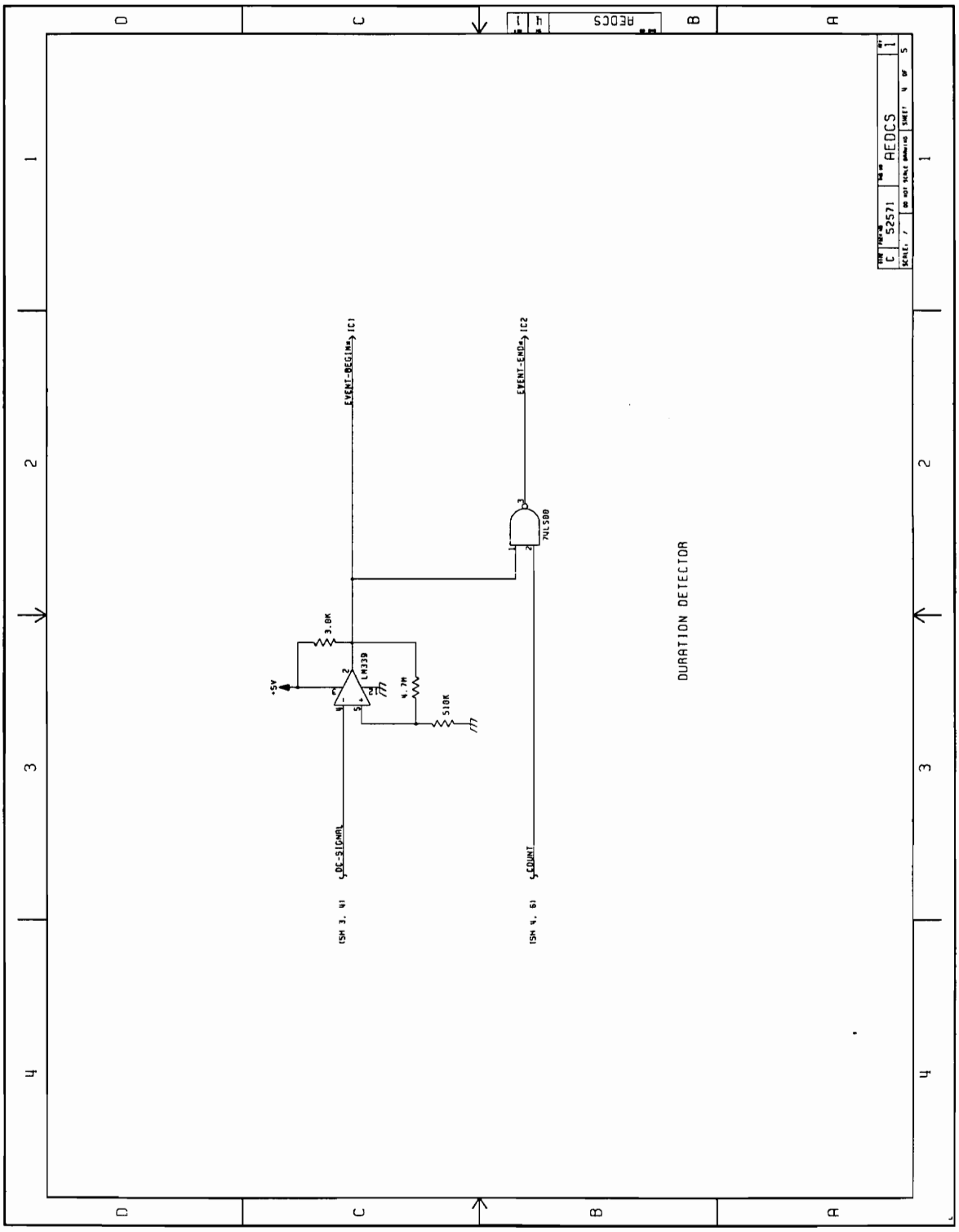
Appendix B

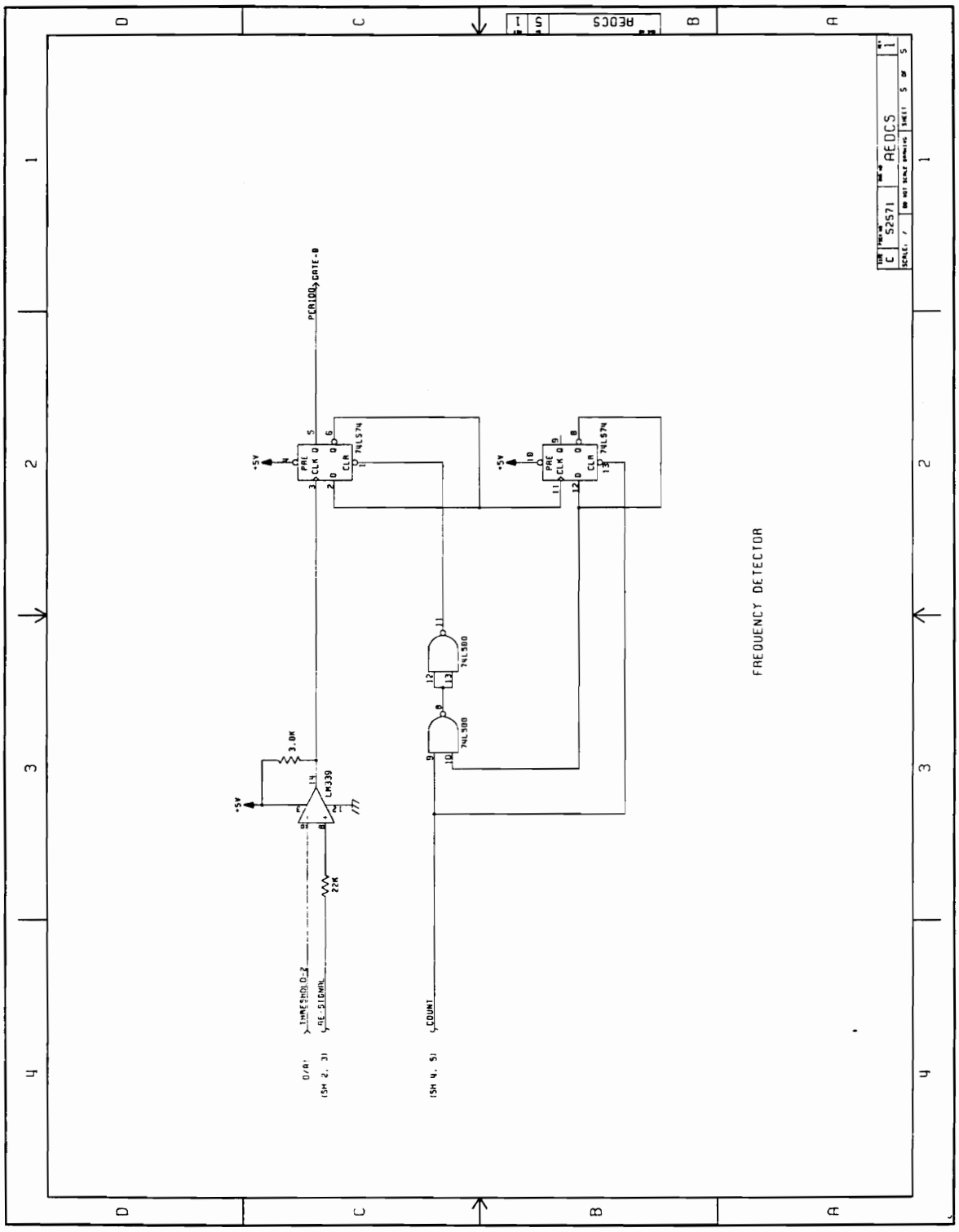
SCHEMATIC DIAGRAMS


AMPLIFIER AND FILTER
AEDC5
C 52571
SCALE: /
SHEET 1 OF 5
RF-SIGNAL
ISH 3, B1
5pF
.15V
COUT
BC1
BC2
V+
V-
LM6032
-15V
240R
.0022uF
2.4K
11K
110
1.5K
.0047uF
PIEZO-CRYSTAL
TRANSDUCER


AEDCS
AC TO DC CONVERTER
DC-SIGNAL
RF-SIGNAL
220pF
43K
22K
11K
22K
22K
680pF
1N914
1N914
LF353
LF353
+5V
-5V
S2571


PEAK DETECTOR
AEDCS
52571
PEAK-VOLTAGE
COUNT
THRESHOLD-I
RESET
DC-SIGNAL
PXD-01
LM339
LF353
3.0K
10K
30K
+5V
+15V
-15V


AEDCS
52571
EVENT-BEGIN
EVENT-END
DURATION DETECTOR
3.8K
LM339
4.7M
510K
5V
74LS00
DC-SIGNAL
COUNT


AEDCS
C 52571
AEDCS
FREQUENCY DETECTOR
PERIOD_GATE-B
74LS74
74LS00
LM339
3.0K
22K
+5V
TIMESHOLD_2
OE-SIGNAL
COUNT
(SH 2, 3)
(SH 4, 5)

Vita

David Darwin Bettinger was born on June 7, 1967 in Syracuse, New York. His secondary schooling was at Baker High School in Baldwinsville, New York, where he graduated in June 1985. In September 1985 he joined Virginia Tech, Blacksburg, Virginia, and graduated from there in May 1989 with a Bachelor of Science degree in Electrical Engineering. He continued his studies in September 1989 at Virginia Tech in pursuit of a Master of Science degree in Electrical Engineering.