

CHAPTER 5: SPATIAL LIGHT MODULATOR SYSTEM

5.1 SPATIAL LIGHT MODULATOR

Spatial Light Modulator (SLM) is a device that modulates the coherent light based on its control input. It is used in the LIM to encode output patterns for areal mapping. The SLM accepts the pattern information from the host computer and converts coherent light input from laser source into output patterns. The commercially available SLMs are classified based on the following criteria [11]:

Method of writing the input patterns on the SLM: This is done either electronically or optically. In the electronic method, each pixel on SLM is supplied with a voltage that represents the shade and intensity of the corresponding pixel in the input pattern. This is implemented by either having an electrode for each pixel that are scanned by an electron beam or by having addressable electrodes to which the necessary voltage is applied. In the optical method, the input pattern is converted to an optical image and is cast on the SLM.

Coherent light requirements: The SLM is designed for a particular wavelength or a range of wavelengths.

Modulation Scheme: The three characteristics of the input light that can be modulated are its amplitude, phase and polarization. The SLMs available differ in the way they modulate the above characteristics, in the number of characteristics being modulated, and the achievable modulation efficiency.

Quality of the output: The qualities of the output pattern used to distinguish between SLMs are the resolution, contrast, uniformity and number of gray levels.

Setup and hold time: Setup time refers to the time taken the by SLM to erase the existing pattern and write the next pattern. Hold time is the duration of time for which the pattern written exists.

Other specifications and requirements: This includes the size, the power consumption, range of temperature in which the SLM can be operated.

5.2 SLM Selection

A number of commercially available SLMs were compared based on their output pattern, overall size, modulation efficiency, operating wavelength, and cost. The comparison of the SLMs manufactured by Displaytech Inc., Spatialight Inc., and Sinectic Technology are provided in Table 5.1. Based on the comparison, the SLM manufactured by Displaytech is chosen for the LIM.

Table 5.1 Comparison Of Commercially Available SLMs

Parameters	Displaytech Inc.	Spatialight Inc.	Sinectic Technology
Array size	256 x 256	640 x 480	256 x 256
Pixel pitch (μm)	15	20	40
Active area (mm)	3.84 x 3.84	14.08 x 10.24	10.24 x 10.24
Overall size (inches)	0.51 x 0.51 x 0.34	1.25 x 1.25 x 0.35	0.55 x 0.25 x 0.14
Efficiency	65%	60%	60%
Peak operating wavelength (nm)	690	1100	633
SLM full frame rate (Hz)	3,000	288	3,000
Cost	\$6,000	\$17,000	\$7000

5.2.1 Principle of Operation of SLM

Displaytech's SLM is a reflective type SLM made of Ferroelectric Liquid Crystal (FLC) material mounted on a conventional CMOS VLSI chip. The function of the silicon backplane is to serve as the modulator mirror as well as the addressable electrode. The operation of FLC devices is based on the principle of birefringence. Birefringence is the phenomenon in which the phase velocity of an optical wave propagating in the crystal depends on the direction of its polarization [4]. Thus, when a light beam is incident on a FLC device in a direction other than the optic axis of the device, two beams whose polarization are perpendicular to each other are reflected as

output by the device. By applying a voltage to the FLC device, its optic axis is aligned in a direction perpendicular to the electrode plates. A change in the polarity of the voltage results in rotation of the optic axis. By using a combination of the FLC crystal, suitable polarizing optics and by switching the polarity of the applied voltage, it is possible to transmit or absorb an input light beam. The FLC device can be used to perform both amplitude and phase modulation of the input light.

Amplitude Modulation System

The arrangement consisting of the FLC device, the beamsplitter and the two polarizers is shown in Figure 5.1.

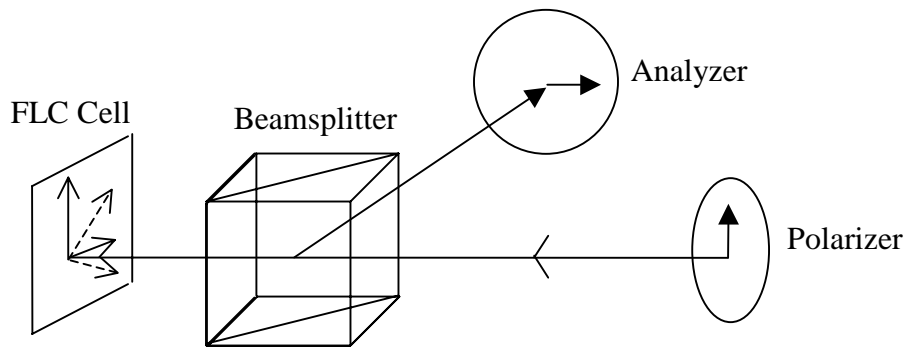


Figure 5.1 Amplitude Modulation System

The input polarizer is used to polarize the input light while the output polarizer is used to analyze the output from the FLC device. The function of the beamsplitter is to separate the input and output beams. The orientation of the FLC is represented by the two pairs of perpendicular lines. The solid lines represent the "on" state of the FLC and the dashed lines represent the "off" state. During the "on" state the incident light passing through the FLC is rotated by 90° while in the "off" state the incident light is unchanged. Light reflected from the FLC, which has the same polarization as the incident light is blocked by the beamsplitter, and the light with its polarization rotated by 90° , is reflected by the beamsplitter to the analyzer. Hence the polarization of the analyzer and the input polarizer are crossed with respect to each other.

Phase Modulation System

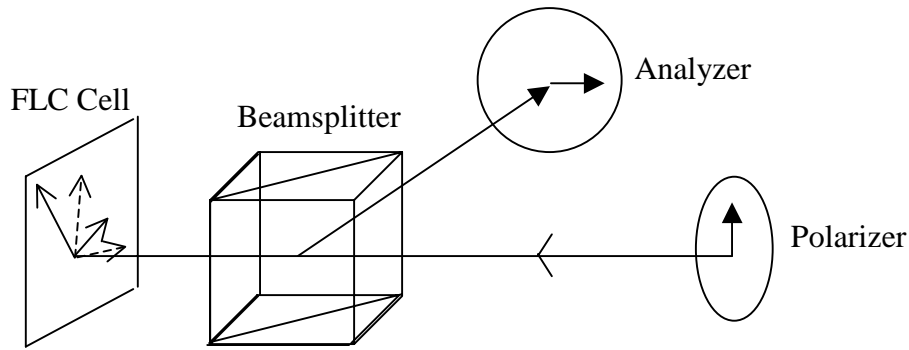


Figure 5.2 Phase Modulation System

The arrangement for phase modulation is similar to the amplitude modulation system and is shown in Figure 5.2. However, the polarization vector of the incident light is aligned, so that it bisects the transmission axes of the FLC. While in the "on" state the reflected light from the FLC is rotated by 45° in the clockwise direction, in the "off" state the reflected light is rotated by 45° in the counter clockwise direction. Thus the resultant separation of the two reflected beams is by 90° as in the amplitude modulation scheme. The beamsplitter either transmits or absorbs the beam depending on the direction of rotation of the polarization of the reflected light.

The SLM purchased for the LIM is an amplitude modulator.

5.2.2 Device Description

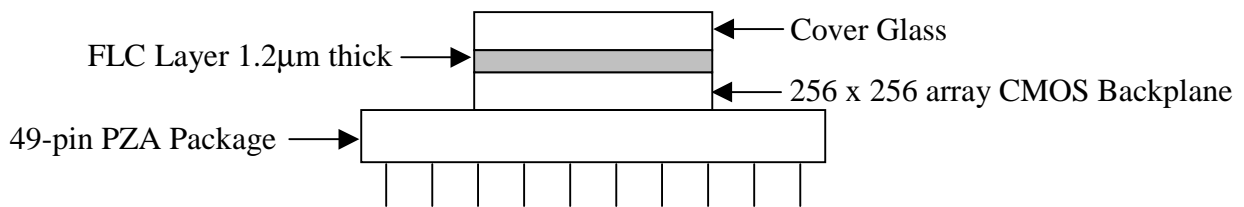


Figure 5.3 SLM Cross Section

The SLM consists of a thin layer of the FLC material sandwiched between a glass window coated with a transparent conductive layer and the CMOS backplane. The cross section of the device is shown in Figure 5.3.

The silicon backplane (Figure 5.4) that consists of the active area, the apron and the mask are manufactured using the standard 0.6 μm CMOS process. The active area contains individually addressable 65,536 standard SRAM cells arranged as a 256 x 256 array. The ratio of the area covered with pixels to the total active area, known as the "fill factor" is 87%. Bordering the active area is a contiguous ring of metal known as the "apron". This apron containing several "fiducial" pixels is connected to a single pin in the final package. The fiducial pixels, which are independent of the apron are electrically connected to each other and are driven using a single pin in the package. The apron can be driven to function as the border to pattern in the active area and the fiducial pixels can be used for device alignment.

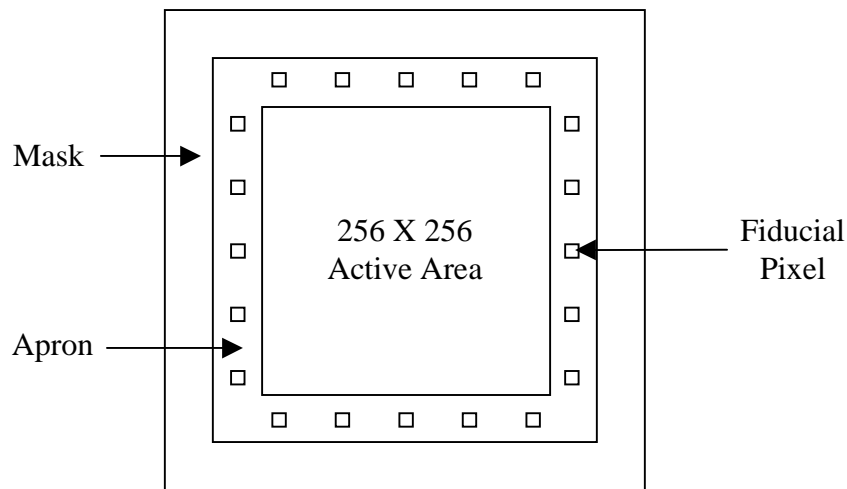


Figure 5.4 CMOS Backplane View

A glass window coated with indium tin oxide (ITO) is fixed to the SRAM backplane with a thickness controlled adhesive, leaving a small gap between the SRAM and the window. The ITO functions as the transparent conductive layer and the device is tuned to different wavelengths by changing the thickness of the gap. The FLC material is filled in the small gap via capillary action. The SLM is packaged as a 49-pin Pin Zigzag Array (PZA), which contains two 5 x 5, 0.1" center-to-center pin arrays arranged in a staggered manner. The PZA package is roughly a 0.5" square and is fixed onto a 2" circular mount. The circular mount contains the ribbon jack to connect the driver to the SLM.

5.2.3 Device Characteristics

Device response times: The maximum usable frame rate of the SLM is defined by the electrical write time and the FLC rise/fall time. The electrical write time is the time required for writing one full frame of data on the SLM. The SLM contains 65,536 pixels; uses a 32-bit wide data bus; and can be clocked at a maximum speed of 80MHz. Using the above values, we obtain a minimum electrical write time of 25.6 μ s. However, in practice, the electrical time is determined by the speed of the driver electronics. The FLC rise/fall time is the time required by the FLC material to respond to electrically written data. This time depends on the thickness of the FLC material and the operating voltage of the SLM. The SLM purchased has a thickness of approximately 1 μ m (corresponding to 630 – 690 nm) and is operated using standard 5V supply. The FLC response time for the above specifications is about 150 μ s. The maximum useable frame rate is the reciprocal of the sum of the electrical write time and the FLC response time. The sum of the two factors (25.6 + 150 μ s) yields a maximum rate of 5 kHz. Most of the applications using the SLM require that the D.C. balance condition is maintained across the FLC and hence the inverse image of each pattern is written on the SLM. This reduces the maximum frame rate by half.

Device Contrast: The SLM system in an application consists of the SLM and the necessary polarizing optics. The device contrast is the ratio of the light intensity transmitted through the system in the "on" state to that transmitted in the "off" state. The "off" state is the one when the polarizing optics has been adjusted to prevent any transmission. According to the specifications, the SLM system has a contrast ratio of 100:1.

Device Throughput: The optical efficiency of the SLM is the percentage of the input optical power which is reflected to a detector in the "on" state, when the SLM system has been adjusted for best extinction in its "off" state. According to specifications at 633 nm the SLM has an optical throughput greater than 25%.

Spatial Uniformity: The above mentioned characteristics are obtained by integrating the entire pixelated area of the SLM and hence provide the measure of performance in a global sense. The spatial uniformity among the pixels is obtained by studying the alignment uniformity, gap thickness uniformity, and reflected wavefront flatness. Alignment uniformity refers to the proper alignment of the FLC and it affects the contrast of the system. When there is uniform alignment,

the contrast of the reflected image remains constant at its center as well as its extremities, even when the device is rotated to different orientations. Non uniformity in the gap thickness between pixels results in different areas of the devices tuning to different wavelengths. When an "all pixels on" pattern is written on the SLM and viewed in the presence of white light, a system with non uniform gap thickness displays colored fringes as output. The wavelength to which a particular portion is tuned is directly proportional to gap thickness. Another factor used to study spatial uniformity is the overall flatness of the reflected wavefront. Any discontinuity in the phase of the reflected wavefront will render the device unsuitable for phase-sensitive applications.

5.3 Evaluation of spatial uniformity of the SLM

The factor, which has a major effect on the quality of the pattern from the SLM, is its spatial uniformity. The following experiment was performed to study the spatial uniformity of the Displaytech SLM.

Experimental setup:

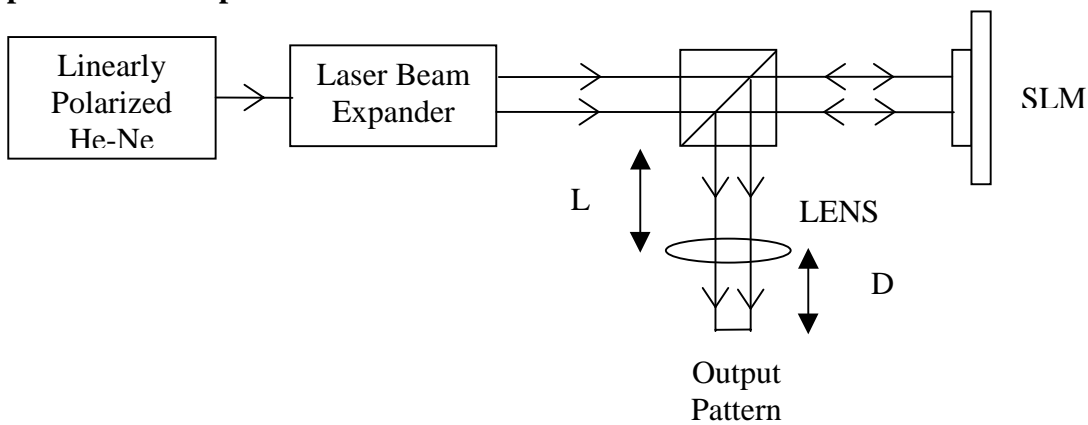


Figure 5.5 Spatial Uniformity Of SLM

Experimental Procedure

1. Align the laser source and the beam splitter. Rotate the laser such that the intensity of light input to the SLM is maximum and the intensity of light output from the other faces of the beamsplitter are minimum.

2. Align SLM with the laser source and the beam splitter to ensure that the input to the SLM is parallel.
3. Insert a lens and adjust the distance between the lens and the beam splitter till the best output pattern is obtained.

Factors considered in determining the quality of the output pattern

1. Shape: The output pattern should be a perfect square
2. Contrast: "ON" pixels should be perfectly bright and "OFF" pixels should be perfectly dark
3. Diffraction: The edges of each line in the pattern should be sharp and the edge of the pattern as a whole should be sharp.

Results

1. The SLM provides maximum contrast when a lens of focal length 8.75 cm is used.
2. The distance between the beam splitter and the lens is 6.6 cm.
3. The distance between the lens and the screen is 110 cm.

The results indicate that it is possible to obtain an output of reasonable quality and hence indicates that the spatial uniformity of the SLM is acceptable. An output pattern of poor quality would have indicated that the SLM does not have good spatial uniformity.

5.4 The SLM system

The LIM designed at FEORC is a 6 x 5 x 3.8 cubic inches box. The driver provided by Displaytech is bigger than the LIM itself. Hence, a driver to the SLM is designed so that it can be mounted on 6.0 x 3.8 square inches wall of the LIM. There is a slot in the LIM to accommodate the cable that runs from the driver to the SLM.

The SLM system used in the LIM consists of the SLM, the beamsplitter, the host computer and the driver. The need for the beamsplitter was explained in the previous section. The function of the host computer is to control the SLM in real time through the driver which includes sending command signals to the SLM and displaying signals received from the SLM. The patterns used

for surface profiling are stored in the host computer. The number of patterns needed to profile a surface is not constant and hence it is difficult to provide a definite memory space in the driver to store the pattern. Further, provision of a large memory space in the driver leads to an increase in the size.

The driver is the interface between the host computer and the SLM. The function of the driver is to accept the patterns from the computer and write them onto the SLM. When the LIM is used for surface profiling, the projected patterns have to change at the rate in which they can be captured by the CCD camera. In United States, the frame rate of video cameras is 30Hz. Hence, the pattern has to change once every (1/30) second. Thus, the new pattern has to be written onto the SLM during the retrace period of the camera. It is not possible to achieve such high data rate by directly connecting the parallel communication port of the host computer to the SLM. The driver accepts the next pattern from the host computer, when the current pattern is being scanned by the camera and stores it. The pattern is then written onto the SLM during the retrace period. The driver has circuits necessary to synchronize the host computer, the SLM, and the CCD camera.

5.5 Design of the driver

The block diagram of the driver shown in Figure 5.6 is based on the functions carried out by the driver. The major functions of the driver are:

- Accept instructions from the host computer and decode them.
- Accept the pattern from the host computer.
- Store the pattern till the retrace period of the camera begins.
- Write the pattern onto the SLM.
- Synchronize the above mentioned operations.

A microcontroller was chosen to function as an interface between the host computer and the SLM and to function as the on-board control unit of the driver. The selection of a microcontroller suitable to be used in the LIM was done by DCS Corporation. The microcontroller accepts instructions from the host computer, decodes it and generates its own

instructions, which are used for internal operations of the driver. The data corresponding to the pattern is received by the microcontroller and sent to the on board memory. A high speed First-In-First-Out (FIFO) memory device is used to store the pattern received from the host computer when the camera is scanning the current pattern. A Programmable Logic Device (PLD) functions as a state machine to sequence the flow of operations in the driver. A clock and a video signal decoder are used for synchronization purposes.

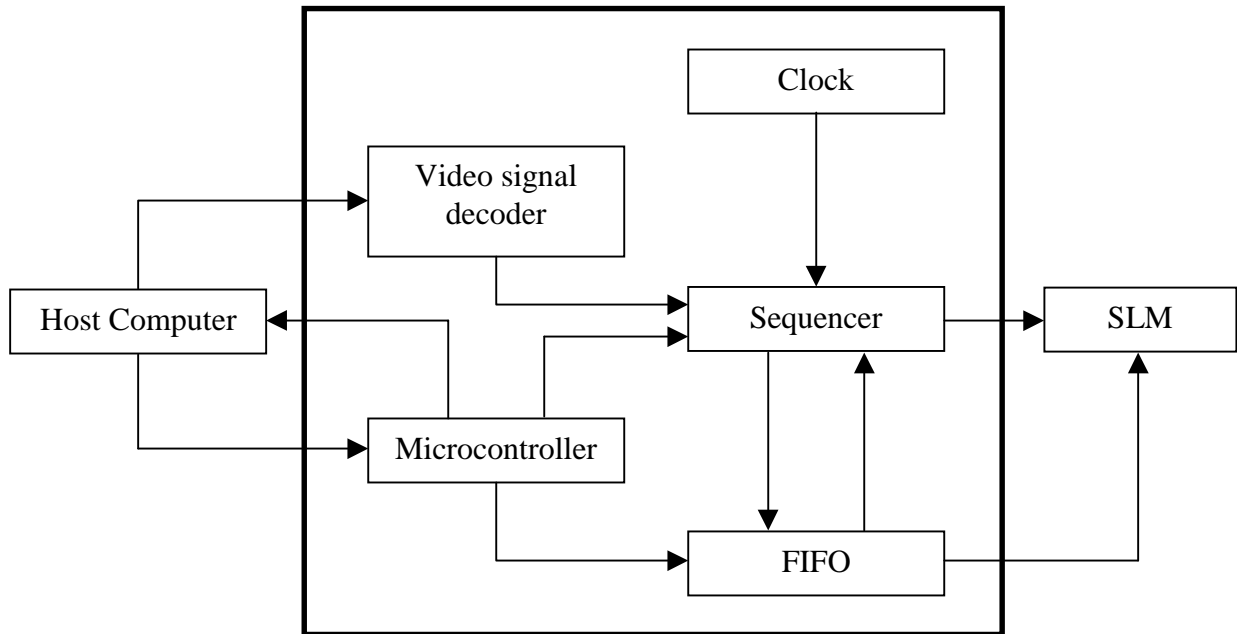


Figure 5.6 Block Diagram Of SLM Driver

The design of the video signal decoder, the sequencer, the FIFO, the clock, and the pseudocode of the software to interface the host computer with the SLM are discussed in this thesis. The design involving the use of the microcontroller, its associated software, and the programming of the PLD were completed by DCS Corporation.

5.5.1 Clock

The purpose of the clock signal is to enable reading of the data from the FIFO during the falling edge of the signal and to write the data in the SLM on the subsequent rising edge. When the read line of the FIFO is enabled, valid data is placed on the data bus of the FIFO after 15 ns. Thus the

duration between two successive read operations has to be 30 ns which corresponds to a clock frequency of 33 MHz. Commercially available clock crystals have fixed frequencies and the nearest available frequency is 32 MHz. This corresponds to a period of 31.25 ns and the duration between the rising edge and the falling edge is 15.625 ns, which is sufficient to read data from the FIFO. Hence the clock oscillator manufactured by CTS Corporation, CTX129-ND was used to generate 32 MHz clock signal. The clock circuit used in the LIM is shown in Figure 5.7.

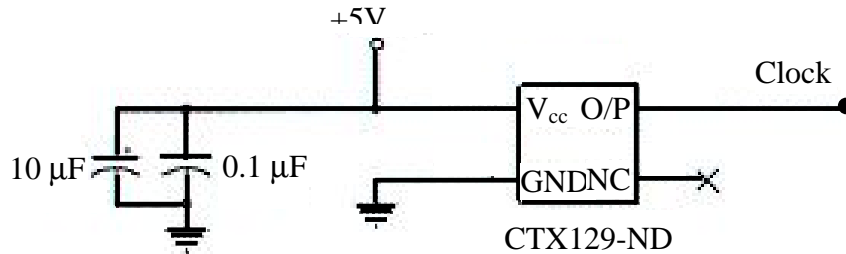


Figure 5.7 Clock Circuit

5.5.2 FIFO

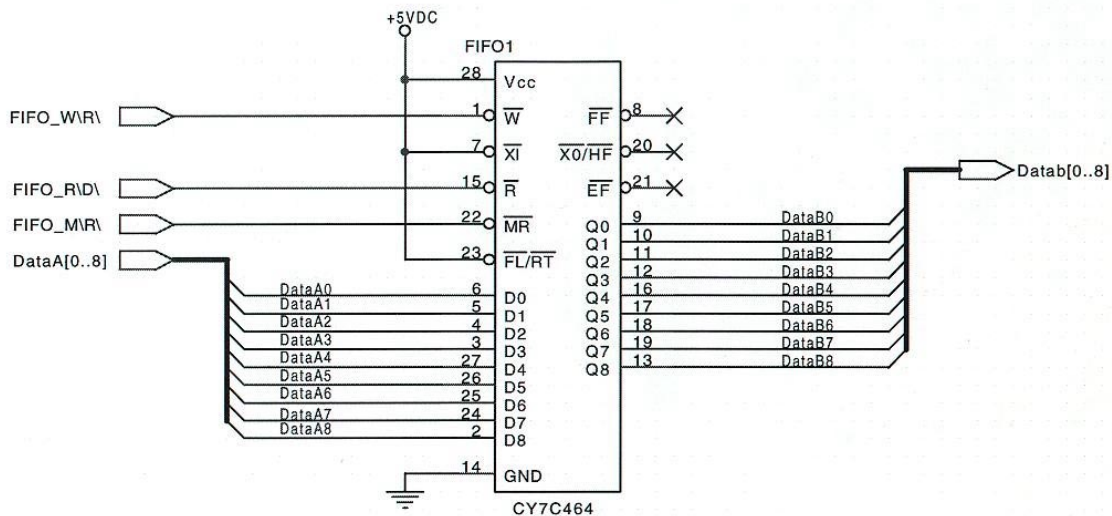


Figure 5.8 FIFO Circuit

The FIFO functions as a high speed buffer between the host computer and the SLM. Data from the SLM is written onto the FIFO when camera scans the current pattern and the FIFO writes the data onto the SLM during the camera's vertical retrace period. The writing of data onto the

FIFO and reading it to load the SLM are controlled by the microcontroller. Each pattern contains information corresponding to 256 x 256 pixels of the SLM. One bit is used to indicate whether a pixel is to be turned “on” or “off”. Thus, each pattern occupies 65,536 (256*256) bits. Since 8 bits = 1 byte, 65,536bits correspond to 8192 bytes. In addition to the 8192 bytes of data, one more byte is used as a “flag” byte to indicate the end of the pattern. Thus, each pattern occupies 8193 bytes of memory. In practice, memory of FIFOs is denoted using powers of 2. For example, 8192 bytes correspond to 2^{13} and is denoted as 8 K. Hence, a FIFO with an 8 K memory is required for the driver.

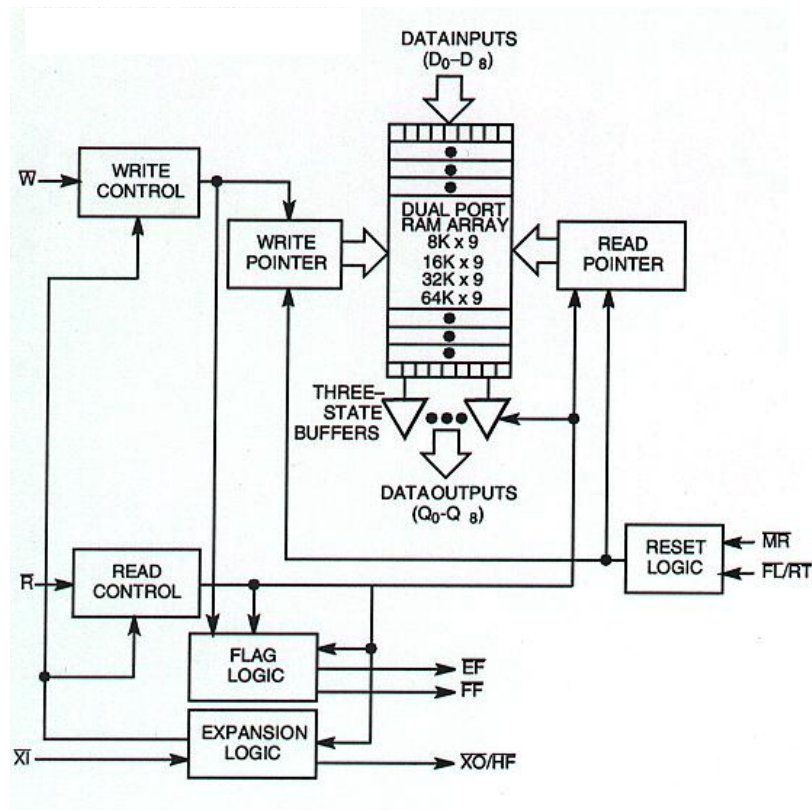


Figure 5.9 Logic Block Diagram Of FIFO

The FIFO used in the driver is CY7C464A, which is manufactured by Cypress Semiconductors. The CY7C464A is a 32 Kwords by 9-bit wide FIFO memory. Each FIFO memory is organized such that the data is read in the same sequential order that it was written. 32 K FIFO was used instead of the necessary 8 K, to enable upgrading the driver in the future. The circuit involving the FIFO is shown in Figure 5.8.

The CY7C464A is an asynchronous device in which the read and write operations can be performed at a maximum rate of 50MHz. The FIFO can be used as a standalone or can be cascaded with additional FIFOs. The logic block diagram of the FIFO is shown in Figure 5.9. The input and output signals of the FIFO is provided in Table 5.2.

Table 5.2 Input And Output Pins Of The FIFO And Their Functions

Input pin	Pin function
W	The write operation occurs when the W signal is LOW.
R	The read operation occurs when the R signal goes LOW.
D ₀ -D ₈	The input data to be written in the FIFO is placed in D ₀ -D ₈ .
MR	The master reset pin has to be enabled to initialize the operation of the FIFO.
FL/RT	The data is retransmitted when the RT signal is low.
XI	The FIFO is indicated that it is operated in the cascaded mode when XI goes low.
Output pin	Pin function
Q ₀ -Q ₈	The output data read from the FIFO is placed in Q ₀ -Q ₈
EF	An empty FIFO is indicated by when EF is low.
FF	A completely full FIFO is indicated when FF goes low.
XO/HF	In the standalone mode, a half filled FIFO that is indicated by a low HF. In the cascaded mode, the XO goes low to activate the next available FIFO.

The timing diagrams for various inputs and outputs are included in the APPENDIX. The master reset (MR) cycle is used to reset the FIFO. This initializes the FIFO and is signified by the Empty flag (EF) being LOW, and both the Half Full (HF) and Full flags (FF) being HIGH. All the outputs (Q₀-Q₈) will be in the high-impedance state when the FIFO is read immediately after the reset cycle. The availability of memory in the FIFO is indicated by HIGH FF signal. When the W signal goes low, the falling edge begins the write cycle and the data appearing at the inputs (D₀ - D₈) when W is LOW will be stored sequentially in the FIFO. The EF signal goes high after the first LOW-to-HIGH transition of the write signal of an empty FIFO. The HF signal goes low after the falling edge of the write signal that causes the FIFO to be half full. The FF signal goes low after the falling edge of the write signal that filled the FIFO completely. The FIFO ignores the data placed on the input after it is FF goes low. The falling edge of the R

signal begins a read cycle provided the EF signal is not LOW. The FF signal goes high following the first read cycle from a full FIFO and the HF signal goes HIGH after the FIFO becomes half full following the read operation. When only one word is in the FIFO, the falling edge of R signal initiates a HIGH-to-LOW transition of EF. When the FIFO is empty, the outputs are in a high-impedance state. A read signal to an empty FIFO is ignored.

5.5.3 Video Signal Decoder

The function of the video signal decoder is to accept the composite synchronization signal from the video camera and generate a vertical sync signal. This vertical sync signal is used to identify the start of the vertical retrace period of the camera. The decoder circuit is shown in Figure 5.10. National Semiconductor's LM1881 is used as the video sync separator. The LM1881 extracts timing information including composite and vertical sync, burst/back porch timing, and odd/even field information from standard negative going sync video signals from a camera. The input to the LM1881 and its output corresponding to one period of the composite video signal is shown in Figure 5.11. The value of resistors and capacitors used in the circuit was suggested by National Semiconductor.

The composite sync output is a reproduction of the signal waveform whose output level is below the composite video black level, with the video completely removed [21]. This signal is generated using a “compare and clamping” circuit present inside the LM1881. The input capacitor of 0.1 μF is used to drain the charge and discharge current of the “compare and clamping” circuit. The resistor (620 Ω) and capacitor (510 pF) pair functions as a low pass filter. This low pass filter of 500kHz bandwidth passes the sync pulse portion of the video signal while filtering out unwanted noise.

The vertical sync output is obtained by integrating the composite sync signal internally. A LOW signal on the vertical sync output indicates the vertical retrace period of the camera. While the integrator circuit and the capacitor of the integrator are present inside the LM1881, the resistor connected to the RSET pin determines the capacitor charge current. The value of 680 K Ω is the minimum resistance required for the video standards in the United States [21].

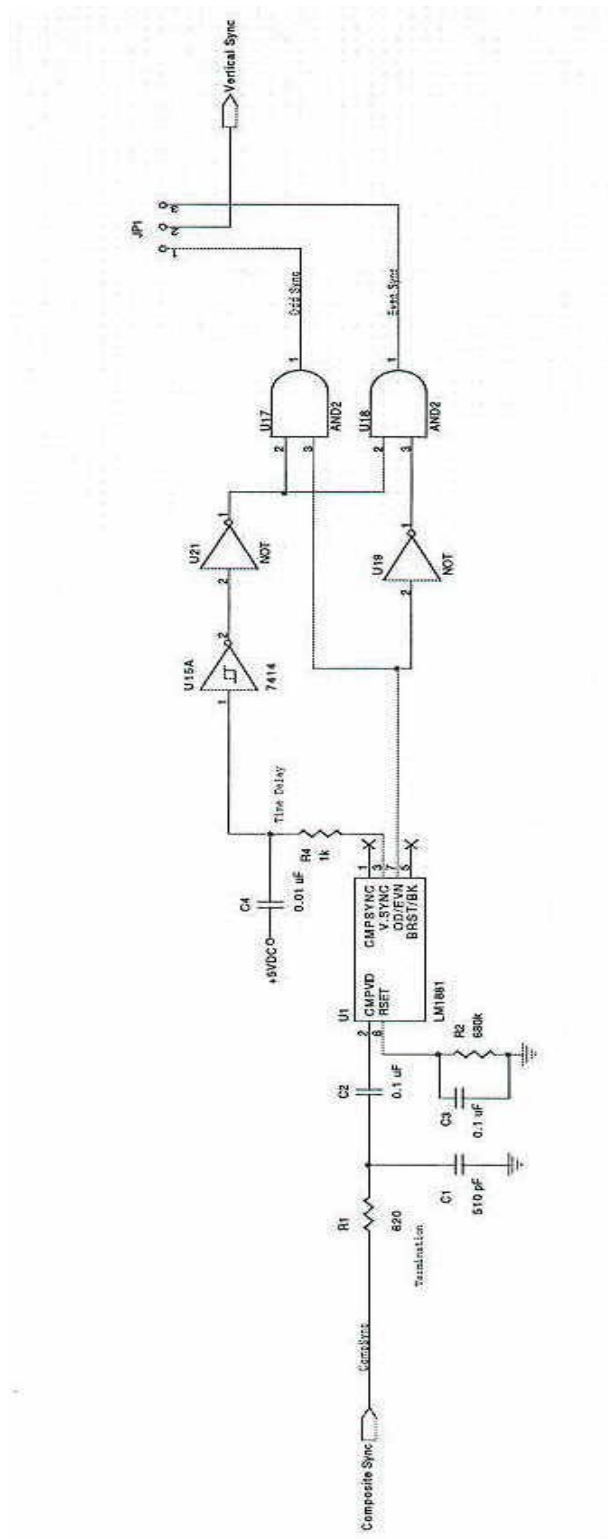


Figure 5.10 Video Signal Decoder

A method known as interlaced scanning is used by the video camera to scan images. In this method, the image is divided in horizontal lines. All the odd numbered lines are scanned first and then the even numbered lines are scanned resulting in a composite video signal with an odd field and an even field. While the odd field has a half horizontal scan line at the end, the even field has a full horizontal scan line at its end. Integrating the composite sync output and toggling the result on successive vertical retrace periods generates the odd/even output. An internal capacitor is charged during the duration between the vertical sync pulses and discharges when the pulse is present. The burst/backporch output provides the color information of the composite video input.

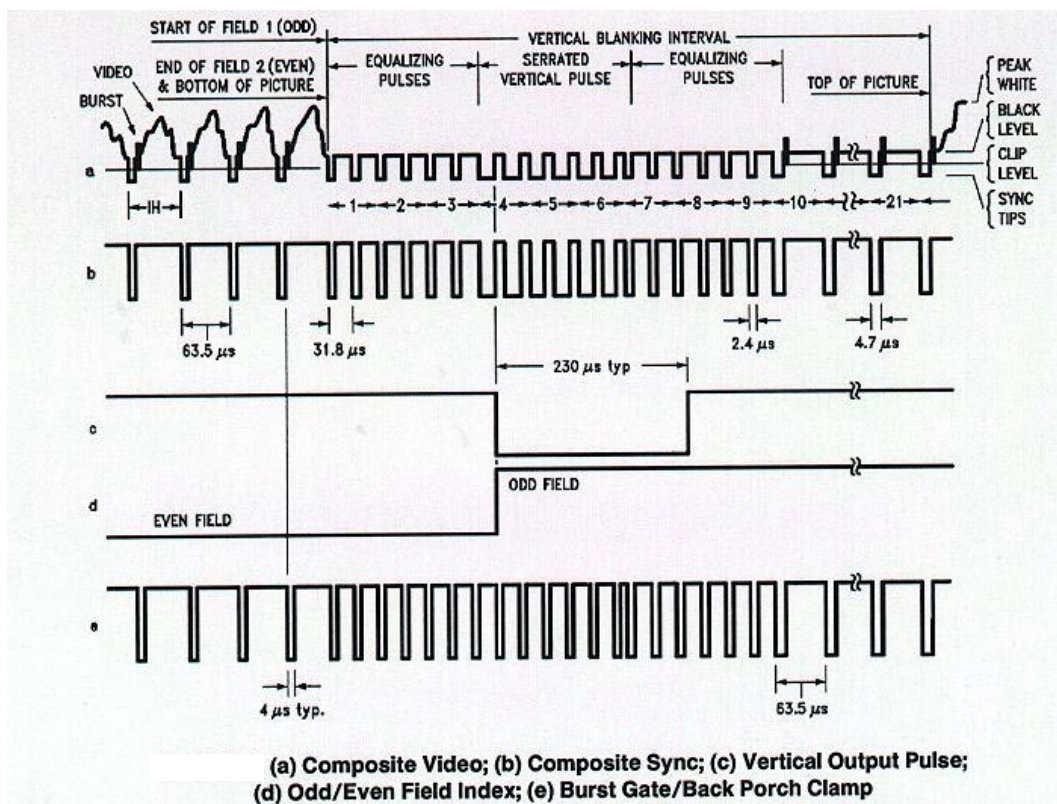


Figure 5.11 Input And Outputs Of LM1881

The vertical sync from the LM1881 as it goes LOW twice during the scanning of each image. However, we need to load the pattern from the FIFO onto the SLM only once. Hence, by combining the vertical sync output and the odd/even output using the circuit shown in Figure 5.11, we obtain a vertical sync signal, which goes LOW once for each pattern. A jumper mechanism was used to provide the flexibility of choosing either the odd sync or the even sync.

5.5.4 Design of the sequencer

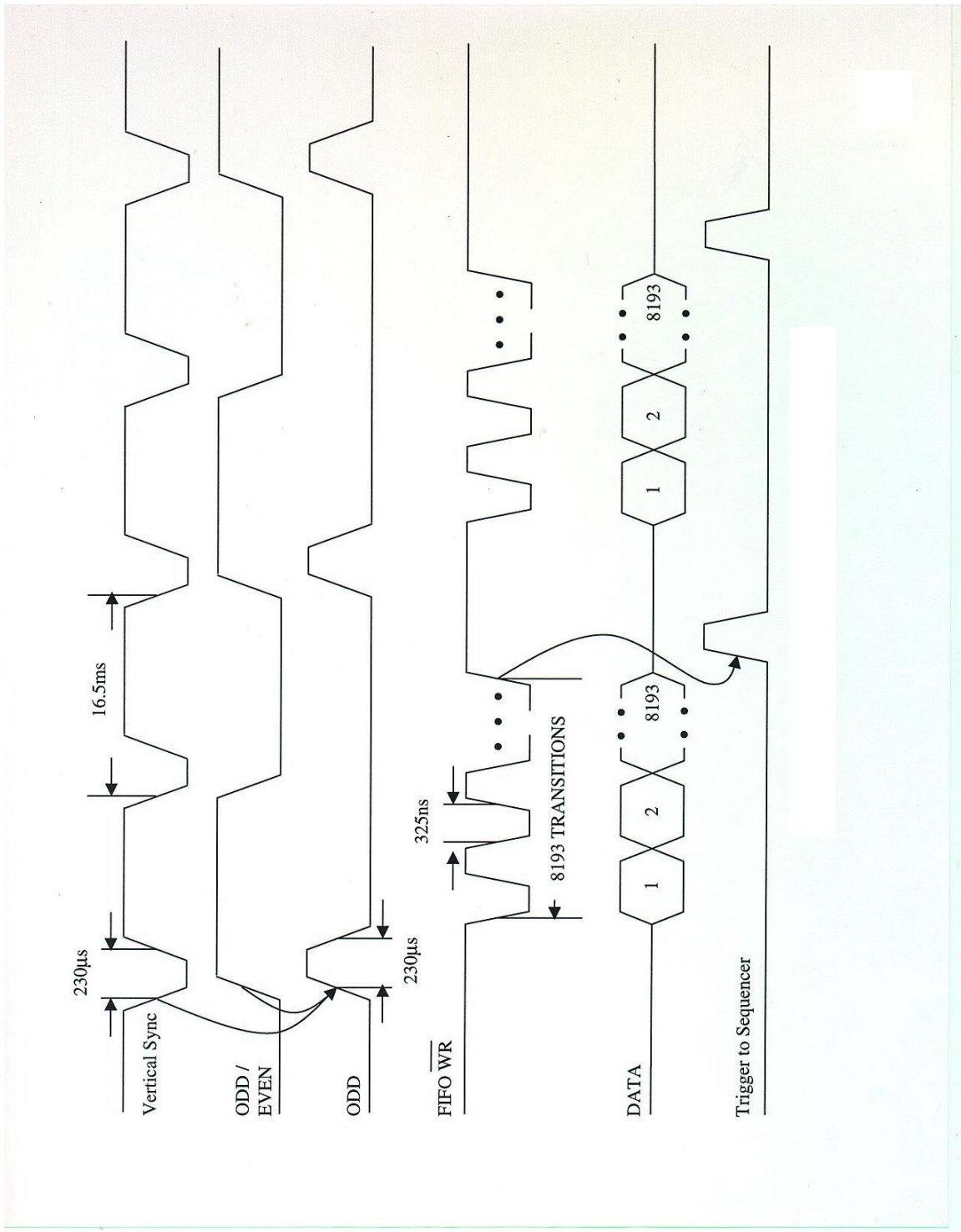


Figure 5.12 Loading Of FIFO By Microcontroller

As mentioned in Section 5.4, while the current pattern is being scanned by the camera, the next pattern is transferred from the host computer to the high speed FIFO and during the vertical retrace period of the camera, the pattern is written onto the SLM. The host computer signals the microcontroller to begin the process of first writing the data into the FIFO and then onto the SLM. The previous section explained the generation of the vertical sync signal by the video synchronization decoder. The duration in which the current pattern is scanned by the camera is defined by the time interval between two successive logic high vertical sync signals. During this period (according to specifications it is 16.5 ms), the microcontroller has to write the data corresponding to the next pattern from its memory to the FIFO. The timing diagram for this write operation is given in Figure 5.12.

The specifications of the FIFO indicate that a write enable signal $FIFOWR$ of 325 ns is necessary to write data onto a single address. There are 8193 data bytes (8192 bytes for the pattern and one byte to function as the end flag). Thus, the write operation takes about 2.7 ms, which is sufficiently less than the period of the vertical sync. The end of the write operation signals to the sequencer that the data to be written onto the SLM is ready in the FIFO. The logic high state of the vertical sync signifies the vertical retrace of the camera. During this interval the data corresponding to the next pattern is read from the FIFO and written onto the SLM. The specifications of the FIFO indicate that the read signal has a setup time of about 15ns and it has to remain enabled for another 15ns for data to be read. Hence, the $PDATA$ signal that enables the SLM to receive data has to have a logic high pulse period of 30ns and a total period of 60ns. The total time required to write 8193 bytes of data onto the SLM is $(8193 * 60 \text{ ns}) 491\mu\text{s}$. However, the time period of the vertical sync pulse is 230 μs . This results in the loss of some amount of information when the pattern is scanned by the camera. The additional time required for writing the data is 261micros while the total scan duration is 16.5ms. This indicates that the data lost corresponds to about 1.5% of the entire information. This distortion was decided as an acceptable value. The timing diagrams corresponding to the loading of the SLM are shown in Figures 5.13 and 5.14.

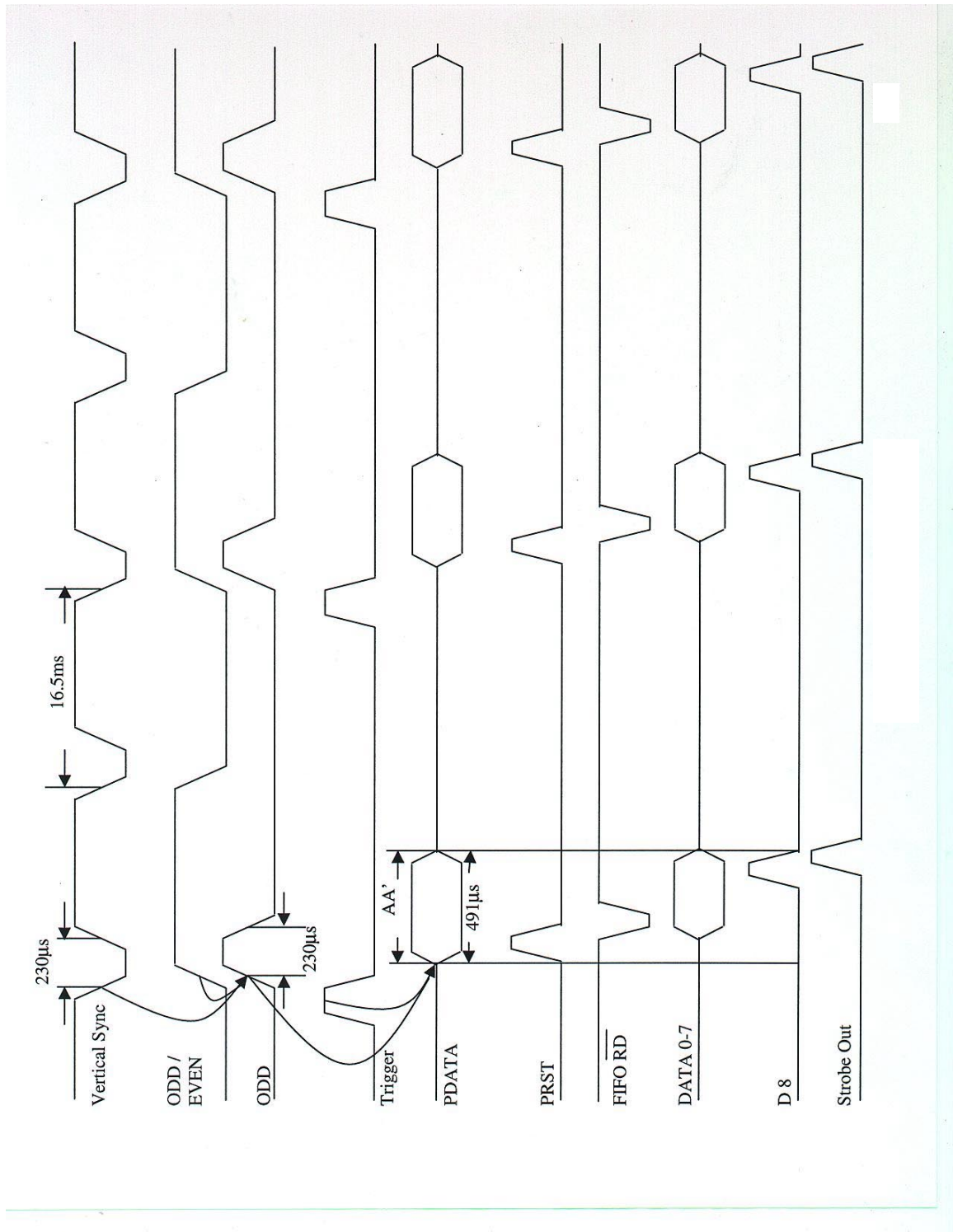


Figure 5.13 Loading Of SLM By Microcontroller

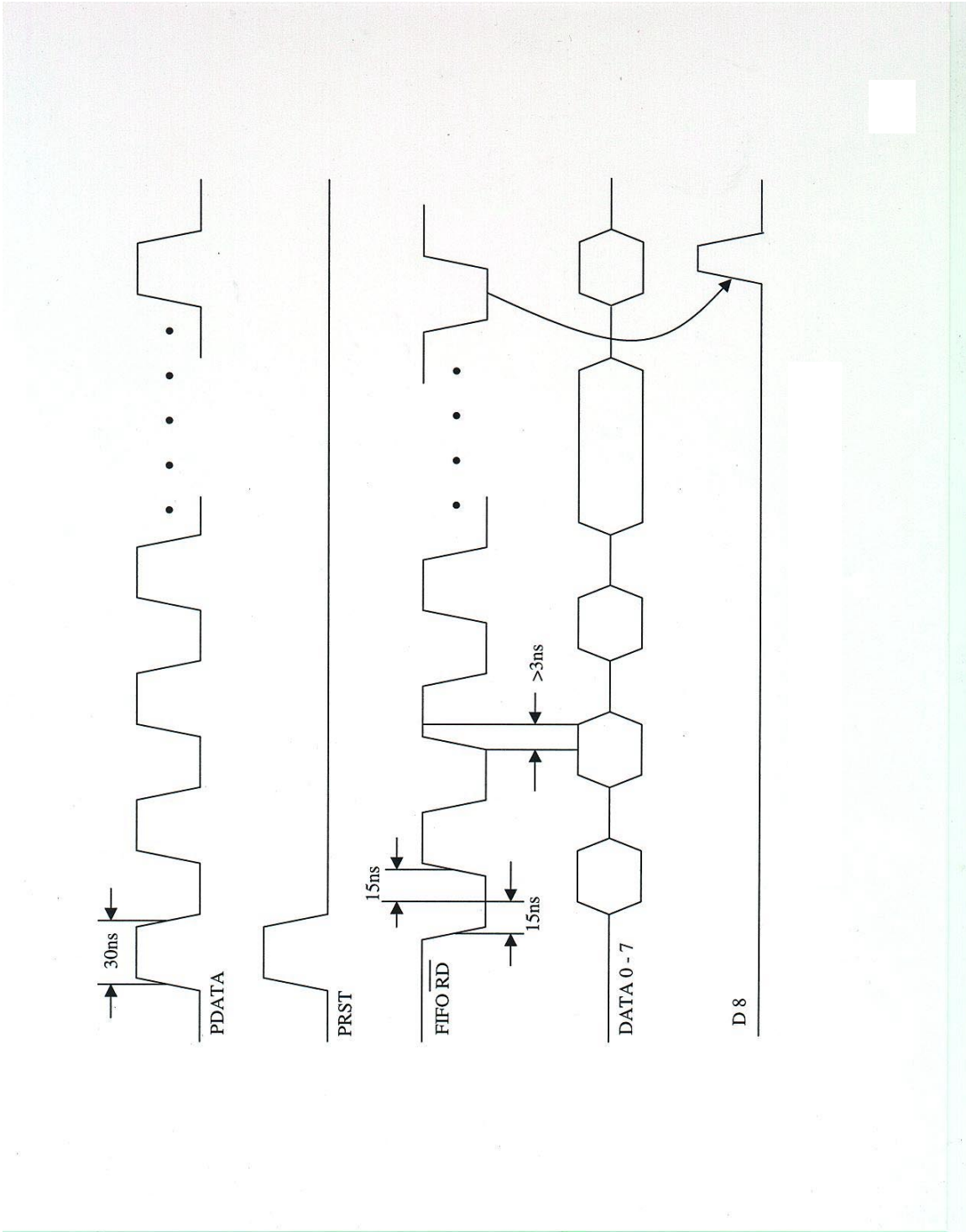


Figure 5.14 Portion Marked As AA' In Figure 5.14

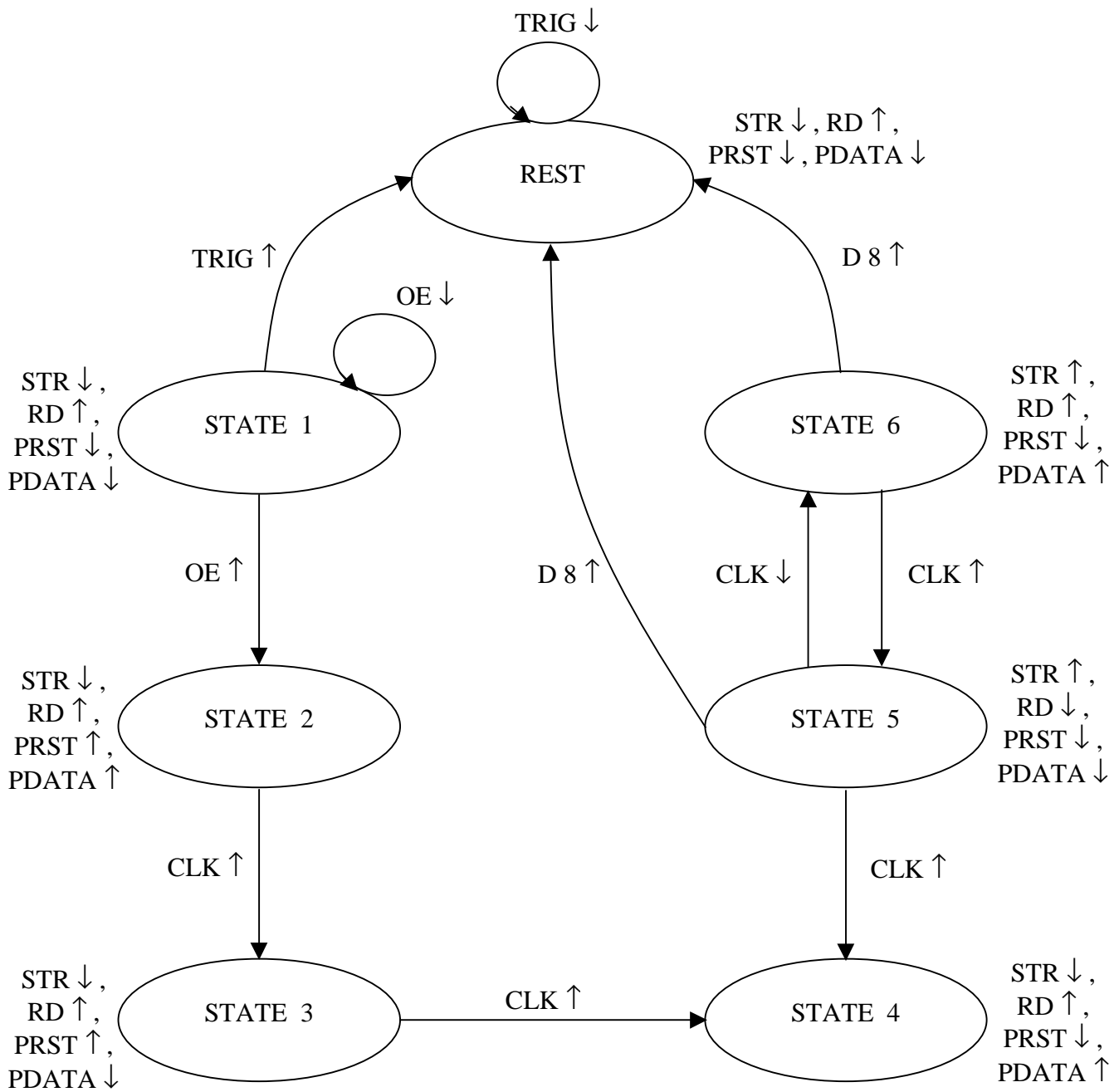


Figure 5.15 State Diagram Of Sequencer

The function of the sequencer is to ensure that the various reading and writing cycles take place in the right order. The inputs to the sequencer are

- Clock (CLK) is used for the sequential operation of the sequencer.
- Data Bit (D8) from FIFO serves as the flag to indicate the last byte of the pattern.

- Trigger (TRIG) from the microcontroller signals the start of the loading of the SLM.
- Synchronization pulse (SYNC) from the Video Synchronization Decoder signifies that the camera is in its vertical retrace period.

The outputs from the sequencer are

- Strobe Out (STRB) to the host computer indicates to the computer that the pattern has been loaded into the SLM.
- Read signal (RD) enables to read the next available data byte from the FIFO.
- Reset signal (PRST) to the SLM initializes the internal counter to point to the first pixel.
- Data signal (PDATA) the falling edge of which latches any input to the SLM.

The state diagram of the sequencer is shown in Figure 5.15. The sequencer starts with the rest state. This indicates the initial or the dormant state. The state machine remains in this state till the trigger signal from the microcontroller is enabled. During this state all the outputs from the sequencer are in the logic low state. The sequencer moves to State 1 once it receives the trigger signal from the microcontroller. At this state the data has been updated in the FIFO and is ready for being loaded into the SLM during the next vertical retrace of the camera. The outputs are in the logic low state waiting for the vertical sync input to be enabled. When the vertical sync signal is enabled, the PRST signal is asserted high. However, this is latched by the SLM only when the PDATA signal goes low. At the next rising edge of the CLK input (State 4), the PDATA output goes low and the SLM is reset by the PRST. The purpose of the internal counter is to keep track of the pixel into which the next data has to be loaded. When this counter is reset, it points to the first available pixel. The PDATA output is also enabled during this state. State 4 was introduced to account for the specification that data can be latched onto SLM only after the second rising edge of the clock following the assertion of the reset input. The data is loaded into the SLM during states 5 and 6. During state 5 the RD signal goes low and data is read from the FIFO. This data is clocked into the SLM when the PDATA goes high (State 6). The sequencer oscillates between states 5 and 6 till all the data bytes from the FIFO has been loaded into the SLM. The exit condition is indicated by the assertion of D8 and the sequencer returns to its rest condition. Design of the PLD circuit and the programming of the PLD were done by DCS Corporation.

5.5.5 Hardware Interface

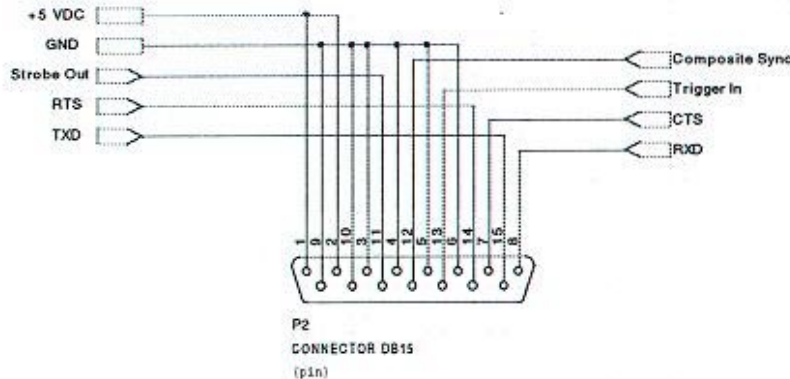


Figure 5.16 D-Connector Of The Driver

The SLM driver electronics is located on a single circuit board that is mounted on the side wall of the LIM with four threaded standoffs. There are threaded holes on the walls of the LIM to receive these standoffs. The driver is connected to the SLM, the host computer and the power supply through three connectors.

1. A 15pin 'D' male connector is provided in the driver to handle power, ground, the RS-232 connection to the host, and other control/output signals from/to the host (Figure 5.16).
2. A 80-pin connector was used to interface the driver with the SLM (Figure 5.17).
3. A BNC jack (female) will accept a coaxial connector carrying the RS-170 video signal.

A 3m cable is used to carry the control signals and power between the LIM and the host. The host computer is connected through its parallel I/O card that supplies the 5 volts DC power required by the driver. The RS-170 video signal and a "Trigger In" signal constitute the input signals to the driver while the "Strobe Out" signal and "Busy" signal are the output signals. The video signal is used as the composite sync input to synchronize various operations of the driver. This includes loading of pattern from the host computer to the driver and from the driver to the SLM during the vertical retrace period of the camera. The cable carrying the sync signal is terminated by a BNC male connector, which connects to its female counterpart in the driver which is terminated by a 50 ohm resistance. The remaining three signals, the "Trigger In", the "Strobe Out" and the "Busy" are standard 5 volt TTL signals which are either active HIGH or

active LOW. The leading edge of "Trigger In" signals the driver to load the pattern into the SLM for display during the following video retrace interval. An active high of the "Strobe Out" signal indicates to the host computer that a new pattern has been loaded into the SLM. The image processor present in the host computer uses this signal to identify the beginning of new pattern input from the camera. The "Busy" signal is set to active high state when the microcontroller in the driver is in the process of either loading the FIFO or the SLM with the pattern.

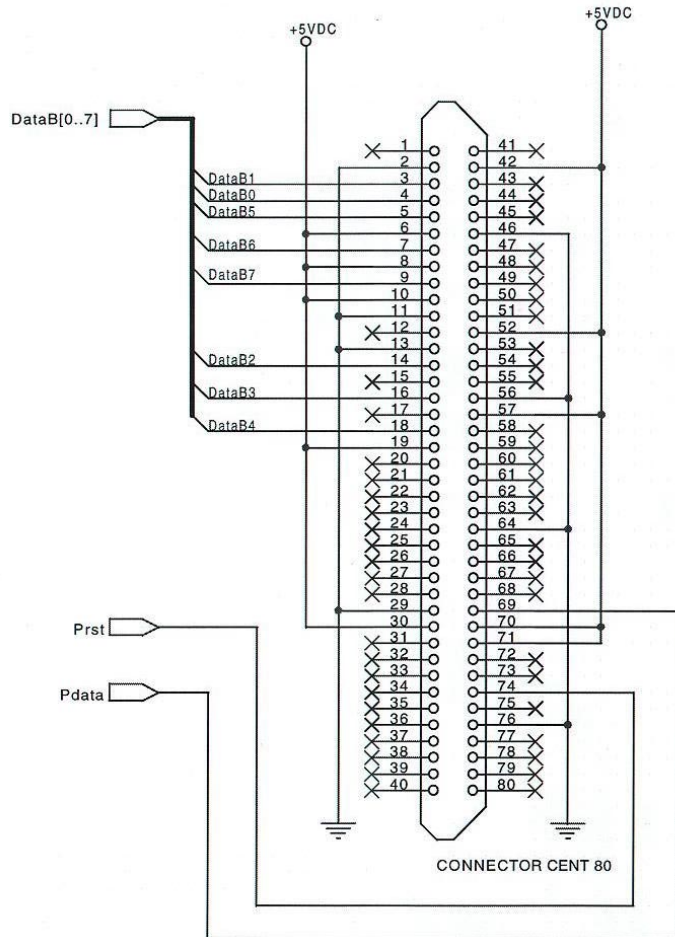


Figure 5.17 80-Pin Connector To The SLM

5.5.6 Software Interface

The microcontroller receives the control signals from the host computer through the RS-232 link at 19.2K Baud rate. The microcontroller is responsible for loading the pattern on to the FIFO

and then to the SLM. There is provision to store upto 10 permanent patterns in the Read Only Memory (ROM) of the microcontroller. It is also possible to load upto 10 patterns into the Random Access Memory (RAM) of the microcontroller from the host computer. The patterns are numbered from 0 to 19, with 0-9 representing the patterns in the RAM and the remaining numbers indicate the patterns in the ROM. The LOAD PATTERN represented by LDPxxaabb..zz instructs the microcontroller to store the pattern of index "xx" in the corresponding RAM location. The "aabb..zz" represent the actual pattern information in the WINDOWS bitmap file format. The sequence in which the patterns are loaded into the SLM is uploaded to the microcontroller during runtime. A maximum of 5 sequences with index number 0 to 4 is stored in the RAM. The sequences can be of any length with a maximum of 256 patterns and each pattern is represented by a two-digit hexadecimal with the 0xFF indicating that the preceding pattern index is the last one in the sequence. For the LOAD PATTERN SEQUENCE the command from the host computer is of the form LPSxaabb..zzFF. "x" represents the one-digit hex number between 0 and 4 indicating the RAM pattern sequence index into which the pattern is to be loaded. "aa", "bb", through "zz" represent upto 256 two-character hex numbers, each containing the pattern index (0 to 0x27) of each pattern in the sequence.

The SLM can be set to display the patterns in two different modes. In the SET DISPLAY MODE IMMEDIATE (SDMI), the pattern is transferred to the SLM during the video vertical retrace and the pattern display cycle starts without waiting for the "Trigger In" signal from the host computer. On the contrary, in the SET DISPLAY MODE TRIGGERED (SDMT), the pattern display is delayed until a trigger signal is received on the Trigger In line. Similar to the display modes, there are two modes in which the patterns are loaded according to the sequence. The SET SEQUENCE MODE MANUAL (SSMM) displays the next pattern in the sequence when it receives the DISPLAY NEXT PATTERN (DNP) command from the host computer. In the SET SEQUENCE MODE AUTOMATIC (SSMA), the next pattern in the sequence is displayed until the sequence is exhausted. The spacing between two patterns is set using the LOAD SEQUENCE SPACING (LSSaa) command, where $0 \leq aa \leq 255$ indicates the number of display cycles that need to be skipped before the display of each pattern. Further, provision has been provided for the host computer to command the SLM to display a programmed sequence

(DISPLAY REQUESTED SEQUENCE, DRS) or display a particular pattern (DISPLAY REQUESTED PATTERN DRPxx, "xx" pattern index).

The host computer ensures error free operation by requesting for feedback from the microcontroller (STATUS REQUEST SRQ). In response to the above request, the microcontroller sends the STATUS REPORT SENT (STRabc) output. "a" represents the current display mode (Immediate or Triggered), "b" is the current sequence mode (Manual or Automatic) and "c" indicates if the LIM is busy or ready to receive the next command. In addition to the status report, the microcontroller also sends the CONFIRM COMMAND (CFM) and the ERROR REPORT back to the host computer. The CONFIRM COMMAND is the acknowledgement sent for all the commands from the host except for the status report request command. The error report (ERRxx) returns a hex digit "xx" which can be used to indicate any of the following conditions:

- Out of range pattern index in the LDP or DRP command.
- Out of range sequence index in the LDS or SPS command.
- DRS command was received while in manual mode.
- DNP command was received while in automatic mode.
- Unrecognizable command.
- Any hardware problem.

The psuedocode for the software interface between the host computer and the micro-controller in the driver circuit for the SLM is included in the APPENDIX.