Design of a Multi-Module Multi-Phase Battery Charger for the NASA EOS Space Platform Testbed

by

James P. Noon

Thesis submitted to the faculty of the

Virginia Polytechnic Institute and State University

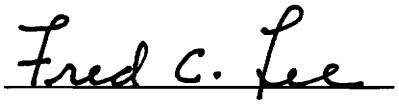
in partial fulfillment of the requirements for the degree of

Master of Science

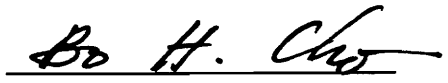
in

Electrical Engineering

APPROVED:



F. C. Lee, Co-Chairman



B. H. Cho, Co-Chairman

D. Y. Chen

July 27, 1992

Blacksburg, Virginia

Design of a Multi-Module Multi-Phase Battery Charger for the NASA EOS Space Platform Testbed

by

James P. Noon

Committee Co-Chairmen: Dr. F. C. Lee and Dr. B. H. Cho

Electrical Engineering

(ABSTRACT)

The design, analysis, and testing of a multi-module, multi-phase (MMMP) battery charger for the NASA Earth Observing System (EOS) is presented. The MMMP converter is comprised of four independent buck converters switched 90° out of phase. The MMMP charger is compared to a single module battery charger, and shown to provide significant performance improvements. The power stage is designed for maximum efficiency and minimum weight. The control loops (Charge Regulation and Bus Voltage Regulation) designs are presented and the small-signal models are verified with experimental results. The charger testing is facilitated by the use of the Space Platform Power System Hardware Testbed. The testbed utilizes battery and solar array simulators which allow for realistic battery charger testing.

To my wife,

Donna

Acknowledgements

I would like to thank my advisors Dr. Fred C. Lee and Dr. Bo H. Cho for their support and contributions to my graduate studies. I would also like to thank Dr. Dan Y. Chen for his suggestions and comments on my research. I am especially grateful for the opportunity to study and conduct research at Virginia Power Electronics Center, one of the foremost centers for Power Electronics research.

I would also like to thank NASA Goddard Space Flight Center for their support, and all the members of the NASA Space Power Testbed project for their comments, suggestions and ideas. The members of the Testbed project are: Steve Butler, Scott Deuty, Tom Sizemore, Ashok Patel, Zvi Gur, Xuesi Mang and Dan Sable. A special note of thanks to Dan for his help with my research. It was Dan Sable who first introduced me to the challenges and rewards of the field of Power Electronics. Tom Sizemore and Pawel Gradzki were also especially helpful with ideas and suggestions.

I would also like to thank the staff at VPEC for their help during my graduate work.

I especially thank my parents, John and Barbara Noon for their love and support; they have always believed in me even when it was difficult to do so. They have instilled in me a love for education and a belief that if you work hard enough, anything is possible, for this I am grateful.

Finally, I would like to thank my wife, Donna. She has always encouraged me in all my endeavors, and it is her love and support that have allowed this to be possible.

Table of Contents

List of Figures

List of Tables

1. Introduction

As part of its Mission to Planet Earth, NASA has embarked on a program of designing and building a series of satellites known as the Earth Observing System (EOS). In order to facilitate the design and testing of these satellites, NASA has contracted with the Virginia Power Electronics Center (VPEC) at Virginia Polytechnic Institute and State University to design and build a Space Platform Testbed.

The testbed power system consists of a battery and solar array simulator as well as an actual prototype charger, discharger and switched shunt unit. This thesis presents the research and design of the battery charger subsystem.

The battery charger is part of the charger/discharger/shunt unit power system. The complete system consists of two charger/discharger units and one shunt unit. Each unit is capable of processing 1.8 KW for a system power level of 3.6 KW. During periods of illumination, the solar array provides power to the spacecraft bus. As power is increased beyond what is required by the load, the battery charger is activated and begins to charge the batteries.

The charger first regulates the bus voltage by directing current to the batteries (Bus Regulation Mode). As solar array power increases, charge current is increased until the commanded level of charge current is reached (Charge Regulation Mode). At this point the switched shunt unit regulates the bus voltage. Since the charger operates in both a bus regulation and a charge regulation mode, two control loops are required to ensure proper operation.

During the first stage of this project a single module charger was developed [1]. As part of the ongoing research project, work continued on the development of the bat-

tery charger subsystem. An alternative approach to the single module converter was investigated. The alternative approach was a multi-module multi-phase (MMMP) battery charger. The MMMP charger consists of four modules, each phase shifted 90° apart. This work was an attempt to quantify any advantages the MMMP charger had over the single module (SM). In addition, this thesis documents the design and testing of the MMMP battery charger.

1.1 Design Specification

The battery charger design specifications are as follows:

V_{Bat} = 64 - 84 V

V_{Bus} = 120 V $\pm$ 2%

Output $Power_{Max}$ = 1472 W

I_{Ch} = 0.85 - 23 A (16 Commandable Rates)

Bus Ripple = 200 mV_{pp}

Efficiency = > 95%

Switching Frequency = 45 KHz

1.2 Thesis Outline

The trade-off study between the MMMP and SM battery charger is presented in Chapter 2. A loss analysis is performed on the power stages and significant loss mech-

anisms are identified and analyzed. A weight comparison is then performed, including allowances for heat sink weight in order to compensate for efficiency. The input and output filter requirement of the two converters are also compared.

Chapter 3 details the design of the MMMP power stage, and the selection of switching devices is presented. The input and output filter design is documented in detail as is the power stage performance.

The control system design is presented in Chapter 4. Both the charge and bus regulation mode designs are introduced here. In both modes the relevant transfer functions are presented. Attention has been placed on verifying theoretical transfer functions with actual measurements. The feedback loops are designed, and system performance is verified.

Chapter 5 presents conclusions from this work.

2. Trade Off Study

2.1 Introduction

The space power system application is a demanding one. A high value is attributed to efficiency, weight, and reliability. In a space environment the efficiency of a subsystem is of importance from both a thermal and energy transfer point of view. The losses in an electrical component cause heat to be produced. The reliability of an electrical component is directly related to its operating temperature. Any heat generated in a space environment must be dissipated through radiation and/or conduction. Since radiation is a rather ineffective method of heat transfer, conduction of heat away from semiconductor components is critical to system reliability. Losses then not only degrade efficiency but increase the overall weight of a system due to increased heat sink requirements. In addition, losses require excess energy capacity in the battery and solar arrays to provide system power requirements. This excess energy capacity can add large weight penalties to the spacecraft and significantly impact spacecraft cost.

The weight of a system is an important factor in spacecraft design. This is especially true of the power system. A satellite is designed and placed in orbit to perform a function or service. The power system is only there to enable the other systems to perform their functions. Usually a satellite design has some maximum weight constraint. If this weight is exceeded there is an enormous cost penalty. This is due to the fact that a launch vehicle has a maximum payload capability. In addition the cost of launching a satellite is directly related to its weight. As satellites are getting larger and more powerful, it is essential that as much of the weight as possible is due to the equip-

ment and systems that are performing the spacecraft's mission. The weight of a system is made up of its components as well as the required heat sinking to ensure reliable component temperatures.

The philosophy of minimum weight allocation for the power system somewhat conflicts with the demand for more power to supply larger spacecraft. The goal then is to find a highly efficient and low weight power system that is capable of processing high power levels to meet the demand of modern spacecraft.

This trade-off study was done to compare both the efficiency and weight of the SM and the MMMP battery chargers. First the power stage losses associated with each design will be compared and then the weight for each system will be calculated.

The SM battery charger in EOS is shown in Fig. 2.1. The SM charger is a basic buck converter with a single energy storage inductor. There are four MOSFETs in parallel to handle the current requirement and two diodes in parallel for the same reason. Input and secondary output filters are required for current ripple attenuation. The design of an SM battery charger was presented in [1]. Many of the design details needed in the comparison of the two chargers are from [1], but in general the loss analysis is generic to any single module design. The results of the comparison are not particular to any one design.

The MMMP converter is shown in Fig. 2.2. The MMMP battery charger is also a buck topology converter. It consists of four separate and independent buck converters (modules) operating in parallel. Each module is operated 90° out of phase. This multiphasing removes the need for a second stage output filter due to the current ripple cancelation. Input and output filter components are common to all the modules. The four modules each contain an energy storage inductor, a power MOSFET, and a power diode.

From strictly the power stage point of view, the MMMP charger has more components. It has in fact two more inductors and two more diodes. The MMMP charger therefore has more components and requires additional control circuitry to produce the multi-phasing. The question becomes, can the MMMP battery charger produce substantial performance improvements to offset any additional component weight and system complexity?

To perform the trade-off analysis, losses within the power stage are compared, and the weight of the power stage and filter components are calculated. To facilitate the loss analysis, a spreadsheet program was written to calculate all the significant losses. This program incorporates the equations developed in the following sections.

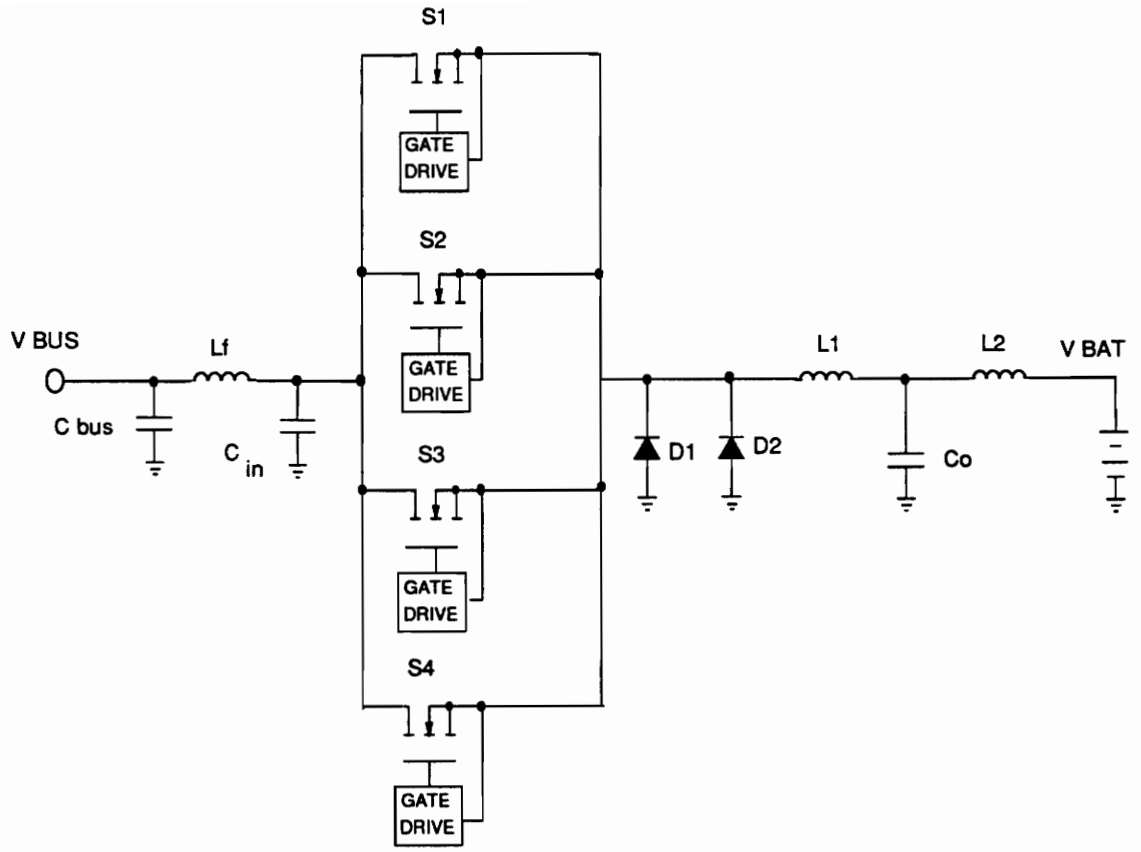


Figure 2.1 Single Module Battery Charger

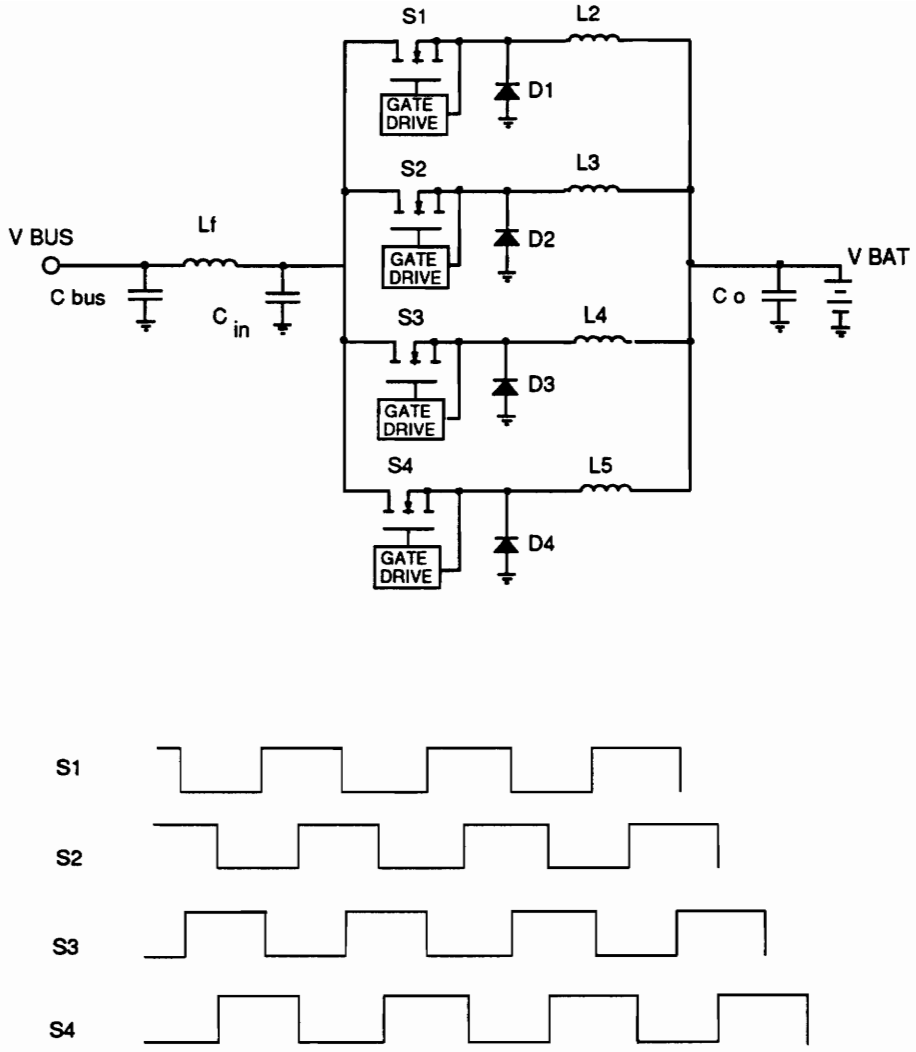


Figure 2.2 Multi-Module Multi-Phase Battery Charger

2.2 Loss Analysis

There are two main components that contribute to power stage loss: semiconductor and magnetic component losses.

2.2.1 Semiconductor Loss

Semiconductor losses are divided between the MOSFET and the diode. Within each device, losses can be further divided between switching and conduction losses. Conduction loss in the MOSFET is a function of the RMS current flowing in the FET and the drain-to-source on resistance. It can be calculated by the following formula:

$$P_{cond} = I_{T_{RMS}}^2 \cdot R_{DS_{ON}}, \tag{2.1}$$

Where for the buck converter operating in CCM I_{RMS}, is given by:

$$I_{T_{RMS}} = \left(\left\{ I_{pk}^2 - (I_{pk} \cdot \Delta i) + \frac{\Delta i^2}{3} \right\} D \right)^{\frac{1}{2}}, \tag{2.2}$$

where

$$I_{pk} = \frac{I_{Charge}}{4} + \frac{1}{2} \cdot \Delta i, \tag{2.3}$$

and

$$\Delta i = \frac{V_{Bus} - V_{Bat}}{L} \cdot t_{on}. \tag{2.4}$$

Switching loss within the MOSFET is made up of several quantities. Turn-on and turn-off loss can closely be approximated by assuming a linear transition from peak value to zero. The turn-on loss is given by:

$$P_{T_{turn-on}} = \frac{V_{DS} \cdot I_{pk} \cdot t_{S1} \cdot F_s}{6}. \tag{2.5}$$

Where t_{S1} is the time required for the switch to transition from its OFF state to the ON state and F_s is the switching frequency. I_{val} is the minimum value of the inductor current and is given by:

$$I_{val} = \frac{I_{Charge}}{4} - \frac{1}{2} \cdot \Delta i. \tag{2.6}$$

The turn-off loss is calculated in the same fashion, except that peak value of switch current is used:

$$P_{T_{turn-off}} = \frac{V_{DS} \cdot I_{pk} \cdot t_{S2} F_s}{6}. \tag{2.7}$$

t_{S2} is the time required for the switch to turn-off. In most instances t_{S1} and t_{S2} are equal.

Turn-on and turn-off present the major switching losses. Secondary losses associated with switching are capacitive discharge loss due to the drain-to-source capaci-

tance, and gate drive loss due to the gate-to-source capacitance. Both of these capacitances are nonlinear but can be approximated by linear equivalent capacitors. The drain-to-source capacitance discharge loss is given by:

$$P_{C_{DS}} = \frac{2}{3} \cdot C_{DS} \cdot V_{DS}^2 \cdot F_s. \tag{2.8}$$

The gate drive loss is given by:

$$P_{gate} = V_{GS}^2 \cdot C_{GS} \cdot F_s. \tag{2.9}$$

In both designs, V_{GS} was equal to 10 V.

The diodes experience similar losses as the MOSFETs. Conduction loss in the diode is a function of the RMS current through the diode and the RMS voltage across it:

$$P_{D_{Cond}} = V_{D_{RMS}} \cdot I_{D_{RMS}}. \tag{2.10}$$

Diodes also experience switching loss during turn-on and turn-off as well as loss during reverse recovery. Turn-on loss is a function of switching speed, peak inductor current, and frequency:

$$P_{D_{Turn-on}} = \frac{V_{D_{pk}} \cdot I_{D_{pk}} \cdot t_{D_{on}} \cdot F_s}{6}. \tag{2.11}$$

$t_{D\,pk}$ is the time required for the diode to turn-on, and $V_{D\,pk}$ is the peak diode voltage. The peak diode voltage is equal to the maximum battery voltage, 84 V. The turn-off loss is a function of the minimum inductor current, the diode ON voltage, the time required to turn-off, $t_{D\,off}$, and of course, the switching frequency:

$$P_{D_{off}} = \frac{V_{D_{on}} \cdot I_{val} \cdot t_{D_{off}} \cdot F_s}{6}. \tag{2.12}$$

The last significant switching loss associated with the diode is reverse recovery loss. The reverse recovery loss is also a function of frequency, and the time required to deplete excess charge from the diode, t_{rr}:

$$P_{D_{rr}} = V_{D_{pk}} \cdot I_{D_{pk}} \cdot F_s \cdot t_{rr}. \tag{2.13}$$

2.2.2 Magnetic Losses

The magnetic losses in a nonisolated buck converter are solely within the energy storage inductors. The nature of the inductors simplifies the magnetic loss analysis as well as the design. For example, copper loss can be calculated by looking at the RMS current flow and wire resistance since proximity effect is negligible. The same is true for core loss.

The copper loss is conduction loss due to the resistance of the conductor.

$$P_{Cu} = I_{RMS}^2 \cdot R_l, \tag{2.14}$$

where the RMS current in the inductor (assuming CCM operation) is given by:

$$I_{L_{RMS}} = I_{Charge_{avg}} \cdot \left(1 + \frac{1}{12}\left(\frac{1-D}{\tau_L}\right)^2\right)^{\frac{1}{2}}, \tag{2.15}$$

and τ_L is L/RT_s. In this case R is the dc value that would give the desired charge current at the given battery voltage; it is not the actual resistance of the battery.

The core loss is a function of ac flux and frequency and is dependant on core material, permeability, and geometry. For a specific core, the manufacturer provides equations or loss curves. For loss analysis this information will be used to calculate actual losses. The equations are of the form:

$$P_{core} \propto F_s^n \cdot B^k, \tag{2.16}$$

where n and k are variables dependant on the core material and permeability, and B is the ac flux density.

2.3 DCM Boundary Choice

In order to compare the MMMP converter to the SM converter, a preliminary design of the MMMP converter must be done. One of the first choices in the power stage design is the DCM boundary. That is, below what power level should the converter enter the discontinuous conduction mode of operation? The DCM boundary is important due to its effect on efficiency. The DCM boundary choice determines the

amplitude of ripple current, which determines the peak switch current. Larger peak currents translate to higher RMS currents, which lead to higher conduction losses. A higher DCM boundary, however, results in a lower required inductance. This lower inductance value usually means a smaller, lighter core can be used. An analysis must be done to determine if the increased losses are offset by the reduced magnetics weight.

The switching frequency for the MMMP was chosen to be 45 KHz. An analysis of the battery discharger was done [2] to determine the optimum switching frequency for maximum efficiency. Since the charger is the dual of the discharger it follows that this analysis remains valid for the charger as well. This also provides compatibility with the battery discharger, which is important from the system EMI point of view.

An analysis of four different DCM boundary levels for the MMMP design was done. The boundaries were 150, 300, 800, and 1200 W. These power levels are for the charger as a system. When calculating values for each module, the system output power must be divided by 4 (the number of modules). To determine the inductance required to support a given boundary condition, it can be shown that at the boundary:

$$I_L = \frac{1}{2} \cdot \Delta i_L, \tag{2.17}$$

since

$$I_L = \frac{V_{Bat}}{R}, \tag{2.18}$$

and

$$\Delta i_L = \frac{V_{Bat}}{L} \cdot D' \cdot T_s. \tag{2.19}$$

Substituting (2.18) and (2.19) into (2.17) yields the equation for determining the minimum inductance required for a given DCM boundary:

$$L = \frac{D' \cdot R \cdot T_s}{2}. \tag{2.20}$$

To ensure the proper DCM boundary, (2.20) must be evaluated with parameters that will produce the maximum value of L. This condition occurs when V_{Bat} is at its maximum. This case produces the largest value for D′ and R. The value of R is the dc resistance required to support the power level. When calculating L for each module, it should be remembered that each module sees 1/4 the output power, and therefore R should be calculated accordingly.

To decide on a DCM boundary, the losses and weight are calculated for each boundary condition. The loss analysis and current characteristics can be found in Table 2.1. The current characteristics (i.e. I_{pk}, I_{RMS}) are useful in analyzing filter requirements and loss trends. It can be seen from the table that as the DCM boundary is increased, the RMS value of the current also increases. This causes an increase in conduction loss within the switch and diode. The switching losses tend to stay constant since an increase in peak current value is offset by a decrease in the minimum current (I_{val}) value.

To calculate the magnetic losses a spreadsheet program was developed. This program allows the comparison of several cores at once. The user inputs the pertinent manufacturers' data such as permeability, core dimensions, weight, length/turn, and the program calculates number of turns, core and copper loss, copper weight flux density and other relevant data. The program is useful in finding the smallest, most efficient core through several user iterations. The magnetic design was optimized for each boundary condition. It can be seen from Table 2.1 that core and copper losses increase

TABLE 2.1. DCM BOUNDARY COMPARISON

	Boundary Level	150 W	300 W	800 W	1200 W
L_{crit},μH		627	313	118	78
I_{avg}		5.75	5.75	5.75	5.75
Δi		1.06	2.12	5.64	8.47
I_{pk}		6.28	6.81	8.57	9.98
I_{val}		5.22	4.69	2.92	1.52
I_{LRMS}		5.76	5.78	5.97	6.24
I_{QRMS}		4.20	4.22	4.36	4.56
I_{DRMS}		3.93	3.95	4.08	4.27
Semiconductor Losses					
Transistor Switching		2.41	2.41	2.41	2.41
Transistor Conduction		1.50	1.51	1.62	1.77
Diode Switching		2.42	2.38	2.27	2.16
Diode Conduction		2.69	2.69	2.78	2.91
Magnetic Losses					
Core Loss		1.08	2.8	3.6	5.2
Cu Loss		4.24	2.8	5.1	5.7
Total (4 Modules), Watts		41.43	41.66	45.16	47.99

as the boundary condition increases. This increase is much more dramatic than the semiconductor loss increase, but it is to be expected due to the nature of the magnetic loss mechanism. The main component of core loss is a function of ac flux. The loss is related to the flux exponentially, and therefore increases in Δi (which directly correspond to increases ΔB) will cause a significant increase in loss. This is true even when accounting for the smaller core and reduced permeability usable for the lower inductance value.

It can be seen from Table 2.1 that the 150 W and 300 W boundary conditions are the most efficient by approximately 7 W. The 150 W and 300 W conditions have approximately the same total losses. While the 150 W condition has slightly lower semiconductor losses the 300 W level has lower magnetic losses (due to the smaller core and reduced number of turns required). Since the 150 W condition requires more inductance, it is important to compare the weights of the four designs to determine if the increase in efficiency is offset by the potentially heavier magnetics. The weight comparison can be found in Table 2.2. It includes the magnetic components and the heatsink weight required for the given loss. The heatsink weight uses a factor of 26 W/Kg. This is a somewhat conservative factor based on spacecraft design [2]. The semiconductor weights are not included because these weights will be the same for each design.

From Table 2.2 it can be seen that there is no significant weight advantage to any of the designs above 150 W. This is due to the lighter magnetics components of the higher DCM levels being offset by the increased heatsink weight due to the reduced efficiency. Below 300 W however, there is no significant increase in efficiency to offset the heavier magnetics. The 150 W design in fact has higher copper losses due to the increased number of turns needed to achieve the desired inductance. The 150 W design is therefore not chosen due to its higher weight. Since there is no significant weight

Table 2.2. Weight Comparison

Weight (grams)	Boundary Level	150	300	800	1200
Core		.534	.368	.188	.144
Copper		.356	.198	.128	.096
Heatsink		1.60	1.60	1.74	1.84
Total (kilograms)		2.49	2.16	2.10	2.08

advantage between the remaining DCM levels, the more efficient system should always be chosen. This is true not only from a component point of view but also from the system point of view. Since a less efficient design requires more system power to charge the batteries to the same level, this has a negative impact on the complete power system. This data supports the choice of the 300 W DCM boundary condition. In addition, if the filter requirements of the different designs are compared, it is clear that the 300 W design requires less filtering than the higher DCM levels. This is due to the larger Δi and I_{pk}. Therefore, due to the better efficiency and reduced filter requirements the DCM boundary of 300 W is chosen.

In order to fairly compare the MMMP and the SM converters, the SM design should be optimized as well. The same procedure was followed as for the MMMP case. The boundary conditions, however, were 200 W, 300 W, and 600 W. The same efficiency relationship holds for the SM converter as for the MMMP. As DCM level increases, efficiency decreases. However, in the SM case, the inductor is carrying all the load current. As DCM level increases, there is a much more significant increase in Δi and I_{pk}. Table 2.3 presents pertinent current data. It can be seen that it is impractical for the SM case to operate at higher DCM levels. The core loss associated with the large ripple currents is prohibitive. In addition, the filter requirements would cause one to avoid such high peak-peak input current surges. The SM converter does not enjoy the benefits of current ripple cancellation as the MMMP converter does, and a DCM level of 600 W would require having to deal with a $31.5A_{pp}$ input current waveform. This is obviously to be avoided. Similarly, as in the MMMP case, going to an even lower DCM boundary provides no efficiency advantage and negatively impacts weight. For these reasons, the SM DCM boundary choice is 200 W.

TABLE 2.3. SM DCM BOUNDARY COMPARISON

	Boundary Level	200 W	300 W	600 W
L_{crit},μH		58	23	12
I_{avg} (amperes)		23	23	23
Δi (amperes)		5.64	8.46	16.93
I_{pk} (amperes)		25.82	27.23	31.46
I_{val} (amperes)		20.18	18.76	14.53
I_{LRMS} (amperes)		23.06	23.13	23.51
I_{QRMS} (amperes)		16.84	16.89	17.17
I_{DRMS} (amperes)		15.75	15.80	16.06

2.4 Topology Trade-Off

Using the equations developed in the previous sections a quantitative comparison of the SM and MMMP battery chargers can be done. The SM battery charger uses four MOSFETs in parallel, switching at 90 KHz (Fig. 2.1). 90 KHz was chosen to keep the filter and magnetic components as small as possible [1]. The MMMP charger also uses 4 MOSFETs in parallel although the switching frequency is reduced to 45 KHz. The SM converter switches at the higher frequency to reduce the size of the magnetic components and to improve the filter requirements. Recall that the SM converter (Table 2.3) has rather large input current pulsing. If the switching frequency is reduced the input filter would become prohibitively large. Also, since the energy storage inductor handles all the charge current, decreasing the frequency would have a negative impact on the inductor size and weight.

If the loss equations of Section 2.2 are analyzed, it can be seen that there is a strong frequency relationship. The semiconductor switching losses are directly proportional to frequency. The turn-on and turn-off losses double as frequency doubles. In addition, the capacitive discharge loss is frequency dependant. The magnetic losses are also frequency dependant.

The semiconductor component parameters used in the loss analysis are found in Table 2.4. These parameters were either taken from the manufacturers' data sheets or were measured in the laboratory.

Using the parameters from Table 2.4. a loss analysis of the two converters was performed. Table 2.5 shows the results of that analysis. It is clear from Table 2.5 that the MMMP charger is significantly more efficient than the SM charger. It is also clear that the areas of difference are the losses associated with switching. This is to be

TABLE 2.4. Component Parameters

Parameter	
IRF250	
Rise Time, t_r	200 ns
Fall Time, t_f	200 ns
ON Resistance, R_{DSon}	0.085 Ω
Drain-Source Capacitance	800 pF
UES706	
Rise Time, t_r	200 ns
Fall Time, t_f	200 ns
Reverse Recovery, t_{rr}	50 ns

expected from the examination of the loss equations. The MOSFET switching loss for the SM case is slightly greater than twice the MMMP due to additional losses associated with semiconductor snubbers. These snubbers were needed in the design of the SM converter [1] but were not required in the MMMP converter. In addition the SM charger was not able to turn on or off as fast as the MMMP charger. This was done to facilitate current sharing between the modules and reduce switching spikes on the MOSFETs which would exceed the V_{DS} derating [1].

The magnetic losses are also higher in the SM case. This is due to the increased ac flux in the inductor. It should be noted that the core loss and copper loss is approximately equal. This is a good indication that the magnetic designs have been optimized. A good magnetic component design usually divides the total loss equally between the core and the windings.

In practice, the SM charger was able to achieve 94% efficiency at maximum charge rate (23 A) and minimum battery voltage (64 V). The MMMP charger was able to achieve 97% efficiency under the same conditions. A plot of measured efficiency data can be found in Fig. 2.3. Clearly the MMMP battery charger exhibits a significant efficiency improvement over the full operating range.

TABLE 2.5. SM/MMMP Loss Comparison

	Single Module	Multi-Module
Semiconductor Losses		
MOSFET Switching	27.6	9.7
MOSFET Conduction	6.1	6.0
Diode Switching	19.3	9.6
Diode Conduction	10.8	10.8
Magnetic Losses		
Copper	3.3	2.8
Core	3.8	2.8
Total (watts)	70.8	41.7

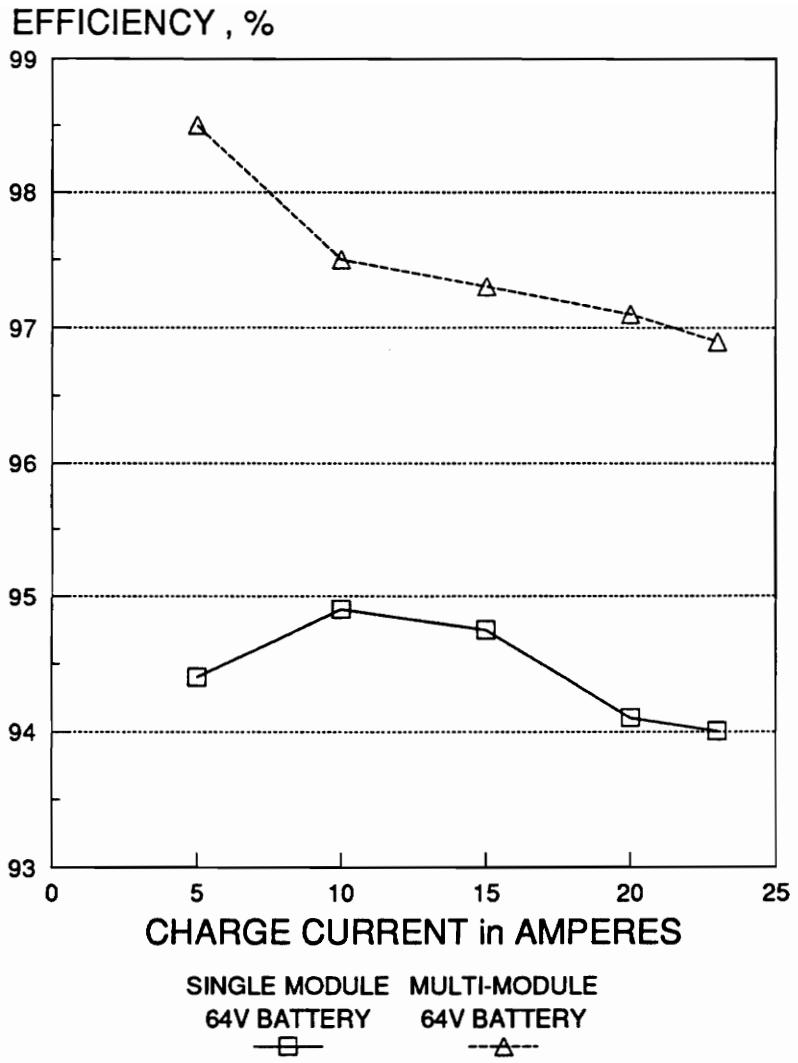


Figure 2.3 Power Stage Efficiency Comparison

The reduction in power stage loss is significant. However, it must be determined whether the energy savings compensates for the increased part count. Recall that both converters require four MOSFETs. The SM converter uses two diodes and one power inductor. In addition, the SM charger requires an input filter consisting of one filter inductor and two capacitors. A second stage output filter is also required. This filter consists of a filter inductor and capacitor. The MMMP charger uses four diodes and four power inductors. An input filter consists of a filter inductor and capacitor. No second stage output filter is needed. The MMMP charger therefore requires three additional power inductors (although individual inductors may be smaller due to decreased power handling requirements) and two additional diodes. To fairly compare weight though, heatsink weight should be factored in. A less efficient design will require additional heat sink weight to maintain similar operating temperatures. Table 2.6 shows the results of the weight comparison for individual power stage components. The filter component weights assume ripple attenuation to an equal level. The weights are total system weights.

From the table it can be seen that even with the additional component weight, the MMMP charger is lighter than the SM charger. This is due to the weight penalty caused by higher losses. The MMMP charger inductor weight is significantly greater than that of the SM. The heat sink weight differential however, is more significant. This analysis shows the importance in considering efficiency in the weight comparison.

From an efficiency and weight point of view, the MMMP charger shows substantial improvement over the SM charger.

TABLE 2.6. SM/MMMP Weight Comparison

COMPONENT	Single Module	Multi-Module
	Mass (grams)	Mass (grams)
Input Filter Inductor	26	20
Input Filter Capacitor	80	60
MOSFETs	52	52
Diodes	14	28
Energy Storage Inductor	94	566
Output Filter Inductor	28	0
Output Filter Capacitor	9	9
Heat Sink	2722	1600
Total	3025	2335

2.5 Filter Requirements

The trade-off analysis so far has demonstrated significant efficiency improvements over the SM case. This increase in efficiency is clearly enough to justify the use of the MMMP battery charger over the SM charger. However, the MMMP charger exhibits a further advantage that in some applications would be enough on its own to indicate implementation: the nature of the switching of the MMMP converter significantly reduces input pulse and output ripple current. This reduction in current ripple reduces the filter requirement and therefore can lead to a smaller, lighter filter.

The reduction in input pulse current can be seen in Fig. 2.4. The input current is the sum of the individual modules input current waveform. The peak-to-peak current pulse occurs when a module turns off. In the SM converter, the module carries the full input current, and therefore, when the switch turns off a 25 A discontinuity results. In the MMMP converter however, each module handles one-fourth of the total current. The MMMP converter only experiences a discontinuity of one-fourth that of the SM converter (assuming a proportional Δi). Fig. 2.4 also shows the increase ripple frequency for the MMMP charger. The ripple frequency is four times the individual module's frequency. This allows the individual modules to switch at a lower frequency to achieve efficiency benefits, while system filtering requirements are reduced due to the relatively high ripple frequency. In this case the SM converter switching frequency is 90 KHz; the ripple frequency of the MMMP charger is 180 KHz. The SM converter could not operate at 180 KHz without a severe efficiency penalty.

To quantify the pulse current waveform the parameters i_a, i_b, i_c, and i_d are derived. These quantities are identified in Fig. 2.4. The equations are valid for $0.5 \leq D \leq 0.75$, which is the range for the given design:

$$i_a = \frac{3 \cdot V_{Bat}}{4 \cdot R} - \left(\frac{V_{Bus} - V_{Bat}}{L} \right) \left\{ \frac{1}{2} \cdot D \cdot T_s - (2 \cdot D - 0.75) T_s \right\}, \tag{2.21}$$

$$i_b = \frac{2 \cdot V_{Bat}}{4 \cdot R} - \left(\frac{V_{Bus} - V_{Bat}}{L} \right) \{ D \cdot T_s - (2 \cdot D - 0.75) T_s \}, \tag{2.22}$$

$$i_c = i_b + \frac{2 \cdot (V_{Bus} - V_{Bat})}{L} (D) \cdot \frac{T_s}{4}, \tag{2.23}$$

and

$$i_d = i_c + \frac{V_{Bat}}{4 \cdot R} - \frac{1}{2} \left\{ \frac{(V_{Bus} - V_{Bat})}{L} \cdot D \cdot T_s \right\}. \tag{2.24}$$

An analysis of these equations confirms the peak Δi is 6.8 A. This corresponds to the peak value of switch current. The MMMP charger therefore requires 20 dB less attenuation than the SM charger to achieve the same input current ripple as seen by the bus.

The output current ripple reduction is equally significant. The output current waveform is shown in Fig. 2.5. Similarly to the input current, the output current waveform is the sum of the individual module's inductor currents. This summing action tends to cancel out the ripple. In fact, at duty cycles of 0.5 and 0.75, the ripple would cancel completely. The output current ripple is given by Eq. 2.25. The worst case ripple occurs between the two null conditions and is equal to D = 0.63. Under this condition the ripple current is 0.51 A. This compares to the individual module's Δi of 2.2 A and the SM chargers ripple current of 5.6 A. This is a significant reduction in ripple

current which will translate into reduced output filter requirements. In the SM charger design, a second stage LC filter was required to attenuate the output ripple current to the battery ripple current specification; this was not required for the MMMP converter.

$$\Delta i_{Bat} = \frac{3 \cdot V_{Bus} - 4 \cdot V_{Bat}}{L} \cdot \left(D \cdot \frac{T_s}{4} \right) \tag{2.25}$$

Table 2.7 quantifies the significant input and output filter requirement improvements due to the multi-phasing of the modules. The Table shows filter data assuming the input current ripple is to be attenuatied to .2 A at the input to the charger and the output current has a maximum ripple of .2 A at the battery. The data shows the MMMP input and output current ripple is substantially lower, allowing for significantly lighter filter components.

TABLE 2.7. SM/MMMP Filter Comparison

COMPONENT	Single Module	Multi-Module
Input Current Ripple (A)	25.8	6.8
Output Current Ripple (A)	5.6	.510
Ripple Frequency (KHz)	90	180
Input Filter Fc (KHz)	10	40
Input Filter Weight (gm)	106	80
Output Filter Weight (gm)	40	9

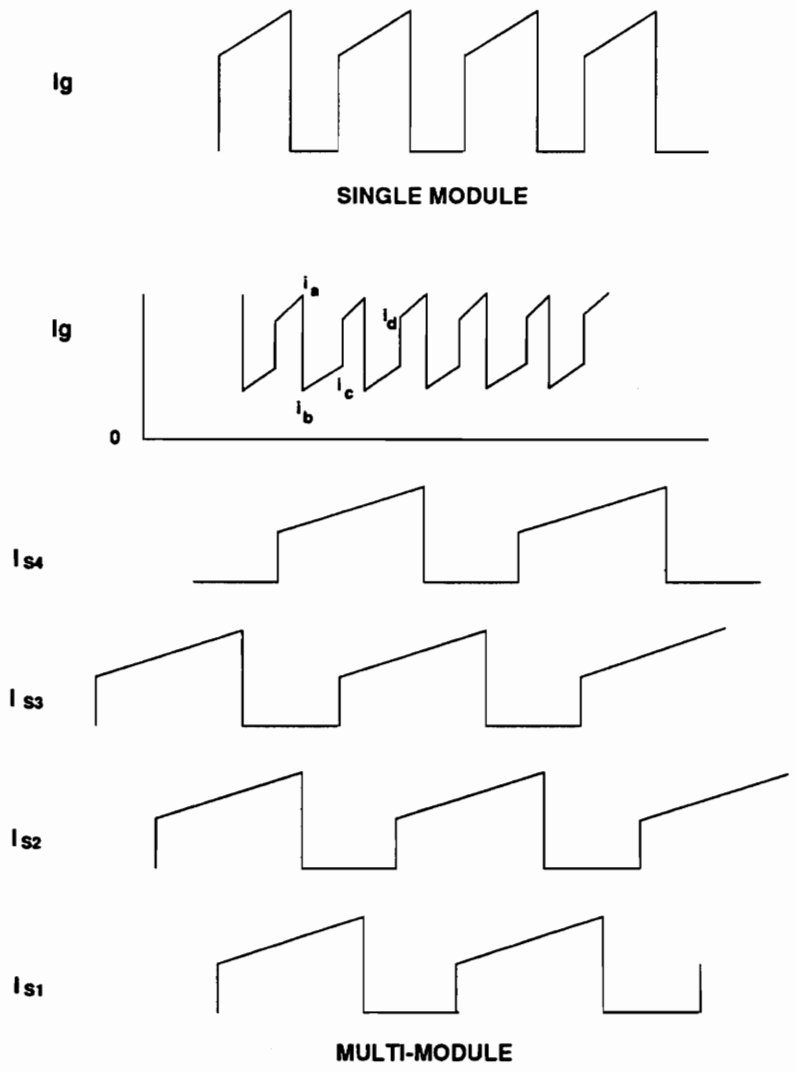


Figure 2.5 Input Current Comparison

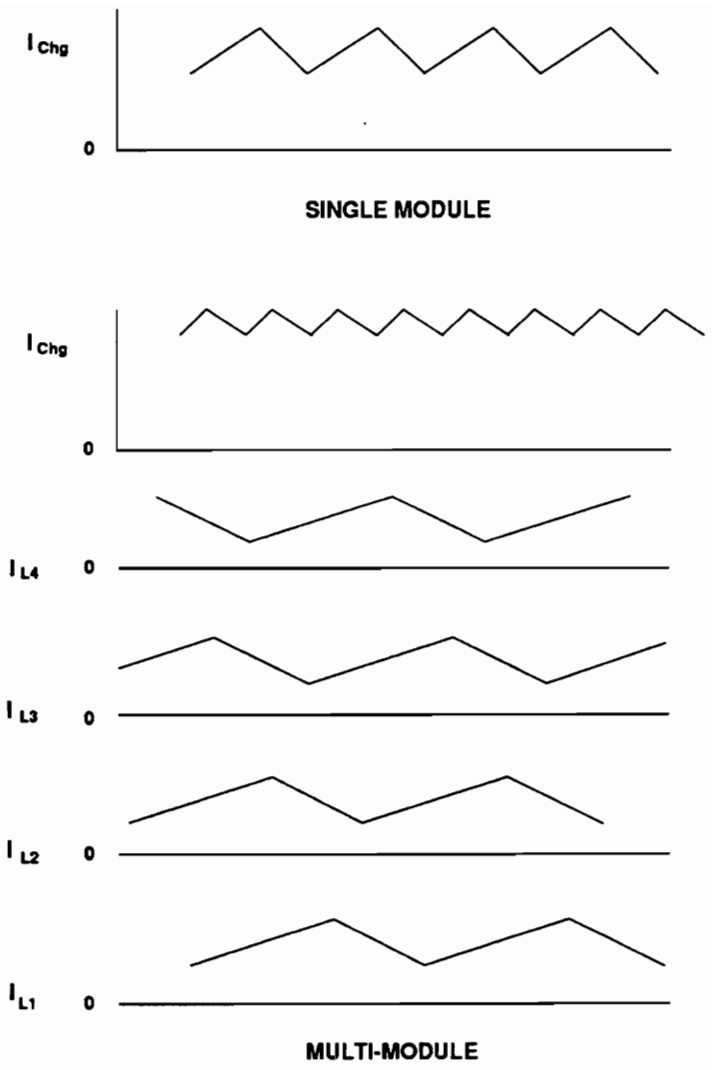


Figure 2.6 Output Current Comparison

2.6 Summary

A detailed loss analysis was performed on the SM and MMMP converters. It was shown that the MMMP converter is able to achieve higher efficiency and lower weight than the SM converter. The higher efficiency is due to the reduced switching losses associated with a reduced switching frequency. The increase in efficiency is able to off-set the added weight due to the increased parts through decreased heat sink weight. The lower switching frequency is possible due to the improved dynamics of the input and output current waveforms. The multi-phasing of the modules greatly reduces the pulse and ripple currents normally found in the buck converter. This multi-phasing also increases the frequency of the current waveforms. The combination of reduced ripple and increased overall frequency significantly improve the filter requirements of the MMMP battery charger.

3. Power Stage Design

3.1 Introduction

A schematic of the battery charger power stage is shown in Fig. 3.1. It consists of an input filter, switching circuit (MOSFET and diode pair), output filter, and PWM and gate drive circuitry. The design of these functional blocks will be documented in this chapter. The preliminary design details were derived in Chapter 2. These details include DCM level and switching frequency. There are four individual power stage modules within the MMMP battery charger. These modules consist of a switch/diode pair, energy storage inductor, and related PWM and gate drive circuitry. The input filter and output filter capacitor are shared by the modules.

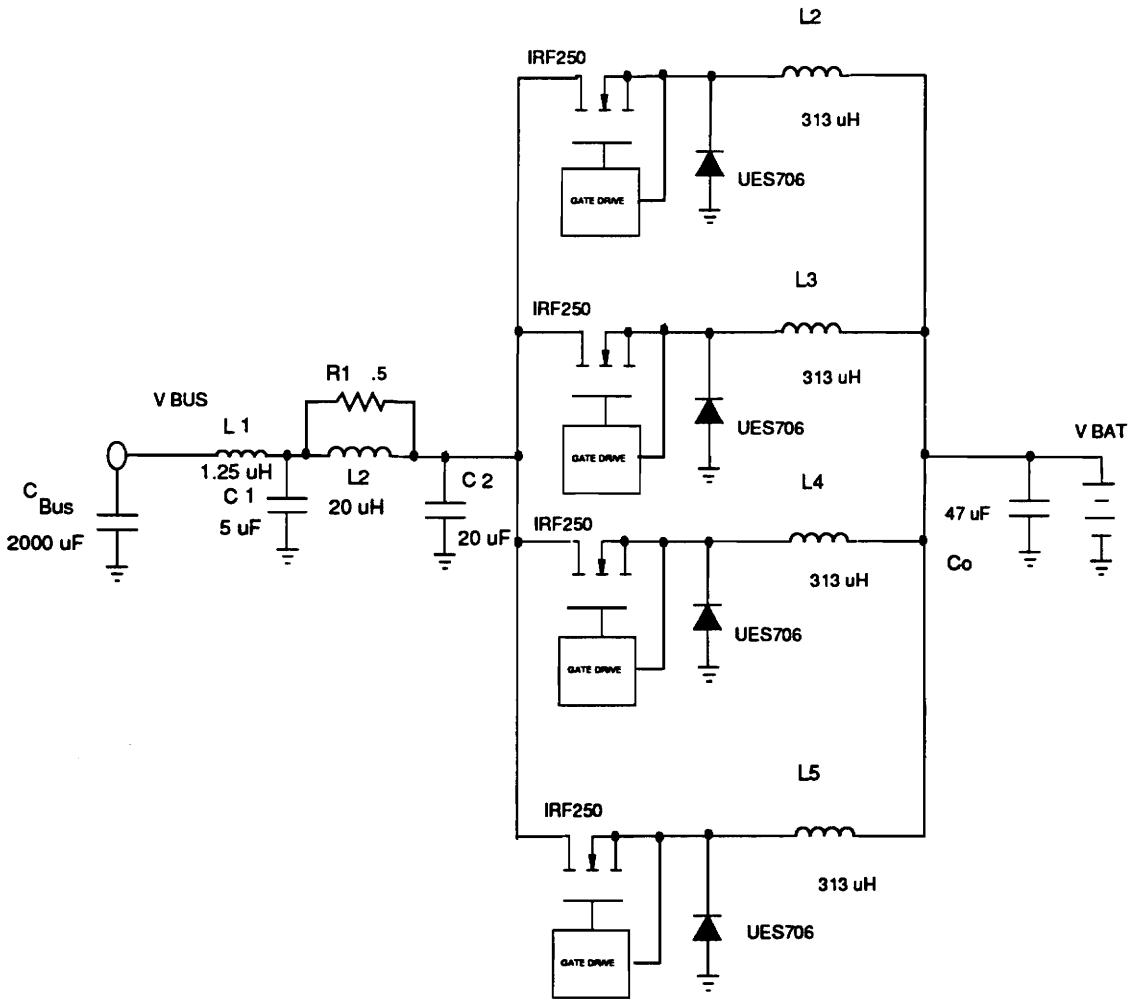


Figure 3.1. MMMP Power Stage

3.2 Switching Circuit

The switching circuit consists of the power MOSFET diode pair. This pair processes the converter power by way of the chopping function. The four individual modules share the power processing so that each module handles one fourth of the total output power. The design procedure for this circuit entails picking semiconductors that can handle the voltage and current stress.

From Table 2.1 it can be seen that for the 300 W DCM boundary condition the peak switch (or diode) current will be 6.8 A and the RMS current 4.22 A. The switches are subjected to a bus voltage of 120 V. Allowing for bus voltage transients and switching spikes, a conservative MOSFET voltage rating would be 180 V. The aerospace derating guideline for maximum voltage stress on a MOSFET is 80% of manufacture's V_{DS} rating. To meet this requirement, a 200 V MOSFET must be chosen. A good choice for a 200 V MOSFET is the IRF250. This MOSFET is on the NASA approved parts list (a requirement for use) and has a low R_{DSon}. The R_{DSon} parameter is very significant in MOSFET selection since conduction loss within the switch is a function of ON resistance. The IRF250 has a nominal R_{DSon} of 0.085 Ω. The IRF250 has a current rating of 30 A continuous current and 150 W maximum power dissipation. These ratings are well above the actual circuit conditions and meet all deratings.

The diode is also subjected to the 120 V bus voltage. In addition it is necessary to select a fast recovery diode to minimize switching losses and switching spikes. The diode selected was the UES706. The UES706 is a fast recovery (50 ns) and high voltage (400 V) device.

3.3 PWM and Gate Drive Circuitry

The PWM circuit controls the switching of the converter. Since each module of the converter is 90° phase shifted from the previous module, four separate PWM signals must be generated. This could be done by synchronizing four commercial PWM ICs. However, to provide greater flexibility in ramp slope design and noise immunity, a discrete PWM circuit was developed [3]. The discrete PWM circuitry is found in Figs. 3.3 and 3.4. This circuit allows a greater input voltage signal from the current injection control (CIC) circuit. This reduces the need to attenuate the dc level and therefore preserves more of the ac information. This circuit also allows changes to be made in the ramp slope easily; this is especially useful when performing control loop optimization.

To drive the circuit, there is a clock generator which oscillates at 180 KHz. This 180 KHz signal is divided down to four 45 KHz clock signals ($\varphi 0$ - $\varphi 3$) that are sent to the respective modules. Each clock signal is phase-shifted 90°. This produces the multi-phasing action desired. This clock generator is shown in Fig. 3.3.

The discrete PWM circuit consists of a ramp generator, a comparitor to perform the PWM, a latch (MC14013) to prevent multiple triggering within a period, and a NOR gate to provide duty cycle limiting. The four modules have identical circuits to perform the PWM function. The PWM circuit is shown in Fig. 3.4. The operation of the circuit can best be described by following the clock signal (φ). When the clock signal is high, the capacitor is discharged through the NPN transistor. This also forces the output of the NOR gate to be low, irrespective of the output of the latch; this limits the duty cycle. Once the clock signal goes low, the capacitor voltage of the ramp generator begins to increase but is still lower than the error voltage. This causes the output of the NOR gate to go high (since the output of the latch is also low), thereby turning on the MOS-

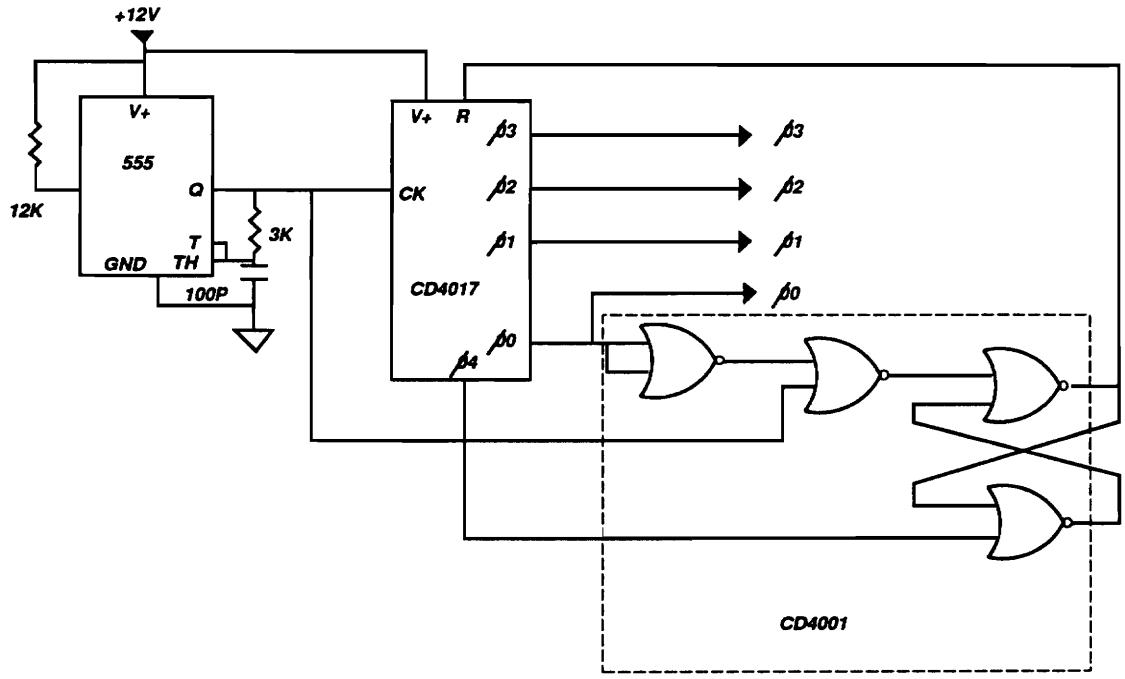


Figure 3.2. Clock Generator

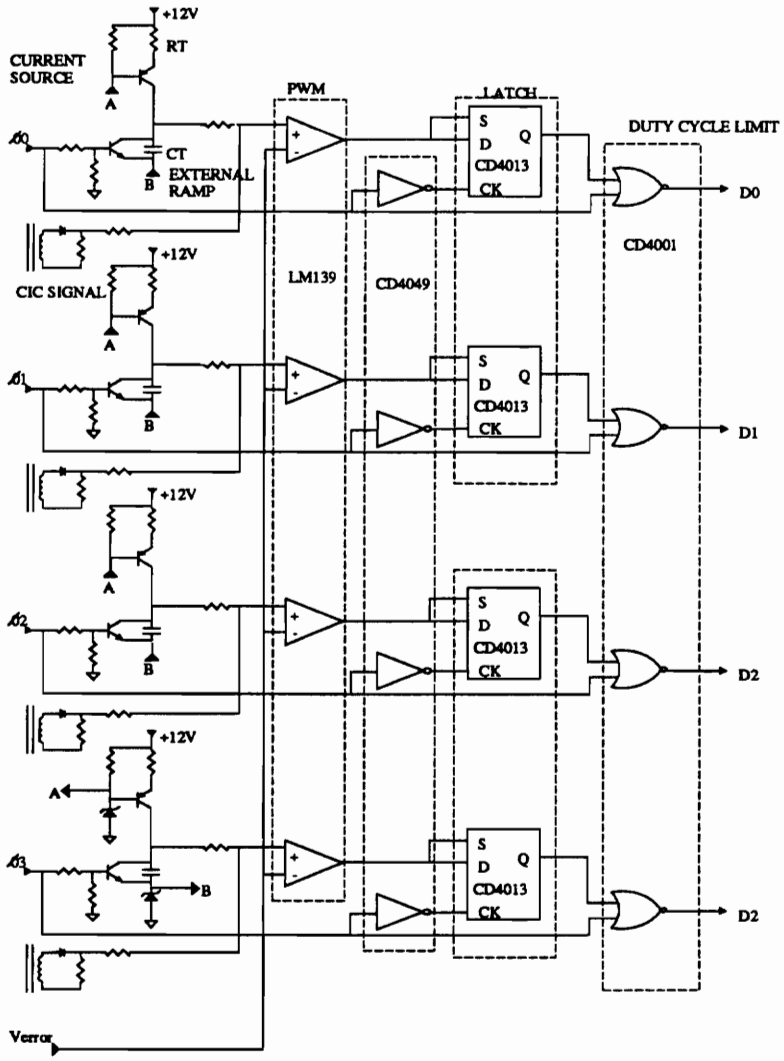


Figure 3.3. Discrete PWM Circuit

FET. When the ramp plus CIC signal equals the error signal, the comparitor switches high, which sets the latch output high. This high signal causes the NOR gate to go low, which turns off the MOSFET. This all happens while the clock signal is low. When the clock signal goes high again, the capacitor is shunted, and the cycle starts all over.

The gate drive circuit is shown in Fig. 3.5. Again, since the MOSFETs are not switched together, four independent (and identical) gate drives are required. The gate drive circuit is driven by the UC3707 IC. This IC provides the drive current needed to turn on the MOSFET. The output of the CMOS NOR gate is not capable of sourcing enough current to drive the FETs. The battery charger is a buck topology and therefore requires a floating gate drive. The secondary side reference must be able to float at the battery potential. This is accomplished with the gate drive transformer. In addition, since the duty cycle varies, the secondary side has dc restoration components (the R C). Since the primary side is capacitively coupled to ensure ac voltage on the transformer, the dc level of the drive signal is reduced. As duty cycle increases, this reduction can become severe. The secondary side capacitor in effect adds back the dc voltage "lost" on the primary side.

To prevent droop of the gate drive signal, the capacitors must be sized to have an RC time constant much greater than the switching frequency. In this case the capacitors were chosen to be 1 μF. This provides for a time constant of 1 ms. The secondary side resistance also serves to provide a load to the gate drive transformer. When the gate drive initially turns off, the current flowing in the magnetizing inductance needs to continue flowing to maintain flux continuity. If the secondary side does not present a low enough impedance, the magnetizing current will attempt to flow back into the drive IC. This could potentially damage the drive circuit. Empirically it was found that a resistance of 1 KΩ was satisfactory.

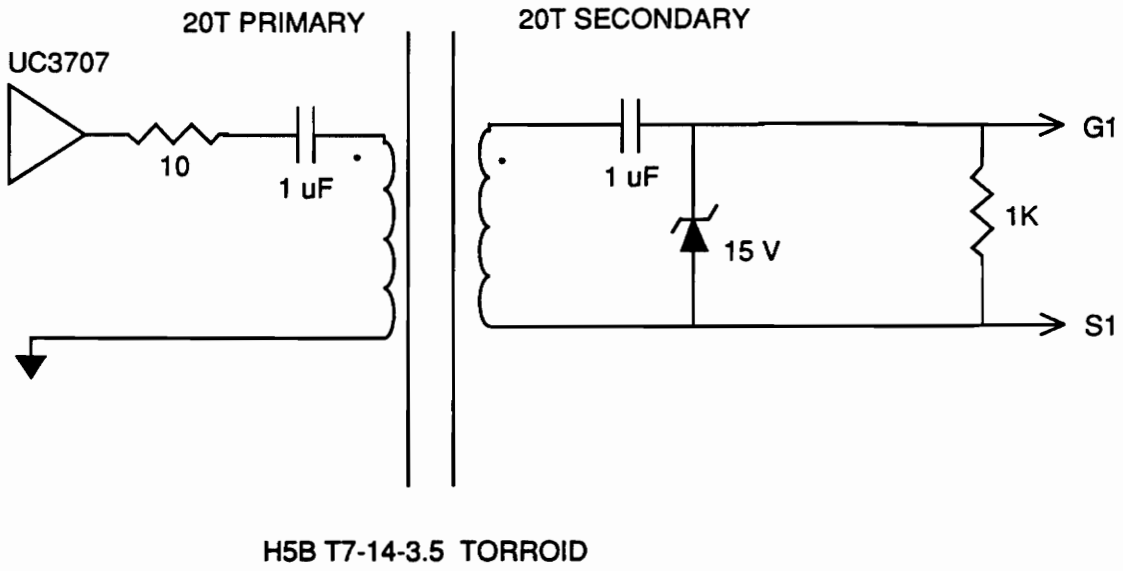


Figure 3.4. Gate Drive

The gate drive transformer is essentiality a pulse transformer. The transformer must be capable of transmitting a large pulse of current to charge the gate-to-source capacitance of the MOSFET. The transformer should do this without requiring a large magnetizing current which would place added burden on the drive circuit. The core material chosen was H5B. This material provides high permeability which allows a low number of turns (and therefore low leakage inductance) to give the required magnetizing inductance. The material has a maximum flux density of 4000 G. The core chosen was the T7-14-3.5. This is a toroid core with a cross sectional area (A_e) of .118 cm^2. The number of turns was chosen to be 20. This ensures low leakage inductance. To calculate the maximum flux density, the following equation must be evaluated:

$$B_m = \frac{V_p \cdot t_{on} \cdot 10^8}{N_p \cdot A_e}. \tag{3.1}$$

The maximum flux occurs with maximum on time. Maximum on time is given by:

$$t_{on} = D_{\max} \cdot T_s, \tag{3.2}$$

where D_{max} is equal to 0.7 and T_s = 22.2 µs. The primary voltage (Vp) is the drive IC output voltage, minus the average voltage of the waveform that is subtracted out by the capacitor:

$$V_p = 12 \cdot D = 5.6V. \tag{3.3}$$

The maximum flux density is therefore:

$$B_m = \frac{5.6 \cdot 16\mu s \cdot 10^8}{30 \cdot 0.118}$$

$$B_m = 2.5 \quad KG.$$

To ensure the magnetizing current is sufficiently small, the magnetizing inductance is first calculated. This core has an inductance factor of 2100 nH/T^2.

$$L_m = 2100nH/Turn \cdot (30Turns)^2 = 1.89 \quad mH, \tag{3.4}$$

$$i_m = \frac{V \cdot t_{on}}{L_m}, \tag{3.5}$$

$$i_m = \frac{12 \cdot 16\mu s}{1.89mH} = 101 \quad mA_{p-p}.$$

Since the UC3707 is capable of sourcing 1.5 A, the magnetizing current is sufficiently small as to be negligent.

Switching waveforms for the MOSFET and diode are shown in Fig. 3.2. The waveform picture was taken in the actual circuit with battery voltage equal to 64V and 23A charge current. It can be seen that these waveforms are remarkably clean. In fact the switches are spike free. The devices are able to switch this cleanly due to the multiphasing operation and proper input filter design (see Section 3.5). The well designed gate drive circuit also contributes to the clean switching. Each module is handling less current and therefore has to interrupt less power, this results in lower spikes. The modules are operating with no snubbers. This is an added benefit to MMMP operation: switching speeds can be increased to reduce switching loss without causing large spikes and ringing. Lower spikes and ringing reduce control circuit noise contamination and EMI problems.

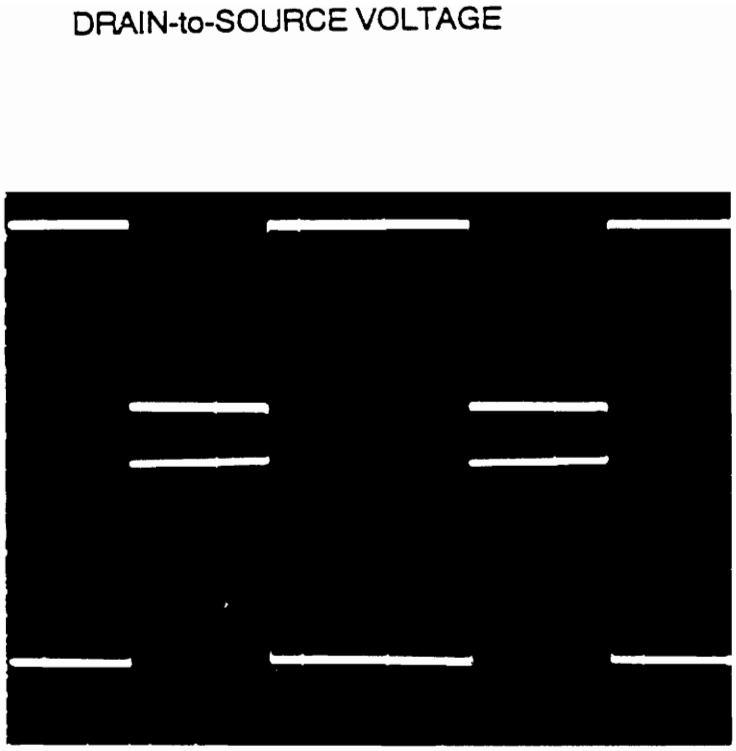


Figure 3.5. Drain-to-Source and Diode Voltage Waveforms

3.4 Output Filter Design

The output filter consists of the individual module's energy storage inductors and the common output capacitor. The design of the output filter inductor is critical to the operation of the system. The inductor design directly impacts the efficiency and weight of the power stage. The inductor was designed to minimize copper and core loss while keeping weight to a minimum.

The inductor design begins by chosing a DCM level. This procedure was done in Section 2.3. Recall a boundary level of 300 W was chosen corresponding to an inductance 313 μH. The core type chosen was a molypermalloy powder (MPP) toroid core. The MPP core exhibits low loss at this operating frequency and provides a wide range of permeabilities for design flexibility. To determine the size core to handle the power requirement, the area product (A_p) [4] is calculated:

$$A_p = \left(\frac{2 \cdot (Energy) \cdot 10^4}{B_m \cdot K_u \cdot K_j} \right)^{1.14}, \tag{3.6}$$

where B_m is the maximum flux density (0.3 Tesla), K_u is the window utilization factor (0.4 for toroids), and K_j is the current density coefficient (403). The maximum energy the core will need to sustain is:

$$E = \frac{1}{2} \cdot L \cdot I_{pk}^2, \tag{3.7}$$

$$E = \frac{1}{2} \cdot 313\mu H \cdot 6.8^2 = 7.2 \cdot 10^{-3} \quad W - s.$$

Therefore, A_p is equal to:

$$A_p = \left(\frac{2 \cdot (7.2 \cdot 10^{-3}) \cdot 10^4}{.3T \cdot 0.4 \cdot 403} \right)^{1.14}$$

$$A_p = 3.5cm^4.$$

This parameter gives an idea of the size core required. Magnetic design is, however, an iterative process and several cores should be investigated to find the smallest, most efficient design. After several cores were compared, the Magnetics 55252 core was chosen. The 55252 parameters are listed below:

Window Area (Wa)	4.26 cm^2
Cross Section (A_e)	1.072 cm^2
Magnetic Path Length (l_m)	9.84 cm
Length/Turn	5.40 cm
μ	160
L/1000 Turns (A_L)	215
Weight	92 gm

To design the inductor first the number of turns are calculated:

$$N = 1000 \cdot \sqrt{\frac{.313}{215}} = 38. \tag{3.8}$$

The magnetic force (H) is calculated to check for reductions in permeability:

$$H = \frac{0.4 \cdot \pi \cdot 38 \cdot 6.8}{9.84} \tag{3.9}$$

$$= 33 \quad Oe.$$

The manufacturer's data [5] shows that at this operating level, the core will lose approximately 30% of its initial permeability. This will result in an equal reduction in inductance. To maintain the desired level of inductance at maximum current, the turns are increased to 49. H is recalculated, and is equal to 42 Oe. At 42 Oe the core is operating with 55% of the initial μ. The extra turns will provide the required inductance at this reduced μ level. It should be noted that it is perfectly acceptable to operate at the reduced μ as long as the core is not close to saturation. The MMP material has a "soft" B-H curve which allows operation at higher H levels.

At this point it is important to ensure this number of turns will fit on the core. Since the inductor current is essentially dc with a small percentage of ac, the skin depth restriction is not relevant. In this case a heavy gauge wire can be used to reduce copper losses. The wire gauge chosen is 14 AWG magnetic wire with a cross sectional area of 0.0229 cm^2, which results in a current density (J) of 310 A/cm^2. To calculate the core window area filled with wire (F_w), the total wire area is divided by the window area. This ratio should be less than 0.4. In fact, since the wire used is rather heavy and will not wind as easily as smaller gauge wire, it would be safer to limit F_w to be less than 0.3. The fill ratio can be found to equal 0.26. This shows the wire will easily fit on the core with little difficulty. To calculate core loss, flux density must be calculated (Eq. 3.1). Flux density is 1236 G.

Since the manufacturer gives core loss equations in terms of an ac flux excursion (and a dc inductor flux excursion is limited to one quadrant) the core loss should be calculated using 1/2 the calculated ΔB. Core loss for this core is given by [5]:

$$P = 0.425 \cdot 10^{-11} \cdot F_s^{1.23} \cdot \Delta B^{2.21} \tag{3.10}$$

$$P = 0.425 \cdot 10^{-11} \cdot 45KHz^{1.23} \cdot 631^{2.21}$$

$$= .714.$$

The copper loss is :

$$P_{cu} = I_{RMS}^2 \cdot R_{cu}, \tag{3.11}$$

where the copper resistance is:

$$R_{cu} = N \cdot MLT \cdot \Omega/cm \tag{3.12}$$

$$R_{cu} = 49 \cdot 5.4cm \cdot 82 \cdot 10^{-6}/cm$$

$$= 21.7 \quad m\Omega.$$

The copper loss then is:

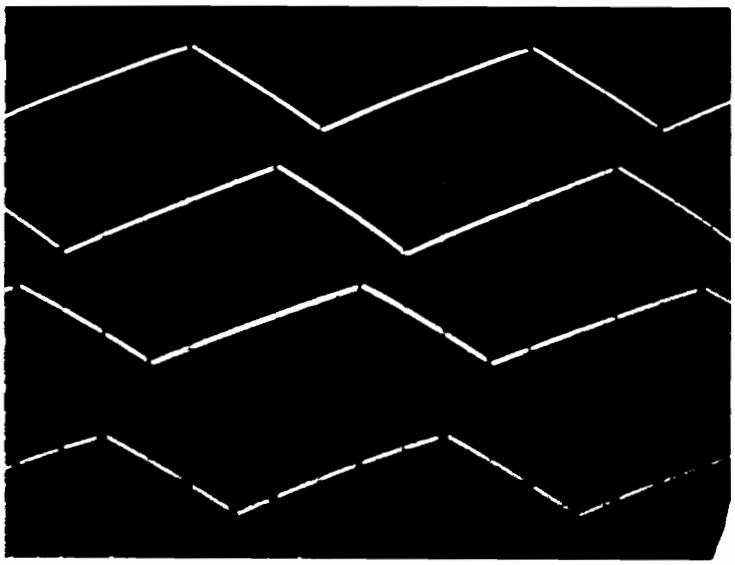
$$P_{cu} = 5.8^2 \cdot 21.7m\Omega = 0.73 \quad W.$$

The output current ripple specification is 200 mA_{pp}. Due to the multi-phasing nature of the output current, the ripple is significantly attenuated from the individual modules ripple value of 2.2 A. The worst case ripple current occurs at V_{Bat} = 80 V. In this condition the ripple current is 0.510 A_{pp}. This ripple is easily attenuated below the specification by the output capacitor and cabling inductance.

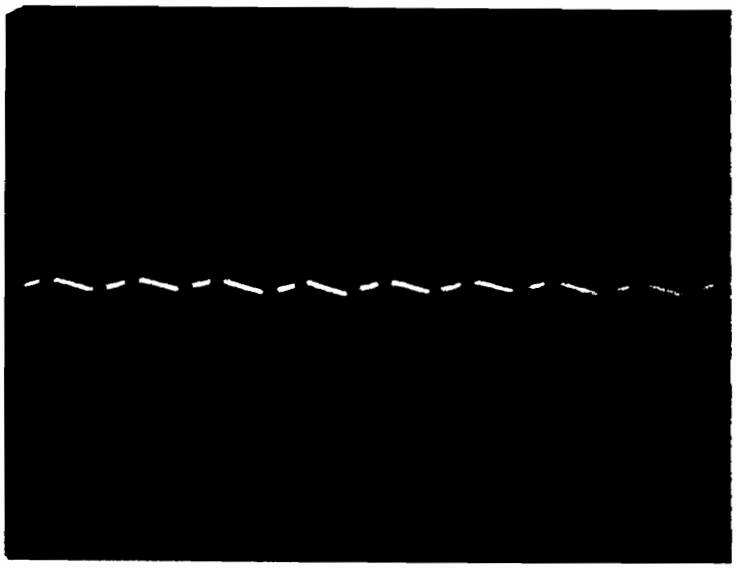
The output filter capacitor can be common to the four stages since this is the point where the output currents are summed to produce the charge current. The output capacitor in reality provides only minimal filtering. However, this filtering is enough to attenuate the output current to the specified value. While the capacitor appears to be in parallel with the battery (and therefore unnecessary), there is cabling impedance between the battery charger and the battery. In addition, the capacitor is beneficial during testbed testing.

Since the output capacitor does not see significant ripple current, the capacitor is chosen mainly for its small size and weight (since ESR is not a concern). The capacitor chosen is a 47 μF electrolytic, with a 200V rating.

Figure 3.6 shows a photograph of the individual modules inductor current and the charge current. Recall the charge current is the sum of the four modules' inductor currents. The charge current can be seen to have a ripple frequency of 180 KHz and ripple amplitude of approximately 50 mA. This is well below the specification. This is accomplished without the need for a second stage output filter as was required in the SM battery charger. This reduced filtering requirement is a significant improvement.



1 A/DIV



.1 A/DIV

Figure 3.6. Inductor and Charge Current Waveforms

3.5 Input Filter Design

While the MMMP charger does exhibit improved input current characteristics, it is a buck topology and has a pulsating input current waveform. Section 2.5 defined the input current waveform. Recall that the peak input current pulse had an amplitude of 6.8 A_{pp}. The charger is connected directly to the bus and therefore must meet the bus ripple specification of 200 mV_{pp}. In addition, the charger can be considered a load on the spacecraft bus during the charge regulation mode. The battery charger exhibits unique characteristics from the input filter design point of veiw. During charge regulation mode the filter is indeed an input filter, but during the bus regulation mode the filter acts as an output filter. In both cases however, the filters purpose is to attenuate the input current pulse to a level such that the bus voltage ripple is below the specified value.

A realistic ripple specification must therefore be set to ensure that the charger has minimal impact on bus ripple. Since the main component to be filtered is the input current, a realistic specification governing current ripple in a spacecraft environment is MIL-461B CEO3. This specification gives an allowable ripple current of 13.5mA at the ripple frequency of 180 KHz. The filter attenuation required, therefore, is 50 dB at 180 KHz.

There are several filter options to achieve the desired attenuation. A single stage L C filter could be used. Parallel damping could be provided by ac coupling a resistor through a large capacitor. This capacitor would have to be rather large due to the 200 V rating. A better technique is to provide damping by paralleling a resistor with the inductor. To achieve the required attenuation though, would require a rather large

resistance (since the filter becomes an R C filter at higher frequencies). Therefore, to get good attenuation with minimum size and weight, it is best to use a two section filter with damping provided by the resistor in parallel with the filter second stage inductance.

The second stage bus capacitor C_{in} is actually four 5 μF polypropolene capacitors distributed between the four modules for a total capacitance of 20 μF. In a multi-module configuration the placement of these capacitors is critical. It is important that they are as close to the MOSFETs as possible. The close placement, and the distributed nature of the capacitance, minimizes the circulating ripple current at the summing junction. This contributes to the clean switching operation of the MOSFETs and helps avoid noise problems. This is especially significant in the multi-phase operation since switches are turning on and off at different times. Excess switching noise can be coupled into an adjacent modules control circuitry causing false triggering or oscillations. These problems were experienced in the initial testing of the converter and found to be significantly reduced by good layout practices. It should also be noted that these capacitors are physically extremely close to each other. The distance should be as small as physically possible so as not to introduce any impedance between the capacitors. Any significant impedance between the capacitors would invalidate the assumption that the capacitors are indeed in parallel.

The polypropolene capacitors provide very low ESR (6 mΩ) to minimize ripple voltage at the summing junction. These capacitors must also handle the RMS input current. The capacitors are rated at 12 A RMS each, and therefore are operated well below their rating (since each module has a maximum RMS input current of 4.2 A).

The second stage filter inductor is chosen to have a value of 20 μH. This gives a corner frequency of 8 KHz, ensuring the filter corner frequency is beyond the outer loop

gain cross over frequency. In addition, this provides the overall filter with the required attenuation. Once the inductor and capacitor have been chosen, the remaining components can be calculated [6].

In order to have a smooth responce with no peaking the damping resistor value can be calculated for a Q = 0.5. The Q of the second stage is given by:

$$Q = \sqrt{L \cdot C} \cdot \frac{R}{L}, \tag{3.13}$$

$$R = 0.5 \cdot \frac{20\mu H}{\sqrt{20\mu H \cdot 20\mu F}}$$

$$= 0.5 \quad \Omega.$$

The first stage components can now be calculated forcing the case where the filter transfer function has all real roots. This will of course ensure minimal peaking.

$$L_1 = \frac{L_2}{16} = 1.25 \quad \mu H, \tag{3.14}$$

$$C_1 = \frac{C_2}{4} = 5 \quad \mu F. \tag{3.15}$$

Since the value of L_1 is 1.25 μH, a discrete inductor is not needed. There is approximately 20 feet of cable connecting the charger to the bus capacitor. This cable has an inductance of 2-3 μH. The cabling will therefore supply the required inductance. The capacitor chosen for C_1 is a polypropolene capacitor identical to the ones used in the filters' second stage. These capacitors are ideal for filter capacitors due to their low ESR.

The simpified transfer function for this filter is [6]:

$$H(s)=\frac{1}{\left(1+\frac{L_1}{R}\cdot s\right)(1+RC_2s)(1+RC_1s)}. \tag{3.16}$$

A bode plot of the filter transfer function is shown in Fig. 3.7. It can be seen that there is minimal peaking and an attenuation of approximately 50 dB at 180 KHz. The filter corner frequency is 10 KHz, which is beyond the outer loop gain cross over frequency (see Chpt. 4). This bode plot is of the forward voltage gain, however, this transfer function is also the reverse current gain.

A photograph of the ripple voltage at the summing junction and the bus capacitor is shown in Fig. 3.8. It can be seen that the bus ripple voltage is practically nonexistent. Some high frequency switching noise can be seen, but this has an amplitude of less than 50 mV. This is well below the ripple specification. The upper trace is the ripple at the summing junction and here can be seen the increased ripple frequency of 180 KHz. Even at the junction before the inductor, the waveform is remarkably clean. The ripple current at the bus is similarly well below the specification.

The inductor design follows the same procedure outlined in Section 2.4. The core chosen was the Magnetics MPP 55894. The number of turns required is:

$$N = 1000\cdot\sqrt{\frac{.02}{75}} = 16 \quad Turns.$$

To ensure against saturation the magnetic force must be calculated:

$$H=\frac{0.4\cdot\pi\cdot 16T\cdot 17A}{6.35}$$

$$H = 53 \quad Oe.$$

This core retains 85% of its permeability at 53 Oe. This is quite below saturation. The core loss can be calculated since the voltage across the inductor is equal to the ripple voltage at the summing junction (500mV):

$$\Delta B = \frac{(500mV)\cdot(0.4\cdot 5.5\mu s)\cdot 10^8}{16\cdot .654}$$

$$\Delta B = 10.5 \quad Gauss.$$

The core loss from this ac flux is, of course, negligent. The wire used was 14 AWG magnet wire. Sixteen turns of 14 AWG wire has a dc resistance of 3.2 mΩ. The maximum copper loss is therefore:

$$P_{cu} = 17^2 \cdot 3.2m\Omega = 925 \quad mW.$$

The input filter has been designed to attenuate the input current pulse and has been shown to perform that function quite well. It is important however to ensure there are no impedance interactions between the input filter and the charger that would cause system instability. A bode plot of filter output impedance and converter input impedance is shown in Fig. 3.9. It can be seen that the input filter is well damped and its output impedance is always below 0 dB. The input impedance of the charger has the same characteristics of a standard buck converter. There is at least 20 dB seperation between the impedances. This ensures against stability problems in the charge regulation mode. The fact that the filter corner frequency is beyond the loop gain cross over frequency gaurds against stability problems in the bus regulation mode.

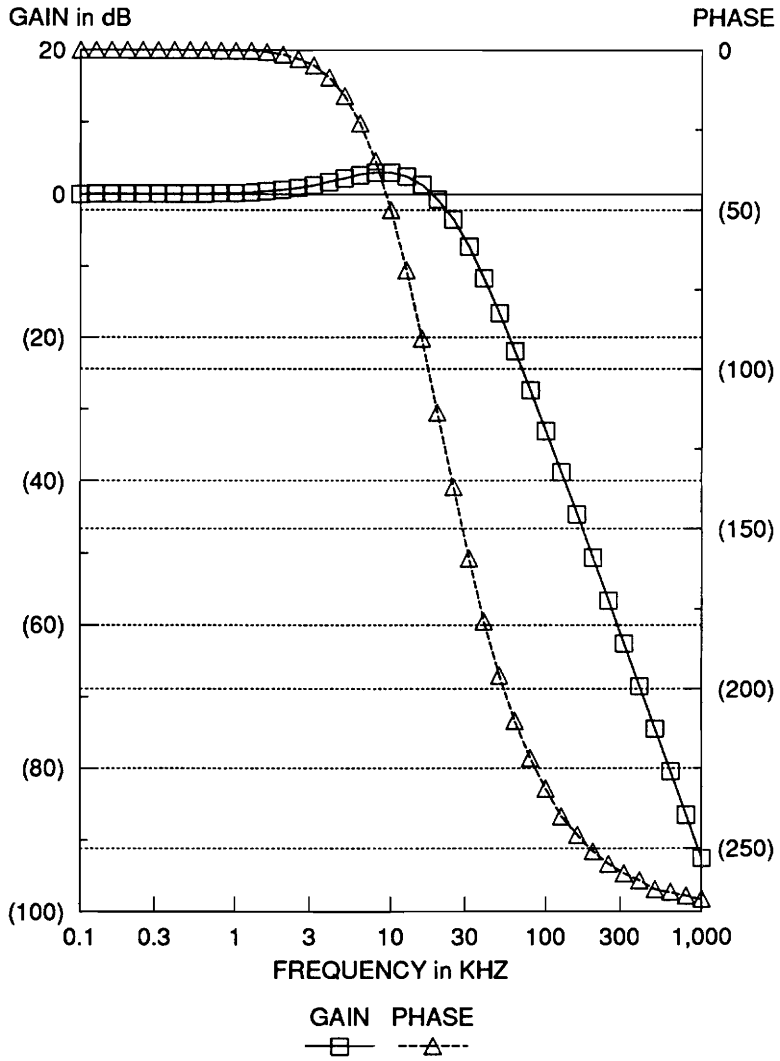
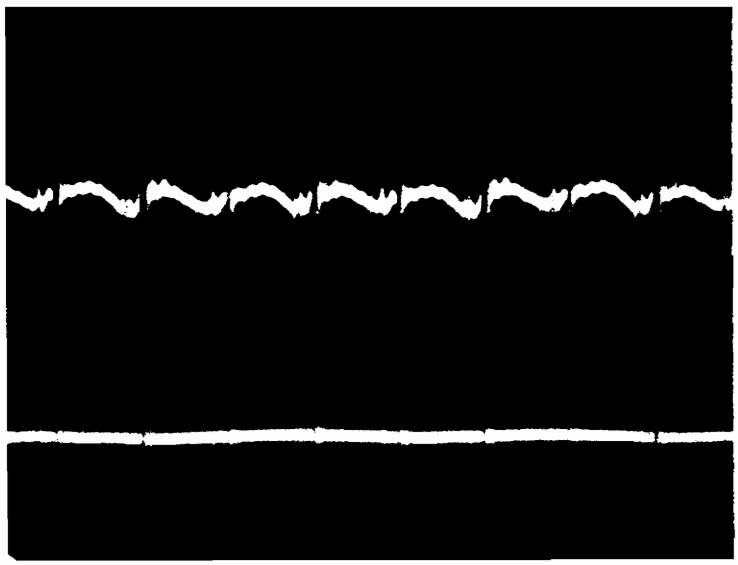


Figure 3.7. Input Filter Transfer Function

SUMMING JUNCTION
RIPPLE VOLTAGE



BUS VOLTAGE RIPPLE

.1 V/DIV

5 us/DIV

Figure 3.8. Bus Voltage Ripple

Figure 3.8. Bus Voltage Ripple

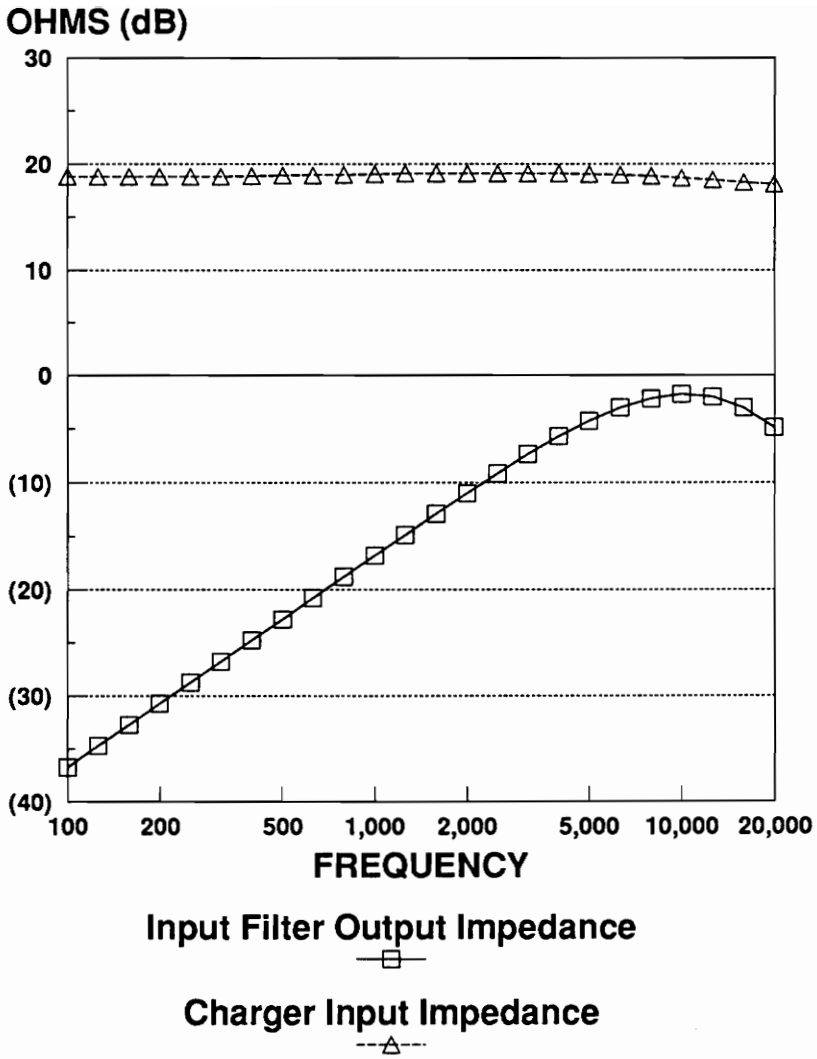


Figure 3.9. Input Filter Output Impedance and Charger Input Impedance

3.6 Summary

The battery charger power stage design has been presented. It has been shown that input and output ripple specifications have been met and exceeded.

The power stage was designed with efficiency and low weight as the main criteria. The power stage efficiency was measured at several battery voltage and charge current levels. A plot of this efficiency data can be found in Fig. 3.10. It can be seen that the worst case efficiency occurs at minimum battery voltage and maximum charge current. The efficiency under these conditions is 97%. This efficiency measurement does not include the control circuitry; however, the control circuit consumes less that 1W and is therefore negligible.

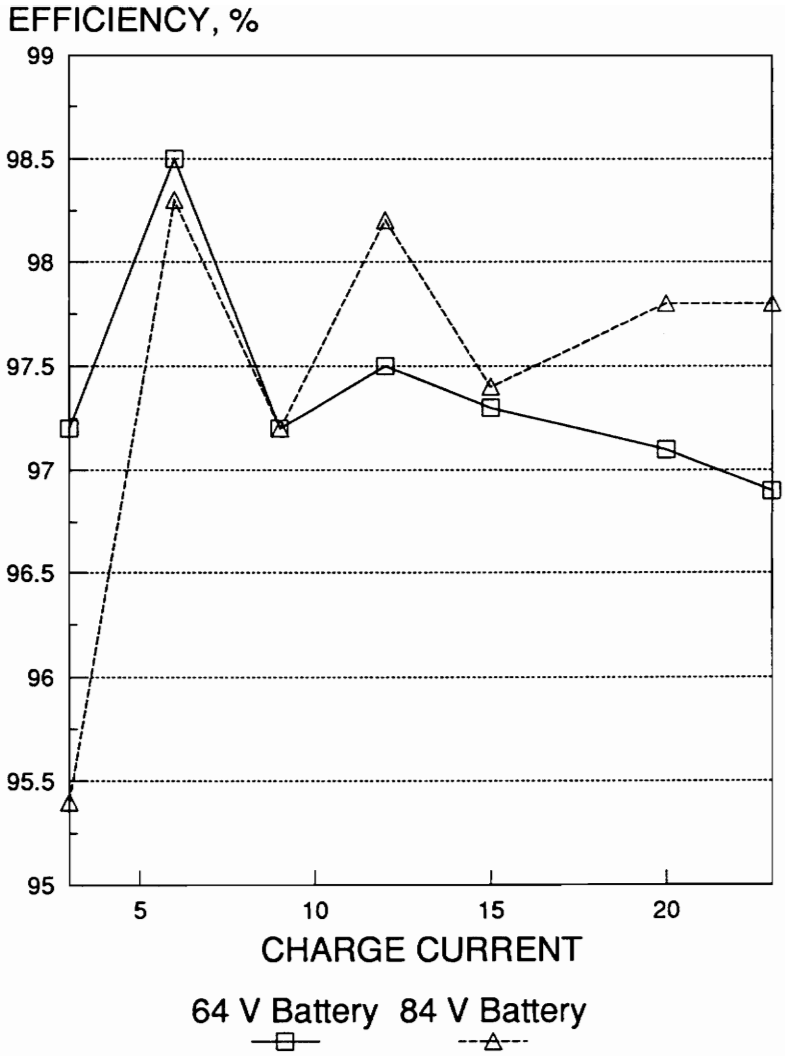


Figure 3.10. Power Stage Efficiency

4. Control System Design

4.1 Introduction

This chapter will describe the modelling and design of the battery charger's control loops. The battery charger has three separate control loops to regulate its operation during the various system modes. The control system block diagram is shown in Fig. 4.1. Each control loop is diode ORed together, producing the error signal, v_c. The charge is controlled by one loop at a time which determines the mode of operation.

During the time when the solar array is providing enough power to supply the spacecraft load and charge the batteries, the charger operates in the charge regulation mode. The charger will stay in the charge regulation mode until the battery voltage or temperature reach a programmable limit, at which time the charge cuts back on the charge current. This mode is the Volt/Temperature (V/T) limit mode of operation.

As the spacecraft is leaving (or entering) eclipse, the solar array cannot provide enough power to supply the load and charge the batteries to the full commanded level. During this time the charger operates in the bus regulation mode. The bus voltage is regulated by controlling the charge current. As solar array power increases charge, current is increased, until eventually the commanded charge rate is reached. The bus regulation error amplifier (E/A) becomes saturated, and the charge regulation loop takes over.

The battery charger provides an interesting and challenging system from a control point of view. As will be seen in the following sections the battery charger behaves quit differently from the standard buck topology converter. In fact, in the bus regulation

mode, the charger looks like a boost converter in the small signal sense, except the charger has a LHP zero. The characteristics of the load (the battery) and the source (the bus) also contribute to the complexity of the battery charger control loop design.

This thesis work has been performed with a solar array simulator that accurately simulates both the small and large signal characteristics of a solar array. This solar array simulator as well as the battery simulator that was used in all testing has facilitated the realistic comparison of test data with modeling data.

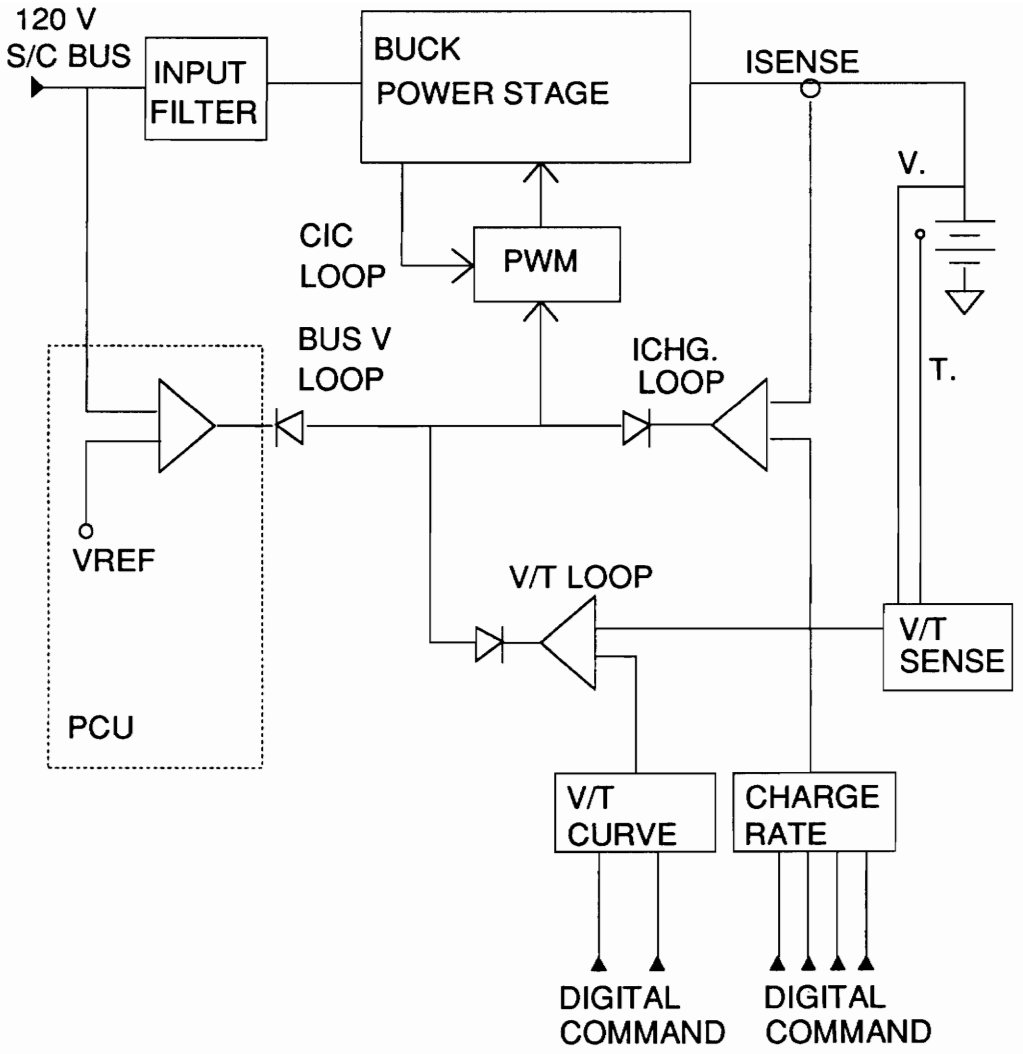


Figure 4.1 Charger Block Diagram

4.2 Current Sensing

It is obvious that for the battery charger to regulate battery charge current, an effective technique of measuring the current supplied to the battery must be developed. This method must be reliable, efficient, and accurate. Several options were investigated in order to determine the best technique.

The first and possibly most obvious option is the meter shunt technique. Using this method a precision resistor is inserted into the charge current path, and the voltage across it is measured to provide current information. Due to the nature of the mechanical design of the batteries, NASA informed us that it would not be possible to place a meter shunt in the battery ground lead, and therefore it would have to be placed in the high side of the battery. This would necessitate sensing an extremely low voltage at the relatively high battery potential. Although difficult, circuitry could be designed to sense this voltage. This method, however, suffers a severe weight penalty due to the relatively heavy meter shunt: the meter shunt investigated had a weight of 12 oz. The weight issue, coupled with the relatively complex instrumentation necessary to cleanly sense the voltage level, and the distasteful idea of intentionally placing a resistance in a high current path, caused this method to be rejected.

Another technique for sensing dc current is to use a Hall effect device. Hall effect devices are very simple to use and are available with instrumentation circuitry inside the package to provide an amplified signal to the user. Data was taken to determine the usefulness of the Hall effect device in this application. Data to determine the linearity of the device is shown in Figure 4.2. From the curve it can be seen that the Hall Effect device is linear between approximately three amperes to the maximum charge current of 23 A. The device is highly non-linear at the low current range of 0 to 3 A. The output

of the Hall Effect device is also temperature dependent. The gain shift for a standard flight approved device is 0.02%/ °C, in addition, the null offset shift is also 0.02%/°C. For the given application, a space environment, a 100 °C temperature range is not unusual. This would mean a worst case temperature drift of 4% of full scale. This error was considered too high to be acceptable.

The third technique investigated was the dual current transformer method. A schematic of the dual current transformer (DCT) is shown in Figure 4.3. The charge current is simply the sum of each individual modules inductor current. Similarly, inductor current is the sum of switch current and diode current; so to get an accurate representation of charge current, the switch and inductor currents from all four modules can be summed together.

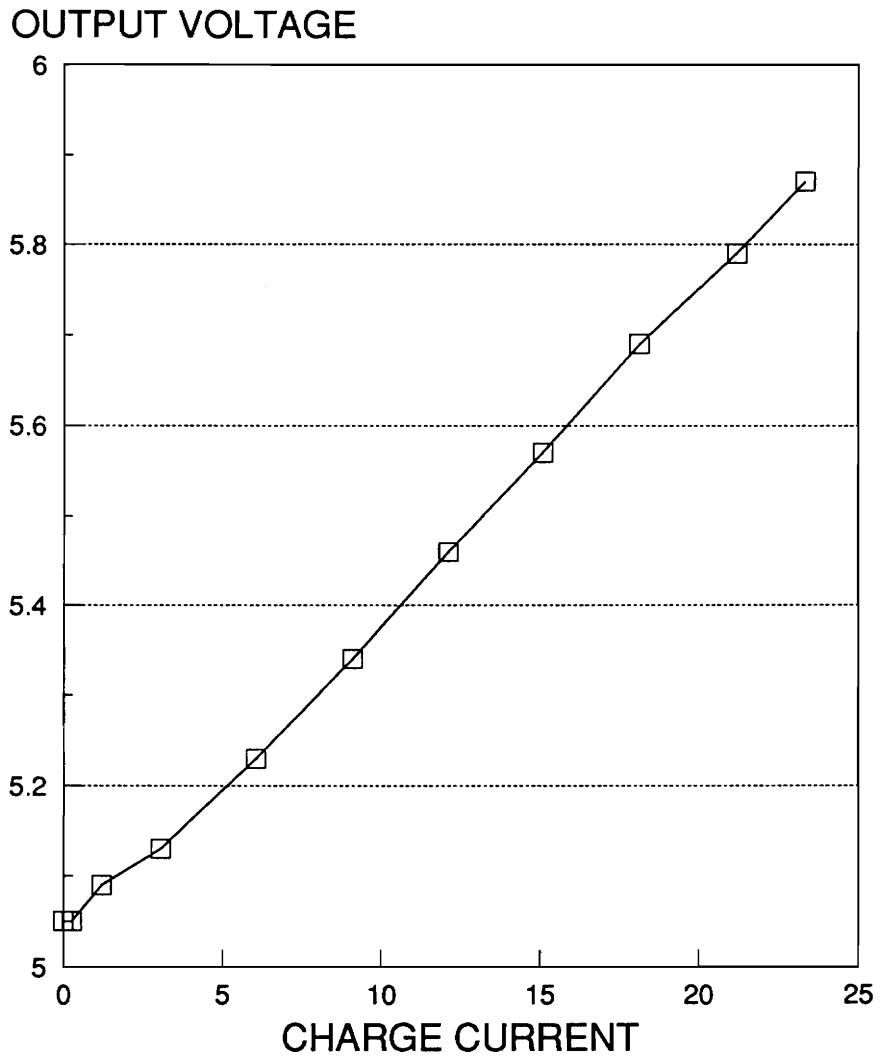


Figure 4.2 Hall Effect Device Data

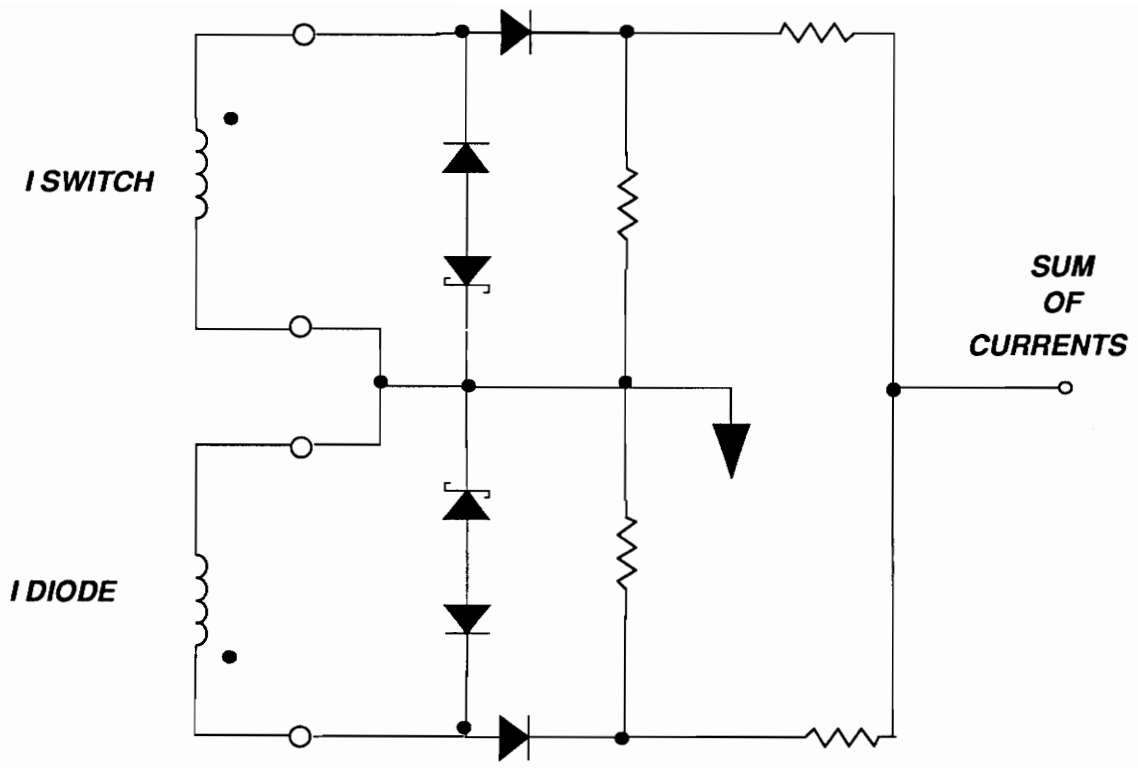


Figure 4.3 Dual Transformer Schematic

Current transformers are placed in series with both the diode and switch. Since a current transformer is needed on each switch to implement CIC, this requires four additional transformers. These transformers are very small and light-weight, so the penalty is very slight. The transformer design is developed in Section 4.1.4. The current from the transformers is summed through a resistor network to provide the dc charge current information. The parallel zener diodes are to reset each core during its OFF time; however, in practice these diodes were not required since the cores easily reset through the series diodes.

Data was taken to determine the linearity of the DCT method. This data can be found in Fig. 4.4. It can be seen that the DCT provides an accurate and linear representation of charge current. At low current levels, the DCT becomes nonlinear, but this occurs at approximately 1 A, vs. 3 A for the Hall Effect device. This nonlinearity is due to the presence of noise on the sensed waveform. This noise occurs at the transition between the MOSFET and the diode conducting. At low charge levels the noise becomes a greater percentage of the sensed waveform. This error, however, is within acceptable levels. A picture of the sensed current waveform can be found in Fig. 4.5. It can be seen that the waveform is fairly clean with a ripple frequency of 180 KHz. This is due to the multi-module nature of the charger.

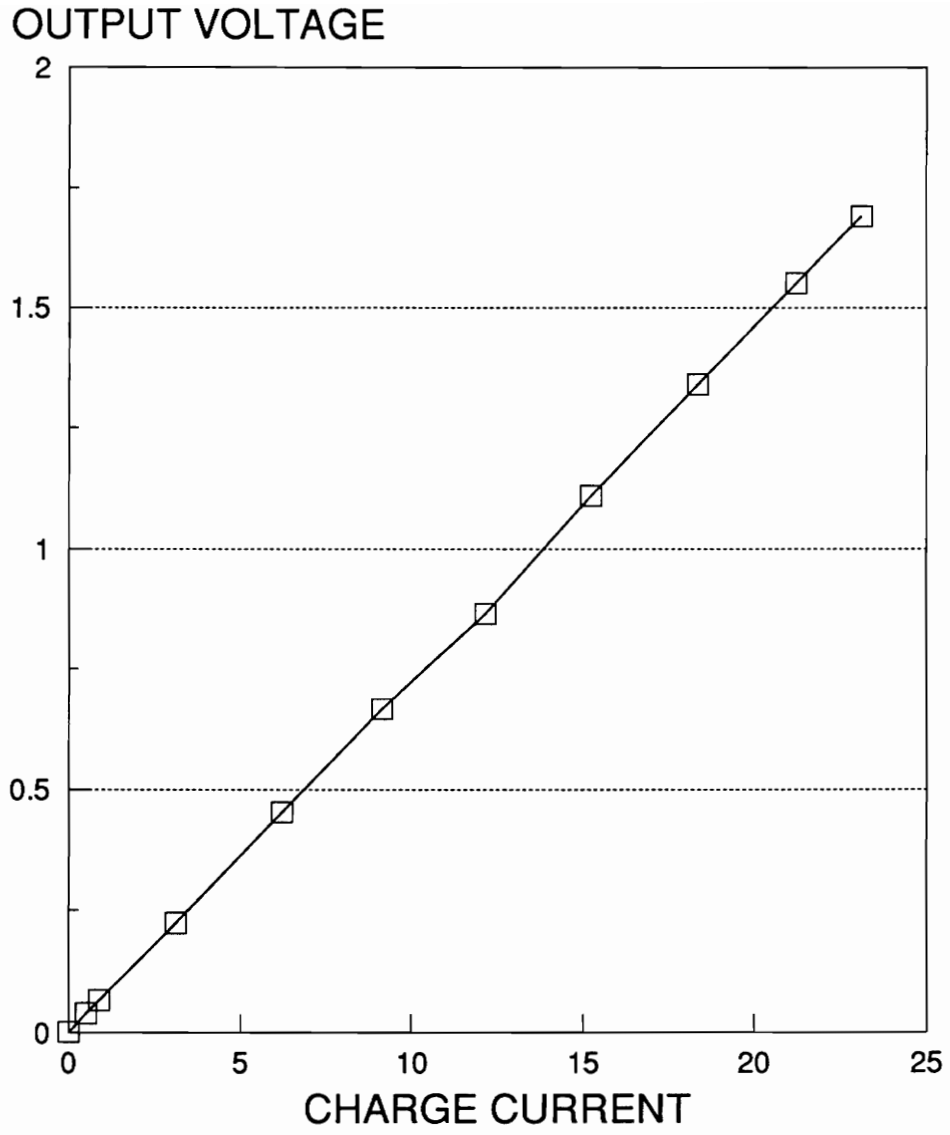
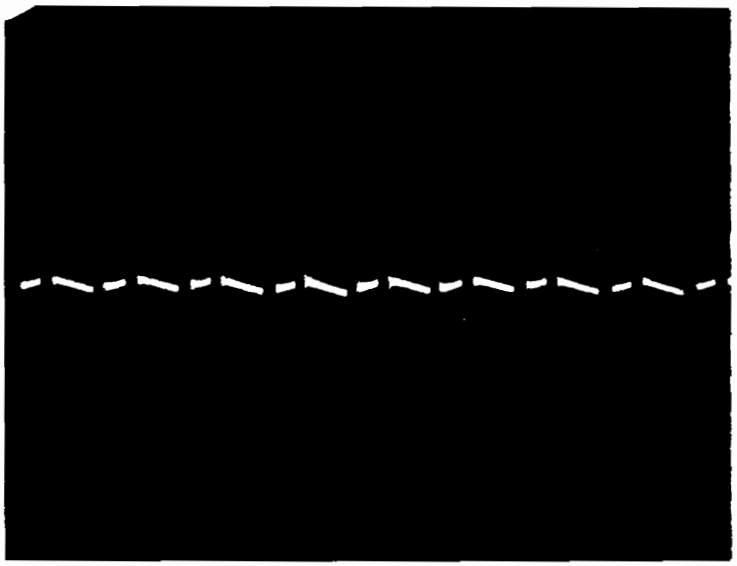


Figure 4.4 Dual Transformer Data



5 mA/DIV

5 us/DIV

Figure 4.5 Sensed Charge Current

The DCT method provides isolation between the sensed current and the control circuitry, is not temperature dependant, and provides good resolution. The disadvantage of the DCT method is the increased part count due to the four extra current transformers and the summing resistors. The increased part count, however, is not significant and is outweighed by the advantages. For these reasons it was decided to use the DCT technique to measure battery charge current.

4.3 Charge Rate Control

The battery charger must be capable of charging the battery at several commandable charge rates. Sixteen programmable charge rates are required corresponding to charge currents between trickle charge of .85 A to full charge of 23 A.

The charge rate control circuitry is designed to operate either from computer command or from a manual command. The charger is normally operated in the computer control mode, but to facilitate testing and trouble shooting, the manual mode is necessary. The charge command circuitry is shown in Fig. 4.6. The switch SW2 enables either U24 or U25. When U24 is enabled, U25 is placed in its high impedance mode, and the system is in the manual mode with commands accepted from SW1 and not the computer. Alternatively, in the automatic mode, the system only "sees" commands from the computer.

The charge current reference circuitry is found in Fig. 4.7. Resistors R93 through R98 are configured in the R, 2R, 4R, 8R sequence to provide the 16 commandable levels. Resistors R89 through R92 are required to provide the biasing needed for trickle charge. If the lowest charge current required was 0 A, this biasing would not be needed.

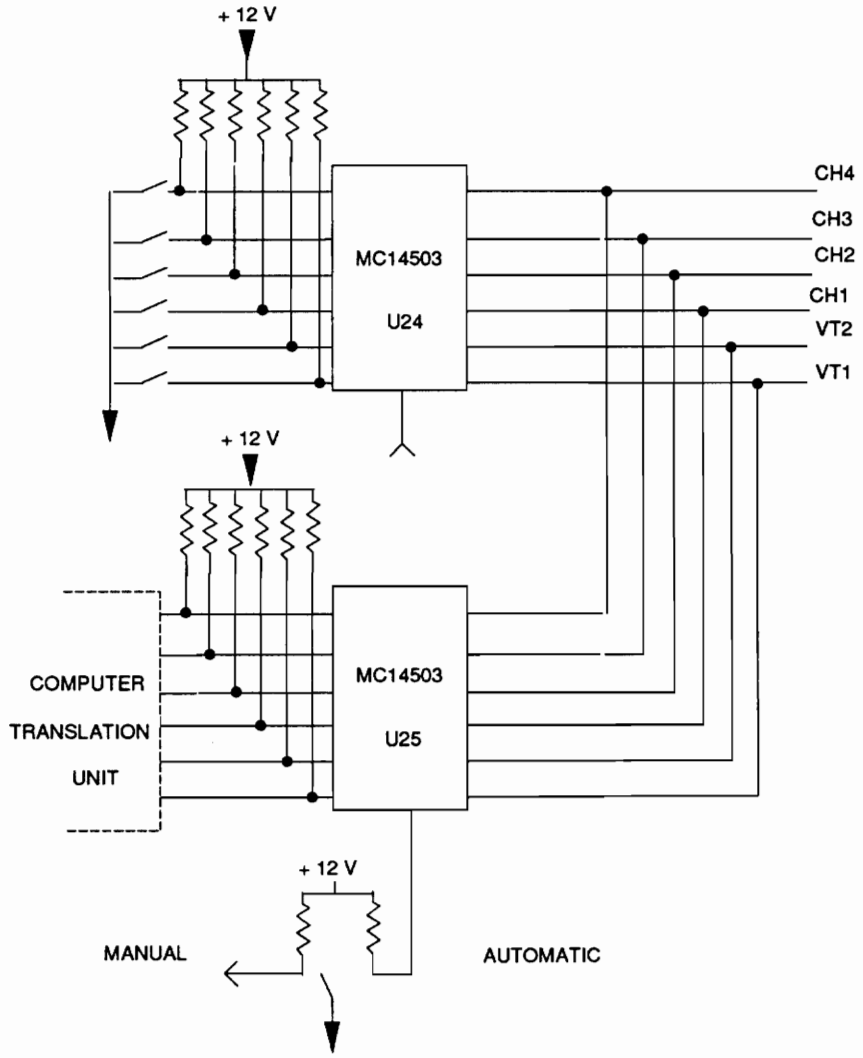


Figure 4.6 Digital Command Circuitry

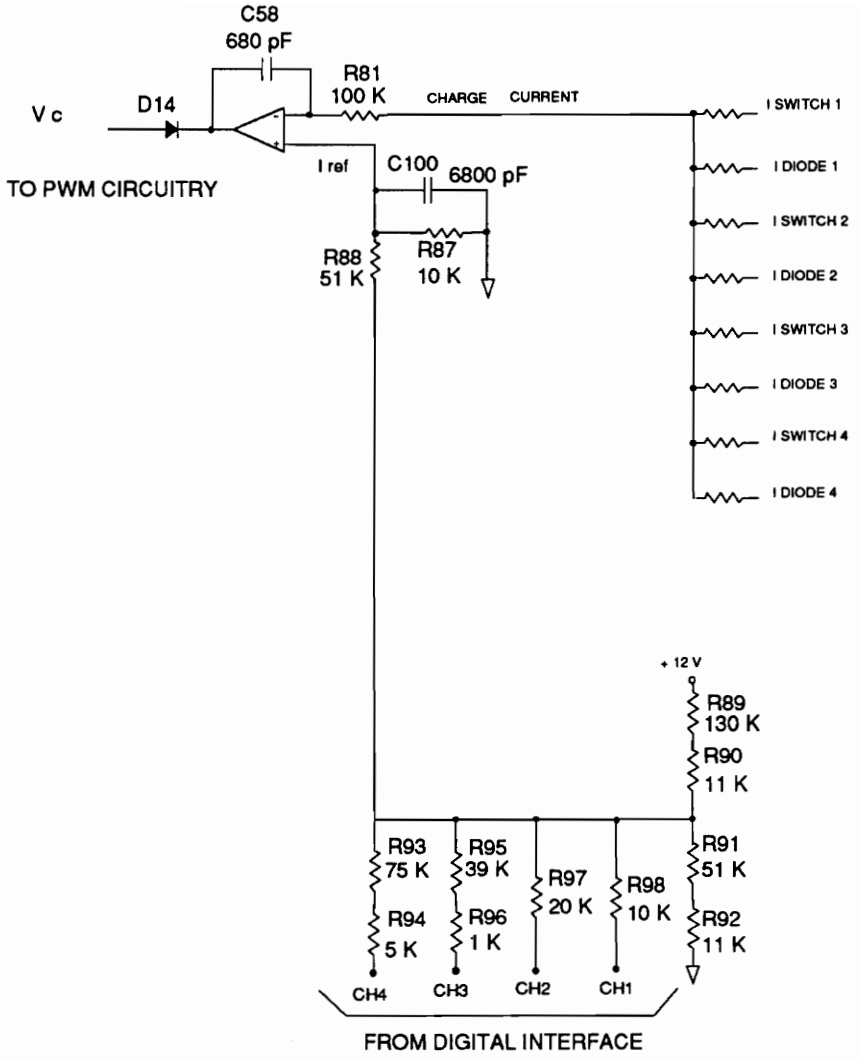


Figure 4.7 Charge Mode Control Circuitry

In order to provide flexibility in testing and to allow the use of different current sense methods (which require different reference voltages for the same required charge current) it was decided to provide a wide reference voltage range and then divide this voltage down through resistors R87 and R88 to the required value. The reference voltage range was picked to be 0.4 V to 10.0 V. If the series combination of R89 and R90 is designated Rt, and the combination of R91 and R92 Rb, then two equations can be written relating reference voltage and resistor value.

When the trickle charge rate is required, the four bit digital word will consist of all 0's. This will pull resistors R93 to R98 to ground. These resistors will then be in parallel with Rb. If the parallel combination of R3 through R98 is called Rx, this leads to the equation:

$$V_{ref} = 12V \frac{Rx//Rb}{(Rx//Rb)+Rt}. \tag{4.1}$$

When the maximum charge current is required, the digital word will be all 1's. This places R93 through R98 in parallel with Rt. This leads to the equation:

$$V_{ref} = 12V \frac{Rb}{(Rx//Rt)+Rt}, \tag{4.2}$$

where $Rx = 5.33 \quad K\Omega.$

Solving these two equations in two unknowns leads to:

$$Rt = 141 \quad K\Omega,$$

$$Rb = 61 \quad K\Omega.$$

To get the required reference voltage for the dual transformer method of current sensing, the reference voltage is divided down by a factor of 0.16. This is accomplished with resistor R88 = 51 K Ω and R87 = 10 K Ω. Capacitor C100 is added to filter any noise from the reference signal.

The charge rates and the measured values are shown in Table 4.1. The goal was to be within 2% of full scale battery charge current. This corresponds to a maximum current error of 0.460 A. It can be seen from Table 1 this specification was met.

Table 4.1. Charge Current Regulation

Charge Rate	Commanded Current (A)	Measured Current (A)	Current Error (A)
0000	.850	.430	.42
0001	2.33	2.12	.21
0010	3.80	3.61	.19
0011	5.28	5.08	.20
0100	6.76	6.51	.25
0101	8.23	7.98	.25
0110	9.71	9.47	.24
0111	11.19	10.93	.26
1000	12.66	12.41	.25
1001	14.14	13.87	.27
1010	15.62	15.37	.25
1011	17.09	16.84	.25
1100	18.57	18.29	.28
1101	20.05	19.76	.29
1110	21.52	21.27	.25
1111	23.00	22.75	.25

4.4 Small Signal Modeling

In order to facilitate control loop design, a small signal model of the battery charger is required. In the charge regulation mode, the small signal model can rather easily be derived due to the nature of the load and source. The charger operates in both the continuous and discontinuous conduction modes. Due to the low DCM boundary, the charger only operates in DCM during trickle charge. The DCM model, however, must be analyzed to ensure stability.

4.4.1 Continuous Conduction Mode

As was discused earlier, the charger operates mainly in the CCM region. The small signal model of the charger in CCM can be seen in Fig. 4.8. The PWM switch model [7] is used to develop the model. The PWM switch model lends itself nicely to deriving the required transfer functions.

In the charge regulation mode, the solar array is suppling both charge current and load current. The solar array is in the current source region of operation, and the shunt switching unit is regulating the bus voltage. The bus therefore is a "stiff" voltage source and from a small signal point of view looks like a short. On the output side of the charger is the battery. Again, from a small signal point of view, the battery looks like a short with a series resistance associated with it. The resistance of the battery is approximately 2 mΩ / cell with a total of 50 cells in series for a total ac resistance of .1 Ω.

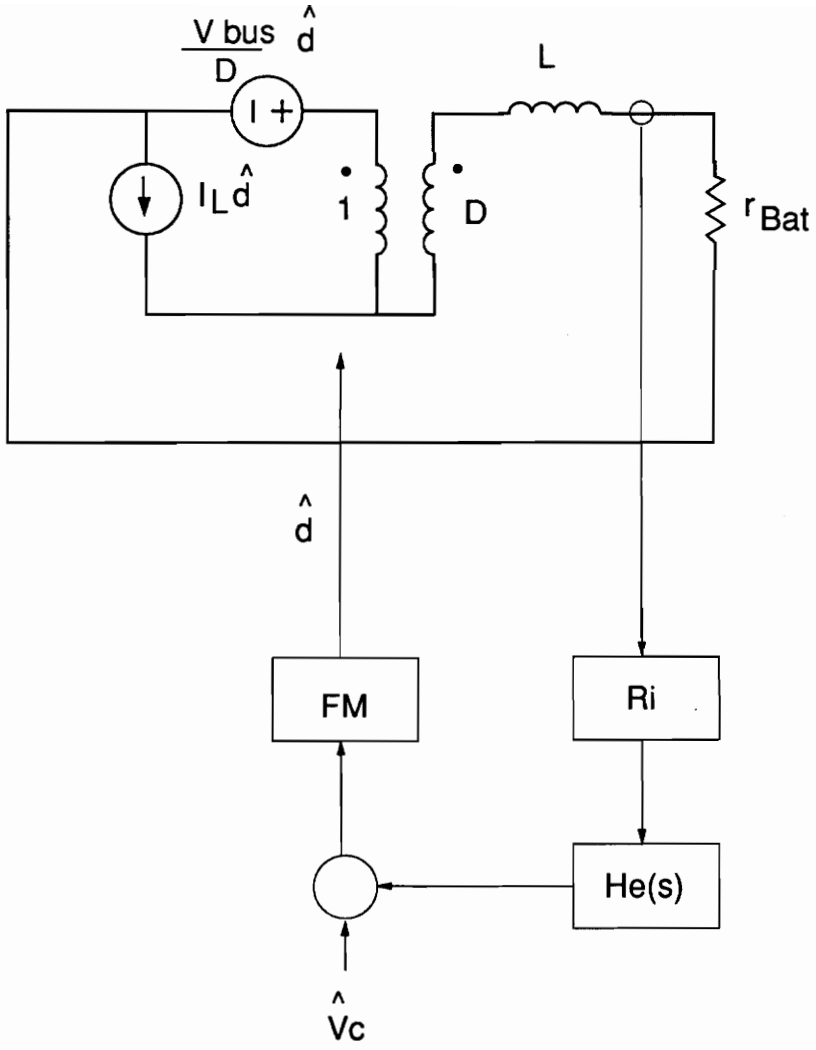


Figure 4.8 Small-Signal Model in Charge Regulation Mode

The transfer function (T.F.) of interest is the control to charge current T.F.. In order to derive this T.F., first the duty cycle to charge current T.F. must be derived, and the single module equivalent of the multi-module converter must be found. It has been shown in [8] and [9] that a multi-module converter has an equivalent single module small signal T.F.. The procedure is very simple and straightforward. The inductor values are divided by the number of modules: since the output capacitors are shared by all modules, no reduction is required. The current loop gain, H_i, must also be reduced by the number of modules. This is due to the fact that the inductors have been divided by four, and therefore to maintain the same gain/current relationship, H_i, must be compensated.

The duty-cycle to charge current T.F. can be derived by writing the equation governing inductor current:

$$i_L = \frac{\frac{V_{BUS}}{D} \cdot \hat{d} \cdot D}{R_l + R_{BAT} + sL}. \tag{4.3}$$

If we recognize that R_{BAT} is much greater than R_l we can simplify the T.F.:

$$F_{id} = \frac{\hat{i}_L}{\hat{d}} = \left(\frac{V_{BUS}}{R_{BAT}}\right) \frac{1}{1 + \left(\frac{L}{R_{BAT}}\right)s}. \tag{4.4}$$

This is a first order T.F.. With the equivalent single module inductance of 78 μH and R_{BAT} = .1 Ω, the T.F. has a pole at approximately 200 Hz. By inspection the control, to charge current T.F with the inner current loop (CIC loop) closed, is:

$$G_{ic} = \frac{\hat{i}_l}{\hat{v}_c} = \frac{F_m F_{id}}{1 + F_m F_{id} R_i He(s)}. \tag{4.5}$$

where as was shown in [10]:

$$F_m = \frac{1}{(S_n + S_e)T_s}.$$

S_n is the slope of the sensed inductor current, and S_e is the external ramp slope.

R_i is the current sense network gain, and He(s) is the high-frequency sampling effect discussed in [10]:

$$He(s) = 1 + \frac{s}{\omega_n Q_z} + \frac{s^2}{\omega_n^2}, \tag{4.6}$$

where

$$\omega_n = \frac{\pi}{T_s}$$

and

$$Q_z = \frac{-2}{\pi}$$

From Eq 4.5, the benefits of current mode control can be seen. As long as:

$$F_m F_{id} R_i He(s) \gg 1$$

which is true up to one-half the switching, the control to charge current T.F. reduces to:

$$F_{id} = \frac{1}{R_i He(s)}$$

This shows that the charger loop gain is immune to bus voltage variations, battery voltage, or battery resistance variations, or changes in charge current levels. In addition this T.F. is quite simple. It is a constant term with a gain of $1/R_i$ up until one-half the switching frequency. At one-half the switching frequency, the sampling effect becomes evident, and the behavior is determined by the design of the CIC loop. Before proceeding with the numerical analysis of the charge regulation loop, the CIC loop must be designed. In order to complete the modeling, however, the DCM transfer functions will be developed in the following section.

4.4.2 Discontinuous Conduction Mode

As was stated previously, due to the power stage design, the charger only operates in DCM during trickle charge. Even though the charger is operating at low power level during this time, it is equally important that the system is stable.

The battery charger in DCM exhibits the same type of behavior as a buck converter. The duty cycle becomes load dependant. The transfer functions of interest were derived in [11]. The charge current to duty cycle T.F. is given by:

$$F_{id} = \frac{\hat{i_L}}{\hat{d}} = \frac{2I_L}{D} \frac{1}{1 + \frac{s}{\omega_p}}, \tag{4.7}$$

where

$$D = \sqrt{(\frac{1}{M} - 1)\frac{I_L}{2LF_sV_{BUS}}},$$

$$M \equiv \frac{I_{in}}{I_L} = \frac{V_{BAT}}{V_{BUS}},$$

and

$$\omega_p = \frac{(1-M)V_{BAT}}{I_L L}.$$

Since the discontinuous case only occurs in trickle charge, the value of the battery voltage is known: it is at its maximum value of 84 V. Recalling that the inductance at this low current is 516 μh, the minimum value of the pole is 36.6 KHz. This is beyond 1/2 F_s. For all practical purposes, the T.F. looks like a constant with a dc gain of 40 dB.

4.5 Design of CIC Loop

The design of the CIC loop is one of the most critical design parameters. Proper design of the loop ensures the advantages of current mode control (CMC) without the problems of instability sometimes seen in systems employing CMC [10].

In a MMMP system, CIC is required to ensure current sharing between the modules. In addition, multi-loop control provides system dynamic benefits as was seen in the charge regulation mode. The CIC loop consists of a current transformer (CT) that senses switch current, and a ramp generator. The switch current and ramp are summed together to provide ramp compensation of the CIC signal. The CIC loop circuitry can be seen in Fig. 4.9. The first step in designing the CIC loop is to design the CT and the related current sensing circuitry.

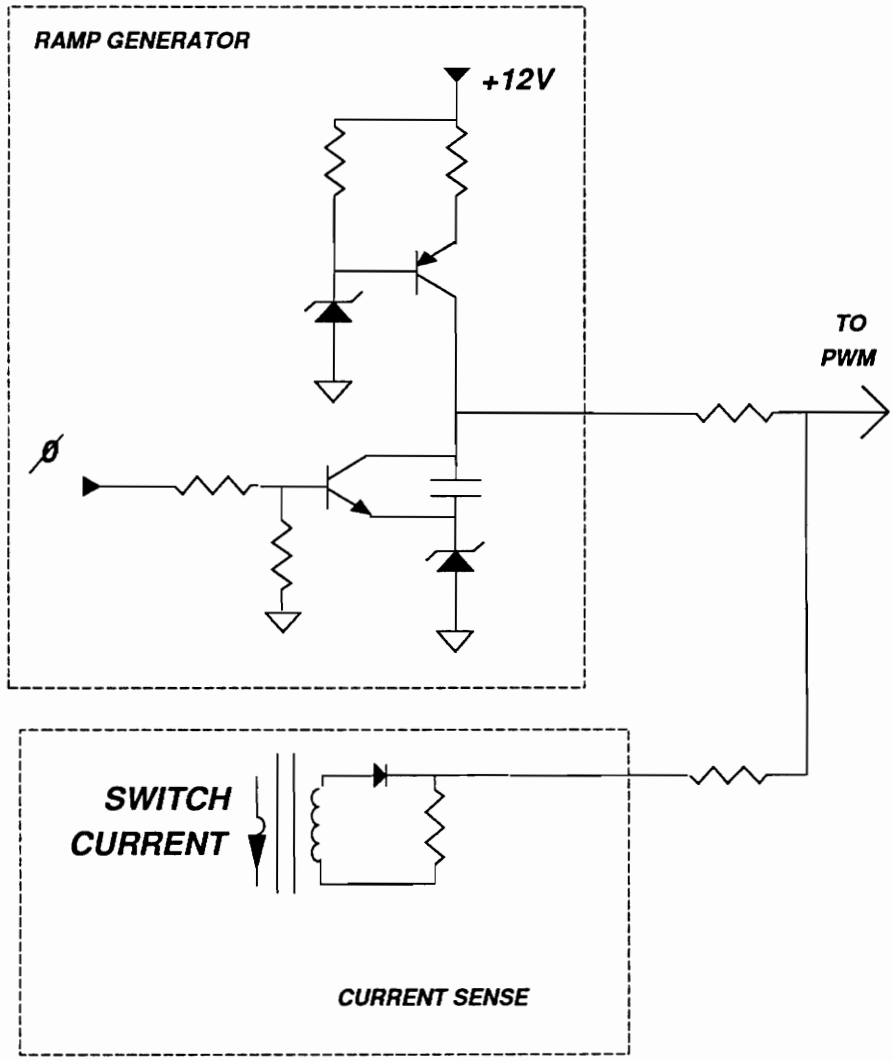


Figure 4.9 Current Injected Control Circuitry

In designing the current sense network, the main design constraint is power consumption. Normally a further constraint is the maximum input voltage range of the PWM circuitry. Due to the development of the discrete PWM circuit, this is not a significant limitation. To limit power dissipation in the current sense network, maximum power loss in one network will be limited to .160 W. This will keep total power loss for all four modules to less than 1 W. In addition, the maximum CT secondary voltage will be limited to 4 V at the maximum switch current of 6.8 A. These decisions lead to two equation in two unknowns that allow us to solve for the sense resistor:

$$I^2R = .160 \quad W,$$

$$IR = 4.0 \quad V.$$

Solving these two equations for R leads to :

$$R = 100 \quad \Omega.$$

also if R = 100 Ω then the transformer secondary current can be calculated:

$$I_S = \frac{4.0}{100} = 40 \quad mA$$

From here the number of turns can be found:

$$N_S = \frac{I_P N_P}{I_S} = \frac{6.8(1)}{40mA} = 170. \tag{4.8}$$

Now that the circuit values are known, the CT itself needs to be designed. The core material chosen is Supermalloy for its high permeability and low loss [12] wound core book] and the core geometry is a toroid. The maximum flux density of supermalloy is 6500 Gauss. To determine the size core needed, the required cross sectional area can be calculated [4]:

$$A_c = \frac{(V_o + V_D)10^4}{KB_m F_s N}, \tag{4.9}$$

where K = 4 (constant for square wave) and V_D = 0.7 V,

$$A_c = \frac{(4.0 + 0.7)10^4}{4(0.6TESLA)(45KHz)(170TURNS)} = 0.0256cm^2.$$

From the data available in [12] the closest core matching this size is the 50153. To ensure the windings will fit on this core, first the wire area (W_A) must be calculated, then compared to the available window area (A_e). For this application 28 AWG will be used. While a smaller area wire could handle the current, it would be more difficult to work with and in aerospace applications, it is generally not used for reliability reasons. 28 AWG has a cross sectional area of .507 cm^2; therefore the total area taken up by the wire is :

$$170TURNS \cdot \frac{.507cm^2}{1TURN} = .190cm^2.$$

The fill factor (K_W) is wire area divided by the available window area :

$$K_W = \frac{W_A}{A_e} = \frac{.190}{.507} = .376.$$

A fill factor of .376 is acceptable, and in fact, K_W should be kept below 0.5 for toroid cores. The next smaller core would require too large a fill factor.

Once the core is designed, the maximum operating flux density should be calculated to make sure the core will not saturate during operation:

$$B_{\max} = \frac{V_{on} 10^8}{4 F_S A_e N}, \tag{4.10}$$

$$= \frac{4(10^8)}{4(45KHz)(0.038cm^2)(170TURNS)} = 348 \quad G,$$

which is well below the saturating flux of 6500 G.

Recall that this CT is also used for current sensing. The magnetizing current (I_m) should now be calculated to ensure it does not cause any significant error in the charge current sense network. If the magnetizing inductance (L_m) is calculated, I_m can be found:

$$L_m = \frac{\mu N^2 A_e}{l_m},$$

where μ is the core permeability and l_m is the mean magnetic path length:

$$L_m = \frac{(20,000)(170^2 TURNS)(0.028cm^2)(0.4\pi 10^{-8} H/cm)}{3.49cm} = 79 \quad mH,$$

$$I_m = \frac{V_{on} T_{on}}{2L_m}, \tag{4.11}$$

where T_{on} is the maximum switch ON time and occurs at maximum battery voltage:

$$I_m = \frac{4(0.7 \cdot 22.2\mu s)}{2 \cdot 79mH} = 393 \quad \mu A.$$

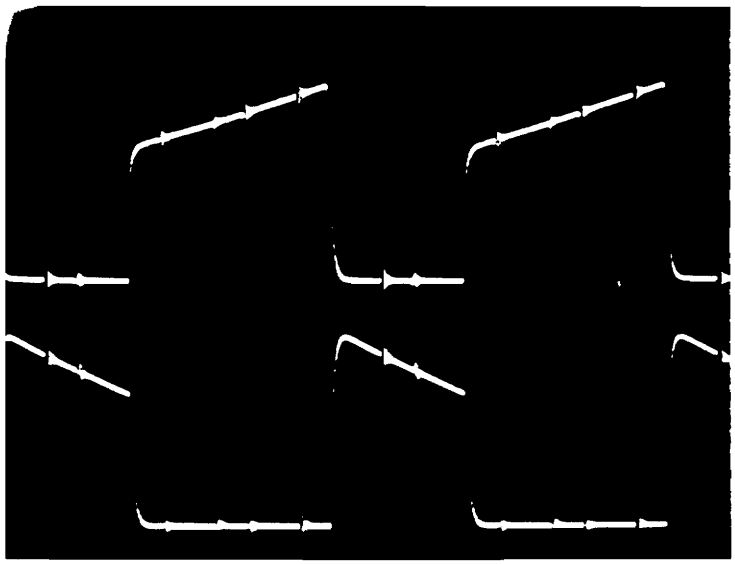
To calculate the percent error, the magnetizing current should be compared to the sensed current:

$$\%error = 100 \cdot \frac{.393mA}{40mA} = .89\%.$$

This error is less than 1% and is acceptable.

The core resets easily through the blocking diode, and no reset zener is required. To filter high-frequency noise spikes, a capacitor is added to the circuit in parallel with the sense resistor. This capacitor is 3300 pF, which with the 100 Ω resistor, gives a cut-off frequency of 482 Khz. This pole only filters high-frequency spikes and has no effect on the loop response. A picture of the switch and diode sensed current waveforms can be found in Fig. 4.10. It can be seen that the waveforms are quite clean.

The current sense circuit is one building block of the CIC loop. Another building block is the ramp generator circuitry. The ramp generator itself is a very simple circuit. The design procedure focuses on determining and then achieving the proper ramp slope.



1 A/DIV

5 us/DIV

Figure 4.10 Switch and Diode Current Waveforms

As was discussed in Section 3.3, the discrete PWM circuit allows for easy design of the ramp slope. The current value from the constant current generator as well as the capacitor need to be determined. These values are chosen to provide a certain ramp slope to compensate the CIC loop. It was developed in [10] to prevent instability in the current loop; an external ramp should be summed with the current sense signal such that:

$$m_c = 1 + \frac{S_e}{S_n} > 1, \tag{4.12}$$

where S_n is the slope of the inductor current, and S_e is the slope of the external ramp. The larger m_c is, the more damping of the sampling effect there is. For this design m_c was chosen to be approximately 2. In order to determine S_e, S_n must be calculated. The slope of the inductor current must be calculated as it is seen at the summing point with the ramp slope. Therefore the attenuation due to the summing network and the current sense network must be taken into consideration. The values of the summing resistors were found partly empirically. The values had to be large enough not to load the ramp or sense networks and therefore were initially picked to be 10 KΩ. To allow more ramp slope relative to the sensed current slope, a 4:1 increase in the relative weight of the ramp slope was chosen. This is done by the 11 KΩ and the 43 KΩ voltage divider:

$$S_n = \frac{\frac{\Delta i}{T}\frac{100\Omega(11K\Omega)}{11K\Omega+43K\Omega}}{\Delta t}, \tag{4.13}$$

where Δi=2.2 A, T=170, and worst case Δt is D_{min}*T_s. Therefore:

$$S_n = \left(\frac{2.2}{170}\right)\frac{(100)(.203)}{.533 \cdot 22.2\mu s} = 22.3 \quad K.$$

For m_c to be 2 or greater, the current generator must therefore be designed to have a ramp slope of 22.3 K. The ramp generator has a dead time of 25% of the period, and therefore the ramp period is:

$$.75 \cdot 22.2\mu s = 16.6 \quad \mu s.$$

The ramp slope is equal to the change in voltage divided by the ramp period. This allows us to find:

$$\Delta V = 22.3K \cdot 16.6\mu s = .371 \quad V.$$

Lastly, the constant current source was designed to provide approximately 500 μA to the capacitor. This leads to the equation for finding the capacitor value:

$$C = \frac{500\mu A \cdot 16.6\mu A}{.371V} = .02 \quad \mu F.$$

In the actual circuit, a .015 μF capacitor was required to get the proper ramp slope. The actual measured ramp slope was 28 K, which lead to an m_c of 2.25. This is quite acceptable, and in fact, it will be seen in the next section that good damping of the sampling effect was achieved.

4.6 Design of the Current Regulation Loop

The purpose of the current regulation loop is to regulate and maintain the commanded value of charge current to the battery. Of course this function must be carried out while ensuring that the charger is stable. In order to design the current regulation loop error amplifier (E.A.), the control to charge current T.F. must be evaluated. This T.F. was derived in Section 4.4 and can now be seen in Fig. 4.11. As was discused in that section, the T.F. is a constant with a gain of $1/R_i$. R_i can be found now that the CIC loop has been designed:

$$R_i = \frac{R_{sense}}{No.ofTurns} \cdot V_{DIVIDER} \cdot No.Modules, \tag{4.14}$$

$$= \frac{100}{170} \frac{11K\Omega}{11K\Omega + 43K\Omega} \cdot \frac{1}{4} = .03.$$

The sampling effect can be seen causing the gain to drop off, starting at approximately 5 KHz. It can be seen that the effect is very well damped. In fact, the complex poles have turned real and begun to split, one moving lower in frequency and the other higher. This causes the drop off in gain to occur before 1/2 F_s. It can also be seen that the charger is very easy to compensate in this mode.

In fact the charger can be compensated with a simple integrator providing zero steady-state error and good gain and phase margin. To design the E.A., a decision must be made as to where the loop gain cross over frequency should occur. By looking at the control-to-charge current transfer function, it can be seen that at approximately 6 KHz there is about 50° of phase margin with a gain of 28 dB. This then is a good choice for

the cross over frequency.

The charge regulation loop must therefore be designed to have a gain of -28 dB at 6 KHz. Figure 4.7 shows a schematic diagram of the E.A.. Due to the sensing network there is 22 dB attenuation between the actual charge current and the sensed current at the E.A.. This is easily verified by recalling that a reference voltage of 1.6 V is required to command 23 A of charge current. The E.A. should have a gain of -6 dB at 6 KHz. This translates to an E.A. cross over frequency (F_c) of 2.5 KHz. The equation of an integrator circuit is:

$$F_c = \frac{1}{2 \cdot \pi \cdot R \cdot C}.$$

Letting R = 100 KΩ, it is easily solved for C = 680 pF.

A bode plot of the charge current regulation loop gain is shown in Fig. 4.12. There is excellent correlation between theoretical and experimental results. It can be seen that the gain does cross 0 dB at approximately 6 Khz with better than 50° of phase margin.

A bode plot of loop gain with the charger in DCM is shown in Figure 4.13. There is some loss of gain in the discontinuous conduction mode of operation. The loop gain cross over frequency is reduced to about 1.2 KHz. Phase margin is increased to close to 90°.

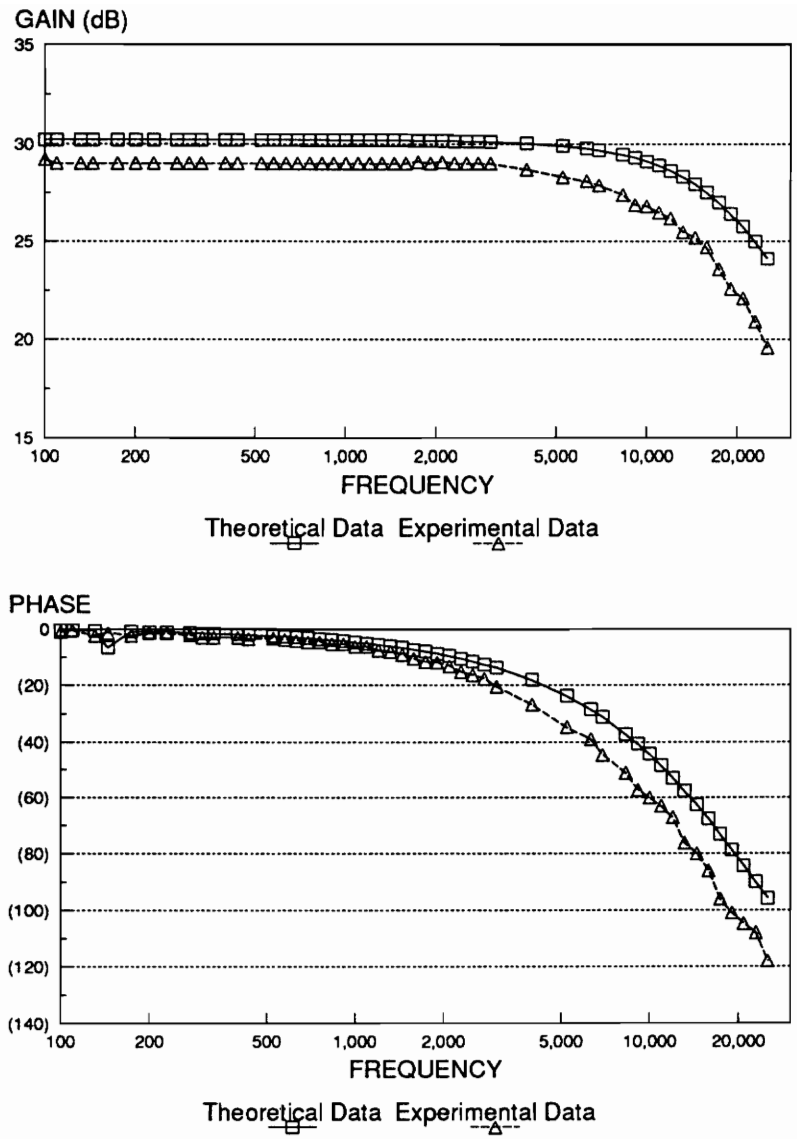
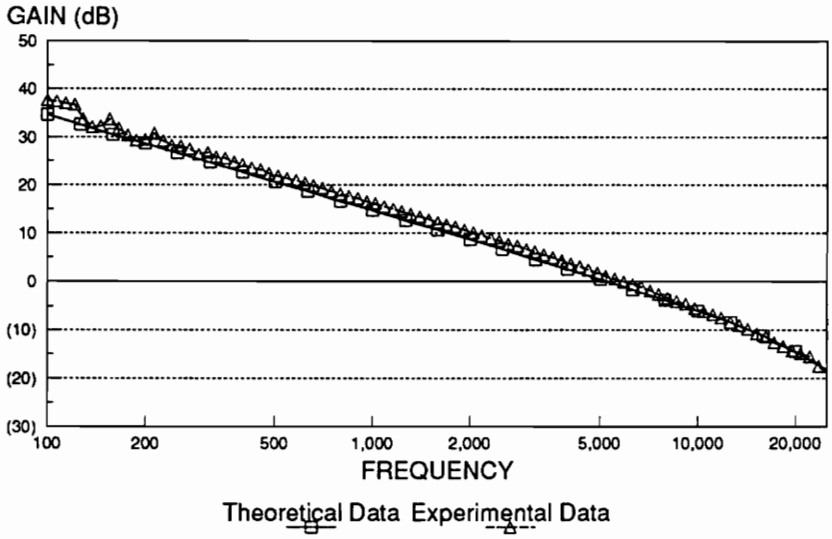


Figure 4.11 Control to Charge Current T.F. in CCM



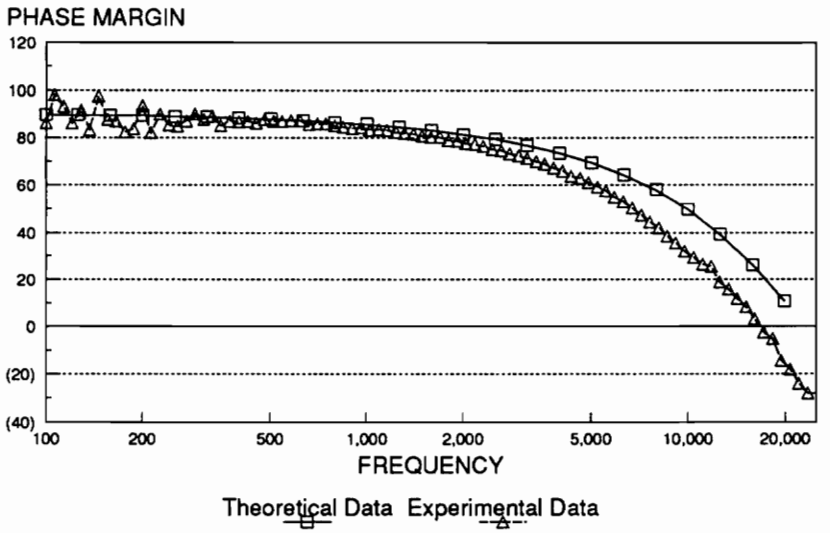


Figure 4.12 Charge Regulation Mode Loop Gain in CCM

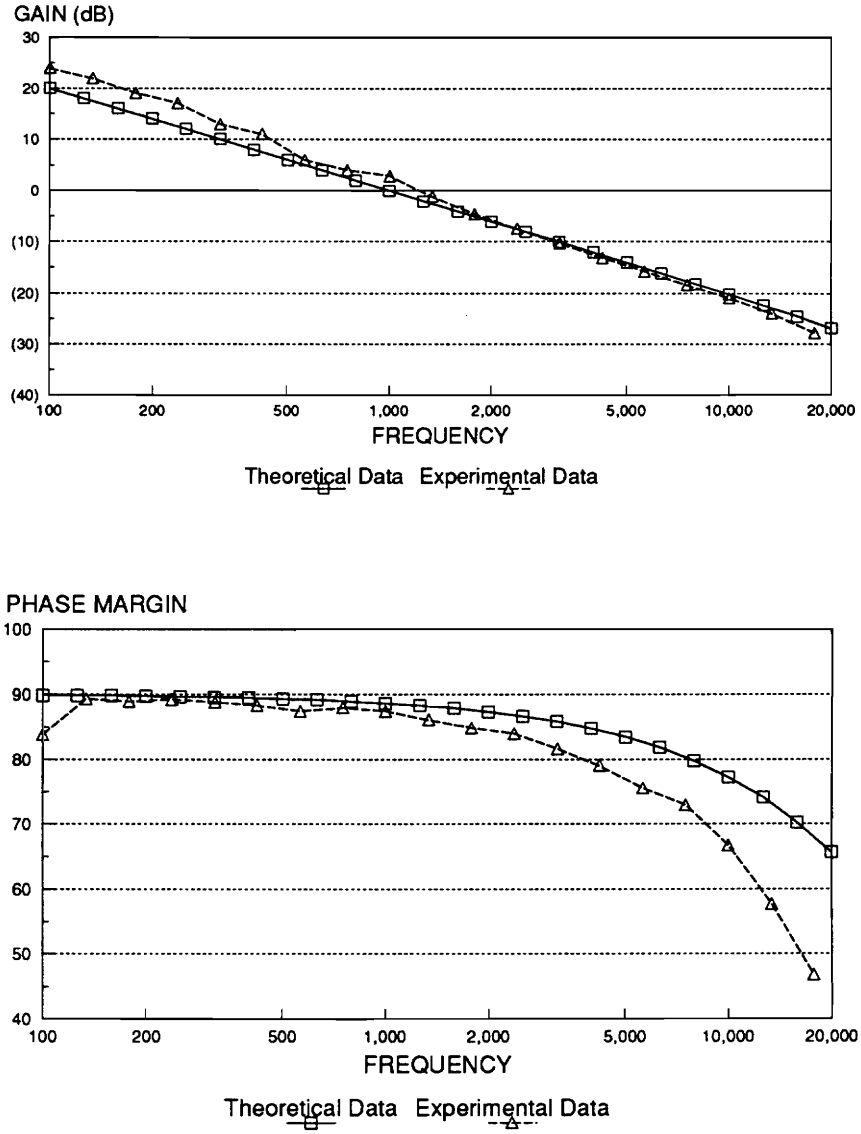


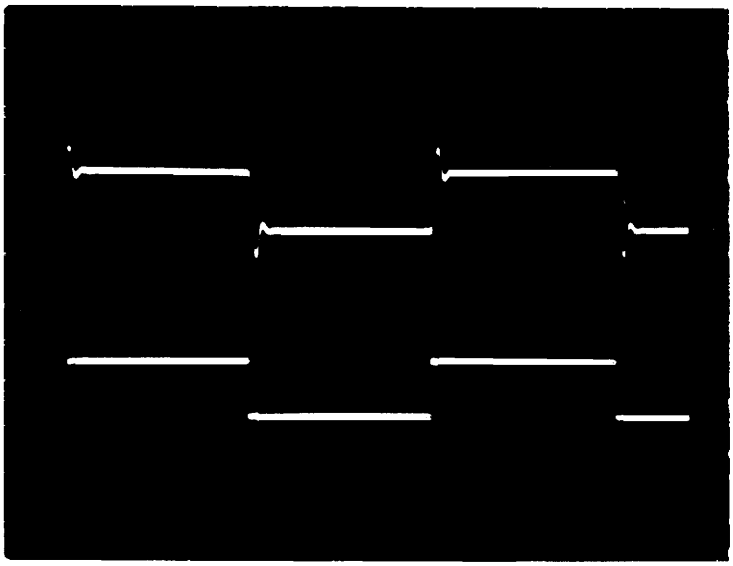
Figure 4.13 Charge Regulation Mode Loop Gain in DCM

4.7 Transint Response

Since the battery is a fixed source with a time constant much greater than the charger and the bus is being regulated by the shunt unit, the only realistic step change for the charge regulation loop is a change in commanded charge current.

The charge current reference is fed into the positive input of the current regulation loop error amplifier. Since the gain from the reference circuit to the charge current is 1 + R_f/R_i, any change in reference voltage is instantaneously translated to the output of the error amplifier. Since this would cause considerable overshoot and possibly oscillations within the loop, filtering of the reference signal is required. This filtering is accomplished quite simply by the addition of a capacitor across the reference voltage resistor divider. The addition of this capacitor is good practice anyway for noise filtering of the reference signal.

Experimental results of a step change in commanded current are shown in Fig. 4.14. The waveforms show both an increasing and decreasing current transition (a 1 A transition is commanded). The step change is the bottom waveform; the top waveform is the charge current. It can be seen that the current exhibits very little overshot (0.5 A) and has a settling time of approximately .4 ms. This settling time is primarily determined by the RC time constant of the reference circuit. The time constant of this circuit is 68 μs. This overshot and settling time are quite well behaved and in fact show the current loop to be stable. Since the battery has such a long time constant, the transient will not be "noticed" by the battery.



1 A/DIV

1 ms/DIV

Figure 4.14 Current Regulation Loop Transient Response

4.8 Bus Regulation Mode

As was previously discussed, during the time when the solar array is unable to supply both the load current and the commanded battery charge current, the charger maintains bus voltage by cutting back on charge current. During this time the charger is regulating bus voltage. From the charger point of view then, the bus voltage is now an output variable, while the battery voltage is an input variable. If the charger is visualized from this input/output point of view, it looks and behaves like a boost converter with reversed power flow. Adding to the complexity of the control design is the load characteristics. The charger load in bus regulation mode is quite complex and nonlinear [11].

4.9 Small Signal Modeling

4.9.1 Continuous Conduction Mode

Small-signal modeling of the charger in bus regulation mode (BRM) is facilitated by the model shown in Fig. 4.15. The figure shows the charger with the CIC loop closed. It has been shown [11] that the control to duty cycle T.F. is:

$$F_v = \frac{\hat{v}_{bus}}{\hat{d}} = \frac{\left(1+\frac{s}{\omega_z}\right)(1+sR_cC_{bus})}{\Delta(s)}, \tag{4.15}$$

where

$$\omega_z = \frac{V_{bat}}{I_L L},$$

$$\Delta(s) = \frac{s^2}{\omega_o^2} + \frac{s}{Q\omega_o} + 1,$$

and

$$\omega_o = \frac{D}{\sqrt{LC}} \quad , \qquad Q = \frac{1}{\omega_o\left(\frac{L}{D^2 r_{bus}} + C_{bus}R_c\right)}.$$

r_{bus} is the equivalent small-signal load resistance seen by the charger. The negative sign is due to the fact that an increase in duty cycle (D) causes a decrease in bus voltage. The T.F. has a LHP zero insted of the RHP zero in a conventional boost converter due to the reverse current flow. I_L is the sum of all four inductor currents or simply the charge current, and L is the equivalent multi-module inductance.

The control to charge current T.F. [11] is:

$$F_i = \frac{I_k}{D^2}\frac{\left(1 + s\frac{V_{bus}C_{bus}}{I_k}\right)}{\Delta(s)}, \tag{4.16}$$

where

$$I_k = \frac{V_{bus}}{r_{bus}} - DI_L. \tag{4.17}$$

Since r_{bus}, D, and I_L all change depending on load requirements and battery voltage, this zero moves considerably, and in fact it can become negative.

The current loop gain, T_i, by inspection is:

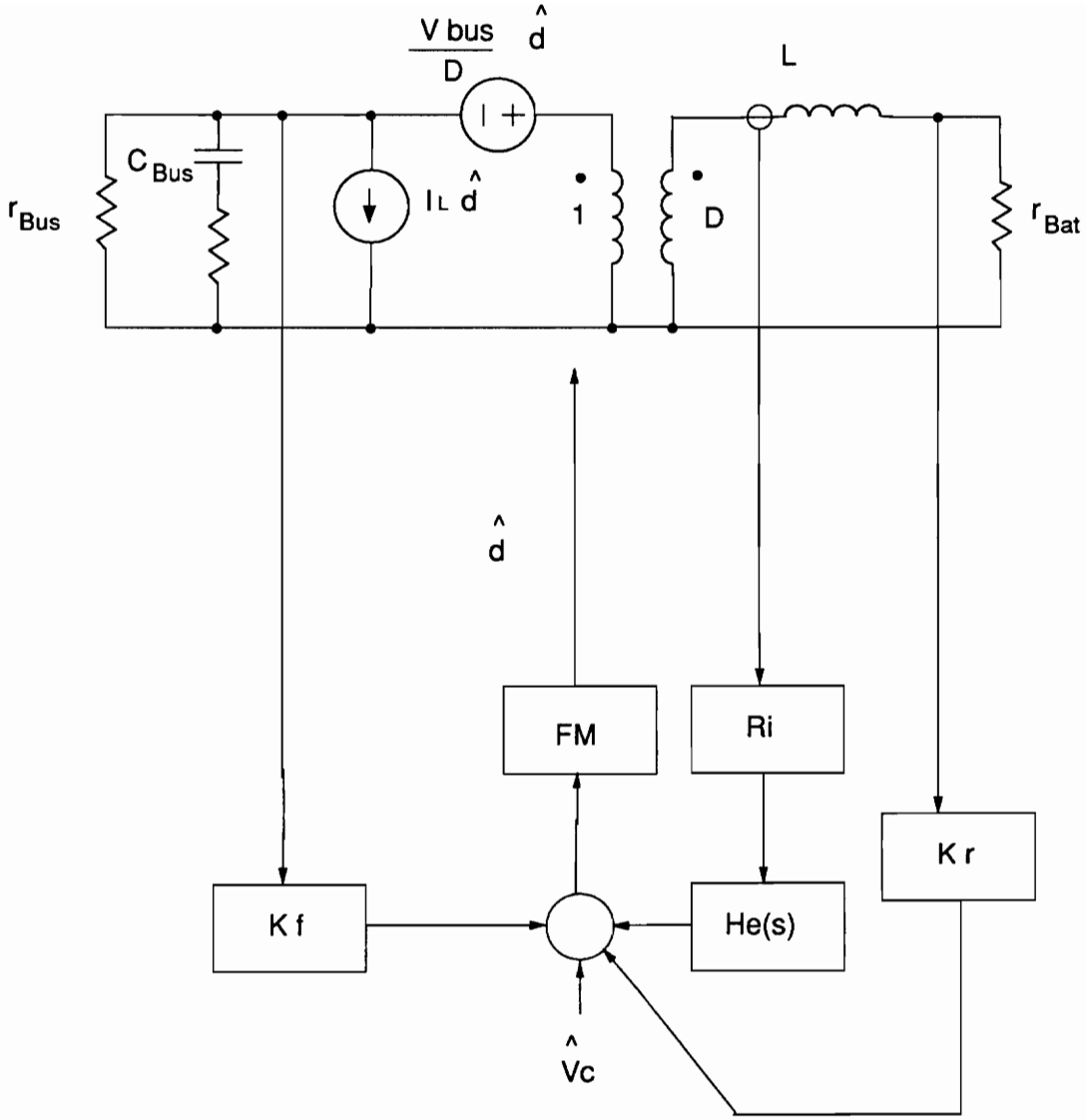


Figure 4.15 Small Signal Model for Bus Regulation Mode

$$T_i = F_m F_i R_i H_e(s),$$

$$= G_i \frac{\left(1+\frac{s}{\omega_i}\right) H_e(s)}{\Delta(s)}, \tag{4.18}$$

where

$$G_i = \frac{I_k}{D^2} F_m R_i,$$

and

$$\omega_i = \frac{I_k}{V_{bus} C_{bus}}.$$

Once the current loop is closed, the control to bus voltage T.F. becomes:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{F_m F_v}{1 + T_i - F_v K_f F_m}. \tag{4.19}$$

which can be simplified to:

$$\frac{\hat{v}_o}{\hat{v}_c} = \frac{\left(1+\frac{s}{\omega_z}\right)(1+sR_c C_{bus})}{\left(1+\frac{s}{\omega_x}\right)\left(1+\frac{s}{\omega_n Q_p}+\frac{s^2}{\omega_n^2}\right)}, \tag{4.20}$$

where

$$\omega_n = \frac{\pi}{T_s} \quad , \qquad Q_p = \frac{1}{\pi(m_c D' - 0.5)},$$

$$G_x = \frac{-F_m \frac{V_o}{D}}{1 + G_i + K_f F_m \frac{V_o}{D}},$$

and from [10]

$$K_f = -\frac{D T_s R_i}{L}\left(1 - \frac{D}{2}\right),$$

$$\omega_x \approx \frac{1 + G_i + K_f F_m \frac{V_{bus}}{D}}{\frac{1}{Q_o \omega_o} + \frac{G_i}{\omega_i}}.$$

In [11] a further approximation of ω_x is given relying on the fact that G_i is usually much greater than 1 and negative. This, however, may not be the case in a multi-module converter. Since R_i is reduced by the number of modules, this has the effect of reducing G_i. In this case G_i had a value of -.4 for a charge current of 10 A. Using the simplification could lead to large errors in evaluating the T.F.. In fact, in certain cases the simplification can lead to a pole appearing in the LHP, when in reality it was in the RHP.

The second order term in the denominator is due to the sampling effect. This effect is obviously only seen at 1/2 the switching frequency and beyond. Proper damping of the sampling effect removes any concern over its effect.

The dc gain of the control to bus voltage T.F. becomes negative since the denominator of G_x is negative.

Here we can see the potential problem with CIC control in the bus regulation mode. The RHP zero in the control to inductor current T.F. has become a RHP pole in the closed loop T.F. This would be expected, since it is the inductor current which is the control variable being fed back. It turns out, however, that the RHP pole is not a significant problem. The system has been analyzed in [11] and shown to be conditionally stable. The criteria for stability is that enough gain is in the feed back loop to maintain adequate phase margin.

It should also be noted that the pole can be either positive or negative and moves around depending on load current as well as charge current. The pole occurs at very low frequencies (< 10 Hz) and moves higher as charge current is increased.

4.9.2 Discontinuous Conduction Mode

Unlike in the charge regulation mode, where the charger can remain for an indefinite period of time in trickle charge and therefore in DCM, the charger will quickly move out of the DCM of operation in bus regulation mode. This is due to the low current required to move into CCM.

It has been shown in [10] that the current loop is not needed in the small signal model in DCM. Using the PWM switch model, it can be shown [11] that the control to output T.F. with CIC is:

$$\frac{\hat{v}_o}{\hat{v}_c} = F_m G_c \frac{\left(1+\frac{s}{\omega_z}\right)(1+sR_cC_{bus})}{\left(1+\frac{s}{\omega_{c1}}\right)\left(1+\frac{s}{\omega_{c2}}\right)}, \tag{4.21}$$

where with several approximations outlined in [11]:

$$G_c = -\frac{2V_{bus}(1-M)r_{bus}}{D\{R(1-M)+r_{bus}\}},$$

$$\omega_z = \frac{RM^2(1-M)}{L(1-M+2M^2)}$$

$$\omega_{c1} = \frac{RM^2\{R(1-M)+r_{bus}\}}{r_{bus}(1-M)(R^2C_{bus}M^2+L)+RL}.$$

The pole ω_{p1} is also a RHP pole at very low frequency as in the CCM case. The dc gain is positive and smaller than the CCM case.

4.10 Feedback Loop Design

In a complete power system there are two battery charger/discharger units as well as a shunt unit. Each of these systems regulate the bus to a given voltage. To determine which unit should be on, and more importantly that only one is on at a time, the power control unit (PCU) monitors bus voltage and sends control signals to each unit. A schematic diagram of the PCU can be found in Fig. 4.16.

The first amplifier U1 senses bus voltage and provides an error signal to the individual error amplifiers. U1 is designed for unity gain. The error signal is divided down through R5, 6, 7. This voltage divider provides a 1 V dead band between modes. This ensures that only one of the error amplifiers will be active at a time. The others will be saturated either high or low, depending on the bus condition.

The PCU is located with the bus capacitor, and the individual error signals are sent to the corresponding units. In the actual system the bus capacitor and PCU are located up to 20 feet away from the charger/discharger assemblies. To reduce noise and allow for the different ground potentials, the error signal is sent to a differential amplifier on the charger control board. The output of the differential amplifier is control voltage, v_c. Notice that the error signal is fed into the negative input of the amplifier. This gives a positive gain for the error signal. This is necessary in order to have an overall negative feedback gain due to the nonminimum phase nature of the system [11].

The PCU sends the error signal to both battery chargers. This has the effect of increasing the system gain by a factor of two. This can be explained by recognizing that this is similar to having eight modulaes in parallel instead of four. This reduces the

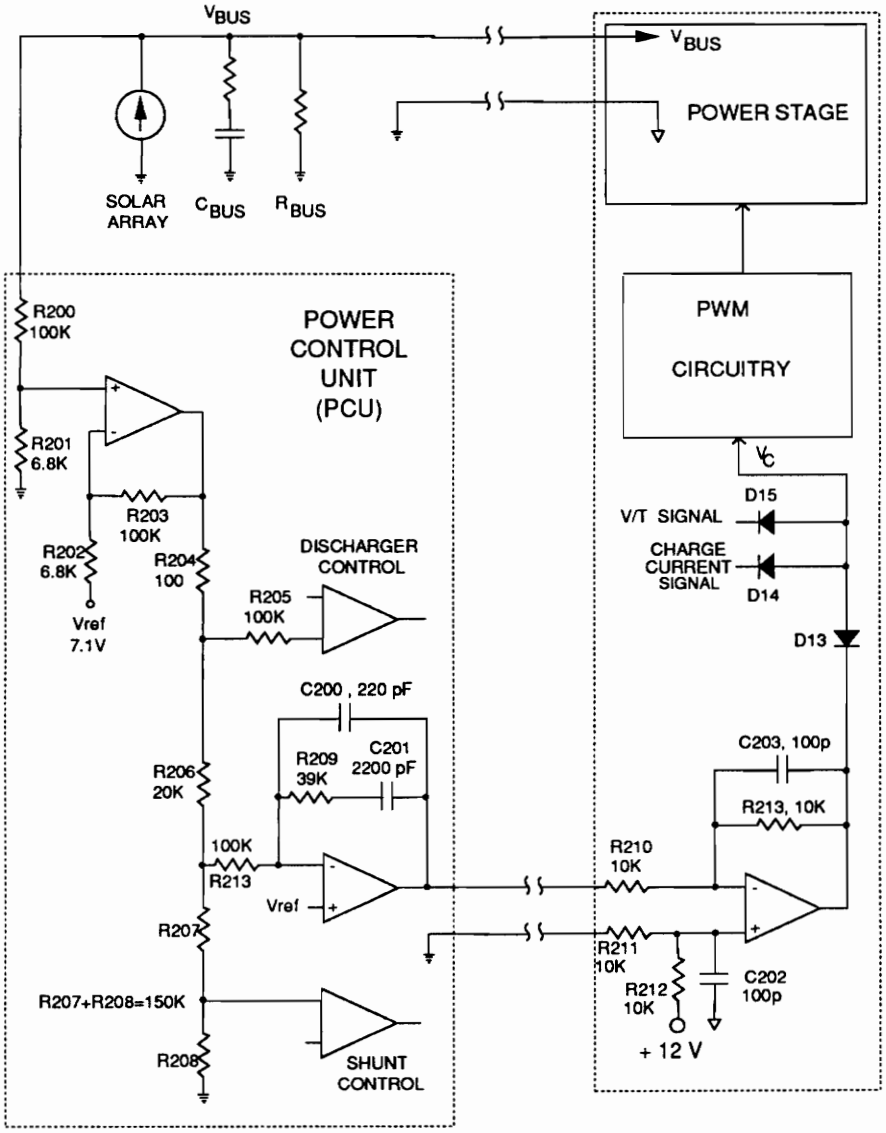


Figure 4.16 Power Control Unit Schematic

overall system R_i, which in turn increases the CIC loop gain. This must be kept in mind when designing the error amplifier for bus regulation mode. The control-to-bus voltage T.F. can be evaluated for a single battery charger if the gain is increased accordingly.

Recall that the control-to bus voltage T.F has a RHP open loop pole, which can also be seen in Fig. 4.18. This RHP pole causes the charger to be open loop unstable. With a voltage-loop compensator circuit shown in Fig.4.19, a root locus plot of the loop gain is shown in Fig. 4.17. It can be seen, that by increasing the compensator gain the system eigen values are moved from the RHP to the LHP. An unstable system becomes stable with proper compensation.

In order to design the error amplifier compensation, several decisions need to be made. First, the cross over frequency must be chosen. Evaluating the control-to-bus voltage T.F., it can be seen that the maximum gain occurs at maximum charge current. A bode plot of this T.F. is shown in Fig. 4.18. From this plot a cross over frequency can be determined. Since the loop gain has a RHP pole, the polar plot of the loop gain must encircle (-1,0) point once to satisfy the Nyquist criteria. Thus relative stability should be defined using a gain margin. In order to have adequate gain margin, a cross over frequency of 4 KHz is chosen. This is the condition that determines the integrator gain. A pole is placed at 18.5 KHz to attenuate switching noise and counteract the ESR zero. The E.A. zero is placed at 1.85 KHz for adequate gain and phase margin.

To complete the E.A. design, the integrator gain is determined. Since the control-to-bus voltage T.F. has a gain of 5 dB at 4 KHz, the E.A. is designed to have -5 dB gain at that frequency. A schematic with design equations for the E.A. is shown in Fig. 4.19.

A bode plot of the loop gain in bus regulation mode is shown in Fig. 4.20 with a 64 V battery and 4 A charge current. This condition shows worst case phase margin as well as minimum cross over frequency. It can be seen that there is adequate phase and gain margins (20 dB and 60°). There is a reduction in gain as charge current is reduced

resulting in a lower cross over frequency. It can also be seen there is excellent agreement between the theoretical model and the experimental data. The cross over frequency is approximately 1.7 KHz.

To verify system stability a Nyquist plot of the loop gain with the given compensation is shown in Fig.4.21. A bode plot of a system containing a RHP pole could give a false indication of stability. The Nyquist plot shows one encirclement of (-1,0). The Nyquist criteria however, allows the encirclement of -1, once, for every RHP pole in the closed loop transfer function. The closed loop transfer function in this mode does indeed contain one RHP pole. The system is therefore stable.

The loop gain in DCM is shown in Fig. 4.22. There is a further reduction in gain, although the cross over frequency is not significantly reduced.

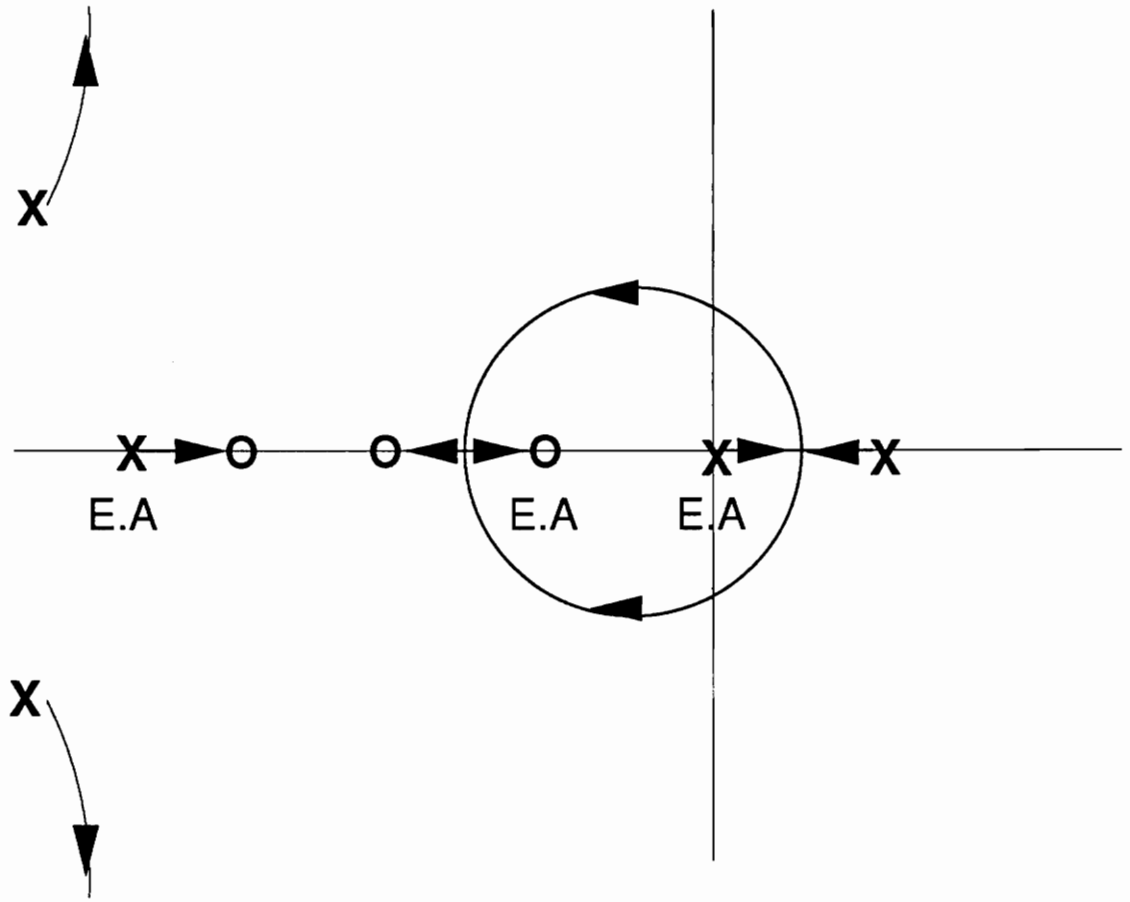


Figure 4.17 System Root Locus,

with respect to the gain variation of the compensator

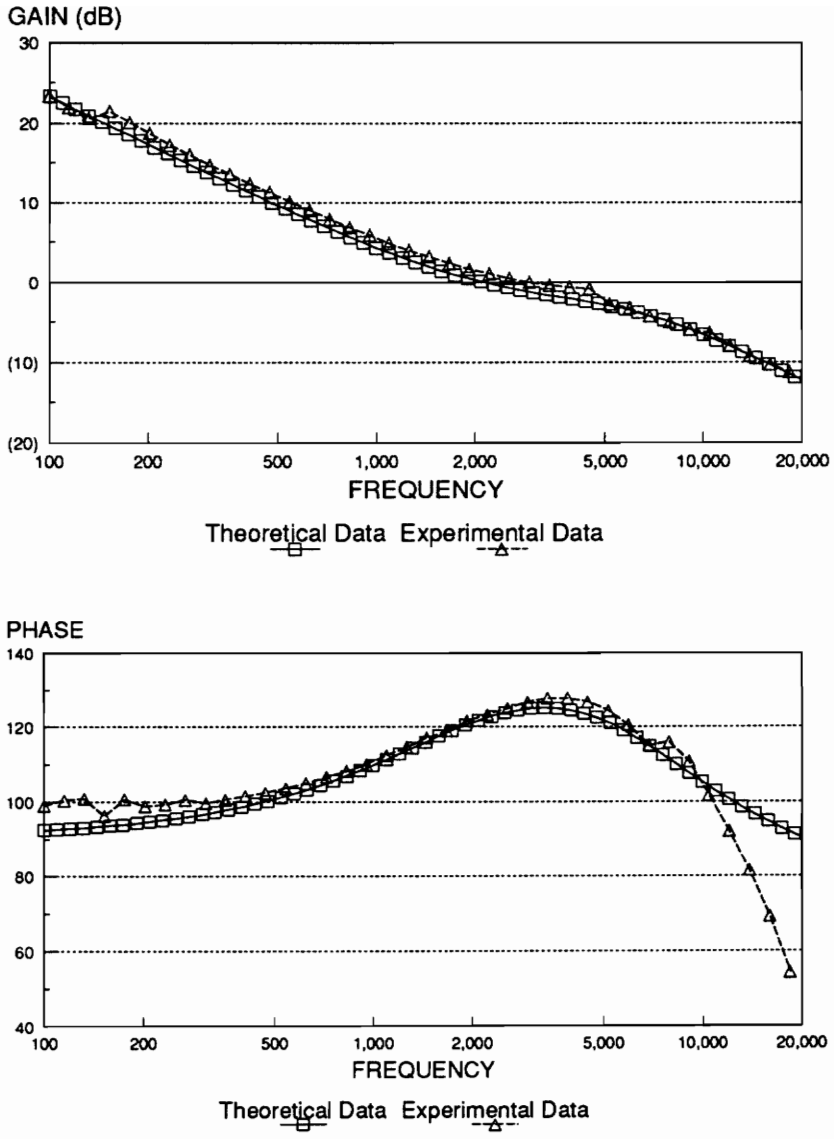


Figure 4.18 Control-to-Bus Voltage Transfer Function

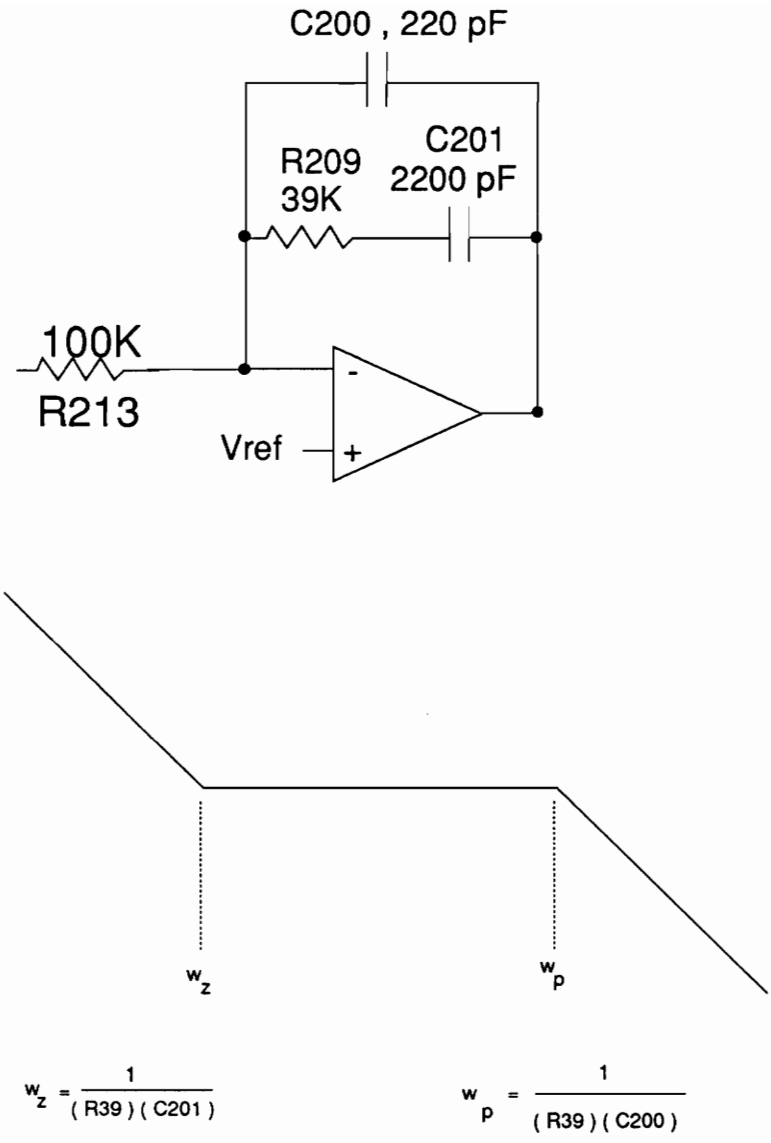


Figure 4.19 Bus Regulation Mode Error Amplifier

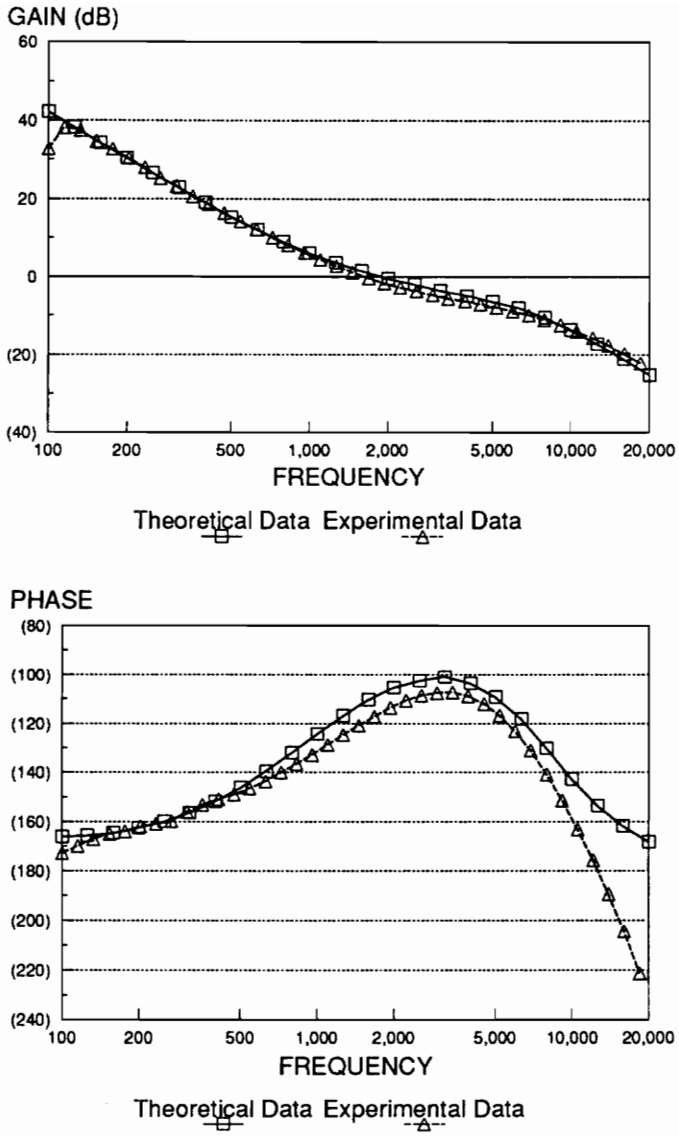


Figure 4.20 Bus Regulation Mode Loop Gain in CCM

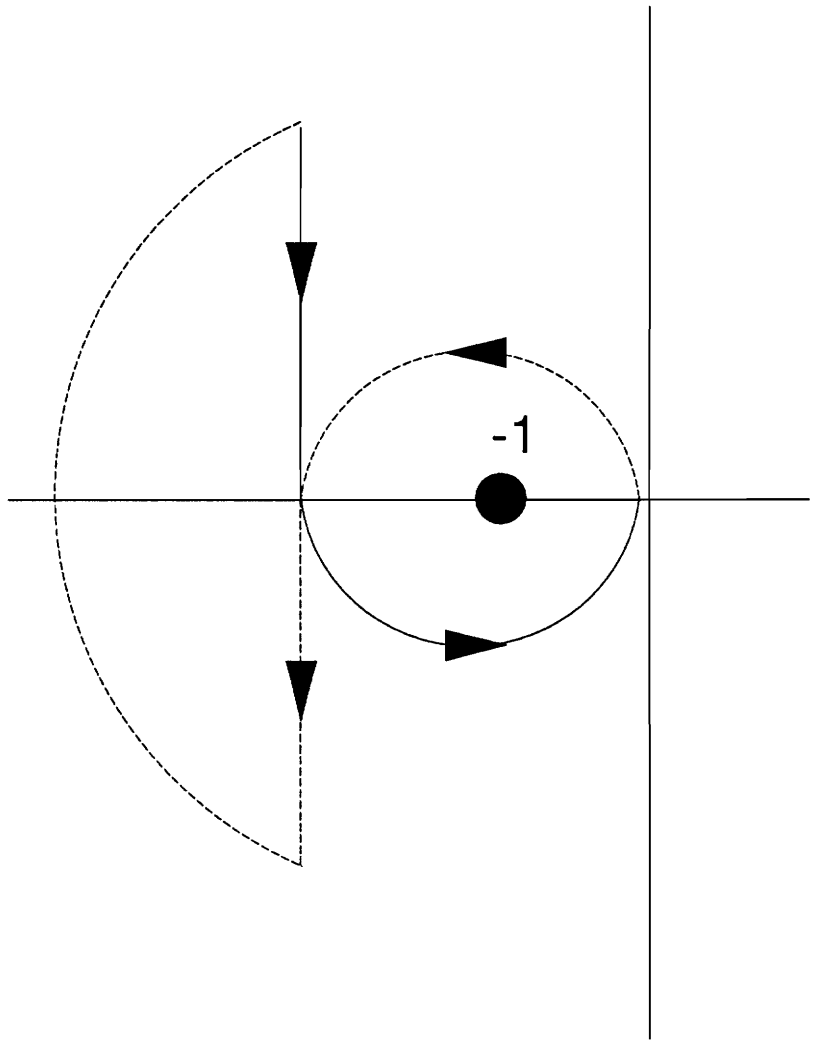
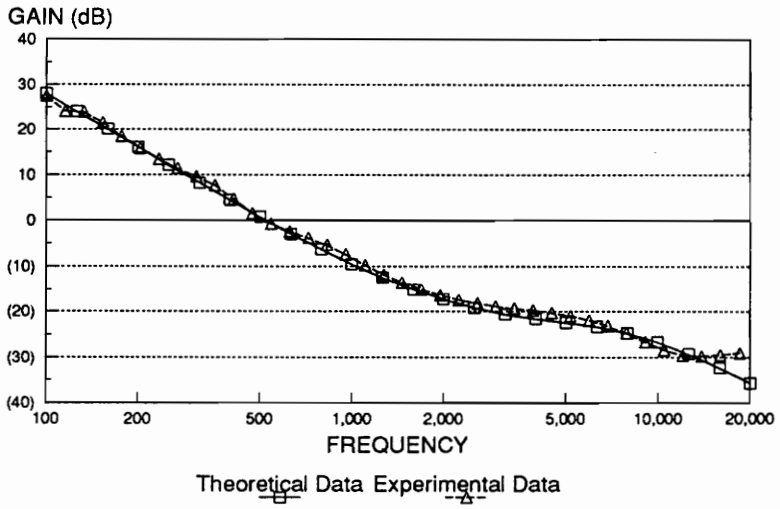


Figure 4.21 Loop Gain Nyquist Plot



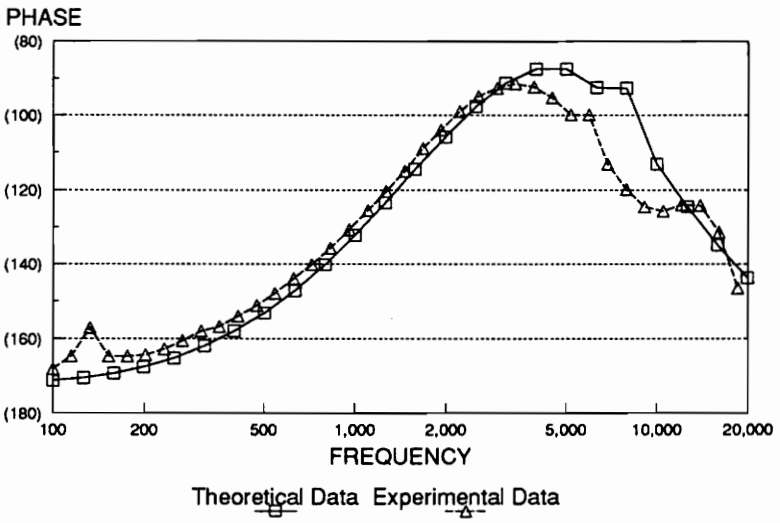


Figure 4.22 Bus Regulation Mode Loop Gain in DCM

4.11 Bus Regulation Mode Transient Response

The peak bus impedance specification for this design was 0.15 Ω. A frequency plot of theoretical and experimental bus impedance is shown in Fig. 4.23. The worst case for bus impedance occurs at low values of charge current. This is due to the loss of gain in the control-to-bus voltage transfer function and therefore a reduction in loop gain. The plot was taken at a charge current of 3.0 A and 64 V battery voltage. It can be seen there is good correlation between experimental and theoretical data. The peak value of bus impedance is approximately -27 dB. This corresponds to .044 Ω, well below the specification. This will ensure good transient response and no system interaction problems.

The transient response is shown in Fig. 4.24. The conditions are as follows: load current = 8.0 A, charge current = 7.5 A, and battery voltage = 69.2. The load current is stepped 5 A_{pp}. The bus voltage is shown in the bottom trace, ac coupled to show the transient response. The bus voltage transient settles to 90% of its final value within 400 μs. This corresponds to a bandwith of 2.5 KHz, which is the approximate bandwith of the converter in this operating condition. The peak transient value of bus voltage is 250 mV. This is approximately the current step times the ESR of the bus capacitance. The transient response is very well behaved and confirms the system stability.

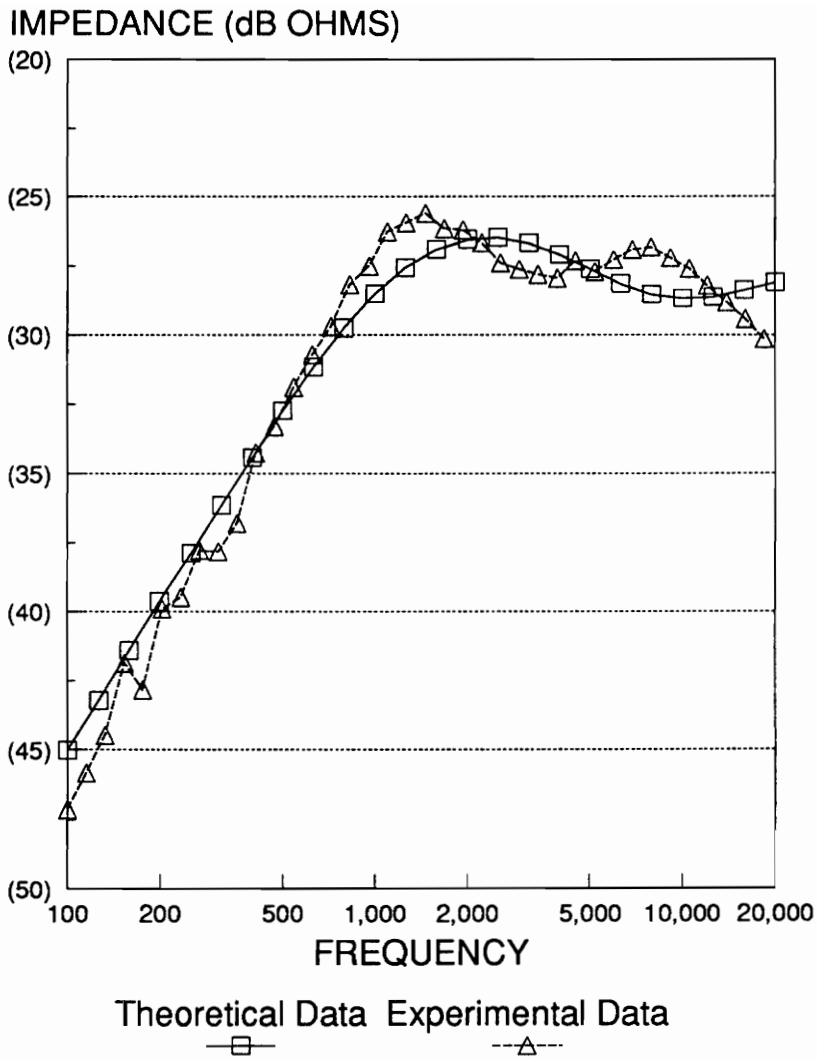
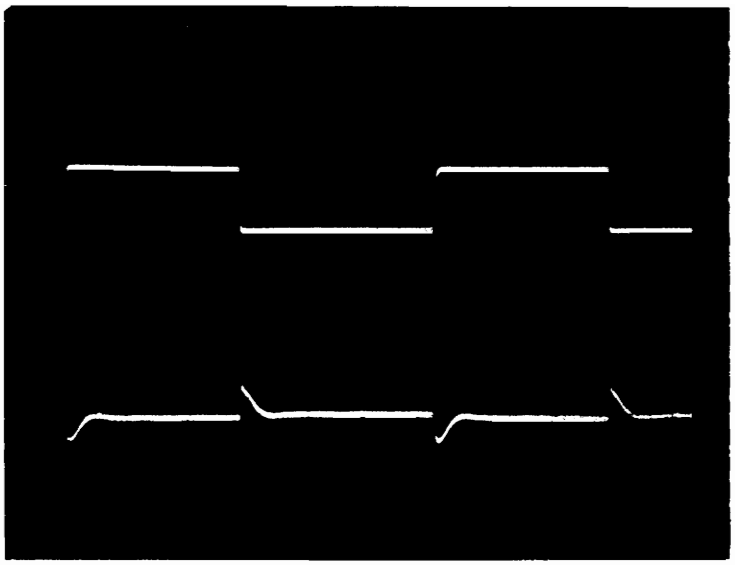


Figure 4.23 Bus Impedance



5 A/DIV

.5 V/DIV

1 ms/DIV

Figure 4.24 Transient Response in Bus Regulation Mode

5. Conclusion

The analysis and design of a MMMP battery charger has been presented. This work has resulted in a low weight highly efficient battery charger.

The MMMP and SM battery chargers have been quantitatively compared. This analysis has shown the MMMP converter to have significant advantages over SM converters. It has been shown that even with more components, the MMMP converter is a lighter subsystem than the SM. This is due to increased efficiency.

The MMMP converter also exhibits superior filter requirements. The equations describing the input and output current characteristics have been derived. The multi-phase operation provides significant improvement in the current waveforms. For applications that have extremely low ripple specifications, the multi-phasing approach is clearly indicated even without the efficiency gains.

The power stage design has been documented. The power stage performance was shown to be quite excellent. The switches actually had no spikes or ringing in the voltage waveforms. The input and output ripple was significantly below specification with only minimal filtering. In addition, the power stage was able to achieve 97% efficiency at minimum battery voltage and maximum charge current.

The current system design was significant in that the theoretical modeling was able to be verified using realistic solar array [13] and battery [14] simulators. Both charge regulation and bus voltage regulation loops were modeled and compared to experimental data. The models matched extremely well with the measurements.

The control loops were designed and both modes shown to exhibit good stability margin and transient response.

Due to the multi-module nature of the converter, CIC control was necessary to achieve current sharing between the modules. The CIC control was shown to provide performance benefits in both modes.

It has been shown the MMMP battery charger is a good choice for the charger subsystem, exhibiting excellent static and dynamic characteristics.

References

[1] T. Sizemore, "Design of a Battery Charger for the NASA EOS Space Platform," M.S. Thesis, Virginia Polytechnic Institute and State University, July, 1991.

[2] D. M. Sable, F. C. Lee and B. H. Cho, "Use of Nonlinear Design Optimization in the Comparison of Battery Charger Topologies for the Space Platform," IECEC, August 1990.

[3] D.M. Sable, A. Patil, T. Sizemore, S. Deuty, J. Noon, B.H. Cho, and F.C. Lee, Space Platform Power System Hardware Testbed, Final Report, June 1991.

[4] W. T. McLyman, *Transformer and Inductor Design Handbook*, New York, New York: Marcel Dekker, Inc., 1988.

[5] Magnetics, Inc., *Powder Cores, MPP and High Flux Cores for Filter Applications,* Manufacturer's Catalog #MPP-303V, Magnetics Inc, Butler, PA, 1986.

[6] T. K. Phelps and W. S. Tate, "Optimizing Passive Input Filter Design," Powercon 6, May 1979, pp. G1-1/10.

[7] V. Vorpérian, "Simplified Analysis of PWM Converters Using the Model of the PWM Switch: Parts I and II," IEEE Trans. on Aerospace and Electronic Systems, Vol. 26, no. 3, May 1990, pp. 490-505.

[8] R. B. Ridley, "Small-Signal Analysis of Parallel Power Converters," M.S. Thesis, Virginia Polytechnic Institute and State University, March 1986.

[9] B. Choi, B.H. Cho, R.B. Ridley, and F.C. Lee, "Control Strategy for Multi-Module Parallel Converter System," PESC, June 1990.

[10] R. B. Ridley, "A New Small-Signal Model for Current-Mode Control," Ph.D. Dissertation, Virginia Polytechnic Institute and State University, November 1990.

[11] S. J. Kim, "Modelling and Analysis of Spacecraft Battery Charger Systems," Ph.D. Dissertation, Virginia Polytechnic Institute and State University, April 1991.

[12] Magnetics, Inc., *Design Manual Featuring Tape Wound CoresPowder Cores,* Manufacturer's Catalog #TWC-300S, Magnetics Inc, Butler, PA, 1985.

[13] S.J. Butler, D.M. Sable, F.C. Lee, and B.H. Cho, "Design of a Solar Array Simulator for the NASA EOS Testbed," IECEC, August 1992.

[14] Z. Gur, A.R. Patil, D.M. Sable, X. Mang, B.H. Cho, F.C. Lee, "A Nickel Hydrogen Battery Simulator for the NASA EOS Satellite," IECEC, August 1992.

Vita

James P. Noon was born in Trenton, N.J., on May 27, 1960. He received the Associate in Applied Science degree from Mercer County Community College, Windsor, N.J. in 1985 and the Bachelor of Science degree from Trenton State College, Ewing, N.J. in 1988, both in Electrical Engineering Technology.

From 1985 to 1987 he was employed as an Engineering Technician at RCA in the Analog Design group. From 1988 to 1990 he was employed by GE Astro - Space Division as an Associate Member of the Technical Staff where he was involved in the design and analysis of power supplies for spacecraft applications. Also during this time he was an Adjunct Instructor in the Electrical Engineering Technology Department at Mercer County Community College.

In June, 1990 he joined the Virginia Power Electronics Center at Virginia Polytechnic Institute and State University as a Graduate Research Assistant while pursuing the Master of Science degree in Electrical Engineering.

After graduation, the author will be employed by Lutron Electronics, Inc. as a Design and Development Engineer in the Power Electronics Group.