

# **Characterization and Failure Mode Analysis of Cascode GaN HEMT**

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## Abstract

Recent emerging gallium nitride (GaN) high electron mobility transistor (HEMT) is expected to be a promising candidate for high frequency power conversion techniques. Due to the advantages of the material, the GaN HEMT has a better figure of merit (FOM) compared to the state-of-the-art silicon (Si) power metal oxide silicon field effect transistor (MOSFET), which allows the GaN HEMT to switch with faster transition and lower switching loss. By applying the GaN HEMT in a circuit design, it is possible to achieve high frequency, high efficiency, and high density power conversion at the same time.

To characterize the switching performance of the GaN HEMT, an accurate behavior-level simulation model is developed in this thesis. The packaging related parasitic inductance, including both self-inductance and mutual-inductance, are extracted based on finite element analysis (FEA) methods. Then the accuracy of the simulation model is verified by a double-pulse tester, and the simulation results match well with experiment in terms of both device switching waveform and switching energy.

Based on the simulation model, detailed loss breakdown and loss mechanism analysis are made. The cascode GaN HEMT has high turn-on loss due to the body diode reverse recovery of

the low voltage Si MOSFET and the common source inductance (CSI) of the package; while the turn-off loss is extremely small attributing to the cascode structure.

With this unique feature, the critical conduction mode (CRM) soft switching technique are applied to reduce the dominant turn on loss and increase converter efficiency significantly. The switching frequency is successfully pushed to 5MHz while maintaining high efficiency and good thermal performance.

Traditional packaging method is becoming a bottle neck to fully utilize the advantages of GaN HEMT. So an investigation of the package influence on the cascode GaN HEMT is also conducted. Several critical parasitic inductors are identified, which cause high turn on loss and high parasitic ringing which may lead to device failure. To solve the issue, the stack-die package is proposed to eliminate all critical parasitic inductors, and as a result, reducing turn on loss by half and avoiding potential failure mode of the cascode GaN device effectively.

Utilizing the proposed stack-die package and ZVS soft switching, the GaN HEMT high frequency, high efficiency, and high density power conversion capability can be further extended to a higher level.

*To my parents:*

*Weilong Liu & Mei Zhang*

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# Chapter 1. Introduction

## 1.1 Overview of GaN Power Device

Advanced power semiconductor devices have consistently proven to be a major force in pushing the progressive development of power conversion technology. The emerging gallium nitride (GaN) high electron mobility transistor (HEMT) is considered a promising candidate to achieve high-frequency, high-efficiency, and high-power-density power conversion. Due to the advantages of the material, the GaN HEMT has the features of a wide band gap, high electron mobility, and high electron velocity [1], [2]. Thus a better figure of merit can be projected for the GaN HEMT [3-5] than for the state-of-the-art Si MOSFETs, which allows the GaN HEMT to switch with faster transition and lower switching loss. By using the GaN HEMT in a circuit design, the switching frequency can be pushed up to multi MHz, and continue to have high efficiency. So it is able to achieve high frequency, high efficiency, and high power density power conversion at the same time.

Table 1.1 Material properties of GaN, SiC, and Si

Parameter	Si	SiC	GaN
Band Gap $E_g$ (eV)	1.12	3.2	3.4
Critical Field $E_{crit}$ (MV/cm)	0.3	3.5	3.3
Electron Mobility $\mu_n$ (cm <sup>2</sup> /(V·s))	1500	650	990~2000
Permittivity $\epsilon_r$	11.8	9.7	9

All of these advantages are stemmed from the basic physical properties of the material. Table 1.1 [4] lists four key parameters of three major materials making power semiconductor devices which are silicon (Si), silicon carbide (SiC), and gallium nitride (GaN).

First of all, both SiC devices and GaN devices are classified as wide band gap (WBG) devices because the band gap energy  $E_g$  of these two materials are significantly higher than Si device. The band gap of a semiconductor material reflects the strength of the chemical bonds between atoms in the lattice. High band gap energy means an electron requires more energy to jump from one site to another site, or saying the lattice structure is more stable. Based on this, power semiconductor devices made of high band gap energy material usually have lower leakage current and higher operating temperature.

For the parameter critical electric field, it is also related to the chemical bonds of the material. Generally speaking the stronger bonds, the higher critical field. Equation 1.1 shows the relationship between breakdown voltage, drift region width, and critical field.

$$V_{BR} = \frac{1}{2} w_{drift} \cdot E_{crit} \quad (1.1)$$

According to this equation, the breakdown voltage is proportional to the width of drift region and the critical field. So for a given breakdown voltage, GaN device has around 10 times narrow drift region compared to Si device.

In order to support this critical field in the region, a certain amount of electrons should be depleted. So a higher critical field also mean higher concentration of carriers in the drift region. Equation 1.2 further shows the relationship, in which  $q$  is the charge of an electron,  $N_D$  is the total number of electrons,  $\epsilon_0$  and  $\epsilon_r$  are vacuum permittivity and relative permittivity of the material respectively.

$$q \cdot N_D = \frac{\epsilon_0 \cdot \epsilon_r \cdot E_{crit}}{W_{drift}} \quad (1.2)$$

According to equation 1.2, it is clear that if the electrical field is 10 times higher, and the drift region is 10 times smaller, then the total number of electrons is 100 times comparing GaN device to Si device. This is the basis that GaN device has significant better performance than Si device for high frequency power conversion.

The on-state resistance of a device is calculated based on equation (1.3), in which  $\mu_n$  is the mobility of electrons.

$$R_{on} = \frac{W_{drift}}{q \cdot N_D \cdot \mu_n} \quad (1.3)$$

Substituting equation 1.1 and 1.2 into 1.3, the on-state resistance is derived as equation 1.4. Then according to this equation, it is very clear that for given breakdown voltage, materials with higher critical field and electron mobility has significantly smaller on-resistance. And Figure 1.1 [2, 6] is drawn based on this equation.

$$R_{on} = \frac{4V_{BR}^2}{\epsilon_0 \cdot \epsilon_r \cdot \mu_n \cdot E_{Crit}^3} \quad (1.4)$$

In Figure 1.1, the x-axis is breakdown voltage while the y-axis is specific on-resistance. The three solid lines are theoretical limit for Si, SiC, and GaN based on material properties. Si technology has become very mature over last three decades so that the state-of-the-art Si MOSFET is close to its theoretical limit. Recent Si Super Junction MOSFET even outperforms Si's limit. So there is still some margin that the performance of Si device can be continually improved in future.

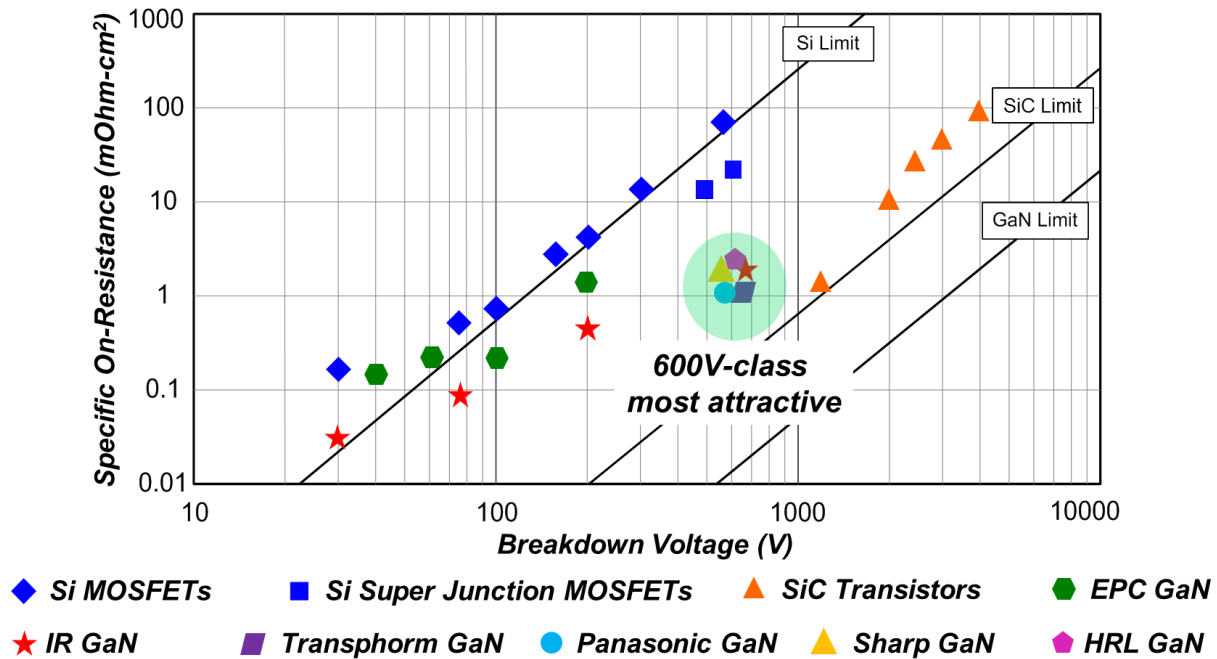


Figure 1.1 Specific on-resistance vs breakdown voltage for Si, SiC, and GaN

SiC transistors are majorly targeted at high voltage and high temperature application because besides high band gap energy, SiC material also has significantly higher thermal conductivity which makes it ideal for high temperature operation. Generally, the voltage rating of SiC transistors are beyond 1200V.

The emerging GaN device has theoretical limit significantly higher than both Si and SiC. Many semiconductor companies recently jump into GaN market and they are marketed on the graph as major GaN players. The early stage GaN device is premature so that they just outperform Si MOSFET but far behind its theoretical limit. What is more interesting is many GaN players simplify focusing on 600V-class devices and it seems that is the most attractive market for GaN at current stage. The research in this thesis is also focused on 600V GaN device and its application for high frequency power conversion.



## 1.2 Enhancement Mode GaN vs Depletion Mode GaN

The conductivity of GaN device is based on its piezoelectric property. As shown in Figure 1.2, by growing a thin layer of AlGaN on top of a GaN, a strain is created at the interface between AlGaN and GaN so that high concentration of electrons are induced which is also referred as two-dimensional electron gas (2DEG) [4, 5]. The electrons in the 2DEG region has high electron mobility and high conductivity, which is the basis of GaN HEMT.

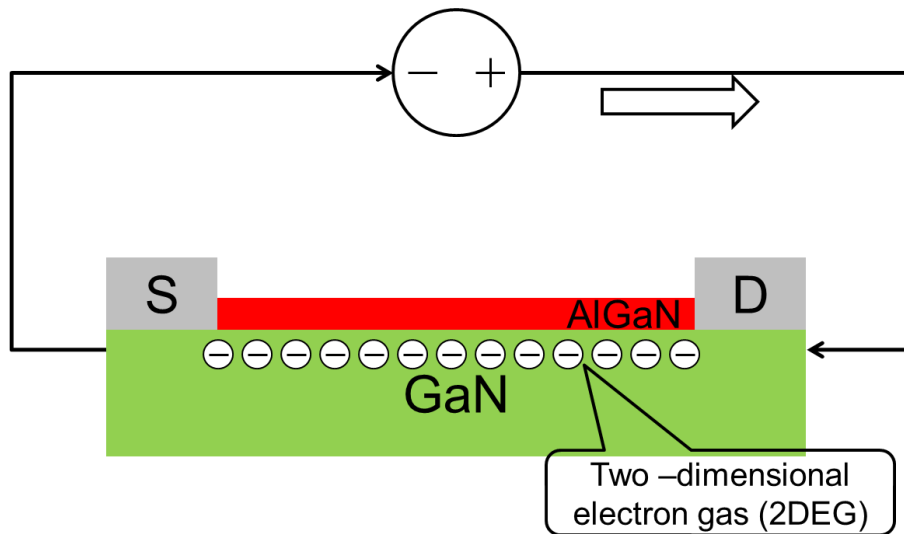


Figure 1.2 Basic structure of GaN device and its piezoelectric property

Then if an external source is applied between drain terminal and source terminal, the GaN is conducting and current flowing through the channel of GaN device.

To control the on/off state of GaN device, a gate electrode is applied. According to different structures of the gate terminal, GaN device can be divided into two categories, depletion mode GaN device and enhancement mode GaN device.

The depletion mode GaN is more natural according to its piezoelectric property. With a simple d-mode gate electrode, the device is naturally conductive if no voltage is applied between

gate and source. To turn off the device, a negative  $V_{gs}$  is applied so that the electrons under the gate area is depleted. The depletion mode GaN device is also named normally-on GaN device.

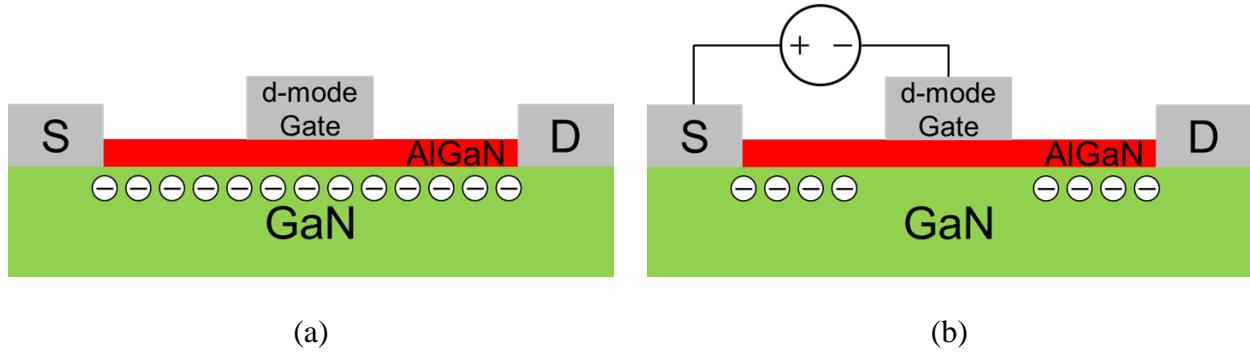


Figure 1.3 Basic structure of depletion mode GaN device, (a) on state, (b) off state

With a more complicated process, an e-mode gate can also be made on the GaN device. Different with the depletion mode GaN device, the enhancement mode GaN device is in off state if no external  $V_{gs}$  applied, while a positive  $V_{gs}$  is in need to turn on the enhancement mode GaN device.

Usually there are three popular structures have been used to create the e-mode gate including recessed gate, implanted gate, and pGaN gate.

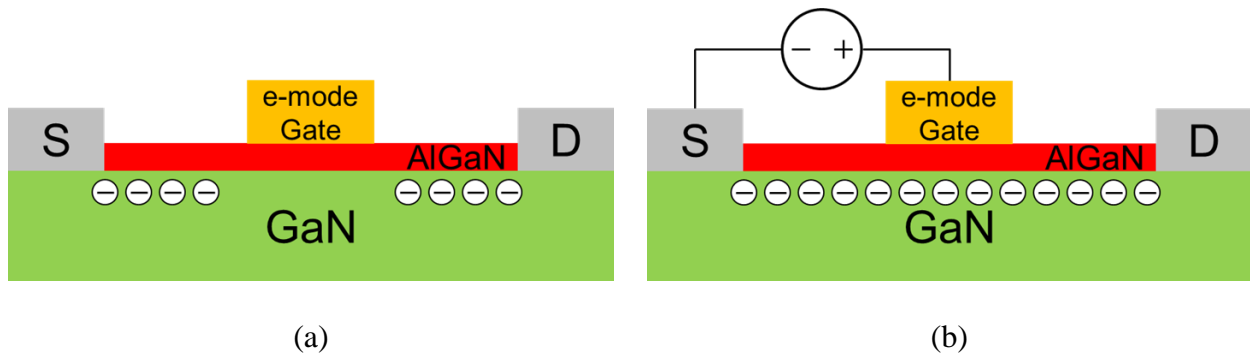


Figure 1.4 Basic structure of enhancement mode GaN device, (a) on state, (b) off state

To further compare depletion mode GaN device versus enhancement mode GaN device, the four quadrants I-V characteristics are plotted (based on simulation models) in Figure 1.5 and 1.6.

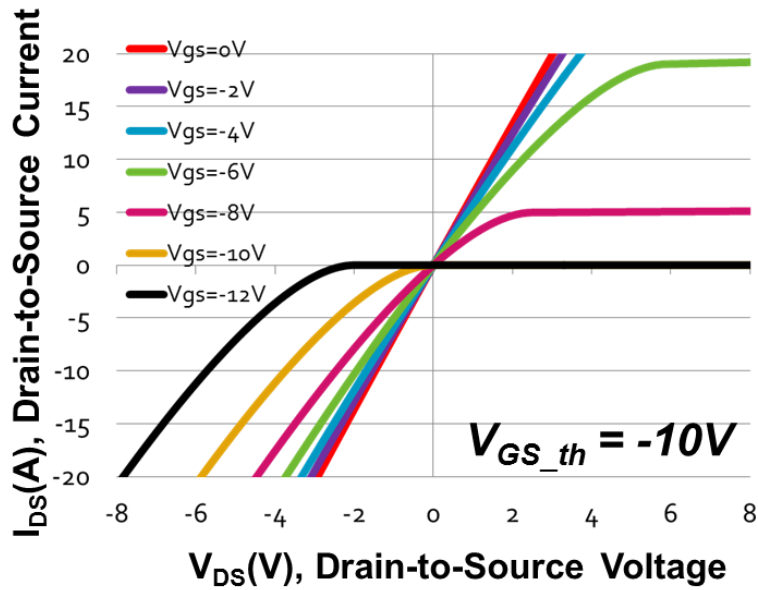


Figure 1.5 I-V characteristics of depletion mode GaN

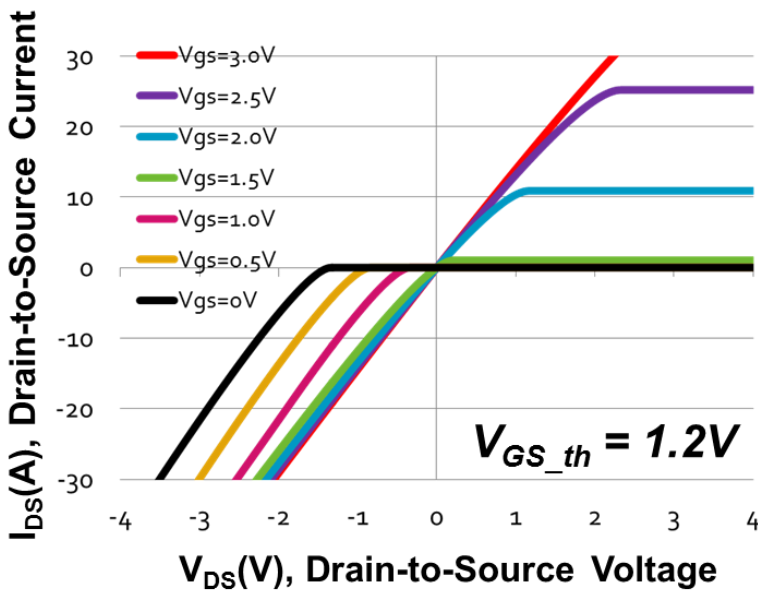


Figure 1.6 I-V characteristics of enhancement mode GaN

The patterns of both four quadrant I-V family curves are similar while the major difference is the  $V_{gs}$  applied on each curve. For the depletion mode GaN device in this example, the threshold voltage is  $-10V$  so that device is fully turned-on when  $V_{gs}=0V$  while negative voltage is applied like  $V_{gs}=-12V$  to turn it off. In comparison, for the enhancement mode GaN device, the threshold voltage is positive like  $1.2V$  in this case, so that device is in off state when  $V_{gs}=0V$  while positive voltage is in need like  $3V$  to fully enhance the channel.

Another similarity can also be observed from both the I-V family curves which is the reverse conduction mode. For traditional Si power MOSFET, there is a built-in body diode from source terminal to drain terminal so that if a positive voltage is applied on  $V_{sd}$ , the device can conduct without  $V_{gs}$  applied, and in this scenario, the device behaves like a diode. For the power GaN HEMT, it doesn't have a body diode. However, it is in a lateral structure and symmetric from both source side and drain side. This feature offers a reverse conduction capability in a very different mechanism compared to Si MOSFET. Since the GaN HEMT is lateral and symmetric, then a voltage higher than threshold voltage applied on both gate-to-source or gate-to-drain can turn on the device. As a result, in the third quadrant of the I-V family curve, the device can conduct when  $V_{gd}$  is higher than the threshold voltage. Take the enhancement mode GaN as an example, the black curve is the I-V characteristic when  $V_{gs}=0V$ . So in the first quadrant, it maintains off state before avalanche breakdown. In the third quadrant, the device starts to conduct when  $V_{ds}$  is lower than  $-1.2V$ . The reason is then  $V_{ds}=-1.2V$ , and  $V_{gs}=0V$ , then  $V_{gd}=1.2V$  which is just the threshold voltage. So further decreasing  $V_{ds}$  will finally fully turn on the device with a positive  $V_{gd}$  driving voltage.

Similar reverse conduction mechanism is observed in the depletion mode GaN device. For example, the black curve is for  $V_{gs}=-12V$  condition. Then when  $V_{ds}$  is lower than  $-2V$ , the  $V_{gd}$

is higher than  $-10\text{V}$  which is the threshold voltage of the normally-on GaN device, so that it starts to conduct when further decreasing  $V_{ds}$ .

The issue of this reverse conduction mode is it doesn't like a diode characteristic during conducting when current increases a lot the voltage drop increases a little, but more like a resistor with negative bias voltage. When applied the GaN device into circuit design, reverse conduction with off state  $V_{gs}$ , like the synchronous rectifier in dead time, leads to significantly higher conduction loss compared to Si MOSFET body diode conduction.

The solution to solve this issue is discussed in paper [7, 8], paralleling diode or fine tuning dead-time are two effective methods.

### **1.3 Characteristics of 600V Cascode GaN HEMT**

Even the processing of the depletion mode GaN device is simpler than the enhancement mode GaN device, normally-on property is usually not preferred in application because firstly the driver design for normally-on device is more complicated since negative voltage is used; secondly there might be shoot-through risk during start-up and other abnormal situations.

To solve this issue but still utilizing the depletion mode GaN device, the cascode structure, as shown in Figure 1.7, is widely used in most depletion mode GaN devices to make it like a normally-off device.

In the cascode structure, the depletion mode GaN is in series with a Si MOSFET. With this configuration, the gate-to-source voltage of GaN equals to the source-to-drain voltage of Si. So the Si MOSFET is used to control the on and off states of the GaN HEMT.

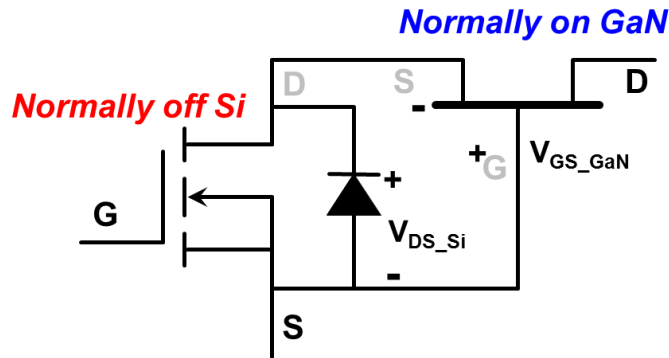


Figure 1.7 Cascode structure for depletion mode GaN

In addition to drive GaN, the Si MOSFET also offers protection to avoid GaN gate breakdown. For example, for a 600V depletion mode GaN, the threshold voltage is -22V while the gate breakdown voltage is -35V. Then a 30V Si MOSFET is used in this cascode structure. On one hand, a 30V MOSFET can make sure to turn off the GaN HEMT effectively while leaving some margin between the threshold voltage and fully turn-off voltage so that it is not easy to false turn on the GaN HEMT and there is enough voltage difference to turn-off the GaN HEMT quickly. On the other hand, the 30V breakdown voltage provides some margin so that even at extreme case the  $V_{ds}$  of Si MOSFET increases quickly but can still be clamped at 30V through avalanche breakdown mechanism. Then the  $V_{gs}$  of GaN HEMT won't see voltage undershoot lower than -35V in steady state.

One side effect of the cascode structure is that the Si MOSFET adds extra on-state resistance to the cascode device. Figure 1.8 [5] shows the percentage of the on resistance from MOSFET added on the total device with different voltage rating devices. Obviously, the cascode structure is not suitable for low voltage device, like in a 40V cascode device, the Si MOSFET contribute more than 40% total on resistance, while this rate is reduced to around 30% in 100V device, below 15% in 200V device, and even below 5% in 600V device.

In future, the on resistance of Si will only reduce in a limited range because Si technology is pretty mature, while the on resistance of GaN is likely to reduce dramatically since the GaN technology has large room to improve. Then the curve in this figure will even shift to the upper right corner which means MOSFET occupies a larger percentage of on resistance.

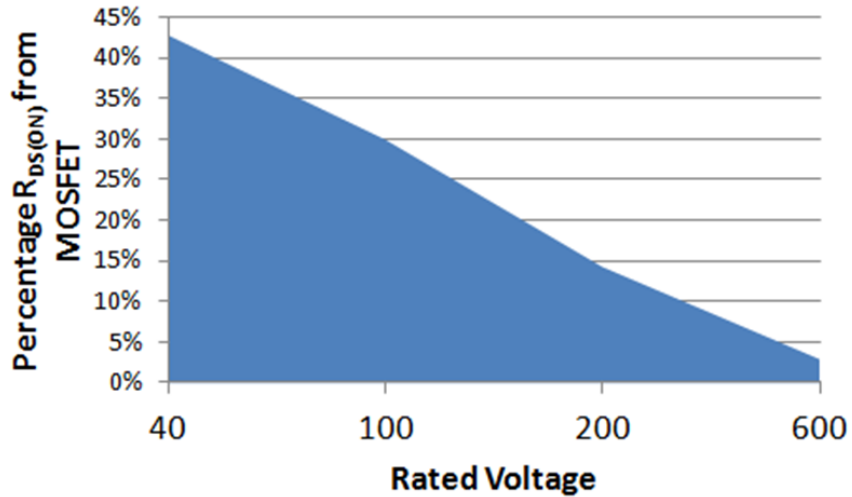


Figure 1.8 Percentage of on-resistance from Si MOSFET to the cascode device [5]  
(used with permission of Efficient Power Conversion Corporation (EPC), 2014)

Considering this reason, the cascode structure is not practical in low voltage device. So far the cascode structure are only seen adopted in 600V-class GaN HEMT.

Table 1.2 Driving characteristics of e-mode GaN and cascode d-mode GaN

	E-mode GaN			Cascode D-mode GaN		
	EPC	HRL	Panasonic	IR	Sharp	Transphorm
$V_{GS\_Max}(V)$	-5~6	0~3.3	-10~4.5	±20	±30	±18
Recommended Gate Voltage (V)	4.5	3	3.2	6	10	10
$V_{TH}(V)$	1.4	0.6	1.2	2	3.5	1.8

The enhancement mode GaN device has many advantages like simple structure, simple packaging, no body diode reverse recovery effect, and no extra on resistance from Si MOSFET. However, the gate drive design is very critical for today's enhancement mode GaN device. A few examples are listed in Table 1.2 which shows that the device fully enhanced gate drive voltage is very close to the breakdown voltage of the gate. The safety margin is usually less than 2V so that any voltage spike or parasitic ringing may easily cause device failure. Till this thesis is drafted, the vulnerable gate characteristic is still an unsolved problem.

On the contrary, the gate drive design for the cascode GaN device is relatively simpler. Since the driving voltage is directly applied on the low voltage Si MOSFET, many commercial gate driver for Si MOSFET is compatible for the cascode GaN device. This is the major reason why at current stage, the cascode GaN structure is popular in 600V-class power GaN devices. The research in this thesis are based on the 600V cascode GaN HEMT.

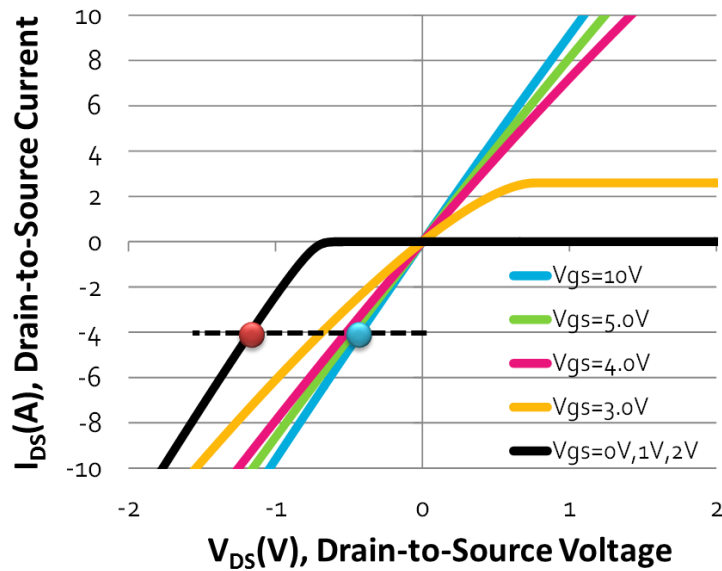


Figure 1.9 I-V characteristics of cascode GaN HEMT





Figure 1.10 Conduction principle of cascode GaN HEMT, (a)  $V_{gs}=10V$ , (b)  $V_{gs}=0V$

The I-V characteristics and conduction principle of the cascode GaN HEMT is shown Figure 1.9 and 1.10. When 10V gate drive voltage is applied, the Si MOSFET is fully enhanced. Since the on resistance of the 30V Si MOSFET is very small (10mOhm level), so the gate drive voltage applied on the depletion mode GaN HEMT is close to zero and the GaN HEMT is fully turned on. In this conduction mode, the current flows through both the channel of the Si MOSFET and the channel of the GaN HEMT, so that the voltage drop equals to equation (1.5). The current can be bidirectional and it is symmetric in the first quadrant and the third quadrant (as the blue curve in Figure 1.9). In this condition, since the on resistance of the 30V Si MOSFET is much smaller than that of the 600V GaN HEMT, the total voltage drop is dominant by the GaN HEMT.

$$V_{DS} = I_{DS} \cdot (R_{ds\_GaN} + R_{ds\_Si}) \quad (1.5)$$

When the Si MOSFET is turned off by applying 0V driving voltage, the cascode GaN HEMT is blocking in the first quadrant while still conducting in the third quadrant. The current first goes through the body diode of the Si MOSFET. Then the gate-to-source voltage of the GaN HEMT equals to the forward voltage of the body diode which makes it in on state. So the current also goes through the channel of the GaN HEMT like shown in Figure 1.10(b). In reverse

conduction mode, the voltage drop equals to equation (1.6) and is corresponding to the black curve in Figure 1.9.

$$V_{SD} = I_{SD} \cdot R_{ds\_GaN} + V_{bd} \quad (1.6)$$

Comparing the two reverse conduction modes in the third quadrant, the second one current going through the body diode has significantly high voltage drop and also high conduction loss. For example, as the red dot and blue dot marked in Figure 1.9, given the same 4A current, the voltage drop of the red dot is about twice the voltage drop of the blue dot, which means the conduction loss is almost doubled.

The reverse conduction modes are common if the cascode GaN HEMT is used as an synchronous rectifier or in a current bidirectional flowing converter. During dead time, the cascode GaN HEMT has significantly higher conduction loss compared to traditional Si MOSFET. So the dead time control is more critical for the cascode GaN HEMT than for Si MOSFET in order to avoid the high dead time loss.

Finally, when comparing the 600V GaN HEMT with the state-of-the-art Si MOSFET, dramatically performance improvement can be projected. Table 1.3 shows several key parameters comparison. Two devices have similar breakdown voltage and on resistance. Dynamic parameters and reverse operation parameters are compared. The total gate charge  $Q_g$  of GaN is smaller than one tenth of Si, which can translate to significantly smaller driving loss. The  $Q_{gd}$  of GaN, also known as the miller charge, is smaller than one fifteenth compared to Si so that much smaller voltage and current transition switching loss can be projected. Similarly, smaller  $E_{oss}$  means smaller  $CV^2$  loss is hard switching turn on; smaller  $Q_{oss}$  means less resonant time, smaller duty cycle loss, and smaller root-mean-square (RMS) current in a resonant converter, so

that smaller conduction loss on both power devices and other passive components. Last but not least, as the depletion GaN HEMT itself doesn't have body diode, so only the low voltage Si MOSFET contributes a smaller reverse recovery charge, the related reverse recovery loss for the cascode GaN HEMT should also be dramatically smaller than the Si MOSFET. All of the benefits indicate that the cascode GaN HEMT is superior for high frequency power conversion.

Table 1.3 Key parameter comparison between cascode GaN vs state-of-the-art Si

Parameter		GaN HEMT	State-of-the-art Si MOSFET
Static	$V_{DS}$	600V	600V
	$R_{DS}$	0.15Ω/0.18Ω <sup>[1]</sup>	0.14Ω/0.16Ω <sup>[1]</sup>
Dynamic	$Q_g$	6.2nC <sup>[2]</sup>	75nC <sup>[3]</sup>
	$Q_{gd}$	2.2nC <sup>[2]</sup>	38nC <sup>[3]</sup>
	$E_{oss}$	6μJ <sup>[4]</sup>	11μJ <sup>[4]</sup>
	$Q_{oss}$	28nC <sup>[4]</sup>	130nC <sup>[4]</sup>
Reverse Operation	$Q_{rr}$	42nC <sup>[5]</sup>	8200nC <sup>[6]</sup>
	$t_{rr}$	24ns <sup>[5]</sup>	460ns <sup>[6]</sup>

[1]  $T_j=25^\circ\text{C}$ ; [2]  $V_{GS}=0-4.5\text{V}$ ,  $V_{DS}=100\text{V}$ ,  $I_b=12\text{A}$ ; [3]  $V_{GS}=0-10\text{V}$ ,  $V_{DS}=480\text{V}$ ,  $I_b=11.3\text{A}$ ;  
 [4]  $V_{GS}=0\text{V}$ ,  $V_{DS}=0-400\text{V}$ ; [5]  $V_{DS}=480\text{V}$ ,  $I_{DS}=9\text{A}$ ,  $di/dt=450\text{A}/\mu\text{s}$ ; [6]  $V_{DS}=400\text{V}$ ,  $I_{DS}=11.3\text{A}$ ,  $i/dt=100\text{A}/\mu\text{s}$ ;

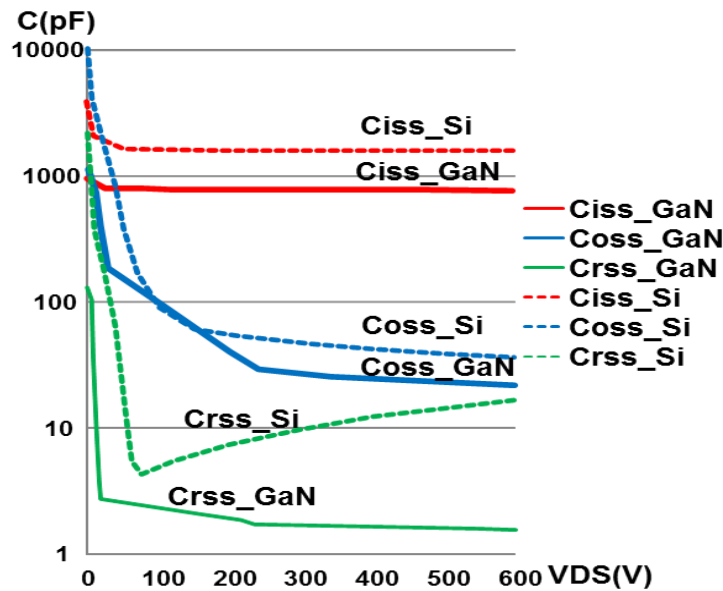


Figure 1.11 C-V characteristics comparison between cascode GaN and state-of-the-art Si

Figure 1.11 further compares the non-linear C-V characteristics of the GaN HEMT and the Si MOSFET, which clearly indicates that for all of the three parasitic capacitances (input capacitance  $C_{iss}$ , output capacitance  $C_{oss}$ , and miller capacitance  $C_{rss}$ ) the GaN HEMT are much smaller than the Si MOSFET. Particularly, the non-linearity of Si MOSFET is more prominent so that the capacitance in low voltage is usually tens of times larger than the capacitance in high voltage. The strong non-linear property further makes Si MOSFET longer turn-on and turn-off delay time and voltage/current rising/falling transition time. Consequently, it is even harder for Si MOSFET to be used in MHz high frequency. As a comparison, the non-linearity of the GaN HEMT parasitic capacitor is much alleviated so that switching transition can be finished significantly faster than the Si MOSFET.

## 1.4 Thesis Organization

As the emerging GaN device is expected to be a game changing device, this thesis focuses on evaluation and characterization of a 600V cascode GaN HEMT, especially for high frequency power conversion.

In order to study the detailed high speed switching performance of the cascode GaN HEMT, an accurate simulation model is first developed in Chapter 2. The model is based on a manufacturer provided preliminary model. Package parasitic inductances are accurately extracted by FEA simulation tool and considering the impact of both self-inductance and mutual-inductance. A double pulse tester (DPT) is carefully designed with critical loop-inductance minimized printed circuit board (PCB) and high bandwidth measurement components. Each component is well modelled so that the DPT can be used to verify the developed simulation model. Simulation and experimental results comparison shows that the developed simulation can

predict the switching performance of the cascode GaN device accurately. With the simulation model, detailed converter loss distribution is broken down. The switching loss mechanism is further studied. Finally, zero-voltage-switching (ZVS) techniques are proposed to improve the high frequency performance of the cascode GaN HEMT.

In Chapter 3, the package influence on the cascode GaN HEMT is investigated. Critical common source inductance (CSI) are identified. Two major issues caused by the cascode package are illustrated. Finally, the stack-die package for cascode GaN is proposed to effectively reduce turn-on loss and reduce turn-off parasitic ringing. What is most important is the potential device failure mode is avoided with the proposed stack-die package. The analysis is verified by both simulation and experiment.

Chapter 4 concludes the thesis with summary and future work.

## Chapter 2. Characterization and Modeling of 600V

### Cascode GaN HEMT

#### 2.1 Simulation Model Development and Package Parasitics Extraction

A SPICE (Simulation Program with Integrated Circuit Emphasis) based behavior-level simulation model is initially provided by the device manufacturer. SIMetrix is used for conducting the circuit simulation.

When the simulation model is first applied into a buck converter, the original simulation waveform doesn't match with the experimental waveform like shown in Figure 2.1.

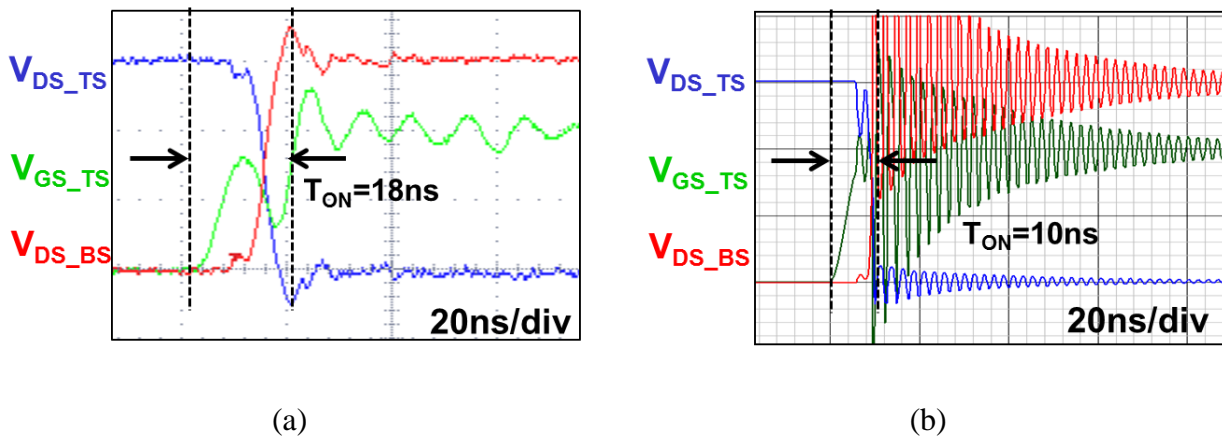
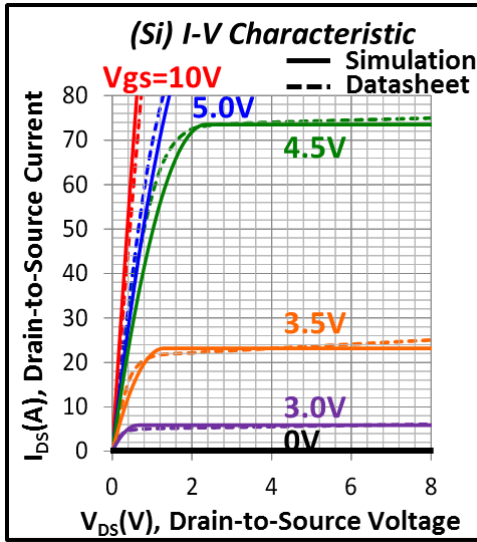


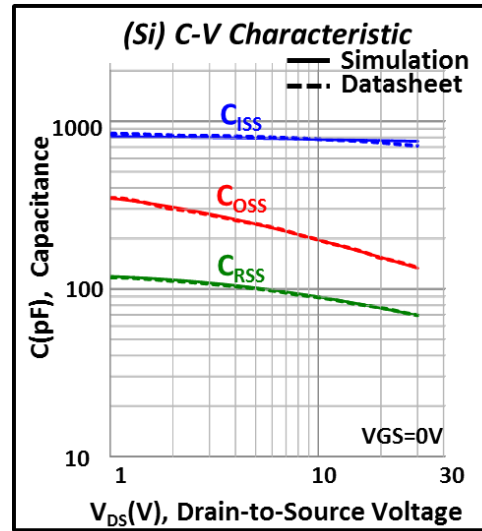
Figure 2.1 (a) Experimental waveform and (b) simulation waveform comparison

In simulation, the delay time, rising and falling slopes, and transition time don't match with the experiment. The parasitic ringing in simulation is excessive with mismatched amplitude, frequency and damping effect. All of the mismatches make it unable to predict the GaN HEMT's switching performance in good accuracy.

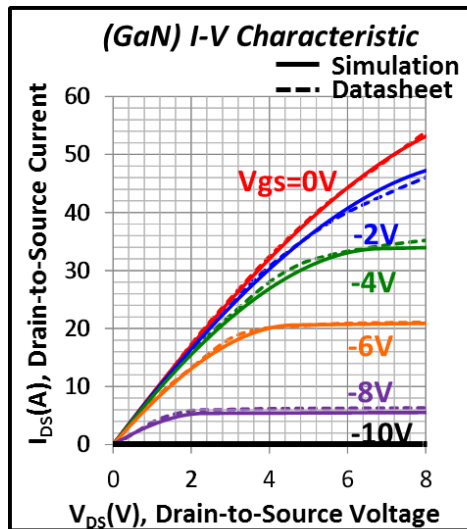
The simulation model modification starts from the basic characteristics of the device. In order to make it more clear, the lumped SPICE code is separated into to independent model so that the Si MOSFET and GaN HEMT can be evaluated separately.



(a)



(b)

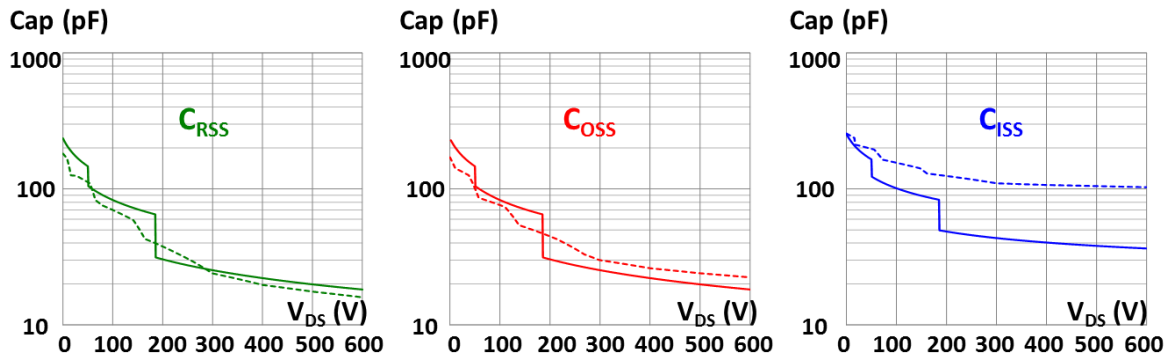


(c)

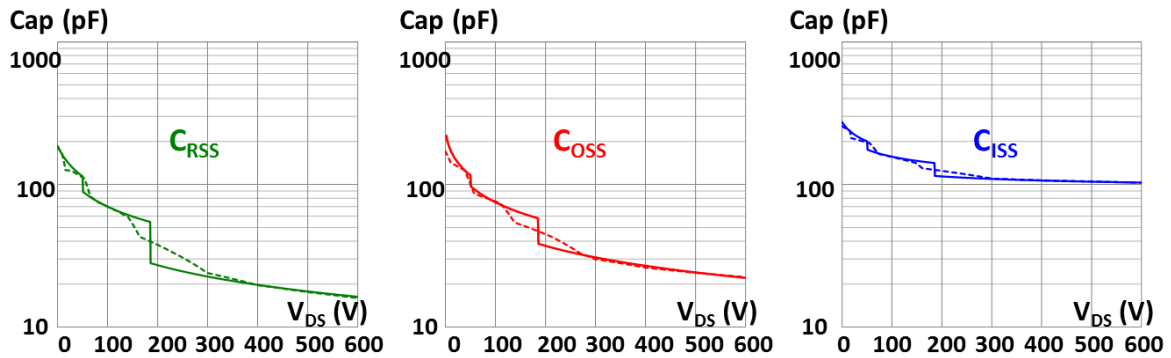
Figure 2.2 Simulation model verification (a) I-V of Si MOSFET, (b) C-V of Si MOSFET, and (c) I-V of GaN HEMT

Figure 2.2 is the I-V characteristic and the C-V characteristic of the Si MOSFET, and the I-V characteristic of the GaN HEMT. The accuracy is verified by comparing the simulated curves with measurements or datasheets.

The first mismatch is found in the C-V characteristic of the GaN HEMT as shown in Figure 2.3. All of the three most important non-linear parasitic capacitance is closer to the datasheet after proper modification on the initial value and non-linearity coefficient.



(a)



(b)

Figure 2.3 C-V characteristic (a) before modification and (b) after modification. (solid line is from simulation, dashed line is from datasheet, all curves are obtained under  $V_{GS}=-24V$ )



Besides the not accurate C-V curves, another important issue is the simulation model lacks accurate package parasitic inductance, which is of major importance to describe the dynamic characteristic of the device.

Figure 2.4 shows the typical bonding diagram of the cascode GaN HEMT in a traditional TO-220 package and its corresponding schematic. Inside the cascode package, the 600V depletion mode GaN die is on the right hand side of the lead frame, while the 30V Si MOSFET die is on the left hand side of the leadframe and mounted on a direct-bond-copper (DBC) substrate. Wire bonding process is used to achieve necessary electric connections.

According to Figure 2.4 (b), it is clearly that many parasitic inductors are introduced due to the inter-connections between the GaN die and the Si die, and between the dies and the lead frame. Moreover, as the currents with fast transitions are confined in such a small area, the coupling effects between different conductors are significant. The mutual inductances of  $L_{int1}$  with the other inductors are labeled in Figure 2.4 (b).

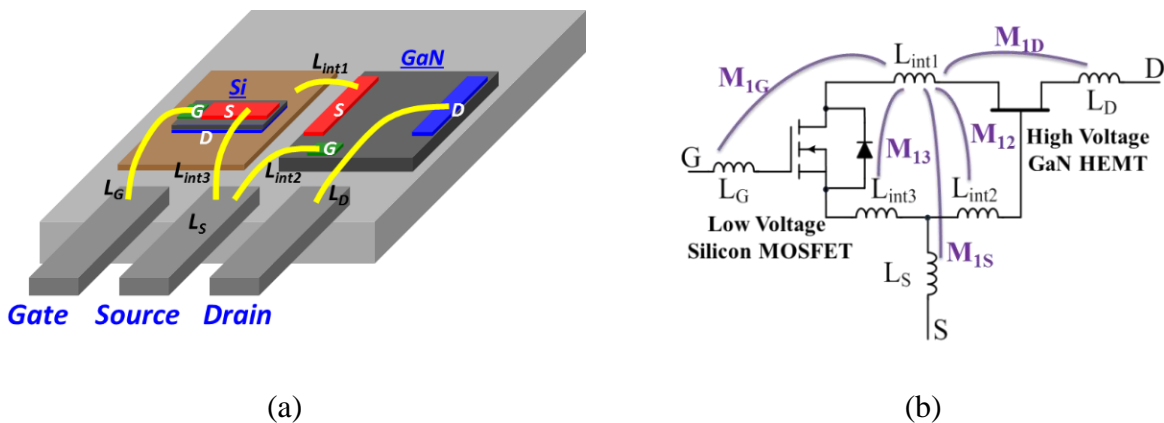


Figure 2.4 TO-220 cascode GaN HEMT package (a) bonding diagram and (b) schematic

The extraction of package parasitic inductance is implemented by Ansoft Q3D Extractor FEA simulation. According to electromagnetic theory, many parameters, like the dimensions, the positions, and the current directions of the conductors, have a significant effect on self-inductance and mutual-inductance. Among these factors, the dimensions and positions of the conductors can be determined based on the device bonding diagram. However, the current directions are sensitive and important, but difficult to define correctly, which will determine the polarity of coupling coefficient and thus have a significant impact. For devices working in switch mode, it is critical to verify the current paths and differentiate parasitic inductance in turn-on and turn-off conditions. However, such criteria are often neglected

To be specific, Figure 2.5 shows a cascode GaN HEMT that is assumed to be working as an active switch in a switch-mode power supply. The blue loop, the red loop, and the green loop represent device's power loop, Si MOSFET driving loop, and GaN HEMT driving loop, respectively. The arrows indicate the current directions of each loop. During turn-on and turn-off transitions, the power loop maintains its direction; the two driving loops change their directions instead. Another important assumption is that when a conductor involves in more than one loop, the specified current direction follows the current direction in the power loop. According to these criteria, the current direction of each conductor can be determined. The inductances can then be accurately extracted by solving Maxwell equations in the FEA simulation, which are shown in Table 2.1. Different values are applied when simulating different switching transition.

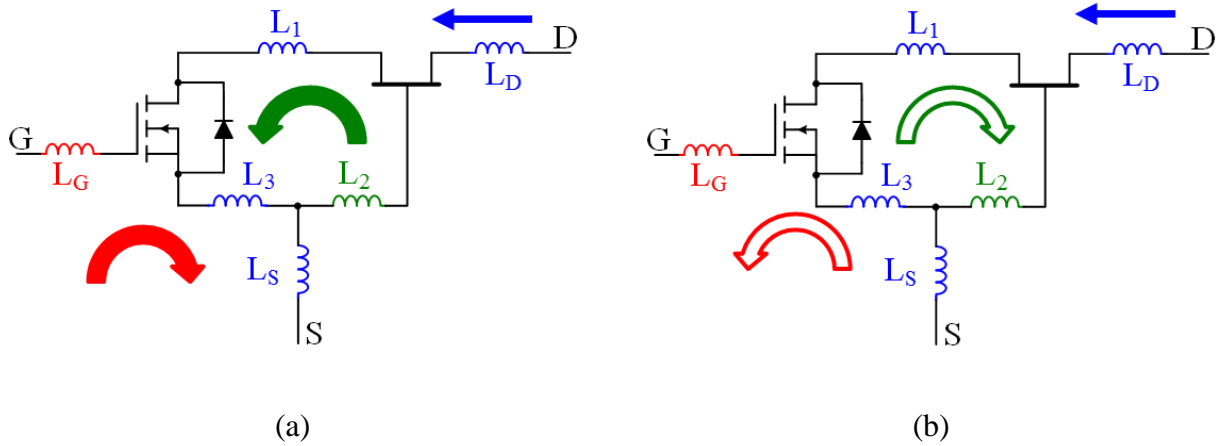


Figure 2.5 Current directions of conductors in cascode package during turn-on and turn-off

Table 2.1 Package parasitic inductance extracted by Ansoft Q3D FEA simulation

Self+Mutual	Turn On	Turn Off
$L_1 + \Sigma M_{1x}$	0.27 nH	0.26 nH
$L_2 + \Sigma M_{2x}$	0.23 nH	0.17 nH
$L_3 + \Sigma M_{3x}$	0.24 nH	0.43 nH
$L_S + \Sigma M_{Sx}$	0.57 nH	0.89 nH
$L_G + \Sigma M_{Gx}$	2.87 nH	3.12 nH
$L_D + \Sigma M_{Dx}$	1.89 nH	1.62 nH

It is important to point out that in this table, the effective parasitic inductance is the sum of self-inductance and mutual-inductance. The coupling effect leads to significant different for several parasitic inductance like  $L_3$  and  $L_S$ , which are proved to be most critical common source inductance and have significant impact on the switching behavior of the cascode GaN HEMT in the next Chapter.

## 2.2 Double Pulse Test and Simulation Model Verification

In order to verify the accuracy of the GaN HEMT simulation model, a double-pulse tester (DPT) is carefully designed and built with minimized parasitics as the test circuit to reveal the

intrinsic switching performance of the device. The reason why DPT is used for simulation model verification is because the DPT can built up testing circuit to required steady state quickly without thermal limitation. With DPT, extreme testing condition is able to be measured, and high bandwidth current shunt with strict thermal limit can be adopted to improve measurement accuracy. This is especially important to characterize the ultra-high speed switching performance of the cascode GaN HEMT.

Figure 2.6 shows the DPT schematic, PCB layout, and prototype. In this DPT, the 600V cascode GaN HEMT, also referred to DUT (device under test), is placed as the low side switch so that all signals are referenced to the ground and high bandwidth passive probes can be used for measurement; the high side switch is a 600V GaN Schottky diode is used as the free-wheeling diode. It almost eliminates the reverse-recovery effect, and thus won't cause extra current overshoot and switching loss during the turn-on transition of the DUT. A high bandwidth current shunt is used to measure the current waveform of the DUT. Both current shunt and DUT is referenced to the ground so that no differential probe, usually has lower bandwidth, is in need.

In the DPT design, the critical loop is the high frequency commutation loop starting from the input capacitor, through the top switch and the bottom switch returning to the input capacitor (as the loop inclosed by the yellow curve). When doing layout, the design principle is to minimize the loop inductance introduced by PCB trace. With optimized layout, the loop inductance is as low as 3.6nH as shown in Figure 2.6 (b).

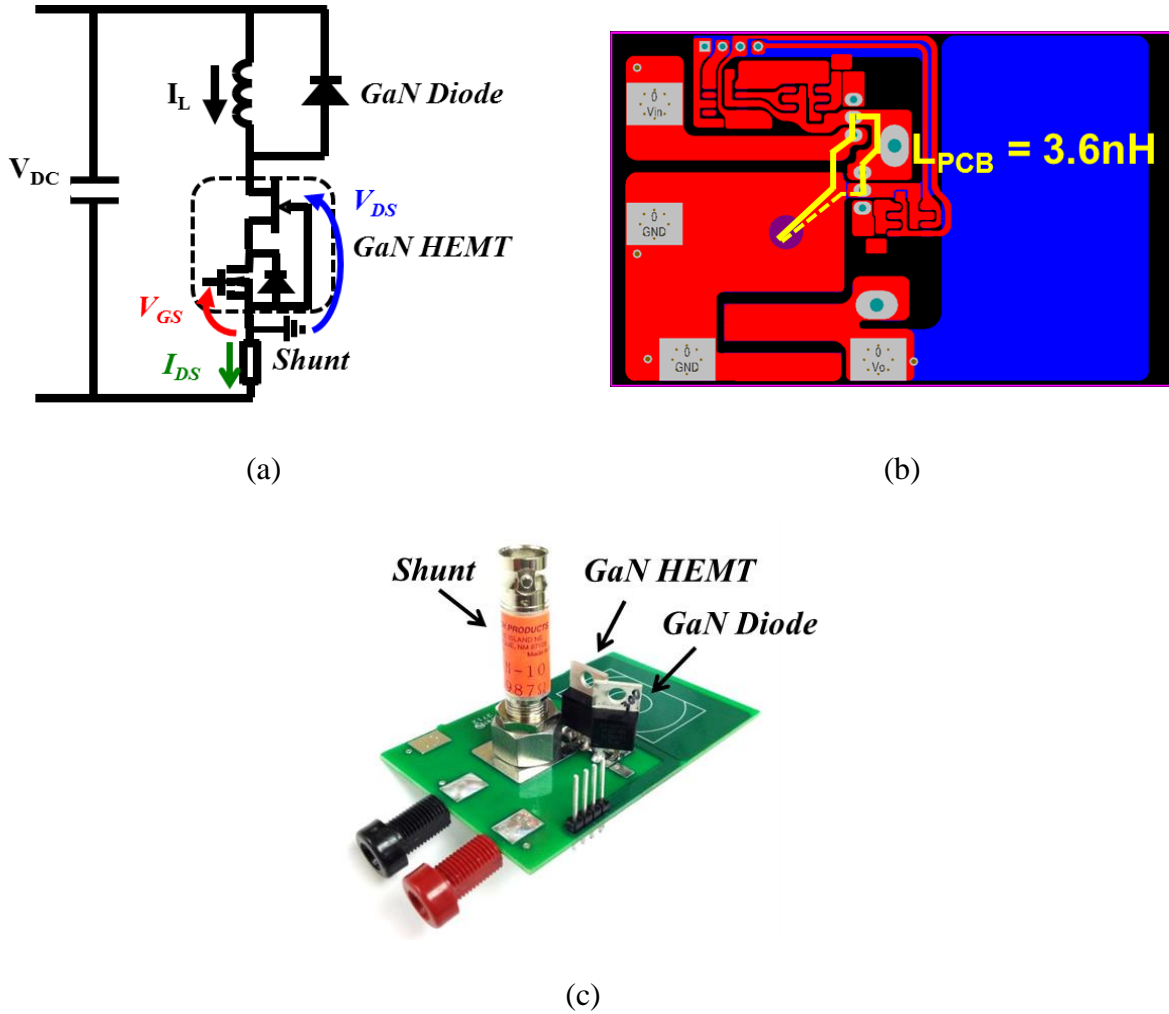


Figure 2.6 Double-pulse-tester (a) schematic, (b) layout, and (c) prototype

Figure 2.7 illustrates the parasitic inductance extraction of the PCB. Ansoft Q3D is used in this thesis to conduct FEA simulation. In general there are three steps. The first step is PCB file importation as shown in Figure 2.7 (a) and (b). The copper traces, holes and vias are imported into Q3D layer by layer to make sure they are exactly the same as in the Altium Designer. Then the second step is assembly as shown in Figure 2.7 (c). Different layers are all aligned according to one reference coordinate so that the relative position of every conductor pieces are accurate. The thickness of copper trace and the distance between each layer are also clearly defined according to real manufacture parameters. The last step is net list and excitation assignment. Any

conductors, including copper traces, holes and vias, physically connected are combined as one entity. Then one sink and one source are defined according to real working condition of the PCB to make sure all simulated self-inductance and mutual-inductance have clear physical meaning.

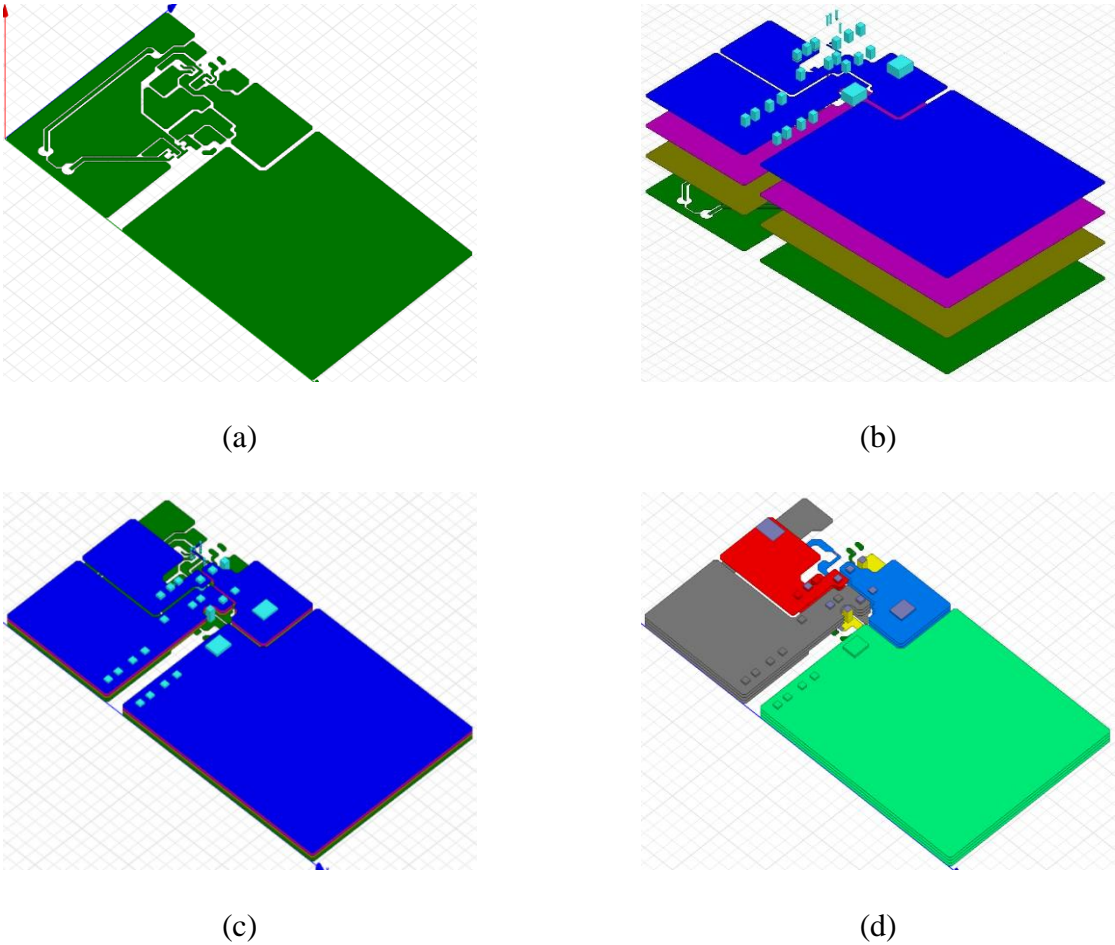


Figure 2.7 PCB parasitic inductance extraction process

To prove the developed cascode GaN HEMT simulation model is accurate, each part of the DPT should also be modelled accurately. An accurate model for the GaN Schottky diode is also provided by device manufacturer, as shown in Figure 2.8. The package parasitic inductance is extracted as 1.8nH. Both the simulated I-V characteristics and the simulated C-V characteristics are matching with its datasheet.

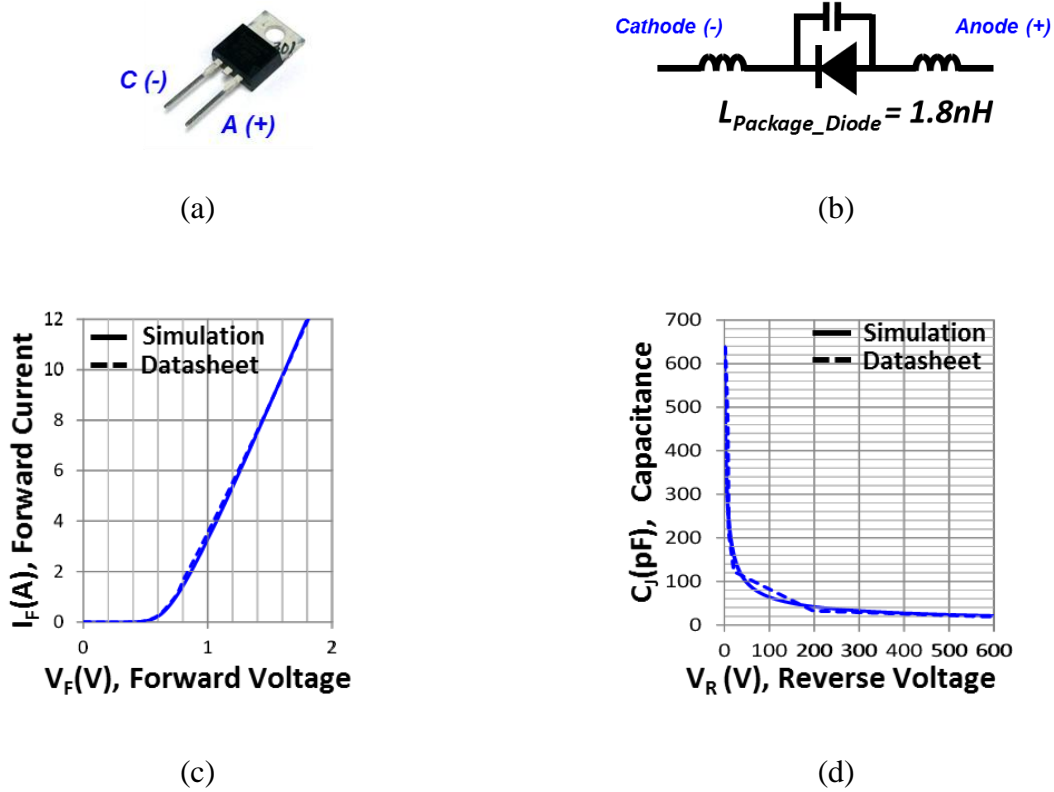


Figure 2.8 600V GaN Schottky diode (a) package, (b) model, (c) I-V curve, (d) C-V curve

The current waveform of the DUT is measured by a coaxial current shunt (part number SSDN-10) manufactured by T&M Research Products Inc., which has accurate resistance, small parasitic inductance, and high bandwidth. Table 2.2 shows the electrical characteristic specifications [9] of the current shunt. The operation principle of the current shunt is elaborated in [10]. Following the same modeling method discussed in [10], the current shunt is modeled by the circuit shown in Figure 2.9. Both of the parasitic inductances are measured by an Agilent 4294A impedance analyzer with proper adaptors.

Table 2.2 Electrical specifications of the coaxial current shunt

Part Number	Resistance	Bandwidth	P <sub>MAX</sub>	E <sub>MAX</sub>
SSDN-10	0.10 ohms	2000 MHz	2 W	2 J

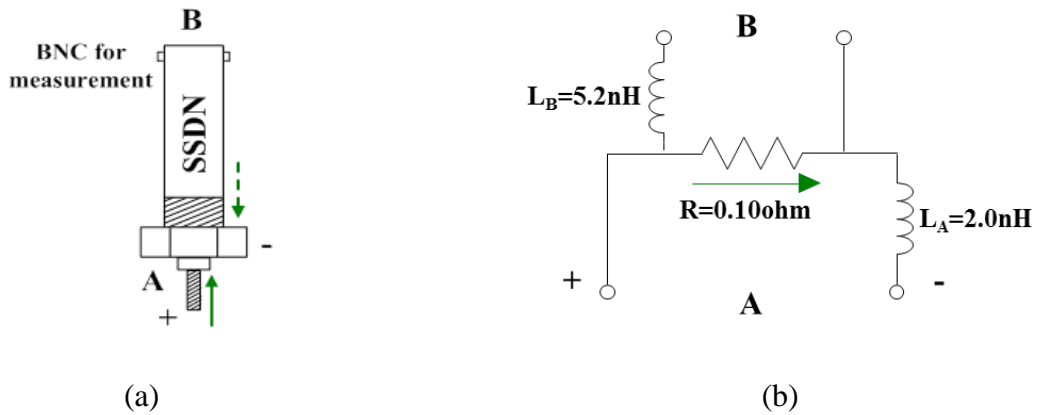


Figure 2.9 High bandwidth coaxial current shunt (a) prototype, (b) model

The secret of the high bandwidth is the shunt resistor is like an inductor-less resistor. Neither  $L_A$  nor  $L_B$  decide the bandwidth, because  $L_A$  is not in the measurement loop while  $L_B$  is not in the main current path. The bandwidth is actually decided by the parasitic inductance shared the two loops which is as small as tens of pH.

The selection of the current shunt is also a trade-off. A current shunt with larger resistance also has larger size so that the inductance introduced to the original power loop is too high. While a current shunt with smaller resistance has reduced magnitude on measured signal and smaller bandwidth which finally leading to less measurement accuracy. A proper current shunt is another key factor for accurate device characterization by DPT.

The model of the current shunt is verified by matching the impedance with the measurement results by impedance analyzer. Figure 2.10 shows that the model matches well with measurement in terms of both magnitude and phase.



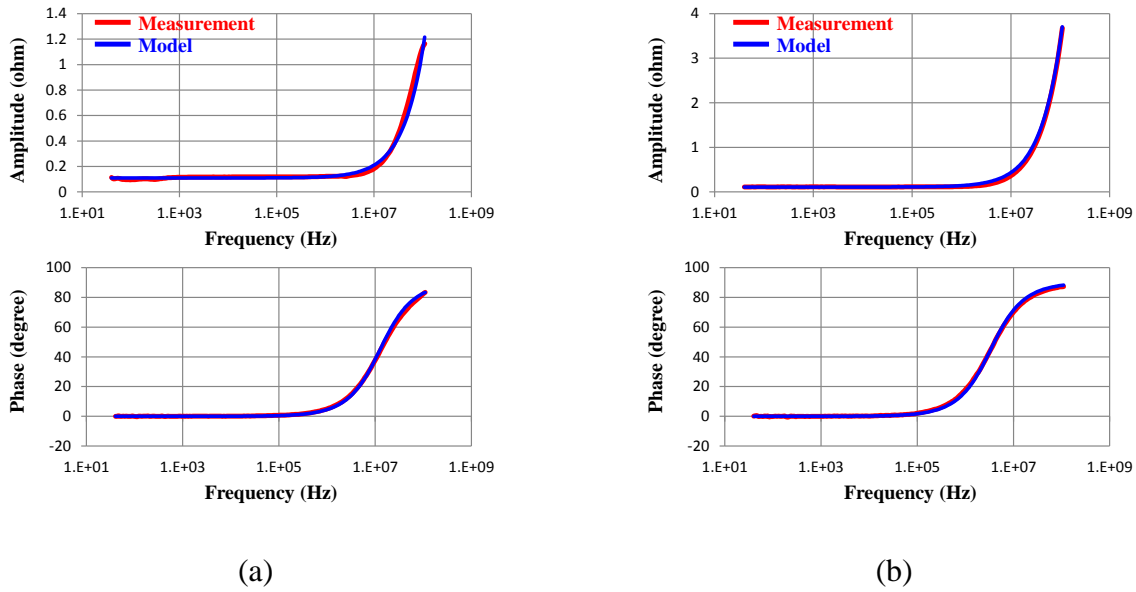


Figure 2.10 Current shunt impedance (a) terminal A, (b) terminal B

After each part of the DPT is well modelled, a series of double pulse tests are conducted to verify the simulation model and to analyze the switching performance of the cascode GaN HEMT. Figure 2.11 shows a typical waveform of the double pulse test. During the first pulse, the inductor current is quickly built up to the required current level. Then at the end of the first pulse, the turn-off transition is measured. Some dead time are applied between the first pulse and the second pulse so that the parasitic ringing is well damped. The dead time is also short enough so that the inductor current free-wheeling through the diode is almost the same before the second pulse. Then at the beginning of the second pulse, the turn-on transition is measured.

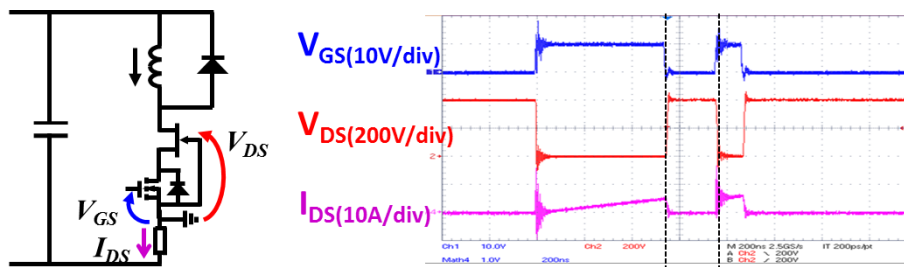


Figure 2.11 Double pulse test typical waveform

Zoom-in waveforms showing detailed switching transition process are listed in Figure 2.12.

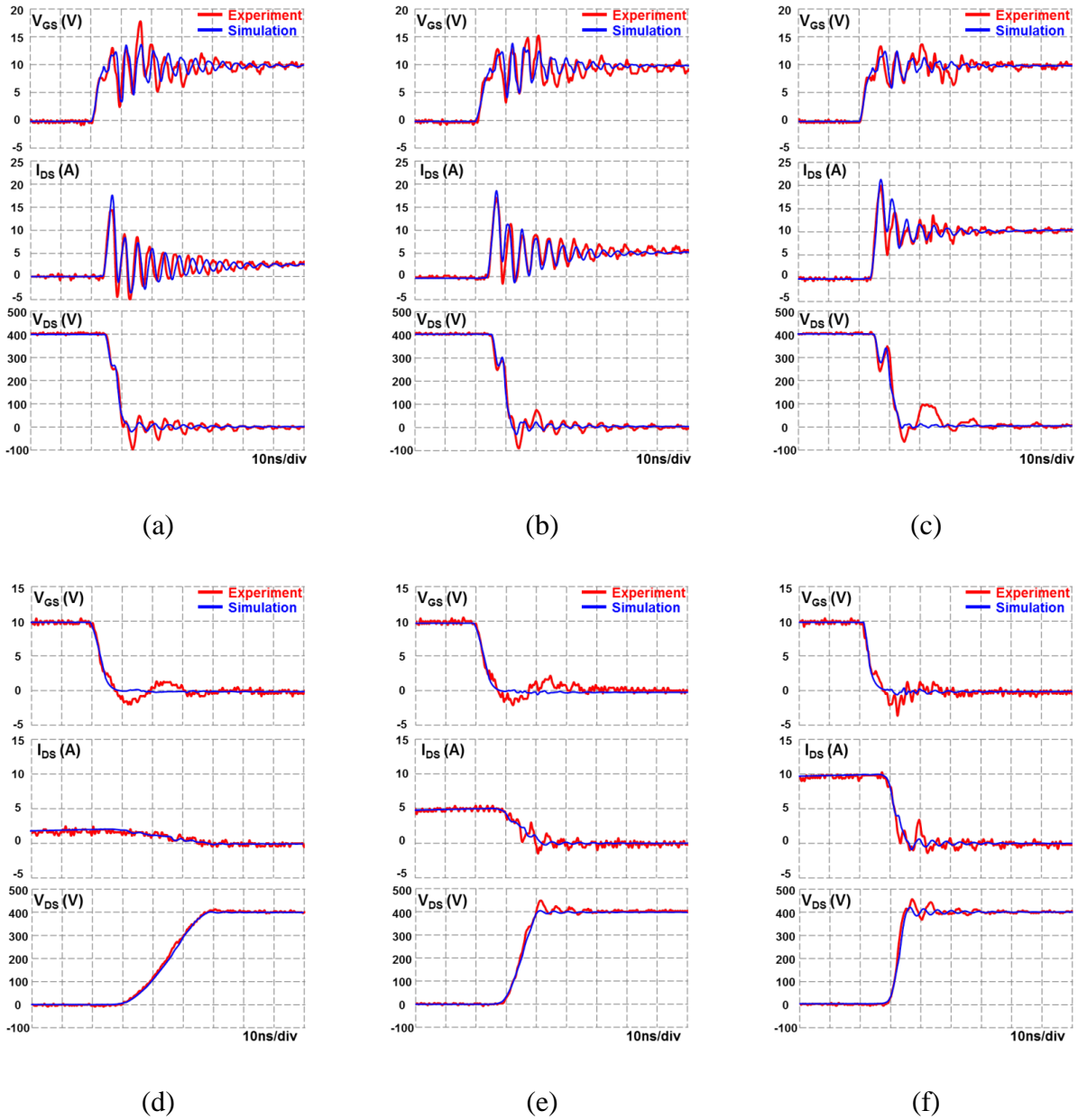


Figure 2.12 Zoom-in switching transition waveforms (a) 400V/2A turn on; (b) 400V/5A turn on; (c) 400V/10A turn on; (d) 400V/2A turn off; (e) 400V/5A turn off; (f) 400V/10A turn off;

The accuracy of the cascode GaN HEMT simulation model is first verified by comparing simulation waveforms with experimental waveforms. The simulation match well with

experiment in terms of switching transition time sequence, rising/falling slope, frequency, magnitude and phase of the parasitic ringing.

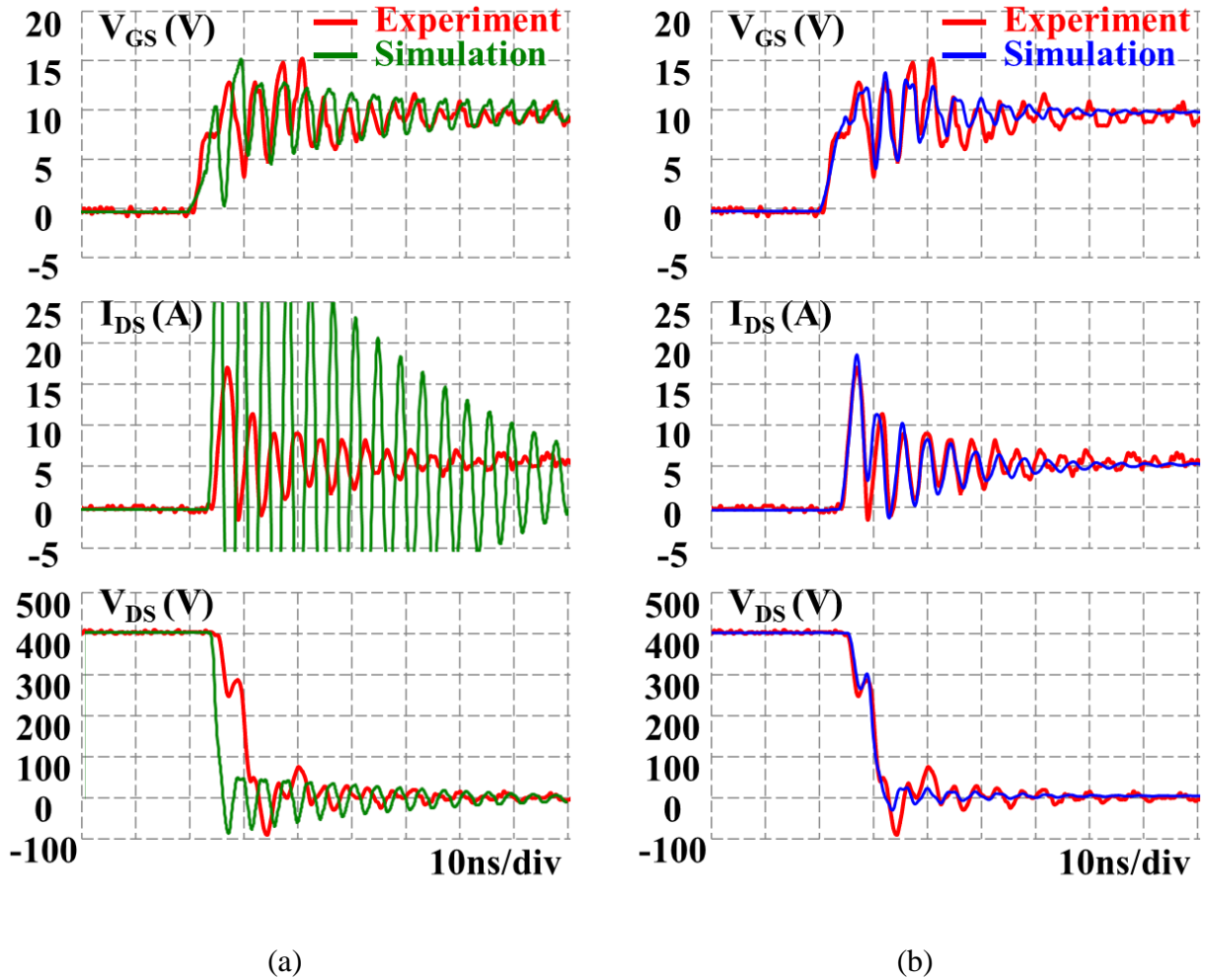


Figure 2.13 Simulation model comparison (a) before modification and (b) after modification (turn on waveforms under 400V/5A condition)

When comparing the simulation waveform before and after modification, the accuracy improvement is prominent. Both Figure 2.13 and Figure 2.14 indicate that the previous simulation model without modification has big mismatch with experiment, while the modified simulation model can predict the real switching performance of the GaN HEMT in high accuracy.

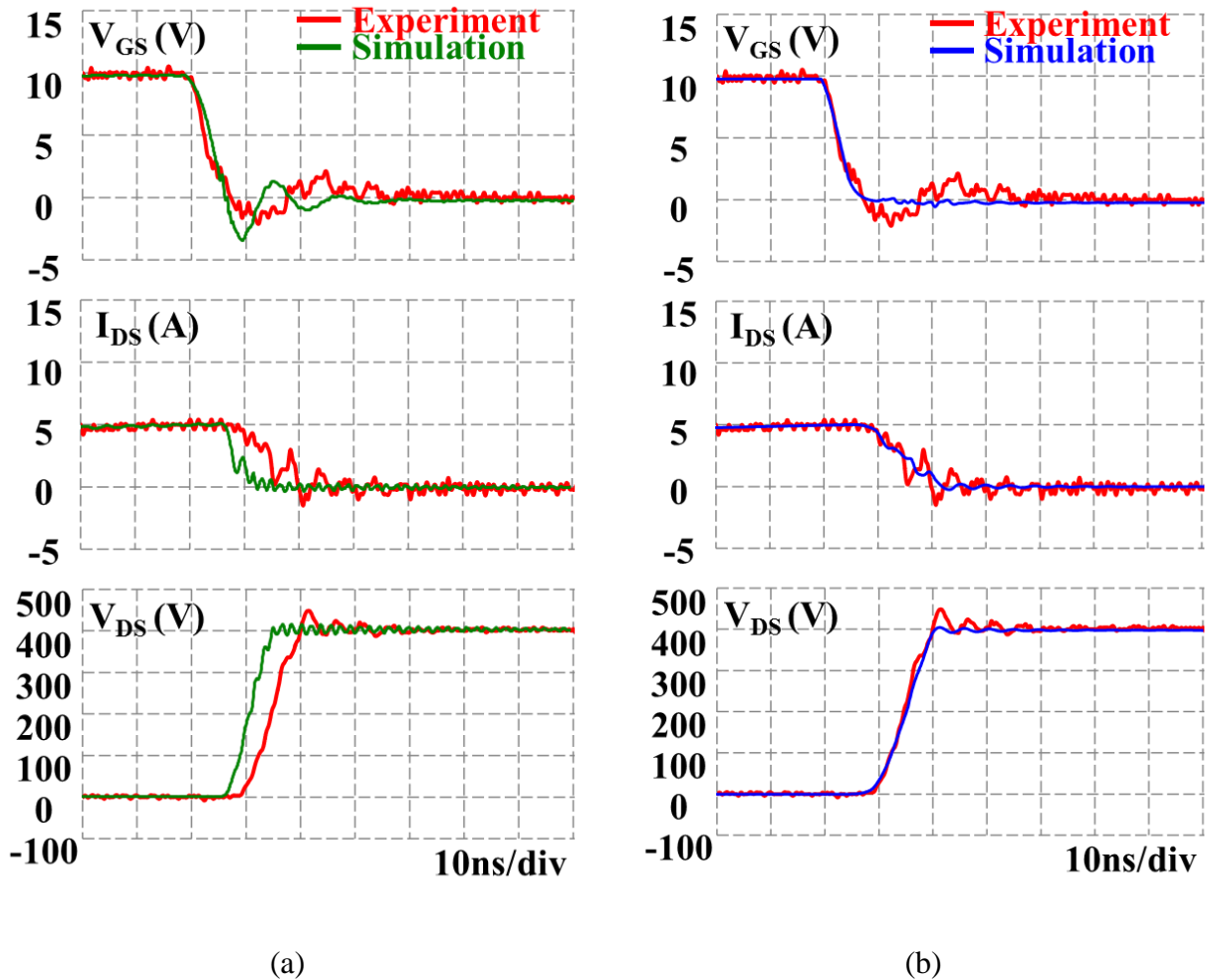


Figure 2.14 Simulation model comparison (a) before modification and (b) after modification (turn off waveforms under 400V/5A condition)

Based on the switching waveforms, the switching energies can be defined and calculated. The turn-on energy ( $E_{ON}$ ) and turn-off energy ( $E_{OFF}$ ) are defined as the energies dissipated on the switch during turn-on transition and turn-off transition. Figure 2.15 shows the calculation of  $E_{ON}$  based on the experimental waveforms of  $V_{DS}$  and  $I_{DS}$ . To be specific, the green curve is the product of  $V_{DS}$  and  $I_{DS}$  which is the instantaneous power dissipated on the device. Then the integral of the instantaneous power from  $t_1$  (the instant when  $I_{DS}$  starts to increase) to  $t_2$  (the instant when  $I_{DS}$  settled to steady state within 10% error band) is defined as  $E_{ON}$ .  $E_{OFF}$  is

calculated following the same method. In this way, the calculated switching energy will contain not only the main transition loss, which is usually the major part of switching loss, but also the ringing loss, caused by parasitic oscillation and is not negligible in this case, during the entire switching transition.

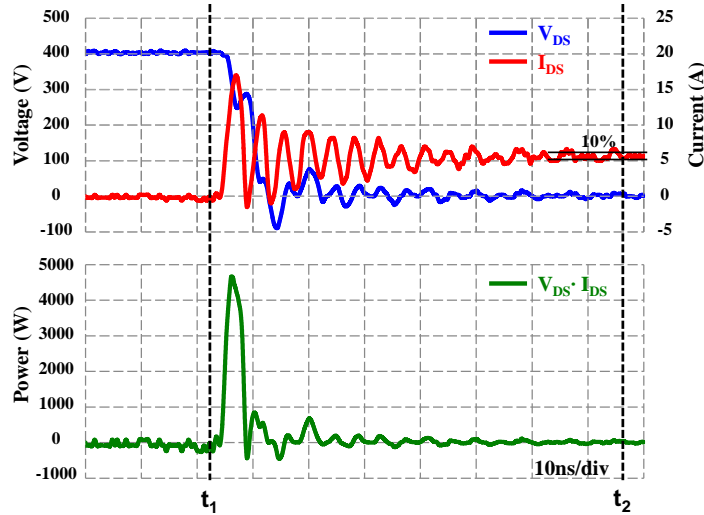


Figure 2.15 Calculation of turn-on energy

The switching energies in different load currents are measured and shown in Figure 2.16 (a). The results of the simulation also match well with experiments. It is a clear trend that the turn-on energy is much larger than the turn-off energy, which is due to severe current spikes and oscillations, in entire range of load current. This phenomenon is also observed in cascode SiC JFET [11]. In addition, the turn-on energy is a strong function of load current. In contrast, the turn-off energy is extremely small and almost constant under different load currents. This phenomenon is unique and related to the specialty of the cascode structure, which will be addressed in the next section.

The double pulse test is based on current waveform from device terminal. So the energy on  $C_{oss}$  is stored in turn off but dissipated during turn on. So the measured turn on energy is

underestimated compared to real turn-on loss while the turn off energy is overestimated compared to real turn-off loss.

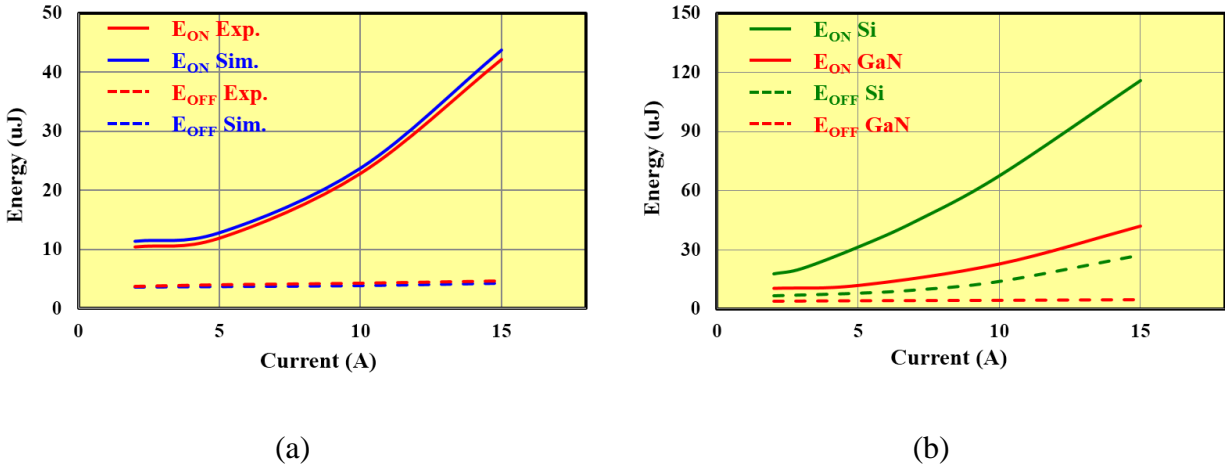


Figure 2.16 DPT switching energy comparison (a) experimental and simulation results of GaN, (b) comparison between GaN and Si

Compared to the state-of-the-art super junction Si MOSFET with similar voltage rating, current rating, and on resistance (part no. IPP60R160C6), the switching energy of the cascode GaN HEMT is significantly smaller as shown in Figure 2.16 (b). In addition, unlike the almost constant turn-off energy of GaN, the turn-off energy of Si MOSFET will increase with the turn-off current gradually.

The turn-on waveform comparison is shown in Figure 2.17. It can be observed that the  $dv/dt$  and  $di/dt$  of GaN is higher than Si MOSFET. Also the main transition time of GaN is significantly smaller than Si MOSFET so that the corresponding turn-on loss is much smaller. So at 400V and 10A turn-on condition, the turn-on time and turn-on energy of GaN is 10ns and 23.4uJ while that of Si is 22ns and 67.5uJ.

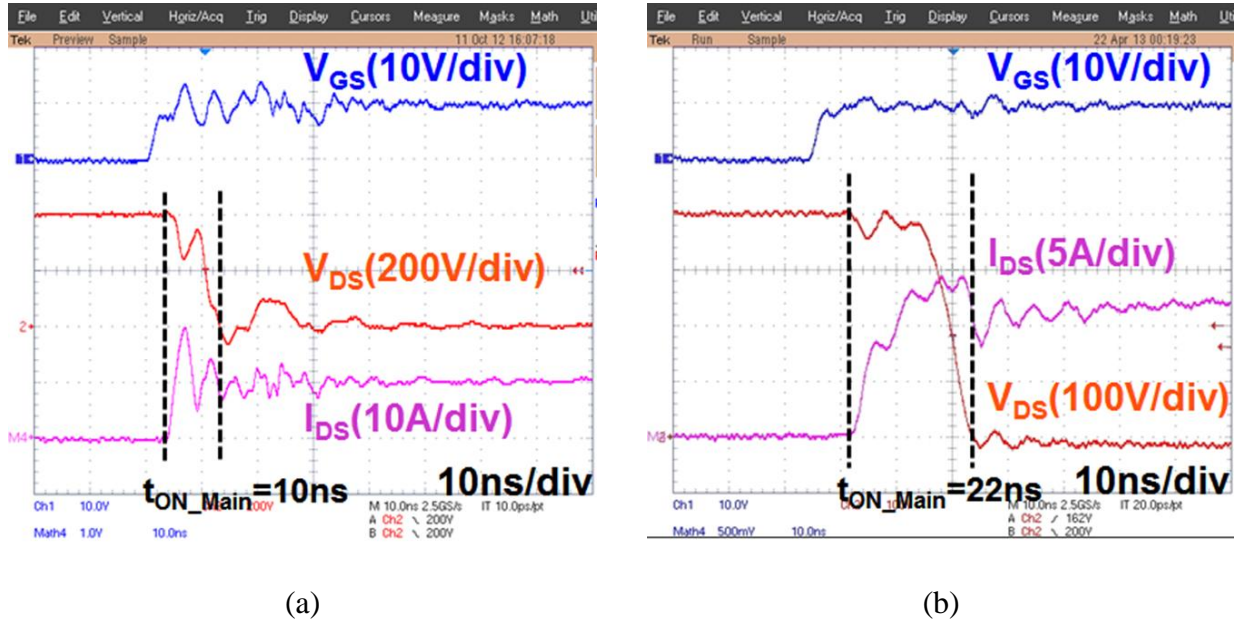
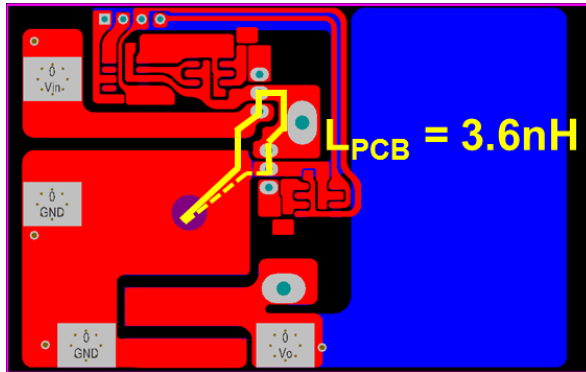


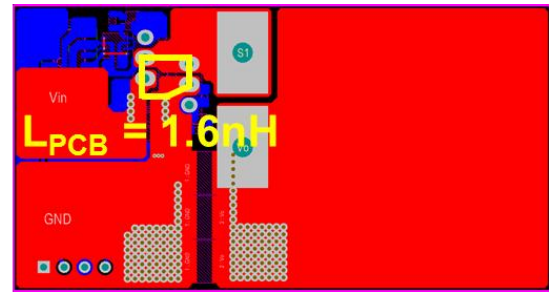
Figure 2.17 DPT turn-on waveform comparison between GaN and Si

Even the simulation model is verified by experiment, there is still another concern that whether the switching energy measured in a double pulse tester can reflect the real switching loss distribution in a buck converter or boost converter because in a real continuously working converter there is no bulky current shunt inserted in the critical power loop and the corresponding parasitic inductance could be very different. So the impact of current shunt should be evaluated.

In order to compare the impact of current shunt in terms of switching loss measurement, a traditional buck converter is built for comparison. The buck converter uses the same devices as the DPT, while loop inductance introduced by PCB can further be shrunk as the current shunt is removed. Figure 2.18 and Figure 2.19 show the comparison of PCB and schematic, respectively. Table 2.3 shows the comparison of parasitic inductance on the commutation loop. More than 30% total commutation loop inductance is saved in an optimized buck converter design than an optimized DPT design.

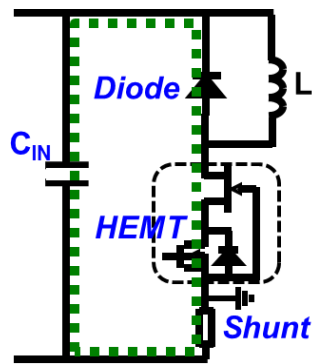


(a)

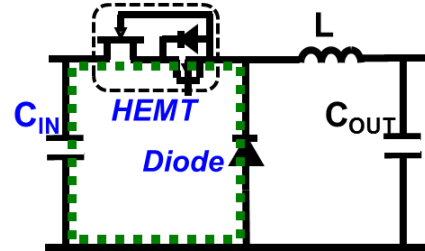


(b)

Figure 2.18 Layout comparison between (a) double-pulse tester and (b) buck converter



(a)



(b)

Figure 2.19 Schematic comparison between (a) double-pulse tester and (b) buck converter

Circuit simulations are conducted for both buck converter and DPT, and corresponding switching loss distributions are compared in Figure 2.20. As the buck converter has smaller loop inductance, higher turn-on loss and lower turn-off loss are observed. This trend is in accordance with the conclusions in [10]. However, the differences are not significant. Through this comparison, it can be concluded that under careful design, a double-pulse tester can reflect the trend of real switching loss distribution in a bridge configuration converter with small differences.



Table 2.3 Parasitic inductance comparison between DPT and Buck

	DPT	Buck
$L_{PCB}$	3.6 nH	1.6 nH
$L_{Cin\_Package}$	0.3 nH	0.3 nH
$L_{HEMT\_Package}$	3.0 nH	3.0 nH
$L_{Diode\_Package}$	1.8 nH	1.8 nH
$L_{Shunt\_Package}$	2.0 nH	-
Loop	10.7 nH	6.7 nH

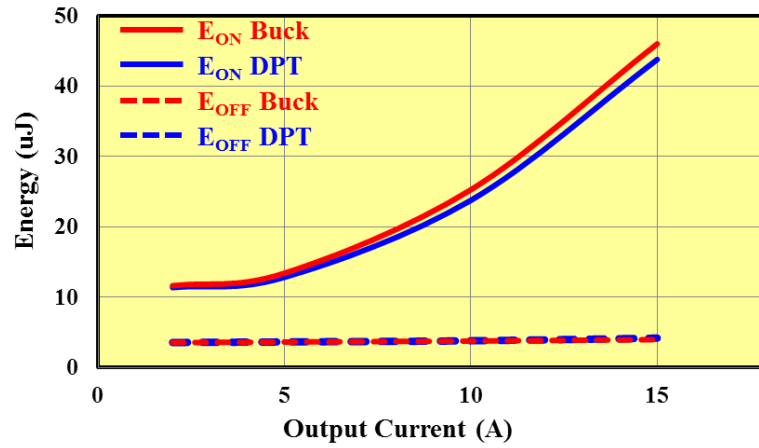


Figure 2.20 Switching energy comparison between DPT and Buck

### 2.3 Loss Mechanism Analysis and Loss Reduction via ZVS

After the development and verification of the simulation model, it can be used as a tool to analyze the switching performance of a given power converter. For the application of bi-directional battery charger/discharger, a 380V/200V bi-direction buck-boost converter is built with 600V cascode GaN HEMTs as both the top switch (TS) and the bottom switch (BS) (Figure 2.21). For TS driving, the ICs NCP5181 and ISL89163 are used in series; for BS driving only the

ISL89163 is used. The PCB is also carefully designed with minimized parasitic inductance of 1.6nH for the commutation loop and 3.3nH for the TS/BS driving loop.

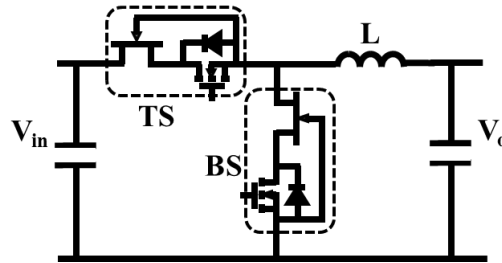


Figure 2.21 Bi-direction buck-boost converter schematic

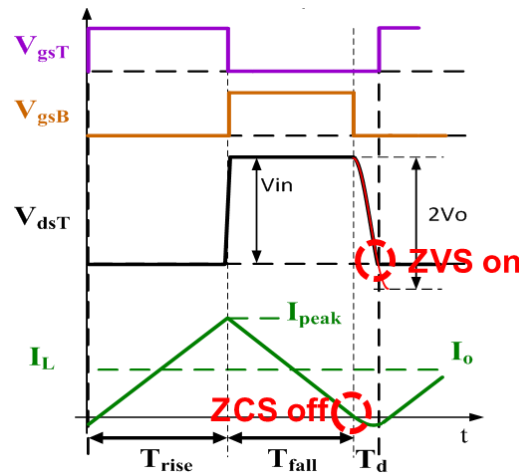


Figure 2.22 Critical conduction mode operation

Fixed frequency continuous-current-mode (CCM) is used for the hard-switching; the inductor peak-peak current ripple is 3A, which is 50% of the full load current. While variable-frequency critical conduction mode (CRM) is used for soft-switching demonstration; the CRM could achieve both ZVS turn-on of TS and ZCS turn-off of BS; the inductor peak-peak current ripple is more than twice the load current at any load conditions. The efficiency curves shown in Figure 2.23 (a) reveals a clear trend that soft switching is superior to hard switching in all load ranges tested.

Furthermore, a converter loss breakdown is conducted and shown in Figure 2.23 (b), in which the total inductor loss, including core loss and winding loss, are tested according to the methods proposed in [12]; the conduction loss and the switching loss are calculated by the developed simulation model.

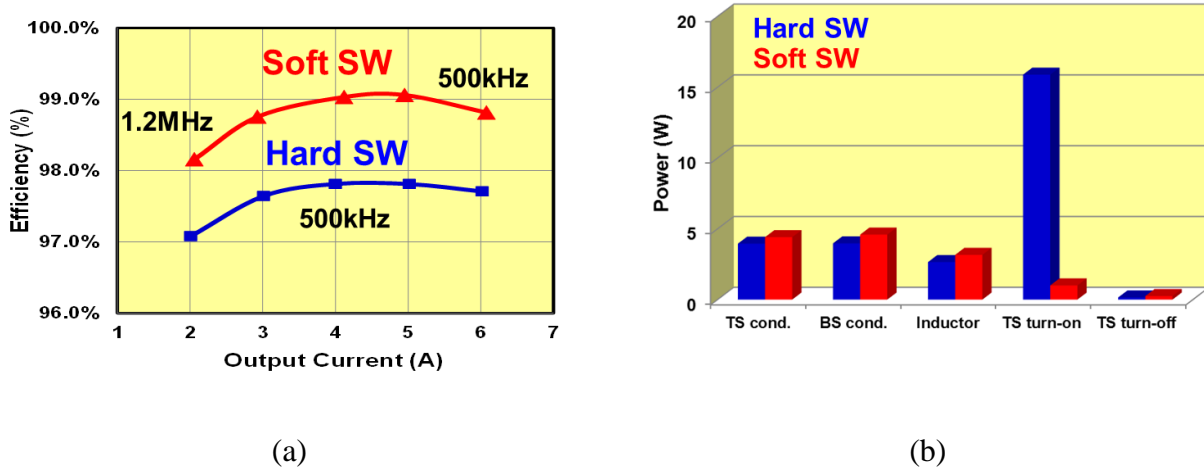


Figure 2.23 Comparison between hard switching and soft switching (a) Buck converter efficiency, (b) loss breakdown at full load

In hard-switching conditions, the TS turn-on loss is the dominant part of total loss. Figure 2.24 shows the corresponding TS turn-on waveforms. Even though the load current is only around 5A, the current overshoot reaches 25A peak value. This is due to the reverse-recovery effect and junction capacitor charging of the BS (highlighted by the red area). The crossover between the high-voltage and high-current overshoot results in a large turn-on loss. It can also be observed that the  $di/dt$  is about 3000A/us, which is much higher than the traditional 600V Si MOSFET. This high speed is due to the inherent characteristics of the GaN HEMT.

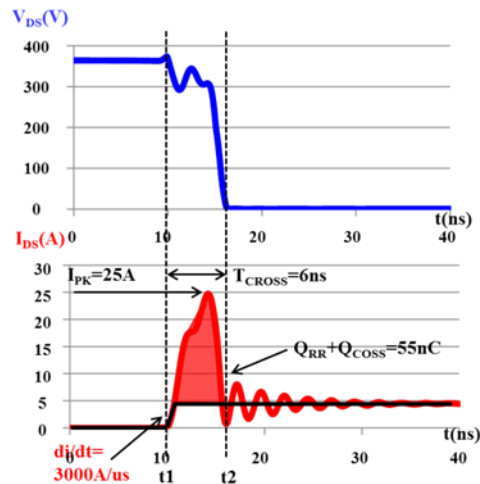


Figure 2.24 Buck converter TS turn-on waveforms at CCM hard-switching condition

When comparing hard switching with soft switching, the loss breakdown indicates that the TS turn-on loss is the dominant loss in hard-switching conditions, much larger than any other loss; this is why hard switching has much lower efficiency. In the soft-switching case, due to higher turn-off current and RMS current, the price paid is a little bit higher conduction loss, turn-off loss and inductor loss, while turn-on loss is eliminated as a trade-off. In total, soft switching benefits a lot in terms of efficiency.

Another important phenomenon observed from both the switching energy distribution and the loss breakdown is the turn-off loss is extremely small and not sensitive to the load current. Similar trend was also observed in cascode SiC JFET mentioned in paper [11]. So it seems a common phenomenon existing in cascode structure. Using both the simulation model discussed in this thesis and the analytical model proposed in paper [13], the current source turn-off mechanism, which accelerates the turn-off transition and reduces turn-off loss, is discovered.

Figure 2.25 introduces the basic concept of the ultra-fast turn-off transition in cascode structure by comparing the turn-off equivalent circuit between a normally-off GaN device and a cascode GaN device.

For a normally-off GaN device, during turn off process the inductor current charges the  $C_{GD}$ , which referred as miller capacitor, so that the charging current affects the external gate driver. This current is in the same direction with the driving current to turn off the device. So the result is the miller capacitor current reducing the driving capability of the driver and leading to a miller plateau with high turn-off loss.

On the contrary, for a cascode GaN device, the current charging the miller cap of the depletion mode GaN device flowing out of the device without affecting the gate driver. So the miller capacitor is charged by a current source and gate driver can turn-off the device as fast as possible. As a result, the corresponding turn-off loss is extremely small and not sensitive to the turn-off current.

The unique feature of the cascode GaN HEMT further justifies the application of CRM mode because ZVS eliminates the dominant turn-on loss while turn-off loss maintaining in low level with high turn-off current compared to CCM operation. Also due to the high current ripple, the RMS current increases at the same time. However, GaN device has smaller specific on-resistance making it less sensitive to conduction loss. The trade-off between switching loss and conduction loss is even different for GaN device than for Si device.

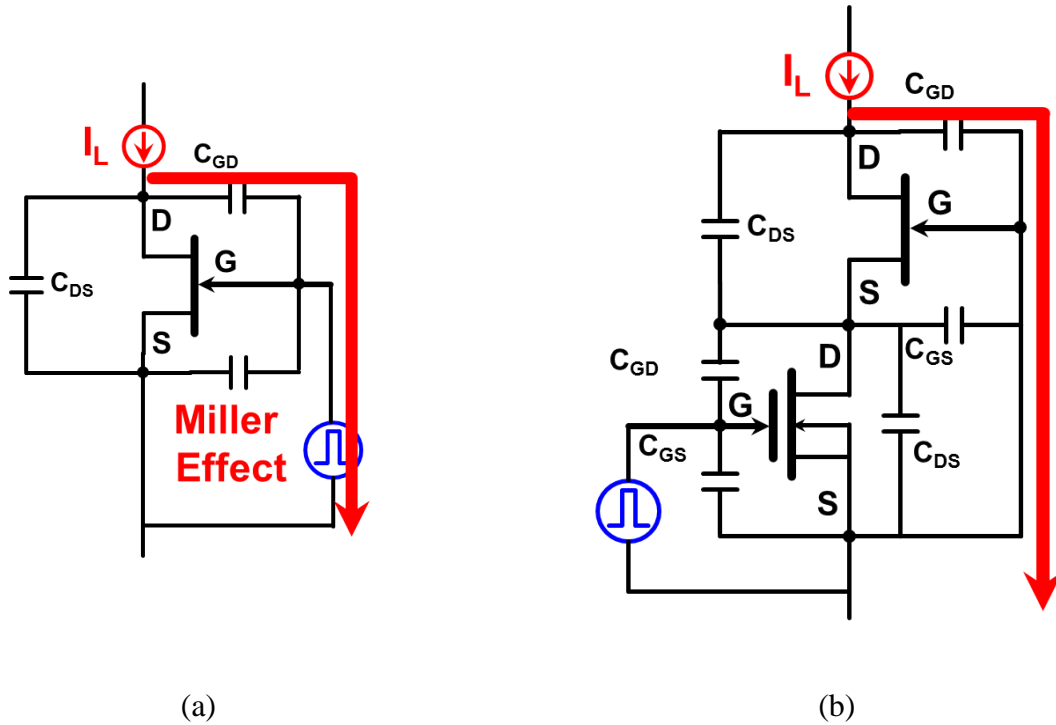


Figure 2.25 Turn-off equivalent circuit comparison (a) N-off GaN, (b) cascode GaN

With CRM operation and ZVS, high frequency and high efficiency are bale to be achieved at the same time. The switching frequency is further pushed to as high as 5MHz. Figure 2.26 shows the waveform at multi-MHz. For a 380V-200V, 600W output buck converter, 99% peak efficiency is still achieved at 5MHz.

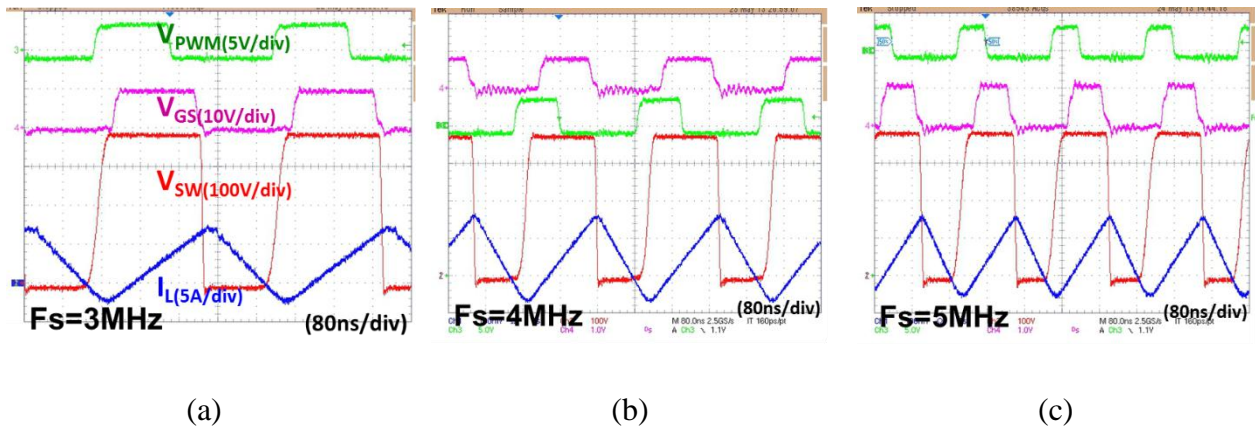


Figure 2.26 CRM buck waveforms at (a) 3MHz, (b) 4MHz, (c) 5MHz

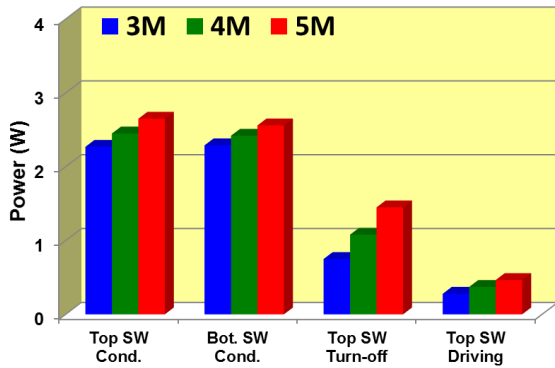


Figure 2.27 Loss breakdown at 3-5 MHz

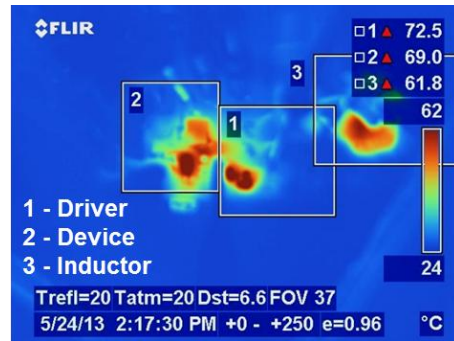


Figure 2.28 Thermal image at 5MHz

The loss breakdown shows that switching related loss are still very small. While thermal image further demonstrates that the temperature of the GaN device is well under control. The higher case temperature is  $72.5^{\circ}\text{C}$ . So the estimated junction temperature is below  $85^{\circ}\text{C}$  leaving enough safety margin.

In summary, CRM mode soft switching benefits the cascode GaN HEMT. Multi-MHz frequency operation is achieved with 99% peak efficiency. Further pushing frequency and power is possible but limited by current packaging design which is illustrated in the next chapter.

## Chapter 3. Packaging Impacts and Stack-Die Package

### 3.1 Common Source Inductance of Cascode GaN Package

Due to the merits of the cascode GaN HEMT, the device is able to switch at very fast speed. However, as a result of the parasitics introduced by the bulky package, large switching losses and severe oscillations are observed during the switching transitions, which definitely limit the switching performance of the device, and cause potentially more electro-magnetic interference (EMI) for none-optimum circuit designs.

Regarding packaging influence study, many efforts are spent on the Si MOSFET with a single switch structure [14-16]. It is a common sense that the common-source inductance (CSI), which is defined as the inductance shared by power loop and driving loop, is the most critical parasitics. The CSI acts as negative feedback to slow down the driver during the turn-on and turn-off transitions, and thus prolongs the voltage and current crossover time, and significantly increases the switching loss.

Recently, there have been some publications discussing the package influence for wide-band-gap devices, like the high-voltage SiC MOSFET and low-voltage GaN HEMT [7], [10]. The devices also use a single-switch structure, and therefore the conclusions are similar to that of the Si MOSFET, in which the CSI still has major impact on the device's switching loss. However, due to the uniqueness of the cascode structure, the definition of the CSI is not straightforward. So far there have been few paper addresses this issue. In this thesis, the analysis starts from the identification of critical parasitic inductance.



Following the same definition of CSI in a single-switch structure, the CSI of the low-voltage Si MOSFET and of the high-voltage GaN HEMT are analyzed. From the perspective of the Si MOSFET (Figure 3.1(a)), the blue loop is the power loop and the red loop is the driving loop. It is clear that  $L_{int3}$  and  $L_S$  are shared by the two loops, so they are the CSIs of the Si MOSFET. Similarly, from the perspective of the GaN HEMT (Figure 3.1(b)), the blue loop is still the power loop, but the driving loop is changed to the green loop. As a result,  $L_{int3}$  and  $L_{int1}$  are the CSIs of the GaN HEMT.

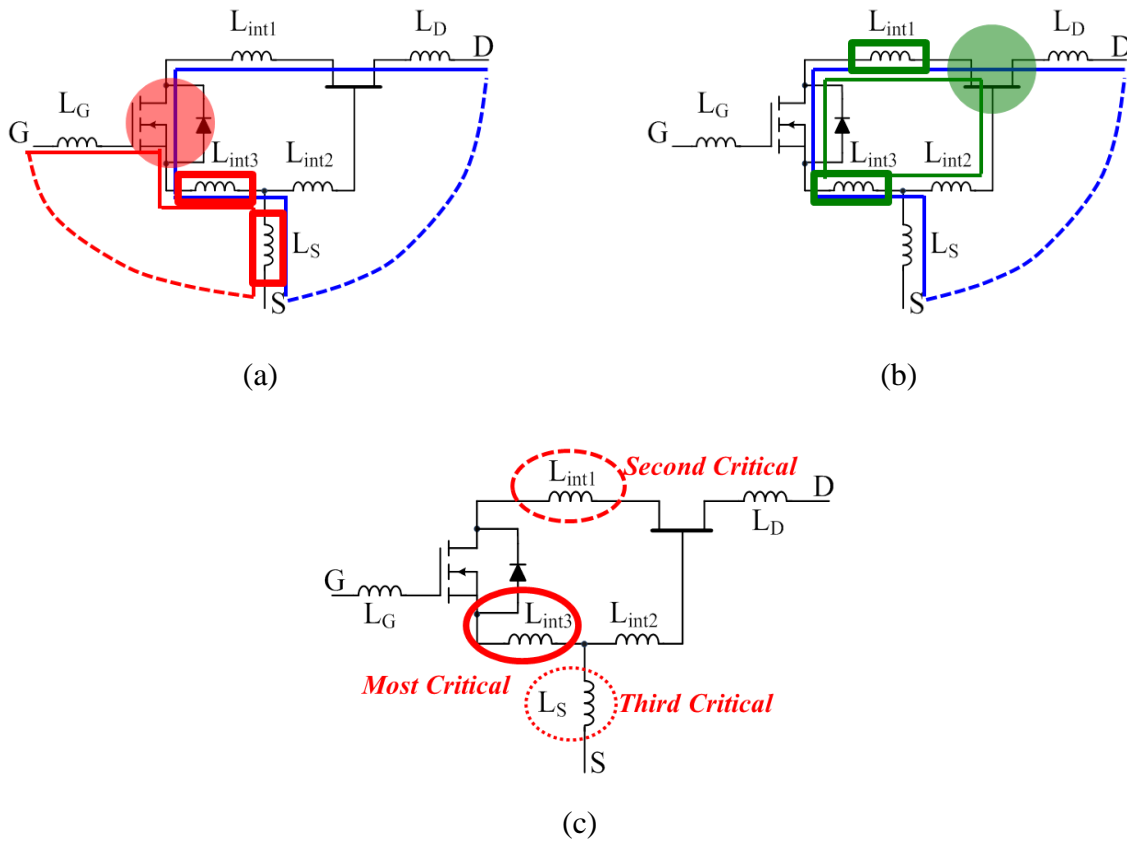


Figure 3.1 Common source inductance in cascode package (a) Si's perspective, (b) GaN's perspective, (c) for cascode structure

Therefore, in terms of the cascode structure (Figure 3.1(c)), since  $L_{int3}$  is the CSI for both the GaN HEMT and the Si MOSFET, it should be the most critical parasitic inductance.  $L_{int1}$  is estimated to be the second-most critical inductance, since it is the CSI of the high-voltage GaN HEMT, which has the major switching loss. Last but not least,  $L_S$  is predicted to be the third-most critical inductance.

After theoretical analysis, the simulation model is used to verify the predictions. A circuit-level simulation is conducted based on a buck converter design working in the continuous-current-mode hard-switching condition. The switching loss during the hard-switching condition is the major concern. Since the turn-on switching loss is the dominant part, the turn-on energy at 400V/10A condition is chosen for comparison. A series of simulation waveforms is shown in Figure 3.2, in which the simulation results based on the TO-220 package is always set as the benchmark (red line), while each comparison case (blue line) removes one of the six parasitic inductance to evaluate the impact of that specific parasitic inductance.

By comparing waveforms, the different impacts of each parasitic inductance can be observed. Without  $L_D$  or  $L_{int2}$ , the waveforms have almost no difference; without  $L_G$ , there is an obvious forward phase shift for  $I_{DS}$  and  $V_{DS}$ ; however, in terms of turn-on energy, there is still no significant difference. In contrast, when without  $L_S$ ,  $L_{int1}$  or  $L_{int3}$ , the  $I_{DS}$  has higher overshoot, while the  $V_{DS}$  has sharper falling edge compared to the benchmark; thus shorter transition times and smaller turn-on energies are observed in these three cases.

For better quantitative comparison, the simulated turn-on switching loss is shown in Figure 3.3. Based on the TO-220 package case, the total turn-on energy is 23.6 $\mu$ J at 400V/10A condition, which is set as the benchmark. By eliminating the impact of  $L_D$ ,  $L_{int2}$  or  $L_G$ , the reduction of turn-on switching loss is negligible (around 1% of 23.6 $\mu$ J). On the other hand, when

the critical parasitic inductance like  $L_S$ ,  $L_{int1}$  or  $L_{int3}$  is removed, the turn-on switching loss will reduce significantly (9%, 15%, and 22% of 23.6uJ respectively).

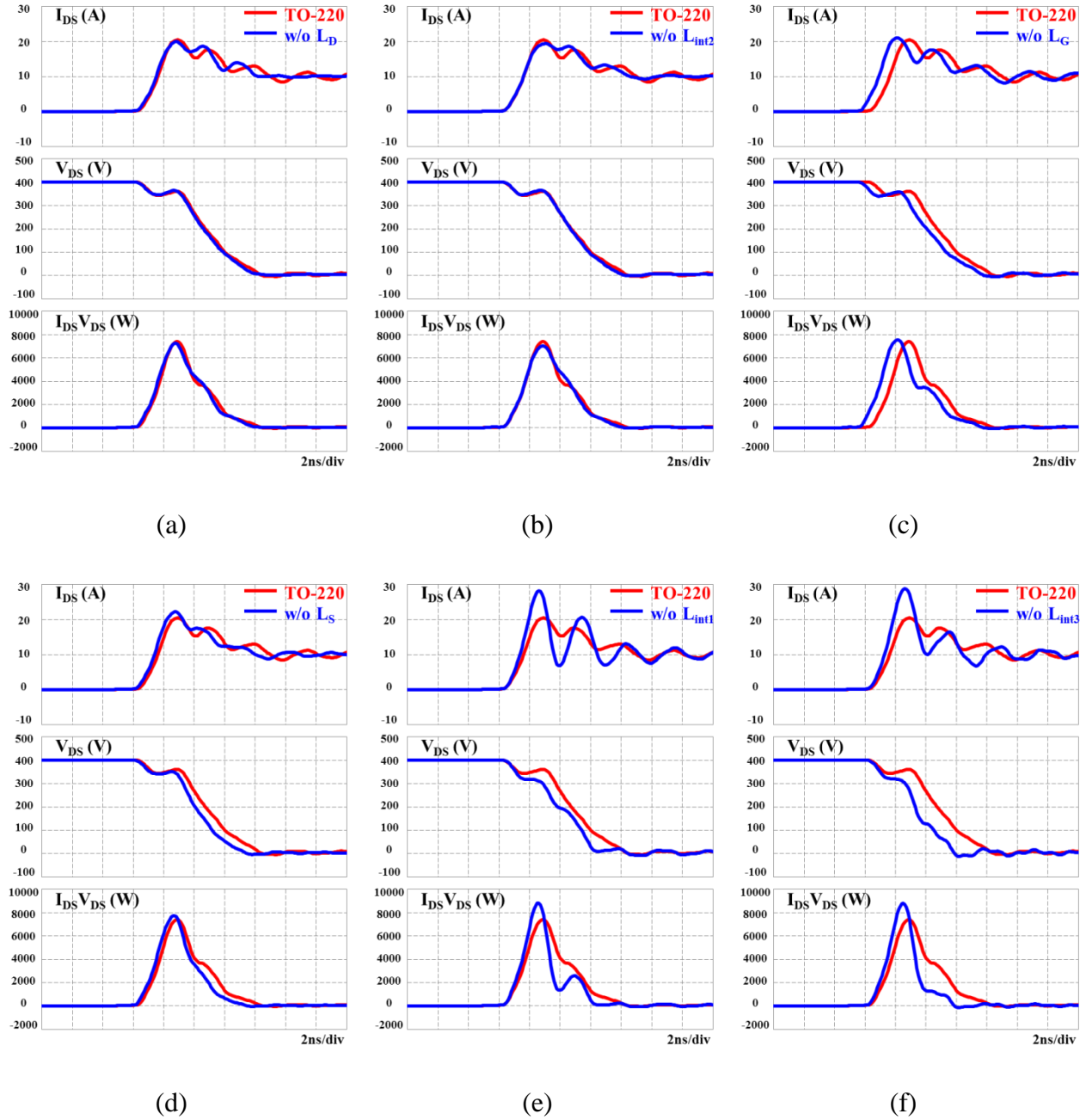


Figure 3.2 Top switch hard-switching turn-on waveforms comparison at 400V/10A

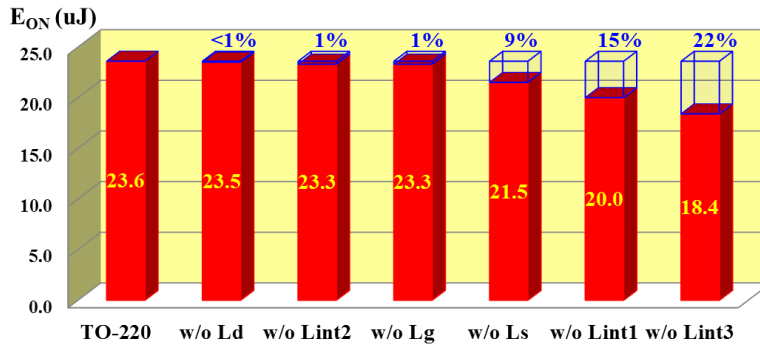


Figure 3.3 Device turn-on loss comparison at 400V/10A

In summary, the simulation results have quantitatively justified the predictions of the theoretical analysis, that the  $L_{int3}$ ,  $L_{int1}$  and  $L_S$  are identified to be the most critical package parasitic inductance. For future research regarding packaging improvement, these three inductances should be minimized in priority. Furthermore, it could be project that if an advanced package realized, which is able to eliminate all three critical parasitic inductances, the total device switching loss should have a significant reduction while better switching performance is expected.

### 3.2 Package Impact and Potential Failure Mode

As mentioned in Chapter 2, when the cascode GaN HEMT operates in CCM hard-switching buck converter, significantly high turn-on switching loss is observed. One of the major reason is the reverse recovery charge and junction capacitor charge of the bottom switch. The other major reason is the package parasitic inductance impact.

Figure 3.4 shows the equivalent circuit of a buck converter with all device package parasitic inductors highlighted. Typical turn-on switching waveforms under 400V/4.5A condition obtained from simulation are shown in Figure 3.5. In the switching waveforms, the black, green,

and purple curves are  $V_{GS}$ ,  $V_{DS}$ , and  $I_{DS}$  respectively, which are the external waveforms of the cascode structure. Furthermore, the red and blue curves are  $V_{SD\_Si}$  and  $V_{GS\_GaN}$  respectively, which are inside the cascode structure.

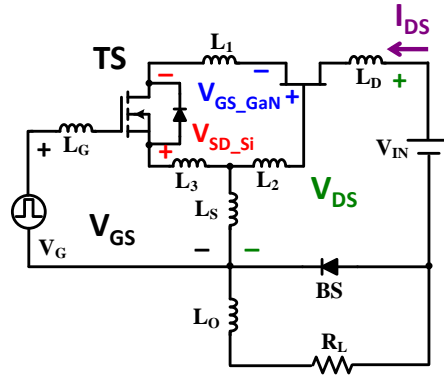


Figure 3.4 Equivalent circuit of a buck converter with the cascode GaN HEMT

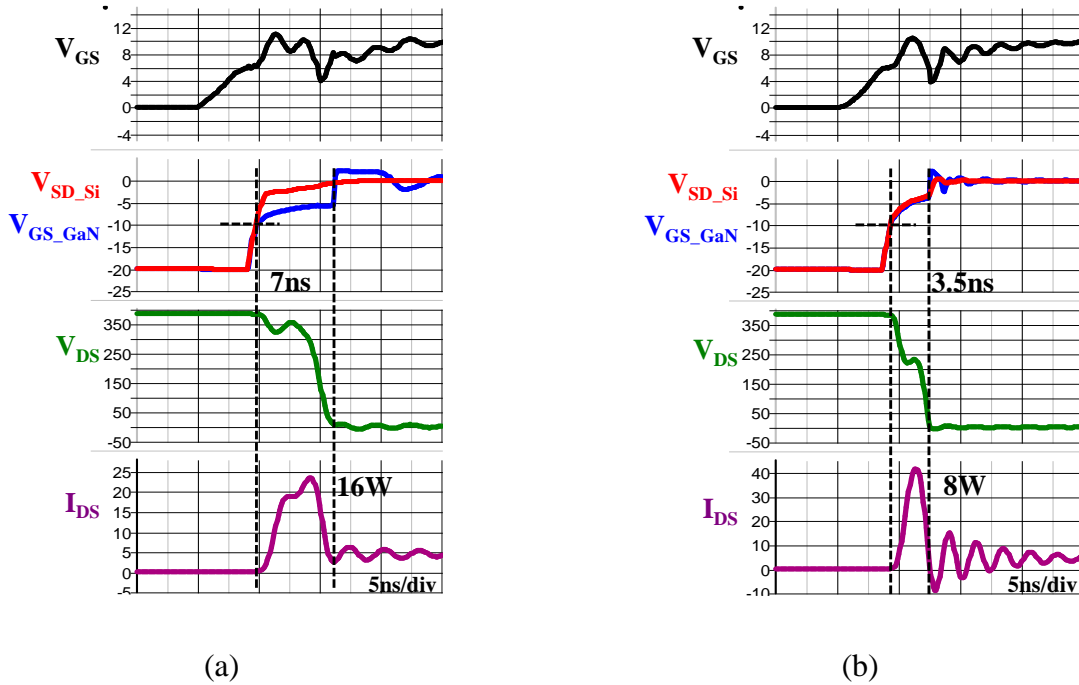


Figure 3.5 Turn-on waveform at 400V/4.5A (a) with package parasitic inductance, (b) without package parasitic inductance

As there is high  $di/dt$  existing in the high frequency commutation loop of the buck converter, during the turn-on transition time interval, significant voltage will be induced on  $L_{int1}$  and  $L_{int3}$ .

The essence of cascode structure is to control the GaN HEMT by controlling the Si MOSFET, or in other word, the blue curve should follow the change of the red curve. However, due to the induced voltage, the blue curve is not able to follow the red curve closely, and as a result, the GaN HEMT cannot turn on as fast as the turn-on of the Si MOSFET. Compared to the case without package parasitic inductance in Figure 3.5(b), the main transition time and turn-on loss are increased from 3.5ns to 7ns and from 8W to 16W respectively. So the package influence in hard-switching turn on is significant turn-on loss increase.

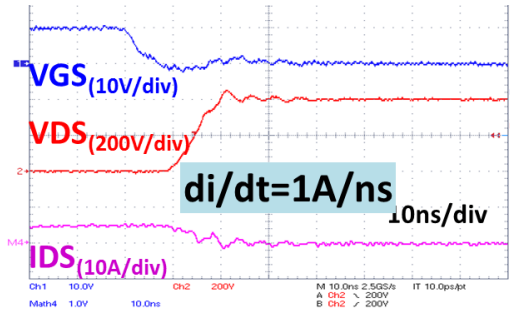
CRM soft switching can eliminates the high turn-on loss. However, even there is no issue from the point of loss, device failure is still observed at high current turn-off condition. Since  $di/dt$  increases with turn-off current quickly, the package effect will also be more significant.

Figure 3.6 shows  $di/dt$  at different turn-off current. It is clearly that the  $di/dt$  increases quickly when the turn-off current increasing. At 15A turn off condition, the  $di/dt$  achieves unprecedented 5A/ns. And around this condition, device failure might be observed.

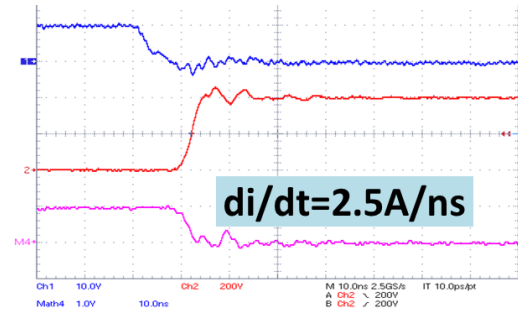
The reason for potential device failure is illustrated in Figure 3.7, in which the black and red curve are  $V_{SD\_Si}$  and  $V_{GS\_GaN}$  respectively; while the green, gray, and blue curves are voltage induced on internal parasitic inductors  $L_{int1}$ ,  $L_{int2}$ , and  $L_{int3}$  respectively.

$$V_{GS\_GaN} = V_{SD\_Si} + V_{Lint1} + V_{Lint2} + V_{Lint3} \quad (3.1)$$

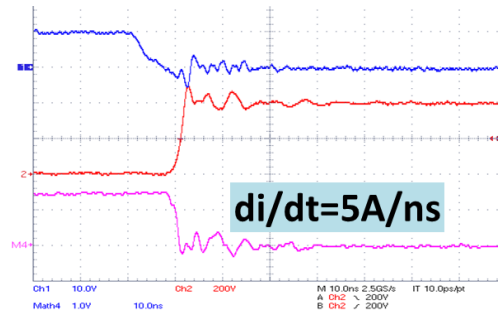
According to Kirchhoff voltage theory,  $V_{GS\_GaN}$  should be the superposition of  $V_{SD\_Si}$  with all voltage induced on the internal parasitic inductors as equation (3.1). So even  $V_{SD\_Si}$  is clamped at -30V due to the avalanche mechanism,  $V_{GS\_GaN}$  is still vulnerable to high voltage spike. As shown in Figure 3.7, the  $V_{GS\_GaN}$  reaches -35V.



(a)

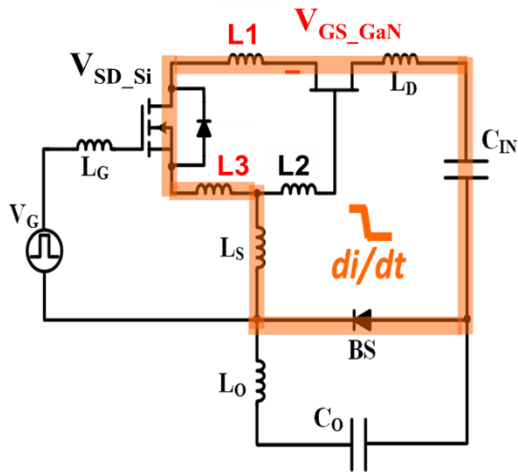


(b)

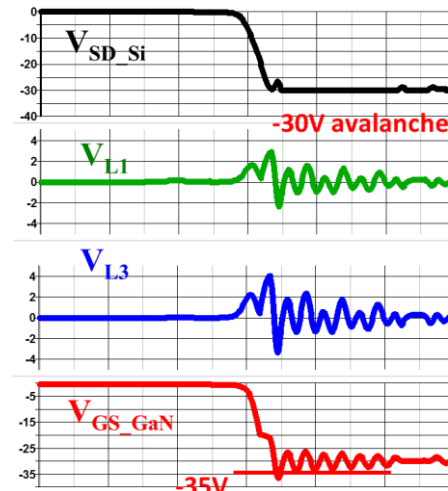


(c)

Figure 3.6  $di/dt$  at different turn-off current (a)  $I_{OFF}=5A$ , (b)  $I_{OFF}=10A$ , (c)  $I_{OFF}=15A$



(a)



(b)

Figure 3.7 Turn-off at 400V/12A (a) buck circuit schematic, (b) simulation waveform

So the package influence in hard-switching turn off is significant internal parasitic ringing which may cause device failure. For a robust design, the  $V_{GS\_GaN}$  of GaN device requires more margin.

### 3.3 Package Improvement Method

Based on the analysis in last section, it is clear that the traditional package has significant side effect on the device switching performance. Since the most critical parasitic inductors had already be identified, the following package improvement will focus on eliminating pre-defined common-source inductance.

Four different packages for high voltage cascode GaN HEMT are shown in Figure 3.8, in which the same GaN die and Si die are assumed. In Figure 3.8 (a) and (b), the TO-220 package and the PQFN package are industry common practice, while the PQFN plus package and the stack-die package are improved package based on previous analysis.

For the TO-220 package, as analyzed before, there are three common-source inductors existing, which are  $L_{int1}$ ,  $L_{int3}$ , and  $L_S$ .

For the PQFN package, three leads are eliminated so that  $L_S$  is no longer existing. In addition, Kelvin connection is applied to provide a separate gate drive return loop. So for Si MOSFET, it's power loop and driving loop are decoupled and no common-source inductance existing. However, the Kelvin connection can only affect Si MOSFET but have limited effect on GaN HEMT. From the prospective of GaN HEMT,  $L_{int1}$  and  $L_{int3}$  are shared by it's power loop and driving loop. So they are still the common-source inductance for GaN HEMT.



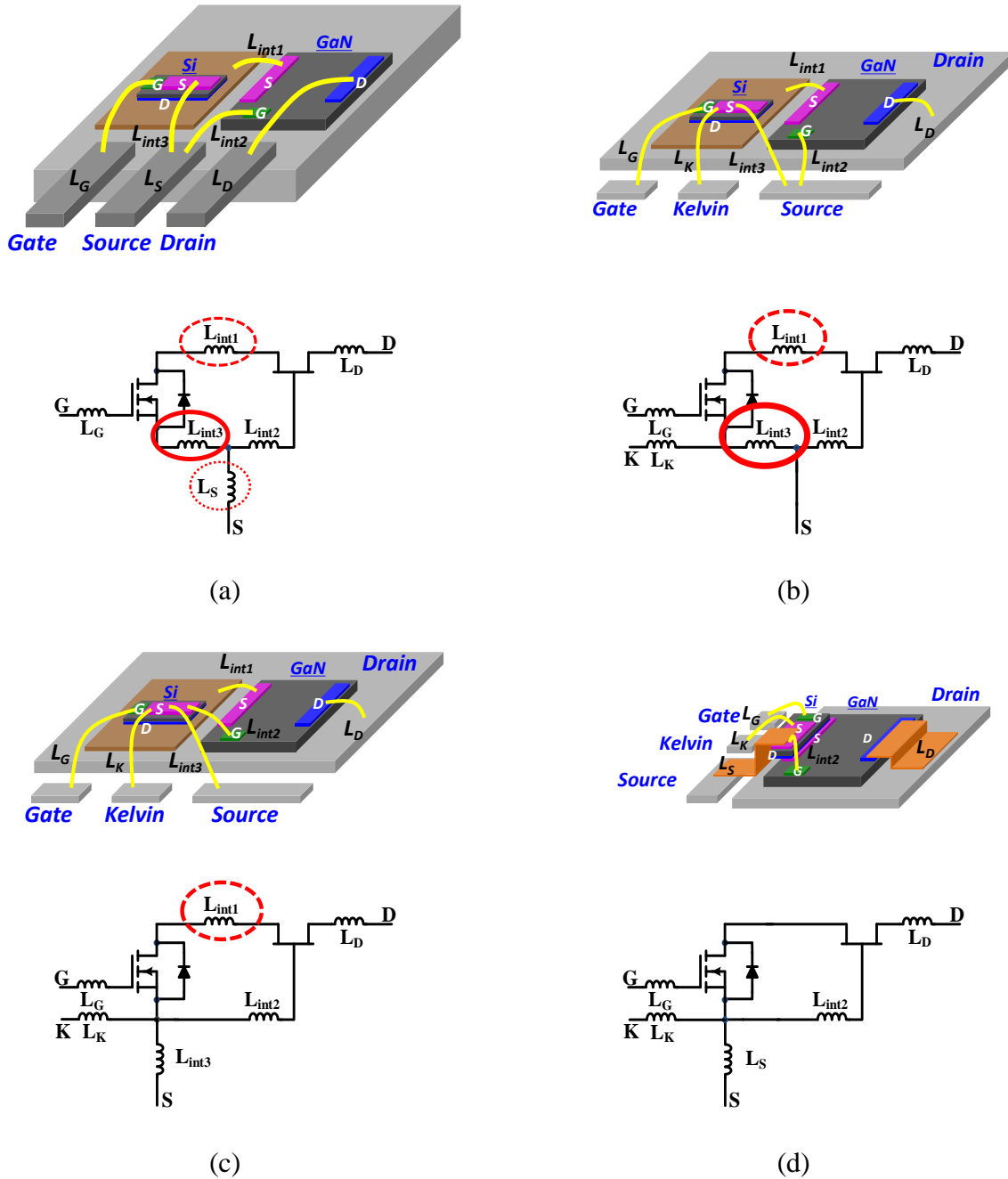


Figure 3.8 Package bonding diagram and schematic for cascode GaN HEMT in different packages. (a) TO-220, (b) PQFN, (c) PQFN plus, (d) Stack-die

A simple but effective way to improve the cascode package is the PQFN plus package shown in Figure 3.8 (c). Comparing to traditional PQFN package, the major difference is redirecting bonding wire  $L_{int2}$ . The purpose of  $L_{int2}$  is to realize the connection between the gate

pad of GaN HEMT and the source pad of Si MOSFET. In PQFN package, one terminal of  $L_{int2}$  is on the gate pad of GaN HEMT while the other terminal is on the source pad of cascode device. With this arrangement,  $L_{int3}$  is included in the driving loop of GaN HEMT so that it becomes the common-source inductance of GaN HEMT. On the contrary, in PQFN plus package, one terminal of  $L_{int2}$  is still on the gate pad of GaN HEMT, while the other terminal is redirected to the source pad of Si MOSFET. In this way, the  $L_{int3}$  is excluded from the driving loop of GaN HEMT. Meanwhile, with Kelvin connection, it is also excluded from the driving loop of Si MOSFET. Finally,  $L_{int3}$  is no longer common-source inductance of this cascode device.

If maintaining Si MOSFET and GaN HEMT side-by-side configuration, further improvement beyond the PQFN plus package seems can hardly be achieved. In order to eliminate the last common-source inductance  $L_{int1}$ , the concept of stack-die configuration, which previously is used in the cascode package of SiC JFET and Si MOSFET [17], is a good candidate. As shown in Figure 3.8(d), in the stack-die package of cascode GaN device, the Si MOSFET (drain pad) is mounted on top of the GaN HEMT (source pad) directly. With this stack-die package, there is no parasitic inductor shared by more than one loop, so all common-source inductances are eliminated. Thus the stack-die package is considered as the optimized package for cascode GaN device.

Among commercial GaN devices, there is a kind of advanced package introduced in [18] which makes the proprietary vertical structure GaN die embedded into a CMOS substrate, in which low voltage Si MOSFET and gate driver are all integrated. In this method, both external and internal parasitic inductance are minimized, and a fully integrated high-voltage cascode GaN HEMT with specifically designed gate driver is realized. However there are still at least two limitations to extend this method to other cases. First, the high voltage GaN HEMT is in

proprietary vertical structure, while most popular high voltage GaN HEMT are usually in lateral structure. Second, the low voltage Si MOSFET is based on many signal level MOSFETs in parallel not standard power MOSFET. As a comparison, the stack-die package proposed in this thesis is based on most common high voltage lateral GaN HEMT and low voltage vertical Si power MOSFET. So this method can solve the package related issue in general and be easily extended to other cascode GaN devices.

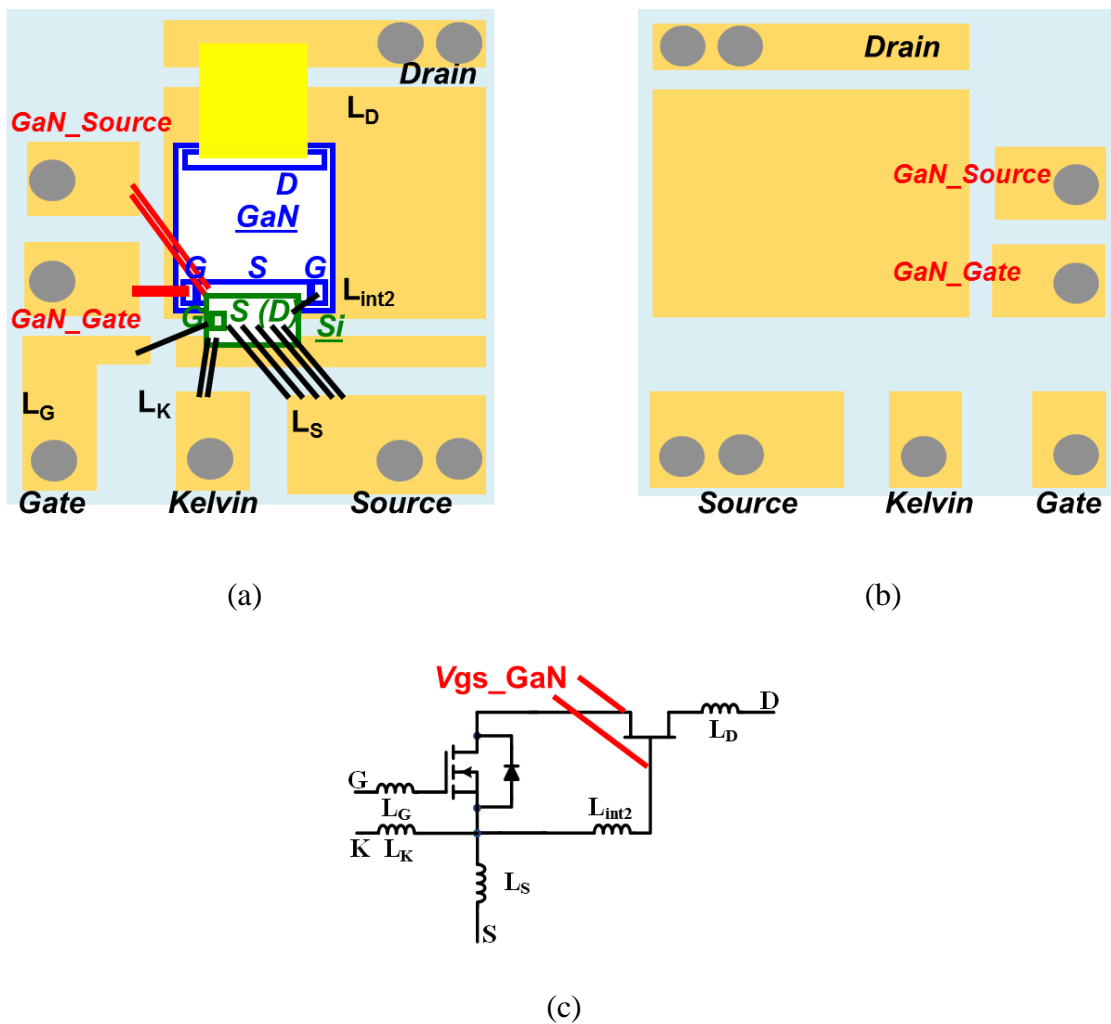


Figure 3.9 Design of stack-die package for cascode GaN HEMT (a) top view, (b) bottom view, and (c) schematic

Figure 3.9 is the design for stack-die package prototype. The top view shows that the Si die is attached on the source pad of the GaN die directly. Then copper foil and bonding wires are both used to achieve necessary electrical connection. All external electrical terminals are clearly marked in which two pads for the gate terminal and the source terminal of the GaN die are purposely introduced so that the internal waveforms  $V_{gs}$  of the GaN HEMT can be measured through this package.

### **3.4 Stack-die Package Fabrication**

The designed stack-die structure has been packaged in a low profile format similar to the conventional PQFN package. As presented in Figure 3.10, the packaged stack-die device can be easily surface-mounted on the testing board using solder reflow technique. The fabrication process includes two major steps: substrate preparation and device assembly.

Alumina direct bonded copper substrate ( $Al_2O_3$  – DBC;  $Al_2O_3$  15 mil, Cu 5mil) of high strength and good thermal conductivity was selected as the chip carrier for this power semiconductor assembly. Firstly, 1-mil thick adhesive Kapton® tape used as etching mask was covered the whole area on both top and bottom Cu surfaces of the DBC substrate. After laser patterning, the attached tapes were selectively removed according to the substrate layout. The exposed Cu areas have been then etched off by ferric chloride solution to form the circuitry. Multiple through holes were drilled on the developed Cu pads using the same CO2 laser machine. A picture of the substrate after laser drilling process is illustrated in Figure 3.11 (a). Next, the plasma-cleaned top Cu pads have been electro-plated by nickel (Ni) and gold (Au) successively, which helps to avoid the surface oxidation and facilitates further die-attachment and wire-bonding. The thickness of the Au finish surface is in the range of 20 to 30  $\mu m$ . Subsequently,

mounting pins with 0.5 mm diameter (head diameter of 1 mm) were inserted to the drilled through holes and firmly connected to both Au plated Cu surface pads by a solder reflow process using a lead-free solder paste (Sn89Sb10.5Cu0.5, solidus temperature of 242°C). The extra parts of soldered pins were truncated and ground to be flush with the bottom surface of the substrate, as shown in Figure 3.11 (b). The prepared DBC substrate has been cleaned once again for the following device assembly step.

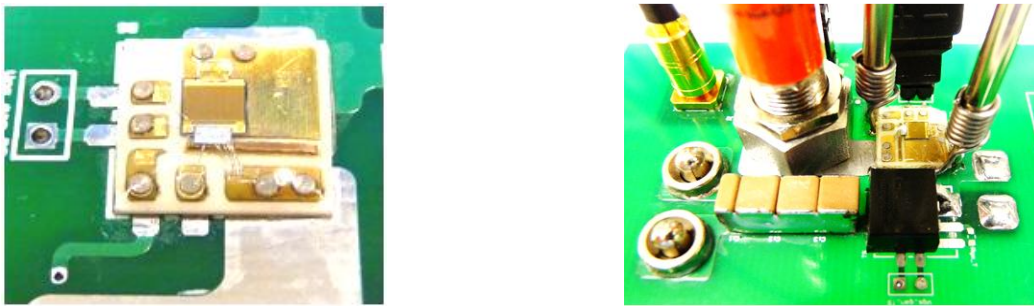
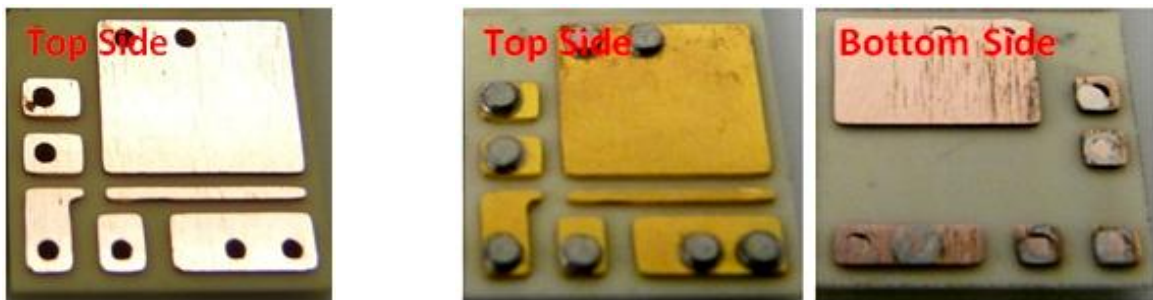


Figure 3.10 Packaged stack-die device mounted on the double-pulse tester board with transparent silicone elastomer glob-top encapsulation



(a)

(b)

Figure 3.11 Patterned  $\text{Al}_2\text{O}_3$  – DBC substrate: (a) top surface pads after etching and laser drilling, (b) electro-plated Au top surface with soldered pins and ground bottom surface

A 600V GaN HEMT and a 30V Si MOSFET bare dies were selected for the stack-die device assembly. The GaN die and a Cu spacer of the same thickness as GaN were first soldered on the substrate. The Cu spacer has been used in order to level the position of Si device mounted directly on GaN device. A solder mask protecting the channel area was applied on the top

surface of GaN die with only source and drain pads uncovered. Then, the Si die was soldered on top of the GaN die. The solder joint links the drain terminal of Si MOSFET to the source terminal of GaN HEMT without wire-bonding. A cut Cu foil (0.2 mm) with Au plating was also soldered simultaneously to make an electrical connection between GaN's drain terminal and the corresponding area on the DBC substrate. The solder paste used in this process is in lead-tin (Pb-Sn) eutectic composition which has a lower melting point of 183°C compared to the one used for the connection pin soldering. After device soldering, 2-mil aluminum (Al) wires were bonded between semiconductors and the electrical pads on the DBC substrate. The gate, Kelvin, and source electrodes on the substrate were wire bonded to the Si MOSFET and additional Al wires for GaN signal sensing were also bonded on the GaN device. Epoxy molding compound or silicone elastomer (as glob-top) was finally applied to encapsulate the packaged stack-die device for electrical/chemical protection and easy handling.

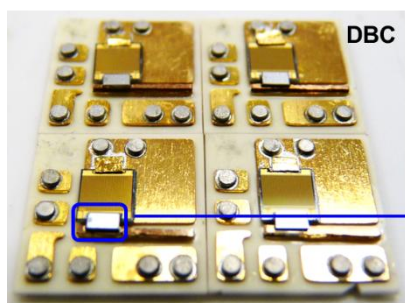


Figure 3.12 Die attachment

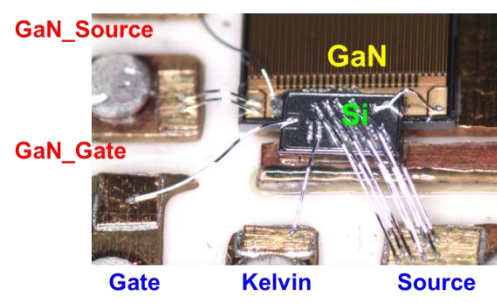
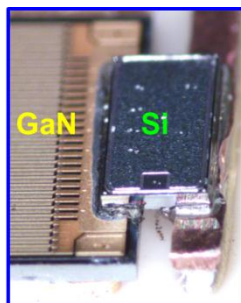


Figure 3.13 Wire bonding process

### 3.5 Evaluation of GaN HEMT in Stack-die Package

The performance of high-voltage cascode GaN HEMT in stack-die package is evaluated by comparing with a commercial product in TO-220 package. Both of them include the same GaN

die and Si die, while the difference is method of packaging. Experimental result shows that the stack-die package has improvement in both hard-switching turn on and turn off.

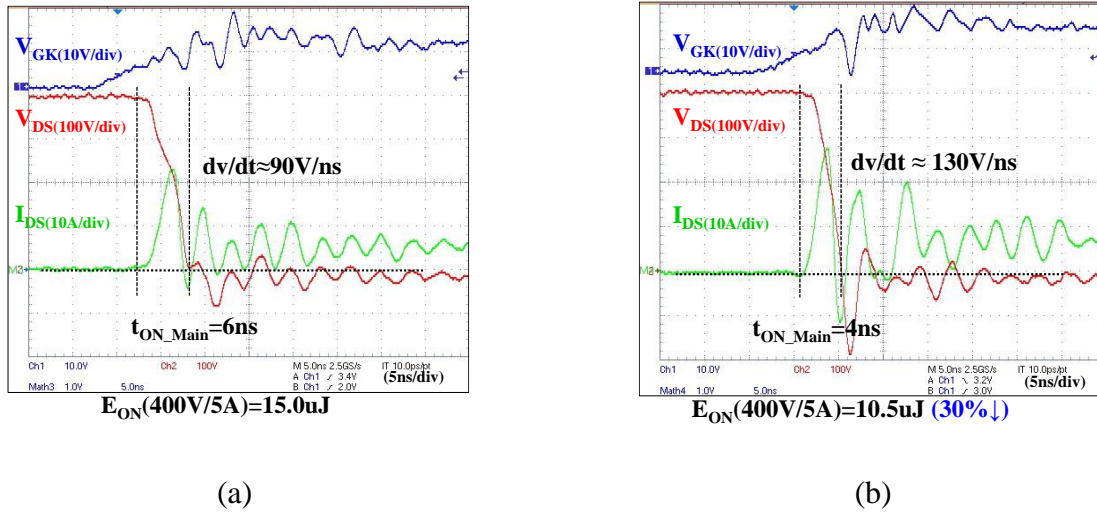


Figure 3.14 Turn-on waveform comparison (a) TO-220 package, (b) stack-die package

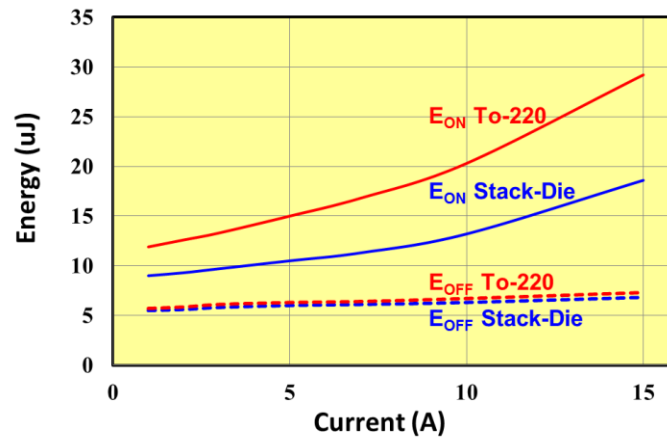


Figure 3.15 Switching energy comparison for different packages

The two devices are tested under the same double-pulse tester setup in Chapter 2. Figure 3.14 shows the turn-on waveforms at 400V/5A condition. In accordance with previous analysis, the stack-die package has faster switching transition speed compared to the TO-220 package. The  $dv/dt$  is increased from 90V/ns to 130V/ns, while the main transition time and turn-on

switching energy is reduced from 6ns and 15.0uJ to 4ns and 10.5uJ respectively. 30% turn-on energy is saved at this condition.

Figure 3.15 is the measured switching energy at different load current conditions. In all load range, the turn-on energy of the stack-die package is reduced significantly.

For the test under high current hard-switching turn off condition, the internal waveform  $V_{GS\_GaN}$  in traditional package cannot be measured. So simulation model is used again in there to predict the internal waveform. Figure 3.16 shows the simulated  $V_{GS\_GaN}$  for different packages.

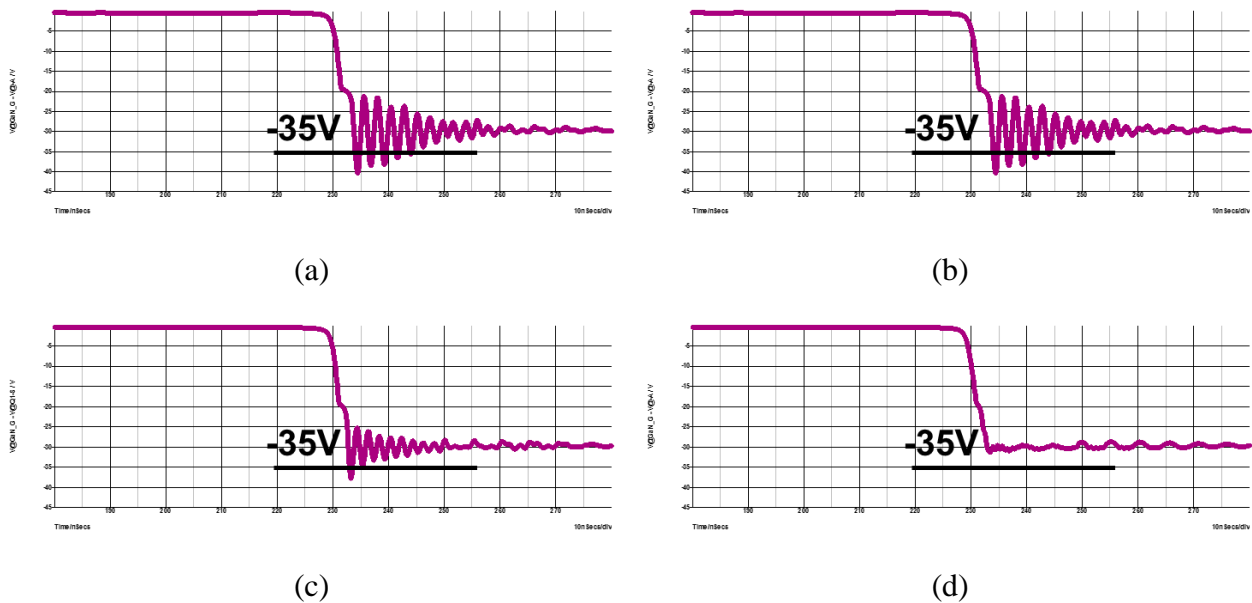


Figure 3.16 Simulated  $V_{GS\_GaN}$  for (a) TO-220, (b) PQFN, (c) PQFN plus, (d) stack-die

The simulated turn-off waveforms are under 400V/15A turn-off condition. It is clear that for TO-220 and PQFN, the parasitic ringing is likely to hit -40V, which is far below -35V. Between TO-220 and PQFN, there is no much difference because their internal bonding wire structure are very similar. So simply eliminating external through leads doesn't affect internal parasitic ringing.



For proposed PQFN plus package, since  $L_{int3}$  is no longer common source inductance and has no effect on the internal GaN driving loop, the parasitic ringing is reduced. However, for all these three cases,  $V_{GS\_GaN}$  over  $-35V$  is observed and if there is enough energy applied on the gate terminal of the GaN die, the parasitic ringing possibly cause device failure.

According simulation, the proposed stack-die package is able to solve the parasitic ringing effectively as shown in Figure 3.16 (d). The  $V_{GS\_GaN}$  is well clamped at  $-30V$  through Si avalanche breakdown mechanism protection.

With proposed stack-die package, the internal waveform is able to be measured. Figure 3.17 is the measured turn-off waveforms of stack-die package under  $400V/15A$  condition. The purple curve shows that  $V_{GS\_GaN}$  is clamped at  $-30V$ , while no voltage overshoot occurs. This is helpful to improve the stability of the cascode GaN HEMT.

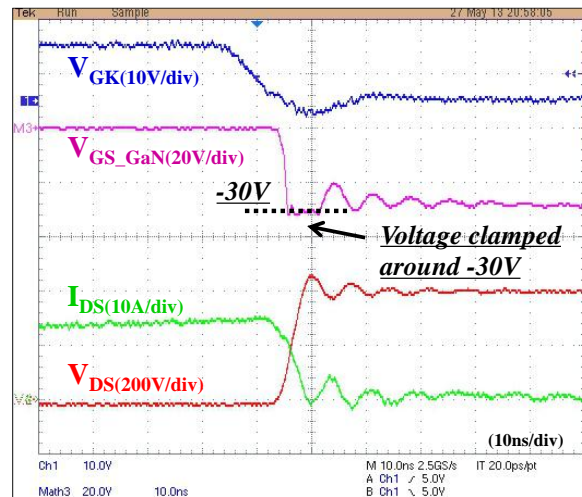


Figure 3.17 Turn-off waveform of stack-die package

To summarize this chapter, the high-voltage cascode GaN HEMT enables higher switching transition speed compared to traditional Si MOSFET and leads to great challenge for device package design. Traditional package is already a limitation to realize the promising performance

of the GaN HEMT. To solve this issue, a stack-die package for the cascode GaN HEMT is introduced which eliminates all package related common-source inductances, and thus, improves the device switching performance and stability significantly and makes the device more suitable for MHz high frequency operation.

## Chapter 4. Summary and Future Work

In this thesis, an evaluation of the 600V cascode GaN HEMT is conducted. The cascode GaN HEMT shows great potential for high frequency power conversion. However, when applying it into a hard switching converter, there is still large switching loss and parasitic ringing, and it is hard to further push the switching frequency to multi-MHz.

In order to analyze the loss mechanism and the switching performance in detail, a simulation model is developed based on a manufacturer provided model. Among different modifications, the most important one is accurate package parasitic inductance extraction, considering both self-inductance and mutual-inductance and differentiating the inductance for turn-on and turn-off transition. The accuracy of the developed simulation model is verified by a double pulse tester. The simulation matches the experiment in both switching waveform and switching energy.

A buck converter loss breakdown is made based on the simulation model, which indicates the turn-on loss is dominant in hard switching condition. While the turn-off loss is extremely small. The reason of the high turn-on loss is discovered as the Si MOSFET body diode reverse recovery and cascode package parasitic inductance. The reason of the small turn-off loss is the current source turn-off mechanism existing in the cascode structure.

To improve the efficiency of the buck converter and further push frequency, critical conduction mode is proposed as a good candidate. It eliminates the dominant turn-on loss while utilizes the small turn-off loss. So the efficiency is increased significantly.

With CRM operation, the frequency is successfully pushed to multi-MHz maintaining high efficiency, however device failure is observed with clean waveform and low loss. After study the impacts of the cascode package, two major issues, extra turn-on loss and significant internal

parasitic ringing, are also discovered. Finally, the stack-die package is proposed to reduce turn-on loss and to reduce parasitic ringing so that potential failure mode is avoided.

Future work will focus on high frequency application of the cascode GaN HEMT. By utilizing soft switching techniques and advanced cascode package, the GaN device offers the opportunity to design a power converter operating at multi-MHz, which is more than 10 times higher than traditional design with Si MOSFET. Dramatically increased frequency will benefit passive components design significantly. Because the size and volume of the total power supply system is expected to shrink a lot. Eventually it is possible and very attractive to achieve high frequency, high efficiency, and high density power conversion at the same time with GaN.

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