A High-Efficiency Hybrid Resonant Microconverter for Photovoltaic Generation Systems

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Dissertation submitted to the faculty of the
Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

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August 28, 2014
Blacksburg, VA

Keywords: High efficiency, photovoltaic, modular power conditioning system, isolated dc-dc converter, resonant power conversion, high-frequency ac switch

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ABSTRACT

The demand for increased renewable energy production has led to increased photovoltaic (PV) installations worldwide. As this demand continues to grow, it is important that the costs of PV installations decrease while the power output capability increases. One of the components in PV installations that has lots of room for improvement is the power conditioning system. The power conditioning system is responsible for converting the power output of PV modules into power useable by the utility grid while insuring the PV array is outputting the maximum available power. Modular power conditioning systems, where each PV module has its own power converter, have been proven to yield higher output power due to their superior maximum power point tracking capabilities. However, this comes with the disadvantages of higher costs and lower power conversion efficiencies due to the increased number of power electronics converters. The primary objective of this dissertation is to develop a high-efficiency, low cost microconverter in an effort to increase the output power capability and decrease the cost of modular power conditioning systems.

First, existing isolated dc-dc converter topologies are explored and a new topology is proposed based on the highly-efficient series resonant converter operating near the series resonant frequency. Two different hybrid modes of operation are introduced in order to add wide input-voltage regulation capability to the series resonant converter while

achieving high efficiency through low circulating currents, zero-current switching (ZCS) of the output diodes, zero-voltage switching (ZVS) and/or ZCS of the primary side active switches, and direct power transfer from the source to the load for the majority of the switching cycle. Each operating mode is analyzed in detail using state-plane trajectory plots. A systematic design approach that is unique to the newly proposed converter is presented along with a detailed loss analysis and loss model. A 300-W microconverter prototype is designed to experimentally validate the analysis and loss model. The converter featured a 97.7% weighted California Energy Commission (CEC) efficiency with a nominal input voltage of 30 V. This is higher than any other reported CEC efficiency for PV microconverters in literature to date.

Each operating mode of the proposed converter can be controlled using simple fixed-frequency pulse-width modulation (PWM) based techniques, which makes implementation of control straightforward. Simplified models of each operating mode are derived as well as control-to-input voltage transfer functions. A smooth transition method is then introduced using a two-carrier PWM modulator, which allows the converter to transition between operating modes quickly and smoothly. The performance of the voltage controllers and transition method were verified experimentally.

To ensure the proposed converter is compatible with different types of modular power conditioning system architectures, system-level interaction issues associated with different modular applications are explored. The first issue is soft start, which is necessary when the converter is beginning operation with a large capacitive load. A novel soft start method is introduced that allows the converter to start up safely and quickly, even with a short-circuited output. Maximum power point tracking and double line frequency ripple

rejection are also explored, both of which are very important to ensuring the PV module is outputting the maximum amount of available power.

Lastly, this work deals with efficiency optimization of the proposed converter. It is possible to use magnetic integration so that the resonant inductor can be incorporated into the isolation transformer by way of the transformer leakage inductance in order to reduce parts count and associated costs. This chapter, however, analyzes the disadvantages to this technique, which are increased proximity effect losses resulting in higher conduction losses. A new prototype is designed and tested that utilizes an external resonant inductor and the CEC efficiency was increased from 97.7% to 98.0% with a marginal 1.8% total cost increase. Additionally, a variable frequency efficiency optimization algorithm is proposed which increases the system efficiency under the high-line and low-line input voltage conditions. This algorithm is used for efficiency optimization only and not control, so the previously presented simple fixed-frequency modeling and control techniques can still be utilized.

To my wife:
Kristin LaBella

To my parents:
Carl LaBella
Cindy Rodrigues

Acknowledgements

First, I would like to express my sincere gratitude to my academic and career advisor, Dr. Jih-Sheng Lai, for affording me the opportunity to work under him in the Future Energy Electronics Center (FEEC). Without his faith in my abilities and his many years of continuous financial support and academic guidance, this degree would not be possible. I would also like to thank my advisory committee members Dr. William Baumann, Dr. Virgilio Centeno, Dr. Kathleen Meehan, and Dr. Douglas Nelson for their suggestions and comments throughout my pursuit of this degree.

I am very grateful to all of my colleagues and friends that I have had the opportunity to interact with on a daily basis in the FEEC. The insight and knowledge I have gained from discussions with all of you have been absolutely invaluable. I want to give a special thanks to Dr. Wensong Yu and Dr. Younghoon Cho for their superb guidance and the motivation they have provided me. In addition to the people I have worked with in the FEEC, I would like to thank Dr. Matthew Senesky for being an incredible mentor to me during my internship at National Semiconductor as well as the three proceeding years guiding me on the projects I've worked on in the FEEC. I would also like to thank Dave Anderson, Dr. Michael Seeman, and Dr. Gianpaolo Lisi with Texas Instruments for providing support, guidance, and funding for the work in this dissertation. Last, but certainly not least, I would like to thank Dr. Richard Hoagland with Digital Receiver Technology for taking me on as an intern and introducing me to the world of power electronics before I ever took my first power electronics course at Virginia Tech. Before my internship there, I had no idea even what a buck converter was.

I would like to thank my parents for their continuous love, support, and encouragement with every venture that I undertake life. Finally, I'd like to give a very special thanks to my wife of 3 years, Kristin, who has been extraordinarily patient and supportive throughout this long journey. The motivation and inspiration she has afforded me has kept me focused and helped me realize not only my academic goals, but also my goals in all aspects of life.

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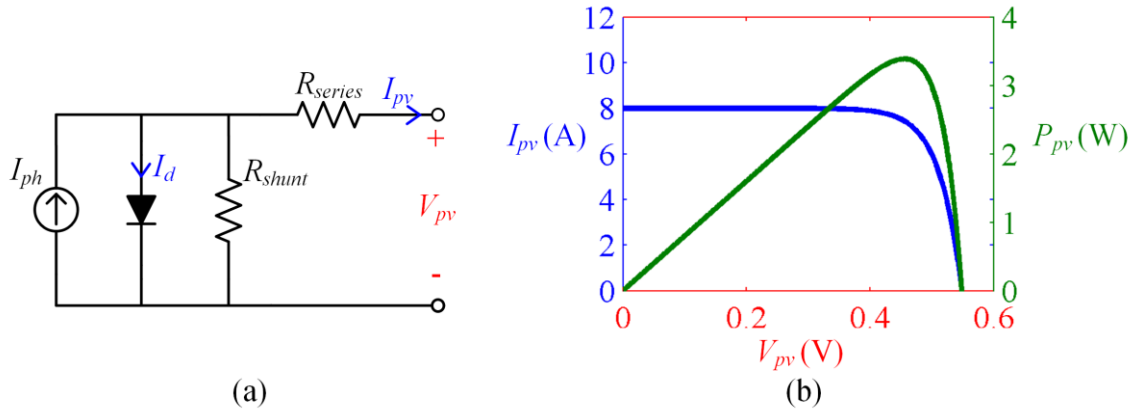
Chapter 1

Introduction

1.1 Background of Photovoltaic Generation Systems

The number of renewable energy installations in the world is steadily increasing each year due to the limited availability of fossil fuels and the negative impact on the environment associated with burning fossil fuels [1]. Among the different types of renewable energy sources, solar, or photovoltaic (PV), power has been one of the fastest growing, shows some of the greatest potential for future installations, and is steadily decreasing in price. The number of solar installations in the world is projected to more than double by the year 2040 [2], and, in the past 3 years alone, the average cost of installing utility-scale solar in the United States (US) has come down from approximately $3.24 per watt to $1.55 per watt and residential has fallen from $4.64 to $2.75 per watt [3].

An integral part to a photovoltaic generation system is the power conditioning system (PCS). The PCS consists of power electronic converters that make the energy output of PV modules usable by the utility grid [4, 5]. It accounts for a large portion of the cost of a PV installation so a significant amount of research, including the work in this dissertation, is focused on increasing the performance while decreasing the costs of these electronics. PV power conditioning systems have three major duties: (i) track the maximum power point (MPP) of the PV modules, (ii) convert the output power of the PV modules to power that is usable by the utility grid, and (iii) provide galvanic isolation between the modules and the grid.



(a) (b)

Figure 1.1. (a) Single-diode model [8] and (b) the I-V and P-V curves of a PV cell.

Maximum power point tracking (MPPT) is necessary for PV modules because of their non-linear output characteristics. A single PV module is made up of several individual PV cells: usually either 60 or 72 connected in series [6, 7]. Figure 1.1 (a) shows the single-diode model of a PV cell [8] and (b) shows the resulting output current versus output voltage and output power versus output voltage curves for a given operating condition. These curves are also known as I-V and P-V curves, respectively. These nonlinear I-V characteristics can vary drastically depending on the PV cell material, solar irradiance, temperature, module shading, etc. [9]. Figure 1.2 shows the I-V characteristics for the commercially available Canadian Solar CS6P-255P 255-W PV module under (a) different solar irradiance levels and (b) different temperatures [6]. As environmental conditions change, it is important that the power conditioning system be able to track the MPP to ensure the module is outputting the maximum available power.

The second major task of the PCS is to convert the dc output of the PV module to either a higher voltage dc bus or ac bus, depending on which type of grid the installation is feeding. The dc output voltage of the PV module (or array of modules) will vary as environmental conditions change, so the PCS needs to be able to handle the voltage

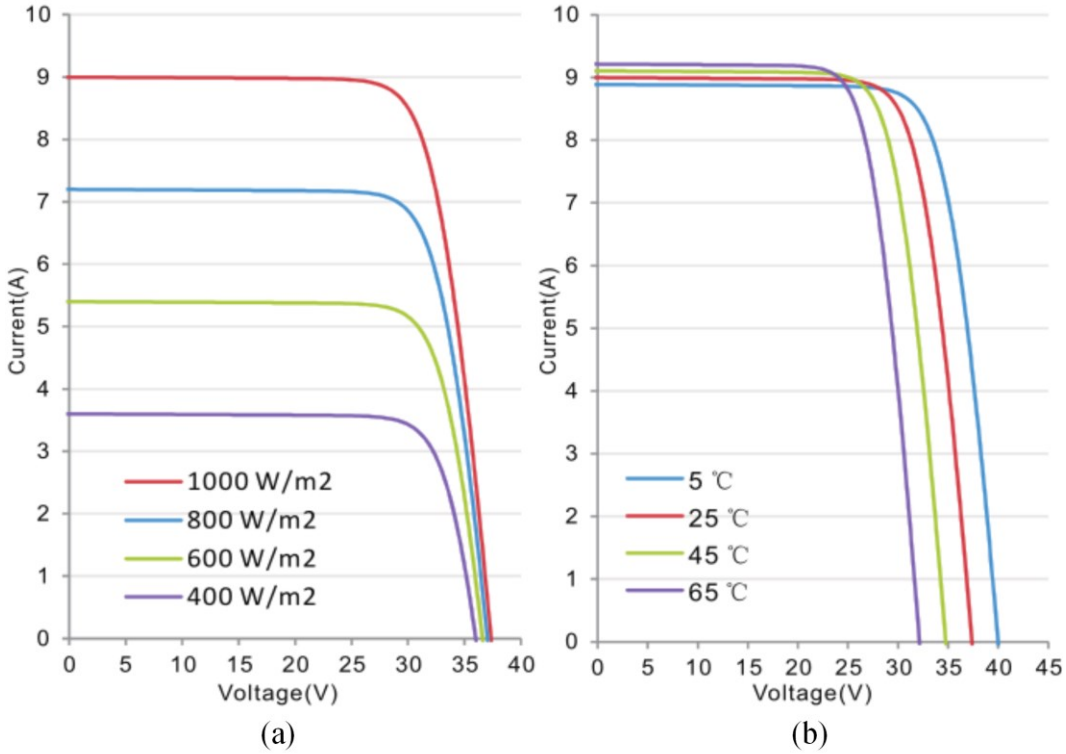


Figure 1.2. I-V curves of the CS6P-255P PV module operating under different (a) solar irradiance and (b) temperature [6].

fluctuations of the modules while providing either a fixed-voltage dc bus output in the case of a dc microgrid or a fixed-magnitude ac bus in the case of a conventional ac utility grid.

The third task of the PCS is to provide galvanic isolation between the PV modules and the utility grid. While there are no standards to date in the US that require galvanic isolation [10], there are several advantages to having it. In the US, the National Electric Code (NEC) requires that the metal frames of the PV modules be grounded to the utility earth ground in order to protect against lightning strikes and for the safety of personnel who install and maintain the modules [11]. There are parasitic capacitances that exist between the PV cells and the metal frame of the module, so without galvanic isolation in the PCS, there is the potential for a ground loop causing large ground leakage currents. This is demonstrated in Figure 1.3. These leakage currents can cause grid power quality

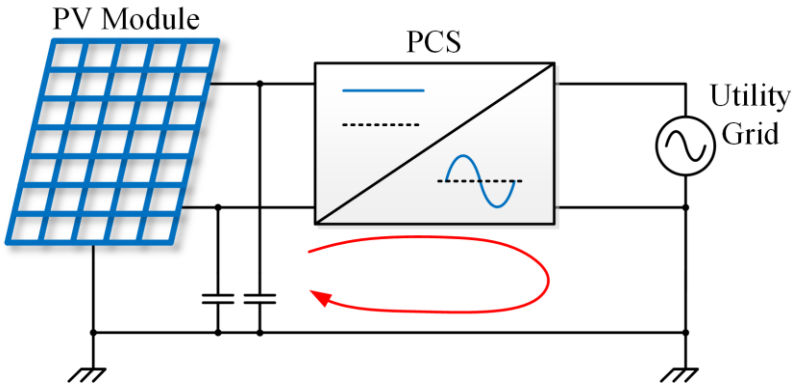


Figure 1.3. Ground loop in a non-isolated PV PCS.

issues such as electromagnetic interference (EMI) and increase grid current total harmonic distortion (THD) [12, 13]. Having isolation in the PCS can help mitigate these problems.

1.2 PV Power Conditioning Systems Architectures

There are three main categories of PV power conditioning system architectures: (i) centralized, (ii) string, and (iii) modular [13-15]. The first two are used with the conventional ac utility grid, and the third can either be used with an ac grid or dc microgrid. With a centralized PCS, several PV modules are connected in series to form strings, and then several strings are connected in parallel. The parallel strings are all connected to one high-power centralized inverter. This inverter tracks the maximum power point of the entire array of modules and sends the power to the ac utility grid, as shown in Figure 1.4 (a). Because there is only one power electronics converter, this type of PCS is the least expensive and easiest to maintain. As a result, this is the most commonly found PCS architecture in PV installations today. A major disadvantage of this architecture, however, is it suffers from low MPPT efficiency. Since there is only one power electronics converter tracking the MPP of the entire array of modules, the overall power output of the array can

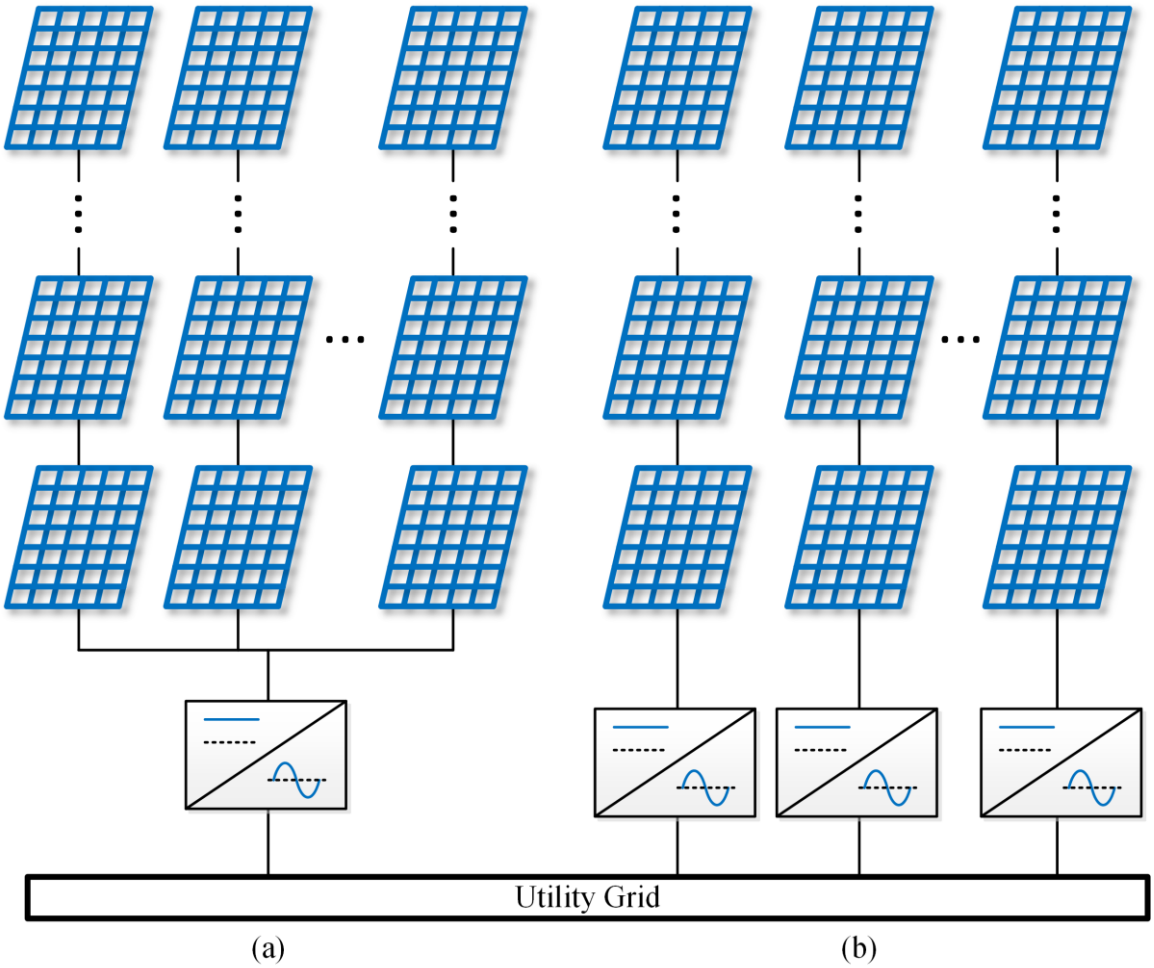


Figure 1.4. Types of conventional PV PCS; (a) centralized inverters and (b) multiple string inverters.

be significantly lower than if each individual module were to have its own MPPT. If one module in the array is outputting less power than the others because of shading or degradation caused by age, the output power of the entire array will suffer. Another disadvantage is poor scalability. Since there is just one inverter for an entire array of modules, different sized applications will require different sized inverters and it is not easy to expand upon a current installation after it is installed.

The second type of PCS architecture is the string inverter system. This type of PCS consists of several modules connected in series to from a string, and then each string has

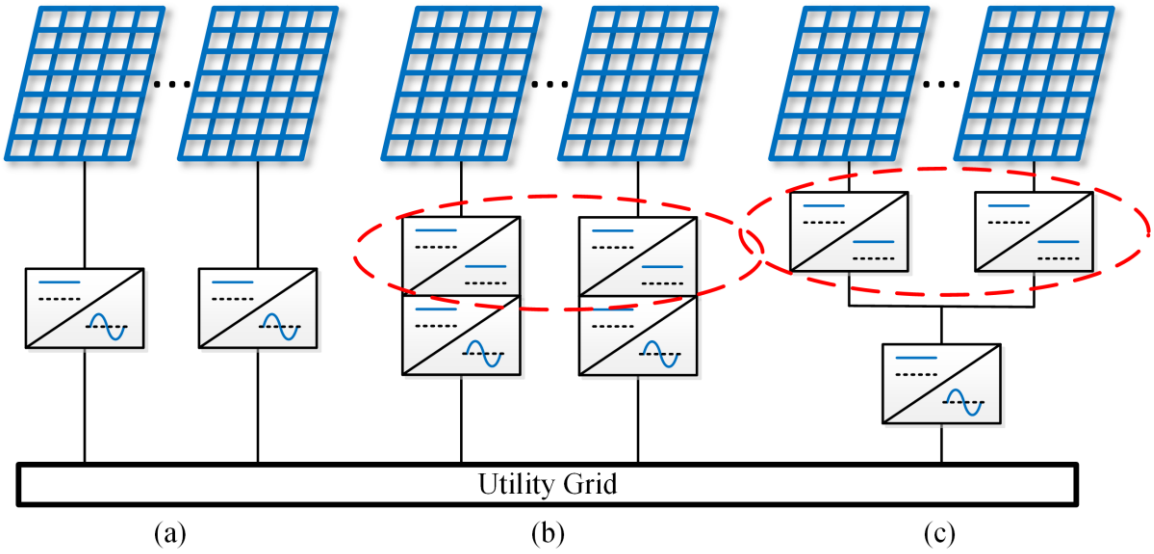


Figure 1.5. Types of modular PV PCS; (a) single-stage microinverter, (b) two-stage microinverter, and (c) distributed microconverter with centralize inverter.

its own medium-power inverter and is pictured in Figure 1.4 (b). This type of configuration has more converters and is therefore more expensive than the centralized system, however both the MPPT efficiency and scalability are improved. Here, each string of modules has its own converter performing MPPT so power mismatch between modules in a string will lower the effective output of that particular string, but it won't affect the entire array as is the case of the centralized system. This type of installation is easier to scale because one inverter and string of modules can be added at a time to scale the system for different applications.

The third type of PCS architecture is the modular system. With modular power conditioning systems, each PV module has its own power converter, or module integrated converter (MIC), which tracks the MPP of each individual module. MICs can either output ac directly to the utility grid (microinverter) or can output dc (microconverter). Microinverters can either be implemented as a single stage where they convert the PV module voltage directly to ac, or two stage where there is an intermediate dc-dc converter

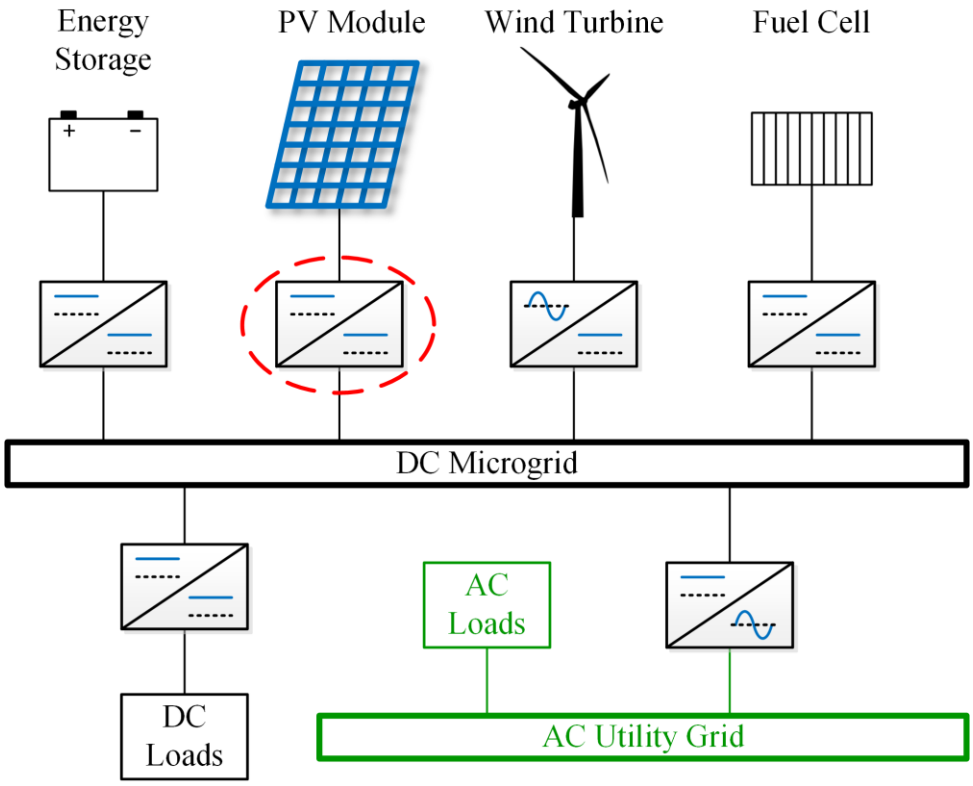


Figure 1.6. Example dc microgrid structure.

between the PV module and inverter stage responsible for MPPT [13]. The output of microconverters can either feed directly into a dc microgrid or can feed into a dc bus that feeds a large centralized or string inverter. Three different types of modular power conditioning systems for ac utility grids are shown in Figure 1.5: (a) single-stage microinverters, (b) two-stage microinverters, and (c) distributed microconverters with a centralized inverter. Figure 1.6 shows an example dc microgrid structure where the output of the microconverter feeds directly to the dc bus. In both of these figures, the microconverter is highlighted in red, as this is the component of the PCS on which the work in this dissertation is focused.

All of these modular configurations are very attractive because when compared to conventional string and centralized systems, they offer far superior MPPT, scalability, and

fault tolerance [15]. Each module and converter combination is connected in parallel which allows independent operation from the rest of the array. This allows for each module to have its own independent MPPT algorithm so maximum power will be extracted from each module. These configurations also have excellent scalability because installations can be scaled by one module/converter combination at a time. Another advantageous feature of modular systems is that, if one unit fails, the rest of the array will remain unaffected and continue to operate. The installation costs of modular systems are higher because there are more power electronics converters, but they are very attractive and becoming more popular due to their superior power optimization, scalability, and fault tolerance.

1.3 Research Objectives and Dissertation Outline

In an effort to reduce the costs of modular power conditioning systems and to increase the performance in order to generate more power for a given PV array, the work in this dissertation proposes a new isolated dc-dc converter topology that is an excellent candidate for PV microconverter applications. The proposed circuit topology can be used as the front end of a two-stage microconverter, in a distributed microconverter with centralized inverter configuration, or in a dc microgrid application. There are five challenging design requirements that must be met:

1. The converter needs to have a simple topology with a low parts count. Because there are many of these converters in a given PV installation, it is important they have a minimum parts count in order to have a low cost and fewer potential failure points.

2. In order to accommodate different types of PV modules operating under different environment conditions, it is important the converter be able to regulate over a wide input-voltage operating range. Typical input-voltage ranges of commercially available modular power conditioning systems are between 15 – 60 V [16-18].
3. The converter needs to have a high boost ratio because the input voltage of a PV microconverter is typically 15 – 60 V while the dc-bus output is typically in the range of 380 – 400 V. This voltage range for the dc bus is required in order to power a 240-V ac inverter which is very common in residential applications in the US.
4. While not strictly required, it is desirable for the microconverter to have galvanic isolation. The benefits of having galvanic isolation in a power conditioning system were discussed in the previous subsection. If a PCS is going to have galvanic isolation, it is desirable to have it implemented in the microconverter rather than the inverter stage. This way the microconverter can be coupled with a highly-efficient non-isolated converter topology of which there are many both in literature and commercially available [19-21]. Additionally, implementing isolation in the microconverter stage makes the high-boost ratio requirement easier to meet because the high frequency isolation transformer can be used to provide a voltage step up.
5. The final design requirement is high power conversion efficiency. Efficiency is the most significant performance metric. It's measured as the ratio of output power versus input power, so a more efficient system will yield more output power given the same input. High-efficiency converters are crucial for maximizing the output power of a PV installation and thus lowering the cost per watt of power generation.

The standard metric for evaluating the efficiency of PV converters and inverters is the weighted California Energy Commission (CEC) efficiency, so naturally this is the metric that will be used to evaluate the proposed converter. The CEC efficiency is a weighted average which puts different weights on different output power operating conditions based on the typical operating conditions of a PV module over the course of a day. An efficiency target of 97.5% CEC is set as this would exceed all microconverters found in literature. There are no parallel-connected microconverters commercially available to date, but commercially available microinverters are in the 94.5 – 96.5% CEC efficiency range [16, 18, 22].

Because of the high boost ratio, wide input range, and isolation requirements, it is difficult to develop a simple converter topology that is capable of reaching high efficiency over the entire input voltage and output power range. This dissertation introduces a new topology that is able to meet all of these goals and is an excellent candidate for modular PV installations. The dissertation outline is as follows:

Chapter 1 gave background information on different types of PV power conditioning systems, the merits of modular power conditioning system, and the challenges associated with developing high-efficiency, low cost microconverters.

Chapter 2 explores existing topologies in literature and introduces a new topology based on the highly-efficient series resonant converter. This chapter provides a detailed analysis of the different operating modes of the proposed converter.

This analysis is validated experimentally with a 300-W microconverter prototype in Chapter 3. Chapter 3 also presents a detailed systematic design procedure that is unique

to the proposed converter, as well as a detailed loss model. The loss model was validated experimentally through efficiency measurements.

Chapter 4 discusses modeling and control of the different operating modes and proposes a smooth transition method to transition smoothly between the different operating modes. The controller designs and transition method are validated experimentally using the same 300-W microconverter prototype.

The proposed converter is designed to be compatible with several different types of modular power conditioning systems, so Chapter 5 explores system-level integration issues the converter will face with different types of systems. First, a novel soft start method is introduced to not only allow the proposed converter to start up with a very large fully discharged capacitive load, but also allows the converter to start up safely with a short-circuited output in case of a dc-bus failure. Next, maximum power point tracking algorithms are discussed, which are an integral part to any PV power conditioning system. Finally, double line frequency ripple rejection algorithms are discussed, which are an integral part to any PV power conditioning system operating with an ac grid.

Chapter 6 focuses on efficiency improvements. First, the merits of using integrated magnetics verses an external resonant inductance are explored. The original prototype used integrated magnetics. In this chapter, a new prototype is designed and tested which utilizes an external resonant inductor and demonstrates significant efficiency improvements. This chapter also proposed a variable frequency efficiency optimization algorithm which also demonstrates significant efficiency improvements.

Finally, Chapter 7 provides a summary of the work presented and proposes future research work.

Chapter 2

Proposed Hybrid Resonant Microconverter Topology

2.1 State-of-the-art Isolated DC-DC Converters

There have been many approaches in literature to develop an isolated dc-dc converter with high efficiency and wide regulation capability. The most commonly used topology is the traditional pulse-width modulated (PWM) flyback converter [23]. The flyback converter is very popular because it is capable of operating over a wide voltage range with simple fixed-frequency PWM operation and has very few components resulting in low costs. The biggest drawbacks to the flyback converter, however, are efficiency limitations due to the high voltage and current stresses of the main switch as well as poor magnetic utilization [24, 25]. Poor magnetic utilization also leads to larger-sized magnetics resulting in lower power density. Both of these drawbacks make the traditional flyback converter unattractive for PV microconverter applications.

Several flyback derivatives have been introduced in an attempt to increase the efficiency of the flyback converter such as the active-clamp flyback [24, 26], dual series resonant active-clamp converter [27, 28], and quasi-resonant boundary conduction mode flyback converters [29]. All of these converters add additional components and therefore additional cost and control complexity, but are able to overcome some of the efficiency limitations of the conventional flyback. The maximum efficiency of these converters is still limited, however, due to high current stresses in the main switch and it is difficult to

guarantee zero-current switching (ZCS) of the output diode(s) for the entire load range. ZCS of the output diodes is important because not only does it reduce switching losses and increase efficiency, but it also minimizes EMI generated by the converter. There have been several other isolated PWM converters implemented in literature that show improved performance over these flyback variants [25, 30, 31], however they each have their own disadvantages such as the inability to guarantee zero-voltage switching (ZVS) over a wide input voltage and load range or high turn-off currents in the switching devices.

Stepping away from PWM-based converters, the most efficient isolated dc–dc converter is the series resonant converter operating at or below the series resonant frequency [32]. This is because it always operates with direct power transfer to the load, the primary-side switches achieve ZVS and ZCS, the output diodes achieve ZCS, and the converter has good transformer utilization. The problem with the series resonant converter, however, is the lack of input voltage regulation that is required for PV applications. Because of these high-efficiency characteristics and lack of regulation, the series resonant converter operating at or below the series resonant frequency is generally used in fixed-input and fixed-output applications. The LLC converter is another high-efficiency isolated resonant converter that is popular in applications where regulation is required [33], but it is difficult to obtain a wide range of regulation while maintaining high efficiency. There has been some research done on optimizing the LLC converter for wide range applications [34, 35], but when the converter is operating far from its series resonant frequency, the light-load efficiency is poor due to large circulating currents. There have also been lots of modified LLC converters proposed in literature that achieve high efficiency while operating under a wide range of input voltage and load currents [36-38], but these involve

adding many extra components, suffer from complex control, and suffer from poor light load efficiency due to large circulating currents. The highest efficiencies that have been demonstrated in literature for PV microconverter applications are in the 95% - 96.7% CEC efficiency range [25, 30, 38-40]. A new topology will now be proposed that will allow much higher efficiencies to be achieved.

2.2 Proposed Topology Introduction and Overview

In order to achieve the highest power conversion efficiency for the majority of the time the microconverter will be operating, it is desirable to optimize the converter to have the highest efficiency when operating at the nominal output voltage of the PV module. The most efficient isolated dc-dc converter is the series resonant converter operating at, or slightly below, the series resonant frequency [32]. However, as previously mentioned, this topology is normally used for fixed-input and fixed-output applications. In order to optimize the efficiency of the proposed microconverter, it will be designed to operate as a series resonant converter for the nominal input voltage.

The topology of the series resonant converter is shown in Figure 2.1 [41]. Here, switches S_1 through S_4 make up a full-bridge switch network. A voltage doubler is used for the output rectifier; these same voltage doubler capacitors are also used as the resonant capacitors C_{r1} and C_{r2} to reduce the parts count. The voltage doubler also helps to achieve the required high-boost ratio and allows for a reduced turns ratio in the isolation transformer. The effective resonant capacitance is the parallel combination of C_{r1} and C_{r2} because they effectively charge and discharge in parallel. L_m and n are the magnetizing inductance and turns ratio of the transformer, respectively. L_r is the resonant inductance

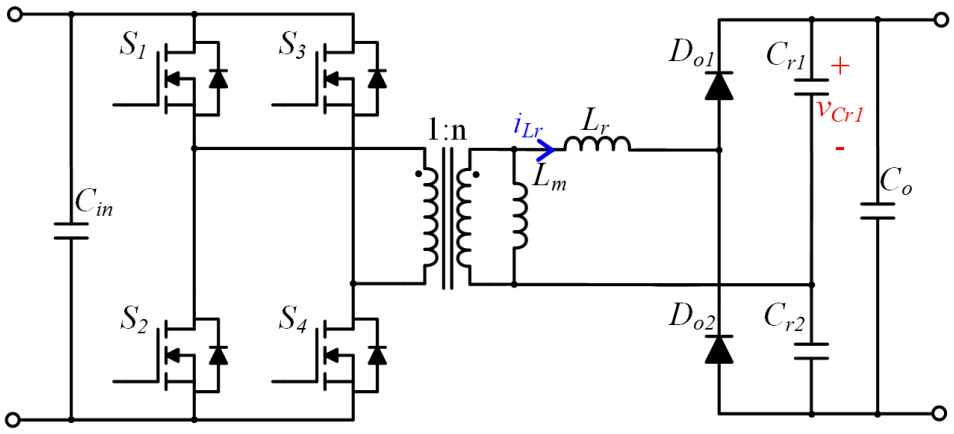


Figure 2.1. Isolated series resonant converter with a voltage doubler output rectifier [41].

and can either be implemented as the leakage inductance of the isolation transformer or the series combination of the leakage inductance and an external resonant inductor. It is possible to use magnetic integration to avoid the size and cost associated with an external resonant inductor [42-44] which will be discussed in more detail in Section 6.1.

The topology for the proposed microconverter is based on the series resonant converter in Figure 2.1. This topology allows the microconverter to operate as a series resonant converter, or in pure series resonant mode (SR Mode), at the nominal input voltage resulting in high efficiency at the most common operating condition. In addition to this mode of operation, the microconverter also needs a way to buck so that it can accommodate input voltages above the nominal as well as a way to boost to accommodate input voltages below the nominal input. In order to buck, the primary-side full-bridge switch network is phase-shift modulated to create a hybrid phase-shifted full-bridge buck and series resonant converter. Phase-shift modulation is performed by adjusting the phase angle, Φ, between the two switching legs of the converter; one is comprised of S_1 and S_2 and the other of S_3 and S_4. This operating mode is very similar to that of the Phase-Shifted Resonant Converter which has previously appeared in literature [45-48]; however this work

will present a more detailed analysis using state-plane trajectory curves which will be presented in detail in Section 2.4. To simplify naming conventions, this mode of operation will be referred to as "Buck Mode."

To add boost capability to the topology, a bidirectional ac switch, S_5, is added across the secondary winding of the isolation transformer [49]. The proposed topology is pictured in Figure 2.2. The ac switch shorts out the secondary winding, allowing the leakage inductance to act as a PWM boost inductor. When the switch turns off, the leakage inductance then resonates with the resonant capacitors. This operation allows the initial conditions of the resonant trajectory to be set, permitting the power flow and conversion ratio to be controlled. This effectively creates a hybrid PWM boost and series resonant converter which adds boost capability to the converter while maintaining the high-efficiency characteristics of the series resonant converter: ZVS and ZCS of the primary-side switches, ZCS of the output diodes, and low circulating currents. The ac switch is pulse-width modulated with a duty cycle of d_{s5} during this mode of operation, and is implemented as two anti-series MOSFETs. To simplify naming conventions, this mode of operation will be referred to as "Boost Mode."

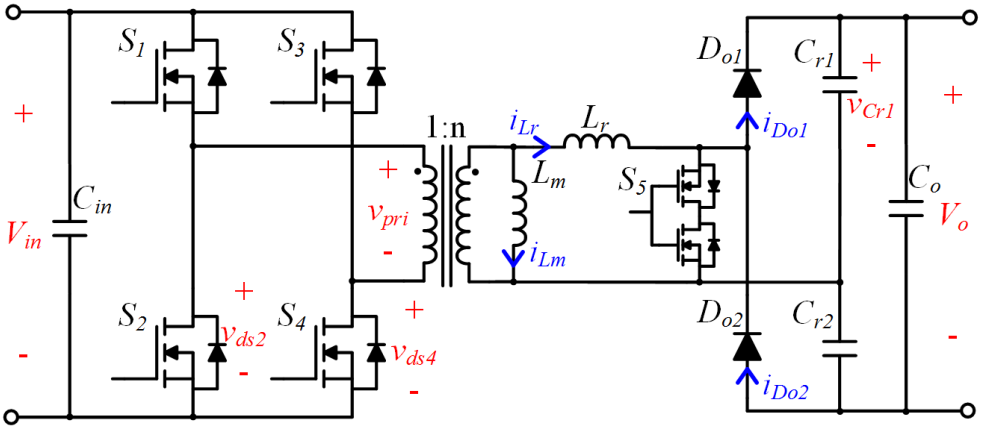


Figure 2.2. Topology of proposed hybrid resonant microconverter [49].

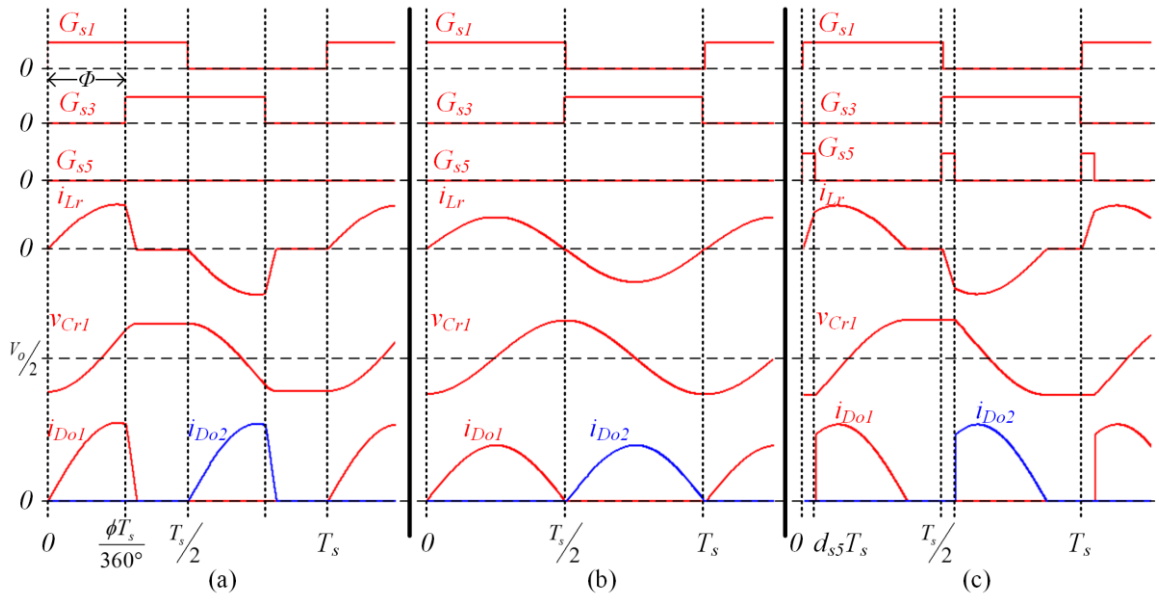


Figure 2.3. Steady-state operating waveforms of the proposed converter operating in (a) Buck Mode, (b) SR Mode, and (c) Boost Mode.

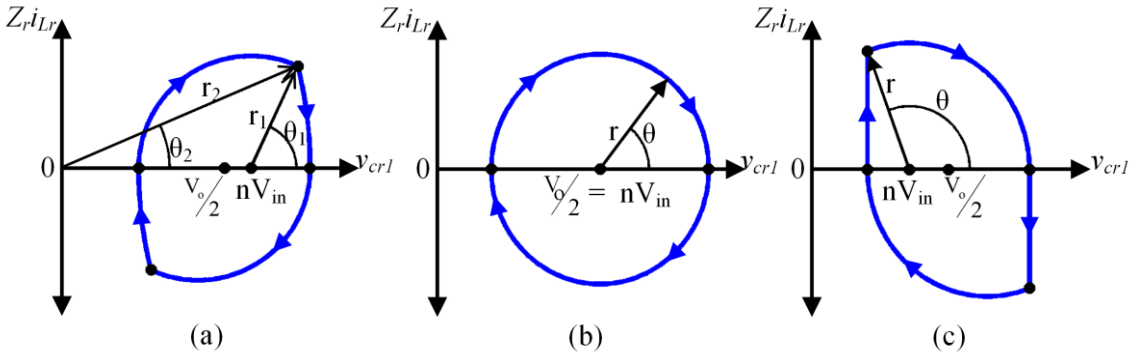


Figure 2.4. State-plane trajectory curves of resonant tank state variables in (a) Buck Mode, (b) SR Mode, and (c) Boost Mode.

Steady-state operating waveform of the proposed converter during all three modes of operation are shown in Figure 2.3. State-plane trajectory curves of the state variables in the resonant tank are shown in Figure 2.4. State-plane analysis reduces the complex converter state variable equations to simple geometry, allowing the converter to be analyzed based on simple geometric figures [50-52]. These state-plane trajectory curves will be used to simplify the analysis of the converter current and voltage waveforms as well as the converter steady-state operating characteristics. The principal of operation—

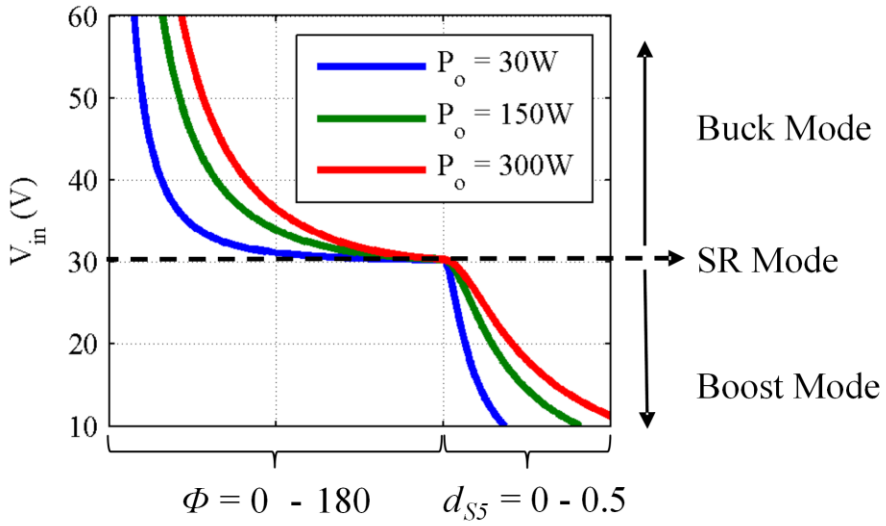


Figure 2.5. Input voltage versus control variable of proposed converter.

including a detailed explanation of the steady-state operating waveforms and state-plane trajectory curves—for all three modes will be discussed in detail in the proceeding sections. Figure 2.5 shows the input voltage versus control variable of the converter. In this example, 30 V is chosen as the nominal input voltage which is where SR Mode occurs. When the input voltage is above the nominal, the primary side devices are phase-shift modulated by controlling Φ and the converter is operating in Buck Mode. When the input voltage is below the nominal, the bidirectional ac switch is pulse-width modulated by controlling d_{s5} and the converter is operating in Boost Mode. Combining these different modes of operation allows the converter to operate at its maximum efficiency at the nominal input voltage [53].

2.3 Series Resonant Converter

2.3.1 Principal of Operation

The operating periods of the series resonant mode of operation are shown Figure 2.6 and the steady-state operating waveforms are shown in Figure 2.7. The steady-state state-plane trajectory curves of the resonant inductor current, i_{Lr}, and resonant capacitor voltage, v_{cr1}, are shown in Figure 2.8 where θ is the angular displacement of the resonant tank and is shown in (2.1) where ω_r is the angular frequency of the resonant tank shown in (2.2). In order to simply the state-plane trajectory analysis, the inductor current is multiplied by the impedance of the resonant tank, Z_r (2.3) so that both axes on the graph share the same units, volts.

$$\theta = \omega_r t \tag{2.1}$$

$$\omega_r = \frac{1}{\sqrt{L_r\left(C_{r1} + C_{r2}\right)}} \tag{2.2}$$

$$Z_r = \sqrt{\frac{L_r}{C_{r1} + C_{r2}}} \tag{2.3}$$

When operating in SR Mode, the switching frequency, F_s, of the primary side devices is equal to the resonant frequency, F_r, as defined in (2.4).

$$F_s = F_r = \frac{\omega_r}{2\pi} = \frac{1}{2\pi\sqrt{L_r\left(C_{r1} + C_{r2}\right)}} \tag{2.4}$$

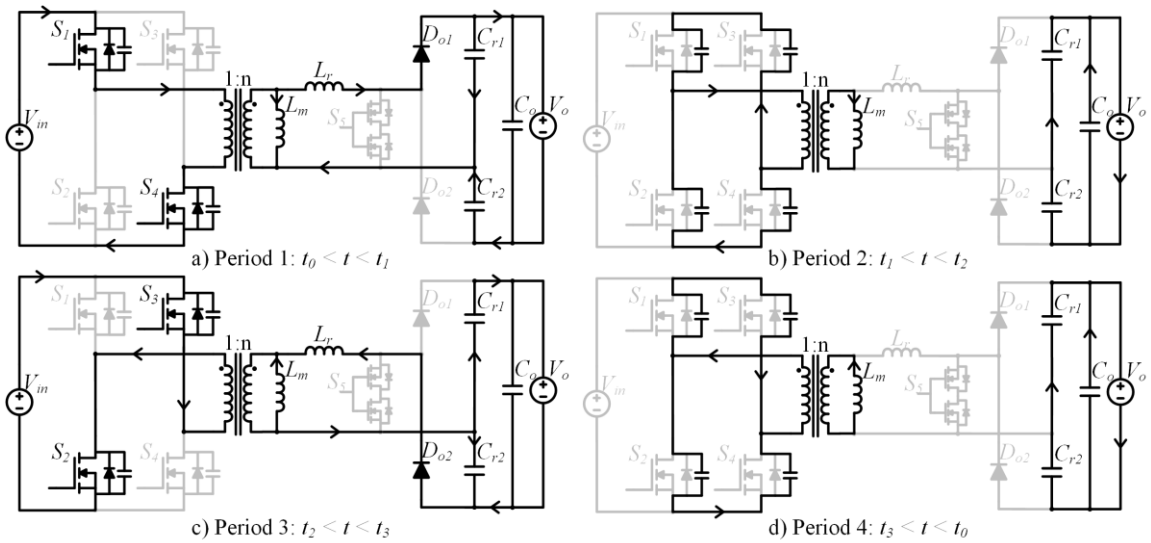


Figure 2.6. Operating periods of proposed converter operating in pure series resonant mode.

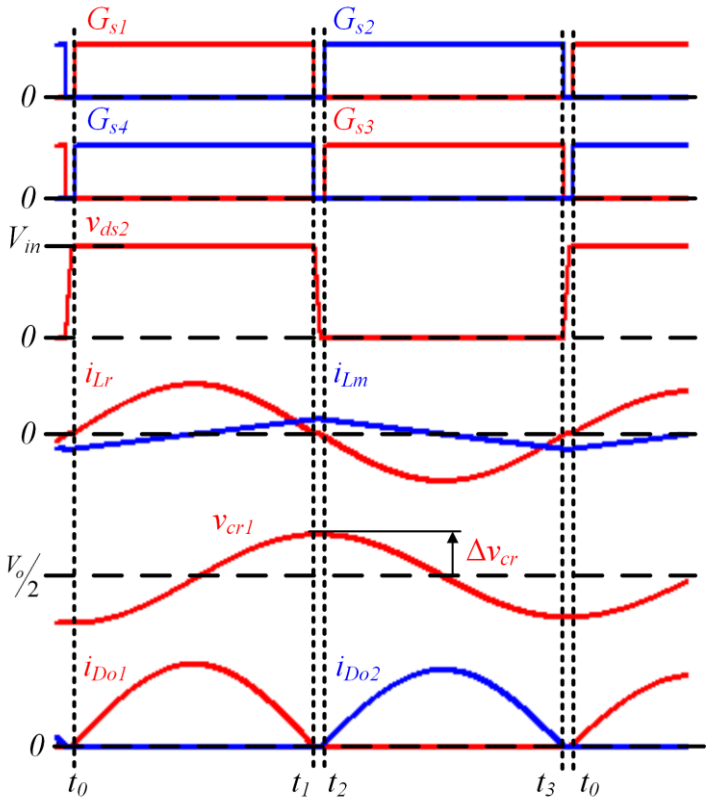


Figure 2.7. Steady-state operating waveforms of converter operating in pure-series resonant mode.

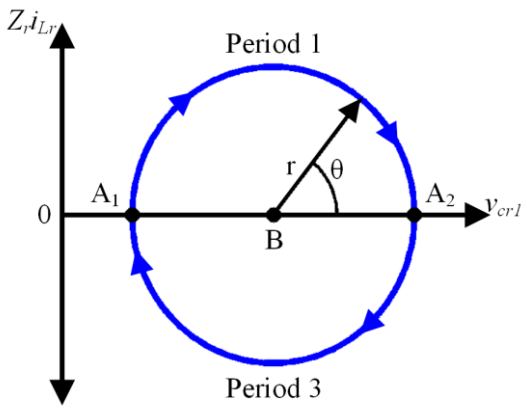


Figure 2.8. State-plane trajectory of resonant tank when converter is operating in pure series resonant mode.

In order to simplify the analysis of the converter, the following assumptions are made:

1. The output capacitance C_o is large enough so that the output voltage V_o can be considered constant during a switching period T_s.
2. C_o is much larger than the resonant capacitors C_{r1} and C_{r2}.
3. C_{r1} and C_{r2} are equivalent in capacitance. This capacitance value will be represented as C_r for the remainder of the paper.

Period 1 [$t_0 < t < t_1$, Figure 2.6. (a)]: Prior to Period 1 beginning, the initial current in L_r is zero and the voltage across C_{r1} is at its minimum value which is shown as point A_1 in Figure 2.8 and is expressed in (2.5) and (2.6).

$$i_{Lr}(t_0) = 0 \tag{2.5}$$

$$v_{cr1}(t_0) = \frac{V_o}{2} - \Delta v_{cr} \tag{2.6}$$

The average value over one switching cycle of v_{cr1} is one half of the output voltage; this is also equal to n times the input voltage, V_{in}, during pure series resonant mode. This

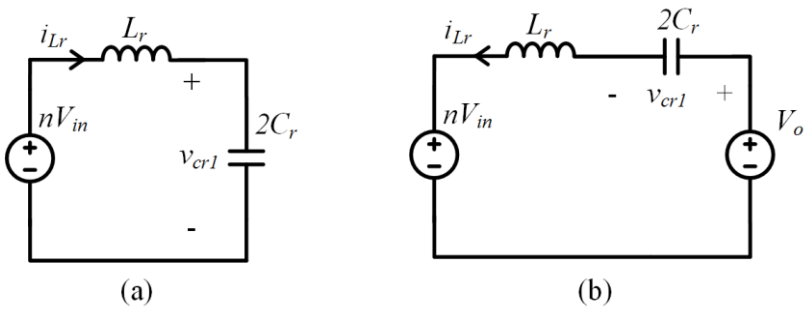


Figure 2.9. Equivalent circuit of resonant tank during (a) Period 1 and (b) Period 3 when converter is operating in pure series resonant mode.

point is shown as B in Figure 2.8. The difference between A_1 and B is the voltage ripple across C_{r1}, Δv_{cr}, which is directly proportional to the output power, P_o, and is expressed in (2.7). During all operating modes, $v_{cr2} = V_o - v_{cr1}$.

$$\Delta v_{cr} = \frac{P_o T_s}{4 V_o C_r} \tag{2.7}$$

At t_0, S_1 and S_4 turn on and Period 1 begins. During this period, V_{in} is applied across the primary winding of the transformer causing L_r and the parallel combination of C_{r1} and C_{r2} to resonate. Here, the operating point moves along the trajectory path from A_1 to A_2. The current through L_r and voltage across C_{r1} are expressed in the time domain in (2.8) and (2.9), respectively, where r is the radius of the trajectory path and is given in (2.10). The center point of the trajectory path is point B in Figure 2.8. The equivalent circuit model of the resonant tank during this operating period is shown in Figure 2.9 (a). During this entire time period, power is directly being transferred from the input to the output.

$$i_{Lr}(t) = \frac{r}{Z_r} \sin(\pi - \omega_r (t - t_0)) \tag{2.8}$$

$$v_{cr1}(t) = nV_{in} + r \cos(\pi - \omega_r (t - t_0)) \tag{2.9}$$

$$r = nV_{in} - \frac{V_o}{2} + \Delta v_{cr} \tag{2.10}$$

During this period, the current in the magnetizing inductance, i_{Lm}, increases linearly because nV_{in} is applied across it. It begins increasing from its initial value in (2.11) and the current is expressed in the time domain during this period in (2.12).

$$i_{Lm}(t_0) = -\frac{nV_{in}T_s}{4L_m} \tag{2.11}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_{in}}{L_m}(t - t_0) \tag{2.12}$$

Since the switching frequency is equal to the resonant frequency, S_1 and S_4 will simultaneously turn off when the resonant inductor current resonates to zero at t_1. This ends Period 1 and the converter enters the first dead time period. By commutating S_1 and S_4 after the resonant inductor current reaches zero, D_{o1} achieves true ZCS. The only current present in S_1 and S_4 during commutation is the magnetizing current. This is very small compared to the resonant current and is required for these devices to achieve ZVS. Because the magnetizing current is very small and is the only current present in S_1 and S_4 during commutation, they are also considered to achieve ZCS.

Period 2 [$t_1 < t < t_2$, Figure 2.6 (b)]: At t_1 switches S_1 and S_4 turn off and the converter enters a dead time period. During this short time period, the magnetizing current is at its peak value and is expressed in (2.13).

$$i_{Lm}(t_1) = i_{Lm}(t_2) = \frac{nV_{in}T_s}{4L_m} \tag{2.13}$$

Since this time period is short, the magnetizing inductor acts as a current source and discharges the parasitic output capacitances of S_2 and S_3 while charging those of S_1 and S_4. As long as the dead time and magnetizing inductance are selected appropriately, the

voltages across S_2 and S_3 will reach zero before t_2, allowing them to be turned on under ZVS conditions. The voltage across S_2, v_{ds2}, is shown in (2.14) where C_{oss} is the effective parasitic output capacitance of one primary side switch. Once C_{oss} is completely discharged, the anti-parallel body diode conducts the magnetizing current until Period 3 begins. i_{Lr} remains zero and v_{cr1} remains unchanged during this time period so the trajectory curve stays at point A_1.

$$v_{ds2}(t) = V_{in} - \frac{n i_{Lm}(t_1)}{2C_{oss}}(t - t_1) \tag{2.14}$$

Period 3 [$t_2 < t < t_3$, Figure 2.6 (c)]: At t_2, S_2 and S_3 turn on under ZVS conditions and Period 3 begins. At the start of this period, i_{Lr} remains zero and v_{cr1} is charged to its maximum value, (2.15), which is represented by point A_2 in Figure 2.8.

$$v_{cr1}(t_2) = \frac{V_o}{2} + \Delta v_{cr} \tag{2.15}$$

Now with S_2 and S_3 on, negative V_{in} is applied to the primary winding of the transformer causing L_r and the parallel combination of C_{r1} and Cr2 to resonate in the opposite direction as Period 1. Here, the operating point moves along the trajectory curve from point A_2 back to A_1. The equivalent circuit model of the resonant tank during this operating period is shown in Figure 2.9 (b). The current through L_r and voltage across C_{r1} are expressed in the time domain in (2.16) and (2.17), respectively. The center point for the trajectory curve during this period is the same as in Period 1: point B in Figure 2.8.

$$i_{Lr}(t) = -\frac{r}{Z_r}\sin(\omega_r(t - t_2)) \tag{2.16}$$

$$v_{cr1}(t) = nV_{in} + r\cos(\omega_r(t - t_2)) \tag{2.17}$$

During this period, i_{Lm} decreases linearly because negative nV_{in} is applied across it. It begins decreasing from its maximum value in (2.18) and the current is expressed in the time domain in (2.19).

$$i_{Lm}(t_2) = i_{Lm}(t_3) = \frac{nV_{in}T_s}{4L_m} \tag{2.18}$$

$$i_{Lm}(t) = i_{Lm}(t_2) - \frac{nV_{in}}{L_m}(t - t_2) \tag{2.19}$$

This period also lasts one half of the switching frequency, and it ends at t_3 when i_{Lr} returns to zero. Once again, this allows D_{o2}, S_2, and S_3 to turn off under ZCS conditions. Power is also directly transferred from the source to the load during this entire time period.

Period 4 [$t_3 < t < t_0$, Figure 2.6 (d)]: After S_2 and S_3 turn off, the converter enters another dead time period. This time the magnetizing inductor current is at its minimum value as was expressed in (2.11). Once again, the dead time period is short enough that the magnetizing inductor will appear as a current source and will discharge the parasitic output capacitances of S_1 and S_4 while charging those of S_2 and S_3. This allows S_1 and S_4 to turn on under ZVS conditions at t_0. The voltage across S_4, V_{ds4}, is shown in (2.20).

$$v_{ds4}(t) = V_{in} - \frac{ni_{Lm}(t_3)}{2C_{oss}}(t - t_3) \tag{2.20}$$

i_{Lr} remains zero and v_{cr1} remains unchanged at its minimum value (2.6) during this time period so the trajectory curve stays at point A_2. At t_0, S_1 and S_4 turn on under ZVS conditions and the operating periods repeat.

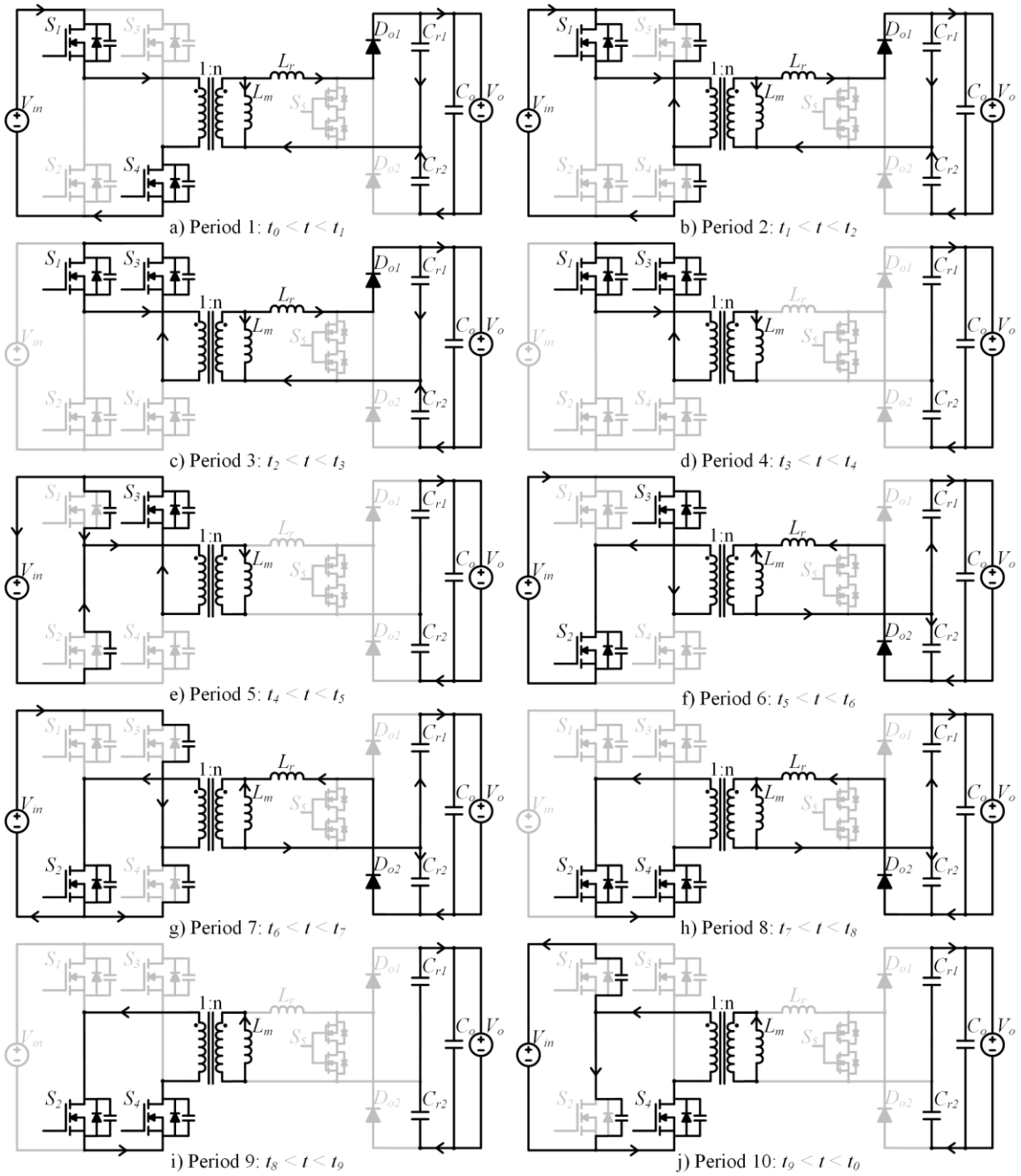


Figure 2.10. Operating periods of proposed converter operating in Buck Mode.

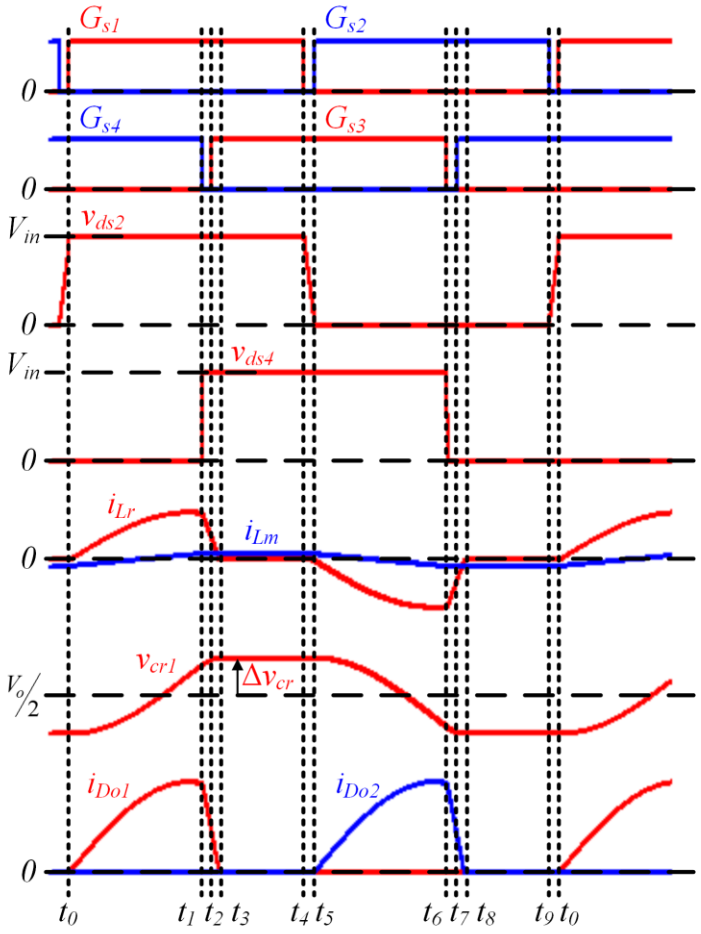


Figure 2.11. Steady-state operating waveforms of converter operating in Buck Mode.

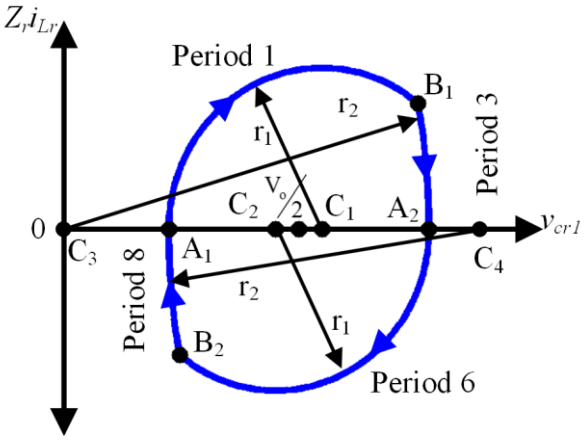


Figure 2.12. State-plane trajectory of resonant tank when converter is operating in Buck Mode.

2.4 Hybrid Phase-Shifted Full Bridge Buck and Series Resonant Converter

2.4.1 Principal of Operation

As discussed in Section 2.2, a Buck Mode of operation is achieved by controlling the phase angle, ϕ, between the two primary-side switching legs. Operating periods of the converter in this mode are shown in Figure 2.10 and steady-state operating waveforms are shown in Figure 2.11. The steady-state state-plane trajectory curves of i_{Lr} and v_{cr1} are shown in Figure 2.12. During this mode, the converter is still operating with a fixed switching frequency which is equal to the resonant frequency.

Period 1 [$t_0 < t < t_1$, Figure 2.10 (a)]: Period 1 in Buck Mode is very similar to Period 1 in SR Mode. Prior to this period beginning, the initial current in L_r is zero and the voltage across C_{r1} is at its minimum value (2.21).

$$v_{cr1}(t_0) = \frac{V_o}{2} - \Delta v_{cr} \tag{2.21}$$

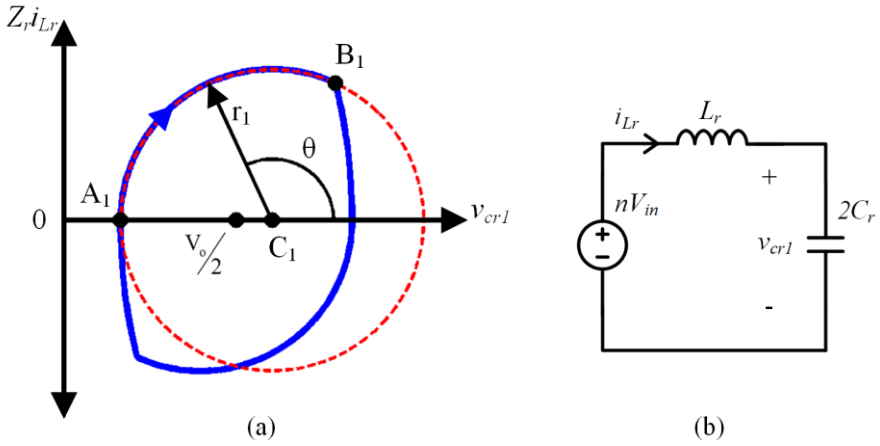


Figure 2.13. (a) State-plane trajectory and (b) equivalent circuit model of resonant tank during Buck Mode Period 1.

During this operating period, V_{in} is applied to the primary winding of the transformer and L_r and the parallel combination of C_{r1} and C_{r2} resonate. The state-plane trajectory path of the resonant network is shown in Figure 2.13 (a) and the equivalent circuit is shown in Figure 2.13 (b). During this period, the trajectory path moves from point A_1 to B_1 with a radius of r_1 (2.22). The center of the trajectory during this operating period is C_1, which is located at (nV_{in}, 0). The time domain equations for i_{Lr} and v_{cr1} are given in (2.23) and (2.24), respectively.

$$r_1 = nV_{in} - V_o/2 + \Delta v_{cr} \tag{2.22}$$

$$i_{Lr}(t) = \frac{r_1}{Z_r}\sin(\pi - \omega_r(t - t_0)) \tag{2.23}$$

$$v_{cr1}(t) = nV_{in} + r_1\cos(\pi - \omega_r(t - t_0)) \tag{2.24}$$

Similar to Period 1 of SR Mode, the magnetizing current increases linearly during this period due to the application of nV_{in} across L_m. The current begins rising from its initial value shown in (2.25) and the current is expressed in the time domain in (2.26).

$$i_{Lm}(t_0) = -\frac{nV_{in}T_s}{2L_m}\frac{\phi}{360°} \tag{2.25}$$

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_{in}}{L_m}(t - t_0) \tag{2.26}$$

Power is transferred directly from the source to the load during this operating period.

Period 2 [$t_1 < t < t_2$, Figure 2.10 (b)]: At t_1, S_4 turns off and the resonance in Period 1 ends early while there is still current present in L_r, and the converter enters a dead time period. The current in L_r, along with the magnetizing current, charges the output capacitance of S_4 and discharges the output capacitance of S_3 as shown in (2.27), where the

values of i_{Lm} and i_{Lr} during this time period are shown in (2.28) and (2.29), respectively. Here Φ is the phase angle in degrees between the two switching legs.

$$v_{ds3}(t) = V_{in} - \frac{n\left(i_{Lm}(t_1) + i_{Lr}(t_1)\right)}{2C_{oss}}(t - t_1) \tag{2.27}$$

$$i_{Lm}(t_1) = i_{Lm}(t_2) = \frac{nV_{in}T_s}{2L_m}\frac{\phi}{360°} \tag{2.28}$$

$$i_{Lr}(t_1) = i_{Lr}(t_2) = \frac{r_1}{Z_r}\sin\left(\pi - \omega_r T_s \frac{\phi}{360°}\right) \tag{2.29}$$

This is a very short time period so L_m and L_r act as current sources as the current in both inductors remains relatively constant. While S_4 doesn't turn off under ZCS conditions, the presence of the resonant current in the switch guarantees S_3 will achieve ZVS turn-on at t_2. When the output capacitance of S_3 is fully discharged, the body diode conducts until S_3 is turned on at t_2.

Period 3 [$t_2 < t < t_3$, Figure 2.10 (c)]: When S_3 turns on under ZVS conditions at t_2, the dead time period ends and another period of resonance begins. During this time period, both S_1 and S_3 are on so the primary side of the isolation transformer is shorted and

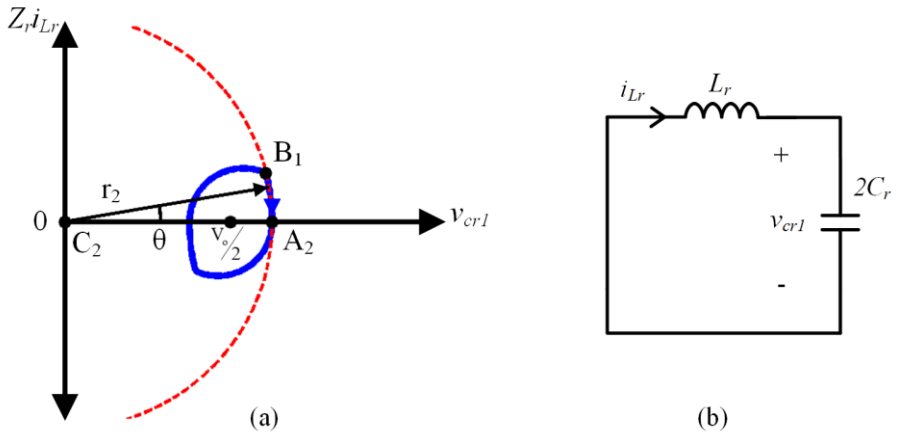


Figure 2.14. (a) State-plane trajectory and (b) equivalent circuit model of resonant tank during Buck Mode Period 3.

zero volts is applied. The resonant tank now begins another resonant trajectory shown in Figure 2.14 (a). The equivalent circuit of the resonant tank during this time period is shown in Figure 2.14 (b). During this period, the trajectory path moves from point B_1 to A_2 with a radius of r_2 (2.30). The center point of this path is point C_2 located at the origin, (0,0). The time domain equations of i_{Lr} and v_{cr1} are given in (2.31) and (2.32), respectively, where θ_2 is the initial angle of the resonant period set by the values of i_{Lr} and v_{cr1} at the end of Period 1. This angle will be explained in more detail in Section 2.4.2.

$$r_2 = {V_o}/{2} + \Delta v_{cr} \tag{2.30}$$

$$i_{Lr}(t) = \frac{r_2}{Z_r}\sin(\theta_2 - \omega_r(t - t_2)) \tag{2.31}$$

$$v_{cr1}(t) = r_2\cos(\theta_2 - \omega_r(t - t_2)) \tag{2.32}$$

The magnetizing current remains unchanged during this time period since zero volts is applied across L_m. It remains at its maximum value in (2.28).

Period 4 [$t_3 < t < t_4$, Figure 2.10 (d)]: Once the resonant current reaches zero, the output diodes prevent the current from becoming negative and the converter enters an idle mode, or discontinuous conduction mode (DCM), where no power is transferred from the source or to the load. This period is important for maintaining constant frequency operation and ensuring ZCS of the output diodes and primary side MOSFETs S_1 and S_2. This mode lasts until half of the switching period is complete. During this time period, i_{Lr} remains zero and v_{cr1} remains at its maximum value (2.33) so the resonant trajectory remains at point A_2.

$$v_{cr1}(t_3) = v_{cr1}(t_4) = \frac{V_o}{2} + \Delta v_{cr} \tag{2.33}$$

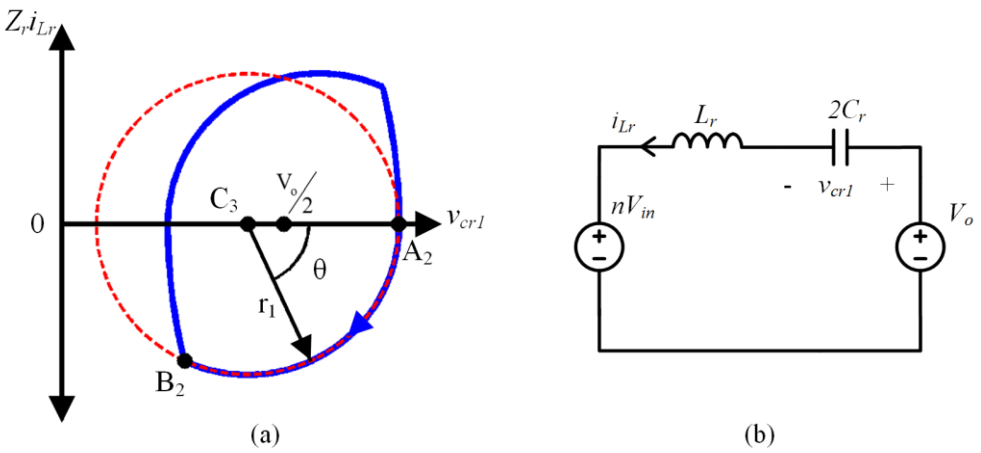


Figure 2.15. (a) Steady-state trajectory and (b) equivalent circuit model of resonant tank during Buck Mode Period 6.

Period 5 [$t_4 < t < t_5$, Figure 2.10 (e)]: At t_4, S_1 turns off and another dead time period begins. The resonant current is zero at this time so S_1 turns off under ZCS conditions. This dead time period is very short, so the magnetizing current acts as a current source and discharges the output capacitance of S_2 while charging that of S_1. The voltage across S_2 is given in (2.34).

$$v_{ds2}(t) = V_{in} - \frac{n i_{Lm}(t_4)}{2C_{oss}}(t - t_4) \tag{2.34}$$

The value of the magnetizing current is still (2.28) and is dependent on ϕ, so ZVS is conditional based on the operating conditions. As a result, ZCS but not ZVS can always guaranteed for both S_1 and S_2.

Period 6 [$t_5 < t < t_6$, Figure 2.10 (f)]: After the dead time period, S_2 turns on under ZVS conditions and another resonant period begins. S_2 and S_3 are now on, resulting in negative V_{in} being applied across the primary winding of the transformer. This causes L_r and the parallel combination of C_{r1} and C_{r2} to resonate along the trajectory path shown in Figure 2.15 (a). The equivalent circuit during this period is shown in Figure 2.15 (b).

During this period the trajectory moves from point A_2 to B_2 with a radius of r_1 and is centered around point C_3 which is located at (V_o-nV_{in}, 0). Time domain equations for i_{Lr} and v_{cr1} are given in (2.35) and (2.36), respectively. The initial condition for i_{Lr} is still zero and v_{cr1} is at its maximum value previously expressed in (2.33).

$$i_{Lr}(t) = -\frac{r_1}{Z_r}\sin(\omega_r(t-t_5)) \tag{2.35}$$

$$v_{cr1}(t) = V_o - nV_{in} + r_1\cos(\omega_r(t-t_5)) \tag{2.36}$$

Now the magnetizing current decreases linearly according to (2.37) from the initial condition of its maxium value in (2.28).

$$i_{Lm}(t) = i_{Lm}(t_5) - \frac{nV_{in}}{L_m}(t-t_5) \tag{2.37}$$

Once again, power is transferred directly from the source to the load during this operating period.

Period 7 [$t_6 < t < t_7$, Figure 2.10 (g)]: At t_6, S_3 turns off, and once again the resonance in Period 6 ends early while there is still current present in L_r. This current, along with the magnetizing current, charges the output capacitance of S_3 while discharging that of S_4 according to (2.38) where the current in L_r is expressed in (2.39) and the current in L_m is at its minimum value (2.25). This is also a very short time period so L_m and L_r appear as current sources and the current in both inductors remains constant.

$$v_{ds4}(t) = V_{in} - \frac{n(i_{Lm}(t_6) + i_{Lr}(t_6))}{2C_{oss}}(t-t_6) \tag{2.38}$$

$$i_{Lr}(t_6) = -\frac{r_1}{Z_r}\sin\left(\omega_r T_s \frac{\phi}{360°}\right) \tag{2.39}$$

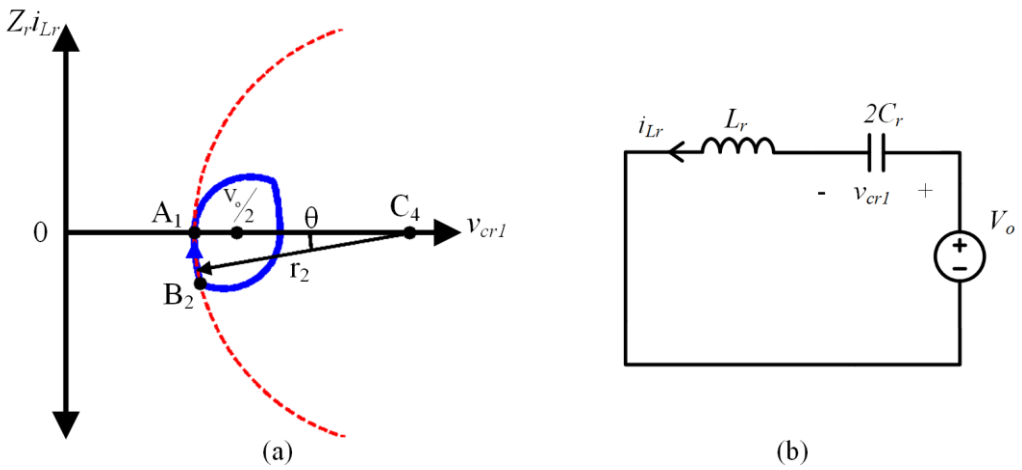


Figure 2.16. (a) Steady-state trajectory and (b) equivalent circuit model of resonant tank during Buck Mode Period 8.

Once the output capacitance of S_4 is fully discharged, the body diode conducts until the switch turns on under ZVS conditions at t_7.

Period 8 [$t_7 < t < t_8$, Figure 2.10 (h)]: S_4 turns on under ZVS conditions at t_7 and another period of resonance begins. This time S_2 and S_4 are on, so the primary winding of the transformer is again shorted and zero volts is applied to the primary winding of the transformer. The state-plane trajectory path during this time period is shown in Figure 2.16 (a) and the equivalent circuit of the resonant tank is shown in Figure 2.16 (b). The trajectory moves from point B_2 back to A_1 with a radius of r_2. The trajectory path is now centered around C_4 which is located at (V_o, 0). Time domain equations of i_{Lr} and v_{cr1} are shown in (2.40) and (2.41) respectively.

$$i_{Lr}(t) = \frac{r_2}{Z_r}\sin(\pi + \theta_2 - \omega_r(t - t_7)) \tag{2.40}$$

$$v_{cr1}(t) = V_o - nV_{in} + r_1\cos(\pi + \theta_2 - \omega_r(t - t_5)) \tag{2.41}$$

The magnetizing current remains unchanged during this time period since zero volts is applied across it. It remains at its minimum value previously expressed in (2.25).

Period 9 [$t_8 < t < t_9$, Figure 2.10 (i)]: Now, when the resonant current reaches zero at t_8, the output diodes prevent the resonant current from becoming positive and the converter enters another DCM period. This ensures that the output diodes and primary side MOSFETs S_1 and S_2 will once again achieve ZCS. During this period, i_{Lr} remains zero and v_{cr1} remains at its minimum value (2.42), so the resonant trajectory remains at point A_1.

$$v_{cr1}(t_8) = v_{cr1}(t_9) = \frac{V_o}{2} - \Delta v_{cr} \tag{2.42}$$

Period 10 [$t_9 < t < t_0$, Figure 2.10 (j)]: S_2 turns off at t_9 under ZCS conditions and the converter enters another dead time period. Once again, this dead time period is very short so the magnetizing current acts as a current source charges the output capacitance of S_2 while discharging that of S_1 according to (2.43). The value of the magnetizing current during this period is shown in (2.44). At t_0, S_1 turns on and the operating periods repeat. Again, ZVS turn-on of S_1 is not guaranteed and is conditional based upon the phase angle, Φ.

$$v_{ds1}(t) = V_{in} - \frac{n i_{Lm}(t_9)}{2C_{oss}}(t - t_9) \tag{2.43}$$

$$i_{Lm}(t_9) = i_{Lm}(t_0) = -\frac{n V_{in} T_s}{2L_m}\frac{\phi}{360°} \tag{2.44}$$

2.4.2 Conversion Ratio

The phase angle and conversion ratio of the converter operating in Buck Mode can be determined using the state-plane trajectory curve. The trajectory curve is symmetrical, so periods 1 and 3 will be used for the following analysis, as using Periods 6 and 8 would yield identical results. The radii of the two resonant period trajectory paths, r_1 and r_2, as

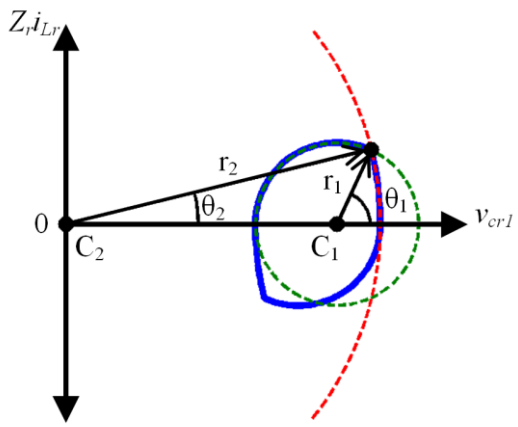


Figure 2.17. State-plane trajectory path of the converter operating in Buck Mode used for determining duty cycle and conversion ratio.

well as the centers of the paths are dependent on both the output power level and the conversion ratio. For a known operating condition, the required phase angle can be determined by finding the intersection point of the two trajectory paths, as shown in Figure 2.17.

Using the standard form for the equation of a circle, the trajectory of Period 1 is defined in (2.45) and the trajectory of Period 3 is defined in (2.46).

$$(v_{cr1} - nV_{in})^2 + (Z_r i_{Lr})^2 = r_1^2 \tag{2.45}$$

$$(v_{cr1})^2 + (Z_r i_{Lr})^2 = r_2^2 \tag{2.46}$$

The intersection of the two circles occurs at the end of Period 1, t_1, so the equations are equal at this point in time. Equating the two circles at t_1 (2.47) gives an equation for the value of v_{cr1} at the intersection point (2.48).

$$(v_{cr1}(t_1) - nV_{in})^2 + (Z_r i_{Lr}(t_1))^2 - r_1^2 = (v_{cr1}(t_1))^2 + (Z_r i_{Lr}(t_1))^2 - r_2^2 \tag{2.47}$$

$$v_{cr1}(t_1) = \frac{V_o}{2} - \Delta v_{cr} + \frac{P_o T_s}{4nV_{in}C_r} \tag{2.48}$$

The length of Period 1 depends on the phase angle, Φ, and is expressed in (2.49). Using (2.9) from the Period 1 analysis, another equation for the value of v_{cr1} at the intersection can be determined (2.50). Equating (2.48) and (2.50) allows the phase angle for a given operating condition to be solved for (2.51).

$$t_1 - t_0 = \frac{\phi}{360°} T_s \tag{2.49}$$

$$v_{cr1}(t_1) = nV_{in} + r_1 \cos\left(\pi - \frac{\phi}{360°}\omega_r T_s\right) \tag{2.50}$$

$$\phi = \frac{360°}{\omega_r T} \cos^{-1}\left(\frac{r_1 - \frac{P_o T_s}{4nV_{in}C_r}}{r_1}\right) \tag{2.51}$$

Now that Φ is known, the length of Period 3 can now be calculated. At the end of Period 1, the trajectory is at the angle θ_1, which is calculated in (2.52).

$$\theta_1 = \pi - \frac{\phi}{360°}\omega_r T_s \tag{2.52}$$

The state variables at this point in time are going to have the same values as when Period 3 beings. Equating (2.29) at t_1 to (2.31) at t_2, a formula for the initial angle of Period 3, θ_2, can be developed. θ_2 will always be small because the amount of current present in the resonant tank multiplied by the impedance, Z_r, is relatively small compared to the radius of the trajectory path. Therefore, the small-angle approximation can be used to determine the value of θ_2 (2.53).

$$\sin(\theta_2) = \frac{r_1}{r_2}\sin(\theta_1), \quad \theta_2 \approx \frac{r_1}{r_2}\sin(\theta_1) \tag{2.53}$$

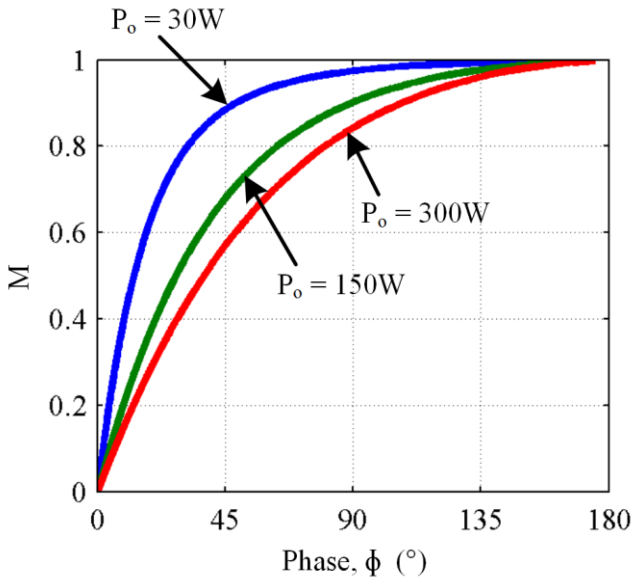


Figure 2.18. Conversion ratio of the converter operating in Buck Mode under different output power operating conditions.

The amount of time Period 3 takes to complete is calculated in (2.54).

$$t_3 - t_2 = \frac{\theta_2}{\omega_r} \tag{2.54}$$

The conversion ratio, M, of the converter operating in Buck Mode is plotted versus Φ for different output powers in Figure 2.18. M is defined in (2.55) where n is the transformer turns ratio and the factor of 2 is from the voltage doubler rectifier.

$$M = \frac{V_o}{2nV_{in}} \tag{2.55}$$

2.5 Hybrid PWM Boost and Series Resonant Converter

2.5.1 Principal of Operation

A Boost Mode of operation is achieved by pulse-width modulating the ac switch, S_5. Operating periods of the converter in this mode are shown in Figure 2.19 and steady-state operating waveforms are shown in Figure 2.20. The steady-state state-plane trajectory curves of the resonant tank state variables are shown in Figure 2.21. During this mode, the

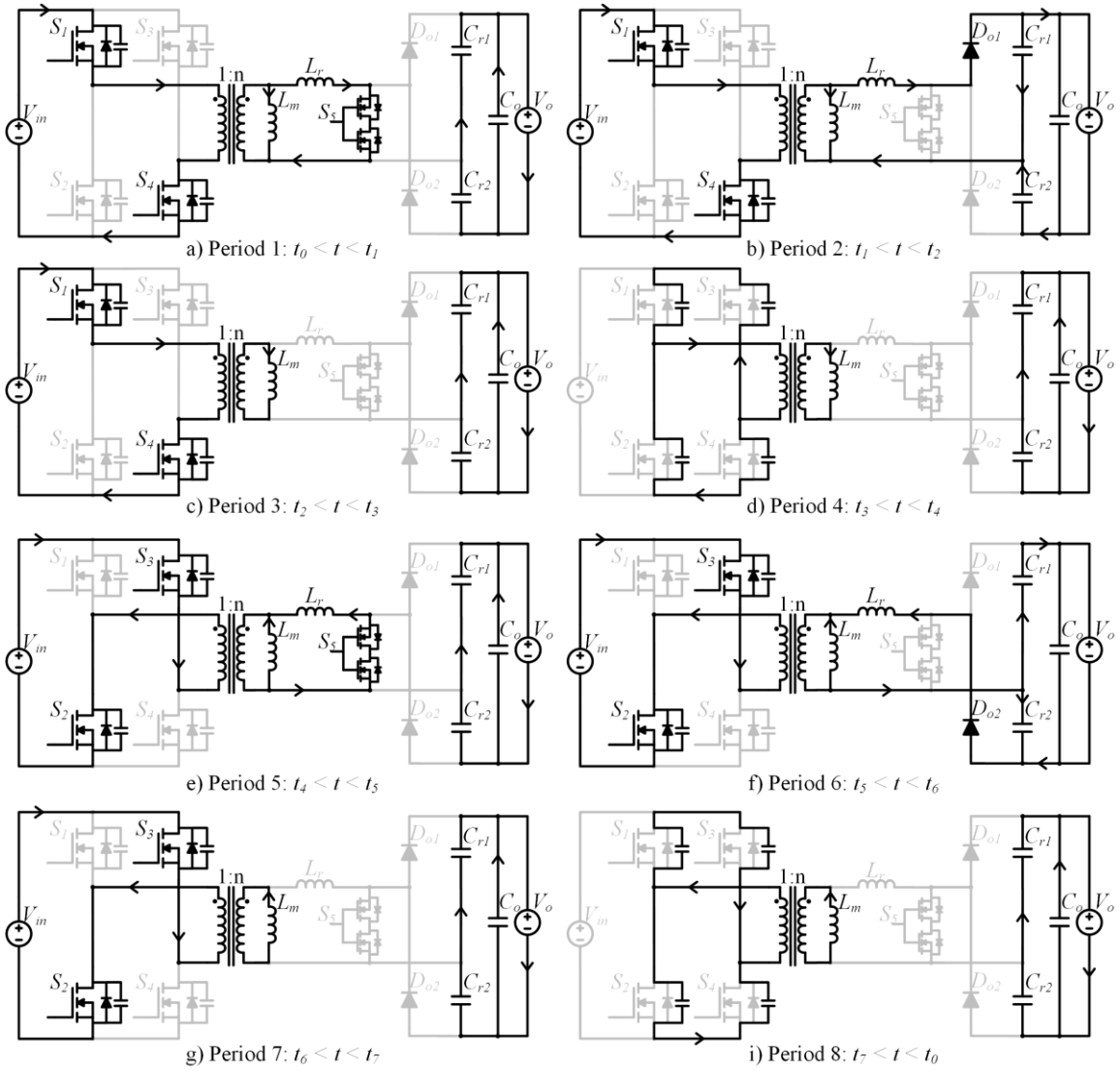


Figure 2.19. Operating periods of proposed converter operating in Boost Mode.

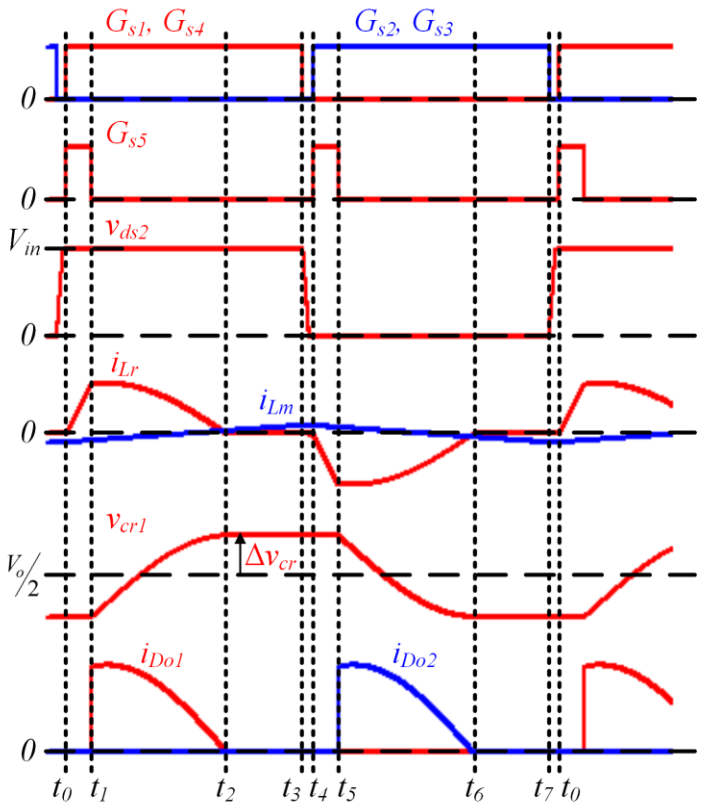


Figure 2.20. Steady-state operating waveforms of the converter operating in Boost Mode.

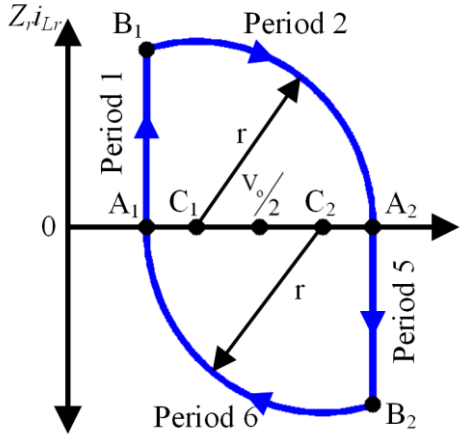


Figure 2.21. State-plane trajectory path of resonant tank when the converter is operating in Boost Mode.

converter is still operating with a fixed switching frequency and the primary side MOSFET switching legs are switched with a phase angle of 180°, similar to SR Mode. In order to achieve regulation, S_5 will be switched at twice the resonant frequency.

Period 1 [$t_0 < t < t_1$, Figure 2.19 (a)]: During Periods 1 through 3, primary side switches S_1 and S_4 are on resulting in a positive voltage V_{in} across the primary winding of the transformer. Prior to S_5 turning on and Period 1 beginning, the resonant current is zero and the voltage across C_{r1} is at its minimum value that is shown as point A_1 in Figure 2.21.

At t_0, S_1, S_4, and S_5 turn on and Period 1 begins. During this period, the converter operates similar to a conventional PWM boost converter. S_5 shorts the secondary winding of the transformer—or the series combination of the secondary winding and external resonant inductor—causing L_r to act as a boost inductor with the current through it increasing linearly according to (2.56). The voltages across the resonant capacitors stay relatively constant during this operating period as shown in (2.57). Here, the operating point moves along the trajectory curve from point A_1 to B_1.

$$i_{Lr}(t) = \frac{n V_{in}}{L_r}(t - t_0) \tag{2.56}$$

$$v_{cr1}(t_0) = v_{cr1}(t_1) = \frac{V_o}{2} - \Delta v_{cr} \tag{2.57}$$

Due to the application of the positive input voltage across the primary winding of the transformer, the magnetizing current increases linearly from its initial value in (2.58) according to (2.59).

$$i_{Lm}(t_0) = -\frac{n V_{in} T_s}{4 L_m} \tag{2.58}$$

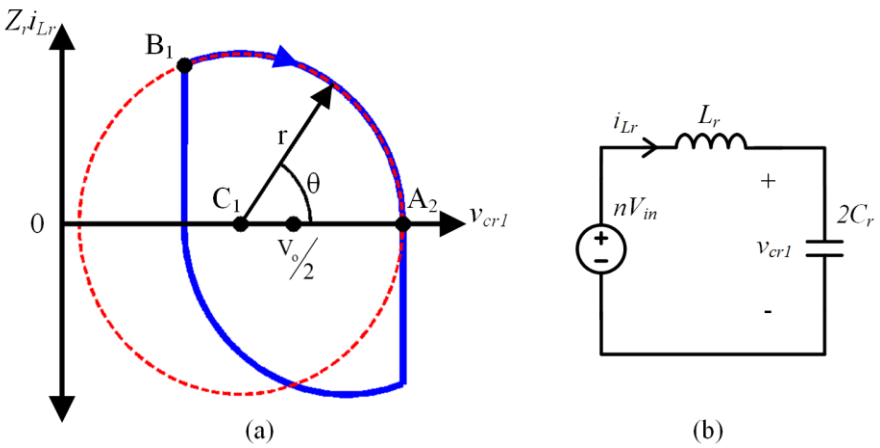


Figure 2.22. (a) Steady-state trajectory and (b) equivalent circuit model of resonant tank during Boost Mode Period 2.

$$i_{Lm}(t) = i_{Lm}(t_0) + \frac{nV_{in}}{L_m}(t - t_0) \tag{2.59}$$

Period 2 [$t_1 < t < t_2$, Figure 2.19 (b)]: At t_1, S_5 turns off and now the converter enters a series resonant period. At the beginning of this period, the current in L_r is charged to the initial condition shown in (2.60) from the previous PWM boost period.

$$i_{Lr}(t_1) = \frac{nV_{in}d_{s5}T_s}{L_r} \tag{2.60}$$

Now L_r and the parallel combination of C_{r1} and C_{r2} resonate from this initial condition. The state-plane trajectory curve of the resonant tank is shown in Figure 2.22 (a) and the equivalent circuit model is shown in Figure 2.22 (b). During this period, the resonant tank moves along the trajectory curve form point B_1 to A_2 with a radius of r (2.61). The center of the trajectory during this operating period is C_1, which is located at (nV_{in}, 0). The time domain equations for i_{Lr} and v_{cr1} are given in (2.62) and (2.63), respectively, where θ_1 is the initial angle of the resonant period that is determined by the initial conditions set by Period 1.

$$r = \frac{V_o}{2} + \Delta v_{cr} - n V_{in} \tag{2.61}$$

$$i_{Lr}(t) = \frac{r}{Z_r} \sin(\theta_1 - \omega_r (t - t_1)) \tag{2.62}$$

$$v_{cr1}(t) = n V_{in} + r \cos(\theta_1 - \omega_r (t - t_1)) \tag{2.63}$$

During this operating period, S_1 and S_4 remain on, so V_{in} is still applied to the primary winding of the transformer resulting in the magnetizing current still increasing according to (2.59). Power is transferred directly from the source to the load during this operating period.

Period 3 [$t_2 < t < t_3$, Figure 2.19 (c)]: When the resonant current reaches zero, the output diodes prevent the current from becoming negative and the converter enters a DCM period. This period ensures the output diodes and primary side MOSFETs S_1 and S_4 will achieve ZCS. Positive V_{in} is still applied to the primary winding of the transformer so the magnetizing current still increases according to (2.59). During this period, i_{Lr} remains zero and v_{cr1} remains at its maximum value (2.64), so the resonant trajectory remains at point A_2.

$$v_{cr1}(t_2) = v_{cr1}(t_3) = \frac{V_o}{2} + \Delta v_{cr} \tag{2.64}$$

Period 4 [$t_3 < t < t_4$, Figure 2.19 (d)]: At t_3, S_1 and S_4 turn off under ZCS conditions and the converter enters a dead time period. At this point, the magnetizing current is at its peak value (2.65) and appears as a current source during this short time period. This current discharges the parasitic output capacitances of S_2 and S_3 while charging those of S_1 and S_4. Once again, as long as the magnetizing inductance is designed appropriately, the voltages

across S_2 and S_3 will be zero at t_4 allowing them to be turned on under ZVS conditions. The voltage across S_2 is expressed in (2.66).

$$i_{Lm}(t_3) = i_{Lm}(t_4) = \frac{nV_{in}T_s}{4L_m} \tag{2.65}$$

$$v_{ds2}(t) = V_{in} - \frac{ni_{Lm}(t_3)}{2C_{oss}}(t - t_3) \tag{2.66}$$

Period 5 [$t_4 < t < t_5$, Figure 2.19 (e)]: During Periods 5 through 7, primary side switches S_1 and S_4 are on resulting in the application of negative V_{in} across the primary winding of the transformer. Prior to this period beginning, the resonant current is still zero and the voltage across C_{r1} is still at its maximum value (2.64). This point is shown as point A_2 in Figure 2.21.

At t_4, S_5 turns on and the converter enters another PWM boost period. The current in L_r and voltage across C_{r1} are shown in (2.67) and (2.68), respectively. Here, the operating point moves along the trajectory curve from point A_2 to B_2

$$i_{Lr}(t) = -\frac{nV_{in}}{L_r}(t - t_4) \tag{2.67}$$

$$v_{cr1}(t_4) = v_{cr1}(t_5) = \frac{V_o}{2} + \Delta v_{cr} \tag{2.68}$$

During this operating period, the magnetizing current is linearly decreasing as shown in (2.69) due to negative V_{in} applied across the primary of the transformer.

$$i_{Lm}(t) = i_{Lm}(t_4) + \frac{nV_{in}}{L_m}(t - t_4) \tag{2.69}$$

Period 6 [$t_5 < t < t_6$, Figure 2.19 (f)]: At t_5 the ac switch turns off and the converter enters another series resonant period. Once again, L_r and the parallel combination of C_{r1} and C_{r2} resonate with an initial resonant current set by Period 5 (2.70).

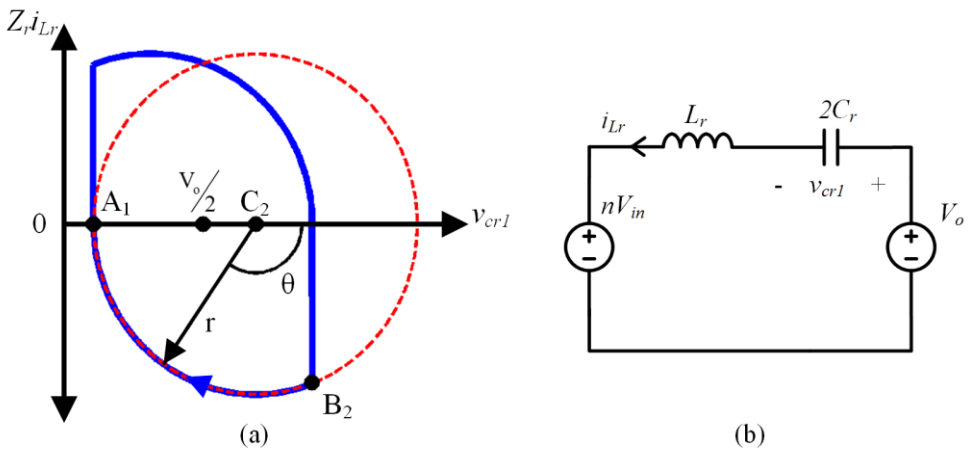


Figure 2.23. (a) Steady-state trajectory and (b) equivalent circuit model of resonant tank during Boost Mode Period 6.

$$i_{Lr}(t_5) = -\frac{nV_{in}d_{s5}T_s}{L_r} \tag{2.70}$$

The state-plane trajectory curve of the resonant tank is shown in Figure 2.23 (a) and the equivalent circuit model is shown in Figure 2.23 (b). Here, the resonant tank moves along the trajectory curve from point B_2 to A_1 with a radius of r and a center point of C_2 which is (V_o–nV_{in},0). The current in L_r and voltage across C_{r1} are given in (2.71) and (2.72), respectively. The magnetizing current is still decreasing according to (2.69).

$$i_{Lr}(t) = \frac{r}{Z_r}\sin(\pi + \theta_1 - \omega(t - t_5)) \tag{2.71}$$

$$v_{cr1}(t) = V_o - nV_{in} + r\cos(\pi + \theta_1 - \omega(t - t_5)) \tag{2.72}$$

Period 7 [$t_6 < t < t_7$, Figure 2.19 (g)]: Once the current in L_r returns to zero, the converter enters another DCM period. At this point, the voltage across C_{r1} has returned to its minimum value where the operating point stays constant until S_2 and S_3 turn off as seen in (2.73). Here, the operating point stays at point A_1 on the trajectory curve.

$$v_{cr1}(t_6) = v_{cr1}(t_7) = \frac{V_o}{2} - \Delta v_{cr} \tag{2.73}$$

Period 8 [$t_7 < t < t_0$, Figure 2.19 (h)]: At t_7, S_2 and S_3 turn off under ZCS conditions and the converter enters another dead time period. This time, the magnetizing current is at its minimum value (2.74) and discharges the output capacitances of S_1 and S_4 while charging those of S_2 and S_3. This allows S_1 and S_4 to turn on under ZVS conditions at t_0 where the operating periods then repeat. The voltage across S_1, v_{ds1}, is expressed in (2.75).

$$i_{Lm}(t_7) = i_{Lm}(t_0) = \frac{nV_{in}T_s}{4L_m} \tag{2.74}$$

$$v_{ds1}(t) = V_{in} - \frac{ni_{Lm}(t_7)}{2C_{oss}}(t - t_7) \tag{2.75}$$

2.5.2 Conversion Ratio

In order to derive the duty cycle and conversion ratio of the proposed converter operating in Boost mode, a closer looks needs to be taken at the trajectory curve. Since the trajectory curve is symmetrical, only Periods 1 and 2 will be considered here, as the analysis using Periods 5 and 6 would yield identical results. Figure 2.24 shows the trajectory curve of the state variables in the resonant network and the initial angle, θ_1, of the trajectory curve when entering Period 2. The length of Period 1 is $d_{s5}T_s$ and therefore is responsible for setting the initial conditions for the resonant period that will result in the proper conversion ratio and output power.

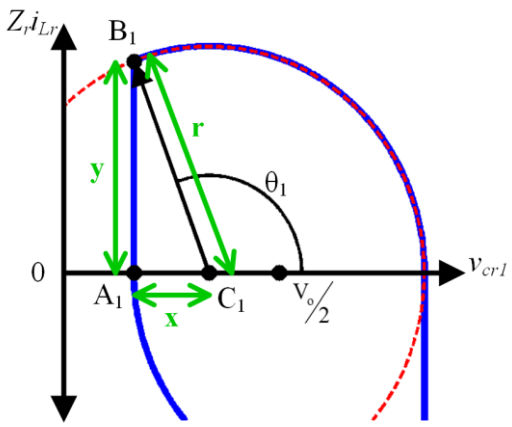


Figure 2.24. State-plane trajectory of resonant tank when the converter is operating in Boost Mode, along with the triangle used for determining the duty cycle.

To determine the required duty cycle, the right triangle that is formed by points A_1, B_1, and C_1 in Figure 2.24 can be analyzed. The length of the sides formed by points A_1 and C_1 as well as the side formed by points B_1 and C_1 are dependent on the conversion ratio and output power. Therefore, the length of the side formed by points A_1 and B_1 and the duty cycle can be determined using Pythagoreans Theorem. The hypotenuse of the triangle has a length r as previously defined in (2.61). Let the bottom side of the triangle be defined as x whose length is expressed in (2.76). Let the left side of the triangle be defined as y whose length is expressed in (2.77).

$$x = C_1 - A_1 = nV_{in} - \frac{V_o}{2} + \Delta v_{cr} \tag{2.76}$$

$$y = Z_r i_{Lr}(t_1) = \frac{Z_r n V_{in} d_{s5} T_s}{L_r} \tag{2.77}$$

Plugging this in to Pythagoreans Theorem (2.78) allows the required duty cycle to be solved for in (2.79). It can be seen that the duty cycle of the proposed converter is highly dependent on both the conversion ratio and the output power. Under most operating

conditions, the duty cycle of S_5 will be small so direct power transfer from the source to the load will occur during most of the switching cycle.

$$y = \sqrt{r^2 - x^2} \tag{2.78}$$

$$d_{s5} = \frac{1}{nV_{in}} \sqrt{\frac{L_r P_o}{T_s} \left(1 - \frac{2nV_{in}}{V_o} \right)} \tag{2.79}$$

Now, the length of the resonant period, Period 2, can be determined by calculating the angle, θ_1, which is a result of the initial conditions set by d_{s5}. θ_1 is calculated in (2.80) by taking the arccosine of the sides x and r.

$$\theta_1 = \pi - \cos^{-1}\left(\frac{x}{r}\right) = \cos^{-1}\left(\frac{r - 2\Delta v_{cr}}{r}\right) \tag{2.80}$$

Once this angle is known, the length of the resonant period will be the length of time it takes for the trajectory curve to travel from an angle of θ_1 to zero (2.81). When this curve reaches an angle of zero, the current in L_r is zero and the resonant period is complete. As long as t_2 is shorter than half of the switching period, T_s, the output diodes and the primary-side MOSFETs will achieve ZCS.

$$t_2 - t_1 = \frac{\theta_1}{\omega_r} \tag{2.81}$$

The conversion ratio, M, of the converter operating in Boost Mode is plotted versus ϕ for different output powers in Figure 2.25. From the figure, it is evident how the duty cycle is highly dependent on both the conversion ratio and the output power.

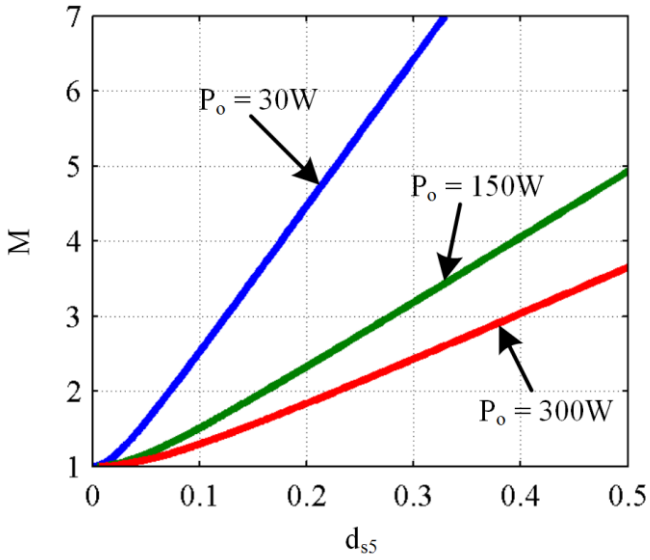


Figure 2.25. Conversion ratio of the converter operating in Boost Mode under different output power operating conditions.

2.5.3 Alternate Gating Method

It is possible to reduce the switching losses in the ac switch by controlling each of the gates separately when the device is comprised of two separate FETs or has two available gate pins. The device only needs to block voltage in one direction at a time, so it is possible to leave the other gate turned on when it does not need to block. Rather than turning both devices on for a short period of time as first introduced in the previous section, it is possible to control the on time of the ac switch by controlling the overlap time of the two halves of the device. This is demonstrated in Figure 2.26 where the gating scheme previously discussed is defined as Method 1 and the reduced-switching-loss scheme is defined as Method 2. The power stage functionality of the converter is identical between the two methods, but the effective switching frequency of the ac switch is reduced by half, greatly reducing the switching losses.

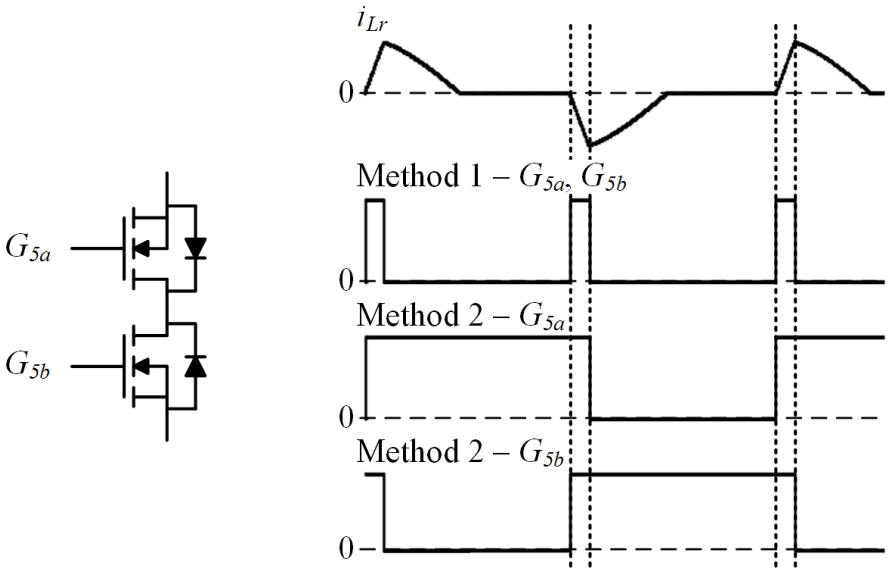


Figure 2.26. Comparison of ac switch gating schemes.

2.6 Summary

This chapter first examined state-of-the-art isolated dc-dc converter topologies and then proposed a new topology that overcomes a lot of the drawbacks of existing topologies. In order to maximize the efficiency of the converter for the nominal input voltage condition, the proposed converter is based around a series resonant converter operating at the series resonant frequency. While this maximizes efficiency, the series resonant converter operating at this point is unable to provide regulation. Two different hybrid operating modes are introduced to provide voltage regulation: a hybrid phase-shifted full-bridge buck and series resonant converter for Buck Mode, and a hybrid PWM boost and series resonant converter for Boost Mode. Both of these operating modes are thoroughly analyzed using state-plane trajectory curves. The key features of the proposed topology are:

1. Low circulating energy because the converter always operates at the series resonant frequency.
2. Guaranteed ZVS and ZCS of the primary side MOSFETs regardless of input voltage or output power in Boost Mode; guaranteed ZCS of one primary-side switching leg and ZVS of the leg regardless of input voltage or output power in Buck Mode.
3. Guaranteed ZCS of output diodes regardless of input voltage or output power.
4. Direct power transfer to the load for the majority of the switching cycle.
5. Voltage regulation through simple fixed-frequency PWM control.

Chapter 3

Power Stage Design Procedure, Loss Analysis, and Experimental Results

3.1 Design Procedure and Loss Equations

The foremost goal in the design procedure for the proposed converter is to maximize efficiency, so loss equations for the different components will be presented simultaneously with the design procedure. Understanding the source of losses for each component will allow for the selection of components that will yield the highest power conversion efficiency.

3.1.1 Transformer Turns Ratio

The most efficient operating point of the proposed converter will be when it is operating as a pure series resonant converter, so it is desired to design the converter to operate at this point for the nominal input voltage condition. Therefore, the converter design process will optimize the converter around the nominal input voltage case, or SR Mode. SR Mode occurs when the duty cycle of the ac switch is zero and the phase angle of the primary side devices is 180°; therefore, the transformer turns ratio needs to be selected so that this occurs when the input voltage is at its nominal. The formula for choosing the proper turns ration is shown in (3.1).

$$n = \frac{V_o}{2V_{in-nom}} \tag{3.1}$$

3.1.2 Resonant Tank

The first step in designing the resonant network is to choose the resonant inductance, L_r. During both Buck and Boost Modes of operation, a larger L_r directly correlates to lower rms currents in the converter's MOSFETs, diodes resonant capacitors, and isolation transformer. This is shown in Figure 3.1 where the rms resonant inductor current is plotted versus different inductance values for L_r. As a result, it is beneficial to make L_r as large as possible, but without violating several upper limit constraints. These constraints are that the converter must remain in DCM for all operating conditions in order to guarantee ZCS of the output diodes and primary side MOSFETs, the voltage ripple across the resonant capacitors cannot be too large, and practicality of physical transformer design unless an external resonant inductor will be used. The design procedure for

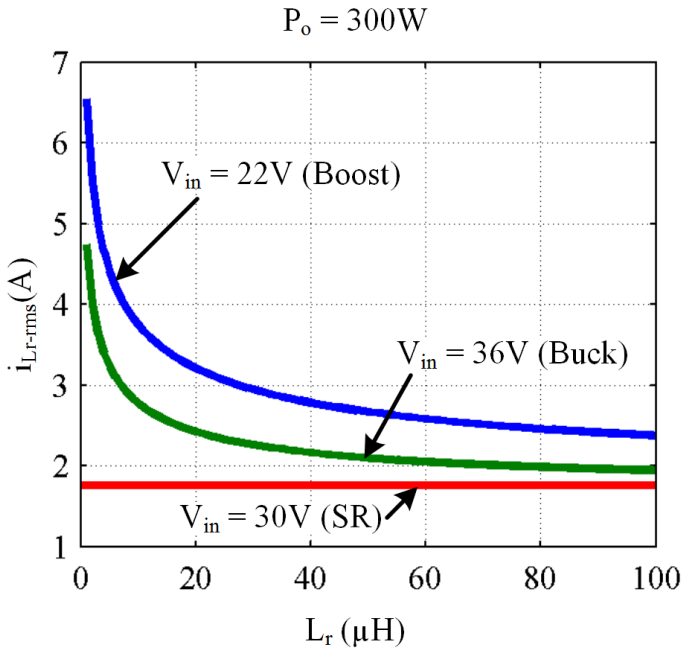


Figure 3.1. Resonant tank rms current versus resonant inductance for different input voltages.

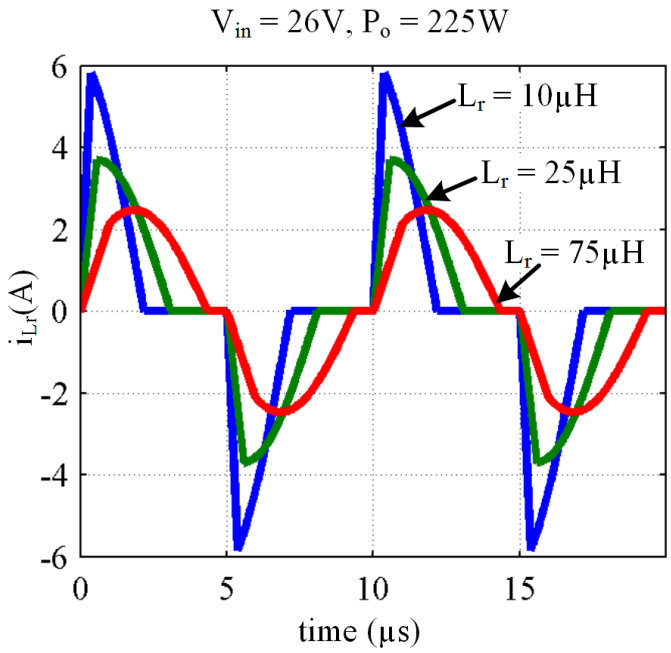


Figure 3.2. Resonant tank current for different resonant inductance values. All cases are operating at the same switching frequency, input voltage, and output power operating conditions.

selecting L_r varies substantially from that of the LLC converter, where L_r is chosen based on a ratio between the leakage and magnetizing inductances that will yield the proper conversion ratio within the desired switching frequency range. For the proposed topology, L_r is independent of the desired conversion ratio because it acts very similar to a PWM inductor operating at a fixed frequency.

During the DCM periods of both Buck and Boost Modes, no power is transferred from the source or to the load, so minimizing the length of this mode will result in higher power conversion efficiency. The larger L_r is designed to be, the shorter the DCM period will be, as is demonstrated in Figure 3.2. Here, three different resonant inductance values are compared during Boost Mode. For all three cases, the input voltage is 26 V, the output power is 225 W, and the switching frequency is 100 kHz. It can clearly be seen that the

larger the resonant inductance, the shorter the DCM period, and the lower the conveter rms currents.

In order to guarantee ZCS of the output diodes and primary-side MOSFETs, an upper limit needs to be set for L_r that will guarantee the converter will always operate in the DCM region. As long as the converter's switching frequency is equal to or below the resonant frequency, the converter will always operate in DCM during Buck Mode. During Boost Mode, however, if L_r is too large, the converter may enter the continuous conduction mode (CCM) and lose ZCS. The upper limit for L_r can be calculated using Boost Mode with the minimum input voltage and maximum output power condition. For this operating point, the combined lengths of operating Periods 1 and 2 needs to be shorter than half of the switching period, as calculated in (3.2) and (3.3).

$$\frac{T_s}{2} > t_2 - t_0, \qquad \frac{T_s}{2} > d_{s5}T_s + \frac{\theta_1}{\omega_r} \tag{3.2}$$

$$\frac{T_s}{2} > \frac{1}{nV_{in-\min}}\sqrt{P_{o-\max}T_sL_r\left(1-\frac{2nV_{in-\min}}{V_o}\right)} + \frac{1}{\omega_r}\cos^{-1}\left(\frac{\frac{V_o}{2}-\frac{P_{o-\max}T_sL_r\omega_r^2}{2V_o}-nV_{in-\min}}{\frac{V_o}{2}+\frac{P_{o-\max}T_sL_r\omega_r^2}{2V_o}-nV_{in-\min}}\right) \tag{3.3}$$

Another constraint placed on the maximum value of the resonant inductor is the acceptable voltage swing across the resonant capacitors. The larger the inductance of L_r, the smaller the capacitances of C_{r1} and C_{r2}, so the larger the ac voltage swing will be across them. In order for proper converter operation, the ac voltage swing on the resonant capacitors, Δv_{cr}, cannot be larger than the dc value, $V_o/2$. Additionally, the voltage seen across the resonant capacitors is the same voltage that is seen across the ac switch, so it

may be desireable to limit the ac voltage swing even further to be able to use a specific volage-rated ac switch and resonant capacitors to reduce cost and device parasitics. The maximum limit for the inductance of L_r is calculated in (3.4), where V_{max} is the maximum voltage seen across S_5 and the resonant capacitors. If there is no constraint placed on the voltage rating of these devices, V_{max} should be set equal to V_o to ensure the ac votlage ripple will not be greater than $V_o/2$.

$$L_r < \frac{V_o\left(2V_{\max} - V_o\right)}{P_o T_s \omega^2} \tag{3.4}$$

The final design constraint limiting the maximum value of L_r is the physical transformer design. While it is possible to add an external resonant inductor, it is desirable to integrate the resonant inductor into the isolation transformer to reduce component count and associated costs. In order to increase the leakage inductance of the isolation transformer so that it can be used as the resonant inductance, the transformer may have to be wound with a split bobbin to provide physical separation between the primary and secondary windings. Even with this winding method, the achievable inductance may be smaller than desired and this design section may need to be revisited after the actual transformer is constructed.

Once the value for the resonant inductance is decided upon, the resonant capacitance value can be chosen according to (3.5).

$$C_r = \frac{1}{2L_r\omega_r^2} \tag{3.5}$$

It is worth noting that when choosing the dielectric material for the resonant capacitors, it is important that one is chosen which has a very low temperature coefficient so that temperature's impact on the converter's series resonant frequency is minimized.

Additionally, all of the ac resonant current passes through these capacitors, so it is important to choose a material with a very low dissipation factor to minimize losses and loss-induced heating of the capacitors. Because of the low temperature coefficient and low dissipation factor requirements, it is desirable to use NP0/C0G ceramic capacitors or polypropylene film capacitors. The maximum rms currents that these capacitors need to handle occur during the maximum input voltage during Buck Mode and minimum input voltage during Boost Mode. These currents are expressed in (3.6) and (3.7), respectively.

$$i_{Cr-rms-buck} = \frac{1}{2Z_r}\sqrt{\frac{1}{2\omega_r T_s}\left(r_1^2\left(\frac{\phi\omega_r T_s}{180} - \sin\left(2\left(\frac{\phi\omega_r T_s}{360} - \pi\right)\right)\right) + r_2^2\left(2\theta_2 - \sin(2\theta_2)\right)\right)} \quad (3.6)$$

$$i_{Cr-rms-boost} = \frac{r}{2Z_r}\sqrt{\frac{1}{2\omega_r T_s}\left(2\theta_1 - \sin(2\theta_1)\right)} \quad (3.7)$$

3.1.3 Transformer Design and Dead Time Selection

Now that the transformer's turns ratio and target leakage inductance have been selected, the transformer itself can be designed. The first step in designing the transformer is to select the core size, shape, and material, which can be done using a number of different design procedures such as the ones outlined in [54-56]. All three of these design procedures use a core geometry factor to pick the optimal size for a core. When selecting the core material, it is important to note that the ambient temperature of the rooftop where these converters will be in operation will vary greatly depending on geographical location. Therefore, it is important to select a core material that has a relatively flat temperature curve such as Ferroxcube 3C95 [57] or Epcos N97 [58].

Once the core size, shape, and material is selected, the number of turns can be selected based on a trade-off between core losses and winding conduction losses. In order to calculate the core losses, the peak ac flux density, ΔB needs to be known which is shown in (3.8) for Buck Mode and (3.9) for SR and Boost Modes where the unit for ΔB is Tesla (T) and A_c is the cross-sectional area of the core in cm^2, which is available from the core shape datasheet.

$$\Delta B_{buck} = \frac{V_{in}\phi T_s}{720 n_1 A_c} \tag{3.8}$$

$$\Delta B_{boost} = \frac{V_{in} T_s}{4 n_1 A_c} \tag{3.9}$$

While the transformer is designed for the SR Mode of operation to optimize the converter efficiency at this point, it is important to calculate ΔB for all operating conditions to make sure the core will not saturate. In order to calculate the conduction losses, the rms currents of both windings need to be calculated. The primary winding current is expressed for Buck Mode in (3.10) and Boost Mode in (3.11). The secondary winding current for both modes is expressed in (3.12).

$$i_{pri-rms-buck} = \frac{n}{Z_r}\sqrt{\frac{1}{2\omega_r T_s}\left(r_1^2\left(\frac{\phi\omega_r T_s}{180} - \sin\left(2\left(\frac{\phi\omega_r T_s}{360} - \pi\right)\right)\right) + r_2^2\left(2\theta_2 - \sin(2\theta_2)\right)\right)} \tag{3.10}$$

$$i_{pri-rms-boost} = n\sqrt{\frac{2d_{s5}^3}{3}\left(\frac{nV_{in}}{F_s L_r}\right)^2 + \frac{1}{2\omega_r T_s}\left(2\theta_1 - \sin(2\theta_1)\right)\left(\frac{r}{Z_r}\right)^2} \tag{3.11}$$

$$i_{\sec-rms} = \frac{i_{pri-rms}}{n} \tag{3.12}$$

Using the aforementioned design procedures, ΔB and $i_{pri\text{-}rms}$ can be used to calculate the core loss, P_{core} (3.13), and copper loss, P_{cu} (3.14).

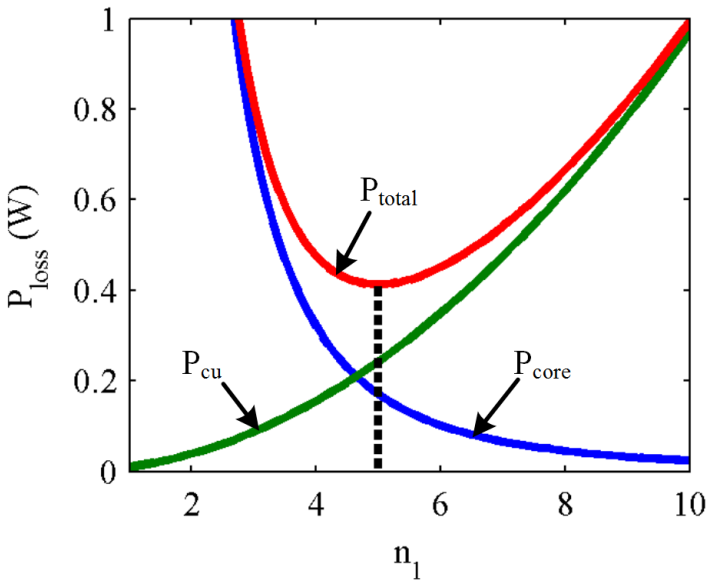


Figure 3.3. Power loss curve of isolation transformer used for selecting turns ratio.

$$P_{core} = aF_s^b \Delta B^c \frac{m}{1000} \tag{3.13}$$

$$P_{cond} = i_{pri-rms}^2 R_{pri} + i_{\sec-rms}^2 R_{\sec} \tag{3.14}$$

Equation (3.13) is based on the Steinmetz equation [59] where *a*, *b*, *c*, and *e* are coefficients which can be obtained by curve-fitting techniques of the power-loss curves from the core material datasheet. *m* is the mass of the core in grams. In (3.14), R_{pri} and R_{sec} are the dc resistance of the primary and secondary windings. Using these two loss figures, the optimal number of primary turns, n_1, can be determined as shown in Figure 3.3 where P_{total} is the combination of P_{cu} and P_{core} losses.

As mentioned in Chapter 2, the magnetizing inductance of the transformer and the length of the dead time period can be chosen to ensure ZVS of the primary side switches under all input voltage and output power operating conditions during SR Mode and Boost

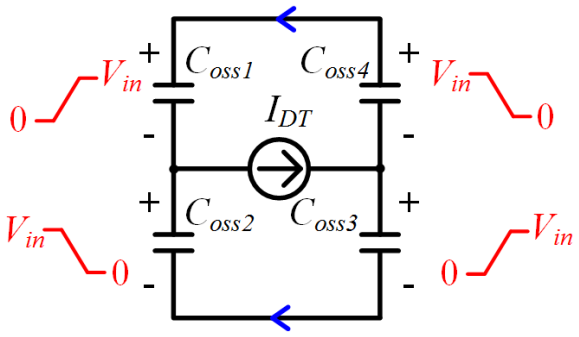


Figure 3.4. Equivalent circuit of primary-side MOSFETs and magnetizing current during the first dead time period during SR and Boost Modes.

Mode. The magnetizing current in the transformer reflected to the primary side is expressed in (3.15).

$$I_{DT} = \frac{n^2 V_{in} T_s}{4 L_m} \tag{3.15}$$

This current acts as a current source and is used to charge and discharge the parasitic output capacitances of the primary side MOSFETs. An equivalent circuit during the first dead time period of both SR and Boost Modes is shown in Figure 3.4.

In order to determine the required magnetizing inductance and dead time, a relationship between these values and the parasitic output capacitance of the primary-side switches can be determined from the basic capacitor charge balance equation (3.16).

$$I = C \frac{dV}{dt} \tag{3.16}$$

Here I is defined in equation (3.15), C is the equivalent capacitance of the four MOSFET output capacitances, dv is the amount of change in voltage across the equivalent output capacitance, and dt is the length of the dead time period, T_{DT}. The two switch capacitances in each leg charge and discharge in series, and each leg charges and discharges in parallel, so the equivalent capacitance is equal to one of the MOSFETs, C_{oss}. The change in voltage will be equal to $2V_{in}$ since the voltage across the current source will swing from

$+V_{in}$ to $-V_{in}$. Plugging in these values into the capacitor charge balance equation, (3.17) is obtained.

$$L_m \leq \frac{n^2 T_{DT}}{8 F_s C_{oss}} \tag{3.17}$$

It can be seen in (3.17) that a tradeoff needs to be made between the magnetizing inductance and dead time. The value of the magnetizing inductance affects the circulating magnetizing currents that affect light load efficiency, and the length of the dead time affects how much of the switching period is able to be used for power transfer; larger dead times result in shorter device conduction periods and higher rms currents. Once this tradeoff is determined, the magnetizing inductance can be set by adjusting the air gap of the transformer according to the previously discussed conventional design procedures.

As long as the magnetizing inductance and dead time are selected such that the inequality in equation (3.17) holds true, the primary side switches will achieve ZVS. Because the output diodes achieve ZCS, there is no load current present in the primary side devices during the dead time. Therefore, the magnetizing current will allow the primary side devices to achieve ZVS for the entire load range, including no load. Also of note here is that (3.17) is not dependent on V_{in}, so the primary side devices are able to achieve ZVS for the entire input voltage range as well. Once again, this design step for selecting the magnetizing inductance is very different from the LLC converter design procedure. Here, the magnetizing inductance only needs to be small enough to discharge the primary side MOSFETs rather than being chosen based on a ratio between the magnetizing and leakage inductances. This design procedure generally results in a larger L_m/L_r ratio than the conventional LLC design procedure which translates to a larger L_m and small air gap for

given L_r. This results in reduced circulating currents and higher light load efficiency than the LLC converter is capable of.

This design procedure for selecting L_m will guarantee ZVS of the primary-side MOSFETs for all input voltage and output power operating conditions for both SR and Boost Mode, but will not guarantee ZVS for switches S_1 and S_2 during Buck Mode. This design procedure for the converter focuses on optimizing the converter efficiency at the nominal input voltage, or series resonant operating point. While it is possible to tune L_m to guarantee ZVS for all of the switches in Buck Mode as well, this would result in a smaller magnetizing inductance, larger magnetizing current, and lower light-load power stage efficiency during the optimal SR Mode of operation.

3.1.4 Input Capacitance

The input capacitance is to be chosen based on the desired switching ripple present at the input of the converter. This switching ripple will impact the operating point of the PV module, so it is desirable to minimize this ripple to ensure maximum power extraction from the PV module. As a result, a tradeoff is to be made here between the input voltage ripple and the physical size as well as cost of the input capacitor.

In order to determine the input capacitance requirement, C_{in}, first the input voltage ripple, Δv_{in}, needs to be calculated. Because of the hybrid resonant and PWM characteristics of the proposed converter, this is non-trivial. The charge-balance equation of a capacitor states that the charge into the capacitor and out of the capacitor in steady state must be equal. Therefore if we analyze the charge that is supplied by the capacitor, Q, Δv_{in} can be determined based on the capacitor-charge relationship $Q = C_{in}\Delta v_{in}$. The

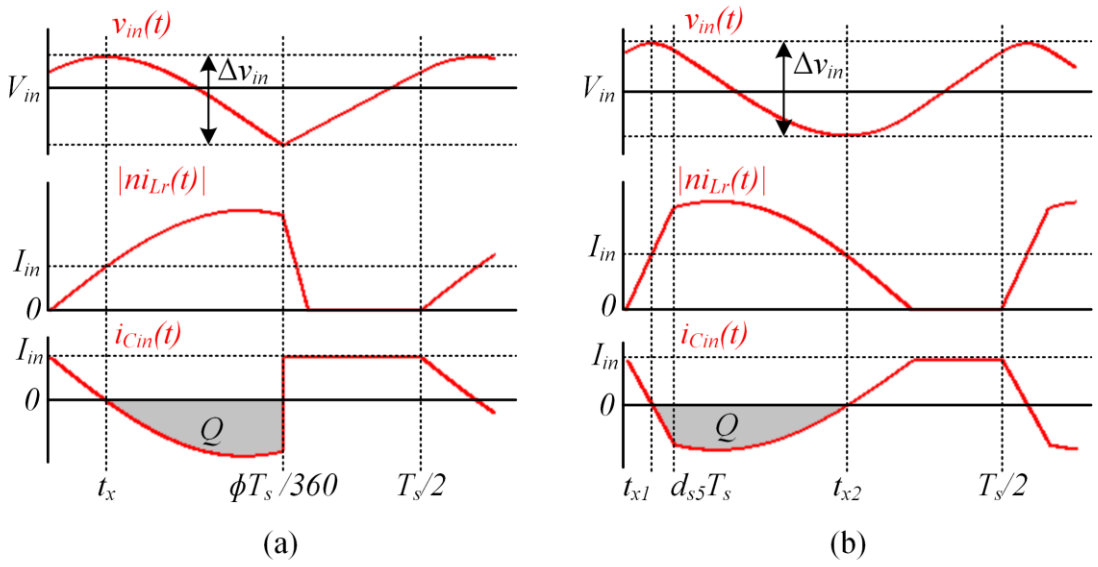


Figure 3.5. Steady-state waveforms of the input voltage ripple and input capacitor current during (a) Buck Mode and (b) Boost Mode.

amount of charge supplied by C_{in} can be determined by integrating the current supplied by C_{in}. The current through C_{in} is expressed in (3.18) and is plotted in Figure 3.5 (a) for Buck Mode and is expressed in (3.19) and is plotted in Figure 3.5 (b) for Boost Mode.

$$i_{Cin-buck}(t)=\begin{cases}\dfrac{P_o}{V_{in}}-|ni_{Lr}(t)| & for \quad 0<t<\dfrac{\phi T_s}{360}, \quad \dfrac{T_s}{2}<t<\dfrac{T_s}{2}+\dfrac{\phi T_s}{360} \\ \dfrac{P_o}{V_{in}} & for \quad \dfrac{\phi T_s}{360}<t<\dfrac{T_s}{2}, \quad \dfrac{T_s}{2}+\dfrac{\phi T_s}{360}<t<T_s\end{cases} \tag{3.18}$$

$$i_{Cin-boost}(t)=\frac{P_o}{V_{in}}-|ni_{Lr}(t)| \tag{3.19}$$

The shaded areas in the figure represent the total charge supplied by C_{in}. Q can be determined by integrating these shaded areas and the results are given in (3.20) for Buck Mode and (3.21) for Boost Mode.

$$Q_{buck} = \frac{P_o}{V_{in}}\left(\frac{\phi T_s}{360} - \frac{\sin^{-1}\left(\frac{P_o Z_r}{nV_{in}r_1}\right)}{\omega}\right) + 2nC_r r_1\left(\cos\left(\omega\frac{\phi T_s}{360}\right) - \sqrt{1-\left(\frac{P_o Z_r}{nV_{in}r_1}\right)^2}\right) \quad (3.20)$$

$$Q_{boost} = \frac{n^2 V_{in}}{2L_r}\left(dT_s - \frac{P_o L_r}{(nV_{in})^2}\right)^2 + \frac{P_o}{V_{in}}(t_{x2} - dT_s) + 2nC_r r\left(\cos\theta_1 - \sqrt{1-\left(\frac{P_o Z_r}{nV_{in}r}\right)^2}\right) \quad (3.21)$$

Where

$$t_{x2} = \frac{1}{\omega}\left(\theta_1 + \omega dT_s - \sin^{-1}\left(\frac{P_o Z_r}{nV_{in}r}\right)\right) \quad (3.22)$$

The required input capacitance can now be determined from the capacitor-charge relation:

$$C_{in} = \frac{Q}{\Delta v_{in}} \quad (3.23)$$

3.1.5 Semiconductor Device Selection

Next, all of the semiconductor devices will be selected based on their maximum blocking voltages and a tradeoff between conduction and switching losses. Because of the full-bridge configuration on the primary side, all of the primary-side MOSFETs have a voltage stress equal to the input voltage, so the maximum voltage these devices need to block is equal to the maximum converter input voltage (3.24).

$$V_{ds1234-\max} = V_{in-\max} \quad (3.24)$$

Once the voltage rating for the primary-side MOSFETs is known, devices can be selected though a trade-off of conduction losses and switching losses. The conduction loss equation for each MOSFET is shown in (3.25) where $i_{s1234\text{-}rms}$ is the rms switch current shown in (3.26). R_{dson} is the MOSFET's drain-source on-resistance when fully conducting.

$$P_{cond1234} = i_{s1234-rms}^2 R_{dson} \tag{3.25}$$

$$i_{s1234-rms} = \frac{i_{pri-rms}}{\sqrt{2}} \tag{3.26}$$

During SR and Boost Modes, the primary side MOSFETs achieve ZVS and ZCS, so their only switching losses are the gate turn-on losses and are expressed in (3.27) where Q_g is the gate charge of the MOSFET, V_{aux} is the auxiliary power supply voltage that powers the gate drivers, and F_s is the switching frequency of the converter.

$$P_{sw1234-boost} = \frac{F_s}{2} Q_g V_{aux} \tag{3.27}$$

During Buck Mode, switches S_1 and S_2 lose ZVS and S_3 and S_4 lose ZCS. The switching losses for these two switching legs are shown in equations (3.28) and (3.29). Here, t_f is the turn-off time of the MOSFET and i_{to}, shown in equation (3.30), is the current present in the MOSFET when it begins to turn off. Since the converter is to be optimized for the nominal input voltage condition, the primary side devices should be selected based primarily on a trade-off between equations (3.25) and (3.27).

$$P_{sw12-buck} = \frac{F_s}{2}\left(C_{oss} V_{in}^2 + Q_g V_{aux}\right) \tag{3.28}$$

$$P_{sw34-buck} = \frac{F_s}{2}\left(V_{in} i_{to} t_f + Q_g V_{aux}\right) \tag{3.29}$$

$$i_{to} = \frac{n r_1}{Z_r} \sin(\theta_1) \tag{3.30}$$

The ac switch, S_5, has the same maximum voltage stress as the resonant capacitors, shown in (3.31). This switch needs to be able to block this voltage in both the positive and negative directions. This device also can be selected based on a trade-off between conduction and switching losses. The conduction losses are shown in (3.32) and the rms current stress is shown in (3.33). The switching losses are shown in (3.34) where $V_{aux\text{-}sec}$ is the secondary-side auxiliary power supply voltage that feeds the ac switch gate driver.

$$V_{ds5-\max} = \pm\left(\frac{V_o}{2} + \Delta v_{cr}\right) \tag{3.31}$$

$$P_{cond5} = i_{s5-rms}^2 R_{dson} \tag{3.32}$$

$$i_{s5-rms} = \frac{n V_{in} d_{s5} T_s}{L_r}\sqrt{\frac{2d_{s5}}{3}} \tag{3.33}$$

$$P_{sw5} = \frac{F_s}{2}\left((nV_{in})^2 C_{oss} + \left(\frac{V_o}{2} - \Delta v_{cr}\right)\frac{n V_{in} d_{s5} T_s}{L_r} t_f + Q_g V_{aux-\sec}\right) \tag{3.34}$$

The output diodes, D_{o1} and D_{o2}, each need to block the entire output voltage, given by equation (3.35), and need to be able to handle the full average load current, which is calculated in equation (3.36). Since these diodes achieve ZCS for all operating modes, the main losses are conduction losses which can be approximated with a diode model consisting of a forward voltage drop, V_f, and series resistance, R_{ac} [60]. These losses are expressed in (3.37). The rms currents during Buck and Boost Modes are expressed in (3.38) and (3.39). It is important to note here, that since these diodes achieve ZCS, there is practically no reverse-recovery loss and it is not necessary to use ultra-fast reverse-recovery diodes

$$V_{d-\max} = V_o \tag{3.35}$$

$$i_{d-ave} = \frac{P_{o-\max}}{V_o} \tag{3.36}$$

$$P_{d-cond} = V_f i_{d-ave} + i_{d-rms}^2 R_{ac} \tag{3.37}$$

$$i_{d-rms-buck} = \frac{1}{2Z_r}\sqrt{\frac{1}{\omega_r T_s}\left(r_1^2\left(\frac{\phi\omega_r T_s}{180} - \sin\left(2\left(\frac{\phi\omega_r T_s}{360} - \pi\right)\right)\right) + r_2^2\left(2\theta_2 - \sin\left(2\theta_2\right)\right)\right)} \tag{3.38}$$

$$i_{d-rms-boost} = \frac{r}{2Z_r}\sqrt{\frac{1}{\omega T_s}\left(2\theta_1 - \sin\left(2\theta_1\right)\right)} \tag{3.39}$$

3.1.6 Auxiliary Power Considerations

As will be discussed in Chapter 5, the microconverter needs to be able to start up when there is no dc bus present (V_o = 0 V), so it is desirable to power the auxiliaries from the PV module input rather from the dc bus output. Additionally, the converter will control the input voltage and measure the input current to perform MPPT which also makes it desirable to have control and sensing on the primary side to avoid the complexities and additional costs associated with isolated sensing.

With the addition of a secondary-side ac switch, the number of required auxiliary power supplies is increased and isolation is now required. A source-connected ac switch adds the requirement for one additional isolated auxiliary power supply and a drain-connected ac switch adds the requirement for two. The gate drivers for each half of the ac switch consume around 10-50 mW including both quiescent power consumption and MOSFET turn-on losses supplied by the gate driver. Commercially available power supply modules are typically rated at 250 mW or 1 W and have unregulated outputs [61, 62]. If the power supply module has an unregulated output, it may be necessary to provide a low-

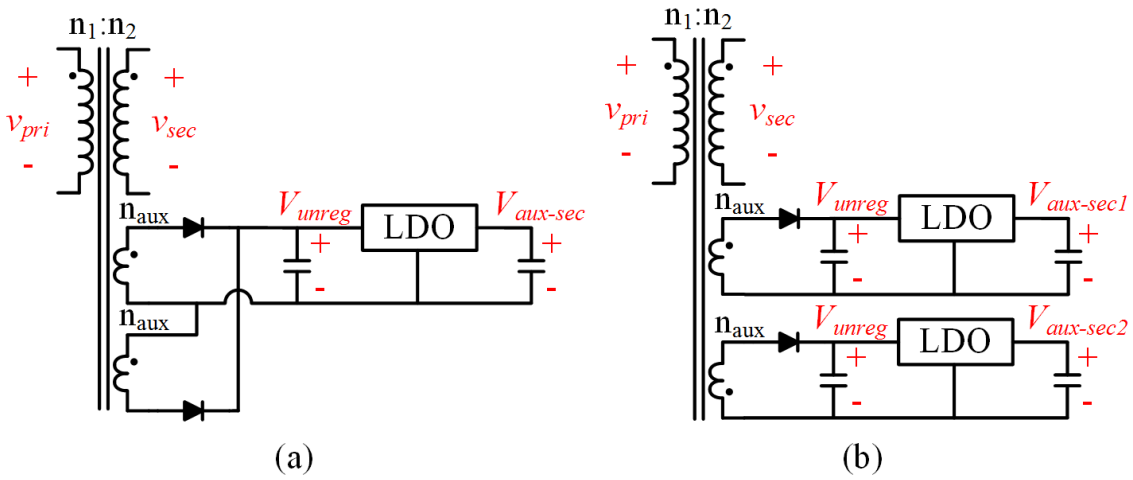


Figure 3.6. Isolation transformer winding configuration for supplying auxiliary power to the S_5 gate drivers when S_5 is implemented with (a) common source and (b) common drain.

dropout regulator (LDO) in series with the output to avoid damaging the gate driver or the actual switch itself. The LDO would be necessary because these unregulated power supplies generally only guarantee a specified output range from 10%-100% rated power. For power levels less than 10%, which is where the secondary auxiliaries would be operating, the output voltage of the supplies can be much higher than rated. With a 25 mW output, commercially available 250 mW power supplies operate in the 20-30% [62] efficiency range and 1-W power supplies operate in the 10-20% [61] efficiency range. Not only are these supplies very inefficient, but they also are costly.

It is possible to avoid the use of commercially available isolated power supply modules by powering the secondary-side auxiliaries using auxiliary windings on the isolation transformer. This is possible because the converter begins operating in Buck Mode during startup, as will be discussed in Section 5.2. As a result, the secondary-side auxiliary power supplies for driving the ac switch gate drivers are not needed until after the converter's primary-side devices have already begun switching. Figure 3.6 shows

transformer winding configurations for powering (a) a single secondary-side auxiliary supply for a source-connected ac switch and (b) two secondary-side auxiliary supplies for a drain-connected ac switch. In the figure, n_1, n_2, and n_{aux} are the number of turns of the primary, secondary, and auxiliary windings, respectively. V_{unreg} the rectified voltage across the auxiliary winding of the transformer and is proportional to V_{in}. V_{aux_sec} is the secondary-side auxiliary supply that will power the ac switch gate drivers and is regulated by an LDO. For the case shown in (a), a full-wave current doubler rectifier [63] is used to rectify the voltage across the auxiliary winding. This is used rather than a single winding and four-diode rectifier to reduce the number of diodes needed. This is also used rather than a single-diode half-wave rectifier in order to keep the magnetic flux balanced in the transformer. For the case shown in (b), two half-wave rectifiers are used – once for each auxiliary supply. It is important to note the dot convention here. If the two windings are wound in the opposite direction of each other, the magnetic flux in the transformer core related to the auxiliary power will be balanced.

When selecting the number of turns for the auxiliary windings, it is important to make sure V_{unreg} will be greater than the comibnatino of $V_{aux\text{-}sec}$ and the dropout voltage of the LDO, V_{do}, during the minimum input voltage case. The formula for determining n_{aux} is given in (3.40).

$$V_{in-\min}\frac{n_{aux}}{n_1} > V_{aux-\sec} + V_{do} \tag{3.40}$$

The dominant factor in determining the efficiency of these auxiliary supplies is going to be the efficiency of the LDO. Both the core losses and conduction losses introduced by these extra windings are very low, so the efficiency of the supplies can be estimated in (3.41).

$$\eta_{aux-\text{sec}} \approx \frac{V_{aux-\text{sec}}}{V_{unreg}} \tag{3.41}$$

While this is not the most efficient solution, it is very simple and low cost. It is also possible to use a non-isolated dc-dc switching regulator integrated circuit (IC) in place of the LDO to increase the auxiliary supply efficiencies at the penalty of additional cost and more complex circuitry.

3.2 Loss Model

In addition to the loss equations presented in the previous section, additional auxiliary losses such as sensing, control, and gate driver quiescent current losses need to be taken into consideration in order to complete the loss model. The sensing losses are made up of current sense resistors, resistive voltage divider networks, signal conditioning circuits, and isolation circuitry necessary for output voltage sensing. The control losses consist of all of the digital controller IC and/or analog ICs and associated biasing circuits that are used to implement MPPT, voltage control, and the ICs to generate PWM gating signals. This also includes any isolation circuitry necessary for passing the PWM gating signals to the secondary-side ac switch gate driver. Finally, the gate driver quiescent current losses can be determined from the gate driver's datasheet. This represents how much power is consumed when the gate driver is operating at the switching frequency, but not driving the gate of a MOSFET.

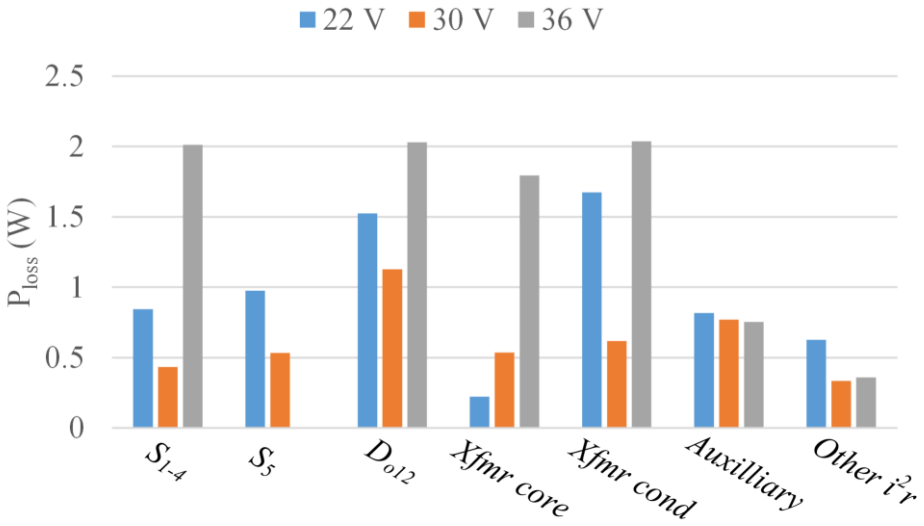


Figure 3.7. Breakdown of converter losses for different input voltages with a 225-W output.

Using the developed loss model, a breakdown of the converter's losses for an example design are shown in Figure 3.7. Here the minimum, nominal, and maximum input voltages are compared at the 75% output power condition. It can be seen here that the overall losses are smallest at the nominal input voltage. The further away from the series resonant point the converter operates, the higher the rms currents are due to the DCM period, so the higher the conduction losses are throughout the converter.

3.3 Experimental Results

3.3.1 Prototype Design Summary

A 300 W prototype was developed to experimentally verify the proposed microconverter and analysis. The specifications for the converter are given in Table 3.1. The input voltage range of the converter was designed to handle 15-55 V, with a maximum power point range of 22-36 V and a nominal input of 30 V. The maximum power point

Table 3.1. Specifications of hardware prototype

Specification	Value
Input Voltage Range	15-55 V
Nominal Input Voltage	30 V
MPP Range	22-36 V
Nominal Output Voltage	380 V
Output Power	30-300 W

Table 3.2. Power stage parameters and switching devices of hardware prototype.

Parameter/Device	Value
Switching frequency, F_s	100 kHz
Resonant capacitance, C_r	44 nF
Resonant inductance, L_r	31.9 µH
Output capacitance, C_o	1.2 µF
$S_1 - S_4$	Infineon BSC016N06NS
S_5	2x Infineon BSC16DN25NS3
D_{o1}, D_{o2}	NXP BYV29B-500

Table 3.3. Isolation transformer design parameters.

Parameter	Value
Core Shape	RM14/ILP
Core Material	Ferroxcube 3C95
Turns ratio, n	6.2
Primary winding, n_1	5 turns, 16 AWG (650/44 Litz)
Primary resistance, R_{pri}	4.7 mΩ
Secondary winding, n_2	31 turns, 22 AWG (160/44 Litz)
Secondary resistance, R_{sec}	135 mΩ
Leakage inductance, L_{lk}	31.9 µH
Magnetizing inductance, L_m	876 µH
Converter deadtime, T_{DT}	50 ns

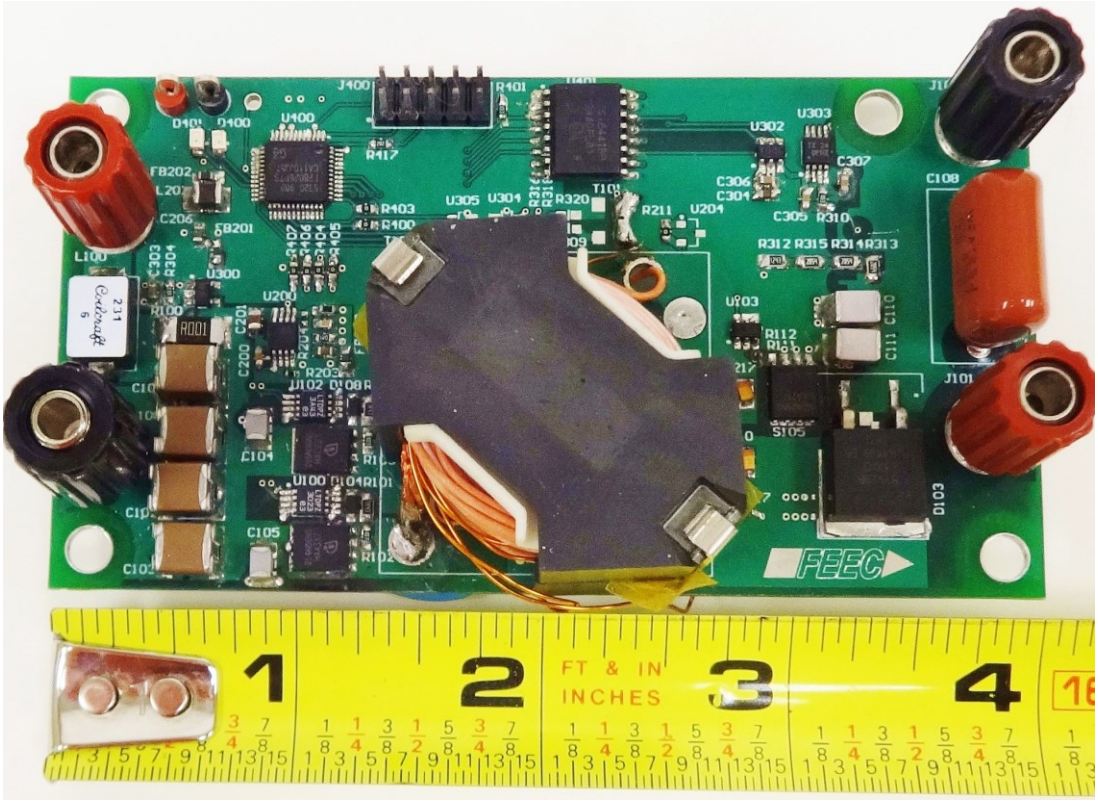


Figure 3.8. Photograph of developed 300-W prototype.

ange is the range of input voltages where the converter is designed to operate with full output power. The nominal input voltage of 30 V was designed to accommodate standard 60-cell PV modules. With the selected turns ratio of 6.2, SR Mode occurs with an input voltage of 30.65 V. When the converter input voltage is above 30.65 V, the converter operates in Buck Mode and the primary-side full bridge is phase-shift modulated; when the input voltage is below 30.65 V, the converter operates in Boost Mode and the bidirectional ac switch is pulse-width modulated. The nominal output voltage of the converter was designed to be 380 V which is enough to power 120-V ac, 208-V ac, or 240-V ac inverters which are all commonly found in the US.

A summary of the power stage parameters and switching devices for the hardware prototype are given in Table 3.2 and a summary of the isolation transformer design is given

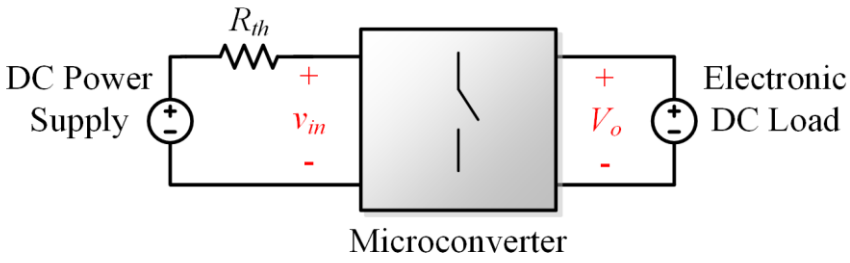


Figure 3.9. Experimental test setup.

in Table 3.3. The leakage inductance of the transformer, L_{lk}, is also utilized as the converters resonant inductance, L_r, so there is no external resonant inductor. A photograph of the developed prototype is shown in Figure 3.8. The board's dimensions are 4.05" x 2.2" x 1.1" resulting in a total volume of 9.8 cubic inches and a power density of 1.87 kW/L. The total weight of the prototype is 114 grams. Control was implemented with Texas Instrument's TMS320F28026 Piccolo Digital Signal Processor (DSP).

The experimental setup used for the remainder of this section is shown in Figure 3.9. The input of the microconverter is connected to a variable voltage dc power supply and an input series resistor. This power supply and resistor combination acts as the Thevenin equivalent of a PV module and allows for the input voltage of the converter to be changed by the control variable of the converter. The output of the microconverter is connected to a BK Precision 8502 Programmable DC Electronic Load operating in constant voltage mode. This electronic load fixes the output voltage to 380 V.

3.3.2 Converter Operation

Steady-state operating waveforms of the converter operating in SR Mode with a 300-W output are shown in Figure 3.10. In the figure, the voltage across the primary winding of the transformer v_{pri}, the resonant capacitance voltage v_{cr1}, and the resonant

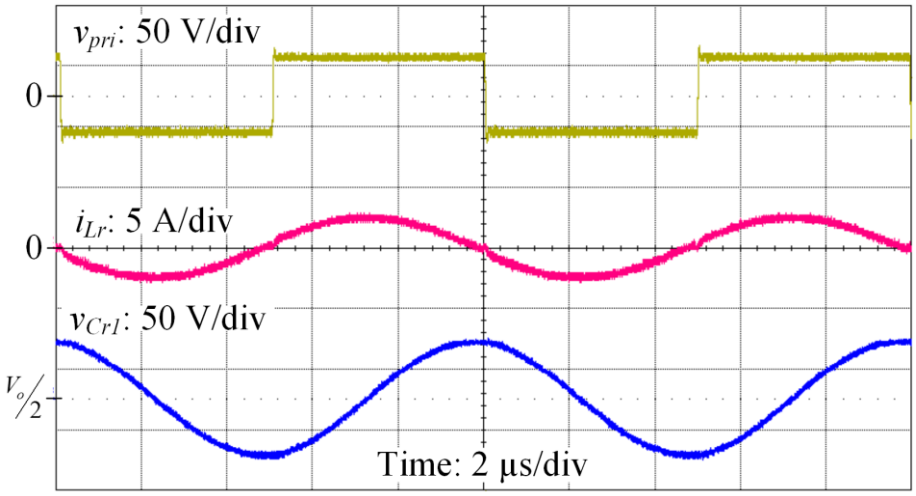


Figure 3.10. Steady-state operating waveforms of the converter operating in pure SR mode with a 31.5-V input and 300-W output.

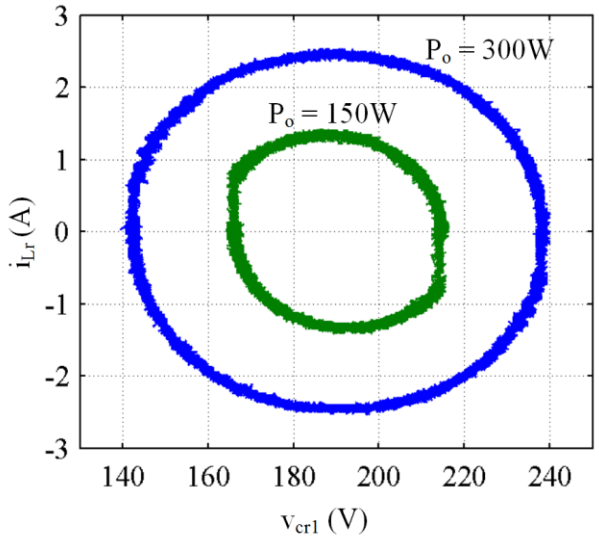


Figure 3.11. Steady-state state-plane trajectory curves of the resonant tank's voltage and current in SR Mode with 150-W and 300-W outputs.

current i_{Lr} are shown. It can be seen from v_{pri} that the phase angle between the two switching legs is 180°. The switching frequency is equal to the resonant frequency, so i_{Lr} and v_{cr1} are almost pure sinusoidal waveforms. With a 300-W output, the input voltage is 31.5 V. While the turns ratio was designed in (3.1) such that a 30.65-V input would result in pure SR operation, this formula does not take into account resistive losses throughout the converter. As a result, the input voltage during SR Mode increases as the output power

increases. Experimental state-plane trajectory plots are shown in Figure 3.11 for 150-W and 300-W output power conditions. Once again, because the switching frequency is equal to the resonant frequency, the waveforms are almost pure sinusoidal so the trajectory plots are circular.

Steady-state operating waveforms of the converter operating in Buck Mode with a 34-V input and 300-W output are shown in Figure 3.12. The effect of the control variable, Φ, can be observed in the figure from v_{pri}. It can be seen that resonance begins at the start of the switching period and then is ended early when v_{pri} is shorted. Switching noise can also be observed on the v_{pri} waveform due to the loss of ZVS during S_1 and S_2 transitions and the loss of ZCS during S_3 and S_4 transitions. Experimental state-plane trajectory plots of the resonant tank state variables for different output power conditions are shown in Figure 3.13. A comparison of the calculated and measured conversion ratios for different output power conditions are shown in Figure 3.14. When Φ is equal to 180°, the conversion ratio isn't equal to 1 as predicted due to the resistive loss elements previously mentioned. As the output power increases, the conversion ratio at 180°, or pure SR Mode, decreases.

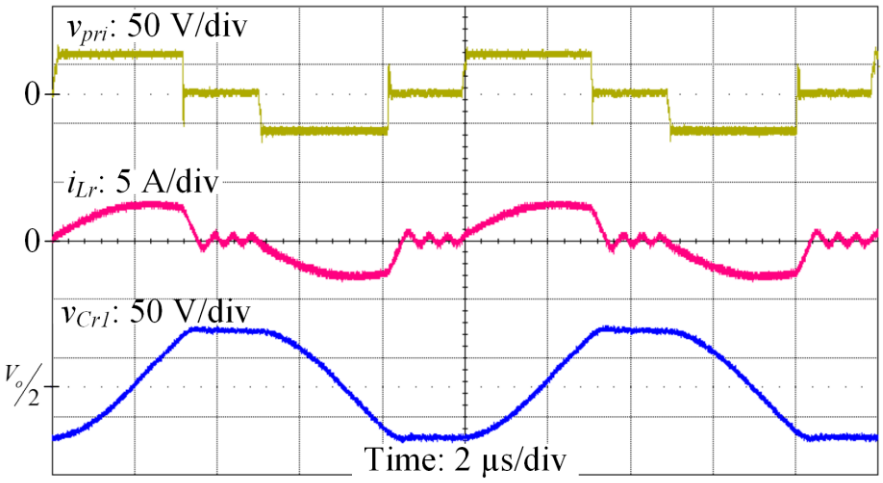


Figure 3.12. Steady-state operating waveforms of the converter operating in Buck Mode with a 34-V input and 300-W output.

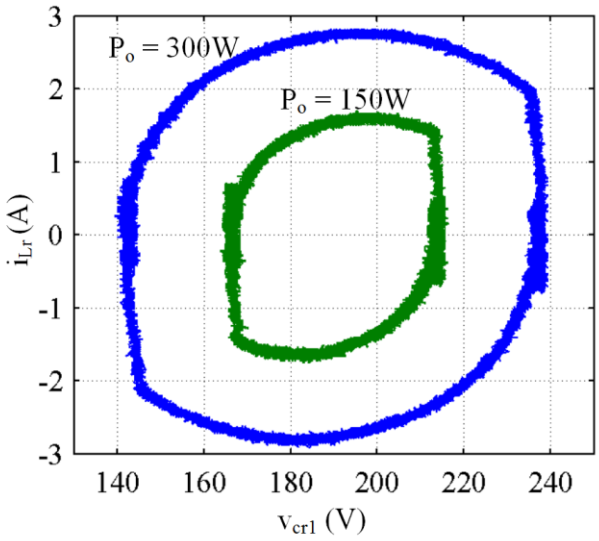


Figure 3.13. Steady-state state-plane trajectory curves of the resonant tank's voltage and current in Buck Mode with a 33-V input and both 150-W and 300-W outputs.

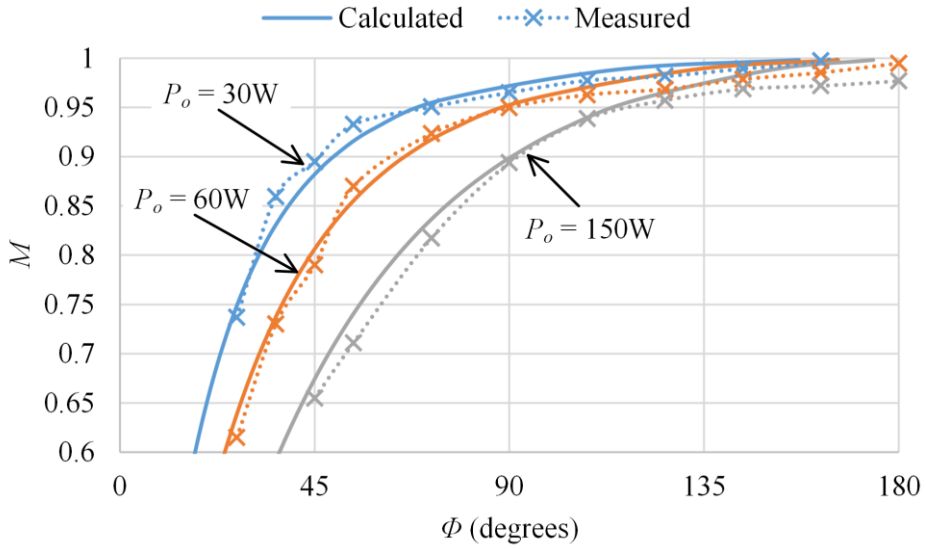


Figure 3.14. Comparison of calculated and measured conversion ratios for the proposed converter with different output power conditions in Buck Mode.

Steady-state operating waveforms of the converter operating in Boost Mode with a 26-V input and 300-W output are shown in Figure 3.15. This time the voltage across the secondary winding of the transformer, v_{sec}, is shown in order to demonstrate the functionality of the ac switch. While this voltage is zero, the ac switch is on, and the current

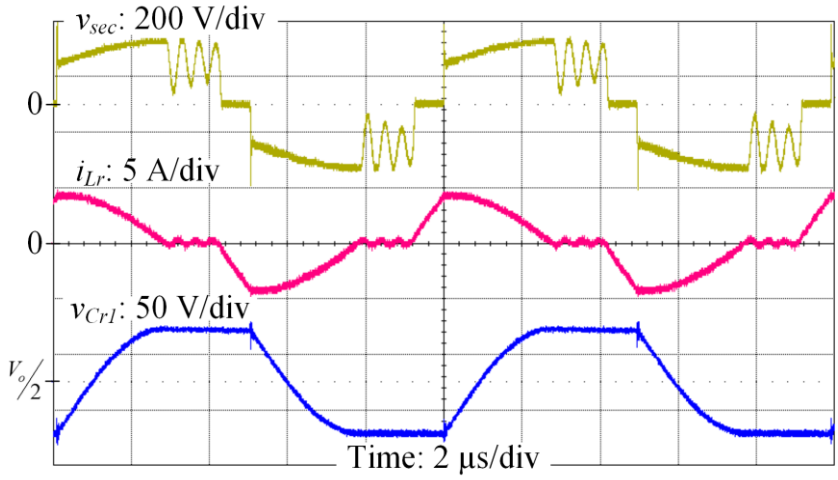


Figure 3.15. Steady-state operating waveforms of the converter operating in Boost Mode with a 26-V input and 300-W output.

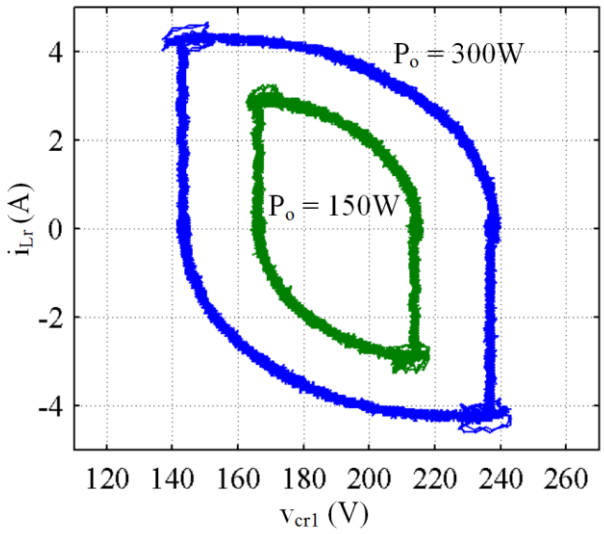


Figure 3.16. Steady-state state-plane trajectory curves of the resonant tank's voltage and current in Boost Mode with a 26-V input and both 150-W and 300-W outputs.

in the resonant inductor increases linearly. When the ac switch turns off, resonance begins from the initial condition set by S_5. Steady-state state-plane trajectory curves of the resonant tank in Boost Mode are shown in Figure 3.16 with an input voltage of 26 V and different output power conditions. Switching noise from the hard turn-off of the ac switch can be observed in the v_{cr1} waveform in Figure 3.15 and in the trajectory curves in Figure

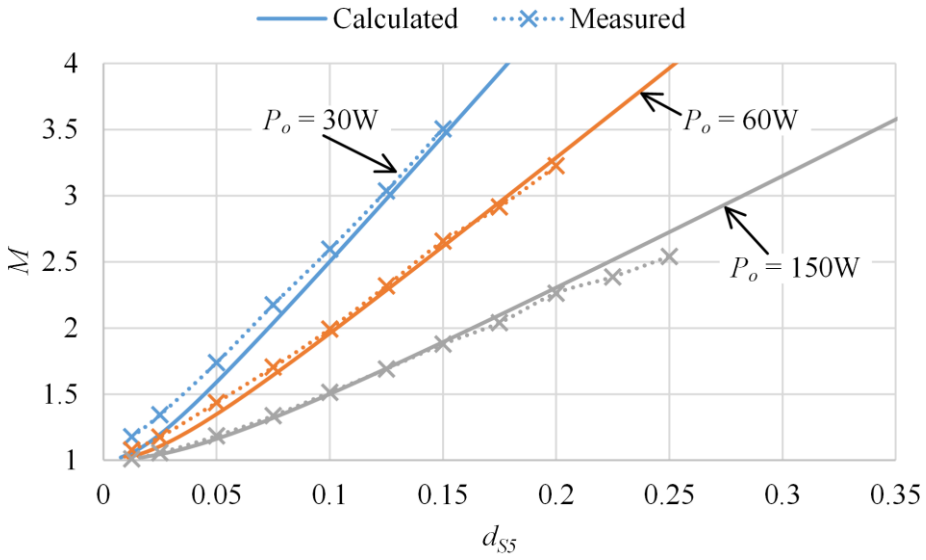


Figure 3.17. Comparison of calculated and measured conversion ratios for the proposed converter with different output power conditions in Boost Mode.

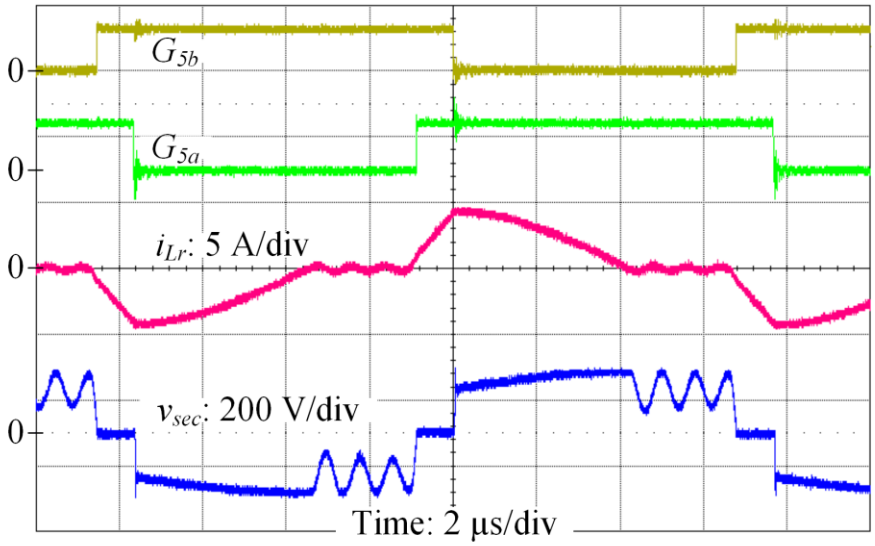


Figure 3.18. AC switch gating signals G_{5a} and G_{5b}, resonant inductor current i_{Lr}, and voltage across the secondary winding of the transformer v_{sec} while the converter is operating with a 25-V input and 225-W output.

3.16 at the start of the resonant period. A comparison of the calculated and measured conversion ratios are shown in Figure 3.17.

AC switch gating waveforms G_{5a} and G_{5b}, the resonant inductor current i_{Lr}, and the voltage across the secondary winding of the isolation transformer v_{sec}, are shown in Figure

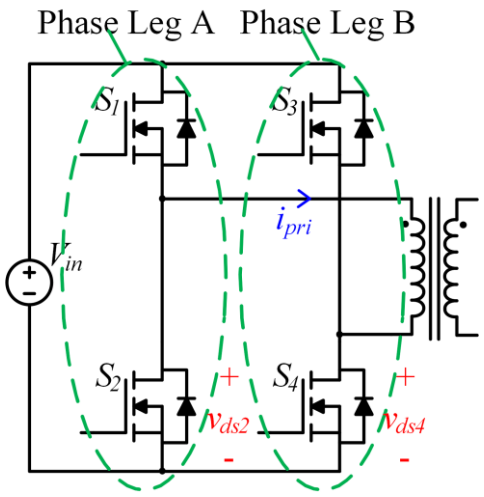


Figure 3.19. Schematic of the primary-side full-bridge MOSFET network showing the definition of the switching legs along with the key voltages and currents used for determining ZVS and ZCS.

3.18 when the converter is operating in the Boost Mode with a 25-V input and 225-W output. Here, the gating scheme used to drive the two gates of the ac switch can clearly be seen. When the gating signals overlap, the ac switch conducts, the voltage across the secondary winding of the transformer is zero, and the inductor current increases linearly.

Now that the basic converter operation has been verified, ZVS and ZCS of the primary-side MOSFETs will be explored. Figure 3.19 defines the two different switching legs that make up the full-bridge network: Phase Leg A is comprised of S_1 and S_2, and Phase Leg B is comprised of S_3 and S_4. The voltages at the switching nodes, v_{ds2} and v_{ds4}, will be used to determine ZVS and the primary winding current, i_{pri}, will be used to determine the current in the devices when they turn off. The current i_{pri} is equal to $n(i_{Lm} + i_{Lr})$.

Steady-state waveforms of v_{ds2}, v_{ds4}, and i_{pri} during Buck Mode are shown in Figure 3.20 where the converter is operating with a 34-V input and 300-W output. It is evident from the figure than during the Leg B transition there is current present in S_3 and S_4 so ZCS

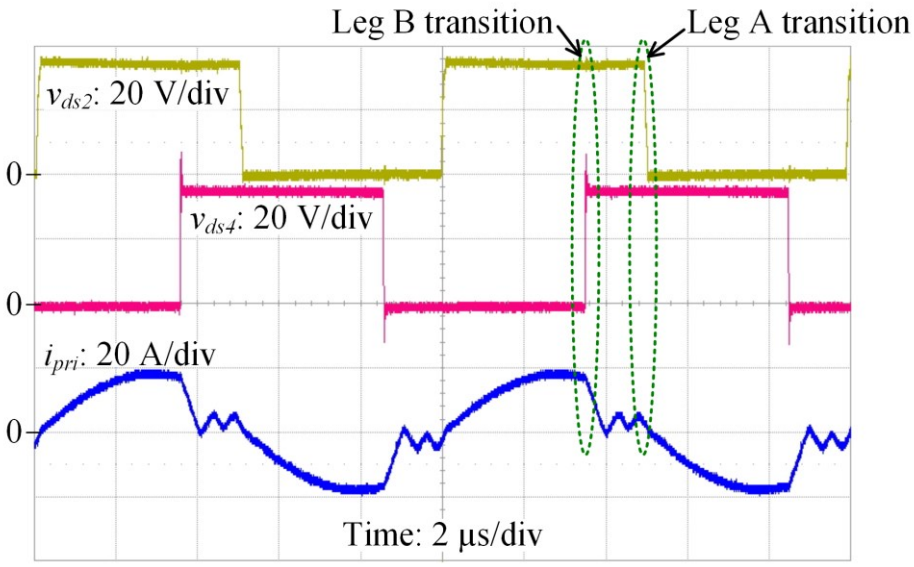


Figure 3.20. ZCS waveforms during Buck Mode of the primary-side switches.

is not achieved. After the Leg B transition, the load current quickly falls to zero and the current present in the primary side devices is just the magnetizing current which is small compared to the load current. During the Leg A transition, this magnetizing current is all that is present in S_1 and S_2 so they essentially achieve ZCS.

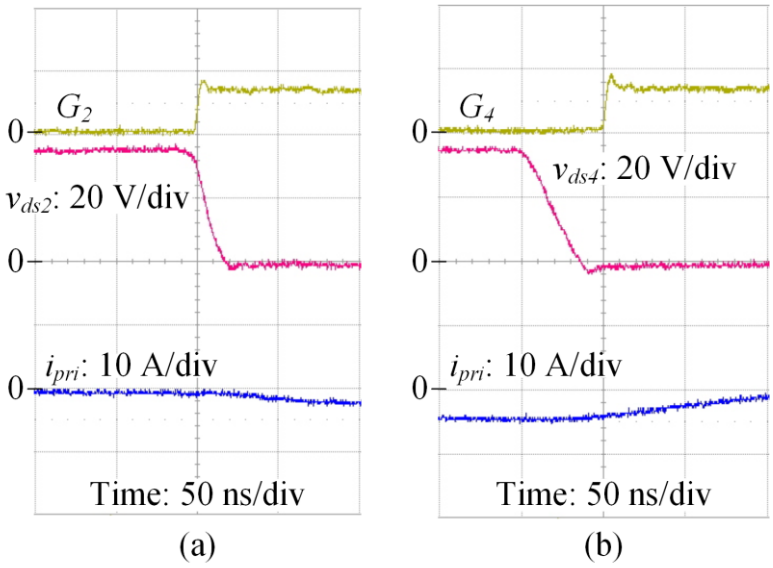


Figure 3.21. Buck Mode switching waveforms of the primary side devices in (a) Phase Leg A and (b) Phase Leg B.

In order to demonstrate ZVS during Buck Mode, waveforms of both transitions are shown in Figure 3.21. In this figure, the input voltage is 34 V and the output power is only 10 W. Such a low power level is chosen to demonstrate how Leg B will always achieve ZVS, even with a very low load current. This is shown in the figure in (b) where v_{ds4} reaches zero before the gating signal, G_4, turns S_4 on. Figure 3.21 (a) shows the switching waveform of S_2 in Leg A. This device does not achieve ZVS because the magnetizing current is very small.

Switching waveforms of the converter operating in Boost Mode are shown in Figure 3.22 where the converter is operating with a 22-V input and 300-W output. This is the minimum input voltage and maximum input current case for the converter. Since the phase angle between the two switching legs is 180° during Boost Mode, the switching transitions of both phase legs occur at the same time. It is evident from the figure that the only current present in the devices when the transition is the magnetizing current, so they all achieve ZCS.

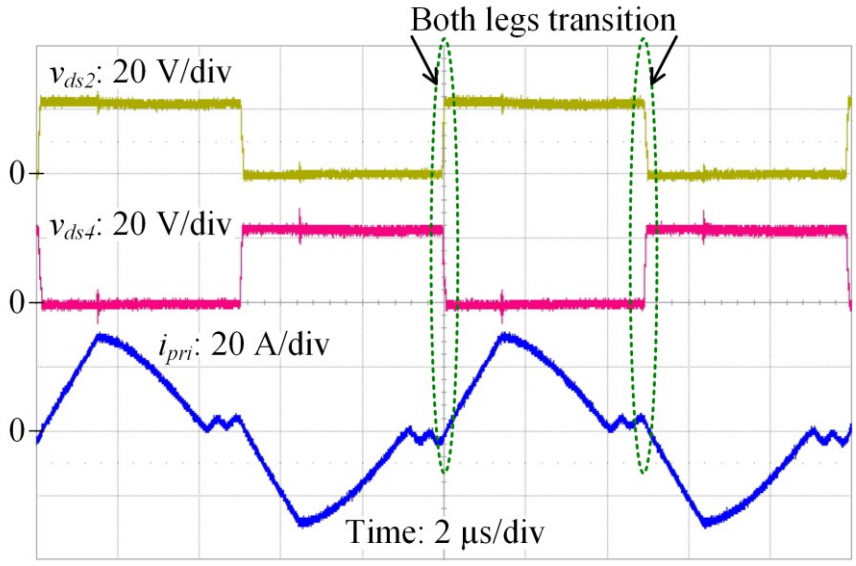


Figure 3.22. ZCS waveforms during Boost Mode of the primary-side switches.

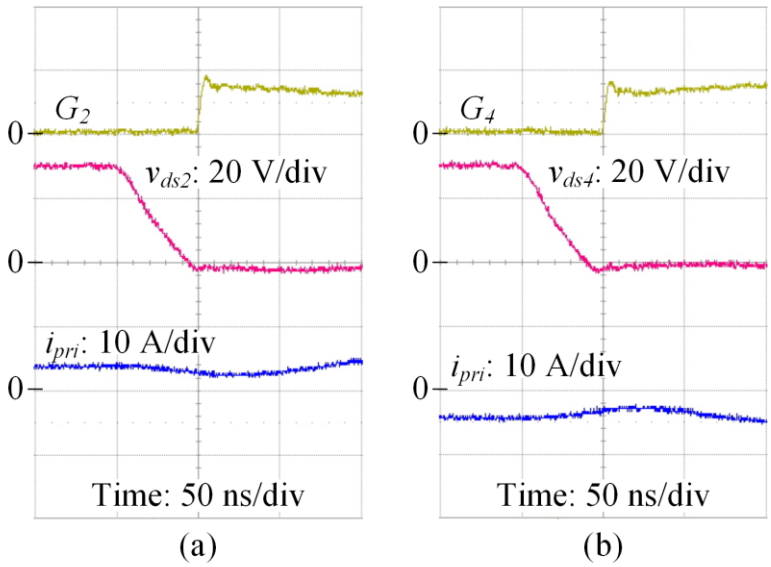


Figure 3.23. Boost Mode switching waveforms of the primary side devices in (a) Phase Leg A and (b) Phase Leg B.

In order to demonstrate ZVS in Boost Mode, zoomed-in waveforms of the switching transitions are shown in Figure 3.23. Here, the output power is 0 W to demonstrate how the converter's ability to achieve ZVS is independent of output power. The no load condition was implemented by disconnecting the secondary side of the transformer so that there is truly zero load current. In the figure, both v_{ds2} and v_{ds4} reach zero volts before the switches turn on, allowing all of the primary side devices to achieve ZVS regardless of output power.

3.3.3 Converter Efficiency

The efficiency of the proposed converter is now tested for different input voltages and output power levels. The projected converter efficiency based on the loss model presented in Section 3.2 is shown in Figure 3.24 for the minimum, nominal, and maximum input voltages. The experimental efficiency curves for the same conditions are shown in Figure 3.25. The expected efficiencies from the loss model match the measured

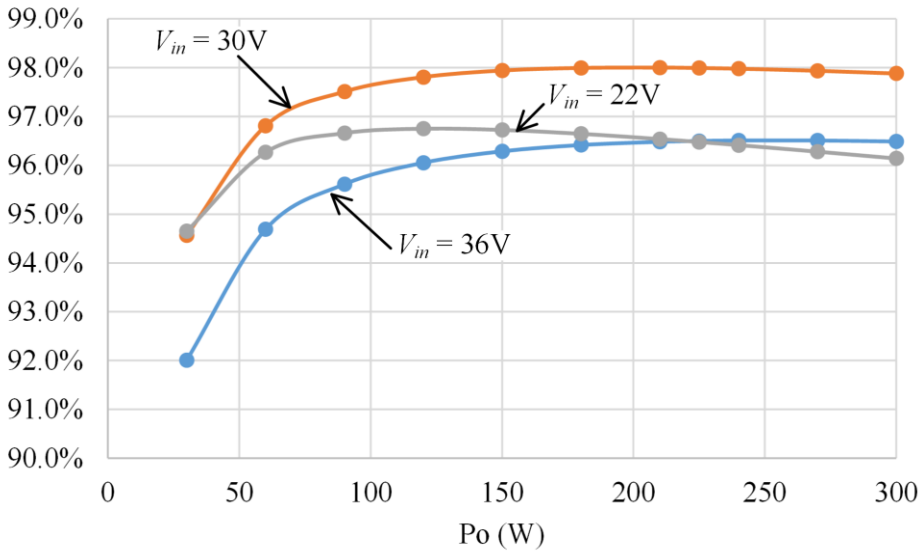


Figure 3.24. Projected converter efficiency based on loss model.

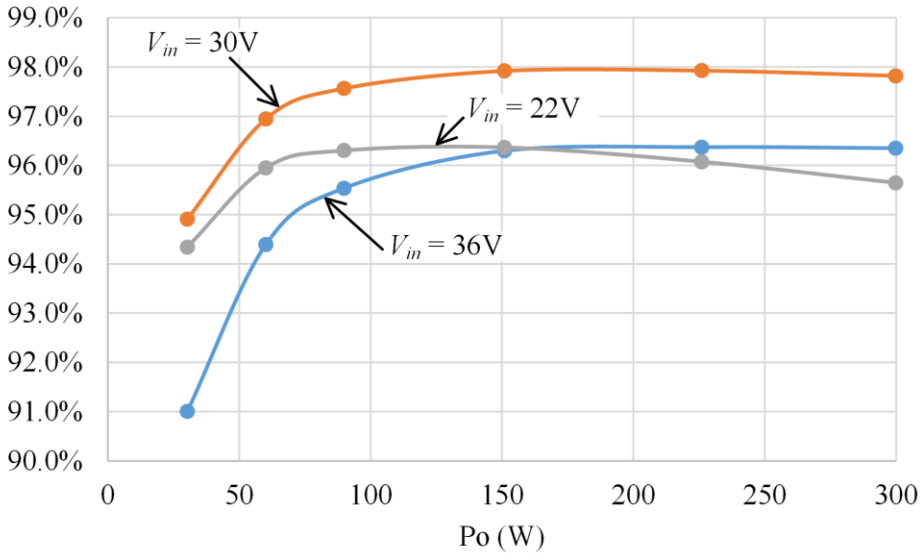


Figure 3.25. Measured converter efficiency.

efficiencies very closely validating the loss model. Weighted CEC efficiencies for different input voltages are shown in Figure 3.26. The converter's peak efficiency is 97.9% and the CEC efficiency at the nominal 30 V input is 97.7%. These loss measurements consist of all system losses including control, sensing, and other auxiliary losses. Measurements were made using Fluke 287 digital multimeters with have a dc voltage

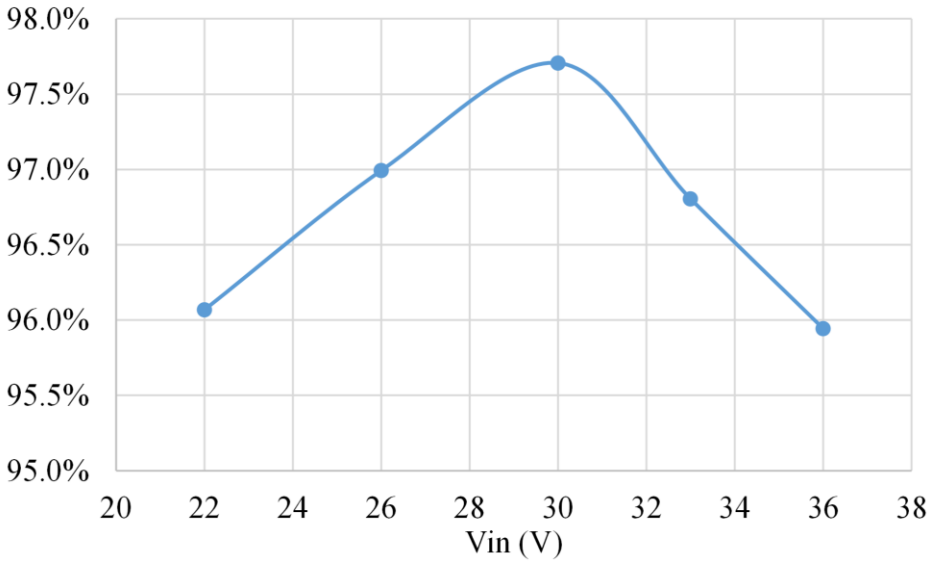


Figure 3.26. Weighted CEC efficiency versus input voltage.

accuracy of 0.025% for the input voltage, 0.03% for the output voltage, and a dc current accuracy of 0.3% for both the input and output currents.

3.4 Summary

A systematic design procedure, loss analysis, and experimental results for the proposed microconverter were presented in detail in this chapter. The design procedure and loss equations were provided simultaneously to ensure components are chosen to maximize converter efficiency. The design procedure for this converter varies greatly form that of the LLC and other resonant converters. For the proposed converter, L_m is not used for voltage regulation, so the resulting L_m/L_r ratio is much larger. This translates to lower circulating currents and higher light-load efficiencies.

Experimental results using a 300-W microconverter prototype were presented to validate the converter analysis presented in Chapter 2 as well as the loss model presented

in this chapter. The steady-state analysis presented in Chapter 2 was validated both in the time domain and with state-plane trajectory curves. The converter is verified to achieve ZCS of the output diodes for all operating conditions, ZCS and ZVS of the primary-side MOSFETs in Boost Mode, and ZVS of one leg with ZCS of the other leg in Buck Mode. The converter's peak efficiency, including all auxiliary, sensing, and control losses, was 97.9% while the weighted CEC efficiency was 97.7% with the nominal input voltage.

Chapter 4

Modeling and Control

4.1 Control System Overview

A high-level block diagram of the proposed microconverter and control system is pictured in Figure 4.1. The dc bus output voltage is regulated by a down-stream converter or inverter stage, so the primary objective of the microconverter's control system is to control the input voltage, or PV module output voltage, in order to track the maximum power point of the module. It is possible to perform MPPT using open-loop control methods where the duty cycle of the converter is directly perturbed and the input or output power is monitored [64-66]. But with these methods it's hard to model and predict the system's behavior over wide operating conditions. Therefore, this converter will perform

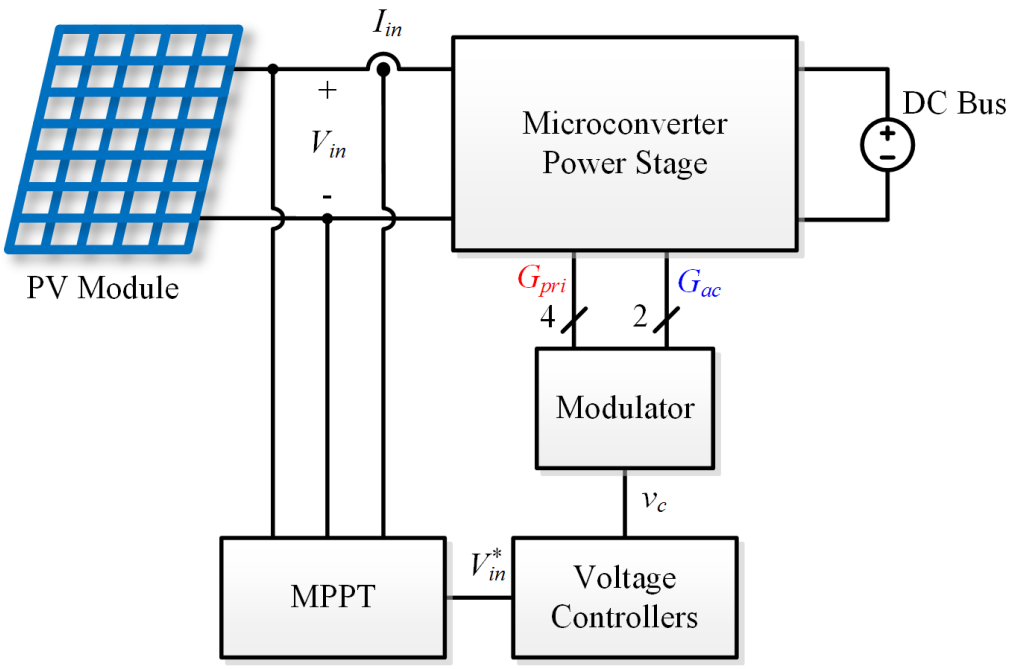


Figure 4.1. Block diagram of proposed microconverter and control system.

MPPT by controlling the input voltage. An MPPT algorithm, which will be discussed in Chapter 5, reads the input voltage and current V_{in} and I_{in} in Figure 4.1, and outputs an input voltage reference V_{in}^*. The input voltage reference is passed to a set of voltage controllers which in turn provides a control signal, v_c, to the modulator. The modulator is responsible for translating v_c into the six gating signals for the active power switches. This chapter will first discuss modeling and controller design for each operating mode, followed by modulation and transition techniques to ensure a smooth transition between the different operating modes. Since the converter cannot regulate when operating in the pure series resonant mode, this chapter will focus on modeling and control of Buck and Boost Modes. Pure SR Mode naturally occurs at the transition point between the two other operating modes.

4.2 Buck Mode

4.2.1 Model Derivation

The proposed converter exhibits characteristics of both DCM PWM converters and resonant converters which makes modeling in the time-domain complicated. There are three state-variables in the system: v_{cin}, i_{Lr}, and v_{cr}. v_{cin} changes slowly over time with respect to the switching frequency so conventional state-space averaging techniques are able to be used for this state variable [67, 68]. v_{cr} on the other hand, is purely a resonant state variable and changes very rapidly with respect to the switching frequency. This variable always has a constant average value so conventional state-space averaging won't work. i_{Lr} combines the characteristics of both v_{cin} and v_{cr}. There are several modeling methods in literature for converting fast-changing resonant state variables into slow-

moving variables so that state-space averaging can be applied [69-71], but this does not work for the proposed converter because one of the resonant state variables, i_{Lr}, also has the slow-moving average characteristics of a PWM state variable. In order to greatly simplify the modeling of the converter, it is possible to neglect C_r and model it as a PWM converter. Neglecting C_r will remove the resonant state variable, v_{cr}, and remove the resonant characteristics of the hybrid state variable, i_{Lr}. C_r is small in value, so the dynamics introduced into the converter from C_r are in a higher frequency range than the desired control bandwidth.

This simplification will provide a model that is accurate enough to design controller bandwidths in the 1-10 kHz range which is around 1000 times faster than typical MPPT bandwidths [72]. Figure 4.2 demonstrates this process where C_r is eliminated, the isolation transformer is removed, and the primary-side components are reflected to the secondary side. Here V_{th} and R_{th} are the Thevenin equivalent voltage source and series resistance of

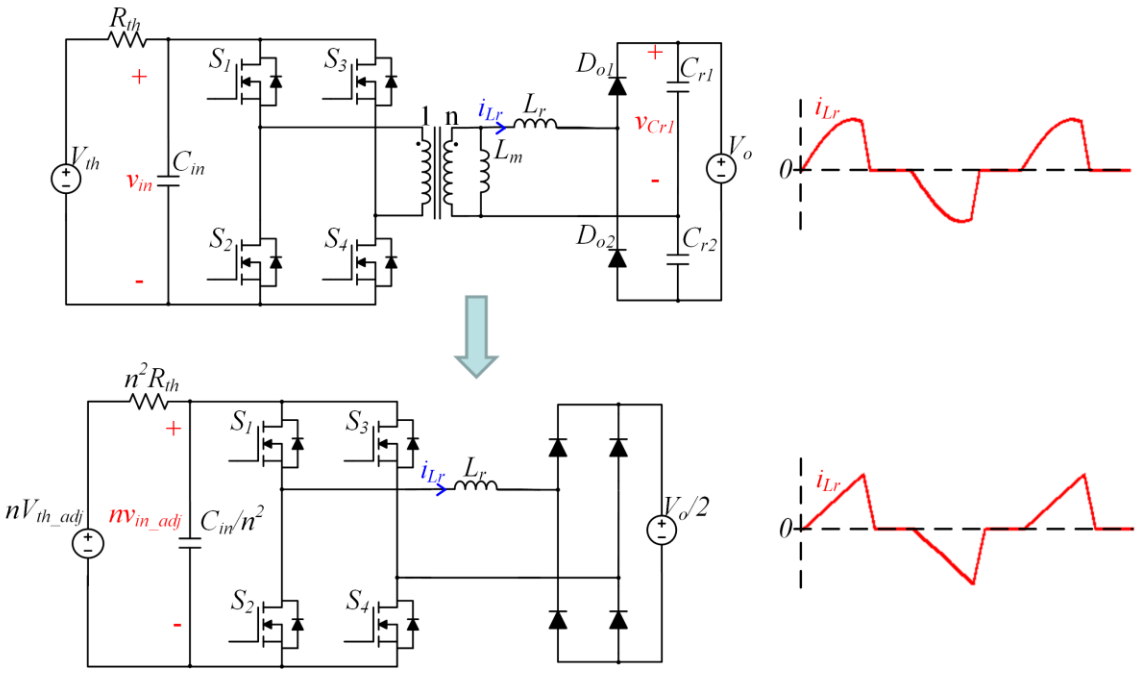


Figure 4.2. Simplification of the Buck Mode circuit model.

a PV module operating at a specific operating point on the I-V curve, respectively. The inductor current is also shown in the figure both before and after the simplification. Here it can be seen how the resonance is removed and the current now looks like that of a standard PWM converter operating in the DCM.

The model can be further simplified by rectifying the inductor current and replacing the two full-bridge switch networks with single-switch networks. The full-bridge diode network reduces to a single diode and the primary-side full-bridge switch network simplifies to a single switch, S_{eq}, which is shown in Figure 4.3. S_{eq} operates at a switching frequency of $2F_s$ (4.1) and with a duty cycle, d_{eq}, proportional to Φ given in (4.2).

$$F_{s\_eq} = 2F_s \qquad T_{s\_eq} = \frac{T_s}{2} \tag{4.1}$$

$$d_{eq} = \frac{\phi}{180°} \tag{4.2}$$

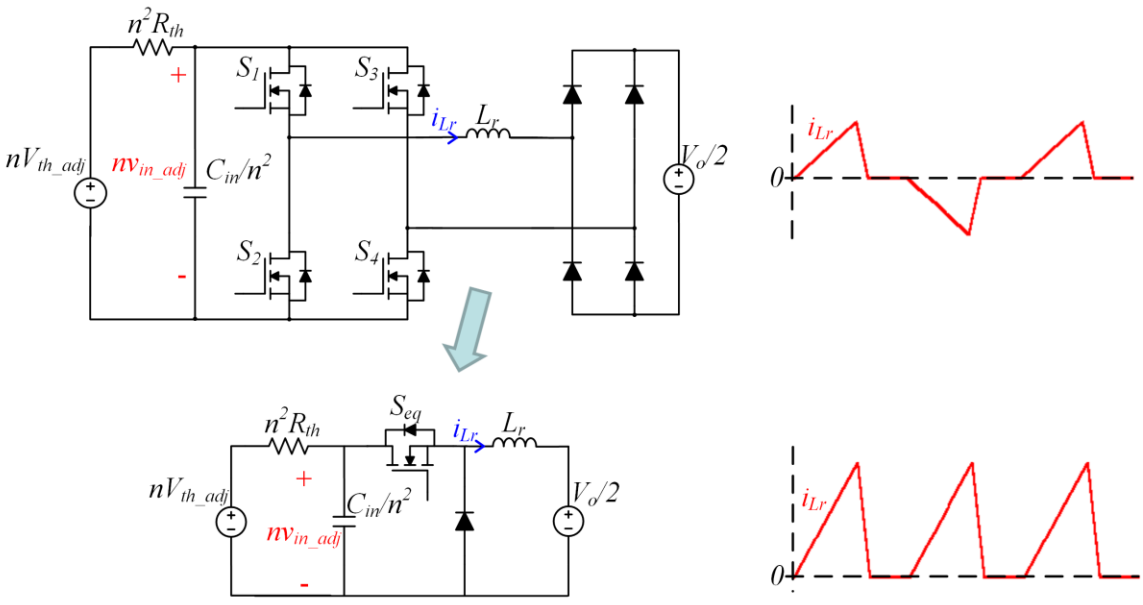


Figure 4.3. Additional simplification of the Buck Mode circuit model.

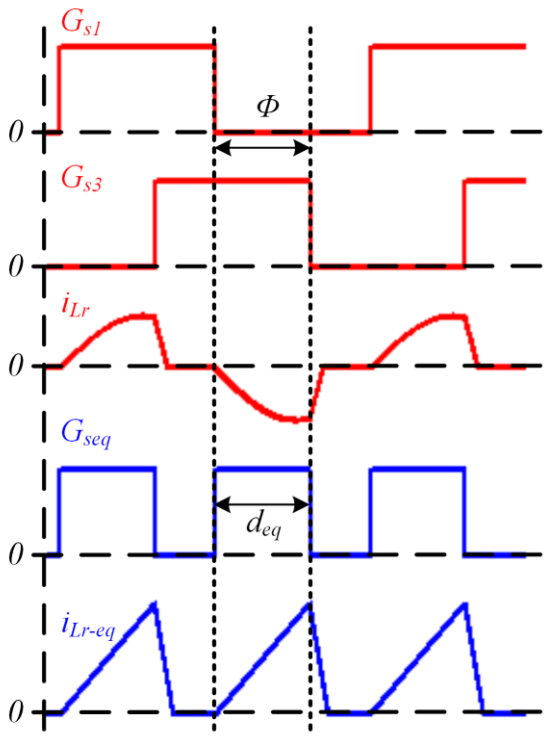


Figure 4.4. Gating signals and inductor current waveforms of the two Buck Mode circuit models.

The operation of S_{eq} is made evident from Figure 4.4 where the gating waveforms and inductor currents are compared between the full model and simplified model. The simplified model is now just a simple single-switch DCM PWM buck converter which can be modeled using conventional modeling techniques.

While this simplified circuit model gives a close approximation of the full circuit's dynamics, the conversion ratio of the two circuits are not the same which is demonstrated in Figure 4.5. Since these conversion ratios are not equal, an additional adjustment needs to be made to the simplified model in order to more closely represent the actual circuit. The different conversion ratios mean that for a given duty cycle, d_{eq}, the simplified circuit will result in a different input voltage than the full model. The resulting input voltage in the simplified model, V_{in_adj}, needs to be used to more accurately model the dynamics. This is calculated in (4.3).

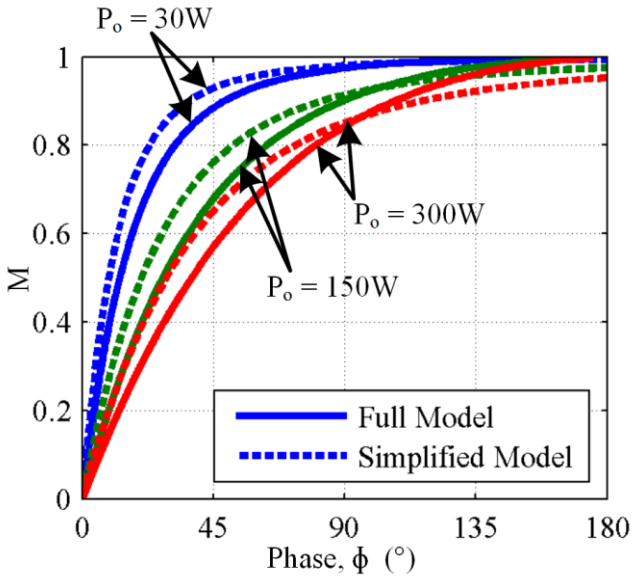


Figure 4.5. Comparison of the conversion ratio of the two Buck Mode circuit models.

$$V_{in\_adj} = \frac{1}{n}\left(\frac{V_o}{4} + \sqrt{\left(\frac{V_o}{4}\right)^2 + \frac{2P_oL_r}{d_{eq}^2 T_{seq}}}\right) \tag{4.3}$$

Additionally, since the input voltage of the simplified model is different than the full model, the output power of the simplified model will also be different in the same Thevenin equivalent input source is used. The simplified model will be more accurate if this source is adjusted so that the two models will be operating at the same power level. As will be seen in the next subsection, the Thevenin input resistance, R_{th}, directly effects the converter dynamics, but the Thevenin input voltage, V_{th}, does not. Therefore V_{th} is adjusted to reflect the proper power level and is shown in (4.4).

$$V_{th\_adj} = \frac{P_oR_{th}}{V_{in\_adj}} + V_{in\_adj} \tag{4.4}$$

4.2.2 State-Space Modeling and Transfer Function Derivation

Modeling converters operating in the DCM differs substantially from CCM due to the period of time when the inductor current is clamped to zero. CCM modeling of simple single-switch converters consists of breaking the converter down into two time periods: when the active switch is on and when it is off. However, with DCM, there is a third time period when the inductor current is zero as demonstrated in Figure 4.6. Here d_1 is the duty cycle of the active switch and d_2T_s is the amount of time it takes for the inductor current to reach zero. Because of the DCM period that exists between d_2T_s and T_s, state-space averaging techniques cannot be directly applied to the converter. There have been many proposed methods to model DCM PWM converters [73-75], but perhaps the simplest method was proposed in [76]. Here, the authors develop a state-space matrix the same way that would be done with a CCM converter and then apply a modification matrix, $\boldsymbol{M}$, before performing averaging. This is shown in (4.5) and (4.6) where x is the state vector, u is the input vector, $\boldsymbol{A}$ is the state matrix, and $\boldsymbol{B}$ is the input matrix.

$$\dot{x} = \boldsymbol{AMx} + \boldsymbol{B}u \tag{4.5}$$

$$\mathrm{M} = \begin{bmatrix} \dfrac{1}{d_1 + d_2} & 0 \\ 0 & 1 \end{bmatrix} \tag{4.6}$$

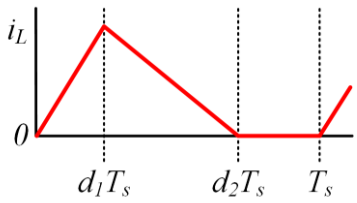


Figure 4.6. Inductor current waveform of a PWM converter operating in the DCM.

Applying this to the simplified circuit model of the converter operating in Buck Mode, the following large-signal state-space model is derived by applying Kirchoff's current and voltage laws (KVL and KCL) to the state variables:

$$\begin{bmatrix} i_{Lr} \\ v_{in\_adj} \end{bmatrix} = \begin{bmatrix} 0 & \frac{nd_1}{L_r} \\ -\frac{nd_1}{C_{in}} & -\frac{1}{R_{th}C_{in}} \end{bmatrix} \begin{bmatrix} \frac{1}{d_1+d_2} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{Lr} \\ v_{in\_adj} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{d_1+d_2}{2L_r} \\ \frac{1}{R_{th}C_{in}} & 0 \end{bmatrix} \begin{bmatrix} V_{th\_adj} \\ V_o \end{bmatrix} \tag{4.7}$$

Since the slope of the inductor current is linear, d_2 can be solved for in terms of d_1. After removing d_2 from the large-signal model, the small-signal model can be derived through conventional perturbation and linearization techniques [54]:

$$\begin{bmatrix} \dot{\tilde{i}}_{Lr} \\ \dot{\tilde{v}}_{in\_adj} \end{bmatrix} = \begin{bmatrix} \frac{-2}{D_{eq}T_{s\_eq}(M-1)} & \frac{nD_{eq}(2M-1)}{L_r(M-1)} \\ 0 & -\frac{1}{R_{th}C_{in}} - \frac{n^2D_{eq}^2T_{s\_eq}}{2L_rC_{in}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{Lr} \\ \tilde{v}_{in\_adj} \end{bmatrix} + \begin{bmatrix} \frac{2nV_{in\_adj}}{L_r} \\ \frac{nD_{eq}T_{s\_eq}V_o(1-M)}{2L_rC_{in}} \end{bmatrix} \tilde{d}_{eq} \tag{4.8}$$

The control-to-input voltage transfer function can now be solved for from the small-signal state-space model. This is shown in (4.9) for the simplified circuit model and is expressed in terms of the full model in (4.10).

$$\frac{v_{in}(s)}{d_{eq}(s)} = \frac{nD_{eq}T_{s\_eq}V_o(1-M)}{2L_rC_{in}} \frac{1}{s + \frac{1}{R_{th}C_{in}} + \frac{n^2D_{eq}^2T_{s\_eq}}{2L_rC_{in}}} \tag{4.9}$$

$$\frac{v_{in}(s)}{\phi(s)} = \frac{n\Phi T_sV_o(1-M)}{4(180)^2L_rC_{in}} \frac{1}{s + \frac{1}{R_{th}C_{in}} + \left(\frac{n\Phi}{180}\right)^2 \frac{T_s}{4L_rC_{in}}} \tag{4.10}$$

The control-to-input voltage transfer functions in (4.10) are plotted in Figure 4.7 and are compared to the control-to-input voltage transfer functions of the full circuit model which were extracted from simulation software. Here the four worst-case operating

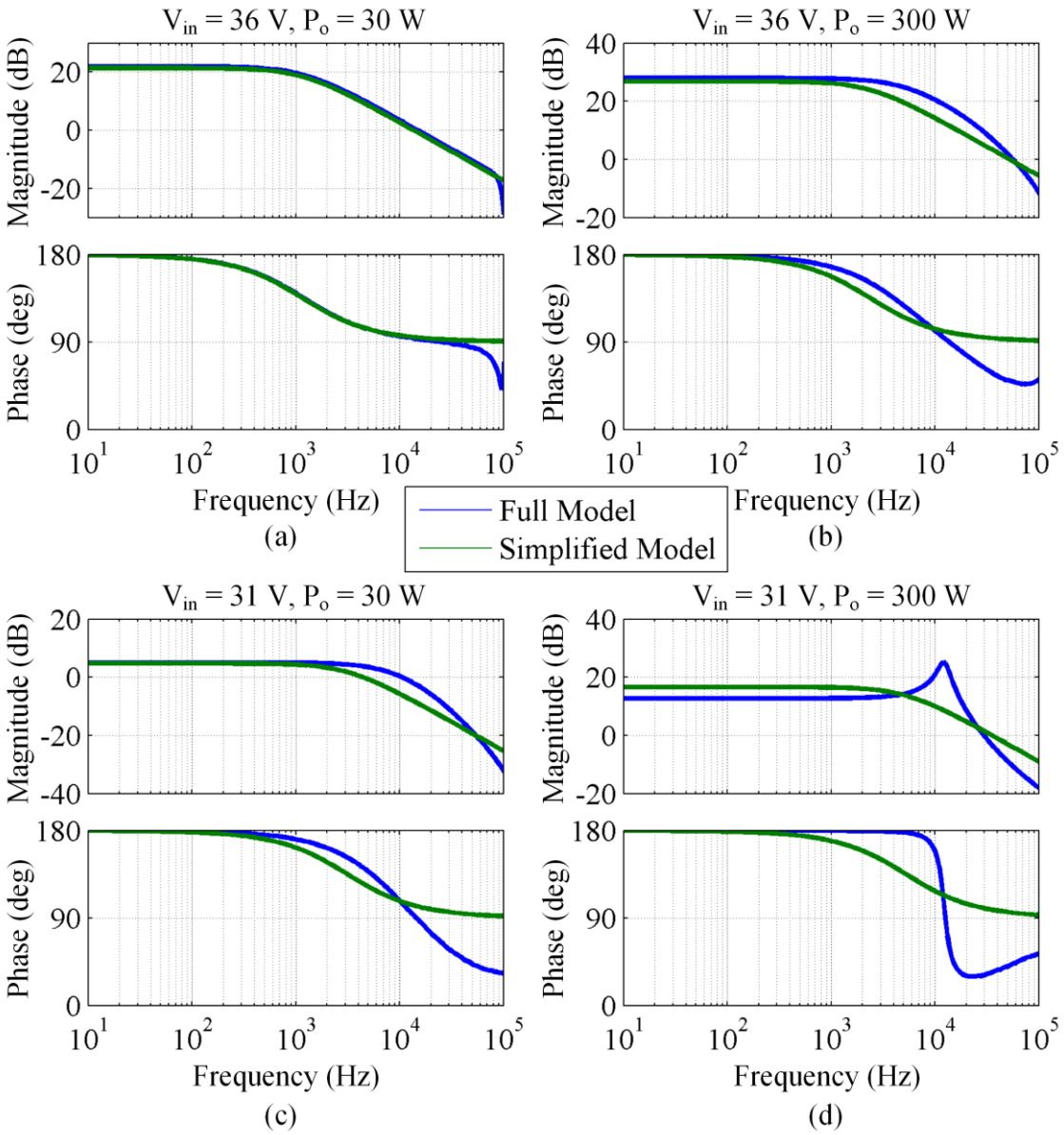


Figure 4.7. Comparison of the Buck Mode full circuit model and simplified circuit model control-to-input voltage transfer functions for the four worst-case operating conditions.

conditions are plotted: minimum and maximum input voltage and minimum and maximum output power. The largest phase angle occurs with the minimum input voltage and maximum output power, shown as (d) in the figure. This results in the least accurate model due to the model simplification process. A voltage controller can now be designed based on these four worst-case transfer functions. Due to the simple two-pole nature of these

transfer functions, controllers with bandwidths in the several kHz range are easy to be realized using a simple proportional integral (PI) controller.

4.3 Boost Mode

4.3.1 Model Derivation

Similar to Buck Mode, C_r can be neglected and the resonant inductor current can be rectified to simplify the converter down to a single-switch PWM converter operating in the DCM. This process is shown in Figure 4.8 along with a comparison of the inductor current before and after simplification. S_{eq} is the single-switch equivalent of the ac switch after rectification. This switch operates at a switching frequency of $2F_s$ (4.11) and with a duty cycle of $2d_{s5}$ (4.12).

$$F_{s\_eq} = 2F_s \qquad T_{s\_eq} = \frac{T_s}{2} \tag{4.11}$$

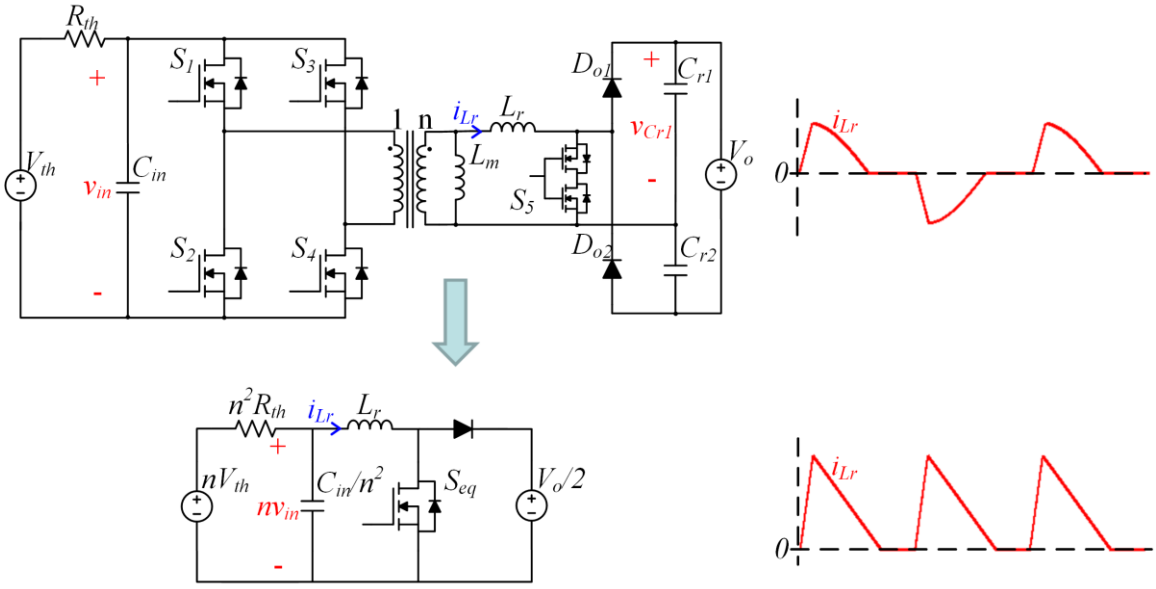


Figure 4.8. Derivation of the simplified circuit model in Boost Mode.

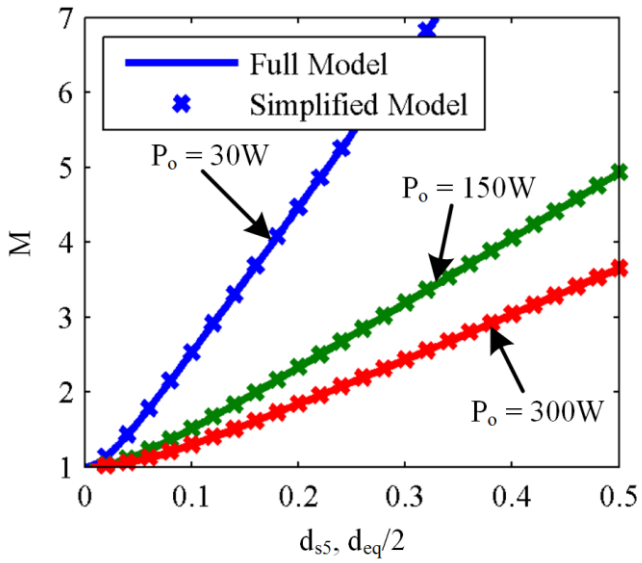


Figure 4.9. Comparison of the conversion ratios of the two Boost Mode circuit models.

$$d_{eq} = 2d_{s5} \tag{4.12}$$

4.3.2 Modeling and Transfer Function Derivation

Applying KVL and KCL to the state variables in the simplified model, the large-signal modified state-space model can be derived:

$$\begin{bmatrix} i_{Lr} \\ v_{in} \end{bmatrix} = \begin{bmatrix} 0 & \frac{n(d_1+d_2)}{L_r} \\ -\frac{n(d_1+d_2)}{C_{in}} & -\frac{1}{R_{th}C_{in}} \end{bmatrix} \begin{bmatrix} \frac{1}{d_1+d_2} & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} i_{Lr} \\ v_{in} \end{bmatrix} + \begin{bmatrix} 0 & -\frac{d_2}{L_r} \\ \frac{1}{R_{th}C_{in}} & 0 \end{bmatrix} \begin{bmatrix} V_{th} \\ V_o \end{bmatrix} \tag{4.13}$$

Once again, d_2 can be removed from this model and the small-signal state-space model can be derived through conventional perturbation and linearization techniques:

$$\begin{bmatrix} \dot{\tilde{i}}_{Lr} \\ \dot{\tilde{v}}_{in} \end{bmatrix} = \begin{bmatrix} \frac{2(M-1)}{Md_{eq}T_{s\_eq}} & \frac{2P_o}{n(V_{in})^2 d_{eq}T_{s\_eq}} + \frac{nd_{eq}}{ML_r} \\ -\frac{n}{C_{in}} & -\frac{1}{R_{th}C_{in}} \end{bmatrix} \begin{bmatrix} \tilde{i}_{Lr} \\ \tilde{v}_{in} \end{bmatrix} + \begin{bmatrix} \frac{V_o}{L_r} \\ 0 \end{bmatrix} \tilde{d}_{eq} \tag{4.14}$$

The control-to-input voltage transfer functions can now be solved for from the small-signal state-space model are given in (4.15) for the simplified circuit. They are expressed in terms of the full model in (4.17).

$$\frac{v_{in}(s)}{d_{eq}(s)} = \frac{-nV_o}{L_r C_{in}} \frac{1}{s^2 + s\left(\frac{2(M-1)}{d_{eq}T_{s\_eq}} + \frac{1}{R_{th}C_{in}}\right) + \alpha_1} \tag{4.15}$$

Where

$$\alpha_1 = \frac{1}{C_{in}}\left(\frac{2(M-1)}{d_{eq}T_{s\_eq}R_{th}} + \frac{1}{V_{in}}\left(\frac{2P_o}{d_{eq}T_{s\_eq}V_{in}} + \frac{nV_o d_{eq}}{2L_r}\right)\right) \tag{4.16}$$

$$\frac{v_{in}(s)}{d_{s5}(s)} = \frac{-nV_o}{L_r C_{in}} \frac{1}{s^2 + s\left(\frac{2(M-1)}{d_{s5}T_s} + \frac{1}{R_{th}C_{in}}\right) + \alpha_2} \tag{4.17}$$

Where

$$\alpha_2 = \frac{1}{C_{in}}\left(\frac{2(M-1)}{d_{s5}T_s R_{th}} + \frac{1}{V_{in}}\left(\frac{2P_o}{d_{s5}T_s V_{in}} + \frac{nV_o d_{s5}}{L_r}\right)\right) \tag{4.18}$$

The control-to-input transfer functions in (4.17) are now plotted in Figure 4.10 and are compared to the control-to-input transfer functions of the full circuit model which were extracted from simulation software. Once again, the four worst-case operating conditions are plotted and a voltage controller can be designed based on them. Controllers with bandwidths in the several kHz range are easy to be realized using a simple PI controller.

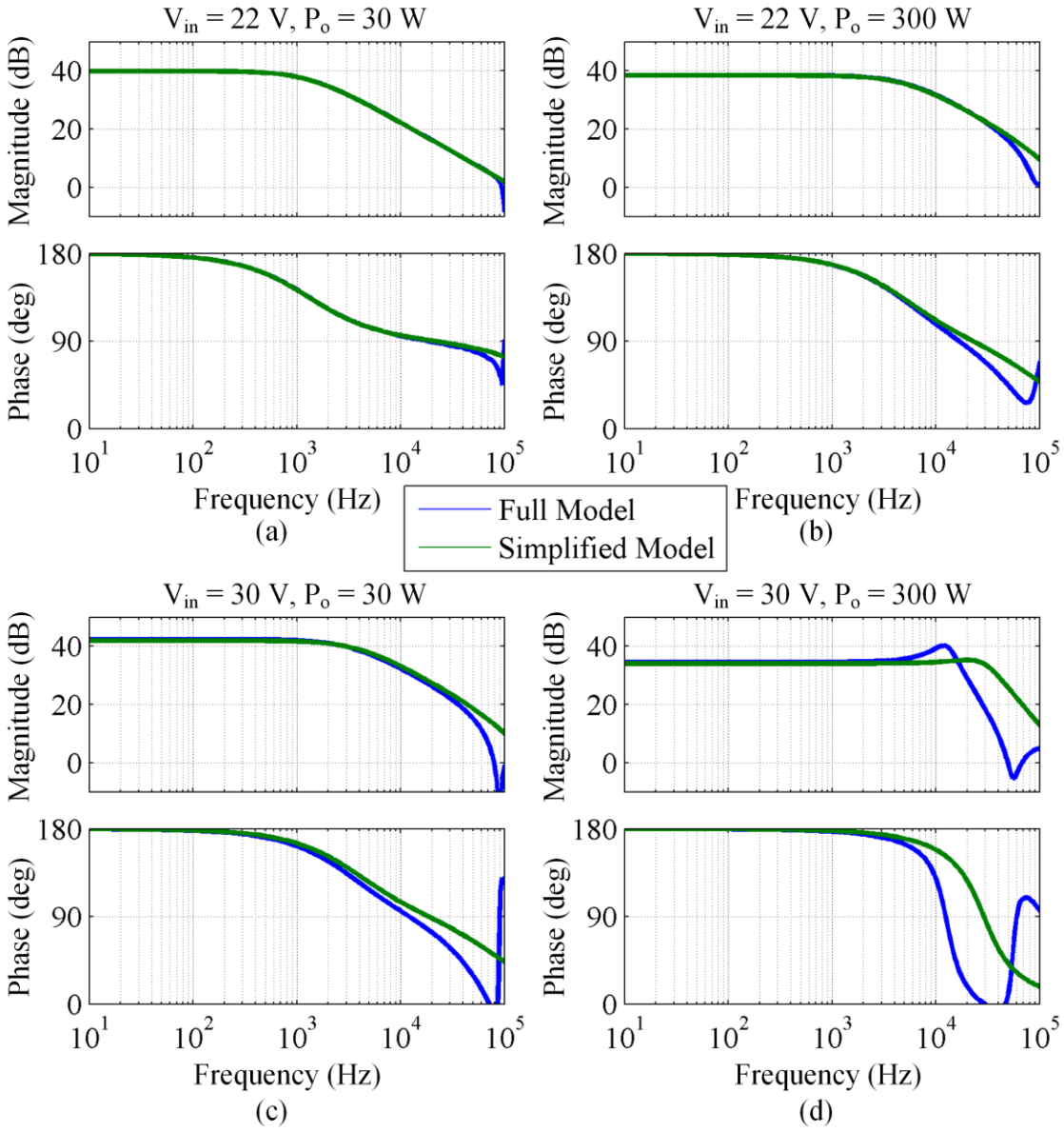


Figure 4.10. Comparison of the Buck Mode full circuit model and simplified circuit model control-to-input voltage transfer functions for the four worst-case operating conditions.

4.4 Modulation and Transition

4.4.1 Modulation Technique

The proposed converter has two modes of operation that need to be controlled, so a smooth transition is necessary to quickly transition between the operating modes while having a minimal impact on the system performance. This can be achieved using a two-carrier modulation technique similar to the techniques used in multi-level cascaded inverter applications [77-79]. A block diagram of the modulation technique is shown in Figure 4.11 and example waveforms are shown in Figure 4.12. The modulator has two different PWM carrier signals – a Buck Mode carrier with an amplitude of V_{m1} and a Boost Mode carrier which is offset by V_{m1} and has an amplitude of V_{m2}. When the output of the voltage controller v_c is below V_{m1}, it is compared to the Buck Mode carrier and the resulting PWM signal is used to phase-shift modulate the primary-side switches. The phase-shift modulator is labeled as the PS Mod block in Figure 4.11. When v_c is above V_{m1}, it is compared to the Boost Mode carrier and the resulting PWM signal can either be used to directly pulse-width modulate the ac switch, or can be used to generate the overlap gating waveforms of the two halves of the ac switch. The ac switch modulator is labeled as the

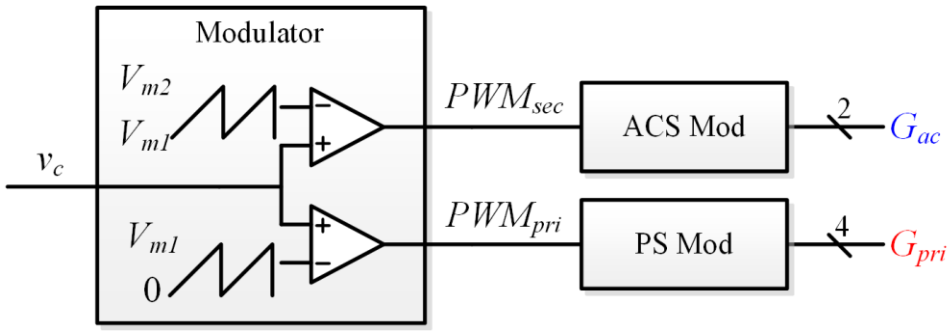


Figure 4.11. Block diagram of the two-carrier modulation technique.

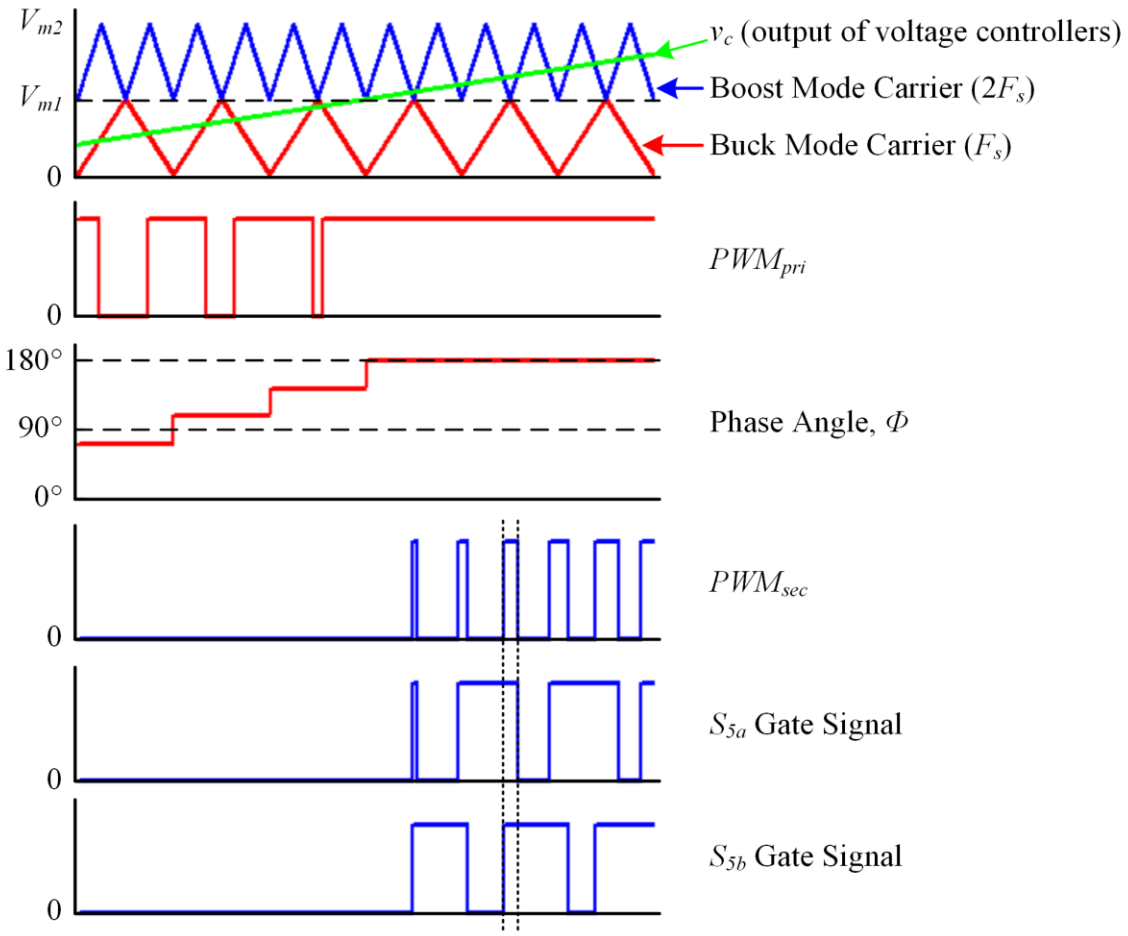


Figure 4.12. Waveforms of the converter's modulator.

ACS Mod block in Figure 4.11. SR Mode naturally occurs when V_{m1} is equal to v_c. Here the primary side switches are switched with a phase angle of 180° and the duty cycle of the ac switch is zero. This modulation technique enables a smooth transition between operating modes and controls the gating signals of all of the active switches.

4.4.2 Transition

Each mode of operation has its own voltage controller, so the two controllers need to be implemented in a manner that will also facilitate a smooth transition. This is accomplished by having the two PI controllers share a common integrator and the

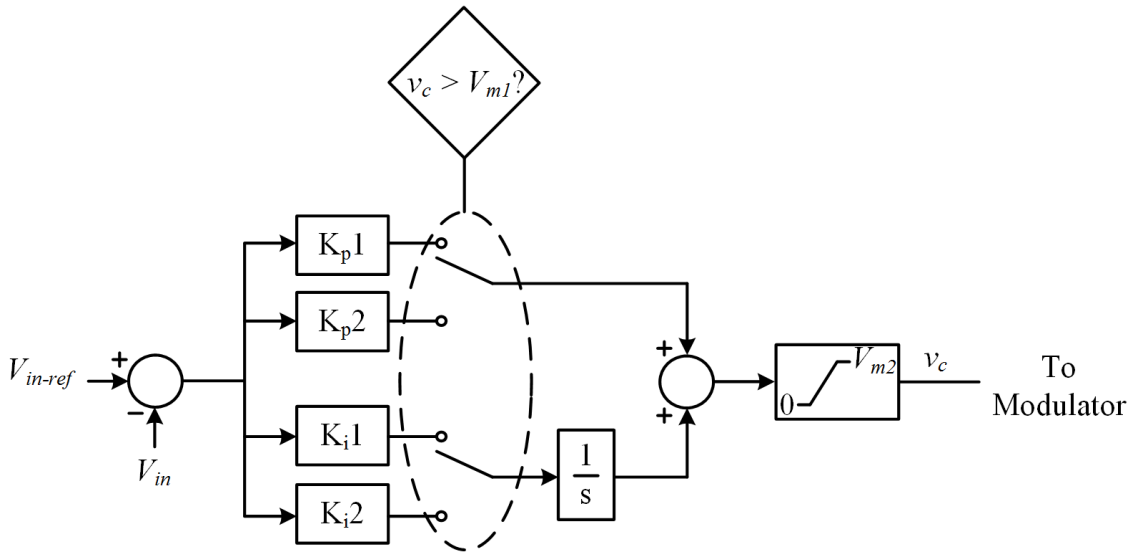


Figure 4.13. Block diagram of the dual-controller implementation.

proportional and integral gains are switched based on the operating mode. Sharing an integrator between the two controllers allows the final condition of one controller to be used as the initial condition of the other controller during the transition. This allows the new controller that is taking over to reach its steady-state much faster. A block diagram of the dual-controller implementation is shown in Figure 4.13. Here K_{p1} and K_{i1} are the proportional and integral gains of Buck Mode and K_{p2} and K_{i2} are the proportional and integral gains of Boost Mode. The two sets of gains are switched between based on the level of v_c.

4.5 Experimental Results

Two different PI controllers—one for Buck Mode and one for Boost Mode—are designed to control the microconverter under all of the input voltage and output power operating conditions discussed in the previous subsections. The voltage controllers, modulators, and transition method are now implemented digitally in the DSP of the

microconverter prototype. The input voltage is sensed through a simple resistive divider network.

In order to verify the bandwidths and phase margins of the designed PI controllers for each operating mode, the loop gain transfer functions are measured using a Venable Frequency Response Analyzer (FRA) Model 350c. The experimental setup is shown in Figure 4.14. The same dc power supply and series input resistance from Section 3.3 is used to emulate a PV module and the same electronic dc load is used to regulate the output voltage to 380 V. During the experiments, the microconverter controls the input voltage and the power level is adjusted by varying the voltage of the input dc power supply. In order to measure the loop gain using the Venable FRA, an injection resistor is added to the resistive voltage sensing network of the converter. The injection resistor is much smaller (~1000 times) than the sensing resistors so it has a minimal impact on the converter's voltage sensing. Using the FRA, a variable-frequency voltage signal is applied across the injection resistor and the ac voltage is measured both before and after the injection resistor (points A and B in Figure 4.14) in order to determine the control-to-input voltage transfer functions.

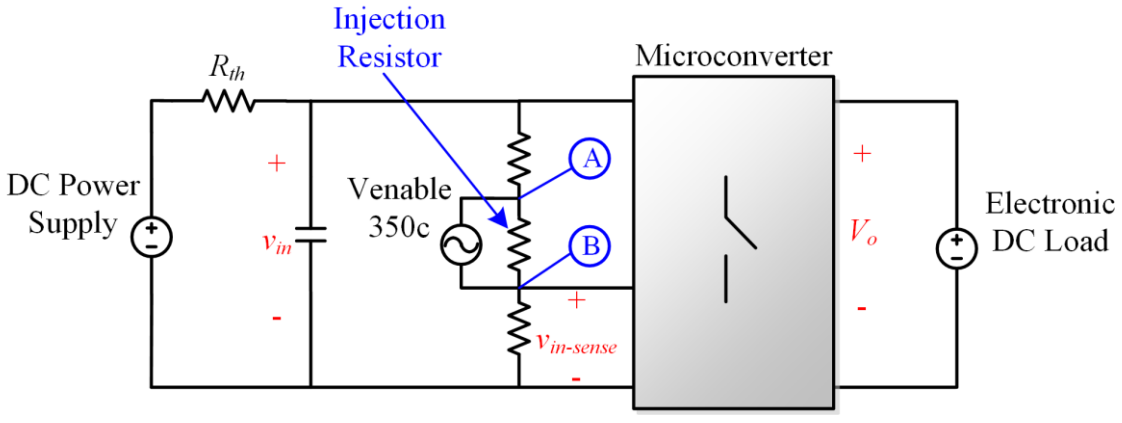


Figure 4.14. Experimental setup for measuring loop gain transfer functions.

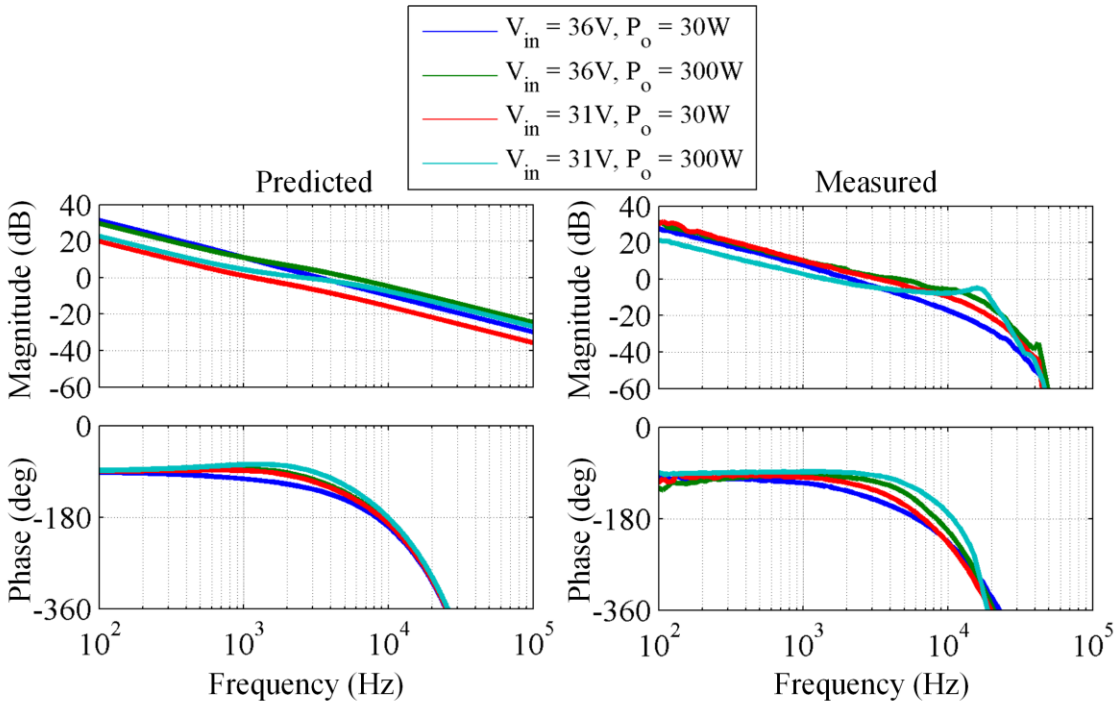


Figure 4.15. Predicted and measured loop gains for the four worst-case operating conditions in Buck Mode.

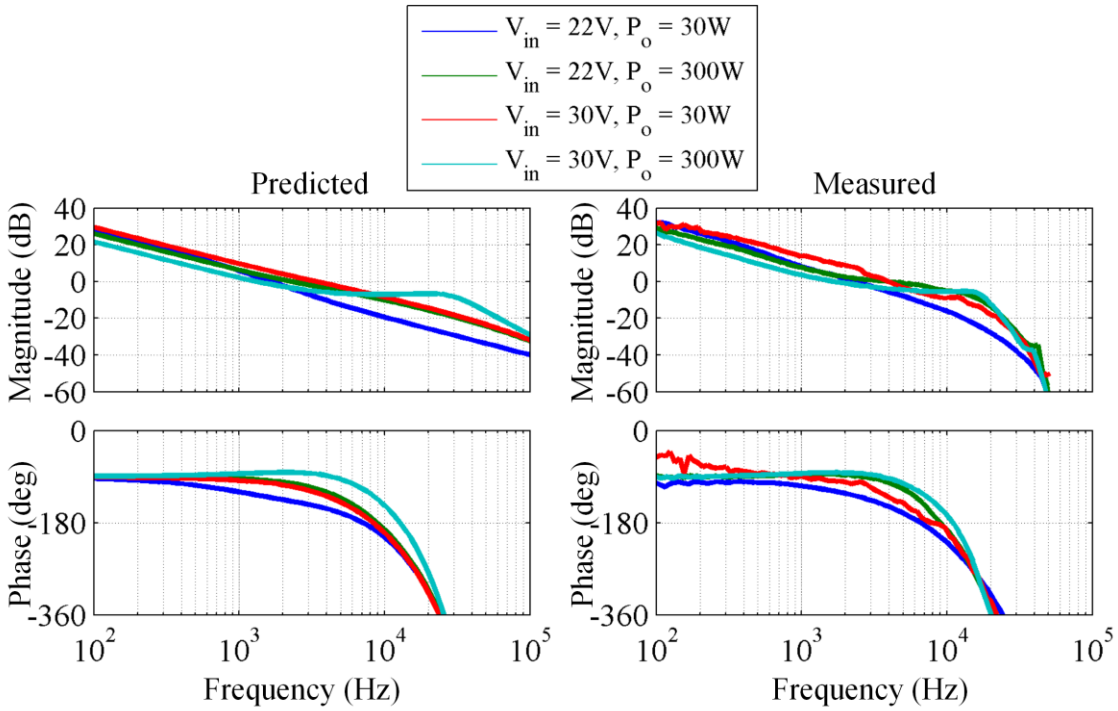


Figure 4.16. Predicted and measured loop gains for the four worst-case operating conditions in Boost Mode.

Table 4.1. Comparison of performance between predicted and measured loop gains

Parameter	Buck Mode	Boost Mode
Predicted Bandwidths	1.2 – 5.5 kHz	1.3 – 3.4 kHz
Predicted Phase Margins	42 - 95°	49 - 97°
Measured Bandwidths	1.4 – 4.6 kHz	1.6 – 4.0 kHz
Measured Phase Margins	49 - 97°	49 - 97°

Loop gains of the converter for the four worst-case operating conditions in Buck Mode were measured and compared to the predicted loop gains in Figure 4.15. The same was done for the four worst-case operating conditions in Boost Mode in Figure 4.16. A summary of the predicted and measured bandwidths and phase margins for the different operating modes is given in Table 4.1. The performance of the predicted and measured loop gains match well, which shows the simplified single-switch PWM models are valid for designing controllers with bandwidths in the several kHz range. It can be seen from looking at the measured loop gains of both Buck and Boost Modes that the models are less accurate at frequencies above the designed controller bandwidths. This is due to the high-frequency dynamics introduced by C_r, which are neglected in the simplified models.

In order to validate the proposed dual-modulation carrier and transition technique, transitions are now made between Buck and Boost Modes while observing the transient response of the input voltage. First, a transition using a relatively large 5-V step is made between a 28-V input and 33-V input. The results are shown in Figure 4.17 for (a) a step from 28 V to 33 V and (b) from 33 V to 28 V. The transitions are made with the converter operating close to a 250-W output. At this power level, series resonant mode occurs close to a 31.5-V input which is the boundary between Buck and Boost Modes. For both transitions, the input voltage reaches its steady-state value within 500 μs which is relatively fasted compared to the control bandwidths of 1.4 – 4.6 kHz.

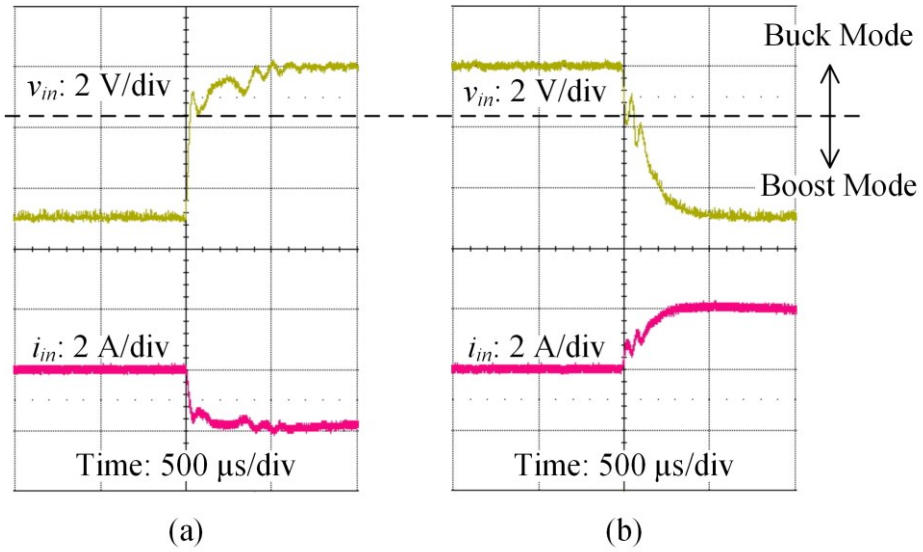


Figure 4.17. Input voltage and current of prototype during transitions from (a) Boost Mode to Buck Mode and (b) Buck Mode to Boost Mode with a step size of 5 V.

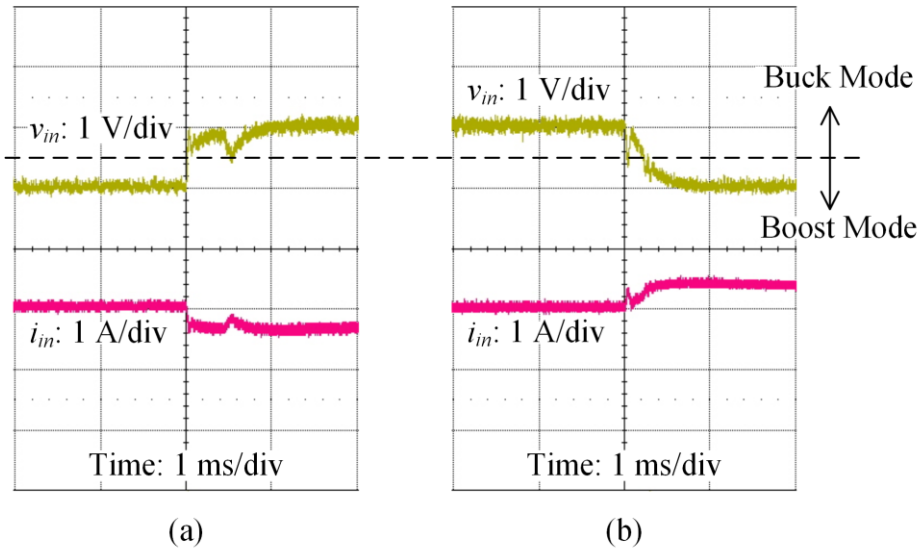


Figure 4.18. Input voltage and current of prototype during transitions from (a) Boost Mode to Buck Mode and (b) Buck Mode to Boost Mode with a step size of 1 V.

Next, a transition using a smaller 1-V step is made between a 31-V input and 32-V input to see how the converter performs when operating very close to the series resonant point of operation. Once again, the power level of the converter is 250 W which results in the boundary between the operating modes being 31.5 V. The results of these transitions are shown in Figure 4.18 for (a) a step from 31 V to 32 V and (b) a step from 32 V to 31V.

These transitions are a little slower than the 5-V case with the input voltage reaching steady-state in close to 750 μs. This is expected since the magnitudes of the control-to-input voltage transfer functions are smaller as the converter operates closer to the series resonant frequency, especially at higher power levels. This is evident from the loop-gain functions.

4.6 Summary

A simplified circuit model was derived for the proposed converter for both Buck and Boost modes of operation. This simplified circuit model neglects C_r, thereby removing all resonant characteristics of the converter allowing it to be modeled as a simple single-switch PWM converter operating in the DCM. This model is accurate in the low frequency range, up to approximately 10 kHz, because the dynamics C_r introduce to the converter are at higher frequencies due to its small value. Control-to-input voltage transfer functions for these simplified circuit models are then derived using simple modified state-space averaging. Voltage controllers can then be designed for each mode based on the four worst-case operating conditions: maximum and minimum input voltage and maximum and minimum output power.

Since the proposed converter employs two different operating modes, each with its own voltage controller, a smooth transition technique is introduced to transition between the operating modes. This is accomplished using a two-carrier PWM modulator along with a voltage controller implementation where both controllers share a common integrator. Experimental measurements of the converter's loop gain transfer functions were given to demonstrate the accuracy of the simplified circuit models, and step-response waveforms

were given of the converter transitioning back and forth between Buck Mode and Boost Mode in order to demonstrate the performance of the proposed transition method.

Chapter 5

System-Level Integration

5.1 PV Power Conditioning System Components

Three different PV power conditioning systems that the proposed microconverter is well suited were discussed in Chapter 1: (a) two-stage microinverters, (b) distributed microconverters with a centralized inverter, and (c) distributed microconverters in a dc microgrid application. All three power conditioning systems consist of a single PV module connected to a single microconverter, with each module/converter combination feeding some type of downstream power converter. Because this microconverter is suitable for different applications where the output will be connected to different types of converters, it is important that it be designed to handle system-level issues associated with all of the possible target applications. The major system-level issues that need to be addressed are soft start for current limiting during the microconverter startup, maximum power point tracking of the PV module, and double line frequency voltage ripple rejection on the input of the microconverter.

5.2 Diode-Clamped Soft Start

5.2.1 Introduction of Startup Issue

The effective output capacitance of a single microconverter is the entire capacitance of the dc bus, which can be very high since the dc bus is designed to operate as a voltage

source. This dc bus capacitance is made up of the parallel combination of the on-board output capacitor of the microconverter, the output capacitance of any other parallel connected converters, and the input capacitance of any down-stream second-stage converters such as grid-tied inverters. This capacitance will vary greatly depending on the application. For example, in a microinverter application where the only converter connected to the output of the microconverter is a low power inverter, the output capacitance could be on the order of 10's of μF. In a centralized inverter application, it's possible for this capacitance to be on the order of 10's of mF. For a dc micro-grid application, this capacitance could be much bigger depending on how many and of what power level the converters are that are connected to the dc bus.

Many applications require the microconverter to possess the ability to start up with no dc bus present on its output. This is especially true of PV applications such as microinverters and centralized- and string-inverter systems where the grid-tied inverter connected to the dc bus is unidirectional. This means power is only designed to be transferred in one direction from the dc bus to the ac grid, so it is not possible to use the ac grid to charge the dc bus during startup. These inverters are not meant to operate until the dc bus voltage is greater than the peak ac line voltage. Therefore, it is the duty of the microconverters to pre-charge the dc bus voltage before the inverter can begin to operate. Even in applications where there are several microconverters connected in parallel, each one needs to possess the ability to charge the entire dc bus on its own. The first microconverter to go on-line during startup will bear the full burden of charging the dc bus, therefore, each converter needs to be able to handle startup with a very large output capacitance.

During startup, the initial condition of the microconverter's output capacitance is zero volts as shown in Figure 5.1. This zero-voltage capacitive load appears as a short circuit during startup which can result in large current and voltage stresses throughout the converter that may over-stress the converter's components causing failure. As a result, it is necessary to implement a soft start algorithm to limit the potentially devastating startup transients. The I-V characteristics of a PV module tell us that the converter will be starting up from the module's open-circuit voltage, so the converter will be starting up in Buck Mode. In Buck Mode, the ac switch is not used so the startup conditions are very similar to that of a full-bridge series resonant or LLC converter with a voltage doubler rectifier.

Startup characteristics of resonant converters have been discussed in literature [80-83] along with several different soft start and overcurrent protection methods. The most commonly used method for resonant converters that utilize variable frequency control is to begin switching at a very high frequency during startup, much higher than the normal operating frequency range, and then to ramp the frequency down to the normal operating range [84-86]. This method, however, is not practical for implementation in a fixed-frequency converter. Once of the greatest benefits of the proposed microconverter

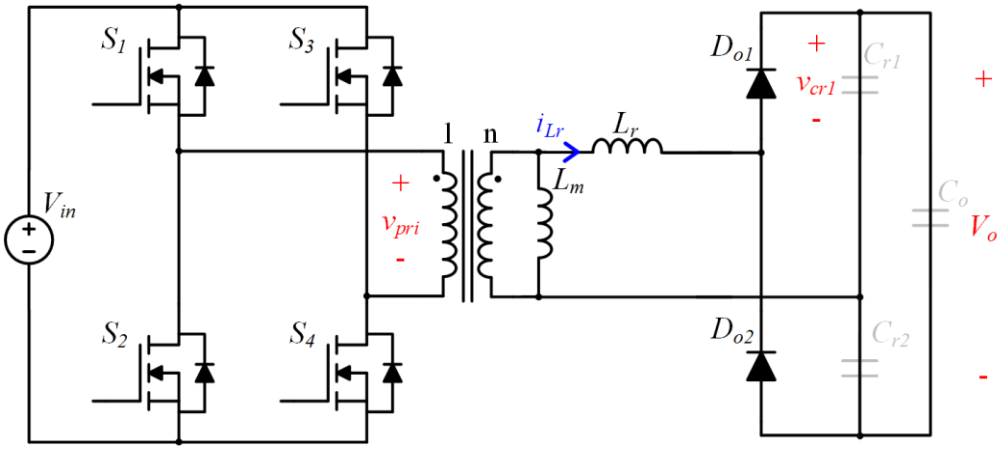


Figure 5.1. Initial conditions of the microconverter during startup.

topology is its ability to operate with simple fixed frequency control which makes implementation of modulation and control simple, whether it is to be digital or analog. Another method for limiting inrush current during startup of resonant converters is to pulse-width modulate the primary side devices with a very small duty cycle (or phase-shift modulate with a very small phase angle) and slowly ramp up the duty cycle or phase angle [87, 88]. Since the proposed converter starts up in Buck Mode, which is phase-shift modulated, this method is actually inherent to the converter operation. The converter starts with a phase angle of zero, and the voltage controller ramps up the phase angle until the steady-state operating condition is reached. This soft start method is excellent for limiting inrush current from the PV module, but as is explored in [88], the inrush current from the input source isn't the biggest problem. While the input current to the converter may be small, it is possible for the circulating energy in the resonant tank to increase to very large levels that will result in unusually high currents and voltages. This phenomenon will be further explored in the next subsection. In order to avoid this problem in the resonant tank during startup, several authors have proposed adding additional circuit components to clamp the resonant capacitor voltages, which in turn clamps the resonant inductor currents [89-91]. These clamp circuits are effective, but consist of adding extra capacitors, diodes, transformer windings, and even an extra transformer that adds additional cost and complexity of control to the converter.

One of the more attractive clamp circuits that appears in literature is the diode clamp presented in [92, 93]. Here, the resonant capacitor is split into three capacitors, two of which make a capacitive voltage divider across either the input or output dc source, V_{dc}. These two capacitors in the voltage divider network have clamp diodes placed in parallel

with them. The capacitor values are designed so that when an overcurrent condition exists, the ripple across the resonant capacitors exceeds $V_{dc}/2$ and the diodes clamp the voltage to V_{dc}. This effectively removes these capacitors from the resonant tank which changes the resonant frequency to limit power flow. Adopting the idea of clamping the capacitor voltages with diodes, a soft start solution is proposed for the microconverter that limits transients during startup and allows the converter to start up with very large output capacitances while adding only a single diode to the converter topology.

5.2.2 Proposed Soft Start Solution

Before the proposed soft start solution is introduced, it is important to analyze the converter during startup to determine exactly what issues exist and what causes them. During initial startup the output capacitance appears as a short circuit, so the following analysis will assume a short-circuited output. Analyzing the converter with a short-circuited output will not only allow for the design of a soft start solution that will be able to handle very large capacitances, but also one that can handle the converter attempting to start up under a true short-circuited output condition without failure.

In order to reduce the inrush currents from the input source of the converter, the converter begins operating from a phase angle $\Phi = 0$ and slowly ramps up. As a result,

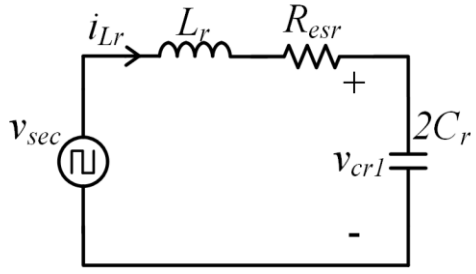


Figure 5.2. Equivalent circuit model of resonant tank during beginning of startup with a short-circuited output.

during initial startup, the phase angle is very small and the applied voltage across the primary winding of the isolation transformer consists of pulses with very small pulse widths. An equivalent circuit of the resonant tank useful for analyzing startup when the output is short circuited is shown in Figure 5.2. First, let us assume a single pulse with a very narrow pulse width is applied to the transformer. Simulation results of this condition are shown in Figure 5.3 where R_{esr} represents the lump sum of the dc resistance of the primary and secondary transformer windings, the equivalent series resistance (ESR) of the resonant capacitors, and if applicable, the ESR of the external resonant inductor. For the simulation, the same circuit parameters from Chapter 3 are used with an input voltage of 40 V and R_{esr} is set to 0.45 Ω. The time constant of this circuit is:

$$\tau = \frac{2L_r}{R_{esr}} \tag{5.1}$$

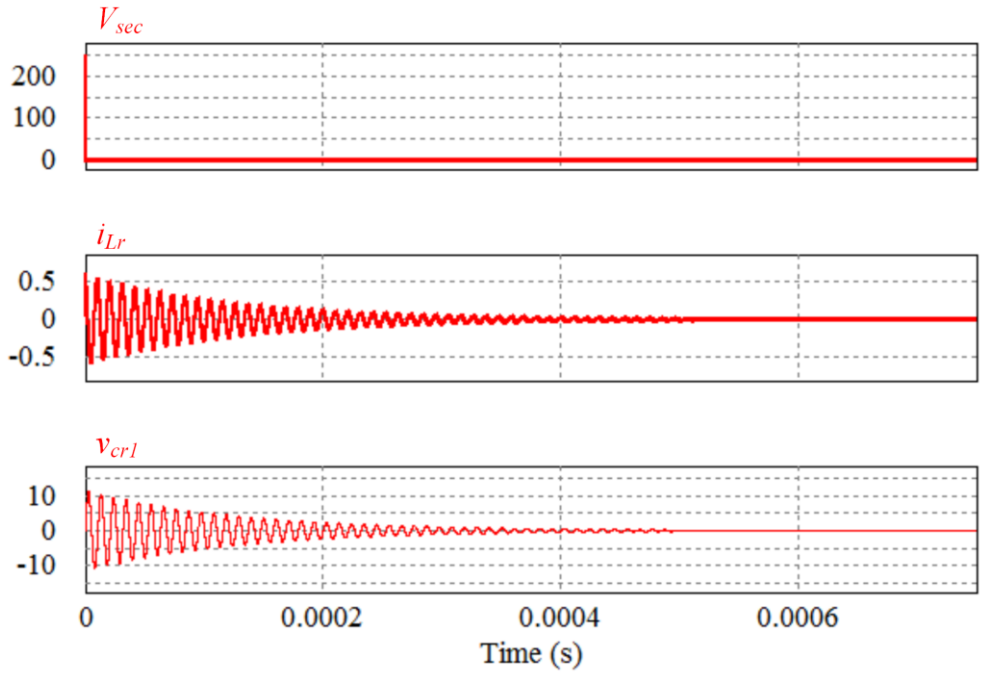


Figure 5.3. The voltage across the secondary winding of the transformer v_{sec}, resonant inductor current, and resonant capacitor voltage during startup after a single pulse is applied to the isolation transformer.

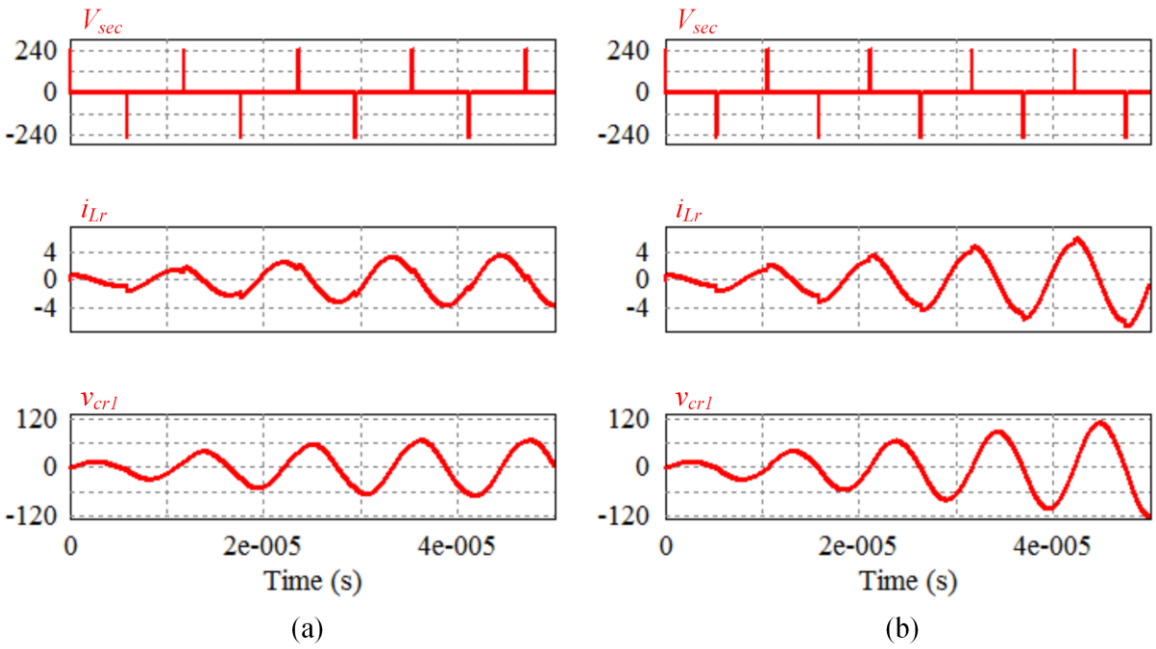


Figure 5.4. Initial resonant inductor current and capacitor voltage during startup with (a) $F_s/F_r = 0.9$ and (b) $F_s/F_r = 1.0$.

For the simulated case, $\tau = 142$ µs. With a switching frequency of 100 kHz, this means that after the first pulse is applied, it takes around 5τ or 71 switching cycles for the resonant tank current to reach zero. If the pulses are applied continuously to the resonant tank, the currents will add with each pulse as seen in Figure 5.4. The amount of current that will be added with each pulse depends on the phase angle, and the point along the sinusoidal current waveform that the current is added to depends on the ratio of F_s/F_r. The worst case scenario will occur when $F_s/F_r = 1$ because the current pulses will be added at the peaks of the current waveform. Figure 5.4 shows the current adding in the resonant inductor for (a) $F_s/F_r = 0.9$ and (b) $F_s/F_r = 1.0$.

Over time, these adding currents will increase until the equivalent circuit reaches steady-state. It is possible for these steady-state values to be very large and for the voltage rating of the resonant capacitors and ac switch to be exceeded causing failure (as has been accidentally proven several times experimentally). Figure 5.5 shows simulation results of

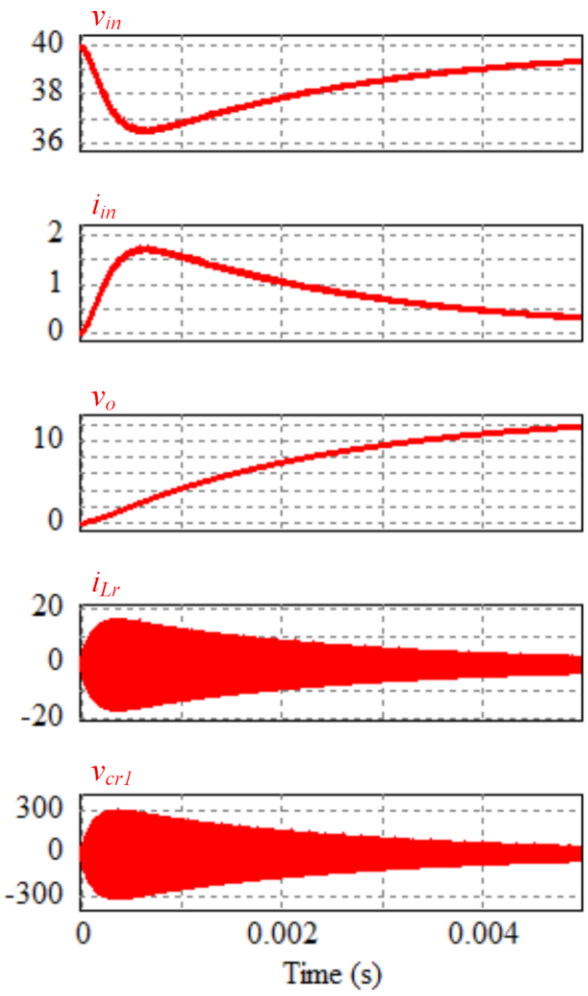


Figure 5.5. Simulation of startup with C_o = 1 mF and Φ = 3.5°. Here the three sensed variables V_{in}, I_{in}, and V_o are shown along with the resonant tank current and voltage.

the converter starting up with an output capacitance of 1 mF and a phase angle of 3.5°. In the beginning, v_{cr1} exceeds 300 V which would have killed the 250-V rated resonant capacitors or the 250-V rated S_5 of the designed prototype. The sensed variables of the converter are V_{in} and I_{in} for MPPT control and V_o for protection. These three variables are also shown in Figure 5.5. Based on these three sensed variables, there is no way of knowing that the converter would fail. Therefore, when Φ is ramping up during startup, it is important that it is limited to prevent v_{cr1} from becoming too high and destroying the

converter in the case of a short-circuited output. Since it's not possible to determine the limit for Φ from sensed variables, it needs to be calculated.

In order to determine the maximum value for Φ, the steady-state values of i_{Lr} and v_{cr} need to be calculated for the worst case scenario which happens when $F_s/F_r = 1$. In this scenario, the positive voltage pulses applied to the resonant tank occur when i_{Lr} is at its peak and the negative pulses are applied when i_{Lr} is at its valley. Each half-switching cycle the peak value of i_{Lr}, $i_{Lr\text{-}pk}$, is increased by $i_{Lr\text{-}add}$ (5.2), which is induced by the voltage pulses from the isolation transformer.

$$i_{Lr-add} = \frac{nV_{in}\phi T_s}{360L_r} \tag{5.2}$$

Also, during each half switching cycle, the magnitude of i_{Lr} decreases by a certain amount, $i_{Lr\text{-}decay}$ (5.3), due to the exponential decay characteristics of the resonant tank's equivalent RLC circuit.

$$i_{Lr-decay} = I_{Lr-pk}\left(1 - e^{-\frac{T_s}{2\tau}}\right) \tag{5.3}$$

Steady state will occur when the amount of current added to the resonant tank each half-cycle is equal to the amount of current decay in the resonant inductor over one half switching cycle. The maximum voltage across C_r, $V_{cr\text{-}max}$, is equal to the resonant current multiplied by the characteristic impedance of the resonant tank (5.4). Plugging this value into (5.3) and then equating (5.2) and (5.3), a formula can be derived for the maximum phase angle, Φ_{max}, based on a maximum desired $V_{cr\text{-}max}$ (5.5).

$$V_{cr-\boldsymbol{max}} = I_{Lr-pk}Z_r \tag{5.4}$$

$$\phi_{max} = \frac{360 V_{cr-max} L_r \left(1 - e^{-\frac{T_s R_{esr}}{4 L_r}}\right)}{Z_r n V_{in} T_s} \tag{5.5}$$

As an example, if the parameters from the designed prototype in Chapter 3 are used and $V_{cr\text{-}max}$ is set to 250 V, Φ_{max} is calculated to be 2.1°. Simulation results of the converter starting up with a short-circuited output and a phase angle of 2.1° are shown in Figure 5.6 for (a) $F_s/F_r = 0.9$ and (b) $F_s/F_r = 1.0$. It can be seen in the figure that there is a very large difference in the resonant tank for just small variances of switching frequency ratio. In a real world application, it is very possible to see switching frequency ratios vary by ± 10% due to component tolerances in the resonant inductance and capacitance values. There is a trade-off between the startup phase angle and the length of time it takes to charge the output capacitance, and using a conservative design approached based on the worst case scenario (5.5), the resulting Φ_{max} would be very small resulting in long startup times.

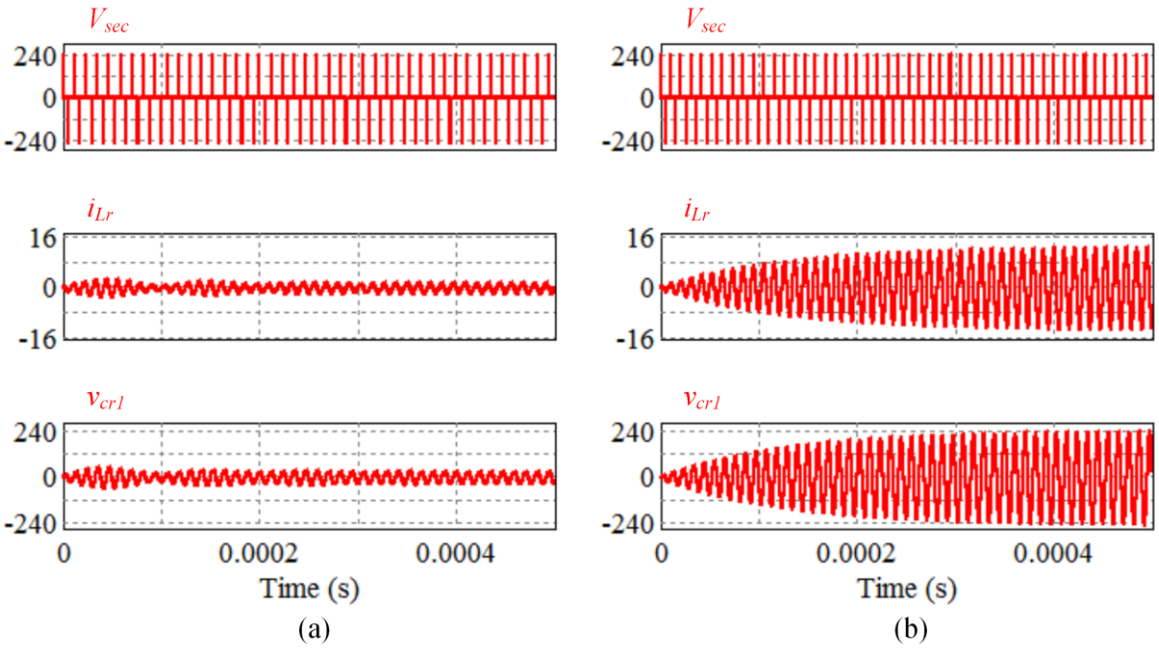


Figure 5.6. Simulation of converter startup with a short-circuited output and $\Phi = 2.1°$. The switching frequency ratio is (a) $F_s/F_r = 0.9$ and (b) $F_s/F_r = 1.0$.

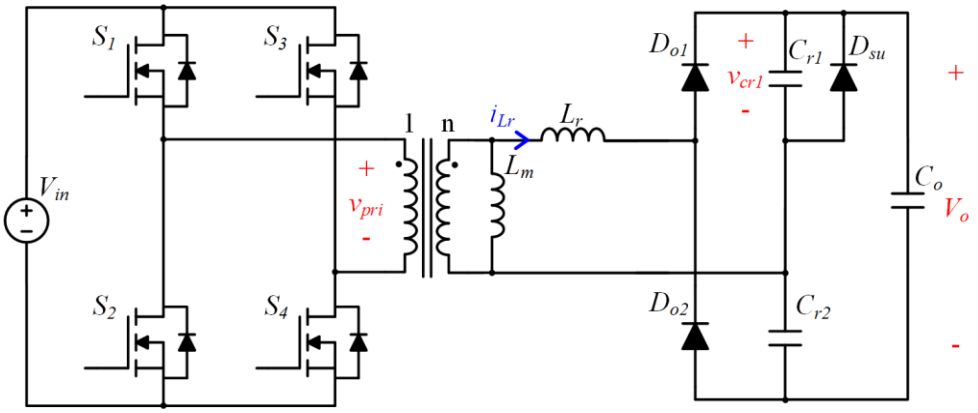


Figure 5.7. Topology of microconverter with proposed soft start diode.

The proposed soft start method allows for a much larger Φ_{max} and is shown in Figure 5.7. Here, a single diode, D_{su}, is placed in parallel with one of the resonant capacitors. This diode effectively removes the resonant properties of the resonant tank during startup by clamping v_{cr1} to zero and not letting it resonate to a negative value. Once the converter has started up and is operating in steady state, v_{cr1} will always be positive, so D_{su} will have no effect on normal converter operation. This diode allows for a larger phase angle to be used for faster startup. It also makes the system much more predictable and less dependent on component tolerances. An example of resonant tank waveforms during

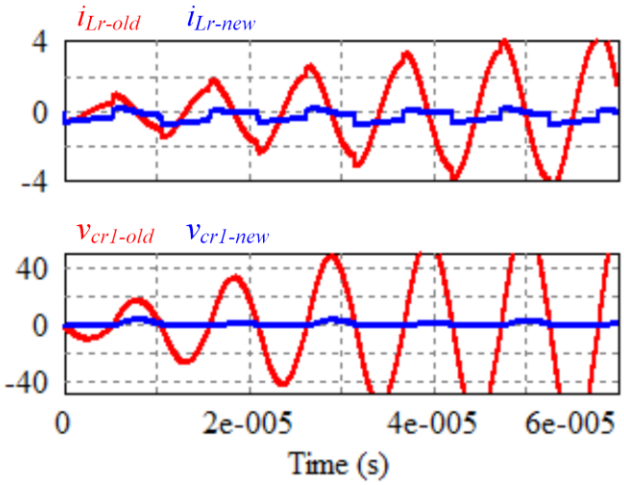


Figure 5.8. Comparison of resonant tank waveforms during startup with (blue) and without (red) the startup diode.

startup with and without the diode are shown in Figure 5.8. For both cases, Φ is 2.1°. Without the diode, the resonant current and voltages increase each half-switching cycle and add up to large values, while with the diode the current and voltage are clamped and remain small. The peak current, $I_{lr\text{-}pk}$, is now (5.6). Previously, the factor that was limiting Φ_{max} was $V_{cr\text{-}max}$, but now that $V_{cr\text{-}max}$ is clamped, the limiting factor is the power dissipation in the startup diode, P_d (5.7), where v_f is the forward voltage drop of the diode. Φ_{max} is now recalculated for a given P_d in (5.8).

$$I_{Lr-pk} = \frac{nV_{in}\phi T_s}{360L_r} \tag{5.6}$$

$$P_d = \frac{1}{2} I_{Lr-pk} v_f \tag{5.7}$$

$$\phi_{max} = \frac{720L_r P_d}{nV_{in} T_s v_f} \tag{5.8}$$

Using the same design example, Φ_{max} is now 22° if P_d is limited to 2 W, which is more than 10 times larger than the previous Φ_{max}. Simulation results comparing startup with and without the diode are shown in Figure 5.9 with (a) C_o = 10 µF and (b) C_o = 1 mF. Without the diode, Φ_{max} is 2.1° and with the diode Φ_{max} is 22°. For both output capacitance cases, the converter charges the output capacitance much faster with the output diode.

The startup procedure using the startup diode is very simple to implement. The steps are as follows:

1. Sense the converter input voltage before startup (the module's V_{oc}) and command an input voltage below V_{oc} so that the voltage controllers begin to operate.
2. Limit the phase angle based on the sensed output voltage.

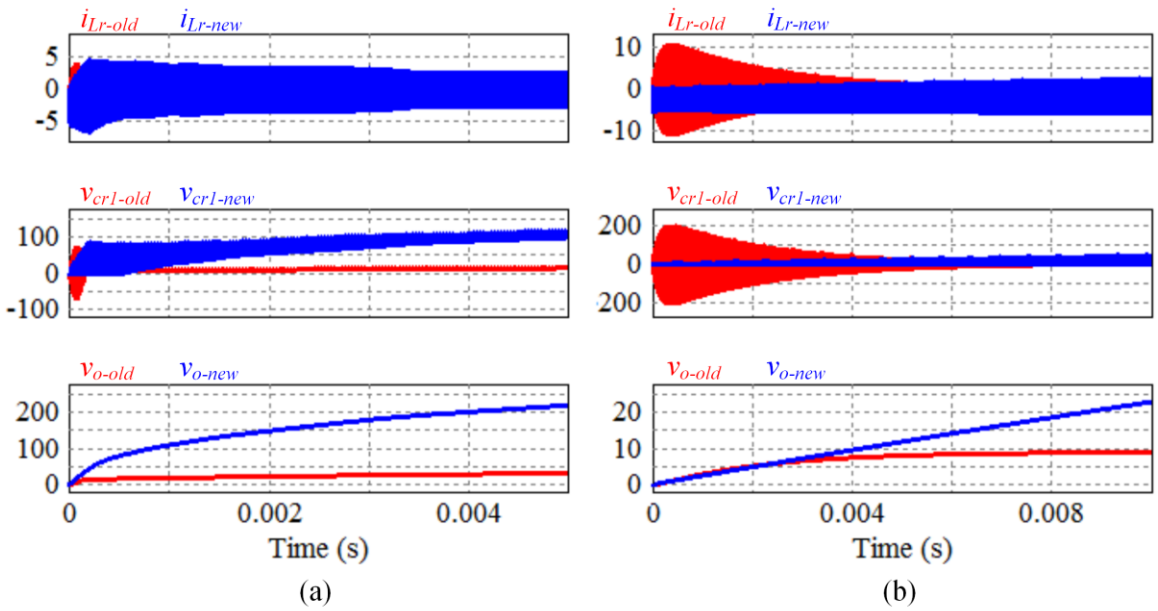


Figure 5.9. Simulated comparison of converter startup with and without startup diode with (a) C_o = 10 µF and (b) C_o = 1 mF.

3. When the output voltage reaches its full value, begin MPPT.

Step 1 automatically happens from the MPPT algorithm so basically the only change that needs to be made to the control algorithm is to pause the MPPT steps and limit the phase angle until the proper output voltage is reached. It is important that initially the phase is limited to Φ_{max} calculated in (5.8) in case of a short-circuit output condition. Once the output voltage begins increasing, it is safe to assume there is no short circuit on the output and Φ_{max} can be incrementally increased as the output voltage increases in order to accelerate the converter startup.

Short-circuit detection and protection is also very simple. A short circuit is detected if the converter is operating and the output voltage remains 0 for an extended period of time. Protection happens naturally since the initial Φ_{max} was calculated in (5.8) in order to allow the converter to operate without failure under a short-circuit condition.

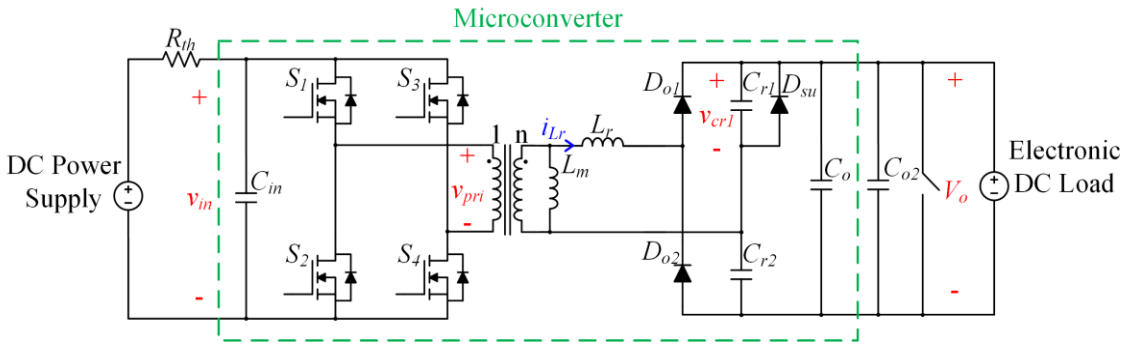


Figure 5.10. Experimental setup for verifying the proposed soft start method.

5.2.3 Experimental Results

The experimental setup for verifying the proposed soft start method is shown in Figure 5.10. For the tests, the output capacitance will vary between 1.2 µF which is the on-board output capacitance, 4.7 mF which is provided by an external capacitor, and a short circuit. Figure 5.11 shows startup with a short-circuited output (a) without the diode and $\Phi = 2.1°$ and (b) with the diode and $\Phi = 22°$. In (a), i_{Lr} increases with each switching cycle resulting in a large v_{cr}, while in (b) i_{Lr} is clamped and the resonant capacitor voltage remains small. Figure 5.12 shows the same condition after the converter has reached steady-state. In Figure 5.12 (a), $V_{cr\text{-}max}$ is around 70 V. In Figure 5.12 (b), Φ is more than 10 times larger and the $V_{cr\text{-}max}$ is only 15 V.

In order to determine the effect component tolerances of the resonant inductance and capacitance will have on startup, F_s/F_r is varied by adjusting F_s. This will have a similar effect as the resonant component values varying F_r. Startup without the diode is shown in Figure 5.13 for (a) $F_s/F_r = 0.9$, (b) $F_s/F_r = 1.0$, and (c) $F_s/F_r = 1.1$. As the frequency ratio varies by 10%, the i_{Lr} and v_{cr1} vary by more than 200%. Startup with the diode is shown in Figure 5.14 for (a) $F_s/F_r = 0.9$, (b) $F_s/F_r = 1.0$, and (c) $F_s/F_r = 1.1$. With the diode, i_{Lr} and v_{cr1} only vary by 10% as the frequency ratio varies by 10%. This shows

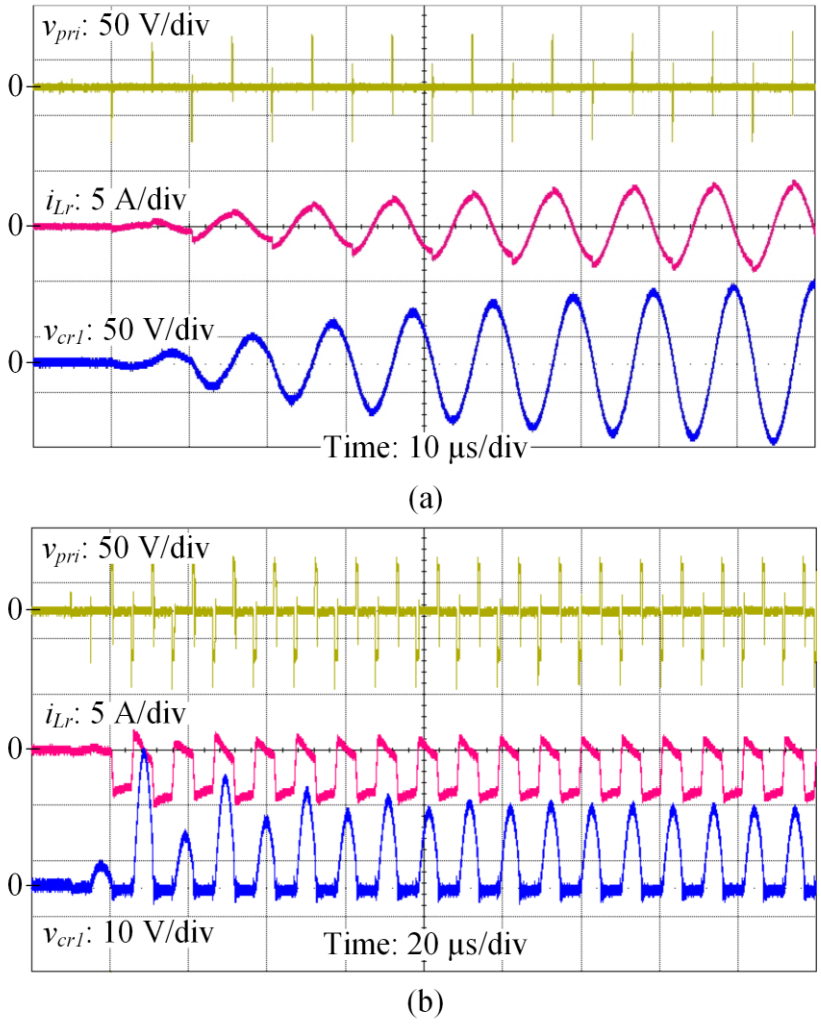


Figure 5.11. Experimental results of converter starting up with a short-circuited output (a) without the startup diode and $\Phi = 2.1°$ and (b) with the startup diode and $\Phi = 22°$.

that the soft start solution using the startup diode is less affected by component tolerances and therefore has a more predictable effect on the resonant tank.

Now the soft start algorithm will be applied to different capacitive loads on the microconverter. Φ_{max} was originally calculated to be 22°. During startup, Φ_{max} will be incrementally increased as the output voltage increases according to Table 5.1. The resonant inductor current, resonant capacitor voltage, and output voltage are shown in Figure 5.15 for startup with (a) just the 1.2 µF on-board output capacitor, (b) an external

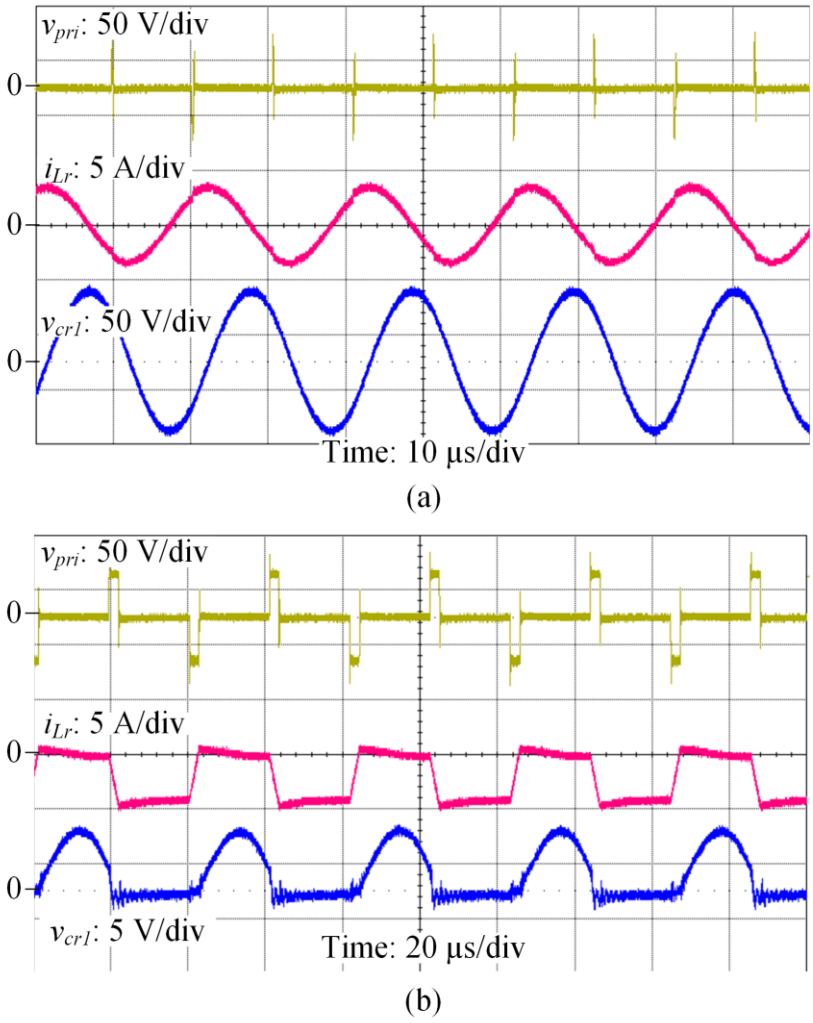


Figure 5.12. Experimental results of converter operating in steady-state with a short-circuited output (a) without the startup diode and $\Phi = 2.1°$ and (b) with the startup diode and $\Phi = 22°$.

4.7 mF capacitor, and (c) with a short circuit. For all three cases, the maximum inductor currents remain the same regardless of the output capacitance, including the short-circuit condition. Figure 5.15 (c) demonstrates that the converter is capable of operating with a short-circuited output so that if the converter were to start up with a short circuit, failure would not occur.

Table 5.1. Phase limits applied during startup.

V_o (V)	Φ_{max} (°)
$V_o < 150$	22
$150 < V_o < 300$	44
$300 < V_o < 350$	90
$350 < V_o$	180

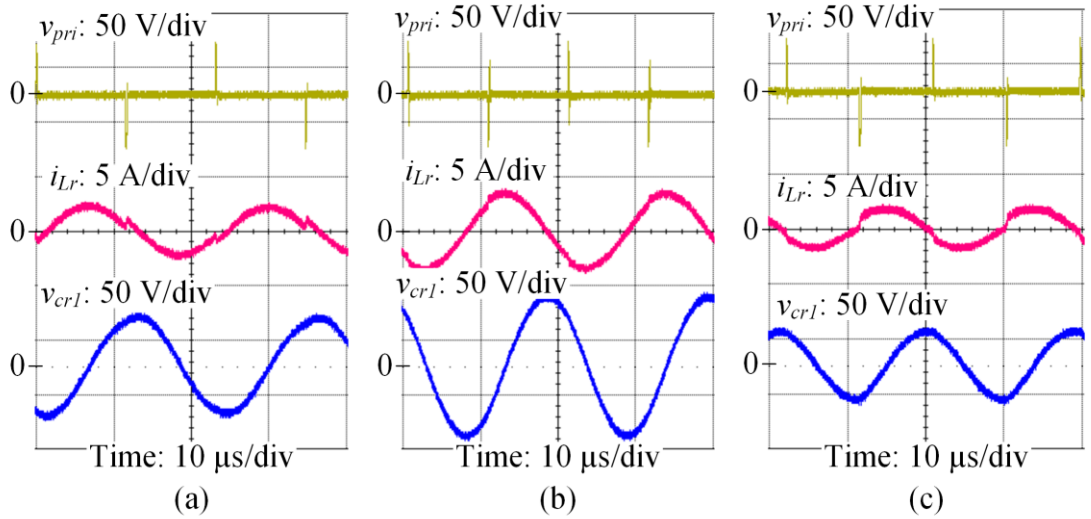


Figure 5.13. Experimental results of converter operating in steady-state with a short-circuited output without the startup diode and with (a) $F_s/F_r = 0.9$, (b) $F_s/F_r = 1.0$, and (c) $F_s/F_r = 1.1$.

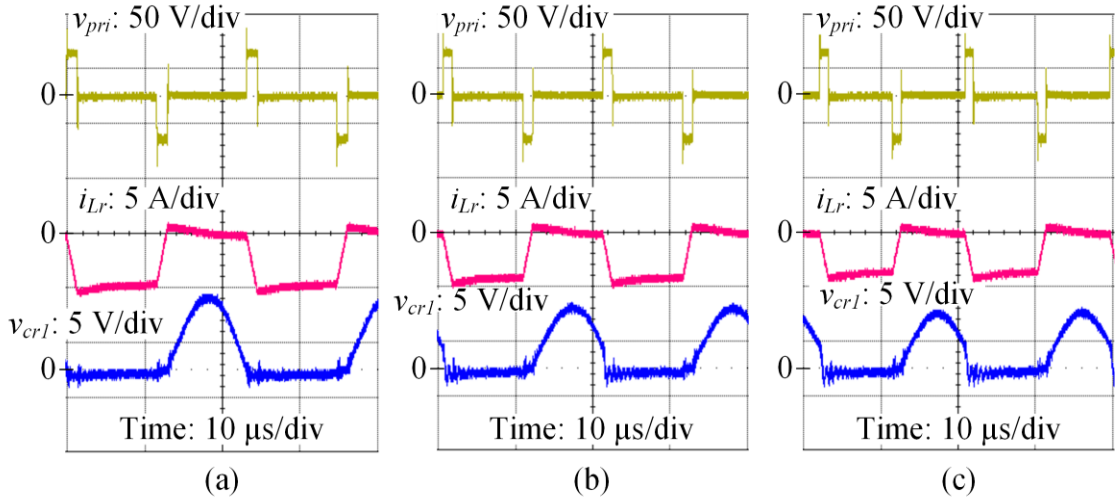


Figure 5.14. Experimental results of converter operating in steady-state with a short-circuited output with the startup diode and with (a) $F_s/F_r = 0.9$, (b) $F_s/F_r = 1.0$, and (c) $F_s/F_r = 1.1$.

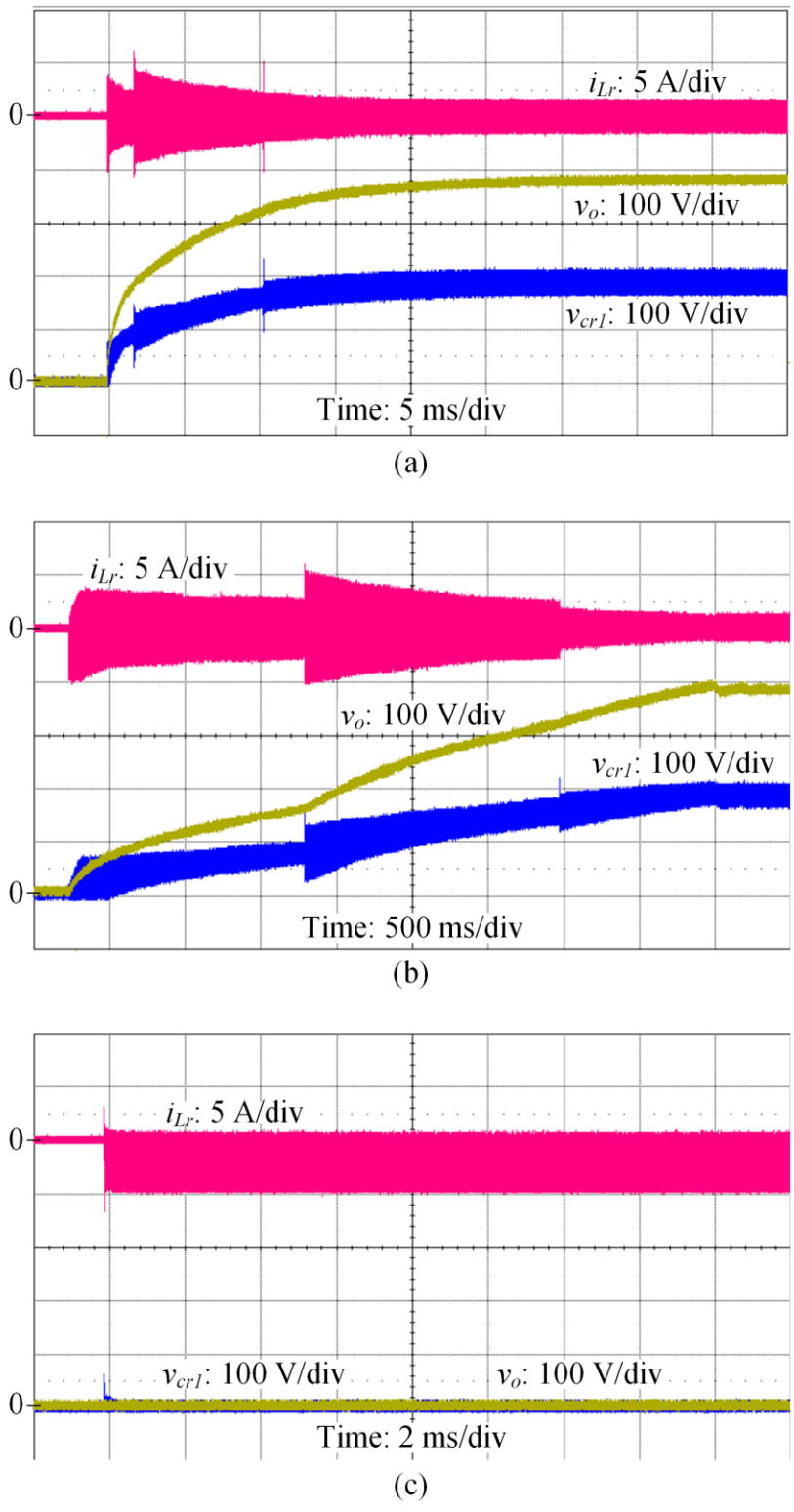


Figure 5.15. Experimental results of the converter starting up using proposed soft start method for (a) C_o = 1.2 µF, (b) C_o = 4.7 mF, and (c) output short circuit.

5.3 PV Module Power Optimization

In addition to soft start, two other important system-level integration issues that are imperative to microconverters operating in PV power conditioning systems are maximum power point tracking and double-line frequency ripple rejection. Both of these issues relate to optimizing the power output of PV modules. While these are both very important system issues, lots of research has been conducted and many solid solutions exist in both literature and commercial products. Rather than reinventing the wheel, both of these issues will only be discussed briefly and existing solutions will be implemented with the proposed microconverter. The aim of this section is to highlight the characteristics of the proposed converter which allow for the simple and straightforward implementation of existing solutions.

5.3.1 Maximum Power Point Tracking

Maximum power point tracking is a vital task of a PV power conditioning system due to the nonlinear output characteristics of PV modules that can change drastically with environmental conditions. As environmental conditions change, the PV module voltage that will result in the maximum power point will change. This is demonstrated in Figure 5.16 where the (a) I-V and (b) P-V curves are given for a module operating with two different solar irradiance levels and ambient temperatures.

There are many different methods of performing MPPT which appear in literature such as fractional open-circuit voltage [94], fractional short-circuit current [94], perturb and observe (P&O) [64, 65], curve-fitting of off-line models [95], look-up tables [95], incremental conductance [96, 97], and ripple correlation control [98]. There also are many

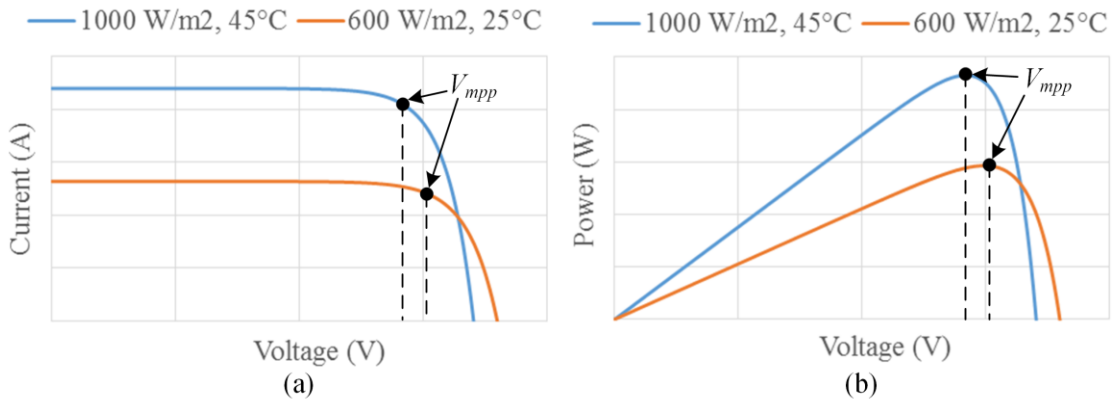


Figure 5.16. Comparison of (a) I-V and (b) P-V curves of a PV module operating under two different environment conditions.

variants of each of the aforementioned techniques. Most of these algorithms have one thing in common: they generate a voltage reference from either an on-line calculation, off-line calculation, or based on measured converter variables, and then they command this voltage reference to the voltage controllers of the power converter. While they all generate the voltage reference differently, they all can be viewed in a similar manner from the perspective of the converter and converter's control requirements: the converter needs to be able to accurately control whatever voltage reference the MPPT algorithm generates.

To demonstrate the compatibility of the proposed converter with MPPT algorithms, a simple P&O algorithm will be implemented. P&O is one of the simplest and most commonly used techniques as it doesn't require any prior knowledge of the PV module characteristics, the same algorithm can universally be applied to any PV module, and it involves very minimal on-line calculations so that it can be implemented with very little processor computation time. P&O algorithms work by perturbing the input voltage of the converter, measuring the resulting input power of the converter, and adjusting the input voltage reference accordingly. This is demonstrated Figure 5.17. When a step change in

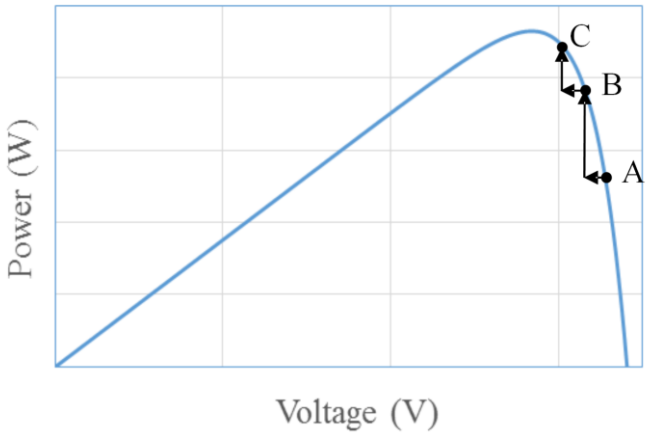


Figure 5.17. Basic operation of a simple P&O MPPT algorithm.

the input voltage reference results in a decrease in the input power, the direction of the step changes reverses.

A P&O algorithm was implemented in a prototype of the proposed converter and connected to a 240-W Canadian Solar CS6P-240P PV module with a rated MPP voltage of 29.9 V and MPP current of 8.03 A under full irradiance. The same BK Precision

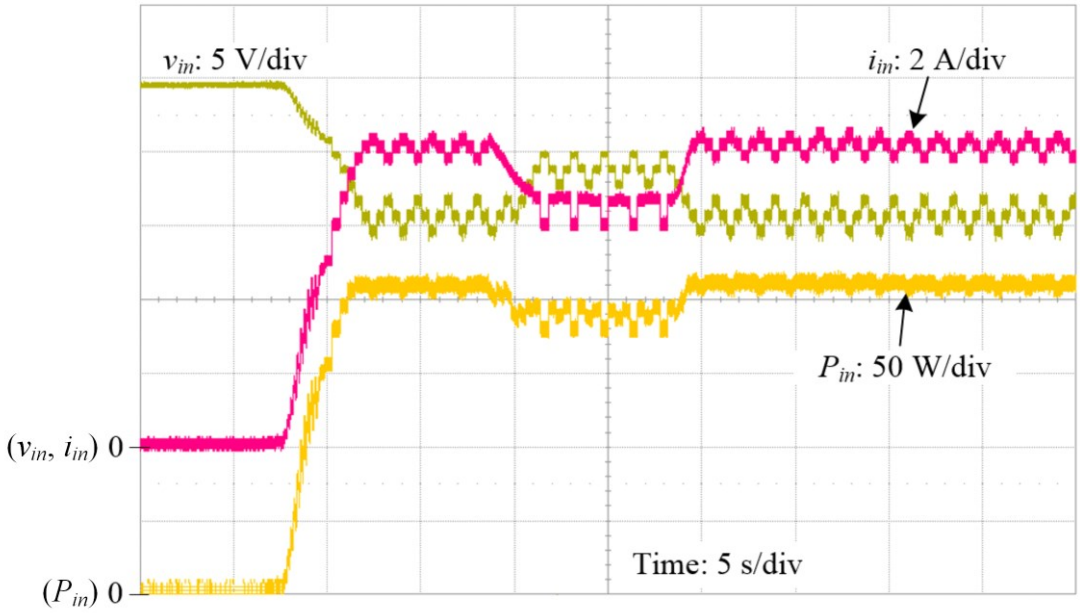


Figure 5.18. Microconverter input voltage, current, and power when connected to a PV module and operating with a simple P&O MPPT algorithm. The waveform shows startup, partial shading, and return to full sun conditions.

electronic load from previous sections was used to regulate the output of the microconverter to 380 V. The implemented P&O algorithm had a voltage step size of 1 V and a time step of 0.4 s in order for the operation of the algorithm to be clearly seen on the screen of the oscilloscope. Experimental waveforms during startup and an irradiance level change are shown in Figure 5.18. Here the irradiance level is changed by partially shading a portion of the module with a piece of cardboard and then removing it. The converter is able to quickly find and maintain the maximum power point within 10 step changes.

5.3.2 Double Line Frequency Ripple Rejection

A problem that ac power conditioning systems for PV applications face is compensating the double line frequency ripple so that it does not appear at the PV module's output terminals. This is true for any type of PCS that delivers an ac load whether it be a grid-tied or standalone inverter system. The double-line frequency ripple originates from the ac power characteristics of the output of the PCS. The equations for ac output voltage v_{ac}, output current i_{ac}, and instantaneous output power, p_o, are given in (5.9)-(5.11) where V_{max} and I_{max} are the peak output voltage and current, Φ is the angle of the power factor of the output, and ω is the angular frequency of the output.

$$v_{ac}(t) = V_{\max}\sin(\omega t) \tag{5.9}$$

$$i_{ac}(t) = I_{\max}\sin(\omega t + \phi) \tag{5.10}$$

$$p_o(t) = v_{ac}(t) \times i_{ac}(t) = \frac{V_{\max} I_{\max}}{2}\left(\cos(\phi) - \cos(2\omega t + \phi)\right) \tag{5.11}$$

(5.9)-(5.11) are plotted in Figure 5.19 for a 300-W, 240-V ac power conditioning system operating with unity power factor. It is obvious from (5.11) and the figure that the

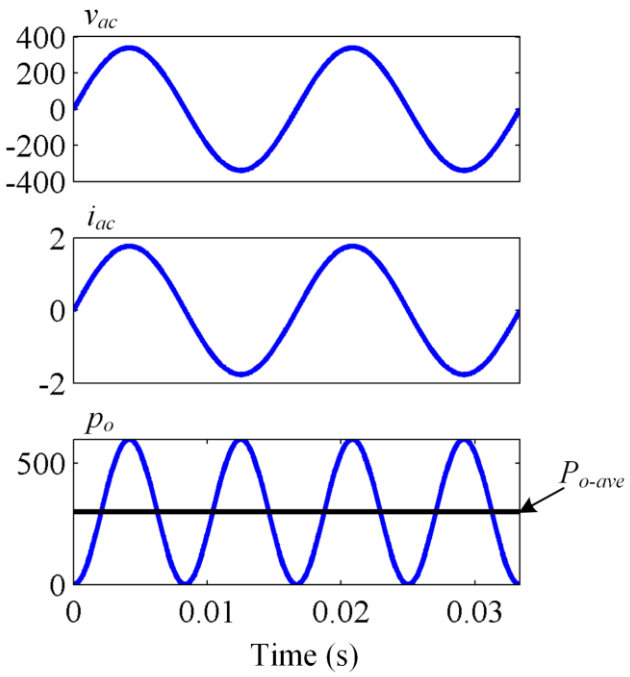


Figure 5.19. Voltage, current, and power output of a 60-Hz 300-W ac power conditioning system.

output power will have a dc term and an ac term with a frequency of twice the line frequency. In order to maximize the output power of the PV module, the power conditioning system needs to be able to supply this double-line-frequency power component without negatively impacting the dc input power. For a power conditioning system that consists of the proposed microconverter and an inverter, this ac power component will be supplied by the major energy storage capacitors in the system which are the dc bus capacitance, C_{bus}, or the input capacitance of the microconverter, C_{in}, which is

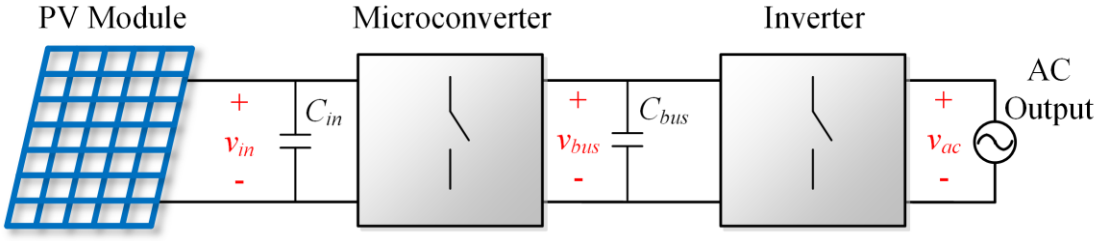


Figure 5.20. Block diagram of an ac power conditioning system and the major energy storage capacitors.

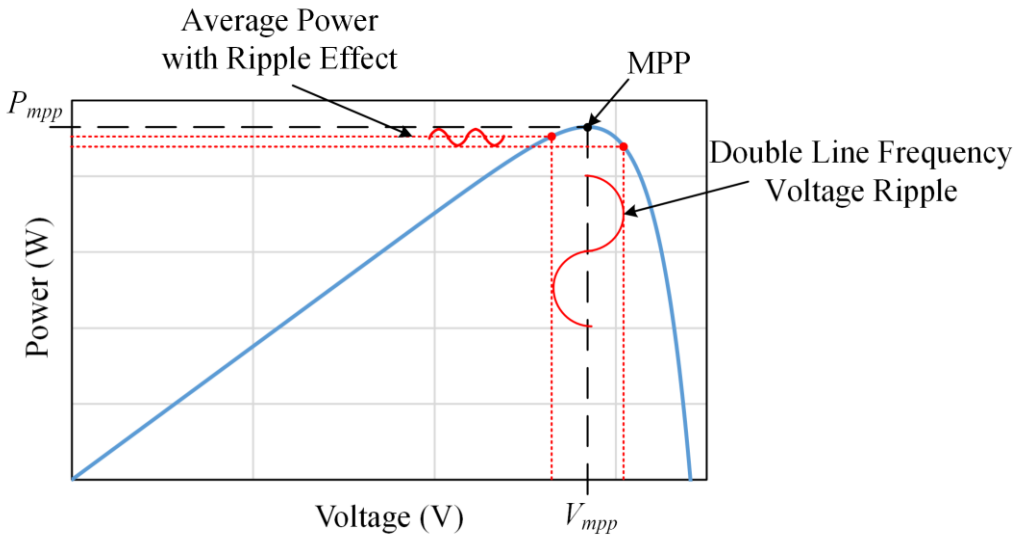


Figure 5.21. The P-V curve of a PV module showing how the double line frequency ripple effects the maximum power point.

shown as a block diagram in Figure 5.20. This results in a double-line-frequency voltage ripple across the capacitors which can have a detrimental effect to the maximum power point of the PV module. This is demonstrated in Figure 5.21 where the P-V curve for an arbitrary PV module is shown along with the maximum power point. In the figure, a voltage ripple is shown along with the resulting average module output power that is lower than the MPP.

In order to prevent this reduced output power and to keep the module operating as close to its MPP as possible, it is imperative to minimize the voltage ripple that appears at the input of the microconverter. The simplest way to reduce the input voltage ripple is to size the capacitors large enough to source the entire ac power component [99, 100]. The dc bus voltage (~380 V) is much larger than the microconverter input voltage (~30 V) so it is desirable to increase C_{bus} rather than C_{in}. This is because capacitor energy storage is related to CV^2, so storing the same amount of energy at a higher voltage would result in a much smaller capacitance. However, even for low power applications such as

microinverters, the C_{bus} requirement is still large enough to require the use of electrolytic capacitors which are known to be one of the most unreliable components in power converters [101]. Because of this, it is desirable to avoid the use of electrolytic capacitors for product reliability and longevity of lifetime purposes [102, 103].

Many different techniques have been proposed in order to minimize the input voltage ripple without the use of electrolytic capacitors such as adding additional passive filters [104, 105], adding additional active filter circuits [106-109], and simply just designing the converter's bandwidth high enough that the front-end converter can compensate for the double-line frequency ripple voltage present on a dc bus with a smaller capacitance [110-112]. The obvious disadvantage to adding either an active or passive filter is that it adds additional size and cost to the converter, and in the case of an active filter, additional control complexity. In [110], the author analyzes the ability of the microconverter's control system to reject the double line frequency ripple and provides a formula for calculating the minimum required gain of the controller's compensator at this frequency. In order to meet this required gain requirement, a high controller bandwidth is required. This could be difficult to achieve, especially in the case of the proposed microconverter where the model used to design the controller was simplified and is inaccurate at higher frequencies. Even with a more accurate plant model, this could still be difficult to guarantee for all units of the converter due to component tolerances between the different units. Implementing higher control bandwidths may also require the use of a more powerful and expensive digital controller capable of higher sampling frequencies [113].

Perhaps the simplest and most universal solution found in literature was proposed in [113] and [114]. In this work, the authors cascaded a quasi-resonant (QR) controller with the already existing voltage controller. This doesn't affect the operation of the existing voltage controller and only requires the addition of a couple of lines of code for implementation. For the proposed microconverter where a simple PI controller was used for voltage regulation, the structure of the controller becomes (5.12) where K_p and K_i are the proportional and integral gains, ω_{dlf} is the angular frequency of the double-line frequency, and Q_z and Q_p are quality factors used for determining the amount of gain that will be added at the double-line frequency.

$$G_c(s) = G_{PI}(s)G_{QR}(s) = \left(K_p + \frac{K_i}{s}\right)\left(\frac{1 + \frac{s}{Q_z\omega_{dlf}} + \frac{s^2}{\omega_{dlf}^2}}{1 + \frac{s}{Q_p\omega_{dlf}} + \frac{s^2}{\omega_{dlf}^2}}\right) \tag{5.12}$$

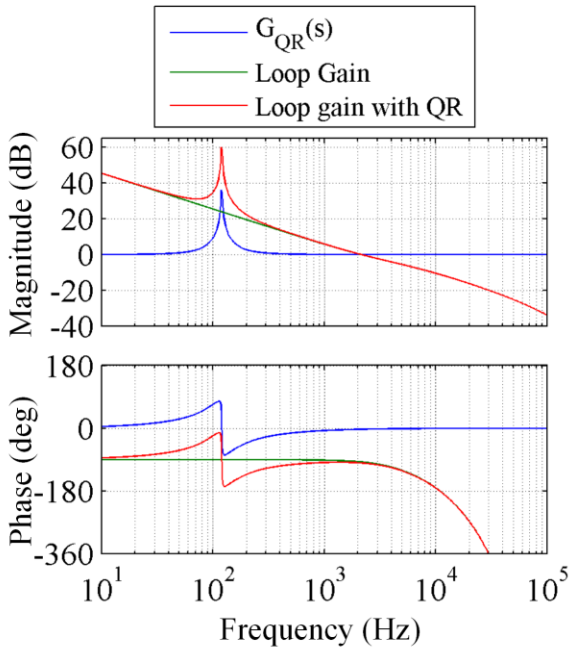


Figure 5.22. Bode plot of the QR controller, the previous converter loop gain, and the new loop gain with the QR controller.

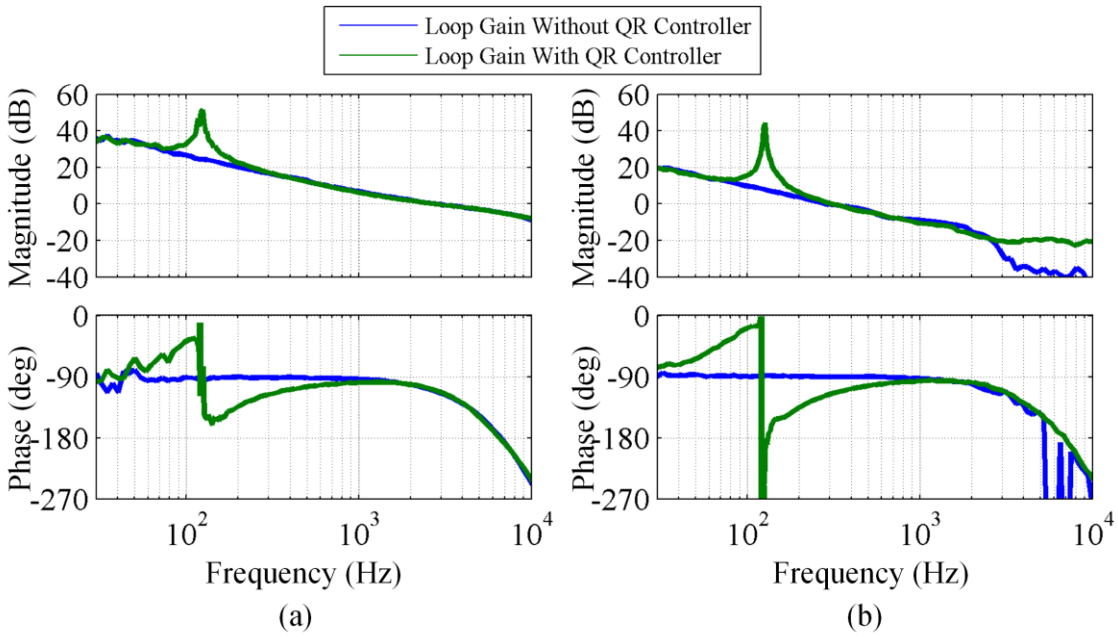


Figure 5.23. Measured loop gains of the converter with and with the QR controller implementation with the (a) 3-kHz PI controller and (b) 300-Hz PI controller.

A bode plot of the QR controller, the previous open-loop gain of the converter and PI controller operating in the Boost Mode, and the new open-loop gain with the addition of the QR controller are shown in Figure 5.22. In the figure the input voltage is 27 V, the output power is 225 W, and the double line frequency is 120 Hz. Without the QR controller, the 120-Hz gain was 35 dB and with the addition of the QR controller it becomes 60 dB without affecting the PI controller's bandwidth or phase margin.

To verify the double line frequency rejection method, the QR controller was added to the existing PI controller of the microconverter prototype. Two different PI controllers—one with a 3-kHz bandwidth and one with a 300-Hz bandwidth—were used to clearly demonstrate both the need for the QR controller and the effect of the QR controller. The loop-gains of the converter were measured experimentally using the Venable 350c FRA and are shown with and without the additional QR controllers in Figure 5.23 for the (a) 3-kHz bandwidth PI controller and (b) 300-Hz bandwidth PI controller.

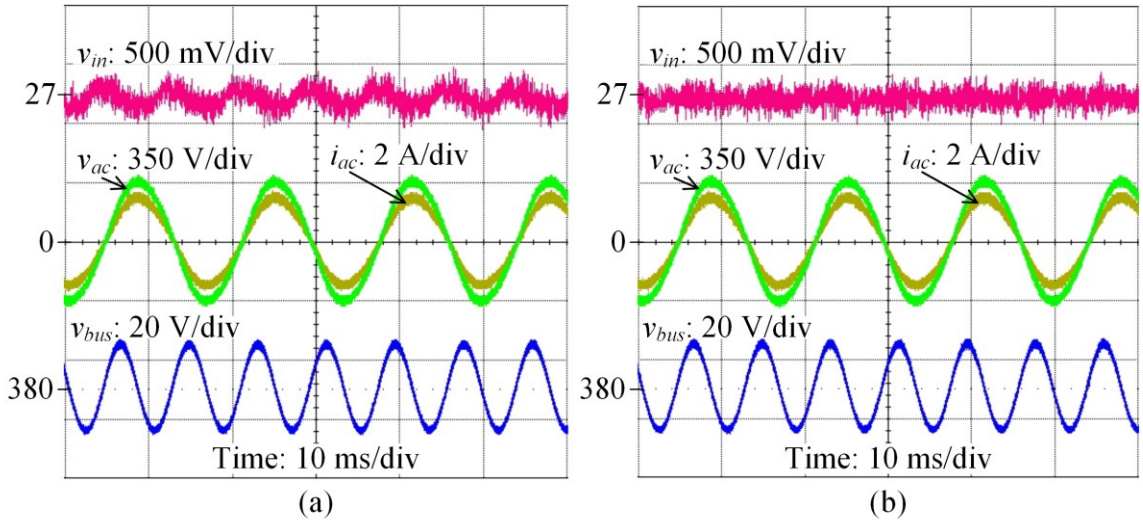


Figure 5.24. Steady-state waveforms of the microconverter operating with a 27-V input and a 225-W output (a) with a 3kHz PI controller and (b) with the combined PI and QR controllers.

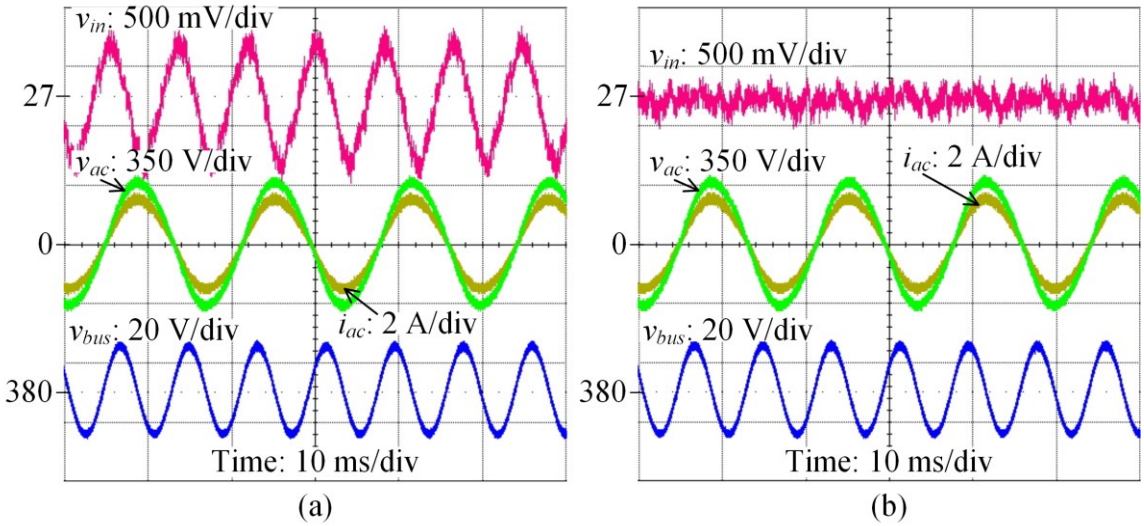


Figure 5.25. Steady-state waveforms of the microconverter operating with a 27-V input and a 225-W output (a) with a 300-Hz PI controller and (b) with the combined PI and QR controllers.

For both cases, the 120-Hz gain is increased between 25 and 35 dB while the controller bandwidths and phase margins remain the same.

The proposed microconverter is now connected to a single-phase inverter which delivers power with a unity power factor to a resistive load. The input source is connected

to the same dc power supply and series resistance from previous chapters. Steady-state operating waveforms of the ac output voltage and current, the dc-bus ripple voltage, and the input voltage ripple are shown in Figure 5.24 for the 3-kHz bandwidth controller and Figure 5.25 for the 300-Hz bandwidth controller. Without the addition of the QR controller, the 3-kHz bandwidth PI controller had a 120-Hz gain of ~25 dB while the 300-Hz bandwidth PI controller only had a 120-Hz gain of ~8 dB. This is evident from (a) in both figures. The 3-kHz bandwidth was already able to attenuate the double line frequency ripple fairly well without the QR controller. The QR controller, when added to the 3-kHz bandwidth system, reduced the ripple from ~0.25 V peak-to-peak to a ripple size that is negligible compared to the switching ripple of the converter. However, when added to the 300-Hz bandwidth system, the QR controller had a much greater effect. Here it reduce the ripple from ~1.2 V peak-to-peak to a ripple size that is negligible compared to the switching ripple of the converter.

5.4 Summary

The proposed microconverter is an excellent candidate for several different types of power conditioning systems so it is important that the converter is designed to universally handle all system-level issues it may face. Three important system-level integration issues that were discussed in this chapter were soft start, maximum power point tracking, and double line frequency ripple rejection. Soft start is very important whenever the converter is beginning operation with a large capacitive load that doesn't haven an initial charge. The proposed soft start method allows the converter to start up regardless of output capacitance with the addition of a single low-cost diode. This method clamps startup resonance in the resonant tank that is difficult to predict and can cause overvoltage

with catastrophic consequences. This diode clamp allows for larger startup phase angles resulting in faster startup times, and allows for the converter to safely start up in the case of a short-circuited output.

Two other system-level integration issues that were discussed were maximum power point tracking and double line frequency ripple rejection. Both of these deal with maximizing the output power of a PV module. A maximum power point tracking algorithm is imperative to all PV power conditioning systems because PV modules exhibit nonlinear output characteristics that change as environmental conditions change. An MPPT algorithm is required to ensure the module is always operating at its maximum power point. Double line frequency ripple rejection is important when the microconverter is used in any type of ac grid configuration. Due to the characteristics of ac power, a voltage ripple will appear at the input of the converter with a frequency equal to twice the grid frequency. It is important that the microconverter be able to attenuate this ripple so that the maximum power point of the PV module isn't effected. There are numerous excellent solutions to both of these issues in literature, so rather than reinvent the wheel, this chapter focused on giving an overview of the issues and implementing existing solutions experimentally to show their effectiveness with the proposed converter. The proposed converter's simple control structure allowed for the easy and successful implementation of both a maximum power point tracking algorithm and a double line frequency rejection algorithm.

Chapter 6

Efficiency Improvements

6.1 External Resonant Inductor

The design procedure in Chapter 3 stated the resonant inductor could either be integrated into the isolation transformer or could be implemented with an external resonant inductor. The converter was originally designed with integrated magnetics, as was presented in the experimental results sections of Chapters 3 – 5, with the aim of reducing size and cost. This section, however, explores the effect leakage inductance indirectly has on ac resistance and transformer conduction losses. Experimental results are provided comparing two different converter designs: one with integrated magnetics and one with an external resonant inductor.

6.1.1 Transformer Leakage Inductance and Proximity Losses

With the proper winding configuration, it is possible to wind the isolation transformer so that the leakage inductance is large enough to also be used as the resonant inductor. This method of using integrated magnetics is highly beneficial due to the reduction in number of components, associated costs, and size of the printed circuit board (PCB). This does, however, come at the cost of an increased ac resistance of the transformer windings resulting in higher conduction losses. In order to understand the

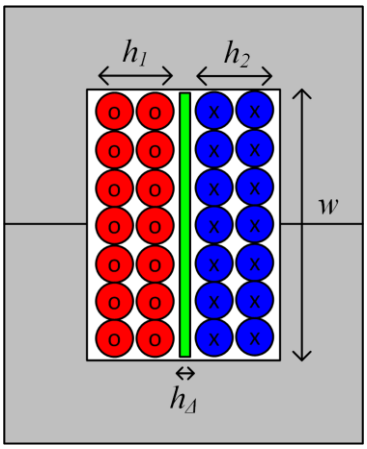


Figure 6.1. Basic winding structure of a transformer wound on an E core.

cause of this, first it is essential to analyze the winding configuration of integrated magnetics.

In order to implement integrated magnetics, a winding configuration must be used that will result in a higher leakage inductance [115, 116]. Figure 6.1 shows one half on an E core with a standard winding technique. Here the primary winding, shown in red, is first wound around the center of the E core. Next a thin layer of insulation, shown in green, is used to isolate the primary and secondary winding. Finally, the secondary winding, shown in blue, is wound on top of the insulation layer. In the figure, h_1 is the height of the primary winding area, h_2 is the height of the secondary winding area, h_Δ is the height of the insulation layer, and w is the width of the winding area. N_s is the number of turns of the secondary winding since we are concerned with the leakage inductance as seen from the secondary side, μ_0 is the permeability of free space, and MLT is the mean length of each turn. Several works have been published on analyzing the leakage inductance for transformers [117-119], and from these works the leakage inductance of this basic winding structure can be calculated as:

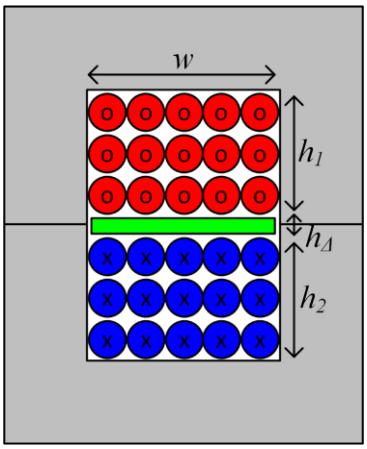


Figure 6.2. Split-bobbin winding structure of a transformer on an E core which results in a large leakage inductance.

$$L_{lk} = \frac{\mu_0 N_s^2 MLT}{w}\left(h_\Delta + \frac{h_1 + h_2}{3}\right) \tag{6.1}$$

It is obvious from (6.1) that in order to increase the leakage inductance without increasing the number of turns, the width of the windings can be decreased, the height of the winding areas can be increased, and the insulation thickness between the layers can be increased. This can be accomplished through the winding configuration shown in Figure 6.2 where the top half of the bobbin area is used for the primary winding and the bottom half is used for the secondary winding. This is the configuration that was used for constructing the isolation transformer designed in Chapter 3.

While this winding configuration results in a high leakage inductance which makes magnetic integration possible, it suffers from high proximity effect losses. The proximity effect is a phenomenon that occurs when two conductors carrying time-varying currents are in close proximity to each other. The current flowing in one of the conductors produces a flux in the space between the conductors. This flux in turn induces a current flowing in the opposite direction in the other conductor [54, 120, 121]. As a result, localized current

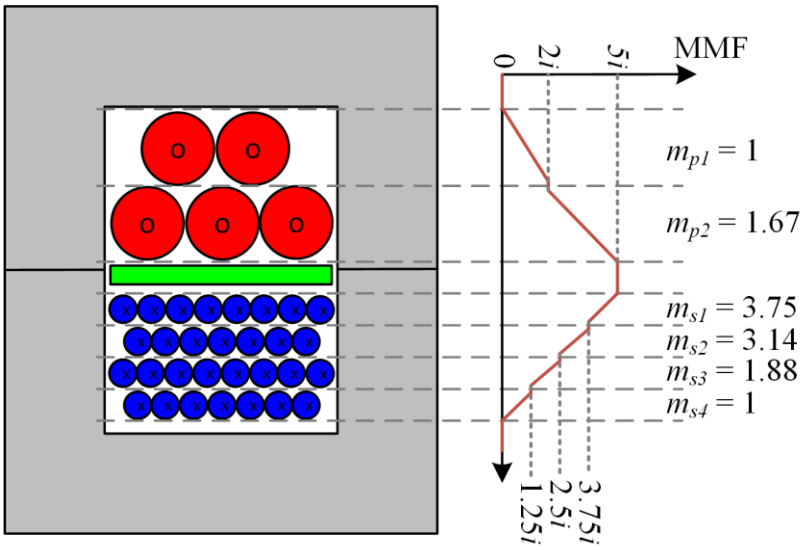


Figure 6.3. Winding structure and MMF diagram of a transformed designed to have a large leakage inductance.

loops form between the conductors. This proximity effect increases with frequency and increases the effective resistance of the windings.

In order to better understand the proximity effect and its effect on winding resistance, it is beneficial to analyze the magnetomotive force (MMF), F, present in the winding area. As an example, let us consider a transformer with a turns ratio of 6. The primary winding consists of 5 turns, the secondary winding consists of 30 turns, and the winding structure is designed to provide maximum leakage inductance. This winding structure, along with the MMF diagram is shown in Figure 6.3. The primary winding, shown in red, is carrying a time-varying current, i. The total MMF of the secondary will cancel the total MMF of the primary, resulting in an overall field intensity of zero [122]. This means that the MMF at either side of the winding area will be zero. The MMF generated by each layer is equal to the number of turns times the amount of current in each turn, and the MMF forces generated by each layer add to that of the previous layer as can be seen in the MMF diagram in Figure 6.3. The MMF force generated by each layer will

affect the adjacent layers. The factor, m, describes how much each layer is effected by the adjacent layers and is defined as the ratio of the peak MMF present in the space of each layer, F_{pk}, to the change in MMF across the space of each layer, $F(0) - F(h)$ where h is the total height of each layer [54, 123]. The calculation for determining m for each layer is given in (6.2).

$$m_{xj} = \frac{\max\left(\left|F(0)\right|, \left|F(h)\right|\right)}{\left|F(h) - F(0)\right|} \tag{6.2}$$

In (6.2) the subscript x defines which winding the layer is part of (in this case it is p for the primary winding or s for the secondary winding) and j defines which layer of that winding the calculation is for. Once m is calculated for each layer, the increase in winding resistance caused by the proximity effect can be determined by applying Dowell's formula to each layer of each winding, and averaging the results for each winding [122, 124].

$$\frac{R_{ac-x}}{R_{dc-x}} = \frac{1}{M_x} \sum_{j=1}^{M_x} \frac{\xi}{2} \left(\frac{\sinh\xi + \sin\xi}{\cosh\xi - \cos\xi} + \left(2m_{xj} - 1\right)^2 \frac{\sinh\xi - \sin\xi}{\cosh\xi + \cos\xi} \right) \tag{6.3}$$

Here R_{dc} is the dc resistance of the winding, R_{ac} is the frequency-dependent resistance of the winding taking into consideration the proximity effect, M_x is the total number of layers for winding x, and ξ is the ratio of the diameter, d, of the conductor to the skin depth, δ, of the conductor at a given switching frequency. ξ for a single cylindrical conductor is given in (6.4), but the formula for calculating ξ will may depending on the type of wire used [125-128].

$$\xi = \frac{\sqrt{\pi}}{2} \frac{d}{\delta} \tag{6.4}$$

Now consider the case where an external resonant inductor will be used so the transformer no longer needs to be designed to have a large leakage inductance. The

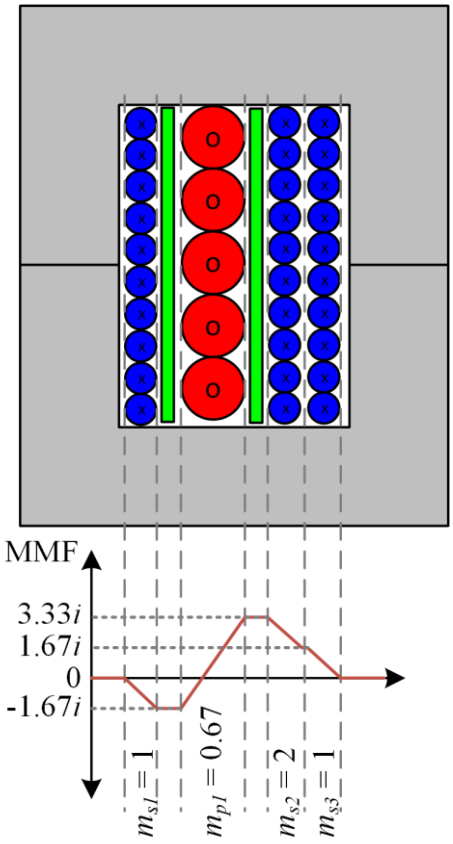


Figure 6.4. Winding structure and MMF diagram of a transformed designed to have a small leakage inductance.

transformer will have the same number of turns and turns ratio, but will be constructed using a different winding configuraiton. It is well documented that interleaving the primary and secondary windings of the transformer will reduce proximity losses [54-56, 119, 122, 129], so the transformer will be wound with the configuration shown in Figure 6.4. The MMF diagram and m for each layer are also given in the figure. It can be seen here that both the peak MMF and m for each layer are reduced with this winding configuration. The increase in ac resistance is now calculated for both transformer designs based on (6.3) and is plotted in Figure 6.5 versus ξ. Here Design A is the winding configuration in Figure 6.3 and Design B is the winding configuration in Figure 6.4. ξ depends on the type of wire used and the frequency components of the current waveform in the converter. As the

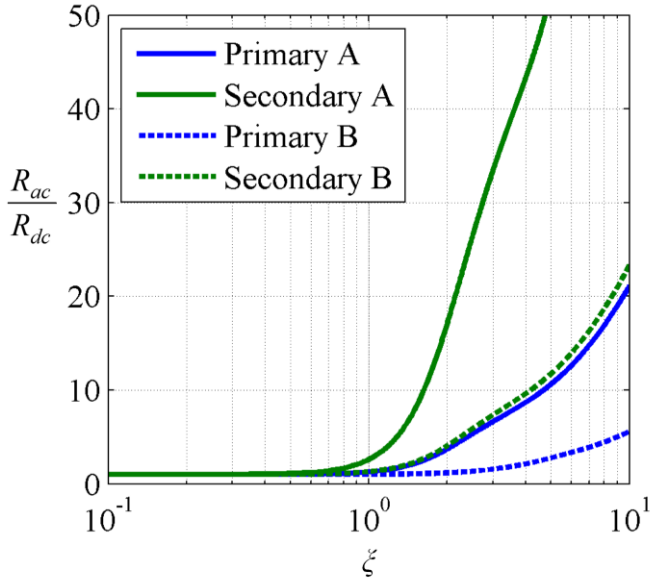


Figure 6.5. Comparison of primary and secondary winding R_{ac}/R_{dc} values for two different winding structures.

converter operating point moves away from the series resonant point, the harmonic contents in the current waveform increase creating a higher effective ac resistance. It can be seen from Figure 6.5 that interleaving the windings greatly reduces this ac resistance, especially at higher operating frequencies.

6.1.2 Resonant Inductor Design

Once the isolation transformer is designed, an external resonant inductor needs to be designed that is equal to the desired L_r value minus the leakage of the transformer. This inductor design is very straight forward and can be done using any of the conventional ac inductor design procedures [54-56]. Using these design procedures, the core size, shape, and material can be selected using a similar core geometry factor as the transformer design procedure. Once again, it is important to select a material with a flat temperature curve

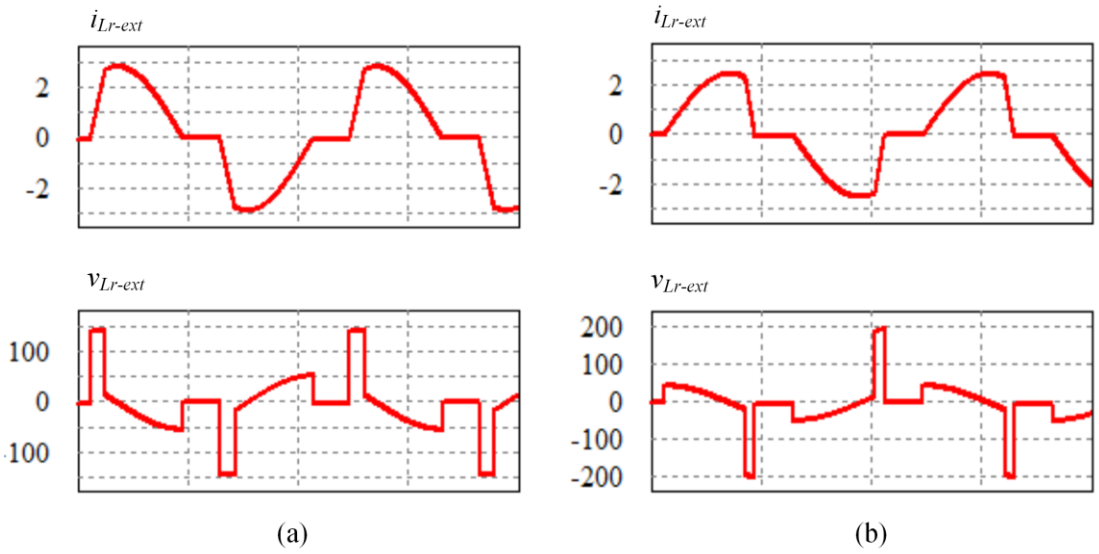


Figure 6.6. External resonant inductor voltage and current waveforms for (a) Buck Mode with 33-V input and 225W output and (b) Boost Mode with 27-V input and 225-W output.

since the ambient temperature on a rooftop can vary tremendously based on geographic location and season.

Once the core size, shape, and material are selected, the number of turns is selected based on a trade-off between core and conduction losses, similar to the design procedure of the isolation transformer. In order to calculate the conduction losses, the current equations in (3.10)-(3.12) can be used where L_r is the sum of both the transformer leakage inductance L_{lk} and the external resonant inductance $L_{r\text{-}ext}$. In order to calculate the flux density and core loss, the volt-seconds (V·s) across the external resonant inductor over one half switching cycle needs to be calculated. For the isolation transformer, the V·s product was simple because V_{in} is applied across the primary winding. When calculating the V·s product for the resonant inductor, however, the voltage waveform is not so straightforward. The voltage and current waveforms for the inductor are shown in Figure 6.6 for (a) Buck Mode and (b) Boost Mode. In order to determine the V·s product, the absolute value of

the inductor voltage must be integrated over one half of the switching cycle. For simplification, this can be approximated as a sine wave and the V·s product is obtained in (6.5) for Buck Mode and (6.6) for Boost Mode.

$$(V \cdot s)_{buck} = \frac{r_1}{\omega}\left(1+\cos\left(\omega\frac{T_s}{2}-\pi\right)\right) \tag{6.5}$$

$$(V \cdot s)_{boost} = \frac{r}{\omega}\left(1+\cos\left(\omega\frac{T_s}{2}-\pi\right)\right) \tag{6.6}$$

Now that the V·s product is known, the core losses can be solved using (3.13) and the number of turns can be selected based on a tradeoff between core and conduction loss similar to the transformer design method previously discussed. Once the number of turns is chosen, the air gap, l_g, needs to be determined which will result in the proper inductance. This formula is shown in (6.7) where N is the number of turns and A_c is the cross-sectional area of the core.

$$l_g = \frac{\mu_0 A_c N^2}{L_{r-ext}} \tag{6.7}$$

6.1.3 Experimental Results

A new prototype of the proposed microconverter was designed and implemented using an external resonant inductor. A photograph of the prototype is shown in Figure 6.7. The converter specifications are identical to those listed in Table 3.1. The isolation transformer has the same parameters as previously outlined in Table 3.3, except the winding configuration is interleaved resulting in a smaller leakage inductance. A summary

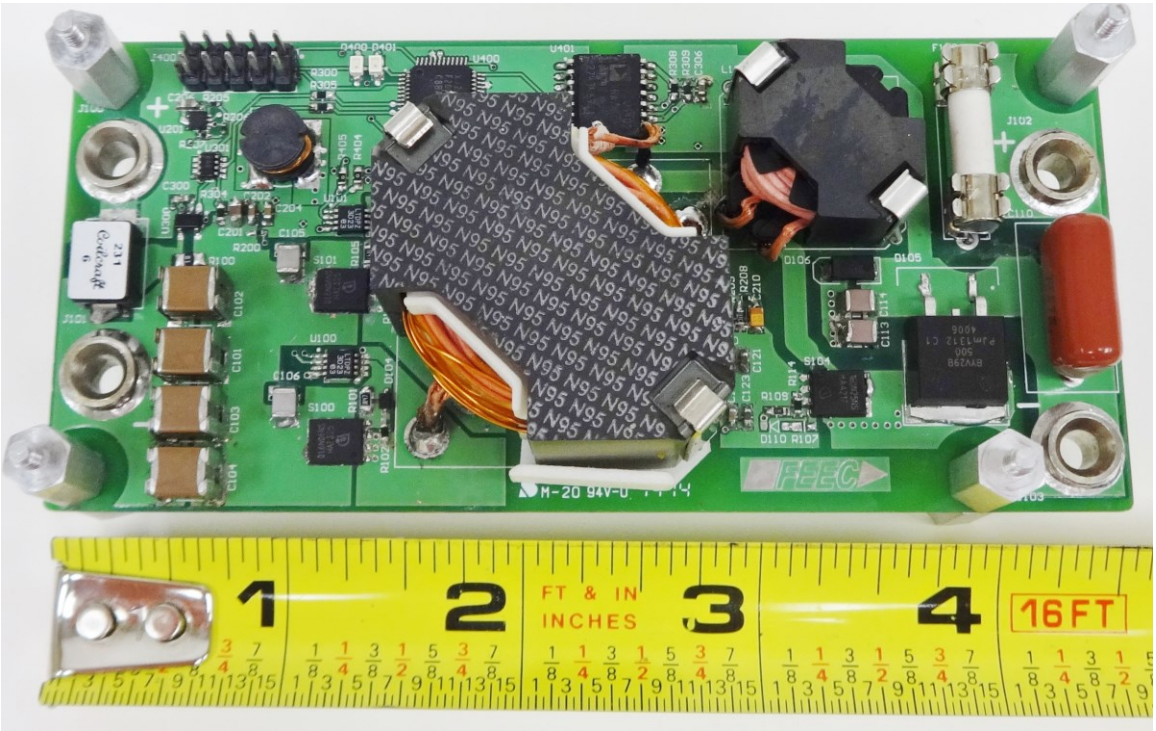


Figure 6.7. Photograph of developed 300-W prototype with an external resonant inductor.

of the external resonant inductor specifications and the new resonant tank is given in Table 6.1.

With the external leakage inductance, the efficiency under all operating conditions was increased due to the reduced R_{ac}/R_{dc} of the isolation transformer. Weighted CEC

Table 6.1. External resonant inductor and resonant tank specifications.

Parameter	Value
Inductor Core Shape	RM8/ILP
Inductor Core Material	Ferroxcube 3C95
Inductor Winding	12 turns, 22 AWG (160/44 Litz)
DC Resistance, R_{Lr}	53 mΩ
Inductance, $L_{r\text{-}ext}$	35.5 µH
Transformer Leakage, L_{lk}	6.7 µH
Total Resonant Inductance, L_r	42.2 µH
Resonant Capacitance, C_r	44 nF
Resonant Frequency, F_r	82.4 kHz

efficiencies versus input voltages for both Design A and Design B are shown in Figure 6.8. Clearly, Design B with the external leakage inductance has better performance with regard to converter efficiency, but the tradeoff is a larger prototype with more components, resulting in higher costs. Table 6.2 shows a comparison of CEC efficiency, size, weight, and bill of material (BOM) cost at 1000 unit pricing between the two converters.

Table 6.2. Efficiency, size, and cost comparison between Design A and Design B.

Parameter	**Design A**	**Design B**
CEC Efficiency	97.7%	98.0%
Volume	160.6 cm^3	172.2 cm^3
Weight	114 g	130 g
BOM Cost (1k)	$48.12	$48.97

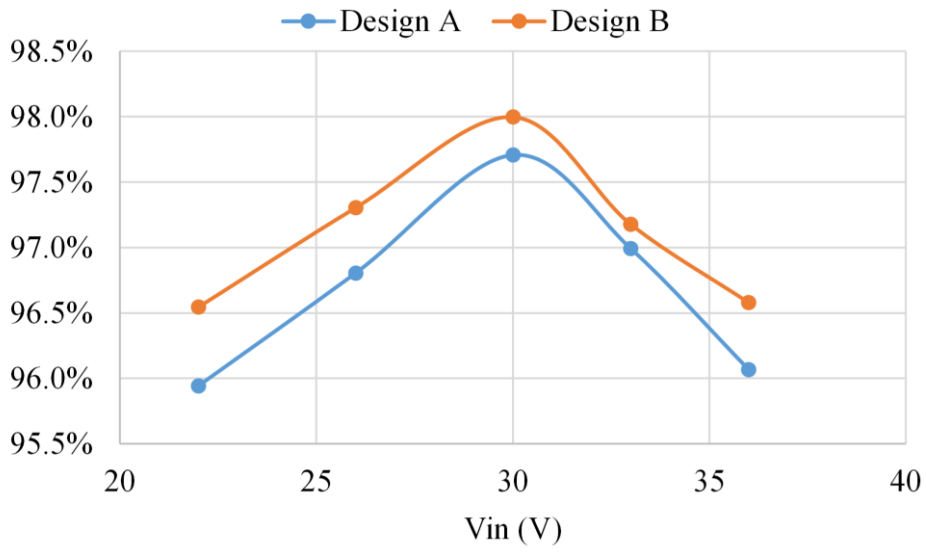


Figure 6.8. Comparison of CEC efficiency between Design A with integrated magnetics and Design B with an external resonant inductor.

6.2 Variable Frequency Optimization

6.2.1 Introduction

Fixed frequency operation is very attractive in power converters because it makes modeling, control, design of power stage components, and implementation of control simpler [54, 68]. The control techniques and analysis presented so far have all been based on simple, fixed-frequency operation. While fixed-frequency operation has its numerous benefits, there is the potential for efficiency improvement by varying the switching frequency. As was discussed in Chapter 2, there is a DCM period in both Buck and Boost Modes after the resonant inductor current reaches zero. The further away from the nominal input voltage the converter operates, the longer this DCM period will be. If the switching frequency is increased to remove this DCM period, the rms currents throughout the converter will decrease, in turn decreasing conduction losses. When the DCM period is minimized, the converter is operating at the boundary between DCM and CCM, known as the Boundary Conduction Mode (BCM). There have been countless works published on

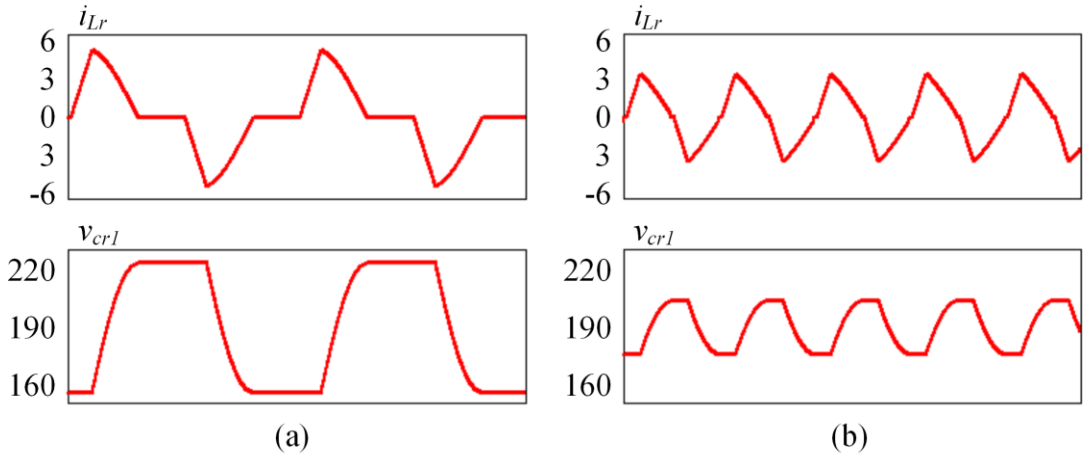


Figure 6.9. Simulation of resonant inductor current and resonant capacitor voltage with a 22-V input and 225-W output and a switching frequency of (a) 100 kHz operating in the DCM and (b) 240 kHz operating in the BCM.

the merits of varying the switching frequency in order to maintain BCM operation [130-133]. BCM is very attractive because it maintains the soft-switching and simplified control benefits of DCM, but has reduced current stresses throughout the converter. Figure 6.9 shows a comparison of (a) the normal fixed-frequency DCM operation and (b) BCM operation of the proposed converter operating with a 22-V input and 225-W output. By increasing the switching frequency, the DCM period is eliminated and the peak and rms inductor currents are reduced along with the voltage ripple across the resonant capacitors.

Among the disadvantages of operating in BCM in order to decrease rms currents and conduction losses, however, are the gate driver and MOSFET switching losses associated with an increase in switching frequency. These losses are especially dominant in the lower power range. In [134] and [135], hybrid control methods are introduced that transition between fixed-frequency DCM and BCM operation to account for the switching losses at light load. These methods increase the power conversion efficiency of the converter, but require separate fixed-frequency and variable-frequency modeling and control techniques. For DCM operation, the converter needs to be modeled and controllers designed based on duty cycle control and in BCM the same needs to be done for variable frequency control.

In order to maintain simple modeling, controller design, and control implementation, a variable frequency algorithm is now introduced in order to optimize the efficiency of the converter for all input voltage and output load ranges. Rather than using variable frequency for control, the frequency will be changed in an open-loop manner at a rate very slow relative to the voltage controllers so as to not affect the operation of the fixed-frequency voltage controllers.

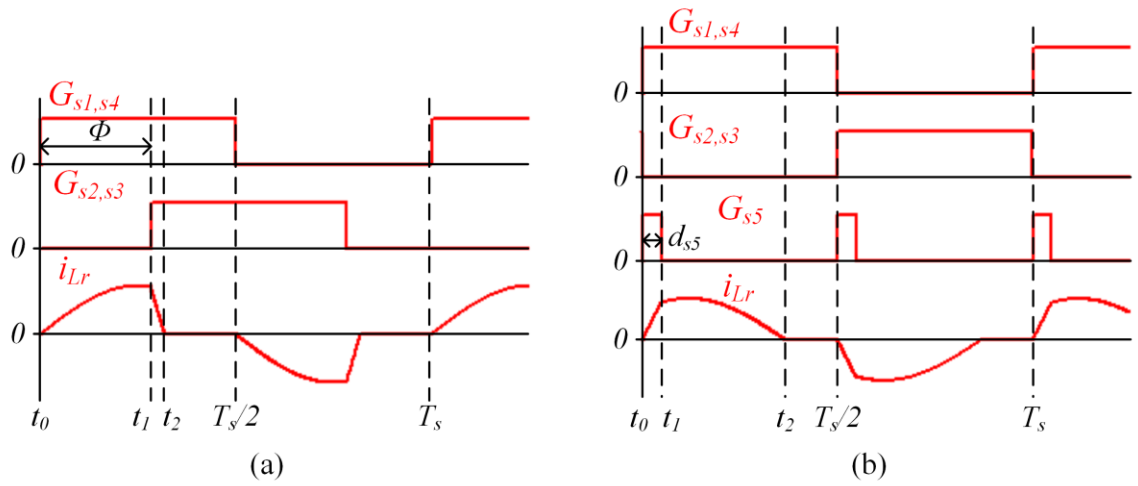


Figure 6.10. Gating signals and resonant inductor current of converter operating in (a) Buck Mode and (b) Boost Mode.

6.2.2 Algorithm

A variable frequency algorithm will now be developed in order to optimize the efficiency of the converter for all input voltage and output power operating conditions. The proposed variable frequency alrogithm will update the switching frequency when the input voltage reference is updated by the MPPT algorithm so as to not inerfere with the fixed-frequency voltage controllers. The bandwitdth of the MPPT algorithm is much slower [72] than the bandwidth of the voltage controllers, so each time the switching frequency changes the fixed-frequency voltage controllers have ample time to reach steady state.

The first step in developing the algorithm is to set an upper limit for the switching frequency so that the converter does not enter CCM. It is important to not operate in the CCM so that ZCS is maintained of the output diodes and primary-side MOSFETs. The upper limit will be the BCM frequency. BCM occurs when one half of the switching period is equal to $t_2 - t_0$, as shown in Figure 6.10 for (a) Buck Mode and (b) Boost Mode. Based

on the analysis in Chapter 2, the cacluations for determining the BCM frequency are given in (6.8) and (6.9) for Buck Mode and Boost Mode, respectively.

$$T_{s-BCM-buck} = 2\left(\frac{\phi}{360} T_s + \frac{nV_{in} - \frac{V_o}{2} + \frac{P_o T_s}{4V_o C_r}}{\omega\left(\frac{V_o}{2} + \frac{P_o T_s}{4V_o C_r} \right)} \sin\left(\omega \frac{\phi}{360} T_s \right) \right) \tag{6.8}$$

$$T_{s-BCM-boost} = 2d_{s5} T_s + 2\frac{\cos^{-1}\left(\frac{\frac{V_o}{2} - nV_{in} - \frac{P_o T_s}{4V_o C_r}}{\frac{V_o}{2} - nV_{in} + \frac{P_o T_s}{4V_o C_r}} \right)}{\omega} \tag{6.9}$$

These equations are non-linear and would be very difficult to compute online with a low cost fixed-point DSP, so it is possible for these values to be calculated offline and stored in a look-up table (LUT) for low-cost implementation. Accessing the LUT to extract the switching frequency takes very little computation time, and with computational math software such as Matlab, generating the LUT is quite simple. For light loads the calculated BCM frequency will be high, so it is also important to set an upper limit for the BCM based on the maximum frequency the DSP or analog control IC can operate.

Now that the upper limit has been set for the variable frequency algorithm by calculating the BCM frequency for all operating conditions, the switching frequency that will result in the minimum power losses for each operating condition will be calculated. From the loss analysis in Chapter 3, all of the loss equations that are switching frequency dependent are used. This includes MOSFET switching and conduction losses (including gate driver losses), diode conduction loss, and transformer core and conduction losses. For each operating condition, these losses are now calculated and summed together for a range of switching frequencies to determine which one will result in the minimum power losses.

This can either be calculated on-line by the digital controller or can be solved off-line through iterative loops in computational math software and stored in a look-up table. The BCM frequencies and minimum power loss (MPL) frequencies for the prototype converter in Section 6.1 are plotted for different input voltages and power levels in Figure 6.11 for Buck Mode and in Figure 6.12 Boost Mode. As can be seen in the figure, for higher output powers where conduction losses are dominant, the MPL frequency is equal to the BCM frequency. The MPL frequencies are generally lower in Buck Mode than in Boost Mode because the switching losses of the primary-side MOSFETs are much greater because one switching leg loses ZVS and the other loses ZCS.

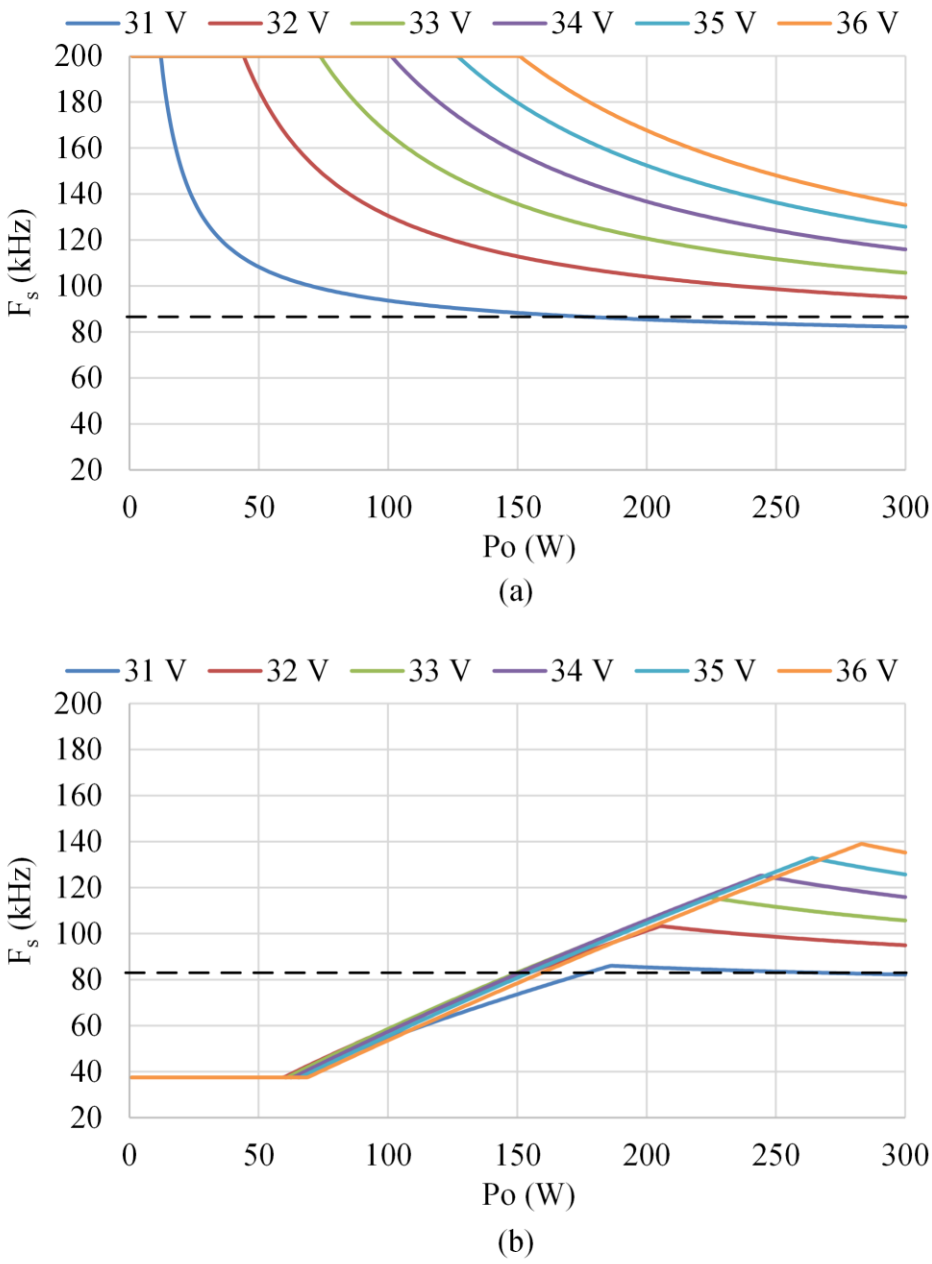


Figure 6.11. (a) BCM and (b) MPL switching frequencies for Buck Mode plotted for different input voltages.

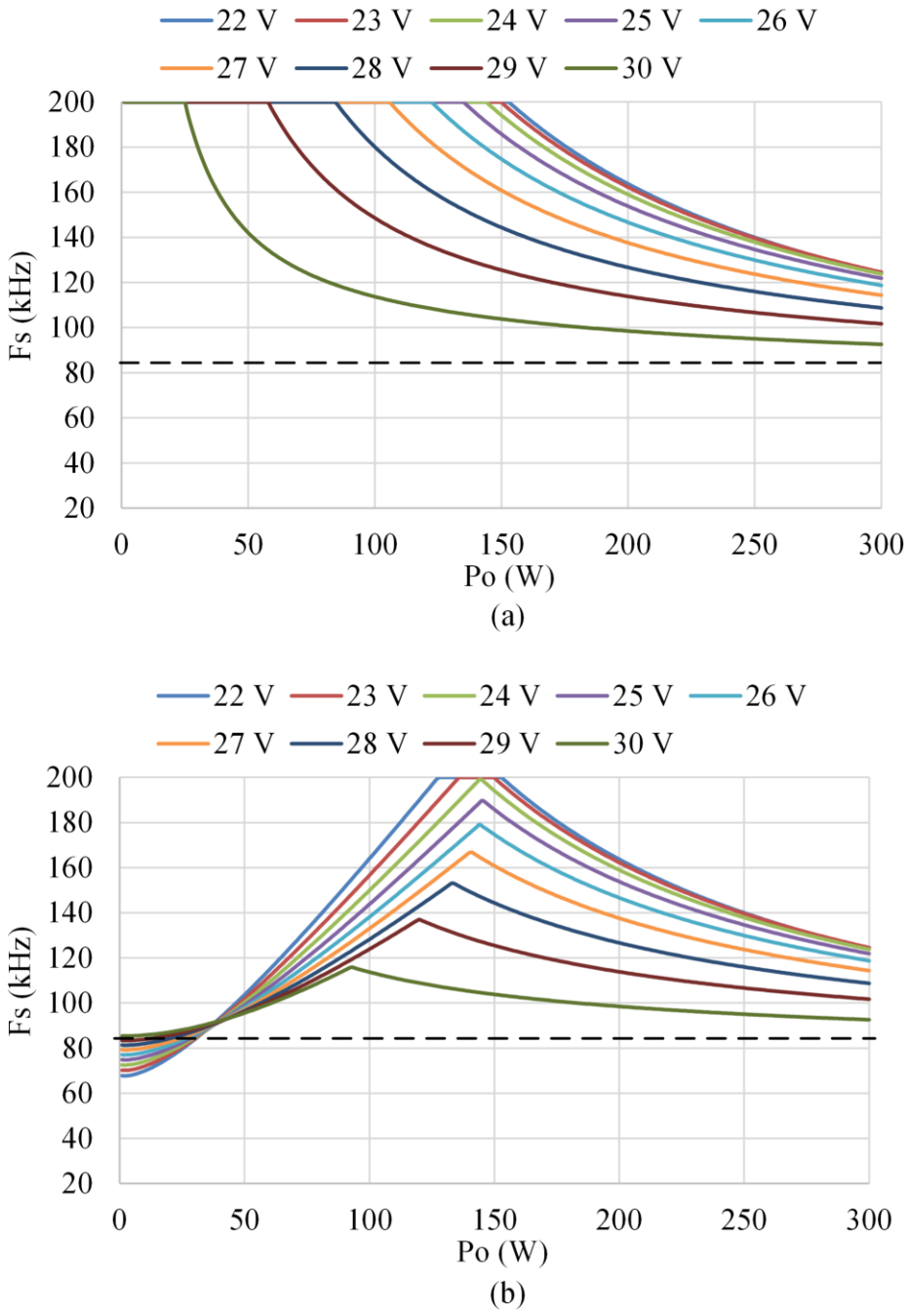


Figure 6.12. (a) BCM and (b) MPL switching frequencies for Boost Mode plotted for different input voltages.

6.2.3 Experimental Results

To verify the proposed variable frequency algorithm, the MPL switching frequencies in Figure 6.11 (b) and Figure 6.12 (b) are implemented as LUTs in the digital controller of the prototype from Section 6.1. Steady-state operating waveforms of the converter are shown for Buck Mode in Figure 6.13 and Boost Mode in Figure 6.14 for both the fixed-frequency DCM operation and (b) the MPL variable frequency operation. Buck

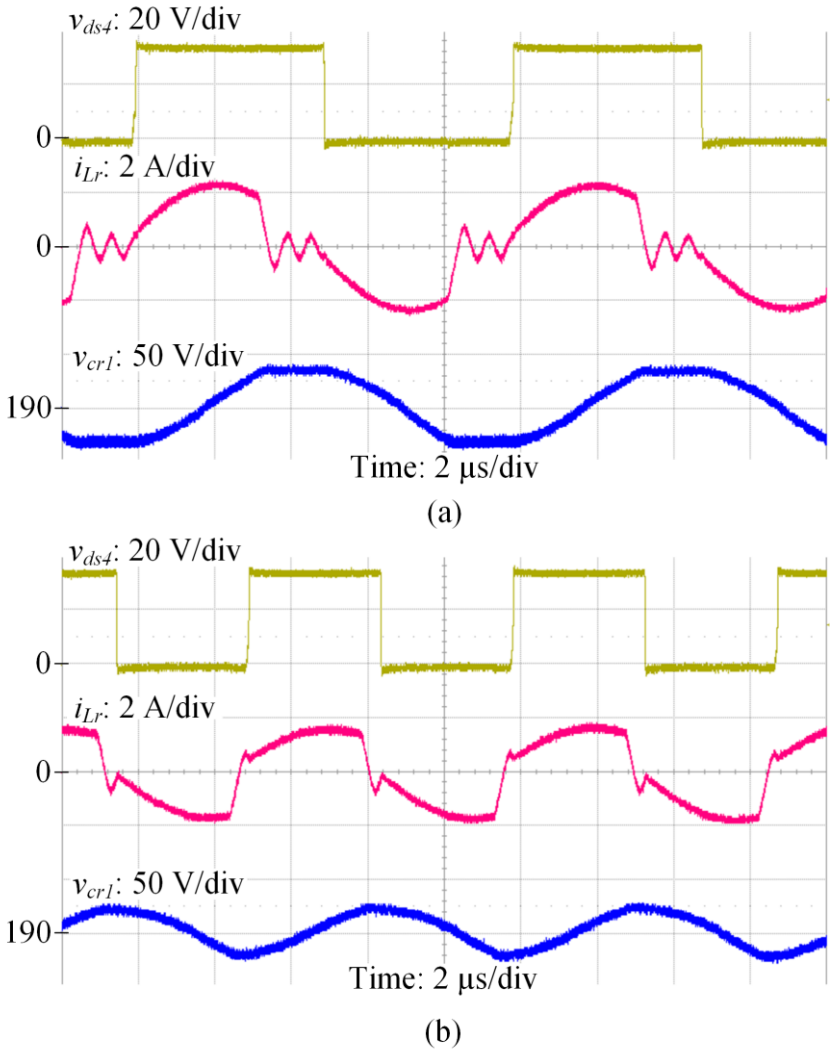


Figure 6.13. Experimental steady-state waveforms of converter operating in Buck Mode with a 33-V input and 225-W output with a switching frequency of (a) 100 kHz and (b) 143 kHz.

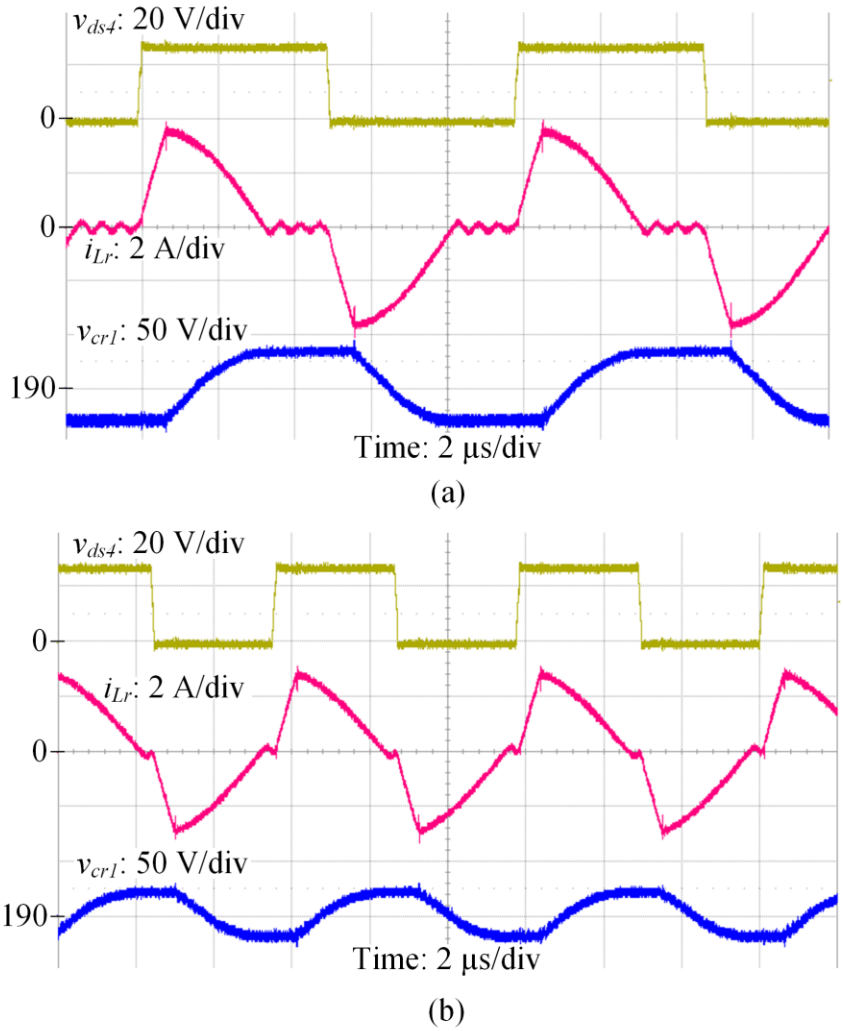


Figure 6.14. Experimental steady-state waveforms of converter operating in Boost Mode with a 26-V input and 225-W output with a switching frequency of (a) 100 kHz and (b) 158 kHz.

Mode is shown with a 33-V input a 225-W output while Boost Mode is shown with a 26-V input and 225-W output. For both cases, the MPL frequency is equal to the BCM frequency. As the DCM period is minimized, the peak and rms values of i_{Lr} and the ripple across v_{cr1} decreases.

Efficiency measurements are shown in Figure 6.15 and Figure 6.16 comparing fixed frequency DCM and variable frequency MPL operation. Figure 6.15 shows the weighted CEC efficiency for different input voltages and Figure 6.15 shows the efficiency

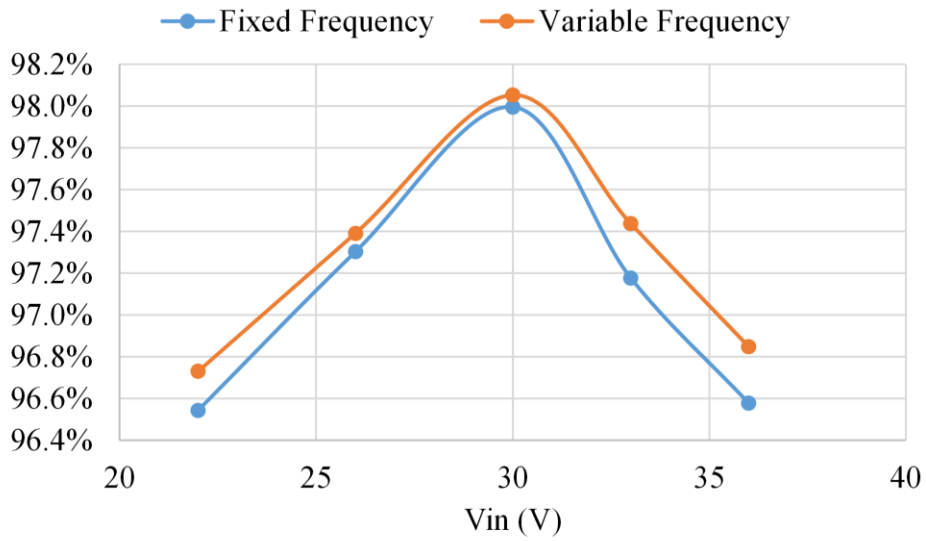


Figure 6.15. Comparison of CEC efficiency between fixed frequency operation and MPL variable frequency operation.

versus output power for (a) V_{in} = 36 V, (b) V_{in} = 30 V, and (c) V_{in} = 22V. When the converter is operating close to the series resonant frequency with the nominal 30-V input, the variable frequency MPL algorithm has very little impact on the converter efficiency. However, as the converter moves farther away from the series resonant point of operation shown in both the 36-V and 22-V input cases, the MPL algorithm has more of an effect. During the 36-V case in Buck Mode, switching losses of the primary-side MOSFETs are more dominant than in Boost Mode, therefore, the light load efficiency in Buck Mode is greatly increased by dropping the switching frequency. For both the 22-V and 36-V cases, the efficiency at heavy loads is increased from the reduction in conduction losses.

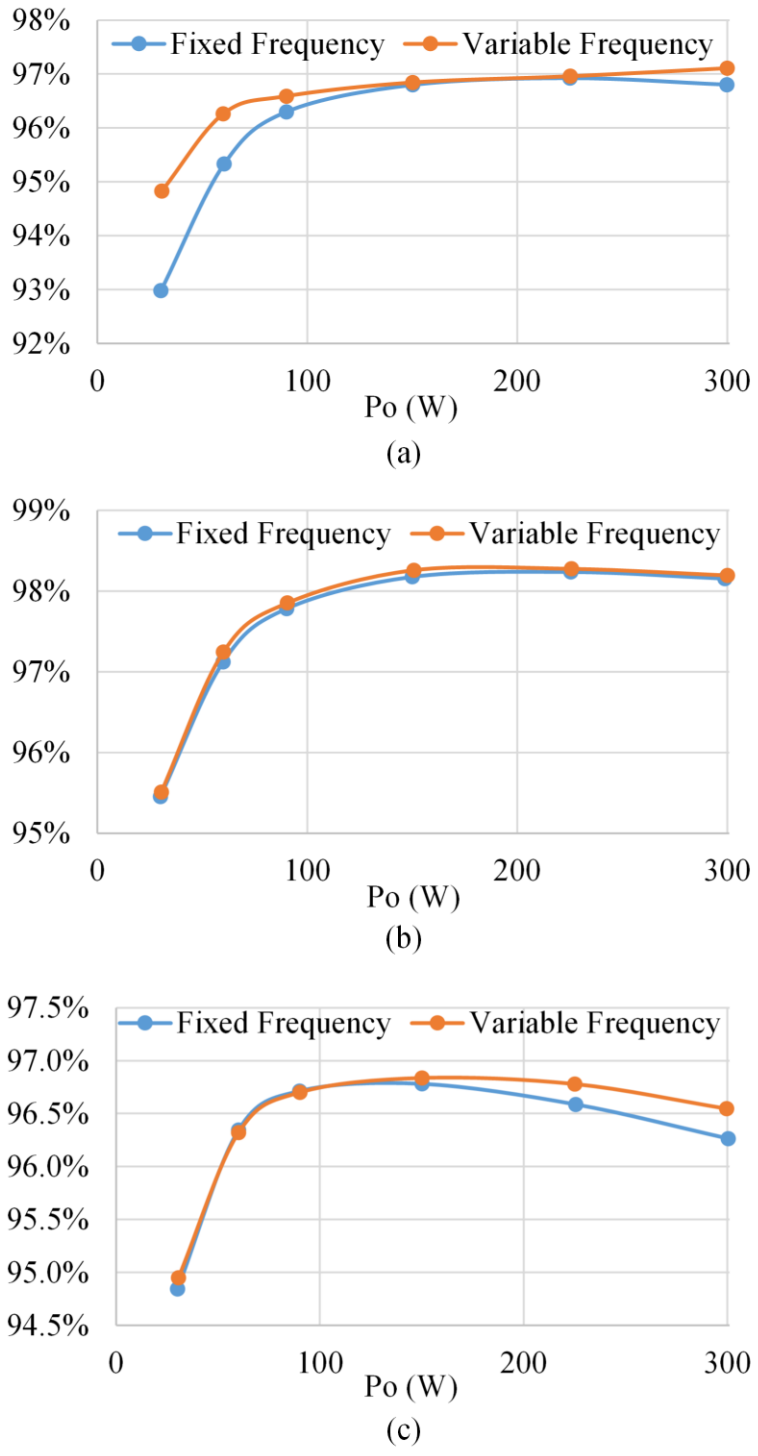


Figure 6.16. Experimental efficiency comparison between fixed frequency and MPL variable frequency operation with an input voltage of (a) 36 V, (b) 30 V, and (c) 22 V.

6.3 Summary

In this chapter the merits of using integrated magnetics versus an external resonant inductance are explored. While integrated magnetics allows for the reduction in number of components, associated cost, and PCB size, it comes at the cost of lower power conversion efficiency. In order to obtain a high enough leakage inductance in the isolation transformer to be able to use it as the resonant inductance, winding configurations need to be used that will result in higher proximity effect losses. The proximity effect increases the effective frequency-dependent ac resistance of the transformer windings resulting in increased conduction losses. When an external leakage inductor is used, a winding configuration can be used that will minimize both leakage inductance and proximity effect resulting in higher efficiency. Two different prototypes were compared: one using integrated magnetics and one using an external resonant inductance. While the prototype with the external resonant inductor was 7.2% larger in size and 1.8% more expensive, it exhibited a 0.3% increase in CEC efficiency resulting in an overall 98.0% CEC efficiency.

This chapter also explores a variable frequency algorithm that maximizes converter efficiency. Based on the input voltage and output power operating conditions, this algorithm calculates all of the switching frequency related losses in the system and selects the frequency that will result in the least amount of losses. This algorithm is used solely for minimizing the losses in the system and not for control, so it is able to be implemented several orders of magnitude slower than the voltage controllers. This way very simple fixed-frequency modeling and voltage controller design techniques can still be used. Experimental results were provided showing the effectiveness of the algorithm. The algorithm was able to increase the light load efficiency with a high-voltage input almost

2% by reducing the dominant MOSFET turn-off losses. The heavy load efficiency was increased for all input voltage levels due to the reduction in dominant conduction losses. This efficiency increase was around 0.4% for both high- and low-input voltage levels which correlates to 1.2 watts of savings at full load. This algorithm is very attractive because it increases the efficiency of the converter without adding any additional system costs or controller complexity.

Chapter 7

Conclusions and Future Work

7.1 Conclusions

As the demand for photovoltaic energy generation increases worldwide, it is becoming more and more important for the power electronics converters in the power conditionings systems to become more efficient and lower in cost. When compared to conventional centralized and string-inverter PCSs, modular have superior maximum power point tracking ability which yields higher power outputs for the same array of PV modules. This is because each PV module has its own converter performing MPPT to ensure each individual module is outputting the maximum amount of power available. However, there are higher costs and lower power conversion efficiencies associated with these types of PCS due to the increased number of power electronics converters. The work in this dissertation proposes a new low-cost high-efficiency microconverter which is an excellent candidate for several different modular PCS architectures.

The dc-dc stage, or microconverter, of a modular PCS is burdened by several difficult design requirements: low component count, wide input-voltage range, high boost ratio, galvanic isolation, and high efficiency over a wide input-voltage and output-power operating range. This dissertation introduces a novel topology which is capable of achieving all of these requirements. The converter is based on the highly-efficient isolated series resonant converter. Based on this topology, two different hybrid modes of operation are introduced using simple fixed-frequency control. The converter is able to achieve high

efficiency through low circulating currents, ZCS of the output diodes, ZVS and/or ZCS of the primary-side active switches, and direct power transfer to the load for the majority of the switching cycle. The converter efficiency is optimized for the nominal PV module output voltage and is able to achieve 97.7% weighted CEC efficiency at this operating voltage.

The work in this dissertation can be grouped into three main categories: (i) the introduction of a new topology and the associated systematic design procedure, loss analysis, modeling, control design, and modulation technique; (ii) system-level integration issues the converter may face when used in different types of modular power conditioning system architectures; and (iii) efficiency optimization of the converter.

The first category this work focuses is the introduction of a new circuit topology. A thorough analysis of the proposed converter's steady-steady operation using state-plane trajectory plots was presented which allowed for the development of a systematic design procedure and an accurate loss model. This loss model was verified experimentally through efficiency measurements. From a control perspective, the proposed converter exhibits both PWM and resonant characteristics which makes modeling difficult. In order to derive control-to-input voltage transfer functions for the converter, a simplification method is introduced which allows the converter to be modeled as a simple single-switch PWM converter. A new smooth transition technique is also introduced which allows the converter to transition smoothly between operating modes. This is done using a two-carrier PWM modulator. Experimental loop gains of the converter were measured using a frequency response analyzer in order to verify the proposed simplified modeling technique and controller design. Using simple PI controllers, the control bandwidths for all operating

conditions were between 1.4 kHz and 4.6 kHz with a minimum phase margin of 49°. The smooth transition method also allowed the converter to successfully transition back and forth between operating modes within 750 μs.

The second major focus of this work was system-level integration issues the converter may face when used in different types of modular power conditioning system applications. This work presented a novel soft start method which allows the converter to start up with a large capacitive load that has no initial charge. Very large capacitive loads may be seen when used in a dc microgrid or distributed microconverter with centralized inverter PCS. The proposed method adds a single low-cost clamping diode in parallel with one of the resonant capacitors to remove initial startup transients that can lead to overvoltage failures of the ac switch and resonant capacitors. With the diode in place, the converter is able to start up quickly and safely. It was even demonstrated to start safely with a short-circuited output condition. In addition to soft start, maximum power point tracking is an essential system-level task that needs to be performed regardless of the type of PCS. Different MPPT algorithms were discussed and one of the most commonly used algorithms was successfully implemented using a prototype of the proposed converter. The final system-level issue that was explored was double line frequency ripple rejection. This is an essential task for any PCS that utilizes an ac grid. Different double line frequency ripple rejection techniques were discussed, and one of the simplest but most effective algorithms that exists in literature was successfully implemented in the prototype converter. Even with a very low bandwidth voltage controller, the algorithm was able to almost completely remove the double line frequency ripple.

The final area of focus in this work is efficiency optimization of the proposed converter. The resonant inductor can either be implemented using integrated magnetics or as an external inductor. The initial prototype design used integrated magnetics with the aim of reducing parts count and associated costs, but this work explored in detail how using integrated magnetics results in higher proximity effect losses which leads to higher conduction losses in the converter. A new prototype was developed utilizing an external resonant inductor and the CEC efficiency with the nominal input voltage was increased from 97.7% to 98.0% while only increasing the component costs by 1.8%. Finally, a variable frequency efficiency optimization algorithm was introduced which changes the switching frequency in order to optimize efficiency, not as a means of control. The switching frequency is updated very slowly which allows the previously introduced simple fixed-frequency modeling and control methods to be implemented. This algorithm has a greater effect on the converter efficiency as the operating point moves farther away from the series resonant point of operation. As the input voltage moves farther away from the nominal input in either direction, the converter moves farther from the series resonant point of operation resulting in larger DCM periods. The variable frequency algorithm was able to reduce these DCM periods to increase high-load efficiency up to 0.4%, and under light-load conditions the efficiency was increased up to 2% through decreased switching losses.

In conclusion, this work presented a novel isolated dc-dc circuit topology with a low parts count, capable of regulating over a wide input-voltage range, a high boost ratio, galvanic isolation, and very high power conversion efficiency. This topology is an excellent candidate for implementation in modular PV power conditioning systems such

as the front end of a two-stage microinverter, distributed microconverters with a centralized-inverter, and in a dc microgrid application.

7.2 Future Work

Further improvements can be made upon the proposed microconverter topology in order to increase efficiency, decrease size, and decrease cost. The largest efficiency limitations of the proposed converter are output diode conduction losses, turn-off losses of the primary-side MOSFETs in Buck Mode, and both turn-on and turn-off losses of the ac switch during Boost Mode. All of these problems will naturally be diminished as more advanced semiconductor devices become available that display better performance characteristics. As more wide-bandgap semiconductors become commercially available, switching losses will be lower so higher switching frequencies can be achieved resulting in more efficient, smaller, and lower cost magnetics. Additionally, different techniques can be explored to achieve zero-voltage switching of the ac switch.

Further improvements could be made to the control system through the development of hybrid PWM and resonant converter modeling techniques. The control simplification presented in this paper results in a model that is only accurate for frequencies up to 10 kHz, thus limiting the potential bandwidths of the voltage controllers.

Last but certainly not least, more research can be done exploring system level integration issues. As distributed dc power generation becomes more mature, new standards regarding safety and fault handling will need to be thoroughly investigated in order to be incorporated into the control system of the microconverter.

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