Identification of Small-Signal dq Impedances of Power Electronics Converters via Single-Phase Wide-Bandwidth Injection

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Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of

Doctor of Philosophy
In
Electrical Engineering

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October 23rd, 2014
Blacksburg, Virginia

Keywords: small-signal dq impedance identification, modeling of diode rectifier, single-phase injection, multi-level shunt current injection converter, interleaved series voltage injection converter, wide bandwidth signals

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ABSTRACT

AC and DC impedances of switching power converters are used for the stability analysis of modern power electronics systems at three-phase AC and single-phase DC interfaces. Therefore, a small-signal characterization algorithm for switching power converter, which is based on FFT, will be presented and explained. The presented extraction algorithm is general and can be used to obtain other small-signal transfer functions of arbitrary power converter switching simulation models. Furthermore, FFT algorithm is improved by using cross power spectral density functions for identification, resulting in an algorithm, which is more noise immune. Both small-signal identification algorithms are validated in simulations, and CPSD algorithm is used in experimental measurement procedure. Several wide bandwidth injection signals, among which are chirp, multi-tone, pulse and white noise, are compared and theoretically analyzed. Several hardware examples are included in the analysis.

The second part of the dissertation will focus on the modeling of small-signal input dq admittance of multi-pulse diode rectifiers, providing comparison between well-known averaged value models (AVMs), parametric averaged value models (PAVM), the switching simulation model and hardware measurements. Analytical expressions for all four admittances present in the dq matrix are derived and analyzed in depth, revealing the accuracy range of the averaged models. Furthermore, a hardware set-up is built, measured and modeled, showing that the switching simulation model captures nonlinear sideband effects accurately. In the end, a multi-pulse diode rectifier feeding a constant power load is analyzed with modified AVM and through detailed simulations of switching model, proving effectiveness of the proposed modifications.

The third part describes implementation and design of a single-phase multi-level single-phase shunt current injection converter based on cascaded H-bridge topology. Special attention is given toward the selection of inductors and capacitors, trying to optimize the selected component values and fully utilize operating range of the converter. The proposed control is extensively treated, including inner current, outer voltage loop and voltage balancing loops. The designed converter is constructed and integrated with measurement system, providing experimental verification. The proposed multi-level single-phase converter is a natural solution for single-phase shunt current injection with the following properties: modular design, capacitor energy distribution, reactive element minimization, higher equivalent switching frequency, capability to inject higher frequency signals, suitable to perturb higher voltage power systems and capable of generating cleaner injection signals.

Finally, a modular interleaved single-phase series voltage injection converter, consisting of multiple paralleled H-bridges is designed and presented. The decoupling control is proposed to regulate ac injection voltage, providing robust and reliable strategy for series voltage injection. The designed converter is simulated using detailed switching simulation model and excellent agreement between theory and simulation results are obtained. The presented control analysis treats different loads, examining robustness of the circuit to load variations. Simulation model and hardware prototype results verify the effectiveness of the proposed wide-bandwidth identification of small-signal dq impedances via single-phase injections.

To my large and happy family

My wonderful wife: ***Svetlana***
Our toddler boy: ***Aleksa***
Our baby twin girls: ***Teodora*** *and* ***Ivona***

My parents: ***Dragoljub*** *and* ***Kosana***
My sister and brother: ***Jelena*** *and* ***Nikola***

Acknowledgement

I am very happy to have a great opportunity to express my sincere gratitude to all the people that helped, influenced and supported my work and stay at Virginia Tech.

I would like to express my sincere gratitude to my advisor, Dr. Dushan Boroyevich, for his support, guidance and encouragement during my study at the Center for Power Electronics Systems (CPES) at Virginia Tech. If I would have to describe him with just a few words I would use: "the greatest motivator". Even when I failed to find a solutions or answers to given questions, I would feel bad that I did not tried harder. His profound knowledge, gentle personality and rigorous attitude toward the research greatly influenced me in several aspects.

It is an honor for me to have Dr. Fred C. Lee as a committee member. I am very thankful to him for all the technical discussion, opinions, and suggestions. I am sincerely grateful to Dr. Rolando Burgos and Dr. Paolo Mattavelli for the guidance during my effort to understand and complete the research and projects tasks. I appreciate their help and the time they have given me in helping me during my studies.

Dr. Virgilio Centeno and Dr. Craig Woolsey influenced my work a lot. I am very thankful to them for all technical discussion, opinions, and suggestions regarding the stability of power systems and control of nonlinear systems.

I also express my thanks to everyone in CPES, who helped me achieve my goal, while still enjoying to be and work in such a great environment. Thanks to Ms. Marianne Hawthorne, Ms. Teresa Shaw, Ms. Trish Rose, Ms. Linda Long, Ms. Linda Gallagher, Mr. Douglas Sterk, Mr. David Gilham, Mr. Ji Shu and Dr. Wenli Zhang.

Thanks and appreciation are given to my team members on the Rolls-Royce, Boeing, Newport News Shipbuilding, Office of Naval Research and Renewable Energy Nanogrid Consortium projects: Dr. Zhiyu Shen, Mr. Igor Cvetkovic, Mr. Bo Wen, Mr. Justin Walraven, Mr. Bo Zhou, Dr. Sara Ahmed, Dr. Ruxi Wang, Dr. Dong Dong, Dr. Di Zhang, Dr. Xuning Zhang, Dr. Jin Li, Mr. Yang Jiao, Mr. Sizhao Lu, Mr. Fang Chen, Mr. Wei Zhang, Mr. Chi Li, Mr. Jun Wang, Mr. Alinaghi Marzhoughi, Mr. Vahid Najmi, Ms Niloofar Rashidi.

I am also very grateful to all my colleagues in CPES for their help, mentorship, and friendship. I cherish the wonderful time that we worked together. I thank to Mr. Milisav Danilovic, Dr.

Hemant Bishnoi, Dr. Daocheng Huang, Dr. Zheng Chen, Dr. Yiying Yao, Dr. Fang Luo, Dr. Qiang Li, Dr. David Reusch, Dr. Mingkai Mu, Mr. Jing Xue, Mr. Jiang Li, Mr. Feng Yu, Dr. Mingkai Mu, Dr. Weiyi Feng, Mr. Shuilin Tan, Mr. Chanwit Prasantanakorn, Dr. Yingyi Yan, Dr. Yipeng Su, Mr. Zhemin Zhang, Mr. Lingxiao Xue, Ms. Christina DiMarino, Mr. Yin Wang, Mr. Woochan Kim, Mr. Pei-Hsin Liu, Mr. Xiucheng Huang, Dr. Jongwon Shin.

I would also like to thank numerous visiting scholars and researchers from all over the world that I met and worked with at Virginia Tech. Thanks to Dr. Milijana Odavic, Dr. Marcos Alonso, Mr. Tine Konjedic, Dr. Fran Gonzalez-Espin, Dr. Montie Vitorino, Dr. Thiago Soeiro, Dr. Fabien Dubois, Mr. Phillip Akira Shiraishi, Dr. Daniel Diaz, Dr. Oscar Lucia, Dr. Virgilio Valdivia, Dr. Qing-Chang Zhong, Mr. Jani Hiltunen.

I am sure I have missed my appreciation to many other people.

To you all, thank you so much!

In the end, I would like to thank my large and happy family for their never-ending support, love, and encouragement that helped me complete this work.

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Chapter 1. Introduction

1.1 Background

The power electronics has been widely used for the power processing, power generation and power conversion purposes in contemporary electrical power systems employed worldwide. One of the main benefits of power electronics technology is the controllability of the switches, providing numerous options for the selection of control strategies. Usually, the regulation of output voltage is implemented, ensuring stable operating point for loads even if variations in the source side are occurring. However, it has been shown [1]-[3] that output voltage regulation can provide negative incremental impedance characteristic at converter's input, which can cause system instability due to the interaction with the control strategy implemented in the source part of power system.

1.2 Power systems

Modern AC power systems include power electronics components and converter in larger and larger scale, offering multiple benefits to the final users like faster response, more user friendly, more reliable, more efficient, more functional etc. This is especially the case in renewable and distributed generation systems, which are evolving rapidly in the whole world [4]-[5] in the recent years.

Furthermore, with the higher enrolment of the distributed generation systems in modern power systems, nanogrid and microgrid concepts, are being proposed and investigated for implementation in the modern power systems [6]-[7]. Bidirectional converter called energy control centers (ECCs), which offer high level of flexibility, are used to realize these concepts and provide hierarchical structure of the grid.

Figure 1-1 shows the electrical schematic of the modern AC power system that consists of wind turbine renewable source, classical power grid, typical three-phase AC and DC loads

connected via active front-end rectifiers and typical three-phase AC and DC loads connected via three-phase diode rectifiers.

The wind turbine source is usually connected to the rest of the power system via two active bridges, which convert variable frequency power present at the wind turbine output to constant frequency power transmitted via AC power grid. In order to successfully transform variable frequency power to constant frequency power, there are two controllers used, one for each bridge, providing effective decoupling control. Furthermore, due to the increased usage of the power electronics converters, control is implemented in each load, demanding proper design and separating of the source and load controller to avoid stability issues. Although, power electronics converters offer many advantages, proper controller design and stability analysis has to be carried out to ensure the stable and reliable operation of the power grid.

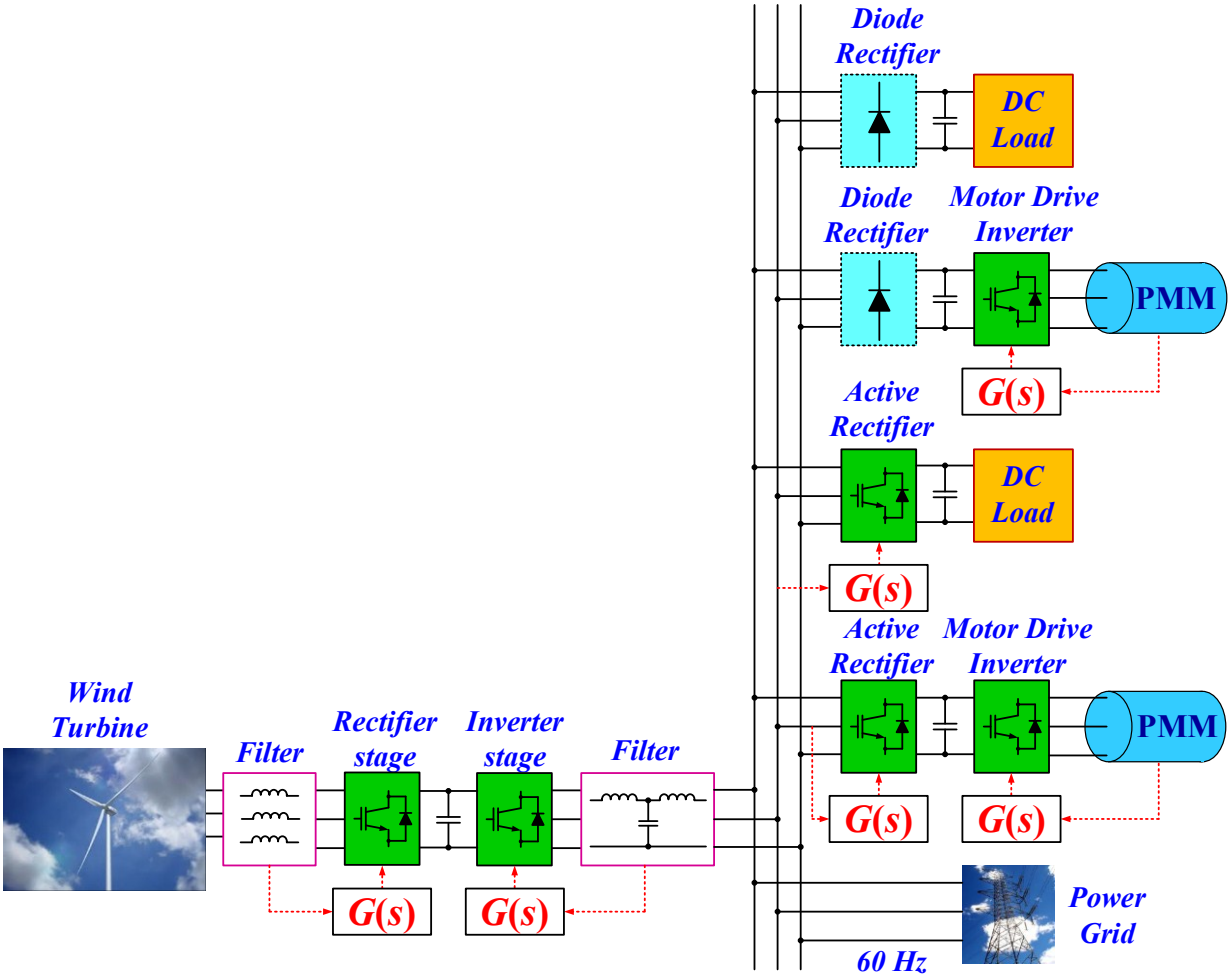


Figure 1-1: Electrical schematic of modern power grid with majority of source and load power electronics converters

Diode rectifiers are passive as no direct control is used to regulate switching pattern, instead the bridge switching depends on the applied ac voltage and current commutation. However, diode bridges map dc side admittance and consequently the control to ac side, imposing stability challenges to the source side controls.

Furthermore, similar stability challenges exist in smaller power systems, like one in service on more electric aircraft (MEA) systems, all electric ships (AESs), hybrid electric vehicles and other vehicular power systems [8].

Modern aircraft power systems use variable frequency generators (360 Hz-800 Hz), instead the traditional constant frequency (400 Hz) drive generators, which are maintenance intensive, less reliable and larger in weight and size. Even more, there is a trend to use electric power to replace parts that are traditionally operated by mechanical, pneumatic, or hydraulic power, improving fuel efficiency or total power system efficiency together with reducing the size and weight of the related parts [9]-[10]. A majority of these functions are operated by electric motor drives, which are used to regulate air conditioning, cabin pressure control, fuel pumping, and flight actuation. The estimate is that more than fifty percent of electric power is processed using a power electronic converters. However, it has been already shown that MEA power systems are prone to the instability due to negative resistance low frequency nature of constant power loads [11]-[12].

Similarly, the power system in AESs has additional power converter load to provide power used for the propulsion, while keeping other power converter loads as in MEA power systems.

1.3 Stability analysis of AC power systems

A lot of research is being conducted in the field of AC and DC stability of the modern power electronics systems in the past years [13]-[17], concentrating on defining stability criteria and performing stability analysis, being more or less conservative.

The stability criteria for DC and AC system are well-defined in terms of small signal source and load impedances. Thus, the small-signal source and load impedances can give valuable insight into the system's stability. The first stability criteria for DC systems were proposed by Middlebrook [2]-[3], which is shown to be a rather conservative approach. The less conservative approach included the usage of Nyquist Criterion over equivalent loop gain defined via the source

and load impedance ratio [16]-[17], providing very effective tool for accurate and precise stability analysis.

$$L(s) = \frac{Z_{dcsource}(s)}{Z_{dcload}(s)} \tag{1–1}$$

The presented stability analysis for DC power systems is straight-forward as a steady-state DC operating point exists in the system. The DC operating point is time changing due to the switching action in the power converters. The "clean" DC operating point can be obtained by averaging the voltage and current variables over the switching period, enabling a usage of the well-defined stability criteria for single-input single output (SISO) systems from the control theory.

The input filter interaction with the converter can lead to the system instability, which has been previously shown in [110]. The measurement of input and/or output impedances of dc power supplies and its applicability to the stability analysis has been shown in [108]. Furthermore, the identification of small-signal transfer functions of dc/dc converters using the cross correlation techniques is explained in [109].

The stability analysis and impedance specification for the dc distribution system together with the estimation of stability margins has been performed in [113], [114].

However, this is not the case in AC power systems, where the voltage and current variables keep changing over the time, with constant or variable frequency, meaning there is no direct operating point that can be defined via voltages and currents. However, virtual DC operating point is obtained if current and voltages are transformed to synchronous coordinates via Park's transformation.

$$T_{dqo/abc}(\theta) = \sqrt{\frac{2}{3}} \begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \tag{1–2}$$

The inverse Park transformation that forms a transformation pair with the previous equation.

$$T_{abc/dqo}(\theta)=T_{dqo/abc}(\theta)^{-1}=T_{dqo/abc}(\theta)^{T}=\sqrt{\frac{2}{3}}\begin{bmatrix}\cos(\theta) & -\sin(\theta) & \frac{1}{\sqrt{2}}\\ \cos\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta-\frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}}\\ \cos\left(\theta+\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right) & \frac{1}{\sqrt{2}}\end{bmatrix} \quad 1–3$$

In this manner the voltages and currents in dqo coordinates are obtained by the following expressions.

$$v_{dqo}(t)=T_{dqo/abc}(\theta)v_{abc}(t) \quad 1–4$$

$$i_{dqo}(t)=T_{dqo/abc}(\theta)i_{abc}(t) \quad 1–5$$

After applying Park's transformation the DC operating point for a three-phase power converter is obtained. However, the obtained DC operating point can be time-varying due to switching actions in the switching power electronic converters. The averaging concept from DC/DC converters can be extended to provide well-defined operating point for three-phase power converters as used in [18].

In this sense the dq impedance matrix is defined as a ratio of voltage and current matrices, as described with the following matrix expression.

$$Z_{dq}(s)=v_{dq}(s)i_{dq}^{-1}(s) \quad 1–6$$

The Generalized Nyquist criterion (GNC) applied on multivariable loop gain defined via the return ratio product of source dq impedance and load dq admittance to assess the stability of three-phase AC power system is first proposed by Belkhayat in 1997 [19]. The stability analysis of the three-phase power systems is focused on a system with constant power loads, which behave as a negative resistance in the small-signal sense.

$$L(s)=Z_{dqsource}(s)Z_{dqload}^{-1}(s)=Z_{dqsource}(s)Y_{dqload}(s) \quad 1–7$$

GNC was introduced for the stability analysis of multi-variable systems by MacFarlane and Postlethwaite [24]-[25]. The stability of the system is obtained by looking at the characteristic loci of the return ratio matrix. The method applies Nyquist criteria on eigenvalues, and gives the precise stability analysis by counting the number of encirclements around critical point (-1,0) in complex

plane. The applicability of GNC to multi-variable systems is treated in classical textbooks like [26]-[27].

The simplified GNC criteria, obtained by reducing it to SISO Nyquist criteria in case when the power converter operates close to unity power factor, is presented in [20]-[21]. In this case, the dominant power flow and coupling in the multi-variable system is happening over a single coordinate, enabling the reduction of GNC criteria to Nyquist criteria.

The other approach to study stability is to inject a perturbation directly via AC single phase and perform the small-signal impedance estimation [22]. Furthermore, stability of the three-phase AC power system can be obtained via the injection of positive and negative sequence impedances of three-phase AC interfaces and applying GNC over source and load impedance ratios of both positive and negative sequences [22]-[23]. The explanation for this approach is that even DC operating point defined in dq coordinates is time variant in nature due to the switching action of power converter, therefore it makes sense to directly apply positive and negative sequence perturbation directly to time-varying three-phase AC interface. Although, this approach cannot be fully explained and validated via equations and theory, it gives reasonable accurate stability analysis in practice.

The stability of modern power systems with the variable frequency is analyzed in [50]. In this work nonlinearity nature of the system are taken into the account and Lyapunov based stability criterions are investigated.

1.4 Impedance measurement techniques for AC power systems

A very detailed survey of impedance measurement techniques in dq coordinates for stability analysis of AC power systems based on FFT algorithm is thoroughly presented in [28]-[30]. This work proposes several practical realizations of power converter that can be used as injection generation circuits. The focus is only on shunt current injection and the proposed solutions are verified in simulations and experimentally.

One more very interesting solution for the impedance extraction based on unbalanced single-phase injection is presented in [31]-[33], [52]. In this solution the complexity of the injection converter is reduced to single-phase, providing small-number of modules and circuit components.

Furthermore, one converter can be used to access the stability of modern AC power grid on three-phase AC interface, single-phase AC interface and DC interface, by using the same connection and converter design. The control needs to be adjusted automatically, depending on the interface voltage, but with the usage of modern digital signal processors (DSPs) this is not an issue.

Very interesting, alternative approach to previously described techniques that are performed in frequency domain, is the time-domain identification of impedances via step load changes. This approach is effectively used to perform black-box modeling, impedance identification and stability analysis as presented in [34]-[37]. The benefit of this approach is that only two transient responses are needed to fully characterize the small-signal impedance characteristic in the full frequency range. However, due to the usage of the step excitation, which has decreasing signal energy as frequency is increasing, higher frequency range is not so precisely characterized.

The small-signal identification of black-box models of the power electronics converters using the transient responses is shown in [49], extending the usability of the already proposed procedure. The unterminated black box modelling of power converters in dq coordinates has been developed in [112].

Furthermore, the neural network techniques for impedance estimation are successfully used to characterize dq impedances in the work presented in [38]-[40].

Parametric identification of large signal impedances via the recursive least square estimation algorithm in complex plane is presented in [41]. Furthermore, a patent for the stability analysis at a three-phase interface, which is based on the injection of of the suppress carrier injection signals, is presented in [48]. The proposed signals are effectively used in the stability analysis.

Wide bandwidth identification by injection of white-noise and with the cross-correlation processing techniques to extract the small-signal dq impedances is presented in [43]-[44].

The impedance measurements of power systems using the power converter and spectrum estimation are presented in [115]-[118].

Finally, several fully automated solutions are also presented in [45]-[47]. Two solutions rely on post processing performed with network analyzers or other similar frequency domain characterization instrumentation. On the other hand, [46] proposes the usage of the chirp signal for wide-bandwidth identification as chirp signal has optimal crest factor and controller injection

bandwidth. The automated solution for the extraction of dq impedances via the injection of multi-tone signal using the power amplifiers is presented in [129].

Once the small-signal impedances are identified, the obtained information can be used to shape the impedances of the converters connected to the grid [42]. In this way, the adaptive online control of grid connected converter ensures the stable operation of the grid. The goal is to use identified impedances to ensure stable operation of the grid in different operating points. The modern power grid offers capability for the integration of larger number of converter, therefore increasing the complexity of the grid with an increased potential of the instability in the grid.

1.5 Algorithms for characterization of small-signal transfer functions of power electronics converters

Furthermore, in order to design the stable system, it is desired to check its stability by simulations, before constructing a complete hardware system. For that purpose, it is preferable to use a switching model in the simulations as it captures hardware properties more accurately. The drawbacks of using the switching model in simulations are following: it is more complicated than any known averaged models; it takes longer time to be simulated and small-signal analysis in frequency-domain is still a vague task, which has not been implemented in majority of simulators.

Usually switching simulations models are built using piecewise linear (PWL) models of switching components, enabling a user possibility to capture the switching behavior nature of the model and to add other more complex nonlinear components into the simulation model [53].

The time-domain simulations as well as the frequency domain analysis of switching models of dc/dc power converters in simulation software tools has been widely used. Usually, pure sinusoidal signal is used to perform ac analysis, but its main drawback is that it requires ac sweeping, which lasts long. On the other hand, the fastest frequency-domain analysis algorithm is implemented in Simplis and it uses periodic operating point (POP) calculation to find a steady-state operating point. Next, AC analysis is performed on top of POP calculation, the small-signal transfer functions are extracted very fast and accurately form the switching simulation model. The idea of using impulse response to characterize small-signal loop gain transfer function of dc/dc converter operating in discontinuous conduction mode (DCM), with the single time domain simulation is

shown in [54]. Time-domain simulations of DC/DC converters can be accelerated with the usage of waveform relaxation method as shown in [55]. AC sweep algorithm which injects sinusoidal signal with "small" magnitude and performs small-signal analysis to obtain different transfer functions is presented in [56], and it is based on assumption that small-signal injection will not change operating point and that the model can be linearized, yielding linear time invariant small-signal transfer functions. A small-signal simulation algorithm based on the sensitivity matrix used in shooting method is developed to characterize DC/DC converters [57]. In addition, multi-tone injection can significantly speed up frequency-domain analysis as shown on boost DC/DC converter [58], where loop gain is extracted accurately in very fast manner. The identification of small-signal immittance characteristic of power converter from a detailed switching simulation models is presented in [119].

Therefore, it is possible to obtain different small-signal transfer functions like input impedance or admittance, output impedance or admittance, control to output, control to inductor current, control to voltage, loop gain etc. Therefore, the design of control for dc/dc power converters and its verification via simulations is relatively straightforward task, which is a task that can be easily achieved in the numerous software tools.

In addition, there are a large number of software tools to simulate switching and dq averaged models of three-phase power converters. Although time-domain simulation of switching models is implemented in numerous software tools, the frequency analysis is still a difficult task which is not implemented in many of them. AC sweep based frequency-domain analysis is implemented in PSIM. In this case, fixed-step trapezoidal solver is used for time-domain simulations and on top of that FFT is applied to characterize small-signal transfer functions. Moreover, the impedance identification algorithm for three-phase voltage source inverter (VSI), which uses step load to create step excitation, is shown in [35]. The small-signal dq impedance transfer functions are characterized with the usage of time-domain identification techniques like ones implemented in MATLAB software tool and identification toolbox.

Hence, AC sweep algorithm that injects pure sinusoidal perturbation is implemented and presented in this dissertation, as it is the basic idea to obtain small-signal transfer function characteristics. The multi-tone and chirp injection signals are implemented to further speed up time

necessary to provide accurate simulation results, providing benefits of the wide bandwidth identification algorithm.

1.6 Modeling of input dq admittance of nonlinear multi-pulse diode rectifiers

The conventional three-phase diode rectifiers or line-commutated rectifiers are typical solutions for a rectifier stages in medium-power variable frequency drives, which are commonly used in industrial as well as commercial applications [62]. Such diode rectifier loads are widely used in modern distribution systems, industrial facilities, distribution generation and transportation systems, etc.

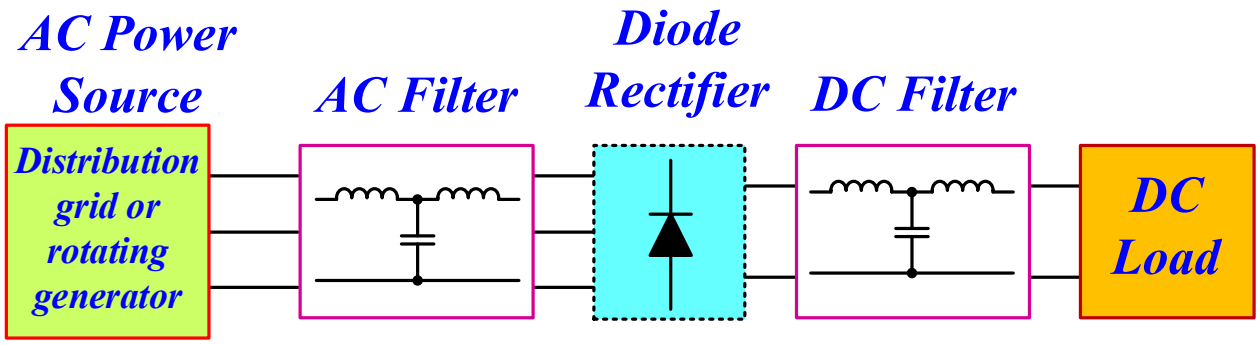


Figure 1-2: Electrical schematic of commonly used front-end diode rectifier unit

Figure 1-2 shows a typical configuration of front-end diode rectifier unit, where either distribution grid or rotating generator supplies power to the system. AC and DC filter topology are optional and usually designed and selected by the system integrator engineer. The AC filter depends strongly on the application, therefore various topologies are possible solutions, including phase shifting transformer, or shunt filters to attenuate low frequency harmonics, typically concentrating on 5^{th}, 7^{th}, 11^{th}, and 13^{th} harmonics [62]-[63].

Power system community has extensively researched the modeling and analysis of diode rectifier in the past [64]-[66], where some of the first work on this topic is published in 1969. Typically, step load transients and time domain responses are primary concern for power system engineers, mainly studying the stability of AC power systems in time-domain.

The dynamic averaged models for six-pulse diode rectifiers can be generally derived using two main approaches. The first approach derives equivalent averaged model by assuming that ripple

of dc current is sufficiently small, so it can be neglected in the derivation procedure, resulting in a first order harmonic assumption procedure. The detailed analysis and complete derivation procedure are presented in [67]-[72]. The important property to notice is the dependence of the averaged model on the conduction mode of diode rectifier, meaning that analytical expression are different for different rectifier operating modes. The precision of derived models depend on the correctness of the used assumptions, resulting in more precise modeling for continuous conduction mode (CCM) and less precise modeling for discontinuous conduction mode (DCM). The main reason for this is that small-ripple assumption for DCM is very inaccurate way of representing the rectifier's behavior. Additional burden on usability of analytical averaged models is that different source models yield different averaged models. Especially if source is the generator machine with complex equations, providing rather complicated averaged model in this case.

The main usage of the derived averaged models is to compare more detailed switching model with averaged model regarding time-domain transient responses to step load changes and small-signal output dc impedance frequency characteristic [73].

In order to improve the transient response of the averaged model, a first order Taylor series expansion term is used in the derivation procedure presented in [74]-[76]. The derivation procedure becomes even more labor intensive, yielding more complicated averaged model, which captures transient dynamic more accurately. The improved transient analytical averaged modeling is successfully applied to multi-pulse diode rectifiers as well.

Alternative approach to previous analytical modeling is the parametric averaged modeling as presented in [77]-[82]. If parametric averaged modeling approach is used, the topology of both ac and dc sides remain unchanged. The controlled voltage and current sources are introduced to couple both sides of the rectifier. However, the corresponding gains of the controlled sources are functions of operating point as well as each component value present in the circuit. Therefore, it is necessary to characterize these gains with respect to any possible change in the circuit. In this sense, the characterization process becomes very numerically intensive, but obtained numerical curves can be characterized parametrically via appropriate algebraic expressions. Finally, the obtained parameterized averaged model can cover much larger range of operating conditions, if enough data are obtained during numerical simulations.

In conclusion, the both modeling strategies are fundamentally different, offering advantages and disadvantages. Thus, both approaches are widely accepted in the engineering practice, as it is hard to conclude which one is better.

Interesting approach to modeling diode rectifier dynamic is based on deriving approximate switching pattern signals and applying Fourier series analysis to extract harmonic content as well as small-signal response [83]. The obtained analytical expressions are matching very accurately hardware measurements and simulation extraction results.

The dominant modeling approach for twelve-pulse, eighteen-pulse and other multi-pulse diode rectifiers is analytical averaged modeling, which is derived in similar manner as the derivation procedure explained for six-pulse diode rectifiers [84]-[88]. Similar conclusions are true for multi-pulse diode rectifiers. In addition, the Fourier analysis of switching pattern signal is extended to multi-pulse case successfully [89]-[90]. Furthermore, in this case the commutation period of switching cycle is modeled via piece wise linear approximation.

The identification of dq impedance of three-phase diode rectifiers with the injection of multi-tone signal via d channel and q channel is shown in [127].

1.7 Dissertation motivation and objective

In the past several years, a lot of work has been done to develop impedance measurement units, which would be capable to characterize small-signal dq impedances of source and load side. Furthermore, a lot of research work has been performed to develop new stability criteria that would offer simple and effective tool to access the stability of the modern AC power grids. Due to the successful implementation of measurement units, there has been increasing interest to further push research in this direction in both academic and industry societies. Although, many new things are explained and solved, there is still need to solve some challenges.

The first challenge, which engineers often face in the practice, is to perform similar small-signal analysis in the software simulation environment, preferably using switching simulation models. Although, the need for such extraction is apparent, only one simulation tool offers capability to perform such small-signal ac analysis. The developed ac block injects small-signal sinusoidal perturbation, runs time-domain simulation until the steady-state response is reached,

and by applying FFT over the steady-state waveforms, it is possible to characterize small-signal characteristic at the injected frequency. The implemented algorithm is not fast enough as fixed-step trapezoidal solver is used to calculate time-domain waveforms. If small enough step is used precision is increased and vice versa. Therefore, during the survey of different algorithms and possible injection signals, a small-signal analysis tool that can perform FFT ac sweep algorithm is implemented in MATLAB using SimPowerSystems toolbox. The next step is to investigate different injection signals and try to select one that would have optimal properties for small-signal extraction of transfer functions of three-phase power electronics converters.

The important part of modern power systems are diode rectifiers loads, where power systems engineers extensively have been studying averaged modeling. The main focus of the research are time-domain responses due to step load changes. The developed averaged models are very useful to be used in large scale simulation systems, when the switching simulation models burden significantly the computational time and available computer resources. In this case, the only way to perform simulation study is to use simplified averaged models, which capture diode rectifier dynamic very accurately.

Nevertheless, the small-signal extraction of dq impedances for diode rectifier has been done with the usage of parametric averaged model and it was not verified. The obtained results claimed new phenomena that needed verification, both in switching simulation and hardware experiments. Therefore, there was the obvious motivation to try to characterize the small-signal dq impedances of diode rectifiers and improve the known averaged models. Similarly, the natural extension of the modeling of diode rectifiers is to include modeling of multi-pulse diode rectifiers.

Furthermore, the developed impedance measurement units have been designed to characterize small-signal dq impedances of three-phase AC power systems for root mean square voltages up to 480 V and power levels up to 100 kW-200 kW. There is a great integration of renewable power systems based on power electronic converters with various control strategies into traditional power grid, resulting in power systems with stability issues up to medium voltage levels 4.16 kV-13.8 kV and power levels up to 2 MW-40 MW. This dissertation presents two modular converter, suitable for the perturbation of three-phase ac and single phase dc power system. The proposed converters are scalable, making them suitable solution for the injection into medium voltage grid. Therefore, the research topic analyzed in chapters is to present a design procedure for shunt current and series

voltage injection converters, which can be used to generate appropriate injection signals. Furthermore, the control strategy regarding both injections need to be robust and capable of decoupling of dynamics coming from either the source or load. In this way, new challenges and problems, which need to be researched and solved, are addressed and analyzed.

Finally, the switches are utilized in the implementation of injection converters need to switch at high frequency, to be able to sustain high voltage stress in off state, low loss and easy to use and maintain. Taking into consideration the described constraints, emerging SiC switches seem to be obvious choice. In this sense, it is desirable to use minimum number of modules, due to high price of SiC switches. Minimization of the number of modules can be accomplished by using unbalanced injection algorithm. The single-phase injection converters are used to generate desired injection signals, which requires the reduced number of modules. The research topic is to find an algorithm that could use a wide-bandwidth injection signals, significantly reducing the measurement time and extracting transfer function at larger number of points.

1.8 Dissertation outline

Chapter 2 of the dissertation describes an algorithm for small-signal characterization of power electronics converters. The described algorithm is incorporated into MATLAB/Simulink to identify small-signal transfer functions of switching simulation models of power electronics converters. The algorithm is further improved by the implementation of the cross power spectral density function to reduce noise influence. The improved algorithm is used to extract experimentally and numerically in simulations the small-signal dq impedances of power electronics converters.

Chapter 3 explains the modeling of input dq admittance of six-pulse diode rectifier and proposes a modification to obtain a more precise impedance modeling results. Furthermore, new effect typical for nonlinear systems, namely sideband admittances around multiples of switching frequencies is shown and contributed to a strong nonlinear behavior of six-pulse diode rectifier. The new effect is a unique property of diode rectifiers, which is not present in the active front-end rectifiers.

Chapter 4 extends the modeling of input dq admittances to the twelve-pulse diode rectifier case. Similar, sideband admittances effects are found in this case also, as this rectifier exhibits same nonlinear behavior due the presence of the diode bridges. Furthermore, it has been shown that in case of balanced power flow through both bridges, the twelve-pulse diode rectifier averaged model can be reduced to an equivalent six-pulse diode rectifier averaged model.

Chapter 5 shows the complete design procedure for multi-level single-phase shunt current injection (SCI) converter. The procedure selects and optimizes the inductor and capacitor values, providing the flexibility to use same components to perturb the three-phase ac power systems as well as single phase ac and /or dc power systems. The control design is treated in details to ensure the desired bandwidths necessary to generate injection signals in the full frequency range. Furthermore, the SCI converter is verified in simulations with the detailed switching model and in experiments.

Chapter 6 explains the design of the single-phase interleaved series voltage injection (SVI) converter and proposes the usage of ac decoupling control for the regulation of the injection voltage. The complete design procedure together with the selection of inductances and capacitances is presented and included into the analysis. Furthermore, the operation of SVI converter covers injection of arbitrary series voltage waveform into the three-phase ac power system as well as single-phase ac or dc system. The designed SVI converter is used in the next chapter for the online estimation of the dq impedances of the power system under test.

Chapter 7 presents the source and load impedances results obtained via the injection of single-phase wide-bandwidth signals. Two identification algorithms are presented and compared, namely FFT algorithm and cpsd algorithm based on Welch periodogram method of estimation of power spectra. The small-signal dq impedance of the actively controlled voltage source is precisely identified with both shunt current and series voltage injection. In addition, the small-signal dq impedance of passive load is accurately estimated. The chirp and multi-tone signals are proposed to be used in the single-phase injection, providing the identification of dq impedances in the increased number of points.

Chapter 2. Identification of Small-Signal dq Impedances of Three-Phase Power Electronics Converters

This chapter focuses on the small-signal identification of dq and dc impedances of different three-phase power electronics converters in simulations. Two identification algorithms based on fast Fourier transform (FFT) and cross power spectral density (CPSD) estimation are presented and explained. In order to characterize the small-signal dq impedances, the three-phase ideal current source as well as the three-phase ideal voltage source are used to generate the excitation signals in dq frame. Several wide-bandwidth injection signals are investigated and used to provide a wide-bandwidth excitation, reducing the extraction simulation time significantly.

2.1 Introduction

The small-signal ac and dc impedances of switching power converters are used for the stability analysis of modern power systems at three-phase ac and single-phase dc interfaces. Although, it is useful to extract impedances from the switching simulation models of three-phase power converters, still the small-signal frequency analysis is not a straight-forward task in many of the contemporary software tools. Thus, an FFT identification algorithm that extracts impedances of the switching simulation models is implemented and presented in this chapter. It is the basic idea for the small-signal impedance extraction, which is very effective when implemented with a sinusoidal signal injection. Furthermore, the presented algorithm is significantly improved with the implementation of wide-bandwidth injection, which enhances speed of the simulation tool substantially. The identification algorithm is implemented in MATLAB as it a commercially available software tool, which uses fast and accurate stiff variable-step solvers. Furthermore, the identification algorithm is validated on the switching simulation models of three-phase VSC when the converter operates as an inverter feeding a resistive load, grid-tied inverter and rectifier supplying a resistive dc load. The obtained impedance results are compared to the dq impedances derived from the classical dq averaged model of VSC. The presented extraction algorithm is general and can be used to obtain other small-signal transfer functions of arbitrary power converter switching simulation models.

The injection of a wide-bandwidth signals is an alternative solution that can significantly reduce simulation time as it does not require frequency sweeping. The proposed wide-bandwidth injection solution is first verified in simulations on three-phase two-level VSC switching model. Moreover, noise was added to obtained simulated variables and small-signal dq impedances are successfully extracted from the switching simulation model. Cross-correlation is applied to reduce error that is present due to the noise, but it is found that it only increases signal to noise ratio as it does not improve the accuracy on impedance evaluation. Finally, frequency averaging was able to improve the obtained impedance results from simulation models.

CPSD is implemented in MATLAB as a function, which estimates the cross power spectral density $P_{xy}(s)$, of two discrete-time signals, $x(t)$ and $y(t)$, using Welch's averaged, modified periodogram method of spectral estimation [91]. It has been shown that when the noise is added to currents and voltages obtained from the simulations models, the CPSD algorithm can significantly reduce noise effects on the identification precision. Usage of the proposed CPSD function and theoretical background will be explained later in this chapter in a separate section. The CPSD algorithm, which is used in simulation models, has also been used for the extraction of small-signal dq impedances in the hardware implementation of the impedance measurement unit [96]. Finally, CPSD function can be used to extract the small-signal dq impedances when single-phase injection signals are used, which will be introduced and explained in details in Chapter 7.

2.2 Properties of Different Injection Signals

This section of the chapter investigates the properties of different injection signals, which could be used for small-signal characterization of three-phase power electronics converters. Several candidate signals are analyzed in depth, namely chirp signal, multi-tone signal, ideal sinusoidal signal and pulse signal. The signals are compared regarding RMS values, crest factor (CF) values and content in the frequency domain. The crest factor of the injection signal $x(t)$ is defined in the following manner.

$$CF = \frac{\max\left(x(t)\right)}{X_{RMS}} \qquad 2\text{–}1$$

$$X_{RMS} = \sqrt{\frac{1}{T}\int_{t_o}^{t_o+T} x^2(t)dt} \qquad 2\text{–}2$$

Based on the analysis tradeoffs among the injection signals, multi-tone signal has been selected to perturb switching simulation models as it provides optimum properties for small-signal transfer function identification.

2.2.1 Sinusoidal Signal

Ideal sinusoidal signal is characterized via magnitude A, frequency f and initial phase θ_0 as described in the equation shown below.

$$x_{\sin}(t) = A\sin(2\pi f_o t + \theta_0) \qquad 2\text{–}3$$

The straightforward property of the sinusoidal signal is that the frequency domain characteristics consist of an ideal Dirac impulse at the injection frequency. The frequency domain characteristics of an arbitrary signal $x(t)$ is obtained with a Fourier transformation pair, as given below.

$$X(j\omega) = \int_{-\infty}^{+\infty} x(t)e^{-j\omega t}dt \qquad 2\text{–}4$$

$$x(t) = \frac{1}{2\pi}\int_{-\infty}^{+\infty} X(j\omega)e^{j\omega t}d\omega \qquad 2\text{–}5$$

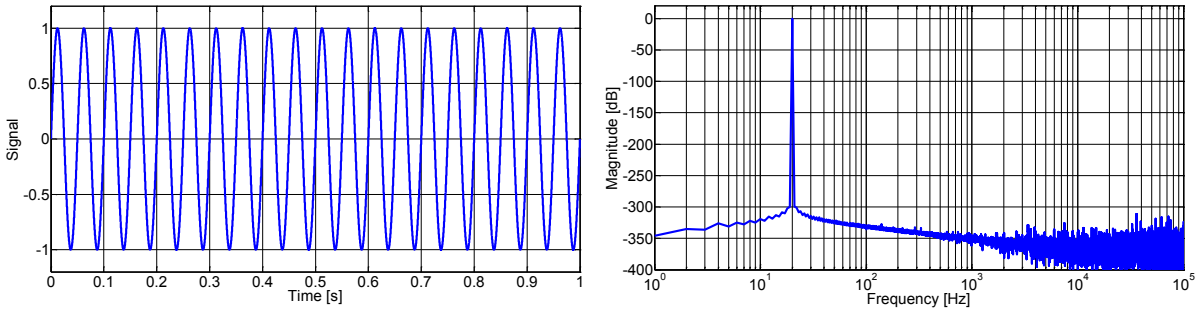
The frequency domain transfer function of sinusoidal signal can be simply written as given below.

$$X_{\sin}(j\omega) = \frac{\pi A}{j}\left(e^{j\theta_0}\delta(\omega-\omega_o) - e^{-j\theta_0}\delta(\omega+\omega_o)\right) \qquad 2\text{–}6$$

The sinusoidal signal has single tone in the frequency domain, therefore it is suitable for the frequency domain characterization of both nonlinear and linear systems. Theoretically, the small-signals frequency characteristic of the systems at the injection angular frequency ω_o is defined as a ratio of the response transfer function $Y(j\omega_o)$ and injected perturbation transfer function $X(j\omega_o)$.

$$H(j\omega_o) = \frac{Y(j\omega_o)}{X(j\omega_0)} \qquad 2\text{–}7$$

Summary of the properties of sinusoidal injection signals are the following: theoretically the frequency domain characteristic of both nonlinear and linear systems can be identified, crest factor of the sinusoidal signal is very good as it a low value of 1.414, whole energy of the time domain signal is grouped into a single frequency point, resulting in the high signal to noise ratio, and the only drawback is that ac sweeping is necessary in order to obtain the full frequency domain characteristics.



(a) (b)

Figure 2-1: Ideal sinusoidal signal (a) time-domain waveform (b) magnitude characteristic in frequency domain

2.2.2 Multi-Tone Signal

The multi-tone injection signal can significantly reduce simulation time necessary to characterize small-signal transfer functions as it excites arbitrary number of frequencies simultaneously. Furthermore, it is the most suitable signal to measure a Bode plot by signal analyzers based on FFT approach [59]. Several practical considerations for multi-tone signal injection are presented for frequency analysis of DC/DC converters [58]. Although, these considerations are similar to one used for frequency analysis in DC/DC power converters, some differences exists due to the nature of AC/DC conversion. The following considerations of multi-tone signals are important and need to be taken into account:

- Phase of each tone component: phase is selected to minimize the crest factor of multi-tone signal as presented in [60]-[61].
- Amplitude of each tone component: amplitude of all components is same, but maximum value of multi-tone signal should be small enough, not to perturb dc operating point too much. Otherwise, incorrect results may be obtained.

- Frequency selection: tone frequencies have to be selected appropriately to prevent overlapping of responses generated by different tones. Harmonics present in PWM three-phase converters can be written as a linear combination of line frequency, switching frequency and injected tones. Therefore, small procedure is written to check whether any tone is a linear combination of other important frequency components. If any such tone component is found, the tone is readjusted. Furthermore, sampling frequency has to be taken into account to prevent spectral leakage when FFT is applied.

  Multi-tone signal is generated with the following expression.

$$x_{mtone}(t) = \frac{1}{\sqrt{N_{tones}}} \sum_{i=1}^{N_{tones}} \sin(\omega_i t + \theta_{oi}) \qquad 2\text{–}8$$

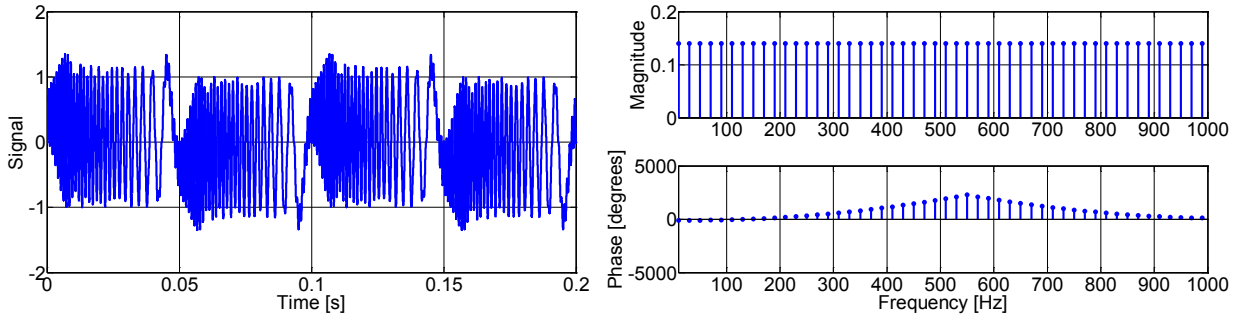
$$\omega_i = 2\pi f_i, f_i = f_o + i\Delta f \qquad 2\text{–}9$$

$$\theta_{oi} = \frac{\pi}{N_{tones}}(i-1)^2 \qquad 2\text{–}10$$

Analytical expression for the frequency domain content of multi-tone signal is obtained by applying Fourier transform to the time domain signal.

$$X_{mtone}(j\omega) = \frac{\pi}{j} \frac{1}{\sqrt{N_{tones}}} \sum_{i=1}^{N_{tones}} \left(e^{j\theta_{oi}} \delta(\omega - \omega_i) - e^{-j\theta_{oi}} \delta(\omega + \omega_i) \right) \qquad 2\text{–}11$$

Several signals can be injected into the system, either single tone signal, multi-tone signal or any other arbitrary signal waveform. Although, multi-tone signal provides faster results than single-tone, the spectral power of each tone is smaller compared to a single-tone signal. This is a



(a) (b)

Figure 2-2: Multi-tone signal (a) time-domain waveform (b) magnitude and phase characteristics in frequency domain

direct consequence of the fact that multi-tone has larger crest factor as more tones are incorporated into the signal. Obviously, it is preferable to use more components and to obtain as complete as possible characteristic of the dq impedance/admittance. On the other hand, putting more components increases crest factor, but maximum signal deviation should be sufficiently small, not to perturb the operating point too much. In this way, if more components are used, magnitude of each component has to be decreased, with the potential to reduce signal to down to the noise level. If obtained results are corrupted with the simulation noise, the simulation step needs to be decreased to reduce simulation noise level, consequently increasing signal to simulation noise ratio. The "beauty" of multi-tone signal is in the following facts: it excites only the specified frequency components (tones) as there is no splitting of the energy on tones that are not of interest, complete dq small-signal transfer function characteristics is obtained with just two time domain simulations as frequency sweeping is no longer necessary.

Figure 2-2 (a) shows the time domain waveform of multi-tone signal, which consists of 40 equidistance frequency points in the frequency range 10 Hz-1 kHz. Similarly, Figure 2-2 (b) shows the frequency domain characteristic of the multi-tone signal. The important property of the described multi-tone signal is that it has almost constant crest factor when number of tones in the signal are increasing. The CF of multi-tone signal for different number of tones is shown in Figure 2-3. It can be concluded that CF of multi tone signal converges to the constant value of 1.9 as number of tones is increased. Even if the low number of tones are used in the generation of multi-

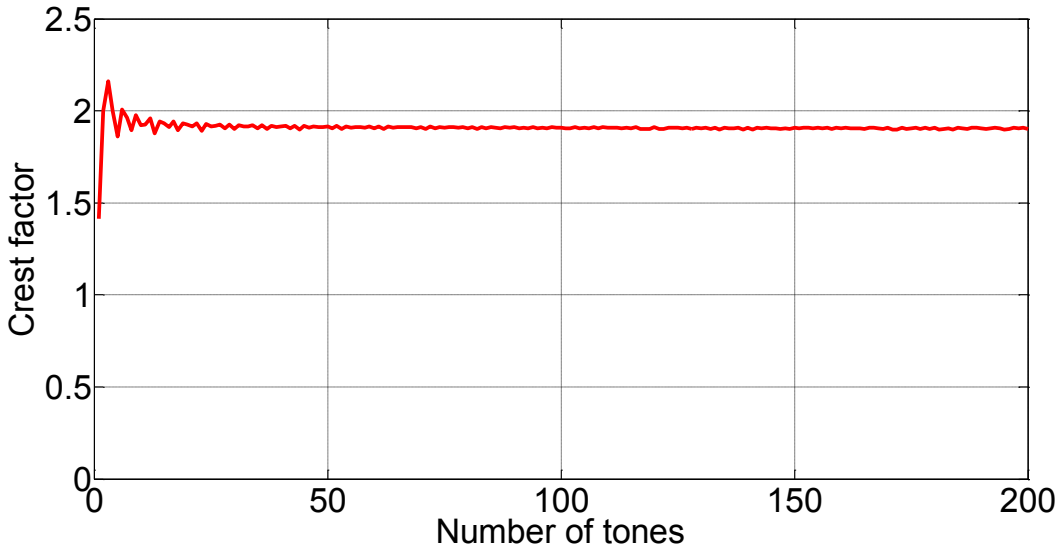


Figure 2-3: Crest factor of the multi tone with respect to the number of frequency points

tone signal, CF of the signal is always lower than 2.2. CF of multi-tone signal is bounded and for the most of the number of tones, CF is equal to 1.9.

2.2.3 Chirp Signal

A chirp signal with linearly increasing frequency is one more potential wide-bandwidth injection signal. The chirp signal with linearly increasing frequency has a constant frequency spectrum in the desired frequency range. Since the chirp signal can be interpreted as a sinusoidal signal with changing frequency, it can be easily generated with switching power electronics converters.

The frequency of the linear chirp signal is changing linearly and it is defined with the following parameters f_0: frequency at the time 0, f_1: frequency at the time T, T is the duration of chirp signal. The equation that describes the frequency of chirp signal is in the form of algebraic equation is given below as.

$$f(t) = f_0 + \frac{f_1 - f_0}{T} t \qquad 2\text{–}12$$

The phase of the chirp signal can be calculated as the integral of the frequency for the arbitrary initial phase θ_o.

$$\theta(t) = 2\pi \int_0^t \left(f_0 + \frac{f_1 - f_0}{T} \tau \right) d\tau + \theta_o = 2\pi \left(f_0 t + \frac{f_1 - f_0}{2T} t^2 \right) + \theta_o \qquad 2\text{–}13$$

Thus, the linear chirp signal cab be written in the following way.

$$x_{chirp}(t) = \begin{Bmatrix} \sin\left(2\pi \left(f_0 t + \frac{f_1 - f_0}{2T} t^2 \right) + \theta_o \right) & 0 < t < T \\ 0 & t > T \end{Bmatrix} \qquad 2\text{–}14$$

A spectrogram is used for a spectral representation of the chirp signal. A spectrogram is a time-varying spectral representation (forming an image) that shows how the spectral density of a signal varies with time. In the field of time–frequency signal processing, it is one of the most popular quadratic Time-Frequency Distribution that represents a signal in a joint time-frequency domain and that has the property of being positive. Also, spectrograms are used to identify phonetic

sounds; and they are commonly used in many other fields including music, sonar/radar, speech processing, seismology, etc.

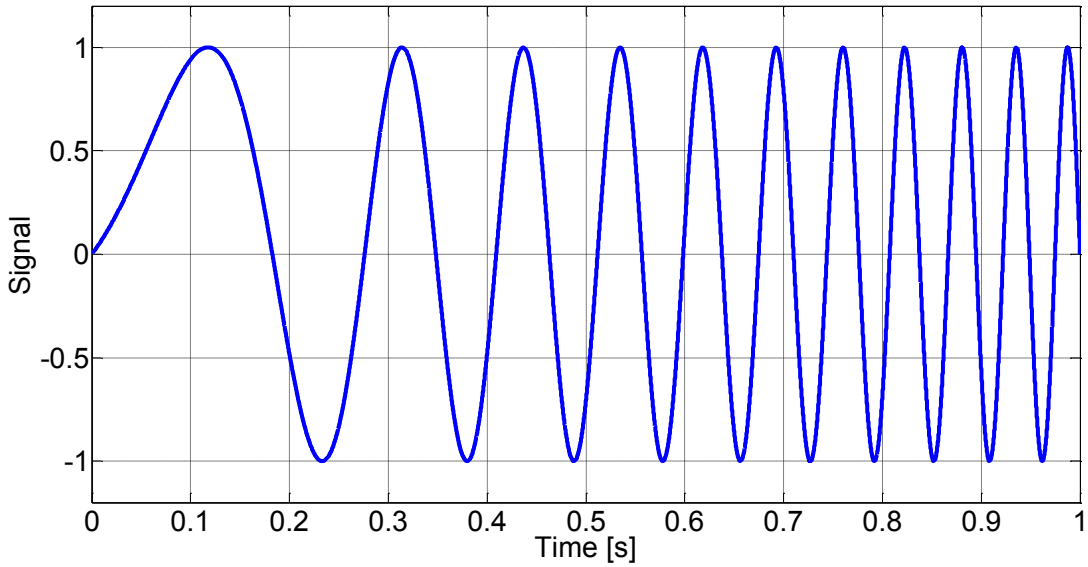


Figure 2-4: Time domain waveform of chirp signal f_0=1, f_1=20, T=1

The most common format is a graph with two dimensions: the horizontal axis represents frequency, the vertical axis is time, a third dimension indicating the amplitude of a particular frequency at a particular time is represented by the intensity or color of each point in the image. Although there are many variations of format: sometimes the vertical and horizontal axes are switched, so time runs up and down; sometimes the amplitude is represented as the height of a 3D surface instead of color or intensity. The frequency and amplitude axes can be either linear or logarithmic, depending on what the graph is being used for. Audio signal engineers would usually represent it with a logarithmic amplitude axis (typical unit is decibels, or dB), and frequency would be linear to emphasize harmonic relationships, or logarithmic to emphasize musical, tonal relationships.

The spectrogram is calculated using Short Time Fourier Transform (STFT), which is in its essence very similar to Welch's estimation method. Digitally sampled data, in time domain, is broken up into chunks, which usually overlap and Fourier transformed is used to calculate the magnitude of the frequency spectrum for each chunk. Braking up the signal into chunks is the same as applying a rectangular window function to the signal. Hence, it is possible to use other window functions as Han, Hamming, Blackman-Harris and others to obtain the spectrogram [120]. Each

chunk then corresponds to a horizontal line in the image; a measurement of magnitude versus frequency for a specific moment in time. The spectrums or time plots are then "laid side by side" to form the image or a three-dimensional surface.

STFT is defined with the following equation

$$X(m,\omega)=\sum_{-\infty}^{+\infty}x[n]\omega[n-m]e^{-j\omega n} \qquad 2\text{–}15$$

A chirp signal waveform in time domain is shown in Figure 2-4. Spectrogram of the chirp signal is easily programmed in software by specifying the length of each “chunk”, the number of overlapping elements, the type of window function, the sampling frequency and other parameters. The spectrogram of the chirp signal obtained in is shown in Figure 2-5.

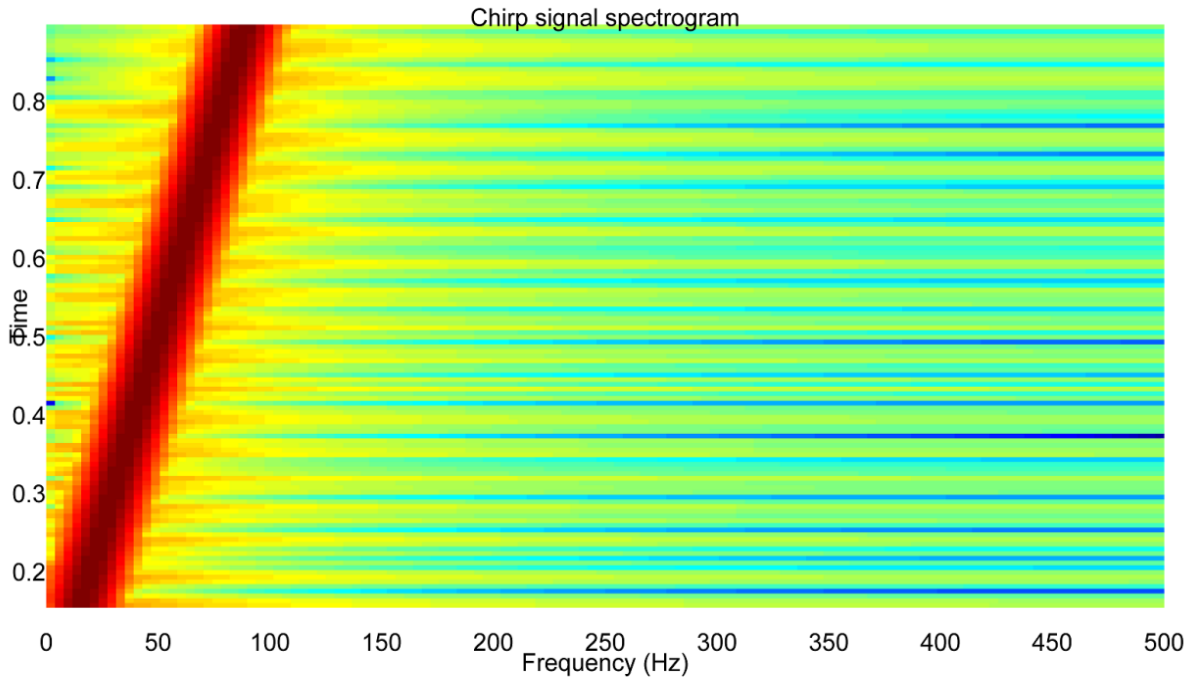


Figure 2-5: Spectrogram of a chirp signal

In similar manner, the frequency domain content of the chirp signal is calculated by applying the Fourier transform as written below.

$$X_{chirp}(j\omega)=\int_{-\infty}^{+\infty}x_{chirp}(t)e^{-j\omega t}dt \qquad 2\text{–}16$$

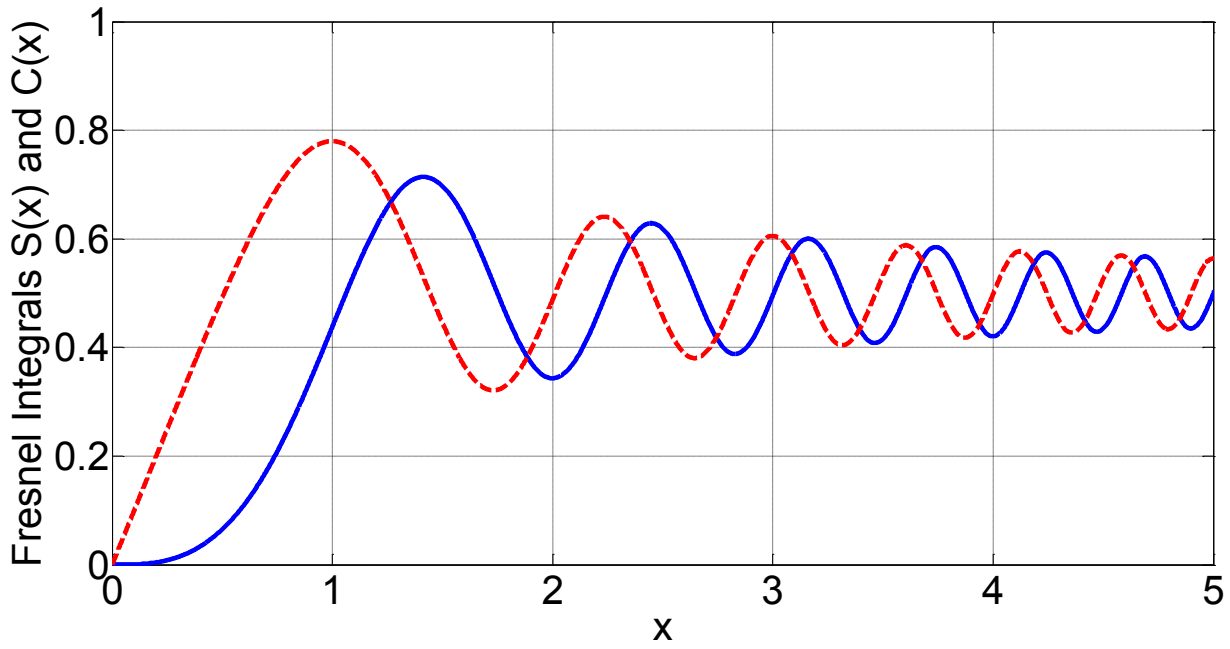


Figure 2-6: Waveforms of Fresnel functions *S*(*x*) (straight blue line) and *C*(*x*) (dashed red line)

After several algebraic manipulations are used, it is possible to get an analytical expression of the Fourier transform of the chirp signal, which consists of Fresnel integrals or Fresnel functions. Analytical expressions of Fresnel functions together with the equivalent power series expansion are given below.

$$S(x)=\int_0^x \sin\left(\frac{\pi}{2}\tau^2\right)d\tau=\sqrt{\frac{2}{\pi}}\sum_{n=0}^{+\infty}(-1)^n\frac{x^{4n+3}}{(2n+1)!(4n+3)} \qquad 2\text{–}17$$

$$C(x)=\int_0^x \cos\left(\frac{\pi}{2}\tau^2\right)d\tau=\sqrt{\frac{2}{\pi}}\sum_{n=0}^{+\infty}(-1)^n\frac{x^{4n+1}}{(2n)!(4n+1)} \qquad 2\text{–}18$$

Signal waveforms of two Fresnel functions *S*(*x*) and *C*(*x*) are shown in Figure 2-6. In order to calculate frequency characteristic of the chirp signal, it is convenient to split the chirp signal into two complex signals as shown below.

$$x_{chirp}(t)=\frac{1}{2j}\left(e^{j\theta_{chirp}(t)}-e^{-j\theta_{chirp}(t)}\right) \qquad 2\text{–}19$$

$$\theta_{chirp}(t)=\omega_0 t+\frac{\Delta\Omega}{2T}t^2+\theta_o \qquad 2\text{–}20$$

$$\Delta\Omega = 2\pi\Delta F = 2\pi\left(f_1 - f_0\right) \quad 2\text{–}21$$

Where the ω_0 is angular frequency of the chirp signal at 0, while the $\Delta\Omega$ is the angular frequency increase at the time t_1. The frequency spectrum of the chirp signal is calculated by applying the Fourier transform on the chirp signal as written below.

$$X_{chirp}(j\omega) = \frac{1}{2j}\left(\int_{-\infty}^{+\infty} e^{j\theta_{chirp}(t)} e^{-j\omega t}\,dt - \int_{-\infty}^{+\infty} e^{-j\theta_{chirp}(t)} e^{-j\omega t}\,dt\right) \quad 2\text{–}22$$

$$X_{chirp1}(j\omega) = \int_{-\infty}^{+\infty} e^{j\theta_{chirp}(t)} e^{-j\omega t}\,dt \quad 2\text{–}23$$

$$X_{chirp2}(j\omega) = \int_{-\infty}^{+\infty} e^{-j\theta_{chirp}(t)} e^{-j\omega t}\,dt \quad 2\text{–}24$$

Fourier transformation of the first complex signal, namely $X_{chirp1}(j\omega)$, is analytically described with the Fresnel functions as.

$$X_{chirp1}(j\omega) = \sqrt{\frac{T}{2\Delta F}} e^{-j\frac{\pi n_1^2}{4}\Delta FT} e^{j\theta_0}\left[\left(C\left(X_2(n_1)\right) - C\left(X_1(n_1)\right)\right) + j\left(S\left(X_2(n_1)\right) - S\left(X_1(n_1)\right)\right)\right] \quad 2\text{–}25$$

$$n_1 = 2\frac{\omega_0 - \omega}{\Delta\Omega} \quad 2\text{–}26$$

$$X_1(n_1) = n_1\sqrt{\frac{\Delta FT}{2}},\ X_2(n_1) = (2 + n_1)\sqrt{\frac{\Delta FT}{2}} \quad 2\text{–}27$$

Similarly, Fourier transformation of the second complex signal, namely $X_{chirp2}(j\omega)$ is analytically described with the Fresnel functions as written below.

$$X_{chirp2}(j\omega) = \sqrt{\frac{T}{2\Delta F}} e^{j\frac{\pi n_2^2}{4}\Delta FT} e^{-j\theta_0}\left[\left(C\left(X_2(n_2)\right) - C\left(X_1(n_2)\right)\right) - j\left(S\left(X_2(n_2)\right) - S\left(X_1(n_2)\right)\right)\right] \quad 2\text{–}28$$

$$n_2 = 2\frac{\omega_0 + \omega}{\Delta\Omega} \quad 2\text{–}29$$

$$X_1(n_2) = n_2\sqrt{\frac{\Delta FT}{2}},\ X_2(n_2) = (2 + n_2)\sqrt{\frac{\Delta FT}{2}} \quad 2\text{–}30$$

Finally, Fourier transformation of the chirp signal is calculated as.

$$X_{chirp}(j\omega)=\frac{1}{2j}\left(X_{chirp1}(j\omega)-X_{chirp2}(j\omega)\right) \qquad 2\text{–}31$$

Analytical expression can be solved using analytical software tools like MATHEMATICA, MATHCAD or numerically in MatLAB. After the implementation of the numerical solution in MatLAB with an ode45 solver function and compared it to the FFT of a sampled chirp signal. A Fourier transform of a chirp signal for different parameter values (f_0, f_1, T) is calculated using the derived expressions. Energy is distributed among the whole spectrum bandwidth and all frequency components can drop to the noise level or even below. This property is not good, because noise can add considerable error to the impedance measurements. In order to get the steady-state response for low frequency components a longer chirp signal is needed, but then the magnitude of the Fourier transform drops down. Therefore, the noise level present in the system determines the duration of the chirp signal and consequently the lowest frequency of the chirp signal. The comparison of magnitude characteristics of three different chirp signals is shown in Figure 2-7. The frequency spectrum of the chirp signal is not a straight line in the injection frequency range. Instead the spectrum contains so called Fresnel ripple, which cannot be eliminated or attenuated as it is the inherent property of the chirp signal spectrum. Furthermore, it can be concluded that if the frequency range of chirp signal is increased, then the signal is equally spread in the whole

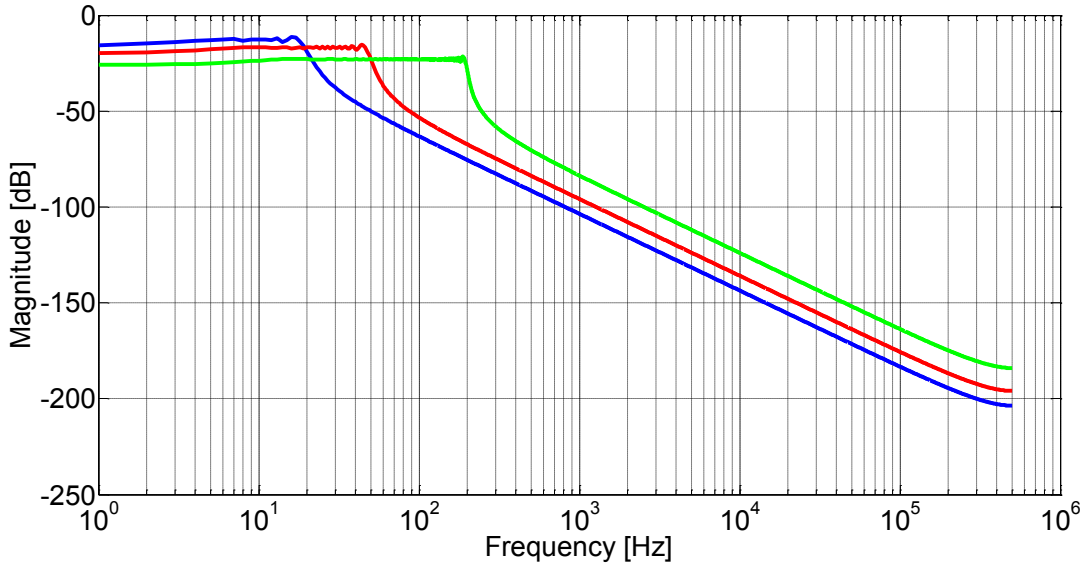


Figure 2-7: Comparison of magnitude characteristics of three chirp signals: f_0=10 Hz, f_1=20 Hz and T=1 s (blue straight line), f_0=10 Hz, f_1=50 Hz and T=1s (red dashed line), f_0=10 Hz, f_1=200 Hz and T=1s (green dotted line)

frequency range, resulting in the lower energy of each spectral component. Nevertheless, the chirp signal can significantly increase the speed of small-signal extraction by injecting a wide frequency range signal into the system. However, if SNR is significantly decreased, the obtained small-signal transfer function results may be severely corrupted with noise, limiting the usefulness of the obtained results.

2.3 Implementation of FFT Algorithm in Simulations

The small-signal impedance extraction based on FFT algorithm has been implemented in MATLAB/Simulink software with the use of SimPowerSystems toolbox. MATLAB has been selected with SimPowerSystems toolbox as it offers several different solvers and it is commonly used software tool for the time-domain simulations of switching power converter circuits. In this way, different wide-bandwidth signals can be tested and compared to the ideal sinusoidal signal. The small-signal frequency-domain analysis is developed as an automated tool for the switching simulation models, which can be used on arbitrary switching models of power electronics converters. Furthermore, the presented small-signal frequency analysis is general and can be used to extract other transfer functions of interest as loop gain, dc impedance, audio susceptibility, etc…

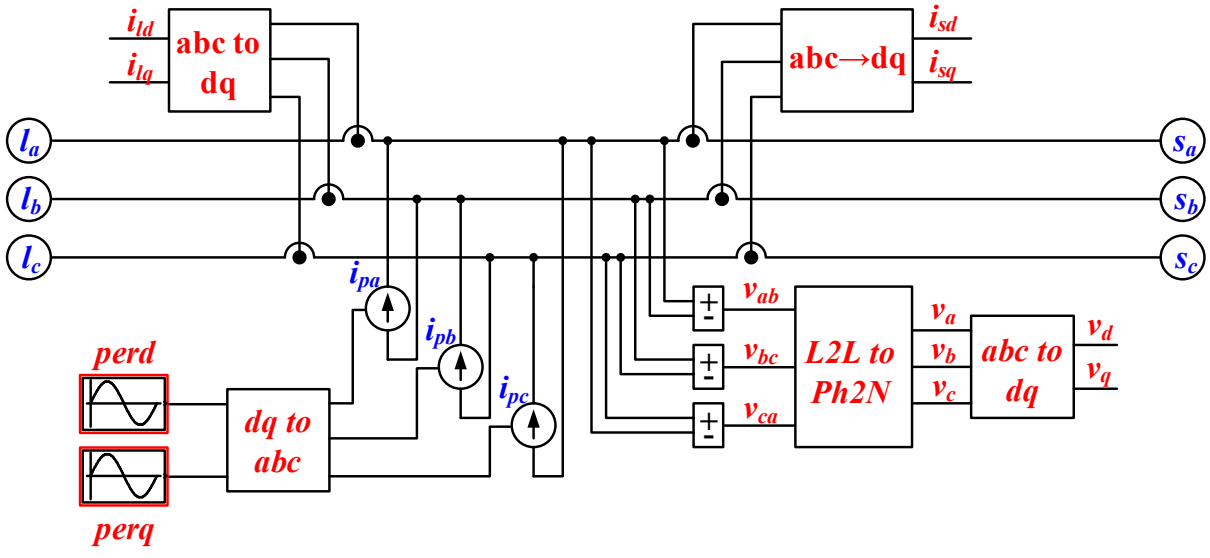


Figure 2-8: Shunt current injection dq measurement block, which provides phase to phase dq impedances

Several types of the impedance identification blocks are built and included into simulink library browser. The purpose of the developed blocks is to perturb the system and collect steady-state responses of voltages and currents, which will be post-processed. The developed blocks can identify either dq or dc impedances, inject multi-tone, chirp or single-tone signal, do shunt or series injection, include inner PLL for phase tracking or have separate phase input port. Moreover, either phase to neutral or phase to phase dq impedances can be identified by dq impedance identification blocks.

2.3.1 Shunt Current Injection of dq Signals via Three-Phase Source

Figure 2-8 shows schematic of shunt current injection block, suitable for characterization of three-phase AC system in dq coordinates with the phase to neutral variables. The dq currents are injected via ideal three-phase current source. In order to characterize dq impedances it is necessary to sense source and load currents and voltages in abc coordinates at the three-phase interface. Three-phase currents and voltages are then transformed to dq coordinates using the following dq transformation.

$$T_{dq}(\theta)=\frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right) \end{bmatrix} \qquad 2\text{–}32$$

During the first perturbation, injection signal is injected via d-coordinate $perd(t)=x(t)$, while q-coordinate injection signal is equal to zero $perq(t)=0$. When the first perturbation is being injected into the power system, the following expression connects dq impedance matrix with the corresponding voltage and current responses.

$$\begin{bmatrix} v_{d1}(s) \\ v_{q1}(s) \end{bmatrix}=\begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix}\begin{bmatrix} i_{sd1}(s) \\ i_{sq1}(s) \end{bmatrix} \qquad 2\text{–}33$$

$$\begin{bmatrix} v_{d1}(s) \\ v_{q1}(s) \end{bmatrix}=\begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix}\begin{bmatrix} i_{ld1}(s) \\ i_{lq1}(s) \end{bmatrix} \qquad 2\text{–}34$$

On the other hand, during the second perturbation, injection signal is injected via q-coordinate $perq(t)=x(t)$, while d-coordinate injection signal is set to zero, $perd(t)=0$. In this way, two sets of

independent vector responses are obtained, which can be used in the identification of dq impedance matrix.

$$\begin{bmatrix} v_{d2}(s) \\ v_{q2}(s) \end{bmatrix} = \begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} \begin{bmatrix} i_{sd2}(s) \\ i_{sq2}(s) \end{bmatrix} \quad 2\text{–}35$$

$$\begin{bmatrix} v_{d2}(s) \\ v_{q2}(s) \end{bmatrix} = \begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} \begin{bmatrix} i_{ld2}(s) \\ i_{lq2}(s) \end{bmatrix} \quad 2\text{–}36$$

Combining previous two equations, the following expression is obtained.

$$\begin{bmatrix} v_{d1}(s) & v_{d2}(s) \\ v_{q1}(s) & v_{q2}(s) \end{bmatrix} = \begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} \begin{bmatrix} i_{sd1}(s) & i_{sd2}(s) \\ i_{sq1}(s) & i_{sq2}(s) \end{bmatrix} \quad 2\text{–}37$$

$$\begin{bmatrix} v_{d1}(s) & v_{d2}(s) \\ v_{q1}(s) & v_{q2}(s) \end{bmatrix} = \begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} \begin{bmatrix} i_{ld1}(s) & i_{ld2}(s) \\ i_{lq1}(s) & i_{lq2}(s) \end{bmatrix} \quad 2\text{–}38$$

Finally, the source and load dq impedance matrices are expressed as a ratio of voltage and current matrices.

$$\begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} = \begin{bmatrix} v_{d1}(s) & v_{d2}(s) \\ v_{q1}(s) & v_{q2}(s) \end{bmatrix} \begin{bmatrix} i_{sd1}(s) & i_{sd2}(s) \\ i_{sq1}(s) & i_{sq2}(s) \end{bmatrix}^{-1} \quad 2\text{–}39$$

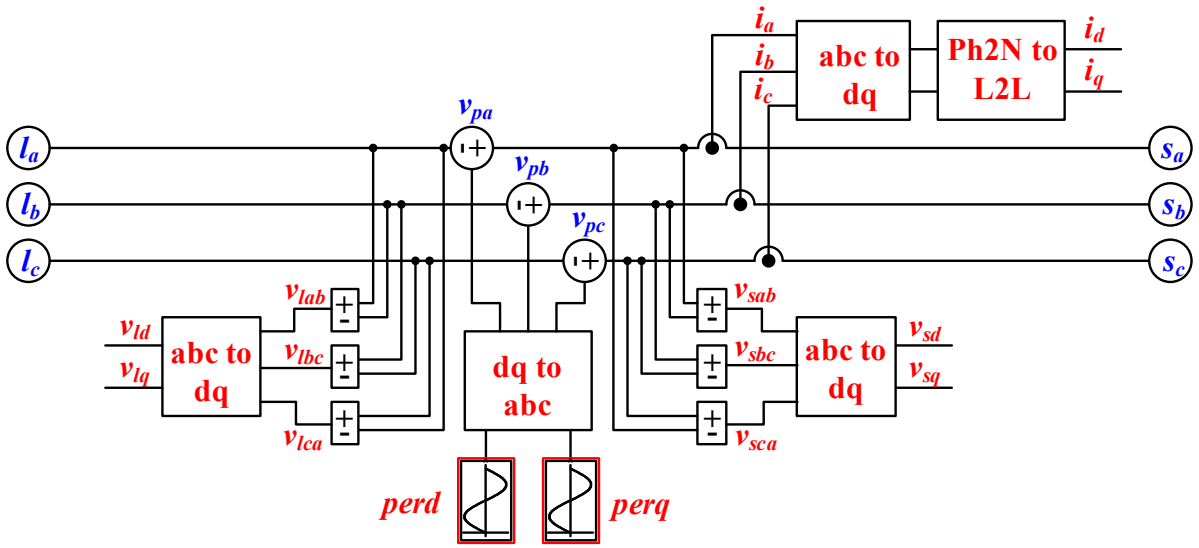


Figure 2-9: Series voltage injection dq measurement block, which provides phase to neutral dq impedances

$$\begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} = \begin{bmatrix} v_{d1}(s) & v_{d2}(s) \\ v_{q1}(s) & v_{q2}(s) \end{bmatrix} \begin{bmatrix} i_{ld1}(s) & i_{ld2}(s) \\ i_{lq1}(s) & i_{lq2}(s) \end{bmatrix}^{-1} \quad 2\text{–}40$$

2.3.2 Series Voltage Injection of dq Components via Three-Phase Source

Furthermore, series voltage injection block, suitable for characterization of three-phase ac power system in dq coordinates with the phase to phase variables is also shown in Figure 2-9.

During the first perturbation the injection signal is injected via d-coordinate, $perd(t)=x(t)$, while q-coordinate injection signal is equal to zero $perq(t)=0$. Similarly, like in the previous case, when the first perturbation is being injected into the power system, the following expression connects dq impedance matrix with voltage and current responses.

$$\begin{bmatrix} v_{sd1}(s) \\ v_{sq1}(s) \end{bmatrix} = \begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} \begin{bmatrix} i_{d1}(s) \\ i_{q1}(s) \end{bmatrix} \quad 2\text{–}41$$

$$\begin{bmatrix} v_{ld1}(s) \\ v_{lq1}(s) \end{bmatrix} = -\begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} \begin{bmatrix} i_{d1}(s) \\ i_{q1}(s) \end{bmatrix} \quad 2\text{–}42$$

In a same manner, during the second perturbation, the following expression can be written.

$$\begin{bmatrix} v_{sd2}(s) \\ v_{sq2}(s) \end{bmatrix} = \begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} \begin{bmatrix} i_{d2}(s) \\ i_{q2}(s) \end{bmatrix} \quad 2\text{–}43$$

$$\begin{bmatrix} v_{ld2}(s) \\ v_{lq2}(s) \end{bmatrix} = -\begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} \begin{bmatrix} i_{d2}(s) \\ i_{q2}(s) \end{bmatrix} \quad 2\text{–}44$$

Combining previous two responses to perturbations via d-coordinate and q-coordinate, the following expressions for the source and load dq impedances are obtained.

$$\begin{bmatrix} Z_{sdd}(s) & Z_{sdq}(s) \\ Z_{sqd}(s) & Z_{sqq}(s) \end{bmatrix} = \begin{bmatrix} v_{sd1}(s) & v_{sd2}(s) \\ v_{sq1}(s) & v_{sq2}(s) \end{bmatrix} \begin{bmatrix} i_{d1}(s) & i_{d2}(s) \\ i_{q1}(s) & i_{q2}(s) \end{bmatrix}^{-1} \quad 2\text{–}45$$

$$\begin{bmatrix} Z_{ldd}(s) & Z_{ldq}(s) \\ Z_{lqd}(s) & Z_{lqq}(s) \end{bmatrix} = -\begin{bmatrix} v_{ld1}(s) & v_{ld2}(s) \\ v_{lq1}(s) & v_{lq2}(s) \end{bmatrix} \begin{bmatrix} i_{d1}(s) & i_{d2}(s) \\ i_{q1}(s) & i_{q2}(s) \end{bmatrix}^{-1} \quad 2\text{–}46$$

The series voltage perturbation excites the system in a dual way compared to the shunt perturbation case. The majority of the perturbation excites large impedance, providing sufficient

excitation to one side. On the other hand, the voltage and current responses of small impedance side may be very small, resulting in inaccurate impedance identification.

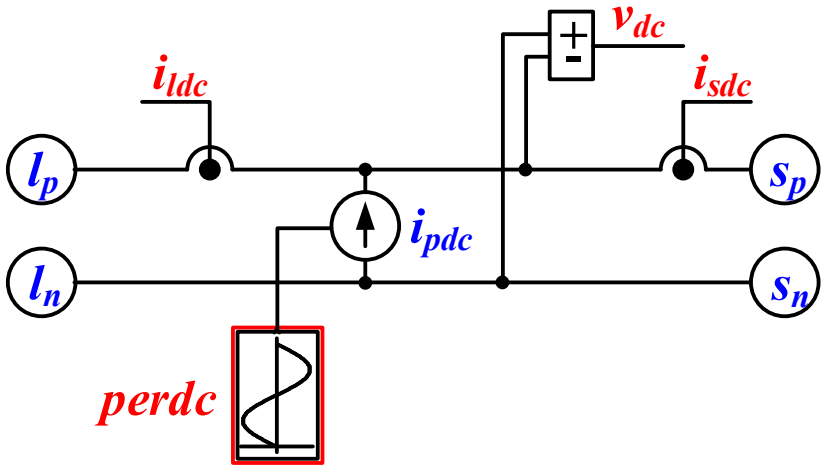


Figure 2-10: Shunt current injection dc measurement block

2.3.3 Shunt Current and Series Voltage Injection Blocks into DC systems

The schematics of shunt current injection block for the impedance estimation of dc power system is shown in Figure 2-10. In this case, only a single perturbation signal is necessary to perform the identification of the source and load impedances.

In this case, dc impedances are identified via the simple expressions as shown below.

$$Z_{sdc}(s)=\frac{v_{dc}(s)}{i_{sdc}(s)} \qquad 2\text{–}47$$

$$Z_{ldc}(s)=\frac{v_{dc}(s)}{i_{ldc}(s)} \qquad 2\text{–}48$$

Furthermore, the schematics of series voltage injection block for the impedance estimation of dc power system is shown in Figure 2-11. In a dual manner, the source and load impedances in this case are identified using the following expressions.

$$Z_{sdc}(s)=\frac{v_{sdc}(s)}{i_{dc}(s)} \qquad 2\text{–}49$$

$$Z_{ldc}(s)=-\frac{v_{ldc}(s)}{i_{dc}(s)} \qquad 2\text{–}50$$

In the case that dq and dc admittances are of interest for the stability analysis, the admittances can be calculated via the inversion of impedances.

$$Y_{dq}(s) = Z_{dq}^{-1}(s); \tag{2–51}$$

$$Y_{dc}(s) = Z_{dc}^{-1}(s) = \frac{1}{Z_{dc}(s)} \tag{2–52}$$

All the developed blocks are easily used with an arbitrary power converter switching simulation model and used to identify source and load dq or dc impedances/admittances.

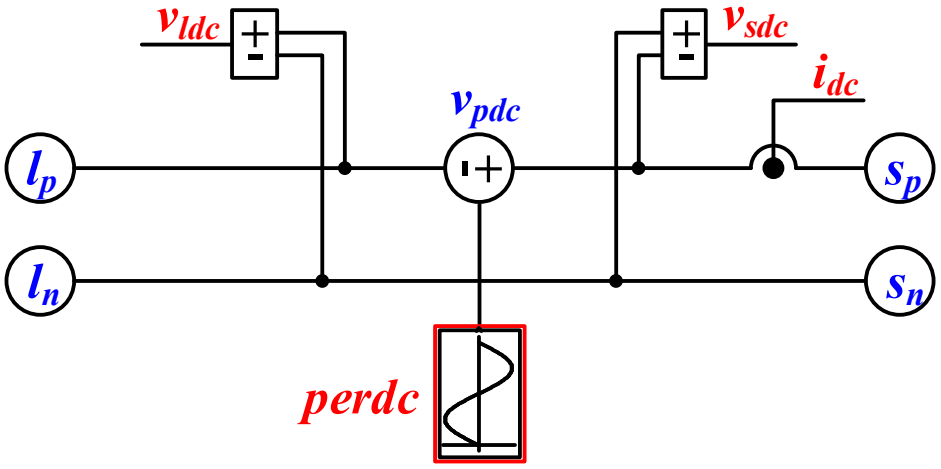


Figure 2-11: Series voltage injection dc measurement block

2.3.4 FFT Algorithm

In order to characterize the small-signal transfer functions values at arbitrary frequency points, the small-signal perturbation is injected into the simulation model via the developed blocks. The assumption is that the model has well defined dc operating point and that small-signal injection would not change the operating condition. The dc operating point of the three-phase voltage source converters is defined in dq coordinates.

FFT has been used to provide magnitude and phase of the current and voltage variables at the injection frequency points. In order to obtain correct results with FFT algorithm, several conditions need to be satisfied. The equidistant sampling is applied with high sampling frequency equal to 1 MHz. Furthermore, MATLAB models can be easily set to produce time specified output and the solver would choose step size automatically to fit absolute and relative error requirements. Interpolating techniques are not used as it is found that they increase error in the model.

The response due to the injection has to be settled before FFT is applied and the length of data window on which FFT is applied has to be large enough to capture all the frequency components present in the signal. In this way, window leakage is prevented and accurate results are obtained.

The tool is further automated in the following ways. The blocks are masked and user can set couple convenient parameters: start injection frequency, end injection frequency, number of frequency points between the start and end injection frequency, injection magnitude and frequency resolution. The user should also provide values for line frequency and response time of the model. The response time of simulation model is equal to time necessary for the model to reach steady-state from the arbitrary initial condition. The tool will wait for the response time for the variables to settle and then FFT is applied. In this way a brute force method for the identification is applied and automated, resulting in accurate and slow identification process. If pure sinusoidal signal is injected, then both linear and nonlinear systems can be successfully characterized. Control of the simulation model and post-processing of the collected data are performed using m-file. Furthermore, all the injection blocks are parameterized and incorporated into the Simulink library, providing a flexible and easy usable blocks.

The most important part in frequency-domain analysis using the small-signal injection is to select appropriate solver. MATLAB software offers large number of different solvers, but only certain solvers yield correct analysis results. The most suitable solvers for power converters switching models are variable-step stiff solvers. Four different stiff solvers are incorporated in MATLAB:

- ode15s
- ode23s
- ode23t
- ode23tb

It has been found that preferable solver is ode23t as it gives fast and accurate small-signal analysis results. The explanation is that ode23t solver does not have numerical damping as other three solvers. Of course, other three solvers can give correct results if maximum simulation step is decreased, thus effectively reducing numerical damping present in the solver. The price paid by decreasing simulation step is increased time to obtain correct small-signal analysis results.

In order to perform dq analysis it is necessary to provide phase for the dq transformation block inside the developed impedance extraction blocks. One possible solution is to implement a synchronous reference frame PLL (SRF PLL) with center frequency reference as shown in [106], [107]. It consists of phase detector low-pass filter and integrator, providing phase at the output. The dq transformation coefficient is selected to be 2/3, so that gain of the phase detector (PD) is equal to the voltage magnitude V_m.

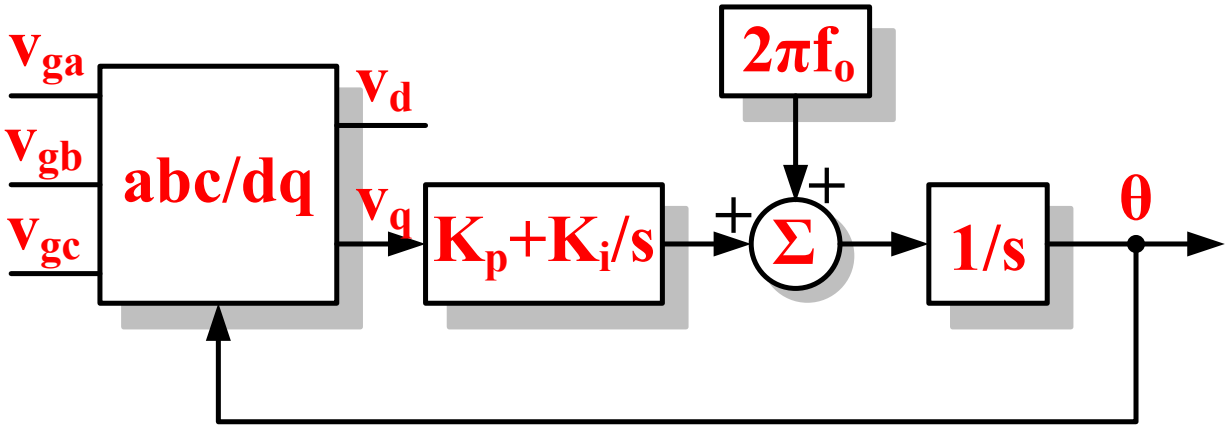


Figure 2-12: Block diagram of the realized SRF PLL block

Figure 2-12 shows block diagram schematic of the realized SRF-PLL, while Figure 2-13 shows equivalent linearized model of SRF PLL. The derivation of linearized model for SRF PLL and analysis of different PLLs is shown in [92]-[93].

The loop gain expression of SRF PLL is derived from the equivalent linearized model as.

$$T_{PLL} = V_m \frac{1}{s}\left(K_p + \frac{K_i}{s}\right) \qquad 2\text{–}53$$

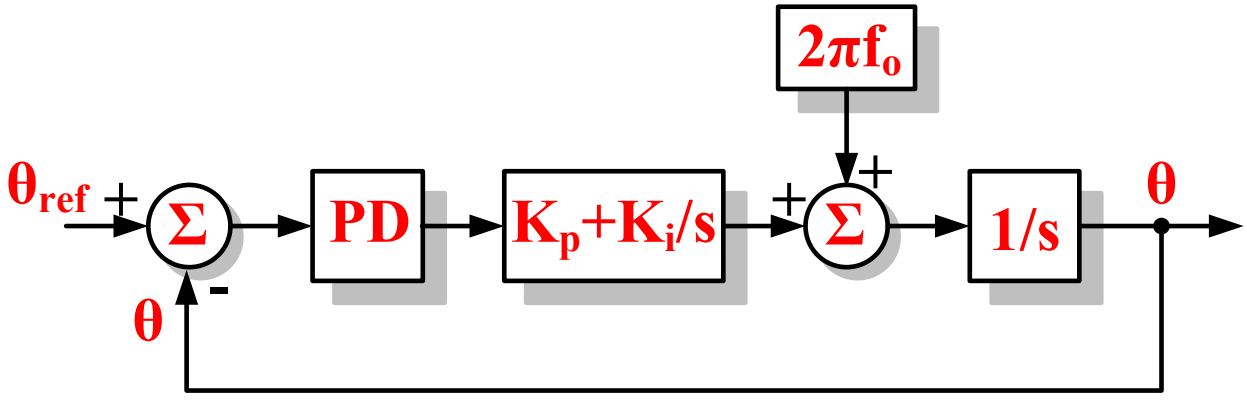


Figure 2-13: Block diagram of the linearized model of SRF PLL

In some cases, it is necessary to have PLL at the interface point for the phase extraction. In this case, PLL needs to have lower bandwidth than the lowest injection frequency to minimize its influence on the extraction process. Although low bandwidth PLL is not a part of the model being investigated, it would slow the response of the complete simulation model, which is not desirable. PLL is just added into to model to provide a phase to dq transformation blocks inside the dq impedance extraction block. Hence, PLL should not slow down the impedance identification process. Therefore, PLL implementation is left optional in the tool, it can be either included into the block or phase can be generated in the model itself and then provided as input to the dq impedance extraction block.

Filtering of the source and load currents to prevent anti-aliasing effect, which is usually done in the hardware, is not necessary. If sampling is high enough, which is implemented in the tool, there is no need for low-pass or band-pass filters. We have investigated the possibility to include either low-pass filter that would have a bandwidth slightly higher than the highest injection frequency, but it only introduces additional states and makes simulation model more complicated and it takes longer time to obtain simulation results. Similarly, we have tried to include band-pass filter, centered on the injection frequency, but again the final conclusion is that the simulation model would have more states and it would be more complicated to simulate. Furthermore, narrow band-pass filter has slow response, so it would further increase simulation time and burden the whole simulation model. Therefore, high frequency sampling of responses is implemented solely, without any prior filtering.

2.4 Application Examples

Two application examples are presented in this section. Three-phase two-level VSI with inner current control and outer voltage control feeding a resistive load is used as the first application example. The effectiveness of the extraction tool is verified on the switching simulation model with digital control implemented and dead-time included. The incorporated dead-time would affect the small-signal dq impedances, which is successfully captured via the tool.

The second application example is a three-phase two-level boost rectifier with inner current loop and dc voltage outer loop controls implemented as digital controllers. In this case, the effect

of dead-time on dq impedances is successfully captured via the extraction tool. Furthermore, SRFPLL is used in the model, affecting the small-signal dq impedances of the rectifier via the q-channel [111]. In this case, PLL effects on small-signal dq impedances are successfully captured via the extraction tool.

2.4.1 Three-Phase Voltage Source Inverter Feeding a Resistive Load

Three-phase VSI typically used in aerospace application is chosen as the first test case. The parameters of the used inverter are given in Table 2-1. After applying averaging concept presented in [18], a classical dq averaged model of three-phase VSI is obtained. The circuit schematics of both switching and classical dq averaged models are shown in Figure 2-14 and Figure 2-15. The three-phase VSI is supplied with a dc source, whose dc impedance is modeled with an LC low pass filter. On the ac side there is a three-phase LC filter, whose main purpose is to filter switching harmonics generated by the switching converter. The three-phase resistive load is supplied by capacitor voltages. The three-phase capacitor voltages are regulated in dq coordinates via the implemented outer voltage loop, while the three-phase inductor currents are regulated in dq coordinates via the inner current loop.

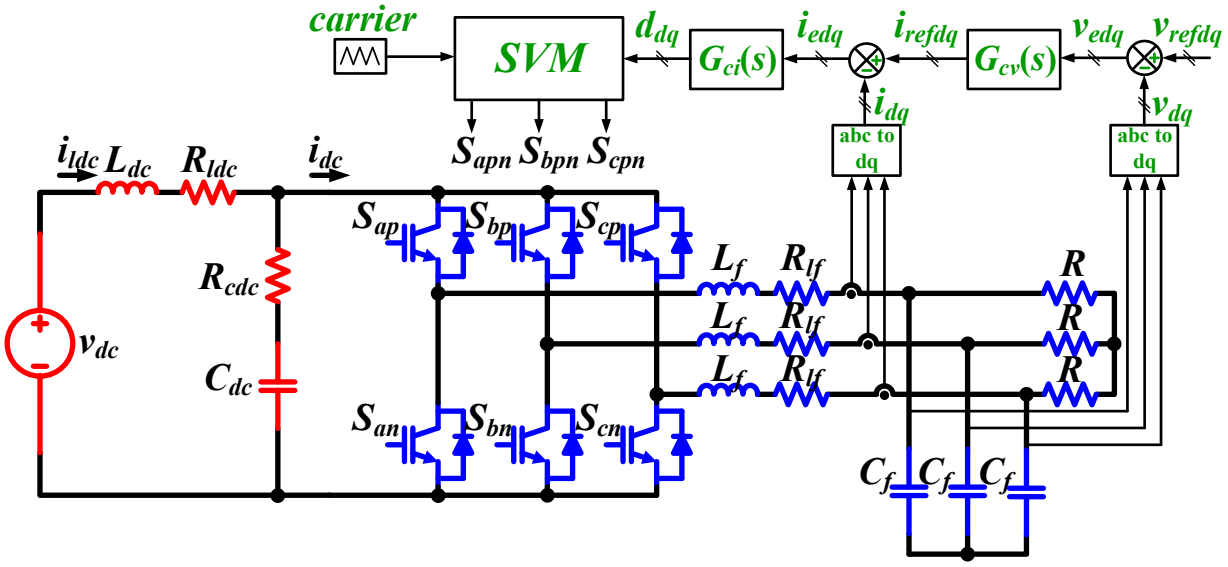


Figure 2-14: Switching model schematic of three-phase VSI

The developed impedance identification algorithm together with the developed injection blocks are used to determine dq and dc impedances from the switching simulation models. In addition, dq and dc impedances from the averaged model are obtained by the linearization as this

model has well defined dc operating point. Furthermore, linearization tool based on calculating a Jacobian of dc model is implemented in MATLAB, and used to calculate small-signal impedances from the averaged models.

Table 2-1 Parameters of three-phase VSI

DC voltage	V_{dc}=300 V	Modulation	CSVM
AC inductor	L_f=180 μH	Control	Current and voltage
Load	R=7 Ω	Dead-time	2 μs
DC inductor	L_{dc}=80 μH	DC capacitor	C_{dc}=40 μF
Switching frequency	f_{sw}=20 kHz	Line frequency	f=400 Hz
PI current loop parameters	k_{pi}=0.014; k_{ii}=175;	Current loop bandwidth	f_i=1000 Hz
PI voltage loop parameters	k_{pv}=0.021; k_{iv}=200;	Voltage loop bandwidth	f_v=200 Hz

Space vector modulation (SVM) with natural sampling is implemented, although other possibility is to implement sinusoidal pulse width modulation with third harmonic injection. Current controller in dq coordinates with an integrator, one zero, two poles, decoupling between d and q coordinates and anti-wind up is implemented to regulate current delivered to the resistive load. The voltage controller is implemented as a PI controller, providing the regulation of capacitor voltages.

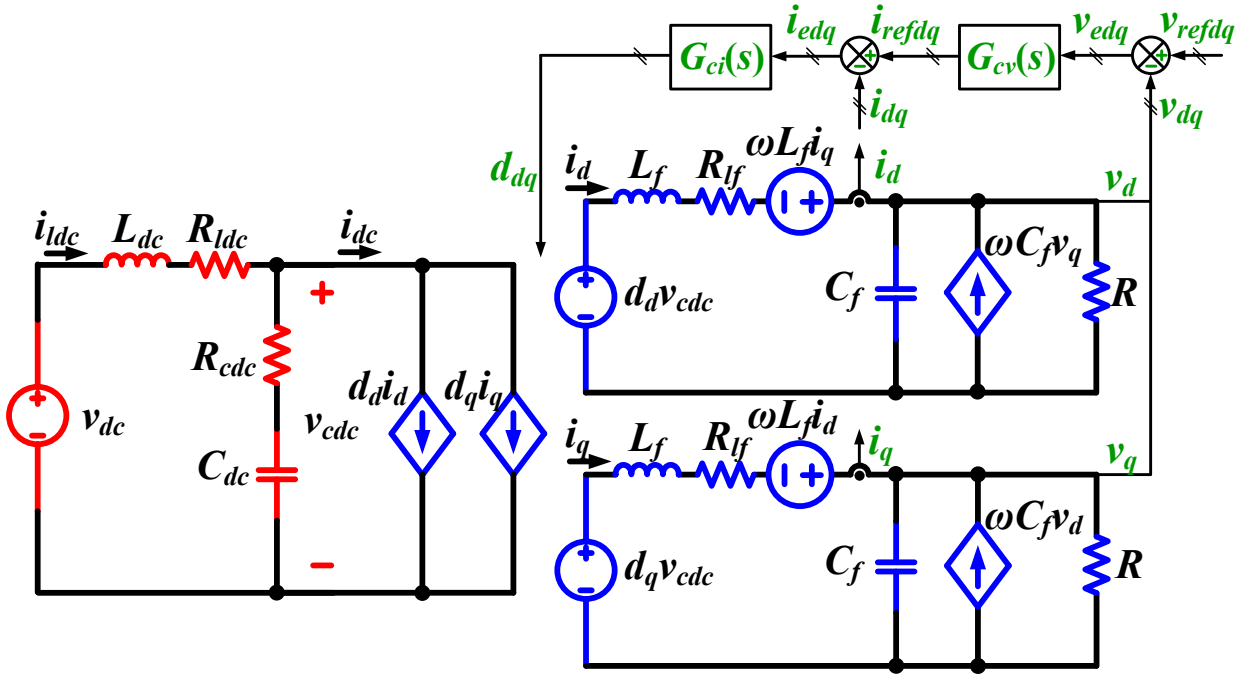
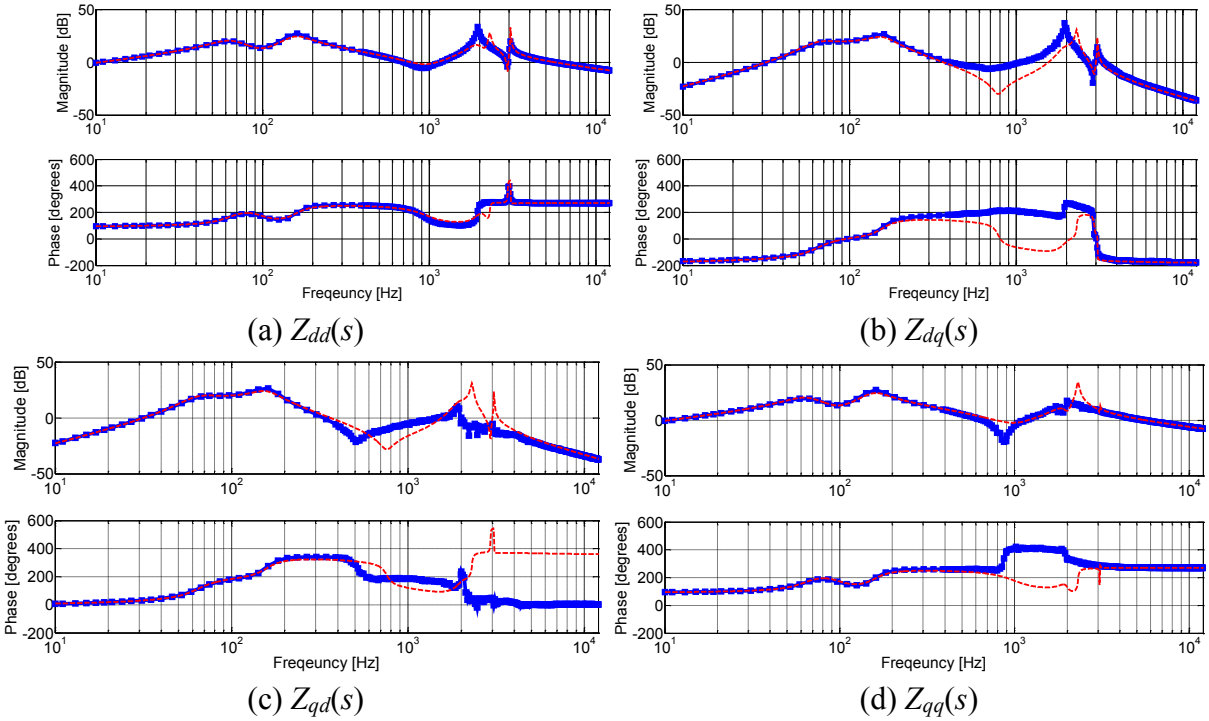


Figure 2-15: Equivalent dq averaged model schematic of three-phase VSI

The VSI small-signal dq impedances are obtained from the switching simulation model by running time domain simulations. In each simulation, a small-signal perturbation is being injected, and small-signal impedances are obtained by applying FFT on the settled responses.

The multi-tone signal is injected into the set-up under test in the frequency ranges around the six times the line frequency (10 Hz-396 Hz, 404 Hz-2396 Hz, 2405 Hz-4795 Hz, 4805 Hz-7195 Hz, 7205 Hz-9595 Hz, 9605-11995 kHz). In each of the six frequency chunks, the multi-tone signal will consist of 30 different frequency tones. Therefore, the small-signal dq impedances are extracted at the total of 280 frequency points. It takes about 90 minutes on a contemporary standard PC computer to perform time-domain simulations and extract dq source and load small-signal impedances.

The small-signal dq impedances of three-phase VSI are extracted from the classical dq averaged model and compared to the dq impedances identified from the switching simulation model as shown in Figure 2-16. The small-signal dq impedances of the controlled three-phase VSI are identified in the frequency range from 10 Hz to 12 kHz. The low frequency part of the VSI



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

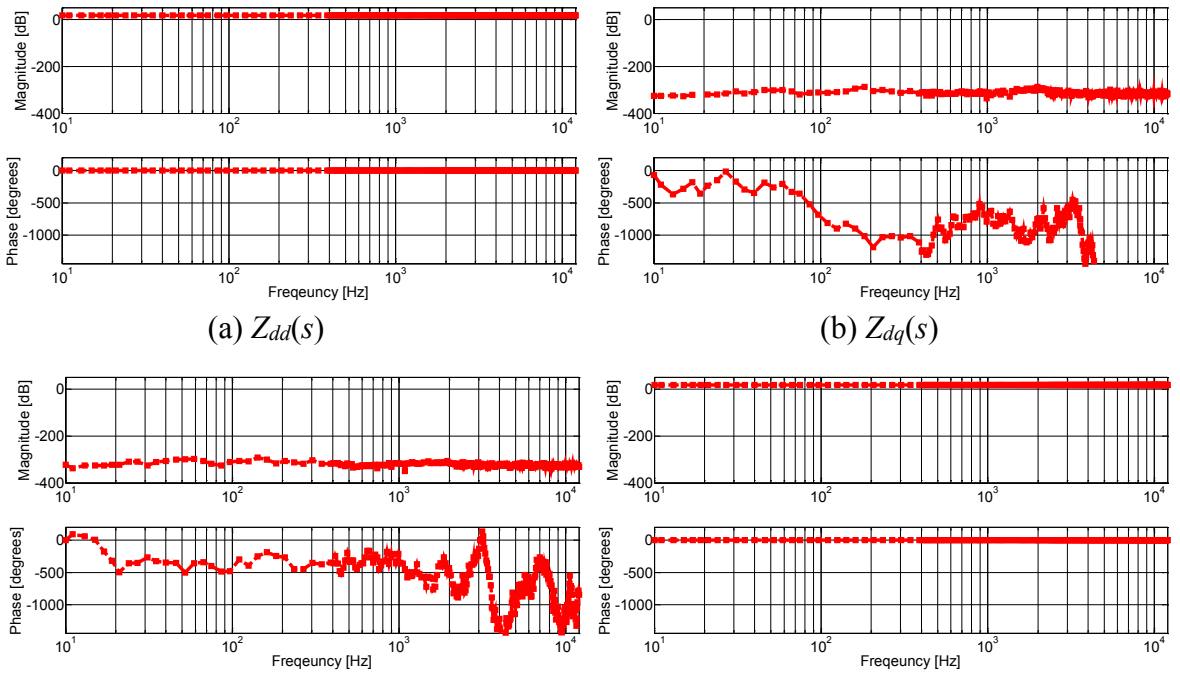
(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 2-16: Comparison of VSI output dq impedances obtained by switching model (squared blue line) and dq averaged model (dashed red line) (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

impedances are shaped via the used voltage and current control, while the high frequency part of VSI dq impedances match with the open-loop VSI impedances. Furthermore, the resonances present in the circuit due to LC filters are accurately captured as impedances are extracted at the sufficient number of frequency points.

If the dead-time is not included, switching model yields same results as dq averaged model. On the other hand if the dead-time is set to 2μs, switching model provides results with resistive damping on impedance $Z_{qq}(s)$. The modeling of dead-time effect on three-phase VSI with different SVM techniques is presented in [94]. In addition, the parametric study of the dead-time effect on the small-signal dq impedances of three-phase VSI is presented in [95].

Similarly, the same dq impedance characteristics is obtained with the injection of sinusoidal (single-tone) signal. The sinusoidal signal is swept from 10 Hz to 10 kHz in 60 equidistant points and injected into the three-phase simulation model. In this case, source and load dq impedances are obtained in about 900 minutes. Comparatively, the achieved speed improvement of the impedance extraction when multi-tone signal is used, is greater than 20 times.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 2-17: Bode diagram of load impedances in dq coordinates (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

In order to perform the stability analysis, both source and load dq impedances are necessary. The load small-signal dq impedances are successfully extracted as well. The obtained small-signal dq impedance of the resistive load is shown in Figure 2-17. The three phase resistive load impedance in dq coordinates is described with the following expression.

$$Z_{rdq}(s)=\begin{bmatrix} R & 0 \\ 0 & R \end{bmatrix} \qquad 2\text{–}54$$

The matching in the low frequency part can be explained with the ability of the average model to capture switching model behavior in the low frequency range. The high-frequency range dq impedance is equal to the open-loop dq impedance as control does not regulate converter effectively at the frequencies higher than the control loop bandwidths. Therefore, both switching model and average model predict high-frequency small-signal dq impedances accurately.

2.4.2 Three-Phase Voltage Source Rectifier

Three-phase two-level voltage source rectifier (VSR) for aerospace application is used as a second test case. The parameters of the used two-level boost rectifier model are given in Table 2-2. The inner current loop regulates the current drawn by the rectifier, providing the high power

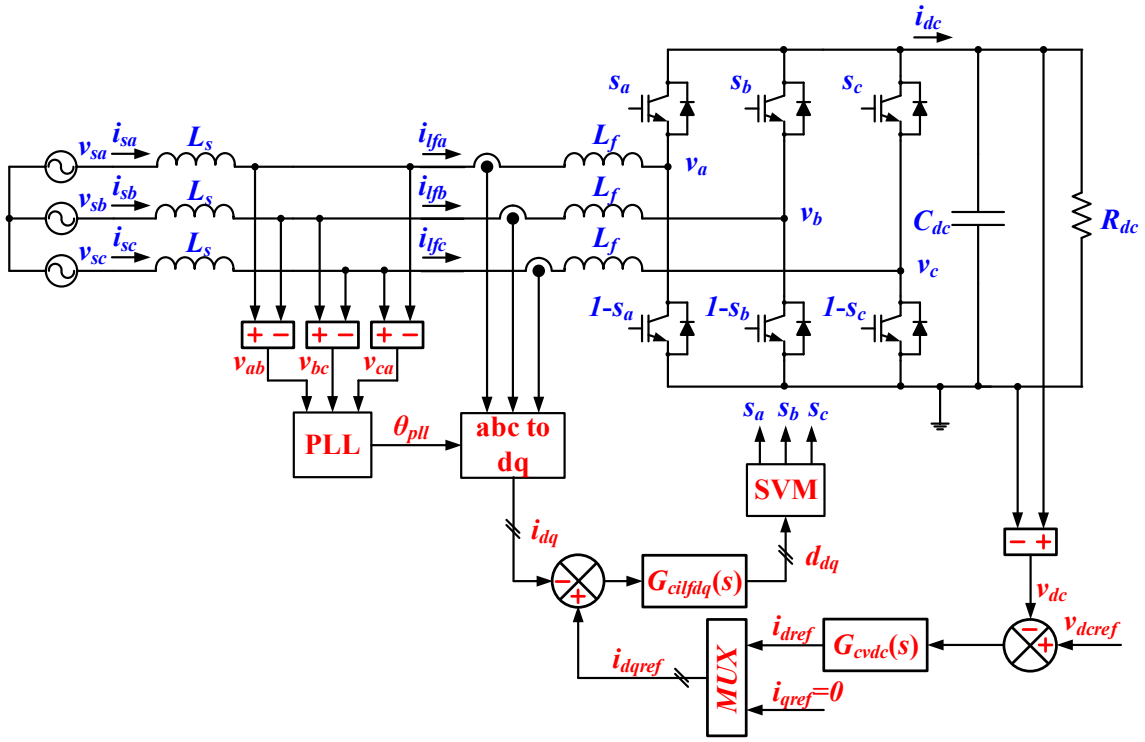


Figure 2-18: Switching model schematic of three-phase boost rectifier

factor. The outer voltage loop regulates the dc voltage and provides the d channel reference for the inner current loop. In this way the input active power is related to the output power delivered to the resistive load. The circuit schematic of the implemented three-phase two-level VSR feeding a resistive load is shown in Figure 2-18.

Table 2-2 Parameters of three-phase boost rectifier

DC voltage	V_{dc}=400 V	Modulation	CSVM
Output inductor	L_f=0.4 mH	Control	Current and voltage loop
Resistive load	R=40 Ω	DC capacitor	C_{dc}=300 μF
Switching frequency	f_{sw}=20 kHz	Line frequency	f=400 Hz
PI current loop	k_{pi}=0.028, k_{ii}=2.33	Current loop bandwidth	f_i=500 Hz
PI voltage loop	k_{pv}=0.031, k_{iv}=13.96	Voltage loop bandwidth	f_v=100 Hz
SRF PLL bandwidth	f_{pllbw}=20 Hz	Output power	P_{out}=4 kW
RMS of voltage source	V_{srms}=120 V	Source inductor	L_s=0.1 mH

The averaged model schematics are shown in and Figure 2-19. The dq impedance of the switching model is obtained via single-tone and multi-tone injection and dq impedance of average model is obtained by the linearization. Bode plots of obtained input dq impedances of three-phase boost rectifier are presented in Figure 2-20. The small-signal dq impedance obtained from the classical dq averaged model is shown in red dashed line, while the blue line with squares represents dq impedance results obtained from the switching simulation models.

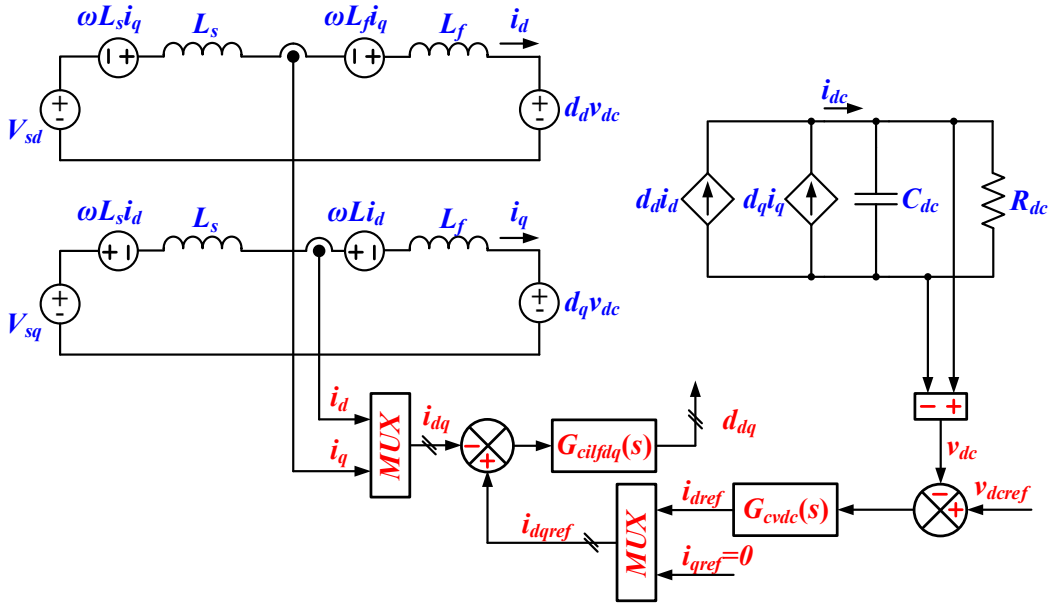
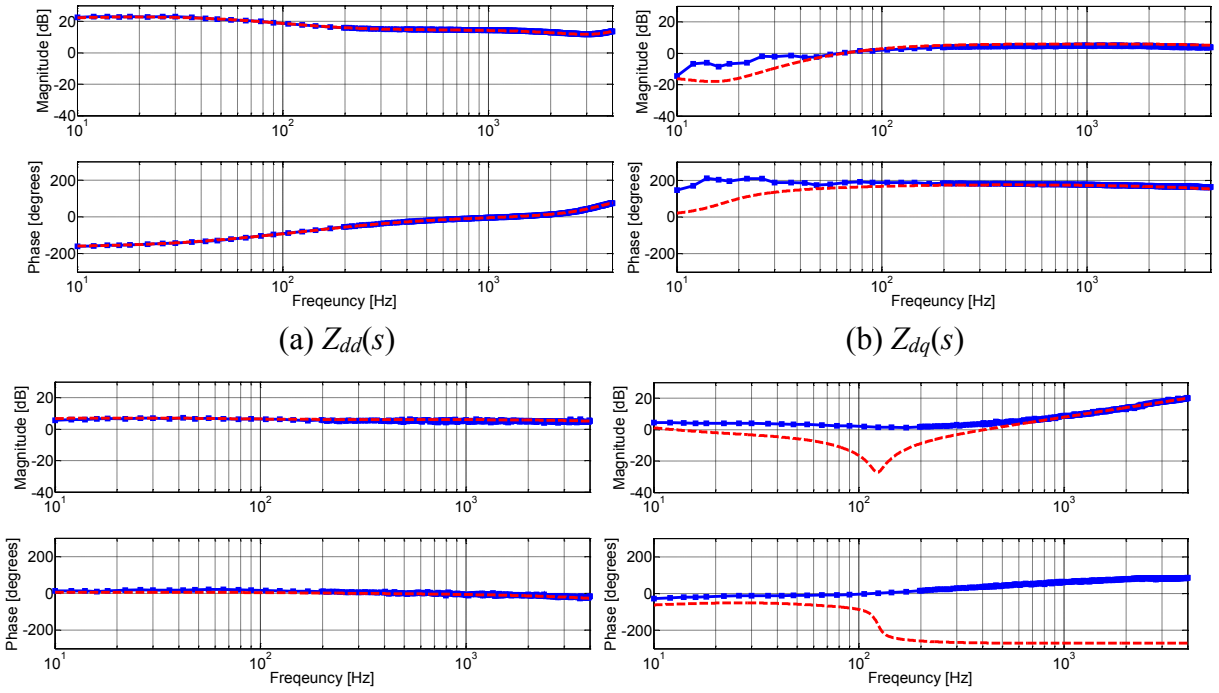


Figure 2-19: Classical dq averaged model of three-phase boost rectifier

Similarly in this case both switching model and averaged model yield same results as SVM with natural sampling is implemented and analog loops are closed. All the conclusions derived for the first case apply also in this case.

The influence of PLL on small-signal dq impedances of two-level VSR is being studied and researched intensively in the last ten years [111]. Furthermore, it has been shown that PLL will mostly influence the small-signal impedance $Z_{qq}(s)$, which is correctly predicted in Figure 2-20. PLL modifies significantly both the phase and magnitude characteristics of the small-signal impedance $Z_{qq}(s)$, which can lead to the instability of the system. In addition, the small-signal impedance $Z_{dq}(s)$ is modified by PLL in the low frequency range, while PLL does not modify impedance in the high frequency range as it is outside of the PLL's bandwidth. Since PLL is realized using the q coordinate source voltage, there is no influence of PLL on the small-signal impedances $Z_{dd}(s)$ and $Z_{qd}(s)$.

The bode diagrams of the source small-signal dq impedance are shown in Figure 2-21. The cross-diagonal small-signal impedances $Z_{dq}(s)$ and $Z_{qd}(s)$ are precisely identified as their



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

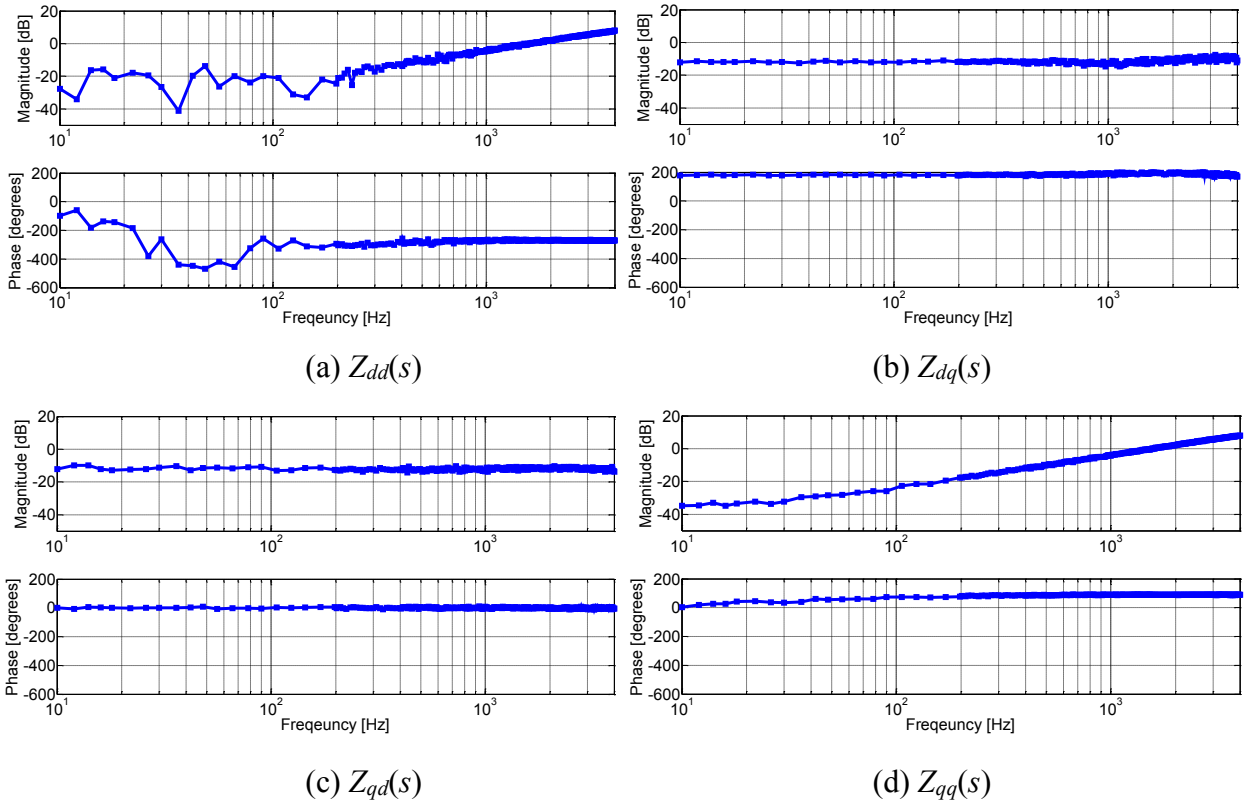
(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 2-20: Comparison of boost rectifier input dq impedances obtained by switching model (straight blue line) and dq averaged model (dashed red line) (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

magnitude characteristic is above the noise level. On the other hand, the main diagonal small-signal impedances $Z_{qq}(s)$ and $Z_{dd}(s)$ have the low magnitude values (close to the noise level) in the low frequency range. Therefore, the obtained impedance results are not "as clean" as other impedance results presented. The small-signal impedance of the source side obtained from the classical dq averaged model can be described with the following analytical expression.

$$Z_{sdqavg}(s)=\begin{bmatrix} sL_s+R_{ls} & -\omega_s L_s \\ -\omega_s L_s & sL_s+R_{ls} \end{bmatrix} \qquad 2\text{–}55$$

Furthermore, due to the implementation of PLL in the model, the small-signal dq impedances of the source side will be influenced and shaped by PLL.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 2-21: Comparison of boost rectifier input dq impedances obtained by switching model and dq averaged model (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

2.5 Identification Algorithm based on Estimation of Power Spectrum

As mentioned before, a Fourier transform can be applied on a discrete signal $x(n)$ of N samples, resulting in the discrete Fourier transform (DFT) calculated in N equidistant frequency points.

$$X(k) = \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi}{N}kn} \qquad 2\text{–}56$$

The inverse discrete Fourier transform (IDFT) is given as.

$$x(n) = \frac{1}{N} \sum_{n=0}^{N-1} X(k) e^{j\frac{2\pi}{N}kn} \qquad 2\text{–}57$$

The straight forward implementation of DFT requires N^2 complex operations, where a single complex operations consists of complex multiplication and complex addition. This especially becomes rather intensive calculation, when the large array signals are being transformed. Therefore, the algorithms for the fast calculation of Fourier transform utilize the periodic and symmetric properties of exponential term $e^{-j2\pi/N}$ to avoid the redundant calculations. The fast algorithms are known as FFT algorithms. One way to implement FFT algorithm, which is widely used today in the practice, is presented in [127].

The energy or power of the deterministic signals can be related to the Fourier transform. The energy spectral density of the discrete time signal $x(n)$ is given below.

$$\left|X(f)\right|^2 = \left| \sum_{n=-\infty}^{+\infty} x(n) e^{-j2\pi fn} \right|^2 \qquad 2\text{–}58$$

The energy spectrum of the signal can be expressed as a Fourier transform of the auto correlation function of the discretized signal.

$$\left|X(f)\right|^2 = \sum_{m=-\infty}^{+\infty} r_{xx}(m) e^{-j2\pi fm} \qquad 2\text{–}59$$

Where the autocorrelation function $r_{xx}(m)$ of the signal $x(n)$ is defined with the following expression.

$$r_{xx}(m) = \sum_{n=-\infty}^{+\infty} x(n) x(n+m) \qquad 2\text{–}60$$

The power density spectrum function of discrete signal is simply obtained as:

$$P_{xx}(f) = \frac{1}{N} \sum_{m=-\infty}^{+\infty} r_{xx}(m) e^{-j2\pi fm} = \frac{1}{N} \left|X(f)\right|^2 \qquad 2\text{–}61$$

The Fourier transform exists only for a signals whose energy is finite. In order to characterize noise, the stationary stochastic signals can be used as a good representative. Due to the stationary condition, the stochastic signals are infinitely long and have infinite energy, therefore the Fourier transform of such signals does not exist. However, for the class of stochastic signals, it is possible to define the power spectral density as the Fourier transform of the autocorrelation function.

$$P_{xx}(f) = \sum_{m=-\infty}^{+\infty} r_{xx}(m) e^{-j2\pi fm} \qquad 2\text{–}62$$

Where the autocorrelation function is defined as written below.

$$r_{xx}(m) = E(x(n)x(n+m)) \qquad 2\text{–}63$$

In practice, the autocorrelation function of the stochastic signal is estimated in the following way.

$$\hat{r}_{xx}(m) = \frac{1}{N-|m|} \sum_{n=0}^{N-|m|-1} x(n)x(n+m), |m| = 0,1,..., N-1 \qquad 2\text{–}64$$

Where its Fourier transform gives the power density spectrum function.

$$\hat{P}_{xx}(f) = \sum_{m=-(N-1)}^{m=N-1} r_{xx}(m) e^{-j2\pi fm} \qquad 2\text{–}65$$

The estimate of correlation function correctly predicts the autocorrelation value.

$$E(\hat{r}_{xx}(m)) = \frac{1}{N-|m|} \sum_{n=0}^{N-|m|-1} E(x(n)x(n+m)) = r_{xx}(m) \qquad 2\text{–}66$$

The variance of autocorrelation function can be expressed in the following way:

$$Var(\hat{r}_{xx}(m)) = \frac{N}{(N-|m|)^2} \sum_{n=-\infty}^{+\infty} \left(|r_{xx}(n)|^2 + r_{xx}(n-m) r_{xx}(n+m) \right) \qquad 2\text{–}67$$

$$\lim_{N\to\infty} Var(\hat{r}_{xx}(m)) = 0 \qquad 2\text{–}68$$

In this way, $\hat{r}_{xx}(m)$ gives unbiased and consistent estimate the autocorrelation function.

Alternatively, the following expression can be used to estimate the autocorrelation function of discrete signal of N samples.

$$\hat{r}_{xx}(m)=\frac{1}{N}\sum_{n=0}^{N-|m|-1}x(n)x(n+m),|m|=0,1,...,N-1 \qquad 2\text{–}69$$

In this way, the estimate of autocorrelation function $\hat{r}_{xx}(m)$, has the systematic error.

$$E(\hat{r}_{xx}(m))=\frac{1}{N}\sum_{n=0}^{N-|m|-1}E(x(n)x(n+m))=\left(1-\frac{|m|}{N}\right)r_{xx}(m) \qquad 2\text{–}70$$

$$\lim_{N\to\infty}E(\hat{r}_{xx}(m))=r_{xx}(m) \qquad 2\text{–}71$$

The estimate of the autocorrelation function is asymptotically unbiased. The variance of autocorrelation function is smaller than in the previous case.

$$Var(\hat{r}_{xx}(m))=\frac{1}{N}\sum_{n=-\infty}^{+\infty}\left(|r_{xx}(n)|^2+r_{xx}(n-m)r_{xx}(n+m)\right) \qquad 2\text{–}72$$

Finally, it can be concluded that the estimate of autocorrelation function is asymptotically unbiased and consistent.

2.5.1 Periodogram identification method

The previously used estimate of the correlation function can be used for the estimation of the power density spectrum function.

$$\hat{P}_{xx}(f)=\sum_{m=-(N-1)}^{N-1}\hat{r}_{xx}(m)e^{-j2\pi fm} \qquad 2\text{–}73$$

$$\hat{P}_{xx}(f)=\frac{1}{N}\left|\sum_{n=0}^{N-1}x(n)e^{-j2\pi fn}\right|^2=\frac{1}{N}|X(f)|^2 \qquad 2\text{–}74$$

The last two expressions are the basis of the power spectra estimation and they are known as periodogram method. The estimate of the periodogram is obtained by applying the estimation operator on the previous equation.

$$E\left(\hat{P}_{xx}(f)\right)=E\left(\sum_{m=-(N-1)}^{N-1}\hat{r}_{xx}(m)e^{-j2\pi fm}\right)=\sum_{m=-(N-1)}^{N-1}\left(1-\frac{|m|}{N}\right)\hat{r}_{xx}(m)e^{-j2\pi fm} \quad 2\text{–}75$$

The last expression can be understood as a Fourier transform of autocorrelation function multiplied with a triangular window.

$$\tilde{r}_{xx}(m)=\left(1-\frac{|m|}{N}\right)\hat{r}_{xx}(m) \quad 2\text{–}76$$

Finally, the estimate of the periodogram can be written as:

$$E\left(\hat{P}_{xx}(f)\right)=\sum_{m=-(N-1)}^{N-1}\tilde{\hat{r}}_{xx}(m)e^{-j2\pi fm}=\frac{1}{2\pi}\int_{-\pi}^{+\pi}P_{xx}(\theta)W_{TR}(\omega-\theta)d\theta \quad 2\text{–}77$$

Where $W_{TR}(\omega)$ is a Fourier transform of the triangular window function. The estimate of power spectrum obtained by a periodogram is actually a convolution of the real power density spectrum and triangular window transfer function. As a number of samples goes to infinity

$$\lim_{N\to\infty}\left(E\left(\hat{P}_{xx}(f)\right)\right)=\lim_{N\to\infty}\left[\sum_{m=-(N-1)}^{N-1}\tilde{\hat{r}}_{xx}(m)e^{-j2\pi fm}\right]=P_{xx}(f) \quad 2\text{–}78$$

Thus, it can be concluded that the periodogram is asymptotically unbiased estimate of the power density functions. However, for the variance of the periodogram for the Gaussian noise is given below.

$$Var\left(\hat{P}_{xx}(f)\right)=P_{xx}^2(f)\left[1+\left(\frac{\sin(2\pi fN)}{N\sin(2\pi f)}\right)^2\right] \quad 2\text{–}79$$

$$\lim_{N\to\infty}Var\left(\hat{P}_{xx}(f)\right)=P_{xx}^2(f) \quad 2\text{–}80$$

Meaning that the periodogram is not a consistent estimate of the real signal spectrum. There are two ways to calculate periodograms, directly from a DFT of signal $x(n)$ or by applying FFT on the correlation function $\hat{r}_{xx}(m)$. Due to the given drawbacks of the periodogram method, a more advanced techniques based on the sectioning and averaging can be used.

2.5.2 Bartlett method

It is possible to obtain the power spectrum by splitting the sampled data into K equal segments, whose length is M.

$$\begin{aligned} &x_i(n) = x(n + iM), \\ &i = 0,1,...,K-1; n = 0,1,...,M-1 \end{aligned} \quad 2\text{–}81$$

The periodogram of each sequence is separately calculated as

$$\hat{P}_{xx}^{i}(f) = \frac{1}{M}\left|\sum_{n=0}^{M-1} x_i(n) e^{-j2\pi fn}\right|^2 \quad 2\text{–}82$$

After that, the Bartlett power density spectrum estimate is obtained by averaging the calculated periodograms of each segment.

$$\hat{P}_{xx}^{B}(f) = \frac{1}{K}\sum_{n=0}^{K-1} \hat{P}_{xx}^{i}(f) \quad 2\text{–}83$$

Estimate of the power spectrum via the Bartlett method is described with the following expression.

$$E\left(\hat{P}_{xx}^{B}(f)\right) = \frac{1}{K}\sum_{n=0}^{K-1} E\left(\hat{P}_{xx}^{i}(f)\right) = E\left(\hat{P}_{xx}(f)\right) \quad 2\text{–}84$$

Which is the expected result, as it is same as the expectation of the periodogram method. The variance of the Bartlett method is given with the following expression.

$$Var\left(\hat{P}_{xx}^{B}(f)\right) = \frac{1}{K^2}\sum_{n=0}^{K-1} Var\left(\hat{P}_{xx}^{i}(f)\right) = \frac{1}{K} Var\left(\hat{P}_{xx}(f)\right) \quad 2\text{–}85$$

Similarly, variance of the Gaussian noise signal obtained by a Bartlett method is obtained in the following manner.

$$Var\left(\hat{P}_{xx}^{B}(f)\right) = \frac{1}{K} P_{xx}^{2}(f)\left[1 + \left(\frac{\sin(2\pi fN)}{N\sin(2\pi f)}\right)^2\right] \quad 2\text{–}86$$

The variance of Bartlett method is K time smaller than the variance of the periodogram method. The described method is more computationally intensive, but offers the way to reduce the variance of unwanted noisy signal.

2.5.3 Welch's averaging method

The Welch's method divides the captured sampled signal into L segments, where each segments consists of M samples and overlapping of segments is allowed.

$$\begin{aligned} &x_i(n) = x(n + iD), \\ &i = 0,1,...,L-1; n = 0,1,...,M-1 \end{aligned} \quad 2\text{–}87$$

If the segments are not overlapping, then $D=M$, and for the case of 50% overlap the $D=M/2$. The periodogram of the i^{th} segment is obtained after windowing the segmented data.

$$\hat{P}_{xx}^{i}(f) = \frac{1}{MU}\left|\sum_{n=0}^{M-1} w(n)x_i(n)e^{-j2\pi fn}\right|^2 \quad 2\text{–}88$$

The U represent the normalization factor, calculated as.

$$U = \frac{1}{M}\sum_{n=0}^{M-1} w^2(n) \quad 2\text{–}89$$

The estimate of power spectrum is calculated as a mean value of modified periodograms.

$$\hat{P}_{xx}^{W}(f) = \frac{1}{L}\sum_{n=0}^{L-1} \hat{P}_{xx}^{i}(f) \quad 2\text{–}90$$

The expectation of power spectrum obtained via Welch's method is as below.

$$E\left(\hat{P}_{xx}^{W}(f)\right) = \frac{1}{L}\sum_{n=0}^{L-1} E\left(\hat{P}_{xx}^{i}(f)\right) = E\left(\hat{P}_{xx}^{i}(f)\right) \quad 2\text{–}91$$

$$E\left(\hat{P}_{xx}^{i}(f)\right) = \frac{1}{MU}\sum_{n=0}^{M-1}\sum_{m=0}^{M-1} w(n)w(m)E\left(x_i(n)x_i(m)\right)e^{-j2\pi f(n-m)} \quad 2\text{–}92$$

$$E\left(\hat{P}_{xx}^{i}(f)\right) = \frac{1}{MU}\sum_{n=0}^{M-1}\sum_{m=0}^{M-1} w(n)w(m)r_{xx}(n-m)e^{-j2\pi f(n-m)} \quad 2\text{–}93$$

$$E\left(\hat{P}_{xx}^{i}(f)\right) = \int_{-0.5}^{0.5} P_{xx}(v)W(f-v)dv \quad 2\text{–}94$$

Where

$$W(\omega)=\frac{1}{MU}\left|\sum_{n=0}^{M-1}w(n)e^{-j\omega fn}\right|^2 \qquad 2\text{–}95$$

The normalization constant is used to satisfy the following condition.

$$1=\frac{1}{2\pi}\int_{-\pi}^{\pi}W(\omega)d\omega \qquad 2\text{–}96$$

The variance of the Welch's method is given by the following expression.

$$Var\left(\hat{P}_{xx}^{W}(f)\right)=\frac{1}{L^2}\sum_{i=0}^{L-1}\sum_{j=0}^{L-1}E\left(\hat{P}_{xx}^{i}(f)\hat{P}_{xx}^{j}(f)\right)-\left(E\left(\hat{P}_{xx}^{W}(f)\right)\right)^2 \qquad 2\text{–}97$$

It has been shown in [91], that if there is no overlap among segments, the variance is.

$$Var\left(\hat{P}_{xx}^{W}(f)\right)=\frac{1}{L}Var\left(\hat{P}_{xx}^{W}(f)\right)\approx\frac{1}{L}P_{xx}^{2}(f) \qquad 2\text{–}98$$

If the overlap among the segments is 50% and triangular window is used, then the variance of the power spectrum calculated with Welch's method is:

$$Var\left(\hat{P}_{xx}^{W}(f)\right)\approx\frac{9}{8L}P_{xx}^{2}(f) \qquad 2\text{–}99$$

In this case the number of segments is almost doubled compared to no overlap case, therefore the overlapping provides further reduction of noise. If other window function is used instead of triangular window, the variance of Welch's method will have different value.

Comparatively, all three methods yield same power spectrum estimate of deterministic signals. However, it is obvious that the Welch's method with 50% overlapping the most effectively attenuates the noise. This is especially important in the identification of small-signal dq impedances, since the sensed current and voltages may be very corrupted with the noise.

2.5.4 Impedance Identification

The identification of spectrum can be performed via the estimation of cross power spectrum density (CPSD) by any of the described methods. Usually, the noise present in the sensing of voltage and current signals, therefore the Welch's method is used to estimate the cross power spectral density.

The algorithm is as follows, output signal is equal to convolution of system impulse response and input signal plus some added noise.

$$y(t) = h(t) \otimes x(t) + n(t) \qquad 2\text{–}100$$

Now we will correlate the previous equation to the input signal, so we can write

$$P_{yx}(j\omega) = H(j\omega) P_{xx}(j\omega) + P_{nx}(j\omega) \qquad 2\text{–}101$$

If the input signal is not correlated to the added noise $P_{nx}(j\omega)=0$, then the transfer function can be estimated as written below.

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} = \frac{P_{yx}(j\omega)}{P_{xx}(j\omega)} \qquad 2\text{–}102$$

Theoretically other approach is also possible, we can correlate equation 2-15 with the output signal and obtain the following expression.

$$P_{yy}(j\omega) = H(j\omega) P_{xy}(j\omega) + P_{yn}(j\omega) \qquad 2\text{–}103$$

If the output signal is not correlated to the noise present in the system, then the transfer function can be estimated as

$$H(j\omega) = \frac{Y(j\omega)}{X(j\omega)} = \frac{P_{yy}(j\omega)}{P_{xy}(j\omega)} \qquad 2\text{–}104$$

The first approach, where the input signal is correlated to the system equation, is called H_1 estimate. The second approach, where output signal is correlated to the system equation is called H_2 estimate. Usually, H_1 estimate is used more often in the practice, because the clean input signal or reference signal is generated inside the DSP.

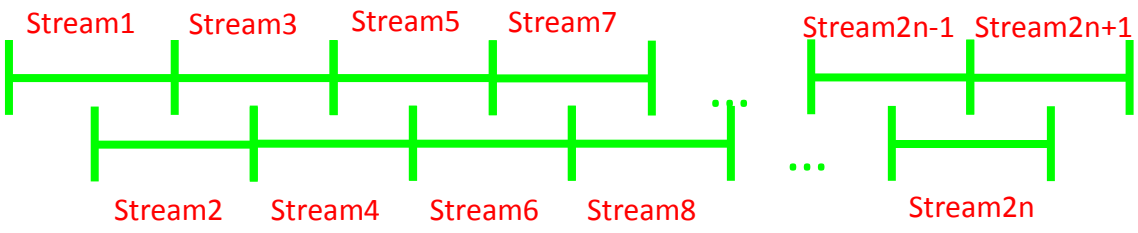


Figure 2-22: Splitting of a signal into the overlapping stream of sections

In our case the reference signal, which can be chirp, multi-tone or sine is a clean input signal, while whatever signal is measured, either voltage or current is the output signal that is usually corrupted with the noise. In order to estimate power spectral density functions we will use the cpsd function in Matlab. The CPSD function divides input signal into the overlapping sections. Next, FFT is applied to the each section and obtained FFTs are averaged, resulting in the reduction of noise power. It has been proven that such an algorithm reduces the noise present in the signal and correctly estimates the wanted transfer function. Figure 2-22 shows an example of overlapping sections with 50% overlap.

Once functions P_{yx} and P_{xx} are estimated, transfer function of H_1 can be calculated. After we obtain all the transfer functions from references to the currents and voltages we can estimate wanted impedances.

In order to estimate the small-signal impedance, during the first injection via d channel, dq currents and voltages of one side can be related to the perturbation signal in the following way.

$$\begin{bmatrix} i_{d1}(s) \\ i_{q1}(s) \end{bmatrix} = \begin{bmatrix} G_{idpd}(s) & G_{idpq}(s) \\ G_{iqpd}(s) & G_{iqpq}(s) \end{bmatrix} \begin{bmatrix} p_1(s) \\ 0 \end{bmatrix} \quad 2\text{–}105$$

$$\begin{bmatrix} v_{d1}(s) \\ v_{q1}(s) \end{bmatrix} = \begin{bmatrix} G_{vdpd}(s) & G_{vdpq}(s) \\ G_{vqpd}(s) & G_{vqpq}(s) \end{bmatrix} \begin{bmatrix} p_1(s) \\ 0 \end{bmatrix} \quad 2\text{–}106$$

Similarly, during the second perturbation, the perturbation signal is being injected via the q-channel. The sensed dq currents and voltages can be related to the perturbation signal.

$$\begin{bmatrix} i_{d2}(s) \\ i_{q2}(s) \end{bmatrix} = \begin{bmatrix} G_{idpd}(s) & G_{idpq}(s) \\ G_{iqpd}(s) & G_{iqpq}(s) \end{bmatrix} \begin{bmatrix} 0 \\ p_2(s) \end{bmatrix} \quad 2\text{–}107$$

$$\begin{bmatrix} v_{d2}(s) \\ v_{q2}(s) \end{bmatrix} = \begin{bmatrix} G_{vdpd}(s) & G_{vdpq}(s) \\ G_{vqpd}(s) & G_{vqpq}(s) \end{bmatrix} \begin{bmatrix} 0 \\ p_2(s) \end{bmatrix} \quad 2\text{–}108$$

Same signal can be injected via both channels, $p_1(s)=p_2(s)=p(s)$, enabling the estimation of the following transfer function with the power spectrum methods.

$$G_{idpd}(s) = \frac{i_{d1}(s)}{p(s)}; G_{idpq}(s) = \frac{i_{q1}(s)}{p(s)} \quad 2\text{–}109$$

$$G_{iqpd}(s)=\frac{i_{d2}(s)}{p(s)};G_{iqpq}(s)=\frac{i_{q2}(s)}{p(s)} \qquad 2\text{–}110$$

$$G_{vdpd}(s)=\frac{v_{d1}(s)}{p(s)};G_{vdpq}(s)=\frac{v_{q1}(s)}{p(s)} \qquad 2\text{–}111$$

$$G_{vqpd}(s)=\frac{v_{d2}(s)}{p(s)};G_{vqpq}(s)=\frac{v_{q2}(s)}{p(s)} \qquad 2\text{–}112$$

Next, the small-signal dq impedances are calculated using the identified transfer functions, yielding that the dq impedance is ratio of voltage and current transfer function matrices. The main benefit of this approach is that the identified transfer functions will have reduced effect of the noise.

$$Z_{dq}(s)=\begin{bmatrix}G_{vdpd}(s) & G_{vdpq}(s)\\ G_{vqpd}(s) & G_{vqpq}(s)\end{bmatrix}\begin{bmatrix}G_{idpd}(s) & G_{idpq}(s)\\ G_{iqpd}(s) & G_{iqpq}(s)\end{bmatrix}^{-1} \qquad 2\text{–}113$$

The previous expression is used to characterize the source and load small-signal dq impedances.

Figure 2-23 shows noisy current signal and ideal current signal. Amount of noise was selected to cover load current "completely", so one cannot recognize current shape within the noisy signal.

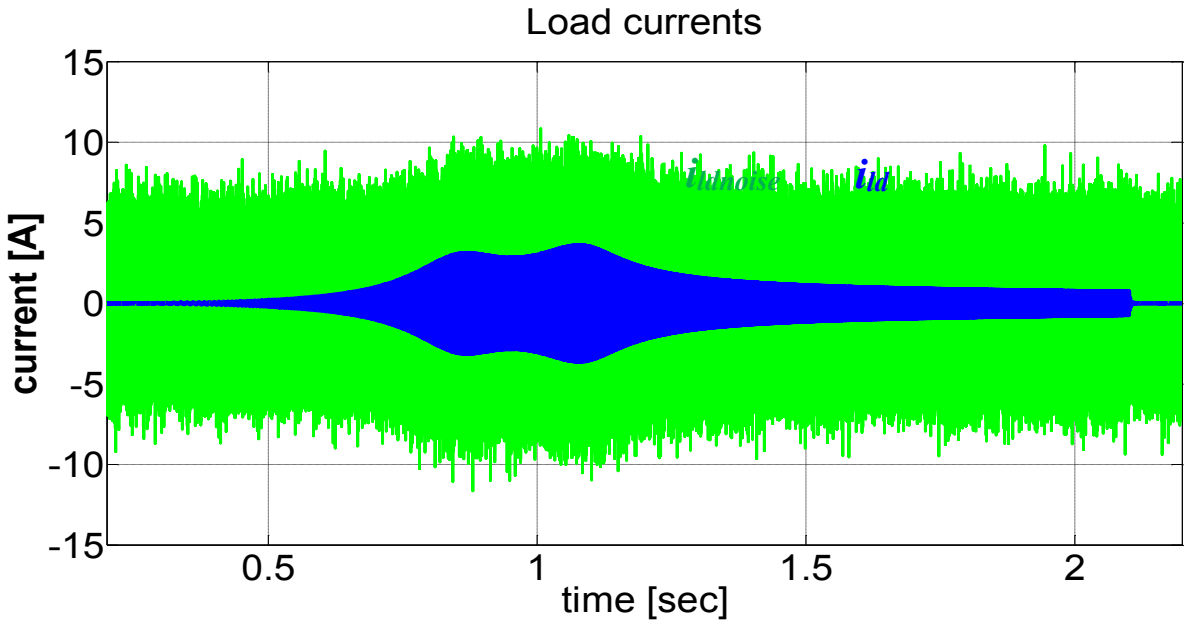


Figure 2-23: Noisy current signal (green curve) and ideal current signal (blue curve)

This amount of noise was added to source and load currents and to voltages. Then FFT and CPSD algorithms are applied to those noisy signals.

Figure 2-24 and Figure 2-25 show a comparison of FFT and CPSD algorithms on source impedance Z_{sdd} and load impedance Z_{ldd}, respectively. We can see that source impedance Z_{sdd} results are accurate for both algorithms because the added noise is below the source current signal level. Hence there is not a big difference in the applied algorithms. Load impedance results are not very accurate when the FFT algorithm is applied, because the noise level is high. The important conclusion is that the cpsd algorithm can clean noise from the load current signals and yield very clean load impedance result.

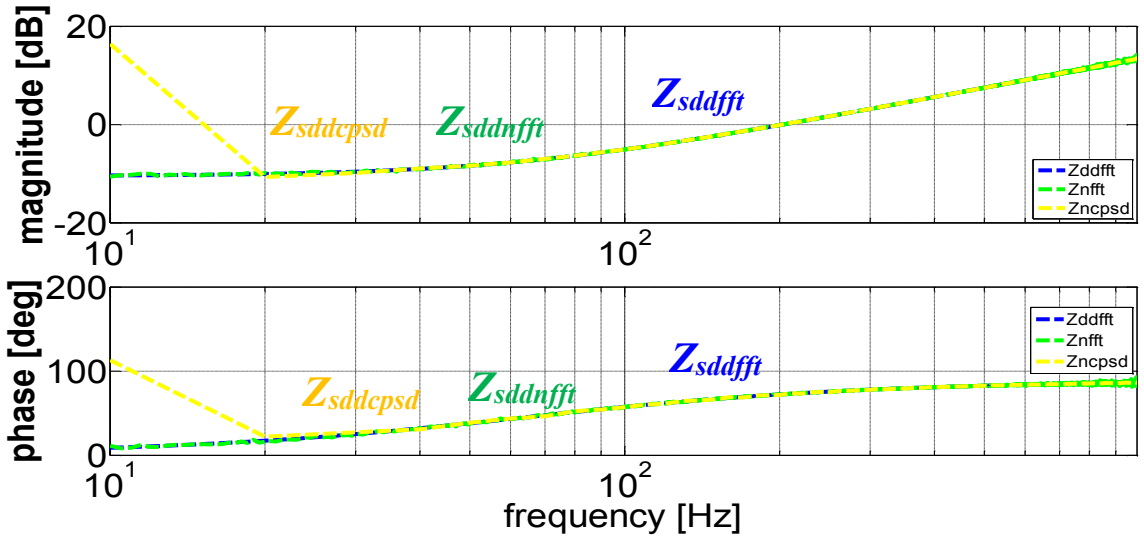


Figure 2-24: Source impedances Z_{sdd} comparison for FFT and CPSD algorithms

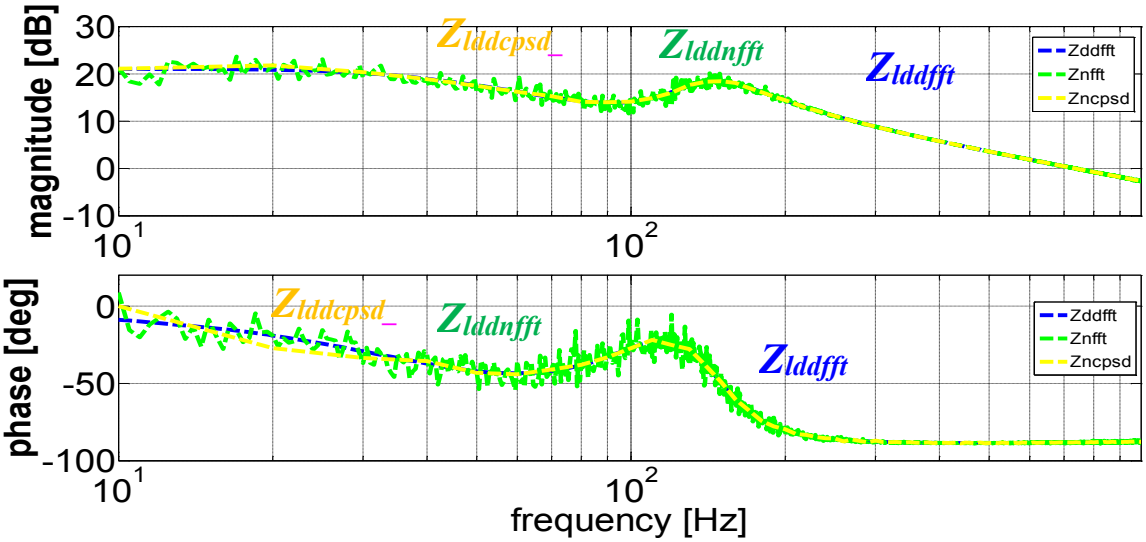


Figure 2-25: Load impedance Z_{ldd} comparison for FFT and CPSD algorithms

If we use a longer signal which is split into more windows then obtained impedances will be even more accurate. Inherent property of the algorithm is that there is an error in low frequency bandwidth, which can be verified easily in previous graphs. The error cannot be avoided, but a longer data stream should be generated, so low frequency error would be moved to lower frequencies. By doing it, an error in the low frequency part can be moved outside of the frequency region of interest. The price paid by applying this approach is that a longer injection is needed and more computational resources will be used.

2.6 Summary

Chirp and multi-tone signals have been successfully used for the small-signal dq impedance extraction. First ideal chirp signal is generated with ideal current and voltage sources. It has been shown that balanced passive networks can be identified accurately with chirp and multi-tone injection signals.

Furthermore, the multi-tone signal has been successfully used to characterize the small-signal dq impedances of three-phase VSI, behaving as an active source with current and voltage loops closed, feeding the three-phase passive load. In this way, the identification of dq impedances is performed in the larger number of points. The effect of dead time on the small-signal dq impedance of three-phase VSI is captured and accurately predicted by FFT extraction algorithm.

The three-phase VSR rectifier feeding the dc resistive load is the second test-case for the small-signal dq impedance identification. The switching simulation model of three-phase VSR, which behaves as an active source with the inner current loop, outer dc voltage loop and PLL for the synchronization. The multi-tone signal was used to identify the small-signal dq impedances of active source, providing the small-signal dq impedance results in the increased number of points. The effect of PLL on the small-signal dq impedances is captured and extracted with FFT identification algorithm.

Even though the noise was added in a small amount it still can significantly make impedance simulation results erroneous. The big problem in instantaneous source and load impedance identification is that the signal is splitting to the source and load side. In the worst case, a small amount of the perturbation signal will go to one side, while a much larger amount of perturbation

signal will go to other side. This happens if the impedance is larger than the other one by the order of the magnitude value. This is the case in one of the examples presented, so we can see that even a small amount of noise can severely corrupt impedances. Therefore, it is very important to find a way to deal with the noise issues.

Finally, in the last part of the chapter the identification algorithm based on the estimation of periodograms is introduced and explained. It has been used on simulation models in order to understand its properties and verify its effectiveness. Obtained impedance results prove that CPSD algorithm can yield clean impedance results in the presence of a substantial amount of noise. An important condition for the usage of the algorithm is that a clean reference signal is necessary to provide a good performance in reducing the noise. The algorithm based on the estimation of power spectrum is general and can be applied with any type of injection signals like chirp, multi-tone, sinusoidal or other wide-bandwidth signals.

Chapter 3. Modeling of Small-Signal Input dq Admittance of Six-Pulse Diode Rectifiers

This chapter focuses on the modeling of small-signal input dq admittance of six-pulse diode rectifiers, providing comparison between well-known averaged value models (AVMs), the switching simulation model and hardware measurements. The analytical AVM (AAVM) is a widely used solution for modeling a six-pulse diode rectifier, but it is found that it has to be modified in order to model the input dq admittance more accurately. Analytical expressions for all four admittances present in the dq matrix are derived and compared to switching model small-signal dq admittances, proving that modified AAVM match small-signal dq admittances of switching simulation model. Furthermore, a parametric AVM (PAVM) is included into analysis, "slightly modified" and analytical expressions for all four dq admittances are derived in this case also. PAVM match dq admittance resonance points somehow better. However, it is concluded that both AVMs predicts two admittances, $Y_{dd}(s)$ and $Y_{qd}(s)$, very precisely even beyond the switching frequency. On the other hand, the prediction of other two admittances, $Y_{dq}(s)$ and $Y_{qq}(s)$, is accurate only up to one third and one half of the switching frequency, respectively. The main sources of differences are found to be sideband resonant points that are mainly present in the response to q-channel injection. The main reason is that q-channel injection modulates commutation angle and yields significant sideband admittances around multiples of the switching frequency, which is typical behavior for nonlinear systems. Furthermore, a hardware set-up is built, measured and modeled, showing that the switching simulation model captures nonlinear sideband effects accurately. In the end, a six-pulse diode rectifier feeding a constant power load is analyzed with modified AAVM and through detailed simulations of switching model, proving effectiveness of the proposed modifications.

3.1 Introduction

Modeling of the input dq admittance of three-phase AC systems has been a "hot research topic" in recent years as there is a need to estimate stability of the modern electric and ship power systems.

Generalized Nyquist Criterion (GNC), which is based on the source small-signal dq impedance and the load small-signal dq admittance, can be used to estimate stability of the power systems at a three-phase interface in a dq rotating frame. This approach has been used in several different publications regarding stability of the power systems as it is widely used tool for small-signal stability analysis [19].

However, still there are not many papers published, which address modeling and characterization of the small-signal input dq admittance of six-pulse diode rectifier, although diode rectifiers are very commonly found in many power systems. A number of averaged models of six-pulse diode rectifiers have been developed, trying to capture inherent nonlinear behavior of the rectifier as shown in [67]-[69]. All the developed AVMs can be grouped into two groups, based on the derivation approach used. The first approach is analytical average modeling, where the model is derived analytically from the state-space equations, describing physical behavior of the diode rectifier. Analytical modeling maps AC side filter to DC side and in some cases the complete derivation of the model is very cumbersome and algebraically intensive. In the second approach, a voltage controlled voltage sources and current controlled current sources are used to describe averaged model, where parameters of AVM are obtained numerically from the switching simulation model. In this way a parametric AVM (PAVM) is obtained. PAVM does not require mapping of AC side parameters to DC side, but it does require intensive simulation of the switching model to obtain appropriate characterization of the model's parameters [76]-[78]. Therefore, both approaches are investigated in this chapter and used to identify small-signal input dq admittance of AVMs. However, it is found that both models need to be somehow modified to provide more accurate small-signal dq admittance results. The modification takes into account the nature of dq injection, thus yielding correct small-signal dq admittance characteristics. Through the detailed analysis it is found that both AVMs are simplifications of the switching model and both models fail to predict the complete small-signal dq admittance characteristic of the six-pulse diode rectifier, especially in the frequency range beyond the switching frequency (360 Hz).

Many of AVMs have been validated through detailed comparison with the switching simulation model as shown in [73]-[75]; steady-state values of voltages and currents are matched, transient step load comparison is investigated and small-signal frequency identification is performed only through the validation of dc impedances. Nevertheless, there have not been many results published on estimating input dq impedance/admittance from the averaged models and/or

from the switching models, although there is an apparent need for such analysis. Small-signal dq admittance identification from PAVM is performed in [78], but obtained results are generalized as correct without comparison to the switching model dq admittance or hardware measurements. Therefore, the focus of the paper is to identify input dq admittance from already known AVMs, to obtain the input dq admittance from the switching simulation model, and to compare those results with hardware measurements. A six-pulse diode rectifier with a simple inductor filter on the ac side and an LC filter on dc side is selected to be a test case model. Schematic of the six-pulse diode rectifier, which is used in hardware set-up, switching simulations and in averaged modeling, is shown in Figure 3-1. The parameters of a six-pulse diode rectifier are given in Table 3-1.

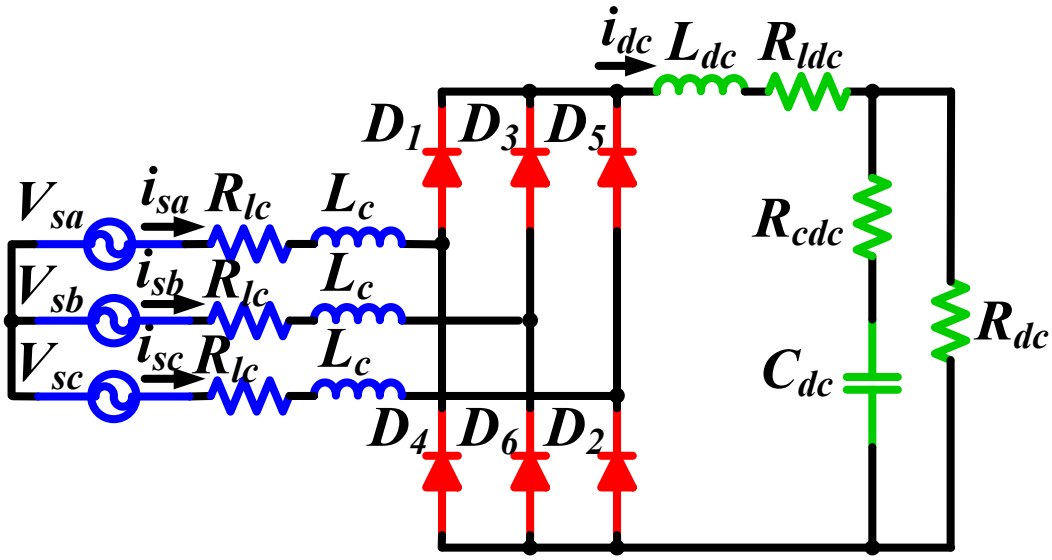


Figure 3-1: Schematic of six-pulse diode rectifier with resistive load.

Furthermore, all the models used throughout the paper, namely switching, AAVM and PAVM, are built in MATLAB using the SimPowerSystem toolbox. The input dq admittances of the switching simulation model are obtained via small-signal identification using an FFT algorithm. For that purpose, series voltage AC sweep small-signal injection in dq coordinates is performed, where the injection voltage root mean square value (RMS) is set to 4 V, which is around 2.5% of the voltage at the three-phase interface. The FFT algorithm was applied at 68 points in a frequency range 1 Hz-1000 Hz.

Finally, the accurate small-signal model in dq coordinates of six-pulse diode rectifier is also necessary to properly close the loops and design the controller for voltage generators used in power

systems. Therefore, the usability of the work presented in the paper is not restricted only to the small-signal dq impedance/admittance identification for stability analysis.

Table 3-1 Parameters of six-pulse diode rectifier

Parameter name	***Parameter values***	
Voltage source	V_{srms}=120 V	f_s=60 Hz
AC Inductor	L_c=0.22 mH	R_{lc}=30 mΩ;
DC Inductor	L_{dc}=0.9 mH	R_{ldc}=60 mΩ
DC Capacitor	C_{dc}=1.05 mF	R_{cdc}=30 mΩ
Load Resistor	R=12.8 Ω	P_{dc}≈6 kW

3.2 Analytical Averaged Value Modeling (AAVM)

AAVM is a widely used solution to model six-pulse diode rectifier [65]-[66], which is derived analytically, using the analytical description of the physical behavior of diode rectifier. The AAVM is described using state-space equations for both commutation period (three diodes conducting) and for conduction period (two diodes conducting). The averaged model is obtained with summing both equations and averaging over a switching period, the so called switching averaging, where in this case the switching frequency is equal to six times the line frequency. Obtained averaged model correctly mimics behavior for the mode that was assumed during the derivation procedure. If a diode rectifier works in some other mode, no matter whether it is a discontinuous conduction mode (DCM) or continuous conduction mode (CCM), it is necessary to derive average model again using the equations specific for that mode. Moving average that is used in the derivation for arbitrary state variable is defined below, where T is the averaging period.

$$\bar{x}(t)=\frac{1}{T}\int_{t-T}^{t}\left(x_{cond}(\tau)+x_{comm}(\tau)\right)d\tau \qquad 3\text{–}1$$

Furthermore, the following Park's transformation, which is magnitude invariant, is commonly used in the derivation process, where θ is angle of the voltage source.

$$T_{dq}=\frac{2}{3}\begin{bmatrix}\cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right)\\ -\sin(\theta) & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right)\end{bmatrix} \qquad 3\text{–}2$$

The main assumption made during a derivation process is that the dc side current has small ripple, which depends strongly on circuit components values. This fact severely limits the usability of the model as it provides modeling with smaller and larger error values depending on the filter parameters on the dc-side. Therefore, the more accurate is the assumption, the more accurate results with AAVM will be obtained and vice versa, the less accurate is the assumption, the less accurate results with AAVM will be obtained. In the used example, it is shown that AAVM fails to predict correct steady-state value of current source q-axis component, which leads to noticeable error in small-signal analysis when AAVM is used. The error is relatively easily eliminated, if the proper scaling is applied.

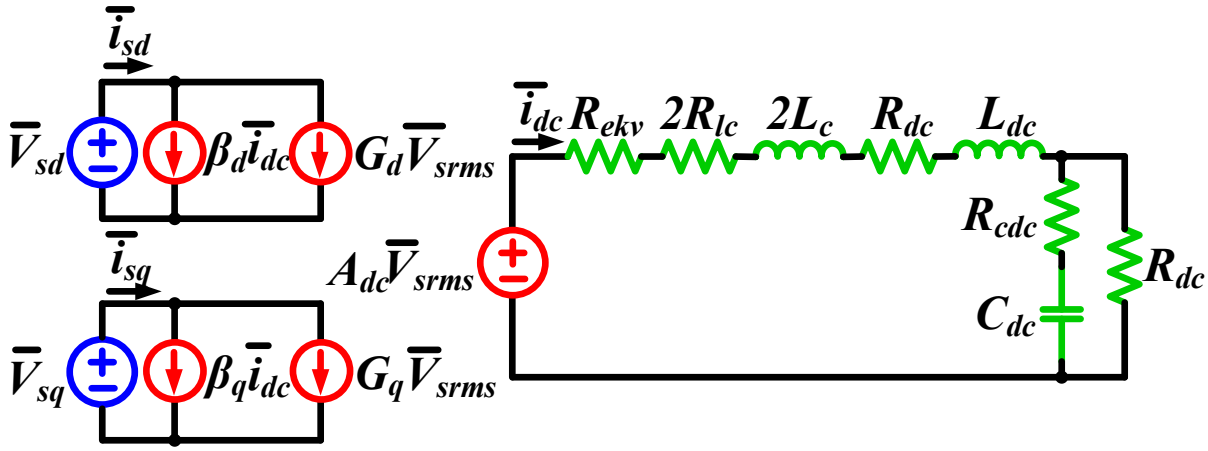


Figure 3-2: Equivalent averaged circuit schematic of AAVM.

3.2.1 Equivalent equations of AAVM

The equations, which describe AAVM, are given below.

$$\begin{aligned} i_{sd} &= \beta_d(\mu) i_{dc} + G_d(\mu) v_{srms}; \\ i_{sq} &= \beta_q(\mu) i_{dc} + G_q(\mu) v_{srms}; \\ v_{rect} &= A_{dc} v_{srms} = A_{dc} \sqrt{0.5} \sqrt{v_{sd}^2 + v_{sq}^2} = Z_{dc}(D) i_{dc} \end{aligned} \qquad 3\text{–}3$$

Equivalent averaged circuit schematic is shown in Figure 2. The parameters used in the previous equations are function of commutation angle μ, source angular speed ω_s and commutating inductance L_c.

$$\beta_d(\mu)=\frac{2\sqrt{3}}{\pi}\cos(\mu);\ \ \beta_q(\mu)=-\frac{2\sqrt{3}}{\pi}\sin(\mu);$$
$$A_{dc}=\frac{3\sqrt{6}}{\pi};\ \ R_{ekv}=\frac{3}{\pi}L_C\omega_s;$$
$$G_d(\mu)=\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_C}\left(\cos(2\mu)-4\cos(\mu)+3\right);$$
$$G_q(\mu)=-\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_C}\left(\sin(2\mu)-4\sin(\mu)+2\mu\right);$$

3–4

In order to obtain a small-signal dq input admittance of the AAVM, (3) has to be modified. AAVM without modification predicts two admittance $Y_{dq}(s)$ and $Y_{qq}(s)$ to be equal to zero. Therefore, the modified AAVM can be written as given below.

$$\begin{bmatrix} i_{sdm} \\ i_{sqm} \end{bmatrix}=\begin{bmatrix} \cos(\delta) & -\sin(\delta) \\ \sin(\delta) & \cos(\delta) \end{bmatrix}\begin{bmatrix} \beta_d(\mu)i_{dc}+G_d(\mu)v_{srms} \\ \beta_q(\mu)i_{dc}+G_q(\mu)v_{srms} \end{bmatrix} \qquad 3–5$$

Where $\cos(\delta)$ and $\sin(\delta)$ are defined via dq parameters of the source voltage.

$$\cos(\delta)=\frac{v_{sd}}{\sqrt{v_{sd}^2+v_{sq}^2}},\ \ \sin(\delta)=\frac{v_{sq}}{\sqrt{v_{sd}^2+v_{sq}^2}} \qquad 3–6$$

3.2.2 Small-signal dq admittance of AAVM

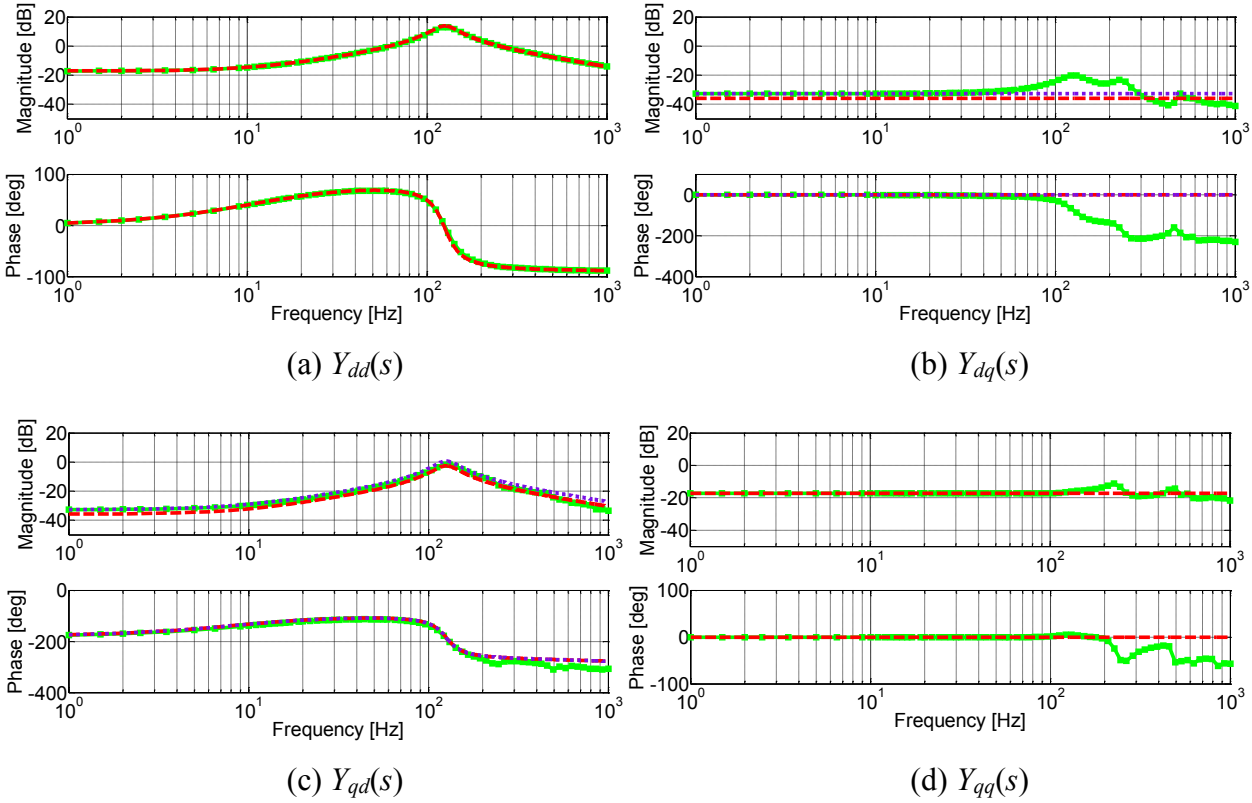
In order to derive the small-signal dq admittance of modified AAVM, it is necessary to linearize (5) with respect to input voltage variables v_{sd} and v_{sq}.

$$Y(s)=\begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix}=\begin{bmatrix} \frac{\tilde{i}_{sdm}(s)}{\tilde{v}_{sd}(s)} & \frac{\tilde{i}_{sdm}(s)}{\tilde{v}_{sq}(s)} \\ \frac{\tilde{i}_{sqm}(s)}{\tilde{v}_{sd}(s)} & \frac{\tilde{i}_{sqm}(s)}{\tilde{v}_{sq}(s)} \end{bmatrix} \qquad 3–7$$

After several algebraic manipulations of (5) using (6), simple expressions for small-signal dq input admittances are obtained. The analytical expressions for small-signal dq input admittances of modified AAVM are provided below.

$$\begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix}=\sqrt{0.5}\begin{bmatrix} \left(\beta_d Y_{dc}(s)A_{dc}+G_d\right) & -\frac{I_{sq}}{V_{srms}} \\ \left(\beta_q Y_{dc}(s)A_{dc}+G_q\right) & \frac{I_{sd}}{V_{srms}} \end{bmatrix} \qquad 3–8$$

The admittances $Y_{dd}(s)$ and $Y_{dq}(s)$ map DC side admittance $Y_{dc}(s)$ via simple algebraic expressions, where different parameters are used in each mapping as shown in (8). On the other hand, the admittances $Y_{qd}(s)$ and $Y_{qq}(s)$ consist of resistive part only, predicting that there is no influence of the DC side impedance. The resistive part is solely determined by the ratio of dq source currents and source rms value. The scaling of admittances is necessary for $Y_{dq}(s)$ and $Y_{qd}(s)$ as they depend on $\beta_q(\mu)$ and $G_q(\mu)$, which determine i_{sq}.



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$

(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 3-3: Small-signal input dq admittance of six pulse diode rectifier: obtained from switching simulation model (green line with squares), analytical expression of modified AAVM (red dashed line) and scaled up expressions of modified AAVM (purple dashed line).

3.2.3 Small-signal dc impedance of AAVM

It is well known and already shown in several previous papers that AAVM captures very accurately small signal output DC impedance of the six-pulse diode rectifier. The analytical expression of the output impedance can be easily derived from 3-3. Furthermore, bode plot comparison of small-signal output dc impedance from switching simulation model and analytical expression given in 3-7 is shown in Figure 3-4.

Obviously, small-signal dc impedance of AAVM matches switching simulation model in a complete frequency range (1 Hz - 1000 Hz), implying that matching is achieved even beyond the switching frequency (360 Hz). In this case the output impedance is simple LC filter, whose resonant frequency point is at 123 Hz, where this resonant point is determined with both AC side inductance L_c and dc side L_{dc}-C_{dc} low-pass filter.

$$Z_{dcout} = \left(R_{cdc} + \frac{1}{sC_{dc}} \right) \| \left(R_1 + sL_1 \right); \qquad 3\text{–}9$$
$$R_1 = R_{ekv} + R_{ldc} + 2R_{lc}; \;\; L_1 = L_{dc} + 2L_c;$$

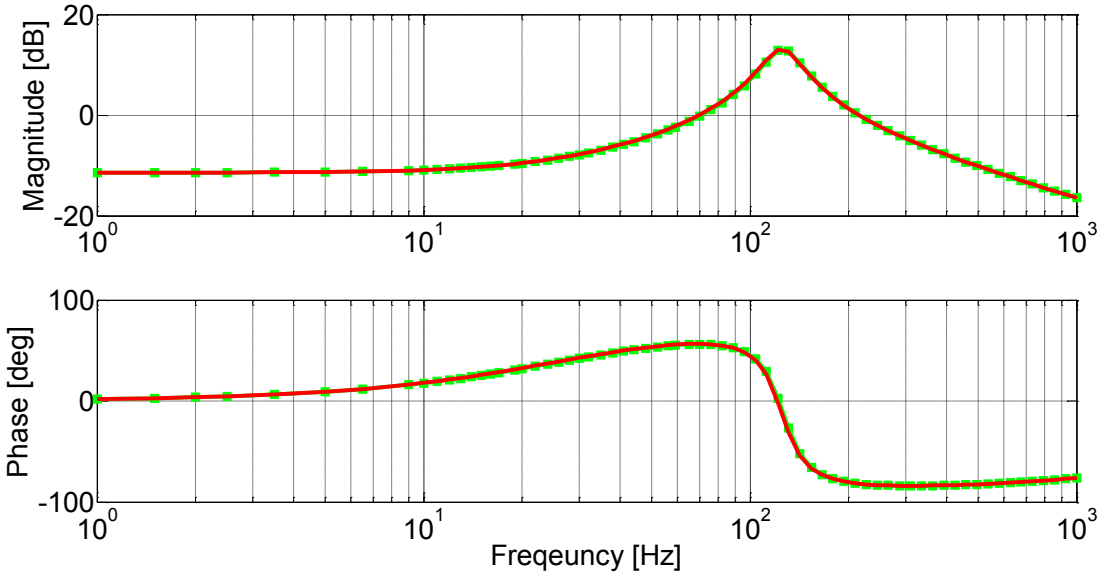


Figure 3-4: Small-signal output DC impedance of six-pulse diode rectifier: obtained from switching simulation model (green line with squares) and analytical expression of AAVM (red dashed line)

3.3 Parametric Averaged Value Modeling (PAVM)

A second averaged model used in the analysis is a PAVM presented in [77]-[78], in this case parameters of the model are calculated using steady state values of the currents and voltages from the switching simulation model. Equivalent circuit schematic of PAVM is shown in Figure 3-5, the equivalent model consists of two current controlled current sources to establish a relationship among dc side current and dq side currents; similarly there is a single voltage controlled voltage

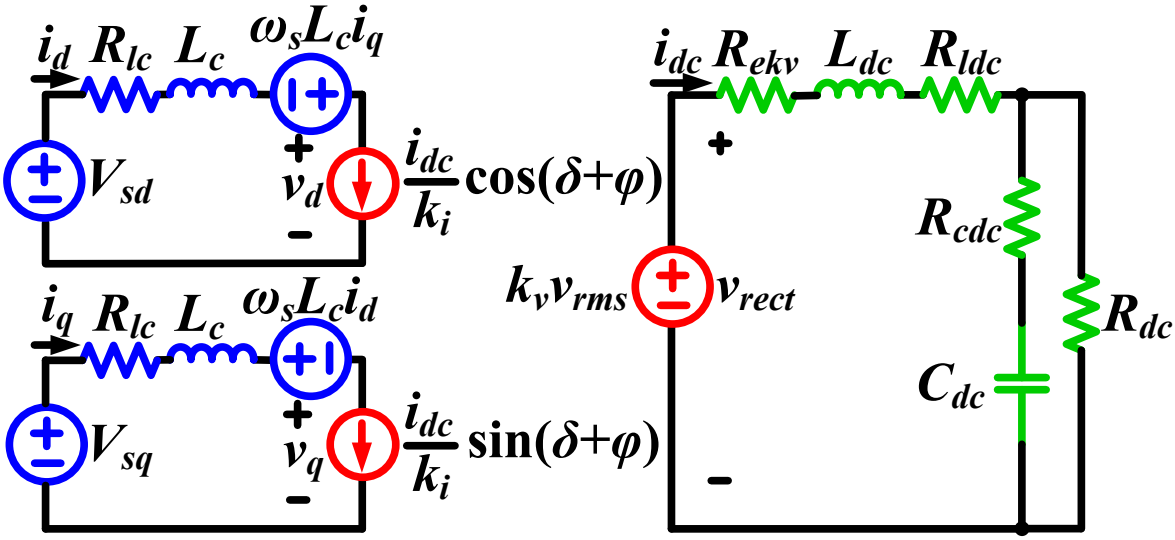


Figure 3-5: Equivalent circuit schematic representation of PAVM

source to establish a relationship among dq side voltages and dc side voltage. Furthermore, same equivalent resistor that is present in AAVM is used in PAVM, providing damping in the averaged model that happens in switching model due to commutation angle. Parameters of the controlled sources are derived from phasor diagram shown in Figure 3-6.

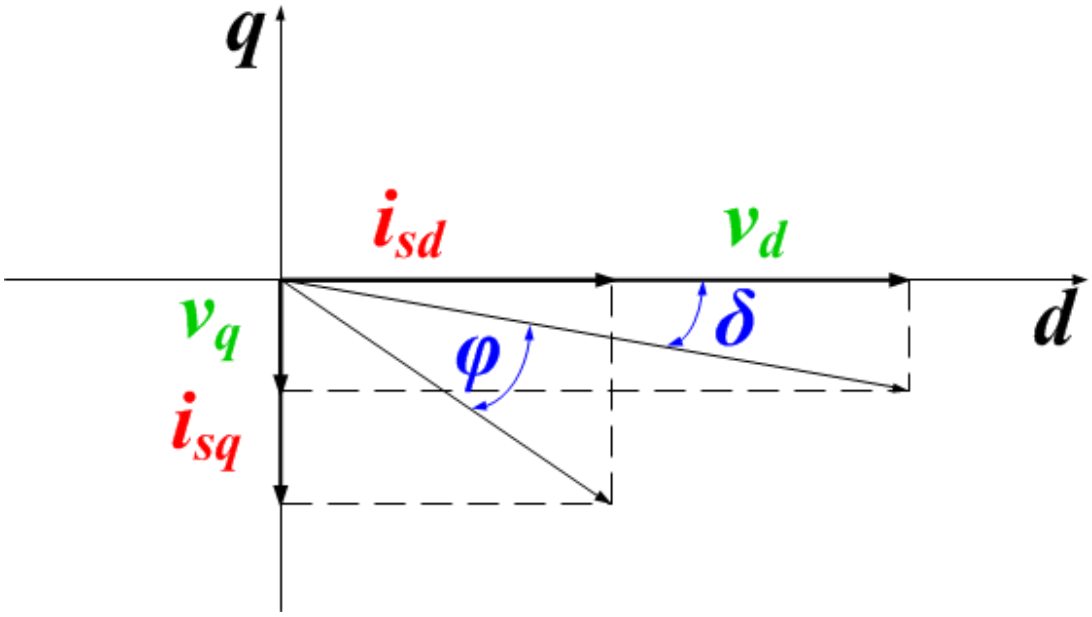


Figure 3-6: Phasor diagram of dq currents and dq voltages used in PAVM

3.3.1 Equivalent equations of PAVM

The equations, which describe PAVM are given below, where cos(δ) and sin(δ) are defined in similar manner as in (6), but ac voltages at diode bridge are used instead of voltage source.

$$\cos(\delta)=\frac{v_d}{\sqrt{v_d^2+v_q^2}},\ \sin(\delta)=\frac{v_q}{\sqrt{v_d^2+v_q^2}} \tag{3–10}$$

$$\begin{aligned}
&v_{sd}-R_{lc}i_{sd}-L_C\frac{di_{sd}}{dt}+\omega_s L_c i_q=v_d;\\
&v_{sq}-R_{lc}i_{sq}-L_C\frac{di_{sq}}{dt}-\omega_s L_c i_d=v_q;\\
&i_{sd}=\frac{i_{dc}}{k_i}\cos(\delta+\varphi);\ i_{sq}=\frac{i_{dc}}{k_i}\sin(\delta+\varphi);\\
&v_{rect}=k_v v_{rms}=k_v\sqrt{v_d^2+v_q^2}=Z_{dc}(D)i_{dc};
\end{aligned} \tag{3–11}$$

Similarly, the input dq admittance of a PAVM is derived via the linearization of (11) with respect to v_{sd} and v_{sq}.

$$Y(s)=\begin{bmatrix}Y_{dd}(s) & Y_{dq}(s)\\ Y_{qd}(s) & Y_{qq}(s)\end{bmatrix}=\begin{bmatrix}\frac{\tilde{i}_{sd}(s)}{\tilde{v}_{sd}(s)} & \frac{\tilde{i}_{sd}(s)}{\tilde{v}_{sq}(s)}\\ \frac{\tilde{i}_{sq}(s)}{\tilde{v}_{sd}(s)} & \frac{\tilde{i}_{sq}(s)}{\tilde{v}_{sq}(s)}\end{bmatrix} \tag{3–12}$$

The derivation process is even more cumbersome than in AAVM case, thus only the final expressions are provided below.

$$\begin{aligned}
&\begin{bmatrix}Y_{dd}(s)\\ Y_{qd}(s)\end{bmatrix}=\left(I+\vec{v}_1[Z_{dd}\quad Z_{dq}]+\vec{v}_2\begin{bmatrix}Z_{qd}\quad Z_{qq}\end{bmatrix}\right)^{-1}\vec{v}_1;\\
&\begin{bmatrix}Y_{dq}(s)\\ Y_{qq}(s)\end{bmatrix}=\left(I+\vec{v}_1[Z_{dd}\quad Z_{dq}]+\vec{v}_2\begin{bmatrix}Z_{qd}\quad Z_{qq}\end{bmatrix}\right)^{-1}\vec{v}_2;
\end{aligned} \tag{3–13}$$

$$\vec{v}_1=\begin{bmatrix}\frac{\cos(\Delta)}{k_{id}}-\frac{\sin(\Delta)}{k_{iq}}\\ \frac{\sin(\Delta)}{k_{id}}+\frac{\cos(\Delta)}{k_{iq}}\end{bmatrix}k_v\frac{\partial v_{rms}}{\partial v_d}Y_{dc}+\begin{bmatrix}\frac{1}{k_{id}}\frac{\partial\cos(\delta)}{\partial v_d}-\frac{1}{k_{iq}}\frac{\partial\cos(\delta)}{\partial v_d}\\ \frac{1}{k_{id}}\frac{\partial\sin(\delta)}{\partial v_d}+\frac{1}{k_{iq}}\frac{\partial\cos(\delta)}{\partial v_d}\end{bmatrix}; \tag{3–14}$$

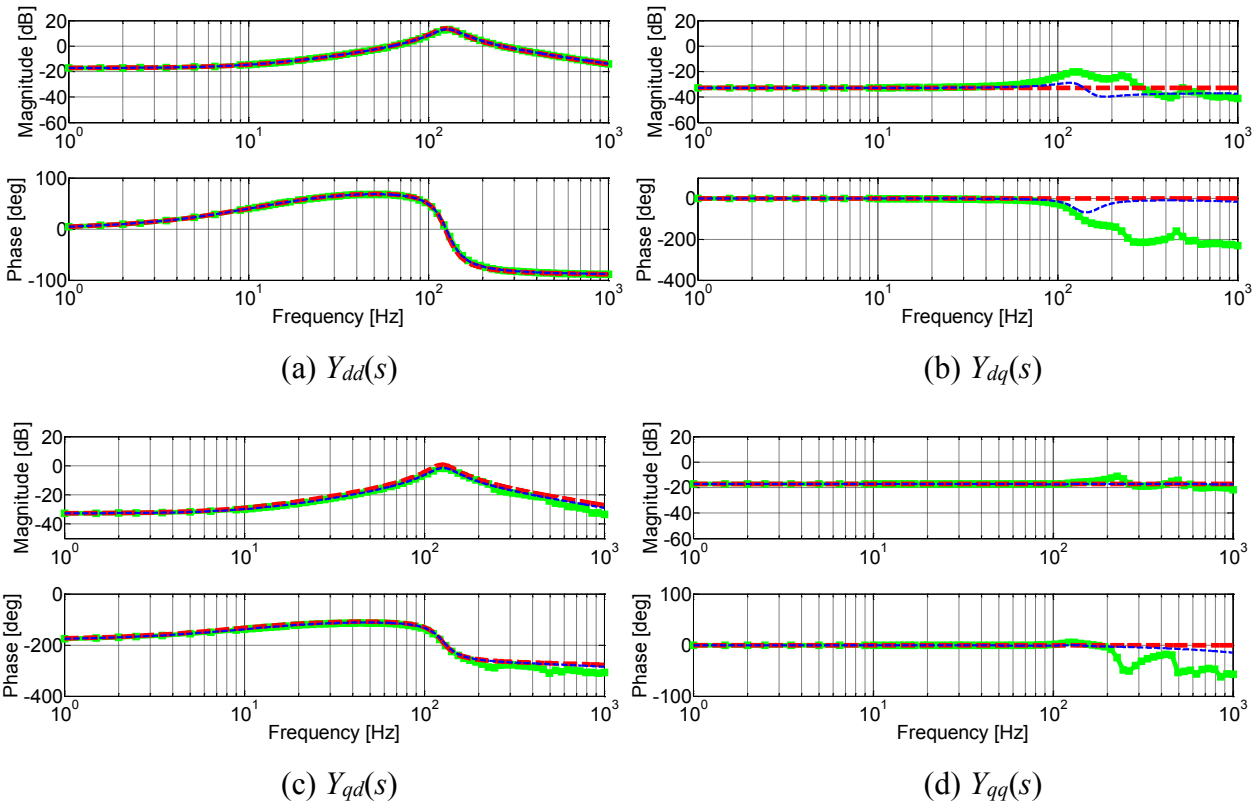
$$\vec{v}_2=\begin{bmatrix}\frac{\cos(\Delta)}{k_{id}}-\frac{\sin(\Delta)}{k_{iq}}\\ \frac{\sin(\Delta)}{k_{id}}+\frac{\cos(\Delta)}{k_{iq}}\end{bmatrix}k_v\frac{\partial v_{rms}}{\partial v_q}Y_{dc}+\begin{bmatrix}\frac{1}{k_{id}}\frac{\partial\cos(\delta)}{\partial v_q}-\frac{1}{k_{iq}}\frac{\partial\cos(\delta)}{\partial v_q}\\ \frac{1}{k_{id}}\frac{\partial\sin(\delta)}{\partial v_q}+\frac{1}{k_{iq}}\frac{\partial\cos(\delta)}{\partial v_q}\end{bmatrix} \tag{3–15}$$

$$\begin{bmatrix}Z_{dd} & Z_{dq}\\ Z_{qd} & Z_{qq}\end{bmatrix}=\begin{bmatrix}R_{lc}+sL_c & -\omega_s L_C\\ \omega_s L_C & R_{lc}+sL_c\end{bmatrix} \tag{3–16}$$

$$k_{id} = \frac{k_i}{\cos(\phi)};\ k_{iq} = \frac{k_i}{\sin(\phi)} \qquad 3\text{–}17$$

3.3.2 Small-signal dq admittance of PAVM

In this part obtained dq admittances from AVMs are compared to corresponding dq admittances of the switching simulation model. By applying the linearization techniques around dc operating point, it is possible to obtain small-signal dq admittance of AVMs. Either the derived analytical expressions or small-signal frequency characteristics obtained by the linearization



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$

(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 3-7: Diode rectifier input dq admittances: switching model (green squared straight line), analytical expression of modified AAVM (red dashed line), analytical expression of PAVM (blue dashed line) (a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$ (c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$.

technique can be used to identify the small-signal dq admittance, as both approaches yield same results.

The comparison of input dq admittances, obtained from the switching model and analytical expressions of AAVM 3-5 and of PAVM 3-7 to 3-9, is shown in Figure 3-7. It can be concluded from the figure that all four admittances have the resonant point at 123 Hz, which is the resonant point of LC filter present in the rectifier. Obviously, the input dq admittance derived from the

AVMs match the two admittances obtained from the switching model, $Y_{dd}(s)$ and $Y_{qd}(s)$, even beyond the switching frequency. This is explained by the fact that d-channel injection behaves like a magnitude injection, which is obviously more linear as it does not modulate commutation angle. Furthermore, both AVMs accurately model admittance $Y_{qq}(s)$ up to half the switching frequency (180 Hz), predicting that $Y_{qq}(s)$ behaves like a resistor in the low frequency range. In the high frequency range (above 180 Hz) there are resonant points present that are not captured by AVMs. Similarly, both AVMs predict admittance $Y_{dq}(s)$ correctly up to 100 Hz, but there is also significant dynamic present in the admittance $Y_{dq}(s)$, which is not captured by AVMs. Furthermore, q-channel injection generates significant sideband admittance response at 237 Hz, at 483 Hz, at 597 Hz, and at 843 Hz due to the modulation of the commutation angle, which is the typical behavior of nonlinear loads, behaving more like a nonlinear injection.

3.4 Modeling of a hardware set-up

This section describes a hardware example and input dq admittance measurement of the six-pulse diode rectifier obtained with dq impedance measurement unit (IMU). It is shown that a switching simulation model can predict hardware dq admittance if all the components are known and precisely modeled. For this purpose a six-pulse diode rectifier is built and measured with the three-phase AC IMU, which is developed to measure dq impedances/admittances at three-phase

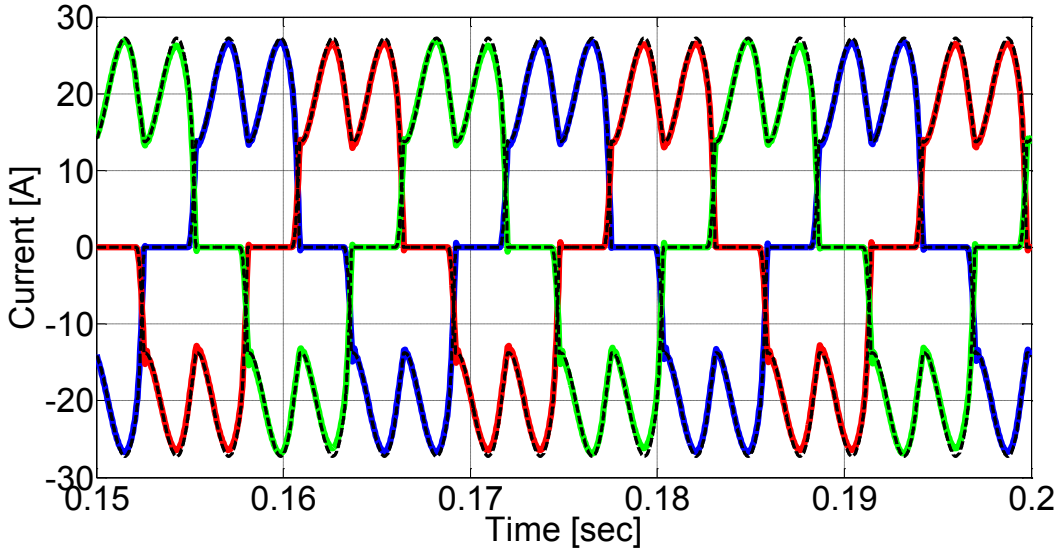
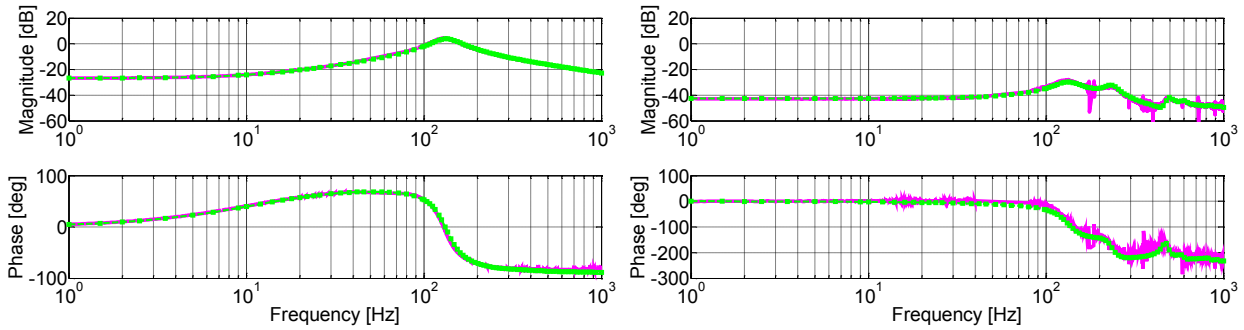


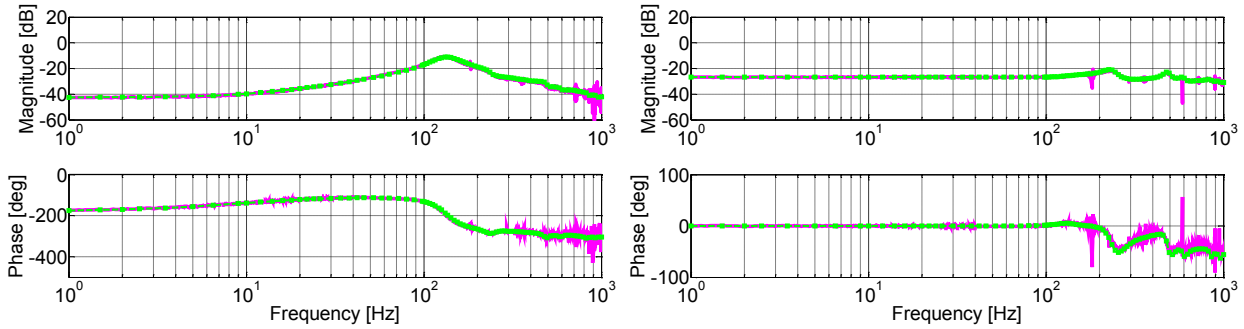
Figure 3-8: Time-domain comparison of simulation model (dashed black line) with hardware waveforms (straight blue, red and green lines)

AC interfaces [96]. The IMU hardware is modeled in Simulink and built model is compared to hardware in both time-domain and frequency-domain. Figure 3-8 shows steady-state time-domain comparison ac side currents of the diode rectifier from the simulation model with corresponding waveforms of the hardware set-up. The obtained waveforms show almost perfect matching between a simulation model and hardware set-up, which is achieved by tuning process throughout several iterations. At the beginning of the tuning process the matching was not achieved as IMU adds parasitic inductive value to the AC side, thus it required an adjustment of the simulation model accordingly. Only after the adding 80 μH parasitic inductor to AC side, the commutation angle of the rectifier was modified to match the one happening in the hardware.

Figure 3-9 shows comparison of small-signal dq admittances obtained by hardware measurements and by switching model simulations. The extraction of small-signal input dq admittance from the switching simulation model matches hardware measurements in the whole frequency range of interest, where nonlinear sideband effects on admittances are captured



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$



(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 3-9: Input dq admittance of six-pulse diode rectifier obtained from the switching simulation model (green squared line) and by hardware measurements (purple straight line) (a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$ (c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$.

accurately. New poles, around multiples of switching frequency, are identified from the switching simulation results with the usage of MATLAB identification toolbox and identification functions. This proves that small-signal analysis performed on switching simulation model is very close to the real hardware measurements. The linearized AVMs are correct only up to certain frequency point, providing not so accurate modeling results in the higher frequency range. The nature of averaging is such that it can be trusted mostly up to half the switching frequency, especially if the considered model exhibits strong nonlinear behavior. The strength of the shown modeling is that it captured nonlinear effects, which were not observed by AVMs as they are just linear approximations of the switching models.

In order to fully characterize the usefulness of AVM model it is necessary to perform several comparisons like the steady-state and transient analysis in time domain, but it is also necessary to fully characterize the used AVM in the frequency domain. It is not enough to look only at DC side as AVMs predict small-signal DC impedance very accurately. The explanation is that DC side injection mainly affects d coordinate of currents and voltages, which behave very linearly. By looking into dq small signals characteristics the complete evaluation of AVM is performed.

3.5 Six-pulse diode rectifier feeding a constant power load

This section describes an example of six-pulse diode rectifier feeding a constant power load that behaves like negative resistance in the small-signal sense. The constant power load is realized as a three-phase voltage source inverter (VSI) with inner current loop and outer voltage loops closed. The circuit schematic of the described example is given in Figure 3-10: Circuit schematic

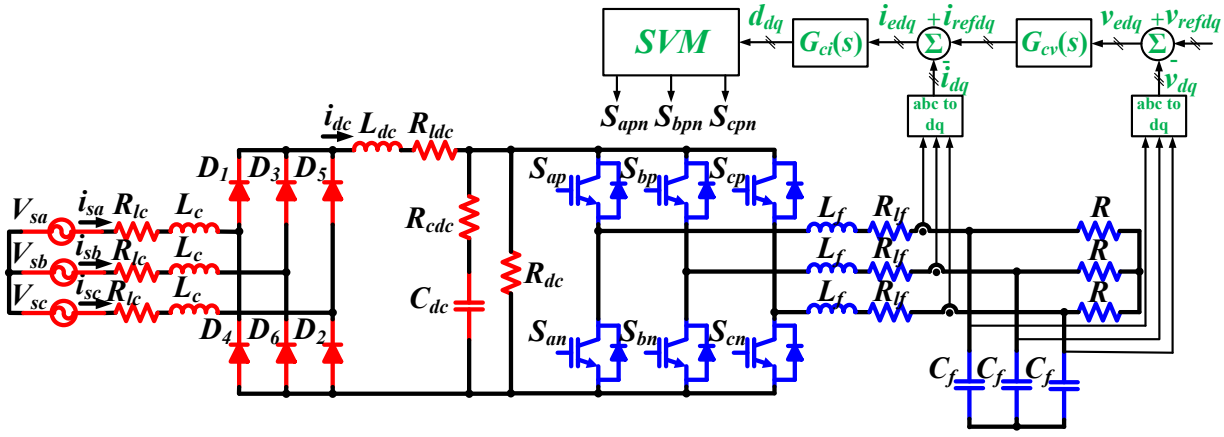


Figure 3-10: Circuit schematic of a six-pulse diode rectifier feeding a three-phase voltage source inverter

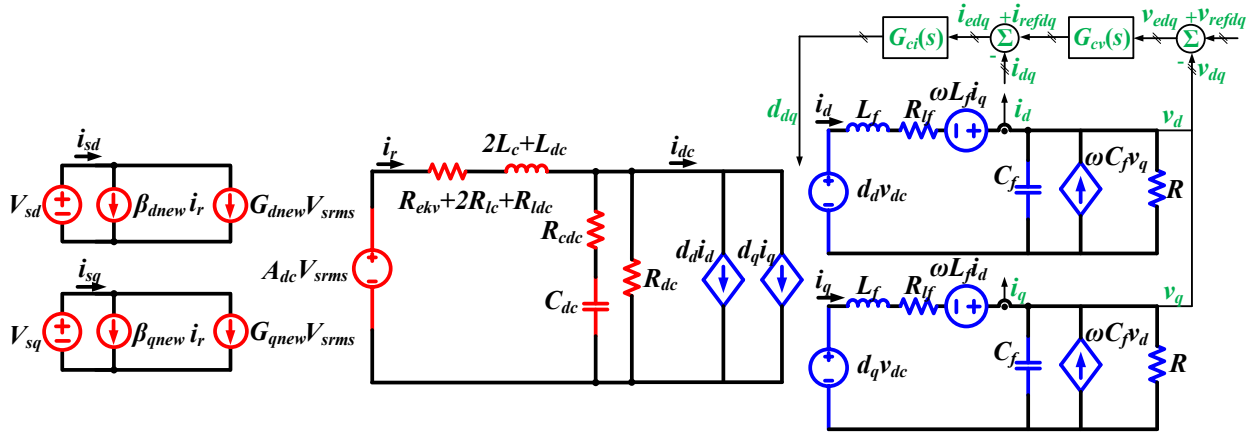


Figure 3-11: Circuit schematic of AAVM of six-pulse diode rectifier feeding a three-phase voltage source inverter

of a six-pulse diode rectifier feeding a three-phase voltage source inverter. Three-phase VSI is realized as a conventional two-level converter that has a simple L-C filter with a pure resistive load on AC side. The inner current loop is closed to have approximately 700 Hz bandwidth and a phase margin of 70 degrees, while the outer voltage loop is designed to have 200 Hz bandwidth with a phase margin of 65 degrees. Same parameters of the six pulse diode rectifier are used in this section. The parameters of three-phase VSI are given in Table 3-2.

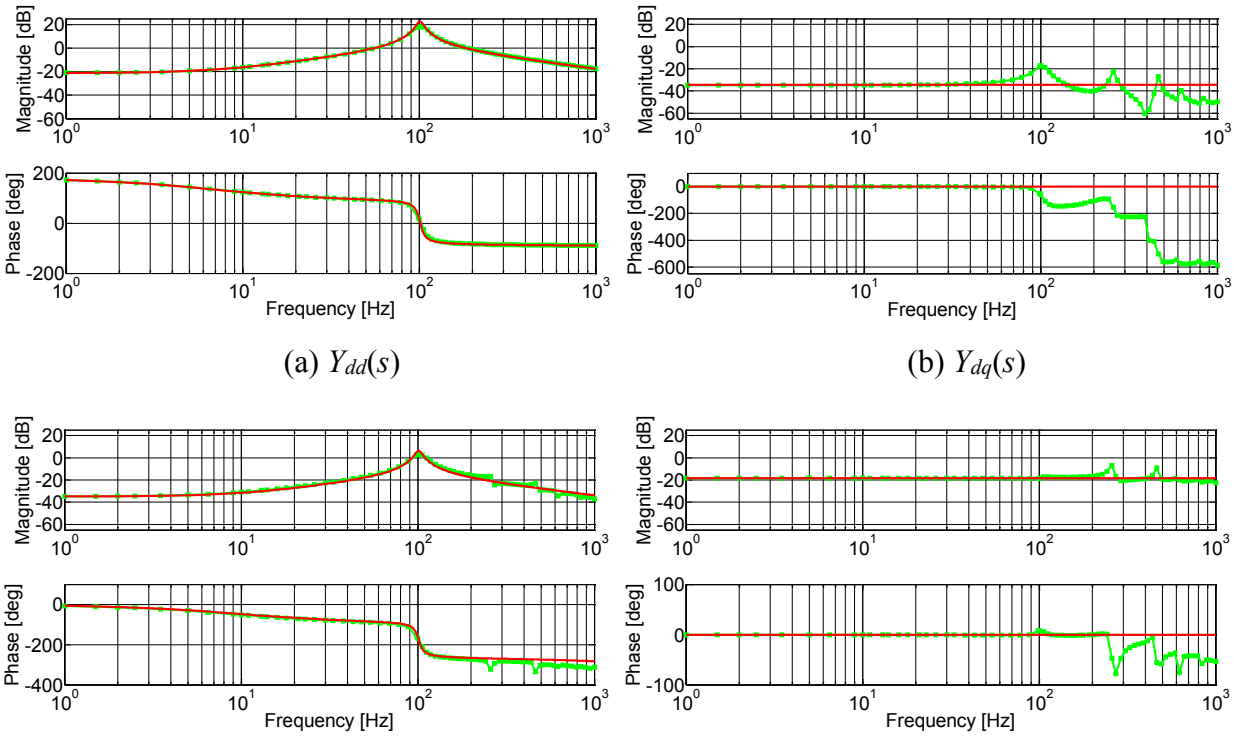
Table 3-2 Parameters of three-phase VSI

Parameter name	*Parameter values*	
AC Inductor	L_f=0.44 mH	R_{lc}=50 mΩ;
AC Capacitor	C_f=50 μF	R_{cf}=10 mΩ
Resistors	R=7 Ω	R_{dc}=100 Ω

This example is only analyzed in the simulations with the help of MATLAB and SimPowerSystems toolbox. In order to obtain input dq admittance of a switching model, small-signal analysis is performed. Series voltage injection is used to perturb AC side of the six-pulse diode rectifier in dq coordinates. The obtained small-signal dq admittance is shown in Figure 3-12.

Furthermore, an averaged model is developed to characterize the small-signal dq admittance of six-pulse diode rectifier feeding a three-phase VSI. Modified AAVM according to (5) is used to model a six-pulse diode rectifier, while the well-known classical averaged model is used for a three-phase VSI as shown in Figure 3-11. Although it is possible to use either PAVM or modified AAVM for modeling of six-pulse diode rectifier, due to the space limitation only one averaged model is presented in the analysis. However, there are no any restrictions to generalize the results

to PAVM. Input dq admittance of the averaged model is calculated by the linearization of model around steady-state DC operating point. Once dq admittance is calculated, the comparison of small-signal dq admittance of both switching and averaged model is shown in Figure 3-12.



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$

(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 3-12: Input dq admittance of diode rectifier feeding a constant power load obtained from the switching simulation model (green straight line with squares) and by linearization of averaged model (red straight line) (a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$ (c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

3.6 Summary

This chapter compares input dq admittances obtained from AVMs, switching simulation model results and hardware measurements. AAVM is modified to correct low frequency values of admittances $Y_{dq}(s)$ and $Y_{qq}(s)$ and PAVM model is modified to include damping resistor R_{ekv}. Furthermore, analytical expressions of the input dq admittance of both AVMs are derived, proving that AVMs can predict precisely admittances $Y_{dd}(s)$ and $Y_{qd}(s)$ even in the frequency range beyond the switching frequency as d-channel injection behaves as linear injection. Admittance $Y_{qq}(s)$ is predicted accurately up to half the switching frequency, while admittance $Y_{dq}(s)$ is predicted accurately up to one fourth of the switching frequency. This is explained by the fact that there are sideband admittances around multiples of switching frequency in admittances $Y_{dq}(s)$ and $Y_{qq}(s)$,

due to the q-channel injection. Finally, it is shown that if the hardware set-up is modeled precisely, then the switching simulation model can provide accurate small-signal input dq admittances in the entire frequency range of interest, capturing nonlinear sideband effects. This chapter shows new effect, sideband admittances around multiples of switching frequency, which was not previously observed in the six-pulse diode rectifiers. The new phenomenon is accurately captured both in hardware measurements and in switching simulation model with the use of developed small-signal extraction technique.

Chapter 4. Modeling of Small-Signal Input dq Admittance of Twelve-Pulse Diode Rectifiers

This chapter focuses on the modeling of small-signal input dq admittance of twelve-pulse diode rectifiers. It provides a comprehensive comparison of small-signal dq admittances between well-known averaged value model (AVM), switching simulation model and experimental measurements of a hardware set-up. Analytical AVM (AAVM) is used in the analysis as it has been commonly used to model diode rectifiers. In order to predict small-signal dq admittance accurately, AAVM had to be modified. The modification describes injection properties in a more natural way by considering a d-channel perturbation as magnitude modulation and by considering a q-channel perturbation as phase modulation. Analytical expressions for dq admittance of AAVM of twelve-pulse diode rectifier feeding a resistive load are derived and presented in the paper. Furthermore, it has been found that sideband admittances around multiples of switching frequency exist in the small-signal response due to the nonlinear behavior of the rectifier. The new phenomenon is analyzed theoretically, characterized in simulations with the extraction of small-signal response from the switching simulation model and captured experimentally by the hardware measurements.

4.1 Introduction

Modern power systems commonly used in aircraft, ship, automotive and grid vehicles, as well as synchronous generator and wind power generator microgrid systems have three-phase ac interface feeding different electronic power loads. Almost all of the electronic loads in such system exhibit negative resistance small-signal impedance behavior due to the wide usage of constant power control. In many such applications, the small-signal stability of these systems becomes an important issue. Although, there are numerous approaches to investigate and estimate stability of those systems, the most commonly used approach is determination of the stability through the input/output ratio of small-signal impedances. If system stability is investigated at dc interface,

measurements and analysis of the impedance ratio is relatively straight forward task. However, in the case of three-phase system, stability analysis can be performed at three-phase interface via the measurements of small-signal impedances in rotating reference frame, for example magnitude invaraiant dq transformation, as used in the previous chapter.

$$T_{dqo}(\theta)=\frac{2}{3}\begin{bmatrix}\cos(\theta) & \cos\left(\theta-\frac{2\pi}{3}\right) & \cos\left(\theta+\frac{2\pi}{3}\right)\\ -\sin(\theta) & -\sin\left(\theta-\frac{2\pi}{3}\right) & -\sin\left(\theta+\frac{2\pi}{3}\right)\\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2}\end{bmatrix} \quad 4\text{–}1$$

Obtained small-signal dq impedances are extracted in the matrix form and the return ratio becomes product of source dq impedance and load dq admittance as written below. The stability of such power system is assessed by Generalized Nyquist Criterion (GNC) or simplified GNC [19]–[21].

$$L(s)=Z_{sdq}(s)Y_{ldq}(s) \quad 4\text{–}2$$

$$Z_{sdq}(s)=\begin{bmatrix}Z_{dd}(s) & Z_{dq}(s)\\ Z_{qd}(s) & Z_{qq}(s)\end{bmatrix}, Y_{ldq}(s)=\begin{bmatrix}Y_{dd}(s) & Y_{dq}(s)\\ Y_{qd}(s) & Y_{qq}(s)\end{bmatrix} \quad 4\text{–}3$$

Matrix $Z_{sdq}(s)$ is the small-signal dq impedance of the source side, with two impedances $Z_{dd}(s)$ and $Z_{qd}(s)$, standing for the responses to d-channel perturbation, and other two impedances $Z_{dq}(s)$ and $Z_{qq}(s)$, being response to q-channel perturbation. Similarly, matrix $Y_{ldq}(s)$ is the small-signal dq admittance of the load side, with two admittances $Y_{dd}(s)$ and $Y_{qd}(s)$, standing for two admittances that are responses to a small-signal voltage perturbation via d-channel. In a same manner, admittances $Y_{dq}(s)$ and $Y_{qd}(s)$ are defined as admittances, which are obtained as current responses to small-signal voltage perturbation via q-channel.

$$Z_{dd}(s)=\frac{\tilde{v}_d(s)}{\tilde{i}_d(s)}|_{\tilde{i}_q(s)=0}; Z_{qd}(s)=\frac{\tilde{v}_q(s)}{\tilde{i}_d(s)}|_{\tilde{i}_q(s)=0}; \quad 4\text{–}4$$

$$Z_{dq}(s)=\frac{\tilde{v}_d(s)}{\tilde{i}_q(s)}|_{\tilde{i}_d(s)=0}; Z_{qq}(s)=\frac{\tilde{v}_q(s)}{\tilde{i}_q(s)}|_{\tilde{i}_d(s)=0}; \quad 4\text{–}5$$

$$Y_{dd}(s)=\frac{\tilde{i}_d(s)}{\tilde{v}_d(s)}|_{\tilde{v}_q(s)=0};Y_{qd}(s)=\frac{\tilde{i}_q(s)}{\tilde{v}_d(s)}|_{\tilde{v}_q(s)=0}; \quad 4\text{–}6$$

$$Y_{dq}(s)=\frac{\tilde{i}_d(s)}{\tilde{v}_q(s)}|_{\tilde{v}_d(s)=0};Y_{qq}(s)=\frac{\tilde{i}_q(s)}{\tilde{v}_q(s)}|_{\tilde{v}_d(s)=0}; \quad 4\text{–}7$$

One typical rectifier circuit in such three-phase power systems is a twelve-pulse diode rectifier feeding resistive load or constant power load. This paper concentrates on the modeling of input dq admittance of twelve-pulse diode rectifier using the test-case model given in Figure 4-1. The considered rectifier consists of phase shifting transformer followed by two sets of inductors L_{c1} and L_{c2}, two three-phase diode bridges, an 1:1 transformer operating as an inner phase reactor (IPR) and a low pass L_{dc}-C_{dc} filter feeding a resistive load. Parameters of a twelve-pulse diode rectifier are depicted in Table 4-1.

Table 4-1 Parameters of twelve-pulse diode rectifier

Source voltage	V_{sm}=120 V	DC inductance	L_{dc}=1.6 mH
Source frequency	f_s=60 Hz	Ser. resistance	R_{ldc}=60 mΩ
Leakage inductances of the inner phase tranformer	L_{lk1}=200 μH L_{lk2}=200 μH	Magnetizing inductance of the inner phase tranformer	L_m=830 μH
AC inductance	L_{c1}=220 μH L_{c2}=220 μH	DC capacitance	C_{dc}=1.05 mF
Series resistance	R_{lc1}=R_{lc2}=30 mΩ	Series resistance	R_{cdc}=30 mΩ
DC resistance	R_{dc}=12.8 Ω	Parasitic inductance of dc side resistor	L_{rdc}=10 μH

The previous research on small-signal modeling of multi-pulse diode rectifiers mainly concentrated on dc impedance characterization. In addition, time-domain modeling main focus was on harmonic content of input currents of the rectifier under unbalanced load conditions, unbalances in the voltage source, load step changes, etc. The small-signal modeling of ac side of line commutated rectifiers using a positive sequence perturbation and negative sequence perturbation is explained in [23], [83]. The proposed method uses switching mapping functions and Fourier series analysis to calculate response to small-signal perturbation, effectively providing an analytical way to calculate small-signal ac impedance. In this case, the obtained small-signal ac impedance maps dc side impedance via the used current and voltage switching mapping functions. The previous approach is successfully extended to general frequency domain modeling of multi-pulse diode rectifiers using double Fourier series analysis in [90].

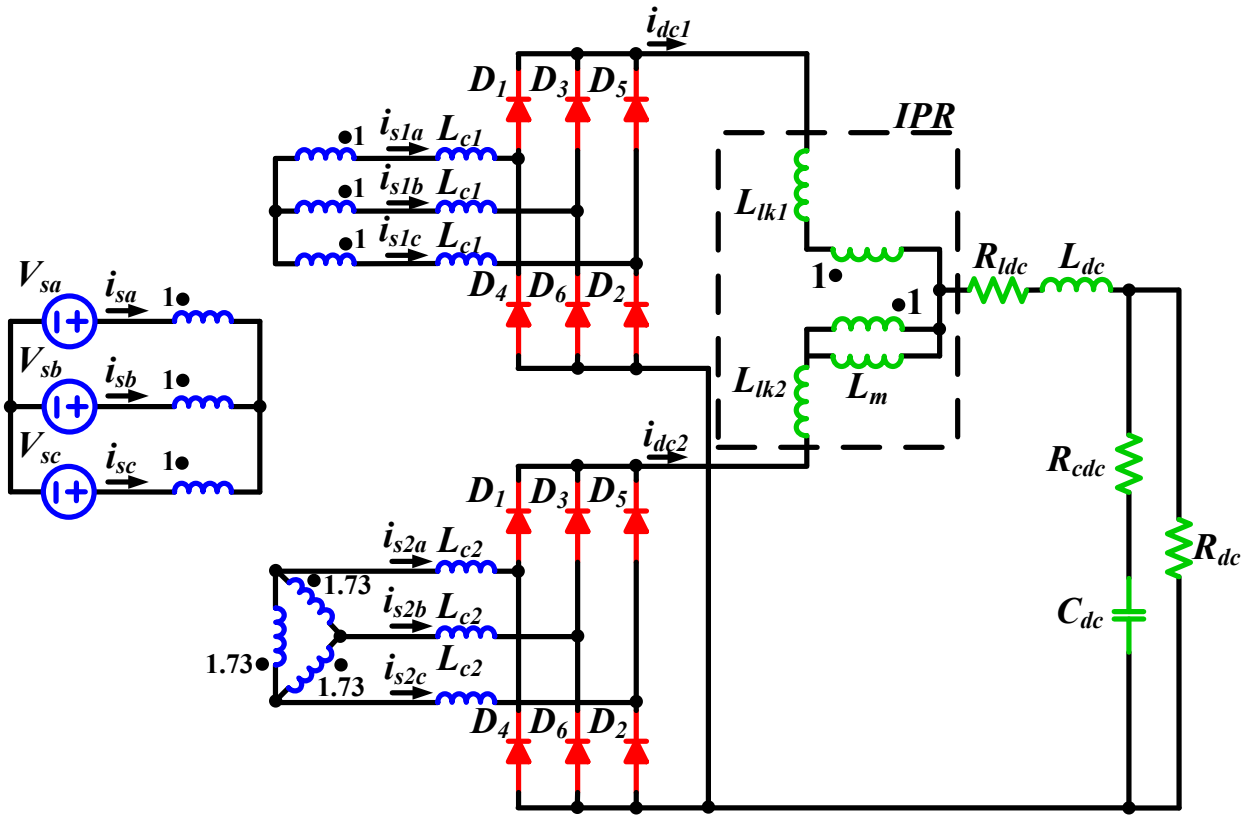


Figure 4-1: Switching model of twelve-pulse diode rectifier with resistive load.

Furthermore, multi-pulse diode rectifier is analyzed with respect to positive and negative sequence perturbations in [89], additionally in this case the effect of front end inductance value on the commutation angle is included in the analysis. A generalized modeling approach for six-pulse diode rectifier with respect to positive and negative sequence perturbations, which includes both ac and dc side filter dynamic is presented in [121]. The accuracy range of the presented model is improved, showing the matching between small-signal impedances of the switching and averaged model several times beyond the switching frequency. Large-signal and small-signal evaluation of averaged models for multi-pulse diode rectifiers is given in [79].

The extensive modeling of small-signal input dq admittances of six-pulse diode rectifiers using both analytical and parametric averaged value models is carried out in the previous chapter. The sideband admittances around multiples of switching frequency are captured both in simulation results and by the hardware measurements. The presence of the sideband admittances is contributed to the nonlinear behavior of the rectifier. The explanation is that q-channel injection behaves like phase modulation, which modulates commutation angle of the rectifier, yielding

responses around the multiples of the switching frequency. Furthermore, the presented modeling of the rectifier is validated with the constant power load. This chapter extends the modeling story previously explained to the twelve-pulse diode rectifier case, providing accurate model for the extraction of small-signal input dq admittance. Nevertheless, the presented model is easily expandable to multi-pulse diode rectifiers, as well as to phase-controlled line-frequency rectifiers.

The chapter is organized in the following manner, the first section derives equivalent AAVM equations and provides analytical expressions for small-signal dq admittances. The comparison of averaged model and switching model admittances is presented and validity range of the averaged model is estimated. Small-signal dq admittance of switching simulation model is obtained in 121 frequency point via series voltage injection, by applying FFT algorithm and by sweeping the frequency of voltage soruce. Second section gives experimental validation by providing comparison of dq admittances obtained by hardware measurements and by small-signal extraction from switching simulation model. In all the presented test-cases sideband resonant responses around multiples of switching frequency are captured and contributed to the nonlinear behavior of the rectifier.

4.2 Analytical Averaged Value Modeling (AAVM)

The analytical AVM (AAVM) is a widely used solution for modeling a twelve-pulse diode rectifier [84]-[85]. AAVM has been derived using equations that describe physical operation of twelve-pulse diode rectifier. The key assumption used in the derivation procedure is to neglect current ripple of DC side inductor current, concentrating only on a dc current component. This fact severely limits the usability of the model as it provides modeling with smaller and larger error values depending on the filter parameters on the dc-side. Therefore, the more accurate is the assumption, the more accurate results with AAVM will be obtained and vice versa the less accurate is the assumption, the less accurate results with AAVM will be obtained. In the used example it is shown that AAVM fails to predict correct steady-state value of current source q-axis component, which leads to noticeable error in small-signal analysis when AAVM is used. The error is eliminated if proper scaling is applied.

AAVM maps all the dynamics from AC side to DC side as depicted in the equivalent averaged model circuit given in [83]. The complete derivation of AAVM is algebraically intensive and already covered in several publications [86]-[88]. This chapter goal is to focus on modeling of small-signal dq admittances, thus the equivalent AAVM equations for a twelve-pulse diode rectifier are only stated here.

The first set of equations describes the first diode bridge behavior using the parameters, which are aligned with the input voltage. Similarly, the second set of equations describes the second diode bridge using the parameters, which are aligned with a voltage shifted by 30 degrees.

$$\begin{aligned} i_{s1d} &= \beta_{d1}(\mu) i_{dc1} + G_{d1}(\mu) v_{s1rms}; \\ i_{s1q} &= \beta_{q1}(\mu) i_{dc1} + G_{q1}(\mu) v_{s1rms}; \\ v_{rect1} &= A_{dc} v_{s1rms} = A_{dc}\sqrt{0.5}\sqrt{v_{s1d}^2 + v_{s1q}^2} \end{aligned} \quad 4\text{–}8$$

$$\begin{aligned} i_{s2d} &= \beta_{d2} i_{dc2} + G_{d2} v_{s2rms}; \\ i_{s2q} &= \beta_{q2} i_{dc2} + G_{q2} v_{s2rms}; \\ v_{rect2} &= A_{dc} v_{s2rms} = A_{dc}\sqrt{0.5}\sqrt{v_{s2d}^2 + v_{s2q}^2} \end{aligned} \quad 4\text{–}9$$

The three-phase phase shifting transformer is assumed to be ideal and influence of the phase shifting is modeled via the following equations.

$$\begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} i_{s1d} \\ i_{s1q} \end{bmatrix} + \begin{bmatrix} \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} i_{s2d} \\ i_{s2q} \end{bmatrix}; \quad 4\text{–}10$$

$$\begin{aligned} \begin{bmatrix} v_{s1d} \\ v_{s1q} \end{bmatrix} &= \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix}; \\ \begin{bmatrix} v_{s2d} \\ v_{s2q} \end{bmatrix} &= \begin{bmatrix} \frac{\sqrt{3}}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{\sqrt{3}}{2} \end{bmatrix} \begin{bmatrix} v_{sd} \\ v_{sq} \end{bmatrix} \end{aligned} \quad 4\text{–}11$$

The parameters used in the previous equations to describe the average model are functions of the diode bridge commutation angle μ, source line angular speed ω_s and commutating inductances L_{c1} and L_{c2}.

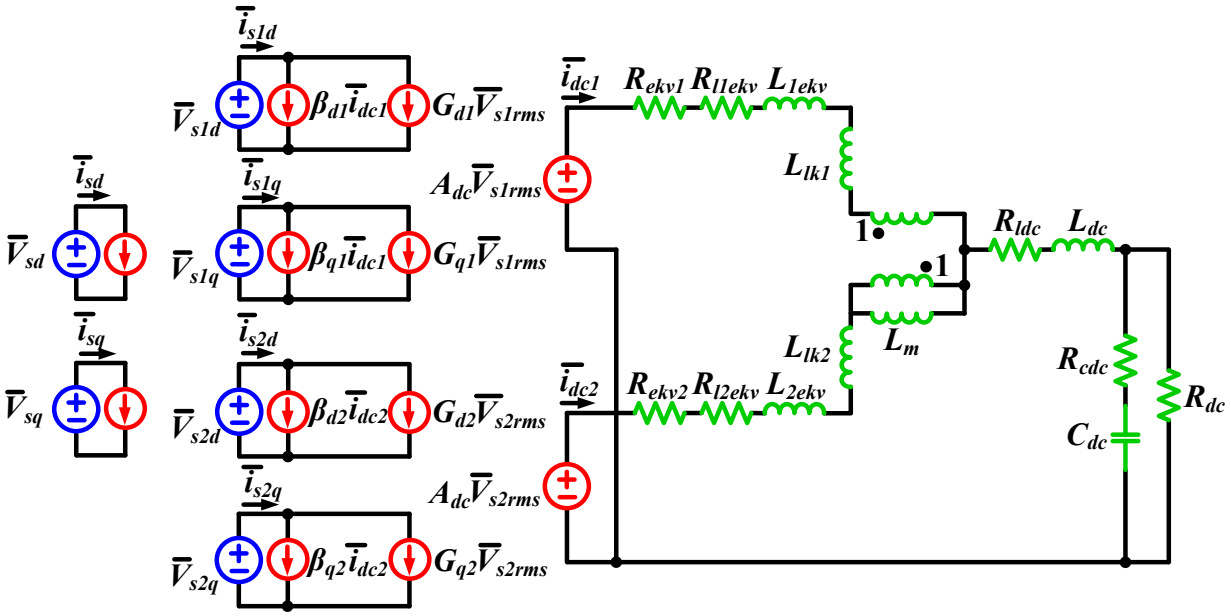


Figure 4-2: Averaged model of twelve-pulse diode rectifier with resistive load.

$$\beta_{d1}(\mu)=\frac{2\sqrt{3}}{\pi}\cos(\mu);\ \ \beta_{q1}(\mu)=-\frac{2\sqrt{3}}{\pi}\sin(\mu);\ \ A_{dc}=\frac{3\sqrt{6}}{\pi};$$
$$G_{d1}(\mu)=\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_{C1}}(\cos(2\mu)-4\cos(\mu)+3); \qquad 4\text{–}12$$
$$G_{q1}(\mu)=-\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_{C1}}(\sin(2\mu)-4\sin(\mu)+2\mu)$$

$$\beta_{d2}(\mu)=\frac{2\sqrt{3}}{\pi}\cos\left(\mu+\frac{\pi}{6}\right);\ \ \beta_{q2}(\mu)=-\frac{2\sqrt{3}}{\pi}\sin\left(\mu+\frac{\pi}{6}\right);\ \ A_{dc}=\frac{3\sqrt{6}}{\pi};$$
$$G_{d2}(\mu)=\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_{C1}}\left(\cos\left(2\mu+\frac{\pi}{6}\right)-4\cos\left(\mu+\frac{\pi}{6}\right)-\mu+1.5\sqrt{3}\right); \qquad 4\text{–}13$$
$$G_{q2}(\mu)=-\frac{3\sqrt{2}}{4\pi}\frac{1}{\omega_s L_{C1}}\left(\sin\left(2\mu+\frac{\pi}{6}\right)-4\sin\left(\mu+\frac{\pi}{6}\right)+\sqrt{3}\mu+1.5\right)$$

$$R_{ekv1}=\frac{3}{\pi}(L_{C1}+L_{TRP}+L_{TRS1})\omega_s;\ \ L_{1ekv}=2(L_{C1}+L_{TRP}+L_{TRS1});$$
$$R_{ekv2}=\frac{3}{\pi}(L_{C2}+L_{TRP}+L_{TRS2})\omega_s;\ \ L_{2ekv}=2(L_{C2}+L_{TRP}+L_{TRS2}); \qquad 4\text{–}14$$

4.2.1 Small-signal model of AAVM

In order to obtain accurate estimate of the small-signal dq input admittance of AAVM, 4-3 has to be modified in the following manner.

$$\begin{bmatrix} i_{s1dm} \\ i_{s1qm} \end{bmatrix} = \begin{bmatrix} \cos(\delta_1) & -\sin(\delta_1) \\ \sin(\delta_1) & \cos(\delta_1) \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \end{bmatrix} = \begin{bmatrix} \cos(\delta_1) & -\sin(\delta_1) \\ \sin(\delta_1) & \cos(\delta_1) \end{bmatrix} \begin{bmatrix} \beta_{d1}(\mu) i_{dc1} + G_{d1}(\mu) v_{s1rms} \\ \beta_{q1}(\mu) i_{dc1} + G_{q1}(\mu) v_{s1rms} \end{bmatrix} \quad 4\text{–}15$$

$$\begin{bmatrix} i_{s2dm} \\ i_{s2qm} \end{bmatrix} = \begin{bmatrix} \cos(\delta_2) & -\sin(\delta_2) \\ \sin(\delta_2) & \cos(\delta_2) \end{bmatrix} \begin{bmatrix} i_{sd2} \\ i_{sq2} \end{bmatrix} = \begin{bmatrix} \cos(\delta_2) & -\sin(\delta_2) \\ \sin(\delta_2) & \cos(\delta_2) \end{bmatrix} \begin{bmatrix} \beta_{d2}(\mu) i_{dc2} + G_{d2}(\mu) v_{s2rms} \\ \beta_{q2}(\mu) i_{dc2} + G_{q2}(\mu) v_{s2rms} \end{bmatrix} \quad 4\text{–}16$$

Where $\cos(\delta_1)$, $\sin(\delta_1)$, $\cos(\delta_2)$ and $\sin(\delta_2)$ are defined via dq parameters of the source voltage as follows.

$$\begin{aligned} \cos(\delta_1) &= \frac{v_{s1d}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}}; \\ \sin(\delta_1) &= \frac{v_{s1q}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}}; \end{aligned} \quad 4\text{–}17$$

$$\begin{aligned} \cos(\delta_2) &= \frac{v_{s2d}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}}; \\ \sin(\delta_2) &= \frac{v_{s2q}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}}; \end{aligned} \quad 4\text{–}18$$

The proposed modification tries to model d-channel perturbation as a magnitude modulation, while it models the q-channel perturbation as a phase modulation. Moreover, the described modification does not change the operating point, leaving the large signal nonlinear averaged model same, but modifying only the small-signal perturbation influence. The modified AAVM of twelve-pulse diode rectifier are written below.

$$\begin{bmatrix} i_{s1dm} \\ i_{s1qm} \end{bmatrix} = \begin{bmatrix} \frac{v_{s1d}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}} & -\frac{v_{s1q}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}} \\ \frac{v_{s1q}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}} & \frac{v_{s1d}}{\sqrt{v_{s1d}^2 + v_{s1q}^2}} \end{bmatrix} \begin{bmatrix} \beta_{d1}(\mu) i_{dc1} + G_{d1}(\mu) v_{s1rms} \\ \beta_{q1}(\mu) i_{dc1} + G_{q1}(\mu) v_{s1rms} \end{bmatrix} \quad 4\text{–}19$$

$$\begin{bmatrix} i_{s2dm} \\ i_{s2qm} \end{bmatrix} = \begin{bmatrix} \frac{v_{s2d}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}} & -\frac{v_{s2q}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}} \\ \frac{v_{s2q}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}} & \frac{v_{s2d}}{\sqrt{v_{s2d}^2 + v_{s2q}^2}} \end{bmatrix} \begin{bmatrix} \beta_{d2}(\mu) i_{dc2} + G_{d2}(\mu) v_{s2rms} \\ \beta_{q2}(\mu) i_{dc2} + G_{q2}(\mu) v_{s2rms} \end{bmatrix} \quad 4\text{–}20$$

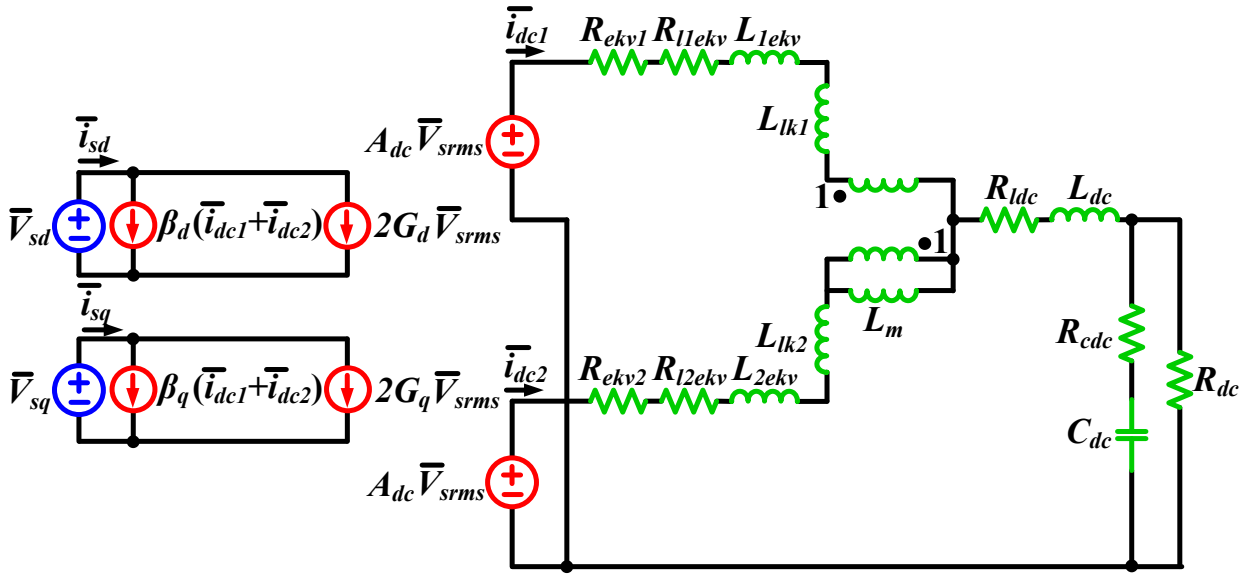


Figure 4-3: Circuit schematic of simplified AAVMs of twelve-pulse diode rectifier feeding a resistive load.

Obviously the described model is rather complicated as all the expressions, which describe six-pulse diode rectifier, are being doubled in order to describe accurately the twelve-pulse diode rectifier. However, in the case of balanced power flow, where equal power is delivered through each diode bridge, averaged model of the rectifier can be reduced to the simple schematic given in Figure 4-3.

Furthermore, the averaged model of twelve-pulse diode rectifier can be reduced to the averaged model of six-pulse diode rectifier model as shown in Figure 4-4. The parameters used in the simplified models are given below.

$$\begin{aligned} R_{ekv} &= R_{ekv1} \parallel R_{ekv2}; \\ L_{ekv} &= \left(L_{ekv1} + L_{lk1}\right) \parallel \left(L_{ekv2} + L_{lk2}\right) \end{aligned} \qquad 4\text{–}21$$

$$\begin{aligned} \beta_d(\mu) &= \beta_{d1}(\mu); \\ G_d(\mu) &= G_{d1}(\mu); \end{aligned} \qquad 4\text{–}22$$

4.2.2 Small-signal input dq admittance of AAVM

After linearization of small-signal model of AAVM, analytical expression of small-signal input dq admittance of twelve-pulse diode rectifier is derived and written below, where $Y_{dc}(s)$ is admittance seen at dc side.

$$\begin{bmatrix} Y_{dd}(s) & Y_{dq}(s) \\ Y_{qd}(s) & Y_{qq}(s) \end{bmatrix} = \begin{bmatrix} \sqrt{0.5}\left(\beta_d Y_{dc}(s) A_{dc} + 2G_d\right) & -\sqrt{0.5}\dfrac{I_q}{V_{srms}} \\ \sqrt{0.5}\left(\beta_q Y_{dc}(s) A_{dc} + 2G_q\right) & \sqrt{0.5}\dfrac{I_d}{V_{srms}} \end{bmatrix} \quad 4\text{–}23$$

$$Y_{dc}(s) = \left(R_{ekv} + R_{lekv} + sL_{ekv} + R_{ldc} + sL_{dc}\right) \| \left(\frac{1}{sC_{dc}} + R_{cdc}\right) \| R_{dc} \quad 4\text{–}24$$

In order to provide a more direct verification, rather intensive simulation study using switching simulation model is performed. The small-signal extraction is automated in MATLAB\Simulink software tool using the SimPowerSystems toolbox. The series voltage injection of magnitude equal to 2% of nominal voltage is injected into the twelve-pulse diode rectifier. The input current and voltage responses to the perturbation are simulated to reach the steady-state operating point, when the small-signal identification using FFT algorithm is applied on the steady state responses.

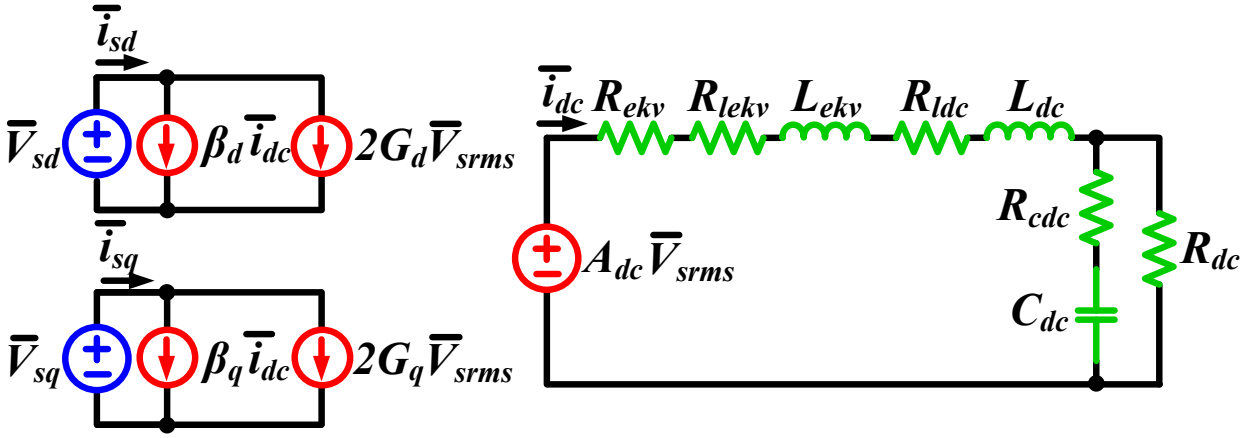
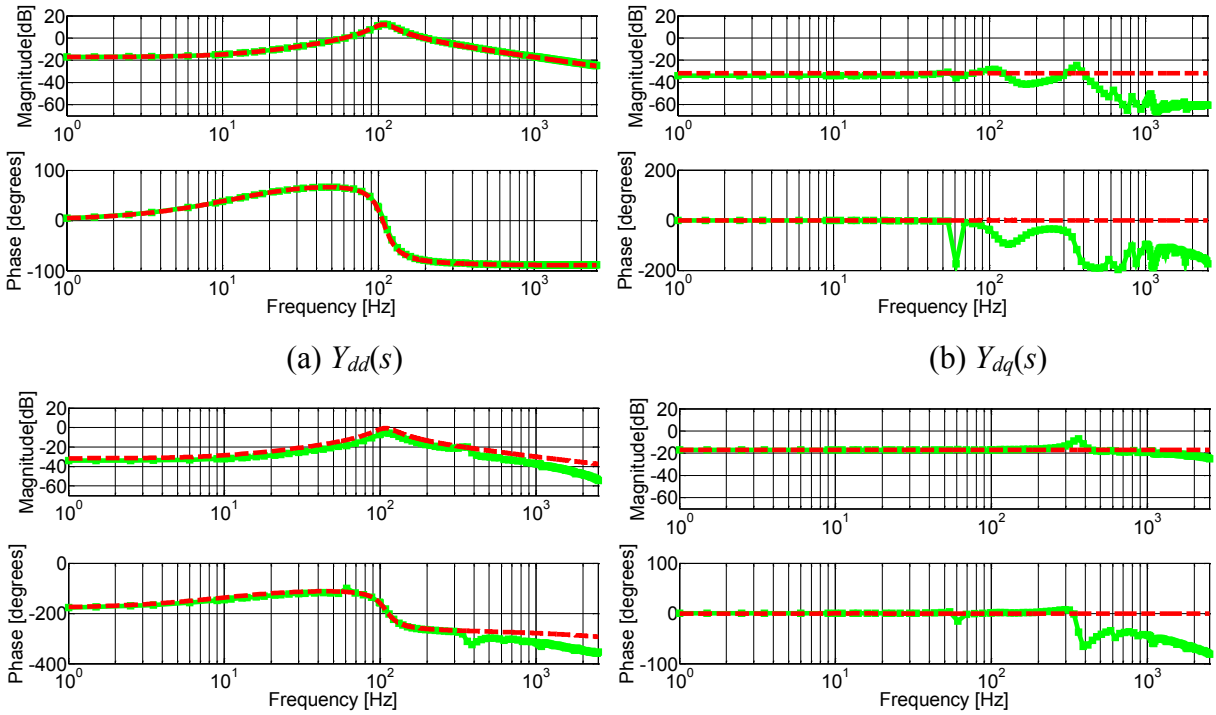


Figure 4-4: Circuit schematic of further simplified AAVMs of twelve-pulse diode rectifier feeding a resistive load.

In a similar manner averaged model is also built in the same software tool. The small-signal extraction is simply performed via the linearization of the model, as well defined DC operating point exists. As expected the analytical expressions matched with the small-signal results obtained via the linearization, verifying the described derivation. In this sense, either numerical results or analytical expressions could be used to describe small-signal input dq admittance of the averaged model.



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$

(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 4-5: Small-signal input dq admittance of twelve-pulse diode rectifier: obtained from switching simulation model (green line with squares), analytical expression of modified AAVM (red dashed line).

The comparison of input dq admittances, obtained from the switching simulation model and analytical expressions of AAVM are shown in Figure 4-5. Several conslusions can be drawn from the shown comparison. The first one is that AAVM predicts admittance $Y_{dd}(s)$ correctly in the whole measurement frqequency range, even beyond the switching frequency. Other three admittances have additional dynamics in the response that is not predicted by the averaged model. Additonal dynamics are especcially noticeable in admittances $Y_{dq}(s)$ and $Y_{qq}(s)$, as they represent response to the q-channel injection, which is more nonlinear. The additional resonant points show left and right around multiples of switching frequencies (720 Hz, 1440 Hz, 2160 Hz etc) and there are additional resonant points in the response at odd multiples of 360 Hz (360 Hz, 1080 Hz, 1800Hz etc). Such responses are typical for nonlinear systems, where injection at one frequency point yields several responses that are strongly coupled each to other. The described behavior is explained with the fact that q-channel injection modulates phase, thus it modulates commutation angle and yields significant sideband response around multiples of the switching frequency. Diode rectifiers are strongly nonlinear systems, hence such response is not suprising. Still to the best of

the author's knowledge sidebands admittances response as well as similar small-signal frequency domain analysis of twelve-pulse diode rectifiers have not been reported in the literature before.

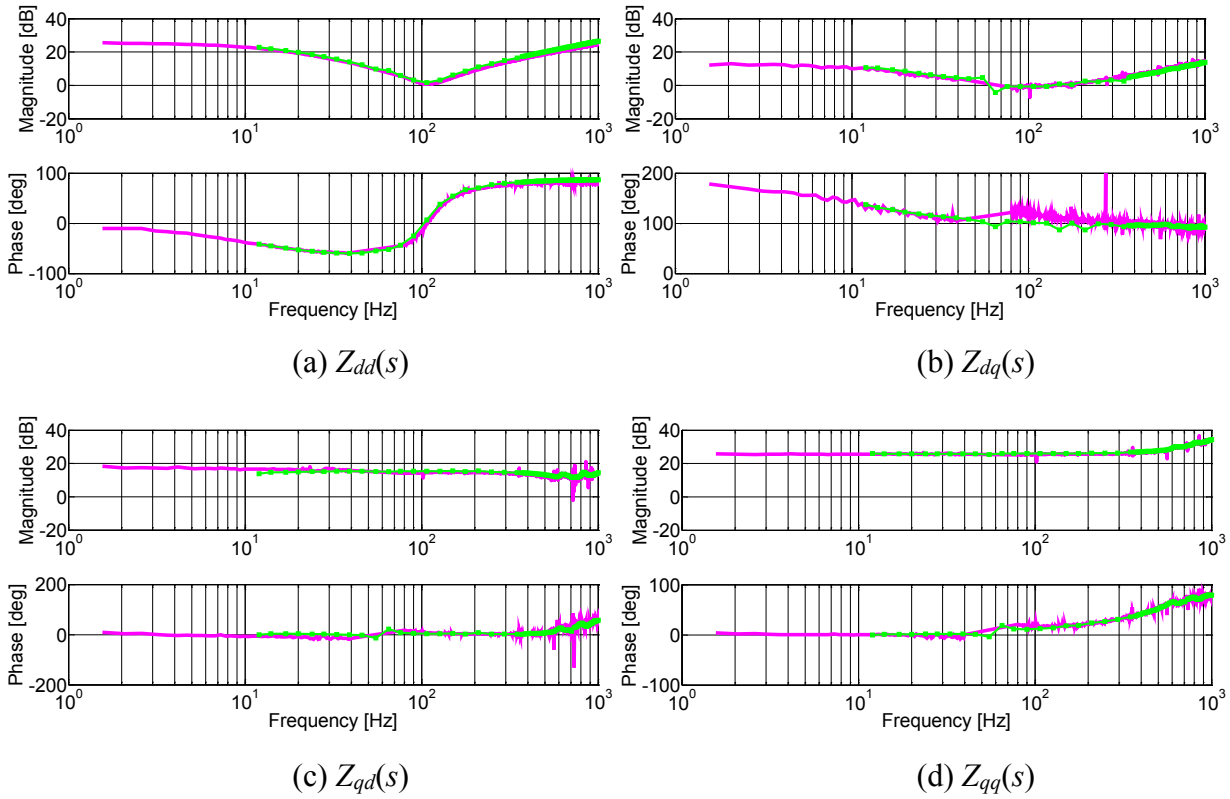
Furthermore, the prediction of other two admittances, $Y_{dq}(s)$ and $Y_{qq}(s)$, is accurate only up to one fourth and one half of the switching frequency, respectively. The presented frequency domain analysis reveals accuracy of the averaged model to be around one fourth of the switching frequency for responses to the nonlinear injection, while it provides extremely accurate prediction for responses to the linear injection.

If small-signal is injected on the DC side to provide a perturbation for a small-signal dc impedance characterization. The averaged model would match the switching model very accurately in the frequency range beyond the switching frequency. The explanation is that main coupling between dq side and dc side happens via the d-channel, which is the linear one as it mainly modulates the magnitude of the ac side voltages. Therefore the injected signal mainly perturbs d-channel and the generated response on the dc side behaves very linearly, yielding very accurate matching between averaged model and switching simulation model.

4.3 Experimental validation of nonlinear sideband effects

The described twelve-pulse diode rectifier is build and characterized with the impedance measurement unit (IMU). The details on IMU design and construction are explained in sufficient details in [99]. The switching simulation model is calibrated to match hardware set-up and the comparison of small-signal dq impedances of hardware set-up and switching simulation model is given in Figure 4-6. Excellent agreement between the obtained hardware measurements and switching simulation results is presented. In addition, the resonant points due to sideband effects around switching multiples are also almost perfectly matched. Obviously, the switching simulation model accurately captures behavior of the hardware set-up in the whole frequency range of interest, capturing sideband admittances.

Frequency-domain validity range of the averaged model is estimated, the discrepancy is contributed to the strong nonlinearity of twelve-pulse diode rectifier. Finally, it is shown that if the hardware set-up is modeled precisely, the switching simulation model can provide accurate small-signal input dq admittances in the entire frequency range of interest, capturing nonlinear sideband



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 4-6: Small-signal input dq impedance of twelve-pulse diode rectifier: obtained from switching simulation model (green line with squares), experimental measurements (purple line)

effects. Furthermore, the sideband admittances, which are the new effects, are characterized and explained.

4.4 Twelve-Pulse Diode Rectifier Feeding a Constant Power Load

The modeling of twelve-pulse diode rectifier feeding the constant power load (CPL) has been presented in this section. The circuit schematic of twelve-pulse diode rectifier feeding the actively controlled three-phase VSI is shown in Figure 4-7. The three-phase VSI is supplied by a twelve-pulse diode rectifier, while it regulates the voltage across the three-phase resistive load. Due to the voltage regulation via the inner current loop and outer voltage loops, the three-phase VSI behaves like a constant power load as seen by dc side of twelve-pulse diode rectifier. LC filter is on ac side of the inverter, filtering the switching harmonics and providing clean voltage for the resistive load.

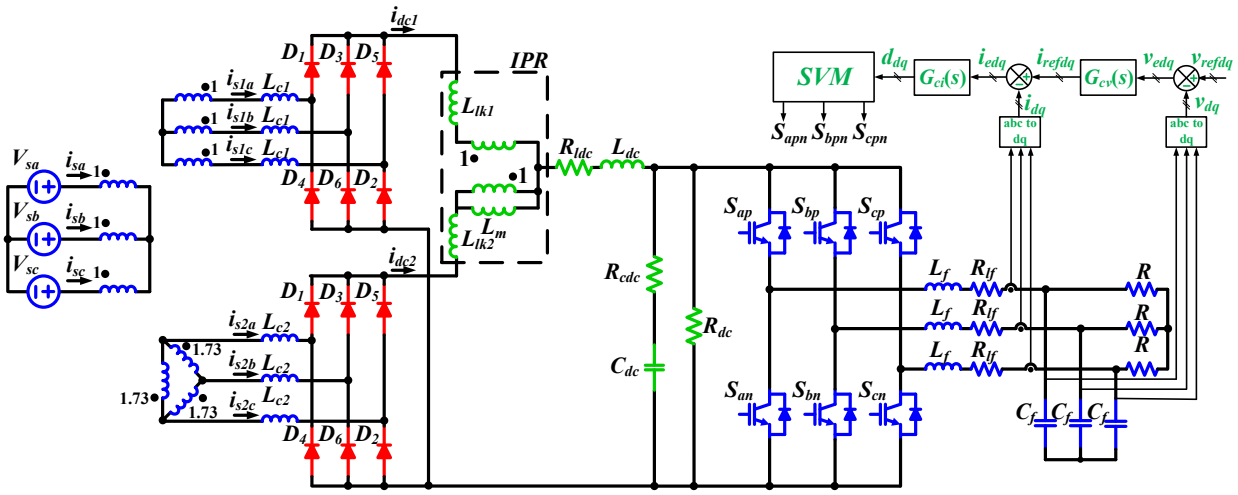


Figure 4-7: Twelve-pulse diode rectifier feeding an actively controlled three-phase VSI

Parameters of the components used in the described twelve-pulse diode rectifier test-case are given in Table 4-2. The outer voltage loop is designed to control the capacitor voltage in dq coordinates with 400 Hz bandwidth. The inner current loop regulates dq inductor currents with decoupling control, whose bandwidth is designed around 700 Hz.

Table 4-2 Parameters of twelve-pulse diode rectifier feeding actively controlled VSI

Source voltage	V_{sm}=120 V	DC inductance	L_{dc}=1.6 mH
Source frequency	f_s=60 Hz	Ser. resistance	R_{ldc}=60 mΩ
Leakage inductances of the inner phase tranformer	L_{lk1}=200 µH L_{lk2}=200 µH	Magnetizing inductance of the inner phase tranformer	L_m=830 µH
AC inductance	L_{c1}=220 µH L_{c2}=220 µH	DC capacitance	C_{dc}=1.05 mF
Series resistance	R_{lc1}=R_{lc2}=30 mΩ	Series resistance	R_{cdc}=30 mΩ
DC resistance	R_{dc}=250 Ω	Parasitic inductance of dc side resistor	L_{rdc}=10 µH
Inverter ac inductance	L_f=440 µH	Inverter ac capacitance	C_f=50 µF
Load resistance	R_{dc}=7 Ω	Output power	P_{out}=4375 W
Output dq current	I_{rd}=25 A I_{rq}=0 A	Output dq voltage	V_{rd}=175 V V_{rq}=0 V
VSI switching frequency	f_{sw}=20 kHz	ac frequency of inverter	f_{inv}=400 Hz

The schematic of averaged model of twelve-pulse diode rectifier feeding the three-phase inverter is shown in Figure 4-8. The twelve-pulse diode rectifier is modeled with the modified dq averaged model derived previously in this chapter. The three-phase inverter is modeled in dq coordinates with the classical dq averaged model.

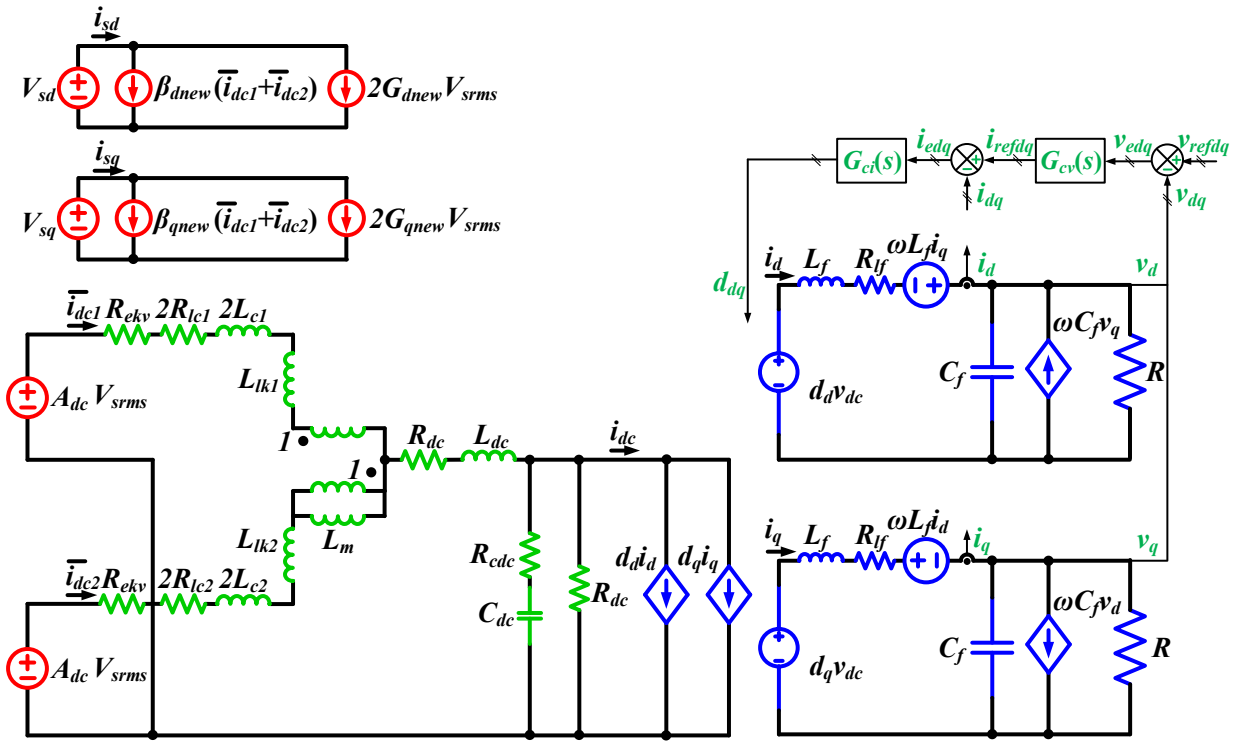
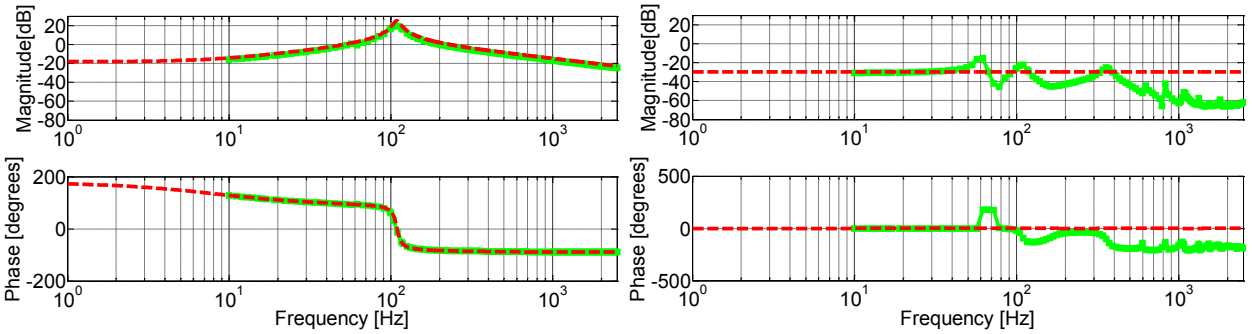


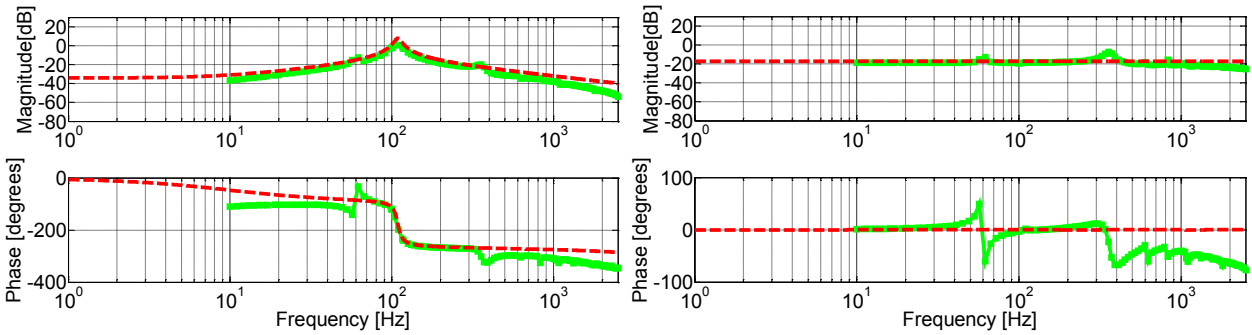
Figure 4-8: Reduced order AAVMs of twelve-pulse diode rectifier feeding an actively controlled three-phase VSI

The identification of small-signal input dq impedances of the switching simulation of the twelve-pulse diode rectifier test-case is obtained with FFT algorithm. The single-tone and multi-tone voltage perturbation signals from, whose magnitude is around 2% of nominal voltage, are injected and identification of small-signal transfer functions is performed on steady-state responses. The small-signal dq admittance of switching simulation model is characterized in 120 points between 10 Hz to 1 kHz as shown in Figure 4-9. In addition, the small-signal input dq admittance, which is obtained by the linearization of dq averaged model, is plotted and shown with dashed red line in Figure 4-9.

The comparison of small-signal dq admittances identified from the switching and averaged models show good matching in the whole frequency range. The identified admittance $Y_{dd}(s)$ has a resonant point around 108 Hz, which occurs due the resonance between dc inductance and dc capacitance. The averaged and switching model admittances $Y_{dd}(s)$ are matched in the full frequency range, even in the high frequency range beyond the diode rectifier switching frequency (720 Hz). Furthermore, the low frequency range of admittance $Y_{dd}(s)$ behave as a negative resistance due to the constant power load behavior of the three-phase inverter. The negative



(a) $Y_{dd}(s)$ (b) $Y_{dq}(s)$



(c) $Y_{qd}(s)$ (d) $Y_{qq}(s)$

Figure 4-9: Small-signal input dq admittance of twelve-pulse diode rectifier feeding a constant power load: switching simulation model (green line with squares), averaged model (dashed red line)

resistance is accurately captured by numerical extraction from the switching simulation model and via modified averaged modeling of diode rectifier. The admittance $Y_{qd}(s)$ has a same resonant point accurately predicted with both switching and averaged models. The matching between averaged and switching model admittance is up to 360 Hz. Due the coupling between d and q coordinates small sidebands around multiples of switching frequency shows up in magnitude characteristic. In addition, a multiple of resonant point excites third switching harmonic (1080 Hz) and shows up at 60 Hz. The low frequency phase characteristics of admittance $Y_{qd}(s)$ tends to zero because of active control of three-phase inverter.

The averaged model predicts the admittances $Y_{dq}(s)$ and $Y_{qq}(s)$ as resistor values in the whole frequency range. Due the interaction between resonance point and switching harmonics a sideband admittance occurs at 60 Hz. Resonance at 108 Hz as well as sideband admittances around multiples of switching harmonics are present in both small-signal admittances. The injection of voltage signal via q-channel modulates commutation angle of both diode bridges, yielding a strong

nonlinear responses. Thus, the sideband admittances are amplified and strongly present in the small-signal admittances.

The modified dq average model of twelve-pulse diode rectifier is general and accurately predicts the small-signal input dq admittance of rectifier with both passive and actively controlled constant power loads.

4.5 Summary

This chapter presented comprehensive comparison of input dq admittances for twelve –pulse diode rectifier feeding a resistive load, which are obtained from AAVM, switching simulation model and hardware set-up measurements. AAVM is modified to predict more accurately small-signal input dq admittance characteristics of twelve-pulse diode rectifier. AAVM is further reduced to equivalent circuit model of six-pulse diode rectifier, providing very simple averaged model solution. Furthermore, analytical expressions of the input dq admittance of modified AAVM are derived, revealing the analytical connection between dq side admittance and dc side admittance and showing inherent impedance mapping property.

Frequency-domain validity range of the averaged model is estimated, where the discrepancies are contributed to the strong nonlinearity behavior of twelve-pulse diode rectifier. Finally, it is shown that if the hardware set-up is modeled precisely, the switching simulation model can provide accurate small-signal input dq admittances in the entire frequency range of interest, capturing very precisely nonlinear sideband effects. This chapter shows the new effect, sideband admittances around multiples of switching frequency, which was not observed previously in the twelve-pulse diode rectifiers. The new phenomenon is captured both in hardware measurements and in switching simulation model using the developed small-signal extraction technique.

Chapter 5. Multi-Level Single-Phase Shunt Current Injection Converter used in Small-Signal dq Impedance Identification

This chapter describes a detailed design procedure of a single-phase multi-level single-phase shunt current injection converter based on cascaded H-bridge topology. The shunt current injection converter can inject an arbitrary current perturbation at three-phase power system interfaces, in order to identify small-signal dq impedances. Special attention is given toward the selection of inductors and capacitors, trying to optimize the selected component values. The proposed control is extensively treated and inner current and outer voltage loops are completely analyzed. Furthermore, voltage balancing is included into the control to assure dc voltage control for each H-bridge module. Analytical expressions, which describe the design procedure, are derived and verified to be accurate. The designed converter is simulated using detailed switching simulation model and excellent agreement between theory and simulation results are obtained. The proposed multi-level single-phase converter is a natural solution for single-phase shunt current injection with the following properties: modular design, capacitor energy distribution, reactive element minimization, higher equivalent switching frequency, capability to inject higher frequency signals, suitable to perturb higher voltage power systems and capable of generating cleaner injection signals.

5.1 Introduction

Modern power systems commonly used in aircraft, ship, automotive and grid vehicles, as well as synchronous generator and wind power generator micro-grid systems have three-phase ac interface feeding different electronic power loads. Various types of the electronic loads in such systems exhibit negative resistance small-signal impedance behavior due to the wide usage of constant power control. In many such power systems, the small-signal stability becomes an important issue, which needs to be addressed by the system integrators, in order to ensure stable and reliable operation of the system. Although, there are numerous approaches to investigate and estimate stability of those systems, the most commonly used approach is determination of the

stability through the input/output ratio of small-signal impedances at the injection interface. Generally, in the case of three-phase AC power systems, the stability analysis can be performed at AC three-phase interface via the measurements of small-signal impedances in the rotating reference frame, for example using dq transformation. The magnitude invariant dq transformation, which is commonly used in the impedance identification process, is defined below. The chapter is organized in the following manner, the second section describes design of the proposed single-phase multi-level cascaded H-bridge converter. Third section validates the design of shunt current injection converter with the time-domain simulations of the equivalent model in MATLAB/Simulink environment. Furthermore, SimPowerSystem toolbox is used as it provides piece wise-linear models (PWLM) for switching power electronic devices, enabling a fast and precise solver, with sufficient precision. Finally, the fourth section gives summary, conclusions and future work.

The main scope of this chapter is a design procedure of multi-level single-phase cascaded H-bridge injection converter, which generates perturbation current for dq impedance identification. Multi-level topology offers several advantages, that are especially important for the shunt current injection application: the possibility to perform impedance identification of higher voltage power systems, generation of cleaner current injection signal, modularity of the design, distribution of the energy storage among module capacitors, usage of smaller inductor and capacitor components, usage of low voltage high switching frequency modules, identification of the impedances in higher frequency range, etc...

This chapter is organized in the following manner, the second section describes the design procedure for the proposed single-phase multi-level cascaded H-bridge converter, including operating point principles, component value selection and PLL implementation. Third section focuses on modeling plant transfer functions using dynamic average value modeling and controller design. Fourth section validates the design of shunt current injection converter, with the time-domain simulations of the equivalent converter model in MATLAB/Simulink using SimPowerSystem toolbox. Furthermore, the fifth section presents experimental verification of the proposed design via the presented experimental results and its comparison to the developed switching simulation model waveforms. In the end, the sixth section gives summary, conclusions and future work.

5.2 Design of multi-level single-phase cascaded H-bridge converter

This section describes the design procedure of a multi-level single-phase cascaded H-bridge converter. The main focus of the section on selecting the appropriate modulation technique, value of AC inductance, value of DC capacitance, implementation of synchronous reference frame phase locked loop (SRF-PLL), and design of several different controllers used to regulate the injected current. In this way, the multi-level cascaded H-bridge converter is optimized to perform current injection into ac power system.

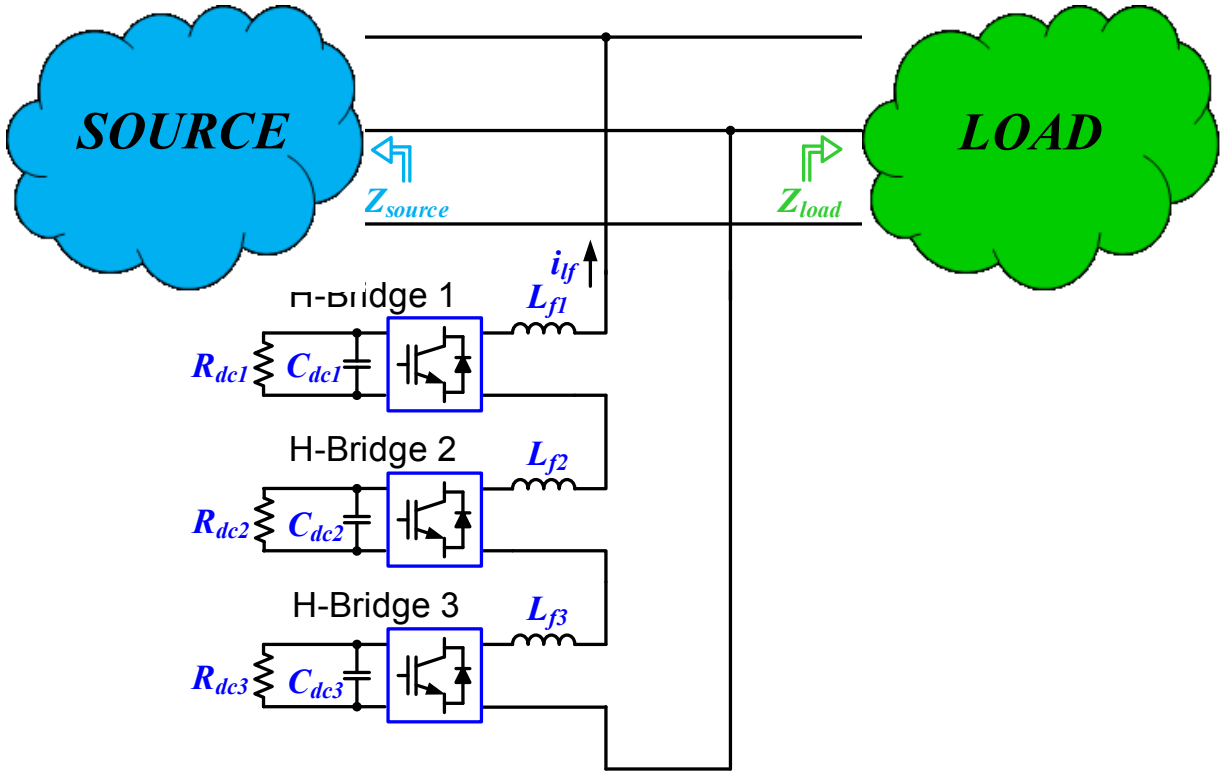


Figure 5-1: Multi-level single-phase shunt current injection converter based on cascaded H-bridge topology

The proposed single-phase multi-level cascaded H-bridge converter, which operates in rectifier mode, is shown in Figure 5-1. The proposed solution consists of three H-bridge modules connected in series. AC inductance is used to filter switching voltage and create a clean current that is injected into the grid. On dc side, there are also three capacitors to store reactive energy used for perturbation and keep dc voltage at desired level, ensuring stable operating point conditions. Multi-level converter offers several benefits: dc voltage is distributed among modules, thus the voltage

stress on each module is lower, which enables the usage of faster switches; equivalent switching frequency seen by AC inductances is three times higher, thus the generated current will have cleaner waveform, each module is switching at same frequency thus the switching losses are minimized, although very clean current waveform is generated; smaller current ripple in the inductor current will cause smaller core losses.

The parameters of the power system, for which a shunt current injection converter is designed, are shown in Table 5-1. Three-phase power systems up to 250kW can be perturbed via the proposed shunt current injection converter. Nominal value of line to line RMS voltage is 480V, but the converter will operate properly even if nominal RMS value is changed by several percent.

Table 5-1 Three-phase power system specifications

System parameter	***Value***	***Base parameter***	***Value***
Power rating	250 kW	Base resistance:	0.92 Ω
Line to line rms voltage	480 V	Base inductance:	2.4 mH
Phase current rms	300A	Base capacitance	2.9 mF
System frequency	60 Hz		

The parameters of converter and component values obtained by the design procedure are given in Table 5-2.

Table 5-2 Single-phase injection converter parameters

System parameter	***Value***	***Base parameter***	***Value***
DC voltage	400 V	Inductance	0.66 mH
Switching frequncy:	10 kHz	Capacitance	3.2 mF
Equivalent switching freqeucny	60 kHz	DC resistance	1 k Ω
Injection frequency range:	10 Hz-1 kHz	Number of modules	3
Injection rms current values	3A-30A	Peak dc voltage	460 V

5.2.1 Modulation technique

The modulation of multi-level cascaded H-bridge converter can be realized via several different techniques, where the most popular are pulse-width modulation (PWM), pulse frequency modulation (PFM), delta modulation etc. In the design of the converter, two PWM techniques are considered, unipolar and bipolar. Unipolar and bipolar PWM techniques for arbitrary simulation waveform are shown in Figure 5-2. As shown in the harmonic plot, unipolar PWM produces lower switching harmonics, while bipolar PWM produces harmonic content at twice the switching

frequency. The advantage of bipolar PWM is that it effectively doubles switching frequency of the bridge [103]. A direct consequence is that the generated current will contain smaller number of switching harmonics. In a sense, the inductor current will be less contaminated with unwanted switching harmonics.

$$v_{absw} = 2V_{dc}M\cos(\omega_s t) + \frac{4V_{dc}M}{\pi}\sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty}\frac{1}{m}J_n(m\pi M)\sin\left(\frac{n\pi}{2}\right)\cos(m\omega_c t + n\omega_s t) \qquad 5\text{–}1$$

$$v_{absw} = 2V_{dc}M\cos(\omega_s t) + \frac{8V_{dc}M}{\pi}\sum_{m=1}^{+\infty}\sum_{n=-\infty}^{+\infty}\frac{1}{2m}J_{2n-1}(m\pi M)\cos([m+n-1]\pi)\cos(2m\omega_c t + [2n-1]\omega_s t) \qquad 5\text{–}2$$

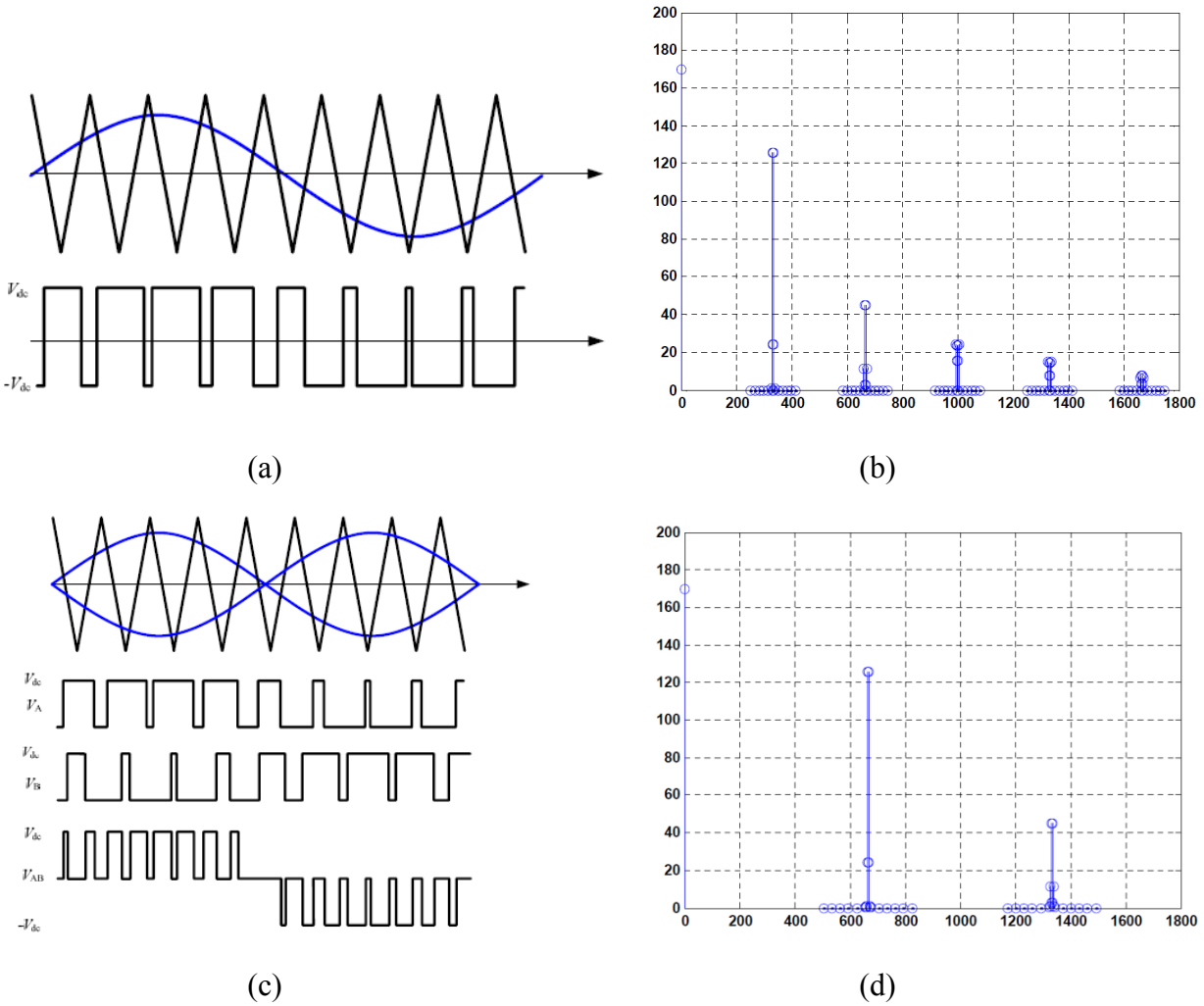


Figure 5-2: Unipolar PWM technique (a) time-domain waveforms (b) frequency-domain content, and bipolar PWM technique (c) time-domain waveforms (d) frequency-domain

However, bipolar PWM technique will increase the switching losses of H-bridge, but the efficiency of the converter is not a critical design constrain. Therefore, a bipolar PWM technique is suitable solution for H-bridge control and modulation. Furthermore, bipolar PWM is implemented in all the simulation models used throughout the paper. The harmonics content of both unipolar and bipolar PWM techniques can be analytically treated via double Fourier analysis. Analytical expression for harmonic content of the switching voltage, assuming there is no significant ripple on dc capacitors, are given with 5-1 and 5-2.

5.2.2 Operating point calculation

The operation of the multi-level cascaded H-bridge converter is determined via control of the applied duty-cycles for each H-bridge cell. The duty cycle consists of two components, system component at line frequency, which controls power transfer and injection component at the specified injection frequency, which generates desired perturbation current. Due to the switching behavior of the converter, additional switching harmonic components would exist in the duty cycle, but with the proper design its influence can be minimized. The first harmonic component, the one at line frequency, is responsible for maintaining dc voltage equal to the specified reference value. Active power drawn from the grid only covers the power losses in the bridge, resulting in small current drawn at line frequency. Analytically, line frequency component of duty-cycle is described with the following expression.

$$NV_{dc}d_{sys}(t) = L_f \frac{di_{lfsys}(t)}{dt} + v_{sab}(t) \qquad 5\text{–}3$$

Assuming small active power consumption of converter, which is reasonable assumption as converter exchanges reactive power with the system, then inductor voltage drop can be neglected. In this way, simple analytical duty-cycle expression is obtained, having enough precision to describe operation of the converter.

$$d_{sys}(t) = \frac{v_{sab}(t)}{NV_{dc}} = \frac{V_{sllm}}{NV_{dc}} \sin\left(\omega_{sys}t + \theta_{syso}\right) \qquad 5\text{–}4$$

The primary purpose of the converter is to generate a perturbation current that would ideally replicate desired signal. In that sense, injection component of duty cycle d_{inj}(t) would be responsible to generate injection current. Equation which describe relationship between injection duty cycle and injection current is as

$$d_{inj}(t)NV_{dc} = R_{lf} i_{lfinj}(t) + L_f \frac{di_{lfinj}(t)}{dt} \quad 5\text{–}5$$

$$d_{inj}(t) = \frac{R_{lf} i_{lfinj}(t) + L_f \dfrac{di_{lfinj}(t)}{dt}}{NV_{dc}} \quad 5\text{–}6$$

If the desired current is of sinusoidal form with frequency different than harmonic frequencies present in the grid (multiples of system frequency), meaning that the desired perturbation current is solely generated by the converter. Following this reasoning, the analytical expression of duty-cycle component corresponding to the injection frequency is derived below.

$$i_{lfinj}(t) = I_{lfm} \sin\left(\omega_{inj} t + \psi_{injo}\right), \omega_{inj} \neq k\omega_{sys}, k = 1, 2, \ldots \quad 5\text{–}7$$

$$d_{inj}(t) = \frac{1}{NV_{dc}} \left(R_{lf} I_{lfm} \sin\left(\omega_{inj} t + \psi_{injo}\right) + L_f \omega_{inj} I_{lfm} \cos\left(\omega_{inj} t + \psi_{injo}\right)\right) \quad 5\text{–}8$$

$$d_{inj}(t) = \frac{I_{lfm}\sqrt{\left(R_{lf}\right)^2 + \left(L_f \omega_{inj}\right)^2}}{NV_{dc}} \sin\left(\omega_{inj} t + \psi_{injo} + \psi\right), \ \psi = \arctan\left(\frac{L_f \omega_{inj}}{R_{lf}}\right) \quad 5\text{–}9$$

In the case that chirp signal with linear frequency progression is selected for the injection, the general analytical expression of desired chirp signal is as follow

$$i_{lfinj}(t) = I_{lfm} \sin\left(\theta(t)\right), t = [0, T) \quad 5\text{–}10$$

$$i_{lfinj}(t) = I_{lfm} \sin\left(2\pi\left(f_0 t + \frac{f_1 - f_0}{2T} t^2\right) + \theta_o\right), t = [0, T) \quad 5\text{–}11$$

Frequency increases linearly from f_0 to f_1 for a specified time T. Variable T represents the duration of the chirp signal, and after that time the chirp signal can be repeated, resulting in periodical injection signal, providing fair comparison with sinusoidal and multi-tone signals, which are periodical signals by definitions.

$$d_{inj}(t) = \frac{1}{NV_{dc}} \left(R_{lf} I_{lfm} \sin\left(\theta(t)\right) + L_f \frac{d\theta(t)}{dt} I_{lfm} \cos\left(\theta(t)\right)\right), t = [0, T) \quad 5\text{–}12$$

$$d_{inj}(t) = \frac{I_{lfm}\sqrt{R_{lf}^2 + \left(L_f \dfrac{d\theta(t)}{dt}\right)^2}}{NV_{dc}} \sin\left(\theta(t) + \psi\right), \ \psi = \arctan\left(\frac{L_f \dfrac{d\theta(t)}{dt}}{R_{lf}}\right) \quad 5\text{–}13$$

Maximum frequency of chirp signal does not exceed maximum frequency of sinusoidal injection signal, implying that maximum injection value of injection duty cycle $d_{inj}(t)$ will remain

same as for sinusoidal injection case. It means that the analysis of the injection duty cycle $d_{inj}(t)$ can be performed for sinusoidal case, implying that same conclusions will hold for chirp injection signal.

Using same reasoning, similar kind of analysis can be performed for a multi-tone signal. The ideal multi-tone signal used as injection current is defined as

$$i_{lfinj}(t) = I_{lfm}\sum_{i=1}^{N}\sin\left(\omega_{inji}t + \psi_{inji} + \psi_o\right) \qquad 5\text{–}14$$

Injection duty cycle, which is responsible for a generation of multi-tone signal is

$$d_{inj}(t) = R_{lf}I_{lfm}\sum_{i=1}^{N}\sin\left(\omega_{inji}t + \psi_{inji} + \psi_o\right) + L_f I_{lfm}\sum_{i=1}^{N}\omega_{inji}\cos\left(\omega_{inji}t + \psi_{inji} + \psi_o\right) \qquad 5\text{–}15$$

$$d_{inj}(t) = I_{lfm}\sum_{i=1}^{N}\sqrt{R_{lf}^2 + \left(L_f\omega_{inji}\right)^2}\,\sin\left(\omega_{inji}t + \psi_{inji} + \psi_i + \psi_o\right),\ \psi_i = \arctan\left(\frac{L_f\omega_{inji}}{R_{lf}}\right) \qquad 5\text{–}16$$

Injection duty cycle can be bounded using following expression

$$\begin{aligned} &d_{inj}(t) < I_{lfm}N\sqrt{R_{lf}^2 + \left(L_f\omega_{injk}\right)^2}\,\sin\left(\omega_{injk}t + \psi_{injk} + \psi_k + \psi_o\right), \\ &\psi_k = \arctan\left(\frac{L_f\omega_{injk}}{R_{lf}}\right), \omega_{injk} = \max\left(\omega_{inji}\right), i = 1,\ldots,N \end{aligned} \qquad 5\text{–}17$$

Equivalent magnitude is equal to magnitudes of tones multiplied with a number of tones N, providing a magnitude constrain. Therefore, for the analysis of the injection duty cycle limitation it is enough to focus on sinusoidal injection and then generalize it to chirp and multi-tone, while keeping magnitude constrained for a multi-tone signal.

The first constraint used in design procedure states that total duty cycle cannot exceed value of one, meaning that pulse width cannot be larger than the switching period. In order to keep some margin duty cycle should not exceed constant *k*, resulting in the following inequality.

$$\left|d(t)\right| = \left|d_{sys}(t) + d_{inj}(t)\right| < k, k = 0.95 \qquad 5\text{–}18$$

5.2.3 Design of AC inductance

The purpose of the inductor is to act as a low-pass filter, which attenuates switching harmonics present in the switching voltage generated by H-bridges. The used inductor filter behaves as a first order low-pass filter with attenuation of 20db/decade.

$$i_{lf}(s) = \frac{1}{sL_f} v_{absw}(s) \tag{5–19}$$

In order to provide very clean current, it is desired to use large inductance value. However, large inductance value would yield large voltage drop during high frequency injection, causing the converter to operate in overmodulation region, which would result in losing controllability. Previously derived inequality for duty cycle should be satisfied for all operating conditions, which would result in an inequality that limits maximum allowable inductance value.

$$\left|d_{sys}(t)\right| + \left|d_{inj}(t)\right| < k \tag{5–20}$$

$$\left|\frac{V_{sllm}}{NV_{dc}}\sin\left(\omega_{sys}t + \theta_{syso}\right)\right| + \left|\frac{L_f\omega_{inj}I_{lfm}}{NV_{dc}}\cos\left(\omega_{inj}t + \psi_{injo}\right)\right| < \frac{V_{sllm}}{NV_{dc}} + \frac{L_f\omega_{inj}I_{lfm}}{NV_{dc}} < k \tag{5–21}$$

If the following inequality is satisfied, which is derived for a sinusoidal injection, then converter will stay away from overmodulation region.

$$L_f < \frac{kNV_{dc} - V_{sllm}}{\omega_{inj}\max\left(I_{lfm}\right)} \tag{5–22}$$

$$L_f < 2\,mH \tag{5–23}$$

The second inductor value inequality can be determined by imposing constrain on the maximum allowed current ripple value, limiting amount of switching noise in the generated current. Starting from equation for inductor current and approximating a source voltage $v_{sab}(t)$ with dNV_{dc}, the inductor current equation becomes:

$$L_f \frac{di_{lf}}{dt} = Nv_{dc} - v_{sab} \tag{5–24}$$

$$L_f \frac{\Delta i_{lf}}{d\frac{T_{sw}}{2N}} = v_{dc} - dv_{dc} \tag{5–25}$$

Inductor current change during the first switching subinterval is obtained by rearranging previous equation.

$$\Delta i_{lf} = \frac{d(1-d)v_{dc}}{2L_f N f_{sw}} \qquad 5\text{–}26$$

Maximum current increase occurs when duty cycle is equal to 0.5, resulting in the following expression for the maximum current change. By imposing constrain on maximum allowed current change lower bound limit for inductance is obtained. In this way, unwanted switching current noise, which is generated by switching H-bridge converters, is limited.

$$\max\left(\Delta i_{lf}\right) = \Delta i_{lf}\left(d = 0.5\right) = \frac{v_{dc}}{8L_f N f_{sw}} \qquad 5\text{–}27$$

By rearranging the previous equation, the second inductor value inequality can be rewritten.

$$L_f > \frac{v_{dc}}{8N f_{sw} \max\left(\Delta i_{lf}\right)} = 0.278mH \qquad 5\text{–}28$$

Inductor value is selected to be 2 mH as it satisfies both inductor inequalities derived in this section. In this way it is ensured that converter will stay away from overmodulation region and maximum ripple current within a switching cycle will be bounded.

5.2.4 Design of DC capacitance

The main purpose of dc capacitors is to maintain desired dc voltage, enabling proper dc operation point for the converter and to store reactive energy during low frequency injection. The proposed converter needs to be designed for a low frequency injection in sub line harmonic range, yielding a design with bulky capacitors compared to active power filter and statcom application. The dc capacitor is designed with respect to the maximum allowed voltage ripple for the lowest injection frequency point. The H-bridge modulates the switching voltage, but it also determines the current flowing through the dc capacitor via the following equation.

$$i_{cdc}(t) = -d(t) i_{lf}(t) \qquad 5\text{–}29$$

The dc capacitor current is obtained by using previously derived expressions for duty-cycle and inductor current.

$$C_{dc}\frac{dv_{cdc}(t)}{dt} = -\left(d_{inj}(t) + d_{sys}(t)\right)\left(i_{lfinj}(t) + i_{lfsys}(t)\right) \qquad 5\text{–}30$$

By expanding a product of duty-cycle and inductor current, dc capacitor current turns out to be a sum of four product terms. After, integrating capacitor current expression, capacitor voltage is determined via expression written below.

$$v_{cdc}(t) = -\frac{1}{C_{dc}}\int d_{inj}(t) i_{lfinj}(t)dt - \frac{1}{C_{dc}}\int d_{inj}(t) i_{lfsys}(t)dt - \frac{1}{C_{dc}}\int d_{sys}(t) i_{lfinj}(t)dt - \frac{1}{C_{dc}}\int d_{sys}(t) i_{lfsys}(t)dt \quad 5\text{–}31$$

In a typical converter operation mode, current $i_{lsys}(t)$ is much smaller than $i_{lfinj}(t)$, so the dc capacitor current can be simplified to a nices expression.

$$v_{cdc}(t) = -\frac{1}{C_{dc}}\int d_{inj}(t) i_{lfinj}(t)dt - \frac{1}{C_{dc}}\int d_{sys}(t) i_{lfinj}(t)dt \quad 5\text{–}32$$

The biggest voltage ripple happens for low frequency injection current. In that case $d_{sys}(t)$ is much bigger than $d_{inj}(t)$, so the dc capacitor becomes.

$$\Delta v_{cdc}(t) = -\frac{1}{C_{dc}}\int \frac{V_{sllm}}{NV_{dc}}\sin(\omega_{sys}t) I_m \sin(\omega_{inj}t + \varphi_{inj})dt \quad 5\text{–}33$$

After several algebraic manipulations, the voltage ripple present on dc capacitor is calculated via the following expression.

$$\Delta v_{cdc\max} = \frac{V_{sllm} I_{lm\max}}{2NV_{dc}C_{dc}2\pi(f_{sys} - f_{inj})} < kV_{dc} \quad 5\text{–}34$$

Finally, a capacitor value inequality is obtained by rearranging the previously obtained expression.

$$C_{dc} > \frac{V_{sllm} I_{lm\max}}{4NkV_{dc}^2\pi(f_{sys} - f_{inj})} \quad 5\text{–}35$$

If maximum allowed voltage ripple is set to be 15% (k=0.15, kVdc=60 V) of nominal dc voltage, then the capacitor value inequality becomes.

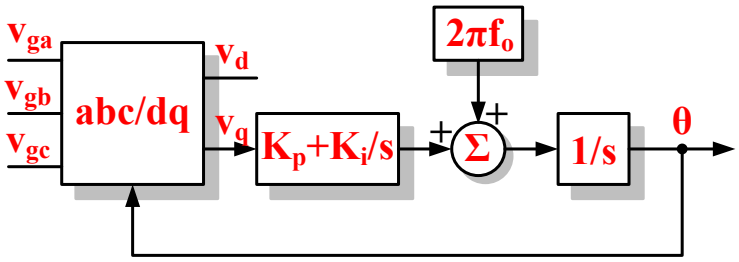
$$\begin{aligned} C_{dc} &> 320mF; \Delta f = f_{sys} - f_{inj} = 0.1Hz \\ C_{dc} &> 32mF; \Delta f = f_{sys} - f_{inj} = 1Hz \\ C_{dc} &> 3.2mF; \Delta f = f_{sys} - f_{inj} = 10Hz \end{aligned} \quad 5\text{–}36$$

In the design specifications, it is stated that frequency difference should go as low as1 Hz, so the capacitor is selected to be 32 mF. In this case, we will allow voltage ripple to be 15% of nominal capacitor voltage. Furthermore, if maximum current that can be injected in the low frequency is lowered to half, the selected capacitor value will satisfy capacitor inequality in the lower frequency range also. The last constrain is that the cut-off frequency of the low-pass filter, which is formed between ac inductor and dc capacitors, should be several times below the switching frequency.

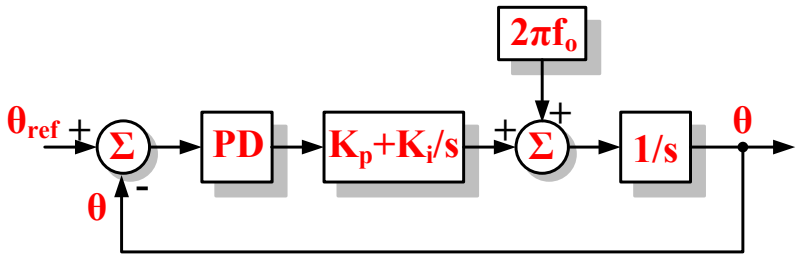
$$f_{cutoff} = \frac{1}{2\pi\sqrt{L_f \frac{C_{dc}}{N}}} < 0.1 f_{sw} \qquad 5\text{–}37$$

5.2.5 Phase-locked loop (PLL)

In order to generate desired current signal it is necessary to sense frequency and phase of the voltage at injection point. One possible solution is to implement a synchronous reference frame PLL (SRF PLL) with center frequency. It consists of phase detector low-pass filter and integrator, providing phase at the output. The dq transformation coefficient is selected to be 2/3, so that gain of the phase detector (PD) is equal to the voltage magnitude V_m.



(a)



(b)

Figure 5-3: Block diagrams of the realized SRF PLL block (a) Equivalent shematic (b) Equivalent small-signal linearized model

$$T = \frac{2}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin(\theta) & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \qquad 5\text{–}38$$

Figure 5-3 shows schematic and linearized model of SRF PLL. The derivation of linearized model for SRF PLL and analysis of different PLLs is shown in previous chapters. Equation, which describes PLL loop gain, is derived from the equivalent linearized model.

$$T_{PLL} = V_m \frac{1}{s}\left(K_p + \frac{K_i}{s}\right) \qquad 5\text{–}39$$

5.3 Dynamic average value modeling and design of digital control

The purpose of the control part is to regulate injected current, while maintaining capacitor voltages of H-bridge voltages to be equal to desired dc values. Furthermore, the control needs to compensate any mismatch between modules by regulating dc side voltage of each module separately, providing effective voltage balancing control. There are different control schemes for multi-level cascaded H-bridge rectifiers, which include voltage balancing control among modules [122], [123]. The complete block diagram of the proposed digital control is shown in Figure 5-4. The outer voltage loop regulates the averaged value of H-bridge module voltages to be equal to the referenced dc value. The inner current loop reference is obtained by multiplying output of voltage compensator with sinusoidal signal obtained from the output of PLL. The purpose of this part of the loop is to keep the dc voltage of modules equal to voltage reference by providing small amount of power from the voltage source, compensating the power losses of the multi-level current injection converter. The desired injection current waveform added on top of the already obtained current reference, thus the current controller will generate both the current that will regulate the capacitor voltages and injection current.

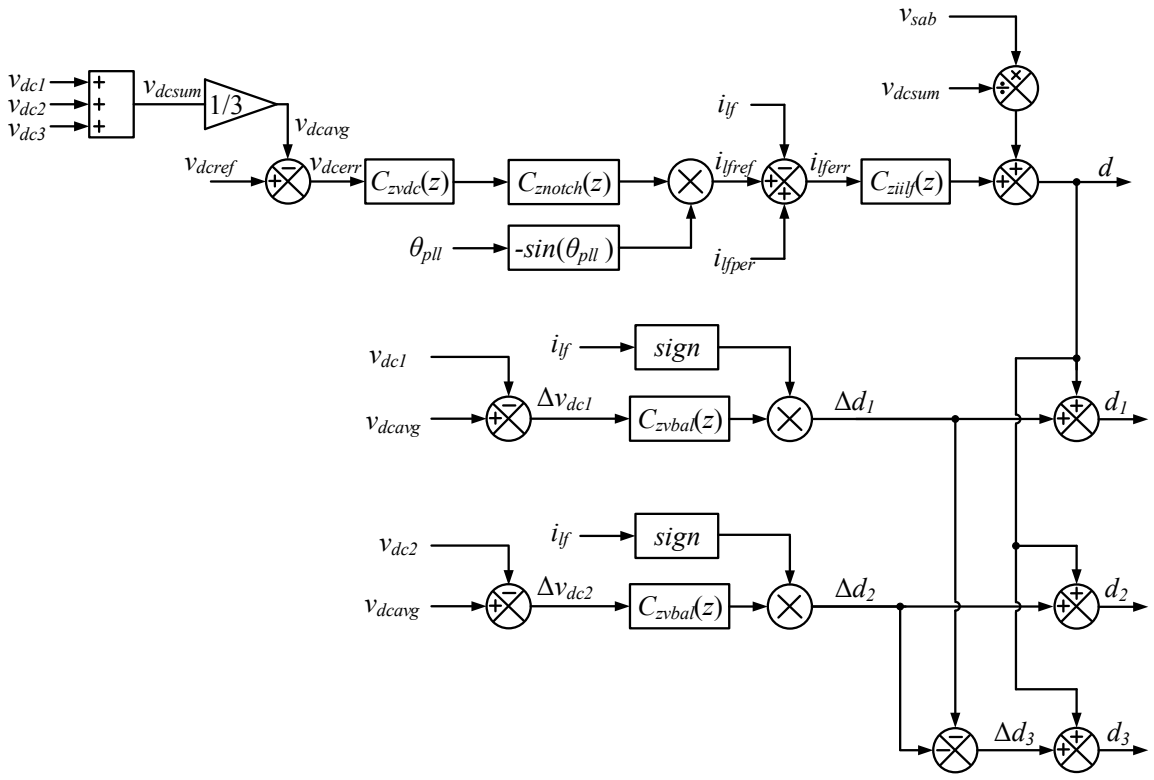


Figure 5-4: Block diagram of digital controller including high bandwidth current control, dc voltage regulation and voltage balancing among modules

The bottom part of control block diagram provides voltage balancing among modules. Without this part the mean value of capacitor voltages is regulated to be equal to desired dc value (400 V), while there might be difference among voltages due to any kind of mismatch among modules. By applying the proposed control, each capacitor voltage is tightly regulated to the desired dc voltages value. The voltage balancing controller and outer voltage control should have much slower dynamic, below 0.1 Hz. On the other hand, the inner current controller is designed to have 3 kHz bandwidth. In this way, the controller ensures the generation of current with the high tracking in the frequency range of interest, 10 Hz-1 kHz.

Design of several different control loops is explained and analyzed in depth in this section. Dynamic average value modeling approach is adopted for the modeling and small-signal analysis of the proposed converter [124], [125]. Figure 5-5 shows equivalent switching model of the converter, while Figure 5-7 shows equivalent averaged model of the multi-level shunt current injection converter.

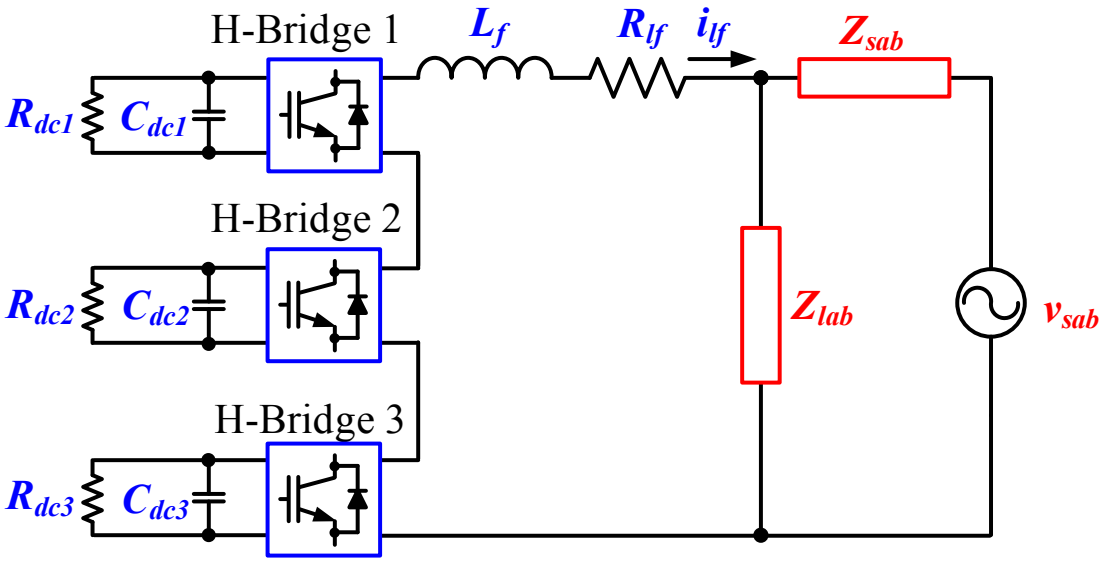


Figure 5-5: Equivalent switching model multi-level cascaded H-bridge circuit

The model is reduced to single-phase system supplied with line to line voltage, including source and load impedances. In order to model converter more precisely, reduced order modeling approach is used in this paper. The reduced order modeling reduces multi-level cascaded H-bridge topology, reduces to a single H-bridge model, which is shown in Figure 5-7 (a). The equivalent averaged model of converter, obtained with reduced order modeling is shown in Figure 5-7 (b).

5.3.1 State-space modeling of cascaded H-bridge converter

Using reduced order average model it is possible to design all the loops in the proposed digital controller. Applying a quasi-stationary linearization approach, small-signal models are derived and used to design loop bandwidths and margins. Equations, which describe operation of the reduced order model of the converter, are obtained by applying Kirchhoff's laws on the given circuit as

$$\begin{aligned} C_{dc}\frac{dv_{dc}(t)}{dt}+\frac{v_{dc}(t)}{R_{dc}} &= -d(\theta(t))i_{lf}(t) \\ Nd(\theta(t))v_{dc}(t) &= R_{lf}i_{lf}(t)+L_f\frac{di_{lf}(t)}{dt}+v_{sab}(\theta(t)) \end{aligned} \qquad 5\text{–}40$$

Directly from previous equation, average model state-space equation is as follow

$$\begin{bmatrix} \frac{dv_{dc}}{dt} \\ \frac{di_{lf}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_{dc}R_{dc}} & \frac{-d(\theta)}{C_{dc}} \\ \frac{Nd(\theta)}{L_f} & \frac{-R_{lf}}{L_f} \end{bmatrix} \begin{bmatrix} v_{dc} \\ i_{lf} \end{bmatrix} + \begin{bmatrix} 0 \\ -\frac{1}{L_f} \end{bmatrix} v_{sab} \qquad 5\text{–}41$$

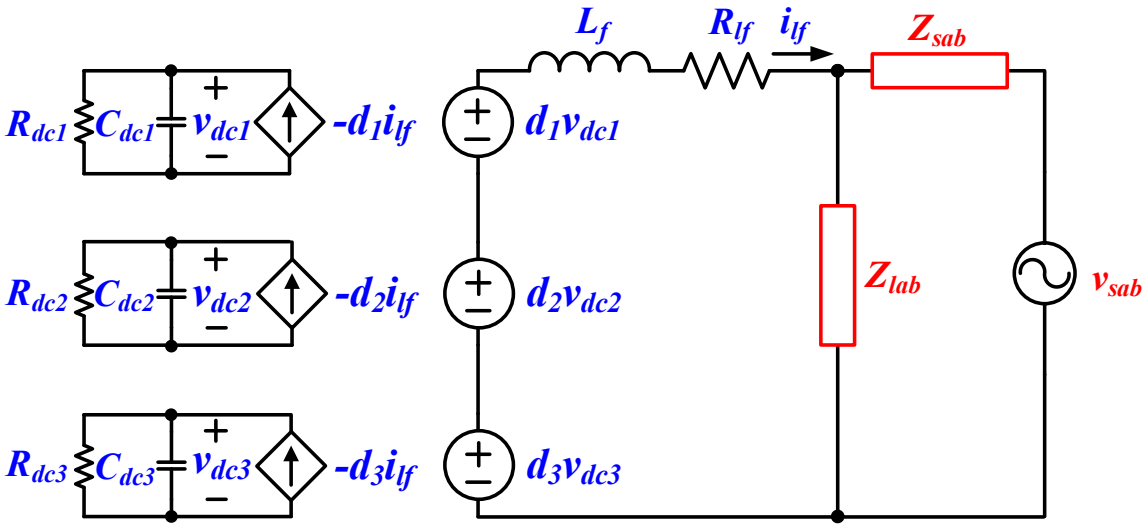


Figure 5-6: Equivalent multi-level cascaded H-bridge circuit

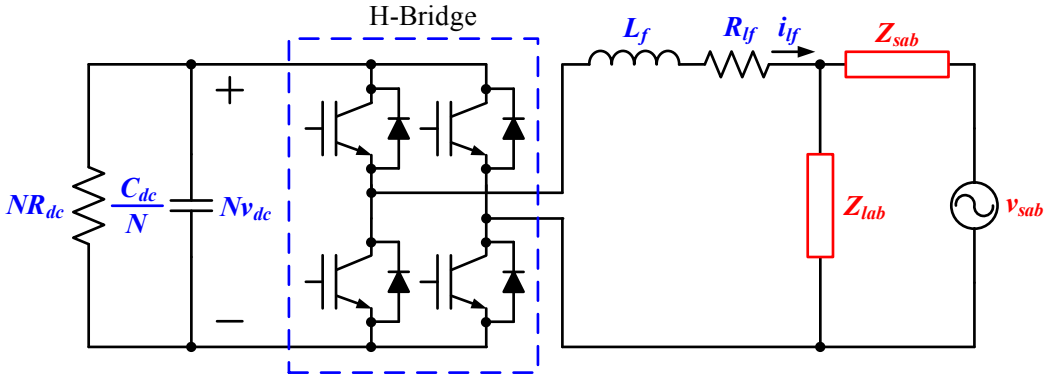
As mentioned, assuming quasi-stationary operating point, it is possible to linearize average model around each operating point separately, and design control for each operating point, being sure that control will have same bandwidth for all quasi-stationary operating points. The small-signal model obtained via reduced order modeling is written below.

$$\begin{bmatrix} \frac{d\tilde{v}_{dc}}{dt} \\ \frac{d\tilde{i}_{lf}}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{1}{C_{dc}R_{dc}} & -\frac{d(\theta_0)}{C_{dc}} \\ \frac{Nd(\theta_0)}{L_f} & -\frac{R_{lf}}{L_f} \end{bmatrix} \begin{bmatrix} \tilde{v}_{dc} \\ \tilde{i}_{lf} \end{bmatrix} + \begin{bmatrix} -\frac{i_{lf}(\theta_0)}{C_{dc}} \\ \frac{NV_{dc}}{L_f} \end{bmatrix} \tilde{d} + \begin{bmatrix} 0 \\ -\frac{1}{L_f} \end{bmatrix} \tilde{v}_{sab} \qquad 5\text{–}42$$

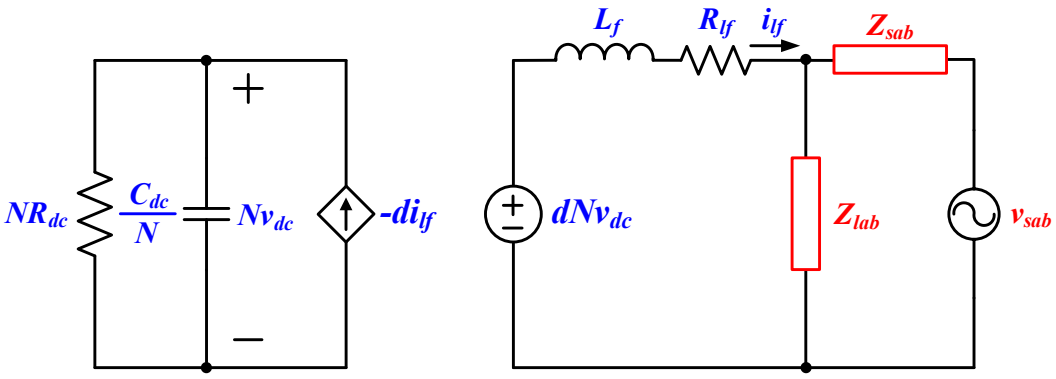
The plant transfer function that represents duty cycle to inductor current can be calculated from the previous equation.

$$G(s) = \begin{bmatrix} \frac{\tilde{v}_{dc}(s)}{\tilde{d}(s)} \\ \frac{\tilde{i}_{lf}(s)}{\tilde{d}(s)} \end{bmatrix} = (sI - A)^{-1} B \qquad 5\text{–}43$$

$$A = \begin{bmatrix} -\frac{1}{C_{dc}R_{dc}} & -\frac{d(\theta_0)}{C_{dc}} \\ \frac{Nd(\theta_0)}{L_f} & -\frac{R_{lf}}{L_f} \end{bmatrix}, B = \begin{bmatrix} -\frac{i_{lf}(\theta_0)}{C_{dc}} \\ \frac{NV_{dc}}{L_f} \end{bmatrix} \qquad 5\text{–}44$$



(a)



(b)

Figure 5-7: Reduced order modeling of multi-level cascaded H-bridge converter (a) switching model (b) averaged model

$$G_{ilfd}(s)=\frac{\tilde{i}_{lf}(s)}{\tilde{d}(s)}=\frac{\left(s+\frac{1}{C_{dc}R_{dc}}\right)\frac{NV_{dc}}{L_f}-\frac{Nd(\theta_0)i_{lf}(\theta_0)}{L_fC_{dc}}}{\left(s+\frac{1}{C_{dc}R_{dc}}\right)\left(s+\frac{R_{lf}}{L_f}\right)+\frac{Nd^2(\theta_0)}{L_fC_{dc}}} \qquad 5\text{–}45$$

The linearized transfer functions strongly depend on the values of the injected current and applied duty-cycles values. The steady-state values of inductor current and applied duty-cycle are ac variable, thus the linearized transfer functions are obtained for several operating point, covering whole period. Therefore, the quasi-stationary operating approach is a meaningful way to design current control. Several control duty-cycle to inductor current transfer functions for different pairs of $d(\theta_0)$ and $i_{lf}(\theta_0)$ are shown in Figure 5-8. The common property of all the presented graphs is that the dominant behavior in high frequency range is purely inductive, thus it is possible to reduce control duty cycle to inductor current transfer function to equivalent plant transfer function of inverter, assuming all the dynamic coming of dc capacitor will influence only low frequency part.

$$G_{ilfdcommon}(s)\approx\frac{\tilde{i}_{lf}(s)}{\tilde{d}(s)}=\frac{NV_{dc}}{Z_{lf}(s)}=\frac{NV_{dc}}{R_{lf}+sL_f} \qquad 5\text{–}46$$

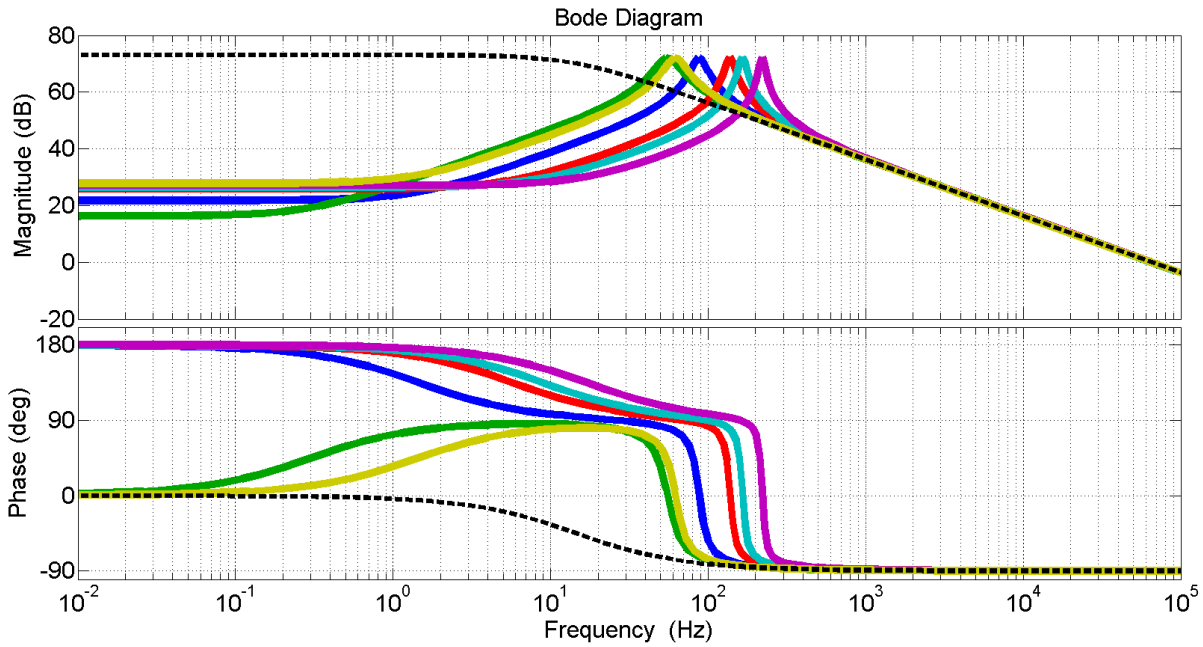


Figure 5-8: Family of bode plots of control duty-cycle to inductor current plant transfer functions: straight lines represent bode diagram of $G_{ilfd}(s)$, dashed line is bode diagram of $G_{ilfdcommon}(s)$

The initial design of the current controller can be done with the simplified transfer function, while after that the design can be verified by plotting several bode plots of current loop using different plant transfer functions.

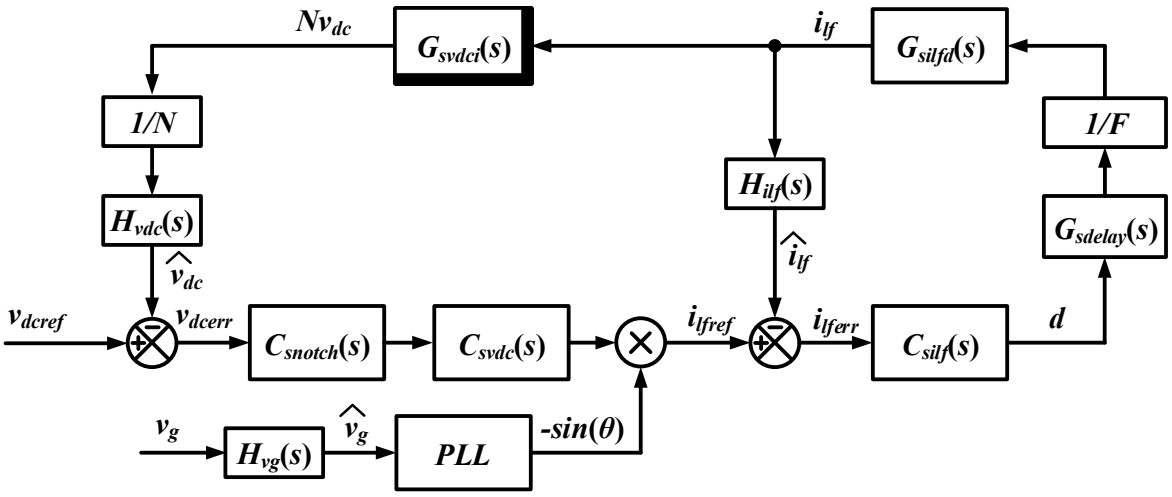


Figure 5-9: Transfer function block diagram of proposed control

5.3.2 Design of high-bandwidth inner current control

The high bandwidth inner current control is designed using a transfer diagram shown in Figure 5-9, which takes into account modulator delay due to digital implementation, sensor transfer functions and small-signal gain of modulator carrier.

The current compensator transfer function is designed to behave as a low-pass filter with integrator, low frequency zero, and a high frequency pole, ensuring a high gain in the low

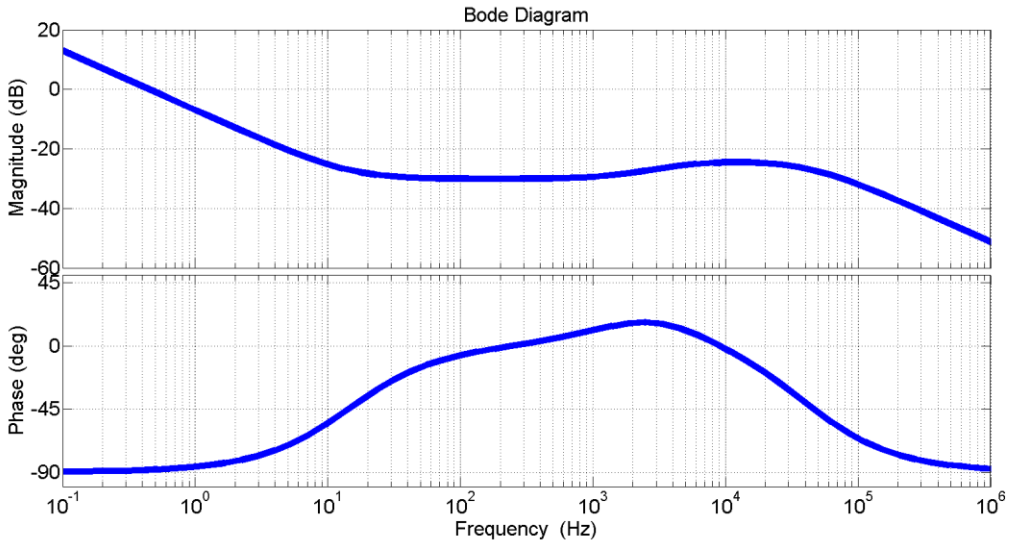


Figure 5-10: Bode plot of the current controller transfer function

frequency region. Bode plot of the designed current compensator is shown in Figure 5-10. The complete expression of used current controller is as

$$C_{silf}(s)=\frac{k_{ilf}}{s}\frac{\left(\frac{s}{\omega_{zilf1}}+1\right)\left(\frac{s}{\omega_{zilf2}}+1\right)}{\left(\frac{s}{\omega_{pilf1}}+1\right)\left(\frac{s}{\omega_{pilf2}}+1\right)} \qquad 5\text{–}47$$

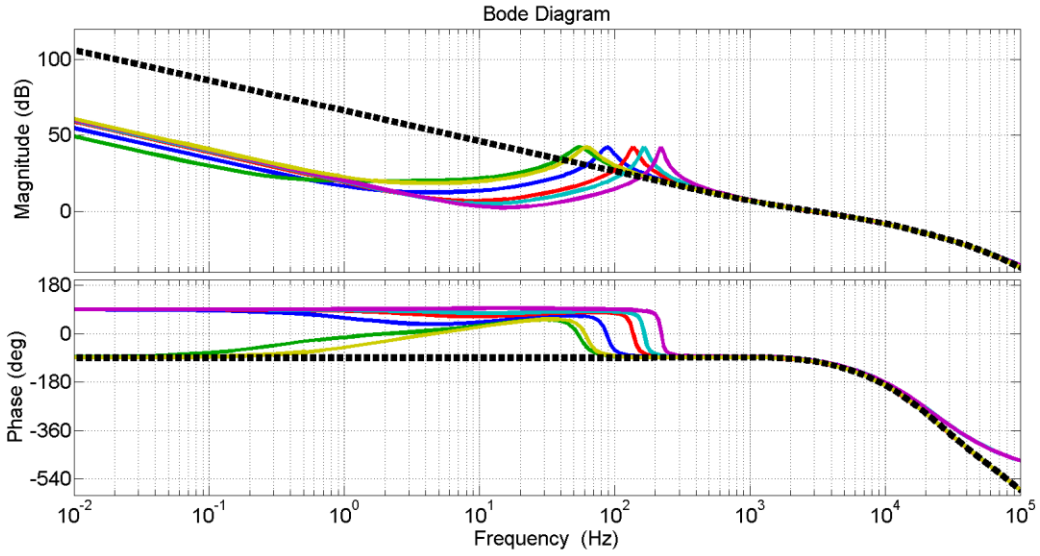


Figure 5-11: Family of bode plots of current loop gain transfer functions

Current loop gain is defined as a product of control duty cycle to inductor current transfer function, digital delay transfer function represented via second-order Pade's approximation and current compensator transfer function. Figure 5-11 shows current loop gain for different control duty-cycle to inductor current transfer functions, verifying that bandwidth of the loop is high for all the quasi-stationary operating point. The compensator current transfer function is designed to provide phase margin of 90 degrees, gain margin of 24 dB and bandwidth of 3 kHz for all given current loop plots. The analytical expressions of current loop gain, closed loop gain and Pade's approximation of digital delay are written here. The used digital delay is equal to one and half of switching period, where delay of digital modulator one half of the switching period and a delay due to DSP implementation is equal to one switching period.

$$T_{ilf}(s)=\frac{1}{F}H_{ilf}(s)C_{silf}(s)G_{ilfd}(s)G_{delay}(s) \qquad 5\text{–}48$$

$$G_{clilf}(s)=\frac{C_{silf}(s)G_{ilfd}(s)G_{delay}(s)}{1+\frac{1}{F}H_{ilf}(s)C_{silf}(s)G_{ilfd}(s)G_{delay}(s)} \quad 5\text{–}49$$

$$G_{delay}(s)=e^{-sT_d}\approx\frac{1-\frac{sT_d}{2}+\frac{(sT_d)^2}{12}}{1+\frac{sT_d}{2}+\frac{(sT_d)^2}{12}},T_d=1.5T_{sw} \quad 5\text{–}50$$

In this way a high bandwidth current control is closed, providing fast and accurate generation of the different injection signals. Furthermore, fundamental frequency component at line frequency is generated very precisely as current loop gain is high in low frequency region, enabling decoupling of the dc voltage control from the fast current control.

5.3.3 Design of outer voltage control

The dc voltage loop is designed to have slow dynamic, assuming the current loop dynamic is much faster and can be assumed as ideal control that can perfectly reproduce input reference signal. In this sense, the closed loop gain of current control can be assumed ideal with unity magnitude gain and zero phase delay, resulting in accurate reference tracking. The voltage loop is slow and needs to be at least one decade below the lowest frequency injection point, providing decoupling between fast current loop and slow dc voltage loop. The power balance modeling is used for plant transfer function derivation, which is typically used in PFC circuits and grid connected converters [97], [98], [126]. The power balance equation of the injection converter circuit is as follows,

$$Nv_{dc}i_{dc}=v_{srms}i_{lfrms} \quad 5\text{–}51$$

$$N\frac{v_{dc}^2}{Z_{dc}(s)}=v_{srms}\frac{i_{lfm}}{\sqrt{2}} \quad 5\text{–}52$$

The inductor current magnitude to output dc voltage is derived by linearization of the power balance equation, yielding the following results.

$$N\frac{2V_{dc}\tilde{v}_{dc}}{Z_{dc}(s)}=V_{srms}\frac{\tilde{i}_{lfm}}{\sqrt{2}} \quad 5\text{–}53$$

$$G_{svdci}(s)=\frac{\tilde{v}_{dc}(s)}{\tilde{i}_{lfm}(s)}=\frac{V_{srms}}{2\sqrt{2}NV_{dc}}Z_{dc}(s)=\frac{V_{srms}}{2\sqrt{2}NV_{dc}}\frac{R_{dc}}{sC_{dc}R_{dc}+1} \quad 5\text{–}54$$

If big resistor is placed in parallel with dc capacitors, then previous plant transfer function reduces to the following expression

$$G_{svdcidef}(s)=\frac{\tilde{v}_{dc}(s)}{\tilde{i}_{lfm}(s)}=\frac{V_{srms}}{2\sqrt{2}NV_{dc}}Z_{cdc}(s)=\frac{V_{srms}}{2\sqrt{2}NV_{dc}}\frac{1}{sC_{dc}} \quad 5\text{–}55$$

The previous derived plant transfer function can be used to design a low bandwidth dc voltage loop, ensuring precise regulation of the mean value of dc capacitor voltages. Equivalent transfer function diagram of the proposed controller is obtained via reduced order modeling and it includes fast inner current loop and slow outer dc voltage loop as shown in Figure 5-9. The designed voltage compensator consists of integrator to ensure accurate dc reference tracking, one zero in the low frequency range and the high frequency pole above the dc voltage loop bandwidth.

$$C_{svdc}(s)=\frac{k_{idc}}{s}\frac{(s+\omega_{zdc})}{(s+\omega_{pdc})} \quad 5\text{–}56$$

$$C_{snotch}(s)=\frac{(s^2+Q_{zn}\omega_n s+\omega_n^2)}{(s^2+Q_{pn}\omega_n s+\omega_n^2)} \quad 5\text{–}57$$

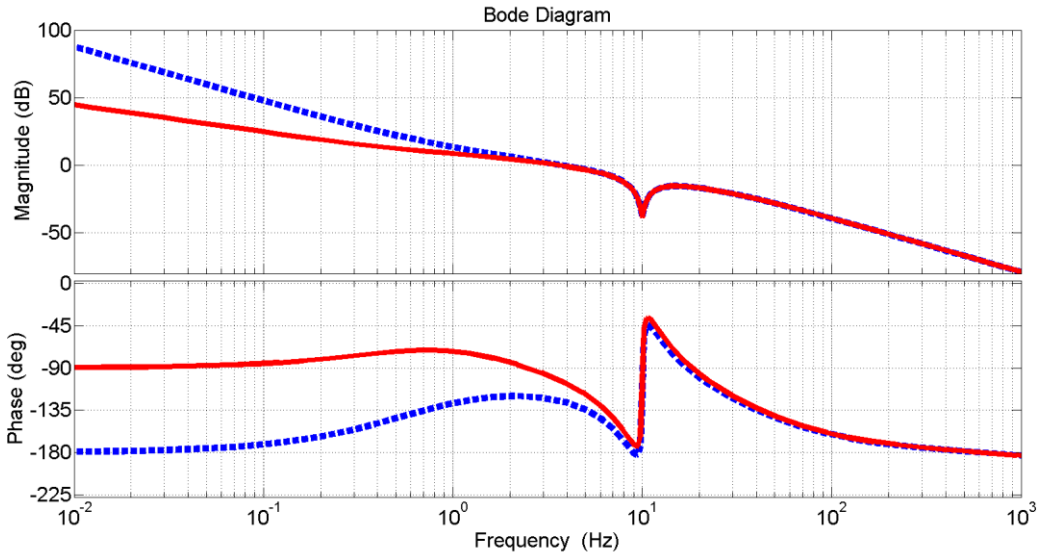


Figure 5-12: Bode plots of dc voltage loop gain transfer functions: $T_{vdc}(s)$ (straight red line) and $T_{vdcdef}(s)$ (dashed blue line)

The dc voltage loop is designed to have 2 Hz bandwidth and phase margin equal to 70 degrees. Notch filter is used only when current is injected close to line frequency, resulting in low frequency ripple with significant magnitude on dc side.

$$T_{vdc}(s)=\frac{1}{N}G_{svdci}(s)C_{svdc}(s)C_{snotch}(s) \quad 5\text{–}58$$

Similarly, voltage loop gain expression using $G_{svdcidef}(s)$ plant transfer function is:

$$T_{vdcdef}(s) = \frac{1}{N} G_{svdcidef}(s) C_{svdc}(s) C_{snotch}(s) \qquad 5\text{–}59$$

Addition of the notch filter will attenuate propagation of low frequency ripple into the control part and consequently into converter itself, enabling generation of inductor current without unwanted low frequency components. The dc voltage loop gain including $C_{svdc}(s)$ and $C_{snotch}(s)$ compensators is shown in Figure 5-12. In this case a notch filter, which attenuates ripple at 10Hz is used to plot bode diagrams of dc voltage loop gain transfer functions $T_{vdc}(s)$ and $T_{vdcdef}(s)$.

5.3.4 DC voltage balancing control

The voltage balancing control is designed to have approximately same bandwidth as the dc voltage loop. However, the control is tuned by running extensive simulations and observing settling time of the responses. The used voltage balancing control consists of integrator, one low frequency zero placed below the control's bandwidth and one high frequency pole.

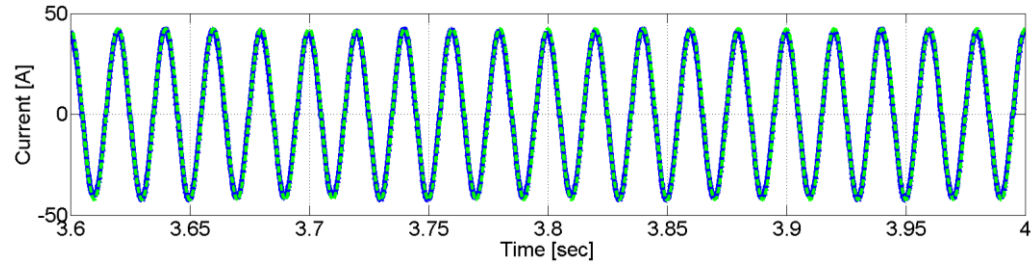
$$C_{svbal}(s) = \frac{k_{ibal}}{s} \frac{(s + \omega_{zbal})}{(s + \omega_{pbal})} \qquad 5\text{–}60$$

5.4 Validation of the design procedure in simulations

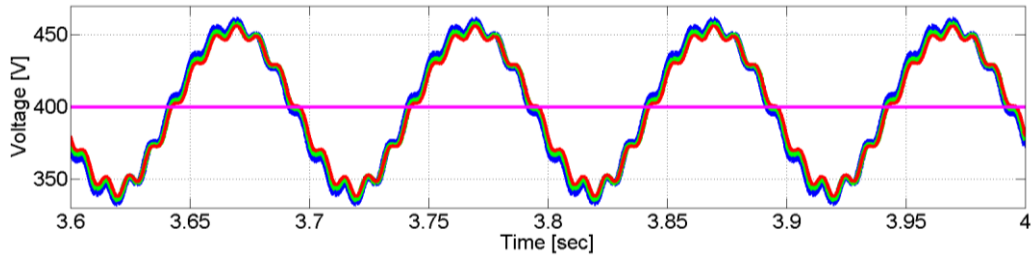
The time domain switching simulation model of the multi-level shunt current injection converter is built and extensively tested in MATLAB/Simulink software with the usage of SimPowerSystems toolbox. The software environment is used to simulate switching model and to characterize the properties of the injected signal and to verify the described designed procedure. This section describes and shows two different simulated operating points, verifying design of the converter regarding capacitor and inductor value selection and validating design of several control loops.

The first simulated operating point investigates waveforms when low frequency (50 Hz) current is being injected into the grid, this operating point is equivalent to 10 Hz injection in dq coordinates. Thus, in this operating point a low frequency voltage ripple at 10 Hz is present in dc capacitor voltages. Other critical operating point is a high frequency injection of 30 A rms, 1 kHz current into the system. Figure 5-13 shows simulation waveforms that verify proper operation when converter is injecting a 50 Hz sinusoidal signal. The dc voltages are balanced among themselves and 10 Hz ripple is slightly below 60 V, which is correctly predicted by analytical

expressions. Furthermore, current control ensures that generated current $i_{lf}(t)$ tracks perturbation reference signal precisely.



(a)



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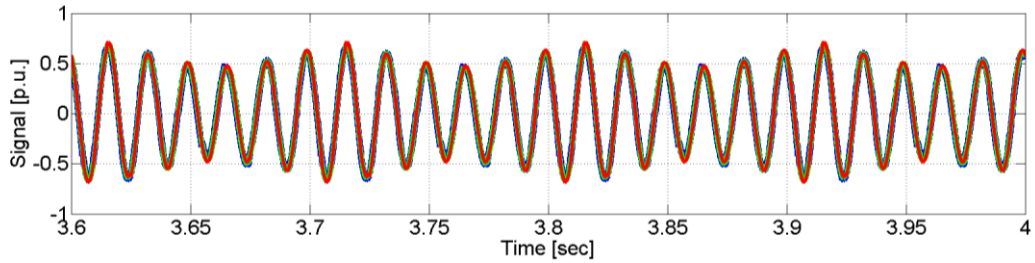

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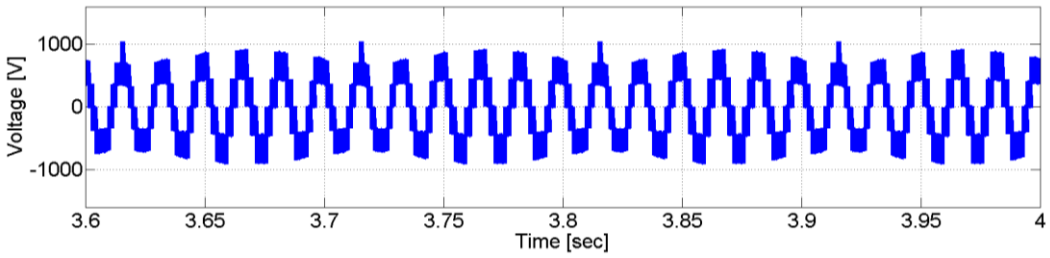


(d)

Figure 5-13: Simulation waveform signals for 30A rms, 50 Hz sinusoidal current injection operating point (a) inductor current $i_{lf}(t)$ and current reference $i_{ref}(t)$ (b) dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$, $v_{dc3}(t)$ and dc voltage reference $v_{dcref}(t)$ (c) duty cycles $d_1(t)$, $d_2(t)$, $d_3(t)$ (d) switching voltage $v_{dcsw}(t)$.

Figure 5-14 shows simulation waveforms of same variables when 1000 Hz 30A rms sinusoidal injection current is being generated by shunt current injection converter. Obtained inductor current $i_{lf}(t)$ waveform shows that current control has high bandwidth capable of generating 1 kHz current,

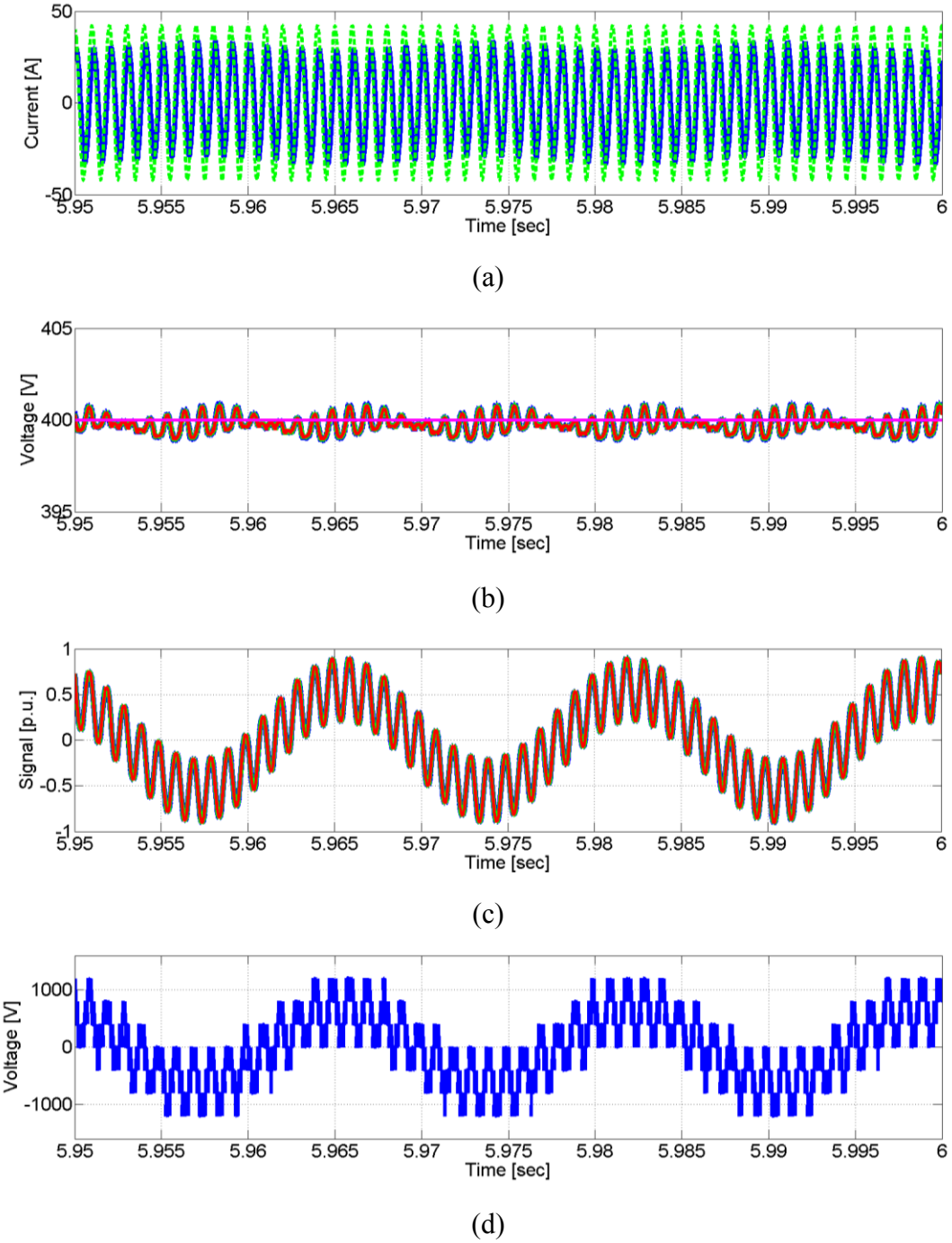


Figure 5-14: Simulation waveform signals for 30A rms, 1000 Hz sinusoidal current injection operating point (a) inductor current $i_{lf}(t)$ and current reference $i_{ref}(t)$ (b) dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$, $v_{dc3}(t)$ and dc voltage reference $v_{dcref}(t)$ (c) duty cycles $d_1(t)$, $d_2(t)$, $d_3(t)$ (d) switching voltage $v_{dcsw}(t)$.

All three dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and $v_{dc3}(t)$ are balanced and accurately regulated to follow 400 V dc reference. Furthermore, duty cycle peak values are as specified in design procedure below 0.9, keeping the converter in the operation range outside the overmodulation region. It is verified when 1 kHz current is being injected duty cycles are near the limit as predicted in design procedure.

5.5 Experimental Verification

The hardware prototype, which is shown in Figure 5-15, of a multi-level single-phase shunt current injection converter is built to experimentally prove feasibility of the proposed multi-level solution. The experimental set-up consists of three H-bridge modules, which are connected to a programmable voltage source (20 A, 120 V, 60 Hz) via six inductors (0.33 mH). Furthermore, each H-bridge module has a dc capacitor (220 μF) and a dc resistor (500 Ω). The control board hardware includes Texas Instruments control card TMS320C28343, together with CPLD chip and analog part for sensing currents and voltages, providing effective resources for a control of the implemented converter.

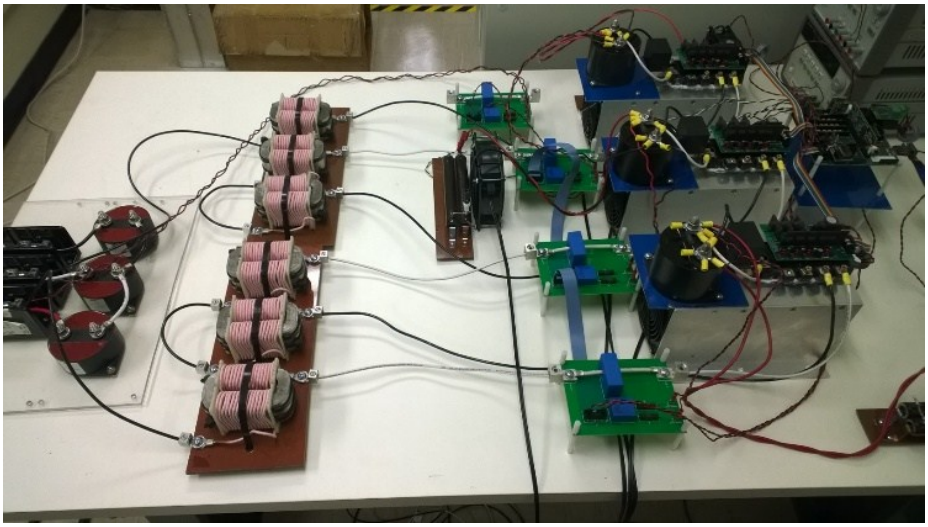


Figure 5-15: Hardware prototype of the designed multi-level single-phase shunt current injection converter.

The proposed seven-level single phase shunt current injection converter is connected in parallel with programmable source, which is feeding high-power factor resistive-capacitive load (17 Ω, 99 μF). The converter is run to inject a perturbation into a described system. Figure 5-16 shows steady-state experimental waveforms for a twelve line periods (20ms) when 5A current at 500Hz is being injected, verifying that the proposed controller regulates current i_{lf} and dc voltages v_{dc1},

v_{dc2}, and v_{dc3} accurately follow dc reference. In order to maintain dc voltages, inductor current i_{lf} has dominant line frequency component, which provides active power to cover losses in bridges and dc resistor dissipation.

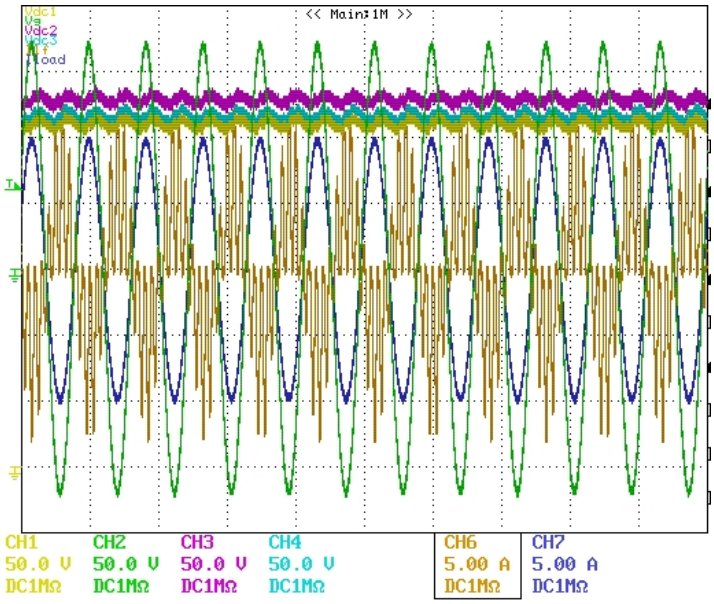


Figure 5-16: Experimental waveforms of converter current $i_{lf}(t)$, load current $i_{load}(t)$, dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$, $v_{dc3}(t)$, and source voltage $v_g(t)$.

In addition, Figure 5-17 compares spectrums of inductor current i_{lf} obtained via simulation and experiment, showing excellent matching of developed switching simulation model with constructed shunt current injection converter hardware.

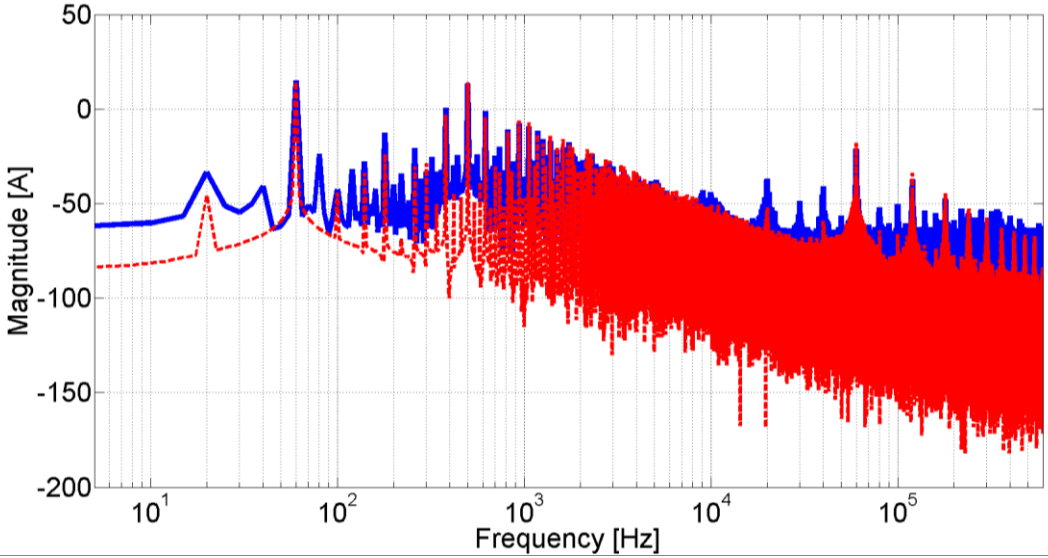


Figure 5-17: Spectral content comparison of inductor current $i_{lf}(t)$ obtained via simulation (dashed red line) and experiment (straight blue line).

5.6 Summary

This chapter describes the detailed design procedure for a multi-level single-phase cascaded H-bridge converter, which is suitable for the shunt current injection. The design procedure includes parameters selection, component value optimization, minimization of the size and weight of inductors and capacitors. Furthermore, the design of the inner current control, voltage balancing among modules, and outer capacitor voltage regulation is presented. Analytical expressions are derived for each critical design step. In addition, the design procedure is completely verified in the simulations using switching model, dead-time and digital controller, proving the effectiveness of the proposed approach. Excellent agreement between analytical expressions, detailed switching simulation model and experimental results is presented. Reduced order dynamic average value modeling approach is used and shown to be very effective tool in the design procedure. A new solution for shunt current injection used for small-signal dq and dc impedance identification is proposed in this paper, consisting of multi-level cascaded H-bridge converter structure, improving overall performance of the converter compared to classical single-module H-bridge converter solution. Finally, the multi-level SCI converter is constructed and experimentally tested, proving feasibility of the proposed concept.

Chapter 6. Interleaved Single-Phase Series Voltage Injection Converter used in Small-Signal dq Impedance Identification

Stability analysis of modern three-phase ac power systems is performed using small-signal impedances identified in synchronous reference dq frame. A single-phase series voltage injection is used to perturb ac and dc systems in order to perform small-signal impedance identification. This chapter explains the design of the interleaved cascaded H-bridge converter, which is used to generate a single-phase voltage perturbation in series with power system. Special attention is focused on the design procedure, including the selection of inductors and capacitors values, trying to optimize converter's performance and maximize injection range. The decoupling control is proposed to regulate ac injection voltage, providing robust and reliable strategy for the regulation series voltage injection. Furthermore, a low bandwidth dc voltage control is included into the control, assuring dc voltage control for each H-bridge module. The dc voltage control regulates average value of capacitor dc voltages by aligning the line frequency reference of injection voltage with system current. Analytical expressions, which completely describe the control procedure, are derived and presented in the analysis. The proposed converter is extensively simulated using switching simulation model and excellent agreement with the developed design procedure is presented. Simulation model and hardware prototype results verify effectiveness of the proposed series voltage injection solution.

6.1 Introduction

Apparently, there is a need to inject voltage and current perturbations into a system to obtain accurate identification of load and source small-signal dq impedances. Therefore, the scope of this chapter is a design procedure of a single-phase interleaved series voltage injection (SVI) converter using H-bridge modules, which is shown in Figure 6-1. The converter's purpose is to generate a voltage perturbation in series with the system, in order to excite response of the power system at desired frequencies. Furthermore, generation of the injection voltage is done in a controlled manner via the ac decoupling control. Typical applications in which decoupling ac control is commonly used to regulate series injection voltage are uninterruptable power supplies (UPS), and

dynamic voltage restorer (DVR) [104], [105]. Following this idea, this chapter proposes to use a decoupling control to effectively regulate small-signal series injection voltage. The proposed solution reduces size and cost of the SVI converter, as it does not require an isolation transformer. In this way, it is capable of injecting frequency components close to dc in dq coordinates, which are not feasible with transformer SVI converter solutions. It differs from DVR application as it does not need a separate energy storage device, resulting in reduced size, cost and weight converter hardware. The proposed interleaved single-phase converter is a practical solution for single-phase SVI with the following properties: modular design, capacitor energy distribution, reactive component minimization, higher equivalent switching frequency, providing a capability to inject

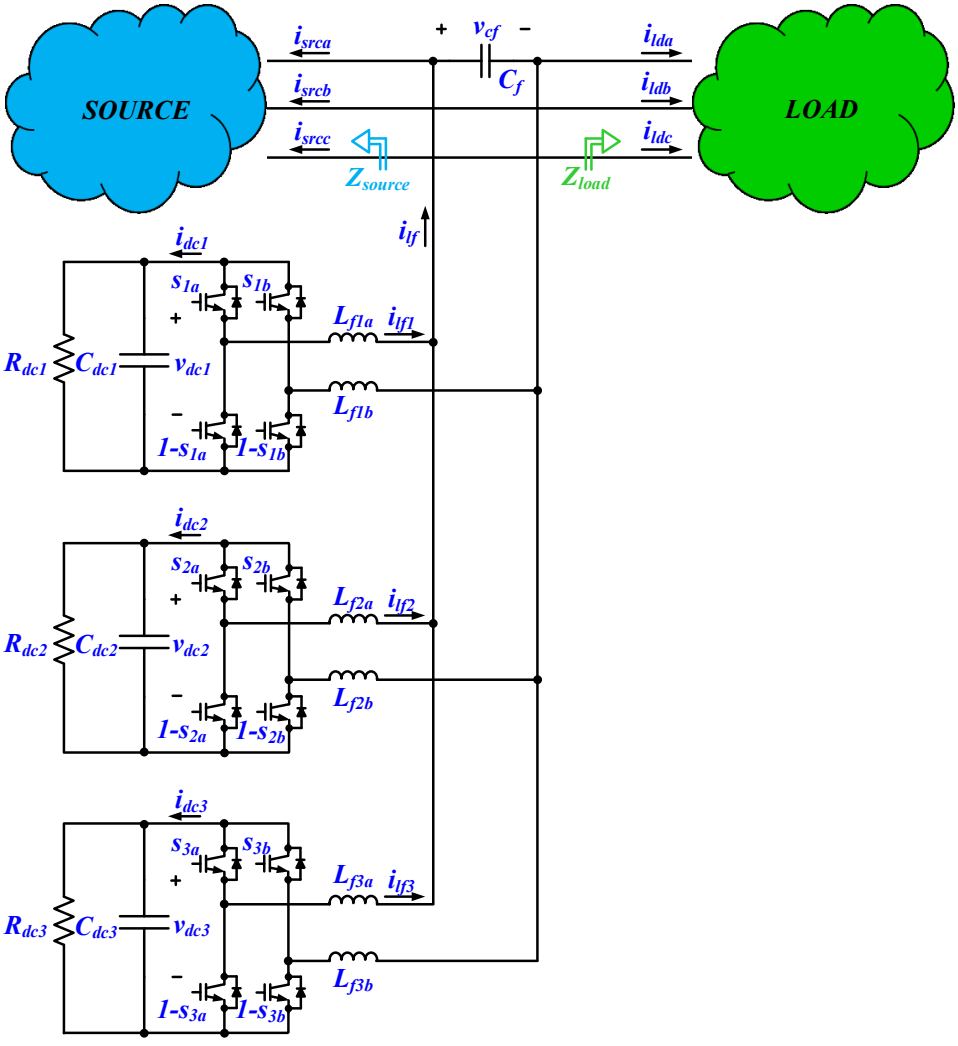


Figure 6-1: Interleaved single-phase series voltage injection converter with H-bridge modules

higher frequency signals, interleaved solution is suitable to perturb high power systems and finally it is capable of generating cleaner injection signals.

6.2 Design of interleaved single-phase series voltage injection converter based on H-bridge modules

The proposed interleaved SVI converter is shown in Figure 6-1. It consists of three H-bridge modules, where each modules has two ac inductances, a dc capacitance and a dc resistor. The purpose of the inductances is to filter switching voltage in order to generate clean current. The dc capacitors have two main tasks, where the first one is to store dc voltage, providing stable operating point for voltage source converter. Furthermore, dc capacitors are main storage for reactive energy, which is exchanged between the system and converter during the low frequency injection. A high value resistor (30 kΩ) is placed in parallel with each dc capacitor, providing voltage discharge when the converter is turned off. The resistance value is selected to be high enough, so it can be neglected in the control analysis. The series voltage is injected via capacitor C_f, which is series inserted between source and load, providing transformerless injection solution. Furthermore, three H-bridge modules are interleaved, providing current sharing, which results in higher efficiency of the interleaved injection converter. In addition, interleaved operation offers generation of switching noise in higher frequency range, providing a generation of cleaner series voltage injection signal. Ideally, designed transformerless SVI converter should generate injection signal at only desired frequencies without any unwanted harmonics. Therefore, interleaved solution offers significant benefits in both aforementioned design considerations, being suitable solution for a series voltage injection. Parameters of the SVI converter, which are used throughout this chapter are given below in Table 6-1.

The implemented control of SVI converter, which regulates average value of dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and $v_{dc3}(t)$, capacitor voltage $v_{cf}(t)$, inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$ and provides voltage balancing among dc capacitor voltage of H-bridge modules is shown in Figure 6-2. The control includes low bandwidth dc voltage control, which provides line frequency reference for the injection voltage $v_{cf}(t)$. This reference is aligned via PLL with the system current, providing active power to cover the converter losses and regulate average dc voltage value of dc capacitors.

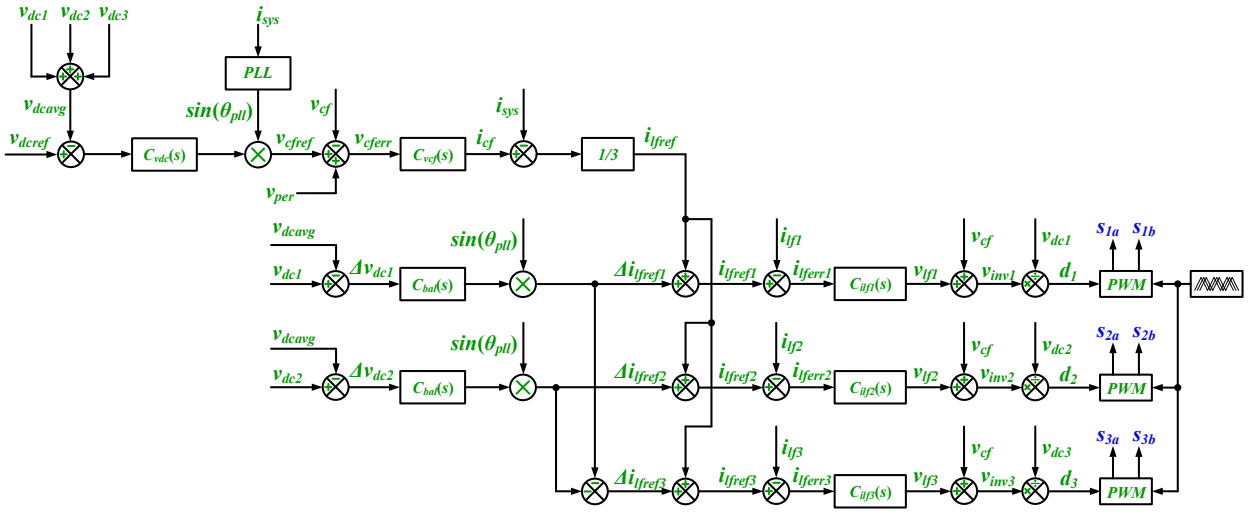


Figure 6-2: Block diagram of the proposed decoupling control for interleaved SVI converter

The ac decoupling control includes regulator for voltage $v_{cf}(t)$ and all three inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$, providing robust control that effectively decouples power system dynamics from the injection converter dynamics. Two balancing controllers regulate voltage balancing among capacitors voltages by changing current references of the corresponding inductor currents. The detailed analysis of all control loops will be presented in the following sections.

Table 6-1 Three-phase power system specifications

Parameter name	***Value***	***Parameter name***	***Value***
DC voltage	V_{DC}=200 V	Inductance	L_f=0.33 mH
Peak dc voltage	v_{dcpeak}=300 V	DC capacitance	C_{dc}=0.22 mF
Injection frequency	f_{inj}=10 Hz-1 kHz	AC capacitance	C_f=35 μF
RMS of system ac voltage	V_{srms}=120 V	System phase rms current	I_{srms}=100 A
Switching frequency	f_{sw}=10 kHz	Switching frequency of H-bridge	f_{swh}=20 kHz
Number of modules	N=3	Equivalent switching frequency	f_{sweq}=60 kHz

6.2.1 Operating point calculation

Analytical expressions describing different operating points are derived in this section using the equivalent averaged model of SVI shown in Figure 6-3. The derived expressions are general and can be used to design SVI converter for injection into arbitrary power system, simply by using system's voltage and power rating. In order to guarantee the generation of desired injection signals

in the full frequency injection range at maximum magnitude, the derived analytical expressions are used to select capacitor and inductor values.

The duty cycle will consist of two components, namely system frequency component $d_s(t)$ and injection component $d_i(t)$. The system frequency component will provide active power to regulate dc voltages at specified level and cover the losses of each converter: switching and conduction losses of H-bridges, losses in inductors and dissipation losses of resistors. As mentioned previously, the proposed control will align injection voltage $v_{cf}(t)$ to a system current via the system duty cycle component. In addition, control performs one more task of generating a desired injection signal, which is achieved by the injection component of duty cycle $d_i(t)$. The total duty cycle applied to each H-bridge can be written in the following manner.

$$d(t) = d_s(t) + d_i(t) \qquad 6\text{–}1$$

In order to derive a system duty cycle component, we will assume that during the steady state operation system current $i_{sys}(t)$ is equally shared by all three H-bridges. The described assumption

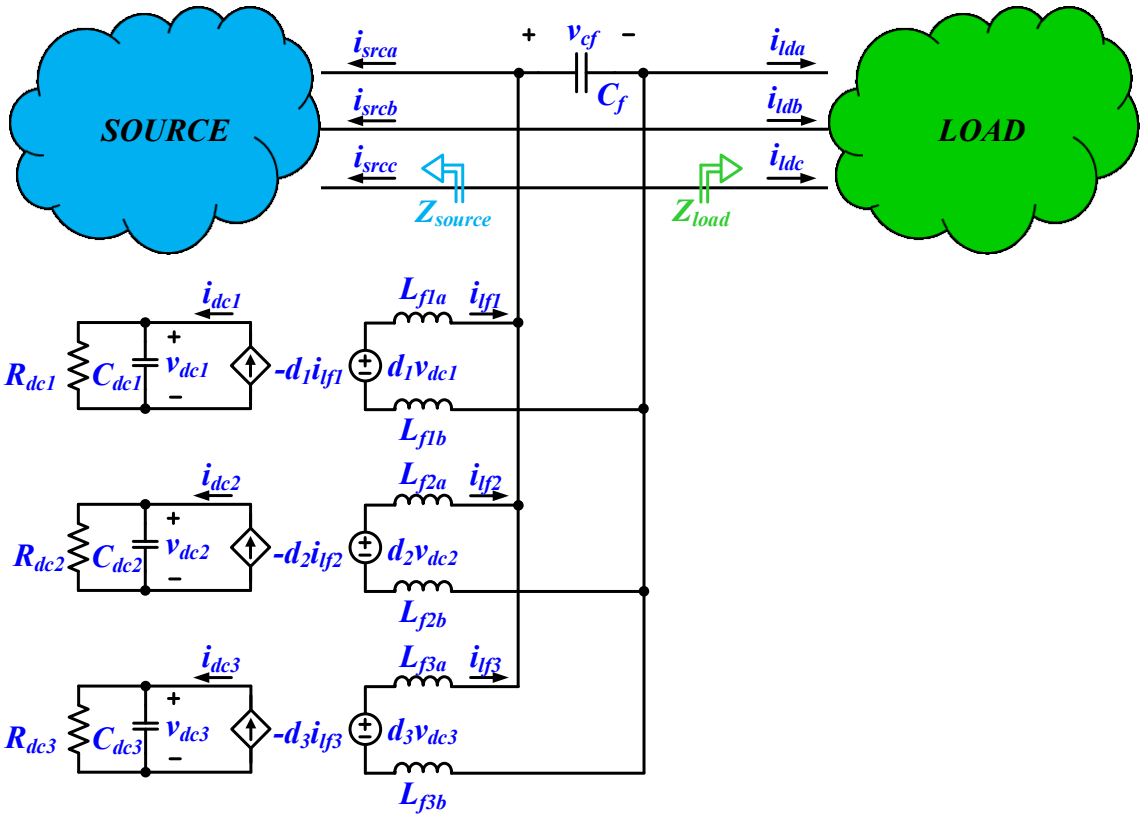


Figure 6-3: Equivalent averaged model of single-phase interleaved series voltage injection converter, which is connected in series with a power system

is enforced by the control, if all the control loops are properly designed. If the switching ripple is averaged, then the line frequency component (system component) $i_{lfs}(t)$ of inductor current can be described by the following expression.

$$\begin{aligned} i_{lfs}(t) &= I_{lfsm}\sin(\theta_s(t)) \\ \theta_s(t) &= \omega_s t + \theta_{so} \end{aligned} \qquad 6\text{–}2$$

Where $\theta_s(t)$ is a phase of system current and ω_s is a power system angular frequency. Furthermore, the control will align the line frequency component of the injection voltage $v_{cf}(t)$ with the system current, thus the following expression is true.

$$v_{cfs}(t) = V_{cfsm}\sin(\theta_s(t)) \qquad 6\text{–}3$$

In this way the active power delivered via the series injected capacitor C_f will regulate the dc value of H-bridge voltages by covering the losses of each converter. Thus, the following expression can be written.

$$0.5 I_{lfsm} V_{cfsm} = P_{losses} \qquad 6\text{–}4$$

After applying the KVL and KCL, the following equations are written below.

$$d_s(t) V_{dc} = L_f \frac{di_{lfs}(t)}{dt} + R_{lf} i_{lfs}(t) + v_{cfs}(t) \qquad 6\text{–}5$$

Since all the terms in the previous equation are well defined, the system component of the duty cycle is calculated as follows.

$$d_s(t) = D_{sm}\sin(\theta_s(t) + \theta_{dso}) \qquad 6\text{–}6$$

$$D_{sm} = \frac{\sqrt{(L_f \omega_s I_{lfsm})^2 + (R_{lf} I_{lfsm} + V_{cfm})^2}}{V_{dc}} \qquad 6\text{–}7$$

$$\theta_{dso} = \arctan\left(\frac{L_f \omega_s I_{lfsm}}{R_{lf} I_{lfsm} + V_{cfm}}\right) \qquad 6\text{–}8$$

The magnitude of system duty cycle component mainly depends on magnitude of system current and losses of the converter. Usually the inductance L_f is selected to have small impedance

at line frequency ω_s and if converter is properly designed, losses can be neglected, meaning that system component of duty cycle is negligible.

In similar way, the injection component of duty cycle is derived. If the switching ripple is averaged, the injection component of voltage $v_{cf}(t)$ is written as follows.

$$v_{cfi}(t) = V_{cfim}\sin(\theta_i(t)) \tag{6–9}$$

$$\theta_i(t) = \omega_i t + \theta_{io} \tag{6–10}$$

Where V_{cfim} and ω_i are magnitude and angular frequency of the injection voltage signal, respectively. Again, after applying the KVL and KCL, the following equations are written below.

$$d_i(t)V_{dc} = L_f\frac{di_{lfi}(t)}{dt} + R_{lf}i_{lfi}(t) + v_{cfi}(t) \tag{6–11}$$

$$i_{lfi}(t) = C_f\frac{dv_{cfi}(t)}{dt} + \frac{V_{cfim}}{|Z_e(j\omega_i)|}\sin(\theta_i(t) + \theta_{zeo}) \tag{6–12}$$

Where $Z_e(j\omega_i)$ represents the equivalent series impedance of source and load, which is seen from the terminals of series inserted capacitor C_f. If the equivalent impedance $Z_e(j\omega_i)$ is high, small injection current $i_{lfi}(t)$ will be generated in inductor L_f, while if the equivalent impedance is small the injection current $i_{lfi}(t)$ can be significantly increased. The worst case occurs if the equivalent impedance $Z_e(j\omega_i)$ is small in the high frequency region, resulting in high injection current, which can cause H-bridge to operate in the overmodulation region. The overmodulation region is not desired as converter is not fully controllable and it generates more unwanted line and switching harmonics.

After substituting the expression of injection voltage signal, $v_{cfi}(t)=V_{cfim}\sin(\theta_i(t))$, into the last two equations the injection duty cycle is written below.

$$d_i(t)\frac{V_{dc}}{V_{cfim}} = \sqrt{(1 - L_f C_f \omega_i^2) + (R_{lf} C_f \omega_i)^2}\,\sin(\theta_i(t) + \theta_{10}) + \sqrt{\frac{(\omega_i L_f)^2 + R_{lf}^2}{|Z_e|^2}}\sin(\theta_i(t) + \theta_{20} + \theta_{ze}) \tag{6–13}$$

Finally, the injection component of duty cycle can be approximated with a sinusoidal signal, where the following inequality for the signal magnitude holds true.

$$d_i(t) = D_{im}\sin(\theta_i(t) + \theta_{io}) \tag{6–14}$$

$$D_{im} < \frac{V_{cfim}}{V_{dc}} \left(\sqrt{\left(1 - L_f C_f \omega_i^2\right) + \left(R_{lf} C_f \omega_i\right)^2} + \sqrt{\frac{\left(\omega_i L_f\right)^2 + R_{lf}^2}{\left|Z_e\left(j\omega_i\right)\right|^2}} \right) \qquad 6\text{–}15$$

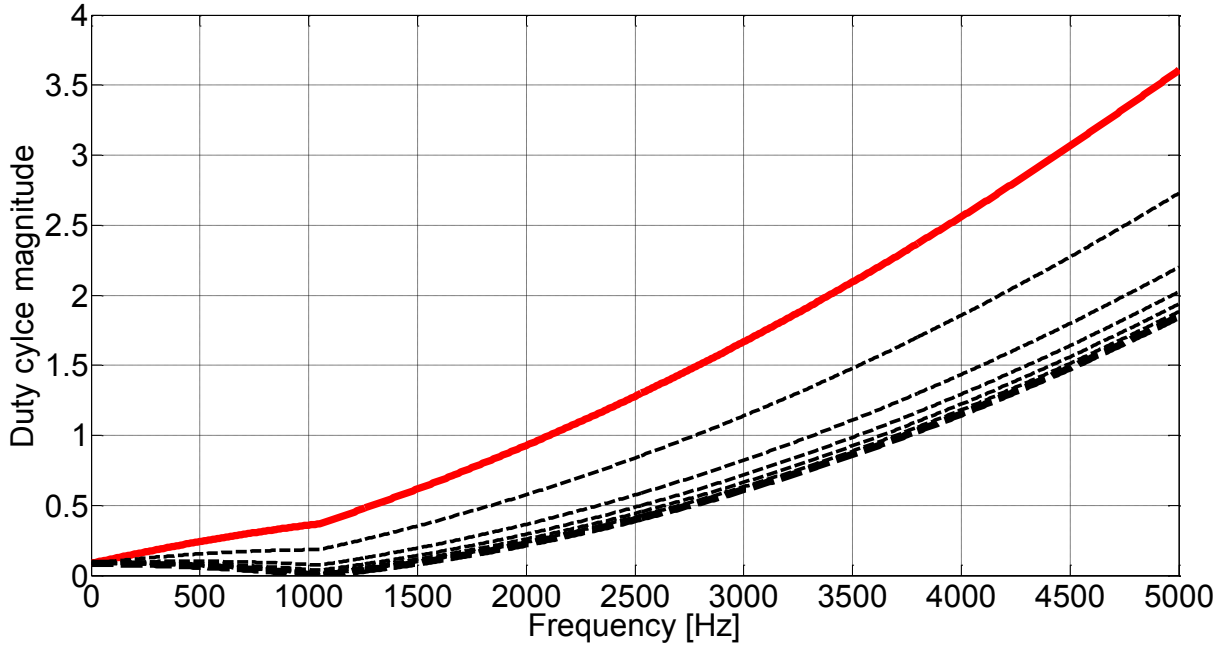


Figure 6-4: Duty cycle injection magnitude versus injection frequency for different values of equivalent system impedance: Z_e=1 Ω (red straight line), Z_e increases (black dashed lines)

It is interesting to plot the dependence of injection duty cycle magnitude with respect to injection frequency for a range of equivalent system impedance values using previously derived equation. The equivalent system impedance seen by capacitor C_f terminals is equal to sum of source and load impedances, $Z_e(s)=Z_s(s)+Z_l(s)$. The proper selection of inductance L_f and capacitance C_f values ensures that converter can generate maximum voltage perturbation in the whole injection frequency range, while converter operates in safe region far enough from the overmodulation region. By avoiding overmodulation region, converter guarantees a controllability of the converter control variables, including the injection voltage $v_{cf}(t)$. Based on the previous analysis, Figure 6-4 shows magnitude of duty cycle injection component versus injection frequency for a range of equivalent system impedances, $1\Omega < \left|Z_e\left(\omega_i\right)\right| < \text{inf}$, , verifying that selected component values provide capability to inject voltage perturbation in the specified frequency range. The converter cannot characterize source and load impedances, whose sum is below 1Ω in the high frequency range. The last condition is usually satisfied in the practice. Even if the SVI

converter is used to perturb a system with infinite small-signal equivalent impedance, the maximum injection frequency is limited to 3.5 kHz.

6.2.2 Selection of dc capacitance value

The design of dc capacitances is done using the averaged model of the interleaved SVI converter. The main task for dc capacitances is to provide stable dc voltage for the stable operation of each H-bridge module. In addition, during the low frequency injection, dc capacitors are main storage components for reactive energy, which is being exchanged between system under measurements and injection SVI converter. Thus, a low frequency voltage ripple will exist when frequency low to system frequency is being injected into the system. The capacitance is designed to keep low frequency voltage ripple within the boundaries specified in Table 6-1. Following the similar reasoning as in calculation of the steady state duty cycle components, the voltage ripple component at injection frequency f_i can be calculated in the following way.

$$i_{cdc1}(t) = -d_1(t) i_{lf1}(t) \qquad 6\text{–}16$$

$$C_{dc1} \frac{dv_{dc1}(t)}{dt} = -\left(d_{1i}(t) + d_{1s}(t)\right)\left(i_{lf1i}(t) + i_{lf1s}(t)\right) \qquad 6\text{–}17$$

The main low frequency voltage component will come from injection duty cycle $d_{1i}(t)$ and system current component of inductor current $i_{lf1}(t)$. Under this assumption, other terms obtained from the product can be neglected, yielding the following results.

$$\Delta v_{dc1}(t) = -\frac{1}{C_{dc1}} \int d_{i1}(t) i_{lf1s}(t) dt \qquad 6\text{–}18$$

$$\Delta v_{dc1}(t) = -\frac{D_{im} I_{lfsm}}{C_{dc1}} \int \sin(\omega_i t + \theta_{io}) \sin(\omega_s t + \theta_{so}) dt \qquad 6\text{–}19$$

The last expression can be further approximated if a product of the sinusoidal terms is transformed into a sum, where the high frequency component is neglected.

$$\Delta v_{dc1}(t) \approx -\frac{D_{im} I_{lfsm}}{2C_{dc1}} \int \cos(\Delta\omega t + \theta_{\Delta}) dt$$
$$\Delta\omega = \omega_i - \omega_s \qquad 6\text{–}20$$

Finally, the magnitude of dc voltage ripple can be approximated with the following expression as written below.

$$\Delta V_{dcm} = \frac{D_{im} I_{lfsm}}{2\Delta\omega C_{dc1}} < kV_{dc} \qquad 6\text{–}21$$

In order to keep the peak value of dc voltage below allowed value it is necessary that capacitance satisfies following inequality.

$$C_{dc1} > \frac{D_{im} I_{lfsm}}{4\pi\Delta f k V_{dc}} \qquad 6\text{–}22$$

The capacitance value is a function of maximum allowed injection duty cycle, magnitude value of system phase current, minimum injection frequency, allowed voltage ripple and the designed dc voltage value.

6.2.3 Reduced order modeling and design of control

In order to simplify the design of control loops, the reduced order average value modeling approach is adopted for the modeling and small-signal transfer function characterization. The equivalent switching model is reduced to single-phase single-module SVI converter as shown in Figure 6-5. The voltage compensator $C_{vcf}(s)$ and current compensator $C_{ilf}(s)$ are designed as proportional compensators with high frequency poles.

$$C_{vcf}(s) = \frac{k_{pvcf}}{\left(1 + \frac{s}{\omega_{pvcf}}\right)} = \frac{2\pi f_{bwvcf} C_{fest}}{\left(1 + \frac{s}{\omega_{pvcf}}\right)} \qquad 6\text{–}23$$

$$C_{ilf}(s) = \frac{k_{pilf}}{\left(1 + \frac{s}{\omega_{pilf}}\right)} = \frac{2\pi f_{bwilf} L_{fest}}{\left(1 + \frac{s}{\omega_{pilf}}\right)} \qquad 6\text{–}24$$

The proportional gains k_{pvcf} in the voltage controller $C_{vcf}(s)$ is set with two parameters, the desired bandwidth f_{bwvcf} of the control and capacitance estimation C_{fest}. Accordingly, the proportional gain k_{pilf} of the current controller $C_{ilf}(s)$ is set with two similar parameters, the desired current control bandwidth f_{bwilf} and inductance estimation L_{fest}. In this way the programming of the current and voltage control is performed in an automated manner. The two high frequency poles

ω_{pvcf} and ω_{pilf} are set higher than the corresponding controller bandwidths, providing the additional attenuation in the high frequency range.

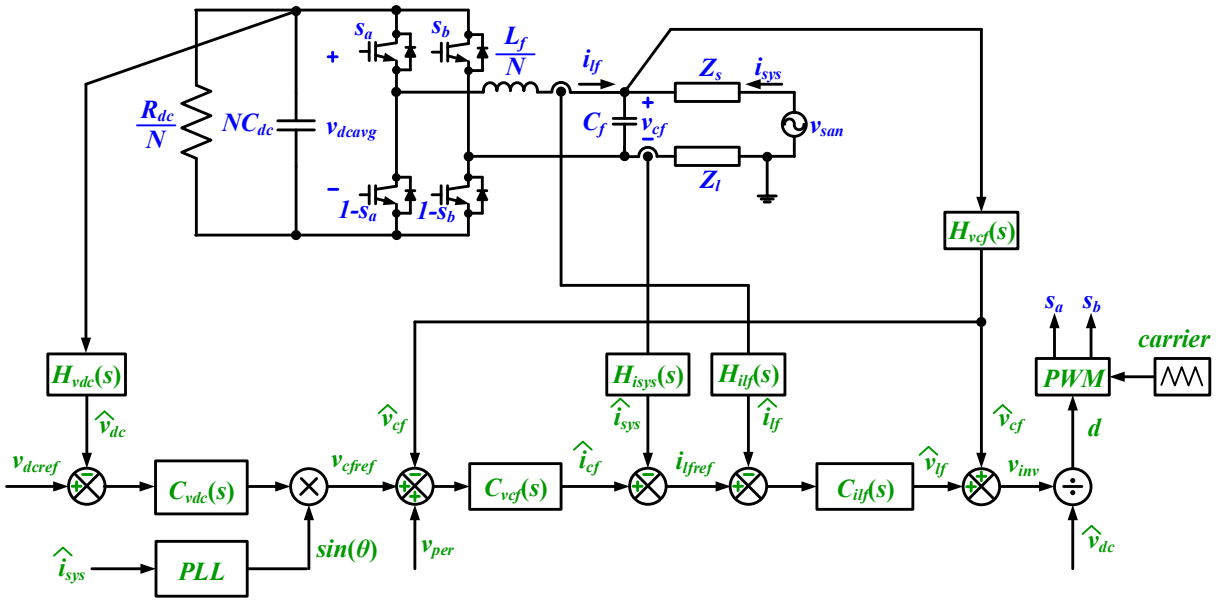


Figure 6-5: The equivalent reduced order single-module model of SVI converter

The equivalent transfer function diagram of converter, obtained with reduced order modeling is shown in Figure 6-6. The current loop gain can be directly derived from the equivalent transfer function diagram.

$$i_{lf}(s) = \frac{1}{Z_{lf}(s)}\left(v_{inv}(s) - v_{cf}(s)\right) \qquad 6\text{–}25$$

$$v_{inv} = \frac{\left(i_{lfref}(s) - H_{ilf}(s)i_{lf}(s)\right)C_{silf}(s) + H_{vcf}(s)v_{cf}(s)}{H_{vdc}(s)}G_{delay}(s) \qquad 6\text{–}26$$

Where the delay function due to DSP implementation and digital delay of modulator is approximated with the second order Pade's expression.

$$G_{delay}(s) = e^{-sT_d} \approx \frac{1 - \frac{sT_d}{2} + \frac{(sT_d)^2}{12}}{1 + \frac{sT_d}{2} + \frac{(sT_d)^2}{12}}, T_d = 1.5T_{sw} \qquad 6\text{–}27$$

The generated inductor current $i_{lf}(t)$ depends on the inductor current reference as well as on the capacitor voltage $v_{cf}(t)$, whose influence cannot be attenuated completely.

$$i_{lf}(s) = i_{lfref}(s)G_{clilf1}(s) + v_{cf}(s)G_{clilf2}(s) \qquad 6\text{–}28$$

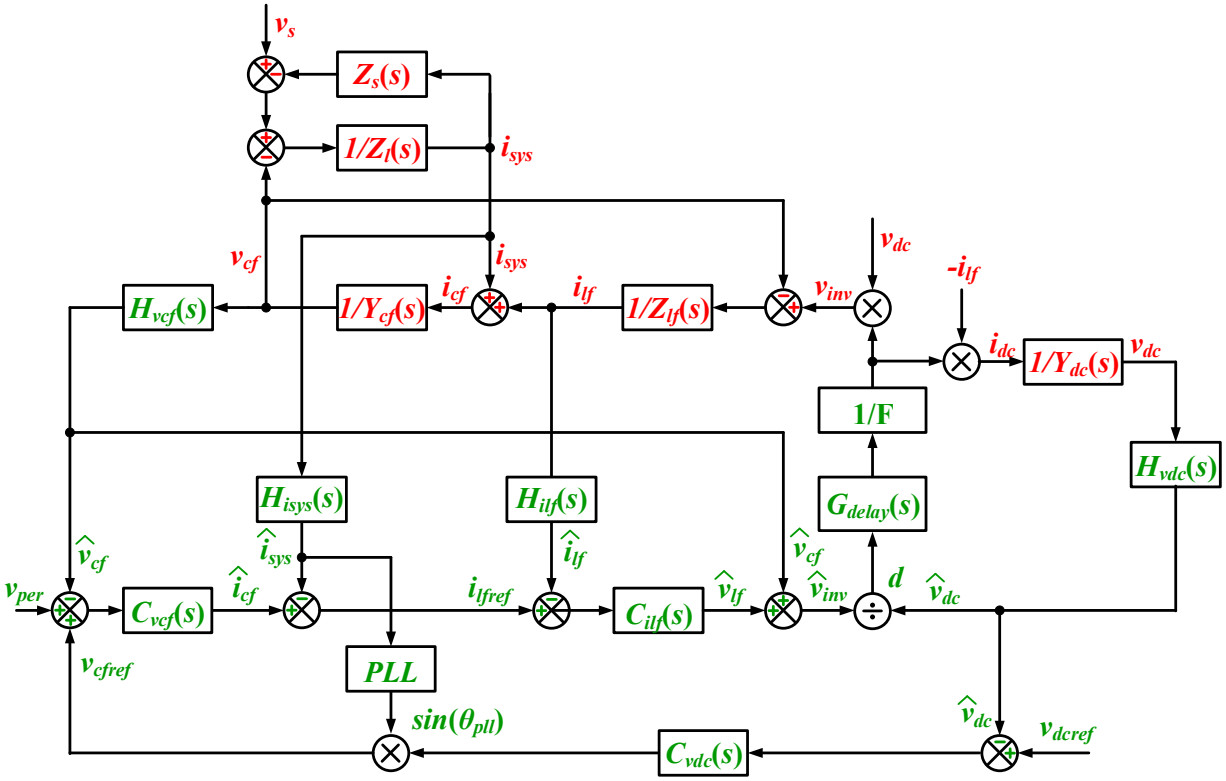


Figure 6-6: The block transfer function diagram of the reduced order model of SVI converter

Due to the decoupling control, the closed loop relationship for inductor current $i_{lf}(s)$ has two inputs, reference $i_{lfref}(s)$ and unwanted capacitor voltage $v_{cf}(s)$. The closed loop transfer function $G_{clilf1}(s)$ should have unity gain in the whole frequency range, ensuring accurate tracking of the current reference. On the other hand, the closed loop transfer function $G_{clilf2}(s)$ should have high attenuation in the whole frequency range, rejecting unwanted dynamic propagating from the capacitor voltage $v_{cf}(t)$ and providing effective decoupling between outer voltage and inner current loops. However, mainly due to the digital implementation of the controller, perfect decoupling is not possible because of the influence of corresponding digital delays in DSP and in the digital modulator.

$$G_{clilf1}(s) = \frac{\dfrac{1}{Z_{lf}(s)}\dfrac{C_{silf}(s)G_{delay}(s)}{H_{vdc}(s)}}{1 + \dfrac{1}{Z_{lf}(s)}\dfrac{H_{ilf}(s)C_{silf}(s)}{H_{vdc}(s)}G_{delay}(s)} \qquad 6\text{–}29$$

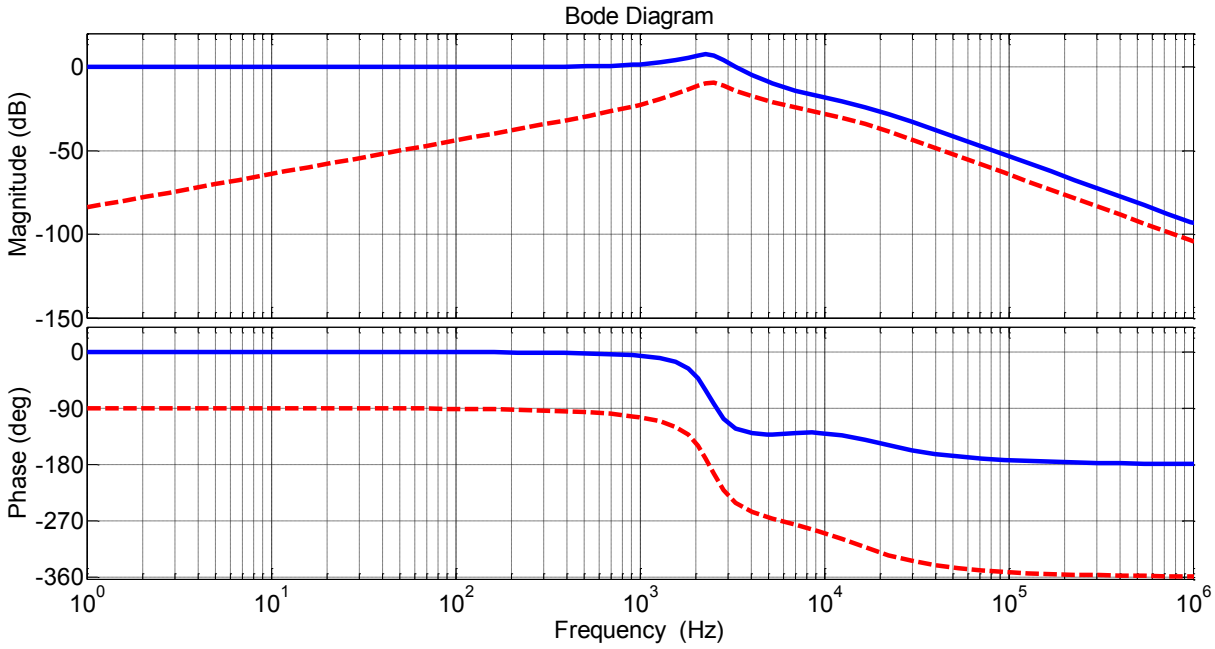


Figure 6-7: Bode diagrams of the closed loop transfer function (a) $G_{clifl1}(s)$ (straight blue line) (b) $G_{clilf2}(s)$ (dashed red line)

$$G_{clilf2}(s)=\frac{\frac{1}{Z_{lf}(s)}\left(\frac{H_{vcf}(s)G_{delay}}{H_{vdc}(s)}-1\right)}{1+\frac{1}{Z_{lf}(s)}\frac{H_{ilf}(s)C_{silf}(s)}{H_{vdc}(s)}G_{delay}(s)} \qquad 6\text{–}30$$

The bode plots of closed current loop transfer functions $G_{clilf1}(s)$ and $G_{clilf2}(s)$ are shown in Figure 6-7. As predicted current loop ensures accurate tracking of the current reference $i_{ref}(t)$ up to 3 kHz. Furthermore, the rejection of disturbances coming from the voltage $v_{cf}(t)$ is very high in the low frequency range and the rejection gain is being decreased as frequency is increasing. The lowest rejection gain is -10 dB, which occurs around 2 kHz. The current loop gain transfer function is identified from the previous two expression as written below.

$$T_{ilf}(s)=\frac{1}{Z_{lf}(s)}\frac{H_{ilf}(s)C_{silf}(s)}{H_{vdc}(s)}G_{delay}(s) \qquad 6\text{–}31$$

The bandwidth of the designed current loop gain transfer function is 1.8 kHz with phase margin around 30 degrees as shown in Figure 6-8. The voltage loop gain transfer function is derived similarly to current loop gain transfer function using transfer function diagram of the equivalent reduced order converter.

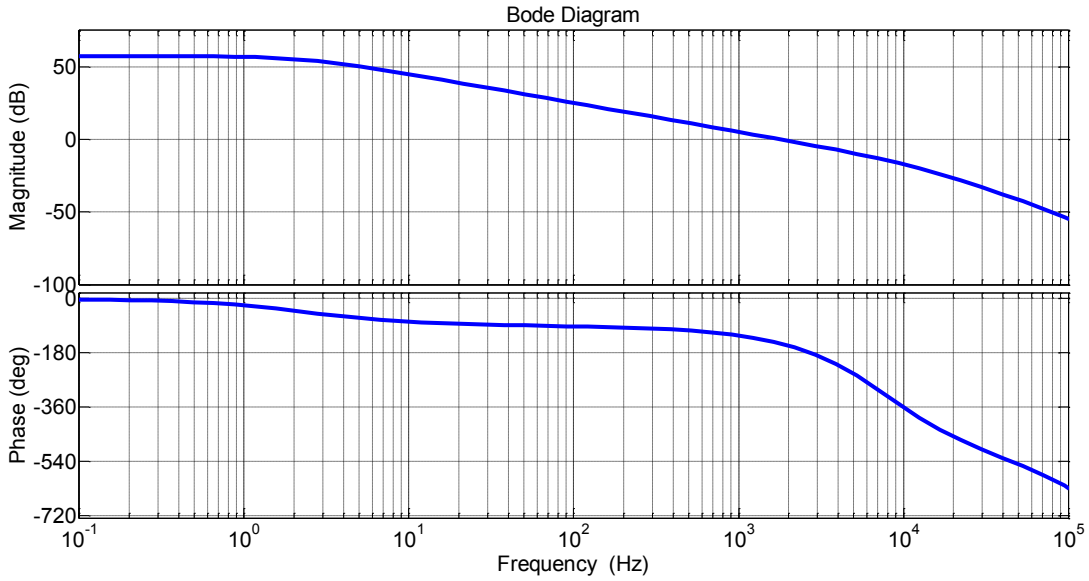


Figure 6-8: Bode diagram of the current loop gain transfer function $T_{ilf}(s)$

$$v_{cf}(s)=\frac{1}{Y_{cf}(s)}\left(i_{lf}(s)+i_{sys}(s)\right) \qquad 6\text{–}32$$

$$\left(v_{cfref}(s)-H_{vcf}(s)v_{cf}(s)\right)C_{svcf}(s)-H_{isys}(s)i_{sys}(s)=i_{lfref}(s) \qquad 6\text{–}33$$

$$v_{cf}(s)=G_{clvcf1}(s)v_{cfref}(s)+G_{clvcf2}(s)i_{sys}(s) \qquad 6\text{–}34$$

The closed voltage loop transfer function $G_{clvcf1}(s)$ should provide accurate tracking of voltage reference $v_{ref}(t)=v_{cref}(t)+v_{per}(t)$, in the whole injection frequency range of interest. The second closed voltage loop transfer function $G_{clvcf2}(s)$ should reject disturbances coming from the system via the system current $i_{sys}(t)$. The both transfer functions are derived using the previous three expressions and are given below

$$G_{clvcf1}(s)=\frac{\frac{1}{Y_{cf}(s)}G_{clilf1}(s)C_{svcf}(s)}{1+\frac{1}{Y_{cf}(s)}\left(G_{clilf1}(s)H_{vcf}(s)C_{svcf}(s)-G_{clilf2}(s)\right)} \qquad 6\text{–}35$$

$$G_{clvcf2}(s)=\frac{\frac{1}{Y_{cf}(s)}\left(1-G_{clilf1}(s)H_{isys}(s)\right)}{1+\frac{1}{Y_{cf}(s)}\left(G_{clilf1}(s)H_{vcf}(s)C_{svcf}(s)-G_{clilf2}(s)\right)} \qquad 6\text{–}36$$

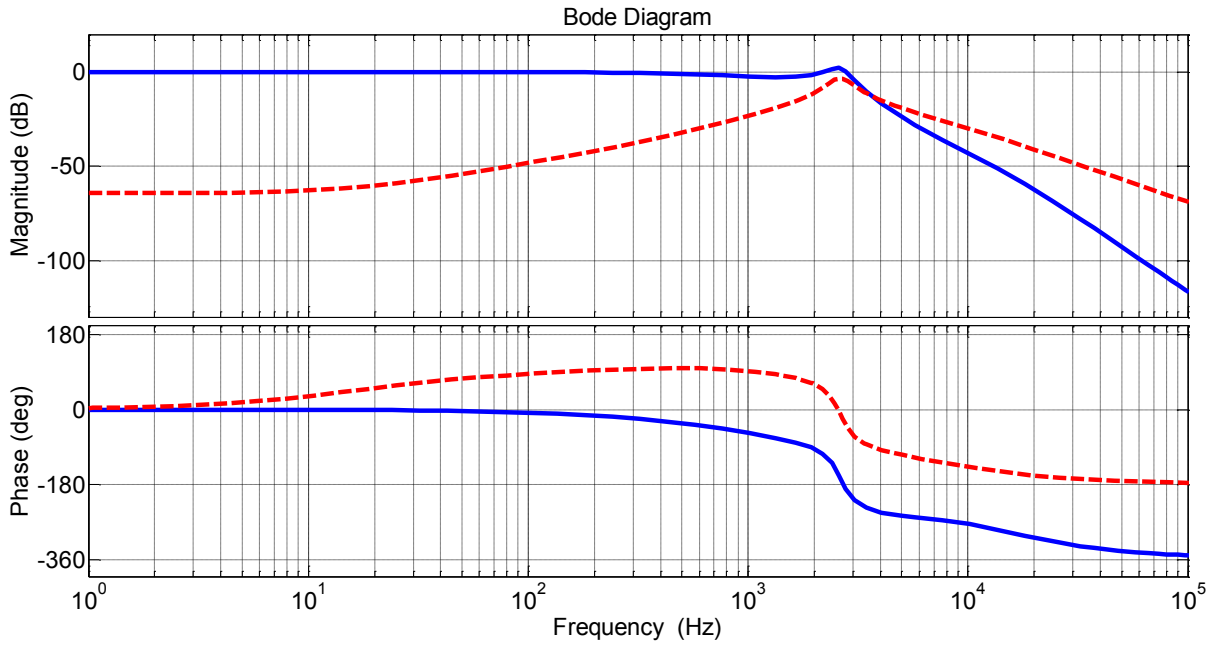


Figure 6-9: Bode diagrams of the closed loop transfer function (a) $G_{clvcf1}(s)$ (straight blue line) (b) $G_{clvcf2}(s)$ (dashed red line)

The designed voltage control is capable of tracking voltage reference signals in the wide frequency range as predicted by the bode diagram of transfer functions $G_{clvcf1}(s)$, which is shown in Figure 6-9. On the other hand, the rejection of the disturbances coming from the system is achieved with a reasonable high attenuation in the low frequency range, while in the frequency range close to the voltage loop bandwidth, attenuation of disturbances is low, as shown in the bode diagram of $G_{clvcf2}(s)$ in Figure 6-9. The main reasons of lower attenuation in the high frequency range are computational delays due to the digital implementation of the proposed decoupling control. If a higher rejection of system disturbances is necessary, then a lower bandwidth control can be used just by adjusting two proportional gains in the corresponding current and voltage controllers.

$$T_{vcf}(s) = \frac{1}{Y_{cf}(s)}\left(G_{clilf1}(s)H_{vcf}(s)C_{svcf}(s) - G_{clilf2}(s)\right) \qquad 6\text{–}37$$

Although, the designed bandwidth of voltage loop should be around 1 kHz, due to the non-perfect decoupling it is actually almost 2 kHz as shown in Figure 6-10. The phase margin is also 25 degrees, which is lower than expected 45 degrees. The derived expressions for both current and voltage loop gains provide a detailed insight into the properties of loops. Furthermore, both ac

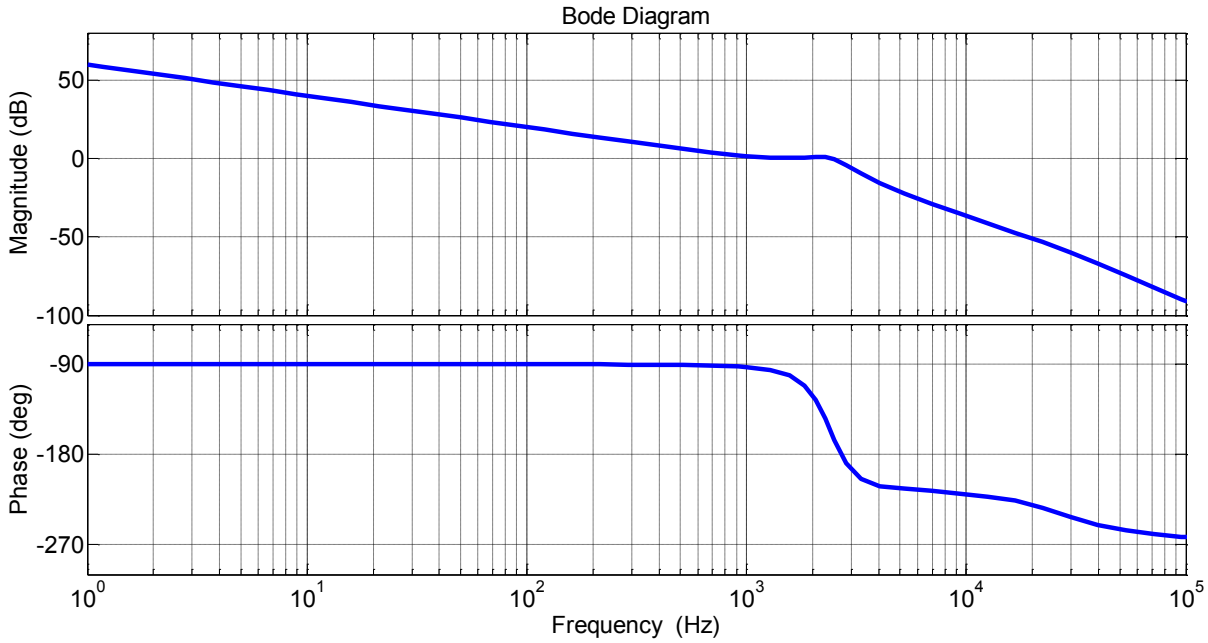


Figure 6-10: Bode diagram of the voltage loop gain transfer function $T_{vcf}(s)$

control loops are designed to have as high as possible frequency bandwidths with low phase margins, providing the capability to generate voltage perturbation signals up to 2 kHz.

6.2.4 Design of dc voltage loop and voltage balancing

The dc voltage loop is designed with the use of power balance principle, stating that active power delivered via series capacitor should maintain desired voltage by covering the losses of interleaved SVI converter and delivering power to the dc side. Therefore, the proposed controller is aligned via phase locked loop with the phase component of system current $i_{sys}(t)$. In this manner, controller ensures that line frequency component of injection voltage will be just small enough to cover the power losses of the injection converter.

$$V_{cfrms} I_{srcrms} = V_{dc} I_{dc} \tag{6–38}$$

$$G_{vdcv}(s) = \frac{\tilde{v}_{dc}(s)}{\tilde{v}_{cfm}(s)} = \frac{I_{srcrms}}{2\sqrt{2}V_{dc}} Z_{dc}(s) \tag{6–39}$$

$$Z_{dc}(s) = \frac{1}{sNC_{dc}} \| \frac{R_{dc}}{N} = \frac{R_{dc}}{N + NsR_{dc}C_{dc}} \tag{6–40}$$

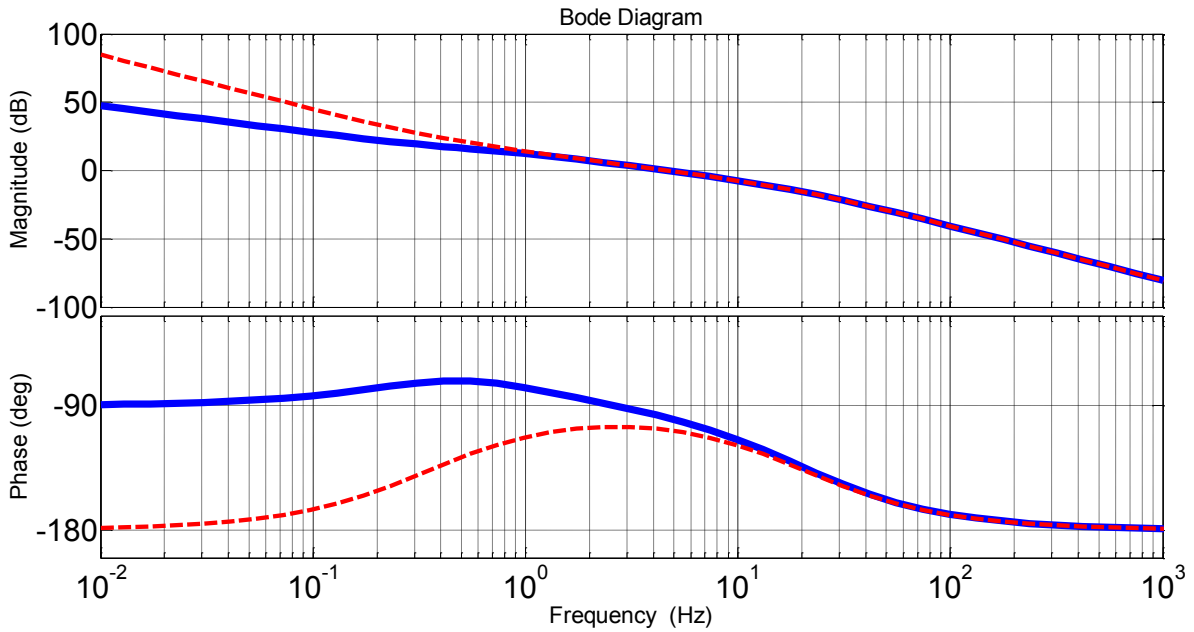


Figure 6-11: Bode diagram of dc the voltage loop gain transfer function $T_{vdc}(s)$: (a) With R_{dc}=1 kΩ (straight blue line) (b) Without dc resistors (dashed red line)

$$C_{vdc}(s) = \frac{k_{idc}}{s} \frac{\left(1 + \frac{s}{\omega_{zvdc}}\right)}{\left(1 + \frac{s}{\omega_{pvdc}}\right)} \qquad 6\text{–}41$$

$$T_{vdc}(s) = C_{vdc}(s) G_{vdcv}(s) \qquad 6\text{–}42$$

After the linearization of the power balance equation, series voltage injection magnitude to dc voltage plant transfer function can be derived and used to design dc voltage loop. Therefore, a dc voltage compensator with an integrator, zero and pole is designed and used to regulate dc voltage. The dc voltage loop has low bandwidth of 4 Hz and phase margin of 60 degrees as shown in Figure 6-11.

The voltage balancing control is designed to have approximately same bandwidth as the dc voltage loop. However, the control is tuned by running extensive simulations and observing settling time of the responses. The voltage balancing control bandwidth depends on the mismatch of the modules and it is not predictable. Therefore, the used voltage balancing control consists of proportional gain controllers, as it provides robust and accurate balancing of capacitor voltages. In this way, the effective balancing of capacitor voltages is achieved.

6.3 Validation of SVI Converter Design in Simulations

The equivalent switching simulation model of the interleaved single-phase SVI converter is built and extensively tested in MATLAB/Simulink software with the use of SimPowerSystems toolbox. The software environment is used to simulate switching model of SVI converter, which includes the dead-time, digital implementation of the proposed decoupling control, one sample delay due to DSP implementation. The simulation switching model is used to characterize the properties of the injected signal, verifying control loop design and selection of inductor and capacitor values. In order to cover the operation of SVI converter, several operating points are simulated and obtained simulation results are presented in this section. Furthermore, the model is extensively tested using different loads typically found in three phase power systems, showing robustness with pure reactive, active or controlled and nonlinear passive loads.

6.3.1 Simulation waveforms in the steady-state operating point

The simulation waveforms of SVI converter when it operates in steady state are shown and explained in this section. In this operating point the converter is charged and ready to perturb the three-phase ac system. Steady-state simulation waveforms of inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$ and i_{lf3}(t), capacitor voltage $v_{cf}(t)$ and corresponding references $i_{ref}(t)$ and $v_{ref}(t)$ are shown in Figure 6-12. The generated inductor currents accurately follow the current reference as depicted in the

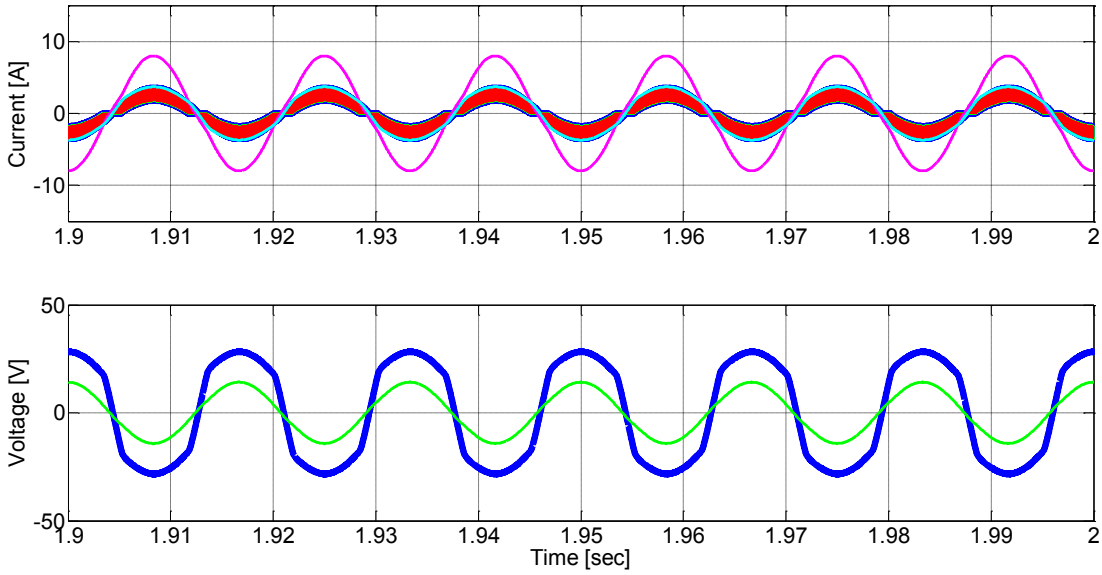


Figure 6-12: Steady state simulation waveforms: (top) Inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$, reference current $i_{ref}(t)$ and system current $-i_{sys}(t)$ (bottom) injection voltage $v_{cf}(t)$ and reference voltage $v_{ref}(t)$

figure. Furthermore, the current sharing among modules is achieved and all the three currents conduct one third of the system current, resulting in the reduced current stress of each H-bridge module. The inserted capacitor voltage $v_{cf}(t)$ accurately follows a line frequency reference, but due to the dead-time implementation, the generated capacitor voltage has additional line frequency harmonics.

In addition, Figure 6-13 shows the steady-state waveforms of capacitor voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and $v_{dc3}(t)$ together with the dc voltage reference $v_{dcref}(t)$ in the top graph. The proposed decoupling control provides equivalent energy sharing among modules as each dc capacitor stores same dc and ripple voltage. In this way, the faster devices with lower voltage rating are used in each H-bridge module, resulting in the generation of cleaner injection signal together. The bottom graph of Figure 6-13 shows the duty cycles $d_1(t)$, $d_2(t)$ and $d_3(t)$, which are applied in the modulation of each H-bridge module. Again due to the symmetry and proposed decoupling control all the three duty cycles are same, providing equal voltage and current stress to H-bridges.

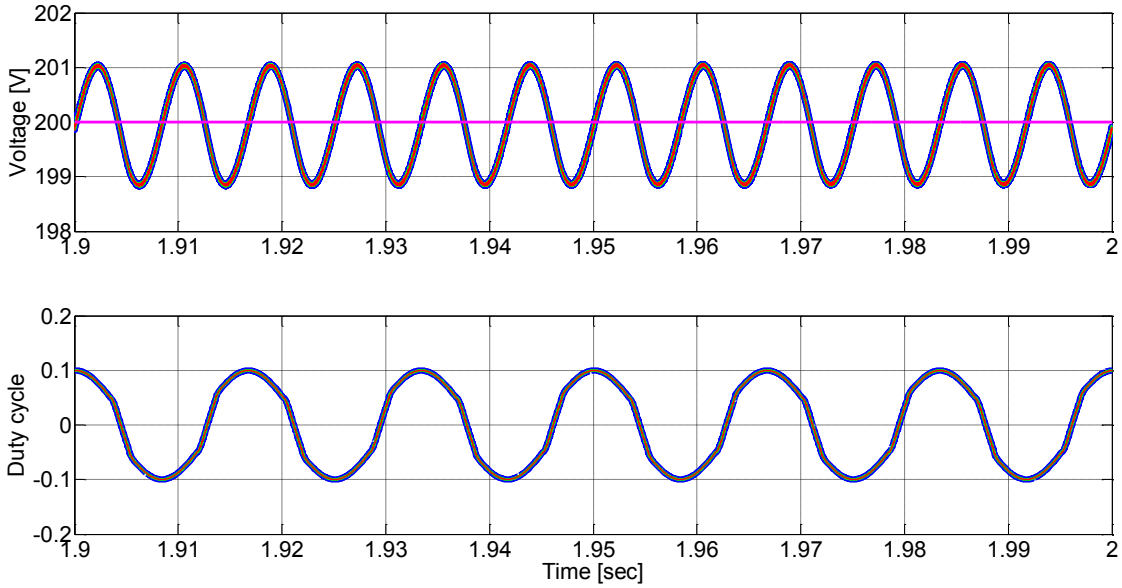


Figure 6-13: Steady state simulation waveforms: (top) dc voltages v_{dc1}(t), v_{dc2}(t) v_{dc3}(t) and dc reference voltage v_{dcref}(t) (bottom) H-bridge duty cycles d_1(t), d_2(t) and d_3(t)

Harmonic content of the capacitor injection voltage $v_{cf}(t)$ is shown in Figure 6-14. Beside the dominant line frequency component, there are significant third, fifth and seventh harmonics of the line frequency present in the capacitor voltage waveform. Due to the interleaved operation of the

converter, the switching harmonics present in the capacitor injection voltage $v_{cf}(t)$ are multiples of 60kHz.

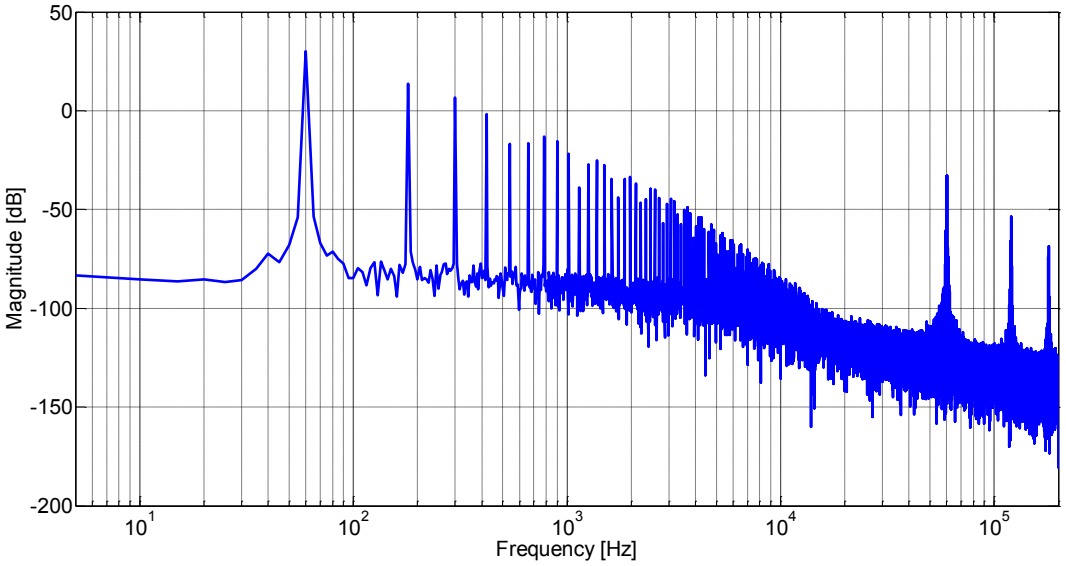


Figure 6-14: Harmonic spectrum of the capacitor injection voltage $v_{cf}(t)$

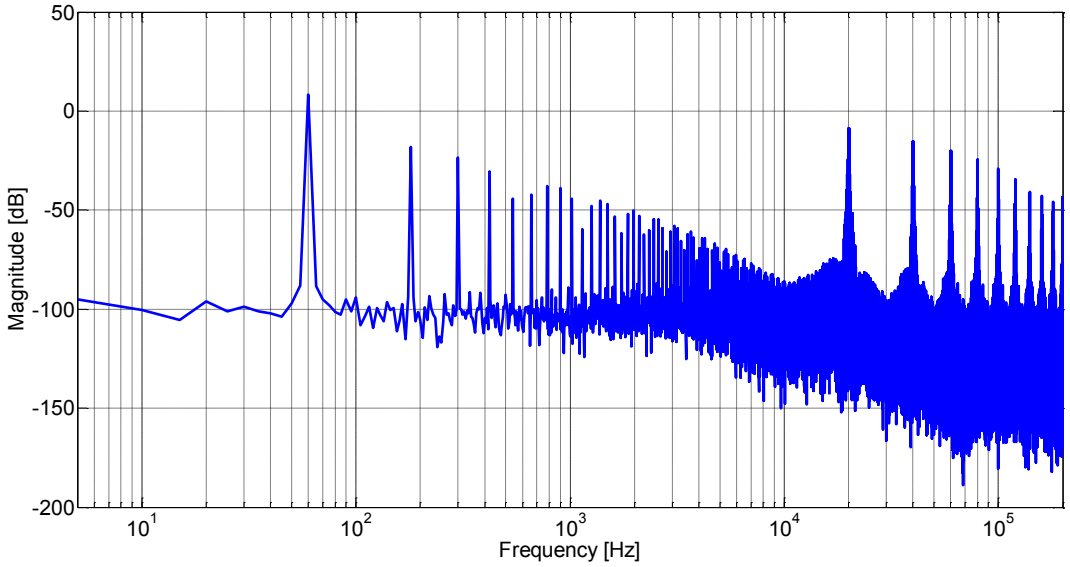


Figure 6-15: Harmonic spectrum of the inductor current $i_{lf1}(t)$

Spectrum content of the simulation waveform of inductor current $i_{lf1}(t)$ is shown in the Figure 6-15. The dominant line frequency component at 60 Hz of inductor current represents one third of the system current, which is equally shared among H-bridge modules. Beside the line frequency component, unwanted harmonics of the line frequency are present in the spectrum due to the dead-time implementation in the gate signals. The inherently generated switching harmonics (multiples of 20 kHz) are also present in the simulation waveform.

6.3.2 Steady-state simulation waveforms during the injection of low frequency sinusoidal signal

The first simulated operating point investigates waveforms of SVI converter when the sinusoidal signal with frequency close to line frequency (80 Hz) is being injected into the three-phase system. This operating point corresponds to 20 Hz injection in dq coordinates, yielding a low frequency voltage ripple of 20 Hz in dc capacitor voltages. The steady-state simulation waveforms of inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$ and i_{lf3}(t), capacitor voltage $v_{cf}(t)$ and corresponding references $i_{ref}(t)$ and $v_{ref}(t)$ are shown in Figure 6-16. The generated inductor currents accurately follow the current reference as depicted in the figure. Furthermore, the current sharing among modules is achieved and all the three currents conduct one third of the system current and one third of the injection inductor current, which is beneficial to each H-bridge module as current stress is reduced. The inserted capacitor voltage $v_{cf}(t)$ accurately follows a line frequency reference and the injection frequency reference, but due to the dead-time implementation, the generated capacitor voltage has additional harmonics.

$$f_{harmonics} = nf_{line} \pm mf_{inj} \qquad 6\text{–}43$$

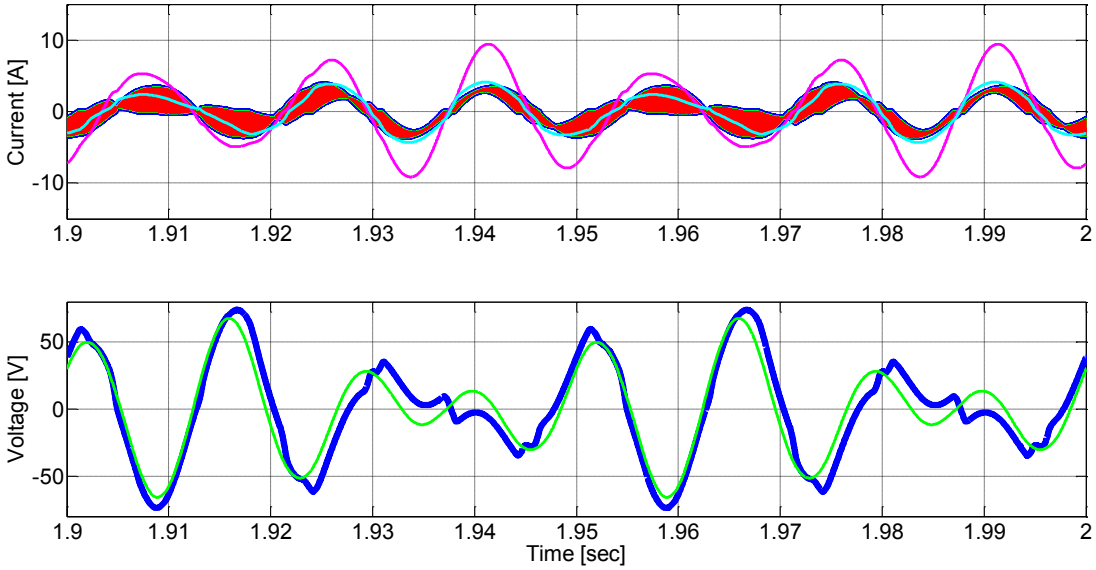


Figure 6-16: Steady state simulation waveforms: (top) Inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$, reference current $i_{ref}(t)$ and system current $-i_{sys}(t)$ (bottom) injection voltage $v_{cf}(t)$ and reference voltage $v_{ref}(t)$

Moreover, Figure 6-17 shows the steady-state waveforms of capacitor voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and $v_{dc3}(t)$ together with the dc voltage reference $v_{dcref}(t)$ in the top graph. The proposed decoupling

control provides equivalent energy sharing of injection ripple, twice the line frequency ripple and dc voltages. The bottom graph of Figure 6-17 shows the duty cycles $d_1(t)$, $d_2(t)$ and $d_3(t)$, which are applied in the modulation of each H-bridge module. Again due to the symmetry all the three duty cycles are same, providing equal voltage and current stress to H-bridges.

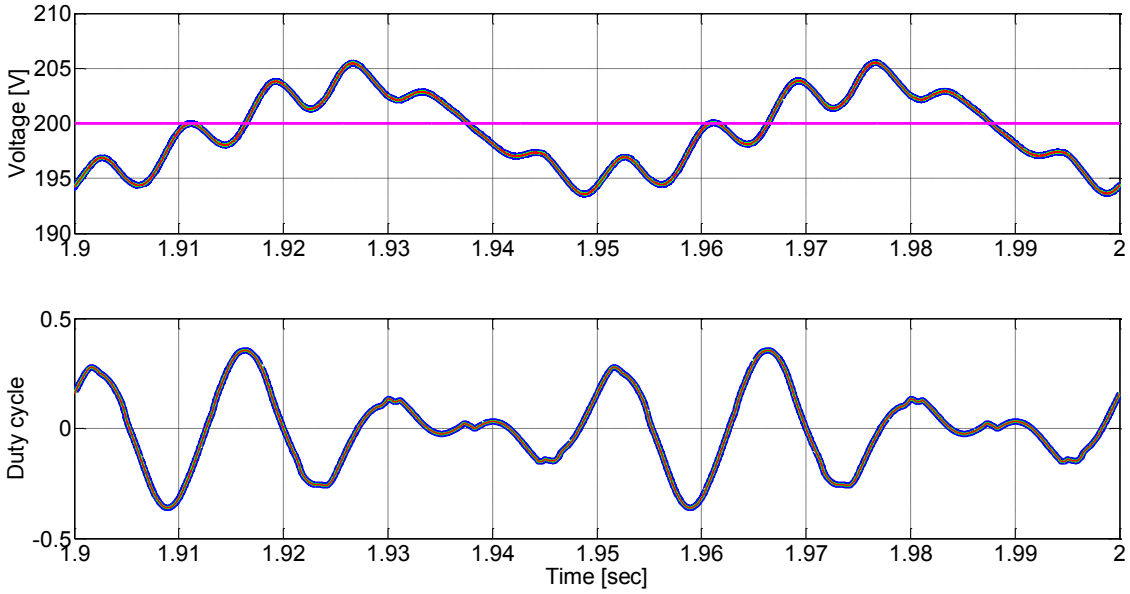


Figure 6-17: Steady state simulation waveforms: (top) dc voltages v_{dc1}(t), v_{dc2}(t) v_{dc3}(t) and dc reference voltage $v_{dcref}(t)$ (bottom) H-bridge duty cycles d_1(t), d_2(t) and d_3(t)

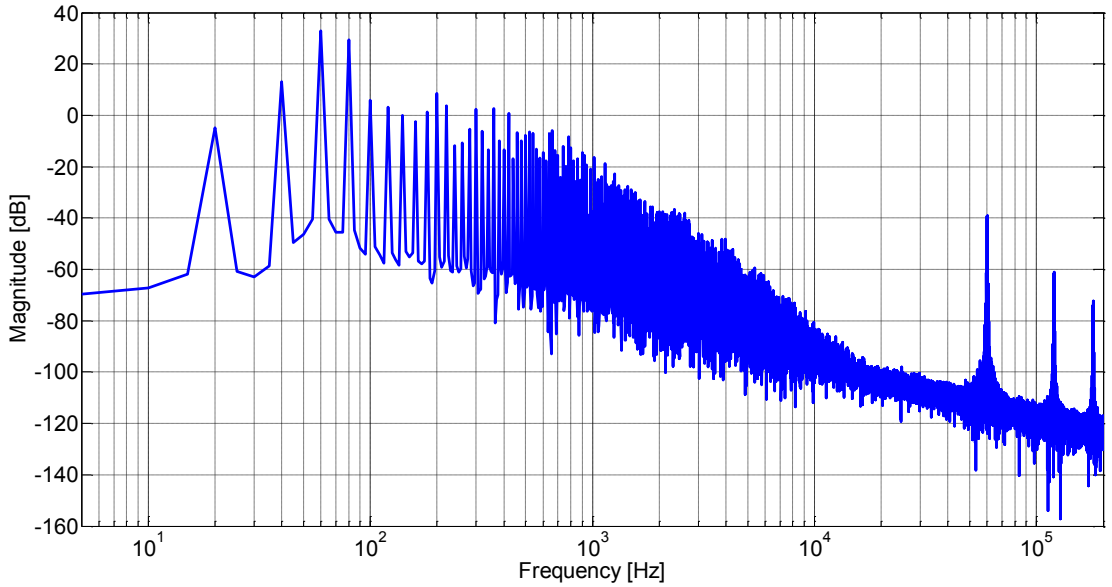


Figure 6-18: Harmonic spectrum of the capacitor injection voltage $v_{cf}(t)$

Harmonic content of the capacitor injection voltage $v_{cf}(t)$ is shown in Figure 6-18. Beside the dominant line frequency and its harmonic components, there is obviously the injection frequency

component. In addition, there are cross modulation harmonics generated as well. Still, the dominant switching harmonics in the generated voltage are multiples of 60 kHz.

Spectrum content of the simulation waveform of inductor current $i_{lf1}(t)$ is shown in the Figure 6-19. Beside the injection frequency component, the line frequency harmonics and cross product harmonics are present in the spectrum of the inductor current. The switching harmonics (multiples of 20 kHz) are also present in the generated spectrum.

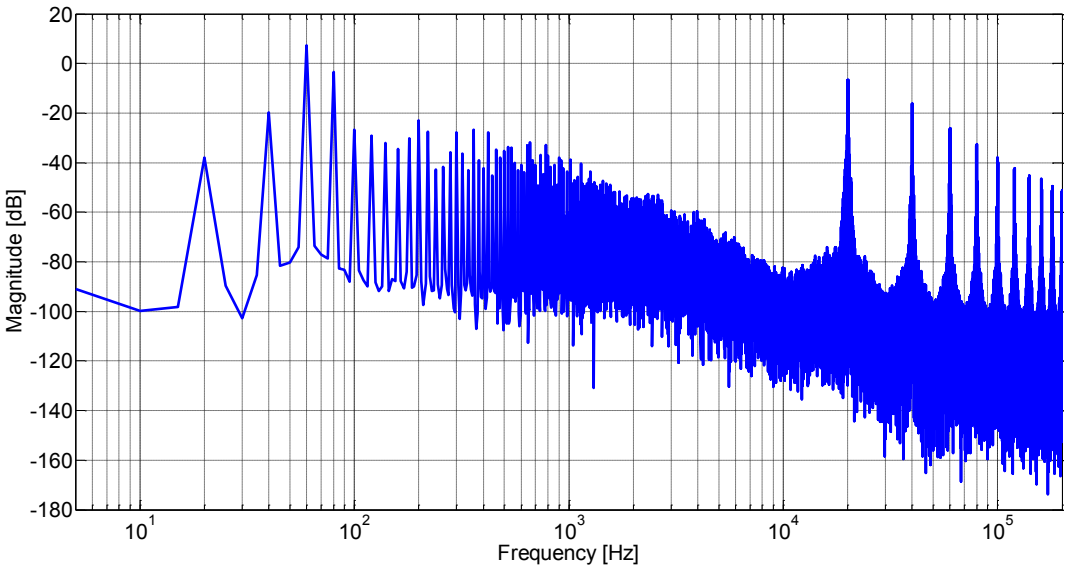


Figure 6-19: Harmonic spectrum of the inductor current $i_{lf1}(t)$

6.3.3 Steady-state simulation waveforms during the injection of high frequency sinusoidal signal

Another critical operating point is a high frequency injection with maximum magnitude, when it is necessary to provide high enough voltage across filter inductors L_{fi} (i= 1, 2, 3) to generate a current to charge a series injection capacitor C_f. Simulation waveforms of interleaved SVI converter that injects 800 Hz sinusoidal signal in series with a power system supplying a pure resistive load are presented in this section.

The steady-state simulation waveforms of inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$ and i_{lf3}(t), capacitor voltage $v_{cf}(t)$ and corresponding references $i_{ref}(t)$ and $v_{ref}(t)$ are shown in Figure 6-20. The generated inductor currents accurately follow the high frequency current reference. Furthermore, the current sharing among modules is achieved and all the three currents conduct one third of the system current and one third of the injection inductor current, allowing the lower dc voltage to be used in

each H-bridge module. The inserted capacitor voltage $v_{cf}(t)$ accurately follows a line frequency reference and the injection high frequency reference.

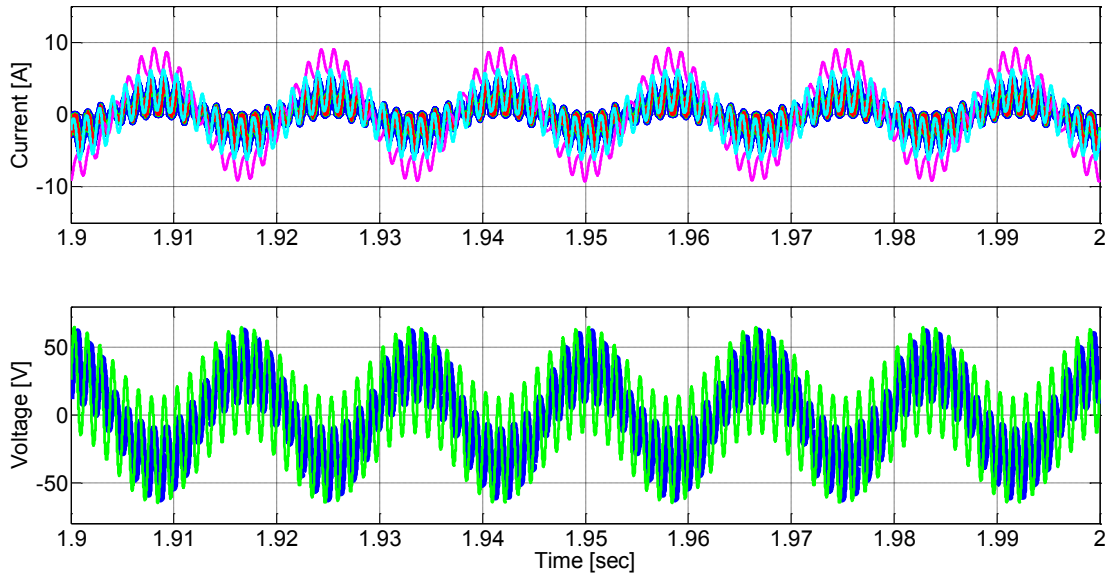


Figure 6-20: Steady state simulation waveforms for high frequency (800 Hz) injection: (top) Inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$, reference current $i_{ref}(t)$ and system current $-i_{sys}(t)$ (bottom) injection voltage $v_{cf}(t)$ and reference voltage $v_{ref}(t)$

Moreover, Figure 6-21 shows the steady-state waveforms of capacitor voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and $v_{dc3}(t)$ together with the dc voltage reference $v_{dcref}(t)$ in the top graph. The proposed decoupling control provides equivalent energy sharing of high frequency injection ripple, twice the line

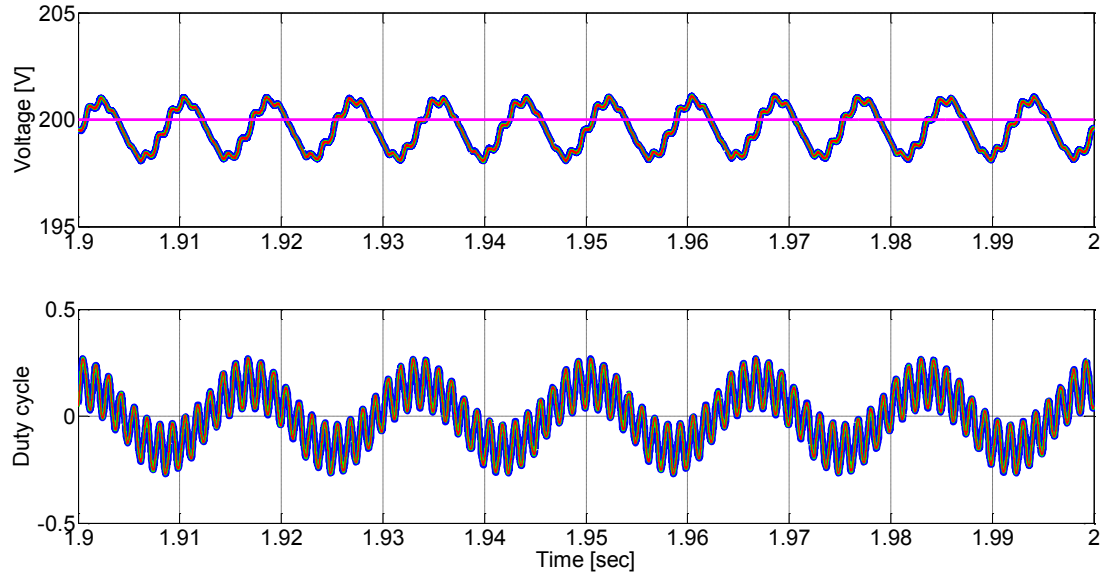


Figure 6-21: Steady state simulation waveforms for high frequency (800Hz) injection: (top) dc voltages v_{dc1}(t), v_{dc2}(t) v_{dc3}(t) and dc reference voltage $v_{dcref}(t)$ (bottom) H-bridge duty cycles d_1(t), d_2(t) and d_3(t)

frequency ripple and dc voltages. The bottom graph of Figure 6-21 shows the duty cycles $d_1(t)$, $d_2(t)$ and $d_3(t)$, which are applied in the modulation of each H-bridge module. Again due to the symmetry all the three duty cycles are same, providing equal voltage and current stress to H-bridges.

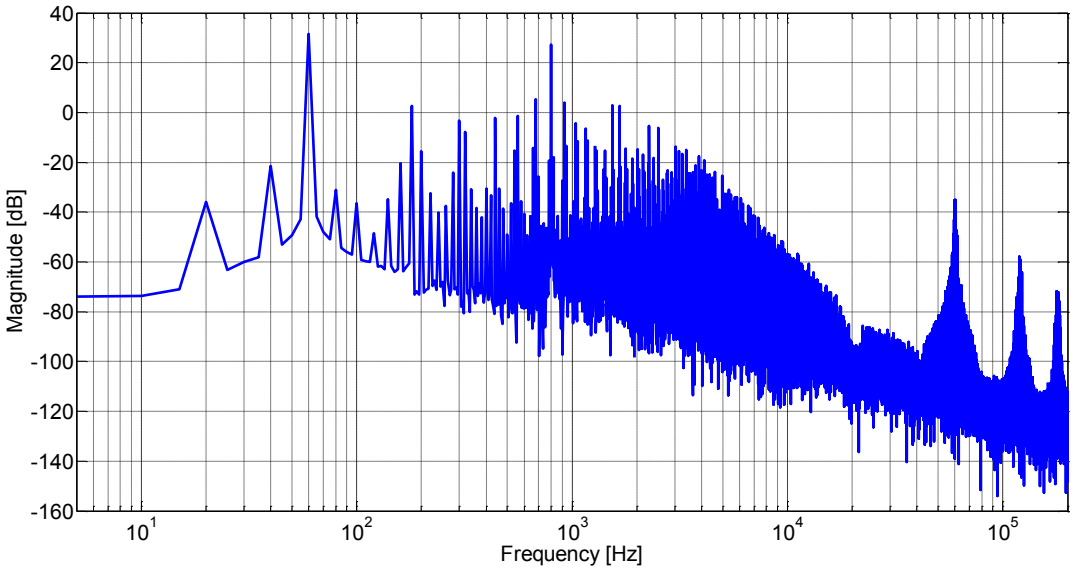


Figure 6-22: Harmonic spectrum of the capacitor injection voltage $v_{cf}(t)$

Harmonic content of the capacitor injection voltage $v_{cf}(t)$ during the high frequency injection is shown in Figure 6-22. The two dominant harmonics are line frequency and the injection frequency components. In addition, there are cross modulation harmonics generated and switching harmonics (multiples of 60 kHz).

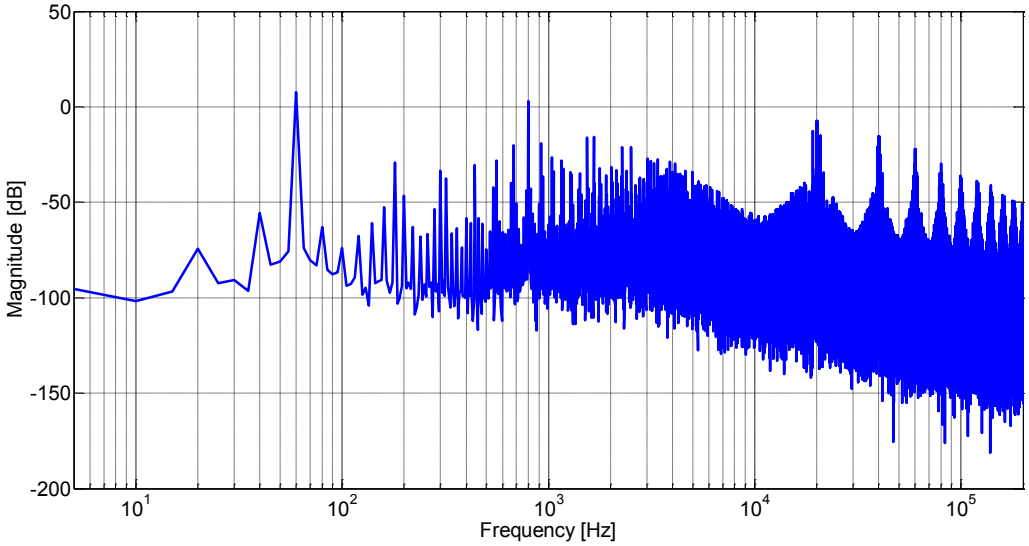


Figure 6-23: Harmonic spectrum of the inductor curretn $i_{lf1}(t)$

Spectrum content of the simulation waveform of inductor current $i_{lf1}(t)$ during the high frequency injection is shown in Figure 6-23. Beside the high frequency injection component, the line frequency harmonics and cross product harmonics are present in the spectrum of the inductor current. The switching harmonics (multiples of 20 kHz) are also present in the generated spectrum.

6.4 Experimental Verification of SVI Converter Design

The experimental set-up includes interleaved three H-bridge modules, control board with DSP controller, analog sensing part and CPLD chip for protection, six ac filter inductors (330 µH), ac filter capacitor (35 µF) inserted in series with system and three dc capacitors (220 µF) with discharging resistors (1 kΩ). Programmable California Instruments source is used as a voltage source to supply line to line RMS voltage of 120 V, 60 Hz to a 9 Ω three-phase resistor load.

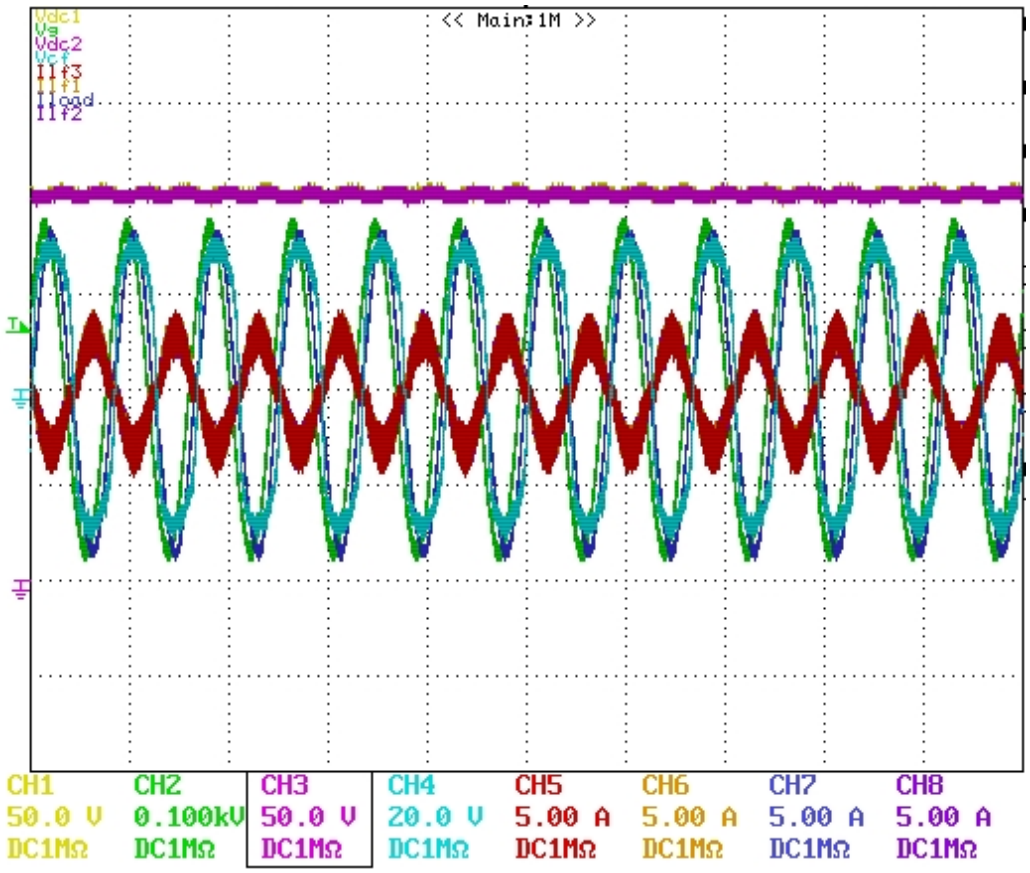


Figure 6-24: Experimental scope waveforms of source voltage $v_s(t)$, load system current $i_{load}(t)$, inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$, $i_{lf3}(t)$, and dc voltages $v_{dc1}(t)$, $v_{dc2}(t)$ and injection voltage $v_{cf}(t)$

Scope experimental waveforms, which are obtained from the described hardware set-up, are shown in Figure 6-24. The scope data show source voltage $v_s(t)$ and load system current $i_{load}(t)$ to be in phase, as expected for a resistive load. In addition, inductor currents $i_{lf1}(t)$, $i_{lf2}(t)$ and $i_{lf3}(t)$ almost equally share the system current $i_{sys}(t)$, which validates proper operation of interleaved H-bridge modules. Furthermore, the inductor currents contain additional switching harmonics at 20 kHz, which are canceled in the converter current $i_{lf}(t)$, providing cleaner current. The injection voltage $v_{cf}(t)$ has the line frequency component (60 Hz) to cover the losses in converter and to maintain dc voltages for each module. Moreover, due to the interleaved operation of the SVI converter the series injected voltage $v_{cf}(t)$ contains switching harmonics which are multiples of the 60kHz. In addition, dc voltage accurately follows 200V voltage reference specified inside DSP code, providing stable operating point for the interleaved single-phase SVI converter.

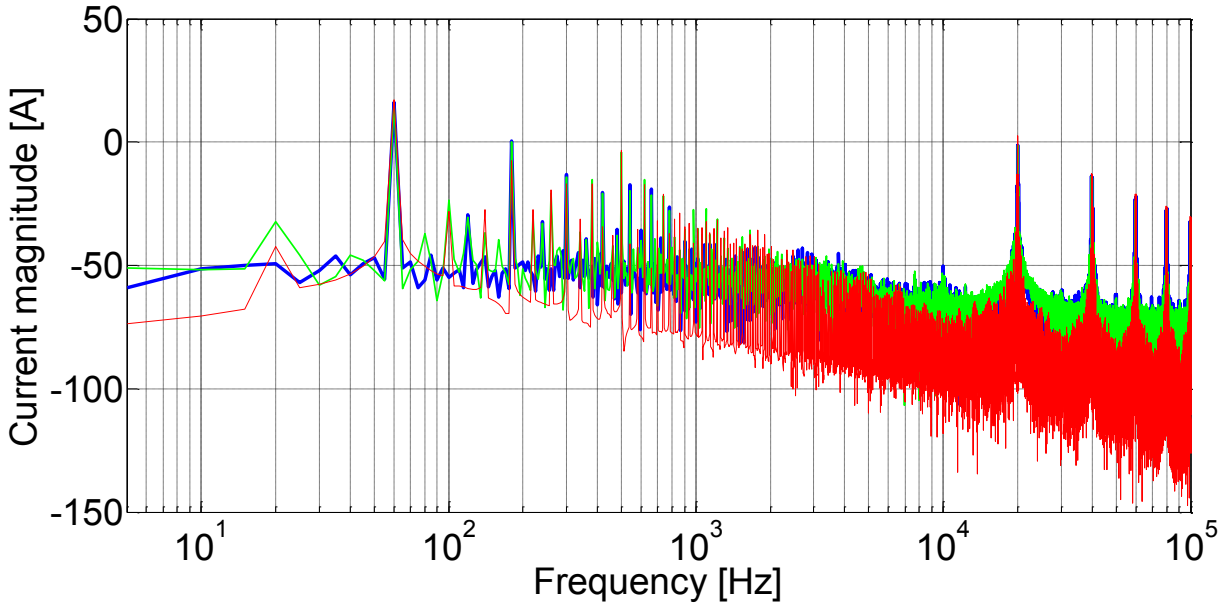


Figure 6-25: Spectrum comparison of inductor current i_{lf1}(t) no injection (blue line), 500 Hz injection (green line) and simulation current waveform (red line).

Spectrum of inductor current $i_{lf1}(t)$ when converter does not inject any signal and when converter injects 500 Hz sinusoidal signal is calculated in MATLAB using scope data and shown in Figure 6-25. On top of that spectrum of inductor current $i_{lf1}(t)$ calculated from the detailed switching simulation model, when 500 Hz sinusoidal signal is being injected, is plotted. As it can be observed, excellent agreement between experimental results and simulations waveforms of the switching simulation model is presented, verifying the effectiveness of proposed interleaved SVI converter.

6.5 Summary

This chapter describes a general design procedure for a single-phase interleaved SVI converter, which is suitable for small-signal dq impedance identification. Special attention is focused on the design of high bandwidth ac current, high bandwidth ac voltage loop and low bandwidth dc voltage loop, providing fast and robust control. The dc voltage loop is designed by a power balance principle and by aligning system frequency reference (60 Hz) of injection voltage with the system current via PLL. Analytical expressions are derived for each critical design step. In addition, the design procedure is completely verified in the simulations using switching model, dead-time, digital controller and one sampling delay due to DSP implementation, proving the effectiveness of decoupling control method. Furthermore, the switching simulation model has been extensively simulated with different loads, including resistive, inductive and capacitive reactive, proving the robustness of proposed decoupling control to the load variations. The interleaved solution provides wider injection range, means to characterize higher current rated systems because of current sharing among modules and enables generation of cleaner injection signal. The used ac side filter is of the second order, minimizing the injection of unwanted switching noise. Even more, the proposed interleaved SVI converter does not require an isolation transformer, resulting in reduced size, weight and cost and is capable of self-charging via dc voltage control. Furthermore, the proposed transformerless solution is capable of injecting low frequency signals in dq coordinates by avoiding transformer saturation problems, resulting in the increased injection frequency range.

Chapter 7. Identification of Small-Signal Impedances via Single-Phase Injection

This chapter describes the identification of small-signal impedances of three-phase ac power systems via the single phase injection. The excitation of the power system under test is realized via single-phase shunt current and series voltage injections, providing precise identification of large and small values of impedances. Hence, single-tone ac sweep FFT algorithm that extracts small-signal impedances from the switching models is implemented and presented in this paper. It is the basic idea for the impedance extraction which is time consuming due to its sweeping nature. Furthermore, frequency analysis is substantially enhanced with the implementation of wide-bandwidth multi-tone and chirp injections, resulting in the faster identification of switching models. Moreover, the proposed extraction algorithm is validated on the detailed switching simulation model of three-phase VSI. In addition, unbalanced single-phase multi-tone injection is proposed to identify small-signal dq impedances as an approach that requires less hardware for the injection implementation. The presented small-signal impedance identification algorithm is general and can be used to obtain small-signal impedances of other power electronics converters.

7.1 Introduction

The single-phase injection can be used to perturb three-phase ac power systems as it creates unbalanced response in all three phases. Furthermore, the unbalanced nature of the single-phase injection dq coordinates as well. In this case a single frequency point injected in single-phase creates two frequency points as responses in dq coordinates. In the case of wide bandwidth signal injection, a single frequency range is being injected into the system via the single-phase, creating unbalanced response in all three phases. A single frequency range creates a response in two frequency ranges around the system frequency in dq coordinates. Nevertheless, it will be shown in this chapter that still it is possible to enhance the impedance identification process by the wide bandwidth injection.

This chapter is organized in the following manner, the second section describes the properties of the single-phase shunt current injection. The pure sinusoidal, chirp and multi-tone injection signals are analyzed and compared. Furthermore, it explains FFT identification algorithm.

The third section investigates the properties of the series voltage injection with regard to all three injection signals. Similarly, FFT identification algorithm for the characterization of the small-signal impedance.

The fourth section provides the small-signal impedance results of three-phase two level converter operating as an inverter and as a rectifier. The fifth section explains the identification algorithm based on the usage of Welch's function as it provides a way to reduce the noise and its unwanted effects. The Welch's algorithm is suitable for the implementation in the impedance measurement unit, which can be used to perform the online characterization of the power systems during the operation. The last section gives summary and conclusions of this chapter.

7.2 Single-Phase Shunt Current Injection

The dq impedances can be obtained via the single-phase injection, which creates unbalanced injection in dq coordinates. The ideal shunt current injection block is shown in Figure 5-1. The first set of injection currents will perturb the power system at a single frequency point that is equal to the sum of system angular frequency and desired injection frequency.

$$\vec{i}_{p1ll}(t)=\begin{bmatrix} i_{p1ab}(t) \\ i_{p1bc}(t) \\ i_{p1ca}(t) \end{bmatrix}=\begin{bmatrix} I_{pm}\cos\left(\omega_p t+\theta_{src}(t)+\varphi_{p1}\right) \\ 0 \\ 0 \end{bmatrix} \qquad 7\text{–}1$$

As mentioned, by injecting a single-frequency point via single phase current, two frequency points are actually being injected in dq coordinates.

$$\vec{i}_{pd1qo}(t)=T_{dqo}(\theta_{src}(t))\vec{i}_{p1ll}(t) \qquad 7\text{–}2$$

$$i_{p1d}(t)=\frac{I_{pm}}{3}\left[\cos\left(2\theta_{src}(t)+\omega_p t+\varphi_{p1}\right)+\cos\left(\omega_p t+\varphi_{p1}\right)\right] \qquad 7\text{–}3$$

$$i_{p1q}(t)=\frac{I_{pm}}{3}\left[-\sin\left(2\theta_{src}(t)+\omega_p t+\varphi_{p1}\right)+\sin\left(\omega_p t+\varphi_{p1}\right)\right] \qquad 7\text{–}4$$

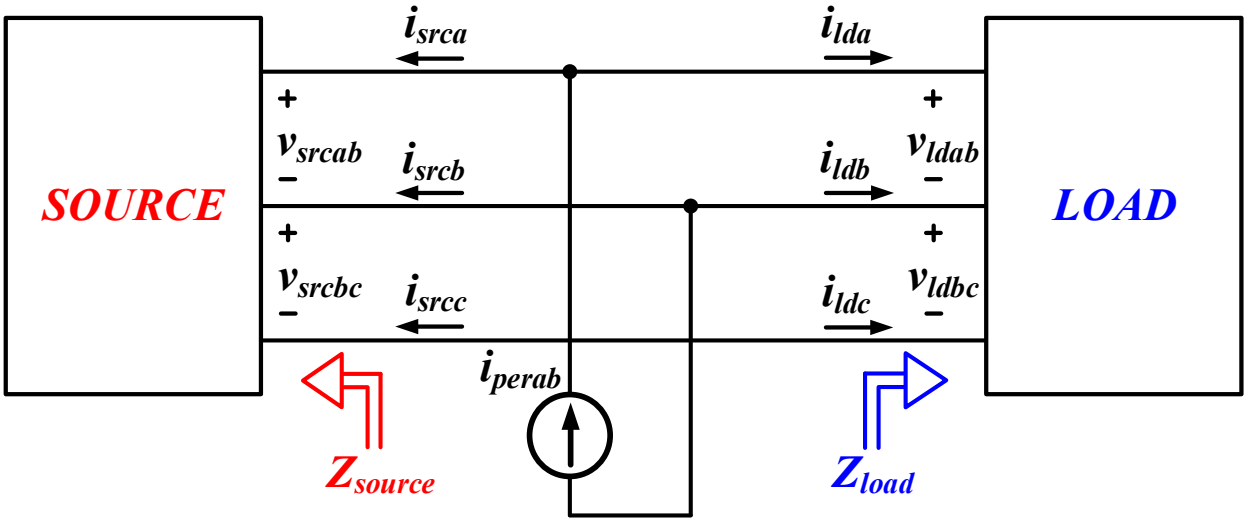


Figure 7-1: Ideal Single-Phase Shunt Current Injection

Complementary, the second set of perturbation currents will inject a single frequency point, which is obtained by subtracting the source angular frequency from the perturbation angular frequency ω_p.

$$\vec{i}_{p2ll}(t)=\begin{bmatrix} i_{p2ab}(t) \\ i_{p2bc}(t) \\ i_{p2ca}(t) \end{bmatrix}=\begin{bmatrix} I_{pm}\cos\left(-\theta_{src}(t)+\omega_p t+\varphi_{p2}\right) \\ 0 \\ 0 \end{bmatrix} \qquad 7\text{–}5$$

Again, in dq coordinates two tones are being generated and injected into the system.

$$i_{p2d}(t)=\frac{I_{pm}}{3}\left[\cos\left(\omega_p t+\varphi_{p2}\right)+\cos\left(2\theta_{src}(t)-\omega_p t-\varphi_{p2}\right)\right] \qquad 7\text{–}6$$

$$i_{p2q}(t)=\frac{I_{pm}}{3}\left[-\sin\left(\omega_p t+\varphi_{p2}\right)-\sin\left(2\theta_{src}(t)-\omega_p t-\varphi_{p2}\right)\right] \qquad 7\text{–}7$$

In order to characterize small-signal impedance at injection angular frequency ω_p, it is necessary to combine both responses. The perturbation current matrix is obtained by putting together both perturbations vector. The perturbation vectors are independent and form a reversible matrix.

$$i_{pdq}(t)=\frac{I_{pm}}{3}\begin{bmatrix} \cos\left(\omega_p t+\varphi_{p1}\right) & \cos\left(\omega_p t+\varphi_{p2}\right) \\ \sin\left(\omega_p t+\varphi_{p1}\right) & -\sin\left(\omega_p t+\varphi_{p2}\right) \end{bmatrix} \qquad 7\text{–}8$$

Shunt current injection is injected into the system via parallel connection, thus each time current perturbation is injected it will generate two independent current responses $i_{sdq}(t)$ and $i_{ldq}(t)$, namely source and load current responses, and one common voltage response $v_{dq}(t)$. The extraction of frequency domain characteristic at the angular frequency ω_p, can be performed by applying Fast Fourier Transformation on sensed current and voltage responses.

$$\vec{i}_{s1dq}(j\omega_p) = FFT\left(\begin{bmatrix} i_{s1d}(t) \\ i_{s1q}(t) \end{bmatrix}\right) = \begin{bmatrix} i_{s1d}(j\omega_p) \\ i_{s1q}(j\omega_p) \end{bmatrix} \quad 7\text{–}9$$

$$\vec{i}_{s2dq}(j\omega_p) = FFT\left(\begin{bmatrix} i_{s2d}(t) \\ i_{s2q}(t) \end{bmatrix}\right) = \begin{bmatrix} i_{s2d}(j\omega_p) \\ i_{s2q}(j\omega_p) \end{bmatrix} \quad 7\text{–}10$$

$$I_{sdq}(j\omega_p) = \begin{bmatrix} i_{s1d}(j\omega_p) & i_{s2d}(j\omega_p) \\ i_{s1q}(j\omega_p) & i_{s2q}(j\omega_p) \end{bmatrix} \quad 7\text{–}11$$

The small signal characteristic combines voltage and current FFT responses.

$$Z_{sdq}(j\omega_p) = V_{dq}(j\omega_p) I_{sdq}^{-1}(j\omega_p) \quad 7\text{–}12$$

$$Z_{ldq}(j\omega_p) = V_{dq}(j\omega_p) I_{ldq}^{-1}(j\omega_p) \quad 7\text{–}13$$

7.3 Single-Phase Series Voltage Injection

The property of a shunt current injection is to mainly perturb the small impedance side, while series voltage injection mainly perturbs large impedance. If a big mismatch between source and load impedance magnitudes is present in a frequency range, then both shunt current and series voltage injection are necessary to be used in measurements to provide precise characterization of the system impedances at arbitrary interface. Apparently, there is a need to inject voltage and current perturbations into a system to obtain accurate identification of load and source small-signal dq impedances. Therefore, the ideal single-phase series voltage injection is shown in Figure 7-2.

In order to excite a system at certain angular frequency ω_p, numerous types of three-phase balanced or unbalanced injection sets are suitable candidates. The straight forward injection set, which can be generated with the proposed interleaved converter is given below.

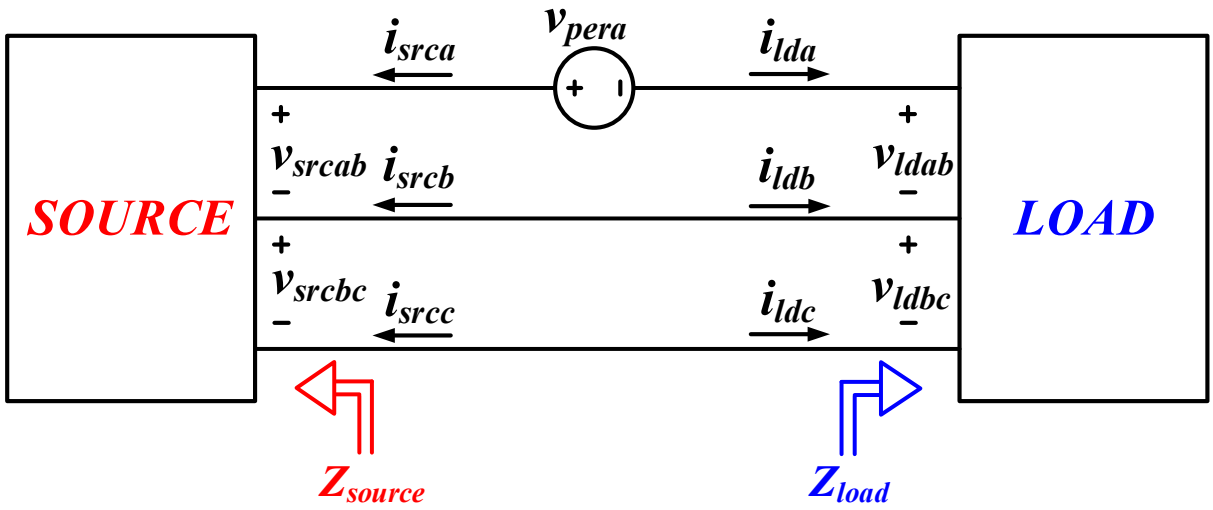


Figure 7-2: Ideal Single-Phase Series Voltage Injection

$$\begin{aligned} v_{p1a}(t) &= V_{pm}\cos\left(\omega_p t + \theta_{src}(t) + \varphi_{p1}\right) \\ v_{p1b}(t) &= 0 \\ v_{p1c}(t) &= 0 \end{aligned} \qquad 7\text{–}14$$

In dq coordinates two frequency points are actually being injected into a power system. The first frequency point is equal to desired injection frequency f_p, while the second frequency point is equal to f_p+2f_{src}.

$$v_{p1d}(t) = \frac{V_{pm}}{2}\left(\cos\left(\omega_p t + \varphi_{p1}\right) + \cos\left(\omega_p t + 2\theta_{src}(t) + \varphi_{p1}\right)\right) \qquad 7\text{–}15$$

$$v_{p1q}(t) = \frac{V_{pm}}{2}\left(\sin\left(\omega_p t + + \varphi_{p1}\right) - \sin\left(\omega_p t + 2\theta_{src}(t) + + \varphi_{p1}\right)\right) \qquad 7\text{–}16$$

The second perturbation injects a single-phase sinusoidal signal at frequency f_p-f_{src}.

$$\begin{aligned} v_{p2a}(t) &= V_{pm}\cos\left(\omega_p t - \theta_{src}(t) + \varphi_{p2}\right) \\ v_{p2b}(t) &= 0 \\ v_{p2c}(t) &= 0 \end{aligned} \qquad 7\text{–}17$$

Similarly, two frequency points are generated in dq coordinates, one at desired injection frequency f_p and one more frequency f_p-2f_{src} due to the nature of injection.

$$v_{p2d}(t)=\frac{V_{pm}}{2}\left(\cos\left(\omega_p t+\varphi_{p2}\right)+\cos\left(\omega_p t-2\theta_{src}(t)+\varphi_{p2}\right)\right) \quad 7\text{–}18$$

$$v_{p2q}(t)=\frac{V_{pm}}{2}\left(-\sin\left(\omega_p t+\varphi_{p2}\right)+\sin\left(\omega_p t-2\theta_{src}(t)+\varphi_{p2}\right)\right) \quad 7\text{–}19$$

It should be noted that two independent perturbation vectors are generated by phase modulating sinusoidal signals. Phase information $\theta_{src}(t)$ of three-phase voltage at a point of injection is necessary to be extracted and phase modulated into an signal injection reference during the both perturbations.

$$v_{pdq}(t)=\frac{V_{pm}}{2}\begin{bmatrix}\cos\left(\omega_p t+\varphi_{p1}\right) & \cos\left(\omega_p t+\varphi_{p2}\right)\\ \sin\left(\omega_p t+\varphi_{p1}\right) & -\sin\left(\omega_p t+\varphi_{p2}\right)\end{bmatrix} \quad 7\text{–}20$$

7.4 CPSD Identification Algorithm

The general expression of the perturbation injected is described with the following expression.

$$x_{pdq}(s)=A_{pm}\begin{bmatrix}H_{\cos}\left(s,\varphi_{p1}\right) & H_{\cos}\left(s,\varphi_{p2}\right)\\ H_{\sin}\left(s,\varphi_{p1}\right) & -H_{\sin}\left(s,\varphi_{p2}\right)\end{bmatrix} \quad 7\text{–}21$$

The following small-signal transfer functions are identified using the cpsd function.

$$V_{sdq}(s)=\begin{bmatrix}G_{vs11}(s) & G_{vs12}(s)\\ G_{vs21}(s) & G_{vs22}(s)\end{bmatrix}x_{pdq}(s) \quad 7\text{–}22$$

$$V_{sdq}(s)=\begin{bmatrix}G_{vl11}(s) & G_{vl12}(s)\\ G_{vl21}(s) & G_{vl22}(s)\end{bmatrix}x_{pdq}(s) \quad 7\text{–}23$$

$$I_{dq}(s)=\begin{bmatrix}G_{i11}(s) & G_{i12}(s)\\ G_{i21}(s) & G_{i22}(s)\end{bmatrix}x_{pdq}(s) \quad 7\text{–}24$$

The following small-signal transfer functions are identified using the cpsd function.

$$G_{vld1sm}(s)=\frac{V_{ld1}(s)}{refs(s)},\ G_{vld1cm}=\frac{V_{ld1}(s)}{refc(s)} \quad 7\text{–}25$$

$$G_{vlq1sm}(s)=\frac{V_{lq1}(s)}{refs(s)},\ G_{vlq1cm}=\frac{V_{lq1}(s)}{refc(s)} \quad 7\text{–}26$$

Two more sets of transfer functions are identified.

$$G_{vsd1sm}(s)=\frac{V_{sd1}(s)}{refs(s)},\ G_{vsd1cm}=\frac{V_{sd1}(s)}{refc(s)} \quad 7\text{–}27$$

$$G_{vsq1sm}(s)=\frac{V_{sq1}(s)}{refs(s)},\ G_{vsq1cm}=\frac{V_{sq1}(s)}{refc(s)} \quad 7\text{–}28$$

$$G_{id1sm}(s)=\frac{I_{d1}(s)}{refs(s)},\ G_{id1cm}=\frac{I_{d1}(s)}{refc(s)} \quad 7\text{–}29$$

$$G_{iq1sm}(s)=\frac{I_{q1}(s)}{refs(s)},\ G_{iq1cm}=\frac{I_{q1}(s)}{refc(s)} \quad 7\text{–}30$$

In order to identify small signal impedances one more set of transfer functions are identified.

$$G_{vld2sm}(s)=\frac{V_{ld2}(s)}{refs(s)},\ G_{vld2cm}=\frac{V_{ld2}(s)}{refc(s)} \quad 7\text{–}31$$

$$G_{vlq2sm}(s)=\frac{V_{lq2}(s)}{refs(s)},\ G_{vlq2cm}=\frac{V_{lq2}(s)}{refc(s)} \quad 7\text{–}32$$

$$G_{vsd2sm}(s)=\frac{V_{sd2}(s)}{refs(s)},\ G_{vsd2cm}=\frac{V_{sd2}(s)}{refc(s)} \quad 7\text{–}33$$

$$G_{vsq2sm}(s)=\frac{V_{sq2}(s)}{refs(s)},\ G_{vsq2cm}=\frac{V_{sq2}(s)}{refc(s)} \quad 7\text{–}34$$

$$G_{id2sm}(s)=\frac{I_{d2}(s)}{refs(s)},\ G_{id2cm}=\frac{I_{d2}(s)}{refc(s)} \quad 7\text{–}35$$

$$G_{iq2sm}(s)=\frac{I_{q2}(s)}{refs(s)},\ G_{iq2cm}=\frac{I_{q2}(s)}{refc(s)} \quad 7\text{–}36$$

The small-signal transfer functions of system current responses to the injection perturbation are identified with the following expressions.

$$G_{i11}(s)=-G_{id1sm}(s)+G_{id2sm}(s) \quad 7\text{–}37$$

$$G_{i12}(s) = G_{id1cm}(s) + G_{id2cm}(s) \quad 7\text{–}38$$

$$G_{i21}(s) = -G_{iq1sm}(s) + G_{iq2sm}(s) \quad 7\text{–}39$$

$$G_{i22}(s) = G_{iq1cm}(s) + G_{iq2cm}(s) \quad 7\text{–}40$$

The small-signal transfer functions of source voltage responses to the injection perturbation are identified with the following expressions.

$$G_{vs11}(s) = -G_{vsd1sm}(s) + G_{vsd2sm}(s) \quad 7\text{–}41$$

$$G_{vs12}(s) = G_{vsd1cm}(s) + G_{vsd2cm}(s) \quad 7\text{–}42$$

$$G_{vs21}(s) = -G_{vsq1sm}(s) + G_{vsq2sm}(s) \quad 7\text{–}43$$

$$G_{vs22}(s) = G_{vsq1cm}(s) + G_{vsq2cm}(s) \quad 7\text{–}44$$

The small-signal transfer functions of load voltage responses to the injection perturbation are identified with the following expressions.

$$G_{vl11}(s) = -G_{vld1sm}(s) + G_{vld2sm}(s) \quad 7\text{–}45$$

$$G_{vl12}(s) = G_{vld1cm}(s) + G_{vld2cm}(s) \quad 7\text{–}46$$

$$G_{vl21}(s) = -G_{vlq1sm}(s) + G_{vlq2sm}(s) \quad 7\text{–}47$$

$$G_{vl22}(s) = G_{vlq1}(s) + G_{vlq2}(s) \quad 7\text{–}48$$

Finally the small signal source and load dq impedances are identified in the following manner.

$$Z_{sdq}(s) = \begin{bmatrix} G_{vs11}(s) & G_{vs12}(s) \\ G_{vs21}(s) & G_{vs22}(s) \end{bmatrix} \begin{bmatrix} G_{i11}(s) & G_{i12}(s) \\ G_{i21}(s) & G_{i22}(s) \end{bmatrix}^{-1} \quad 7\text{–}49$$

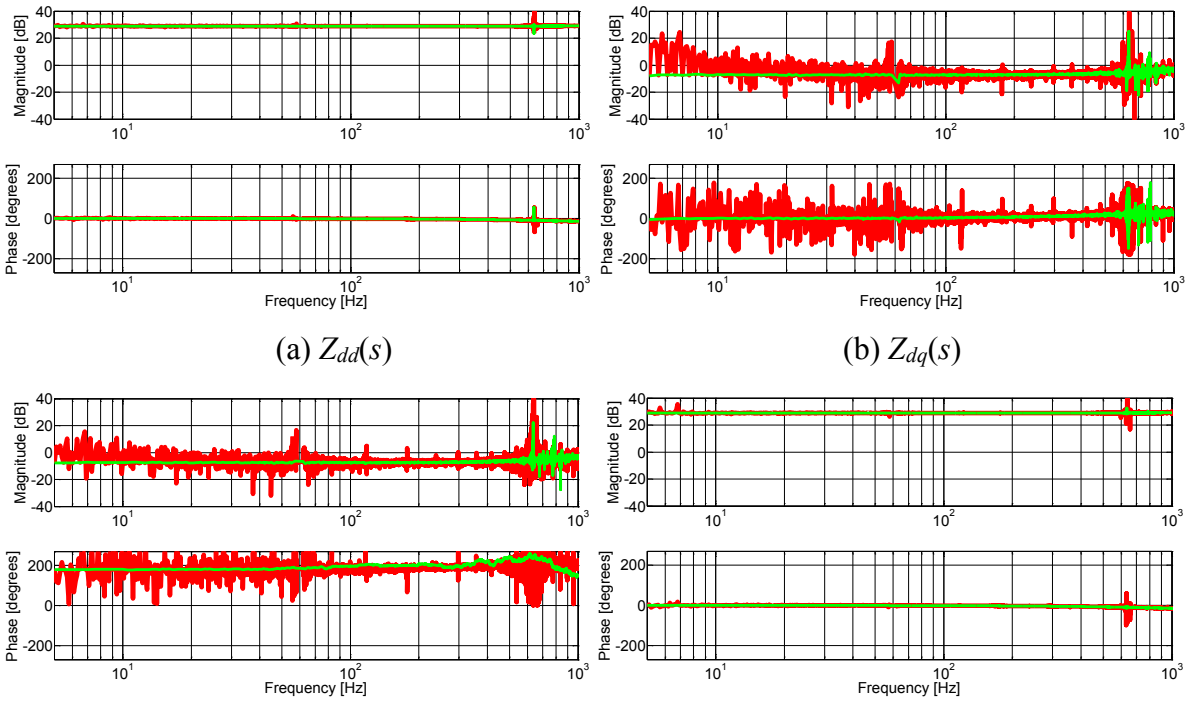
$$Z_{ldq}(s) = -\begin{bmatrix} G_{vl11}(s) & G_{vl12}(s) \\ G_{vl21}(s) & G_{vl22}(s) \end{bmatrix} \begin{bmatrix} G_{i11}(s) & G_{i12}(s) \\ G_{i21}(s) & G_{i22}(s) \end{bmatrix}^{-1} \quad 7\text{–}50$$

7.5 Small-Signal dq Impedance Results Identified with SVI Converter

This section presents the identification of small-signal dq impedances via the single-phase series voltage injection is presented in this section. Single-phase SVI converter is connected between a programmable voltage source and three-phase resistive load.

7.5.1 Impedance Identification via the Single-Phase Voltage Injection of Chirp Signal

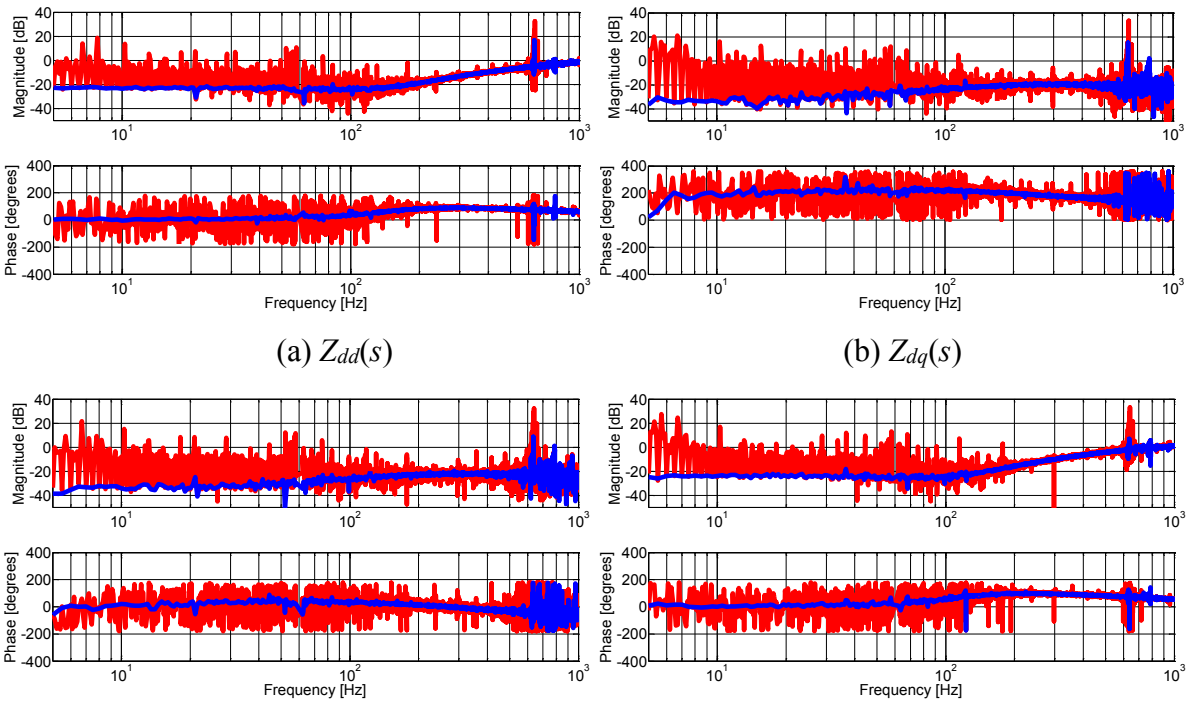
The comparison of load dq impedances obtained via the SVI of chirp signal in 17 frequency ranges around the line frequency (5 Hz - 58 Hz, 62 Hz - 118 Hz, ...,902 Hz - 958 Hz and 962 Hz - 1000 Hz) is shown in Figure 2-20. In this way, the chirp signal spreads the signal energy equally in the entire frequency range, resulting in the identification in large number of points. The small-signal dq impedance of resistive identified with FFT algorithm is shown with straight red line. In addition, the small-signal dq impedance of resistive load identified with cpsd algorithm is shown with the straight green line. It can be verified that cpsd algorithm effectively reduces the noise influence on the small-signal dq impedances. The cross-diagonal impedances $Z_{dq}(s)$ and $Z_{qd}(s)$ are covered with noise and FFT algorithm yields unclear results. However, cpsd algorithm effectively reduces the noise level in the voltage and current responses, providing much cleaner results. The main diagonal small-signal impedances $Z_{dd}(s)$ and $Z_{qq}(s)$ are higher in value and above the noise level. In this case, both FFT and cpsd algorithms yield very similar results.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 7-3: Comparison of load dq impedances obtained via voltage injection of chirp signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

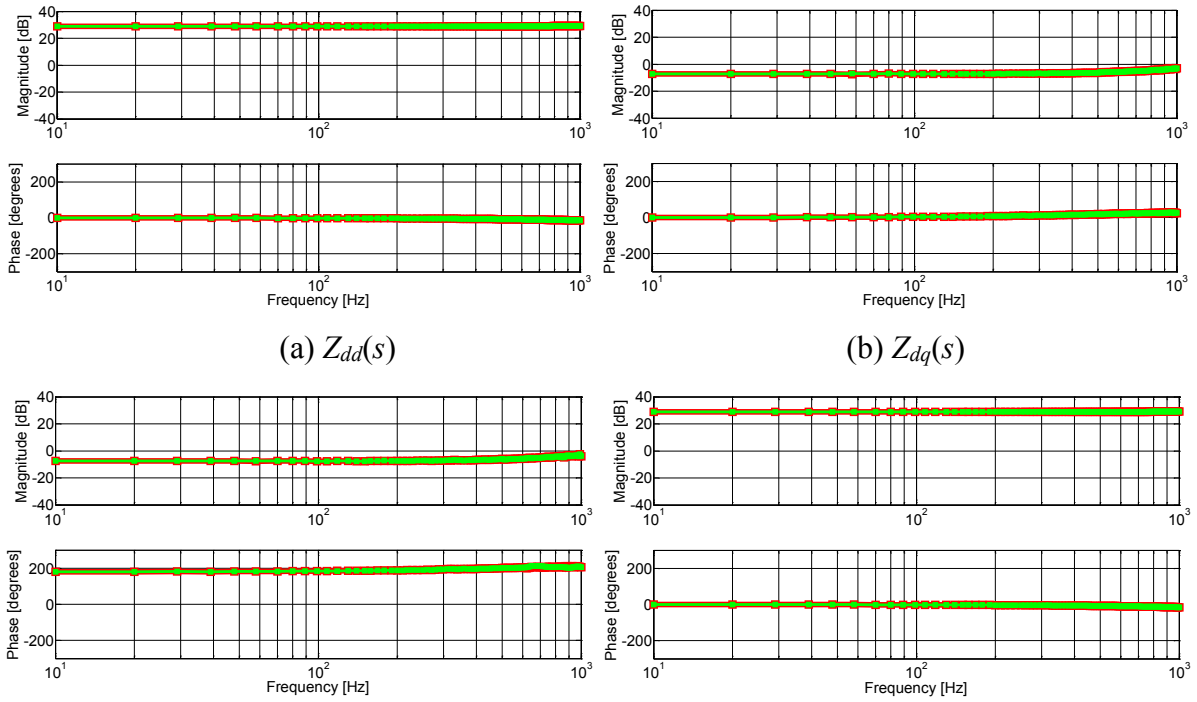
Figure 7-4: Comparison of source dq impedances obtained via voltage injection of chirp signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

The comparison of source small-signal dq impedances obtained via chirp injection are shown in Figure 7-4. The source impedances are smaller in values compared to load dq impedances, thus the identified source impedance results are covered even more in noise. In this case FFT algorithm provides unclean results for all four dq impedances. CPSD algorithm provides much cleaner results. Still, the high frequency range of cross-diagonal impedances $Z_{dq}(s)$ and $Z_{qd}(s)$ is small in value and intensively covered with noise, thus the cpsd algorithm fails to completely remove the noise.

7.5.2 Impedance Identification via the Single-Phase Voltage Injection of Multi-Tone Signal

The small-signal dq impedances of programmable voltage source and resistive passive load are identified via the injection of multi-tone signal. The multi-tone signal is injected in 17 frequency ranges, but in each frequency range about 5 points are being excited. In this way the energy of the multi-tone is shared among number of points in the range, resulting in the identification of impedance in 100 points. The comparison of resistive load dq impedances via the

injection of multi-tone signal and identification by FFT and cpsd algorithms are shown in Figure 7-5.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

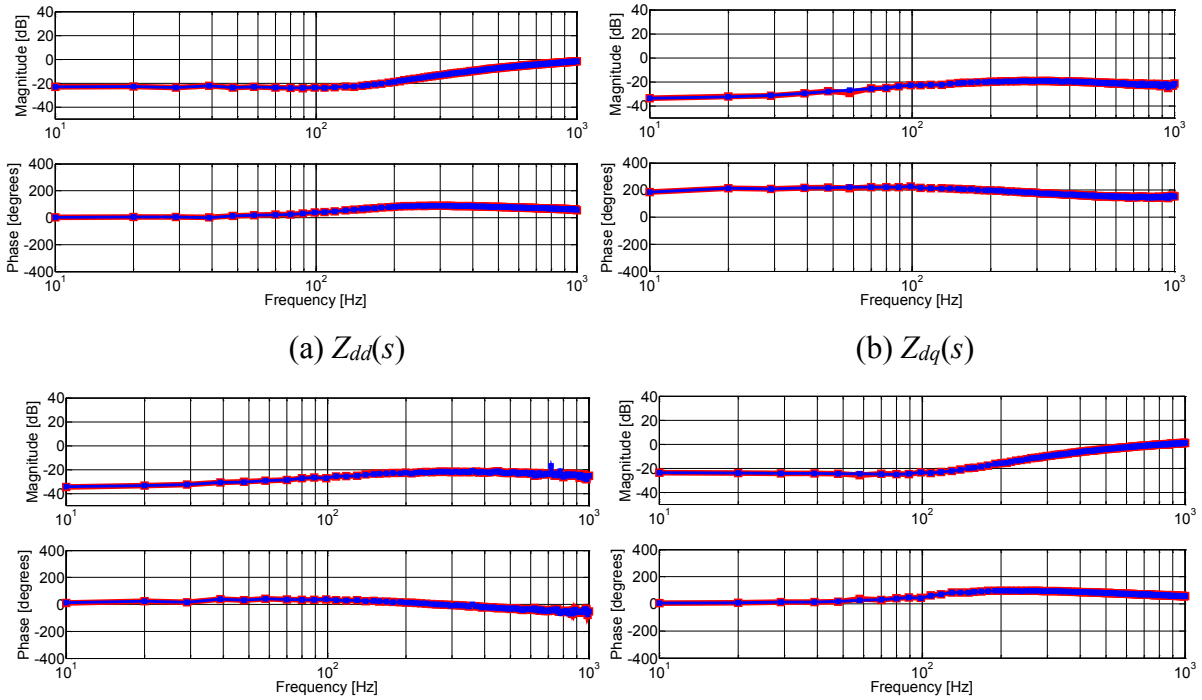
(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 7-5: Comparison of load dq impedances obtained via voltage injection of multi-tone signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

In this case, the current and voltage responses are much above the noise level, resulting in the clean identification of impedances. Furthermore, both FFT and cpsd algorithm yield similarly clean results, meaning that no significant improvement is achieved with the usage of cpsd algorithm. The clean impedances results are obtained as signal energy is used to excite smaller number of frequency points, compared to the injection of chirp signal.

In addition, the comparison of small-signal dq impedance of programmable voltage source are shown in Figure 7-6. The impedances identified with FFT algorithm are shown in red line and compared to the impedances identified with cpsd algorithm, which are shown in blue line. Due to the injection of multi-tone signal, the source dq impedances are successfully extracted with both identification algorithms. Comparatively, both FFT and cpsd identification algorithms provide very similar results. In this case, it can be concluded that no significant benefit is obtained with the usage of cpsd algorithm, as voltage and current responses are significantly above the noise

level. Furthermore, since the three-phase power system under test is excited with multi-tone signal, the voltage and current responses of both source and load side are above the noise level, resulting in the precise identification of source and load dq impedances.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

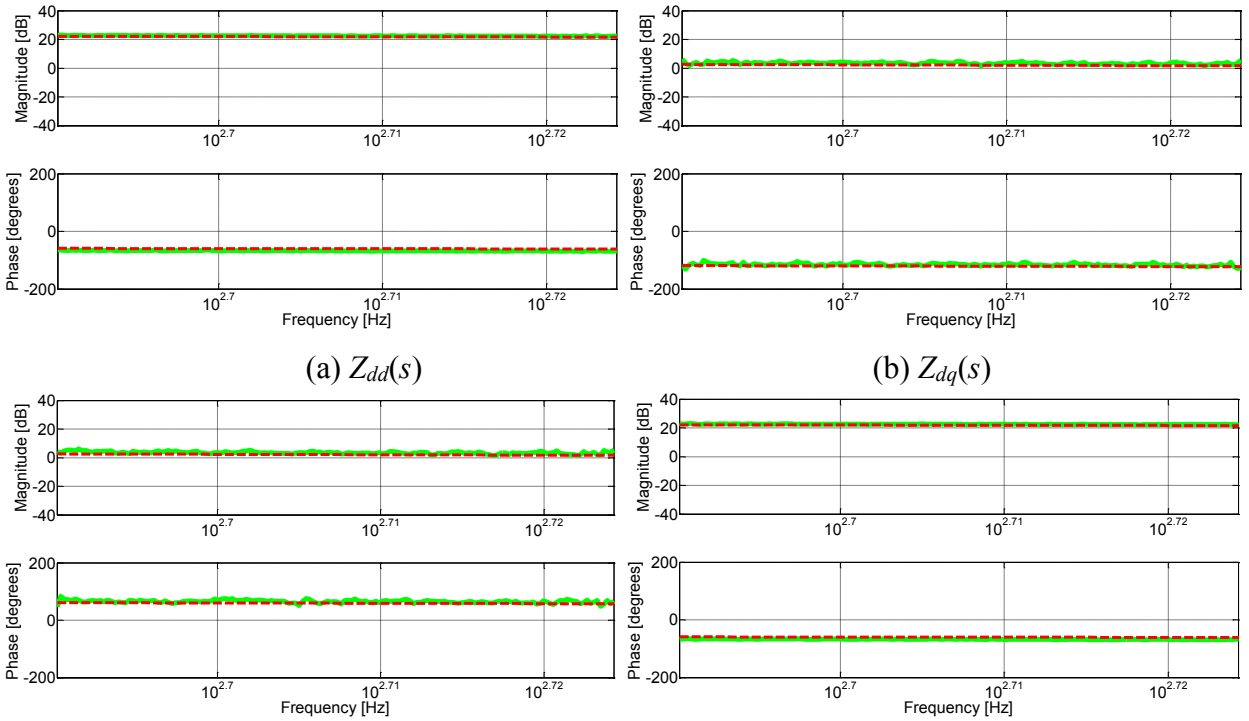
Figure 7-6: Comparison of source dq impedances obtained via voltage injection of multi-tone signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

7.6 Small-Signal dq Impedance Results Identified with SCI Converter

This section presents the identification of small-signal dq impedances via the single-phase shunt current injection is presented in this section. Single-phase SCI converter is connected between a programmable voltage source and passive load (parallel connection of three-phase resistors and capacitors).

7.6.1 Impedance Identification via the Single-Phase Current Injection of Chirp Signal

The load dq impedances of three-phase passive load are obtained with the injection of chirp signal in single frequency range (490 Hz – 530 Hz). The small-signal dq impedances of passive load are identified with the usage of cpsd algorithm. The obtained dq impedances are shown with



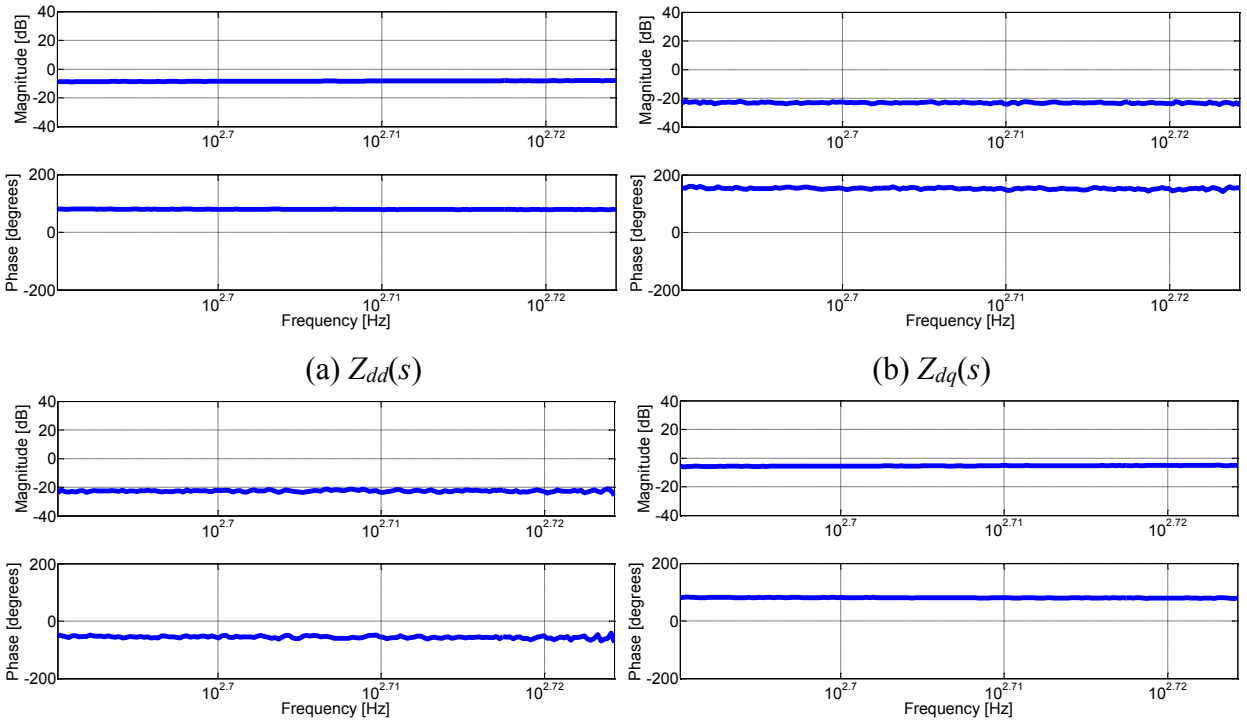
(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 7-7: Comparison of load dq impedances obtained via current injection of chirp signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

green line in Figure 7-7. The estimated dq impedances of passive load are shown in dashed red line and compared to experimental measurements as shown in Figure 7-7.

The small-signal dq impedances of programmable voltage source is extracted with cpsd algorithm. The identified impedance results are shown in Figure 7-8. The obtained source small-signal dq impedance results are cleaner compared load small-signal dq impedances. The shunt current injection excites the small impedance side better as current splits unequal. Nevertheless, the identification of source and load impedances is achieved with reasonable high accuracy.



(a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$

(c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

Figure 7-8: Source small-signal dq impedances obtained via current injection of chirp signal (a) $Z_{dd}(s)$ (b) $Z_{dq}(s)$ (c) $Z_{qd}(s)$ (d) $Z_{qq}(s)$

7.7 Summary and Conclusions

The impedance extraction of small-signal dq impedances is successfully performed by FFT algorithm. The algorithm is further improved by the implementation of cpsd algorithm, which is based on Welch's periodogram spectral density estimation. Wide-bandwidth injection signals are proposed for the system excitation, providing a way to simultaneously excite more frequency points instantaneously. The small-signal dq impedances of programmable voltage source, which is actively controlled, and resistive passive load are successfully extracted using chirp and multi-tone signals. The effectiveness of shunt current single-phase injection for the precise characterization of small impedances is presented. Furthermore, the effectiveness of the series voltage single-phase injection for the precise characterization of large impedances is presented as well. In some of the presented cases, the injection of multi-tone signal yielded the precise characterization of both source and load dq impedances.

Chapter 8. Conclusions and Future Work

8.1 Conclusions

The identification of small-signal dq impedances of power electronics converters via the single-phase injection of wide-bandwidth signals is presented and proposed in the dissertation. In order to identify small-signal dq impedances, two wide-bandwidth injection signals, multi-tone and chirp, are comprehensively analyzed and proposed for the injection into the power system under the test.

The tradeoffs between the two signals are presented, proposing the injection of chirp signal if the power system under measurement does not response with the noisy results. In this way the accurate identification is performed in greater number of points. However, if the excitation of the power system yields noisy current and voltage responses, then the multi-tone injection is proposed for the system perturbation, providing the impedance identification in smaller number of points with the increased accuracy. In the case of the identification of strongly nonlinear systems, which generates significant sideband harmonics as a response to signal injection, then the sinusoidal signal injection is proposed for the impedance identification. In this way, the whole signal energy is used to excite a single frequency point, and ac sweeping is used to provide the small-signal impedance results in the frequency range of interest. The impedance identification is performed via brute force method, which is time intensive in nature.

Two different identification algorithm base on fast Fourier transform (FFT) and cross power spectral density (CPSD) estimation are proposed and presented. The effectiveness of CPSD estimation algorithm is presented for the wide-bandwidth perturbation if the responses are covered in noise. Furthermore, due to the reduction of noise influence on the measurements, in some case it was possible to identify the source and load impedances with just single type of injection. In order to effectively use the CPSD estimation algorithm, the knowledge of input reference signal was used to clean out the influence of the noise.

Additionally, the comprehensive modeling of small-signal dq impedances of diode rectifiers is presented. The comparison of small-signal dq admittances obtained from the analytical and parametric averaged models of diode rectifiers, switching simulation models and experimental set-up is presented. The small-signal modification of analytical average value model (AAVM) is proposed, providing the improvement in the accuracy of the average model. Furthermore, analytical expressions of the input dq admittance of both AVMs are derived, proving that AVMs can predict precisely admittances $Y_{dd}(s)$ and $Y_{qd}(s)$ even in the frequency range beyond the switching frequency as d-channel injection behaves as a linear injection. Admittance $Y_{qq}(s)$ is predicted accurately up to half the switching frequency, while admittance $Y_{dq}(s)$ is predicted accurately up to one fourth of the switching frequency. This is explained by the fact that there are sideband admittances around multiples of switching frequency in admittances $Y_{dq}(s)$ and $Y_{qq}(s)$, due to the q-channel injection. The new phenomenon is accurately captured both in hardware measurements and in switching simulation model with the use of developed small-signal extraction techniques. The validity range of AAVMs and parametric averaged value models (PAVMs) is estimated and limitations in the precision are explained.

In addition, a detailed comparison of input dq admittances for twelve –pulse diode rectifier feeding a resistive load, obtained from AAVM, switching simulation model and hardware set-up measurements are presented. The same sideband admittances are captured and contributed to the strong nonlinear behavior of twelve-pulse diode rectifier.

The single-phase multi-level cascaded H-bridge converter is proposed of the shunt current injection of wide-bandwidth injection signals. The complete design procedure, which aims to optimize the control and selection of inductance and capacitance values, is presented. The effectiveness of the proposed solution is verified in the online identification of impedances. The main benefits of the proposed current injection solution are the generation of the cleaner current injection, reduced stress of the used power electronics switches, distributive reactive energy storage and modular design. Furthermore, due to the multi-level modular structure of the converter, the proposed solution is scalable and can be used in the identification of the impedances of medium voltage power systems.

The implemented SCI converter is reconfigurable to a single-phase interleaved converter suitable for the single-phase series voltage injection (SVI). Special attention is focused on the design of high bandwidth ac current, high bandwidth ac voltage loop and low bandwidth dc voltage loop, providing fast and robust control. The interleaved solution provides wider injection range, means to characterize higher current rated systems because of current sharing among modules and enables generation of cleaner injection signal. The used ac side filter is of the second order, minimizing the injection of unwanted switching noise. Even more, the proposed interleaved SVI converter does not require an isolation transformer, resulting in the reduced size, weight and cost and is capable of self-charging via dc voltage control. Furthermore, the proposed transformerless solution is capable of injecting the low frequency signals in dq coordinates by avoiding transformer saturation problems, resulting in the increased injection frequency range.

Wide-bandwidth injection signals are proposed for the system excitation, providing a way to simultaneously excite more frequency points instantaneously. The effectiveness of the proposed single-phase wide-bandwidth injection is demonstrated on the impedance identification of actively controlled programmable voltage source supplying the passive load.

8.2 Future Work

The following future research direction are identified during the development of the single-phase impedance measurement unit.

The proposed single-phase converters, which are used to perturb the power systems, are modular and scalable to medium voltage range (4160 V). Therefore, the proposed solution is suitable to be used in small-signal identification of ac medium voltage high power systems. Based on the presented analysis, it is expected that both multi-level and interleaved converters are straight forward for the implementation in the medium voltage range. In order to implement a medium voltage scaled up IMU, a high-voltage silicon carbide MOSFETs could be used, providing high blocking voltage, high current conductivity and fast switching capability.

Furthermore, the designed IMU can be easily modified to characterize positive and negative sequence or abc small-signal impedances. The purpose of modifying IMU is to compare all three

impedance identification approaches and theirs usability in the stability analysis of modern ac power systems. The final goal would be to identify benefits and limitations of each approach.

In order to try to minimize values and size of dc capacitors, a possible way to improve injection converters is to implement the active energy concept. The implementation of the concept requires one more phase leg (two MOSFETs) with additional inductance and capacitance. By actively controlling the added phase leg it is possible to move the stored ripple energy to additional inductor and capacitor. In this way, additional capacitor could tolerate higher ripple values as it does not influence the operation of the converters.

The control of the injection converter could be improved via the implementation of MIMO control strategies. In this way, higher bandwidth of the control loops is achievable, which would result in improved identification frequency range of the unit.

In addition, the applicability of other converter topologies in the impedance identification process could be researched as well. Current source based topologies consist of second order filter on ac side, providing the possibility to inject the cleaner current perturbation into the system. In addition, modifying the existing current injection converter by coupling the ac side inductors could reduce the ac filter impedance in high frequency range, resulting in the increased frequency range of the conveter.

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