Analysis and Design of a DCM SEPIC PFC with Adjustable Output Voltage

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ABSTRACT

Power Factor Correction rectifiers are widely adopted as the first stage in most grid-tied power conversion systems. Among all PFC converts for single phase system, Boost PFC is the most popular one due to simplicity of structure and high performance. Although the efficiency of Boost PFC keeps increasing with the evolution of semiconductor technology, the intrinsic feature of high output voltage may result cumbersome system structure with multiple power conversion stages and even diminished system efficiency. This disadvantage is aggravated especially in systems where resonant converters are selected as second stage.

Especially for domestic induction cooker application, step-down PFC with wide range output regulation capability would be a reasonable solution. Conventional induction cooker is composed by input filter, diode-bridge rectifier and full bridge or half bridge series resonant circuit (SRC). High frequency magnetic field is induced through the switching action to heat the pan. The power level is usually controlled through pulse frequency modulation (PFM). In such configuration, first, a bulky input differential filter is required to filter out the high frequency operating current in SRC. Second, as the output power decreases, the operating point of SRC is moved away from the optimum point, which can result large amount circulating energy. Third, when the pan is made of well conducting and non-ferromagnetic material such as aluminum, due to the heating resistance

become much smaller and peak output voltage of the switching bridge equals to the peak voltage of the grid, operating the SRC at the series resonant frequency can result excessive current flowing through the switch and the heating coil. Thus for pan with smaller heating resistance, even at maximum power, the operating frequency is pushed far away from the series resonant point, which also results efficiency loss.

To address these potential issues, a PFC circuit features continuous conducting input current, high power factor, step-down capability and wide range output regulation would be preferred. The Analysis and design work is present in this article for a non-isolated hard switching DCM SEPIC PFC. Due to DCM operation of SPEIC converter, wide adjustable step-down output voltage, continuous conduction of input current and elimination of reverse recovery loss can be achieved at same time.

The thesis begins with circuit operation analysis for both DC-DC and PFC operation. Based on averaged switching model, small signal model and corresponding transfer functions are derived. Especially, the impact from small intermediate capacitor on steady state value are discussed.

With the concept of ripple steering, theoretic analysis is applied to SEPIC converter with two coupled inductors. The results indicate with proper selected coupling coefficient, the equivalent input inductance can be multiple times larger than the self-inductance. Because of this, while maintaining input current ripple same, the two inductors of SEPIC can be implemented with two smaller coupled inductors. Thus both the total volume of inductors and the total number of windings can be reduced, and the power density and efficiency can be improved. Based on magnetic reluctance model, a corresponding winding

scheme to control the coupling coefficient between two coupled inductors is analyzed. Also the impact of coupled inductors on the small signal transfer function is discussed.

For the voltage follower control scheme of DCM PFC, single loop controller and notch filter design are discussed. With properly designed notch filter or the PR controller in another word, the closed loop bandwidth can be increased; simple PI controller is sufficient to achieve high power factor; THD of the input current can be greatly reduced.

Finally, to validate the analysis and design procedure, a 1 kW prototype is built. With 120 Vrms AC input, 60V to 100V output, experimental results demonstrate unity power factor, wide output voltage regulation can be achieved within a single stage, and around 93% efficiency with 1 kW output.

Acknowledgements

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Chapter 1:

Introduction

1.1 Overview of Power Factor Correction Circuits

With the increasing demand for electrical energy and concerns on harmonics contents in ac grid, *Power Factor Correction* (PFC) circuits, as an essential power conversion interface between various electrical load and AC power grid, are widely adopted in many applications to meet the *Electromagnetic Interference* (EMI) standard - IEC EN 61000-3-2 [1]. As shown in TABLE. 1.1, the standard set clear limitation on current harmonics level for various applications.

TABLE. 1.1 IEC 61000-3-2 harmonics standard classification [2]

Abidin M N Z. IEC 61000-3-2 Harmonics Standards Overview[J]. Schaffner EMC Inc., Edsion, NJ, USA, Luterbach Switzerland, 2006. Used under fair use, 2015.

Class A	- Balanced three-phase equipment - Household appliances, excluding equipment identified by Class D - Tools excluding portable tools - Dimmers for incandescent lamps - Audio equipment - Everything else that is not classified as B, C or D
Class B	- Portable tools - Arc welding equipment which is not professional equipment
Class C	Lighting equipment
Class D	- Personal computers and personal computer monitors - Television receivers Equipment must have power level 75W up to and not exceeding 600W

In principle, with diode bridge rectifier, PFC function can be achieved based on any basic DC-DC converter topology, including buck, boost, buck-boost, SEPIC, Cuk and Zeta.

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In practice, PFC circuit based on boost, flyback and SEPIC converter are more widely adopted compared to other DC-DC topologies.

As the most efficient PFC circuit [3], the boost type PFC is widely adopted in applications with power rating from hundred watts to several kilo-watts. Due to the intrinsic boost characteristic, the output voltage of boost PFC must be higher than the peak of ac line voltage, which usually is 400V. Thus in different applications, at least a second stage is required to convert the boost PFC output to a specific voltage level of the application. Figure 1.1 shows the circuit diagram of the boost type PFC.
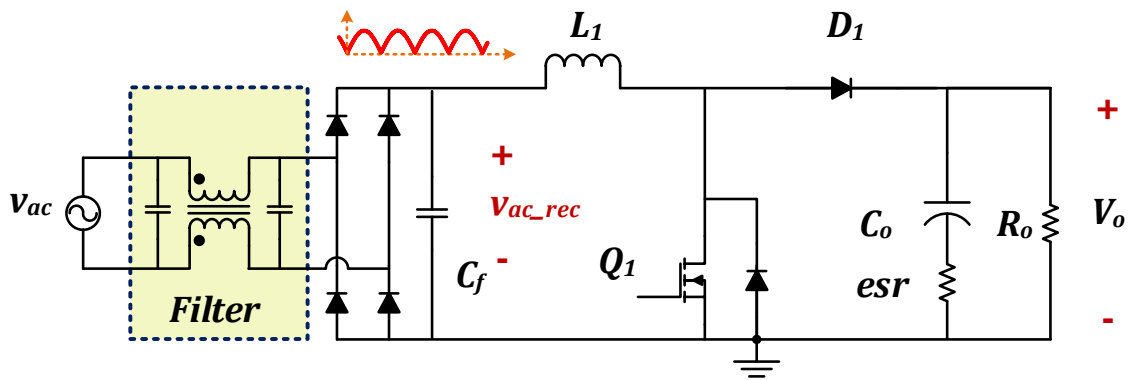
Figure 1.1 The boost PFC
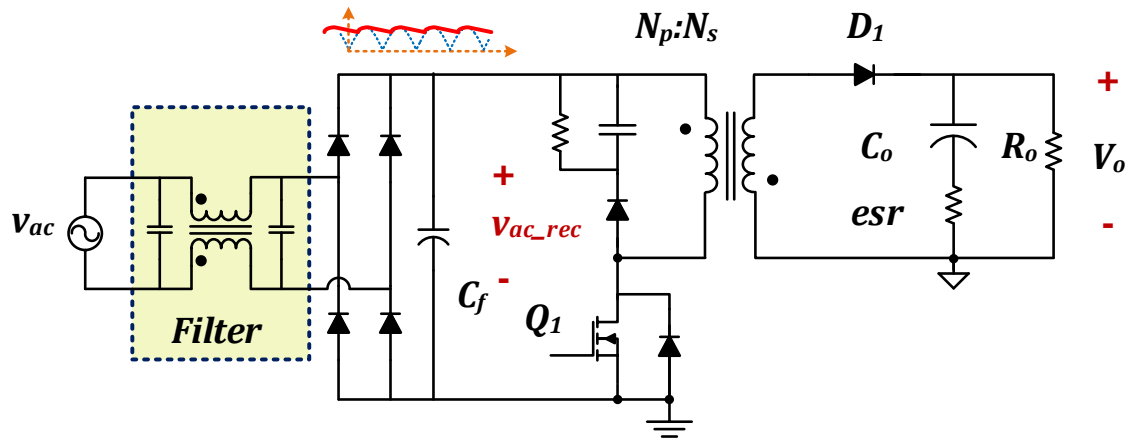
Figure 1.2 The passive PFC with flyback converter

For low power applications such as auxiliary power supply inside the grid connected equipment and adaptors for mobile devices, since harmonics requirement is not specified in IEC 61000-3-2 when power rating is less than 75W, the combination of passive

PFC and flyback converter almost excludes all other type PFC circuits in this application. The circuit diagram is shown in Figure 1.2. Compared with boost PFC, the drawback is the low power factor and bulky electrolytic capacitor C_f, while the advantages include single stage solution, galvanic isolation between AC grid and the load, reduced capacitance requirement on the output side, and also low cost and small size.

In applications such as LED lightning, which is classified as Class C in IEC 61000-3-2, active flyback PFC and SEPIC PFC are widely adopted [4] - [11]. The corresponding circuit diagrams are shown in Figure 1.3 and Figure 1.4. Compared to passive flyback PFC, the power factor with active PFC can be improved. Compared to boost PFC, both circuit is single stage solution. In these applications, cost and size limitation are the major design constraints.
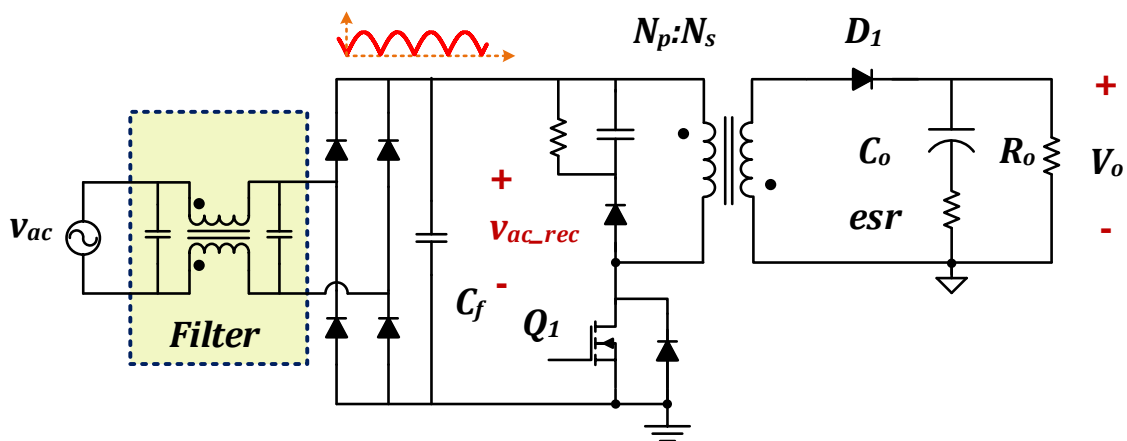
Figure 1.3 The flyback PFC for LED lighting
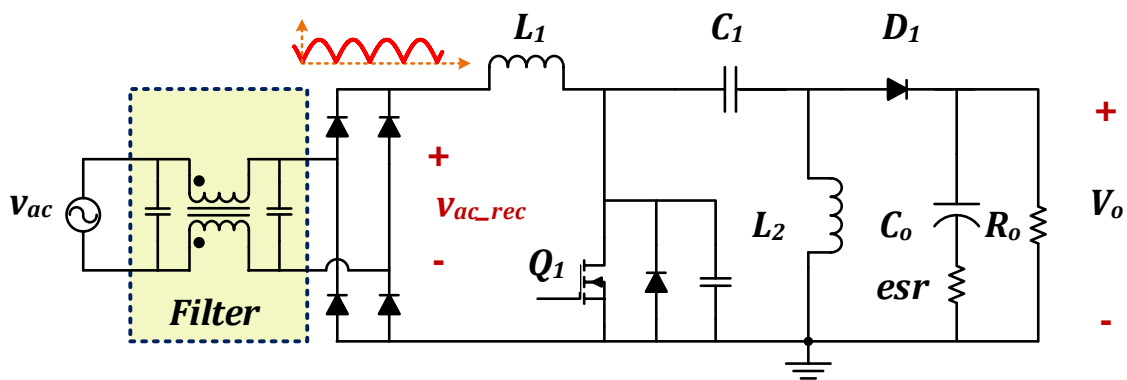
Figure 1.4 The SEPIC PFC

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1.2 Induction Cooking System

Although the efficiency of the front end boost PFC could be as high as 99% [3], the overall system efficiency could be suffered when the subsequent converter needs to operate at the non-optimal point, which is especially apparent when resonant converter and wide load range are involved.

Usually the output of resonant converter is regulated by PFM (pulse frequency modulation), in which the operating frequency varies when the load changes. Under light load condition, the operating frequency would move away from the optimized operating frequency that is designed for full load condition, the circuit would generate large amount of circulating energy exchanging between the source and the resonant elements, which eventually would result decreased efficiency.
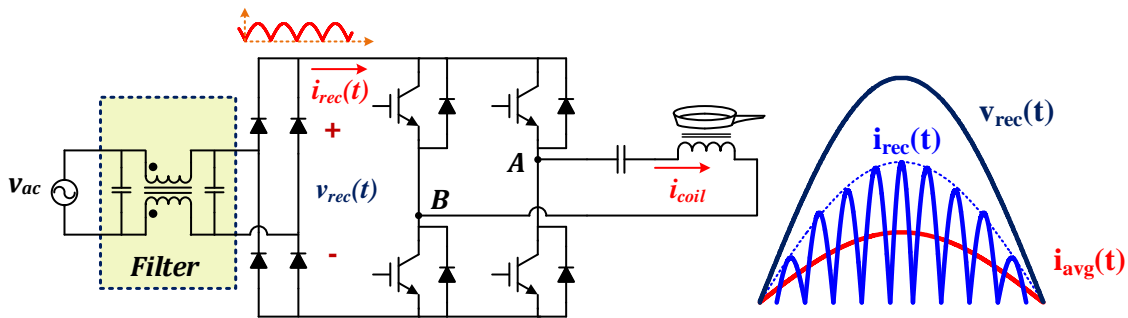
Figure 1.5 A full bridge induction cooker
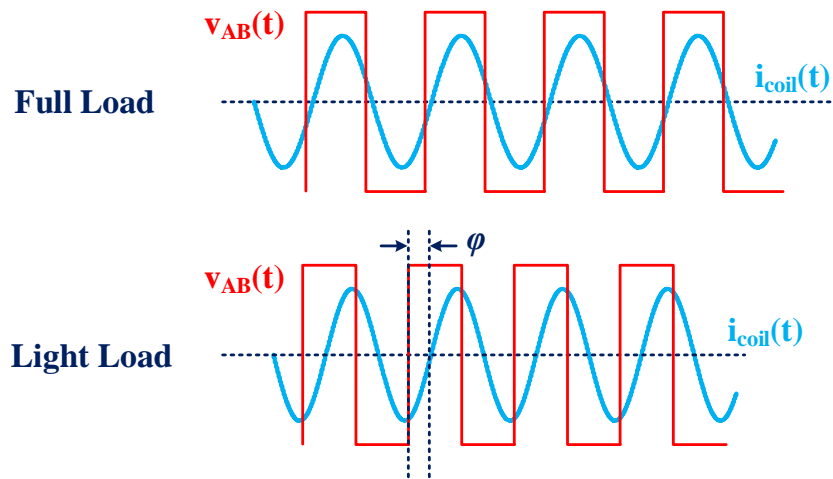
Figure 1.6 Phase difference between switch node voltage and coil current

The induction cooker [12][13][14] is an example application to demonstrate this issue. As shown in Figure 1.5, the series resonant converter is adopted in the circuit. Because the coil and the pan can be modeled as a series L-R branch, when the operating frequency is close to but larger than the resonant frequency, the current flowing through the coil is almost a sinusoidal current in switching frequency. The input diode bridge current will be the same as the coil current within each half line cycle. Since the magnitude of coil current is proportional to the DC bus voltage, the averaged input current will follow the rectified input AC voltage under fixed operating frequency. After adding the input filter stage, the PFC function can be achieved.

In this configuration, as shown in Figure 1.6, when load decreases, the operating frequency needs to be increased. Since the switching frequency moves away from the resonant frequency, the phase difference between the switch node voltage and coil current increases. In this case, the turn off switching loss would increase; the ratio of circulating energy to heating energy would also increase; thus the efficiency decreases.

For this configuration, another potential issue may arise when considering the compatibility with stainless steel or aluminum pan. As presented in [13], most domestic induction cooker can cook pan made with ferromagnetic material, and the typical equivalent reflected resistance is higher than 8Ω with operating frequency in the range of 25 kHz to 40 kHz. For pan made with stainless steel, within the same frequency region, the reflected resistance can be in the range of 2.5Ω to 6Ω; while for pan made with aluminum, the reflected resistance can be lower than 1 Ω. Considering an induction cooker for stainless steel pan is built with this circuit, assuming the equivalent inductance are same for all the pans with different reflected resistance, if the operating frequency is designed to be close to resonant frequency for 4 Ω pan,; when cooking with 6 Ω pan, the power delivered to the pan would be insufficient, when cooking with 2.5 Ω pan at full load condition, the operating frequency need to be moved away from the resonant frequency to avoid over power.

To address these potential issues, a PFC circuit with continuous conducting input current, step down output voltage and capability to adjust the output voltage in wide range

is a good solution. By adding a PFC circuit which can fulfil all these requirement as the front end of series resonant inverter, the load variation can be compensated by the output voltage adjustment, thus the operating frequency of the series resonant inverter can be always set to optimum frequency.

1.3 DCM SEPIC PFC
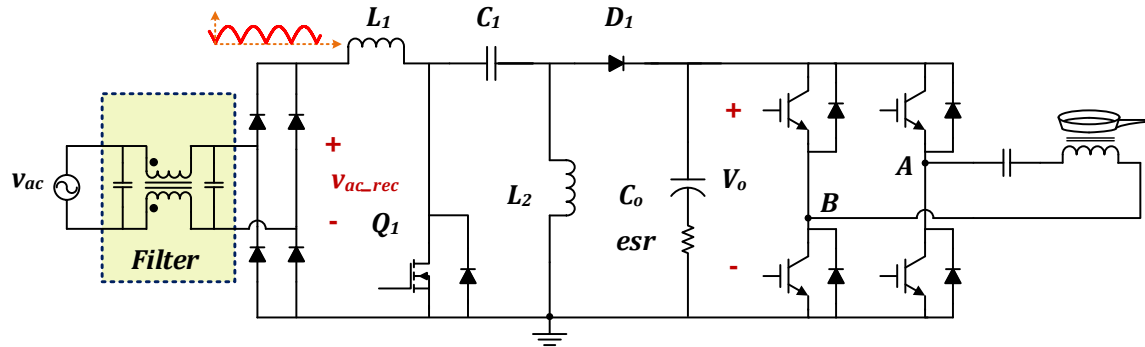
Figure 1.7 DCM SEPIC PFC front end for induction cooker

Considering the single stage *single-ended primary-inductor converter* (SEPIC) PFC operating in DCM, the input current can be continuous conducting, the output voltage can be lower than the input voltage and the output voltage regulation can be achieved with simple duty cycle modulation.

Meanwhile, other benefits can be obtained from DCM operation including the output diode turns off with zero current; when the main switch turns on, the current increases at relative low slew rate which is controlled by the paralleled inductance of L_1 and L_2; with fixed switching frequency, the control loop is very simple, only voltage feedback loop is required for PFC function; with coupled inductors, two inductor can be coupled together, which make the total components number almost comparable to boost PFC.

With all these features, design and implementation work for a 1kW DCM SEPIC PFC with 60V to 100V output is selected as the study topic.

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1.4 Study Objective and Outline of Thesis

The target of this research is to implement a non-isolated 1 kW single phase single stage PFC converter with adjustable output voltage range from 60V to 100V. To achieve this goal, the thesis covers analysis and design of a single phase DCM SEPIC PFC converter.

Chapter 1 presents the application background. Chapter 2 focuses on the switching average modeling of DCM SEPIC converter. Chapter 3 discusses the characteristics of coupled inductors adopted in SPEPIC converter. Chapter 4 describes the system design considerations. Design criteria on power stage parameters are analyzed. Control loop design is also presented. Chapter 5 demonstrates the experimental results. Chapter 6 concludes the thesis and provides possible directions for future work.

Chapter 2:

Circuit Operation Analysis and Modeling for DCM SEPIC Converter

In this chapter, circuit operation and key waveforms of DC-DC SEPIC converter working in DCM are analyzed first. With the concept of averaged PWM switch, the derivation of switching averaged model is presented. Formulas revealing the relationships between averaged state variables are summarized. Correspondingly the small signal model and transfer functions are presented. Then the same analysis is applied to PFC operation. The variations of operating point and corresponding bode plots of transfer functions in PFC operation are presented. Finally, the derived model is compared with simulation results. The agreement validates the analysis procedure and derived models.

2.1 DCM Operation of DC-DC SEPIC
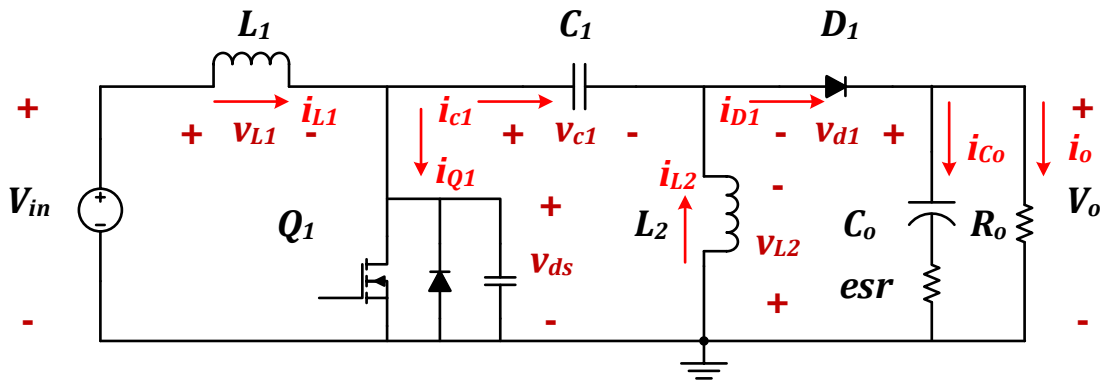
Figure 2.1 DC-DC SEPIC converter

For a DC-DC SPEIC converter shown in Figure 2.1, by defining DCM as the current flowing through the output rectifying diode D_1 is in discontinuous conducting mode, two DCM operations can be achieved with different inductance selection. As shown in Figure 2.2, the major difference between the two DCM modes resides in the continuity of

inductors' current. In one mode the current of both inductors are still continuous conducting, while in another mode they are discontinuous conducting. $2 \cdot \Delta i_{L1}$ and $2 \cdot \Delta i_{L2}$ denote peak to peak current ripple of inductor L_1 and L_2; I_r denotes **the interval mean current** of inductor L_1 during the third interval D_3T_s; and T_s denotes switching period.
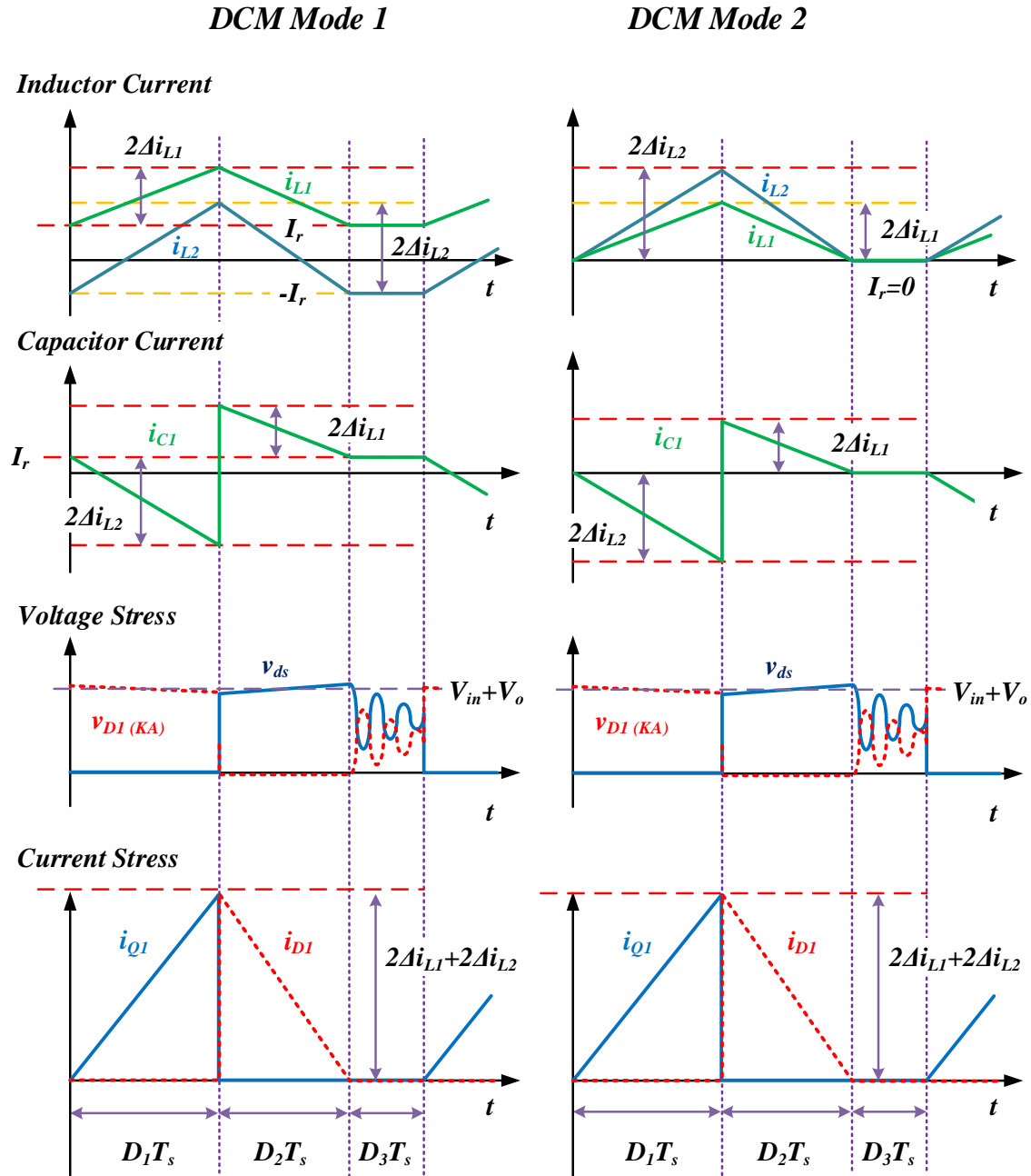
Figure 2.2 Key waveforms of DCM SEPIC

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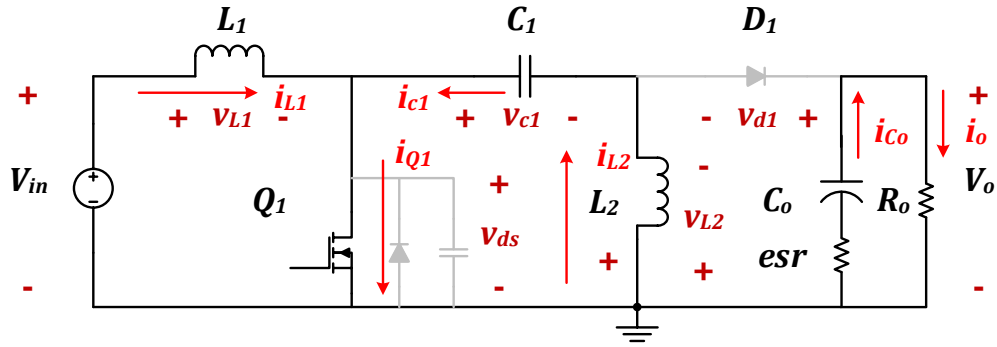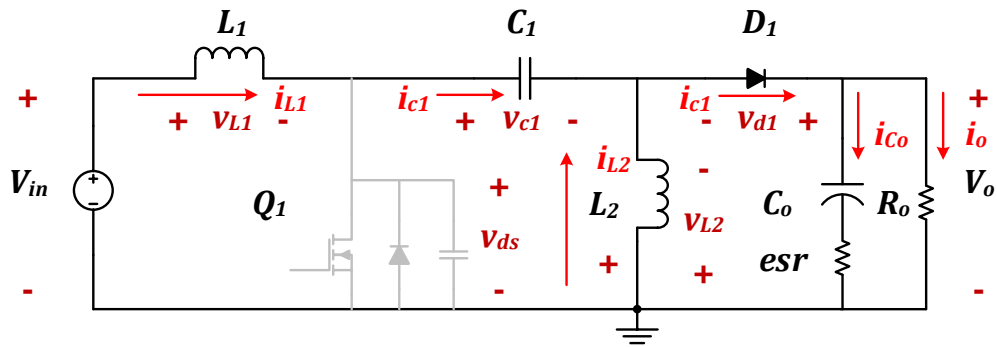
(a) Interval D_1 T_s

(b) Interval D_2 T_s
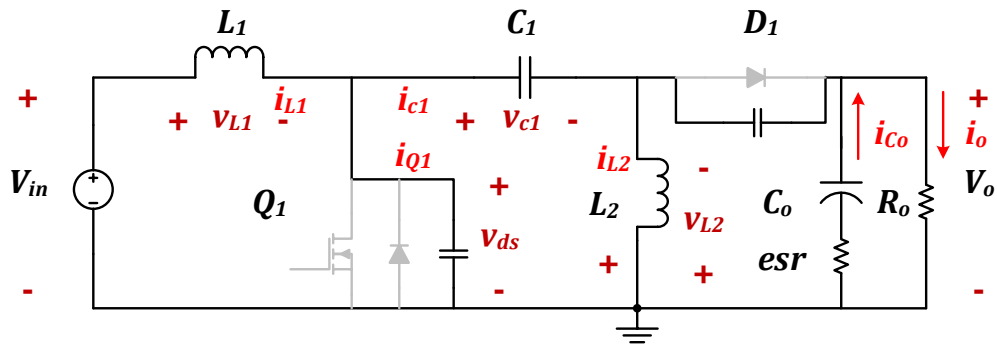
(c) Interval D_3 T_s

Figure 2.3 The equivalent circuits in three intervals

The equivalent circuits for three operation intervals are demonstrated in Figure 2.3. In the first interval D_1 T_s, the main switch is turned on. The input voltage V_{in} is applied to inductor L_1, and the capacitor voltage v_{c1} is applied to inductor L_2. The current of both inductors linearly increase if the voltage ripples on capacitor C_1 is neglected. There is no current flowing through the output rectifying diode D_1. The current flowing through the

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main switch is the sum of the two inductors' current. The load current is supplied by the output capacitor C_o.

The main switch Q_1 is turned off at the end of first interval. Then the converter enters the second interval $D_2 \cdot T_s$. The current flowing through the main switch Q_1 would be diverted to flow through the output rectifying diode D_1 since there is no other conducting path. During this interval, the voltage applied to both inductors is $-V_o$ if the voltage ripple on the capacitor C_1 is neglected. Thus both current decrease linearly. The current flowing through the output rectifying diode is also the sum of the two inductor's current. The load current is supplied by part of this current.

When the current flowing through the output diode D_1 decreases to zero, the converter enters the third interval $D_3 \cdot T_s$. Since both switch is off, the non-zero inductor current in DCM mode 1 would flow through the passive components L_1, C_1, L_2. Because the voltage on capacitor C_1 equals to input voltage V_g and C_1 is large enough to hold the voltage, ideally the current would stay constant. In DCM mode 2, since both current of the inductors are zero at the beginning of this interval, ideally the current would stay at zero. When considering the parasitic junction capacitors of the main switch Q_1 and the diode D_1, all the L-C components would form resonant tanks. Since the parasitic capacitances are usually quite small, high frequency ringing current and ringing voltage waveforms would be observed in reality.

From the energy transferring point of view, when the main switch Q_1 turns on, energy is transferred from the input voltage source to the inductor L_1 and stored in it, meanwhile part of the energy stored in capacitor C_1 is transferred to inductor L_2; and part of the energy stored in the output capacitor Co is transferred to the load. When switch Q1 turns off, the energy stored in inductor L_1, L_2 and the energy from the input voltage source are transferred to capacitor C_1, capacitor C_o and the load. In the third interval, in DCM mode 1, energy is transferred from the input voltage source to capacitor C_1 and the load is supported by output capacitor C_o; in DCM mode 2, ideally there is no energy transferred from the input voltage source to the system. To summarize, in DCM mode 1, the energy transferring from the input voltage source happens in all three intervals; while in DCM

mode 2, the energy transferring from the input voltage source is only happens in the first and second intervals. In common, the energy from the input source is first stored in two inductors and then released to the load.

From the device stress point of view, the voltage stress of both the main active switch Q_1 and passive diode D_1 equals to the sum of input voltage and output voltage; the current stress of either semiconductor device equals to the sum of the two inductors' current, which are also illustrated in Figure 2.2.

2.2 Switching Averaged Model of DCM SEPIC

To further analyze the steady state voltage gain and characteristics of small signal transfer function of the DCM SEPIC converter, two methods could be adopted. For DCM mode 1, with the state-space variables averaging method [16] [17] [18] and the averaged PWM switch method [19][20][22], steady state voltage gain and small signal model can be derived. With an assumption of negligible voltage ripple on intermediate capacitor in SEPIC converter, these derivations should be the same. For the case when the intermediate capacitor is small, the steady state results from all the two methods can be inaccurate.

2.2.1 State-Space Variables Averaging Method

For the first interval, the time duration is D_1Ts, the equations are shown in (2.1).

$$D_1 \cdot T_S : \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_g \\[2mm] L_2 \dfrac{di_{L2}}{dt} = v_{c1} \\[2mm] C_1 \dfrac{dv_{c1}}{dt} = -i_{L2} \\[2mm] C_o \dfrac{dv_{co}}{dt} = -\dfrac{v_{co}}{esr + R_o} \end{cases} \qquad v_o = \frac{R_o}{esr + R_o} \cdot v_{co} \qquad (2.1)$$

For the second interval, the time duration is D_2Ts, the equations are shown in (2.2).

$$D_2 \cdot T_S : \begin{cases} L_1 \dfrac{di_{L1}}{dt} = v_g - v_{c1} + L_2 \dfrac{di_{L2}}{dt} \\[2mm] L_2 \dfrac{di_{L2}}{dt} = V_d - \left(i_{L1} + i_{L2}\right) \cdot \dfrac{R_o \cdot esr}{R_o + esr} - \dfrac{R_o}{R_o + esr} v_{co} \\[2mm] C_1 \dfrac{dv_{c1}}{dt} = i_{L1} \\[2mm] C_o \dfrac{dv_{co}}{dt} = \left(i_{L1} + i_{L2}\right) \cdot \dfrac{R_o}{R_o + esr} - \dfrac{v_{co}}{R_o + esr} \end{cases} \tag{2.2}$$

$$v_o = \left(i_{L1} + i_{L2}\right) \cdot \frac{R_o \cdot esr}{R_o + esr} + \frac{R_o}{R_o + esr} v_{co}$$

For the third interval, the time duration is $(1\text{-}D_1\text{-}D_2)Ts$, the equation is shown in (2.3). For simplicity, the parasitic junction capacitances are neglected.

$$D_3 : \begin{cases} \left(L_1 + L_2\right) \dfrac{di_{L1}}{dt} = v_g - v_{c1} \\[2mm] \left(L_1 + L_2\right) \dfrac{di_{L2}}{dt} = -v_g + v_{c1} \\[2mm] C_1 \dfrac{dv_{c1}}{dt} = i_{L1} = -i_{L2} \\[2mm] C_{co} \dfrac{dv_{co}}{dt} = -\dfrac{1}{esr + R_o} \cdot v_{co} \end{cases} \qquad v_o = \frac{R_o}{esr + R_o} \cdot v_{co} \tag{2.3}$$

After some algebraic manipulation, the equations can be rearranged in canonical form.

$$\dot{x} = A \cdot x + B \cdot u \qquad y = c^T \cdot x \tag{2.4}$$

Where the state variables and output variables are defined as: $x = \begin{bmatrix} i_{L1} \\ i_{L2} \\ v_{c1} \\ v_{co} \end{bmatrix}$, $u = v_g$, $y = v_o$. The corresponding matrices for three intervals are designated as A_1, b_1, C_1, A_2, b_2, C_2 and A_3, b_3, C_3. With the switching cycle averaging concept, the form of averaged state space model is shown in (2.8), where $\langle x \rangle, \langle y \rangle$ denote switching averaged value.

$$A_1 = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \dfrac{1}{L_2} & 0 \\ 0 & -\dfrac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & -\dfrac{1}{C_o \cdot (esr + R_o)} \end{bmatrix}, b_1 = \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, c_1 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \dfrac{R_o}{esr + R_o} \end{bmatrix} \qquad (2.5)$$

$$A_2 = \dfrac{1}{(R_o + esr)} \begin{bmatrix} \dfrac{-R_o \cdot esr}{L_1} & \dfrac{-R_o \cdot esr}{L_1} & \dfrac{-(R_o + esr)}{L_1} & \dfrac{-R_o}{L_1} \\ \dfrac{-R_o \cdot esr}{L_2} & \dfrac{-R_o \cdot esr}{L_2} & 0 & \dfrac{-R_o}{L_2} \\ \dfrac{(R_o + esr)}{C_1} & 0 & 0 & 0 \\ \dfrac{R_o}{C_o} & \dfrac{R_o}{C_o} & 0 & -\dfrac{1}{C_o} \end{bmatrix}, \qquad (2.6)$$

$$b_2 = \begin{bmatrix} \dfrac{1}{L_1} \\ 0 \\ 0 \\ 0 \end{bmatrix}, c_2 = \begin{bmatrix} \dfrac{R_o \cdot esr}{R_o + esr} \\ \dfrac{R_o \cdot esr}{R_o + esr} \\ 0 \\ \dfrac{R_o}{R_o + esr} \end{bmatrix}$$

$$A_3 = \begin{bmatrix} 0 & 0 & \dfrac{-1}{L_1 + L_2} & 0 \\ 0 & 0 & \dfrac{1}{L_1 + L_2} & 0 \\ \dfrac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & \dfrac{-1}{C_o \cdot (esr + R_o)} \end{bmatrix}, b_3 = \begin{bmatrix} \dfrac{1}{L_1 + L_2} \\ \dfrac{-1}{L_1 + L_2} \\ 0 \\ 0 \end{bmatrix}, c_3 = \begin{bmatrix} 0 \\ 0 \\ 0 \\ \dfrac{R_o}{esr + R_o} \end{bmatrix} \qquad (2.7)$$

$$\langle \dot{x} \rangle = A \cdot \langle x \rangle + B \cdot \langle u \rangle \qquad \langle y \rangle = c^T \cdot \langle x \rangle \qquad (2.8)$$

The averaged variables within one switching cycle could be derived with integration of the whole switching cycle.

$$\frac{d\overline{x}}{dt} = \frac{1}{T_s}\int_0^{T_s}\dot{x}dt$$

$$A\cdot\overline{x} = \frac{1}{T_s}\left[A_1\cdot\int_0^{D_1T_s}xdt + A_2\cdot\int_{D_1T_s}^{D_1T_s+D_2T_s}xdt + A_3\cdot\int_{D_1T_s+D_2T_s}^{T_s}xdt\right]$$

$$B\cdot\overline{u} = \frac{1}{T_s}\left[b_1\cdot\int_0^{D_1T_s}udt + b_2\cdot\int_{D_1T_s}^{D_1T_s+D_2T_s}udt + b_3\cdot\int_{D_1T_s+D_2T_s}^{T_s}udt\right] \tag{2.9}$$

$$\overline{y} = \frac{1}{T_s}\left[c_1^T\cdot\int_0^{D_1T_s}xdt + c_2^T\cdot\int_{D_1T_s}^{D_1T_s+D_2T_s}xdt + c_3^T\cdot\int_{D_1T_s+D_2T_s}^{T_s}xdt\right]$$

In DCM mode, because the averaged current in one switching cycle is different to the averaged current within one interval, the integration of inductor current over each interval can no longer be simply expressed as the product of switching cycle averaged current and duty cycle. Based on the inductors' current waveforms, the integration results in every intervals could be derived as (2.10). The averaged current of one switching cycle is also derived as (2.11) to show the difference.

$$\int_0^{D_1T_s}i_{L1}dt = \left(I_r + \Delta i_{L1}\right)\cdot D_1\cdot T_s, \quad \int_0^{D_1T_s}i_{L2}dt = \left(-I_r + \Delta i_{L2}\right)\cdot D_1\cdot T_s,$$

$$\int_{D_1T_s}^{D_1T_s+D_2T_s}i_{L1}dt = \left(I_r + \Delta i_{L1}\right)\cdot D_2\cdot T_s, \quad \int_{D_1T_s}^{D_1T_s+D_2T_s}i_{L2}dt = \left(-I_r + \Delta i_{L2}\right)\cdot D_2\cdot T_s, \tag{2.10}$$

$$\int_{D_1T_s+D_2T_s}^{T_s}i_{L1}dt = I_r\cdot D_3\cdot T_s, \quad \int_{D_1T_s+D_2T_s}^{T_s}i_{L2}dt = -I_r\cdot D_3\cdot T_s$$

$$\frac{1}{T_s}\int_0^{T_s}i_{L1}dt = I_r + \left(D_1 + D_2\right)\cdot\Delta i_{L1},$$

$$\frac{1}{T_s}\int_0^{T_s}i_{L2}dt = -I_r + \left(D_1 + D_2\right)\cdot\Delta i_{L2} \tag{2.11}$$

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By assuming the output voltage ripples are negligible compared to the averaged value, the integration of output capacitor voltage for every interval can be expressed as product of averaged voltage and duty cycle of corresponding intervals.

$$\int_0^{D_1T_s} v_{co}dt = \overline{v}_{co} \cdot D_1 \cdot T_s,$$

$$\int_{D_1T_s}^{D_1T_s+D_2T_s} v_{co}dt = \overline{v}_{co} \cdot D_2 \cdot T_s, \tag{2.12}$$

$$\int_{D_1T_s+D_2T_s}^{T_s} v_{co}dt = \overline{v}_{co} \cdot D_3 \cdot T_s$$
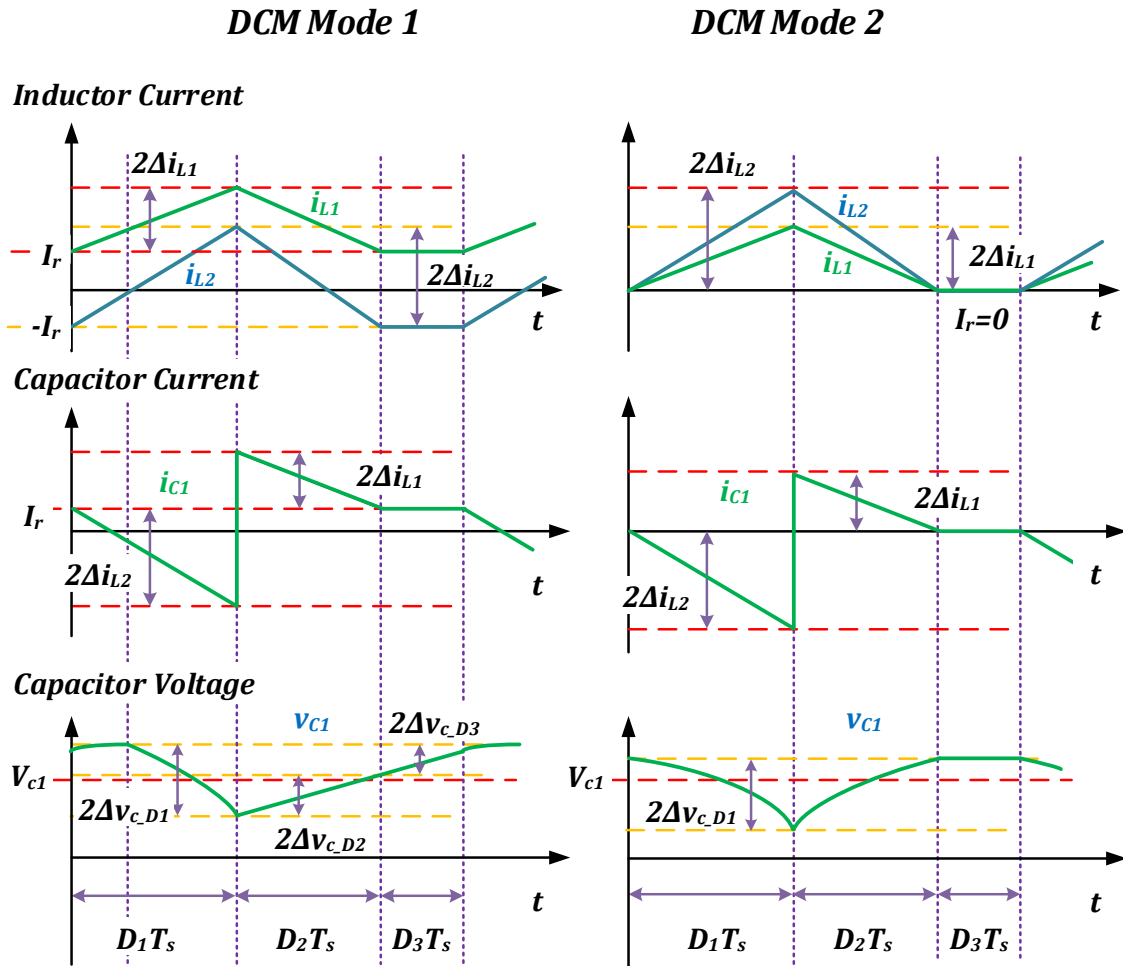
Figure 2.4 The voltage ripple of the intermediate capacitor C_1

For the intermediate capacitor C_1, when small capacitance is selected, the negligible voltage ripple assumption would be not applicable. As shown in Figure 2.4, in the first interval $D_1 \cdot T_s$, intermediate capacitor C_1 resonates with inductor L_2; in the second interval $D_2 \cdot T_s$, intermediate capacitor C_1 resonates with inductor L_1; in the third interval $D_3 \cdot T_s$, intermediate capacitor C_1 resonates with series connected inductors L_1 and L_2. According to the first mean value theorem for integration, the mean value of intermediate capacitor voltage in each interval can be expressed as (2.13). δv_{c1_D1}, δv_{c1_D2}, δv_{c1_D3} denote the difference between interval mean value and cycle mean value.

$$\int_0^{D_1 T_s} v_{c1} dt = \left(\bar{v}_{c1} + \delta v_{c1\_D1} \right) \cdot D_1 \cdot T_s ,$$

$$\int_{D_1 T_s}^{D_1 T_s + D_2 T_s} v_{c1} dt = \left(\bar{v}_{c1} + \delta v_{c\_D2} \right) \cdot D_2 \cdot T_s ,$$

$$\int_{D_1 T_s + D_2 T_s}^{T_s} v_{c1} dt = \left(\bar{v}_{c1} + \delta v_{c\_D3} \right) \cdot D_3 \cdot T_s ,$$

$$\frac{1}{T_S} \int_0^{T_s} v_{c1} dt = \bar{v}_{c1} + \left(\delta v_{c\_D1} \cdot D_1 + \delta v_{c\_D2} \cdot D_2 + \delta v_{c\_D3} \cdot D_3 \right) = \bar{v}_{c1}$$

(2.13)

Combined equations (2.5)~ (2.13), the averaged model of DCM SEPIC converter could be derived as (2.14). The steady state operating point could be solved based on the averaged model. By making $\dot{\bar{x}} = 0$, $\bar{v}_o = V_o$, $\bar{v}_g = V_g$ and $\bar{v}_{c1} = V_{c1}$, the averaged solution of state variables are shown in (2.15), (2.16) and (2.17).

Equation (2.16) shows the voltage ripple of the intermediate capacitor and the equivalent series resistance of output capacitor would affect the relationship between D_1 and D_2. If the impact from the intermediate capacitor voltage ripple and equivalent series resistance of output capacitor are neglected, the derived relationship between duty cycle D_1 and D_2 can be much simpler, as shown in (2.17).

In the third interval, since the current flowing through the intermediate capacitor is the remaining current I_r in DCM mode 1, the interval mean voltage would be larger than

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mean voltage of switching cycle. δv_{c_D3} must be positive value. The final solution for steady state duty cycle is shown in (2.19).

$$\frac{d}{dt}\begin{bmatrix} \overline{i}_{L1} \\ \overline{i}_{L2} \\ \overline{v}_{C1} \\ \overline{v}_{Co} \end{bmatrix} = A \cdot \begin{bmatrix} \overline{i}_{L1} \\ \overline{i}_{L2} \\ \overline{v}_{C1} \\ \overline{v}_{Co} \end{bmatrix} + b \cdot \overline{v}_g$$

$A \cdot \overline{x} =$

$$\begin{bmatrix} \dfrac{-D_3 \cdot \left(\overline{v}_{C1} + \delta v_{c\_D3}\right)}{L_1 + L_2} - \dfrac{D_2 \cdot \left(\overline{v}_{C1} + \delta v_{c\_D2}\right)}{L_1} - \dfrac{R_o \cdot D_2 \cdot \left[\overline{v}_{Co} + esr \cdot \left(\Delta i_{L1} + \Delta i_{L2}\right)\right]}{L_1 \cdot \left(R_o + esr\right)} \\[4mm] \dfrac{D_3 \cdot \left(\overline{v}_{C1} + \delta v_{c\_D3}\right)}{L_1 + L_2} + \dfrac{D_1 \cdot \left(\overline{v}_{C1} + \delta v_{c\_D1}\right)}{L_2} - \dfrac{R_o \cdot D_2 \cdot \left[\overline{v}_{Co} + esr \cdot \left(\Delta i_{L1} + \Delta i_{L2}\right)\right]}{L_2 \cdot \left(R_o + esr\right)} \\[4mm] \dfrac{I_r - D_1 \Delta i_{L2} + D_2 \Delta i_{L1}}{C_1} \\[4mm] \dfrac{-\overline{v}_{Co} + R_o \cdot D_2 \left(\Delta i_{L1} + \Delta i_{L2}\right)}{C_o \cdot \left(R_o + esr\right)} \end{bmatrix} \qquad \textbf{(2.14)}$$

$$b \cdot \overline{v}_g = \begin{bmatrix} \dfrac{D_3}{L_1 + L_2} + \dfrac{\left(D_1 + D_2\right)}{L_1} \\[4mm] \dfrac{-D_3}{L_1 + L_2} \\[4mm] 0 \\[2mm] 0 \end{bmatrix} \cdot \overline{v}_g,$$

$$\overline{v}_o = \frac{R_o}{R_o + esr} \cdot \left[\overline{v}_{co} + D_2 \cdot esr \left(\Delta i_{L1} + \Delta i_{L2}\right)\right]$$

$$V_{c1} = V_g,\ V_{Co} = V_o,\ \left(\Delta i_{L1} + \Delta i_{L2}\right) = \frac{1}{D_2} \cdot \frac{V_o}{R_o},\ I_r = D_1 \Delta i_{L2} - D_2 \Delta i_{L1}$$

$$\qquad \textbf{(2.15)}$$

$$\Delta i_{L1} = \frac{D_1 T_s}{2} \cdot \frac{V_g}{L_1},\ \Delta i_{L2} \approx \frac{D_1 T_s}{2} \cdot \frac{V_g}{L_2} \Rightarrow D_1 \cdot D_2 \approx \frac{V_o}{V_g} \cdot \frac{2 \cdot L_1 \cdot L_2}{R_o \cdot \left(L_1 + L_2\right) \cdot T_s}$$

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$$D_2 \cdot \delta v_{c3} \frac{L_2}{L_1 + L_2} = D_2 \cdot V_o \cdot \frac{R_o + esr/D_2}{R_o + esr} - D_1 \cdot V_g \tag{2.16}$$

$$D_2 \cdot V_o - D_1 \cdot V_g = 0 \tag{2.17}$$

$$D_1 = D_2 \cdot \left(\frac{V_o}{V_g} \cdot \frac{R_o + esr/D_2}{R_o + esr} - \frac{\delta v_{c3}}{V_g} \cdot \frac{L_2}{L_1 + L_2} \right)$$

$$D_1 = \sqrt{\frac{V_o}{V_g} \cdot \frac{2 \cdot L_1 \| L_2}{R_o \cdot T_s} \cdot \left(\frac{V_o}{V_g} \cdot \frac{R_o + esr/D_2}{R_o + esr} - \frac{\delta v_{c3}}{V_g} \cdot \frac{L_2}{L_1 + L_2} \right)}$$

$$\leq \frac{V_o}{V_g} \cdot \sqrt{\frac{2 \cdot L_1 \| L_2}{R_o \cdot T_s}} \tag{2.18}$$

$$D_2 = \sqrt{\frac{\dfrac{V_o}{V_g} \cdot \dfrac{2 \cdot L_1 \| L_2}{R_o \cdot T_s}}{\left(\dfrac{V_o}{V_g} \cdot \dfrac{R_o + esr/D_2}{R_o + esr} - \dfrac{\delta v_{c3}}{V_g} \cdot \dfrac{L_2}{L_1 + L_2} \right)}} \approx \sqrt{\frac{2 \cdot L_1 \| L_2}{R_o \cdot T_s}}$$

$$\begin{cases} \text{Boundary: } (\Delta i_{L1} + \Delta i_{L2}) \cdot (1 - D_1) = \dfrac{V_o}{R_o} \Rightarrow D_1 + D_2 = 1 \\[3mm] \text{CCM: } (\Delta i_{L1} + \Delta i_{L2}) \cdot (1 - D_1) \leq \dfrac{V_o}{R_o} \Rightarrow L_1 \| L_2 \cdot \dfrac{f_s}{R_o} \geq \dfrac{1}{2} \cdot \dfrac{V_g^2}{\left(V_o + V_g \right)^2} \\[3mm] \text{DCM: } (\Delta i_{L1} + \Delta i_{L2}) \cdot (1 - D_1) \geq \dfrac{V_o}{R_o} \Rightarrow L_1 \| L_2 \cdot \dfrac{f_s}{R_o} \leq \dfrac{1}{2} \cdot \dfrac{V_g^2}{\left(V_o + V_g \right)^2} \end{cases} \tag{2.19}$$

From (2.15), the solution for the mean value I_r of remaining current shows DCM mode #2 is a special case of DCM mode #1. When the ratio of inductance L_1 to inductance L_2 equals to the ratio of input voltage V_g to output voltage V_o, the interval mean value of remaining current would be zero, the circuit operates at DCM mode #2.

From (2.18), it's clear that the ESR of the output capacitor would increases D_1, while the voltage ripples on the intermediate capacitor decreases D_1. Thus when the intermediate capacitor is small or the ESR of output capacitor is not negligible, traditional

state space averaged model [16] would not be able to provide an accurate solution of the steady-state variables. With the assumption of negligible voltage ripple on intermediate capacitor, duty cycle D_1 derived from conventional model would be the simplified result shown in (2.18). With the averaging method provided above, the accuracy could be improved.

The CCM-DCM boundary criterion is presented in (2.19). Boundary operation occurs when the output diode current decreases to zero at the end of the switching cycle. Thus the third interval $D_3 \cdot T_s$ would be zero; the second interval $D_2 \cdot T_s$ would equal to (1-D_1)$\cdot T_s$. Based on the averaged diode current in the second interval, the boundary condition can be derived.

Based on all these steady-state value, the small signal model could be derived through perturbation procedure. Due to the complexity of this four order system, the small signal transfer function is derived through another averaging method, which is the averaged PWM switch model.

2.2.2 Averaged PWM Switch Method

Based on the work of Dr. Vorperian [18], the switching cell can be replaced with an equivalent linear block, which is named as averaged PWM switch.

In Figure 2.5 (a), active, passive and common connection point are first identified in SEPIC converter. Then the equivalent averaged linear circuit can be derived by replacing the active and passive switch with the PWM switch as shown in Figure 2.5 (b). The averaged circuit in (b) contains both the averaged DC steady state and small signal dynamic characteristics of the original SEPIC converter. For averaged DC steady state, since the averaged DC voltage applied to inductor would be zero and the averaged DC current flowing through capacitor would be zero, the averaged DC steady state circuit can be acquired by shorting the connection of inductors and opening the connection of capacitors, as shown in Figure 2.5 (c). For small signal dynamic characteristics, small signal model of PWM switch is inserted as Figure 2.5 (d).

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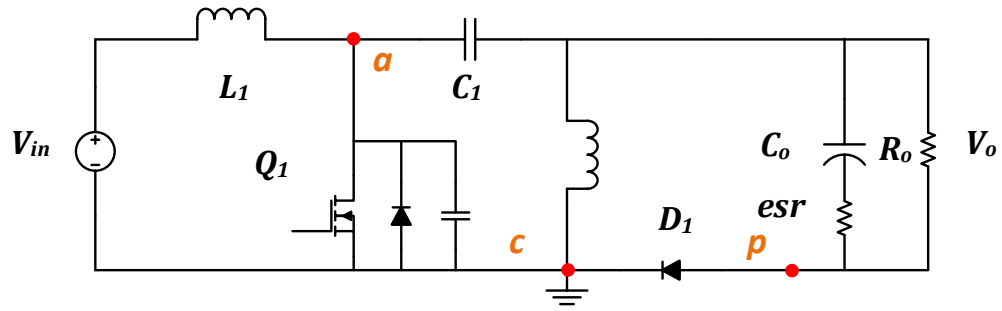
(a) a, c, p port
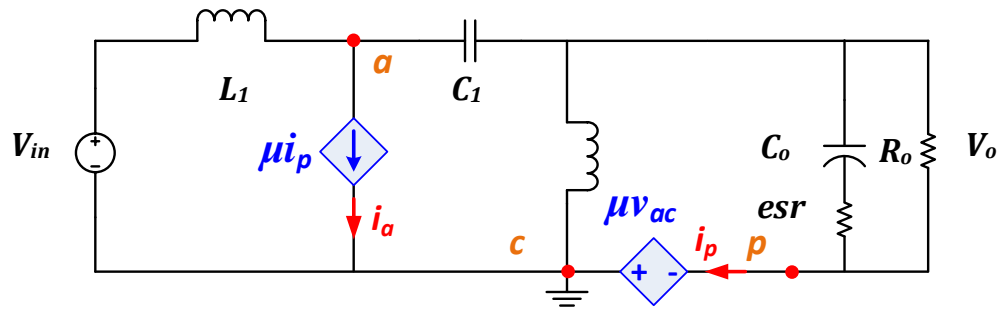
(b) Equivalent Averaged Circuit
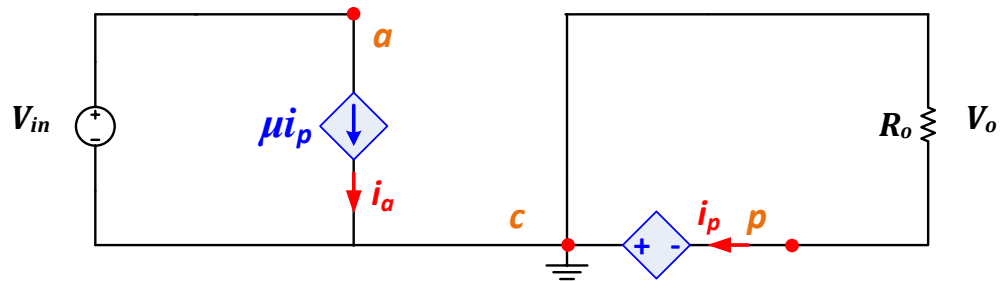
(c) DC Averaged Steady State
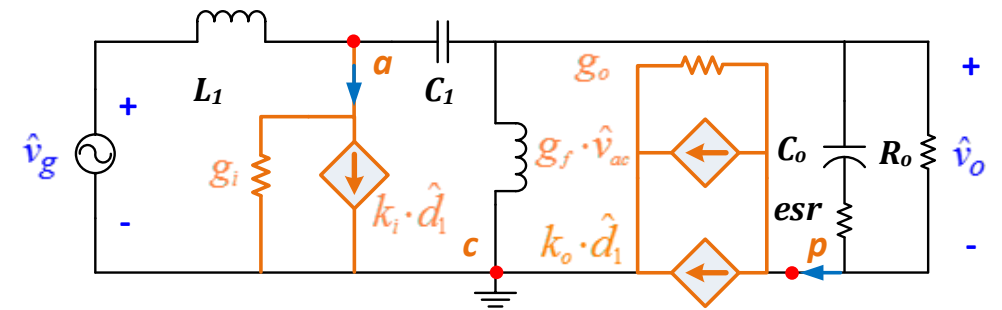
(d) Equivalent Circuit for Small Signal

Figure 2.5 The averaged equivalent circuit with PWM switch

From the PWM switch model, current and voltage relationship for the two controlled source can be expressed as (2.20). Compare the averaged linear circuit with the original SEPIC circuit, clearly i_a is the averaged current flowing through the active switch, and i_p is the averaged current flowing through output rectifier diode; v_{ac} and v_{cp} are the averaged voltage applied on a-c and c-p port. Combined with the key waveform shown in Figure 2.2, expression of the averaged current and voltage can be derived as (2.20) and (2.21).

$$\begin{cases} i_a = \mu \cdot i_p \\ v_{cp} = \mu \cdot v_{ac} \end{cases}, \begin{cases} i_a = \dfrac{d_1}{2}(2\Delta i_{L1} + 2\Delta i_{L2}) = d_1(\Delta i_{L1} + \Delta i_{L2}) \\[2mm] i_p = \dfrac{d_2}{2}(2\Delta i_{L1} + 2\Delta i_{L2}) = d_2(\Delta i_{L1} + \Delta i_{L2}) \\[2mm] v_{ac} = L_1 \dfrac{2 \cdot \Delta i_{L1}}{d_1 T_s} = L_2 \dfrac{2 \cdot \Delta i_{L2}}{d_1 T_s} \\[2mm] v_{cp} = L_1 \dfrac{2 \cdot \Delta i_{L1}}{d_2 T_s} = L_2 \dfrac{2 \cdot \Delta i_{L2}}{d_2 T_s} \end{cases} \tag{2.20}$$

Combined (2.19), (2.20) and the DC steady state equivalent circuit, the voltage gain of DCM SEPIC can be derived as (2.21). Then the DC steady state duty cycle can be solved as (2.22).

$$\begin{cases} i_a = \dfrac{d_1^2}{2 \cdot L_1 \| L_2 \cdot f_s} v_{ac} \\[3mm] i_p = \dfrac{d_2^2}{2 \cdot L_1 \| L_2 \cdot f_s} v_{cp} \\[3mm] v_{ac} = \dfrac{d_2}{d_1} v_{cp} \\[3mm] i_a = \dfrac{d_1}{d_2} i_p \end{cases}, \quad L_1 \| L_2 = \dfrac{L_1 \cdot L_2}{L_1 + L_2} \tag{2.21}$$

$$\mu = \frac{d_1}{d_2} = \frac{V_o}{V_g} = \frac{D_1^2}{2 \cdot L_1 \| L_2 \cdot f_{sw}} \frac{V_{ac}}{I_p} = \frac{D_1^2}{\dfrac{2L_1 \| L_2 \cdot f_{sw}}{R_o}} \frac{V_g}{R_o I_o} = \frac{D_1^2 \cdot R_o}{2L_1 \| L_2 \cdot f_{sw}} \frac{V_g}{V_o} \tag{2.22}$$

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$$D_1 = \frac{V_o}{V_g} \cdot \sqrt{\frac{2 \cdot L_1 \cdot L_2}{R_o \cdot (L_1 + L_2) \cdot T_s}} , \quad D_2 = \sqrt{\frac{2 \cdot L_1 \cdot L_2}{R_o \cdot (L_1 + L_2) \cdot T_s}} \qquad \textbf{(2.23)}$$

With the DC steady state solution, small signal model can be derived by introducing perturbation on averaged steady state current i_a and i_p as shown in (2.24) and (2.25).

$$\begin{cases} i_a = \dfrac{d_1^2}{2 \cdot L_1 \| L_2 \cdot f_s} \cdot v_{ac} \\[4mm] i_p = \dfrac{d_1^2}{2 \cdot L_1 \| L_2 \cdot f_s} \cdot \dfrac{v_{ac}^2}{v_{cp}} \end{cases} \qquad \textbf{(2.24)}$$

$$\begin{cases} I_a + \hat{i}_a \approx \dfrac{(D_1 + \hat{d}_1)^2}{2 \cdot L_1 \| L_2 \cdot f_s}(V_{ac} + \hat{v}_{ac}) \\[4mm] I_p + \hat{i}_p \approx \dfrac{(D_1 + \hat{d}_1)^2}{2 \cdot L_1 \| L_2 \cdot f_s}(V_{ac} + \hat{v}_{ac})^2(\dfrac{1}{V_{cp} + \hat{v}_{cp}}) \\[4mm] \qquad \approx \dfrac{1}{2 \cdot L_1 \| L_2 \cdot f_s}(D_1^2 + 2D_1\hat{d}_1)(V_{ac}^2 + 2V_{ac}\hat{v}_{ac})(\dfrac{1}{V_{cp}} - \dfrac{1}{V_{cp}^2}\hat{v}_{cp}) \end{cases} \qquad \textbf{(2.25)}$$

By removing the steady state DC variables, the equivalent circuit shown in Figure 2.5 (d) can be derived as (2.26). All the coefficients are presented in (2.27).

$$\begin{cases} \hat{i}_a \approx \dfrac{2D_1 V_{ac}}{2 \cdot L_1 \| L_2 \cdot f_s}\hat{d}_1 + \dfrac{D_1^2}{2 \cdot L_1 \| L_2 \cdot f_s}\hat{v}_{ac} = \dfrac{I_a}{V_{ac}}\hat{v}_{ac} + \dfrac{2I_a}{D_1}\hat{d}_1 = g_i\hat{v}_{ac} + k_i\hat{d}_1 \\[4mm] \hat{i}_p \approx \dfrac{1}{2 \cdot L_1 \| L_2 \cdot f_s}\left[D_1^2 \cdot \dfrac{1}{V_{cp}} \cdot 2V_{ac}\hat{v}_{ac} + V_{ac}^2 \cdot \dfrac{1}{V_{cp}} \cdot 2D_1\hat{d}_1 - D_1^2 V_{ac}^2 \dfrac{1}{V_{cp}^2}\hat{v}_{cp} \right] \\[4mm] \qquad \approx \dfrac{2I_p}{V_{ac}}\hat{v}_{ac} + \dfrac{2I_p}{D_1}\hat{d}_1 - \dfrac{I_p}{V_{cp}}\hat{v}_{cp} = g_f\hat{v}_{ac} + k_0\hat{d}_1 - g_o\hat{v}_{cp} \end{cases} \qquad \textbf{(2.26)}$$

With KCL and KVL, transfer function of duty cycle to output voltage can be derived as (2.28). The corresponding coefficients are shown in (2.29).

$$g_i = \frac{D_1^2}{2 \cdot L_1 \| L_2 \cdot f_s} = \frac{I_a}{V_{ac}} = \frac{V_o^2}{V_{in}^2 \cdot R_o}$$

$$k_i = \frac{2 D_1 V_{ac}}{2 \cdot L_1 \| L_2 \cdot f_s} = \frac{2 I_a}{D_1} = \frac{D_1 V_{in}}{L_1 \| L_2 \cdot f_s}$$

$$g_f = \frac{D_1^2 \cdot \dfrac{1}{V_{cp}} \cdot 2 V_{ac}}{2 \cdot L_1 \| L_2 \cdot f_s} = \frac{2 \cdot V_o}{V_{in} \cdot R_o} \tag{2.27}$$

$$k_0 = \frac{V_{ac}^2 \cdot \dfrac{1}{V_{cp}} \cdot 2 D_1}{2 \cdot L_1 \| L_2 \cdot f_s} = \frac{2 I_p}{D_1} = \frac{V_{in}^2 \cdot D_1}{V_o \cdot L_1 \| L_2 \cdot f_s}$$

$$g_o = \frac{D_1^2 V_{ac}^2 \dfrac{1}{V_{cp}^2}}{2 \cdot L_1 \| L_2 \cdot f_s} = \frac{1}{R_o}$$

$$\frac{\hat{v}_o}{\hat{d}_1} = \frac{N(s)}{D(s)}$$

$$\tag{2.28}$$

$$N(s) = R_L \cdot (s \cdot C_o \cdot esr + 1) \cdot (b_3 \cdot s^3 + b_2 \cdot s^2 + b_1 \cdot s^1 + b_0),$$

$$D(s) = (a_4 \cdot s^4 + a_3 \cdot s^3 + a_2 \cdot s^2 + a_1 \cdot s + a_0)$$

$$b_3 = C_x L_1 L_2 \left(g_i \cdot k_o - g_f \cdot k_i - g_o \cdot k_i \right)$$
$$b_2 = C_x \left(L_1 + L_2 \right) k_o$$
$$b_1 = L_1 \left(g_i \cdot k_o - g_f \cdot k_i \right) \qquad ,$$
$$b_0 = k_o$$

$$a_4 = C_o C_x L_1 L_2 \cdot \left[(R_L + esr)(g_i + g_f + g_o) + g_i g_o \cdot esr \cdot R_o \right]$$
$$a_3 = C_x L_1 L_2 \left(g_i + g_f + g_o + g_i g_o \cdot R_o \right) \tag{2.29}$$
$$\quad + C_o \cdot \left[(R_o + esr)(C_x L_1 + C_x L_2 + L_1 L_2 g_i g_o) + C_x \cdot esr \cdot R_o \cdot g_o (L_1 + L_2) \right]$$
$$a_2 = \left[C_x L_1 + C_x L_2 + L_1 L_2 g_i g_o + R_o C_x \left(L_1 + L_2 \right) g_o \right]$$
$$\quad + C_o \left[(L_1 g_i + L_2 g_o)(R_o + esr) + R_o \cdot esr \cdot L_1 g_i g_o \right]$$
$$a_1 = \left(L_1 g_i + L_2 g_o + R_o L_1 g_i g_o \right) + C_o (R_o + esr) + R_o \cdot C_o \cdot esr \cdot g_o$$
$$a_0 = 1 + R_o g_o$$

2.3 Model Validation
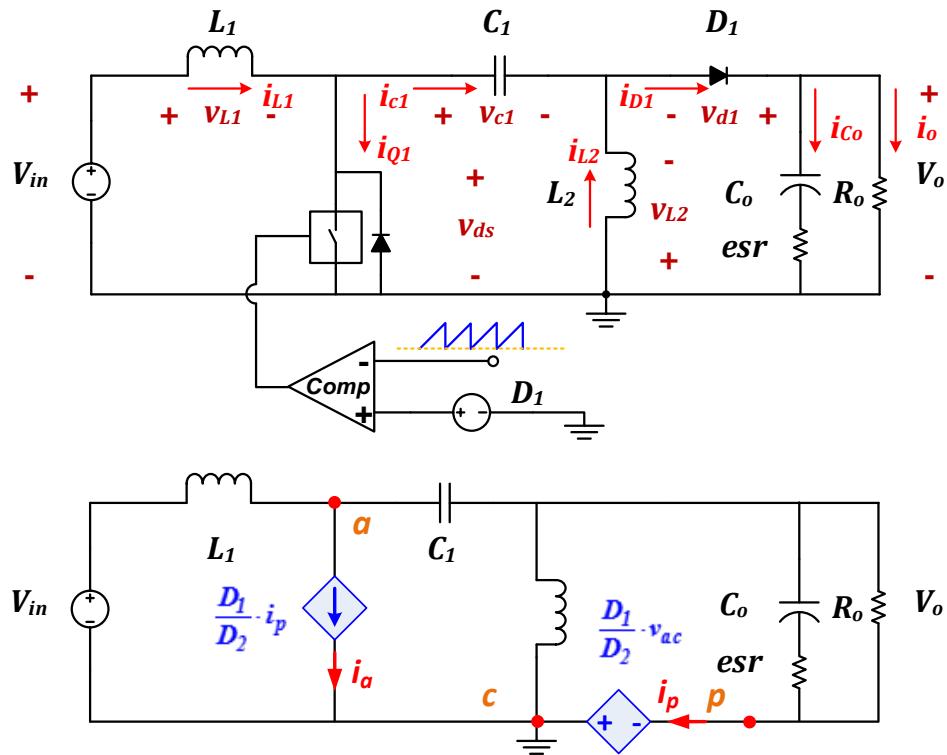
Figure 2.6 Simulation diagram for steady state model verification

Simulation circuits in SIMPLIS are built to verify both the DC steady state and small signal dynamic characteristics of the derived model as shown in Figure 2.6. Three sets of parameters are used to show the impact from non-negligible voltage ripple of intermediate capacitor and equivalent series resistance of output capacitor. Parameters and electrical specification of the SEPIC converter are listed in TABLE. 2.1.

TABLE. 2.1 DC-DC SEPIC simulation parameters

	#1	#2	#3
Input Voltage V_{in} (V)	100	100	100
Output Voltage V_o (V)	**100**	**100**	**50**
Power P_o (W)	1000	1000	1000
Switching Frequency (kHz)	100	100	100

Inductor L_1 (μH)	168	168	168
Inductor L_2 (μH)	4.2	4.2	4.2
Capacitor C_1 (μF)	**1**	**3000**	**3000**
Capacitor C_o (mF)	4	4	4
Equivalent Series Resistance ESR (mΩ)	15	15	15
(2.24) Estimated Duty D_1	**0.2863**	**0.2863**	**0.2863**
Actual Duty D_1 in Simulation	**0.2581**	**0.2861**	**0.2864**
μ=D_1/D_2 for averaged model	**1**	**1**	**0.5**

With (2.24), duty cycles are first calculated and inserted into the simulation circuits for transient analysis. Key waveforms for DC steady state are compared. As shown in Figure 2.7, comparing case #1 to case #2, when intermediate capacitor is small (case #1), the voltage ripple is non-negligible, the estimated duty-cycle from (2.24) is larger than required, which results inaccurate estimation for averaged current of the input inductor and output voltage. As the intermediate capacitance increases (case #2), the estimated duty-cycle becomes more accurate. Meanwhile, comparing case #2 to case #3, as the output current increases, with same ESR, the loss increases, and the duty increases. The simulation results well validate previous discussion with state-space averaging model.
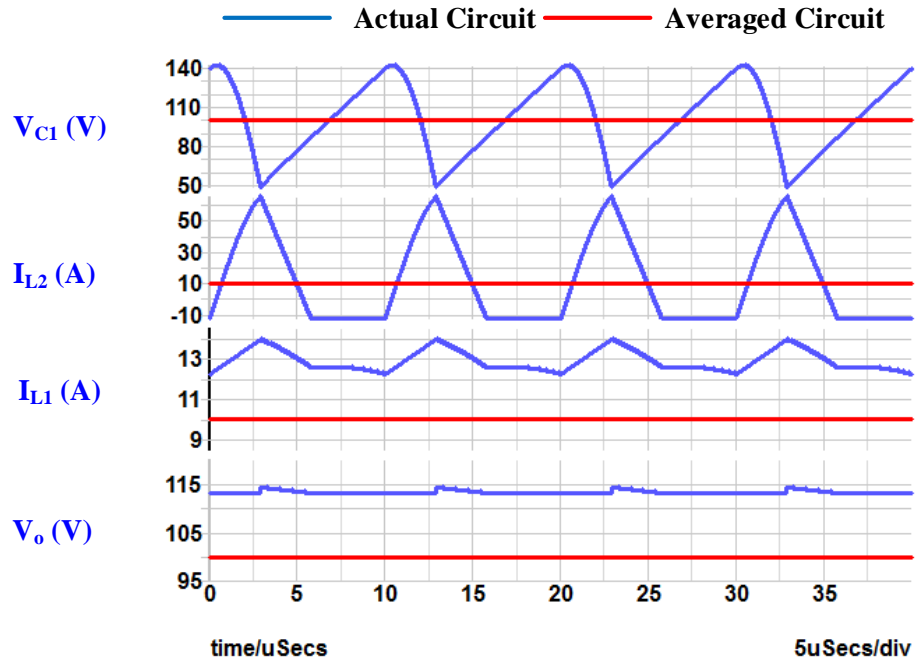
(a) Case#1 Steady-State with Estimated Duty
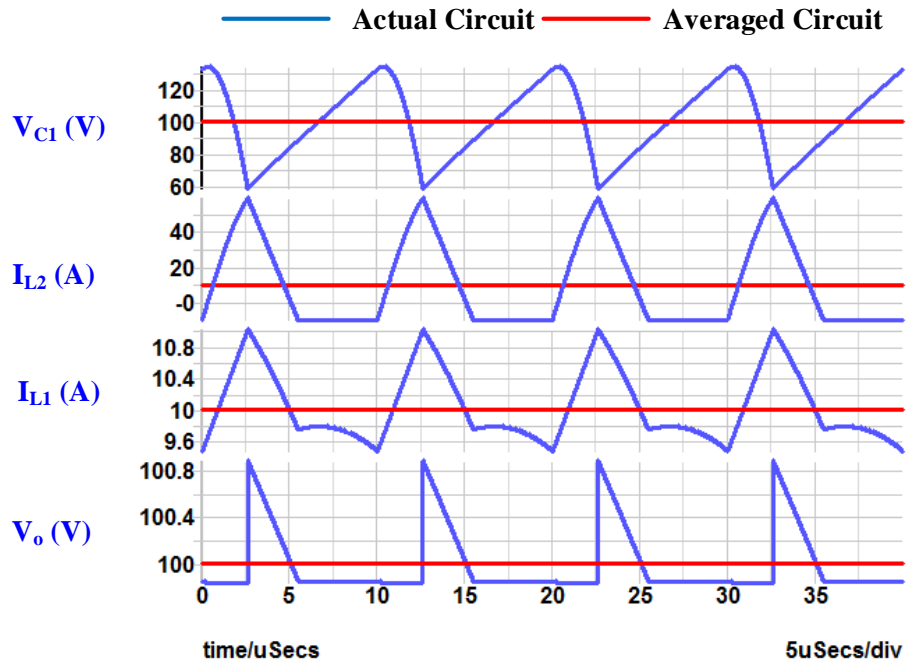
(b) Case#1 Steady-State with Modified Duty

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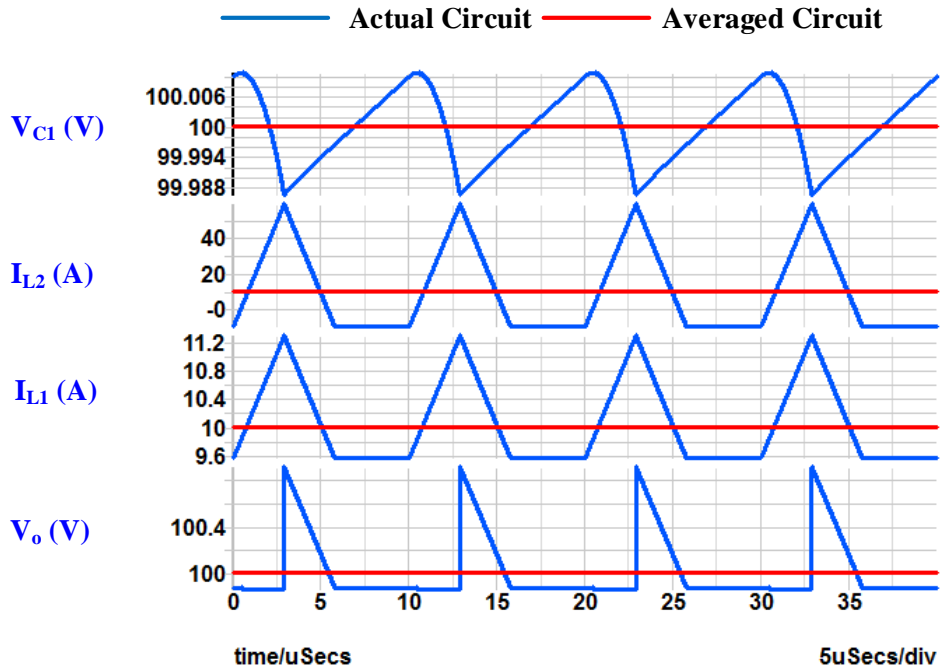
(c) Case#2 Steady-State with Modified Duty
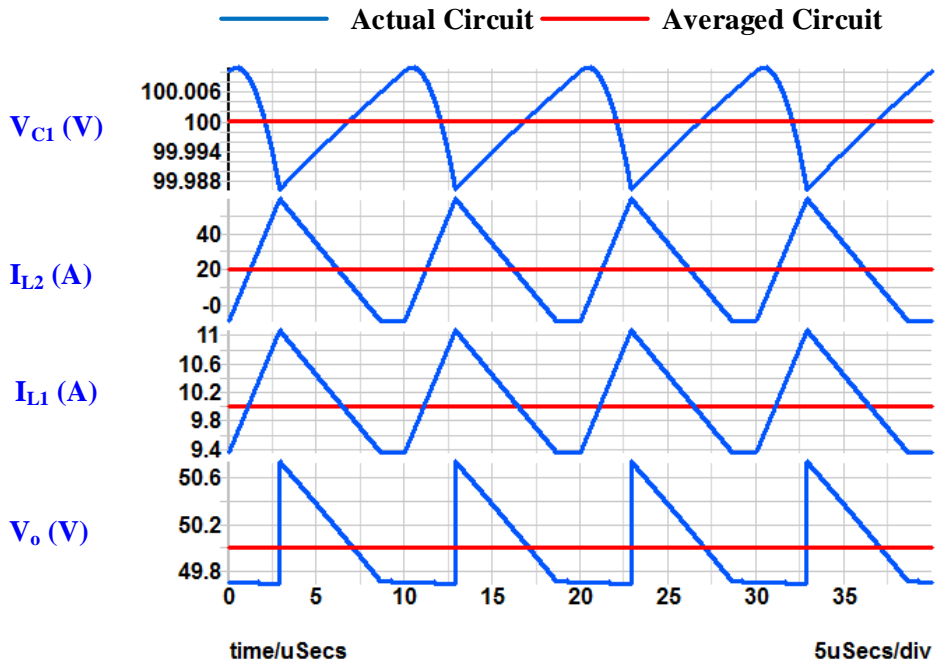
(d) Case#3 Steady-State with Modified Duty

Figure 2.7 Comparison of key waveforms for steady state

Through the simulation results, while the PWM switch model is simple to derive the DC steady state value and voltage gain, the accuracy of PWM switch model relies on an assumption of small voltage ripple on capacitor. If the voltage ripple is large enough, in another words, if the resonant frequency formed by inductor and capacitor loop is comparable to the switching frequency, the PWM switch model would be not accurate for steady state estimation. For the impact from ESR, equivalent resistor should be inserted into the PWM switch as the same way for CCM, and then the ESR impact could be estimated.
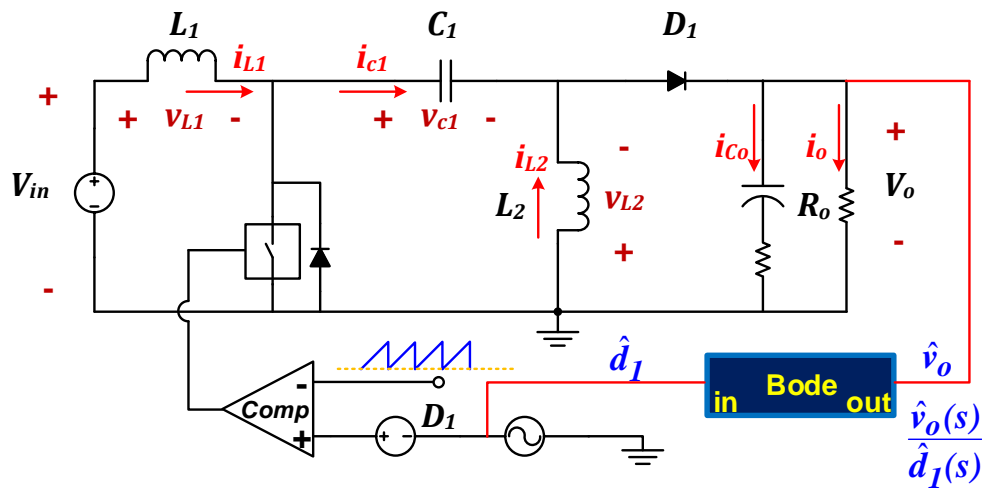
Figure 2.8 Simulation circuit diagram for AC analysis

With (2.28) and (2.29), small signal transfer function of active duty to output voltage can be calculated first, then corresponding bode plots are drawn and compared to the simulation results. The simulation circuit diagram for AC small signal analysis is shown in Figure 2.8. The comparison is shown in Figure 2.9.

From Figure 2.9, for case #1, when intermediate capacitor is small, the gain curve predicted from average model is slightly lower than simulation results, while the phase curve matches with simulation results until almost one third of the switching frequency. For case #2, since intermediate capacitor is large enough, both the gain curve and the phase curve predicted from averaged model exactly matches the simulation results until one third of the switching frequency. Thus the derived average model is valid.
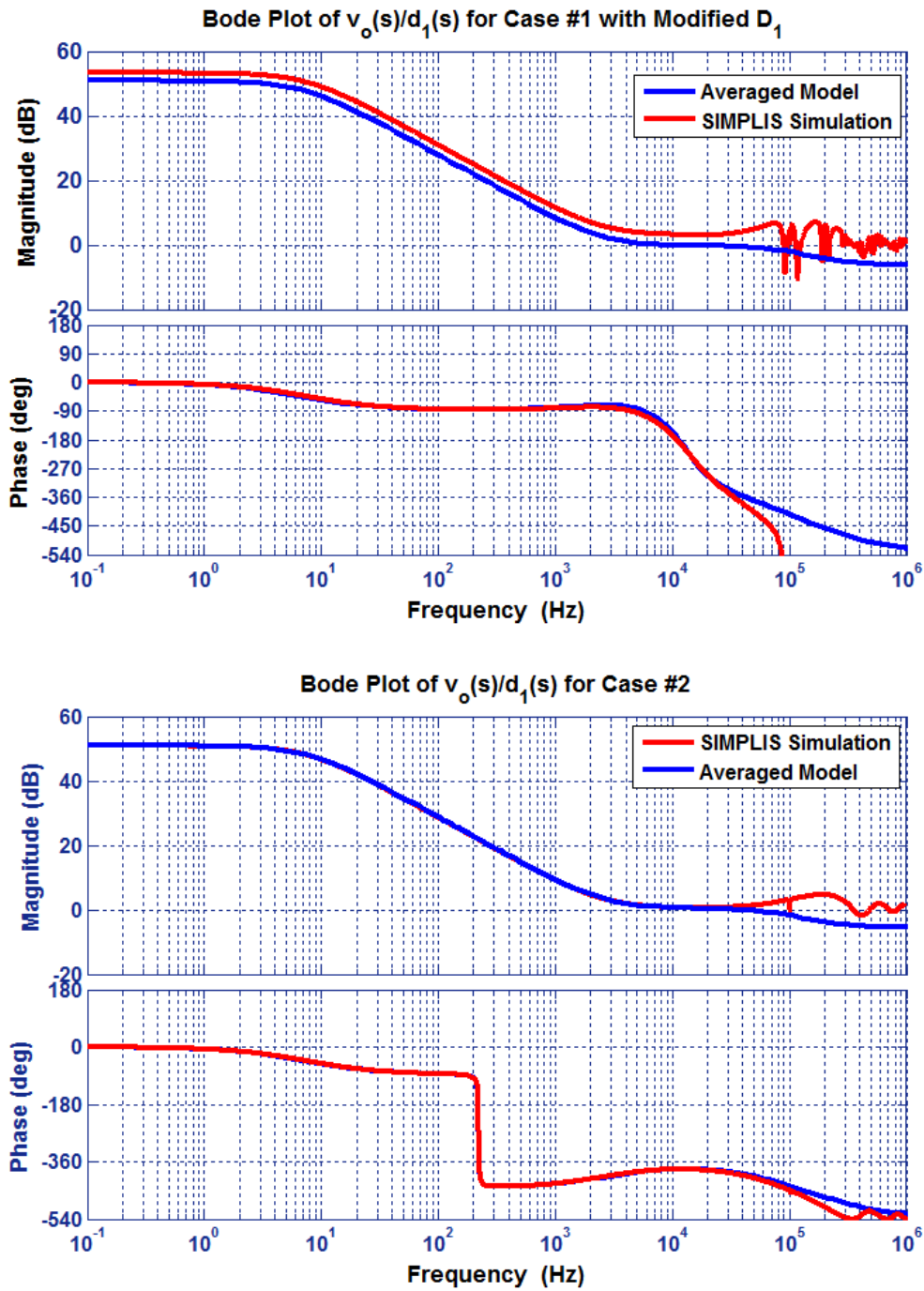
Figure 2.9 Bode plots comparison

Further analysis for the transfer function of active duty cycle to output voltage indicates the system is still fourth order. Four poles include two LHP (left half plane) real poles and a pair of LHP complex poles; four zeroes include one LHP ESR real zero, one

RHP real zero and a pair of RHP complex zeroes [18]. All the poles and zeros can be obtained through numerical method by solving (2.28) and (2.29).

At low frequency region, the dominating low frequency LHP real pole s_{p1}, which can be estimated with (2.30), makes the system behave like a first order system. Corresponding low frequency gain can be estimated with (2.31). Another single LHP real pole s_{p2} is shown in (2.33), whose frequency is close to or even higher than switching frequency. The ESR real LHP zero is also shown in (2.32).

The LHP complex poles and RHP complex zeroes are close to each other; the corresponding corner frequency can be approximated with ω_o [18], which is majorly determined by the intermediate capacitor and the two inductors. Increasing capacitance would result these LHP complex poles and RHP complex zeroes move towards lower frequency region, which can be observed from the bode plot of case #1 and #2. Together, the LHP complex poles and RHP complex zeroes result 360 degree phase drop within a narrow frequency range around the corner frequency ω_o. When the intermediate capacitor is large, the phase drop occurs in a quite stiff way; when the intermediate capacitor is small, the phase drop occurs in a relatively mild way.

$$s_{p1} = \frac{2}{R_o \cdot C_o} \tag{2.30}$$

$$Gain = \frac{V_g}{2} \cdot \sqrt{\frac{2 \cdot R_o}{L_1 \| L_2 \cdot f_{sw}}} \tag{2.31}$$

$$s_{z1} = \frac{1}{C_o \cdot esr} \tag{2.32}$$

$$s_{p2} = \frac{2 \cdot f_{sw}}{\left(D_1 + D_2\right)^2} \geq 2 \cdot f_{sw} \tag{2.33}$$

$$\omega_o = \frac{1}{\sqrt{C_{tot} \cdot L_{tot}}}, \; C_{tot} = \frac{C_1 \cdot C_o}{C_1 + C_o}, \; L_{tot} = \frac{L_1 \cdot L_2}{L_1 + L_2} \tag{2.34}$$

2.4 Applying Averaged Model for PFC Operation

2.4.1 Steady State Analysis for PFC Operation

The SEPIC PFC circuit diagram is shown in Figure 2.10. With the diode bridge rectifier, the grid AC voltage is converted to DC voltage.
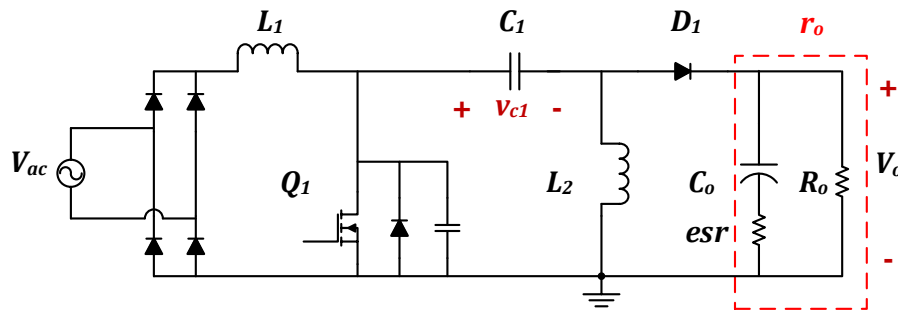
Figure 2.10 SEPIC PFC diagram
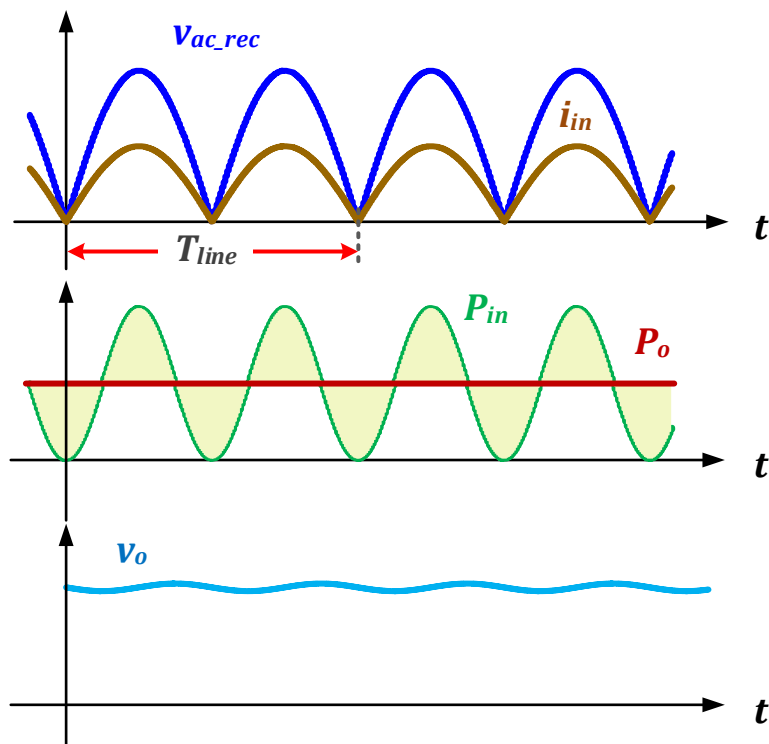
Figure 2.11 Fluctuating input power of PFC

As illustrated in Figure 2.11, for PFC operation, since the input AC power is fluctuating in double line frequency while the output power is constant, the unbalanced power is stored in output capacitors. Since the output voltage is constant, assuming an equivalent time variant load $r_o(t)$ can absorb all the fluctuating input power when the circuit operates at unity power factor, then the input and output power can be balanced for any time instant. With the equivalent time variant load $r_o(t)$, the PFC circuit can be modeled as DC-DC circuit in any time instant [20] [21] [31].

Assuming the AC line voltage and input current can be expressed as (2.35) and (2.36), then the input AC power and the equivalent load can be derived as (2.37) and (2.38).

$$v_{ac}(t) = \sqrt{2} \cdot V_{ac\_rms} \cdot \sin(\omega_{line} \cdot t) \tag{2.35}$$

$$I_{ac}(t) = \sqrt{2} \cdot I_{ac\_rms} \cdot \sin(\omega_{line} \cdot t) \tag{2.36}$$

$$P_{ac}(t) = V_{ac\_rms} \cdot I_{ac\_rms} \cdot \left[1 - \cos(2 \cdot \omega_{line} \cdot t)\right] = P_o - P_o \cdot \cos(2 \cdot \omega_{line} \cdot t) \tag{2.37}$$

$$r_o(t) = \frac{R_o}{2 \cdot \sin^2(\omega_{line} \cdot t)} \tag{2.38}$$

For any time instant $t = t_x$, by replacing R_o with $r_o(t)$ in (2.18) (2.11) and (2.15), the duty cycle can be derived as (2.39).

$$D_1(t) = \frac{V_o}{|v_{ac}(t)|} \cdot \sqrt{\frac{2 \cdot L_1 \cdot L_2}{r_o \cdot (L_1 + L_2) \cdot T_s}} = \frac{V_o}{V_{ac\_rms}} \cdot \sqrt{\frac{2 \cdot L_1 \cdot L_2}{R_o \cdot (L_1 + L_2) \cdot T_s}},$$

$$D_2(t) = \sqrt{\frac{2 \cdot L_1 \cdot L_2}{r_o \cdot (L_1 + L_2) \cdot T_s}} = 2 \cdot \sqrt{\frac{L_1 \cdot L_2}{R_o \cdot (L_1 + L_2) \cdot T_s}} \cdot |\sin(\omega_{line} \cdot t)| \tag{2.39}$$

The averaged input current within one switching cycle and current ripple can be derived as (2.40) and (2.41).

$$\overline{I}_{ac}(t) = D_1(t) \cdot \left[\Delta i_{L1}(t) + \Delta i_{L2}(t)\right] = \frac{D_1^2(t)}{2 \cdot L_1 \| L_2 \cdot f_s} \cdot v_{ac}(t) \qquad \textbf{(2.40)}$$

$$\Delta i_{L1} = \frac{D_1 T_s}{2} \cdot \frac{v_{ac}(t)}{L_1}, \ \ \Delta i_{L2} = \frac{D_1 T_s}{2} \cdot \frac{v_{ac}(t)}{L_2} \qquad \textbf{(2.41)}$$

Based on DC-DC DCM boundary condition (2.19), DCM boundary condition for PFC can be derived by replacing V_g and R_o with $v_{ac}(t)$ and $r_o(t)$, which is shown in (2.42).

$$DCM\ \ D_1(t) + D_2(t) \leq 1 \Rightarrow \frac{L_1 \cdot L_2}{L_1 + L_2} \cdot f_{sw} \leq \frac{R_o}{4} \cdot \frac{\left(\sqrt{2} \cdot V_{ac\_rms}\right)^2}{\left(V_o + \sqrt{2} \cdot V_{ac\_rms}\right)^2} \qquad \textbf{(2.42)}$$

From the expression of duty cycle and averaged current, if the operating frequency f_{sw} is constant, constant output voltage can be achieved with constant duty cycle D_1; meanwhile, with constant duty cycle and constant switching frequency, the averaged input current in each switching cycle would be proportional to input AC line voltage. Thus when SEPIC converter is operated in DCM, with constant switching frequency and constant duty cycle, the PFC function can be achieved in voltage follower mode [21].
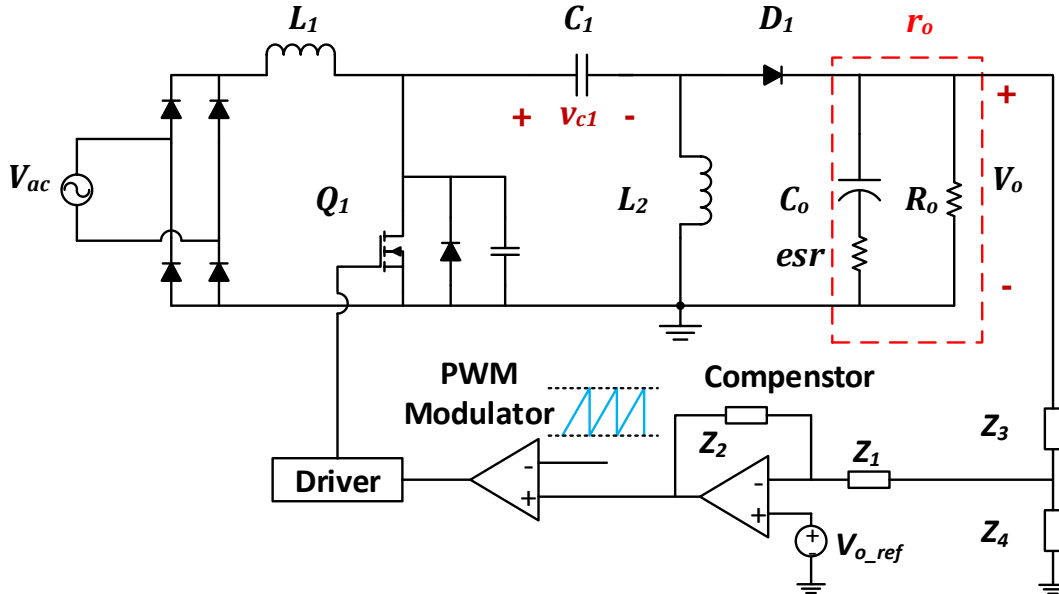
Figure 2.12 Control diagram for DCM SEPIC PFC in voltage follower mode

In voltage follower mode, the duty cycle no longer need to track the phase information of ac line voltage, instead, the duty cycle is constant when output voltage and load are constant. Thus the control loop can be implemented in a simple single voltage loop structure, which is shown in Figure 2.12.

2.4.2 Bode Plots of Control to Output Voltage for PFC Operation

According to the control to output small signal model derived in (2.28), with the equivalent load r_o, transfer function of control to output at any time instant can be derived for PFC circuit. For three cases $\omega_{line} \cdot t = 10°, 45°, 90°$, the corresponding bode plots of control to output voltage are illustrated in Figure 2.13 and Figure 2.14.
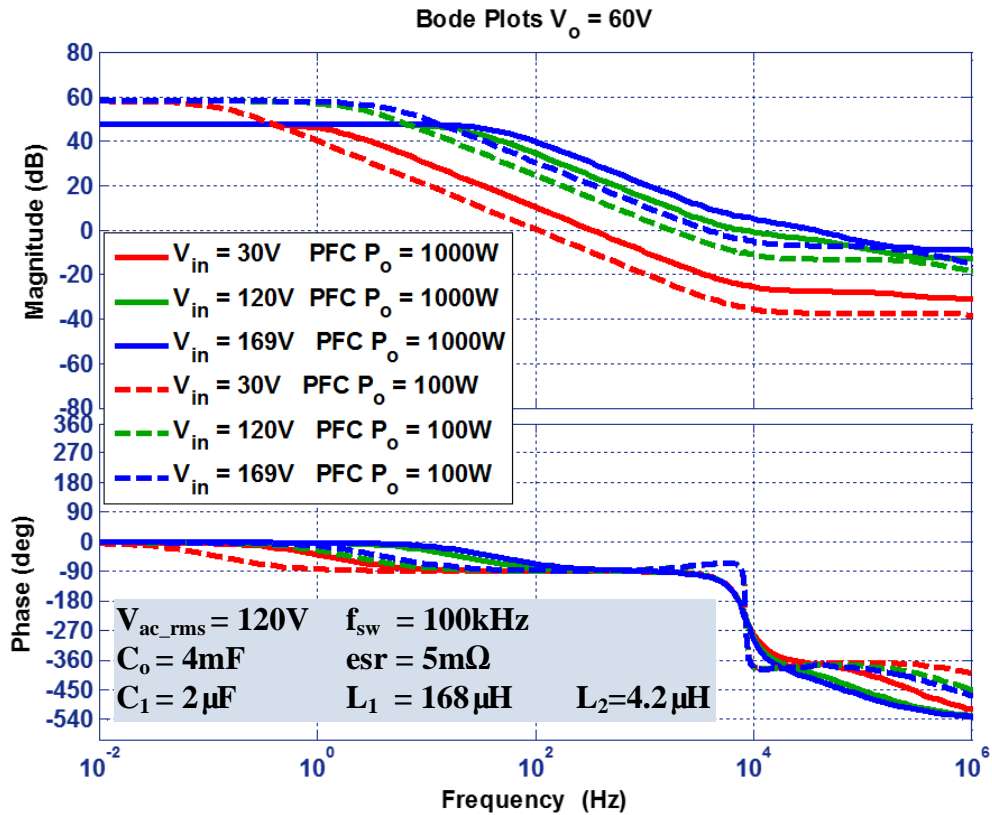
Figure 2.13 PFC control to output bode plots with 60V output
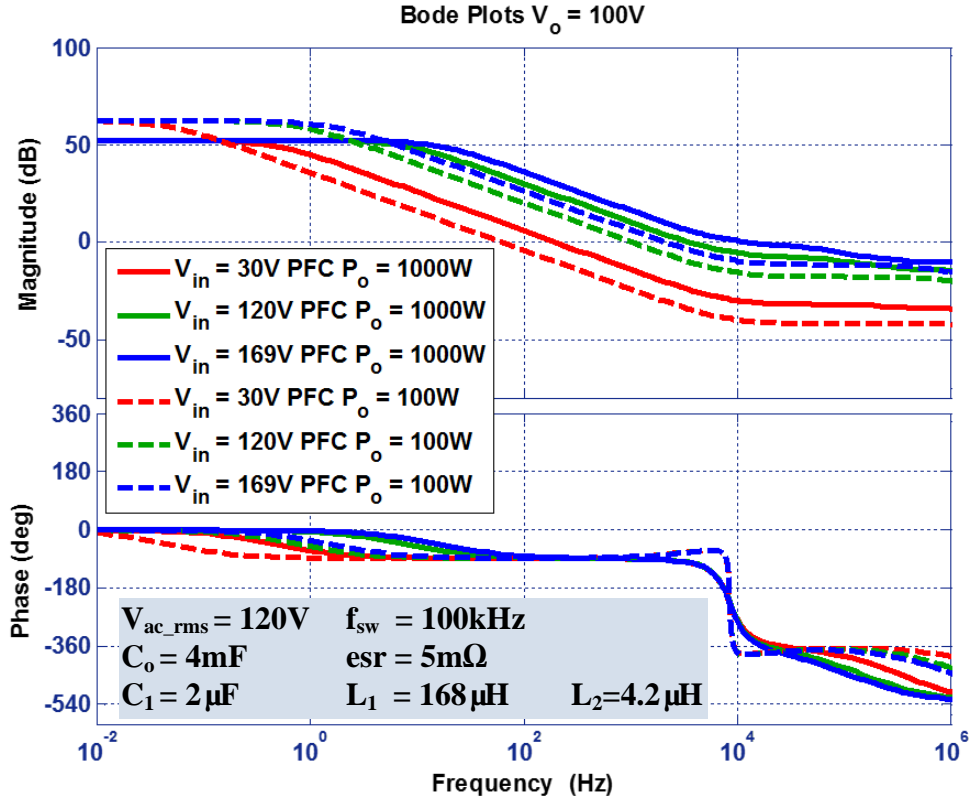
Figure 2.14 PFC control to output bode plots with 100V output

From Figure 2.14, for fixed output power, the DC gain for PFC is constant; lower output power results higher DC gain. Meanwhile, according to (2.30), within half line cycle, the low frequency pole is moving with the instant power. When the instant input power increases, the low frequency pole is moving towards higher frequency region. For the PFC operating in voltage follower mode, the bandwidth of voltage loop gain is required less than one tenth of double line frequency, which is much lower than the frequency of the LHP double pole and RHP double zero. Thus for PFC voltage loop compensator design, the control to output transfer function can be approximated with (2.43).

$$\frac{\hat{v}_o(s)}{\hat{d}(s)} = V_{ac\_rms} \cdot \sqrt{\frac{R_o}{2 \cdot L_1 \| L_2 \cdot f_{sw}}} \cdot \frac{1}{s \cdot \dfrac{R_o \cdot C_o \cdot V_{ac\_rms}^2}{2 \cdot v_{ac}^2(t)} + 1} \tag{2.43}$$

Chapter 3:
Coupled Inductors in DCM SEPIC PFC

In this chapter, based on the ripple steering concept, coupled inductors adopted in DCM SEPIC converter is analyzed. Based on the unique feature in SEPIC convert the two inductors share same voltage-seconds in each switching interval, the equivalent inductance model is derived. Simulation comparisons between circuits with equivalent inductances and de-coupled T model demonstrates the equivalent inductances model is valid in predicting both steady state and dynamic response of the DCM SEPIC converter with coupled inductors. From the equivalent inductance model, with well-designed coupling coefficient, the equivalent inductance can be amplified to couple times to self-inductance, thus same input current ripple can be achieved by a much smaller input inductor. Accordingly, a winding scheme in E-core for coupled inductors is analyzed and tested.

3.1 Coupled Inductors and Ripple Steering

The coupled inductors technique is widely used in power electronics circuits. In different circuits, adoption of coupled inductors may help in size and cost reduction, ripple reduction, stress reduction, and sometime help to achieve soft switching [28].

To analyze circuits include coupled inductors, coupled inductors need to be first modeled. For different circuits, mutual inductance model, decoupled T model or transformer with leakage model, as shown in Figure 3.1, can be used. All of these model maintains same relationship between the voltage and current of this two ports system where the two coupled inductors are connected to. In Figure 3.1, L_1, L_2 and M denote self-inductance and mutual inductance; n denotes winding turns ratio, equals to turns of No.1 inductor over the turns of No. 2 inductor, L_{1_lk} and L_{2_lk} denote physical leakage inductance formed by flux which is not coupled to the other inductor; when the coupled inductors are modeled as conventional transformer with equivalent lumped leakage inductance, the N_{x1}

denotes the equivalent voltage ratio, L_{Lk1} denotes the equivalent lumped leakage inductance in No.1 inductor side, and L_{m1} denotes the equivalent magnetizing inductance also in No. inductor side. The relationships between these quantities are shown in equations (3.1) ~ (3.3), in which k_c denotes the coupling coefficient of the two coupled inductors.

(a) Mutual Inductance Model

(b) Decoupled Model

(c) Transformer Model #1

(d) Transformer Model #2
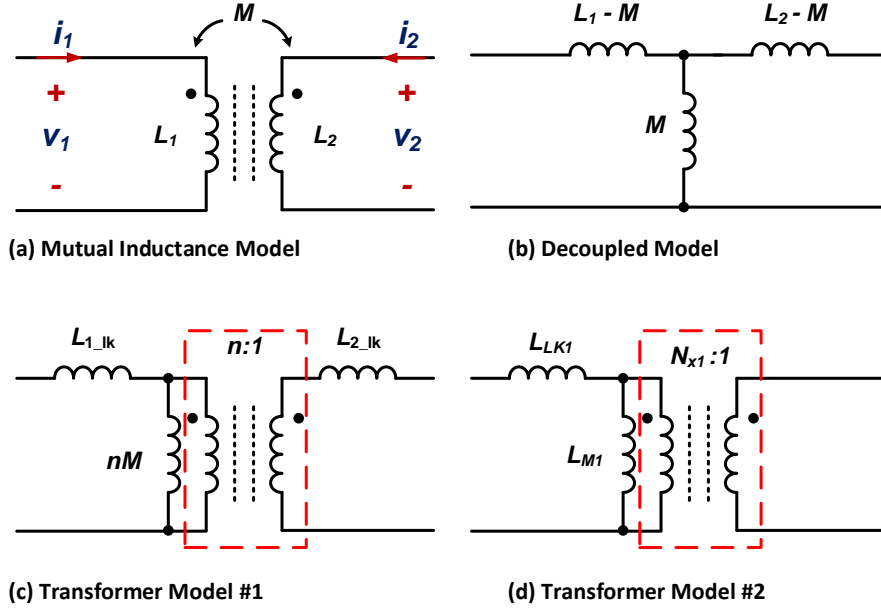
Figure 3.1 Different models of two coupled inductors

$$k_c = \frac{M}{\sqrt{L_1 \cdot L_2}} \tag{3.1}$$

$$n = \frac{N_1}{N_2}, \ L_{1\_lk} = L_1 - n \cdot M, \ L_{2\_lk} = L_2 - \frac{M}{n} \tag{3.2}$$

$$N_{x1} = k_c \cdot \sqrt{\frac{L_1}{L_2}}, \ L_{M1} = L_1 \cdot k_c^2, \ L_{LK1} = L_1 \cdot \left(1 - k_c^2\right) \tag{3.3}$$

$$\begin{cases} v_1(t) = L_1 \dfrac{di_1(t)}{dt} + M \dfrac{di_2(t)}{dt} \\ v_2(t) = L_2 \dfrac{di_2(t)}{dt} + M \dfrac{di_1(t)}{dt} \end{cases} \tag{3.4}$$

With the model (a), (b) and (c), the relationship between the voltage and current in this two port system can be expressed as (3.4), (3.5) and (3.6).

$$\begin{cases} v_1 = (L_1 - M) \cdot \dfrac{di_1}{dt} + M \dfrac{d(i_1 + i_2)}{dt} \\[4mm] v_2 = (L_2 - M) \cdot \dfrac{di_2}{dt} + M \dfrac{d(i_1 + i_2)}{dt} \end{cases} \tag{3.5}$$

$$\begin{cases} v_1 = L_{1\_lk} \cdot \dfrac{di_1}{dt} + n \cdot M \cdot \dfrac{d\left(i_1 + \dfrac{i_2}{n}\right)}{dt} \\[6mm] v_2 = L_{2\_lk} \cdot \dfrac{di_2}{dt} + M \cdot \dfrac{d\left(i_1 + \dfrac{i_2}{n}\right)}{dt} \end{cases} \tag{3.6}$$

When coupled inductors technique is adopted to achieve current ripple steering in No.1 inductor, which means $\lim\limits_{\Delta t \to 0} \int_t^{t+\Delta t} \dfrac{di_1(t)}{dt} dt = \lim\limits_{\Delta t \to 0} \Delta i_1 \big|_t^{t+\Delta t} = \dfrac{di_1(t)}{dt} = 0$, combined with (3.4), the ripple steering criterion can be derived as (3.7). Thus if the self-inductances and coupling coefficient meet this criterion, the current ripple in No.1 inductor can be eliminated.

$$\lim_{\Delta t \to 0} \Delta i_1 \bigg|_t^{t+\Delta t} = 0 \Rightarrow \lim_{\Delta t \to 0} \frac{\int_t^{t+\Delta t} v_1(t)dt}{\int_t^{t+\Delta t} v_2(t)dt} = \frac{v_1(t)}{v_2(t)} = \frac{M}{L_2} = k_c \cdot \sqrt{\frac{L_1}{L_2}} \tag{3.7}$$

A more general coupled inductors filter building block can be adopted in all ripple steering circuits [26] [27], as shown in Figure 3.2. The filter include two coupled inductors and one filtering capacitor. The equivalent circuit with decoupled T model is also presented.
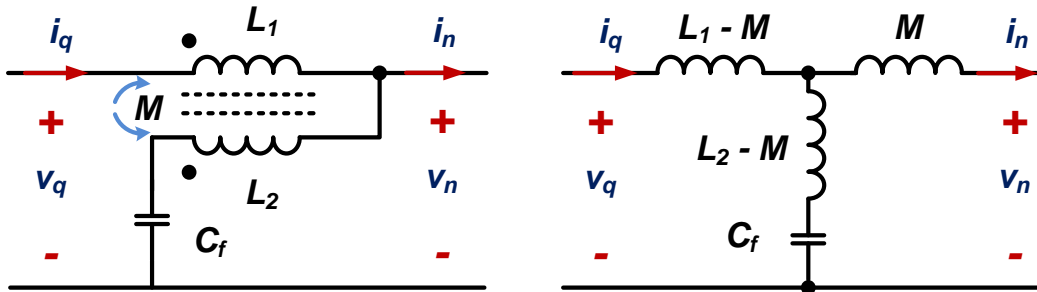
Figure 3.2 Coupled inductors filter building block

In this general coupled inductors filter block, the two port can be denoted as quiet port and noisy port [27]. Assuming the voltage at the noisy port consists of a DC component V_{n_DC} and a superimposed AC ripple v_{n_ac}. Because the averaged voltage across inductors must be zero, the averaged DC component V_{q_DC}, V_{n_DC} and V_{cf_DC} would equal to each other. Assuming C_f is large enough, which means the AC voltage ripple is small enough, then most of the AC voltage component v_{n_AC} existing in the noise port would drop on the coupled inductor L_2. If the parameters of the coupled inductors meet the criteria shown in (3.7), ideally, zero current ripple can be achieved at the quiet port.

3.2 Ripple Steering in SEPIC Converter

The ripples steering phenomenon was originally investigated in Cuk Converters, but the same technique can be effectively applied to all converter topologies in which two or more inductors are fed by same or scaled voltage waveforms [29]. In SEPIC converter, which is shown in Figure 3.3, to study ripple steering, the voltage feeding into the two coupled inductors need to be studied first, which is listed in (3.8) ~ (3.10).
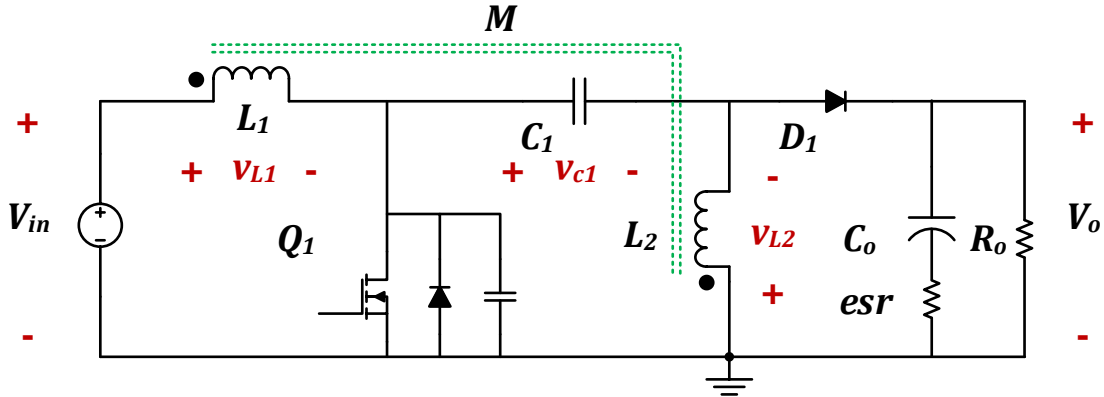
Figure 3.3 SEPIC converter with coupled inductors

1st Interval:
$$v_{L1}(t) = V_g, \; v_{L2}(t) = v_{c1}(t) \tag{3.8}$$

2nd Interval:
$$v_{L1}(t) = V_g - v_o(t) - v_{c1}(t), \; v_{L2}(t) = -v_o(t) \tag{3.9}$$

3rd Interval:
$$v_{L1}(t) - v_{L2}(t) = V_g - v_{c1}(t) \tag{3.10}$$

When intermediate capacitor is infinite, which results zero voltage ripple, thus the voltage across the intermediate capacitor is exactly same as the input voltage. In this case, because voltage across the two coupled inductors are same in every interval, zero ripple can be achieved if parameters of coupled inductors meet the equation (3.11). In practical, with finite intermediate capacitor, although the averaged intermediate capacitor voltage is the same as the input voltage, due to the voltage ripple on intermediate capacitor, the voltage ratio between the two inductors is not constant, zero current ripple is impossible. From this point, larger intermediate capacitor would result smaller voltage ripple, which would make the practical circuit more close to the ideal ripple steering condition.

$$\frac{v_{L1}(t)}{v_{L2}(t)} = 1 = \frac{M}{L_2} = k_c \cdot \sqrt{\frac{L_1}{L_2}} \tag{3.11}$$

3.3 Equivalent Non-Coupled Inductance Model

When the intermediate capacitor is large enough, the voltage ripple can be neglected, thus the voltage across the two coupled inductors equals to each other in three switching intervals. Inserting (3.12) into the mutual inductance model (3.4) results (3.13), by comparing with non-coupled case, the equivalent inductance model (3.14) can be derived.

$$v_{L1}(t) = v_{L2}(t) \tag{3.12}$$

$$\begin{cases} \dfrac{di_{L1}}{dt} = v_{L1}(t) \cdot \dfrac{L_2 - M}{L_1 \cdot L_2 - M^2} = v_{L1}(t) \Big/ \left(L_1 \cdot \dfrac{1 - k_c^2}{1 - M/L_2} \right) \\[4mm] \dfrac{di_{L2}}{dt} = v_{L2}(t) \cdot \dfrac{L_1 - M}{L_1 \cdot L_2 - M^2} = v_{L2}(t) \Big/ \left(L_2 \cdot \dfrac{1 - k_c^2}{1 - M/L_1} \right) \end{cases} \tag{3.13}$$

$$\begin{cases} L_{1\_equ} = L_1 \cdot \dfrac{1 - k_c^2}{1 - M/L_2} = L_1 \cdot \dfrac{1 - k_c^2}{1 - k_c \cdot \sqrt{L_1/L_2}} \\[4mm] L_{2\_equ} = L_2 \cdot \dfrac{1 - k_c^2}{1 - M/L_1} = L_2 \cdot \dfrac{1 - k_c^2}{1 - k_c/\sqrt{L_1/L_2}} \end{cases} \tag{3.14}$$

From this equivalent inductance model, it is clear when the mutual inductance M is close to self-inductance L_2, the equivalent inductance L_{1_eq} can be amplified couple times to self-inductance L_1. The amplification ratio is determined by coupling coefficient and mutual inductance. From this point, the ripple steering is achieved through amplified equivalent inductor. With carefully designed coupling coefficient, self-inductance of input inductor is no longer need be large enough to limit the input current ripple, instead, the equivalent input inductor is supposed to be.
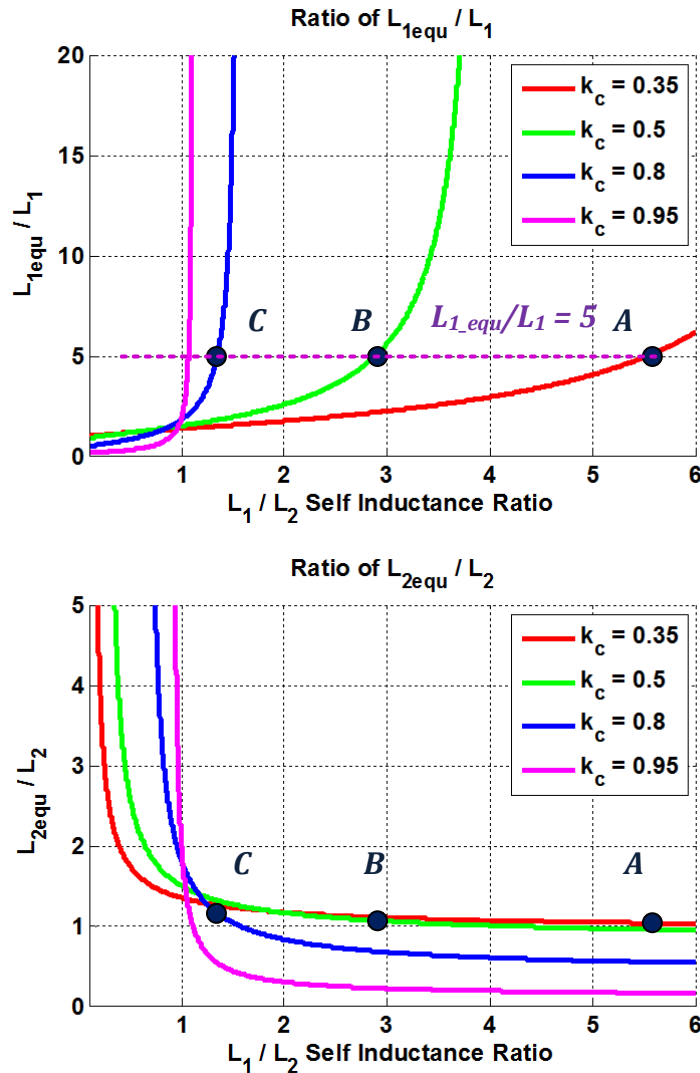
Figure 3.4 Ratio of equivalent inductance over self-inductance

Based on this model, the amplifying ratio of equivalent inductor over self-inductor curves under different coupling conditions are illustrated in Figure 3.4. Since with higher

amplifying ratio, better input current ripple reduction can be achieved. The ripple steering effect could be quantified with this amplifying ratio L_{1_equ}/L_1. From the curves in Figure 3.4, to achieve same amplifying ratio, with larger coupling coefficient, the ratio between self-inductances L_1/L_2 should be smaller.
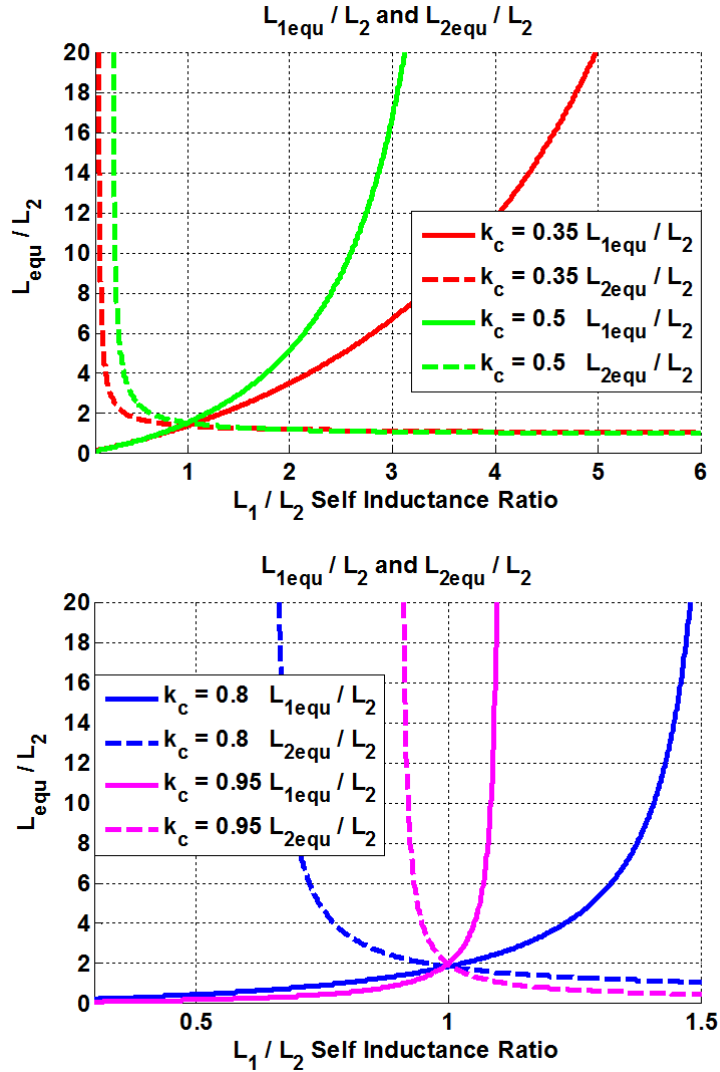
Figure 3.5 Normalized equivalent inductances based on L₂

Considering the upper limit for the parallel equivalent inductances $L_{1\_equ}//L_{2\_equ}$ is set by DCM boundary condition (2.19(2.19) and large L_{1_equ} is preferred for low input current ripple, thus L_{1_equ}/L_{2_equ} must be larger than one. From Figure 3.5, only when the self-inductance ratio L_1/L_2 is larger than one, the equivalent inductance ratio L_{1_equ}/L_{2_equ} is larger than one. In the region where L_1/L_2 is larger than unity, as L_1/L_2 increases, L_{1_equ}/L_2

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increases, L_{2_equ}/L_2 is approaching unity. Thus with fixed self-inductance L_2, increasing self-inductance L_1 would result larger amplify ratio L_{1_equ}/L_1.

To design the coupled inductors for SEPIC converter, the equivalent inductance L_{1_equ} and L_{2_equ} could be first designed based on corresponding specification. According to (3.15), self-inductance L_1 and L_2 can be solved with certain coupling coefficient k_c and the designed equivalent inductance L_{1_equ} and L_{2_equ}.

From Figure 3.6, to achieve same equivalent inductance L_{1_equ} and L_{2_equ}, the coupled inductors can be implemented with either high coupling coefficient or low coupling coefficient. With higher coupling coefficient, the required self-inductance L_1 is lower.

$$\lambda = \frac{L_{1\_equ}}{L_{2\_equ}} - 1 \Rightarrow \begin{cases} L_1 = \dfrac{L_{1\_equ}}{1-k_c^2} \cdot \left[1 - k_c \cdot \dfrac{\sqrt{k_c^2 \cdot \lambda^2 + 4 \cdot (\lambda+1)} - k_c \cdot \lambda}{2} \right] \\[4mm] L_2 = \dfrac{L_{2\_equ}}{1-k_c^2} \cdot \left[1 - \dfrac{2 \cdot k_c}{\sqrt{k_c^2 \cdot \lambda^2 + 4 \cdot (\lambda+1)} - k_c \cdot \lambda} \right] \end{cases} \qquad \textbf{(3.15)}$$

Compared with loosely coupled case, tightly coupled implementation requires accurate control on L_1/L_2. Tiny variation of L_1/L_2 may result large variation on L_{1_equ}/L_{2_equ}. Because the ratio of output inductor current ripple magnitude to input inductor current ripple magnitude equals to L_{1_equ}/L_{2_equ}, thus tiny variation of L_1/L_2 would result noticeable different current ripple. For L_{1_equ}/L_{2_equ} in the range from 10 to 160, the required L_1/L_2 ratio is around 1.1. Considering the two windings are implemented with toroid shape core or wound around same pillar of E shape core, because L_1/L_2 is proportional to N_1^2/N_2^2, to achieve 1.1 inductance ratio, turns number of both windings should be at least larger than 20. Due to turns numbers are integral, higher accuracy on L_1/L_2 require even larger number of turns. From this point view, implementation with relatively low coupling coefficient would be better choice.
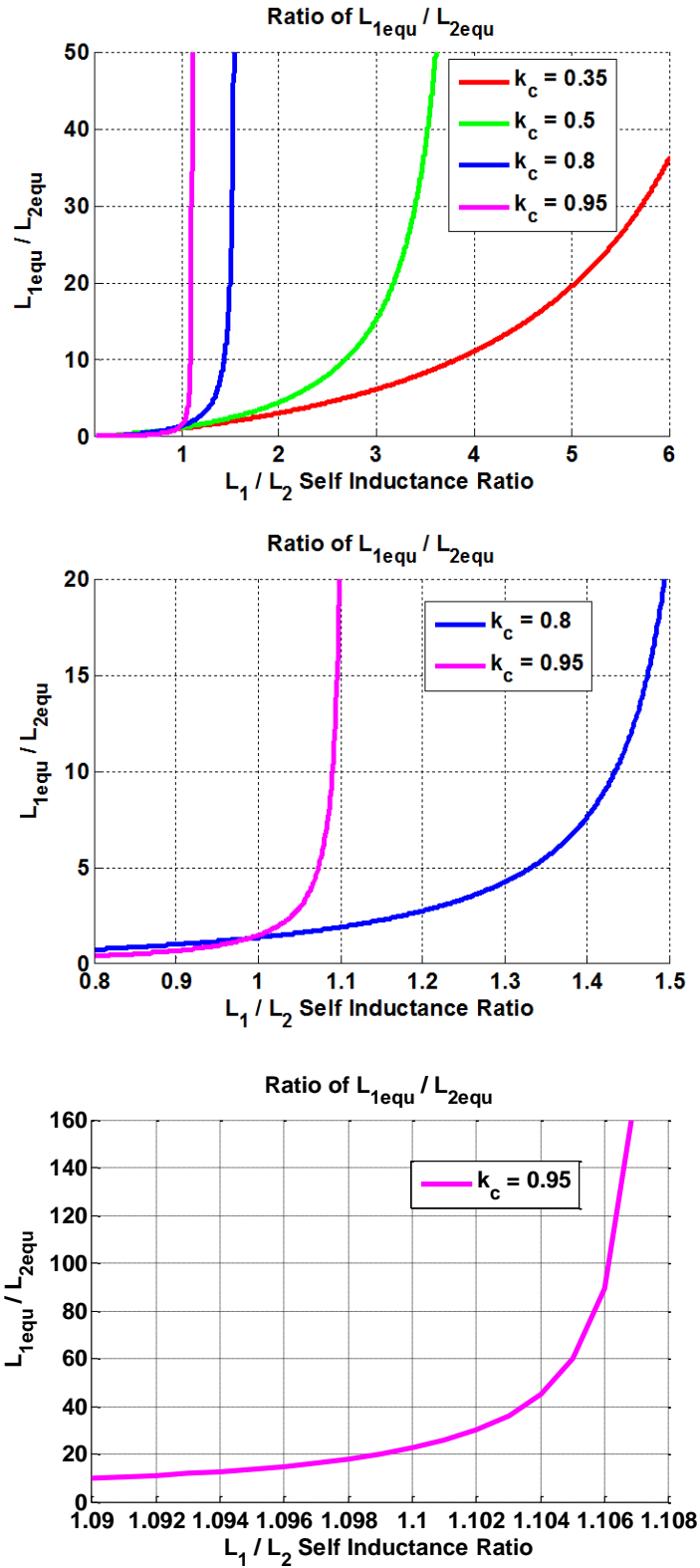
Figure 3.6 Coupling coefficient impact on equivalent inductance ratio
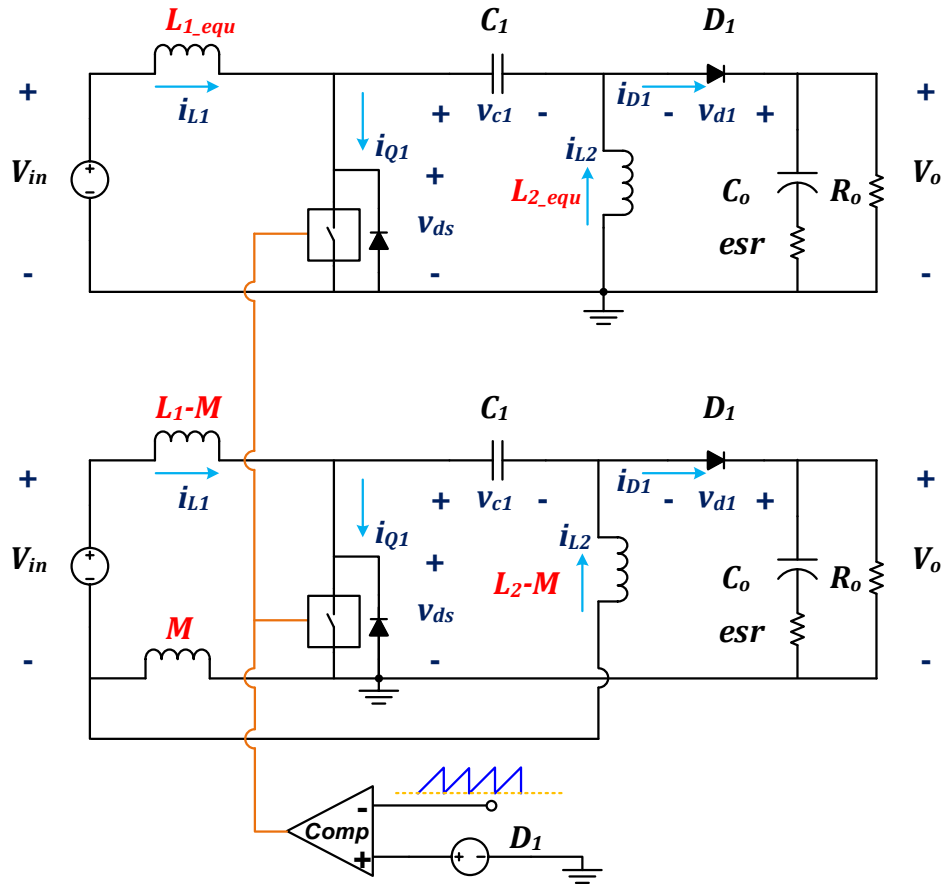
Figure 3.7 Simulation diagram for equivalent inductors in SEPIC

To investigate the circuit behavior difference of DCM SEPIC converter between coupled inductors case and non-coupled inductors with equivalent inductances case, simulation circuits shown in Figure 3.7 are built to compare both steady-state and small-signal characteristics. The two SEPIC converters are driven by same PWM signal. Decoupled T model is inserted into the SEPIC converter with coupled inductors, while equivalent non-coupled inductors are inserted into the other SEPIC converter. The corresponding parameters are listed in TABLE. 3.1.

TABLE. 3.1 Simulation parameters for equivalent inductor model

	#1	#2	#3	#4
Input Voltage V_{in} (V)	100			
Output Voltage V_o (V)	100			
Power P_o (W)	1000			
Switching Frequency (kHz)	100			
Equivalent Inductor L_{1_equ} (μH)	133			
Equivalent Inductor L_{2_equ} (μH)	5.2			
Coupled Inductor L_1 (μH)	27.3		5.46	
Coupled Inductor L_2 (μH)	5.0		4.97	
Mutual Inductance M (μH)	4.1		4.95	
Equivalent Inductor L_r (μH)	29.2		0.51	
Coupling Coefficient k_c	0.35		0.95	
Capacitor C_1 (μF)	1	10	10	100
Capacitor C_o (mF)	4			
Equivalent Series Resistance ESR (mΩ)	15			
Duty D_1 in Simulation	0.3187			

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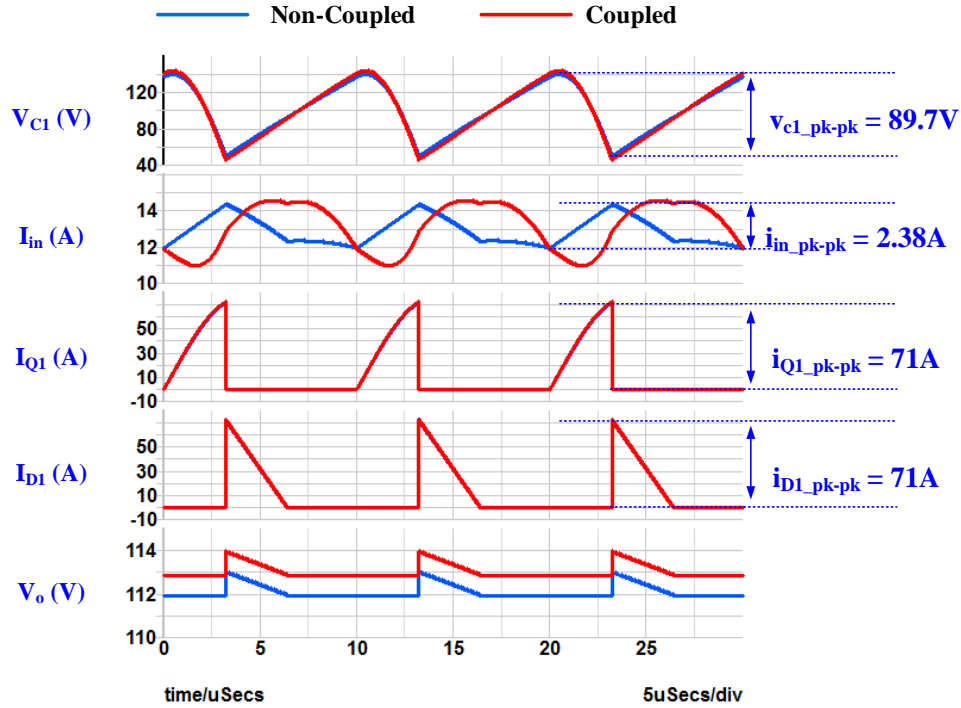
(a) Case #1 Low Coupling kc = 0.35, Intermediate Capacitor C1 = 1μF
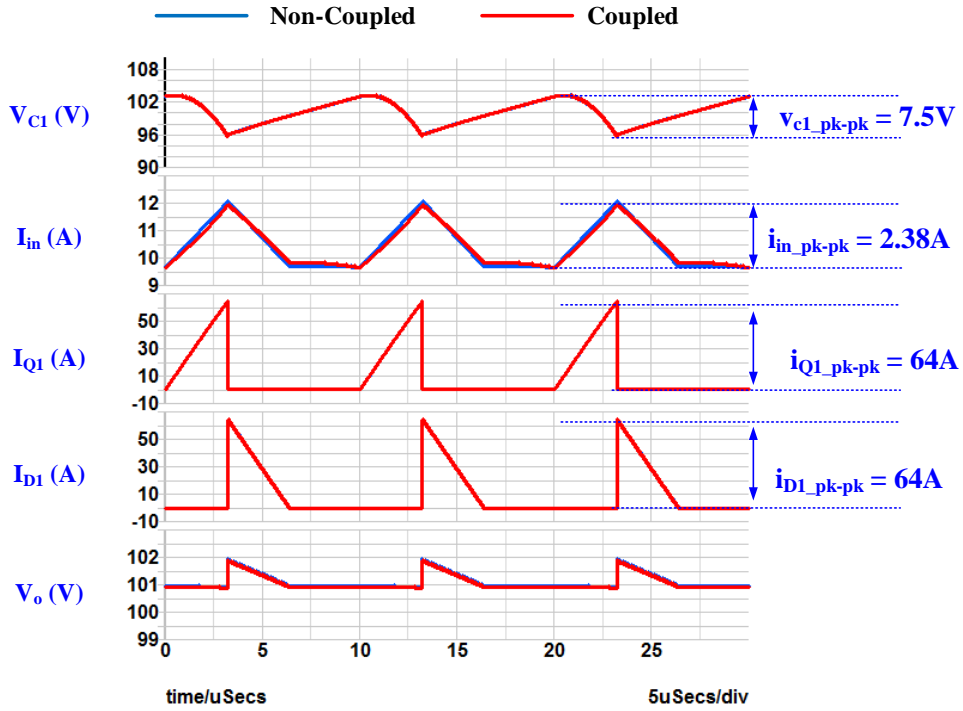
(b) Case #2 Low Coupling kc = 0.35, Intermediate Capacitor C1 = 10μF
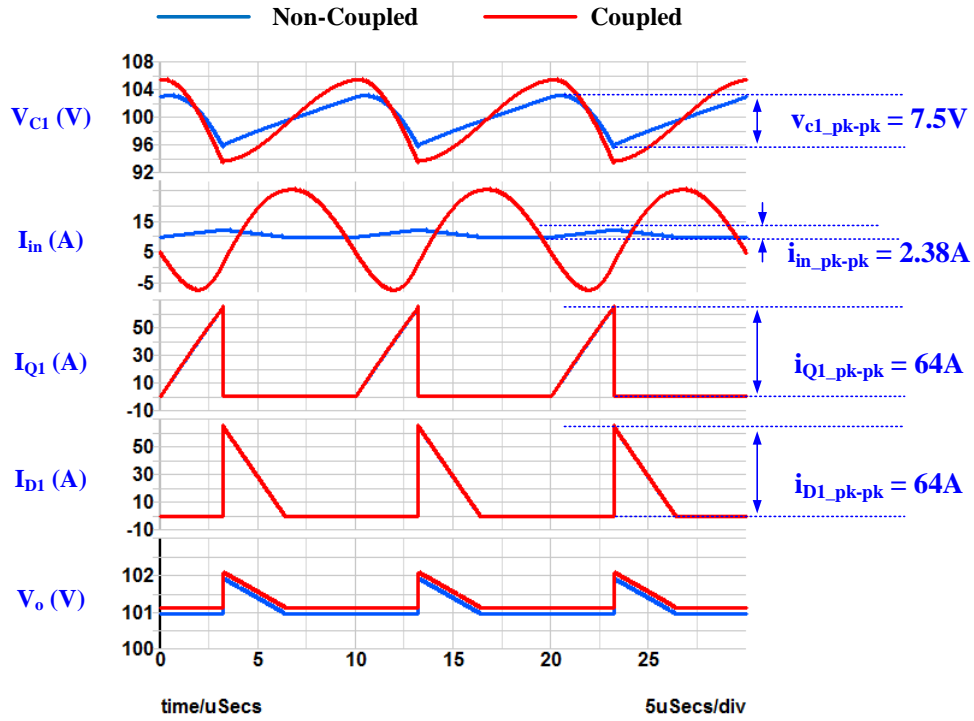
(c) Case #3 High Coupling kc = 0.95, Intermediate Capacitor C1 = 10μF
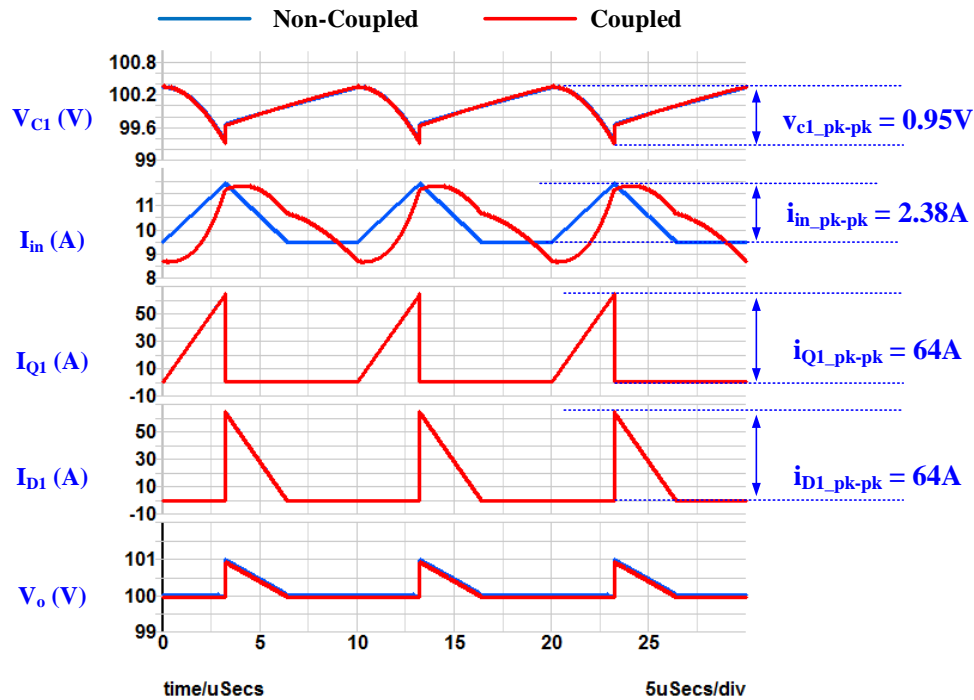
(d) Case #4 High Coupling kc = 0.95, Intermediate Capacitor C1 = 100μF

Figure 3.8 Steady state comparison for different coupling k_c and capacitor C_1

From Figure 3.8, for all the four cases, the non-coupled equivalent inductance model accurately predicts the current stress in the main switch and output diode.

From Figure 3.8 (a) and (b), under low coupling condition, coupling coefficient k_c is **0.35**, when intermediate capacitance is large enough (case #2), the steady state waveforms of coupled inductors case are almost same as non-coupled inductors case. Thus the equivalent inductances model is accurate to predict steady state characteristics for SPEIC converter with coupled inductors. When intermediate capacitance is small (case #1), the ripple steering effect would be deteriorated. Comparing the voltage ripple on intermediate capacitor and input current ripple in (a) and (b), while one tenth smaller capacitance results more than ten times larger voltage ripple on intermediate capacitor, the input current ripple increases from 2.38A to 3.38A. Although the input current ripples do not show dramatic increase, smaller intermediate capacitance results in inaccuracy of the equivalent inductances model.

For Figure 3.8 (c) and (d), under high coupling condition, coupling coefficient k_c is **0.95**, same phenomenon can be observed. Meanwhile, considering the voltage ripple on intermediate capacitor and input current ripple in (b), (c) and (d), although in case #4 the voltage ripple on intermediate capacitor is less than 1V, compared to non-coupled case, the input current ripple of coupled inductors case is 3.88A, which is higher than 2.38A. Thus to achieve same input current ripple with same equivalent inductances, coupled inductors with high coupling coefficient requires much higher intermediate capacitance compared to low coupling case.

The impact from intermediate capacitor can be explained with the equivalent circuit shown in Figure 3.9. Equivalent circuit (b) is derived by inserting decoupled T model into circuit (a). With Y-Δ transformation, circuit (c) is derived. Compare (c) to SEPIC converter with non-coupled inductors diagram, the only difference is the inductor L_r (3.16), which is connected across input source and intermediate capacitor. Since the voltage across L_r is the voltage ripple of intermediate capacitor, the resonant current flowing through L_r would change the input current shape, which results increased input current ripple. With higher coupling coefficient k_c, the inductance of L_r is lower, thus larger intermediate capacitance

is required to limit the current flowing through this inductor. From this point, the intermediate capacitance can be designed based on limitation on current flowing through this equivalent inductor. Corresponding criterion is derived in (3.17), (3.18) and (3.19).

$$L_r = \frac{L_1 \cdot L_2 - M^2}{M} \qquad (3.16)$$
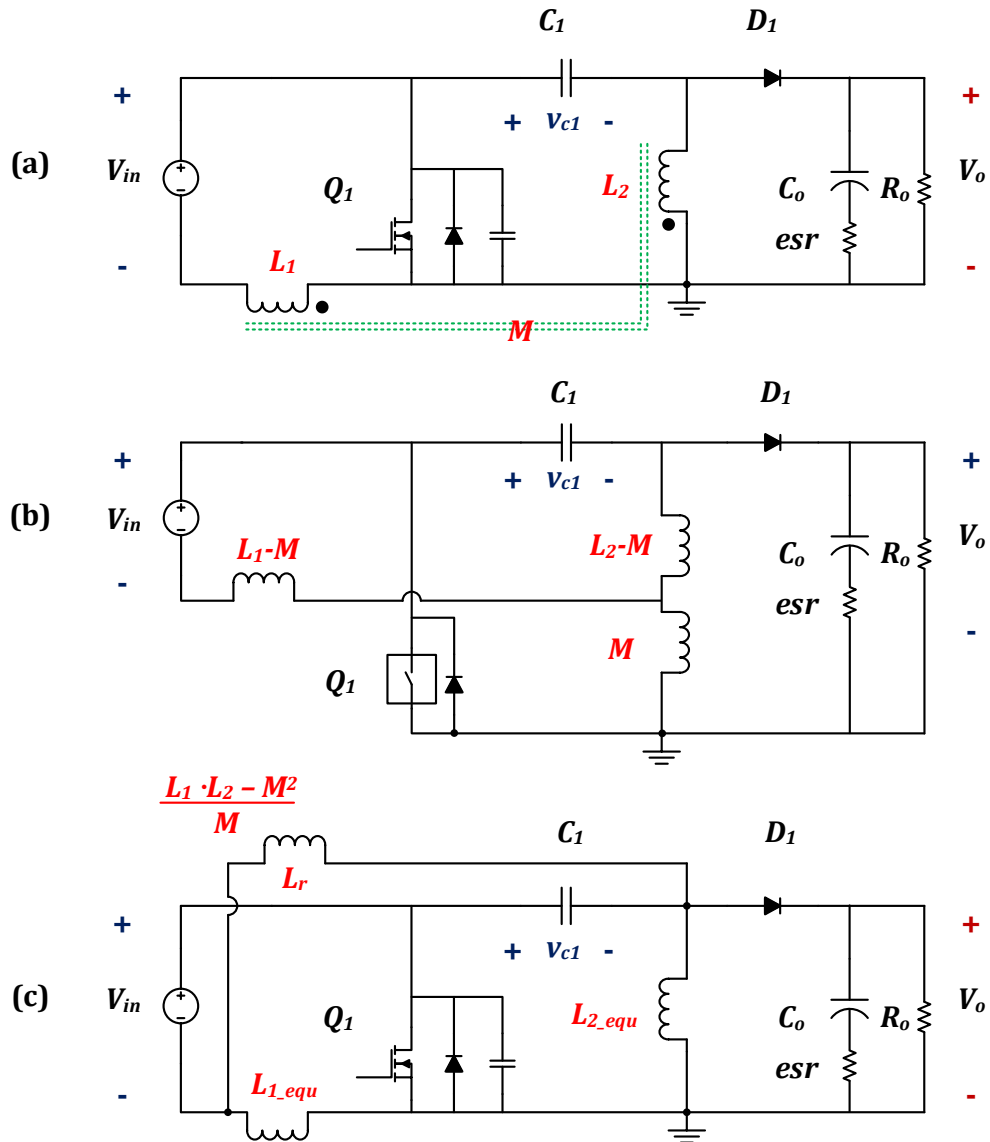
Figure 3.9 Equivalent circuit of SEPIC converter with coupled inductors

$$\Delta v_{c1} \approx \frac{1}{C_1} \cdot \frac{1}{2} \cdot \frac{V_{in}}{L_{2\_equ}} \cdot \left(D_1 \cdot T_s \right)^2 \qquad (3.17)$$

$$\Delta i_{Lr} \simeq \frac{\Delta v_{c1}}{2\pi f_{sw} \cdot L_r} \leq k_{rr} \cdot \Delta i_{L1\_equ} = k_{rr} \cdot \frac{V_{in}}{L_{1\_equ}} \cdot D_1 \cdot T_s, \; 0 < k_{rr} \leq 1 \qquad (3.18)$$

$$C_1 \geq \frac{L_{1\_equ}}{L_{2\_equ}} \cdot \frac{1}{L_r \cdot k_{rr}} \cdot \frac{D_1}{4\pi \cdot f_{sw}^2} \qquad (3.19)$$

In (3.17), the peak to peak voltage ripple of intermediate capacitor is estimated based on current waveform shown in Figure 2.4. By introducing a ratio k_{rr} between current ripple of inductors L_r and L_{1_equ} in (3.18), the capacitance design criterion can be derived as (3.19). Since input current is the sum of current flowing through the two inductors, small k_{rr} means the current flowing through inductor L_r is negligible compared to the ripple current of inductor L_{1_equ}, the steady state characteristics of coupled inductors can be predicted by the equivalent inductance model.

With (3.19) and the given parameters in TABLE. 3.1, if k_{rr} is selected as 1, the intermediate capacitance should be larger than 2.2 µF when coupling coefficient is 0.35; and the intermediate capacitance should be larger than 122 µF when coupling coefficient is 0.95.

With the given parameters listed in TABLE. 3.1, for case #2 and case #4, simulation circuits shown in Figure 3.10 are built to investigate the difference of control to output small signal transfer function $\dfrac{v_o(\mathrm{s})}{d_1(\mathrm{s})}$ between coupled inductors case and non-coupled inductors case. The equivalent inductances of the coupled inductors are used in non-coupled circuit. The corresponding bode plots from the simulation are shown in Figure 3.11.

For low coupling case, as shown in Figure 3.11 (a), adoption of the coupled inductors doesn't change the gain curve, only changes the phase curve. The LHP complex poles and RHP complex zeros are moved towards higher frequency region.
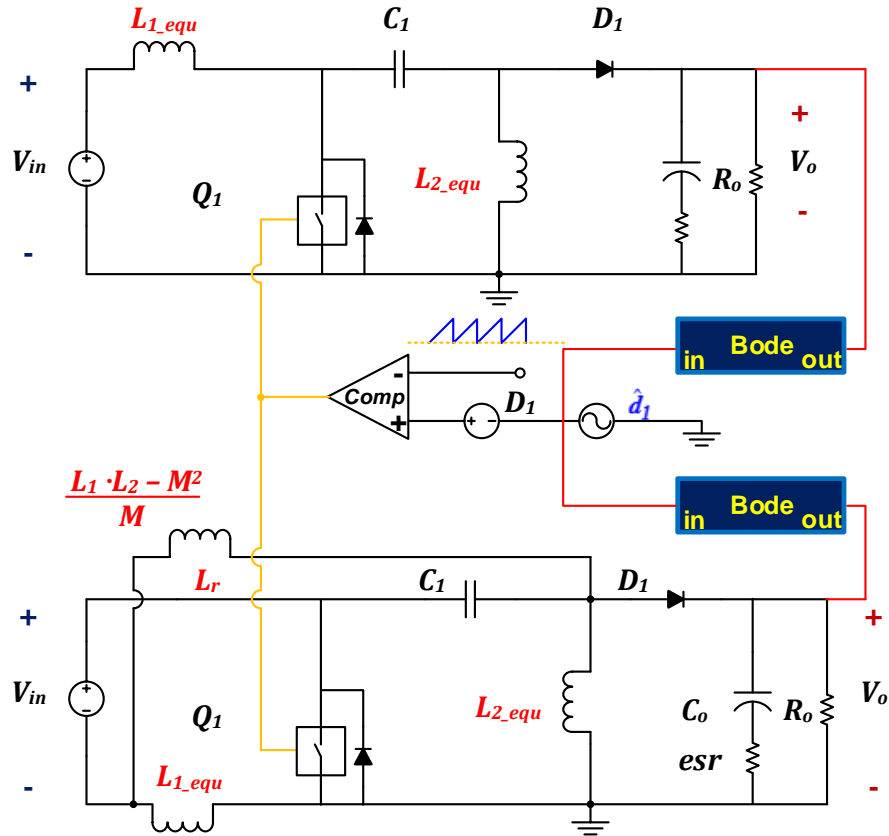
Figure 3.10 Simulation circuit for comparison of control to output bode plots
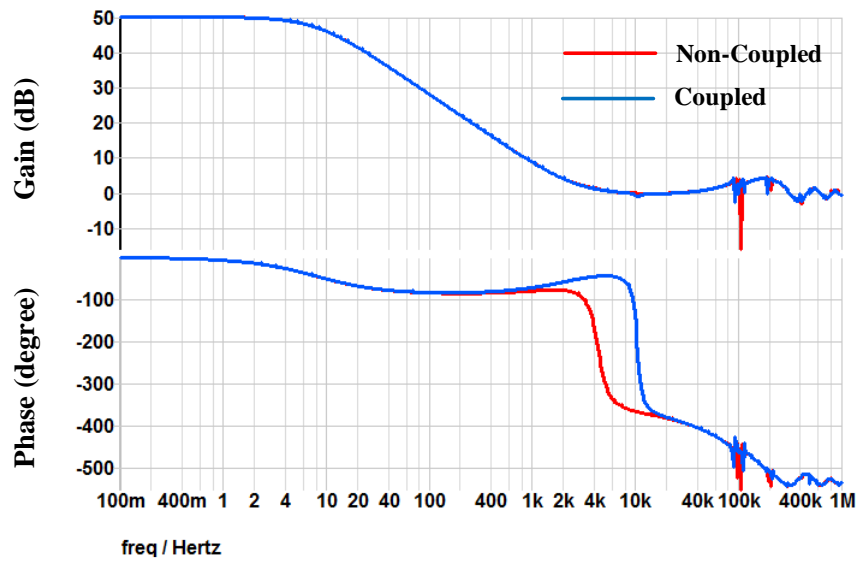
(a) Case #2 Low Coupling kc = 0.35, Intermediate Capacitor C1 = 10μF
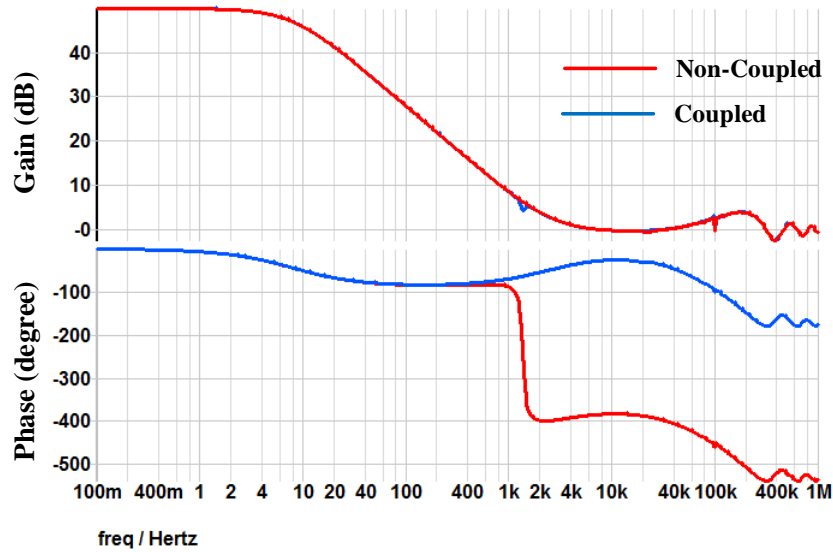
(b) Case #4 High Coupling kc = 0.95, Intermediate Capacitor C1 = 100µF

Figure 3.11 Bode plots comparison for case #2 and case #4

For high coupling case, as shown in Figure 3.11 (b), again, adoption of the coupled inductors doesn't change the gain curve, only changes the phase curve. An interesting phenomenon is the LHP complex poles and RHP complex zeros are eliminated compared with non-coupled case. In low frequency region, the system behaves like a simple first order system with one low frequency pole, the ESR zero and the RHP zero together make the phase stays above -90 degree, and the final high frequency LHP pole drops the phase to -180 degree. The system order is reduced from four to two.

To summarize, the major benefit of coupling the two inductor in a DCM SEPIC converter is the larger equivalent input inductances can be achieved with relatively smaller self-inductances, which is usually referenced as ripple steering effects. With coupled inductors, the required intermediate capacitance increases with the coupling coefficient. In frequency domain, for the control to output small signal transfer function, the coupled inductors would not change gain curves of the system. In low frequency region, system response stays same since the low frequency single pole is irrelevant with either the inductors or the intermediate capacitor. For higher frequency region, the coupled inductors increases the corner frequency of the LHP complex poles and RHP complex zeros.

Meanwhile, highly coupled inductors can almost eliminate the LHP complex double pole and the RHP complex double zeros, thus reduce the system order from four to two.

3.4 Winding Scheme for Coupled Inductors

From above analysis, the ripple steering can be achieved with coupled inductors under either high coupling condition or low coupling condition. Consider implementing the two coupled inductors in an E shape ferrite core, the general winding scheme for both high coupling and low coupling is illustrated in Figure 3.12.
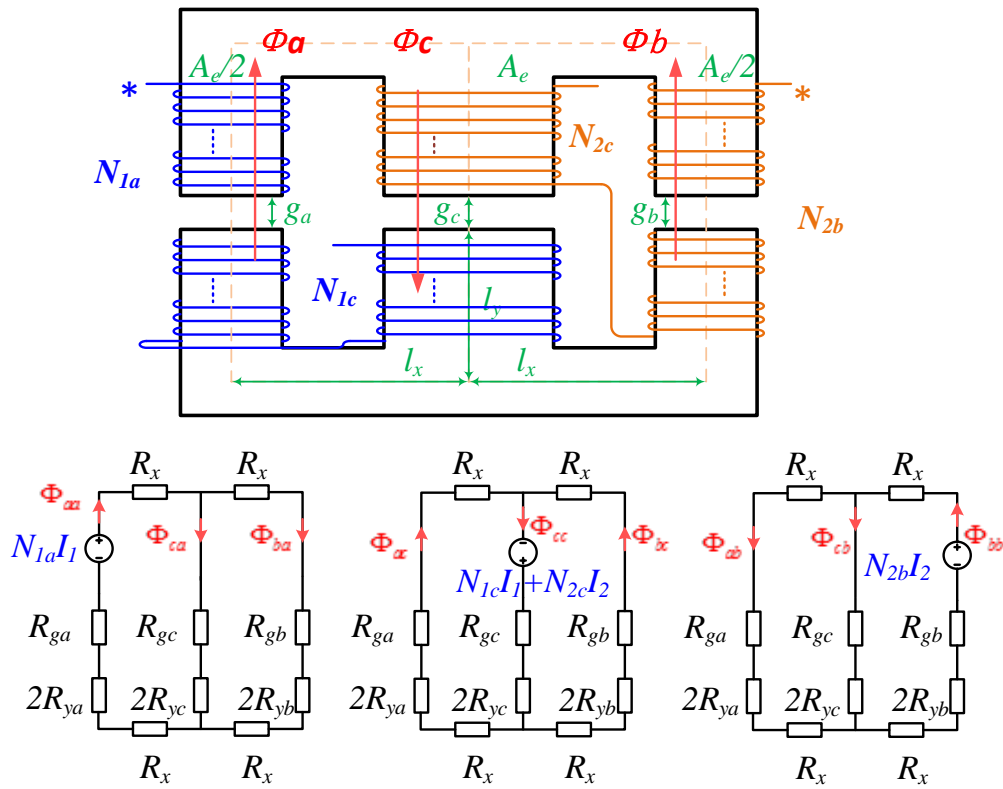
Figure 3.12 Coupled inductors winding scheme for low coupling coefficient

For the E shape core, winding can be placed around the center pillar or side pillar. For the two inductors, when only center pillar is used, the coupling coefficient could be high; while only side pillars are used, the coupling coefficient can be relatively low. As shown in Figure 3.12, assume the two inductors' winding are wound on both center pillar and side pillar, then four different windings with turns number N_{1a}, N_{1c}, N_{2b} and N_{2c} can

be found in this configuration. Each inductor are composed by one winding on center pillar and another winding on side pillar. When N_{1c} and N_{2c} are zero, only side pillars are utilized, which results the low coupling configuration. On the contrary, zero N_{1a} and N_{2b} would result high coupling configuration. With corresponding reluctances model and superposition principle, the self-inductances and mutual inductance of these four windings can be estimated. Based on the connection of these four windings, the self-inductances and mutual inductance of the two inductor can be extracted.

As shown in Figure 3.12, the cross section area of center pillar and side pillar are denoted as A_e and $A_e/2$; the length of the vertical and horizontal segments are denoted as l_x and l_y; and the relative permeability of the ferrite core is denoted as μ; and the three gap distance are denoted as g_a, g_b and g_c, assume all of them equal to g_p. With all these parameters and neglecting both the leakage flux and the fringing effect, the reluctance R_x, R_{ya}, R_{yb}, R_{yc} and R_g can be calculated by (3.20) and (3.21).

$$R_x = \frac{2 \cdot l_x}{\mu_0 \cdot \mu \cdot A_e}, \quad R_{yc} = \frac{l_y}{\mu_0 \cdot \mu \cdot A_e} = R_y, \quad R_{ya} = R_{yb} = \frac{2 \cdot l_y}{\mu_0 \cdot \mu \cdot A_e} = 2 \cdot R_y, \tag{3.20}$$

$$R_{gc} = \frac{g_p}{\mu_0 \cdot A_e} = R_g, \quad R_{ga} = R_{gb} = \frac{2 \cdot g_p}{\mu_0 \cdot A_e} = 2 \cdot R_g \tag{3.21}$$

$$\Phi_{a\_1a} = \frac{\left(3 \cdot R_g + 6 \cdot R_y + 2 \cdot R_x\right)}{\left(2 \cdot R_g + 4 \cdot R_y + 2 \cdot R_x\right) \cdot \left(4 \cdot R_g + 8 \cdot R_y + 2 \cdot R_x\right)} \cdot N_{1a} \cdot I_1 \tag{3.22}$$

$$\Phi_{c\_1a} = \frac{1}{\left(4 \cdot R_g + 8 \cdot R_y + 2 \cdot R_x\right)} \cdot N_{1a} \cdot I_1 \tag{3.23}$$

$$\Phi_{b\_1a} = -\frac{R_g + 2 \cdot R_y}{\left(2 \cdot R_g + 4 \cdot R_y + 2 \cdot R_x\right) \cdot \left(4 \cdot R_g + 8 \cdot R_y + 2 \cdot R_x\right)} \cdot N_{1a} \cdot I_1 \tag{3.24}$$

From equivalent reluctance circuit model and superposition principle, the flux generated by any one of the four windings in each branches can be calculated. Taking winding **1a** as an example, the flux generated by winding **1a** in three branches can be calculated as (3.22), (3.23) and (3.24).

Then the self-inductances and mutual inductances of the four windings can be calculated as (3.25) ~ (3.31).

$$L_{1a} = N_{1a} \cdot \frac{\Phi_{a\_1a}}{I_1}, L_{1c} = N_{1c} \cdot \frac{\Phi_{c\_1c}}{I_1}, L_{2b} = N_{2b} \cdot \frac{\Phi_{b\_2b}}{I_2}, L_{2c} = N_{2c} \cdot \frac{\Phi_{c\_2c}}{I_2} \qquad (3.25)$$

$$M_{1a\_1c} = N_{1a} \cdot \frac{\Phi_{a\_1c}}{I_1} = M_{1c\_1a} = N_{1c} \cdot \frac{\Phi_{c\_1a}}{I_1} \qquad (3.26)$$

$$M_{1a\_2c} = N_{1a} \cdot \frac{\Phi_{a\_2c}}{I_2} = M_{2c\_1a} = N_{2c} \cdot \frac{\Phi_{c\_1a}}{I_1} \qquad (3.27)$$

$$M_{1a\_2b} = N_{1a} \cdot \frac{\Phi_{a\_2b}}{I_2} = M_{2b\_1a} = N_{2b} \cdot \frac{\Phi_{b\_1a}}{I_1} \qquad (3.28)$$

$$M_{1c\_2c} = N_{1c} \cdot \frac{\Phi_{c\_2c}}{I_2} = M_{2c\_1c} = N_{2c} \cdot \frac{\Phi_{c\_1c}}{I_1} \qquad (3.29)$$

$$M_{1c\_2b} = N_{1c} \cdot \frac{\Phi_{c\_2b}}{I_2} = M_{2b\_1c} = N_{2b} \cdot \frac{\Phi_{b\_1c}}{I_1} \qquad (3.30)$$

$$M_{2c\_2b} = N_{2c} \cdot \frac{\Phi_{c\_2b}}{I_2} = M_{2b\_2c} = N_{2b} \cdot \frac{\Phi_{b\_2c}}{I_2} \qquad (3.31)$$

With voltage and current relationship between two coupled inductors, the final self-inductance and mutual inductance for inductor #1 and inductor #2 can be calculated according to (3.32), (3.33) and (3.34).

$$L_1 = L_{1a} + L_{1c} + 2 \cdot M_{1a\_1c} \qquad (3.32)$$

$$L_2 = L_{2b} + L_{2c} + 2 \cdot M_{2b\_2c} \qquad (3.33)$$

$$M_{12} = M_{1a\_2b} + M_{1a\_2c} + M_{1c\_2c} + M_{1c\_2b} \qquad (3.34)$$

The total flux and flux density in each branch of the core could be calculated based on (3.35), (3.36) and (3.37).

$$\Phi_a = \Phi_{a\_1a} + \Phi_{a\_1c} + \Phi_{a\_2c} + \Phi_{a\_2b}, \ B_a = \frac{2 \cdot \Phi_a}{A_e} \tag{3.35}$$

$$\Phi_{1c} = \Phi_{2c} = \Phi_{c\_1a} + \Phi_{c\_1c} + \Phi_{c\_2c} + \Phi_{c\_2b}, \ B_c = \frac{\Phi_c}{A_e} \tag{3.36}$$

$$\Phi_b = \Phi_{b\_1a} + \Phi_{b\_1c} + \Phi_{b\_2c} + \Phi_{b\_2b}, \ B_b = \frac{2 \cdot \Phi_b}{A_e} \tag{3.37}$$

Based on the reluctance model, four sets of calculation result are listed in TABLE. 3.2. The parameters are based on E65/32/27 ferrite core with material 3C95; 3 mm gap distance in all three pillars are assumed.

TABLE. 3.2 Calculated inductances for several winding configurations

	#1	#2	#3	#4**
L₁ Side Pillar Turn Number N_{1a}	0	7	9	19
L₁ Center Pillar Turn Number N_{1c}	10	7	4	0
L₂ Center Pillar Turn Number N_{2c}	0	3	4	0
L₁ Side Pillar Turn Number N_{2b}	7	5	3	7
Self-Inductance L₁ (μH)	11.1	14.9	12.5	29.9
Self-Inductance L₂ (μH)	4.1	4.7	3.8	4.1
Mutual Inductance M (μH)	3.9	4.5	3.7	3.6
Coupling Coefficient k_c	0.58	0.54	0.53	0.33
Equivalent Inductance L_{1_equ} (μH)	170.1	198.3	224.5	257.2
Equivalent Inductance L_{2_equ} (μH)	4.1	4.8	3.9	4.1
Equivalent Inductance L_r (μH)	7.7	11.3	9.3	29.7

**In case #4, the polarity should be reverse

Chapter 4:

System Design and Implementation

In this chapter, the power stage parameters design considerations for 1 kW SEPIC power factor correction circuit are presented. Based on DCM operation boundary, maximum input current ripple specification and selected switching frequency, design criteria on inductances of the two inductor and capacitance of the intermediate capacitor and output capacitor are discussed. With all the power stage parameters, the control to output small signal transfer function is derived based on discussion in Chapter 2; a simple PI compensator is designed accordingly. To attenuate the third harmonic components in input current, which is induced by double line ripple of output voltage, a notch filter is inserted in the control loop. The design consideration for the notch filter is also presented. At last, the design is verified by close-loop simulation.

4.1 Power Stage Parameters Design

The main specifications of the SEPIC PFC are listed in TABLE. 4.1.

TABLE. 4.1 PFC specification

Input Voltage V_{in} (V rms)	120
Output Voltage V_o (V)	60 ~ 100
Maximum Power P_o (W)	1000
Switching Frequency (kHz)	100
Output Voltage Ripple Peak (Full Load)	20%

4.1.1 Inductances Design

Based on the analysis in previous chapters, for non-coupled inductors, steady state duty cycle (2.39), switching averaged input current (2.40), input current ripple (2.41) and DCM boundary condition (2.42) are summarized together as (4.2) ~ (4.5).

$$v_{ac}(t) = \sqrt{2} \cdot V_{ac\_rms} \cdot \sin(\omega_{line} \cdot t) \tag{4.1}$$

$$D_1(t) = \frac{V_o}{V_{ac\_rms}} \cdot \sqrt{\frac{2 \cdot L_1 \cdot L_2}{R_o \cdot (L_1 + L_2) \cdot T_s}} \tag{4.2}$$

$$\bar{I}_{ac}(t) = \frac{D_1^2(t)}{2 \cdot L_1 \| L_2 \cdot f_{sw}} \cdot v_{ac}(t) \tag{4.3}$$

$$\Delta i_{in\_pk}(t) = \Delta i_{L1\_pk}(t) = D_1 T_s \cdot \frac{\sqrt{2} \cdot V_{ac\_rms} \cdot |\sin(\omega_{line} \cdot t)|}{L_1}$$

$$= \frac{2}{L_1} \cdot \sqrt{P_o \cdot \frac{L_1 \cdot L_2}{(L_1 + L_2) \cdot f_s}} \cdot |\sin(\omega_{line} \cdot t)| \tag{4.4}$$

$$DCM \ D_1(t) + D_2(t) \le 1 \Rightarrow \frac{L_1 \cdot L_2}{L_1 + L_2} \cdot f_{sw} \le \frac{R_o}{4} \cdot \frac{\left(\sqrt{2} \cdot V_{ac\_rms}\right)^2}{\left(V_o + \sqrt{2} \cdot V_{ac\_rms}\right)^2} \tag{4.5}$$

From (4.4), the input current ripple is proportional to square root of output power; the maximum appears when input voltage reaches the peak value. The ratio between input current ripple (**pk-pk**) and switching averaged input current is derived as (4.6). By defining the upper limit of this ratio under full load condition as **K_r**, criterion (4.7) can be derived.

$$\frac{\Delta i_{in\_pk}(t)}{|\bar{I}_{ac}(t)|} = \frac{1}{L_1} \cdot \sqrt{\frac{1}{P_o} \cdot \frac{L_1 \cdot L_2}{(L_1 + L_2) \cdot f_s}} \cdot \sqrt{2} \cdot V_{ac\_rms} \le K_r \tag{4.6}$$

$$\sqrt{\frac{L_1}{L_2} \cdot (L_1 + L_2) \cdot f_s} \ge \frac{\sqrt{2} \cdot V_{ac\_rms}}{K_r} \cdot \sqrt{\frac{1}{P_o}} \tag{4.7}$$
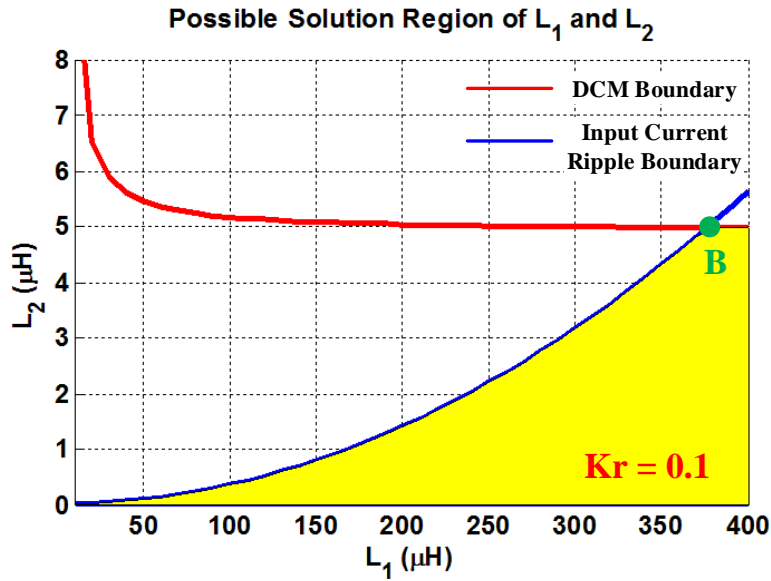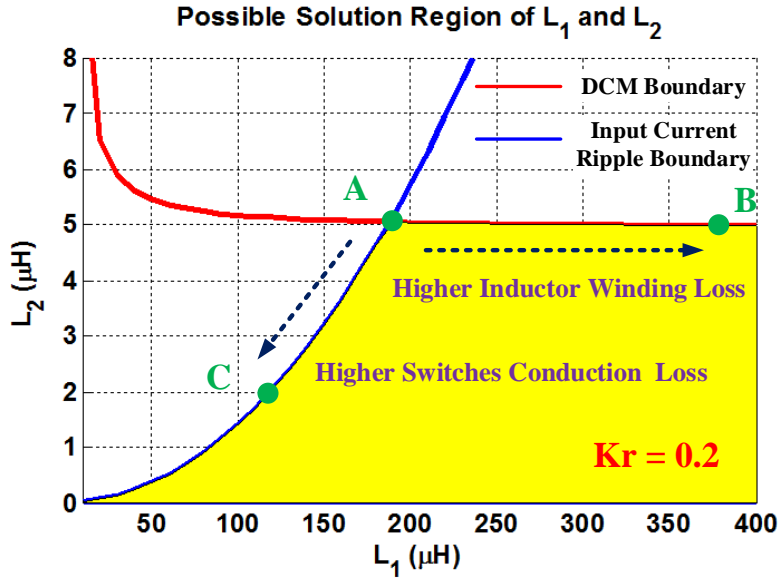
Figure 4.1 Possible inductances solution for DCM and given input current ripple

With the DCM and input current ripple ratio criteria, possible inductances combination is shown as the yellow region in Figure 4.1 for different K_r.

For proper inductances selection, two other factors should be considered. The first is the efficiency, second is the current ripple of the output inductor L_2 (4.9).

From efficiency point view, impact from inductances on the conduction loss of semiconductors and inductor windings should be considered. Because the current stress on

the main switch and output diode are determined by the paralleled inductance of L_1 and L_2, as shown in (4.8), larger paralleled inductance can reduce the conduction loss of switches. In Figure 4.1, although the input current ripple of combination A and C is same, the conduction loss in switches of combination A is less than combination C. For inductor copper loss, comparing the inductances combination A and B in Figure 4.1, because the output inductance L_2 and the paralleled inductance are almost same, the current ripple in switches and output inductance L_2 are almost same, the conduction loss on switches and copper loss of output inductance L_2 are almost same; for combination B, if the increased input inductances is achieved by increased numbers of winding turns, the conduction loss in L_1 would increases.

$$\Delta i_{Q1\_pk}(t) = \Delta i_{D1\_pk}(t) = \frac{2 \cdot V_o}{\sqrt{R_o \cdot f_s \cdot L_1 \| L_2}} \cdot \left|\sin(\omega_{line} \cdot t)\right| \tag{4.8}$$

$$\Delta i_{L2\_pk}(t) = \frac{2}{L_2} \cdot \sqrt{P_o \cdot \frac{L_1 \cdot L_2}{(L_1 + L_2) \cdot f_s}} \cdot \left|\sin(\omega_{line} \cdot t)\right| \tag{4.9}$$

From the efficiency point of view, the intersection of the two boundary would be the optimal design point. The two inductances are selected as (4.10), which is close to combination A. The corresponding K_r is around 21% ~25%.

$$L_1 = 130\mu H \sim 170\mu H , \ L_2 = 4.2\mu H \sim 5.1\mu H \tag{4.10}$$

4.1.2 Inductors Implementation

For PFC operation, the average current flowing through the input inductors equals to input current, the average current flowing through output inductor equals to load current. When input voltage reaches the peak value, the average input current and current ripple in two inductors reach maximum; meanwhile, the instant power delivered to the output is two times to the average output power. To estimate current peak of the two inductor, conditions shown in (4.11) based on equivalent DC-DC converter are used. The calculated results are listed in TABLE. 4.2. The RMS value of the current can be extracted from simulation.

$$V_{in} = \sqrt{2} \cdot V_{ac\_rms}, \quad P_o = 2000W \qquad\qquad (4.11)$$

TABLE. 4.2 Estimated maximum current of two inductors for 1kW PFC

Output Voltage (V)	60	100
Duty Cycle D_1	0.249	
Duty Cycle D_2	0.705	0.423
Inductance L_1 (μH)	170	
Inductance L_2 (μH)	4.6	
Average Current I_{L1} (A)	11.785	
Peak to Peak Current Ripple Δi_{L1_pk} (A)	2.49	
Peak Current I_{L1_peak} (A)	**11.09**	**13.44**
Average Current I_{L2} (A)	33.33	20
Peak to Peak Current Ripple Δi_{L2_pk} (A)	92.01	
Peak Current I_{L2_peak} (A)	**81.41**	**81.06**
Remaining Current I_r (A)	10.6	10.95
Line Cycle RMS Current I_{L1_rms} (A)	8.85	
Line Cycle RMS Current I_{L2_rms} (A)	28.8	24.9

Based on the line cycle RMS value of inductor current, winding wires are selected. For inductor L_1, relatively conservative 650 circular mil per ampere rule is used, which results AWG#12. For inductor L_2, 450 circular mil per ampere rule is used, thus AWG#10 is selected.

Based on the peak current value, inductances and the selected wire gauge, with given maximum flux density B_{max}, the minimum product of the cross section area and the window area can be estimated with (4.12). In which, W_A presents the window area of the

core, A_e presents the cross section area, A_w is the copper area of a single winding wire, K_u is the window utilization ratio.

$$W_A \cdot A_e \geq \frac{A_w \cdot L \cdot I_{max}}{K_u \cdot B_{max}} \tag{4.12}$$

$$K_u = 0.4, \ B_{max} = 0.16\text{T}$$

$$W_{A\_L1} \cdot A_{e\_L1} \geq 1.27 \times 10^{-7} m^4, \ W_{A\_L2} \cdot A_{e\_L2} \geq 0.33 \times 10^{-7} m^4 \tag{4.13}$$

The minimum core area product (AP) for the two inductors is calculated under both 60 V output and 100 V output condition. The maximum results are shown in (4.13). With the dimension data from **Ferroxcube**, for non-coupled inductors implementation, the designed parameters for L_1 and L_2 are listed in TABLE. 4.3. The number of turns and gap distance are calculated based on (4.14) and (4.15).

$$n \approx \frac{L \cdot I_{max}}{A_e \cdot B_{max}} \tag{4.14}$$

$$l_g \approx \frac{\mu_0 \cdot L \cdot I_{max}^2}{B_{max}^2 \cdot A_e} \tag{4.15}$$

TABLE. 4.3 Designed parameters of non-coupled inductors #1

	L₁	L₂
Designed Ferrite Core	ETD54/28/19	ETD44/22/15
Area Product A$_e$·W$_A$ (m⁴)	1.26×10^{-7}	0.48×10^{-7}
Wire Gauge (AWG)	12	10
Number of Turns	**54**	**14**
Estimated DC ESR (mΩ)	28.1	3.7
Estimated Total Gap distance (mm)	**6.1**	**9.4**
Material	3C94	

Flux Density Swing ΔB$_{pk\_pk}$ (T)	0.028	0.175
Maximum Flux Density B$_{max}$ (T)	0.151	0.154

For the coupled inductors design, the flux flowing inside the core is generated by the two inductors together. Considering the worst case, with the unity coupling coefficient, all the flux generated by one inductor is coupled to the other inductor. In this SEPIC design, since inductor current reach maximum at same time, the maximum flux would be the sum of maximum flux of the two inductor. Under this worst case assumption, the AP method can be modified as (4.16). When the two winding are symmetrical, the turns-ratio can be estimated with (4.17).

$$W_A \cdot A_e \geq \left(\frac{N_1}{N_2} \cdot A_{w1} + A_{w2} \right) \cdot \frac{\left(L_{1\_self} \cdot I_{1\_max} + L_{2\_self} \cdot I_{2\_max} \right)}{K_u \cdot B_{max}} \cdot \left(\frac{N_2}{N_1} + 1 \right) \tag{4.16}$$

$$\frac{N_1}{N_2} = \sqrt{\frac{L_{1\_self}}{L_{2\_self}}} \tag{4.17}$$

According to Figure 3.6 and (3.15) in Chapter 3, (4.18) can be extracted. For the high coupling condition case, the minimum AP can be estimated with (4.19). Thus E65 is selected for coupled inductors implementation.

$$\frac{L_{1\_self}}{L_{2\_self}} = 1.1031, \quad \frac{L_{2\_self}}{L_2} \approx 1.316 \tag{4.18}$$

$$W_A \cdot A_e \geq 1.65 \times 10^{-7} m^4 \tag{4.19}$$

$$E65 \quad W_A \cdot A_e \approx 2.13 \times 10^{-7} m^4 \tag{4.20}$$
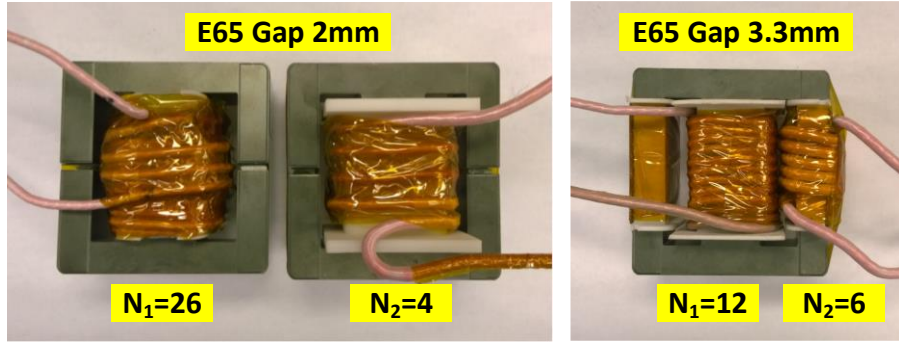
Figure 4.2 Inductors implementations

Based the design procedure, E65/32/27 ferrite core with material 3C95 is selected as the core for coupled inductors. For comparison, separate inductors are also implemented with this core, as shown in Figure 4.2. Parameters for this implementation are listed in TABLE. 4.4 and TABLE. 4.5.

TABLE. 4.4 Measured parameters of non-coupled inductors #2

	L_1	L_2
Total Gap distance (mm)	4	4
Number of Turns	**26**	**4**
Wire Gauge (AWG)	12	10
Inductance (μH)	**171.2**	**4.58**
DC ESR (mΩ)	20.3	3
Ferrite Core Size	E65/32/27	
Core Material	3C95	
Flux Density Swing ΔB_{pk_pk} (T)	**0.03**	**0.196**
Maximum Flux Density (T)	0.163	0.173

TABLE. 4.5 Measured parameters of coupled inductors

	L_1	L_2
Gap distance In Three Pillars (mm)	3.3	3.3
Number of Turns	**12**	**6**
Wire Gauge (AWG)	12	10
Self-Inductance (µH)	**27.54**	**5.02**
DC ESR (mΩ)	11.3	2.8
Mutual Inductance (µH)	**4.1**	
Coupling Coefficient	0.349	
Equivalent Inductor L_{1_equ} (µH)	**132**	
Equivalent Inductor L_{2_equ} (µH)	**5.18**	
Equivalent Inductor L_r (µH)	**29.6**	
Center Flux Density Swing ΔB_{pk_pk} (T)	0.14	
Center Maximum Flux Density (T)	0.11	
Side Pillar Flux Density Swing ΔB_{pk_pk} (T)	0.23	
Side Pillar Maximum Flux Density (T)	0.24	

4.1.3 Capacitance Design for Intermediate Capacitor

For implementation with separate inductors, according to analysis in Chapter 2, large voltage ripple on intermediate capacitor would not ruin the steady state characteristics of DC-DC SEPIC converter, but small capacitance of intermediate capacitor would result higher output voltage with the estimated duty cycle. From control to output small signal characteristics, selecting intermediate capacitor with smaller capacitance would push the LHP complex pole pair and RHP complex zero pair to higher frequency region, which

would facilitate compensator design when high bandwidth loop gain is preferred. Although PFC operating in voltage follower mode does not require high bandwidth, selecting intermediate capacitor with smaller capacitance is still preferred when size and cost are considered.

According to [21] and [31], the resonant frequency between intermediate capacitor and the two inductor should meet criterion as (4.21), which is a loose criterion.

$$f_r = \frac{1}{2 \cdot \pi \cdot \sqrt{C_1 \cdot (L_1 + L_2)}} \, , f_{line} < f_r < f_{sw} \qquad \textbf{(4.21)}$$

For PFC operation, the minimum capacitance requirement comes from low distortion requirement on input current. When capacitance of the intermediate capacitor is too small, large voltage ripple on intermediate capacitor may result the sum of intermediate capacitor voltage and output voltage smaller than input voltage before the main switch turns off. Under this circumstance, due to positive voltage across the input inductor, the input current would continue increase after switch turns off, which is supposed to decrease. The averaged input current would be increased for same duty cycle. For DC-DC converter, this current error can be compensated by high bandwidth feedback control; for PFC working in voltage follower mode, because the single voltage loop bandwidth is much lower than double line frequency, the close loop would not be able to response for this input current error. Thus for PFC circuit, small capacitance of intermediate capacitor may result distortion of input current.

$$V_{in} - \frac{\Delta v_{c1\_pk}}{2} + V_o \geq V_{in} \Rightarrow \Delta v_{c1\_pk} \leq 2 \cdot V_o \qquad \textbf{(4.22)}$$

$$\Delta v_{c1\_pk} \approx \frac{1}{C_1} \cdot \frac{1}{2} \cdot \frac{V_{in}}{L_2} \cdot (D_1 \cdot T_s)^2 \leq 2 \cdot V_o \Rightarrow C_1 \geq \frac{1}{4} \cdot \frac{V_{in}}{V_o} \cdot \frac{(D_1 \cdot T_s)^2}{L_2}$$

$$\qquad \textbf{(4.23)}$$

$$C_1 \geq \frac{1}{4} \cdot \frac{\sqrt{2} \cdot V_{ac\_rms}}{V_o} \cdot \frac{(D_1 \cdot T_s)^2}{L_2}$$

To avoid this distortion, the voltage ripple on intermediate capacitor should meet criterion (4.22). With the approximated peak to peak voltage ripple on intermediate capacitor, as shown in (3.17), the lower limit on capacitance could be derived as (4.23).

The maximum capacitance requirement comes from the intrinsic nature of SEPIC converter that the voltage across intermediate capacitor would follow the input voltage. As shown in Figure 4.3, in SEPIC converter, due to the series loop of intermediate capacitor and two inductor, the input voltage source is connected to a LC filter. The averaged DC value of intermediate capacitor voltage can always track DC component of input voltage. For PFC operation, the rectified input voltage include not only the DC component but also the even order line frequency based components, which can be expand with *Fourier* series as (4.24). From frequency domain point of view, if the corner frequency of the LC filter is f_r, the voltage of intermediate capacitor would be able to track all the even order components whose frequency is less or equal than $f_r/10$ without phase distortion. Thus the upper limit on capacitance can be derived as (4.25).
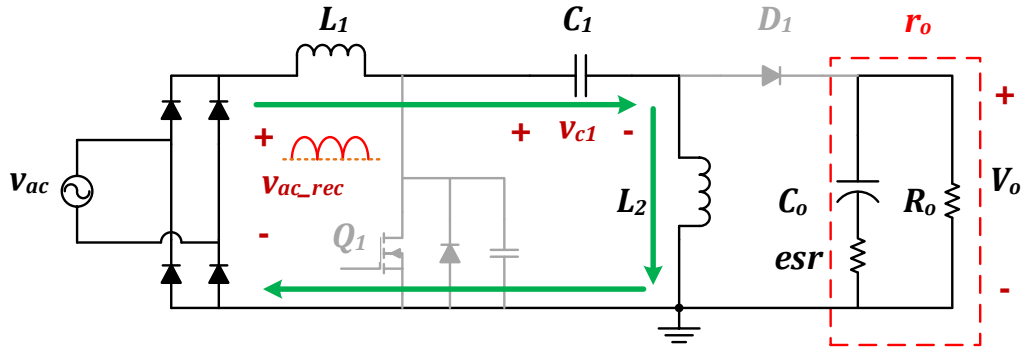

Figure 4.3 Intermediate capacitor charging loop

$$v_{ac\_rec}(t) = \sqrt{2} \cdot v_{ac\_rms} \cdot |\sin(\omega_0 \cdot t)| = \sqrt{2} \cdot v_{ac\_rms} \left[\frac{2}{\pi} - \frac{4}{\pi} \sum_{n=1}^{\infty} \frac{\cos(n \cdot \omega_0 \cdot t)}{4 \cdot n^2 - 1} \right] \qquad \textbf{(4.24)}$$

$$f_r = \frac{1}{2\pi \cdot \sqrt{C_1 \cdot (L_1 + L_2)}} \geq 10 \cdot 2 \cdot n \cdot f_0$$

$$\Rightarrow C_1 \leq \frac{1}{4\pi^2 \cdot (20 \cdot n \cdot f_0)^2 \cdot (L_1 + L_2)} \qquad \textbf{(4.25)}$$

Based on (4.23) and (4.25), for separate inductor implementation, the capacitance selection criteria can be summarized as (4.26).

$$\frac{1}{4} \cdot \frac{\sqrt{2} \cdot V_{ac\_rms}}{V_o} \cdot \frac{\left(D_1 \cdot T_s\right)^2}{L_2} \leq C_1 \leq \frac{1}{4\pi^2 \cdot \left(20 \cdot n \cdot f_0\right)^2 \cdot \left(L_1 + L_2\right)} \qquad \textbf{(4.26)}$$

For coupled inductors, with equivalent de-coupled model discussed in Chapter 3, the lower limit should be modified (3.19) due to the current flowing through the equivalent inductor L_r (3.16) would change the input current shape. For the upper limit, the same principle as separate inductor can be applied to coupled-inductor, but the sum of inductance for the LC filter should be modified. The selection criteria for coupled inductors are shown as (4.27).

$$\frac{L_{1\_equ}}{L_{2\_equ}} \cdot \frac{1}{L_r \cdot k_{rr}} \cdot \frac{D_1}{4\pi \cdot f_{sw}^2} \leq C_1 \leq \frac{1}{4\pi^2 \cdot \left(20 \cdot n \cdot f_0\right)^2 \cdot \sqrt{C_1 \cdot \left(L_1 + L_2 - 2M\right)}} \qquad \textbf{(4.27)}$$

According to the inductances in TABLE. 4.4 and TABLE. 4.5, the capacitance range can is calculated as (4.28) and (4.29).

$$\text{Separate Inductors with } n = 5, f_0 = 60Hz : \ 960nF \leq C_1 \leq 4\mu F \qquad \textbf{(4.28)}$$

$$\text{Coupled-Inductors with } k_{rr} = 1: \ 1.7\mu F \leq C_1 \leq 28.9\mu F \qquad \textbf{(4.29)}$$

4.1.4 Capacitance Design for Output Capacitors

For most PFC converter used in server or telecom equipment, the bulky output capacitors are designed based on the hold-on time. Since this SEPIC front end is designed to support induction cooker, hold-on time would be not necessary. Thus the capacitance is designed based on the output voltage ripple requirement. Due to the difference between fluctuating input power and constant output power is mainly buffered by the output capacitor, voltage ripple on output capacitor are composed by double line frequency ripple and switching frequency ripple. Because the switching frequency is much higher than line frequency, the energy either stored into or released from the output capacitor in one

switching cycle is much lower than the energy stored or released in half line cycle. Thus the voltage ripple magnitude is mainly determined by double line ripple component.
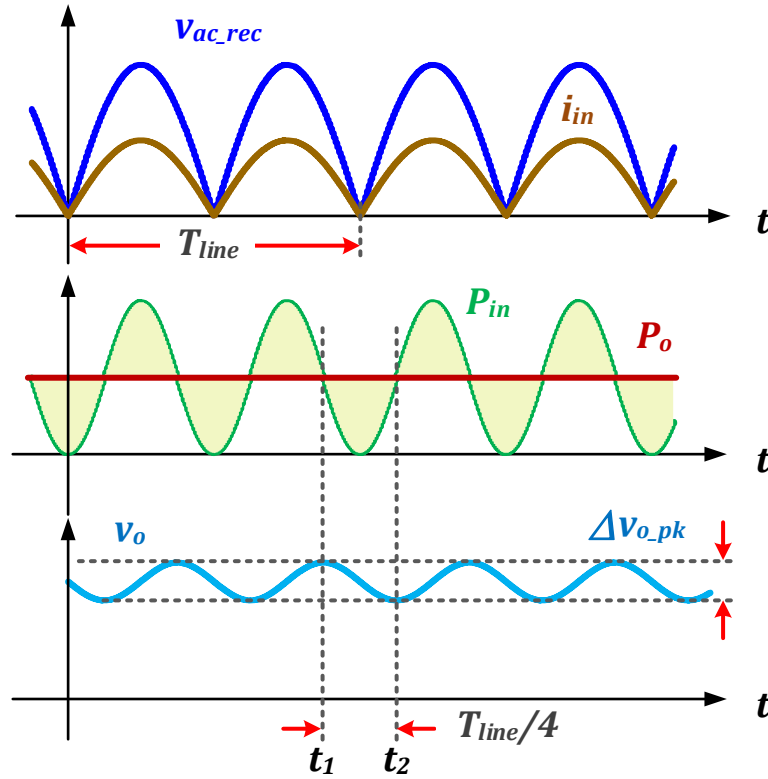

Figure 4.4 Output voltage double line ripple

For this DCM SEPIC PFC converter, capacitance of output electrolytic capacitors is designed based on the imbalance energy accumulated within half line cycle. From Figure 4.4, the energy released from the output capacitor to load within time period [t_1, t_2] can be calculated based on the difference between input power P_{in} and output power P_o, which is shown in (4.30).

$$\frac{1}{2} \cdot C_o \cdot (V_o - \frac{\Delta v_{o\_pk}}{2})^2 - \frac{1}{2} \cdot C_o \cdot (V_o + \frac{\Delta v_{o\_pk}}{2})^2 = \int_{t1}^{t2} \left(P_{in}(t) - P_o(t) \right) \cdot dt \qquad \textbf{(4.30)}$$

$$\Delta v_{o\_pk} = \frac{1}{C_o} \cdot \frac{P_o}{2\pi \cdot V_o \cdot f_{line}} \leq K_{vr} \cdot V_o \Rightarrow C_o \geq \frac{1}{K_{vr}} \cdot \frac{P_o}{2\pi \cdot V_o^2 \cdot f_{line}} \qquad \textbf{(4.31)}$$

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According to the specification, the peak to peak output voltage ripple should be less than 15 V under full load condition. With (4.31), capacitance of output electrolytic capacitors should be larger than 3 mF for 60V output and 2mF for 100V output.

$$C_o \geq 3mF \tag{4.32}$$

4.1.5 Open Loop Simulation

To verify the designed parameters, simulation circuit shown in Figure 4.5 is used. Simulation parameters are listed in TABLE. 4.6 and TABLE. 4.7. Simulation results are presented with Figure 4.6, Figure 4.7 and Figure 4.8.
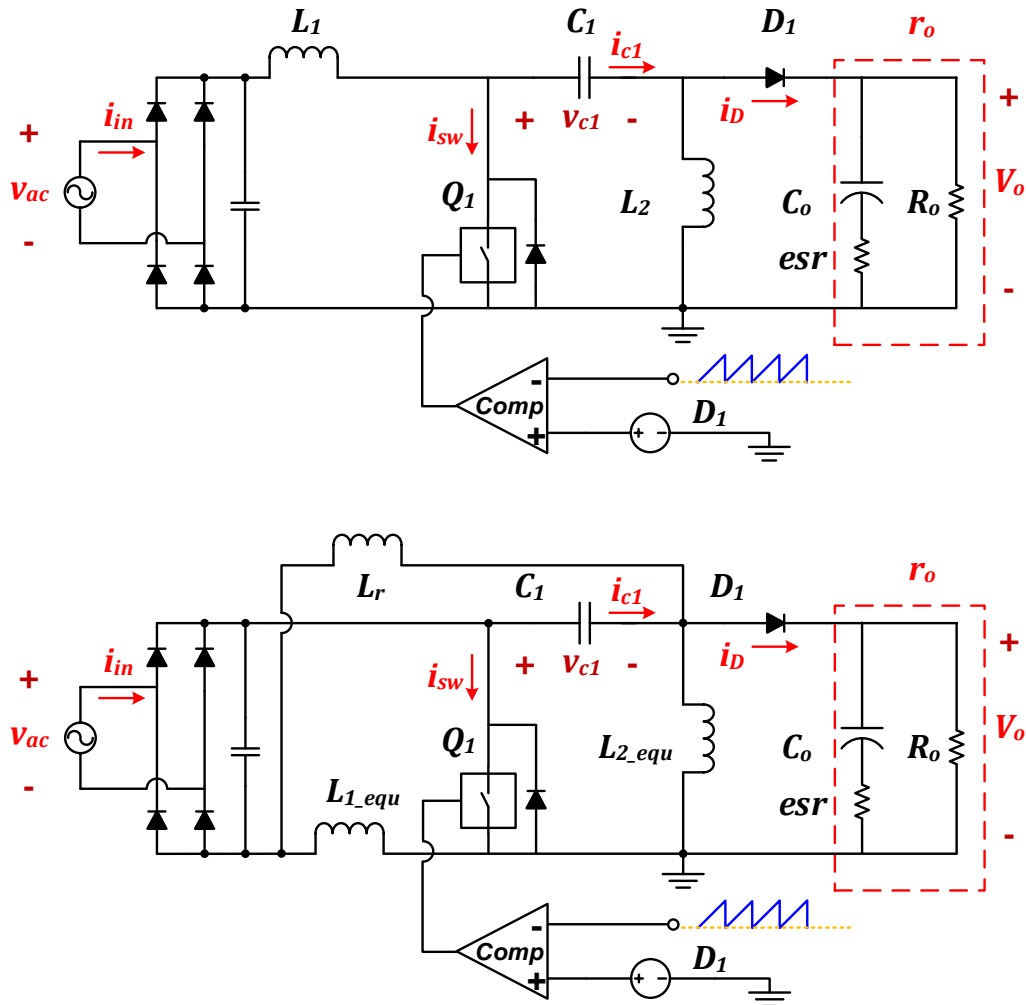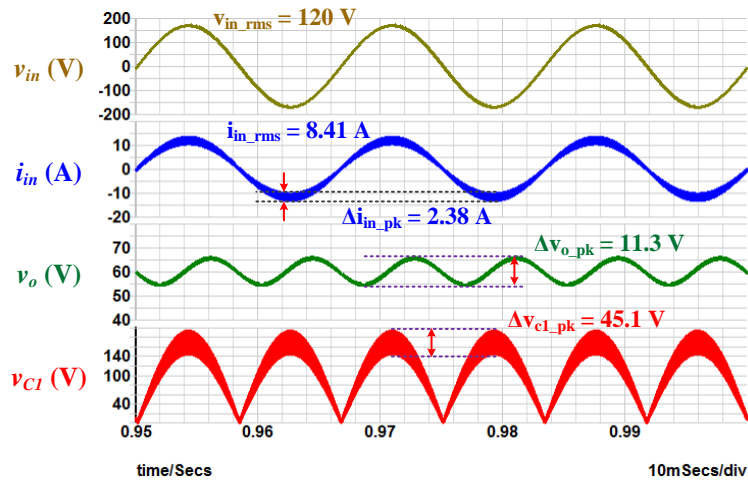

Figure 4.5 Open-loop simulation with designed parameters

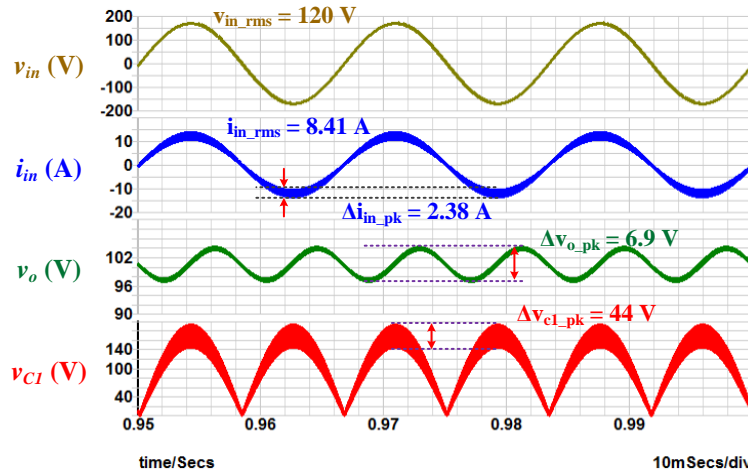**TABLE. 4.6 Simulation parameters for separate inductors**

L_1	L_2	C_1	C_o	C_o ESR	R_o
171 μH	4.6 μH	2 μF	4mF	5mΩ	3.6Ω, 10Ω

TABLE. 4.7 Simulation parameters for coupled-inductors

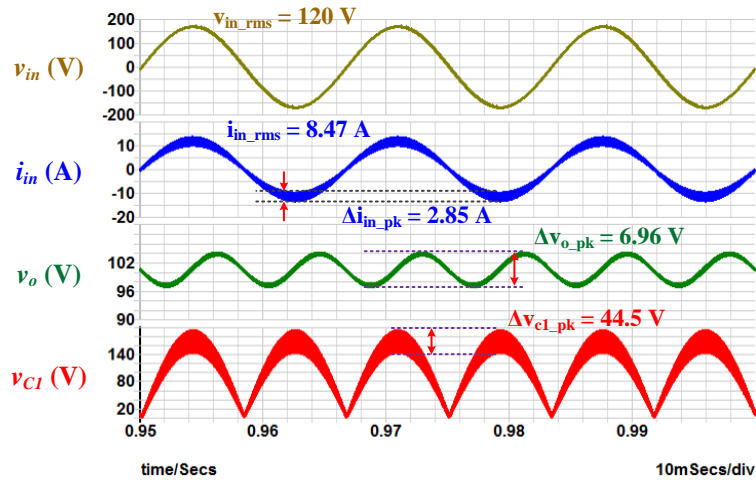| L_{1_equ}	L_{2_equ}	L_r	C_1	C_o	C_o ESR	R_o
132 μH	5.2 μH	29.7 μF	2 μF	4mF	5mΩ	3.6Ω, 10Ω

(a) 60V 1kW with Separate Inductors

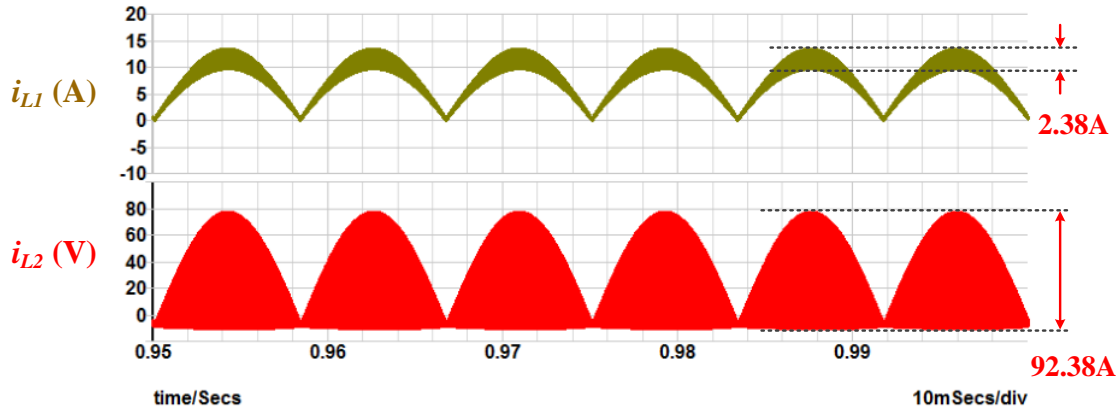(b) 100V 1kW with Separate Inductors

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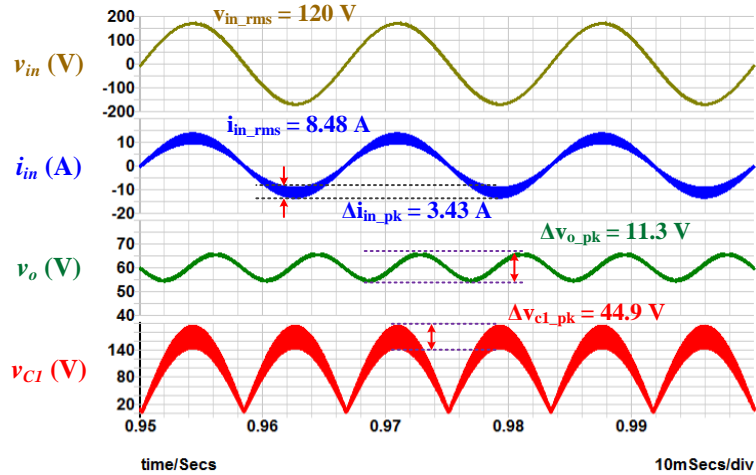
(c) 60V 1kW with Coupled Inductors

(d) 100V 1kW with Coupled Inductors

Figure 4.6 PFC function waveforms

As seen from Figure 4.6, for the designed parameters, PFC function is verified at 1 kW output with 60V and 100V output. The voltage ripple on output is less than the required 15V. For the input current, due to the input equivalent inductance of coupled inductors is smaller than the case with separate inductors, the input current ripple is higher than separate inductor case.
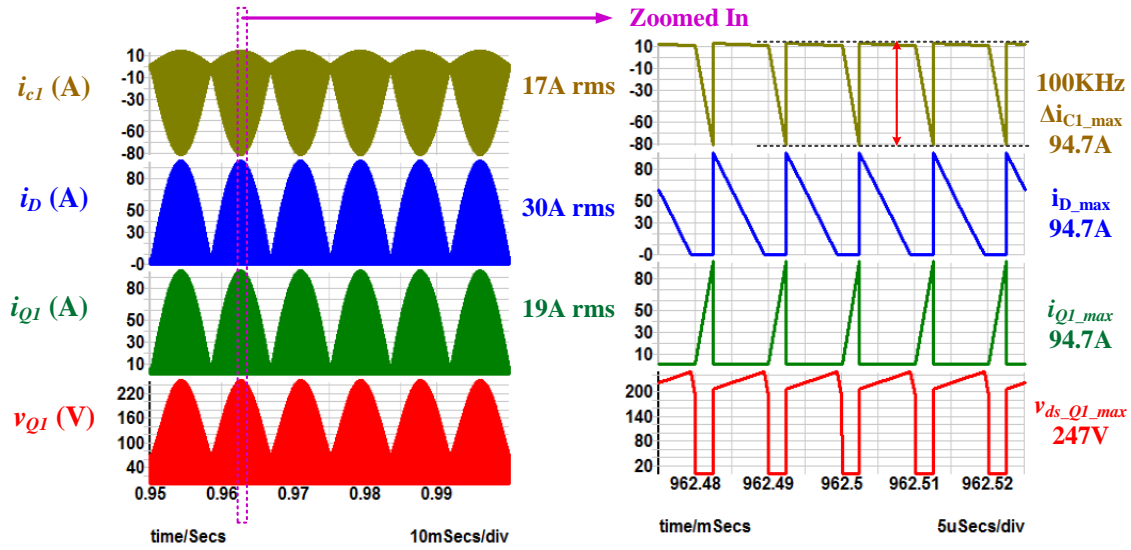
(a) 60V 1kW with Seperate Inductors
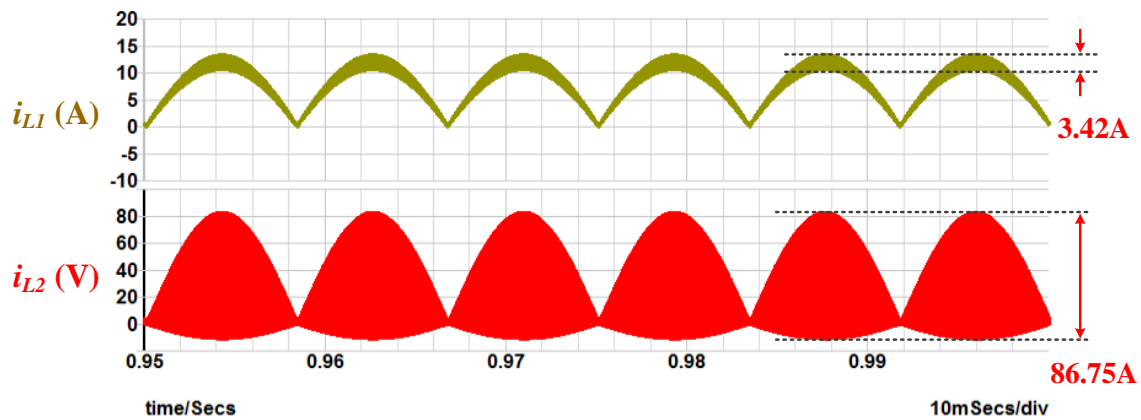
(b) 60V 1kW with Coupled Inductors

Figure 4.7 Inductor current waveforms

As seen from Figure 4.7, because the equivalent inductances of coupled inductors are different to the inductance of the separate inductors, the current ripple in two cases are different.

From the simulation parameters, the equivalent input inductance of coupled inductors case is lower than the input inductance of separate inductors case, thus the input current ripple is higher for coupled inductors case. For the current ripple of output inductor, it's opposite. With coupled inductors, while almost same input current ripple is achieved, the self-inductance of L_1 (27.54 µH) with coupled inductors is reduced more than 80% compared to the inductance of L_1 (171 µH) with separate inductors.

(a) 60V 1kW with Seperate Inductors
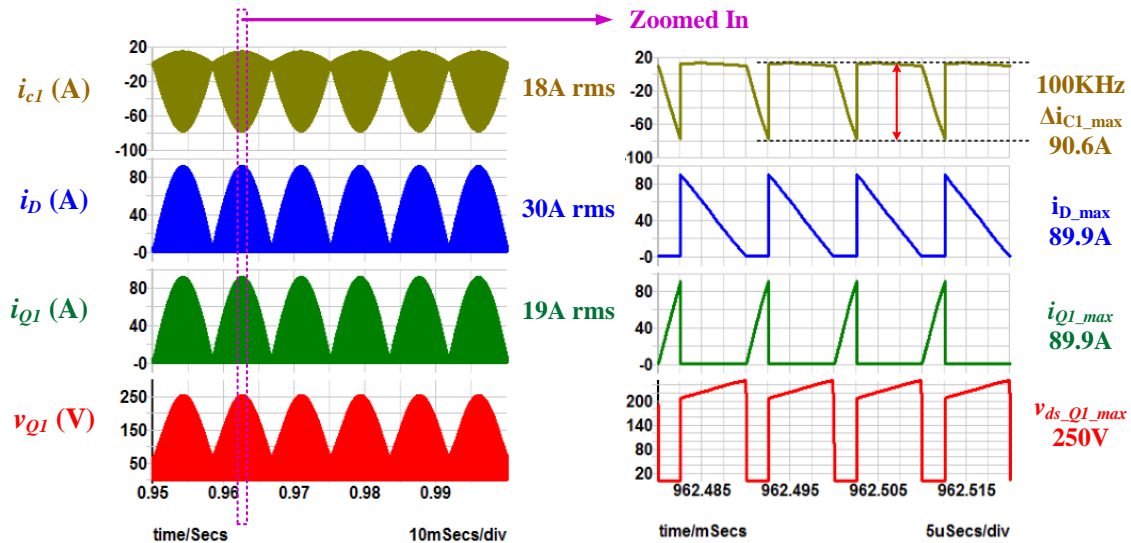
(b) 60V 1kW with Coupled Inductors

Figure 4.8 Components stress

The current stress of main switch, output diode and intermediate capacitor are presented in Figure 4.8. For the intermediate capacitor, large current swing can be observed, thus the intermediate capacitor should be selected with very good 100 kHz current conducting capability.

The voltage stress on main switch is same as output diode, both equals to the sum of input voltage and output voltage.

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4.1.6 Components Selection

Based on the voltage and current stress, the selected power stage components are listed in TABLE. 4.8.

TABLE. 4.8 Selected components

	Part	Manufacture
Input Diode Bridge	**GBPC3506W**	Diodes
Main Switch	**FCH041N60F**	Fairchild
Output Diode	**VS-60APU04**	Vishay
Intermediate Capacitor	**MP88BG105-**	Electronic Concept
Output Capacitor	**ECEC2EP102DX**	Panasonic
	B32674D3106K	TDK

4.2 Controller Design and Implementation

For PFC operating in voltage follower mode, single voltage loop control structure can be used. According to the control to output small signal model derived in Chapter 2, voltage loop compensator can be designed for separate inductors case first. According to analysis in Chapter 3, the adoption of coupled inductors only changes the LHP double pole and RHP double zero, it does NOT change the low frequency characteristics of the power plant transfer function. Because the bandwidth of voltage loop should be lower than one tenth of double line frequency to attenuate the double line ripple content from the output voltage, within this bandwidth, with the equivalent inductance model, the transfer function of power plant with coupled inductors can be predicted by transfer function of power plant with separate inductors. Both can be approximated with (2.30) and (2.31).

4.2.1 Plant Transfer Function of Control to Output

Based on the analysis in Chapter 2, the transfer function of control to output can be calculated numerically.

With the designed parameters, the corresponding bode plots for coupled inductors case are illustrated in Figure 4.9.
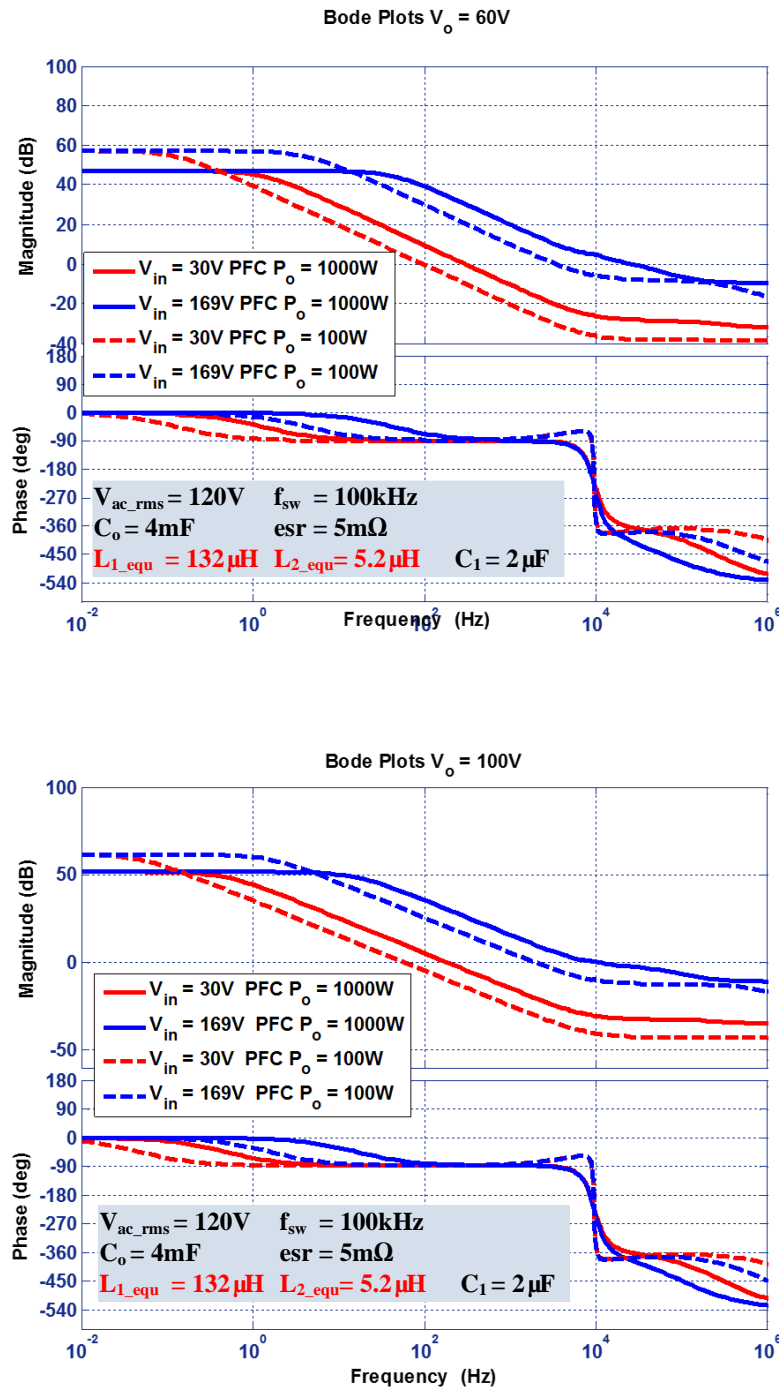

Figure 4.9 Bode plots of control to output with coupled inductors

4.2.2 Compensator and Notch Filter Design

Based on the control to output transfer function, a PI compensator is designed as (4.33). The bandwidth of the voltage loop gain is set around 10 Hz to attenuate the double line ripple on output voltage.

$$G_v(s) = K_p + \frac{K_i}{s} = K_p \cdot K_i \cdot \frac{\dfrac{s}{K_i} + 1}{s} = 0.03 \times \frac{\dfrac{s}{5} + 1}{s} \tag{4.33}$$

The double line ripple on output voltage brings double line ripple component in the control signal (the duty cycle), which would generate third harmonics in input current and eventually results high THD value. To reduce the amplitude of the third harmonics in the input current, a notch filter could be inserted before the compensator to further attenuate the double line ripple component from the output voltage.

The transfer function of a notch filter is shown in (4.34). Since the notch filter is designed to attenuate the double line frequency ripple, the notch filter frequency ω_d is selected as double line frequency.

$$G_{notch}(s) = \frac{\dfrac{s^2}{\omega_d^2} + \dfrac{s}{\omega_d \cdot Q_n} + 1}{\dfrac{s^2}{\omega_d^2} + \dfrac{s}{\omega_d \cdot Q_d} + 1} \tag{4.34}$$

Bode plots of the denominator and the numerator are illustrated in Figure 4.10 and Figure 4.11. Because the bandwidth of the PFC converter is usually designed below than the double line frequency, the preferred attenuation gain of the notch filter should be as low as possible. If the preferred bandwidth of the converter is higher than notch filter frequency, (which is almost none in practical PFC designs without notch filter), then the attenuation gain of the notch filter should be as high as possible.

For the low bandwidth PFC application, selection of Q_d, should make the second-order system $1 \Big/ \left(\dfrac{s^2}{\omega_d^2} + \dfrac{s}{\omega_d \cdot Q_d} + 1 \right)$ slightly under-damped or over-damped. From Figure 4.10, large Q_d would result under-damped system, sharp phase drop and high gain at double

line frequency, both are not preferred. Small Q_d would result over-damped system, phase-drop start at lower frequency region, which may result reduced phase margin.
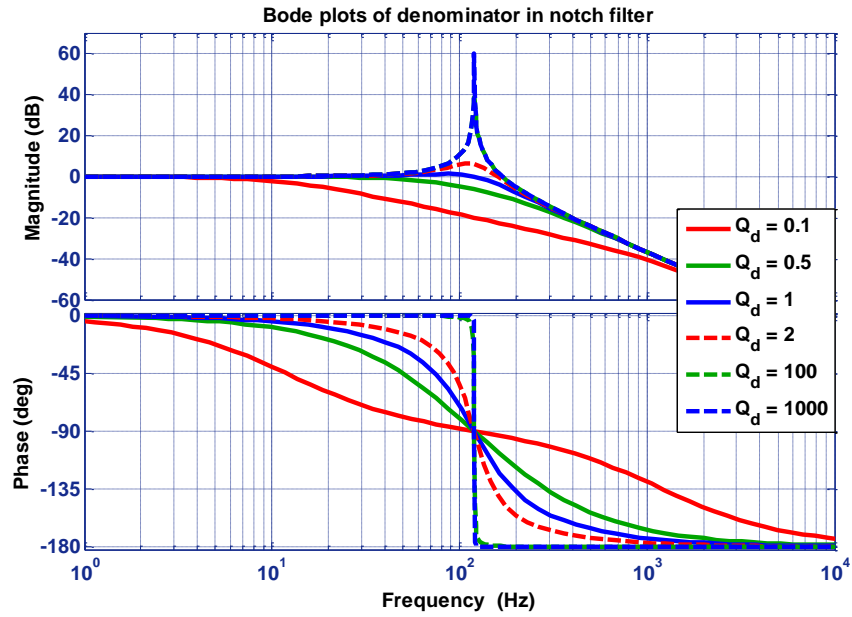

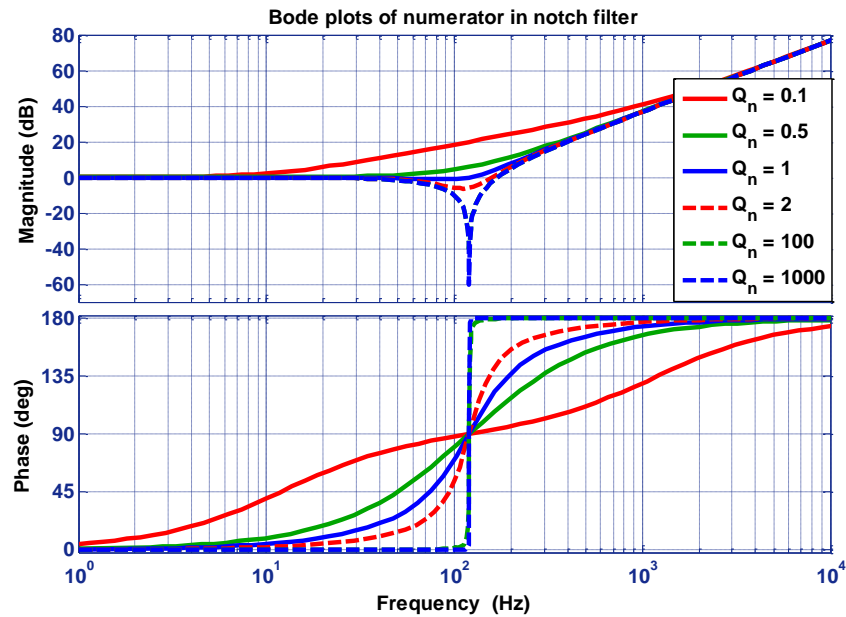**Figure 4.10 Bode plots of the denominator in notch filter**

Figure 4.11 Bode plots of the numerator in notch filter

For the selection of quality factor Q_n, as shown in Figure 4.11, under-damped system is preferred due to low gain and quick phase boost at double line frequency. Smaller Q_n may not be able to provide enough attenuation to double line ripple. From these observations, the notch filter parameters are selected as (4.35).

$$\omega_d = 2\pi \cdot 2 \cdot f_{line}, Q_d = 1, \ Q_n = 2000 \tag{4.35}$$

The loop gain for different conditions are shown in Figure 4.12. With simple PI controller, it's hard to limit the bandwidth below than 12Hz for all conditions. With the help of notch filter, the attenuate gain is provided by notch filter itself, then the double line ripple attenuation still can be achieved even the voltage loop gain has higher bandwidth. Since when output voltage is 60V and input voltage is the peak value, the loop gain has the highest bandwidth, which is the worst case for double line ripple attenuation. Thus the effect of notch filter is illustrated under this condition as Figure 4.13. The loop gain with the notch filter is compared to loop gain without the notch filter. It's clear that notch filter provides extra attenuation gain at double line frequency.
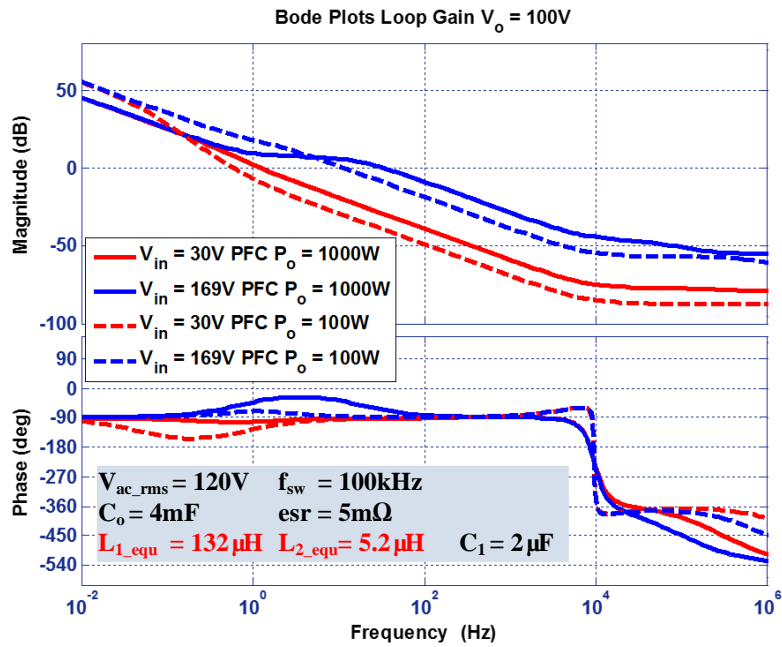
Bode Plots Loop Gain $V_o = 100V$
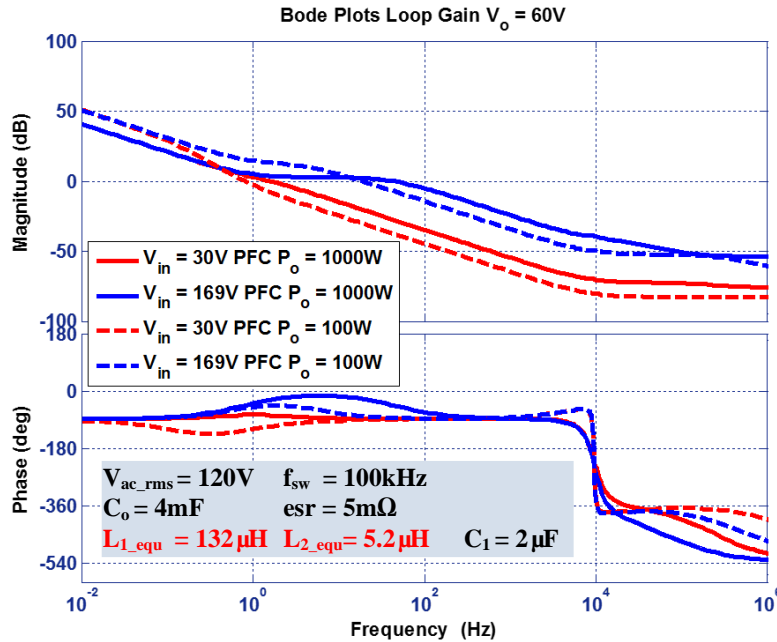
Figure 4.12 Bode plots of loop gain with coupled inductors

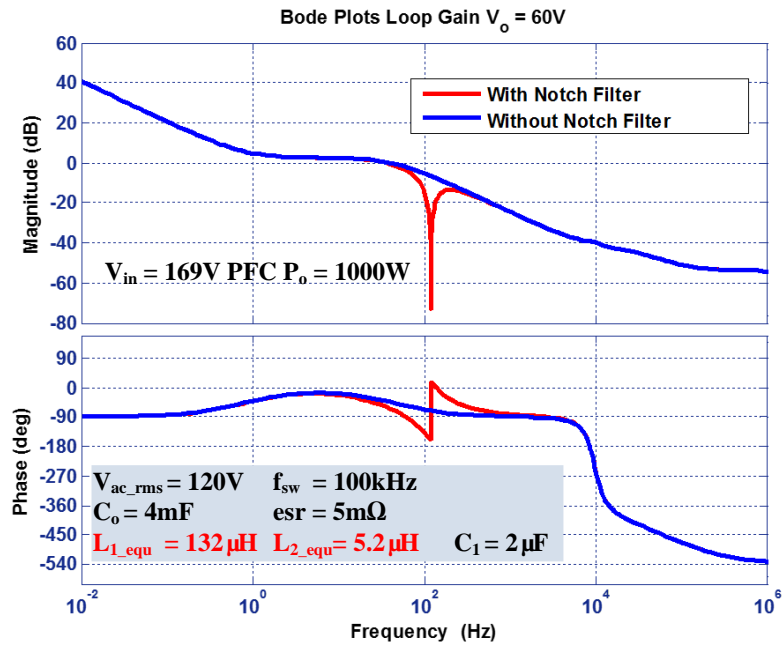**Bode Plots Loop Gain $V_o = 60V$**

Figure 4.13 Effects of notch filter

4.2.3 Closed Loop Simulation

To verify the designed compensator and notch filter, simulation circuit shown as Figure 4.14 is built in PSIM.
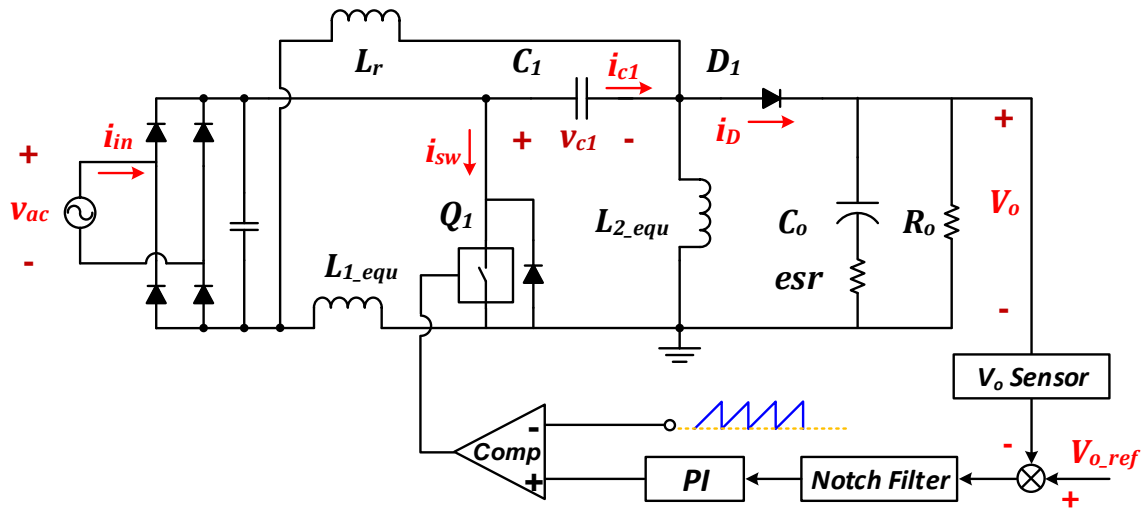
Figure 4.14 Close loop simulation

The simulation results for simple PI controller are shown in Figure 4.15. With the designed notch filter, the simulation results are shown in Figure 4.16. Compared to the simple PI controller, adding notch filter reduced the THD value. Correspondingly, the input current frequency spectrum comparison between with and without notch filter are shown in Figure 4.17, from which it can be seen the notch filter greatly reduced the magnitude of third order harmonics in input current.
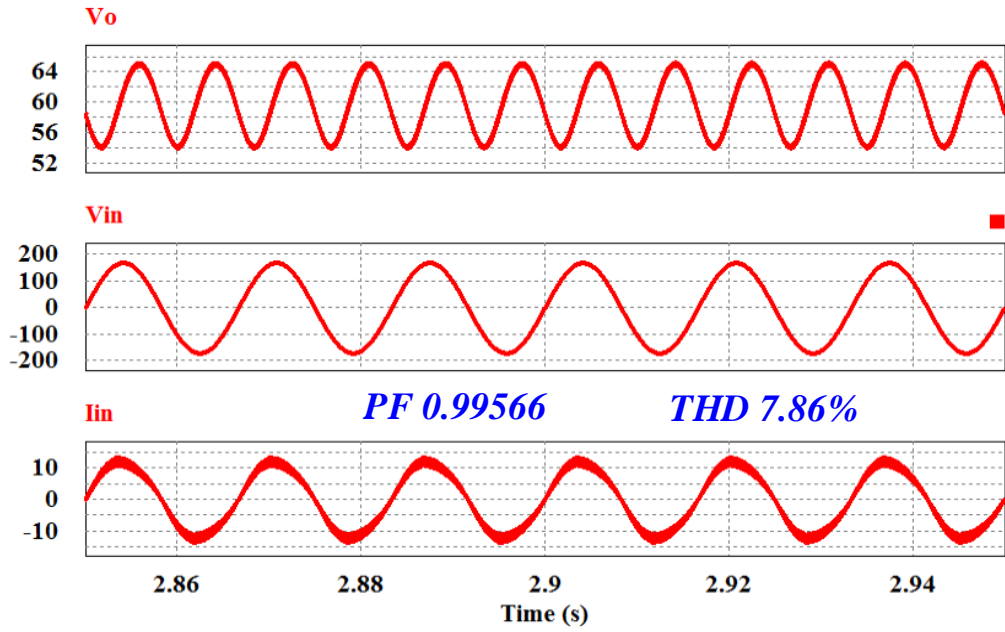
(a) 60V 1kW Closed Loop with L_{1equ} and L_{2equ}
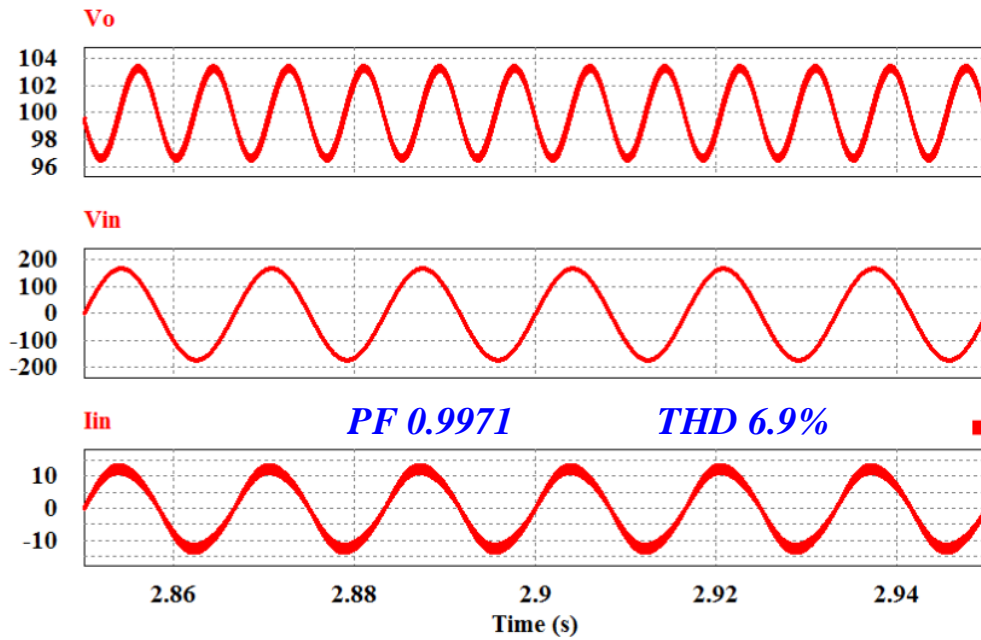
(b) 100V 1kW Closed Loop with L_{1equ} and L_{2equ}

Figure 4.15 Close loop simulation results without notch filter
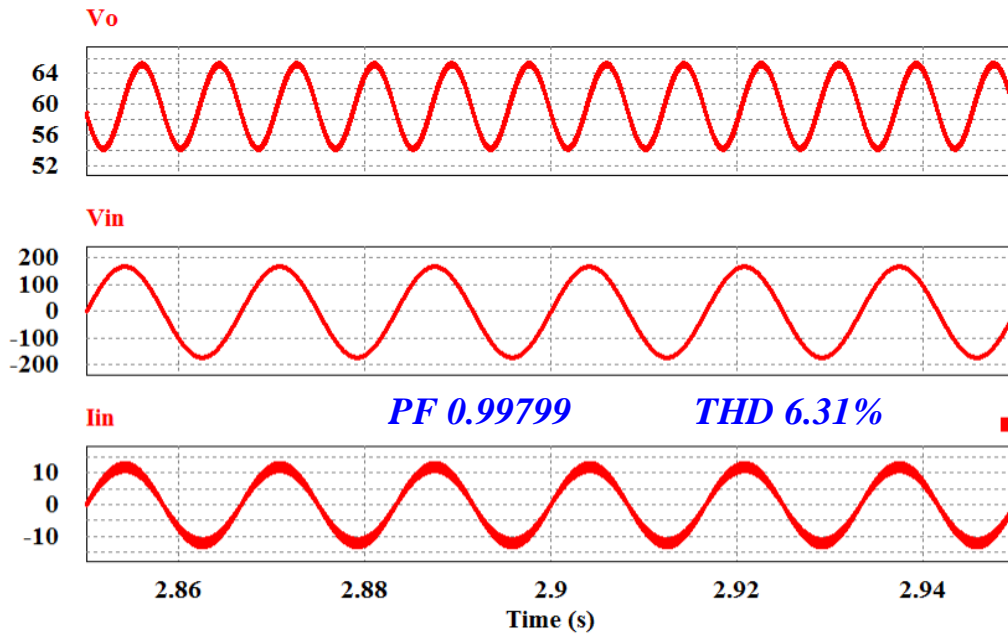
PF 0.99799   THD 6.31%

(a) 60V 1kW Closed Loop with L_{1equ} and L_{2equ}

PF 0.9979   THD 6.327%

(b) 100V 1kW Closed Loop with L_{1equ} and L_{2equ}

Figure 4.16 Close loop simulation results with notch filter
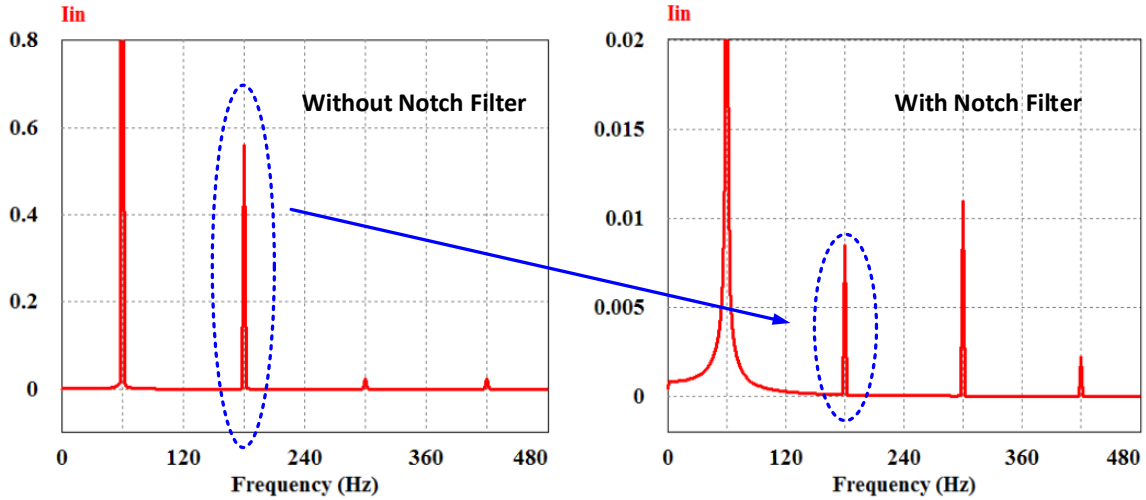
(a) 60V 1kW Closed Loop with L_{1equ} and L_{2equ}
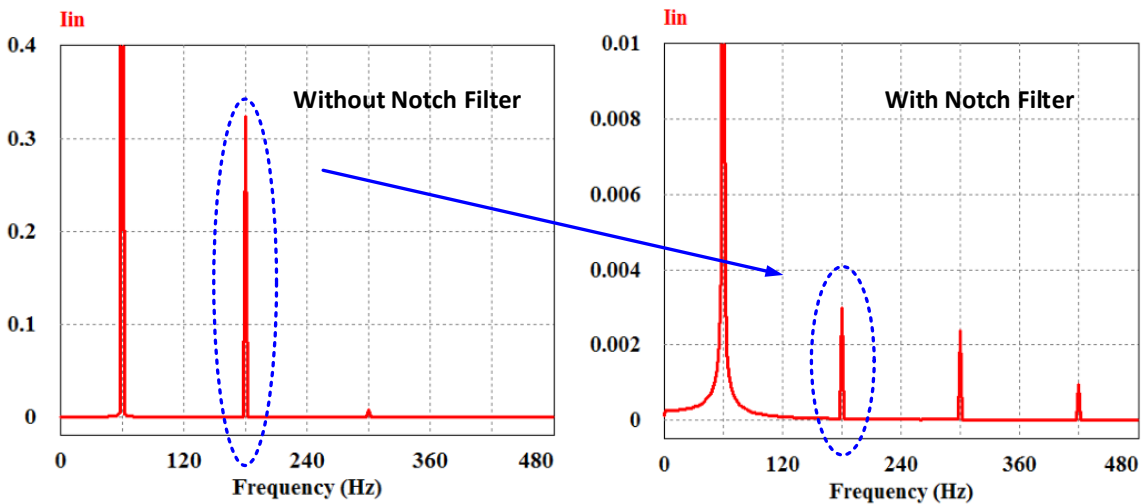
(b) 100V 1kW Closed Loop with L_{1equ} and L_{2equ}

Figure 4.17 Input current harmonics comparison

The system response to output voltage command step change are shown in Figure 4.18 and Figure 4.19. Due to the low bandwidth, the settling time are longer than half second. During the transition, the unity power factor operation is maintained after half line cycle.
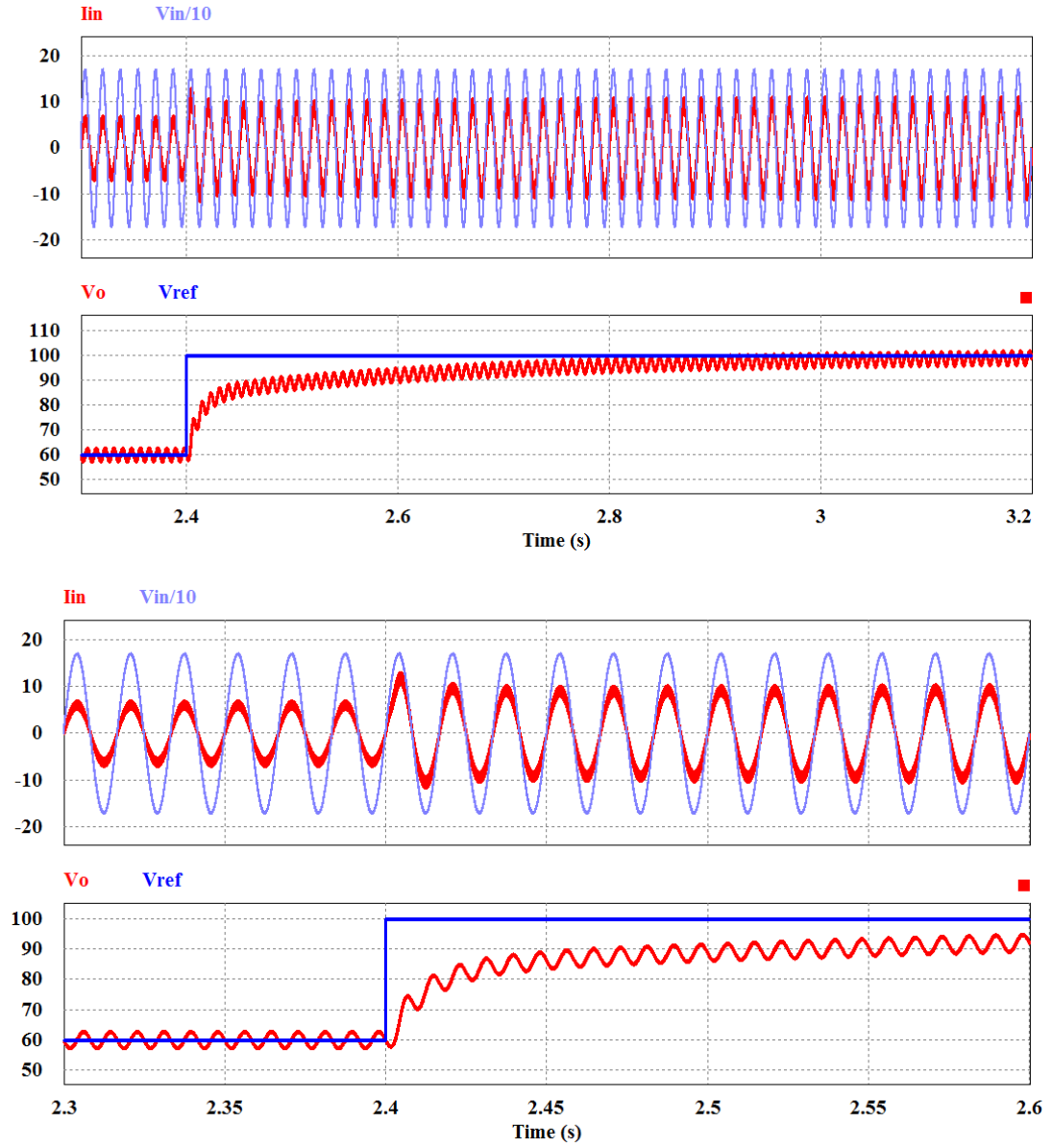
Figure 4.18 Output voltage step-up response
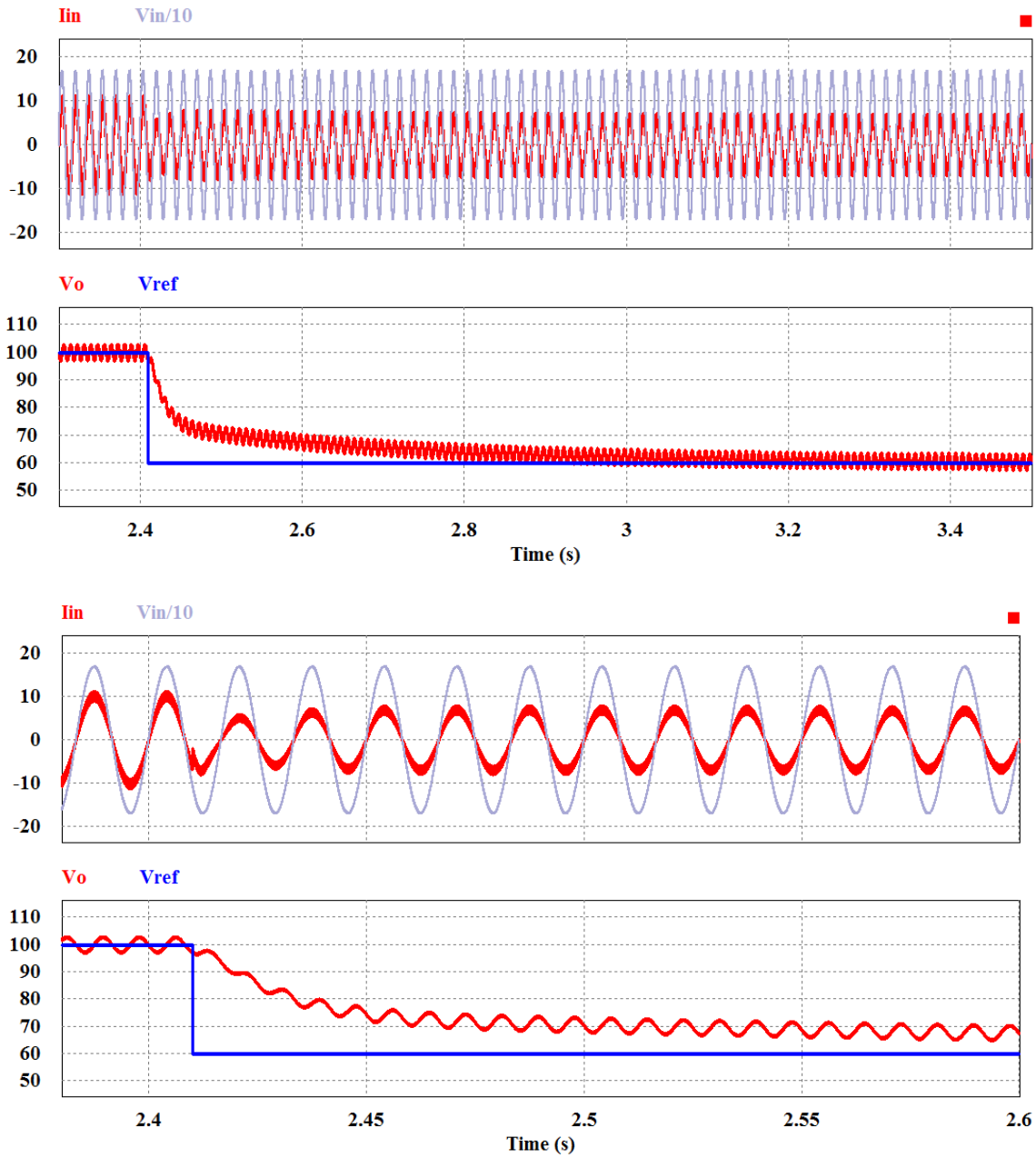
Figure 4.19 Output voltage step-down response

Chapter 5:
Experimental Results
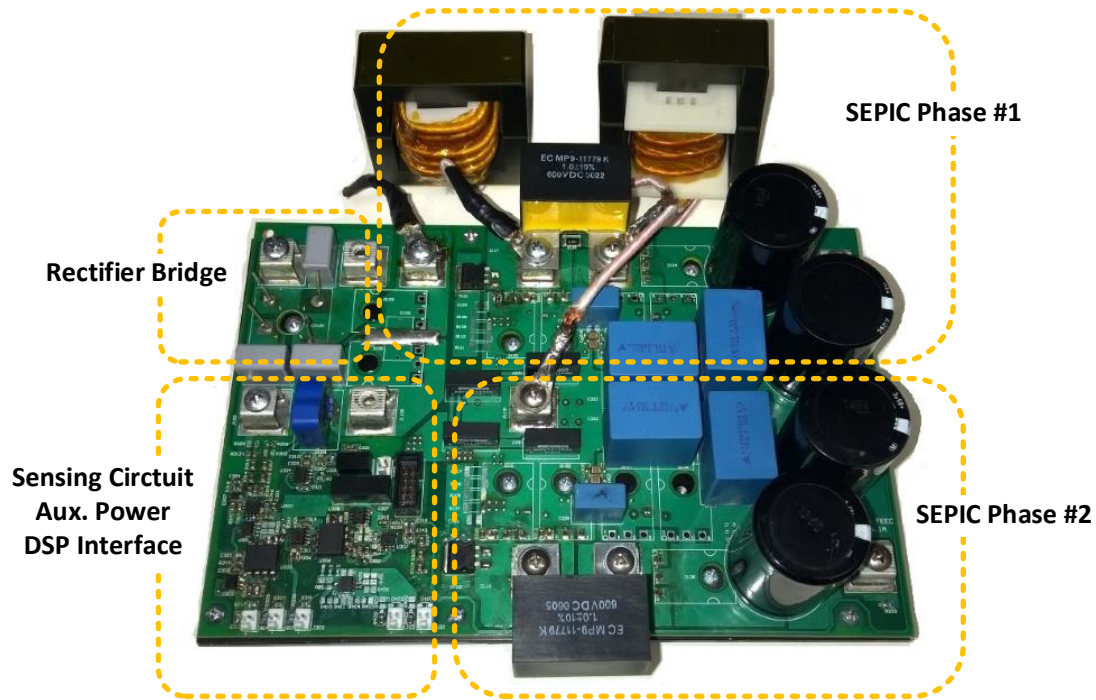
Figure 5.1 SEPIC PFC power stage

As shown in Figure 5.1, the prototype includes two sets of SEPIC converter. By changing the jumper connection, the prototype can be configured as interleaving structure or bridgeless structure. In this chapter, all the waveforms and test results are based on 1 kW design, only one phase of the prototype is used.

5.1 PFC Operation Waveforms

With closed voltage loop, experimental waveforms of DCM SEPIC PFC under full load condition are shown in Figure 5.2. The input current THD value, power factor and displacement power factor are measured by Yokogawa WT1600 digital power meter. Parameters of coupled inductors and separate inductors are listed in TABLE. 4.6 and TABLE. 4.7.

Input Current THD 3.0% PF 0.9565 DF 1.0

v_{in} (100V/div)

i_{L1} (10A/div)

v_o (20V/div)

i_{L2} (50A/div)

Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:max(C3)	P5:max(C4)	P6:freq(C1)
value	120.20 V	8.17 A	26.8 A	80 A	66.9 V	60.012985 Hz
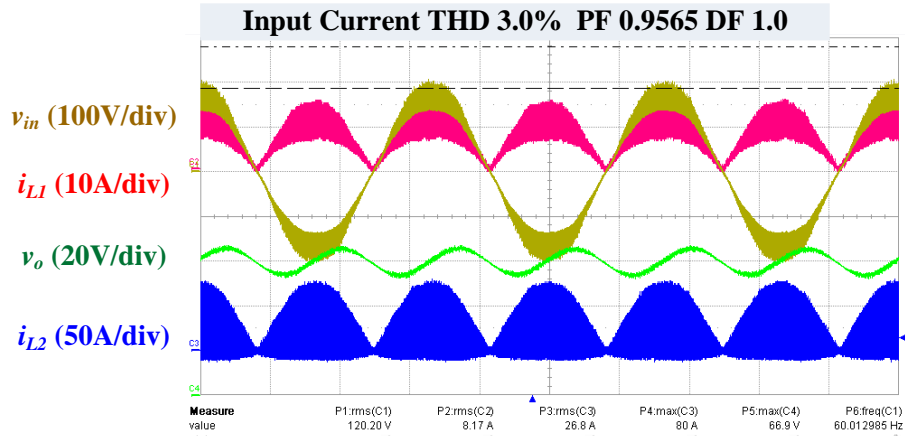
(a) V_o=60V I_o=16A with Coupled Inductors

Input Current THD 3.08% PF 0.9976 DF 1.0

v_{in} (100V/div)

i_{L1} (10A/div)

v_o (20V/div)

i_{L2} (50A/div)

Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:max(C3)	P5:max(C4)	P6:freq(C1)
value	120.48 V	8.50 A	28.8 A	82 A	69.5 V	59.988362 Hz
status						
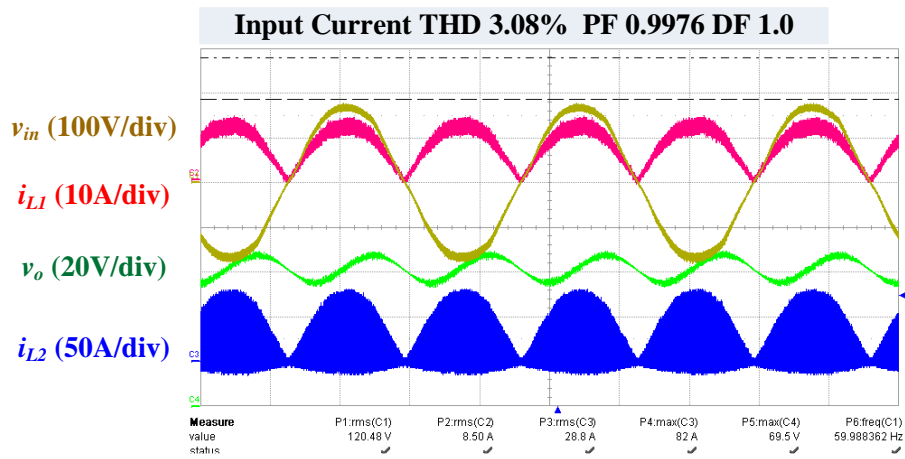
(b) V_o=60V I_o=17A with Separate Inductors

Input Current THD 2.82% PF 0.9923 DF 1.0

v_{in} (100V/div)

i_{L1} (5A/div)

v_o (20V/div)

i_{L2} (50A/div)

Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:max(C3)	P5:max(C4)	P6:freq(C1)
value	120.22 V	7.98 A	23.5 A	79 A	107.2 V	60.025811 Hz
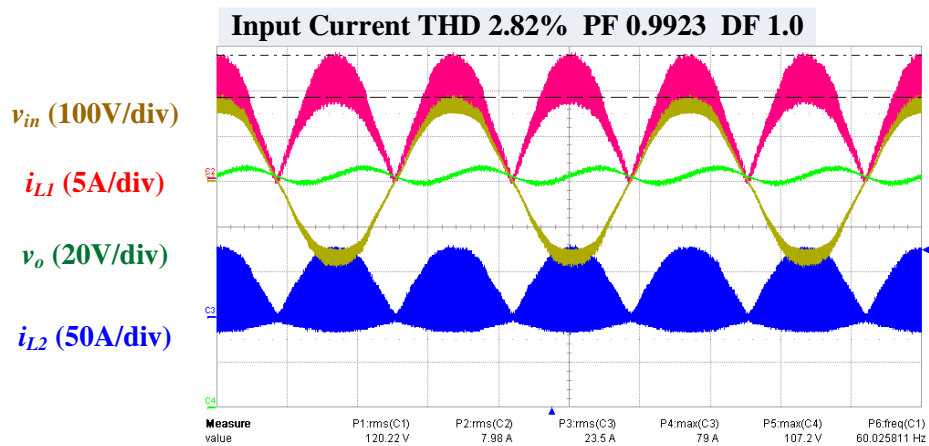
(c) V_o=100V I_o=9.6A with Coupled Inductors

Input Current THD 2.93% PF 0.9975 DF 1.0

v_{in} **(100V/div)**

i_{L1} **(5A/div)**

v_o **(20V/div)**

i_{L2} **(50A/div)**

Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:max(C3)	P5:max(C4)	P6:freq(C1)
value	119.62 V	8.18 A	24.8 A	83 A	108.2 V	0 GHz
status						
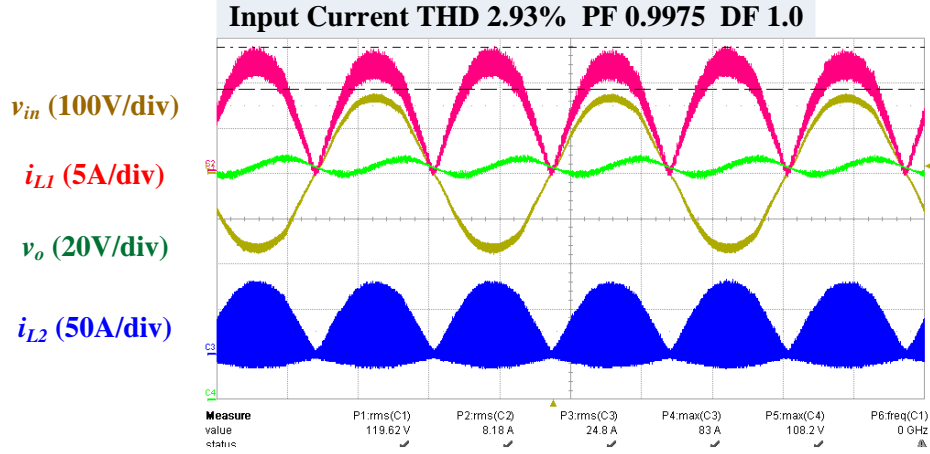
(d) V$_o$=100V I$_o$=10A with Separate Inductors

Figure 5.2 Experimental waveforms

From the measurements, at full load condition, unity displacement power factor is achieved for both 60V and 100V output, with separate inductors, high power factor (larger than 0.997) and low input current THD (lower than 3.5%) are achieved for both 60V and 100V output; with coupled inductors, due the equivalent input inductance L_{1equ} (132 μH) is smaller than the input inductance L_1 (171 μH) of separate inductors, higher input current ripple, higher THD and lower power factor are observed.

5.2 Power Factor and THD Measurements

For different load conditions, displacement factor and THD of input current are measured with Yokogawa WT1600 digital power meter, which are shown in Figure 5.3 and Figure 5.4. Again, as stated for full load condition, the lower equivalent input inductance of coupled inductors results lower power factor and higher input current THD.

Much higher input current THD value are observed at low load condition. According to (4.6), for the input current, the ratio of switching current ripple's magnitude to fundamental current magnitude is inversely proportional to output power level. Thus for output power higher than 200W, low frequency harmonics content dominates the total harmonics, which results relative flat curves as output power increase; for output power lower than 200W, switching frequency harmonics dominates the total harmonics.
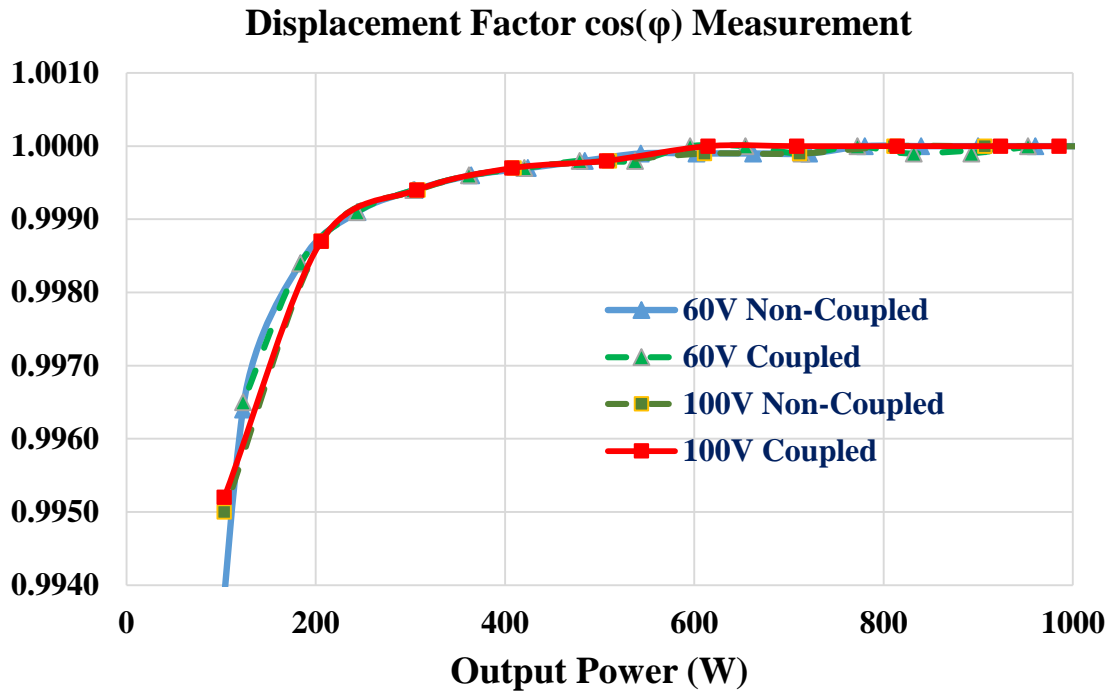
Figure 5.3 Measured displacement factor cos(φ)

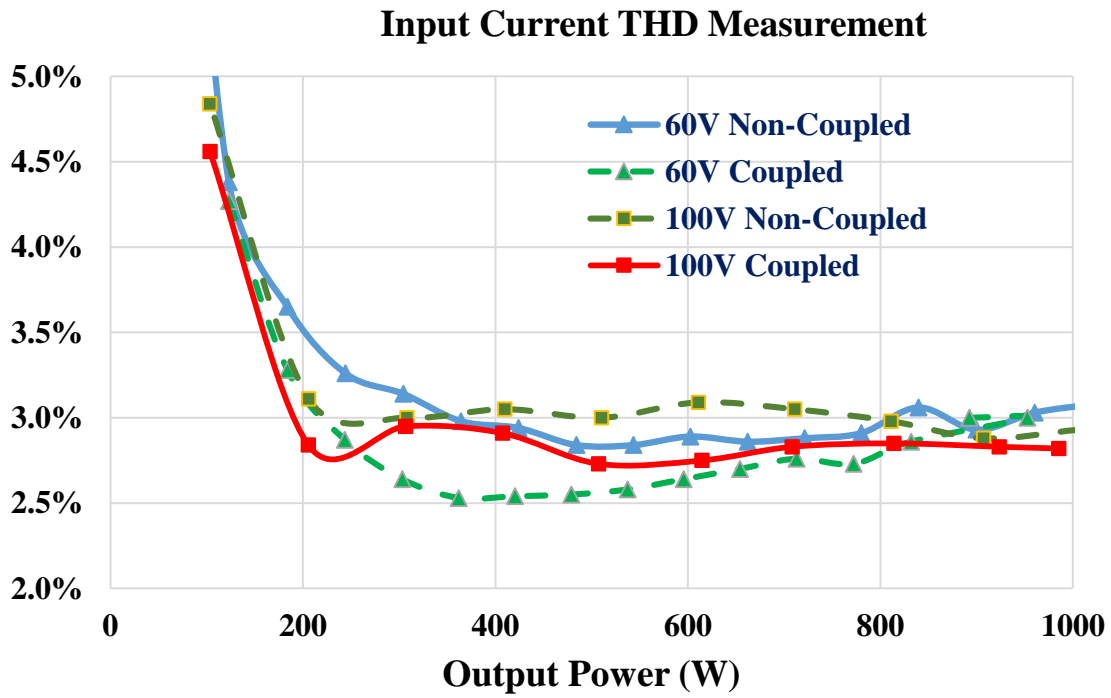**Figure 5.4 Measured THD of input current**

5.3 Efficiency and Loss Break Down

Efficiency Measurement
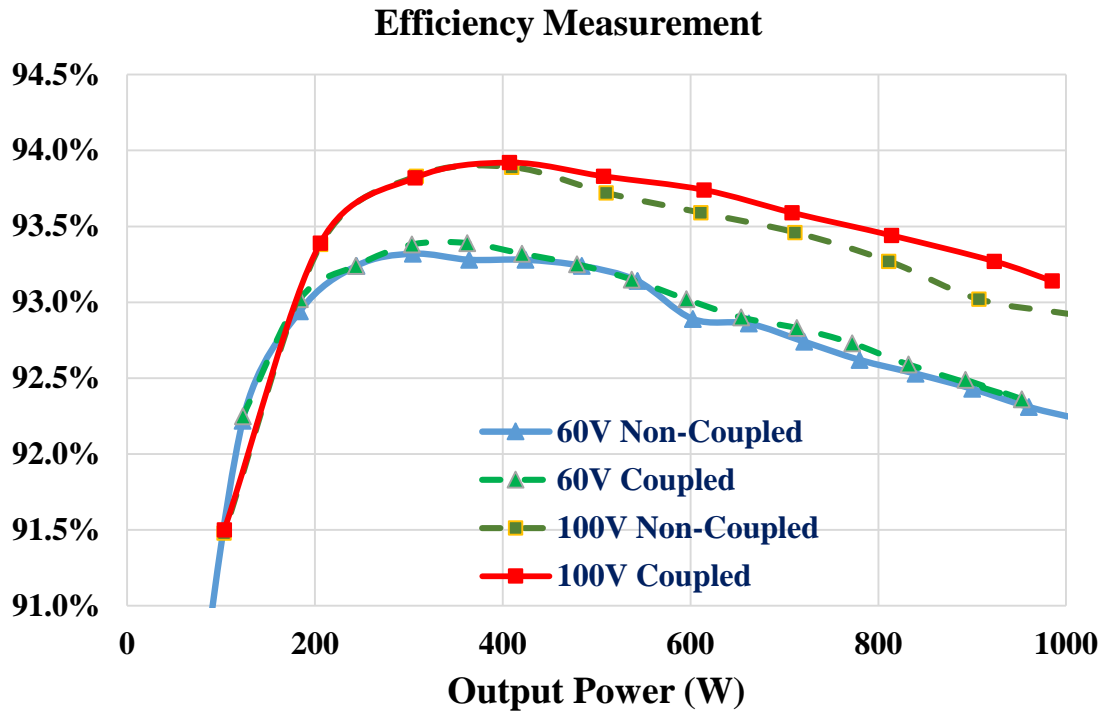
Figure 5.5 Measured efficiency

Measured efficiency curves are shown in Figure 5.5. Compared to 100V output condition, for same output power, 60V output case delivers around 50% higher output current, thus the efficiency at heavy load condition is around 0.8% lower than 100V output case. At light load condition, as the switching loss of 100V output case is higher than 60V output case, the efficiency curves cut across each other.

To further analyze the efficiency, losses of components are calculated with equivalent DC-DC SEPIC converter in a cycle by cycle manner. For half line cycle, based on instant input AC voltage and instant power, losses in each switching cycle are calculated and summed up together. With this method, the calculated efficiency for full load condition, are 93.81% for 100V output and 92.97% for 60V output, which are close to the measurements. The calculation results are shown in Figure 5.6, in which, the ESR conduction loss includes the winding loss of two inductors, the ESR loss of output capacitor.

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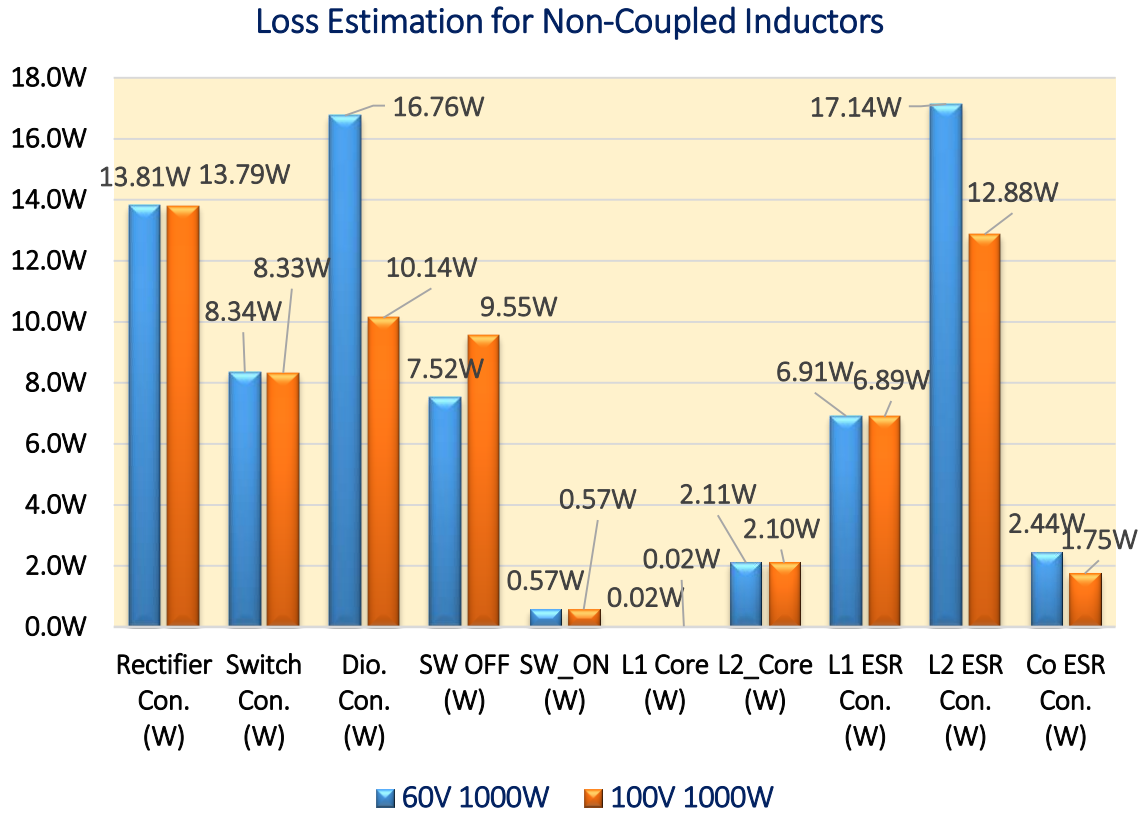
Figure 5.6 Estimated loss break down

5.4 Transient Response for Load Transient

Figure 5.7 presents the system transient response to the step changes on output voltage reference with fixed output current. The output voltage reference is set to step between 60V to 100V with 5A output current. The settling time from the test results are around 0.5s.
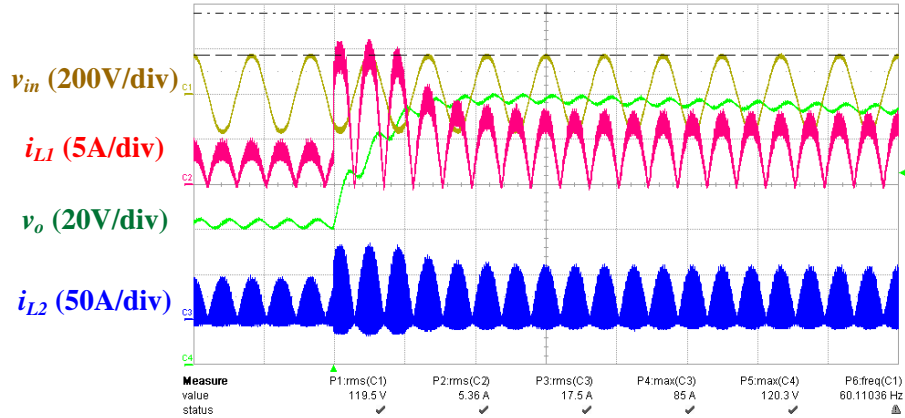
(a) V_o=60V to V_o=100V fixed I_o=5A with Separate Inductors
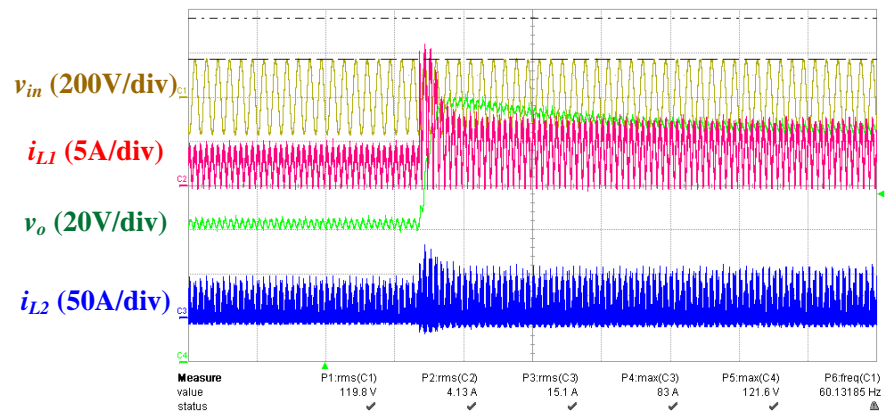
(b) V_o=60V to V_o=100V fixed I_o=5A with Separate Inductors

(c) V_o=100V to V_o=60V fixed I_o=5A with Separate Inductors

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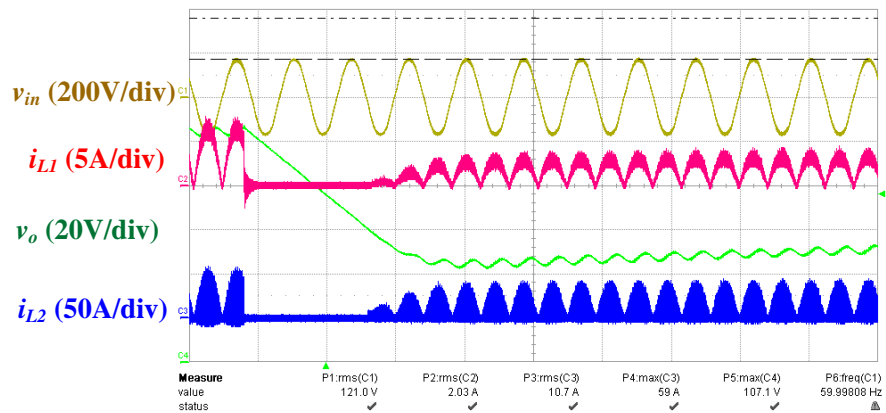
Measure	P1:rms(C1)	P2:rms(C2)	P3:rms(C3)	P4:max(C3)	P5:max(C4)	P6:freq(C1)
value	120.5 V	2.81 A	12.9 A	59 A	108.6 V	59.91415 Hz
status	✓	✓	✓	✓	✓	⚠
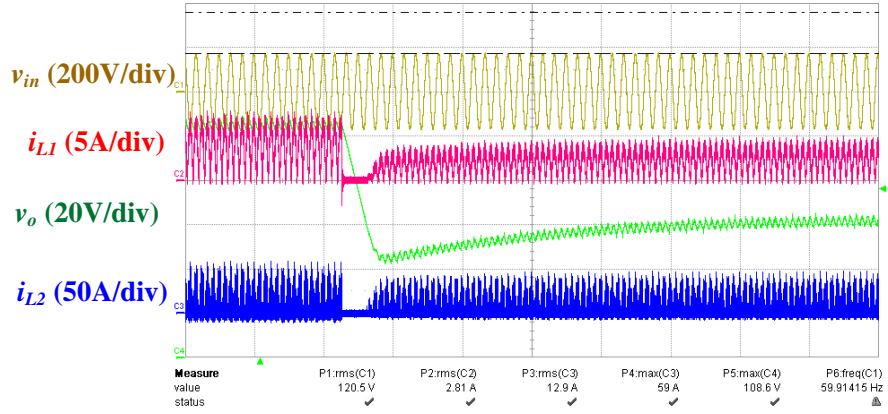
(d) V$_o$=100V to V$_o$=60V fixed I$_o$=5A with Separate Inductors

Figure 5.7 Transient response of output voltage reference step

Chapter 6:
Conclusion and Future Work

6.1 Conclusion

The thesis presents the system design procedure and experimental results of a 1 kW DCM SEPIC PFC converter with adjustable output voltage from 60V to 100V. As demonstrated in circuit analysis, simulation and experimental results, the merits of DCM SPEIC PFC can be summarized as following: AC-DC conversion where the output DC voltage is lower than grid peak voltage can be achieved with single power processing stage; the input current is continuously conducting, same input current waveform as CCM boost PFC can be achieved; the control structure is simple, high power factor can be achieved with single output voltage feedback loop, the input current loop and multiplier are not necessary; the output diode turns off with zero current, the turn-off loss of the diode is zero and turn on loss of the main switch is reduced compared to other topology with continuous conducting input current; with the coupled inductors, same input current ripple can be achieved with much lower self-inductance of input inductor, which reduces the winding turns number and the winding conduction loss.

Analysis on averaged model of DCM SEPIC reveals the control to output small signal transfer function is still a fourth order system which is same as CCM SEPIC. However, DCM operation separates the LHP complex pole pair and RHP complex zero pair of system, thus the gain peaking caused by LC resonance is well damped. Meanwhile, the system behaves like a first order system in low frequency region. For low bandwidth PFC design, simple PI controller is sufficient to stable the system.

Analysis on coupled inductors reveals the equivalent input inductance can be achieved with smaller self-inductance of coupled input inductor. Coupled inductors with both high coupling coefficient and low coupling coefficient can be used. For high coupling coefficient implementation, to magnify the input self-inductance, the ratio of self-

inductance of input inductor to self-inductance of output inductor should be controlled accurately. When considering the tolerance of core material, winding distribution, the leakage flux and fringing effects, lower coupling coefficient range from 0.3 to 0.6 seems more practical for implementing the coupled inductors for SEPIC. From control point of view, if the equivalent inductances of the coupled inductors are the same as the inductances of separate inductors, the coupled inductors does not change low frequency characteristics of the system, it moves the LHP complex pole and RHP complex zero towards higher frequency region. Under high coupling coefficient condition, the complex pole and zero can be even moved beyond the switching frequency, which makes the system a true first order system.

Through the discussion on system parameters selection, design criteria are derived and verified by simulations. With given input and output specification, operating frequency of DCM SEPIC PFC and the DCM boundary condition limit the available range of inductances. The input current ripple requirement forms the second limitation. Within the available range of inductance, the optimum design point should be the intersection of the two boundaries. For capacitance selection of intermediate capacitor, compared to separate inductor case, implementation with coupled inductors requires larger capacitance.

For control structure of the DCM SEPIC PFC, single output voltage feedback loop with PI controller is sufficient to stable the system. With a PR controller or notch filter inserted into the loop, extra attenuation on double line ripple from the output voltage can be achieved, magnitude of third harmonics of input current can be greatly reduced.

With the designed parameters, both separate inductors and coupled inductors with 0.35 coupling coefficient are implemented. Experimental results demonstrate the major design targets are fulfilled.

6.2 Future Work

Despite all the merits of DCM SEPIC converter, due to the intrinsic circuit configuration, it is less efficient compared with boost PFC. To improve the efficiency of this converter, the future work could be carried out in following direction.

- Investigating converter performance with the interleaved structure or bridgeless structure
- Optimizing the design for coupled inductors
- Modifying the fixed switching frequency modulation scheme, operating the SEPIC converter in Boundary Conduction Mode
- Replacing output diode with MOSFET and extending the conduction of SR to achieve ZVS turn-on of the main switch.

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