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Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application

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The experimental study of the valence band offset (ΔE_v) of a mixed As/Sb type-II staggered gap $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterostructure used as source/channel junction of n-channel tunnel field effect transistor (TFET) grown by molecular beam epitaxy was investigated by x-ray photoelectron spectroscopy (XPS). Cross-sectional transmission electron micrograph shows high crystalline quality at the source/channel heterointerface. XPS results demonstrate a ΔE_v of 0.39 ± 0.05 eV at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. The conduction band offset was calculated to be ~0.49 eV using the band gap values of source and channel materials and the measured valence band offset. An effective tunneling barrier height of 0.21 eV was extracted, suggesting a great promise for designing a metamorphic mixed As/Sb type-II staggered gap TFET device structure for low-power logic applications. © *2013 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4775606]

I. INTRODUCTION

The tunnel field-effect transistor (TFET) is one of the devices that can achieve subthreshold swing (SS) < 60 mV/dec at 300 K based on band-to-band tunneling (BTBT) injection mechanism.[1–3] Currently, it is under intensive study due to the promising applications for sub-0.5 V operation and low standby power.[4] Heterostructures with type-II band alignment at source/channel heterointerface represent a steep p-n junction and have been investigated as TFET performance boosters,[5] such as higher ON current (I_{ON}),[6,7] lower OFF state leakage (I_{OFF}),[8,9] and stepper sub-threshold swing.[8,9] Among these heterostructures, mixed As/Sb based heterojunction enables a wide range of staggered band lineups depending on the alloy compositions in the source and channel materials.[6,7] The band offset of the staggered gap heterojunction at the source/channel heterointerface also defines the effective tunneling barrier height (E_{beff}), which not only determines the ON-state tunneling current, but also sets the blocking barrier of OFF-state leakage.[5,7,10] Therefore, efforts have been devoted to optimize the band offset to boost I_{ON} and suppress I_{OFF};[6,7,10] however, to our knowledge, there is no prior report of experimental demonstration of band offset on mixed As/Sb type-II staggered gap heterojunction n-channel tunnel FET structures. Very recently, we have demonstrated the valence band (VB) offset of the p-channel TFET structure.[11] In this work, we report the experimental study of the valence band offset of a mixed As/Sb type-II staggered gap $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ n-channel tunnel FET structure that shows a great promise for low-power applications.

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II. EXPERIMENTAL

In this study, n-channel TFET structures were grown by solid source molecular beam epitaxy (MBE) and Figure 1 shows the schematic of the layer structure used for this work. The details of the growth process can be found elsewhere.[10] The crystalline quality of the structure was characterized by cross-sectional transmission electron microscopy (TEM). TEM samples were prepared using conventional mechanical thinning procedure followed by Ar^+ ion milling. Reciprocal space maps (RSMs) were obtained using Panalytical X'pert Pro system with Cu $K\alpha$-1 line focused x-ray source to determine the layer compositions of the TFET structure. The detailed x-ray studies on this structure can be found elsewhere.[10] The valence band offset (ΔE_v) of the internally lattice-matched $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterojunction at the source/channel interface was measured by x-ray photoelectron spectroscopy (XPS). The 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ structure was used for the measurement of binding energy information at the heterointerface. To measure the binding energy value of bulk $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers, (i) 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ heterostructure and (ii) 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer were used. The 10 nm p^{++} $GaAs_{0.35}Sb_{0.65}$ layer with heavily carbon (C) doping of $1 \times 10^{20}/cm^3$ in the source region was used to create abruptly doped junction and thus increasing the tunneling probability from source to channel.[12] XPS measurements were performed using a Phi Quantera Scanning XPS Microprobe instrument with a monochromated Al-$K\alpha$ (energy of 1486.6 eV) x-ray source. Oxide layer at sample surfaces was removed by wet chemical etching with citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) at volume ratio of 50:1 for 10 s on $In_{0.7}Ga_{0.3}As$ surface and 1 min on $GaAs_{0.35}Sb_{0.65}$ surface,

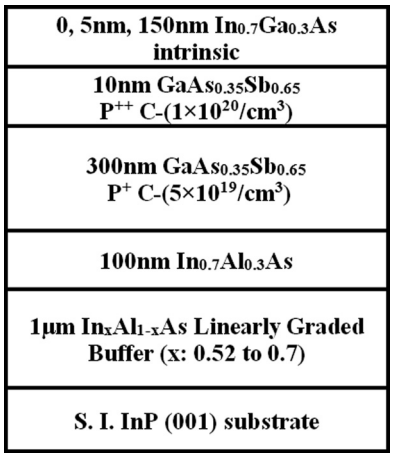

FIG. 1. Schematic diagram of the n-channel TFET layer structure. 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ was used for the measurement of binding energy information at the heterointerface, while 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ and 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer were used to measure the binding energy information of bulk $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively.

respectively, prior to loading into the XPS chamber.[10] Approximately, 2-3 nm was etched from each sample surface based on the premeasured etching rate. The Sb and In core level (CL) binding energy spectra as well as $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ valence band binding energy spectra were collected with pass energy of 26 eV. An exit angle of 45° was used for all measurements. Curve fitting was performed by the CasaXPS 2.3.14 program using a Lorentzian convolution with a Shirley-type background.

III. RESULTS AND DISCUSSION

As fixed charges caused by defects at the source/channel heterointerface would influence the band lineup of the heterojunction,[10] cross-sectional TEM was used to characterize the crystalline quality of the entire TFET structure. Figure 2 shows a cross-sectional TEM micrograph of such TFET structure with 150 nm intrinsic $In_{0.7}Ga_{0.3}As$ channel and 200 nm n^+ $In_{0.7}Ga_{0.3}As$ drain layer. All layers were labeled in this figure and the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface

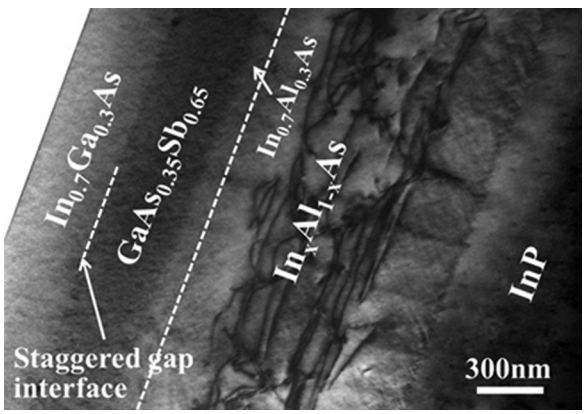

FIG. 2. Cross-sectional TEM micrograph of the entire TFET layer structure with 150 nm intrinsic $In_{0.7}Ga_{0.3}As$ channel and 200 nm n^+ $In_{0.7}Ga_{0.3}As$ drain layer. No threading dislocations were detected in the $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$ layers, indicating high crystalline quality of the active region.

was denoted by an arrow in the micrograph. It can be seen from this figure that the linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch induced defects between the active layer and the InP substrate. Cross-sectional TEM micrograph shows high contrast at the source/channel heterointerface and no threading dislocations were observed in both the $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$ layers and their interface at this magnification, indicating a threading dislocation density in the lattice-matched source/channel layers on the order of or below $10^7\,cm^{-2}$.

XPS measurement can provide binding energy information about the core level and the valence electrons emitted from each layer structure. This allows to determine ΔE_v of $In_{0.7}Ga_{0.3}As$ channel relative to $GaAs_{0.35}Sb_{0.65}$ source by the method as described by Kraut *et al.*[13] Using this approach, XPS spectra were collected from the following three samples: (i) 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$, (ii) 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$, and (iii) 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer. The ΔE_v can be determined using the following equation:

$$\Delta E_v = \left(E^{GaAsSb}_{Sb3d_{5/2}} - E^{GaAsSb}_{VBM}\right) - \left(E^{InGaAs}_{In3d_{5/2}} - E^{InGaAs}_{VBM}\right) - \Delta E_{CL}(i), \quad (1)$$

where $E^{GaAsSb}_{Sb3d_{5/2}}$ and $E^{InGaAs}_{In3d_{5/2}}$ are CL binding energy of $Sb3d_{5/2}$ and $In3d_{5/2}$ from thick $GaAs_{0.35}Sb_{0.65}$ and thick $In_{0.7}Ga_{0.3}As$ film surfaces, respectively; E_{VBM} is the valence band maxima (VBM) of the corresponding samples and it can be determined by linear extrapolation of the leading edge of VB spectra to the base lines;[14] $\Delta E_{CL}(i) = E^{InGaAs/GaAsSb}_{Sb3d_{5/2}}(i) - E^{InGaAs/GaAsSb}_{In3d_{5/2}}(i)$ is the energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ CLs which are measured at the $In_{0.7}Ga_{0.3}As$/$GaAs_{0.35}Sb_{0.65}$ heterointerface. Figures 3(a)–3(f) show the CL and VB spectra from each sample. High resolution XPS measurements with a step-size of 0.025 eV were performed to resolve the spin-orbit splitting of In3d and Sb3d peaks. XPS survey scan in the range of 0-600 eV and high resolution scan around the O1s peak (~530 eV) was taken before each measurement to confirm that no oxygen component was left on each film surface. Figure 3(g) shows the high resolution scan from 526 eV to 540 eV on $GaAs_{0.35}Sb_{0.65}$ surface. No oxygen 1s peak and Sb-O bond (~530 eV)[15] was detected at an exit angle of 45°. Similar scans on other sample surfaces (not shown in Figure 3) also show that no oxygen component was detected at this exit angle. Furthermore, the symmetric CL peaks of $In3d_{5/2}$ and $Sb3d_{5/2}$ also indicate that only single bond, either In-As or Sb-Ga, presents within the sample surfaces studied in this work, suggesting that no In-O or Sb-O bonds formed on the sample surface. All measured binding energy values are summarized in Table I. From the XPS measurements, the values of $\left(E^{GaAsSb}_{Sb3d_{5/2}} - E^{GaAsSb}_{VBM}\right)$, $\left(E^{InGaAs}_{In3d_{5/2}} - E^{InGaAs}_{VBM}\right)$, and $\Delta E_{CL}(i)$ were determined to be 527.70 eV, 443.79 eV, and 83.52 eV, respectively. The valence band offset of $In_{0.7}Ga_{0.3}As$ channel relative to $GaAs_{0.35}Sb_{0.65}$ source is determined to be 0.39 ± 0.05 eV using Eq. (1). The uncertainty value of 0.05 eV is from the

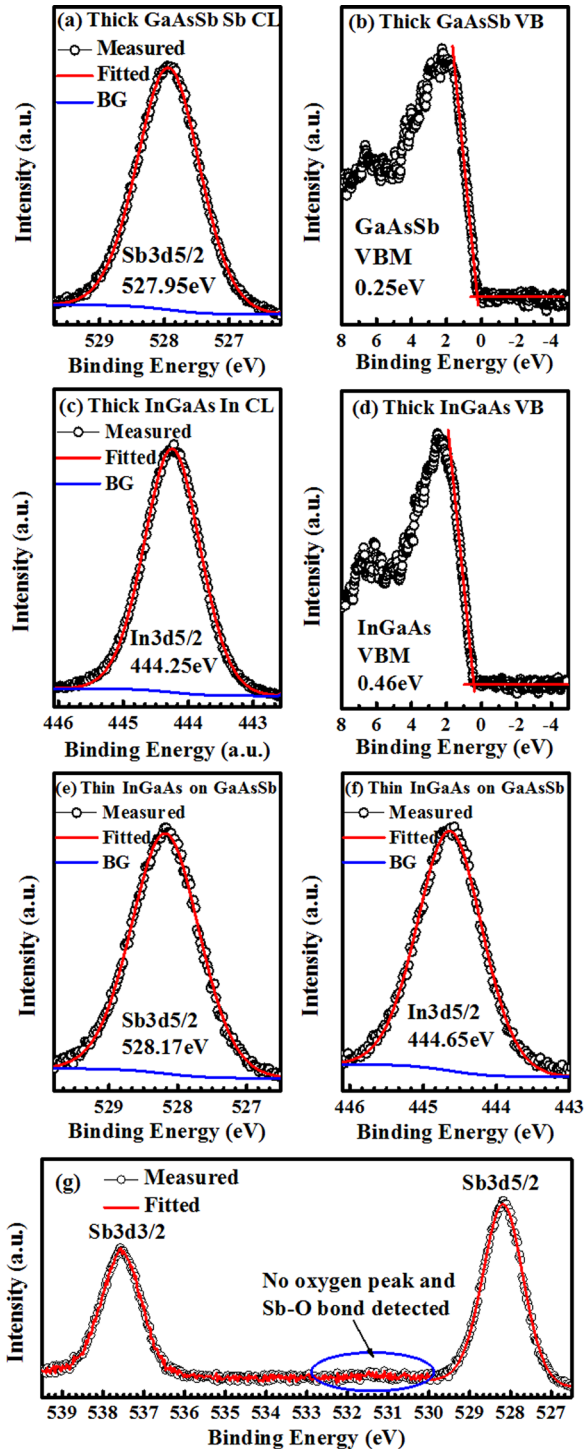

FIG. 3. XPS spectra of (a) $Sb3d_{5/2}$ CL and (b) VB spectra from 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer; (c) $In3d_{5/2}$ CL and (d) VB spectra from 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ sample; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL spectra from 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ sample measured at the interface; (g) high resolution scan in the range of 526-540 eV and no O1s peak or Sb-O bond was detected. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background.

scatter of VB data with respect to the fitting in VBM position.

Shallow CL spectra of In4d and Sb4d were also recorded to confirm the results obtained from In3d and Sb3d spectra. Curve fittings were used to separate the spin-orbit splitting of

TABLE I. Measurement results of XPS CL spectra and VBM positions obtained by linear extrapolation of the leading edge to the extended base line of the valence band spectra.

		Binding energy (eV)	
Sample	States	$3d_{5/2}$	$4d_{5/2}$
310 nm $GaAs_{0.35}Sb_{0.65}$	Sb CL	527.95	32.12
	VBM	0.25	0.25
150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$	In CL	444.25	17.44
	VBM	0.46	0.46
5 nm $In_{0.7}Ga_{0.3}As$/310 nm$GaAs_{0.35}Sb_{0.65}$	Sb CL	528.17	32.01
	In CL	444.65	17.48

In4d and Sb4d peaks as well as to resolve In4d from the combined Ga/In 3d peaks. Figures 4(a)–4(c) show the CL and VB spectra from 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$, 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer

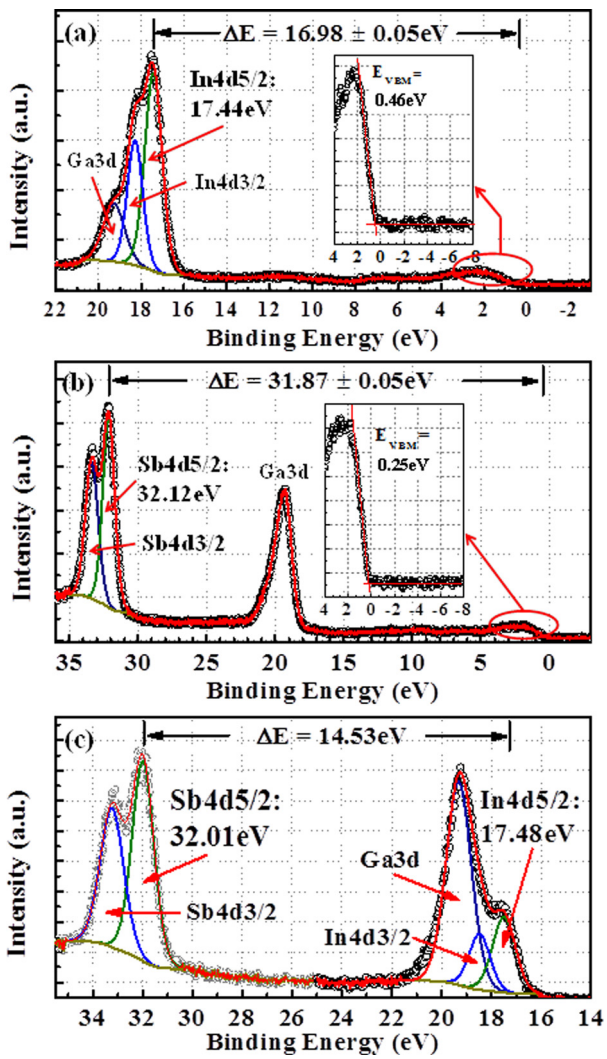

FIG. 4. XPS spectra of (a) Sb4d CL and VB spectra from 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer; (b) In4d CL and VB spectra from 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ sample; (c) Sb4d CL and In4d CL spectra from 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ sample measured at the interface. The insets of (a) and (b) show the magnified VB spectrum of the corresponding sample.

and 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ samples, respectively. An accurate determination of valence band maximum value of each material is the key point of the measurement of valence band offset.[13,16] According to Kraut's method,[13] the VBM was determined by fitting a instrumentally broadened valence band density of states (DOS), for which the VBM is uniquely identified as the energy at which the DOS goes to zero, to the leading edge of the experimental valence band spectrum.[13,16] Based on this method, the insets of Figs. 4(a) and 4(b) show the corresponding magnified VB spectra of $In_{0.7}Ga_{0.3}As$ and $GaAs_{0.35}Sb_{0.65}$, respectively. The intersection of two straight lines, one fits to the linear portion of the valence band leading edge and one fits to the base line of valence band spectrum, determines the VBM value of the corresponding material. All measured binding energy information was also summarized in Table I. The ΔE_v of $In_{0.7}Ga_{0.3}As$ channel relative to $GaAs_{0.35}Sb_{0.65}$ source measured from shallow CL spectra was determined to be 0.36 ± 0.05 eV using Eq. (1). It should be noted that the difference between measured ΔE_v values from 4d CL peaks (0.36 ± 0.05 eV) and 3d CL peaks (0.39 eV ± 0.05 eV) could be caused by the uncertainty during the curve fitting process. However, the ΔE_v value difference within these two measurements (0.03 eV) is in the range of experimental error (0.05 eV) labeled in the paper, indicating good consistency between the results from 4d CL and 3d CL measurements.

The conduction band offset (ΔE_c) can be estimated by the following equation:

$$\Delta E_c = E_g^{GaAsSb} + \Delta E_v - E_g^{InGaAs}, \quad (2)$$

where E_g^{GaAsSb} and E_g^{InGaAs} are the band gaps of $GaAs_{0.35}$ $Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$, respectively. The bandgap of intrinsic $GaAs_{0.35}Sb_{0.65}$ at 300 K was found to be ~0.7 eV by the commonly used empirical law[17] and the experimental measured bandgap of intrinsic $In_{0.7}Ga_{0.3}As$ material at 300 K is 0.6 eV.[18] Using these data, the ΔE_c is calculated to be ~0.49 eV. It should be noted that, in reality, the value of ΔE_c could be smaller than the evaluated one due to the band gap narrowing effect caused by the heavily C doping in the $GaAs_{0.35}Sb_{0.65}$ layer.[10]

Figure 5 shows the schematic band alignment diagram of the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterojunction based on the present results above. A type-II staggered band lineup is formed at the source/channel interface of the n-channel TFET structure. The effective tunneling barrier height ($E_{beff} = E_g^{InGaAs} - \Delta E_v$) is determined to be 0.21 ± 0.05 eV. This effective tunneling barrier height plays a key role on the performance of TFET devices such as, I_{ON} and I_{OFF}.[7] It has been reported that reducing E_{beff} from 0.5 eV to 0.25 eV results in at least 200% improvement of I_{ON} in mixed As/Sb heterojunction TFETs due to the increase of tunneling transmission coefficient.[6,7] On the other hand, the reduced E_{beff} also improves the drain induced barrier thinning (DIBT) due to the fact that the inter band generation process occurs closer to the source/channel junction, thus improving electrostatics of devices.[11] Nevertheless, if $E_{beff} < 0$, a broken bandgap lineup will occur at the source/channel heterointerface. Although, further improvement is expected on I_{ON} and SS by decreasing E_{beff},[5] the I_{OFF} will increase simultaneously and thus additional gate bias is required to turn off this tunneling mechanism.[19] As a result, the E_{beff} should be well modulated to guarantee both the ON-state and OFF-state performance of a TFET device. An I_{ON}/I_{OFF} ratio of greater than 10^4 with high $I_{ON} > 100\,\mu A/\mu m$ has been reported experimentally using the same TFET structure as studied in this paper,[7] indicating that a 0.21 eV effective barrier at $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface can provide promising performance for n-channel TFET device application.

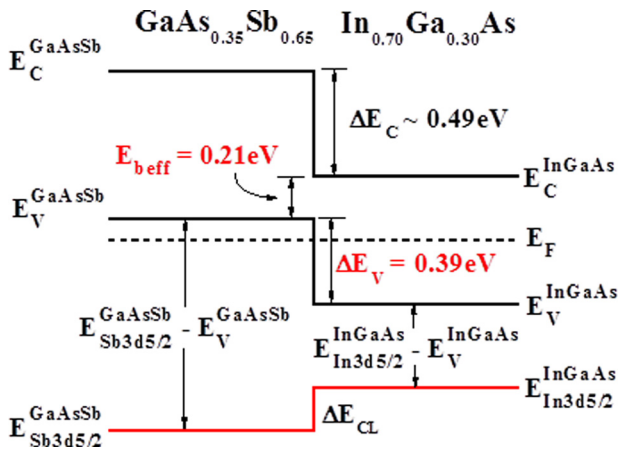

FIG. 5. Schematic of the energy-band diagram of $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface in an n-channel TFET structure. A type-II staggered band alignment with an effective tunneling barrier height of 0.21 eV was measured at the heterointerface.

IV. CONCLUSION

In summary, the experimental study of the valence band offset of an n-channel $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterostructure tunnel FET structure grown by MBE was investigated using XPS. Cross-sectional TEM micrograph indicated threading dislocation free interface at the source/channel region. XPS results showed the valence band offset of 0.39 ± 0.05 eV at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ source/channel heterointerface. The conduction band offset is calculated to be ~0.49 eV using bandgaps of $GaAs_{0.35}Sb_{0.65}$ and $In_{0.7}Ga_{0.3}As$, and the effective tunneling barrier height was found to be 0.21 eV. These results and the self-consistency among device, material, and growth properties indicate that mixed As/Sb material systems provide access to various combinations of band gaps and band offset energies while maintaining high material quality to design metamorphic staggered gap TFET devices for ultra-low power logic applications.

ACKNOWLEDGMENTS

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