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The compositional dependence of effective tunneling barrier height (E_{beff}) and defect assisted band alignment transition from staggered gap to broken gap in GaAsSb/InGaAs n-channel tunnel field effect transistor (TFET) structures were demonstrated by x-ray photoelectron spectroscopy (XPS). High-resolution x-ray diffraction measurements revealed that the active layers are internally lattice matched. The evolution of defect properties was evaluated using cross-sectional transmission electron microscopy. The defect density at the source/channel heterointerface was controlled by changing the interface properties during growth. By increasing indium (In) and antimony (Sb) alloy compositions from 65% to 70% in $In_xGa_{1-x}As$ and 60% to 65% in $GaAs_{1-y}Sb_y$ layers, the E_{beff} was reduced from 0.30 eV to 0.21 eV, respectively, with the low defect density at the source/channel heterointerface. The transfer characteristics of the fabricated TFET device with an E_{beff} of 0.21 eV show 2× improvement in ON-state current compared to the device with E_{beff} of 0.30 eV. On contrary, the value of E_{beff} was decreased from 0.21 eV to −0.03 eV due to the presence of high defect density at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. As a result, the band alignment was converted from staggered gap to broken gap, which leads to 4 orders of magnitude increase in OFF-state leakage current. Therefore, a high quality source/channel interface with a properly selected E_{beff} and well maintained low defect density is necessary to obtain both high ON-state current and low OFF-state leakage in a mixed As/Sb TFET structure for high-performance and lower-power logic applications. © *2012 American Institute of Physics*. [http://dx.doi.org/10.1063/1.4764880]

I. INTRODUCTION

As aggressive scaling of silicon (Si) metal-oxide semiconductor field-effect transistors (MOSFETs), the static power dissipation has become a big problem in current microprocessors. The static power dissipation has a strong dependence on the sub-threshold swing (SS), which is defined as $SS = (d \log I_{DS}/d V_{GS})^{-1}$, where I_{DS} is the drain-to-source current under an applied gate-to-source voltage, V_{GS}. As the SS of a MOSFET is governed by the transport mechanism of thermionic-emission over a thermal barrier and limited to 60 mV/dec at 300 K, further scaling down of Si MOSFET supply voltage becomes difficult without significantly increasing the OFF-state current (I_{OFF}). In order to control the rapidly increasing power dissipation of a conventional MOSFET, the tunnel field-effect transistor (TFET)[1–12] has been proposed as an alternative switching device in recent years. The TFET device is a reverse biased gated p^+-i-n^+ diode, which exploits the gate-controlled band-to-band tunneling (BTBT) mechanism to overcome the fundamental kT/q thermodynamic limit of SS in a conventional MOSFET.[2,3] Great efforts have been devoted to boost the performance of TFETs, such as reducing SS,[4–6] improving ON-state current (I_{ON}),[7,8] and lowering I_{OFF}.[9,10] Recently, steep SS of <60 mV/dec was demonstrated in a III-V TFET.[6] Besides, high I_{ON} of 135 μA/μm with high I_{ON}/I_{OFF} ratio of 2.7×10^4 at $V_{DS} = 0.5$ V and V_{ON}-$V_{OFF} = 1.5$ V (Ref. 9) was also reported within TFET based on III-V materials. This brought to the potential application of TFETs as a promising replacement or complement of Si MOSFETs for low standby power circuits.

A further strategy to improve I_{ON} and reduce SS is to use low-bandgap materials as well as band engineering to increase BTBT probability.[11] For this purpose, group III-V materials can provide small tunneling mass and allow tailored-made band alignments.[7,12] Among them, mixed As/Sb based heterostructure namely, $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ allows a wide range of bandgaps and band alignments depending on the alloy compositions in $GaAs_{1-y}As_y$ source and $In_xGa_{1-x}As$ channel layers.[9,10,13,14] The band alignment at the source/channel interface determines the effective tunneling barrier, E_{beff}, which is defined as the energy difference between the conduction band minimum of the channel and the valence band maximum of the source. This E_{beff} plays a significant role on the performance of a TFET device, which not only determines the ON-state tunneling rate but also sets the blocking barrier for the OFF-state leakage.[9,10,12] Thus, proper alloy compositions of mixed As/Sb source and channel material system should be selected in order to obtain an appropriate E_{beff} to increase I_{ON} without sacrificing I_{OFF}. However, engineering an abrupt heterointerface of mixed anion $GaAs_{1-y}Sb_y$

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and mixed cation $In_xGa_{1-x}As$ is a significant growth challenge due to different surface sticking coefficient of arsenic (As) and antimony (Sb) at the specific growth temperature.[9,10] Furthermore, improper change of group-V fluxes at the source and channel interface will introduce intermixing between As and Sb that leads to uncontrolled layer composition at this heterointerface, which in turn will produce high dislocation density in this region.[8,10] These dislocations will introduce fixed charges at the source/channel interface[15] and thus, it will affect the band alignment as well as the value of E_{beff}.[10] Very recently, we have demonstrated by simulation that the band alignment is indeed converted from staggered gap to broken gap with a fixed positive charge density of $\sim 6 \times 10^{12}/cm^2$ caused by high dislocation density at the source/channel $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface.[10] This resulted in four orders of higher leakage current experimentally measured from this fabricated TFET structure.[9,10] Therefore, it prompted us to verify the experimental proof of defect induced band alignment conversion from staggered to broken gap lineup in a mixed As/Sb tunnel FET heterostructure.

In this work, the compositional dependence and defect assisted transition of band alignment in $GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ n-channel tunnel FET structures were experimentally investigated by x-ray photoelectron spectroscopy (XPS). The experimental results revealed that the E_{beff} was reduced by increasing indium (In) and Sb compositions in InGaAs and GaAsSb layers, respectively. Furthermore, the band alignment was converted from staggered gap to broken gap due to high defect density at the interface for fixed In and Sb compositions in a TFET structure. Therefore, controlling defect density is indispensable in growing mixed As/Sb tunnel FET heterostructures in order to achieve the desired effective tunneling barrier and the proper band alignment for a high-performance TFET structure in low-power logic applications.

II. EXPERIMENTAL

$GaAs_{1-y}Sb_y/In_xGa_{1-x}As$ n-channel TFET structures were grown by solid source molecular beam epitaxy (MBE) on semi-insulating (100) InP substrates and the schematic layer structures are shown in Fig. 1(a). Different Sb and In compositions were selected for structure A ($GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$) and B ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) to determine the band offset at source/channel interface. The layer structure C ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$) is essentially the same as structure B except that much higher defect density was found at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface and within the $In_{0.7}Ga_{0.3}As$ layer due to different terminated atoms at the heterointerface,[10] which is confirmed by x-ray diffraction (XRD) and cross-sectional transmission electron microscopy (TEM) analysis. Besides, samples with different InGaAs thicknesses (as shown in Fig. 1(b)) were also prepared from each structure for band offset measurements. Table I summarized the composition and defect density difference of these three TFET structures. The strain relaxation and defect properties of these TFET structures were characterized by high-resolution XRD and cross-sectional TEM. X-ray reciprocal space maps (RSMs) were obtained using

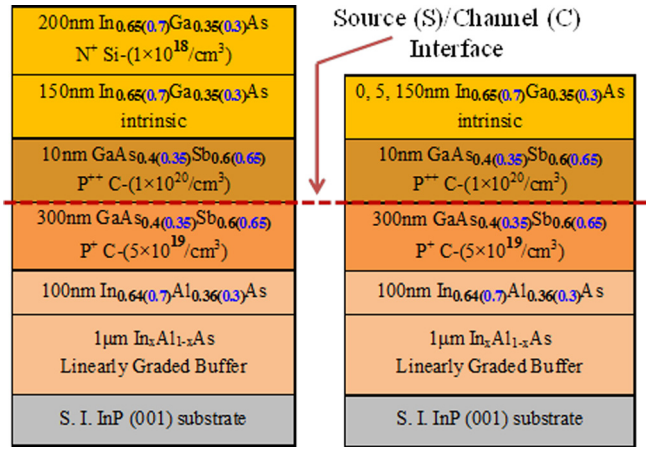

FIG. 1. (a) Schematic diagram of n-channel TFET layer structures. (b) Samples with different InGaAs thickness from each structure for band offset measurements. 5 nm InGaAs/310 nm GaAsSb was used for the measurement of binding energy at the heterointerface, while 150 nm InGaAs/310 nm GaAsSb and 310 nm GaAsSb without the top InGaAs layer were used to measure the binding energy of bulk InGaAs and GaAsSb, respectively. The arrow denotes the source/channel interface.

Panalytical X'pert Pro system with Cu Kα-1 as an x-ray source. TEM samples were prepared using conventional mechanical thinning procedure followed by Ar^+ ion milling. TFET devices were fabricated from these structures using self-aligned gate process[8] to validate the difference in transfer (I_{DS}-V_{GS}) characteristics.

The valence band offset (VBO) of GaAsSb/InGaAs heterojunction at source/channel interface was determined using XPS by measuring the binding energy from core levels (CLs) of $Sb3d_{5/2}/In3d_{5/2}$ and valence band maxima (VBM) of GaAsSb/InGaAs, respectively. As shown in Fig. 1(b), XPS spectra were collected from three samples of each structure: (1) 5 nm InGaAs/310 nm GaAsSb was used to measure CL binding energy of In and Sb at the interface; (2) 150 nm InGaAs/310 nm GaAsSb was used to measure the CL binding energy of In and VBM of InGaAs; (3) 310 nm GaAsSb without the top InGaAs layer was used to measure the CL binding energy of Sb and VBM of GaAsSb. XPS measurements were performed on a Phi Quantera Scanning XPS Microprobe instrument using a monochromatic Al Kα (1486.6 eV) x-ray source. $In3d_{5/2}$ CL, $Sb3d_{5/2}$ CL, InGaAs valence (VB), and GaAsSb VB spectra were recorded using pass energy of 26 eV. An exit angle of 45° was used in all measurements. In order to improve accuracy of the measured binding energy information, high resolution measurements with a step-size of 0.025 eV was performed to resolve the

TABLE I. Summary of composition and defect density difference of the TFET structures studied in the work.

Structure details	Composition		Defect density at source/channel interface and in InGaAs layer
	Source	Channel/ Drain	
A	$GaAs_{0.4}Sb_{0.6}$	$In_{0.65}Ga_{0.35}As$	Low
B	$GaAs_{0.35}Sb_{0.65}$	$In_{0.7}Ga_{0.3}As$	Low
C	$GaAs_{0.35}Sb_{0.65}$	$In_{0.7}Ga_{0.3}As$	High

spin-obit splitting of In and Sb 3d peaks. Oxide layers on all sample surfaces were carefully removed by wet chemical etching using citric acid/hydrogen peroxide ($C_6H_8O_7$:H_2O_2) at volume ratio of 50:1 for 10 s on InGaAs surface and 1 min on GaAsSb surface, respectively, before loading into the XPS chamber. About 2-3 nm was etched from each sample surface according to the premeasured etching rate.[10] Curve fitting was done by the CasaXPS 2.3.14 using a Lorentzian convolution with a Shirley-type background.

Once the binding energy information from each sample surface was collected, the VBO can be determined by Kraut's[16] method

$$\Delta E_V = (E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}) - (E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}) - \Delta E_{CL}(i), \quad (1)$$

where $E_{Sb\ 3d_{5/2}}^{GaAsSb}$ and $E_{In\ 3d_{5/2}}^{InGaAs}$ are CL binding energies of $Sb3d_{5/2}$ and $In3d_{5/2}$; E_{VBM} is the VBM of the corresponding samples. E_{VBM} was determined by linearly fitting the leading edge of the VB spectra to the base line.[17] $E_{In\ 3d_{5/2}}^{InGaAs} - E_{VBM}^{InGaAs}$ and $E_{Sb\ 3d_{5/2}}^{GaAsSb} - E_{VBM}^{GaAsSb}$ were measured from 150 nm InGaAs/310 nm GaAsSb and 310 nm GaAsSb without the top InGaAs layer, respectively. $\Delta E_{CL}(i) = E_{Sb\ 3d_{5/2}}^{GaAsSb}(i) - E_{In\ 3d_{5/2}}^{InGaAs}(i)$ is the CL binding energy difference of $Sb3d_{5/2}$ and $In3d_{5/2}$ measured at the heterointerface from 5 nm InGaAs/310 nm GaAsSb sample of each structure. The conduction band offset (CBO) can be estimated by[17]

$$\Delta E_C = E_g^{GaAsSb} + \Delta E_V - E_g^{InGaAs}, \quad (2)$$

where E_g^{GaAsSb} and E_g^{InGaAs} are the band gaps of GaAsSb and InGaAs, respectively. The effective tunneling barrier of the TFET is described as

$$E_{beff} = E_g^{InGaAs} - \Delta E_V, \quad (3)$$

where ΔE_V is the above measured valence band offset.

III. RESULTS AND DISCUSSION

A. Strain relaxation properties

The relaxation state and residual strain of epilayers were obtained from RSMs. Wet chemical etching was performed on all structures to certificate each epilayer with its corresponding reciprocal lattice point (RLP).[10] Figures 2(a)–2(c) show symmetric (004) RSMs of these TFET structures with the projection of x-ray beam along $[1\bar{1}0]$ direction. All layers with the measured compositions were labeled to the corresponding RLPs. As shown in Figs. 2(a) and 2(b), four distinct RLP maxima were found in RSMs of structures A and B, corresponding to (1) the InP substrate, (2) GaAsSb source layer, (3) InGaAs channel/drain layer, and (4) the 100 nm InAlAs uppermost layer of the linearly graded $In_xAl_{1-x}As$ buffer. Detailed strain relaxation analysis based on the symmetric (004) and asymmetric (115) RSMs (not shown in Fig. 2) shows similar strain relaxation states of structures A and B. Only ~10% strain relaxation in the InGaAs and GaAsSb active layers with respective to the InAlAs "virtual substrate" was derived from structures A and B,[10] suggesting the pseudomorphic nature of these two layers. Different from the RSMs of structures A and B, one can find from

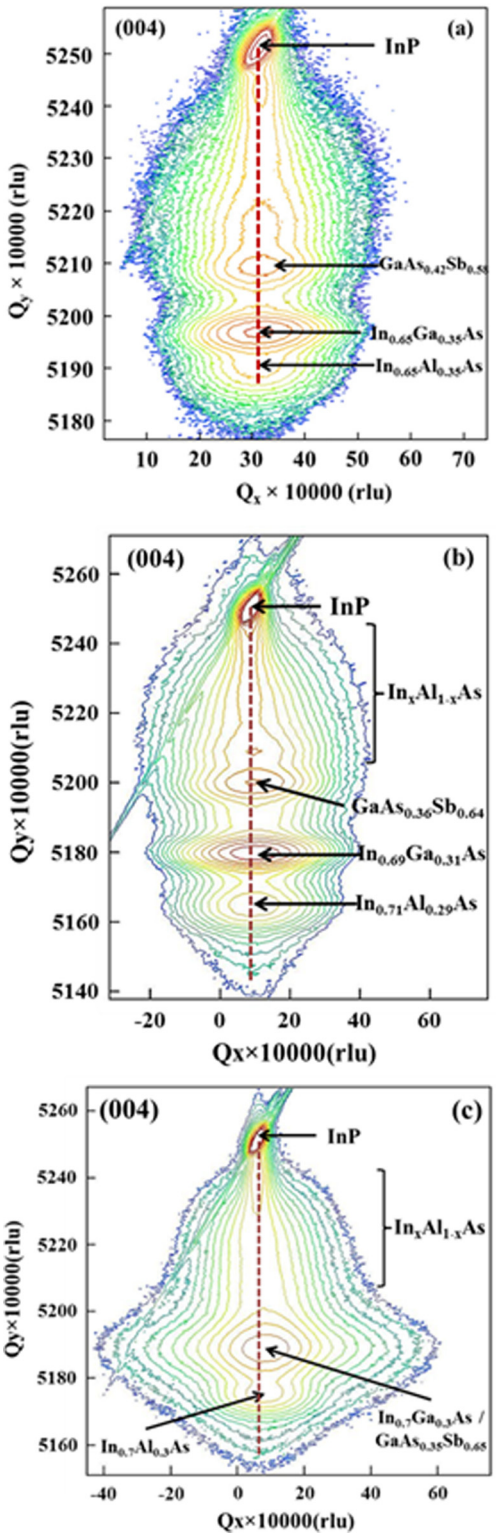

FIG. 2. Symmetric (004) reciprocal space maps (RSMs) of n-channel TFET structures with different compositions in active region and different strain relaxation states in InGaAs layer: (a) $GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$ with low strain relaxation, (b) $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ with low strain relaxation, and (c) $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ with high strain relaxation. RSM of structure C shows combined RLP of $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ layers and large elongation of this RLP along the x-axis, indicating high dislocation density within this region.

Fig. 2(c) that the contour of $In_{0.7}Ga_{0.3}As$ channel/drain layer was merged with $GaAs_{0.35}Sb_{0.65}$ source layer in RSM of structure C. Calculation shows higher percentage of strain relaxation of 94% with respect to InP substrate from these two layers than that in structures A and B, which is 75% and 72% in structure A and 75% and 80% in structure B, respectively.[10] Large elongation of the corresponding RLP along the x-axis of RSM indicates high degree of dislocations. In fact, the elongation of this RLP is highly enfeebled after removing the top $In_{0.7}Ga_{0.3}As$ layer from structure C, and the relaxation value of the $GaAs_{0.35}Sb_{0.65}$ layer of structure C was re-calculated and it was found to be ~80% after etching the top $In_{0.7}Ga_{0.3}As$ layer, which is almost identical with that in structure A or B.[10] The above results reveal that the $GaAs_{0.35}Sb_{0.65}$ layer is not as defective as the $In_{0.7}Ga_{0.3}As$ layer in structure C, and the higher dislocation density is only confined within the top $In_{0.7}Ga_{0.3}As$ layer.

B. Dislocation and defects

The structural properties of these TFET structures were further characterized by cross-sectional TEM. Figures 3(a)–3(c) show the cross-sectional TEM micrographs of structure A ($GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$), B ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$)m and C ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$), respectively. All layers were labeled in these figures, and the GaAsSb/InGaAs heterointerface was denoted by an arrow. One can find from these figures that the linearly graded $In_xAl_{1-x}As$ buffer layer effectively accommodates the lattice mismatch induced defects between active layers (GaAsSb/InGaAs) and the InP substrate in all three structures. It can be seen from Figs. 3(a) and 3(b) that no threading dislocations were observed in structures A and B in both the GaAsSb and InGaAs layers and their interface at this magnification, indicating a threading dislocation density on the order of or below $10^7\,cm^{-2}$ in this region. In contrary, high dislocation density was detected in the $In_{0.7}Ga_{0.3}As$ layer in structure C, which generated from the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface and went all the way through the $In_{0.7}Ga_{0.3}As$ layer. The dislocation density within the $In_{0.7}Ga_{0.3}As$ channel/drain layers of structure C was too high to be quantified. The high dislocation density of $In_{0.7}Ga_{0.3}As$ layer of structure C is in agreement with the XRD analysis above. Besides, no threading dislocations were found in the $GaAs_{0.35}Sb_{0.65}$ layer of structure C, which confirms that the high dislocation density is indeed confined in the top $In_{0.7}Ga_{0.3}As$ layer and $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ interface.

C. Band offset properties

XPS measurements were performed on all of these structures to determine the band offset values. Before each CL and VB measurement, XPS survey scan in the range of 0-600 eV and high resolution scan around the O1s peak (~530 eV) was performed to confirm that no oxygen component was left on each film surface. Figure 4(a) shows the high resolution scan of Sb3d CL from 525 eV to 542 eV on 310 nm $GaAs_{0.4}Sb_{0.6}$ surface of structure A. No oxygen 1 s peak or Sb-O bond (~530 eV (Ref. 18) for $Sb3d_{5/2}$ bonds with oxygen and ~540 eV (Ref. 19) for $Sb3d_{3/2}$ bonds with oxygen) was detected at an exit angle of 45°. Similar scans were also taken on 150 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ and 5 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ surfaces of structure A. Figures 4(b) and 4(c) show the XPS spectra of In3d CL taken from 150 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ and 5 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$, respectively. Both of these two figures exhibited no In-O bond (~444.90 eV (Ref. 20)). The inset of Fig. 4(b) displays the XPS measurement is in the range of 527–534 eV, and no O1s peak appears in this figure, indicating the absence of oxygen component on the sample surface. The inset of Fig. 4(c) shows the XPS spectra of Sb3d taken from the surface of 5 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$. It also shows that no O1s peak appears in this figure, confirming that the oxygen layer was successfully removed from the sample surface prior to each measurement. Furthermore, the symmetric CL peaks of $In3d_{5/2}$ and $Sb3d_{5/2}$ as shown in Fig. 5 also indicate that only single bond, either In-As or

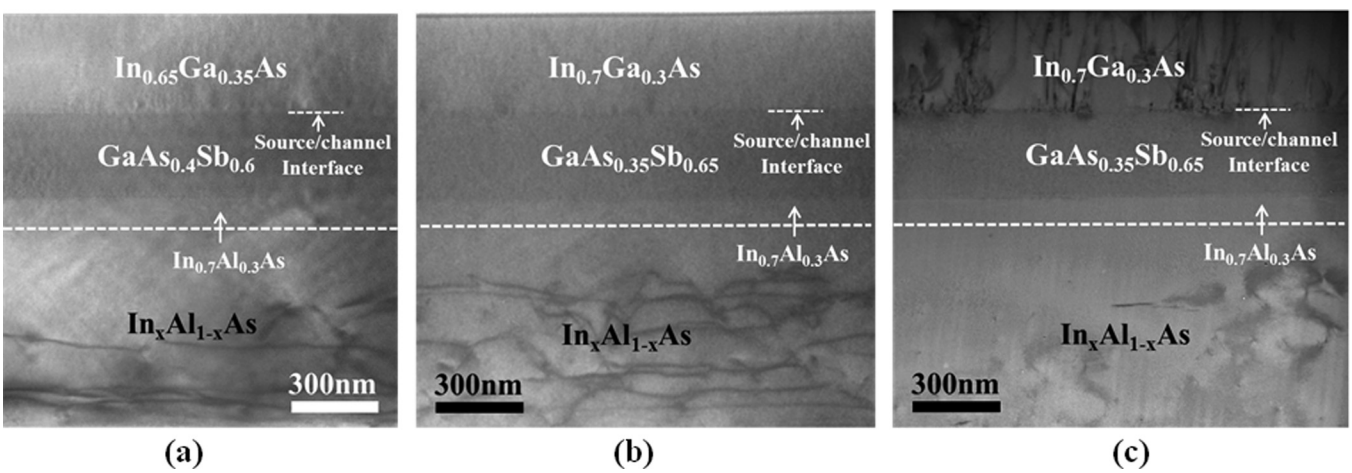

FIG. 3. Cross-sectional TEM micrographs of (a) structure A ($GaAs_{0.4}Sb_{0.6}/In_{0.65}Ga_{0.35}As$), (b) structure B ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$), and (c) structure C ($GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$). No threading dislocations are observed in the InGaAs and GaAsSb layers of the structure A and B, indicating a threading dislocation density on the order of or below $10^7\,cm^{-2}$ in this region. High dislocation density was detected at the $In_{0.7}Ga_{0.3}As/GaAs_{0.35}Sb_{0.65}$ interface and in the $In_{0.7}Ga_{0.3}As$ layer of structure C. Only the active layers and some part of the graded buffer were shown.

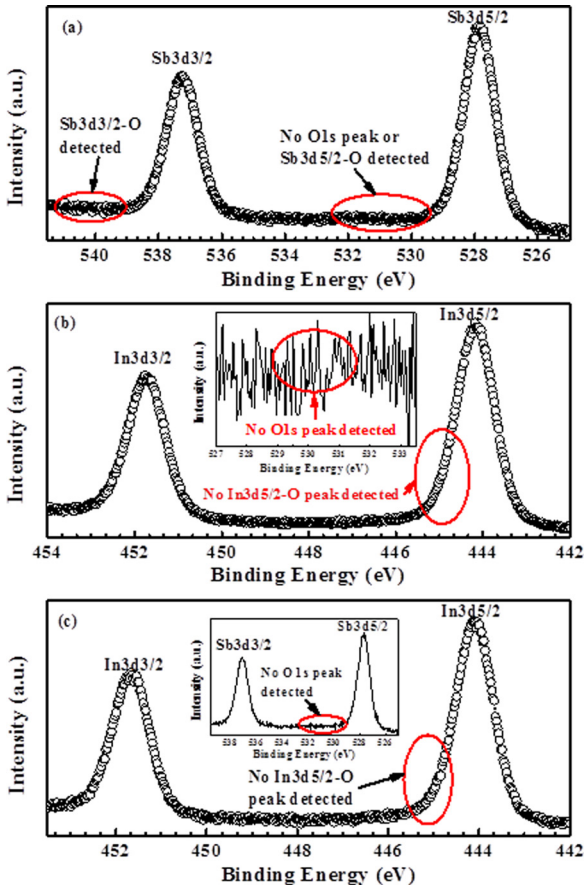

FIG. 4. (a) XPS spectra of Sb3d CL taken from 310 nm $GaAs_{0.4}Sb_{0.6}$ without the top $In_{0.65}Ga_{0.35}As$ layer of structure A. No O1s peak or Sb-O bond was detected. (b) XPS spectra of In3d CL taken from 150 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ of structure A. No In-O bond was detected. The inset shows the XPS spectra in the range of 527-534 eV taken from the same surface. No O1s peak was appear in the figure. (c) XPS spectra of In3d CL taken from 5 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ of structure A. No In-O bond was detected. The inset shows the XPS spectra in the range of 527-539 eV taken from the same surface. No O1s peak was detected.

Sb-Ga, presents within the samples studied in this work, suggesting that no In-O and Sb-O bonds formed on the sample surfaces.

Figures 5(a)–5(f) show the CL and VB spectra from each sample of structure A. The CL energy position was defined to be the center of the peak width at half of the peak height (i.e., full width at half maximum). The CL to VBM binding energy difference for $GaAs_{0.4}Sb_{0.6}$ and $In_{0.65}Ga_{0.35}As$ of structure A was summarized in Table II. The results show that the values of $(E^{GaAsSb}_{Sb\ 3d_{5/2}} - E^{GaAsSb}_{VBM})$ and $(E^{InGaAs}_{In\ 3d_{5/2}} - E^{InGaAs}_{VBM})$ are 527.66 eV and 443.71 eV, respectively. The binding energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ at the heterointerface $(\Delta E_{CL}(i))$ was found to be 83.60 eV. Using these results, the VBO of $In_{0.65}Ga_{0.35}As$ channel relative to $GaAs_{0.4}Sb_{0.6}$ source is determined to be 0.35 ± 0.05 eV. The uncertainly value of 0.05 eV is from the scatter of VB curve during the fitting of VBM positions. Similar pre-cleaning and binding energy measurements were also executed on structures B and C. No oxygen component was detected from the surfaces of these two structures. The detailed measurements, measured CL and VB XPS spectra of structure B were reported elsewhere.[13] The CL and VB

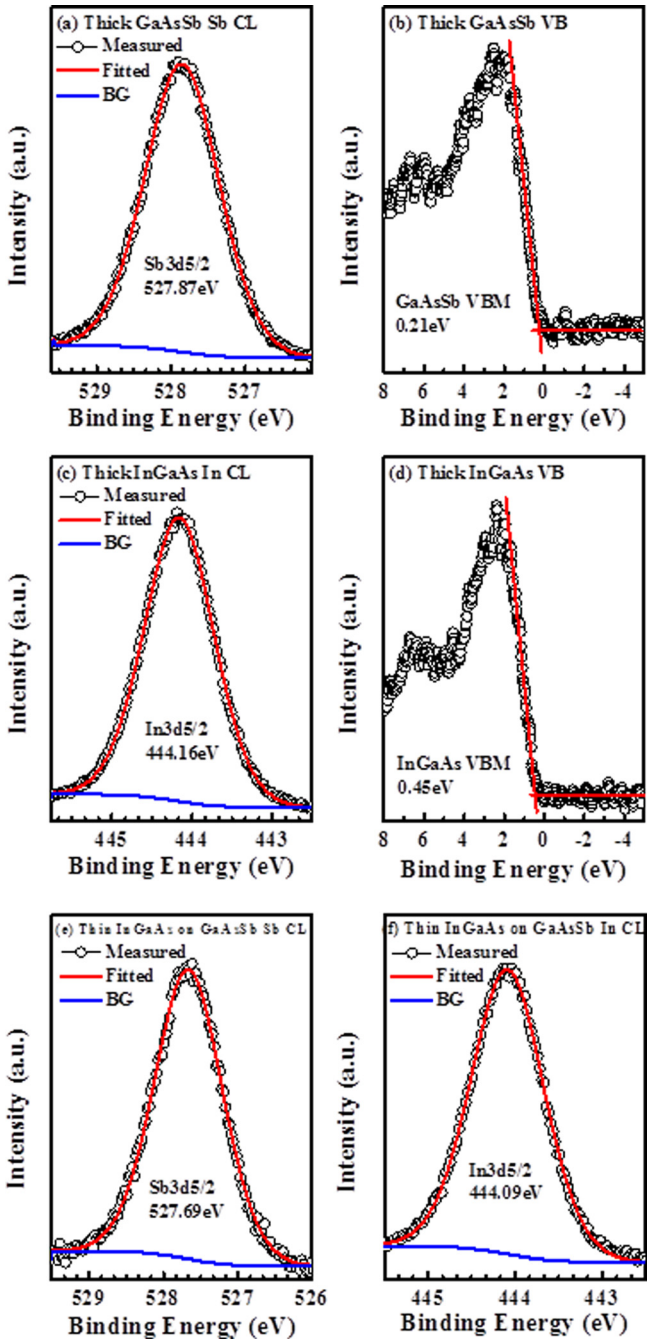

FIG. 5. XPS spectra of (a) $Sb3d_{5/2}$ CL and (b) $GaAs_{0.4}Sb_{0.6}$ VB from 310 nm $GaAs_{0.4}Sb_{0.6}$ without the top $In_{0.65}Ga_{0.35}As$ layer of structure A; (c) $In3d_{5/2}$ CL and (d) $In_{0.65}Ga_{0.35}As$ VB from 150 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ of structure A; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL from 5 nm $In_{0.65}Ga_{0.35}As$/310 nm $GaAs_{0.4}Sb_{0.6}$ structure measured at the heterointerface of structure A. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. VBM were determined by linearly fitting the leading edge of the VB spectra to the base line.

spectra from each sample of structure C were shown in Figs. 6(a)–6(f). The measured values of $(E^{GaAsSb}_{Sb\ 3d_{5/2}} - E^{GaAsSb}_{VBM})$, $(E^{InGaAs}_{In\ 3d_{5/2}} - E^{InGaAs}_{VBM})$ and $\Delta E_{CL}(i)$ from structures B and C are also summarized in Table II. The calculated VBO was 0.39 eV for structure B and 0.63 eV for structure C.

The CBO of all three structures were estimated from Eq. (2) using bandgaps of InGaAs and GaAsSb and the measured values of VBO. The bandgap of intrinsic $GaAs_{0.4}Sb_{0.6}$ and $GaAs_{0.35}Sb_{0.65}$ at 300 K was found to be ~0.72 eV and

TABLE II. Summary of core level to valence-band maxima binding energy difference (eV) for GaAsSb and InGaAs, and the binding energy difference between $Sb3d_{5/2}$ and $In3d_{5/2}$ at the heterointerface ($\Delta E_{CL}(i)$) from the three structures. The calculated valence band offset (ΔE_V), conduction band offset (ΔE_C), and effective tunneling barrier (E_{beff}) are also listed in the table.

	Structure A	Structure B	Structure C
$E^{GaAsSb}_{Sb\ 3d_{5/2}} - E^{GaAsSb}_{VBM}$ (eV)	527.66	527.70	527.59
$E^{InGaAs}_{In\ 3d_{5/2}} - E^{InGaAs}_{VBM}$ (eV)	443.71	443.79	443.74
$\Delta E_{CL}(i)$ (eV)	83.60	83.52	83.22
ΔE_V (eV)	0.35	0.39	0.63
ΔE_C (eV)	0.42	0.49	0.73
E_{beff} (eV)	0.30	0.21	−0.03

0.70 eV, respectively, by the commonly used empirical law.[21] The experimental measured bandgap of intrinsic $In_{0.7}Ga_{0.3}As$ is 0.60 eV (Ref. 22) and the bandgap of intrinsic $In_{0.65}Ga_{0.35}As$ is ~0.65 eV by empirical model.[23] The CBO was calculated to be ~0.42 eV for structure A, ~0.49 eV for structure B, and ~0.73 eV for structure C. All calculated VBO are summarized in Table II. It should be noted that the VBO values should be smaller in actual situation than the estimated ones due to the band gap narrowing effect in the GaAsSb material caused by heavily carbon doping. Finally, the effective tunneling barrier height was carried out using Eq. (3). Here, the E_{beff} determines the type of band alignment in the GaAsSb/InGaAs heterostructure, i.e., the band alignment is staggered lineup if $E_{beff} > 0$ but broken lineup if $E_{beff} < 0$. Positive effective tunneling barrier height of 0.30 eV and 0.21 eV were determined on structure A (In = 0.65 and Sb = 0.6) and B (In = 0.7 and Sb = 0.65), respectively, indicating a staggered band alignment.

Figures 7(a) and 7(b) show the schematic band alignments of these three structures based on the band gap energy values determined above and the experimental results of VBO measured by XPS. From these figures, one can find that the measured VBO of intrinsic InGaAs channel layer with respect to GaAsSb source layer is 0.35 eV and 0.39 eV for In (Sb) compositions of 0.65 (0.60) and 0.70 (0.65), respectively. The higher value of VBO for In compositions of 0.7 compared to 0.6 is expected due to the lower bandgap of $In_{0.7}Ga_{0.3}As$. Wang *et al.*[24] systematically calculated the valence band offsets between most of the III-V semiconductor alloys by a self-consistent band structure method. Using these calculations, the VBO of intrinsic $In_{0.65}Ga_{0.35}As$ relative to intrinsic $GaAs_{0.4}Sb_{0.6}$ as well as intrinsic $In_{0.7}Ga_{0.3}As$ with respect to intrinsic $GaAs_{0.35}Sb_{0.65}$ was determined to be 0.32 eV and 0.34 eV, respectively. The measured VBO values are in close agreement with the calculated ones. The difference in VBO values between experimental and calculation may be due to the doping induced band gap narrowing effect in GaAsSb layer.

By comparing the effective tunneling barrier height for structures A and B, it can be seen that by increasing In alloy composition from 65% to 70% in InGaAs layer and simultaneously increasing Sb alloy composition from 60% to 65% in GaAsSb layer to keep internally lattice matching with respect to each other, the E_{beff} reduces from 0.30 eV to 0.21 eV. Thus, one can modulate the values of E_{beff} at the mixed As/Sb based lattice matched heterojunctions (GaAsSb/InGaAs) by carefully controlling both Sb and In compositions. As a result, the mixed As/Sb based material system is a preferred choice for TFET application as it provides a wide range of compositionally controlled E_{beff}.

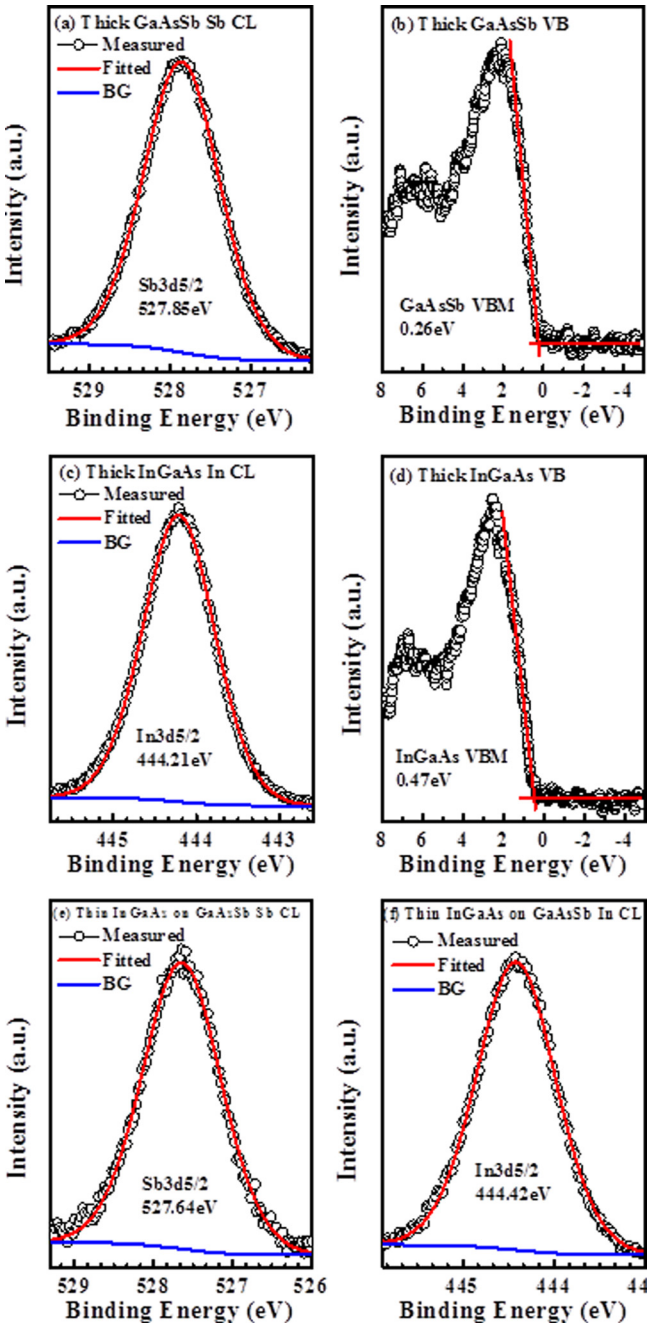

FIG. 6. XPS spectra of (a) $Sb3d_{5/2}$ CL and (b) $GaAs_{0.35}Sb_{0.65}$ VB from 310 nm $GaAs_{0.35}Sb_{0.65}$ without the top $In_{0.7}Ga_{0.3}As$ layer of structure C; (c) $In3d_{5/2}$ CL and (d) $In_{0.7}Ga_{0.3}As$ VB from 150 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ of structure C; (e) $Sb3d_{5/2}$ CL and (f) $In3d_{5/2}$ CL from 5 nm $In_{0.7}Ga_{0.3}As$/310 nm $GaAs_{0.35}Sb_{0.65}$ structure measured at the heterointerface of structure C. CL spectra curves were fitted using a Lorentzian convolution with a Shirley-type background. VBM were determined by linearly fitting the leading edge of the VB spectra to the base line.

The value of E_{beff} can be drastically reduced at the GaAsSb/InGaAs heterojunction if the defects level is high. Figure 7(c) shows the schematic band alignment of structure

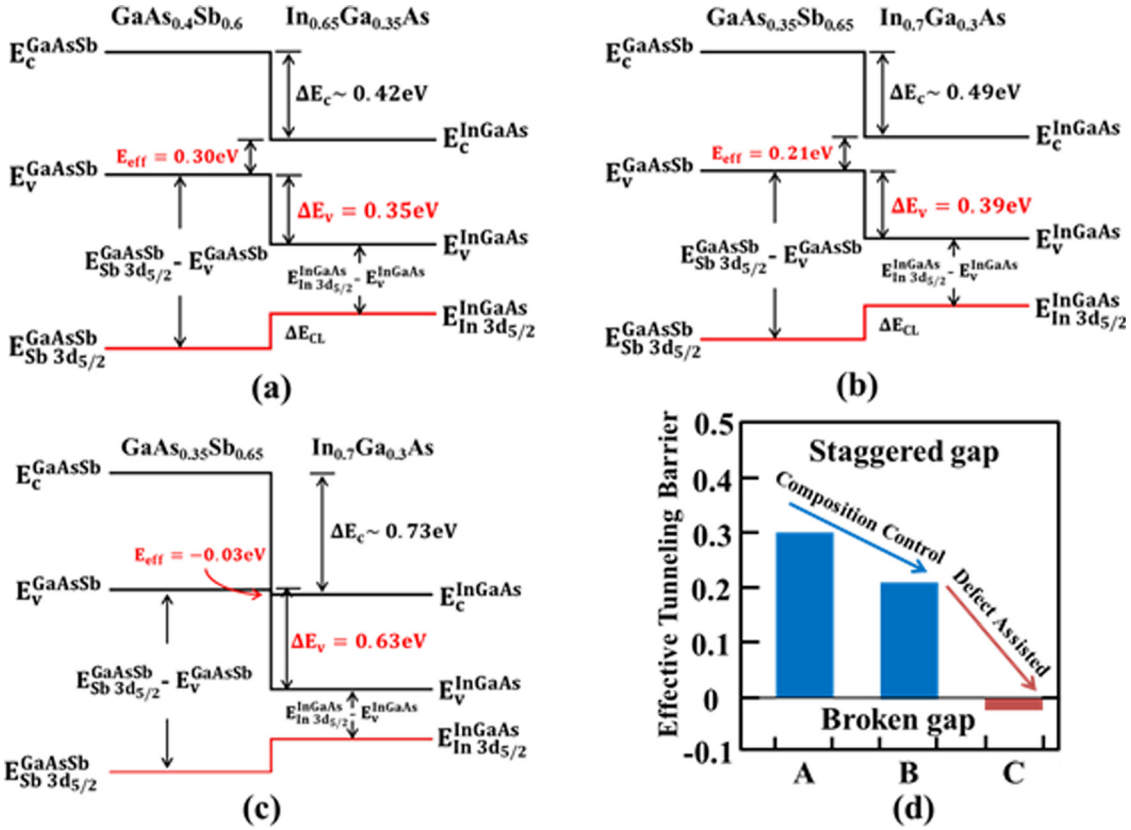

FIG. 7. Schematic energy band diagram of (a) structure A, (b) structure B, and (c) structure C. A type-II staggered band lineup with positive effective tunneling barrier height of 0.30 eV and 0.21 eV were determined at the heterointerface of structures A and B, respectively, while a broken band lineup with negative tunneling barrier height of −0.03 eV was found at the heterointerface of structure C. (d) Histogram summarized the effective tunneling barrier height and the corresponding band alignment types of these structures.

C where large amount of defects were confined at the interface as well as $In_{0.7}Ga_{0.3}As$ layer, as confirmed by RSM and cross-sectional TEM micrograph. Note that the alloy compositions of In and Sb were the same as that in structure B except the higher defect density at the interface as well as in $In_{0.7}Ga_{0.3}As$ layer. One can find from Fig. 7(c) that the value of E_{beff} is −0.03 eV, suggesting a broken band lineup. It is interesting to note that the band alignment was converted from staggered gap (structure A or B) to broken gap (structure C) due to the presence of large amount of defects in structure C. Figure 7(d) summarizes the effective tunneling barrier height and the corresponding band alignment types of these three structures. Previously, it has been predicted by simulation that fixed positive charges induced by defects at the GaAsSb/InGaAs heterointerface would bend the energy band and reduces the value of E_{beff}.[10] If the fixed charge density is large enough ($>6\times10^{12}/cm^2$), it will assist the band alignment transition from staggered to broken gap in a mixed As/Sb heterostructure.[10] Thus, the experimental data corroborated with the simulation result and confirmed the band alignment conversion from staggered to broken gap lineup in a mixed As/Sb TFET heterostructure. Although, greater BTBT probability is expected in a broken gap TFET than staggered gap due to lower tunneling barrier, the OFF-state leakage will drastically increase due to the reduced blocking barrier at OFF-state. As a result, reducing defect density at the GaAsSb/InGaAs interface is indispensable to achieve a tailored-made tunneling barrier height and possess the staggered band alignment, without which the steep switching and higher I_{ON}/I_{OFF} ratio of a TFET device would not be realized.

D. Device performances

In order to assess the impact of different effective tunneling barrier height and different band alignments on the performances of TFET devices, three sets of TFET devices with self-aligned gates were fabricated and tested. The detailed nano-pillar TFET device fabrication process flow can be found elsewhere.[8,25] Figure 8 shows the room temperature transfer characteristics (I_{DS}-V_{GS}) of TFET devices fabricated from structures A, B, and C measured at $V_{DS}=0.05$ V and 0.5 V. By comparing the transfer characteristics of TFETs fabricated from structures A and B, it can be observed that I_{ON} increased by ~2× with the reduction in E_{beff} from 0.30 eV to 0.21 eV. This is due to the reduced effective tunneling barrier height that enhances the tunneling transmission coefficient,[9] which effectively increased BTBT rate and I_{ON} current. Besides, the SS is also improved with reducing E_{beff} due to the bandpass filter behavior cutting off the high and low energy tail of the source Fermi distribution as a result of the particular band alignment condition.[26] In addition, the same tunneling current can be achieved at a lower applied gate voltage with a reduced E_{beff}, indicating that the low E_{beff} TFET device is more suitable for low power operation. In contrast, the I_{OFF} also increased due to

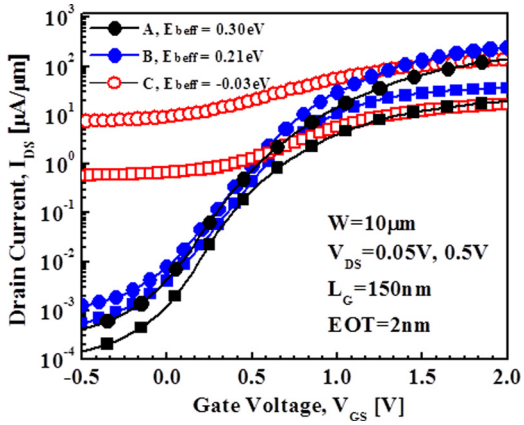

FIG. 8. Measured transferred characteristics (I_d-V_g) of TFET devices ($L = 150$ nm, $W = 10$ μm, and $EOT = 2$ nm) fabricated from structures A, B, and C at V_{DS} of 0.05 and 0.5 V. The TFET B ($E_{beff} = 0.21$ eV) demonstrated 2× improvement in ON-state current compared with A (E_{beff} of 0.30 eV). About 4 orders of magnitude increase in OFF-state leakage current was observed from TFET C than B due to the reduction of E_{beff} from 0.21 eV to −0.03 eV.

the reduction of E_{beff}. Essentially, I_{OFF} increased faster than I_{ON} with the scaling of E_{beff}. This is due to the reduced E_{beff} decreases the blocking barrier, which enhances both the BTBT probability and traps assisted tunneling process at OFF-state condition.[27] Furthermore, the bandgaps of source and channel materials also decreased with reducing E_{beff}, and a small energy gap leads to an additional increase of the OFF-state leakage due to more pronounced thermal emission process.[28] Therefore, a proper E_{beff} with appropriate bandgap energy in source and channel layer should be selected in order to fulfill high I_{ON} with desired I_{ON}/I_{OFF} ratio.

By comparing transfer characteristics of the TFET devices from structure C with structure B, significant difference within I_{ON} and I_{OFF} was found between these two structures although the Sb and In composition in source and channel materials kept the same. About 4 orders of magnitude higher OFF-state leakage current was observed from the structure C than that from structure B due to higher defect density within the source/channel interface and channel/drain layers of structure C. The value of I_{OFF} was extensively amplified due to the broken band alignment nature of structure C. In this case, the direct BTBT process dominates the OFF-state transport,[10] which is different as the Shockley-Read-Hall recombination mechanism in the OFF-state transport of most staggered gap TFETs.[10,27] An additional negative gate bias is required to turn off the OFF-state tunneling mechanism.[29] Besides, I_{ON} of the TFET from structure C is smaller than that from structure B under the same applied drain voltage. It is due to the fact that higher degree of recombination occurs owing to trap centers caused by much greater defect density in structure C. In addition, more than 4 orders in magnitude deterioration of I_{ON}/I_{OFF} ratio was found in the TFET devices fabricated from structure C than structure B. The largely increased I_{OFF} and degraded I_{ON}/I_{OFF} ratio indicates that the high defect density indeed present at the source/channel interface that assists the transition of band alignment from staggered to broken gap, supporting the structural analysis results. Measure must be taken to prevent the formation of large amount of defects at the critical heterointerface during the growth of TFET structure. Consequently, great efforts should be taken to preserve the staggered band alignment with low E_{beff}, otherwise all promotion on the performance of TFET brought by E_{beff} modulation will be in vain due to the band alignment transition.

IV. CONCLUSION

The compositional dependence of effective tunneling barrier height (E_{beff}) and defect assisted band alignment transition from staggered gap to broken gap in GaAsSb/InGaAs n-channel tunnel field effect transistor structures were demonstrated. By increasing In and Sb alloy compositions from 65% to 70% in $In_xGa_{1-x}As$ and 60% to 65% in $GaAs_{1-y}Sb_y$ layers, the E_{beff} was reduced from 0.30 eV to 0.21 eV, respectively. The transfer characteristics of TFET devices with E_{beff} of 0.21 eV demonstrated 2× improvement in ON-state current without significantly increase in OFF-state leakage. On contrary, the value of E_{beff} was decreased from 0.21 eV to −0.03 eV due to the presence of high defect density at the $GaAs_{0.35}Sb_{0.65}/In_{0.7}Ga_{0.3}As$ heterointerface. As a result, the band alignment was converted from staggered gap to broken gap, which leads to 4 orders of magnitude increase in OFF-state leakage current. These experimental findings were self-consistent with the simulated results previously reported. Therefore, a proper selection of E_{beff} and a high quality source/channel interface with well maintained low defect density is essential in a mixed As/Sb TFET structure in order to achieve high ON-state current and low OFF-state leakage for low standby power circuit applications.

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[1]W. M. Reddick and G. A. J. Amaratunga, Appl. Phys. Lett. **67**, 494 (1995).
[2]E. H. Toh, G. H. Wang, L. Chan, D. Sylvester, C. H. Heng, G. S. Samudra, and Y. C. Yeo, Jpn. J. Appl. Phys., Part 1 **47**, 2593 (2008).
[3]Hraziia, A. Vladimirescu, A. Amara, and C. Anghel, Solid-State Electron. **70**, 67 (2012).
[4]J. Appenzeller, Y. M. Lin, J. Knoch, and P. Avouris, Phys. Rev. Lett. **93**, 196805 (2004).
[5]W. Y. Choi, B. G. Park, J. D. Lee, and T. J. King Liu, IEEE Electron Device Lett. **28**, 743 (2007).
[6]G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, 2011), p. 785.
[7]H. Zhao, Y. T. Chen, Y. Z. Wang, F. Zhou, F. Xue, and J. C. Lee, Appl. Phys. Lett. **98**, 093501 (2011).
[8]D. K. Mohata, R. Bijesh, S. Mujumdar, C. Eaton, R. Engel-Herbert, T. Mayer, V. Narayanan, J. M. Fastenau, D. Loubychev, A. K. Liu, and S. Datta, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, 2011), p. 781.
[9]D. K. Mohata, R. Bijesh, Y. Zhu, M. K. Hudait, R. Southwick, Z. Chbili, D. Gundlach, J. Suehle, J. M. Fastenau, D. Loubychev, A. K. Liu, T. S. Mayer, V. Narayanan, and S. Datta, in *IEEE Symposium on VLSI Technology (VLSI)* (IEEE, 2012), p. 53.

[10]Y. Zhu, N. Jain, S. Vijayaraghavan, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, W. K. Liu, N. Monsegue, and M. K. Hudait, J. Appl. Phys. **112**, 024306 (2012).
[11]A. M. Ionescu and H. Riel, Nature **479**, 329 (2011).
[12]J. Knoch and J. Appenzeller, IEEE Electron Device Lett. **31**, 305 (2010).
[13]Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, "Band offset determination of mixed As/Sb type-II staggered gap heterostructure for n-channel tunnel field effect transistor application," J. Appl. Phys. (submitted).
[14]Y. Zhu, N. Jain, D. K. Mohata, S. Datta, D. Lubyshev, J. M. Fastenau, A. K. Liu, and M. K. Hudait, Appl. Phys. Lett. **101**, 112106 (2012).
[15]E. G. Seebauer and M. C. Kratzer, Mater. Sci. Eng. R **55**, 57 (2006).
[16]E. A. Kraut, R. W. Grant, J. R. Waldrop, and S. P. Kowalczyk, Phys. Rev. Lett. **44**, 1620 (1980).
[17]M. Kumar, M. K. Rajpalke, B. Roul, T. N. Bhat, A. T. Kalghatgi, and S. B. Krupanidhi, Phys. Status Solidi B **249**, 58 (2012).
[18]C. D. Wagner, Faraday Discuss. **60**, 291 (1975).
[19]A. W. C. Lin, N. R. Armstrong, and T. Kuwana, Anal. Chem. **49**, 1228 (1977).
[20]R. Delobel, H. Baussart, J. M. Leroy, J. Grimblot, and L. Gengembre, J. Chem. Soc., Faraday Trans. I **79**, 879 (1983).
[21]R. E. Nahory, M. A. Pollack, J. C. Dewinter, and K. M. Williams, J. Appl. Phys. **48**, 1607 (1977).
[22]M. K. Hudait, Y. Lin, M. N. Palmisiano, and S. A. Ringel, IEEE Electron Device Lett. **24**, 538 (2003).
[23]I. Vurgaftman, J. R. Meyer, and L. R. Ram-Mohan, J. Appl. Phys. **89**, 5815 (2001).
[24]H. Q. Wang, J. C. Zheng, R. Z. Wang, Y. M. Zheng, and S. H. Cai, Surf. Interface Anal. **28**, 177 (1999).
[25]D. K. Mohata, R. Bijesh, V. Saripalli, T. Mayer, and S. Datta, in *IEEE 69th Conference Proceedings of Device Research Conference (DRC)* (IEEE, 2008), p. 203.
[26]J. Knoch, S. Mantl, and J. Appenzeller, Solid-State Electron. **51**, 572 (2007).
[27]S. Mookerjea, D. Mohata, T. Mayer, V. Narayanan, and S. Datta, IEEE Electron Device Lett. **31**, 564 (2010).
[28]J. Knoch and J. Appenzeller, in *IEEE 63th Conference Proceedings of Device Research Conference (DRC)* (IEEE, 2005), p. 153.
[29]S. O. Koswatta, S. J. Koester, and W. Haensch, in *IEEE Conference Proceedings of International Electron Devices Meeting (IEDM)* (IEEE, 2009), p. 909.