tel-00417838, version 1 - 17 Sep 2009

Ph.D. THESIS

DESIGN OF CMOS ANALOG INTEGRATED CIRCUITS AS READOUT ELECTRONICS FOR HIGH-T_C SUPERCONDUCTOR AND SEMICONDUCTOR TERAHERTZ BOLOMETRIC SENSORS

By

VRATISLAV MICHAL

THESIS SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE DEGREE OF DOCTOR OF PHILOSPHY

UNIVERSITY PIERRE ET MARIE CURIE,

Laboratory: Laboratoire de Génie Electrique de Paris

Approved by: **BRNO UNIVERSITY OF TECHNOLOGY**

Laboratory: Department of Theoretical and Experimental Electrical Engineering

Defended: 10th of June 2009

Committee in charge:

Prof. Alain Kreisler	UPMC Univ. Paris 6	Supervisor
Assoc. Prof. Jiří Sedláček	Brno University of Technology	Supervisor
Prof. Pascal Fouillat	Université de Bordeaux 1	Examiner
Assoc. Prof. Pravoslav Martínek	Czech Technical University, Prague	Examiner
Prof. Aziz Benlarbi-Delaï	UPMC Univ. Paris 6	Committee Member
Prof. Dalibor Biolek	Brno University of Technology	Committee Member
Dr. Geoffry Klisnick	UPMC Univ. Paris 6	Invited member
Prof. Annick Dégardin	UPMC Univ. Paris 6	Invited member

tel-00417838, version 1 - 17 Sep 2009

THESE DE DOCTORAT DE L'UNIVERSITÉ PIERRE ET MARIE CURIE

Spécialité : Sciences pour l'ingénieur - Mention : Électronique

Approuvée par :

L'UNIVERSITÉ TECHNIQUE DE BRNO

Présentée par

M. Vratislav Michal

Pour obtenir le grade de

DOCTEUR DE L'UNIVERSITÉ PIERRE ET MARIE CURIE

Sujet de la thèse :

CONCEPTION DE CIRCUITS INTÉGRÉS CMOS ANALOGIQUES POUR L'ELECTRONIQUE DE LECTURE DE CAPTEURS BOLOMÉTRIQUES THz À BASE DE SEMICONDUCTEURS OU DE SUPRACONDUCTEURS À HAUTE TEMPÉRATURE CRITIQUE

Soutenue le 10 Juin 2009

Devant le jury composé de :

Prof. Alain Kreisler	UPMC Univ. Paris 6	Directeur de thèse
Assoc. Prof. Jiří Sedláček	Brno University of Technology	Directeur de thèse
Prof. Pascal Fouillat	Université de Bordeaux 1	Rapporteur
Assoc. Prof. Pravoslav Martínek	Czech Technical University, Prague	Rapporteur
Prof. Aziz Benlarbi-Delaï	UPMC Univ. Paris 6	Examinateur
Prof. Dalibor Biolek	Brno University of Technology	Examinateur
Dr. Geoffry Klisnick	UPMC Univ. Paris 6	Invité
Prof. Annick Dégardin	UPMC Univ. Paris 6	Invité

Université Pierre & Marie Curie - Paris 6
Bureau d'accueil, inscription des doctorants et base de données
Esc G, 2ème étage
15 rue de l'école de médecine
75270-PARIS CEDEX 06

Brno University of Technology
Faculty of Electrical Engineering and Communication
Údolní 244/53, 602 00 BRNO
CZECH REPUBLIC

E-mail author : vratislav.michal@gmail.com

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Acknowledgements

My PhD thesis presents a work elaborated in an intense collaborative context. It is therefore my pleasant task to express my gratitude to the persons and institutions which contributed to the thesis and helped me to develop my professional skills. First of all, I am very grateful that my supervisors accepted me for this thesis: Mr. *Jiří Sedláček* from UTEE VUT in Brno (Czech Republic) and Mr. *Alain Kreisler* from LGEP-Supélec (France).

My first contact with the research area started long before my thesis, by the contact with first named Mr. *J. Sedláček*. Mr. *Sedláček* permitted me to pass from the passionate amateur-radio world encountered in the electronics group of the Olomouc youth centre, leaded by *Karel Vrtěl* OK2VNJ, - to the word of academic and industrial research. At this period, Mr. *Sedláček* actively supplied me with interesting research tasks and helped me to acquire appropriate specific competences. Thanks to him, I also made acquaintance with people such as *Bohumír Sviežený* from ISEP-Paris engineering school, *Karel Hájek* from Military Academy of Brno or *Stanislav Sedlák* from S3 electronic company, all confirmed in the field of analog electronics. I was fortunate to spend long time with Professor *Hájek,* in a unique way by working, experimenting, and having unending discussions. This, looking back, mostly influenced my future centre of interests and workflow, and motivated me for my future work in the field of analogue electronics and analog signal processing.

Starting the Ph.D thesis at the end of 2004 has been based on the collaboration and excellent guidance of all these mentioned persons. As the work progressed, my attention has been more and more attracted to electronics, rather integrated than discrete ones. This because I estimated some electrical performances as being limited in the discrete-components word, and the neverending drilling of the printed circuit boards started to be boring. Therefore, I applied to the internship Nanotime located in the Paris engineering school Supélec, leaded by Ms. *Annick Dégardin*. This internship, of which the results expressively contributed to the thesis, gave me a possibility to discover the domains of the ultimate quantum and low-temperature physics, and allowed me to capitalize my experiences from the previous work and research in the field of applied analogue electronics.

A major importance of this internship was the possibility to collaborate with L2E laboratory of Paris 6 university (LISIF at the time). This presented dissertation would not have been possible without the expert guidance of the colleagues which I meet there, namely *Geoffry Klisnick, Gérard Sou, Michael Redon and Damien Prêle*. The initiations to the design of CMOS circuits or layout were always extremely perceptive, helpful, and appropriate; the passionate “eternal” discussions about the designed circuits are only a small fragment of the good memories which I will remember from this collaboration.

tel-00417838, version 1 - 17 Sep 2009

The role of my colleagues at L2E laboratory was also essential during the final – and difficult phase of the thesis writing. I executed many long travels from Grenoble, when I was employed at the time in "Commissariat à l'Energie Atomique". During these staying in L2E, I obtained many corrections and remarks of a crucial importance. During the long discussion with all above named colleagues, we clarified the basic ideas to be highlighted in the thesis. Here, I wish to underline my gratitude to Professor *M. Redon* for his time-expensing and rigorous verification of all mathematical theorems presented in the thesis. The provided instructions, together with the clear and well-oriented instructions and advices of Mr. *Sedláček* presented the main guide-line during the thesis writing. The final typographic and form checking was a last important phase to ensure a best impression of the assembled thesis and I thank Prof. *A. Kreisler* to have taken part in this task.

During the elaboration of the thesis, I was surrounded by many skillful people, both from the academic and the research world. Even thought many discussions were important for the thesis elaboration, they also helped me to organize my thesis and socially survive some difficult situations during the thesis preparation. I give hereby only an incomplete list of names: Prof. *Jarmila Dědková*, and Prof. *Karel Bartušek*, who helped me with the preparation of the thesis contract. Next, *Petr Drexler, Radek Kubásek, Mattia Longhin* and *Mario Aurino,* the friends being on the Ph.D preparation at the time. Here, I have to thank also to other friends and colleagues who helped me during the thesis writing, especially with the English grammar: *Vilém Guryča, Laurent Maingault, Panayotis Spathis, Bianca Hugo,* and others. The finalization of the thesis was facilitated by the gratitude of *Jean-Claude Villegier* from CEA-INAC laboratory in Grenoble, which employed me at the second half-period of the thesis and allowed me to perform almost complete cryogenic characterization of the fabricated circuits in INAC laboratory. I also thank to *Monique* and *Gilbert Zambetti*, my favorite professor of the ballroom dancing for contributing to a meaningful stay and integration in Paris.

At the end, my sincere gratitude goes to my parents and my whole family, who supported me during my youth "radiometers" age, as well as during the following engineering studies. They sometimes made considerable efforts to surmount some "difficulties" related to my interest in electronics; such as the disorder continuously diffused from my "ham-shack", or by providing a protection against the attacks from our neighbors, perturbed by my unwanted electromagnetic radiation.

I therefore express, once again, my gratitude to all these above mentioned persons as well as to many others who could not be named in this short, but important paragraph.

to Bianca

tel-00417838, version 1 - 17 Sep 2009

Table of contents

II Architecture of readout electronics

tel-00417838, version 1 - 17 Sep 2009

III Design of CMOS amplifiers

tel-00417838, version 1 - 17 Sep 2009

IV High performance active frequency filters

tel-00417838, version 1 - 17 Sep 2009

Appendix

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Scope of the PhD thesis:

My thesis was developed in the frame of the NanOtime project (NANostructures of Oxides for Terahertz IMaging Exploration), managed by LGEP-Supélec. The thesis deals with an innovative concept of *analog electronic circuits*. In particular, we aimed to provide low noise and low power signal amplification, as well as frequency filtering. The main goal is to create high-performance electronics being capable to operate at extreme conditions, such as low temperatures ("*cryogenic*" operations). As for real applications, I have constructed the signal readout electronics for bolometric detectors (THz range) working at both ambient (290K) and cryogenic (down to 40K) temperatures. As the output of my project, the electronics circuit designed might be advantageously employed in testing and developments of new- generation semiconductor bolometric sensors, as well as in high-performance superconductor THz imagers.

Although designed for operations at extreme conditions, the architecture of electronics presented here remains relatively uncomplicated and could easily be capitalized in a broad scale of common industrial applications, where robustness, high-performance, and low-cost are highly demanded.

Objectives of the thesis

The objectives of this thesis include two main topics concerning the design of:

i) *CMOS differential amplifiers for wide temperature range operations*

ii) *High-performance active frequency filters*

According to *i)*: I have revealed that classic amplification in closed loop could possess some limitations, such as lower frequency bandwidth, higher power consumption, or increased noise. The main contributions of the thesis in this area reside in the following:

- **Architecture of a feedback-free amplifier** (*chapter 4.6.2*)
  - The key element in electronic circuit design - differential voltage amplifier - was examined. The analysis of traditional amplifiers' architectures, employing negative

feedback, has shown some drawbacks, such as reduction of bandwidths caused by frequency compensation or increased complexity. Based on these conclusions, I have considered an unusual feedback-free architecture as an advantageous way to improve performances of the voltage amplifier. However, in such architecture, some serious problems had to be overcome (such as accuracy gain setting).

- **Low transconductance composite transistor**: (*chapter 5.3.5*)
  - The main challenge of the design is to achieve accurate and temperature-independent gain setting in the open-loop architecture. In order to do so, as the key part of the amplifiers designed hereafter, I have designed a *Low Transconductance Composite Transistor*. This transistor allows an accurate control of transconductance with subsequent accurate setting of final voltage gain.
- **1st type of differential fixed gain amplifier**: (*chapter 5.5*)
  - In order to provide high accuracy of the voltage gain, an amplifier benefiting from perfect component matching available in CMOS was designed. The design was performed in order to remove all inaccurate parameters (like channel length modulation). The resulting amplifier possesses voltage gain fixed only by the transistor's geometric ratios.
  - The electrical performances obtained by integration in conventional CMOS 0.35 µm process were proved to be competitive with the state-of-the-art of industrial amplifiers. I have confirmed the ability of this amplifier to operate at extreme conditions (40 K - 390 K).
- **2nd type of differential fixed gain amplifier** (*chapter 5.6*)
  - Another fixed gain amplifier I have designed is based on the integration of a low transconductance composite transistor in a *widely linear composite load*. This integration provides high linearity of DC characteristics. Moreover, it opens up an interesting way to control the temperature characteristics of gain (see next point). Similarly to the 1st type amplifier, the 2nd one operates in the feedback-free architecture and was integrated in 0.35 µm CMOS process. It results in very good electrical performances, constant over a wide temperature range (40 K - 390 K). This amplifier is, from the electrical point of view, almost ideal for a compact design (*e.g.* VLSI), due to large bandwidth, high input impedance, low distortion, and low noise/power consumption together with small final die size.
- **Voltage Control of the Thermal Gain characteristics:** (*chapter 5.6.4*)
  - In the design of 2nd type amplifier, I considered the effects of temperature, occurring in the MOS transistor. I have shown how this effect can be controlled by special circuit design. The proposed temperature compensation allows compensating the contributions of various temperature effects, thanks to bias supply voltage. This compensation is based on *hybrid current/voltage biasing*, where the temperature behavior of amplifier can be adapted either for ambient or wide temperature range.

According to *ii)* I focused on high-performance frequency filters and their possible extensions to higher frequency/dynamic range operations. In this section I reviewed the principal limitations of active low pass filters, caused by non-ideal characteristics of active

tel-00417838, version 1 - 17 Sep 2009

elements. Consequently, I have designed new filter structures allowing considerable improvements of the parameters. I am going to discuss:

- **Analysis of stop-band degradation of active low pass filters:** (*chapter 9.3*)
  - In fact, the extension of active frequency filters to higher frequencies is limited by the performances of active elements (such as operational amplifier). Especially for low-pass type of filters, the final stopband attenuation can be downgraded. I have identified the parasitic zero of two exemplary structures (Sallen-Key and FNDR) as main factors of this degradation.
- **Design of type II Sallen-Key biquadratic section:** (*chapter 9.4*)
  - Based on previous analysis, I modified the Sallen-Key biquadratic section. The idea was based on the removal of parasitic feedforward transfer in the circuit, which allows both increasing of the frequency of dominant parasitic zero and consequently reaching higher cut-off frequencies.
- **Current mode cascade section with no stopband degradation:** (*chapter 9.5*)
  - According to previous analysis, I defined some rules allowing to remove spurious transfers from the stop band area of AC characteristics. One of these rules is the elimination of active elements from the direct signal way at higher (stop-band) frequencies. I have designed a biquadratic filter based on the 2nd generation current conveyor CCII, which ideally possesses no parasitic zero in the transfer function. In doing so, 4th order low-pass filter with 10 MHz cut-off frequency reaching attenuation up to 100 dB was realized. In designing these two biquadratic sections (Sallen-Key and CCII) I have approximately shown how *the frequency range of low-pass filters can be enhanced by an alternative way to the common using of high frequency active elements*.
- **CMOS CCII current conveyor:** (*chapter 10*)
  - The current conveyor of second generation CCII is the core element of the previous CCII based biquadratic filter. In order to verify this structure, the CMOS integrated current conveyor CCII has to be developed. To provide a state-of-the-art electrical performance of the CCII, I have focused on the optimization of unity follower output impedance. In the final integrated version, this impedance reaches a low value, constant up to higher frequencies.

In résumé, my PhD thesis is suggesting a design of robust electrical circuits that might be of interest for future state-of-the-art scientific and industrial applications.

The present thesis is an outcome of a collaborative work amongst the Department of Theoretical and Experimental Electronics DTEE of Brno Technical University (Czech Republic); Laboratoire de Génie Electrique de Paris LGEP-Supélec (France); Military Academy of Brno (Czech Republic) and the Laboratory of Electronics and Electromagnetism L2E at UPMC-Paris 6 University (France).

This research project has been supported by a Marie Curie Early Stage Research Training Fellowship of the European Community's Sixth Framework Program under contract number MEST-CT-2005-020692, and by the Grant Agency of the Czech Republic under Grant 102/03/1181.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Part I:

General introduction

Summary

The general introduction is presented in thee separate chapters. We focus on the topics introducing the basic background, which is essential for the next design. The goal is the integration of very high electrical performance differential CMOS amplifiers, to be associated with the new generation of THz bolometric detectors (either low temperature superconducting, or room temperature semiconductors). In the first chapter, we introduce the basic concepts, physics and applications of bolometric detectors. The Second chapter deals with the basic principles and features of the MOS transistors, and the third chapter treats the fundamentals of electrical noise and low noise design.

tel-00417838, version 1 - 17 Sep 2009

1 BOLOMETRIC DETECTORS

1.1 Terahertz Imaging

Terahertz (THz) radiation covers a wavelength range of the electromagnetic spectrum spanning from submillimetre waves to the far infrared (see *Fig. 1.1*). Due to various interesting properties such as a high penetration capability (see [1], [2] for instance), the THz region is an important area of interest in many research domains. The operation with THz waves must also take into account various physical aspects such as the very low energy of the radiation (1 THz corresponds to photon energy of 4.1 meV). This is why the development of very high sensitivity terahertz detectors, allowing detection and processing of the electromagnetic signals in this area, is mandatory.

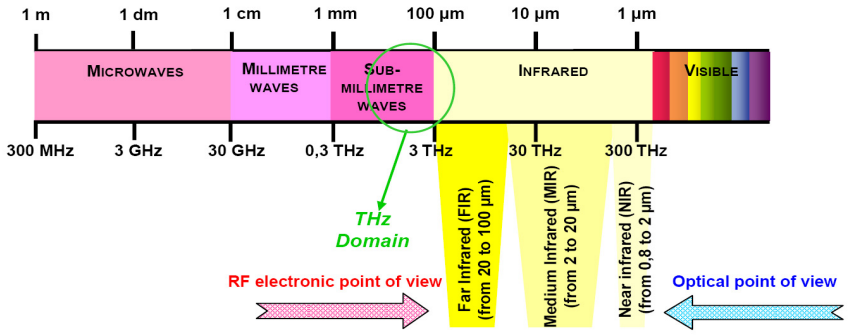


FIG. 1.1: *Spectral representation of investigated THz area [3]*

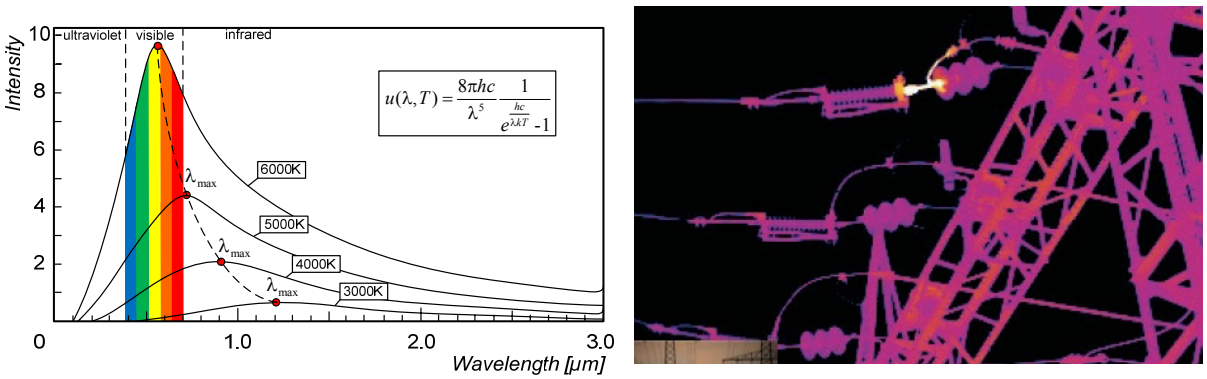
The spectrum of application using the properties of THz waves covers many research and civil domains. Two most important phenomena allow to distinguish the fields of application into two groups: one is the applications based on the penetration ability of THz waves; the other concerns the spectral analysis.

The *spectral analysis* investigates the electromagnetic radiation emitted by the objects, as the consequence of its chemical composition or inherent temperature (blackbody radiation). For instance, we can mention the application in chemical engineering, where the chemical composition of the investigated compounds is performed from their spectrum (*e.g.* the analysis of atmospheric pollution or submillimetre wave astronomy where the spectral lines allow the detection of specific molecules in Space).

The *blackbody radiation* is related to the object temperature and follows Planck's law. (See *Fig. 1.2 a*). The application related to the blackbody radiation concerns in particular thermal imaging in the THz and the infrared regions. We can see an example of thermal image in *Fig. 1.2 a*), provided by an industrial infrared sensor. In the scientific domain, a well known applications of THz imaging consists in the observation of tiny non-uniformities in the fosse radiation from the early universe

(Cosmic Microwave Background - CMB) exhibiting a spectrum peaking around $f \approx 160$ GHz (T = 2.725 K) (Cobe satellite (1989 [4]) or Planck satellite scheduled for late 2008 [5]).

The second type of applications is linked to the penetration of THz waves, for instance in the field of medicine [6] (the THz waves are not suspected to damage the tissues) or in civil security (detection of hidden weapons or explosives – see [2] for instance).



a) *b*)

FIG. 1.2: *a) Spectral density distribution of Planck's blackbody radiation, b) example of thermal imaging in the far infrared [7]*

1.2 Principal Detectors for the THz

Terahertz detection can be achieved with different types of sensors using various physical principles. The common function of these sensors is to convert the incoming energy to another physical parameter that can be easily measured. We can distinguish three principal types of detectors:

- **Photon detectors:** based on the direct interaction between a photon of the incoming radiation and the detector material. In a semiconductor junction, the absorbed IR photons create electron-hole pairs, and induce a photocurrent proportional to the intensity of the radiation. The fundamental property of these detectors is their limited frequency range, given by the incoming photon energy $E = \hbar \cdot \omega$. Recently investigated photon detectors such as Superconductor Single-Photon Detectors SSPD [8] are also among the most sensitive radiation detectors.
- **Thermal detectors**: transform the incoming radiation into thermal energy (heating), where the output electrical signal is a function of the absorbed energy. Change in temperature affects electrical properties allowing sensing through resistive or pyroelectric effects. In contrast with photon detectors, the wavelength operation range is given by the absorption of the sensor and can cover several decades of wavelengths.
- **Point detectors:** mostly realised as Schottky or S-I-S junctions (Superconductor-Insulator-Superconductor Josephson junction, see *section 3.5.3*). These detectors use the non-linear I-V characteristic with respect to the incoming RF (THz or microwave) power. Their application can be found in systems using heterodyne detection, where the local oscillator power and input signal are mixed due to the nonlinear characteristic of detector (more details are given in *section 1.3)*

1.2.1 Bolometric Detectors

A bolometer is a thermal detector based on the so called bolometric effect [9], [10] and is nowadays one of the most frequently used detectors in the submilimetre and infrared areas. The first experiment that demonstrated a bolometric effect used a metallic conducting layer as the bolometer material. Since then, improvements in materials science have allowed the use of semiconductors or superconductors having larger dR/dT values. The principle of bolometric effect is based on the

tel-00417838, version 1 - 17 Sep 2009

absorption of incident radiation and its transformation into heat produced in the bolometer sensitive layer. This sensitive layer is connected via a thermal link to the heat sink, having a constant temperature T_0. *Fig. 1.3* shows the structure of a typical bolometric detector. The sensitive layer is covered with an absorbing material. This material is characterized by a *factor* η, from which the reflection properties determine the wavelength range. The thermally sensitive layer is characterized by its *temperature coefficient of resistance* $\alpha = R^{-1}(dR/dT)$. The thermal link with conductance G provides the equilibrium between the sensitive layer and the heat sink at T_0. The both layers are characterized by the overall thermal capacitance C. The sensing of temperature is provided by associated electronics *via* the variations of the internal electrical resistance R_B.

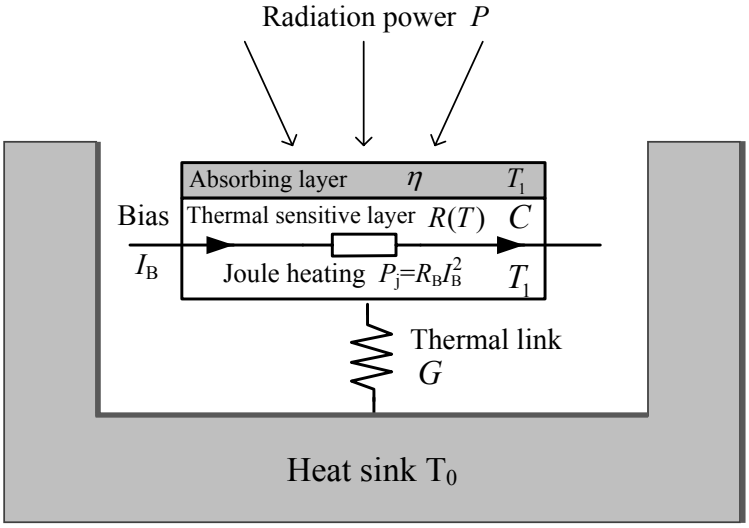


FIG. 1.3: *Composite bolometric sensor with absorbing layer (η), bolometer resistive body thermally connected to the heat sink at constant temperature T_0.*

During the time Δt, the incident power P (radiation or RF power) and joule heating P_j are stored in the bolometer body that increases its temperature by $\Delta T = (\eta \cdot P + P_j)\Delta t / C$. The temperature difference ΔT causes the heat flow $G\Delta T$ between the bolometer's body and the heat sink. When the system reaches internal thermal equilibrium, the heat outflow is equal to the incoming energy $\eta \cdot P + P_j$. The thermal time response can then be described by a 1st order linear heat transfer equation:

$$C\frac{dT}{dt} = \eta P + P_j - G(T - T_0)\,. \tag{1-1}$$

The joule heating, proportional to the bias current induces a constant temperature increase of $\Delta T = RI_B^2 / G$. For an applied sinusoidal radiation $\eta P = P_C + P_1 e^{j\omega t}$, the temperature response can be written as:

$$\Delta T = T_C + T_1 e^{j\omega t}\,, \tag{1-2}$$

where T_C is the constant temperature enhancement of P_C/G and $T_1 e^{j\omega t}$ a temperature variation defined as proportional to P_1. The value of T_1 can be found from (1-1) as:

$$T_1(\omega) = \frac{P_1}{G \cdot (1 + j\omega\tau)}, \tag{1-3}$$

where $\tau = C / G$ is the bolometer time constant corresponding to a pole of this elementary 1st order transfer function. The responsivity of the bolometric sensor (related to the output detected voltage) biased by a constant current I_B can be found by differentiation of (1-3) as:

tel-00417838, version 1 - 17 Sep 2009

$$R_V(\omega) = \frac{dV}{dP} = \frac{dV}{dT}\frac{dT}{dP} = I_B \frac{dR}{dT}\frac{1}{G\cdot(1+j\omega\tau)}. \quad (1\text{-}4)$$

In this equation, the dR/dT represents Thermal Coefficient of Resistance $TCR = \alpha = R^{-1}(dR/dT)$ $[K^{-1}]$

These two parameters (responsivity $R_V(\omega)$ and time constant τ) define basic performances of the bolometric detector. Equations (1-3) and (1-4) show that for achieving optimal responsivity versus maximal frequency leads to a trade-off for the values C and G. For instance, in high sensitive devices, the optimal configuration uses a low active volume (micro or nano – bridges) which allows to reduce the thermal capacity C. These bridges are then connected to the heat sink by means of a weak thermal link, reducing G (suspended bolometers) to prevent the thermal leakage. Naturally, good parameters for the device also depend on a proper materials choice, where a high TCR value is desired. The dR/dT characteristics of two materials commonly uses to fabricate bolometers (semiconductor and superconductor) are shown *Fig. 1.4*.

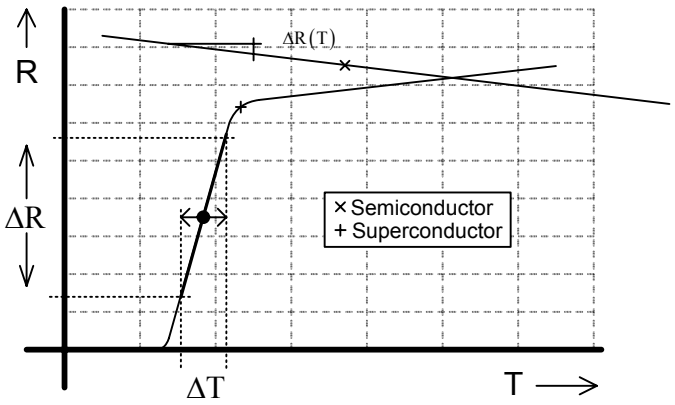


FIG. 1.4*: R(T) characteristics of superconductor and semiconductor bolometers.*

The superconductor material shows a positive dR/dT slope versus temperature in contrast to the negative one exhibited for the semiconductor device. Superconducting bolometers used in the transition area (also referred as Transition Edge Sensor - TES) can reach very high TCR values (thousands of K^{-1}).

1.2.2 Hot Electron Bolometric Effect

Various materials can be used to exploit different principles of heat transfer via the different mechanisms of particle interactions. This can contribute to different properties of detectors, in particular in the time domain. For instance, *Fig 1.5 a)* shows the classical bolometric effects occurring in normal (metallic or semiconductor) bolometer which can be compared with electron interactions occurring in superconducting Hot Electron Bolometers (HEB - *Fig. 1.5 b)* operating at the superconducting transition (*Fig. 1.4*).

The bolometric effect is usually described using macroscopic relations as described in the previous *section 1.2.1*. However, these physical quantities can be studied also on a microscopic level that allow to highlight other interesting features as we shall see further.

Microscopic interactions occurring in metallic bolometers can be explained as follows: a conductor is exposed to an external heating power (photon radiation or RF) which excites the electrons (e) from their conducting band. These free electrons interact with other free electrons but mainly with the crystal lattice of the bolometer body (represented by phonons p). The interaction time constants ($\tau_{e\text{-}e}$, $\tau_{e\text{-}p}$, $\tau_{p\text{-}e}$) determine the relationships for energy transfer between the free particles as shown on *Fig. 1.5 a)*. In a metal, electrons and phonons are closely interacting and are therefore in close thermal

tel-00417838, version 1 - 17 Sep 2009

equilibrium. The dominant time constant is then given by the time needed to reach a thermal equilibrium between the sensitive layer and heat sink, *i.e.* the phonon escape time τ_{esc}.

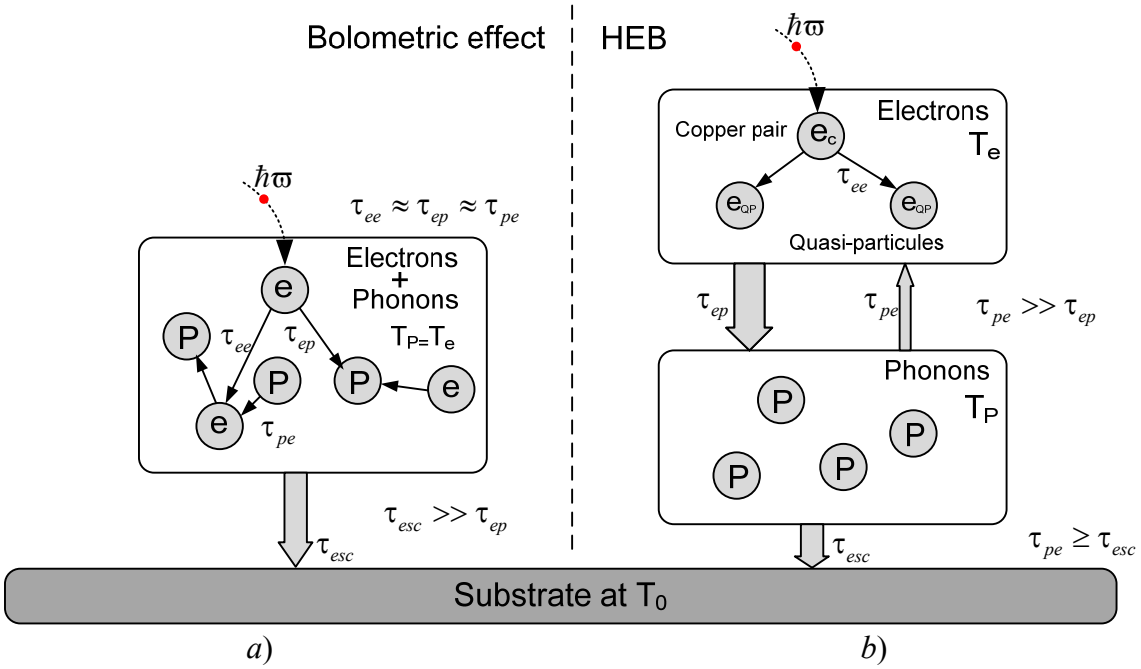


FIG. 1.5: *a) Interaction mechanism in a metallic bolometer (normal bolometric effect) and b) in superconductor Hot Electron Bolometer (HEB).*

In a BCS-like superconductor, the supercurrent transfer involves Cooper pair (e_C) flow [11]. Interactions of incoming photon with the superconducting material can break the Copper Pairs and create two high energy (hot) electrons called "quasi-particles" (QP) moving in the crystalline lattice (see *Fig 1.5 b*). These high energy electrons interact with other Copper pairs, as well as with other free electrons in the lattice structure. These interactions are very fast ($\tau_{e\text{-}e}$) and therefore all electron gas in the superconducting material is *spontaneously thermalized* [12]. Once the electron gas reaches internal equilibrium, the free electrons can be cooled down by two mechanisms: partly by hot electron diffusion into the normal metal pads at the end of the bolometric film (diffusion cooled bolometers [9], [10]) or by phonon scattering in the substrate as shown *Fig. 1.5 b*). Whereas the resistance of normal metallic materials is determined by phonon heating T_P, the superconducting materials in the resistive (transition) area exhibit a strong resistance versus electron temperature T_e dependence (dependence on the concentration of quasi-particles in the superconducting film).

It follows that the hot electron bolometric effect is observed in a time period for the incident radiation shorter than the phonon escape time τ_{esc}. If thermal variation time is longer than τ_{esc}, the system reaches a thermal equilibrium and normal bolometric effect is observed. The dominant time constant ($\tau_{e\text{-}p}$) of hot electron bolometer depends on the material lattice structure. For instance, niobium nitride (NbN) bolometers having a transition at ~16K reach $\tau_{e\text{-}p} \approx 10$ps. The newly developed high T_c bolometers based on yttrium barium copper oxides $Y_1Ba_2Cu_3O_{7\text{-}\delta}$ with superconducting transition close to liquid nitrogen boiling point (77 K) reach the $\tau_{e\text{-}p}$ in order of a few ps [10].

The frequency response of HEB is principally function of sensitive layer material, geometric dimensions and thermal coupling with the substrate. An example of modelled frequency response of an YBaCuO high T_c superconducting bolometer is shown in *Fig. 1.6* [10] for several device dimensions. In this model, we can distinguish a 1st normal bolometric plateau in the lower frequencies and hot electron bolometric effect above the frequency $1/\tau_{esc}$.

tel-00417838, version 1 - 17 Sep 2009

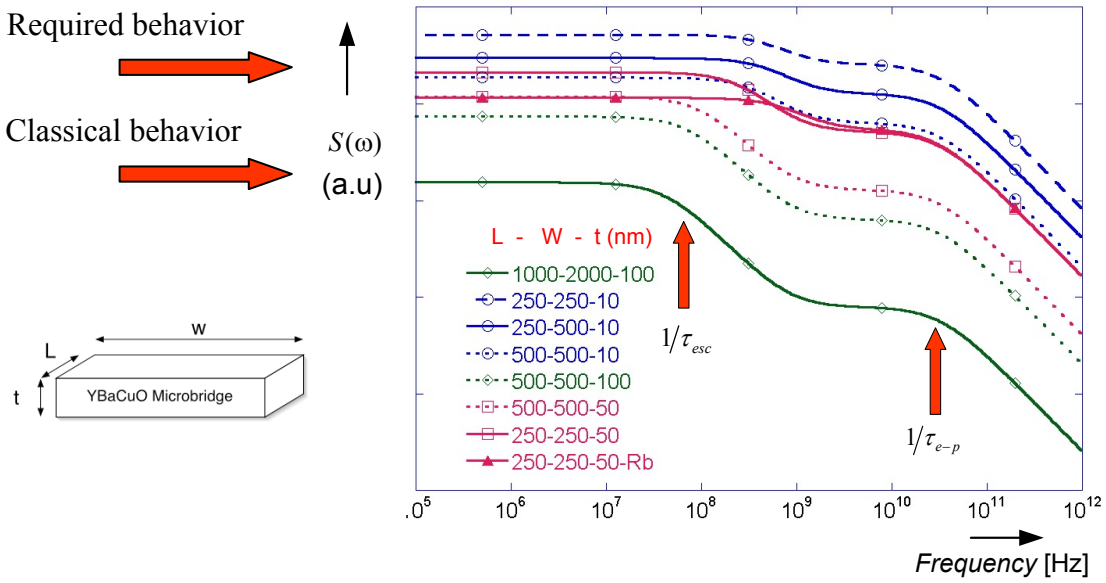


FIG. 1.6: *Frequency characteristic of YBaCuO superconductor thin bolometer with normal bolometric area and with hot electron bolometric response, calculated upon a three thermal reservoir flux model [10]*

1.2.3 Variety of Bolometric Sensors

In the previous paragraphs *1.2.1* and *1.2.2*, we saw that the basic properties of bolometric sensors are determined by the choice of material and geometrical shape. In *Section 1.2.1* we have also shown that the performances are a trade-off between the power sensitivity and maximum frequency response. Moreover, the output signal depends on the supplied power and thus on the active bolometer surface.

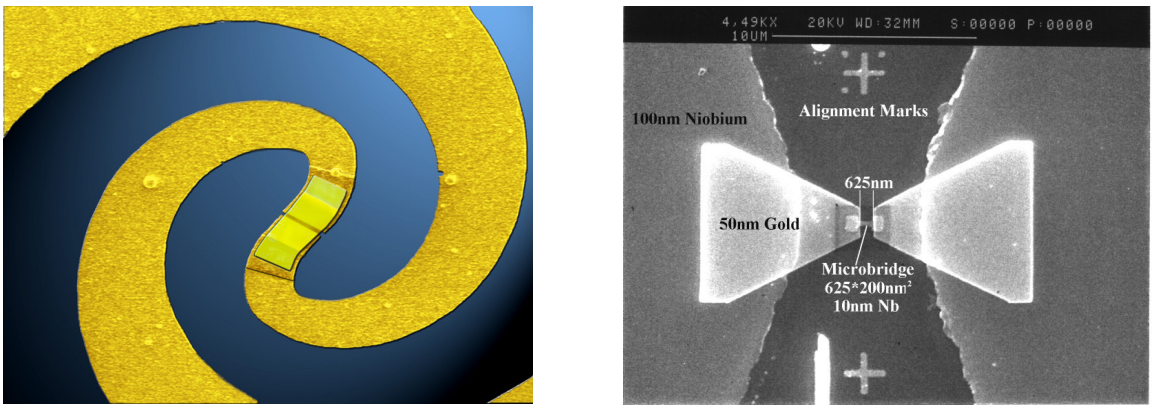


FIG. 1.7: *a) NbN nanobolometer with log-periodic spiral antenna [14], b) detail of such a nanobolometer patterned in an ultra-thin superconductor Nb film [15]*

Depending on the geometric shape, we may distinguish two basic groups of bolometers:

- **Superconductor nano-bolometers:** nanostructure of superconducting materials with very fast time response used for ultra high frequency applications (spectroscopy, heterodyne detection etc.) and generally realized as HEB.
- **Semiconductor or superconductor micro-bolometers:** structures designed for low frequency applications as thermal imaging, remote temperature measurements etc…, using various geometric patterns and various dimensions scale (tens of micrometers up to millimetres).

tel-00417838, version 1 - 17 Sep 2009

Since the detected output signal depends on the absorbed radiation power, the effective surface of the nanobridge/micro-bridge can be too small to receive the appropriate power. In this case, the incoming power need to be supplied by an external circuit such as miniature (metallic) antenna operating in the considered THz band [13]. *Fig. 1.7 a*) shows an example of wideband log-spiral gold antenna connected to an NbN nanobolometer and *b*) shows a SEM picture of an NbN 625×200×10nm nanobolometer. We can find a more detailed description of THz detectors in [21].

1.3 Heterodyne Detection

When an incoming signal (RF, THz or infrared) is simply absorbed by the bolometer, the measured output value is proportional to the average power dissipated in the bolometer sensitive layer. The bolometer is then operated in the so-called direct detection mode. A second type of operation can be achieved using two separate incident radiations. The heterodyne detection consists in mixing the power from a local oscillator (LO) with the wide band signal to be measured (RF). In the mathematically ideal case, the mixer output contains both input (LO and RF) signals as well as the signals at beating frequencies ω_{LO}-ω_{RF} and ω_{LO}+ω_{RF}, also called *Intermediate Frequency* products IF. When the ω_{LO}-ω_{RF} frequency is selected as the output signal, the mixer works in a down-conversion mode. In doing so, the input (THz) band can be translated to the lower GHz domain, where any classical laboratory equipment as a spectrum analyser can be used for the measurements. Devices usually used for the THz heterodyne detection are Schottky diodes, Superconductor-Insulator-Superconductor (S-I-S) Josephson Junctions or HEB bolometers [16], [17]. The principle of spectrum translation in a heterodyne detector is sketched on *Fig. 1.8*.

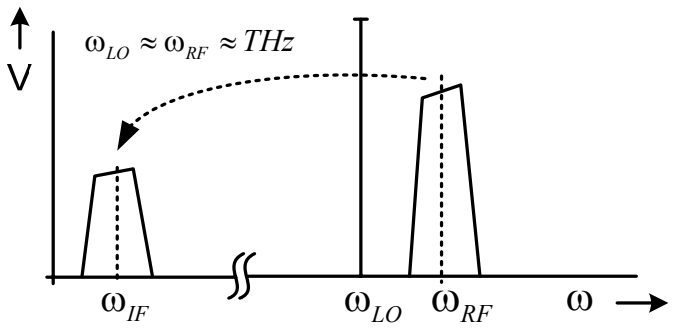


FIG. 1.8: *Translation of frequency spectrum in heterodyne detection*

In the case of a bolometric mixer, the dissipated power is proportional to the squared sum of both signals P_{LO} and P_{RF} and can be expressed as follows:

$$P(t) \approx \left(V_{LO}\cos\omega_{LO}t + V_{RF}\cos\omega_{RF}t\right)^2 \approx P_{LO} + P_{RF} + \\ + 2V_{LO}V_{RF}\left[\cos((\omega_{RF}-\omega_{LO})\cdot t) + \cos((\omega_{RF}+\omega_{LO})t)\right]. \quad (1\text{-}5)$$

As shown in a previous section (1.2.2), the bandwidth of a hot electron bolometer is limited by τe-p, the dominating time constant. The signal above $\omega = 1/\tau$(e-p) is integrated into a constant heating power as represented by P_{LO}+P_{RF} in (1-5). It follows that the bolometer temperature can only vary if the frequency is low enough so that $\omega < 1/\tau_{e\text{-}p}$, which can be the case for the intermediate frequency $|\omega_{RF}-\omega_{LO}|$. The principle of mixing on a resistive bolometer is shown in *Fig. 1.9*.

tel-00417838, version 1 - 17 Sep 2009

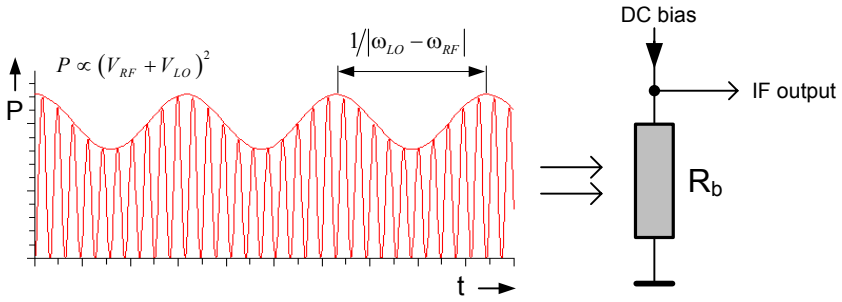


FIG. 1.9: *Heterodyne detection on a resistive bolometer body*

As shown in *section 1.2.2*, the maximum intermediate frequency of a HEB can reach the order of several GHz (~10 GHz for NbN HEB [18] and up to 100 GHz for YBCO High *Tc* bolometers [10]).

1.4 Noise in Bolometric Detectors

Each bolometric sensor generates an output voltage (current) independent of the signal of interest. This signal is referred to the noise voltage (current) [9], [10], [19]. Noise signals are one of the limiting factors for the detector sensitivity. However, the bolometer is the most sensitive part in the detectors chain because all spurious voltages are amplified by the signal amplifier. In the noise analysis, we can distinguish two kinds of noise sources: the noise having an electrical origin and the noise provided by other physical process such as environmental variations of (temperature, radiation etc.).

- **Electrical noise:** is caused by random electron motion interacting with the material lattice of a resistive bolometer body. The noise spectrum can be divided in three principal regions: *a*) a low frequency band following a 1/*f* asymptote and also referred to flicker noise; *b*) a middle frequency area with constant noise spectral density (mostly originating from Johnson thermal noise) and referred to white noise; and *c*) upper frequency band, where the noise spectral density decreases due to a shunt capacitance effect (see *chapter 3*). Noise properties of a bolometer can be optimized through its design. Both flicker and Johnson noises are function of the bolometer resistance, shape and operating temperature (*Eq*. 3-7 *chapter 3.3.1*). Flicker noise spectral density also depends on the material choice, where its homogeneity (on the surface first of all) plays a major role. A typical example of very low noise bolometer is the low resistance Transition Edge bolometric Sensor (TES [20]) operating at very low temperatures (hundreds of mK) and using a superconducting thin film with very good surface rugosity. In contrast, semiconductor bolometers designed for low cost room temperature applications yields in a higher inherent noise.
- **Noise sources with non-electrical origins:** includes all exterior influence affecting the output signal. Typical example is a dark noise caused by optical radiation not related to the investigated signal or thermal fluctuations caused by temperature variations of a thermal regulation system.

The classification of dominant noise sources is an important point to be taken into account during the architecture design. The choice of voltage/current biasing method as a function of the bolometer resistance, the conception of an optical system or the definition of the amplifier performance is the first step in the proper design of the THz detector chain (*chapter 4*).

tel-00417838, version 1 - 17 Sep 2009

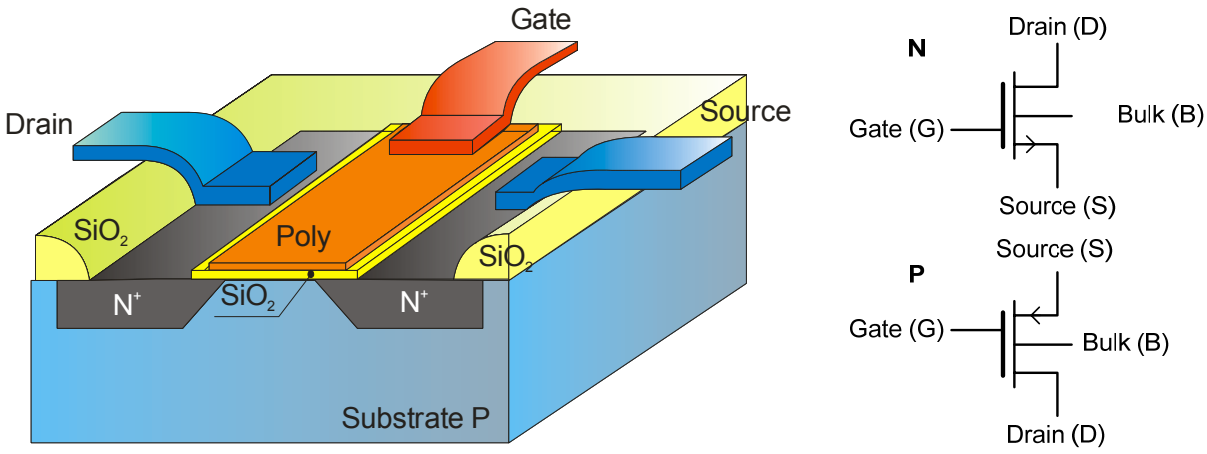
tel-00417838, version 1 - 17 Sep 2009

2 THE MOS TRANSISTOR

2.1 CMOS Device Overview

The CMOS (*Complementary Metal-Oxide-Semiconductor*) is a technological approach allowing the realization of discrete integrated circuits containing two polarities of Metal Oxide Transistors MOS, patterned on the same chip. The fabrication of both transistors' polarities onto a single chip was a fundamental stimulus in electronics, leading to the VLSI (Very Large Scale Integration) circuit concept. An example of a fundamental block realized in the CMOS technology is the simple inverter based on N and P channel type MOS transistors.

The basic building element in CMOS circuits is the MOS transistor, relying on the modulation of the channel current by an applied electric field. This means that contrary to a *Bipolar Junction Transistor* BJT, the MOS transistor has ideally no power dissipation occurring on the driving electrode. We consider the transistor MOS as a four-terminal semiconductor device, patterned in the *substrate*, where the driving electrodes are the *gate* G and *substrate* (Bulk - B), and output electrodes are *drain* D and *source* S. We can see the sketch of an N-channel type transistor in *Fig. 2.1 a*).



a) *b*)

FIG. 2.1: *a) Simple N-channel type transistor MOS with the substrate (bulk), drain, gate and source electrodes and thin insulating SiO_2 barrier b) schematic symbols of N and P-MOS transistors*

As we can observe in *Fig. 2.1*, the drain and source electrodes are the highly doped (N+) semiconductors embedded in the P-type substrate. The gate conducting electrode (metallic or polysilicon) is separated by a very thin silicon oxide insulating barrier ($\approx$ 10nm). The electrical

charge of the oxide is at the origin of the control mechanism, driving the current flow between the source and drain terminals: an applied gate voltage exceeding the so-called "*threshold voltage* V_{TH}" makes the transistor conductive and allows to control the drain-to-source current.

Fig. 2.1 b) shows the established symbols and assigned electrodes, used for N and P channel type transistors. The implementation of a P-MOS transistor in a standard CMOS process is shown in *Fig. 2.2,* where this device is plugged in the N-well region. Contrarily, the N-MOS transistor is simply patterned in the common substrate P (we refer the substrate regions as wells: N-well and P-well).

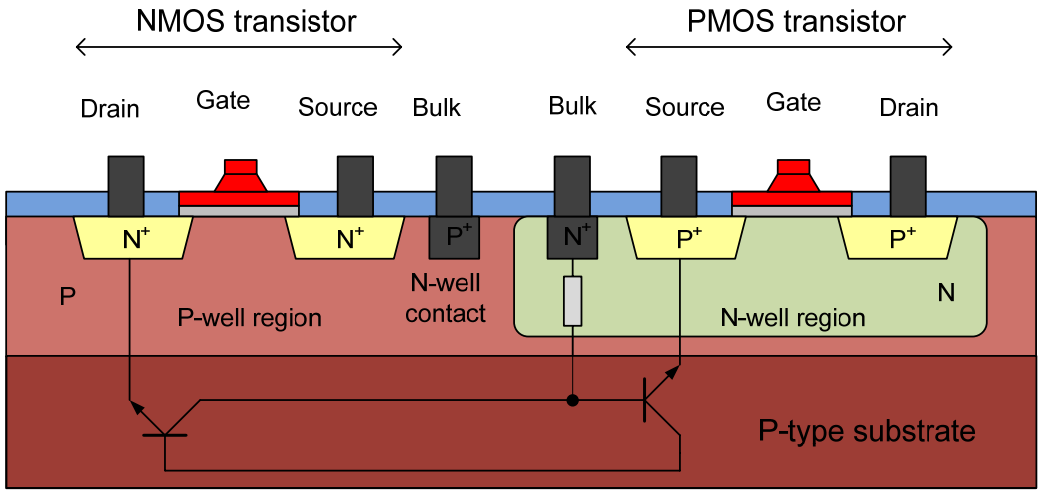


FIG. 2.2*: Cross-section of planar N-MOS and P-MOS transistor in common P-type substrate, with indicated parasitic thyristor causing the latch-up effect*

To ensure correct operation of CMOS devices, the substrate needs to be correctly biased. If this is the case, the PN junction between the P and N-well regions provides a natural isolation between the transistor wells. The rule is to keep the substrate (P) at the lower potential available in the circuit on the contrary to the P channel type transistor, where the N-well is usually connected to positive V_{DD}. However, under some unfavourable conditions, the circuit can reach a state called *latch-up* where the power supply lines are shorted by a parasitic thyristor. This thyristor (NPNP configuration, *Fig. 2.2*) is formed in the structure and its excessive current can damage the circuit. As we shall show in *chapter 8*, a correct biasing using substrate and well taps is an effective way to avoid this effect.

The impact of new technologies allows scaling the transistor to very low dimensions, commonly much below 1 µm. This has accelerated a fabrication of very high density circuits. The complexity of such circuits needs solving a large number of associated problems, like excess heat removal or miniaturizing local interconnection. As an example, we can show a cross-section showing the six-level metallic interconnecting system of a CMOS integrated circuit (*Fig. 2.3*).

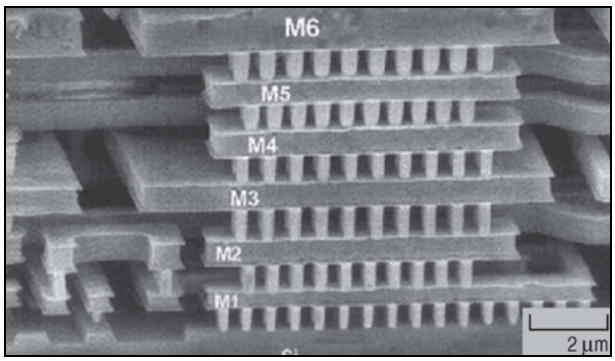


FIG. 2.3: *Cross-section e of a six-level metallic connection [38]*

In the following, we focus on MOS transistors provided by the Austria Microsystems foundry (AMS 0.35 µm). This process is characterized by four level connections and is detailed in *Fig. 2.17.*

tel-00417838, version 1 - 17 Sep 2009

The detailed description of a MOS transistor is available in the literature as [21], [22], [23]. In the following sections, we will summarize the basic principles and electrical characteristics, where the main features to design and optimize our future circuits will be highlighted. Some special properties, as transistor noise and temperature behaviour, will be treated in *chapters 3* and *chapter 5*.

2.2 Physics of the MOS Transistor

2.2.1 Semiconductors

Semiconductors are the elements found in columns II-VI of the periodic Mendeleyev table. The materials principally used for manufacturing the semiconductor devices are the silicon (Si) and germanium (Ge) or the compound semiconductors GaAs and InP. These two later are frequently used for the special (*i.e.* radio frequency or optoelectronic) applications. The pure (*intrinsic*) semiconductors have almost no free electrical carriers and have electrical properties very close to an insulator.

Naturally, we are interested in controlling the conductance of semiconducting elements. The current transfer can be allowed by several mechanisms: on the one hand by thermally excited free electrons from the parental atom and on the other hand by artificially introduced impurities (atoms with different valence number). The elements introduced in the intrinsic semiconductor are called dopants. The concentration of the dopants allows to control (during the manufacturing) the resistance over a wide range of values. The dopants for the silicon (Si) can be:

- **Dopants with 5 valence electrons** (*donors*) introduce one free electron per atom into the crystalline lattice (usually arsenic or phosphor). These donors provide free negative carriers in the semiconductor which are available for the conduction. The semiconductors doped by donors are called as N-type semiconductors.
- **Dopants with 3 valence electrons** (*acceptors*) attract one electron from neighbours' atom and cause the negative ionization of the semiconductor. The semiconductor doped by acceptors is labelled as P-type semiconductor.

The impurity concentrations are given by the number of acceptors (N_A) or donors (N_D) per cm^3. An increase in doping concentration gives rise to an increase of conductivity due to the higher concentration of carriers available for conduction.

The electrical current is a flow of carriers (electrons or holes). When the electric field is applied the free carriers, these are accelerated up to a speed called drift (carrier) velocity, determined by the electrical field value $\boldsymbol{E}$ [V/m] and carrier mobility μ_x (μ_n and $-\mu_p$ for the electron and hole, respectively). The carrier velocity can be written as:

$$v = \mu_x E\,, \tag{2-1}$$

where the carrier mobility depends on the concentration and polarity of dopants. The definition of electrical current as the volume of electrical charges transported per time unit allows, upon *Eq*.(2-1), to determine the resistance of elementary section of length *dx* and width *w* as:

$$dR = \frac{1}{\mu_x n_i q}\,dx\,, \tag{2-2}$$

where $n_i q$ present an electrical charge dQ in the elementary volume $w \cdot dx$. It follows that controlling the charge concentration allow the controlling of the resistance of semiconductor.

tel-00417838, version 1 - 17 Sep 2009

2.2.2 Physical Overview of the MOS Transistor

We have already presented the cross-section of the transistor MOS (*Fig. 2.1*). When considering the order of semiconductor layers, we can notice a similarity with another well-known element: a vertical N-P-N bipolar transistor. This simple comparison leads us to a first hypothesis: when the P layer separating the drain and source (N+ terminals) is under no influence of any external electrical field, no current can flow through such a device.

M-O-S Structure Viewed as Capacitor

We can start the analysis of the N channel type transistor (*Fig. 2.1*) with all four electrodes grounded (*e.g*. Gain, Drain, Source and Substrate B). We assume that the device is a "*long channel type*", which means low drain-to-source electrical field.

The section of the transistor MOS (seen in perpendicular direction to the gate surface) contains a sandwich of three layers: gate metallic electrode, SiO_2 insulator barrier and the P type substrate. This configuration can be seen as a capacitor with two electrodes: metallic at the gate side and semiconductor at the substrate side. As we expect, the ordinary capacitor with shorted electrodes contains no electrical charge in the dielectric. However, this is not the case of our investigated Metal-Insulator-Semiconductor capacitor. Here an inner potential Φ (in Volts) is present and such a device is not in electrical equilibrium. The potential Φ makes the Q-V curve (gate-to-substrate charge vs. voltage) complicated and composed of several different regions. In the following, a description of the charge distribution in the MOS device for various V_{GB} voltages will be provided, by using *Fig. 2.4* model, representing the MOS transistor with grounded Drain and Source electrodes.

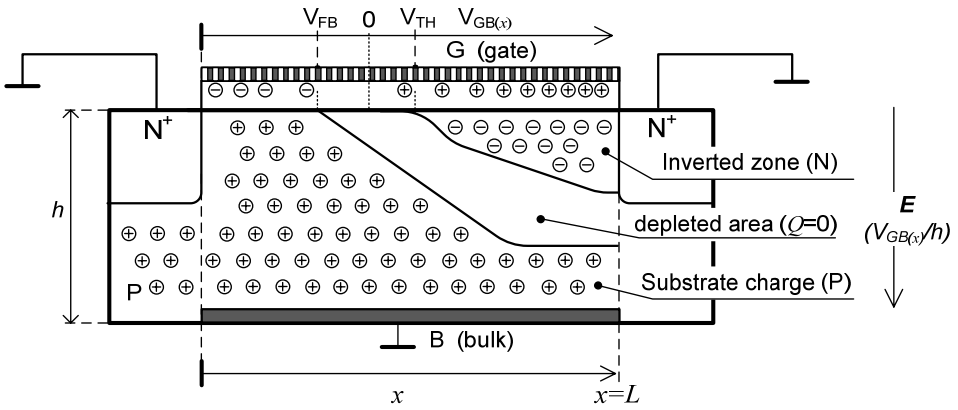


FIG. 2.4*: Idealized MOS capacitor demonstrating the charge distribution dependence on the Gate-to-Bulk voltage V_{GB}. The gate is composed from the isolated elements of the voltage increasing along the channel (this is not real MOS device!)*

In this model (*Fig. 2.4*), the gate-to-substrate voltage V_{GB} increases along the channel length (x), starting at any negative voltage at the left side (this is not the case in real MOS device because of the gate conductivity). Accordingly, the electric field ***E(x)*** (having only a gate to substrate direction) increases along the distance x together with increasing V_{GB}.

At some negative voltage V_{GB}, the positive free carriers of the channel are attracted to the substrate surface. Transistor operates in regime called *accumulation* where the drain and source are separated by the P-type channel and no current can circulate.

An increase of V_{GB} voltage (above the internal potential Φ) repulses the positive charges away from the channel surface and the charge decrease up to the original channel concentration N_A. The value of V_{GB} voltage where the barrier stores no free charge (depleted area) is called Flat Band voltage V_{FB} (cf. *Fig. 2.4*). The properties are close to an intrinsic semiconductor - insulator. An important situation occurs for the V_{GB} above so called "*Threshold voltage* V_{TH}" when the negative charges are attracted on the channel surface. The positive charges close to the gate metallic electrode attract free electrons to the channel surface: channel has changed the "polarity" and become an N-type semiconductor.

tel-00417838, version 1 - 17 Sep 2009

The value of the threshold voltage is mostly a function of the materials and process parameters (difference in work-function between gate and substrate materials, oxide thickness, Fermi voltage, charge of impurities trapped at the surface, dose of implanted ions, etc.) For zero V_{SB} voltage, the V_{T0} can be expressed as:

$$V_{T0} = V_{FB} + 2\Phi_F \pm \gamma\sqrt{2\left|\Phi_F\right|}. \tag{2-3}$$

In this equation, V_{FB} is the above mentioned flat-band voltage, $\Phi_F = -\Phi_T \ln(N_A/n_i)$ the Fermi potential, $\Phi_T = kT/q$ = 26 mV at 300 K is the thermal voltage; N_A is the acceptor ion concentration; $n_i \approx 1.5\text{x}10^{10}$ cm^{-3} at 300 K is the intrinsic carrier concentration in pure silicon). $\gamma = \sqrt{(2q\varepsilon siN_A)}/C_{OX}$ is the body factor depending on the channel doping concentration. Until now, we have considered the bulk at an identical (zero) voltage such as the drain and source. Naturally, the V_{SB} voltage has an impact to the channel charge distribution. This voltage can increase the width of the depleted area between the inducted channel and the substrate. It causes the threshold voltage swing:

$$V_{TH} = V_{T0} \pm \lambda\left(\sqrt{2\left|\Phi_F\right| + V_{SB}} - \sqrt{2\left|\Phi_F\right|}\right). \tag{2-4}$$

The exact physical interpretation of the symbols can be found for instance in [22].

Channel Conduction

We focus now on the case, were the V_{GS} voltage exceeds the threshold voltage V_{TH}. Above the V_{TH}, the channel charge density *continues to grow* and attracts even more free electrons to the channel surface. The local presence of the negative charge on semiconductor surface turns locally the polarity with respect to original channel doping. A so called "*inducted channel N*" uniform (for $V_{DS} = 0$) along the channel has been created. The charge accumulated on the channel surface Q_I can be calculated as:

$$Q_I = -C_{OX} W \cdot L\left(V_{GS} - V_{TH}\right), \tag{2-5}$$

where C_{OX} is the gate capacitance per unit surface specified by barrier thickness t_{ox} and dielectric constant $\varepsilon_0\varepsilon_r$ as $C_{OX}(\varepsilon_0\varepsilon_r/t_{ox})$ [F/m^2]. We can notice that until now, the N$^+$ doped source and drain terminals are interconnected by a uniform N-type conductive channel. Moreover, the negative charge close to the channel surface repels the positive charge and creates a depleted area between the channel surface and bulk electrode.

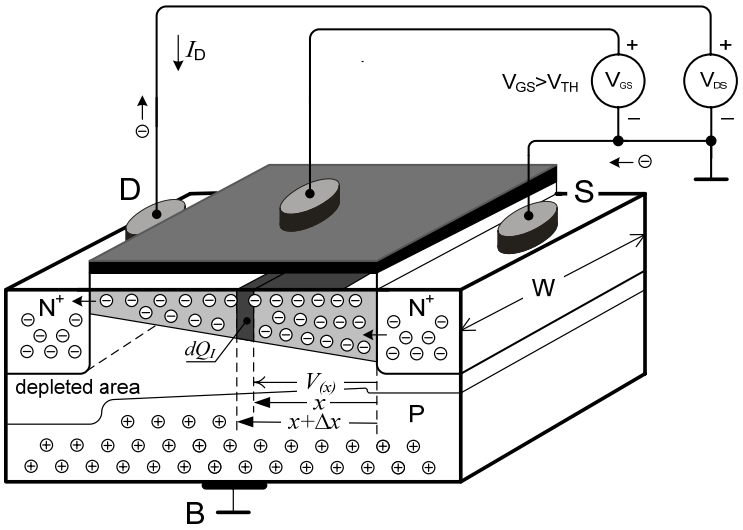


FIG. 2.5: *N-Channel transistor MOS with induced channel, allowing the current transfer between the drain and source*

tel-00417838, version 1 - 17 Sep 2009

Now, the drain to source voltage can be slightly increased. As shown in *Fig. 2.5*, the distribution *Q(x)* is no longer constant for $V_{DS} > 0$. The positive drain voltage makes the gate to channel voltage smaller in approaching the drain, which yields the decreasing of the accumulated charges (thickness of inducted channel). The effect of non-uniform Gate-to-Bulk potential can be inserted in *Eq.* (2-5) as the term *V(x)* (see *Fig. 2.5*). The elementary charge $dQ_I(x)$ accumulated at the distance *x* (measured from the source) can be expressed as:

$$dQ_I(x) = -C_{OX} W \left[(V_{GS} - V_{TH}) - V_{(x)} \right] dx \,. \tag{2-6}$$

We can deduce, that the presence of inducted charges along all the channel can occur only if the term $(V_{GS} - V_{TH} - V(x)) > 0$. As $V(x)$ at the drain end is directly V_{DS}, this condition can be expressed by means of new *saturation voltage* V_{DSsat} as $(V_{GS} - V_{TH}) > V_{DSsat}$.

The basic (*I-V*) characteristic of the MOS transistor can be derived from *Eq.*(2-6). *Eq.* (2-1) shows, that the carrier speed *v* is proportional to the electrical filed *E*. We can define the electrical current as the flow of free charges:

$$dQ = i \cdot dt \,, \tag{2-7}$$

where *dt* can be substituted by *dx*/*dv*. *Eq.*(2-7) can be inserted to the *Eq.*(2-6):

$$i \frac{dx}{dv} = -C_{OX} W \left[(V_{GS} - V_{TH}) - V(x) \right] dx \,. \tag{2-8}$$

The drift velocity *v* can be expressed by (2-1), where $E = dV/dx$:

$$i \cdot dx = -C_{OX} W \left[(V_{GS} - V_{TH}) - V(x) \right] dx \cdot \left(\mu \frac{dV}{dx} \right). \tag{2-9}$$

In this equation, we can notice the previously mentioned relationship of the resistance versus charge concentration in the semiconductor (see *Eq.*(2-2)). To obtain the value of drain current, the charge along the channel can be integrated:

$$i \int_0^L dx = -\mu C_{OX} W \int_0^{V_{DS}} \left[(V_{GS} - V_{TH}) - V(x) \right] dV \,. \tag{2-10}$$

This gives:

$$I_D = -\mu C_{OX} \frac{W}{L} \left[(V_{GS} - V_{TH}) V_{DS} - \frac{V_{DS}^2}{2} \right]. \tag{2-11}$$

This equation (2-11) describes the behaviour of transistor in the so called *linear* (ohmic) region. In this region, the transistor behaves as a quasi-linear resistor. However, *Eq.*(2-11) is only valid if the channel induction is present all over the device length.

The further increase of V_{DS} above V_{DSsat} can make the local gate electric field low enough, so that the channel carrier concentration becomes zero at some drain distance (*Fig. 2.6*). We say that the channel is "*pinched off*" and the charge does not increase any more with the V_{DS} voltage. The transistor is operating in so-called saturated region and behaves as V_{GS} *voltage controlled current source*. For drain voltage slightly larger than V_{DSsat}, the inducted channel is separated from the drain by the depleted area (L_{dep}) and the conduction is provided through a drift mechanism of electrons under the influence of the positive drain voltage: as the electrons leave the channel, they are injected into the drain depletion region and are subsequently accelerated toward the drain.

The drain current can be delivered by replacing the V_{DS} voltage (2-11) by the term V_{DSsat}. This results into a quadratic V_{GS} versus I_D current transfer characteristic:

$$I_D = \frac{\mu C_{OX}}{2} \frac{W}{L} \left(V_{GS} - V_{TH} \right)^2 . \tag{2-12}$$

tel-00417838, version 1 - 17 Sep 2009

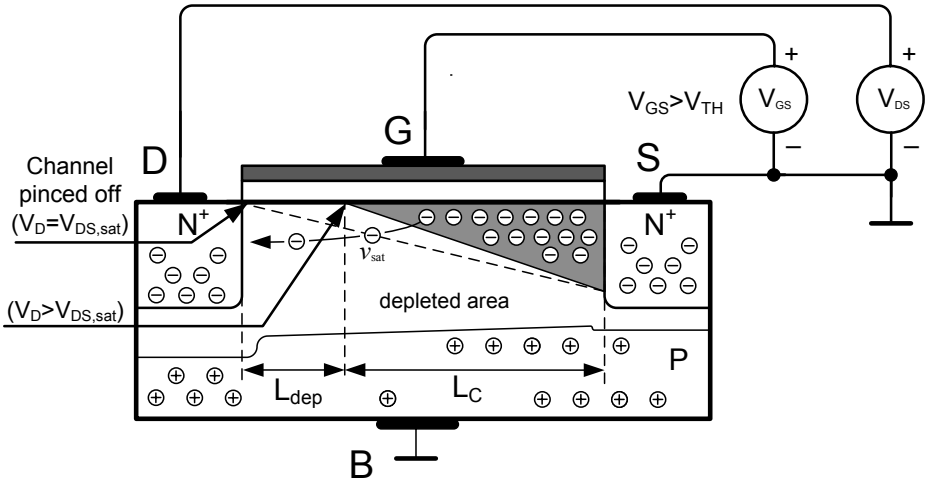


FIG. 2.6: *N-Channel MOS transistor in saturation with a) $V_{DS}=V_{GS}-V_{TH}$: dashed line and b) $V_{DS} > V_{GS}- V_{TH}$: dark area*

We can notice that this equation contains the V_{DS} voltage no more. Such a hypothesis is correct only when one of two following conditions is reached: *i*) the V_{DS} voltage is close to V_{DSsat}, *ii*) the device length is large enough so that the variation of the depleted area between the pinched off channel and drain (L_{dep}) can be neglected. If this is not the case, the *channel length variation* has to be taken into account.

The increasing of V_{DS} above V_{DSsat} causes the pinch-off point to move slightly away from the drain, consequently reducing the length of channel (*cf. Fig. 2.6*). We can define the effective electrical length of the channel as:

$$L_C = L - L_{dep}\,. \tag{2-13}$$

The effect of the channel length modulation can be evaluated by replacing the physical length of the channel L by the L_C (2-13) and by differentiating the I_D with respect to V_{DS} [22]:

$$\frac{\partial I_D}{\partial V_{DS}} = \frac{\mu_x C_{OX}}{2}\frac{W}{L_C^2}\left(V_{GS}-V_{TH}\right)^2\frac{dL_C}{dV_{DS}} = I_D\frac{1}{L_C}\cdot\frac{dL_{dep}}{dV_{DS}}\,. \tag{2-14}$$

The last term reflects an important property of transistor MOS operating in saturation area where the variation V_{DS} voltage impact to the drain current. To evaluate this effect, a new parameter - channel length modulation factor λ can be defined as:

$$\lambda = \frac{1}{L_C}\cdot\frac{dL_C}{dV_{DS}} = \frac{1}{L_C E}, \tag{2-15}$$

naturally its values depend on the device length. The channel length modulation can be taken into account in (2-12) and the saturation current I_D can be written as:

$$I_D = -\frac{\mu_x C_{OX}}{2}\frac{W}{L}\left(V_{GS}-V_{TH}\right)^2\left[1+\lambda\left(V_{DS}-V_{DSsat}\right)\right], \tag{2-16}$$

describing the drain current in the saturation with included channel length modulation effect. In order to operate with both channel type transistors (N-MOS and P-MOS), the notation (V_{TH}, μ_x) utilized in the previous equations has to be replaced by corresponding values: μ_p, μ_n and V_{THN}, $|V_{THP}|$, respectively.

tel-00417838, version 1 - 17 Sep 2009

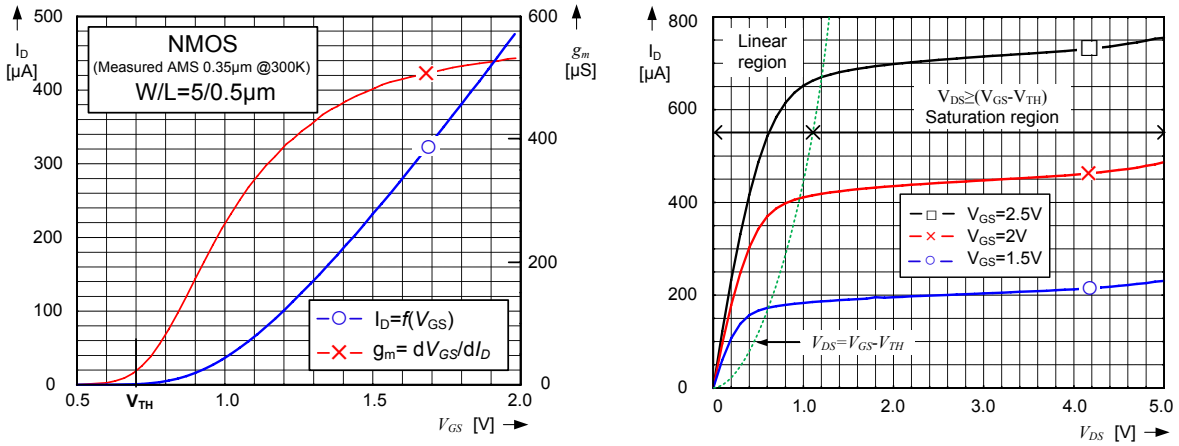
2.3 Electrical Characteristics of the MOS Transistor

To describe the electrical behaviour of the transistor MOS, we make use of the previous physical analysis. The design flow of CMOS circuits generally consists of several phases. In the phase dedicated to the circuit analysis, three steps are generally considered:

- **DC static analysis (circuits operating point (OP), DC transfer analysis)**
- **AC linear analysis (AC transfer, stability)**
- **Transient (step response, large signal stability)**

2.3.1 Static I-V Characteristic

Fig. 2.7 shows typical $I_D=f(V_{DS})$, $I_D=f(V_{GS})$ characteristics. As we have already pointed in the previous section, the transistor operates basically in three operating modes: cut off (subthreshold), linear and saturation.



a) *b)*

FIG. 2.7: *Measured characteristic of N-MOS transistor 15/5 µm a) I_D vs. V_{GS} with plotted $g_m = dI_D/dV_{GS}$ b) I_D vs. V_{GS} characteristic for the same transistor for various V_{GS} voltage*

In the following, we summarize the basic *I-V* characteristic and show that the basic transistor parameters can be controlled in the transistor geometrical scaling of *W* and *L*).

To simplify the notations, the parameter μC_{OX} will be also labelled *gain factor* KP_N and KP_P for an N-MOS and P-MOS transistor, respectively, and product $\mu C_{OX} W/L$ as the transistor "*gain*" β (both expressed in $A/V^{-½}$).

Transistor in the Subthreshold Area

The Transistor with the gate voltage below V_{TH} has no induced channel on the barrier interface and was previously considered as switched off. In reality, the concentration of free electrons on the channel surface is not fully zero for $V_{GS} < V_{TH}$ and a small diffusion current between the source and the channel can be observed. The transistor operating in this region (also called weak inversion) has an exponential dependence of I_0 and V_{GS}, given approximately by [25]:

$$I_D \approx 2\mu_x C_{OX} \frac{W}{L} \frac{(nkT/q)^2}{e} \left[\exp\left(\frac{V_{GS} - V_{TH}}{nkT/q} \right) \right] (1 + \lambda V_{DS}) \qquad (2\text{-}17)$$

This equation well approximates the subthreshold conductance around the zero gate voltage. A continuous increase of V_{GS} towards V_{TH} results in successive increase of channel charge, up to channel induction. It means that no abrupt On/Off drain switching occurs when the V_{GS} voltage swing around

tel-00417838, version 1 - 17 Sep 2009

the V_{TH} voltage. The consideration of subthreshold current is important in some cases, such as the evaluation of leakage current at high temperatures. Hence, many applications can make use of this region because of the high g_m/I_D factor (*chapter 2.4.3*), where a very low power application can be designed, as is the case of very low consumption amplifiers [26] (I_q = 10 nA).

Transistor in the Linear Region

For the gate-source V_{GS} voltage above the V_{TH} and drain to source voltage lower than $V_{GS} - V_{TH}$, the transistor operates in so-called linear (ohmic) regions. We can assimilate the transistor as a resistance controlled by the gate voltage. The drain current follows *Eq.*(2-11), where for very low V_{DS}, the quadratic term can be neglected. We can rewrite the linear formula by making use of *KP* and β as:

$$I_D \approx KP \cdot \frac{W}{L}(V_{GS} - V_{TH})V_{DS} = \beta \cdot (V_{GS} - V_{TH})V_{DS} \,. \tag{2-18}$$

The resulting drain-source resistance can be so deduced as in linearized form as:

$$R_{DS} = \frac{V_{DS}}{I_D} \approx \frac{1}{KP \cdot \frac{W}{L}(V_{GS} - V_{TH})}, \tag{2-19}$$

when the V_{DS} voltage approaches the V_{DSsat}, the term $V_{DS}^2/2$ in *Eq.*(2-11) has to be considered. In this case, the $1/R_{DS}$ slope is no longer exactly linear as we can see in *Fig. 2.7 a*).

Transistor in the Saturation Region

The horizontal parts of *I-V* characteristics *Fig. 2.7 b*) corresponds to the transistor operating in a mode "*constant current source*" called saturation. This region can be reached by setting V_{DS} above the value V_{DSsat} ($V_{DS} > V_{DSsat}$). As we have shown in *section 2.2.2,* the channel reaches no longer the train extremity and is "pinched off". The drain current follows the square law given by (2-16). Usually, the channel length modulation term $\lambda(V_{DS}\text{-}V_{DSsat})$ is simplified to $\lambda \cdot V_{DS}$, from which results:

$$I_D = \frac{KP}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2\left(1 + \lambda V_{DS}\right), \tag{2-20}$$

valid for $V_{SB} = 0$. The channel length modulation factor λ is defined by (2-15), and vary in function of process parameters in between 0.1-0.01 [V^{-1}] (the channel length modulation is sometimes assimilated to the Early voltage (*Fig. 2.8*) of a bipolar transistor). This factor limits the output resistance of the transistor operating as a current source and for small signal variations can be modelled as the parasitic source to drain resistance r_{DS}:

$$r_{DS} = \frac{1}{\lambda I_D} \,. \tag{2-21}$$

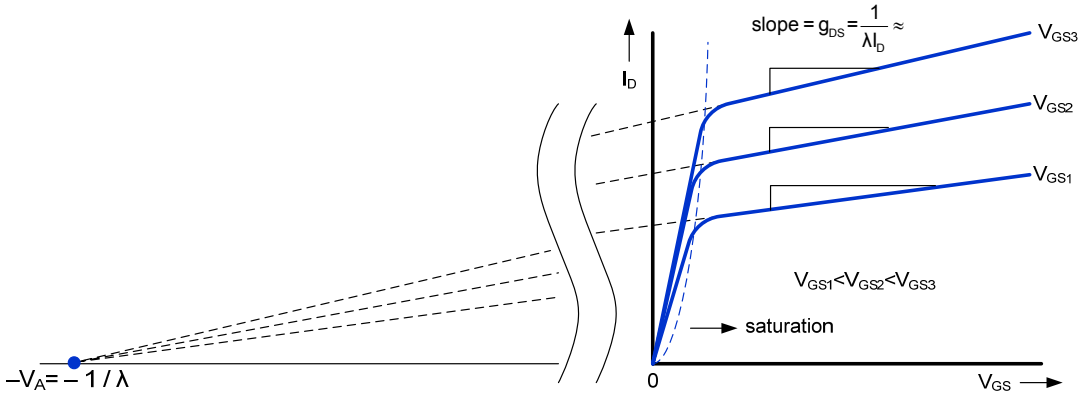


FIG. 2.8: *Effect of channel length modulation to the current I_D*

tel-00417838, version 1 - 17 Sep 2009

In a majority of analog CMOS circuits, the transistors operate in the saturation mode, where the performances are well defined and are easily reproducible. On this account, we consider formula (2-20) as one of most important one in CMOS circuit design.

2.3.2 Small Signal Parameters

In many cases, we are interested to determine the dynamic parameters of CMOS circuits as the voltage gain of amplifier, input or output impedances etc. Usually, this family of parameters makes use of linearized static parameters, what refers to the 1st derivative of the *I-V* characteristics. The linearized parameters are called "*small signal*" parameters and analysis dealing these parameters is called *small signal analysis*.

Basically, two kinds of parameters are used in the analysis: static small signal transconductance (or conductance) *g* and small signal capacitance *c*. The interest this use can be realized during the analysis, where even a complex circuit can be modelled by a simple linear model. However, the results are only valid for signals that are relatively small as compared to eventual nonlinearities of the circuit characteristics.

The transistor MOS is described by the basic parameters:

- **Gate transconductance g_m**
- **Channel conductance g_{DS}**
- **Body transconductance g_{mB}**

As mentioned above, all parameters are derived by using the static *I-V* characteristic, namely (2-17), (2-18), (2-20). The (small signal) drain current i_{DS} of the transistor can be written as function of all the terminal voltage as the superposition:

$$i_{DS} = \left(\frac{\partial I_D}{\partial V_{GS_Q}}\right) v_{GS} + \left(\frac{\partial I_D}{\partial V_{SB_Q}}\right) v_{SB} + \left(\frac{\partial I_D}{\partial V_{DS_Q}}\right) v_{DS}\,, \tag{2-22}$$

where $\delta f(x)/\delta V(x)$ is one of the three considered transconductances, calculated for *a given operating point* (V_{GSQ}, I_{DSQ},V_{SBQ}). Accordingly, *Eq.* (2-22) can be re-written in the simple form:

$$i_{DS} = g_m v_{GS} - g_{mB} v_{SB} + g_{DS} v_{DS}\,. \tag{2-23}$$

This symbolic expression can be graphically represented by an equivalent circuit named *static small signal* model of the transistor MOS. It contains a gate to source voltage controlled current source i_D, a source to substrate voltage controlled current source i_B and constant drain to source resistance r_D.

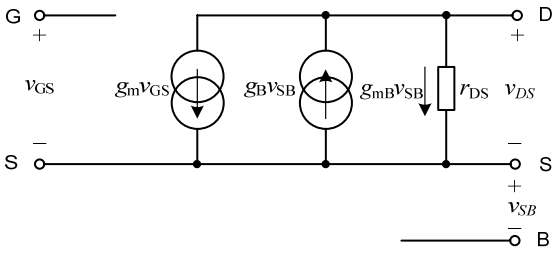


FIG. 2.9: *Static small signal model of the MOS transistor containing the gate and substrate transconductance g_m an g_B, and channel resistance r_{DS} (=1/g_{DS})*

Gate Transconductance g_m

For an alternative signal v_{GS} superposing to the continuous voltage V_{GS}, the saturation drain current given by (2-20) can be rewritten as the sum $I_{DS}(V_{GS})+i_{DS}(v_{GS})$:

tel-00417838, version 1 - 17 Sep 2009

$$I_{DS} + i_{DS} = \frac{KP}{2}\frac{W}{L}\left(\left(V_{GS} + v_{GS}\right) - V_{TH}\right)^2 \left(1 + \lambda V_{DS}\right), \tag{2-24}$$

where the value of i_{DS} is a function of the slope $\partial I_D / \partial V_{GS}$, called *gate transconductance* g_m. For a given operating point (indices *Q*), the value of the gate transconductance can be written as a function of V_{GS}:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = KP\frac{W}{L}\left(V_{GS} - V_{TH}\right), \tag{2-25}$$

and can be assimilated into the *voltage/current gain*. *Fig 2.7 a*) shows a graphical interpretation of g_m where the value g_m depending on applied V_{GS} can be seen. In some cases, it can be advantageous to express the gate transconductance in terms of the drain current I_D:

$$g_m = \sqrt{2KP\frac{W}{L}I_D} = \frac{2I_D}{V_{GS} - V_{TH}}. \tag{2-26}$$

These two last equations (2-25) and (2-26) show that the gate transconductance can be fixed simultaneously by the V_{GS} voltage, or by the drain current I_D. We can similarly derive the transconductance of the transistor operating in the ohmic region:

$$g_m = KP\frac{W}{L}V_{GS} \tag{2-27}$$

and subthreshold region respectively:

$$g_m = \frac{I_D}{kT/q \cdot N_0}, \tag{2-28}$$

where $V_T = kT/q$ is the thermal voltage and N_0 the subthreshold slope parameter [22].

Channel Conductance g_{DS}

The channel conductance g_{DS} can be assimilate to the parallel channel resistance r_{DS} (*Fig. 2.9*), as defined by *Eq.*(2-21). This "resistance" is caused by the channel length modulation occurring in the saturation area and by the channel conductance in the linear region (*Eq*. (2-19)). By derivation of (2-20) with respect to V_{DS}, the channel conductance in the saturation region can be expressed as:

$$g_{DS} = \frac{\partial I_D}{\partial V_{DS}} = \lambda \cdot \frac{KP}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 \approx \lambda I_{DS}, \tag{2-29}$$

where λ is the channel length modulation factor (2-21). The value of g_{DS} in linear region can be found similarly as:

$$g_{DS} = KP\frac{W}{L}\left(V_{GS} - V_{TH} - V_{DS}\right). \tag{2-30}$$

Generally, the channel conductance is the parameter that degrades the performance of the transistor operating in the saturation. Its elimination can be provided by a proper circuit design (*i.e*. using of cascode configuration, see *section 5.4.1*) or by proper device scaling (λ is less for the long channel devices, see *Eq*.(2-15)).

Substrate Transconductance g_{mB}

As shown by *Eq*. (2-3) and *Eq*.(2-4), the threshold voltage has a slight dependence on source to substrate voltage. Since $V_{SB} \neq 0$, value g_{mB} can be expressed as:

tel-00417838, version 1 - 17 Sep 2009

$$g_{mB} = \frac{\partial I_D}{\partial V_{TH}} \frac{\partial V_{TH}}{\partial V_{SB_Q}} \frac{\gamma}{2\sqrt{2|\Phi_F| + V_{SB_Q}}} \cdot g_m, \tag{2-31}$$

where γ, and Φ_F are the parameters introduced in *section 2.2.2*, V_{SB} is source to substrate voltage at operating point Q and g_m is the gate transconductance given by (2-25) or (2-26).

2.4 Parasitic Elements in the MOS Device

The aim of the mathematical description of the MOS transistor is to approximate the behaviour of a real device. However, a real MOS transistor is affected by many "secondary" parameters. A complex mathematical description of such parameters is available in the appropriate CAD models. In this section, we will focus to the most important "parasitic" elements: capacitances in the MOS device and effects arising from the low dimensions of the transistor.

2.4.1 Capacities in the MOS transistor

If the small signal model is used for the dynamic analysis (AC or transient), it has to be completed by the parasitic capacitances present in the structure. In the previous section, we have noticed, that the capacitance is considered as a small signal parameter. Generally, two types of capacitances are present in the CMOS circuits:

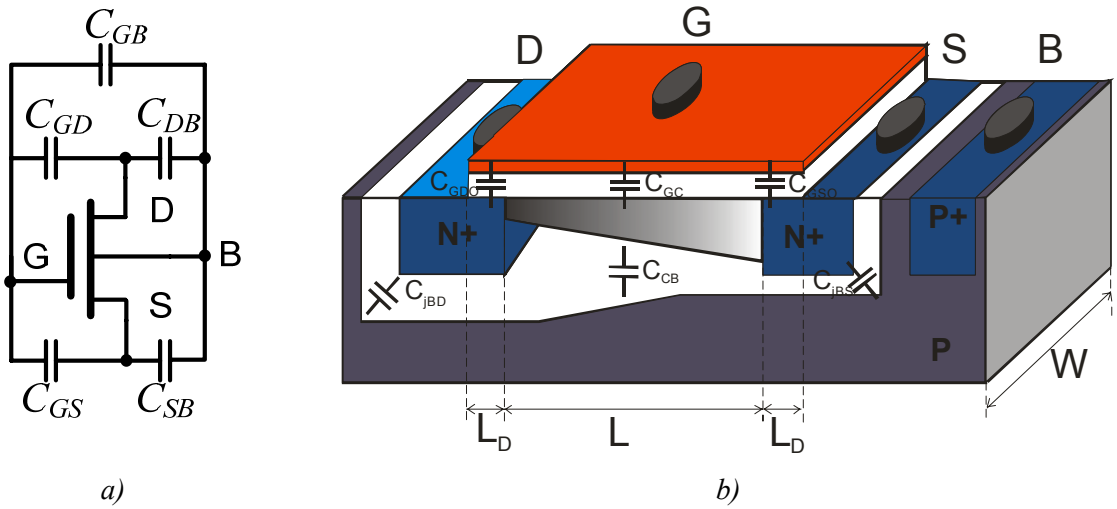
- **Capacitances caused by device geometry**
- **Variables capacitances depending on the operating point**

Since the sum of theses capacitances on the device terminals is present, the total capacitance has to be evaluated for a given operating point. The basic model, including all terminal capacitances is shown in *Fig. 2.10 a*) and the physical meaning of these capacitances is presented in the device model *Fig. 2.10 b*).

The gate-drain and gate-source overlap capacitances C_{GDO}, C_{GSO}, respectively, originate from the device shape. The gate electrode covers the drain and source areas and are characterized by the overlap length L_D (*Fig. 2.10*). Since the dielectric is characterized by the thickness t_{ox} and ε_r, the C_{GDO} and C_{GSO} capacitances can be expressed as the product:

$$C_{GSO} = C_{GDO} = \frac{\varepsilon_0 \varepsilon_r}{t_{ox}} W \cdot L_D = C_{OX} \cdot W \cdot L_D, \tag{2-32}$$

where the C_{OX} is the gate surface capacitance. The overlap length is generally given as a capacitance per unit of length (~100 pF/m for AMS 0.35 µm process).



a) *b)*

FIG. 2.10: *a) MOS terminal capacitances, b) physical interpretation off the MOS capacitances*

tel-00417838, version 1 - 17 Sep 2009

The dominant capacitance of the MOS transistor is the gate-to-channel capacitance, treated in the *section 2.2.2*. Here, a strong V_{GS} voltage vs. gate-to-channel capacitance dependence in depleted region can be observed (see also *Fig. 2.11*). If the channel surface is free of charge (depleted) the gate-to-channel capacitance is replaced by the gate-substrate C_{SB} capacitance with relatively low value. When positive charges are present on the channel surface (transistor in accumulation mode), the gate-substrate C_{GB} capacitance is given by channel surface capacitance C_{OX}:

$$C_{GB} = C_{OX} \cdot W \cdot L \,. \tag{2-33}$$

In the other hand, we can write the same formula for strong inversion (ohmic and saturated regions), where the inducted (conducting) channel is present. So that the gate to channel capacity $C_{GC} = C_{GB}$.

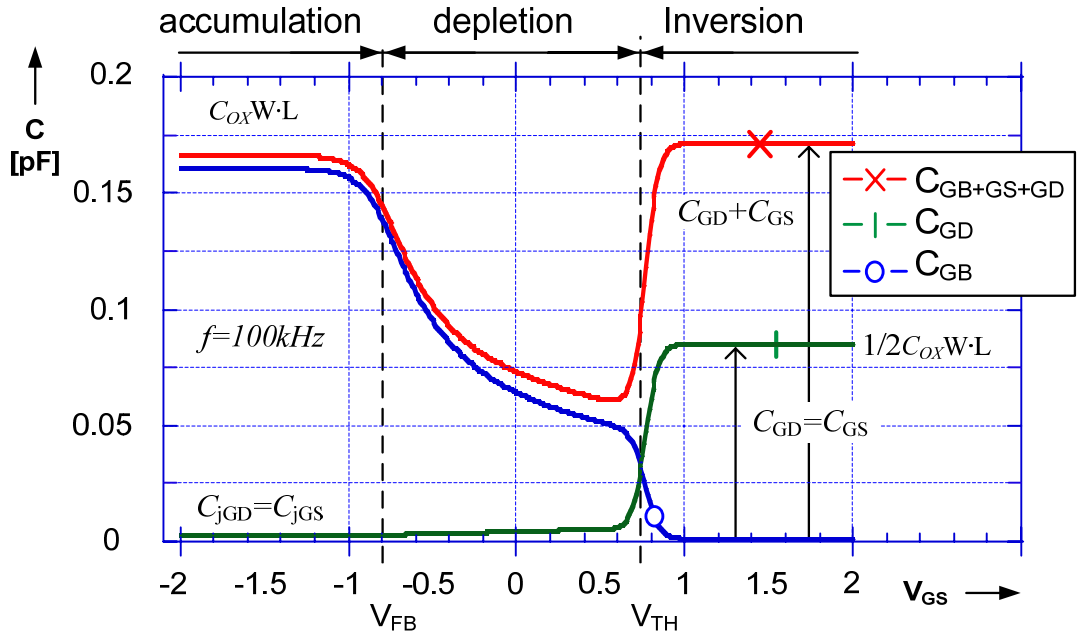


FIG. 2.11: *C-V characteristic of the N-MOS 15 µm/5 µm transistor.(Terminals D, S, B are grounded)*

To show the relationship between the V_{GS} voltage and gate capacitance C_{GS}, *Fig. 2.11* was drawn as a typical *C-V characteristic* [27], [22]. As we can show in *Fig. 2.4*, the inducted channel creates the depleted area between the channel and the substrate. It follows that the gate-substrate capacitance C_{GC} is "shielded" by the inducted channel (connected to the source and drain terminals). Consequently, the C_{GC} capacitance in the ohmic region is splitted between the drain and source electrodes (so that $C_{GS} = C_{GD} = ½C_{GC}+C_{GO}$). This is not the case in the saturated region, where the drain is separated from the channel (therefore $C_{GD} = 0$). Generally, we estimate $C_{GS} = 2/3C_{GC} + C_{GDO}$.

This situation is demonstrated in *Fig. 2.12*, where the capacitance distribution was drawn as a function of the V_{GS} and V_{DS} voltages (for N-MOS $W/L = 15\mu m / 5\ \mu m$). Here, we can see the 50% capacitance division between the source and drain. By focusing to the V_{DS} voltage, the transition between the saturation and ohmic region is visible as the decrease of capacitance above V_{DSsat}.

The drain and source electrodes create also the inversely polarized PN junctions (see *Fig. 2.10*), with barrier capacitance C_j given approximately by:

$$C_j = \frac{C_{j0} \cdot A}{\left(1 - \frac{V}{\Phi_B}\right)^{m_j}}, \quad \text{where} \quad C_{j0} = \sqrt{\frac{q_e \varepsilon_0 \varepsilon_{si} N_{SUB}}{2|\Phi_B|}}, \tag{2-34}$$

tel-00417838, version 1 - 17 Sep 2009

where C_{j0} is the surface zero voltage junction capacitance, Φ_B the intrinsic PN junction potential, A the effective junction surface and m_j the gradient coefficient of the junction. The PN junction exhibits a typical, decreasing capacitance vs. applied voltage tendency.

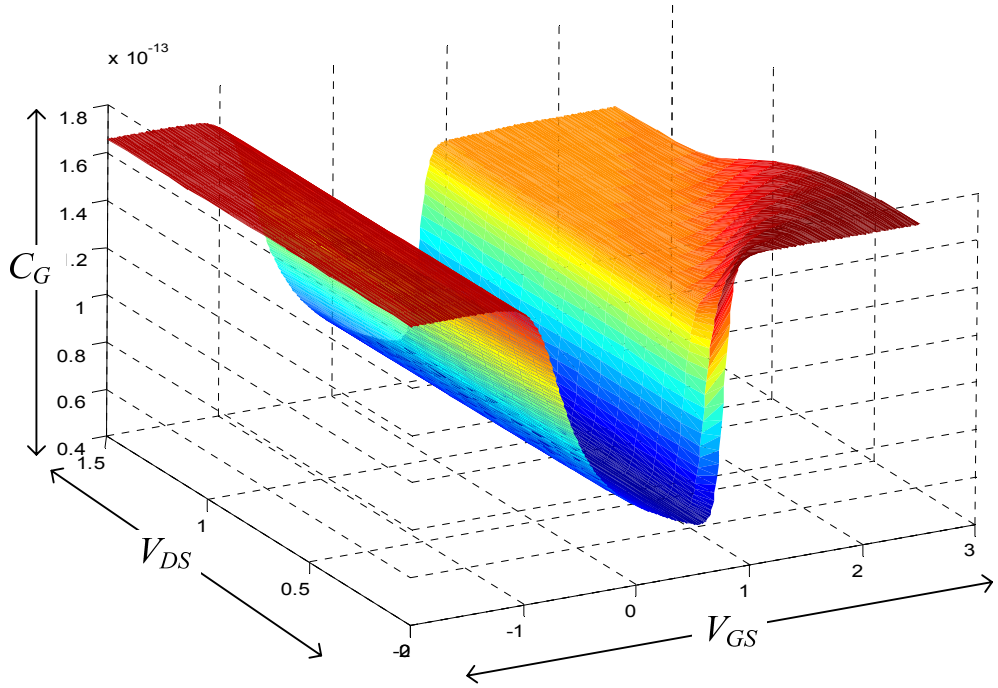


FIG. 2.12: *C-V characteristic of gate capacitance plotted as function of V_{GS} and V_{DS} showing the transition between the ohmic and saturation area (N-MOS 15µm/5µm)*

The contribution of all particular capacitances is collected in *Tab. 2.1* for various operating modes.

TAB 2.1: IMPACT OF PHYSICAL CAPACITIES TO THE TERMINAL CAPACITIES IN THE VARIOUS OPERATING AREAS

	WEAK INVERSION	**STRONG INVERSION** (LINEAR)	**STRONG INVERSION** (SATURATION)
C_{GD}	C_{ol}	$C_{GC}/2+C_{ol}$	C_{ol}
C_{GS}	C_{ol}	$C_{GC}/2+C_{ol}$	$^2/_3C_{GC}+C_{ol}$
C_{GB}	$C_{GC}\|\|C_{CB}$	0	0
C_{SB}	C_{jSB}	$C_{jSB}+C_{CB}/2$	$C_{jSB}+ {}^2/_3C_{CB}$
C_{DB}	C_{jDB}	$C_{jDB}+C_{CB}/2$	C_{jDB}

2.4.2 High Frequency Small Signal Model

To provide an analysis in the frequency domain, we need to construct a simple AC model of the transistor. This can be performed by including the parasitic capacitances *Fig. 2.10* into the static

tel-00417838, version 1 - 17 Sep 2009

model of transistor *Fig. 2.9*. *Fig. 2.13* shows such a model, where all nodal capacities *Fig. 2.10 a*) have been accounted for.

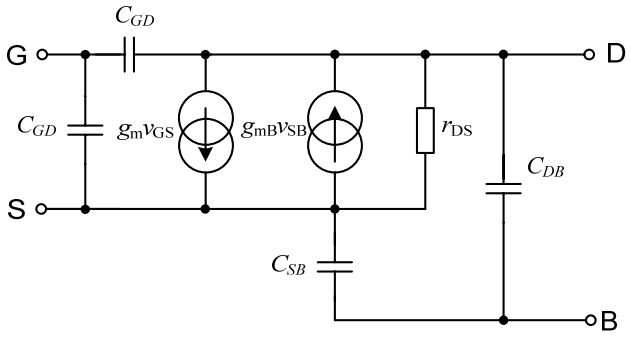


FIG. 2.13: *AC small signal model of the MOS transistor*

In many cases, we operate with the MOS transistor having the bulk and source terminal at equal potentials. In this case, the capacitances related to the bulk are shorted and model *Fig. 2.13* can be simplified as shown in *Fig. 2.14*.

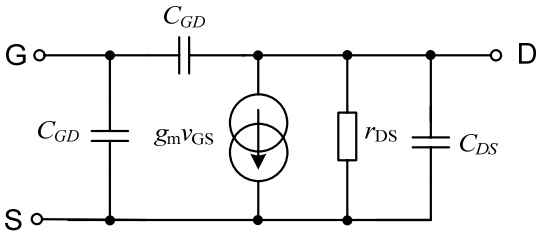


FIG. 2.14: *AC small signal model without substrate effect*

However, the complex evaluation of AC performances is relatively difficult and in practice is usually provided by the simulation with complex (high level) transistors model.

2.4.2 Small Scale Transistor Devices

The previously presented description of the transistor based on the "linear, gradual channel approximation" fits well for large scale devices (L, W > ~2 µm) [28]. Hence, this model can lead to some unexpected behaviour, as an infinite electrical field and infinite carrier velocity at the pinch-of region (see *sub-section 2.2.2*). However, new phenomena can occur due to the capability of recent technologies which approaches the quantum limits at nanometeric scale. In the following, we are going do describe the two most important effects occurring at low-scale devices: the carrier velocity saturation and the threshold voltage swing.

Carrier Mobility Saturation

The carrier velocity was shown in *Eq.* (2-1) to be a linear function of the electrical field. Hence, its value is limited by *scattering speed* v_{sat}, caused by collisions with the semiconductor crystalline lattice [22], [29]. A typical critical field E_{sat}, where carriers reach this speed are 10^4 *V*/cm and 5×10^5 *V*/cm for N-type and P-type silicon semiconductors, respectively. Therefore, the effect of carrier velocity saturation become more important for N-type MOS devices, and must be considered for a channel length L small enough as a few µm). In reality, the velocity saturation causes the *smoothing* of the pinched-off area and results in a thin electron channel where particles are carried towards the drain.

For a longitudinal electric field high enough so that induced carriers reach the velocity saturation, the drain current I_D remains almost constant and depends only on the depth of inducted channel. Naturally, this "depth" is controlled by the applied voltage V_{GS}.

tel-00417838, version 1 - 17 Sep 2009

In this case, the transistor enters in saturation with a voltage V_{DSEsat} lower, than the above considered V_{DSsat}. The definition of a "new" saturation voltage has to take into account the critical electrical field E_{sat} and is frequently provided by the following equation [23]:

$$V_{DSEsat} = \frac{V_{GS} - V_{TH}}{1 + \frac{V_{GS} - V_T}{L \cdot E_{sat}}}, \tag{2-35}$$

For E_{sat} exceeding the value $(V_{GS}-V_{TH})/L$, the saturation velocity voltage V_{DSEsat} can be simply deduced from the channel length as $V_{DSsat} = Lv_{sat}/\mu = L \cdot E_{sat}$. Consequently, the velocity saturation can be considered in *Eq.* (2-9) by replacing the term $(\mu dV/dx)$ by v_{sat}:

$$I_D = \frac{\mu_x C_{OX}}{2} W (V_{GS} - V_{TH}) \cdot E_{sat}. \tag{2-36}$$

In this equation, the current is no longer a quadratic function of the V_{GS} voltage. To demonstrate carrier velocity saturation, an example of the *I-V* characteristic has been plotted in *Fig. 2.15*. The characteristics correspond to a transistor (W/L=10/1µm N-MOS), where the operating conditions have allowed to reach both regimes of normal and carrier velocity saturation. In this figure, linear *vs.* quadratic dependence of the I_D *vs.* V_{GS}, as follows from *Eq.*(2-36) can be seen.

Similarly to the saturation area, the transconductance can be delivered in the velocity saturated transistor by $\delta I_D/\delta V_{GS}$:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{\mu_x C_{OX}}{2} W E_{sat}, \tag{2-37}$$

which is to be included in the small signal model of transistor *Fig. 2.13* (the nodal capacitances correspond to the normal saturation area).

A transistor operation in the velocity saturation mode is usually considered as inconvenient, because of low value g_m/I_D (see further the *section 2.4.3*). For the nowadays low dimension transistors, the value of maximum "current per width" is one of the important figures of merit. Its optimization can be performed *via* a choice of the process parameters, as using of very thin insulating (*e.g.* high-κ) dielectric, for instance.

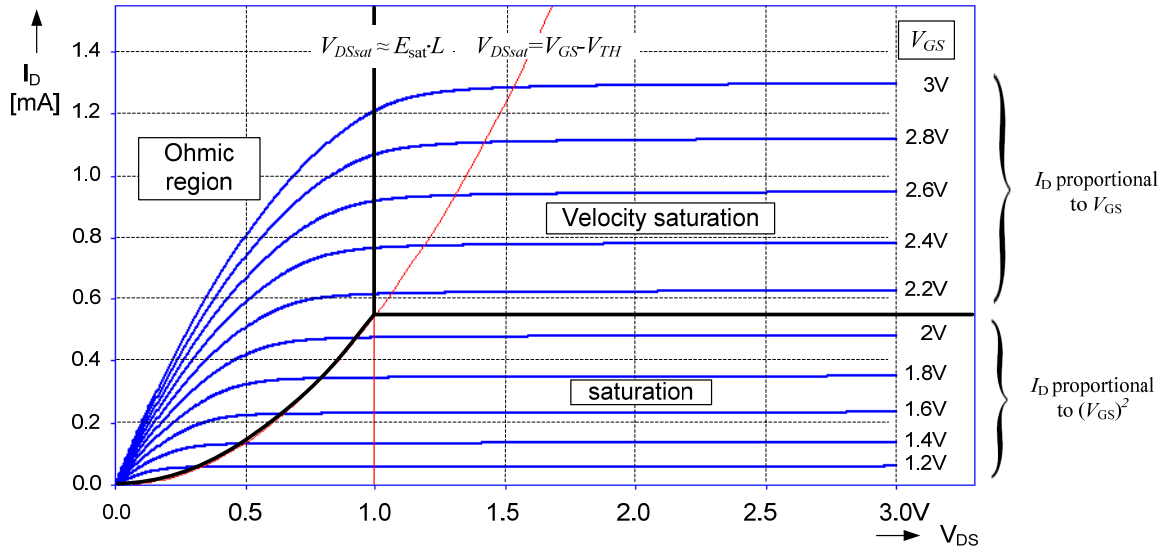


FIG. 2.15: *I-V characteristic of transistor in linear, saturated and velocity saturated regions (plotted for N-MOS 10 µm/1 µm)*

tel-00417838, version 1 - 17 Sep 2009

Threshold Voltage Swing

Another effect arising in the low dimension devices is the threshold voltage swing. This effect is linked to the charge distribution in transistor. The charge distribution varies with dimensions of drain and source depleted regions as well as when approaching the channel edges. A complex mathematical solution results in a 3D problem and it is usually included in the complex transistor models.

Generally, a short channel device (with a channel length comparable to the width of depleted region) results in lower threshold voltage. On the other hand, narrow channel devices have a slight V_{TH} voltage increasing dependence [29].

2.4.3 Figure of Merit of the MOS Transistor

Reaching the optimal performances of electrical circuits is naturally conditioned by the optimal choice of the CMOS process. It is common, for instance, to choose a process with lower V_{TH}, to provide a larger switching speed in digital circuits. On the contrary, from low V_{TH} can result an unwanted higher leakage in the switch-off state which is an important drawback for a low power design.

Each process (*e.g.* CMOS, BiCMOs) is characterised through key parameters, as the geometrical resolution, SiO_2 oxide thickness or doping concentration. In electronic design, we are interested to use rather "electrical" parameters such as *KP*, V_{TH}, or some specific parameters as further introduced g_m/I_D or parameters describing the maximal frequency range.

g_m over I_D

One of the frequently considered parameters of the MOS transistor is the transconductance efficiency. Generally, the performances of CMOS circuits (gain, transition speed) are improved by higher transconductance. Therefore, the transconductance related to the static drain current (*i.e.* power consumption), expressed as g_m/I_D is one of the fundamental figures of merit of the transistor. The curve $g_m/I_D=f(I_D)$ is almost the same for all transistors fabricated on the identical technological process. This feature would allow a simple comparison between different transistors with respect to goal application. Moreover it provides an interesting tool allowing the designer to get an optimal choice of transistor operating conditions.

An example of the $g_m/I_D=f(I_D)$ characteristic is plotted for N-MOS and P-MOS transistors (W/L=10 µm/1 µm) operating in all important areas (*e.g.* velocity saturation, saturation, and subthreshold), as shown in *Fig. 2.16.*

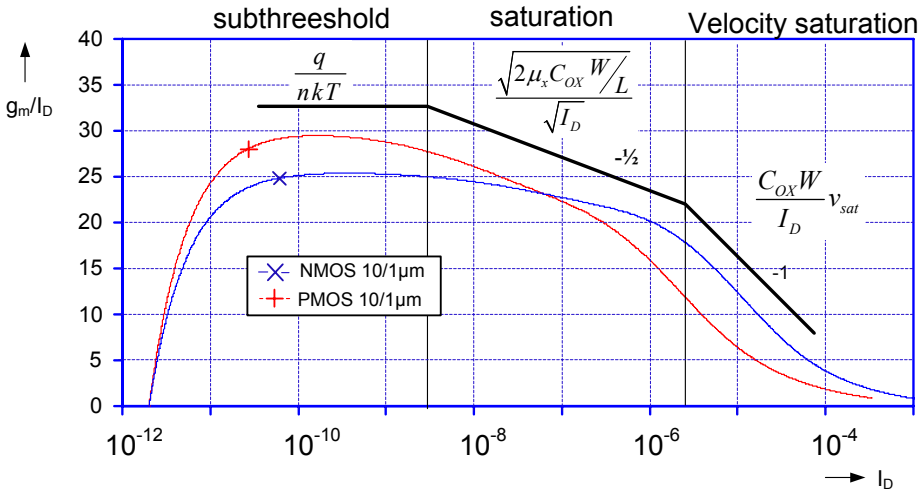


FIG. 2.16: *g_m/I_D characteristic of an N-MOS and P-MOS AMS 0.35µm transistor drawn from Spice-level 7 model*

tel-00417838, version 1 - 17 Sep 2009

Naturally, a high value of g_m/I_D is desired. It is interesting to notice that the higher value is reached in the subthreshold region, where the drain currents in the range of nA. This makes the subthreshold region very attractive for ultra low power applications. On the contrary, in the velocity saturation area we can observe a low g_m/I_D value, where, as already mentioned, the performances of the transistor are degraded.

The g_m/I_D characteristic is an interesting design tool important in particular for weak and moderate inversion. The use of g_m/I_D is a promising way to an accurate MOS transistor modelling. The main advantage of this model (such as EKV [32], [33]) is the fact that the transistor is considered as an integral element, where no "transition errors" between different regions are observed.

Frequency Figures of Merit

The high frequency performance is another important factor considered in the design of electronic circuits. However, it should be difficult to express the high frequency behaviour by a single parameter (number), as its value would differ for each particular configuration. We usually consider the frequency of *extrapolated unity current gain* ω_T of the transistor as the fundamental figure of merit. This current transfer can be expressed in common source configuration with grounded drain terminal as:

$$\left|\frac{i_D(\omega)}{i_G}\right| = \frac{g_m}{\omega(C_{GD}+C_{GS})}. \tag{2-38}$$

Here, the gate current i_G (ideally zero for DC) is only due to the C_{GD} and C_{GS} capacitances. However, we can notice, that the large capacitance C_{DB} is not considered in this transfer function. This equation (2-38) allows to find the extrapolated unity current gain frequency ω_T:

$$\omega_T = \frac{g_m}{C_{DG}+C_{GS}}, \tag{2-39}$$

where, as shown in *sub-section 2.4.1,* a sum of capacitances has to be considered for a given operating point. To reach the optimal high frequency behaviour, various optimisation tools can be used. For instance, it is advantageous to consider the g_m/I_D characteristic or make use of an analytical description as shown in *section 6.1.1* (see *Eq.*(6-5)).

The value of ω_T can be expressed as a function of transistors' parameters (μC_{OX}) and channel dimension W and L. As shown in *Tab. 2.1*, the C_{GS} gate-source capacitance is dominating in the saturation mode. In this way, the ω_T of a saturated transistor can be written as:

$$\omega_T \approx \frac{g_m}{C_{GS}} = \frac{\mu_x C_{OX}\frac{W}{L}(V_{GS}-V_{TH})}{\frac{2}{3}C_{OX}W\cdot L} = \frac{3}{2}\frac{\mu_x(V_{GS}-V_{TH})}{L^2}. \tag{2-40}$$

and similarly, in the velocity saturated mode:

$$\omega_T \approx \frac{g_m}{C_{GS}} = \frac{\mu_x C_{OX} W E_{SAT}}{\frac{2}{3}WLC_{OX}} = \frac{3}{4}\frac{\mu_x E_{SAT}}{L}, \tag{2-41}$$

reaching lower ω_T frequencies compared to a transistor in the normal saturation mode. Naturally, the correct evaluation should be based on more accurate models, *e.g.* including the gate access resistance r_g or previously mentioned C_{GD} capacitance for instance.

tel-00417838, version 1 - 17 Sep 2009

2.5 Basic process parameters

The selected process ASM 0.35µm 5V is a standard CMOS process with 4 interconnection layers and a maximum supply voltage of 5.5 V. This technology allows integration of all basics components, as the MOS transistors, capacitors and resistors. The cross-section is shown in *Fig. 2.17*. Basic parameters characterising the N-type and P-type transistors are collected in *Tab. 2.2*.

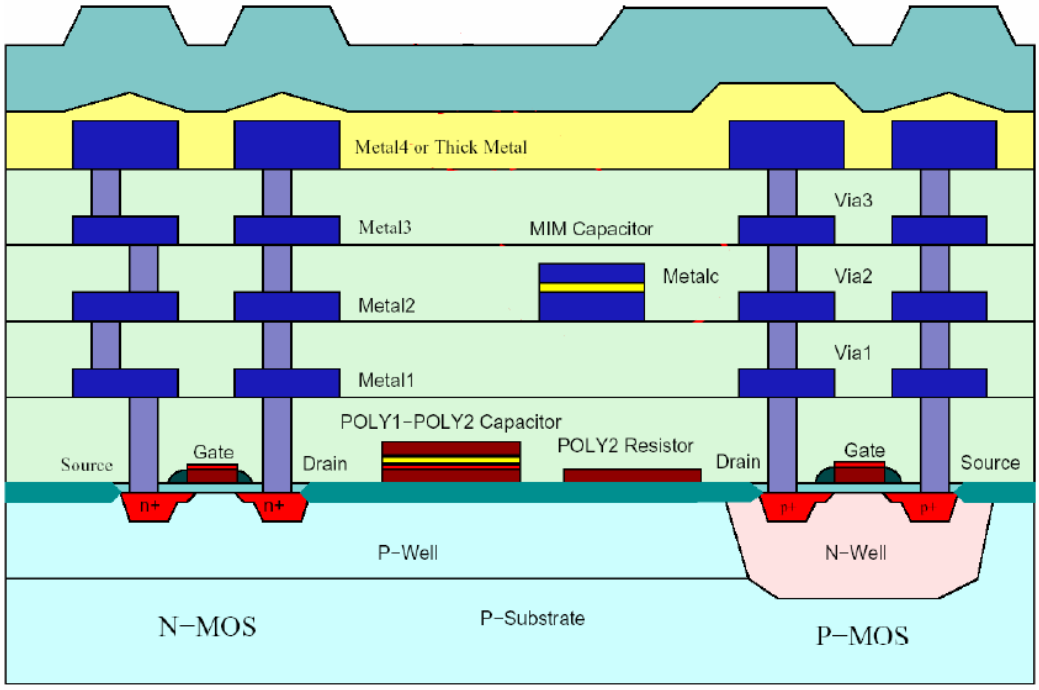


FIG. 2.17*: Cross section of the AMS 0.35µm process*

In reality, any CMOS process has a large dispersion of process parameters. However, the tolerance remains constant for a given process run. This is an important feature resulting in almost perfect devices matching in a range well below 1%.

TAB 2.2: KEY PARAMETERS FOR AMS 0.35µm 5 V PROCESS (ε_0=8.85×10^{-12} F/m)

PARAMETER	N-MOS	P-MOS	UNIT
V_{TH}	0.7	-0.9	V
γ	1	-0.65	√V
KP	100	32	µA/V^2
μ	450	135	cm^2/Vs
t_{ox}	15	15	nm
N_{sub}	160	70	10^{15}/cm^3
dV_{TH}/dT	-1.5	2.1	mV/K
ε_{OX}	3.9	3.9	-

2.6 Trends in CMOS development

Nowadays, we find many different research ways in the domain of microelectronics. We can mention for instance the area concerning the *technological research* allowing the integration of nanometeric components, or the *applied research* integrating such recent devices in the industrial applications.

tel-00417838, version 1 - 17 Sep 2009

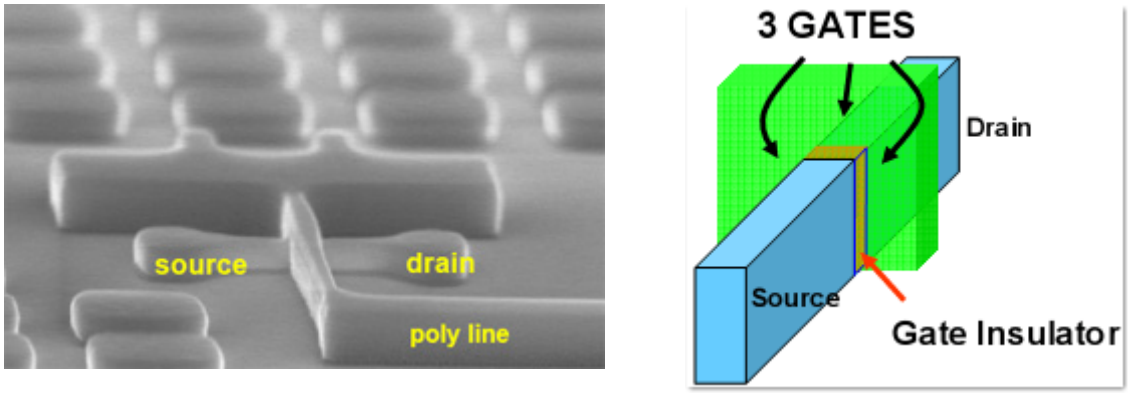
Generally, the research is split between the analog and digital circuits. This is caused by different objectives, where for instance the digital circuits require very small devices allowing high density integration, whereas the analog circuits can be based on larger transistors, which are advantageous with respect to the power consumption or noise.

In the following, we are briefly introducing two representative domains in the micro/nano electronic research: *ultra low scale CMOS* devices and *single electron transistors*.

2.6.1 Very Low Dimension Transistors

The impacts of recent technologies allow to scale the channel length of silicon transistor down to some tens of nm. This should approach the physical limits of classical planar CMOS devices.

Fig. 2.18 shows an example of a 45nm MOS transistor *TriGate*, fabricated by Intel [34]. As we can see in *Fig. 2.18 b*), this transistor has the drain current controlled by the "3D" gate, surrounding the channel. This provides better control of channel conductivity (expressed by ratio of on/off currents). The relatively good performances are reached by using of a special strained silicon, *high-κ* dielectric (~3nm) and metallic high conductivity gate electrode.



a) *b*)

FIG. 2.18: *45nm Intel TriGate transistor, a) AFM image; b) schematic design [34]*

Devices with size below ~10 nm no longer behave as classical MOS transistors based on the drift-diffusion theory. In these devices, the electron mean free path is equal or lower than the mean length between two electron collisions with crystalline lattice. The current transfer is described by the quantum transport theory and by quantum effects (tunnelling). The most important effect controlling the drain to source current is the ballistic/quasi-ballistic transport and source-to-drain (S/D) tunnelling.

The ballistic transport is linked to the mean free path (λ), which dominates devices shrieked down to 10 nm. The transport theory [28] defines the drain current of a low dimension transistor as:

$$I_D = \frac{\lambda}{L+\lambda} W Q_i \frac{v_T}{2k_B T} V_{DS}. \qquad (2\text{-}42)$$

In this Equation, Q_i is a channel charge, L the length of the channel and v_T the electron scattering velocity. The mobility of carriers in the semiconductor can be generally expressed as $\mu = v_T\lambda/(2k_BT)$, which can be compared with (2-9). Here, for $L > \lambda$ both expressions (2-9) and (2-42) become equivalent.

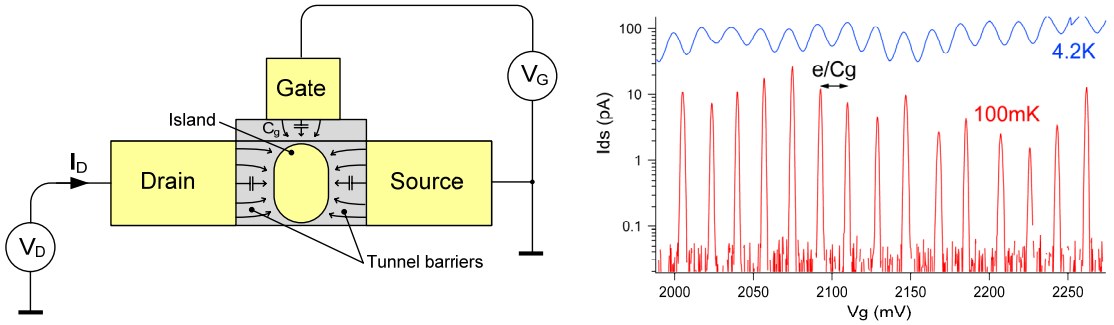
On the contrary, the source/drain tunnelling imposes the fundamental gate length limits, caused by leakage current in the off-state. It is estimated that the fundamental device length is limited to some 5 nm, where the I_{ON}/I_{OFF} current ratio reaches a value around 100.

tel-00417838, version 1 - 17 Sep 2009

2.6.2 Single Electron Transistor

A device of the size of the atomic scale is completely dominated by the quantum effects. A single electron transistor (SET) is the nanoscale quantum transistor based on the *Coulomb Blockade* [36]. The coulomb blockade is the effect allowing to control the electron tunnelling *via* the potential difference between the electrodes

In the SET, the drain current is, similarly to the classical MOS transistor, controlled by the gate voltage. *Fig. 2.19 a*) shows a physical setup of the SET, which consists of an isolated metallic electrode (*island*), separated from the drain and source by two tunnel junctions. The gate electrode is



a) *b)*

FIG. 2.19: *Single Electron Transistor (SET) a) structure with two tunnel junctions, b) drain current periodicity with island charge [36]*

capacitively coupled to the "island" *via* a very small capacitance C_g. The charge of this capacitor allows to control the resulting drain-to-source current.

The potential of the island can be controlled by the applied gate voltage V_G. If we consider the C_g capacitance (of very low value) with charge $n \cdot q$, the resulting potential can reach only the discrete values $V = n \cdot e/C_g$. The drain current is consequently controlled by this discrete potential and results in a periodical I_{DS} versus V_G *I-V* characteristic (as a new electron is added/removed from the isolated region - see *Fig. 2.19 b*).

To provide a correct function of the transistor, the energy qV has to be large compared to the thermal energy of the electron k_BT. This requires either an island size about one nanometer (almost one atom dimension), or very low temperature (cryogenic) operation in the m*K* range.

We can notice that the transistor operates with ultra low drain current as well as with high access resistance (source, drain). This latter, in fact, make a subject of discussion about the usefulness of such a transistor in integrated electronic devices. Nevertheless, we can find some experimental circuits based on the described coulomb blockade in [37], for instance.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

3 NOISE IN ELECTRONIC CIRCUITS

3.1 Noise in Electronic Circuits

Electrical noise is an unwanted signal unavoidably imposing a sensitivity limit to any electronic circuit. The presence of noise can have many origins, such as microscopic fluctuations in matter or variations of system conditions (*e.g.* temperature). The unpredictable, random nature of noise does not allow its simple removal from the signal path. However, correct circuit design and advanced signal processing, along with the use of recent, ultra-low noise devices, allows approaching the quantum limits imposed by the front-end physical sensors.

In this chapter, we briefly introduce basic elements being responsible for the noise and introduce the relationships between the parameters of components and generated noise. These relationships would present a fundamental background in the next design of low noise amplifiers.

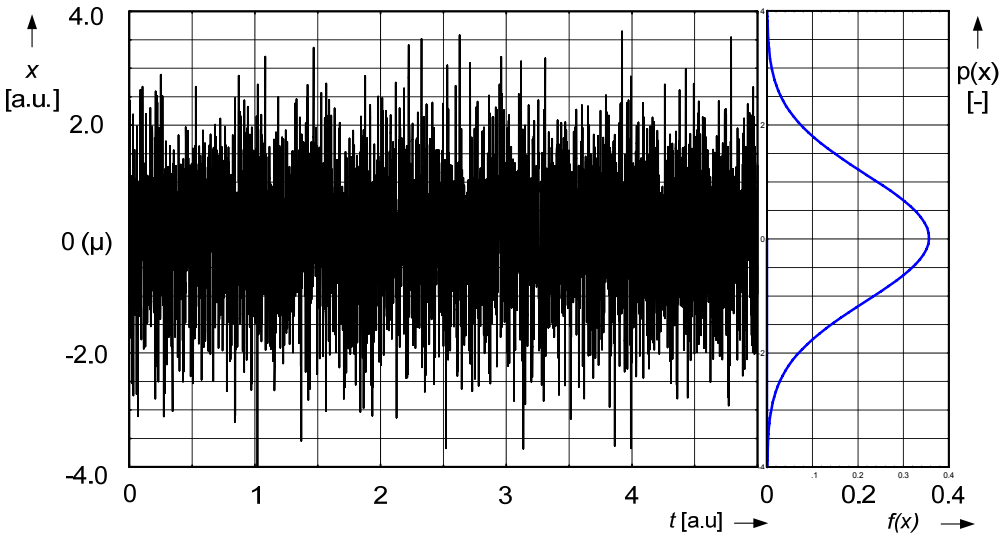


FIG. 3.1: *Generated sequence of noise with Gaussian distribution*

3.1.1 The Random Nature of Noise

Each electronic component contains one or several uncorrelated noise sources. These so-called "stochastic" sources can be quantified by a statistical mathematical description [39], [40]. The most important characteristics are the amplitude distributions in time and in frequency domains.

Fig. 3.1 shows an example of generated noise sequence (left) and its distribution function (right), giving the probability of the signal to have a specific value inside a [V_{MIN}, V_{MAX}] range. The most frequently used distribution is the "*Gaussian distribution*" characterized by its *mean* value μ and its *standard deviation* σ, given as:

$$p(x) = \frac{1}{\sigma\sqrt{2\pi}} e^{-\left[\frac{(x-\mu)^2}{2\sigma}\right]}. \tag{3-1}$$

The $p(x)dx$ is the probability of a measurement to have a value within the range [x ; x+dx]. The distribution *mean* is the arithmetic average value of the stochastic (noise) signal and is sometimes referred to the DC voltage. Its value can be calculated for any continuous random process in a given time interval T as:

$$\overline{v} = \frac{1}{T}\int_0^T v_{(t)}dt\,, \tag{3-2}$$

Ideally, we take $T \to \infty$. The *standard deviation* σ is defined as the square root of the variance, which derives from the squared differences between data points and the mean value μ. The natural characteristic of any probability distribution (*e.g.* Gaussian) is the unity surface below the curve:

$$\int_{-\infty}^{\infty} p(x)dx = 1. \tag{3-3}$$

The quantification of the noise in terms of electrical voltage (current) can be done by using a classical *Root-Mean-Square RMS* value. A noise signal can be characterized by a continuous voltage of value V_{RMS}, defined as voltage having an equivalent heating effect as the noise signal. The RMS value of an alternating signal $v(t)$ is defined as:

$$V_{RMS} = \sqrt{\frac{1}{T_P}\int_0^{T_P} V^2(t)dt}\,, \tag{3-4}$$

where T_P is the observation time, which should be ideally equal to one period or to infinity (for a stochastic signal). The values of V_{RMS} and standard deviation allow estimating a maximum peak voltage. For instance, for a typical $\sigma \sim 3$ the noise will remain within the interval [-6·V_{RMS},+6·V_{RMS}] in 99.7% of time.

As will be shown in following, noise analysis dealing with uncorrelated signals uses methods differing from these used in the analysis of linear circuits. This is primarily due to the invalidity of the superposition principle. Usually, we operate with the squared values (voltages and currents, *i.e.* v^2_n and i^2_n), which in fact correspond to the noise powers.

Another important parameter of the noise is its frequency distribution (spectrum). Contrarily to periodic signals, spectral characterization of stochastic process cannot be provided by classical Fourier series. It is evident that for such a signal, the phase (for instance) cannot be defined. To describe the noise (voltage, current, power) distribution in the frequency domain, spectral density values (voltage $v_n(\omega)$, current $i_n(\omega)$, and power $G_n(\omega)$ respectively) are defined as the "amount" of the signal per unit of bandwidth (Hz).

tel-00417838, version 1 - 17 Sep 2009

3.2 Noise Sources in Electronic Systems

Noise can have many origins and is omnipresent in almost all physical processes. However, some noise sources are usually dominant, and therefore need prior investigation. Each noise source has a major dependence on some parameter such as the value of a resistance, the temperature, or operating frequency range, for instance. The understanding to these basic parameters can play an important role in the noise optimization of electronic circuits.

3.2.1 Thermal Noise

Thermal noise is one of the fundamental noises in electronic circuits. It is also called *Johnson* or *Nyquist* noise. The origin of thermal noise can be found in the thermal agitation of electrons and phonons in the conductor. This agitation is due to the thermal energy k_BT. The collision of electrons with the crystal lattice induces a local variation of the charge, which is revealed by the presence of a noise current or voltage on the conductor terminals. The noise power available in any conductor is defined by the Johnson formula:

$$P_N = k_B T \Delta f \,, \tag{3-5}$$

where k is the *Boltzmann constant* (1.380×10^{-23} J·K^{-1}), T the absolute temperature in kelvin and Δf the (effective) noise bandwidth where the noise power is measured. The thermal noise is characterized by a constant spectral density ideally through the whole frequency spectrum. The noise with such spectral distribution is frequently referred to as *white noise*. However, taking an infinite frequency bandwidth Δf, the total noise power defined by (3-5) would seem to diverge into infinity. In reality, this bandwidth is limited and remains constant only until k_BT is much lower than hf [*] [42].

The thermal noise defines the fundamental limits in electronic circuits. For instance, *Eq.*(3-5) can be used to express a *noise floor* of the electronic circuits operating at room temperature, being -174 dBm/Hz (dBm is the decibel referenced to 1 mW).

Noise current and voltage: the noise power available in a conductor can be expressed in terms of a noise voltage and current, through its intrinsic resistance. Thermal noise voltage and current can be determined for maximum power transferred towards the load resistance R_L. For matched source and load resistances $R = R_L$, the transferred power can be obtained as:

$$P_N = \frac{v_n^2}{4R} = kT\Delta f \,, \tag{3-6}$$

The resulting RMS voltage v_n at the resistor contacts measured within a limited bandwidth Δf is :

$$v_n = \sqrt{4kTR\Delta f} \,, \tag{3-7}$$

expressed in $V/Hz^{-½}$ or n$V/Hz^{-½}$. Similarly, we can define the noise current generated by the resistor R:

$$i_n = \sqrt{\frac{4kT\Delta f}{R}} \,, \tag{3-8}$$

[*] In fact, the spectral distribution of thermal noise is given by Plank's Law. The total noise power available in the conductor can be expressed by integral of its frequency spectrum:

$$\overline{P} = \int_0^\infty \frac{h\nu}{e^{\left(\frac{h\nu}{kT}\right)} - 1} d\nu \,,$$

which leads to the total power of 4.10^8 W at T = 290 K

tel-00417838, version 1 - 17 Sep 2009

in A or n$A/Hz^{-½}$. In practice, calculations commonly consider the squared noise voltages (currents), equivalent to the noise power and expressed in V^2/Hz and A^2/Hz, respectively:

$$\overline{v_n^2} = 4kTR\Delta f \quad \text{and} \quad \overline{i_n^2} = 4kT\Delta f / R\,, \tag{3-9}$$

The presence of Johnson noise can raise a question about the origin of such a power. We can show that for devices in thermal equilibrium, the power transfer between two resistive elements is balanced (*i.e.* no power is entering nor generated by the system). We can demonstrate such equilibrium by a simple (idealized) experiment.

We can imagine two resistances R_1 and R_2 with identical values, placed into ideal calorimeters and interconnected by a virtual (noiseless and zero thermal conductivity) transmission line. At $t = 0$, the first resistor is at room temperature T_1 and second one at a lower temperature T_2 (*Fig. 3.2*).

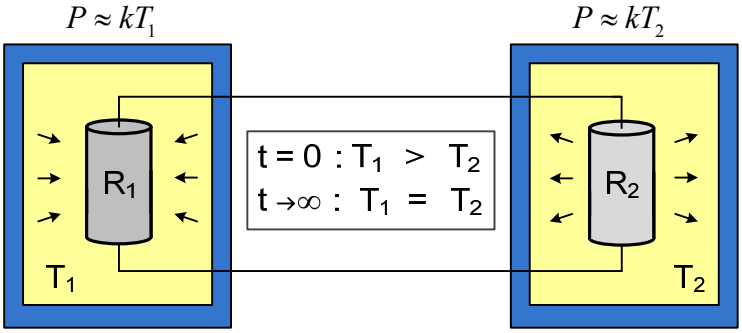


FIG. 3.2: *Demonstration of noise power transfer between two resistors maintained at different temperatures*

At $t = 0$, both resistances generate powers P_1 and P_2, where $P_1 > P_2$. The transmission line enables the power flow between these two resistances. We can deduce that for $t \to \infty$, both temperatures become equal, and the system reaches the thermal equilibrium. In this way, the resistance thermal noise can be assimilated to the one-dimensional radiation of black-body objects.

3.2.2 The 1/f$^{\alpha}$ Low Frequency Noise

The spectral density of noise can exhibit many forms, given by the noise sources and the frequency transfer characteristic of the amplifier. The $1/f$ noise is characterized by a spectral density increase at lower frequencies. We define the coefficient α as a slope of noise power spectrum in a logarithmic scale (we consider typically $\alpha = 1$) [39], [43], [44]. The $1/f$ noise can have many origins, and exists in almost all physical systems: from electronic devices as resistors, diodes or transistors, to non-electric ones as road traffic distribution, for instance.

$1/f$ noise, also referred as flicker noise is associated to a current flow in electronic device. Its current spectral density can be written in following form:

$$i_{n,f}^2 \equiv K \cdot \frac{I_{DC}^{\beta}}{f^{\alpha}} df\,, \tag{3-10}$$

where I_{DC} is the device quiescent current, K a constant characterizing the device, α the slope considered above and β a specific constant close to unity. We can note that, in real devices, the value of K is usually inversely proportional to the *effective device surface*. The *RMS* voltage at the resistance R resulting from integration between two frequencies f_L and f_H, can be written as:

$$v_{n,f}^2 = K \cdot R \int_{f_L}^{f_H} \frac{I_{DC}^{\beta}}{f^{\alpha}} df \overset{(\alpha=1)}{=} K \cdot R \ln\left(\frac{f_H}{f_L}\right), \tag{3-11}$$

tel-00417838, version 1 - 17 Sep 2009

As opposed to white noise, the amount of signal remains constant over a frequency decade (for $\alpha = 1$), which means for instance, that the integrated noise power is equal within the 0.1 - 1 Hz and 10 – 100 Hz frequency span.

The asymptotic nature of the spectrum can raise the questions about its limit at nearly zero or infinite frequencies. At higher frequencies, the noise is dominated by the thermal noise. The characteristic frequency at which the thermal and 1/*f* noise levels are equal is called "*corner*", or *corner frequency* f_C (*Fig. 3.3.*).

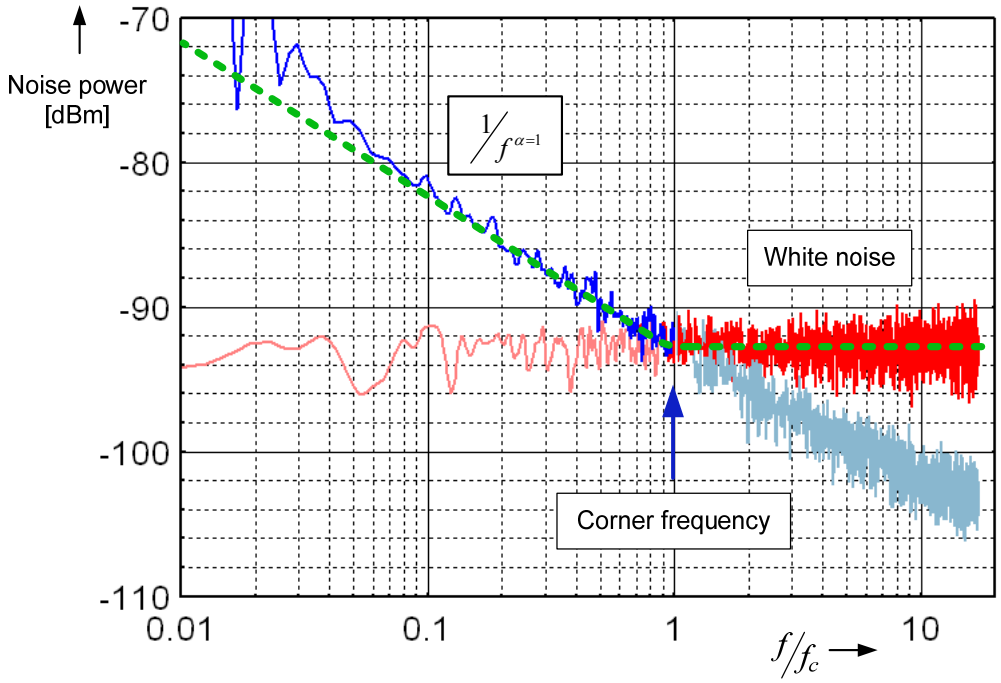


FIG. 3.3: *Power spectral density (PSD) of generated white and 1/f noise sequences*

On the contrary, the flicker noise diverges at low frequency (DC) (see *Eq.*(3-11)). Obviously, this concept is unrealistic. Defining the mean value *Eq.*(3-2), we can mathematically avoid such divergence. Usually, the DC value of noise can be set to zero (as in *Fig. 3.1*), which causes the noise spectrum to naturally fall down at zero frequency. Alternatively, we can attribute the DC component of the flicker noise to the offset voltage of an amplifier.

The physical origins of the 1/*f* noise are still a current research topic, particularly in recent low scale physics and quantum electronics. Suppression of this noise can improve the performances of low scale electrical components, where the *1/f* noise is naturally enhanced. Generally, the origins of *1/f* noise are sought as consequences of materials' inhomogeneity. A_most critical point for electronic devices concerns the interface (surface), where impurity concentration is dominating (as is the case for the channel and SiO_2 barrier interface of a MOS transistor). The amplitude distribution of the 1/*f* noise is often non-Gaussian.

3.2.3 Shot Noise

This noise is due the discreteness of the electrical current and occurs as a consequence of charges recombination in a potential barrier (like PN junction). Similarly to the *1/f* noise, its value depends on the current flow, as it can be seen on the expression of the shot noise:

$$\overline{i_n} = \sqrt{2qI_{DC}\Delta f}\ , \qquad (3\text{-}12)$$

tel-00417838, version 1 - 17 Sep 2009

where q is the elementary charge. This definition is valid as long as the upper frequency of Δf becomes comparable to $1/\tau$, where τ is the charge transit time through the barrier. For this reason, its spectral density is white (and Gaussian) only up to this frequency $1/\tau$.

On the contrary, shot noise is not present (or exhibits a very low value) in conductors, because there is no potential barrier and the motion of electrons are correlated.

3.2.4 Non-Electrical Noise Sources

Random noise signals can arise as well, from fluctuations in the environmental conditions. This interaction can be limited by a correct design, for instance by a good shielding of the circuit. A most common external perturbation is the electromagnetic radiation caused by natural electromagnetic signals (atmospheric noise) or being the consequence of human activity. This latter may arise from 50/60 Hz power lines or radio station signals, for instance.

There are also non-electrical effects which should be considered as noise: the ambient temperature variation which affects the device parameters, acoustical noise related to the well-known "*microphonic effects*", high energy (ionizing) particles (*e.g.* cosmic radiations), or the components' aging.

3.3 Noise Analysis, Basic Noise Characteristics

An electrical circuit contains many different electrical parts, each having its own noise contribution. However, instead of a complex description including all these elements, we aim to characterize the system as an integral block. Such a characterization can be provided by relevant parameters: *Signal-to-Noise Ratio* SNR, *Noise Figure* NF and *noise temperature* T_n [40], [41].

3.3.1 Signal to Noise Ratio SNR

The amount of the noise (present in any electrical system) can be evaluated by comparing both noise and signal powers. This ratio can be expressed in dB by the SNR:

$$SNR = 10\log_{10}\left(\frac{p_s}{p_n}\right) = 10\log_{10}\left(\frac{v_s^2}{v_n^2}\right), \tag{3-13}$$

where p_s and v_s refer to the signal and p_n and v_n to the noise, respectively. As we have shown above, the effective noise power increases with the effective noise bandwidth Δf. It follows that the value of SNR has to be defined for any specific (given) frequency range. The SNR ratio can be used to define the so called "*Noise Equivalent Power NEP*" as the equivalent signal power per unit bandwidth, where the SNR is equal to unity. This NEP is considered as the minimally detectable signal level.

3.3.2 Noise Figure NF

We have defined the SNR ratio characterizing the noise properties of the signal. On the contrary, noise figure is the factor detailing the noise properties of an amplifier. The noise figure is defined as the *SNR* degradation caused by amplifier and is one of fundamental figure of merit. Comparing both input and output *SNR* values gives directly the NF in dB:

$$NF = SNR_{IN} - SNR_{OUT}, \tag{3-14}$$

and being above 0dB (if the bandwidth is not reduced in the amplifier). We can now consider the amplifier connected to the signal source of internal resistance R_S, where the output signal is only

tel-00417838, version 1 - 17 Sep 2009

thermal noise. The noise figure can be defined by amplifier noise v^2_a which is referred to the R_S input thermal noise:

$$NF = 10\log_{10}\left(\frac{4kTR_S + v_a^2}{4kTR_S}\right). \tag{3-15}$$

Naturally, we wish to make the NF as low as possible. The (3-15) shows the NF decreasing by the increase of the source's resistance R_S. In this case, the low NF is caused by the high SNR_{IN} (*i.e.* amplifier noise is not significant as compared to the high input SNR). It follows that in real systems, we must try to push the source resistance R_S at the lower possible level (if a current is to be amplified, we do the opposite). Hence, in some cases, this method must be re-viewed: In the case of detectors, for instance, where the detectivity increases faster (with increasing resistance) than thermal noise (see *subsection 4.2.1*).

3.3.3 Noise Temperature

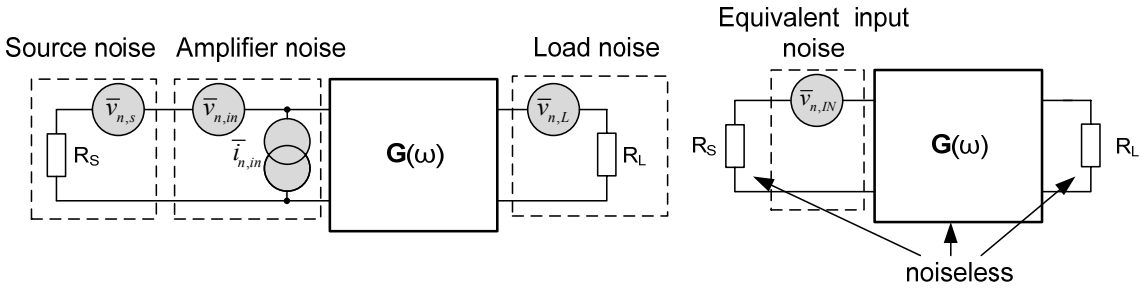
Another way to describe the noise properties of an amplifier is to use the *noise temperature* T_N. Its value is determined as the equivalent temperature of a resistive source for which the input SNR reaches identical level as the amplifier output SNR. We can figure a noisy amplifier amplifying signal with no noise (generated by source resistance R_S at T = 0 K). In this case, only the amplifier noise is present at the output. Now, any ideal noise-free amplifier is connected to a real noise source (with identical R_s value). The original amplifier noise value is reached at the source - having temperature T_N - in fact being equal to noise temperature. The noise temperature can be obtained from the NF as:

$$T_N = T(10^{NF/10} - 1). \tag{3-16}$$

Typically, the T_N value of any good amplifier must be significantly lower than the ambient temperature, which means that the noise produced by the amplifier itself is lower than the noise delivered by the sensor.

3.3.4 Equivalent Input Noise Voltage: v_n-i_n Noise Model

The purpose of the noise model using the equivalent input noise voltage is to provide a simple tool allowing the replacement of all noisy elements in the circuits by a unique noisy element: *equivalent noise source*. This noise source includes the contribution of all components in the circuits. It is usually connected to the input, close to the signal source. This allows to compare both noise and signal amplitudes. Since this noise source is placed at the input, it is named as "*equivalent input noise source*".



a) *b*)

FIG. 3.4: *Construction of an equivalent input noise voltage source*

tel-00417838, version 1 - 17 Sep 2009

We can consider an simple signal chain composed of the signal source with input resistance R_S, high input impedance amplifier (with gain $G(\omega)$) and load resistance R_L. This is schematically shown in *Fig. 3.4*.

We typically consider two noise generators: noise provided by signal source (Johnson noise), and amplifier noise voltage and current (v_n-i_n). Measurements of (v_n-i_n) values can be provided by the measurements of output noise with amplifier having: *i*) shorted input and *ii*) input connected to a high impedance source. The measured output noise voltage can be then referred to the input by simply dividing by the voltage gain G_v. In real amplifier, the two noise sources ($v_{n,in}$ - $i_{n,in}$) are closely correlated (depended, C ≈ 1 ; see *section 3.4.5*) as both are generated in the same structure. However, correlation can significantly complicate the calculation. For a given value of source resistance, the sources form *Fig. 3.4 a*) can be replaced by a unique noise voltage source $v^2_{n,IN}$ ($v_{n,in}$ - $i_{n,in}$ considered uncorrelated):

$$v^2_{n,IN} = v^2_{n,s} + v^2_{n,in} + R^2_s i^2_{n,in}\,, \tag{3-17}$$

expressed usually in the PSD or RMS voltage. This noise source further allows to consider the amplifier as noiseless. As mentioned above, the equivalent input noise can be determined from the measured output noise, divided by the voltage gain $G(\omega)$:

$$v^2_{n,in}(\omega) = \frac{v^2_{n,out}(\omega)}{G^2(\omega)}\,. \tag{3-18}$$

The analysis based on the equivalent v_n - i_n noise model is a general technique valid for all types of amplifiers or active devices. Its consideration is important for the choice of the amplifier with respect to the signal source impedance (*e.g.* fabricated in bipolar or CMOS process).

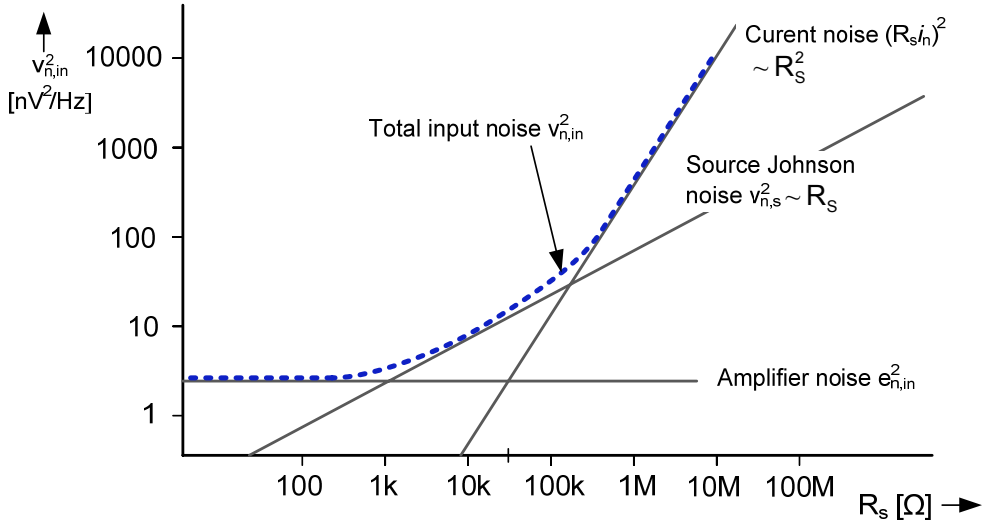


FIG. 3.5: *Equivalent input noise voltage of bipolar transistor as a function of input resistance R_S*

To demonstrate the dependence of the input noise on the source resistance, we can consider two limiting cases *i)* when the amplifier is connected to a signal source with zero resistance (*i.e.* a transformer) or *ii)* to a source with a very high resistance. In the first case, the short-circuit eliminates the contribution of the current source $i_{n,in}$, and only the noise voltage source is dominant. In the second case, however, even a low current $i_{n,in}$ causes an excessive noise voltage across r_s , which increases the total amplifier noise. This dependence is plotted in *Fig. 3.5*, where the total input noise v_{in} increases with the source resistance, following *Eq.*(3-17). Here, the first line (amplifier noise $e_{n,in}$) shows a constant noise voltage. The thermal noise of source resistance is

tel-00417838, version 1 - 17 Sep 2009

proportional both to r_s (with slope 1/2), and to the $i_{n,in} \cdot R_S$ product (3-17), corresponding to a drop of noise current on the source resistance.

3.3.5 Correlation

Correlation provides a measurement of the association between two signals. When two signals have an identical shape (but not necessary the same amplitude), we say that these signals are *correlated*. Typical examples of correlated signals are two DC voltages or two sinusoidal signals with identical frequencies. The correlation is characterized by a *correlation coefficient C*:

$$C(\tau) = \lim_{T\to\infty} \int_0^T v_{n,1}(t) v_{n,2}(t-\tau) dt \,. \tag{3-19}$$

This coefficient reaches unity for identical signals. On the contrary, noise signals produced by two independent sources are considered as uncorrelated ($C = 0$). A typical property for operations with correlation is whether superposition is valid or not. Superposition of uncorrelated signals has to be done *via* the sum of their *squared RMS values*, corresponding to the sum of their powers. The general expression can be written for two time signals $v_{n,1}(t)$ and $v_{n,2}(t)$ as:

$$v_n^2 = \lim_{T\to\infty} \frac{1}{T} \int_0^T \left(v_{n,1}(t) + v_{n,2}(t) \right)^2 dt = v_{n,1}^2 + v_{n,2}^2 + 2C v_{n,1} v_{n,2} \,. \tag{3-20}$$

As we already mentioned, the correlation may complicate the calculations. For instance, the nonzero value of C results in an additional term $2 \cdot C \cdot v_{n,in} i_{n,in} R_S$ in *Eq.*(3-17). This can be included in *Fig. 3.4* noise model as the additional noise (current or voltage) generator.

3.4 Noise in the MOS Transistors

The noise in a MOS transistor is mainly caused by the channel noise. The principal difference compared to BJT transistor is the lack of shot noise (important only in the subthreshold region). The hand-made calculation usually deals with an equivalent input model v_{in}-i_{in} (*Fig. 3.4*), or directly with drain noise i_{nD}, as shown in *Fig. 3.6*.

Figure 3.8 shows only a single noise source i_{nD}, covering all noise sources of the transistor. More accurate noise models, such as the models used in specialized software (CAD), deal with other noise sources, such as the substrate noise, or RTS (Random Telegraph Signal noise). These sources are well discussed in the available literature [45], [46], [47].

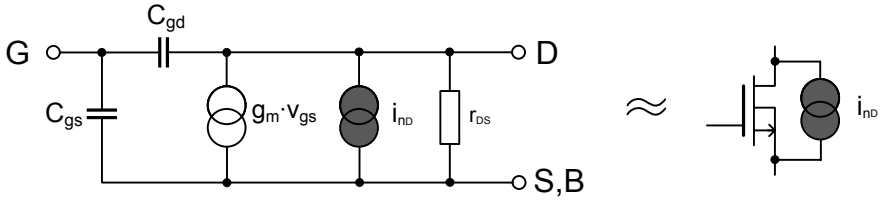


FIG. 3.6: *Simplified small signal noise model of the MOS transistor*

Thermal Noise

Thermal noise of a MOS transistor is caused by the drain-to-source channel resistance. We have shown in the previous chapter that this resistance is directly $1/g_m$ in the ohmic region. In the saturation area, we consider that the noise is reduced by an empiric constant ~ 2/3 [22]. By accounting this constant, the drain noise current in the saturation region can be expressed by (3-8) as:

tel-00417838, version 1 - 17 Sep 2009

$$i_{n,D}^2 \cong \frac{8}{3} kTg_m . \tag{3-21}$$

The equivalent input noise voltage $v_{n,\text{in}}$ of the MOS transistor can be found by dividing $i_{\text{n,D}}$ by the gate transconductance g_{m}. The equation (3-21) shows the relationship between the drain noise current and the operating point (resulting from W/L, I_{D} etc.), which is an important criterion for the following design.

Flicker (1/f) Noise

As we already mentioned in the previous section, the 1/*f* flicker noise is dominant at lower frequencies. Equation (3-10) gives the basic formula that determines the 1/*f* noise brought by a DC current.

We estimate that the 1/*f* noise in MOS transistor is originates from two effects: charge trapping at the SiO_2 surface, and local fluctuations of carrier mobility. These two sources are described by the *McWhorter* and *Hooge* model.

The McWhorter Model

The first model dealing with 1/*f* noise proposed in [48] uses the fact that the noise is produced by charge variations close to the channel - SiO_2 interface. This variation is mainly caused by charge trapping in surface states. The 1/*f* spectrum results from the distribution of charge trapping time constant ~1/τ and is similar to *Eq*.(3-10):

$$i_{D,f}^2 = \frac{KI^{\beta}}{f^{\alpha \approx 1}}, \tag{3-22}$$

Here K is a process-dependent constant including the parameters such as W, L and C_{OX}, surface trap density, etc..

The Hooge Model

This theory [49], [50], states that the 1/*f* noise is essentially a bulk phenomenon and is manifested by resistance fluctuations occurring in the channel. Contrary to the previous model, the noise is caused here by mobility variations, and can be explained by charge transport mechanisms (such as phonon scattering). This model is named as Hooge's model and is characterised by a *Hooge's constant* α_{H}:

$$i_{D,f}^2 = \frac{I_D^2}{N} \cdot \frac{\alpha_H}{f}, \tag{3-23}$$

where N is the numbers of the carriers in the device. The α_{H} value varies for every material and is usually around 2×10^{-3}.

Some recent work showed that both mechanisms (described by Hooge and McWhorter models) are correlated at higher frequencies [43].

For hand-made calculations, we can use any simplified model, as shown on the example of a 1st Level model:

$$i_{D,f}^2 = \frac{K_F I_D^{AF}}{f^{EF} C_{OX} W \cdot L}, \tag{3-24}$$

where the constant (AF, EF, K_{F} and C_{OX}) are process-dependent parameters and W, L are the transistor channel dimensions. By exploring equation (3-24), an important dependence between the channel surface ($W{\cdot}L$) and the noise 1/*f* can be observed. Consequently, a correct device sizing and

tel-00417838, version 1 - 17 Sep 2009

an optimal choice of the operating point (I_D) can be used in order to optimize the noise. It is also common to consider PMOS transistor as less noisy than the NMOS transistors. This will be taken into account in our future design.

3.5 Low Noise Design

Noise signals are omnipresent and therefore generated in all phases of signal amplification. We will explore here several approaches which may significantly affect the noise. We have already shown two fundamental parameters of which the choices yield reduction of the noise: effective noise signal bandwidth Δf and the impedance level.

In the following, we shall discus the noise properties of two common amplifiers' topologies: *closed loop* and *chopper* amplifiers. We shall conclude this chapter with an approach employing a *Superconducting QUantum Interference Device* SQUID as the ultra low noise magnetic detector.

3.5.1 Feedback in Electrical Circuits

Feedback amplification is a circuit design approach that allows to improving some parameters, such as the gain accuracy or THD (total harmonic distortion) [40]. The feedback is realised with a circuit having the transfer commonly fixed by *accurate external resistors*.

To examine the noise in feedback network (amplifier), we will further assume the dominant noise of the amplifier is generated by its input stage. Therefore, it can be replaced by an equivalent input noise voltage source, as shown in *Fig. 3.7 a*) and *b*). *Fig. 3.7 a*) shows a feedback-free (open-loop) amplifier. Here, it is evident that the equivalent input noise voltage is directly the voltage v_{noise} (3-18).

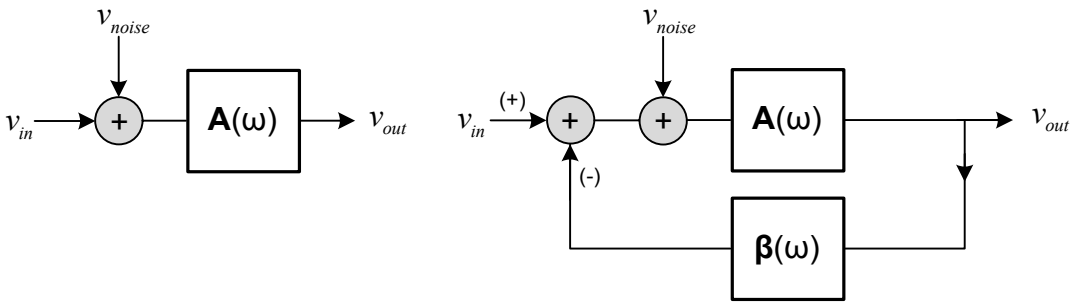


FIG. 3.7: *a) Feedback-free and b) feedback configuration of amplifiers with noise source modelling the noise of input amplifier stage*

Fig. 3.7 b) shows an amplifier using a feedback, represented by transfer β(ω). We assume the feedback network as noise-free. Using block algebra [51], the resulting voltage transfer (gain G) of *Fig. 3.7 b*) can be written as (see section *4.4.1*):

$$G = \frac{v_{out}}{v_{in}} = \frac{A}{1 + A\beta} \cong \frac{1}{\beta}. \tag{3-25}$$

The simplification has been provided when A tends to infinity. Here, the term $1/\beta$ means that the resulting transfer is determined *only* by the feedback coefficient β. Naturally, this transfer function can also be applied to the noise signal. We can therefore refer the total output noise ($v_{n,out} = G \cdot v_{n,in}$) to the amplifier input:

$$v_{n,in} = \frac{v_{n,out}}{G} = \frac{v_n / \beta}{1/\beta} = v_n. \tag{3-26}$$

tel-00417838, version 1 - 17 Sep 2009

This gives the expected results, showing no influence of feedback on the value of input referred noise voltage $v_{n,in}$.

Generally, such amplifier is realised by using an operational amplifier. Here, the feedback network is made of discrete resistors. However, these resistors can contribute to the total noise of amplifier and *deteriorates the noise properties*. Therefore, noise properties of the amplifier are not always improved by using the feedback technique, and on the contrary, an excess noise produced by the structure itself can arise.

3.5.2 Chopper Amplifier

The accurate amplification of very low voltages in lower frequency spectrum (close to DC), is affected by excess 1/*f* noise and the DC offset of amplifier. A suitable technique in order to reduce low frequency noise is the use of high frequency signal modulation [40], [52].

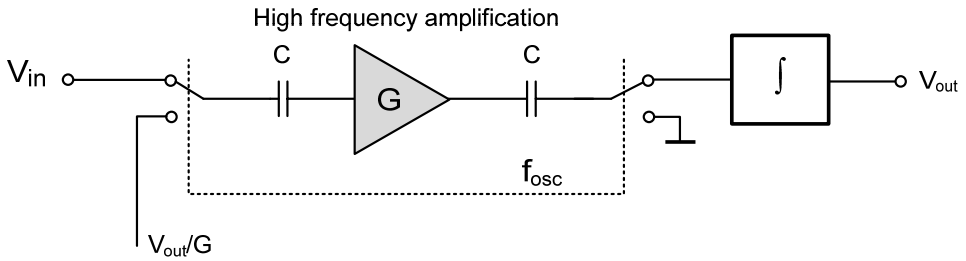


FIG. 3.8: *Chopper (auto zero) amplifier reducing the 1/f noise*

This concept is presented in *Fig. 3.8*. An amplifier with a high gain is capacitive coupled at the input and output. The signal v_{in} is sampled at some clock frequency, usually several hundreds of kHz. This sampling translates the low frequency spectrum into frequencies $n \cdot f_{clock,}$ where the amplification is provided. A second switch provides synchronous demodulation. The demodulated signal is integrated in a following integrator, where all higher spectral components are removed.

The advantage is that amplifiers can exhibit poor DC properties and 1/*f* excess noise but, due to the modulation, only flat-band white (thermal) noise interferes with the signal. Naturally, adequate switch quality and clock frequency filtering must be provided.

In some cases, we can use the amplification on higher frequencies directly. The measured sample (sensor) can be biased by an AC current and the narrow band amplification can be provided (*e.g.* by lock-in amplifier). For instance, such configuration has been used to measure static characteristic of nanoscale Single Electron Transistor *Fig. 2.19* being in a range of some 0.1 pA.

Typical noise of commercial chopper amplifiers is some tens of $nV/Hz^{1/2}$ in a frequency range as low as 100 µHz. (*e.g.* Analog Devices AD 8551).

3.5.3 Superconducting Quantum Interference Device

The superconducting quantum interference device is today the most sensitive magnetic sensor. Its performances approach the quantum limit with sensitivity reaching the nT range. The SQUID is made of one or two superconducting Josephson junctions, interconnected by a small superconducting coil. The coupling with an external circuit is done *via* inductive coupling, converting the measured signal into magnetic flux.

Superconducting Quantum Interference device is commonly used, for instance as an ultra low noise readout device for the bolometric detectors, as shown in *section 4.2.3*.

tel-00417838, version 1 - 17 Sep 2009

Josephson Junction

The Josephson junction is made of two superconductors, separated by a very thin insulator or metallic barrier (weak link), as shown in *Fig. 3.9*. In a bulk superconductor, the electrons can be present as single carriers or can be condensed in so-called *Cooper Pairs*. The Cooper Pairs are represented by a wave function similar to a free particle wave function. They are correlated and the wave function is constant even over macroscopic distances.

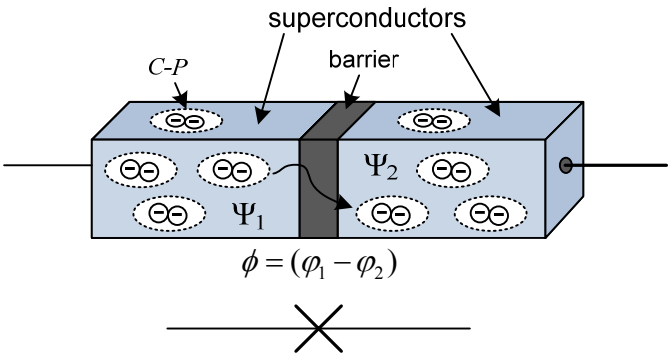


FIG. 3.9: *Josephson junction composed of two superconducting electrodes and weak insulator link*

The junction behaviour is characterized by the *Josephson effect* stating, that two superconductors separated by a thin transparent barrier keep the coherence of the phase between both wave functions Ψ_1 and Ψ_2. This mechanism is based on the interaction through tunnelling across barrier.

The behaviour of the Josephson junction is described by the *Josephson Equations*:

$$V(t) = \frac{h}{2e}\frac{\partial \phi}{\partial t} \tag{3-27}$$

$$I(t) = I_C \sin(\phi(t)) \tag{3-28}$$

In these equations, $V(t)$ is the voltage across the junction, $I(t)$ the current passing trough the junction and I_C the critical current. The term $h/2e$ is also called *magnetic flux quantum* Φ_0, equal to 2.0678×10^{-15} T·m^2.

The Josephson junction is characterized by *DC* and *AC* Josephson effects:

- **DC Josephson effect**: in the superconducting state, the current through the junction is caused by tunnelling of the copper pairs. The voltage $V(t)$ across the barrier remains zero and the phase difference between the wave functions in both superconductors is given by *Eq.*(3-27).
- **AC Josephson effect**: if the current exceeds the critical current I_C, a voltage V appears across the junction and the phase increases linearly with time, following *Eq.*(3-28). The phase oscillations induce the RF *Josephson current* of frequency $f = 2eV/h$, corresponding to 483 597.9 GHz/V. The junction becomes an oscillator, controlled by the applied voltage ≈ 483.5 MHz/μV.

The *I-V* characteristic of a typical *S-I-S* (Superconductor-Insulator-Superconductor) Josephson junction is shown in *Fig. 3.10*, corresponding to measured (averaged) envelopes.

In this figure, we can observe the previously mentioned zero voltage in superconducting state. Above the critical current, the resistance reaches a very high value, voltage limited by the *superconducting gap* around a few mV. In this region, we can observe the AC *Josephson current*, with the frequency dependence (3-28). Above the superconducting gap, the junction behaves like a

tel-00417838, version 1 - 17 Sep 2009

normal metal resistance characterized by R_n (*i.e.* normal electron tunnelling occurs). The AC Josephson current is commonly demonstrated by so-called *Shapiro's steps*, when the Josephson current is "frequency modulated" by exteriors the RF radiation. The resulting average DC envelope (second order Bessel function) exhibits voltage steps separated by $V(\mu V)=f(\mathrm{RF})/483{,}5$ MHz. This property of Josephson junction is *e.g.* used for today most accurate volt etalons.

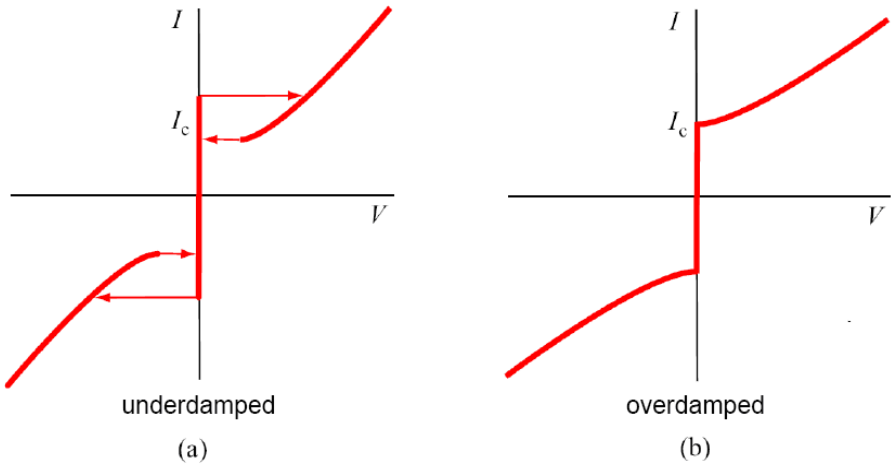
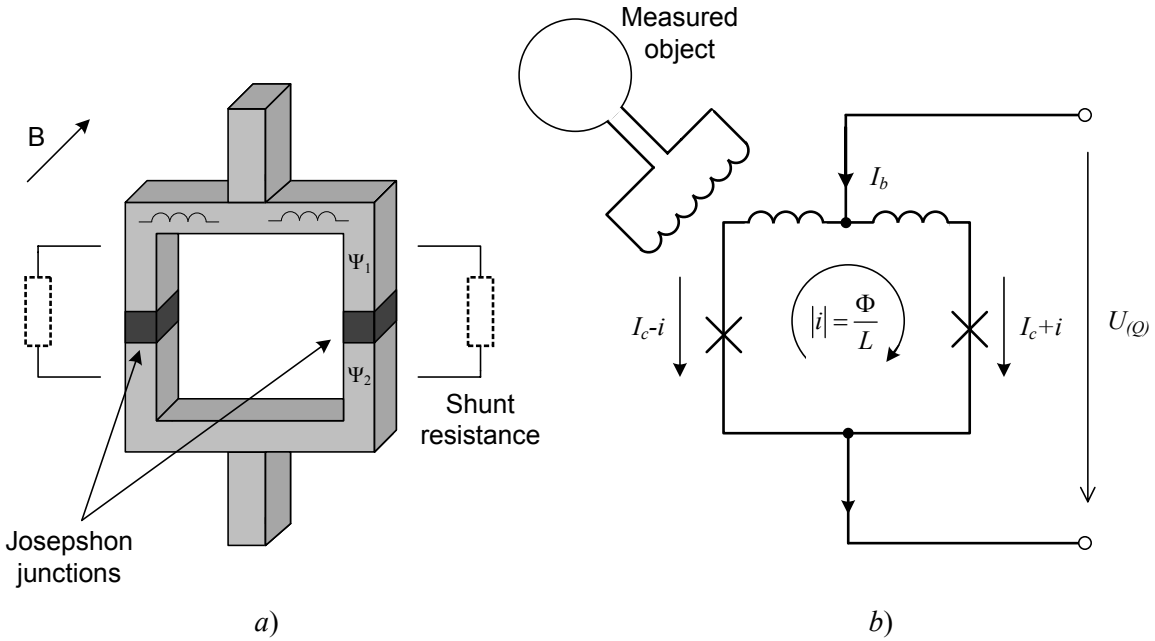


FIG. 3.10: *Hysteretic (under-damped) and non-hysteretic (over-damped) Josephson junctions I-V characteristics*

The SIS junction has an inconvenient hysteretic *I-V* characteristic. One commonly used way eliminating this hysteresis is the use of an external shunt resistor or a resistive (metallic) barrier.

DC SQUID

The basic configuration of a SQUID built from two Josephson junctions is shown in *Fig. 3.11*. The Josephson junctions are interconnected by two superconducting coils with diameters of some tens of μm, typically.



a) *b*)

FIG 3.11: *a) DC SQUID realized with two Josephson junction, b) schematic design with an external coupling inductance*

tel-00417838, version 1 - 17 Sep 2009

When investigating the electrical behaviour of the DC SQUID in presence of a magnetic field, we can find a small inducted current *i* circulating in the loop (*Fig. 3.11 b*):

$$\Phi_a = L|i|, \tag{3-29}$$

where L is the inductance of the coil and $\Phi_a = B \cdot S$ (S is the surface of the loop). We assume $\Phi_a << \Phi_0$. In the superconducting loop, the induced current reminds coastally circulating and results in an increase of the phase difference ($\varphi_1 - \varphi_2$) across the junctions:

$$\Delta\phi(B) = 2\pi \frac{\Phi_a}{\Phi_0}. \tag{3-30}$$

The induced current changes the critical current value I_C of both junctions to a "new" value $I_c \pm i$. By applying an external bias, (see *Fig. 3.11. b*), the new "critical current" depending on the applied magnetic flux would results in a transition of one of the junction (into a normal state), even for a bias current below $2I_C$. Since the critical current without applied magnetic field is $2I_C$, in the presence of magnetic field the current decreases to:

$$I_C^{'} = 2I_C \left| \cos\left(\pi \frac{\Phi_a}{\Phi_0} \right) \right|, \tag{3-31}$$

and the SQUID behaves as single Josephson junction with critical current modulated by the external magnetic field Φ_a, periodic with Φ_0. The voltage across the SQUID biased with a DC current (above $2I_C$) in presence of magnetic field is plotted in *Fig. 3.12*. This modulated voltage is the output voltage and can be amplified by further low noise (cryogenic) electronic.

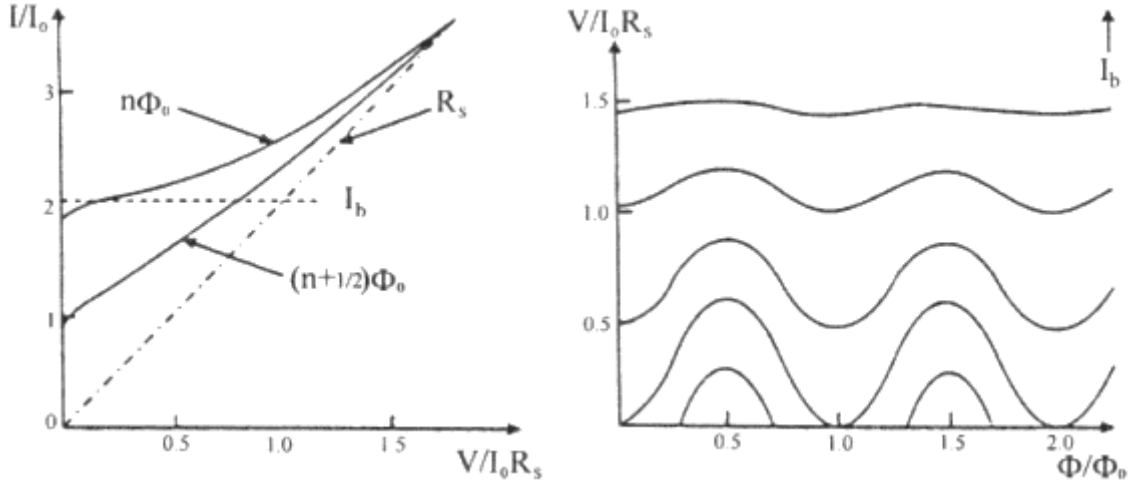


FIG. 3.12: *Characteristic of DC SQUID a) Junction I-V for two magnetic field (Φ_a and $n \cdot 0.5\Phi_0$) and b) V_{out}/Φ_a DC characteristic for various bias currents [54]*

In order to avoid the periodic response of the SQUID, magnetometric configuration (*Fig. 4.3,* [61]) can be used to limit the external flux to one hall of period: $\Phi_a < 0.5 \cdot \Phi_0$. In this configuration, linearization is provided by an artificial magnetic feedback (see *section 4.2.3*).

As we have already noted, the SQUID device presents today the most sensitive detector (magnetic amplifier), with noise in the range of fW/Hz^{½}, typically. Its application can be in the readout electronics of Transition Edge Sensors (*Fig. 4.3*), magnetic microscopy, or in recent superconducting digital electronic for quasi-THz clock frequency, based on *Rapid Single Quantum Flux Logic* RSFQ [55].

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Part II:

Architecture of Readout Electronic

Summary

In the second part, we describe the basic objectives aimed by development of readout electronics (amplification). Consequently, we introduce the general concepts of readout electronics used in industrials and scientific applications, in order to compare with our final architecture. This final architecture is based on a differential amplification, whose basic features and realisations are deeply examined, in order to define an unusual – feedback free- architecture. This architecture is considered as an optimal solution, opening a new and interesting possibility in the design of high performances electrical circuits.

tel-00417838, version 1 - 17 Sep 2009

4 ARCHITECTURE OF READOUT ELECTRONICS

4.1 Electrical Specification of Sensors

The main purpose of the electronics we intend to design is to provide amplification and additional frequency filtering for signals generated by *resistive bolometric detectors*. We thus intend this study to contribute to properly characterize the bolometers, with respect to their basic performance, such as power sensitivity, frequency response or thermal crosstalk. The results would hereby allow the optimization of the detector fabrication process, and, in final, it would also pave the way to a compact THz imager.

In this chapter, we are going to specify the basic constraints relative to amplification and discuss the choice of an amplifier architecture. The next important issue, frequency filtering, will be discussed in *part IV* of the thesis.

By definition, the resistive sensor (bolometric detector) is characterized by its steady state resistance R_0, which thermal variation is due to the input signal power variation. The output electric signal originates from external bias and is processed by readout electronics (*e.g.* amplifiers).

TAB 4.1: ESTIMATED PARAMETERS FOR THE DEVELOPPED YBCO BOLOMETRIC SENSORS

PARAMETER	**SUPERCONDUCTOR**	**SEMICONDUCTOR**
Temperature operating range	*~ 80 K*	*~ 290 K*
Resistance [Ω]	*Hundreds of Ω*	*Several kΩ*
Temperature coefficient TCR	*50-150, positive*	*0.5-10, negative*
Dominant pole	*Units of MHz (GHz for HEB)*	*Several Hz*
Inner noise	*Low*	*Increased*

The readout electronics will provide the amplification of signals issued from the bolometric detectors which operate at low (80 K) or room temperature. The design of low temperature detectors is based on high *Tc* superconducting YBCO micro and nano-bolometers, developed in the PhD thesis of M. Aurino. The room temperature detector has been developed using semiconducting YBCO micro

bolometers in the frame of the thesis of M. Longhin. Both PhD theses are developed in the frame of European project NanOtime (see for more information in [56]). The optimal choice of amplification setup is, naturally, determined by the basic parameters of these sensors, which estimated parameters are summarized in *Tab. 4.1*.

In our project, the bolometers (superconductor and semiconductor) will be integrated in a four pixel matrix configuration. In the case of hot electron nanobolometer (see *chapter 1*), only single detector patterns will be used.

In the following sections, we are going to describe the basic aspects of signal amplification, focusing the optimal noise and frequency response. We shall introduce some techniques used in scientific and industrial applications, as well as a configuration previous used in [57] and [58], aiming the characterisation of a similar configuration of 4-pixel bolometric array.

This study is important for the choice of an optimal amplifier configuration, presented in the end of the chapter. This choice is particularly sensitive, as quite different (and almost contradictory) detector parameters are to be considered (see *Table 4.1*). Concerning the operating frequency, our amplifiers will be designed for the lower frequency range (units of MHz) only. The design of high frequency (RF) amplifiers has been previously developed in [58].

tel-00417838, version 1 - 17 Sep 2009

4.2 Basic Concepts of Readout Electronics

4.2.1 Current and Voltage Bias

In general, the readout electronics concept makes use of a DC biasing current I_B or voltage V_B. The constant current I_B provides biasing of the detector (*Device Under Test* – DUT) and produces a terminal voltage which is amplified by an voltage amplifier. This configuration is depicted in *Fig. 4.1 a)* where the amplifier is AC-coupled. In the same way, the biasing can be made by constant bias voltage V_B where the current is the output parameter to be amplified (*Fig. 4.1 b*). Clearly, in both cases the output voltage V_{OUT} is a function of the steady state resistance variation ΔR.

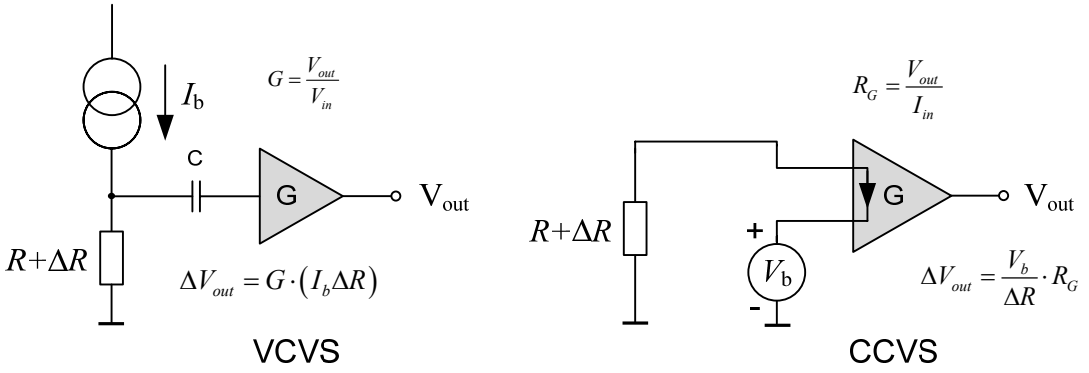


FIG. 4.1: *a) Current bias with voltage amplifier (AC coupled) and b) voltage biased sensor with current amplifier (R_G is the current gain - transresistance)*

We can discuss the basic properties which are required for biasing according to the main criteria:

- **Bias feasibility**
- **Noise and responsivity**
- **Electro-thermal feedback**
- **Frequency response**

i) **Bias Feasibility:** This criterion is related to the value of resistance R_0 which has to respect some voltage (or current) drop across the detector. For detectors with relatively low resistance, the

voltage biasing can become difficult because of excessive current. This current can damage such sensors which possess a sharp *I-V* characteristic (*e.g.* a superconductor sensor). Unlikely, detectors with high resistance have to be biased with a very small bias current; therefore, voltage biasing is to be preferred.

ii) **Noise and responsivity:** Considering the steady state resistance R_0 of the sensor, the related Johnson noise voltage (or current) is proportional to R_0 and $1/R_0$, respectively (see *Eqs.*(3-10) and (3-11)). The responsivity of a thermal detector can be expressed by its relative temperature coefficient of resistance (TCR) $\alpha = (1/R)\cdot(dR/dT)$ (*Eq.*(1-5)). Taking these quantities, we can define the detectivity D as a simple relationship of the noise and detected signal for a uniform radiation power as:

$$D = \frac{\Delta Signal_{out(\Delta T=1K)}}{Noise_{out}} = \alpha \left.\frac{\left(I_b \cdot R_0\right)}{\sqrt{4kT\Delta f \cdot R_0}}\right|_{\text{Current bias}} = \frac{V_b}{R_0/\alpha + 1} \cdot \left.\sqrt{\frac{R_0}{4kT\Delta f}}\right|_{\text{Voltage bias}} \qquad (4\text{-}1)$$

From these equations, we can perceive that for a current biased detector, the output detected voltage grows faster with the resistance than the noise (we consider an ideal noise-free amplifier). On the contrary, the output detected current increases faster than the noise current with decreasing resistance.

Eqs.(4-1) show the way to choose between current and voltage bias methods, with respect to the noise level. However, the rule, implicated from *Eqs.*(4-1), can be in cases of extreme resistance values (nearly zero or very high values), in direct contradiction to the statements mentioned in paragraph *i)*.

iii) **Electrothermal Feedback (ETF)**: The ETF is the effect arising from the dependence of dissipated bias power on the thermal sensitivity function *dR*/*dT* (*Chapter 1*). As an example, we can consider first the current biased semiconductor sensor characterized by negative thermal coefficient α. The dissipated bias power is defined by $R_0 \cdot I_B^2$ and V_B^2 / R_0 for current and voltage biasing, respectively. In our example (semiconductor sensor), the bias current heating causes the decrease of resistance $R_0(T)$. Consecutively, the change of dissipated bias power can be written as:

$$\Delta P = \frac{dP}{dT} \cdot T' = I_b^2 \cdot \frac{dR}{dT} \cdot T' . \qquad (4\text{-}2)$$

From *Eq.*(4-2), the joule heating resulting from the bias power induces the decrease of dissipated power itself and results *in a thermal equilibrium*. This effect is coined as the negative electrothermal feedback. It can occur as well for a metallic (or superconducting) detector characterized by positive thermal coefficient α and biased at constant voltage V_B.

The ETF effect can be utilized with advantage to stabilize the operating conditions of detectors, for instance the operating point of a *TES* (Transition Edge Sensor). In this case, such operating point has to be maintained inside the superconducting transition region. Moreover, this negative ETF can considerably reduce the detector time constant τ_x, even below its fundamental value defined as $\tau = C/G$ [59] (C is the heat capacity and G the thermal conductance).

In contrast, the positive ETF can damage the sensor if the dissipated power increase (resulting from the bias) is larger than the heat outflow. For instance, the current biased sensor with negative value α will exhibit a temperature increase causing the additional power dissipation, until the point of device failure.

iv) **Frequency Response:** In general, the electrical model of a detector contains parasitic capacitances. The total parasitic capacitance along with the resistance R_0 defines the

tel-00417838, version 1 - 17 Sep 2009

fundamental electrical time constant $\tau = R_0 C_0$, limiting the signal bandwidth. It is obvious that a relatively small R_0 allows, with respect to frequency response, using both current and voltage biasing. Hence, for detectors with high values of R_0, the voltage biasing can be advantageous as the capacitance is eliminated by the low resistance bias voltage source V_B. In that case, the time constant reaches a smaller value.

These four factors demonstrating the choice of the bias technique may be of decisive issue to reach the optimal detector parameters and operating conditions.

4.2.2 The Differential Readout Technique

For some applications, the use of an AC coupled voltage amplifier (*Fig. 4.1 a*) may, to some extent, be problematic. Especially in cases when the low frequency (static) signals are to be investigated, like in applications of thermal imaging. Alternatively, direct DC coupling can be employed, if the DC voltage drop is not large enough to provoke the amplifier saturation.

One possible solution is to provide auto-calibration by the "differential sensing", as recently used in industrial thermal imaging sensors [60]. The principle of differential sensing is based on the comparison of a DC signal originating from an irradiated (active) bolometer with a signal of an electrically identical *blind* (reference) bolometer, placed in the vicinity of the active one (*Fig. 4.2*). This setup would allow to cancel the system temperature variations as well as the instabilities of bias sources.

The configuration can basically operate in two modes: static or charging/discharging integrator. They both use the noise filtering provided by an analog integrator. The charging/discharging mode is similar to the analog-digital converter with double integration, where the integrator is in the first period charged by the active bolometer and subsequently discharged by the blind bolometer (within identical time intervals). The residual integrated voltage is proportional only to the temperature difference between the blind and active (irradiated) bolometer. In the static mode, both bolometers are biased by signals with opposite polarities and the output voltage is directly proportional to $1/T_P \int (i_a - i_b) dt$.

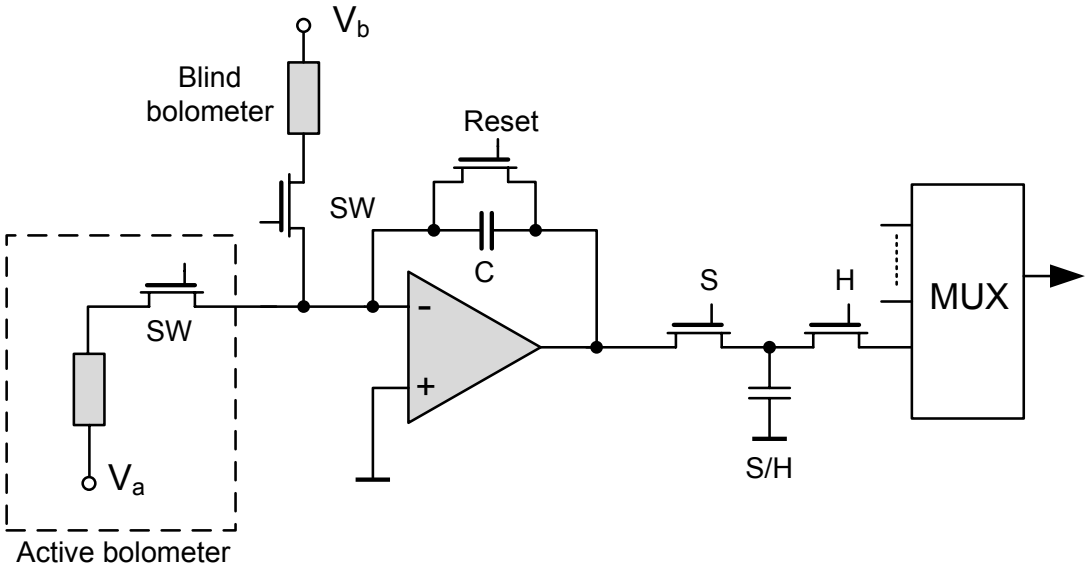


FIG. 4.2: *Differential configuration of bolometric sensor [60]*

However, this configuration requires one integrator for each pixel and therefore a hybrid integration of (*e.g.*) CMOS circuits and bolometers on the chip.

tel-00417838, version 1 - 17 Sep 2009

4.2.3 Special Readout Techniques

The bolometric detectors can be utilized in a broad domain of scientific applications (see *chapter 1*). In our study, we introduce two cases of such applications: *i)* large-frequency bandwidth (hot electron) bolometric sensors for THz heterodyne detection and *ii)* very-low temperature Transition Edge Sensor (TES) for ultra low noise applications.

High Frequency Readout Electronics

Typically, this readout is connected to a high sensitivity THZ frequency mixer, realised by a superconducting hot electron bolometer. The local oscillator (LO) and input power are mixed on its resistive body. The concept of readout electronics is in most cases based on current biasing. The difficulty of such setup resides in the intermediate frequency signal connection and amplification. As the frequency range can be in order of tens of GHz, a wideband impedance matching and connectivity provided by microstrip or CPW lines must be employed.

Ultra-Low Temperature TES

The Transition Edge Sensor may operate in the temperature range as low as dozens of *mK's*. At such temperature, the intrinsic noise of sensors approaches the ultimate noise limits. To maintain the decent properties of the detector, specific measures to protect the sensor against the environmental noise have to be considered.

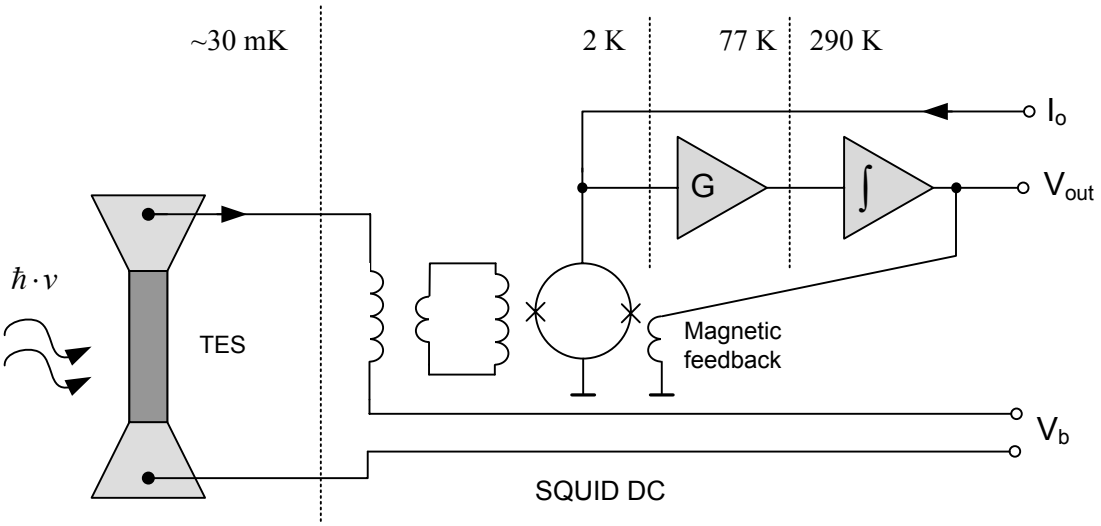


FIG. 4.3: *SQUID based ultra low noise readout of a Transition Edge Sensor*

One way to realize the ultra-low noise readout is to employ a Superconducting QUantum Interference Device (DC SQUID, see *section 3.5.3*). The DC SQUID is generally used in so called "*magnetometric"* configuration (*Fig. 4.3*) linearizing its periodic response (*Fig. 3.12*). The SQUID is biased by a constant current and exhibits periodical variations of its terminal voltage as a function of applied magnetic flux [61], see *Fig. 3.12*. This voltage is amplified by a cryogenic amplifier (at an intermediate temperature) and subsequently integrated. The mentioned linearization is provided by magnetic feedback maintaining the magnetic field in the SQUID loop at zero.

Nowadays, in the field of THz and infrared imaging, it is the common trend to implement multi-pixel *i.e.* arrays of detectors. Here, the readout electronics can be based on some advanced techniques, such as frequency domain multiplexing [62], reducing the number of active devices (*e.g.* SQUID, amplifiers). It is worth mentioning that such a configuration may exhibit a very high sensitivity but is limited in the terms of frequency to several tens or hundredths of Hz.

tel-00417838, version 1 - 17 Sep 2009

4.3 Choice of Readout Configuration

As mentioned in the previous sections, the detector setup can be advantageously carried out in the so called "multi-pixel configuration". We distinguish two basic groups of configurations: for example, in civil or military fields, IR arrays containing several hundreds of pixels are available [60]. Such types of sensors utilize the readout techniques similar to those used in the high density optical array sensors.

Secondly, most of scientific applications rely on detectors containing lower pixel numbers. In our study, we focus to the four pixel configuration (*chapter 4.1*). This low number makes possible a realization of the electronics setup with discrete components (amplifiers).

In the choice of a readout configuration, we are also facing problems with very low output signals. It is necessary to use certain techniques allowing the noise reduction. For instance, one of requirements is to place the amplifier close to the detector and to make it operate at the detector temperature. Another issue is the choice of voltage/current bias configuration (*chapter 4.2.1*). Naturally, it is convenient to use a unique bias source for all pixels in order to provide a good matching between all pixels. It is obvious, once the current has been selected, that the bolometer pixels must be connected in *series,* in contrast to the voltage bias, where the sensors must be connected in *parallel.*

Pointing out the configurations given in *section 4.1* and parameters in *Tab. 4.1*, we have in our study chosen a technique based on ***CURRENT BIASING*** with subsequent voltage amplification. This choice allows some practical simplifications of the testing set-up, necessary for device installation in a cryogenic environment. In the following sections, we determine an optimal configuration of readout electronics as well as the basic requirements on the voltage amplifier.

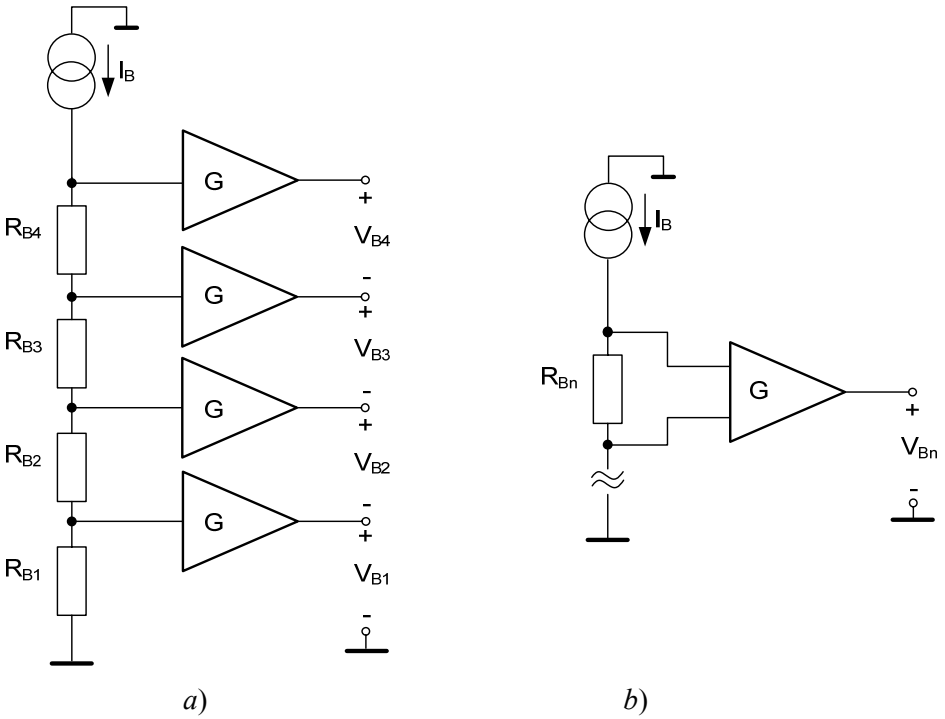


FIG. 4.4: *a) Structure of cascaded amplifier used in [57],[58] (R_{Bi} is the steady state pixel resistance), b) our selected differential read-out technique.*

Firstly, we present a configuration previously used in the frame of former PhD thesis [57], [58] (*Fig. 4.4 a),* elaborated at LGEP/LISIF (today L2E) laboratories. Here, all four pixels are serially connected and biased by a single current source I_B. Each nodal voltage is then amplified simply by one amplifier. Such a configuration can be evaluated in terms of positive and negative factors:

tel-00417838, version 1 - 17 Sep 2009

- **(+) simplicity of architecture**
- **(+) necessity of only one bias current**
- **(+) use of non-differential amplifiers**
  - as it is simpler and generally better for the noise and higher frequency bandwidth
- **(−) differential signal output**
  - the additional differential amplifier is needed to provide single ended output
- **(-) dynamic range of the amplifier**
  - Due to the superimposition of nodal voltages (V_{B1} – V_{B4} in *Fig 4.4*), the voltage at appropriate (higher) node may be higher compared to those closes to the ground. This would require different specifications of the amplifiers relative to theirs dynamic ranges.

We will then assume the last two drawbacks to be very important, when considering the final choice of a readout architecture. In particular, the asymmetrical output requires the use of a complicated connectivity between the cryogenic electronic and exteriors differential amplifiers. On this account, an architecture employing ***DIFFERENTIAL VOLTAGE SENSING*** (*Fig. 4.4 b*) based on a differential voltage amplifier with fixed gain G_0 has been selected for our future developments.

In the next section, we are going to classify the techniques that are being candidates to realize the differential amplification.

4.4 Differential Voltage Amplifiers

The general purpose of a differential amplifier is to provide a differential gain $G_0 = V_{OUT}/(V_+ - V_-)$, where the output voltage is proportional to the voltage between two input ports in_+ and in_- whereas the common voltage $(V_+ + V_-)/2$ has ideally no influence to the output voltage (*Fig. 4.5*). The vast majority of differential amplifiers possess an asymmetrical output, where the amplified signal is measured between output node and the ground. In principle, the differential sensing uses differential input cells, for instance transformer coils, optocouplers, or *integrated differential amplifiers*. The latter will indeed represent our centre of interest.

4.4.1 Dynamic Model for an Operational Amplifier

The definition and properties of an ideal Operational Amplifier (OA) are notoriously described in the literature (*e.g.* [40]). In this chapter we present a model, allowing a simple interpretation of its dynamic behaviour. We will focus firstly on basic limitations such as finite voltage gain and limited frequency response, important for the definition of the structure, used in a subsequent design.

The simplified structure of an operational amplifier (OA) is depicted in *Fig.4.5*. The structure can be interpreted as the combination of an *Operation Transconductance Amplifier OTA* (or transconductor) and a simple *voltage amplifier* of gain G_2. The input OTA provides the voltage/current conversion characterized by the *transconductance* $g_m = i_{out}/v_{in,diff}$. The output current is symmetrical with respect to the ground and flows thought a very high load resistance R_P. At this node (point A) a major part of gain is accomplished. In *Fig. 4.5*, the resistance R_P is in fact formed of parasitic elements only (such as the channel length modulation effect occurring in MOS transistors) and is constraining the maximal voltage gain G_0. The total amplifier gain can be written as:

$$A_{OL} = G_0 = \frac{V_{OUT}}{V_+ - V_-} = G_2 \cdot \left(g_m \cdot R_P \right), \tag{4-3}$$

tel-00417838, version 1 - 17 Sep 2009

where G_2 is the gain of the second stage. The symbol G_0 refers to the total low frequency (DC) voltage gain (sometimes cited as A_{OL} – Open Loop Amplification). The typical gain, achievable by such a structure resides in the 80 to 120 dB range.

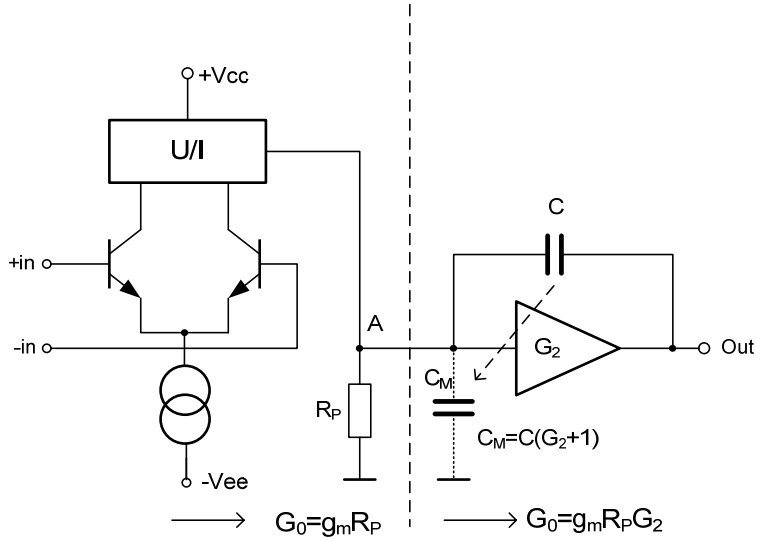


FIG. 4.5: *Simplified structure of an Operational Amplifier modelling the final voltage gain and frequency range*

Compensation of Amplifier

The operational amplifier is frequently used as a linear amplifier with fixed voltage gain. To achieve a constant value, the very large open loop value A_{OL} of the amplifier has to be decreased by an *external feedback*, as shown on the previously shown block schematic *Fig. 3.9 b)*. For convenience, we repeat here the transfer function of the closed-loop network:

$$G_{CL} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}}, \tag{4-4}$$

where G_{CL} is the resulting (closed-loop) voltage gain, A_{OL} is the open-loop gain and β is the transfer gain of the feedback network. The principle of a closed-loop amplifier is usually written in the limiting case $A_{OL} \rightarrow \infty$ in *Eq.*(4-4), as:

$$G_{CL} = \lim_{A_{OL} \to \infty} \frac{A_{OL}}{1 + \beta \cdot A_{OL}} = \frac{1}{\beta}. \tag{4-5}$$

Therefore, the resulting transfer function is determined by means of β only. The value of β is generally being fixed by accurate passive elements (resistances, capacitors) allowing very accurate setting of the gain. In practice, such an accuracy can be very difficult (or even impossible) to achieve in the open loop amplifier; *i.e.* directly in an active (CMOS, Bipolar) structure.

As previously noticed, the parasitic resistance R_P (*Fig. 4.5*) commonly reaches very high values (in the order of MΩ). Accordingly, even a small parasitic capacitance creates one *dominant pole* causing the decrease of the open loop frequency gain:

$$A_{OL}(j\omega) = g_m \cdot Z_{(A)} = g_m \cdot \frac{R_P}{1 + j\omega R_P C_M} = \frac{g_m \cdot R_P}{1 + j \cdot f / f_{c1}}. \tag{4-6}$$

It follows that above the frequency of the dominant pole f_{c1}, the operational amplifier exhibits a constant decrease of AC characteristic with a slope of -20dB/dec. In actual cases, some additional

tel-00417838, version 1 - 17 Sep 2009

poles can appear at higher frequencies. These additional poles cause, except for the degradation of the open-loop characteristics, an additional phase shift:

$$\varphi_{A_{OL}(f>f_i)} \approx n \cdot \pi \,, \tag{4-7}$$

where $\varphi_{AOL(f>fi)}$ is the phase shift beyond the *i*-th pole. Generally, in any linear feedback system, *the stability* is ensured by the presence of a *dominant negative feedback*. However, in the case of an excessive phase shift, the polarity of negative feedback may become reversed at higher frequencies, causing instabilities and oscillations. Hereto, we introduce the stability condition "*Nyquist criterion*" stating, that the phase shift of the open loop transfer $|\beta \cdot A|$ must be below 180º in the whole region of positive (dB) gain [40], [64]. In mathematical form, this can be re-written as:

$$\left|\beta(s)\cdot A(s)\right| = 1 \quad \text{for} \quad \arg\left\{\beta(s)\cdot A(s)\right\} \le \pi \,. \tag{4-8}$$

If the condition (4-8) is not satisfied, the system starts to oscillate. It follows from (4-7) and (4-8), that the oscillations can appear uniquely in dynamic systems containing at least three poles. An example of AC Bode plot of such a dynamic system is depicted in *Fig. 4.6*.

To provide an exact explanation, we define a "*gain crossover frequency*" as a value where the open loop gain $|A \cdot \beta|$ reaches unity (0 dB point, *Fig. 4.6*). For instance, uncompensated AC characteristic shown in *Fig. 4.6* exhibits the value of the gain crossover frequency well above that point, where the phase shift exceeds 180º (*phase crossover frequency*). In such a case the condition (4-8) is not satisfied.

In order to comply with *Eq.*(4-8), two methods of compensation are commonly used. Either the *feedback compensation*, where the value of β lowers the $|A \cdot \beta|$ in order to keep the gain crossover frequency below the value where $\varphi_{OL} = 180º$) or the *frequency compensation,* aiming to decrease of A value directly.

i) **Frequency Compensation:** The frequency compensation consists in artificially reducing the dominant pole frequency by Δf_{c1} (see *Fig. 4.6*) [64]. Such a pole shifting is the only way to maintain the system stability for the whole range of $\beta \in \langle 0, +1 \rangle$ (the extreme value $\beta = 1$ corresponds to the unity gain voltage follower). It is then obvious that the frequency compensation *does degrade* the open loop AC characteristics of the amplifier by decreasing the frequency of the dominant pole f_{c1}.

Fig. 4.5 demonstrates a classical technique used for frequency compensation, where a small capacitance is increased by the so-called *Miller effect,* in order to provide a more significant shift of the dominant pole or to provide a surface-optimal design (low-surface C). In this figure, a second amplifier having a negative voltage gain G_2 is bypassed by capacitance C. This capacitance C can be viewed as an equivalent grounded *Capacitor* C_M, appearing in the high impedance node A.

The value of C_M can be determined from the output voltage v_{out} and capacitor current i_C. The output voltage can be simply written as $V_{OUT}(t)_{out} = -G_2 \cdot V_{(A)}(t)$ and results in a current flowing through the capacitor C : $I_C(t) = \{V_{(A)}(t) - G_2 \cdot V_{(A)}(t)\} \cdot j\omega C$. In this equation, we can notice the value of voltage gain G_2 affects the final current value. This value G_2 appears therefore in the final formula for the equivalent capacitor C_M:

$$C_M = \frac{i_C}{j\omega \cdot v_{(A)}} = \left(1 + G_2\right) \cdot C \,. \tag{4-9}$$

Here, for $G_2 >> 1$; resulting *Miller Capacitor* C_M increases so that $C_M >> C$. This equivalent value of capacitor can be inserted into (4-6) and allows determining the impact of C_M to the amplifier AC response.

tel-00417838, version 1 - 17 Sep 2009

For the majority of commercially available amplifiers, the degree of compensation is selected so that the value of the feedback coefficient β can reach up to unity. Such class of amplifiers is referred to as *unity gain stable* amplifiers. Nevertheless, in order to realize the amplifier with voltage gain higher than unity, one prefers to use an amplifier compensated up to a *certain gain* value only (*i.e.* can obtain higher BW for prescribed closed loop gain).

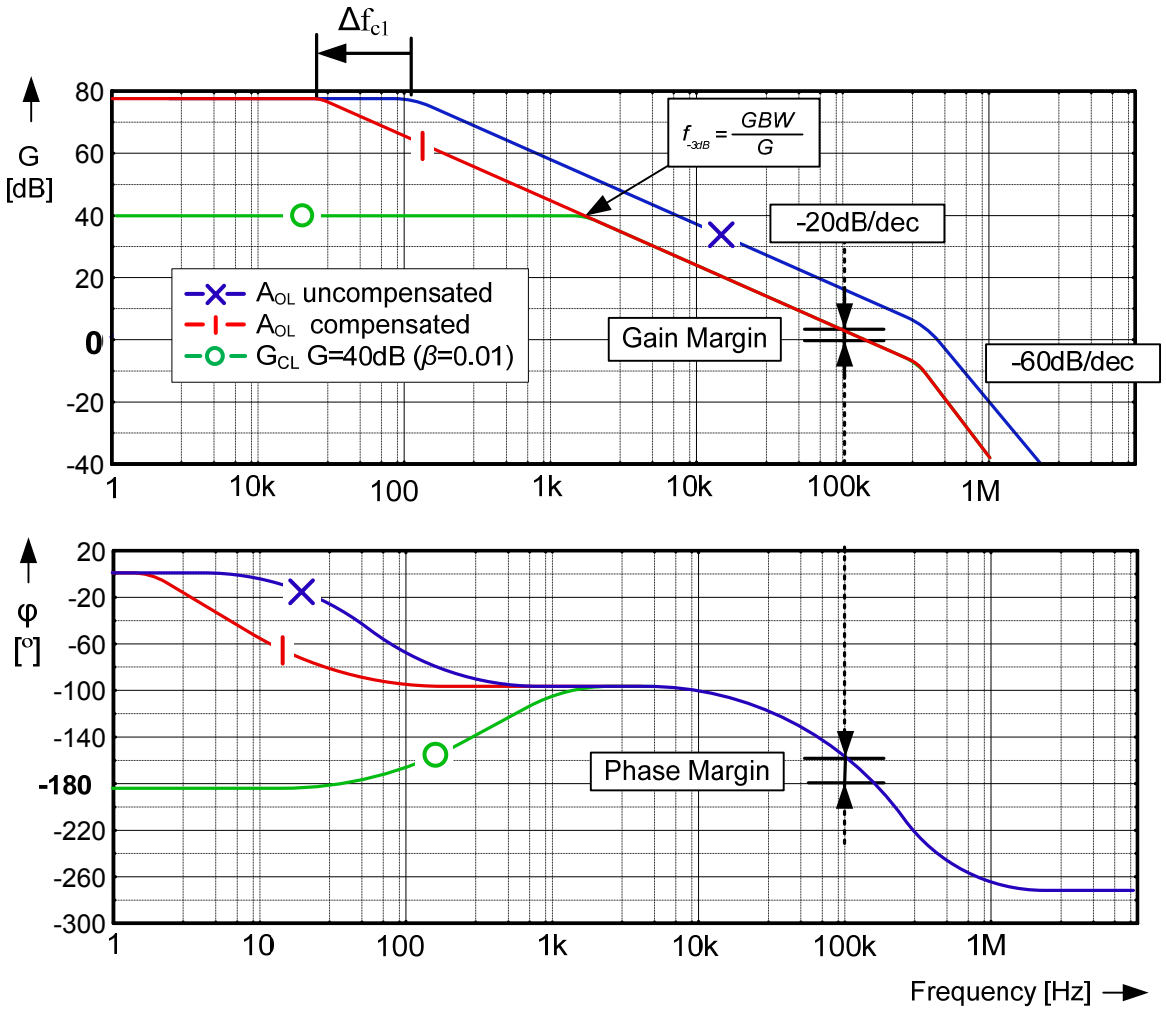


FIG. 4.6: *Magnitude and phase characteristic of uncompensated and compensated (here unity gain stable) operational amplifiers*

In practice, the capacitor C can be integrated in the amplifier structure directly, or connected externally (by option). However, the external compensation is feasible for lower frequency amplifiers only. For higher frequency ones, the value of C (or C_M) has to be very low and C can be overwhelmed by access capacitors (bounding or routing ones). In contrast to this technique, more optimal ways to provide the frequency compensation can be found in the literature [65].

ii) **Feedback Compensation**: The purpose of external compensation is to make the feedback coefficient β value so small that the *gain crossover frequency* $f_{|A\cdot\beta|=1}$ lies below the *phase crossover frequency* ($f_{(\varphi(A\cdot\beta))=180°}$). This technique is frequently used in *uncompensated operational amplifiers*. Here, the amplifier stability is ensured only for gain values larger than certain "critical" value. The use of uncompensated amplifiers allows a lower degree of frequency compensation with subsequent larger bandwidth operation. Another type of feedback compensation can be also carried out by an adequate frequency transfer of feedback network, as frequently used in the field of automatization [66].

tel-00417838, version 1 - 17 Sep 2009

By definition, a "*Marginally stable amplifier*" operates if condition (4-8) is exactly maintained. In reality, however, such a condition does not ensure the amplifier stability. That's why the amplifier has to be designed with sufficient *Gain* and *phase margins*. Typically, if the value of the phase margin is above 67º, the time response shows no amplitude ringing.

In the following paragraphs we are going to define some important terms allowing the evaluation of the properties of amplifiers operating in closed loop.

Slew Rate

In order to provide a comparison between various operational amplifiers, one typically specifies the *Gain×BandWidth product GBW*. The GBW is defined as the product of the open-loop low-frequency (DC) gain G_0 (4-3) times the frequency of the dominant pole f_{c1}. This GBW value is constant for compensated amplifiers. As shown in *Fig. 4.6*, for a VFA (voltage feedback amplifier), the -3dB cut-off frequency f_{-3dB} and GBW of the closed-loop amplifier are in mutual relationship *via* a required closed-loop gain G as: $f_{-3dB} = GBW/G$. It is necessary to mention, that in some recent approaches (such as the current mode operating circuits as CFA (*Fig. 4.7*) [67]), the GBW product does not have to depend on the closed loop voltage gain G any more.

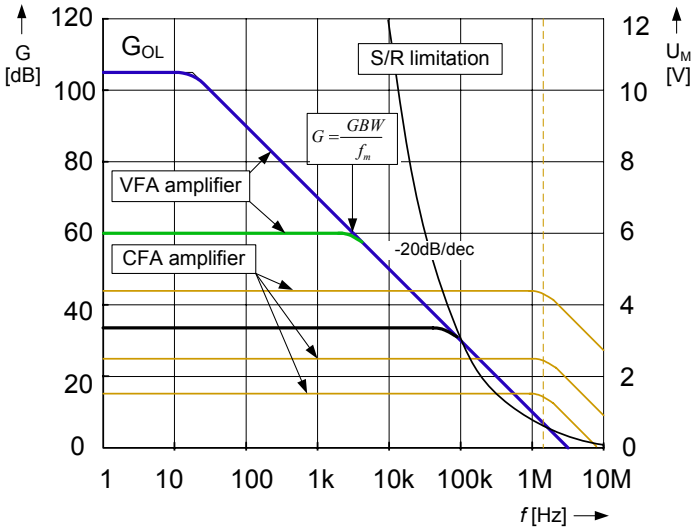


FIG. 4.7: *Comparing of the small gain bandwidth of the VFA (Voltage Feedback Amplifier) and the CFA (current feedback amplifier). Slew-Rate large signal limitation of classical VFA is also shown (see bellow)*

Another important dynamic parameter of an OA is the *Slew-Rate SR* [*V*/µs], indicating the maximum rising slope of output voltage for a large input voltage step. Unlike the cut-off frequency, the *SR* is a non-linear effect causing a distortion of the output signal. Therefore, in order to evaluate the *SR*, the amplifier output voltage must be considered along with the signal frequency (see *Eq. (4-10)* below).

The reason of *SR* limitation can be found directly in the simplified schematic of *Fig. 4.5*. In this figure, the Miller capacitor C_M is charged by the current provided by the input transconductance amplifier. For sufficiently high input voltages, the differential pair delivers its maximal saturation current I_{SAT}. The voltage on the capacitor is then simply given by $V(t) = (I_{SAT}/C_M)\cdot t$, which shows that the voltage rises linearly with an ultimate slope I_{SAT}/C_M [V/s].

We can demonstrate the amplifier *SR* limitation by the relationship between the maximal peak voltage and frequency for an output sinusoidal voltage. This can be done by comparing the maximal signal slope with the value of *SR*. For a sine wave, the maximal rising slope occurs when the signal transition goes through zero. Its maximal value dV/dt can be then determined by:

tel-00417838, version 1 - 17 Sep 2009

$$SR = \max\left\{\frac{dV}{dt}\right\} = V_{peak}\sin\left(\frac{\omega_{\max}}{nT}\right)\Bigg|_{n=0,1,2,\ldots}. \tag{4-10}$$

From this result, we can determine the methodology allowing the proper amplifier design with respect to the value of *SR*. For instance, for a given (required) output peak voltage (V_{peak}) the limiting frequency of the amplifier can be calculated from the *SR* as:

$$f_{\max} = \frac{SR}{V_{peak}} = \left(\frac{I_{SAT}}{C_M}\right)/G_2. \tag{4-11}$$

For V_{peak} equal to the amplifier saturation (output) voltage, this frequency is referred to as the *maximum power frequency*. Above this frequency, the signal is distorted and exhibits a decrease of its peak amplitude. As an example of this relationship, *Eq*. (4-11) was plotted together with the small-signal frequency response in *Fig. 4.7*.

4.4.2 Conclusion of Feedback and Frequency Compensation

The previous section pointed out some advantages of closed loop amplification, such as the accuracy of the voltage gain. In contrast, several important parameters can be degraded by using the feedback concept, as the maximum amplifier bandwidth or the *SR* that is limited by the frequency compensation.

We are now going to show that the use of feedback requires the integration of a high driving capability output buffer and that high input impedance differential amplifiers require usually 3 OA. These two factors result in the considerable increase of total power consumption and the complexity of the amplifier.

4.5 Applications of Operational Amplifiers

There are typically three basic configurations for an Operational Amplifier: inverting, non-inverting or differential. Generally, the global AC performances are determined by the dynamic properties of the active elements discussed in the previous section. We will now examine how various elements (resistor and OA) contribute to the overall noise. A simple rule allowing evaluation of OA based applications with respect to noise will be introduced as well.

4.5.1 Non-Inverting Amplifier

In *Fig. 4.8* we present the Operational Amplifier (OA) in the classical non-inverting configuration, where the gain is fixed by feedback resistors R_1 and R_2. At low frequencies, the gain v_{out}/v_{in} can be written as:

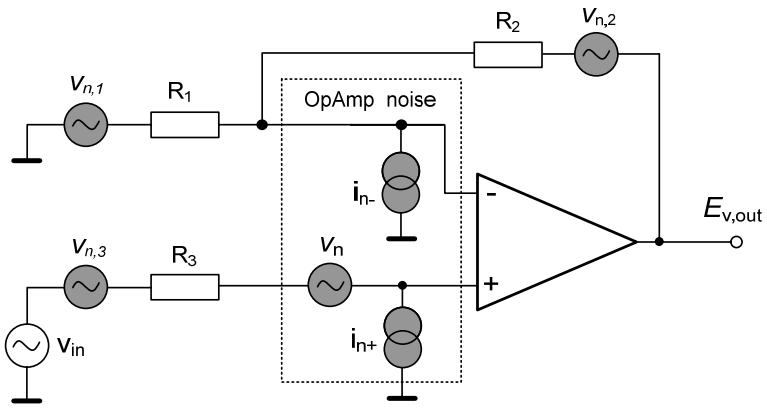
$$G_0(j\omega) = \frac{v_{out}}{v_{in}} = \frac{R_1 + R_2}{R_1 + \left(\frac{R_1 + R_2}{A_{OL}(j\omega)}\right)} \cong 1 + \frac{R_2}{R_1}\Bigg|_{A_{OL}\Rightarrow\infty}, \tag{4-12}$$

where $A_{\text{OL}}(j\omega)$ is the open-loop DC gain of the amplifier (4-6). For a bipolar OA, the optional resistor R_3 can be employed in order to compensate the input offset current.

In *section 3.4.4*, we have introduced a basic concept, allowing to characterize the amplifiers by their equivalent input noise voltage $v_{\text{n,in}}$. *Fig. 4.8* shows such a concept applied to the operational amplifier. The amplifier noise is represented by equivalent input voltage noise (v_{n}) and noise currents ($i_{\text{n+}}$ and $i_{\text{n-}}$). The thermal noise voltage generated by the feedback resistors are represented by relevant sources $v_{\text{n,1}}$ - $v_{\text{n,3}}$. The contribution of each noise source to the total output noise can be calculated as simple transfer

tel-00417838, version 1 - 17 Sep 2009

ratios $E_{n,out}/v_{n,x}$ of uncorrelated noise sources. The value obtained from circuit *Fig. 4.8 (left)* are collected in table *Fig. 4.8 (right),* where $v_{n,1\text{-}3}$ are Johnson noise voltages (see *Eq.*(3-8)).



Noise source	Output voltage $E^2_{v,out}$ $(nV/\sqrt{Hz})$
$v_{n,1}$	$v_{n,1}^2\left(R_2/R_1\right)^2$
$v_{n,2}$	$v_{n,2}^2$
$v_{n,3}$	$v_{n,3}^2\left(1+R_2/R_1\right)^2$
v_n	$v_n^2\left(1+R_2/R_1\right)^2$
i_{n-}	$i_{n-}^2 R_2^2$
i_{n+}	$\left[i_{n+}\cdot R_3\left(1+R_2/R_1\right)\right]^2$

FIG. 4.8: *Generalized noise circuit of an operational amplifier network*

The output noise voltages can be referenced to the input (v_{in}) by using the principle defined in *Eq.*(3-20):

$$E_{v,in}=\frac{E_{v,out}}{G_0}=\sqrt{\frac{E_{v,n1}^2+E_{v,n2}^2+E_{v,n3}^2+E_{v,n}^2+E_{v,in-}^2+E_{v,in+}^2}{\left(1+\frac{R_2}{R_1}\right)^2}}. \tag{4-13}$$

Hence, by using the values computed in *Fig. 4.8* we can express the input referenced noise voltage:

$$v_{n,in}=\sqrt{\underbrace{\left[4k_BT\left(R_1\|R_2+R_3\right)\right]}_{\text{noise caused by feedback resistors}}+\underbrace{v_n^2+i_{n+}^2R_3^2+i_{n-}\left(R_1\|R_2\right)^2}_{\text{noise generated by operational amplifier}}}. \tag{4-14}$$

In is interesting to associate the values of input noise $v_{n,in}$ and voltage gain G_0 with the values of feedback resistors R_1 and R_2. This can be done by comparing *Eq*. (4-14) with the voltage gain *Eq.*(4-12): we can notice the gain is depending on the R_2/R_1 ratio, whereas the total input noise generated by feedback network depends on the resistor *absolute values*.

This remark induces a simple rule, allowing the reduction of the noise: the use of *very low impedance level of feedback network*. Obviously, this rule is limited with the required power consumption of the amplifier and its output driving capability.

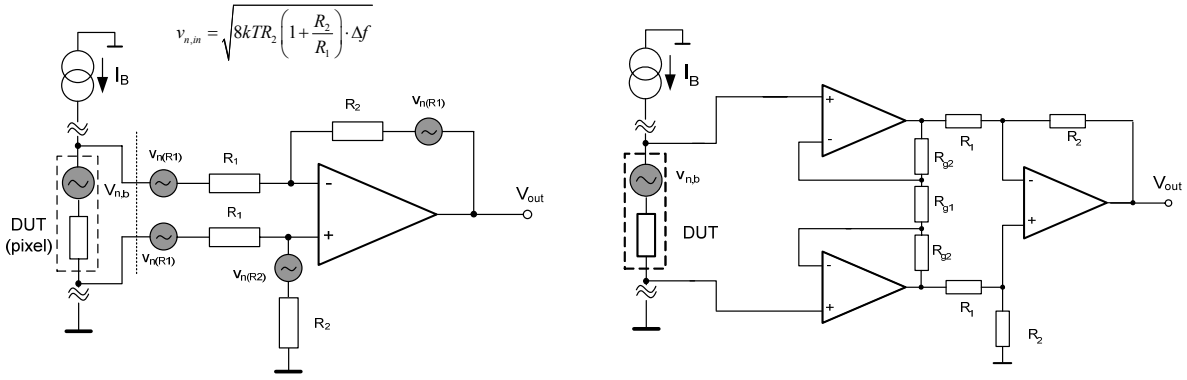
4.5.2 Differential Amplifiers

The basic structure of differential amplifier is presented in *Fig. 4.9 a*). Here, the value of the gain is given as $G_0 = R_2/R_1$. The analysis of noise can lead to a similar conclusion, compared to previous analysis of non-inverting amplifier, where the total input noise can be reduced by a choosing low feedback impedance values (see the noise formula shown in the inset of *Fig. 4.9 a*).

The main drawback for such an amplifier is the *finite (low) value of the input resistance* imposed by the feedback network and equal to $2{\cdot}R_1$. This low value can cause problems with high impedance sources, as semiconductor bolometric detectors. It can result in the undesired *shift of the gain* and subsequent *damping of the sensor*. The design of a differential amplifier with high input impedance can be done by using two methods: *1)* two followers connected to low impedance inputs or, *2)* by use of *instrumentation amplifier* [40]. The instrumentation amplifier can be realized by using at least two

tel-00417838, version 1 - 17 Sep 2009

or three OA's, as shown in *Fig. 4.9 b)*. The use of instrumentation amplifiers is advantageous because of the simple setting of the voltage gain by a single feedback resistor R_{g1}.



a) *b*)

FIG. 4.9: *a) single OA differential amplifier, b) Three OA instrumentation amplifier providing a high input impedance (DUT – device under test)*

In fact, the input section of the instrumental amplifier (*Fig. 4.9 b)* contains two non-inverting amplifiers with identical voltage gain. Both amplifiers share the feedback resistor R_{g1} and are followed by the single OA differential amplifier from *Fig. 4.9 a)*. For unity gain (*i.e.* $R_1 = R_2$), the voltage gain can be defined as:

$$G_0 = 1 + 2 \cdot \frac{R_{g2}}{R_{g1}}. \tag{4-15}$$

In practice, the instrumentation amplifiers are realized as discrete circuits, containing integrated resistors on a chip. The resistor integration would allow their very good matching and accurate gain value (frequently adjusted by laser during the fabrication). In many cases, the resistor R_{g1} is also optional, to be connected *via* external pins.

As shown in previous paragraphs, the values of feedback resistors influence the amplifier noise. As an example, we mention an ultra low noise (1 nV/√Hz) instrumentation amplifier INA103, which has the R_{g1} resistance of only 60.3 Ω ($G_0 = 100$ or 40 dB). Naturally, such an impedance level causes increased power consumption. Moreover, according to vendor datasheets, the instrumentation amplifier exhibits very low signal bandwidths, which limit its application to only a low frequency domain (see *Tab.7.4*).

4.5.3 Cryogenic Aspects

Operational amplifiers are available in a very large variety. The vendor specification includes usually the static and dynamic parameters of the amplifiers. Naturally, the industrial applications usually do not require cryogenic operation. Nevertheless, some experiments have shown the ability of several operational amplifiers, to be operating in a cryogenic environment (see [68], for instance).

Generally the restraints originate from the uncontrolled temperature swing of the operating point of the amplifier. This can be, in some cases overcome by increasing the power supply voltage, as shown in [68], or, by external compensation (*i.e.* external input bias voltage).

However, once the correct DC operating point is reached, all typical properties of operational amplifiers remain valid. In some cases, we can observe spurious oscillations (*e.g.* for CMOS operational amplifiers, even if they have been originally designed as unity gain stable. This is due to the transconductance increase in the internal CMOS structure.

tel-00417838, version 1 - 17 Sep 2009

4.6 Specification of Amplifiers to be Designed

In the previous sections we have introduced basic methods and properties of circuits which are potential candidates as the readout electronics for bolometric detectors or detector arrays. In the following section, we are going to propose an optimal amplifier configuration, according to our required electrical performance.

4.6.1 Choice of CMOS/Bipolar Process

As a desirable objective of the project we wish to integrate both high and low resistance superconducting and semiconducting bolometers in the identical test setup. However, with respect to noise, the range of resistances does not allow the choice between CMOS and bipolar realizations in an optimal way. Moreover, the availability of design tools in the concerned laboratories had to be respected.

By considering possible electrical constraints, the selected process for final amplifier realization was silicon CMOS AMS 0.35 µm process (see *section 2.5*).

The main reason of the choice was the lower input current noise current, as compared to bipolar technologies. The excessive noise current which is present *e.g.* in bipolar technology can degrade the noise properties, but also provides (altogether with high input offset current) an additional heating which should hamper the detection of weak signals.

The CMOS allows the realization of very high impedance input stages, operating with relatively low supply current. As we wish also to show further, the CMOS opens interesting ways of design techniques and circuit optimization.

4.6.2 Choice of an Amplifier Topology

As investigated previously, the most important drawbacks for operational amplifiers employing a classical feedback technique are:

- **Artificial decreasing of *GBW* and *SR* in amplifiers due to frequency compensation**
- **Low input impedance of classical differential amplifier (as from *Fig. 4.9 a*)**
- **Additional noise introduced by the feedback network**
- **Increased power consumption**
- **Integration of passive components on the chip** (see the size of C_M in [69], for instance)

For convenience, we notice the pros for a feedback topology, as high gain accuracy, low *THD* (Total Harmonic Distortion), nearly zero output impedance (at low frequencies), or high versatility of the amplifiers.

After thorough consideration, we selected an unusual configuration:

A feedback-free architecture

A feedback-free architecture would utilize an amplifier, *which has got the gain fixed in the active structure itself*. The architecture of such an amplifier is shown in *Fig. 4.10*. This amplifier structure operates with an AC-coupled resistive detector (DUT). The only passive elements subject to degrade the noise, are the high value resistors R_1 which are setting the DC operating point.

tel-00417838, version 1 - 17 Sep 2009

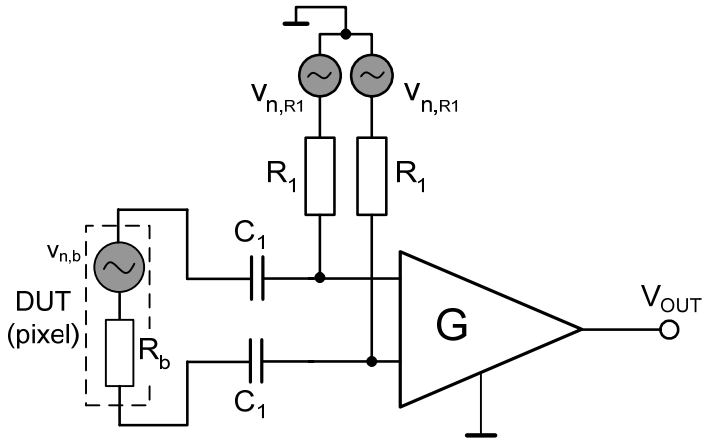


Fig 4.10: *Fixed gain differential amplifier with floating signal source modelled by $v_{n,b}$ and R_b*

In this configuration, the input noise voltage of the amplifier is directly the input noise voltage, to which the noise caused by resistors R_1 is added (see *subsection 3.5.1*). The noise contribution of R_1 can be evaluated by means of equivalent input noise $v_{n,in}$. Since the R_b is considered as noise free for simplification, this equivalent input noise voltage $v_{n,in}$ can be expressed as:

$$v_{n,in} = \sqrt{\frac{8k_BT}{R_1}} \cdot \left(\frac{2 + j\omega R_b C_1}{2 j\omega C_1} \right). \tag{4-16}$$

In this equation, we can notice a positive impact of the *high value of* R_1 to the total input noise. In consequence, the total input noise results from this noise *Eq.*(4-16), the detector noise $v_{n,b}$ and the amplifier input noise v_n. A high value of R_1 is desirable, because, in practice, it determines the input impedance of the amplifier.

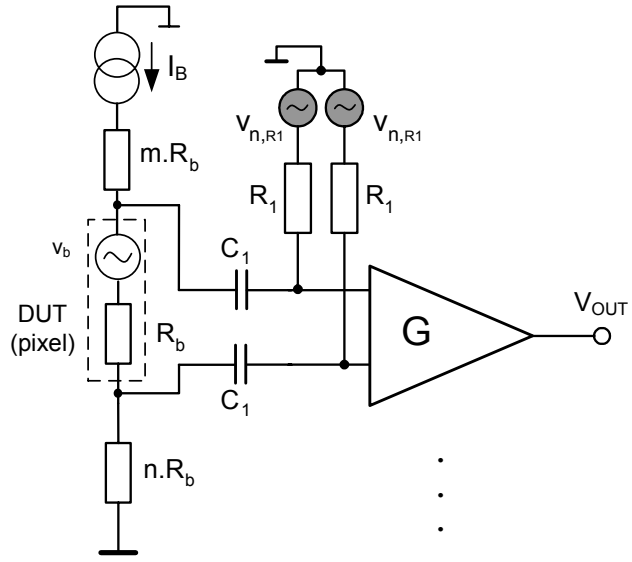


FIG. 4.11: *Fixed gain differential amplifier in a configuration with m pixels*

In reality, however, the noise of the bias resistors R_1 (*Eq.*(4-16)) is only approximative. The real configuration as show for *m* pixels in *Fig. 4.11* exhibits a slightly different noise, when changing the *n* and *m* values. However, the noise generated by R_1 can remain negligible, as the $R_1 >> R_b$ and the impedances of are C_1 is small as compared to R_b.

The fact that the relatively high (40 dB) voltage gain is to be set directly in the structure of the amplifier is one of the key reasons, why such structures are not established in practice (see an example

tel-00417838, version 1 - 17 Sep 2009

of a low gain amplifier in [70]). Generally, the absolute accuracy of active elements (transistors) are still considered as insufficient to allow a simple and accurate setting of the gain, namely for the high values above some 20 dB. Due to this fact, the design of such amplifiers will be of a major challenge for our future development.

4.6.3 Specifications on Electrical Performances

Considering the requirements for the electrical setup, we wish to define the parameters of the developed amplifiers. We require these amplifiers with:

- **40 dB static gain,**
- **Low static gain error**
- **Cryogenic and room temperatures operations**
  - in the 70 K to 300 K range
- **High differential bandwidth**
  - from DC to several MHz
- **Low noise level**
  - in units of nV/√Hz
- **High input impedance**
  - above 100 $k\Omega|_{DC}$
- **Low power consumption**
- **Simple architecture containing no passive elements**

4.7 Conclusion

In this chapter, we have reported the techniques being candidates for the realisation of readout electronics of bolometric detectors arrays. The different techniques such as using the simple current or voltage biasing, asymmetrical or differential sensing or the superconducting SQUID amplification were discussed. Upon these considerations, a current biasing with differential readout CMOS amplifier was selected.

We then inspected the solutions commonly used for the integration of differential amplifiers. These amplifiers are realised by using external feedback network. Their limitations (caused by stability, low input impedance, increased power consumption etc.) lead us to define in *section 4.6* an optimal *feedback-free architecture* of amplifier, having the gain defined only in the CMOS structure.

From this structure, we expect the performances, when compared, to be superior to classical solutions, like using instrumentation amplifiers. However, a main difficulty to be solved in the next following chapters is to design such amplifiers, where high gain accuracy of the gain is achieved, and maintained in an extreme (cryogenic) temperature range.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Part III:
Deign of Integrated CMOS Amplifiers

Summary

In the part III, design, optimization and experimental characterisations of fixed gain CMOS differential amplifiers will be presented. Two types of amplifiers will be designed, both based on the feedback-free architecture. The main challenge of the design is to provide high gain being accurately fixed directly in the structure, within a wide temperature range (T = 77 K to 390 K). This is provided by using a new low transconductance composite transistor, which is used in the i) geometric ratio fixed gain amplifier and ii) in the temperature compensated wide linear differential amplifier. The discussion of obtained results and their comparison with the state of the art is presented as the conclusion, confirming a good choice of architecture and design techniques.

tel-00417838, version 1 - 17 Sep 2009

5 DESIGN OF CMOS FIXED GAIN DIFFERENTIAL AMPLIFIERS

5.1 Constant Gain Amplifiers, Design Approaches

A differential amplifier with a constant voltage gain is one of the fundamental blocks in the design of electronic circuits. A traditional approach, based on the use of an operational amplifier in a closed-loop configuration was investigated in the previous chapter. In the construction of such amplifiers, frequency compensation is usually needed in order to stabilize the feedback loop. A drawback of the closed-loop concept (caused by limited bandwidth [70] and excess noise generated by the feedback network) is conjoined with increased complexity of the amplifier, requiring the on-chip integration of a low impedance output buffer or passive elements (*i.e.* resistors and capacitors). This leads us to define in *chapter 4* architecture of amplifier, where the gain is *fixed in a structure operating in open loop (*see *Fig. 4.10)*.

This chapter provides a summary of the techniques that are suitable for the design of fixed gain voltage amplifiers. Thereafter, two architectures of high, fixed gain amplifiers using a new ***low g_m composite transistor*** will be introduced. The first amplifier (*type I*) derives benefits from the accuracy matching of the transistors available in a classical CMOS process. The second amplifier (*type II*)

exploits temperature compensation of fundamental physical parameters, in order to provide the voltage gain constant within a large temperature range.

The key features required by the design have been defined in the *4th chapter*. They are being revised here:

- **40 dB differential voltage gain**
- **Low gain error**
- **Cryogenic and room temperature operations (in the 77 K to 300 K range)**
- **Differential gain bandwidth from DC to several MHz**
- **Low noise (~nV/√Hz)**
- **High input impedance (≈100 kΩ)**
- **Low power consumption**
- **Simple architecture**

5.1.1 Basic Types of Feedback-Free Voltage Amplifiers

The amplifiers with no external feedback loop can be basically designed as:

- **Amplifiers with fixed voltage gain**
- **Variable gain amplifiers (VGA)**

Since the first group is designed for an assigned voltage gain, the gain of VGA can be controlled *via* an external control signal (*e.g.* bias current or voltage). A VGA is usually designed for a large range of voltage gains with linear or logarithmic gain controlling. As an example, refs. [71] and [72] exhibit gain ranges of about 40 dB, which can be interesting in systems using the AGC (**A**utomatic **G**ain **C**ontrol). However, such a range generally results in a lower accuracy. It follows that the techniques used in the design of VGAs are not suitable for accomplishment of an amplifier with accurate assigned gain, especially for extreme (cryogenic) temperatures.

We will consider the fixed gain amplifier as the amplifier having a constant voltage gain, either not or only weakly depending on the external bias.

5.2 Temperature Modelling of the MOS Transistor

In this section we provide an analytical description allowing the wide temperature range modelling of a MOS transistor and related circuits. The temperature model is based on variable temperature measurements and numerical approximation of the transistor I-V characteristics.

Complex models based on a quantum mechanical concept and particle interactions can be found in the literature (*e.g.* [76], [81]). Several recent works have revealed an ability of CMOS process AMS 0.35 µm to operate down to the liquid helium temperature (4.2 K) (see [80] for instance). However, the available (SPICE) models are generally designed for temperatures in the -55 ºC to 390 ºC range. In order to design circuits for low temperature (cryogenic) operation (down to 77 K), a simple, and empirical model allowing to predict the behaviour of middle size saturated transistors has to be developed.

tel-00417838, version 1 - 17 Sep 2009

5.2.1 Thermal Behaviour of the MOS Transistor

Fig. 5.1 shows a measured characteristic $I_D = f(V_{GS})$ of a PMOS transistor for a temperature range between room and liquid helium T = 4.2 K (provided by author in collaboration with CEA-INAC Grenoble). We can observe two effects occurring at lower temperatures: an increase of the threshold voltage V_{TH} and an increase of the slope of $I_D = f(V_{GS})$. We can estimate that such a deviation of the transistor *I-V* characteristics can affect the circuit properties such as the DC operating point or voltage gain of an amplifier.

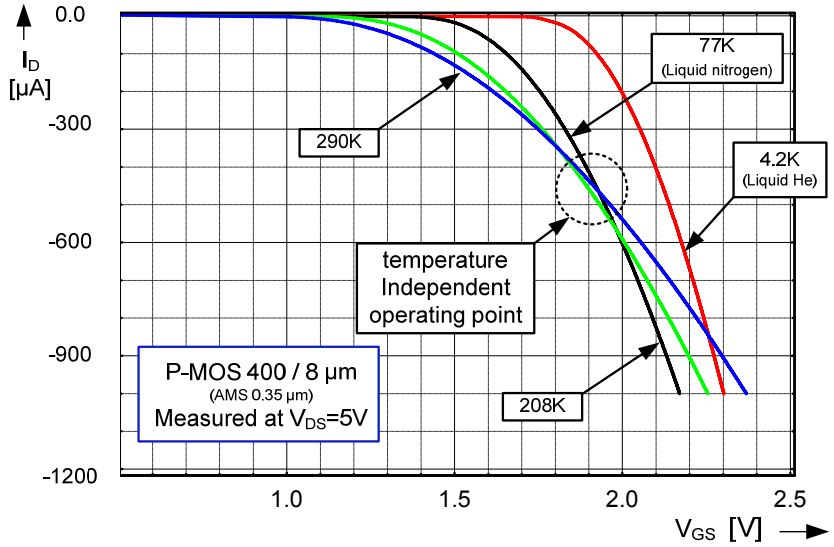


FIG. 5.1: *Measured I-V characteristic for a PMOS 400/8 µm transistor in 4.2K-290K temperature range*

The slope of $I_D = f(V_{GS})$ characteristics is depending on the *carrier mobility* (see *Eq.* (2-12)). The temperature dependence of carrier mobility can be interpreted as a consequence of atomic vibrations ("phonon scattering") related to the phonon energy. Generally, this dependence can be well fitted by a power-law [79]:

$$\mu(T) = \mu(T_0)\left(\frac{T}{T_0}\right)^{-x}, \tag{5-1}$$

where T is the temperature of the device and x is a constant related to the process. The value of this temperature coefficient x reaches theoretically 1.5, but vary for different processes due to different scattering effects. By exploring the temperature dependence of $\mu(T)$, an increase of the mobility can be observed at lower temperatures. However, at very low temperature, the characteristics exhibit an inflection where μ drop down to an extremely low level.

The shift of V_{TH} is basically caused by processes occurring in the MOS capacitor (see *chapter 2*). This function $V_{TH}(T)$ is modelled approximately by a constant temperature drift of – (1 to 4) *mV/°C* and can be described as:

$$V_{TH}(T) = V_{TH}(T_0)\left[1 + \alpha_{THX} \cdot (T - T_0)\right], \tag{5-2}$$

where α_{THX} is a relative thermal coefficient:

$$\alpha_{THX} = \frac{1}{V_{TH}} \cdot \frac{dV_{TH}}{dT}. \tag{5-3}$$

It can be shown that for $x = 2$, the variations resulting from the carrier mobility *Eq.*(5-1) and threshold voltage shift *Eq.*(5-2) can be compensated. This compensation occurs at one particular value of drain

tel-00417838, version 1 - 17 Sep 2009

current, called the *Zero Temperature Coefficient Point*. *Fig. 5.1* shows the area where the temperature variation of drain current is very low. However, in contrast to the low drain current variation, the variation of transconductance (slope) remains high. As we will show later on, the transconductance is a fundamental parameter that impacts the voltage gain of CMOS amplifiers.

As shown in the 2nd chapter, the drain current of the MOS transistor operating in the saturation regime follows the quadratic law (*Eq*. (2-16)):

$$I_D = \frac{\mu C_{OX}}{2}\frac{W}{L}\left(V_{GS} - V_{TH}\right)^2 . \tag{5-4}$$

From this current, a simplified 1st order model of the MOS transistor thermal behaviour can be expressed by virtue of (5-1) and (5-2):

$$I_D = \frac{KP}{2}\left(\frac{T}{T_0}\right)^{-x}\frac{W}{L}\cdot\left[V_{GS} - V_{TH}(T_0)\left[1+\alpha_{THX}\left(T-T_0\right)\right]\right]^2 . \tag{5-5}$$

The values of x and α_{THX} will be obtained by the measurement of static *I-V* characteristics for room and liquid nitrogen (77K) temperatures by numerical fit using the Least Squares (LS) method [83].

Secondary effects related to low temperature operation

The relative high cryogenic temperature (77 K), envisaged for our experiments does not give rise to important secondary effects mentioned in the previous section (*i.e*. carrier mobility drop at very low temperature). At low temperatures, we can take advantage of increased transconductance, lower noise but also of the weaker influence of parasitic parameters (*e.g.* lower resistivity of interconnection layers). This allows reaching better performance at cryogenic temperatures, such as lower gate delay and higher frequency operation, for instance. These features were demonstrated by measurements performed on a standard CMOS 4000 logic circuit, where a considerable (up to 2 times) increase of the gate delays was observed. On the contrary, the increase of V_{TH} results in a decreased dynamic range. The increased V_{TH} requires a higher power supply voltage (and therefore higher power consumption) compared to the operations at room temperature. We can refer to [82], where the cryogenic tests at 4.2 K have pointed out the presence of others effects – "Kink effect" or "electron freeze-out". At such low temperatures, we can note also the drop of the current gain concerning the parasitic bipolar transistors, which is favourable with respect to the latch-up effect (see *Fig. 2.2*).

5.2.2 Extraction of the Parameters

In order to acquire the thermal model using *Eq.*(5-5), the basic process parameters ($K_p = \mu_x C_{OX}$), V_{TH}, α_{THX} and x) have to be extracted. The basic parameters at room temperature ($V_{TH}(T_0)$ and $\mu_x(T_0)$) have been shown in 2nd chapter (see *Tab. 2.2*). These parameters will be corrected according measurement on fabricated transistors. The values of x and α_{THX} can be then obtained from the shift of measured parameters between room and liquid nitrogen temperatures.

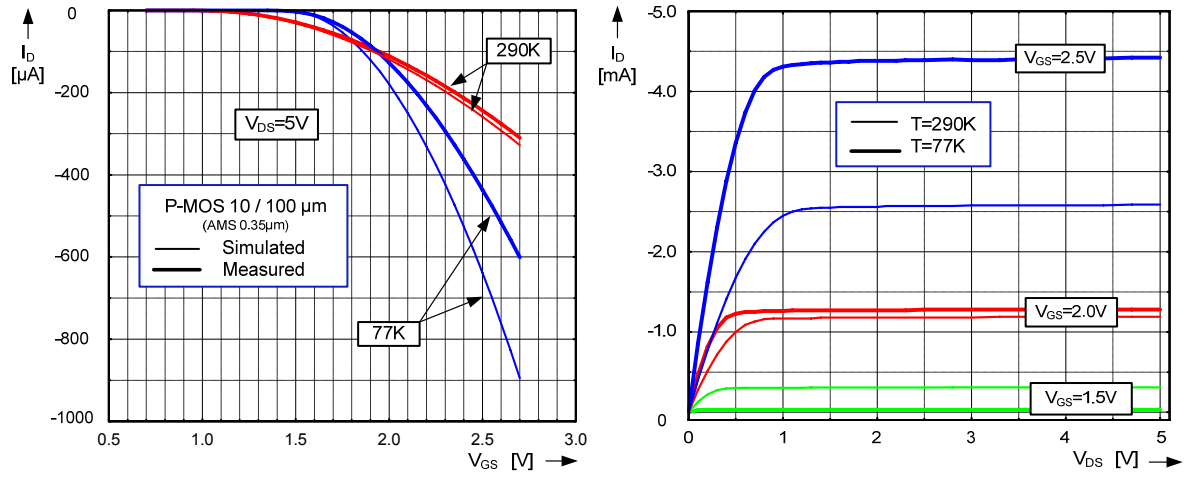
During the design of our amplifier, we have disposed of only four MOS transistors provided by AMS foundry: P-channel type MOS W/L = 100 µm/10 µm and 15 µm/0.5 µm and N-channel MOS transistors W/L = 250 µm/0.5 µm and 5 µm/0.5 µm. In fact, this W/L is not very convenient since only one transistor has the gate length above 1 µm. As it has been shown in 2nd chapter, the submicron dimension can introduce supplementary terms in the transistor model, as the carrier velocity saturation, channel length modulation etc. Moreover, the transistor with $L < 1$ µm is at the limit of technological resolution and displays therefore higher parameters dispersion. It follows that the only worthy candidate is the first transistor: 100 µm/10 µm MOS transistor with P-channel type. This

tel-00417838, version 1 - 17 Sep 2009

transistor can be well approximated by the 1st order quadratic model (5-4). In fact, the availability of a P-channel transistor is advantageous. This is due to the lower 1/*f* noise compared to an N-channel type transistor and therefore its intended use in the input differential pair of the amplifier.

Static I-V Characteristics

The measurements and simulation were performed at room (T = 290 K) and liquid Nitrogen (T = 77 K) temperatures for all transistors. *Fig. 5.2 a*) shows a comparison of simulated (SPICE level-7 model) and measured *I-V* characteristic of the selected P-MOS transistor *W*/*L*= 100 µm/10 µm. *Fig* (*a*) illustrates a very good matching between the simulation and measurements at room temperature. However, this figure also cleary confirms the needs of an accurate model for cryogenic (~77 K) temperatures.



a) *b*)

FIG. 5.2: *Comparison of characteristic obtained by measurements and simulations on a PMOS transistor W/L=10 / 100 µm*

5.2.3 LS Model Parameters Fitting

A simple determination of V_{TH} and gain factor *KP* from the *I-V* characteristics (*Fig.5.2 a*) can be doubtful as the I_D current rising around V_{TH} is "vague" (*chapter 2*). To provide an accurate value of V_{TH}, we can use a standard quadratic *Least Squares* (LS) fit, minimizing the squared difference between the points of measured characteristic and approximation. The general criterion of least squares algorithm can be written as:

$$R^2 \equiv \sum_{i=0}^{n}\left[y_i - f\left(x_{1,i}, x_{2,i}\ldots x_{m,i}, a_1, a_2\ldots a_m\right)\right]^2 \rightarrow \min \Rightarrow \frac{\partial R^2}{a_{1,2,..m}} = 0\,, \qquad (5\text{-}6)$$

The minimum of *R* can be found by setting all partial derives of the fitting function to zero. In our case, the goal function (5-4) can be rewritten in the following form: $y_i = b\cdot(x_i - a)^2$. However, this function differs from a general 2nd order polynomial one, which analytic fit is known in the matrix equation form (*e.g.* see [84]). The partial derives of the approximating function $y_i = b\cdot(x_i - a)^2$ can be expressed as:

$$\begin{aligned} &\frac{\partial}{\partial a}\sum_{i=1}^{n}\left\{ y_i - b\cdot\left(x_i - a\right)^2\right\}^2 = nb^2a^3 + \sum_{i=1}^{n}\left(y_i bx_i - aby_i - b^2x_i^3 + 3b^2ax_i^2 - 3b^2a^2x_i\right), \\ &\frac{\partial}{\partial b}R^2 = 2nba^4 + \sum_{i=1}^{n}(2ay_ix_i - y_ix_i^2 - y_ia^2 + bx_i^4 - 4bax_i^3 + 4ba^2x_i^2 - 4ba^3x_i). \end{aligned} \qquad (5\text{-}7)$$

tel-00417838, version 1 - 17 Sep 2009

where, setting the above expressions to zero leads to a system of two nonlinear equations in the parameters *a* and *b* which can be solved by Newton's method. The V_{TH} and gain factor *KP* can be then calculated by comparing the coefficients *a* and *b* to *Eq.*(5-4). The coefficients computed are listed in following *Tab. 5.1*.

The values in *Tab. 5.1* confirm our assumption that only the P-MOS 100 µm / 10 µm transistor provides an accurate agreement between the simulation and measurements (for room temperature).

TAB 5.1: PARAMETERS OF *EQ.*(5-4) MODEL OBTAINED BY LM FIT (5-7) BASED ON MEASUREMENTS AND SIMULATION (SPICE LEVEL 7) ON PMOS 100 µm/10 µm TRANSISTOR. THE SIMULATION AT 77 K GIVES V_{TH} = 1.23 V AND KP = 76,37 µA/V^2

TRANSISTOR TYPE	**SIMULATION 296K**	**MEASURED AT 296K**	**MEASURED AT 77K**
P-MOS 100 /10 µm			
KP [A/V^2]	20.67×10^{-6}	21.63×10^{-6}	72.43×10^{-6}
V_{TH}[V]	-0.9649V	-0.9534V	-1.40493V
P-MOS 15 / 0.5 µm	-	--	-
KP [A/V^2]	16.08×10^{-6}	$19{,}03 \times 10^{-6}$	35.02×10^{-6}
V_{TH} [V]	-0.8853V	-0.7344V	-1.1566V
N-MOS 250 / 0.5 µm	-	-	-
KP [A/V^2]	102×10^{-6}	79.013×10^{-6}	214.12×10^{-6}
V_{TH} [V]	0.6855	0.67599	0.9370V
N-MOS 5 / 0.5 µm	-	-	-
KP [A/V^2]	51.0×10^{-6}	48.23×10^{-6}	89.65×10^{-6}
V_{TH} [V]	0.4902	0.5415	0.8164

It is worth noting that the empiric model can provide better simulation results and in our case allows to improve the hand calculations even for cryogenic temperatures (compare the measured value of *KP at T = 290K* and values provided by foundry, *Tab. 2.1*).

The values of coefficient *x* and α_{THX} can be determined by solving the equations (5-3) and (5-1) for both 296 K and 77 K temperatures and are summarized in *Table. 5.2* (PMOS *W*/*L*=100 µm / 10 µm).

TAB. 5.2: PARAMETERS OF MODELS (5-5) OBTAINED FOR THE PMOS TRANSISTOR *W*/*L*=100 µM / 10 µM (T_0=296 K)

	x	**α_{THX}**	**V_{TH} shift**
PMOS 100 µm/10 µm	0.90	-2.163 mK^{-1}	-2.06 mV/K

5.2.4 Verification of the Model

In order to validate the parameters of the model, we have carried out a measurement on a P-MOS transistor 400 µm / 8 µm fabricated in a different run (1 year later). The parameters were calculated by applying the described method of LM fitting and are listed in *Tab. 5.3*. The parameters show a good agreement with *Tab. 5.1* and *Tab. 5.2*. Comparison of the model applied to a 400 µm/8 µm P-type

tel-00417838, version 1 - 17 Sep 2009

transistor (using the parameters *Tab. 5.1* and *Tab. 5.2*) and measurement performed on a "more recent" transistor is given *via* the characteristics in *Fig. 5.3*.

TAB. 5.3: EXTRAPOLATED PARAMETERS OF TRANSISTOR PROVIDED IN 2ND FABRICATION RUN

TRANSISTOR TYPE	**MEASURED 296K**	**MEASURED 77K**	***x***	α_{THX}
MOSP 400 µm/8 µm				
KP [A/V^2]	21.45×10^{-6}	70.16×10^{-6}	0.89	-
V_{TH} [V]	-0.9999V	-1.4154V	-	-1.95mV

In this table, the accuracy of the model presented above is sufficient for both cryogenic and room temperatures, concerning the $V_{TH}(T)$ voltage in particular. The errors are caused by the dispersion of transistor parameters occurring between two different fabrication runs, as well as by the difference between the W/L ratios of the transistors.

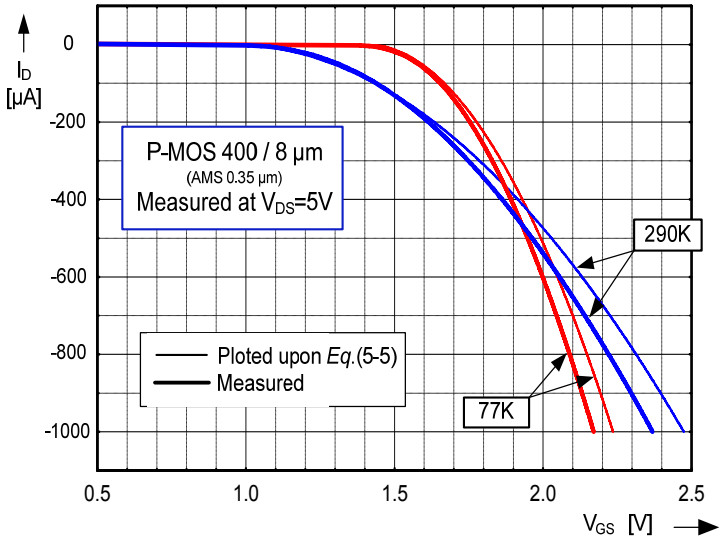


FIG. 5.3: *Verification of model Eq.(5-5) with TAB 5.1 and TAB 5.2 parameters and measurements performed on a transistor fabricated in a different run*

In the complex models of transistors, the dispersion of parameters is covered by a set of so called "*corner parameters",* allowing the worst case analysis with respect to the maximal process errors. The previously delivered model allows to estimate the parameters at 77 K upon these accurate models (*e.g.* BSIM-3) at room temperature, but also to provide an analytical description of the amplifier in a wide temperature range.

5.3 Structures of CMOS Fixed Gain Amplifiers

It has been already shown that the use of classical feedback amplifiers can exhibit limited electrical performances. In the following sub-sections, three fundamental types of open loop amplifiers will be presented along with their basic features. Consequently, a new component, the ***low transconductance MOS composite transistor*** will be designed for their use in further design of high, fixed-gain amplifiers.

tel-00417838, version 1 - 17 Sep 2009

5.3.1 Common Source Amplifier

One of the basic configurations that is frequently used in CMOS and intended to provide fixed voltage gain is the *common source* (CS) amplifier. It is shown in *Fig. 5.4* [22]. For low gain values, the CS amplifier is based on the connection of two MOS transistors, the *driving transistor* M_1 characterized by its transconductance g_{m1} and a *load (diode connected) transistor* M_2 with transconductance g_{m2}. The interesting feature of the amplifier is the voltage gain being set *by virtue of a high accuracy dimension ratio*.

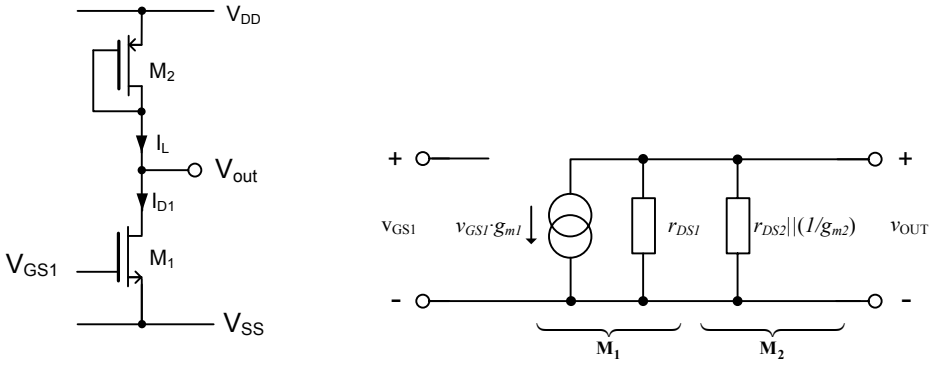


FIG. 5.4: *a) Basic configuration of a common source amplifier and b) linearized model*

The voltage gain G_0 of the CS network (*Fig. 5.4)* can be determined in two ways:

i) As slope of static DC transfer characteristic $V_{OUT} = f(V_{GS1})$;

ii) By small signal analysis using the linear amplifier model *Fig. 5.4 b*).

i) Static DC Voltage Transfer

The analysis of the DC transfer characteristics will allow us to obtain the large signal voltage transfer $V_{OUT} = f(V_{in})$ and evaluate the voltage gain $G_0(V_{in})$ as a function of the amplifier operating point. This characteristic can be deduced from the voltage drop on the *diode connected MOS* transistor M_2, caused by the drain current M_1. The drain current (I_{D1}) results from the quadratic law (5-4) (after neglecting the channel length modulation):

$$I_{D1} = \frac{KP_N}{2}\frac{W_1}{L_1}\left(V_{GS1} - V_{THN}\right)^2, \tag{5-8}$$

where KP_N and V_{THN} are parameters related to a N channel type transistor. Obviously, the drain current of both transistor M_1 and M_2 are equal ($I_{D1} = I_L$) and V_{GS2} reaches:

$$\left|V_{GS2}\right| = \left|V_{DS2}\right| = \sqrt{\frac{2 \cdot I_L / KP_P}{(W/L)_{M2}}} + \left|V_{THP}\right|, \tag{5-9}$$

As $I_{D1} = I_L$, the output voltage $V_{OUT}(V_{GS1})$ can be determined by inserting (5-8) into (5-9):

$$V_{OUT} = V_{DD} - \left\{\sqrt{\frac{KP_N}{KP_P}}\sqrt{\frac{(W/L)_{M1}}{(W/L)_{M2}}} \cdot (V_{GS1} - V_{THN}) + \left|V_{THP}\right|\right\}. \tag{5-10}$$

This equation shows the DC transfer characteristic (V_{GS1}/V_{OUT}) as a linear function of V_{GS1} (we suppose the both transistors are operating in saturation and the channel length modulation can be neglected).

tel-00417838, version 1 - 17 Sep 2009

The small signal voltage gain G_0 can be obtained as the slope dV_{OUT}/dV_{GS1} (5-10) and is independent on the operating point:

$$G_0 = \frac{dV_{OUT}}{dV_{GS1}} = -\sqrt{\frac{KP_N}{KP_P}}\sqrt{\frac{W_1/L_1}{W_2/L_2}}, \tag{5-11}$$

It can be noticed that the numerator and denominator are similar to the small signal transconductance $\sqrt{2KP_X\,W/L}\cdot\sqrt{I_D}$ of a current biased MOS transistor *Eq.* (2-26). On this account *Eq.*(5-11) can be rewritten as a transconductance ratio:

$$G_0 = -\frac{g_{m1}}{g_{m2}}, \tag{5-12}$$

which represents a fundamental expression of the small signal voltage gain important in further design.

ii) Small Signal Voltage Gain

The voltage gain in the form *Eq.*(5-12) can also be obtained from the linearized model (*Fig 5.4. b*). The drain current $i_{d1} = g_{m1}\cdot v_{GS1}$ of the driving transistor M_1 causes the voltage drop on the load transistor equal to $i_{d1}\cdot r_{out}$, (where r_{out} is the impedance of the output node). This impedance includes the drain output resistance $r_{ds1} // r_{ds2}$ and gate transconductance g_{m2} of the load transistor M_2: $r_{out} = (r_{ds1}||r_{ds2})||(1/g_{m2}) = g_{d1} + g_{d2} + g_{m2}$ which results in the small signal voltage gain G_0:

$$G_0 = \left|\frac{v_{out}}{v_{in}}\right| = \frac{i_{D1}}{v_{in}}\cdot r_{out} = \frac{g_{m1}}{g_{m2}}\cdot\frac{1}{1+\left(g_{D1}+g_{D2}\right)/g_{m2}}, \tag{5-13}$$

This equation agrees with (5-12) where the channel length modulation (g_{d1}, g_{d2}) was neglected.

The amplifier *Fig. 5.4* is a good example of how the voltage gain can be fixed *by* a *constant transconductance ratio of the driving and load transistors*. In CMOS, this transconductance ratio can be controlled *via* the **W**idth over **L**ength (W/L) ratios of M_1 and M_2 (*Eq.*(5-11)).

In contrast to the absolute accuracy of the transistor parameters (KP, V_{TH}, W,L), a very good device matching is available with modern CMOS processes. The good matching properties are used in many design techniques such as switched capacitor (SC) or switched current (SI) circuits. However, beside the $(W/L)_1/(W/L)_2$ ratio of M_1 and M_2 transistors, the voltage gain G_0 given by *Eq.*(5-11) is a function of unmatched parameters KP_N/KP_P, introducing some uncertainty and temperature drift of the voltage gain.

The voltage gain of CS amplifier *Fig. 5.4* is generally not high enough to satisfy the goal of our prescribed 40 dB value. Following *Eq.*(5-12), the 40 dB voltage gain result in a ratio of $g_{m1}/g_{m2} = 100$. It follows that the dispersion of the transistor dimensions can reach a high value. In other words $(W/L)_1/(W/L)_2$ can be as high as $10\,000\cdot KP_P/KP_N$ (see *Eq.* (5-11)). Obviously, this is unrealistic and the practical voltage gain of *Fig. 5.4* CS amplifier is limited to ca. 20 dB. To reach a 40 dB voltage gain, other design approaches must be considered.

5.3.2 Increasing of the Voltage Gain

i) OTA Fixed Gain Amplifier

The voltage gain, defined as a transconductance ratio, leads us to the use of *Operational Transconductance Amplifiers OTA*. *Fig. 5.5 a)* shows an amplifier where the load transconductance g_{m2} is represented by a simple load resistor $R_L = 1/g_{m2}$. However, the investigation of temperature characteristics $g_{m1}(T)$ and $R_L(T)$ can results in a strong temperature dependence of the voltage gain. The

tel-00417838, version 1 - 17 Sep 2009

temperature dependence of voltage gain can be cancelled when the temperature functions $g_{m1}(T)$ and resistivity $R_L(T)$ become identical. *Fig. 5.5 b)* shows a resistive-connected OTA (g_{m2}) as an active load where constant G_0 results from a naturally good temperature matched $g_{m1}(T)/g_{m2}(T)$ ratio.

The transconductance g_m realized by two CMOS OTAs, is generally related to the bias current as $g_m \approx \sqrt{I_B}$. This dependence extends the possibilities to increase the voltage gain by a constant ratio of bias currents I_{B1} and I_{B2} (besides the geometric scaling of OTA amplifiers). Naturally, a good matching of $I_{B1}(T)/I_{B2}(T)$, provided by an accurate current mirror, is assumed. Such a configuration can be a decent solution in the design of a 40 dB differential amplifier. However, the amplifier based on *Fig. 5.5 b*) requires the integration of two differential OTAs, which is not optimal with respect to the surface saving and power consumption. Moreover, a special care has to be taken of the linearization of the second OTA amplifier (*e.g.* using the techniques shown in [89], [90]).

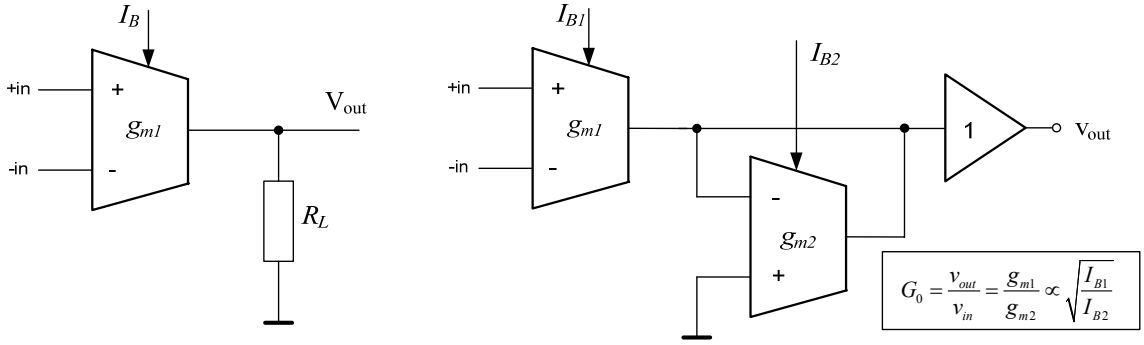


FIG 5.5: *a) Fixed gain amplifier with resistively loaded OTA, b) active load realised by two OTA with a good temperature matching*

ii) Cascading of the Low Gain Amplifiers

Another way to increase the voltage gain is to cascade low gain amplifiers. However, the cascading of the non-differential amplifiers such as *Fig.5.4 a*) common source can be problematic with respect to the DC Operating Point (OP). The setting of the operating point would require a complicated DC feedback network as we can see on CMOS amplifier developed in [57].

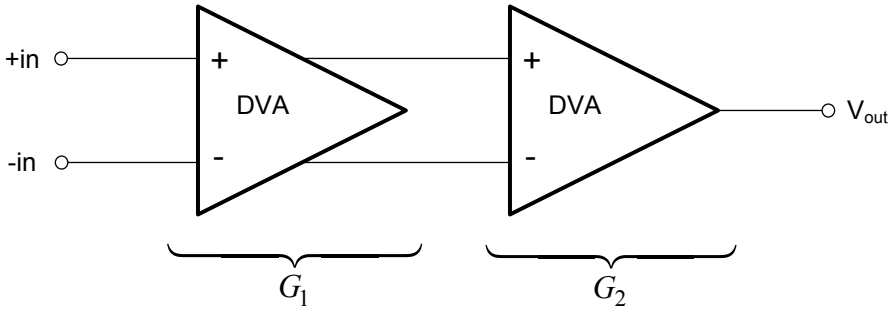


FIG 5.6*: Cascading of low gain Differential Voltage Amplifiers*

On the contrary, the DC accuracy of cascaded differential amplifiers *Fig. 5.6* is dominated by the *offset voltage* of 1st differential pair only. For a classical CMOS, this voltage is generally in the order of several m*V*.

The cascading of low gain differential amplifiers is a widely used technique for the design of VGA, in particular (see [73] for instance). The internal structure is usually based on the input differential pairs loaded by an active load (*e.g.* diode connected MOS transistor). However, the complexity of such amplifiers is similar, when compared to the former two OTA amplifiers configuration *Fig. 5.5 b*), where a linearization of 2nd differential amplifier has to be achieved.

tel-00417838, version 1 - 17 Sep 2009

5.3.3 Adopted Solution: Low g_m Active Load

The main challenge for the design of the fixed gain amplifier is to realise the amplifier with voltage gain which is constant over a wide temperature range. Such gain accuracy is to be achieved simultaneously with the other parameters (defined in *section 5.1*). In order to avoid an unexpected behaviour of the amplifier at cryogenic temperatures, the use of an easy-to-analyze structure is preferred. *For this reason, the previously presented concept of the temperature matched transconductance ratio $g_{m1}(T)/g_{m2}(T)$ will be used. To achieve the 40 dB voltage gain, this ratio has to be increased by load transconductance g_{m2} reaching a low value.*

Fig. 5.7 a) shows the diode connected active load transistor, as shown in previous CS amplifier *Fig. 5.4*. The transconductance can be controlled *via* the *W*/*L* transistor sizing and drain current I_L as:

$$g_{m2} = \sqrt{2 \cdot KP_P \cdot \frac{W_2}{L_2} I_L} \tag{5-14}$$

We have already noticed that a 40 dB voltage gain results in a high dispersion of transistor dimensions (*section 5.3.1, Eq.*(5-11)). The low value of g_{m2} can be achieved with a long transistor, possessing $(W/L) < 1$. However, the utilisation of such transistors is not recommended by the foundry for integration of high accuracy circuits [85].

An interesting solution has been introduced in [80]. The idea presented here is to decrease the transconductance by means of an additional current sink as shown in (*Fig. 5.7 b)*. The new transconductance g'_m is similar to *Eq.*(5-14), where the current I_L is decreased by an (auxiliary) constant current I_{D3}:

$$g'_m = \sqrt{2KP_P \cdot \frac{W_2}{L_2}\left(I_L - I_{D3}\right)}\,. \tag{5-15}$$

However, a considerable decrease of transconductance g_{m1} can be provided when the drain current I_{D3} exceeds the I_{D2} significantly. In other words, we can write $I_{D3} = k \cdot I_L$, where k is close to unity ($k < 1$). The equivalent transconductance (5-15) can be then expressed in terms of k:

$$g'_m = \sqrt{2KP_P \cdot \frac{W_2}{L_2} I_{D1}\left(1-k\right)}\,. \tag{5-16}$$

FIG. 5.7: *a) Diode connected P-MOS transistor with transconductance g_m, b) Diode connected MOS transistor with decreased transconductance g'_m [80]*

We can demonstrate that the value of k close to unity has a negative impact on the accuracy of the transconductance and the resulting voltage gain. This can be expressed by the "relative sensitivities" defined as:

$$S_k^{g'_m} = \frac{\partial g'_{m(k)}}{\partial k} \cdot \frac{k}{g'_{m(k)}} = -\frac{1}{2}\frac{k}{1-k}\,. \tag{5-17}$$

tel-00417838, version 1 - 17 Sep 2009

The value of $S_k^{g'_m}$ can reach an important value for k close to unity. The accuracy of the gain setting must be therefore provided by an another active element, avoiding such terms similar to (5-16).

5.3.4 Low g_m Composite Transistor

The transconductance g_m for voltage V_{GS} and current I_L biased MOS transistor was previously introduced as:

$$g_{m2} = KP_P \frac{W_2}{L_2} \cdot \left(V_{GS} - \left| V_{THP} \right| \right) = \sqrt{2KP_P \frac{W_2}{L_2} I_L} \,. \tag{5-18}$$

Basically, the expression of transconductance (5-18) has three degrees of freedom: W/L ratio and values of V_{GS} voltage or bias (drain) current I_L. It has been shown that use of the scaling by W/L is not an accurate way to reach the 40 dB voltage gain and the scaling using the bias current (*Fig. 5.7 b*) has the sensitivity limits. On this account, we use the *scaling of the V_{GS} voltage of a diode connected transistor in such way that $V_{GS} = \eta \cdot V_{DS}$, where $\eta < 1$.*

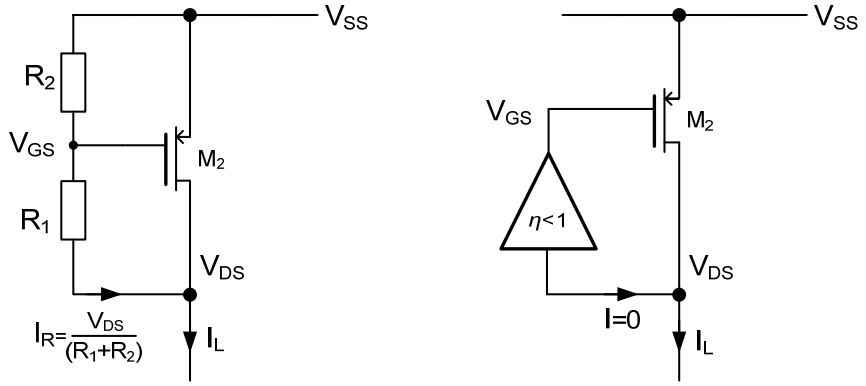


FIG. 5.8: *a) Decreasing of transconductance by the V_{GS} voltage scaling, b) high impedance drain voltage sensing by an attenuator with $\eta < 1$*

The voltage scaling can be carried out by a voltage divider as shown in *Fig. 5.8 a)*. Here the R_1 and R_2 provide the division of the drain voltage so that $V_{GS}/V_{DS} = \eta = R_2/(R_1+R_2)$. For a given voltage V_{DS}, the drain current is decreased to a new value:

$$I_L = \frac{KP_P}{2} \frac{W_2}{L_2} \left(\eta \cdot V_{DS} - \left| V_{THP} \right| \right)^2 + \frac{V_{DS}}{R_1 + R_2} \,. \tag{5-19}$$

The output resistance in the output node of *Fig. 5.8 a*) can be defined by (2-25). In order to provide an equivalence with a single transistor having a low transconductance, the value of output resistance will be labelled as g'_m . Its value can be written:

$$g'_m = \frac{\partial I_L}{\partial V_{DS}} = \eta \cdot KP_P \frac{W_2}{L_2} \cdot \left(\eta \cdot V_{DS} - \left| V_{THP} \right| \right) + \frac{1}{R_1 + R_2} \,. \tag{5-20}$$

Accordingly, the constant η is a parameter allowing to reduce the transconductance of transistor M_2. However, this decrease of transconductance is limited by the second term in *Eq.* (5-19) due to the additional current I_R. This term can be removed by using a high impedance (voltage) sensing of the M_2 drain voltage. Such high impedance sensing is depicted in *Fig. 5.8 b)* where the scaling of drain voltage is provided by a high input impedance attenuator with voltage attenuation $\eta < 1$.

tel-00417838, version 1 - 17 Sep 2009

Fig. 5.9 shows an implementation CMOS of a low transconductance composite transistor based on the concept of *Fig. 5.8 b)*, with high impedance $V_{D(M1)}$ voltage sensing. The voltage transfer η is provided by the common source amplifiers built from the M_2 to M_5. These amplifiers provide a voltage gain equal to the gain of CS amplifier (*Fig. 5.4*). For convenience, however, the technique of current scaling' provided by $M_{3\text{-}4}$ and $M_{5\text{-}1}$ current mirrors) will be used for the behaviour description of the circuit.

In the following section, the composite transistor (*Fig. 5.9*) will be examined in order to demonstrate the method of transconductance setting by using the current scaling techniques.

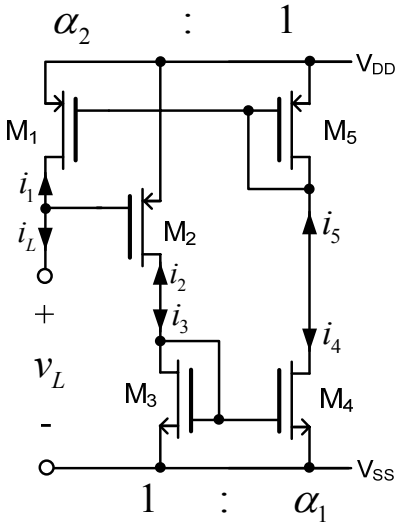


FIG. 5.9: *Low transconductance composite transistor*

5.3.5 Analysis of the Low g_m Composite Transistor

In order to determine the gain of an amplifier following *Eq.*(5-12), the equivalent small signal transconductance g'_m of the low transconductance composite transistor is the first parameter to be analysed.

The architecture analysis can be based on two different (previously mentioned) approaches: ***voltage and current scaling***. The voltage scaling uses two Common Source amplifiers (M_2, M_3 and M_4, M_5) with diode connected active loads (M_3, M_5). These CS amplifiers provide an attenuation $\eta = V_{GS2}/V_{DS5}$ analogous to that two serially connected CS amplifiers (*Fig. 5.8 b*).

The current scaling allows the description of the composite transistor as the circuit in *Fig. 5.9*, where the M_2 drain current is decreased by two *current mirrors* $M_{3\text{-}4}$ and $M_{5\text{-}1}$. This principle is to be further applied in order to derive the value of the small signal transconductance g'_m.

Small Signal transconductance g'_m

The equivalent transconductance g'_m of the diode connected composite transistor *Fig. 5.9* is defined by Ohm's law:

$$g'_m = \frac{i_L}{v_L} \ . \tag{5-21}$$

Transistor M_2 is a voltage controlled current source, with drain current i_2 equal to:

$$i_2 = g_{m2} \cdot v_L \ . \tag{5-22}$$

tel-00417838, version 1 - 17 Sep 2009

We can identify two current mirrors composed of M_3, M_4 and M_5, M_1. These current mirrors scale the output current so that $i_{out} = \alpha \cdot i_{in}$, where α is the scaling factor given by transconductance ratio:

$$\alpha_1 = \frac{g_{m4}}{g_{m3}} = \frac{W_4/L_4}{W_3/L_3} \quad \text{and} \quad \alpha_2 = \frac{g_{m1}}{g_{m5}} = \frac{W_1/L_1}{W_5/L_5}. \tag{5-23}$$

The input current i_3 of the 1st current mirror is given by M_2 drain current (5-22), so the i_4 can be written as:

$$i_4 = \alpha_1 \cdot i_3 = g_{m2} \cdot \frac{g_{m4}}{g_{m3}} \cdot v_L. \tag{5-24}$$

In the same way, the output current i_L can be written in terms of the product of $\alpha_1 \cdot \alpha_2$:

$$i_L = \alpha_1 \cdot \alpha_2 \cdot i_3 = g_{m2} \cdot \frac{g_{m4} \cdot g_{m1}}{g_{m3} \cdot g_{m5}} \cdot v_L, \tag{5-25}$$

resulting in the equivalent transconductance $g_m^{'}$:

$$\boxed{g_m^{'} = \frac{i_L}{v_L} = g_{m2} \cdot \frac{g_{m4} \cdot g_{m1}}{g_{m3} \cdot g_{m5}} = \alpha_1 \cdot \alpha_2 \cdot g_{m2}}. \tag{5-26}$$

It appears that the *Fig. 5.9* realise a composite diode connected transistor equivalent to the transistor M_2 with transconductance decreased by a factor $\alpha_1 \cdot \alpha_2 < 1$. In this expression, the transconductance g_{m2} is controlled by DC gate-to-source voltage V_{GS2}. We can also determine the equivalent transconductance for the circuit biased by DC current I_L. This make appear a term $\sqrt{(\alpha_1 \cdot \alpha_2)}$:

$$g_m^{'} = \sqrt{\alpha_1 \, \alpha_2} \cdot \sqrt{2 \cdot KP_P \cdot \frac{W_2}{L_2} \cdot I_L}. \tag{5-27}$$

The difference between (5-26) and (5-27) results from the difference between the current and voltage biased transistor, such as shown in *Eq.*(5-18). In the both equations (5-26) and (5-27), the terms *W/L,* related to M_1-M_5 transistors, are expressed as the identical product. In other words, the equations (5-26) and (5-27) can be written as the function of V_{GS} and I_L and the transistor parameters as:

$$g_m^{'} = KP_P \cdot \frac{W_2}{L_2} \cdot \left(\frac{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}} \right) \left(|V_{GS2}| - |V_{THP}| \right) = \sqrt{2 \cdot KP_P \cdot \frac{W_2}{L_2} \cdot \left(\frac{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}} \right) \cdot I_L}, \tag{5-28}$$

where $(V_L = V_{DD} - V_{GS2})$. This expression illustrates that the transconductance of the composite transistor results from the product of geometrical ratios W_i/L_i of M_1 to M_5 transistors.

Large Signal Analysis

The analysis of the DC operating point requires to establish the relationship between the DC bias current I_L and the terminal voltage V_{out} of the low g_m composite transistor (*Fig. 5.9*). The analysis can be provided in the same way as compared with previous analysis: by investigating the DC drain (saturation) current of M_2, scaled by M_3, M_4 and M_5, M_1 current mirrors. It results in the large signal characteristics - functions of I_L and V_{GS2}:

tel-00417838, version 1 - 17 Sep 2009

$$|V_{GS2}| = \sqrt{\frac{2}{KP_P\left(\frac{W_2}{L_2}\right)}\cdot\left(\frac{\frac{W_3}{L_3}\cdot\frac{W_5}{L_5}}{\frac{W_4}{L_4}\cdot\frac{W_1}{L_1}}\right)\cdot I_L} + |V_{THP}|; \qquad I_L = \frac{KP_P}{2}\cdot\frac{W_2}{L_2}\cdot\left(\frac{\frac{W_4}{L_4}\cdot\frac{W_1}{L_1}}{\frac{W_3}{L_3}\cdot\frac{W_5}{L_5}}\right)\cdot\left(|V_{GS2}| - |V_{THP}|\right)^2 \quad (5\text{-}29)$$

Properties of Composite Transistor: Summary

It has been demonstrated that both small signal and large signal characteristics of the composite transistor are determined by M_2 transistor and scaling factors α_1 and α_2.

An important point to be considered during the design is the static drain current of M_2. This current can exhibit a high variation, in function of the operating point. It is important parameter related to the power consumption of the composite transistor.

To provide a high accuracy of the equivalent transconductance g'_m, the second order effects (velocity saturation, channel length modulation etc., see *chapter 2*), must be reduced. This can be done by a proper choice of transistor dimensions, in particular by keeping the transistor channel *L* length above ca. 2 µm.

The structure in *Fig. 5.9* is only operating for $\eta < 1$, whereas the factor $\eta > 1$ causes the device saturation. Although the circuit is presented as an active load (diode), the gate of M_2 can be disconnected in order to create a classical three terminal low g_m composite transistor, as shown in further *section 5.6.2*). The detailed analysis (AC, noise etc) will be provided in the following *chapter 6*.

5.3.7 Common Source Amplifier with Low g_m Load

In order to reach reasonable dimensions of transistors used in the CS amplifier (*Fig. 5.4*), the voltage gain is limited to some 20 dB. This voltage gain can be increased by applying the diode connected low g_m transistor as the active load of the amplifier. This is depicted in *Fig. 5.10* where the driving transistor M_D is loaded by M_1-M_5 low g_m composite transistor.

The linearized voltage gain G_0 can be derived as the v_{out}/v_{in} voltage transfer, where v_{out} is the voltage drop on the low g_m load caused by the drain current:

$$i_D = -g_{mD}\cdot v_{in}\,. \quad (5\text{-}30)$$

Here, the g_{mD} is the transconductance of M_D: $g_{mD} = \sqrt{2KP_N W_D/L_D}\cdot\sqrt{I_D}$. As i_D and i_L are equal, the output voltage can be obtained as:

$$v_{OUT} = -\frac{i_L}{g'_m}\cdot = -\frac{v_{in}\cdot g_{mD}}{\sqrt{\alpha_1\,\alpha_2}\cdot\sqrt{2\cdot KP_P\cdot\frac{W_2}{L_2}\cdot I_L}}, \quad (5\text{-}31)$$

where the numerator term is a substitution of (5-27). By inserting $g_{mD} = \sqrt{2KP_N W_D/L_D}\cdot\sqrt{I_D}$ in the previous equation, the voltage gain v_{out}/v_{in} can be obtained as the following function:

$$G_0 = -\frac{g_{mD}}{\sqrt{\alpha_1\,\alpha_2}\cdot\sqrt{2\cdot KP_P\cdot\frac{W_2}{L_2}\cdot I_D}} = -\frac{1}{\sqrt{\alpha_1\cdot\alpha_2}}\sqrt{\frac{KP_N}{KP_P}}\sqrt{\frac{W_D/L_D}{W_2/L_2}}\,. \quad (5\text{-}32)$$

tel-00417838, version 1 - 17 Sep 2009

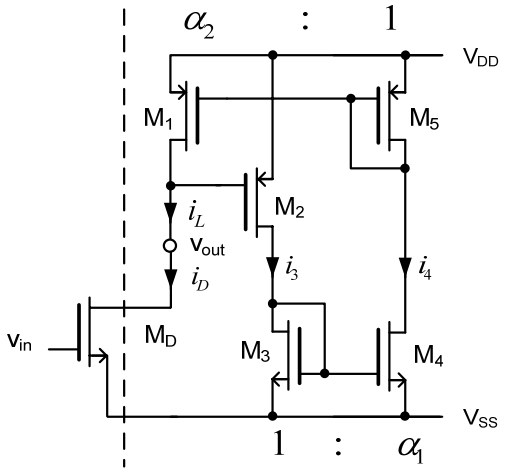


FIG. 5.10: *Common source amplifier with Fig. 6.9 low g_m composite transistor as the load*

We can see that G_0 is fixed only by transistor dimensions and by KP_N/KP_P ratio, which is in fact related to the electron to hole mobility ratio [22].

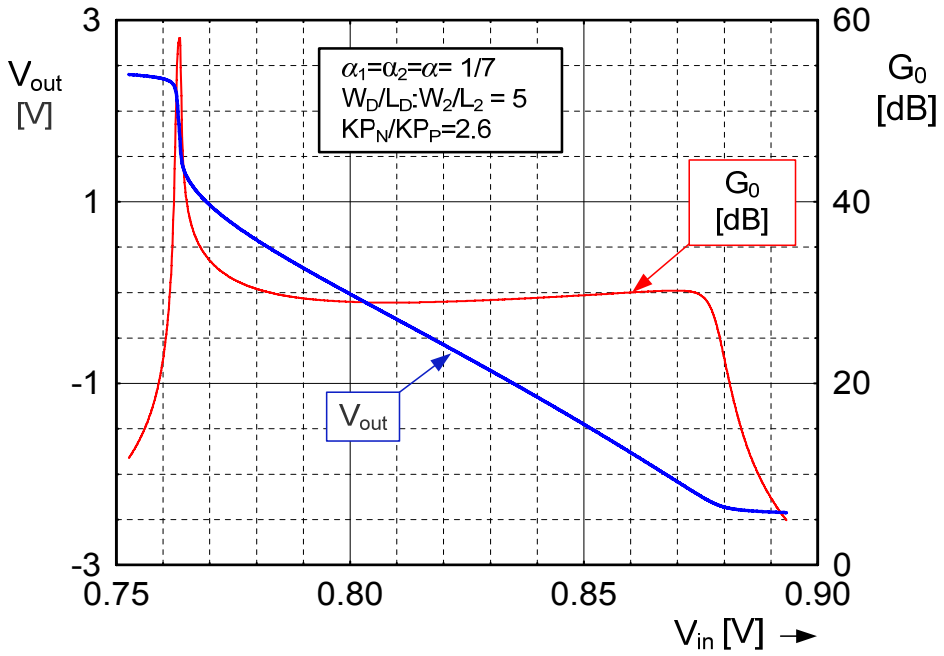


FIG. 5.11: *Static DC characteristics of Fig. 5.10 CS amplifier with plotted dV_{out}/dV_{in} voltage gain*

The value of the voltage gain can be compared with (5-11) where an increase by $(\alpha_1 \cdot \alpha_2)^{-½}$ in (5-32) can be observed. An example of simulated characteristics of amplifier from *Fig. 5.10*, designed for $G_0 = 28$ dB, is shown in *Fig 5.11*. The amplifier characteristic is quasi-linear in a wide range of input voltages and is only realised with *very reasonable dimensions of the transistors.*

However, the KP_N/KP_P in (5-32) can have a negative impact to the accuracy of the amplifier gain and its temperature evolution. This term is eliminated in the design of the two following amplifiers:

- **Amplifier with G_0 fixed by transistor geometric ratio;**
- **Amplifier with temperature compensated voltage gain.**

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

5.4 Differential Pair and Cascode Effect

The ways allowing a design of a fixed gain amplifier with accurate voltage gain has yielded a "robust" circuit, conditioned by only three parameters: W/L ratios, I_{BIAS}. It follows that all secondary parameters subject to affect the voltage gain (*e.g.* the channel length modulation) have to be removed by virtue of a proper design and the choice of component values.

The common source architecture with low g_m composite transistor (*section 5.3.8*) exhibits a voltage gain, depending on the gain factors KP_N/KP_P. The way to remove this KP_N/KP_P factor is to make it equal to unity. Such compensation can be carried out by using the driving and load transistors, both of the same channel type. This can be achieved by employing the driving transistor M_D of P-channel type and to "fold" the i_{D1} (i_L) current either by means of a simple current mirror or by using a differential *folded cascode* [22] configuration.

5.4.1 Cascode and Folded Cascode

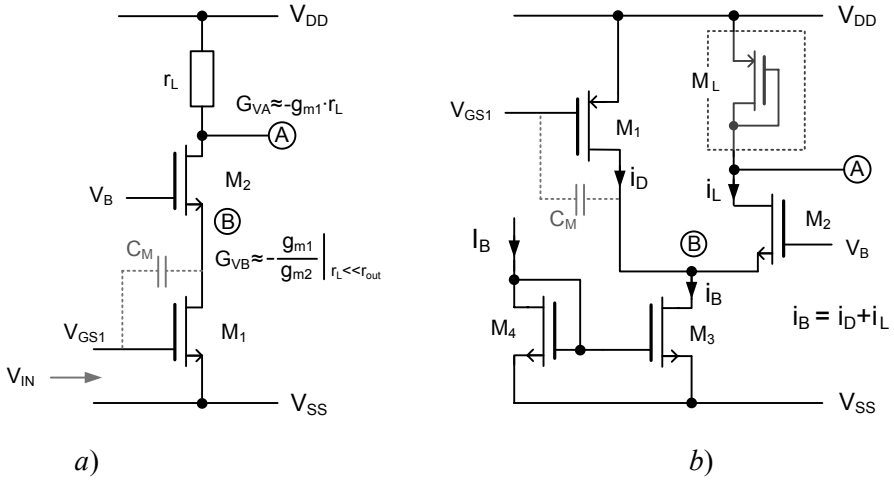
The cascode is a very useful structure in the design of CMOS and bipolar integrated circuits [16]. Generally, the design employs two components: input transistor M_1 and cascode transistor M_2. The benefits improving the circuit performances are following:

- **Reducing of the channel length modulation (r_{DS});**
- **Decreasing of the Miller capacitance C_M**

These properties are frequently called as *cascode effects,* and they will be thoroughly examined in the following section. Beyond the elimination of r_{DS} and C_M, the folded cascode amplifier would present an effective (mentioned) way to remove the KP_N/KP_N term from (5-32). Also it avoids the *cascading of the transistors,* as compared to the telescopic cascode. This is an important issue for operations under a low supply voltage V_{DD}.

The cascode using the MOS transistors is presented in *Fig. 5.12 a)*, as a simple and *Fig. 5.12 b)* folded cascode configuration. The both circuits contain one driving (M_1) and one cascode transistors (M_2). The load resistance r_L and (M_L) shown in *Fig. 5.12* are not considered as the active part of cascode and its significance will be discussed later.

The current through drain resistance i_{rDS1} is determined by v_{DS} voltage as v_{DS1}/r_{DS1}. However, this voltage v_{DS1} is relatively high for the common source amplifier. The cascode circuit makes its *relatively low, fixed by voltage follower: cascode transistor M_C.* This causes the drain voltage of M_1 standing almost constant (fixed by V_B) resulting in a lower current through r_{DS1} and C_M [22].



a) *b*)

FIG. 5.12: *a) Simple (telescopic) cascode and b) folded cascode (r_{out} defined in Eq. (5-35))*

Cascode Effect

The need of decreasing the parasitic resistance r_{DS} is evident in *Eq.*(5-13), where the channel length modulation affects the accuracy of the gain. By using the folded cascode, the voltage gain is ideally only determined by the transconductance of the driving transistor g_{mD} and load resistance r_L.

Both circuits from *Fig. 5.12 a)* and *b)* can be transformed into the equivalent linear model *Fig. 5.13* in order to demonstrate the above mentioned features of the cascode effect. By applying Thevenin's theorem, *Fig. 5.12* circuits can be transformed into an equivalent current source of value i_{CC} and resistance r_{out}.

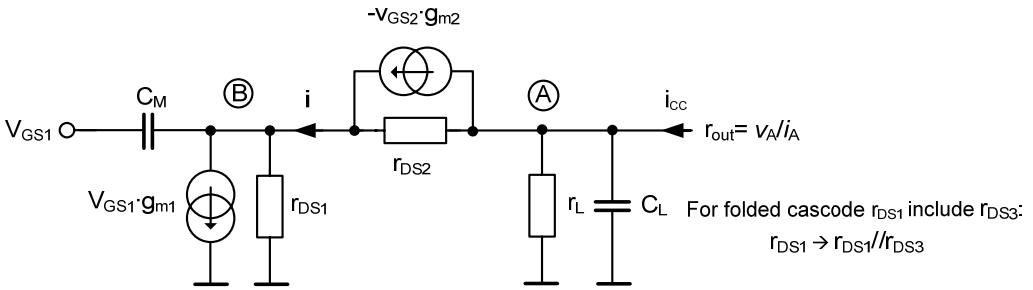


FIG. 5.13: *Linearized model of the simple and folded cascode structure. The r_{DS1} includes also the output resistance r_{DS3} of folded cascode Fig. 5.12 b). The substrate transconductance g_{DS} of M_C was neglected.*

Focusing only to the low frequency behaviour, the nodal equations of circuit from *Fig. 5.13* can be written as:

$$i_{CC} = g_{mD} \cdot v_{in} - \frac{v_B}{r_{DS1}} \quad \text{and} \quad i_{CC} = -v_B \cdot g_{mC} + \frac{v_B}{r_{DS2}}, \tag{5-33}$$

where the r_{DS2} is represented by the output resistance of M_C for the simple cascode and by $r_{DS2}//r_{DS3}$ for the folded cascode. The output current can be expressed using *Eq.*(5-33) as:

$$i_{CC} = v_{GS1} \cdot g_{m1} \cdot \frac{r_{DS1}\left(1 + r_{DS2} \cdot g_{m2}\right)}{r_{DS2} + r_{DS1}\left(1 + r_{DS2} \cdot g_{m2}\right)}, \tag{5-34}$$

and the output resistance for zero input voltage and the disconnected load resistance can be obtained:

$$r_{out} = r_{DS2} + \underbrace{\left(1 + g_{m2} r_{DS2}\right)}_{>>1} r_{DS1}. \tag{5-35}$$

These two equations show the 1st cascode effect: the resistance appearing in the output node (drain of M_2) is increased by the term $(1 + g_{m2}r_{DS2})$, reaching some tens in CMOS and about hundred in the bipolar technology. This term can be found in almost all expressions dealing with cascode configuration, as *Eq.*(5-34), for instance.

The load resistance r_L, connected to the cascode output node, is in parallel with r_{out}. By applying an input voltage, the voltage gain available at the output node can be written as a function of $r_{out}//r_L$:

$$G_0 = \frac{\left(r_{out} // r_L\right) \cdot i_{CC}}{v_{in}} \cong \left.\frac{r_L \cdot i_{CC}}{v_{in}}\right|_{r_L << r_{out}}, \tag{5-36}$$

which can be expressed from (5-34) and (5-35) as:

tel-00417838, version 1 - 17 Sep 2009

$$G_0 = -g_{m1}\frac{\left(1+g_{m2}\cdot r_{DS2}\right)r_{DS1}\cdot r_L}{\left(1+g_{m2}\cdot r_{DS2}\right)\cdot r_{DS1}+r_{DS2}+r_L} \cong -g_{m1}\cdot r_L\big|_{r_L<<r_{out}}. \qquad (5\text{-}37)$$

The last simplification can be done within a negligible error only for $r_L << r_{out}$. This is ensured by low g_m transistor from *Fig. 5.9* ($r_L=1/g'_m$) of which the transconductance is in order of tens of μS.

The elimination of the channel resistances is common in the design of Operating Amplifiers, where the gain is to be very high (≈ 80 - 120 dB). This can be achieved in the model *Fig. 5.13* by replacing M_L by an active load - current source (so r_L is only given by $r_{DS} \sim 1/\lambda I_D$). The gain of such an amplifier can be written as:

$$G_0 \cong -g_{mD}\cdot r_L = -\frac{1}{\lambda}\cdot\sqrt{\frac{2KP_N}{I_D}\frac{W_1}{L_1}}. \qquad (5\text{-}38)$$

Here, λ refers only to the channel length modulation of the load transistor.

The second important effect arising from the use of a cascode structure is the *reduction of the Miller capacitance* which value affects the AC characteristics of the amplifier [86]. On can deduce that a high load resistance r_L of *Fig. 5.13* sets the dominant pole p_1 to frequency $\sim 1/r_L C_L$. This is true for a low output impedance signal source. For a high impedance source the dominant pole can appear at frequency $\sim 1/r_{in}C_M$, resulting from the source resistance and increased Miller capacitance C_M (see *chapter 4.4.1*). However, in *Fig. 5.12* and *Fig. 5.13*, the voltage a terminal (B) remains relatively low, maintained by the cascode transistor M_C. The low voltage at this node causes the current *via* C_M to decrease and consecutively, to reduce the impact of the capacity C_{GD}. This is the 2nd important cascode effect to be exploited in the amplifier design.

The transconductances of driving (D) and load (*e.g.* diode connected) transistors (L) in *Fig. 5.12 a)* are provided by an identical bias current. On the contrary, the transconductances g_{m1} and g_{m2} of the folded cascode are function of unequal currents I_D and I_L ($I_L = I_B - I_D$) and the voltage gain can be expressed also by means of these currents I_L and I_D:

$$G_0 = \left|\frac{g_{m1}}{g_{mL}}\right| = \frac{\sqrt{2KP_P\left(W_D/L_D\right)\cdot I_D}}{\sqrt{2KP_P\left(W_L/L_L\right)\cdot I_L}} = \sqrt{\frac{W_D/L_D}{W_L/L_L}}\cdot\sqrt{\frac{I_D}{I_L}}, \qquad (5\text{-}39)$$

where the current ratio can contribute to the high value of voltage gain G_0. Naturally, this term must be provided by an accurate current mirror. Equation (5-39) is an important point for the design of amplifiers where a high accuracy of the voltage gain constant over a wide temperature range is required: G_0 is determined by transistor geometric dimensions only and is no longer function of KP_N/KP_P.

In contrast to the operational amplifiers, the reduced r_{ds} is not important for the high value of the gain, but is an important condition to reach the high gain accuracy. To demonstrate this effects, we can present the result obtained with the 1st amplifier (*Tab.5.7*), where the transconductance of driving transistors (differential pair) reaches g_{mD}=2.04 mS, composite load g'_m=20.5 μS and the drain channel conductance the value of 6.04 μS. The simulated conductance $1/r_{out}$ in the output node of amplifier *Fig. 5.18* is then decreased to 723 pS.

5.4.2 MOS Input Differential Pair

The differential gain of an amplifier can be provided by a cell including two driving transistors M_D, called *differential pair* [22]. This differential pair removes the common voltage appearing at the transistors gates and delivers the output current proportional to the *input differential voltage*. As we have shown in the previous section, the folded cascode configuration *Fig. 5.12 b)* allows to accurately

tel-00417838, version 1 - 17 Sep 2009

define the output current of the driving transistors $i_{D1,2}$, which value is not (or very little) affected by channel length modulation (value r_{DS}). This conclusion can be applied to the *differential folded cascode* for which the input differential pair will be now analysed.

Fig. 5.14 shows the input differential pair (transistors M_{D1}, M_{D2}) as folded cascode transconductance amplifier. To ensure the symmetry, we assume furthermore that M_{D1} and M_{D2} are identical, as well as M_{C1} and M_{C2}. In the following, the notation β, KP, $g_{m1,2}$ as well as W_D and L_D refers to the transistors M_{D1} and M_{D2}.

The differential input pair acts as a voltage controlled current source (or *differential transconductor*) characterized by a transconductance g_{mDiff}. This transconductance results from the DC characteristic $I_{D1} = f(V_{IN})$ and is important with respect to the V_{out}/V_{in} voltage transfer of the amplifier.

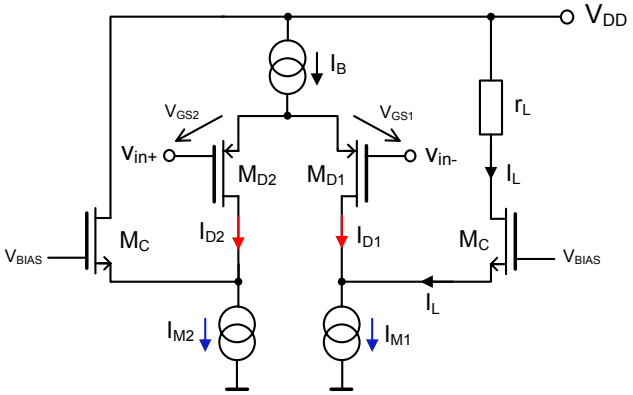


FIG. 5.14: *Input differential pair in the folded cascode configuration*

We will refer to V_{GS1} and V_{GS2} as the gate-to-source voltages of input transistors M_{D1} and M_{D2} and ΔV_{GS} as the differential input voltage $V_{GS1} - V_{GS2}$. For zero ΔV_{GS} voltage, the overall bias current I_B is divided symmetrically into I_{D1} and I_{D2} currents, so $I_{D1} = I_{D2} = I_B/2$. For an applied ΔV_{GS} voltage, the KCL (Kirchhoff Current Law) results in the difference between currents I_{D1} and I_{D2}:

$$\Delta V_{GS} = V_{GS1} - V_{GS2} = \sqrt{\frac{2I_{D1}}{\beta}} - \sqrt{\frac{2I_{D2}}{\beta}} = \sqrt{\frac{2}{\beta}} \cdot \left(\sqrt{I_{D1}} - \sqrt{I_{D2}}\right), \tag{5-40}$$

where β is the transistor "gain" $KP \cdot (W/L)$ of transistors M_D. The bias current I_B maintains the sum of currents $I_{D1}+I_{D2}$ constant, so that the ΔV_{GS} can be expressed in terms of I_{D1} and I_B as:

$$\Delta V_{GS} = V_{GS1} - V_{GS2} = \sqrt{\frac{2}{\beta}} \left(\sqrt{I_{D1}} - \sqrt{I_B - I_{D1}}\right), \tag{5-41}$$

where the current I_{D1} can be developed in a quadratic form:

$$I_{D1}^2 - I_B I_{D1} + \frac{1}{4}\left\{I_B^2 - I_B \beta_D \cdot \Delta V_{GS}^2 + \left(\frac{\beta \cdot \Delta V_{GS}^2}{2}\right)^2\right\} = 0, \tag{5-42}$$

$$I_{D1} = \frac{1}{2} I_B \pm \frac{1}{2}\sqrt{\frac{2I_B \Delta V_{GS}^2}{\left(\frac{2}{KP} \cdot \frac{L_D}{W_D}\right)^2} - \frac{\Delta V_{GS}^4}{\left(\frac{2}{KP} \cdot \frac{L_D}{W_D}\right)^4}} = \frac{1}{2} I_B + \frac{1}{4}\sqrt{\underbrace{KP \frac{W_D}{L_D} V_{GS}^2}_{b}} \cdot \sqrt{\underbrace{4I_B - \underbrace{KP \frac{W_D}{L_D} \Delta V_{GS}^2}_{b}}_{a-b}} \tag{5-43}$$

tel-00417838, version 1 - 17 Sep 2009

where by applying the identity $\left(\sqrt{a-b}+\sqrt{b}\right)^2 = a-b+2\sqrt{b}\sqrt{a-b}+b$, the I_{D1} expression results in:

$$I_{D1} = \frac{1}{8}\cdot\left(\sqrt{4\cdot I_B - KP\cdot\frac{W_D}{L_D}\cdot\Delta V_{GS}^2} + \sqrt{KP\cdot\frac{W_D}{L_D}}\cdot\Delta V_{GS}\right)^2. \tag{5-44}$$

We can now determine the load current I_L (*Fig. 5.14*). This current is solely a linear translation of (5-44) by current I_{M1}, so that:

$$I_L(\Delta V_{GS}) = I_{M1} - I_{D1}(\Delta V_{GS}). \tag{5-45}$$

For zero input voltage (ΔV_{GS}=0) the value of $I_{L,Q}$ is a function of static bias currents I_M and I_B only: $I_{L,Q} = I_B/2 - I_M$. By plotting the characteristics $I_L = f(\Delta V_{GS})$, a nearly ideal straight line is obtained for small values of V_{IN} (*Fig. 5.15 a*), in spite of the complicated expression *Eq.*(5-45). The characteristics *Fig. 5.15 a*) was plotted for the predicted values (W=1000 µm, L=2 µm, I_B=500 µA, I_{M1}=275 µA) where $I_{L,Q}$=25 µA.

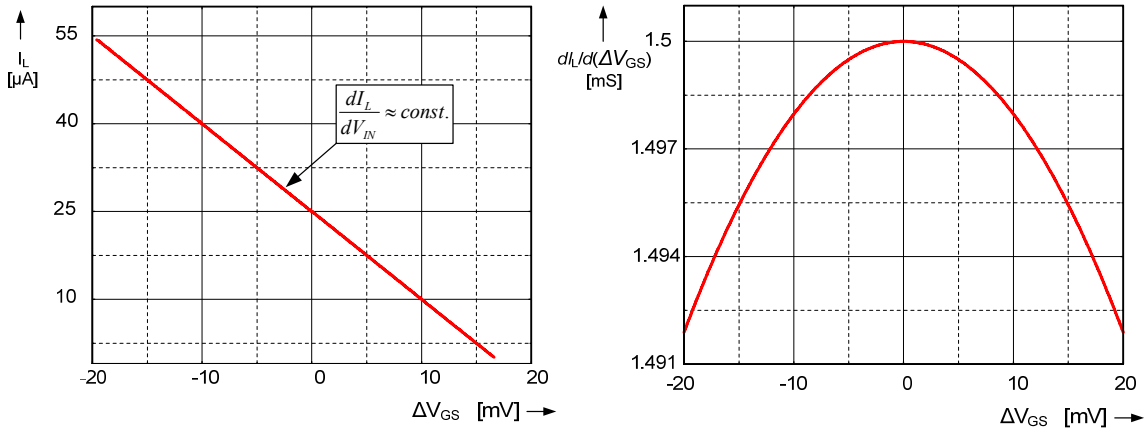


FIG. 5.15: *a) Static characteristics $I_L/\Delta V_{GS}$ and b) its derivation, equivalent to the transconductance of the differential pair*

The linearity of $I_L = f(\Delta V_{GS})$, plotted in *Fig. 5.15 a*), can be investigated from $dI_{D1}/d\Delta V_{GS}$, corresponding to the transconductance of the input differential pair $g_{mDiff} = f(\Delta V_{GS})$:

$$\frac{dI_{D1}}{d\Delta V_{GS}} = \frac{1}{2}\cdot\sqrt{KP\cdot\frac{W_D}{L_D}}\,\frac{\left(2\cdot I_B\cdot L_D - KP\cdot W_D\cdot\Delta V_{GS}^2\right)}{\sqrt{4\cdot I_B\cdot L_D^2 - KP\cdot W_D\cdot L_D\cdot\Delta V_{GS}^2}}, \tag{5-46}$$

where W_D/L_D refers to transistors M_{D1} and M_{D2}. This derivation is plotted for the identical (previously mentioned) values in *Fig. 5.15 b*). We can observe that inside the ±15 mV input voltage range, the transconductance varies by 0.33% which allows to consider the input differential pair as a *quasi-linear voltage controlled current source*. Hence this assumption remains valid just for relatively small ΔV_{GS} voltages.

The linearized current gain (differential transconductance g_{mDiff}) can be determined for zero ΔV_{GS} input voltage directly from *Eq.*(5-46):

$$g_{mDiff} = \left.\frac{dI_{D1}}{d\Delta V_{GS}}\right|_{\Delta V_{GS}=0} = \frac{1}{2}\cdot\sqrt{KP_P\cdot\frac{W_D}{L_D}\cdot I_B}. \tag{5-47}$$

tel-00417838, version 1 - 17 Sep 2009

and it appears to be half the value of transconductance (*Eq.*(2-26)). The linearized (small signal) transconductance of MOS differential pair can be consequently expressed for $\Delta V_{GS} = 0$ as:

$$g_{mDiff} = \frac{1}{2} g_{m1,2}\,, \tag{5-48}$$

where $g_{m1,2}$ are the transconductances of both input transistors M_{D1} and M_{D2} ($g_{m1} = g_{m2}$). As we can perceive from this, the factor ½ penalizes the current gain of the final differential amplifier; in consequence, resulting in 4 times larger *W*/*L* ratio, when compared to the identical gain of simple CS (*Fig. 5.4*) amplifier. This is obvious, because both M_D transistors are "serially connected". The additional analysis (noise and AC) of the differential folded cascode transconductor will be provided in the following chapter *6*.

5.5 Amplifier with Low g_m Composite Transistor

The structure of our high, fixed gain differential amplifier can be derived from *Fig. 5.14* by replacing the load r_L by a low g_m composite transistor, as depicted in *Fig. 5.9*. The resulting circuit based on the input differential folded cascode transconductor (input transistors M_D and cascode transistors M_C) and M_1-M_5 low g_m composite transistor (diode connected) as the active load, is shown in *Fig. 5.16*. The amplifier is biased by I_B and $I_{M1,2}$ current sources. In the following, this amplifier will be labelled as *type I*, *geometric ratio fixed gain amplifier*.

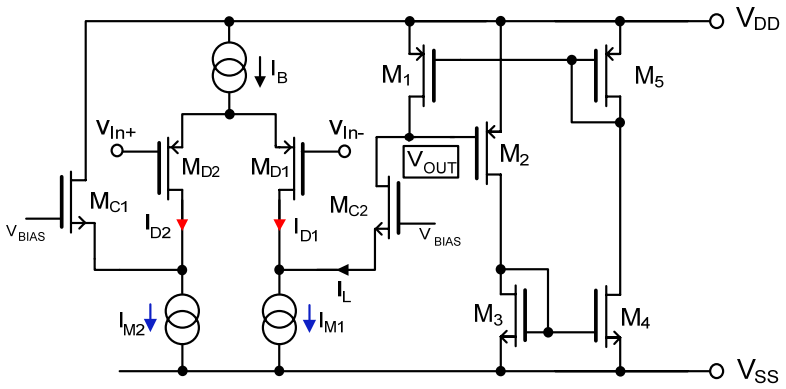


FIG. 5.16: *Type I folded cascode amplifier with low g_m composite load (Fig. 5.9)*

The DC V_{OUT}/V_{IN} characteristics can be expressed as a function of the load current I_L (5-44), delivered by the input differential pair and the *I*-*V* characteristics (5-29) of the low g_m composite transistor. We obtain the output voltage of the amplifier in the following form:

$$V_{OUT} = V_{DD} - |V_{THP}| - \sqrt{\frac{2}{KP_P \cdot \left(\frac{W_2}{L_2}\right)} \cdot \left(\frac{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}}{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}} \right) \cdot \left[I_{M1} - \frac{1}{8} \cdot \left(\sqrt{4 \cdot I_B - KP_P \cdot \frac{W_D}{L_D} \cdot \Delta V_{GS}^2} + \sqrt{KP_P \cdot \frac{W_D}{L_D}} \cdot \Delta V_{GS} \right)^2 \right]}\,. \tag{5-49}$$

This DC transfer relationship describes the basic properties of amplifier as a static V_{in}/V_{out} characteristic and the voltage gain. Obviously, the form (5-49) can be simplified by introducing the *effective width to length ratio* W_{eff}/L_{eff} of the low g_m composite transistor:

$$\frac{W_{eff}}{L_{eff}} = \left(\frac{W_2}{L_2}\right) \left(\frac{\frac{W_4}{L_4} \cdot \frac{W_1}{L_1}}{\frac{W_3}{L_3} \cdot \frac{W_5}{L_5}} \right) = \alpha_1 \cdot \alpha_2 \cdot \frac{W_2}{L_2}\,. \tag{5-50}$$

tel-00417838, version 1 - 17 Sep 2009

By considering the differential pair as a quasi-linear ΔV_{GS} controlled current source I_L (*Fig. 5.15*), Eq. (5-50) can be rewritten as:

$$V_{OUT} = V_{DD} - |V_{THP}| - \sqrt{\frac{2}{KP_P} \cdot \frac{L_{eff}}{W_{eff}} \cdot I_L}\ , \tag{5-51}$$

where I_L is the load current (5-45). As it can be seen from *Fig. 5.19*, the linearity is suitable for small signals (low noise amplifiers do deal with the small signals) and acceptable for large signals.

The voltage gain is related to the transconductance of the differential input pair $dI_L/d\Delta V_{GS}$ (5-46) and to the *I-V* characteristic of the low g_m composite transistor (5-29). We can define the voltage gain as:

$$G_0 = \frac{dV_{OUT}}{d\Delta V_{GS}} = \frac{dI_L}{d\Delta V_{GS}} \cdot \frac{dV_{OUT}}{dI_L}\ . \tag{5-52}$$

As dI_L/dV_{IN} exhibits an almost constant value in the considered input voltage range, the linearity of amplifier is mainly related to the dV_{OUT}/dI_L term, which is inversely proportional to the square root of I_L in accordance to *Eq.*(5-51). dV_{OUT}/dI_L affects the linearity of the gain for large signals. This voltage gain can be expressed directly by differentiating the DC characteristic of *Eq.*(5-49):

$$G_0(\Delta V_{GS}) = \frac{dV_{OUT}}{d\Delta V_{GS}} = \frac{1}{2}\sqrt{\frac{L_{eff}}{W_{eff}} \cdot \frac{W_D}{L_D}} \cdot \sqrt{\frac{I_B}{2 \cdot I_L(\Delta V_{GS})}} = \frac{1}{2}\frac{g_{m1,2}}{g_m'}\bigg|_{\Delta V_{GS}=0}\ , \tag{5-53}$$

where I_L reaches the value $I_{L,Q}=I_M - I_B/2$ at operation point $\Delta V_{GS}=0$. We observe that for an operating point fixed by V_{IN}, the AC voltage gain of *Fig. 5.16 type I* differential amplifier is fixed by the accurate W/L dimension ratios only, and depends no longer on KP_N/KP_P. This feature is a chief benefit of the design.

5.5.1 DC Operating Point

It has been so demonstrated that the voltage gain does not show signs of the dependency on the technological parameters. However, this is not the case for the DC output voltage (5-51) which exhibits a dependency on parameters V_{TH} and *KP*. This is the reason why the choice of the DC operating point is important for providing a wide temperature range operation.

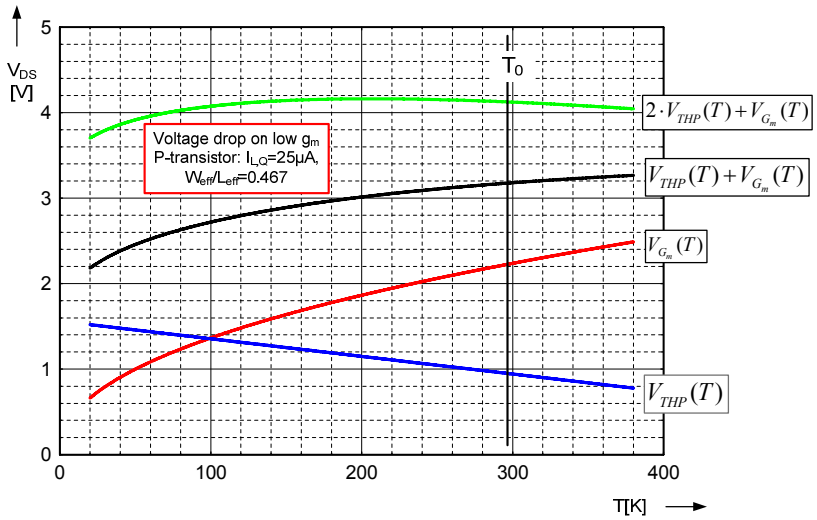


FIG. 5.17: *Temperature evolution of DC voltage on the low g_m composite load biased by $I_{L,Q}$= 25 µA (parameters Tab. 5.1). The curves correspond to the terms of (5-54). Improved compensation is provided by extra term $2\cdot|V_{THP}(T)|$*

tel-00417838, version 1 - 17 Sep 2009

By applying the temperature model of the transistor (*section 5.2*) to the expression of the amplifier output DC voltage (5-51), a temperature dependence $V_{OUT}(T)$ can be obtained as:

$$V_{OUT} = V_{DD} - \underbrace{|V_{THP}| \cdot \left[1 + \alpha_{THX} \cdot (T - T_0)\right]}_{V_{THP}(T)} - \underbrace{\sqrt{\frac{2 \cdot I_{D1}}{KP_P (T/T_0)^{-x} W_{eff}/L_{eff}}}}_{V_{Gm}(T)}, \qquad (5\text{-}54)$$

where the function (5-54) was divided in two parts: firstly the temperature evolution $V_{THP}(T)$ of the threshold voltage and secondly the contribution caused by temperature variation of carrier mobility $V_{Gm}(T)$. These contributions are plotted separately in *Fig 5.17*, where the opposite slopes of $V_{THP}(T)$ and $V_{Gm}(T)$ can be observed. It means, that the trends of both curves are partially compensated, as displayed by the sum of $V_{THP}(T) + V_{Gm}(T)$ (representation of (5-54)). Nevertheless, the total temperature drift remains high: $\Delta V_{OUT} = 1$ V for $\Delta T = 20$ K-380 K. However, this is not so critical, with regard to envisaged AC coupling of the inputs.

It is to be noted that the temperature compensation can be improved by increasing the contribution of the term $V_{THP}(T)$. For instance, by rewriting the (5-54) as $2 \cdot |V_{THP}(T)| + V_{Gm}(T)$. This function is plotted in *Fig. 5.17* (upper curve), where the temperature drifts exhibits a decrease of 0.22 V within whole 77 K-380 K temperature range. The term $2 \cdot |V_{THP}(T)|$ can be provided by a supplementary P-type MOS diode possessing high W/L, and connected serially to a low g_m composite load; such supplementary transistor have for a low current values high (dominant) variation of $V_{THP}(T)$, in spite of $V_{Gm}(T)$.

5.5.2 Design of our Type I Amplifier

The most important parameters to be determined in this section are the dimensions of the low g_m composite transistor W_{eff}/L_{eff}, the dimension of its input differential pair W_D/L_D and the I_B/I_L bias current ratio. Moreover, the absolute values of W and L can be optimized to provide a high frequency bandwidth and to reduce the $1/f$ noise, for instance (this is detailed in special *chapter 6*). In designing this of amplifier, the most important parameters are listed as:

- **DC operating point**
- **Gain accuracy**
- **Low inherent noise**
- **AC response**
- **Power consumption**
- **Chip surface**

Except the choice of the DC operating point, the important parameter to be considered is the high accuracy of the voltage gain. Our foremost objective is to *realize the amplifier with the accurate gain of 40dB in the first fabrication run*. This aspect guides us to base the design on transistors with $L > 2$ µm and to perform sensitivity analyses of all relevant components. The strategy, minimizing the noise and optimizing the AC response, will be detailed in *chapter 6*.

The first parameter – DC operating point leads us to choose the I_L/I_B with respect to the temperature swing of output voltage and the dynamic range of the amplifier. The W_D/L_D ratio can be deduced from the expression of the voltage gain (5-53):

$$\frac{W_D}{L_D} = 8 \cdot \frac{W_{eff}}{L_{eff}} \cdot \frac{I_{L,Q}}{I_B} \cdot G_0^2 . \qquad (5\text{-}55)$$

tel-00417838, version 1 - 17 Sep 2009

The calculation of parameters W_D/L_D is based on the analytical expression using a 1st order transistor model. However, more accurate results can be obtained with complex SPICE models. On that account, the "ideal" parameters computed with *Eq.*(5-55) were slightly modified by using the computer simulation. The resulting parameters are listed in the *Tab. 5.4*, including the parameters calculated upon (5-55) and $(W/L)_D$ corrected by simulation (as used for final integration).

TAB. 5.4: MAIN PARAMETERS CALCULATED FOR THE FIRST AMPLIFIER

PARAMETER:	CALCULATED	CORRECTED
$(W/L)_D$	2493µm/2µm	2360µm/2µm (-5.6%)
$(W/L)_{M1,M2,M4}$	15 µm/5 µm	-
$(W/L)_{M3,M5}$	38 µm/5 µm	-
I_B	750 µA	Simulated: 745µA
$I_{L,Q}$	25 µA	Simulated: 25.7µA
$V_{DC,OUT,296K}$	-0.7V	Simulated: -0.847V

Fig. 5.18 shows the final circuit of our *type I* 40 dB differential folded cascode amplifier. This figure contains, in addition to the structure introduced in *Fig. 5.16,* other components such as bias sources or output voltage buffer realised by emitter follower M_{O1}. The entire circuit is biased by a single current source $I_b = 500$ µA applied to the diode connected transistor M_{B1}. The bias voltage (V_{GSB1}) is distributed towards the gates of all current sources $M_{B2\text{-}B6}$. These transistors provide the biasing of the differential pair and low g_m composite load and its accuracy is critical. The cascode transistors are biased with $V_{bias} = 0$ V and do not require any additional circuits.

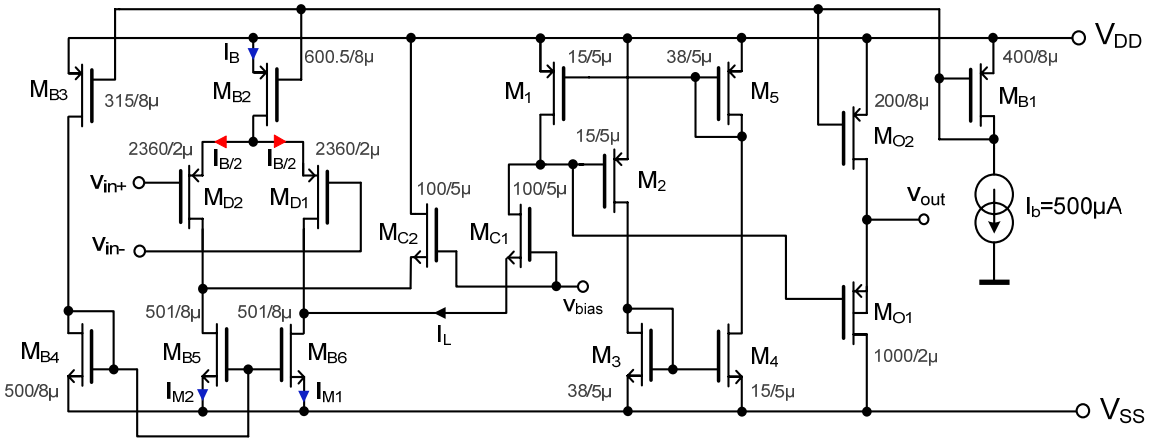


FIG. 5.18: *Folded cascode type-I fixed gain amplifier designed for 40 dB voltage gain (see sub-section 5.7.1 for discussion concerning the output voltage buffer)*

The *W*/*L* values of all transistors are shown in *Fig. 5.18*, whereas the detailed operating points are listed in the *Tab. 5.7* (at the end of this chapter). In the next section we will provide simulations of the main amplifier characteristics, allowing to check the design.

5.5.3 Simulated Characteristics of the Amplifier

In order to verify the design shown in *Fig. 5.18*, we provide simulations of the basic electrical characteristics: voltage gain G_0, DC voltage transfer $\Delta V_{GS}/V_{OUT}$ and AC transfer for various temperatures. We can refer to *Tab.5.7* (end of chapter), where the simulated operating points of

tel-00417838, version 1 - 17 Sep 2009

transistors from circuits shown in *Fig. 5.18* are detailed, and also to further *chapters 6* and *7*, where deeper investigation based on analytical, simulated and measured results will be presented.

The most important characteristic of the amplifier is the DC voltage transfer. This DC voltage transfer is shown in *Fig.5.19*, as provided through simulations with SPICE level-7 model and compared with the analytical model *Eq.*(5-49).

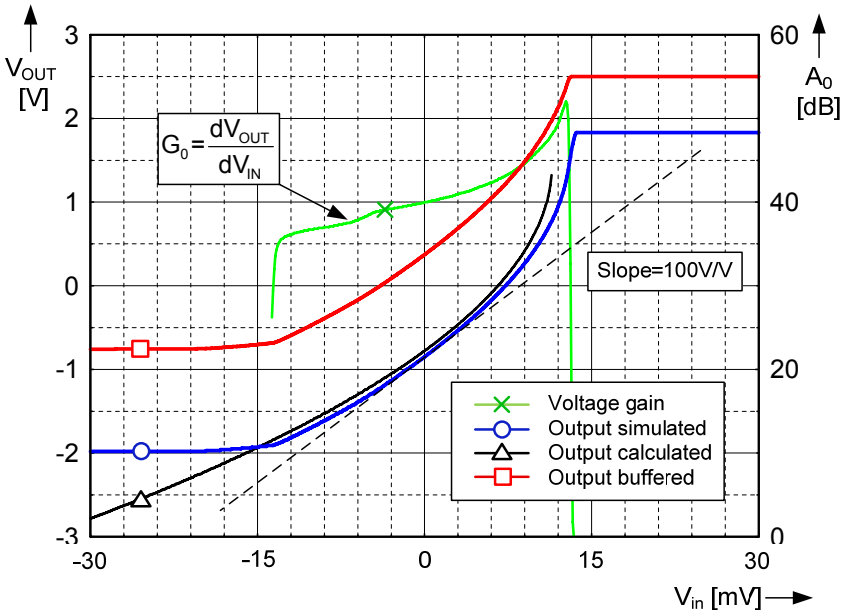


FIG 5.19: *Simulated and calculated (5-49) DC transfer characteristics of type I amplifier (room temperature, V_{DD} = 5 V)*

This figure shows a static voltage gain of G_0 = 39.9 dB and an acceptable choice of the DC operating point allowing the output peak-to-peak voltage swing up to 2 V. The DC transfer non-linearity can be characterised by a THD (total harmonic distortion): for instance 0.6 % for 0.1 $V_{P\text{-}P}$ output voltage (f = 1 kHz). The analytical form (5-49) of V_{OUT} is plotted in order to verify previously developed mathematical description, based on the 1st order model of transistor (*section 5.5*). Here the parameters of transistors obtained by measurements (*Tab. 5.1*) were used. The curve –□– represents a constant DC shift provided by the output voltage buffer M_{O1} (see *sub-section 5.7.1* bellow).

As we have shown in *section 5.2*, the temperature simulations are limited by the SPICE model accuracy below -55ºC. Nevertheless, the simulations can be used to estimate the tendency of the gain and evolution of frequency bandwidth. The AC response was plotted in the temperature range from -100 ºC to 100 ºC and exhibits only a low variation, well below 0.4 dB. This simulation confirms the decent temperature stability of the amplifier, as demonstrated in *Eq.*(5-53), where the gain is defined by the accurate transistor geometry ratios only.

We can investigate the "robustness" of the design in terms of relative sensitivities applied to *Eq.*(5-53) voltage gain. These sensitivities reaches |½| for all parameters present in the equation, so:

$$S_{x_i}^{G_0} = S_{W_D, L_{eff}, I_B}^{G_0} = -S_{L_D, W_{eff}, I_L}^{G_0} = \frac{\partial G_0}{\partial x_i} \cdot \frac{x_i}{G_0} = \frac{1}{2}, \qquad (5\text{-}56)$$

This low value is suitable with respect to the accuracy of the voltage gain. However, by reviewing the *Eqs.* (5-45) and (5-49), the I_B/I_L term can be also expressed as $I_B/I_L = 2/(k - 1)$, where the $k = I_{M1}/I_D$. The relative sensitivity can be now investigated in terms of the voltage gain G_0 and the value of k:

tel-00417838, version 1 - 17 Sep 2009

$$S_k^{G_0} = \frac{1}{2}\frac{k}{k-1}, \tag{5-57}$$

where its value can reach a high value. This is why a special attention must be paid about the accuracy of I_B/I_L. This accuracy is related to the matching of current mirrors and their low r_{DS} channel resistance, first of all.

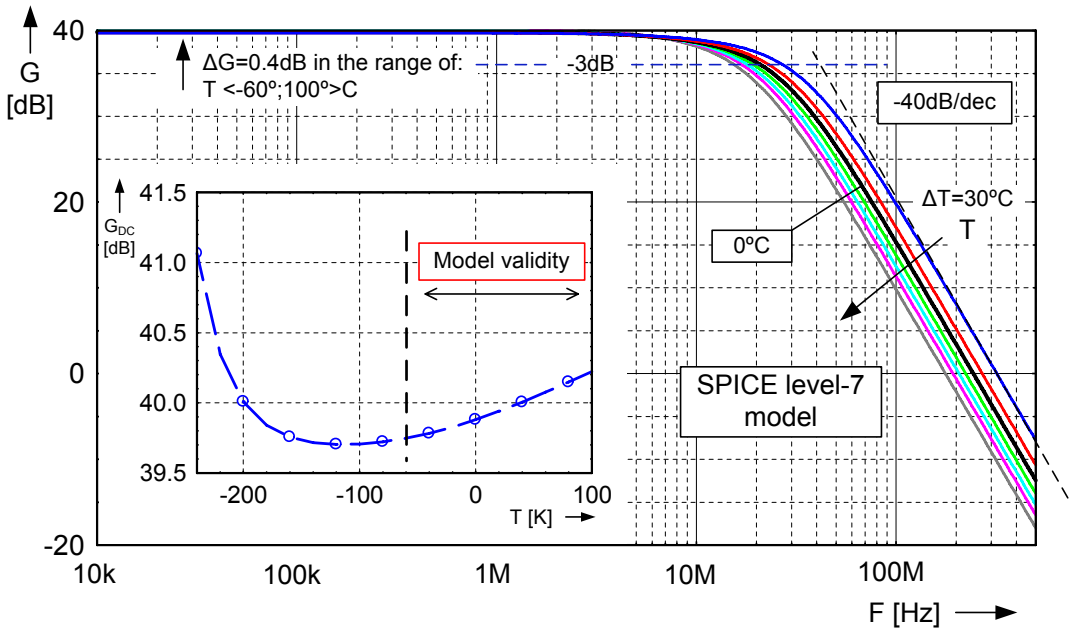


FIG. 5.20: *Simulated type I amplifier AC transfer characteristic for +80 to – 100 °C temperature range*

5.5.4 Summary of 1st Amplifier Basic Parameters

The results obtained from simulations of the first amplifier are in line with the initial prescribed requirements, namely in terms of the gain accuracy. Such accuracy is usually difficult to achieve by open loop amplifier. The relatively simple architecture of our amplifier allows to obtain a wide frequency bandwidth: 40 dB gain together with cut-off frequency 20 MHz results in a **GBW product of 2 GHz**, with relatively low consumption (~2 mA). However, the static characteristics can cause a high THD. In case of small signals, the non-linear part of characteristics is sufficiently small and the harmonic products in the frequency spectrum are negligible. Nevertheless, the linearization of the DC characteristic will be also treated in the next section.

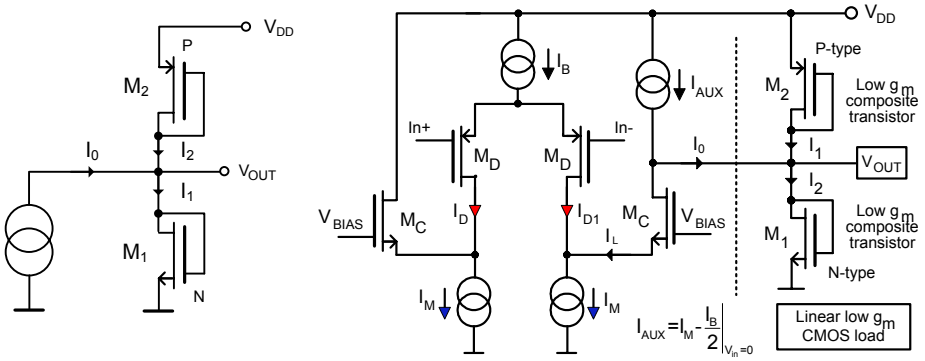
5.6 Linear Temperature Compensated Amplifier

In this section, the design of a second, wide linear and low input offset differential amplifier, based on a new, *low transconductance **linear** composite load,* will be presented. It will be demonstrated how the voltage gain can be accurately defined using a hybrid technique of current and voltage biasing and how its temperature characteristics can be *controlled* in order to reach optimal performances either for room or cryogenics environment. The designed amplifier will exhibit an accurate wide linear voltage gain, with low $G_0(T)$ dependency, this later being easily controlled by the V_{DD} supply voltage.

tel-00417838, version 1 - 17 Sep 2009

5.6.1 Low Transconductance Linear Composite Load

The analysis presented in *section 5.4.2* revealed that the differential folded cascode transconductor behaves (for low input voltages) as a quasi-linear voltage controlled current source. Accordingly, a linear DC characteristics of the amplifier can be realised by any load having a *linear current/voltage dependence* (*i.e.* constant resistance dV_{OUT}/dI_L in *Eq*. (5-52), see for an example [90]). By investigation of the quadratic form of the transistor current, we can deduce that the second order term can be cancelled by the subtracting the two drain currents of mutually biased transistors. *Fig. 5.21 a)* shows a circuit using two diode connected transistors for which the *I-V* characteristic is linearized. The circuit is based one N (M_1) and one P (M_2) channel type transistors.



a) *b*)

FIG. 5.21: *a) Linear load realised by two N and P channel MOS transistors, b) implementation of the linear load in folded cascode amplifier (the diode connected transistors are realized by low g_m composite MOS transistors (Fig.5.9)*

Both transistors in *Fig. 5.21 a)* are diode connected and are biased by a steady state current $I = I_1 = I_2$. This current results from the V_{DD} voltage and transistors parameters: V_{TH} and $\beta = KP(W/L)$. *Fig. 5.21 b*) also contains an auxiliary current source I_{AUX}, which value is chosen in such way that the current $I_0 = 0$ for zero input voltage $V_{IN} = 0$. By applying the KCL, I_0 can be obtained as:

$$I_0 = \left(I_{D1} - I_{M1}\right) + I_{AUX}\,. \tag{5-58}$$

The node equation can be written as the function of output voltage V_{OUT} and (5-58) bias current I_0:

$$\frac{\beta_1}{2}\left(V_{OUT} - V_{TH1}\right)^2 = \frac{\beta_2}{2}\left(V_{DD} - V_{OUT} - \left|V_{TH2}\right|\right)^2 + I_0\,, \tag{5-59}$$

where β_1, β_2 and V_{TH1},V_{TH2} refer to M_1 and M_2, respectively. The extraction of output voltage V_{OUT} can be done by decomposition of (5-59), which for identical $\beta_1 = \beta_2 \equiv \beta$, and $|V_{TH1}| = V_{TH2} \equiv V_{TH}$ leads to the expression:

$$V_{OUT} = \frac{V_{DD}}{2} + \frac{I_0}{\beta(V_{DD} + 2\cdot V_{TH})}\,, \tag{5-60}$$

This equation illustrates two basic properties of the load: the first term determines the steady-state operating point being $V_{DD}/2$ for zero input voltage ($I_0 = 0$). This results in a low (ideally zero) DC offset voltage of the amplifier. The second term in (5-60) shows an important property, namely that the *DC characteristic is a linear function of the bias current* I_0.

tel-00417838, version 1 - 17 Sep 2009

5.6.2 Differential Folded Cascode with Linear Load

Fig. 5.21 b) shows the linear load, based on the N and P MOS diode connected transistors. The external bias current I_0 is provided by the differential folded cascode transconductor. By definition, the amplifier gain remains a function of the transconductance ratio: ratio of the differential pair and linear load transconductance. Similarly to the previous design, the 40dB voltage gain requires a very low value of transconductance g_{mL}. This is why the low g_m composite transistors *Fig. 5.9* will be used in the linear load from *Fig. 5.21 a*). Similarly with our previous *Type I* amplifier, the use of low transconductance composite transistor allows to achieve a very low value of load transconductance with mid-size MOS transistors having $W/L > 1$.

However, the condition $\beta_1 = \beta_2$ and $V_{TH1} = V_{TH2}$, cannot be realised with transistors of different channel types, *i.e.* N and P. This is due to an important difference between V_{THP} and V_{THN}, and KP_P and KP_N. This difference can result in a DC operating point shift and nonlinear DC characteristics. Moreover, the temperature mismatch between M_1 and M_2 can enhance these effects.

The perfect matching ($\beta_1 = \beta_2$ and $V_{TH1} = V_{TH2}$) can be achieved with M_1 and M_2 composite transistors, both having the same channel type: *the grounded transistor M_1 can be realised as a P-channel type and referred to the ground by a special level shifter,* in order to behave as an equivalent N-channel type transistor.

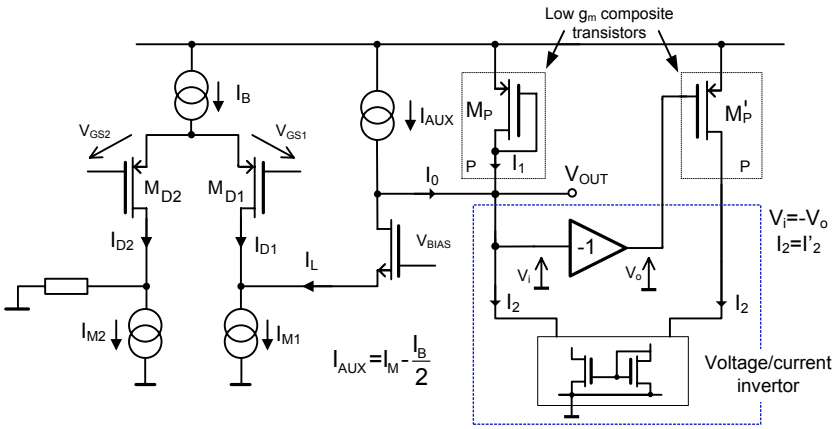


FIG. 5.22*: Symmetrisation of the low g_m linear provided by a impedance inverter*

Fig. 5.22 shows how this level shifter (or voltage/current inverter) can be realised by means of an accurate inverter and ground-referenced current mirror. The fact that the N-channel type transistor (M_1 of *Fig. 5.21 a*) is simulated by means of a P type transistor, allows to build the linear low g_m composite load with *identical* M_P and M'_P transistors. In this way, the condition $\beta_1 = \beta_2$ and $V_{TH1} = V_{TH2}$ can be accurately fulfilled.

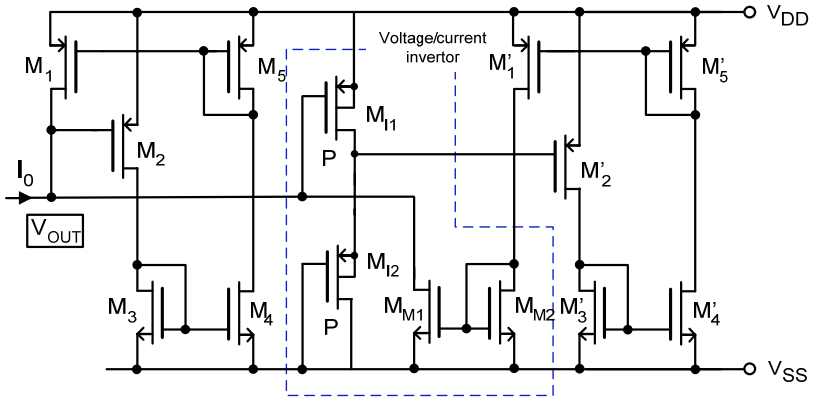


FIG. 5.23: *Linear low-g_m CMOS load (to be connected the input stage)*

tel-00417838, version 1 - 17 Sep 2009

Fig. 5.23 demonstrates an implementation of *Fig. 5.22* voltage/current inverter containing the current mirror (M_{M1}, M_{M2}) and inverter (M_{I1}, M_{I2}). Here, two identical low g_m composite transistors based on M_1-M_5 and M'_1-M'_5 are interconnected in conformity with the concept of *Fig 5.22*.

In order to provide a good matching of M_P and M'_P both voltage and current inversion have to be done with a high precision. The accuracy of the current mirror is determined by the drain resistance r_{DS} (channel length modulation effect λ), the saturation of carrier mobility and the transistor (geometric) mismatch. In our case, the mismatch of input and output currents is accentuated by the fact that the transistors M_{M1} and M_{M2} operate with a high difference of V_{DS}. The transfer of the current mirror can be expressed as a function of λ [22] (indices $_1$ and $_2$ correspond to the transistor M_{M1} and M_{M2}, respectively):

$$\frac{I_{M1}}{I_{M2}} = \left(\frac{W_1 L_2}{W_2 L_1}\right) \cdot \left[\frac{1+\lambda V_{DS1}}{1+\lambda V_{DS2}}\right]. \tag{5-61}$$

In a real MOS transistor, the channel length modulation is lower for a long channel device than for a short channel one (*Eq.* (2-15)). It follows, that the accurate transfer 1:1 can be provided by using a long device (*i.e.* channel length above some 2 μm). An accurate current transfer can be also provided by a cascode current mirror. However, simulations have shown the accuracy of large channel current mirrors as satisfactory for our application.

More difficult is to obtain an accuracy inversion -1 in a wide dynamic range of V_{DD} to V_{SS}. The inverter can use a common source configuration similar to *Fig. 5.4*, were $g_{m1} = g_{m2}$. However, this equivalence requires matched (*i.e.* identical channel type) transistors M_{I1}, M_{I2}. In doing so, the bulk transconductance caused by nonzero V_{BS} voltage has to be cancelled. As shown in *Fig.5.23*, the inverter is realized by two identical P-channel type transistors. In CMOS technology, the transistor can be isolated by using a "*hot well*", allowing to fix the local substrate potential at any arbitrary value (*Fig. 2.2*, *chapter 2*). In the case of AMS process, the hot well can be applied to the P-channel type transistor only. The zero V_{BS} voltage can then be obtained by a hot N-well having the potential equal to the V_S source voltage of transistor M_{I1}. This is depicted at *Fig. 5.23*, where this zero $V_{BS(MI2)}$ voltage allows further removing of the bulk transconductance and ensures a very good matching of M_P and M'_P transconductances (*Fig. 5.22*).

5.6.3 Basic Characteristics of the Linear Amplifier

The previous analysis reveals that the DC characteristic $V_{out}=f(\Delta V_{in})$ is linear in a wide dynamic range. This is due to the constant dV_{OUT}/dI_L resulting form *Eq.*(5-60). In *Fig. 5.21* and *Fig. 5.22,* an auxiliary current source I_{AUX} has been added. Its value is determined by I_B and I_M in such way that $I_0 = 0$ for zero input voltage:

$$I_{AUX} = I_{M1} - \frac{I_B}{2}. \tag{5-62}$$

The zero I_0 current provides the DC operating point at ½V_{DD} (*Eq.*(5-60)). Moreover, (5-58) removes the term $I_{M1} - I_B/2$ present in previous *type I* design (5-45) which increases the relative sensitivity of the voltage gain. The output voltage can be written as a function of the folded cascode output current I_0 (5-44) and the voltage response of the composite linear load (5-60):

tel-00417838, version 1 - 17 Sep 2009

$$V_{OUT} = \frac{1}{2}V_{DD} + \frac{\frac{1}{2}I_B - \frac{1}{8}\left(\sqrt{4\cdot I_B - KP_P\cdot\frac{W_D}{L_D}\cdot\Delta V_{GS}^2} + \sqrt{KP_P\cdot\frac{W_D}{L_D}}\cdot\Delta V_{GS}\right)^2}{KP_P\cdot\frac{W_{eff}}{L_{eff}}\left(V_{DD} - 2\cdot|V_{THP}|\right)}. \qquad (5\text{-}63)$$

This characteristic is a nearly-linear function of ΔV_{GS} with voltage gain constant in wide dynamic range (see simulation in *Fig. 5.25*). The voltage gain G_0 can be determined by differentiation of (5-63) at $\Delta V_{GS} = 0$:

$$G_0 = \left.\frac{dV_{OUT}}{d\Delta V_{GS}}\right|_{\Delta V_{GS}=0} = \frac{1}{2}\cdot\frac{\sqrt{I_B\cdot\frac{W_D}{L_D}}}{\sqrt{KP_P}\cdot\frac{W_{eff}}{L_{eff}}\cdot\left(V_{DD} - 2\cdot|V_{THP}|\right)}, \qquad (5\text{-}64)$$

This expression shows the voltage gain as the function of:

- $\sqrt{(W/L)_D}/(W/L)_{eff}$ **ratio,**
- **Technological parameters:** KP_P, V_{THP}.
- **Bias current** I_B **and power supply voltage** V_{DD}.

These dependences can be explained as follows: as the input differential pair is biased by the constant current I_B, its transconductance is proportional to the square root of $I_B\cdot(W_D/L_D)$ (see *Eq.* (5-47)). On the contrary, the quiescent current of the linear low g_m composite load is a function of V_{DD} voltage and the transconductance has a *linear W/L* dependence similarly to the voltage biased transistor *Eq.*(2-25) (the linear composite load is *self-biased*). The presence of such different terms results in a particular ratio g_{m1}/g_{m2}. The properties and advantages of this current/voltage biasing technique will be discussed in *sub-section 5.6.4*

On the other hand, one can object that the dependence on process parameters (*KP* and V_{TH}) may deteriorate the accuracy of the amplifier gain. However, by analysing the sensitivities related to all parameters of *Eq.*(5-64), a relatively low impact to the voltage gain can be observed. These sensitivities are calculated in the following table 5.5, upon the definition (5-56).

In fact, the sensitivity on *KP* is favoured by the presence of the $\sqrt{}$ term resulting on a low value ½. Similarly, a low sensitivity on V_{TH} being around $^2/_3$ is acceptable for the design. In addition, the comparison of parameters *Tab. 5.1* and *Tab 5.2* (parameters measured in two different fabrication runs) shows a good accuracy of AMS 0.35 µm process, which led us to expect accurate results.

TAB. 5.5: RELATIVE SENSITIVITIES OF THE VOLTAGE GAIN FUNCTION *EQ.*(5-64)

	KP	$\mathbf{V_{TH}}$	$\mathbf{V_{DD}}$	$\mathbf{I_B}$	$\mathbf{W_D/L_D}$	$\mathbf{W_{Eff}/L_{Eff}}$
$S_{x_i}^{G_v}$	$-\frac{1}{2}$	$\frac{2\cdot V_{THP}}{V_{DD} - 2\cdot V_{THP}}$	$-\frac{V_{DD}}{V_{DD} - 2\cdot V_{THP}}$	$\frac{1}{2}$	$\frac{1}{2}$	-1

The low dependence of the gain on V_{DD} voltage is not a problem, as most of semiconductor circuits are biased with a stabilized voltage source. On the contrary, we will show bellow, how the V_{DD} voltage can be used to control the temperature characteristics $G_0(T)$ in such a hybrid *current versus voltage biased* amplifier.

tel-00417838, version 1 - 17 Sep 2009

5.6.4 Analysis of the Temperature Behaviour

By focusing to the voltage gain (5-64), we can identify the constant parameters as transistor dimensions W/L or bias current I_B. These parameters can be extracted and (5-64) can be rewritten as:

$$G_0(T) = \frac{C}{\sqrt{KP_P(T)} \cdot \left(V_{DD} - 2 \cdot \left|V_{THP}(T)\right|\right)}, \tag{5-65}$$

where constant C corresponds to the extracted parameters. In consequence we can apply the temperature model of transistor MOS described in *section 5.1*. The thermal dependence of the gain factor KP is conditioned by carrier mobility $\mu(T)$ *Eq.*(5-1) and threshold voltage temperature is related to *Eq.*(5-2). We obtain the relative temperature function of the voltage gain $G_0(T)/C$ in the following form:

$$\frac{G_0(T)}{C} = \frac{1}{\sqrt{KP_P(T_0) \cdot \left(\frac{T}{T_0}\right)^{-x}} \cdot \left[V_{DD} - 2 \cdot \left|V_{THP}(T_0)\right| \left[1 + \alpha_{THX} \cdot (T - T_0)\right]\right]}. \tag{5-66}$$

This expression is particularly interesting because it shows the temperature function of the gain to be dependent on one variable parameter: the V_{DD} *voltage*. It will be demonstrated that the tendencies of both temperature functions $KP(T)$ and $V_{TH}(T)$ are in the opposite sense, and therefore results in the *temperature compensation of the voltage gain*. Moreover, the variable V_{DD} voltage *control the contribution of V_{TH} voltage on the compensation of $G_0(T)$*. This allows regulating the shape of the thermal characteristic $G_0(T)$ and to reach better performances either for room temperatures or for wide temperature (cryogenic) range. This property will be demonstrated through simulation in the following section (see *Fig. 5.27*).

In sub-section dealing with DC operation point (*5.5.1*) the absolute value of terms $KP(T)$ and $V_{TH}(T)$ were considered (contribution was adjusted by an integral factor as $2 \cdot |V_{THP}(T)|$, see *Fig. 5.17*). On the contrary, the compensation $G_0(T)$ described by *Eq.*(5-66) allows controlling the slope of the mobility variation (constant x) by the previously mentioned technique of hybrid *current versus voltage biasing*: the temperature characteristic $KP_P(T)$, given by (5-1), becomes in this case $\sqrt{KP_P}(T)$. This can provide almost perfect temperature compensation within a wide temperature range (see *Fig. 5.26* and *Fig. 5.27*).

5.6.5 Design of the Type II Amplifier

The design of the *type II*, linear temperature compensated amplifier, is based on the specifications as these mentioned in *sub-section 5.5.2*. For this 2nd amplifier, the wide output voltage linearity does not make appear the difference of currents as in *Eq.*(5-45), causing a high sensitivity of the voltage gain similar to *Eq.*(5-57). The good matching of I_{M1} and I_{AUX} is important only in order to reach a low input offset voltage.

The circuit of this linear 40dB differential amplifier is reported in *Fig.5.24* where the values of W/L are shown. We can see the differential transconductor containing the transistors M_D, cascode transistors M_C and the low transconductance linear load based on the low transconductance composite transistors (as shown in *Fig. 5.23*). The circuit is biased by current mirrors M_{M1}-M_{M5} controlled by the input bias transistor M_{B1}.

tel-00417838, version 1 - 17 Sep 2009

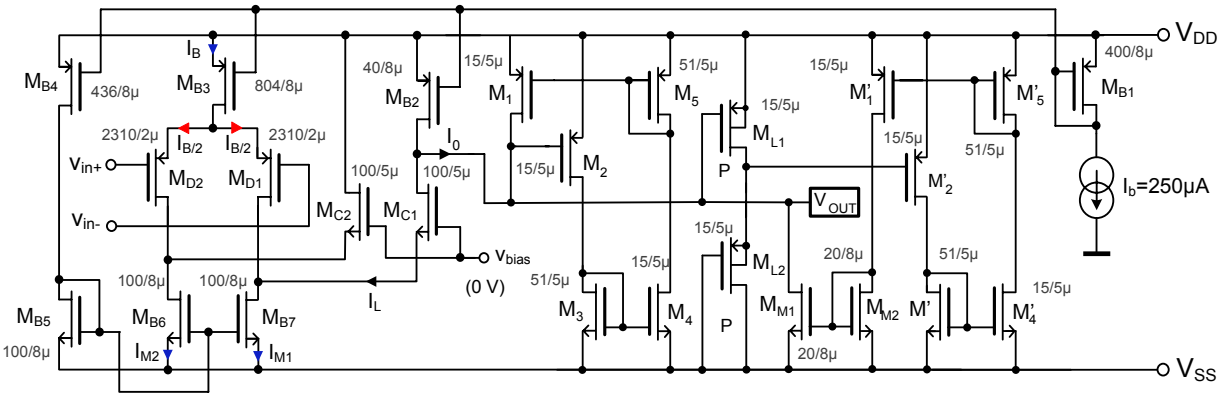


FIG. 5.24: *Final realization of type II linear temperature compensated CMOS amplifier*

To determine the basic parameters (*W*/*L* ratios, bias currents etc.) we use the expression of the voltage gain (5-64) and to measured parameters of the PMOS transistor *Tab. 5.1*. The basic parameters are summarized in following table 5.6.

TAB 5.6: CALCULATED PARAMETERS AND PARAMETERS CORTRECTED BY SIMULATION OF THE SECOND DIFFERENTIAL AMPLIFIER

PARAMETER:	CALCULATED	CORRECTED
$(W/L)_D$	2493 µm / 2 µm	2310 µm/2 µm (-5%)
$(W/L)_{M1,M2,M4}$	15 µm / 5 µm	-
$(W/L)_{M3,M5}$	62 µm / 5 µm	-
I_B	500 µA	500.4 µA
I_{AUX}	25 µA	24.89 µA
Input offset	0V	60.24 µV

The checking of the design was carried out by the simulations. *Fig. 5.25* shows the DC characteristics of amplifier obtained with SPICE level-7 model, analytical form of DC voltage transfer (5-63) and SPICE level-1 model with *Tab. 5.1* parameters (plotted for V_{DD} = 5 V).

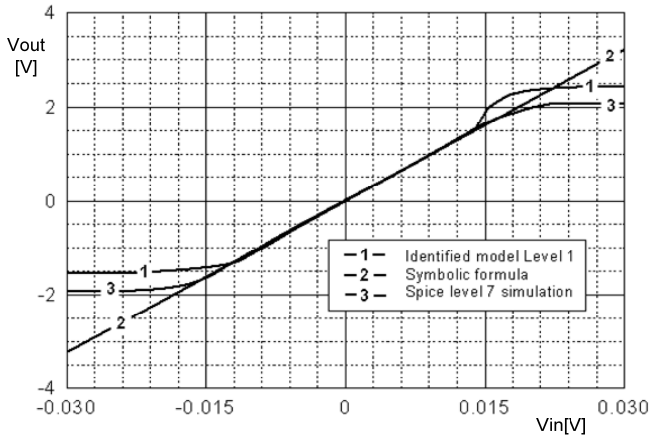


Fig. 5.25: *DC transfer characteristics plotted by simulation with level-7 SPICE model, SPICE level 1 model and by formula (5-63) with measured parameters (Tab. 5.1)*

This resulting DC characteristics (*Fig.5.25*) show a very good linearity within the ±2 V voltage range as well as the high accuracy of fixed gain: 39.9dB (simulation – adjusted *Tab. 5.6* parameters). We can also see fine agreement between the analytic (5-63) model and SPICE Level 7 model, provided by the

tel-00417838, version 1 - 17 Sep 2009

AMS foundry. The detailed values of the operating points are summarized in *Tab. 5.8* (Appendix at the end of this chapter).

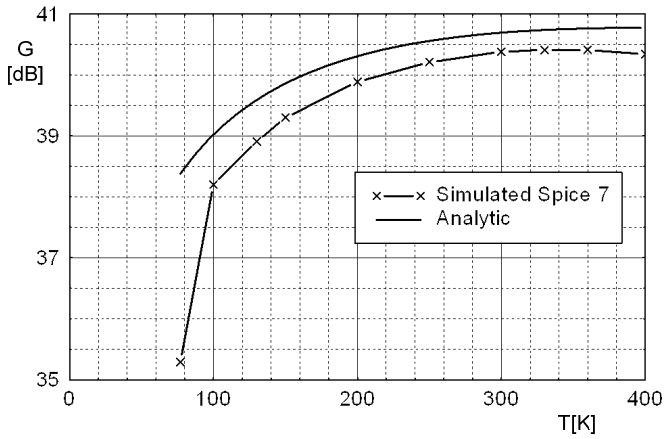


FIG. 5.26: *Comparing of calculated and simulated thermal function of AC gain (calculated parameters Tab. 5.1, V_{DD} = 5 V)*

The 40 dB voltage gain was calculated for 5 V supply voltage V_{DD}. As we have shown in the *sub-section 5.6.4*, the temperature function of the gain $G_0(T)$ can be *controlled via* the V_{DD} voltage (5-66). By exploring the temperature characteristic $G_0(T,V_{DD})$, we can find out that the temperature function has a maximum flatness in the vicinity of room temperature around V_{DD} = 5 V. This is shown in *Fig. 5.26*, where the $G_0(T)$ characteristics resulting from the analytical thermal model (5-66) and simulation with SPICE Level-7 model are plotted.

A good agreement between the analytical model and simulation (except for a small gain error) is evident in the range of 100 K – 400 K. Below T = 100 K, the SPICE model is no longer valid and we have to consider the results based on the empirical model from *section 5.1*.

However, for V_{DD} = 5 V we can observe an important deviation of the gain: -2 dB at T = 77 K. This deviation can be compensated by decreasing the V_{DD} voltage below 4.4 V. This is shown on the $G_0(T)$ characteristics *Fig. 5.27* where two V_{DD} voltages were applied to the analytic model (5-66): V_{DD}= 5 V and V_{DD}= 4.4 V. For 4.4 V the variation does not exceed 0.9 dB within the whole temperature range 77 K - 400 K. The measurements performed in that range with the fabricated amplifier show indeed a lower variation for V_{DD}= 4.4 V as shown in the chapter 7 (see *Fig. 7.26* and related comments).

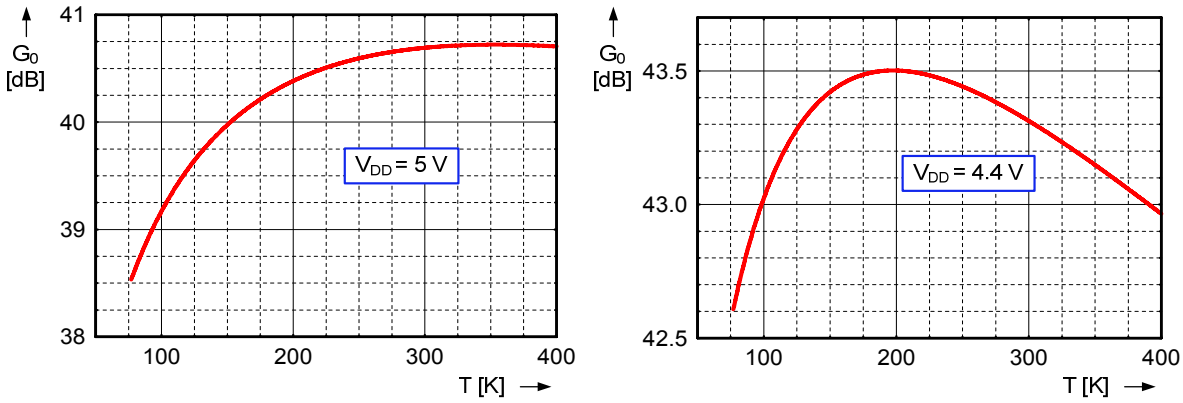


FIG. 5.27: *Thermal function of the gain $G_0(T)$ for two supply voltage values*

tel-00417838, version 1 - 17 Sep 2009

However, from the change in V_{DD} results a shift of amplifier gain (see *Fig. 5.27 a* and *b*). This is implicit from expression *Eq.*(5-64). Obviously, such a shift of the gain is systematic and therefore constant for all amplifiers operating with a given V_{DD}.

5.6.6 Performances of the 2nd (Linear) Amplifier: Summary

The design of *type II* linear, temperature compensated amplifier provide a wide-linear operations and exhibits intrinsically low DC offset voltage. The delivered equations show the dependence of the gain on the bias current/voltage as well as on the process parameters. However, from the measurements performed on the MOS transistors and from the low relative sensitivities of the voltage gain function; we can thus expect a good accuracy of the parameters obtained with the fabricated circuit. The simulated AC characteristic shows a 4 MHz frequency bandwidth (**GBW = 400 MHz**). This large bandwidth together with high input impedance and low power consumption (~1 mA) make this amplifier quite interesting as a compact and universal block for VLSI design. The simulated performances comply with the technical specifications of the amplifier mentioned in *sub-section 4.6.3* and are important for a high performance cryogenic and room temperature test bench, dedicated to the test of THz imagers.

5.7 Output Voltage Buffer

Both amplifiers presented in previous sections achieve the 40 dB voltage gain at nodes exhibiting the high impedance. These impedances result from the low g_m composite load and are in order of 20 µS (50 kΩ). Obviously, these nodes have to be isolated, in order to preserve the voltage gain and frequency bandwidth of the amplifier. Depending on the amplifier DC performances, we use two different voltage buffers:

i) An emitter follower, realised by a common drain transistor used for *type I* amplifier;

ii) A sophisticated linear low DC offset voltage buffer applied to the *type II* amplifier.

5.7.1 Common Drain Voltage Follower

The purpose of the common drain voltage follower (VF) is to preserve the gain and bandwidth of the amplifier. In addition, the constant DC shift (approximately V_{TH}) of common drain VF can decrease the offset of the amplifier (see *Fig. 5.19*). This DC shift is also important to reduce the high gain of the amplifier that appears close to the positive saturation point (see again *Fig. 5.19*).

The voltage follower is shown in *Fig. 5.18* where transistor M_{O1} (P- channel type 1000 µm / 1 µm) is biased by a constant current source 250µA (M_{O2}). The key parameter of the voltage buffer is its output resistance determined by M_{O1}:

$$r_{out} = \frac{1}{g_{mO1}} = \frac{1}{\sqrt{2KP_P(W_{O1}/L_{O1})\cdot I_{O1}}}. \qquad (5\text{-}67)$$

It reaches some 600 Ω (see *Tab 5.7*). It will be demonstrated (*chapter 7*) that this impedance introduces an additional pole in the AC transfer characteristic and the low bias current (250 µA) limits the slew rate (S/R) to a relatively low value (for instance S/R = 25 V/µs for 10 pF load).

Such relatively high impedance is imposed by the required low power dissipation of amplifier. However, the parameters r_{out} and *S/R* can be improved by any auxiliary (external) current source increasing the drain current of M_{O2} (*Eq.*(5-67)).

tel-00417838, version 1 - 17 Sep 2009

5.7.2 Linear Low Offset Voltage Buffer

The purpose of the voltage buffer is to preserve the excellent DC properties of the *type II* amplifier, such as the linear V_{in}/V_{out} characteristic or low DC offset. The design of the output buffer is based on a modified version upon [91] and the final circuit is shown in *Fig. 5.28*.

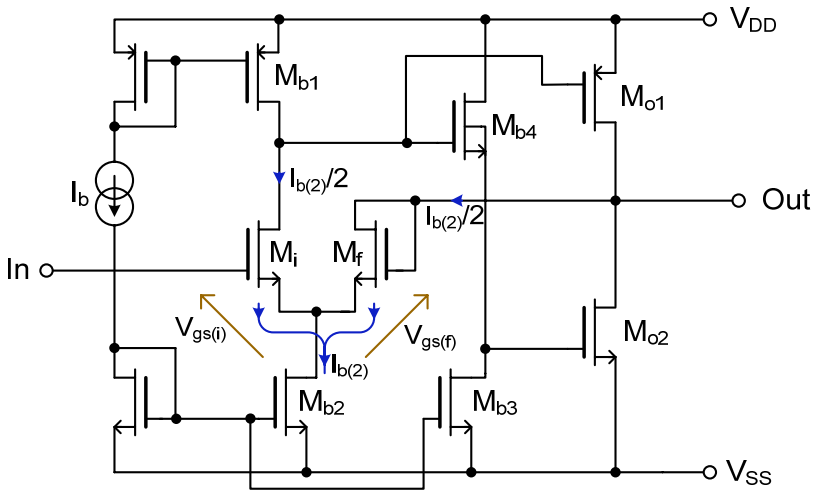


FIG. 5.28: *Design of the linear, low offset output buffer for type II amplifier*

In this chapter, we provide only basic information and explanation, whereas the detailed analysis will be provided in *chapter 10* (in *chapter 10*, a similar configuration is used in the design of a low output impedance second generation current conveyor CCII-).

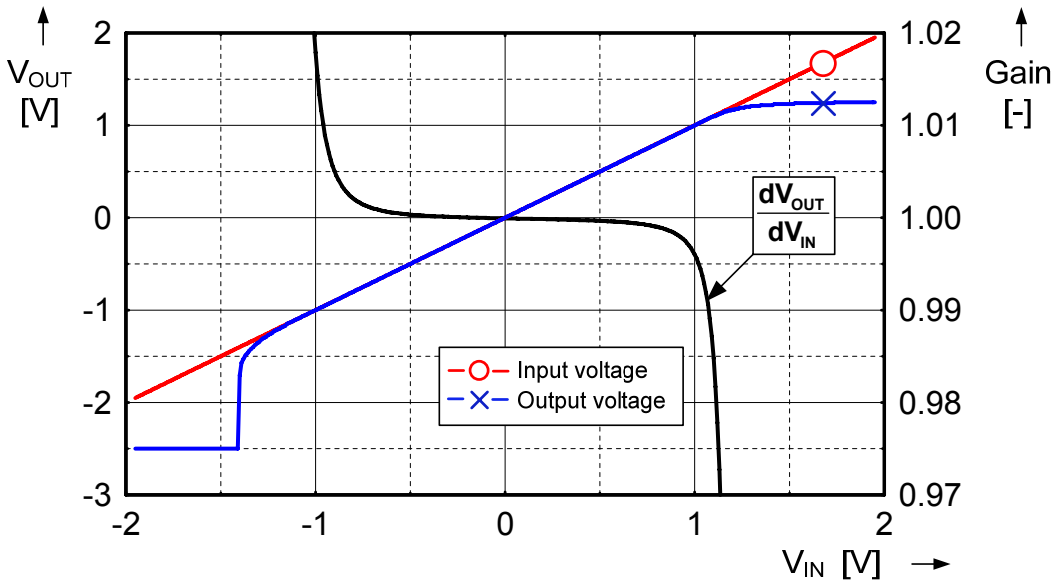


Fig. 5.29: *Transfer characteristics of output buffer for type II amplifier, with plotted voltage gain, linear in wide dynamic range (simulation SPICE-level 7 model, V_{DD} = 5 V)*

Fig. 5.28 shows the input transistor M_i biased by two current sources M_{b1} and M_{b2}. The drain of M_i is a high impedance node. This node is connected to the gates of transistors M_{O1} and M_{O2} which are the common source amplifiers. The value of the bias current of $M_{o1,2}$ is controlled by M_{b4}. The low offset voltage of the follower is achieved *via* a feedback loop provided by diode-connected transistor M_f. Both input and feedback transistors are biased *by the identical currents* $I_B/2$. This cause (for identical

tel-00417838, version 1 - 17 Sep 2009

M_i and M_f) also identical $V_{GSi} = V_{GSf}$ and zero voltage difference between V_{IN} and V_{OUT}. The output transistors M_{O1} and M_{O2} are self-biased. This means that the quiescent current can depend on the temperature and may affect the power consumption, particularly at cryogenic temperatures. Its value has to be determined by simulations with accurate models and carefully verified by a worst-case analysis.

In order to provide comparative and correct measurements, one of the amplifiers was integrated *without* the voltage buffer. This allows avoiding an additional distortion or DC offset provided by the voltage buffer. The second reason is the value of the quiescent current of M_{O1}, M_{O2} at lower temperatures. Above all, we are interested in testing the amplifier linearity, in demonstration of temperature compensation of the gain and it's controlling *via* the value of V_{DD} voltage.

Fig. 5.29 shows a simulated DC characteristic exhibiting an excellent DC accuracy (*i.e.* linearity and offset). The simulated properties of voltage buffer comply with all static parameters of amplifier as well as with the simulated bandwidth.

Appendix: Simulated operating points

TAB 5.7 SIMULATED OPERATING POINT OF CHAPTER 6.3 AMPLIFIER

TRANSISTOR	M_{D1}	M_{D2}	M_{C1}	M_{C2}	M_1	M_2	M_3	M_4	M_5
TYPE	P:2360/2µm	P:2360/2µm	N:100/5µ	N:100/5µ	P:15/5µ	P:15/5µ	N:38/5µ	N:15/5µ	P:38/5µ
I_D	-373u	-373u	25,8u	25,8u	-25,8u	-166u	166u	65,4u	-65,4u
V_{GS}	-1,47	-1,47	1,4	1,4	-1,89	-3,35	1,54	1,54	-1,89
V_{DS}	-2,88	-2,87	554m	3,9	-3,35	-3,46	1,54	3,11	-1,89
V_{BS}	1,03	1,03	-1,1	-1,1	0	0	0	0	0
V_{TH}	-1,33	-1,33	1,24	1,24	-1,03	-1,03	768m	766m	-1,02
V_{DSAT}	-152m	-152m	135m	134m	-673m	-1,82	469m	470m	-677m
g_m	4,17m	4,17m	268u	269u	56,8u	132u	405u	159u	143u
g_{DS}	6,07u	6,07u	165n	55,5n	186n	1,42u	325n	89,6n	681n
g_{MB}	1,04m	1,04m	101u	102u	18u	40,9u	184u	72,1u	45,3u
C_{GSOV}	215f	215f	10,8f	10,8f	1,37f	1,37f	4,1f	1,62f	3,46f
C_{GDOV}	215f	215f	10,8f	10,8f	1,37f	1,37f	4,1f	1,62f	3,46f
C_{GBOV}	220a	220a	550a	550a	550a	550a	550a	550a	550a

TRANSISTOR	M_{O1}	M_{O2}	M_{B1}	M_{B2}	M_{B3}	M_{B4}	M_{B5}	M_{B6}
TYPE	P:1000/2µ	P:200/8µ	P:400/8µ	P:600.5/8µ	P:315/8µ	N:500/8µ	N:501/8µ	N:501/8µ
I_D	-250u	-250u	-500u	-745u	-398u	398u	398u	398u
V_{GS}	-1,33	-1,95	-1,95	-1,95	-1,95	1,17	1,17	1,17
V_{DS}	-2,98	-2,02	-1,95	-1,03	-3,83	1,17	1,1	1,1
V_{BS}	0	0	0	0	0	0	0	0
V_{TH}	-1,02	-1,02	-1,02	-1,02	-1,02	763m	763m	763m
V_{DSAT}	-262m	-725m	-725m	-725m	-725m	256m	256m	256m
g_m	1,48m	512u	1,02m	1,52m	815u	1,85m	1,85m	1,85m
g_{DS}	1,82u	1,63u	3,33u	10u	1,68u	1,12u	1,17u	1,17u
g_{MB}	497u	160u	321u	476u	255u	884u	885u	885u
C_{GSOV}	91f	18,2f	36,4f	54,6f	28,7f	54f	54,1f	54,1f
C_{GDOV}	91f	18,2f	36,4f	54,6f	28,7f	54f	54,1f	54,1f
C_{GBOV}	550a	880a	880a	880a	880a	880a	880a	880a

tel-00417838, version 1 - 17 Sep 2009

TAB. 5.8: SIMULATED OPERATING POINT OF CHAPTER 6.4 AMPLIFIER

TRANSISTOR	M_{D1}	M_{D2}	M_{C1}	M_{C2}	M_{L1}	M_{L2}	M_{M1}	M_{M2}	M_1
TYPE	P:2310/2µ	P:2310/2µ	N:100/5µ	N:100/5µ	P:15/5µ	P:15/5µ	N:20/8µ	N:20/8µ	P:15/5µ
I_D	-250u	-250u	24,8u	24,8u	-70,8u	-70,8u	6,19u	6,22u	-6,1u
V_{GS}	-1,45	-1,45	1,4	1,4	-2,51	-2,51	1,01	1,01	-1,43
V_{DS}	-2,85	-2,85	3,9	1,39	-2,49	-2,51	1,01	2,49	-2,51
V_{BS}	1,05	1,05	-1,1	-1,1	0	0	0	0	0
V_{TH}	-1,34	-1,34	1,24	1,24	-1,03	-1,03	760m	760m	-1,03
V_{DSAT}	-130m	-130m	132m	132m	-1,14	-1,14	166m	166m	-332m
g_m	3,22m	3,22m	262u	262u	90,7u	90,7u	46,4u	46,5u	28,1u
g_{DS}	4,1u	4,1u	54,1n	61,8n	686n	683n	24,8n	21,4n	50,5n
g_{MB}	800u	800u	99,2u	99u	27,8u	27,8u	22,6u	22,7u	9,35u
C_{GSOV}	210f	210f	10,8f	10,8f	1,37f	1,37f	2,16f	2,16f	1,37f
C_{GDOV}	210f	210f	10,8f	10,8f	1,37f	1,37f	2,16f	2,16f	1,37f
C_{GBOV}	220a	220a	550a	550a	550a	550a	880a	880a	550a
TRANSISTOR	M'_1	M_2	M'_2	M_3	M'_3	M_4	M'_4	M_5	M'_5
TYPE	P:15/5µ	P:15/5µ	P:15/5µ	N:51/5µ	N:50.5/1µ	N:15/5µ	N:15/5µ	P:51/5µ	P:51/5µ
I_D	-6,19u	-71,6u	-70,4u	71,6u	70,4u	21,1u	21u	-21,1u	-21u
V_{GS}	-1,44	-2,51	-2,49	1,19	1,19	1,19	1,19	-1,43	-1,44
V_{DS}	-3,99	-3,81	-3,81	1,19	1,19	3,57	3,56	-1,43	-1,44
V_{BS}	0	0	0	0	0	0	0	0	0
V_{TH}	-1,03	-1,03	-1,03	768m	768m	766m	766m	-1,02	-1,02
V_{DSAT}	-333m	-1,14	-1,13	268m	267m	269m	269m	-335m	-336m
g_m	28,5u	91,8u	91,1u	317u	313u	92,9u	92,6u	96,2u	95,4u
g_{DS}	36,7n	507n	498n	212n	210n	47n	46,9n	234n	232n
g_{MB}	9,48u	28,2u	28u	151u	150u	44,4u	44,2u	31,9u	31,6u
C_{GSOV}	1,37f	1,37f	1,37f	5,51f	5,45f	1,62f	1,62f	4,64f	4,6f
C_{GDOV}	1,37f	1,37f	1,37f	5,51f	5,45f	1,62f	1,62f	4,64f	4,6f
C_{GBOV}	550a	550a	550a	550a	550a	550a	550a	550a	550a

TRANSISTOR	M_{B1}	M_{B2}	M_{B3}	M_{B4}	M_{B5}	M_{B6}	M_{B7}
TYPE	P:400/8µ	P:40/8µ	P:804/8µ	P:436/8µ	N:100/8µ	N:100/8µ	N:100/8µ
I_D	-250u	-24,9u	-5,00E-04	-275u	275u	275u	275u
V_{GS}	-1,67	-1,67	-1,67E+00	-1,67	1,55	1,55	1,55
V_{DS}	-1,67	-2,51	-1,05E+00	-3,45	1,55	1,1	1,1
V_{BS}	0	0	0	0	0	0	0
V_{TH}	-1,02	-1,02	-1,02E+00	-1,02	762m	762m	762m
V_{DSAT}	-512m	-510m	-5,12E-01	-512m	473m	473m	473m
g_m	731u	73u	1,46E-03	805u	671u	670u	670u
g_{DS}	1,73u	137n	4,59E-06	1,21u	478n	791n	791n
g_{MB}	235u	23,5u	4,70E-04	259u	304u	303u	303u
C_{GSOV}	36,4f	3,64f	7,32E-14	39,7f	10,8f	10,8f	10,8f
C_{GDOV}	36,4f	3,64f	7,32E-14	39,7f	10,8f	10,8f	10,8f
C_{GBOV}	880a	880a	8,80E-16	880a	880a	880a	880a

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

6 AC AND NOISE ANALYSIS

6.1 AC Analysis of the Amplifier

This chapter is focused on the AC and noise analysis and optimization of the amplifiers, which was designed the previous chapter. The main goal of this analysis is to understand the relationships between the design parameters (like size of the transistors) and the main amplifier characteristics. Regarding this, we focus mainly on the analytical description of the amplifiers. The conclusions are confirmed by simulation and by the measurements performed on the integrated silicon circuits (see *chapter 7*).

6.1.1 AC Response of Folded Cascode Transconductor

The general concept of the voltage amplification was previously introduced in *chapter 4* (*Fig. 4.5*). Here, the amplification is provided by the input transconductor (OTA) connected to the resistive load. It has been demonstrated that in such a configuration, the dominant pole is caused by the high impedance node, *i.e.* time constant $r_L.c_L$ defined in *Eq.*(4-5). In this case, we expect that the differential pair (transconductor) delivers the output current i_L constant up to the dominant pole frequency.

Fig. 6.1 shows the differential folded cascode structure presented in *sub-section 5.4.2*, with two important capacitances. The figure also shows the voltage transfer between the differential inputs and the nodes labelled (A) and (B).

The node (A) is a common node of the differential pair and (B) the output current node. The voltage transfers $v_{in} \rightarrow v_A$ and $v_{in} \rightarrow v_B$ shown in *Fig. 6.1* can be used to demonstrate the influence of parasitic capacitances on the frequency response of the amplifier.

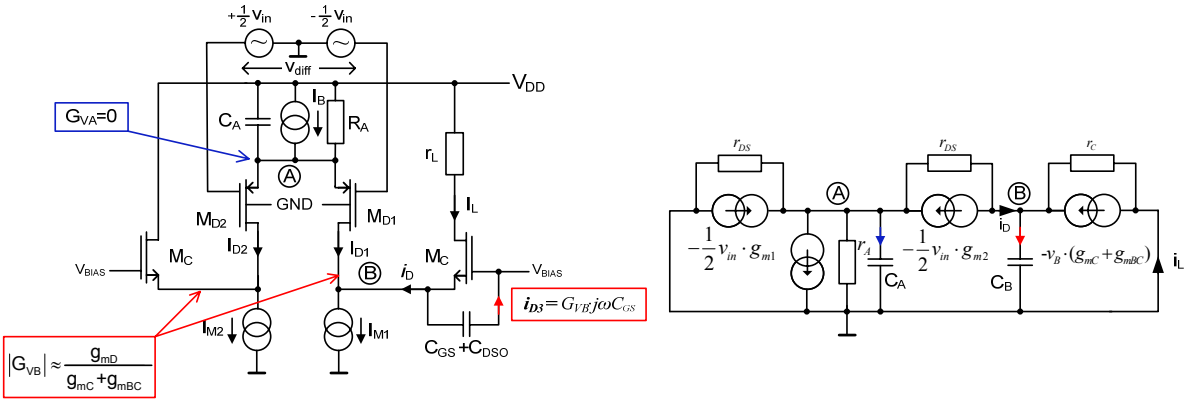


FIG. 6.1: *a) Simplified AC model of the input differential pair and b) linearized model. $g_{m1,2}$ and g_{mC} refer to the transconductances of the input pair (Eq. (5-48)) and cascode transistors, g_{mBC} refers to the bulk conductance of M_C*

Due to the symmetry in the common node (A), the voltage transfer $v_{(A)}/v_{in}$ is ideally zero for a symmetrical input voltage (*i.e.* $V_{GS,D1} = -V_{GS,D2}$). Thus, there is no current through $C_{(A)}$, and in the first approximation the capacitor $C_{(A)}$ does not contribute to i_L/v_{in} current transfer.

However, the situation is different for node (B). It has been demonstrated that the current delivered by the input differential pair is given by the input voltage and *transconductance of differential pair* g_{mDiff} (*Eq*. (5-48)). From the output current of the input differential pair $i_{D1} = g_{mDiff} \cdot v_{in}$ results a voltage drop across the resistance appearing in node (B):

$$v_{(B)} = \frac{i_{D1}}{g_{(B)}} = \frac{v_{in} \cdot g_{mD}}{\left(g_{mC} + g_{mB}\right)}, \tag{6-1}$$

where g_{mC} and g_{mB} are the transconductance and substrate transconductance of M_{C1}, respectively (*Fig. 6.1 b*). The voltage gain $v_{(B)}/v_{in}$ at node (B) can be obtained as:

$$G_{v(B)} = \frac{g_{mD}}{g_{mC} + g_{mB}}. \tag{6-2}$$

It is obvious that this voltage generates a current through $C_{(B)}$. In fact, the current $g_{mD} \cdot v_{in}$ provided by the differential pair is reduced by the ratio of cascode transistor drain impedance $1/g_{(B)}$ and the impedance of capacitor $C_{(B)}$. Accordingly, the output current i_L can be written as:

$$i_L = i_D - i_{C_{(B)}}. \tag{6-3}$$

This can be written in the terms of frequency transfer i_L/v_{in} corresponding to the *effective transconductance of differential folded cascode OTA* $g_{m,tot}$:

$$g_{m,tot} = \frac{i_L(j\omega)}{v_{in}} = \frac{g_{mD}}{1 + j\omega C_{(B)} \big/ \left(g_{mC} + g_{mB}\right)}, \tag{6-4}$$

This relationship shows how the capacitors $C_{(B)}$ affects the output current i_L of the folded cascode structure; it create an extra pole, located at frequency $p_1 \approx g_{mC}/C_{(B)}$ (g_{mB} was neglected here).

The simulation has shown that this pole can be located close to the dominant pole of the amplifier, caused by the high impedance node. Therefore, the function (6-4) can be used as a criterion of optimization, based on any mathematical numerical method such as a simplex method. By applying this method, optimal values of W_C and L_C can be found. The goal is to keep the transconductance of cascode transistors g_{mC} as high as possible, but only until the C_{GS} capacity ($\sim W_C \cdot L_C$) affects the frequency response. The pole of the transfer function (6-4) can be rewritten in the terms of transistor parameters (*Eqs.* (2-26), (2-32) and *Tab 2.1*), and its value can be minimized:

$$p_1 \approx \frac{g_{mC}}{C_{(B)}} = \frac{\sqrt{2 \cdot KP_N \frac{W_C}{L_C} \cdot I_L}}{C_{GDO} \cdot \left(W_{D1} + W_{MB6}\right) + \frac{2}{3} \cdot C_{OX} \cdot W_C \cdot L_C} \Rightarrow \min. \tag{6-5}$$

In this function, the term $C_{GDO} \cdot (W_{D1} + W_{MB6})$ is the contribution of transistors M_{D1} and M_{D6} to the total capacitor $C_{(B)}$ (*Fig. 5.18*). Applied to this *Eq*.(6-5), the simplex method has been used to find the following optimum: $L_C = 5$ µm and $W_C = 50.33$ µm, for initial conditions $C_{OX} = 0.0023$ *F/m*, $W_D = 2350$ µm, $W_{MB1} = 501$ µm, $KP_N = 80$ µA/V^2, $I_L = 25$ µA, $C_{GDO} = 130$ pF/m.

A simulation has validated this optimum by sweeping the parameter W_C around 50 µm. However, a relatively low transconductance g_{mC} penalized the cascode effect (*Eq*. (5-35)), which lead us to an increase of the W_C to the final value of 100 µm.

tel-00417838, version 1 - 17 Sep 2009

6.1.2 Analysis of the low-g_m Composite Transistor

The basic analysis of low transconductance composite transistor providing the values of the large and small signal transconductances was carried out in *section 5.3.5*. A detailed linearized model of the low g_m composite transistor from *Fig. 5.9* is shown in *Fig. 6.2*. This model contains five controlled current sources (transistors M_n), the drain resistances r_{DSn} and the nodal capacitances $C_{GS,n}$. In the first phase, previously obtained transconductance g'_m (5-26) can be precise by a low frequency (DC) analysis including the channel resistance $r_{DS,n}$ for each transistor.

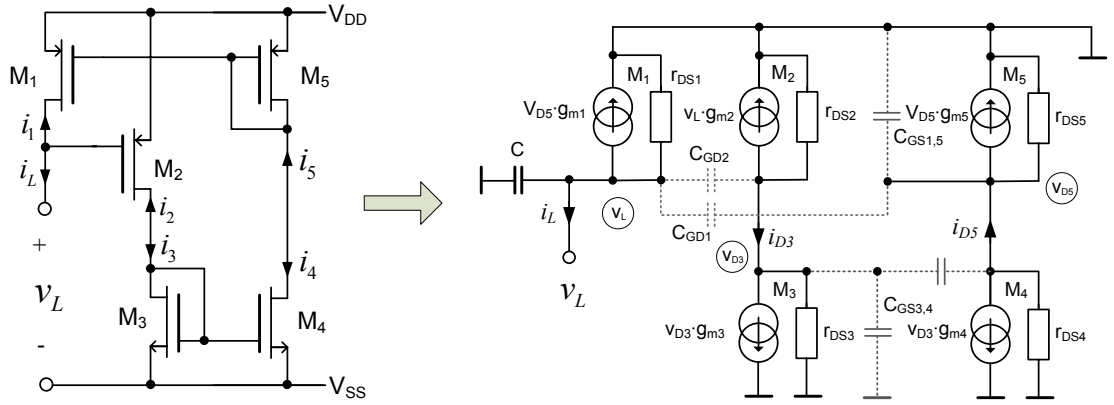


FIG. 6.2: *low transconductance composite transistor and its small signal model*

This transconductance g''_m can be found as i_L/v_L at the output node v_L, where the expression result in:

$$g''_m = \underbrace{\frac{g_{m1}\cdot g_{m2}\cdot g_{m4}}{g_{m5}\cdot g_{m3}}}_{g'_m} \cdot \underbrace{\left\{ \frac{1+\dfrac{g_{DS1}}{g_{m1}\cdot g_{m2}\cdot g_{m4}}\cdot\left(g_{m5}\cdot g_{m3}+g_{m3}\cdot g_5+g_{m5}\cdot g_2+g_5\cdot g_2\right)}{1+\dfrac{g_2}{g_{m3}}+\dfrac{g_5}{g_{m5}}+\dfrac{g_5\cdot g_2}{g_{m3}\cdot g_{m5}}} \right\}}_{\approx 1} \tag{6-6}$$

The notation g_n corresponds to the sum of transconductances at the common nodes, as shown in *Fig. 6.2* (*i.e.* $g_3 = g_{DS2}||g_{DS3}$, $g_5 = g_{DS5}||g_{DS4}$). This equation illustrates that the most important channel resistance (with respect to the total conductance g''_m) is r_{DS1}, because the drain of M_1 is the node with highest impedance in the circuit.

The analytical AC analysis of the circuits shown in *Fig. 6.2* gives a complicated result, which is difficult to interpret. However, as already noticed, the elements limiting the frequency bandwidth are the parasitic capacitances at the high impedance node; this is illustrated by the capacity C in *Fig. 6.2*. In the MOS transistor, the input impedance is dominated by C_{GS} (see *chapter 2*). Applied to the low-g_m transistor (*Fig. 6.2*), the capacitance C is determined mainly by the capacitors C_{GS2} of transistor M_2. Consequently, a parasitic zero can appear in the trivial form of frequency-dependent transconductance $g'_m(j\omega)$:

$$g'_m(j\omega) \cong g'_m\left(1+j\omega\frac{C_{GS2}}{g'_m}\right), \tag{6-7}$$

which determines the previously mentioned *dominant pole of the amplifier*. Consequently, more detailed analysis, including all parasitic capacitances shown in *Fig. 6.2* was performed. The result is a complicated polynomial transconductance of the form:

tel-00417838, version 1 - 17 Sep 2009

$$g_m'(j\omega) = \frac{N(j\omega)}{M(j\omega)} \tag{6-8}$$

where $N(j\omega)$ and $M(j\omega)$ are the 3rd and 2nd order polynomials, respectively. The ratio of the orders of $N(j\omega)$ and $M(j\omega)$ being higher than unity is advantageous, because it causes a natural decrease of the voltage gain at higher frequencies (*e.g.* removes possible oscillations, excessive noise etc.). This situation is illustrated by the sets of simulations shown in *Fig. 6.3*, where the transconductance of low-g_m composite load and the transconductance g_{mDiff} of the differential pair have been plotted in a Bode diagram (performed on *type I* amplifier from *Fig. 5.18*).

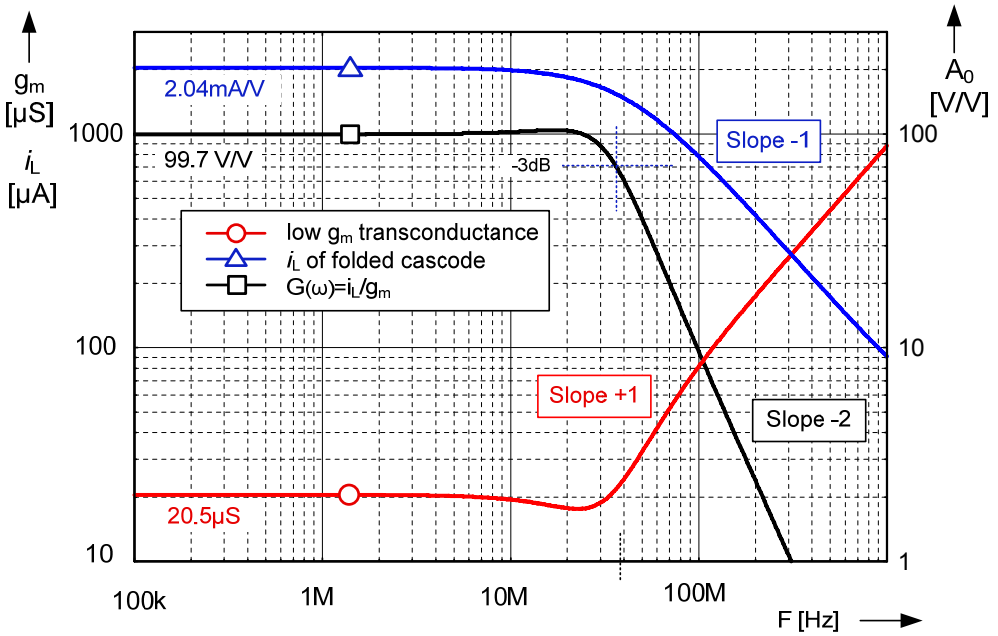


FIG. 6.3: *Frequency characteristic of differential pair transconductance g_{mDiff} and composite transistor transconductance $g'_{m,tot}$, their product $g_{mD}g'_{m,tot}$ corresponding to the voltage gain (simulation was performed with no additional capacitive load at the output node, SPICE level-7 model)*

In this figure, we can observe the cut-off frequencies of g_{mDiff} and $g'_{m,tot}$ to be close to each other (~ 30 MHz), causing a slope of the AC characteristic of -40 dB/decade. Moreover, we observe a small resonance at f = 25 MHz, caused by the complex poles in $M(j\omega)$.

Fig. 6.3 simulation assumes ideal conditions, where no load is connected to the high impedance node. However, this node is loaded by additional capacitances, as the input capacitance of voltage buffer or by the routing capacitance. This causes an increase of the value C and resulting decrease of the amplifier bandwidth. This decrease removes the resonance shown in *Fig. 6.3* and makes the frequency response naturally flat (see simulation in *Fig. 5.20* provided with the output buffer – circuit from *Fig. 5.18*).

6.1.3 Common Mode Rejection Ratio and the Gain Symmetry

The *Common Mode Rejection Ratio CMRR* is another parameter which can influence the frequency response of the differential amplifier. The CMRR compare the rejection of common voltage $(V_+ + V_-)/2$ to the amplification of the input differential voltage $(V_+ - V_-)$. Generally, the voltage transfer of a differential amplifier can be written in terms of differential and common mode voltage gain G_v and G_C as:

tel-00417838, version 1 - 17 Sep 2009

$$V_{OUT} = \underbrace{G_v \cdot (V_+ - V_-)}_{\text{diff voltage}} + \underbrace{G_C \cdot \frac{1}{2}(V_+ + V_-)}_{\text{common mode voltage}}, \tag{6-9}$$

where typically $G_v >> G_C$. CMRR is defined as a positive dB ratio of the differential gain G_v and common mode gain G_C:

$$CMRR = 20 \cdot \log \cdot \frac{|G_v|}{|G_C|}. \tag{6-10}$$

Measurement of the common mode gain G_C is typically performed as the transfer between shorted differential inputs and the single ended amplifier output. It is known that the CMRR of a differential amplifier is depended on the parasitic impedance at the common node (A). However, the impedance $Z_{(A)}$ may also affect another parameter: *the amplifier symmetry*. This is why a superposition principle will be unusually used in this section in order to express the individual transfers ($G_{v+} = v_{out}/v_{in+}$ and $G_{v-} = v_{out}/v_{in-}$). When doing so, a *symmetry of the voltage gain* $G_{v+} = G_{v-}$ can be verified and individual transfers G_{v+} and G_{v-} allow us to determine both CMRR and differential voltage gain. In a further analysis, only the simplified model of input differential pair (*Fig. 6.4*) containing the parasitic r_A and C_A, will be used.

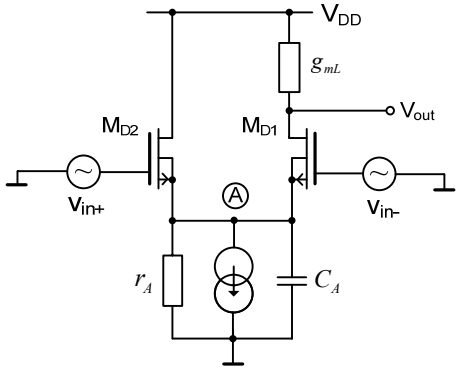


FIG. 6.4: *Simplified model of the input differential pair*

The individual voltage transfers G_{v+} and G_{v-} are defined between the amplifier output and the corresponding input. In such a configuration, the differential voltage gain $G_v = v_{out}/v_{in}$ can be defined by G_{v+} and G_{v-} as $G_v = ½(G_{v+} - G_{v-})$, and the G_C remain $½\cdot(G_{v+} + G_{v-})$, as defined by *Eq.*(6-9). The G_{v+} and G_{v-} are expected to be equal within whole frequency range.

Transfer G_{v+} results from the drain current of M_{D2}, which is divided in the node (A) between the parasitic impedance ($r_A||C_A$) and the load g_{mL} as:

$$G_{v+} = \frac{v_{out}}{v_{in+}} = \frac{1}{2} \cdot \frac{g_{m1}}{g_{mL}} \cdot \frac{1}{\left(1 + \frac{g_A}{2g_{m1}} + \frac{C_A}{2g_{m1}} \cdot s\right)}, \tag{6-11}$$

where the transconductance of input transistors M_{D1} and M_{D2} are referred to as g_{m1}. Similarly the transfer G_{v-} results in:

$$G_{v-} = \frac{v_{out}}{v_{in-}} = -\frac{1}{2}\frac{g_{m1}}{g_{mL}} \cdot \frac{\left(1 + \frac{g_A}{g_{m1}} + \frac{C_A}{g_{m1}} \cdot s\right)}{\left(1 + \frac{g_A}{2g_{m1}} + \frac{C_A}{2g_{m1}} \cdot s\right)}. \tag{6-12}$$

tel-00417838, version 1 - 17 Sep 2009

These two equations show that the MOS input differential pair is not perfectly symmetrical. The symmetric behaviour will be verified by simulation in the following.

The superposition of transfers (6-11) and (6-12) allows us to determine the differential voltage gain as the familiar transconductance ratio (see *Eq*. (5-53)):

$$G_v = \frac{1}{2}\cdot\left(G_{v+} - G_{v-}\right) = \frac{1}{2}\cdot\frac{g_{m1}}{g_{mL}}. \tag{6-13}$$

We can see that the differential gain is not affected by the impedance of the common node (A), only for the "ideal" differential signal (*i.e.* $V_+ = -V_-$). As mentioned above, this signal results in zero voltage $v_{(A)}$, and the impedance $Z_{(A)}$ has no impact on the voltage gain (we assume that the bias current of M_{D1} and M_{D2} is constant). In other cases, the consideration of individual transfers may be important.

The common mode gain G_C, contains one zero and one pole in transfer function:

$$G_C = \left(G_{v-} + G_{v+}\right) = -\frac{1}{2}\cdot\frac{1}{g_{mL}}\cdot\frac{g_A\cdot\left(1+\frac{C_A}{g_A}\cdot s\right)}{\left(1+\frac{g_A}{2g_{m1}}+\frac{C_A}{2g_{m1}}\cdot s\right)}, \tag{6-14}$$

where the numerator transfer zero causes the *common mode gain to increase at high frequencies*. By inspecting the *type I* amplifier *Fig. 5.18*, we can deduce that g_A is primarily determined by the r_{DS} of the current source M_{B2} and capacitances C_{GS} of M_{D1} and M_{D2} input transistors. Accordingly, the CMRR can be expressed following the definition (6-10) as the log ratio:

$$CMRR = 20\cdot\log\frac{|G_v|}{|G_C|} = 20\cdot\log\left|-\frac{2\cdot g_{m1}+g_A+C_A\cdot s}{2\left(g_A+C_A\cdot s\right)}\right|, \tag{6-15}$$

reaching at low (DC) frequency:

$$CMRR_{DC} = CMRR\big|_{s\to 0} = 20\cdot\log\left|-\frac{2\cdot g_{m1}+g_A}{2\cdot g_A}\right|. \tag{6-16}$$

These equations show the above mentioned dependence of the CMRR on the impedance $Z_{(A)}$, witch value is to be maintained at a very high value.

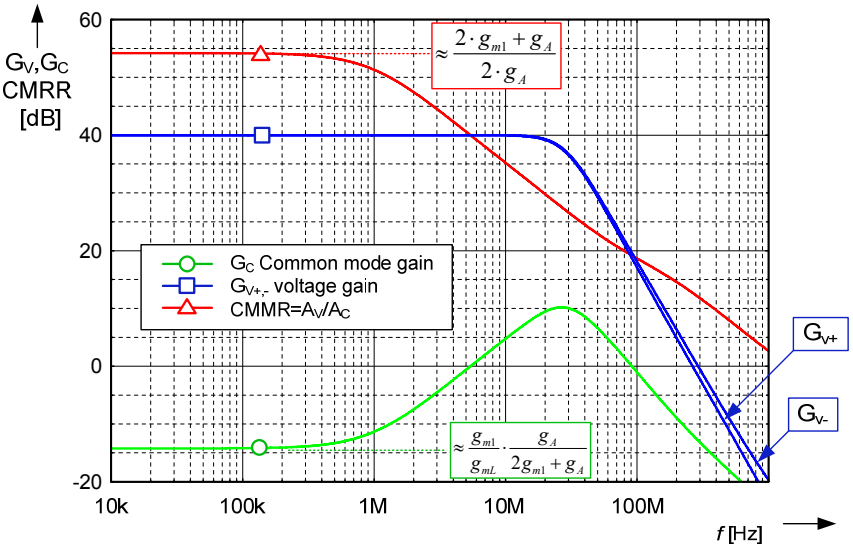


FIG. 6.5: *Simulated Gv+ and Gv- AC characteristic, AC common mode transmission and CMRR characteristics (simulation SPICE level-7 models, type I amplifier)*

tel-00417838, version 1 - 17 Sep 2009

Verification of the analysis is provided by simulations (*Fig. 6.5*) performed with accurate models applied to *Fig. 5.15 type I* amplifier. In *Fig. 6.5*, a low common mode transfer G_C can be observed up to the frequency of transfer zero frequency which is close to 1 MHz (6-14). At higher frequencies, the value of G_C is limited by the amplifier voltage gain, having a decreasing tendency with -40 dB/dec slope.

Focusing on G_{v+} and G_{v-}, a negligible difference between both voltage transfers can be observed at higher frequencies. This allows us to consider the amplifier to be fully-differential.

A last comment can be made on the temperature dependence of the amplifier bandwidth. In *Eq.*(6-7), the dominant pole was defined by the transconductance of the low g_m composite load and parasitic capacitance C_{GS2}. In *chapter 5.1* we have investigated the temperature behaviour of the MOS transistor. It has been demonstrated that the transconductance increases at low temperatures, as the consequence of the higher carrier mobility μ_x (*Eq.*(5-1)). Considering this fact, the frequency bandwidth is expected to increase at lower temperatures, which is advantageous for cryogenic operations (see the simulated characteristic $G_0(T)$ in *Fig. 5.20* for *type I* amplifier, or the wide temperature range measurements provided in the next chapter).

6.2 Noise of the Amplifier

In this section we provide the amplifier analysis allowing to determine the elements having an impact to the total amplifier noise. The relationship between the input-referred noise and component values are highlighted here as an important criterion for the amplifier design. In the following analysis, we consider noise-free signal sources only.

One of the main advantages of the amplifier shown in *Fig. 4.10* is the absence of external feedback. This would allow to remove an important contributor of the total noise, as compared to the classical concept of closed loop amplification. The aim of the analysis is to find a methodology reducing the noise by transistor sizing and design of operating points, for instance.

In *sub-section 3.5.2*, the principal noise source in the transistor MOS was defined as the channel noise current:

$$i_n^2 = \frac{8}{3} k_B T g_m + KF \frac{\left|I_{DS}\right|^{AF}}{C_{OX} \cdot L_{eff}^2 \cdot f^{EF}}, \tag{6-17}$$

where the first term is related to the white noise and second to the flicker noise 1/*f*. In this chapter, two different contributions of amplifier noise will be analysed: *i*) noise provided by the input differential pair $i_{n,L}$, and *ii*) noise generated by the amplifier load $i_{n,gm}$. The total output noise can be written as the voltage drop on the load resistance r_L caused by uncorrelated currents $i_{n,L}$ and $i_{n,gm}$:

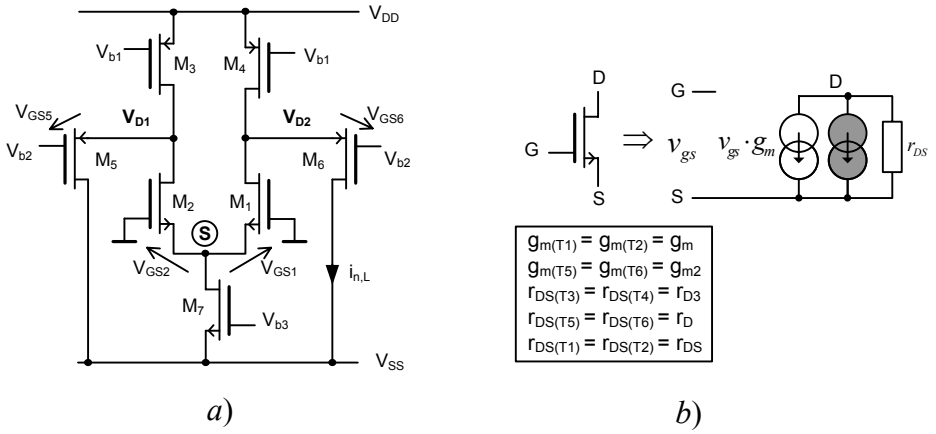
$$v_{n,out}^2 = \left(i_{n,gm}^2 + i_{n,L}^2\right) \cdot r_L^2 \quad . \tag{6-18}$$

6.2.1 Noise of the MOS Input Differential Pair

Differential folded cascode transconductor contains elements, which are responsible for the majority of the amplifier noise. The total noise can be computed as individual transfers for each noise source towards the output. In the mathematical analysis, we consider only the white noise, whereas the 1/*f* noise will be analysed by the simulation.

A schematic view of the input amplifier part is shown in *Fig. 6.6*. In order to simplify the analysis, we use a notation that is shown in *Fig. 6.6*, grouping the symmetric components (transistors).

tel-00417838, version 1 - 17 Sep 2009



a) *b*)

FIG. 6.6: *a) Schematic view of the differential folded cascode used for noise analysis; b) equivalent noise model of the transistor MOS (Fig. 3.8)*

Since the noise current is generated only in the CMOS structure, the gate voltages of input transistors M_{D1}, M_{D2} are set to zero. The circuit of differential folded cascode transconductor (*Fig. 6.6*) can be redrawn into a linearized small signal circuit, which is shown in *Fig. 6.7*. In this figure the dark current sources represent the noise currents of transistors (*i.e.* represent *Eq.*(6-17)).

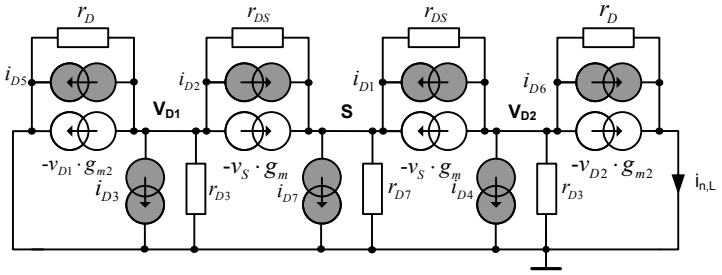


FIG. 6.7: *Small-signal equivalent circuit of differential folded cascode OTA from Fig. 6.6 a)*

The total output noise $i_{n,L}$ results from the transfer of all particular noise sources to the output node. We can write a set of nodal equations in the following matrix form:

$$\begin{bmatrix} g_D + g_{D3} + g_{DS} - g_{m2} & -g_m - g_{DS} & 0 \\ -g_{DS} & -2\cdot g_m + g_{D7} + 2\cdot g_{DS} & -g_{DS} \\ 0 & -g_m - g_{DS} & g_D + g_{D3} + g_{DS} - g_{m2} \end{bmatrix} \cdot \begin{bmatrix} V_{D1} \\ V_S \\ V_{D2} \end{bmatrix} = \begin{bmatrix} -i_{D5} - i_{D3} - i_{D2} \\ -i_{D2} - i_{D1} + i_{D7} \\ -i_{D1} - i_{D6} - i_{D4} \end{bmatrix}, \quad (6\text{-}19)$$

where $i_{D,n}$ are the noise currents (6-17) of relevant transistors. The output current $i_{n,L}$ can be found from the node voltage v_{D2} as:

$$i_{n,L} = -v_{D2} \cdot \left(g_{DS} - g_{m2} \right) + i_{D6} . \quad (6\text{-}20)$$

The analytic form of $i_{n,L}$ resulting form (6-20) can be simplified by imposing:

$$g_D = g_{D3} = g_{D7} = g_{DS} . \quad (6\text{-}21)$$

This allows us to find a general expression of the total output noise $i_{n,L}$. For convenience and in order to provide an expression dealing only with the transconductances g_m, we assume that $g_{DS} \to 0$. $i_{n,L}$ can be obtained as the sum of uncorrelated noise currents $\overline{i}_{D,x}^2$:

$$\overline{i}_{n,L}^2 = \frac{1}{4}\overline{i}_{D1}^2 + \frac{1}{4}\overline{i}_{D2}^2 + \frac{1}{4}\overline{i}_{D7}^2 + \overline{i}_{D4}^2 = \frac{1}{2}\overline{i}_{D1,2}^2 + \frac{1}{4}\overline{i}_{D7}^2 + \overline{i}_{D4}^2 , \quad (6\text{-}22)$$

tel-00417838, version 1 - 17 Sep 2009

where the term $i_{D1,2}$ is the sum of M_1-M_2 noise currents. This equation shows a meaningful contributions of each transistor to the value of total output noise $i_{n,L}$. By considering the output noise voltage $v_{n,out} = i_{n,L} \cdot r_L$ (we neglect the noise provided by the low g_m composite load) the equivalent input-referred noise $v_{n,in}$ can be derived in following form:

$$v_{n,in}^2 = \frac{v_{n,out}^2}{G_0^2} = \frac{8}{3} k_B T \cdot \frac{\left(\frac{1}{2} g_{mDiff} + \frac{1}{4} g_{m7} + g_{m4}\right) \cdot r_L^2}{g_{mDiff}^2 \cdot r_L^2} = \frac{8}{3} k_B T \left(\frac{1}{2} \cdot \frac{1}{g_{mDiff}} + \frac{1}{4} \cdot \frac{g_{m7}}{g_{mDiff}^2} + \frac{g_{m4}}{g_{mDiff}^2} \right), \quad (6\text{-}23)$$

where G_0 is the differential gain of the amplifier and g_{mDiff} refers to the transconductance of the differential pair, *Eq.*(5-48). In this expression, the last term shows the methodology of the design allowing reduction of the input referred noise voltage $v_{n,in}$: the aim is to make the transconductance of differential pair g_{mDiff} large compared to g_{m7} and g_{m4}. This equation (6-23) also shows the expected zero contribution of cascode transistors M_5 and M_6 and the zero contribution of transistor M_3.

6.2.2 Noise of the Low Transconductance Composite Transistor

The transistors used in the low-g_m composite load (amplifiers from *Fig. 5.18* and *Fig. 5.23*) can also contribute to the total input referred noise. In the following, the current noise $i_{n,gm}$ and resulting voltage drop $v_{n,gm}$ on the low g'_m transistor will be investigated. The noise model corresponding to the composite load (*Fig. 5.9*) is drawn in *Fig. 6.8*, where R_{OUT} is the output resistance of the folded cascode stage, defined by *Eq.* (5-35) ($R_{OUT} >> 1/g'_m$).

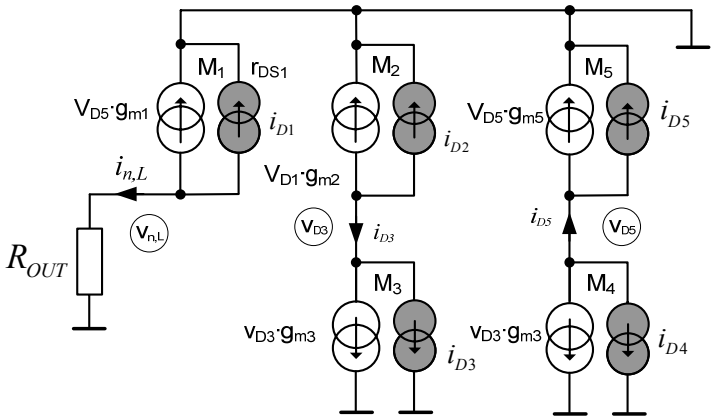


FIG. 6.8: *Noise model of the low gm composite transistor connected to the output resistance of the differential folded cascode (R_{OUT})*

In order to determine the total noise current $i_{n,gm}$ the superposition of uncorrelated noise sources i_{D1} - i_{D5} can be used. The current generated by the composite load (passing through the resistance R_{OUT}) can be written as the inter-nodal transmission from each current source $i_{D1\text{-}5}$ to the load resistance R_{OUT}:

$$i_{n,g_m}^2 = \frac{i_{D1}^2 \cdot \left(g_{m3} \cdot g_{m5}\right)^2 + \left(i_{D4}^2 + i_{D5}^2\right) \cdot \left(g_{m1} \cdot g_{m3}\right)^2 + \left(i_{D2}^2 + i_{D3}^2\right) \cdot \left(g_{m1} \cdot g_{m4}\right)^2}{\left(R_{OUT} \cdot g_{m1} \cdot g_{m2} \cdot g_{m4} + g_{m3} \cdot g_{m5}\right)^2} = \quad (6\text{-}24)$$

$$= \frac{i_{D1}^2 + \alpha_2^2 \cdot \left(i_{D4}^2 + i_{D5}^2\right) + \alpha_1^2 \cdot \alpha_2^2 \cdot \left(i_{D2}^2 + i_{D3}^2\right)}{\left(R_{OUT} \cdot g'_m + 1\right)^2},$$

tel-00417838, version 1 - 17 Sep 2009

where for $R_{OUT} \rightarrow \infty$, then $i_{n,gm} \rightarrow 0$. The values of α_1 and α_2 refer to g_{m4}/g_{m3} and g_{m1}/g_{m5}, as defined in *Eq.*(5-23). The noise current $i_{D,x}$ of each transistor can be expressed by transconductance $g_{m,x}$ following *Eq.*(6-17). The resulting noise $v_{n,gm}$ of the low-g_m composite load can be written as:

$$v_{n,g_m}^2 = \frac{8}{3} k_B T \cdot \frac{R_{OUT}^2 \left\{ g_{m1} + \alpha_2^2 \cdot (g_{m4} + g_{m5}) + \alpha_1^2 \cdot \alpha_2^2 \cdot (g_{m2} + g_{m3}) \right\}}{\left(R_{OUT} \cdot g_m' + 1 \right)^2} \tag{6-25}$$

$$\text{and for } \left(R_{OUT} \cdot g_m' \right) >> 1: \quad v_{n,g_m}^2 \cong \frac{8}{3} k_B T \cdot \frac{1}{\left(g_m' \right)^2} \left\{ g_{m1} + \underbrace{\alpha_2^2}_{<1} \cdot (g_{m4} + g_{m5}) + \underbrace{\alpha_1^2 \cdot \alpha_2^2}_{<<1} \cdot (g_{m2} + g_{m3}) \right\}.$$

A last simplification can be done by assuming $R_{OUT} >> 1/g'_m$. To express an approximate value of $v_{n,gm}$, the operating points listed in *Tab. 5.7* can be inserted in *Eq.*(6-25). Consequently, $v_{n,gm}$ add 28.8 n*V*/√*Hz* of the noise voltage. The input-referred noise resulting from (6-25) is therefore $v_{n,gm}/G_0 = 0.28$ *nV*/√*Hz*. Obviously, this value is negligible as compared to the estimated noise caused by the input differential pair (being in the order of *nV*/√*Hz*).

It is interesting to compare the noise of the low-g_m transistor (*Fig. 6.8*) with an equivalent resistor having the value $1/g'_m$ ($g'_m = 20.5$ µS, *Fig. 6.3*). The 40 dB gain of amplifier can be realised with an equivalent load resistor $r_L = 1/20.5$ µS generating the noise voltage:

$$v_{n,g_m}^2 = \frac{4k_B T}{g_m'} = 4k_B T \cdot \left(\frac{g_{m3} \cdot g_{m5}}{g_{m2} \cdot g_{m1} \cdot g_{m4}} \right), \tag{6-26}$$

reaching 28.3 n*V*/√*Hz @ 290 K* ,which is very close to the value obtained with *Eq.*(6-25).

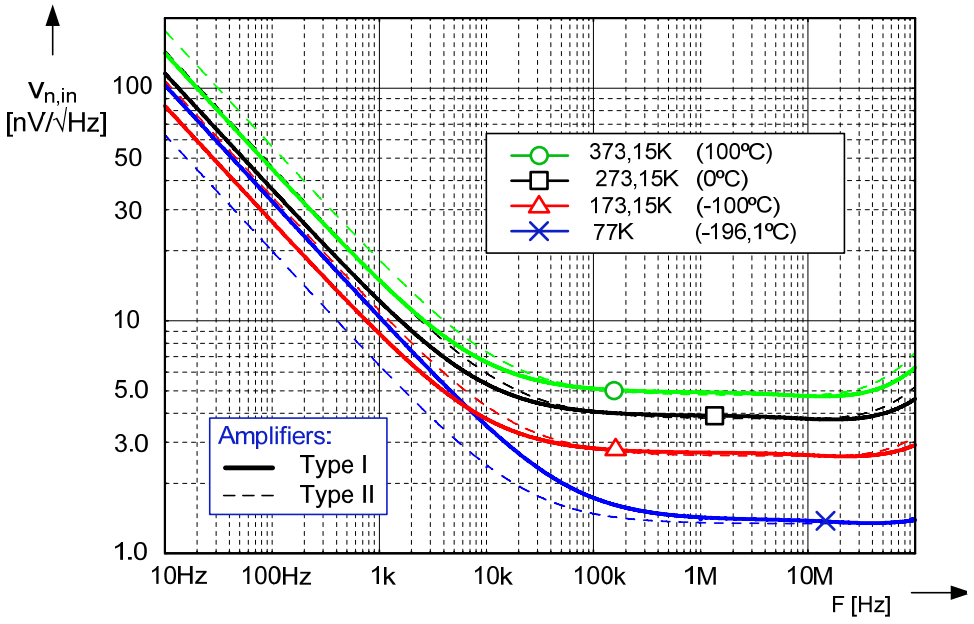


FIG. 6.9: *Simulated (SPICE level-7) input-referred noise voltage (spectral density) of both amplifiers: from Fig. 5.18 (type I) and Fig. 5.24 (Type II)*

6.3.3 Noise Characteristic of the Amplifiers

Results provided by the analysis were used in the design and optimization of the amplifiers presented in the previous chapter. Afterwards, the noise characteristics that are displayed in *Fig. 6.9* were obtained by simulation with SPICE level-7 model. We can see that the simulated white noise reaches

tel-00417838, version 1 - 17 Sep 2009

approximately 4 $nV/\sqrt{Hz}$ at room temperature for both, *type I* and *type II* amplifiers. Such a noise level, as well as the low corner frequency (~ 10 kHz), is a very good result for differential amplifiers realised in a classical silicon CMOS process. In the design, the corner frequency is primarily related to the use of transistors having a large surface $W \cdot L$ as well as to the relatively good quality of the AMS 0.35 µm CMOS process.

The simulations were performed for a wide range of temperatures. As we have already noticed, the accuracy of models at lower (cryogenic) temperatures is limited and concerning the noise, was not verified by the measurements. Nevertheless the simulation can give an idea about the noise temperature dependence. In *Fig. 6.9* a slight increase of $1/f$ noise when approaching the cryogenic temperatures can be observed. This increase is, however, a common property of the MOS circuits. On the contrary, the decrease of white noise is related to the Johnson formula (6-17), which is function of temperature. Accordingly, a very low amplifier thermal noise is observed at cryogenic temperature (T = 77 K): $\boldsymbol{v_{n,in} = 1.5\ nV/\sqrt{Hz}}$.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

7 Integration in CMOS AMS 0.35 µm: Results

7.1 Layout of the Differential Amplifiers

The differential amplifiers designed in the previous chapters have been laid out and fabricated as an ASIC (Application Specific Integrated Circuit) with 3×3 µm^2 die size. As defined in *chapter 4*, the objective of the design was to develop compact readout electronics, applied to a four-pixel bolometric array of detectors. This led us to integrate the following components into the circuit:

- **4 geometric-ratio fixed-gain amplifiers** (*Type I* amplifier *Fig. 5.18*);
- **1 geometric-ratio fixed-gain amplifier (A5) for testing purposes** (*Type I, Fig. 5.18*);
- **2 linear temperature-compensated *type II* amplifiers (*Fig. 5.24*) with their output buffers (*Fig. 5.28*);**
- **1 linear temperature-compensated amplifier (*type II Fig. 5.24*) without output buffer;**
- **Circuit described in the following *chapter 10*: second generation current conveyor CCII-.**

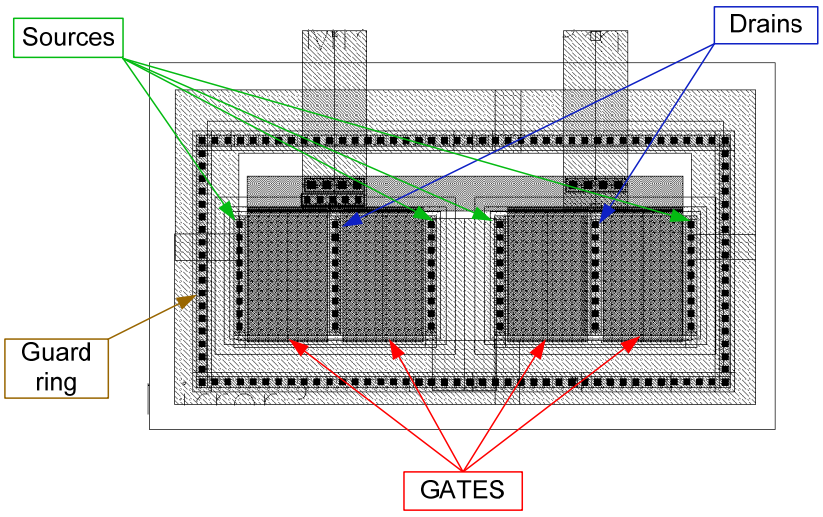


FIG. 7.1: *Layout of the mask for a simple current mirror (W/L=15 µm/5 µm)*

The goal of the layout was to achieve good electrical performances of the circuit, from the first fabrication's run. In particular, the high accuracy of the voltage gain or low DC offset voltage of the *Type II* amplifier can be affected by the quality of the layout. Accordingly, the geometric structures minimizing the dispersion of process parameters were used.

7.1.1 Matching of the MOS Transistors

As it has been mentioned in the previous chapters, good component matching is a general feature of the CMOS process. This advantage is widely used in circuits such as the SC (Switched Capacitor) or SI (Switched Current) devices. However, good performances can be impaired by a poor layout. A generally recommended rule in the design is to use transistors having a large $W/L > 1$. This was one stimulus leading to the design of the low transconductance composite transistor, where all W/L reach acceptable values of $\approx (3 - 10)$.

In the CMOS, a good uniformity of parameters (*e.g.* t_{OX}) across the wafer is generally achieved. Nevertheless, special layout techniques can improve transistor matching. Consequently, the parameter mismatch of properly designed CMOS circuits can be much below 1 %.

In our design, we strived to provide:

- **perfect matching of all current mirrors, namely in the low-g_m circuit;**
- **perfect matching of input differentia-pair MOS transistors.**

Besides the mentioned objectives of gain accuracy, the perfect matching of the input differential pair is important to provide a low DC offset voltage, important namely for the *type II* linear amplifier design.

7.1.2 Symmetric Layout, Common Centroid Structure

Systematic mismatch in CMOS refers to a spatial gradient of the component values. This spatial gradient becomes more problematic as component length increase (*e.g.* see *Fig. 5.18*, where transistors of $W = 2500\mu m$ are used).

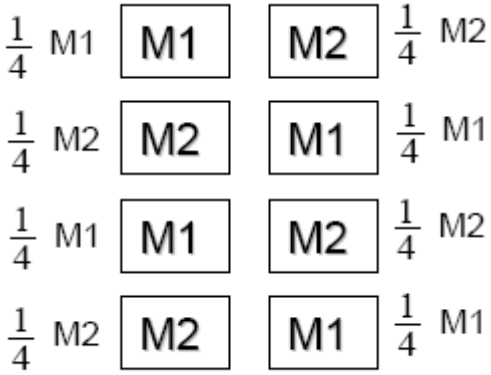


FIG. 7.2: *Geometry of the common centroid layout of the input differential pair; each transistor is separated in four isolated devices*

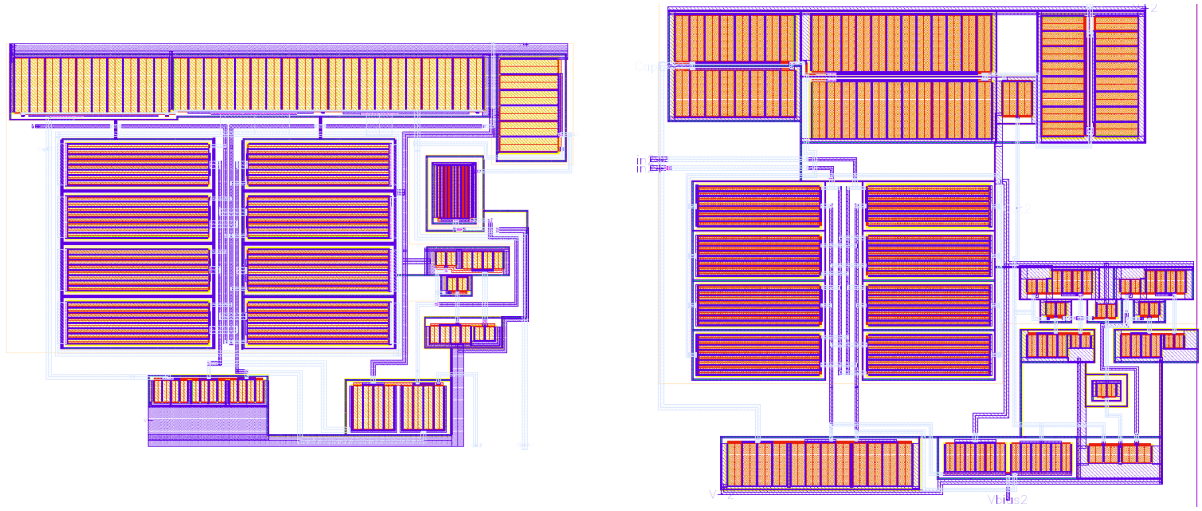
In this case, a technique commonly used is the transistor "compression" into a concentrated area (ideally being a square [22]). For this reason the transistor are commonly laid out using multi-gate fingers, distributed around some central point. The idea is to design a long device as an array of n parallel transistors reducing the length to W/n. An example is shown in a layout of a current mirror *Fig. 7.1*, where two transistors $W/L = 15/5$ μm are nearly square.

For long enough devices where n could reach a high value, it is more advisable to disassociate the device into several segments and to use the so-called "*common centroid*" configuration, *Fig. 7.2*.

tel-00417838, version 1 - 17 Sep 2009

7.1.3 Layout of the Amplifiers

The layout of the circuit has been performed in Cadence® environments with AMS 0.35 µm design kit. The amplifier cells have been routed on a small surface of approximately 0.1×0.15 µm^2. The layout for both amplifiers *is* shown in *Fig. 7.3*. We can observe that the largest surface is occupied by the input differential pair. This is split into four transistors, respecting *Fig. 7.2* common centroid configuration.



a) *b*)

FIG. 7.3: *a) Layout of the type I geometric ratio fixed-gain amplifier; b) type II linear, temperature compensated amplifier*

The fabricated chip containing all integrated components is shown on the microphotography *Fig. 7.4*. The perimeter contains 80 input/output and power supply contacts. We can distinguish five geometry-fixed amplifiers on the upper side and three temperature-compensated amplifiers on the left. The central and right parts are occupied by the integrated 1.5 MHz active frequency filter and by current conveyors CCII-, which will be described in the following chapters.

7.2 Testing the Amplifiers

The electrical testing of integrated amplifiers is focused on providing all basic characteristic in wide temperature range. The room temperature test follows a routine procedure similar to measurements of classical differential amplifiers (*e.g.* operational amplifier). Characteristics to be measured on both types of amplifiers are:

- **DC transfer V_{in}/V_{out} characteristic** (4.2 K to 400 K);
- **Voltage gain as the function of temperature** (4.2 K to 400 K);
- **Dispersion of the voltage gain for several amplifiers** (room temperature T = 296 K);
- **Variation of the voltage gain versus V_{DD} and I_B bias** (T = 296 K);
- **Large signal common-mode amplification** (T = 296 K) ;
- **AC response** (T = 77 K and 296 K);
- **Input-referred noise spectral density** (T = 77 K and 296 K).

tel-00417838, version 1 - 17 Sep 2009

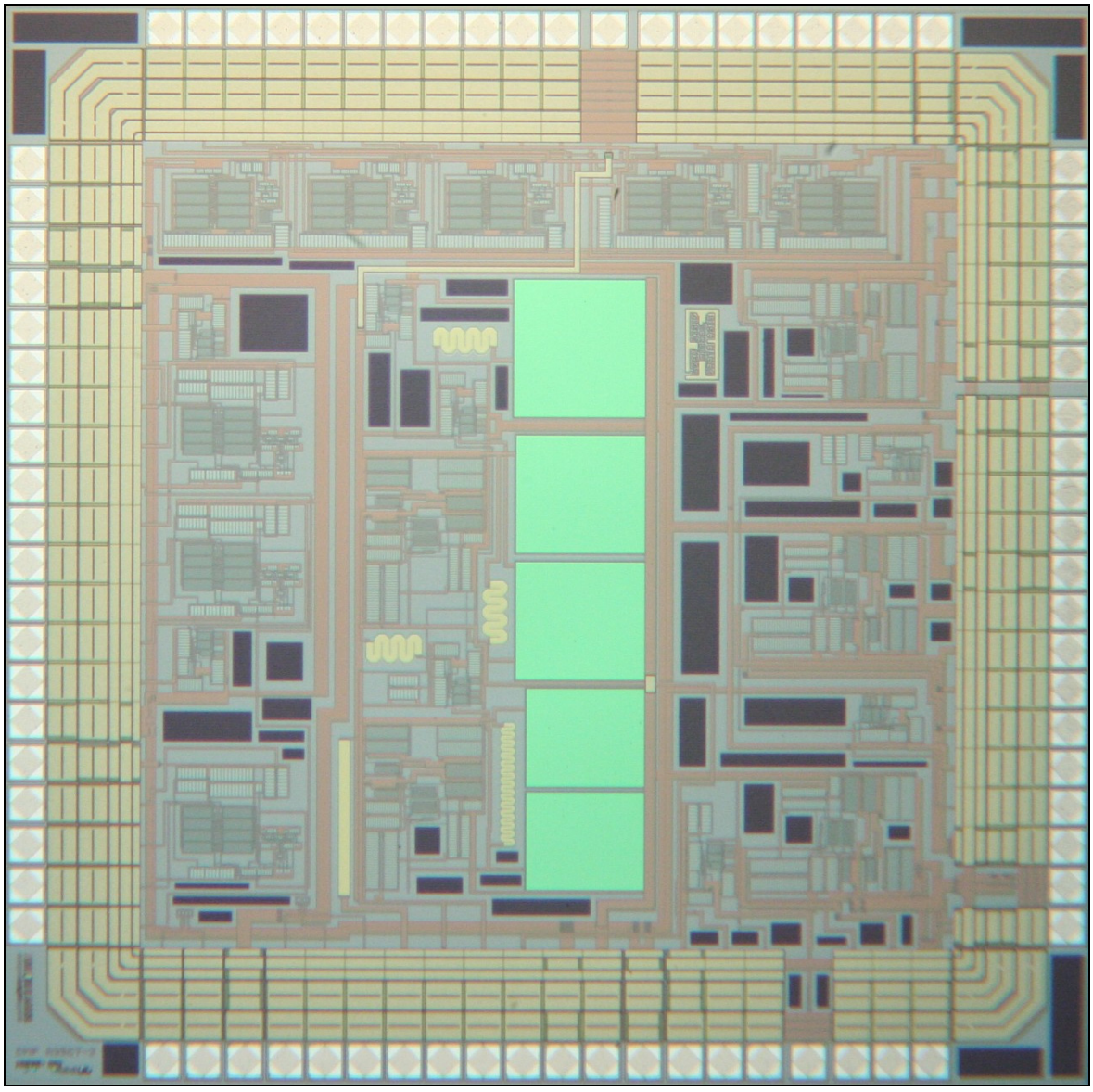


FIG. 7.4: *Microphotography of fabricated chip on 3×3 mm ^{2} surface*

7.2.1 Test Facility

The tests of the amplifiers were performed in the department on Nanoscience and Cryogenic of the "Commissariat à l'Energie Atomique" situated in Grenoble, and in L2E, laboratory of Paris 6 University. In the test, we utilized very high accuracy equipments, such as the Keithley nanovoltmeter (model 2182), femto-amper current generator (model 2240), vector analyzer Agilent/ Hewlett-Packard etc. The using of the high-performance instruments together with optimized testing circuit is essential and allows us to presents very high accuracy results.

During the testing, the principal objective was to verify the basic amplifier function and particularly the accordance with the parameters being originally intended by the design. To provide a correct testing, we strive to operate the circuit in ideal conditions. This is why we have developed a testing PCB card *Fig. 7.6*, including circuits as regulated low noise symmetrical power supply, adjustable bias current sources, input/output high frequency unity voltage buffers, and other test components. Another purpose of this card was to facilitate the measurements by providing a simple and reconfigurable support, allowing access to all integrated blocks in the ASIC.

tel-00417838, version 1 - 17 Sep 2009

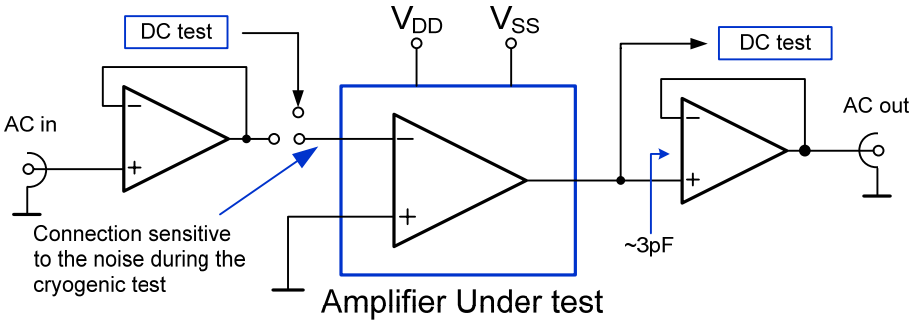


FIG. 7.5: *Different configuration used for AC and DC testing of amplifiers*

The set-up shown in *Fig. 7.5* is a simple way allowing operating the amplifiers in almost ideal conditions and thus avoiding all effects susceptible to perturb the measurements. In this figure, the input/output of the amplifier under test are buffered by high frequency unity gain voltage buffers realized by AD 8045 operational amplifiers. These buffers ensure high driving capability and low input capacitance at the output. The buffers are bypassed for the DC tests, in order to avoid potential offset introduced by the OAs.

Obviously, the developed PCB card *Fig. 7.6* is intended only to provide tests at room temperature. To provide cryogenic tests, a simple support, allowing the connections of vital signals to the *Fig. 7.6* PCB was developed. The cryogenic measurements were done within a wide temperature range (4.2 K to 390 K), where the integrated circuit was placed in the regulated vacuum calorimeter, immersed in liquid helium (T = 4.2K) or in He vapour. However, the conditions were not ideal (*e.g.* we used long wires) and some measurements were influenced by parasitic signals (particularly the noise measurements at T = 77 K), as shown in *Fig. 7.5*. As we show later, the measurements comparing the room temperature (~ideal) and cryogenic characterization show, a good accordance.

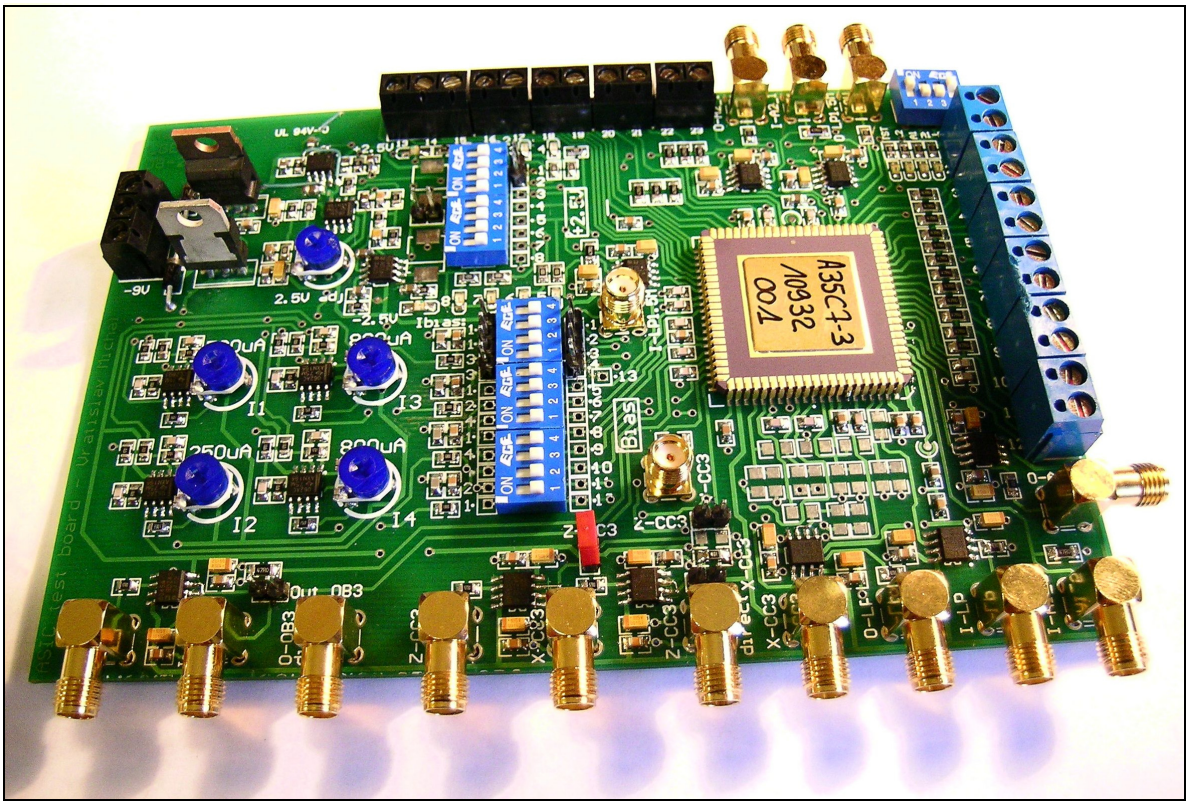


FIG. 7.6: *Testing board for room temperature test*

tel-00417838, version 1 - 17 Sep 2009

In order to eliminate the noise in the power supply lines, the amplifiers are supplied by symmetrical regulated power supply equipped by the low-pass frequency filters with the cut-off frequency in order of several hertz, *Fig. 7.7*. These low pas filters (see *Fig. 9.2* and *Fig. 9.3* for details) was realised with high driving capability low-noise amplifiers. In the following, the chip soldered on *Fig. 7.5* test card is named as *Chip 1* and the ASIC mounted on the cryostat support as *Chip 2*.

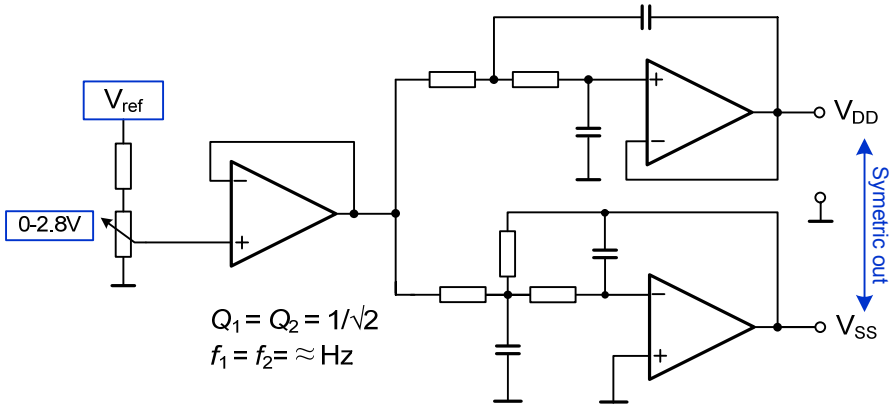


FIG. 7.7: *Symmetrical regulated power supply with low-pas frequency filters reducing the noise level in the power lines*

7.3 Type I Geometry-Fixed Gain Amplifier

7.3.1 DC characteristics (room temperature)

Our first comment concern the measured DC transfer characteristics, *Fig. 7.6* (provided by the of the reference amplifier, further labelled A5) and their comparison with the simulated results. The voltage gain was extracted as the derive of the characteristics around the zero input voltage:

$$G_0 = 39.84\ \text{dB}_{@296\text{K.}}$$

This result demonstrates that the main objective of our design, *i.e. high accuracy of the voltage gain has been reached*. The characteristics fit well with simulated results. The high accuracy was confirmed by measurements of all five *Type I* amplifiers. We can find the gain to be in the targeted range (the reference amplifier on chip 2 is labelled A5_2):

TAB: 7.1: *VOLTAGE GAIN OF MEASURED AMPLIFIERS (A5_2 REFERS TO CHIP 2)*

AMPLIFIER	GAIN [dB]
A_5	**39.84**
A_{5_2}	39.75
A_1	40.10
A_2	39.62
A_3	39.52
A_4	39.85
AVG	39.78

tel-00417838, version 1 - 17 Sep 2009

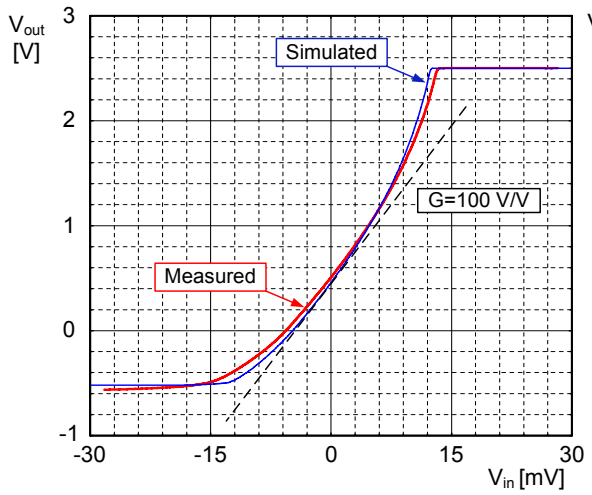


FIG. 7.8: *DC V_{in}/V_{out} voltage transfer characteristic compared with simulation on BSIM 3 model*

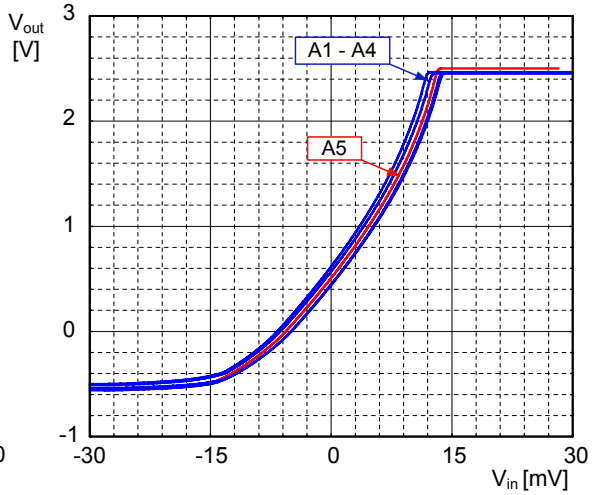


FIG. 7.9: *DC V_{in}/V_{out} voltage transfer characteristic for all five amplifiers.*

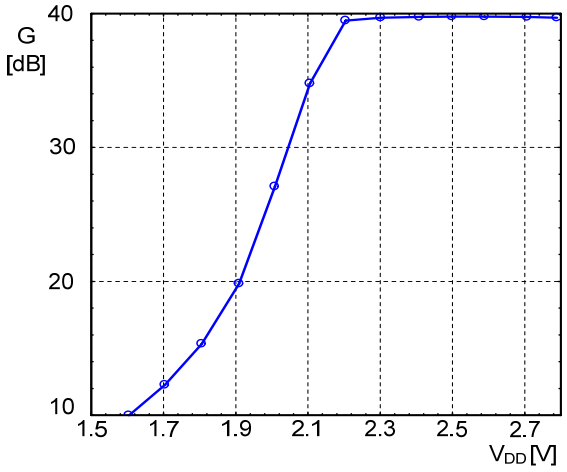


FIG. 7.10: *Voltage gain for various V_{DD} voltages*

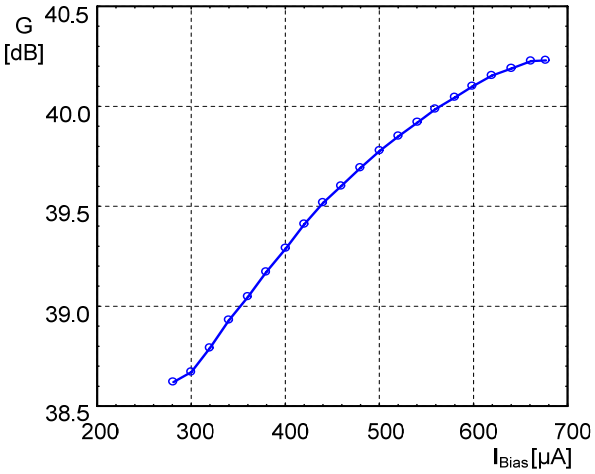


FIG. 7.11: *Voltage gain as a function of bias current. V_{DD}=5V*

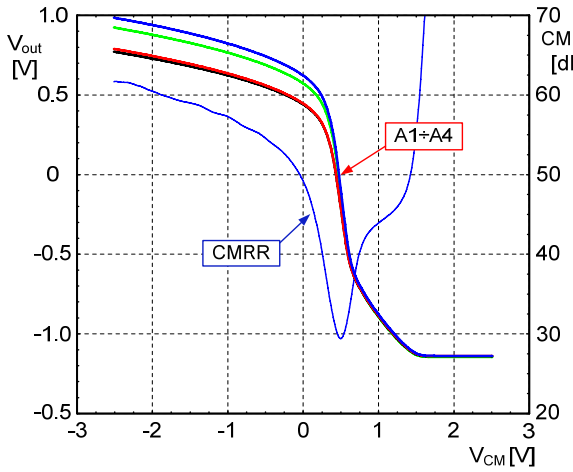


FIG. 7.12: *Common mode amplification and CMRR*

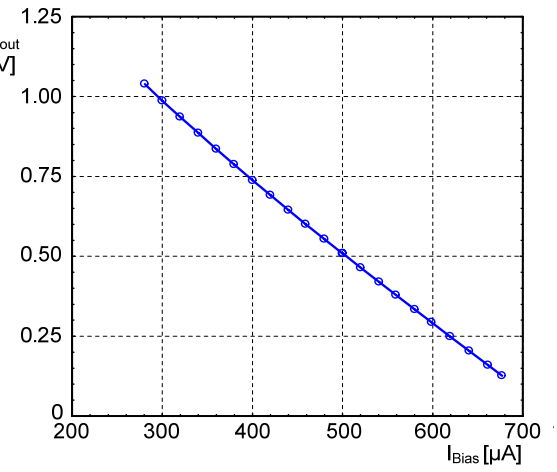


FIG. 7.13: *DC output voltage for various I_{Bias}*

tel-00417838, version 1 - 17 Sep 2009

The *table 7.1* shows very good matching of the amplifiers parameters. However, *Fig. 7.7* shows that the DC offset varies from one amplifier to the other. This was considered in the 5th chapter where the DC operating point was described as a function of absolute parameters, such as V_{TH} or *KP* (*sub-section 5.5.1*). This is accentuated by the fact, that the bias transistor M_{B1} is shared between A_1-A_4 which causes less advantageous matching of A1-A5 amplifiers (*i.e.* current I_L varies). This is why the amplifier A_5 was integrated as the *reference amplifier*, containing its own M_{B1} transistor. On this account, this amplifier exhibits the best agreement with simulated results.

Fig. 7.10 and *Fig 7.10* show the dependence between the voltage gain and the DC bias (voltage V_{DD} and bias current I_B). Here, a very good stability of the voltage gain can be observed (0.05 dB variation between 2.3 - 2.8 V).

An important characteristic is shown in *Fig. 7.12*, where the V_{out} has been plotted as function of the input common mode voltage. This shows the dynamic range limited by approx. +0.4 V. The common mode voltage can thus be as high as ± 1 V, when referring the input signal to -1 V, for example. The characteristic shows also the DC CMRR as the function of common mode voltage, reaching ~50 dB, which is a good value (note that CMRR of conventional OpAmps, usually reaches higher values due to their inherently higher gain).

7.3.2 AC Performances of the 1st Amplifier (room temperature)

The AC performances concern primarily the amplifier bandwidth and input referred noise. These tests were realised with a low capacitive load, approximately 5 pF (Fig. 7.5 configuration).

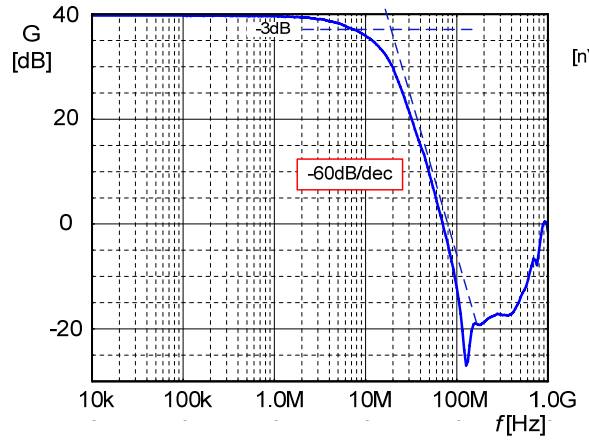


FIG. 7.14: *Amplifier frequency response (A5)*

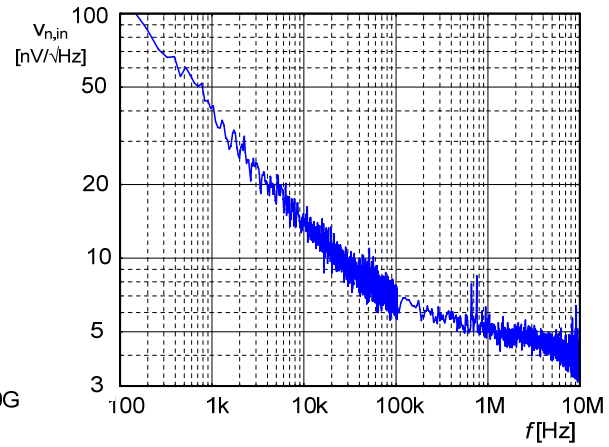


FIG. 7.15: *Input-referred noise spectral density*

The AC characteristic *Fig. 7.14* was measured with input power -40 dBm @ 50 Ω. The resulting bandwidth is 10MHz. This is a very important result allowing to justify the advantages of the *feedback free architecture*: such a cut-off frequency has been achieved with only 2 mA of supply current. In terms of classical operational amplifier design, this corresponds to 1 GHz of gain-bandwidth product (GBW) for unity gain stable OA (see *chapter 4*). Such parameters of OA (high GBW and low quiescence current) are difficult to achieve even with bipolar technology.

Above the cut-off frequency, the AC characteristic exhibits a slope of -60 dB/dec, whereas the simulated characteristic shown in *Fig. 5.20* shows a slope of -40dB/dec only. As shown in *sub-section 5.7.1*, the supplementary pole is caused by the high output impedance of voltage buffer. The noise voltage has been measured in two frequency ranges: 5 Hz - 100 kHz and 10 kHz - 10 MHz. The

tel-00417838, version 1 - 17 Sep 2009

corner frequency is around 100 kHz having a noise floor (white noise) of approx. 5.5 nV/√Hz. Such noise level is also a very good result, when compared to conventional CMOS amplifiers.

7.3.3 Wide Temperature Range Measurements

The wide temperature range measurements have been provided with the 2nd integrated chip mounted on a support, designed to be placed inside the cryostat. We have performed the detailed measurements of DC transfer characteristics within the temperature range from 400 K down to liquid helium (4.2 K). This measurement allows to explore the basic amplifier characteristics, namely the temperature variation of the voltage gain.

Several representative DC characteristics are shown in *Fig. 7.14*. Here, we can see that the amplifier operates down to T ≈ 23 K, where it approaches saturation causing abrupt decrease of the gain.

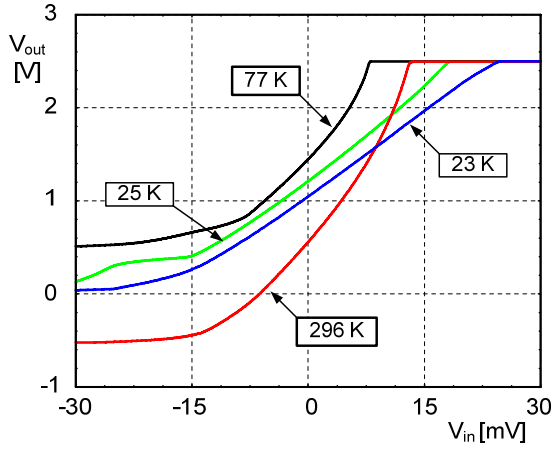


FIG. 7.16: *DC characteristic for various temperatures*

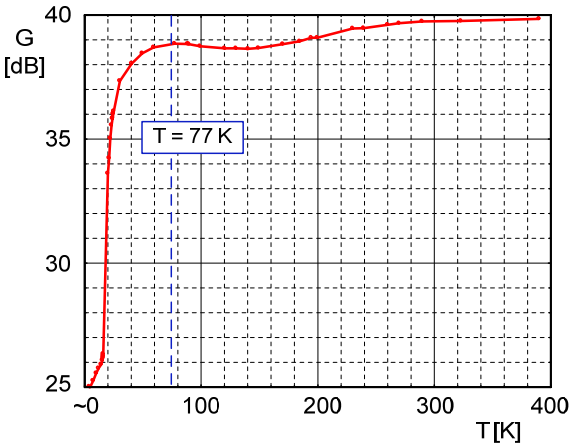


FIG. 7.17: *Temperature function of voltage gain*

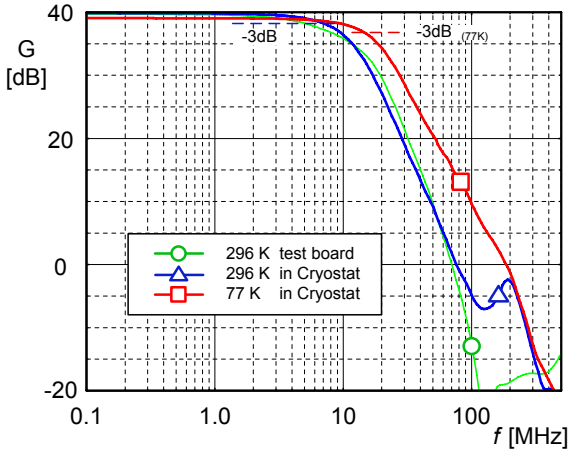


FIG. 7.18: *Frequency response for Chip 1 and 2 for room temperature and Chip 2 for T = 77 K*

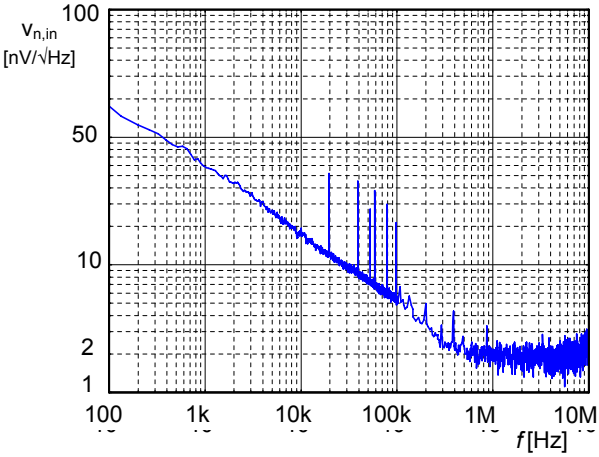


FIG. 7.19: *Input-referred noise for T = 77 K. The peaks reflect the environmental noise*

The temperature characteristic for the voltage gain flattens out around room temperature and cryogenic temperatures. The difference between both areas is about 1 dB. The curve (*Fig. 7.16*) is a universal (calibration) curve, verified by various measurements on two samples of integrated amplifiers. *This characteristic shows that the amplifiers comply with the requirement and can be used for both, room -*

tel-00417838, version 1 - 17 Sep 2009

and cryogenic temperatures. The power consumption remains almost constant for all temperatures (≈ 2 mA).

Fig. 7.18 shows three frequency characteristics: the characteristic shown in *Fig. 7.14* (chip 1 at T = 290 K) and the characteristic measured with the cryostat support at room and cryogenic temperatures.

The AC characteristic at T = 77 K shows an increase of the bandwidth from 10MHz to 17MHz. This effect has been explained in the 6th chapter, where the dominant pole is shifted to $\approx (g_{mL(77K)}/C)$. This is due to increasing transconductance at lower temperatures. On the contrary, the noise measurements at 77 K have been influenced by non-ideal connections which would allow parasitic signals to interfere with the useful signals (see *Fig. 7.5*). However, the noise floor can be extrapolated from characteristic *Fig. 7.19* to be as low as 2 nV/√Hz.

7.4 Type II Temperature-Compensated Linear Amplifier

The measurement of DC Characteristics (performed in the same conditions as *Type I* amplifier measurements), aims to demonstrate the large signal linearity and temperature compensation of the voltage gain.

The first characteristic shown in *Fig. 7.20* is the DC transfer V_{in}/V_{out}, measured on the integrated amplifier without *output buffer* (labelled as A_3 in this paragraph). This figure also compares the simulated characteristic obtained with SPICE level-7 model. *Here, we can see that the characteristic is linear for a wide input voltage range with constant voltage gain being close to 40 dB.*

This DC transfer characteristic allows to extract the voltage gain as the derive dV_{out}/dV_{in}. This voltage gain is 39.3 dB for a supply voltage V_{DD} = 5V. Such accuracy is achieved thanks to the accuracy of the technological parameters (KP,V_{TH}) and design exhibiting the low sensitivity functions of the voltage gain (*Tab. 5.5*). *Tab. 7.2* shows *a very good reproducibility* of this voltage gain even between two different chips of the integrated amplifier.

TAB: 7.2: *MEASURED GAIN FOR THREE FABRICATED TEMPERATURE-COMPENSATED AMPLIFIERS AT T = 296 K, (A_3 – REFERENCE AMPLIFIER WITHOUT OUTPUT BUFFER)*

AMPLIFIER	GAIN [dB]
$A_{\_3}$	**39.3**
A_1	39.29
A_{3_2}	39.26

As shown in *sub-section 5.6.4*, amplifier properties can be controlled *via* the supply voltage V_{DD} and the bias current I_B. Accordingly, an increase of the voltage gain caused by decreasing V_{DD} voltage can be observed, in conformity with *Eq. (5-64)*. The voltage gain as a function of bias (V_{DD} and I_B) has been plotted thanks to various measurements and is shown in *Fig. 7.22* and *Fig. 7.23*.

The characteristics of *Fig. 7.20* to *Fig. 7.23* were obtained by measurements on the amplifier A_3 having no integrated output buffer (*Fig. 5.28*). This would avoid an eventual distortion and DC offset caused by the output buffer. The characteristics of the amplifier with voltage buffer are shown in *Fig. 7.24* and *Fig. 7.25*, for several load resistances. In these characteristics we can notice: *1*) the relatively low driving capability of the output buffer, *2*) a distortion appearing close to the negative V_{DD} (corresponding to simulation *Fig. 5.29*), and *3*) very good linearity of the voltage buffer. The low driving capability is caused by the quiescence current of M_{o1} and M_{o2}, which has been designed very low, in order to reduce the power dissipation. In *chapter 10*, the realisation of an CCII- based on architecture identical with employed voltage buffer will be presented, reaching +/- 20mA of output current.

tel-00417838, version 1 - 17 Sep 2009

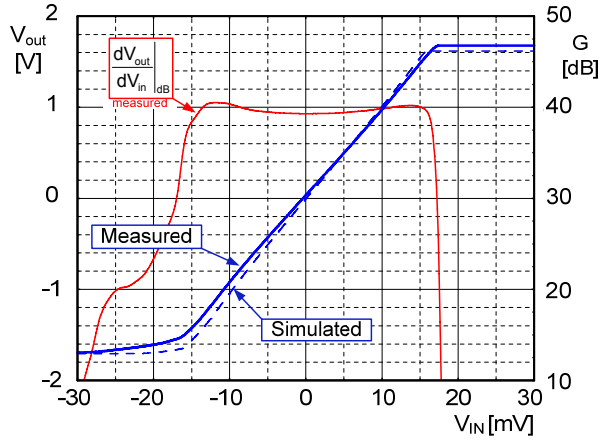


FIG. 7.20: *DC V_{in}/V_{out} characteristic of type II amplifier with no output buffer (A2_3)*

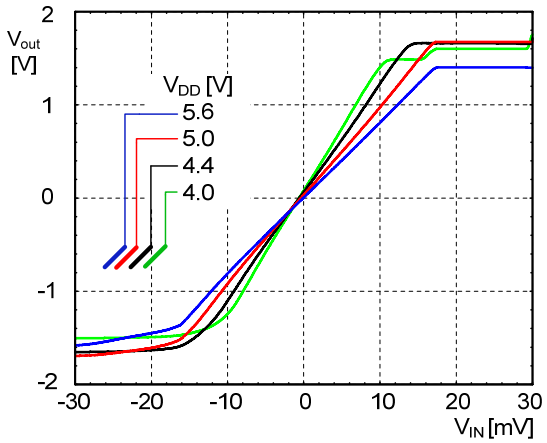


FIG. 7.21: *DC V_{in}/V_{out} characteristic of A2_3 for various V_{DD} voltages.*

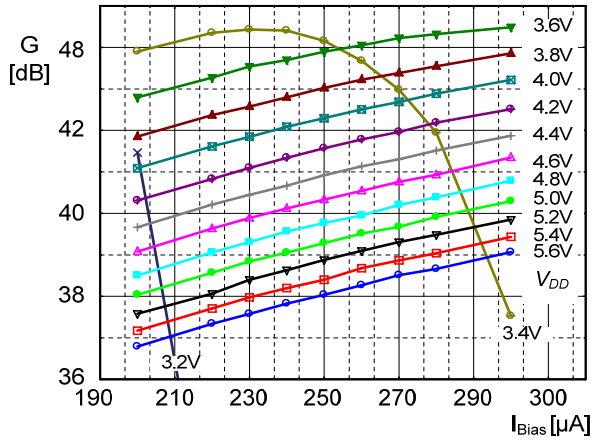


FIG. 7.22: *Voltage gain as function of I_B and V_{DD}.*

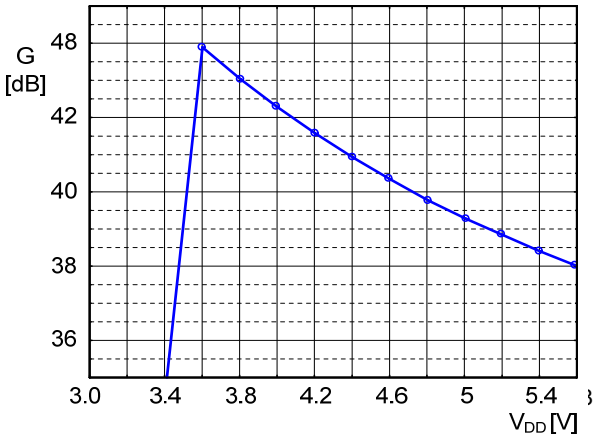


FIG. 7.23: *Voltage gain as a function of V_{DD}.*

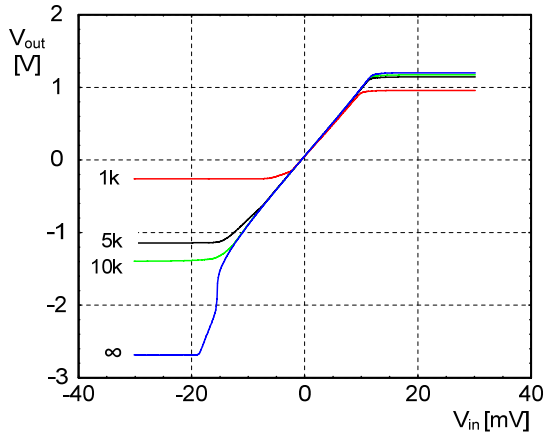


FIG. 7.24: *DC V_{in}/V_{out} characteristic of amplifier with integrated output buffer for various load resistances*

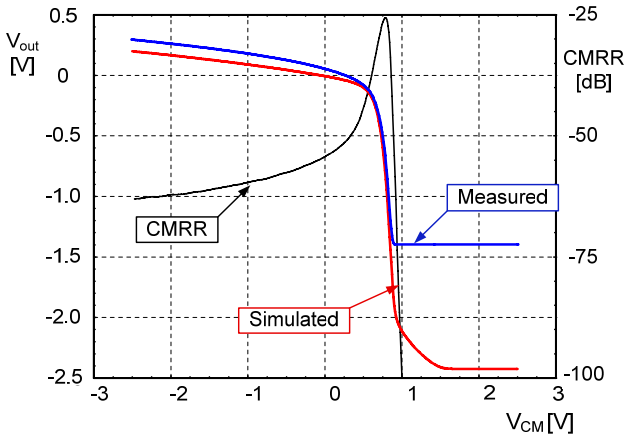


FIG. 7.25: *Common mode gain of amplifier with integrated OB, loaded by 10KΩ resistance*

tel-00417838, version 1 - 17 Sep 2009

7.4.2 AC Performances of 2nd Amplifier (room temperature)

The frequency response of the *Type II* amplifier was measured for various V_{DD} voltages: 5 V, 4.2 V, and 4 V, in order to demonstrate *equation* (5-64). Measured characteristics are plotted in *Fig. 7.26*, where the dominant pole is located approximately at $f = 4$ MHz, followed by a triple pole at $f = 20$ MHz. This triple pole is caused by the amplifier load capacitance and frequency characteristic of the output buffer. The measured white noise is comparable to the previous *type I* amplifier, whereas the corner frequency slightly decreases (*Fig. 7.27, Fig. 7.15*).

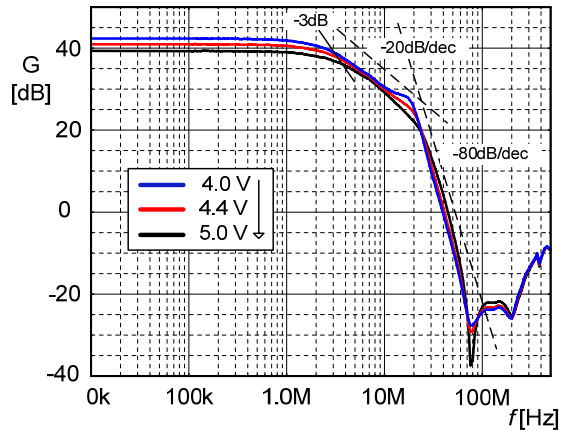


FIG. 7.26: *AC response plotted for various V_{DD} voltages*

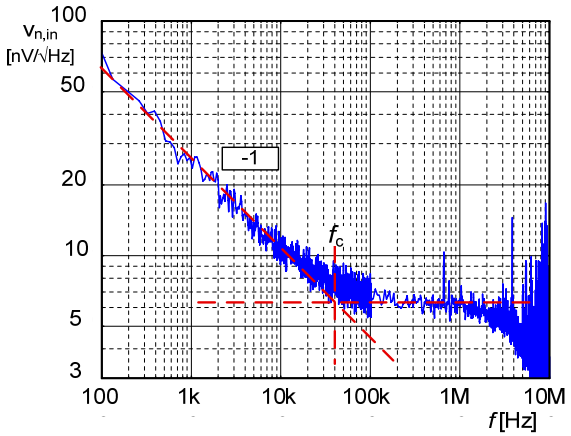


FIG. 7.27: *Input-referred noise voltage spectral density*

7.4.3 Cryogenic measurements of Type II amplifier

The cryogenic measurements confirm the good, wide linear DC operation of the integrated *type II* amplifier down to 40 K. As explained in *chapter 5*, the gain temperature characteristic $G_0(T)$ *can be controlled via the voltage* V_{DD}. The fact that *Eq.*(5-66) depends on V_{DD} provides an interesting way to control and balance the thermal $G_0(T)$ characteristic. Indeed, the gain computed from *Eq.*(5-66) exhibits a better flatness in the 270 to 380 K range for $V_{DD} = 5$ V (*Fig. 7.28*) than for $V_{DD} = 4$ V (*Fig. 7.28*). However, the global performances of the circuit in the 77 K to 380 K temperature range are better at $V_{DD} = 4.4$ V (0.9 dB gain variation within the whole 390 to 77 K temperature range as compared to 2.2 dB gain error at $V_{DD} = 4.4$ V).

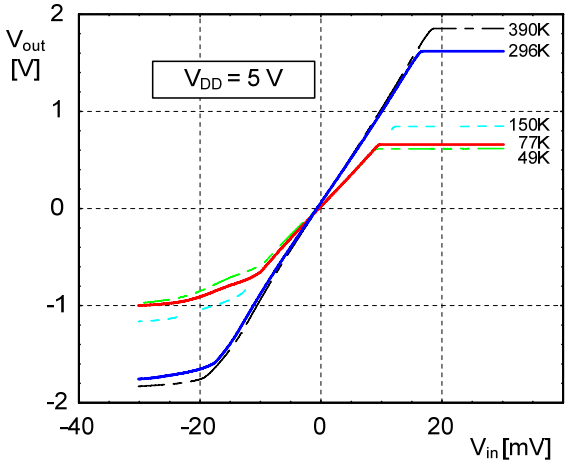


FIG. 7.28: *DC V_{in}/V_{out} characteristic for various temperatures at $V_{DD} = 5$ V.*

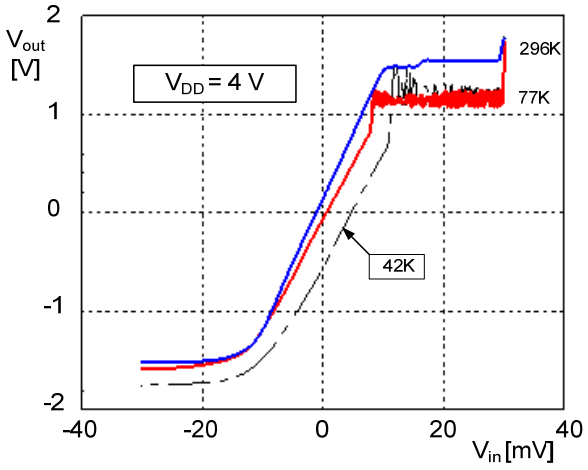


FIG. 7.29: *DC V_{in}/V_{out} characteristic for various temperatures at $V_{DD} = 4$ V.*

tel-00417838, version 1 - 17 Sep 2009

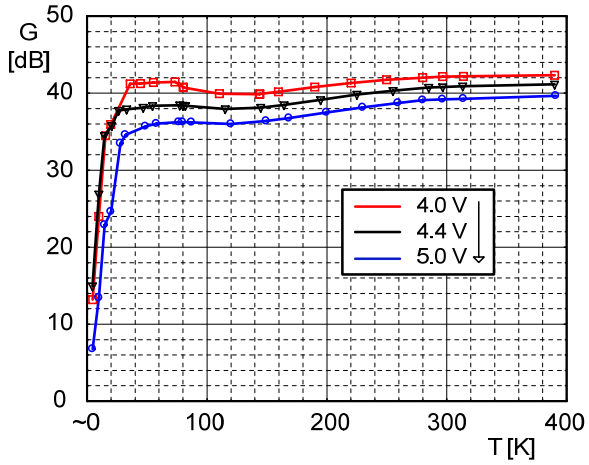


FIG. 7.30: *Temperature functions of the voltage gain for three V_{DD} voltages.*

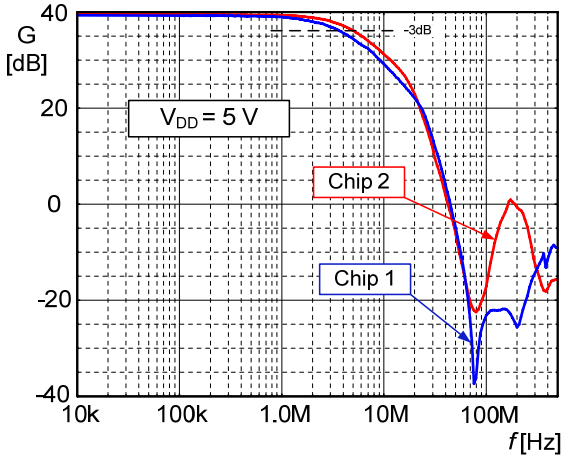


FIG. 7.31: *Matching between Chip 1 (Fig. 7.5) and cryostat mounted Chip 2*

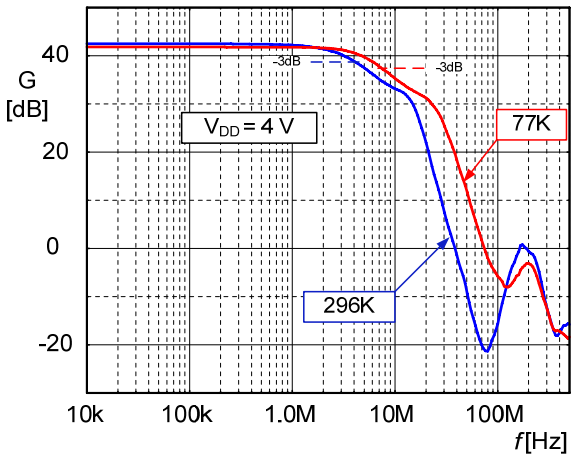


FIG. 7.32: *AC response at V_{DD} = 4 V*

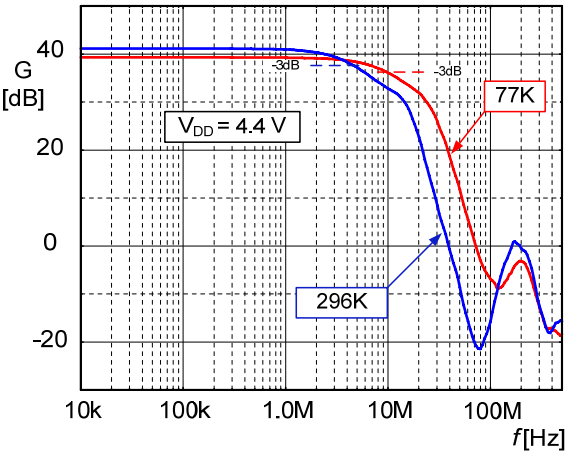


FIG. 7.33: *AC response at V_{DD} = 4.4 V*

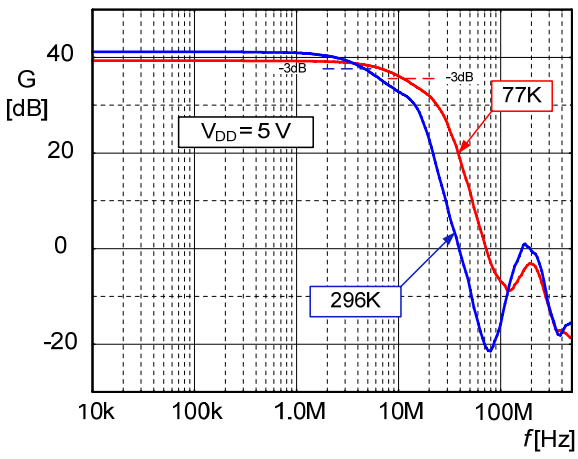


FIG. 7.34: *AC response at V_{DD}=5 V*

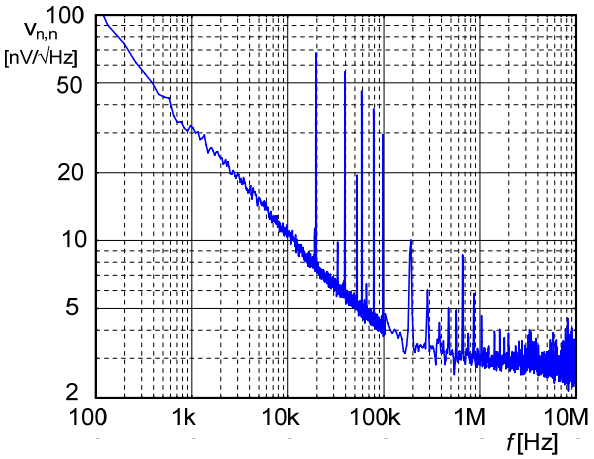


FIG. 7.35: *Input referenced noise voltage spectral density at T = 77 K*

tel-00417838, version 1 - 17 Sep 2009

This was also confirmed by the AC measurements, where the voltage gain in the 4.2 K to 390 K temperature range (*Fig. 7.30*), exhibits also the agreement with *Eq.*(5-66), namely around 300 K and 77 K, where the parameters x and α_{TH} were experimentally determined (*Section 5.1*). For V_{DD} = 5V, the measured gain remains constant around room and cryogenic temperatures (dashed lines in *Fig. 7.28* and *Fig. 7.29*).

The characteristic from Fig. 7.28 demonstrate the principle of voltage gain temperature compensation, using the hybrid voltage vs. current biasing, allowing the control of $G_0(T)$ via the V_{DD} voltage.

However, some deviation from *Eq.*(5-66) could be noticed around T = 100 K, where the characteristic reaches a local extremum. This deformation is quite similar to effect in *Fig. 7.17,* although the gain is fixed here by rather different principle. This can be attributed to two following effects:

i) the increase of the steady state current of M_2 in the low transconductance composite transistor,

ii) and (more probably) simplification in (5-1), where parameters x and α_{TH} have been considered constant through the whole temperature range [81]

In order to properly validate the $G_0(T,V_{DD})$, the measurements were provided on two different amplifiers (on chip 2). The AC characteristic (for V_{DD} = 4 V, 4.4 V and 5 V), measured at room temperature and at 77 K also proves the principle of temperature compensation used in the *type II* differential amplifier – chip 2. In fact, the good accuracy of G_0 at T = 77 K and T = 290 K is evident, as the coefficient x was determined from the measurements at 77 K and 296 K. Therefore, further temperature characterisation of AMS 0.35 μm process provided at intermediate temperatures can be done in order to improve the model *Eq.*(5-5) and optimize the temperature characteristic.

The temperature range of the amplifier is limited at T = 40 K by excessive shifts of the operating point (see *Fig. 7.27* dashed line). This dynamic range (and therefore temperature range) can be extended by referencing the signal to a lower voltage (approx. -1 V)

7.5 Summary of Achieved Results

The measurements performed on both integrated amplifiers are in very good agreement with theoretical results and with required parameters. We have achieved in particular:

- **HIGH ACCURACY OF THE GAIN;**
- **WIDE BANDWIDTH OPERATION WITH LOW QUIESCENCE SUPPLY CURRENT;**
- **WIDE TEMPERATURE OPERATING RANGE 40 K TO 400 K;**
- **LOW NOISE INPUT VOLTAGE.**

Even though good performances are evident from the presented characteristic, a weak point appears to be the output voltage buffer. In order to achieve high bandwidth, the output of the amplifiers has to be loaded by very low capacitances. This is due to the high output resistances of the voltage buffers. Moreover:

- in the 1st amplifier design, the large transistor of output buffer (M_O) creates a dominant capacitance in the high impedance node and limits the bandwidth (10MHz measured – 30MHz simulated at T = 290 K);
- in the 2nd type of amplifier, the voltage buffer *Fig. 5.28* exhibits an important increase of power consumption at low temperatures: 1.3 mA with no output buffer (OB) and 3 mA with OB at 290 K, whereas at 77 K the bias current is 11mA@2.5V (or 9mA@2.0V). This was explained in the sub-*section 5.7.2*, as a result of the self-biasing of M_{O1}, M_{O2} (*Fig. 5.28*). We can now summarize the basic properties of both amplifiers in the following table 7.3:

tel-00417838, version 1 - 17 Sep 2009

TAB.7.3: BASIC MEASURED FEATURES OF THE AMPLIFIERS.

MEASURED PARAMETERS	TYPE *I* AMPLIFIER	TYPE *II* AMPLIFIER
Operating supply voltage	4.1 V to 5.5 V	3.6 V to 5.5 V
Quiescent current	2.1 mA	1.3 mA[1]
– 3 dB bandwidth (T = 290 K)	10 MHz **(GBW=1GHZ)**	4 MHz at V_{DD} = 5 V
– 3 dB bandwidth (T = 77 K)	17 MHz **(GBW=1.7GHZ)**	10 MHz at V_{DD} = 5 V
Input noise (T = 290 K)	5 nV/Hz^{½}	5 nV/Hz^{½}
Input noise (T = 77 K)	2 nV/Hz^{½}	3 nV/Hz^{½}
Gain G_0 (T = 290 K)	39.85 dB	39.3 dB at V_{DD} = 5 V
Δ Gain 270 K − 390 K	– 0.12 dB	– 0.5 dB at V_{DD} = 4 V
Gain error (at T = 77 K)	– 1.2 dB	– 1.3 dB at V_{DD} = 4 V
Input offset voltage	-	500 µV
SR (V/µs)	25	100
THD[2] (V_{out} = 0.3 V_{pp})	1 %	0.03 %

[1] the output buffer consumption was not included,
[2]Tot. harm. distortion

7.5.1 Comparison with the State-of-the-Art

The basic features summarized in the previous table can be compared with the technological state-of-the-art, for instance [93]. However, in conformity with the definition of fixed gain amplifier (as provided in *chapter 4, Fig. 4.10*), the comparison can be vague such as this configuration is not commonly employed in practice. Moreover, the required cryogenic operation limits the family of eligible candidates, which can be used for the comparison (see [63], where the cryogenic performances of industrial amplifiers are demonstrated). However, the performances of our feedback-free amplifiers should be compared with the following devices:

TAB 7.4: MAIN FEAUTURES OF SEVERAL DIFFERENTIAL AMPLIFIERS SELECTED FOR COMPARISON [90]

Type	Configuration	GBW [MHz]	SR [µV/s]	V_{DD} [V]	Iq [mA]	Input noise nV/√Hz	Other
AD8045	OA Bipolar[1]	1000	1350	3.3 - 12	19 × 3[2]	3	
LTC6401-20	Fixed gain 20dB+/-0,6dB Bipolar	1300	4500	2,85-3,5	50 × 3	2,1	R_{in}=200Ω
LT1226	OA Bipolar	1000	400	5-36	7 × 3	2,6	25dB stable[2]
OPA699	OA Bipolar	1000	1400	5-12	22,5 × 3	4,1	12dB stable
OPA2354	OA CMOS[1]	250	150	2,7-5,5	7,5 × 3	6,5	
INA2331	Instrumentation[4] CMOS	50	5	2,5-5,5	0,5	46	
INA103	Instrumentation BIPOLAR	80	15	9-25	9	1	

[1] Operational amplifier based on bipolar or CMOS technology,
[2] term×3 represent that three OA have to be used to realise the high impedance differential input
[3] frequency compensated for this gain
[4] Instrumentation amplifier

- **Variable gain amplifiers (VGA)** (e.g. [71], [72], [73]) ;
- **Instrumentation amplifiers** [83];
- **Operational amplifier (OA)** [83].

tel-00417838, version 1 - 17 Sep 2009

As shown in *chapter 4*, to realize an amplifier with bandwidth 10 MHz and gain 40 dB, a 1 GHz GBW product unity stable *OA*, or non compensated OA (with lower GBW), is required. In general, operational amplifiers with such bandwidth are commercially available in bipolar technology, having the quiescent supply current substantially larger than 10mA. Moreover, in order to realize high impedance differential inputs, three (or two) amplifiers are needed (see *Fig. 4.9 b*, this is included in *Tab. 7.4* by term × 3). In addition, the noise properties of bipolar versus CMOS are difficult to compare, as they are targeted to different applications (*i.e.* generally bipolar or JFET technology have lower f_c, but higher current noise). Nevertheless, we selected a representative group of amplifiers in *Tab. 7.4*, for comparison with parameters shown in previous *Tab. 7.3*, summarizing the performances of our CMOS integrated differential fixed gain amplifiers. These tables allows the reader to evaluate our achieved results.

tel-00417838, version 1 - 17 Sep 2009

Conclusion of part III

In this *part III*, we have reported new structures and principles for the design and integration of feedback-free fixed-gain CMOS differential amplifiers. The main objective of the design was to comply with the requirements provided in *part II* (*section 4.6*), where the feedback-free amplifier was defined as optimal with respect to the high frequency bandwidth, low noise & power consumption operations. The feedback-free architecture is also advantageous as they attain very high input impedance. The amplifiers are intended to operate in extreme conditions: in a temperature ranging at least from 77 K to 390 K.

These requirements incited us to design a new structure, called low-g_m composite transistor presented in *sub-section 5.3.4*. This structure allows to simulate an transistor with geometry being difficult to realize with accurate, middle size MOS transistors; this is a feature essentials with regard to the gain accuracy. The low-g_m transistor was consequently utilized in the design of two amplifiers:

- ***Type I*** **amplifier** having the gain fixed by the high accuracy transistor geometric matching,
- ***Type II*** **widely-linear amplifier** based on the temperature compensation of transistor parameters

During the design, we have performed deep analysis, in order to optimize the amplifier parameters, namely the above mentioned gain accuracy, temperature behaviour and noise or frequency bandwidth. Basic analyse and design were reported in *chapter 5,* whereas the deeper analysis was presented in *chapter 6*. During the layout in 0.35 µm CMOS process and presented in the chapter 7, we respected the rules of high accuracy circuit design, what also positively affected the performances of the circuits.

The results obtained by the measurements exhibit very good agreement with required parameters for both, ambient and cryogenic temperatures (down to T = 40 K). In particular, a high bandwidth, low input-referred noise, high gain accuracy and low power consumption was obtained (see details provided in *chapter 7* and summarized in *Tab. 7.3*). These parameters with relatively small final die size (≈ 150 × 200 µm), render the amplifiers interesting as a versatile analog blocks in VLSI design, or as a discrete integrated circuit.

The comparison of performances (with examples of parameters listed in *Tab. 7.4*), shows that the circuits are very competitive with the state-of-the-art, and that they fully comply to required parameters for high performance readout electronics dedicated to the developments of new generations of THz detectors.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

Part IV:

High Performances Active Frequency Filters

Summary

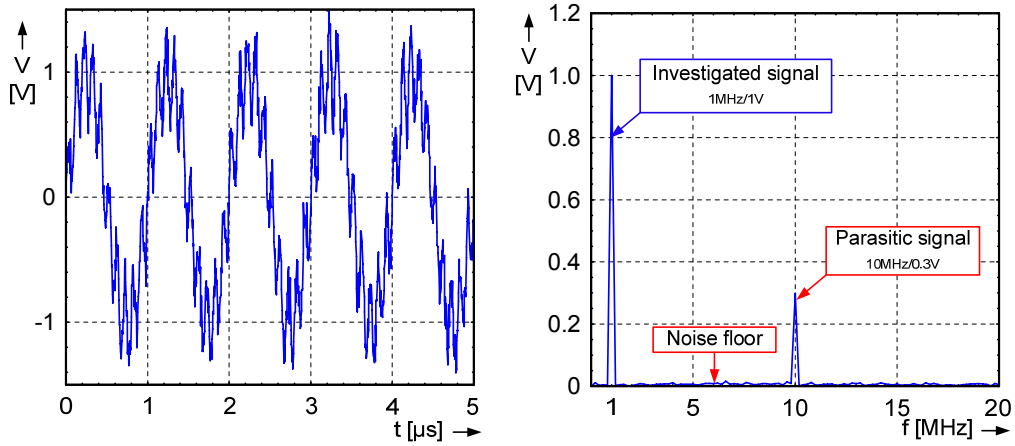
In the fourth section, we introduce the concept of continuous-time frequency filters, allowing an extension of their frequency and dynamic ranges. The objectives of the work are defined in chapter 8.2, followed by an introduction of basic design techniques. Chapter 9 deals with the cascade 2nd order low-pas sections. The causes of the decreased stopband attenuation are explained in order to be avoided in the design of two innovate structures: type II Sallen-Key and current-mode based low pass biquadratic sections. These sections allow a considerable increase of the stopband attenuation and achievable cut-off frequency. In the last chapter, a design of a high performance integrated CMOS current conveyor CCII will be presented. In this design, we primarily wish to reach a very low impedance of the voltage follower at MHz frequencies.

tel-00417838, version 1 - 17 Sep 2009

8 DESIGN OF ACTIVE FREQUENCY FILTERS

8.1 Frequency Filters in the Amplification Chain

Frequency filters are elementary active blocks used in analog signal processing and intended to modify the *spectral distribution of signals*. The filters are characterised by the linear (power, voltage, current) AC transfer function allowing the separation of two or more spectral regions. The example in *Fig. 8.1* shows the waveform obtained from the superposition of an observed signal (1 MHz) in the presence of a spurious signal at the 10 MHz carrier frequency.



a) *b)*

FIG. 8.1: *a) The superposition of two harmonic electrical signals and noise viewed in the time domain b) the spectral (amplitude) representation of the signals*

This case illustrates a common situation encountered in many electrical systems where the frequency filters can be used in order to separate the investigated signal and increase the signal-to-noise ratio (SNR) [94], [95].

The frequency filters split the spectrum into two regions, the *pass-band,* where the signals are unaffected, and the *stop-band*, where the signals are rejected. *Fig. 8.2* shows four basic types of filters.

These four basic filter types are noted as follows: *low-pass* (LP), *high-pass* (HP), *band-pass* (BP) and *bandreject* (BR), which is sometimes referred to as *notch-filter*.

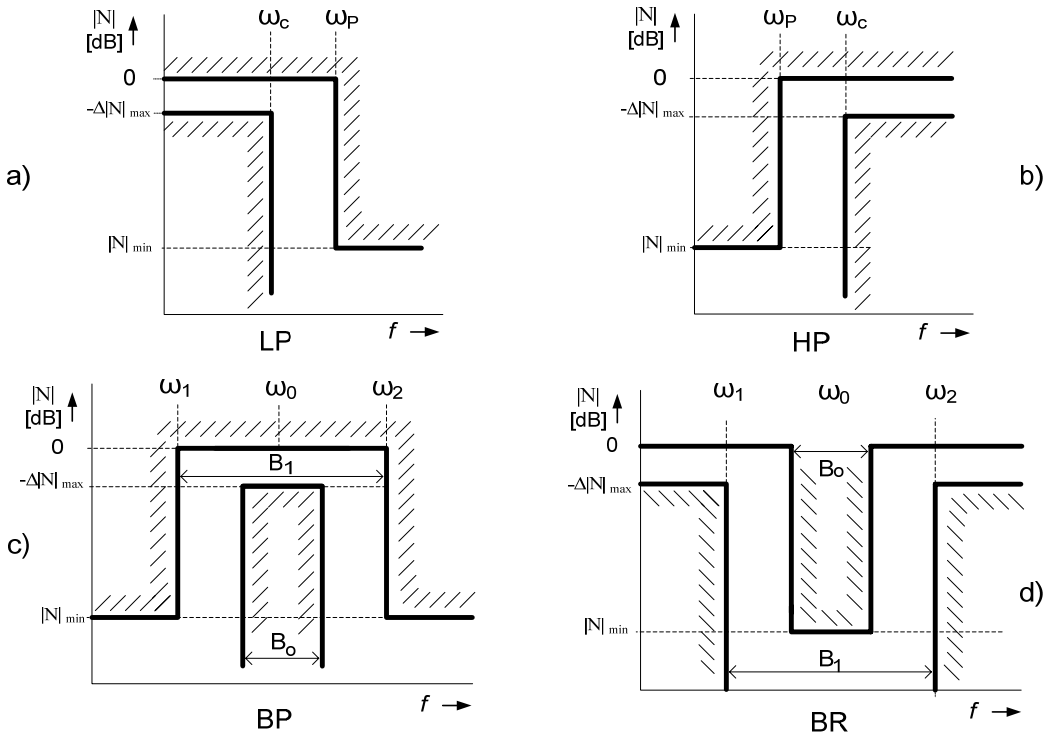


FIG. 8.2: *Different types of transfer functions specifications: a) low-pass, b) high-pass, c) band-pass, d) bandreject filter*

In the process of frequency filter designing, the aim is to realize the transfer function of the filters by means of an electric circuit. The development of such electric circuits represents an important domain of signal processing and has been pursued throughout the history of electronics. We will focus on the area of *continuous time active frequency filters*, where specific methods allowing to improve their high frequency behaviour will be developed.

In the following theoretical introduction, we will briefly introduce two basic principles of the active filters synthesis, namely the active simulation of RLC ladder network and cascade synthesis. As an example of the importance of analog signal processing, a system will be presented of versatile analog frequency filter which has been developed within the framework of the project related to this thesis

8.2 Scope of the Work

The present-day conventional integrated technologies (CMOS, bipolar) facilitate the design of frequency filters within the range of up to MHz frequencies. At present, however, higher frequencies can be reached only by means of the application of special technologies like allied semiconductors. These techniques hamper the high density integration of electronic circuits; therefore, one of the central and currently desirable aims in this respect is to increase the limits of frequency filters built on the classic integrated technologies..

The maximum achievable range of active frequency filters is primarily limited by the frequency at which the behaviour of active elements differs from the function assigned in the initial design. In order to enhance the operational frequency range, the natural approach is often utilized of using higher frequency active devices. Nevertheless, it is also notable that the influences of active elements are

tel-00417838, version 1 - 17 Sep 2009

different for different electrical realisations of filters. The research into these parasitic effects would allow us to define certain rules of design whose application could support further extension of the available frequency range of conventional active frequency filters.

Thus, the investigation of new methods and structures allowing a increase of maximal available cut-off frequency of the standard *cascade active frequency filters* will constitute the focal point of the following sections of this thesis.

The real performances of the biquadratic (2^{nd} order) blocks used for the cascade filter synthesis show generally two kinds of degradation: firstly, there is the aspect of an undesired shift of their cut-off frequency (Ω_n) and quality factor (Q_n), and, secondly, there occurs the appearance of *parasitic zero in the transfer function.* Both of these types are principally caused by the degraded performances of active elements (such as operational amplifier) and they limit the practicable frequency range. In this respect, however, it is necessary to point out that the presence of parasitic zeros limits this frequency range by the *increased transfer in the stop-band area*.

Different techniques of preventing the variation of Ω_n and Q_n have been widely discussed in scientific reports (for example, the issue of providing some compensation by means of the predistortion technique). This type of compensation can be easily performed using conventional design software. However, predistortion can not improve the attenuation in the stop band area, the main reason for this being the fact that the degradation of the active element is usually rather more important and can not be easily compensated for.

In the text sections following the above-described analysis, namely in *chapter 9*, we would like to investigate the origins of the degradation in stop band characteristics for the low-pass biquadratic sections SAB (single amplifier biquad). This investigation will result in analytical explications allowing us to classify the main causes of transfer increase in the considered area. On the basis of these analyses, we will define certain rules which will be further applied in the process of designing two new active structures. The structures are as follows:

i) *The improved low pass Sallen-Key biquadratic section* with increased suppression in the stop-band (labelled as *type II Sallen-Key filter*).

ii) *The current mode low pass biquadratic section* without transmission zeros in the stopband. In the absence of parasitic zeros, all spurious transfers occurring above the cut-off frequency may theoretically be avoided.

These two new active structures may constitute an alternative way in the traditional electronic circuit design, where a considerable extension of the available frequency range can be realised even by means of the conventional low frequency active elements (low cost, low power consumption). These two concepts will be verified by the help of simulation and experimental measurements. As an example, the practical realisation of a 10MHz cut-off frequency filter with high attenuation will be shown.

In *chapter 10,* the *second generation current conveyor CCII-* in a 0.35µm CMOS will be designed in order to experimentally validate the biquadratic section proposed in *chapter 9*. During the process of designing, special attention will be paid to the high frequency performances, mainly to the *low value of voltage buffer output impedance*. The design approach has allowed us to obtain very low impedance of X voltage output port, which was verified by the measurements on the fabricated sample (~2 Ω constant up to MHz frequencies).

tel-00417838, version 1 - 17 Sep 2009

8.3 Design Approaches to Active Frequency Filters

Various technologies may be utilized for the design of frequency filters. For instance, in this respect we can refer to filters based on mechanical resonances [96] (ceramic resonators, Quartz, Surface Wave filters and others), microwave filters based on the simulation of lumped elements network by transmission lines [97],[98] or to the technology which stands in the centre of our interest, namely *frequency filters based on active elements* (active filters). In this case, the scale of realisations is very large and comprises many different techniques. In the following text, a theoretical overview of two most widely applied design techniques will be presented. The two approaches we would like to focus on are:

- **A synthesis based on the simulation of RLC ladder prototype**
- **A cascade synthesis based on the 1st and 2nd order sections**

Before presenting these two techniques, the formalism currently used for the AC description of filters will be presented.

8.3.1 Approximation of Transfer Function

In order to describe the AC behaviour of a frequency filter, we need to express mathematically the AC frequency transfer. In *Fig. 8.*2 we have already seen the ideal (rectangular) plots enclosing the AC transfer characteristic by virtue of parameters like the cut-off frequency ω_c, (ω_0 for BP and BR), band pass ripple $-\Delta|\boldsymbol{N}|_{max}$, and attenuation $|\boldsymbol{N}|_{min}$. The approximations describe the AC transfers in order to satisfy the *Fig. 8.2* plots. In linear electric circuits, we describe the AC transfer by the rational function $\boldsymbol{N}$(s) of the complex variable $j\omega$ or the Laplace operator "s":

$$\boldsymbol{N}(s) = \frac{\boldsymbol{B}(s)}{\boldsymbol{A}(s)} = \frac{b_0 + b_1 \cdot s + b_2 \cdot s^2 + ... + b_m \cdot s^m}{a_0 + a_1 \cdot s + a_2 \cdot s^2 + ... + a_n \cdot s^n}, \tag{8-1}$$

where $\boldsymbol{B}$(s) and $\boldsymbol{A}$(s) are the nominator and the denominator of the transfer function. This transfer function can be expressed by the magnitude of transfer (absolute value) and its phase:

$$\left|\boldsymbol{N}\right|_{dB}(\omega) = 20 \cdot \log\left(\frac{\left|\boldsymbol{B}(j\omega)\right|}{\left|\boldsymbol{A}(j\omega)\right|}\right) \quad and \quad \varphi(\omega) = \arg\left(\frac{\boldsymbol{B}(j\omega)}{\boldsymbol{A}(j\omega)}\right), \tag{8-2}$$

which is used in the graphical interpretation called *Bode plot*. The coefficients in *Eq.*(8-1) are determined by an *approximation* of the *ideal transfer characteristic*. The ideal transfer characteristic is a rectangular characteristic with no pass-band, and infinite stop-band attenuation, and net transition between these two areas. The approximation type and order result from the required filter properties, for example passband ripple, phase linearity, or the parameters of *Fig. 8.2* [94],[95].

The *roll-off rate* (sharpness of the transition) is given by order m of the transfer function. For LP and HP filters, the roll-off rate reaches ($20 \cdot m$) dB/decade, whereas BP and BR transfers reach only ($10 \cdot m$) /decade (m/2 zeros are placed in the origin of the complex plane, which results in a reduced roll-off rate). However, for the given order m, different types of approximation show different transition rates in the proximity of the cut-off frequency.

The mathematical solution of approximation is a relatively complex problem which is mostly based on operations using the squared transfer function $|\boldsymbol{N}(j\omega)|^2$ defined as [94]:

$$\left|\boldsymbol{N}(j\varpi)\right|^2 = \boldsymbol{N}(j\varpi) \cdot \boldsymbol{N}(-j\varpi). \tag{8-3}$$

tel-00417838, version 1 - 17 Sep 2009

Its application allows us to avoid operations with complex numbers, which disappear in the squared terms $N(j\omega)$. The amplitude squared transfer function of a 2-port filter network is usually defined as:

$$\left|N(j\varpi)\right|^2 = \frac{1}{1+\varepsilon^2 F_n^2(\Omega)}, \tag{8-4}$$

where ε is the passband ripple constant, F_n is the characteristic function of approximation, and Ω is the frequency variable. In practice, the most frequently used approximations are the maximally flat Butterworth approximations, where $\varepsilon = F_n = 1$, and the *Chebyshev* approximations with equal ripple characteristic, where the constants ε and F_n can be arbitrarily chosen. More details on the approximation techniques can be found in related sources [94],[99]. In the following text we will present the methods allowing us to implement these approximations by means of using the electric circuits

8.3.1 Design of Passive RLC Ladder Filters

The passive RLC network is an important structure in the frequency filter design as it can be easily transformed in other realisations like the active circuit or the microwave planar structure. We use the *normalized LP_n prototype* in the *T* (*Fig. 8.3 a*) or *Π* (*Fig. 8.3 b*) forms. Here, normalisation means that the values of the filter components are designed for the cut-off frequency $\Omega_0 = 1$ *rad/sec* and terminal resistances $r_{n1} = r_{n2} = 1\ \Omega$.. The reactive part (*L - C* network) is generally considered as lossless, which denotes that ideal building components are required. The poles of such network are distributed only on the imaginary axis of the complex plane. In the final circuit, attenuation is obtained by the power dissipation in the *terminal resistances* r_{n1},r_{n2}.

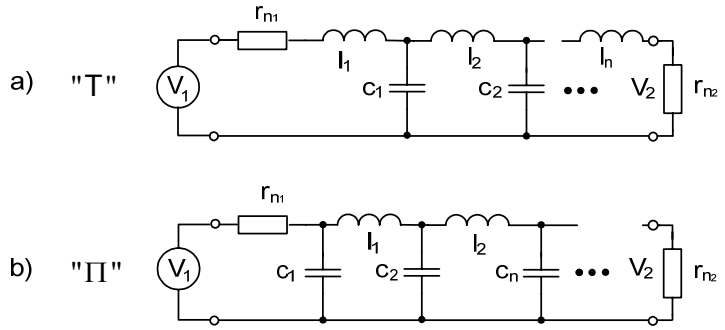


FIG. 8.3: *Normalised prototypes of the LP ladder filter (ω=1 rad/sec, r_n=1 Ω) a) T and b) Π*

The component values of the LP_n prototypes are widely available in catalogues of approximation or, alternatively, can be obtained by means of the design software. The double ended RLC prototypes are generally considered as the best solution to facilitate the obtainment of optimal sensitivities of the transfer function as well as the low spreading of components values [94]. However, in some cases (like the active FNDR structures, whose details are described hereafter) the use of single ended RLC prototypes can be more interesting.

The final form of RLC filter can be obtained from a normalised prototype by means of applying impedance *denormalisation* [94]. This enables us to find the resulting network topology and the component values from the prototype (l_n,c_n,r_n) values for the required Ω_0, R_{n1} and R_{n2}.

Tab. 8.1 shows how this type of transformation can be done. We can see that, for the low-pass prototype (*Fig. 8.3 a,b*), the topology remains unchanged. The high-pass design is obtained by means of permutation of inductors and capacitors. For BP and BR, the branches of the LP_n prototype are replaced by the second order parallel or series resonant LC circuits.

tel-00417838, version 1 - 17 Sep 2009

TAB 8.1: TRANSFORMATION OF THE NORMALISED FIG. 8.3 LP PROTOTYPE INTO THE FINAL CIRCUIT STRUCTURE (K_L, K_C DEFINED BY (8-5))

Prototype:	l	c	Transformations:
LP	L	C	$L_n=l_n \cdot K_L \quad C_n=c_n \cdot K_C$
HP	C	L	$L_n=\frac{K_L}{c_n} \quad C_n=\frac{K_C}{l_n}$
BP	L C	L C	$L_n=l_n \cdot K_L \cdot K_C \quad C_n=\frac{K_C}{l_n \cdot K_L}$
BR	L C	L C	$C_n=c_n \cdot K_L \cdot K_C \quad L_n=\frac{K_C}{c_n \cdot K_L}$

In order to achieve the frequency denormalisation, the new values L_n,C_n, need to be determined. The purpose of such denormalisation is to find the value of new components L and C. Their impedances at Ω_0 must be identical with the l_n,c_n impedances at $\Omega = 1$ multiplied by terminal resistance values (impedance level of the filter). We can define the transformation constant K_L and K_C as:

$$K_L = \frac{R}{2\pi \cdot \Omega} \quad \text{and} \quad K_C = \frac{1}{2\pi R \cdot \Omega}. \tag{8-5}$$

The application of impedance denormalisation is shown in *Tab. 8.1*. As an example we can provide the denormalised networks obtained from the LP_n network (*Fig. 8.3 a*) for all standard transfers in *Fig. 8.4*.

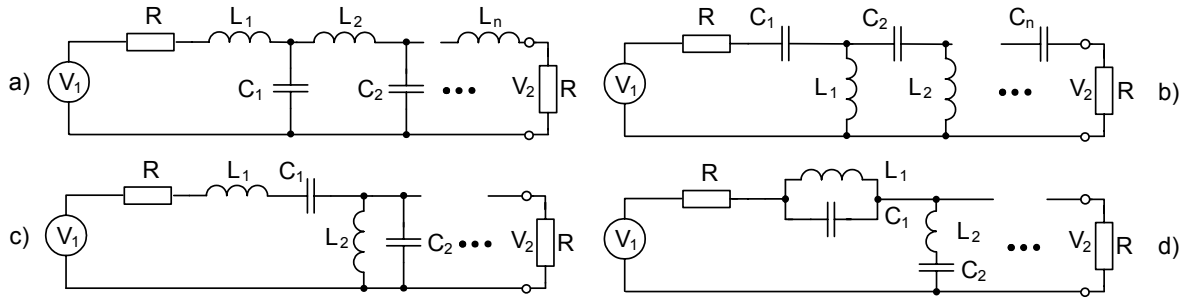


Fig. 8.4: *The transformed RLC "T" type filters for the (a) low-pass, (b) high-pass, (c) band-pass and (d) bandreject filter*

8.3.2 Active Simulation of Passive RLC Filters

The previously presented RLC ladder structure is an interesting way to realize frequency filters within the range of above a few units of MHz. In order to reach lower frequencies, inductors of high values may be required; however, the realization of these inductors constitutes a difficult step. Therefore, alternative solutions based on active elements have been developed and are used in electronics [94],[95],[100]. Several techniques can be utilized for active filters designed from passive RLC prototypes. In this respect, let us point to the following ones:

- **The use of active synthetic inductor**
- **The use of impedance invertors (GIC, gyrator and others)**
- **The transformations of transfer function (for example, the Bruton transformation)**

These methods are well-known as the direct realisation (simulation) of the RLC ladder prototype and will be briefly introduced now.

tel-00417838, version 1 - 17 Sep 2009

i) Active Synthetic Elements (Inductor)

The use of active synthetic elements is important primarily for the replacement (simulation) of the inductances in the RLC ladder (*Fig. 8.4*) networks. However, it is important to note that there can also be created a synthetic capacitor allowing us to reach high values and high Q (interesting for the low frequency area).

The active synthetic elements can be designed in the lossless form or as elements with the finite quality factor Q (the lossy element). Naturally, the accurate simulation of an ideal RLC lossless prototype requires the lossless synthetic elements. We can, nevertheless, point to the techniques utilizing the design based on lossy RLC prototypes, which is interesting mainly thanks to the economical aspect [102],[103],[104],[105].

The simulation of lossless elements has to be done using at least two active devices (amplifiers). Concerning the final circuit, grounded elements are preferably used to reduce the number of amplifiers. The integration of floating synthetic inductors/capacitors usually requires a rather high number of amplifiers, which may increase the complexity of the circuit [107]. It follows from this that the *synthetic inductor is primarily important for the design of the High Pass and the coupled resonator type Band Pass filters*.

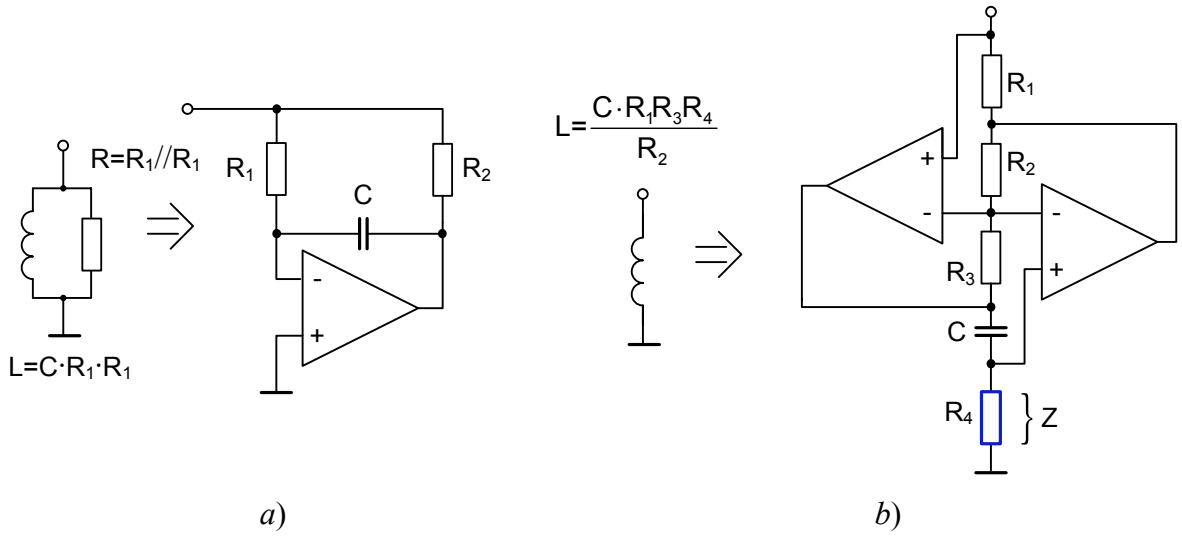


FIG. 8.5: *a) a lossy grounded synthetic inductor b) inductor realised by means of the Antoniou's General Impedance Inverter (GIC). The structure can facilitate the realisation of the synthetic capacitor by permuting the C with R_4, R_3 or R_1*

The example of lossy active grounded inductors is shown in *Fig. 8.5 a)*. Here, the losses are represented by equivalent parallel resistance R. In practice, the quality factor of such circuit is limited by the acceptable dispersion of the component values. The lossy grounded inductor also exists in the serial lossy model [95].

Fig. 8.5 b) shows the implementation of an ideal lossless inductor realized by two (ideal) OA. This design is based on the *Antonius GIC circuit* [107] and features very interesting properties at higher frequencies. The quality factor can reach the values of up to a few hundreds, which is sufficient with respect to the simulation of ideal elements.

ii) General Impedance Converter GIC

tel-00417838, version 1 - 17 Sep 2009

The general impedance converter is a two port network allowing the multiplication or division of impedances by the Laplace operator s [108],[109]. An example of the transformation using a GIC is shown in *Fig. 8.6,* where a resistive loaded GIC on one side behaves as the inductance at port ● side. This inductance arises from the multiplication of *R* by the Laplace operator *s*. The division by the Laplace operator can be performed in the opposite way, namely by connecting the impedance to the ● port. In this case, a capacitor connected at the ● port can be transformed into a new element called the *Frequency Depended Negative Resistor FDNR* [110], which is characterized by the real impedance of $Z_{FDNR}=1/s^2D$. This component is an important block for the synthesis of low-pass and band-pass frequency filters and its utility will be shown later. It can be further noted that an Antoniou GIC structure is similar to the lossless synthetic inductor represented in *Fig. 8.5 b*). This similarity is obvious as the resistance load is transformed into synthetic inductance by means of the division provided by the Laplace operator *s*.

The impedance of the FDNR is purely real and decreases with the frequency. It is commonly represented by the symbol *Fig. 8.6 b)*. In the following chapter, the transformation of the RLC ladder filter into an equivalent FDNR (RCD) network will be shown.

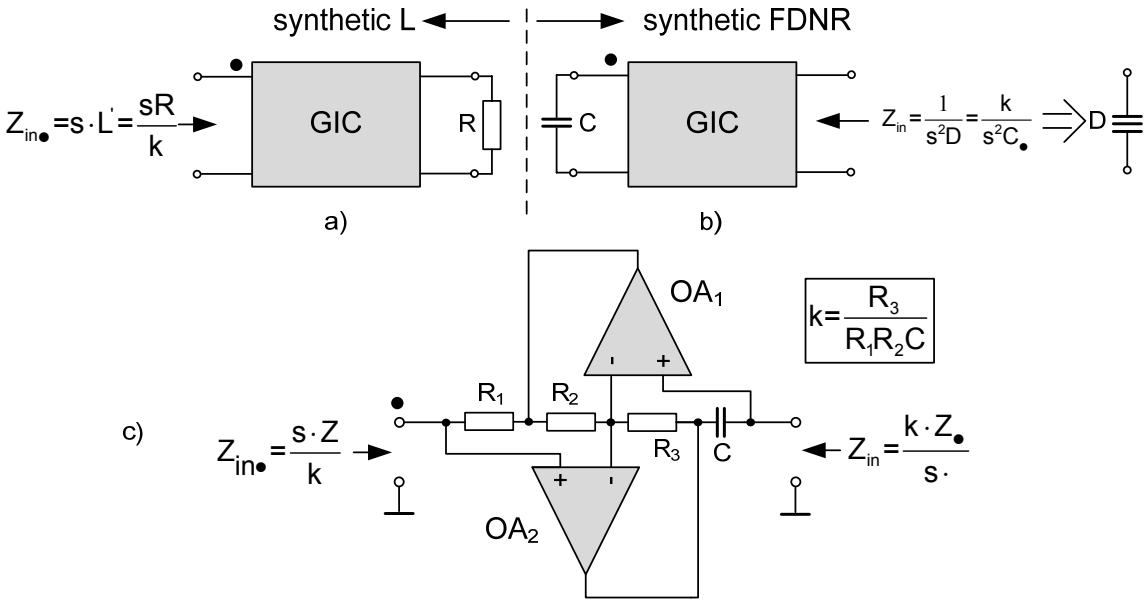


FIG. 8.6: *The general impedance converter simulation of a) a synthetic inductor, b) the Frequency Depended Negative Resistor FDNR and c) its physical implementation by the Antoniou´s network.*

iii) RCD Network

In addition to the transformation provided by the division/multiplication by the help of the Laplace operator *s*, the GIC can perform scaling by means of the dimensionless constant *k*. The transformation where all the circuit impedances are divided by the term *k·s* is called the *Bruton transformation* [110]. This transformation utilizes the fact that the resulting voltage transfer remains unchanged if all impedances of circuits are scaled by an identical term (*k·s*). We can write the immitance of a transformed element in the equivalent circuit:

$$Z'(s)=\frac{Z(s)}{k\cdot s} \quad and \quad Y'(s)=k\cdot Y(s)\cdot s\,, \tag{8-6}$$

The impedance scaling *via* the choice of value *k* is important with respect to the optimal filter impedance level (choice of component values).

tel-00417838, version 1 - 17 Sep 2009

However, the division/multiplication by the Laplace operator modifies the physical essence of elements. For instance, an inductor with impedance $s \cdot L$ divided by the Laplace operator results in an equivalent resistance of value $R' = L/k$. Similarly, a resistor is transformed into a capacitor and the capacitor is transformed into the previously described FDNR. This can be illustrated in the following transformation of the parallel RLC resonant circuit:

$$Y(s) = G + sC + \frac{1}{sL} \longrightarrow Y'(s) = s^2 D + sC' + G'$$

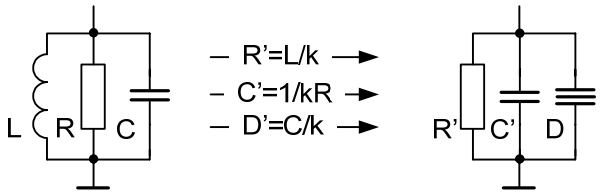


FIG. 8.7: *The application of the Bruton transformation to the parallel RLC circuit*

The transformation shown in *Fig. 8.7* can be applied to the entire *RLC* ladder filter. This is demonstrated on the example in *Fig 8.8*, where a RLC low pass filter (denormalised) is transformed into the equivalent RCD form.

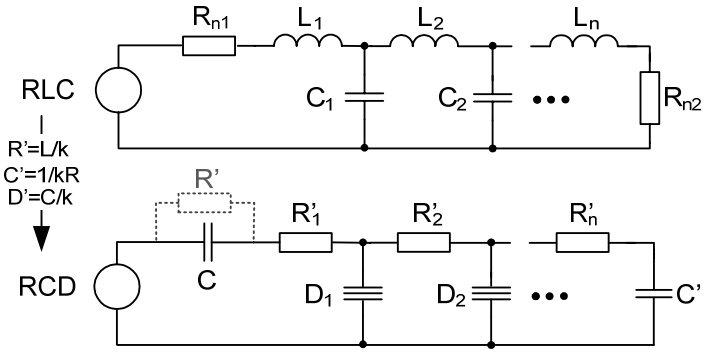


FIG. 8.8: *The transformation applied on the RCL network.*

Here, both RLC and RCD networks show the equivalent voltage transfer function. In the case of a low-pass filter, it is preferable to use the single ended prototype of RLC filter ($R_{n1} = 0$ results in the removal of C ($C \rightarrow \infty$), which is advantageous in relation to DC properties). The FDNR can be realised by the Antonius GIC (*Fig. 8.5*) where impedance Z has to be replaced by the capacitor. The lossy (single OpAmp) FDNR will be presented in *section 9.3.3* and can utilize the direct goal-lossy synthesis technique [104].

8.3.3 Cascade Synthesis of Frequency Filters

Another way to realize active filters is cascade synthesis, where the transfer function (9-1) is split into lower order sections (of the 1st and 2nd order) [94]. These basic sections are realized as independent selective blocks characterized by their specific cut-off frequencies Ω_n and (for the 2nd order block) by the specific quality factors Q_n. In the cascade synthesis, the elementary blocks have to be isolated from each other. This isolation is provided by *zero output impedance of the blocks*.

tel-00417838, version 1 - 17 Sep 2009

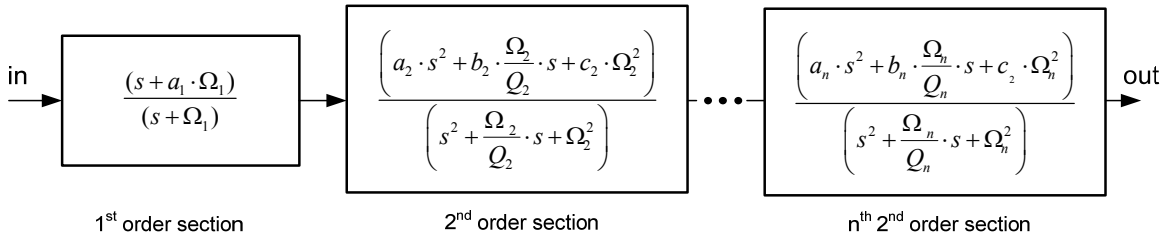


FIG. 8.9: *The cascade realisation of the transfer function. The first block realises the odd order of the transfer function and it is followed by 2nd order blocks*

Fig. 8.9 shows the principle of cascade synthesis. The first block of the 1st order facilitates the obtainment of an odd order of transfer function. The remaining blocks are of the 2nd order. The coefficients (a_n,b_n,c_n and Ω_{0n}, Q_n) can be obtained by the help of the mathematical decomposition of $\boldsymbol{N}(j\omega)$ (8-1) and their values determine the resulting types of filter (LP,HP,BP etc.) (*see section 9.1*).

The electrical design can use various electric circuits to realise the 2nd order biquadratic transfer. The choice of electrical structure is related to the parameters of filters; among these parameters there are, for example, frequency range or quality factor. Thus, for instance, the choice of circuits containing one or several active elements depends primarily on the required value of the Q_n quality factor. The basic configuration and its properties will be discussed in the following chapter.

However, the cascade design is affected by several problems like the rather high sensitivities of the transfer function or high component dispersion as compared with the previously described design approaches based on active simulation of the ladder RLC network.

The synthesis of active filters is, however, the most popular method in the present-day filter design and will constitute our centre of interest in the following chapters. Here, the approaches improving the performances at higher frequencies will be shown.

8.4 Imperfections of Frequency Filters

The practical designing of frequency filters is affected by the errors accumulated during the actual process of designing and electrical integration. These errors result in the difference between the real (measured) and the ideal (designed) AC transfer characteristic.

The first error results from the mathematical approximation of the ideal AC transfer characteristic. This is expressed by the limited roll-off rate and the eventual band pass ripple. The remaining errors are caused by the use of real components (R, L, C, OpAmps etc.) affecting the final characteristic.

The main sources of errors can be divided into the followings classes:

- **Errors due to inaccuracies of component values**
- **Limited components frequency range**
- **Presence of parasitic components**

All the errors affect the final AC frequency characteristic in both passband and stopband areas.

***i*) Errors caused by components inaccuracies.** These errors are linked to the relation between the important parameters (like Ω_n and Q_n) and component values. This relation is examined by the help of *sensitivity analysis*. The relative sensitivity is expressed as percentage shift of the required parameters (X) caused by component dispersion δa_i:

$$S_{a_i}^{X}=\frac{\partial X}{\partial a_i}\cdot\frac{a_i}{X}. \tag{8-7}$$

Naturally, by minimizing this function during the filter synthesis, we can reduce the error caused by component inaccuracies.

tel-00417838, version 1 - 17 Sep 2009

However, sensitivity analysis can not be always performed in the (8-7) analytical form. Whenever the analytical description becomes too complicated (when, for example, it contains many variables or nonlinear models), other statistical tools like the Monte-Carlo analysis can be used. These options are available in the engineering design software.

***ii*) Limited frequency range:** The use of active and passive components is limited by the maximal frequency range. A typical example is an operational amplifier with degraded voltage gain and output resistance at higher frequencies. This degradation reduces the frequency range of conventional frequency filters and its evaluation is of fundamental importance for the achievement of higher practicable frequencies. This problem will be discussed in *chapter 9*.

***iii*) Parasitic behaviour of the elements:** The complex electric models of real components generally include secondary elements like the (parasitic) *R*, *L*, *C*. In some cases, we can encounter nonlinear behaviour. A well-known error caused by parasitic components consists in the losses occurring in inductors and capacitors; for instance, the error limits the quality factor *Q* of the discrete capacitors. This parasitic behaviour has to be analysed during the process of designing by means of the related engineering software.

8.5 Digitally Controlled Analog Filtering System

In many electrical instrumentation systems we encounter the problem of the variation of conditions during the experiment. These variations include the sliding frequency of the examined signal or spurious signals with variable spectral composition. In this case, the use of adaptive filtering system can improve the performance of the electrical test bench. This type of adaptive device (instrument) should allow us to realize all types of filters using basic standard and non-standard approximations. In order to provide maximum flexibility, the parameters are to be controlled digitally (either manually or by an optional computer) [112].

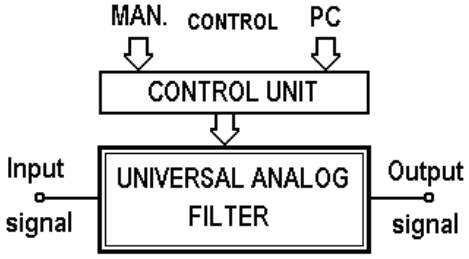


FIG. 8.10: *The block diagram of a digitally controlled analog frequency filter*

This type of system is shown in *Fig. 8.10.* In practice, we can frequently find similar systems using the Digital Signal Processing (DSP). These systems have the typical positive properties of the DSP like high accuracy; however, they are affected by the signal sampling and related problems (for example, quantisation noise and limited dynamic range).

We will describe here an integral system of high performance adaptive analog frequency filter. The development of the device constitutes the actual product of the project related to this thesis [116] and its use is envisaged for the future practical experiences. The aim of the presentation is to show the potentialities of analog signal processing in the domain where the dominance of the DSP can be seen at the present time. As we will see on the following example, the analog (adaptive) system can acquire very interesting properties like the high dynamic range, which is difficult to obtain with the digital signal processing.

8.5.1 Structure of the Universal Analog Frequency Filter

As we can see in *Fig. 8.10,* the concept of the instrument utilizes analog filters whose parameters can be controlled numerically (*i.e.* via the design software or manually via a customer interface).

tel-00417838, version 1 - 17 Sep 2009

In the process of development we were following these main objectives:

- The design of an analog part including analog filters controlled via the A/D convertors. We required the 1 Hz to 120 kHz frequency range, 0.1-50 [-] of quality factor, and very high dynamics range
- The development of a microprocessor control unit ensuring the control of A/D convertors user interface and additional functions
- The development of the related computer software (*Frequency Filter Design Studio*) facilitating access to the filter options

The required versatility of the instrument involves the cascade method of filter synthesis (*Fig. 8.9*). By combining one 1st order filter block and *m* blocks of the 2nd order, it is possible to realise the transfer function ***N***(s) up to the order of *m*+1 (see *section 9.1* for more details on the biquadratic transfer function):

$$N(s) = \frac{\pm B_{(m+1)} s + \Omega_0 C_{(m+1)}}{s + \Omega_{0(m+1)}} \cdot \prod_{i=1}^{m} \frac{A_i s^2 \pm B_i \left(\Omega_{0i}/Q_i\right) s + C_i \cdot \Omega_{0i}^2}{s^2 + s \cdot \left(\Omega_{0i}/Q_i\right) + \Omega_{0i}^2}, \qquad (8\text{-}8)$$

where Ω_{0i} is the angular resonant frequency, Q_i the quality factor, and A_i, $\pm B_i$ and C_i are the relative transfer coefficients. In order to obtain an arbitrary type of filter and approximation (*e.g.* Bessel, Butterworth, Chebyshev, Inverse Chebyshev, Cauer *etc*.), we have to ensure the control of all parameters in the (8-8) transfer function. The architecture of the instrument respecting the philosophy of cascade synthesis is described in *Fig. 8.11*.

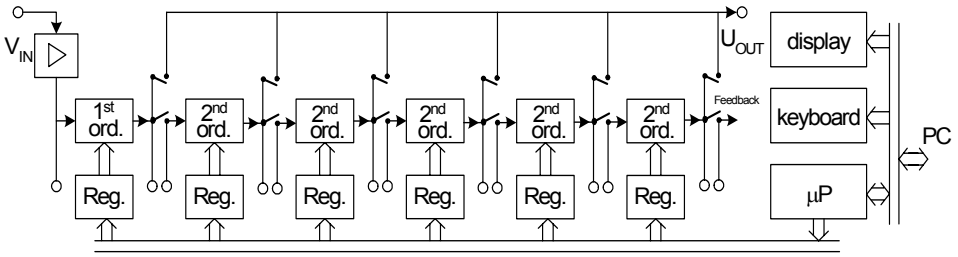


FIG. 8.11: *The architecture of the adaptive frequency filter*

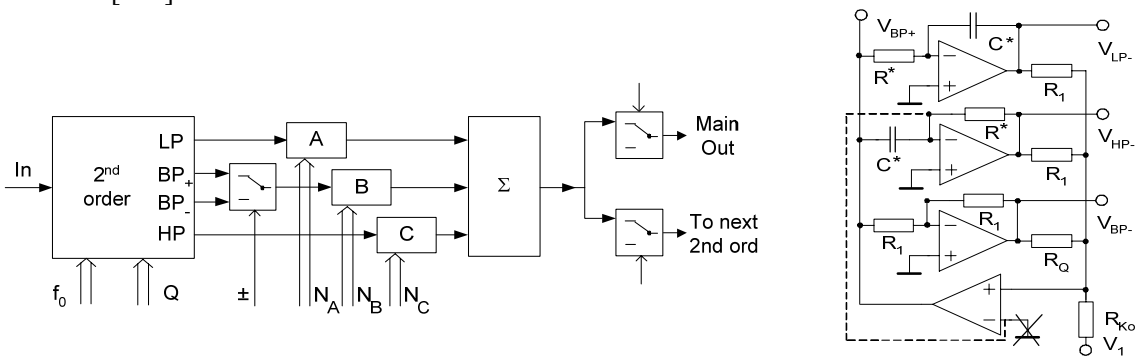
In the input of instrument we can see an amplifier with variable voltage gain allowing optimal setting of the amplitude level. In the structure, the signal flow is mediated by the analog switches. These switches allow us to determine the order of filter or, for instance, to isolate each block for its independent use. We can also connect one arbitrary output of the block to the global filter output (marked as V_{OUT} in *Fig. 8.11*). The switches position and the values of all variable parameters (f_{0i}, Q_i ,A_i, B_i, C_i) are controlled *via* the serial bus (I^2C) from the microprocessor. The configuration of the entire instrument can be commanded manually using the integrated miniature keyboard or, alternatively, it can be commanded by a computer (PC). The parameters are displayed on the LCD screen placed together with the keyboard in the front panel of the instrument.

8.5.2 Electrical Design of Filter Blocks

The design of the 1st and 2nd order blocks must respect the specifications of the (8-8) transfer, whereas all basic transfers (LP, HP and ±BP for the 2nd order) have to be realized using a single active structure. Moreover, independent controlling of F_0 and Q is required.
A suitable solution can be illustrated by the topology of the 2nd order block shown in *Fig. 8.12*. Here, the inputs parameters (F_0, Q, N_A, N_B, N_C) are a 10-bits binary word. (The structure of the 1st order block is equivalent). The numerators coefficients of (8-8) are determined by variable gain amplifiers

tel-00417838, version 1 - 17 Sep 2009

(blocks A, B, C) following the biquadratic section. Their outputs are summarized in the last block which leads to the output switches (as shown in *Fig. 8.11*.) As the biquadratic section, the modified *Akerberg - Mossberg* network presented in [114] was selected (see *Fig. 8.12 b*)). This block is a "state variable" interpretation of the 2nd order transfer function simulating the parallel RLC circuit and conforming to all the above-mentioned specifications. The dotted line in *Fig 8.12* is used to provide an additional compensation of the 2nd pole (stability) as suggested in [114]. The control of the F_0 frequency is provided roughly in four ranges (1 Hz -100 Hz, 100 Hz-1 kHz, 1 kHz-10 kHz and 10 kHz-120 kHz) *via* the value of capacitor *C**. The fine frequency setting is provided by the value of *R**. All variable parameters are controlled by the 10-bits R-2R type four-quadrant DA converter AD7533 [115].



a) *b*)

FIG. 8.12: *The block scheme of the 2nd order section (containing a biquadratic filter, switches and variable gain amplifiers A, B, C.). The parameters are controlled by 10 bits D/A converter), b) The Modified Akerberg - Mossberg biquad with second pole compensation [114] used as the 2nd order section.*

In order to provide high accuracy of the parameters, a set of the calibration characteristics was obtained by variable measurements. The universal calibration functions (the nonlinear function peculiar to each frequency range) were implemented in the controlling microprocessor and can be individually adjusted for each block by the help of measurements and embedded algorithms. As an example of the resulting accuracy, *Fig. 8.13* shows a typical curve of relative error of F_0 frequency in the function of the control DAC number (higher 10 kHz-120 kHz range).

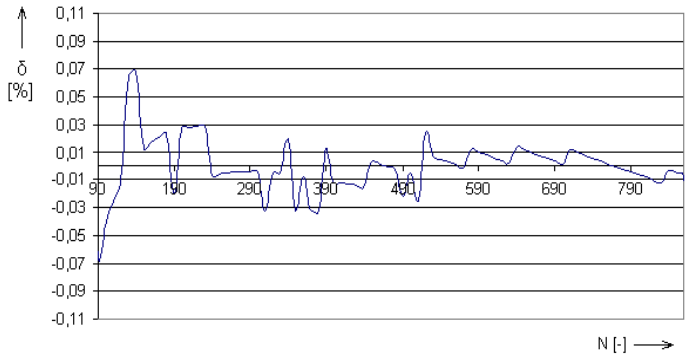


FIG. 8.13: *The measured relative error of resonant frequency f_0 plotted in the function of the DAC control number*

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

8.5.3 Control Software of Frequency Filter

In order to facilitate the controlling of the filters, a complex microprocessor control unit has been developed. Amongst the various functions ensured by the control unit there are, for example, these most important aspects:

- Management of the user interface
- Controlling of the 1st and 2nd order blocks parameters (DA convertor and switches)
- Calibration and correction of the frequency
- Interface with the computer
- Non-volatile memories and others

As the core of the control unit, a microprocessor (μP) Motorola® MC68HC912B32 was used together with the control program developed in the "C" programming language under the Codevarior® environment. Communication between the microprocessor and the blocks of filters is based on the I^2C bus, and the computer interface uses the serial RS232/USB bus (see the detailed chart in *Fig. 8.14*, left side)

In addition to the integrated front-panel keypad and the LCD display enabling the complete autonomous operations and control of the device, the controlling can be also performed by a superior computer. For this purpose, a user-friendly control software product "*Frequency Filter Design studio* FFD" was developed. Its hierarchy and functions were designed to provide a simple interface and, importantly, to enhance the versatility of the instrument. The main purpose of the software product is to calculate the transfer function parameters and to ensure their (instantaneous) transfer into the device.

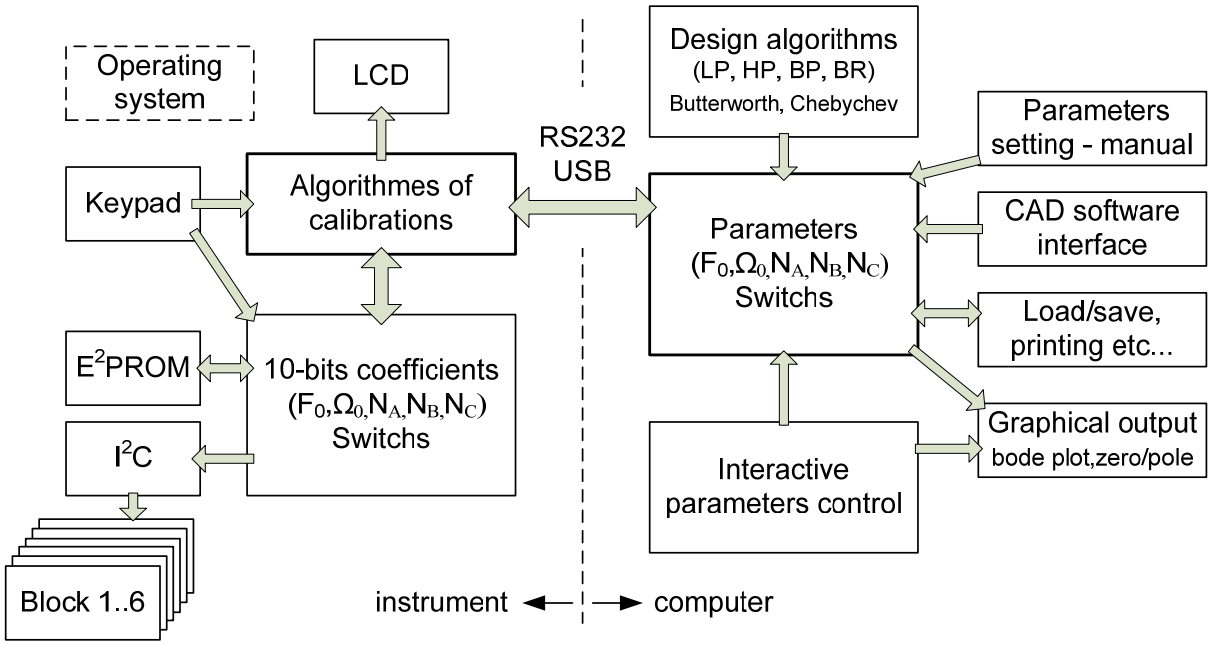


FIG. 8.14: *Controlling of the instrument. Left side: the functions provided by the microprocessor in the instrument, right side: the functions implemented in the FFD computer software. All data exchange is "real time"*

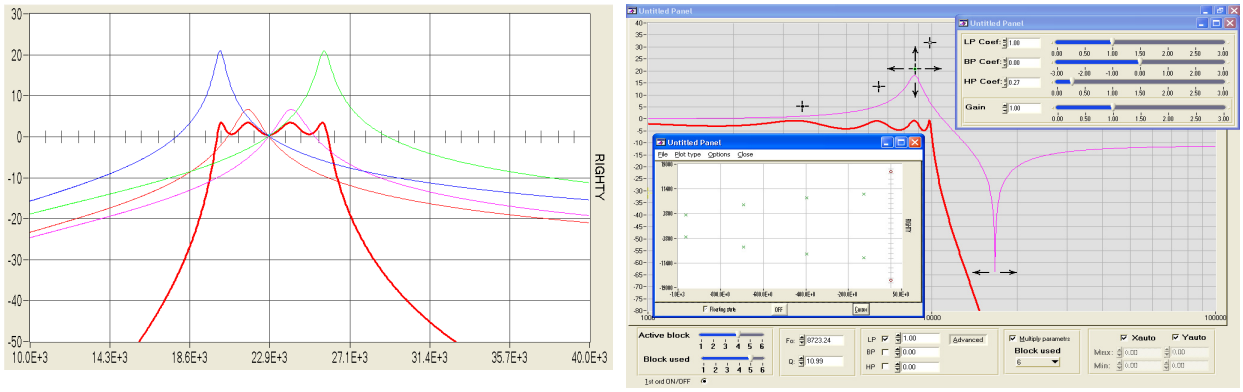
However, the computation of coefficients is still provided by the control μP via the algorithms of calibrations. In order to specify the basic functionalities of the program, let us mention the following points:

- Provision of design algorithms of the transfer function (according to the *Fig. 9.2* diagram)

- Graphical interpretation of the transfer function in all magnitude, phase and zero/pole plots (see *Fig. 8.15 a* for the example)
- Real time adjustments (and transfer into the device) of coefficients of the transfer function *via* their numeric values or by the graphical interface (see *Fig. 8.15 b* and the description below).

As shown in the detailed chart, *Fig. 8.14*, the FFD provides additional options such as the configuration of the internal switches or the interface with the engineering design software. We show here two examples of screen captures of the FFD studio. The first one (*Fig. 8.15 a*) shows an exemplary output of the design routines: 8th order Chebyshev BP with the detailed transfer of all 2nd order blocks.

The screen capture *Fig. 8.15 b*) is a "*key*" user interface. On the screen, we can see an 8th order low-pass filter with the detailed complex pole-zero location in the left sub-window. On the main screen, the resulting characteristic of the filter is displayed together with the transfer of one arbitrary 2nd order block. The parameters of the 2nd order blocks can be set either by setting the exact (numeric) value in the upper sub-window, or by the mouse sliding on the screen as suggested by the flashes. Here, the X position corresponds to the central frequency (F_0) of the block and the Y position to the quality factor Q. These modified parameters are immediately included in the final characteristic and (in the real time) transferred into the instrument.



a) *b*)

FIG. 8.15: *Screen captures of the FFD studio software, a) the graphical interpretation of BP filter as the sum of particular transfers of each block, b) the virtual design and control of the filter parameters*

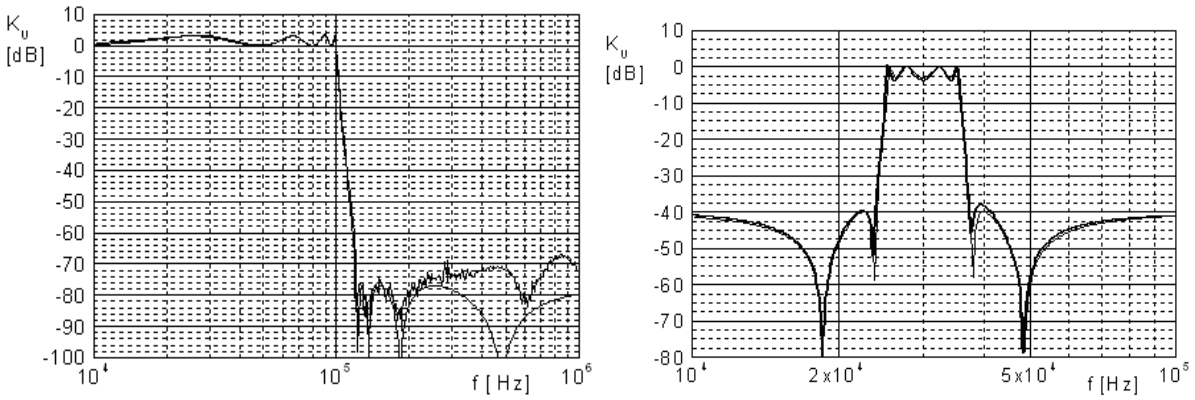
8.5.4 Realisation of the Instrument and Conclusion

The physical realisation of the instrument is shown in *Fig. 8.16*. The layout of the front panel items can be compared with the block hierarchic structure shown in *Fig. 8.11*. The left side part includes the user interface, the processor control unit, and the power supply part. The right side part includes the m+1 blocks of filters. Each block is equipped with the input and output connectors important for their individual use. The last block contains the central output, where an assignment is indicated by the graphical lines and pilot lights.

In order to demonstrate the achieved properties of the filters, we present two examples of the 8th order LP and BP filters with inserted zeros (*Fig. 8.17*, the elliptic Cauer approximations). In practice, this approximation requires very high accuracy and quality factor of building components. However, the obtained results fitting perfectly with the computed approximation confirm the fact that this instrument is capable of realizing even very complicated transfer functions.

tel-00417838, version 1 - 17 Sep 2009

FIG. 8.16: *The final realisation of the instrument*



a) *b*)

FIG. 8.17: *Theoretical and experimental responses of the a) 8th order LP filter, b) 8th order BP filter. Both are based on the Cauer approximations*

The measured dynamic range (determined mostly by the noise level and obtained with the filters without inserted zeros) attains approximately the value of 110 dB. This value allows us to employ the instrument even in the most demanding applications like the test-bench of a cryogenic bolometric detector or the nonlinear ultrasound spectroscopy for NDT (Non-Destructive Testing, see [116] for an example). Here, the benefits of the analog signal pre-processing can be clearly seen.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

9 BIQUADRATIC CASCADE SECTIONS WITH INCREASED ATTENUATION

9.1 Biquadratic Sections for Cascade Filter Design

The synthesis of cascade frequency filters is based on fractional decomposition of the transfer function (8-1) into low order (1st and 2nd) transfers (*Fig. 8.9*). As shown in *Fig. 8.9*, these low order blocks are serially connected. Although this serial connection makes the cascade synthesis relatively simple, the final electrical design can utilize many potential solutions. The family of the 2nd order (biquadratic) electrical circuits can be classified according to many criteria. The most important criteria are high frequency performances and the scale of achievable quality factor [94]. In this study, we will examine the high frequency performances. Our objective is to analyze the main causes limiting the frequency range of active frequency filters and, on the basis of these analyses, to design new structures facilitating an increase of the maximum cut-off frequency.

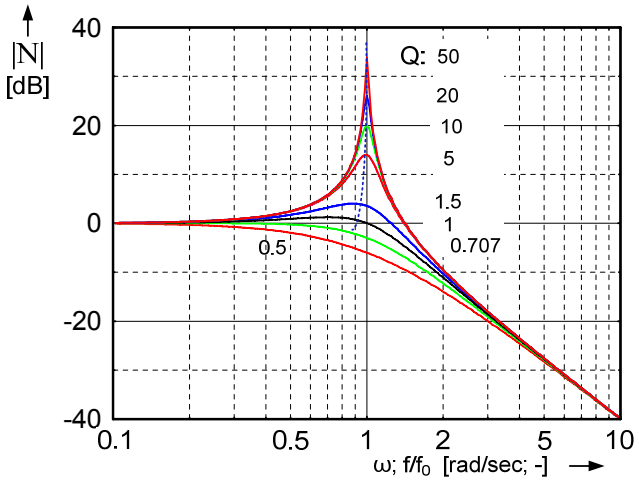


FIG. 9.1: *The normalized 2nd order LP transfer function plotted for $\Omega_0 = 1$ and various quality factors*

The first part of this study comprises a brief introduction of the 2nd order transfer function and of the basics of electrical structures used in the design of cascade filters. It will be shown that the use of *real active elements* may have strong (negative) impact on the frequency characteristic of the filter.

The figures of merit frequently used to compare the high frequency behavior of biquadratic filters are the following characteristics: passive sensitivities, gain-sensitivity products GSP, and deviations of Ω_0 and Q caused by the limited bandwidth of amplifiers [94],[95]. We will focus on the low-pass frequency filters based on the Single Amplifier Biquad (SAB) where limited frequency bandwidth of the amplifier may become the cause of spurious transfers in the stopband area of the AC transfer characteristic.

In contrast to the compensation of the Ω_0 and Q parasitic shift (*e.g.* by using a predistortion technique as suggested in [119]), the degradation of the stop band characteristics can not be simply compensated. Regular ways of increasing rejection in the stopband consist in either the use of high frequency active devices (Operational Amplifiers) or an increase of the order of the transfer function (the number of cascaded blocks). Both these ways feature rather high power consumption and final device cost. However, an increase of attenuation can be also achieved by means of proper choice of the active biquadratic structure.

Further, we will point out the fact that the causes of increased transfer in the stopband area are similar for many biquadratic structures. This will be demonstrated by an analysis performed on two biquadratic sections: the FDNR based 2nd order network, and the Sallen-Key low-pass filter. The main parameter that will be used for the characterization is the *frequency and multiplicity of parasitic zeros* in the *real* transfer function (*i.e.* the transfer function that is obtained using the real model of operational amplifier). Afterwards, the increase of this frequency or "removal" of the parasitic zeros from the transfer function can lead to the increase of achievable attenuation and, consequently, to the extension of the use of biquadratic structures to higher frequencies. Although the different biquadratic structures show different influences of the OA real properties, we will focus in the first part of the analysis on the most widely used (yet not optimal) *Sallen-Key* biquad [120]. On the basis of the investigation of this filter, an improved *type II Sallen-Key* low-pass cascade section with increased attenuations will be shown. Then, we will utilize the conclusion resulting from the previous analysis in order to design a *CCII based biquadratic section* with, ideally, no spurious transfer in the stopband area.

All the theorems and solutions mentioned in the following sections will be simultaneously confirmed by the simulations and experimental measurements performed on the fabricated filters.

9.1.1 The Biquadratic Transfer Function

The biquadratic transfer function is a representation of the general 2nd order differential equation that relates the input and output of a 2nd linear time-invariant system. This function is usually written in terms of the Laplace operator "s", real coefficients a_i, b_i or cut-off frequency Ω_{0i} (F_0), and quality factor Q_{0i}:

$$\boldsymbol{N}_i(s) = \frac{s^2 + b_{i1}s + b_{i0}}{s^2 + a_{i1}s + a_{i0}} = \frac{A_i s^2 + B_i s\Omega_{0i}/Q + C_i\Omega_{0i}^2}{s^2 + s\Omega_{0i}/Q_i + \Omega_{0i}^2}, \tag{9-1}$$

where i means the i-th blocks in the cascade. It can be shown that the values of A_i, B_i, C_i determine the filter type realized by the i-th block. An instance of realisation of the basic filters follows here :

- $A_i=1;\ B_i=C_i=0 \rightarrow$ *high-pass*
- $B_i=1;\ A_i=C_i=0 \rightarrow$ *band-pass*
- $A_i=B_i=0;C_i=1 \rightarrow$ *low-pass.*

tel-00417838, version 1 - 17 Sep 2009

An arbitrary choice of the coefficients A_i, B_i, C_i results in the superposition of the *LP, BP* and *HP* transfers. This superposition is required in some particular cases like the synthesis of elliptic filters (filters with inserted zeros in the transfer function) or the synthesis of *all- pass filters*.

The physical interpretation of Ω_{0i} and Q_{0i} can be shown in the example, *Fig. 9.1,* of magnitude characteristic plotted for the low pas transfer ($A = 1$). We can see that the quality factor Q_{0i} corresponds to the voltage transfer (resonance gain) at cut-off frequency Ω_0 ($|\boldsymbol{N}(\omega=\Omega_0)| = Q_0$). For instance, the typical -3dB value of voltage transfer at cut-off frequency Ω_0 can be obtained for the quality factor of $Q_0 = 1/\sqrt{2}$. For higher values of quality factor, the AC response shows a resonance gain resulting in the ringing in the filter time response.

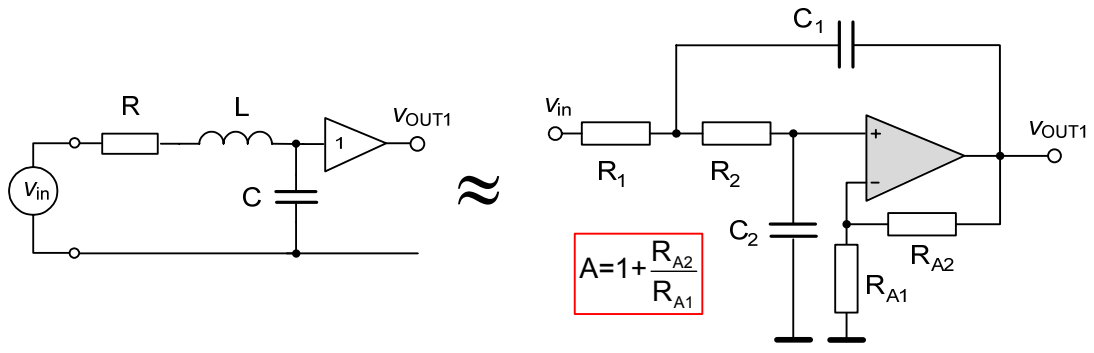
The roll-off slope of the biquadratic LP and HP transfer reaches -40dB per decade, whereas the band-pass or bandreject filters are characterized by the value of -20dB/decade (see *section 8.3.1*). In order to illustrate the basic properties of a standard 2nd order transfer function and the related RLC circuits, a simple software tool has been developed for educational purposes [128]. The complex design tool *Frequency Filter Design Studio* allowing the interactive synthesis of cascade filter has been developed within the frame of the [112] project (see *section 8.5.3*).

9.2 Active Biquadratic Sections

In the field of analog filters design, a large scale of active biquadratic sections has been developed throughout the history of electronics (see [94], [100]). The classification of these circuits is based on various criteria. Among the most important types of classification there is the classification according to the *numbers of active elements*.

9.2.1 Single Amplifier Biquad (SAB)

Sallen-Key: One of the best-known circuits in the field of analog filters design was introduced by R.P. Sallen and E. L. Key of MIT Lincoln Laboratory in 1955. This biquadratic structure is called *Sallen-Key* (S-K), and its realization with a voltage feedback operational amplifier (OA) is shown in *Fig. 9.2 b)*. A simple transformation of circuit from *Fig. 9.2* allows us to obtain other types of filters, for instance permuting the $R_{1,2} \leftrightarrow C_{1,2}$ results in the HP filter.



a) *b)*

FIG. 9.2: *The low-pass passive RLC circuit and the equivalent Sallen-Key active filter*

By means of an analysis using the ideal operational amplifier, we obtain the expressions of cut-off frequency Ω_0 and quality factor Q_0 in the well-known form:

$$F_0 = \frac{1}{2\omega\sqrt{R_1R_2C_1C_2}} \qquad Q_0 = \frac{\sqrt{R_1R_2C_1C_2}}{(1-A)R_1C_1 + R_2C_2 + R_1C_2} = \frac{1}{2}\sqrt{\frac{C_1}{C_2}}\bigg|_{A=1,R_1=R_2}, \tag{9-2}$$

tel-00417838, version 1 - 17 Sep 2009

where A is the frequency-independent voltage gain given by the feedback resistors R_{A1}, R_{A2}.

In the process of practical design we can follow miscellaneous objectives like low dispersion of component values (K_C, K_R) or low relative sensitivities $S^{x_i}_{\Omega_0,Q_0}$. Three different approaches are used on the basis of the initial choice of component values. These approaches are as follows:

- **Equal components ($C_1 = C_2$, $R_1 = R_2$)**
- **Equal capacitors ($C_1 = C_2$)**
- **Equal resistors ($R_1 = R_2$)**

i) **Equal $R_1 = R_2$ and $C_1 = C_2$.** For this configuration, the quality factor (9-2) can be simplified as:

$$Q_0 = \left.\frac{\sqrt{R_1 R_2 C_1 C_2}}{(1-A)R_1 C_1 + C_2\left(R_2 + R_1\right)}\right|_{\substack{R_1=R_2 \\ C_1=C_2}} \Rightarrow Q_0 = \frac{1}{3-A}. \tag{9-3}$$

Here, it appears that the quality factor can be adjusted independently of the Ω_0 by virtue of the value of static gain A. However, this voltage gain determines also the gain in the passband; this gain can be compensated by an additional circuit. We can see that, approaching the value of $A = 3$, the quality factor approaches infinity and the circuit becomes *marginally stable*. In practical design, the maximal value of quality factor is relatively low ($Q_0 \approx 10$), limited by the increasing sensitivities.

ii) **Configuration with equal capacitors $C_1 = C_2$**: This design is used for the cases where a limited range of capacitor values is available. The resistance ratio is set according to (9-2). However, this type of filter is not optimal in respect of sensibility.

iii) **Equal resistors $R_1 = R_2$:** The approach is considered as optimal to reach lower sensitivities on the passive components. The relative sensitivities $S^{\Omega_0}_{R_1,R_2,C_1,C_2}$ reach the value of 0.5 for $A = 1$, whereas the sensitivities of $S^{Q}_{R_1,R_2} = 0$ and $S^{Q}_{C_1,C_2} = 0.5$ [94],[95]. For equal resistances R_1=R_2, the dispersion of capacitors values C_1 and C_2 can be defined from (9-2) as:

$$K_C = \frac{C_1}{C_2} = 4Q^2. \tag{9-4}$$

The dispersion of capacitors, however, limits the maximum achievable quality factor. In this context, reference can be made to source [94] which deal with the *Gain Sensitivity Product* (GSP or Γ) (a function respecting the influence of an active element on the Ω_0 and Q_0 parameters). In [95], a technique that provides a very low value of the GSP is shown, using a slight increase of the static gain A (for the equal resistance configuration). Generally, the optimum between the sensitivities and the GSP can be found in the range of $K \approx 1.3$.

The *S-K* filter realized with real components is affected by many parasitic influences (see *section 8.4*). Among the most significant of these influences there is the widely discussed shift of Ω_0 and Q_0 [117], [118], which is important mainly for higher frequencies. The techniques of *predistorsion* allowing us to anticipate the influence of active elements have been developed and discussed in various sources (see, for instance, [119]), and they can be performed in a simple manner using the simulation design tools.

Furthermore, the experimental measurements carried out on the S-K filters show a *systematic degradation of the stopband characteristic* that causes the remounting of the ideal -40dB/decade roll-off rate [122], [134]. This remounting induces lower attenuation in the stopband, and the situation

tel-00417838, version 1 - 17 Sep 2009

consequently brings about spurious transfer in that area. The degradation becomes more important for higher resonant frequencies (F_0 above 1 MHz) or, generally, for circuits where the unity gain frequency f_T of the operational amplifier is close to the cut-off frequency F_0 (as a rule, $F_0/f_T \approx 0.1$ is considered as a reasonable limit). In the following text (*section 9.4*) we will analyze this degradation in order to determine the main causes as well as to design the improved *type II* Sallen-Key filter.

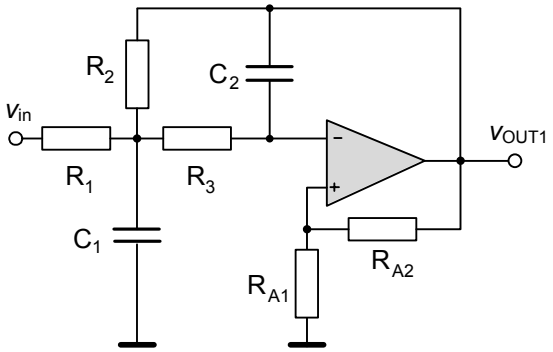


FIG. 9.3: *The multiple feedback network (MFB) low-pass filter*

The Multiple Feedback Network: An alternative to the *Fig. 9.2 b)* Sallen-Key network is the *Multiple Feedback Network Biquad MFB*, *Fig. 9.3* [121]. The MFB filter uses a *non-inverting* amplifier as the active element. The DC gain can be set by $A = -R_2/R_1$ (for the grounded (+) terminal) or, alternatively, it can be adjusted by R_{A1} and R_{A2}. The transfer in the pass-band is inverted, which means that the phase difference between the input and the output signal reaches $\varphi = -180°$. The cut-off frequency and quality factor can be obtained by using the ideal OA model:

$$F_0 = \frac{1}{2\pi\sqrt{R_2R_3C_1C_2}} \qquad Q_0 = \frac{\sqrt{R_2R_3C_1C_2}}{C_2\left[R_2+R_3\left(1+A\right)\right]} = \frac{1}{3}\sqrt{\frac{C_1}{C_2}}\bigg|_{A=1;R_2=R_3}, \tag{9-5}$$

where, for the unity gain A, the dispersion of the capacitors´ values is:

$$K_C = \frac{C_1}{C_2} = 9Q^2 \tag{9-6}$$

and can be compared with (9-4). It follows from this that, in order to obtain an identical quality factor, the dispersion of capacitors C_1 and C_2 will be higher for the MFB filter than for the *S-K*. However, as we will see later, the grounded capacitor in the signal way is convenient with respect to the high attenuation in the stopband. This is also why that MFB structure can be more interesting for higher frequency applications.

For applications requiring higher quality factors (like Chebychev or Cauer approximations), we use the multiple active elements networks.

9.2.2 Multiple Active Element Biquad: Antonius GIC

As noted in *chapter 8.3.2*, the active 2nd order *lossless* element can be only realized by employing at least two active elements (Operational Amplifiers). This is also valid for the cascade blocks. The presence of a higher number of active and, usually, also passive elements can be considered as providing a higher degree of freedom for the designer. This may also result in the obtainment of some interesting features of certain networks; these features include, for example, the independent tuning of

tel-00417838, version 1 - 17 Sep 2009

Ω_0 and Q_0 or the availability of all standard transfers (*LP, BP,BR, HP*). An instance is provided in *Fig. 8.12*, where the modified Akerberg – Mossber biquad [114] is shown.

Generally, there are two types of approach utilized for the design of the multiple-active element biquadratic sections: the application of the *Antonius GIC* configuration, and the use of the *state variable* networks.

We will show here an example of the Antonius low-pass biquadratic section. This two-OA filter is based on the Antonius GIC (General Impedance Converter, see *chapter 8.3.2*) and is shown in *Fig. 9.4*. The circuit provides a low-impedance output realized by the output of OA_2. In order to realize the low-pass transfer, we can use three different configurations of the passive components [95].

The zero losses in the Antonius biquad correspond to the infinity quality factor of the filter. This is why the value of the quality factor has to be set by an external dumping element. By reviewing the concept of the FDNR (RCD) active filter design (*chapter 8.3.2*), the quality factor can be determined by the external dumping capacitor C_Q. The dispersion of capacitors K_C *is no longer dependent upon* Q_0 as is the case with the dispersion K_C of SAB filters (see *Eq.*(9-4) and *Eq.*(9-6)). This property can be seen on the equations of resonant frequency F_0 and quality factor Q_0:

$$F_0 = \frac{1}{2\pi\sqrt{R_2 \cdot R_4 \cdot C_1 \cdot C_3}}\sqrt{\frac{R_5}{R_6}} \qquad Q = \frac{\sqrt{C_1 C_2}}{C_Q}\sqrt{\frac{R_2 R_3}{R_1 R_4}}\,. \tag{9-7}$$

Furthermore, the analysis shows a low value of $S_{x_i}^{Q}$, which is also independent of the quality factor.

Concerning the high frequency properties, the effects of active elements on the Ω_0 and Q_0 values can be investigated for each active element (OA_1, OA_2). For instance, *Fig. 9.4* shows OA_1 with the feedback capacitor C_2; thus, the amplifier is, in fact, similar to an integrator. It can be shown that the requirements placed on OA_1 are much lower, which facilitates the realization of an economical design reducing the power consumption ($f_{T1} << f_{T2}$). The typical values of quality factor achieved by the Antonius GIC in *Fig. 9.4* are within the order of several hundredths (up to frequencies of around $0.1 \cdot f_T$ of OA).

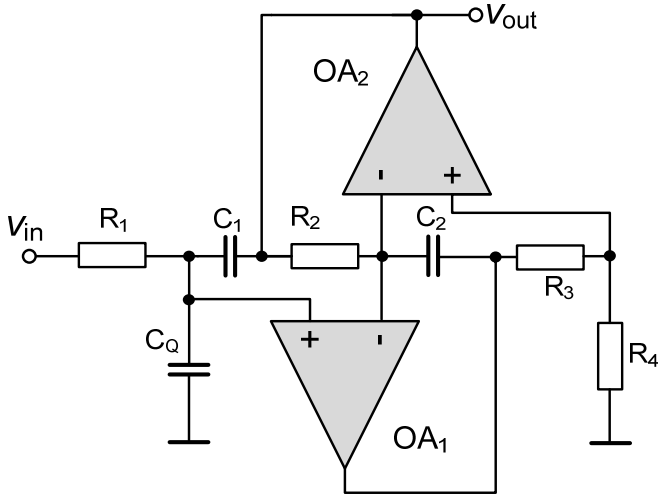


FIG. 9.4: *The Antonius GIC- based biquadratic LP section*

tel-00417838, version 1 - 17 Sep 2009

9.3 Degradation in the Stopband of LP Filters

Fig. 8.2 presented in the previous section shows that a fundamental parameter of the filters is the minimal attenuation in the stopband $|\boldsymbol{N}|_{\min}$. However, the achievement of high attenuation can be difficult, mainly at higher frequencies. The real transfer function (of low-pass filters) contain n multiple *parasitic zeros* reducing the ideal slope of -40dB/decade by the rate of n·20dB/decade. For this reason, the frequency f_Z and quantity n of the parasitic zeros will be investigated in order to classify high frequency performances of the cascade sections.

In practice, the achievement of high stopband attenuation results in the use of fast active elements (*e.g.* the OA with ~GHz f_T frequency). However, the increasing power consumption and device cost make this solution less interesting.

In this chapter, two exemplary biquadratic sections (the *S-K* and "*FDNR"*) will be investigated in order to explain the reasons of the parasitic zeros origination. On the basis of these analyses, we define the rules applied for the future design of active biquadratic sections with increased stopband attenuation. Consequently, two biquadratic sections will be designed: a modified *type II Sallen Key* filter (*chapter 9.4*), and a *current mode CCII biquadratic* section (*chapter 9.5*).

In the first phase we will use a "low-performance" OA, the *LM-741* (f_T = 1 MHz, R_{out} = 75 Ω), for the realization. Sequentially, high frequency measurements will be performed using the standard higher frequency active elements.

9.3.1 Causes of the Parasitic Effect

In active frequency filters based on the standard technologies (*e.g.* CMOS), the high frequency performances are mostly determined by active elements. In the following text we will focus on the most frequently used active element: the Voltage Feedback operational Amplifier (or the VFA) labeled as OA.

The frequency properties of operational amplifiers are commonly described by the linear single or two-pole model characterized by time constants τ_1, τ_2 and DC gain A_0 (the origins of the dominant pole have been explained in *chapter 4*). The differential open loop voltage gain A(s) can be written as:

$$A(s) = \frac{A_0}{(\tau_1 s + 1)} \approx \frac{A_0}{\tau_1 s}. \tag{9-8}$$

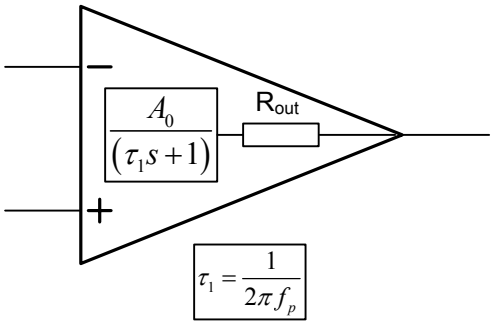


FIG. 9.5: *The linear single pole model of Operational Amplifier (OA)*

The typical values of commercial OpAmp's are within the ranges of 80–120 dB for the DC gain and 5 Hz to 1 kHz for the frequency of the dominant pole. The frequency at which the open loop gain reaches unity is labelled as the f_T or GBW product (see *chapter 4*). Further, as we will see, the parasitic

tel-00417838, version 1 - 17 Sep 2009

zeros of the filters occur generally much below the second pole $1/\tau_2$. This is why the parasitic zeros considered in this chapter are reflected only as the consequence of the 1st pole $1/\tau_1$. For this reason, the OA model in *Fig. 9.5* is adequate for our analysis. The 1st order OA mode can be characterized by the following points:

- the 1st order transfer function (*Fig. 9.5*), *Eq*. (9-8)
- final output resistance R_{out} (considered as constant for all frequencies)

However, in order to obtain more accurate results (especially at higher frequencies), a high order (complex) model can be used for the numeric simulations.

Fig. 9.6 shows a typical (idealized) characteristic of a low-pass biquadratic section realized by means of a real operational amplifier. For the double parasitic zero, the original -40dB/dec slope decreases to 0dB/dec. More zeros in the transfer function cause the remounting of AC characteristics; in certain cases, the characteristics can even cross the 0dB axis (see *Fig. 9.21*).

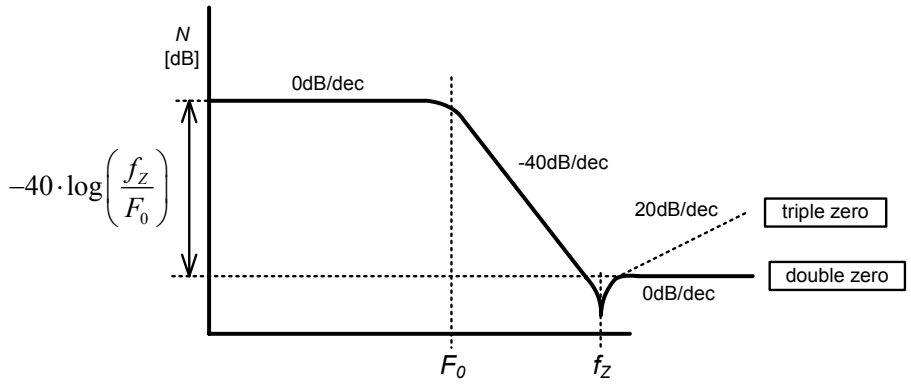


FIG. 9.6: *The effect of parasitic zeros in the AC response of frequency filter*

In addition to the multiplicity of parasitic zeros n, the difference between cut-off frequency F_0 and the parasitic transfer zero frequency f_Z is an important figure of merit allowing us to estimate the maximal achieved attenuation ATT_{max}:

$$ATT_{\max} \approx -40\log\left(\frac{f_Z}{F_0}\right). \tag{9-9}$$

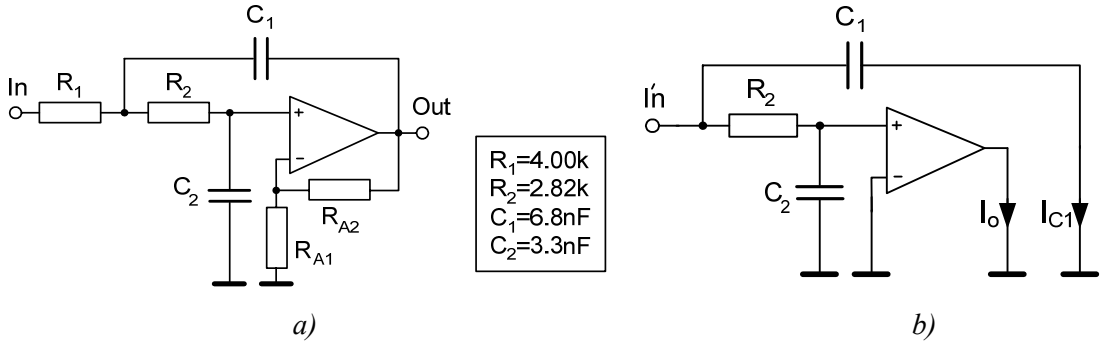
In many biquadratic filters, high values of f_Z/F_0 can be achieved by means of proper choice of the operational amplifier, where the cut-off frequency F_0 is to be placed much below the f_T frequency ($f_0 < 0.01 f_T$). Contrary to this, the realization of a low-pass filter above several units of MHz may show very low stop band attenuation in the order of several units of dB.

There are only a limited number of ways leading to an increase of the stopband attenuation. As a matter of fact, we can either use the above mentioned high-performance (high-consumption) active elements or try to realize proper choice of active structure. Among the good candidates respecting this specification can be found, for example, the conventional OTA-C filters containing the grounded capacitors [129], or the MFB network from *Fig. 9.3*.

tel-00417838, version 1 - 17 Sep 2009

9.3.2 Stop Band attenuation of the Sallen-Key LP Section

The single pole model of the real OA (*Fig. 9.5*) will be used to examine the parasitic zero frequency f_Z of the Sallen-Key circuit described in *Fig. 9.7 a*). In doing so, the value of f_Z can be determined trivially by applying the model (9-8) into the circuit shown in *Fig. 9.2*. However, an intuitive way will be utilized to determine the value of f_Z in order to explain the reasons leading to the origination of the parasitic zeros.



a) *b)*

FIG. 9.7: *a) the Sallen Key low-pass filter designed for F_0= 10 kHz and Q_0 = 0.707*
b) the superposition of two current ways leading to parasitic zeros

In order to determine the f_Z of the low-pass filter shown in *Fig. 9.7 a*), we can make the following computation-simplifying presumption: As the attenuation at f_Z reaches generally high values, a complex transfer of the filter is situated close to the imaginary axis. In other words, the output voltage is almost zero at the f_Z frequency. This allows us to "virtually ground" the output of the OA (only at the f_Z), and to *isolate two current ways*: i_{C1} and i_{OUT} (*Fig. 9.7 b*). In order to facilitate the location of zero frequency, the magnitudes of I_{C1} and I_{out} has to be equal, therefore:

$$I_{C_1} = -I_{out} \tag{9-10}$$

Here, we can deduce that resistor R_1 does not affect f_Z as the R_2 and C_1 are on the identical potential $v_{in}^{'}$ (*Fig. 9,7 b*). Equation (9-10) can be expressed in terms of I_{C1} and I_{out} as:

$$I_{C1}(s) = s \cdot C_1 \cdot V_{in}^{'}(s)\,, \tag{9-11}$$

and

$$I_{out}(s) = \frac{A_0}{s^2 R_2 C_2 \tau_1 + s(\tau + R_2 C_2) + 1} \cdot \frac{V_{in}^{'}(s)}{R_{out}}. \tag{9-12}$$

By performing a certain degree of simplification, the (9-10), (9-11) and (9-12) expressions result in the *triple parasitic zero at the frequency of*:

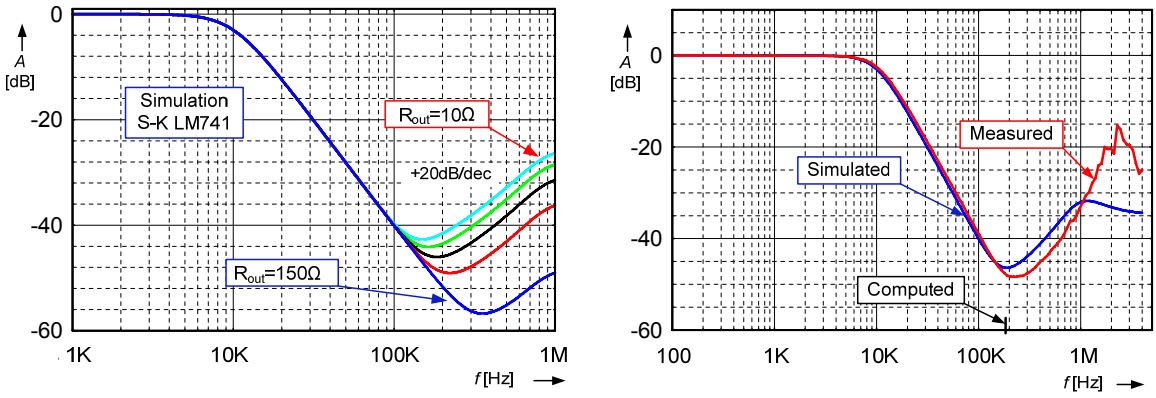
$$f_Z \cong \frac{1}{2\pi}\sqrt[3]{\frac{2\pi\left(f_p \cdot A_0\right)}{R_{out} R_2 C_1 C_2}} = \frac{1}{2\pi}\sqrt[3]{\frac{2\pi GBW}{R_{out} R_2 C_1 C_2}}\,, \tag{9-13}$$

In this expression, the influence of components on the value of the parasitic zero frequency can be seen. Equation (9-10) shows that the stopband parasitic zeros result from the *direct signal way* between the source and the output of the filter. This direct way is provided by capacitor C_1.

In order to express graphically equation (9-13), we have performed a stepped simulation for various values of R_{out} (*Fig. 9.8 a*), and the measurement on the fabricated sample (*Fig. 9.8 b*) (both with the

tel-00417838, version 1 - 17 Sep 2009

identical OA LM-741). On these characteristics there can be observed good agreement between *Eq.* (9-13), the simulation, and the experimental results.

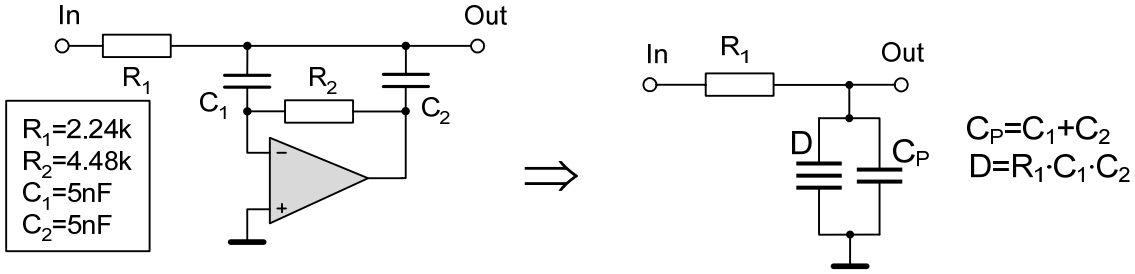


a) *b)*

FIG. 9.8: *a) The simulation of the S-K for various R_{out}, b) a comparison of the measurements, simulation, and Eq.(9-13) performed on the circuit from Fig. 9.7a) (both characteristics obtained with LM 741)*

9.3.3 The lossy RCD 2nd Order Section

The second investigated network is a one-port reactive network – the lossy FDNR (see *chapter 8.3.2,* [123]). The FDNR has been used to realize the low-pass transfer, where its configuration arises from the Burton transformation RLC → RCD (see *Fig. 8.7*). In *Fig. 9.9*, resistor R_1 simulates a serial inductor. The complete circuit is a two-port 2nd order circuit with a high impedance output.



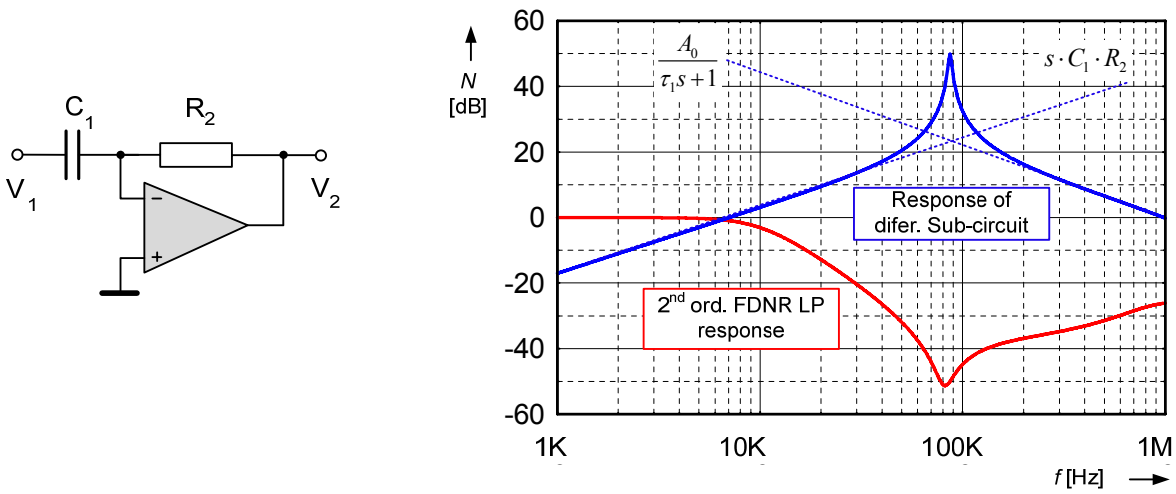
a) *b)*

FIG. 9.9: *a) The LP RCD filter realized with the lossy FDNR and b) its equivalent schema (D is the value of the FDNR)*

The voltage output of the operational amplifier creates, in fact, a band-pass filter. As the resistor value is frequency-independent, the parasitic zero in the transfer function V_{out}/V_{in} is only caused by the zero occurring in the FDNR impedance $D(s)$. This zero is caused by the differentiator sub-circuit as shown in *Fig. 9.10 a)*.

The frequency transfer of an ideal differentiator is given as $s \cdot R_1 \cdot C_1$ and has an increasing magnitude AC characteristic with a positive 20dB/dec slope. This characteristic is, however, limited at higher frequencies by a limited gain of the OA. This limitation causes the output voltage v_2 to decrease at a certain frequency. This decrease in voltage influences the current through C_2, and consequently it also exerts influence on the transfer of the biquadratic section. This is why the cut-off frequency of the differentiator sub-circuits corresponds to the zero frequency of the FDNR. This situation is demonstrated in *Fig. 9.10 b)*, which shows the response of the filter shown in *Fig. 9.9 a)* and the differentiator sub-circuit *9.10 a)*.

tel-00417838, version 1 - 17 Sep 2009



a) *b*)

FIG. 9.10: *a) The differentiator sub-circuits, b) a comparison of the differentiator sub-circuit (a) response with the Fig. 9.9 voltage transfer (LM741 SPICE Model)*

In this figure we can see the "resonance" of the differentiator sub-circuit and its relation to the magnitude transfer of the filter. The "resonance" frequency of the differentiator can be obtained by means of using the single pole *Fig. 9.5* OA model. The voltage transfer of *Fig. 9.10 a*) circuit can be written as:

$$N(s) = \frac{V_2}{V_1} = \frac{s \,.\, A_0 \,.\, R_2 \,.\, C_1}{\tau \,.\, R_2 \,.\, C_1 \cdot s^2 + R_2 \,.\, C_1 s - A_0}, \tag{9-14}$$

and is equivalent to the 2nd order band-pass transfer. The resonance can be simply found as a root of the denominator polynom, which results into:

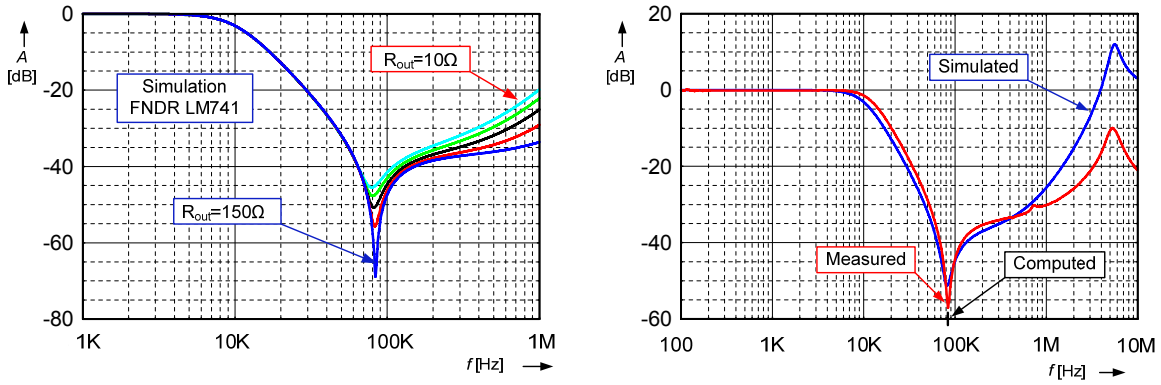
$$f_z = \frac{1}{2\pi}\sqrt{\frac{2\pi f_p \left(A_0 - 1\right)}{C_1 R_2}} \doteq \frac{1}{2\pi}\sqrt{\frac{2\pi GBW}{C_1 R_2}}\,. \tag{9-15}$$

The value of zero frequency shows two interesting features: *the transfer zero is of the 2nd order and does not depend on the value of* R_{out}. This independence is shown by the simulations in *Fig. 9.11 a)* for the stepped value of R_{out} (performed with a higher order of the model).

Fig. 9.11 b) shows the comparison of the measured and the simulated characteristic obtained with the LM-741 operational amplifier. We can see good agreement between these two characteristics and the analytical results (9-15).

In the practical design, the FDNR parasitic zeros are less important in comparison with the Sallen-Key circuit; the RLC→RCD transformation of an odd order LP filter results in the load realized by the grounded capacitor (see *Fig. 8.8*). This capacitor ensures high attenuation up to high frequencies.

tel-00417838, version 1 - 17 Sep 2009



a) *b*)

FIG. 9.11: *a) the frequency response of the Fig. 9.9 FDNR low-pass filter for various output resistances and b) a comparison of the measured and the simulated frequency responses and the computed f_Z from Eq.(9-15) provided on the Fig. 9.9 FDNR low-pass filter (LM741)*

In both cases (the cascade and the ladder RCD designs), the stopband attenuation depends naturally from the order of transfer function and is a dB sum of particular transfers (for the cascade synthesis).

9.3.4 Causes of LP Stopband Degradation

In the two previous sections we have shown how the stopband characteristic of simple LP cascade sections is degraded by limited performances of the operational amplifier. In both cases, *the input and output of the filter were interconnected by a passive element causing the direct signal way*. The role of the OA in the LP filter is to "ground" the signal at higher frequencies by its low impedance output. This is obviously possible only in frequencies much below the f_T. *It follows from this that these LP sections (and many other standard ones) require the active element operating at high frequencies (in the stop-band), where the output voltage is to be close to zero*.

This can be viewed as a paradox because the zero output voltage in the stopband ought to be provided rather by a break in the signal way. In any case, the passive circuits allowing wideband attenuation are well-known; the simple passive RC circuit could be referred to as an instance..

In the cascade synthesis, the rules of the design providing high attenuation can be therefore defined as:

i) removal of the passive elements from the signal way at higher frequency and

ii) ensuring of the high suppression by the passive circuit containing ideally grounded capacitors.

As we have shown in the introduction, the roll-off slope for the low-pass filter is independent of the approximation. In the circuit designed on the basis of the previous two rules, the role of the active elements should be only to provide the pass-band transfer and the "resonance gain" at Ω_0. Above Ω_0, the suppression is to be ensured only by a passive circuit.

To show an example of this methodology, we can refer to the *Fig. 9.3* MFB biquad, where the input signal is naturally attenuated (in the wide frequency range above $\sim 1/R_1C_1$) by the grounded capacitor C_1. The classic *OTA-C* filters containing only grounded capacitors too reach very good stopband attenuation. However, many of these solutions may cause secondary negative effects. For instance, the linearity of OTA transconductance is generally not sufficient for certain applications and the filter parameters may be temperature-dependent.

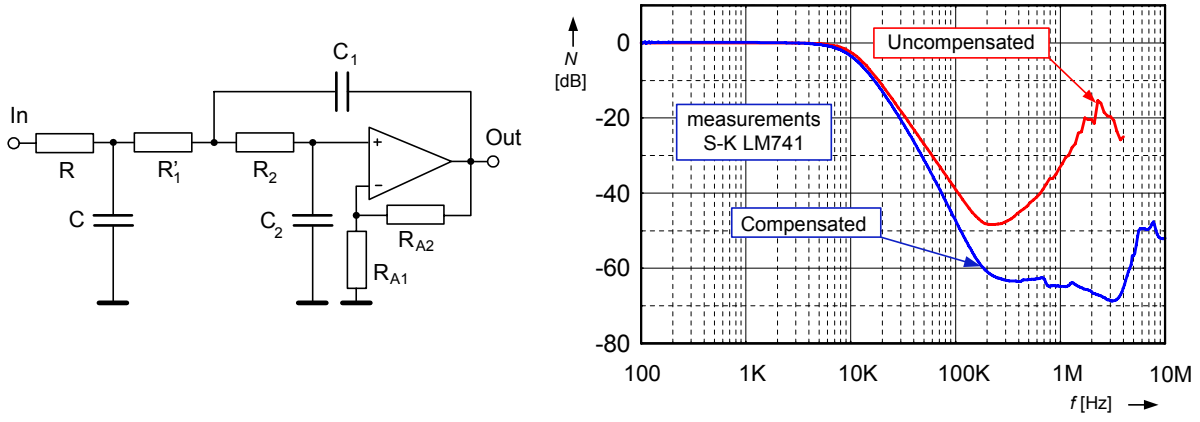
tel-00417838, version 1 - 17 Sep 2009

The fact that low attenuation in the stopband limits the frequency range of active filters can be seen, for instance, on the characteristic shown in *Fig. 9.21*. Here, a circuit which has not been optimized in this respect reaches only low attenuation (below 15dB). The circuits presented in the following text will show an approach which allows us to enhance the frequency range of cascade active filters by increasing the stop band rejection.

9.4 Type II Sallen-Key with Improved Stopband Rejection

One of the solutions increasing the suppression in the stopband consists in adding one supplementary pole provided by a passive RC network. We have shown that the *S-K* low-pass filter has a triple parasitic zero (see *Eq.*(9-13)). As shown in *Fig. 9.6,* one supplementary pole then results in the constant slope of 0 dB/dec above the f_Z frequency. The time constant of the RC network can be determined by using *Eq*. (9-13) or by applying an empirical simulation as shown in [134]. An example of such compensation is shown in *Fig. 9.12*. The measured characteristic with a supplementary RC bridge shows the expected 0 dB/dec slope, which remains constant for more than one decade. It is evident that such compensation causes a shift of Ω_0 and Q_0. In this case, the resulting transfer function is no longer of the 2nd order. It should be therefore convenient to build the design directly on the section of the 3rd order as shown in [130], [131].

However, it could be somewhat more interesting to remove the parasitic zeros or to move the f_Z to higher frequencies, rather than to provide a compensation of parasitic zeros



a) *b)*

FIG. 9.12: *a) Compensated (3rd ord.) Sallen – Key network [130], b) the measured frequency response of the compensated (Fig. 9.12 a) and uncompensated Fig. 9.7 a) SK*

A considerable zero-frequency shift can be done by cancelling the direct signal way *via* capacitor C_1. As shown in *Fig. 9.13*, the feedback capacitor C_1 "short-circuits" the amplifier output with the R_1-R_2 node. It follows from this that the OA output has to absorb the current i_{c1} in the wide frequency bandwidth, ideally up to infinity.

tel-00417838, version 1 - 17 Sep 2009

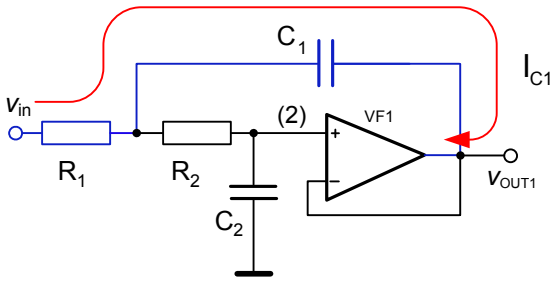


FIG. 9.13: *The direct current way causing the parasitic transfer zeros in the stopband characteristic of the S-K filter.*

Hence, as the voltage follower (*VF1*) ideally has unity voltage gain, the output voltage v_{OUT1} is identical with the voltage in node (2). In this node, the direct transfer *via* C_1 is cancelled by the reverse transfer of voltage follower *VF1,* which is ideally zero. We can therefore expect higher attenuation at this node. In the frequency range where the OA performance is impaired, the attenuation achieved by the passive 1st order R_1, R_2, C_2 circuit has a monotonous -20dB/dec attenuation slope. This is an important improvement in comparison with the v_{out1} output.

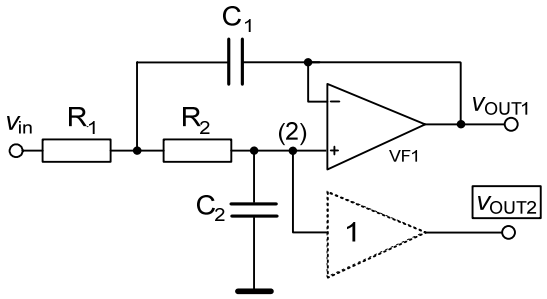


FIG. 9.14: *The Sallen Key low-pass biquadratic section with standard low impedance output v_{OUT1} [120] and high impedance node (2) buffered as (v_{OUT2}): Type II Sallen-Key.*

This hypothesis can be confirmed by a deeper analysis of the transfer applying model (9-8) of the operational amplifier. The analysis results in the transfer characterized by the 3rd order denominator and 2nd order numerator polynoms. The nominator term has the following form:

$$\boldsymbol{B}(s) = R_{OUT}C_1s^2 + (1 + R_{OUT}C_1\omega_p)s + \omega_p(A_0 + 1) \tag{9-16}$$

where the $\omega_p = 2\cdot\pi\cdot f_p$ is the dominant pole of the amplifier. The frequency f_Z of transfer zeros can be derived from polynom (9-16). The passive components affecting the f_Z are capacitor C_2 and output resistance R_{out}. We can write the new zero frequency of node (2) as:

$$f_{Z(2)} \cong \frac{1}{2\pi}\sqrt{\frac{A\cdot\omega_P}{C_1R_{OUT}}}, \tag{9-17}$$

which, compared to the *type I* Sallen-Key zero frequency given in *Eq.*(9-13), can attain a higher value; this higher value increases the attenuation. This is why the classic *S-K* circuit can be considerably improved at higher frequencies by adding a supplementary voltage follower, which ensures low impedance of the filter output.

tel-00417838, version 1 - 17 Sep 2009

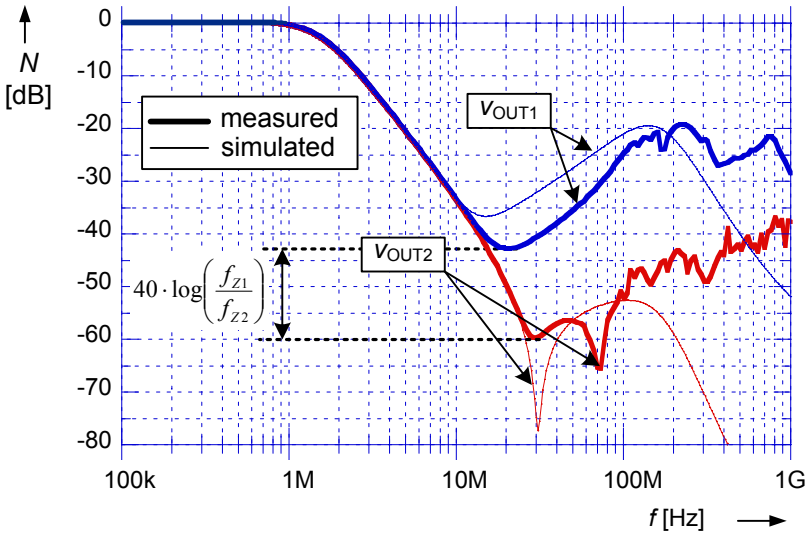


FIG .9.15: *The measured and the simulated AC characteristics of the Sallen-Key filter (Fig.9.14) for the standard Type I (v_{OUT1}) and Type II (v_{OUT2}) with increased suppression (R_1=168Ω, R_2=100Ω, C_1=1.2nF, C_2=560pF, OA=AD8055).*

In order to provide a comparison between the standard (v_{OUT1}) and the buffered *type II* (v_{OUT2}) Sallen-Key, a sample of F_0 = 1.5 MHz, Q_0 = 1/√2 low-pass section was realized. The simulated and measured results performed with a 300MHz OA (AD 8055) show an important pole shift and, therefore, an increase of the stopband suppression in the order of ~20dB (*Fig. 9.15*)

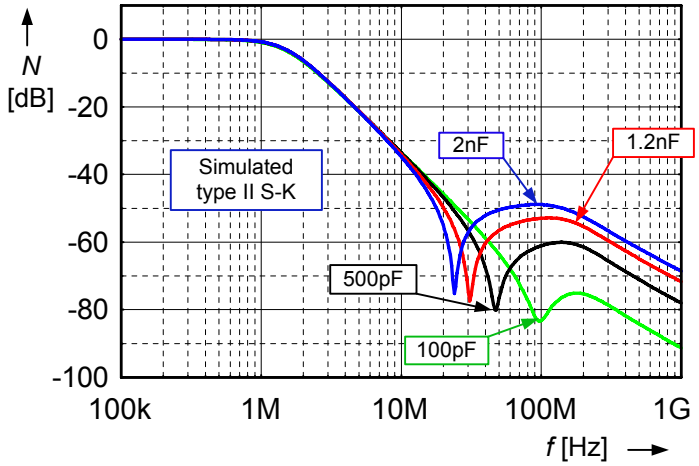
It is obvious that, for an *identical operational amplifier*, the presented *type II* Sallen-Key filter allows us to obtain higher attenuation in comparison with the *type I* S-K circuit. For instance, it can be shown that a 10 MHz *type I* Sallen-Key filter ($R_1 = R_2 = 112\ \Omega$, $C_1 = 200$ pF, $C_2 = 100$ pF) reaches only average attenuation of -20dB in the stopband, whereas for the *type II* S-K roughly 40 dB is achieved. This rate of attenuation is sufficient for the cascade synthesis (the result obtained with the AD8055 SPICE model).

In order to compare both *Type II* and *Type I Sallen-Key* LP filters, the measurements shown in *Fig. 9.15* were realized with identical values of passive components. Hence, *Eq.* (9-17) shows the dependency of $f_{Z(2)}$ only on C_1 capacitor, whose value can be arbitrary selected. The choice of the filter impedance level (through the value C_1) can be therefore used for the *further increase of the stopband attenuation*.

Fig. 9.16 shows the characteristics of the section of *type II S-K* designed for various impedance levels. We can see the shift of the $f_{Z(2)}$ zero frequency with the simultaneous decrease of the value of C_1, which conforms to *Eq.* (9-17). As a matter of fact, an excessive increase of impedance level may lead to the formation of secondary parasitic influences as discussed in *section 8.4.*

A handicap of this approach is that one additional voltage buffer is needed. However, the function of this voltage buffer is to create a new, low impedance voltage output. As the unity follower has to ensure the low impedance output primarily in the passband area (*i.e.* at relatively low frequencies), an amplifier with a relatively low value of f_T can be used. In some cases, we can even eliminate the voltage buffer by means of a direct connection between node (2) and a high impedance input which is joined immediately to the filter (for instance, a high impedance input of an A/D converter). Moreover, proper choice of a low DC offset voltage follower can improve the final DC offset of the *type II S-K* filter as the output of VF_1 is only AC-coupled.

tel-00417838, version 1 - 17 Sep 2009



a)

C_1 (nF)	C_2 (nF)	R_1=R_2 (Ω)	f_Z (MHz)
2.0	1.0	75	24.1
1.2	0.60	125	31.0
0.50	0.25	300	47.5
0.10	0.050	1.5k	95.1

b)

FIG. 9.16: *a) The simulation of F_0=1.5MHz Q=1/√2 Sallen-Key type II section for various impedance levels b) the components values. The simulation was performed with the AD 8055 model*

However, the Sallen-Key filter is not an optimal structure in respect of the stop-band rejection. As it is the most frequently used structure in the cascade synthesis, its optimization can be important in the practical filter design. However, other biquadratic sections based on the operational amplifier can also show a good stopband attenuation rate. For instance, the use of a single-amplifier FDNR with serial losses in LP configuration as described in *Fig. 9.9* (see [123], in the 1st figure (b)) exhibits a single parasitic zero. In the next section, we will present a structure based on the second generation current conveyor CCII which posses ideally no parasitic zero in the stopband area.

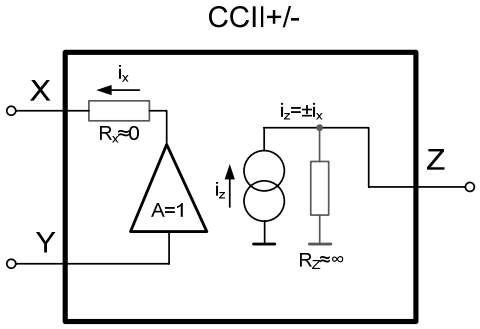
9.5 Current Mode CCII Section Without Parasitic Zero

A biquadratic structure containing no parasitic zero in the transfer attains ideally the -40dB/dec constant roll-off slope, which is limited only by parasitic leakage of the signal. The constantly decreasing AC transfer of -40dB/decade can be ensured by a 2nd order passive RC filter. However, the conventional RC 2nd order LP filters can only be designed for a quality factor lower than $Q_0 < 0.5$. Therefore, an ideal solution would be to split the frequency bandwidth into two regions. These regions encompass a lower frequency area, where the resonance gain is provided by an active element, and a higher frequency area (stopband), where, the suppression should be ensured by a passive 2nd order RC bridge containing grounded capacitors.

There are many methods applied in the design of biquadratic sections (see *chapter 9.1*). The design of filters based on a single active device (SAB) usually utilizes a generalized T-bridge. An example of the application of this technique is shown in [100]. The approach utilizing the biquadratic sections that use a single *Current Conveyor CC* has been presented in [124]. The "rules" defined in *section 9.4.3* - together with the techniques presented in [100] - can facilitate the design of a CC-based biquadratic section characterized by high attenuation in the stop-band.

The presented network includes a second generation current conveyor CCII- (*Fig. 9.17 a*) containing three terminals: a low impedance voltage output **X**, a high impedance voltage input **Y**, and a current output **Z**. The transfers between these terminals are defined as: $V_X = V_Y$, $I_Z = -I_X$ and $I_Y = 0$ [126] (more details about CCII are provided in *chapter 10*).

tel-00417838, version 1 - 17 Sep 2009



$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_y \\ i_z \\ v_z \end{bmatrix}$$

FIG. 9.17: *a) The internal structure of CCII± with parasitic R_x and R_z resistance, b) the matrix form of the transfer function*

The biquadratic section containing two grounded capacitors together with input and feedback resistors is depicted in *Fig. 9.18*. The input signal is connected to the low impedance input *via* resistor R_1 and coupled with the current output terminal **Z** according to the relation $I_Z = -I_X$. The current source is loaded by the π-bridge C_1, R_2, C_2. The transfer of such circuit reaches ideally the slope of -40dB/dec in the whole stopband area.

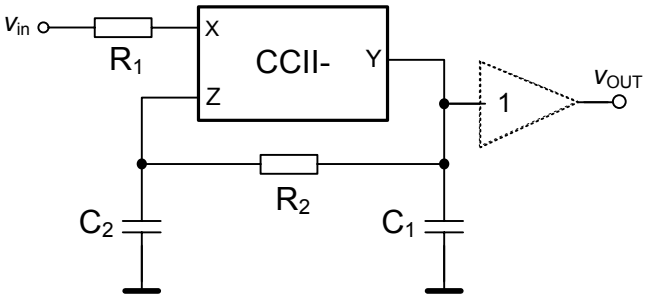


FIG.9.18: *The CCII- low-pass biquadratic section with no parasitic transfer zero in the stopband*

By means of an analysis performed with the ideal CCII- model (*Fig. 9.17*), the cut-off frequency and quality factor can be obtained in the following form:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}, \quad Q = \frac{\sqrt{R_2}}{\sqrt{R_1}} \cdot \frac{\sqrt{C_1 C_2}}{C_1 + C_2} = \frac{1}{2} \cdot \sqrt{\frac{R_2}{R_1}}\bigg|_{C1=C2}. \tag{9-18}$$

Contrary to the *type I* and *type II S-K* (*Fig. 9.14*), this circuit has *ideally no direct signal path between input v_{IN} and output v_{OUT}* terminals. A potential direct signal path is interrupted here by a low (ideally zero) reverse transfer of the voltage buffer between terminals **X** and **Y**. The attenuation above cut-off frequency F_0 is ensured by the above-mentioned passive network containing shunt capacitors. For this reason, terminal **Y** (located at the output of RC network) has been chosen as the filter output.

In order to analyze the attenuation in the stopband, we have to use a complex model of a current conveyor which includes the frequency-limited transfer **X**→**Y** , the non-zero voltage buffer (**X**) output impedance, the frequency-limited $I_X \rightarrow I_Z$ transfer, and other properties. The mathematical analysis and numeric simulation of this type of network show that the decreasing voltage and current transfer as well as the final R_{out} value of terminal **X** have no negative impact on the stop band attenuation.

For convenience, we provide here the result obtained by means of a simplified analysis. In this analysis, only the main imperfection of the conventional CCII is included, namely the frequency-limited transfer **X**→**Y** and the non-zero value R_X of terminal **X**. For this analysis, the voltage buffer is

tel-00417838, version 1 - 17 Sep 2009

realized by an operational amplifier characterized by the single pole model shown in *Fig. 9.5*. The analysis of the v_{out}/v_{in} frequency transfer results in the following expression:

$$H(s) = \frac{\Omega_0^2}{\left(s^2 + s\cdot\Omega_0/Q_0 + \Omega_0^2\right)} \cdot \frac{\left(\omega_P \cdot A_0 + s\right)}{\left(\omega_P \cdot (1+\alpha)\cdot A_0 + s\right)}, \qquad (9\text{-}19)$$

where $s^2 + s\cdot\Omega_0/Q + \Omega_0^2$ is the standard 2nd order polynom with parameters Ω_0 and Q_0 given by *Eq.*(9-18). Parameter α is defined as $\alpha = R_{OUT}/R_2 << 1$. This voltage transfer contains, in fact, one nominator zero which is eliminated by the denominator pole. The theoretical -40dB/dec roll-off slope in the stopband is practically limited only by the parasitic signal leakage (the input--output crosstalk).

Other parasitic parameters of CCII can be analyzed in the same way or by means of a simulation using the complex model. As we will show later, these simulations also result in the almost constant -40dB/dec roll-off slope in a large frequency bandwidth. The limitation caused by the above-mentioned crosstalk is primarily due to the parasitic input-output capacity $C_{X\text{-}Y}$.

In order to verify the performance of the circuit, an example of a 10MHz 4th order Butterworth low-pass filter was realized using the current conveyor based on the CCII-K network [127] (*Fig. 9.20*). The CCII-K allowed the current conveyor to be realized with discrete, commercially available components (the integrated version in 0.35 µm CMOS will be presented in the following chapter). The characteristic obtained by the measurements performed on the fabricated filter shows a *very good rate of suppression reaching up to 100 dB* (the 4th order filter). Such suppression on MHz frequencies is usually proper only to passive RLC filters. Note: Although the circuit is based on two active elements (the CCII and the unity follower), it still belongs to the SAB circuits.

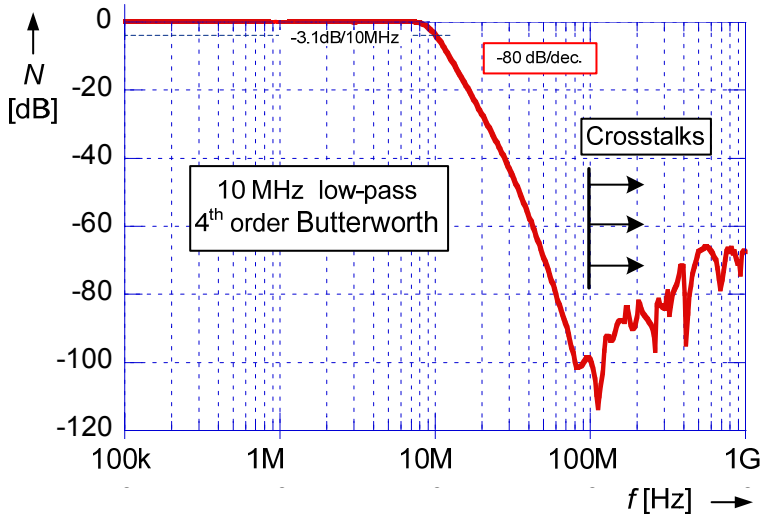


FIG. 9.19: *An example of measured AC response of the 10 MHz 4th order low-pass filter realized by means of the CCII-K circuit, Fig. 9.20 (OPA860+AD8055)*

The circuit in *Fig. 9.18* contains, in reality, other parasitic elements not included in the analysis. One of the most important elements is the above-mentioned non-zero overlap capacity $C_{X\text{-}Z}$, which causes a reverse voltage transfer **X**→**Z**. The influence of this capacity can be demonstrated by the simulation with final quality-factor capacitors C_1 and C_2 (a serial R_Q model). The influence of $C_{X\text{-}Z}$ can be important for a low value of $Q_{(C1,C2)}$. Other parasitic effects may arise from, for instance, ground loops or parasitic transmission through power supply lines. Naturally, good performances can only be achieved by a proper design of the PCB respecting the general rules of RF design.

tel-00417838, version 1 - 17 Sep 2009

In order to show the importance of isolation between the direct signal way (provided by the "zero" reverse transfer between the **X** and **Y** terminals), we can use the concept of RCD low-pass filter shown in *Fig. 9.9.* In [123], a lossy FDNR one-port network described in *Fig. 9.21 a*) was presented. In this study, the limitation caused by the finite frequency bandwidth of the FDNR has been shown. The FDNR impedance $1/s^2D$ of *Fig. 9.21 a*) arises in the node **X** of the CC.

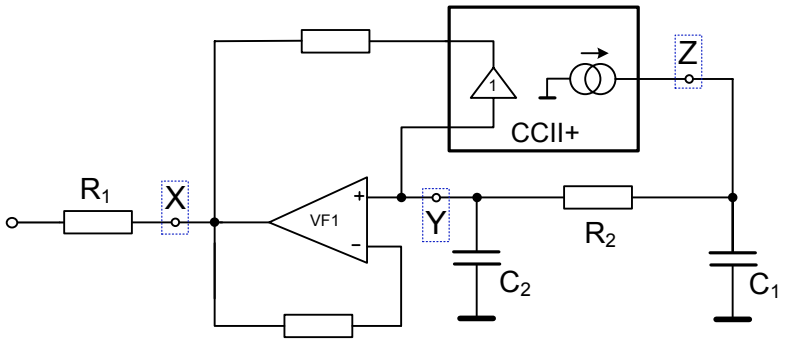
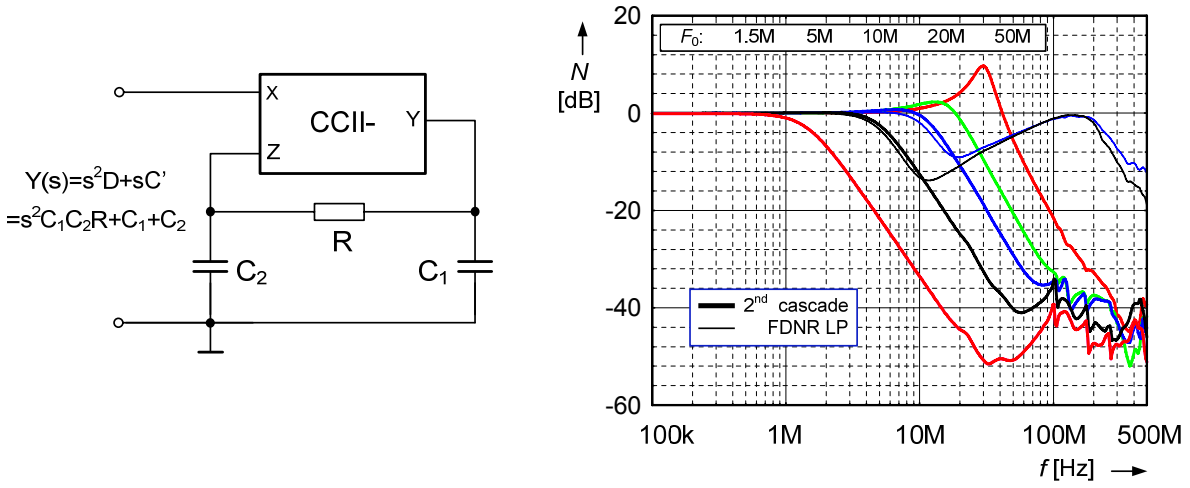


FIG. 9.20: *The realization of an inverting CCII- employing the CCII-K [127] circuit (CCII+ OPA 860, OA AD 8055)*

In this type of filter we can expect certain difference between the stopband attenuation achieved in the **X** and **Y** nodes; voltage transfer in these nodes has to be ideally equal. In order to show this difference, the voltage transfer was measured in both node **X** (output of the RCD LP filter) and node **Y** (output of the filter from *Fig. 9.18*). The measurements were performed using the CCII-K circuit shown in *Fig. 9.20,* and the resulting characteristics are plotted for various cut-off frequencies (Q_0=1/√2) in *Fig. 9.21.* Here, the difference in the stopband characteristic can be evaluated for two cut-off frequencies: F_0 = 5 and 10 MHz.



a) *b*)

FIG.9.21: *A comparison of the CCII biquadratic section from Fig. 9.18 and the lossy FDNR section a) The CC realization of the FDNR [123] and b) the resulting voltage transfer for various F_0 frequencies.*

In the characteristics shown in *Fig. 9.21 b),* an increasing voltage transfer at resonant frequency can be observed; this increase becomes more significant at higher frequencies. The last characteristic with resonance peak at 30 MHz was designed for F_0 = 50 MHz. In comparison with instances of significant shift of Ω_0 and Q_0, the *transfers of the stopband remain unaffected and are independent of* F_0.

tel-00417838, version 1 - 17 Sep 2009

Both realizations (the cascade and the FDNR) were used in higher order filters. *Fig. 9.22* shows a 10 MHz low-pass filter realized as a 5th order cascade filter (*a*) and a 5th order RCD simulation of a lossy-ladder RLC (*b*). The RCD design was based on the Button transformation of lossy-ladder RLC prototypes [104]. The model of the CCII used for the simulation is the MOS transistor level CCII- current conveyor developed in the next chapter (*Fig. 10.6*). The simulations show very good high frequency properties of the cascade filter, whereas the attenuation of the RCD filter corresponds to the conclusions described in [123].

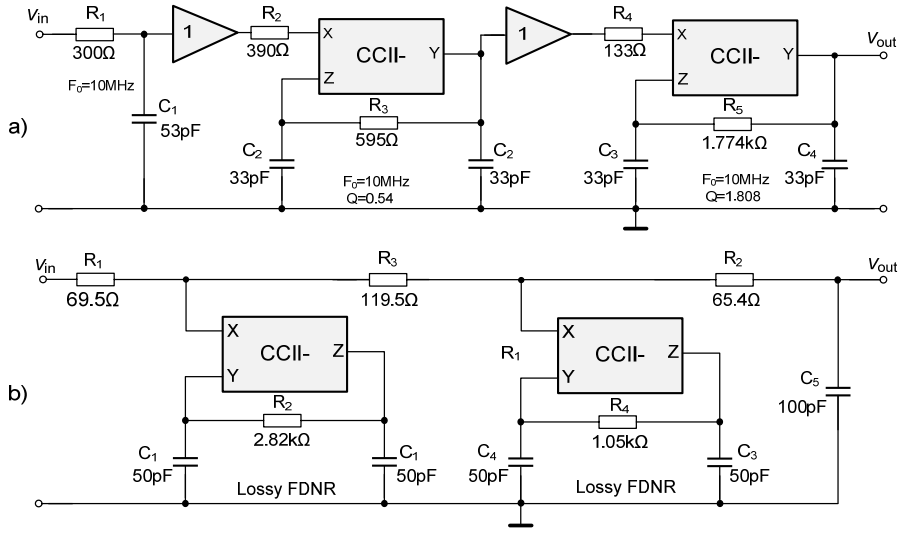


FIG. 9.22: *A low- pass 5th order 10MHz Butterworth filter designed as a) a cascade realization using the biquadratic sections from Fig.9.18 and b) the FDNR simulation of the lossy RLC*

A structure similar to the one shown in *Fig. 9.21 a)* (designed for $F_0 = 1.5$ MHz) has been also realized using a second generation current conveyor integrated in CMOS 0.35 µm. The results will be shown in the following chapter (see *Fig. 10.14*).

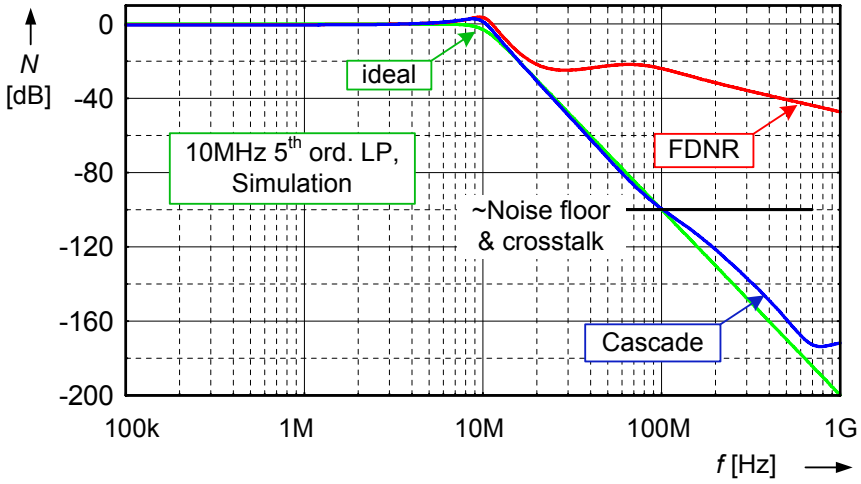


FIG. 9.23: *Simulated characteristics of the LP frequency filters shown in Fig. 9.21. (Simulated with a transistor-level CCII, Fig. 10.6)*

Similarly as in the previously presented *type II* Sallen-Key filter, an additional voltage buffer is used. The voltage buffer has to provide low impedance primarily in the pass-band area (*i.e.* at relatively low frequencies), and therefore a low f_T (low power consumption and low cost) operational amplifier can be used.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

10 DESIGN OF CMOS SECOND GENERATION CCII-

10.1 Current Conveyor

The current conveyor (CC) is a versatile three-terminal electronic device which enables the realization of various functions in the design of electronic circuits. The most important field of application is in the *current-mode* analog signal processing [135], [136]. In contrast with the voltage mode approach, the current-mode signal processing uses the currents as a state variable. This approach often offers improved performances as compared with operational amplifier-based circuits; the improvement is measurable in terms of, for example, bandwidth or facility of integration..

As a matter of fact, several generations of CC are recognized, and among these the most important ones are the first and the second generation current conveyors: the CCI and CCII [135], [136], [138]. In the following sections, the design and integration will be presented of a high performance *second generation inverting current conveyor CCII-* in a regular 0.35 μm CMOS process (AMS).

The main motivation and aims behind the design and integration of the current conveyor are expressed in the following points:

1) **The aim to validate the new CCII-based LP biquadratic section** (*chapter 9.5*). This biquadratic section with *high stopband attenuation* is based on the division of frequency bandwidth between the active element, which provides the resonance gain at cut-off frequency, and the passive RC network, which facilitates the maintenance of high attenuation *up to very high frequencies*. The necessity of the development mainly results from the fact that a discrete version of the CCII- is not commercially available. In order to demonstrate the good high-frequency performance of the biquadratic section, we aim the cut-off frequencies of filters in units of MHz. Such cut-off frequencies are relatively difficult to achieve with standard CMOS operational amplifiers.

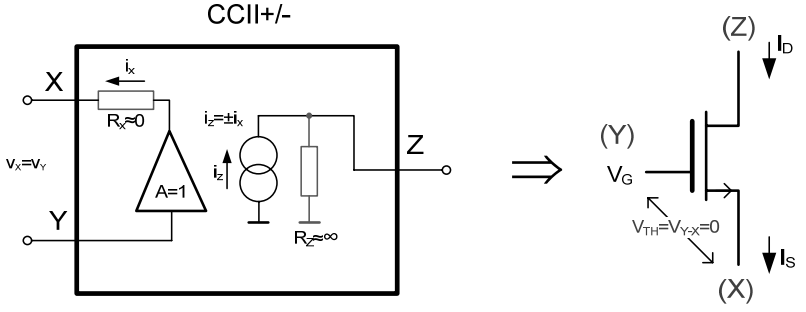


FIG. 10.1: *a) The structure of CCII± with parasitic R_X and R_Z resistance, the equivalence of CCII- with an ideal transistor MOS*

2) **The aim to design a universal high-performance CCII device.** The analysis presented in the previous chapter has shown the importance of low resistance r_{out} of the voltage output in the design of active frequency filters. A very low (and frequency-independent) value of r_{out} (= r_x) can improve the properties and frequency range of ordinary CCII-based circuits.

This chapter presents an introduction of the basic principle and structure used in the integration of CCII. In *sections 10.2* and *10.3*, the design of the current conveyor in CMOS is described. Here, low impedance of the output buffer is investigated as a principal objective of the design. In the last part, the layout and integration of the circuit are presented. The performances are verified by measurement of the circuit fabricated in CMOS 0.35 µm. An example of the 1.5 MHz low pass-filter with high attenuation in the stopband is presented at the end of the chapter.

10.1.1 The Second Generation Current Conveyor

The second generation current conveyor is a three-terminal device with *low impedance voltage output* **X**, *high impedance voltage input* **Y**, and *high impedance current output* **Z**. The different facets of the relationship between the terminals are given by the following transfer matrix:

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \cdot \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix}, \tag{10-1}$$

where the polarity of the output current i_z results in a different notation CCII+/-. The structure of CCII is illustrated in *Fig. 10.1*, where one controlled source and one voltage follower are used. In this figure, a similarity between the CCII and an ideal transistor MOS can be observed. This similarity is expressed by the zero V_{TH} voltage and zero channel conductance of the transistor (*i.e.* $g_{DS} = 0$).

In *Fig. 10.1*, the zero voltage V_{TH} is provided by a unity gain follower connected between terminals **X** and **Y**. The transfer of current is realised between the voltage output terminal **X**, from which the output current I_X is *conveyed* to the output terminal **Z**.

Due to the similarity with a simple transistor, the CCII is frequently referred to as a diamond transistor or transconductor.

10.1.2 The Basic Structure of the Current Conveyor

The approaches used in the design of current conveyors are generally based on the realisation of controlled sources as shown in *Fig. 10.2* [137]. In this figure, a unity gain voltage follower can be identified. The current transfer $I_X \rightarrow I_Z$ is provided by the *sensing of bias currents* I_{B+} and I_{B-}. The output current I_Z results from the difference between the positive and the negative bias currents and can be delivered by applying the *KCL* as:

$$I_Z = -I_X = I_{B-} - I_{B+} \tag{10-2}$$

In *Fig. 10.2*, the unity gain follower is realised by an operational amplifier. This operational amplifier is biased by a first pair of current mirrors sensing the currents I_{B+} and I_{B-}. These currents then merge onto the output node **Z**. In the case of the circuit illustrated by *Fig. 10.2*, the inverting type CCII- is realised. Opposite polarity (CCII+) can be obtained by means of eliminating the second pair of current mirrors.

tel-00417838, version 1 - 17 Sep 2009

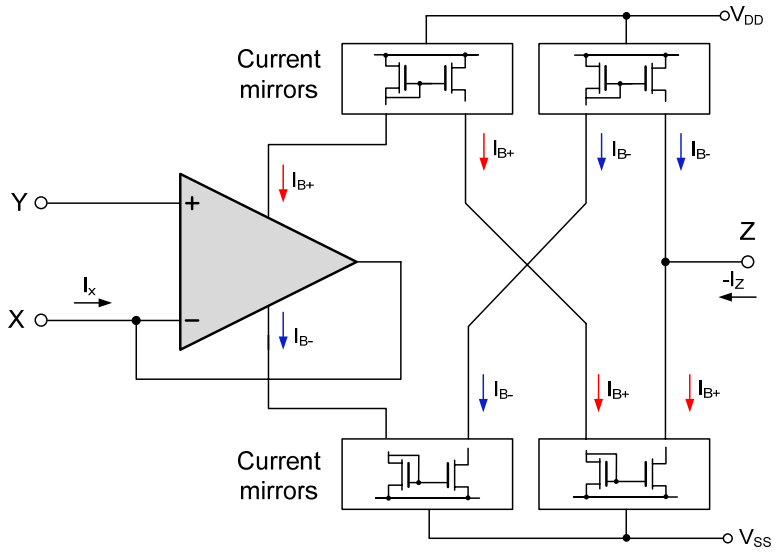


FIG. 10.2: *The structure of CCII- using the sensing of supply bias currents [137]*

10.1.3 Real Properties of CCII

The practical use of the current conveyor is affected, similarly as the use of the operational amplifier, by a limited frequency range and DC errors. The most important parameters for high frequency applications are the AC voltage transfer $V_X \rightarrow V_Y$ and output resistance R_X of the voltage buffer. As a matter of fact, the two parameters are dependent on each other (*e.g.* an increase of the cut-off frequency of transfer $V_X \rightarrow V_Y$ leads to lower output resistance at higher frequencies).Therefore, the output resistance $R_X(f)$ will be further considered as the most important parameter related to the high frequency performances of the voltage follower.

Generally, the appearance of output resistance R_Z in node **Z** (*Fig. 10.1*) is considered as a main DC imperfection of the CC. However, the influence of this parameter depends on the application. The final impedance of node **Z** can be related to the absolute current transfer $I_X \rightarrow I_Z$. This impedance can derive an important part of the current I_Z and violate the condition $I_X = -I_Z$. Moreover, this effect can be accentuated at higher frequencies, where the impedance is affected by the parasitic capacity C_Z. Considering the low-pass biquadratic section described in *Fig. 9.18*, the current node **Z** is loaded by a shunt capacitor C_2 which value is supposed to be much higher than the parasitic capacity C_Z. It follows from this that the final output resistance can affect only the required DC transfer of the filter.

Contrary to this, the limited frequency range and the final output impedance of the voltage buffer can affect the values Ω_0 and Q of the filter. This is in accordance with *Eq.*(9-18), where the non-zero resistance of voltage buffer $R_X(f)$ is serially connected with R_1 (*Fig. 9.18*) (*i.e.* enters in the equations of Ω_0 and Q). An example of such effect can be seen in the measured characteristics given in *Fig.9.21*.

In the following text we will focus on the design of the low output impedance voltage follower as a critical part of CCII.

10.2 CMOS Realisation of the CCII-

The design of the second generation current conveyors can be realized in many different ways [143]. As we have pointed out in the above-stated sections, our attention is focused on the very low impedance of the output buffer r_x (= r_{out}). In addition, we require a high driving capacity of both **X** and **Z** output terminals.

tel-00417838, version 1 - 17 Sep 2009

In the design of active frequency filters, a *low value of output impedance* is related to the impedances of passive elements of the filter which are taken at the frequencies of interest (*e.g.* at Ω_0 or the frequency region of the stopband). In our design, output resistance R_X is expected in the order of ohms from DC up to several MHz.

The design of the low output resistance voltage buffer can utilize many special approaches. Generally, terms can be found that describe the output impedance as a difference of transconductances or that result from the use of feedback (*e.g.* [142], [143], [144], [145]). As an interesting and typical example, a circuit based on the subtraction of transconductances is shown in the design of a *universal voltage conveyor* (UVC) [12]. The voltage buffer utilizes four OTAs. However, it can be shown (by means of simulation) that a critical point of this structure [145] is the *complexity of the circuit*. The use of four (*i.e.* Miller) OTAs produces complicated CMOS circuits, which contain many parasitic capacitances limiting the frequency bandwidth.

In order to reduce these parasitic capacitances, a circuit using only a few transistors will be used in the following design. The parameters of this circuit will be optimized by a mathematical analysis and computer simulations.

10.2.1 The Low Impedance Voltage Buffer

The circuits of CMOS unity gain followers are widely discussed in related sources. The above-defined electrical specifications lead to the choice of voltage follower, which has been derived from the design of "a fully differential voltage buffer [91]". The circuit adapted for use in the CCII is described in *Fig. 10.3*.

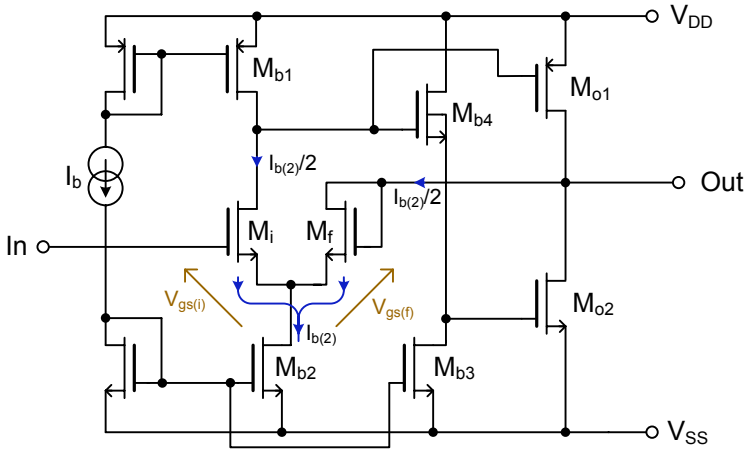


FIG. 10.3: *The unity gain voltage follower.*

The main feature of the circuit in *Fig. 10.3* is a zero DC offset of the output voltage, *e.g.* $V_{in}=V_{out}$. This feature relies on *accurately matched transistors*, namely the input transistor M_i and the feedback transistor M_f. Both the transistors are biased by *constant currents* of values $I_{b(2)}/2$ (see *Fig. 10.3*). The gate of M_i is the input (In) and the gate of diode-connected transistor M_f is connected to the output of the buffer (Out). In order to provide the accurate transfer $V_{in}=V_{out}$, the bias currents have to be set to:

$$I_{D(Mi)} = I_{D(Mf)} = \frac{1}{2} I_{B(Mb2)} . \qquad (10\text{-}3)$$

The open loop amplification of the circuit shown in *Fig. 10.3* is realised in the high impedance node (D) of M_i. Additional amplification is achieved by the output common source amplifiers M_{o1} and M_{o2}. Transistor M_{b4} is important for the biasing of M_{o2} *via* the value $V_{GS(Mb3)}$. Transistor M_f provides the

tel-00417838, version 1 - 17 Sep 2009

feedback, ensuring the *unity voltage gain and zero DC offset of the* voltage follower. In the original design [91], the output resistance r_{out} was not investigated as an important parameter.

Fig. 10.4 shows a simplified linearized model of the voltage buffer shown in *Fig. 10.3*, containing the M_i and M_f input and feedback transistors (*i.e.* represented by g_{mi} and g_{mf}), and the output transistors M_{o1} and M_{o2} (both substituted by g_{mo}). In this model, two important parasitic parameters were also included, namely resistances r_1 and r_2 resulting from the channel length modulation of transistors M_{b1} and M_{b2}.

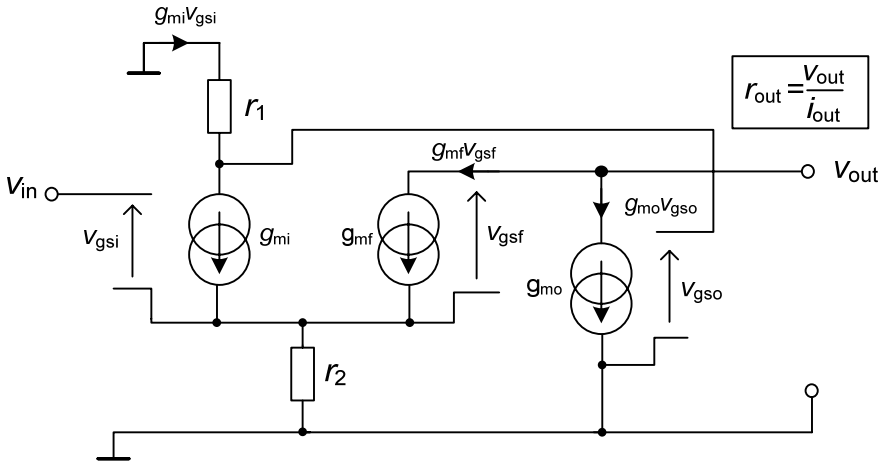


FIG. 10.4: *A simplified small signal model of the unity voltage follower from Fig. 10.3 (we consider $g_{mo} = g_{mo1} + g_{mo2}$)*

Voltage transfer of the circuit from *Fig. 10.4* can be determined from the nodal equations. This transfer G_0 can be expressed as a function of transconductances and resistances r_1 and r_2,

$$G_0 = \frac{v_{out}}{v_{in}} = \frac{g_{mi} \cdot g_{mf} \cdot r_2 + g_{mo} \cdot g_{mf} \cdot g_{mi} \cdot r_1 \cdot r_2 + g_{mo} \cdot g_{mi} \cdot r_1}{g_{mi} \cdot g_{mf} \cdot r_2 + g_{mf} + g_{mi} \cdot g_{mf} \cdot g_{mo} \cdot r_1 \cdot r_2}, \tag{10-4}$$

which can be simplified by assuming identical (matched) transistors M_i and M_f as well as matched bias current sources M_{b1} and M_b (*i.e.* $r_1 = r_2$):

$$G_0 = \frac{g_{mi}}{g_{mf}} \cdot \frac{g_{mf} \cdot r_{22} + g_{mo} \cdot r_1 + g_{mf} \cdot g_{mo} \cdot r_1 \cdot r}{1 + g_{mi} \cdot r_2 + g_{mi} \cdot g_{mo} \cdot r_1 \cdot r_2}\Bigg|_{\substack{g_{mi}=g_{mf} \\ r_1=r_2 \approx \infty}} \approx 1. \tag{10-5}$$

As noted in this *Eq.*(10-5), voltage transfer G_0 is very close to desired value – *unity* (see an example of simulation in *Fig. 5.29, chapter 5*). However, the analytical results (10-5) match for the infinite load resistance only. To evaluate the driving capacity of the voltage buffer, the output resistance can be deduced as v_{out}/i_{out}. This can be calculated for identical $g_{mi} = g_{mf} = g_m$ and the grounded input as:

$$r_{out} = \frac{v_{out}}{i_{out}} = \frac{2 \cdot r_2 + 1}{r_2 \cdot g_{mf} + r_1 \cdot r_2 \cdot g_{mo} \cdot g_m + g_m} \approx \frac{2}{r_1 \cdot g_{mo} \cdot g_m} \Rightarrow 0, \tag{10-6}$$

Here, a method allowing the optimization of output resistance r_{out} *via* the values of r_1, g_{mo} and g_m can be seen.

The frequency bandwidth of the voltage buffer from *Fig.10.3* is determined by the high impedance node at the drain of M_i. Here, capacitance *C*' contributes to the dominant time constant, which is determined primarily by C_{GS} of M_{o1} (see *chapter 2.4.1*). A frequency dependence of the output impedance $Z_{out}(j\omega)$ can be obtained from the previously derived DC output resistance (10-6) by replacing r_1 with a new impedance z_1:

tel-00417838, version 1 - 17 Sep 2009

$$z_1 \rightarrow \left(\frac{1}{r_1} + j\omega C' \right)^{-1} . \tag{10-7}$$

This substitution allows us to compute the zero frequency ω_z of the output impedance $Z_{out}(j\omega)$:

$$\omega_z = \frac{1}{r_1 \cdot C'} . \tag{10-8}$$

It is evident that, in order to achieve a high bandwidth, a low value of *C'* is required. Moreover, when using the feedback, frequency *compensation* may be required in order to eliminate oscillations (see *chapter 4*). In the case of *Fig. 5.13*, the stability of voltage buffer was evaluated by simulation. This simulation has results in an optimal value of *C'*, determined by the $_1$ channel dimension ($W{\cdot}L$) of M_{o1}.

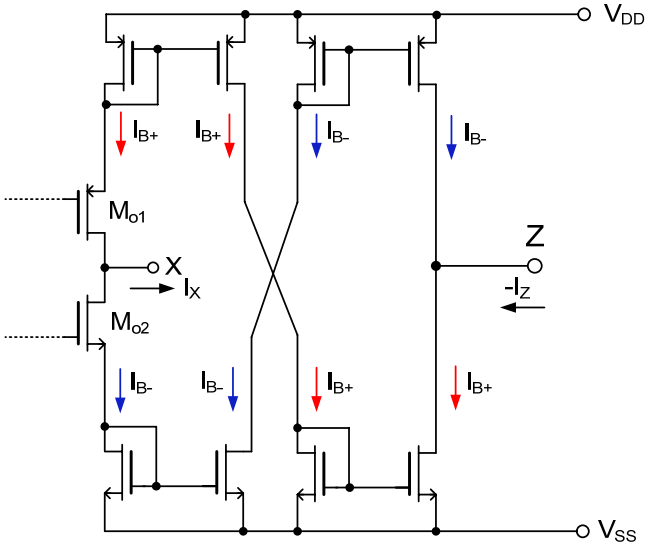


FIG. 10.5: *Implementation of current sensing applied to the voltage buffer shown in Fig. 10.3*

The dependence of output resistance r_{out} and transconductance g_{mo} was expressed by *Eq.*(10-6). As we can see in *Fig. 10.3*, the operating point of M_{o1} and M_{o2} (and thus the value g_{mo}) results from the V_{GS} voltage of M_{b4}. This voltage can be controlled by the size of the transistor $(W/L)_{b4}$ or the bias current I_D (drain current of M_{b3}). However, the operating point also results from process parameters *KP* and V_{TH} (the output transistors are *self-biased*). Consequently, the drain currents of M_{o1} and M_{o2} have to be carefully verified (*e.g.* by a corner analysis) in order to eliminate unexpected excessive consummation and to reach low output resistance.

10.2.2 CCII- CMOS Current Conveyor

The unity gain voltage follower shown in *Fig. 10.3* can be used in the concept of CCII shown in *Fig. 10.2*. The previously described technique of current sensing, which is applied to the V_{DD} and V_{SS} terminals, is depicted in *Fig. 10.5*. This current sensing can provide an accurate current transfer between terminals **X** and **Z**. However, we can expect a reduced maximal peak-to-peak voltage of terminal **X**. This is due to the use of two transistors, which are serially connected between the output transistors M_{o1} and M_{o2} and supply voltage terminals (causing a voltage drop $2{\times}V_{GS}$).

The cascading of the transistors can be avoided by sensing the gate driving voltage V_{GS} of M_{o1} and M_{o2}, accomplished by two supplementary transistors. This sensing of the V_{GS} voltage was used in the design of the conveyor, where a high peak-to-peak output voltage V_X is obtained. *Fig. 10.6* shows the CCII- containing the voltage buffer presented in *chapter 10.2.1*, biased by a floating current source I_b. The transfer $I_X \rightarrow I_Z$ is provided by four transistors $M_{m1} - M_{m4}$. It is evident that, to obtain the accurate

tel-00417838, version 1 - 17 Sep 2009

current transfer, the transistors of the output buffer and the transistor measuring their V_{GS} need to have an identical dimensions (*i.e.* $(W/L)_{Mo1}=(W/L)_{Mm1}$ and $(W/L)_{Mo2}=(W/L)_{Mm2}$ – see transistor dimensions in *Tab. 10.1*)

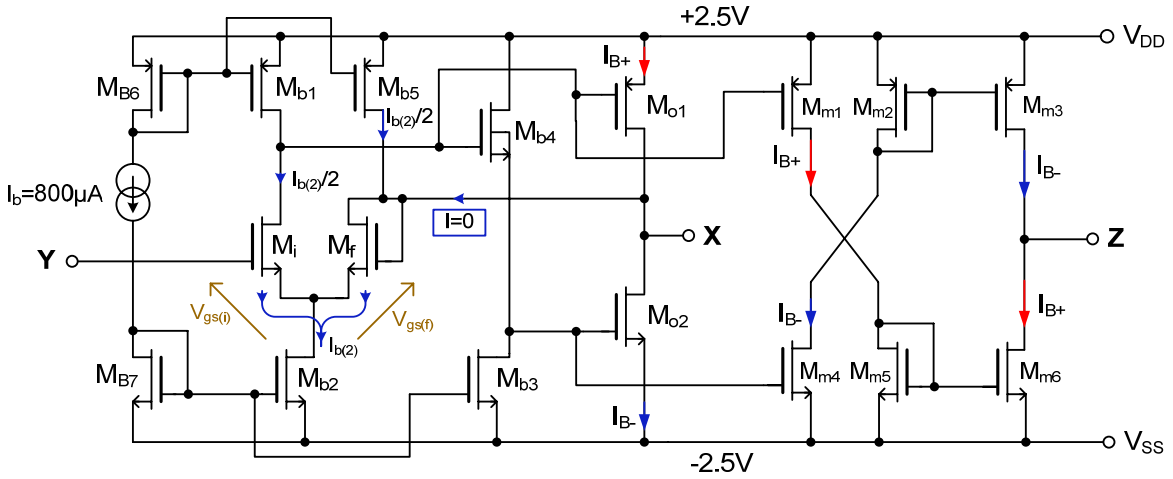


FIG. 10.6: *Integrated CMOS CCII-. The transistor sizes and operating points are listed in Tab. 10.1*

By inspecting the circuit in *Fig. 10.3* we can observe a difference between the drain currents of M_{o1} and M_{o2}. This difference is due to the constant bias current $I_{b(2)}/2$ passing through the feedback transistor M_f. However, *Eq.*(10-2) requires the steady state current to be equal for both output transistors (*i.e.* $I_{B+}=I_{B-}$ for $I_X=0$). The condition $I_{B-}=I_{B+}$ can be achieved by an additional current source realised by transistor M_{b5}, as shown in *Fig. 10.6*. In this way, the gate of the feedback transistor M_f becomes a high impedance input, and no additional current is added to I_{B+}.

TAB. 10.1: TRANSISTOR SIZING AND DETAILED OPERATING POINTS FOR CCII- IN FIG. 10.7

NAME	M_i	M_f	M_{b1}	M_{b2}	M_{b5}	M_{o1}	M_{o2}	M_{b3}	M_{b4}
Size/type	N:800/1 µ	N:800/1µ	P:400/5 µ	N:401/5µ	P:400/5µ	P:400/2µ	N:1000/3µ	N:400/5µ	N:100/1µ
I_D	401u	400u	-401u	802u	-403u	-2,32m	2,33m	800u	800u
V_{GS}	1,39	1,39	-1,68	1,28	-1,68	-2,06	1,19	1,28	1,74
V_{DS}	1,83	1,39	-2,06	1,11	-2,5	-2,5	2,5	1,19	3,81
V_{BS}	-1,11	-1,11	0	0	0	0	0	0	-1,19
V_{TH}	1,33	1,33	-1,02	769m	-1,02	-1,04	781m	769m	1,35
V_{DSAT}	86,7m	86,6m	-515m	317m	-515m	-800m	262m	317m	286m
g_M	6,32m	6,31m	1,17m	2,96m	1,17m	4,24m	10,5m	2,95m	3,61m
g_{DS}	11u	11,3u	3,86u	2,41u	3,46u	48,2u	5,68u	2,22u	6,33u
g_{MB}	2,38m	2,38m	376u	1,39m	378u	1,34m	5,02m	1,39m	1,35m

NAME	M_{b6}	M_{b7}	M_{m1}	M_{m2}	M_{m3}	M_{m4}	M_{m5}	M_{m6}
Size/type	P:800/5µ	N:400/5µ	P:400/2µ	P:800/3µ	P:800/3µ	N:1000/3µ	N:800/4	N:800/4µ
I_D	-800u	800u	-2,37m	-2,33m	-2,37m	2,33m	2,37m	2,37m
V_{GS}	-1,68	1,28	-2,06	-1,91	-1,91	1,19	1,33	1,33
V_{DS}	-1,68	1,28	-3,67	-1,91	-3,3	3,09	1,33	1,7
V_{BS}	0	0	0	0	0	0	0	0
V_{TH}	-1,02	769m	-1,04	-1,03	-1,03	781m	773m	773m
V_{DSAT}	-515m	317m	-801m	-688m	-688m	262m	343m	343m
g_M	2,33m	2,95m	4,34m	5,01m	5,11m	10,5m	8,02m	8,02m
g_{DS}	8,58u	2,09u	37,1u	38,7u	27,8u	5,51u	6,17u	5,16u
g_{MB}	749u	1,39m	1,37m	1,59m	1,62m	5,03m	3,75m	3,76m

tel-00417838, version 1 - 17 Sep 2009

The dimensions of the transistors have been calculated with respect to the previously defined parameters, mainly with respect to low output resistance of the voltage buffer and low DC offset. An important parameter in the design is also the low input capacity of terminal **Y**. The input capacity is determined by $(W \cdot L)_{Mi}$ and requires the use of a narrow channel transistor M_i (L_{Mi} = 1 µm). Contrary to that, the bias transistors (M_{b1}–M_{b7}) are of the wide channel type in order to provide very low DC offset and good matching of the output transistors (M_{o1}, M_{o2}) bias currents.

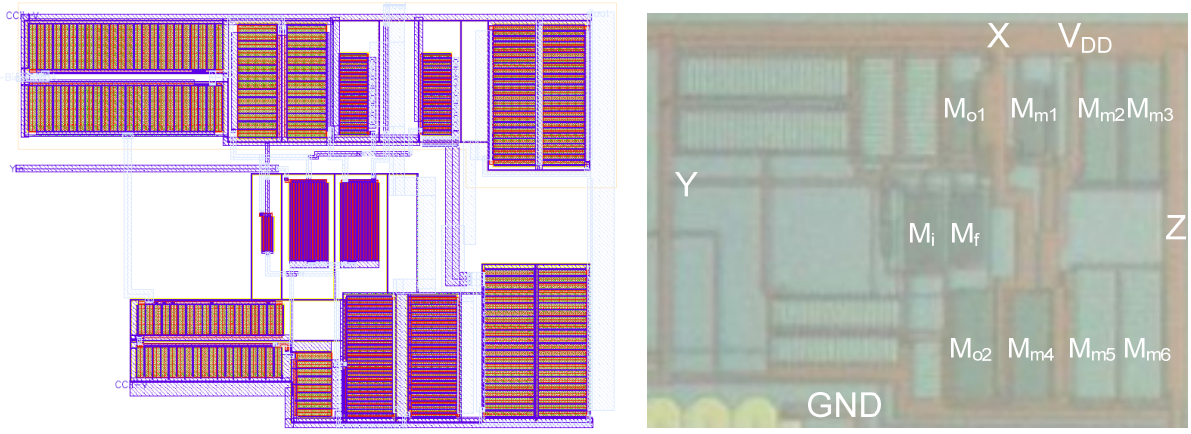
The value of the output transistors bias current is an important parameter determining the value of output resistance (see *Eq.*(10-6)). In addition, this current determines the total power consumption of the current conveyor. This consumption reaches approximately $4 \times I_{Mo}$ due to double folding of the output current provided by transistors M_{m1} - M_{m6}.

The AC characteristic of the voltage follower is not frequency-compensated with a special capacitor. A sufficient compensation is provided only by the C_{GS} capacitance of both M_{o1} and M_{m1} transistors, ensuring the stability of the unity gain follower. The dimensions of all transistors as well the corresponding operating points are listed in *Tab 10.1*.

10.3 The CMOS Integration of CCII-

The layout of the current conveyor shown in *Fig. 10.6* was provided in the Cadence® environment and integrated in a conventional process CMOS AMS 0.35 µm (*Fig. 10.7*). During the layout, all rules mentioned in *chapter 7* were respected. In particular, the high driving capacity of **X** and **Z** outputs require the use of large metallic interconnections and multi-finger transistors, which can be seen in *Fig. 10.7*.

The integrated circuit has been characterized in order to investigate the basic AC and DC parameters. An example of application in a 1.5 MHz low-pass filter based on the CCII biquadratic section with high stopband suppression was also realised, and it is shown in *section 10.3.2*.



a) *b)*

FIG. 10.7: *a) Layout of the CCII- in Cadence® environments b) microphotography of the fabricated CCII- in CMOS 0.35 µm (die size 500×350 µm²)*

10.3.1 The AC & DC Characteristics of the Integrated Circuit

In this section we will provide the basic DC and AC characteristic obtained by measurements of the manufactured circuit. The main measured features are summarised in *Tab. 10.2*.

tel-00417838, version 1 - 17 Sep 2009

TAB. 10.2: MAIN FEATURES OF INTEGRATED CCII- MEASURED AT T = 290 K

V_{DD}	+/- 2.5V
Quiescence current	11 mA
Port X,Z voltage swing	+/- 1.5 V
Port X,Z driving capacity	+/- 20 mA
Port Z DC impedance	~7.5 MΩ
Port X offset voltage	2.7 mV
Port Z offset current	2.25 µA
-3dB AC transfer Y→X	~110 MHz
Port X resistance @ DC	2 Ω
Port X impedance @ 1MHz	2.5 Ω
Port X impedance @ 10MHz	8.5 Ω

The measurements of DC characteristics allow us to verify the basic functions of current conveyor, as described by transfer matrix (10-1). This verification was provided by an automatic test bench containing one voltage/current generator and one voltmeter.

Fig. 10.8 shows the measured transfer between terminals **X**, **Y** and **Z**. The input voltage V_Y was swept in the range of ± 2.5 V. The voltage V_X was measured on terminal **X**, *i*) open and *ii*) loaded by resistor $R_L = 500\ \Omega$. This load resistor enables the generation of current I_X and, consecutively, the generation of current I_Z. For the required $I_X = -I_Z$, a resistor of identical value (500 Ω) can be connected to terminal **Z** in order to provide a voltage drop $V_Z = -V_X$. In this way, the DC transfer between all the three terminals can be measured at the same time.

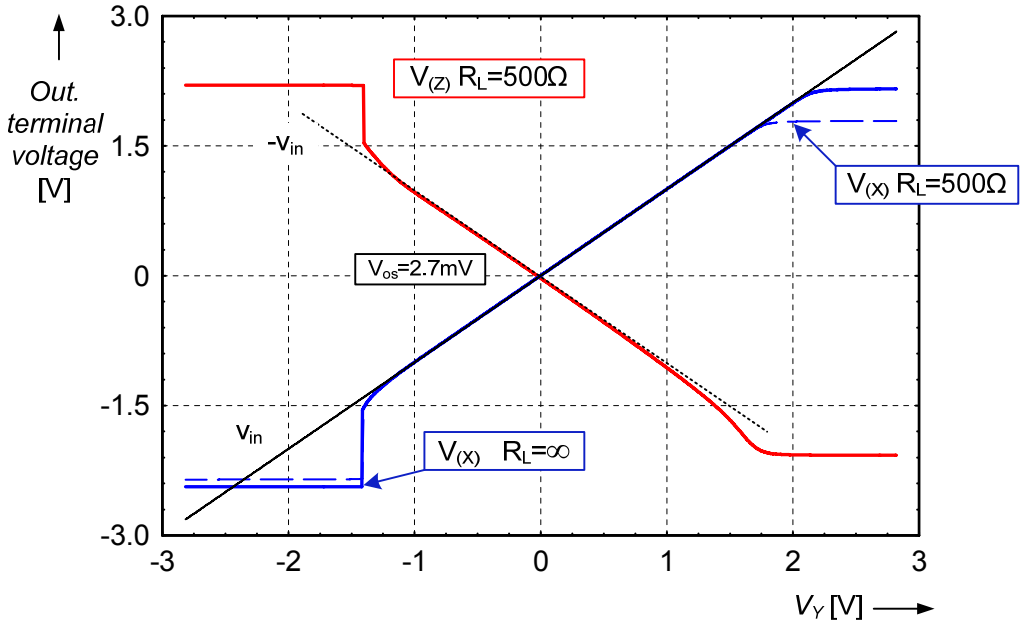


FIG. 10.8: *The DC transfer characteristic: voltage* **Y**→**X** *transfer for the* **X** *terminal, open-ended and loaded by 500 Ω,* **X**→**Z** *current transfer for both the* **X** *and the* **Z** *output loaded by matched resistances 500 Ω.*

In *Fig. 10.8,* a very good linearity of transfer **Y**→**X** can be observed. This is caused by the voltage feedback *via* transistor M_f. Moreover, we have obtained an accurate current transfer **X**→**Z** having a gain very close to -1.

tel-00417838, version 1 - 17 Sep 2009

The parameter related to output resistance r_x is the maximal driving capacity. The driving capacity is limited by the maximal (positive and negative) currents of terminals **X** and **Z**. The measured characteristic, *Fig. 10.9,* shows the maximal current value of ± 20 mA and has very good linearity within the range of ± 10 mA.

As already mentioned, the high impedance of terminal **Z** is not critical in our application. Hence, its value was measured (by means of an external current source $I_{Z(extern)}$) and shows 7.5 MΩ (*Fig. 10.10*), which is a very good result for CMOS (note that this value exceeds the simulated value of g_{DS} of the M_{m3} and M_{m6} transistors, see *Tab. 10.2*).

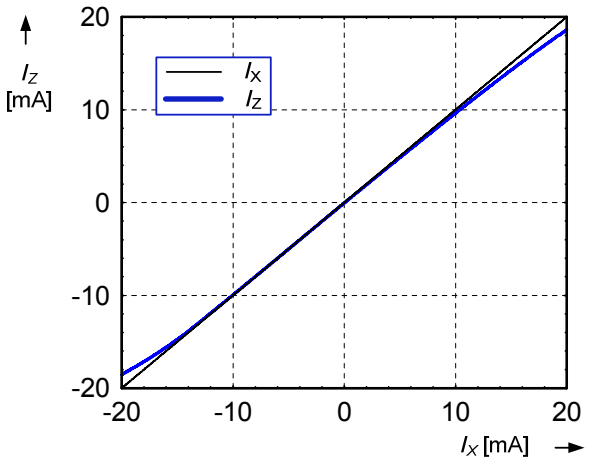


FIG. 10.9: *The measured **X**→**Z** static current transfer*

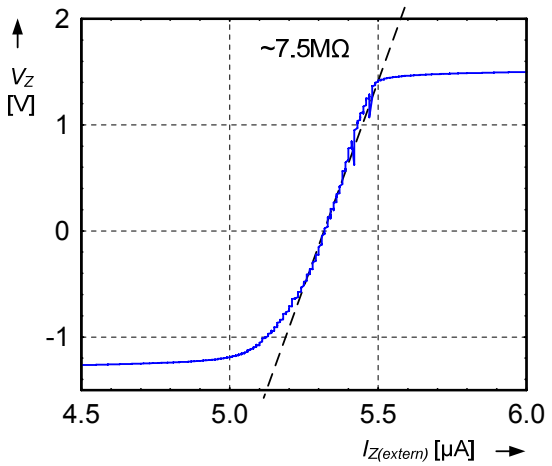


FIG. 10.10: *The measured impedance of terminal **Z***

The AC test was performed in order to determine the frequency transfer $v_{(y)}/v_{(x)}$ and the value of output resistance $r_x(f)$. *Fig. 10.11* shows the simulated and measured frequency response $v_{(y)}/v_{(x)}$. The measurement was effected with a small (~pF) load capacitance and exhibits resonance of around 100 MHz (the simulation was performed with the zero capacitive load).

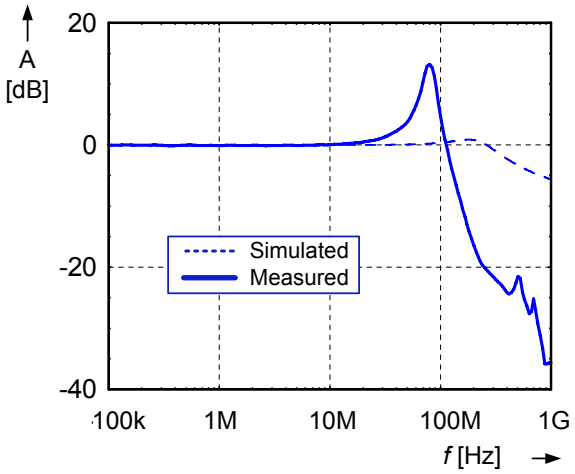


FIG. 10.11: *The Measured and simulated AC response of the unity gain voltage buffer (measured with ~3 pF load)*

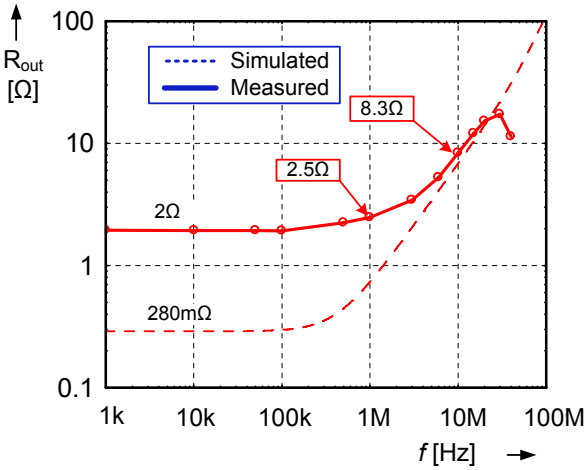


FIG. 10.12: *The measured and simulated resistance of output terminal **X***

The most important result is shown in *Fig. 10.12*, where output resistance was plotted as a function of frequency. This characteristic confirms the selected design approach, allowing us to achieve the low and frequency-constant output resistance by means of the use of a feedback structure with minimized

tel-00417838, version 1 - 17 Sep 2009

parasitic capacitance (*i.e.* using simple architecture). *Fig. 10.12* shows the low value of r_x: 2.5Ω/$_{1MHz}$ and ~8.5Ω/$_{10MHz}$, which can be favourably compared with another result achieved in CMOS (for instance [145], [146], [147]).

10.3.2 Application of the CC in 1.5MHz 5th order LP filter

One of the aims of the design was to verify the parameters of the biquadratic cascade section from *Fig. 9.18*, which features high attenuation in the stopband. A 5th order low-pass cascade filter containing two biquadratic sections *introduced in Fig. 9.18* and one 1st order section is shown in *Fig. 10.13*. The filter is composed of two integrated current conveyors and two unity gain voltage followers. The voltage followers were also added into the input and output of the filter in order to operate the circuit in ideal conditions. These buffers were built with AD8055 operational amplifiers.

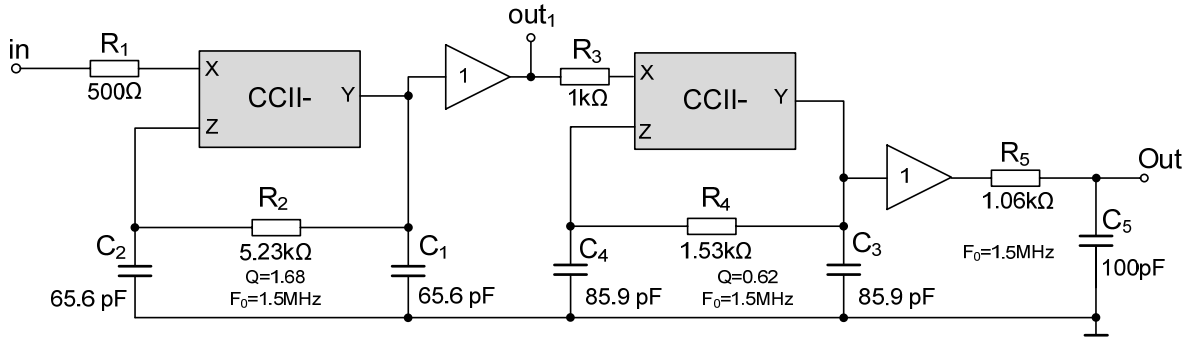


FIG. 10.13: *Cascade realization of the 5th order LP filter (Butterworth) using Fig. 9.18 low- pass cascade section*

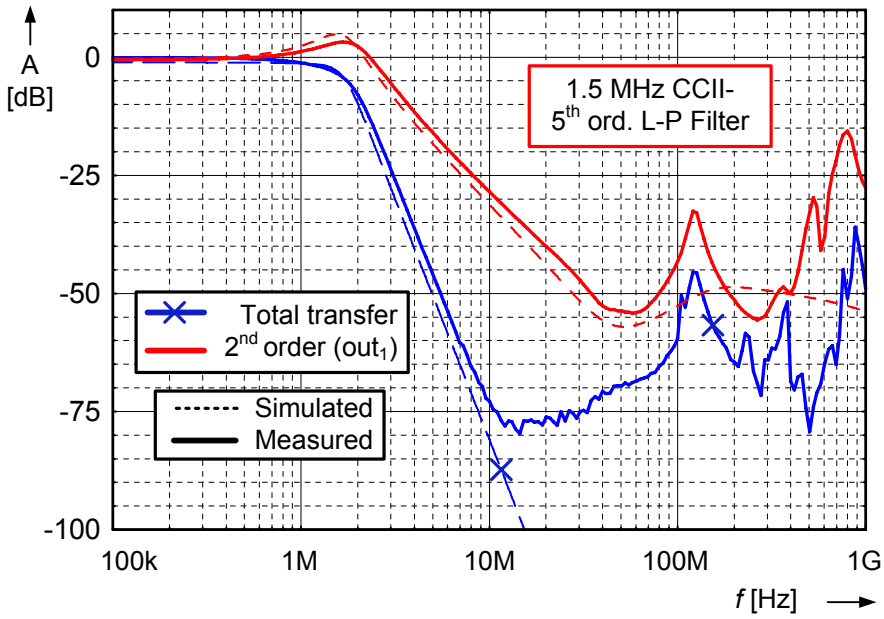


FIG. 10.14: *The measured and the simulated characteristic of 1.5MHz 5th ord. Fig. 10.14 LP filter realised with Fig. 10. 7 CCII-*

In order to demonstrate the performance of the filter, we used the PCB support as described in *Fig. 8.5*. However, this multi-purpose PCB circuit was not optimized for high frequencies (*i.e.* shielding, crosstalk, and other aspects), which can cause the spurious transfers and limits the stopband attenuation (*e.g.* we can refer to a resonance peak at $f \approx 100$ MHz in *Fig. 10.14*). Nevertheless, the

tel-00417838, version 1 - 17 Sep 2009

measured frequency transfer shown in *Fig. 10.14* exhibits a very good rate of suppression reaching approximately -50dB for the 1st biquadratic block of filter.

The simulation results shown in *Fig. 10.15* were provided on the transistor level using the CCII- *Fig. 10.7* (SPICE Level-7). For the 1st order biquadratic block, (where the attenuation in the stop-band is not affected by the cornstalks) the simulations agree well with the measurements.

10.4 Conclusion

A design of CMOS, second generation current conveyor CCII- was reported in this chapter. In the design, the structure of CMOS output buffer was optimized in order to reach the low output resistance at MHz frequencies.

As initially required, the integrated current conveyor can be advantageously used in the frequency filters up to MHz frequencies. This is due to the good achieved performances. For instance, the measured output resistance of node **X** was particularly low, *e.g.* 2.5 Ω at 1MHz (see *Fig. 10.12*). Such low impedance was the important objective of design and would allow to realise frequency filters having the high dynamic range at higher frequencies (high attenuation in the stopband). Moreover, the obtained DC performances such as high driving capacity (+/- 20mA, *Fig. 10.9*) or the linearity of voltage transfer (*Fig. 10.8*) make this device suitable for high accuracy circuits, as required by the laboratory instrumentation. The example of 1.5 MHz frequency filter demonstrates the good performance of the biquadratic section was presented in the last paragraph.

The high AC and DC performances were also a criterion in the layout of the integrated circuit. This layout was provided in regular 0.35 µm silicon CMOS technology and the circuit was patterned on a silicon wafer in the AMS foundry (die size 500×350 μm^2).

The integrated circuit achieves parameters competitive with the state-of-the-art and complies with the requirements of high performance test bench, applied to the development of new generation bolometric THz detectors.

tel-00417838, version 1 - 17 Sep 2009

Conclusion of part IV

The partial conclusion concerning the III[rd] part: "Design of CMOS Feedback-Free Differential Amplifiers for Wide Temperature Range" is provided on the page 129.

In the IV[th] part of the thesis we have presented certain methods improving the parameters of analog filters, namely their maximal frequency and dynamic ranges. These filters will be used in the low noise cryogenic test-bench intended to facilitate the development of the THz bolometric detectors as well as the development of the other projects related to this thesis.

Following a list of objectives, a theoretical review of the continuous-time frequency filters has been done in *chapter 8*. At the end of this chapter, an example is introduced of an adaptive system of frequency filter developed by the author; the system was presented in order to demonstrate the good performances of analog signal processing. These performances can be favorably compared to the current solutions using the DSP.

As described in the section "goals of the work", our primary aim is to define the methods allowing an increase of the frequency range of frequency filters that are based on standard technologies and components (such as the low-cost CMOS amplifiers). In this respect, low stopband suppression was pointed out as a fundamental limiting factor, mainly for the reason that it is a consequence of the real properties of active devices. Two analyses were performed as an example indicating a way which allows us to increase the stopband suppression. Briefly, this technique consists in the shifting or cancelling of the parasitic transfer zeros in frequency responses of an active filter.

When applied to the design, the technique enables us to obtain a structure called *type II* Sallen-Key low-pass filter, whose parasitic zero can be arbitrarily selected. The presented approach allows the frequency response of this widely used structure to be improved by means of using one additional voltage follower and realizing an optimal choice of impedance level. We have demonstrated this improvement by simulation and measurements: an increase was obtained in the stopband attenuation of ≈ 20 dB without optimization and of ≈ 50 dB with optimization.

In the following paragraph, a biquadratic structure having ideally no parasitic zero has been designed and successfully tested at frequencies up to 20 MHz; we have observed constant and high attenuation during the measurements. This biquadratic section using the current conveyor CCII is based on the separation of the frequency span into two types of regions, namely a low frequency region covered by the active element, and the stopband one, where the high attenuation is ensured only by a passive RC network. As an example, a 10 MHz cut-off frequency Butterworth filter of the 4[th] order was realized with the rate of attenuation reaching 100 dB.

In order to facilitate the utilization of this biquadratic filter, an integrated high performance current conveyor (CCII-) was designed and realized in the CMOS 0.35 µm process (*chapter 10*). The main argument to justify the design was the realization of the previous biquadratic section testing. We also wished to materialize a versatile component with superior performances; this component is important for the future research in the domain. The performances of the conveyor were optimized in order to provide a low value of the voltage buffer output resistance $R_{(X)}$. Our strategy was to utilize an optimal (CMOS) structure containing only several elements (*i.e.* only a small number of parasitic capacitances) and to provide its mathematical optimization. For instance, we measured mainly the low output resistance of node X: 2.5 Ω at 1MHz, but also the high driving capacity (+/- 20mA, see *Fig. 10.9*) and good DC linearity of the CCII. This makes the device suitable for high accuracy circuits, which is required by laboratory instrumentation.

As described in the above-stated text, the results of the work presented in the 4[th] part were already applied in practical projects related to this thesis and they are intended to be utilized in the process of development of new generation bolometric THz detectors.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

i RESUME DE LA THESE DOCTORALE

Présentation

Le sujet de ce travail de thèse doctorale porte sur la conception de circuits électroniques analogiques, destinés à des capteurs THz, de type *bolomètres*. L'électronique développée dans cette thèse est un important maillon de la chaîne de traitement des signaux issus des ces capteurs. Avant d'aborder les aspects techniques, nous exprimerons les objectifs de cette thèse en quelques mots-clés :

- Amplification à faible bruit;
- Mise en œuvre cryogéniques;
- Basse consommation;
- Large plage de dynamique et précision.

Le sujet traité dans ce manuscrit est réparti en trois groupes principaux. Après une introduction du sujet (*partie I – chapitres 1, 2, 3*) nous étudierons dans une *partie II* abordée au *chapitre 4* l'amplification pour un imageur-test contenant quatre-pixels. Ici, nous définissons une configuration optimale, utilisant des amplificateurs différentiels CMOS de gain $G_0 = 40$ dB et fonctionnant *en boucle ouverte*. L'utilisation de cette configuration « inhabituelle » peut conduire à une bande passante plus grande (dû au non-besoin d'une compensation fréquentielle), à une très grande impédance d'entrée et un bruit réduit, en raison de l'absence de réseau de contre-réaction.

En dépit de ces avantages, un amplificateur en boucle ouverte souffre couramment d'une variation importante de son gain, en raison de la dispersion de paramètres du *process*. De ce fait, la deuxième partie du travail s'appuie sur la conception d'amplificateurs CMOS sans contre-réaction, de gain fixé avec précision ($G_0 = 40$ dB), et ceci dans une plage de températures allant de 70 K à 390 K. Nous définissons au *chapitre 5* les structures et les principales innovations, permettant d'atteindre ces objectifs et aboutir à deux réalisations d'amplificateurs différentiels : l'amplificateur de *Type I* basé sur la fixation du gain par des rapports géométriques des transistors, et l'amplificateur linéaire de *Type II*, basé sur une stabilisation du gain par une compensation thermique élaborée. Les deux amplificateurs font appel à un nouvel élément appelé « *transistor synthétique à basse transconductance* » (low transconductance composite transistor). L'optimisation du *lay-out* en technologie CMOS 0.35 µm est également présentée. Dans le *chapitre 7* nous présentons les résultats

obtenus sur les circuits intégrés CMOS, qui ont montré des performances très intéressantes, comparables à l'état de l'art dans le domaine.

La *partie III* de la thèse est dédiée à des filtres de fréquence actifs, considérés comme des éléments essentiels d'une chaîne de traitement de signal bas bruit. Dans cette partie, nous nous appuierons sur l'étude des limitations causées par les éléments actifs, réels. L'analyse de ces limitations sera utile par la suite pour la conception de deux structures des filtres passe-bas biquadratiques, ayant des performances améliorées notamment en ce qui concerne l'atténuation aux hautes fréquences. Ceci permet d'aboutir à des fréquences de coupure plus élevées, comme vérifié par les mesures. Le dernier *chapitre 10* est dédié à la conception d'un convoyeur de courant CCII- en CMOS 0.35 µm. Ce convoyeur est destiné à être utilisé dans la section biquadratique conçue dans la *chapitre 9*. Les performances de ce convoyeur ont été optimisées afin d'obtenir une impédance de sortie très basse (de l'ordre de l'ohm à des fréquences des quelques MHz).

Dans ce résumé, nous allons brièvement présenter les principes et les résultats obtenus avec les circuits réalisés. La description complète et détaillée est traitée dans ce manuscrit en anglais.

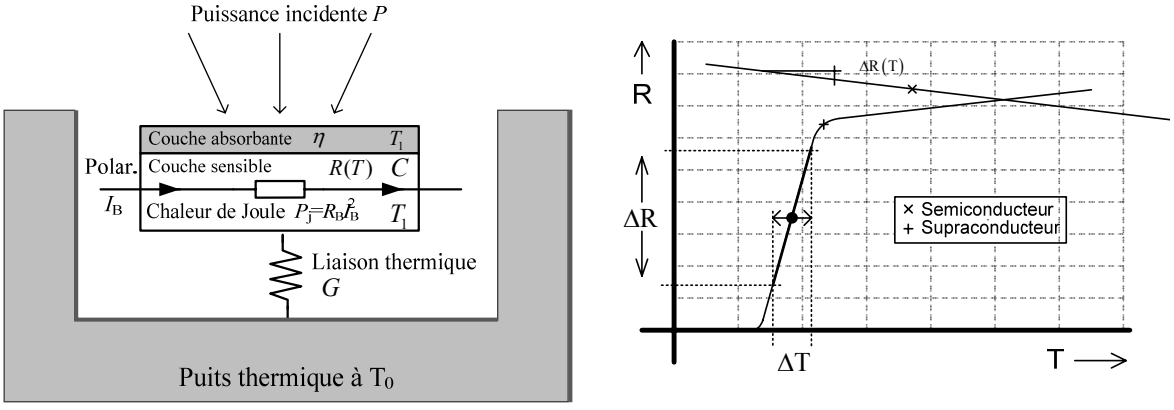
Les travaux présentés dans cette thèse s'inscrivent dans le programme NanOtime, sous un contexte collaboratif entre quatre laboratoires en France et en République Tchèque : LGEP-Supélec, et L2E associés à l'Université de Pierre et Marie Curie – Paris 6, le Département d'Electronique Théorétique de l'Université Technique de Brno et l'Université de Défense de Brno.

I Electronique de lecture

Les bolomètres sont des capteurs thermiques, convertissant la variation de puissance d'un rayonnement incident en une variation de résistance électrique. Dans ce chapitre, nous esquissons le principe d'un capteur bolométrique, et le choix de l'électronique de lecture.

I.1 Capteur bolométrique

La composition typique d'un bolomètre est montrée sur la *Fig. i.1 a*) [1]. Il est composé d'une couche absorbante, d'une couche sensible de résistance dépendant de la température $R = f(T)$ (*Fig. I.1 a*), et d'un puits thermique de température constante. Ce puits thermique est connecté à la couche sensible par un lien thermique de conductance G.



a) *b*)

FIG. *i*.1: *a) Empilement d'un bolomètre classique, b) caractéristique R = f(T) d'un bolomètre à semi-conducteur et à supraconducteur*

Le fonctionnement d'un bolomètre est basé sur la transformation de l'énergie du rayonnement électromagnétique incident en chaleur au sein de l'absorbant ; il s'ensuit variation de la résistance de la couche sensible (*Fig. i.1*). La mesure de cette résistance est la fonction principale de l'électronique de lecture.

tel-00417838, version 1 - 17 Sep 2009

I.2 Configuration de l'électronique de lecture

L'électronique de lecture est un ensemble de circuits, dédiés à la conversion de la résistance du bolomètre en une valeur électrique, exploitable. Le choix de la méthode peut affecter les paramètres clés du détecteur (rapport signal à bruit, sensibilité, bande passante etc.). Afin d'obtenir les paramètres optimaux, une lecture différentielle CMOS et une polarisation en courant ont été choisis. Les paramètres de l'amplification différentielle ont été estimés plus avantageux, comparés aux structures non-différentielles, utilisées dans des travaux précédents [57], [58].

Sur le circuit de la *Fig. i.2*, un ensemble de *m* pixels est polarisé à courant constant. Cette polarisation induit une tension sur chaque bolomètre. Il est évident que tout changement de la résistance R_b induit aussi une variation de la tension correspondante. Forme qui concerne notre projet, des groupes de quatre pixels bolométriques sont envisagés. Dans ce qui suit, nous allons définir la structure de l'électronique et concevoir les amplificateurs différentiels à gain fixe.

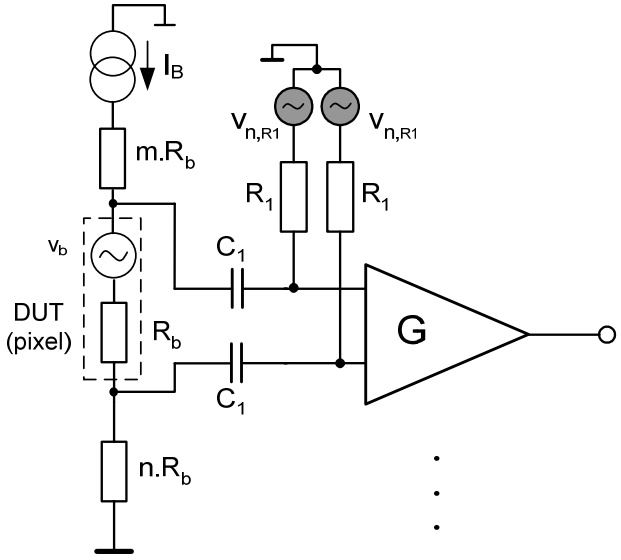


FIG. *i.2*: *Principe de la lecture d'une matrice de m bolomètres. Les capacitances C_1 enlèvent les composantes DC et les résistances R_1 polarisent les entrées d'amplificateurs*

I.3 « Architecture sans contre-réaction »

Les structures d'amplificateurs différentiels ont été largement étudiées, notamment les solutions classiques à boucle fermée, utilisant les amplificateurs opérationnels (AO). Dans cette étude, certaines limitations connues de ces structures ont été identifiés. Parmi les plus importantes, la diminution de la bande passante causée par la compensation fréquentielle, sa limitation importante pour assurer la stabilité de la boucle. D'autres phénomènes ont été également mentionnés, comme le niveau bruit élevé causé par le réseau résistif de contre-réaction, ou la faible résistance d'entrée du montage différentiel d'AO (ceci peut aboutir à une configuration d'AO d'instrumentation, contenant deux ou trois AO).

Une structure sans contre-réaction, ou « feedback-free », est représentée sur la *Fig. i.2*, ou l'amplificateur fonctionne en boucle ouverte. L'utilisation d'une telle structure permettre d'éviter les effets mentionnés précédemment, et de plus, peut conduire à une consommation réduite – un paramètre clé pour les applications cryogéniques.

Malgré ces côtés positifs, les structures sans contre-réaction peuvent atteindre une dispersion importante des paramètres (gain), en conséquence de la variation des paramètres technologiques. Ceci sera notamment plus important pour la plage de température prévue, allant de T = 40 K à T = 390 K. La conception des tels amplificateurs différentiels CMOS à gain 40 dB est le défi principal de notre travail.

tel-00417838, version 1 - 17 Sep 2009

II Conception des amplificateurs CMOS

Dans cette deuxième partie, nous allons brièvement présenter l'approche de la conception des amplificateurs différentiels, fonctionnant en boucle ouverte. Le premier paragraphe présentera la caractérisation des transistors MOS en milieu cryogénique, afin d'obtenir un modèle thermique symbolique. Une approche de conception d'amplificateurs en boucle ouverte sera présentée dans le deuxième paragraphe. A ce propos, un nouvel élément, le transistor composite à faible transconductance sera introduit et utilisé dans deux types d'amplificateurs : l'amplificateur de *Type I* basé sur la fixation du gain par des rapports géométriques de transistors et amplificateur linéaire de *Type II*, basé sur la constance du gain par compensation thermique des paramètres physiques du transistor.

II.1 Comportement thermique d'un transistor MOS

La construction d'un modèle analytique du transistor MOS va nous permettre d'optimiser l'amplificateur présenté dans le *chapitre II.3*, dans la plage des températures de 70 à 390 K. La construction d'un tel modèle est nécessaire, du fait de la non-validité des modèles standard (SPICE) en milieu cryogénique.

Le courant de drain d'un transistor NMOS en saturation suit la loi quadratique :

$$I_{\mathrm{D}} = \frac{\mu C_{\mathrm{OX}}}{2} \cdot \frac{W}{L} \cdot \left(V_{\mathrm{GS}} - V_{\mathrm{TH}}\right)^2, \tag{i-1}$$

où μ est la mobilité des porteurs, C_{OX} la capacité de grille par unité surface, W/L le rapport entre la largeur et la longueur du canal, V_{GS} la tension grille-source et V_{TH} la tension de seuil. Dans la pratique, nous faisons appel aux deux autres paramètres : facteur de gain $KP_{(\mathrm{P,N})} = \mu_x \cdot C_{\mathrm{OX}}$ et le gain $\beta = \mu \cdot C_{\mathrm{OX}} \cdot W/L$. Dans la formule (i-1), deux quantités dépendant de la température peuvent être identifiées:

- La mobilité $\mu(T_0)$, (T_0 est la température ambiante de référence) [22]:

$$\mu(T) = \mu(T_0)\left(T/T_0\right)^{-x} \tag{i-2}$$

- Et la tension de seuil:

$$V_{\mathrm{TH}}(T) = V_{\mathrm{TH}}(T_0)\left[1 + \alpha_{\mathrm{TH}} \cdot \left(T - T_0\right)\right], \tag{i-3}$$

Où t_h est le coefficient de température:

$$\alpha_{\mathrm{TH}} = V_{\mathrm{TH}}^{-1} \cdot \left(dV_{\mathrm{TH}}/dT\right). \tag{i-4}$$

Avec ces trois dernières équations, nous sommes en mesure d'établir le modèle analytique pour un transistor à saturation:

$$I_{\mathrm{D}} = \frac{KP_{\mathrm{N}}(T_0)}{2} \cdot \left(\frac{T}{T_0}\right)^{-x} \cdot \frac{W}{L} \cdot \left[V_{\mathrm{GS}} - V_{\mathrm{TH}}(T_0) \cdot \left(1 + \alpha_{\mathrm{TH}}\left(T - T_0\right)\right)\right]^2. \tag{i-5}$$

Les résultats obtenus par la mesure et simulation (avec le modèle BSIM3 model) pour les températures ambiante et cryogénique (T = 77 K) (PMOS W = 100 3M / L = 10 3M) sont regroupés dans le *Tab. i.1*. Les coefficients thermiques t_h et x ont été déduits des caractéristiques *I-V* et *Eq.*(i-2) Et *Eq.*(i-4): $x = 0.90$, $t_h = -2.163\ \mathrm{km}^{-1}$ et $dd_t/ddt = 2.06\ \mathrm{mV \cdot K^{-1}}$. Dans ce *tableau i.1*, une inexactitude du model BSIM-3 pour les basses températures peut être notée.

TAB *i*.1: *Les paramètres de transistor PMOS W/L = 100 µm / 10 µm, fabriqué en 0.35 µm CMOS*

TYPE / TEMPERATURE	KP_{P} (µA/V^2)	V_{TH} (V)
Simulation T = 296 K	20.67	– 0.965
Mesure T = 296 K	21.63	– 0.953
Simulation T = 77 K	76.37	–1.230
Mesure T = 77 K	72.43	– 1.405

tel-00417838, version 1 - 17 Sep 2009

II.2 Méthode de Conception

Fixation de la valeur du gain

Un exemple d'amplificateur à gain fixe CMOS est le montage *source commune*. Ce montage est composé d'un transistor de *commande* M_D (de type N par exemple), et d'un transistor de *charge* (transistor P), monté en diode. Le gain G_0 d'un tel amplificateur peut être défini à l'aide du rapport des transconductances:

$$G_0 = \frac{v_{OUT}}{v_{IN}} = -\frac{g_{mD}}{g_{mL}} = -\sqrt{\frac{KP_N}{KP_P}} \cdot \sqrt{\frac{W_D / L_D}{W_L / L_L}}, \tag{i-6}$$

Où KP_N, KP_P, W_D/L_D, KP_P et W_L/L_L sont relatifs aux transistors M_D et M_L. Dans cette formule, le gain G_0 est déterminé par les dimensions des transistors KP_N/KP_P. Ce rapport est en effet équivalent à un rapport de mobilité des porteurs (électrons vs. trous) [22]. En conséquence, le gain ne dépend que du rapport des dimensions précises, mais aussi de KP_N/KP_P introduisant ainsi une inexactitude. De plus, une valeur de gain de l'ordre de quelques dB seulement peut être réalisée, avec des dimensions de transistors raisonnables. [70].

Le transistor à faible transconductance

Afin d'atteindre le gain requis de 40 dB, nous avons conçu un transistor de charge, dont la transconductance est diminuée par une méthode de division des courants. Ce transistor (*Fig. i.3*) est en fait un transistor composite, équivalent à un transistor ayant un rapport *W*/*L* faible. Ce faible *W*/*L* est réalisé avec des transistors de dimensions grands et précise.

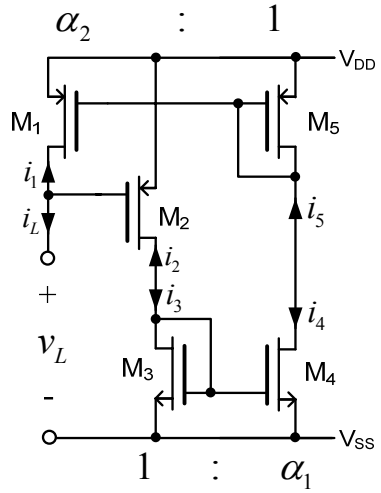


FIG. *i.3*: *Le transistor à faible transconductance*

La transconductance équivalente g'_m peut être déterminée à partir du rapport i_d/v_{al}. Le courant de drain du transistor M_2 ($-g_{m2} \cdot V_{GS2}$) est diminué grâce à deux miroirs de courant M_3–M_4 et M_5–M_1, respectivement caractérisés par α_1 et α_2:

$$\alpha_1 = \left(W_4/L_4\right) \Big/ \left(W_3/L_3\right), \text{ et } \alpha_2 = \left(W_1/L_1\right) \Big/ \left(W_5/L_5\right). \tag{i-7}$$

Le courant du drain peut être écrit:

$$i_D = -\alpha_1 \cdot \alpha_2 \cdot g_{m2} \cdot v_{OUT}, \tag{i-8}$$

où $v_{outa} = v_{GS2}$. La transconductance équivalente g'_m apparaît sous la forme suivante:

$$g'_m = \sqrt{\alpha_1 \alpha_2} \cdot \sqrt{2 \cdot K_{PP} \cdot \frac{W_2}{L_2} \cdot I_D}. \tag{i-9}$$

tel-00417838, version 1 - 17 Sep 2009

De là, nous déduisons la réduction de la transconductance par le terme $(\alpha_1 \cdot \alpha_2)^{½}$, inférieur à l'unité.

II.3 Amplificateur de Type I

L'une des méthodes permettant d'éliminer le facteur KP_N/KP_P est de faire en sorte que celui-ci devienne égal à l'unité, par l'utilisation de transistors M_D et M_L ayant le même type de canal. Ceci peut être réalisé par le montage dit *cascode replié* [22].

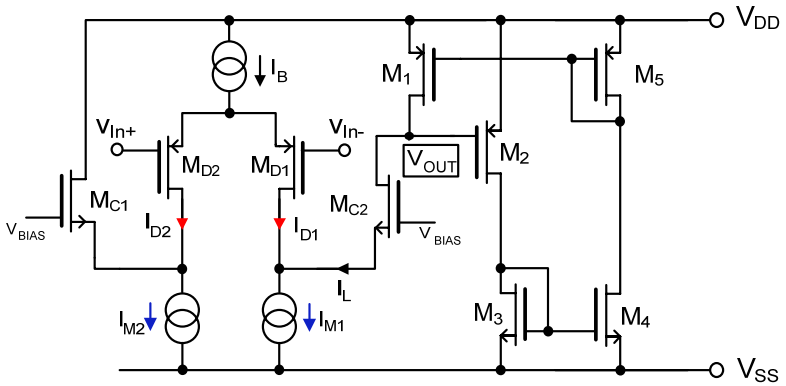


FIG. *i*.4: *L'amplificateur de Type I composé de la paire différentielle et du transistor à faible transconductance*

La *Fig. i.4* montre l'amplificateur de *Type I*, composé du transistor à faible transconductance *Fig. i.3*, et de la paire différentielle (transistor M_D). Le circuit est polarisé par les sources de courant I_B et I_M.

Le paire différentielle se comporte ainsi comme une source du courant I_D commandée par la tension d'entrée différentielle $V_{IN} = V_{IN+} - V_{IN-}$. Le courant de charge I_L s'écrit comme :

$$I_L = I_M - I_D\,, \tag{i-10}$$

Ce qui est égal, pour une tension d'entrée nulle, à $I_L = I_M - I_B/2$. L'expression du courant donne la réponse DC de la paire différentielle :

$$I_D = \frac{1}{8}\left(\sqrt{4I_0 - \beta_D \cdot V_{IN}^2} + \sqrt{\beta_D}\cdot V_{IN}\right)^2. \tag{i-11}$$

Pour $\alpha_1 = \alpha_2 \equiv \alpha$, la réponse DC d'amplificateur de *Type I* peut être décrite par une fonction de tension d'entré, exprimée par l'intermédiaire du courant I_L :

$$V_{OUT} = V_{DD} - \left|V_{TH\,(T2)}\right| - \frac{1}{\alpha}\cdot\sqrt{\frac{2}{KP_{(T2)}}\cdot\frac{L_2}{W_2}\cdot I_L}\,. \tag{i-12}$$

De manière générale, le gain peut être écrit comme un produit de la transconductance d'_{il}/de_{vin} et par la résistance du transistor composite Da_{vout}/d'_{il}:

$$G_0 = \frac{dV_{OUT}}{dV_{IN}} = \frac{dV_{OUT}}{dI_L}\cdot\frac{dI_L}{dV_{IN}}\,. \tag{i-13}$$

Concernant la caractéristique en transconductance d'_{id}/de_{vin}, nous observons une bonne linéarité autour du point de polarisation (±15mV, *Fig. i.5*), en dépit de l'expression compliquée(i-11). Comme cette transconductance est linéaire, la forme de la caractéristique DC est liée à Da_{vout}/d'_{il}, qui est fonction de la racine carrée de I_L suivante l'$_{Eq.}$(i-12). D'après l'*Eq.*(i-13), le gain en tension peut être formellement écrit:

$$G_0(V_{IN}) = \frac{1}{2\alpha}\cdot\sqrt{\frac{W_D/L_D}{W_2/L_2}}\cdot\sqrt{\frac{I_B}{2I_L(V_{IN})}}\,. \tag{i-14}$$

Ici, nous observons qu'au voisinage d'un V_{IN} constant, le gain de cet amplificateur est seulement défini par un rapport (précis) de dimensions des transistors, et n'est plus dépendant de KP_N/KP_P comme dans

tel-00417838, version 1 - 17 Sep 2009

l'*Eq.*(i-6). De plus, malgré son expression non-linéaire, la caractéristique statique est convenable pour un fonctionnement en faibles signaux (une caractéristique DC mesurée est montrée sur la *Fig. i.5*).

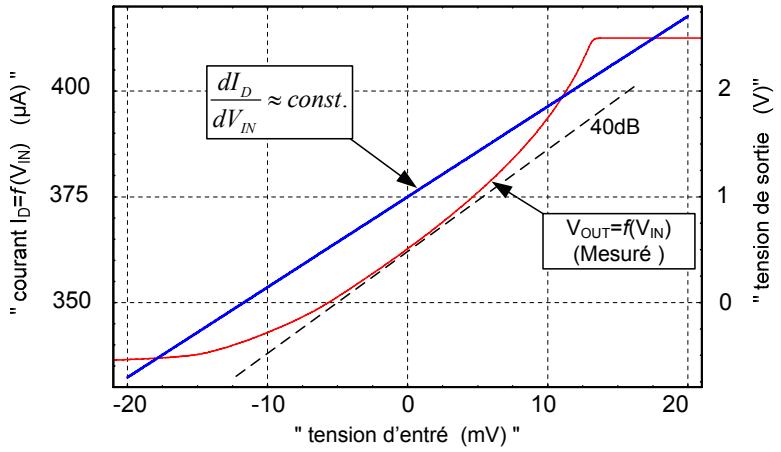


FIG. *i.5*: *Transconductance en forte signaux (dI_D/dV_{IN}) et caractéristique V_{OUT}/V_{IN} mesurée sur l'amplificateur intégré de Type I (Fig. i.4): le gain obtenu est de 39.84 dB*

Paramètres de l'amplificateur de type I

L'amplificateur *Fig. i.4* a été réalisé en technologie CMOS 0.35 µm. Les paramètres mesurés sont regroupés dans le *tableau i.2 (voir plus loin)*. Avant tout, nous pouvons mentionner la bande passante (–3 dB) obtenue pur $G_0 = 40$ dB : 10 MHz (T = 290 K) et 17 MHz (T = 77 K) pour un courant d'alimentation de 2.1 mA. Ceci correspond à des produits gain-bande de 1 GHz et 1.7 GHz, respectivement.

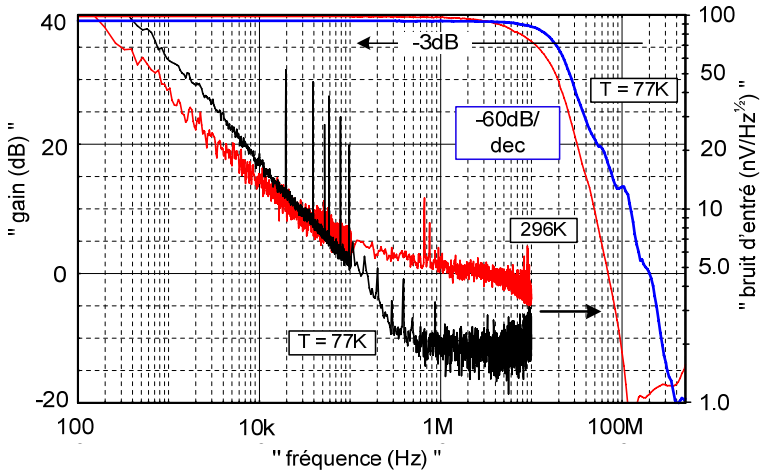


FIG. *i.6*: *Caractéristiques AC et bruit d'entrée pour T = 290 K et T = 77 K, mesurées sur l'amplificateur intégré de type I, fabriqué en CMOS 0.35 µm*

II.3 Amplificateur de type II

L'amplificateur de *type II* est basé sur une compensation thermique de gain et utilise une architecture permettant de linéariser la caractéristique DC. Cette linéarisation est obtenue par une fonction constante dV_{OUT}/dI_L. Un tel élément linéaire peut être réalisé avec deux transistors MOS connectés en diodes et mutuellement polarisés.

La *Fig. i.7* montre l'amplificateur composé du cascode replié différentiel, de la charge linéaire composée de M_1, M_2 et d'une source auxiliaire I_{AUX}. Nous allons montrer la linéarité de cette structure, ainsi que ses propriétés thermiques intéressante.

tel-00417838, version 1 - 17 Sep 2009

La valeur de I_{AUX} est choisie de manière à ce que $I_0 = 0$ pour $V_{IN} = 0$. L'expression de I_0 peut être alors exprimée à l'aide de (i-11):

$$I_0 = \left(I_M - I_D\right) - I_{AUX}\,. \tag{i-15}$$

Nous allons déterminer la caractéristique *I-V* de la charge composite montrée sur *Fig. i.7*. La loi des nœuds peut être exprimée par la fonction quadratique du courant de drain (i-1):

$$\frac{\beta_1}{2}\left(V_{OUT} - V_{TH1}\right)^2 = \frac{\beta_2}{2}\left(V_{DD} - V_{OUT} - \left|V_{TH2}\right|\right)^2 + I_0\,, \tag{i-16}$$

d'où, une expression compliquée de V_{OUT}, qui peut être simplifiée en admettant que les transistors M_1 et M_2 sont identiques ($\beta_1 = \beta_2 \equiv \beta$, $|V_{TH1}| = V_{TH2} \equiv V_{TH}$). L'extraction de V_{OUT} donne:

$$V_{OUT} = \frac{V_{DD}}{2} + \frac{I_0}{\beta \cdot \left(V_{DD} - 2V_{TH}\right)}\,. \tag{i-17}$$

Sur cette équation importante, nous pouvons observer la dépendance linéaire entre V_{OUT} et I_0, ainsi que la tension de repos V_{OUT} égale à $V_{DD}/2$. Afin de réaliser avec précision la condition $\beta_1 = \beta_2$ et $|V_{TH1}| = V_{TH2}$, les deux transistors M_1 et M_2 doivent être du même type (*par ex.* P - M_2 doit être alors « inversé »). Cette inversion peut être réalisée avec un circuit de transformation, composé d'un inverseur de tension et d'un miroir de courant. La réalisation d'une telle inversion est montrée sur la *Fig. i.8*. Cette figure montre l'inverseur de tension composé de M_{I1} et M_{I2}, et le miroir du courant composé de M_{M1} et M_{M2}. Afin d'obtenir un appariement parfait des deux transistors composites (M_1–M_5 et $M'_1 - M'_5$), le miroir de courant est réalisé avec deux transistors identiques M_{M1} et M_{M2}, ainsi que l'inverseur avec deux transistors P identiques M_{I1} et M_{I2}.

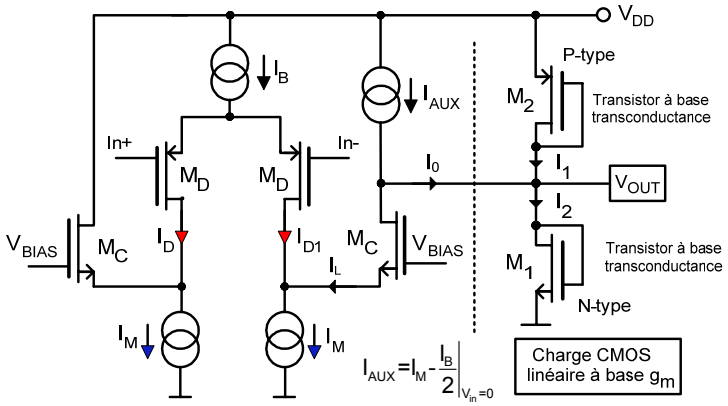


FIG. *i.7*: *Amplificateur de type II linéaire, à compensation thermique*

À cause de l'effet de substrat, le contact de M_{I2} doit être relié à la source (caisson flottant). Ceci garantira un gain constant et précis (–1) dans toute la plage dynamique.

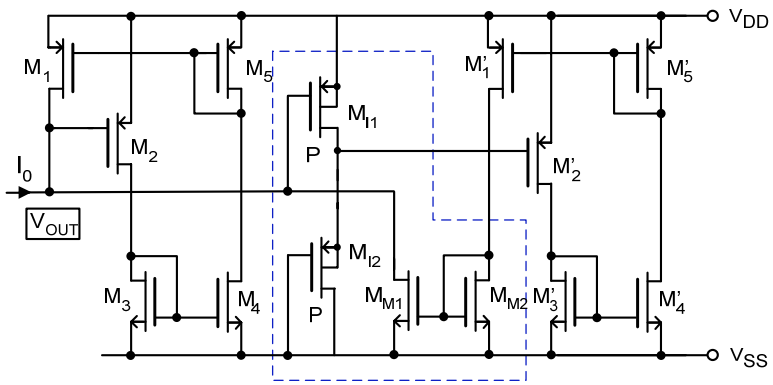


FIG. *i.8*: *Charge composite linéaire symétrisée*

Le gain en large signaux signal peut être obtenu par dérivation des équations (i-11) et (i-17), d'ou:

tel-00417838, version 1 - 17 Sep 2009

$$G_0 = \frac{1}{2\alpha} \cdot \sqrt{I_B \cdot \frac{W_D}{L_D}} \cdot \left(\sqrt{KP_P} \frac{W_2}{L_2} \left(V_{DD} - 2\left|V_{THP}\right| \right) \right)^{-1} . \qquad \text{(i-18)}$$

Nous observons ici la dépendance du gain en fonction de plusieurs paramètres: les paramètres du *process* KP_P et V_{THP}, les dimensions W/L, le courant I_B et la tension V_{DD}.

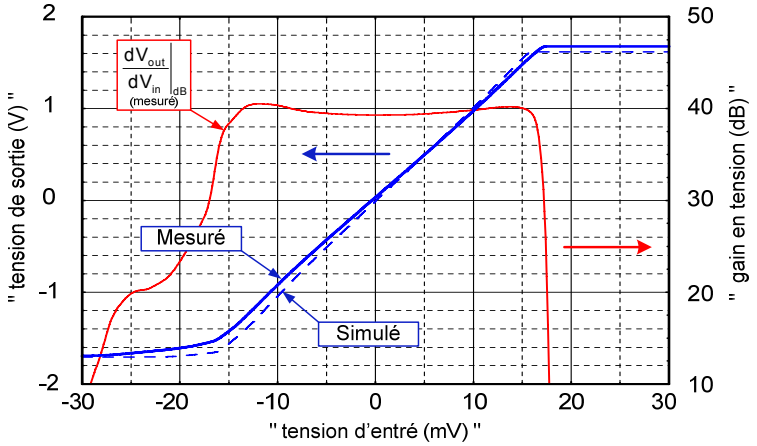


FIG. *i.9*: *La caractéristique DC mesurée et simulée de l'amplificateur de Type II. Le gain est obtenu par comme une dérivation de la caractéristique DC*

La caractéristique expérimentale mesurée sur un circuit fabriqué en CMOS 0.35 µm montre un très bon accord avec la simulation, et avec le gain requis (*Fig. i.9*). Ceci est principalement lié à l'*Eq.*(i-18) où les sensibilités $S^{G}_{I_B,K_{PP}}$ sont naturellement basses. Cependant, afin d'obtenir de bons résultats, quelques précautions ont été prises par exemple, l'utilisation des transistors larges (L > 2 µm), éliminant les effets de deuxième ordre.

L'analyse thermique

Afin d'analyser le comportement thermique, le gain en tension peut être réécrit sous la forme suivante:

$$G_0(T) = \frac{C}{\sqrt{KP_P(T)} \cdot \left(V_{DD} - 2 \cdot \left| V_{TH}(T) \right| \right)}, \qquad \text{(i-19)}$$

où le C est un terme représentant les paramètres constants, indépendants de la température: les dimensions (rapport géométrique W/L) et le courant de polarisation I_B. Tenant compte des équations (i-2) et (i-3), le comportement thermique peut être déduit à partir de l'équation (i-19). La dépendance thermique du gain est la suivante :

$$G_0(T) = \frac{C}{\sqrt{KP_P(T_0) \cdot \left(\frac{T}{T_0} \right)^{-x}} \cdot \left[V_{DD} - 2 \cdot \left| V_{TH}(T_0) \right| \cdot \left(1 + \alpha_{TH} \left(T - T_0 \right) \right) \right]}, \qquad \text{(i-20)}$$

où les paramètres mentionnés dans le *tableau 1* peuvent être utilisés, afin d'évaluer la variation dans la plage de température de 77 à 300 K.

Le fait que l'équation (i-20) dépende de la tension d'alimentation V_{DD} nous permet de contrôler la contribution de $V_{TH}(T)$ et, par conséquent, d'équilibrer la caractéristique thermique $G_0(T)$: le gain déduit de la formule (i-20) a une meilleure stabilité entre T = 270 − 380 K pour V_{DD} = 5 V que pour V_{DD} = 4 V. Cependant, les performances calculées pour la plage entière 77 − 380 K sont meilleures pour V_{DD} = 4 V (variation du gain de 1.3 dB pour T = 77 K) que pour V_{DD} = 5 V (soit 2.5 dB de variation pour T = 77 K). Cette dépendance $G_0(T)$ a été mesurée entre 4.2 et 390 K (*Fig. i.10*) ; elle est en bon accord avec (i-20), notamment aux environs de 300 K et de 77 K où les paramètres x et α_{TH} ont été mesurés. Néanmoins, aux alentours de 100 K, un écart à l'*Eq.*(i-20) peut être observé. Ceci est

tel-00417838, version 1 - 17 Sep 2009

attribué à une simplification en (i-5), où, pour la plage de température envisagée, les paramètres x et α_{TH} ont été considérés comme constants.

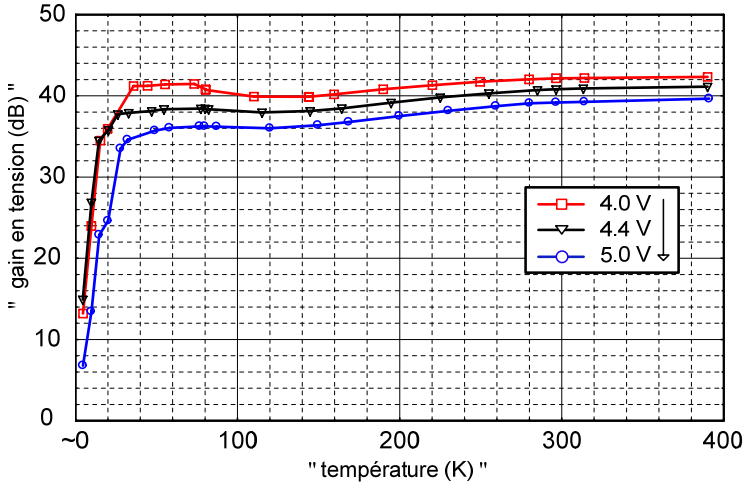


FIG. *i.10*: *Les caractéristiques $G_0(T)$ mesurées pour plusieurs V_{DD} pour l'amplificateur de Type II*

II.4 Conclusion A

Les performances obtenues sur les deux amplificateurs (*Tab i.2*) peuvent être comparées avec les amplificateurs opérationnels d'instrumentation, fonctionnant à la température ambiante [93] ou cryogéniques [68]. Par exemple, notre amplificateur CMOS sans contre-réaction à gain de 40 dB avec la bande passante de 10 MHz est réalisé avec un courant d'alimentation très bas. La réalisation de ces amplificateurs peut être intéressante, comparée aux approches standard, pour l'utilisation en blocks de conception VLSI. La performance acquise convient aux spécifications requises par le banc de test d'imageurs supraconducteurs et semi-conducteurs THz.

TAB. *i.2* : LES PARAMETRES MESURE SUR LES CIRCUITS FABRIQUES (CMOS 0.35 µM)

PARAMETRES MESURES	AMPLIFICATEUR TYPE *I*	AMPLIFICATEUR TYPE *II*
Tension d'alimentation	4.1 V to 5.5 V	3.6 V to 5.5 V
Courant d'alimentation	2.1 mA	1.3 mA[1]
Bande passante (T = 290 K)	10 MHz **(GBW=1GHZ)**	4 MHz at V_{DD} = 5 V
Bande passante (T = 77 K)	17 MHz **(GBW=1.7GHZ)**	10 MHz at V_{DD} = 5 V
Bruit d'entrée (T = 290 K)	5 nV/Hz^{½}	5 nV/Hz^{½}
Bruit d'entrée (T = 77 K)	2 nV/Hz^{½}	3 nV/Hz^{½}
Gain G_0 (T = 290 K)	39.85 dB	39.3 dB pourV_{DD} = 5 V
Δ Gain 270 K − 390 K	– 0.12 dB	– 0.5 dB pour V_{DD} = 4 V
Variation du gain (at T = 77 K)	– 1.2 dB	– 1.3 dB pour V_{DD} = 4 V
Tension d'offset d'entrée	-	500 µV
SR (V/µs)	25	100
THD[2] (V_{out} = 0.3 V_{pp})	1 %	0.03 %

[1] sans l'étage de sortie, [2] Distorsion harmonique totale

tel-00417838, version 1 - 17 Sep 2009

III Filtres de fréquences actifs

Un filtre de fréquence est un élément essentiel dans une chaîne analogique, en vue d'améliorer les paramètres fondamentaux, notamment le rapport signal-à-bruit. De manière générale, pour ce qui concerne les fonctions à bas bruit, un prétraitement analogique est plus avantageux, comparé à traitement numérique. De ce fait, nous consacrerons une partie importante à ce sujet, afin d'améliorer les paramètres des chaines d'amplification de signaux bas niveaux envisagés : la chaîne de détections THz, ainsi d'autres application liés à la thèse (l'étude de qualité des matériaux [116]). Dans ce paragraphe, nous étudierons avant tout l'influence des éléments actifs sur l'atténuation de filtres passe-bas haute fréquence. Nous montrerons qu'une amélioration du taux d'atténuation des circuits peut aboutir à une augmentation de dynamique et une augmentation de la plage de fréquences des filtres actifs. Nous présenterons deux filtres biquadratiques dont l'atténuation haute fréquence est ainsi augmentée : Sallen-Key de *type II*, et une section biquadratique utilisant un CCII- (convoyeur de courant de deuxième génération). Enfin, nous présenterons une conception de CCII- à très hautes performances réalisée en CMOS 0.35 µm.

III.1 L'atténuation des filtres passe-bas

Les filtres passe-bas sont conçus afin de rejeter les fréquences au dessus de la fréquence de coupure F_0. Cependant, la quasi-totalité des filtres actifs dédiés à la synthèse en cascade atteignent une bonne atténuation dans la seule plage de fréquences où les paramètres des éléments actifs (par exemple Amplificateur Opérationnel AO) ne sont pas dégradés. La fonction de transfert des structures « réelles » contient des *zéros parasites* de fréquences f_Z. Ces zéros parasites peuvent causer une remontée de la caractéristique AC pour les fréquences $f > f_Z$. Cette caractéristique aura en effet une pente de 0 dB/decade pour un zéro d'ordre 2, et une pente de + 20 dB/dec pour un zéro d'ordre 3. Il est évident que la pente positive peut aboutir à une atténuation très faible en haute fréquence. Nous allons décrire deux structures qui éliminent cette remontée typique de la caractéristique fréquentielle.

III.2 Sallen-Key de type II

La structure Sallen-Key (S-K) *Fig. i.11* est l'une des structures biquadratiques les plus fréquemment utilisées pour la conception des filtres actifs. La fréquence de coupure et le facteur de qualité Q sont donnés par les équations:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}};\ Q = \frac{\sqrt{C_1}}{\sqrt{C_2}}\frac{\sqrt{R_1 R_2}}{R_1 + R_2} = \frac{1}{2}\sqrt{\frac{C_1}{C_2}}\bigg|_{R1=R2} \tag{i-21}$$

La conception de la structure S-K (sensibilités $S_{\Omega_0,Q} < 1$) demande l'utilisation d'amplificateurs à gain unitaire. Malgré l'utilisation fréquente de cette structure, ses paramètres, notamment l'atténuation, ne sont pas optimaux. Dans cette thèse, nous avons montré qu'un triple pole apparait comme une conséquence des propriétés réelles de l'amplificateur opérationnel. La fréquence du zéro parasite f_Z peut être exprimée ainsi :

$$f_{Z1} \cong \frac{1}{2\pi}\sqrt[3]{\frac{A_0 \cdot \omega_P}{C_1 C_2 R_2 R_{OUT}}}, \tag{i-22}$$

où A_0 et ω_p sont les paramètres du modèle d'AO d'ordre 1 (A_0 est le gain DC et ω_p la fréquence du pole dominant).

Nous pouvons expliquer les origines de ce triple pole *Eq.*(i-22). Comme indiqué sur la *Fig. i.11*, la présence de ce pole est due à une connexion entre l'entrée du filtre et sa sortie. Il est évident que pour les fréquences où les performances de l'AO sont dégradées (notamment la résistance de sortie élevée), le courant à travers la capacité C_1 domine et augmente le transfert du filtre.

tel-00417838, version 1 - 17 Sep 2009

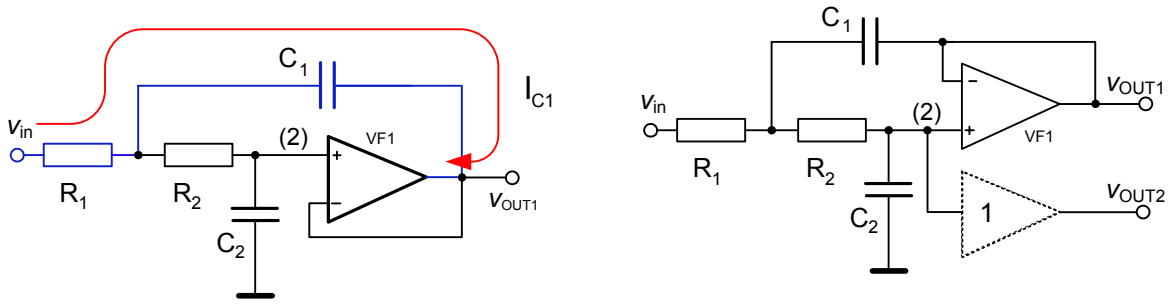


FIG. *i*.11: *a) la section Sallen-Key passe-bas biquadratique avec son transfert parasite. b) S-K de Type I (standard sortie v_{OUT1}) et Type II S-K (v_{OUT2}) avec atténuation augmentée*

Une augmentation de l'atténuation sur les hautes fréquences revient à interrompre ce transfert parasite. D'après la *Fig. i.11 a*), les tensions d'entrée et de sortie du suiveur de tension sont égales. De plus, nous constatons que le transfert inversé de ce suiveur est égal à zéro. Ainsi, le transfert de type passe-bas apparaît à l'entrée du suiveur (nœud (2)). L'atténuation en bande d'atténuation de ce filtre sera augmentée aux hautes fréquences. Ceci peut être montré par une analyse qui donne la fréquence du zéro parasite :

$$f_{N2} \cong \frac{1}{2\pi}\sqrt{\frac{A_0 \cdot \omega_P}{C_1 R_{OUT}}}\,. \qquad \text{(i-23)}$$

Ici, l'ordre du zéro parasite est réduit à 2. Le filtre utilisant le nœud 2 (*Fig. i.11 b*) comme sortie sera appelé filtre Sallen-Key de *Type II*. Pour ce filtre, la fréquence f_Z *Eq.*(i-23) dépend des paramètres du modèle d'AO, ainsi que d'un seul composant passif: C_1.

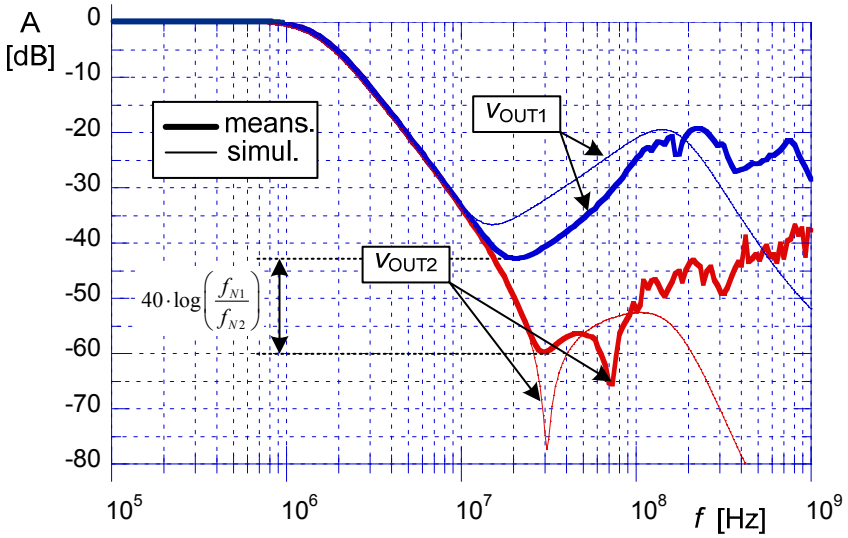


FIG. *i*.12: *Caractéristiques mesurées et simulées du filtre Sallen-Key: Type 1 standard v_{OUT1} et type II (v_{OUT2}) avec une atténuation augmentée (R_1 = 168Ω, R_2 = 100Ω, C_1 = 1.2nF, C_2 = 560pF, OA = AD8055).*

La démonstration de ceci est montrée sur la *Fig i.12* où les transferts v_{OUT1} (*Type I* S-K) et v_{OUT2} (*Type II* S-K) sont mesurés pour un filtre de F_0 = 1.5 MHz et Q = 1/√2, en utilisant un amplificateur opérationnel avec f_T = 300MHz (type AD8055). Sur cette figure, l'atténuation de la version originale de S-K atteint quelques 30 dB en moyenne, alors que pour la version de *Type II* elle atteint 50 dB. De plus, l'équation (i-23) présente une manière simple d'augmenter cette atténuation par le choix du niveau d'impédance du filtre (les simulations ont montré une atténuation jusqu'a -70 dB pour une valeur raisonnable : C_1 = 100 pF).

tel-00417838, version 1 - 17 Sep 2009

III.3 Section CCII sans zéro parasite

Une structure biquadratique n'ayant pas de zéro parasite dans sa fonction de transfert peut atteindre une pente de – 40dB/dec constante dans toute la bande d'atténuation. L'atténuation ne sera alors limitée que par les fuites des signaux parasites. Un moyen d'obtenir une telle atténuation est de séparer la bande de fréquences en deux régions : région de la bande passante où le transfert est assuré par l'élément actif, et la région de la bande d'atténuation (au-dessus de F_0) où l'atténuation est obtenue par un circuit passif.

La mise en œuvre d'un tel principe est montrée sur la *Fig. i.13*. La section biquadratique est composée du convoyeur de courant CCII- [137]. Le signal d'entrée est connecté à la résistance R_1. Le couplage avec le réseau passif est assuré par le transfert entre les borne X et Z : $i_Z = -i_X$. Ce courant est atténué par le réseau passif $R_2 - C_{1,2}$. La sortie du filtre est également l'entrée du suiveur du convoyeur (borne Y). Comme pour le S-K de *Type II*, la sortie est à haute impédance et doit être munie d'un suiveur de tension supplémentaire.

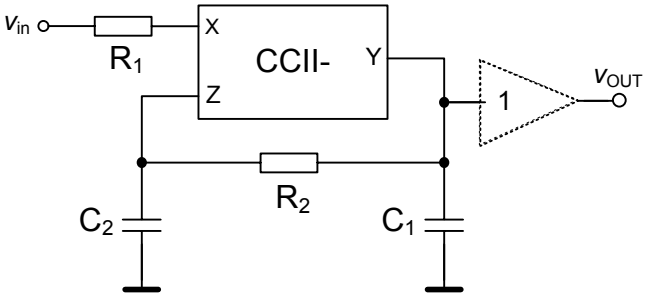


FIG. *i*.13: *La section biquadratique CCII- sans influence parasite en bande de réjection*

La fréquence de coupure et le facteur de qualité Q du circuit *Fig. i.13* sont donnés par les équations suivantes:

$$f_0 = \frac{1}{2\pi\sqrt{R_1 R_2 C_1 C_2}}, \quad Q = \frac{\sqrt{R_2}}{\sqrt{R_1}} \cdot \frac{\sqrt{C_1 C_2}}{C_1 + C_2} = \frac{1}{2} \cdot \sqrt{\frac{R_2}{R_1}}\Bigg|_{C1=C2}. \tag{i-24}$$

Comparé au filtre Sallen-Key, le filtre *Fig. i.13* n'a idéalement pas de zéro parasite dans sa fonction de transfert. Un transfert parasite potentiel entre l'entrée et sortie du filtre est éliminé par le transfert en retour du suiveur entre X et Y, qui vaut idéalement zéro.

Afin d'analyser ces propriétés parasites, un modèle simplifié du CCII va être utilisé. Ce modèle contiendra seulement le suiveur de tension (transfert Y→X) réalisé par un AO (modèle d'ordre 1). Le transfert v_{OUT}/v_{In} du filtre de la *Fig. i.13* peut être exprimé par:

$$N(s) = \frac{\Omega_0^2 \cdot \left(\omega_P \cdot A + s\right)}{\left(s^2 + s \cdot \Omega_0 / Q + \Omega_0^2\right) \cdot \left(\omega_P \cdot (1+\alpha) \cdot A + s\right)}, \tag{i-25}$$

où $s^2 + s \cdot \Omega_0 / Q + \Omega_0^2$ est la fonction de transfert standard d'ordre 2, avec Ω_0 et Q définis par (i-24), et le coefficient $\alpha = R_{OUT}/R_2 << 1$. Cette fonction montre que le seul zéro au numérateur est compensé par un pôle de fréquence très voisine. La structure a donc un transfert idéalement de -40dB/decade, limité en pratique seulement par les fuites parasites du signal.

Afin de confirmer la forte atténuation de la structure biquadratique *Fig. i.13*, un exemple de filtre passe-bas de $F_0 = 10$ MHz d'ordre 4^{th} (Butterworth) a été réalisé à l'aide du circuit CCII-K [127] (ce circuit permets de réaliser un CCII- avec les éléments discrets commerciaux).

La caractéristique mesurée montre une forte atténuation allant jusqu'à 100 dB à 100 MHz. Une telle atténuation est en générale seulement observé sur des structures passives.

tel-00417838, version 1 - 17 Sep 2009

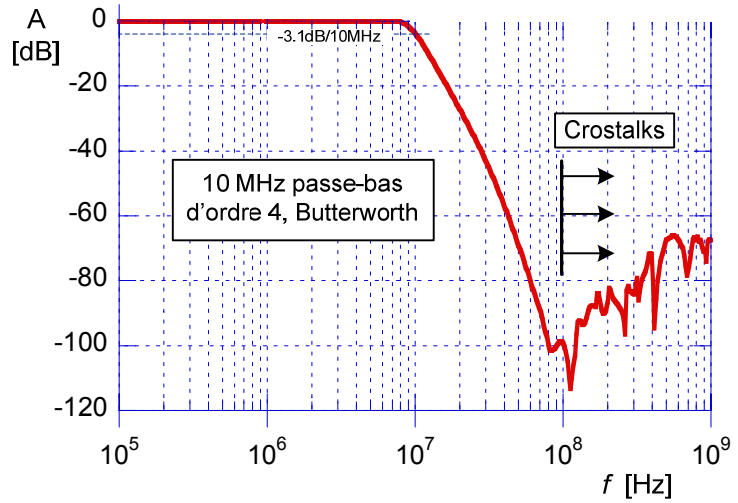


FIG. *i*.14: *L'exemple du transfert AC du filtre passe-bas de 10 MHz d'ordre 4, réalisé avec la structure biquadratique Fig. i.13 et le circuit CCII-K [127] (OPA860+AD8055)*

III.4 Convoyeur de courant CCII

Afin de mettre en pratique le filtre biquadratique présenté dans le paragraphe précédent, le convoyeur de courant doit être réalisé sous la forme d'un circuit intégré. Dans cette section, nous allons présenter la structure du CCII intégré et fabriqué en technologie CMOS 0.35 µm. La structure du CCII est optimisé afin d'obtenir une impédance de sortie très faible à haute fréquence $R_{(X)}$.

Structure CMOS de CCII-

Par les équations (i-22), (i-23), nous avons montré l'importance de la résistance des sorties de tension vis-à-vis les propriétés en bande atténué. Comme montré pour la section biquadratique *Fig. i.13*, l'influence de cette résistance est négligeable (*Eq.*(i-25)). Néanmoins, notre développement est focalisé notamment sur l'obtention d'une résistance de sortie $R_{(X)}$ basse, afin de pouvoir valoriser le circuit du CCII dans d'autres structures en mode courant (par exemple zéro-offset FDNR à pertes [132]).

Parmi les étages de sortie connus et publiés, nous avons choisi le circuit utilisé en [91], qui a été adapté pour l'utilisation comme suiveur de tension en CCII.

Nous présentons le circuit du CCII sur la *Fig. i.15*. Sur cette figure, la circuiterie placée à gauche représente le suiveur de tension (bornes X, Y), alors que la partie droite représente la sortie en courant (borne Z). L'optimisation de cette structure a été effectuée par les analyses mathématiques sur un schéma linéaire. Pour cette analyse, les principaux transistors ont été identifiés, dont les paramètres (points de repos) doivent être optimisés. Notamment, M_i, M_{o1}, M_{o2} et M_{b1}.

Fonctionnement du suiveur de tension

La borne d'entrée du suiveur est X, et la borne de sortie Y. Sur la *Fig. i.15* le transistor M_i est le transistor d'entrée, M_f le transistor de contre-réaction et les $M_{o1,2}$ sont les transistors de sortie. Les transistors de polarisation sont marqués $M_{b,x}$.

Dans la structure, les transistors M_i et M_f sont polarisés par des courants I_D identiques et constants $I_{b(2)}/2$ (*Fig. i.15*). Le nœud de drain de M_i est le point de haute impédance. La tension de ce nœud commande les transistors de sortie par l'intermédiaire de M_{b4}. Le fait que M_f et M_i soient polarisés avec les mêmes courants constants fait apparaître leurs tensions V_{GS} comme égales. De ce fait, l'égalité des tensions d'entrée et de sortie, ainsi que le gain unitaire sont atteintes. Les transistors M_{m1} et M_{m4} mesurent le courant de sortie I_X, qui est ensuite transféré vers la sortie Z, par l'intermédiaire des miroirs de courants M_{m2}-M_{m3} et M_{m5}-M_{m6}.

tel-00417838, version 1 - 17 Sep 2009

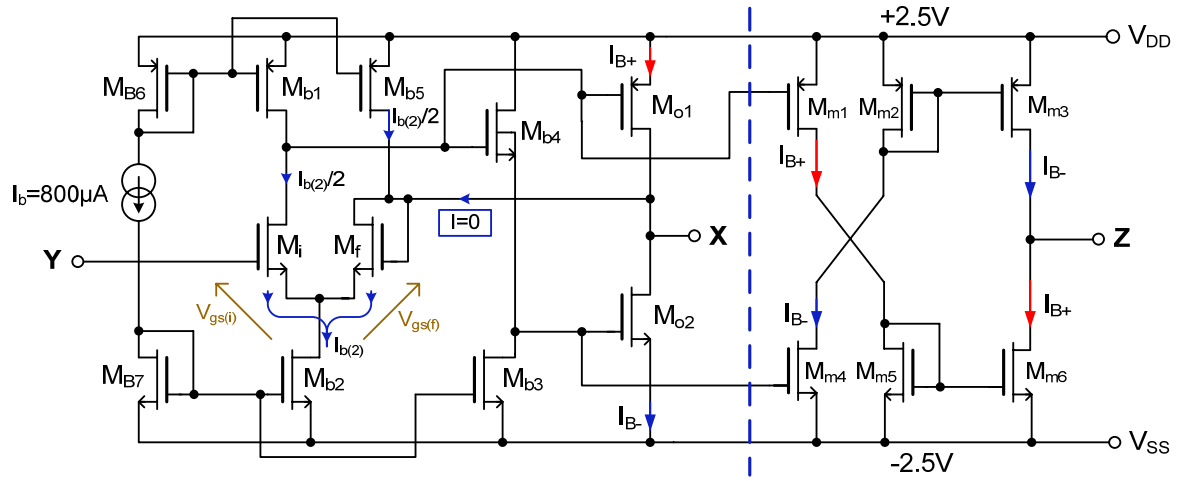
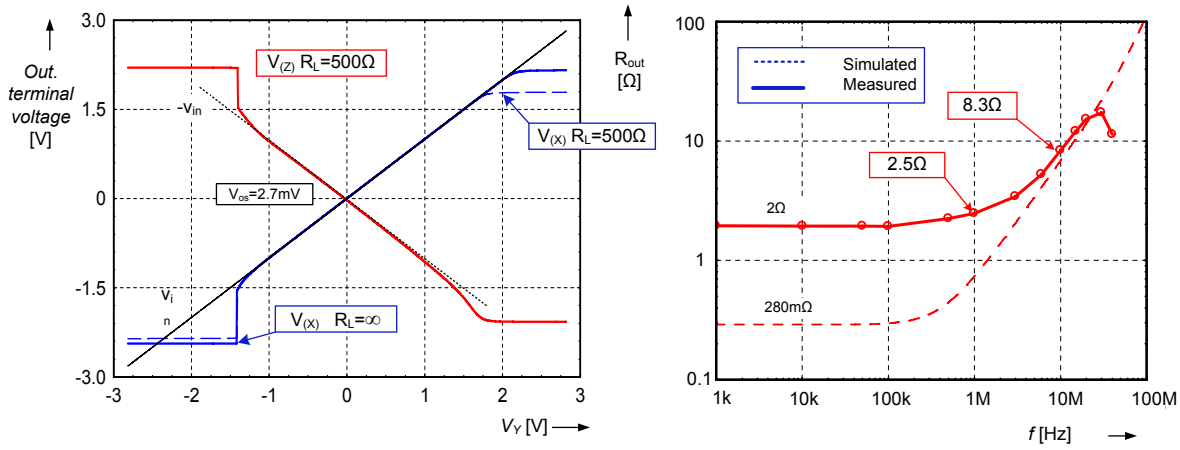


FIG. *i*.15 *: Le circuit final du convoyeur de courant CCII-*

Les caractéristiques obtenues

Le circuit a été fabriqué en technologie CMOS 0.35 µm et a été testé en vue de vérifier les fonctions DC et AC. La caractéristique principale est montrée sur la *Fig. i.16 a*). Sur cette figure, nous pouvons évaluer les propriétés statiques : les transferts entre tous les terminaux. Pour ce faire, une tension en dents de scie de -2.5 à +2.5 V a été appliquée à l'entrée Y. La tension de sortie V_X a été mesurée avec sur la borne X : *i*) sans charge et ii) avec la charge $R_{(X)} = R_{(Z)} = 500\ \Omega$. Comme défini par la fonction de CCII, les tensions V_X et V_Z doivent être identique pour la même charge, à cause de l'égalité $I_X = I_Z$. Ceci est montré sur la *Fig. i.16*).

Le courant de consommation statique du convoyeur est de 11 mA et le courant maximal I_X et I_Z de ± 20 mA).



a) *b*)

FIG. *i*.16*: a) Fonction de transferts DC mesurés: transfert Y→X pour la borne X sans charge et avec une charge de 500 Ω, transfert du courant X→Z pour X et Z chargé avec les résistors appariés de 500 Ω b) la résistance de sortie $R_{(X)}$ en fonction de la fréquence*

La caractéristique *Fig. i.16 b*) montre la dépendance de la résistance de sortie $R_{(X)}$ en fonction de la fréquence. Nous observons une résistance de 2.5 Ω à 1 MHz et 8.3 Ω à 10 MHz. Ces résultats sont très intéressants si on le compare avec des résultats publiés (par exemple [144], [145]), y compris les circuits intégrés en technologie bipolaire. Ceci justifie le choix de l'architecture ainsi que l'optimisation effectuée sur le circuit du suiveur de tension.

tel-00417838, version 1 - 17 Sep 2009

III.3 Conclusion B

Les structures biquadratiques introduites dans cette section offrent un moyen d'améliorer les propriétés des filtres vers les hautes fréquences grâce à une optimisation focalisée sur le transfert en bande d'atténuation. L'objectif a été d'éliminer le rôle d'éléments actifs aux hautes fréquences, où l'atténuation est assurée seulement par les éléments passifs. Ces structures ont montré une amélioration significative de l'atténuation, ce qui permet leurs utilisations pour les fréquences de coupure F_0 plus élevées.

Malgré cette amélioration, la présence d'un suiveur supplémentaire peut être considérée comme un inconvénient. Cependant, un élément ayant une fréquence f_T relativement basse (c'est-à-dire un élément à basse consommation et coût) peut être utilisé (le suiveur supplémentaire doit assurer le transfert seulement jusqu'à la fréquence F_0). De plus, ce suiveur peut être évité par la connexion directe à une entrée à haute impédance, par exemple une entrée de convertisseur CAN.

Afin de pouvoir utiliser la section biquadratique, le convoyeur de courant CCII a été développé. Ses performances ont été optimisées par un choix judicieux de l'architecture du suiveur de tension et son optimisation. Les propriétés obtenues sur le circuit réalisé en CMOS 0.35 µm confirme notre approche : par exemple la résistance $R_{(X)}$ a été mesurée comme étant particulièrement basse: 2.5 Ω à la fréquence 1 MHz et 8.3 Ω à 10 MHz.

Les exemples des caractéristiques mesurées confirment les bonnes performances des filtres concernant l'atténuation sur les hautes fréquences. L'optimisation de la bande d'atténuation peut ainsi améliorer les performances des circuits, en utilisant des composants standards (par exemple basse consommation), ou atteindre des fréquences F_0 plus élevées.

tel-00417838, version 1 - 17 Sep 2009

Bibliographic resources cited or related to the thesis

[1] P.H. Siegel, "*Terahertz technology*", IEEE Transactions on microwave theory and techniques, Volume 50, Issue 3, March 2002 Pages: 910 - 928

[2] T. Maya, S. Andersa, V. Zakosarenkoa, M. Starkloff, H.-G. Meyera, G. Thorwirthb, E.Kreysac, N. Jethavac, "*A Superconducting Terahertz Imager*", IEEE/CSC & ESAS European Superconductivity News Forum, No.A, July 2007

[3] After A. Dégardin, Internal repport of NanOtime research group activity

[4] W. J. Spiesman, M. G. Hauser, T. Kelsall, C. M. Lisse, S. H. Moseley Jr., W. T. Reach, R. F. Silverberg, S. W. Stemwedel, & J. L. Weiland, "*Near and far infrared observations of interplanetary dust bands from the COBE diffuse infrared background experiment*", Astrophysical Journal 442 (1994)

[5] Planck homesite at Europen Space Agency website (2007): http://www.rssd.esa.int (2008)

[6] K.Humphreys, J.P. Loughran, M.Gradziel, W. Lanigan, T. Ward, J.A. Murphy, C. O'Sullivan, " *Medical applications of terahertz imaging: a review of current technology and potential applications in biomedical engineering",* Engineering in Medicine and Biology Society, 2004. IEMBS '04. 26th Annual International Conference of the IEEE, Volume: 1, 1302-1305, Sept. 2004

[7] ULIS website : http://www.ulis-ir.com (2008)

[8] C. Constancias, R.E. de Lamaestre, O. Louveau, P. Cavalier, J.-C. Villégier, "*Patterning issues in superconducting nanowire single photon detector fabrication*", J.Vac. Sci. Technol. B accepted for publication (2007)

[9] D. Chouvavev, "*Normal metal hot electron microbolometer*", PhD thesis, Chalmers University of Technology 2001, ISBN 97-7291-024-0

[10] A. Adam, A. Gaugue, C. Ulysse, A. Kreisler, C. Boulanger, "*Three-temperature model for hot electron superconducting bolometers based on high-T/sub c/ superconductor for terahertz applications*" IEEE Transactions on Applied Superconductivity, , Volume 13, Issue 2, Part 1, June 2003, Page(s):155 - 159 ; See also: A. Adam, "*Bolomètres à électrons chauds supraconducteurs pour la détection des ondes submillimétriques: modélisation et caractérisations*", PhD thesis Paris 6 University, 2003, in French

[11] J. Bardeen, L. N. Cooper, and J. R. Schrieffer, "*Theory of superconductivity*", Physical Review 108 (5), 1175 (1957)

[12] E. M. Gershenzon, M. E. Gershenzon, G. N. Gol'tsman, A. M. Lyul'kin, A. D. Semenov, and A. V. Sergeev, "*Electron-phonon interaction in ultrathin Nb films*", Sov. Phys. JETP, vol. 70, no. 3, pp.505–511, 1990

[13] S. E. Schwartz, B.T Ulrich, "*Antenna-coupled infrared detector*", Journal of applied physics, 48(5): 1870-1873, May 1997

[14] Netherlands Institute of Space Research, website: http://sron.nl (2007)

[15] The KOSMA 3m submillimeter telescope, website: www.astro.uni-koeln.de (2008)

[16] E. M. Gershenzon, G. N. Gol'tsman, I . G. Gogidze, Y. P. Gusev, A. I. Elant'ev, B. S. Karasik, and A. D. Semenov, "*Millimeter and submillimeter range mixer based on electronic heating of superconducting films in the resistive state*", Sov. Phys.-Superconduct., vol. 3., pp 1582-1597, 1990

[17] K. Kroug, "*NbN Hot electron bolometer mixer for a quasi-optical THz Receiver*", PhD thesis, Chalmers University of Technology, Sweden, 2001

tel-00417838, version 1 - 17 Sep 2009

[18] Yuriy B. Vachtomin, Matvey I. Finkel, Sergey V. Antipov, Boris M. Voronov, Konstantin V. Smirnov, Natalia S. Kaurova, Vladimir N. Drakinski and G. N. Gol'tsman, "*Gain bandwidth of phononcooled HEB mixer made of NbN thin film with MgO buffer layer on Si*", 13th Int. Symp. on Space Terahertz Tech., Harvard University, March 2002, pp. 259-270

[19] C. Ulysse, "*Bolomètres à électrons chauds à supraconducteurs haute température critique pour les ondes, submillimétriques Elaboration et caractéristisations*", PhD thesis at Paris 6 University, 2003, in French

[20] C. Cabrera "*Cryogenic detectors based on superconducting transition edge sensors for time-energy resolved single-photon counters and for dark matteer searches*", Physica B 46A, New York, 1999, pp. 651-654

[21] A.J. Kreisler, A. Gaugue, "*Recent progress in high-temperature superconductor bolometric detectors: from the mid-infrared to the far-infrared (THz) range*", Superconductor Science and Technology, vol 13, pp 1235-1245, 2000

Chapter 2

[22] R. Jacob Baker, Harry W. Li, David E. Boyce, "*CMOS Circuit Design, Layout, and Simulation*", ISBN: 0780334167 Publisher: Wiley-IEEE Press (1997)

[23] Thomas H. Lee, " *A rewiev of MOS device phisic*", document of Harvard course EE214, 2001

[24] Etienne Sicard, Sonia Bendhia, "*Basic CMOS cell Design*", Mc Graw Hill, November 2006

[25] G. Massobrio and P. Antognetti, "*Semiconductor Device Modeling with Spice"*, 2nd edition, McGraw-Hill, 1993

[26] I.E Opris. Kovacs, G.T.A, "*Large-signal subthreshold CMOS transconductance amplifier*",Electronics Letters, Volume 31, Issue 9, 27 April 1995 Page(s):718 – 720

[27] Rong, B. Nanver, L.K.; Burghartz, J.N. Jansman, A.B.M. Evans, A.G.R. Rejaei, B.S, "*C-V characterization of MOS capacitors on high resistivity silicon substrate*", European Solid-State Device Research, 2003. ESSDERC '03. 33rd Conference on 16-18 Sept. 2003 Page(s):489 – 492

[28] Christian Piguet, "*Low-Power CMOS CircuitsTechnology, Logic Design and CAD Tools*", CRC Press 2005 ISBN 0849395372

[29] Murphy, B.T, "*Unified field-effect transistor theory including velocity saturation*", Solid-State Circuits, IEEE Journal of Volume 15, Issue 3, Jun 1980 Page(s):325 – 328

[30] Vancaillie, L. Silveira, F. Linares-Barranco, B. Serrano-Gotarredona, T. Flandre, "*MOSFET mismatch in weak/moderate inversion: model needs and implications for analog design*.", Solid-State Circuits Conference, 2003. ESSCIRC '03. Proceedings of the 29th European 16-18 Sept. 2003 Pages: 671 – 674

[31] J.-P. Eggermont, D. De Ceuster, D. Flandre, B. Gentinne, P.G.A. Jespers, J.-P. Colinge, "*Design of SOI CMOS operational amplifiers for applications up to 300°C*", IEEE Journal of Solid-State Circuits, Volume 31, Issue 2, Feb. 1996 Pages:179 – 186

[32] M. Bucher, C. Lallement,; C. Enz, F. Krummenacher, "*Accurate MOS modelling for analog circuit simulation using the EKV model*", IEEE International Symposium on Circuits and Systems, ISCAS '96, Volume 4, 12-15 May 1996 Pages: 703 - 706

[33] Matthias Bucher, Christophe Lallement, Christian Enz, Fabien Théodoloz, François Krummenacher: "*The EPFL-EKV MOSFET Model Equations for Simulation*" Technical Report, Electronics Laboratories, Swiss Federal Institute of technology (EPFL), Lausanne, Switzerland, Model version 2.6, June, 1997

[34] "*Tri-Gate Transistor Moving from Research to Development*", Intel application note, http://www.intel.com/technology/magazine/silicon/si07031.pdf (2008)

tel-00417838, version 1 - 17 Sep 2009

[35] Robert S. Chau, Intel Senior Fellow, "*Integrated CMOS Tri-Gate Transistors: Paving the Way to Future Technology Generations*" http://www.intel.com/technology/magazine/silicon/tri-gate-transistors-0806.htm (2008)

[36] J. Gautier, M. Sanquer, X. Jehl "*Single electronics: potentialities and issues*" Invited talk, 8th International Conference on Solid-State and Integrated-Circuit Technology (ICSICT - 2006) ,Sanghaï Chine

[37] J. R. Tucker, *Complementary digital logic based on the Coulomb blockade"* Journal of Applied Physics - Volume 72, Issue 9, pp. 4399-4413,November, 1992

[38] Image: L.J. CHEN, "*Metal Silicides: An Integral Part of Microelectronics*", JOM journal of the Mineral, Metals and materials society, Vol. 57, No.9, pp. 24-31

Chapter 3

[39] C. D. Motchenbacher, J. A. Connelly, "*Low-Noise Electronic System Design*", ISBN: 978-0-471-57742-3. Hardcover. 422 pages. June 1993

[40] Paul Horowitz , Winfield Hill, "*The Art of electronics*" Book, Cambridge University Press; 2 edition (July 28, 1989)

[41] Van der Ziel, A, "*Noise in solid-state devices and lasers*" Proceedings of the IEEE, Volume 58, Issue 8, Aug. 1970 Pages: 1178 – 1206

[42] Frederick Reif, "*Fundamentals of Statistical and Thermal Physics*" McGraw-Hill Statistical mechanics , pp. 589 – 594, 1965

[43] Van der Ziel, A, "*Unified presentation of 1/f noise in electron devices: fundamental 1/f noise sources*" Proceedings of the IEEE, Volume 76, Issue 3, Mar 1988 Page(s): 233 – 258

[44] P.H. Handel, "*Fundamental quantum 1/f noise in semiconductor devices Electron Devices*", IEEE Transactions on, Volume 41, Issue 11, Nov 1994 Page(s):2023 - 2033

[45] M. Haartman, "*Low-frequency noise characterization, evaluation and modeling of advanced Si- and SiGe-based CMOS transistors*", PhD Thesis KTH, Dpt. of Microelectronics and Information Technology, 2006

[46] R.P. Jindal, "*Compact Noise Models for MOSFETs*". IEEE Transactions on Electron Devices, Volume 53, Issue 9, Pages: 2051 – 2061, Sept. 2006

[47] Kent H. Lundberg "*Noise Sources in Bulk CMOS*", Master courses of Massachusetts Institute of Technology, http://web.mit.edu/ (2008)

[48] A. L. McWhorter, "*Noise and related surface effects in germanium*", Repport published by Lincoln Lab Rep. 80, Boston, MA, May 1955

[49] F. N. Hooge, and. L. K. J. Vandamme, "*Lattice scattering causes 1/f noise*," Phys. Lett. A, vol. 66, p. 315, 1978

[50] Wang, A. Svizhenko, K.L. Bandyopadhyay, A. "*The fundamental 1/f noise and the Hooge parameter in semiconductor quantum wires Balandin"*,. Electron Devices, IEEE Transactions on Volume 46, Issue 6, Jun 1999 Page(s):1240 – 1244

[51] P. Vavřín, " *Linear control theory (Teorie automatického řízení I)*". book, Brno, VUT 1991 (in czech)

[52] D. Kugelstadt, "*Auto-zero amplifiers ease the design of high-precision circuits*", application note SLYT204, www.ti.com

[53] J. C. Gallop, "*Superconducting Devices*.", Science, Volume 254, Issue 5034, pp. 1052-1053, 1991

[54] Picture from the cours of supraconductivity, Website Ecole Plytechnique Federale de Lasanne, Switzerland, http://lanoswww.epfl.ch (2008)

tel-00417838, version 1 - 17 Sep 2009

[55] K. Brock, "*RSFQ Technology: circuit and system darren HYPRES*", Hypres publication, www.hypres.com

Chapter 4

[56] website of LGEP Nanotime project: http://nanotime.lgep.supelec.fr. see also http://madelec.lgep.supelec.fr/mdmi/ (2008)

[57] Fabrice Voisin, "*Integration d'une électronique analogique à faible niveau de bruit sous la forme de circuit ASIC en technologie CMOS pour la mis en oeuvre de detecteurs bolmetriques à supraconducteurs HTC* " PhD thesis UPMC Paris 6, 2002

[58] Damien Prele, "*Instrumentation Cryogénique Bas Bruit et Large Bande en Technologie SiGe*" , PhD thesis UPMC Paris 6, 2006

[59] T. Adrian. Lee, L.P. Richards, S. W. Nam, B. Cabrera, K. D. Irwin, "*A superconducting bolometer with strong electrothermal feedback*",Applied Physycal Letters. 69, 1801 (1996)

[60] See the document at ULIS website (2008): www.**ulis-ir**.com/

[61] M. Kiviranta, H. Seppä, J. van der Kuur, and P. de Korte, "*SQUID-based readout schemes for microcalorimeter arrays*," in Proceedings of the 9th International Workshop on Low Temperature Detectors (LTD-9), AIP Conference Proceedings, vol. 605, 2002, pp. 295–300.

[62] J. Yoon et al, "*Single superconducting quantum interference device multiplexer for arrays of lowtemperature sensors*", Applied Physycal Letters 78, pp. 371-373 (2001).

[63] K Warwick *"An introduction to control systems",* Second Edition, Singapore: World Scientific, Chapter 5, *pp. 137-196.* ISBN 9810225970

[64] H. Calleja "*An approach to amplifier frequency compensation*". IEEE Transactions on Education 2003; 46(1):43-49.

[65] Ka Nang Leung, P.K.T. Mok, "*Nested Miller compensation in low-power CMOS design*", IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing, Volume: 48, Issue: 4, Apr 2001

[66] Christopher Kilian (2005). "*Modern Control Technology"*. Thompson Delmar Learning. ISBN 1-4018-5806-6

[67] I. Koudar, "*Variable gain differential current feedback amplifier*", Custom Integrated Circuits Conference, 2004. Proceedings of the IEEE 2004 3-6 Oct. 2004 Page(s):659 – 662

[68] Z. Švindrycha, Z. Janůb, F. Soukupb and R. Tichýb,"*Operational amplifiers operating in temperature range from 300 to 4.2 K*", Cryogenics, Volume 48, Issues 3-4

[69] Giovanni Anelli , Kurt Borer, Luca Casagrande, Matthieu Despeisse, Pierre Jarron, Nicolas Pelloux and Shahyar Saramad "*A high-speed low-noise transimpedance amplifier in a 0.25 μm CMOS technology*" Nuclear Instruments and Methods in Physics Research Volume 512, Issues 1-2, 2003

[70] Comer DT. "*A wideband integrated circuit amplifier for fixed-gain applications*". Analog Integrated Circuits and Signal Processing 1996;11(3):243-251

Chapter 5-8

[71] Mangelsdorf, C.W "*A variable gain CMOS amplifier with exponential gain control*",VLSI Circuits, 2000. pp 146-149, ISBN: 0-7803-6309-4, 2000

[72] Naktongkul, P.; Thanachayanont, A.; "*1.5-V 900-/spl mu/W 40-dB CMOS variable gain amplifier*", Circuits and Systems, 2006. ISCAS 2006. Proceedings. 2006 IEEE International Symposium on 21-24 May 2006 Page(s):4 pp

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

[73] Grafe, M. Oehm, J. Schumacher, K. "*A wide range dB-linear variable gain CMOS amplifier*", Solid-State Circuits Conference, 1997. ESSCIRC '97 Publication Date: 16-18 Sept. 1997

[74] Ja Chun Ku, Yehea Ismail, "*A Compact and Accurate Temperature-Dependent Model for CMOS Circuit Delay*", IEEE International Symposium on Circuits and Systems, 2007. ISCAS 2007

[75] Young, K.K.; Tsaur, B.-Y."*Operation of SOI CMOS devices at liquid-nitrogen temperature*", Electron Device Letters, IEEE Volume 11, Issue 3, March 1990

[76] K.S. Kalonia, F.C.Jain, "*A two-dimensional analytical model for MOSFETs operating at 77 K*" University/Government/Industry Microelectronics Symposium, June 1989

[77] J.W. Schrankler, J.S.T. Huang, Lutze, R.S.L. Vyas, H.P. Kirchner, "*Cryogenic behavior of scaled CMOS devices*" Electron Devices Meeting, 1984

[78] Tianbing Chen, "*Operation of SiGeBiCMOSTechnology Under Extreme Environments*", PhD Thesis, Georgia Institute of Technology, 28 Nov 2005

[79] A. Osman, M. Osman, N. Dogan, and M. Imam, "*An extended tanh law MOSFET model for high temperature circuit simulation*" JSSC,pp. 147-150, 1995

[80] G. Klisnick, Y. Hu, F. Voisin. M. Redon, A. Gaugue, A. Kreisler, "*A low noise cryogenic CMOS preamplifier for high critical temperature superconducting IR and FIR sensors*" Proceedings of the 24th Europea Solid-State Circuits Conference, 1998. ESSCIRC '98. Sept. 1998

[81] S. M. Sze, "*Physics of Semiconductor Devices*". New York: Wiley, 1983

[82] K. Kato, T. Wada, and K. Tanigushi, "*Analysis of kink characteristics in silicon on insulator MOSFETs using two carrier modeling*," IEEE Trans. Electron Devices, vol. ED-32, p. 458, 1985.

[83] Bretscher, Otto."*Linear Algebra With Applications",* 3rd editionn.. Upper Saddle River NJ: Prentice Hall, 1995

[84] http://mathworld.wolfram.com see the note abot Least Squares Fitting (2008)

[85] AMS 0.35 µm design kit for Cadence® Company document

[86] John M. Miller, "*Dependence of the input impedance of a three-electrode vacuum tube upon the load in the plate circuit*", Scientificc Papers of the Bureau of Standards, 15(351):367{385, 1920.

[87] KD. Peterson, RL. Geiger "*Area/bandwidth tradeoffs for CMOS current mirrors*". IEEE Transactions on Circuits and Systems 1986;CAS-33(6):667-669.

[88] C. Hill, Y. Sun, S. Szczepanski ,"*Low noise, low distortion, high frequency, fully differential CMOS transconductor*", The 2000 IEEE Asia-Pacific Conference on Circuits and Systems, 2000. IEEE APCCAS 2000

[89] Katsuji Kimura, "*A linear CMOS transconductance element of an adaptively biased source-coupled differential pair using a quadritail cell*", Analog Integrated Circuits and Signal Processing octobre 1996

[90] E. Seevinck, R.F. Wassenaar, "*A versatile CMOS linear transconductor/square-law function*" IEEE Journal of Solid-State Circuits, Volume 22, Issue 3, Jun 1987

[91] Hassan O. Elwan, Mohammed Iqbal Younus, Hussein A. Al-Zaher, and Mohammed Ismail,"*A Buffer-Based Baseband Analog Front End for CMOS Bluetooth Receivers*", IEEE transaction on Circuit and Systels II, Vol. 49n No. 8, August 2002

[92] I. M. Hafez, G. Ghuibaudo, F. Balestra, "*Analysis of the kink effect in MOS transistors*", IEEE. transactions on electron devices, 1990

[93] Website of fabricants: for instance: www.analog.com, www.linear.com, www.ti.com

Chapter 8

[94] Lawrence P. Huelsman, "*Active and Passive Analog Filter Design: an Introduction*", McGraw-Hill Education, ISBN: 0070308616, book Published: March 1993

[95] K. Hájek, J.Sedláček, "*Kmitočtové filtry*". BEN, Praha, 2002

[96] Y. Nakazawa, "*High Frequency Crystal Electromechanical Filters*", 16th Annual Symposium on Frequency Control. 1962, pp 373-390

[97] D.M. Pozar,"*Microwave eingienering*", Willey 2005

[98] Levy, R., Snyder, R.V. and Matthaei, G. "*Design of microwave filters*", IEEE Trans. Microwave Theory Tech., vol. MTT-50, pp. 783–793, Mar. 2002

[99] S. Winkler, "*The Approximation Problem of Network Synthesis Circuit Theory*", IRE Transactions on Volume 1, Issue 3, Sep 1954 Pages:5 - 20

[100] George S. Moschytz, " *Linear Integrated Networks*", Van Nostrand Reinhold. New York, 1975

[101] J.M. ROLLET "*Active filter using a predistorsion technique*", Electronics Letters, P. 25-26, 1968

[102] J.M. Rollett, "*Economical RC active lossy ladder filters*", Electronics Letters, Volume: 9, Issue: 3 On page(s): 70-72, 1973

[103] R.E. Massara, "*Design considerations for lowpass and highpass all-pole f.d.n.r. networks*", Electronics Letters, Volume 14, Issue 7, March 30 1978 Page(s): 225 - 226

[104] K. Hájek, J.Sedláček, "*Lossy LC Ladder Prototypes and their use for ARC Filter Optimization*", WSEAS TRANSACTIONS on ELECTRONICS, Issue3, Volume2, July 2005, pp. 94-99,ISSN 1109-9445

[105] P. Martínekm D. Tichá "*Evolutionary algoritmes by ARC filter synthesis*", ECCTD 05, Cork, 2005,pp.155-159

[106] S.C. Roy Dutta, "*A circuit for floating inductance simulation*", Proceedings of the IEEE, Volume 62, Issue 4, April 1974 Page(s):521 – 523

[107] A. Antoniou, " *Novel RC-active-network synthesis using generalized- immittance converters*", Circuits Theory, IEEE Transactions on, May 1970 ISSN: 0098-4094.

[108] S. Mitra, N.Herbst, "*Synthesis of Active RC One-Ports Using Generalized Impedance Converters*", Circuits Theory, IEEE Transactions on [legacy, pre - 1988], Volume 10, Issue 4, Dec 1963 Page(s):532 - 532

[109] L. T. Bruton, "*Filter synthesis using generalized impedance converters*," NATO Institute of Advanced Signal and Network Theory, Bournemouth, England, Sept. 1972

[110] L. T. Bruton, "*Network transfer functions using the concept of frequency-dependent negative resistance*," IEEE Trans. Circuit Theory, vol. CT-16, pp. 406-408, Aug. 1969

[111] D.Youla, "*A New Theory of Cascade Synthesis, Circuit Theory*", IRE Transactions on, Volume 8, Issue 3, Sep 1961 Page(s):244 – 260

[112] V. Michal, K. Hájek, J.Sedláček "*The Analog Filter Design and Interactive Analog Signal Processing by PC Control*", In Applications of Electrical Engineering AEE 05,. Prague: WSEAS, 2005. s. 119-122. ISBN: 960-8457-13-0.

[113] Final report of the Grant 102/03/1181 and 102/04/0442, Grant Agency of the Czech Republic

[114] K. Hájek, J.Sedláček, B. Sviezeny, "*The New Universal Tunable Biquad with optimization for the High Frequency Band",* In the proceedings of the XI. International Symposium on Theoretical Electrical Engineering ISTET´01. Linz 2001, pp. 139 – 142.

tel-00417838, version 1 - 17 Sep 2009

[115] Analog devices, datasheet AD 7533, www.analog.com (2008)

[116] Hajek, K. Korenska, M. and Sikula, J, "*Nonlinear Ultrasonic Spectroscopy of Fired Roof Tiles*", World Conference on NDT, Montreal, Canada, Aug 30 - Sep 3, 2004

Chapter 9

[117] A.Sedra, J. Espinoza, "*Sensitivity and frequency limitations of biquadratic active filters*", Transactions on Circuits and Systems, IEEE, Volume: 22, Issue: 2, Feb 1975

[118] R. Padukone, Mohammed S. Ghausi, "*A comparative study of multiple amplifier active RC biquadratic sections"*, International Journal of Circuit Theory and Applications, Volume 9 Issue 4, Pages 431 – 459, Dec 2006

[119] P. R. Geffe, "*Exact synthesis with real amplifiers*", IEEE Trans., Vol. CAS-23, pp.45-55, January 1976

[120] R.P. Sallen, E.I. Key, "*A practical method of Designing RC-Active Filters*". IEEE Trans. Circuit Theory. Vol. 7. CT-2, March 1955, p. 74-85.

[121] D.J. Perry, "*New multiple feedback active RC network*", Electronics Letters, Volume: 11, Issue: 16, On pages 364-365, August 1977

[122] H. Schmid, G.S. Moschytz, "*Fundamental frequency limitations in current-mode Sallen-Key filters*", Circuits and Systems, 1998., p. 57-60 vol.1, June 1998. See also: J. Punčochář, "*Low-Pass Filters SALLEN and KEY With Real Operational Amplifiers*", Elektrorevue, Int. journal VUT, 2005/10, http://www.elektrorevue.cz

[123] K. Soundarajan, "*Nonideal performance of single amplifier simulated frequency dependent negative resistances*" IEEE Transactions on Circuits and Systems,Volume 23, Issue 9, Page(s):573 – 577, Sep 1976

[124] Shen-Ivan Liu; Hen-Wai Tsao; Jingshown Wu; Jiann-Horng Tsay;, "*Realizations of the single CCII biquads with high input impedance"*, IEEE International Sympoisum on Circuits and Systems, 1991, Pages:1428 - 1431 vol.3, June 1991

[125] L. T Bruton, "*Nonideal performance of two-amplifier positive impedance converters*", ibid., 1970, CT-17, pp. 541-549

[126] C. Toumazou, F. J. Lidgey, D. G. Haigh "*Analogue IC Design*: *The Current-Mode Approach"*, Book, EII Circuits and Systems Series, 1993, ISBN-10: 0863412971

[127] Long Wan; Natarajan, S. "*Optimal design of CCII-K circuits for high frequency applications*", System Theory, Mar 1995, p. 175 – 179

[128] V. Michal, "*BCC1, BCC1, software tools developped for education purpouses ad DTEE brno University of Technology*", 2002, www.utee.feec.vutbr.cz/, www.postreh.com/vmichal/

[129] H. Nevarez-Lozano, J.A.Hill, E. Sanchez-Sinencio,"*Frequency limitations of continuous-time OTA-C filters*" IEEE International Symposium on Circuits and Systems, 1988. S.C. Dutta

[130] Roy, K.K. Malik, "*Active RC realisation of a 3rd-order lowpass Butterworth characteristic*,"Electronics Letters -- 28 December 1972 -- Volume 8, Issue 26, p. 630-631

[131] L. P. Huelsman, *"Equal-valued-capacitor active-RC-network realisation of a 3rd-order lowpass Butterworth characteristic*", Electronnics Letters, 1971, 7, pp. 271-272

[132] P. Martinek, "*Lossy FDNR based on CCII- current conveyor*", Proceding on internatinal conference Radioelektronika, Brno, 2006

[133] Long Wan, S. Natarajan, "*Optimal design of CCII-K circuits for high frequency applications*," ssst,pp.175, 27th Southeastern Symposium on System Theory (SSST'95), 1995

[134] "*Analysis of Sallen-Key Architecture*", Application note Texas instrument SLOA024B, july 1999

tel-00417838, version 1 - 17 Sep 2009

Chapter 10

[135] A. Sedra, K.C. Smith, "*The current conveyor: A new circuit building block*", Proc. IEEE, Vol.56, pp. 1368-1369, Aug. 1968

[136] P. Aronhime, "*Transfer-function synthesis using a current conveyor*," IEEE Trans. Circuits Syst., vol. CAS-21, pp. 312–313, Mar. 1974.

[137] A. Sedraa, K.C. Smith, "*A second generation current conveyor and its application*", IEEE Trans., 1970, CT-17, pp. 132-134

[138] Fabre, A, "*Third-generation current conveyor: A new helpful active element*", Elec. Letters, Vol. 31, No.5, pp. 338-339, Mar. 1995

[139] Tielo-Cuautle, E.; Sarmiento-Reyes, L.A., "*Synthesis of the CCII- using the nullor concept*",Third IEEE International Caracas Conference on Devices, Circuits and Systems, 2000.

[140] W. Chiu, S.I. Liu, "*CMOS differential difference current conveyors and their applications*", IEE Proc.-Circuit Devices Syst., Vol. 143, No.2, pp.91-96, 1996

[141] A. PAYNE, C. TOUMAZOU, "*Practical integrated current conveyors*.", ISCAS'94 Tutorials, chap. 11.2.6, pp.595-596

[142] I. Mucha, "*Low-output-impedance CMOS voltage buffer*", Electronics Letters - 22 October 1992 -- Volume 28, Issue 22, p. 2071-2072

[143] G. Palmisano , G. Palumbo and S. Pennisi,"*Design Strategies for Class A CMOS CCIIS*", Analog Integrated Circuits and Signal Processing, Volume 19, Number 1 / avril 1999

[144] K. Manetakis, C. Toumazou, "*A new high-frequency very low output-impedance CMOS buffer*", Circuits and Systems, 1996. ISCAS '96., 'Connecting the World'., 1996 IEEE

[145] M. Minarcik, K. Vrba, "*Continuous-Time Multifunctional Filters with Wide Bandwidth Using Universal Voltage Conveyors*", Sixth International Conference on Networking, 2007. ICN '07.

[146] R. Sponar, K. Vrba, "Measurements and Behavioral Modeling of Modern Conveyors", IJCSNS International Journal of Computer Science and Network Security, VOL.6 No.3A, March 2006

[147] B. CALVO,S. CELMA, P.A. MARTINEZ AND M.T. SANZ, "High-Speed High-Precision CMOS Current Conveyor", Analog Integrated Circuits and Signal Processing, 36, 235–238, 2003

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

List of publications (until 04/2009)

Journals (peer-reviewed)

[1] V. Michal, J. Sedláček. "*Low-pass biquadratic filters with high suppression rate*", Electronics Letters, Volume 45, Issue 12, p. 591-593 (2009).

[2] V. Michal et al. "*Fixed-gain CMOS differential amplifiers with no external feedback for a wide temperature range*", Cryogenic, doi:10.1016/j.cryogenics.2008.12.014 (2009).

Iinternational conferences and workshops

[3] V. Michal, J. Sedláček, K. Hájek, "*Low-Pass Cascade Filters with High Attenuation Rate in the Stopband"*, Proceeding of the IEEE int. Conference Radioelek (2009).

[4] V. Michal, S. Bouat, J-C Villegier, J. Sedláček, "*Superconducting NbN Band-Pass Filter and Matching Circuit for 30GHz RSFQ Data Converter*", Proceeding of the IEEE int. Conference Radioelek (2009).

[5] V. Michal, A. Kreisler, A. Degardin, G.Klisnick, G. Sou, M. Redon, "*Fixed-gain CMOS Differential Amplifiers for the 40 K to 390 K Temperature Range".* Proceeding of 8th European Workshop on Low Temperature Electronics (WOLTE 8)*,* Ilmenau, Allemagne (23-26 June 2008), Oral presentation.

[6] V. Michal, S. Bouat and J.C. Villegier, "*Design of NbN Superconducting Band Pass Filters at 30 GHz for High Speed RSFQ Data converter*", International Workshop on Teleinformatics and Electromagnetic Field TIEF 2008 8. - 12. 9. 2008 Paris, ISBN 978-80-214-3718-0.

[7] V.Michal "*New approaches of read-oud electronics for superconducting single photon detectors",* 1st Karlsruhe Detector Workshop, S-Pulse project*,* oral presentation (May 2008).

[8] A. Kresiler, M. Longhin, V. Michal, M. Aurino, V. Jagtap, I. Türer, X. Gaztelu, A. Scheuring & A.F. Dégardin, "*NANOTIME project: superconducting and semiconducting YBaCuO thin film bolometer investigations for THz imaging arrays*", 1st Karlsruhe Detector Workshop, S-Pulse project*,* Invited presentation (May 2008).

[9] V. Jagtap, M. Longhin, V. Michal, A.F. Degardin, P. Teste, A.J. Kresiler, G. Klisnick, G. Sou, M. Redon, "*Semiconducting vs superconducting YBaCuO thin film bolometers: sensitivity and crosstalk investigations for future far-infrared imagers*", Invited Poster, Applied Superconductivity Conference (ASC 08) Chicago, USA.

[10] E. Baggetta, S. Bouat, V. Michal, J.-C.Villegier, I, D. Renaud, Ch. Bornier, P. Lefervre, R. Guelaz, P. Lumeau "*Elaboration of NbN ADC circuits on large area wafers for HyperSCAN*", Poster, Applied Superconductivity Conference (ASC 08) Chicago, USA.

[11] P. Febvre, D. Bouis, V. Michal, R. Setzu, J.-C. Villégier, "*Evaluation of self-shunted NbN/TaN/NbN Josephson junctions for digital electronics*". Poster, Applied Superconductivity Conference (ASC 08) Chicago, USA.

[12] R. Setzu, S. Bouat, V. Michal, J.-C. Villegier, I, D. Renaud, "*Study of NbN Josephson Junctions with Barrier Tuned to the Metal-Insulator Transition*". Poster, Applied Superconductivity Conference (ASC 08) Chicago, USA.

[13] V. Michal, A. Kreisler, A. Degardin, G.Klisnick, G. Sou, M. Redon, "*Integrated readout electronics for THz bolometric detector characterization*". Poster, International Workshop on Teleinformatics and Electromagnetic Field TIEF 2007, 1. - 5. 7. 2006 Epita-Paris.

tel-00417838, version 1 - 17 Sep 2009

[14] E. Bagetta, V. Michal, R. Setzu, J-C. Villegier, "*Implementation of a Superconducting High Frequency Divider Circuit with NbN/TaXN/NbN Josephson Junctions*". Poster, International Workshop on Teleinformatics and Electromagnetic Field TIEF 2007, 1. - 5. 7. 2006 Paris presentation.

[15] Ch. Péroz, A.F. Dégardin, V. Michal & A.J. Kreisler; J-C. Villegier; G. Beaudin, Y. Delorme & A. Ferret; M. Redon, A. Sentz, G. Klisnick & D. Prele, "*Fabrication and characterization of ultrathin PBCO/YBCO/PBCO constrictions for hot electron bolometer terahertz mixing application*" Invited poster, Applied Superconductivity Conference (ASC'06), Seattle, USA (August 2006).

[16] V.Michal, K.Hájek, J.Sedláček. "*Active filters based on goal-directed lossy RLC prototypes*". Proceeding of Int. conference on fundamentals of electrotechnics and circuit theory 2006. Gliwice-Ustron: Silesian University of Technology, 2006. s. 393-396. ISBN: 83-85940-28-6.

[17] V.Michal, K.Hájek, J.Sedláček, "*Non-ideal performance of active biquadratic filter blocks*". Proceeding of Int. conference on fundamentals of electrotechnics and circuit theory 2006. Gliwice-Ustron: Silesian University of Technology, 2006. s. 397-400. ISBN: 83-85940-28-6.

[18] V. Michal, K.Hájek, J.Sedláček, "*Modern operational amplifiers and their degeneracy effects on active filter performance"*. Proceeding of Int. conference on fundamentals of electrotechnics and circuit theory 2006. Gliwice-Ustron: Silesian University of Technology, 2006. s. 505-507. ISBN: 83-85940-28-6.

[19] K.Hájek, V.Michal, J.Sedláček, "*Real parameters of active filter sections used by non-cascade synthesis*". In Electronics Devices and Systems IMAPS 06. Brno: VUT Brno FEKT, 2006. s. 85-90. ISBN: 80-214-3246-2.

[20] K.Hájek, V.Michal, J.Sedláček, "*A non-cascade synthesis of optimized ARC filters*". Proceeding of International Workshop ISEP - DTEE Brno: VUT Brno, FEKT, 2006. s. 1-4. ISBN: 80-214-3250-0.

[21] K.Hájek, V.Michal, J.Sedláček, "*Active filter blocks for non-cascade filter synthesis*". Proceeding of International Workshop ISEP - DTEE. Brno: VUT Brno FEKT, 2006. s. 1-6. ISBN: 80-214-3250-0.

[22] K.Hájek, V.Michal, J.Sedláček, "*Real properties of two active biquadratic filter sections*". In Digital Technologies 2005 DT´05. Žilina: EDIS -Žilina university publishers, 2005. s. 44-47. ISBN: 80-8070-486-4.

[23] K.Hájek, J.Sedláček, V. Michal, "*An interactive control of universal analog filter*". In AMTEE '05 Seventh International Conference on Advanced Methods in the Theory of Electrical Engineering Applied to Power. Plzeň, 2005. s. 13-18. ISBN: 80-7043-392-2.

[24] K.Hájek, V.Michal, J.Sedláček, "*A New Integral System of Cascade Frequency Filter Design"*. In IC-SPETO 2005. Gliwice-Ustroň: Institute of theoretical and industrial engineering, 2005. s. 467-470. ISBN: 83-85940-27-8.

[25] V. Mchal, K.Hájek. J.Sedláček, "*The Analog Filter Design and Interactive Analog Signal Processing by PC Control*". In Application of electrical engieneering (AEE 05). Praha: WSEAS, 2005. s. 119-122. ISBN: 960-8457-13-0.

[26] K.Hájek., J.Sedláček, B.Sviezeny, V. Michal, "*Universal Digitally Controlled Analog Filter*. In Radioelektronika 2003. Brno: 2003. s. 29-32. ISBN: 80-214-2383-8.

National workshops and publications

[27] A. Kreisler, A. Dégardin, M. Longhin, V. Michal, "*Bolomètres supraconducteurs dans le domaine terahertz : une large famille de dispositifs et d'applications*", 3rd National Workshop on Superconductivity of the French network SEFIRA (Rustrel, France, 4-6 April 2006), Oral presentation.

[28] K.Hájek, V.Michal, J.Sedláček, "*An optimization of non-cascade realized active filters using lossy RLC prototypes*". In Electronic Devices and Systems. Brno: VUT Brno, 2006. s. 79-84. ISBN: 80-214-3246-2.

[29] J. Sedláček, M.Murina, M.Steinbauer, V.Michal, "*Elektrotechnika 2, laboratorní a počítačová cvičení*". BRNO: Ing. Zdeněk Novotný, CSc., Ondráčkova 105, 628 00 Brno, 2006. s. 1-148. ISBN: 80-214-3127-X.

[30] V.Michal, "*Bezdrátový mikrofon VKV*", Journal Praktická elektronika PE 12/2006, ISSN: 1211-328X.

[31] M. Steinbauer, M. Murina, V.Michal, J.Sedláček,"*Elektrotechnika 2 - laboratorní cvičení, počítačová cvičení*". Brno: Ing. Zdeněk Novotný, CSc. Ondráčkova 105, 628 00 Brno, 2005. s. 1-152. ISBN: 80-214-2862-7.

[32] V.Michal, "*Conception of universal digitally controled analog filter*". In Sborník příspěvků konference Radešín 2004. Brno: FEKT VUT BRNO, 2004. s. 89-90. ISBN: 80-214-2726-4.

[33] V.Michal, "*Mikroprocesorový časovač*", Journal Praktická elektronika PE9/2000, ISSN: 1211-328X.

[34] V. Michal, "*Automaticky telegrafni klic*" Proceeding of student conference Student EEICT 2002, Brno. Avard for the best presentation.

[35] V.Michal, "*Modem pro komunikaci po vedení 220V* " Proceeding of student conference Student EEICT 2001, Brno. Avard for the best presentation.

[36] V.Michal, "*čítač 1.3GHz*", AMA, Journal of Czech Radioclub, 6/1998.

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

tel-00417838, version 1 - 17 Sep 2009

SUMMARY OF THE PHD THESIS

This PhD thesis deals with the conception of integrated circuits in the technology CMOS 0.35 µm, dedicated to treatment of the signals generated by the bolometric terahertz detectors, either semiconductors, or High T_C superconductors. We study techniques of reading-out and amplifications of signals generated by bolometric detectors. We opt for an optimal structure, based on a differential amplifier with fixed gain without an external feedback. This may be advantageous, since this class of amplifiers can attain higher bandwidth and reduced noise. However, a higher gain-variation can be observed, especially for required temperatures between 70 and 390 Kelvins. We consecrate a major part of this manuscript to the development and optimisation of these amplifiers, with posses a constant differential gain. Two amplifiers have been conceived, optimised, and fabricated as integrated circuit. The measures effected between 70 and 390 K showed a quite small variation of parameters (gain), as well as a large bandwidth (up to 17 MHz for 10 mW of consummation).
The second part of this manuscript is dedicated to analog signal (pre) processing provided by the frequency filters. The main objective was to improve key parameters of biquadratic filters, especially the high frequencies attenuation. Such filters can be used for higher frequencies as well as for applications requiring a high dynamic range. We introduce two innovative structures, whose good properties were verified by measurements: a modified Sallen key filter, and a structure using a current conveyor CCII. Finally, we present the conception and realisation of the second generation current conveyor CCII, having a very weak output resistance on high frequencies.

SHRNUTI DOKTORSKE PRACE

Tato doktorská práce se zabývá návrhem integrovaného obvodu v technologii CMOS 0.35 µm určeného pro analogové zpracování signálů z polovodičových a supravodivých detektorů záření v oblasti THz. V práci jsou probrány základní metody a principy práce se signály generovanými bolometrickými detektory. Je navržena optimální struktura, založena na diferenciálním zesilovači, jehož zesílení je nastaveno bez použití externí zpětné vazby. Zesilovač v otevřené smyčce může dosáhnout většího mezního kmitočtu a nižšího šumu, ale také velkého rozptylu parametrů. Tento rozptyl může být v našem případě zvýšen extrémním požadovaným teplotním rozsahem: mezi 70 a 390 Kelviny. Návrhu takových zesilovačů se zesílením 40 dB je věnována podstatná část práce. Byly navrženy, optimalizovány a vyrobeny dva typy rozdílových zesilovačů, jejichž měřením v teplotním rozsahu mezi 40 K a 390 K bylo dosaženo nízké variace parametrů (zesílení) a vysokého mezního kmitočtu (až 17 MHz při spotřebě 10 mW)
Zpracování signálů pomocí kmitočtových filtrů je věnována druhá část práce. Hlavním cílem je zlepšit některé parametry klasických (kaskádních) kmitočtových filtrů, především potlačení v nepropustném pásmu. Takovéto filtry je možné použít i do vyšších kmitočtů. V práci jsou uvedeny dvě struktury, jejichž výhodné parametry byly ověřeny měřením: modifikovaná struktura Sallen-Key a struktura založena na proudovém konveyoru CCII. V závěru je představen návrh a realizace integrovaného proudového konveyoru CCII, jež dosahuje velmi nízkých hodnoty výstupního odporu na vysokých kmitočtech.

RESUME DE LA THESE DOCTORALE

Cette mémoire de thèse porte sur la conception de circuit intégré en technologie CMOS 0,35 µm, dédiée au traitement des signaux analogiques issu de capteurs bolométriques térahertz, semi-conducteurs et supraconducteurs. Nous étudions les techniques de la lecture et d'amplification des signaux générés par les capteurs bolométriques. Une structure optimale, basée sur un amplificateur différentiel à gain fixe, sans contre-réaction, a été adoptée. Cette amplification effectuée en boucle ouverte permet d'atteindre une bande-passante plus large, ainsi qu'un niveau du bruit réduit. Cependant, la variation du gain est généralement plus importante, notamment en tenant compte de la plage de température requise, entre 70 et 390 Kelvins. Nous consacrons une grande partie du manuscrit au développement et à l'optimisation de ces amplificateurs à gain différentiel constant. Deux amplificateurs ont été conçus, optimisés et fabriqués, dont les mesures, effectuées entre 70 et 390 K, ont démontré une variation des paramètres (gain) faible, ainsi qu'une bande-passante importante : jusqu'à 17 MHz pour une consommation de 10 mW.
La seconde partie du manuscrit est dédiée au traitement de signal par les filtres analogiques. L'objectif principal a été d'améliorer les paramètres-clés des filtres biquadratiques, notamment leur atténuation en hautes fréquences. De tels filtres peuvent être utilisables pour des fréquences plus élevées, ainsi que pour des applications à haute dynamique. Nous introduisons deux structures innovantes, dont les bonnes caractéristiques ont été vérifiées expérimentalement: un filtre de Sallen-Key modifié, et une structure utilisant un convoyeur du courant CCII-. Enfin, nous présentons la conception et la réalisation d'un convoyeur du courant CCII- ayant une très faible résistance en hautes fréquences.