# A TWO-MODE SYCHRONOUS BUCK CONVERTER FOR LOW POWER DEVICES WITH THE SLEEP MODE

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## ABSTRACT

The power consumption of smart camera in car black box varies significantly between light load and heavy load. The high efficiency voltage regulator is necessary in prolong the life of smart camera battery. Since the smart camera only recording the video when car is driving, the most time of the smart camera works in the sleep mode. Hence the light load efficiency is important in this application, however, conventional buck converter usually have high efficiency at heavy load but poor efficiency at light load. To increase the light load efficiency of buck converter, this research continues Yeago's two phase buck converter with optimum phase selection control and Zhao's two mode buck converter to further improve the light load efficiency for the target application.

With 5V input voltage and 1.2V output voltage, the proposed two-mode synchronous buck converter can supply the load power from 12mW to 1.44W. To improve the light load efficiency of conventional buck converter, the proposed design applied Wei's baby buck concept to provide another light load power stage to reduce the switching loss and driving loss at light load. Then, the variable frequency ripple-based constant on-time control with discontinuous conduction mode (DCM) in light load is applied to the baby-buck mode to reduce the switching frequency to further reduce the switching loss. Also, the baby-buck mode uses the synchronous buck topology to remove the diode in asynchronous converter to increase the efficiency at light

load. Finally, a sensorless mode selector remove the sensing resistor in power stage to increase the efficiency for entire load range, especially for the heavy load. The mode selector can select the optimum mode for different load condition, and the opposite mode would completely shut down to save the loss.

The proposed design is implement in CMOS 0.25um technology. The proposed monolithic buck converter which include the power stage of heavy buck mode, baby-buck mode and the controller is fabricated. The measurement result shows the close loop efficiency varies from 70%-83% toward the entire load range.

*To my parents, my grandma and grandpa*

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# Chapter 1

# Introduction

## 1.1 Motivation

Nowadays, more and more electronic devices are powered by Li-ion batteries, so a high efficiency converter is essential in maximizing battery life and enhance the operation time. When the battery is used in powering microprocessors, which operate mostly in sleep mode to save power, [1] the influence of converter's light load efficiency become severe.

The smart camera implemented in car black box continuously detects motion in sleep mode, once motion detected, the camera switches to active mode to record video, while return to sleep modes when motion stop. Since the camera and its microprocessor work in sleep mode for the majority of times, and powered by the car battery, a step down converter with high efficiency at light load is necessary for car battery life extension. Also, since power consumption increase significantly from sleep mode to active mode, the converter also need to handle power at heavy load. The proposed research is focus on the light load efficiency improve in step-down power converter while maintain a high efficiency at heavy load.

# 1.2 Step-down DC/DC Converter

Figure 1.1 shows the general block diagram of DC-DC power converter. The power processor designing is base on the input and output voltage requirement. And the feedback controller is to make the output voltage stable when the other state variables change in operation. Basically, the power processor can be categorized as the step-up converter and the step-down converter. In step-up converter the Vout is larger than Vin, while in step-down converter the Vout is smaller than Vin. The common goal of all converters is to minimize the total power dissipation and hence improve the efficiency. We only focus on the step-down converter here.

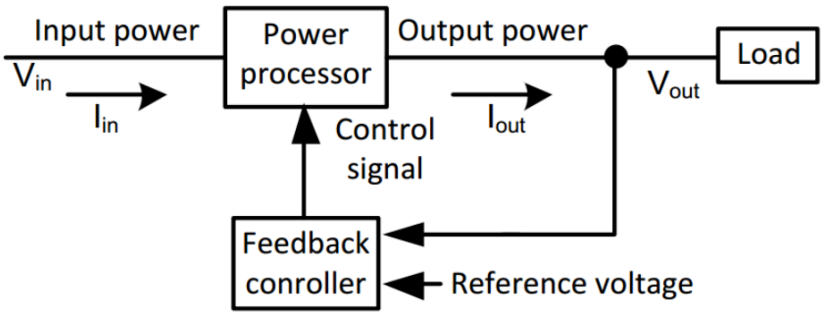


**Fig 1.1: Block Diagram for a Power Converter System [2]**

In the family of step-down converter, the synchronous buck topology is widely used to regulate output voltage. Figure 1.2 shows the specific topology of a DC-DC synchronous buck converter.

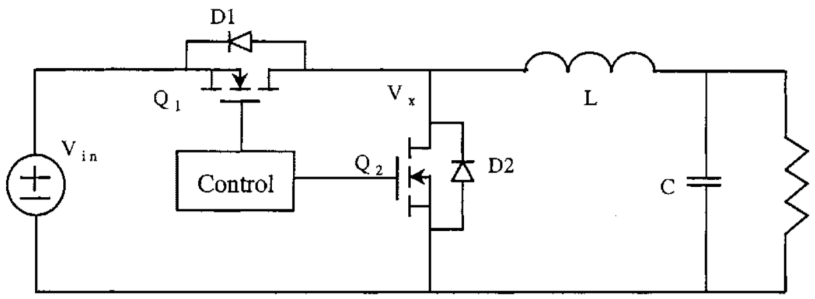

**Fig 1.2: Synchronous Buck Converter**

Compare to the asynchronous buck converter, a synchronous MOSFET Q2 is used to emulate the operation of a freewheel diode. The disadvantage of this topology is its low efficiency at light load, due to the higher conduction loss and gate drive loss. [3] Also, when the load power range is under tens of milliwatts controller loss would become significant. The operation of the synchronous buck converter would be addressed in Chapter 2.

# 1.3 Technical Contributions of the Proposed Research

This research is focus on the light load efficiency improvement of DC/DC step down converter which have 5V input voltage and 1.2V output voltage. Since the application of this buck converter is to supply power to a processor in car black box, the light load efficient is important in improving the car battery life.

The research work of this thesis was to adapt the two-mode buck converter proposed by Zhao [4] to further improve the light load efficiency for low power application. The synchronous buck topology was implied in both heavy-load mode and baby-buck mode to maximize the heavy load efficiency and light load efficiency. The optimum mode is selected base on the load current condition, and the opposing mode would be shut down while the other mode is working. The heavy-load mode adopts the continuous conduction mode(CCM), while the baby-buck mode adopts the pulse frequency

modulation(PFM) with discontinuous conduction mode(DCM) to reduce the switching frequency at light load. The sensing resistor that use to sense the load current condition is replaced by a digital mode selector which utilize the time sequence difference of gate signal and zero current crossing signal in DCM and CCM to select the corresponding mode. Hence the efficiency of heavy-load mode is improved. In the baby-buck mode, the zero current detector is designed to control the synchronous MOSFET to remove the Schottky diode to further improve the light load efficiency. Also, the Constant on-time $V^2$ control which eliminate the outer loop is used to reduce the controller power consumption in light load. The mode selector and Constant on-time block is optimized to reduce the power consumption at light load. The tapered gate driver with fast turn-on speed and slow turn-off speed introduce the dead time between control MOSFET and synchronous MOSFET to avoid shoot through during switching process.

The power MOSFET of the proposed optimized two mode buck converter and its controller is fabricated in CMOS 0.25um technology. The measurement result validates the performance of proposed design.

# 1.4 Thesis Organization

The organization of this thesis is organized as follow: Chapter 2 give the preliminaries and back ground for proposed design. It gives the description of CCM and DCM in buck converter, then a general discussion of loss breakdown in buck is introduced. The explanation and calculation of conduction loss, switching loss and driving loss is introduced. The COT $V^2$ in PFM is reviewed and its benefit in light load is discussed. Then the former

research about light load improvement and baby-buck concept is introduced, the advantage of different method for light load efficient is covered. Chapter 3 described the block diagram of proposed design. The design procedure and design strategy of power stage is discussed. Then the following section gives the selection consideration of inductor and capacitor in power stage. Finally, the design of controller that implemented in CMOS technology is covered. The important block such as constant on-time block, zero current detector, comparator is introduced, the transistor level circuit diagram is giving. Chapter 4 present the simulation result and measurement result of proposed design to validate the functionality and performance of proposed design. Finally, chapter draw a conclusion on proposed two modes synchronous buck converter and give the suggestion of future research.

# Chapter 2

# Preliminaries

The preliminary knowledge is provided to understand the proposed two mode synchronous buck converter. Section 2.1 gives the two basic conduction modes in converter operation. Section 2.2 provides the general loss breakdown in conventional buck converter. Section 2.3 describes the Pulse frequency modulation(PFM) and Constant on-time control. Section 2.4 gives Zhou's research in improving light load efficiency. Section 2.5 reviews the baby-buck concept in existing research and their drawback. Section 2.6 summarizes the chapter.

# 2.1 Continuous Conduction Mode and Discontinuous Conduction Mode in Synchronous Buck Converter

The synchronous buck converter which shows in Fig.1.2 have two switching MOSFETs in power stage, and the operation of these two switching MOSFET in different conduction mode would explain in detail in this section.

## 2.1.1 Conduction Mode

In the conduction mode, the inductor current is continuous in steady state, which is show in following figure.

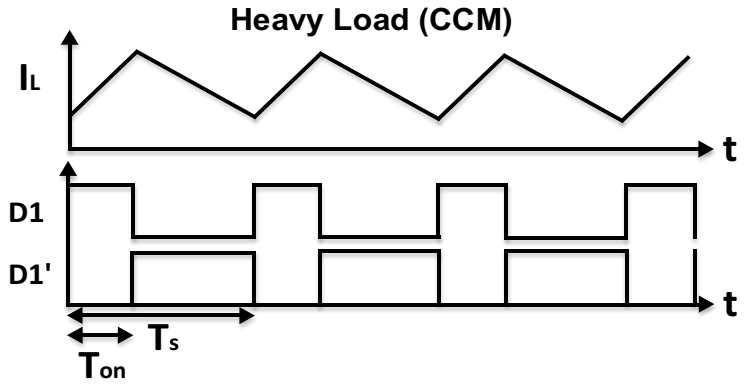


**Fig 2.1 Inductor Current and Gate Signal of MOSFET in CCM(Steady State)**

The $I_L$ represent inductor current, $D_1$ is the gate signal of control MOSFET $Q_1$ , $D_1^{'}$ is the gate signal of synchronous MOSFET $Q_2$. Under same load condition, the CCM mode would have lower RMS current compare

to CCM mode, hence the CCM mode normally apply to heavy load operation. Since a MOSFET always turns on in one period, the resonant noise which induced by inductor and capacitor would not happen, hence the EMI situation would be better in CCM mode. The tradeoff for CCM mode is that it requires a large inductor to maintain inductor current ripple small enough.

The steady state operation of $Q_1$ and $Q_2$ is shown in Fig. 2.1. The control MOSFET would turn on first, because of the buck topology, the energy from input source would store in inductor, which made the inductor current increase. After $DT_s$, the control MOSFET turns off and synchronous MOSFET turns on, the inductor would provide energy to load and inductor current reduce. $C_{out}$ work as a los pass filter to remove high frequency noise in load. The increasing slope and reducing slope of inductor is derived below:

$$k_{inc} = \frac{V_{in} - V_{out}}{L} \tag{1}$$

$$k_{dec} = \frac{-V_{out}}{L} \tag{2}$$

$k_{inc}$ represent the increasing current slope, and $k_{dec}$ represent the decreasing slope.

When converter works in steady state, the inductor must have voltage-second balance [3], which means the voltage and time product apply on inductor in one period equals to zero, hence we can have

$$\frac{V_{in} - V_{out}}{L} D_1 T_s - \frac{-V_{out}}{L} D_1' T_s = 0 \tag{3}$$

and

$$D_1 = \frac{V_{in}}{V_{out}} \tag{4}$$

So a buck converter achieve a voltage step down function.

## 2.1.2 Discontinuous Conduction Mode

As the inductor current reduced, the converter would finally enter DCM, where inductor current become discontinuous. Fig 2.2 shows the inductor current in different conduction mode.

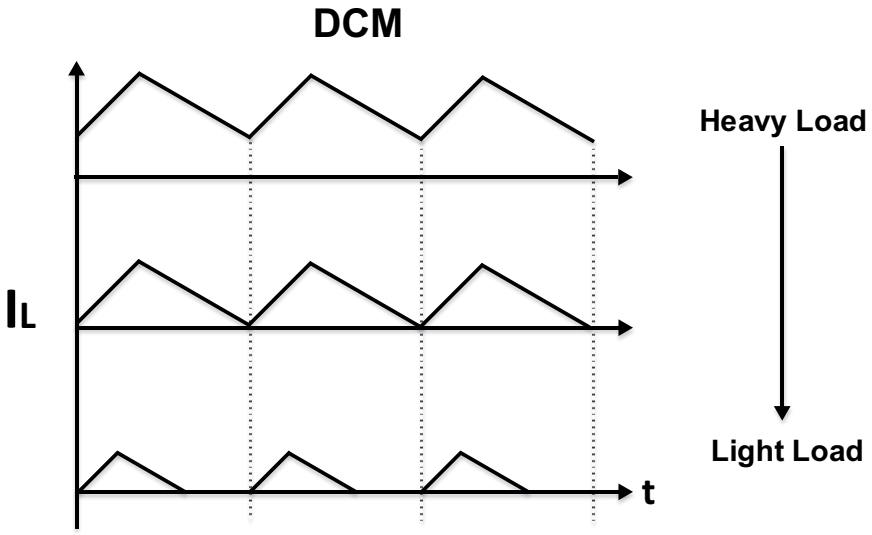


**Fig 2.2 Inductor Current Waveform in CCM, BCM and DCM**

Fig 2.3 shows the MOSFET gate signal corresponding to the inductor current.

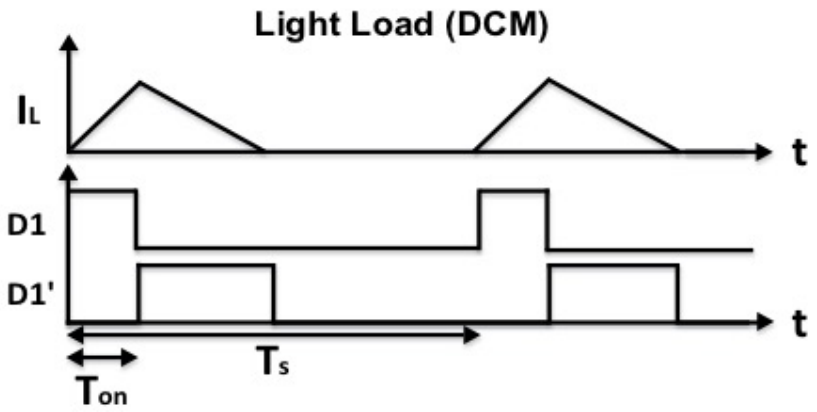


**Fig 2.3 Inductor Current and Gate Signal of MOSFET in DCM (Steady State)**

Comparing to the CCM, another time interval where both MOSFET turns off appear in a single period operation. When the inductor current touch zero, if the path for current still exist, the current would become negative, which would make the efficiency decrease, also, the negative current is useless, because it can't provide energy to load.

In the DCM mode, when inductor current touch zero, both switching MOSFETs would turn off, and the output capacitor would provide energy to load. Since the MOSFET have parasitic capacitors, the inductor and parasitic capacitor would begin resonant in that time interval. Although the DCM mode would increase the light load efficiency, the extra components which detect the zero crossing point of inductor current is needed. Also, the resonant of LC circuit would increase the EMI noise in circuit.

## 2.2 General Loss Breakdown in Converters

The loss distribution of converter varies as load current change, especially under light load condition. In typical converter design, the power stage is optimized for maximum load because of the higher impact on power

consumption. In normal case, the conduction loss would dominant in heavy load, while switching loss and conduction loss would dominant in light load. An example which road range is close to our target output current is show in Fig.2.1, the ratio of driving loss and MOSFET switching loss become significant in light load.

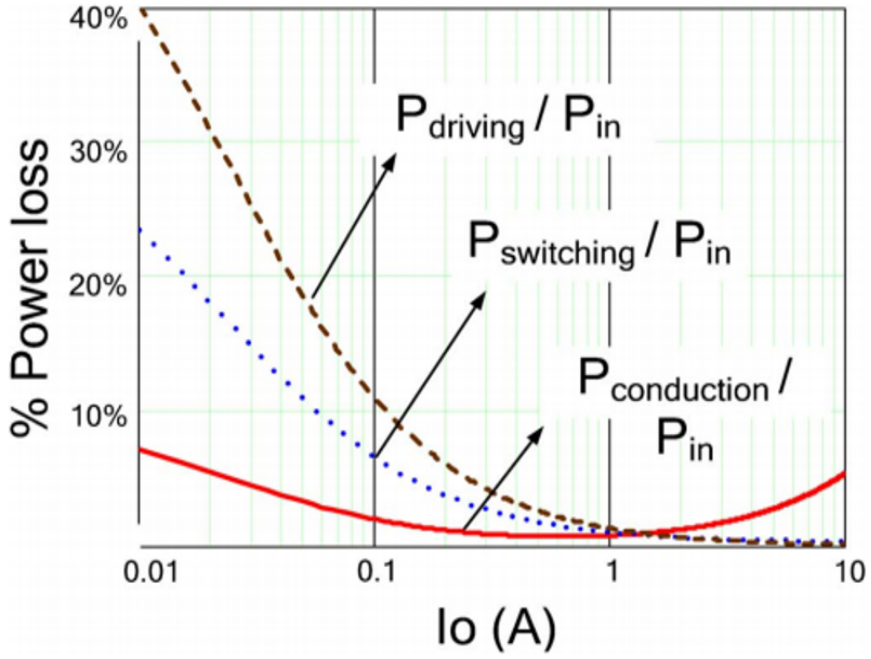


**Fig 2.4 Loss Breakdown vs Load [4]**

As the load current approaching to 1A, the ratio of driving loss and switching loss reduce greatly. Due to the increasing $I_o$, the conduction loss dominants, hence relative low $R_{dson}$ is prefer for heavy load in high current situation. In the light load situation, since current reduce, the power consume by $R_{dson}$ (drain to source resistance in MOSFET) reduces, the $Q_g$ (gate charge of MOSFET) and $C_{gd}$ (capacitor between gate terminal and drain terminal in MOSFET) would dominant switching loss. However, the $Q_g$, $C_{gd}$ and $R_{dson}$ can‘t be small at the same time. The larger the $R_{dson}$ the

smaller the $Q_g$ and vice versa, hence the trade off between $R_{dson}$ and $Q_g$ is made in converter design.

### 2.2.1 Conduction Loss in Synchronous Buck Converter

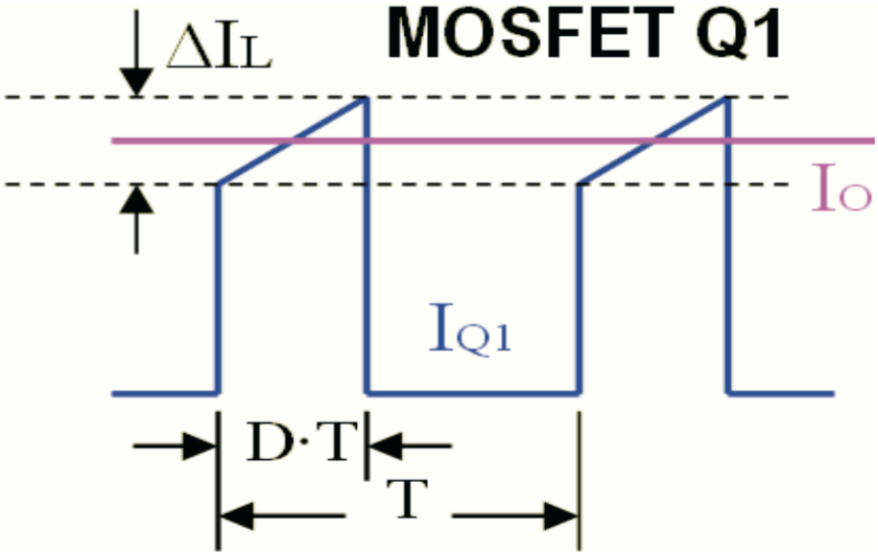


**Fig 2.5 Current in Control MOSFET Q1[5]**

Figure shows the current pass through control MOSFET $Q_1$ in $DT_s$ (CCM), where the current include both DC and AC parts. To calculate the conduction loss in control MOSFET, we can use:

$$P_{Q1\_con} = I^2_{RMS\_Q1} * R_{dson_{Q1}} \quad (5)$$

where

$$I^2_{RMS\_Q1} = \left(I_o^2 + \frac{\Delta I_L^2}{12}\right) * D \quad (6)$$

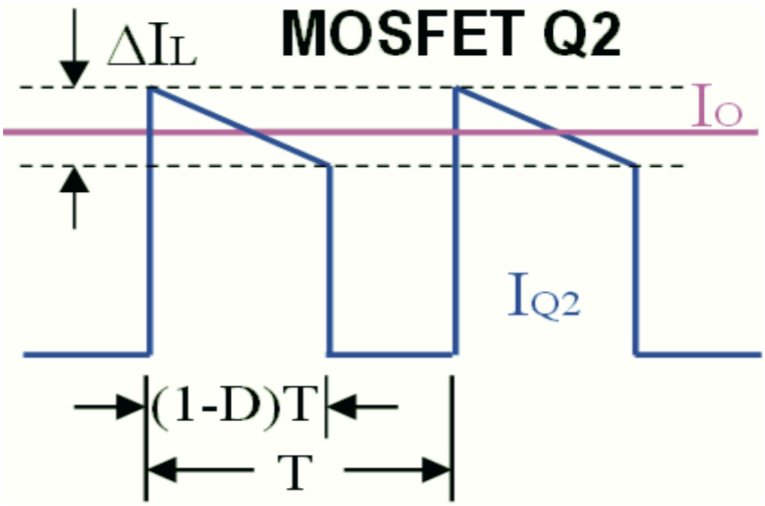


**Fig 2.6 Current in Synchronous MOSFET Q2[5]**

Figure 2.6 shows the current pass through synchronous MOSFET in CCM mode, as calculate above, we can obtain the conduction power dissipation in synchronous MOSFET. So the total conduction loss in power switch equals to:

$$P_{Q1\_con} = \left(I_o^2 + \frac{\Delta I_L^2}{12}\right) * \left[\frac{V_o}{V_{in}}\left(R_{dson_{Q1}} - R_{dson_{Q2}}\right) + R_{dson_{Q2}}\right] \qquad (7)$$

where

$$\Delta I_L = (V_{in} - V_o) * \frac{V_o}{L * f * V_{in}} \qquad (8)$$

Where $L$ is the inductance of inductor, $f$ is the switching frequency of design converter.

## 2.2.2 Switching Loss and Driving Loss

The switching loss are created as a result of miller plateau, which induce a simultaneous exposure of high current and voltage during the turn on and turn off procedure of MOSFET. Figure 2.7 shows the equivalent model of power MOSFET and Figure 2.8 shows the current and voltage waveform of a power MOSFET during turn on procedure.

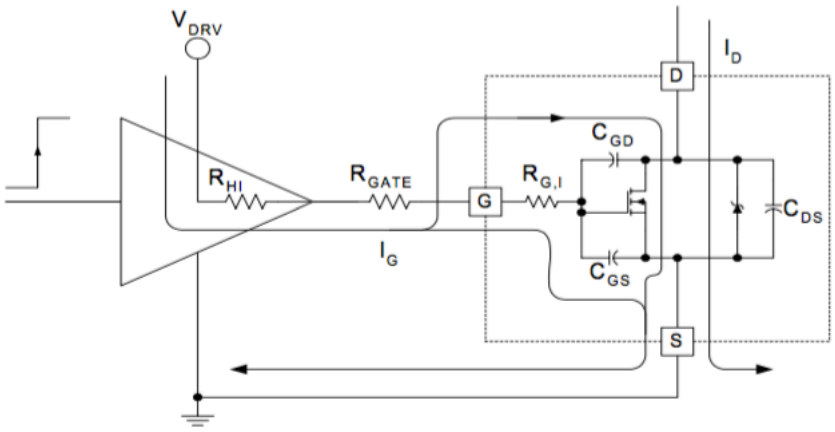


**Fig 2.7 Equivalent Model of Power MOSFET [6]**

In Figure 2.7, the capacitor $C_{GD}$, $C_{GS}$, $C_{DS}$ are included in the MOSFET model, all these three capacitor would have impact on the switching loss. The switching loss and driving loss is generated during the procedure of charging and discharging these parasitic capacitors.

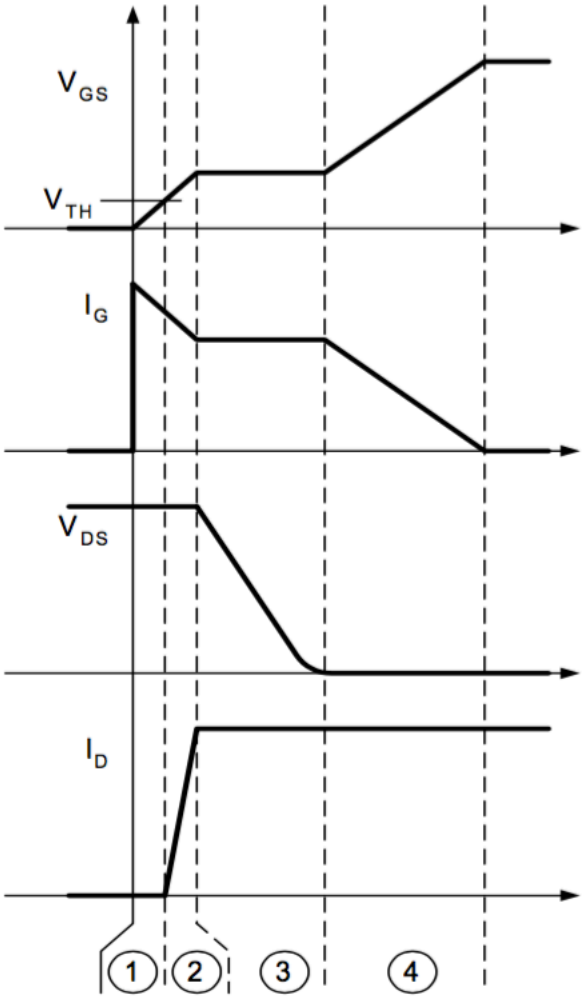


**Fig 2.8 MOSFET Turn on Time Interval [6]**

The interval 3 shows in Fig 2.8 is the miller plateau, which is the discharging process of $C_{GD}$. Since the current pass through MOSFET would increase when $V_{GS}$ exceed $V_{th}$, and the voltage of capacitor can't change simultaneously, when current is increasing, the $V_{DS}$ would still remain high. So a cross between high voltage and current induce the switching loss. A rough formula for switching loss calculation is:

$$P_{sw} = \frac{1}{2} V_{in} * I_{out} * F_{sw} * \frac{Q_g}{I_{driver}} \tag{9}$$

where $I_{driver}$ is the current provided by gate driver.

The gate driving loss is the lost energy used to charge and discharge the gate capacitance of the MOSFET at each switching event.

$$P_{gate} = Q_g * F_{sw} * V_{gs} \quad (10)$$

As we can observe from the equation, the larger the parasitic capacitance, the larger the switching loss and driving loss. Also, these two losses would not change greatly as the output current increase. The dilemma that heavy load require a low $R_{dson}$ and light load require low $Q_g$ is meet. Through reducing the switching frequency $F_{sw}$ or $Q_g$ in light load would improve the light load efficiency. The proposed converter adopts the two modes due to the tradeoff mentioned above. The heavy-load mode adopts the synchronous buck converter approach for high efficiency at heavy load and baby-buck mode adopts PFM control with DCM operation to reduce switching frequency, and $Q_g$, and optimizes baby-buck power switches for higher efficiency at light load.

## 2.3 Pulse Frequency Modulation (PFM)

The PFM technique is common in step down DC-DC converter, it can help to increase the light load efficiency through reducing the switching frequency. When the converter works in DCM, the switching frequency reduce with the decrease of load current.

The constant on-time and constant off-time control are two popular control scheme in PFM control [7][8]. For constant on-time control, the on time of control MOSFET is fix, while the on time of synchronous MOSFET changes.

The valley value of sensing signal is tracked, once the value is below threshold voltage and detected, a constant on-time pulse would be generated to trigger the control MOSFET turns on. In the constant off-time control, the on-time for synchronous MOSFET is fix, and a comparator continuous track the peak threshold value. Normally, the COT control can be realized through hysteretic control and valley current mode control. The hysteretic control direct sensing the output voltage to generate on-time pulse, while the valley current mode control need to sense the inductor current. One drawback of the hysteretic control is that it need a large ESR of output capacitor, otherwise, the sub-harmonic oscillation would happen, because of the phase delay between inductor current and output voltage. In valley current mode control, since the inductor current information is used to trigger on-time pulse, this oscillation would not happen, but it requires a more complex control scheme and compensation network.

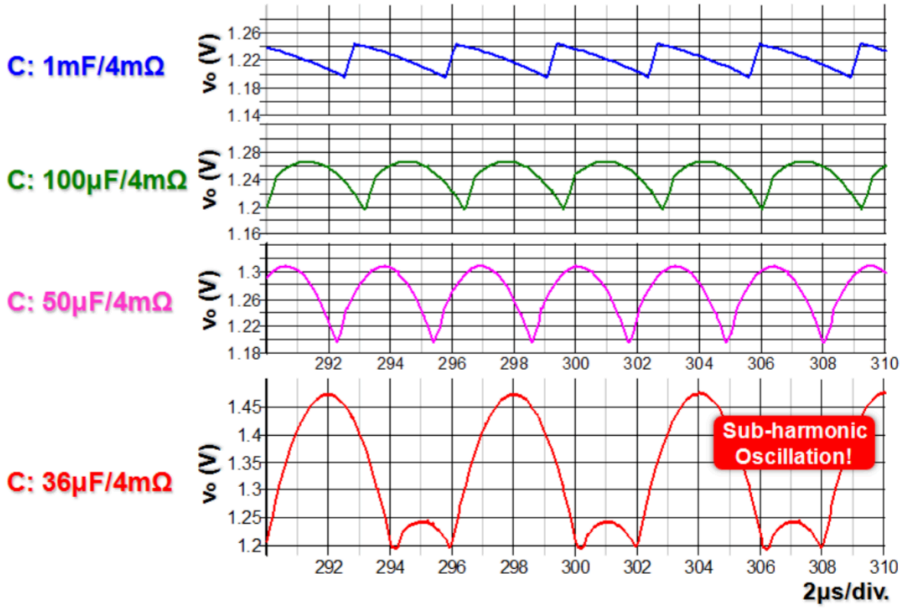


**Fig 2.9 The Influence of the Capacitor Ripple for Sub-harmonic Oscillation [9]**

The Constant off-time control uses trailing edge modulation, resulting in delayed transient performance for load step-up [10]. Thus, COT control is generally more preferred by industry.

## 2.3.1 Constant On-time $V^2$ Control

The Constant On-time $V^2$ control also called the ripple-based control. Since this control method have several advantages such as no current sensing network required, fast load transient speed with direct output voltage feedback and simple outer-loop compensation, it has been widely applied in point-of-load buck converter [11]-[15]. This control works well while using an output capacitor with large RC time constant. The small RC time constant capacitor would introduce a sub-harmonic oscillation as shown in Figure 2.9.

Figure 2.10 shows the architecture of variable frequency modulation Constant On-time $V^2$. Since the output voltage ripple signal directly feed to the modulator, a fast transient can be achieved. The dash green line in the diagram means the integrator can be further can be eliminated to simple the control loop, and this simplified one is call ripple-base control [16][17][18].

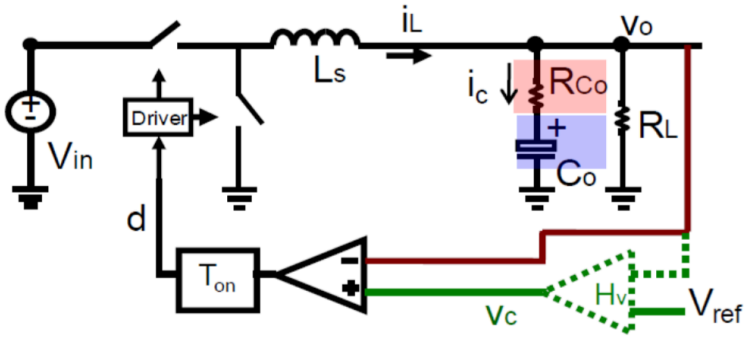


**Fig 2.10 The Architecture of Variable Frequency Modulation Constant On-time $V^2$ [19]**

Since the ripple-base control method is applied in proposed design, the eliminated integrator can further improve the light load efficiency and reduce

the off chip components. Fig.2.11 shows the transfer function of Constant On-time $V^2$ with OSCON cap:

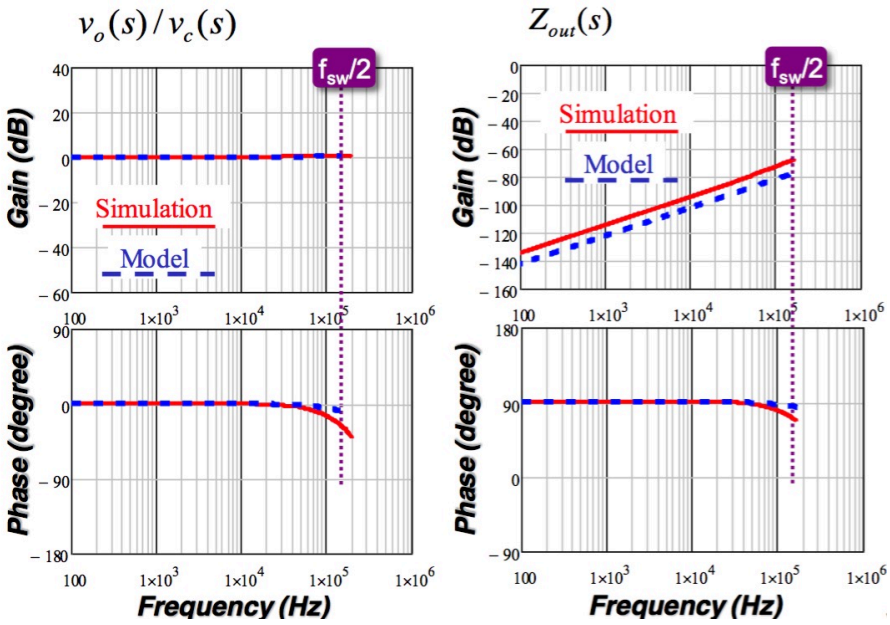


**Fig 2.11 Transfer Function of Constant On-time $V^2$ with OSCON Cap Proposed in Lecture by Q. Li, "Chapter 7 – $V^2$ Control." Bradley Department of Electrical and Computer Engineering, Virginia Tech, Blacksburg, VA, Slide VII-26, Fall 2015.**

The result shows a high bandwidth in all transfer function, which indicate a fast transient speed.

# 2.4 Zhou's Approach in Light Load Efficiency Improvement

The light load efficiency for synchronous rectifier buck VRM is discussed in Zhou's paper [20]. The comparison between synchronous buck converter in CCM and a synchronous buck converter with a diode parallel with synchronous MOSFET is made first. Fig 2.12 shows the schematic of test circuit in [20].

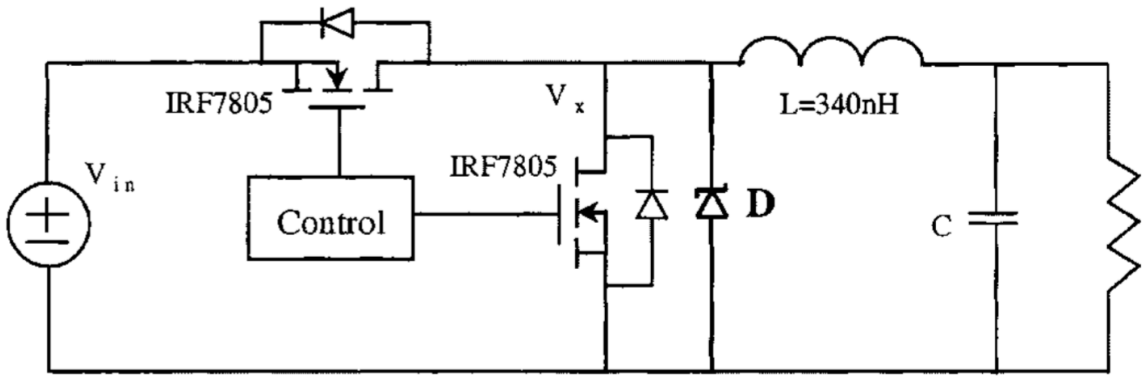


**Fig 2.12 Test Circuit [20]**

The synchronous MOSFET would be turned off completely during light load condition, hence the diode would block the reverse current of inductor, which made the converter works in DCM. Fig.2.12 shows the efficiency comparison result of CCM and DCM at light load.

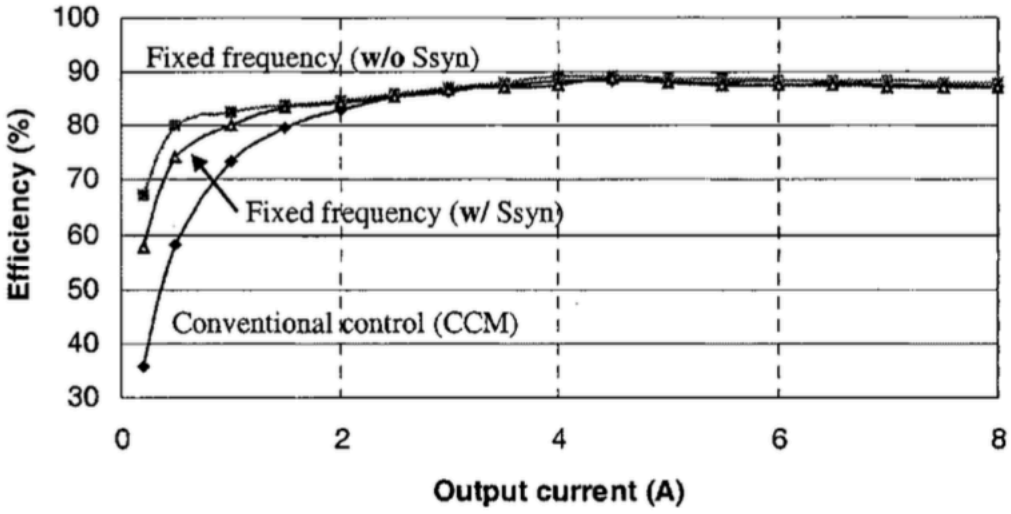


**Fig 2.13 Efficiency Comparison between Different Approaches [20]**

The test result indicate the DCM is more efficient than CCM at light load condition. The reverse inductor current would introduce efficiency drop. Also, the efficiency comparison between synchronous buck in DCM and asynchronous buck in DCM is made in Fig.2.13. Although the synchronous buck owns lower efficiency in the comparison, the light load definition for

this converter is around 1A, while the light load condition for our specification is 10mA.

The continuous comparison between variable frequency and fix frequency control method in light load is made in the paper. Fig.2.14 shows the result,

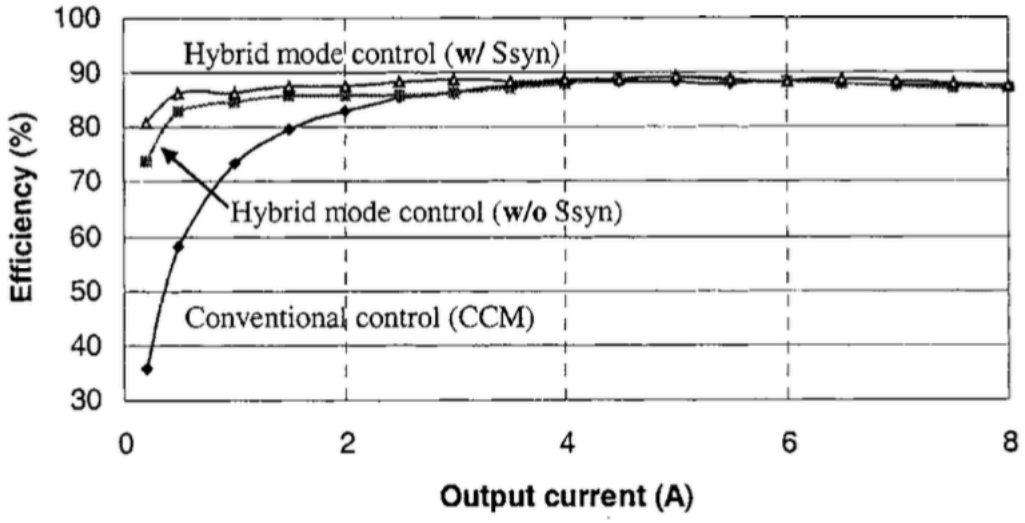


**Fig 2.14 Switching Frequency and Efficiency versus Load Current [20]**

The hybrid mode control in Fig.2.14 means the converter works in fix frequency for heavy load(CCM), while the frequency would reduce as the converter enter DCM, the smaller the load current the smaller the load frequency. Different with the result shows in Fig.2.13, the synchronous buck obtains higher efficiency than asynchronous buck in light load. This is because of the reduced frequency greatly reduced the switching loss in synchronous MOSFET. As a result, loss in Schottky diode would be larger than MOSFET in light load. Although the target application has a lower light load current, where the extra controller part for synchronous buck converter takes a large proportion in total loss, Zhou's result still provides a clear comparison and direction in improving rectifier light load efficiency

# 2.5 Baby-Buck Concept in Current Research

The Baby-buck concept is first proposed by Wei for a two stage buck converter for laptop voltage regulator application, which provide 50 W output power [21]. Fig.2.15 shows the configuration of the two-stage converter; the first stage generates the bus voltage and the second stage convert the bus voltage to lower voltage. A four-phase buck converter including a baby-buck phase is introduced to improve the light load efficiency.

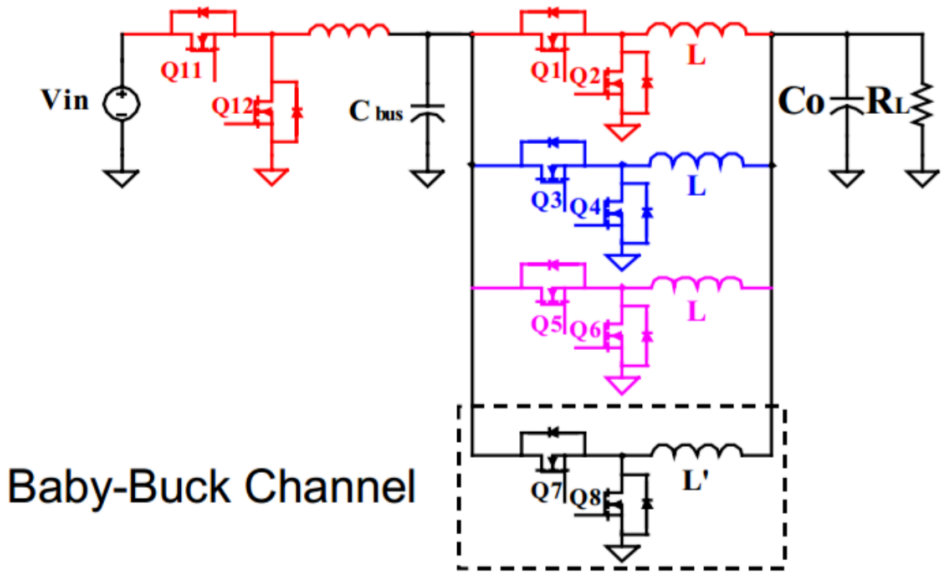


**Fig 2.15 Two Stage Buck Converter with Baby-buck Phase in Second Stage[21]**

The baby-buck phase can handle 3A current, and it is active all the time. The optimal number of phases (ONP) control would select phase based on load condition, all phase is active in heavy load and only baby-buck phase is active in light load. The efficiency can be maximized throughout the entire load range through changing the active number of phase. It uses a PWM control scheme with fixed switching frequency.

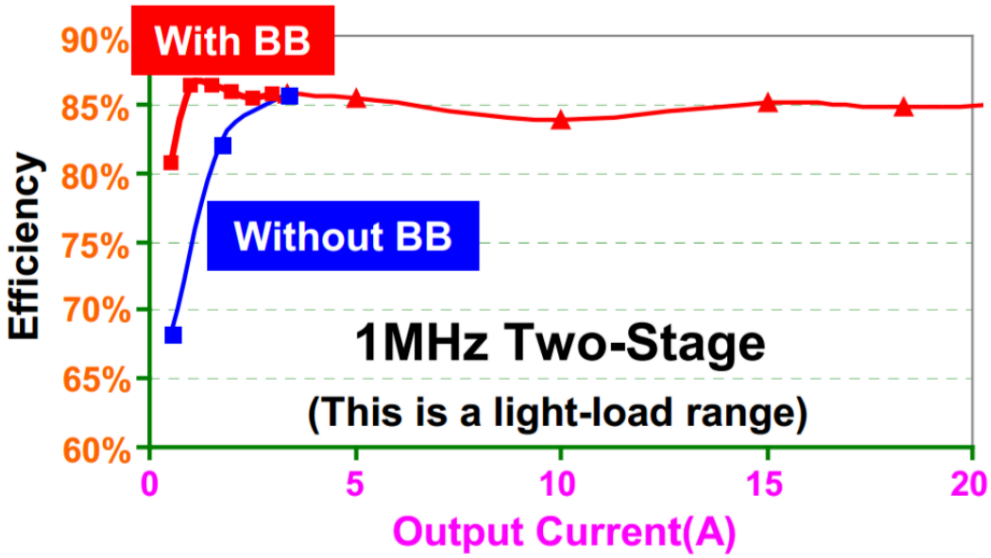


**Fig 2.16 Efficiency Comparison with and without Baby-buck phase[21]**

The Baby-buck phase is designed specifically for the very light load range, the MOSFET with smaller $Q_g$ is used to reduce the switching loss with slight increase of conduction loss. Fig.2.16 shows the theoretical efficiency with baby-buck concept. The efficiency increase more than 10 percent for the lowest load current.

Due to the load current is large in Wei's application, the baby-buck concept need to modify and apply to our low power application. Taylor applied the baby-buck concept with optimum phase selection(OPS) to improve the light load efficiency [22]. The ONP control is replaced by OPS control to reduce the controller loss for low power application. Only two phase is design in Taylor's work, and the controller would select the phase base on load condition. The PFM control is used in light load condition to further reduce switching loss and controller loss. The efficiency of open loop two phase buck converter is show in Fig.2.17

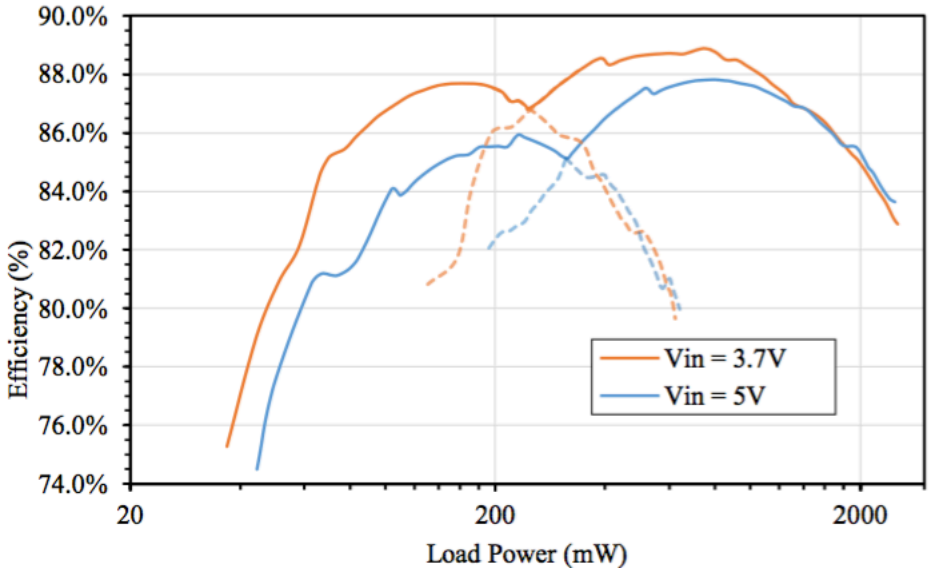


**Fig 2.17 Open Loop Two-phase Converter Efficiency [1]**

The dash line in Fig.2.17 shows the efficiency of the phase used for heavy load. Through changing the heavy phase to baby-buck phase, the efficiency increase near 10 percent in Taylor's work. However, Taylor only implemented the hardware in discrete components, which made the MOSFET and controller can't be fully customize for specific specification. Also, a resistive sensor is used to sensing the load condition for phase selection, which decrease the efficiency at heavy load condition. The proposed converter implements the digital mode selector, which eliminate the sensing resistor and all MOSFET is carefully customize in one chip to increase the integrity of regulator.

## 2.6 Chapter Summary

The topics that related to the proposed design were reviewed in this chapter.

First the CCM and DCM was introduced, the advantage and disadvantage under different load were discussed. Then a general loss breakdown in buck

converter was discussed, the rough ratio of switching loss, driving loss and conduction loss was reviewed, the calculation of each loss and important variable in loss calculation was introduced. This chapter also reviewed Zhou's research in VRM light load efficiency improvement, where the light load efficiency comparison of synchronous buck and asynchronous buck under PWM and PFM is discussed. Wei's multi-phase with baby-buck channel with optimum phase number control and Taylor's baby-buck phase with optimum phase selection control was introduced. Their shortcoming in low power application was discussed. The proposed converter which consist two different modes with optimized power MOSFET would improve the efficiency over entire load range compared to Wei's and Taylor's approach for low power application.

# Chapter 3

# Proposed Design

## 3.1 Proposed Two-Mode Buck Converter

The proposed two-mode buck converter further improve the light load efficiency. The optimized MOSFET size is designed in each mode to get the optimized conduction loss, switching loss and gate driver loss. The controller can select mode adaptively base on load current, and a sensorless load current detector helps saving loss in heavy load condition. This chapter would

organized as follow: Section 3.1 gives the specification of design requirement，which include the input/output voltage, output load current and maximum output voltage ripple. Section 3.2 shows the power stage of proposed two-mode buck converter and its operation principle. Section 3.3 provide the detail of controller circuit and function of each control block. Section 3.4 gives the design strategy of the power stage. Section 3.5 shows the circuit implementation in 0.25um CMOS technology.

### 3.1.1 Specification of the Proposed Converter

Table. 1 gives the specification of require design, which is provide by KAIST. The proposed converter is designed to regulate the output voltage at 1.2 V, with an input of 5 V. The load current ranges from 10 mA to 1200 mA. The peak-to-peak output ripple must be within the processor input requirement of 30 mV, with load transient requirement of 60 mV. The main challenge in design is the wide load current range, the smart camera only draws 10mA current in sleep mode, which is only 1% of full load current.

**Table 1: Specifications of the Proposed Buck Converter**

| Specification | Requirement |
|---|---|
| **Input/output voltage** | 5V/1.2V |
| **Minimum/maximum load current** | 10mA/1000mA |
| **Output voltage steady / transient peak-peak ripple** | 40mV/60mV |

# 3.2 The Power Stage in Proposed Converter with Two Mode Approach

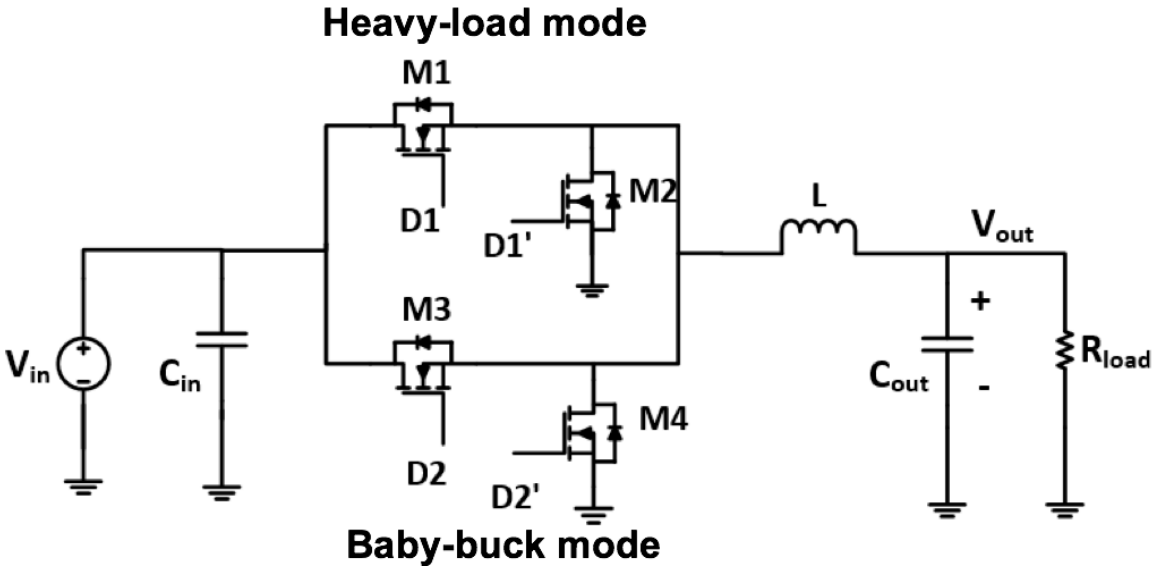


**Fig 3.1 Power Stage of Proposed Two-mode Buck Converter**

Fig. 3.1 shows the power stage of proposed two-mode buck converter, where the inductor and output capacitance is shared by the two modes. The active mode which works in CCM is designed to handle load range from 180mA to 1200mA, while the baby-buck mode works in DCM to handle the light load situation from 10mA to 180mA, only one mode would be activated during voltage regulation, the other mode would be shut down to save controller loss. The switching MOSFET is tuned to fit the corresponding load range, and both two mode have close efficiency at transition load point. These two mode both applied with Constant-on-time V2 control to adjust the

## 3.3 Design Consideration and Components selection of Power Stage

As describe in section 3.2, the proposed converter has two modes in the power stage, the load transition point was determined through intersection of optimized open loop power stage simulation. Due to the Heavy-load mode works in heavy load and Baby-buck mode works in light load, each mode would have different design strategy. Also, the power stage not only include the switching MOSFET but inductor and output capacitor as well. Both inductor and output capacitor selection have important impact on the control loop design.

Before designing the switching MOSFET, we should consider the guaranteed drain-source breakdown voltage to make sure the MOSFET would not break down and destroy during operation. Due to our input voltage is 5V, so the cell of 7V LDMOS in IC PDK is selected to compose our power stage, where 40% of overshoot voltage is allowed. The other parameters such as on-resistance, total gate charge would affect the overall converter efficiency greatly. As MOSFET is the switching element in DC/DC converter, the on-resistance is related to the conduction loss and the total gate charge is related to switching loss, which are two majority loss in switching MOSFET. The product of the two important MOSFET parameters $R_{dson}$ and $Q_g$ is called Figure of Merit(FOM):

$$FOM = Q_g * R_{dson} \tag{11}$$

Each type of MOSFET owns a fix FOM, so the relationship and tradeoff between gate charge and on-resistance can be observed from the equation. The

larger the gate charges the smaller the on-resistance. Hence to obtain a MOSFET with low $R_{dson}$ and low $Q_g$ at the same time is impossible. Our selected 7V LDMOS in TI PDK have a low FOM of $28.4m\Omega - nC$. To design MOSFETs with the lowest overall loss, the gate charge and the on-resistance were iteratively varied to find the optimum point. The consideration of designing heavy-mode MOSFET would be introduced below.

## 3.3.1 Switching MOSFET Design

The switching MOSFET in heavy-load mode would be design first. The synchronous buck converter works in CCM during heavy load, and because the large current flow through power switch, conduction loss dominants in this situation. Hence a low $R_{dson}$ on-chip Power Switch is essential for heavy load efficiency boost. Fig 3.2 shows the the trend of full load open loop efficiency when size of control MOSFET varies.

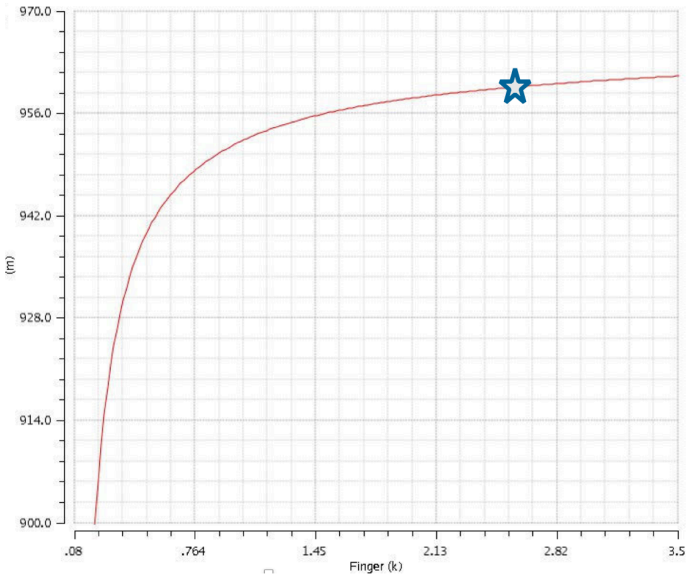


**Fig 3.2 Eff vs Area for Control MOSFET in Heavy-buck Mode**

The efficiency almost saturated when finger is larger than xxx. The benefit

from continuing increasing size of MOSFET is small. From the consideration of chip area, we chose the finger number of xxx. As the heavy-load mode would handle high load current in CCM, a small $R_{dson}$ is preferred. From the simulation result in Figure 3.2, the larger the $R_{dson}$, the smaller the efficiency, which is as expected. The same method would be used in choosing the size of synchronous MOSFET. The size of synchronous MOSFET is determined as xxx.

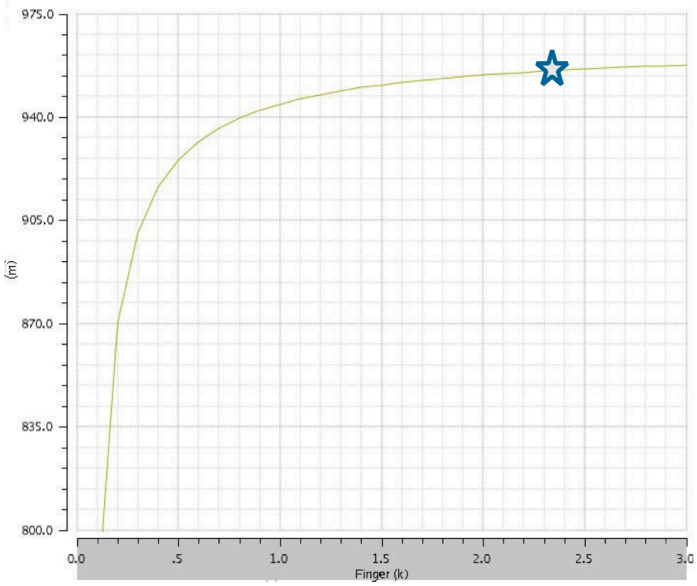


**Fig 3.3 Eff vs Area for Synchronous MOSFET in Heavy-buck Mode**

The character of heavy-load mode MOSFET is summarized in Table 2.

**Table 2: Parameter summarize for heavy-buck mode**

| **Active Mode** | $R_{dson}$ | **Cgd** |
|---|---|---|
| Control MOSFET | 20mohms | 169pF |
| Synchronous MOSFET | 13mohms | 242pF |

As the converter works in baby-buck mode, conduction current become relatively small, and hence the ratio of conduction loss in total MOSFET loss decrease, while switching loss matter in this case. So a design strategy

with low Ciss and Coss would greatly reduce turn-on loss and crossover losses during MOSFET switching transition. After same iteration simulation process, The character of heavy-load MOSFET is summarized in Table 3.

**Table 3: Parameter summarize for baby-buck mode**

| Baby-Buck Mode | $R_{dson}$ | Cgd |
|---|---|---|
| Control MOSFET | 120mohms | 27pF |
| Synchronous MOSFET | 51mohms | 62pF |

Through comparison, we can find the optimum MOSFET for baby-buck mode owns larger $R_{dson}$ and $C_{gd}$. This follow the general design trends in (xx)-(xx). For light-load case, the gate charge has the biggest impact on MOSFET losses. The proposed top baby MOSFETs has a small $C_{gd}$ of 27 pF. For heavy load case, the on-resistance must be kept low to prevent excessive conduction loss. The on-resistance $R_{dson}$ is 20 mΩ for the top heavy MOSFET, and it is even lower, 13 mΩ, for bottom MOSFET due to a longer conducting period.

To demonstrate the effectiveness of the baby-buck mode, a loss breakdown comparison at 80mA load current is performed in Cadence.

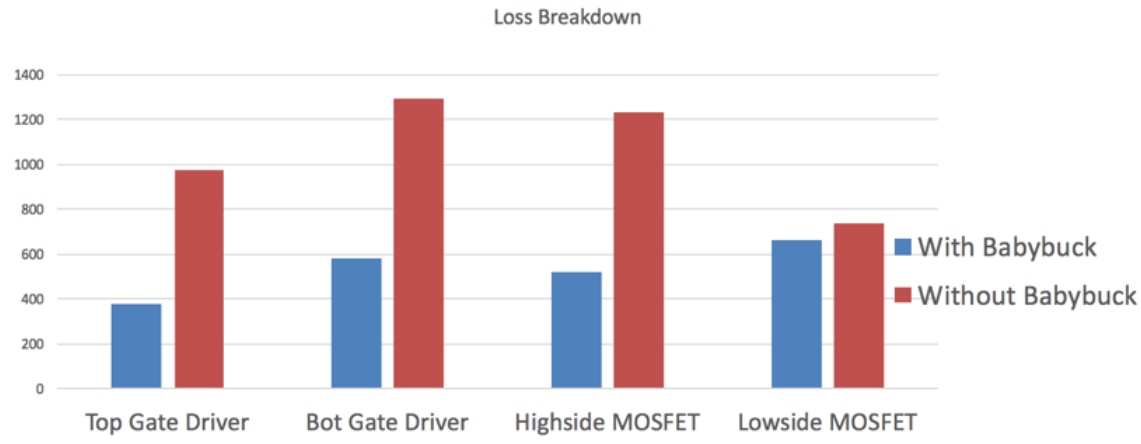


**Fig 3.4 MOSFET and Gate Driver Loss Comparison between w/wo Baby-buck**

In the comparison, the heavy-load mode is applied in light load to compare

with the baby-buck mode. Both case works at 80mA load current in DCM. The total power loss for heavy-load mode MOSFET is 4.24mW, while the baby-buck mode consumes 2.14mW. The power loss in MOSFET and gate driver reduce to 50%, which demonstrate the effectiveness of baby-buck mode. The ratio of driver loss and MOSFET loss in overall loss breakdown would be introduced in chapter 4.

### 3.3.2 Off-chip Components Design and Selection

The inductor and output capacitor are the two discrete components in the power stage. Since the two mode concept and Constant on-time V2 control are applied in our proposed converter, the inductor would determine the mode transition point in proposed converter, and the character of capacitor would affect the stability of control loop, hence extra attention should be paid during the design procedure. The design procedure of inductor is introduced first, then the consideration of capacitor selection is present.

The inductance of inductor decides the current ripple as below[x]:

$$\frac{\Delta I_L}{2} = \frac{(V_{in} - V_{out}) * D}{F_s * L} \tag{12}$$

The larger the inductance, the smaller the inductor current ripple. A good estimation for the inductor current ripple $\Delta I_L$ is 20-40% of the maximum output current [29]. However, the inductor current ripple also determines the boundary of CCM and DCM. Due to our heavy-load mode only works in CCM and baby-buck mode only works in DCM, the inductance would determine the mode transition point is proposed converter. What's more, in

the COT V2 control, the inductor ripple current also relates to capacitor esr voltage, which is important in control loop. The 30% current ripple is selected as a starting point for design. With $V_{in}$ =5V,$V_{out}$ =1.2V, $D$=0.24, $F_{sw}$ =250kHz, $\Delta I_L$ =30%, $I_{out\_max}$=1200mA, the inductance is obtained as 10.1 μH. The following equation is used to verify the theoretical critical load current for CCM / DCM boundary, which is obtained as180 mA for the design.

$$I_{o\_crit} = \frac{(V_{in} - V_{out}) * V_{out}}{F_{CCM} * 2L * V_{in}} \tag{13}$$

So the inductor 2100LL-100-H-RC is selected as our output inductor, which have 10uH inductance and 5mohms DCR.

Then we can design the output capacitor. The capacitance of output capacitor and its ESR would determine the output voltage ripple.

$$\Delta V_{Co} = \frac{\Delta I_L}{8 * F_{sw} * C_o} \tag{14}$$

$$\Delta V_{esr} = R_{esr} * \Delta I_L \tag{15}$$

$$\Delta V_{out} = \Delta V_{Co} + \Delta V_{esr} \tag{16}$$

The equation xx and xx can used to calculate the output voltage ripple cause by the capacitor ESR and capacitor itself. Generally, the ESR of capacitor should be chosen as small as possible to minimize loss. However, in the constant on-time V2 control, the control loop need to sense the $\Delta V_{esr}$ information to control the voltage regulation. Achieving stable in a COT V2 without external ramp and error amplifier, the output voltage ripple that

cause by capacitor ESR must dominant in output voltage waveform[shuiling], also, the capacitor should satisfy the condition that in equation xx.

$$R_{Co}C_o \geq \frac{T_{on}}{2} \tag{17}$$

Otherwise, the sub harmonic oscillations would happen due to the phase delay in capacitor voltage ripple. (shown in figure 3.5)

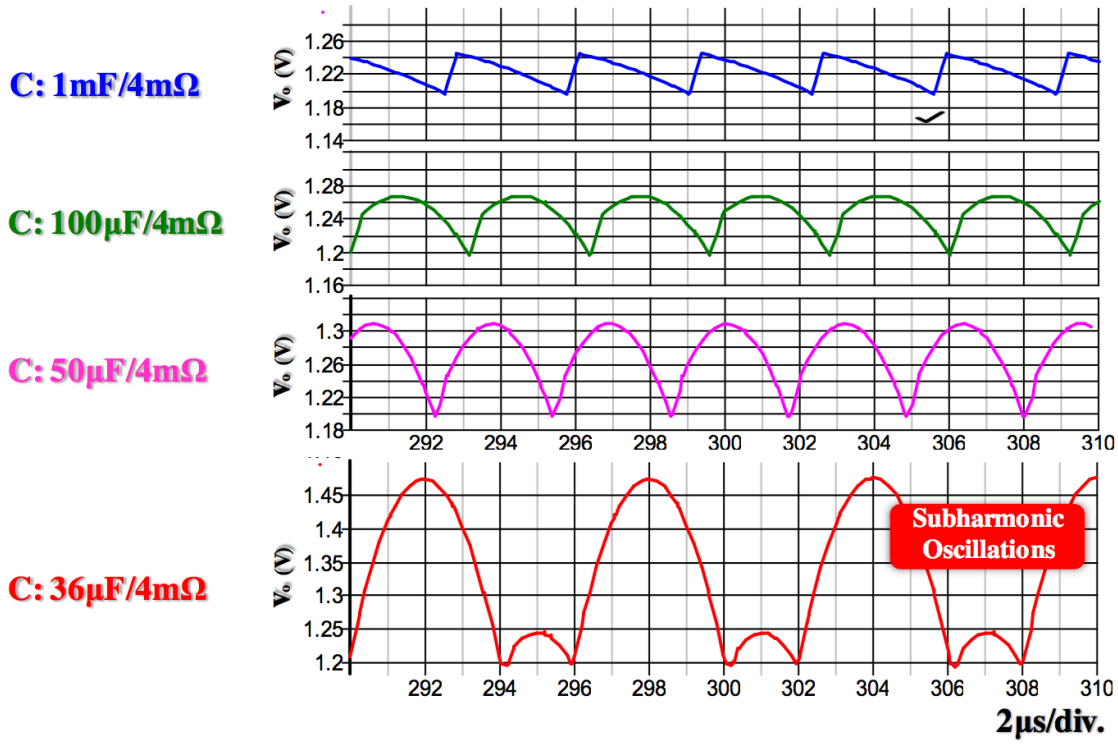


**Fig 3.5 Sub-harmonic Oscillations due to Small Output Cap Time Constant [9]**

The proposed converter has output voltage ripple specification of 30mV, so 18 mV ESR voltage ripple results in 50 $m\Omega$ ESR resistance, and 2 mV capacitor voltage ripple results in 90 !F output capacitance. An OSCON capacitor (P16360CT-ND) with 82 µF and 45 $m\Omega$ ESR is selected for the proposed power stage. The OSCON cap has a long life span, and its ESR is stable from -55oC to 105oC, which is important for the target design as the

control information is based on the ripple across the ESR. Simulation results indicate that the chosen capacitance value provides good stability and keeps the output voltage ripple within the specification throughout the entire load range.

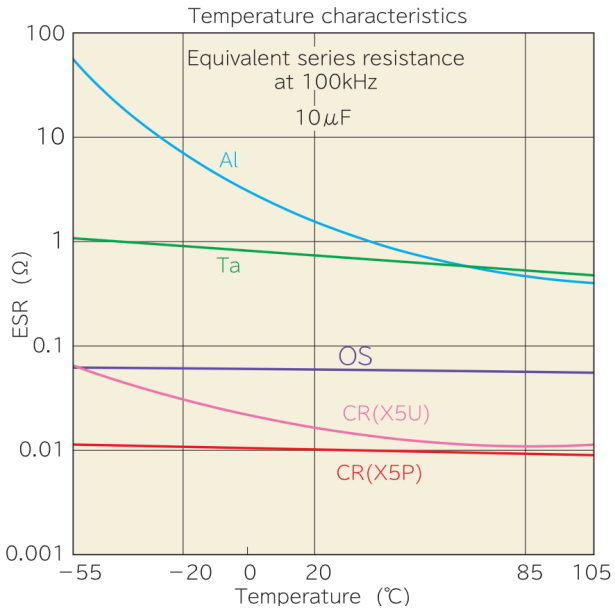


**Fig 3.6 Temperature Characteristic of Selected Output Capacitor [23]**

# 3.4 The Controller Circuit in Proposed Converter

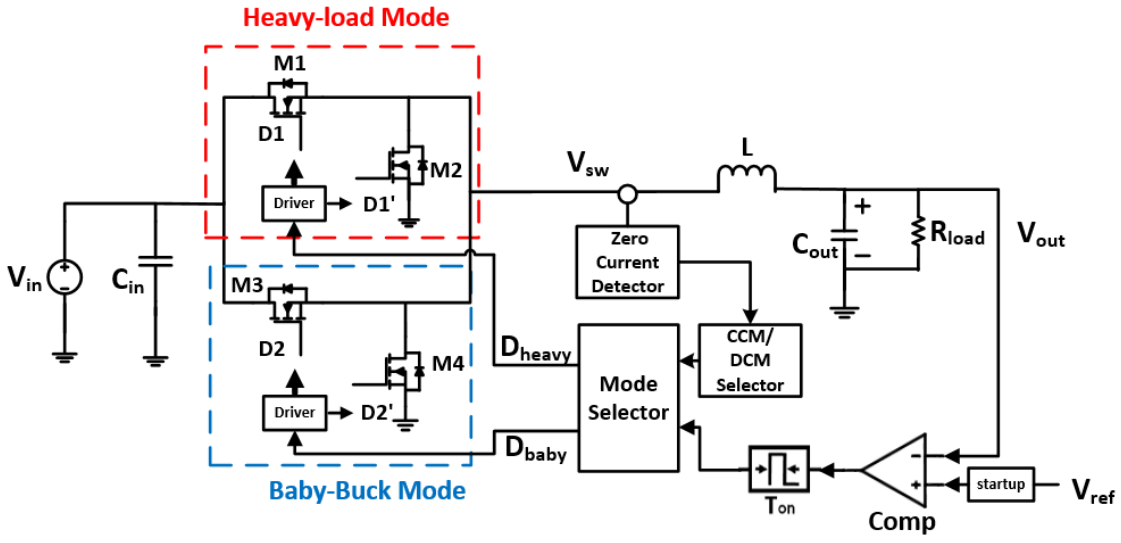

**Fig 3.7 Full Diagram of Proposed Two-mode Buck Converter**

The proposed converter combined the heavy load mode and baby-buck mode converter into a single converter. These two mode would share the inductor, output capacitor and controller, which include the comparator, constant on-time generator, zero current detector, CCM/DCM selector, and mode selector. The monolithic buck integrated switching MOSFET and controller in one chip to minimize off-chip components, only input cap, output cap, inductor, the bootstrap cap and bootstrap diode connected outside the chip. With the zero current detector and CCM/DCM selector, the proposed converter can sense the load current level without sensing resistors, which further reduce the off-chip components.

## 3.4.1 Operation of Proposed Converter

The proposed converter shows in Figure 3.7 work in the load range from 10mA(12mW) to 1200mA(1440mW), where Baby-Buck mode handle the load range from 10mA(12mW) to 180mA(196mW) and Heavy-load mode deal with the load range from 180mA(196mW) to 1200mA(1440mW). The switch in Baby-Buck mode is optimized for low current condition, where MOSFET owns small gate charge $Q_g$. The switch in Heavy-load mode owns a lower on-resistance $R_{dson}$.

When converter works in heave load condition (load current > 180mA), the heavy-load mode activates, at the mean while, the baby-buck mode turns off. The heavy-load mode only works in continuous conduction mode. During the duty cycle period, the mode selector would turn on the M1 and turn off M2, when M1 turns on, the input source would charge the inductor, where inductor current would increase with the slope of:

$$s_{inc} = \frac{V_{in} - V_{out}}{L} \tag{18}$$

When M1 turns off and M2 turns on, the inductor is disconnected with input source, while supply energy to load individually. The inductor current decrease with the slope

$$s_{dec} = \frac{-V_{out}}{L} \tag{19}$$

When converter works in light load condition (load current < 180mA), the Baby-buck mode activates, at the mean while, the heavy-load mode turns off. The Baby-buck mode only works in discontinuous conduction mode. The difference between heave load operation and light load operation is that there would be a period when both switch in power stage would turn off, only output capacitor can supply energy to the load. This stage happens when the inductor current reach zero, then the synchronous MOSFET would turns off to forbid reverse inductor current, hence increase efficiency at light load. Both mode would have 360mA inductor peak-to-peak current ripple, so when load current decrease below 180mA, the mode would transit from heavy-load mode to baby-buck mode.

As show in Figure3.7, the Zero Current detector only provide function for the DCM operation. The DCM/CCM selector works all the time to detect the load condition of converter. Because of the Constant V2 control is used, the comparator would detect output voltage ripple and trigger the constant on-time generator to generate constant on-time signal.

When proposed converter works in continuous conduction mode, the comparator with 1.2V input reference voltage would detect if output voltage

drop to 1.2V. As the output voltage drop below 1.2V, the comparator's output become high, hence trigger the on-time generator generate the square waveform with 1us constant on time and 0.3us minimum off time. As inductor current would not touch zero in heavy load, the CCM/DCM detector's output is high, which indicated converter works in heavy load. Then the mode selector would combine the information from CCM/DCM detector and on-time generator to control M1, M2, M3, M4. The difference operation in light load is when inductor current touch zero, the mode selector would know converter need to enter DCM, then an extra period where all switches shut down would add to the working period of converter operation.

### 3.4.2 Constant On-time Generator

The COT pulse generator creates a fixed on-time pulse through the capacitor charging/discharging timing circuit. Each fixed on-time period is succeeded by a minimum off-time period to protect the timing capacitor. In the design, a 1us constant on time and 300ns minimum off-time allow the generator create a series on pulse with maximum 77% duty cycle.

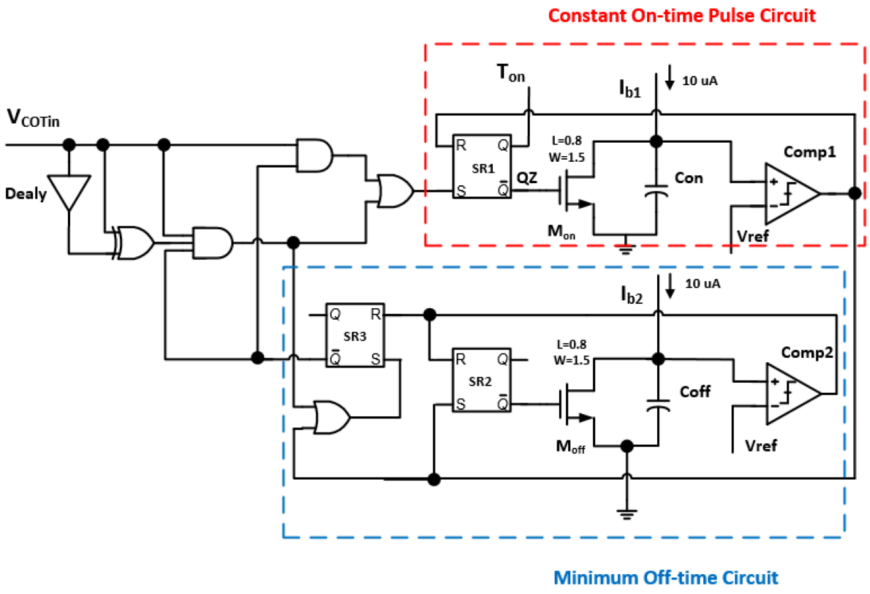


**Fig 3.8 Circuit Diagram of Constant On-time Generator [4]**

Figure 3.8 shows the structure of COT pulse generator, which is a reference of Zhao's thesis work. The $V_{COTin}$ is generate from comparator in Figure 3.7, a delay buffer and XOR gate is used to detect the rising edge of $V_{COTin}$ signal. Because of a fix on-time period is need, the timing circuit is required for the circuit. In the implementation, the charging capacitor timing block is used. The capacitor is charged with fix current, and equation xx shows the relationship between time and capacitance.

$$t = \frac{CV}{I} \tag{20}$$

To prevent a continuous on time pulse generated by the generator, a minimum off-time is introduced into this block. Another minimum off time timing circuit guarantee a 0.3us rest between each on-time pulse. This not only protects the timing capacitors, but prevent a long turn on time in controlling MOSFET, which may result in the inductor saturation. Because of the fix on-

time and minimum off time, a theoretical maximum duty cycle 77% is design inherently.

## 3.4.3 Zero Current Detector

The Zero current detector is necessary for the proposed converter works in DCM mode, it can detect when the inductor current touch zero and give a signal to turn off the synchronous MOSFET. Lots of research give the ZCD circuit in their application [24] [25] [26]. Normally, the performance of the zero current detector is depending on the performance of comparator. In the proposed zero current detector, a fast comparator topology in [27] is applied. A general structure for ZCD is used in the proposed design. Fig 3.10 shows the structure of the ZCD circuit.

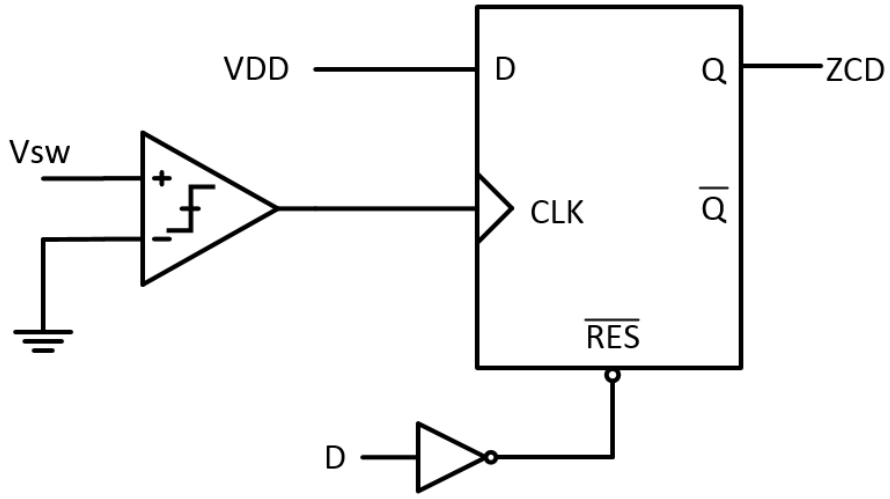


**Fig 3.9 Circuit Diagram of Zero Current Detector**

The comparator in Fig 3.10 can continuous detect the switching node voltage in buck converter. As long as the voltage become positive, a clock signal would send to the following D flip-flop, since the D terminal in the D flip-flop is always connect to $V_{DD}$, once the clock signal arrive, the output would become high. The reset terminal of D flip-flop is connecting to the gate

signal of control MOSFET, when the control MOSFET turns on, the switching node voltage would equals to $V_{in}$, the reset function in D flip-flop can prevent the false trigger of ZCD signal during that period. Hence, the zero current detector would only detect if the clock signal arrives when the synchronous MOSFET turns on. The ZCD signal can also utilized in CCM/DCM Detector to detect if the converter works in CCM or DCM. The detail would be explained in the following section.

## 3.4.4 CCM/DCM Detector

In order to change mode from heavy-load mode to sleep mode or change from sleep mode to heavy-load mode the circuit needs to know when the voltage regulator works in CCM or DCM. While the converter works in CCM, the heavy-load mode should be active, and when the converter works in DCM, the baby-buck mode (sleep mode) should be active. Hence a that can detect the converter's conduction mode is necessary.

Instead of the sensing resistor, the proposed design utilizes the difference of signal's time sequence in DCM and CCM to achieve the detection of current conduction mode.

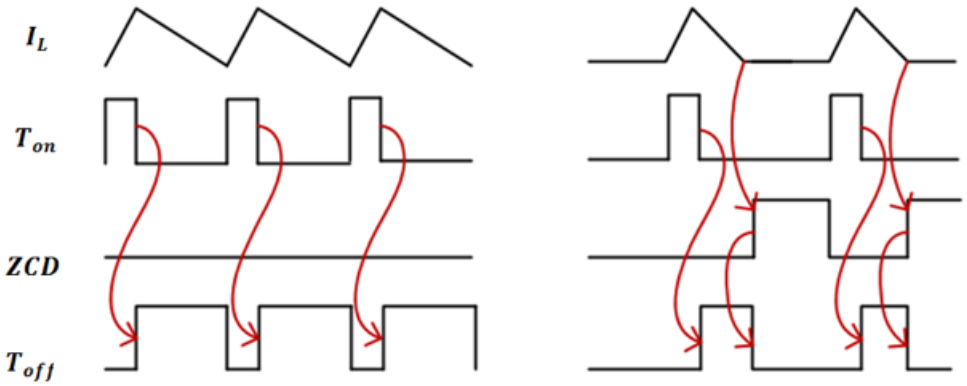


**Fig 3.10 Signal Time Sequence in CCM and DCM**

Fig.3.11 shows the converter's signal timing sequence for CCM and DCM. The $I_L$ represents the inductor current, $T_{on}$ represents the gate signal of control MOSFET, ZCD represent the output of zero current detector and $T_{off}$ represents the gate signal of synchronous MOSFET. As the converter works in CCM mode, the ZCD signal always remain at low level. When the converter works in DCM mode, the ZCD signal would rise in last switching cycle. The difference between CCM and DCM can be utilized to sense if the converter works in CCM or DCM in last switching cycle. Fig3.12 shows the circuit used to detect the deference of timing sequence in DCM and CCM.

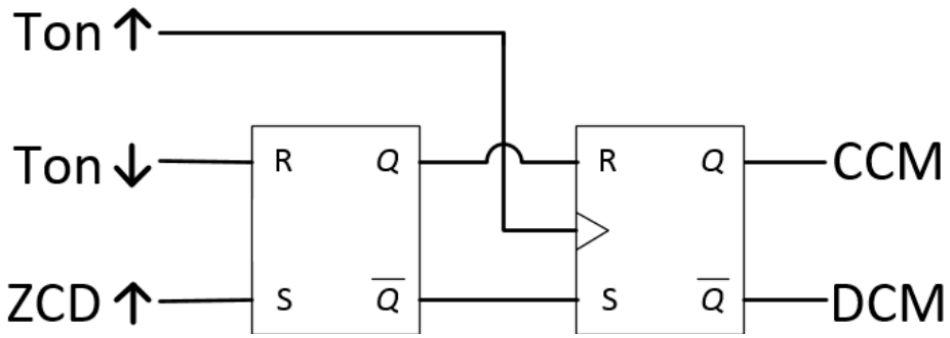


**Fig 3.11 Circuit of CCM/DCM Detector**

In the circuit above, the rising edge of $T_{on}$ is used as the clock signal of second SR latch, when the rising edge is detected, the output of first SR latch would determine if converter works in CCM or DCM. If the circuit works in CCM, the rising edge of ZCD signal would never appear, hence the output of first SR latch is Q equals to 0, when the next cycle's $T_{on}$ rising edge coming the output of whole circuit would be "CCM". If the circuit works in DCM, the ZCD rising signal always appear after the falling edge of $T_{on}$, hence the output of this circuit would be DCM.

## 3.4.5 Customized Gate Driver

In the switch mode converter, shoot-through current loss is another major loss beside conduction loss and switching loss [28]. Hence the gate driver should be carefully design to avoid shoot through happen during switching transition. A build-in customize dead time achieved through different size change in cascade inverter stage which makes the turn-on speed different from turn-off speed. Base on the size of power transistors, a tapering factor of 3 to 4 is selected to design the cascade inverter stage [29]. As shown in Fig.3.13, the M1, M4, M5, M8 and M2, M3, M6, M7 increase gradually, while the increase scale of M1, M4, M5, M8 are smaller than M2, M3, M6, M7 which results the gate signal through turn-on path have larger on-resistance compare to the turn-off path, and lowering the turn on speed to achieve the build-in dead time. In the simulation, a fixed 20ns turn on and turn off dead time is designed to avoid power switches conduct at the same time. Also, the size of inverter chain also optimized for avoiding the high dv/dt shoot through happen during high-side MOSFET turns on procedure [30].

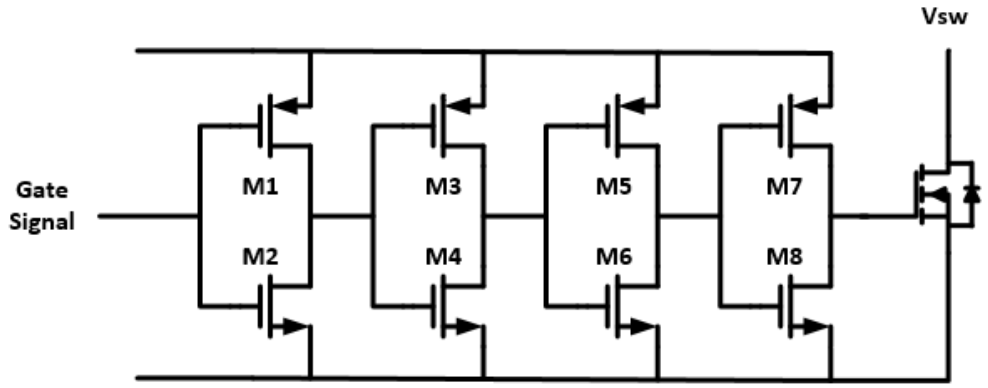


**Fig 3.12 Structure of Gate Driver in Heavy-buck Mode**

# Chapter 4

## Simulation and Measurement Result

This chapter describe the functionality of proposed converter through simulation in cadence. It includes the close loop simulation results, open loop power stage measurement result, and close loop efficiency measurement. Finally, future improvements for the proposed two-phase converter are offered and the chapter is summarized.

## 4.1 Close Loop Simulation Through Designed On-chip Components

The proposed converter is implemented in 0.25um CMOS process, and the performance is validated in cadence, where the steady state waveform, transit response, efficiency measurement and power loss breakdown is presented in this section.

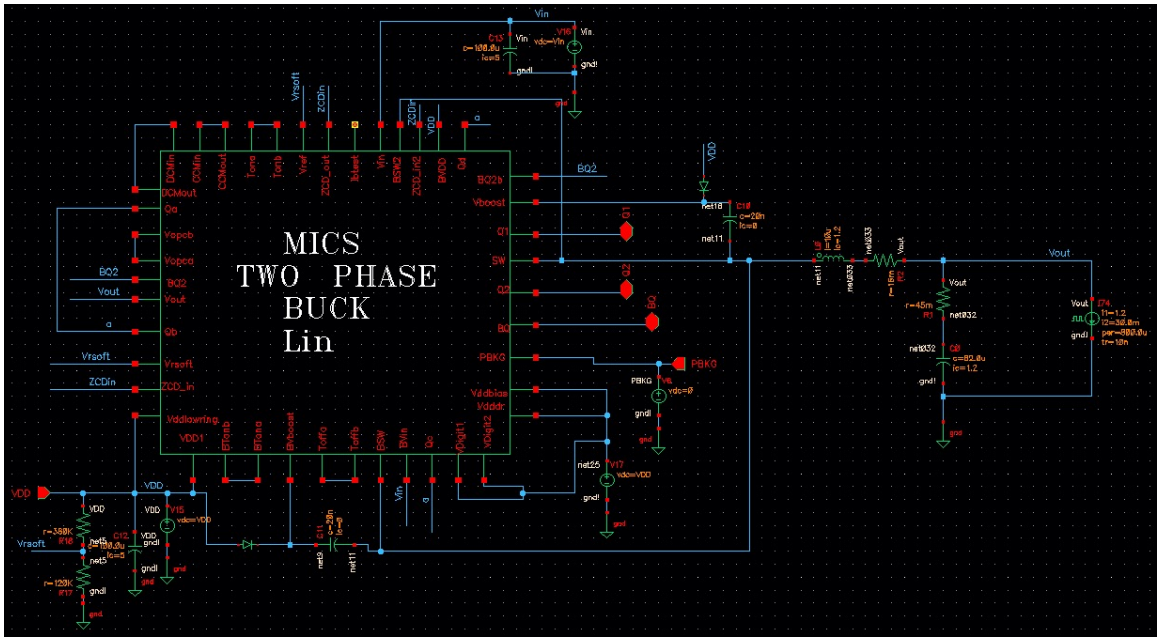


**Fig 4.1 Test Bench of Proposed Converter in Cadence**

Figure 4.1 shows the test bench in Cadence. A 5v input voltage supplied the test bench and another 5v supply voltage supplied the power of controller. Two small resister add to simulation to bring the effect of DCR and ESR of Off-chip inductor and capacitor into simulation.

## 4.1.1 Steady State and transient Waveform

The steady state waveforms of the proposed converter are shown in Figure 4.2, which include the output voltage, inductor current, Constant on-time pulse, switching node voltage and CCM/DCM indicator. The inductor current in pink in Figure 4.2 have a peak to peak current of 378mA. Due to the heavy mode converter works in CCM, a continuous inductor current is presented. The red one shows the 1.2V output voltage with 17mV voltage ripple. The blue one shows the output of constant on-time block, which have 1.06ms on-time. The high voltage of shown CCM/DCM indicator means that converter works in continuous conduction mode, also the Vsw is shown last, the small

negative spike in Vsw is cause by the dead time of proposed converter, the parasitic diode of power MOSFET would turn on at that time, hence a large negative voltage around 700mV shows.

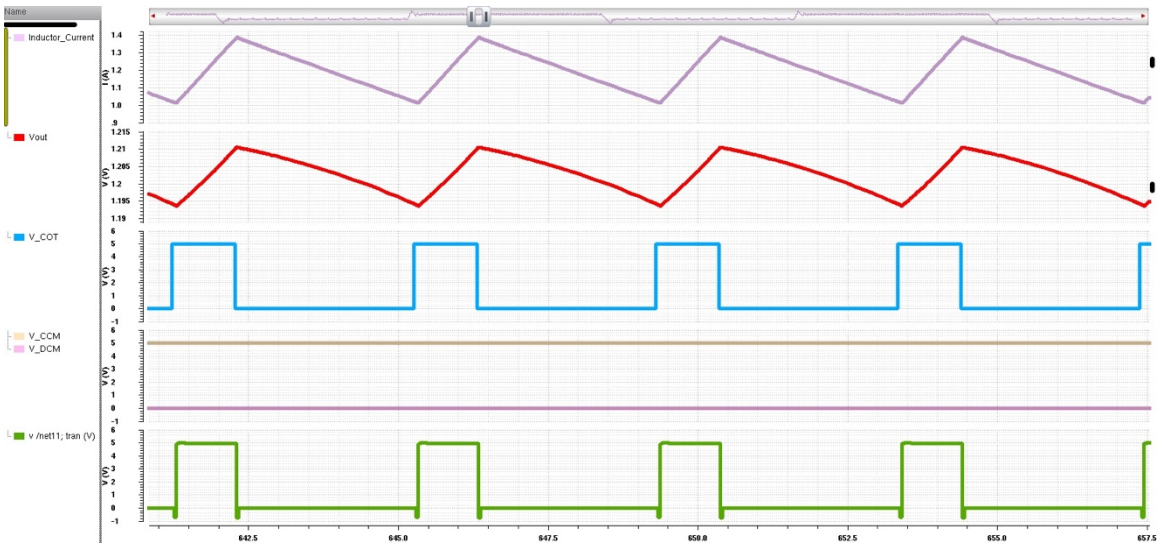


**Fig 4.2 Heavy Load Steady State Variable Simulation result in Cadence**

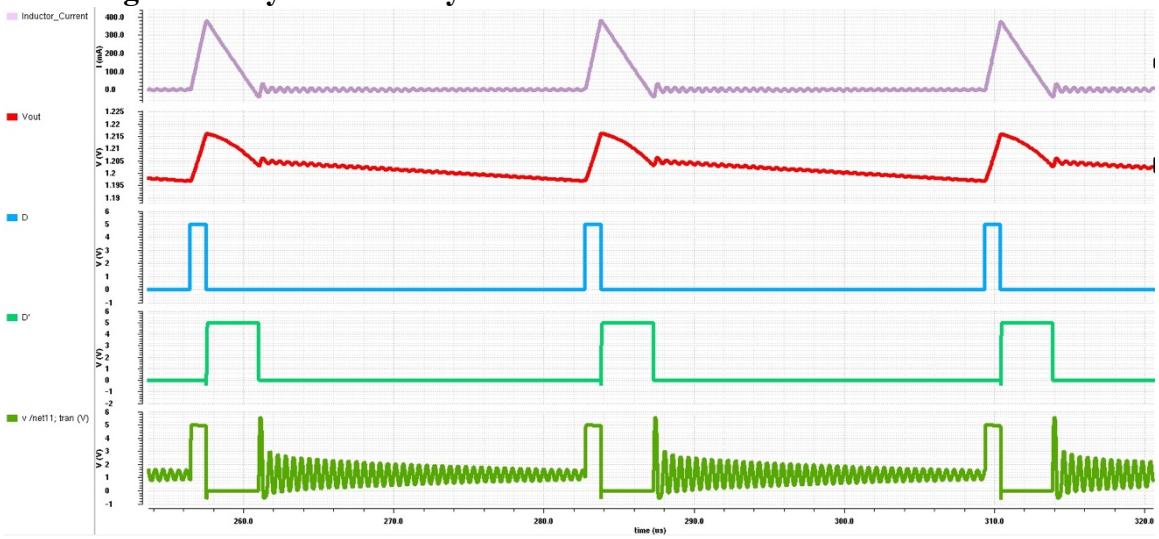


**Fig 4.3 Light Load Steady State Variable Simulation result in Cadence**

Figure 4.3 shows the steady state that converter works in light load, where a discontinuous inductor current shows the converter works in DCM. The inductor current ripple still remains the same under DCM, while output voltage ripple slightly increase to 19mV. From the Switching node voltage,

we can find the converter works in three stage in one full period. The control MOSFET would turn on first, and input source would provide energy to load, at the same time the inductor current and output voltage increase. Then the control MOSFET turns off, and synchronous MOSFET turns on, the inductor provide energy to load. At last, both MOSFET turns off and the output capacitor provide energy to load, the ripple is induced by the resonant of inductor in power stage and the parasitic capacitor of MOSFET. The control signal of each MOSFET below shows the turn on/off order of power MOSFETs. Also, From the output of constant on-time block, we can find the on-time still remains around 1us, while the frequency reduced to 38kHz as expected. The frequency is reduced by increasing the off-time. Also, it can help to reduce switching loss at light load.

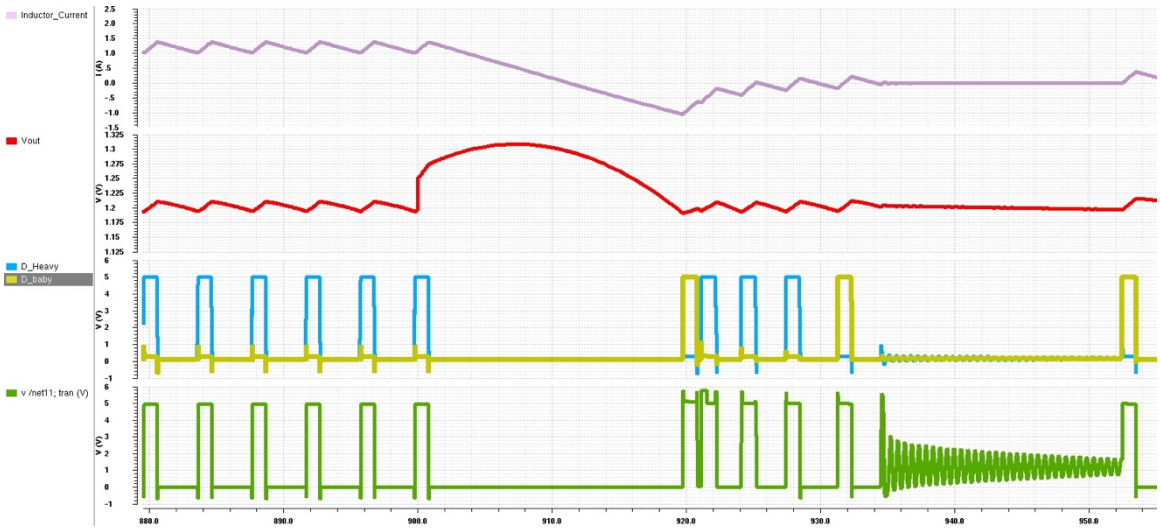


**Fig 4.4 Step Down Transient Response Simulation in Cadence**

Figure 4.4 shows the simulation waveform of step down transient response; the converter switches from active mode(1.2A) to baby-buck mode(30mA) which is the maximum load and minimum load of proposed converter. The control signal shows that the gate signal for heavy load would turn off first then the baby-buck mode would activate and switching frequency reduced.

The over shoot voltage is around 100mV, and the settling time is around 17uS which still meet the specification.

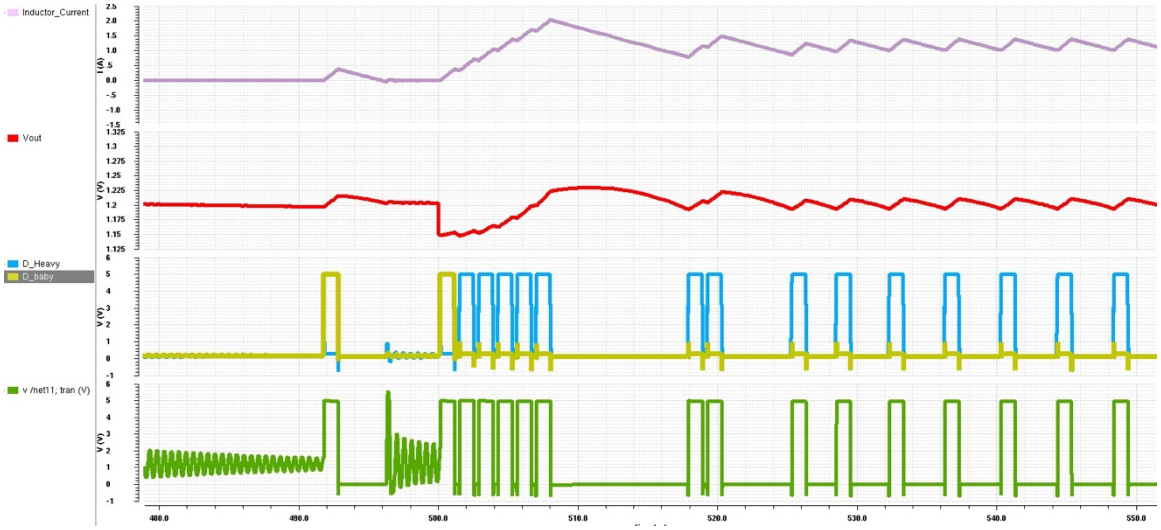


**Fig 4.5 Step up Transient Response Simulation in Cadence**

Figure 4.5 shows the simulation waveform of step up transient response, the converter switches from baby-buck mode(30mA) to active mode(1.2A). During the transient process, a compact constant on-time signal is generated to increase the inductor current to load current level. The active control MOSFET's gate signals change from baby-buck mode to heavy load mode. The under shoot voltage is around 50mV and the settling time is around 7us.

# 4.2 Efficiency in Circuit Level Simulations

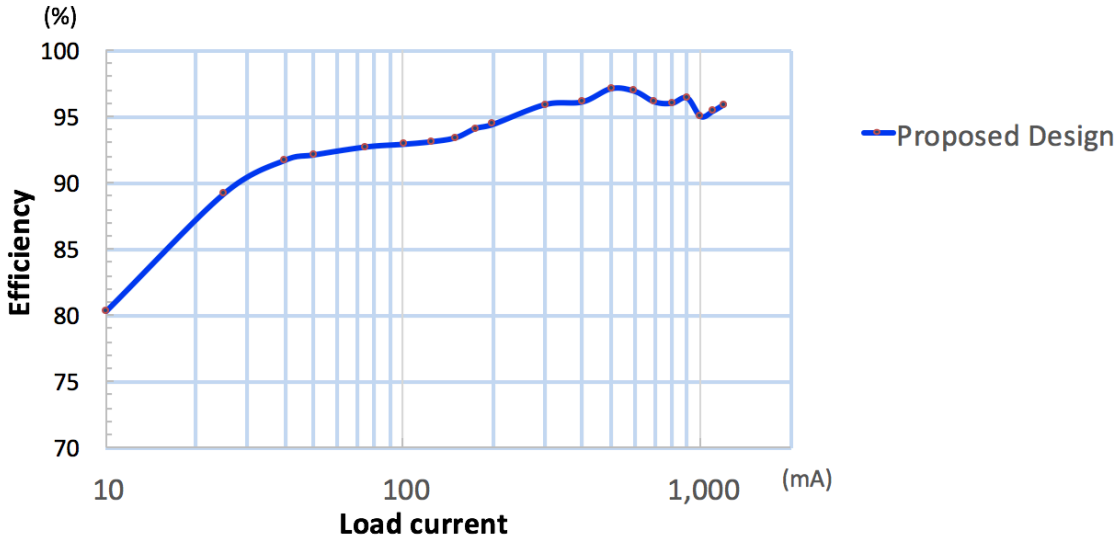


**Fig 4.6 Efficiency Distribution**

According to the same test bench shows in Figure 4.1. The efficiency of proposed converter is acquired by the load power over the total supply power from input voltage source and control voltage source. Figure 4.6 shows the overall efficiency of proposed converter. Where the efficiency is above 80% for the entire load range, a maximum efficiency 97.1% is achieved at load current of 500mA.

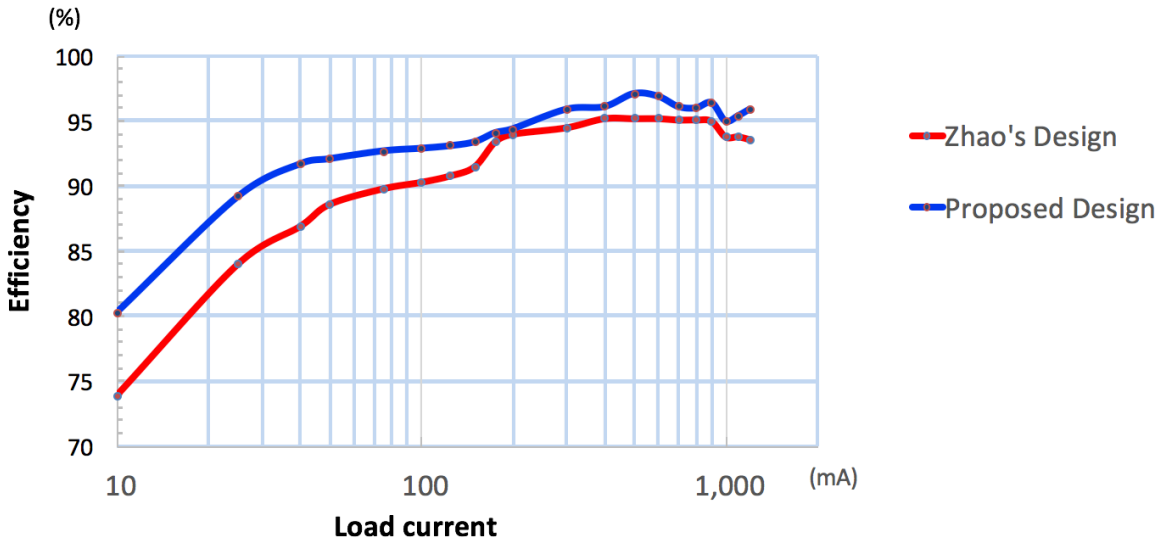


**Fig 4.7 Efficiency Comparison in Cadence Simulation**

Figure 4.7 shows the efficiency comparison between Zhao's design and the proposed design. The proposed converter is more efficient throughout the entire load range compare to Zhao's design. In the heavy load, the proposed converter improves the efficiency through replacing the sensing resistor with the designed DCM/CCM detector. In the light load, proposed converter replaced the Schottky diode with a synchronous MOSFET, which have no forward voltage and small on-resistance. Although the controller become more complicate and consume more power, there still have 5% efficiency improvement in simulation.

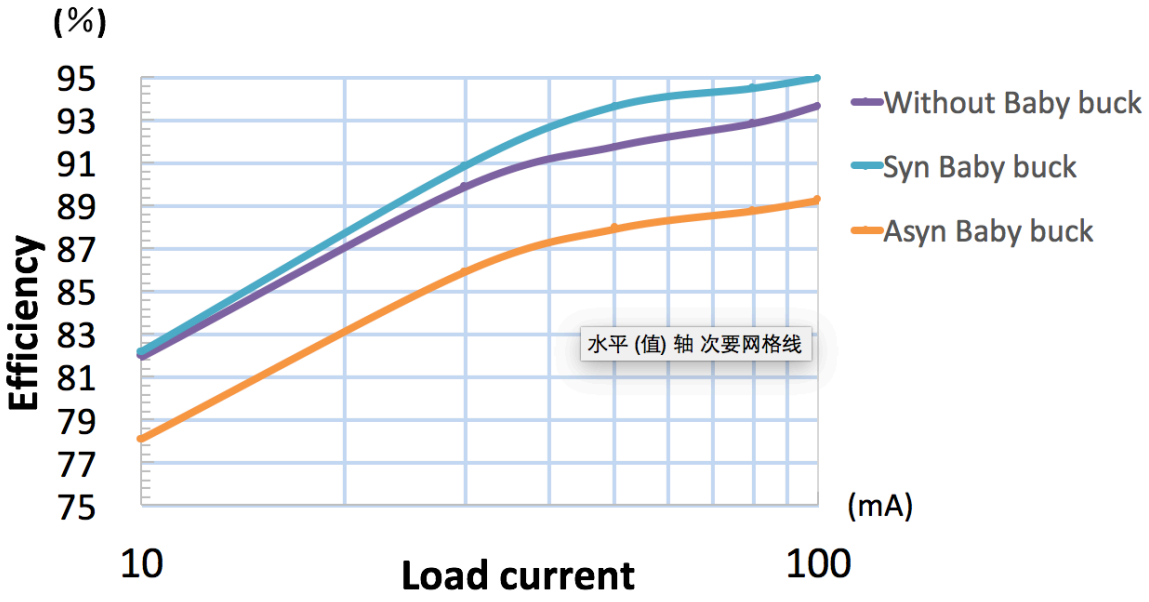


**Fig 4.8 Efficiency Comparison in Cadence Simulation**

Figure 4.8 shows the general load efficiency comparison among synchronous two-mode buck converter, synchronous buck converter and asynchronous buck converter. The result shows asynchronous buck converter have the lowest efficiency in these three case. Also, the loss breakdown in Figure 3.4 shows the main different between two-mode buck converter and synchronous buck converter. Figure 4.9 and Figure 4.10 shows the details of overall loss break down in two-mode buck converter and synchronous buck converter. With same controller, inductor and capacitor, the MOSFET loss reduced about 13% among load range 10mA to 100mA.

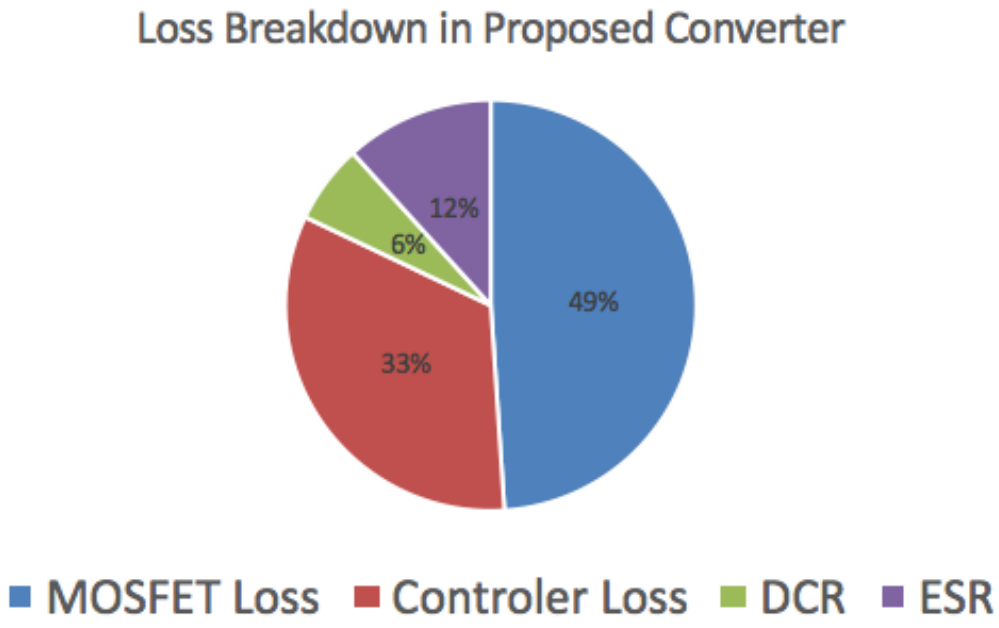


**Fig 4.9 Loss Breakdown in Proposed Converter**

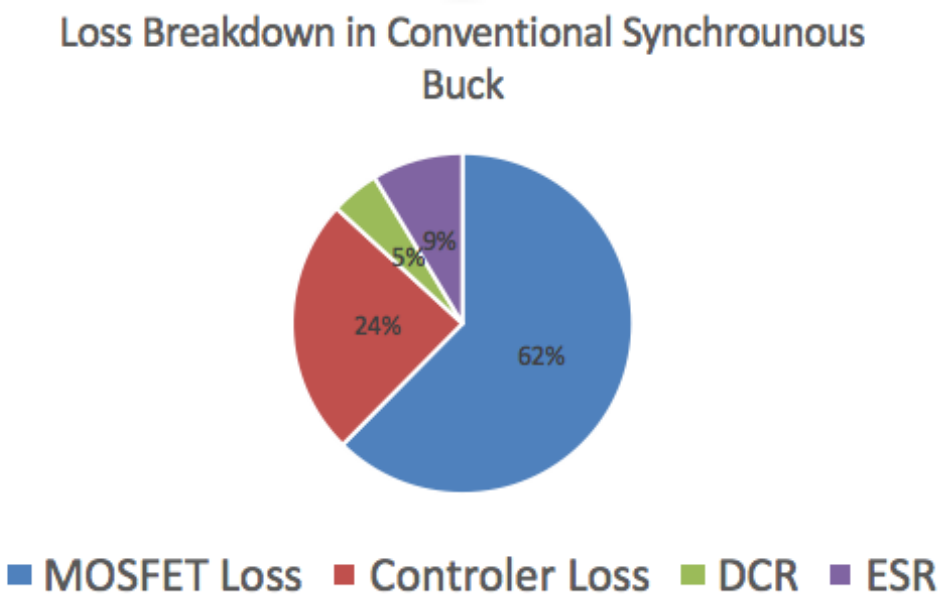


**Fig 4.10 Loss Breakdown in Conventional Buck Converter**

## 4.3 Measurement Result of Proposed Design

The tape out chip include the power stage of baby-buck mode and heavy load mode, which each contain two power MOSFETs, and the controller which include the comparator, constant on-time block, mode selector, zero current detector. The functionality of key block and efficiency of proposed converter would be presented in this section.

### 4.3.1 Functionality of Constant on-time and ZCD

The functionality of Zero current detector is shown in Figure 4.11, where green curve is the switching node voltage and yellow one is the output of zero current detector.

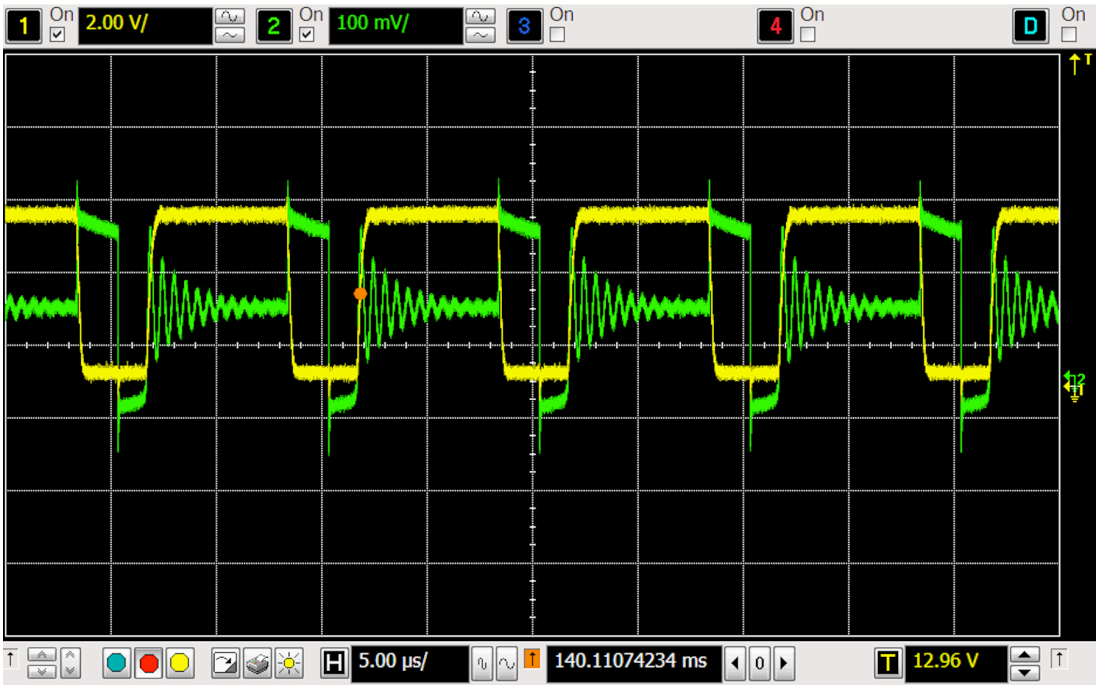


**Fig 4.11 Measurement result of ZCD signal and Vsw**

Due to the reset signal in D flip-flop, the output of ZCD would reset to zero when control MOSFET turns on. In Figure 4.11, the proposed converter is working in baby-buck mode(DCM), when ZCD signal become high, the synchronous MOSFET turns off, then converter enter the resonant period. The output capacitor would provide power to load.

Figure 4.12 shows a continuous output signal of constant on-time block, the waveform contains the design constant on-time and minimum off time information.

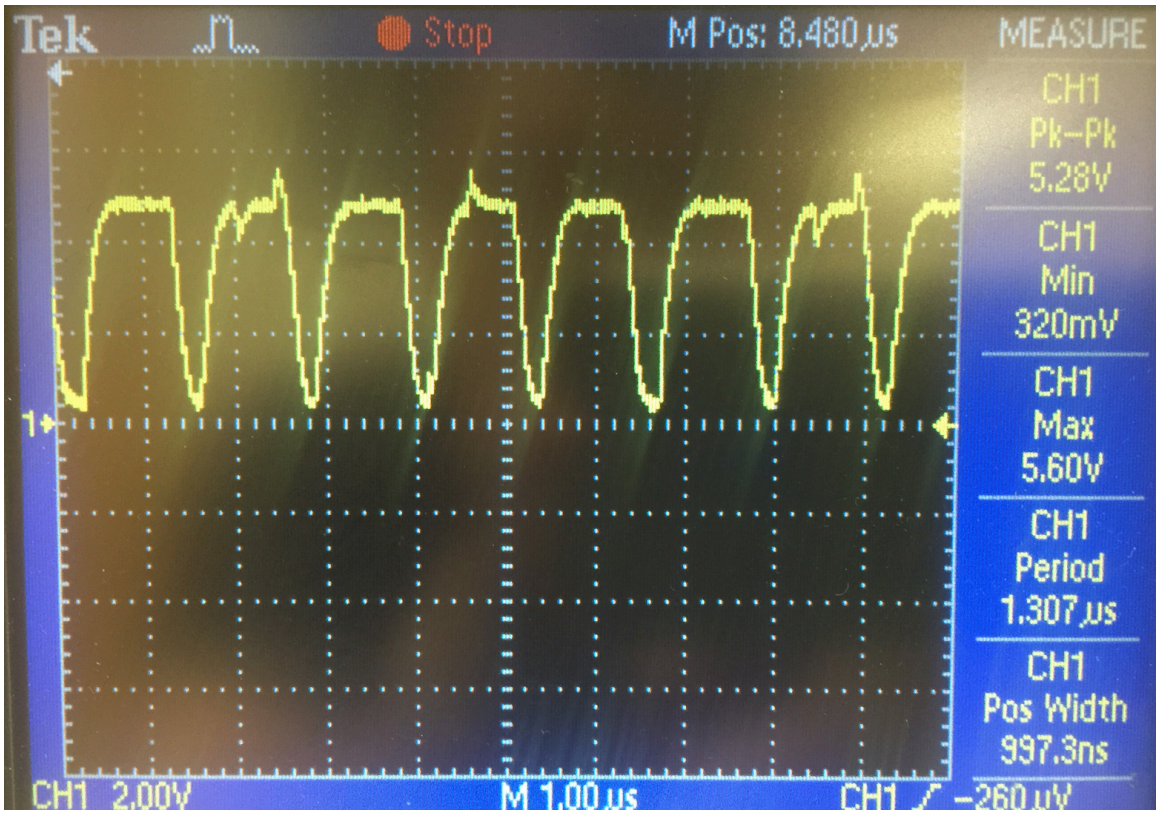


**Fig 4.12 Measurement Output of Constant On-time Block**

In the design, an expected 1us constant on time and 0.3us minimum off time was measured. From Figure 4.12, a continuous signal with 1.307us period presented, and the pulse width is 997.3ns, which meet our desired design. To measure the block separately, all the pin of constant on-time block

and zero current detector are connected outside the chip. Due to the large parasitic capacitor of on-chip pads, the slew rate of rising slope and falling slope reduced.

### 4.3.2 Functionality of Power Stage and Gate Driver

The functionality of baby-buck mode and heavy load mode is tested under 5V input voltage, and a simulated constant on-time signal is generated through function generator. As shown in figure 4.13, the yellow waveform shows the switching node voltage. The yellow waveform shows that converter works in discontinuous conduction mode, and the load current is 30mA. The rectangular part means control MOSFET is on. Then the control MOSFET would turns off, and synchronous MOSFET turns on, the current flow from source terminal to drain terminal, so a negative voltage which equals to current times the $R_{dson}$ presents in that period. Then both power MOSFET would turn off, and the parasitic capacitor and the inductor in power stage begin resonant. Due to the delay of zero current detector, the synchronous MOSFET couldn't turns off exactly when current equals to zero. Hence extra energy in inductor induce the first peak voltage during resonant. After the resonant energy dissipated, the voltage at switching node equals to output voltage.

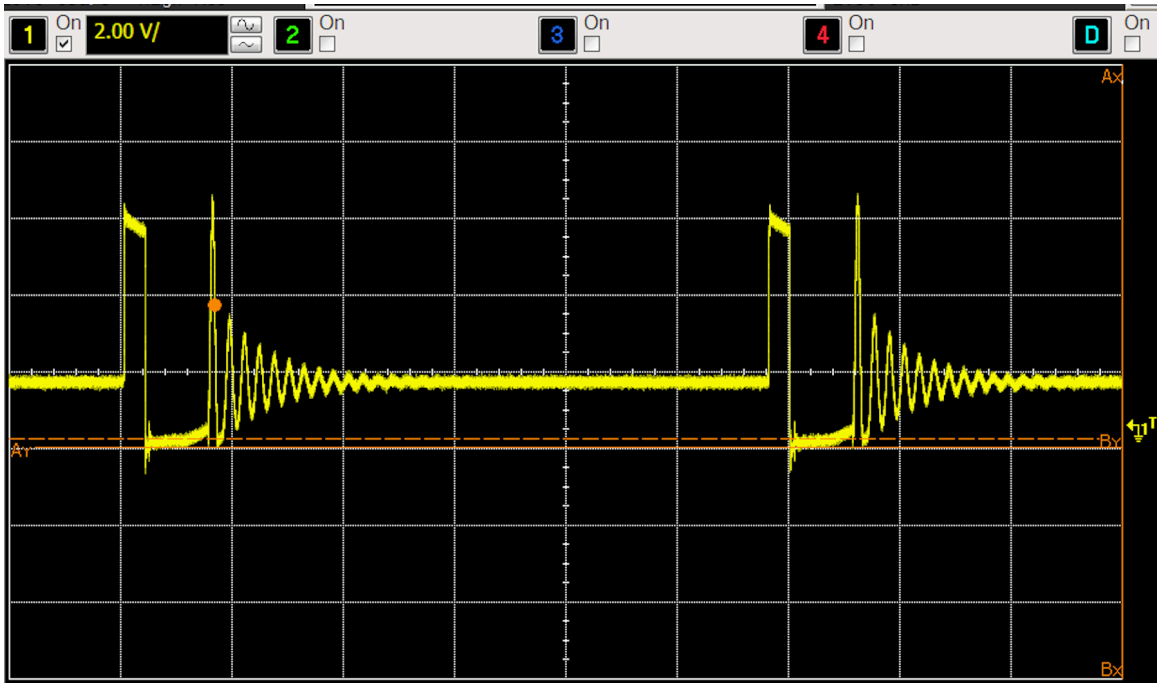


**Fig 4.13 Switching Node Voltage**

Since the gate driver and power MOSFET works correctly, the efficiency of power stage was measured. Figure 4.14 shows efficiency measurement result.

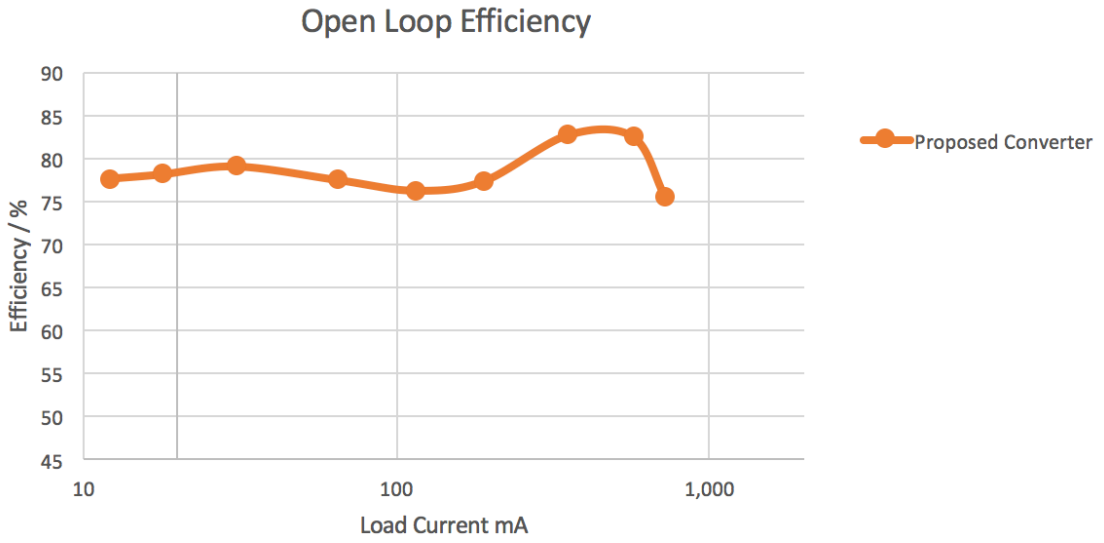


**Fig 4.14 Open Loop Efficiency Measurement Result**

The measurement results show the peak efficiency is 83% at round 400mA. And the overall efficiency is above 75%. In light load conditions (load current less than 180mA), the peak efficiency is 79% at 30mA, and quite stable between 10mA to 200mA. The valley around 200mA shows the baby-buck mode couldn't provide high efficiency as load current increase. As the design target, the heavy load mode would activate at 180mA load current, the MOSFET with smaller $R_{dson}$ would begin switching in heavy load mode to save loss. The measurement result also shows that efficiency begin to increase after the heavy load mode activated. Due to the insufficient wire width in gate driver, as the load current continue increase, the gate driver couldn't handle the large gate current, and the efficiency would drop quickly. This is an important issue that can be improved in the future.

### 4.3.3 Steady State and Transient Response Measurement result

In this section, the measurement results of steady state performance and step-up/step-down transient response is shown, the function of mode selector and frequency variation in baby-buck mode is validated.

Figure 4.15, Figure 4.16 and Figure 4.17 shows the frequency variation versus load power variation.

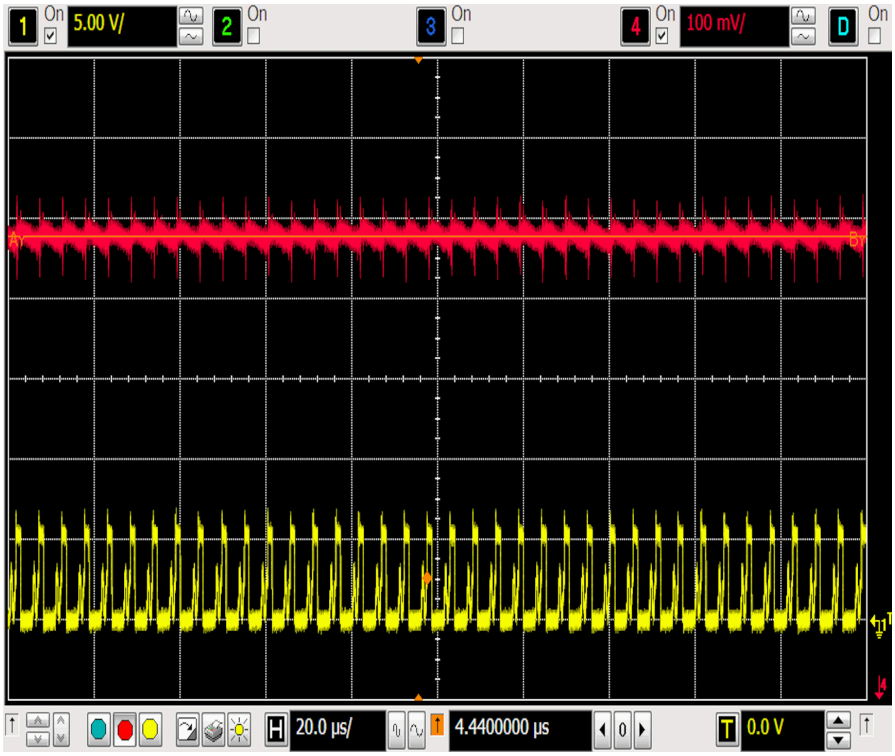


**Fig 4.15 Output voltage and Vsw at Pout=144mW**

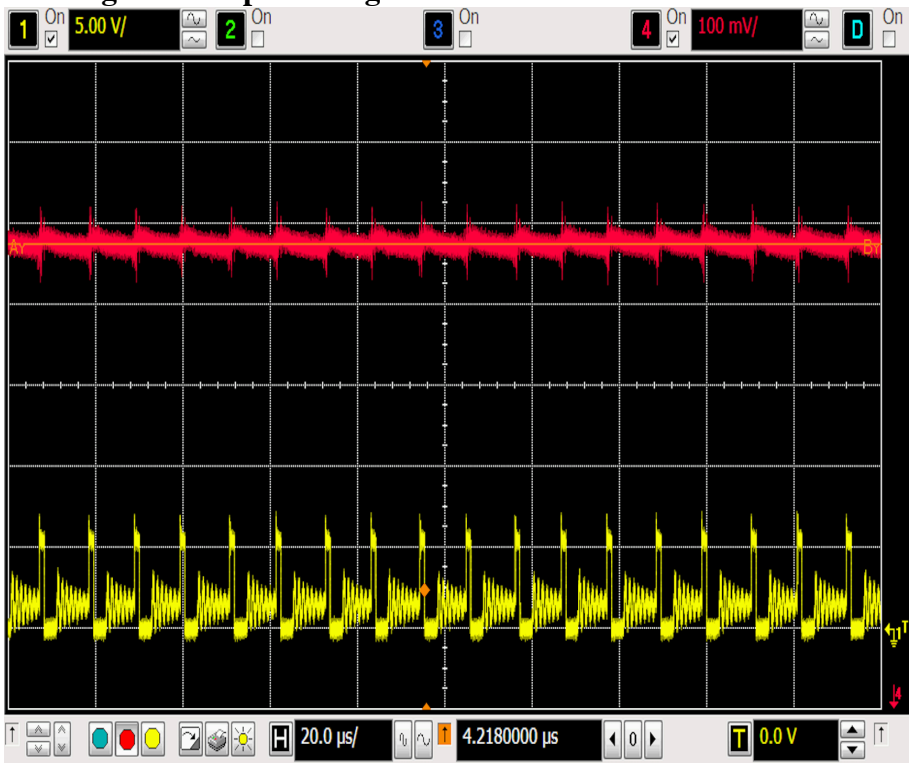


**Fig 4.16 Output voltage and Vsw at Pout=72mW**

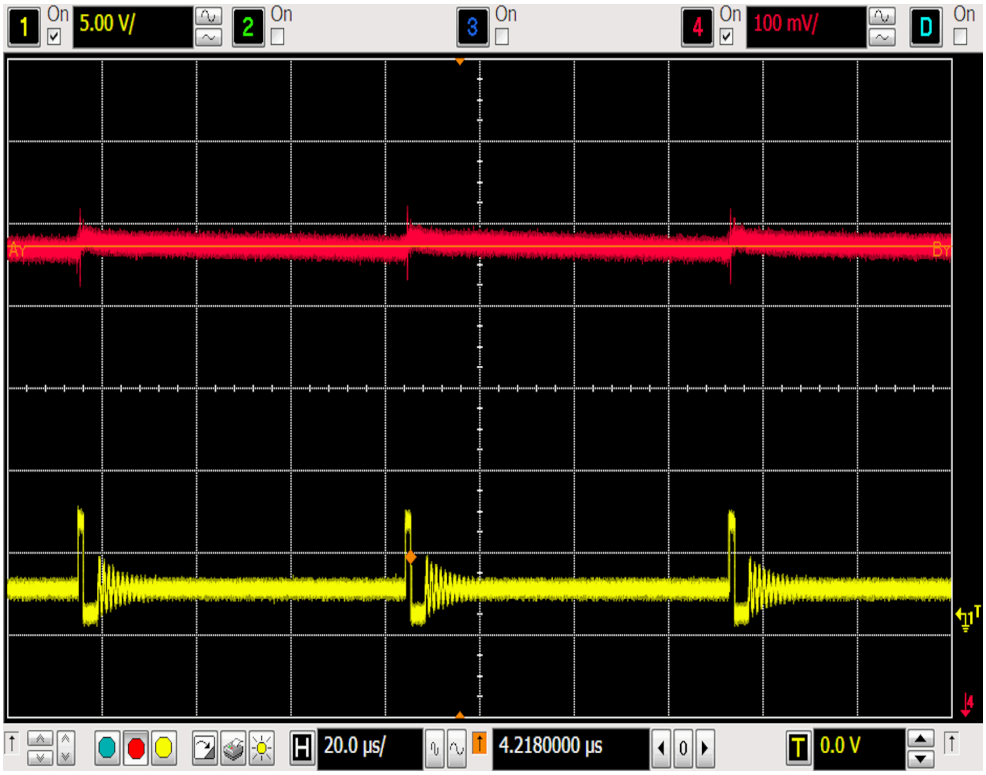


**Fig 4.17 Output voltage and Vsw at Pout=12mW**

Table 4 summarized the detail of the waveform above:

**Table 4: $V_{out}$ and $f_{sw}$ for baby-buck mode in different load condition**

| | $V_{out}$ | $f_{sw}$ |
|---|---|---|
| **$P_{out}$=144mW** | 1.204V | 189kHz |
| **$P_{out}$=72mW** | 1.201V | 95.4kHz |
| **$P_{out}$=12mW** | 1.200V | 14.6kHz |

As we can found from the summarization above, as the load power decrease, the switching frequency also reduce, hence the switching frequency is reduced.

Figure 4.18 also shows the largest voltage ripple at lightest load, which also fit the 40mV peak to peak output voltage ripple.

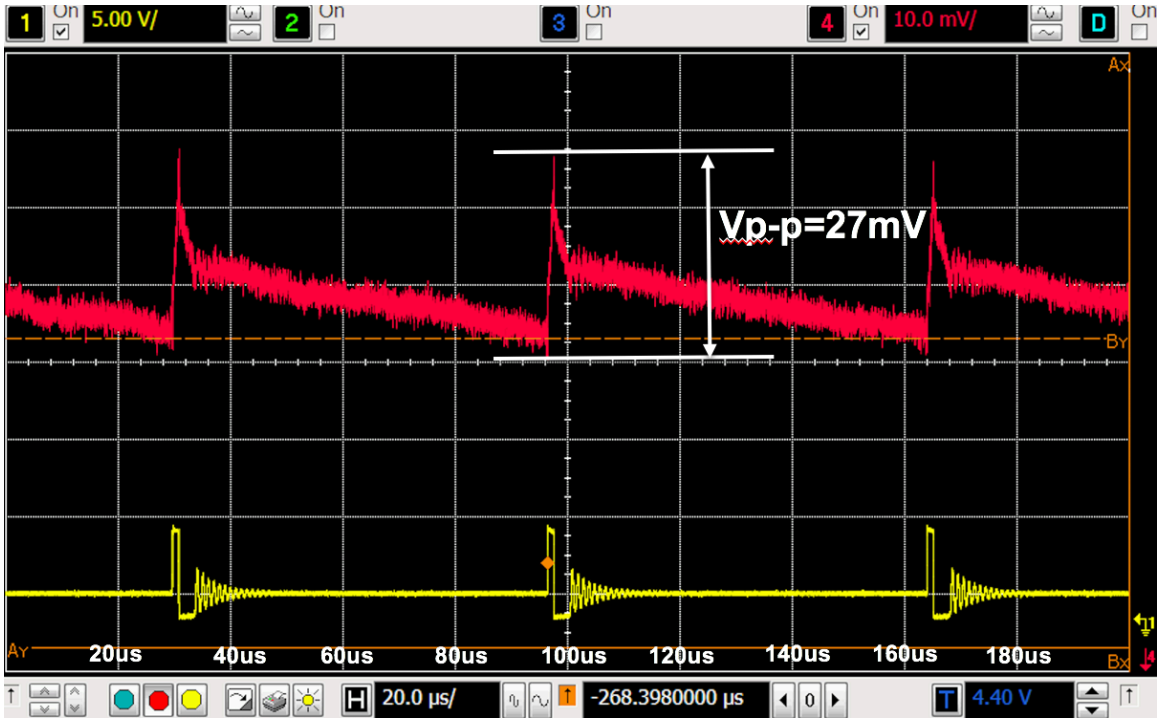


**Fig 4.18 Output voltage and Vsw at Pout=12mW**

Figure 4.19 shows the steady state waveform of heavy-buck mode, in which the converter only works in CCM mode.

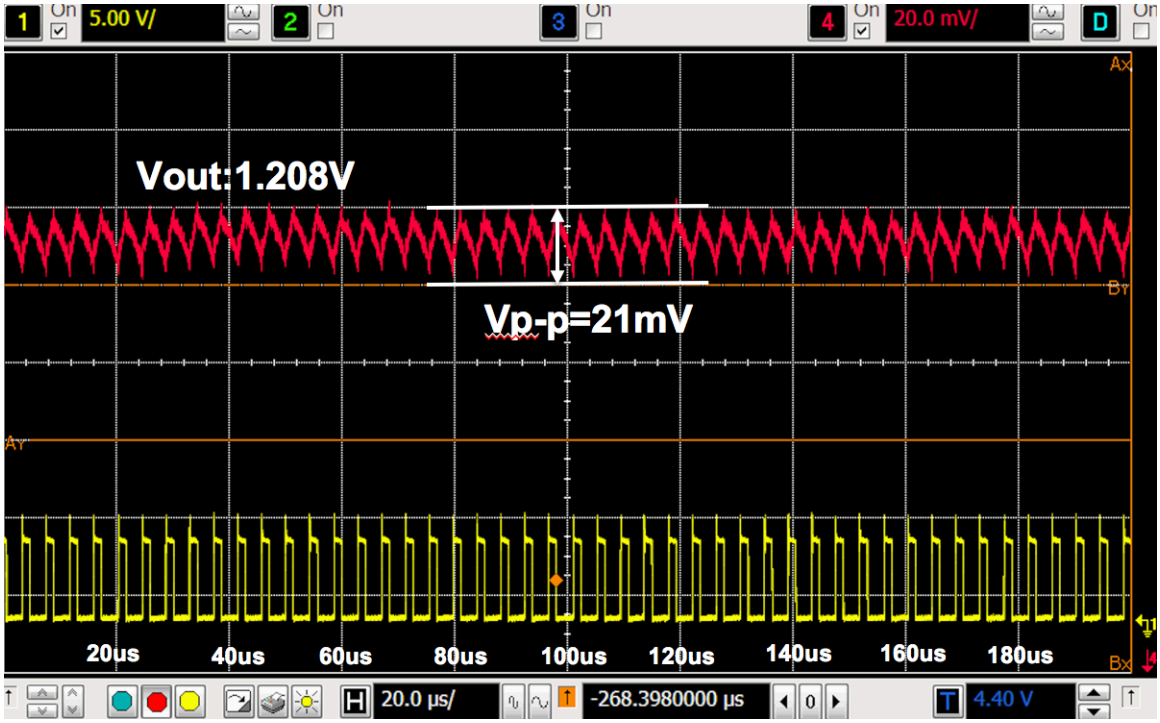


**Fig 4.19 Output voltage and Vsw for heavy-buck mode**

In the CCM mode, the converter works with the 231.2kHz switching frequency, which is close to the designed 250kHz switching frequency, also, the output 1.208V voltage is in the specification.

Figure 4.20 and Figure 4.21 shows the step-down and step-up transient response from 30mA to 260mA.

In the Figure 4.20, the red waveform represents the output voltage ripple, the blue waveform represents the DCM indicator, the yellow one represent the switching node voltage. The red and yellow one represent the same waveform in Figure 4.21, except the blue one represent the CCM indicator.

In the step-down transient response, we can find the converter is working in continuous conduction mode(CCM), after transition happen, it changes to discontinuous conduction mode(DCM). During the transition, the overshot voltage is about 18mV, which is about 1.5% of output voltage.

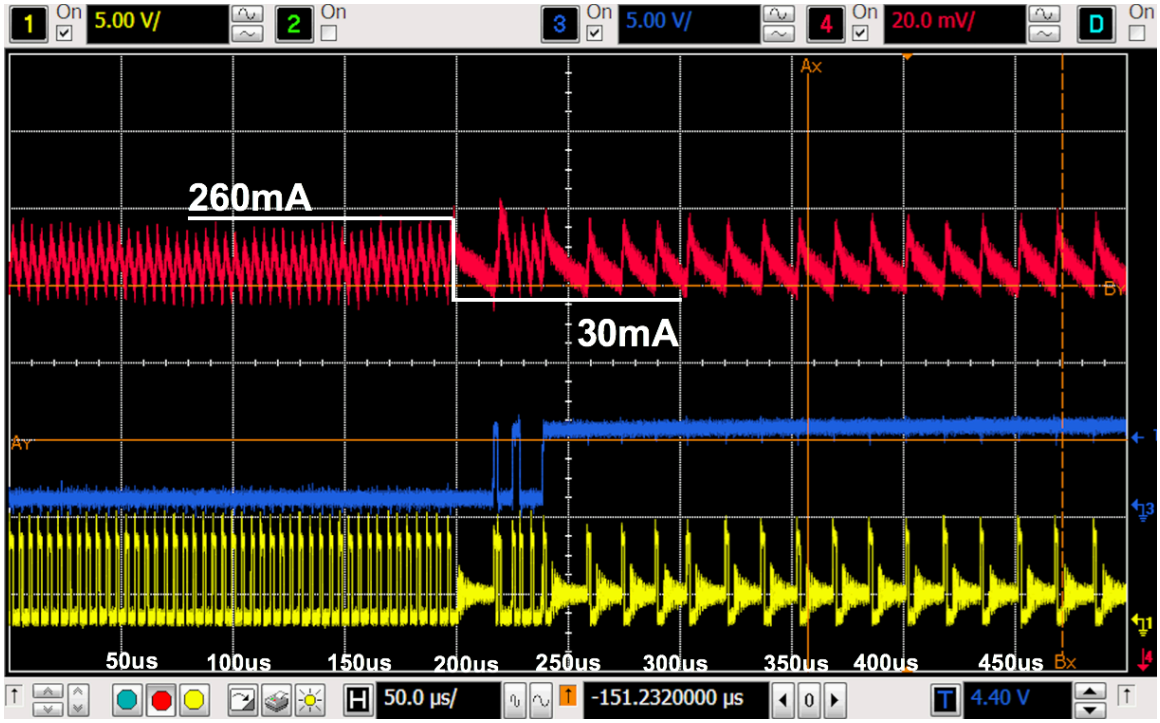


**Fig 4.20 Measurement of step-down transient response**

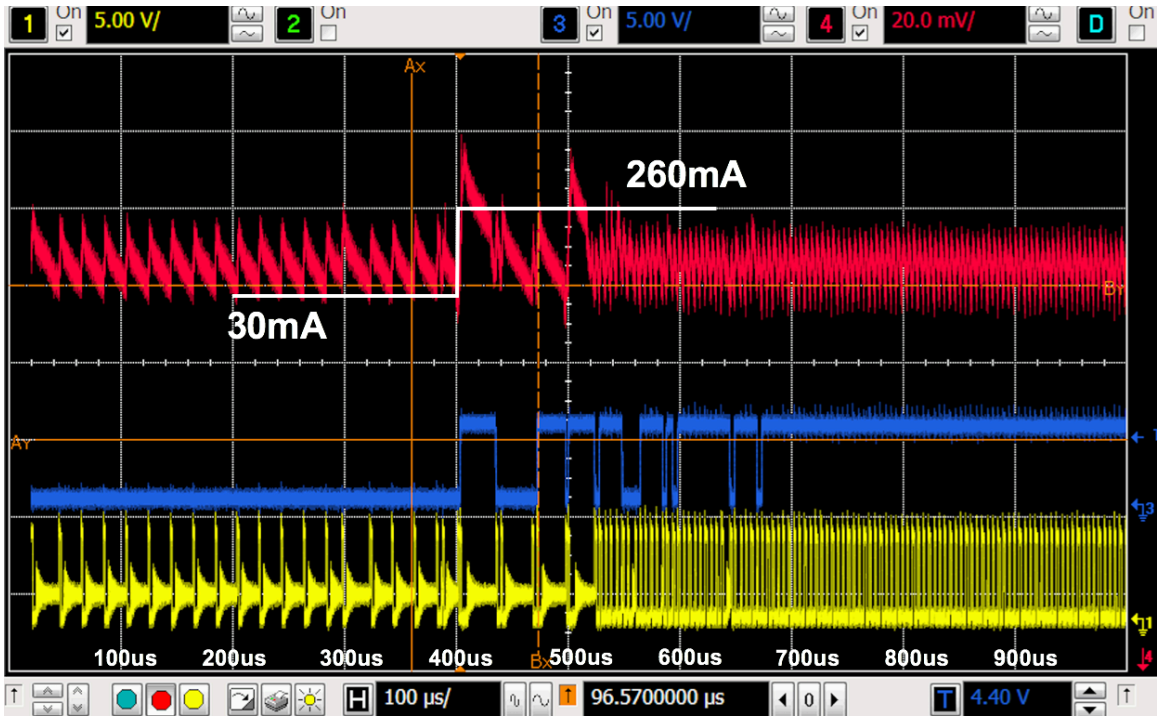


**Fig 4.21 Measurement of step-up transient response**

In the step-up transient response, we can find the converter is working in discontinuous conduction mode(DCM), after transition happen, it changes to continuous conduction mode(CCM). During the transition, the overshot voltage is about 35mV, which is about 3% of output voltage. Since the comparator in controller only have like 3mV hysteresis, the noise affect the output of CCM/DCM detector and converter switch between mode during the transition.

## 4.3.4 Efficiency Comparisons

Figure 4.14 shows the efficiency comparison between open loop and close loop converter operation.

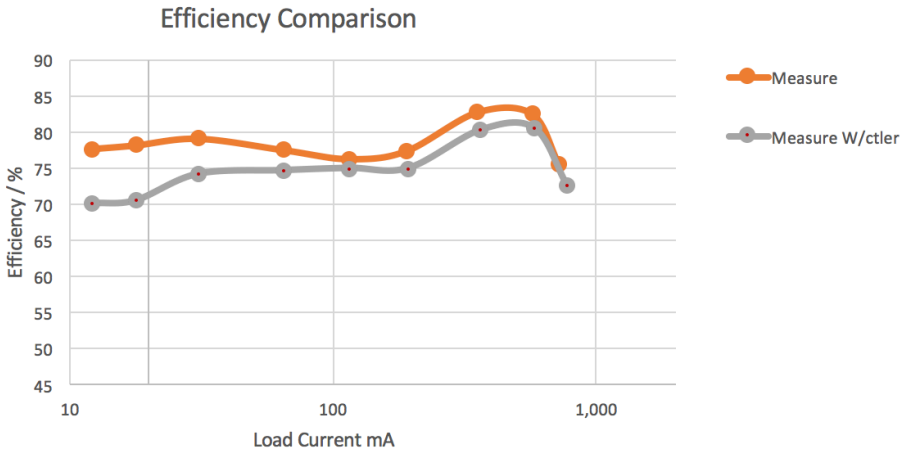


**Fig 4.22 Efficiency Measurement Comparison between Open Loop and Close Loop**

Since the controller loss was introduced into close loop operation, the efficiency drops about 7% percent at 10mA load. However, as the load current increase, the efficiency difference become smaller. The main difference in heavy load is introduce by the slew rate difference between waveform generator and on-chip mode selector and gate signal generator. The output

signals of waveform generator have quite straight rising and falling edge. However, in the on-chip controller, the effect introduced by pad's parasitic capacitors which discussed in 4.3.1 reduced the slew rate of digital signal. And extra delay was introduced into gate switching, hence about 2% difference exist in heavy load. By adding proper buffers before the signal connect to pad can help to reduce this effect, also connecting the signal line inside the chip can also help to reduce the parasitic effects.

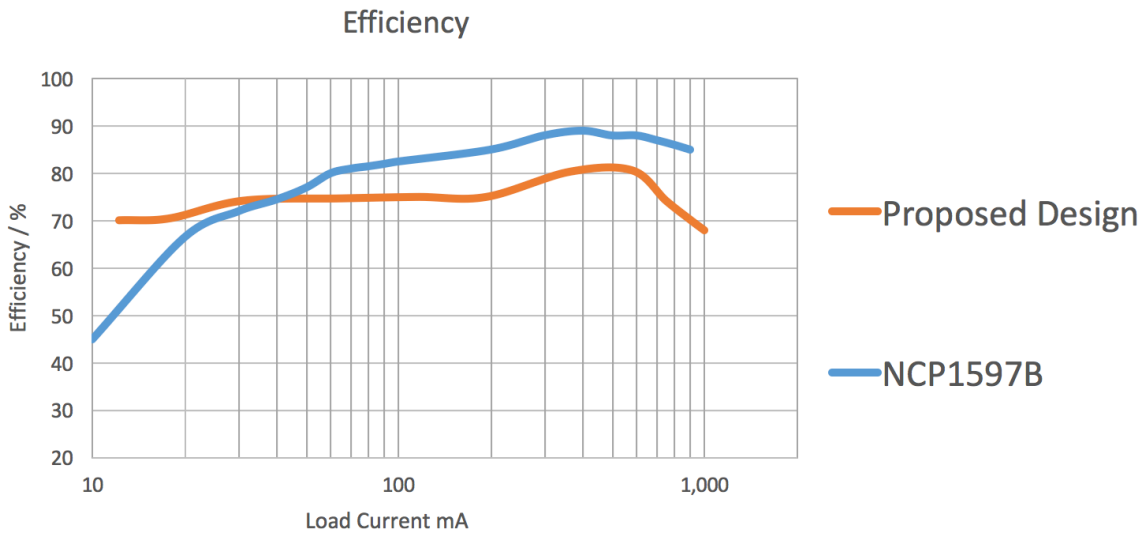


**Fig 4.23 Efficiency Comparison with NCP1597B**

Figure 4.23 shows the efficiency between proposed design and NCP1597B, we can find the proposed chip have higher light load efficiency compare to this commercial chip. Due to the reasons give above, the heavy load efficiency is lower than this commercial chip, which can improve in future research.

# 4.4 Future Improvement

This chapter presents the proposed integrated on-chip two modes monolithic synchronous buck converter. The simulation results in cadence shows the performance and stability of the proposed converter. And it

demonstrates the good performance in steady, transient and high efficiency. However, there still exist some drawback in this tape out, and further improvement can be made in continue research and tape out. Base on Zhao's suggestion, the redesign of power MOSFET have improved the sudden efficiency drop at mode transition point. Also, the Schottky diode in Zhao's design have been replaced by an on-chip synchronous MOSFET, and the light load efficiency in tape out chip increase greatly. However, four MOSFET for one power stage consume large chip area in layout. The area can be utilized more efficiently by changing the power MOSFET sizable. These four MOSFET can change to two large MOSFET, which is consist of several small MOSFETs and each MOSFET owns its own gate driver. Then the mode selector can turn on different number of power MOSFETs based on the load condition. The small power MOSFET and its gate driver can be layout more compactly to save chip area.

In section 4.3.1, the low slew rate problem of digital part can also be improved in future tape out. A simple way to solve this problem is to add some buffer before the signal path connects to on-chip pads, then sufficient current can handle the large parasitic capacitor of pads. However, this method would make the layout more complex, also, the buffer would consume extra powers. Another way to solve this problem is to connect all the signal path inside the chip then parasitic can reduce greatly. Also, in section 4.3.3, the problem that gate driver doesn't have enough line width can be solved through more careful layout. The wires that flow large current should be highlight in simulation to remind in layout.

## 4.5 Chapter Summary

This chapter give the simulation result of proposed two modes synchronous buck converter, the steady state waveform, transient waveform was present in above chapter. The simulation waveform shows the high performance of this design. Also, the measurement result of tape out chip was present, which include the measured waveform of controller components, open loop efficiency, close loop efficiency. The performance improved a lot when compare to last tape out, but drawback and defect still exist. At last, several ways to improve the circuit was provided.

# Chapter 5

## Summary and Future Work

The power consumption of smart cameras application varies significantly between sleep mode and active mode, and smart cameras stay in sleep mode for majority of time. The input voltage of the converter is 5 V, and the output voltage is 1.2 V with the load ranging from 10 mA to 1200 mA. Hence the research work is focus on the light load efficiency improvement of buck converter and the thesis research investigated a power converter to supply sufficient energy for the microprocessor of the smart camera at heavy load while have high efficiency at sleep mode. This research is to prolong the battery life of smart cameras through increasing the light load efficiency.

To improve the light load efficiency of conventional buck converter, the proposed design applied Wei's baby buck concept to provide another light load power stage to reduce the switching loss and driving loss at light load. Then, the variable frequency ripple-based constant on-time control with discontinuous conduction mode (DCM) in light load is applied to the baby-buck mode to reduce the switching frequency at light load, hence further reduce the switching loss. Also, the baby-buck mode uses the synchronous buck topology to remove the diode in asynchronous converter to increase the efficiency at light load. Finally, a sensorless mode selector remove the sensing resistor in power stage to increase the efficiency for entire load range, especially for the heavy load. The mode selector can select the optimum mode for different load condition, and the opposite mode would completely shut down to save the loss.

The proposed design is implement in CMOS 0.25um technology. The proposed monolithic buck converter which include the power stage of heavy buck mode, baby-buck mode and the controller is fabricated. The measurement result shows the efficiency varies from 70%-83% toward the entire load range.

This research can properly improve properly, the existing problem and suggestion is give below:

Since four MOSFET for one power stage consume large chip area in layout. The area can be utilized more efficiently by changing the power MOSFET sizable. These four MOSFET can change to two large MOSFET, which is consist of several small MOSFETs and each MOSFET owns its own gate driver. Then the mode selector can turn on different number of power

MOSFETs based on the load condition. The small power MOSFET and its gate driver can be layout more compactly to save chip area.

Also, during the layout procedure, the gate driver can be design more carefully with sufficient line width inside the chip to handle sufficient gate current for faster turn on speed and further increase the efficiency.

# References


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