3D Micromachined Passive Components and Active Circuit Integration for Millimeter-wave Radar Applications

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(ABSTRACT)

The development of millimeter-wave (30-300 GHz) sensors and communications systems has a long history of interest, spanning back almost six decades. In particular, mm-wave radars have applications as automotive radars, in remote atmospheric sensing applications, as landing radars for air and spacecraft, and for high precision imaging applications. Mm-wave radar systems have high angular accuracy and range resolution, and, while susceptible to atmospheric attenuation, are less susceptible to optically opaque conditions, such as smoke or dust. This dissertation document will present the initial steps towards a new approach to the creation of a mm-wave radar system at 94 GHz.

Specifically, this dissertation presents the design, fabrication and testing of various components of a highly integrated mm-wave a 94 Ghz monopulse radar transmitter/receiver. Several architectural approaches are considered, including passive and active implementations of RF monopulse comparator networks. These architectures are enabled by a high-performance three-dimensional rectangular coaxial microwave transmission line technology known as PolyStrata^{TM}as well as silicon-based IC technologies. A number of specific components are examined in detail, including: a 2x2 PolyStrata antenna array, a passive monopulse comparator network, a 94 GHz SiGe two-port active comparator MMIC, a 24 GHz RF-CMOS 4-port active monopulse comparator IC, and a series of V- and W-band corporate combining structures for use in transmitter power combining applications.

The 94 GHz cavity-backed antennas based on a rectangular coaxial feeding network have been designed, fabricated, and tested. 13 dB gain for a 2 x 2 array, as well as antenna patterns are reported. In an effort to facilitate high-accuracy measurement of the antenna array, an E-probe transition to waveguide and PolyStrata diode detectors were also designed and fabricated. A W-band rectangular coaxial passive monopulse comparator with integrated

antenna array and diode detectors have also been presented. Measured monopulse nulls of 31.4 dB in the ΔAZ plane have been demonstrated.

94-GHz SiGe active monopulse comparator IC and 24 GHz RF-CMOS active monopulse comparator RFIC designs are presented, including detailed simulations of monopulse nulls and performance over frequency. Simulations of the W-band SiGe active monopulse comparator IC indicate potential for wideband operation, with 30 dB monopulse nulls from 75-105 GHz. For the 24-GHz active monopulse comparator IC, simulated monopulse nulls of 71 dB and 68 dB were reported for the azimuthal and elevational sweeps. Measurements of these ICs were unsuccessful due to layout errors and incomplete accounting for parasitics.

Simulated results from a series of rectangular coaxial power corporate power combining structures have been presented, and their relative merits discussed. These designs include 2-1 and 4-1 reactive, Wilkinson, and Gysel combiners at V- and W-band. Measured back-to-back results from Gysel combiners at 60 GHz included insertion loss of 0.13 dB per division for a 2-1 combination, and an insertion loss of 0.3 dB and 0.14 dB for "planar" and "direct" 4-1 combinations, respectively. At 94 GHz, a measured insertion loss of 0.1 dB per division has been presented for a 2-1 Gysel combination, using a back-to-back structure. Preliminary designs for a solid-state power amplifier (SSPA) structure has also been presented. Finally, two conceptual monopulse transceivers will be presented, as a vehicle for integrating the various components demonstrated in this dissertation.

To Kimberly

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I would like to thank the numerous people I have worked with in the process of completing this work, in the lab and beyond.

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Chapter 1

Introduction

This chapter provides an introduction to the basic concepts of millimeter-wave radar and monopulse radar, as well as an overview of motivations for developing millimeter-wave monopulse systems and previous work in the field. A review of rectangular coaxial technology, specifically micromachined structures created using the Polystrata® process technology, is included. Finally, a proposed architecture for a compact millimeter-wave monopulse receiver system is presented and the structure of this dissertation document completes this chapter.

1.1 Millimeter-wave systems

There has been significant interest in using millimeter-wave frequencies (30-300GHz) for the past several decades [1]. Millimeter-wave systems have greatly reduced size and weight over microwave and other RF systems due to the reduced wavelength of the operating frequency. Reduced wavelength also results in an increased gain and narrower beamwidth for a given aperture size, as antenna gain scales with the operating frequency squared. Narrow beam widths translate to reduced ground clutter for radar systems, which makes these systems useful for low-angle detection tasks. Narrow beamwidths also reduce multipath, in which reflected signals from the target are re-reflected from the ground or other obstruction into

the antenna aperture, which can cause ghosting in radar systems. Another important result of a reduced beamwidth is an increased angular accuracy. This improved angular resolution is important in imaging systems, providing a smaller target pixel resolution.

Increased operating frequency also contributes to increased range resolution through increased bandwidth of operation, which translates to shorter pulses. Wide bandwidth is also of particular interest in high-data-rate point-to-point communications [2]. Additionally, as the microwave spectrum becomes more and more crowded, relatively open millimeter wave frequencies become increasingly attractive. A look at FCC frequency allocation [3] shows typical band allocations of 0.1-0.5 GHz in the 1-10 GHz range, 1-2 GHz in the 10-40 GHz range, and 5 GHz or more in the mm-wave regime. Another advantage of millimeter-wave frequencies is the low probability of transmission interception, given the limited range and the lack of ubiquitous receiving equipment.

However, millimeter wave systems are subject to increasing atmospheric attenuation relative to microwave and infrared frequencies as shown in Figure 1.1. However, certain bands, centered around 35 GHz, 94 GHz, 140 GHz and 220 GHz offer relatively lower levels of attenuation in the mm-wave regime, and have long been utilized for military sensing systems [5]. While millimeter waves are susceptible to attenuation due to precipitation in the same manner as infrared and optical frequencies, they are less susceptible to optically opaque conditions such as fog (Figure 1.1), dust, and smoke. This makes millimeter-wave systems ideal for low-visibility, high-resolution sensing applications.

One commercial application of millimeter-wave systems is automotive radar at 77 GHz [6][7][8], for collision avoidance, active cruise control [9] and parking assistance. A number of commercially available vehicles have such systems implemented. Chemical sensors using the frequency band from 225-315 GHz have also been proposed [10], as well as a myriad of applications in atmospheric remote sensing [11][12] ranging in frequency from 50-380 GHz. Many airports have recently begun to utilize millimeter-wave scanning systems for passenger security [13]. Millimeter-wave radar systems are also used in instrumentation radars such as

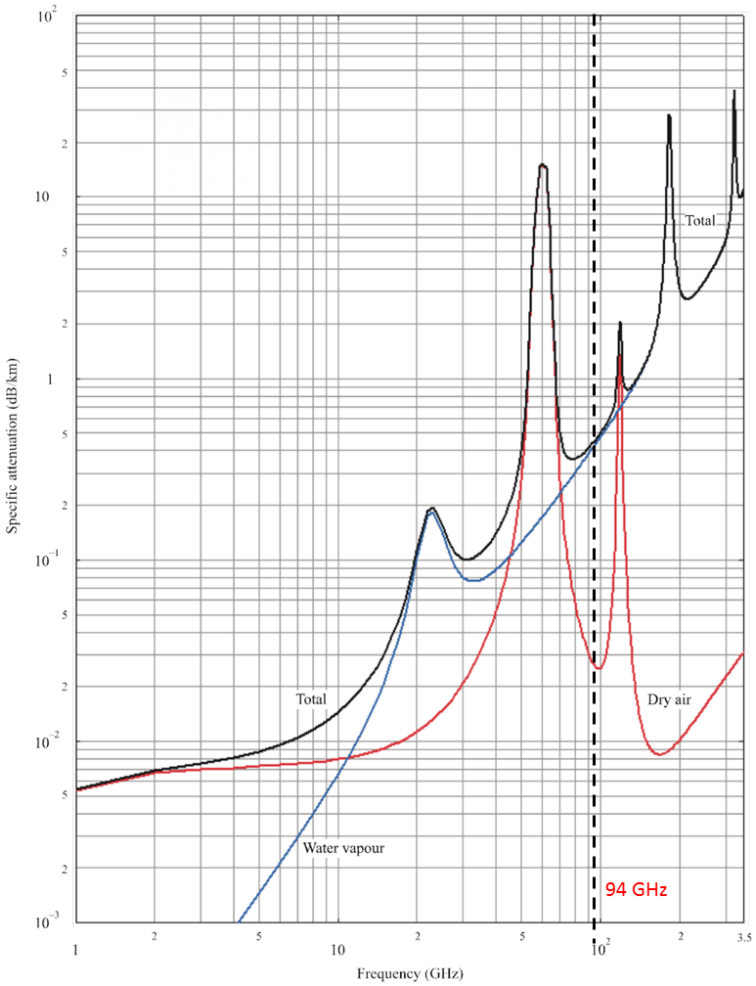


Figure 1.1. Atmospheric attenuation plot vs. frequency. Frequencies around 94 GHz occupy a window in relative attenuation, ∼0.35 dB/km. Plot data taken at 1013 hPa, 15° C, and water vapor density of 7.5 g/m^3 [4]

the one presented in [14]. Recent advances in semiconductor technology have enabled full millimeter-wave systems on a chip [15] up to 60 GHz. The frequency band about 60 GHz is currently in use for high-datarate wireless applications, and a number of compact, low-cost receivers have been developed [16] [17] [18] [19]. Perhaps the most relevant application to this dissertation is the Sandblaster radar developed by Sikorsky for DARPA [20]. This 94 GHz radar is designed to provide dust and smoke penetrating landing assistance with a significant savings in size and weight over comparable Ka-band radars.

Despite advances in MMIC and microwave technologies, the cost for millimeter wave systems still remains a significant consideration. Bulky TWTAs are required for high-power transmission capabilities, reducing the size and weight advantage for longer-range millimeter-wave systems. However, for short-range, high-resolution, high-bandwidth applications, millimeter-wave radar systems are very attractive.

1.2 Monopulse tracking radar

A tracking radar is one which automatically keeps the antenna beam axis aligned with a selected target [21]. Tracking radars are primarily implemented for military applications such as fire control, missile guidance, and aircraft tracking. However, tracking radars have a variety of applications beyond military uses, including communication systems, instrumentation, satellite tracking, and astronomical observation [22]. Tracking requires angular location information in at least one plane, as well as range information. In order to provide high-quality angular coordinates, a narrow beamwidth antenna is necessary. It follows, then, that a millimeter-wave system would be well suited to a short-range tracking radar application, given the narrower beamwidth for a given aperture and high angular resolution.

The earliest tracking radars utilized a single antenna beam, moved in a pattern, to arrive at angular position information for a target. Two such techniques are sequential lobing and conical scan [23]. Sequential lobing utilizes several antennas (or feeds), and switches between them. These antenna beams are designed to be slightly off-axis from the boresight of the system. The comparison of the received signal magnitudes would indicate the direction in which the antennas should be steered. If the comparison result equals zero, then the target is at boresight. Conical scan techniques operate with essentially the same concept, rotating an off-angle antenna or feed about the boresight, in essence replacing the multiple switched beams with one rotating beam. The target return for conical scan is modulated by the scanning frequency. The return signal must then be demodulated to receive information

about the target's angular location.

The drawbacks to these systems are clear: multiple pulses are required to estimate the target's location. This limits the system datarate, pulse repetition interval, and reduces tracking accuracy. Furthermore, variations in radar return signal from pulse to pulse may be erroneously interpreted as changes in target location. A technique which is designed to mitigate these problems is called *monopulse tracking*.

A monopulse tracking system generates the multiple overlapping antenna beams simultaneously, allowing the system to generate angular information from a single pulse (hence, the term monopulse). This eliminates the pulse to pulse target variation errors, providing higher-resolution angular data. Another advantage of monopulse systems is higher signal to noise ratio in the sum (range) channel, since the main beam is pointed directly at the target, vs. having offset beams to either side [21]. Monopulse systems are also less susceptible to switching or noise from the mechanical rotation of a scanned beam, and are more resistant to certain types of electronic counter measures (ECM). The major disadvantage of monopulse systems is increased cost and complexity, though the cost of such systems is decreasing.

While this discussion is primarily concerned with the tracking of a single target, it is worth noting that, in phased array radars, it is quite common for monopulse techniques to be applied to the tracking of many targets simultaneously. This approach is in use in systems such as Aegis and Patriot. Another application is in certain scanning radar systems which utilize monopulse techniques for tracking while scanning. Scanning radars, in contrast with tracking radars, do not use a feedback system to follow specific targets, instead providing a 360° image of surrounding targets. These techniques have a lower refresh rate, limited by the rotational speed of the antenna. Such systems, called automatic detection and track (ADT), are in use in civil air-traffic control as well as military systems [23]

The two major types of monopulse tracking are *amplitude-comparison* monopulse and *phase comparison* monopulse. An amplitude comparison monopulse system consists of overlapping antenna patterns with beams pointed in slightly different directions (beam squint,

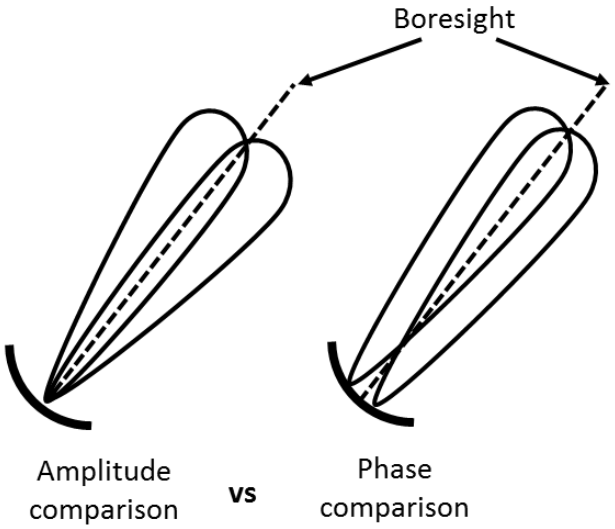


Figure 1.2. Antenna beam angle configuration for amplitude-comparison and phase-comparison monopulse techniques

or offset), as shown in Figure 1.2. In essence, this antenna beam configuration is the same as that of sequential lobing; however, instead of switched means, the antenna beams are monitored simultaneously. One common means of generating beams of this nature is using two feeds slightly displaced in opposite directions from the focus of a parabolic reflector [23]. The signals received in an amplitude monopulse system when the target is off of boresight will have the same phase, but different amplitudes. In contrast, phase-comparison monopulse antennas employ two beams which are identical, and parallel to each other, essentially operating as an interferometer. The resulting signals from each antenna are the same in amplitude, but different in phase. The phases are only equal when the target is located along the central axis of the two antenna beams. A typical phase-comparison monopulse system would employ an array of antennas.

However, these distinctions are not necessarily relevant in a modern monopulse system, as most modern systems utilize a *monopulse comparator*. A monopulse comparator synthesizes sum (Σ) and difference (Δ) values, utilizing *both* phase or amplitude information [22]. In phase- and amplitude-comparison monopulse systems, variance between beams introduces

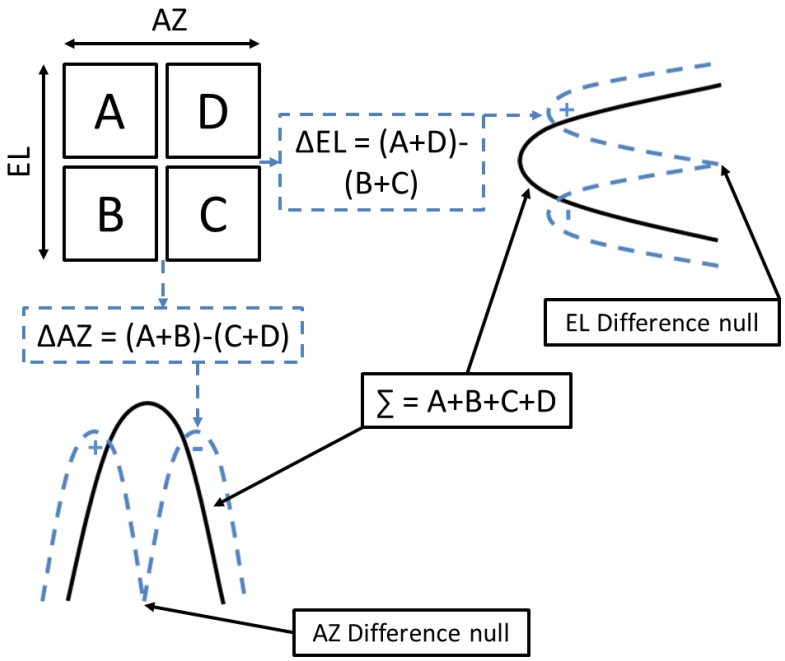


Figure 1.3. Monopulse comparator sum and difference patterns. A-D represent the received signals from an antenna or feed arrangement which allows for 3-D angular location. AZ is the azimuth plane, EL is the elevation plane. Odd phase symmetry about boresight is used to resolve ambiguity as to which side of null the target is located.

significant angle error. A monopulse comparator system mitigates this issue.

The Σ channel provides overall range data, typically by adding the received signals from all beams. The Δ channel provides angular locational data; a target on boresight will be in the *null* of the difference pattern. Due to the sharp slope of the difference null, small changes in angle away from boresight result in large error signal. The sign of the phase information is used to determine which side of the monopulse null the target is on. This is critical for feedback systems used for tracking. The tracking accuracy (ϕ_θ) of a monopulse system is directly related to the null depth and antenna 3-dB beamwidth ($\theta_{difference}$), as shown in Equation 1.1 [1] [24]. Often, the null-depth is limited by the signal-to-noise ratio (SNR) of the receiver system.

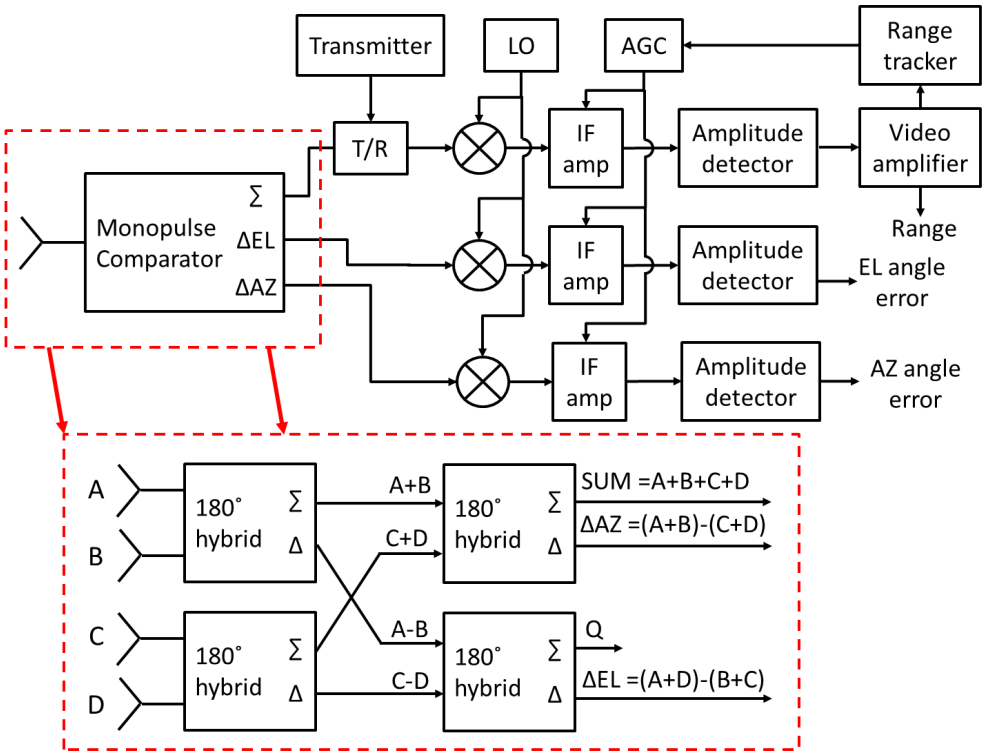


Figure 1.4. Generalized block diagram for a monopulse transceiver. Range tracker provides normalization of difference nulls to eliminate signal magnitude-related error. (inset) monopulse comparator architecture based on four 180° hybrid junctions. The "Q" output is typically terminated and remains unused or used for calibration purposes.

$$\phi_\theta = \frac{\theta_{difference}}{2\sqrt{nulldepth}} \tag{1.1}$$

To reduce errors due to changes in radar return strength, the Σ signal is used to normalize the Δ pattern. To receive three dimensional tracking information, a difference null is required in two planes (azimuth and elevation). Typically, this is achieved using four antennas, or an array divided into four quadrants. A diagram of the four antennas and the signal processing required to generate each pattern is shown in Fig. 1.3.

A common architecture for a monopulse radar transceiver is shown in Figure 1.4; the comparator network is shown in the inset. 180° hybrids typically perform the addition and subtraction operations at microwave frequencies. Both passive and active implementations of

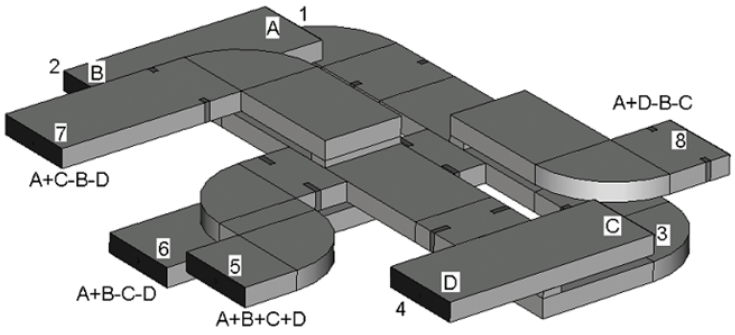
these circuits will be discussed in this dissertation. It is possible to perform the addition and subtraction of the signals utilizing quadrature hybrids, although additional 90° phase shifts in the signal paths are required. The additional phase shifts tend to limit the bandwidth of the comparator. The monopulse comparator network generates four signals, SUM (Σ), elevational angle (ΔEL), azimuthal angle (ΔAZ), and a "diagonal difference" channel (Q), which is typically terminated often remains unused. However, certain systems use the Q channel for calibration. Many implementations of the monopulse comparator network exist. The next section will discuss the state-of-the-art in millimeter-wave monopulse architectures.

1.3 Millimeter-wave Monopulse Architectures

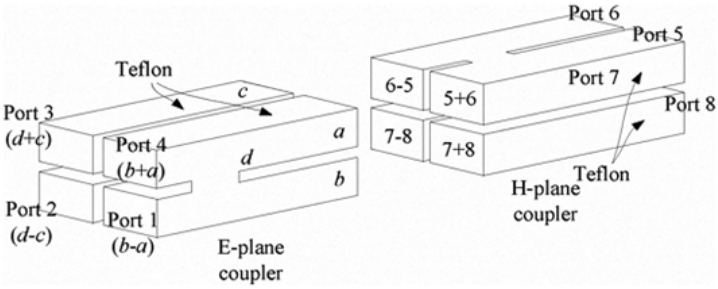
A variety of millimeter-wave monopulse comparators and receivers have been proposed and demonstrated. While waveguide implementations are high performance, they are often expensive and bulky. Sum and difference operations are often performed by magic-T or similar structures. A fairly compact implementation of a 15 GHz magic-T monopulse comparator is outlined in [25]. E- and H-plane couplers can also be used to generate the sum and difference patterns (Fig. 1.5) [26].

Planar implementations are a common approach to reducing the size and cost of monopulse transceivers at millimeter-wave. Planar circuitry at W-band is not without issues. A chief concern is the loss due to routing from the antenna to the comparator circuitry and within the comparator itself. Typically, planar transmission lines would result in 2-3 dB of insertion loss, which is a direct contributor to overall system noise figure. To overcome this limitation, a common approach is to down convert to IF, where comparator circuit losses are lower, and noise figure has been set by the preceding LNA.

Monopulse receivers developed at University of Michigan demonstrate this IF monopulse technique. In a system [27] with four integrated horn cavities as antennas was demonstrated. The integrated horn cavity is a 70° flared bulk micromachined silicon cavity with dual dipole



(a)



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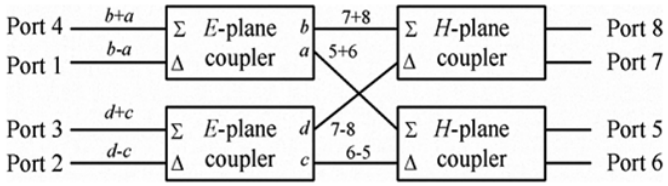
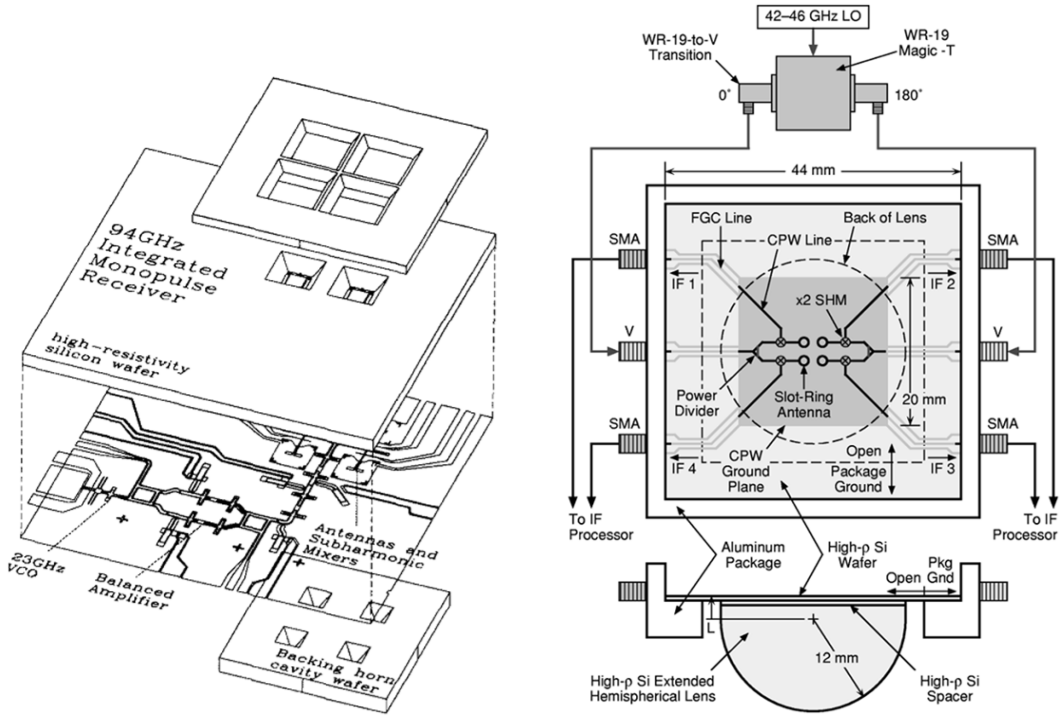


(c)

Figure 1.5. (a) 15 GHz waveguide magic-T comparator. System dimensions are 45.3mm x 89.8mm x 100mm (407 cc) [25] © 2006 IEEE. (b) a W-band waveguide monopulse comparator based on Teflon-loaded E- and H-plane waveguide couplers [26] © 2010 IEEE. (c) circuit diagram for W-band waveguide monopulse comparator based on Teflon-loaded E- and H-plane waveguide couplers [26] © 2010 IEEE.

antennas and the mixing circuitry directly integrated. The comparator operations were performed at IF on *co-planar waveguide* (CPW) with hybridly integrated active components on silicon. A difference null of 35 dB was reported for a 20 MHz bandwidth. Another University of Michigan monopulse receiver was based around the use of a dielectric lens fed with a 2 x 2 array of slot-ring antennas [22] [28]. This approach inserted GaAs Schottky



(a) (b)

Figure 1.6. (a) W-band integrated horn monopulse receiver. The horn cavities are etched in Si. Received signals are directly converted to IF at the antenna, and comparator functions performed at IF [27] © 1994 IEEE. (b) a W-band dielectric lens-based monopulse radar receiver. Received signals are downconverted to an IF of 2-4 GHz [28] © 1998 IEEE.

diode mixers immediately following the antenna elements, and mixed the incoming signal to a frequency between 2-4 GHz via a x2 subharmonic mixer with an LO of 42-46 GHz. The deepest nulls occurred around an IF of 3 GHz. A difference null of 45 dB over 200 MHz and 25 dB over 600 MHz for ΔEL were reported.

The IF comparator technique is also utilized in a transceiver demonstrated by the Beijing Institute of Technology [29]. This approach uses microstrip antennas and a spatial combiner for transmit power, which has a reported 90% efficiency. To balance signal phase, routing to and from the antennas was loaded with dielectric. This implementation has a 30 dB difference null, and 29.5 dB of gain in the SUM pattern.

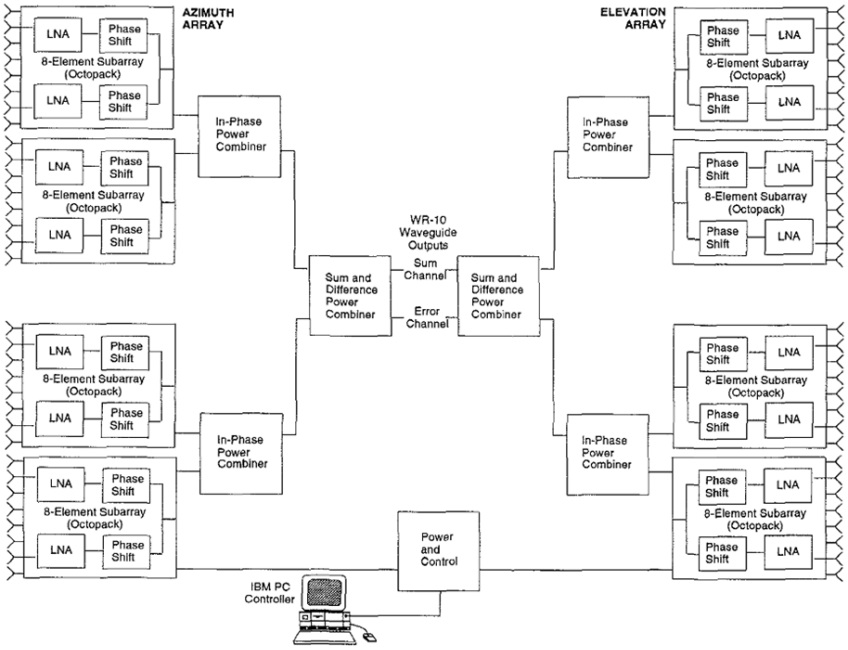


Figure 1.7. Block diagram of 94 GHz "octopack" monopulse receiver [31]. The "octopacks"' were constructed on multilayer substrates © 1996 IEEE.

A more recent iteration of this design approach performs IF monopulse synthesis in the digital domain [30]. High speed ADCs convert the IF signals to digital. In addition to receiving channels, the digital logic also produces four calibration channels, which facilitate easier channel calibration. The system is reasonably stable over a 500 MHz bandwidth. While the published system was designed for Ku band, this could be a viable option for millimeter-wave frequencies.

Another transceiver was developed in [31] by Lockheed Martin/Sanders. The monopulse front-end operates at 94 GHz. This particular module has 64 dipole antenna elements arranged into a cross-shape in two independent lines. Sub-arrays of 8 elements are combined using an "octopack" which is a package containing a dedicated variable amplitude GaAs MMIC LNA and phase shifter for each element. The "octopacks" utilized multilayer substrates for DC and RF routing within the module. 2.3° beamwidths were reported. The monopulse comparator operations were performed in a waveguide comparator, and a 20 dB difference null was demonstrated.

Another transceiver of interest is the monopulse front-end outlined in [32] by Northrop Grumman. The antennas are circularly polarized microstrip patches, placed at the focal point of a small parabolic dish. The comparator is implemented in microstrip on a quartz substrate. A monopulse null depth of 25 dB is reported. While this approach is interesting, high-quality quartz substrates are expensive, and rather delicate.

Though not a monopulse radar system, the system described in [33] is particularly relevant to the topic of this dissertation. A Ka-band *low-temperature co-fired ceramic* (LTCC) based system demonstrates the use of advanced fabrication techniques to design high-performance mm-wave systems. LTCC is a technique for creating multilayer microwave circuits, in essence, it can be used as a multilayer RF PCB. The design in [33] takes advantage of the dense circuit routing capabilities, packing 25 monolithic circuits and 4 microstrip isolators in an area of 12 square centimeters.

An alternative to the LTCC implementation is represented in [34]. This 60 GHz transceiver, developed at Georgia Tech, utilizes *liquid-crystal polymer* (LCP) antennas and hybrid assembly techniques with a custom MMIC. The MMIC contains a full transceiver, including power amplifiers, SPDT T/R switch and LNAs. In the next section, an additional advanced fabrication technique, the PolyStrata process will be examined. Its use as a platform for designing a mm-wave monopulse radar transceiver represents an evolution of the systems described in this section.

1.4 Overview of PolyStrata Technology

The PolyStrata® process is a sequential micromachining technique used to create unique air-dielectric microwave components and systems [35]. The process used to create these structures is a sequential deposition of copper and photoresist on a carrier substrate (either silicon or ceramic). A graphical representation of the process is shown in Figure 1.8. Proprietary photoresist ranging in thickness from 25-100 μm is patterned on a carrier substrate.

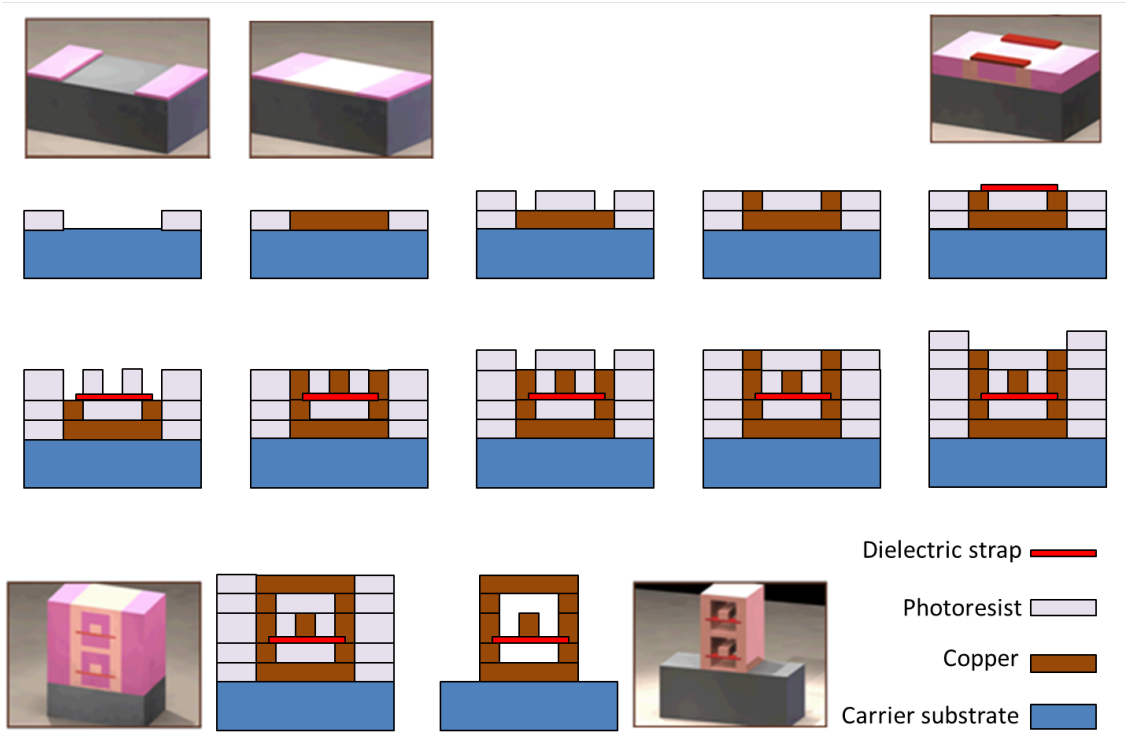


Figure 1.8. Graphical representation of PolyStrata process used to create an air dielectric rectangular coaxial structure. Thick photoresist is patterned. Copper is electroplated and planarized. Dielectric straps are inserted periodically. The final step represents the removal of the photoresist ("release").

Feature sizes are limited by photoresist aspect ratios, 1:1.1 for gap and feature widths. Copper is electroplated in the photoresist openings, and the entire wafer is planarized, chemically and mechanically.

This process is repeated multiple times, in order to realize multilayer structures. To date, as many as fifteen layers have been fabricated, though more are possible. To complete the process, the unwanted photoresist is removed chemically ("released"). Enclosed features require a sufficient number of holes in the enclosing structure for dissolved resist to flow during release. These are referred to as "release holes" and are typically 150-250 μm in width and depth. A rendering of a Polystrata structure with release holes are shown in Fig. 1.9. Since the PolyStrata process is a batch process, component costs can be low. In addition to copper features, dielectric support structures are also patterned. These range

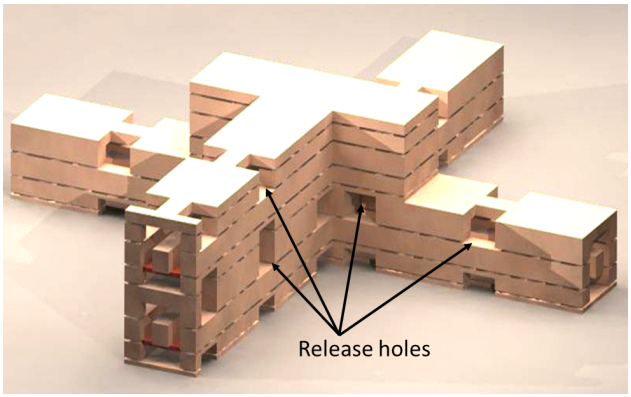


Figure 1.9. Rendering of PolyStrata structure demonstrating release holes. Holes are electrically small and do not radiate to 120 GHz. Additionally, this structure features adjacent lines sharing a wall. This is possible due to the high isolation of the rectangular coax structure.

in length from 300 to 1000 μm, and are typically 100 μm wide and 20 μm thick. These support straps are often used to support the center conductor of rectangular coax, although they may have additional uses. While the straps have an associated dielectric constant, their contribution to the overall effective dielectric constant is less than 0.5%. This is due to the sparse volume they occupy in a typical PolyStrata rectangular coaxial cross-section relative to the volume occupied by air. Except in special cases, the straps are ignored for simulation purposes. After fabrication PolyStrata parts may remain on the Si or alumina substrate, or they may be detached from the substrate as individual components that can be mounted in other assemblies.

The air-dielectric rectangular coax forms the basis for most PolyStrata structures and systems. Electromagnetic models of rectangular coaxial structures have been studied for many decades [36][37][38]. Extensive numerical modeling of PolyStrata rectangular coax lines is presented in [39] and [40]. The work in [40] represents a comprehensive study of manufacturing effects on PolyStrata device performance in regards to bandwidth, impedance, attenuation, and power handling. A study of copper surface roughness effects on performance is presented in [41]. The available impedances in PolyStrata rectangular coaxial line range from 13.6 to 130 Ω. A plot of impedance vs. coax dimensions is shown in Fig. 1.10. Rectangular coaxial transmission lines have a number of advantages over traditional microwave

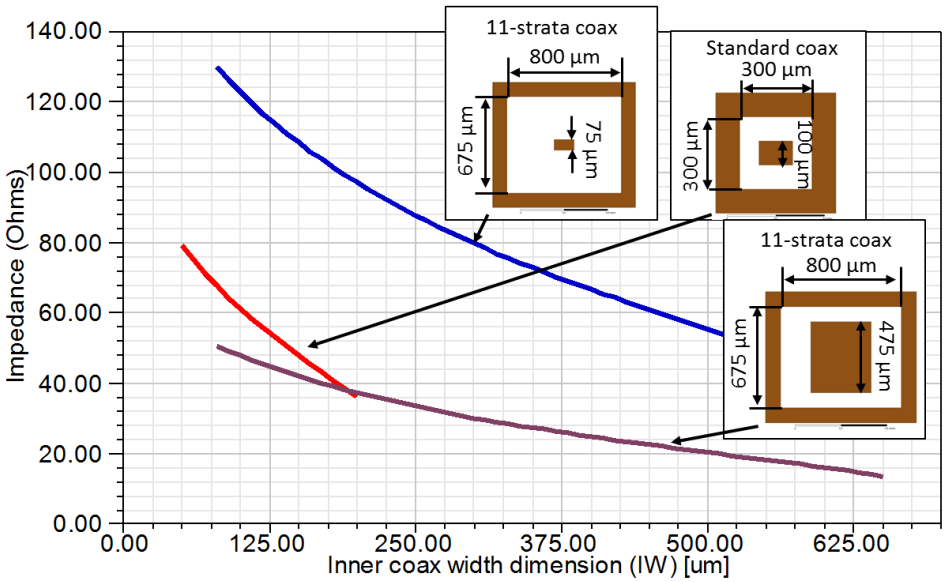


Figure 1.10. Plot of inner conductor dimensions vs. line impedance. Standard 6-strata rectangular coax ranges from 80 to 37 Ω. 11-strata coax with various center conductor thicknesses can extend the available impedances from 13.6 to 130 Ω

transmission line technologies:

- Simulated dominant TEM mode operation to 450 GHz for coaxial lines with 250 x 250 μm outer cross-section. This allows for very broadband components to be realized in PolyStrata [40]. The phase velocity, group velocity, and impedance of rectangular coaxial lines are not functions of frequency.

- Loss as low as 0.1 dB/cm at Ka band [42]. Insertion loss at 110 GHz has been measured to be less than 0.4 dB/cm. The use of an air dielectric eliminates dielectric loss tangent as a loss mechanism. Additionally, the high conductivity of copper reduces the resistive loss of coaxial lines.

- Isolation measured as low as 60 dB for two coaxial lines sharing a common ground wall [43] [44], despite the periodic breaks in the outer conductor for release holes. A simulation of a crossover structure which illustrates the high isolation of rectangular coaxial lines is shown in Fig. 1.11. The simulated line to line isolation is in excess of 100 dB, though measured results, limited by the measurement system noise floor, have

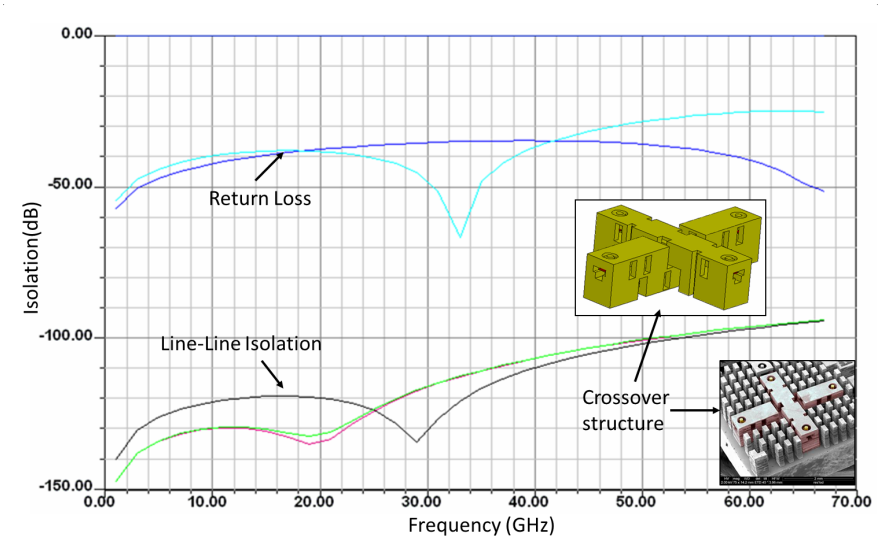


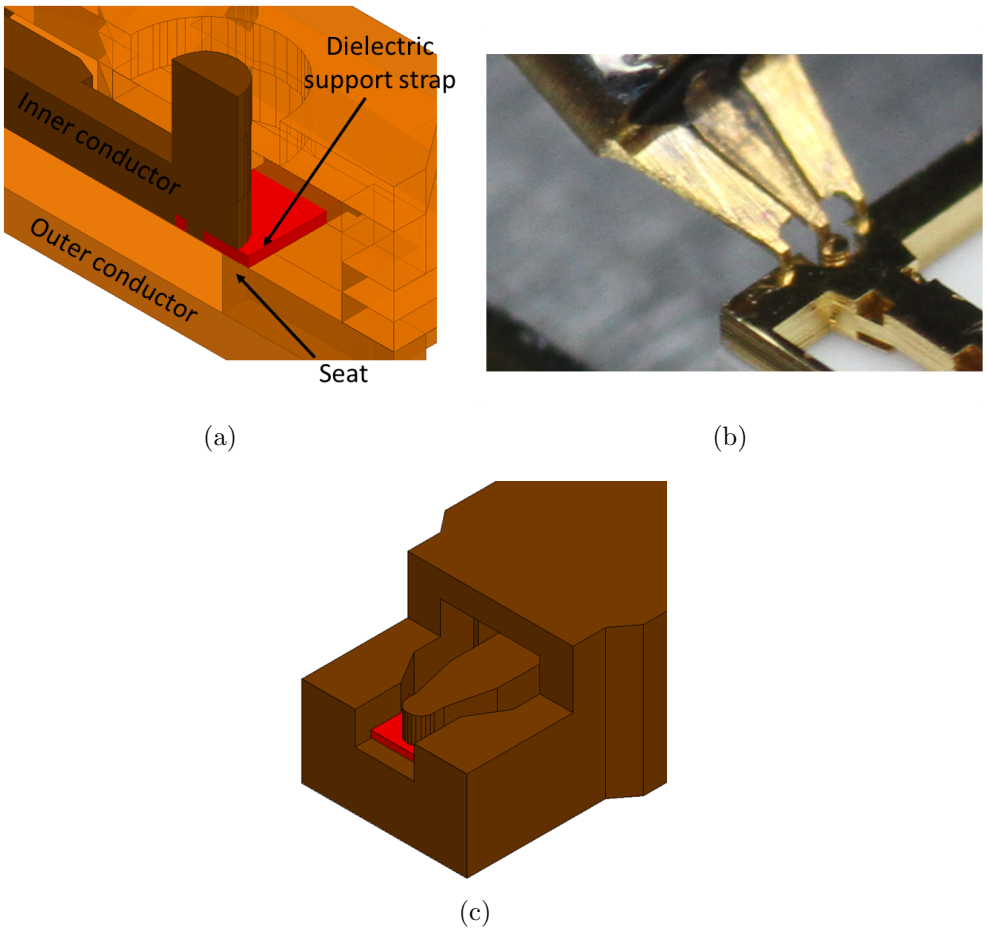
Figure 1.11. Simulation of PolyStrata crossover structure. Simulated line-to-line isolation is greater than 100 dB, but measured line-to-line isolation has been 60 dB, limited by the noise floor of the measurement system.

only demonstrated 60 dB isolation. This performance allows for much more densely packed transmission line elements than traditional microwave transmission lines. These transmission lines can be routed in three-dimensions without additional assembly. A meter of PolyStrata coax would occupy approximately 20mm x 12.5mm x 1mm, or 250 mm^2.

- Micron scale accuracy across centimeters of distance. Extremely high complexity monolithic systems can be fabricated in Polystrata, currently limited in size only by the six inch wafer tooling in the current fabrication facilities.

- Power handling capability: In [45], 53 Watts of pulsed power were passed through a 15mm long 7-strata rectacoaxial line at 2.5 GHz before arcing occurred. 11-strata coaxial lines with additional heat-sinking structures for the center conductors have further extended this capability. Transmission through a coaxial line of 200 watts at 2 GHz was demonstrated in [46].

Prototype PolyStrata components are tested in the same manner as ICs and CPW-

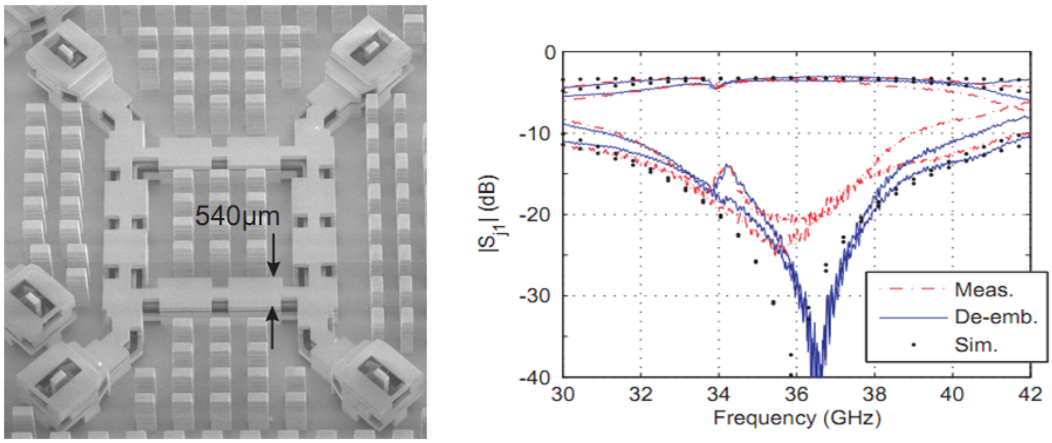


(a) (b)

(c)

Figure 1.12. (a) Cross-section of a typical PolyStrata "launch" (b) PolyStrata launch being probed with GGB GSG probe (c) a "W-band launch"

based microwave circuitry: using GSG probes. A methodology for designing "launches" which allow for this style of probing was initially outlined in [39]. These launches allow for repeatable and consistent measurements. Figure 1.12a shows a cross-section of a typical launch. This particular launch includes a "seat": a dielectrically isolated metal support which provides additional mechanical support when probing or wirebonding. This feature adds capacitance to the coaxial line and must be compensated. In order to compensate for 100 μm pitch probes, which are commonly used at W-band frequencies, launches of the type shown in Fig. 1.12c are used on many of the designs shown in this dissertation. The main distinguishing feature of these "W-band launches" is that, instead of bringing the center

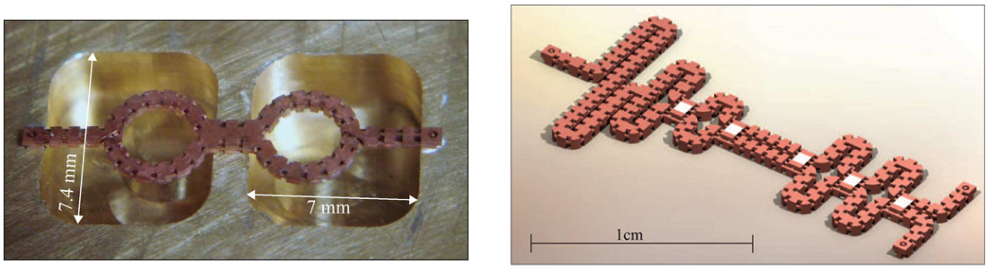


(a) (b)

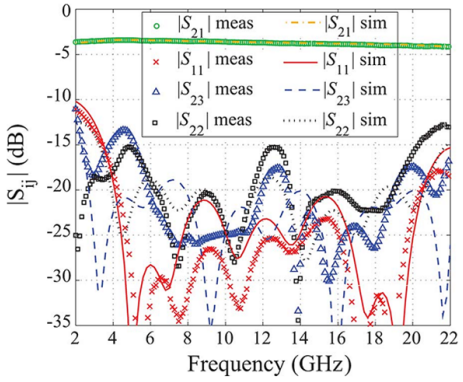
Figure 1.13. (a) An SEM image of a Polystrata Ka-band 90° hybrid (b) Simulated measured and de-embedded results for port 1 being excited of the branch-line coupler [47] © 2007 IEEE.

conductor up vertically to the top surface of the outer conductor, the outer conductor is removed to expose the center conductor. Often, the thinner strata of metal in a PolyStrata build are located at the center conductor, to allow greater control over impedance. In order to accomodate the gap spacing and conductor width necessary for 100 μm pitch probes, these thinner layers are required for the probe launch.

A number of components have been demonstrated in the PolyStrata process using rectangular coaxial transmission lines. A first generation Ka-band 90° hybrid was demonstrated in [47] (Fig. 1.13). Measured output amplitude of 3.2 dB $\pm$0.1 dB and output phase of 90° $\pm$ 2° over a band from 34.5-36.5 GHz were presented. Broadband 4:1 and 2.25:1 Impedance transformers are demonstrated in [48], a Ka-band Gysel combiner was demonstrated in [50], and broadband Wilkinson dividers were demonstrated in [49]. The Wilkinson divider provides a 2:1 division over 2-22 GHz, with an insertion loss of 0.71 dB at 12 GHz and return loss is less than 13 dB for the band. Figure 1.14 shows the impedance transformer and the Wilkinson divider, as well as the Wilkinson divider performance. In order to maintain the reported 11 dB isolation at the output ports, discrete resistors are integrated assembled into the Wilkinson divider, represented as white squares in Fig. 1.14b.



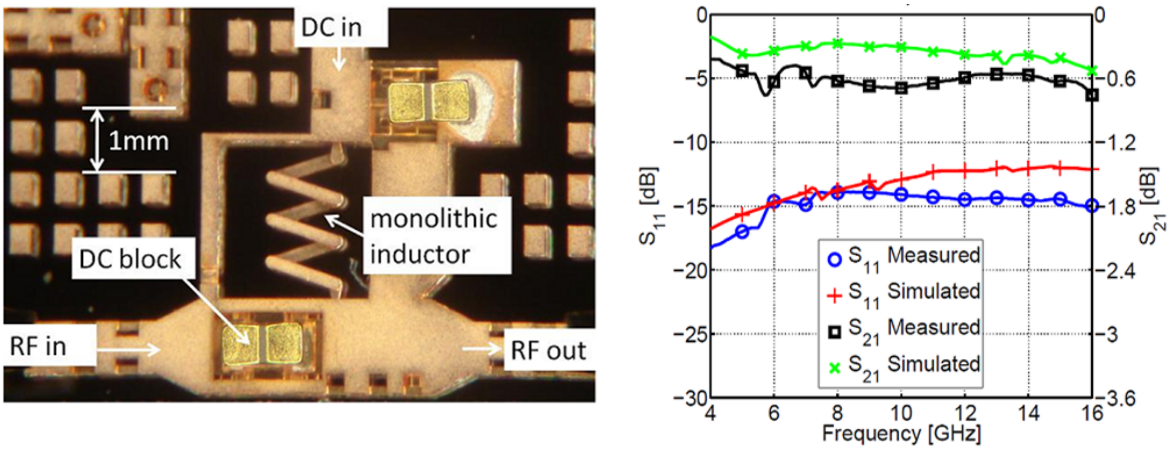
(a) (b)



(c)

Figure 1.14. (a) Photograph of fabricated broadband 4:1 impedance transformer mounted on brass carrier with conductive epoxy [48]. The cavities shown under the device are to prevent interference by with current flows on the outer conductor of the impedance transformer © 2010 IEEE. (b) 3-D model of broadband Wilkinson divider. White squares represent hybridly assembled isolation resistors. (c) Simulated and measured insertion loss, return loss, and isolation of broadband Wilkinson divider [49] © 2009 IEEE.

In general, Polystrata structures allow for the integration of any number of passive and active devices with PolyStrata components. Another demonstration of this integration is the bias tee pictured in Figure 1.15. Discrete 0402 capacitors are assembled into PolyStrata sockets. The inductor is monolithically fabricated in PolyStrata, providing a Q of approximately 20. The PolyStrata bias tee has a significant advantage in DC current handling and RF power handling capability when compared with commercially available bias tees [51]. Fig. 1.15 shows a fabricated 12-Ω bias tee, which was specifically matched to a PA MMIC. A 50-Ω version was also fabricated, and a comparison with other similar available bias tees is shown in Table 1.1.



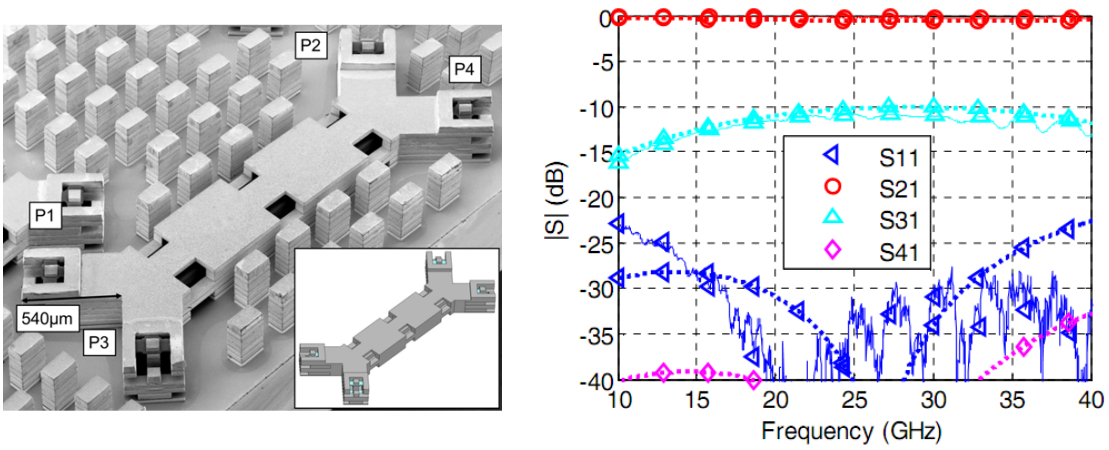
(a) (b)

Figure 1.15. (a) Photograph of fully assembled 12Ω PolyStrata bias tee including monolithic PolyStrata inductors. (b) Measured and simulated results for the 12Ω bias tee [**?**] © 2010 IEEE.

Table 1.1. Bias-tee comparison [**?**] © 2010 IEEE

	MEMS [52]	Picosecond 5545 [53]	PolyStrata
DC current	50 mA	500 mA	>5 A
RF Power	Not available	2W avg. max	20W
Area	4 mm^2	645mm^2	8.3mm^2
BW(3 dB)	20GHz	20GHz	18GHz
Capacitance	8.2 pF	30 nF	3 pF
Inductance	18 nH	340 μH	1.2 nH
Insertion Loss	<1.5 dB, f<24 GHz	<1.5 dB,f<12 GHz	<1.5 dB,f<18 GHz
Return Loss	>10 dB, f<24 GHz	>12 dB,f<14 GHz	>10 dB,f<18 GHz

In addition to assembly of discrete components onto PolyStrata sockets, PolyStrata parts can be surface mounted onto microstrip or CPW structures. This technique has been demonstrated in [54]. 10- and 20-dB directional couplers designed for use about 26 GHz were measured and a PolyStrata component was assembled onto a high-resistivity Si CPW substrate. Polystrata structures for optimized wirebond transitions and direct connectorization of PolyStrata parts have also been developed. An SEM image of the 10-dB coupler and its measurements are shown in Figure 1.16. The directional coupler is designed using two coupled signal lines suspended in the same outer conductor shielding.



(a) (b)

Figure 1.16. (a) SEM image of 10-dB directional coupler. Inset represents the model used for FEM simulation (b) Simulated (dotted) vs. measured (solid) for a 10-dB coupler designed for use at 26 GHz [54] © 2008 IEEE.

It is also possible to create other types of components, particularly resonators [47] [55]. These resonators can be used to design various filters and sensors. One particularly interesting application of PolyStrata resonators is the 40/50 GHz diplexer presented in [56] (Fig. 1.17. Two comb line filters were designed with center frequencies at 40 GHz and 50 GHz. These filters were then combined into a diplexer using a coaxial T-junction between the ports. The realized diplexer has channels centered at 40.8 GHz and 51.1 GHz with fractional bandwidths of 2.36 GHz (5.8%) and 2.07 GHz (4.05%) and mid-band insertion losses of 1.58 dB and 3.52 dB, respectively. Channel-to-channel isolation is greater than 48.5 dB for all frequencies from 0.1-67 GHz [56].

Other PolyStrata components include baluns, rat-race hybrids, and antennas. A variety of antennas have been developed in PolyStrata, including cavity backed patch antennas [41] [58], spiral antennas, sinuous antennas, and log-periodic antennas [57] [59] [60]. These antennas can be arranged into arrays and monolithically fed. [61] demonstrates arrays of W- and G- band waveguide slot arrays, fed by rectangular coax. Cavity backed patch antennas and antenna arrays at W-band will be examined at length in Chapter 2. Two extremely wideband examples of the log-periodic antenna and their simulated VSWR are shown in

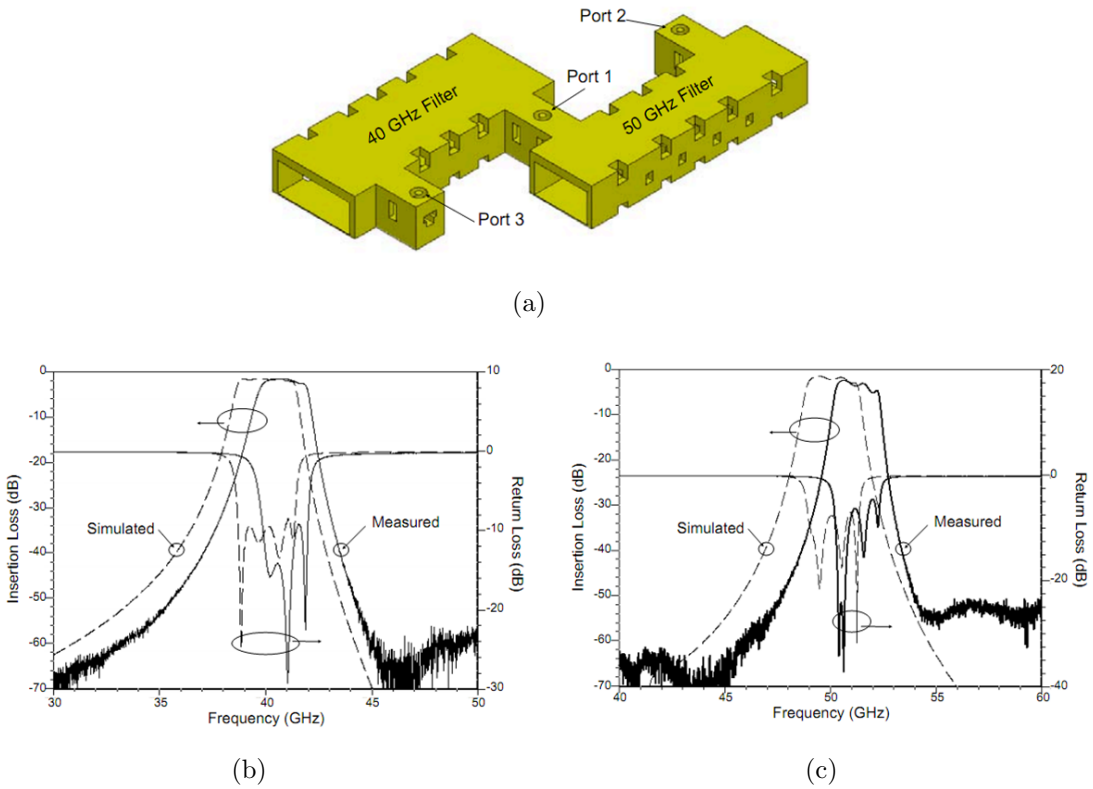


Figure 1.17. (a) 3-D model of 40/50 GHz diplexer (b) 40 GHz band measured vs simulated performance of diplexer (c) 50 GHz band measured vs simulated performance of diplexer

Figure 1.18. The planar log-periodic antenna (Fig. 1.18a) has a VSWR performance of less than 2 from 2-110 GHz. The end-fire log-periodic antenna (Fig. 1.18c) has VSWR less than 1.5 and gain greater than 6 dBi from 18-110 GHz. In addition to these two broadband antennas, [57] presents an additional version of each design with an integrated Polystrata notch filter at 60 GHz.

1.5 Proposed Architecture

While the LTCC monopulse front-end described in Section 1.3 exhibits high-performance at Ka-band, at much higher frequencies its performance is greatly degraded. A PolyStrata architecture has no dielectric loss tangent and high conductivity, greatly decreasing insertion

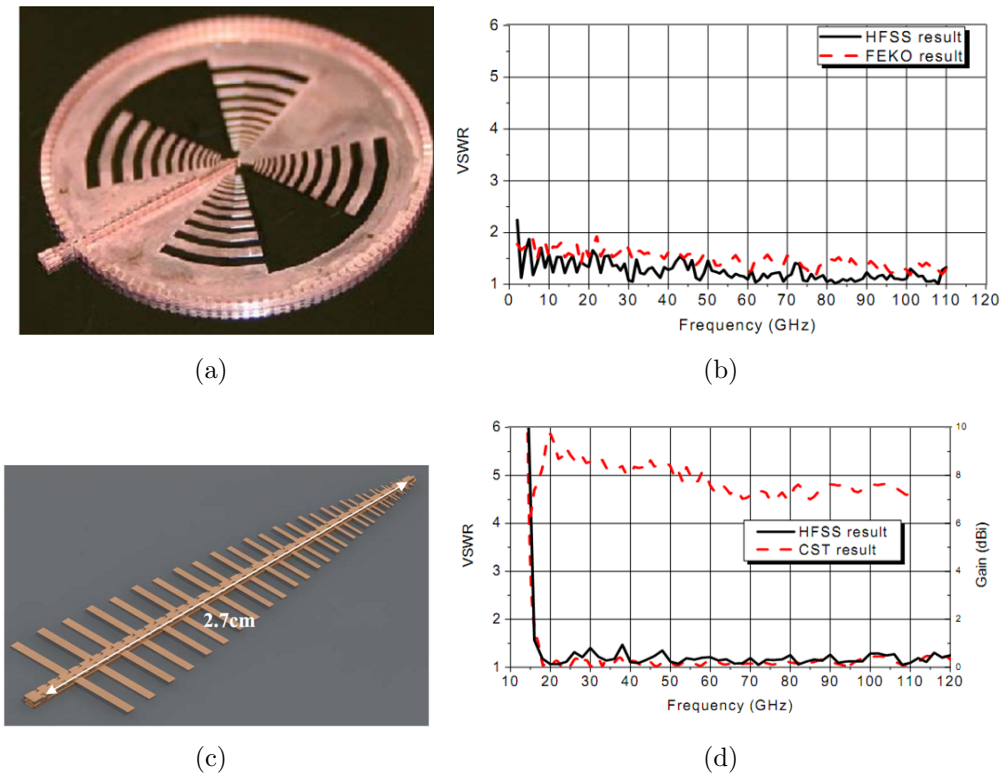


Figure 1.18. (a) Photograph of a fabricated planar 2-110 GHz log-periodic antenna with integrated feed/ impedance transformer (b) Simulation of planar log-periodic antenna VSWR. (c)Solidworks model of an 18-110 GHz end-fire log periodic antenna (d) Simulation of endfire log-periodic antenna VSWR and gain [57] © 2009 IEEE.

loss. Additionally, fully shielded coax architecture reduces radiation loss, coupling, and mitigates any substrate modes.

With the addition of monolithically integrated antennas and antenna arrays and the post-fabrication assembly of passives and actives, PolyStrata becomes a promising platform for highly integrated systems, such as the conceptual system shown in Figure 1.19. The diagram shows the integration of multiple passive and active components into a number of PolyStrata backplanes. These backplanes include RF and DC routing for the discrete components as well as passive PolyStrata RF structures, such as hybrid couplers and cavity resonators. The backplanes are vertically integrated to create a W-band steerable transceiver cell. A number of transceiver cells are connected together to create a much larger phased array. The W-band

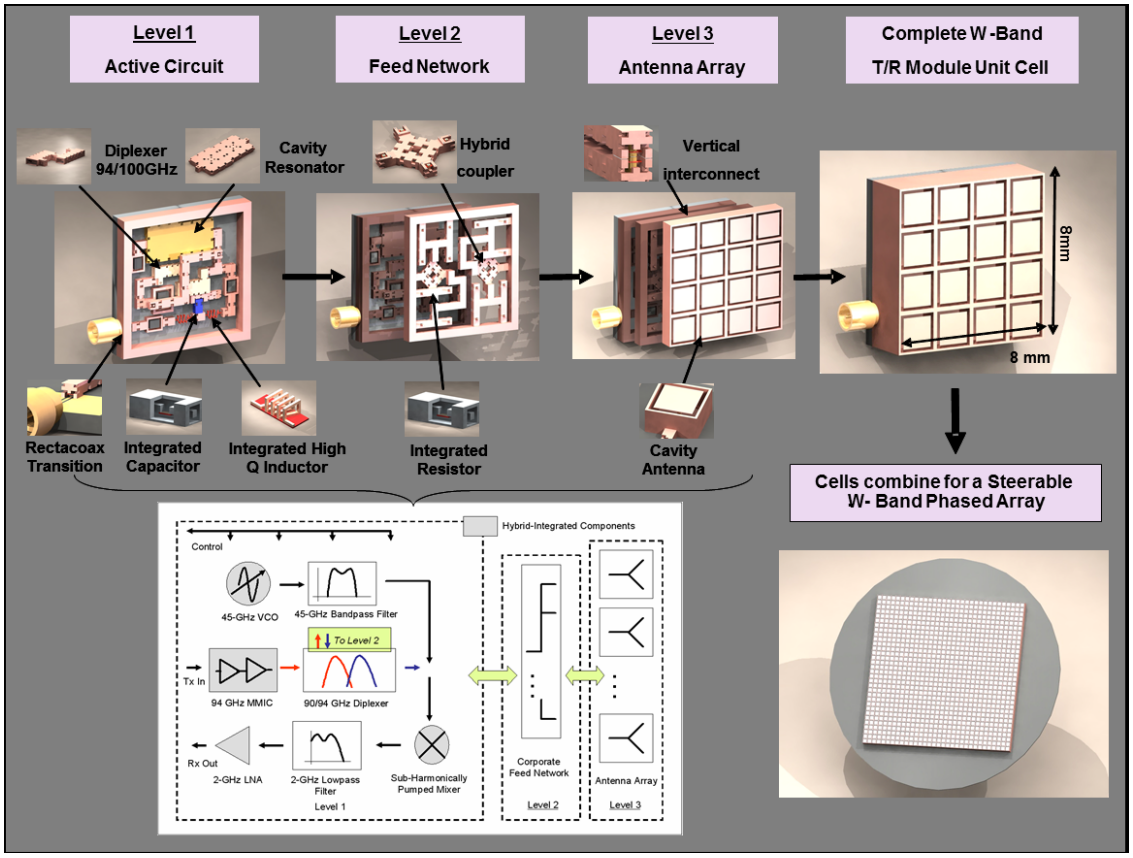


Figure 1.19. A conceptual 3-D PolyStrata W-band phased array T/R module implemented from PolyStrata transceiver "cells"

monopulse receiver outlined in this dissertation will use similar hybrid assembly techniques to integrate discrete components with PolyStrata routing and RF structures.

This dissertation is concerned with assembly the building blocks necessary for a W-band PolyStrata-based monopulse transceiver. One approach is to integrate all of the active circuitry onto a single MMIC, to be interfaced with a set of PolyStrata antennas, and packaged in PolyStrata to interface with the outside world. This effort involves the design of a SiGe W-band active monopulse comparator IC. The active monopulse comparator can be significantly broader band than traditional transmission line implementations, on the order of tens of GHz. The active monopulse comparator architecture employed also adds gain to the system, a crucial component at W-band, where transmission attenuation is higher.

W-band MMICs remain very expensive, however. As a low-cost, lower-performance alternative, a fully passive PolyStrata monopulse receiver is also explored. This system is an evolution of traditional microstrip comparator architectures that capitalizes on the low-loss, high isolation, and 3-D routing capabilities of PolyStrata. The use of these architectures is intended to eliminate some of the complexity traditionally associated with millimeter-wave systems.

1.6 Dissertation Organization

This dissertation consists of seven chapters. Chapter two focuses on the design and simulation of PolyStrata cavity backed antennas and antenna arrays. A number of measurement techniques as well as a series of measured results are described. Chapter 3 decribes the design of a 94-GHz rat-race hybrid, as well as its monolithic integration into a passive monopulse comparator network. Simulated and measured results for a full passive monopulse receiver incorporating a passive, rectangular coaxially based monopulse comparator network, an antenna array, and diode detectors are presented.

Chapter 4 describes the design of a 94-GHz 2-port active monopulse comparator network IC using the IBM 8HP SiGe process. Chapter 5 discusses the design of a 4-port 24 GHz active monopulse comparator IC using the IBM 8RF 130 nm RFCMOS process. Chapter 6 examines a series of V- and W-band GHz power combining network designs in rectangular coax, as well as the initial steps to designing a 94 GHz solid-state power amplifer (SSPA). Chapter 7 will discuss the contributions of this work to the field and outline two conceptual monopulse transceivers using the technology developed in this dissertation.

Chapter 2

W-band Polystrata Cavity-Backed Patch Antenna Arrays

Antennas are critical components for millimeter wave systems. Antennas, or arrays of antennas, often dictate the effective range of a system. They also tend to be a limiting factor for overall system system size. It can also be challenging to integrate antennas with MMICs or other circuitry at mm-wave frequencies. This chapter will outline the design, simulation, fabrication and testing of W-band PolyStrata-based cavity-backed patch antenna arrays. Both waveguide and diode-detector based measurement architectures will be discussed.

2.1 Millimeter-wave antennas

Mm-wave antennas are a critical component of any mm-wave systems. A variety of antenna structures and configurations have been explored to suit arange of applications. For example, long-range radio-astronomy applications typically use arrays of high-gain electrically large parabolic antennas [62]. The Atacama Large Millimeter/submillimeter Array (ALMA), which is scheduled for completion in 2012, is comprised of 66 antennas functioning from 30-1000 GHz with a combined synthetic aperture of 18 km [63]. These antennas are very high gain, but occupy vast amounts of space (on the order of km), which is not desirable for

compact mm-wave systems.

One option for more compact antennas and antenna arrays are waveguide horns and slot arrays [64] [65]. [64] demonstrates a 60 GHz waveguide slot array created from a series of laminated metal structures. A 16 x 16 array is shown to have a gain of 32 dBi and a gain bandwidth of 11%. Another common technique for creating compact millimeter-wave antennas is the utilization of Printed Circuit Board (PCB) materials to create antennas. PCB architectures represent an improvement in size over waveguide slot arrays, as well as potentially easier integration with other microwave circuitry.

A differentially-driven K-band Yagi-Uda antenna printed on two sides of a Teflon substrate was demonstrated in [66]. 19.4 $\pm$ 0.7 dB gain was reported. A 60 GHz dual-polarized series fed patch antenna array has been demonstrated, also on Teflon [67]. [68] presented a dual-polarized sinuous UWB antenna fabricated on Rogers/Duroid 3010 substrate with an integrated silicon dielectric lens up to 24 GHz. However, loss tangents for PCB dielectric materials increase insertion loss at high frequencies and degrade performance. This makes PCB-based antennas less attractive at W-band. Other fabrication techniques are often employed at these frequencies to improve insertion loss.

One low-cost solution is the fabrication of antennas and arrays on plastic substrates with lower loss tangents. In [69], a 40- and 60-GHz waveguide horn arrays are demonstrated on Cyclo-Olefin Polymer and Grafted Olefin Styrene substrates, respectively. These plastic substrates are chosen for their flexibility and relatively low manufacturing cost. A plastic 77 GHz slot array was presented in [70].

Another interesting fabrication technique is the formation of three-dimensional antenna structures. Often, the mechanical structures are formed in polymer and coated with a metal, several skin depths thick at the frequency of interest. The work in [71] demonstrates a dielectrically loaded Ka-band waveguide horn array. The array is formed by a stereolithographic technique, and then plated with copper. A vertical, copper-coated polymer W-band Yagi-Uda antenna was presented in [72]. The antenna was fabricated as a series of monopoles, and

functions as a Yagi-Uda via the image theory. Using the same technique, W-band monopole antennas are integrated onto a variety of substrates (including Si, sapphire, and soda-lime glass) in [73].

One factor driving the development of mm-wave antennas is the ease of integration with active mm-wave devices. A number of implementations of antennas on semiconductors substrate via post-processing techniques have been explored. The 60- and 77- GHz Yagi-Uda antennas in [74] are supported on a thin membrane of SiO_2/Si_3N_4 over GaAs. [75] demonstrates a 75-110 GHz tapered slot antenna for integration with 325 μm thick low-resistivity Si. The antenna is suspended on a benzocyclobutene (BCB) membrane over the silicon. 4.6 dBi gain was demonstrated across the band. A 60 GHz waveguide horn antenna directly integrated with a silicon substrate was demonstrated in [76]. In the University of Michigan 94 GHz monopulse receiver discussed in Chapter 1 ([27]), four integrated horn cavities as antennas were demonstrated. The integrated horn cavities were 70° flared bulk micromachined silicon cavities with dual dipole antennas. Several silicon wafers with different size etched holes in them were stacked to create the full structure, with the detector diodes directly integrated.

A further drive for integration is development of antennas using standard semiconductor manufacturing techniques. A G-band (210 GHz) bowtie dipole antenna (presented in [77]) was fabricated using standard III-IV semiconductor manufacturing air-bridge techniques. It is fed by a gold post from the CPW on the Si-GaAs substrate. A triangular 60-GHz monopole antenna is fabricated using the metal layers in the commercially available TSMC 0.18 μm CMOS process in [78]. [79] demonstrates a fully integrated 60 GHz on-off keying receiver in a commercial 90 nm RF CMOS process, including on-chip ntenna. [79] also provides a good overview of techniques to reduce the effects of the high permittivity of Si on radiation efficiency. The 94 GHz planar log-periodic antenna developed in [80] was designed in a GaAs MMIC process and uses in-process air-bridges as the crossovers in the antenna.

A large number of systems operating in the 60 GHz range have recently been implemented

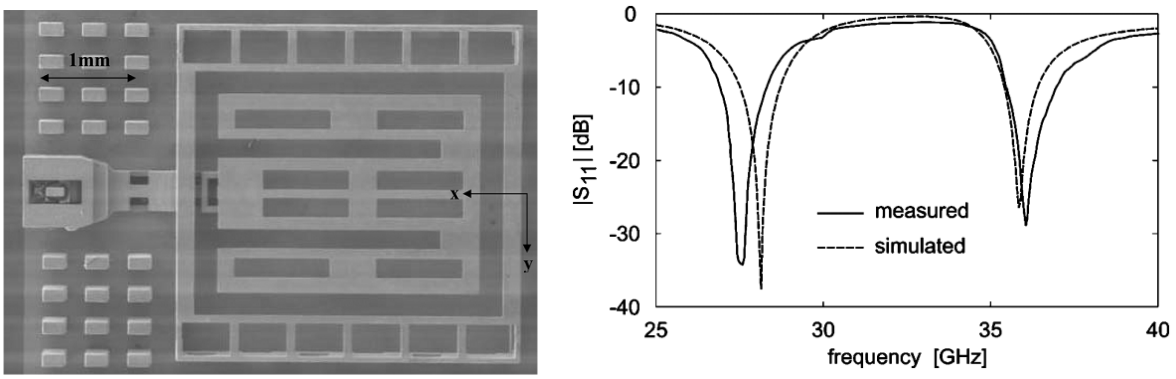
for high-data-rate wireless transfer. Some highly integrated Multi-chip modules (MCMs) with antennas have been produced for this application. [16] implements an end-fire post-wall waveguide horn with a receiver chip into a package. A single horn with directors and a dual-antenna package for transmit and receive are demonstrated. The antenna with directors demonstrated a gain greater than 6 dBi across the 58-68 GHz range with 60° and 30° beamwidths in the E- and H-plane respectively. A 4x6 antenna array with integrated MMIC downconverters was reported in [81]. The antenna array and feeding network are constructed from multilayer microstrip structures made of fluorine resin.

LTCC is also a popular platform for realizing mm-wave antennas. LTCC has been used to implement grid array antennas [30], stacked ring antennas [82], and many other architectures. LTCC is also useful for packaging antennas integrated with MMICs, as in [83]. An interesting 94 GHz Vivaldi antenna is presented in [84]. A machined horn hybridly assembled with the LTCC substrate to improve performance.

As discussed above, the drive for low-cost, low-profile antennas and integration with MMICs has led to the development of a wide variety of antenna architectures and configurations. However, this chapter will focus on a particular antenna type: the micromachined patch antenna.

2.2 Micromachined Patch Antennas

Microstrip patch antennas have long been of particular interest, due to their planar profile and relative simplicity for fabrication, as well as the ability to easily integrate with ICs. A number of variations on the patch antenna have been developed on a variety of platforms. For example, a 2x1 60 GHz patch array antenna which is fully compatible with commercial CMOS processes was developed in [85]. In [86], a 25 GHz elevated microstrip antenna based on surface micromachining was designed and fabricated. In [87], a G-band overlapping, elevated patch has been demonstrated using gold posts and traces on a semi-insulating GaAs

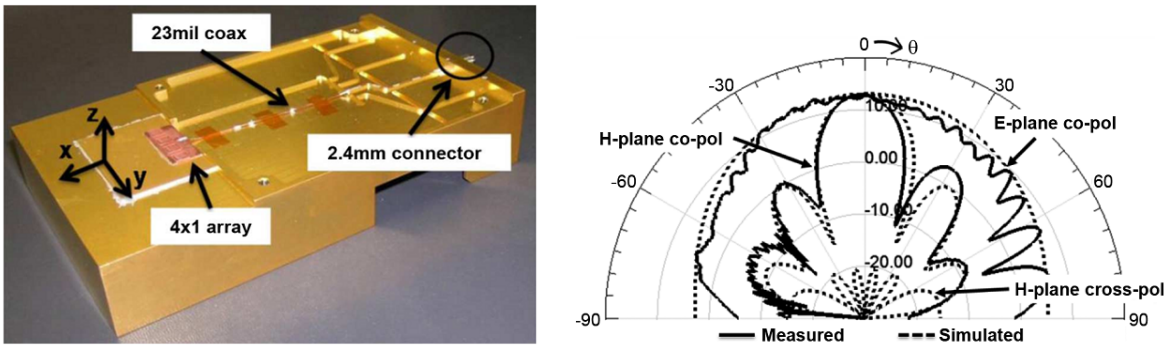


(a) (b)

Figure 2.1. (a) SEM image of a probeable single 36 GHz PolyStrata cavity-backed patch antenna (b) Simulated and measured return loss results for a probed single cavity-backed patch antenna [41] ©2007 IEEE

substrate. A 4 x 2 array of 60 GHz patches on a polydimethylsiloxane (PDMS) substrate is demonstrated in [88]. PDMS is a flexible polymer, allowing the antenna array to be bent into a conformal shape.

Patch antennas have also been used in highly integrated mm-wave systems. An array of hybridly integrated 60 GHz patch antennas on a micromachined high-resistivity Si was integrated with active devices in a "system in a package" configuration in [17]. [89] presents a novel integration of a W-band microstrip patch on quartz with a Si MMIC power amplifier. Both on-chip 60 GHz patch antennas and stacked microstrip patches are demonstrated in an effort to realize low-cost, highly integrated 60 GHz receivers using commercial CMOS in [18]. Due to the interest in creating integrated systems with high performance patch arrays; this chapter will demonstrate the development of a patch antenna array using rectangular coax structures. Of direct relevance to the this dissertation, the work presented in [41] demonstrated a 36 GHz cavity-backed patch antenna fabricated in the Polystrata process. The antenna and its measured results are shown in Fig. 2.1. A 4% bandwidth at 36 GHz was measured, and a gain of about 6 dBi. The antenna is an E-shaped patch, with additional holes to facilitate the release of sacrificial photoresist in fabrication, as discussed in Section 1.4. [90] and [44] incorporate the Ka-band patch into an array and a phased array, respectively.



(a) (b)

Figure 2.2. (a) Fabricated 4 x 1 Ka-band patch array in test fixture(b) Simulated and measured patterns for the array [90] ©2009 IEEE

[90] presents measured results of a 4x1 array of cavity-backed patch antennas which are corporately combined using rectangular coax. The combining network has an insertion loss of less than 0.5 dB at Ka-band. Additional slits in each antenna element are added to extend the bandwidth to 8% at 36 GHz. The gain and bandwidth of the array are 12.73 dBi and 13.7 %, respectively. Array patterns, as well as a fabricated antenna array mounted on its test structure are shown in Fig. 2.2.

However, scaling the design and fabrication of these antennas to W-band frequencies presents unique challenges, as well as opportunities. Material losses become more significant at W-band; however, PolyStrata structures have air dielectrics, significantly mitigating this issue. The reduced cavity depth of the W-band antenna allows for monolithic vertical integration of the feed network underneath the antennas, as opposed to interspersed between antennas, as in [90]. The integration of waveguide backshort transitions to rectangular coax also becomes practical at W-band frequencies.

2.3 Design of W-band PolyStrata cavity-backed patch antennas

Initial selection of design parameters for a PolyStrata cavity-backed patch antenna can be approached in much the same way as the design of a standard microstrip patch antenna, using a transmission line model, as outlined in [91]. Initial design of patch width, W, is determined by Equation 2.1:

$$W = \frac{1}{2f_r\sqrt{\mu_o\epsilon_o}}\sqrt{\frac{2}{\epsilon_r + 1}} \tag{2.1}$$

Since $\epsilon_r = 1$ for PolyStrata structures, the width is simply $\frac{\lambda}{2}$ at the frequency of interest. The antennas in this chapter are designed at 94 GHz. ΔL represents the effective length extension given by the fringing fields at the edge of the patch, and is approximated using Equation 2.2:‘

$$\frac{\Delta L}{h} = 0.412\frac{(\epsilon_{reff} + 0.3)(\frac{W}{h} + 0.264)}{(\epsilon_{reff} - 0.258)(\frac{W}{h} + 0.8)} \tag{2.2}$$

h is the thickness of the microstrip substrate or, for the PolyStrata structure, the distance from the backside of the patch to the cavity below. Based on the available layer stackup, h is 300 μm. The effective dielectric of the patch, ϵ_{reff}, is one. Equation 2.3 yields the designed patch length, L:

$$L = \frac{\lambda}{2} - 2\Delta L \tag{2.3}$$

After initial parameters are calculated, the optimization of the design is performed using HFSS 3-D FEM software [92]. The patch dimensions L and W are shown in Fig. 2.3b, and are 1110 μm and 862 μm, respectively.

The major difference between the Polystrata patch and its traditional microstrip counterpart is the feed point. The PolyStrata feed is based on a standard rectangular coaxial structure, the dimensions of which are shown in Fig. 2.3a, and the center conductor of which connects to the patch from its underside. The rectangular coax center conductor is

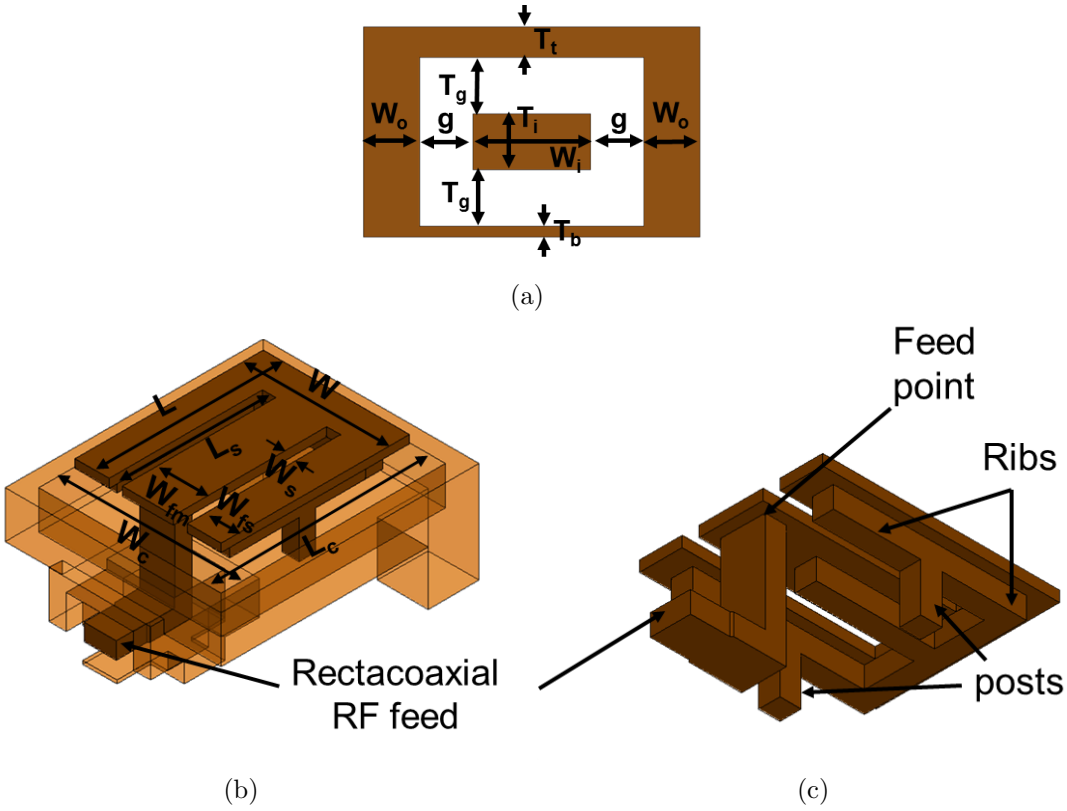


Figure 2.3. (a) Cross-section of air-dielectric rectacoax structure. Inner conductor is suspended on a periodic dielectric support strap inside of the outer conductor. Dimensions for a 50 Ω line: T_g = T_i =100 μm, W_i = 178 μm, g= 111 μm, W_o = 100 μm, T_b = 75 μm, and T_t = 75 μm. (b) Structure of 94 GHz cavity-backed patch antenna with vertically integrated feed. Dimensions are: W = 862 μm, L = 1110 μm, L_s=905 μm, W_s=80 μm, W_{fs}=201 μm, W_{fm} = 300 μm, W_c =1074 μm and L_c = 1322 μm (c) Underside of antenna-mechanical ribs add stability, posts support the structure. Feed is shown contacting patch. W_{fp} = 55 μm.

periodically supported by dielectric straps, which are not shown. The antenna element is a cavity-backed "E-shaped" patch antenna; the slits in the patch are designed to improve impedance matching and tune frequency performance [58]. After optimization using HFSS, the antenna structure, with relevant dimensions, is shown in Fig. 2.3b-c. The slits are 905 μm in length (L_s), 80 μm in width (W_s), and located 150 μm from the center line of the antenna. Variation in L_s significantly impacts matching for the antenna. Figure 2.4 shows variation in the slit length in increments of 10 μm. 10 μm variations may result in up to 12 dB variation in return loss, as well as detuning of the resonant frequency. The length of

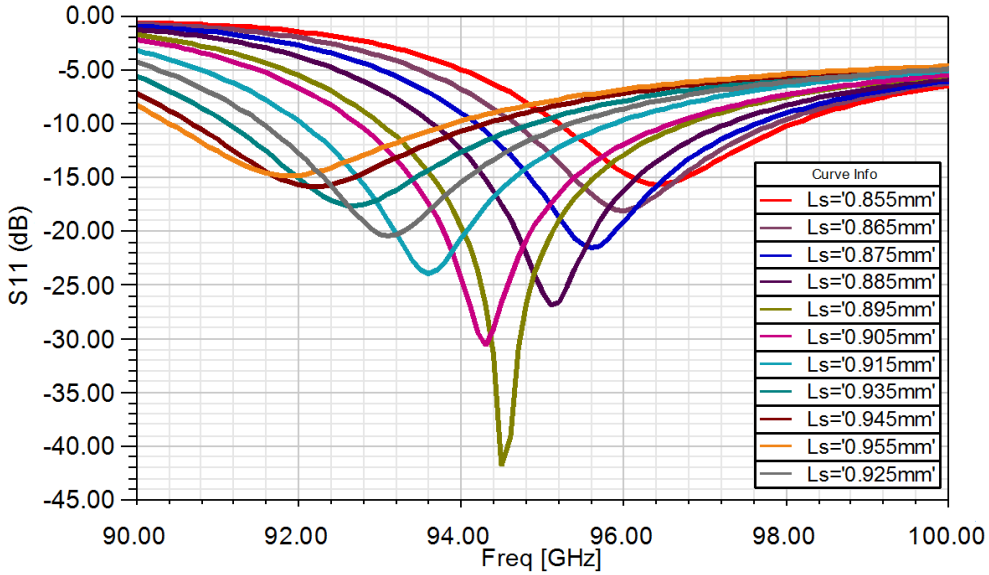


Figure 2.4. Variation in slit length, L_s in 10 μm increments.

the patch (L) is 1110 μm, which is approximately one-third the wavelength at the design frequency of 94 GHz; the width (W) is 862 μm.

The dimensions of the cavity are 1074 μm x 1322 μm (W_c x L_c), leaving a gap between the antenna structure and the outer walls of 106 μm on all four sides of the antenna. The outer walls of the cavity were lowered such that there is a height difference (H_g) of 150 μm between the antenna element and the outer, grounded wall (Fig. 2.5a) which surrounds each element. This provides an improvement in gain and bandwidth, based on the work presented in [93]. This height is limited by the available layer thicknesses of the PolyStrata process. Details of this optimization are shown in Figure 2.5b&c. Reducing H_g increases boresight gain and reduces beamwidth. However, decreasing H_g also results in a pattern null in the E-plane at 90° from boresight and increased sensitivity to cross-polarized signals.

The outer cavity walls are 100 μm (W_{cw}) thick. The underside of the antenna is located 325 μm (H_t) above the ground plane of the cavity, and the patch is 50 μm (H_p) thick. The antenna is made more mechanically stable by 100 μm thick ribs, which can be seen in Fig. 2.3c. The structure is supported by two 100 x 100 μm posts located in the virtual ground of the patch. These posts do not affect the designed electrical performance of the antenna

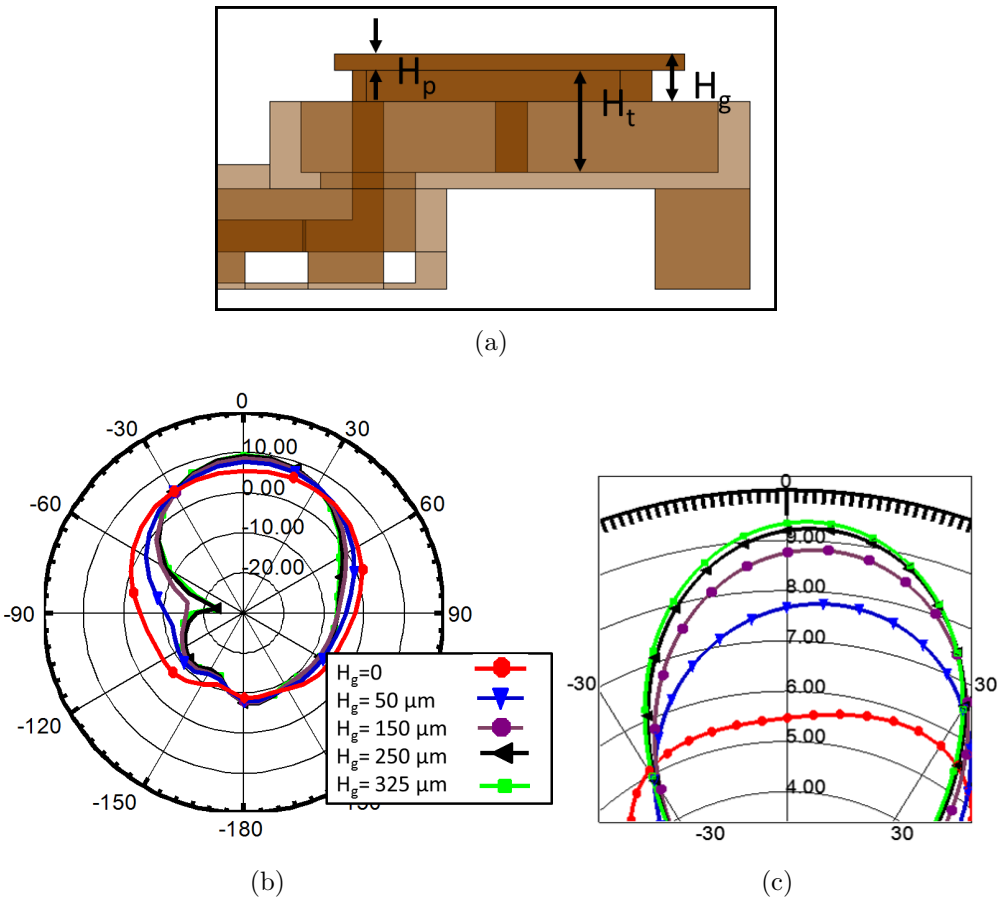


Figure 2.5. (a) Side-view of patch antenna, detailing wall height gap (H_g). H_g is the distance from the top face of the antenna element to the top of the grounded wall which surrounds the element. $H_t = 325\mu$m and $H_p = 50\mu$m (b) Simulated variation in E-plane co-pol pattern due to changes in H_g. Simulations were performed using HFSS FEM software (c) Simulated detail of boresight pattern changes. Increasing H_g increases gain.

at 94.5 GHz, but do result in a second radiation band around 77 GHz, with a monopole-like pattern. This pattern arises from a combination of the supporting posts which act as a pair of monopoles, which are capacitively loaded by the patch, lowering their resonant frequency. The 77 GHz band provides potential additional functionality, as this band is a possible operating frequency for automotive radar systems. Similar behavior from this type of antenna was previously documented in [41].

The dimensions and location of the feedpoint contact with the patch (210 μm x 100 μm) are critical to the impedance matching of the antenna. The feed point is located along the

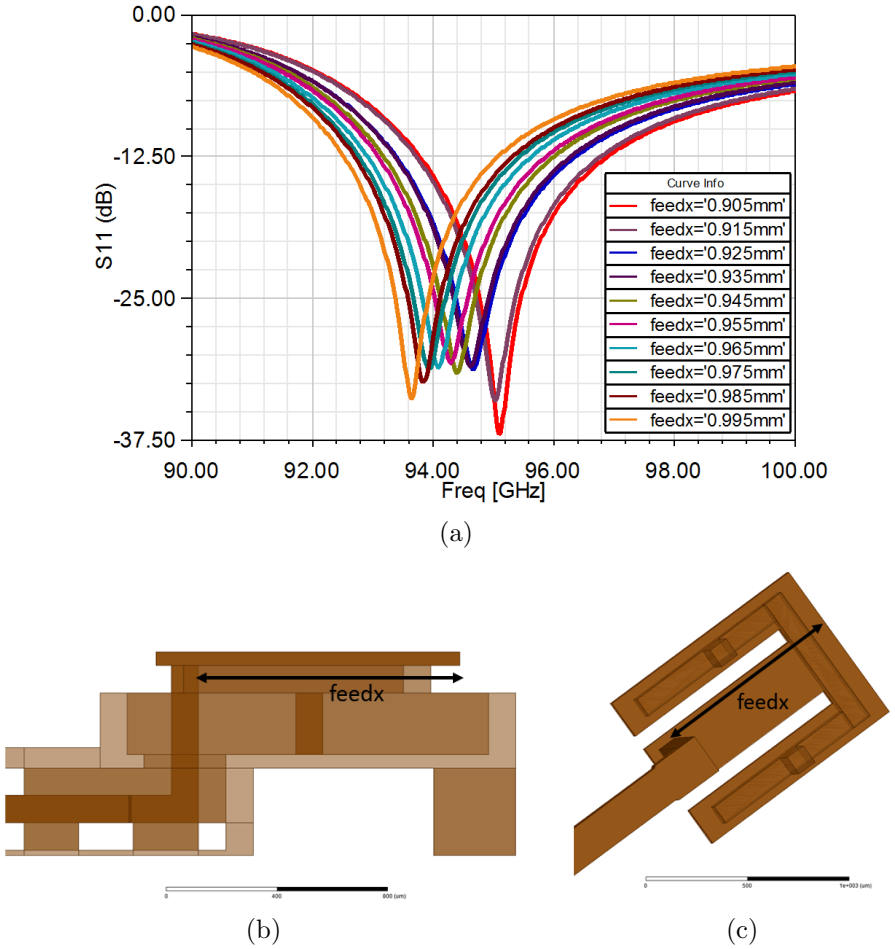
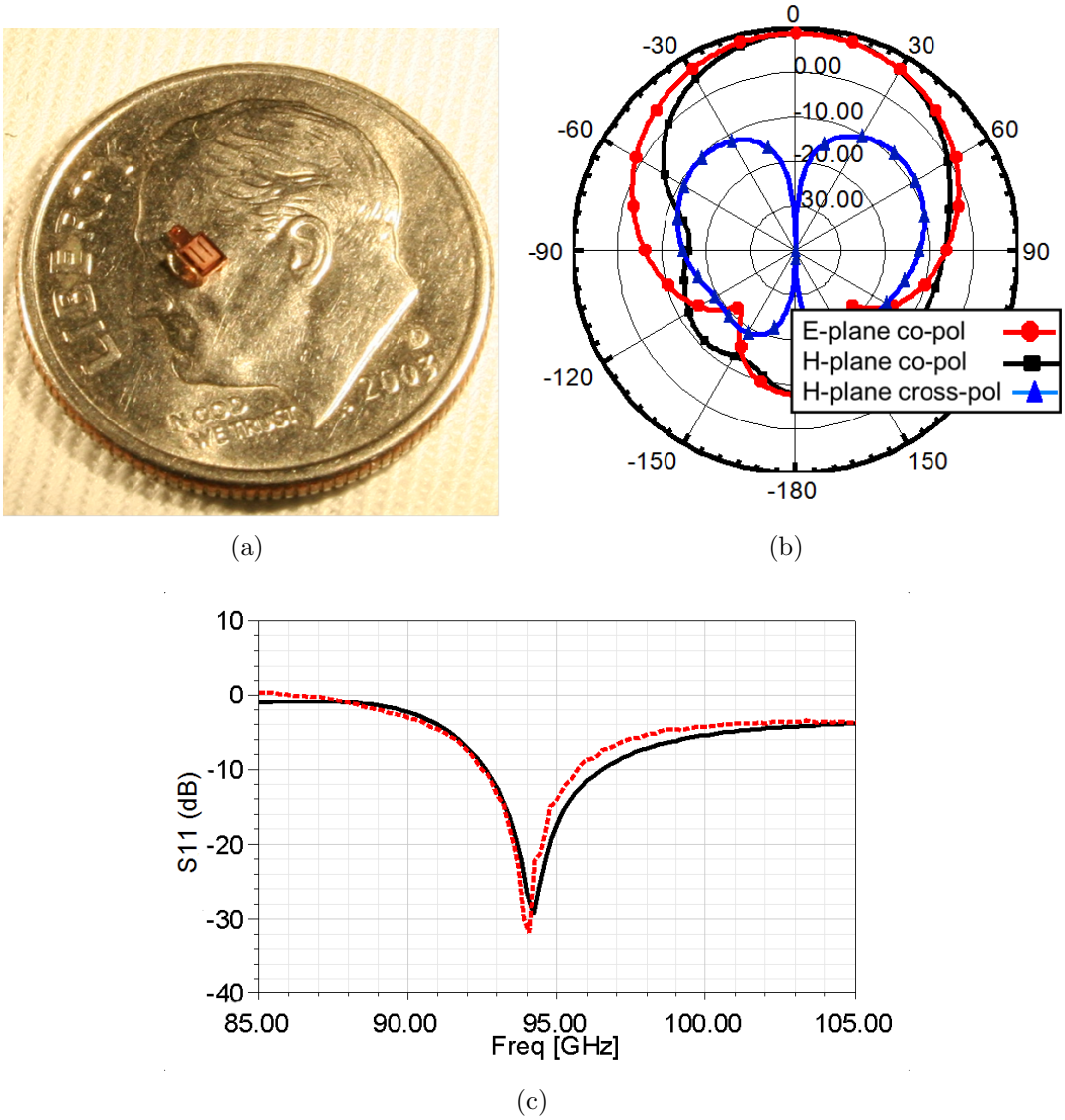


Figure 2.6. (a) Variation of feed location in an x direction. Changes in feed location directly impact center frequency. (b) Side view of antenna and feed. Feedx is measured from the unslitted edge of the antenna to the closest edge of the feedpoint.(c) View of the underside of antenna, backing cavity removed.

E-plane center line of the antenna, 55 μm (W_{fp}) from the edge of the patch which has no slit openings (this dimension is referred to as feedx). The feed is an extension of a center conductor of a rectangular coaxial line located below the base of the cavity. The feeding rectacoax inner conductor has the same dimensions as the probe, and the inner dimensions of the outer conductor are 300 μm x 400 μm. Feed location impacts frequency performance, as shown in Figure 2.6a.

The simulated maximum gain of a single antenna at broadside is 8.3 dB, with a radiation



(a) (b)

(c)

Figure 2.7. (a) Fabricated single antenna with probe point (b) Simulated antenna patterns for a single cavity-backed E-shaped Polystrata patch antenna (c) measured and simulated return loss for a single antenna

efficiency of 95% and a 3-dB beamwidth of 76° in the E-plane, as shown in Figure 2.7b. The simulated 10-dB return loss bandwidth is 4.15 GHz, or 4.4°. The antenna is fabricated with a launch designed for probing with a standard 150 μm-pitch GSG probes, as discussed in Chapter 1. Return loss characterization is performed using a Cascade ACP 110 1mm coax probe and an HP 8510C vector network analyzer with mm-wave extenders. A custom

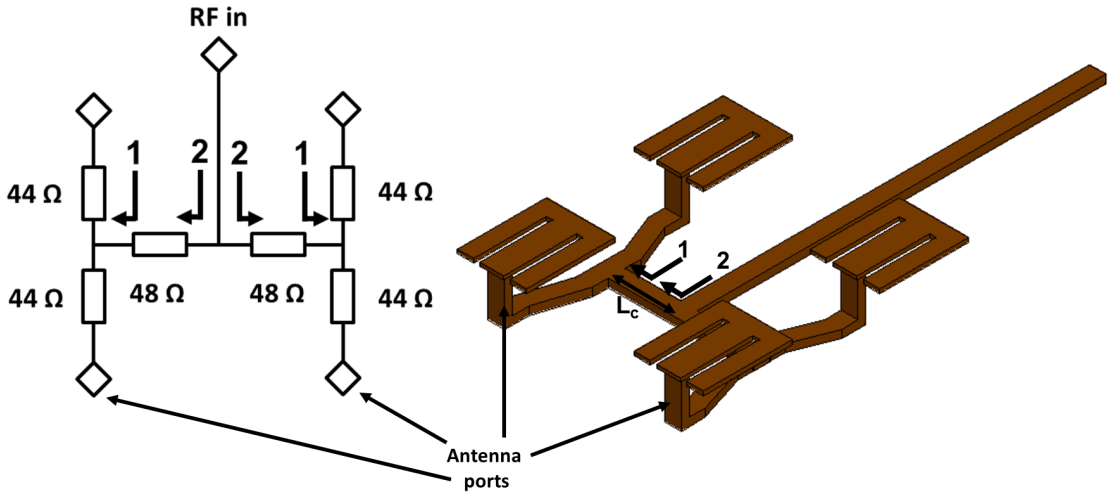


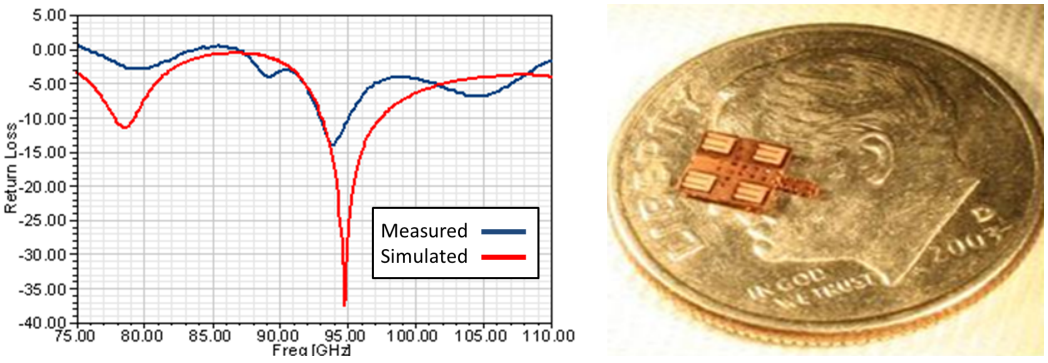
Figure 2.8. Circuit diagram and inner conductors for array feed network. Outer conductor not shown for clarity. All antenna ports are 44 Ω, RF input impedance is 50 Ω. L_c= 800 μm
.

rectangular coaxial TRL standard is used for calibration. Measured return loss results show a good correlation with simulated results (Figure 2.7c). A measured 10-dB bandwidth of 3.25 GHz, or 3.5%, and a maximum return loss of 32 dB are demonstrated. While maximum return loss is slightly better than the simulated result, 10 dB return loss bandwidth is reduced. Line loss greater than simulated would increase measured return loss and slight shift in resonant frequency may result in a slight increase in return loss. The frequency shift is related to small variations in layer thicknesses (<10 μm cumulative).

2.4 2x2 Antenna Array

Using the patch antennas described in the preceding section, a 2x2 array was designed with an integrated feed network. The antennas are spaced 2200 μm apart ($\sim 0.69\lambda$), in an effort to maximize broadside gain, while minimizing grating lobe presence. The array is located on top of the feed network, which is based on rectangular coaxial line with a cross-section shown in 2.3, differing only in the dimension W_i.

This feed network (Figure 2.8) divides the input power source four ways to provide each

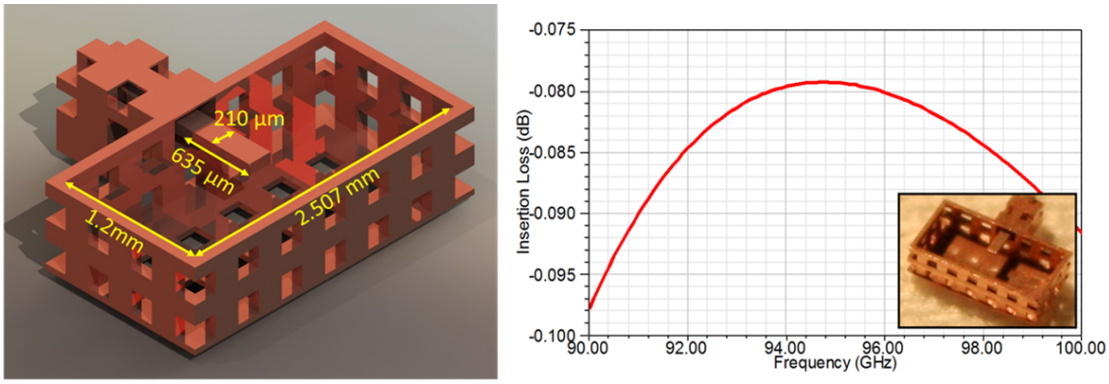


(a) (b)

Figure 2.9. (a) Measured and simulated results of an array of cavity-backed patch antennas. (b) Fabricated 2x2 array with GSG probing point

antenna with $\frac{1}{4}$ of the total power from the source. Figure 2.8a shows a circuit diagram of the impedance network; Figure 2.8b shows a CAD model of the network. Only the center conductors of the feed network are shown in Figure 2.8b. At each antenna port, the desired impedance is 44 Ω, based on the optimum dimensions for the feed at the feedpoint. Looking in to point 1 in 2.8b, the impedance is 22 Ω, the parallel combination of the two antenna feeds. This impedance network is replicated for the other pair of antennas. The RF input impedance is 50 Ω. Two 100 Ω impedances in parallel are required at point 2 to provide the correct impedance for the RF input. The 100 Ω impedances looking into point 2 are realized by a quarter wavelength impedance transformer, which has a line impedance of 48 Ω, operating on the 22 Ω impedance seen looking into point 1. The quarter wavelength impedance transformer between points 1 and 2 has $W_i = 190$ μm, and the transmission line between the antenna ports and point 1 has $W_i = 210$ μm.

A GSG probe point similar to that which was used for the single antenna is also fabricated with the antenna array, for use in return loss characterization. Results of the measurement are shown in Figure 2.9. Return loss measurements show a 14 dB return loss and a 2 GHz return loss bandwidth. Discrepancies between measured and simulated results are believed to have been due to the proximity of the GSG probe used to perform the measurements. The probe is less than 500 μm away from two of the antenna elements potentially causing



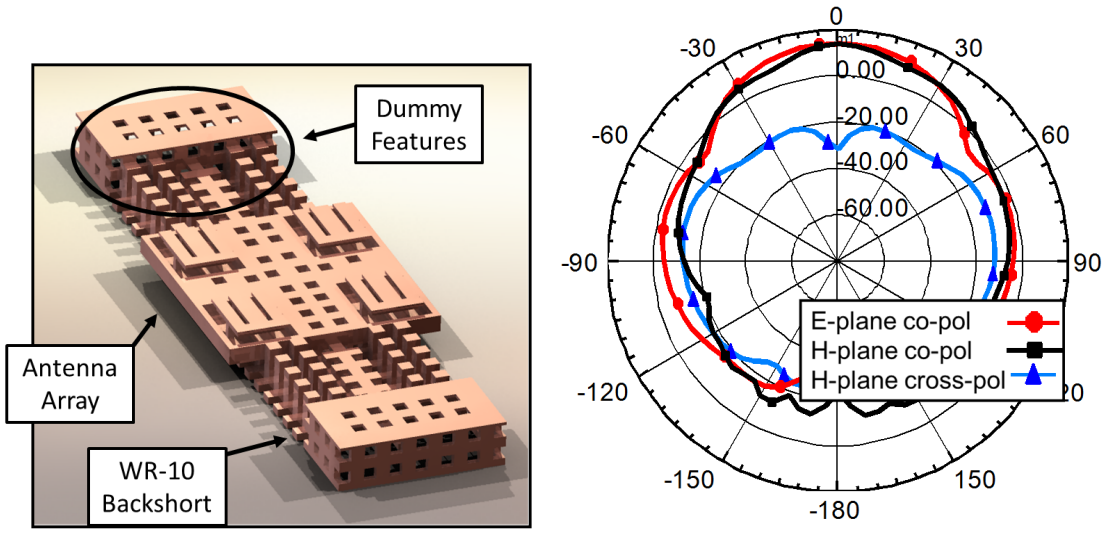
(a) (b)

Figure 2.10. (a) 3-D model of WR-10 transition to rectangular coaxial line. Distance from the top of the E-probe to the backshort is 475 μm ($\sim 0.15\lambda$) (b) Simulated E-probe insertion loss. Loss at 94.5 GHz is -0.08 dB (Inset: bottom view of WR-10 E-probe cavity)

undesired loading on portions of the array. A number of efforts to create probe-based antenna characterization systems ([94], [95]) have been undertaken, but each requires specialized equipment and results have been mixed. In order to mitigate these difficulties, the ability of the PolyStrata process to create 3-D monolithic structures has been leveraged to create transition structures which allow for improved return loss and pattern characterization.

2.5 Rectacoax transition to WR-10 waveguide

In order to facilitate the measurement of antenna performance and for future system integration, a transition from rectangular coax to WR-10 waveguide was fabricated based on an E-probe. This technique was also intended to mitigate some of the detuning effects of the GSG probe shown in previous measurements. A backshort was designed which maintains the inner dimensions of W-band waveguide (1.2 mm x 2.51 mm), with 100 μm walls. A number of holes are included in the backshort to facilitate the final release step of the PolyStrata process. These holes have a minimal effect on the simulation results. The E-probe is simply the extension of the feed network rectacoax center conductor into the backshort cavity. The probe is 210 μm in width, 100 μm thick, and extends 635 μm into the cavity. The distance



(a) (b)

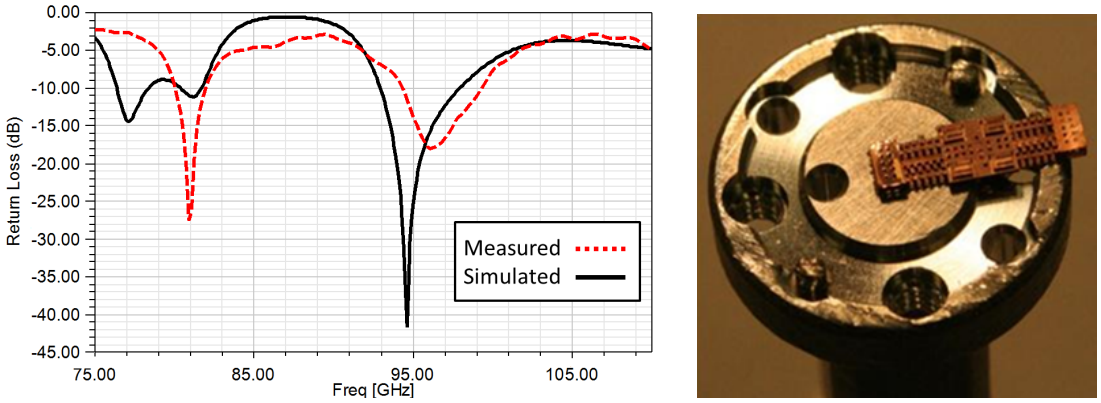
Figure 2.11. (a) Rendering of structure with WR-10 backshort transition and dummy features. (b) Simulated antenna pattern for antenna array with integrated feed and rectacoax transition to waveguide. Gain at 94 GHz is 13 dB.

from the cavity back to the E-probe is 475 μm, 0.15λ. These dimensions are chosen through optimization based on insertion loss simulations. The simulated insertion loss, shown in Figure 2.10, is 0.08 dB at 94.5 GHz.

The backshort design was fabricated with an antenna array, as well as dummy features (Figure 2.11a). These dummy features add mechanical stability, and also help extend the antenna groundplane. The backshort for the E-probe, as well as the rectacoax feed, is also duplicated in the dummy features. Initial designs which did not include this feature suffered from beam squint in the direction of the backshort, which reduced gain in addition to affecting the pattern. By adding the dummy backshort on the other side of the structure, this problem was eliminated. The total footprint of the part is 3.11 x 11.06 x 0.745mm.

FEM simulations of the array indicate an overall gain of the antenna array of 13 dB broadside, and a 3-dB beamwidth of 42°. The 10-dB return loss bandwidth is 4 GHz, or 4.2%. Simulated antenna patterns for the array are shown in Figure 2.11b.

To measure return loss, the Polystrata part was mounted directly to WR-10 waveguide.



(a) (b)

Figure 2.12. (a) Measured vs. simulated return loss measurements for antenna array with rectacoax transition to waveguide. Return loss of 18 dB and bandwidth of 4.6 GHz (4.9%) are measured. (b) Antenna mounted on WR-10 waveguide section for measurement.

This was accomplished using a manual die-bonder and Epotech HE-20 conductive silver epoxy. Verification of the alignment was performed optically, and the error was shown to be less than 20 μm. FEM simulations indicated that misalignment of this value would cause negligible additional loss. Measurements of return loss were performed by connecting the WR-10 section to the 75-110 GHZ mm-wave extender of the 8510C VNA.

After calibration, the waveguide section with attached antenna array was directed towards a piece of absorber located in the far field. The results are shown in Figure 2.12. A measured return loss of 18 dB and 10 dB return loss bandwidth of 4.6 GHz (4.9%) are reported, with good correlation with simulated results. Additionally, improvements in correlation between measured and simulated results over previous GSG probe measurements were observed, likely due to the removal of metal structures within close proximity of the antenna elements.

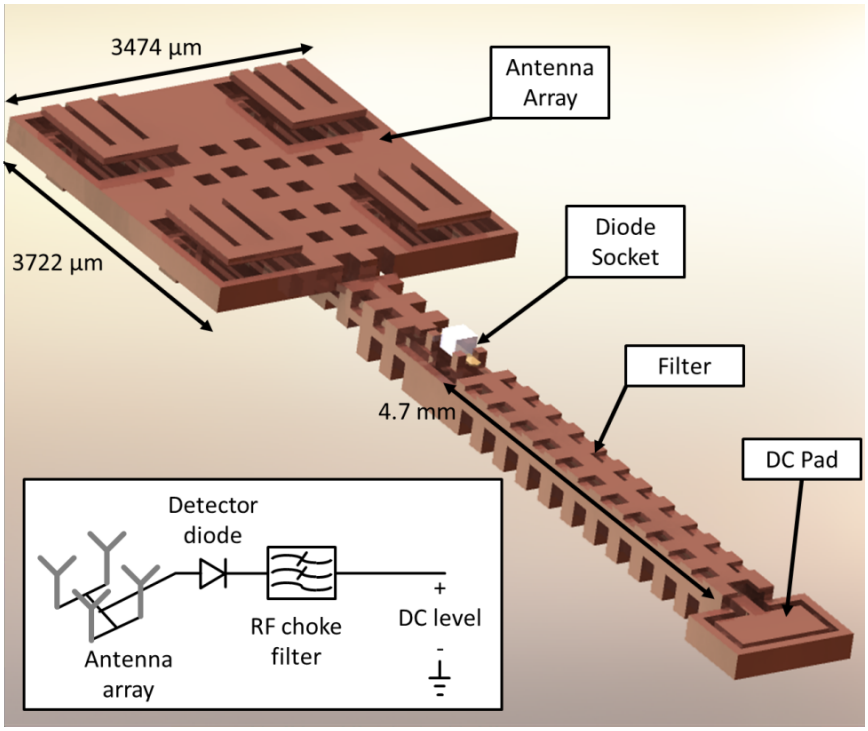


Figure 2.13. 3-D Model of Antenna array and diode detector. The diode is assembled with conductive silver epoxy into the PolyStrata socket. Antenna array is 3474 μm x 3722 μm. Output filter is 4.7mm in length (inset) block diagram of system

2.6 Antenna Array with Integrated Diode Detector

In order to facilitate antenna pattern measurements, an additional series of test structures was fabricated: an antenna array with an integrated diode detector. Measurement attempts using the previously described waveguide transition proved too cumbersome for use in the available motorized rotational stage for measuring antenna patterns. The necessary waveguide hardware was either too bulky to be easily accommodated by the motor, or required flexible waveguide. The integrated diode detector required only one DC lead for measurement, which was easily handled in the available pattern measurement system. In addition, the diode integration is representative of the future direction of more integrated PolyStrata microsystems combining passive structures and semiconductor devices and ICs. To minimize complexity and eliminate the need for the application of a bias voltage, a self-biased diode was selected: an Aeroflex/Metelics MZBD-9161 GaAs Beam-Lead detector diode. This diode

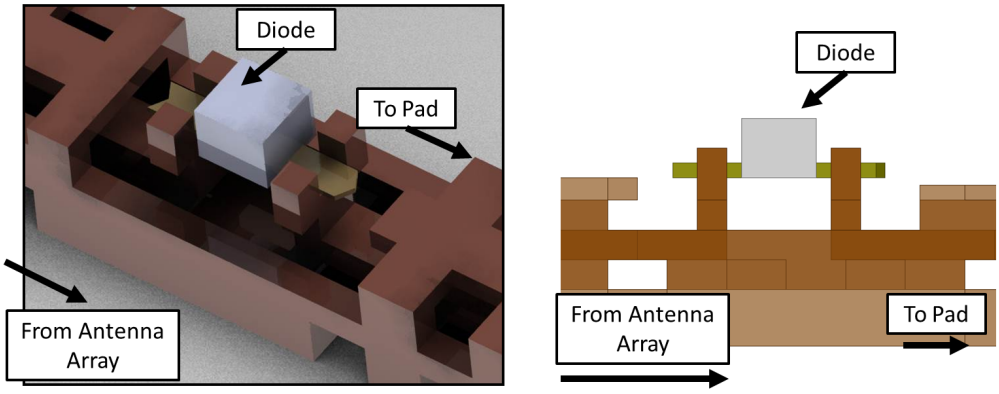
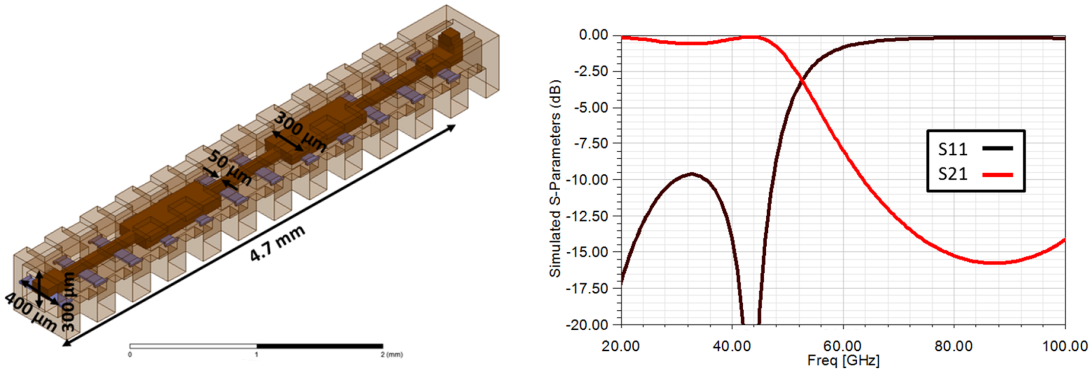


Figure 2.14. Detail of detector diode socket. Diode shown is a zero-bias GaAs beam-lead diode



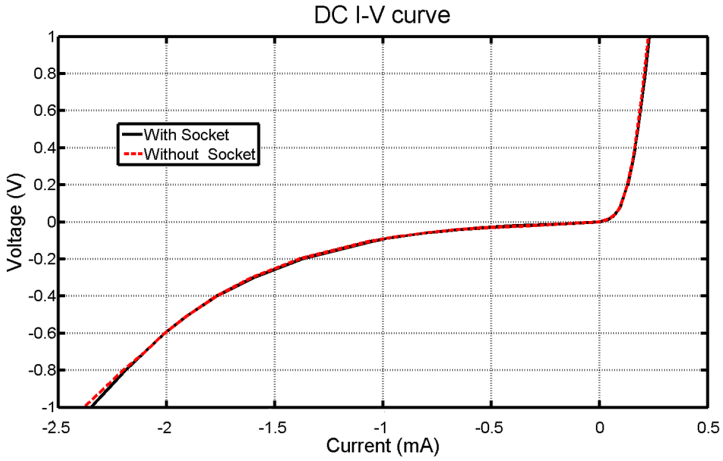
(a) (b)

Figure 2.15. (a) Stepped impedance filter structure. All four sections are 150 μm in length. Low impedance center conductors are 300 x 100 μm, and high impedance sections are 50 x 100 μm. Coax outer conductor is shown as transparent. (b) Simulated frequency response of the low-pass stepped impedance filter which follows the diode detector.

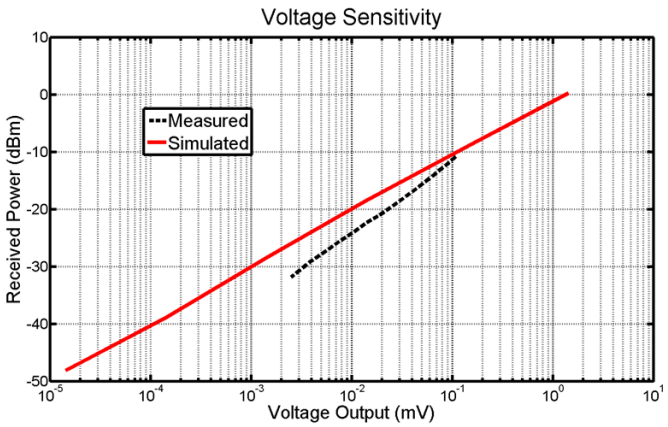
is useful for power measurements to 110 GHz. The diode is seated in a "socket", constructed out of rectangular coax (Figure 2.14). The integration of discrete passives and active devices with rectangular coax has previously been demonstrated using the same concept [**?**]. The diode socket is constructed based on the basic rectangular coax structure of PolyStrata transmission lines by breaking the center conductor and raising the structure several layers (200 μm) to facilitate assembly. To mechanically align the beam-leads of the diode, the pads have posts placed the width of the beam leads apart, giving the socket a "U" shape.

On one side of the break in the center conductor is the feed for the antenna array. On the other side of the diode, a stepped impedance low-pass filter prevents RF feed through. The filter is formed by alternating quarter wavelength segments of the widest and narrowest available coax center conductors, which yield 30Ω and 85 Ω, respectively. 3 high impedance and two low impedance sections are included. The filter is 4.7 mm in length, with 300 x 400 μm inner dimensions. A drawing of the filter and simulated filter performance is shown in Figure 2.15. 18 dB rejection at 94 GHz is simulated. Once the signal passes the filter, the DC signal level at the output of the filter is measured to determine the power output of the antennas. A specially designed pad for DC output voltage wire interconnection is included.

The diode was assembled by hand into the socket using conductive silver epoxy. Tests were performed to determine that no degradation in performance occurred when the diode was placed into the socket. A test structure with a probe point, diode socket, and output filter only was used for these measurements. The IV curve of the diode was measured, both before and after insertion into the socket (Figure 2.16a) and good correlation was shown in the results. Voltage sensitivity measurements were also performed at 94 GHz. The HP 8510 VNA with W-band extenders was used to generate the input signal and vary the power level. A waveguide calibration was performed on the system, and the loss due to cable conversion, cable and probes were quantified. Power measurements were performed using an HP 8486A power head and an HP E4419A power meter at the VNA waveguide port. The curve, shown in Figure 2.16b, was generated by applying 94 GHz signal of varying powers on one side of the test socket and measuring DC output voltage on the other side of the filter. The measured voltage sensitivity is 1304 mV/mW, compared to 1151 mV/mW simulated in Ansoft Designer circuit simulator diode model parameters provided by the manufacturer.



(a)



(b)

Figure 2.16. (a) Measured I-V curves for the diode detector with and without the rectangular coaxial socket (b) Diode voltage sensitivity measurements and simulations. A sensitivity of 1151.2 mV/mW was simulated, and 1304 mV/ mW was measured.

2.7 Array Measurement and Results

After initial characterization, the entire array/detector system was mounted onto a machined brass backplane which has a cutout on the top surface which ensures that the underside of the patch antenna is flush with the surrounding brass surface. DC wire attachment was done with conductive epoxy. The DC wire is AWG 30 enamel coated magnet wire. Additional stability was provided to the DC pad by underfilling it with non-conductive UV epoxy. The

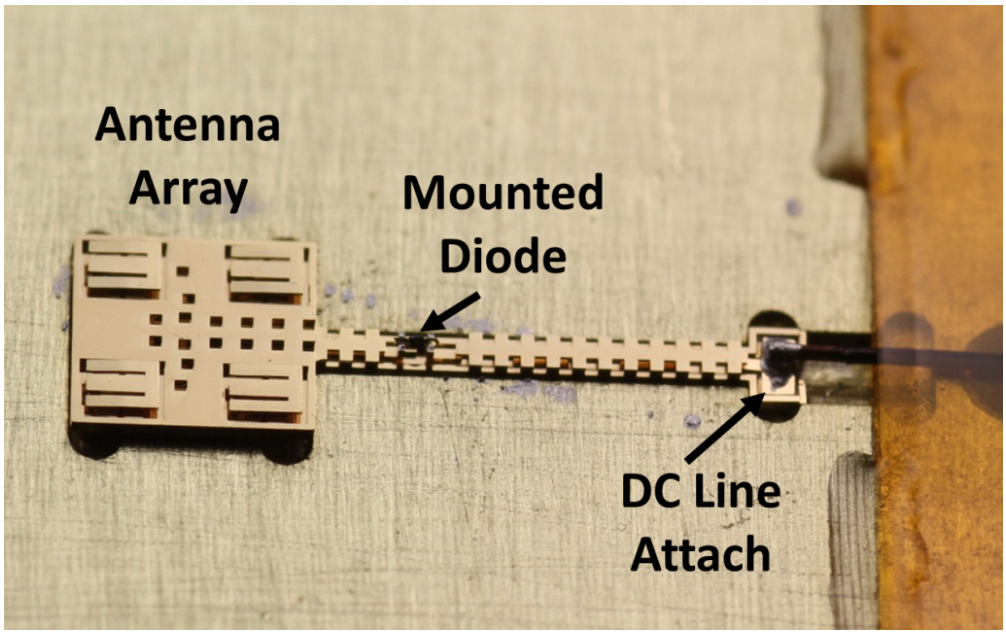


Figure 2.17. Mounted antenna part with diode and DC line. Diode and DC line attach are performed by hand using silver conductive epoxy

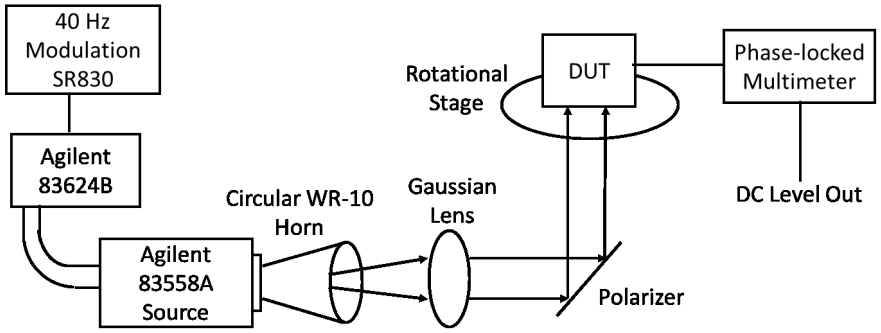


Figure 2.18. Test setup for antenna pattern measurement. A plane wavefront is generated, and the DUT is swept in elevation and azimuthal directions

fully assembled part is shown in Figure 2.17.

The antenna measurements for this device were performed at National Institute of Standards and Technology (NIST) in Boulder. The measurement setup diagram is shown in Figure 2.18. In order to improve DC level detection, the signal source was modulated with a 40 Hz signal, which was then phase locked to a multimeter on the output. A frequency doubler was used to provide the 94 GHz signal, with a circular WR-10 waveguide horn on the

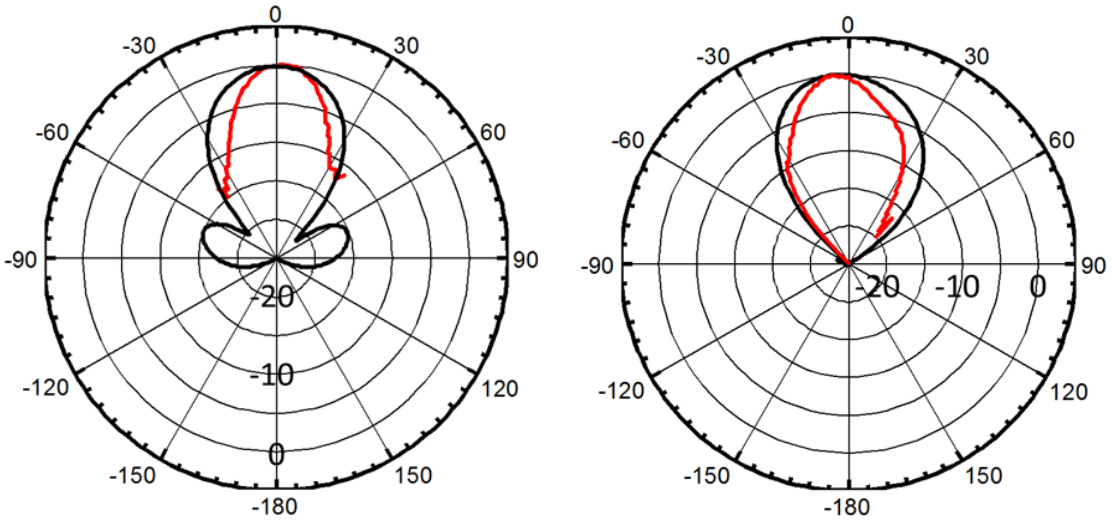


Figure 2.19. (a) Normalized H-plane co-polarization gain pattern (dB). (b) Normalized E-plane co-polarization gain pattern (dB). Black represents pattern simulated in HFSS, red indicates the measured data.

output. A Gaussian lens was used to provide a planar wavefront, which was then horizontally polarized. The DUT was mounted on a rotational stage which provides fine angular control in both elevational and azimuthal directions. Eccosorb absorber material was attached to the fixture on either side of the antenna to reduce reflections due to the planar wavefront.

A normalized E-plane co-polarization pattern is shown in Figure 2.19a. A reasonable correlation between measured and simulated can be seen in the figure. The pattern measurement covers $\pm 45°$ from boresight. The measurable angle is limited by the dynamic range of the diode detector. Figure 2.19b shows the normalized H-plane pattern. Cross-polarization measurements in the H-plane were also performed, by rotating the antenna 90 degrees. No power was detected by the diode detector. From the simulated results in Figure 2.11b, we see this is expected. The maximum power in the simulated H-plane cross-polarization pattern is 30 dB below the E-plane for all angles, thus beyond the dynamic range of the diode detector.

Further simulations of these patterns were performed to include the effects of the fixture and RF absorber materials. The RF absorber is approximated as a dielectric with dielectric

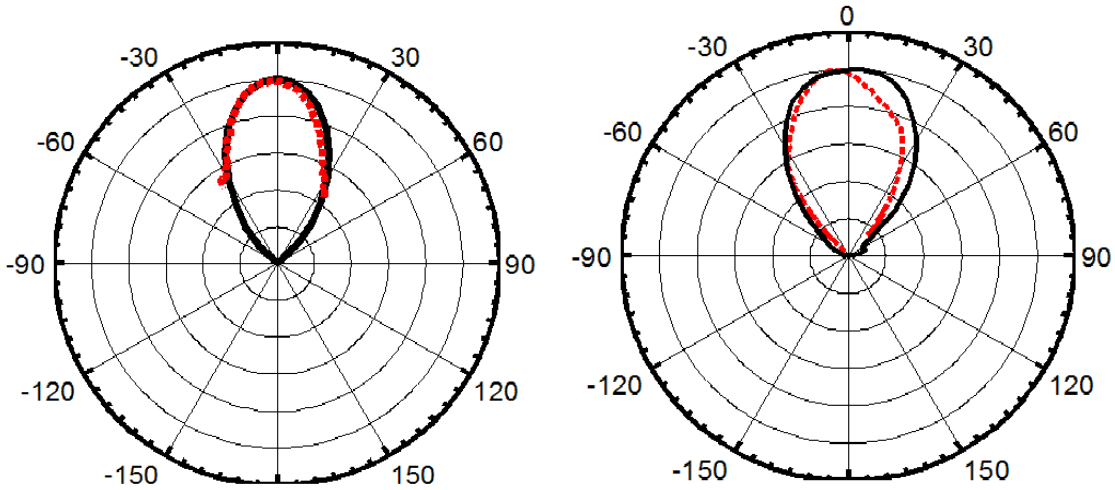


Figure 2.20. (a) Normalized H-plane co-polarization gain pattern (dB). (b) Normalized E-plane co-polarization gain pattern (dB). Black represents pattern simulated in HFSS, red indicates the measured data.

constant of 8, and a magnetic and dielectric loss tangent of 0.125. These constants were derived from available data on the absorber from the manufacturer. The simulation of the fixture ground plane added 1 dB of broadside gain to previously simulated results, as well as slightly increasing directivity. The addition of the RF absorber to the simulation greatly reduce the sidelobes in the E-plane, and narrowed the antenna patterns by reducing reflected signal at low angles entering the sidelobes of the antenna pattern. The resimulated results are shown in Fig. 2.20a and b. Significantly better correlation is shown. The remaining discrepancy in the positive angle side of the H-plane pattern may be due to the copper tape used to shield the diode detector.

The calculation for antenna gain from a diode detector can be expressed with the following equation:

$$G_a = 20 \log \left(\frac{V_d}{V_s} \right) - P_d \tag{2.4}$$

Where G_a is antenna gain in dB, V_d is detected voltage, V_s is detector sensitivity and

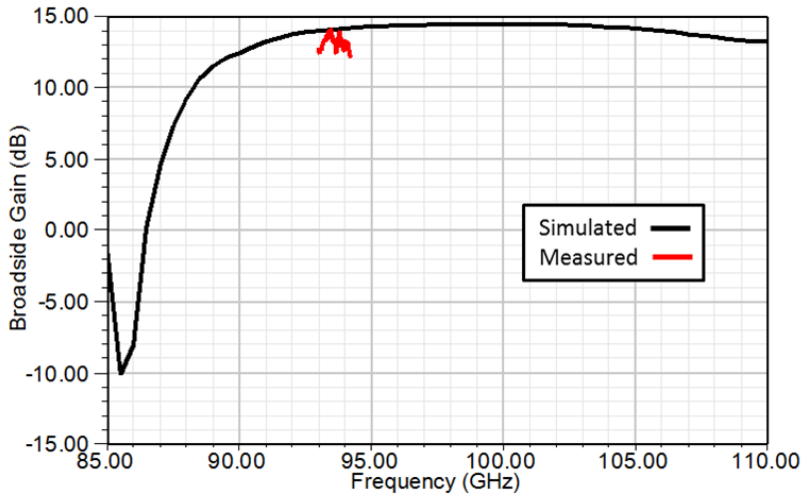


Figure 2.21. Simulated and measured broadside gain vs. frequency

P_d is the detected power normalized to the input of the detector in dB. A standard W-band waveguide horn and an off-the-shelf Millitech diode detector were used to determine the P_d for the test setup. The Millitech detector had a measured sensitivity of 2200 mV/mW at 94 GHz. The measured voltage from the Millitech diode detector was 17.55 mV. This correlates to a detected power of -21 dBm at the input of the antenna. The standard waveguide horn has a gain of 24 dB, thus the broadside received power at the Millitech diode detector (P_d) was measured to be -45 dBm.

The custom antenna detector diode had a voltage output of 1.07 mV at broadside. Based on the measured voltage sensitivity at 94 GHz shown in Fig 2.16b, this correlates to 717 μW (-31.45 dBm). Using the previously calculated P_d value and Eq. A.1, the measured broadside gain (G_a) for the antenna array at 94 GHz is 13.55 dB, which is close to the simulated gain of 13 dB. Figure 2.18 shows a plot of measured gain at broadside vs. frequency, as well as simulated results.

2.8 Conclusions

A Polystrata antenna and an array of antennas have been designed and tested. The antenna is a cavity backed patch antenna with an integrated feed. Return loss measurements of 32 dB at 94 GHz with a GSG probe are demonstrated for a single antenna. The antenna array is measured via rectacoax transition to waveguide and an integrated diode detector. A return loss of 18 dB is measured with the waveguide structure. Co-pol antenna patterns and a gain of 13.5 dB are measured with the integrated diode detector, and match well with simulated results.

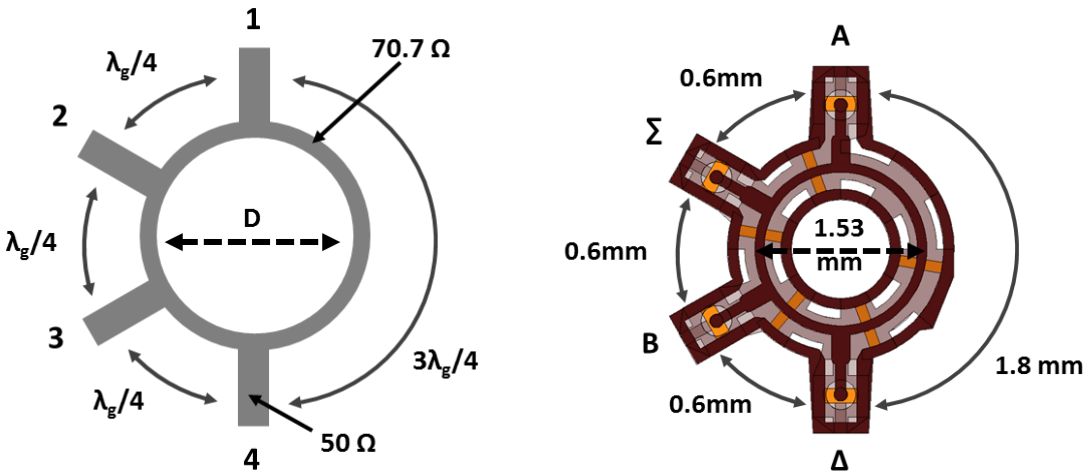
Future extensions of this antenna work include the creation of larger arrays for use in electronically-scanned phased arrays. These antennas are also intended to be directly integrated with a variety of circuits, specifically passive and active monopulse comparator circuits, which will be described in the coming chapters.

Chapter 3

Rectangular coaxial 3-D Passive Monopulse Comparator Network

One of the most common techniques for generating monopulse tracking patterns is a processing network utilizing passive transmission line components, such as hybrid combiners, to synthesize the addition and subtraction operations at the RF frequency range, as discussed in Section 1.3. While such solutions are cost-effective, they are typically narrow-band and tend to introduce significant loss at millimeter-wave frequencies. Such loss can be reduced relative to traditional transmission line technologies through the use of the Polystrata platform while also significantly increasing compactness through 3-D topologies.

This chapter will outline the design, fabrication and measurement of a rectangular-coaxial-based 3-D passive monopulse comparator network based on 180° rat-race hybrid combiners.



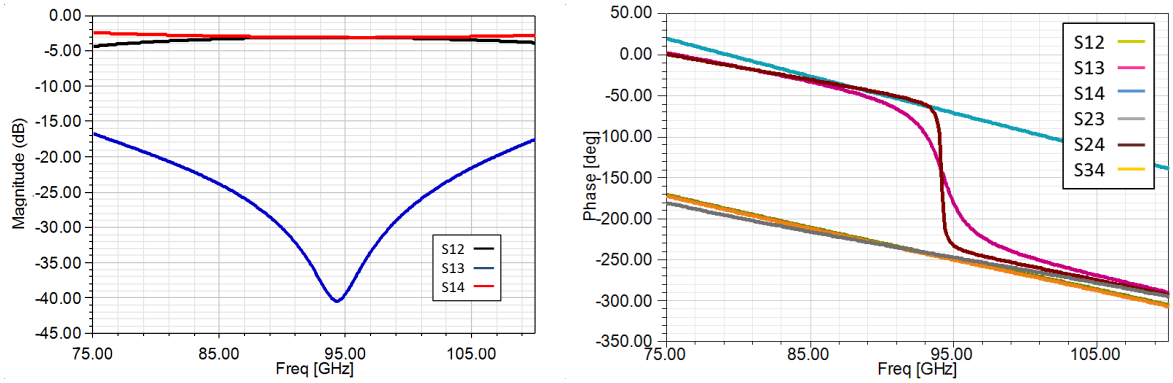
(a) (b)

Figure 3.1. (a) Standard microstrip rat-race hybrid combiner. (b) Top-down cross-section view of Polystrata rat-race hybrid centered about 94 GHz for inputs at ports A and B. The Σ port provides an in-phase combined signal, and the Δ provides a 180° out-of-phase combined signal.

3.1 Rectangular Coaxial Rat-Race Hybrid Combiners

A 180° hybrid is a microwave component that consists of a $1.5\lambda_g$ ring of transmission line connected with ports at $\frac{\lambda_g}{4}$ intervals on one side of the structure. A generic microstrip layout is shown in Figure 3.1a. The coupler can be used in two different modes: as a power combiner and as an in-phase or out out-of-phase power divider. When combining two input signals at Ports 1 and 3, port 2 yields an in phase combination of the two signals. Meanwhile, port 4 yields a combination of the signal at Port 3 and a 180°-shifted signal from Port 1, which results in the subtraction of the two signals. In the divider case, an input signal at Port 3 and a termination at Port 1 provides two in-phase signals at Ports 2 and 4. Terminating Port 3 and an input signal at Port 1 provides two 180° out-of-phase signals at Ports 2 and 4.

The Polystrata rat-race hybrid for the monopulse comparator network is designed at a center frequency of 94 GHz. The design of such a component using the Polystrata process



(a) (b)

Figure 3.2. (a) Simulated frequency response of a W-band Polystrata rat-race hybrid (b) Simulated phase response of a W-band Polystrata rat-race hybrid Port numbers from Figure 3.1

is not fundamentally different from design using microstrip. The basic structure of the Polystrata combiner is shown in Figure 3.1b. For rectangular coaxial structures, which have an air dielectric, $\lambda_g = \lambda_0$. The ring is constructed of 70.7 Ω impedance rectangular coax of similar construction to that found in Figure 2.3a. The ring has a centerline diameter (D) of 1.53 mm is intersected at 60° intervals by 50 Ω rectacoax ports. The 50 Ω rectacoax inputs have center conductors with dimensions 175 μm x 100 μm. The center conductor of 70.7 Ω rectacoax ring has dimensions of 88 μm by 100 μm. The inner dimensions of the outer conductor are 400 μm x 300 μm for the entire system. Each segment in the center ring is 600 μm long.

A simulated frequency sweep of the rat-race performance is shown in Figure 3.2. Simulations are performed using Ansoft HFSS FEM software, in combination with Ansoft Designer circuit simulator. The optimized impedance match occurs around 94 GHz. When utilizing ports 1 and 3 as inputs, port 2 yields the sum of the signals 1 and 3, while port 4 yields the difference of 1 and 3. In terms of S-parameters, the magnitudes of S13 and S14 should be about -3 dB, while S13 should be minimized at the frequency of interest.

Figure 3.3 shows the deviation from the expected phase over frequency. For the in-phase response, this is deviation from a phase difference of 0°; for out-of-phase, it is deviation from

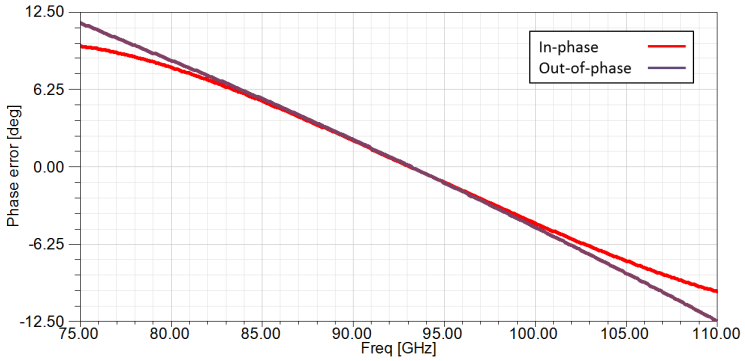


Figure 3.3. Phase error between output ports for rat-race hybrid. For the In-phase response, this is deviation from a phase difference of 0°; for out-of-phase, it is deviation from 180° phase difference.

180° phase difference. This phase error is a result of the electrical length of the transmission lines deviating from $\frac{\lambda_g}{4}$ as frequency moves farther away from the design frequency.

3.2 Monopulse Comparator Design

In the actual Polystrata implementation, two rat-race hybrids are laid out adjacent to one another, and the other two hybrids are fabricated on top of the first two. Figure 3.4 shows a 3-D model of the comparator network. This implementation highlights the dense routing capabilities of the Polystrata process, and fully utilizes all available layers. This configuration also minimizes the length of the interconnections between the hybrids. The interconnection length is 1.57 mm.

Essentially, the monopulse network compares differences in angle of arrival at each of the antenna elements. Since the angle of arrival at all of the antennas is identical at boresight, the output of the subtraction operations will be very close to zero. Small changes in angle away from boresight result in large variations in signal output for a difference pattern. This is turn increases the angular accuracy, which is important for tracking systems. This performance is simulated by varying the phase at pairs of inputs relative to the other inputs. To simulate a signal sweeping across an antenna array in an azimuthal direction the inputs A and D are

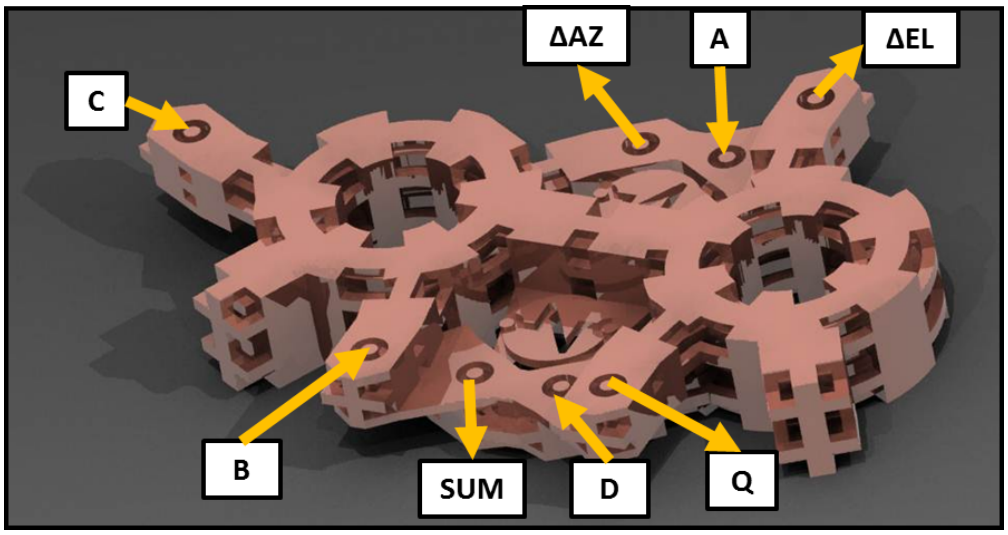
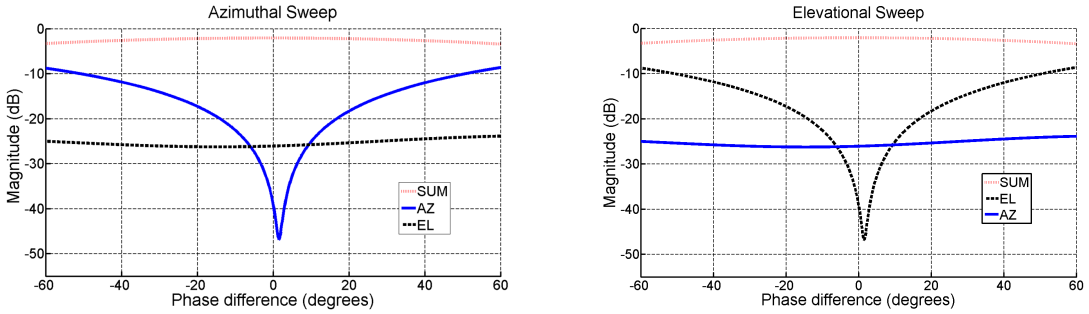


Figure 3.4. An HFSS 3-D model of a probe-able monopulse comparator network. Footprint of network is 6 x 3 mm



(a) (b)

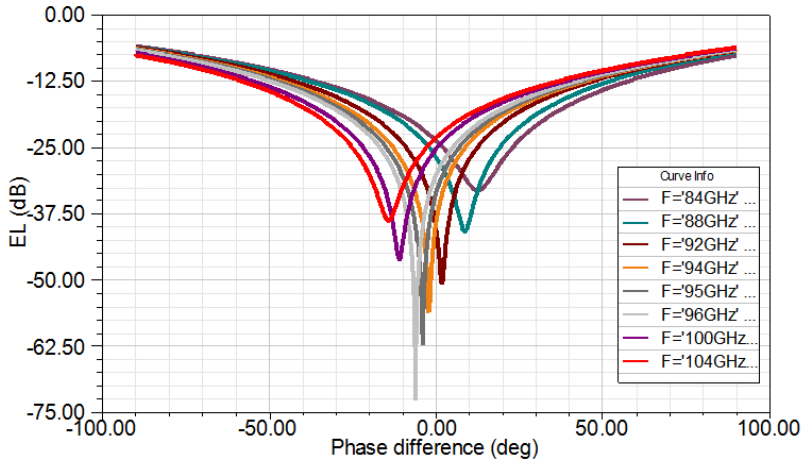
Figure 3.5. (a) Simulation of EL sweep of monopulse comparator network at 93.5 GHz, simulated by sweeping the phase of inputs A and D vs inputs B and C. (b) Simulation of EL sweep of monopulse comparator network at 93.5 GHz, simulated by sweeping the phase of inputs A and B vs inputs C and D.

set equal and swept in phase relative to the inputs B and C. The output at the azimuth difference port (ΔAZ) is (B+C)-(A+D). Simulation results of this sweep are shown in Figure 3.5a. The ΔAZ null is simulated to be 44.6 dB relative to boresight value of the SUM output. The SUM output port provides the combination of all four inputs (A+B+C+D). The SUM output provides range data, replicating traditional radar. The SUM channel has a simulated insertion loss of 2 dB at boresight.

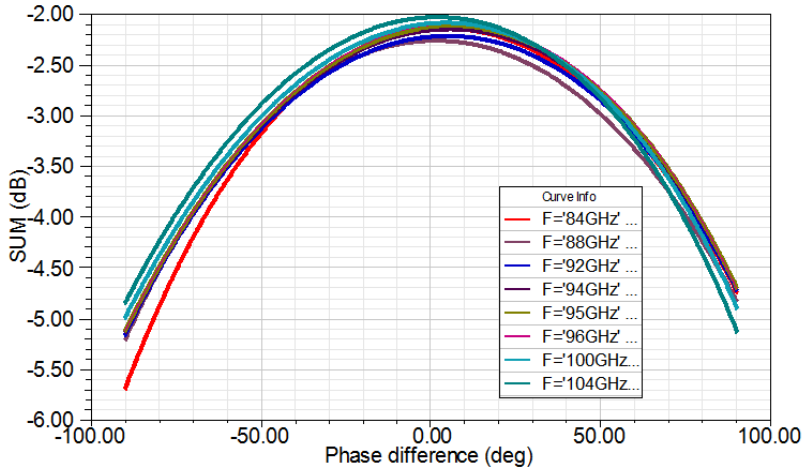
To simulate the signal source sweep in an elevational direction, the inputs A and B are set equal, and swept relative to the C and D inputs. The elevation difference port (ΔEL) is (C+D)-(A+B). The simulation results for this sweep are shown in Figure 3.5b. The ΔEL null is 44.4 dB relative to boresight value of the SUM output. The ΔAZ is also shown during the sweep, and displays the low-level expected when the signal source is held at the zero point in the azimuth plane. Interconnections between the rat race hybrids are designed to be equal in distance, so as not to introduce phase error into the addition and subtraction operations.

Figure 3.6a shows simulated ΔEL patterns at selected frequencies while sweeping in an elevational plane. The maximum null in the ΔEL pattern actually occurs at 96 GHz, but with a phase difference at the minima of 6.2°. This translates to a boresight offset of 1.2°. The simulated results are translated from phase difference ($\Delta\phi$) at the input ports to angle of arrival (θ) at the antenna via the expression $\Delta\phi = \text{kd}\cos(\theta)$, where d is .6875$\lambda$. ΔEL nulls of 30 dB or greater are demonstrated from 84 to 104 GHz, but the center points of the ΔEL nulls at those frequencies are shifted by 8° and 15° phase difference (1.9° and 2.8° boresight phase error). Aside from shifting the angular point of the maxima, little change is shown in the SUM output when swept over frequency in an elevational direction (Figure 3.6). Similar results from the SUM output were shown when sweeping in an azimuthal direction.

When sweeping in an azimuthal direction over frequency, some interesting variation in ΔAZ is observed, as shown in Fig. 3.7a. The maximum null occurs at 98 GHz, and much less shift in center angle is shown for 99-100 GHz. 30 dB or better nulls are simulated from 94-100 GHz. When the ΔEL output is observed during the sweep in the azimuthal direction (Fig. 3.7b), it has its minima at 94 GHz. A plot of null depth vs. frequency for the ΔEL and ΔAZ outputs (swept on their respective axes) is shown in Fig. 3.8. The variation in null depth over frequency is an indicator of the usable bandwidth of the system, as long as boresight angular error can be accounted for. Variations over frequency are a result of the phase error over frequency, as shown in Fig. 3.3. As signals from multiple rat-races are combined, the phase errors compound.



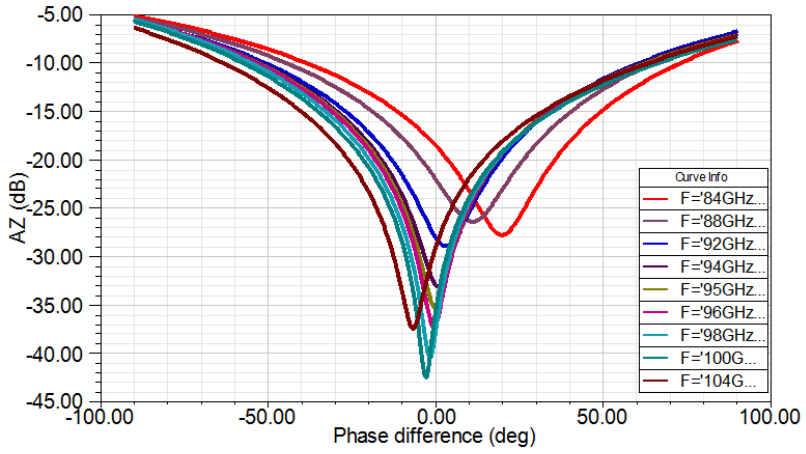
(a)



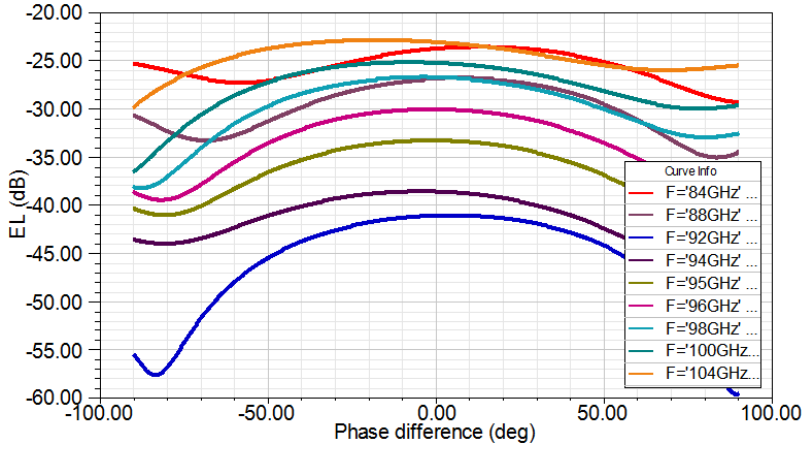
(b)

Figure 3.6. (a) Simulation of EL, sweeping inputs to monopulse comparator network, in elevation at a variety of selected frequencies versus the phase difference at the inputs to the monopulse comparator network. Maximum null occurs at 95 GHz. (b) Simulation of SUM, sweeping inputs to monopulse comparator network in elevation at a variety of selected frequencies versus the phase difference at the inputs to the monopulse comparator network.

The comparator structure shown in Fig. 3.4 is probe-able; however, the logistics of positioning 8 W-band probes are such that direct probe measurement of this structure is not possible at the time of this work. Therefore, to facilitate characterization of the comparator network, it was monolithically integrated with an antenna array and diode detectors.



(a)



(b)

Figure 3.7. (a) Simulation of ΔAZ, sweeping inputs to monopulse comparator network in azimuth at a variety of selected frequencies versus the phase difference at the inputs to the monopulse comparator network. Maximum null is at 99 GHz. (b) Simulation of ΔEL, sweeping inputs to monopulse comparator network in azimuth at a variety of selected frequencies versus the phase difference at the inputs to the monopulse comparator network.

3.3 Integration of Comparator with Antenna Array and Detector Diodes

The monopulse comparator network shown above in Figure 3.4 is integrated with an array of four cavity-backed patch antennas, shown in Figure 3.9. The performance of these antennas and array has previously been reported in Chapter 2. Each antenna is matched to an input

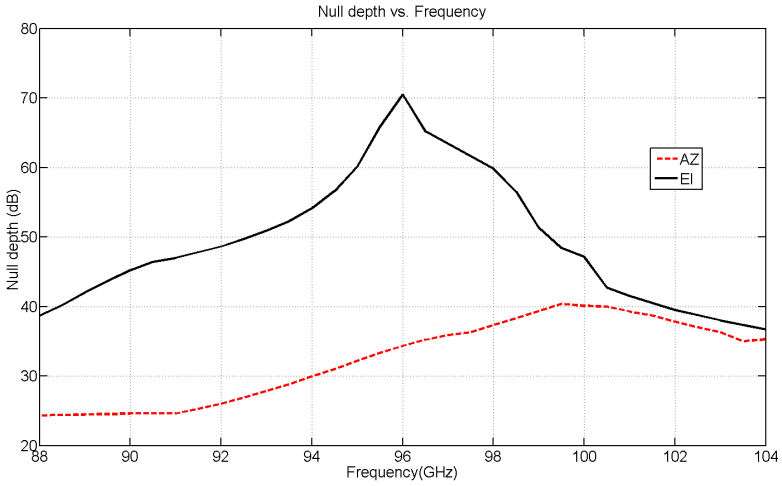


Figure 3.8. Plot of null depth vs. frequency for ΔEL and ΔAZ signals

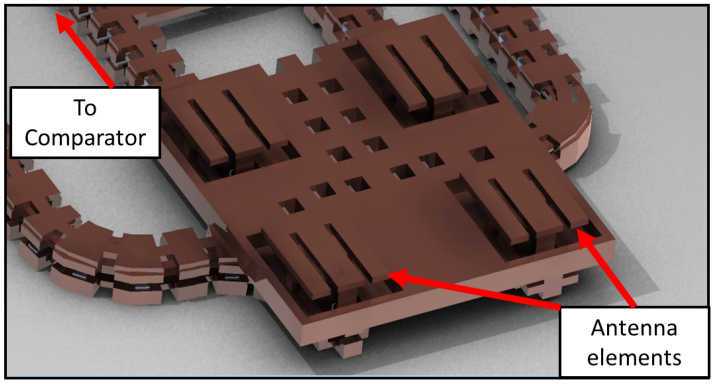


Figure 3.9. Array of four cavity-backed patch antennas fabricated in Polystrata. Each antenna feeds an input to the comparator network.

of the monopulse comparator network. The antenna spacing is $0.6875\lambda_0$.

To simplify measurement, detector diodes are used to convert W-band signals at the outputs to DC levels corresponding to power levels. The diodes used are Aeroflex/Metelics zero-bias GaAs beam-lead diodes, which have a voltage sensitivity of 0.5 $\frac{mV}{\mu W}$. The diodes are directly mounted in line on the Polystrata center conductors in a receiving socket and followed by a stepped impedance filter, as previously discussed in Chapter 2. The filter is terminated in a pad designed to receive a discrete wire. The outer conductor of the coax is

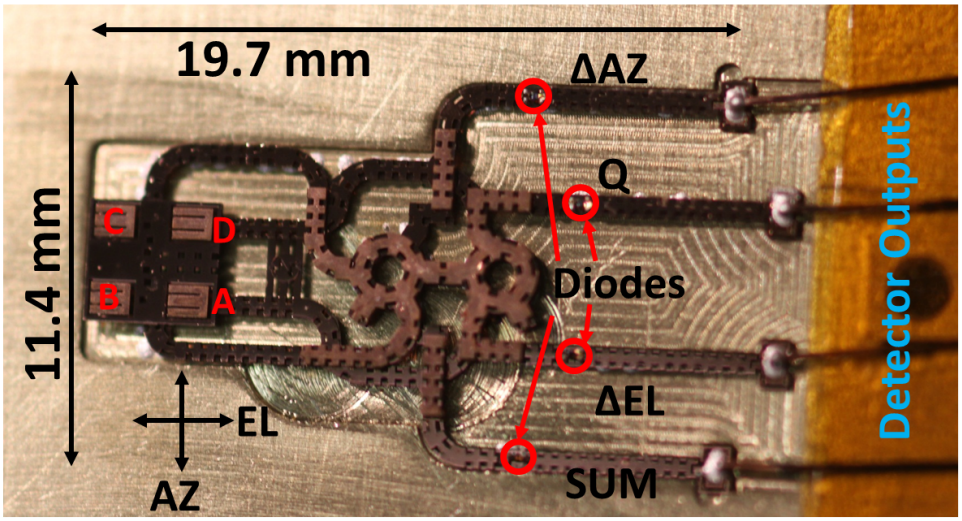


Figure 3.10. Fabricated monopulse receiver attached to baseplate with diodes assembled.

removed underneath to prevent shorting the wire assembly pad to ground when pressure is applied in the wire assembly process. A large number of dielectric straps provide additional support for wire assembly pad.

Assembly of the discrete diodes is performed using H20E conductive epoxy. The epoxy has a cure temperature of 150° C, performed under a nitrogen blanket to prevent corrosion. After the comparator and array is passivated using electroless nickel - gold, the diodes are hand-assembled into the sockets with the epoxy, and the entire network is attached to a brass baseplate. The baseplate has an indentation in the shape of the comparator network to assure alignment of the antenna array to the center of the baseplate. AWG 30 magnet wire is attached to the bondpads using H20E conductive epoxy. A 1-2 foot length of wire is left attached for ease of measurement. The fully assembled monopulse receiver is shown in Figure 3.10. The total dimensions of the Polystrata part fit in a 19.7 x 11.4 mm footprint. This footprint can be further reduced in future revisions of the component.

3.4 Measurements and Results

Measurements were performed at NIST in Boulder, CO using the same setup described in Section 2.6. A frequency multiplier is used to provide the 94 GHz signal. A circular waveguide horn is attached to Agilent 83558A mm-wave source. The horn output signal is passed through a Gaussian lens, and through a horizontal polarizer to provide a plane wavefront. This provides a wide beam of uniform magnitude, and reduces the error due to misalignment of the antenna and beam. The monopulse receiver and baseplate are attached to the motorized positioner, which can be swept physically in azimuthal and elevational planes. Eccosorb absorber material is affixed to the baseplate around the antenna elements to reduce reflected signals into the antenna in non-boresight measurement angles. Initial measurements were distorted by transmitter signals rectifying directly at the diodes when exposed to the incident RF, so a small piece of copper tape was used to shield the exposed diodes from the input signal. The signal source is modulated with a 40 Hz signal, which is phase locked to the multimeter to provide better resolution for output voltages. Output voltages are in the linear region of the diode's response curve as shown in Figure 2.16, and are converted to dB power levels directly, using the equation

$$P = 20log_{10}(V_d) \tag{3.1}$$

where V_d is the output voltage of the diode.

Measured sum and difference signals are presented in Figure 3.11 and Figure 3.12. In addition to de-embedding the antenna pattern, measured results are normalized to the maximum of the SUM output in the simulated results. The simulated results shown in Figure 3.5 have been translated from phase difference ($\Delta\phi$) at the input ports to angle of arrival (θ) at the antenna via the expression: $\Delta\phi$ = kd cos(θ), where d is .6875λ. The results shown in Figure 3.11 show a sweep in the azimuthal plane. A ΔAZ null of 31.4 dB relative to the SUM output is measured. The null depth is degraded by the angular resolution of the

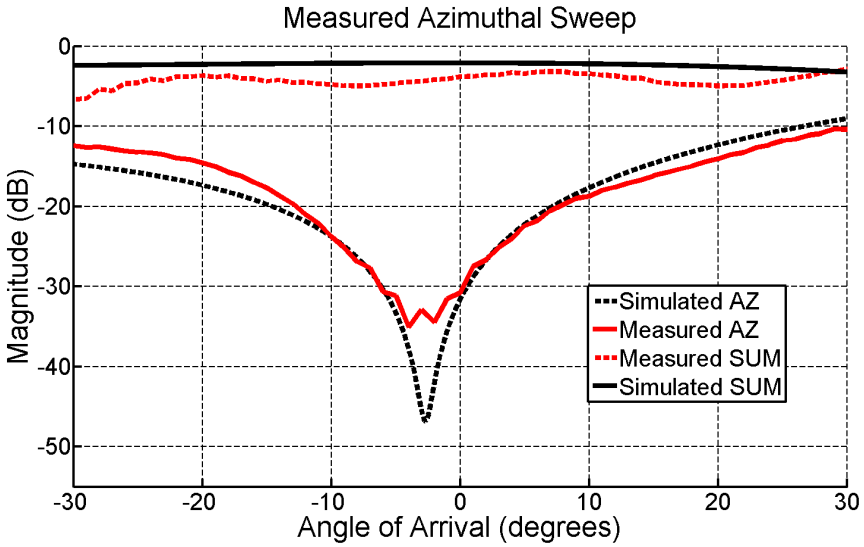


Figure 3.11. Measured results for a mechanical sweep in the azimuthal plane

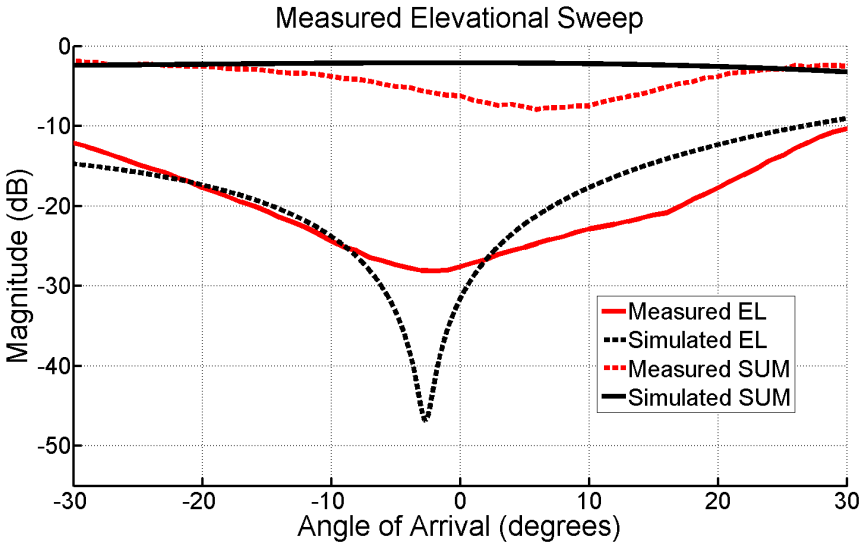
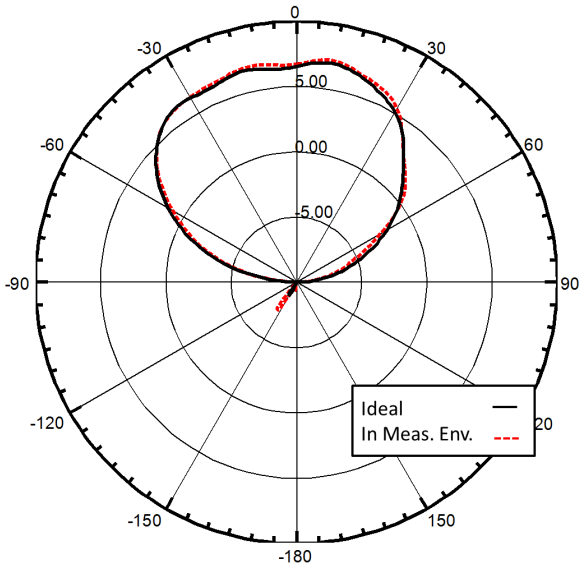


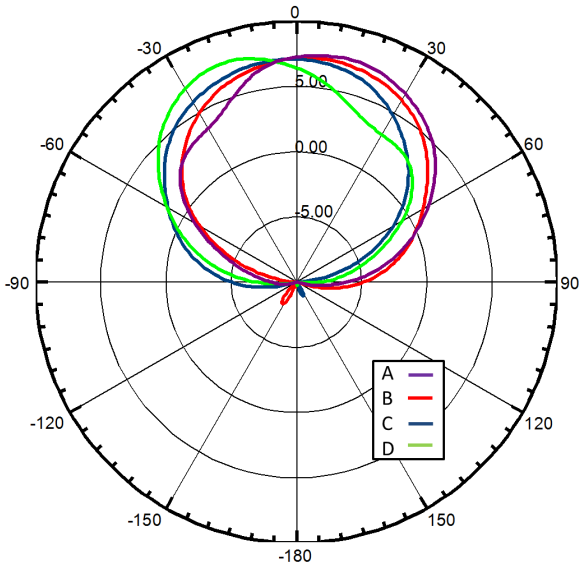
Figure 3.12. Measured results for a mechanical sweep in the elevational plane

measurement and the dynamic range of the diode detector, as well as angular misalignment.

The results shown in Figure 3.12 show a sweep in the elevational plane. A ΔEL null of 22.5 dB relative to the SUM output is measured. The ΔAZ output for the elevational sweep and the ΔEL output for the azimuthal sweep were below the minimum detectable level for the diodes, and are not shown here.



(a)



(b)

Figure 3.13. (a) Previously simulated "ideal" azimuthal antenna pattern vs. pattern simulated in measurement environment. This includes the physical comparator structure, which is planar with the antennas, as well as the mounting fixture and absorber material. (b) Simulated individual elevational pattern of antennas in measurement environment. The antennas are labelled in Figure 3.10.

One potential explanation for the distortion in the sum and difference patterns in the elevational sweep is distortion of the antenna element patterns from the hitherto unsimulated aspects of the measurement environment. One major contributor to this distortion is the physical structure of the comparator network and it's associated routing to the antennas. The comparator network is at the same heght as the antennas in the elevation plane. Since the comparator structure is located out of the azimuth plane, it causes no distortion in the azimuthal antenna patterns, as shown in Figure 3.13a. The "ideal" azimuthal antenna pattern (the antenna simulated by itself) compared with the antenna simulated with the nearby comparator structure shows little discrepancy, and all antennas exhibit an identical pattern. However, the simulation of each antenna's elevational pattern in the presence of the comparator structure shows significant variance from element to element, as shown in Figure 3.13b. The labels A-D correspond to the individual antenna elements shown in Figure 3.10.

Further simulation of the feed network also indicated an additional phase error of 2° in the C and B antenna paths relative to the A and D antenna paths. This phase discrepancy does not impact the azimuthal pattern. However, while the inclusion of this phase error and the antenna pattern discrepancies does slightly change the slope, depth and angular location of the elevational difference pattern, it does not account for the distortions shown in Fig. 3.12. These errors likely result from variance between detector diodes, or an assembly issue or fabrication issue with the specific network tested.

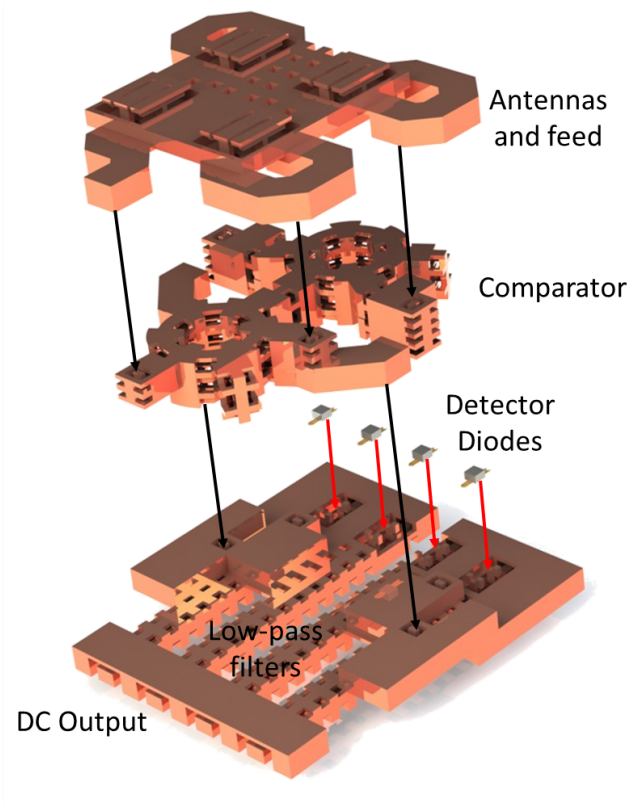
3.5 Summary

A passive monopulse comparator network based on PolyStrata rat-race combiners was designed and tested. The comparator network is integrated with PolyStrata antennas and diode detectors to simplify the pattern measurements. Measurements were performed, showing good correlation with simulated data. Ultimately, the depth of the measured monopulse null was limited by the noise floor of the detector diode. It may be possible to measure a

deeper monopulse null in a measurement system with more output power. However, the availability of such a system at W-band was limited at the time of this work.

Ultimately, a much more compact 94 GHz passive monopulse receiver is realizable using a PolyStrata platform. One approach to create a significantly more compact receiver is the hybrid assembly of a PolyStrata antenna array on top of the monopulse comparator network, as shown in 3.14. This concept drawing shows the hybrid assembly of three PolyStrata pieces. The first layer contains the antenna and feed network, including phase matching for the antenna paths. The middle layer contains the monopulse comparator network. The final layer includes the diode sockets, which would receive hybridly integrated beam-lead diodes for detection, the output low-pass filters, and the DC outputs. In this design, the DC outputs are intended to be directly connectorized, or assembled to a PCB board. Additional mechanical supports would be necessary for assembly, but are omitted from the drawing for clarity. The overall footprint of the conceptual design in 3.14 is 6.2 x 6.9 x 2.5 mm. Compared to the 11.4 x 19.7 x .85 mm system presented in this chapter, the conceptual compact monopulse receiver represents a volumetric reduction of greater than 2x (96.1 mm^3 versus 190.9 mm^3).

A passive monopulse comparator network based on rat-race couplers is inherently narrow band, however. Additionally a passive system may suffer from high insertion loss and ultimately be limited in its performance. Alternative architectures are available to increase the bandwidth of the system. One such approach, an active monopulse comparator MMIC, will be examined in Chapters 4 and 5.



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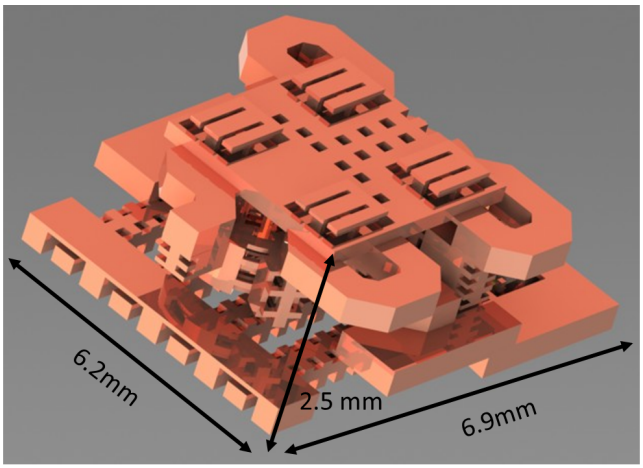


(b)

Figure 3.14. (a) Exploded drawing of a conceptual compact passive monopulse receiver. Three layers of PolyStrata passive devices and four detector diodes are used in its assembly. (b) Assembled conceptual compact monopulse receiver. The total footprint is 6.2 x 6.9 x 2.5 mm.

Chapter 4

A W-band SiGe Active Monopulse Comparator

An alternative to implementing passive monopulse comparator techniques is the development of MMIC active monopulse comparators. Active monopulse comparators have the potential for wideband operation, as well as the ability to provide gain to the signal. IC monopulse comparators may also have RF front-end and baseband signal processing capabilities integrated. In the past, active monopulse systems were limited in RF frequency by the available MMIC technologies. Therefore, mm-wave monopulse systems have been developed with integrated antennas and monopulse processing at an IF frequency [27] [28]. However, advances in IC technology over the past decade have made it practical to perform monopulse comparator operation at the RF frequency range, dramatically reducing system size. [96] represents an early implementation of an active monopulse comparator architecture at 2 GHz. Another approach (demonstrated in [97] at 5-6 GHz) integrates active devices with traditional ring-hybrid comparator techniques. An RF CMOS implementation at 24 GHz is demonstrated in [98]; a block diagram of that architecture is shown in Figure 4.1.

This chapter extends the architecture proposed in [98] to W-band frequencies, specifically, a 20 GHz band centered about 94 GHz. The monopulse comparator circuitry presented here

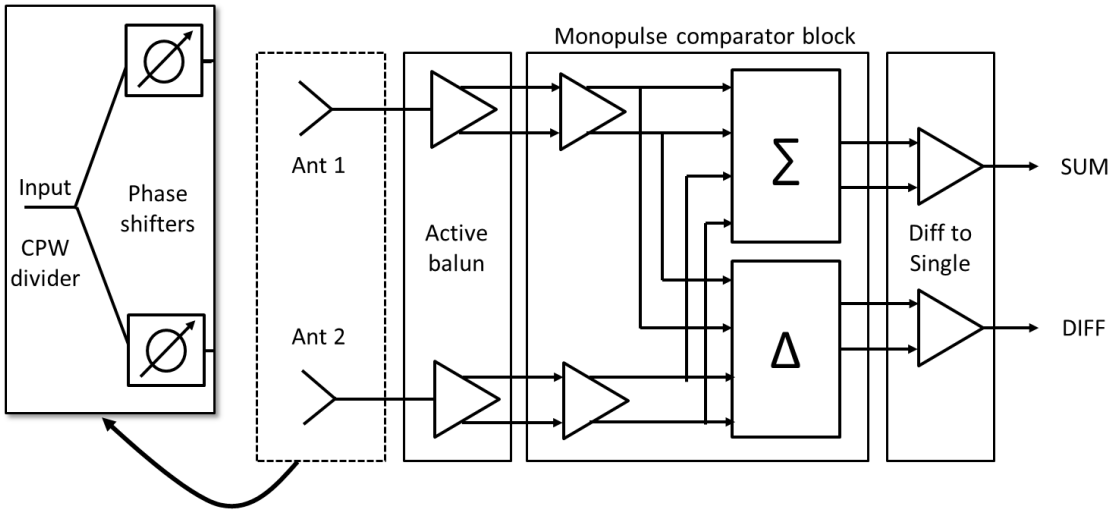


Figure 4.1. Block diagram of an active IC-based architecture for a monopulse comparator. Inset: Replacement for antennas in block diagram to facilitate testing on-chip. Single RF input is divided in CPW and with independently controlled phase in each branch

is a two-port implementation, providing tracking information in only one plane, but can be straightforwardly extended to a 4-port design. Two versions of the chip were designed and fabricated: a two input version (for ultimate integration with Polystrata antennas), and a version with a single RF input that is split into two branches with integrated voltage-controlled phase shifters, to facilitate probe measurement (as shown in Fig. 4.1 inset). This chapter will discuss the design, layout and measurement approaches for this W-band monopulse comparator.

4.1 Active Comparator Circuit Blocks

From Fig. 4.1, it can be seen that the majority of the circuitry in the design is differential. This is required for the difference (Δ) operation, but also has the added benefit of reducing the susceptibility of the circuits to common mode noise and improving second order linearity performance. However, the IC implementation has single-ended RF inputs and outputs which must be converted with active baluns to differential paths on-chip, given the lack

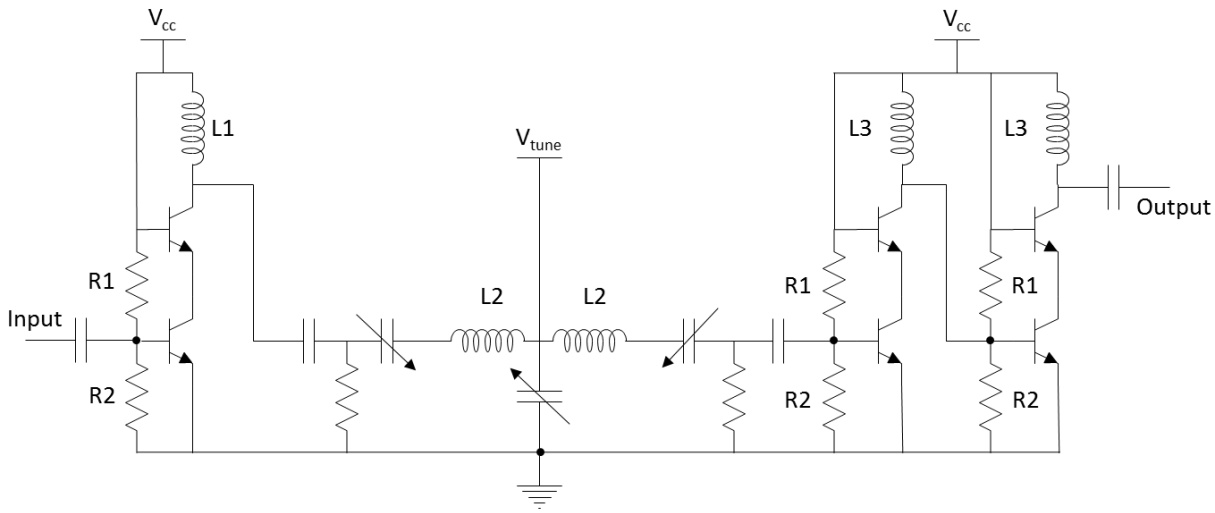


Figure 4.2. Design for phase shifter based on a tunable LCL matching network. Gain stages are provided to the input and output to mitigate insertion loss

Table 4.1. Phase shifter component values

Resistors		Inductors	
R1	2.3kΩ	L1	277pH
R2	2.8kΩ	L2	500pH
R3	10kΩ	L3	191pH

of availability of differential W-band probes. A more integrated system would not require these stages in favor of differential downconverting mixers and/or differential antennas. This section will discuss the design of each of the sections outlined in the block diagram. The chip is designed in IBM 8HP 130 nm SiGe BiCMOS technology. Unless otherwise noted, the supply voltage is 1.5 V, and capacitors are 400 fF. This value was chosen because it is the minimum area capacitor allowed in the 8HP process. Emitter widths are 120 nm unless otherwise noted, for maximum f_T.

4.1.1 Phase shifters

To facilitate on-chip testing, a simple voltage controlled phase shifter was implemented in each input path branch after the splitter. This provides for a relative phase shift between

the two input paths, simulating the effect of a scattering target moving across the detection plane. The circuit is based on the work in [99], and is shown in Fig. 4.2.

The core of the phase shifter consists of an LCL tuning network. The shunt capacitor is a varactor, and each inductor (L2) also has a varactor in series with it. The varactor in series with a fixed inductor creates a tunable inductance. Two types of varactor are available in the IBM 8HP process: a hyperabrupt (HA) junction diode varactor and a diode-connected NMOS varactor. The hyperabrupt junction diode varactor is selected for its higher Q factor and wider tuning range. These varactors have a tuning range of 32 fF to 84 fF. Resistor R3 provides a resistive path to ground to allow a DC voltage drop across each varactor. However, it is also of a sufficiently high resistance (10kΩ) to act effectively as an RF choke. By changing V_{tune}, a linear shift in phase is achieved.

The L2 inductors are custom-designed, and are shown in Figure 4.3a. The inductor is a U-shaped microstrip in the 4 μm thick top metal available in the 8HP process. A ground shield in the bottom (M1) metal prevents feedthrough from the silicon substrate. The gap between the shield and the inductor is 12.6 μm. The signal line is 10 μm wide, and 320 μm in length. The simulated insertion loss of the inductor is 0.35 dB at 94 GHz, and the match is better than 15.5 dB from 75-100 GHz. The simulated inductance is shown in 4.3c. The inductance is 500 pH at 94 GHz, but varies across the W-band. The maxima in the inductance plot at 107 GHz and the "negative" inductance at higher frequencies is a result of the inductor reaching its self-resonant frequency. The self-resonant frequency is the frequency at which the shunt capacitance of the transmission line resonates with the inductor, and beyond that frequency, the capacitance begins to dominate the impedance. The "negative‘ inductance is a mathematical representation of the change in sign of the imaginary part of the impedance.

Cascode gain stages are added at both the input and output of the circuit, to mitigate some of the insertion loss due to the mismatch. At 94 GHz, the circuit provides a phase tuning range of 79°, and an amplitude tuning range from 0.8 dB to 3.2 dB (Fig. 4.4). The

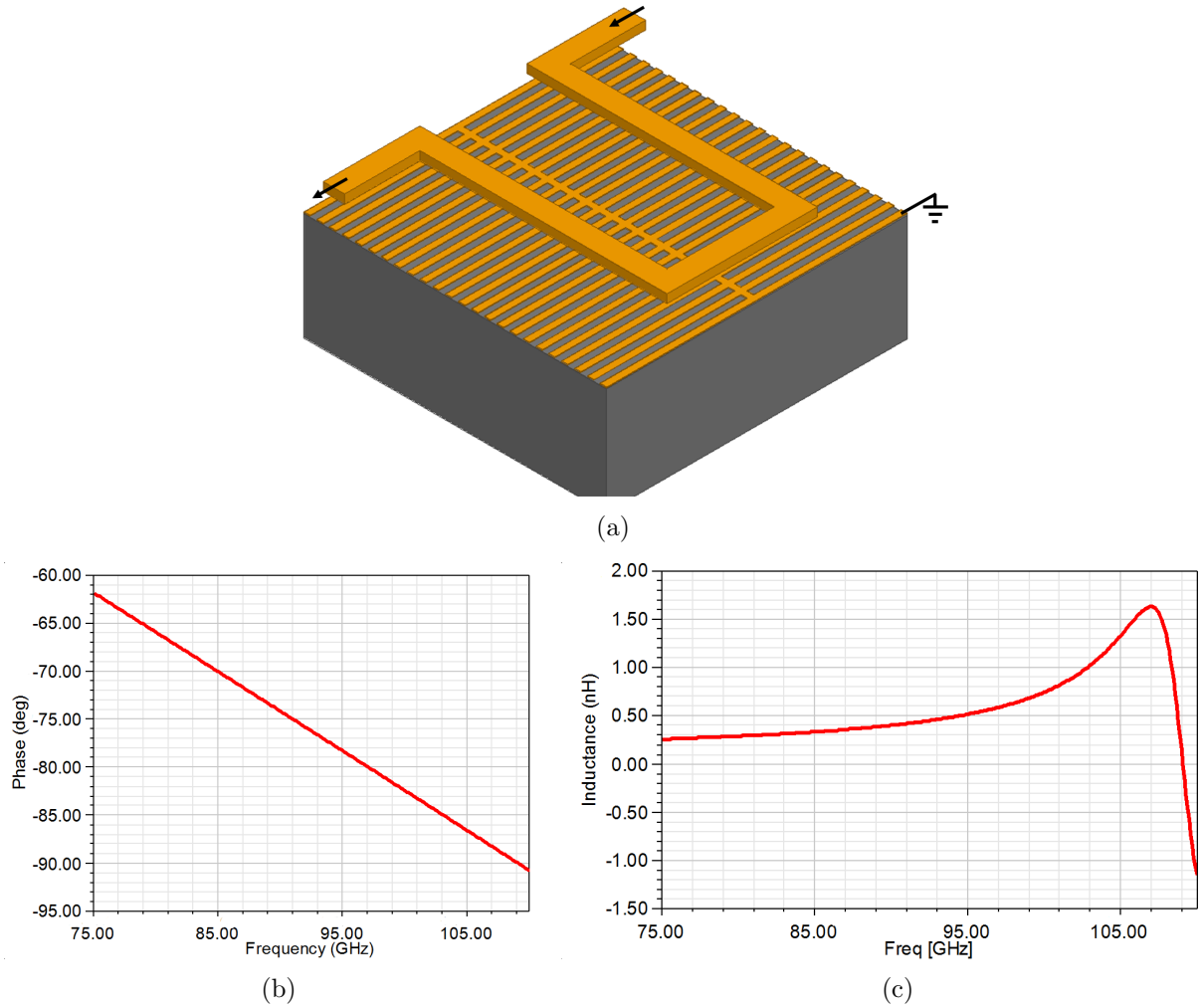


Figure 4.3. (a) 3-D custom inductor model (b) Simulated phase of custom inductor (c) Simulated inductance of custom microstrip inductor

angle of arrival (Θ) is calculated using the relationship $\Delta f = kd\cos(\Theta)$, where d is assumed to be 0.5λ, and Δf is the phase difference at the input ports. The simulated phase shifters give an equivalent angle of arrival range of $\pm 25°$. All simulations are performed using Cadence and the Virtuoso© Analog Design environment.

4.1.2 Active Balun

The first block after the phase shifters is the active balun (Fig. 4.5), which converts the single-ended RF inputs from each branch into differential outputs. The active balun design

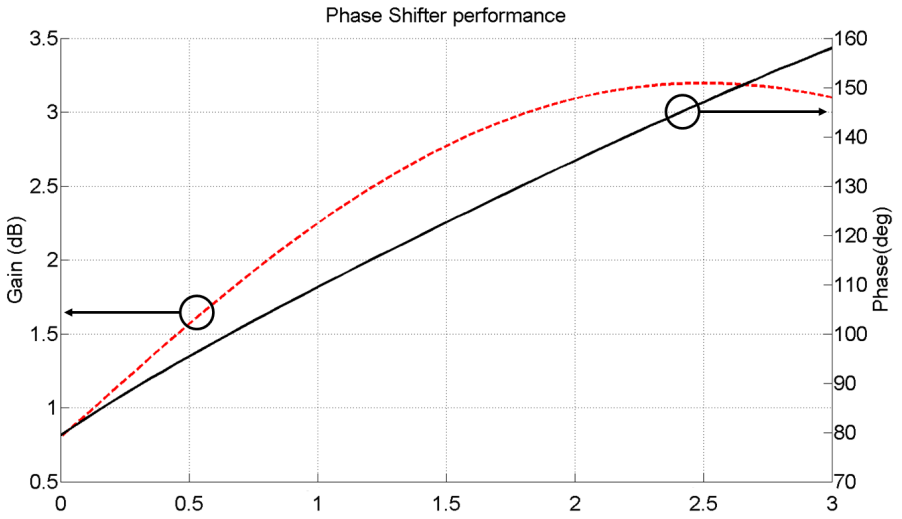


Figure 4.4. Simulated results for phase shifter at 94 GHz: 79° of phase tuning and 0.8 dB to 3.2 dB of amplitude tuning

Table 4.2. Active balun resistance values

Resistance			
R1	140kΩ	R5	23.5kΩ
R2	330Ω	R6	2.06kΩ
R3	14.8kΩ	R7	27.8kΩ
R4	100.8Ω	R8	220Ω

consists of a common-base amplifier and a common-source amplifier, fed from a common input. The common-base transistor (Q0) has an emitter length of 1 μm, and the common-emitter transistor (Q1) has an emitter length of 3 μm. These values, as well as the resistor bias values, are chosen to minimize the phase and amplitude imbalance between the two paths. The identical common-emitter amplifiers which follow in each path also help to mitigate the phase and amplitude imbalance, in addition to providing additional gain.

The common emitter amplifier and the common base amplifier are isolated at their inputs by a capacitor, to prevent loading and feedthrough. The lower values of resistance (R2, R4, R8) are able to be accurately reproduced using BEOL resistors available in the IBM 8HP process. Other resistors are created using the traditional base-diffused resistors. Resistive biasing was chosen over current source biasing based on headroom concerns.

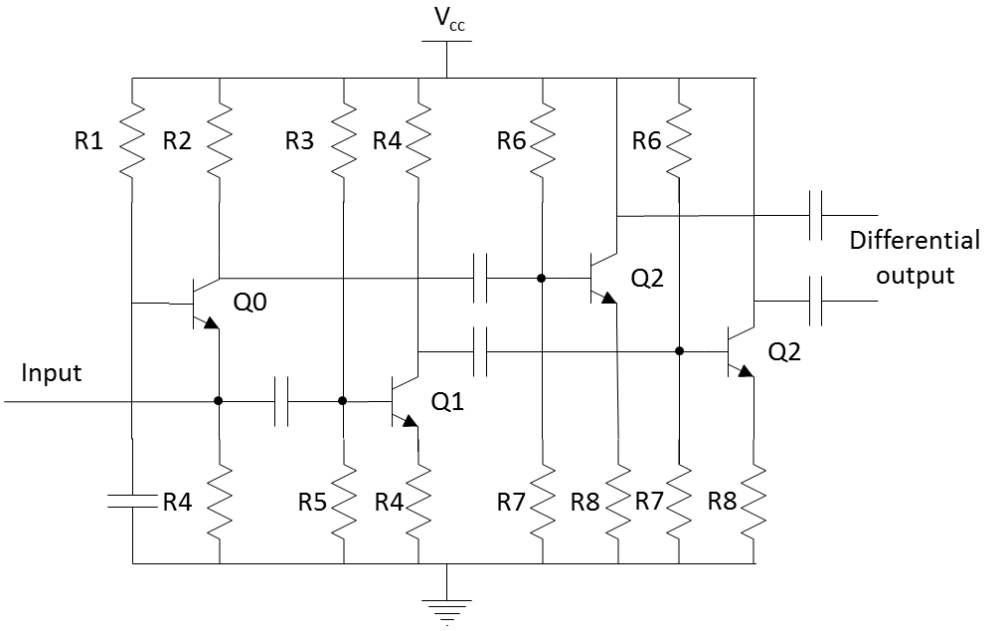


Figure 4.5. Circuit design of active balun for conversion of single-ended input to differential signal.

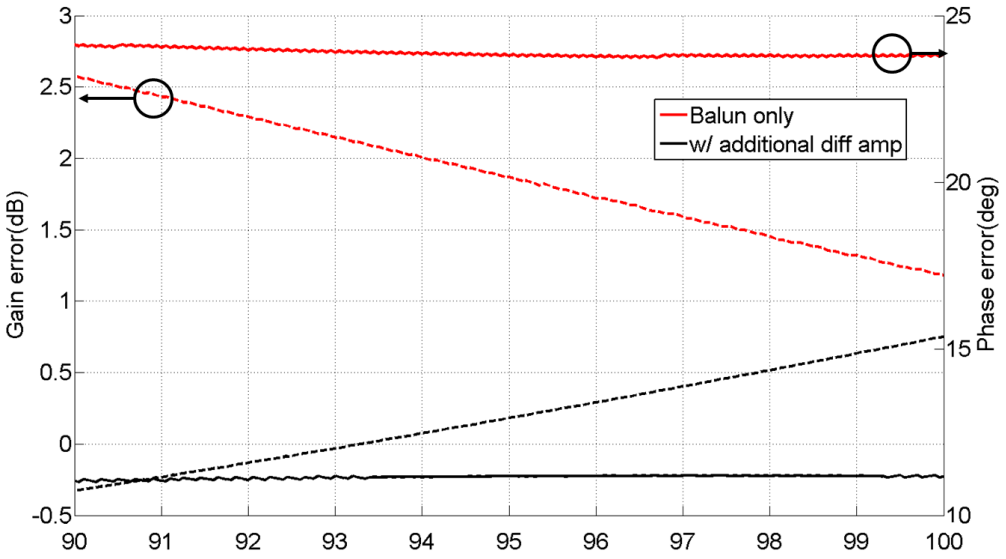


Figure 4.6. Amplitude and phase error in the balun. Red lines represent phase and amplitude error of just the balun itself, while black lines represent the error after the differential amp that follows

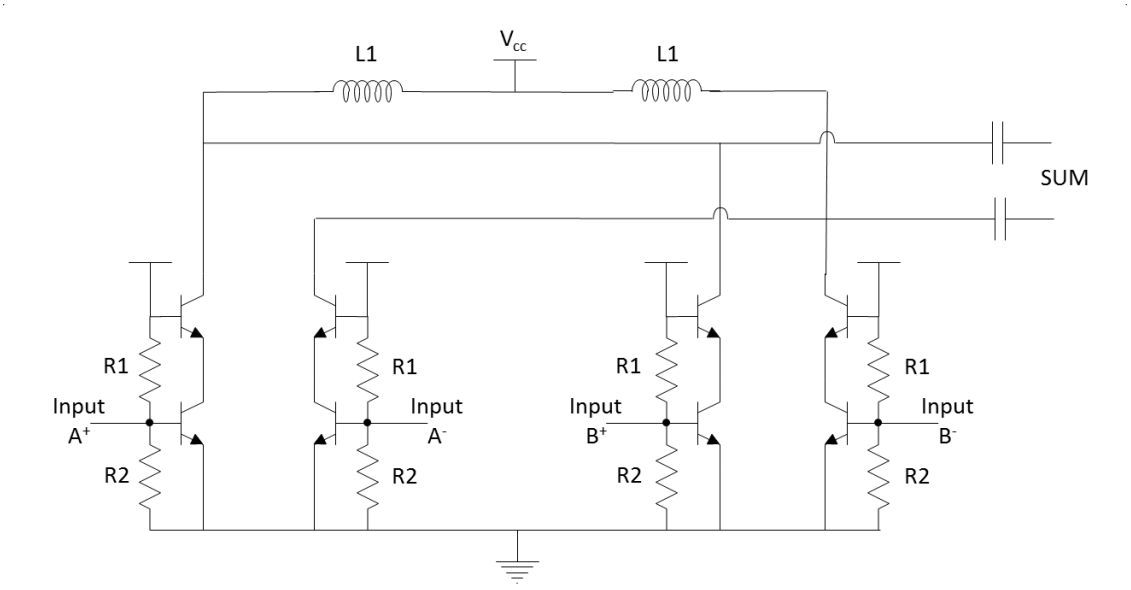


Figure 4.7. Cascode summing amplifier

Table 4.3. Summing and Difference amplifier component values

Resistors		Inductors	
R1	2.3kΩ	L1	277pH
R2	2.8kΩ		

At 94 GHz, the simulated phase deviation of the differential signal is 15°, and the simulated amplitude imbalance is 2.5 dB. The differential amplifier which follows the active balun block provides gain and mitigates the imbalance effects of the single-ended to differential conversion. From simulation, the phase and amplitude imbalances after this stage are essentially reduced to zero, particularly at 94 GHz. Simulation results can be seen in Fig. 4.6. The differential amplifier provides 4 dB of gain to the path with the greatest loss, which helps provide amplitude balance.

4.1.3 Summing and Difference Amplifiers

The summing (Σ) amplifier shown in Fig. 4.7 consists of two sets of cascoded amplifiers. All of the transistors have an emitter length of 12 μm. The two differential input signals

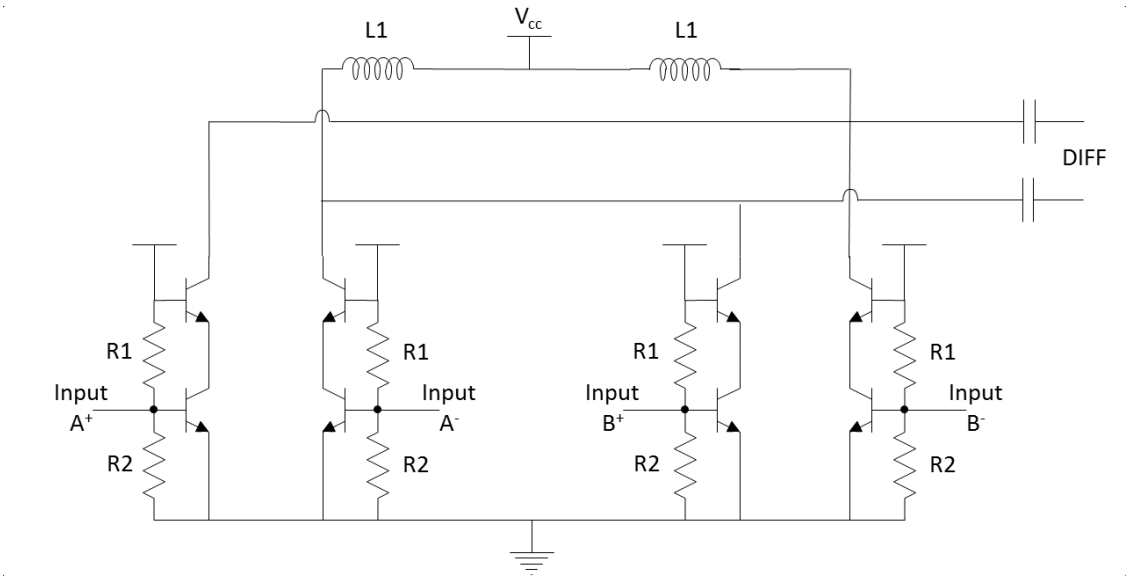


Figure 4.8. Cascode difference amplifier

Table 4.4. Differential to single ended conversion circuit resistance values

	Resistance		
R1	1.1kΩ	R3	6kΩ
R2	4.6kΩ		

(Input A and B) are added in phase. This generates the SUM output of the monopulse comparator. The summing amplifier has a gain of 2 dB at 94 GHz when input phases are identical, and introduces negligible phase or gain imbalance.

The difference (Δ) operation is performed using the difference amplifier shown in Fig. 4.8. The summing and difference amplifiers share the same component values, as shown in Table 4.3. This circuit is identical to the summing amplifier, except that the components of the two input differential signals are added out of phase. This provides a net subtraction operation, and generates the DIFF output of the comparator.

4.1.4 Differential to Single Ended Conversion

The final operation is the conversion back to single-ended signals for coupling off of the chip. This is achieved using a basic push-pull differential to single-ended conversion

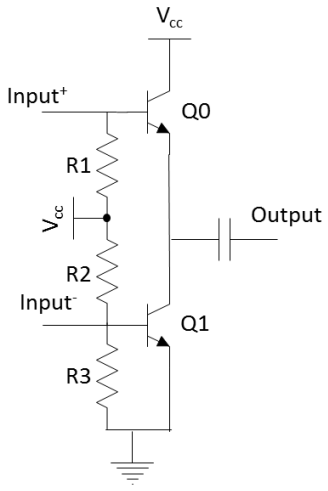


Figure 4.9. Differential to single ended conversion circuit. A push-pull technique is used to convert the differential signal to single-ended to couple the signal off-chip.

circuit, as shown in Figure 4.9. The component values for the circuit are shown in Table 4.4. The output signal is delivered to the pads via a CPW line designed using Sonnet, which is discussed in the following section.

4.2 Simulation and Layout

The simulated response for the entire monopulse comparator network at is shown at 94 GHz in Fig. 4.10. Simulations are done using Cadence Spectre simulation environment. The overall simulated gain in the SUM pattern at 94 GHz is -3.8 dB, and the monopulse null depth is 32.9 dB, referenced to the SUM pattern. The depth of the null is limited by device performance, and the loss associated with the SUM performance which is used to normalize the null depth. The phase performance of the system is also shown. The phase plot in Figure 4.10 is the relative phase between the sum and difference path. The phase transitions from positive to negative at boresight, and is used to determine which side of the null the output is located on in a control system.

Figure 4.11 shows a simulation of monopulse null depth vs. frequency, demonstrating the potential wideband nature of this IC. A null depth of better than 31.5 dB is simulated

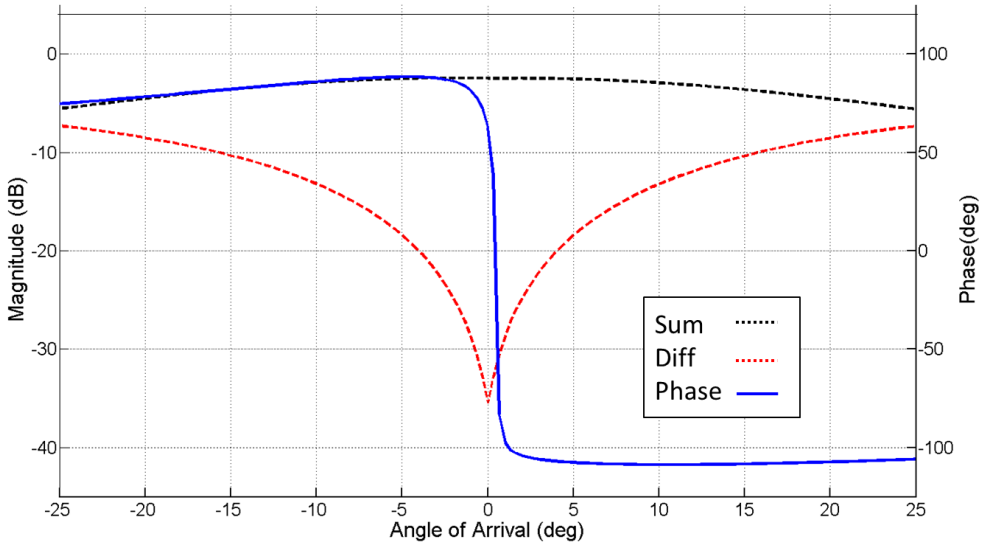


Figure 4.10. Simulated monopulse pattern at 94 GHz. A null depth of 32.9 dB is shown.

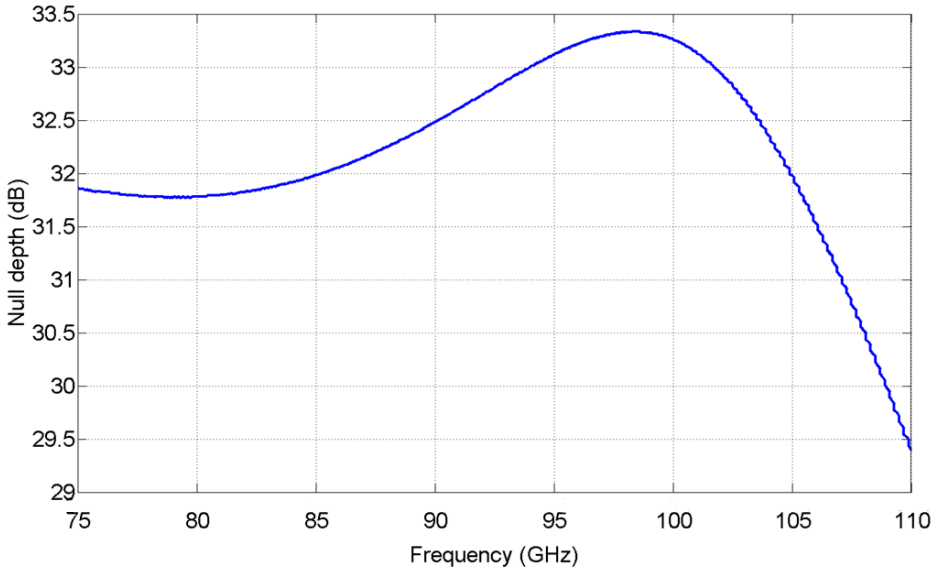


Figure 4.11. Monopulse null depth vs. frequency. Simulation does not take into account input and output CPW.

from 75-105 GHz. The performance of the circuit at higher frequencies is likely limited by the performance of available passive components. Many of the reactive components reach their self-resonating frequency around 110 GHz.

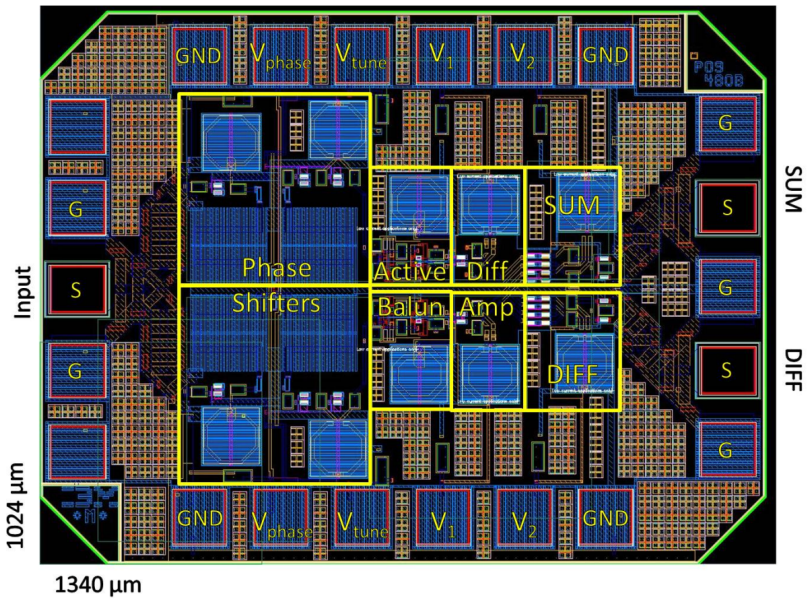
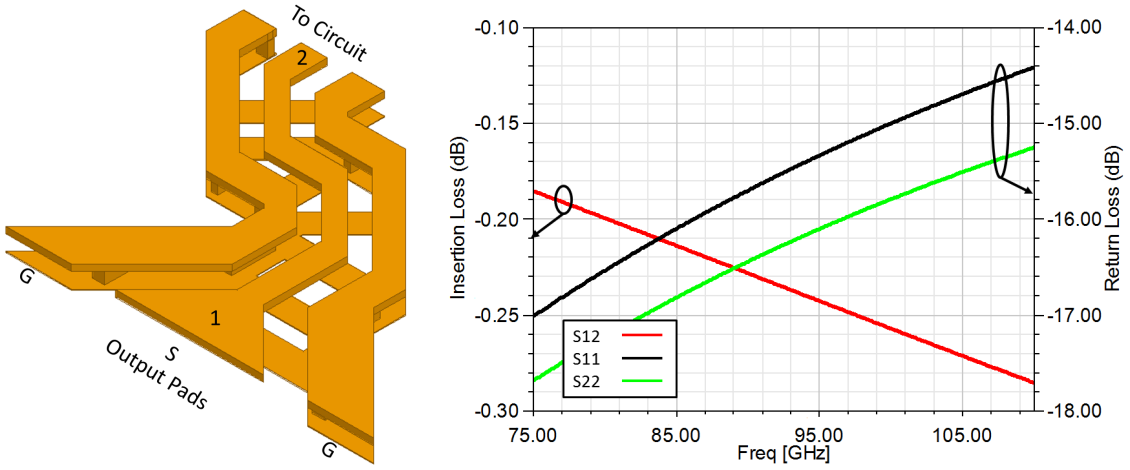


Figure 4.12. Cadence layout for monopulse comparator chip in IBM 8HP SiGe BiCMOS process. V_{phase} is V_{dd} for the phase shifter, V_{tune} is the control voltage for the phase shifter, V_1 is V_{dd} for the active balun and diff amp, and V_2 is V_{dd} for the remainder of the system.

The layout of the circuit is created using Cadence using the Virtuoso© Layout Editor and Assura DRC checking. Pads and inductors are the major contributors to die area. Two variations on the die were fabricated with different purposes in mind. The layout of ariation 1 can be seen in Fig. 4.12. The purpose of variation 1 was to be probed using the available GSG probes. As such, this variation has a single input which is split 1:2 and routed to the inputs of the phase shifters. The final dimensions of variation 1 are 1025 x 1340 μm, including pads. In addition to the input and output GSG RF pads, 8 DC pins and 4 ground pins are also included, with 6 pins along both the top and bottom of the chip. The spacing for both DC and RF pins is 150 μm pitch.

Custom CPW structures are used to route from the input and output of the active circuit to the GSG probe pads. The output routing for variation 1 is shown in fig 4.13a. The CPW lines are routed in the 4 μm thick aluminum top metal available in the 8 HP process. A ground shield, to allow DC routing in the lower metal layers is included in the third metal from the top (MQ), with vias connecting the ground lines in the top metal to the shield. The



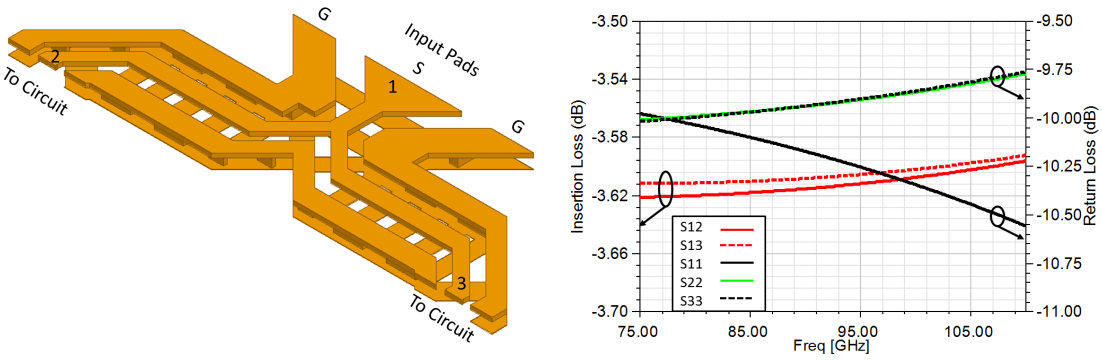
(a) (b)

Figure 4.13. (a) 3-D model of output CPW routing from active circuit to probe pads. Dielectric is not shown, for clarity. (b) Simulated performance of output CPW routing

shield is crosshatched underneath the signal line to reduce the per-unit-length capacitance of the signal line, while still acting as a shield. The gaps in the shield are less than 20 μm in width.

The width of the 50 Ω line is 16 μm, with 15 μm gaps between the center and outer conductors. The gap between the center conductor and the underlying ground shield is 9.25 μm, with a dielectric of silicon dioxide ($\epsilon_r = 4.1$). Since the ground shield gap is less than the edge gap, it is a significant contributor to the impedance of the line. Also included in the simulation is the tapering of the line to match the 150 μm pitch GSG probe pads. This approach was chosen rather than a step impedance change at the pads to minimize loading capacitance at the transitions. The final center conductor width is 90 μm, with gaps of 27 μm. The total length of CPW from the circuit to the pads is 200 μm. The performance of the CPW routing is shown in Figure 4.13b. The simulated insertion loss is 0.24 dB at 94 GHz, and less than 0.3 dB to 110 GHz. The input and output return losses are less than 14 dB.

Ideally, the divider from the GSG input to the inputs of the phase shifters would be a



(a) (b)

Figure 4.14. (a) 3-D model of input CPW splitter from active circuit to probe pads for MMIC Variation 1 (b) Simulated performance of input CPW splitter from active circuit to probe pads for MMIC Variation 1

reactive divider or a Wilkinson Divider, to provide isolation and improve matching. However, given the area available and the relatively short length of each path (260 μm, $\sim \frac{\lambda}{8}$), a simple 1:2 splitter with 50Ω line dimensions was simulated. Similar dimensions are used for the 50Ω center conductor as the output routing. Simulations of the divider show reasonable performance (Figure 4.13), return loss of less than 9 dB and insertion loss of less than 0.62 dB. Output isolation was a concern, but simulations indicated that this did not impact performance.

A second chip variant was fabricated with the intention of future integration with Polystrata antennas and to facilitate standalone measurement of the phase shifter circuits. Each phase shifter input is individually accessible via a set of GSG probe pads. Variation 2 (layout shown in Fig. 4.15) also includes pads at the output of the phase shifter as a means of measuring phase shifter performance. Due to the the lack of availability of W-band differential probes for the inputs, variant two is not able to be fully characterized without some sort of additional structures. The final dimensions for the variation 2 MMIC are 1025 x 1650 μm.

For the output routing of the active circuit to the pads for variant 2, identical routing to the ones shown in Figure 4.13 were used. Similar CPW was used for routing the individual inputs (see Figure 4.16). The total length of the input routing was 180 μm, and the simulated

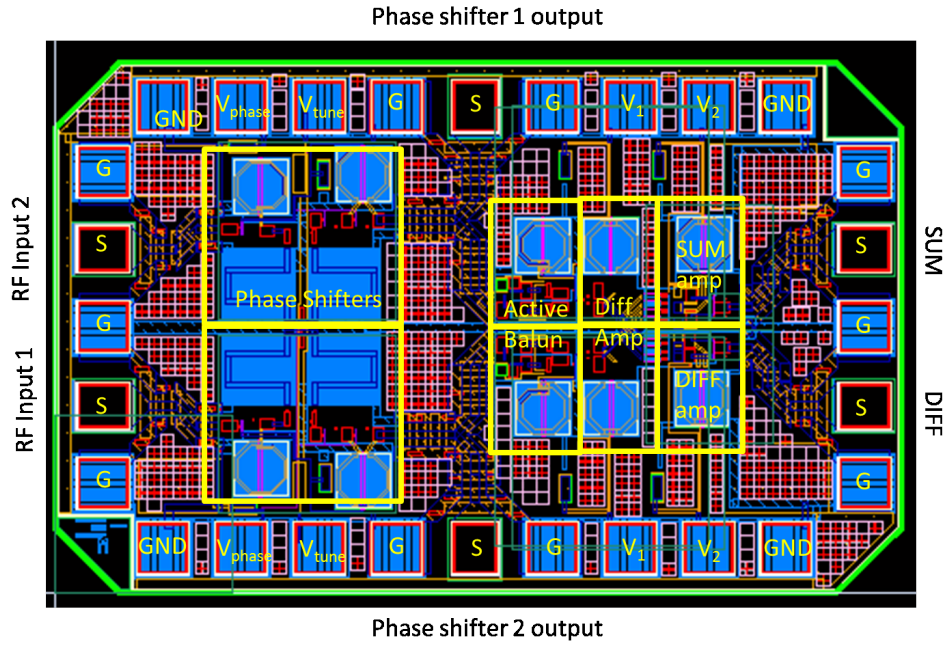
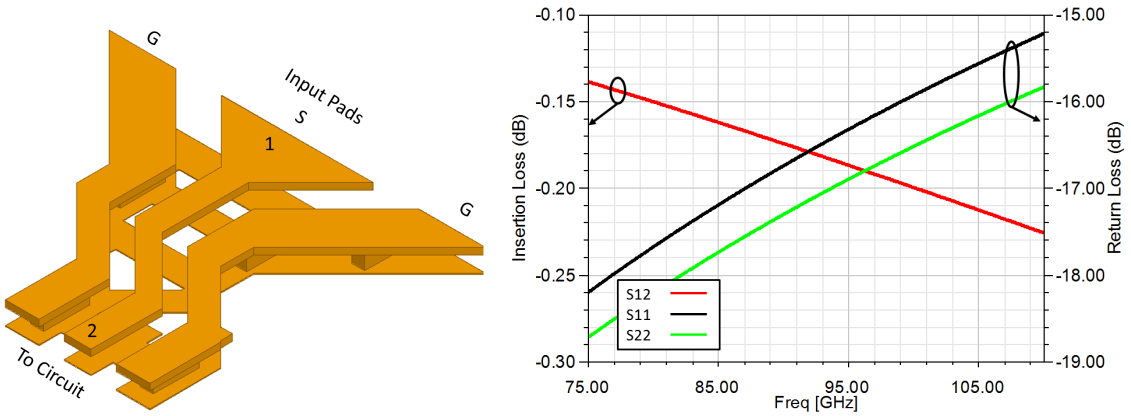


Figure 4.15. Cadence layout for monopulse comparator chip in IBM 8HP SiGe BiCMOS process, variation 2. DC signals are identical to Variation 1, with the addition of GSG probe pads for single phase shifter characterization. Total die area is 1650 x 1020 μm.



(a) (b)

Figure 4.16. (a) 3-D model of input CPW routing from active circuit to probe pads for MMIC Variation 2 (b) Simulated performance of input CPW routing from active circuit to probe pads for MMIC Variation 2

insertion loss and return loss were less than 0.22 dB and 15 dB, respectively.

The CPW routing for phase shifter characterization has two different cases for which

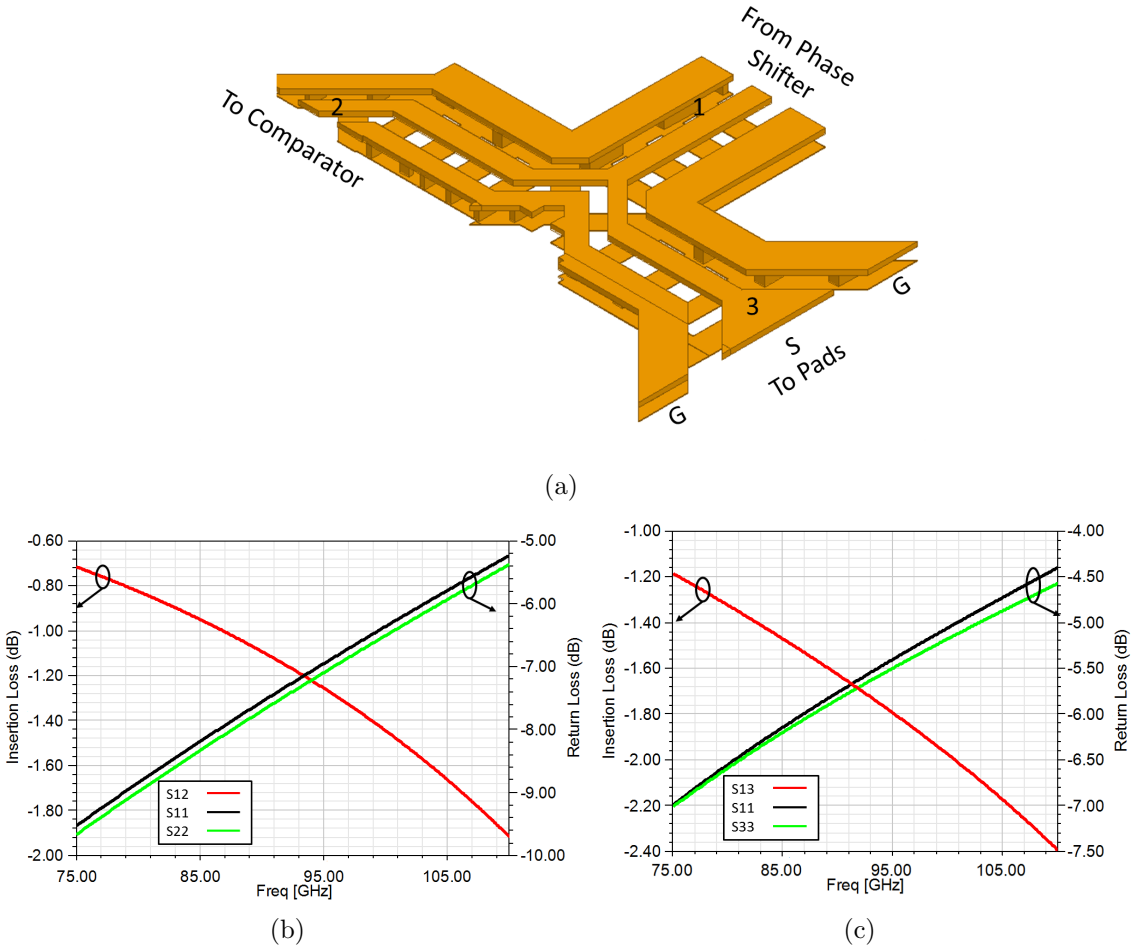


Figure 4.17. (a) 3-D model of CPW routing phase shifter to probe outputs and comparator circuitry for MMIC Variation 2 (b) Simulated performance of post-phase shifter CPW under normal operating conditions (1→2) (c) Simulated performance of post-phase shifter CPW for phase shifter probing (1→3).

it was simulated: normal circuit operation and probing of the phase shifter output. These simulations were done after the chip was fabricated due to time contraints in the design phase. At no point would both output ports be terminated simultaneously. The structure itself is shown in Figure 4.17a. For normal circuit operation (1→2), the routing appears as a 50Ω line with a 180 μm long open-circuit stub at 115 μm from the input to a 320 μm long line. This is quite detrimental to the overall performance of the network, as shown in Figure 4.17b. The simulated insertion loss is 1.2 dB at 94 GHz, and the return loss is 7 dB.

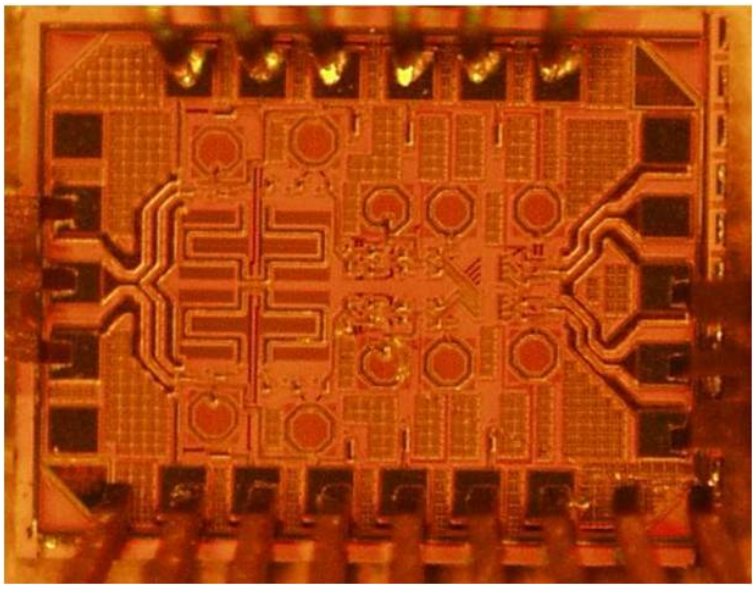


Figure 4.18. Fabricated variation one chip with probes down for measurement. The die area is 1024 x 1340 μm

Mismatch loss and potential radiation by the tapered end of the stub are contributors to this performance.

In the probing configuration (1→3), the network is modeled as a 295 μm long 50Ω line with a 205 μm capacitively loaded stub at 115 μm from the input. The capacitance is ∼ 5 fF, which is the series combination of the blocking capacitor and the BE capacitance of the NPN transistor which is connected to the line in its off-state. It is assumed that when the phase shifters are under test, the comparator circuit is not powered on. The simulated performance of the CPW under these conditions is shown in Figure 4.17c. The simulated insertion loss at 94 GHz is 1.8 dB, and the return loss is 5.5 dB.

4.3 Measurement and Test

Fabricated chips (Fig. 4.18) were mounted to a handling substrate using conductive epoxy. The devices were tested using a HP 8510C Vector Network Analyzer with HP 85105A mm-wave controller and W-band waveguide heads. From the waveguide, a transition to 1 mm

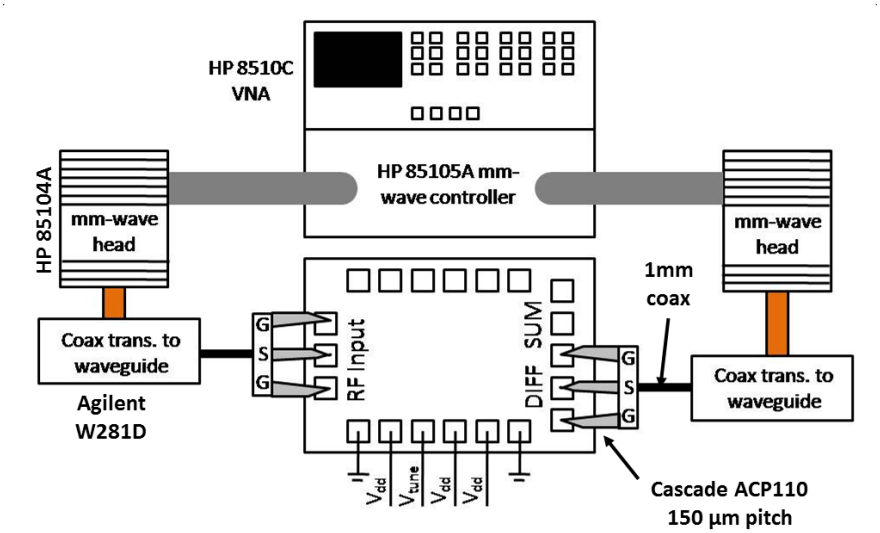


Figure 4.19. Test setup for monopulse comparator IC. DC voltages are mirrored top and bottom and are applied via six-pin DC probes

coaxial cable was used to connect to Cascade ACP110 GSG probes for the input and output signals. This measurement setup can be seen in Fig. 5.19. Only a single output (SUM or DIFF) can be measured at a time, due to lack of available GSGSG W-band probes. DC voltages are delivered to the chip via six-pin DC probes. For measurement, one phase shifter control voltage is held at 0V, while the other is swept.

Initial issues with achieving the expected quiescent point led to the discovery of a layout error which rendered variation one unmeasurable. The probe pad for V_{tune} on one path was not connected properly to the circuit, resulting in an inability to control the phase shifters. Measurements of the phase shifters were performed using the alternative output pads on Variant 2, and the results are shown in Figure 4.20. Measurement results did not match well with simulated results at several bias points. Measurement discrepancies are likely caused by insufficient decoupling capacitance on the bias control lines. Higher decoupling capacitance would prevent power supply noise or radiation from the chip from entering the DC bias lines. This noise can cause unwanted oscillations in the varactor values and active circuitry. Future measurements should include discrete decoupling capacitors as close to the chip as possible.

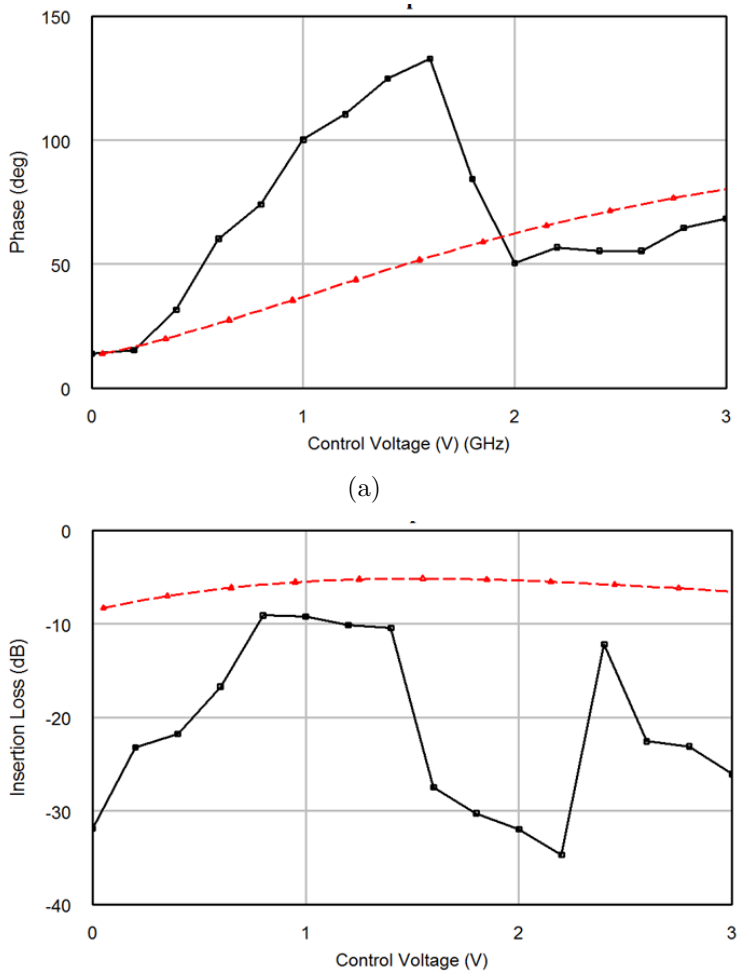


Figure 4.20. (a) Measured vs. simulated phase response for MMIC phase shifters(b) Measured vs. simulated magnitude response for MMIC phase shifters

4.4 Conclusions

A W-band active monopulse comparator circuit in IBM HP 130 nm SiGe BiCMOS technology was designed and laid out. Simulation results showed a 33 dB difference null and -4 dB insertion loss in the SUM pattern. Two variations of the chip were fabricated: variation 1, which is probeable via a GSG microwave probe, and variation 2, designed for integration with Polystrata antennas. Efforts to measure the variation 1 chip were unsuccessful due to a layout error. Measured results of the phase shifters alone showed discrepancies between

measured and simulated responses, believed to be due to insufficient decoupling capacitance on the DC bias lines.

This MMIC design functions as a proof of concept for W-band active monopulse comparator circuitry. Previously, the technology was not available to perform these operations at the frequency of interest. After measured results are acquired from future iterations of the MMIC, the addition of on-chip detectors, mixers and automatic gain control are the logical next step for this work. The addition of this functionality would enable the implementation of compact W-band radar systems for a variety of applications.

Chapter 5

A 24 GHz CMOS Active Monopulse Comparator

Mm-wave frequencies have traditionally been the domain of III-V semiconductors and more recentl, SiGe technology. However, in the last decade, Silicon CMOS technology has been aggressively scaled in an effort to meet demands for digital computing. As a result, the f_t and f_{max} of commercially available technologies has scaled to 300 GHz [100] [101]. In the last several years, a number of CMOS circuits in the mm-wave frequency range, even beyond 100 GHz, have been published [102] [103]. This research is often driven by the applications of automotive radar and mm-wave imaging, which require lower cost and lower power consumption, advantages afforded by CMOS technologies.

This chapter will discuss an RF-CMOS implementation of a 4-port active monopulse comparator RFIC at 24 GHz. In contrast with the work in Chapter 4, this chapter will extend the work in [98] to provide target locational information in both azimuth and elevation. The limited availability of discrete 94 GHz phase shifters and multi-probe heads capable of mm-wave frequencies were also a factor in implementing a proof-of-concept 4-port monopulse comparator system at 24 GHz instead of 94 GHz. A block diagram of the system is shown in Fig. 5.1. In the full system, each input is connected to an off-chip antenna or sub-array.

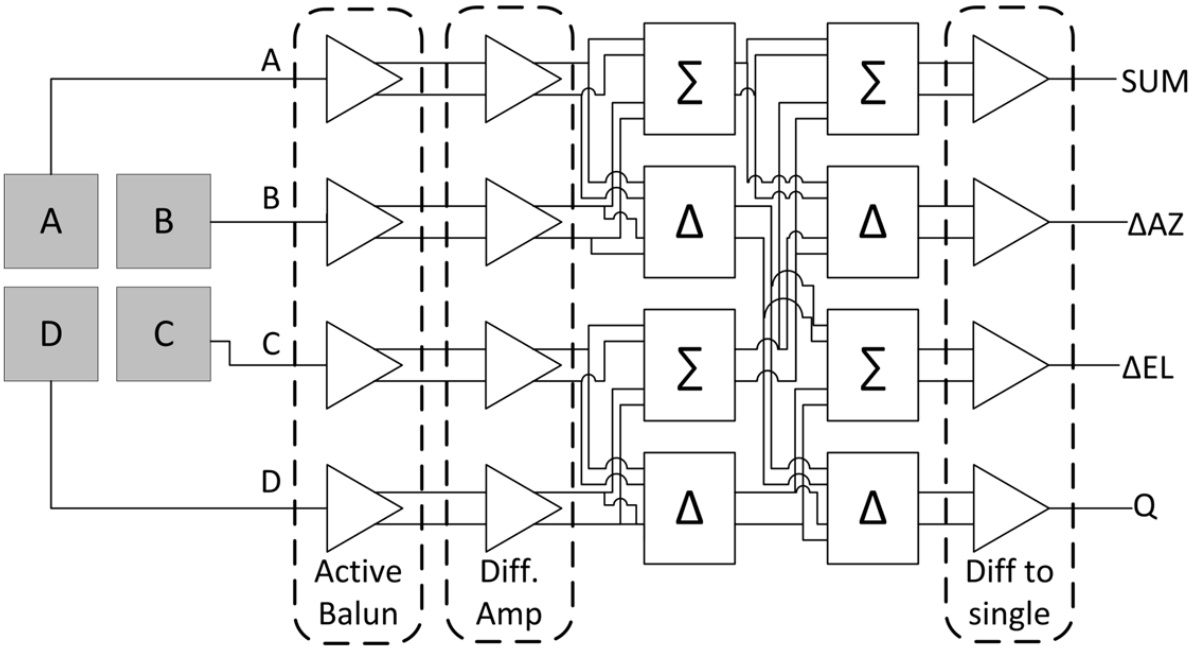


Figure 5.1. Block diagram of 4-port active monopulse comparator. Each antenna is connected to an input. The system consists of an active balun, differential amplifier, two layers of summing and difference amplifiers, and a differential to single-ended conversion circuit on the output.

For the RFIC implementation, these antennas are replaced ith 150 μm pitch GSG probe points. Each input signal (A-D) is then converted to a differential signal, via an active balun. Differential antennas would eliminate the need for this conversion.

After amplification, the signals are added and subtracted in the manner shown in Fig. 5.1. As in Chapter 3, 4 output signals are generated from the circuit. The SUM output is generated by the addition of all signals (A+B+C+D), and represents a traditional radar return signal, which is used to generate range information. The ΔAZ signal is is the subtraction of two half-array sums ((A+B)-(C+D)) and provides locational information in the azimuth direction. The ΔEL signal is is the addition of two half-array subtractions ((A-B)+(C-D)) and provides locational information in the elevation direction. Q ((A-B)-(C-D)) is often used as an error term for calibration purposes. After the output signals are generated, the differential signals are converted back to single-ended signals for measurement. Again, in a fully integrated system, differential mixers could eliminate the need for this final

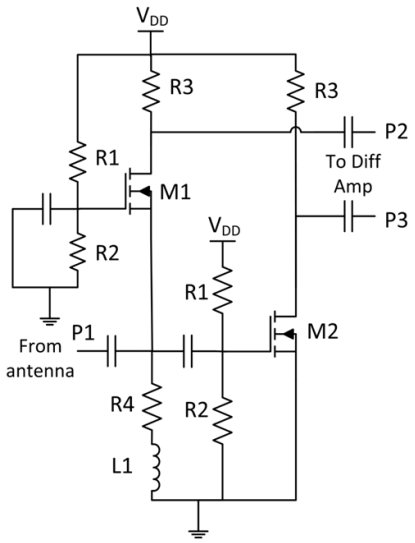


Figure 5.2. Active Balun circuit diagram. Circuit uses a parallel common-gate and common-drain amplifiers to change a single-ended signal to a differential signal. Transistor gate widths are 25 μm.

circuit stage. The next section will examine each of these circuit blocks in turn.

5.1 Active Comparator Circuit Blocks

This section will discuss the design of each of the circuit blocks represented in Fig. 5.1. Supply voltage for all circuits is 1.5V, and any capacitors which are unmarked are 1 pF. The RFIC is designed using the IBM 8RF 130 nm RF-CMOS process using Cadence design tools. All transistor gate lengths are 130 nm unless otherwise marked.

5.1.1 Active Balun

The active balun is used convert the single-ended input signals to differential signals. This conversion is necessary for the addition and subtraction operations which follow. The circuit diagram of the active balun is shown in Fig. 5.2. The basic circuit consists of a common-base amplifier and a common-source amplifier in parallel, which ideally provide a

Table 5.1. Active balun component values

Resistors		Inductors	
R1	3kΩ	L1	313 pH
R2	2kΩ		
R3	463Ω		
R4	11Ω		

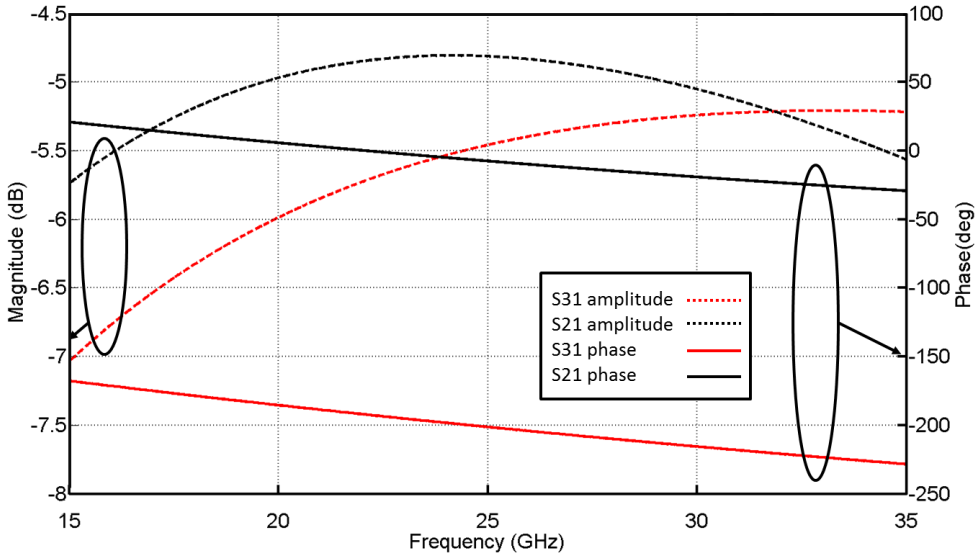


Figure 5.3. Simulated performance of the active balun circuit. At 24 Ghz, the simulated error between the two phases is 13.3°, and amplitude imbalance of 0.73 dB.

phase shift of 180 degrees relative to one another. Blocking capacitors on the input and output of the circuit prevent DC bias from affecting the adjacent stages. Resistors R1 and R2 are base-diffused resistors which provide the gate bias to the amplifiers. R4 and L1 are used for input matching. The values for R4 and R3 (which provides the drain bias) are relatively small for a traditional base-diffused resistor. Therefore, high-quality BEOL resistors available in the IBM 8RF process are used. The transistor gate widths are 25 μm.

The gain of the active balun circuit is a little more than unity, when factoring in the 3 dB loss due to splitting the signal in half. Fig. 5.3 shows the performance of the active balun circuit over a frequency range of 15-35 GHz. At 24 GHz, the simulated error between

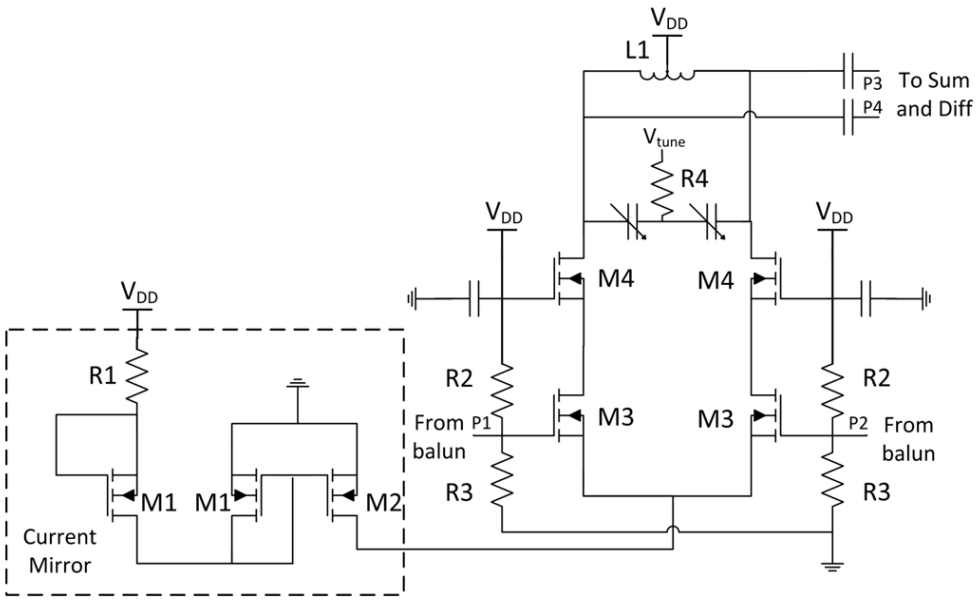


Figure 5.4. Differential amplifier circuit diagram. Cascode amplifier with current mirror (inset) to provide virtual ground and varactors for frequency response tuning.

Table 5.2. Differential amplifier component values

Resistors		Inductors		Gate widths	
R1	1.5kΩ	L1	313 pH	M1	1 μm
R2	6kΩ			M2	50 μm
R3	2kΩ			M3	25 μm
R4	3kΩ			M4	40 μm

the two phases is 13.3°, with an amplitude imbalance of 0.73 dB, as shown in Fig. 5.3. This imbalance is corrected in the differential amplifier stage which follows the active balun.

5.1.2 Differential Amplifier

The differential amplifier (shown in Fig. 5.4) consists of a cascode differential pair amplifier, with a current mirror providing a common mode virtual ground instead of an inductor. In addition to providing a virtual ground, the current mirror is used to provide the tail current to the differential pair. Current mirrors are used to maximize gain and occupy a relatively small area when compared with a resistor sized to provide adequate current [104].

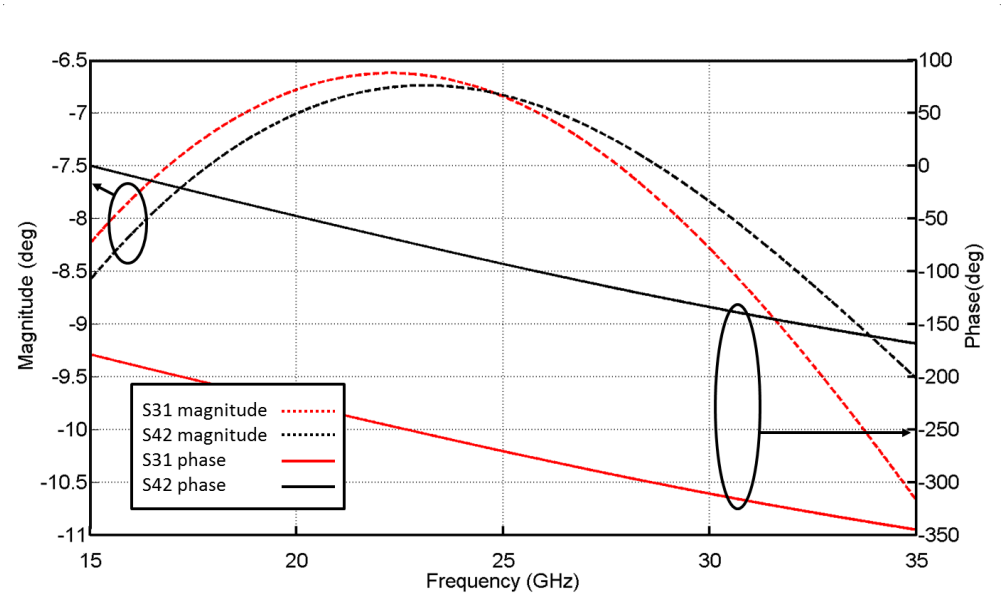


Figure 5.5. Simulated frequency performance of a differential amplifier circuit and active balun. Ports are defined in Figure 5.4. The phase between the two paths is ideally 180°.

For the RF choke (L_1), a center-tapped inductor was chosen. This topology was selected primarily for layout considerations. The die area occupied by a single symmetric, center-tapped inductor is approximately half that occupied by two regular inductors. Two varactors provide frequency response tuning via the V_{tune} voltage. The tuning range of these varactors is between 16 and 48 fF, for a voltage range of 0 to 1.5 V. For the simulations discussed in this section, the V_{tune} voltage is held at 1.5 V.

The simulated frequency response of the active balun and differential amplifier in series is shown in Fig. 5.5. The primary purpose of the differential pair amplifier is to correct the phase and amplitude error of the active balun, as opposed to adding gain. The simulated gain of the differential amplifier is slightly less than unity. Figure 5.6 shows the phase and amplitude error between path 12 and path 13 of the balun and the path from Port 1 of the balun to the outputs of the differential amplifier. The error is optimized at the center frequency of 24 GHz. At 24 GHz, the error is reduced from a phase imbalance 13.3° and an amplitude imbalance of 0.73 dB without the differential amplifier to a phase imbalance 2.4° and an amplitude imbalance of 0.05 dB with the differential amplifier. Optimizing these

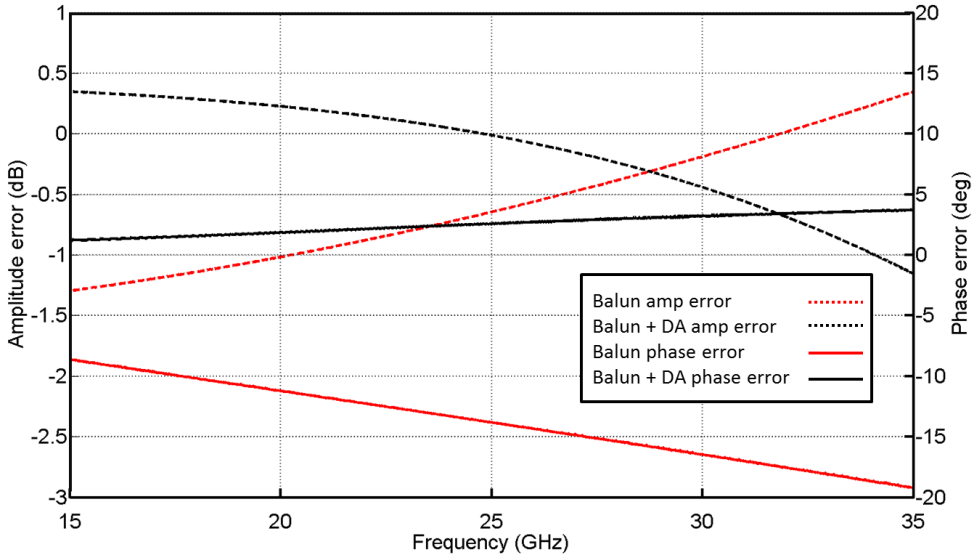


Figure 5.6. Simulated amplitude and phase error for active balun and differential amplifier. At 24 GHz, simulated phase imbalance is 2.4° and amplitude imbalance is 0.05 dB

values improves gain in the sum and difference amplifier stages, as well as reduces error in the comparator operation.

5.1.3 Sum and Difference Amplifiers

The sum and difference amplifiers shown in are shown in 5.7 and 5.8, respectively. These circuits consist of two sets of differential pair amplifiers, whose structure is very similar to the cascode differential amplifier of Section 5.1.2. The component values for the sum and difference amplifiers are the same and are summarized in Table 5.3. However, the signals from the two differential pairs are combined differently using current summing nodes to generate the sum and difference operations. For the sum amplifier, in-phase paths are added together. For the difference amplifier, the out-of-phase paths are summed. Ideally, the two inputs are in-phase to the difference amplifier, the two signals being summed from each output are exactly 180° out of phase; thus, a subtraction operation is performed.

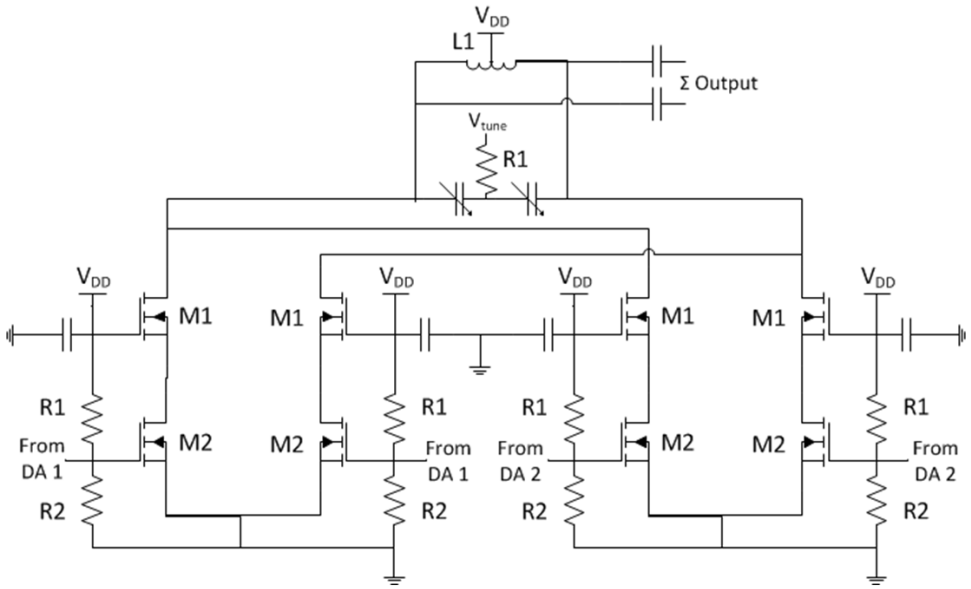


Figure 5.7. Summing amplifier circuit diagram. In-phase legs are summed to provide an overall sum operation.

Table 5.3. Summing amplifier and Difference amplifier component values

Resistors		Inductors		Gate widths	
R1	3kΩ	L1	496 pH	Q1	40 μm
R2	2kΩ			Q2	30 μm

The most useful circuit simulation of the sum and difference amplifier performance is with the configuration of a two port monopulse comparator, as shown in Fig. 4.1. For simulation purposes, an ideal balun is used at the output of the sum and difference amplifiers. Fig. 5.9 shows the performance of such a two-port comparator when swept over angle of arrival. The angle of arrival is simulated by sweeping the phase of one input relative to the other. The relationship between the phase difference at the input of the circuit ($\Delta\Phi$)and the angle of arrival of the signal relative to the simulated antenna array(Θ) can be expressed as $\Delta\Phi = kdcos(\Theta)$, where d is the antenna spacing (center to center), and k is $\frac{2\pi}{\lambda}$. For the purposes of these plots, d is assumed to be 0.5λ, or 1.25 cm at 24 GHz.

The summing amplifier provides a gain of 7.1 dB, with the output signal at 5.1 dB at boresight. A null in the difference amplifier output of 92 dB is simulated, with an overall

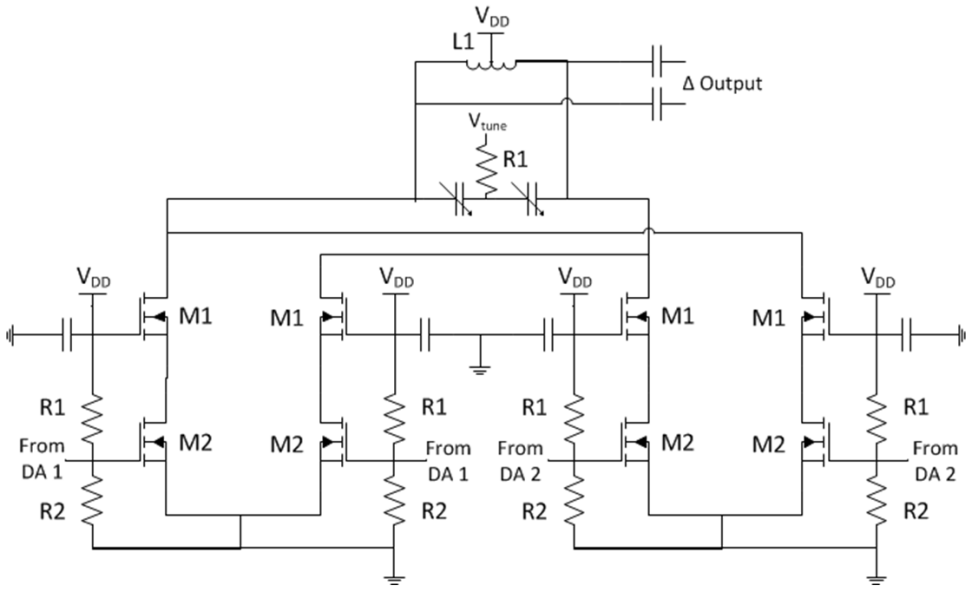


Figure 5.8. Difference amplifier circuit diagram. Out-of-phase legs are summed for an overall subtraction operation

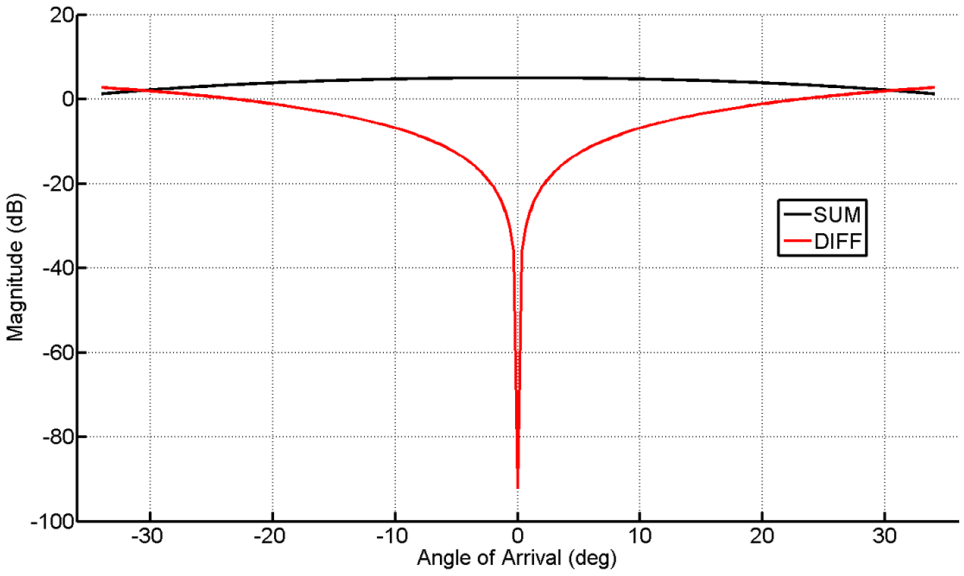


Figure 5.9. Simulated sweep of 2-port comparator against angle of arrival. At boresight, a monopulse null of 97 dB is simulated relative to the sum pattern.

monopulse null of 97.1 dB relative to the sum pattern. In practice, this result is unmeasurable. In addition, layout-related parasitics will further degrade the depth of this null. Fig.

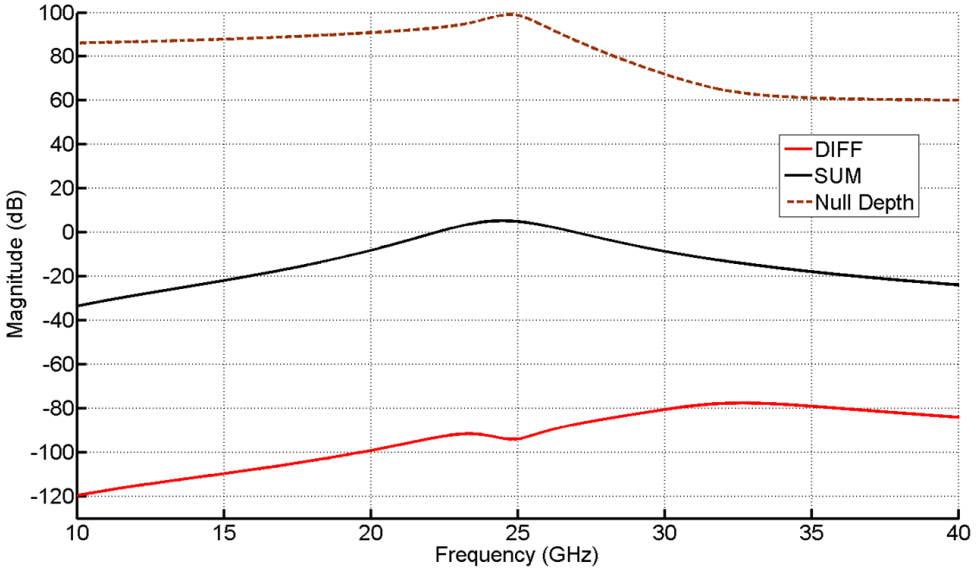


Figure 5.10. Simulated frequency sweep of 2-port comparator at boresight. Summing and difference amplifiers are shown, as well as simulated null depth, referenced to the summing amplifier output.

5.10 shows the simulated outputs of the summing and difference amplifiers in the 2-port monopulse comparator configuration over frequency. It is clear from this figure that the designs are optimized at 24 GHz, but may be functional over a larger bandwidth by trading off null depth.

5.1.4 Differential to Single-Ended Conversion

The final circuit block is a push-pull differential to single-ended output circuit (shown in Fig. 5.11). As with the active balun, in a fully integrated receiver, this circuit would not be necessary. It is included in this design to facilitate single-ended probe measurements.

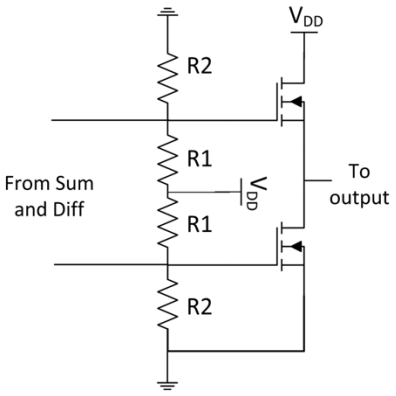


Figure 5.11. Differential to single ended conversion circuit diagram. R1 and R2 are 3kΩ and 2kΩ, respectively. Transistor gate widths are 30 μm

5.2 Comparator Simulation and Layout

5.2.1 4-port System simulation

The full simulation of the 4-port system with two stages of sum and difference amplifiers as shown in Fig. 5.1 is outlined in this section. Fig. 5.12 shows the result of a sweep of the signal source across an azimuthal plane, while at boresight in the elevational plane. This is approximated in simulation by sweeping the phase of inputs A and B relative to the phases of inputs C and D. An overall gain of 12 dB of boresight is shown for the SUM channel. The ΔAZ output has a null of 59 dB, for a total monopulse null of 71 dB. Both the ΔEL and Q channels remain below -56 dB.

The sweep of the signal in an elevational plane is shown in Fig. 5.13. This is approximated in simulation by sweeping the phase of inputs A and D relative to the phases of inputs B and C. An overall gain of 12 dB of boresight is shown for the SUM channel. The ΔAZ output has a null of 56 dB, for a total monopulse null of 68 dB. Both the ΔAZ and Q remain below -59 dB. The small discrepancy in the two nulls may be a result of the order the sum and difference operations are performed. The ΔEL is a sum of differences, which tends to be slightly larger than the difference of sums ΔAZ in an ideal system. The performance of each

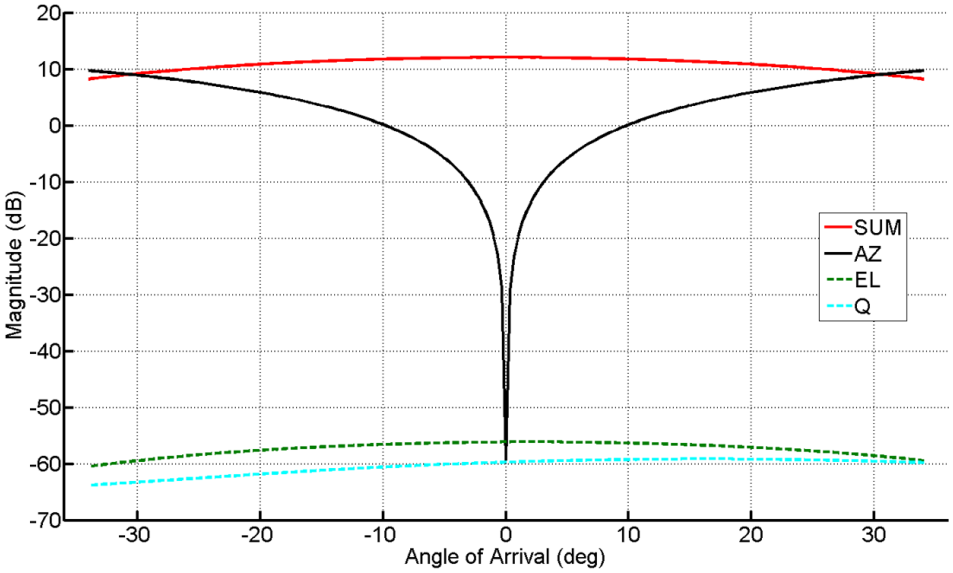


Figure 5.12. Simulated sweep of full comparator performance in an azimuthal direction. A monopulse null of 71 dB is simulated

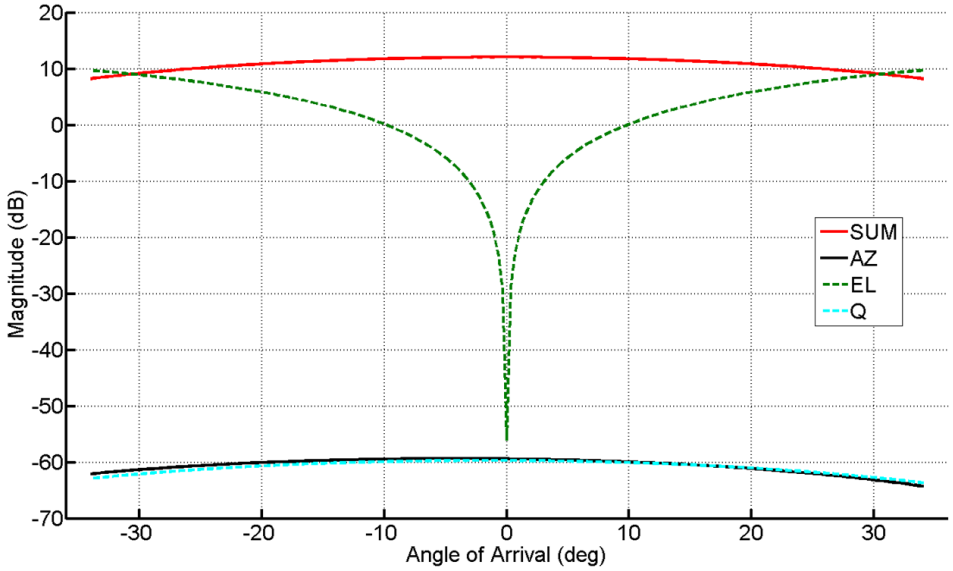


Figure 5.13. Simulated sweep of full comparator performance in an elevational direction. a monopulse null of 68 dB was simulated.

signal at boresight over frequency is shown in Fig. 5.14. Acceptable performance (> 60 dB null) is shown from 22 to 28 GHz. All of the simulations in this and the previous section

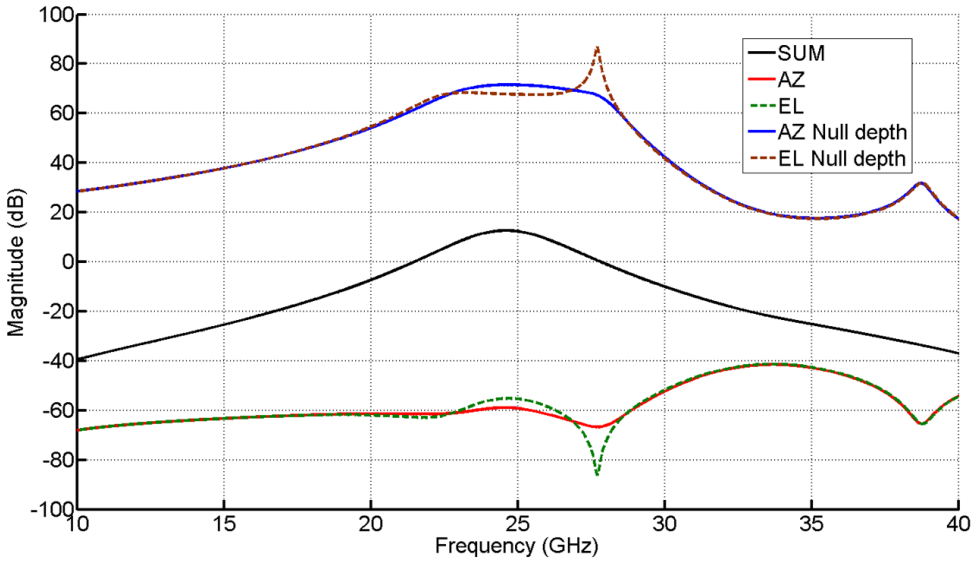


Figure 5.14. 4-port monopulse outputs vs frequency. SUM, ΔEL and ΔAZ are included, as well as the total monopulse nulls in azimuth and elevation

do not include layout-related parasitics. The addition of these parasitics would likely reduce the overall null depth produced by these circuits.

5.2.2 Layout

The layout of the MMIC was performed using Cadence Virtuoso Layout tools, and is shown in Fig. 5.15. The circuit was fabricated in the IBM 8RF RFCMOS process. In addition to the RF CMOS devices, the process features thick metal inductors, MIM capacitors, base-diffusion resistors, and highly accurate BEOL resistors. The metal option for the multi project wafer on which the chip was fabricated was DM, which consists of an eight metal stackup, with 4 thick top metals for RF transmission lines and passives.

When laying out the circuit, it was necessary to pay special attention to the measurement requirements, especially in regards to the layout of the input and output pads. The left and right sides of the chip are used for RF inputs, with two inputs applied to each side using a 150 μm pitch GSGSG RF probe. Both the top and bottom contain 2 single-ended RF

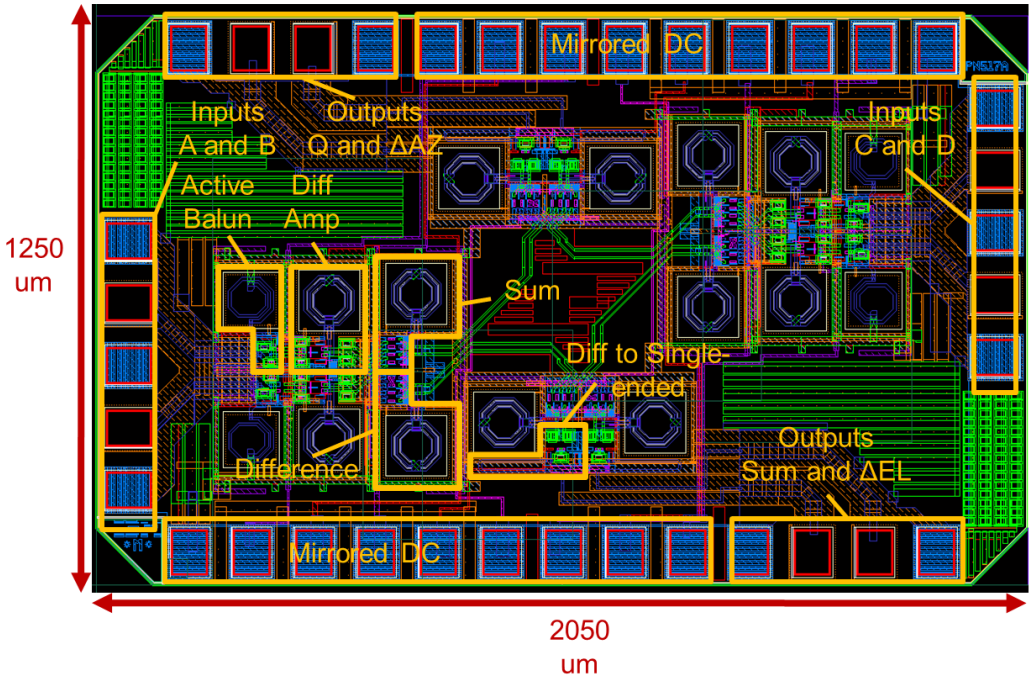


Figure 5.15. 24 GHz 4-port monopulse comparator MMIC layout. Chip dimensions are 1250 x 2050 μm. Inputs are located on the left and right of the chip, outputs on the top and bottom. DC lines are mirrored top and bottom

outputs and 9 DC pads. The DC pads are mirrored on top and bottom of the chip. RF outputs are measured using a 150 μm pitch GSSG probe. With this configuration, only two outputs can be measured at once (either Q and ΔAZ or SUM and ΔEL), while the DC signals are applied to the other side of the chip. Simulations indicated that it was not necessary to terminate the un-probed output ports. To measure the other two outputs, the DC and RF probes are switched.

Aside from input and output limitations, care was taken to minimize interconnection distance. Other than input and output pad routing, there are no routing paths greater than $\frac{\lambda}{20}$ (625 μm). Extensive use of hierarchal design to promote symmetry was also key to reducing phase mismatch between paths. A layout "core" consisting of the 2 active baluns, 2 diff amps, a summing amplifier and a difference amplifier is replicated at both sets of input pads. The second stage of sum and difference amplifiers and output differential to single-

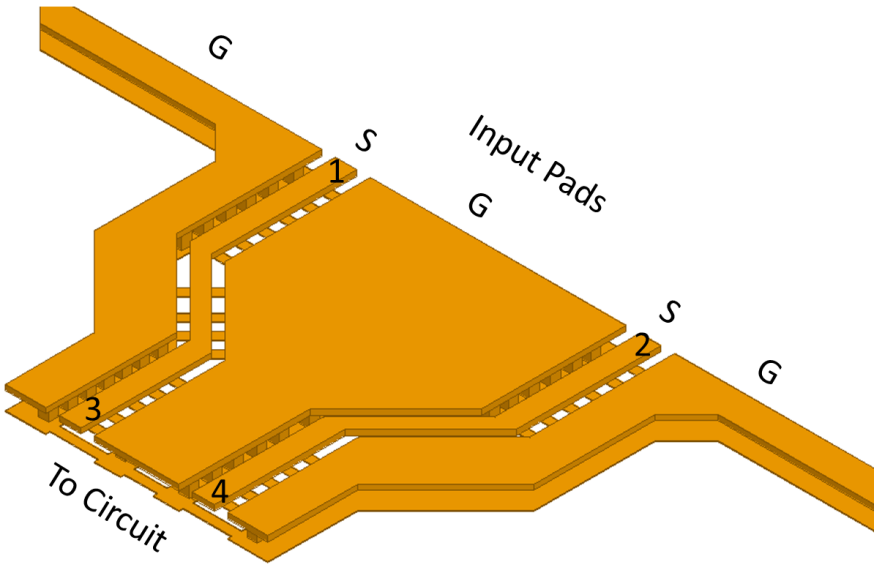


Figure 5.16. Input CPW model for 3-D FEM simulation

ended circuits are also mirrored in such a way as to maintain balanced interconnection lengths. Extraction of layout related parasitics was not completed, due to time constraints during the design phase.

5.2.3 Input and Output CPW Simulation

50Ω coplanar waveguide (CPW) transmission lines are used to connect the probe pads for testing to the active circuit. The CPW signal lines are routed in the 4 μm thick aluminum top metal (MA) available in the 8RF-DM process. To allow DC lines to be routed under the CPW lines with minimal crosstalk, a ground shield is added on the fourth metal layer down from the surface (MQ). The ground shield directly below the signal line is cross-hatched to minimize the its capactivie effects on the signal line, while maintaining the shielding from DC lines routed underneath. No gaps in the shielding larger than 35 μm occur, and most are less than 8 μm (thousandths of a wavelength at 24 GHz). The gap from the signal line to the ground shield underneath is 12.9 μm, and the dielectric is Silicon dioxide, which has a relative dielectric constant of 4.1.

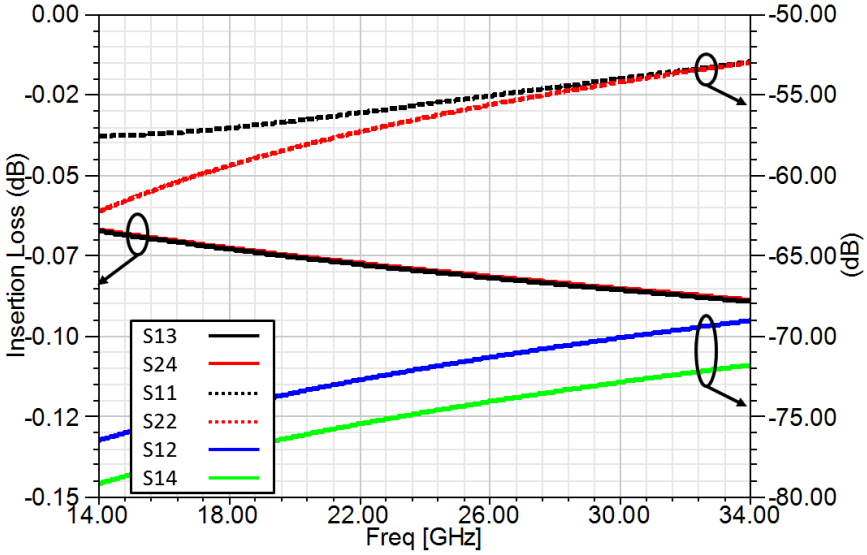
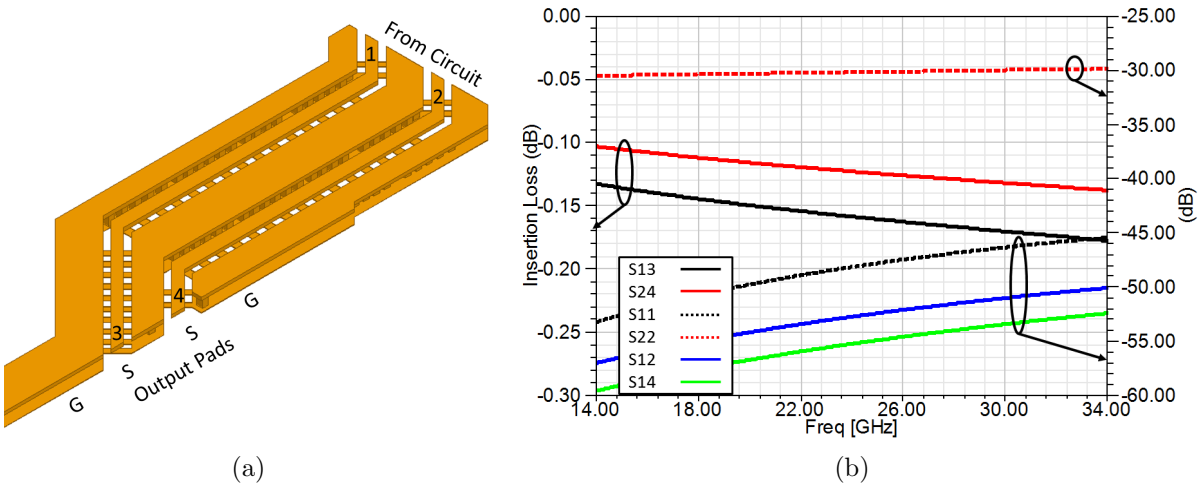


Figure 5.17. Simulated performance of input CPW. Simulations performed using Ansys HFSS 3-D FEM software.

The routing of the CPW is dictated by the location of the pads and their spacing along the outside edge of the MMIC. A 3-D model of the design is shown in Figure 5.16; the dielectric is omitted for clarity. The center conductors are 16 μm wide and the gap between the signal line and the ground lines is 10 μm. The choice of these dimensions is dictated by the spacing design rule for the top metal. The total length of the signal line is approximately 290 μm ($\sim \frac{\lambda}{4}$ at 24 GHz).

Simulated results are shown in 5.17. Simulations are performed using Ansys HFSS 3-D FEM software. The insertion loss for both paths is less than 0.1 dB, and the return loss is greater than 50 dB. Line to line isolation is simulated to be greater than 65 dB.

Similar modeling (Figure 5.18a) was done for the CPW which connects the outputs of the active circuitry with the GSSG pads for probing. The dimensions of the CPW are similar to the input CPW, but routed differently as required for the location of the pads. The path from Port 1 to Port 3 (13) is 400 μm and the path from port 2 to port 4 is 520 μm. At the outputs, since the comparator operation is complete, phase matching is not required. The simulated results are shown in Figure 5.18b. The insertion loss is less than 0.19 dB



(a) (b)

Figure 5.18. (a) 3-D model of output CPW structure (b) Simulated performance of output CPW

for path 24 and less than 0.14 dB for the 13 path. The additional loss is consistent with the additional length of line and the difference in return loss for the two lines. Line-to-line isolation is less than 65 dB.

5.3 Testing

The test setup to measure the MMIC is shown in Fig. 5.19. The input of the VNA is connected to an in-phase splitter, whose outputs are each connected to a phase shifter. The output from each phase shifter is then split again. The outputs of the second layer of splitters is different depending on which sweep is desired. To approximate an sweep of the signal in an azimuthal direction, the inputs A and B are assigned to one phase shifter, and the inputs C and D are assigned to the second phase shifter. To approximate an sweep of the signal in an elevational direction, the inputs A and D are assigned to one phase shifter, and the inputs B and C are assigned to the second phase shifter. The signals arrive at the inputs of the RFIC via two 150 μm GSGSG probes on either side of the chip. Once beyond the phase shifters, matched cables must be used to prevent undue phase error at the RFIC A-D

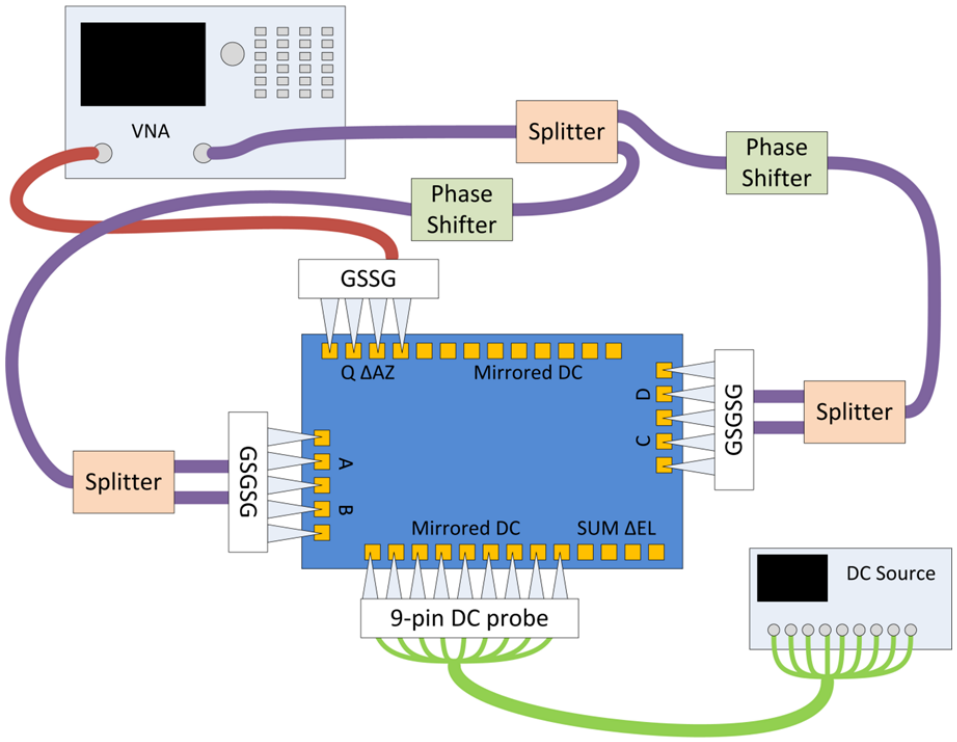


Figure 5.19. Testing configuration of the 4-port 24 GHz monopulse comparator RFIC for Q and ΔAZ output measurements. To measure other outputs, RF output and DC probes must be swapped (see Figure 5.20)

inputs.

As described in Section 5.2.2, nine DC pads and two RF outputs in GSSG configuration are on the top and bottom of the MMIC. The DC pads are mirrored, so that the entire chip can be powered from either edge. In general, all voltage inputs are set to 1.5V, but individual voltage control of each input is possible as well. Finally, one of the four RF outputs is attached to the second port of the VNA for measurement. Measurements of the MMIC were inconclusive. Bias voltages provided to the circuit did not result in proper currents. This may be a result of undetected layout errors or unaccounted for parasitics. Improper ESD handling may also have resulted in the devices failure.

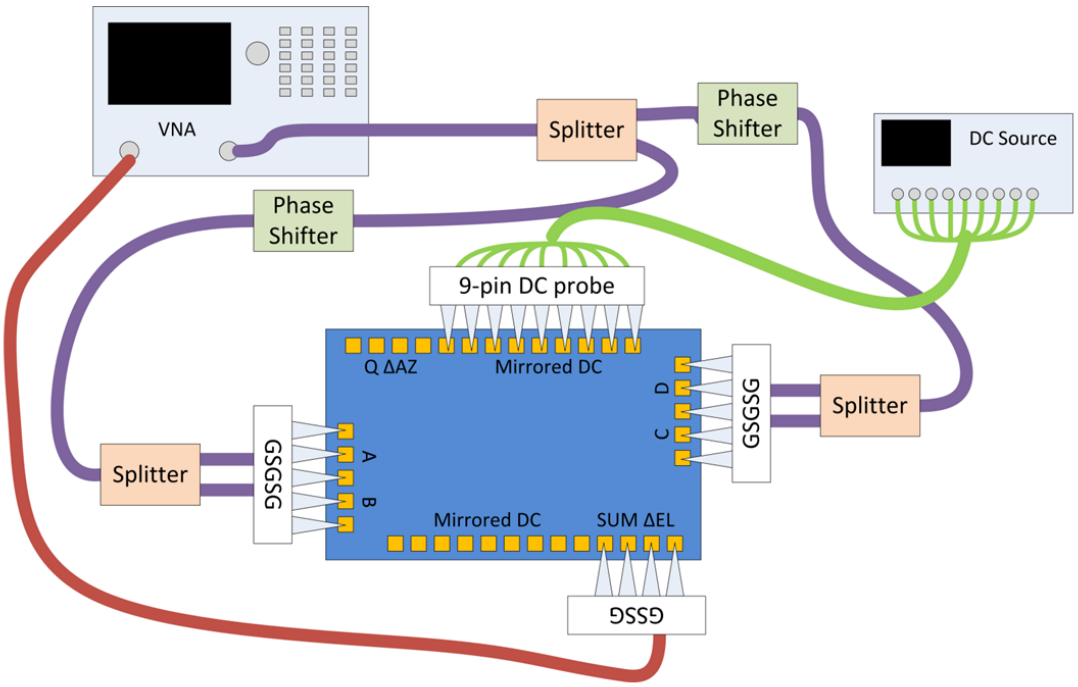


Figure 5.20. Testing configuration of the 4-port 24 GHz monopulse comparator RFIC for SUM and ΔEL output measurements.

5.4 Conclusions

This chapter has outlined the design and simulation of a 4-port active monopulse comparator RFIC. The RFIC was designed in the IBM 8RF 130 nm RF CMOS process. Simulated nulls of 71 dB and 68 dB were reported for the azimuthal and elevational sweeps, respectively. The design was laid out and fabricated. A test plan for the RFIC was presented. This circuit demonstrates the possibility of a compact 4-port implementation of an active comparator RFIC, which could be monolithically integrated with an RF-front-end to realize a compact mm-wave monopulse receiver. As CMOS technology improves, this circuit could be scaled to 94 GHz or other, higher, frequencies. Alternatively, the design could be implemented in the SiGe technology as utilizedn in Chapter 4. Future iterations will focus on scaling and integration into a more complex RF monopulse system-on-a-chip.

Chapter 6

V- and W-band Rectangular Coaxial Power Combining Networks and Solid-State Power Amplifier Implementations

While the majority of this work has focused on the receiver portion of a compact mm-wave monopulse transceiver, the transmit portion of the transceiver is often the limiting factor in terms of integration of mm-wave systems. In the VHF/UHF frequency range, the drive towards more compact solid state power amplifiers (SSPAs) has been ongoing for several decades [105]. Solid state amplifiers utilize a number of power-combined transistors or MMICs to achieve higher power levels. There are a number of advantages for solid-state transmitters compared to vacuum tubes, including higher linearity, higher reliability, superior noise performance, reduced size and weight, and the elimination of warmup time [106]. SSPAs are less prone to "hard" failures, as individual amplifier cells within power-combined modules can be replaced while the SSPA is in the field. For high-power broadcast applications, solid-state transmitters provide efficiency improvements over tube-based transmitters, as

well. Adoption rates in the broadcast industry are very high, with very few new tube-based transmitters being produced at this writing.

At microwave/mm-wave frequencies, however, SSPAs are not as in wide use. Microwave applications which require higher power levels, such as X-band radar and satellite communications links tend to be dominated by vacuum electronics, such as travelling wave tube amplifiers (TWTAs). TWTAs are an established technology, dating from the 1960s. They offer high-reliability, long lifetimes, high efficencies (70% at Ku band [107]), and high power levels (several kilowatts at X-band) [108]. However, TWTAs are often very large. A need for more compact high power microwave and mm-wave power sources has driven extensive research into the development of SSPAs at these frequencies. TWTAs also have a number of other disadvantages, including linearity issues and relatively long startup times.

There are a number of impediments to the development of mm-wave SSPAs. Silicon CMOS chip technology improvements which allow for much higher frequency operation, such as shorter gate lengths and reduced thickness gate oxides, are not conducive to high-power operation. On the other hand, Recent advantages in wider band-gap technologies such as GaN and InP have significantly improved performance. At X-band, GaN MMICs with power outputs in the 50 watt range have been demonstrated [109], and at V-band InP MMICs have been demonstrated with 40% efficiency [110]. These values are beginning to approach available TWTA performance. In addition to limitations from available chip technologies, efficiency losses from combining is a significant contributing factor to lower overall efficiency. This chapter will examine the use of rectangular coaxial power combiners as an enabling technology for compact mm-wave power amplifiers at V- and W-band. This chapter will discuss the design and test of several V-band Gysel combiners, as well as provide a comprehensive examination of W-band power combining approaches which leverage rectangular coaxial routing for optimal performance.

6.1 Microwave Power Combining Techniques

At microwave frequencies, building SSPAs using traditional transmission line technologies such as microstrip, CPW or stripline to implement corporate combining networks is a prevalent technique. Reference [111] describes the use of a suspended stripline Wilkinson dividers to create a 250 W X-band SSPA. To minimize the insertion loss of the combiners, the isolation resistors were removed. The measured pulsed power was 263 W, with an efficiency of 24% by combining 4 GaN MMICs. Given that each MMIC has a measured output of 81W and Power Added Efficiency (PAE) of 34%, it is clear that the 0.4 dB insertion loss cited in from the combining network in [111] is a serious detriment to overall performance. As the frequency of operation increases, the losses in the microstrip combining networks also increase. For example, a loss of 0.6 dB per path at V-band is reported in [112] for a three-way microstrip combining network.

One alternative to traditional planar transmission line approaches is corporate combining using custom fabricated waveguide hardware, as shown in [113]. This particular implementation combines 4 GaAs MMICs at 35 GHz with an insertion loss per path of 0.2 dB for a peak combining efficiency of 91%. However, a corporate waveguide combiner at microwave frequencies requires high-precision machining and is significantly larger and heavier than the stripline implementation presented above.

Spatial power combining is another mm-wave combining technique that has received significant attention. Spatial combining refers to the use of "free-space combining", essentially coupling the output of a series of MMICs via an antenna array or a waveguide aperture. Spatial combiners typically take one of two forms: the "pallet" or "tray" form or the "tile" form [114]. The tray form is broadly defined as one which propagates the input and output power tangential to the power devices. Typically, this is achieved by mounting the power devices in a carrier with radiators on the input and output. These carriers are then stacked to create a 2-D aperture and the outputs coupled into an overmoded rectangular waveguide, where the power combining occurs. Some examples of the tray architecture are shown in [115], [116],

and [117]. An alternative architecture to the stacked trays is a radial combiner, as discussed in [118], [119] and [120]. Radial combiners place the combiner pallets in waveguide sections that have a toroidal segment cross-section. These waveguides are situated around a central supporting cylinder. At the output, the power is combined in a radial waveguide combiner.

The tile form of a spatial combiner is broadly defined as one which the array of power devices couples to a signal normal to the power device. Two distinct forms of tile combiners exist in the literature: "grid" amplifiers and active array amplifiers [114]. The grid amplifier is an array of differential transistor pairs with cross-polarized input and output dipole antennas. This approach lends itself to high density, single MMIC implementations, as shown in [121] and [122]. Active array implementations use antennas such as patches or slots in the same manner. The unit cell for an active array is larger than that of a grid, which allows the use multistage MMICs (as opposed to a single differential pair per cell) for higher gain and power. Often, passive antennas and tuning networks are hybridly integrated to save valuable die real estate [123].

Generally speaking, spatial combiners have advantages for combining a large number of devices, which are necessary for higher power levels at mm-wave. Fig. 6.1 (from [124]) shows the relationship between the number of devices combined and the combining efficiency. For spatially combined PAs, there is ideally a flat efficiency no matter how many MMICs are combined. For corporate combining networks, on the other hand, the slope of the overall efficiency is related to the insertion loss of a single 2:1 combination (represented in Fig. 6.1 by α). Given the limitations on insertion loss at mm-wave in microstrip and other trasitional transmission lines, spatially combined SSPAs have an advantage, particularly for large numbers of amplifiers.

However, the use of rectangular coaxial technology to create power combining networks represents a significant improvement over traditional transmission line technology, with reduced loss and higher isolation. Given a value for α of less than 0.1 dB at mm-wave frequencies, a rectangular coax-based corporately combined SSPA becomes attractive in comparison

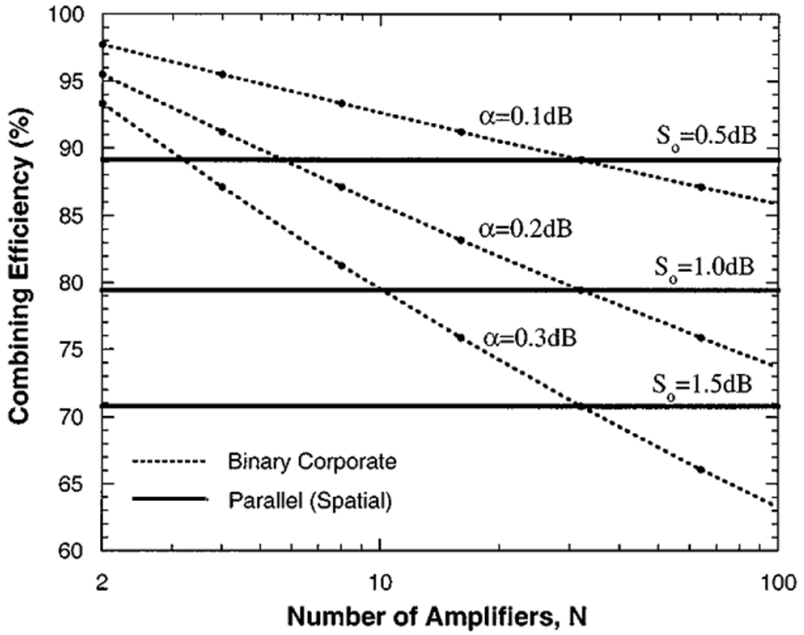


Figure 6.1. Plot of combining efficiency vs number of amplifiers for spatial and corporate combining [124]. α represents combining loss per binary division for corporate combiners. © 2001 IEEE

to spatial combiners. High isolation allows for extremely compact SSPA architectures, often 10x more compact than a waveguide combiner. A general discussion of the advantages of a rectangular coaxially-based SSPA can be found in [42].

Three basic combiner architectures will be examined in this chapter, (1) reactive combiners, (2) Wilkinson combiners and (3) Gysel combiners. The simplest form of microwave passive combiner is a T-junction, or reactive combiner. This combiner is a resonant structure; each leg of the combiner acts as a quarter-wave transformer, and should have a length equal to $\frac{\lambda}{4}$ at the frequency of interest. A circuit diagram for a two-way reactive combiner is shown in Figure 6.2a. The impedance of the transformer segments for an N-way reactive combiner can be expressed as:

$$Z_a = Z_0\sqrt{N} \tag{6.1}$$

The structure of a 2-way Wilkinson combiner is similar to that of the reactive combiner,

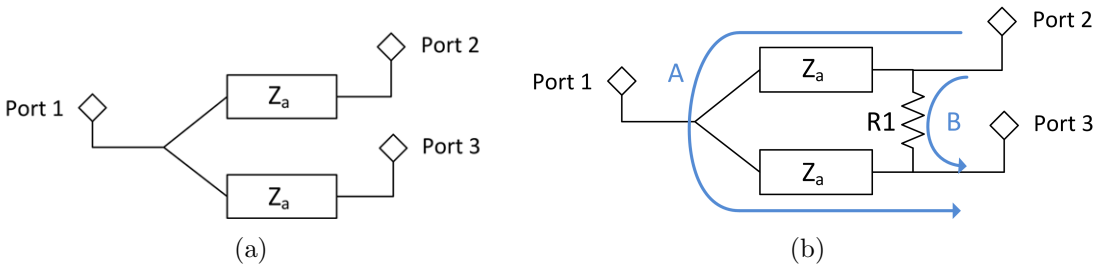


Figure 6.2. (a) Circuit diagram for a 2-way reactive combiner. For a 2-way equal split reactive combiner, $Z_a = 70.7\ \Omega$. (b) 2-way Wilkinson combiner circuit diagram. For a 2-way equal split Wilkinson, $Z_a = 70.7\ \Omega$ and R1 = 100 Ω.

with the addition of a $2Z_0$ resistor between input ports 2 and 3 (Figure 6.2b). This resistor provides isolation between the output ports. A signal applied to port 2 will be evenly split between the transmission line path A to Port 3 and the resistor (path B). Since an ideal resistor has no phase delay, and transmission line A path results in a 180° phase shift, the port 2 signal arriving at port 3 should be completely cancelled [125]. However, since non-ideal resistors have a finite phase shift associated with them, only finite cancellation is achieved in practice.

In addition to isolation, the Wilkinson's resistor provides a path for graceful degradation of an SSPA module. Graceful degradation refers to a state in which one or more of the component amplifiers fails and the system continues to operate, albeit at a reduced level [126]. The isolation provided by the resistor prevents the power reflected from the failed amplifier from entering the output of the functioning amplifier and causing it to fail. Unfortunately, a portion of the power from the functioning amplifier is dissipated in the isolation resistor as well. Generally speaking, this power level is related to the square of the fraction of remaining amplifiers [125] [127]:

$$P_f = P_0(1 - \frac{m}{n})^2 \tag{6.2}$$

where m represents the number of amplifier die failures and n is the total number of amplifier die in the SSPA system. For the combination of two PA MMICs, if one fails, the overall

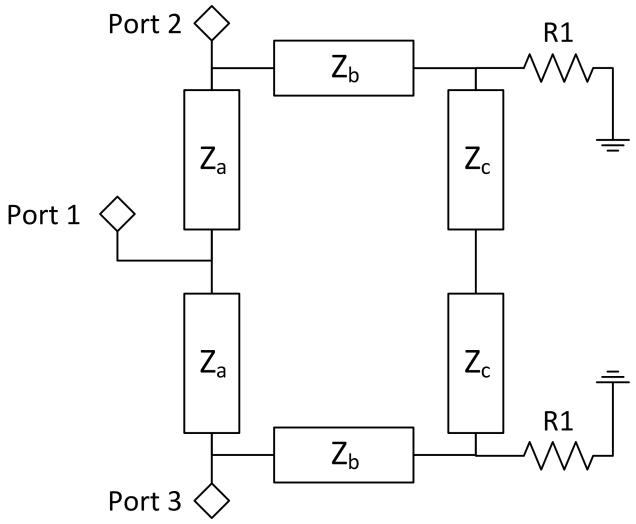


Figure 6.3. 2-way Gysel combiner circuit diagram.

system output power decreases by 6 dB. However, for a four PA MMIC combination, the loss of one MMIC results in a 2.5 dB reduction in overall system power.

The Gysel combiner architecture represents a more complex alternative to the Wilkinson combiner [128]. Fig. 6.3 shows the structure of 2-way Gysel power combiner. Each transmission line section is $\frac{\lambda}{4}$ in length. The inputs (ports 2 and 3) are connected to the output (port 1) via the Z_a impedance sections. The inputs are also connected to a load via the Z_b sections, and the loads from each branch are connected together via the Z_c sections.

One of the major advantages of the Gysel combiner over the Wilkinson is the placement of the resistive loads. The loads in the Gysel provide a thermal path to ground, which is invaluable for high power applications, particularly in the case of air-dielectric rectangular coax. In a microstrip or stripline structure, the substrate provides a thermal path to heatsinks for the heat generated on the signal line. However, air is a relatively poor thermal conductor, thus necessitating the need for alternative heat paths to ground for air-dielectric rectangular coaxial structures.

There are no closed-form equations for designing Gysel combiners with optimum performance [128], so optimum values for Z_a, Z_c, Z_b, and R1 are determined from a series of

simulations using ANSYS Designer or similar circuit simulation software. A number of V- and W-band implementations of these combiner architectures will be discussed at length later in this chapter.

6.2 Prior Rectangular Coaxial Power Combiners Work

Several implementations of rectangular coaxial corporate power combiners have been demonstrated in the literature. [129] demonstrates the design of a single-stage Wilkinson combiner from 20-40 GHz which has an insertion loss of 0.2 dB at 30 GHz. This particular implementation uses a NiCr isolation resistor sandwiched between two dielectric supporting straps which suspend the center conductor. The Ka-band Gysel combiner in [50] also utilizes an embedded resistor, and has insertion loss performance of 0.22 dB and isolation 20 dB for the entire Ka-band (26.5-40 GHz). It should be noted that fabrication difficulties were encountered with these embedded resistors. These issues were compounded by mechanical stresses exerted on the resistor structure as a result of its suspension between the center and outer conductors. In both [129] and [50], these failures resulted in only the resistor-less measurements of the dividers being presented. This is not an issue from an insertion loss perspective, but the output isolation of the combiners was severely degraded.

Broadband multi-section Wilkinson dividers are presented in [49], and discussed in more detail in [130]. Commercially available resistors were used to provide isolation over a 4.5:1 bandwidth (4-18 GHz). The process technology required a 100 μm gap between the center and outer conductor for successful fabrication. Due to these limitations, desired impedance values for the multisection Wilkinson could not be achieved for a 50 Ω system impedance, so a broadband Polystrata impedance match was added to the input of the divider.

6.3 V-band Rectangular Coaxial Gysel Combiners

This section will discuss the design, simulation and test of three V-band Gysel rectangular coaxial combining structures: a 2-1 combiner, a 4-1 "direct" combiner, and a 4-1 cascade of 2-1 combiners. Each of the combiners described in this section is intended to function over a band of 58-62 GHz.

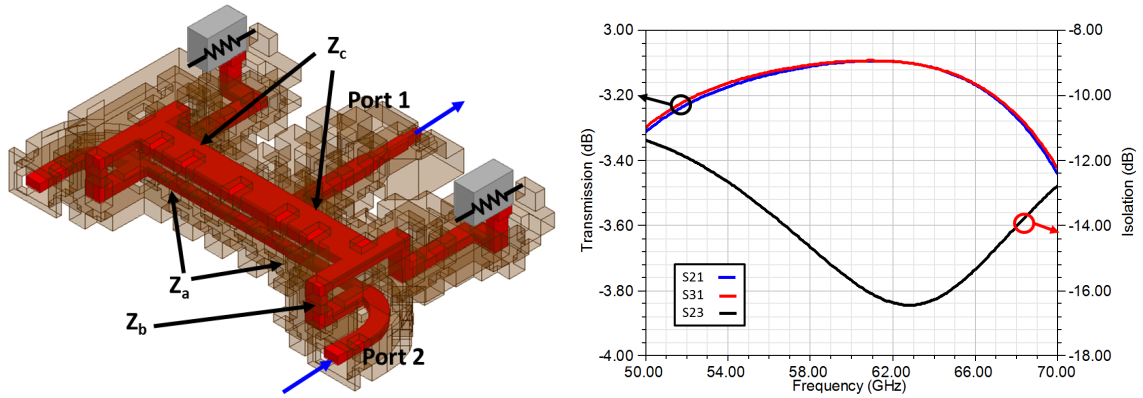
Though the devices discussed in this section and Sections 6.4 and 6.5 are being used in a combining mode, the simulation results reflect operation in a splitting mode. This is due to a fundamental limitation of S-parameter simulations, which only allow for the excitation of a single port at once. As such, 2-1 combiner simulations will have an additional -3 dB beyond the insertion loss, and 4-1 combiners will have -6 dB beyond the insertion loss.

Experimental verification of the insertion loss of combiners is often performed using a "back-to-back" structure. This consists of two combiners with their inputs connected together, resulting in a 2-port system. Back to back measurements have no splitting loss, and reflect 2x the insertion loss of a single combiner structure.

6.3.1 2-1 V-band Gysel Combiner

As discussed in Section 6.1, the combiner impedances in Figure 6.3 were optimized using ANSYS Designer. The optimization target was minimized insertion loss and maximized isolation over the desired bandwidth. Figure 6.4a shows the 3-D combiner designed in the PolyStrata process. Each transmission line section is 1.4 mm in length. The desired impedances are achieved by modifying the widths of the center and outer conductors. The required impedances and the dimensions of the rectangular coaxial line required to achieve the impedance for each section is shown in Table 6.1.

The termination resistor (R1) has a value of 75Ω. The termination resistors are commercially available wirebondable 0201 Al-N resistors (manufactured by US Microwaves),



(a) (b)

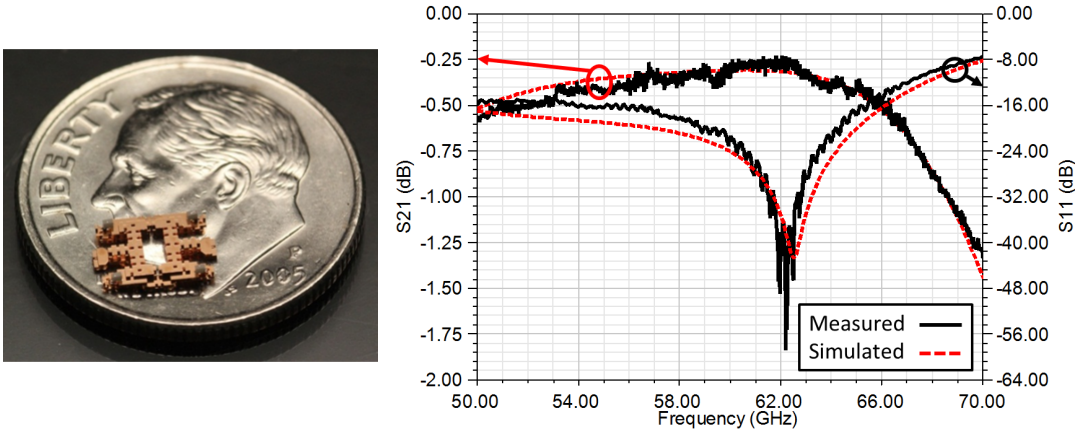
Figure 6.4. (a) 3-D model of rectangular coaxial implementation of 2-1 combiner. The Z_c transmission lines are located on top of the Z_a lines. Mounting locations for termination resistors are routed towards the combiner input to reduce footprint. (b) Simulated performance of 2-way rectangular coaxial Gysel combiner. The simulated results reflect splitting mode operation.

Table 6.1. 2-way Gysel impedances

	Impedance	Inner Conductor Dimensions	Outer Conductor Dimensions
Z_a	70.7Ω	100 μm x 88 μm	300 μm x 500 μm
Z_b	50Ω	100 μm x 176 μm	300 μm x 400 μm
Z_c	26Ω	100 μm x 390 μm	300 μm x 500 μm

assembled onto the circuit using conductive epoxy. The high isolation and 3-D routing capabilities of the PolyStrata process are used to full advantage to reduce the combiner footprint. Z_c transmission lines are located on top of the Z_a lines, and the termination resistors are routed back towards Port 1. 50 Ω lines are used to connect the termination resistors and the input and output ports. The Z_b impedance sections are routed vertically as a transition between Z_a and Z_c. The total volume of the combiner is 4.4 mm x 2.8 mm x 1.025 mm.

The simulated performance of the 2-1 combiner is shown in Figure 6.4b. The simulated insertion loss across the band for a single combiner is 0.11 dB, with an isolation between the two output ports of greater than 14.4 dB. In order to measure the insertion loss of the combiners, a back to back structure was fabricated. This device, shown in Figure 6.5a, is



(a) (b)

Figure 6.5. (a) Fabricated and assembled back to back 2-1 combiner (b) Measured vs simulated performance of back to back 2-1 combiner. Measured insertion loss and return loss are less than 0.35 dB and greater than 18 dB, respectively.

designed to be probed using standard 150 μm pitch GSG probes. A PolyStrata Through-Reflect-Line (TRL) calibration structure was used for calibration. The measured results are shown in Figure 6.5b, and show good correlation with simulation. The measured back-to-back insertion loss is 0.35 dB across the 58-62 GHz band. Given additional routing on the inputs which accounts for 0.09 dB of loss, the insertion loss for a single combiner structure is measured to be 0.13 dB.

6.3.2 4-1 Cascaded V-band Gysel Combiner

The first approach to realizing a 4-way combining network is a "planar combiner", which mimics an N-way microstrip combiner. The 2-way combiner in Section 6.3.1 is used as a building block and cascaded, with routing between the output of the first stage of combining and the input to the second stage of combining. The simulated performance is shown in Figure 6.6. The simulated insertion loss is less than 0.35 dB across the band, and the isolation is greater than 12.5 dB for adjacent output ports, and greater than 22 dB for non-adjacent ports. 0.13 dB additional loss beyond the ideal cascade (2x the insertion loss from

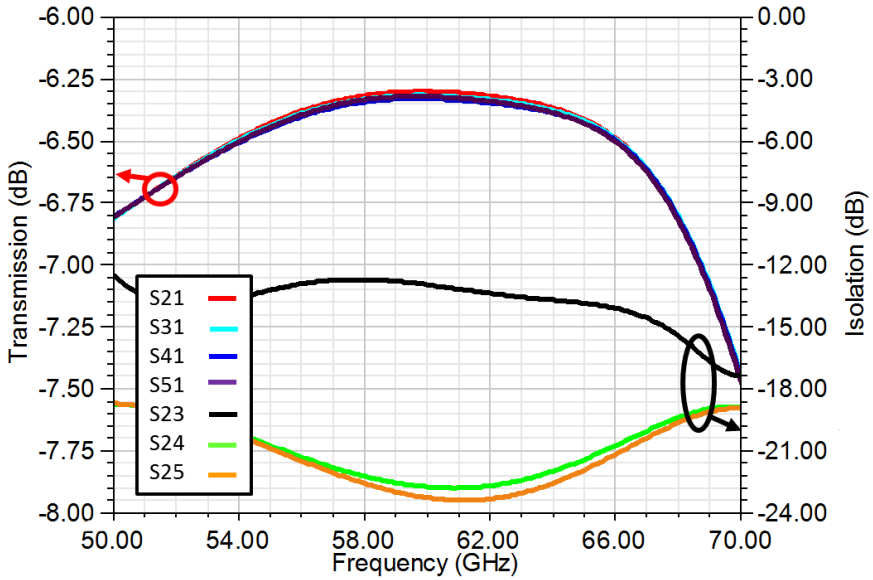
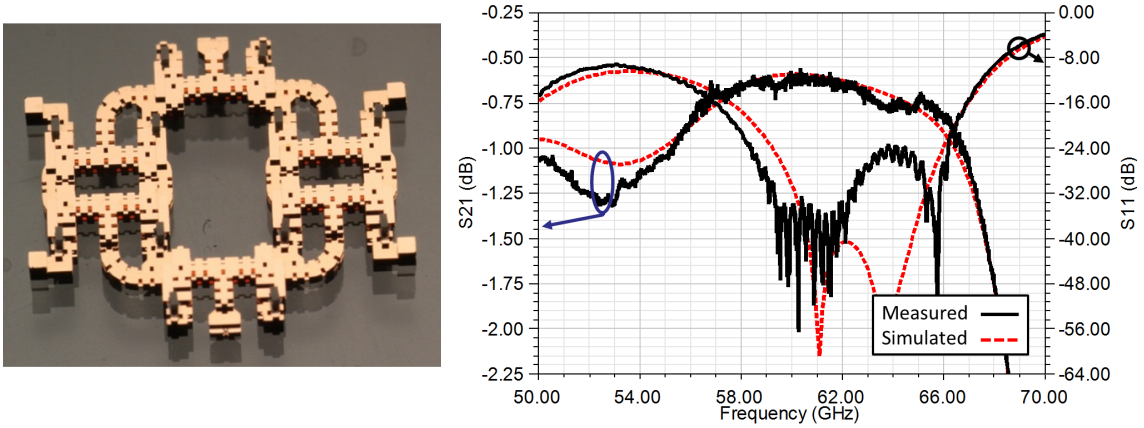


Figure 6.6. Simulated performance of 4-way planar rectangular coaxial Gysel combiner. The simulated results reflect splitting mode operation.



(a) (b)

Figure 6.7. (a) Fabricated and assembled back to back 4-1 "planar combiners. (b) Measured vs simulated performance of back to back 4-1 "planar combiners. Measured insertion loss and return loss are less than 0.7 dB and greater than 20 dB.

Section 6.3.1) is incurred due to the routing between stages.

The volume of the "planar" combiner is 12 mm x 5.5 mm x 1.025 mm (fabricated and assembled device shown in Figure 6.7a). The measured results for a back-to-back "planar combiner" are shown in Figure 6.7b. The simulated insertion loss for the back-to-back

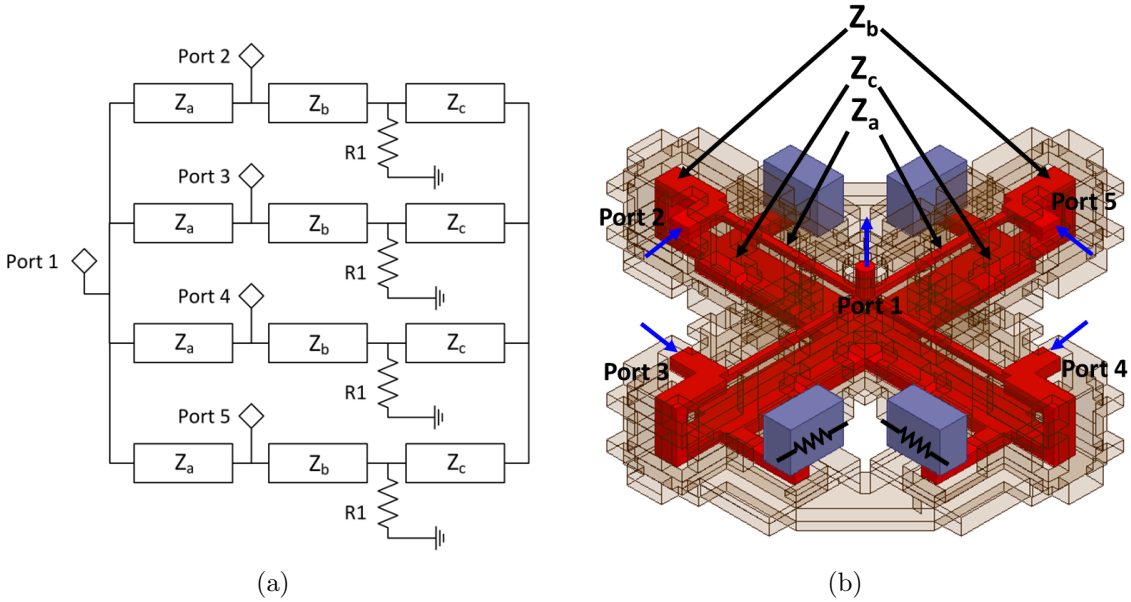


Figure 6.8. (a) Circuit model of 4-1 direct combiner. Each transmission line segment is 1.4 mm in length. The termination resistor is 75Ω. (b) 3-D model of rectangular coax implementation of the direct 4-1 combiner. Input (Port 1) is located at the top of the part.

structure is less than 0.65 dB across the band. The measured data correlates well with the simulation results. The discrepancies in return loss are most likely due to unaccounted for parasitics associated with the assembly of the resistors. However, the measured return loss of greater than 28 dB across the design bandwidth still represents a reasonable match.

6.3.3 4-1 Direct V-band Gysel Combiner

An alternative to cascaded binary approach of the previous section is the extension of the Gysel architecture to direct 4-1 combining, as shown in Figure 6.8a. For the 3-D model shown in Figure 6.8b, the impedances of each section and their dimensions are shown in Table 6.2. These values are again obtained through optimization in a circuit simulator.

The inputs of the combiner are located on each leg in the upper layer of coaxial line. In the lower layer, at the intersection of the Z_b and Z_c impedance sections, a short section of 50 Ω line is used to provide a mounting location for the load resistor. The resistors chosen

Table 6.2. 4-way Gysel impedances

	Impedance	Inner Conductor Dimensions	Outer Conductor Dimensions
Z_a	100Ω	50 μm x 55 μm	300 μm x 400 μm
Z_b	50Ω	100 μm x 201 μm	300 μm x 500 μm
Z_c	26Ω	100 μm x 390 μm	300 μm x 500 μm

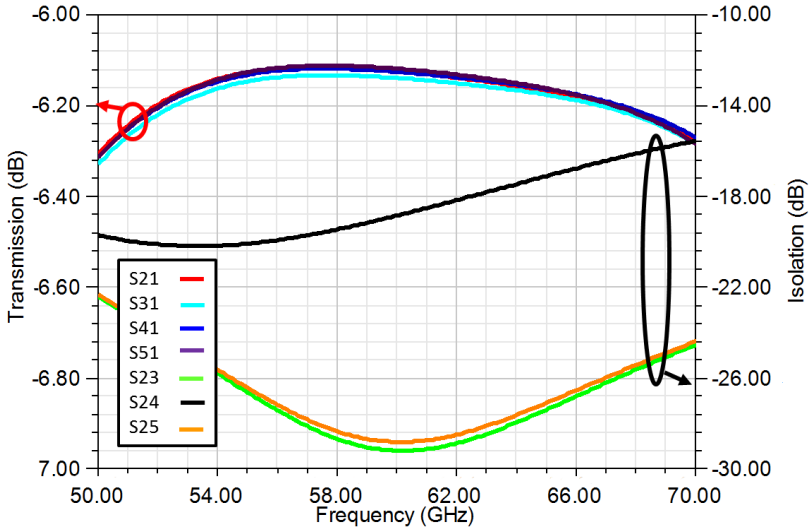


Figure 6.9. Simulated performance of a single 4-way direct rectangular coaxial Gysel combiner. The simulated results reflect splitting mode operation.

are the same 0201 aluminum nitride resistors discussed in previous sections. The output of the combiner is located in the center of the structure and exits through the top of the combining network. The simulated performance of the direct combiner is shown in Figure 6.9. The simulated insertion loss is less than 0.15 dB, and the isolation is greater than 18 dB for directly opposite legs and greater than 28 dB for adjacent legs. The overall volume of the direct combiner is 4.2 mm x 4.2 mm x 0.85 mm.

To facilitate insertion loss measurements, a back to back structure was assembled. The outputs of the combiners (Port 1) were routed to the edges. Given the 15 layer stack-up of the available fabrication run, this routing was fabricated as partial coax, and a cap was assembled to complete the coax (see Figure 6.10a). In practice, this additional assembly step could be eliminated by directly interfacing with the next layer, or the addition of more

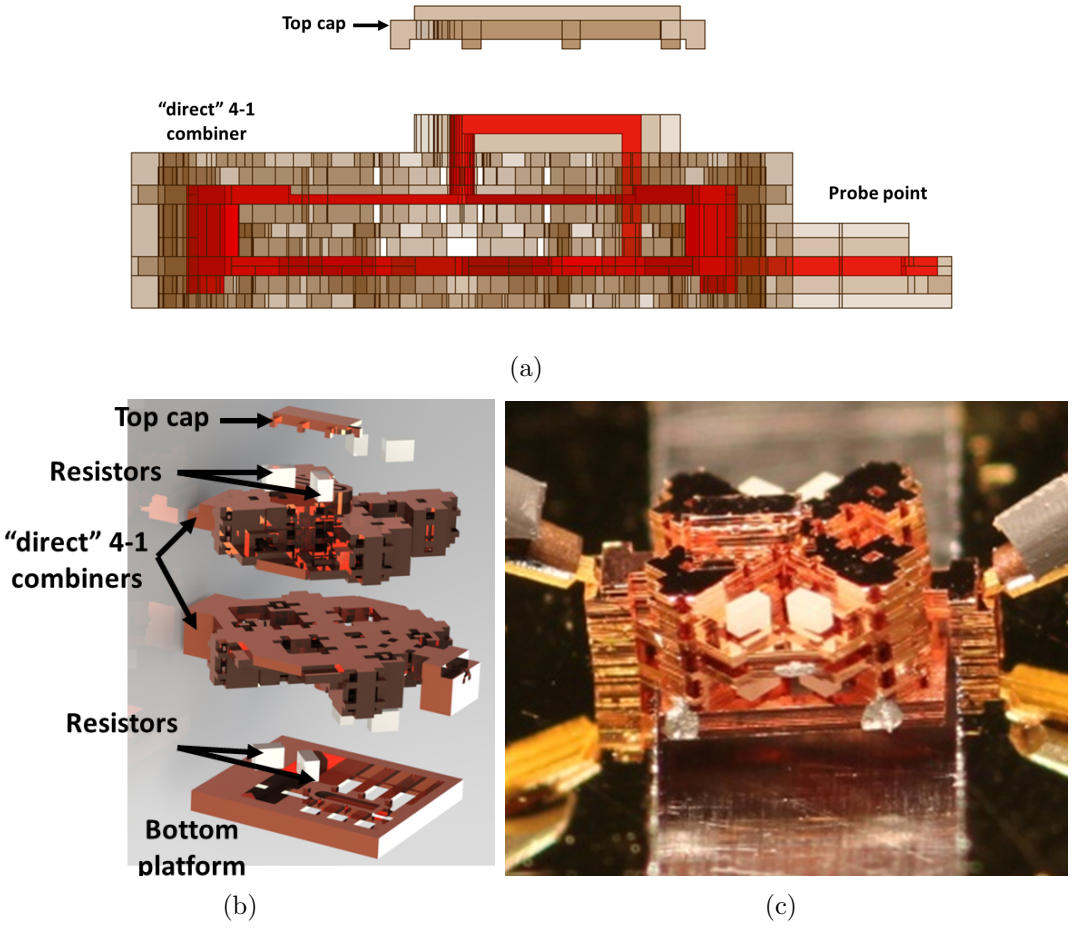


Figure 6.10. (a) (a) Side view of top combiner in back-to-back stack. A limited number of layers forced the top layer of coax to be a "partial" coax, which is made into a fully shielded coaxial line with the assembly of a "cap". (b) Assembly diagram of back to back direct 4-1 combiner. (c) Assembled back to back direct 4-1 combiner under test.

layers to the fabrication build. The outputs of the combiners were routed down flush with the bottom of the combining network. One of the two combiner structures had resistors assembled, and was flipped upside down. The second combiner was assembled on top of it. The probe point for the flipped combiner was fabricated in such a way that it could be probed when the part was assembled. The bottom combiner also had mechanical supports for the upper combiner's probe point attached. A detailed assembly drawing of the part and fully assembled part under test are shown in Figure 6.10. The measured results of the part are shown in Figure 6.11. Good correlation with simulation is shown for S21. Discrepancies

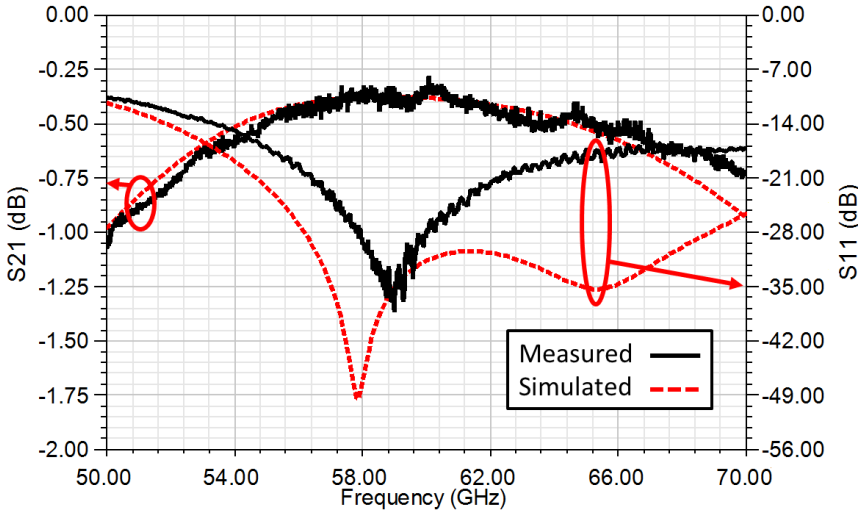


Figure 6.11. Measured vs. simulated results for back to back direct 4-1 combiner. Measured insertion loss and return loss are less than 0.35 dB and greater than 21 dB, respectively.

in S11 may be related to unaccounted for parasitics in the assembly of the resistors, the assembly of the two combiner structures and their caps, or the assembly of the two combiner structures to one another. Additionally, return loss may have been affected by the conditions under which the inputs were probed. The bottom cap assembly did not provide a perfectly flat surface for the probes to touch down upon.

6.4 W-band Rectangular Coaxial 2-1 Combiners

This section will examine various 2-way W-band rectangular coaxial power combining structures designed in the PolyStrata process, including reactive, Wilkinson and Gysel combiners. The 2-1 combiner is the most basic building block of more complex power combining networks needed for W-band SSPAs. In general, each of these devices can also be used equally well in a power splitting mode. This section and the one following it will provide a comprehensive overview of W-band rectangular coaxial combining structures.

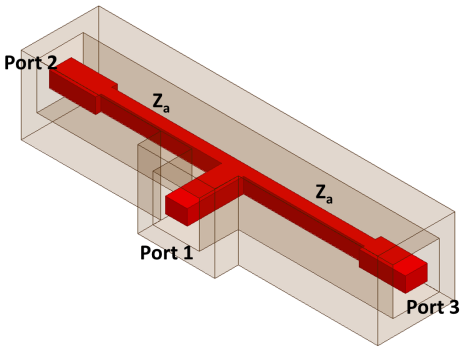


Figure 6.12. 3-D model of rectangular coaxial reactive combiner. Impedance of Z_a is 70.7 Ω

6.4.1 Reactive Divider

The simplest form of microwave passive divider is a T-junction, or reactive combiner as discussed in Section 6.1. A rectangular coaxial implementation of a reactive combiner is shown in Fig. 6.12. For a structure designed at 94 GHz, the length of each quarter-wave transformer is 798 μm.

The design shown in Fig. 6.12 is a 2-way combiner in a 50 Ω system, so the Z_a value is 70.7 Ω. The design shown has been optimized using Ansys HFSS 3-D FEM tools. The length of the Z_a segments from the center of the device is 850 μm (slightly longer than $\frac{\lambda}{4}$ at 94 GHz to compensate for junction parasitics). This dimension is optimized using the 3-D FEM tools to provide the lowest insertion loss at 94 GHz. While the design shown has outputs at right angles from the input, different output routing angles can also be used for the division. Since there are no load resistors, the outputs of the reactive divider can be routed more flexibly. This is in contrast to the more complex combining structures to be discussed later in this section. The inner dimension of outer conductor of the rectangular coax is 300 μm x 300 μm. Inner conductor dimensions are 100 μm x 142 μm for the 50 Ω segments, and 72 μm x 100 μm for the 70.7 Ω segments. The total volume of this combiner is 2.3 mm x 0.65 mm x 0.5 mm, or 0.75 mm^3.

The simulated performance of the reactive combiner is shown in Fig. 6.13. The simulated insertion loss at 94 GHz is 0.05 dB, and better than 0.1 dB across the W-band (75-110

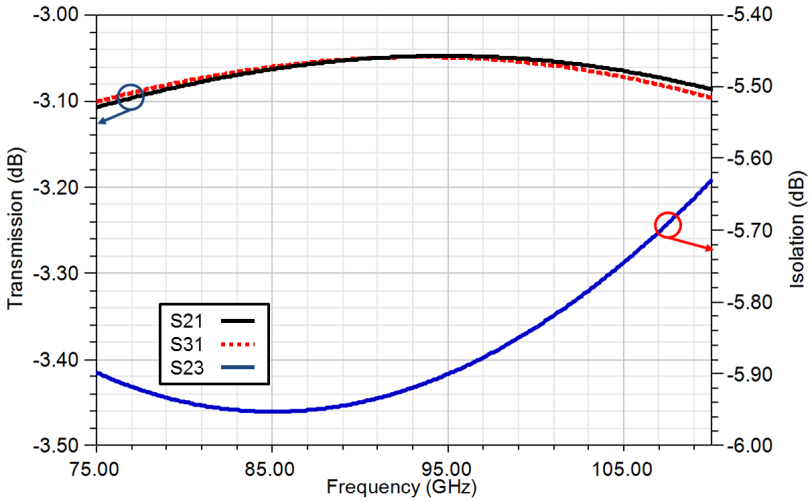
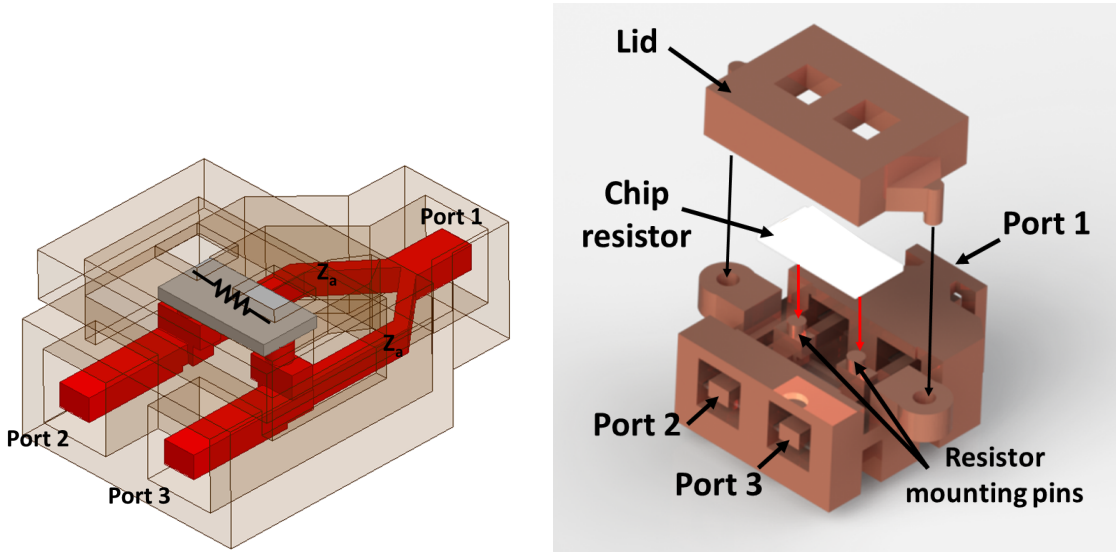


Figure 6.13. Simulated performance of 94 GHz reactive combiner. At 94 Ghz, the simulated insertion loss and isolation are 0.05 dB and 5.9 dB, respectively. The simulated results reflect splitting mode operation.

GHz). Despite the inherently narrowband nature of impedance transformers, the reactive combiner has a low insertion loss over a fairly wide band. However, the isolation between the output ports is only 5.9dB at 94 GHz, and 5.6 dB across the W-band. Isolation is important in a power combining system to prevent unwanted reflection of power into the outputs of the power MMICs. The poor isolation of reactive combiners coupled with a need for graceful degradation is often the driving factor in selecting a more complex power combining architecture, such as the Wilkinson or Gysel.

6.4.2 2-1 Wilkinson Combiner

An implementation of a 2-1 Wilkinson combiner in rectangular coax is shown in Fig. 6.14. As in Figure 6.2, the required Z_a impedance is 70.7Ω, and the required load resistor R1 value is 100Ω. The inner dimension of outer conductor of the rectangular coax is 300 μm x 300 μm. Inner conductor dimensions are 100 x 142 μm for the 50 Ω segments, and 72 μm x 100 μm for the 70.7 Ω segments. At the end of the Z_a impedance sections, posts are added to the center conductor which are flush with the top of the outer conductor. The outer conductor



(a) (b)

Figure 6.14. (a) 3-D Model of rectangular coaxial 94 GHz 2-1 Wilkinson combiner. Outer conductor is transparent (b) Assembly drawing of 2-1 Wilkinson combiner. The thinned chip resistor is flipped attached to the pins via a silver conductive epoxy. The metal shield is used to close the opening in the outer conductor and reduce radiation loss.

is removed around these posts to allow unobstructed chip resistor assembly.

This design uses a commercially available AlN resistor, connected with conductive epoxy. At W-band, however, the use of such resistors impacts performance significantly. The length of the resistor structure itself becomes electrically significant, so radiation and resonant loss become a factor. The resistor chip shown is thinned to 50 μm, to reduce substrate modes. Figure 6.14 shows the assembled Wilkinson combiner. A custom resistor could be fabricated to help alleviate some of the insertion loss caused by substrate moding. To prevent radiation loss, a 3-D metal lid is also necessary, with mechanical alignment features to aid in assembly. Figure 6.14b shows the assembly process.

The volume of this combiner is 1.3 mm x 1 mm x 0.675 mm, or 0.88 mm^3. Since the ends of the Z_a sections must be in proximity to each other for resistor assembly, additional output routing is often needed, which would further increase the footprint, as well as add loss into the system. In addition, the constraint of the resistor location forces the split at

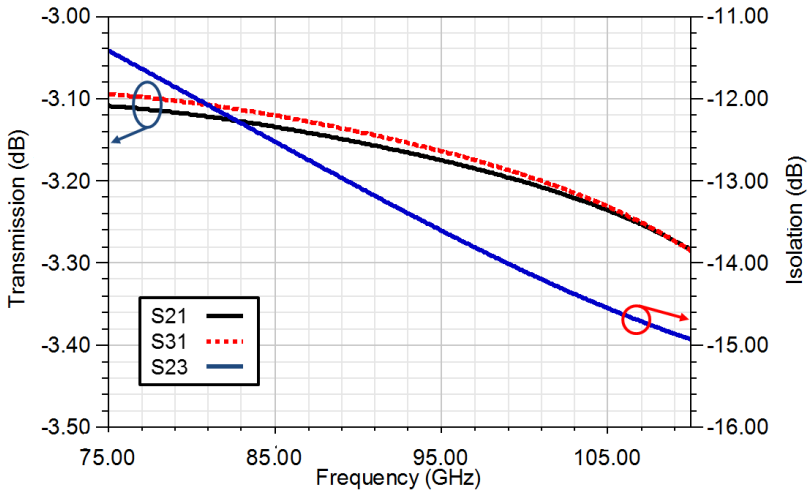
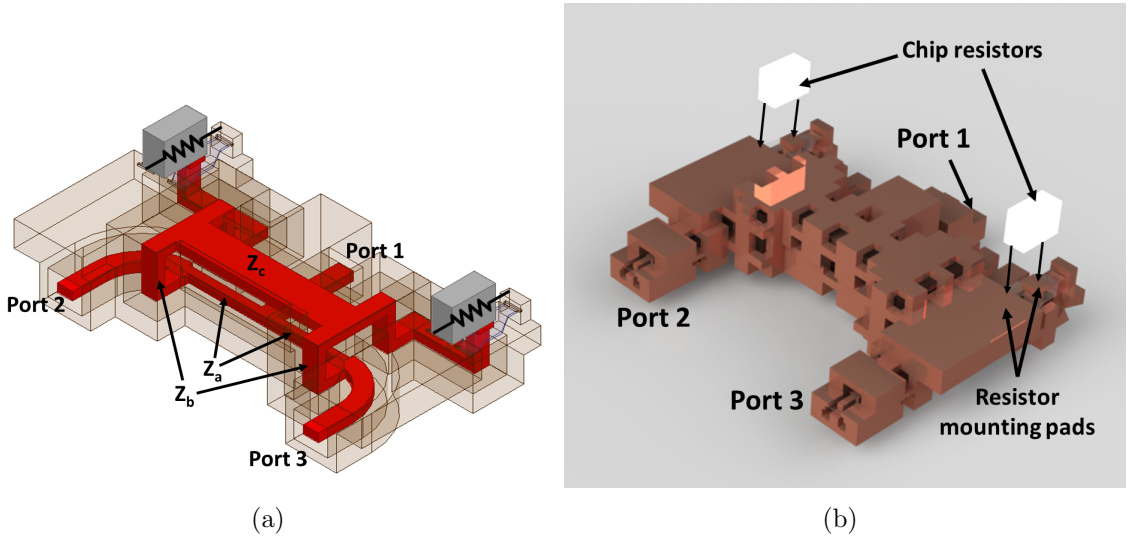


Figure 6.15. Simulated results for rectangular coaxial 2-1 Wilkinson power combiner. At 94 GHz, the simulated insertion loss and isolation are 0.18 dB and 13.5 dB, respectively. The simulated results reflect splitting mode operation.

the output to be at an angle which is less than 180°. In a 180° configuration (as shown for a reactive divider in Figure 6.12), the coupling between the two paths is minimized. Additional optimization at the junction was required to compensate for this. The simulated results of the 94 GHz Wilkinson combiner are shown in Fig. 6.15. At 94 GHz the simulated insertion loss is 0.18 dB, and the insertion loss is better than 0.28 dB loss for the entire W-band. The isolation is 13 dB at 94 GHz, and better than 11 dB across the W-band. There are a number of techniques to increase the bandwidth of a Wilkinson combiner, including the addition of input transformers, and multisection Wilkinson dividers. These techniques typically come at the expense of insertion loss, however, which is paramount in SSPA power combining applications.

6.4.3 2-1 Gysel Combiner

A rectangular coaxial implementation of the Gysel combiner using the optimized impedance values is shown in Fig. 6.16. The optimized impedance values are the same as those shown for the 60 GHz Gysel combiner in Table 6.1. The optimal R1 value is 75Ω. Each transmission



(a) (b)

Figure 6.16. (a) 3-D Model of rectangular coaxial 94 GHz 2-1 Gysel combiner. Outer conductor is transparent (b) Assembly drawing of 2-1 Wilkinson combiner. Two commercially available aluminum nitride resistors are assembled as loads with conductive epoxy.

line section is $\frac{\lambda}{4}$ in length (800 μm at 94 GHz).

This Gysel design takes advantage of the 3-D routing capabilities of rectangular coax for compactness and minimized input routing. Two monolithically fabricated layers of coax are used to place the Z_c impedance sections directly over the Z_a impedance sections. A vertical section of Z_b connects the Z_c and Z_a impedance sections . The transmission line section that routes to the resistor from Z_c is 50Ω, and its length has no impact on the performance of the circuit. Commercially available 0201 (500 μm x 250 μm x 375 μm) aluminum nitride resistors manufactured by US Microwaves are assembled using conductive silver epoxy. The resistor pads are routed flush with the top surface of the outer conductor, and the resistor is placed across the gap from the center conductor pad to an outer conductor.

The Wilkinson combiner shows significant detuning of its performance from the chip resistor substrate, which is compensated in the design. This means that the combiner performance is very sensitive to both the type and location of the resistor substrate. In contrast, the Gysel architecture is much less sensitive to the effects of the resistor substrate, and can accept virtually any resistor which has the correct value and pad footprints with little impact

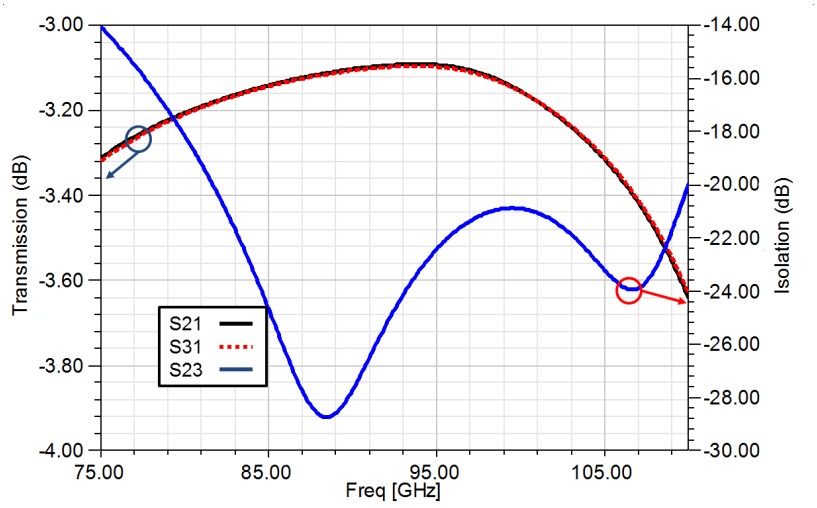
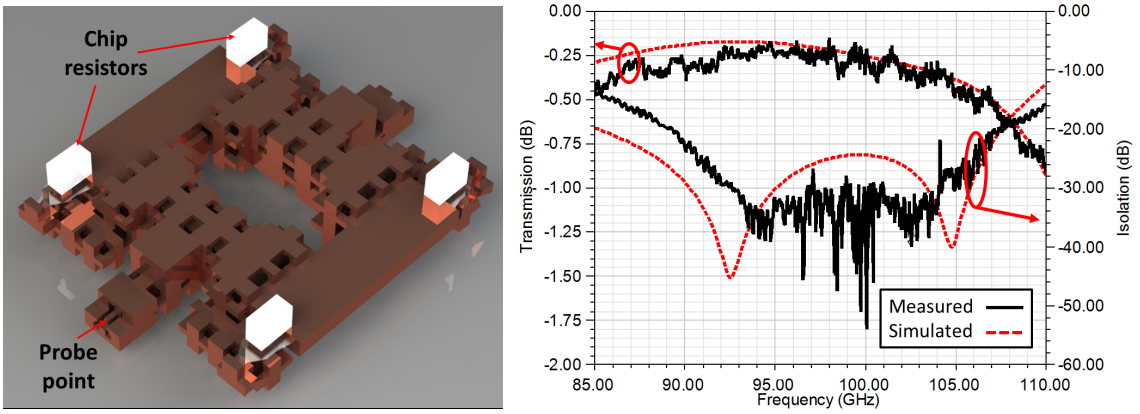


Figure 6.17. Simulated results for rectangular coaxial 2-1 Gysel power combiner. At 94 Ghz, the simulated insertion loss and isolation are 0.1 dB and 23 dB, respectively. The simulated results reflect splitting mode operation.

on performance. The assembly is shown in Fig. 6.16b. The overall volume occupied by this design is 4.1 mm x 1.86 mm x 1.08 mm, or 8.2 mm^3.

The simulated results for the 2-way Gysel combiner are shown in Fig. 6.17. The insertion loss at 94 GHz is 0.1 dB; however over the W-band the insertion loss becomes as high as 0.65 dB. The isolation at 94 GHz is 23 dB, and it is as high as 14 dB over the W-band. From this simulation, it is clear that the Gysel combiner has a narrower bandwidth than the Wilkinson or reactive combiners, but achieves a better isolation.

A back-to-back version of the 2-1 Gysel combiner was constructed, assembled, and measured. The back-to-back structure was designed to be probed using two 150 μm pitch GSG probes. The simulated insertion loss at 94 GHz is 0.25 dB for the total back-to-back structure ($\sim$ 0.1 dB per junction and 0.05 dB for additional routing to probe pads). The measured data (shown in Figure 6.18) correlates well with the simulated performance, with an insertion loss for the back-to-back structure of 0.3 dB at 94 GHz, and a return loss of better than 30 dB.



(a) (b)

Figure 6.18. (a) 3-D Model of back to back rectangular coaxial 94 GHz 2-1 Gysel combiner. (b) Measured results for 2-1 Gysel back to back combiners. Measured insertion loss is less than 0.3 dB at 94 GHz.

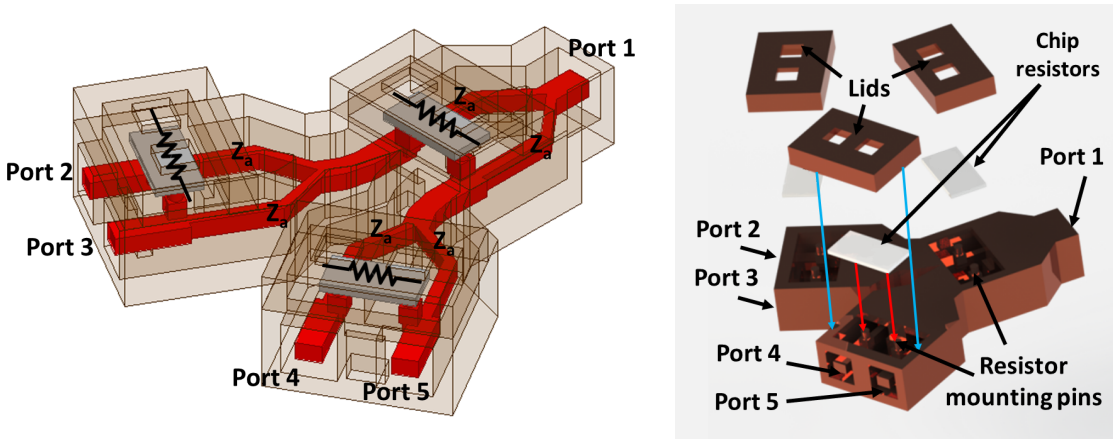
6.5 4-1 W-band Rectangular Coaxial Combiners

Section 6.4 outlined a number of basic 2-1 W-band combiner structures and their implementation in rectangular coax. This section will examine the extension of those topologies to different 4-1 combining architectures, including cascaded binary Wilkinson combiners, and 4-1 reactive, Wilkinson and Gysel combiner designs.

6.5.1 Cascaded Binary Wilkinson Combiners

One method for 4-1 combining is simply cascading of the various binary (2-1) combiners detailed in Section 6.4. Each of the combiner architectures outlined can be cascaded. In this section, we will examine the cascaded W-band Wilkinson binary combiners. An example of cascaded Gysel combiners (at 60 GHz) can be found in Section 6.3.2.

3-D models of cascaded binary Wilkinson combiners are shown in Fig. 6.19. The combiner bodies are identical to those related previously, with the thinned commercially available resistors with vias and radiation lid assembled onto each 2-1 junction. The lids and resistors are assembled in the manner described in Section 6.4.2. For the purposes of comparison, the



(a) (b)

Figure 6.19. (a) 3-D Model of cascaded binary rectangular coaxial Wilkinson combiners. Outer conductor is transparent (b) Assembly drawing of cascaded binary Wilkinson combiners

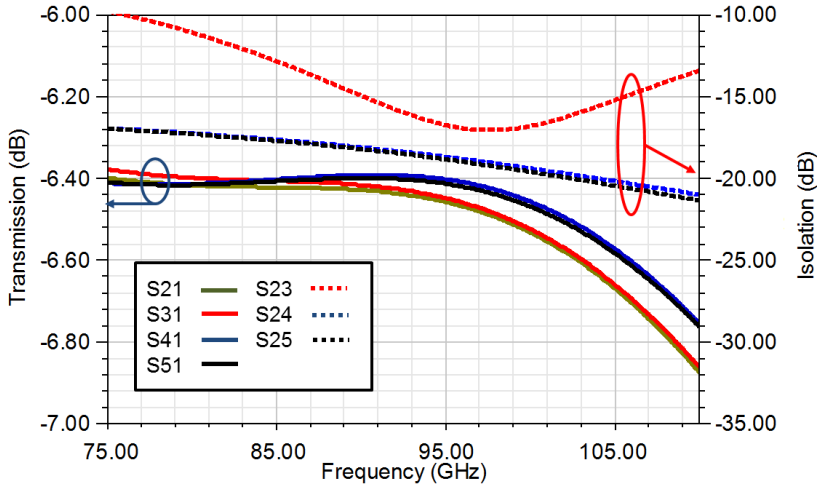


Figure 6.20. Simulated results of cascaded binary Wilkinson combiners. At 94 GHz, the simulated insertion loss is 0.22 dB and the isolation is 20 dB. The simulated results reflect splitting mode operation.

interconnection between the stages is minimized to reduce footprint and loss. The volume occupied by the cascaded Wilkinson combiners is 2.7 mm x 2.8 mm x 0.675 mm, or 5.1 mm^3. In an SSPA, longer routing between stages is used to accomodate chip footprints.

The simulated performance of the cascaded binary Wilkinson combiners is shown in Fig. 6.20. Simulated insertion loss and isolation at 94 GHz are 0.55 dB and 16 dB, respectively.

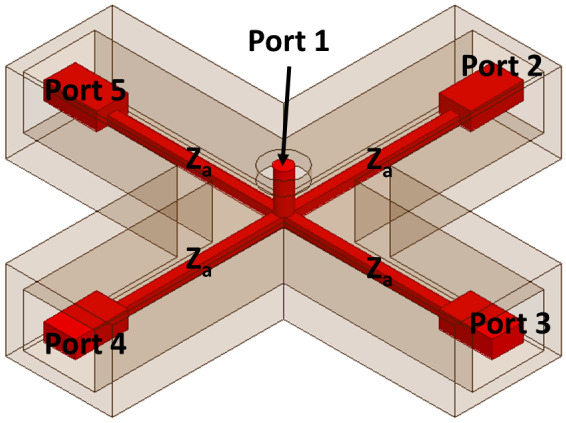


Figure 6.21. 3-D model of 4-1 reactive combiner. Outer conductor is transparent.

The insertion loss is, as expected, approximately two times the loss of a 2-1 junction, plus additional loss for routing between the two stages. For the W-band, overall insertion loss is less than 0.8 dB, and isolation is greater than 11 dB. The insertion loss variance between paths is related to the routing between stages.

Similar results can be obtained by cascading the 2-1 reactive and Gysel combiners previously discussed. However, an interesting alternative is a direct extension the 2-1 combining junctions of these various architectures to a 4-way combination.

6.5.2 4-1 Reactive Combiner

Again, the simplest 4-1 architecture is the reactive divider, of which the rectangular coax implementation is shown in Fig. 6.21. From Eqn. 6.2, Z_a is 100 Ω and the length of each Z_a impedance section is 0.9 mm from the center. For a 300 μm x 400 μm outer conductor cross-section, the inner conductor dimensions necessary to achieve this impedance are 50 μm x 55 μm.

The design in Fig. 6.21 is an X-shape, with each leg representing an input, and the output exiting the coax in the center of the X. This is the simplest design, but the reactive combiner can be routed in a number of more complex ways. For example, a planar design

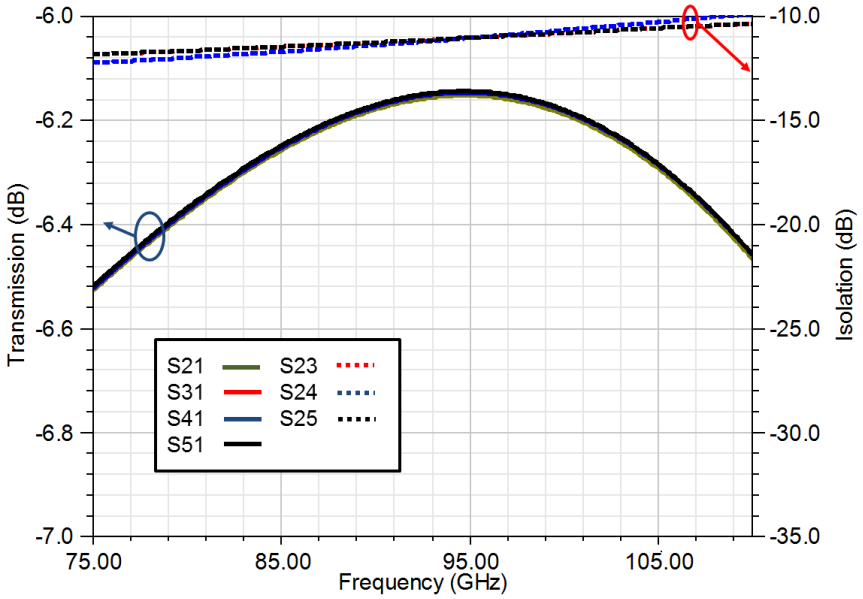


Figure 6.22. Simulated performance of 4-1 reactive combiner. At 94 GHz, the simulated insertion loss and isolation are 0.15 dB and 11 dB, respectively.

could be realized with the output moved from the top to the side and the inputs legs spaced at 60° intervals on the other half of the part. For the X-shaped design, the volume is 2.5 mm x 2.5 mm x 0.45 mm, or 2.8 mm^3.

The simulated results of the 4-1 reactive divider are shown in Fig. 6.22. At 94 GHz, the simulated insertion loss and isolation are 0.15 dB and 11 dB, respectively. Over the W-band, the insertion loss is 0.46 dB and the isolation is greater than 10 dB.

6.5.3 4-1 Wilkinson

Fig 6.23a shows the extension of the 2-1 Wilkinson combiner circuit shown in 6.2 to a 4-1 combiner. As in the previous section, Z_a is 100 Ω and the length of each Z_a impedance section is 0.9 mm from the center. This particular layout has four individual resistors, each one between two different legs of the combiner. The value of R1 for an N-way combiner is $NZ_0\Omega$. This configuration of resistors is referred to here as a "delta" configuration.

The delta configuration of resistors places considerable restrictions on the layout of the

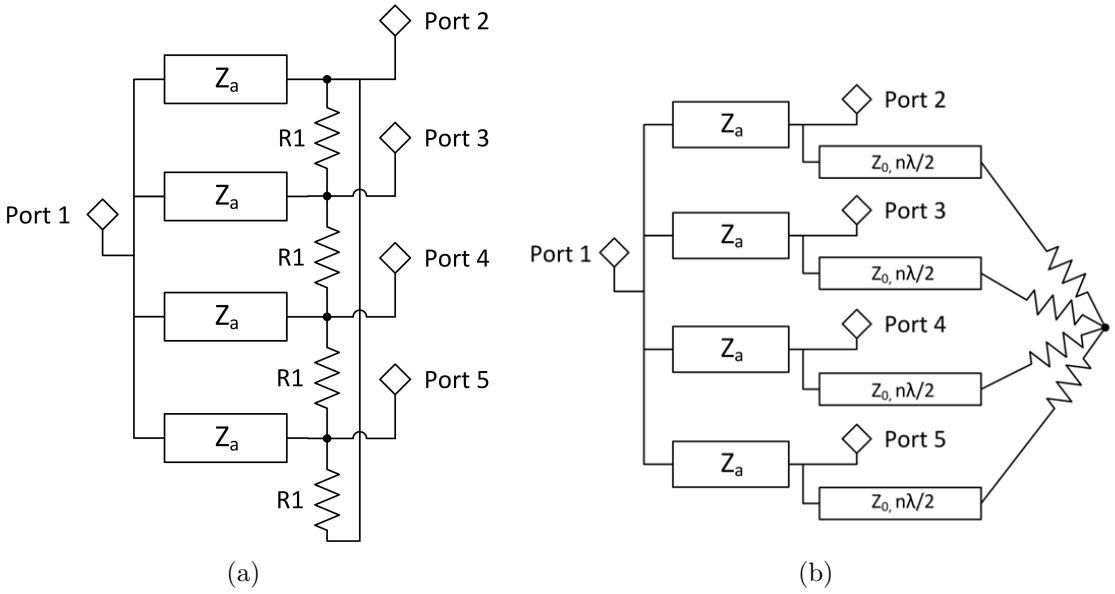
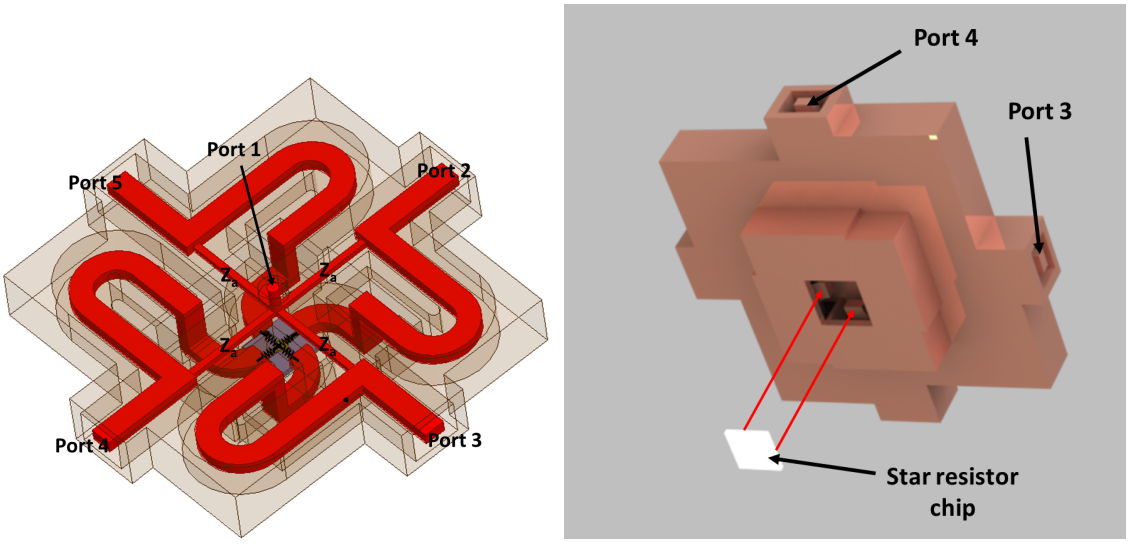


Figure 6.23. (a) Circuit diagram of a 4-way Wilkinson combine with termination resistors in a "delta" configuration. (b) Circuit diagram of a 4-way Wilkinson combiner with termination resistors in "star" configuration. $\frac{n\lambda}{2}$ sections of Z_0 are used to route from the inputs to the resistor for a radial combiner.

combiners. Each leg is forced to be in close proximity to all other legs at two separate points, at the junction and at the isolation resistors. It is really only possible in a radial configuration. One popular alternative to this is the "star" configuration of resistors [131]. This configuration is derived by performing a delta-wye transformation on the resistor network. This allows all of the resistors to be combined into a single custom, star-shaped chip resistor, with each leg's impedance equal to Z_0. A further extension of this design is shown in Fig. 6.23b. To improve routing capabilities, a $\frac{n\lambda}{2}$ section of Z_0 transmission line is used to connect the resistor to each input. This has additional benefit for a 94 GHz combiner, because it allows the resistor lengths to be electrically small.

Fig. 6.24 shows a rectangular coaxial implementation of this design. An input is located on each leg of the X shape, and the output (Port 1) is located in the center of the X. The custom, star-shaped resistor interface point is located on a lower level of coax, directly below Port 1. This particular implementation uses a full wavelength (320 μm at 94 GHz) of transmission line to connect to the star shaped resistor pads from the input ports. The



(a) (b)

Figure 6.24. (a) 3-D Model of rectangular coaxial 94 GHz 4-1 Wilkinson combiner. Outer conductor is transparent (b) Assembly drawing of 4-1 Wilkinson combiner.

star-shaped resistor is fabricated with NiCr on a 50 μm thick alumina substrate. The overall volume occupied by the 4-1 Wilkinson combiner is 3 mm x 3 mm x 0.825 mm, or 7.65 mm^3.

The simulated performance of the 4-1 Wilkinson combiner is shown in Fig. 6.25. The simulated insertion loss at 94 GHz is 0.16 dB, and simulated isolation is 14 dB. From 87 to 110 GHz, the insertion loss is less than 0.32 dB, and the isolation is better than 11 dB. The precipitous drop off at lower frequencies is due to a null at 70 GHz where the 320 μm section of transmission line connecting the inputs to the resistor has an electrical length of $\frac{3\lambda}{4}$. If a $\frac{\lambda}{2}$ routing could be used, the nulls would occur at 50 and 125 GHz, making the combiner significantly wider band.

6.5.4 4-1 Gysel

A 4-1 extension of the Gysel architecture is shown in Fig. 6.8. The optimized impedance values from Table 6.2 were developed using HFSS simulations of the rectangular coaxial implementation. The optimal R1 value is 100 Ω. Fig. 6.26 represents the W-band imple-

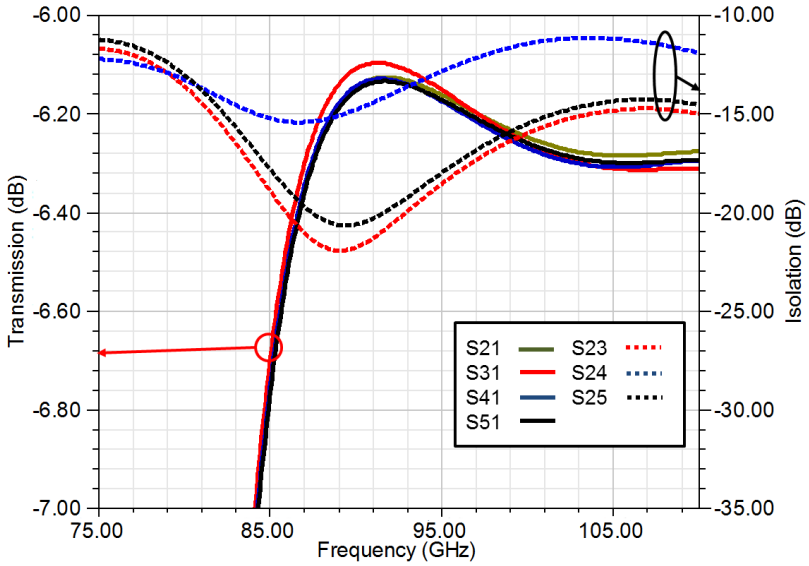
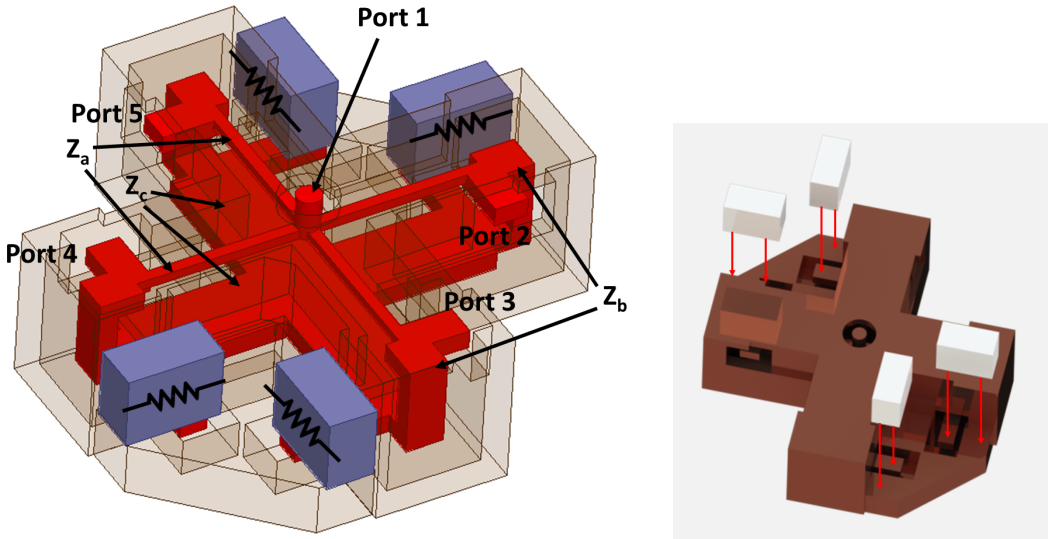


Figure 6.25. Simulated results of a 4-way Wilkinson combiner. At 94 GHz, the simulated insertion loss is 0.16 dB and the isolation is 14 dB. The simulated results reflect splitting mode operation.



(a) (b)

Figure 6.26. (a) 3-D Model of rectangular coaxial 94 GHz 4-1 Gysel combiner. Outer conductor is transparent (b) Assembly drawing of 4-1 Gysel combiner.

mentation, realized in rectangular coax.

Once again, the structure is designed in an X-shape. Each of the inputs is located on

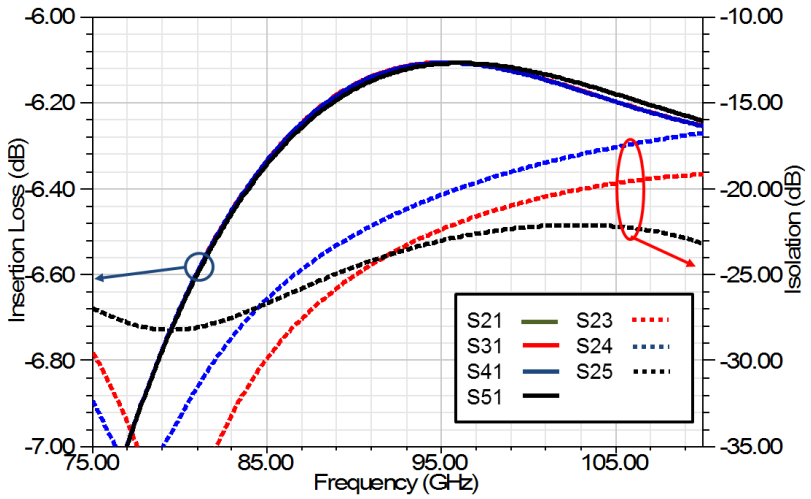


Figure 6.27. Simulated results of a 4-way Gysel combiner. At 94 GHz, the simulated insertion loss is 0.11 dB and the isolation is 20.5 dB.

the side of the top layer of rectangular coax one-third of the way from the end of each leg. From the input, each leg is connected to the output (Port 1) in the center of the X via the Z_a sections directly. The Z_b sections are used to transition down to the lower layer of coax, where all of the Z_c sections meet together in the middle, directly underneath Port 1. Four 100 Ω commercially available 250 μm x 500 μm x 375 μm (0201) aluminum nitride resistors manufactured by US Microwaves are assembled onto the combiner. On each leg, a resistor is attached to a short section of coax which exits the side of the outer conductor at the point on the lower layer where the Z_b impedance section transition to the Z_c impedance sections. The other end of each resistor is connected to the system ground, which is the outer conductor of the rectangular coax. The overall volume occupied by the 4-1 Gysel combiner is 2.4 mm x 2.4 mm x 0.875 mm, or 5 mm^3.

The simulation results for this design can be found in Fig. 6.27. At 94 GHz, the simulated insertion loss is 0.11 dB and the isolation is 20.5 dB. From 87-110 GHz, the insertion loss is less than 0.28 dB and the isolation is greater than 17 dB.

6.6 Rectangular Coax Power Combiner Based W-band SSPAs

The next step in this work was the integration of the rectangular coax combiner designs into a W-band SSPA platform. Fig. 6.28 shows a combining platform designed for InP LSPA2 W-band medium-power amplifier MMICs from HRL. The lack of commercially available W-band PA MMICs was a key factor in the selection of these MMICs for combining: they had the distinction of having the highest power output at 94 GHz of any commercial MMIC at the time (13 dBm typical).

The SSPA consisted of a W-band waveguide backshort input and output of the sort designed in Section 2.5, with a copper platform for a driver amp (in this case, designed using another LSPA2 MMIC as the driver), input and output cascaded Wilkinson combiners, and platforms for the power combined chips and their accompanying decoupling capacitors for the DC bias lines. The decoupling capacitor layout was based on the MMIC datasheet, with two shunt single-layer ceramic capacitors (10 pF and 100 pF) for each of three V_g pads and three V_d pads. DC routing for the chips was done using traces on the alumina substrate and grounded CPW structures in PolyStrata for crossing over the combiners. All of the MMIC V_g bias lines were tied together, and all of the V_{DD} bias lines were tied together, to simplify control. The V_{DD} voltage was 2.0V, with a V_g range of 0 to -1.0 V, and an optimal quiescent current of 120 mA. The MMIC has a PAE of 14% in saturation. The footprint of the MMICs is 1.25 mm x 2.06 mm and the chips were thinned to 50 μm thickness.

The combiners are cascaded Wilkinson dividers, with phase matched routing on the inputs. This combiner was selected for the simple reason that it only required 6 strata for fabrication, and could have the DC lines monolithically routed over it in a single build. The cascaded Wilkinson is an older iteration than the one shown in Sec. 6.5.1 which uses AlN resistors. The resistors are manufactured by US Microwaves. The resistor (part number USMRG1020AN10-101) has a volume of 254 μm x 508 μm x 254 μm. RF and DC inter-

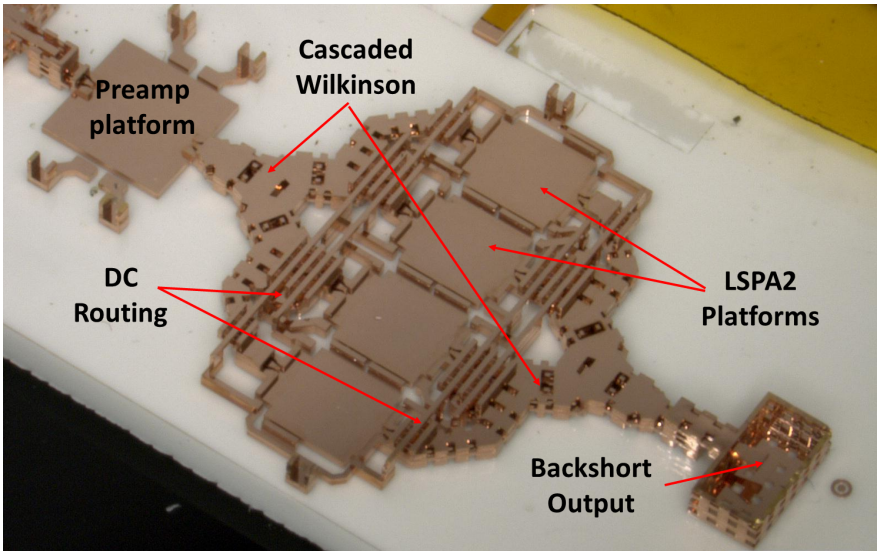


Figure 6.28. Fabricated preliminary 94 GHz SSPA platform.

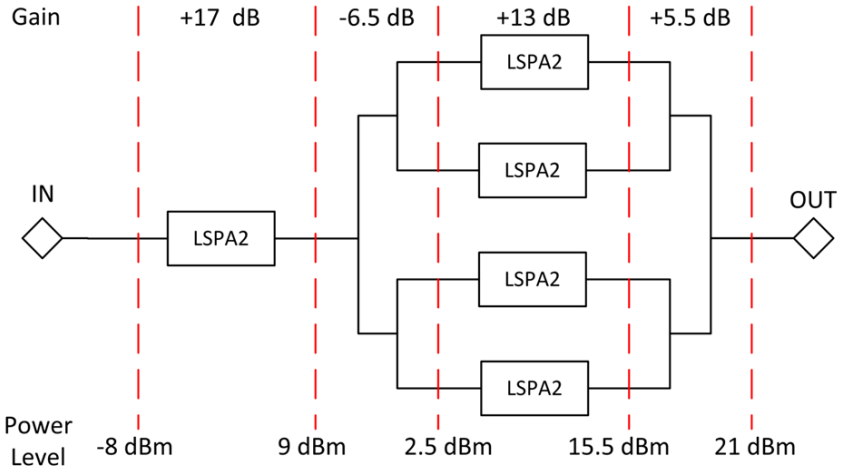


Figure 6.29. Block diagram of expected SSPA performance.

connections were made using wirebonds. The total volume of the first generation combiner platform was 19.5 mm x 10.78 mm x 0.745 mm, or 367 mm^3, including the 1mm thick alumina substrate to which the part was attached for structural support and DC routing.

Figure 6.29 shows a block diagram and power/gain budget of the SSPA platform when populated with HRL InP LSPA2 PA MMICs. The MMIC performance is taken from the manufacturer's data sheet [132]. A power of -8 dBm is provided at the input of the driver

MMIC from an external source. The driver provides 17 dB of gain to the signal, resulting in +9 dBm at the input to the PolyStrata 1-4 divider. 6 dB of dividing loss, along with 0.5 dB insertion loss from the divider results in 2.5 dBm at the input of each amplifier MMIC. This input power drives the amplifiers into saturation, and only 13 dB of gain is provided by each MMIC. Given the 6 dB 4-1 combining gain and 0.5 dB insertion loss in the output combiner, the total expected output power of the SSPA platform is +21 dBm (130 mW). The expected PAE for the SSPA platform is 10%. At the time of this writing, measured results from the populated SSPA were not available for publication.

6.7 Conclusions

This chapter has presented a series of mm-wave combiner designs for the realization of rectangular-coaxially based W-band SSPAs. Simulated and measured results for three separate 60 GHz rectangular coaxial power combiner circuits were presented. A series of designs for W-band combining were also presented, including 2-1 and 4-1 implementations of Wilkinsons, Gysels and reactive combiners.

Table 6.3 provides a comprehensive comparison of all of the designs realized. Each design has its own particular advantages, depending on the application. The table includes numbers for insertion loss and isolation at 94 GHz for the W-band combiners and at 60 GHz for the V-band combiners, as well as the volume required for each combiner structure. The bandwidth is defined as the frequency range over which the insertion loss degrades 0.1 dB from its minimum value. A field denoting the need for custom resistors and the quantity of resistors required is also included. Finally, three more subjective fields are included: assembly, thermal, and routing flexibility. The numbers in these columns represent rankings according to ease of assembly (1 being the easiest), generalized thermal performance (1 being best) and flexibility of routing (1 being most flexible).

For two-way combining, the reactive combiner has the minimum loss, footprint, and

greatest bandwidth, but is hindered by the poor isolation inherent in a reactive combining network. The Gysel has better isolation, a better thermal path to ground, and significantly simpler assembly than the Wilkinson, but it has a significantly larger footprint, and narrower bandwidth.

For four-way combining, the cascaded Wilkinson is attractive given only six strata, allowing monolithic integration of a second layer of routing coax or DC lines, and has a large bandwidth. However, it has the highest insertion loss and is relatively difficult to assemble. The reactive divider, being the simplest, is easy to assemble and has good insertion loss and bandwidth, but is still hampered by its relatively poor isolation performance. The 4-1 Gysel has the best insertion loss and isolation performance, as well as the best thermal performance, but relatively narrow bandwidth and difficult input routing. The Wilkinson 4-way is perhaps the least attractive, with the largest footprint, poorest bandwidth, and need for a custom "star" resistor.

There are a few examples of W-band combining networks and SSPAs available in the literature. The work in [133] illustrates the difficulty in using on-chip metal layers for power combining networks. The 2-way Wilkinson combiner used had 3.25 dB insertion loss at 80 GHz. Micromachined finite ground coplanar waveguides (MFGCW) are used to design combining networks in [134]. Measured insertion losses of 0.9 dB and 2.1 dB are reported for 2-1 and 4-1 combiners at 90 GHz, respectively. These numbers iclude routing loss, however, and the estimated insertion loss for a single binary Wilkinson combiner using the MFGCW is 0.5 dB. While the both of these combiners are slightly more compact than the comparable PolyStrata combiners presented in this work, they both also have significantly more loss at W-band.

In [135], a 5-W SSPA at 95 GHz based on a radial combiner is presented. The SSPA combines GaN MMICs to reach its 5-W output power. A combining efficiency of 87.5% for a 12-way SSPA was reported in a footprint of 6.73 in^3 with a combining loss of 0.6 dB. While it is somewhat inaccurate to compare the combiners discussed herein to the entire

SSPA reported in [135], it is worth noting that the SSPA is six orders of magnitude the size of the combiners discussed here (100000 mm^3), and has a comparable insertion loss to the rectangular coaxial combiners discussed here.

From these examples, it is clear that the V- and W- band rectangular coaxial combiners have a combination of compact size and insertion loss at mm-wave that is unmatched in the literature. This chapter has also detailed the extension of these combining architectures into a preliminary W-band SSPA platform. The use of rectangular coaxial technology for the creation of corporate combining networks gives an attractive platform for the creation of W-band SSPAs for mm-wave radar transmitter applications.

Table 6.3. Combiner Comparisons

	Insertion Loss	BW	Isolation	Volume	Custom Resistors? (Qty)	Assembly	Thermal	Routing flexibility
V-band PolyStrata combiners (60 GHz center frequency)								
2-way Gysel	0.12dB	16 GHz	23 dB	12.6 mm^3	N (2)	-	-	-
Cascaded Gysel	0.3dB	11 GHz	14 dB	67.7 mm^3	Y (6)	-	-	-
4-way Gysel	0.13 dB	12GHz	20.5 dB	15 mm^3	N (4)	-	-	-
W-band PolyStrata combiners (94 GHz center frequency)								
2-way								
Reactive	*0.05 dB*	*35+ GHz*	*5.6 dB*	0.7475 mm^3	N (0)	1	3	1
Wilkinson	*0.18 dB*	*25 GHz*	*13.5 dB*	0.8775 mm^3	Y (1)	3	2	3
Gysel	0.1dB	20 GHz	*23 dB*	8.2 mm^3	N (2)	2	1	2
4-way								
Cascaded	*0.55 dB*	*25 GHz*	*16 dB*	5.1 mm^3	Y(3)	4	3	2
Reactive	*0.15 dB*	*20 GHz*	*11 dB*	2.81 mm^3	N	1	4	1
Wilkinson	*0.6 dB*	*14 GHz*	*14 dB*	7.65 mm^3	Y(1)	4	3	3
Gysel	*0.11 dB*	*14 GHz*	*20.5 dB*	5.04 mm^3	N(4)	2	1	3
Combiners from literature								
95 GHz 2-1 Wilk [133]	3.25dB	-	-	<0.1 mm^3	-	-	-	-
90 GHz 2-1 Wilk [134]	0.5 dB	-	-	∼1.1 mm^3	-	-	-	-
95 GHz 12-1 radial [135]	0.6 dB	-	-	125,000 mm^3*	-	-	-	-

simulated results denoted in italics

* size provided for a full, packaged SSPA

Chapter 7

Conclusions

This chapter will summarize the work presented in this dissertation and its contributions to the field, and suggest future work stemming from this work. Two conceptual miniaturized mm-wave monopulse radar transceiver architectures will be presented and additional component research and development necessary for their construction will be discussed.

7.1 Summary and Contributions

This dissertation has presented the conception and development of a variety of components necessary for the realization of compact mm-wave tracking monopulse radar transceivers. In many cases, these results represent significant performance increases or size reductions from the published state-of-the-art components. Contributions of this work include:

- Design, simulation, and testing of novel 94 GHz cavity-backed patch antennas. The simulated maximum gain of a single antenna at broadside is 8.3 dB, with a radiation efficiency of 95% and a 3-dB beamwidth of 76° in the E-plane. Simulations of the array indicate an overall gain of the antenna array of 13 dB broadside, and a 3-dB beamwidth of 42°. Measured results correlate well with full-wave EM simulations.

This work represents the first published results of a W-band rectangular-coaxially based antenna array to date.

- Development of a novel W-band transition from rectangular coaxial transmission line to WR-10 waveguide. The simulated insertion loss for the transition is 0.08 dB at 94 GHz. A rectangular coaxial transition to waveguide is critical for high-power W-band systems. To date, no other results for a waveguide to rectangular coax transition have been published.

- The first demonstration of the hybrid integration of discrete diodes with rectangular coaxial transmission lines to implement a 94 GHz diode detector. An integrated high Z-low Z low-pass filter is included to block RF leakage to the DC pad.

- The design, simulation and characterization of a W-band 4-port rectangular coaxial passive monopulse receiver. This includes antennas, a monopulse comparator based on four rectangular coaxial rat-race hybrids, integrated diode detectors, and output low-pass filters. A measured AZ null of 31.4 dB and an EL null of 22 dB were reported at 94 GHz. This work represents the first demonstration of a rectangular coaxial based monopulse comparator system, and to date is the most complex rectangular coaxial W-band system ever fabricated using the PolyStrata process.

- Design and simulation of a W-band active RF monopulse comparator in the IBM 8HP SiGe process. An active monopulse comparator extends the functionality of a passive monopulse comparator over a wider range of frequencies, and with the addition of gain, which may be critical for system link budgets. Simulation results showed a 33 dB difference null and -4 dB insertion loss in the SUM pattern. Simulations also indicated potential wideband performance, with a difference null of greater than 31.5 dB simulated for 75-105 GHz. The MMIC was not able to be tested due to an error in routing the DC control voltages to the pads. To date, there have been no published implementations of W-band active RF comparator ICs.

- Design and simulation of a 94 GHz active phase shifter in the IBM 8HP SiGe technology. Measurements of the phase shifter were believed to have been hampered by unforeseen oscillations on the DC bias lines.

- Extension of the concept of an active RF comparator to 4 ports, including the design and simulation of a 24 GHz comparator RFIC in IBM 130 nm RF-CMOS technology. Simulated nulls of 71 dB and 68 dB were reported for the azimuthal and elevational sweeps, respectively. There have been no published 4-port active monopulse comparator MMIC results published to date at mm-wave frequencies.

- Demonstration of a number of novel low-loss rectangular-coaxially based V- and W-band combiner/dividers for power combining/splitting. These combiners represent a highly compact alternative to currently available waveguide and spatial combiners at W-band. The low insertion loss of rectangular-coaxial based transmission lines relative to traditional planar transmission line technologies presents a compelling case for the realization of mm-wave corporate power combiners, an architecture which has historically been impractical for high performance power amplifiers at mm-wave. To date, no W-band corporate combiners with lower insertion loss and smaller footprint have been published.

7.2 Future Work

There are a number of opportunites for future work stemming from the work presented in this dissertation:

- The antenna design work could be scaled to much larger arrays for higher overall gain and increased flexibility of the aperture. Of particular interest is the direct integration of a PolyStrata antenna array with active devices at a wafer-scale which could be used to create extremely compact mm-wave ESAs.

- An additional iteration of the passive monopulse comparator discussed in Section 3.5, focusing on mitigation of the unexplained variance in the elevational pattern, would be a desirable intermediate step for realizing a passive monopulse transceiver system.
- The redesign and full characterization of the active comparator RFICs/MMICs described in Chapters 4 and 5 would be an essential next step for the design of a monopulse transceiver system which uses active RFICs/MMICs as its basis.
- Ideally, the active monopulse comparator RFIC/MMIC efforts Chapters 4 and 5 could be extended to an implementation of a 4-port, 94 GHz active monopulse comparator IC. Additional functionality, such as mixers, detectors, and automatic gain control could also be integrated onto a single RFIC/MMIC. Differential Polystrata antennas would be ideal for integrating with such an RFIC/MMIC, to eliminate the need for conversion from single-ended to differential signals for processing.
- Further efforts to integrate the power combiners outlined in Chapter 6 with PA MMICs is also critical to the transmit side of these proposed systems, and is ongoing.
- The optimization of flip-chip integration of RFICs and MMICs with PolyStrata structures is an area deserving of further study. Flip-chip integration allows the elimination of wire-bonds, and the loss/tuning associated with them.

The final sections of this chapter will examine two conceptual systems building on the work in this dissertation: one which utilizes the passive monopulse architecture to create a "staring" array, and a system which extends the active comparator concept to a fullly steerable electronically steerable array (ESA) based transceiver.

7.2.1 Passive Monopulse Transceiver

The passive monopulse transceiver in this section is envisioned as a lower-cost alternative to ESA-based systems. The passive system would ideally be used for UAV applications

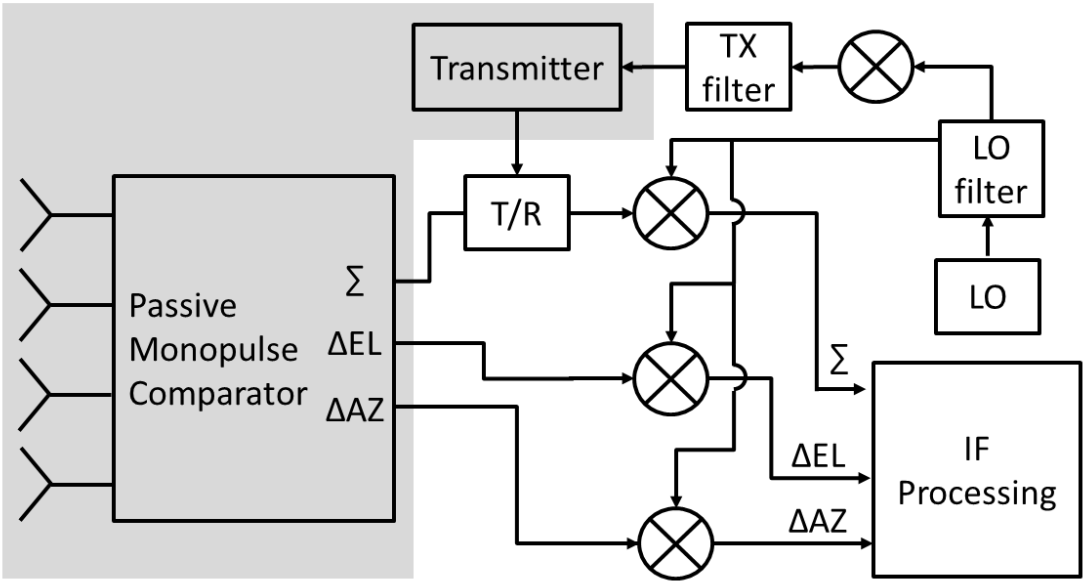


Figure 7.1. Block diagram of a conceptual passive monopulse transceiver. Grey components indicate those developed in this dissertation.

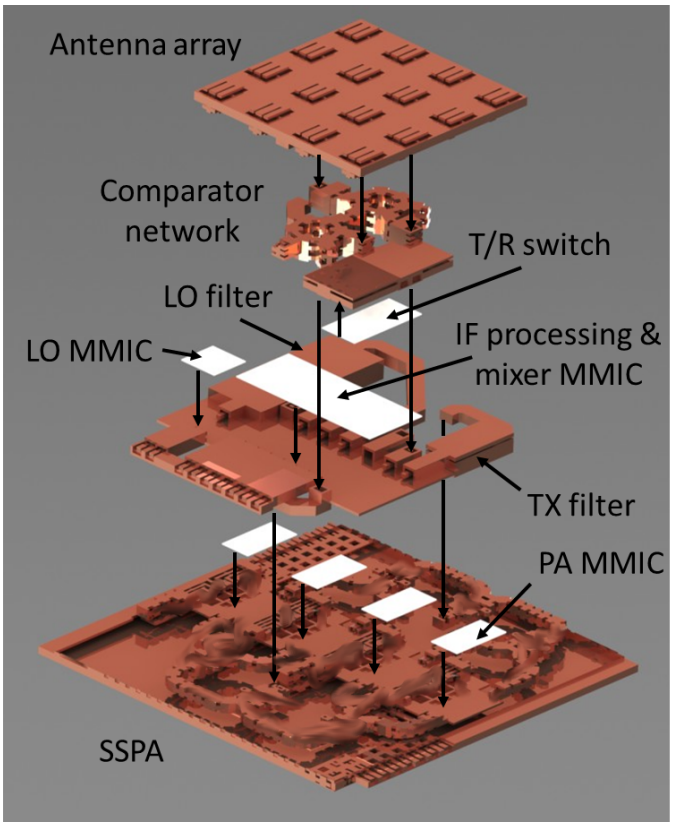
such as collison avoidance and communications tracking, where size, weight, and power consumption requirements are paramount. A block diagram of the conceptual system is shown in Figure 7.1. While the monopulse comparator, transmitter module and antennas have been researched in this dissertation (and are represented in grey in the block diagram), there are several component blocks of this system which would require further development. These include mixers, filters, and the transmit/receive (T/R) switch.

Depending on the intermediate frequency (IF), commercially available MMICs could be used for the IF receiver processing and the local oscillator (LO) blocks. These components would need to be integrated within a rectangular coaxial structure, an approach which has already been demonstrated in previous work at microwave frequencies. The LO and pre-power amplifier filters would need to be scaled from designs developed for lower frequencies. The PolyStrata-based resonant cavity filters demonstrated previously ([56] [136] [137]) represent a significant size reduction over waveguide or YIG filters, while maintaining a high level of performance.

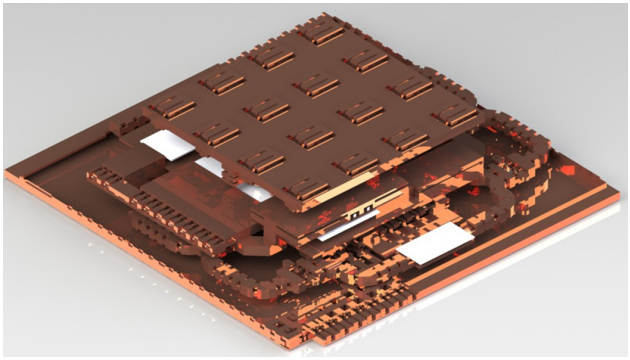
The necessary mixers could be developed in one of two ways: a custom MMIC or a hybrid circuit using commercially available diodes. Both approaches have their advantages. The custom MMIC approach would likely provide a performance improvement over the diode-based mixers, and could potentially reduce the overall size of the mixers by combining several or all of the necessary mixer blocks onto a single MMIC. Additionally, the potential integration of LNAs with the mixers on a single die is quite attractive. However, given the development cycle necessary for this type of mm-wave custom MMIC, it may be more straightforward to assemble the mixers based on commercially available diodes. The diode sockets used in Chapters 2 and 3 could be adapted to implement a double balanced mixer or a subharmonic mixers

The T/R switch also presents a challenge for development. A solid-state switch capable of handling the required power and provide the necessary isolation to an LNA is challenging at mm-wave. However, this is an active area of research [138] [139]. Another attractive option may include MEMS switches [140], or some combination of RF-MEMS and rectangular coaxial routing for lower insertion loss. Alternatives to the T/R switch include circulators and isolators. Efforts to create miniaturized circulators have been underway for many years [141] [142]. However, they require the integration of ferrite materials for high-performance operation. A hybrid rectangular coax-ferrite device could provide a high-performance miniaturized circulator or isolator.

A rendering of the passive monopulse transceiver is shown in Figure 7.2. The conceptual transceiver consists of four rectangular coaxial structures stacked together. Mechanical supporting structures are omitted from each layer to clearly show the functionality. The bottom layer is an SSPA, combining four GaN MMICs. The SSPA is on the bottom layer so that the heat that it generates can be easily dissipated. The input to the combining network comes from the TX filter (a resonant cavity filter fabricated in the PolyStrata process) located on the second layer. A final implementation would likely include several stages of preamplification before the final transmit stage. The output of the transmitter is routed through the second layer to the T/R switch on the third layer. DC control for the PA MMICs is routed



(a)



(b)

Figure 7.2. (a) Exploded drawing of a conceptual compact passive monopulse receiver. Three layers of PolyStrata passive devices and four detector diodes are used in its assembly. (b) Assembled conceptual compact monopulse receiver. The total footprint is 14.2 mm x 14.6 mm x 3.4 mm.

to the outside edges, for wirebonding or the attachment of a flex-circuit to a control board.

For simplicity, all of the IF processing functionality and mixers have been combined

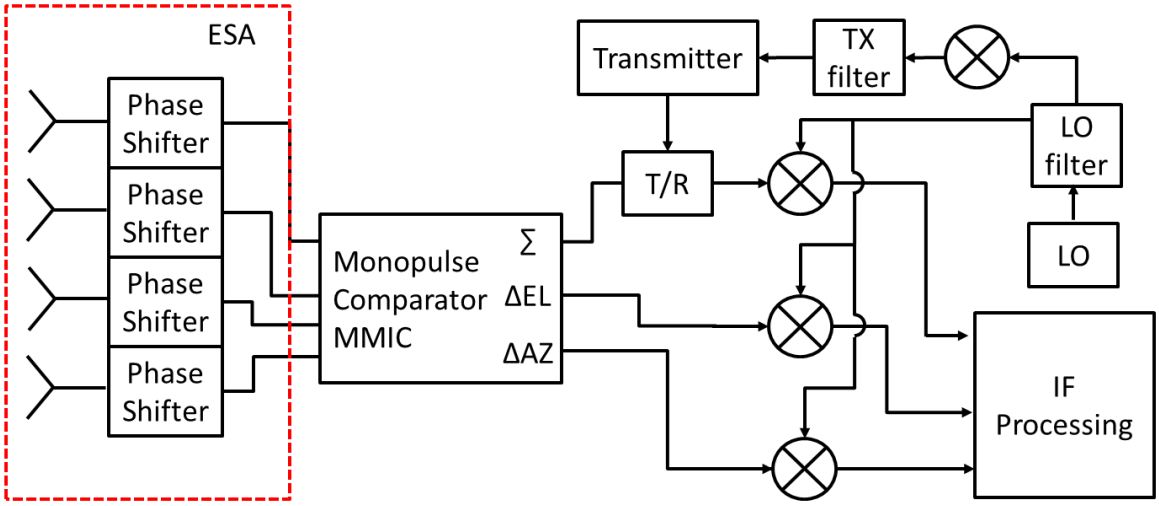


Figure 7.3. Block diagram of active monopulse transceiver

into a single custom MMIC on the second layer. The output from a separate, smaller LO MMIC is fed through a PolyStrata resonant cavity filter to the large processor MMIC. The IF processing MMIC also takes in all of the outputs of the monopulse comparator network, and outputs the TX signal prior to the TX filter. DC lines and the IF output are routed to the edge of the part for attachment to a control board.

The third layer contains the passive monopulse comparator network and the T/R switch, whose output is routed into the SUM port of the monopulse comparator for distribution to the antennas. For this concept, the T/R switch is represented as a MMIC, though that may not be the case in practice. To increase the gain, an array of 4 x 4 cavity-backed patch antennas makes up the fourth and final layer. Each 2x2 quadrant is combined as in Chapter 2 prior to the monopulse comparator network. The total footprint of this conceptual passive monopulse transceiver system is 14.2 mm x 14.6 mm x 3.4 mm.

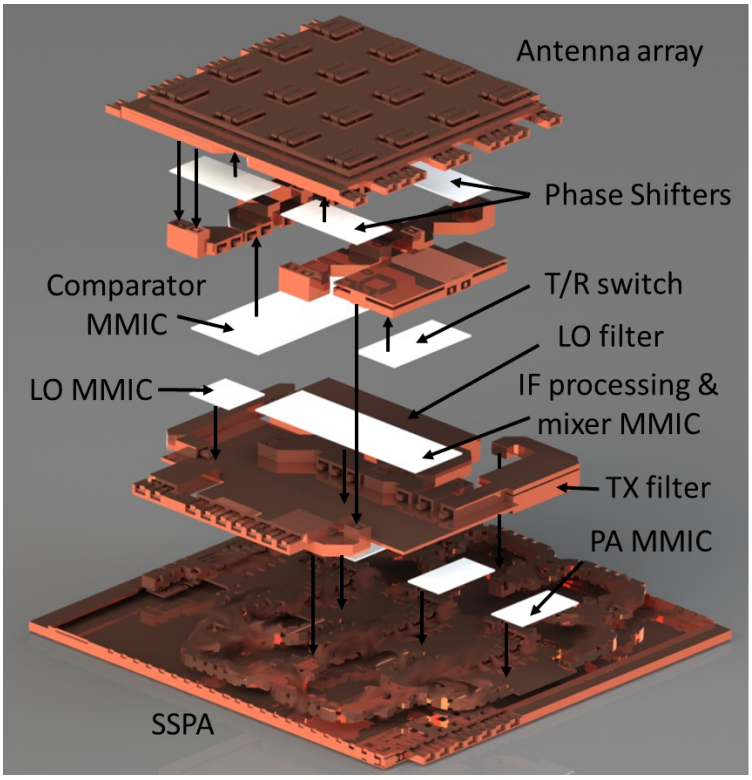
7.2.2 Active Monopulse Transceiver

Figure 7.3 shows a block diagram of a conceptual ESA-based "active" monopulse transceiver. The major additional components required are a monopulse processing chip with additional functionality and the ESA itself. Beyond expanding the W-band active monopulse comparator functionality discussed in Chapter 4 to four-ports for azimuth and elevation locational information, an expanded monopulse processor chip may also integrate output LNAs, the T/R switch, and/or the mixers necessary to downconvert the output signals down to the IF. There are arguments for all of this functionality being contained on one chip, but it may a lower risk option to distribute the functionality amongst several chips and interconnect them using low-loss rectangular coaxial transmission lines. The distribution of functionality amongst the MMICs must be carefully considered from a system-level and cost perspective.

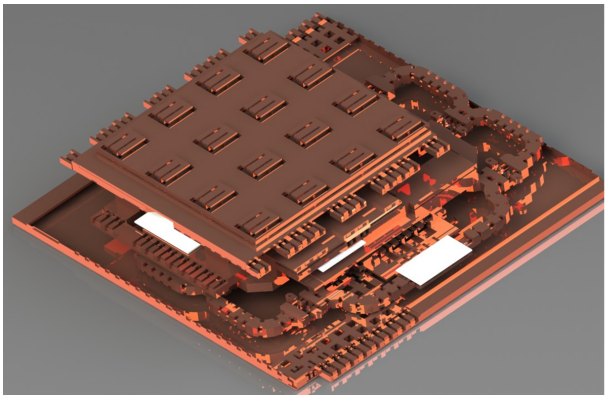
It may also be possible to include the phase shifters for each antenna or subarray on a single monopulse processor chip. The phase shifters are necessary for the electrical steering functionality of the ESA. Given an ESA type architecture, it would be possible to develop very large arrays with switched feed networks and tight elemental phase and gain control to allow for multiple beams and reconfigurable tracking modes. The phase shifter MMICs would also have integrated LNAs directly after each antenna element to reduce system noise figure.

While the T/R switch is shown at the input of the SUM port in the block diagram, as was the case in the passive monopulse architecture, this may not be the final configuration. Given the limited power handling of mm-wave MMICs, the phase shifter die may not be able to handle the power required for each transmitting element. Alternative architectures, including multiple T/R switches located before the receiver phase shifters, may be required to bypass the monopulse comparator MMIC in transmit mode.

Figure 7.4 shows a rendering of a conceptual active monopulse transceiver. Again, four layers are assembled for the complete transceiver. The bottom two layers, SSPA and IF processing/mixer layers, are similar to those shown for the passive transceiver, albeit with



(a)



(b)

Figure 7.4. (a) Exploded drawing of a conceptual compact passive monopulse receiver. Three layers of PolyStrata active devices and four detector diodes are used in its assembly. (b) Assembled conceptual compact monopulse receiver. The total footprint is 14.2 mm x 14.6 mm x 3.4 mm.

slightly different routing. The third layer contains a similar socket for a MMIC T/R switch, but also includes a comparator MMIC which receives inputs from all 16 antennas, and has

four outputs to the IF processing MMIC. This chip could also have adaptive functionality, including the subdivision of the array into subarrays for multiple beams, or combining inputs from the antennas directly.

The array layer itself contains phase shifter MMICs for array steering, with all of the DC inputs routed to the outside edges. Each conceptual phase shifter MMIC has 4 phase shifters with isolated paths for each of a set of 4 antennas. The phase shifters are combined into a single die to reduce occupied area and assembly complexity. As with the passive transceiver concept, the DC control lines are simply routed to the edges of the part. In practice, they would likely be routed down through the layers to connect with the control board beneath the SSPA.

7.3 Conclusion

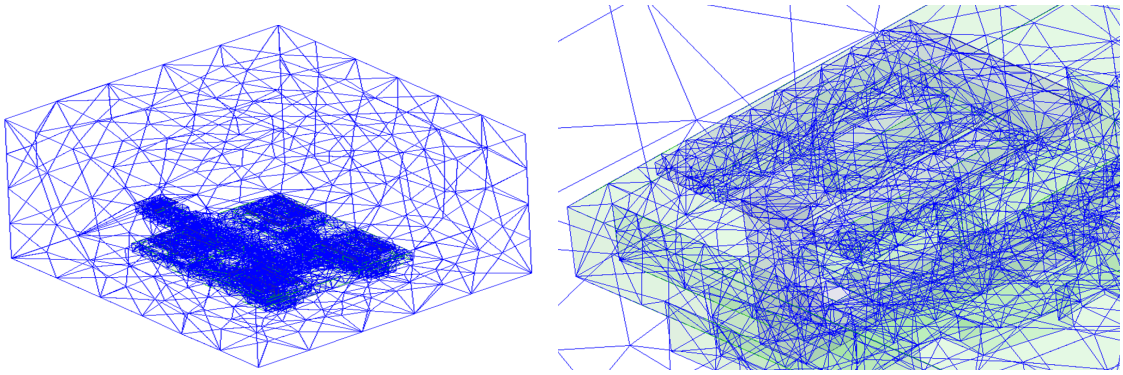
This dissertation has provided a foundation for the design of compact mm-wave monopulse transceivers, based on rectangular coaxial line technologies. This included the design, simulation and characterization of W-band cavity-backed patch antennas, waveguide transitions to rectangular coaxial transmission lines, integrated diode detectors, passive monopulse comparator networks, active monopulse comparator ICs, and state of the art rectangular coaxial power combiners. These contributions may lead to very compact mm-wave tracking radar systems in the near future.

Appendix A

3-D FEM Modeling

This appendix will discuss the finite element method (FEM) electromagnetic modeling techniques and setups used in this dissertation. The finite element method is a generalized mathematical approach for generating numerical answers which closely approximate the solutions of boundary value problems. For many complex boundary-value problems, the analytical solution is unobtainable; the finite-element method is invaluable in these instances [143]. FEM modeling tools are used for mechanical, thermal, fluid and electromagnetic analysis. Though originally developed for use in civil and mechanical engineering problems, FEM techniques have been applied to electromagnetics problems for several decades [144].

The electromagnetics problems analyzed in this dissertation document were solved using ANSYS HFSS 3-D FEM simulation software. FEM analysis can generally be thought of as consisting of 4 distinct steps: discretization of the domain, selection of interpolation functions, formulation of a system of equations, and solution of that system of equation [143]. HFSS begins this process by breaking up the three dimensional space of the model into a number of tetrahedra. For a typical problem, this could initially require on the order of one thousand tetrahedra. Within each tetrahedra, the software generate equations to approximate the solutions of various equations. For example, to solve for the electric field,



(a) (b)

Figure A.1. (a) Fully converged mesh of a 2 x 2 array of 94 GHZ cavity-backed patch antennas (b) detail mesh of a single antenna. In both figures, only the tetrahedra faces which coincide with a surface are shown.

the boundary value problem under consideration is:

$$\Delta \times (\frac{1}{\mu_r} \Delta \times \overrightarrow{E}) - k_0^2 \epsilon\_r = -jk_0 Z_0 \overrightarrow{J} \tag{A.1}$$

HFSS uses proprietary approximation techniques to generate a system of equations which approximate this (and other) boundary value problems. The software constructs a matrix of the equations and solves it at a particular frequency. In areas where the field density is highest, the software will adaptively generate additional, more dense tetrahedra, and regenerate the matrix. Once this matrix is solved, a calculation is done comparing the results to the previous step. When the comparison reaches a user-defined threshold, the solution is said to have converged. This process is called adaptive meshing. Final solutions of typical problems may require upwards of several hundred thousand tetrahedra and beyond, necessitating significant computing power [145].

An example of an adaptive mesh for the airbox surrounding a 2 x 2 array of 94 GHz cavity backed patch antennas is shown in Figure A.1a (detail of a single antenna in Figure A.1b). The images shown only show the faces of tetrahedra which intersect faces of the air box or structures contained therein. This problem required 70,150 tetrahedra to meet the

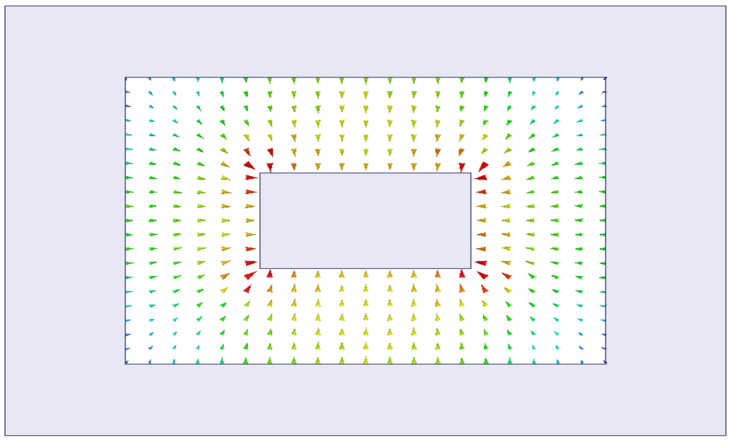


Figure A.2. Field lines for a rectangular coaxial waveport in HFSS.

desired convergence threshold, the majority of which (60,000+) are required for the airbox. In contrast, conductive materials are generally solved with significantly fewer. It is possible to solve for the fields within a conductor, but it is generally avoided, due to the large number of tetrahedrons required near the surface to accurately model skin depth effects. Surface boundary conditions provide an adequate approximation for the effects of fields within the conductive materials and are generally used by the software instead of full characterization.

In the case of time-harmonic field problems, an excitation is typically required. In HFSS, the most commonly used excitations are lumped ports and waveports. A lumped port represents an AC voltage or current applied between two conductive surfaces, whereas waveports use a 2-D eigen solver to generate a field pattern at the port given the cross-sectional geometry and materials at the port. All simulations shown in this work use a waveport as shown in Figure A.2. The structure shown is a coaxial port, with the corners removed.

With the excitation ports included, the next important aspects are boundary conditions at all of the interfaces between objects. Typically, these are set by the material properties of the objects, all of which must be set prior to simulation. At the perimeter of the simulation, however, these must be set manually. Though the default condition is perfect electrical conduction, for all simulations shown in this work, a radiation boundary is set. This boundary approximates the effect of infinite space, and is essential at W-band frequencies to account for

loss due to radiation. If the PEC boundary condition is used, reflections from the bounding box may cause anomalies in the simulation results.

HFSS also has the option for lumped RLC boundary condition, which provide a resistance, inductance, and/or capacitance of the users choosing between two points. These boundaries are used in simulations in this work to emulate chip resistors. A resistive boundary is combined with a block of material representing the chip resistor's substrate to simulate all of the effects of the chip resistor in the circuit.

A.1 HFSS Simulation Setup Example

This section will provide a step by step explanation of the setup for an ANSYS HFSS simulation. This is the typical setup for a simulation used in this dissertation document. The model may be drawn in the HFSS drawing package, or a third-party 3-D CAD software, such as Solidworks or Inventor. The model to be simulated is assumed to be finalized prior the first step in this procedure.

1. The device to be simulated is surrounded by a bounding box of air. The ports of the device should be located on the face of the bounding box.

2. All faces of the bounding air box are set to a radiation boundary condition. This boundary condition approximates an infinite space and is important at mm-wave frequencies to prevent oscillations within the bounding box. The radiation boundary is also used for the far-field setup for antenna simulations.

3. Any lumped boundary conditions are set. This may include capacitance, inductance, and resistance. Typically for the simulations in this work, the lumped boundary consitions are used to simulate resistive boundaries.

4. Draw planes or select appropriate faces for use as excitation ports. For all simulations in this work, waveports are used, with an integration line drawn from the ground to

the center conductor. All ports for this work were coax, and as such only the TEM propagation mode is supported. Thus, port setup requires only the simulation of the dominant port.

5. An analysis setup is selected for the problem. This includes the selection of solve frequency, maximum number of adaptive passes, and convergence threshhold. For the simulations in this work these values were 94 GHz, 12, and 0.005, respectively.

6. A frequency sweep range is set for the solutions. Interpolating frequency sweeps are generally used for minimum simulation time, although discrete sweeps may be used for verification.

7. A far field setup is added for any simulations which include radiating elements, such as antennas. The far field setup includes the setting of angular resolution and the selection of the radiation boundary for field calculations. The radiation boundary from the bounding air box is selected for any simulations shown in this work.

8. Run the automated check for any model errors. This may include intersections between model elements and non-manifold edges.

9. Simulate and plot the desired data.

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