The Modeling and Simulation of a Cascaded Three-Level Converter-Based SSSC

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Abstract

This thesis is dedicated to a comprehensive study of static series synchronous compensator (SSSC) systems utilizing cascaded-multilevel converters (CMCs). Among flexible AC transmission system (FACTS) controllers, the SSSC has shown feasibility in terms of cost-effectiveness in a wide range of problem-solving abilities from transmission to distribution levels. Referring to the literature reviews, the CMC with separated DC capacitors is clearly the most feasible topology for use as a power converter in the SSSC applications. The control for the CMC-Based SSSC is complicated. The design of the complicated control strategy was begun with well-defined system transfer functions. The stability of the system was achieved by trial and error processes, which were time-consuming and ineffective.

The goal of this thesis is to achieve a reliable controller design for the CMC-based SSSC. Major contributions are addressed as follows: 1) accurate models of the CMC for reactive power compensations in both ABC and DQ0 coordinates, and 2) an effective decoupling power control technique.

To simplify the control system design, well-defined models of the CMC-Based SSSC in both ABC and DQ0 coordinates are proposed. The proposed models are for the CMC-Based SSSC focus on only three voltage levels but can be expanded for any number of voltage levels. The key system transfer functions are derived and used in the controller design process. To achieve independent power control capability, the control technique, called the decoupling power control used in the design for the CMC-Based STATCOM is applied. This control technique allows both the real and reactive power components to be independently controlled.

With the combination of the decoupling power control and the cascaded PWM, a CMC with any number of voltage levels can be simply modeled as a three-level cascaded converter, which is the simplest topology to deal with. This thesis focuses on the detailed design process needed for a CMC-Based SSSC.

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Chapter 1 Introduction

1.1 Motivation

Series Compensation is a means of controlling the power transmitted across transmission lines by altering or changing the characteristic impedance of the line. There are two types of series compensation: the fixed capacitor or inductor type series compensators, or the converter type series compensators. Traditionally, series compensation of transmission lines has been performed by fixed-type thyristor controlled series reactance, either inductive or capacitive, depending on the power system requirement. The switching-based converter Static Synchronous Series Compensator (SSSC) provides another degree of freedom to series compensation in that the voltage-source converter (VSC) used for series compensation has the ability to maintain a constant compensating voltage in the presence of varying line current. The SSSC can also control the amplitude of the injected compensating voltage independent of the amplitude of the line current. The SSSC output voltage has the capability of injecting voltage that can either lead or lag the line current. The fixed capacitor type series compensators cannot perform these functions [A1].

Until recent advances in power semiconductor devices, the SSSC has not been used for most series compensation needs due to their relatively high cost. The primary objective of this thesis is to examine the possible uses of the SSSC based on a cascaded multi-level VSC topology with state-of-the-art power semiconductor devices in order to provide a more cost effective solution.

1.2 Objective and Research Outline

The objective of this research is to study the possibility of using a state-of-the-art power semiconductor device in a cascaded multi-level converter configured as a SSSC. The SSSC is viable cost effective alternative to the problems associated with power flow control. Figure 1.1 shows a block diagram for a typical SSSC.

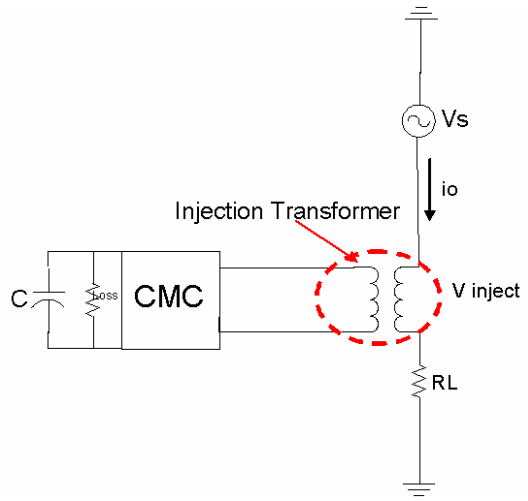


Figure 1.1 - Block Diagram for a SSSC

Past work at Virginia Tech [G4, I1], has resulted in the development of a cascaded VSC for shunt compensation. The primary objective of this thesis is to expand the prototype VSC to include not only shunt compensation or STATCOM operation but series compensation as well. In addition, a series-compensating device with the addition of energy storage can also be used to provide "real" voltage support to a power system. The combination of a series compensation device, energy storage, and a shunt compensating device will yield a Unified Power Flow Controller or UPFC device used for power flow control. This thesis will develop an accurate model and an effective

control scheme for the SSSC based on a cascaded multi-level topology. The SSSC control scheme developed should be easily expandable to include an energy storage system. The SSSC control scheme should also be easily incorporated with the existing STATCOM to produce a UPFC using state-of-the-art power semiconductor devices and a modern modular converter design methodology. In order to meet the stated objectives, a study of the various types of series compensating devices is needed as well as a detailed analysis of existing SSSC technology. Chapter 1 will explain what series compensation is and how it works. Chapter 2 will introduce the cascaded voltage source converter topology used for the proposed SSSC as well as some commonly used voltage source converter topologies. Chapter 2 will also give a detailed power stage design of a state-of-the-art power semiconductor-based cascaded multi-level converter, including information on the converter hardware itself and on future high power devices and their potential benefits to FACTS device design. Chapter 3 will be a detailed explanation of the SSSC modeling techniques proposed in this thesis. Chapter 4 will include the closed loop controller design for the SSSC. Chapter 4 will also discuss the simulated SSSC performance based on the average and switching models. Finally, a summary of the SSSC design will be presented and future work including the possibilities for DVR and UPFC will be discussed in Chapter 5.

1.3 Applications of Series Compensation

High power quality is becoming desirable for industrial factories and commercial building. The use of electronic devices has improved the manufacturing process by providing a means for automated production. Automated production processes are

particularly sensitive to electrical disturbances such as voltage sags and swells, voltage flicker, and harmonic interference. Voltage sags that last for only a few milliseconds can cause entire production processes to stop. The loss in production or damage to products due to these sags account for considerable financial losses for industry. According to an EPRI report (1995), the amount of money lost due to poor power quality to U.S. businesses alone were $400 billion per year. Advances in semiconductor technology as well as power electronic technology has provided a way to protect sensitive loads against the effects of poor power quality.

The applications for a SSSC are the same as for traditional controllable series capacitors. The SSSC can be used for power flow control, voltage stability, and phase angle stability [A2]. The benefit of the SSSC over the conventional controllable series capacitor is that the SSSC can induce both capacitive and inductive series voltages on a line. In other words, the SSSC has a wider range of operation compared with the traditional series capacitors [A3]. A SSSC can increase or decrease the power flow in a transmission line. Since power system stability is crucial, the SSSC has better possibilities for damping electromechanical oscillations compared to fixed capacitors [A3]. The primary reason that the converter type SSSC is not frequently used for series compensation is that the SSSC requires an interfacing transformer to the power system. The interfacing transformer is a big cost disadvantage to traditional series capacitors. In other words, performance is sacrificed for cost.

1.4 What is Series Compensation?

The series compensator is primarily applied to solve the power flow problem [A2]. There are two main causes for the problems associated with power flow. First, the power flow problem may be related to the length of the line. The length of the line maybe compensated to meet the transmission requirements by a fixed capacitor or inductor. Second, the power flow problem may be related to the structure of the transmission network. Network related problems typically result in power flow unbalance. There is a phenomenon called inadvertent interchange in a power system. Inadvertent interchange occurs when the power system tie-line schedule becomes corrupted. In other words, there is an unexpected change in load on a distribution feeder that causes the demand for power on that feeder to increase or decrease. If this occurs generators need to be turned on or off to compensate for the change in load. If the generators are not activated quickly enough, voltage sags or surges can occur. Network related problems might require controlled series compensation particularly if contingency or planned network changes are anticipated [A3].

Series compensation, if correctly controlled, can provide a significant improvement in transient stability for post-fault systems and can be very effective in damping power oscillations [A2]. There are two ways in which series compensation can be accomplished. Series compensation is accomplished either using a variable impedance-type series compensator or using a switching converter-type series compensator. The remainder of this section of the report will be used to describe the basics of both the variable type series compensators and the switching converter type series compensators.

1.5 Variable Impedance Type Series Compensator

All of the variable type series compensators are thyristor controlled. The type of thyristor used for the variable fixed type series compensators has an impact on their performance. In order to fully understand the fixed type of series compensators, a basic understanding of the various types of thyristors is needed. There are several types of high voltage and high current thyristors relevant to high power FACTS devices. The types of thyristors are as follows: Silicon Controller Rectifier (SCR); Gate Turn-Off Thyristor (GTO); MOS Turn-Off Thyristor (MTO); Integrated Gate Commutated Thyristor (GCT or IGCT) [A3]; MOS Controlled Thyristor (MCT) [A3]; and Emitter Turn-Off Thyristor (ETO) [J1]. Each of these types of thyristors have several important device parameters that are attractive for FACT device design. These parameters include but are not limited by voltage and current rating for the device, di/dt capability, dv/dt capability, turn-on time and turn-off time, Safe Operating Area (SOA), forward drop voltage, switching speed, switching losses, and gate drive power.

The details for each of the important device parameters will not be discussed, except to state that FACTS controllers constructed out of state-of-the-art power semiconductor devices with high switching speeds will have a cleaner output waveform for the load resulting in lower harmonic content and thus better performance. In many cases, higher speeds of operation induce more losses into the FACTS device. Power losses are a cost liability to the user. Electrical utility companies evaluate losses and some industrial customers evaluate losses on a lifetime present worth basis and these values can be from $1000 to $5000 per kilowatt losses for the evaluation of the purchase price. For example,

if a FACTS controller costs $100 per kilowatt and its losses are 2%, the value of the losses for an evaluated value of $2000 per kilowatt will be $40 per kilowatt or 40% of the purchase price of the converter itself. Therefore, it is imperative that the efficiency of a complete FACTS controller of several hundred MW rating must be greater than 98% and the losses have to be less than 1% in order to compete with the fixed type series compensators [A3].

A. GTO Thyristor Controlled Series Capacitor (GCSC)

Figure 1.2 (a) shows GCSC proposed by Karady and others in 1992. A GCSC consists of a fixed capacitor in parallel with a GTO Thyristor that has the ability to be turned on or off. The objective of the GCSC is to control the voltage across the capacitor (Vc) for a given line current. In other words, when the GTO is closed or on the voltage across the capacitor is zero and when the GTO is open or off the voltage across the capacitor is at its maximum value [A3].

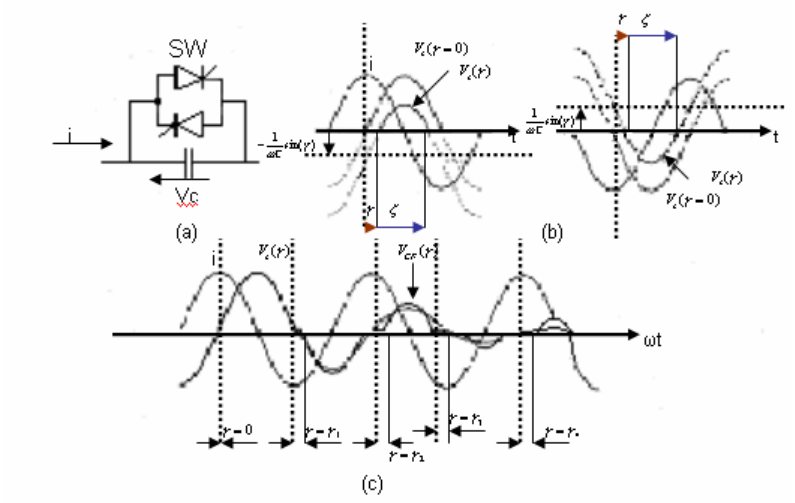


Figure 1.2 - (a) GTO-Controller Series Capacitor, (b) Turn-off Delay Angle. Control, (c) Possible Compensating Voltage Waveform

In order to control the capacitor voltage the GTO switch is opened and closed during each half cycle synchronous to the ac system frequency. The GTO switch is designed to close automatically whenever the voltage across the capacitor is zero. However, the time at which the GTO switch is turned off during each half cycle is controlled by turn-off delay angle with respect to the peak value of the line current. The turn-off behavior of the GCSC is shown in Figure 2(b). When the GTO switch is opened at the peak value of the line current without any delay, the voltage across the capacitor is the same as the capacitor voltage obtained in a steady state with a permanently opened switch. If the time at which the GTO switch is opened is delayed by the phase angle γ with respect to the peak value of the line current, the voltage across the capacitor can be defined according to Equations (1.1) and (1.2) [A3].

$$V_c(t) = \frac{1}{C} * \int_{\gamma}^{\omega t} i(t)dt = \frac{1}{\omega C} * (\sin(\omega * t - \sin\gamma)) \qquad \textbf{Equation } 1.1$$

$$i(t) = I * \cos(\omega * t) \qquad \textbf{Equation } 1.2$$

From Figure 1.2(c), it is clear that the magnitude of the capacitor voltage can be varied continuously by the method of delayed angle control stated previously (max $\gamma = 0$, zero $\gamma = \pi/2$). For practical applications, the GCSC is controller to either compensate voltage or reactance. In voltage compensating mode, the function of the GCSC is to maintain the rated compensating voltage even if the line current decreases over a defined interval. The capacitive reactance X_c is selected to produce a compensating voltage

$Vc_{Max} = X_c * I_{min}$. The turn-off delay angle γ increases to reduce the duration of the capacitor injection and thereby maintain the compensating voltage in the face of increasing line current [A3].

If the GCSC is operated in the impedance compensating mode, the primary function of the GCSC is to maintain the maximum rated reactance at any line current up to the maximum rated line current for the transmission line. For the impedance compensating mode, the capacitive impedance is chosen in such a way as to provide the maximum amount of series compensation at rated current ($X_c = Vc_{max}/I_{max}$) [A3].

B. Thyristor Switched Series Capacitor (TSSC)

Another type of variable fixed series capacitors is known as the Thyristor Switched Series Capacitor (TSSC). Figure 1.3 shows the basic schematic of the Thyristor Switched Series Capacitor TSSC also known as the Utility Controlled Thyristor or SCR. The TSSC consists of several capacitors shunted by a reverse connected thyristor bypass switch.

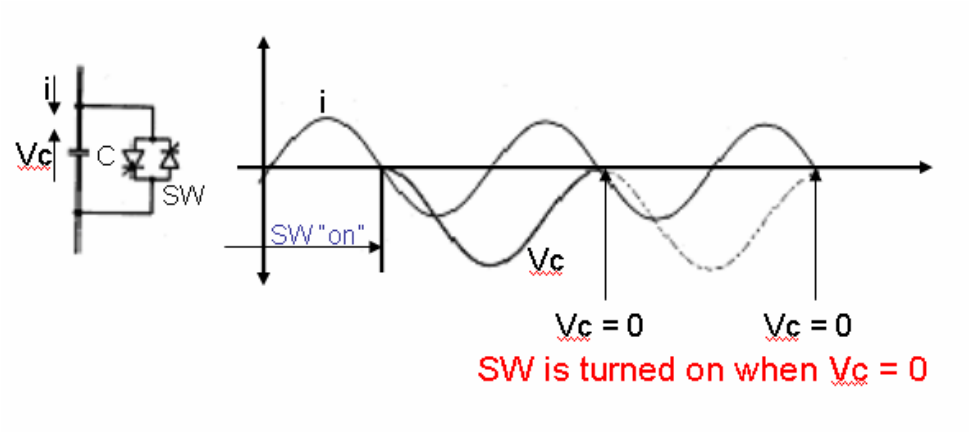


Figure 1.3 - Schematic of TSSC and Capacitor dc offset voltage at zero line current.

The basic operating principle of the TSSC is simple. The amount of series compensation is controlled in a step-like manner by increasing or decreasing the number of series capacitors inserted into the line. The thyristor turns off when the line current crosses the zero point. As a result capacitors can only be inserted or deleted from the string at the zero crossing. Since the capacitors are inserted at the zero crossing it takes one full half-cycle of the line current to charge the capacitor from zero to full charge. Consequently, opposite polarity half-cycles will be used to discharge the series capacitors. Due to the fact that the capacitors are inserted when the line current crosses zero, a dc offset voltage results that is equal to the amplitude of the ac capacitor voltage. In order to keep the initial surge current at a minimum, the thyristor is turned on when the capacitor voltage is zero. There could be a limit for the attainable response time (up to one full cycle) for the TSSC due to the dc-offset voltage when a capacitor is inserter and due to the requirement that the thyristor can only be turned on when the capacitor voltage is zero [A3].

The TSSC controls the degree of compensating voltage by either inserting or bypassing series capacitors but it cannot change the natural characteristics of the classical series capacitor compensated line. There are several limitations to the TSSC. First, a high degree of TSSC compensation could cause subsynchronous resonance in the transmission line just like a traditional series capacitor. The switching of the TSSC could be modulated to counteract the subsynchronous resonance but due to relatively long switching delays, the modulation will likely be ineffective if not counter productive [A3]. As a result, the TSSC would not be used in applications where a high degree of series compensation is needed. The TSSC is most commonly used for power flow control and

for damping power flow oscillations where the response time required is moderate.

There are two types of modes of operation for the TSSC. First, the TSSC can be operated to control the amount of compensating voltage. In this mode, the reactance of the capacitor bank is chosen in such a way as to produce the average rated compensating voltage ($Vc_{max} = 4X_C*I_{min}$) even if the line current decreases. As the line current increases from I_{min} to I_{max}, the numbers of series capacitors are progressively bypassed in order to reduce the overall capacitive reactance and maintain the level of compensating voltage as the line current is increased. Second, the TSSC can be operated in impedance compensating mode. In this mode, the maximum compensating reactance is maintained at any line current up to the rated maximum. The capacitive impedance is chosen in such a way as to provide the maximum series compensation at rated current ($4X_c = Vc_{max}/I_{max}$) [A3].

C. Thyristor Controlled Series Capacitor (TCSC)

The basic thyristor controlled series capacitor scheme was proposed in 1986 by Vithayathil as a means of "rapid adjustment of network impedance"[A3]. Figure 1.4 shows the basic thyristor controlled series capacitor (TCSC) scheme.

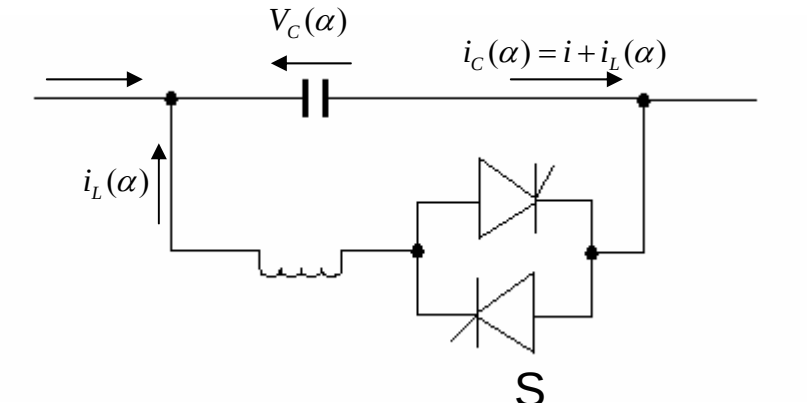


Figure 1.4 - Basic Thyristor Controlled Series Capacitor

The TCSC is composed of a series-compensating capacitor in parallel with a thyristor-controlled reactor. The TCSC is constructed similar to the TSSC if the impedance of the reactor is significantly smaller than the impedance of the capacitor. If this is the case the TCSC can be operated in a similar on/off manner as the TSSC. The basic operating principle behind the TCSC is that it can provide a continuously variable capacitor by means of partially canceling the effective compensating capacitance of the thyristor-controlled reactor. The thyristor controlled series reactor operating at the fundamental system frequency behaves like a continuously variable reactive impedance, controllable by a delay angle α. The parallel LC circuit determines the steady-state impedance of the TCSC. The LC circuit consists of a fixed series capacitor and a variable inductive impedance. The impedance of the TCSC as a function of the delay angle α is illustrated by Equation (1.3) and Equation (1.4) [A3].

$$X_{TCSC} = \frac{X_C * X_L(\alpha)}{X_L(\alpha) - X_C} \qquad \textbf{Equation } 1.3$$

$$X_L(\alpha) = X_L * \frac{\pi}{\pi - 2\alpha - \sin(\alpha)}, X_L \le X_L(\alpha) \le \infty \qquad \textbf{Equation } 1.4$$

X_L from Equation (4) is ωL and the delay angle α is measured from the crest of the capacitor voltage or the zero crossing of the line current. As the impedance of the controllable reactor is varied from its maximum (infinity) to its minimum (ωL), the minimum capacitive compensation is increased by $X_{TCSCmin} = X_C = 1/\omega C$. Thus, the degree of series capacitive compensation is increased. When $X_C = X_L(\alpha)$, the impedance of the TCSC becomes infinite. The TCSC has two operating ranges; one is when $\alpha_{Clim} \le \alpha \le \pi/2$, where the TCSC is in capacitive mode. The other range of operation is $0 \le \alpha \le \alpha_{Llim,}$ where the TCSC is in inductive mode [A3].

In the impedance compensation mode the TCSC maintains the maximum rated compensating reactance at any line current up to its rated maximum. For this mode the TCSC thyristor controlled reactor and capacitor are chosen so that at the α_{Clim} the maximum capacitive reactance can be maintained at and below the maximum line current rating. The two types of voltage compensation modes are capacitive and inductive. In the capacitive voltage compensation mode the minimum delay angle α_{Clim} sets the limit for the maximum compensating voltage up and until the line current reaches such a value that the voltage across the capacitor is a maximum. The maximum voltage across the capacitor constrains the operation of the TCSC until the maximum line current is reached. For the inductive voltage compensation mode, the maximum delay angle α_{Llim} limits the

voltage at low line currents and the maximum rated thyristor current at high line currents [A3].

1.6 Control of Variable Impedance Type Series Compensators

The internal controls for the GCSC, TSSC, and TCSC are similar. In principle, the basic controller function is to define the conduction and to block intervals of the thyristors in relation to the fundamental frequency component of the line current. The control of the three types of variable impedance type series compensators can be broken down into three basic functions. First, the thyristor controller series capacitors must be synchronized with the line current. Providing a phase-locked loop circuit that runs in synchronism when the line current accomplishes this. Second, the turn-on or turn-off delay angle must be calculated. Finally, the gate signals of the thyristors must be generated [A3].

The main consideration for the internal control of the variable impedance type series compensators is to ensure their immunity to subsynchronous resonance. There are two ways in which this is done. First, the phase-locked loop (PLL) is operated on the basis of the fundamental frequency component of the line current. Second, the PLL is synchronized to the fundamental frequency of the line current for the generation of the basic timing reference only. In order to accomplish the first method substantial filtering is required to remove the subsynchronous frequency components while at the same time maintaining the correct phase relationship with the line current. For the second method, the actual zero crossing of the capacitor voltage is estimated from the prevailing capacitor voltage and line current from an angle correction circuit. The delay angle is calculated

based on the desired angle and the estimated correction angle. The desired delay angle can be adjusted by a closed-loop phase shift of the basic time reference provided by the PLL circuit. The second approach is more likely to provide a faster response for those applications requiring such a response [A3]. Figure 1.5, shows a block diagram of the proposed variable impedance type control scheme.

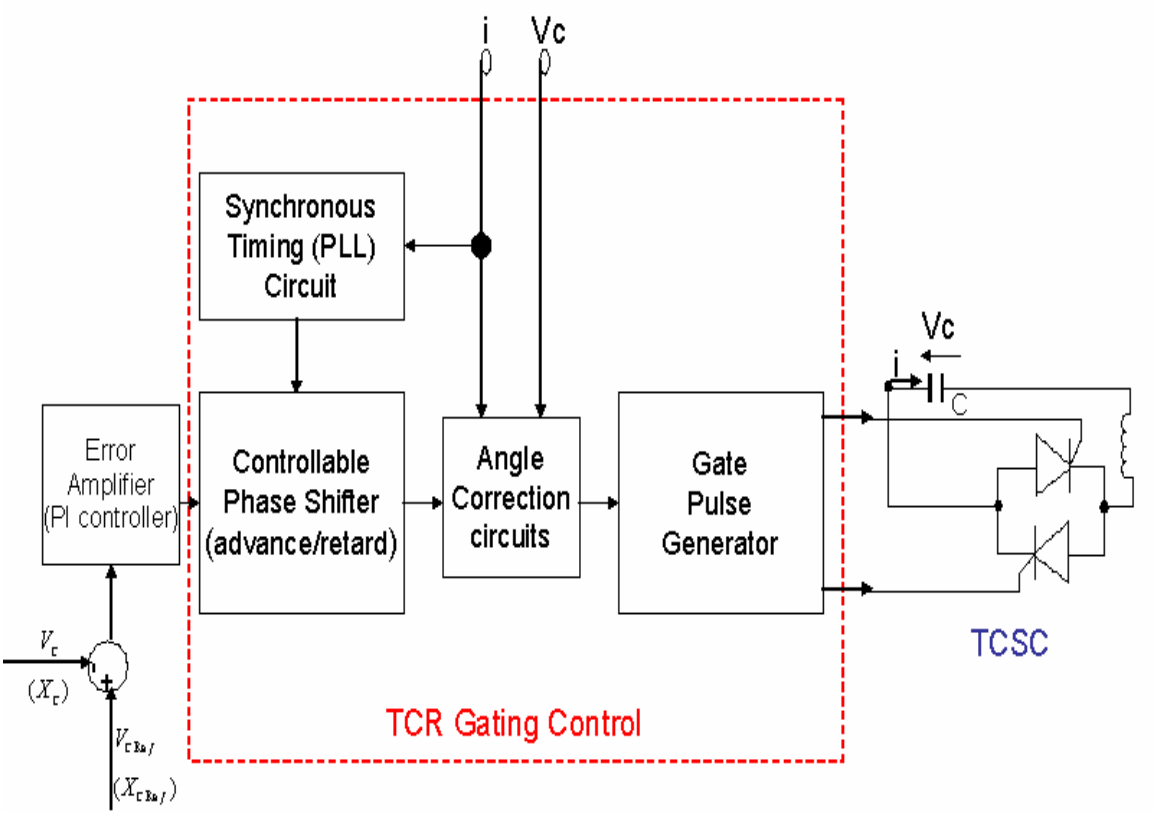


Figure 1.5 - Variable Impedance Type Series Compensator Control Scheme.

1.7 Switching Converter Type Compensators

Switching converter type compensators are known as Flexible AC Transmission Systems or (FACTS) devices. STATCOM, SSSC, DVR, and UPFC are all types of FACTS devices. The acronym FACTS has been used earlier in this chapter; however, a brief explanation for the potential for FACTS devices is needed.

Reactive power compensation has been a well known and effective control strategy in electric power systems for decades [A3]. Due to advances in power semiconductor technology for high-power forced-commutated valves such as the GTO and ETO, the converter-based FACTS controllers have become real. There are several advantages to converter-based FACTS controllers that include continuous and precise power control, cost reduction of the associated relative components, and a reduction in size and weight of the overall system. FACTS can be connected to the power grid in three ways: shunt, series, and a combination of shunt and series. The series connected FACTS device is known as a SSSC. A SSSC is an example of a FACTS device that has as its primary function to change the characteristic impedance of the transmission line and thus change the power flow. The impedance of the transmission line is changed by injecting a voltage that either leads or lags the transmission line current by 90º. If the SSSC is equipped with an energy storage system, the SSSC becomes a DVR with the added feature of voltage sag compensation due to power system instability.

A. Switching Converter Type Compensators

A voltage source converter with internal control can be considered a synchronous voltage source. A synchronous voltage source can produce a set of three alternating sinusoidal voltages at the desired fundamental frequency with controllable amplitude and phase angle. A synchronous voltage source can also generate or absorb reactive power and exchange real power with the ac system. The concept of using a voltage source converter or synchronous voltage source for series compensation comes from the fact that the impedance verses frequency characteristics of the series capacitor has no role in accomplishing the desired compensation of a transmission line. The function of the series capacitor is to simply produce an appropriate voltage at the fundamental frequency in quadrature with the line current in order to increase the voltage across the inductive line impedance and therefore increase the line current and the transmitted power [A3]. The voltage source converter provides additional degrees of freedom to series compensation due to the fact that both real and reactive power can be injected into the transmission line and the voltage source converter has an inherent ability to reduce subsynchronous resonance [A2].

1.8 The Static Synchronous Series Compensator (SSSC)

The voltage-sourced converter based series compensators, also known as the Static Synchronous Series Compensator (SSSC) was proposed by Gyugyi in 1989. The basic operation principle of the SSSC can be explained with reference to Figure 1.6.

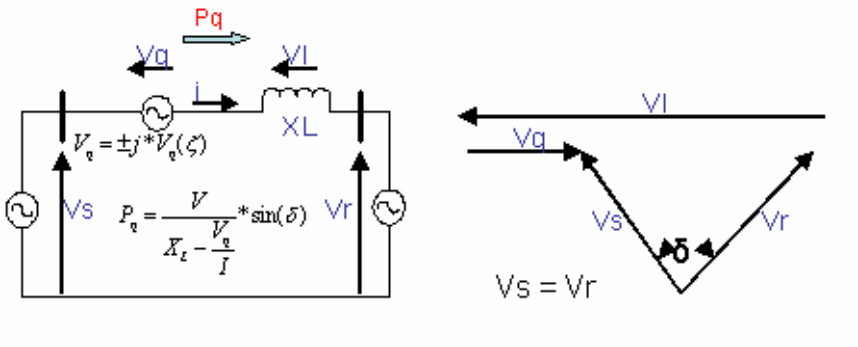


Figure 1.6 - Simplified Diagram of Series Compensation with the Resulting Phasor Diagram.

From the Phasor diagram it can be stated that at a given line current the voltage across the series capacitor forces the opposite polarity voltage across the series line reactance in order to increase the magnitude of the capacitor voltage. In other words, the series capacitive compensation works by increasing the voltage across the transmission line and thus increasing the corresponding line current and transmitted power [A3].

During normal capacitive compensation, the output voltage lags the line current by 90 degrees. The voltage source converter can be controlled in such a way that the output voltage can either lead or lag the line current by 90 degrees. The SSSC injects a compensating voltage in series with the line irrespective of the line current. The transmitted power verses transmitted phase angle relationship is shown if Equation (1.5).

$$P = \frac{V^2}{X}\sin\delta + \frac{V}{X}V_q\cos\frac{\delta}{2} \qquad \textbf{Equation } 1.5$$

According to Equation (5) if the SSSC is intended to be used for power flow control then the SSSC has a rating of twice the controllable compensating range as the VA rating of the converter. In other words, the compensation capability of the SSSC is twice the VA rating of the voltage source converter. This means that the SSSC can increase or decrease the power flow to the same degree in either direction simply by changing the polarity or reversing the polarity of the injected ac voltage. The reversed (180 degree) phase shifted voltage adds directly to the reactive voltage drop of the line; meaning, the reactive line impedance appears as if it were increased. If the amplitude of the reversed polarity voltage is large enough, the power flow will be reversed. Figure 1.7 shows the transmitted power verses transmitted angle as a function of the degree of series compensation [A3].

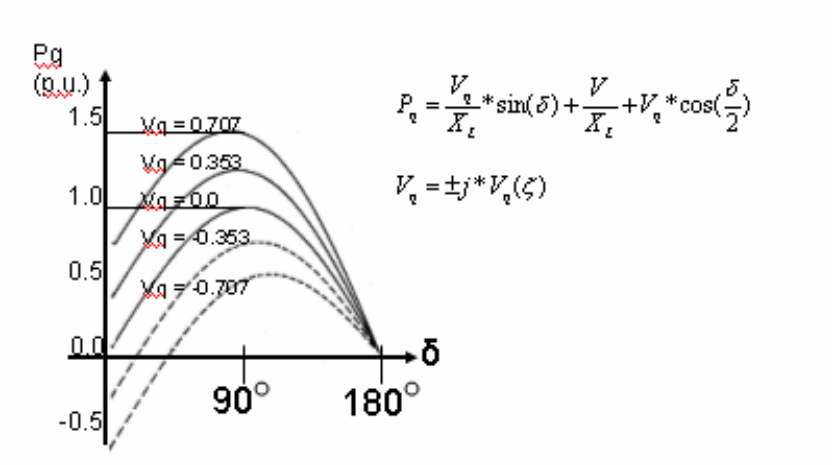


Figure 1.7 - Transmitted Power verses Transmitted Angle as a Function of Series Compensation.

A. Control Range and VA Rating of a SSSC

The SSSC can provide capacitive and inductive compensating voltage independent of the transmission line current up to the rated current for the line. In voltage compensation mode, the SSSC can maintain the rated capacitive and inductive compensating voltage regardless of the changes in the line current. In impedance compensation mode, the SSSC must maintain the maximum rated capacitive compensating reactance at any line current. The rating of the SSSC power components must be rated for the maximum line current and compensating voltages [A3].

B. Real Power Compensation of a SSSC

One of the advantages of the SSSC over the traditional variable thyristor controlled series capacitors is the SSSC's ability to provide real power by controlling the angular position of the injected voltage with respect to the line current. However, the SSSC cannot inject real power into the ac system without an additional energy storage element added to the converter. The capability of the SSSC to provide both real and reactive power to the ac system has significant application potential [A3].

C. Internal Control of a SSSC

There are two ways in which the voltage source converter can be internally controlled. First, in order to maintain a quadrature relationship between the converter voltage and the line current, to provide series compensation, and to handle the subsynchronous resonance, the converter can be indirectly controlled. Second, in order to maintain synchronism with the fundamental frequency, the converter must be directly

controlled. The high power directly controlled converters are more costly and more difficult to implement, but, they provide better control flexibility. A possible control scheme for the indirectly controlled converter is shown in Figure 1.8 [A3].

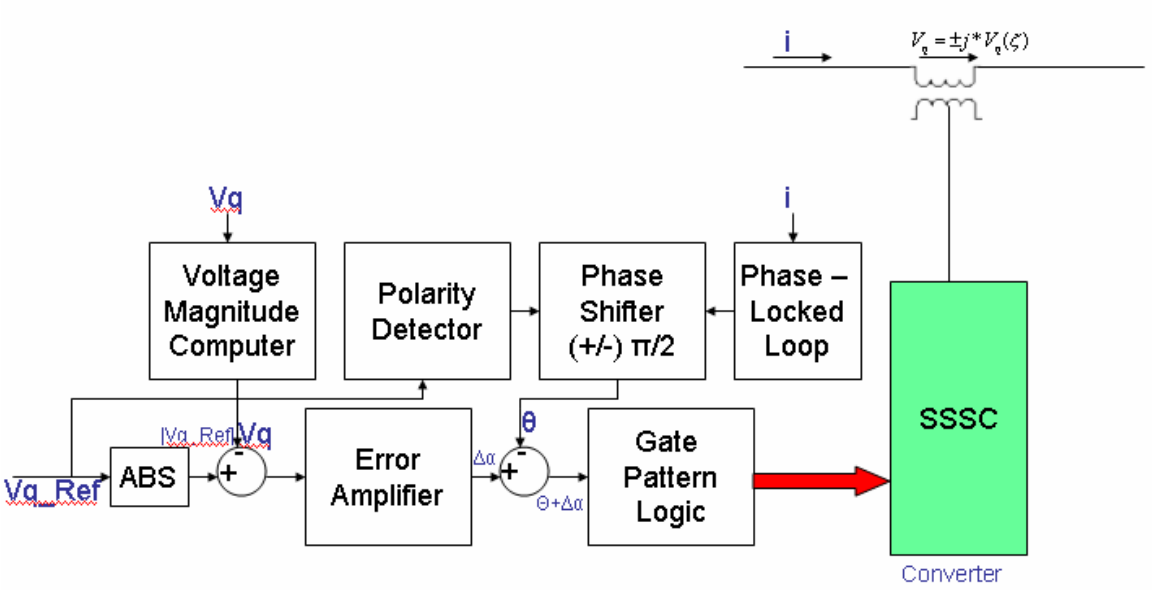


Figure 1.8 - Block Diagram of a Possible Indirect Control Scheme.

The inputs to the internal control are the line current, the injected compensating voltage, and the reference voltage. The control is synchronized to the line current through the PLL control. The phase shifter is operated from the output polarity detector, which determines the positive capacitive reference voltage or the negative inductive reference voltage. A simple closed-loop controller controls the compensating voltage. The absolute value of the reference voltage is compared to the measured magnitude of the injected voltage and the amplified difference is added as a correction angle to the synchronizing signal. As a result the gate signals will be either increased or decreased

and the compensating voltage will be phase shifted with respect to the line current [A3].

A possible control scheme for the directly controlled converter is shown in Figure 1.9. This scheme can be used to eliminate the unwanted output voltage due to the modulation of the dc capacitor voltage.

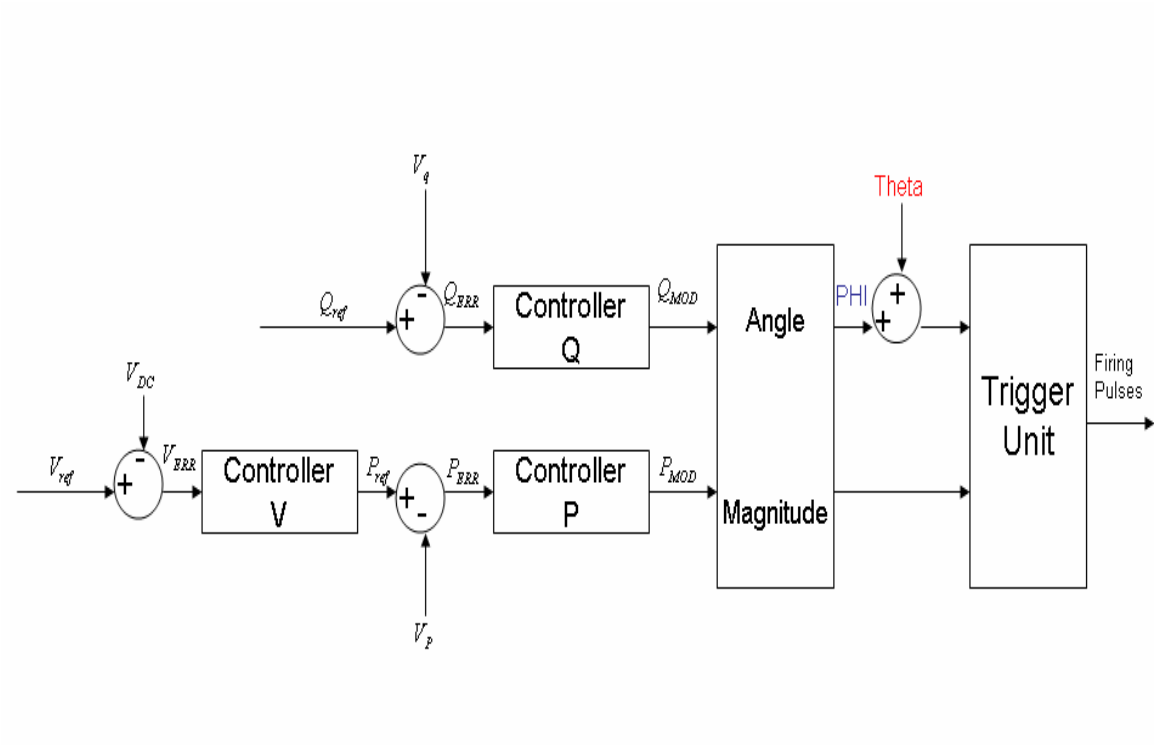


Figure 1.9 – Possible Control Scheme for Directly Controlled Converters.

This direct control scheme is also valid to provide both real and reactive line compensation if the converter is equipped with a suitable dc power supply. The control is operated from three reference signals. The reference signals provide the desired magnitude of the series reactive compensating voltage, the series real compensating voltage, and the operating voltage of the dc capacitor. The reactive voltage reference and the overall real voltage reference are compared to the corresponding components of the

measured compensating voltage. From these signals, the magnitude of the injected voltage and the phase angle are used to generate the gate drive signals for the converter [A3].

1.9 Comparison of Variable Impedance Type Series Compensators and Switching Converter Type Series Compensators

Figure 1.10 shows a comparison table for the variable type series compensators and the converter based series compensator. The following can be concluded from this table.

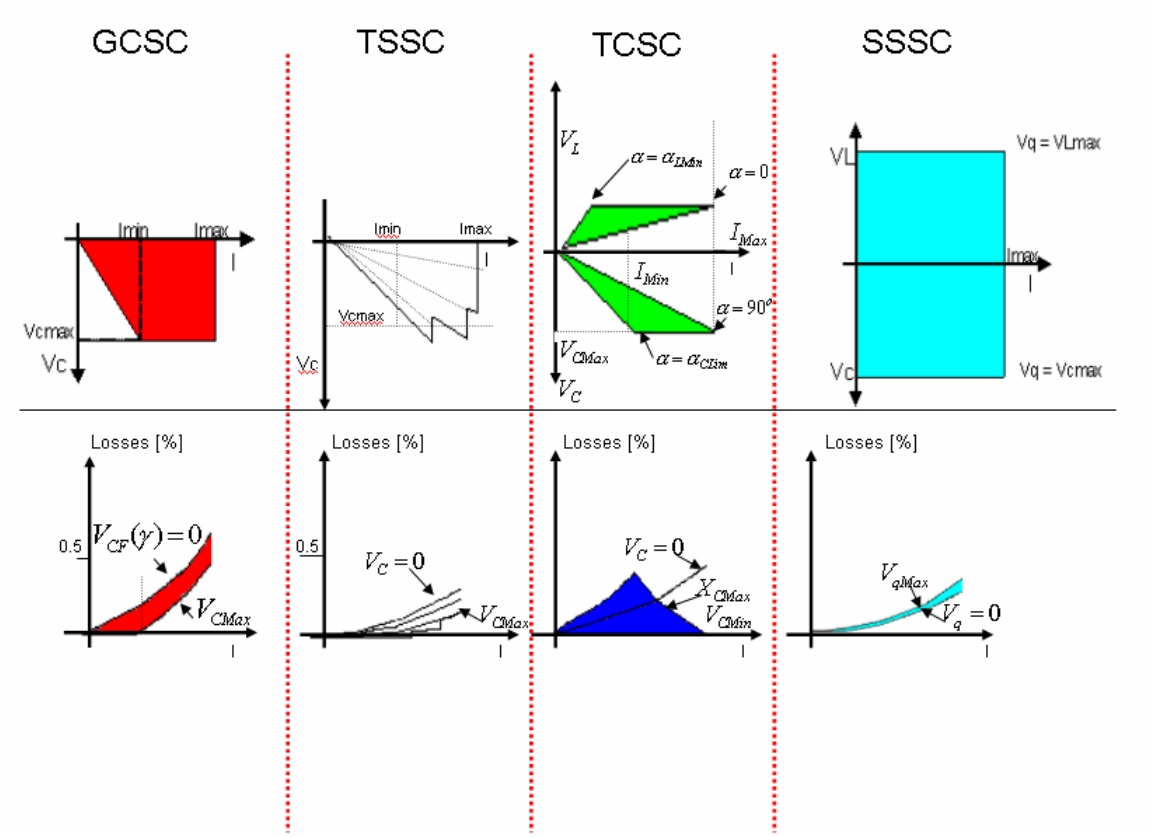


Figure 1.10 - Comparison of Variable Type Series Compensators to Converter Type Series Compensators.

1. The SSSC is capable of internally generating a controllable compensating voltage over any capacitive or inductive range independent of the magnitude of the line current. The GCSC and the TSSC generates a compensating voltage that is proportional to the line current. The TCSC can maintain the maximum compensating voltage with decreasing line current but the control range of the compensating voltage is determined by the current boosting capability of the thyristor controlled reactor [A2, A3].
2. The SSSC has the ability to be interfaced with an external dc power supply. The external dc power supply is used to provide compensation for the line resistance. This is accomplished by the injection of real power as well as for the line reactance by the injection of reactive power. The variable impedance type series compensators cannot inject real power into the transmission line. They can only provide reactive power compensation [A2, A3].
3. The SSSC with energy storage can increase the effectiveness of the power oscillation damping by modulating the amount of series compensation in order to increase or decrease the transmitted power. The SSSC increases or decreases the amount of transmitted power by injecting positive and negative real impedances into the transmission line. The variable-type series compensators can damp the power oscillations by modulating the reactive compensation [A2, A3].

1.10 Summary

This chapter has introduces the basic techniques used for series compensation. This chapter also gives a brief introduction to the converter-based series compensator or the SSSC. Further details concerning the operation and control techniques for the SSSC will be given in later chapters. Chapter 2 of this thesis will discusses the operating principle of the SSSC and outlines the power stage design for the proposed CMC-Based SSSC.

Chapter 2 Voltage Source Converter Topology Selection and Power Stage Design of a SSSC

A SSSC is one of the series type FACTS controllers. The key component of a SSSC is the voltage source converter (VSC). There are several different types of VSC's that could be used in the design of a SSSC. This chapter will give a brief summary of the types of VSC's along with an outlined specification for the proposed SSSC. This chapter presents the basic operating principles of the SSSC. Also, this chapter will provide incite into the power stage design or VSC hardware design of the proposed SSSC.

2.1 Brief Summary of Multilevel Voltage Source Converter Topologies

Over the past twenty years there have been several multilevel voltage source converter (VSC) topologies introduced by universities and industry. These VSC topologies can be summarized into two distinct categories. The first category is known as topology-level multilevel converters. The second category is known as hybrid multilevel converters.

A. Topology-Level Multilevel Converters

The behavior of the topology-level multilevel converters can be summarized by examining the behavior of four types of capacitor-voltage synthesized-based multilevel converters. The first type of capacitor-voltage synthesized-based multilevel converter is called a diode-clamped multilevel converter. The second type of capacitor-voltage synthesized-based multilevel converter is called a flying-capacitor multilevel converter. A third type of capacitor-voltage synthesized-based multilevel converter is called a P2 multilevel converter. Finally, the last major type of capacitor-voltage synthesized-based

multilevel converter is a cascaded converter with separate DC sources. The following subsections of this thesis will briefly explain how these four types of converters work.

A1. Diode-Clamped Multilevel Converter

The diode-clamped multilevel converter (DCMC) makes use of capacitors in series to divide the DC bus voltage into a distinct set of voltage levels. For example, in order to produce a *m*-level phase voltage, a diode-clamped inverter needs *m*-1 capacitors on the DC bus. A three-phase, five-level diode-clamped inverter is shown in Figure 2.1. The DC bus consists of four capacitors: C_1, C_2, C_3 and C_4. For a DC bus voltage V_{dc}, the voltage across each capacitor is divided by the number of DC bus capacitors. The device voltage stress will be limited to one capacitor voltage level or $V_{dc}/4$, through clamping diodes [B1-B4].

In order to explain how the staircase-shaped converter output voltage synthesized, the neutral point N is used as the reference point for the converter output phase voltage. Using the five level converter shown in Figure 2.1, there are five possible switch combinations that can be used to generate a five level voltage from point A to point N. Table 2.1 is used to illustrate the five possible switching states of the converter as well as their corresponding output phase voltage [B1-B4].

From Table 2.1, a 1 is used to represent a condition when the converter switch is on, and a 0 represents a condition when the converter switch is off. For each phase leg, a set of four adjacent switches is on at any given time. There are four complementary switch pairs in each phase, i.e., S_{a1}-$S_{a'1}$, S_{a2}-$S_{a'2}$, ..., and S_{a4}-$S_{a'4}$ [B1-B4].

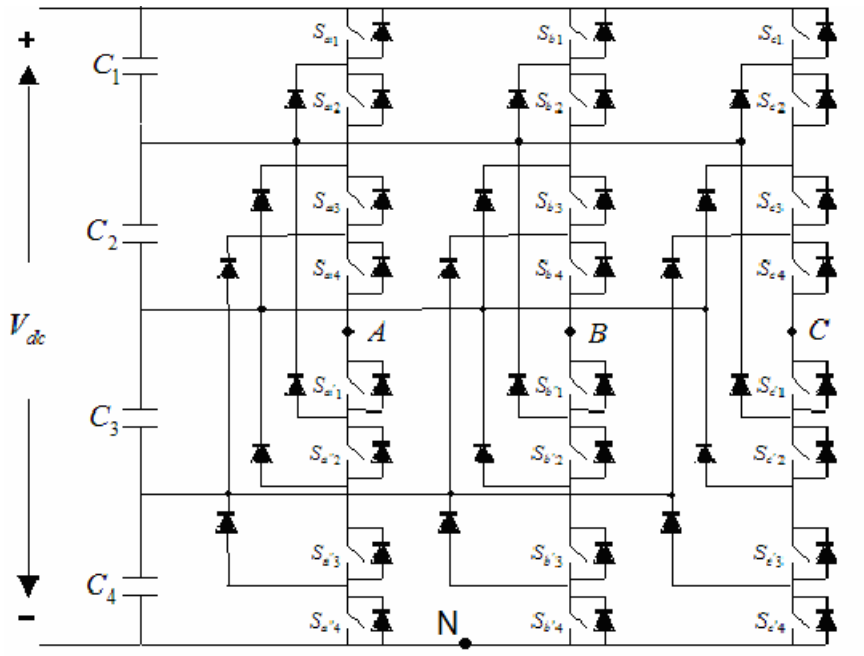


Figure 2.1 - A three-phase, five-level diode-clamped converter.

TABLE 2.1. DIODE-CLAMPED FIVE-LEVEL CONVERTER VOLTAGE LEVELS AND THEIR SWITCH STATES.

Output	Switch State							
V_{AO}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	$S_{a'1}$	$S_{a'2}$	$S_{a'3}$	$S_{a'4}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3Vdc/4$	0	1	1	1	1	0	0	0
$V_3=Vdc/2$	0	0	1	1	1	1	0	0
$V_2=Vdc/4$	0	0	0	1	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

A2. B. Flying-Capacitor Multilevel Converter

A flying-capacitor multilevel converter (FCMC), as shown in Figure 2.2, makes use of a ladder type structure of DC capacitors. The voltage across each capacitor differs from the voltage on the next capacitor. In order to generate an *m*-level staircase output voltage, *m*-1 capacitors in the DC bus are needed. The structure of each phase leg is the same. The size of the voltage increments between two capacitors is used to determine the number of levels of the converter's output voltage [C1-C4].

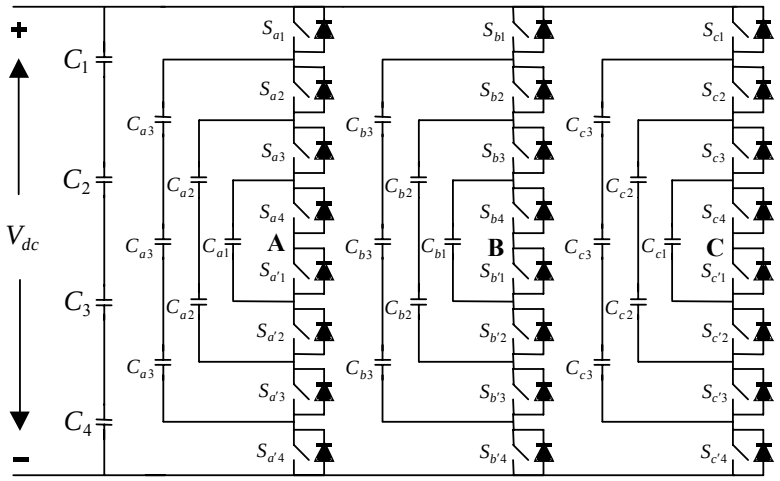


Figure 2.2 - A three-phase, five-level flying-capacitor converter topology.

Figure 2.2 shows three inner capacitors (C_{a1}, C_{a2} and C_{a3}) in phase A that are used for voltage balancing purposes. It must be noted that the capacitors used for voltage balancing purposes are different from phase to phase whereas all three phases of the flying-capacitor topology share the same DC link capacitors. Table 2.2 shows one possible combination for the switching states of the flying-capacitor topology. It must be noted that there is more than one possible set of switch combinations that can generate the desired converter output voltage. Due to this fact, the FCMC has more flexibility than the DCMC [C1-C4].

TABLE 2.2 - A POSSIBLE SWITCH COMBINATION OF THE VOLTAGE LEVELS AND THEIR CORRESPONDING SWITCH STATES (FLYING CAPACITOR)

Output	Switch State							
V_{AO}	S_{a1}	S_{a2}	S_{am-1}	S_{am}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$V_5=V_{dc}$	1	1	1	1	0	0	0	0

$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

A3. P2 Multilevel Converters

According to [D1], the P2 multilevel converter consists of a number of two-level cells. Regardless of the load characteristic, the P2 converter can balance each voltage level independently. Figure 2.3 shows a phase leg of the P2. The main devices that the P2 converter uses to synthesize the desired converter output voltage are switches S_{p1}-S_{p4}, S_{n1}-S_{n4} and their anti-parallel diodes. The remaining switches and diodes in the P2 converter are used to provide voltage clamping and balancing for the converter capacitors. Table 2.3 shows one possible switching combination used to produce a five-level output voltage.

TABLE 2.3. SWITCHING STATE TO PRODUCE OUTPUT VOLTAGE OF THE P2MC.

Output	Switch State							
V_{ON}	S_{p1}	S_{p2}	S_{p3}	S_{p4}	$S_{a'1}$	$S_{a'2}$	$S_{a'm-1}$	$S_{a'm}$
$4V_{dc}$	1	1	1	1	0	0	0	0
$3V_{dc}$	1	1	1	0	0	0	0	1
$2V_{dc}$	1	1	0	0	0	0	1	1
V_{dc}	1	0	0	0	0	1	1	0
0	0	0	0	0	1	1	1	1

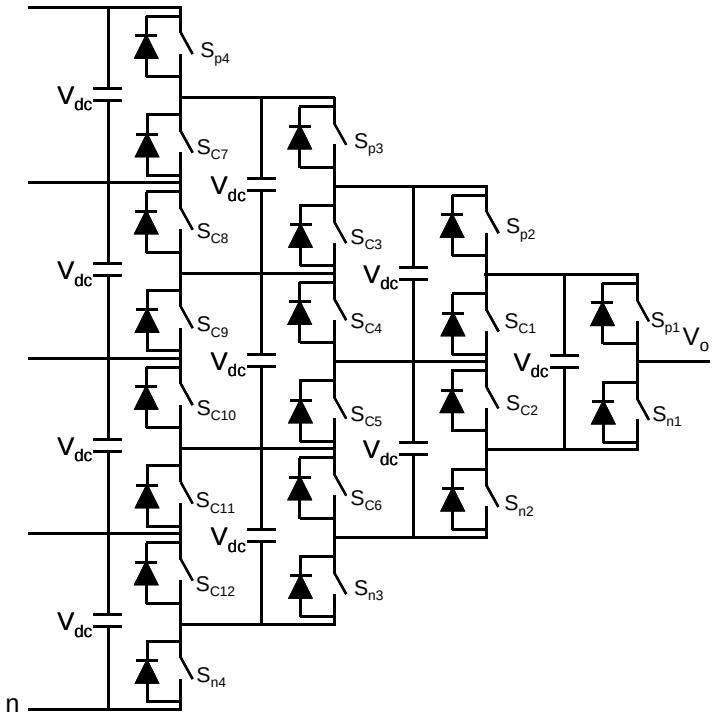


Figure 2.3 - Phase leg of the five-level P2 converter.

A4. D. Cascaded-Multilevel Converters with Separated DC Sources

Finally, the last major type of capacitor-voltage synthesized-based converter discussed in this thesis is the multilevel converter. The multilevel converter consists of several cascaded converters using separate DC sources. This converter is known as the CMC. The primary function of the CMC is to synthesize a desired output voltage from the separate DC voltage sources. There are several different types of DC sources that can be used in the CMC. For example, some DC sources include but are not limited by batteries, fuel cells, and solar cells. One of the most popular applications of the CMC is the high-power AC power supplies and adjustable-speed motor drives. One of the benefits of this converter topology is that the multilevel topology eliminates the use for any additional clamping diodes or voltage balancing capacitors. Figure 2.4 shows a diagram of a single-phase CMC [G1-G28].

Each single-phase CMC is associated with its own H-Bridge converter. The converter output voltages of each H-Bridge converter are connected in series with one another per phase. If the switch combinations of switches S_1-S_4 are varied, it is possible to generate three different converter output voltage levels ($+V_{dc}$, $-V_{dc}$ and 0). For the CMC topology, the number of output phase-voltage levels is defined as $m = 2N+1$, where N is the number of separate DC sources [G1-G28]..

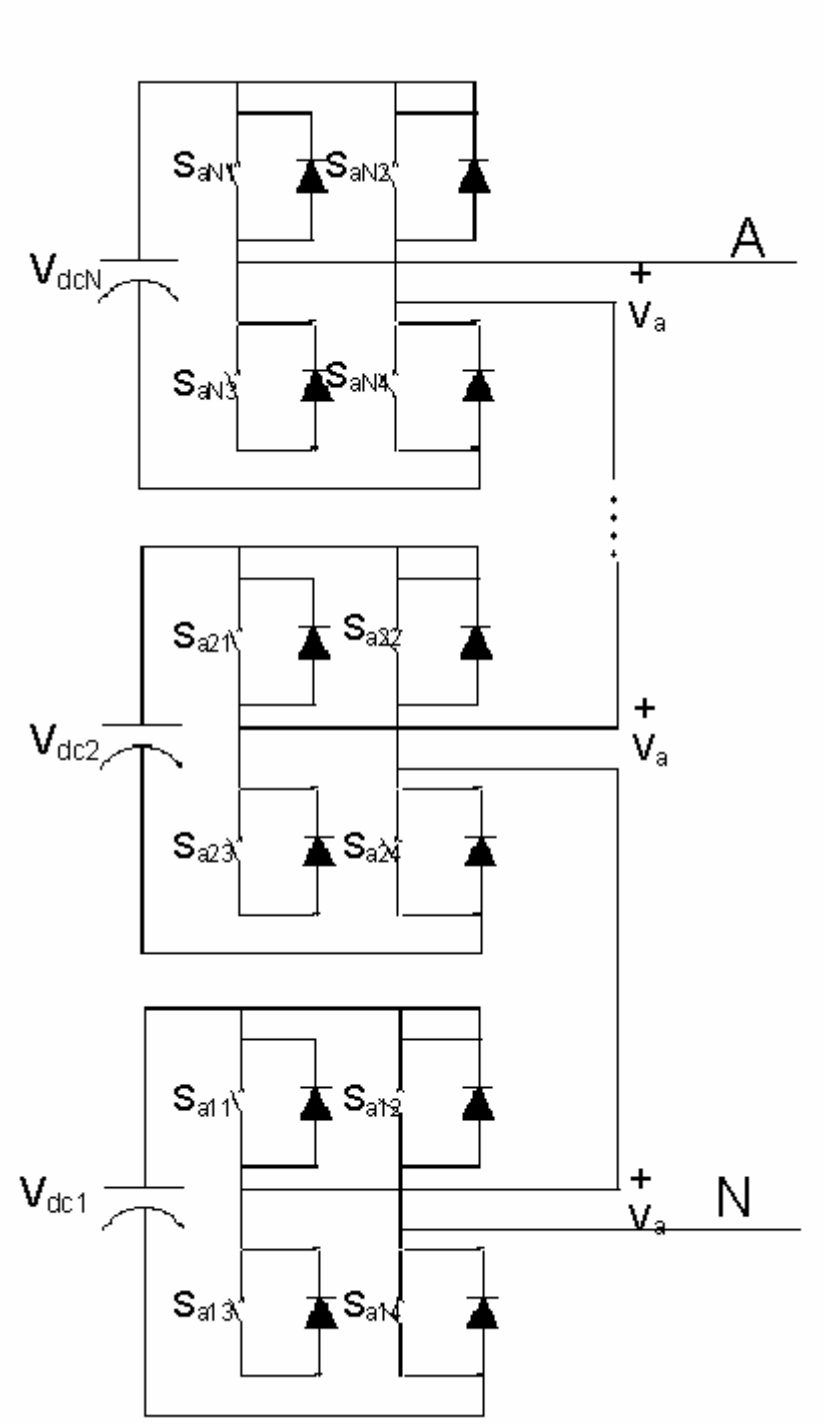


Figure 2.4 - Single-phase structure of the cascaded-multilevel converter.

For a three-phase system, the output voltage of the three cascaded inverters can be connected in either wye or delta configurations. A wye-configured m-level converter using a CMC with separated capacitors is shown in Figure 2.5.

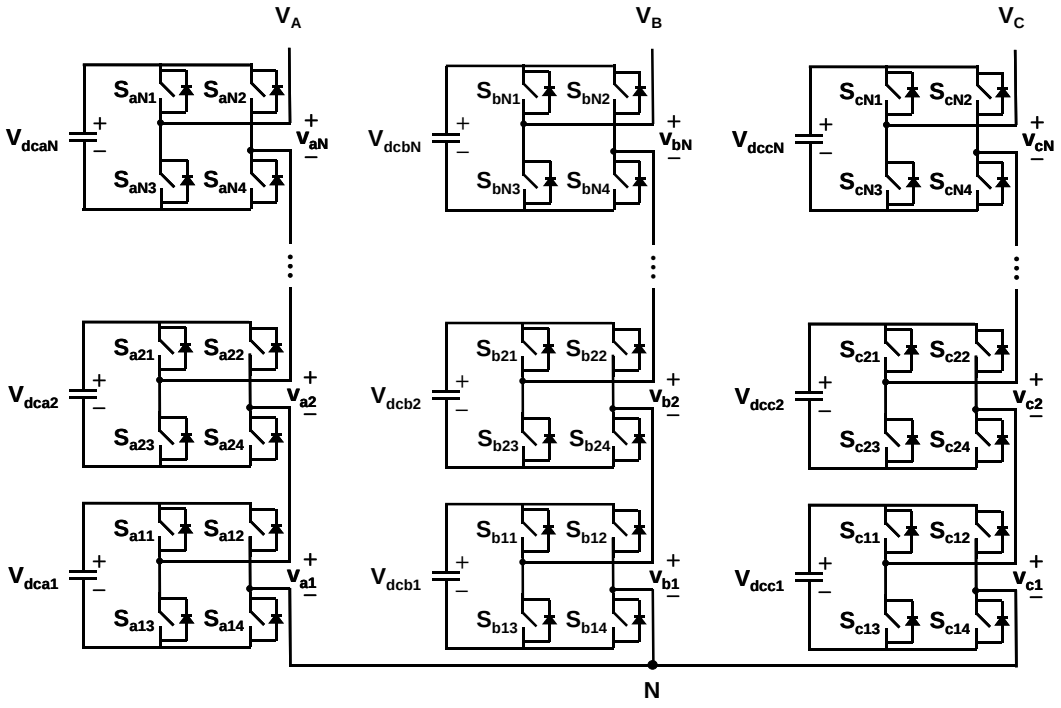


Figure 2.5 - A general three-phase wye-configuration CMC.

B. Hybrid Multilevel Converters

Hybrid multilevel converters can be broken down into two categories. The first category of hybrid multilevel converter can be constructed using a combination of two converters in the first category of multilevel converters and adding additional magnetic circuitry. The second category of a multilevel hybrid converter can be categorized by two basic topologies. The first topology of a hybrid multilevel converter is called a multi-pulse based on two-level and three-level converters [E1], and, the second topology is called a mixed level hybrid cell converter [E2-E3].

Hybrid multilevel converters are not a focus of this thesis. Hybrid multilevel converters are a type of VSC; therefore, they were mentioned here. For more information on hybrid multilevel converters, consult these references [E1-E3].

2.2 Basic Operating Principle of a SSSC

The role that static power converters have in changing the characteristics and operations of power systems can be viewed from examining the requirements and applications of power system compensation. Power system compensation can be viewed from the standpoint of injecting power, usually reactive power, either leading or lagging, into the power system. The primary function of a SSSC is to inject a capacitive (leading) or inductive (lagging) voltage into the power system to partially compensate for the series impedance of the transmission line. Figure 2.6 shows a VSC connected in series with a transmission line via an injection transformer.

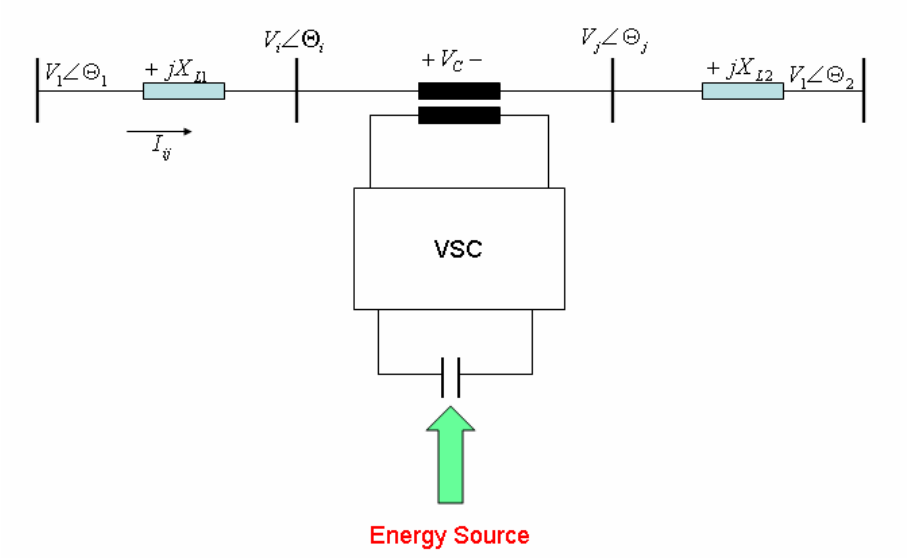


Figure 2.6 - Basic Configuration of a SSSC.

According to the figure, a separate energy source is needed to provide the DC voltage across the DC-Link capacitors and supply the losses of the VSC. Principally, the SSSC is able to interchange both real and reactive energy with the power system. It must be noted that if only reactive power compensation is needed then the size of the energy source needed for the DC-Link capacitors can be small. For reactive power compensation only the magnitude of the voltage is controllable due to the fact that the vector of the inserted voltage is perpendicular to the line current. In other words, the vector of the inserter voltage is either 90º leading or 90º lagging the power system current. The SSSC behaves similar to a voltage source in series with the transmission line. The series voltage source is modeled with an ideal voltage source in series with a reactance. Figure 2.7(a) shows a representation of a series connected voltage source and Figure 2.7(b) shows the resulting Phasor diagram of the equivalent circuit of the SSSC [H1-H11].

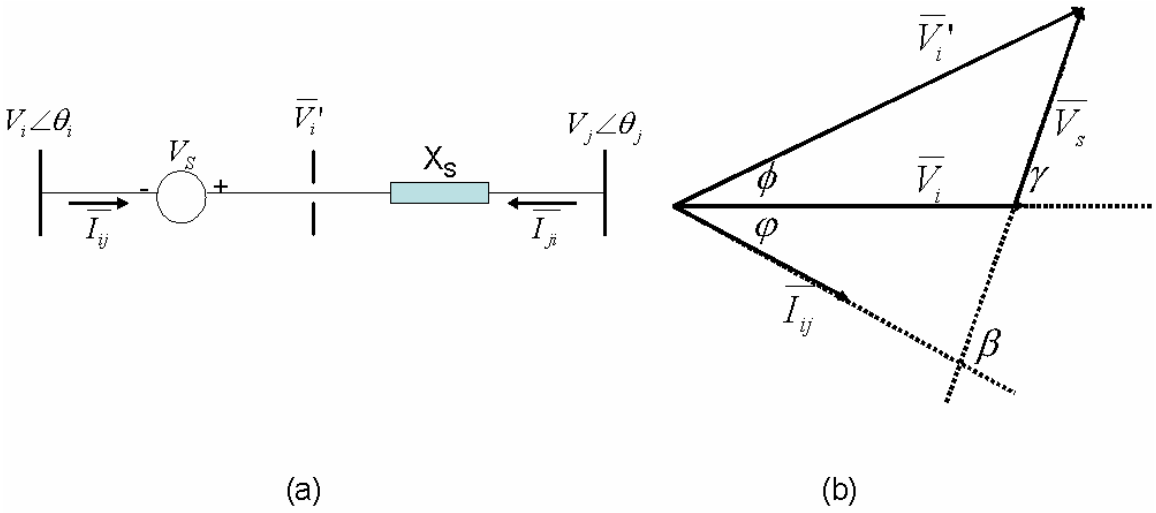


Figure 2.7 – (a) Circuit Diagram of a Series Connected Voltage Source, and (b) Phasor Diagram.

This means that the SSSC can be controlled at any value leading or lagging in the operating range of the VSC. As a result, the overall behavior of the SSSC is very similar to a controllable series reactor or capacitor. The only difference is that the converter based SSSC voltage injection is not related to the line current and can be independently controlled. This fact plays a significant role in that the SSSC is effective for both low and high power system loading conditions [H1-H11].

The potential applications for the SSSC are the same as the controllable series capacitor. In general, a SSSC is used for power flow control, voltage support, and stability enhancement of the power system. The fact that the SSSC can be used to provide both real and reactive power compensation expands the operating region of the converter based SSSC over that of the controllable series capacitor. If the SSSC is used for power flow control, the SSSC can be used to both increase and decrease the flow. The only disadvantage of the SSSC is that at lower voltage levels a high-voltage interphasing transformer is needed. The transformer reduces the effectiveness of the SSSC's compensating ability due to increased reactance. The transformer is also a big cost liability compared with the controllable series capacitor [H1-H11].

2.3 Why use a CMC-Based Converter for a SSSC*?*

Multi-level voltage source converter structures have been developed to overcome the inadequacy in power semiconductor voltage ratings so that they can be applied to high-voltage electrical systems such as FACTS and custom power system applications [G4] and [I1]. Figure 2.8 shows three well-known multi-level voltage source converter topologies discussed above. According to [H1] and [H4], for reactive power compensation or in the case of the SSSC, reactive voltage support, the cascaded converter with separate dc capacitors is a more favorable topology. The cascaded multi-level voltage source topology does not need clamping diodes and the balancing capacitors that the diode clamped converter and the flying capacitor converter need. For this reason, the cascaded multi-level voltage source converter requires fewer primary components. The cascaded converter is constructed the same for each level. Meaning that for a three-phase, three-level SSSC, there would be three identical converters needed for each phase. Thus, the desirable amount of reactive voltage support for the SSSC can be adjusted by simply connecting different numbers of the identical hardware modules together. The primary disadvantage of the diode-clamped topology and the flying-capacitor topology is that the same layout can not be used to expand the converter to higher power levels. Extra clamping diodes and balancing capacitors are needed for these topologies. One of the primary advantages of the cascaded topology is that in the case of the SSSC, if real voltage support is needed, low voltage energy storage elements, such as the ultra-capacitor, can be easily integrated with the HBBB converter units [A3].

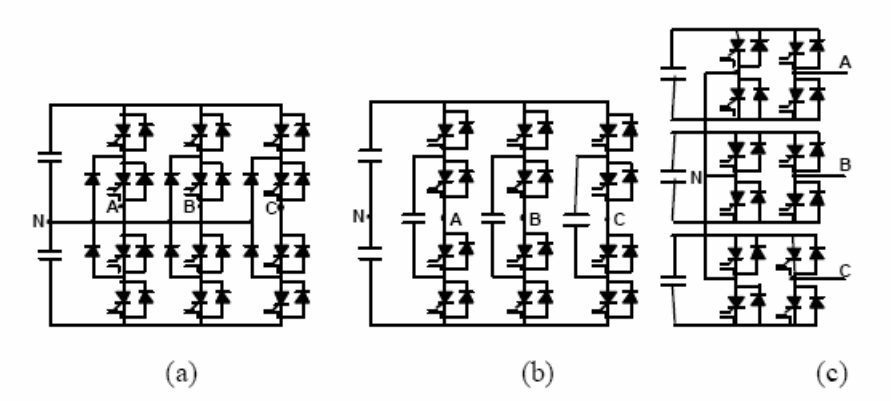


Figure 2.8 – Three types of three-phase multi-level voltage source converters: (a) diode-clamped converter, (b) flying capacitor converter, and (c) cascaded converter.

A. Multi-Level Voltage Source Converters and Sinusoidal Output

There are three ways that multi-level voltage source converters can generate sinusoidal outputs. First, the switching frequency is kept constant for all HBBBs, but more dc power sources are required and thus decrease the total harmonic distortion (THD) in the output waveforms. This accomplishes two things; first, the switching loss of the power switch is minimized and second, the output voltage THD is also minimized. Second, the number of converter levels is kept constant and the switching frequency is increased. For this approach, the limiting factor is the thermal. The faster the power device is switched the more heat is generated. Third, the number of converter levels is increased as well as the switching frequency [F1-F5]. For practical purposes the first approach is more suitable for high-voltage applications such as transmission networks. The cascaded multi-level converter topology is preferable because of its flexible hardware configurations. Figure 2.9 shows a diagram of a seven-level cascaded converter connected in series with the power grid to illustrate what a cascaded multi-level converter configured as a SSSC might look like.

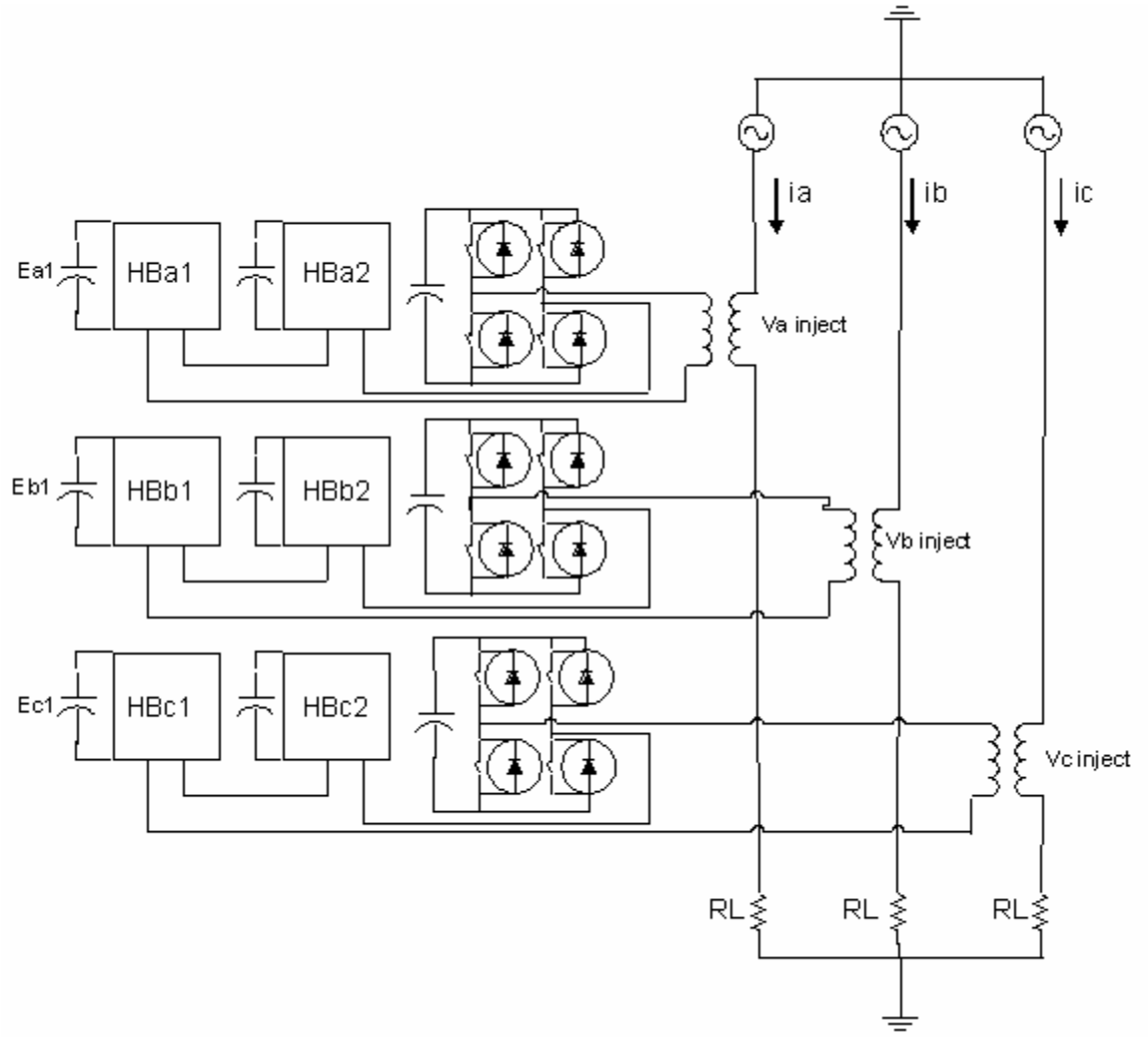


Figure 2.9 – Seven-Level Cascaded Multi-Level Converter Configured as a SSSC.

The overall objective of this thesis is to design a CMC-Based SSSC according to the specification shown in Table 2.4.

TABLE 2.4 - PROPOSED SSSC DESIGN SPECIFICATION

Power System Specification	
Source Voltage	13.8 kV
Line Current	1250 A r.m,s
Voltage Source Converter Rating	
DC Bus Voltage	2500 V
Converter Output Current	1250 A r.m.s
Switching Frequency	1.0 kHz
Reactance Compensating Range	10% - 15% of Line Impedance

2.4 HBBB Design

Table 2.4 shows the specification for a CMC-Based SSSC. At full load the converter hardware is capable of operating with a 2.5 kV dc bus voltage and a 1.25 kA r.m.s. output current. The power capability of the converter hardware is approximately 3.125 MVA per phase. A dv/dt snubber circuit is required. The dv/dt snubber is used to reduce the switching loss of the switching device and as a result increases the long-term switch reliability. A di/dt snubber is also needed because the reverse recovery of the high power diode increases the stress on the device. The schematic of the HBBB complete with snubber circuitry is shown in Figure 2.10(a). S_1 and S_4 are the primary switches, D_1 and D_4 are the primary anti-parallel diodes. The snubber circuit proposed by McMurray [G4] is comprised of dv/dt capacitors C_{SN}, di/dt inductors L_{SN}, auxiliary diodes D_{SN}, and discharge resistors R_{SN}, where N ranges from 1 to 4 [J4]. Figure 2.10(b) shows a picture of a ¼ HBBB Stack and Figure 2.10(c) shows the prototype HBBB converter.

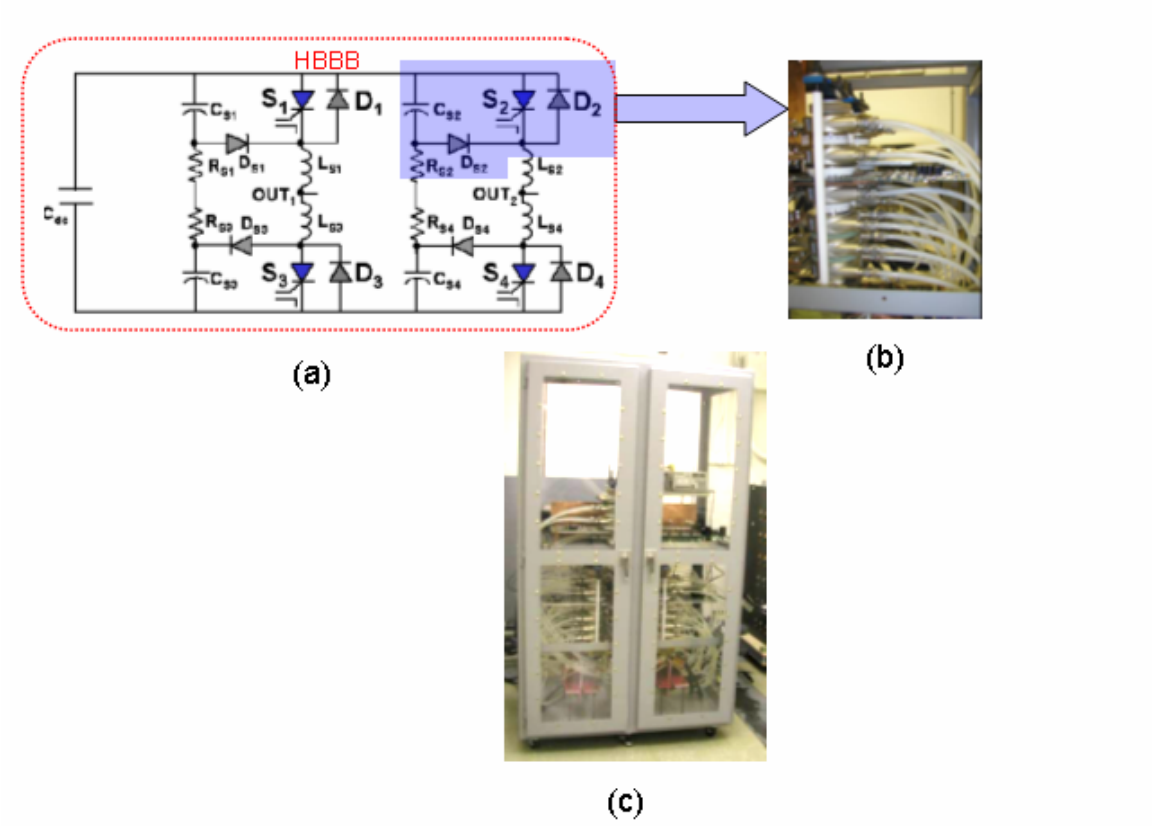


Figure 2.10 – Structure of the H-Bridge Building Block: (a) Schematic, (b) ¼ HBBB Structure, (c) HBBB Prototype.

2.5 Power Stage Design Requirements

The hardware currently developed for the CMC-Based DSTATCOM is based on a modular building block concept. The modular H-bridge building block (HBBB) is intended to be used in high power applications with both real (only with energy storage elements present) and reactive power compensation applications. Due to the fact that the HBBB's have an identical layout, the power stage hardware for each phase of the converter are easily manufactured. Whenever the power requirement of the power system needs to be changed, the HBBB's are simply added into or taken away from the system without redesigning the HBBB component rating [G4].

There are several key parameters that need to be identified when designing the power stage of any voltage source converter. First, the power type of power switching device used in the converter needs to be chosen. The power switching device is chosen based on the design specification for the converter as well as the application in which the converter is intended for. Second, the topology of the converter needs to be chosen. For the SSSC design presented in this thesis the topology chosen for the converter is the cascaded multi-level topology. Third, the HBBB internal component selection needs to be considered. In other words, does the power switching device need a snubber circuit in order to control the voltage overshoot on the device during turn-on? If the answer to this question is yes, then how are these components chosen based on the converter ratings? There is only one main difference between the ETO Based STATCOM power stage and the ETO Based SSSC, that is, the power system interface. The STATCOM is interfaced to the power system in a shunt configuration via a coupling inductor. The SSSC is interfaced to the power system in a series configuration via a coupling transformer.

The remaining sections of this chapter will discuss how the HBBB power stage was designed based on state-of-the-art power semiconductor device. This chapter will also discuss how the power stage for the HBBB could be modified or improved if a non-solid-state device could be used as the main switch for the power converter.

A. Switching Device Selection

In general, FACTS applications are a representative of three-phase power ratings that range in the tens of hundreds of megawatts. FACTS controllers are basically an assembly of ac/dc converters and/or dc/ac converters that make use of high-power

semiconductor devices. The device ratings and characteristics play a pivotal role in the cost, performance, size, weight, and losses of FACTS devices. For example, the faster the switching capability of the power semiconductor device leads to fewer snubber components, lower snubber losses, and lower total harmonic distortion of the converter's output waveform. The following sections of this thesis provide a brief look into the various types of switching devices that could be used for a SSSC design. At the end of this section, a power semiconductor device will be selected for the proposed SSSC.

A1. Conventional Thyristor

The basic operation of the conventional thyristor shown in Figure 2.11(a) is equivalent to the integration of two transistors. One transistor of type pnp and the other transistor of type npn. When a positive gate is applied to the p gate of the upper npn transistor it starts to conduct. The current flowing though the npn transistor becomes the gate current of the pnp transistor causing it to conduct as well. The current through the npn transistor becomes the gate current of the pnp transistor as shown in Figure 2.11 (b). Due to the fact that the current in the npn transistor becomes the gate current of the pnp transistor a regenerative effect occurs that causes latched conduction that results in low device forward drop voltage with the device current being limited by external circuitry. This behavior is very important to understand. The internal regenerative action of the device forces it to saturation. Once the device is turned on, the internal p and n layers are saturated with electrons and holes. As soon as the device goes into its saturation region, the device behaves like a short circuit in the forward direction. In other words, the device behaves like a single pn junction diode. Thus the device's forward drop voltage is only

due to one junction compared to other devices like the IGBT and MOSFET that have two junctions [A2-A3].

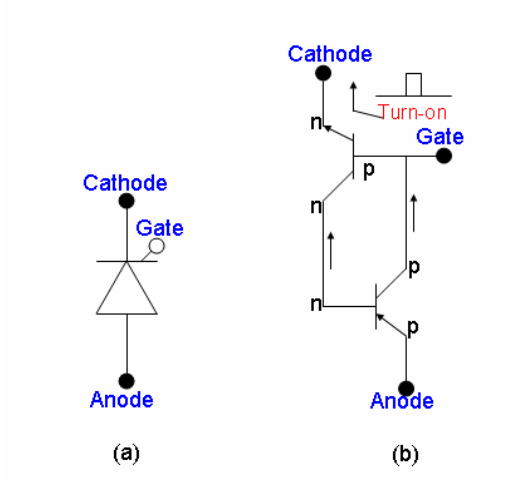


Figure 2.11 - Conventional Thyristor (a) Thyristor Symbol, and (b) Thyristor Equivalent Circuit.

Another important device behavior that must be examined is when a turn-on pulse is applied to the device. When the turn-on pulse is applied, there must be enough anode-to-cathode forward voltage to cause a rapid turn on of the device. If there is not enough anode-to-cathode voltage, the device has a condition known as soft turn-on. If a soft turn-on of the device occurs, there can exist high turn-on loss in parts of the device and can lead to damage [A2-A3]..

A conventional Thyristor at high temperatures has a negative temperature coefficient. At high temperatures the number of thermal carriers and ultimately the number of total carriers increase and this could lead to lower forward drop voltage. Once the device is turned on there must exist a minimum anode-to-cathode current in order for the device to stay on [A2-A3].

Due to the low cost, high efficiency, ruggedness, and high voltage and current capability of conventional Thyristors, their applications are limited to those that do not call for turn-off capability. Higher turn-off capability does not offer sufficient benefits to justify higher cost and losses of the device.

A2. Gate Turn-Off Thyristor

The GTO is similar to the conventional thyristor and is shown in Figure 2.12(a). The GTO is equivalent to the conventional Thyristor except that the turn-off process has been added between the gate and the cathode, in parallel with the turn on. The turn-on process of the GTO is shown only by arrows in Figure 2.12(b) [A2-A3]..

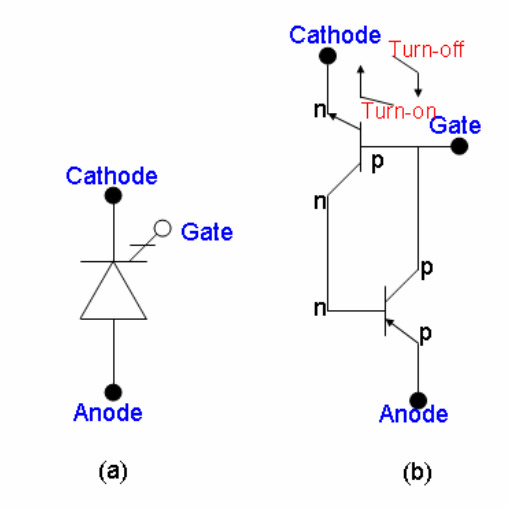


Figure 2.12 - Gate Turn-off Thyristor (GTO), (a) Device Symbol, and (b) Equivalent Circuit.

When a large gate pulse is passed from the cathode to the gate in order to take away enough carriers from the gate, the upper pnp transistor will be drawn out of saturation. As the upper transistor is turned off, the lower transistor is left with an open gate and the device returns to an off state. The required gate current for the GTO to turn off is large;

whereas, the current required to turn-on the device is small. For example, it may take 30 A to turn-on a 1000 A GTO and it may take 300 A to turn it off. The forward voltage required for the device is low (10 – 20 V) and the energy required to turn-off the device is not very big. However, the turn-off losses are high enough to where there maybe significant cost issues when it comes to losses and the cooling requirements for the GTO in converters having many devices. In general, the turn-on process of the GTO behaves like a conventional Thyristor [A2-A3]..

The turn-off process of the GTO requires a larger gate current pulse. The magnitude of the gate current pulse can be as high as 30% greater than the device current. Due to the turn-off requirement, there is a significant time delay (storage time) in the cathode before the current begins to decrease and the voltage begins to increase. As the device turns off the anode-cathode currents begins to decrease rapidly to a low level until the charge carriers recombine in the pn region of the anode side of the device. The delay is responsible for the majority of the turn-off loss of the device. As a result, there is a larger energy requirement for the gate driver [A2-A3]..

A3. Insulated Gate Bipolar Junction Transistor (IGBT)

The IGBT operates as a transistor with high-voltage and high-current capability and a moderate forward voltage drop during conduction. Similar to the conventional thyristor and the GTO, the IGBT has a two transistor structure. The turn-on and turn-off processes are carried out by a MOSFET transistor. During turn-on there is a current flow through the base and the emitter of the npn transistor but not enough to force the device to avalanche into a latched conduction state. The base junction of an IGBT is shunted by a

resistance that is built into the IGBT structure. The resistance is used to bypass some of the cathode current rather than all of it. Figure 2.13(a) shows the IGBT symbol and Figure 2.13(b) shows the equivalent circuit of the IGBT [A2-A3]..

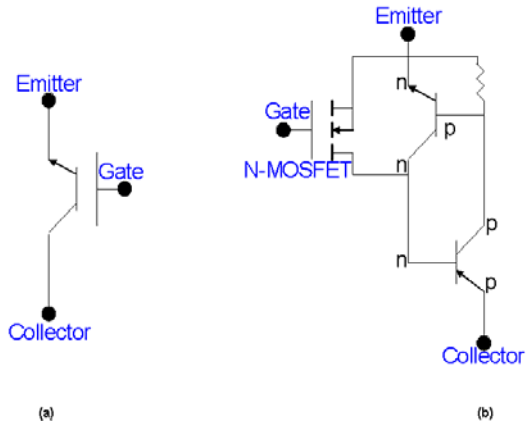


Figure 2.13 - Insulated Gate Bipolar Junction Transistor (IGBT): (a) Symbol, and (b) Equivalent Circuit.

The turn-on process of the IGBT can be described in a similar manner to the turn-on process of a MOSFET. The IGBT turns on when the gate of the MOSFET is positive with respect to the emitter. Type n carriers are drawn into the p channel. The p channel is located near the gate region. As a result, the base of the npn transistor is forward biased and the MOSFET turns on. The IGBT is turned on by applying a positive base voltage to open the channel for n carriers to flow. The turn-off process for the IGBT is simple, the IGBT is turned off by removing the base voltage to close the channel [A2-A3].

The advantages of the IGBT are that the IGBT has a fast turn-on and turn-off process. Due to the fast turn-on and turn-off process of the device, the device becomes ideally suited for use in Pulse Width Modulation (PWM) converter operating at a high switching frequency. Another major advantage of the IGBT for high-power applications is that

IGBT modules have low-switching losses, fast switching speeds, and current limiting capability. The only major disadvantage of the IGBT is that it has a higher forward voltage drop compared to that of the GTO [A2-A3]..

A4. Emitter Turn-off Thyristor (ETO)

The emitter turn-off thyristor or ETO is a new type of MOS-controlled thyristor that is suitable for high power converters due to its improved switching performance and simple control [J1-J3]. Recently, multi-level converters have become an important technology in high power applications. Today, multi-level converters have a particular importance to FACTS devices [J1]. According to [J1–J3], several multi-level converter topologies have been developed and their superiority demonstrated in high power applications. In the past, lower voltage oriented power switches such as the insulated gate bipolar junction transistor (IGBT) has been stacked using the multi-level topology to medium voltage levels. For high power applications IGBT's are not a suitable device. For high voltage applications; however, efforts were seldom made to use the gate turn-off thyristor (GTO) based devices for multi-level converters [J1]. For these reasons and more, there became a need for a new type of power semiconductor switch. Thus, the ETO was developed to incorporate the high switching frequency capability that the IGBT has with the power rating that the GTO has.

If a comparison were made between the conventional GTO, the ETO can be turned off under hard-driven conditions and therefore has a shorter storage time and large reverse-biased safe operational area RBSOA [J3]. One of the primary advantages of the third generation ETO is that it has built in over-current, over-voltage, and over-

temperature protection. All of these additional functions are implemented without the use of any additional external sensors. In addition, the integrated ETO gate driver provides minimum on-time and off-time control, flexible controller interface, on-board power supply, and the protection schemes mentioned above. Thus, the ETO becomes an attractive semiconductor switch to use for high power applications. The question now becomes, how does the ETO work?

Basic Operational Principle of the ETO

Figure 2.14(b) shows the equivalent circuit of an ETO. An ETO is formed by the combination of a GTO with a ring of MOSFETS. The ring of MOSFETS around the GTO is in parallel and represents two switches Q_E, the emitter switch, and Q_G, the gate switch.

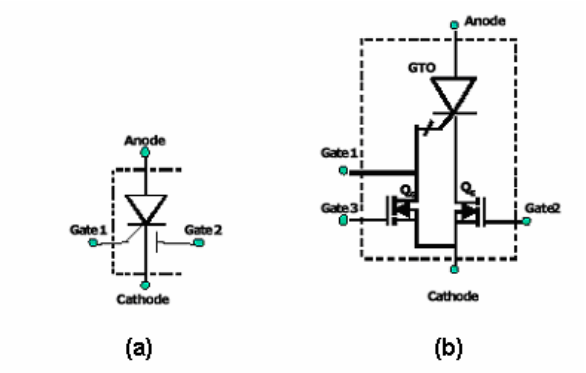


Figure 2.14 – Emitter Turn-off Thyristor (ETO): (a) Symbol, and (b) Equivalent Circuit.

During normal operation when the ETO has a forced turn-off condition Q_E is turned off and Q_G is turned on. The GTO's cathode current is completely bypassed by switch Q_G before the anode voltage begins to rise. If the GTO's cathode current is completely bypassed using switch Q_G, the thyristor latch-up is broken and the ETO is turned off

under the hard driven condition [J3]. When the GTO is turned off, the GTO's anode current will flow through the GTO's via the gate. The current will continue to flow in this manner until to storage time of the GTO ends [J3]. During the turn-on transient condition, Q_E is turned on and Q_G is turned off. A high current pulse is injected into the GTO's gate in order to reduce the turn-on delay time and make the turn-on di/dt faster [J1]. During the time the ETO is switched on the current flows into the anode of the GTO and flows out of the GTO's cathode through the MOSFET switch Q_E [J3]. Also during the time the ETO is on, a small DC current is provided to the GTO's gate in order to ensure that the GTO remains in a state that has a low conduction loss. Figure 2.15 shows a photograph of the 4kA/4.5kV Generation 4 ETO with integrated gate driver used as the main switch for the STATCOM.

Figure 2.15– 4kA/4.5kV Generation 4 ETO.

Figure 2.16 and Figure 2.17 show the ETO turn-off and turn-on waveforms respectively.

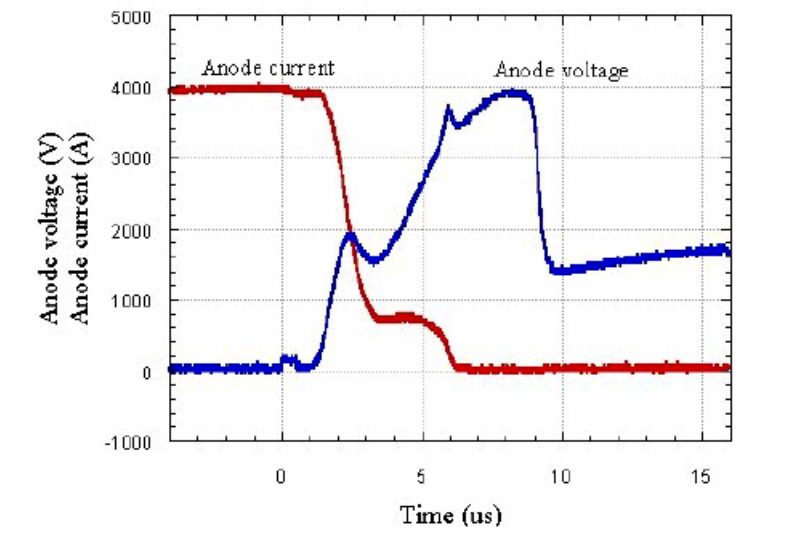


Figure 2.16 – ETO Turn-off Waveform with a 3µF di/dt Snubber Capacitor.

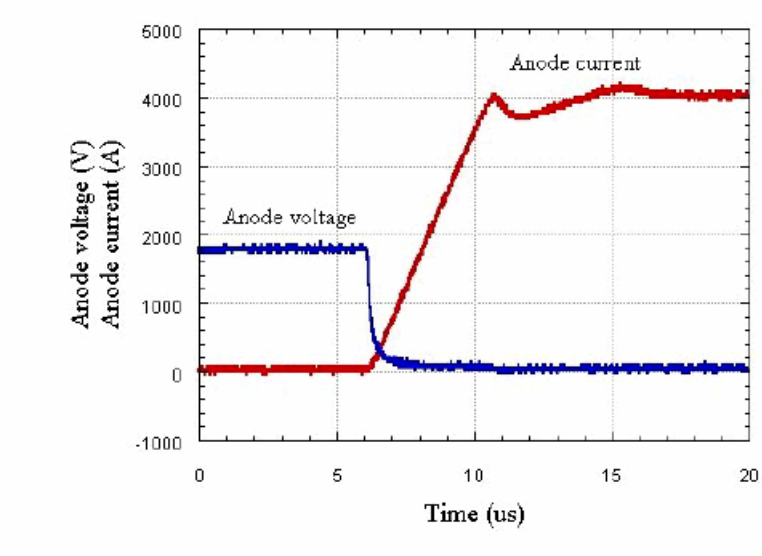


Figure 2.17 - ETO Turn-on Waveform.

ETO Over-Current Protection Capability and Ratings

During the time that the ETO is on, all of the device's anode current will flow through the Q_E MOSFETS. These MOSFETS behave similar to small linear resistors during the time that the ETO is conducting. As a result the voltage drop across these

MOSFETS has a direct relationship to the current flowing through the device; therefore, the voltage drop across the Q_E MOSFETS can be used as the over-current protection feature of the Generation 4 ETO [J1-J3].

The Generation 4 ETO is fairly simple to manufacture and its performance and reliability have been proven [J3]. Table 2.5 shows the device specification for the Generation 4 ETO. The Generation 4 ETO has many advantages in that it has a high power rating, low conduction loss, fast switching speed, suitable for series and parallel operation and mass production. These advantages or characteristics make the ETO a promising candidate for megawatt power conversion applications; therefore, it has been chosen to be used as the primary high power switch for the SSSC design.

TABLE 2.5 - ETO DEVICE SPECIFICATION

Parameters (operation at 2000V DC Bus and 4000 A anode current)	**Ratings & Characteristics**
Repetitive peak off-state voltage	4500 V
On-state voltage	3.3 V
Rate of rise of on-state current	1000A/μs
Rising rate of gate current during turn-on	2000A/μs
Turn-on delay time	3μs
Turn-on Rise time	0.4μs
Turn-on loss per pulse	0.38J
Peak on gate current	200A
DC on gate current	3A
Snubberless turn-off current	4000A
Storage time	1.4μs
Turn-off delay time	4μs
Turn-off Fall time	0.8μs
Rising rate of gate current during turn-off	7000A/μs
Turn-off loss per pulse	13.5J

2.6 Hardware Layout

There are two objectives of the hardware layout for the HBBB. First, the hardware layout must fit into the building block concept and must be easy to manufacture. Second, in order to achieve high power density, the hardware layout needs to be as compact as possible. The parasitic inductance or stray inductance must be kept as small as possible in order to minimize the voltage stress across the ETO caused by the voltage overshoot of the output waveform due to these stray inductances [G4]. As a result, the converter itself must be located as close as possible to the dc capacitor bank and the capacitor snubber loop needs to be as small as possible.

The structure of the HBBB is broken down into four identical sections shown in Figure 2.10(a). The structure of these four identical sections is shown in Figure 2.10(b). The ¼ HBBB stack consists of an ETO (S_2), an anti-parallel diode (D_2), a snubber diode (D_{s2}), a snubber capacitor (C_{S2}), and two discharge resistors in parallel (R_{Sa} and R_{Sb}). To form the H-Bridge structure the four ¼ HBBB stacks are connected together using a copper busbar. The copper busbar was designed using the convention that there must be one square inch of copper per 1 kA of current. Once the ¼ HBBB stacks are connected together, the dc capacitor bank and snubber inductor is connected to the H-Bridge converter to compete a HBBB Phase Leg.

Before the HBBB hardware could be tested, an insulation test must be conducted on each ¼ HBBB stack. Figure 2.18 shows two points on the stack where electrical isolation is important. Point A is the most critical point because this is where the ETO meets the threaded rod of the clamp. Teflon whose thickness is 0.0625 inches is used to provide

electrical isolation between the ETO and the clamp [G4]. The breakdown voltage at this point is measured by using a SERIES HIPOT & MEGOHMETER. At Point A the breakdown voltage is 4.5 kV. The other critical point on the ¼ HBBB stack where isolation is important is the point at which the bottom heatsink is closest to the metal chassis of the HBBB enclosure, denoted as Point B. The breakdown voltage of Point B is 6 kV [G4]. Teflon is used here also to provide electrical isolation. The thickness of the Teflon used to insulate the bottom of the heatsink from the chassis is 0.5 inches.

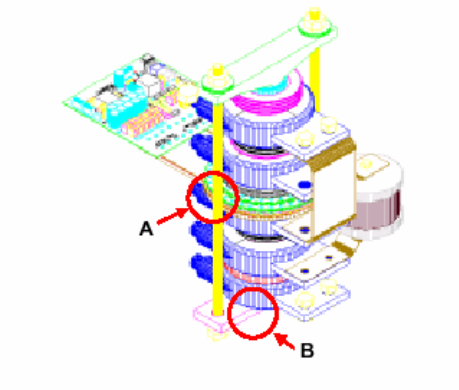


Figure 2.18 – ¼ HBBB Stack with Critical Insulation Points.

A. DC Bus Capacitor Requirement

Figure 2.19 shows the voltage, current, and voltage ripple of the dc capacitor used in the HBBB for reactive power compensation or in the case of the SSSC, the injection of reactive voltage. When the HBBB is operating at a high frequency, the output voltage of the converter is assumed to be sinusoidal with a small harmonic content. The design of the dc bus capacitor takes into consideration only the fundamental components of the converter voltage and current. The general equation for the dc bus capacitance is shown in Equation (), where ΔV_{dc} is the maximum allowable capacitor ripple voltage.

$$C_{dc} = \frac{Q}{\Delta V_{dc}}$$ **Equation 2.1**

The maximum ripple voltage occurs, according to Figure 15, during every π/4 period; therefore, the area Q under the curve shown in Figure 15 is as follows:

$$Q = \int_0^{\pi/4} \sqrt{2} * I_{rms} * \cos(2\pi * f * t) dt$$ **Equation 2.2**

I_{rms} is equal to the rms current of the converter and f is the fundamental frequency [G4]. The final equation for the dc capacitor is expressed below.

$$C_{DC} = \frac{I_{rms}}{\sqrt{2} * \pi * f * \Delta V_{dc}}$$ **Equation 2.3**

The DC-Link capacitance required for the SSSC according to the specification shown in Table 2.4 is C_{DC} = 9.6mF per phase.

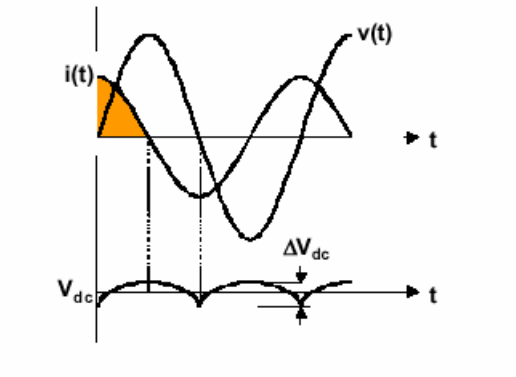


Figure 2.19– Fundamental components of the output voltage, output current, and voltage ripple of the dc capacitors used in the HBBB.

For a given ΔV_{dc}, assuming that the operating rms current is 1.25 kA, the dc bus capacitance requirement is given by Equation 2.3. For a system operating at 60Hz with a 2.5 kV dc bus and a 12% maximum allowable ripple, the required dc bus capacitance is 8.0 mF per phase. The voltage rating of the designed capacitor is 3.0 kV for the SSSC. Customized polypropylene film capacitors will be used for the dc bus capacitance. These capacitors were used for the STATCOM designed in [G4]; therefore, they have a slightly different rating. Additional polypropylene capacitors having the same characteristics but higher voltage rating will be needed for the proposed SSSC. Figure 2.20 shows the designed dc bus capacitor unit which have a 850 μF, 2.5 kV, and 740 A_{rms} rating. Table 2.6 shows the final DC-Link capacitor specification.

TABLE 2.6 - DC LINK CAPACITOR SPECIFICATION

Nominal Capacitance	850.0 μF
Tolerance	+/- 10%
DC Voltage Rating	2500 V
E.S.R.	< 0.001 Ω
Inductance	20 nH
Maximum Peak Current	55000 A
DV/DT	70 V/μs

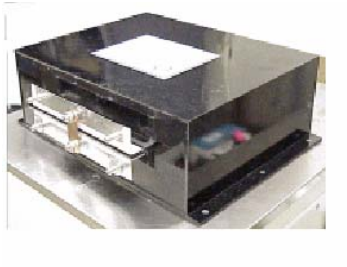


Figure 2.20 – DC Bus Capacitor.

B. Snubber Inductor Design

During the turn-on process of the ETO, the di/dt is limited by the snubber inductor. The top and bottom ETO in each phase leg share the same snubber circuit. Figure 2.21(a) show a schematic of the snubber and Figure 2.21(b) shows a picture of the actual snubber inductor used in the H-Bridge converter. In order to increase the total inductance, two series inductors (L_{S1} and L_{S2}) are magnetically coupled with a mutual coefficient k. The total series inductance of the snubber inductor is $2L_s(1+k)$. To avoid saturation and core losses of the inductor an air-core inductor is chosen. According to [G4], an air-core inductor, compared to the conventional iron-core inductor is expected to lower losses and lighter weight.

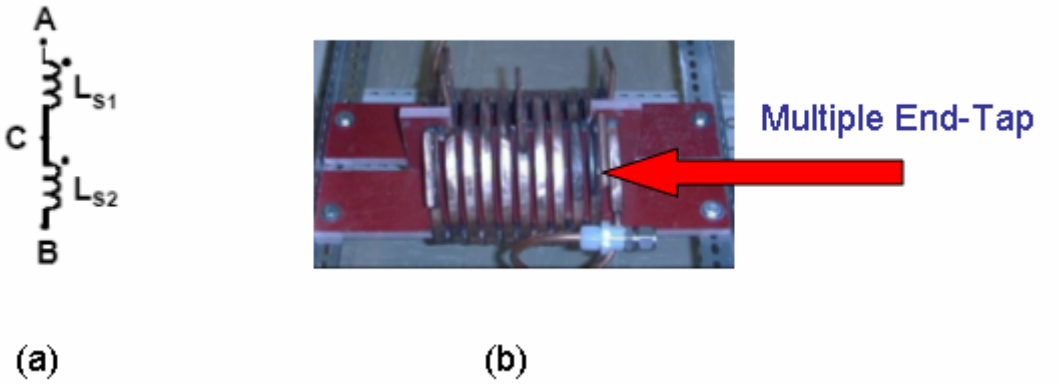


Figure 2.21 - Snubber Inductor: (a) Schematic, and (b) Actual Inductor.

The snubber is designed to limit the di/dt of the ETO's anode to 500 A/µs. This value is chosen based on the maximum allowable turn-on di/dt of the antiparallel diode. According to the datasheet for the ABB diode used, the maximum allowable turn-on di/dt

is 650 A/μs. Some design margin is required; therefore, the di/dt of the snubber inductor is 500 A/μs. The designed DC bus voltage of the SSSC is 3 kV, the required total inductance is 6μH. In other words, L_{S1} and L_{S2} are equal to 3 μH. The snubber inductor shown in Figure 2.21 (b) has the capability to be adjusted from a range of inductance by using the end taps of the inductor.

C. BusBar Requirement

There are only two main design considerations that need to be considered for the copper bus structure. First, the copper pieces need to be designed in such a way as to minimize the amount of parasitic inductance induced into the converter. Parasitic inductance equates to converter losses due to heat. The primary design concern for the DC bus is to minimize the amount of losses in the converter due to the copper bus. This is done by minimizing the length of the copper pieces from each connection point. The copper pieces need to be as short as possible from one point to another. Second, the copper bus must be designed to handle the maximum allowable converter current. For current handling capability, the DC busbar for the HBBB is designed according to the specification that for every 1000 A r.m.s of current flowing through the converter, the surface area of copper is required to be $1inch^2$. The heatsink's shown in Figure 2.10(b) of the HBBB structure have an electrical connection point that is three inches in length; therefore, the required thickness of the copper bus is 0.333 inches. Figure 2.22 shows an AutoCAD drawing of one of the HBBB copper connections.

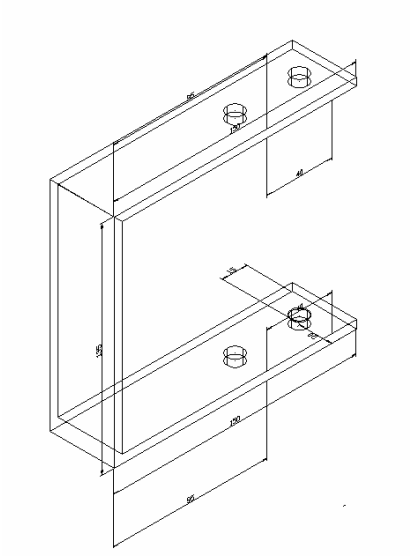


Figure 2.22 – AutoCAD drawing of one HBBB copper connection.

There is a laminated busbar used to connect the DC-Link capacitors in parallel. The busbar consists of five layers and a diagram is shown in Figure 2.23. Two of the five layers are copper and the other three layers are a garolite insulator. To withstand 3 kV across the positive and negative copper busbar, 1/8'' thick garolite sheets are used. In order to provide the maximum amount of safety, the front and back sides of the busbar are also covered with garolite. The copper sheets that are used to connect the positive and negative terminals of the capacitors together are 0.064''-thick and can withstand approximately $1.5kA_{peak.}$ The overall dimensions of the copper bus structure are 36''X24''.

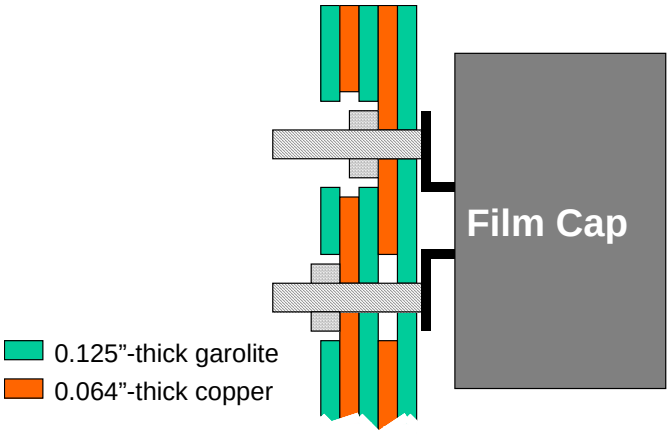


Figure 2.23 - Cross-sectional drawing of the laminated busbar.

D. Coupling Injection Transformer Design

The main key magnetic component for SSSC applications is the coupling transformer. At the transmission level, the leakage inductance of the coupling power transformer can serve as the coupling inductor, as long as its size is suitable. A single-line diagram shown in Figure 2.24, illustrates the connection of the coupling inductor and the coupling transformer to the Power Grid. The coupling inductor can serve as a low-pass filter for either a power electronic converter or a reactive power coupler. The size of the coupling inductor, however, plays an important role in the performance of the SSSC system.

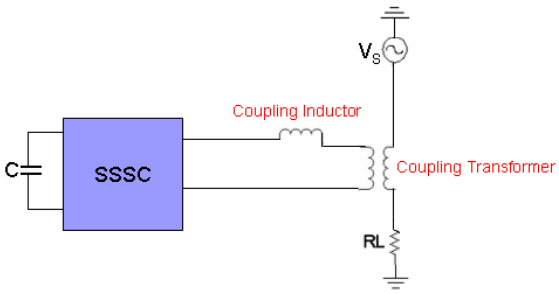


Figure 2.24 - Connection between coupling inductor and coupling transformer.

The coupling inductor and coupling transformer are calculated as follows:

Coupling Inductor

$$X_S = \frac{\frac{V_{o\_Max}}{\sqrt{2}} - V_{inj\_phase}}{I_o} \qquad X_S = 141.4m\Omega \quad \textbf{Equation 2.4}$$

$$L_S = \frac{X_S}{2 * \pi * f} \qquad L_S = 375.1\mu H \quad \textbf{Equation 2.5}$$

Assuming that the losses of the coupling inductor are approximately 10% of the coupling inductor's impedance then the loss resistance can be calculated as follows:

$$R_S = \frac{X_S}{10} \qquad R_S = 14.1m\Omega \quad \textbf{Equation 2.6}$$

Coupling Transformer

The coupling transformer is modeled as an equivalent impedance. If the assumption is made that a standard transformer for a 13.8 kV system is used, then the equivalent inductance for the transformer is between 0.035 per-unit and 0.12 per-unit. If the coupling transformer inductance is assumed to be 0.10 per-unit then:

$$kV_{Rating} = 13.8kV \qquad X_{spu} = 0.10 \qquad MVA_{Rating} = \sqrt{3.0} * I_o * V_{inj\_line} \quad \textbf{Equation 2.7}$$

$$Z_B = \frac{V_{inj\_line}{}^2}{MVA_{Rating}} \qquad Z_B = 1.1 \qquad \textbf{Equation 2.8}$$

$$X_{base} = X_{spu} * Z_B \qquad X_{base} = 113.1m\Omega \qquad \textbf{Equation 2.9}$$

$$L_{eq\_pu\_trans} = \frac{X_{base}}{2 * \pi * f} \qquad L_{eq\_pu\_trans} = 300.1\mu H \qquad \textbf{Equation 2.10}$$

Assuming that the losses for the transformer are approximately 10% of the coupling transformer impedance then:

$$R_{S\_trans} = \frac{X_{base}}{10} \qquad \textbf{Equation 2.11}$$

$$R_{s\_pu\_trans} = \frac{R_{S\_trans}}{Z_B} \qquad R_{s\_pu\_trans} = 10m\Omega \qquad \textbf{Equation 2.12}$$

Since the coupling transformer impedance was calculated on a per-unit base. The coupling inductor must also be calculated according to the same per-unit base. If this is done then the per-unit impedances for the coupling transformer are as follows:

$$L_{S\_pu\_ind} = 331.6\mu H$$
$$R_{S\_pu\_ind} = 12.5m\Omega$$

Due to the fact that the coupling inductor and the coupling transformer leakage inductance is approximately equal. The coupling transformer's leakage inductance will be used for the coupling inductance parameter.

E. Converter Cooling Requirements

The primary objective of cooling the HBBB converter is to maintain a safe operating temperature of the components inside the converter. The first step in the design process for the water cooling system is to identify the "hot spots" inside the converter. This is done by calculation and measurement. Figure 2.25 shows the components in a typical

HBBB stack. It was determined that the two "hot spots" within this stack are the ETO and the ceramic resistor.

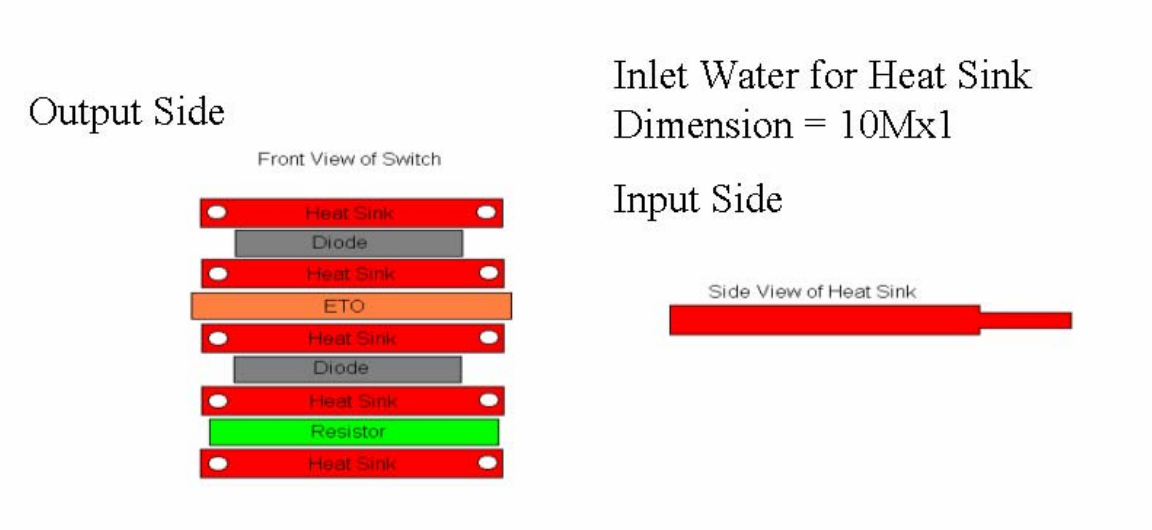


Figure 2.25 - Typical HBBB Stack

The first step is to calculate the thermal resistance of the ETO and to determine the maximum power dissipation (i.e. losses) of the device. The thermal resistance junction-to-case of the ETO is 12k/kW. The power dissipation of the ETO can be calculated as follows:

$$P_{\max} = \frac{T_{junction} - T_{case}}{R_{thJC\_ETO}} = \frac{125-80}{12} = 3.75kW \; or \; 4k/kW \qquad \textbf{Equation 2.13}$$

The worst case scenario occurs if one heatsink is required to dissipate 4k/kW in losses. The next step is to calculate the thermal resistance of the heatsink.

$$P_{\max\_HS} = \frac{T_{case} - T_{HS}}{R_{thJC\_HS}} = \frac{80-25}{R_{thJC\_HS}} = 4k/kW; R_{thJC\_HS} = 13.75k/kW \; or \; 14k/kW \qquad \textbf{Equation 2.14}$$

Next, the theoretical calculations needed to be verified via measurement. It was concluded that the thermal resistance for cathode side of the ETO is 35k/kW and for the anode side of the ETO the thermal resistance is 20k/kW. These two thermal resistances are in parallel; therefore, the total thermal resistance of the ETO is 12.7k/kW. Next, the plot shown in Figure 2.26 is used to illustrate the relationship between flow rate and the heatsink thermal resistance. If an estimated flow rate of 1 GPM (gallon per minute) is used then the thermal resistance of the heatsink is 7k/kW assuming the water temperature is kept at 55ºC.

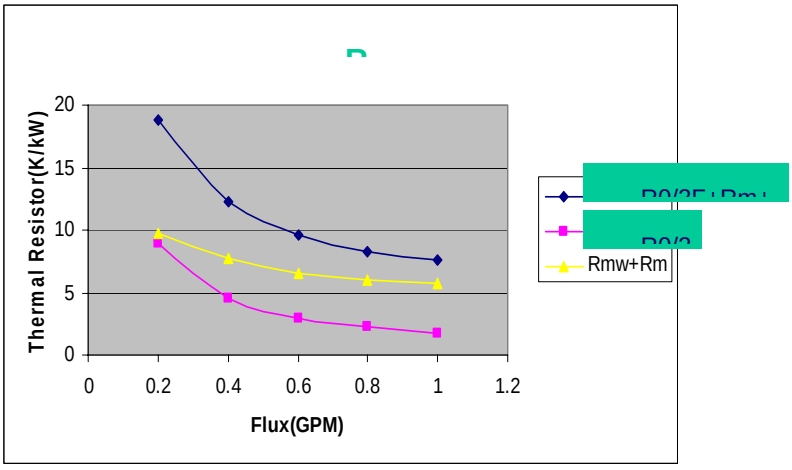


Figure 2.26 Thermal resistance of the heatsink verses flow rate.

It was determined that the combined thermal resistance of the ETO and heatsink inside the HBBB is 23.5k/kW. Figure 2.27is used to illustrate this.

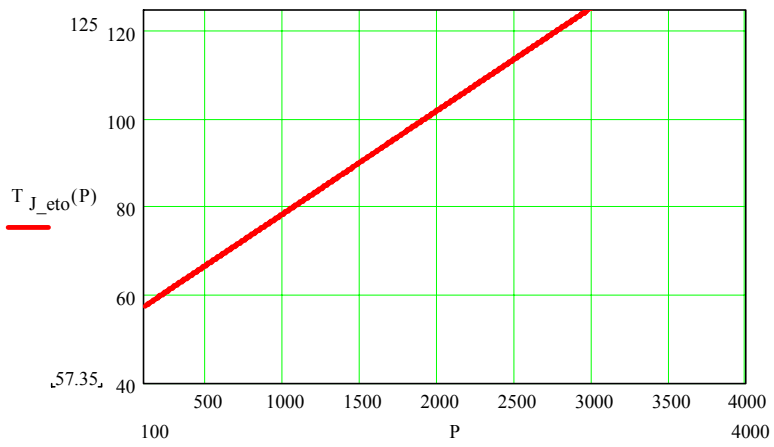


Figure 2.27 - ETO Temperature verses Power Loss inside the HBBB.

The next step is to calculate the maximum power dissipation for the ceramic resistor. This was done by examining the resistor's datasheet. The ceramic resistor can have a thermal impedance of (130 k/kW – 165 k/kW) with 145k/kw as a suggested value. The maximum power loss in the resistor is 1kW which equates to approximately a 150ºC temperature rise. These results need to be verified via an experiment. A test was setup where 1kW of DC input power was supplied to the resistor. Four different thermal resistances were calculated based on the theoretical 1GPM flow rate. Figure 2.28 is used to illustrate the test setup.

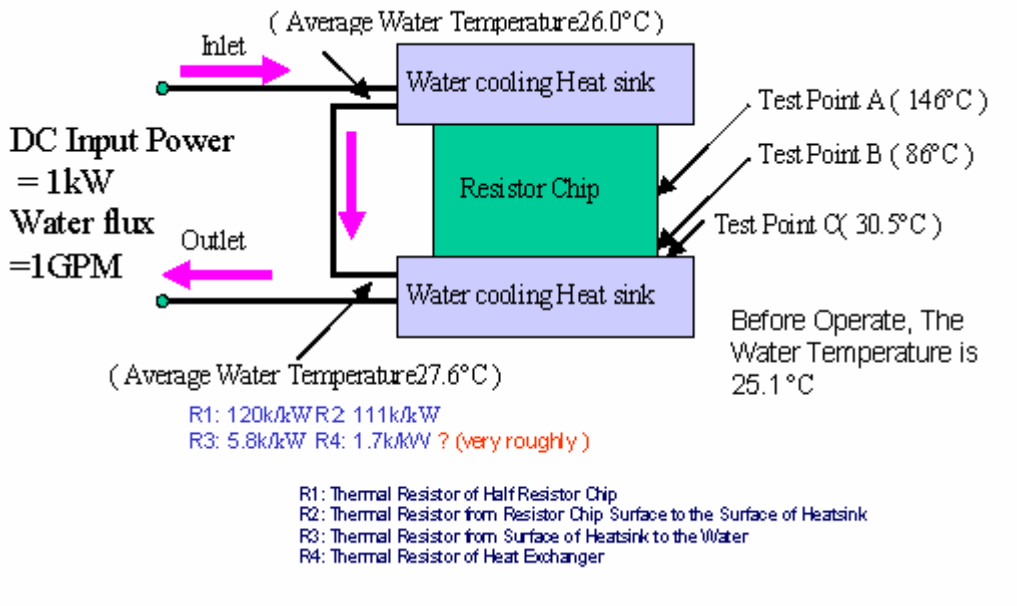


Figure 2.28 - Ceramic Resistor Test Setup.

If it is assumed that all four of these thermal resistances are in parallel as shown in Figure 2.29, then the combined thermal resistance of the double-side cooling resistor would be equal to the parallel combination of these four resistors.

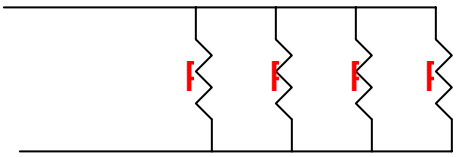


Figure 2.29 - R_1 – R_4 in parallel.

The total thermal impedance of the ceramic resistor is approximately 1.5k/kW. If the proposed flow rate of 1GPM is used then the thermal impedance of the heatsink is 7k/kW; therefore, the total thermal impedance is approximately 8.5 k/kW. The datasheet for the heatsink contains a flow rate curve shown in Figure 2.30. From Figure 2.30, it can be concluded that the desired flow rate for the HBBB converter should be 1GPM. The 1GPM flow rate corresponds to a thermal resistance of 8.5 k/kW.

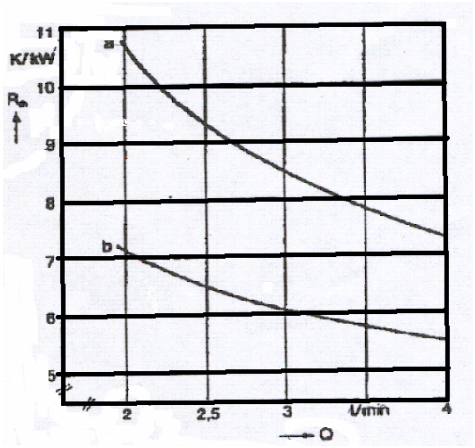


Figure 2.30 - Flow Rate Curve from Heatsink Datasheet.

Finally, the water cooling systems were designed according to common standards for deionized water quality. The water cooling manifolds were constructed out of 1 inch diameter 304 stainless steel. The tubing used to connect the water lines to the heatsinks was made out of 3/8 inch outside diameter nylon tubing. The inlets and outlets that were used to supply water to and bring water from the heatsinks were 3/8 inch 304 stainless steel compression fittings. The inlets and outlets for the heatsinks themselves were 3/8 inch compression fittings with M10 thread. The M10 thread corresponds to thread pattern of the heatsink. The 3/8 inch diameter for all of the tubing and fittings was selected based on the fact that the metric M10 measurement is very close to the standard 3/8 inch diameter. The desire is to use standard size fittings when possible.

2.7 Summary

A brief explanation of the VSC topologies as well as the basic operating principle of the SSSC has been presented. The configuration and structure of the high-voltage ETO-based HBBB has also been presented. A summary of the various types of power

semiconductor devices that could be used in a VSC configured as a SSSC has been discussed. Because of their identical layout, the HBBBs are simple to manufacture. Their modularity makes the entire system flexible in terms of power capability. By connecting these modules in series, the CMC topology that is suitable for reactive power compensations can be readily implemented. Finally, the overall specification for the proposed SSSC has been derived. Table 2.7[1] summarizes the specification for the proposed SSSC.

TABLE 2.7 - SPECIFICATION FOR THE PROPOSED SSSC

Power System Specification	
Source Voltage	13.8 kV
Line Current	1250 A r.m,s
Voltage Source Converter Rating	
Main Switch	4.5kV/4.0kA ETO
DC Bus Voltage	2500 V
DC Bus Capacitor	9.6 mF/phase
Converter Output Current	1250 A r.m.s
Switching Frequency	1.0 kHz
Coupling Inductor Impedance	331.6 μH
Coupling Inductor Loss Resistance	12.5 mΩ
Coupling Transformer Impedance	300.1 μH
Coupling Transformer Loss Resistance	10.0 mΩ
Reactance Compensating Range	10% - 15% of Line Impedance

[1] Refer to Appendix A for the SSSC Design Specification Derivation

Chapter 3 Modeling of a Cascaded-Multilevel-Based SSSC

3.1 Operating Principle of the Cascaded Multilevel Converter-Based Static Series Synchronous Compensator (SSSC)

A schematic of a cascaded multilevel converter (CMC) based SSSC is shown in Figure 3.1. The SSSC system is comprised of three main parts: a multilevel-cascaded voltage source converter with separate dc link capacitors, a coupling transformer, and a controller.

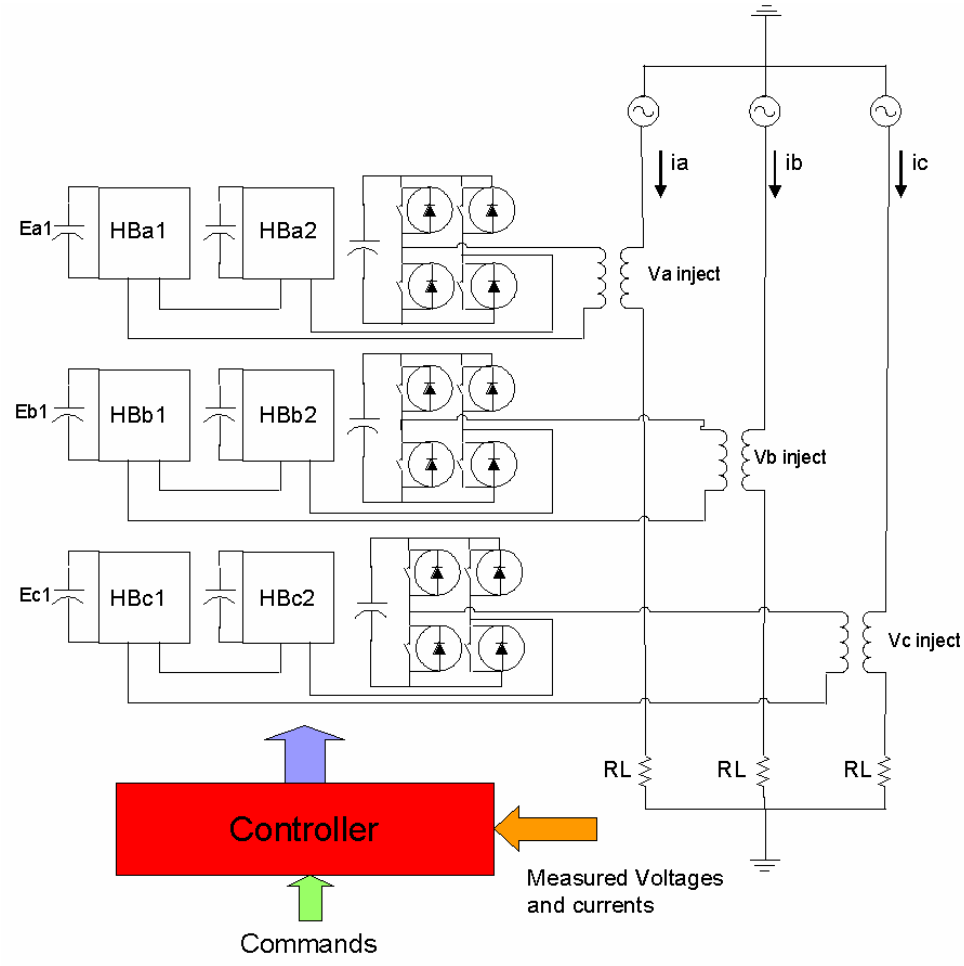


Figure 3.1 - Schematic of CMC Based SSSC System.

As discussed in Chapter 2, the CMC consists of a number of identical H-Bridge

converters, whose output is connected in series with the transmission line via a coupling transformer. The number of output line-to-neutral voltage levels equals 2N+1. The main purpose for the coupling transformer is to provide electrical isolation for the converter from the power system and to step-up the voltages that are injected into the network if needed. To make the entire system work effectively and perform properly a carefully designed controller is needed. All the necessary line voltages are measured and fed into the controller to be compared with the controller commands. The controller then performs feedback control and outputs a set of switching signals (duty cycles) to drive the main switches of the power converter. The single line diagram of the SSSC is shown in Figure 3.2. The CMC is generally represented as an ideal voltage source associated with internal losses connected to the ac power grid via a coupling transformer.

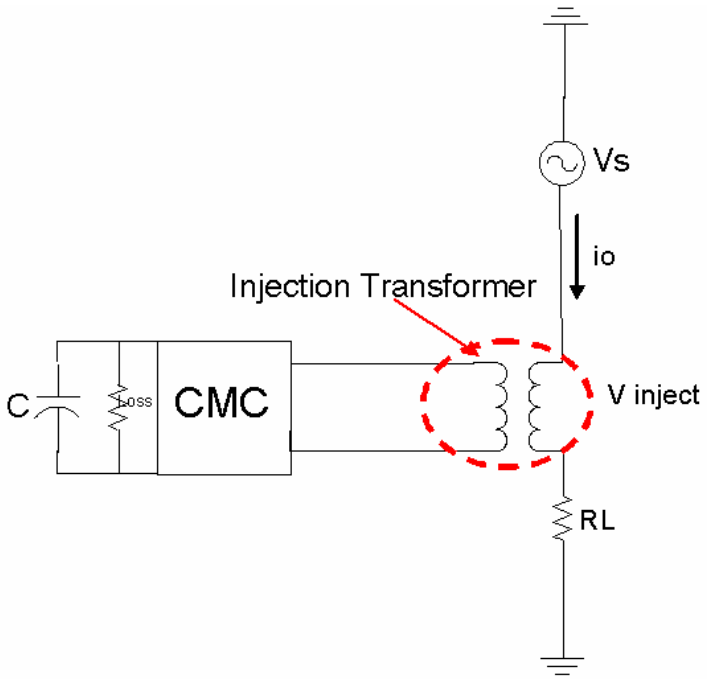


Figure 3.2 - Single Line Diagram of the CMC Based SSSC.

One of the primary functions of a SSSC is to provide power flow control to the power

grid. The power flow on a transmission line can be controlled by changing the converter's output voltage. If the converter is to be operated in capacitive mode, +Q, the converter output voltage lags the line current by 90º. If the converter is to be operated in inductive mode, -Q, the converter output voltage leads the line current by 90º.

For practical applications, the converter is associated with internal losses caused by the power semiconductor devices used as well as the converter's passive components. As a result without any control, the dc capacitor voltage will decrease. To regulate the capacitor voltage; a phase shift is needed between the converter output voltage and the power system voltage.

3.2 Modeling and Feedback-Control Development

This section summarizes the development procedures used to model a cascaded-multilevel converter-based SSSC. The process starts with generating a switching model of the power converter and then an average model in abc coordinates. The average model is integrated with a linear model of a three-phase power system. The linear model of the three-phase power system includes ac sources and coupling transformers. In order to implement the decoupling controller, the average model of the SSSC in abc coordinates is transformed into a model in dq0 coordinates. To design the feedback control loops using linear compensators, a small signal model of the ac system in dq0 coordinates is derived for its average model in the same coordinates. Figure 3.3 shows a diagram of the control development of the cascaded-multilevel converter-bases SSSC.

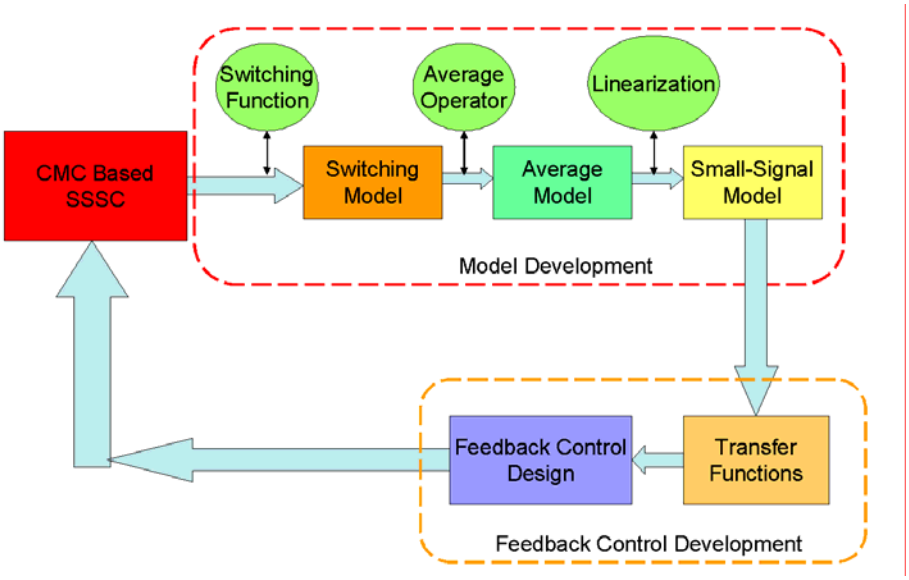


Figure 3.3 - Control Development for the Cascaded-Multilevel Converter-Based SSSC.

The model development flow chart is shown in Figure 3.4. The modeling process starts with a definition of the switching functions. The CMC is represented by a switching model in an abc coordinate system. The next step in the modeling process is to apply the average operator to the switching functions. During this step all of the switching functions are neglected and only the fundamental components are considered. The duty cycles are the main control parameters that are derived from the average model. The duty cycles are used to provide the switching signals to the CMC. First, a generalized average model is derived in abc coordinates. This model can be used in any type of power-conversion systems. The derived average model of the SSSC is combined with the linear model of a three-phase ac system. The combined model constitutes the equivalent average model for the system under study.

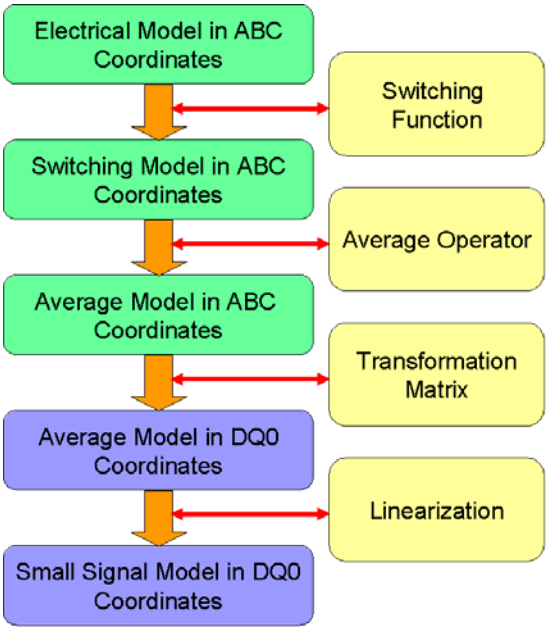


Figure 3.4 - Model Development Procedures.

According to the flow chart, the average in the abc coordinate frame must be transferred to an average model in the DQ0 frame. Once the average model in abc coordinates has been transferred into DQ0 coordinates, a linearization step is necessary to derive the small signal model for the SSSC. Transfer functions for the system are then derived from the small signal model. In the synchronous frame, all ac parameters become dc parameters [G4]. In other words, the converter behaves similar to a dc-to-dc converter. As a result, classical linear control techniques can then be applied to the CMC. Since simple linear control techniques can be applied to the CMC, the stability and feedback loops can be evaluated and the control parameters can be optimized for peak performance. Also, the real and reactive components of the system can be controlled independently of one another.

A. Switching Sequence

The CMC consists of many different H-Bridge converters connected in series. The simplified structure of the H-Bridge is shown in Figure 3.5.

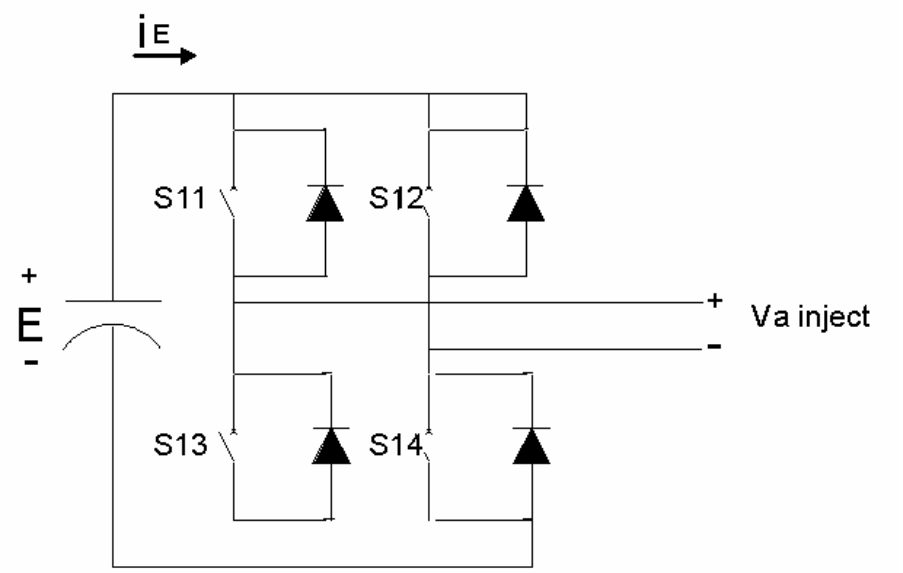


Figure 3.5- Basic Structure of an H-Bridge Converter.

There are three possible output voltage levels that can be synthesized from the possible switching combinations. These voltage levels are shown in Figure 3.6.

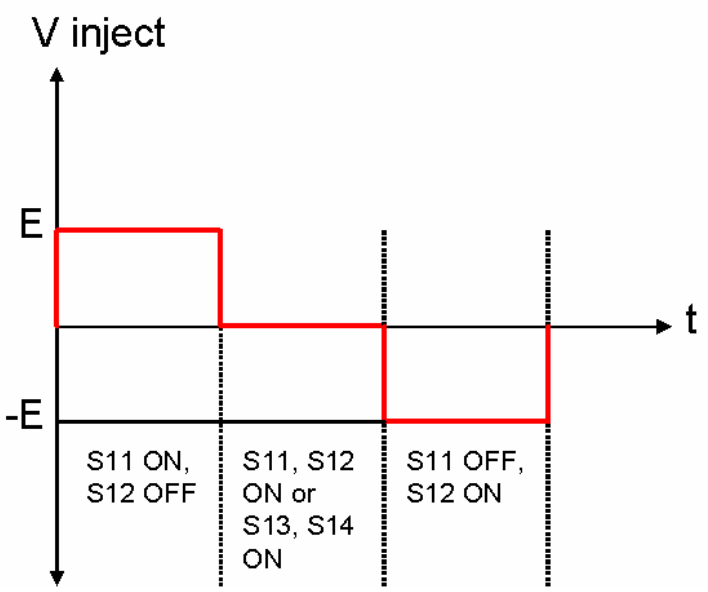


Figure 3.6 - Output Voltage of H-Bridge Converter.

In order to prevent a short circuit, the top and bottom switches in the same phase leg of the CMC must not be turned on at the same time. In other words, whatever state that the top switch is in (either on or off) the bottom switch must be opposite. The equivalent circuit of the H-Bridge is shown in Figure 3.7. To illustrate the relationship between the output current and voltage on the dc side of the converter and on the ac side of the converter, four possible switch combinations are shown in Table 3.1.

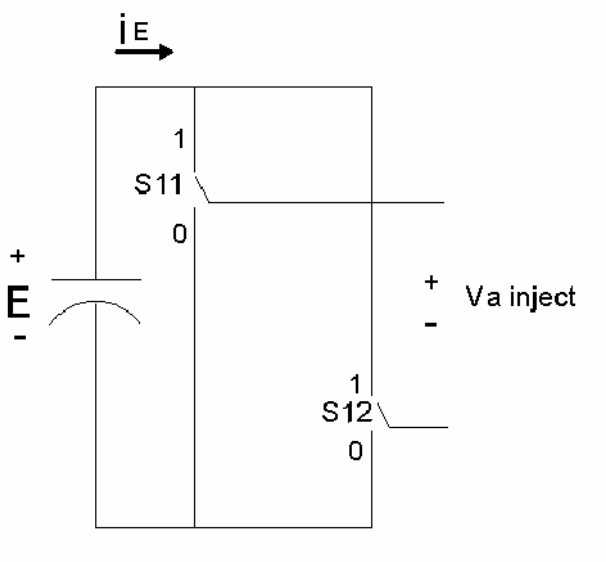


Figure 3.7 - Equivalent Circuit of the H-Bridge Converter.

Table 3.1 - CMC Switch Combinations

S_{11}	S_{12}	V_{inject}	i_E
0	0	0	0
1	0	E	i_o
0	1	-E	$-i_o$
1	1	0	0

According to [G4], the relationship between the dc voltage and the converter output voltage as well as the capacitor current and the converter output current are represented in Equations 3.1 and 3.2. The converter output current equation must be equal to the line current of the power system because the SSSC is connected in series with the power system.

$$V_0 = (S_{11} - S_{12})E \qquad \textbf{Equation 3.1}$$

$$i_E = (S_{11} - S_{12})i_o \qquad \textbf{Equation 3.2}$$

S_1 can be defined as the difference between the status of the two top switches.

$$S_1 = (S_{11} - S_{12}) \qquad \textbf{Equation 3.3}$$

By substituting Equation 3.3 into Equations 3.1 and 3.2

$$V_0 = S_1 E \qquad \textbf{Equation 3.4}$$

$$i_E = S_1 i_o \qquad \textbf{Equation 3.5}$$

The derived switching model for the H-Bridge converter is shown in Figure 3.8. Each H-Bridge converter shown in Figure 3.5 can be replaced by the switching model in Figure 3.8. The result is the final switching model of the CMC shown in Figure 3.9.

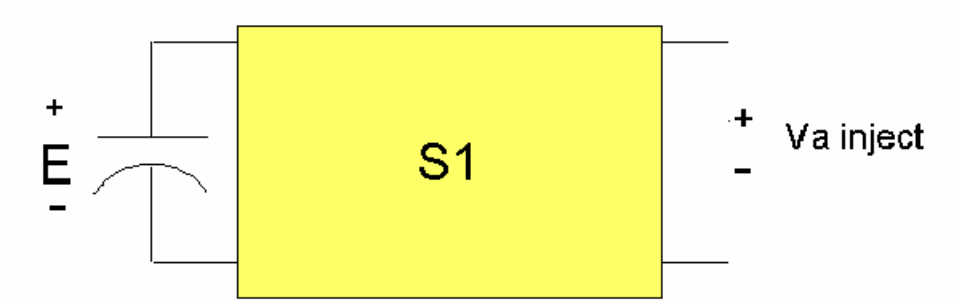


Figure 3.8 - Switching Model of the H-Bridge Converter.

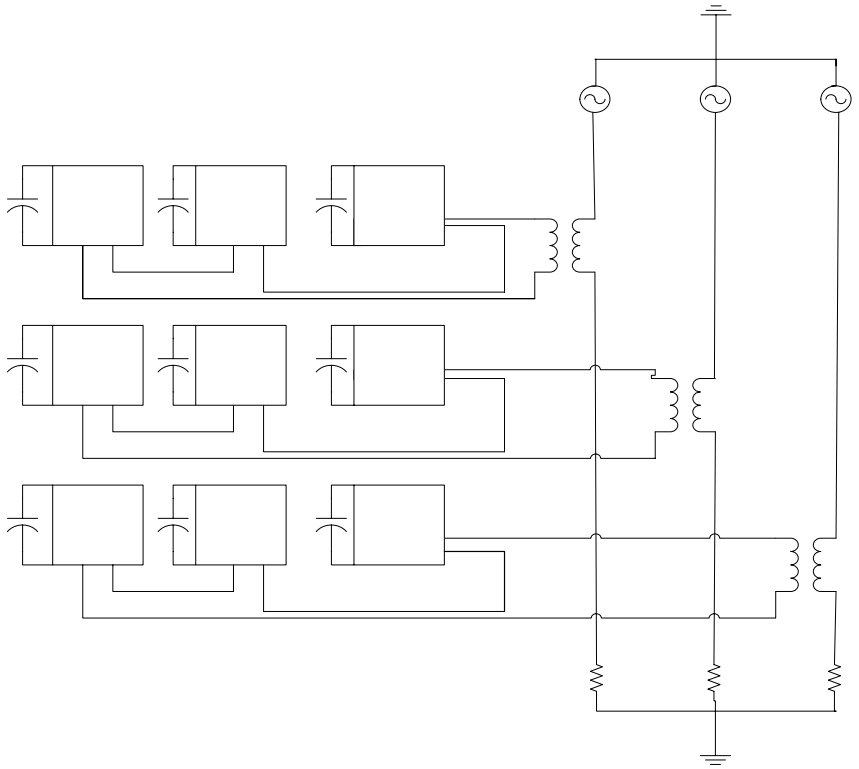


Figure 3.9 - Switching Model of the CMC.

B. Average Model in ABC Coordinates

In order to develop the average model of the H-Bridge Converter, the switching functions are averaged to take into account the switching behavior and the harmonic components for all parameters. The average operator is expressed in Equation 3.6.

$$d = \bar{S}(t) = \frac{1}{T}\int_{t-T}^{t} S(\tau)d\tau \qquad \textbf{Equation 3.6}$$

S(τ) in Equation 3.6 is defined as the switching function of the CMC and d and $\bar{S}(t)$ are defined as the average values of the switching function defined here as the duty

cycles.

The average operator is applied to Equation 3.4, and Equation 3.5, the duty cycle for the switching function S(t) is d_1 from time 0 to T. The behavior of the average switching function is shown in Figure 3.10. From Figure 3.10, it can be stated that the average switching function for time T to 2T is $-d_2$. The green line represents the average switching cycle of a switching function.

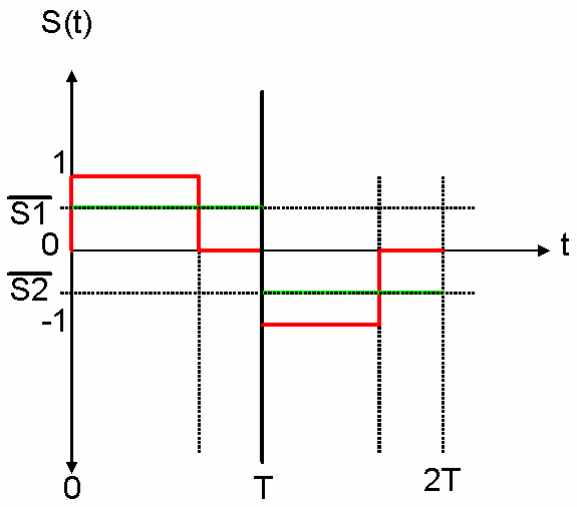


Figure 3.10 - Average Switching Function Over a Switching Cycle.

The next step in the development of the average model of the H-Bridge Converter is to apply the average operator to the voltages and currents of Equation 3.4 and Equation 3.5. The right hand side of both the current and voltage equations consists of two quadratic terms. These quadratic terms are due to the multiplication of two time-dependent terms. Before the average operator can be used on Equation 3.4 and Equation 3.5, something must be done to simplify the quadratic terms on the right-hand side of both equations. To do this, several assumptions need to be made. First, the dc

voltages must be reasonably assumed to be constant during one switching cycle. Second, the output currents must be reasonably assumed to be constant during one switching cycle. These assumptions are valid for two reasons. First, the dc-link capacitors are relatively large for high power applications such as the SSSC; therefore, their voltages do not change very much over a switching period. Second, the switching frequencies of the high power semiconductor devices used in the SSSC are significantly higher than the fundamental frequencies of the power system. For example, the switching frequency of the CMC is in the range of 500 Hz to 3 kHz; whereas, the fundamental switching frequency of the power system is in the range of 50 Hz to 60 Hz.

If the average operator is applied to Equation 3.4, the average voltage equation becomes:

$$\bar{v} = \frac{1}{T}\int_{t-T}^{t} S(\tau)d\tau * E = d * E \qquad \textbf{Equation 3.7}$$

If the average operator is applied to the current Equation 3.5 the result is as follows:

$$\bar{i_E} = d * i_o \qquad \textbf{Equation 3.8}$$

For a 2N+1-level CMC, where N is the number of H-Bridge converters per phase, the average output voltage of the converter is the summation of the average output voltage of each N H-Bridge converters as illustrated in Equation 3.7. The converter's output current is the same as the line current of the power system because the SSSC is connected in

series with the transmission line. Since the SSSC only injects voltage into the systems, the converter's output current is equal to the line current.

The average model in abc coordinates for the CMC-Based SSSC is shown in Figure 3.11. The ESR of the high-power dc capacitors is neglected in the average model because it is relatively small compared to the impedance of the dc capacitors.

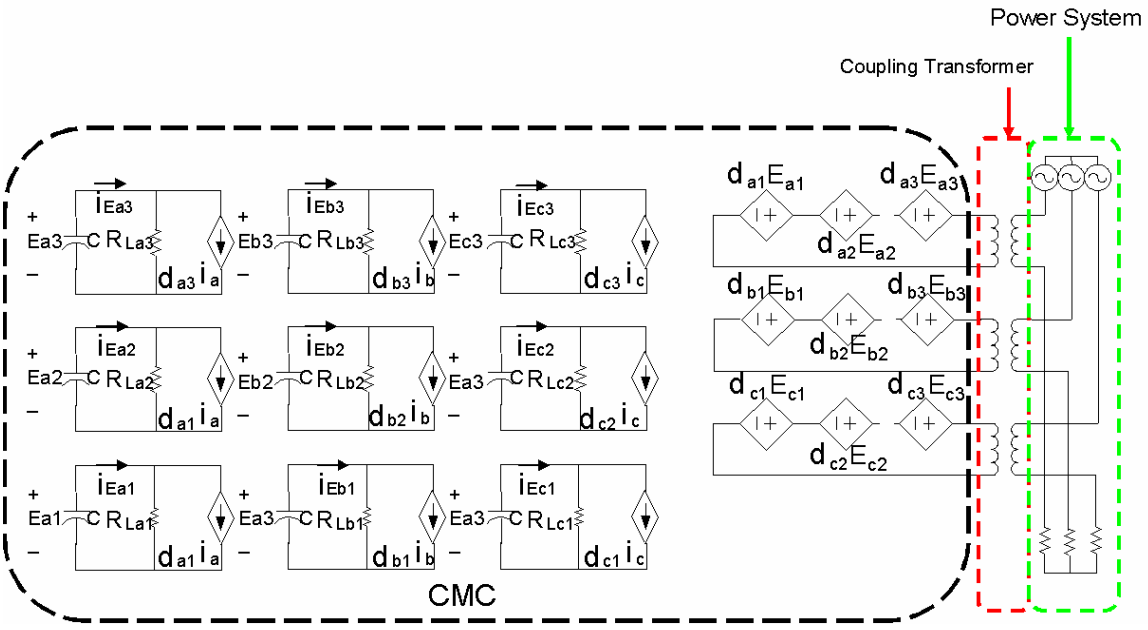


Figure 3.11 - Average Model of CMC-Based SSSC in ABC Coordinates

The average model shown in Figure 3.11 is still very complicated to be used in the SSSC control design process. In order to simplify this model several assumptions need to be made based on the definition of the average operator. These assumptions are:

1. All dc voltage sources are assumed to be regulated; therefore, there will little to no unbalances in these sources. In other words, the dc sources are assumed to be constant.
2. Internal losses for high power converters are usually small; therefore, the losses in

each H-Bridge converter are assumed to be identical.

3. If the capacitor charge balance technique is applied to the dc capacitors then all of the duty cycles in each phase are assumed to be identical.

Based on these assumptions the average model of the SSSC in abc coordinates can be further simplified and shown in Figure 3.12.

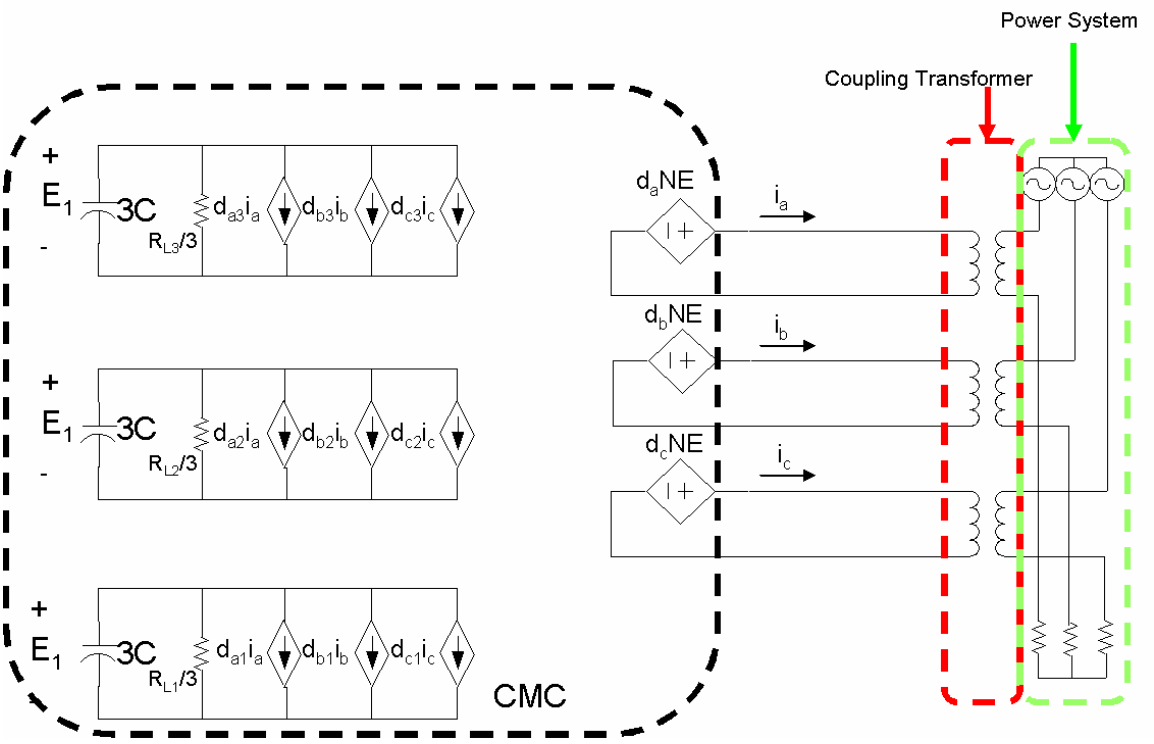


Figure 3.12 - Simplified Average Model of a CMC-Based SSSC in ABC Coordinates.

The average model shown in Figure 3.12 can be further simplified by taking into consideration the coupling transformer. The coupling transformer shown above can be replaced by the transformer equivalent circuit shown if Figure 3.13.

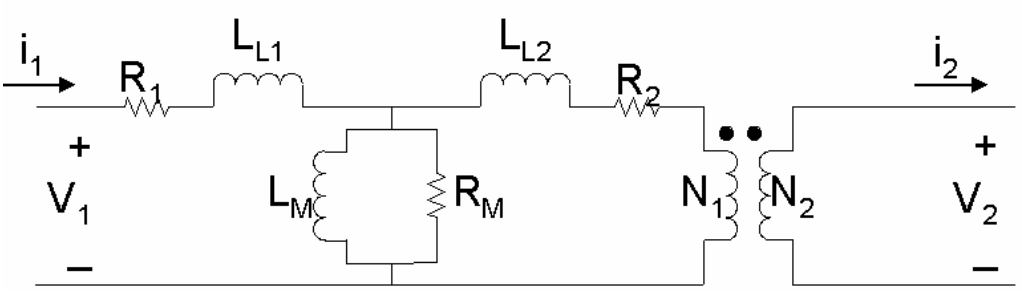


Figure 3.13 - Equivalent Circuit for a Transformer.

If the transformer is replaced by its equivalent circuit, several additional assumptions can be made.

1. Since the SSSC maximum current determined is Chapter 2 is 1250 Amps, the winding resistance R_M can be ignored.
2. Assume that the magnetic core is ideal; therefore, L_M can also be ignored.
3. Assume that the turns ratio of the transformer is 1:1.
4. $R_{Total} = R_1 + R_2$.
5. $L_{Total} = L_1 + L_2$

If the above assumptions are true the equivalent circuit for the transformer is drastically simplified and is shown in Figure 3.14.

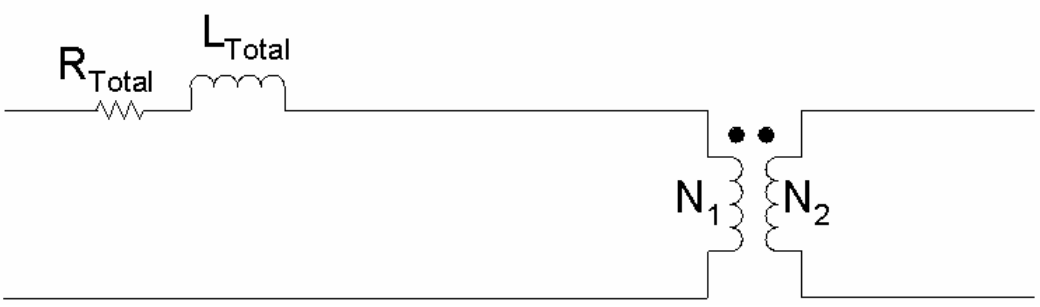


Figure 3.14 - Simplified Transformer Equivalent Circuit.

If the simplified transformer equivalent circuit is placed in the average model for the CMC-Based SSSC, a further simplified average model for the SSSC is shown in Figure 3.15. The final average model of the SSSC in DQ0 coordinates is shown in Figure 3.16. In Figure 3.16, the transformer is removed due to the transformer turns ratio of 1:1 and the power system's sources and loads are transferred from the secondary side of the transformer to the primary side of the transformer via the turns ratio.

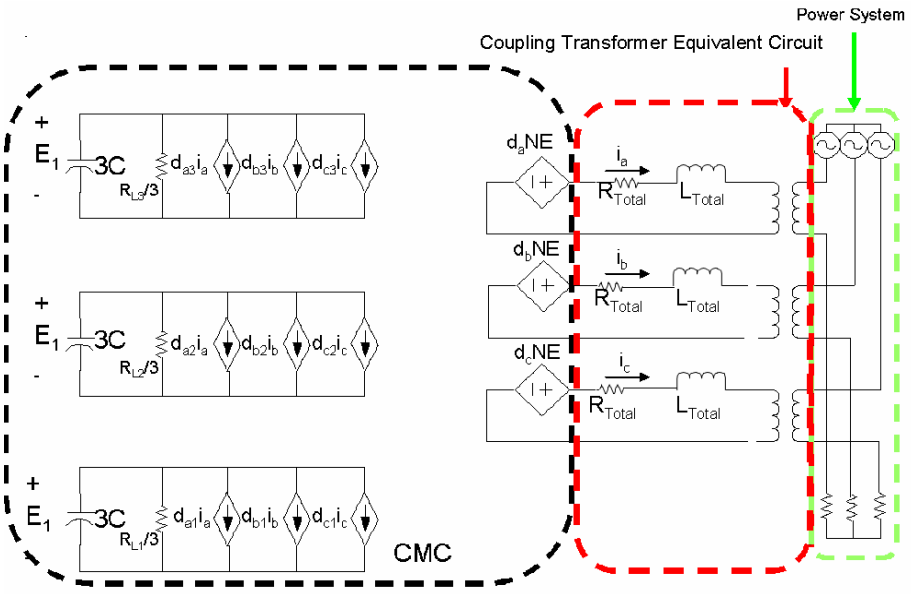


Figure 3.15 - Simplified Average Model for the CMC-Based SSSC.

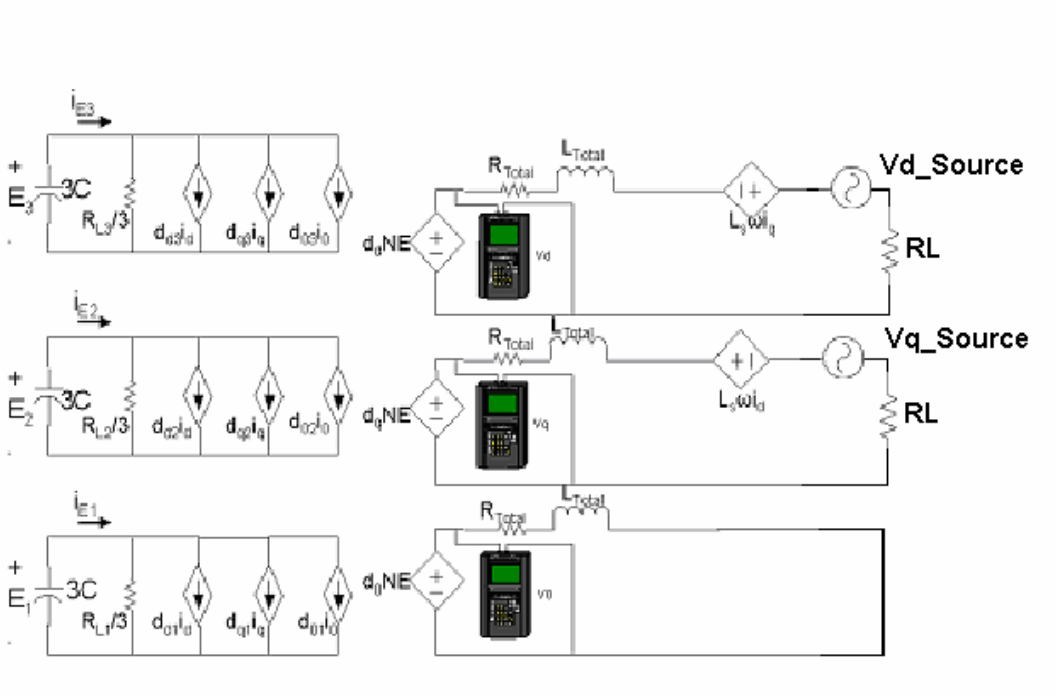


Figure 3.16 – Final Simplified Average Model for the CMC-Based SSSC in DQO Coordinates.

Using Equation 3.7 and Equation 3.8 the small signal model for the SSSC System is shown in Figure 3.17.

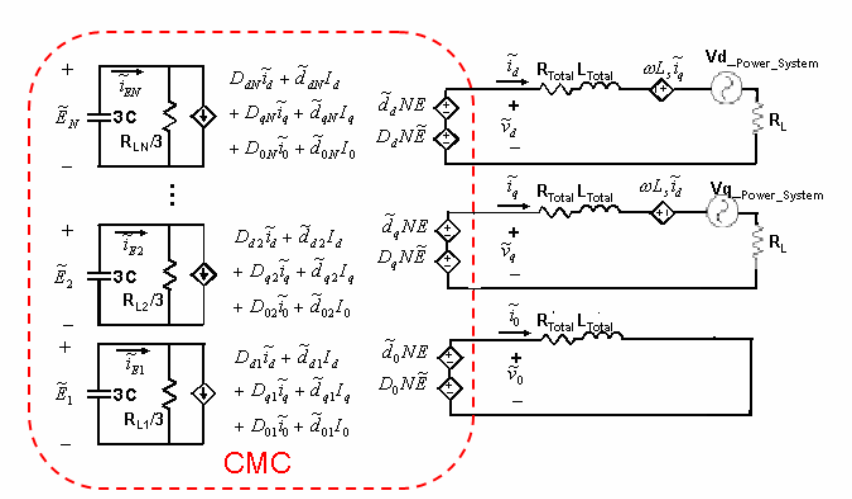


Figure 3.17 – Small-Signal Model of a CMC-Based SSSC in DQ0 Coordinates.

C. Development of the Average Model in DQO Coordinates

According to the decoupling control scheme proposed in [I1], the control variables in DQ0 can be derived from the differential equations for the voltage and current that are represented in Figure 3.16.

The three-phase output-current differential equation matrix for the CMC is:

$$\frac{d\overrightarrow{i_{abc}}}{dt} = \frac{E * N * \overrightarrow{d_{abc}}}{L_{Total}} - \frac{V_{eq}}{L_{Total}} - \frac{R_{Total}}{L_{Total}} * \overrightarrow{i_{abc}} \qquad \textbf{Equation 3.9}$$

The three-phase dc-link voltage differential equation matrix for the CMC is:

$$\frac{dE}{dt} = -\frac{3 * E}{R_{Lj}} - \frac{1}{3 * C} * \overrightarrow{d_{abcj}}^{T} * \overrightarrow{i_{abc}},\ j = 1...N \qquad \textbf{Equation 3.10}$$

Where: $\overrightarrow{i_{abc}} = \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix}, \overrightarrow{d_{abc}} = \begin{bmatrix} d_{aj} \\ d_{bj} \\ d_{cj} \end{bmatrix}$ and N is the number of H-Bridge converters per phase.

To transform the variables in the abc coordinate system to the DQ0 coordinate system, Equation 3.9 and Equation 3.10 are multiplied by the Park's Transformation Matrix shown in Equation 3.11. The SSSC designed in this thesis only supplies reactive power to the network and not real power, the decision was made to align the voltage in the DQ0 frame with the Q axis because the Q axis is responsible for the reactive

components of the SSSC. Possibilities for energy storage for the SSSC will be discussed in this thesis but actual simulation results will not be covered. In this thesis, the Park's Transformation Matrix is defined as follows:

$$\overrightarrow{T_{dq0/abc}} = \sqrt{\frac{2}{3}} * \begin{bmatrix} -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix} \qquad \textbf{Equation 3.11}$$

Where: $\theta = \int_0^t \omega(\tau) d\tau + \theta(0),$ and ω(τ) is the angular velocity

As a result, the average output-current differential equation matrix in DQ0 coordinates for the CMC-Based SSSC is expressed as follows:

$$\frac{d}{dt}\begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} = \frac{N * E}{L_{Total}} * \begin{bmatrix} d_d \\ d_q \\ d_0 \end{bmatrix} - \frac{1}{L_{Total}} * \begin{bmatrix} V_{d\_Power\_System} \\ V_{q\_Power\_System} \\ V_{0\_Power\_System} \end{bmatrix} - \begin{bmatrix} \frac{R_{Total}}{L_{Total}} & -\omega & 0 \\ \omega & \frac{R_{Total}}{L_{Total}} & 0 \\ 0 & 0 & \frac{R_{Total}}{L_{Total}} \end{bmatrix} * \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \qquad \textbf{Equation 3.12}$$

The differential equation matrix in the DQ0 coordinates for the dc-link voltage is as follows:

$$\frac{dE}{dt} = -\frac{3 * E}{R_{Lj} * C} - \frac{1}{3 * C} * \begin{bmatrix} d_{dj} & d_{qj} & d_{0j} \end{bmatrix} * \begin{bmatrix} i_d \\ i_q \\ i_0 \end{bmatrix} \qquad \textbf{Equation 3.13}$$

3.3 Open-Loop Transfer Function Derivation

Using Equation 3.9, and Equation 3.10, there are four possible open-loop control transfer functions that can be derived. They are as follows:

I. Control-to-Output-Voltage Transfer Function

- $G_{Vdd} = \frac{\tilde{V}_d}{\tilde{d}_d}$ *and* $G_{Vqq} = \frac{\tilde{V}_q}{\tilde{d}_q}$

II. Control-to-Output-Current Transfer Function

- $G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d}$ *and* $G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q}$

III. Control-to-Cross-Coupling-Output-Current Transfer Function

- $G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d}$ *and* $G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q}$

IV. Output-Voltage-to-DC-Bus-Voltage Transfer Function

- $G_{Edq} = \frac{\tilde{E}_j}{\tilde{d}_q}$

A. Control-to-Output-Voltage Transfer Function, G_{idd}

From Equation 3.9, by setting other perturbations to zero, the KVL of the D channel is expressed as:

$$\tilde{d}_d * E * N - \omega * L_{Total} * \tilde{i}_d = \left[R_L + R_{Total} + S * L_{Total}\right] * \tilde{i}_q . \qquad \textbf{Equation 3.14}$$

By applying the KVL to the Q channel, its output current is derived, as follows:

$$\tilde{i}_q = \frac{-\omega * L_{Total}}{\left[R_L + (R_{Total} + S * L_{Total})\right]} \tilde{i}_d . \qquad \textbf{Equation 3.15}$$

Substituting Equation 3.15 into Equation 3.14 yields

$$G_{vdd} = \frac{\tilde{V}_d}{\tilde{d}_d} = \frac{N * E * R_L}{R_L + R_{Total} + S * L_{Total}} . \qquad \textbf{Equation 3.16}$$

From the Small-Signal model shown in Figure 3.17,

$$G_{vqq} = \frac{\tilde{V}_q}{\tilde{d}_q} = \frac{N * E * R_L}{R_L + R_{Total} + S * L_{Total}} . \qquad \textbf{Equation 3.17}$$

B. Control-to-Output-Current Transfer Function, G_{idd}

From Equation 3.9, the output current in the D channel is

$$\tilde{i}_d = \frac{-\left[R_L + R_{Total} + S * L_{Total})\right]}{\omega * L_{Total}} \tilde{i}_q . \qquad \textbf{Equation 3.18}$$

Substituting the D-channel output current Equation 3.18 into Equation 3.9 yields:

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{N * E}{R_L + R_{Total} + S * L_{Total} + \omega^2 * \frac{L_{Total}^{\ 2}}{R_L + R_{Total} + S * L_{Total}}} . \qquad \textbf{Equation 3.19}$$

Likewise, the transfer function G_{iqq} is:

$$G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q} = \frac{N * E}{R_L + R_{Total} + S * L_{Total} + \omega^2 * \frac{L_{Total}^{\ 2}}{R_L + R_{Total} + S * L_{Total}}} \qquad \textbf{Equation 3.20}$$

C. Control-to-Cross-Coupling-Output-Current Transfer Function, G_{idq}

Substituting Equation 3.14, for the D-channel output current into Equation 3.9 yields:

$$G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q} = \frac{N * E}{(R_L + R_{Total} + S * L_{Total}) * \frac{-R_L - R_{Total} - S * L_{Total}}{\omega * L_{Total}} + \omega * L_{Total}} . \qquad \textbf{Equation 3.21}$$

Likewise, the transfer function G_{idd} is:

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{N * E}{(R_L + R_{Total} + S * L_{Total}) * \frac{-R_L - R_{Total} - S * L_{Total}}{\omega * L_{Total}} + \omega * L_{Total}} \qquad \textbf{Equation 3.22}$$

D. Output-Voltage-to-DC-Bus-Voltage Transfer Function, G_{Evd}

Using the DC capacitor circuit shown in Figure 3.17, with perturbations of the D-channel and Q-channel currents, yield:

$$\widetilde{E}_j = -\frac{(D_{dj}\widetilde{i}_d + D_{qj}\widetilde{i}_q)}{3CS},\ j = 1 \ldots N, \qquad \textbf{Equation 3.23}$$

where N is the number of H-bridge converter per phase. Due to the fact that Equation 3.23 contains current information, this equation therefore becomes invalid. The explanation can be found in Chapter 4.

3.4 Summary

This chapter presented the operating principles of the CMC-based SSSC system. The model developed for the CMC-Based SSSC is in both ABC and DQ0 coordinates. Based on practical assumptions, the simplified model of the SSSSC utilizing the CMC was proposed. The key transfer functions, which will be used in Chapter 4 for the SSSC controller design, were derived.

Chapter 4 Closed-Loop Control of Cascaded-Multilevel Converter-Based SSSC

Chapter 4 uses the control strategy proposed in [I1] to control a CMC-Based SSSC. The proposed SSSC model, which was derived in Chapter 3, is used in the design process. Real and reactive power exchanged between the SSSC and the power networks can be controlled independently by decoupling the real and reactive components of the SSSC into D-Channel and Q-Channel components. The injection of reactive voltage into the power grid is only being considered in this thesis; however, real power can also be injected. This thesis mainly focuses on the injection of reactive voltage for power flow control purposes.

4.1 Control Analysis and Design

A three-level CMC-based SSSC is used to design the control of the SSSC. The control of the SSSC is designed in a DQ0 coordinate frame. The modeling accuracy and control performance are verified via computer simulations.

A. Control Law for the CMC-Based SSSC

The proposed SSSC system, as shown in Figure 4.1, is composed of a generic CMC, which is coupled to a power system via coupling reactor and an injection transformer. The coupling transformer is represented by a leakage inductor combined with a series resistor. The series resistor of the coupling transformer is used to represent the internal losses of the transformer. Figure 4.2 illustrates a single-line diagram of the generic CMC-based SSSC system. The power network is modeled as three ideal sinusoidal voltage sources and an equivalent load resistance. In general, the source voltage and the load

depend on the power system's operating condition. For example, during different times of the day, the power system's load will change according to pre-existing load curves. Also, the power system's characteristics will change in the event of a fault.

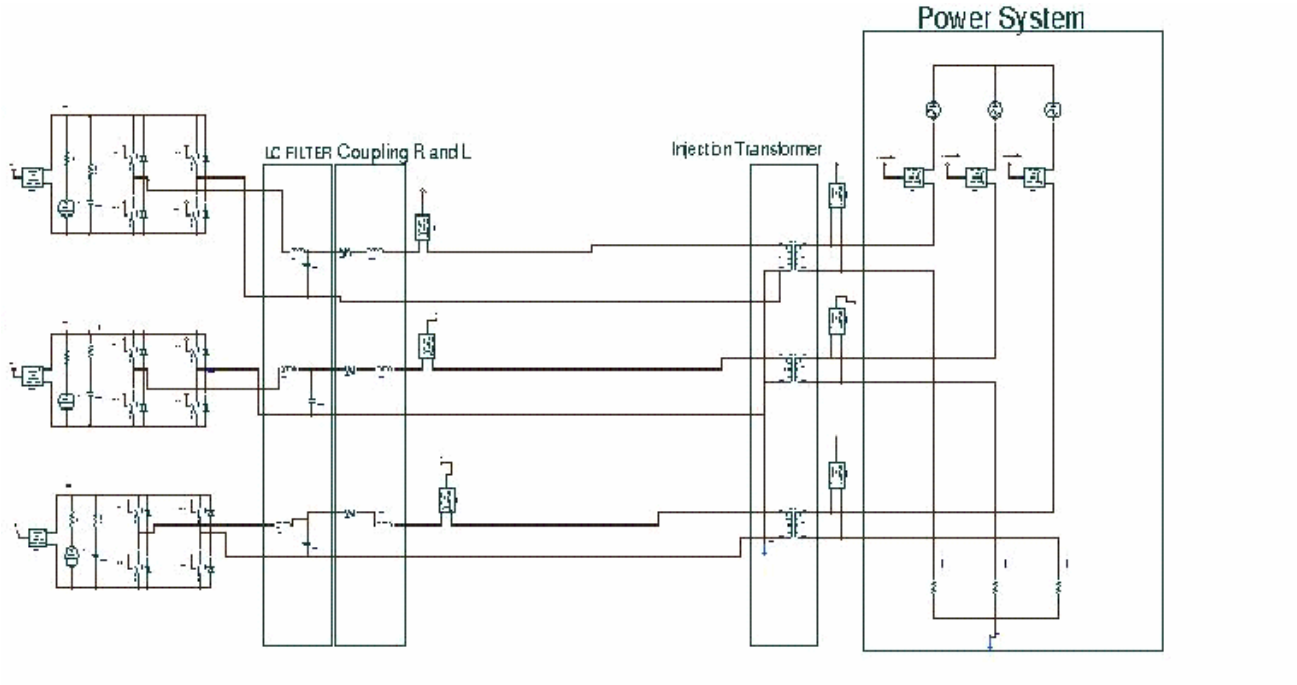


Figure 4.1 - Proposed SSSC System.

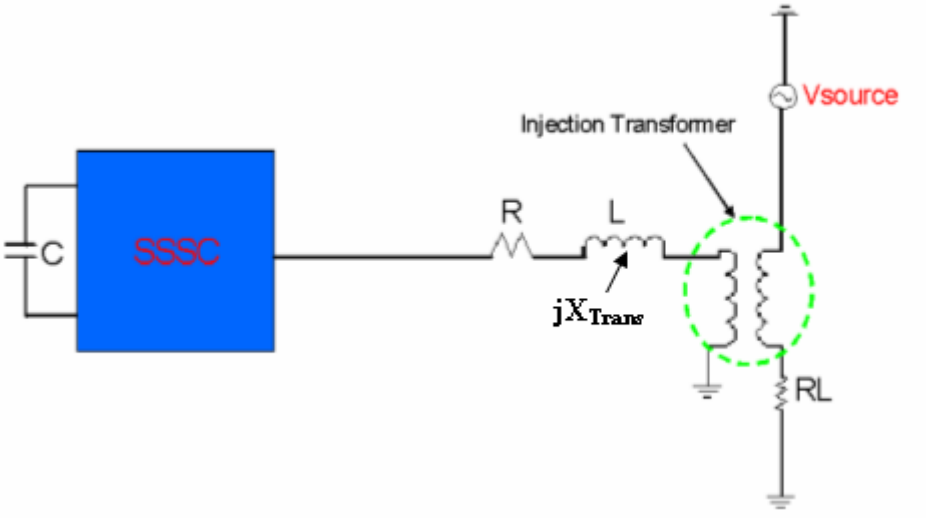


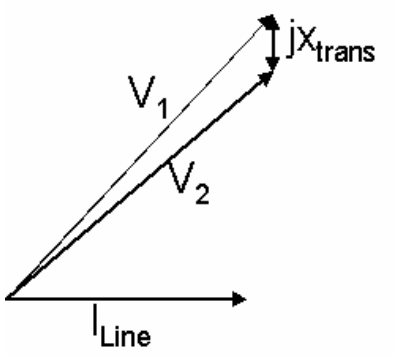
Figure 4.2 - Single-Line Diagram of a Generic SSSC.

The SSSC can operate properly and effectively as long as the following two sets of key electrical parameters are controlled: three-phase output voltage and multiple DC capacitor voltages. The output voltage determines the amount of reactive power exchanged with the power network. A single-line diagram of the SSSC shown in Figure 4.2 is used as an example. At this point, the CMC is assumed to be lossless. The SSSC behaves similar to an adjustable capacitive or inductive series impedance which injects reactive power into the power network. Figure 4.3(a) illustrates a Phasor diagram of the converter when the output voltage of the converter is zero. V_1 represents the source side voltage whereas V_2 represents the load voltage. In other words, the converter is in what is called "stand-by" mode. Figure 4.3(b) illustrates a phasor diagram of the converter output voltage, V_{inj}, and the power system current, I_{Line}, when the SSSC operates in the capacitive mode. If the SSSC is operating in capacitive mode, the injected voltage into the power grid forces the series impedance of the transmission line to increase when the demand for power delivered to the load is lower. In contrast, as shown in Figure 4.3(c), the converter output voltage of the SSSC is controlled in such a manner as to force the series impedance of the transmission line to be lower when the demand for power delivered to the load is higher.

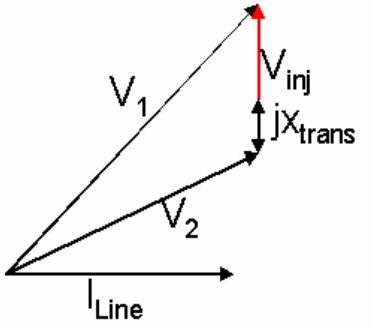
It must be noted that for all practical purposes, the SSSC is not lossless. Only a lossless converter is being considered in this chapter.

There are two key control laws for the cascaded-multilevel VSC used in the SSSC applications. The two key control laws are:

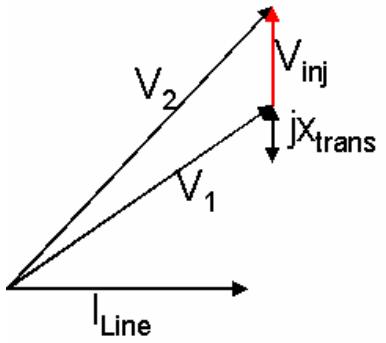
1. The amount of the transferred reactive power (Var, Q) can be controlled by adjusting the magnitude of the converter output voltage.
2. The DC-Link voltage must be regulated in such a way any imbalances in the DC-Link voltage does not affect the overall performance of the converter.



(a)



(b)



(c)

Figure 4.3- Operating phasor diagrams of the lossless three-level converter-based SSSC: (a) standby mode, (b) capacitive mode, and (c) inductive mode.

Figure 4.3(a),(b), and (c) illustrates the Phasor diagrams for the various modes of operation for the SSSC. V_{inj} represents the injected voltage into the power grid, where jx_{trans} represents the leakage inductance of the transformer.

B. Three-Level Cascaded-Based SSSC Control Design

For this thesis, the controller design is carried out for a three-phase three-level CMC-Based SSSC. With only one H-bridge converter per phase, a voltage-balancing problem does not exist in this case. The purpose of starting with the three-level converter is to verify the correctness and accuracy of the output currents and single DC capacitor voltage regulation.

This particular SSSC system, as shown in Figure 4.1, is formed by a three-level cascaded converter that is coupled to a power system by the coupling inductor and coupling transformer at the injection point. There are two possible control strategies that could be used to control the SSSC. First, a direct voltage control strategy could be used to control the SSSC. The basic behavior of this control strategy is to monitor the system voltage. If a capacitive mode command is given to the controller, then the converter will inject the required voltage into the power grid. The same is true for the inductive mode of operation. Figure 4.4 shows an open-loop block diagram for the direct voltage control scheme. The D-Channel is used to control the reactive voltage V_d, and the Q-Channel is used to control the DC Bus voltage (E).

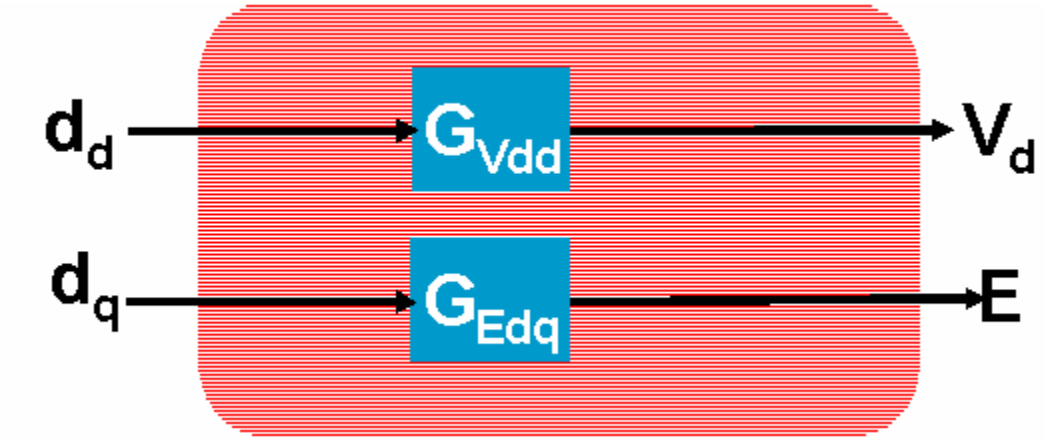


Figure 4.4 - Open-Loop Block Diagram for the Direct Voltage Control Scheme.

The second control strategy that could be used to control the SSSC uses a more indirect method for control purposes. This method can only be used if an energy storage element is added for "real" voltage injection. Since the CMC-Based converter is connected in series with the transmission line, the power system current and the CMC-Based converter current must be the same. The power system current is determined by the power grid requirements at the time; therefore, there is no longer any degree of freedom to directly control the converter current (i.e. the power system current). However, due to Ohm's Law shown in Equation 4.1, there is a way to indirectly control the power system current.

$$V = X * I \qquad \textbf{Equation 4.1}$$

The voltage injected by the SSSC behaves like a series impedance; therefore, the impedance value (X) shown in Equation 4.1 is changed by the converter. The power system voltage (V) is fixed, so for every value of resistance there is a corresponding current to make the voltage constant. The desired range of compensation for the converter is +/- 10% - 15% of the power system current. If a command is given to the

controller for maximum capacitor compensation there is a specific power system current that represents this condition. The controller can thereby adjust the duty cycle of the converter so that the converter injects the appropriate amount of voltage corresponding to the correct series impedance in order to satisfy Ohm's law. For example, during normal operation the power system current is 1250 A r.m.s. For 10% capacitive compensation, the power system current would decrease by a value of 125 A r.m.s. The command to the converter would be +1125 A, the converter would then adjust the duty cycle of the converter until the error or the difference between the actual power system current and the current value of this current is approximately equal to zero. The amount of voltage injected by the converter would be the equivalent of the correct value of the series impedance added to the power grid by the converter. This control scheme is similar to that for the STATCOM control scheme outlined in [I1]. Figure 4.5 shows an open-loop block diagram for the indirect current control of the SSSC.

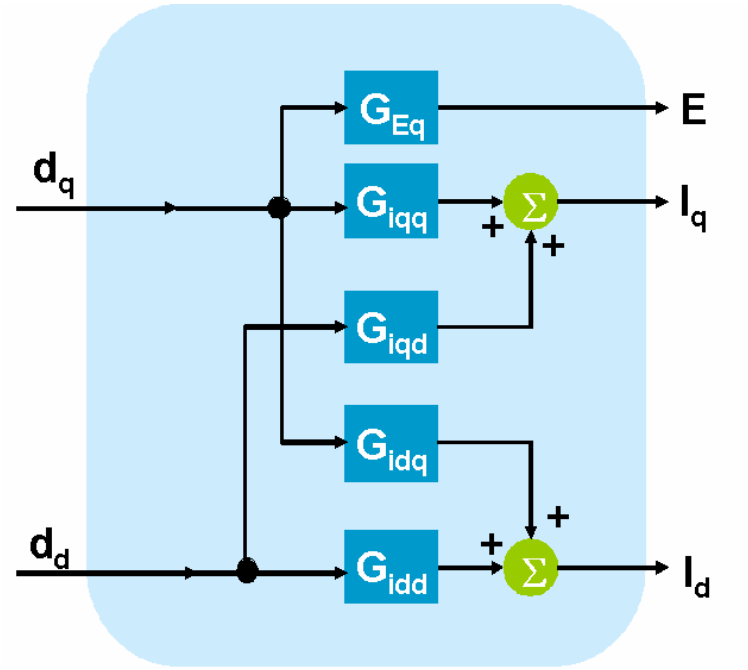


Figure 4.5 - Open-Loop Block Diagram for the Indirect Current Control Scheme.

The schematic of the completed power stage of the three-level CMC-Based SSSC is shown in Figure 4.1. Each phase of the cascaded converter consists of an H-bridge converter, which can generate three levels of output voltages, i.e., –E, 0 and +E.

Based on the proposed HBBB discussed in Chapter 2, the electrical parameters of the cascaded three-level CMC and the power network are designed are shown in Table 4.1.

TABLE 4.1 - SPECIFICATION OF THE STUDIED SYSTEM.

Power System Specification	
Source Voltage	13.8 kV
Line Current	1250 A r.m,s
Voltage Source Converter Rating	
Main Switch	4.5kV/4.0kA ETO
DC Bus Voltage	2500 V
DC Bus Capacitor	9.6 mF/phase
Converter Output Current	1250 A r.m.s
Switching Frequency	1.5 kHz
Coupling Transformer Impedance	300.1 μH
Coupling Transformer Loss Resistance	10.0 mΩ
Reactance Compensating Range	10% - 15% of Line Impedance

4.2 SSSC Modeling Verification

The SSSC model verification is broken down into four distinct sections. First, the DC steady-state solution for the SSSC is determined. The DC steady-state solution provides the initial conditions used for simulation. Second, the open-loop transfer functions derived in Chapter 3 must be verified. Third, once the system transfer functions have been verified, the overall functionality of the SSSC must be verified according to the SSSC average model. Finally, the average model results must be compared to the switching model results; therefore, the modeling cannot be assumed correct until the switching model is verified. The next three sections of this chapter will give the detailed step-by-step procedure used to verify the SSSC modeling.

C. DC Steady State Solution

The circuit shown in Figure 4.6 was used to derive the DC steady-state equations/

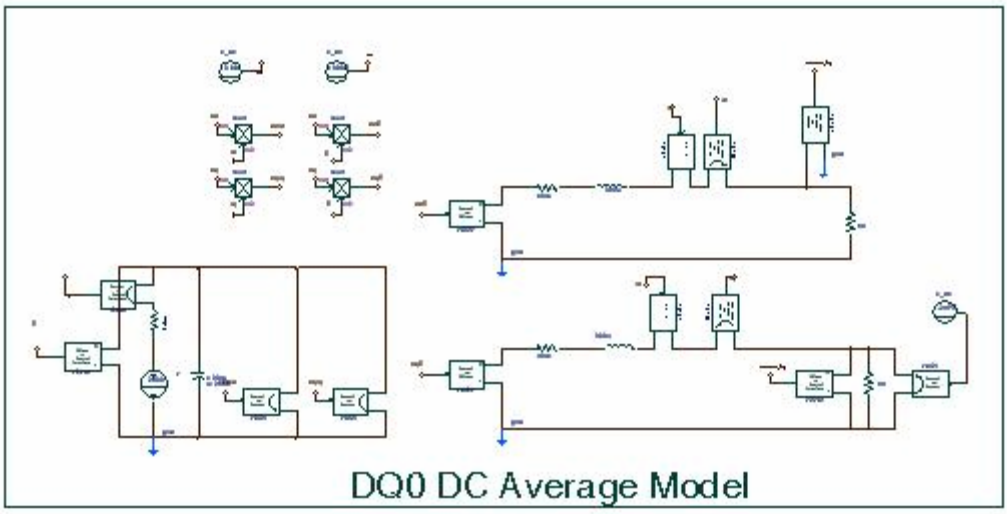


Figure 4.6 – DC Simulation Schematic

The DC steady-state equations are as follows:

$$d_d * i_d = -d_q * i_q \qquad \textbf{Equation 4.2}$$

$$d_d * E = (R_T + R_L) * i_d - \omega * L_T * i_q \qquad \textbf{Equation 4.3}$$

$$d_q * E = R_T * i_q + \omega * L_T * i_d + V_q \qquad \textbf{Equation 4.4}$$

$$i_d = \frac{V_{d\_ref}}{R_L} \qquad \textbf{Equation 4.5}$$

$$i_q = -I_q - \frac{V_q}{R_L} \qquad \textbf{Equation 4.6}$$

I_q is represents the power grid current transformed into the dq0 frame. Since the current is aligned with the q-axis, V_q is equal to zero and V_{d_ref} is equal to the value of the command. I_{abc} and V_{d_ref} are calculated as follows:

$$I_{abc} = \frac{V_{Power}}{R_L} = \frac{13.8kV}{11.0} = 1254.0Amps \qquad \textbf{Equation 4.7}$$

$$V_{d\_ref} = \%compensation * V_{Power} * \sqrt{\frac{3}{2}} = 2440V \qquad \textbf{Equation 4.8}$$

The next step in the derivation of the DC steady-state solution is to transform the current represented via Equation 4.7 into its Q-Axis current represented by Equation 4.9.

$$I_q = \sqrt{2.0} * \frac{V_{Power}}{R_L} * \sqrt{3/2} = 2173Amps \qquad \textbf{Equation 4.9}$$

The DC solution for the SSSC was derived by systematically solving Equations 4.2 – 4.6 in MathCAD. Table 4.2 compares the analytical DC steady-state solution to the simulated DC steady state solution for accuracy.

TABLE 4.2 - COMPARISON BETWEEN CALCULATED AND SIMULATED DC STEADY-STATE SOLUTIONS.

Parameter	Calculated Value	Simulated Value
E	2500	2500
D_d	0.98	0.98
D_q	0.09	0.09
i_d	200	200.04
i_q	-2189	-2189.3
v_d	2200	2200.4
v_q	179.274	179.23

Figure 4.7 shows the Saber simulation waveforms for the DC steady-state solution.

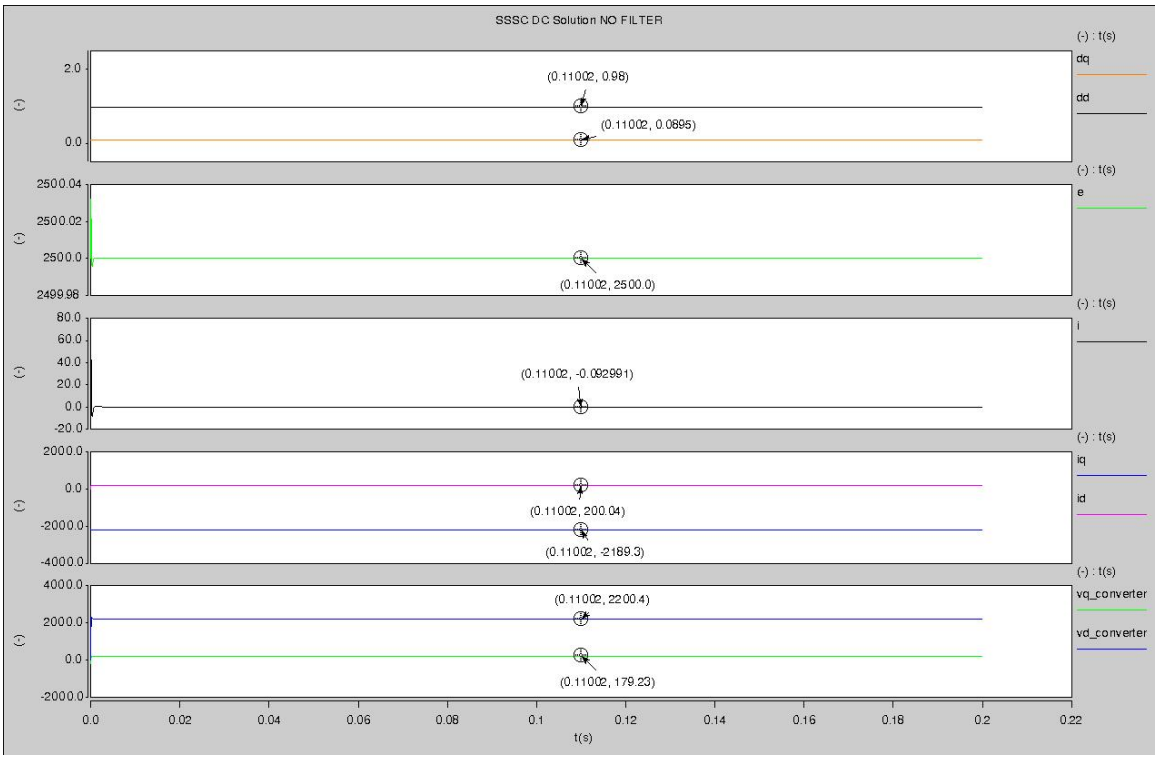


Figure 4.7 – Simulated DC Steady-State Solution

D. System Transfer Function Verification

The first step for the SSSC modeling verification process is to determine if the transfer function derived for the SSSC's average model is correct. This is done by constructing an AC DQ0 equivalent circuit for the SSSC with all steady-state parameters set. Figure 4.8 shows the MatLab simulation schematic used to simulate the AC DQ0 equivalent circuit of the SSSC. Table 4.1 contains the set parameters used for the AC DQ0 equivalent circuit. In the beginning, the DC Bus is assumed to be constant for the purposes of deriving the open-loop transfer functions in terms of voltage and current for the D-Channel and for the Q-Channel After careful analysis of the system transfer functions it was determined that the assumption that the DC Bus is constant is not valid. If the DC Bus is considered to be a constant the impact that the state variable E has on the

open-loop transfer functions at low frequencies is negated. To observe the effect that the state variable E has on the open-loop transfer functions two MabLab Simulink files were created. Figure 4.8 shows represents E as a constant. Figure 4.9 represents E as a function of dd, dq, id, and iq.

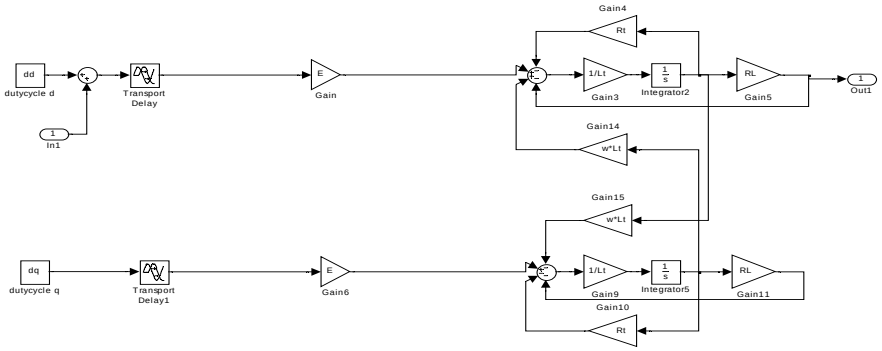


Figure 4.8- MatLab AC Equivalent Circuit for the DQ0 Average Model E Constant.

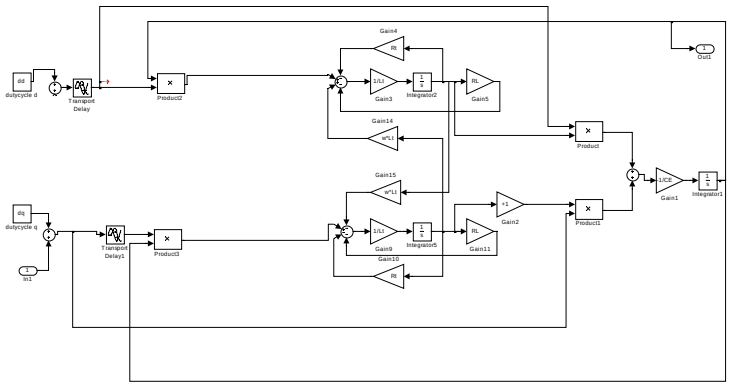


Figure 4.9 - MatLab Equivalent Circuit for the DQ0 Average Model E Not Constant

Figure 4.10 shows the MatLab simulation waveform for the control-to-output-voltage transfer function G_{vdd} with E assumed to be a constant. Figure 4.11 shows the Matlab simulation waveform for the same transfer function with E not constant. A close examination of Figure 4.11 shows that there is a dip (apparent right-half plane pole) at low frequencies not shown in Figure 4.10. Therefore, in order for an accurate controller to be designed for the SSSC E must remain as a state variable.

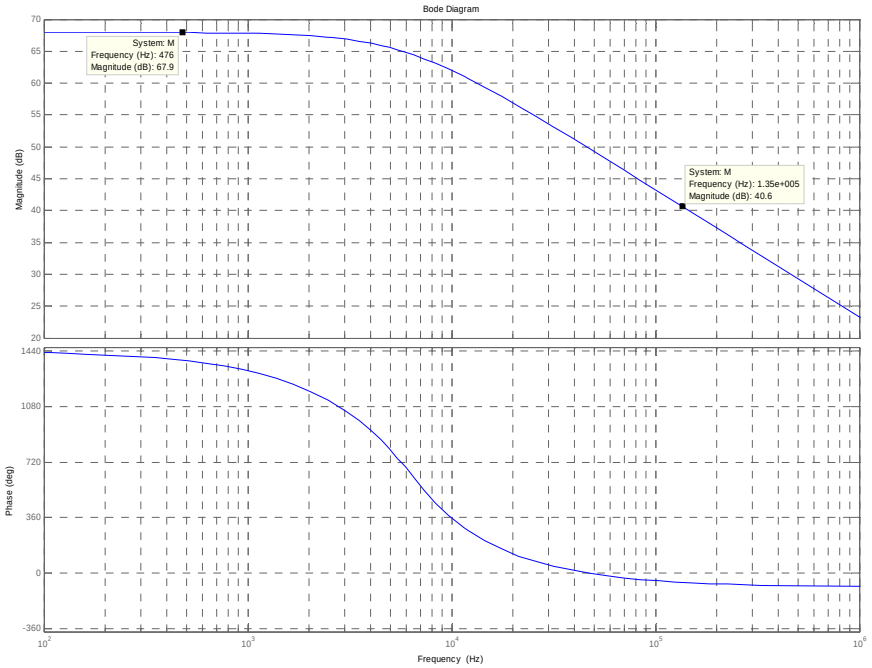


Figure 4.10 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{vdd}.E Constant.

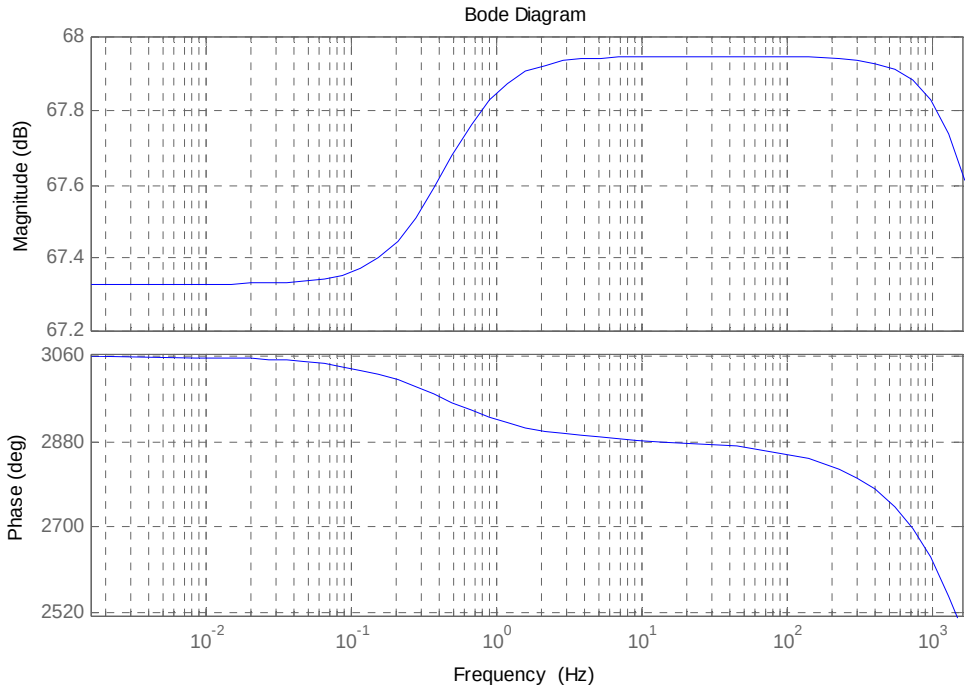


Figure 4.11 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{vdd} E Not Constant

Once the steady-state parameters for the SSSC are set, a small AC perturbation is added to each D-Channel and Q-Channel component separately. An AC sweep is performed on each channel and the effect of the perturbation is observed. The effects of transport delay will be discussed in a later section of this chapter.

D1. D-Channel Transfer Function

There are three transfer functions that correspond to perturbations in the D-Channel. Each transfer function will be described by its characteristic equation as well as its MatLab open-loop bode plot. The open-loop bode plots were obtained using the MatLab Simulink circuit shown in Figure 4.9

Control-to-Output-Voltage Transfer Function G_{vdd}

$$G_{vdd} = \frac{\tilde{V}_d}{\tilde{d}_d} = \frac{N * E * R_L}{R_L + R_{Total} + S * L_{Total}} \qquad \textbf{Equation 4.10}$$

Figure 4.12 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Voltage Transfer Function G_{vdd}.

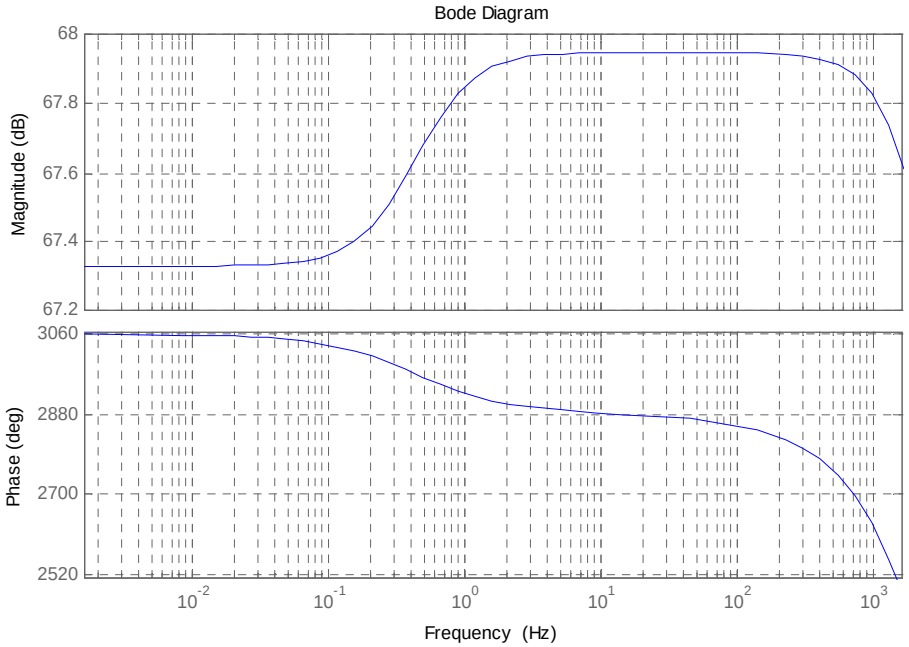


Figure 4.12 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{vdd}.

Control-to-Output-Current Transfer Function G_{idd}

$$G_{idd} = \frac{\tilde{i}_d}{\tilde{d}_d} = \frac{N * E}{R_L + R_{Total} + S * L_{Total} + \omega^2 * \frac{L_{Total}^{\ 2}}{R_L + R_{Total} + S * L_{Total}}} \qquad \textbf{Equation 4.11}$$

Figure 4.13 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Current Transfer Function $G_{idd.}$

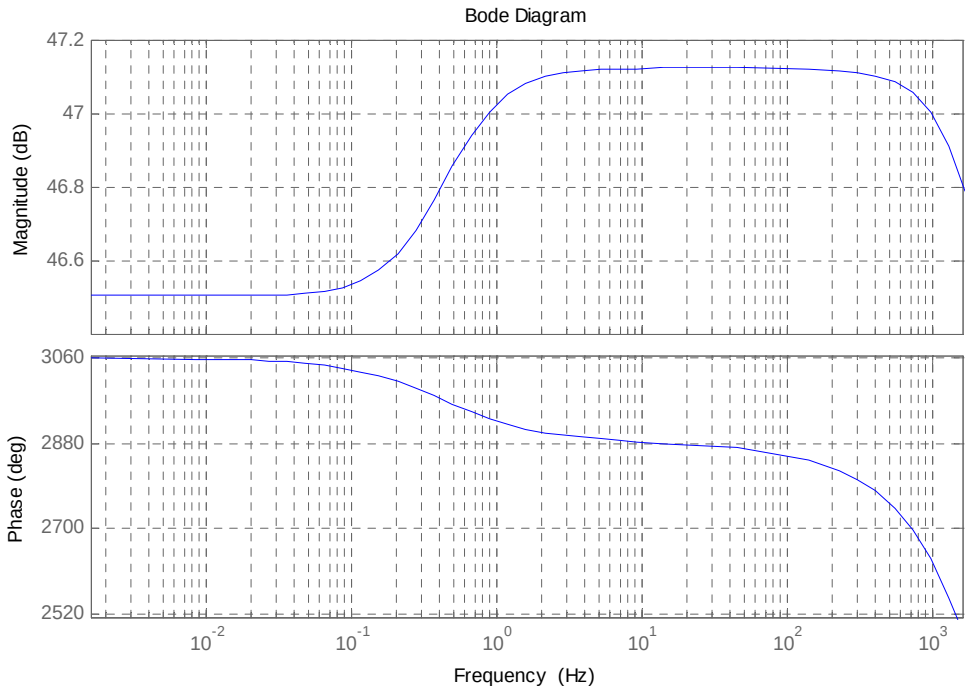


Figure 4.13 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function $G_{idd.}$

Control-to-Cross-Coupling-Output-Current Transfer Function G_{idq}

$$G_{idq} = \frac{\tilde{i}_d}{\tilde{d}_q} = \frac{N * E}{(R_L + R_{Total} + S * L_{Total}) * \dfrac{-R_L - R_{Total} - S * L_{Total}}{\omega * L_{Total}} + \omega * L_{Total}} \quad \textbf{Equation 4.12}$$

Figure 4.14 shows the MatLab simulation plot for the gain and phase of the Control-to-Cross-Coupling-Output-Current Transfer Function G_{idq}.

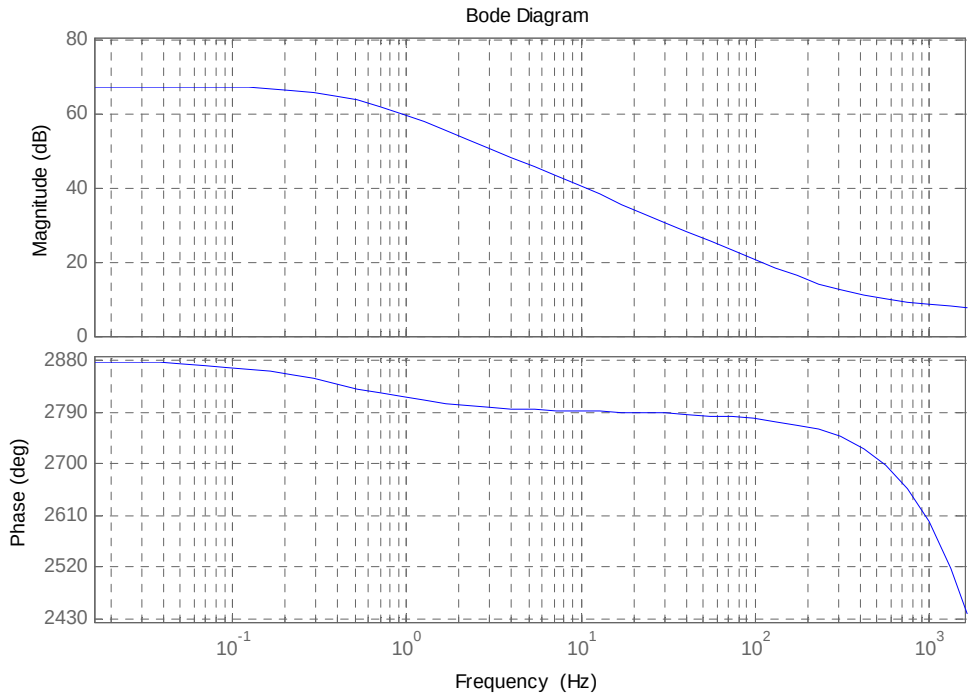


Figure 4.14 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{idq}.

D2. Q-Channel Transfer Function

There are four transfer functions that correspond to perturbations in the Q-Channel. Each transfer function is defined with its characteristic equation, MathCAD bode plot, and MatLab simulation waveform.

Control-to-Output-Voltage Transfer Function G_{vqq}

$$G_{vqq} = \frac{\tilde{V}_q}{\tilde{d}_q} = \frac{N * E * R_L}{R_L + R_{Total} + S * L_{Total}} \qquad \textbf{Equation 4.13}$$

Figure 4.15 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Voltage Transfer Function G_{vqq}.

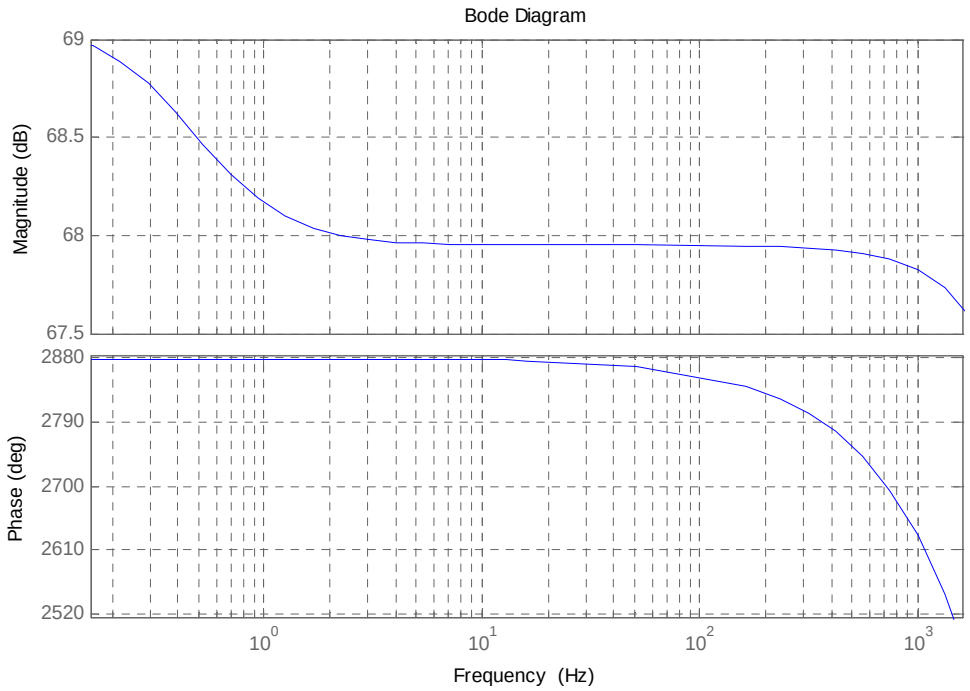


Figure 4.15 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{vqq}.

Control-to-Output-Current Transfer Function G_{iqq}

$$G_{iqq} = \frac{\tilde{i}_q}{\tilde{d}_q} = \frac{N * E}{R_L + R_{Total} + S * L_{Total} + \omega^2 * \frac{L_{Total}^{\ 2}}{R_L + R_{Total} + S * L_{Total}}} \qquad \textbf{Equation 4.14}$$

Figure 4.16 shows the MatLab simulation plot for the gain and the phase of the Control-to-Output-Current Transfer Function $G_{iqq.}$

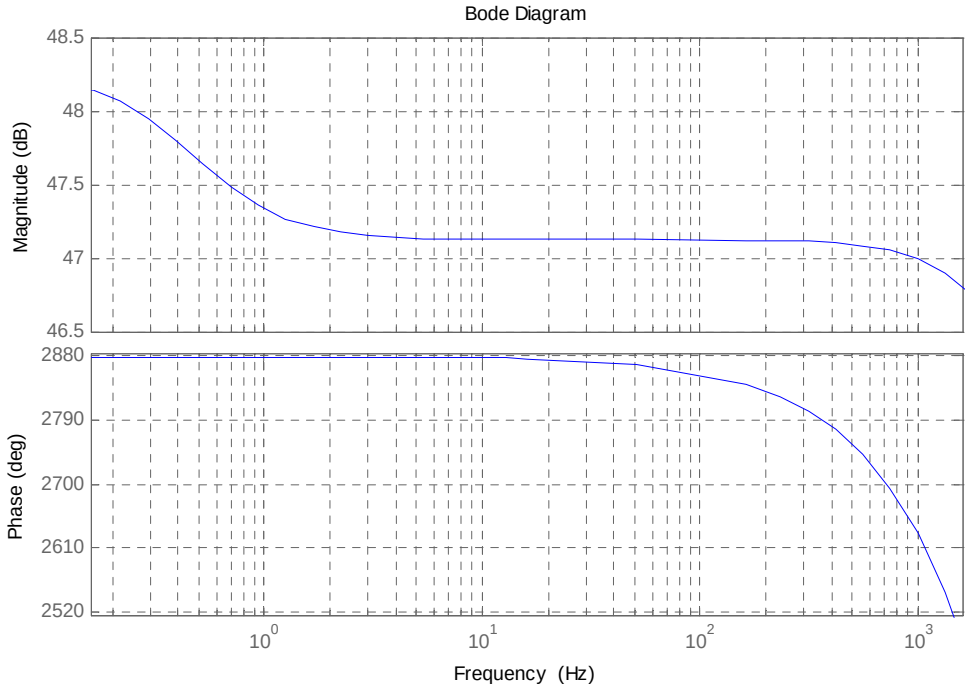


Figure 4.16 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function $G_{iqq.}$

Control-to-Cross-Coupling-Output-Current Transfer Function G_{iqd}

$$G_{iqd} = \frac{\tilde{i}_q}{\tilde{d}_d} = \frac{N * E}{(R_L + R_{Total} + S * L_{Total}) * \dfrac{-R_L - R_{Total} - S * L_{Total}}{\omega * L_{Total}} + \omega * L_{Total}} \qquad \textbf{Equation 4.15}$$

Figure 4.17 shows the MatLab simulation plot for the gain and the phase of the Control-to-Cross-Coupling-Output-Current Transfer Function G_{iqd}.

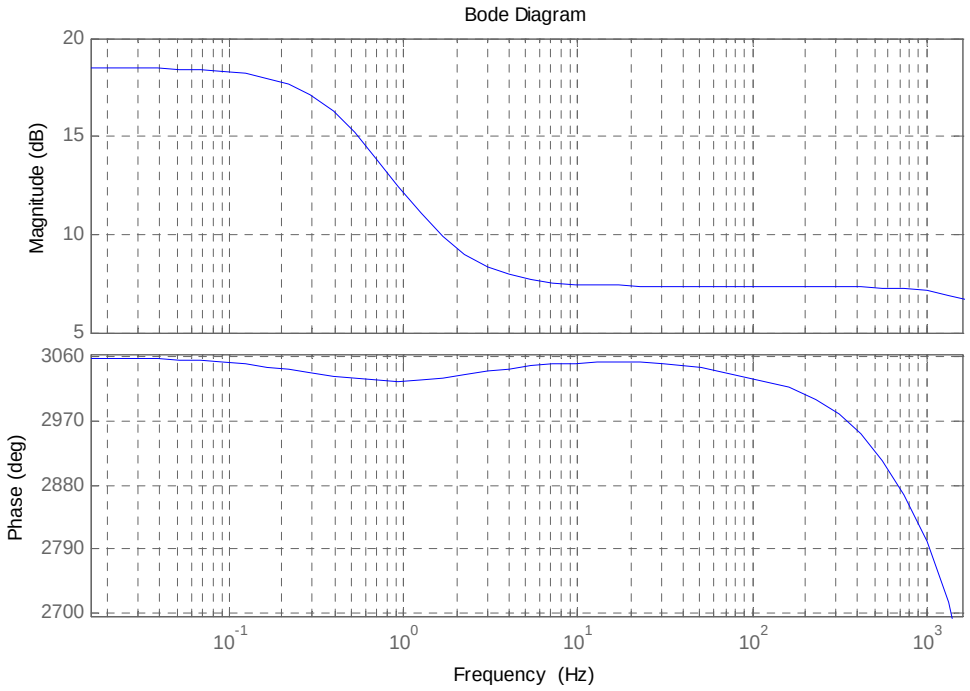


Figure 4.17 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{iqd}.

Control-to-DC-Bus-Voltage G_{Eq}

$$\widetilde{E}_j = -\frac{(D_{dj}\widetilde{i}_d + D_{qj}\widetilde{i}_q)}{3CS}, \quad j = 1 \ldots N \qquad \textbf{Equation 4.16}$$

The control-to-DC-Bus-Voltage transfer function is difficult to derive. The equation that can be derived from the AC Equivalent Circuit model is in terms of current. Since, the current is a fixed parameter dictated by the power grid, there is no degree of freedom to control current. As a result, a second MatLab simulation schematic is needed to determine the G_{Eq} transfer function. Since the current is aligned with the Q-Axis, the Q-Axis is used to control the "real" power and therefore control the DC Bus voltage. Figure 4.18 illustrates the control-to-DC-Bus-Voltage transfer function obtained from MatLab.

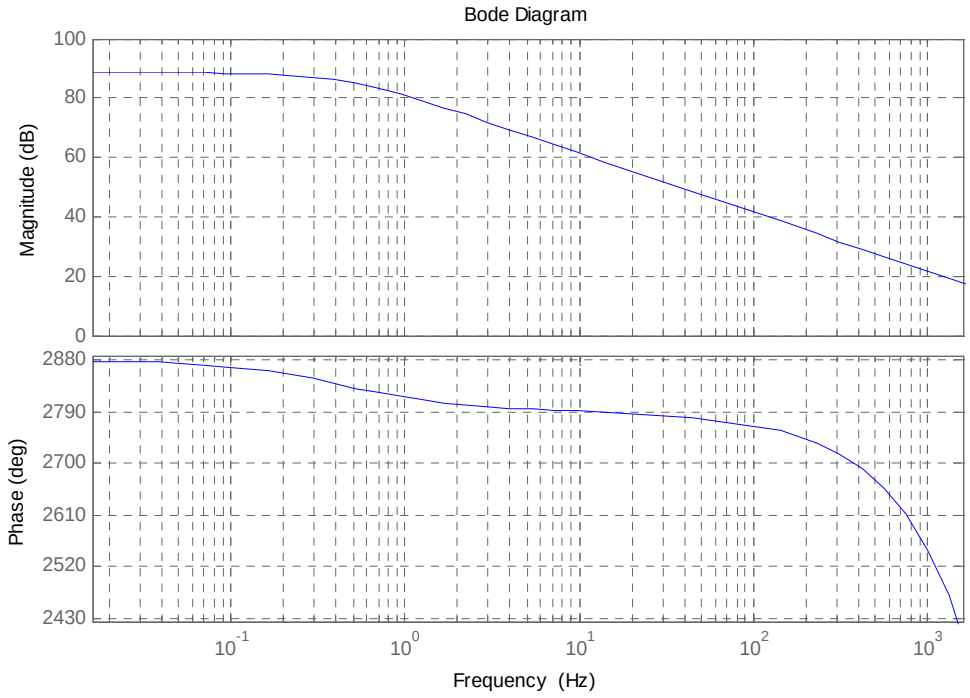


Figure 4.18 - MatLab Simulation Waveform for the Control-To-DC-Bus-Voltage Transfer Function.

E. Summary of the Potential Effects of Various Delays on the Transfer Functions

There are three important delays embedded in both the power stage and the controller which must be considered: the switching, the calculation and the transducer delays. The following sections give a brief summary of the various types of delays.

E1. Switching Delay

The switching frequency of most high-power semiconductor devices can range from the kilohertz range to a few hertz range. The high switching frequencies are due to the recent advances in high-power semiconductor technology. The switching delay is, therefore, the most important factor of concern in the high-power electronic control design. In order to explain how to determine the switching delay for the CMC, an H-bridge converter phase-leg, shown in Figure 4.19, is used as an example. An H-bridge converter consists of two phase-legs. Each phase-leg consists of two complementary switches. The relationship of the total output voltage and individual phase-leg voltage is simply expressed as follows:

$$V_{LR}(t) = V_{LN}(t) - V_{RN}(t) \qquad \textbf{Equation 4.17}$$

Each phase-leg is assumed to switch at 1/T Hertz. The left side of the phase-leg is controlled by the positive duty cycle; whereas, the right phase-leg is controlled by the negative duty cycle. The negative duty cycle is out of phase with the positive duty cycle. The duty cycle is updated every half-cycle. In other words, each phase leg responds to the duty cycle every half-cycle and has a half-cycle delay time.. Since the output of the CMC is the summation of *N* individual H-bridge converters, its switching delay is:

$$T_{d\_sw}(t) = \frac{1}{2 \cdot N \cdot f_s}$$ **Equation 4.18**

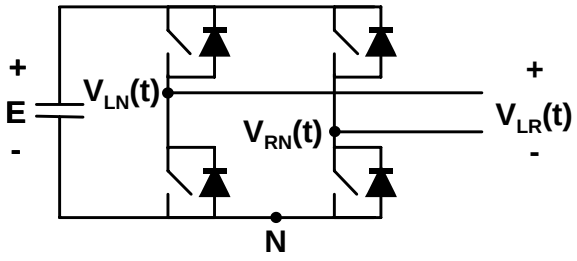


Figure 4.19 - Two phase legs forming an H-bridge converter.

E2. Calculation Delay

The calculation delay is a function of the processor used in the controller. Due to its high-speed arithmetic units, the recent floating-point DSP is widely employed in real-time control applications. Since the SSSC designed in this thesis has not been built, the calculation delay has no purpose in the SSSC simulations.

E3. Transducer Delay

In general, the signals used for the feedback control loops for a digital controller are measured using voltage and current transducers. The measured signals are sent to analog-to-digital converters (ADC's) to be transformed into digital signals to be used by the processor. The transducer delay is also known as the sampling delay, which is indirectly proportional to the sampling frequency of the ADC. Since the actual controller for the SSSC has not been built and no signal is physically being measured, the transducer delay plays no role in the SSSC simulations.

E4. Total Delay

The total delay is the summation of these three previously discussed delays. Due to the fact that the calculation delay and the transducer delay play no role in the SSSC simulations and the fact that the switching delay in most applications is dominant, the total delay time can be approximated by the switching delay, as shown in Equation 4.19:

$$T_d = T_{d\_sw} \qquad \textbf{Equation 4.19}$$

The switching delay mainly affects the phase delay of the loop gain, and can be modeled in Laplace form as follows:

$$\tau(S) = e^{-T_d S} \qquad \textbf{Equation 4.20}$$

The open-loop transfer function plotted above take the switching delay into account.

F. Feedback-Controller Design

Figure 4.30 shows the complete proposed control block diagram for the three-level cascaded-based SSSC system. The primary objective of the D-Channel feedback controller is to regulate the D-Channel voltage to follow the command as fast as possible.

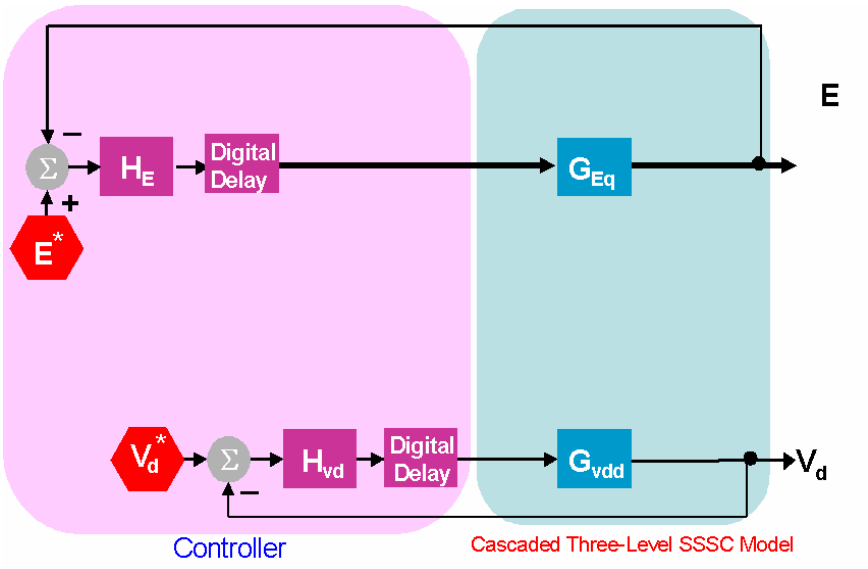


Figure 4.20 - Control block diagram.

In the D-Channel, there is only one main control loop: the external output voltage loop (V_d-loop). The reference for the V_d-loop is the voltage command that is generated from either the power system control center or an automatic controller. Finally, the output of the voltage regulator is the D-Channel duty cycle.

In the Q-channel, the three DC capacitor voltages are averaged and compared to the reference, which is fixed at 2500 V. The error is compensated by the voltage compensator, H_E. The output of this compensator is the Q-Channel duty cycle.

The control process starts with the external D-Channel control loop. First, the DC-Bus is assumed to be regulated. In other words, a constant DC source is used as the DC Bus instead of a capacitor. Once this is done, the D-Channel compensator is designed based on the open-loop voltage transfer function in order to meet the gain and phase margin requirements of the control.

F1. Design of Voltage Compensator, H_{vd}

The Open-Loop transfer function for the voltage shown in Figure 4.12 is used to design the D-Channel compensator. Due to the Nyquist's criteria, the designed crossover frequency of the voltage loop should not be higher than half of the effective switching frequency, which equals twice the individual phase-leg switching frequency or 3 kHz. First, an average model of the SSSC is used to verify the controller design and to check the final gain and phase margin of the compensator in order to insure its stability. An average model is capable of predicting the behavior of its switching model from DC up to half of the effective switching frequency. The next step in the design process for the closed-loop controller is to determine the type of compensator to use for the voltage loop.

F2. Compensator Selection

There are various types of compensators that can be used for the closed-loop controller design of the SSSC. One type of controller is known as the standard pole zero compensator. The standard pole zero compensator places poles and zeros at desired frequencies in order to achieve stability. There is also another type of compensator known as the lag compensator or the proportional-plus-integral (PI). The pole zero compensator is the best candidate for the closed-loop control of the SSSC based on its robustness, controllability, and performance.

With the compensator, the closed-loop transfer function of the D-Channel voltage can be expressed as follows:

$$T_{vd}(S) = H_{vd}(S) \cdot G_{vdd}(S) \qquad \textbf{Equation 4.21}$$

The standard pole zero controller is optimized using the MatLab SISO tool. The SISO tool in MatLab allows the user to import the open-loop transfer function into MatLab. Poles and zeros can be added and adjusted by the user until the desired crossover frequency, gain margin, and phase margin of the closed-loop system is obtained. The SISO tool also tells the user if the compensator designed is stable or not. The general rules used for the compensators are as follows:

1. The Gain Margin of the closed-loop system should be at least 3dB.
2. The Phase Margin of the closed-loop system should be larger than 30°.
3. The crossover frequency should be as high as possible but must satisfy the Nyquist criteria.

The desired crossover is selected to be as high as possible, but must be less than 1.5 kHz, which is half of the effective switching frequency.

Equation 4.22 expresses the characteristic equation of the designed controller.

$$H_{vd}(s) = 0.00251 * \frac{1.0}{(1.0 + 0.00072 * s)} \qquad \textbf{Equation 4.22}$$

TABLE 4.3 - GAIN MARGIN, PHASE MARGIN, AND CROSSOVER FREQUENCY OF THE DESIGNED D-CHANNEL CONTROLLER

Gain Margin	Phase Margin	Crossover Frequency
3.23 dB	59.5°	277 Hz

Figure 4.21 shows the Gain and Phase plot of the D-Channel compensator designed using the SISO tool in MatLab.

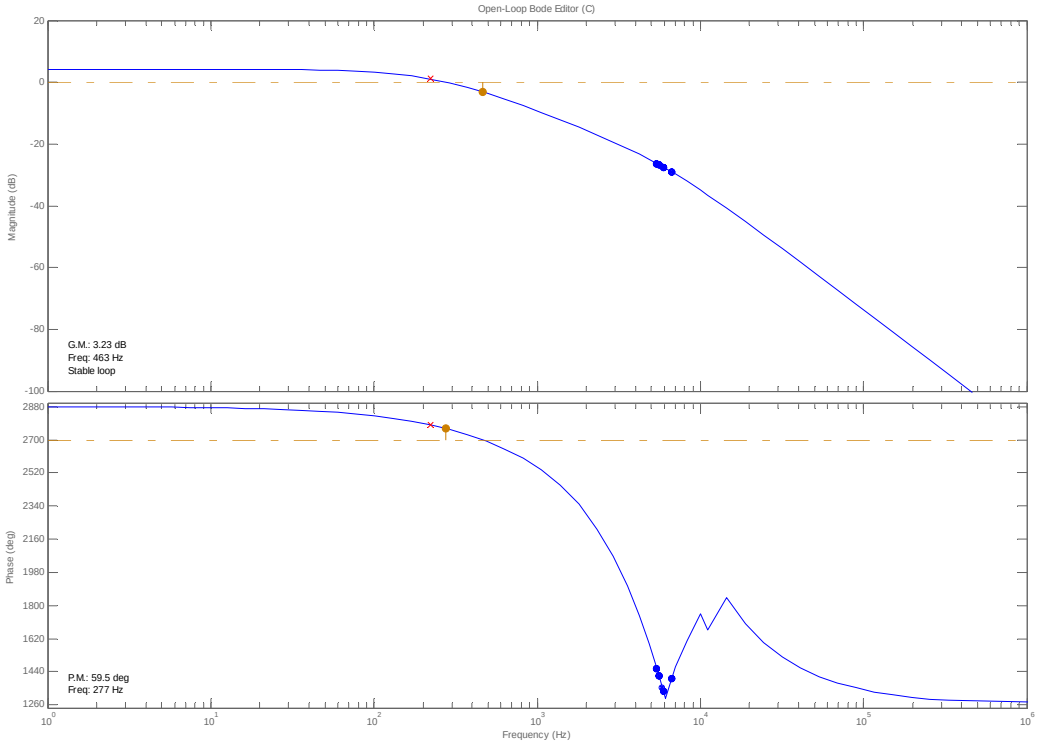


Figure 4.21 – Closed-Loop Bode Plot for the H_{vd} Compensator.

F3. Design of DC Capacitor Voltage Compensator, H_{Eq}

With the D-Channel voltage loop closed, the next step is to design the Q-Channel voltage compensator to control the DC-Bus voltage.

The Bode plot obtained from MatLab of transfer function $G_{Edq}(S)$ is shown in Figure 4.18. A compensator is needed to regulate the DC-Bus voltage around its operating point. It is customary to design the crossover frequency for the DC-Bus loop low. In other words, the response of the compensator to regulate the DC-Bus need not be as fast (the crossover frequency is low) as the compensator for the D-Channel voltage loop. Equation 4.23 expresses the characteristic equation of the designed controller.

$$H_{vd}(s) = 0.000642 * \frac{1.0}{(1.0 + 0.00072 * s)} \qquad \textbf{Equation 4.23}$$

Table 4.4 shows the Gain Margin, Phase Margin, and Crossover Frequency of the designed controller.

TABLE 4.4 - GAIN MARGIN, PHASE MARGIN, AND CROSSOVER FREQUENCY OF THE DESIGNED Q-CHANNEL CONTROLLER

Gain Margin	Phase Margin	Crossover Frequency
24.6 dB	79.6°	29.8 Hz

Figure 4.22 shows the Gain and Phase plot of the D-Channel compensator designed using the SISO tool in MatLab.

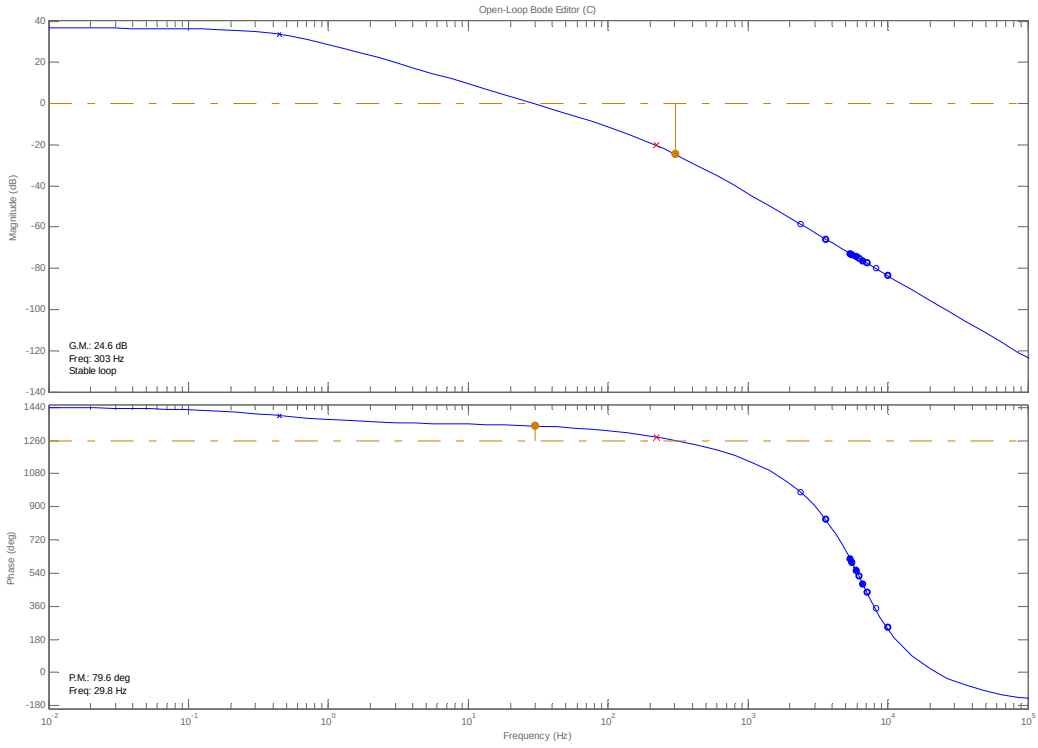


Figure 4.22 – Closed-Loop Bode Plot for the H_{Eq} Compensator.

4.3 SSSC Average Model Verification

In order to verify if the compensators designed for the SSSC work effectively an average model is used. The SSSC average model is used to verify the operation of the SSSC and will be used to verify the stability of the closed-loop control compensators.

G. Simulation Results of the Average Model with the Designed Control

To verify the stability and performance of the proposed control parameters, the average model of the three-level CMC-Based SSSC with the designed feedback control is simulated. At the voltage injection point, the power exchange between the SSSC and the power network is monitored. The following is a list of modes of operation for the SSSC:

1. standby mode is the mode in which the SSSC generates zero real and reactive power (P = 0 Watt and Q = 0 Var);
2. inductive mode is the mode in which the SSSC absorbs the reactive power from the power network. The injected voltage lags the line current by 90 degrees (at full inductive mode, P = 0 Watt and Q = -3.1 MVar);
3. capacitive mode is the mode in which the SSSC injects the reactive power into the power network. The injected voltage leads the line current by 90 degrees (at full capacitive mode, P = 0 Watt and Q = +3.1 MVar).

In this simulation, the SSSC is commanded to operate in the following three modes:

1. at time 0 to 99 ms, the SSSC operates in full capacitive mode, V_d = 2440 V;
2. at time 100ms to 149 ms, the SSSC operates in the full inductive mode, V_d = -2440 V; and,

3. at time 149 ms to 200 ms, the SSSC operates in standby mode, V_d = 100 V. NOTE: A small amount of voltage is needed to generate enough current in the converter to maintain the charge on the DC-Bus.

The command V_d at the full load is calculated from the full-load output voltage in the ABC coordinate. The relationship between the AC parameters in the DQ0 and ABC coordinates yields the following:

$$v_{d\_command}(t) = \sqrt{\frac{3}{2}} \cdot v_{A\_pk}(t), \qquad \textbf{Equation 4.24}$$

where $v_{A\text{-}pk}(t)$ is the peak of the output-phase voltage.

Figure 4.23 shows the simulation schematic of the average model used to simulate the behavior of the SSSC. The simulation results show that the SSSC compensators are stable throughout the entire operating range.. The D-channel output current closely follows the V_d command. The average DC capacitor voltage is also regulated within an acceptable range. During each transition period, the details of the simulation results are discussed and verified.

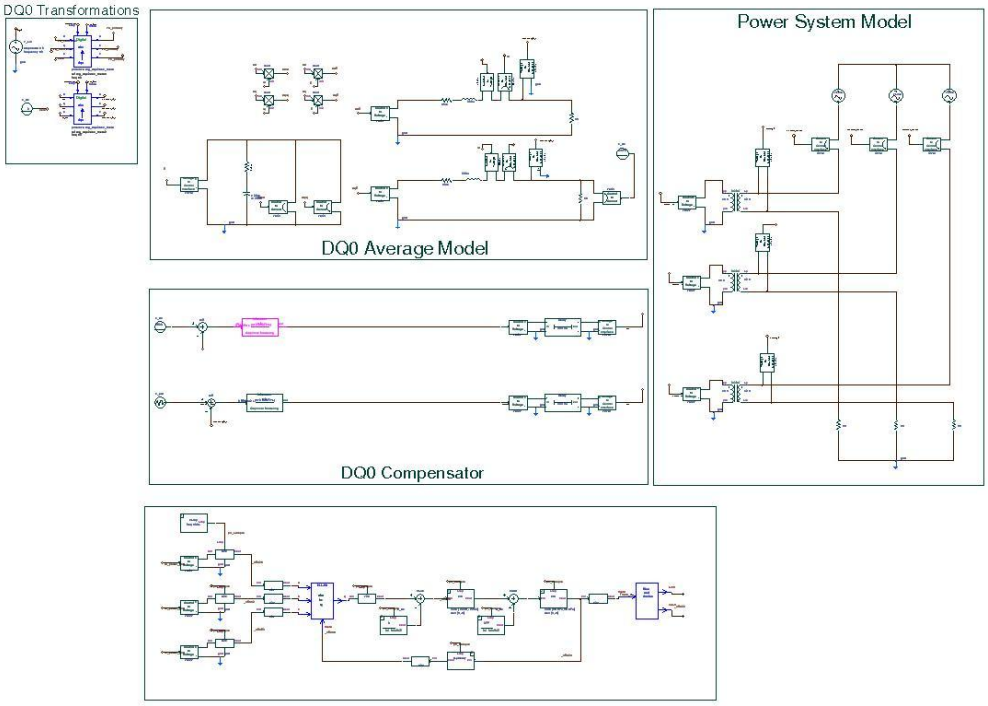


Figure 4.23 - Simulation Schematic of the SSSC Average Model.

The simulation results for the average model to follow makes one basic assumption. It is assumed that the DC-Bus is initially charged to 2500V.

G1. Mode 1 (Capacitive Mode)

Initially, the SSSC begins its mode of operation in capacitive mode. At t = 100 ms, the SSSC is commanded to abruptly change its operation mode from full capacitive mode to full inductive mode by adjusting the V_d command from 2440 to -2440. Due to the assigned current direction during the modeling procedure, the output voltage lags the I_{Line} by 90° in the capacitive mode and leads the I_{Line} by 90° in the inductive mode. In mode 2, the simulation result verifies that phase-A output voltage V_{a_inject}, lags I_{Line} by 90°. Figure 4.24 is used to illustrate capacitive mode of operation.

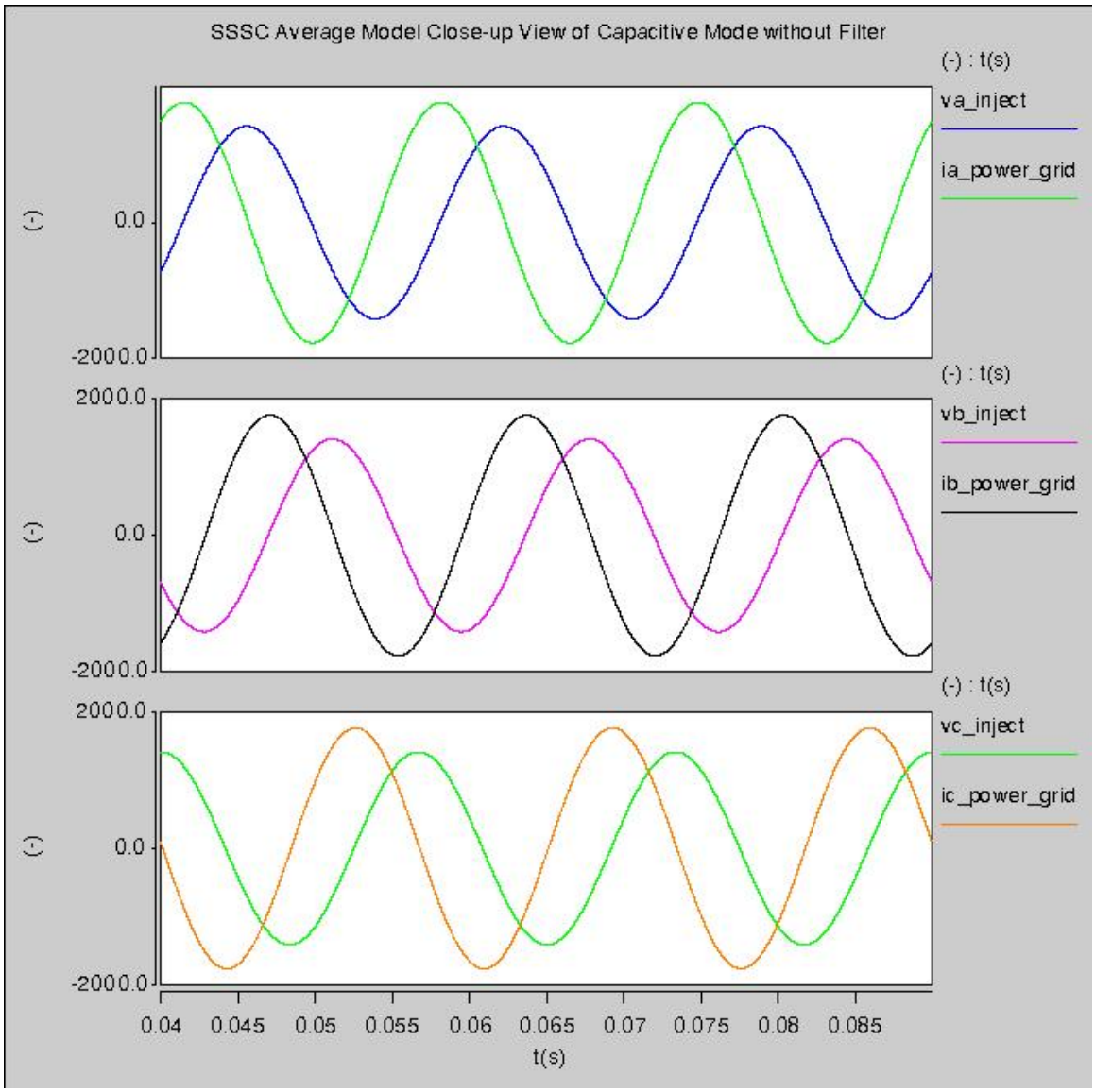


Figure 4.24 - SSSC Average Model Simulation in Capacitive Mode.

G2. Transition 2: from Mode 1 to Mode 2

As stated above, at t = 100 ms, the SSSC is commanded from full capacitive mode to full inductive mode of operation. Figure 4.25 shows the saber simulation waveform for Transition 2. This transition is the worst-case operation.

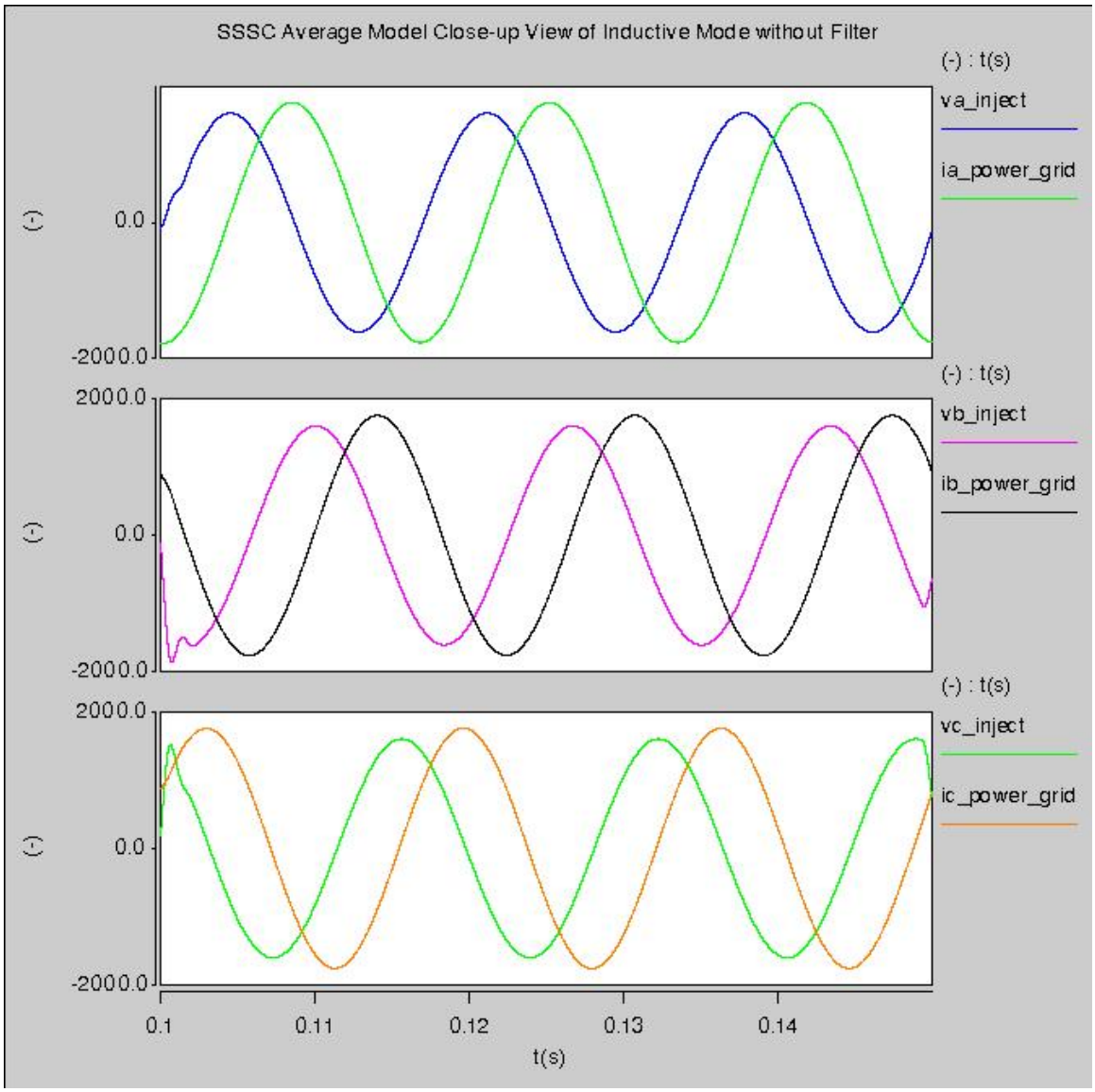


Figure 4.25 - SSSC Average Model Simulation in Inductive Mode.

G3. Transition 3: from Mode 2 to Mode 3

At t = 150 ms, the SSSC is commanded from full inductive mode of operation to standby mode of operation. During the standby mode of operation only a small amount of voltage is injected into the power system. This voltage can be neglected. The primary reason that there is a small amount of voltage injected into the power grid is due to the fact that the V_d command for standby mode is 100V. As stated above, there needs to be a small amount of voltage in the converter in order to generate enough converter current to

charge the DC-Bus capacitor. Figure 4.26 shows the Saber simulation waveform for Transition 3.

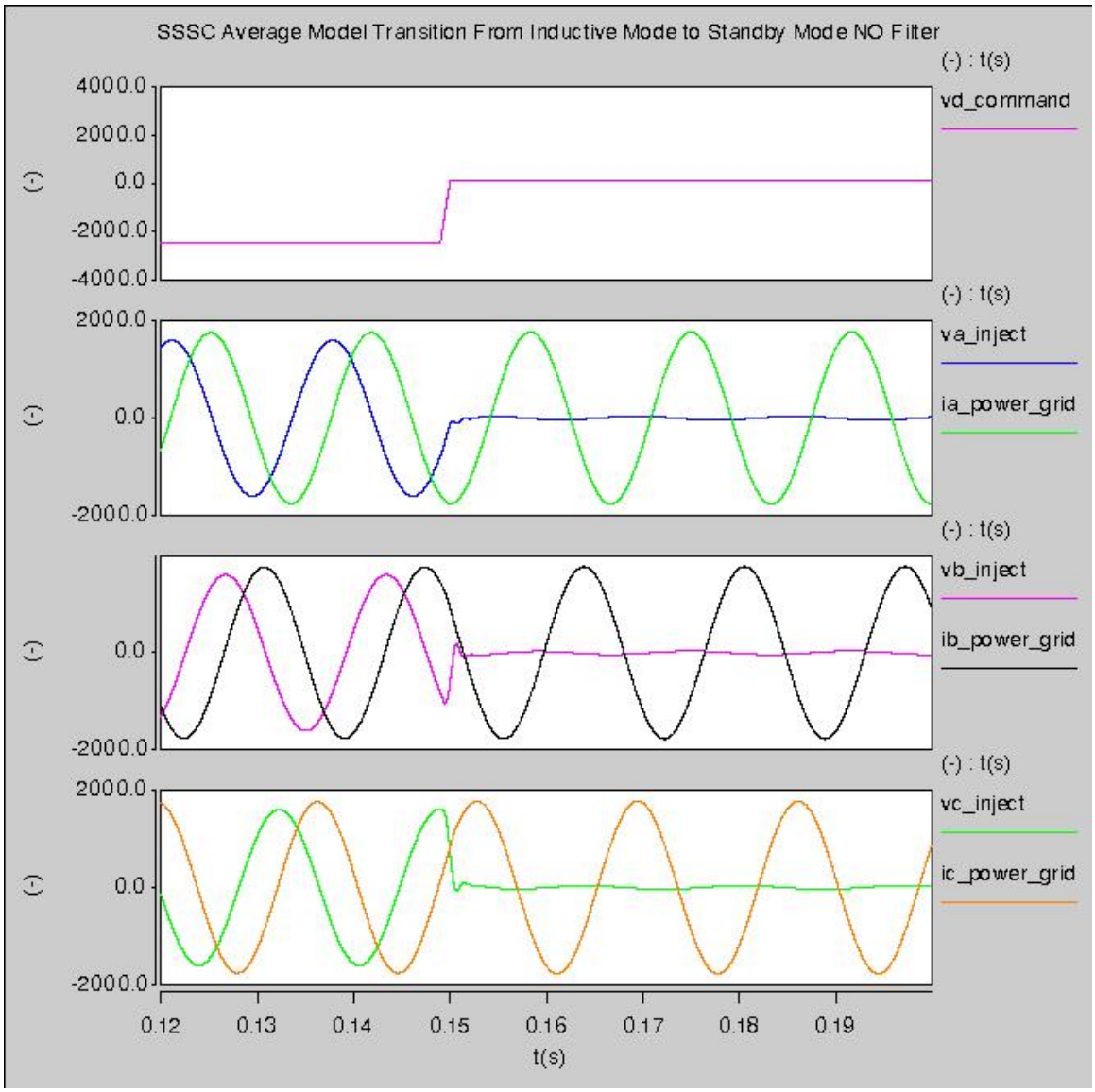


Figure 4.26 - SSSC Average Model Transition from Inductive Mode to Standby Mode.

H. Additional SSSC Average Model Simulation Results

Figure 4.27 is used to show that the DC-Bus voltage is regulated within acceptable margins. In Figure 4.27 there is a small amount of error between the desired DC-Bus voltage of 2500V and the actual DC-Bus voltage. This error is due to the fact that the bandwidth of the DC-Bus control loop is considerably slower than the bandwidth of the D-Channel control loop. Figure 4.28 illustrates the duty cycle response to the given command. Figure 4.29 shows that the D-Channel voltage follows the V_d command very well. Figure 4.29 also shows such parameters as I_d, I_q, and V_q. These parameters will prove to be important when analyzing and verifying the results of the switching model for the SSSC.

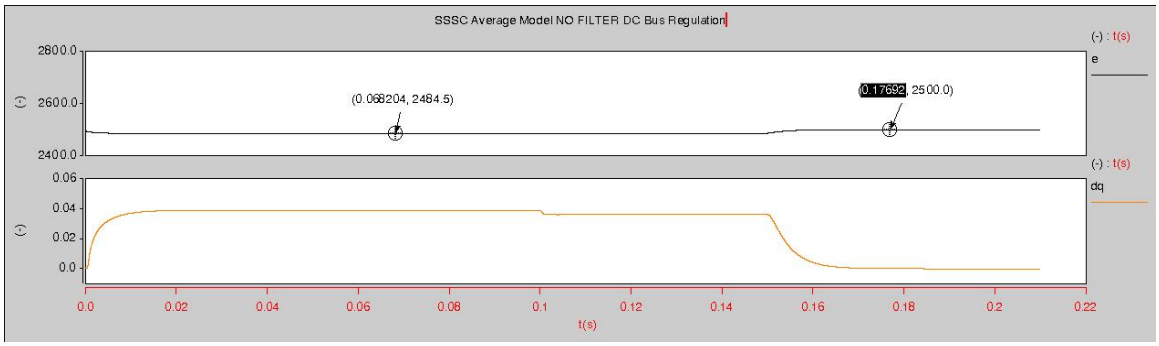


Figure 4.27 - SSSC Average Model DC-Bus Regulation.

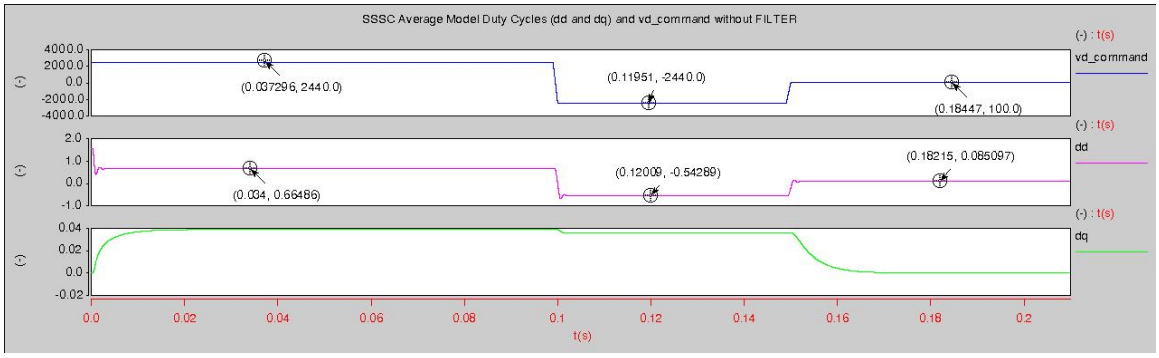


Figure 4.28 - SSSC Average Model Duty Cycles.

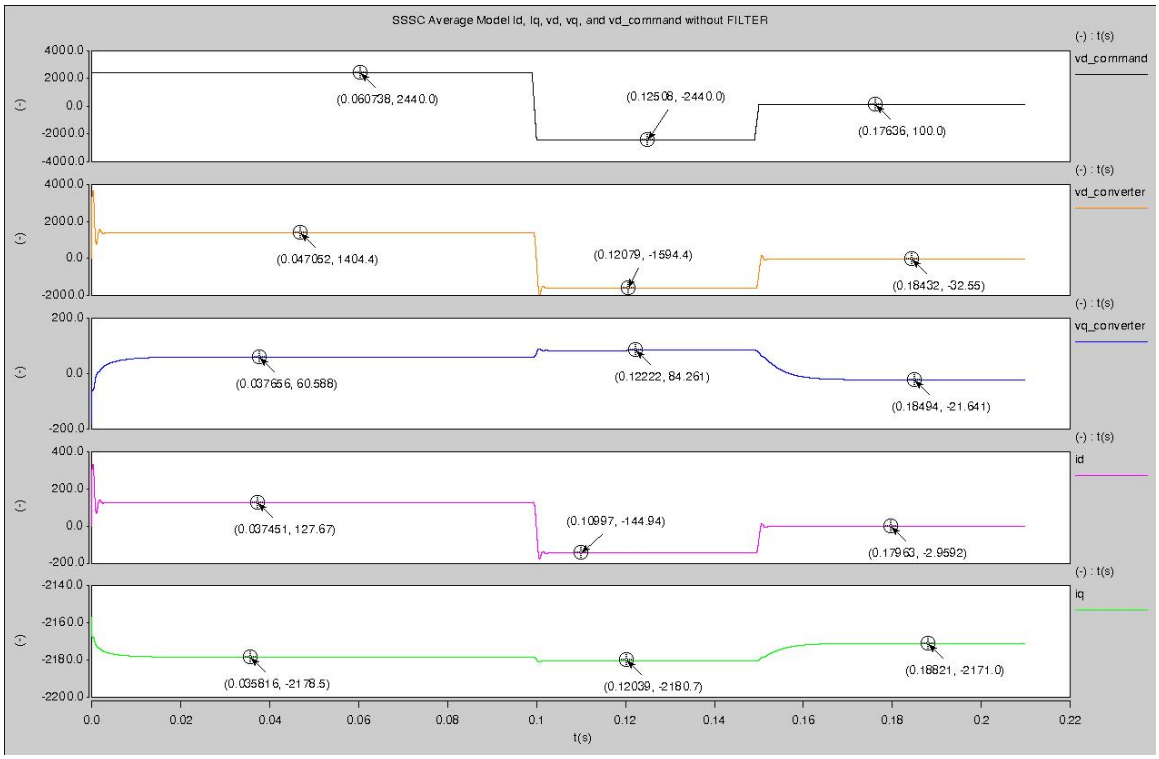


Figure 4.29 - SSSC Average Model V_d Command verses System Parameters.

4.4 Proposed Control System for Three-level CMC-Based SSSC

After the average model has been verified, the feedback-parameter acquisition must be modified before being applied in the actual electrical circuit of the SSSC in which all parameters are in ABC coordinates. Figure 4.30 represents the completed block diagram of the proposed controller for the three-level CMC-Based SSSC. Additions to the control designed for the average model of the three-level cascaded-based SSSC are as follows: a Park's transformation, an inverse Park's transformation, a PWM generator and a phase lock loop (PLL). All feedback parameters are measured using voltage transducers. Initially, all feedback signals are in ABC coordinates. With the proposed control technique, all signals are real-time transferred into DQ0 domain by Park's transformation

matrix[2]. The PLL Block is used to acquire phase information from the power system current in order to generate the appropriate phase angle for the injected voltage. The inputs of the PLL are the three-phase currents in the power grid, and the PLL output is the phase information of the currents at the point of injection in the form of cosine and sine functions. The Park's and its inversed transformation matrix are based on the positive-sequence, three-phase system.

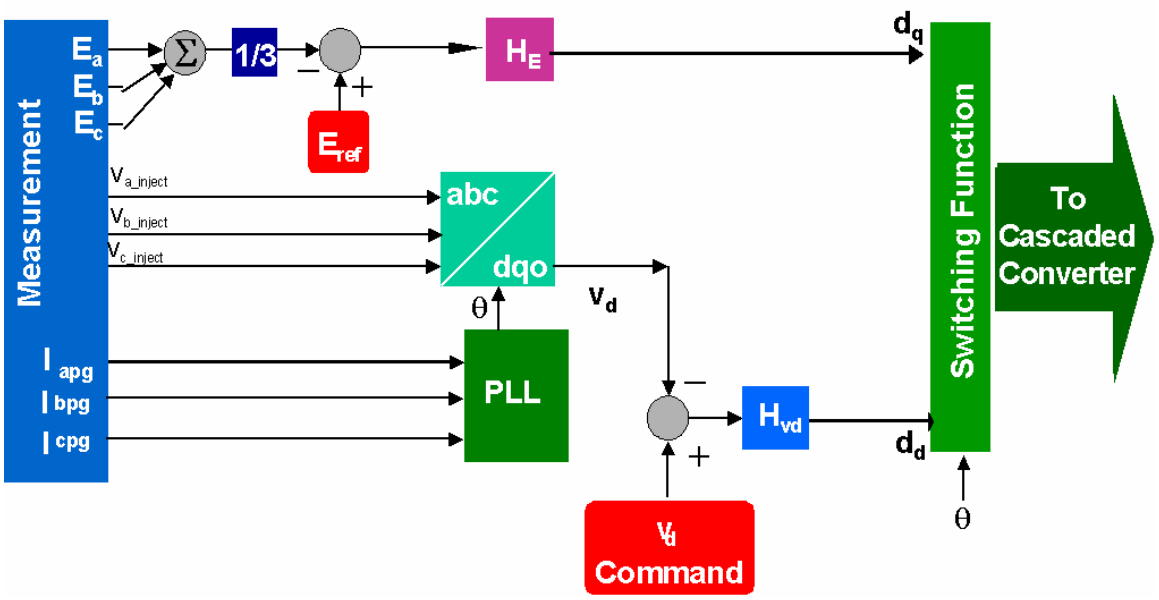


Figure 4.30 - Complete Block Diagram for the Switching Model Controller.

Due to the fact that an average DC voltage-control technique is proposed in the control system, the three-phase DC capacitor voltages, E_a, E_b and E_c, are averaged, and the average value is used as the feedback-control parameter. After all DQ0 parameters are calculated, the control process is the same as described above. The primary objectives of

[2] Derivation of the specific version of the Park's transformation matrix used in this dissertation is shown in Appendix B.

the control system are to make the SSSC respond to the reactive voltage command, V_d, as well as to regulate all three DC capacitor voltages. To alleviate the cross-coupling effects between the D and Q channels, the decoupling technique is adopted.

The products of the feedback control are the duty cycles in the DQ0 coordinates: D_d, D_q and D_0. The SSSC is connected to the three-phase, three-wire power grid and the Zero-Channel, therefore, is omitted. Consequently, D_0 is set to zero. To be able to control the power stage of the SSSC, the duty cycles must be transferred back into ABC coordinates. Once the duty cycle in ABC coordinates (D_a, D_b and D_c) are calculated, these three duty cycles are used as the input of the PWM generator in order to produce the proper switching signals for the power stage.

l. Simulation Results of the Cascaded Three-Level SSSC with the Designed Controller

Based on the small-signal model of the three-level cascaded-based SSSC, the feedback-control parameters are designed, according to the feedback-control design section on page 134 of this thesis. The feedback-control is applied to the completed electrical model of the proposed SSSC. In addition, all parasitic components and power-stage losses are taken into account in the circuit. Figure 4.31 shows the complete simulation schematic for the SSSC Switching Model.

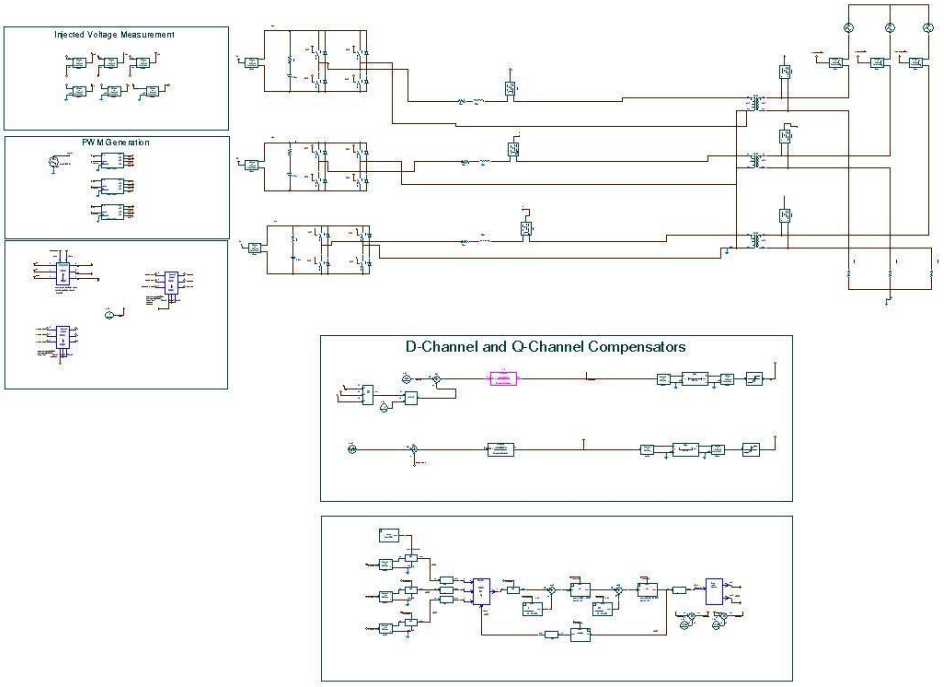


Figure 4.31 - SSSC Switching Model Schematic.

The simulation results for the switching model to follow make one basic assumption. It is assumed that the DC-Bus is initially charged to 2500V through a RC network.

I1. Mode 1 (Capacitive Mode)

Initially, the SSSC begins its mode of operation in capacitive mode. At t = 100 ms, the SSSC is commanded to abruptly change its operation mode from full capacitive mode to full inductive mode by adjusting the V_d command from 2440 to -2440. Due to the assigned current direction during the modeling procedure, the output voltage lags the I_{Line} by 90° in the capacitive mode and leads the I_{Line} by 90° in the inductive mode. In mode 1, the simulation result verifies that phase-A output voltage V_{a_inject}, lags I_{Line} by 90°. Figure 4.32 is used to illustrate capacitive mode of operation.

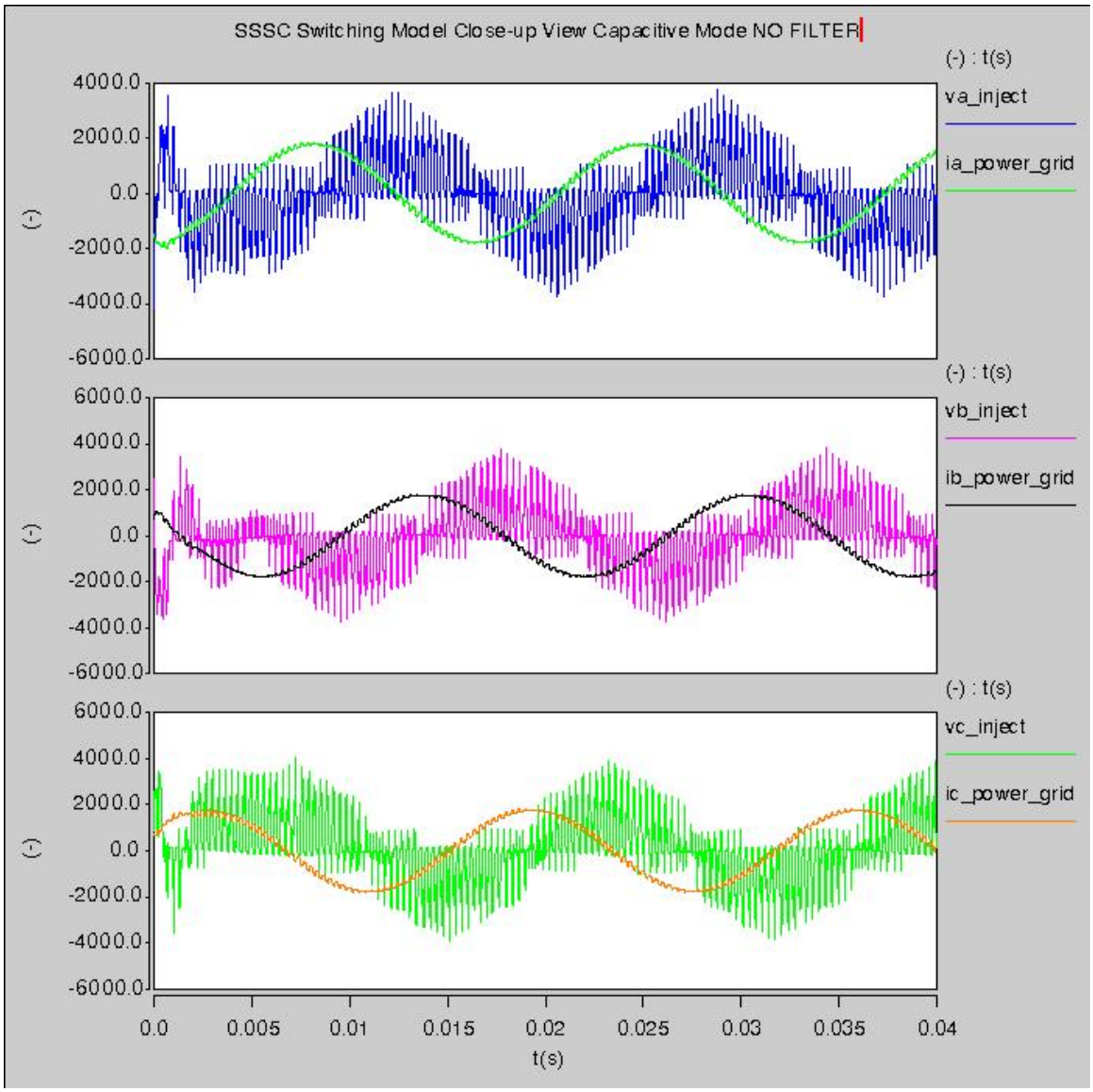


Figure 4.32 - SSSC Switching Model Simulation in Capacitive Mode.

Transition 2: from Mode 1 to Mode 2

As stated above, at t = 100 ms, the SSSC is commanded from full capacitive mode to full inductive mode of operation. Figure 4.33 shows the saber simulation waveform for Transition 2. This transition is the worst-case operation.

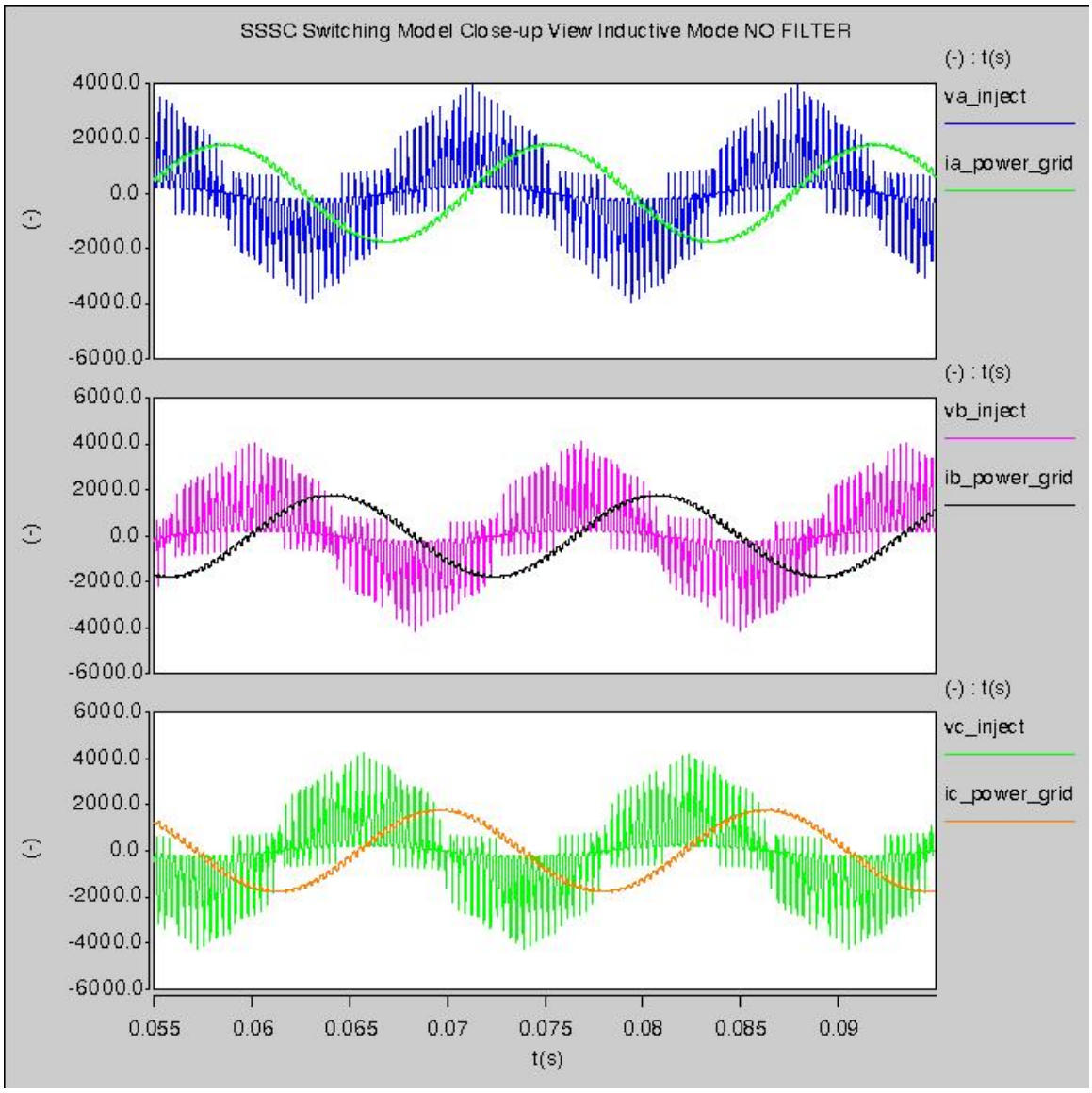


Figure 4.33 - SSSC Switching Model Simulation in Inductive Mode.

Transition 3: from Mode 2 to Mode 3

At t = 150 ms, the SSSC is commanded from full inductive mode of operation to standby mode of operation. During the standby mode of operation only a small amount of voltage is injected into the power system. This voltage can be neglected. The primary reason that there is a small amount of voltage injected into the power grid is due to the fact that the V_d command for standby mode is 100V. There needs to be a small amount of voltage in the converter in order to generate enough converter current to charge the DC-Bus capacitor. Figure 4.34 shows the Saber simulation waveform for Transition 3.

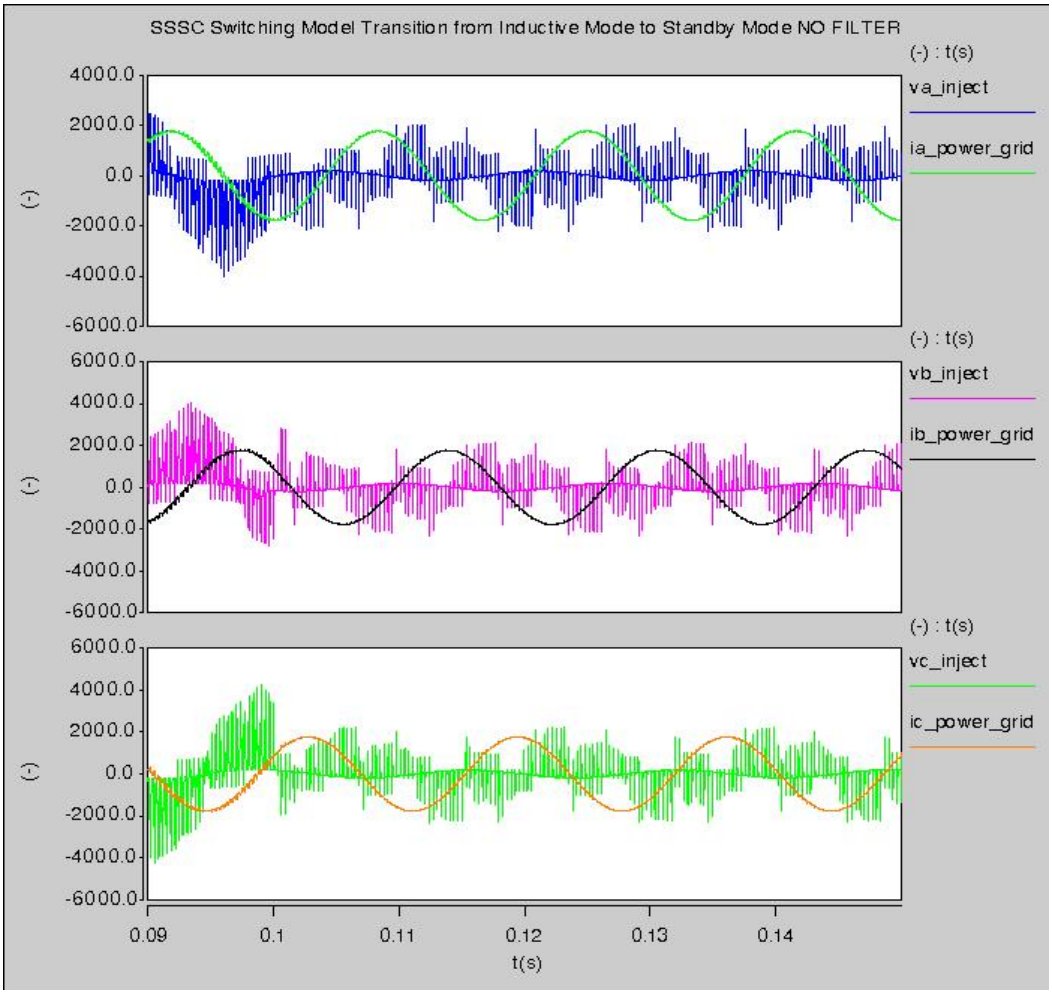


Figure 4.34 - SSSC Average Model Transition from Inductive Mode to Standby Mode.

I2. Additional SSSC Switching Model Simulation Results

Figure 4.35 is used to show that the DC-Bus voltage is regulated within acceptable margins. Figure 4.36 illustrates the duty cycle response to the given command. Figure 4.37 shows that the D-Channel voltage follows the V_d command very well. Figure 4.37 also shows such parameters as I_d, I_q, and V_q.

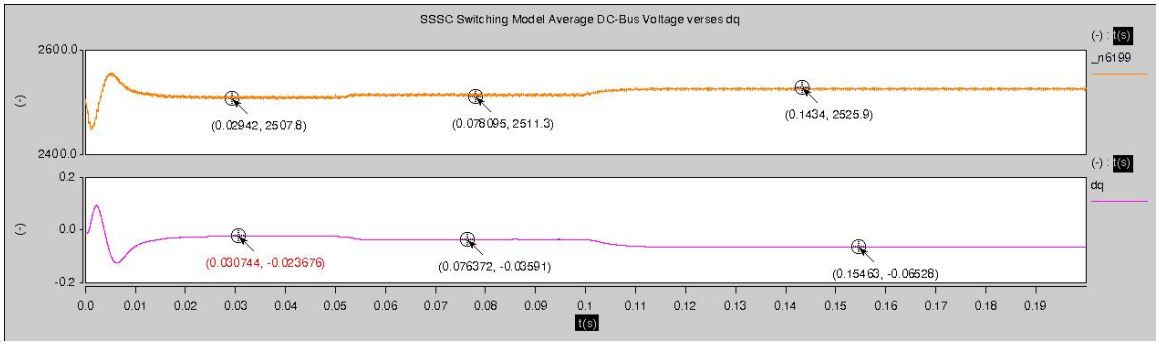


Figure 4.35 - SSSC Switching Model DC-Bus Regulation.

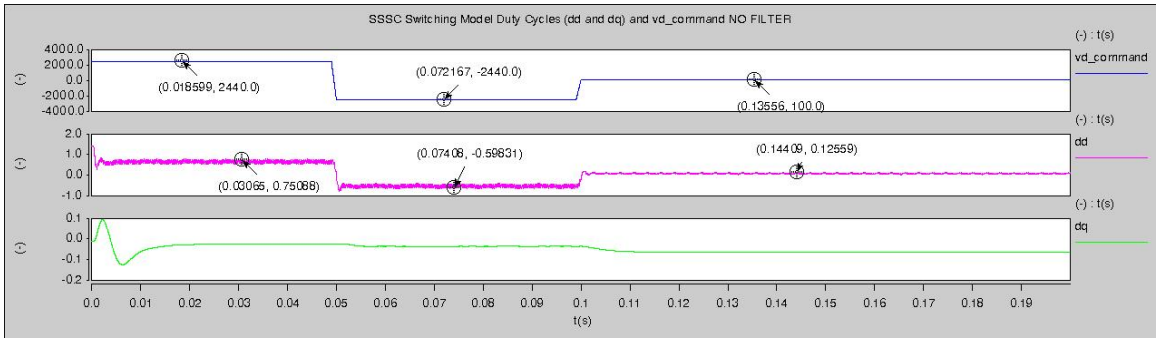


Figure 4.36 - SSSC Switching Model Duty Cycles.

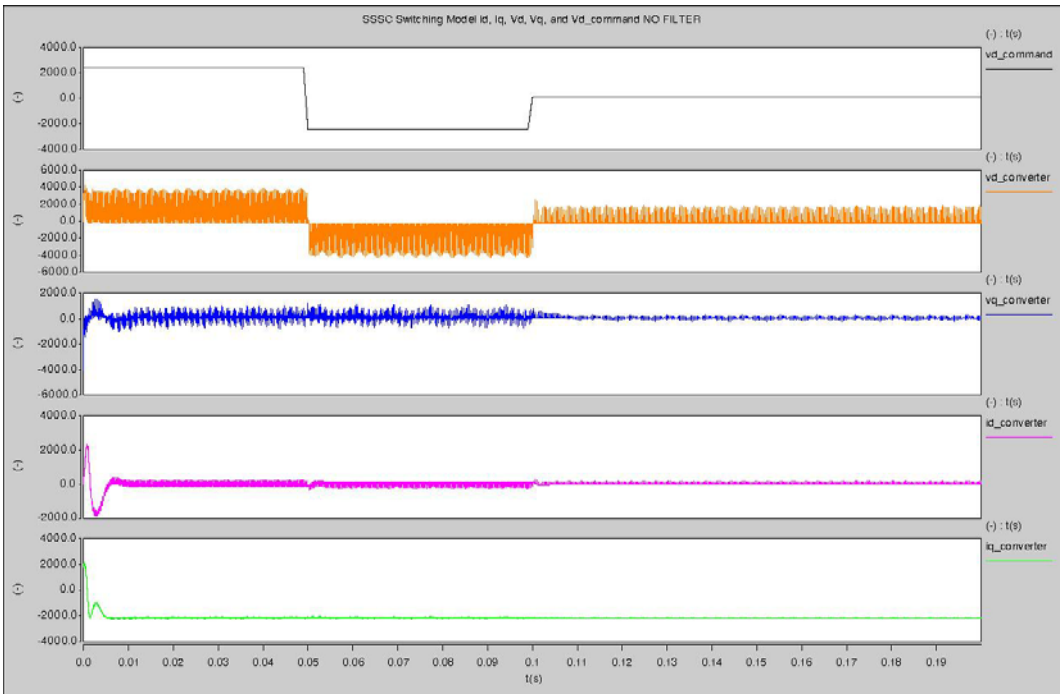


Figure 4.37- SSSC Average Model V_d Command verses System Parameters.

The overall conclusion that can be drawn from comparing the switching model results to the average model results is that in both cases the simulation results are approximately the same. The main difference is that the injected voltage contains a considerable amount of noise. The noise is undesirable and must be removed using a filter. The next step in the design process for the SSSC is to design a filter to remove the noise from the output voltage waveform. Figure 4.38 shows a close-up view of the ripple voltage associated with the three-phase injected voltage.

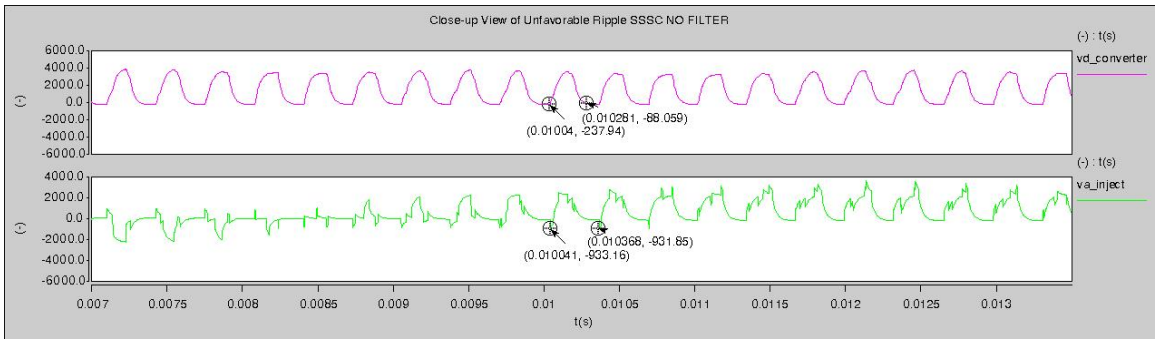


Figure 4.38 - Close-up View of the SSSC Switching Model Injected Voltage Ripple.

4.5 SSSC Switching Model Filter Design

The first step in the design process for the filter that will be used in the switching model of the SSSC is to determine the order of the harmonics inside the injected voltage waveform that must be removed. To determine the order of the harmonics, a THD analysis of the output voltage waveforms is simulated in Saber. Figure 4.39 shows the THD plot obtained from Saber.

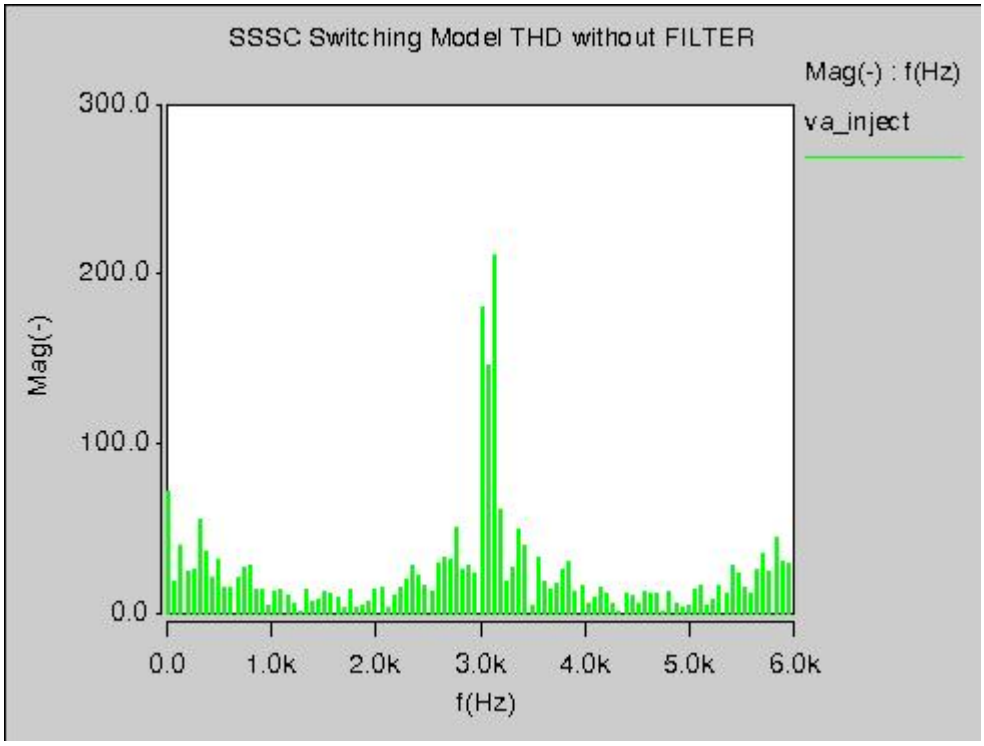


Figure 4.39 - SSSC Switching Model THD Plot.

According to Figure 4.39, the majority of the harmonics are located at twice the switching frequency of 3 kHz. There is also a 6^{th} Harmonic component to the ripple or a 360 Hz ripple. The THD of the phase A injected voltage is 26.38%. The objective of the filter design for the SSSC is to remove the majority of the switching ripple voltage. To accomplish this, a filter with a cut-off frequency of much less than 360 Hz is desirable.

J. SSSC Switching Model Filter Selection

At first glance, it would make sense to design a low-pass filter that has a low cut-off frequency in order to remove the harmonics. The objective of the filter design is to design a low-pass filter with a cutoff frequency of fc=300Hz.

The type of filter that is needed for the SSSC Switching Model is one that contains only passive elements such as inductors and capacitors. The next step in the design process for the filter is to design an LC low-pass filter.

K. *LC Filter Design*

Figure 4.40 shows a schematic of the LC low-pass filter. As the frequency approaches zero, the impedance of the capacitor approaches infinity. As the frequency approaches zero, the impedance of the inductor approaches zero. The capacitor behaves like an open circuit; thus, the input and output voltage is the same. The inductor behaves like a short circuit; thus the input and output voltage is the same. Meaning, the magnitude of the filter transfer function is equal to one. As the frequency approaches infinity, the impedance of the capacitor approaches zero and the capacitor behaves like a short circuit. As the frequency approached infinity, the impedance of the inductor approaches infinity. This means that the magnitude of the filter transfer function is equal to zero.

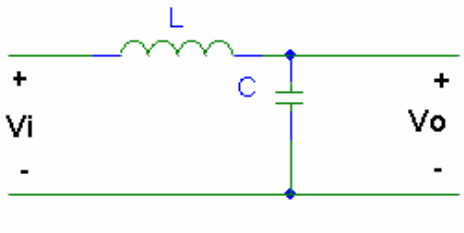


Figure 4.40 - Schematic of LC Filter

Equation 4.25 expresses the final transfer function for the LC filter.

$$H(s) = \frac{V_o(s)}{V_I(s)} = \frac{1/sC}{1/sC + sL} = \frac{1}{s^2 * LC + 1}, where\ s = j\omega \qquad \textbf{Equation 4.25}$$

The magnitude of the transfer function for the LC filter can be expressed as Equation 4.26.

$$|H(s)| = \left|\frac{V_o(s)}{V_I(s)}\right| = \frac{1}{\sqrt{\omega^2 + (\omega_{LC}{}^2)^2}} \qquad \textbf{Equation 4.26}$$

The first step in the design process for the LC filter is to select a value for C. Next, design the cut-off frequency. Finally, calculate the value for L. The step-by-step procedure is shown below:

$Step 1: Select\ a\ value\ for\ C$

$Let\ C = 400\mu F$

$Step 2: Design\ the\ cut-off\ \ frequency$

$$\omega_{Lc} = \frac{1}{\sqrt{LC}} = 2\pi f_c$$

$$Let\ \omega_{Lc} = 2112.8Hz$$

$$f_c = 336.26Hz$$

$Step 3: Calculate\ L$

$$\omega_{Lc} = \frac{1}{\sqrt{L * 560\mu}} = 2112.8 \qquad \textbf{Equation 4.27}$$

$$L = 560\mu H$$

Once the LC filter has been designed the next step is to re-simulate the average and switching models for the SSSC to see the effect that the filter has on the closed-loop controller design. The controller needs to be checked for stability and to see if the SSSC models still work.

L. SSSC Transfer Function Derivation with LC Filter

Once the design of the CMC-Based SSSC dictates that a filter must be used to filter out the undesirable voltage harmonics, the initial design process is repeated again to observe the effects that the filter has on the system transfer functions. As stated above, the only open-loop equation used to design the compensator for the D-Channel is the Control-to-Output-Voltage Transfer function $G_{vdd.}$ Since the characteristic equations for the open-loop transfer functions with an LC filter are complex, the decision is made to use the MatLab simulation waveforms as a guide for designing the compensators for the LC filter addition to the SSSC.

M. DC Steady-State Solution with LC Filter

Before the open-loop transfer functions for the SSSC with the addition of the LC filter could be obtained, the DC steady-state solution for the SSSC is derived. Figure 4.41 shows the saber simulation schematic used to obtain the DC steady-state solution for the SSSC.

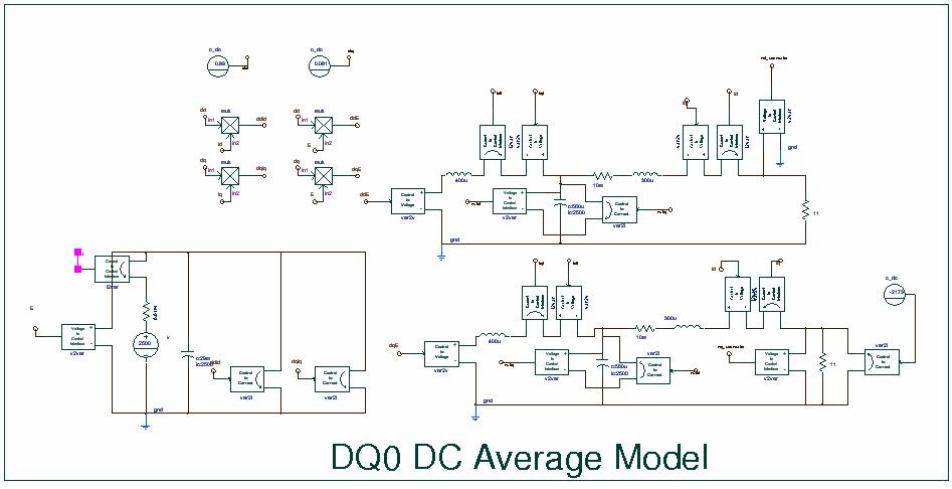


Figure 4.41 – Saber Simulation Schematic for the DC Steady-State Solution with LC Filter

The DC steady-state equations are as follows:

$$d_d * i_d = -d_q * i_q \quad \textbf{Equation 4.28}$$

$$V_{Cd} = d_d * E + \omega * L_f * i_{q1} \quad \textbf{Equation 4.29}$$

$$V_{Cq} = d_q * E - \omega * L_f * i_{d1} \quad \textbf{Equation 4.30}$$

$$V_{Cd} = (R_T + R_L) * i_d + \omega * L_T * i_q \quad \textbf{Equation 4.31}$$

$$V_q = V_{Cq} + R_T * i_q - \omega * L_T * i_{dq} \quad \textbf{Equation 4.32}$$

$$i_{q1} = \omega * V_{Cd} * C_f + i_q \quad \textbf{Equation 4.33}$$

$$i_{d1} = \omega * V_{Cq} * C_f + i_d \quad \textbf{Equation 4.34}$$

$$i_d = \frac{V_{d\_ref}}{R_L} \quad \textbf{Equation 4.35}$$

$$i_q = -I_q - \frac{V_q}{R_L} \quad \textbf{Equation 4.36}$$

I_q is represents the power grid current transformed into the dq0 frame. Since the current is aligned with the q-axis, V_q is equal to zero and V_{d_ref} is equal to the value of the command. I_{abc} and V_{d_ref} are calculated as follows:

$$I_{abc} = \frac{V_{Power}}{R_L} = \frac{13.8kV}{11.0} = 1254.0Amps \quad \textbf{Equation 4.37}$$

$$V_{d\_ref} = \%compensation * V_{Power} * \sqrt{\frac{3}{2}} = 2200V \quad \textbf{Equation 4.38}$$

The next step in the derivation of the DC steady-state solution is to transform the current represented via Equation 4.7 into its Q-Axis current represented by Equation 4.9.

$$I_q = \sqrt{2.0} * \frac{V_{Power}}{R_L} * \sqrt{3/2} = 2173Amps \quad \textbf{Equation 4.39}$$

The DC solution for the SSSC was derived by systematically solving Equations 4.28 – 4.36 in MatLab.

Table 4.5 compares the analytical DC steady-state solution to the simulated DC steady state solution for accuracy.

TABLE 4.5 - COMPARISON BETWEEN CALCULATED AND SIMULATED DC STEADY-STATE SOLUTIONS WITH LC FILTER.

Parameter	Calculated Values	Simulated Value
$\mathbf{E}$	2500	2500
$\mathbf{D_d}$	0.89	0.89
$\mathbf{D_q}$	0.081	0.081
$\mathbf{i_d}$	200.00	199.26
$\mathbf{i_q}$	-2184.00	-2185.10
$\mathbf{v_d}$	2200.00	2191.80
$\mathbf{v_q}$	123.89	133.31
$\mathbf{i_{dlf}}$	234.27	219.34
$\mathbf{i_{qlf}}$	-1786.00	-1800.00
$\mathbf{v_{dcf}}$	1955.00	1909.00
$\mathbf{v_{qcf}}$	168.35	177.00

Figure 4.42 shows the Saber simulation waveforms for the DC steady-state solution. Figure 4.43 shows the Saber simulation waveforms for the cross-coupling effects of the LC filter. Figure 4.44 shows the DC steady-state solution for Equation___. In order for the DC source to be removed and the circuit to maintain a true DC steady-state the current (i) in Figure 4.44 must be small.

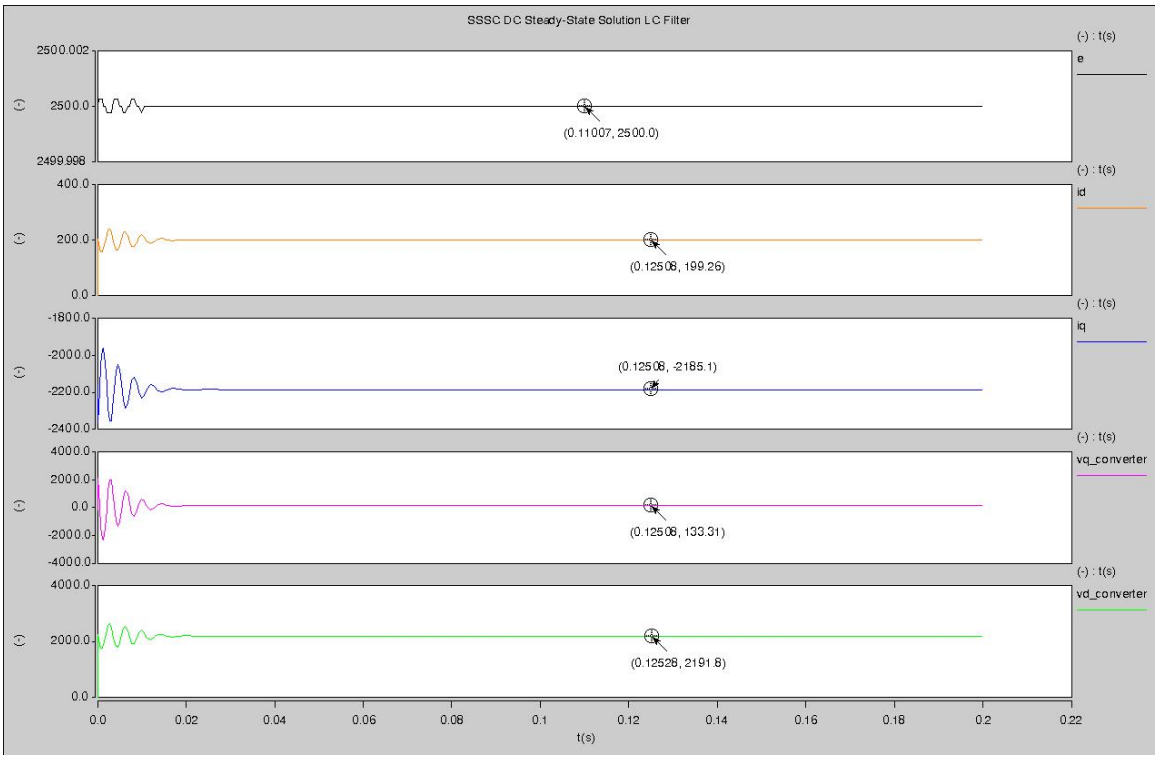


Figure 4.42 – DC Simulation Results with LC Filter

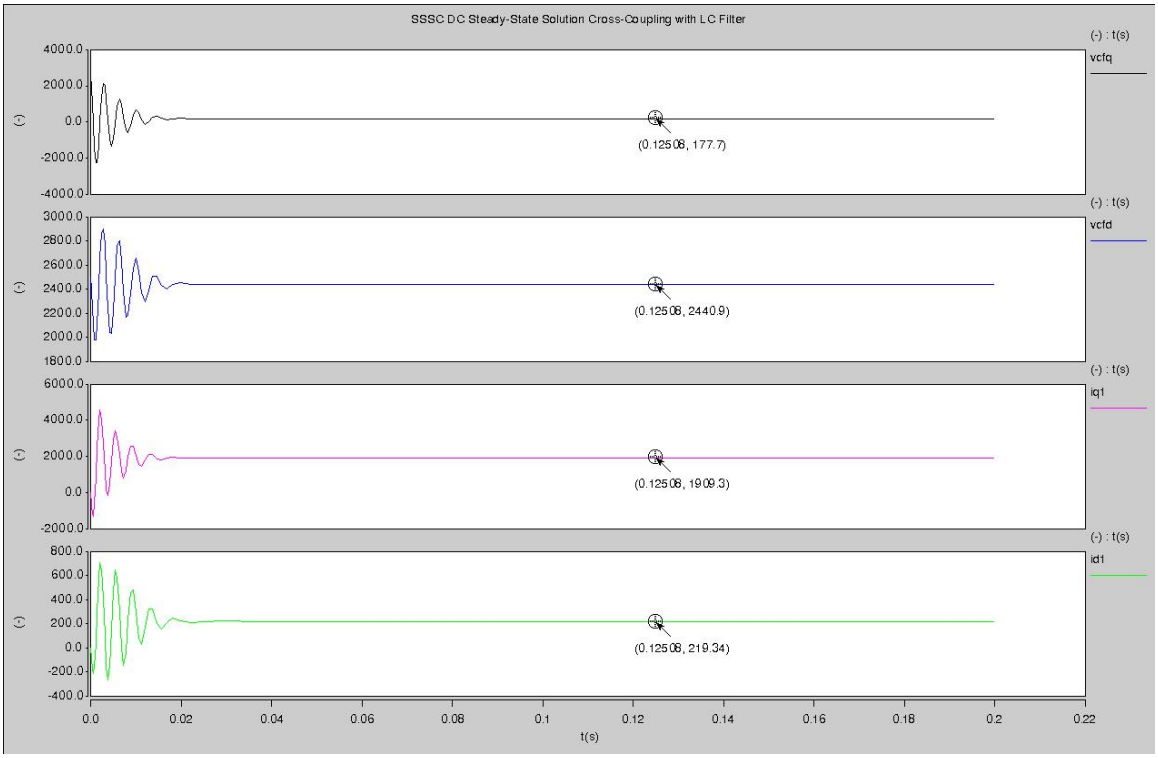


Figure 4.43 - Cross-Coupling effect of the LC Filter

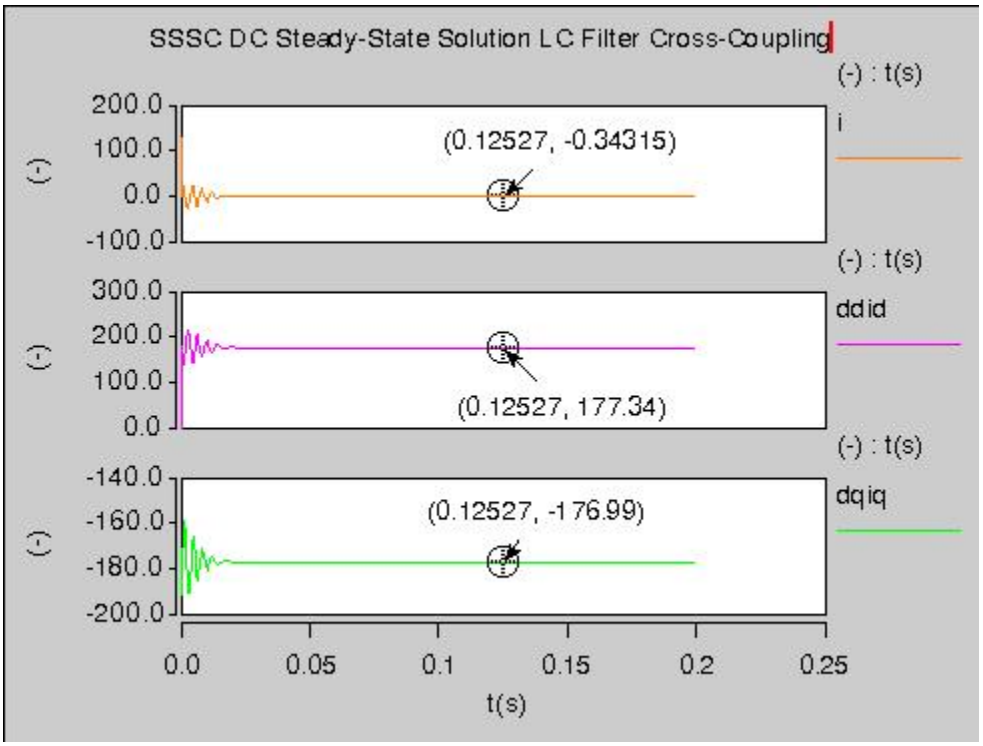


Figure 4.44 – True DC Steady-State Condition for SSSC with an LC Filter.

M1. D-Channel Transfer Function with LC Filter

There are three transfer functions that correspond to perturbations in the D-Channel. Each transfer function is defined by its MatLab simulation waveform. Figure 4.45 shows the MatLab simulation schematic used to obtain the open-loop transfer functions for D-Channel and Q-Channel. The only difference between Figure 4.45 and the circuit shown in Figure 4.9 is that the cross-coupling effects that the addition of the LC filter has on the SSSCs' average model are added. Once again, the assumption is made that the DC Bus voltage is regulated.

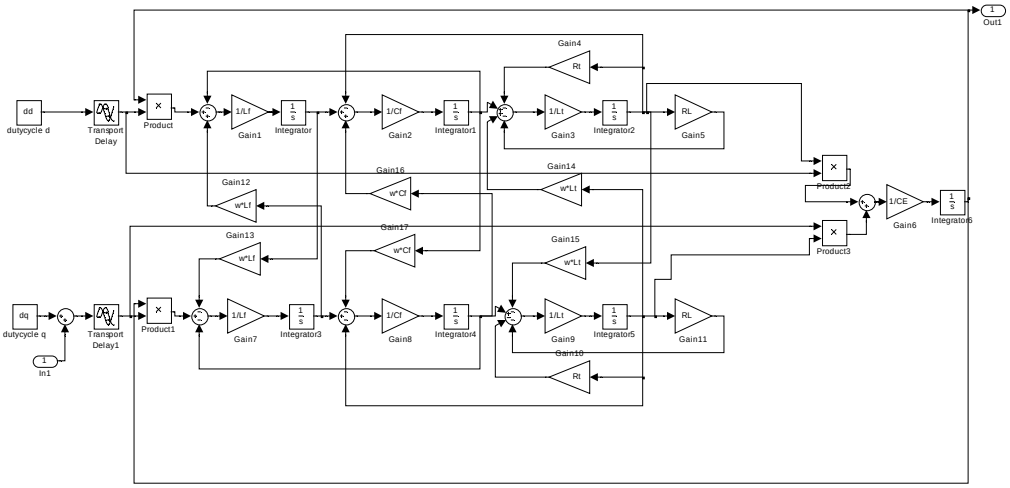


Figure 4.45 MatLab SSSC Small Signal Model with LC Filter

Control-to-Output-Voltage Transfer Function G_{vdd}

Figure 4.46 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Voltage Transfer Function G_{vdd} with LC Filter.

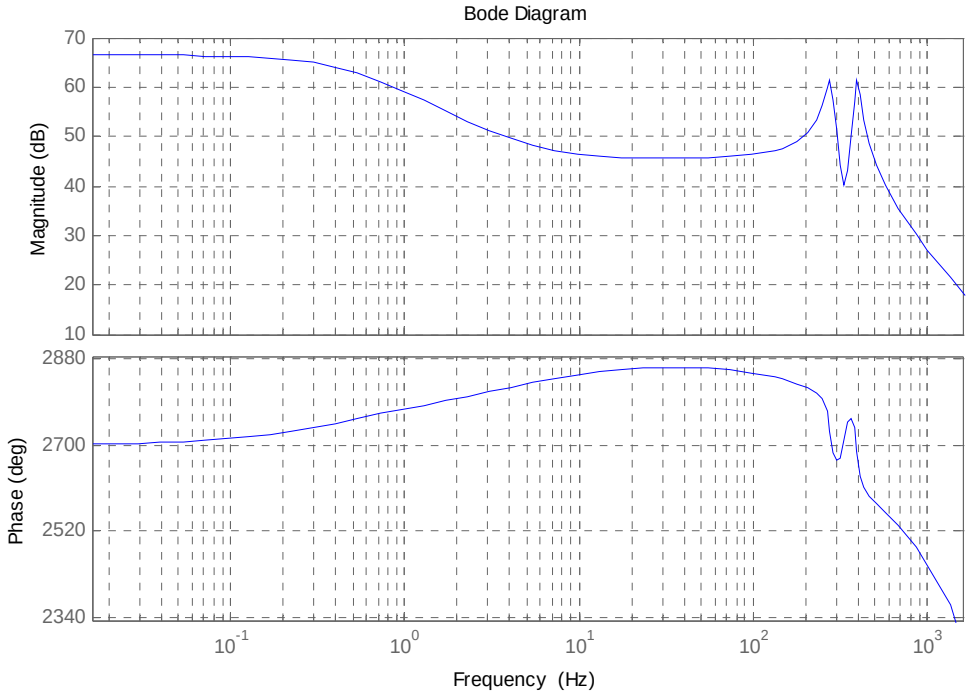


Figure 4.46 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{vdd} with LC Filter.

Due to the complexity of these equations, it becomes difficult to derive them without making mathematical mistakes. As a result the MatLab simulation waveforms are used as the basis for any compensator changes needed for correct operation of the SSSC with a LC filter. For completeness, the remaining open-loop transfer functions for the SSSC with a LC filter will be shown as MatLab simulation waveforms.

Control-to-Output-Current Transfer Function G_{idd}

Figure 4.47 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Current Transfer Function G_{idd}.

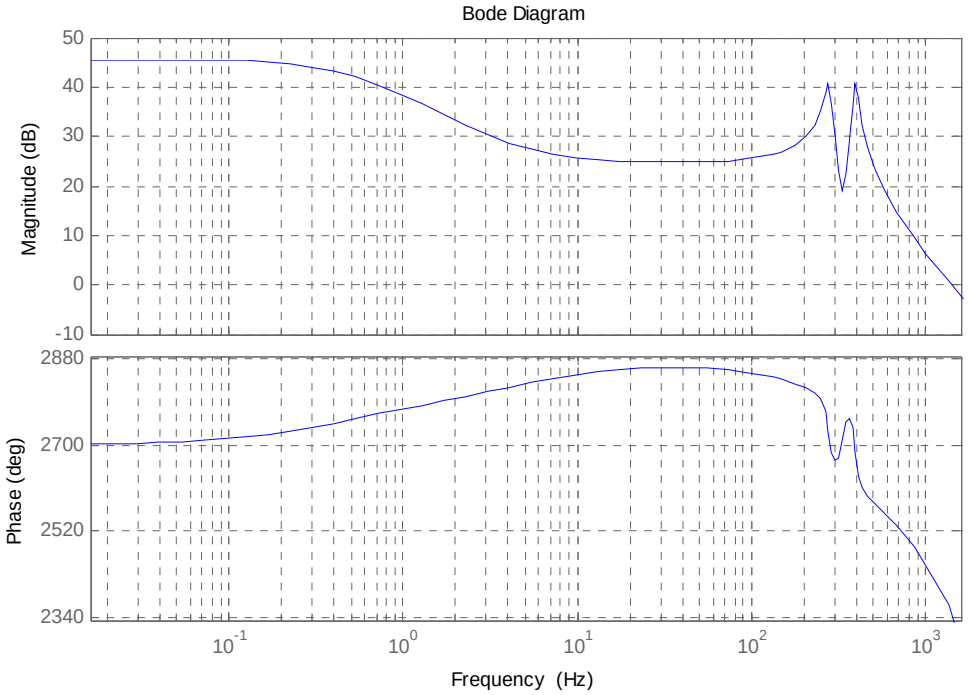


Figure 4.47 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{idd} with LC Filter.

Control-to-Cross-Coupling-Output-Current Transfer Function G_{idq}

Figure 4.48 shows the MatLab simulation plot for the gain and phase of the Control-to-Cross-Coupling-Output-Current Transfer Function G_{idq}.

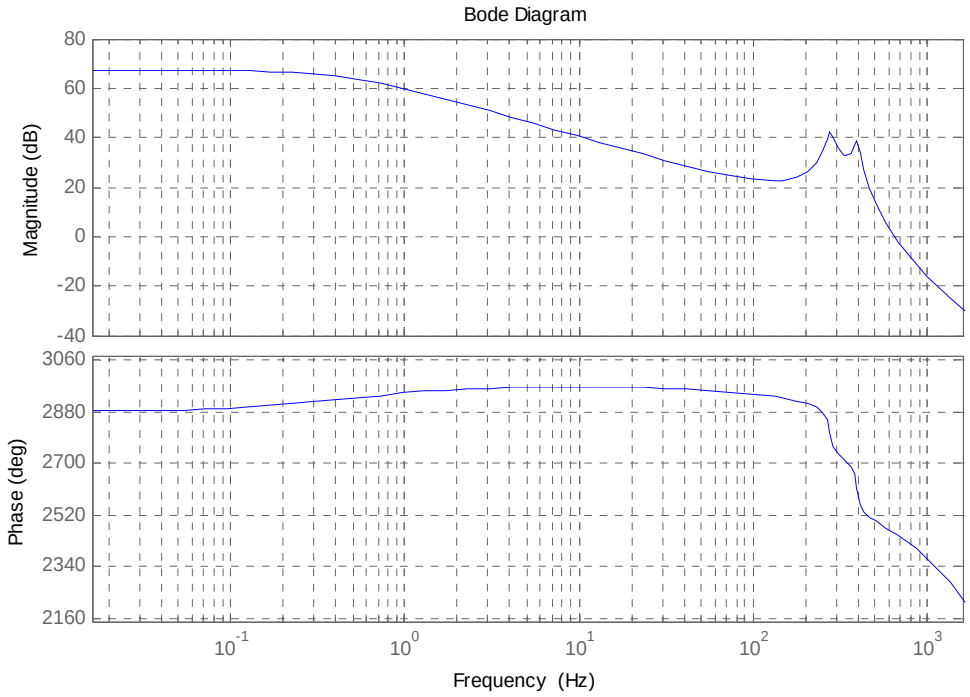


Figure 4.48 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{idq} with LC Filter.

M2. Q-Channel Transfer Function

There are four transfer functions that correspond to perturbations in the Q-Channel. Each transfer function is defined with its MatLab simulation waveform.

Control-to-Output-Voltage Transfer Function G_{vqq}

Figure 4.49 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Voltage Transfer Function G_{vqq}.

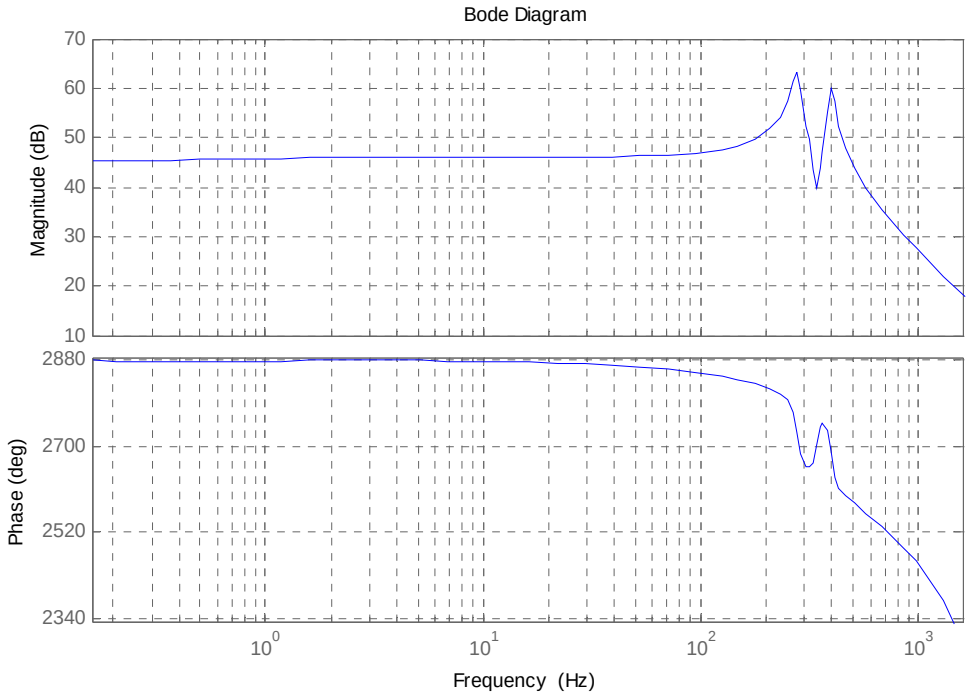


Figure 4.49 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function $G_{vqq.}$

Control-to-Output-Current Transfer Function G_{iqq}

Figure 4.50 shows the MatLab simulation plot for the gain and phase of the Control-to-Output-Current Transfer Function G_{iqq}.

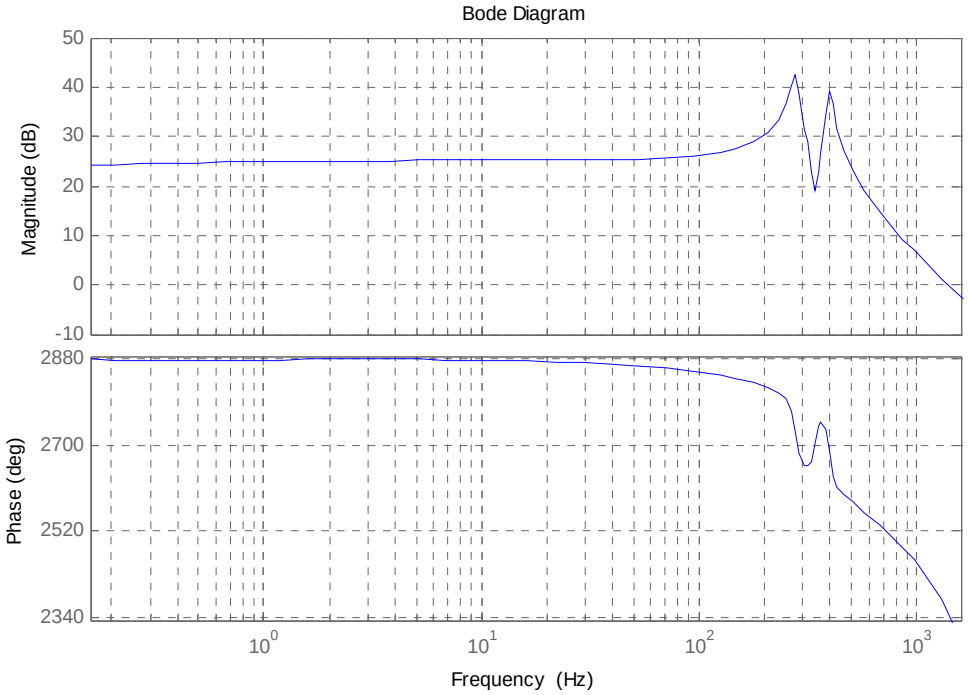


Figure 4.50 – MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{iqq} with LC Filter.

Control-to-Cross-Coupling-Output-Current Transfer Function G_{iqd}

Figure 4.51 shows the MatLab simulation plot for the gain and phase of the Control-to-Cross-Coupling-Output-Current Transfer Function G_{iqd}.

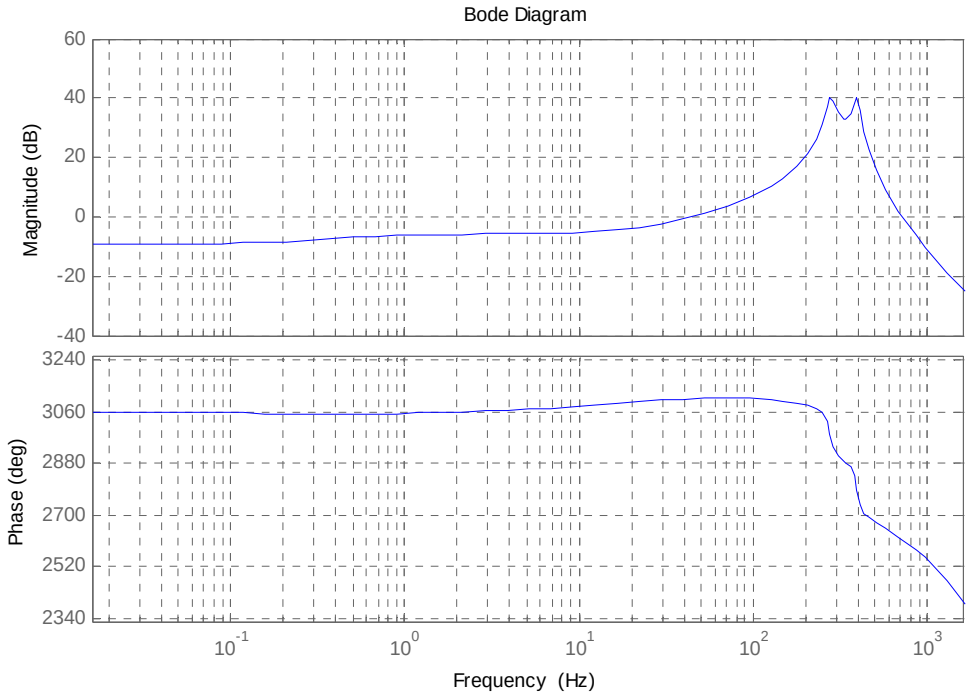


Figure 4.51 - MatLab Simulation Waveforms for the Gain and Phase of the Open-Loop Transfer Function G_{iqd} with LC Filter.

Control-to-DC-Bus-Voltage G_{Eq}

Figure 4.52 shows the control-to-DC-Bus-Voltage transfer function obtained from MatLab.

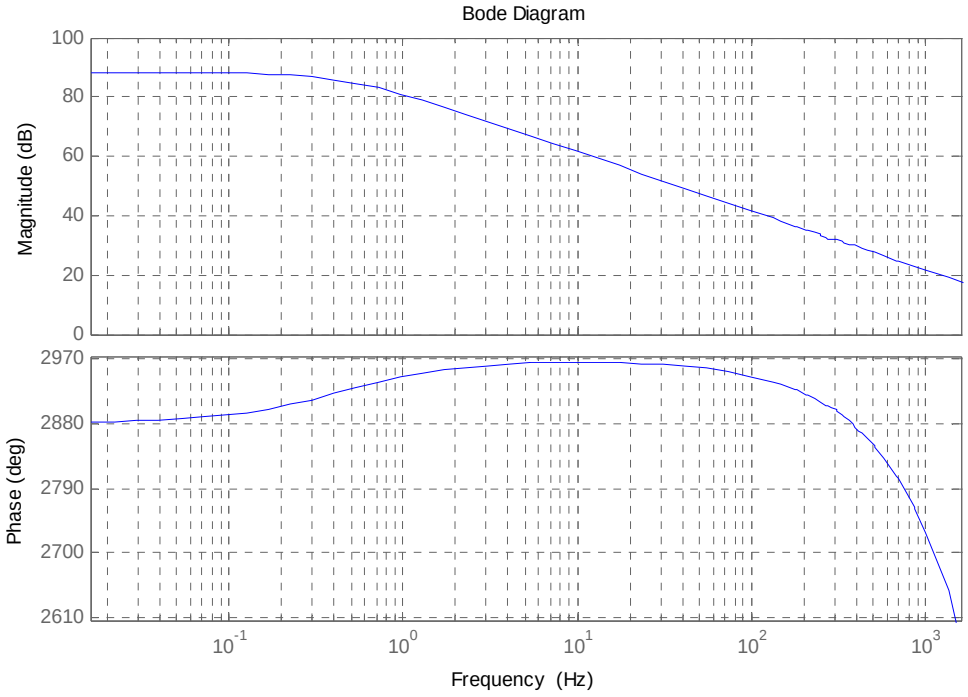


Figure 4.52 - MatLab Simulation Waveform for the Control-To-DC-Bus-Voltage Transfer Function with LC Filter

N. Design of Voltage Compensator, H_{vd} with LC Filter

The standard pole zero controller is optimized using the MatLab SISO tool. The general rules used for the compensators are as follows:

4. The Gain Margin of the closed-loop system should be at least 10dB.
5. The Phase Margin of the closed-loop system should be larger than 30°.
6. The crossover frequency should be as high as possible but must satisfy the Nyquist criteria.

The desired crossover is normally selected to be as high as possible, but must be less than 1.5 kHz, which is half of the effective switching frequency. In this case, the resonant peak frequency of the filter (300 Hz) is too close to the desired crossover frequency of 200 Hz. Therefore, in order for the system to be stable the crossover frequency must be low.

Equation 4.40 expresses the characteristic equation of the designed controller.

$$H_{vd}(s) = 0.015 * \frac{1.0}{(1.0 + 0.031 * s) * (1.0 + 0.0022 * s)} \qquad \textbf{Equation 4.40}$$

TABLE 4.6 - GAIN MARGIN, PHASE MARGIN, AND CROSSOVER FREQUENCY OF THE DESIGNED D-CHANNEL CONTROLLER

Gain Margin	Phase Margin	Crossover Frequency
10.8dB	43.7°	47.3 Hz

Figure 4.53 shows the Gain and Phase plot of the D-Channel compensator designed using the SISO tool in MatLab.

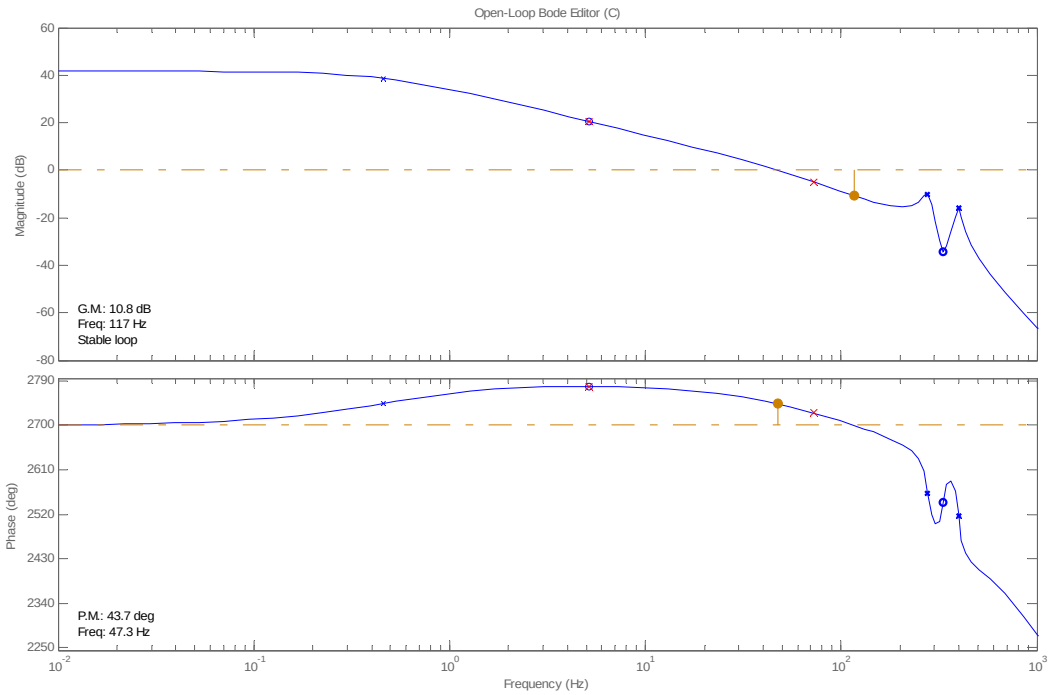


Figure 4.53 – Closed-Loop Bode Plot for the H_{vd} Compensator.

O. Design of DC Capacitor Voltage Compensator, H_{Eq}

With the D-Channel voltage loop closed, the next step is to design the Q-Channel voltage compensator to control the DC-Bus voltage.

The Bode plot obtained from MatLab of transfer function $G_{Edq}(S)$ is shown in Figure 4.52. A compensator is needed to regulate the DC-Bus voltage around its operating point. It is customary to design the crossover frequency for the DC-Bus loop low. In other words, the response of the compensator to regulate the DC-Bus need not be as fast (the crossover frequency is low) as the compensator for the D-Channel voltage loop. Equation 4.41 expresses the characteristic equation of the designed controller.

$$H_{vd}(s) = 0.0034 * \frac{1.0}{(1.0 + 0.002 * s)} \qquad \textbf{Equation 4.41}$$

Table 4.7 shows the Gain Margin, Phase Margin, and Crossover Frequency of the designed controller.

TABLE 4.7 - GAIN MARGIN, PHASE MARGIN, AND CROSSOVER FREQUENCY OF THE DESIGNED Q-CHANNEL CONTROLLER

Gain Margin	Phase Margin	Crossover Frequency
15.8 dB	56.7°	37.0 Hz

Figure 4.54 shows the Gain and Phase plot of the D-Channel compensator designed using the SISO tool in MatLab.

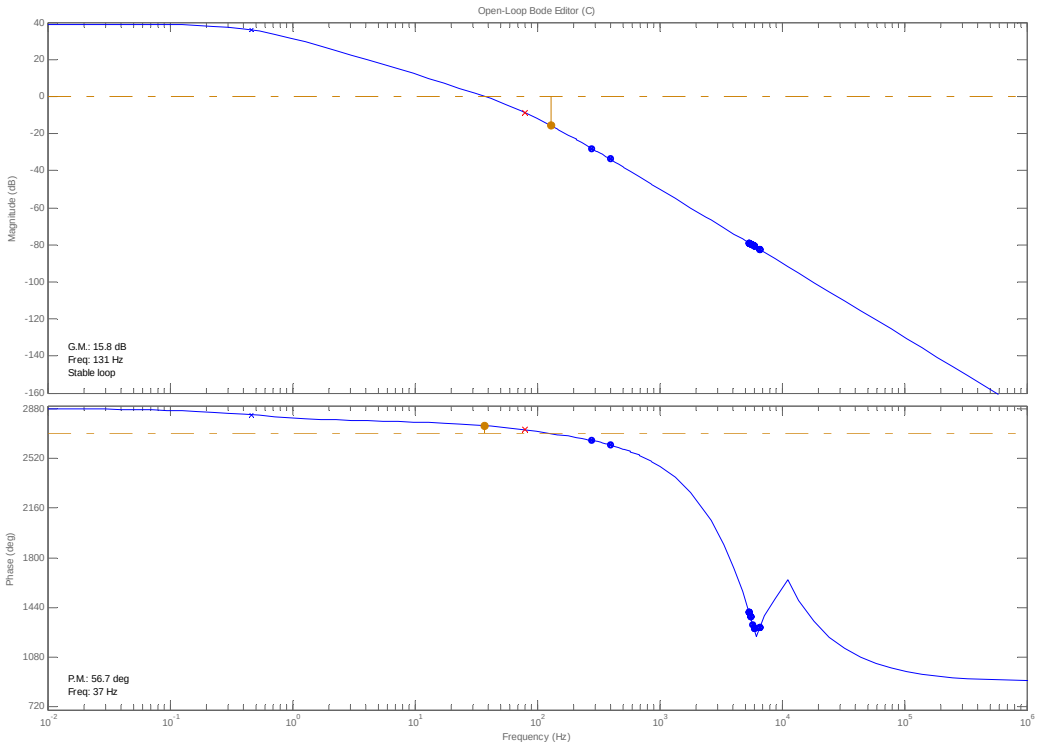


Figure 4.54 – Closed-Loop Bode Plot for the H_{Eq} Compensator.

P. SSSC Average Model Simulation Results with LC Filter

The simulation results from the average model make one basic assumption. It is assumed that the DC-Bus is initially charged to 2500V.

P1. Mode 1 (Capacitive Mode)

Initially, the SSSC begins its mode of operation in capacitive mode. At t = 100 ms, the SSSC is commanded to abruptly change its operation mode from full capacitive mode to full inductive mode by adjusting the V_d command from 2440 to -2440. Due to the assigned current direction during the modeling procedure, the output voltage lags the I_{Line} by 90° in the capacitive mode and leads the I_{Line} by 90° in the inductive mode. In mode 2, the simulation result verifies that phase-A output voltage V_{a_inject}, lags I_{Line} by 90°. Figure 4.55 is used to illustrate capacitive mode of operation.

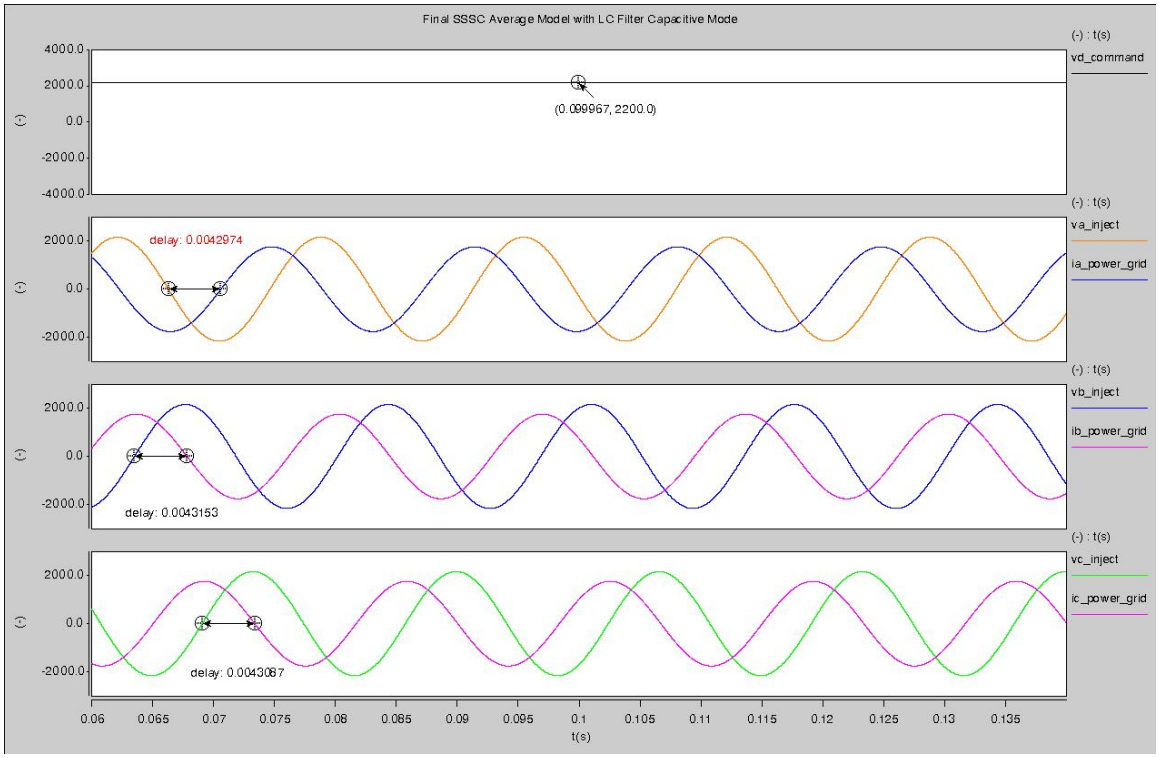


Figure 4.55 - SSSC Average Model Simulation in Capacitive Mode with LC Filter.

Transition 2: from Mode 1 to Mode 2

At t = 100 ms, the SSSC is commanded from full capacitive mode to full inductive mode of operation. Figure 4.56 shows the saber simulation waveform for Transition 2. This transition is the worst-case operation.

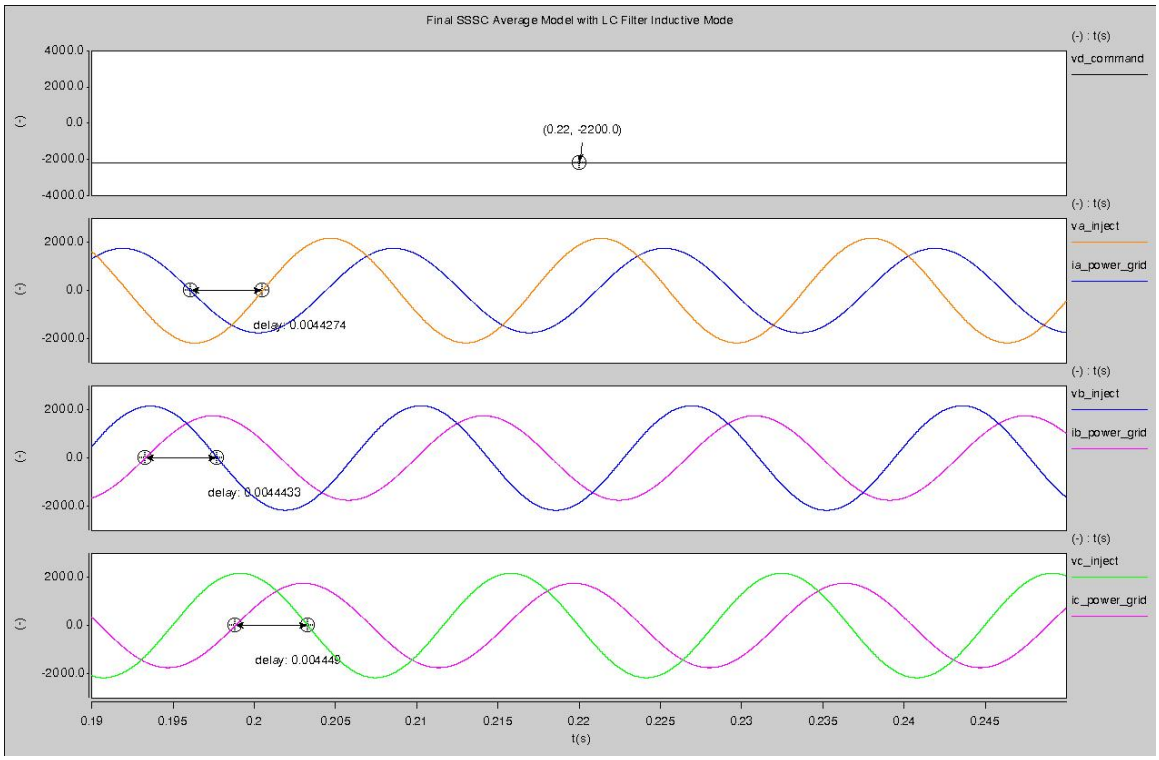


Figure 4.56 - SSSC Average Model Simulation in Inductive Mode with LC Filter.

Transition 3: from Mode 2 to Mode 3

At t = 150 ms, the SSSC is commanded from full inductive mode of operation to standby mode of operation. During the standby mode of operation only a small amount of voltage is injected into the power system. This voltage can be neglected. The primary reason that there is a small amount of voltage injected into the power grid is due to the fact that the V_d command for standby mode is 100V. A small amount of voltage in the

converter is required in order to generate enough converter current to charge the DC-Bus capacitor. Figure 4.57- shows the Saber simulation waveform for Transition 3.

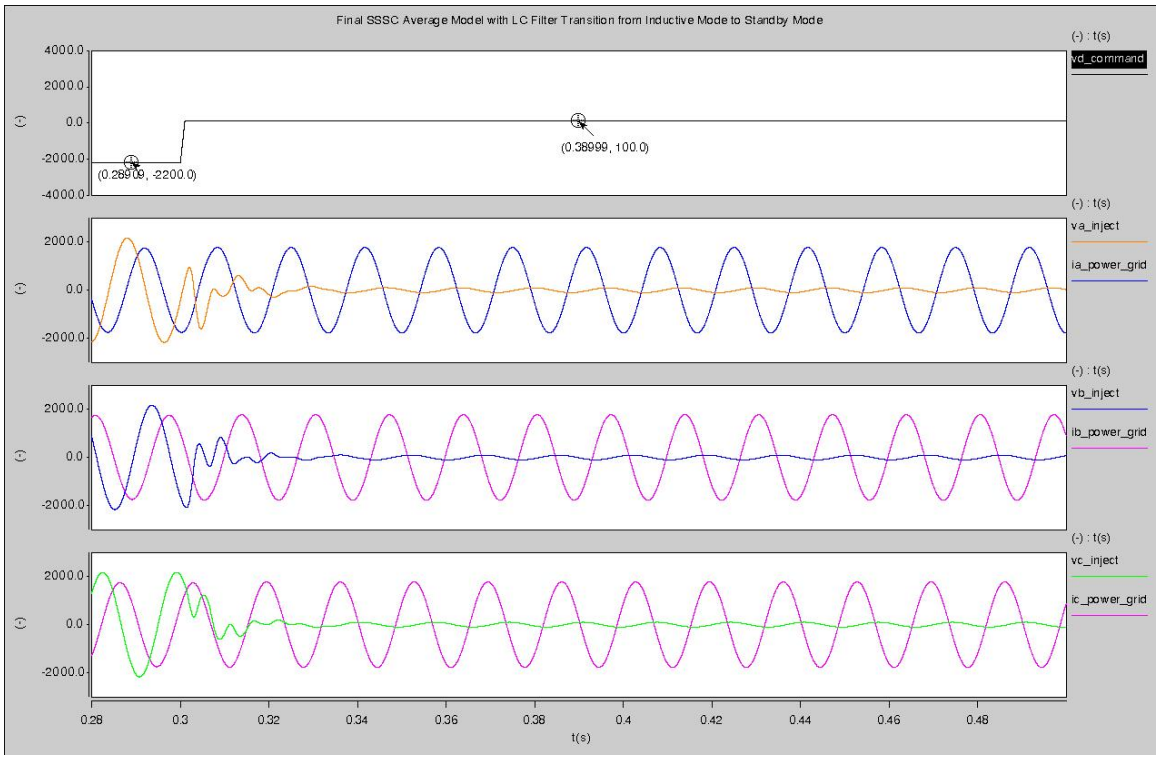


Figure 4.57 - SSSC Average Model Transition from Inductive Mode to Standby Mode.

Q. *Additional SSSC Average Model Simulation Results with LC Filter*

Figure 4.58 is used to show that the DC-Bus voltage is regulated within acceptable margins. Figure 4.59 illustrates the duty cycle response to the given command. Figure 4.60 shows that the D-Channel voltage follows the V_d command very well. Figure 4.60 also shows such parameters as I_d, I_q, and V_q. These parameters will prove to be important when analyzing and verifying the results of the switching model for the SSSC. Figure 4.61 illustrates the operation of the SSSC Average Model with the LC filter over the entire operating range.

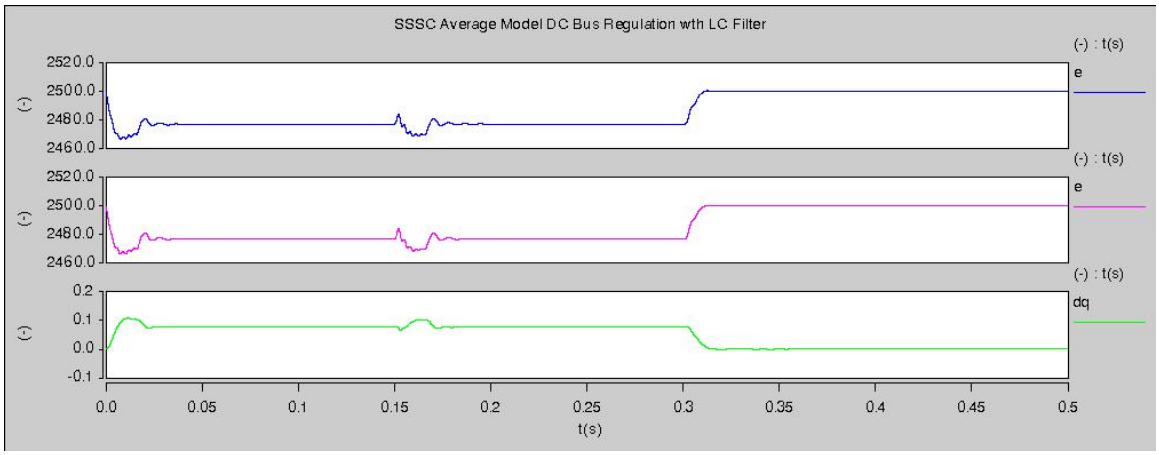


Figure 4.58 - SSSC Average Model DC-Bus Regulation with LC Filter.

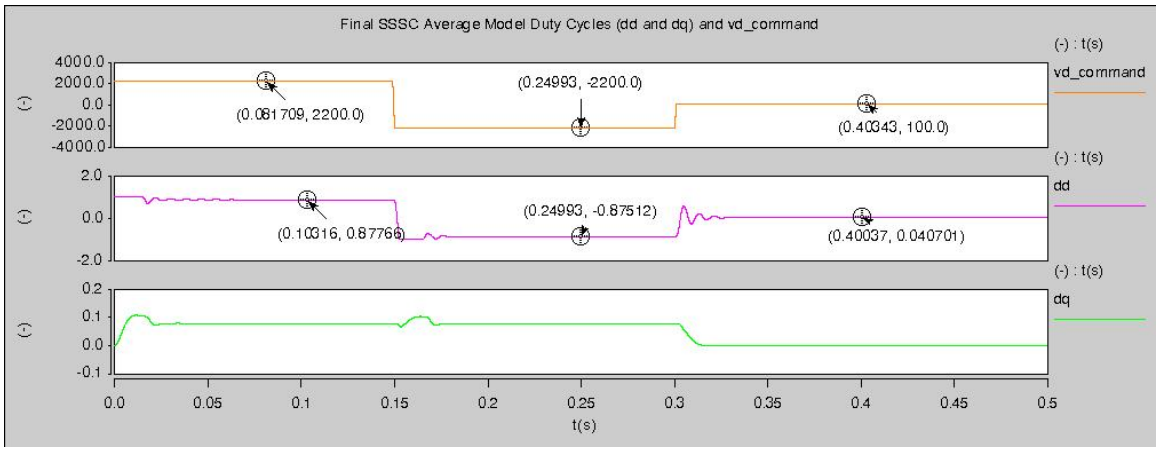


Figure 4.59 - SSSC Average Model Duty Cycles with LC Filter.

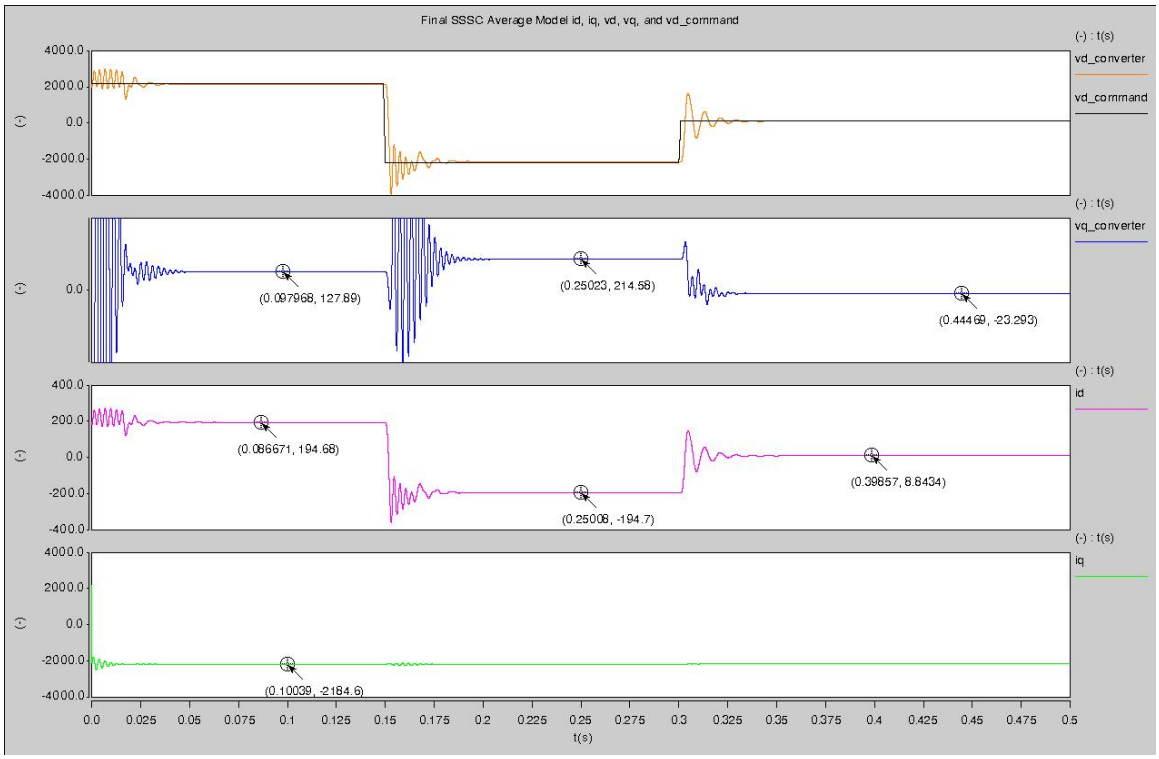


Figure 4.60- SSSC Average Model V_d Command verses System Parameters with RC Filter.

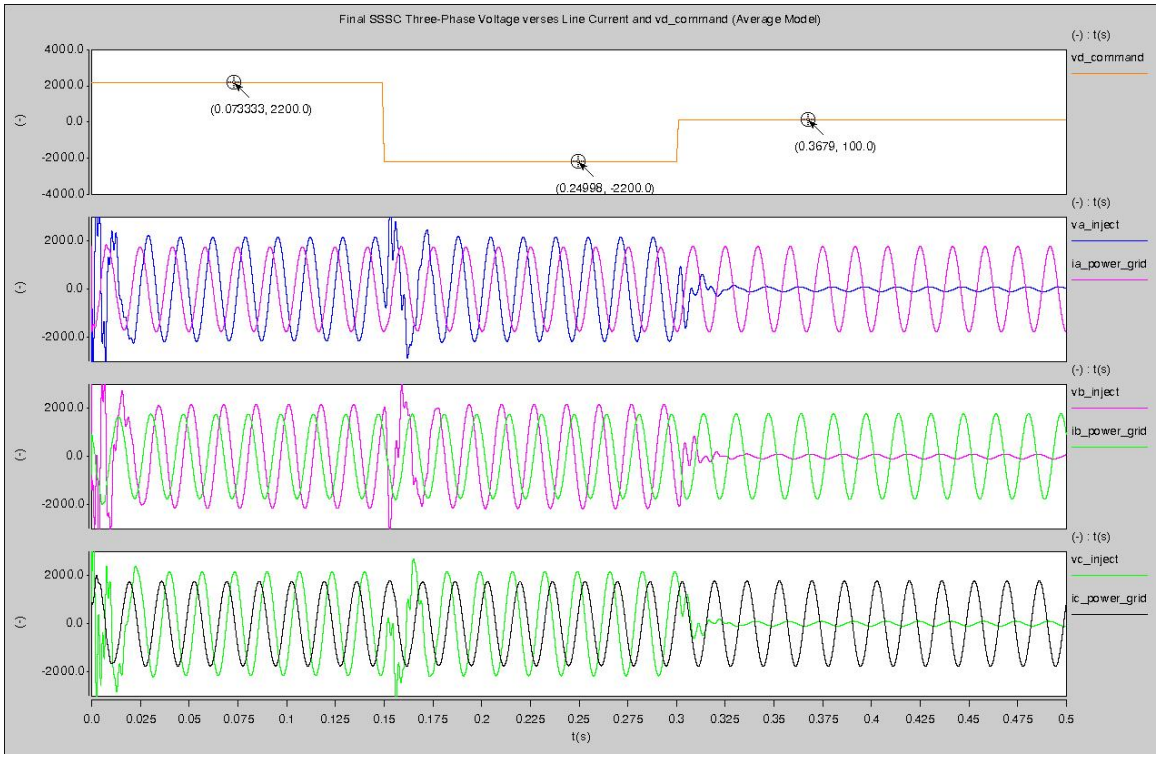


Figure 4.61- SSSC Average Model Simulation Results Over the Entire Operating Range.

R. Simulation Results of the Cascaded Three-Level SSSC with the Designed Controller

The simulation results from the switching model make one basic assumption. It is assumed that the DC-Bus is initially charged to 2500V. The simulation results show that there is a small amount of low frequency ripple contained in the output voltage waveforms. After consulting Dr. Boroyevich, the cause of this ripple is still unknown. The ripple does not effect the overall performance of the SSSC.

R1. Mode 1 (Capacitive Mode)

Initially, the SSSC begins its mode of operation in capacitive mode. At t = 100 ms, the SSSC is commanded to abruptly change its operation mode from full capacitive mode to full inductive mode by adjusting the V_d command from 2440 to -2440. Due to the assigned current direction during the modeling procedure, the output voltage lags the I_{Line} by 90° in the capacitive mode and leads the I_{Line} by 90° in the inductive mode. In mode 2, the simulation results verify that phase-A output voltage V_{a_inject}, lags I_{Line} by 90°. Figure 4.62 is used to illustrate capacitive mode of operation.

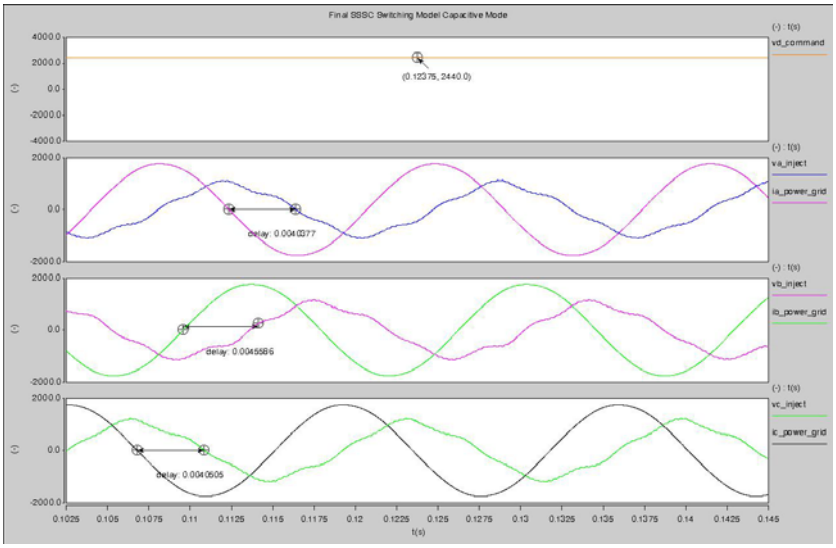


Figure 4.62 - SSSC Switching Model Simulation in Capacitive Mode with LC Filter.

Transition 2: from Mode 1 to Mode 2

At t = 100 ms, the SSSC is commanded from full capacitive mode to full inductive mode of operation. Figure 4.63 - shows the saber simulation waveform for Transition 2. This transition is the worst-case operation.

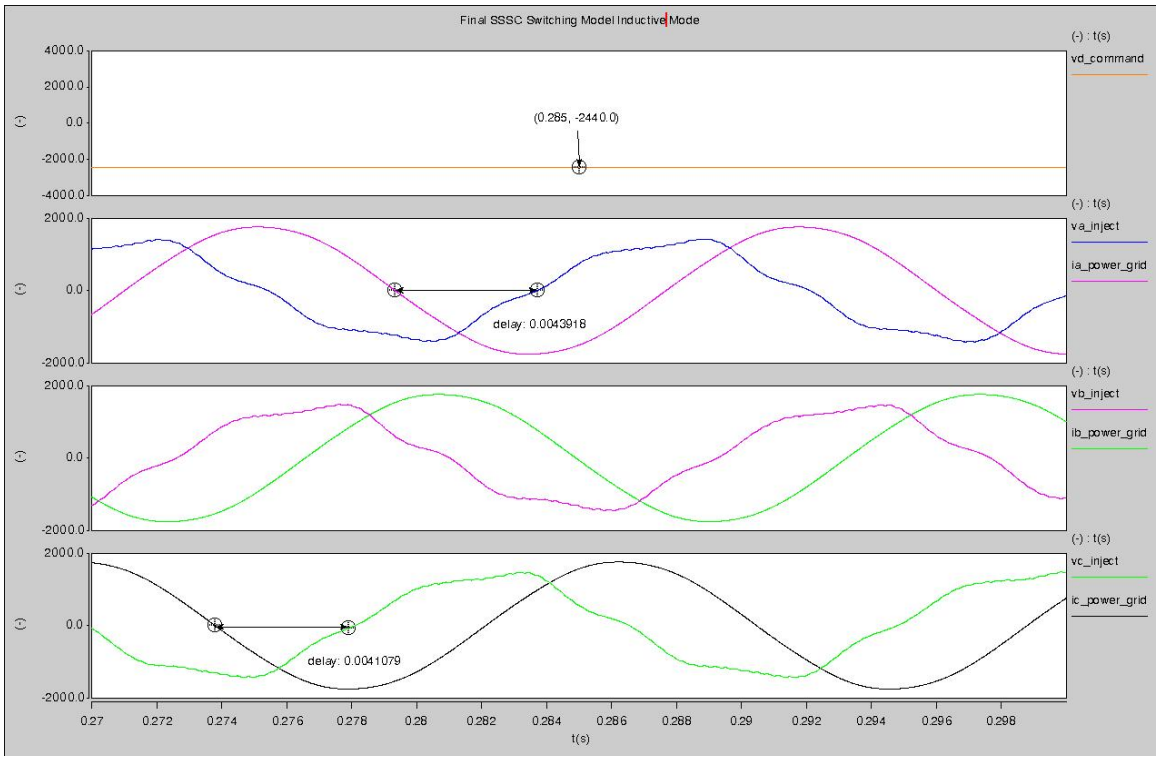


Figure 4.63 - SSSC Switching Model Simulation in Inductive Mode with LC Filter.

Transition 3: from Mode 2 to Mode 3

At t = 150 ms, the SSSC is commanded from full inductive mode of operation to standby mode of operation. During the standby mode of operation only a small amount of voltage is injected into the power system. This voltage can be neglected. The primary reason that there is a small amount of voltage injected into the power grid is due to the fact that the V_d command for standby mode is 100V. As stated above, there needs to be a small amount of voltage in the converter in order to generate enough converter current to

charge the DC-Bus capacitor. Figure 4.64 shows the Saber simulation waveform for Transition 3.

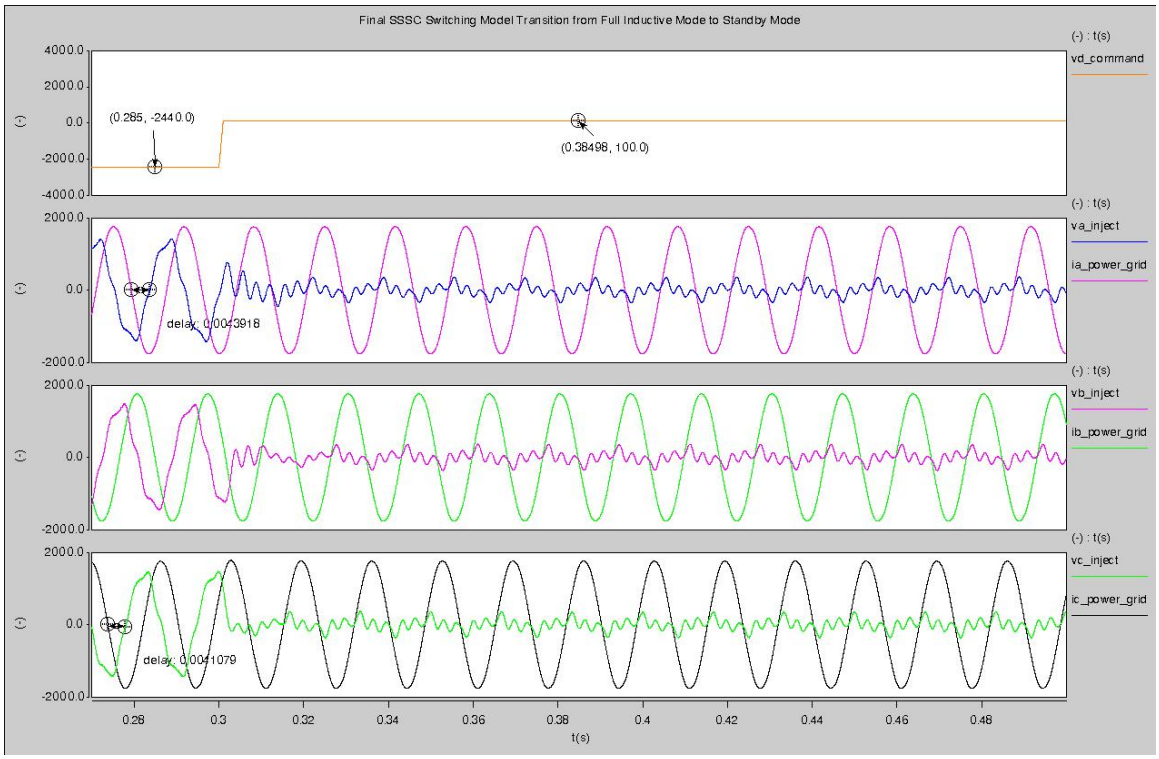


Figure 4.64 - SSSC Switching Model Transition from Inductive Mode to Standby Mode.

R2. Additional SSSC Switching Model Simulation Results

Figure 4.65 is used to show that the DC-Bus voltage is regulated within acceptable margins. Figure 4.66 illustrates the duty cycle response to the given command.

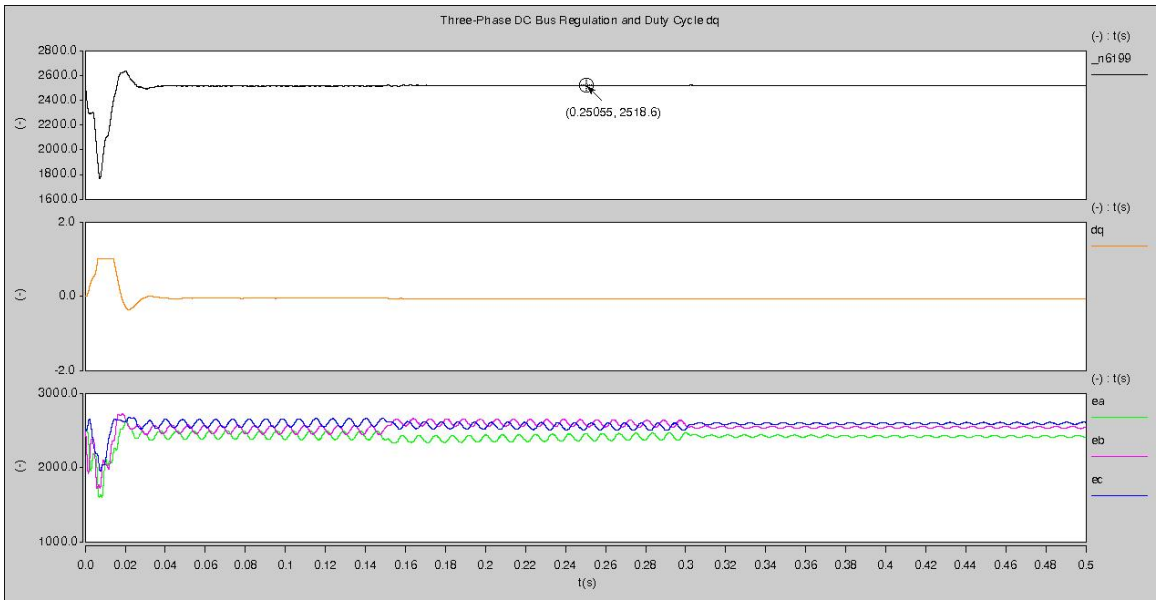


Figure 4.65 - SSSC Switching Model DC-Bus Regulation with LC Filter.

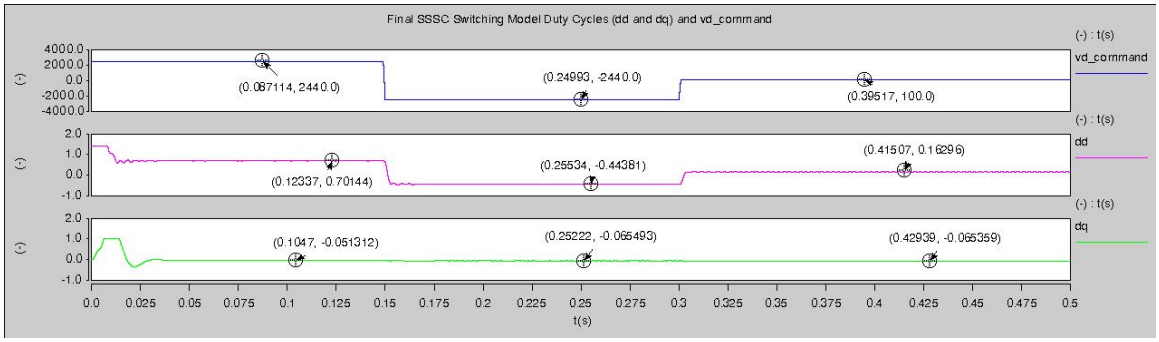


Figure 4.66 - SSSC Switching Model Duty Cycles with LC Filter.

The overall conclusion that can be drawn from the addition of an LC filter to the SSSC is that the behavior of both models is approximately the same. There are, however, several important differences. First, the duty cycle d_q and the V_q voltage are not considerably higher with the LC filter. This condition is due to the fact that the high losses associated with the resistor in the RC filter are eliminated. Due to this fact, the magnitudes of the injected voltages are within range that the design allows. For example, the magnitude of the injected voltage in the average mode is approaching 2500V, the design is for only 2440V peak amplitude. The LC filter performes according to its

design; meaning, the majority of the ripple voltage seen in the injected voltage waveform in Figure 4.39 has been eliminated. Figure 4.67 shows a close-up view of the ripple voltage associated with the three-phase injected voltage with an LC filter.

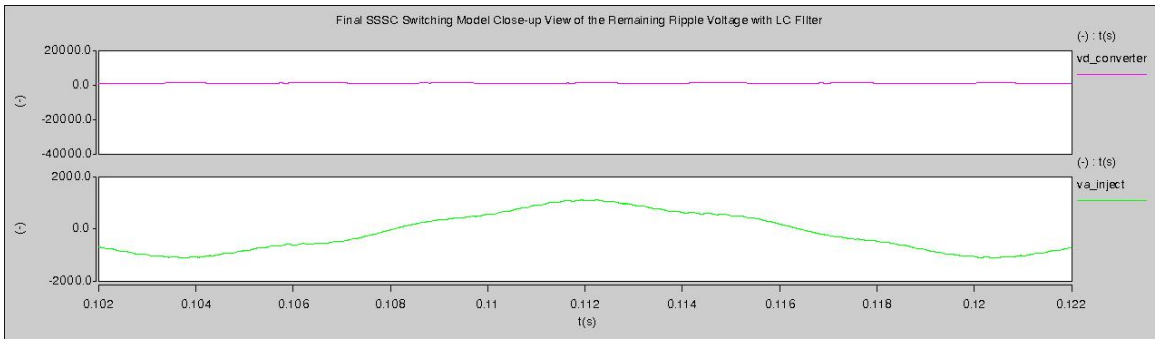


Figure 4.67- Close-up View of the SSSC Switching Model Injected Voltage Ripple with LC Filter.

Figure 4.68 shows the THD plot obtained from Saber.

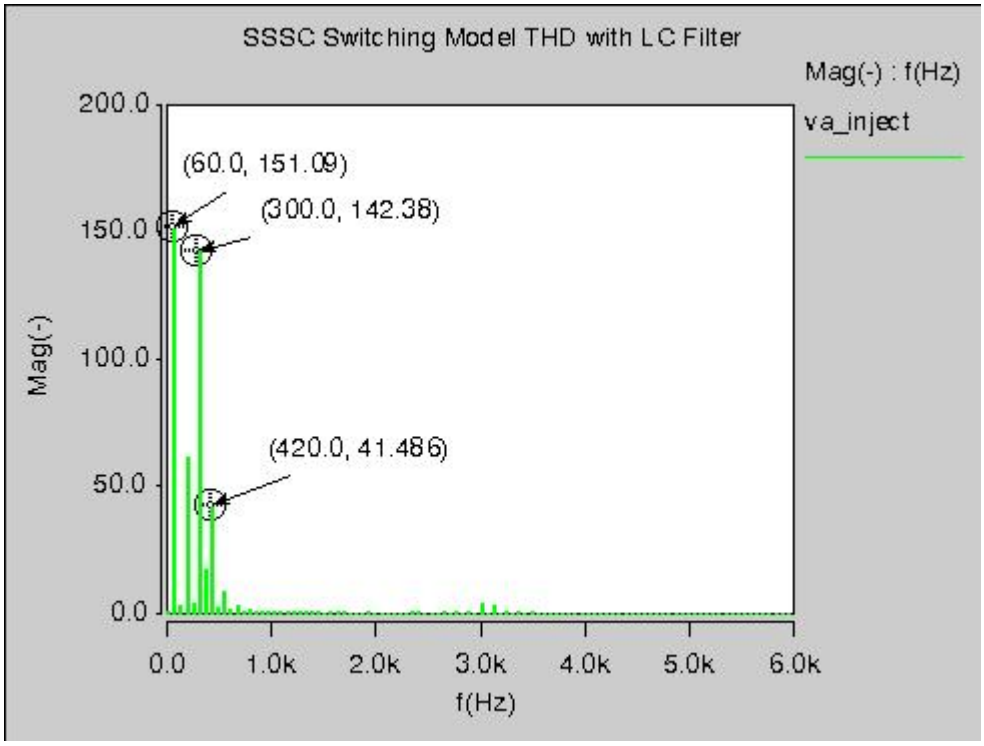


Figure 4.68 - SSSC Switching Model THD Plot with LC Filter.

According to Figure 4.68, the majority of the harmonics are located at the fundamental frequency of 60 Hz and the 6^{th} Harmonic or 360 Hz. The THD of the phase A injected voltage is now 1.04% compared to 26.38% with no filter added. The objective of the filter design for the SSSC is to remove the majority of the switching ripple voltage and the objective is met.

The simulation results for the case where a LC filter was added to the SSSC compare well with the simulation result for the SSSC with no added filter, therefore, it can be concluded that the design of the CMC-Based SSSC is finished. The next step is to perform a more detailed comparison between the final average and switching model for the SSSC and summarize the results.

4.6 Comparison of Simulation Results of the Average and Electrical Models

Before the SSSC average model results can be compared with the switching model results the overall design needs to be summarized. The next two sections of this chapter will be used to summarize the SSSC design.

Figure 4.69 illustrates the single line diagram of the SSSC including the LC Filter. If Figure 4.23 and Figure 4.31 are analyzed it can be seen that these figures for the schematic of the SSSC average model and the SSSC switching model include the LC filter.

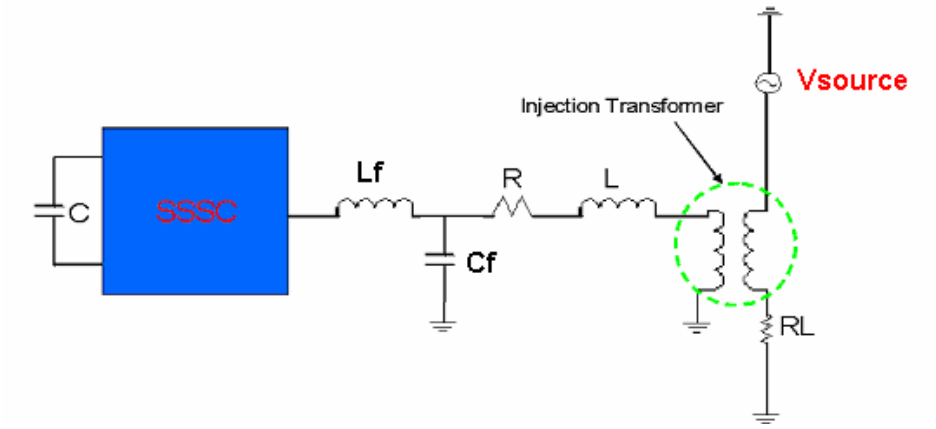


Figure 4.69 - Complete Single-Line Diagram of the SSSC including LC Filter.

S. *Verifying the accuracy of the Average and Switching Models*

To verify the accuracy of the average model and the performance of the proposed control system, a set of simulations, which uses the SSSC power electronics model as the reference, is performed. In the first simulation, the SSSC is commanded to abruptly transition from the full capacitive mode to the full inductive mode, and its simulation results are shown in Figure 4.70. The first simulation is for the worst-case operation in which the SSSC is controlled to respond to the step command from full capacitive to full

inductive modes Three major parameters are compared between the results from the average model and those from the electrical model: the D-channel output voltage, V_d; the average DC capacitor voltage, E_Average; and, the output voltage of phase A, V_{a_inject}. Due to the switching action in the electrical model, the switching ripple appears in the simulation results.

In this case, the Saber simulation results show that there is no voltage overshoot and that the average model and the switching model results match exactly. The settling time is approximately 13.5 ms. Figure 4.71reveals the Saber simulation results for the DC-Bus voltage E verses E_Average. Figure 4.72 illustrates that by neglecting the switching ripple, the dynamic response of the Phase-A output voltage is represented well by the average output voltage of Phase-A. The Phase-A injected voltage for the average model is slightly larger than the Phase-A injected voltage for the switching model. This is due to the fact that there is a slight gain discrepancy between the two models. Also, there are some additional losses present in the switching model compared to the average model due to the large discharge resistor used in the switching model for the DC-Bus.

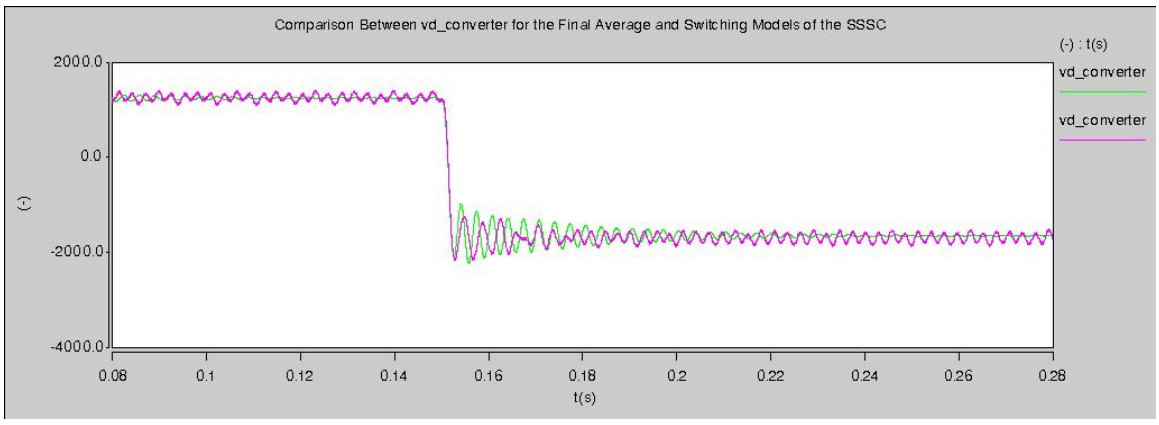


Figure 4.70 - Comparison of Vd_converter for the Average and Switching Models of the SSSC.

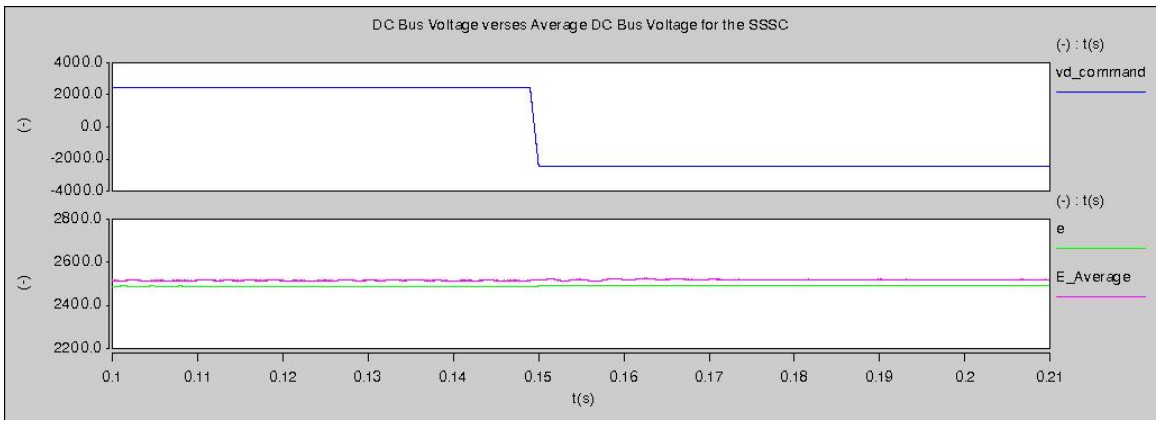


Figure 4.71 - Comparison of E and E_Average for the Average and Switching Models of the SSSC.

The next sets of simulation waveforms for the SSSC illustrate the transition from full inductive mode to standby mode. Figure 4.73 shows the abrupt change from full inductive mode to standby mode. In this case, the Saber simulation results reveal that there is no voltage overshoot and that the average model and the switching model results match exactly. The settling time is approximately 13.5 ms. Figure 4.74 shows the Saber simulation results for the DC-Bus voltage E verses E_Average. Figure 4.75 illustrates that by neglecting the switching ripple, the dynamic response of the Phase-A output voltage is represented well by the average output voltage of Phase-A.

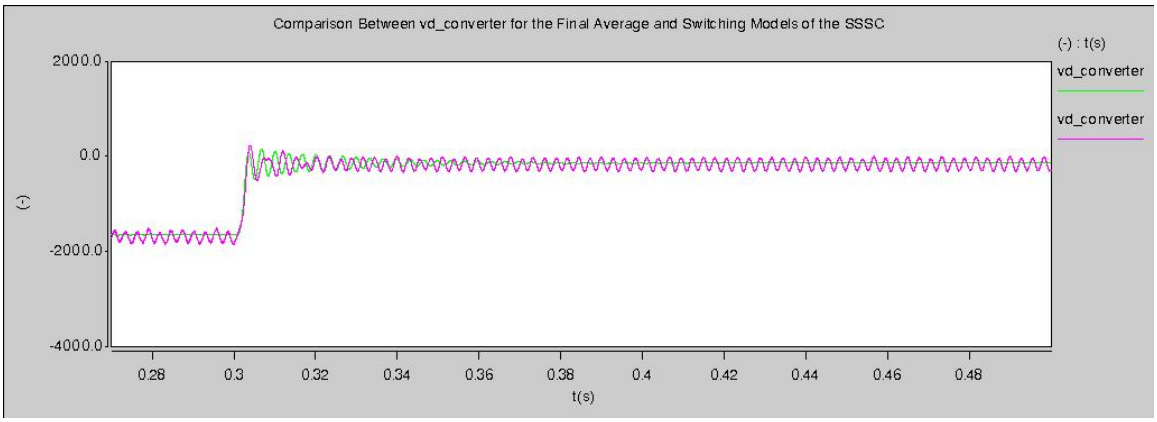


Figure 4.72 - Comparison of Vd_converter for the Average and Switching Models of the SSSC.

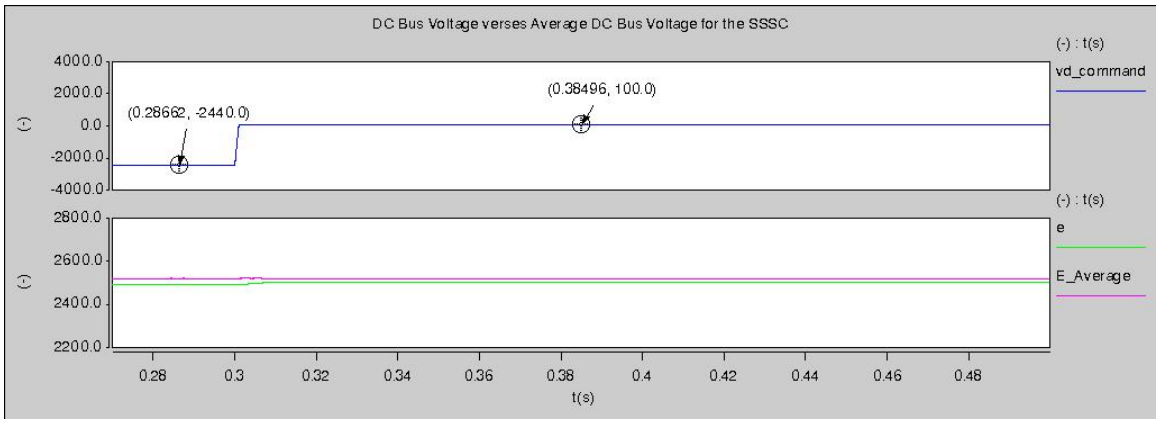


Figure 4.73 - Comparison of E and E_Average for the Average and Switching Models of the SSSC.

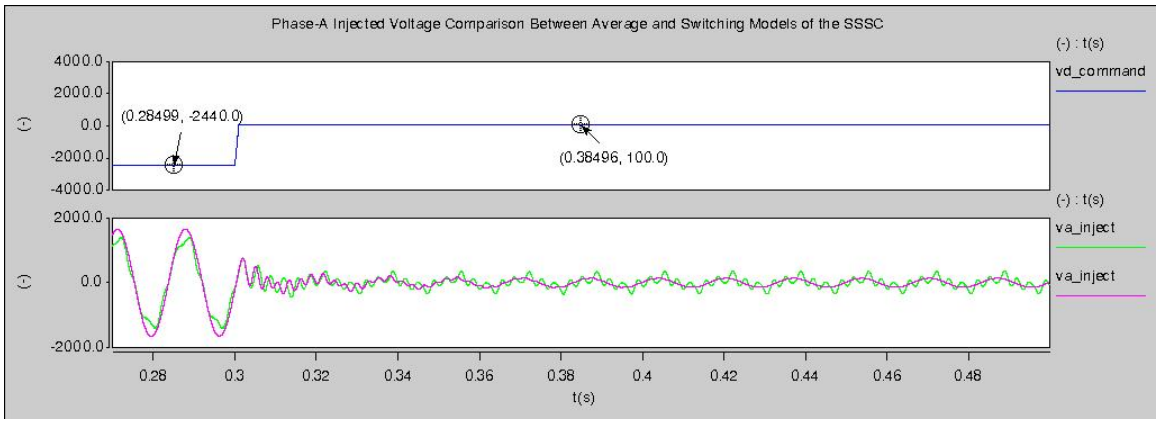


Figure 4.74 - Comparison of Phase-A Injected Voltage for the Average and Switching Models of the SSSC.

In conclusion, the results indicate that the proposed average model is accurate and can closely predict the dynamic behaviors of the three-level cascaded-based SSSC.

4.7 Simulation Results of the Electrical Model with the Proposed Controller

To further verify the stability and performance of the proposed SSSC controller, more continuous operation modes are simulated. The SSSC is commanded to operate in the following seven modes:

1. at time 0 to 39.9 ms, the SSSC operates in full capacitive mode, V_d = +2440 V, and Va_inject = +1725 V_{RMS},
2. at time 40 ms to 99 ms, the SSSC operates in full inductive mode, V_d = -2440 V, and Va_inject = -1725 V_{RMS},
3. at time 100 ms to 139.9 ms, the SSSC operates in standby mode, V_d = +100 V and Va_inject = +70.7 V_{RMS},
4. at time 140 ms to 159.9 ms, the SSSC operates in full capacitive mode, V_d = +2440 V, and Va_inject = +1725 V_{RMS},
5. at time 160 ms to 179.9 ms, the the SSSC operates in standby mode, V_d = +100 V and Va_inject = +70.7 $V_{RMS,}$
6. at time 180 ms to 189.9, the SSSC operates in full inductive mode, V_d = -2440 V, and Va_inject = -1725 $V_{RMS.}$ And
7. at time 190 ms to 210 ms, the SSSC finally operates in shutdown mode, V_d = 0 V and Va_inject = 0 V_{RMS}.

The simulation results of the SSSC operating in these seven modes are illustrated in Figure 4.75. As shown, the SSSC is stable for the entire range. In general, the D-Channel output voltage, V_d, closely follows its command. The average DC voltage is also regulated with slight unbalances. Five transitions occur in this simulation. Detailed simulation results are discussed and verified.

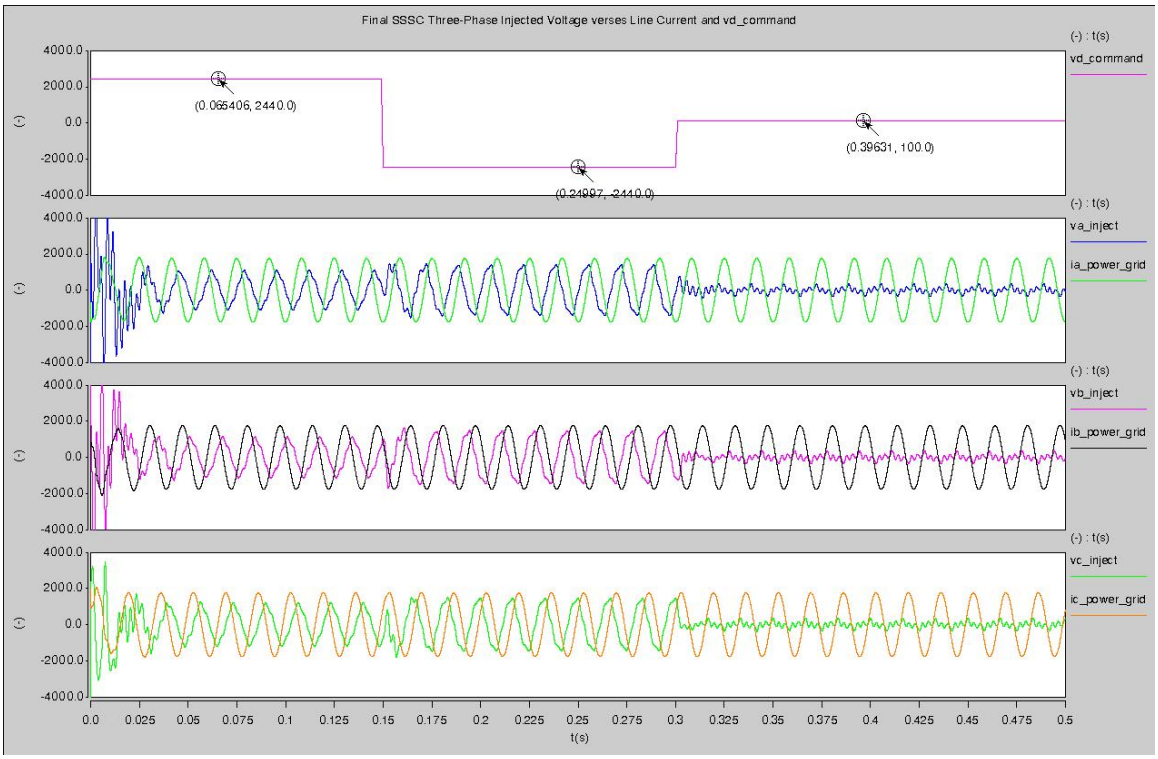


Figure 4.75 - SSSC Switching Model Results Over the Entire Operating Range.

The details from each transition from full capacitive mode to full inductive mode and then to standby mode have been detailed above. The remaining waveforms shown are used to illustrate the behavior of the SSSC over the entire operating range

Figure 4.76 shows the three-phase line-to-line switching voltage waveforms at the output of each phase of the CMC-Based SSSC Converter.

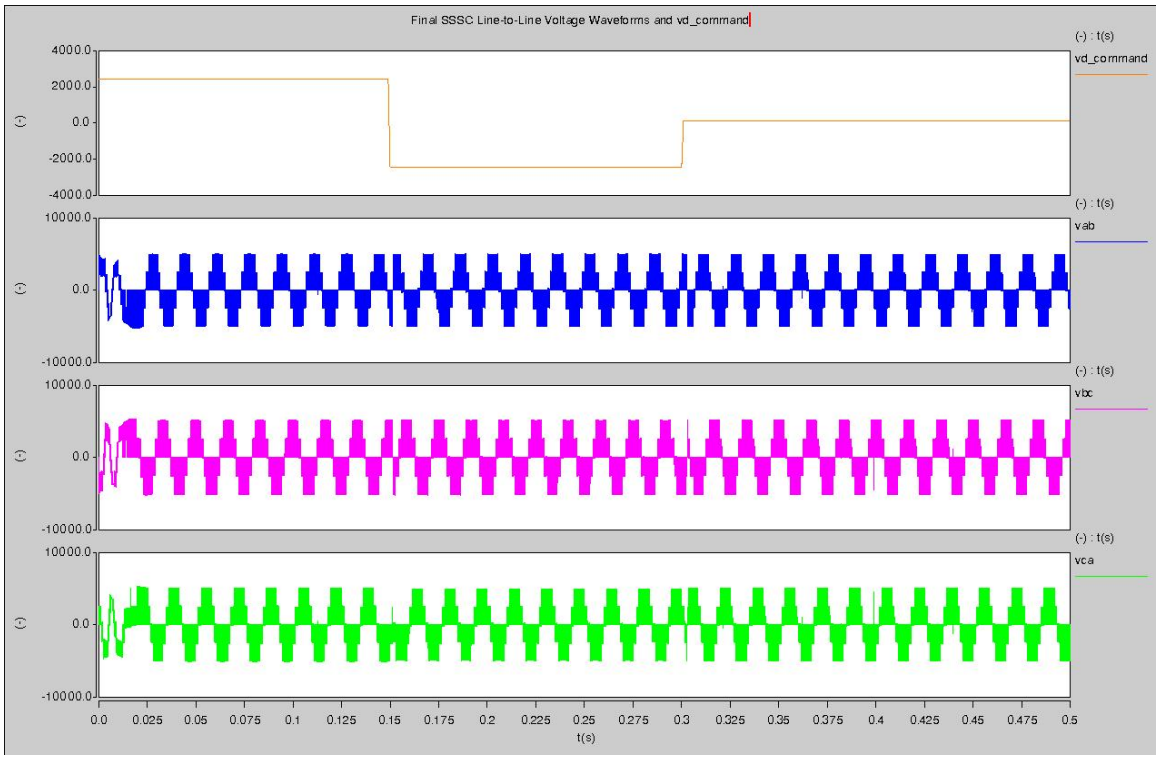


Figure 4.76 - SSSC Line-to-Line Switching Voltage Waveforms.

4.8 Summary

Chapter 4 has presented a detailed design process for the closed-loop controller design of the CMC-Based SSSC. The open-loop transfer function of the SSSC were derived as well as plotted in MatLab. The effects that the addition of a passive filter has on the closed-loop controller design were presented. A detailed comparison of the average model for the SSSC verses the switching model for the SSSC was conducted and the results outline. It can also be concluded that the compensators designed for the SSSC function well. Figure 4.78 obtained from the Average Model of the SSSC, is used to illustrate this robustness of the designed controllers. In Figure 4.77, the DC Bus is initially zero volts. At time t = 0.15 ms an E_Command is given to the SSSC to begin charging the DC Bus. The DC Bus charges to 2500 V and begins to operate in inductive mode. Therefore, the conclusion can be made that both control loops work well.

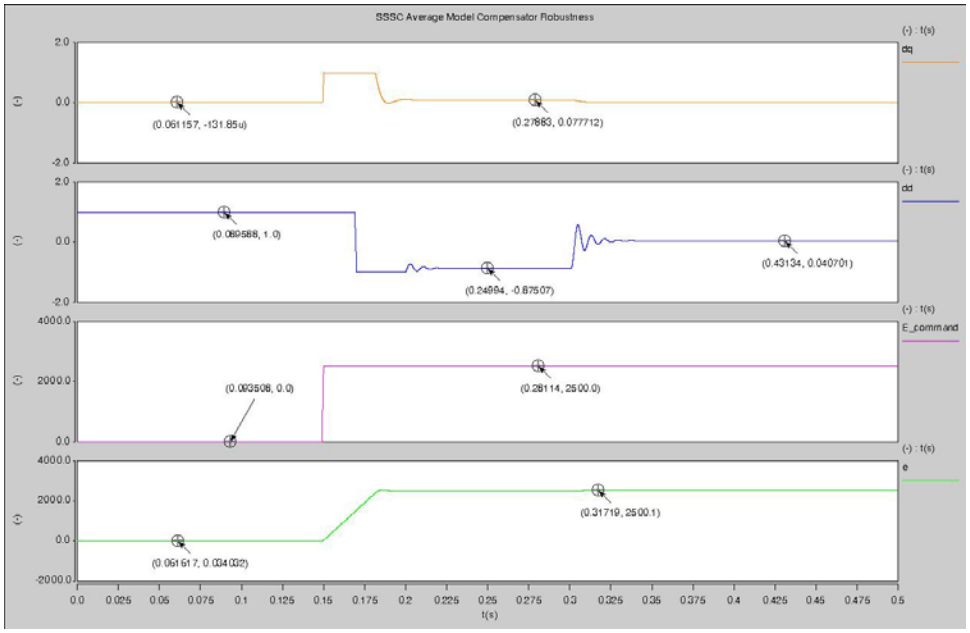


Figure 4.77 – SSSC Controller Stability Test

Table 4.8 summarizes the final SSSC design parameters.

TABLE 4.8 - FINAL SSSC SPECIFICATION OF THE STUDIED SYSTEM.

Power System Specification	
Source Voltage	13.8 kV
Line Current	1250 A r.m,s
Voltage Source Converter Rating	
Main Switch	4.5kV/4.0kA ETO
DC Bus Voltage	2500 V
DC Bus Capacitor	9.6 mF/phase
Converter Output Current	1250 A r.m.s
Switching Frequency	1.5 kHz
Coupling Transformer Impedance	300.1 μH
Coupling Transformer Loss Resistance	10.0 mΩ
Low-Pass Filter Capacitance	560 μF
Low-Pass Filter Inductance	400 μH
Reactance Compensating Range	10% - 15% of Line Impedance

Chapter 5 Conclusions and Future Work

5.1 Conclusions

Among FACTS controllers, the series controllers have promising characteristics in a wide range of problem-solving functions for transmission and distribution levels. A cost comparison between converter-based FACTS controllers and the fixed type series compensators has not been performed in this thesis. However, it is generally known that the primary cost disadvantage of the VSC-based compensators is the injection transformer. It is felt that if a converter-based SSSC could be designed without the use of a coupling transformer, the converter based SSSC would replace the fixed variable type series compensators. This is due to the fact that the converter based SSSC provides a wider range of compensation capability as well as performance compared to that of the fixed variable type series compensators.

For decades, it has been known that the transmitted power flowing through transmission lines could potentially be increased without adding any additional transmission infrastructures. The voltage traveling along the transmission line can be controlled using an appropriate amount of compensated reactive power. In addition, the series controller with the addition of energy storage can improve transient stability and can provide voltage support in the event that either a three-phase or a single-phase voltage sag occurs due to a fault condition.

As stated in the Introduction, the SSSC is a voltage source type series compensator and the TSSC, TCSC, and GCSC are variable impedance type series compensators. Both

types of compensators can provide effective power flow control, although their operating characteristics are different. The voltage-source converter-based SSSC offers capabilities and functional features that can not be obtained with the variable impedance type compensators. The variable impedance type compensators, on the other hand, make it easier to incorporate the necessary protection features required to handle fault conditions. This is due to the circuit structures of the power semiconductors used in the variable impedance type compensators.

The CMC-Based SSSC has the following advantages:

1. The SSSC can generate, internally, a controllable compensating voltage over an identical capacitive and inductive range independent of the magnitude of the line current.

2. The SSSC has the ability to interface with an external DC power supply in order to provide compensation of the line resistance by injecting real power. The SSSC also has the ability to inject reactive power into the power grid for the purposes of keeping the X/R ratio high. This is done independently of the amount of series compensation.

3. The SSSC with the addition of energy storage increases the effectiveness that the converter has to damp power oscillations. This is done by modulating the series reactance to increase or decrease the amount of transmitted power.

Using the turn-off-capability of the next generation of power semiconductor devices, switching power converters are now able to operate at higher switching frequencies and

to provide a faster response than before. This makes the VSC an important part in the FACTS controllers. The SSSC is the first power-converter-based series-connected controller. Instead of directly deriving reactive power from the energy-storage components, the SSSC circulates power with the connected network. Thus, the reactive components used for the SSSC are reduced.

For transmission and distribution voltage levels, the multilevel VSC offers various advantages over its counterparts. As discussed in Chapter 2, among the family of multilevel converter topologies, the CMC is the best alternative for the SSSC application. To achieve the same number of output voltage levels, the CMC requires the least total number of components. With its modular structure, the CMC can flexibly expand the output power capability that corresponds to the requirements of the connected power system networks [G4]. In addition, a modular design is favorable to manufacturing. If a modular design is used, it will allow for redundancy to be easily applied in the CMC to enhance reliability for the entire system. A complete control system for SSSC applications consists of two main parts: external and internal controls. Generally, the external control depends on the characteristics of the power system network to which the SSSC is connected. In contrast, the internal control primarily depends on the VSC topologies. This thesis focuses on the internal control for the SSSC using the CMC-Based topology. There are two major challenges that have made this research area very attractive.

First, a well-defined model is needed in order to improve the effectiveness and stability of feedback control and for system parameter optimization. There are numerous

parameters that must be controlled making the modeling of the CMC-based SSSC modeling difficult. Until [G4, I1], none of the previous work presented a valid model. As a result, the feedback-control parameters were randomly selected. The second challenge is how to design the converter output voltage filter in such a way as to minimize its effect of the closed-loop control and ultimately the stability of the SSSC. It has been shown that the filter has a large impact on the closed-loop controller design. The effect for the CMC-Based SSSC is mainly seen in the Q-Channel. The Q-Channel is used to regulate and balance the DC-Bus voltage. Voltages across this DC-Bus must be balanced to avoid over-voltage on any particular phase-lag. Not only do these unbalanced DC voltages introduce voltage stress on the semiconductor switches, but they also lower the quality of the synthesized output waveforms of the converter. Consequently, how to choose the filter components in order to maintain and balance the DC-Bus voltage with a straightforward and cost-effective technique is the second challenge for this topology.

The concept of the high-power electronic building block, which becomes a basic unit of the CMC topology, is presented in Chapter 2. Because of their identical layouts, the HBBBs are simple to manufacture and very cost-effective. Their modularity feature makes the entire system design and planning processes flexible in terms of power capability. If these modules are connected in series, the CMC topology that is used as the power converter in the SSSC application can increase the overall compensation capability of the entire system. The reactive component requirement criteria for the reactive power compensations have been investigated. Four main passive components that are included in this study are the DC capacitors, coupling transformer, filter inductor, and filter

capacitor. For a given operating voltage, the size of the DC capacitor used in the HBBB for reactive power compensation should be selected based on the following considerations. According to [G4], one of the factors limiting the minimum capacitance is over-voltage, which is a function of the voltage ripple and the transient voltage overshoot. In the H-bridge VSC, the voltage ripple is directly proportional to the maximum modulation index of the HBBB. Cost is the only factor that limits the maximum size of the capacitor. For a given operating voltage, the size of the coupling transformer is minimally limited by the maximum power system rating and by the cost. The filter inductor and filter capacitor are chosen based on the desired amount of harmonics to be removed from the output voltage waveform. There is a limited operating window to choose the values for the capacitor and inductor due to the fact that the bandwidth is limited between 60 Hz and 1.5 kHz. The overall rule for determining the size of the filter components is to try and design the cut-off frequency of the filter as small as possible (i.e. around 300 Hz) while at the same time maintaining the value for the components within standard and practical values. In other words, do not choose values that are too large for the filter components.

The proposed model, which can be used in all applications, is generally suitable for the CMC topology with any number of voltage levels. An accurate and simple modeling technique for the CMC-based SSSC in both stationary (ABC coordinates) and synchronous (DQ0 coordinates) frames has been presented. All key system transfer functions, which will be used in the control design process, have been verified. Based on the verified transfer functions, basic electrical characteristics of the CMC-based SSSC

have been investigated. In addition, the DQ0 model of the CMC-based SSSC enhances the feasibility of the proposed decoupling power control technique in which real and reactive power channels can be controlled separately.

Based on the proposed SSSC model, the feedback-control technique, called the decoupling power control, is presented for the three-level CMC-Based SSSC, and its performance and stability are verified using computer simulations. This control technique allows reactive and real power to be independently controlled.

5.2 Future Work

This thesis has covered some of the interesting issues and challenges of the CMC-based SSSC, additional work has been left for future research. The future work is summarized in the following list.

1. Detailed study of the effect that the output voltage filter has on closed-loop controller design. This thesis has established that the type of filter used and the filter parameters chosen has a substantial impact on the overall stability of the controller. A detailed study of the type of filter chosen as well as a detailed filter parameter optimization procedure is needed. It can be stated that the choice of filter components has a direct effect on determining if the DC-Bus voltage is balanced or not. Once the full impact that the output voltage filter has on the SSSC is known the filter parameters can be selected in such a way as to achieve maximum performance and reliability of the CMC-Based SSSC.

2. Study the start-up and shut-down criteria for the CMC-Based SSSC. In most cases for series compensation a "crowbar" is used to separate the converter from the power grid. In other words, the "crowbar" is used to connect or disconnect the converter from the power system. This device is also used to during the start-up and shut-down process for the converter. For example, if the "crowbar" is used as by-pass switch, the transformer can be shorted during start-up. Once the DC-Bus voltage is charged to its nominal value and the converter current is approximately equal to the power grid current, the by-

pass can be opened allowing the SSSC to be connected to the power grid. The exact functionality of the "crowbar" needs to be researched so an accurate start-up and shut-down procedure for the SSSC can be designed and implemented.

3. Study the effect that increasing the number of voltage levels contained in the converter output voltage waveform has on series compensator so that the SSSC can be operated without a transformer. As stated earlier, the transformer is the major cost disadvantage to the converter-based series compensators. The primary function of the transformer is to provide electrical isolation between the converter and the power grid. The secondary function of the transformer is to provide a voltage boost to the converter output voltage waveform to increase the level of series compensator. The main question, therefore, is how to achieve the necessary amount of electrical isolation for a series connection without a transformer. In the end it would be advantageous to remove the transformer from the system.

4. Study the effect of adding energy storage to the SSSC to result in a DVR. A DVR is essentially a SSSC with energy storage added. The addition of energy storage allows the SSSC to provide real power voltage support during a voltage sag condition caused by a fault.

5. Study the potential for combining the CMC-Based STATCOM proposed in [G4] with the CMD-Based SSSC to result in a UPFC.

Final CMC-Based SSSC Design Summary

Figure 5.1 and Figure 5.2 show the r.m.s values for the SSSC switching model. Figure 5.1 shows the simulation results for capacitive mode; whereas, Figure 5.2 shows the simulation results for inductive mode. The information contained in these figures is summarized in Table 5.1. Table 5.1 is used to illustrate the comparison between the design specification and the actual SSSC simulation results.

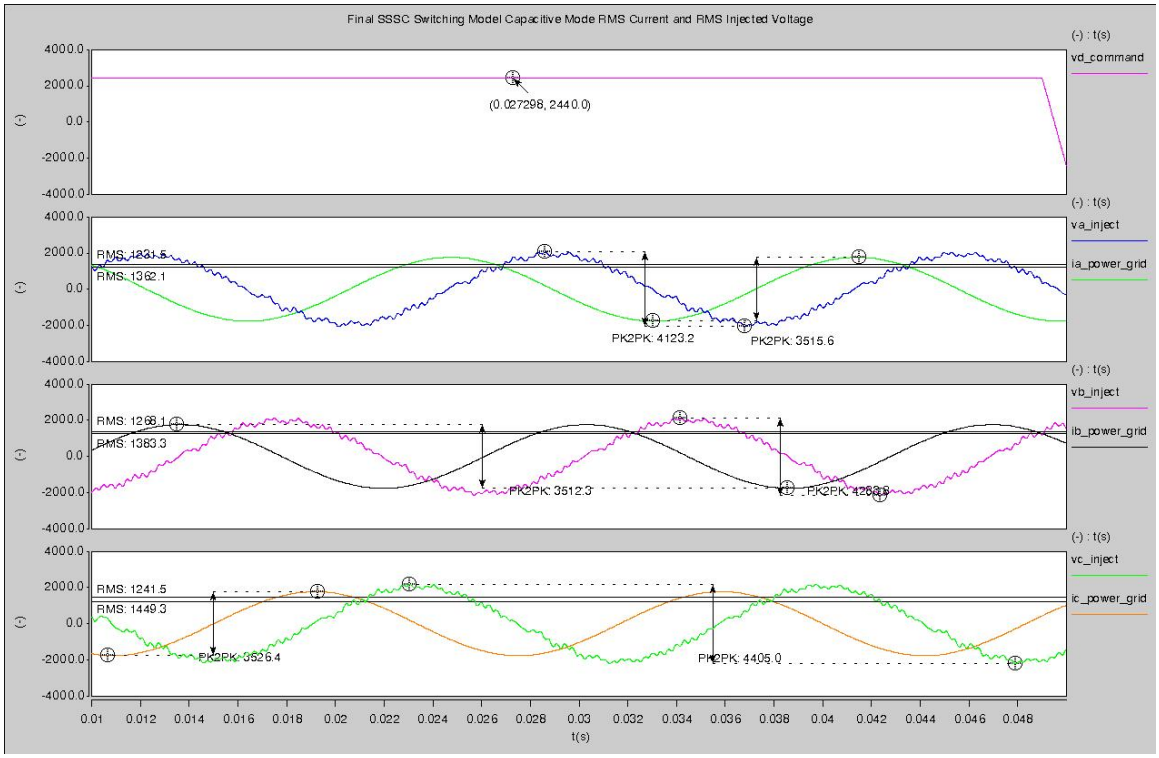


Figure 5.1 – R.M.S. Voltage and Current Waveforms for the SSSC Switching Model Operating in Capacitive Mode.

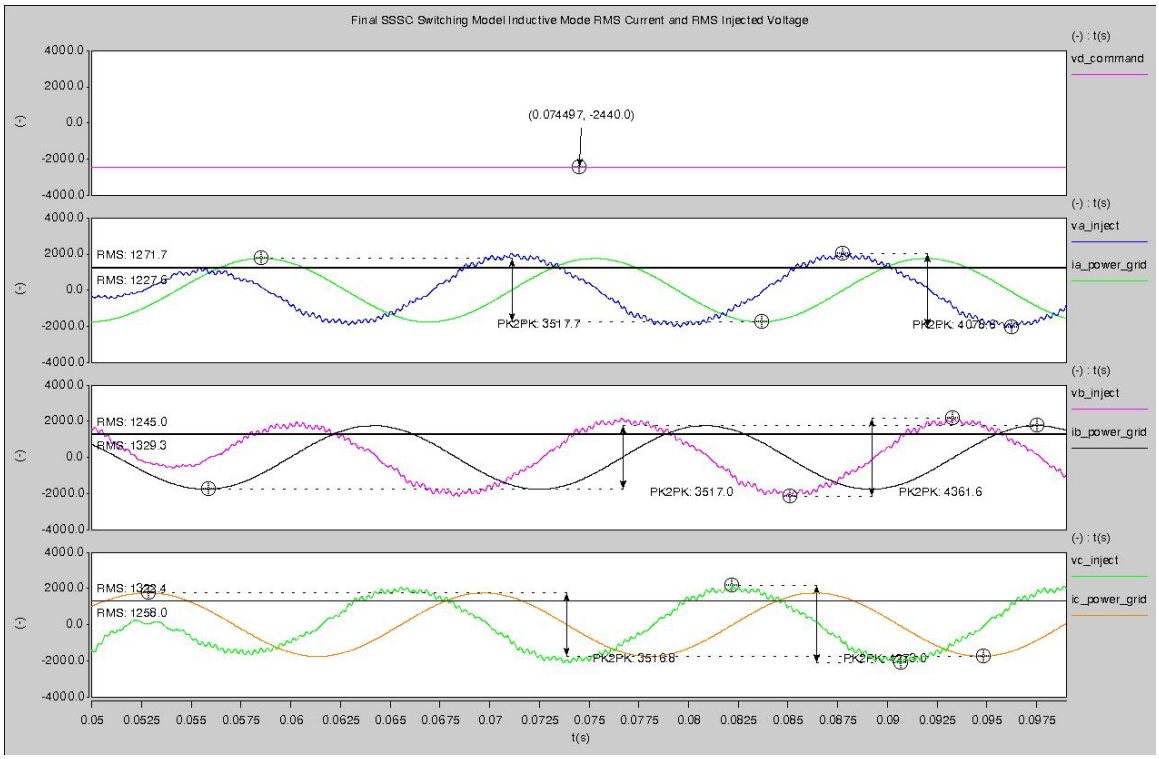


Figure 5.2 – R.M.S. Voltage and Current Waveforms for the SSSC Switching Model Operating in Inductive Mode.

TABLE 5.1 – COMPARISON BETWEEN THE PROPOSED SSSC DESIGN SPECIFICATION AND THE ACTUAL SIMULATION RESULTS.

Power System Specification	
Source Voltage	13.8 kV
Line Current	1250 A r.m,s
Voltage Source Converter Rating	
Main Switch	4.5kV/4.0kA ETO
DC Bus Voltage	2500 V
DC Bus Capacitor	9.6 mF/phase
Converter Output Voltage	1803 V r.m.s
Converter Output Current	1250 A r.m.s
Switching Frequency	1.5 kHz
Coupling Transformer Impedance	300.1 μH
Coupling Transformer Loss Resistance	10.0 mΩ
Low-Pass Filter Capacitance	1200 μF
Low-Pass Filter Inductance	30.0 μH
Reactance Compensating Range	10% - 15% of Line Impedance
Voltage Source Converter Output	**Capacitive Mode**
Phase A r.m.s. Output Voltage	1457 V r.m.s
Phase B r.m.s. Output Voltage	1513 V r.m.s
Phase C r.m.s. Output Voltage	1557 V r.m.s
Phase A r.m.s. Line Current	1243 A r.m.s
Phase B r.m.s. Line Current	1242 A r.m.s
Phase C r.m.s. Line Current	1247 A r.m.s
Reactance Compensation Range	Approximately 11.28 %
	Inductive Mode
Phase A r.m.s. Output Voltage	1442 V r.m.s
Phase A r.m.s. Output Voltage	1542 V r.m.s
Phase A r.m.s. Output Voltage	1497 V r.m.s
Phase A r.m.s. Line Current	1244 A r.m.s
Phase B r.m.s. Line Current	1243 A r.m.s
Phase C r.m.s. Line Current	1243 A r.m.s
Reactance Compensation Range	Approximately 11.17%

Appendix A – SSSC Parameter Definition

Based on the 4.5kV/4kA Emitter Turn Off (ETO) Thyristor capacity, the device voltage and rms current are limited at 2800 V and 1500 A, respectively.

Then voltage rating of the dc capacitors is selected for 2.5 kV.
Let, the operating dc bus be

$Vdc := 2500 \quad V$

Assume the converter modulated by well-PWM (SPWM,SVM), thus the maximum modulation index (M) is 1.
In general, the higher M, the lower output THD. We thus prefer to operate the converter in the range of 0.6 to 1. Then, we chose the standby mode M of 0.8.

$M := 0.8$

And the max M and min M are

$M_{max} := 0.9 \qquad M_{min} := 0.7$

By these statement, the normal peak Injected Voltage is

$Vinj\_peak := Vdc \cdot M \qquad Vinj\_peak = 2 \times 10^3 \quad V$

Then, output RMS Injected Voltage is

$$Vinj\_phase := \frac{Vinj\_peak}{\sqrt{2}} \qquad Vinj\_phase = 1.4 \times 10^3 \quad V$$

And line-to-line Injected Voltage is

$Vinj\_line := \sqrt{3} \cdot Vinj\_phase \qquad Vinj\_line = 2.4 \times 10^3 \quad V$

Based on the power stage design, the rated output RMS current is

$Io := 1250 \quad kArms$

Therefore, the maximum Var compensation per phase is

$Q_{max} := Vinj\_phase \cdot Io \qquad Q_{max} = 1.8 \times 10^6 \quad Var$

Therefore,

$Vo\_max := M_{max} \cdot Vdc \qquad Vo\_max = 2.3 \times 10^3 \quad V$

$Vo\_min := M_{min} \cdot Vdc \qquad Vo\_min = 1.8 \times 10^3 \quad V$

DC capacitor design:

From the system parameter,

$$\Delta Vdc := 0.10 \cdot Vdc \qquad f := 60 \qquad T := \frac{1}{f} \qquad f_s := 1500$$

Then, the dc capacitance can be calculated as follows:

$$Cdc := \frac{\int_0^{\frac{T}{4}} \sqrt{2} \cdot Io \cdot \cos(2 \cdot \pi \cdot f \cdot t)\, dt}{\Delta Vdc} \cdot \frac{1}{\left(2 - \frac{f}{f_s}\right)}$$

$$Cdc = 9.6 \times 10^{-3} \qquad F/phase$$

Therefore, the peak dc voltage appearing across the dc capacitor is

$$Vdc_{max} := Vdc + \frac{\Delta Vdc}{2} \qquad Vdc_{max} = 2.6 \times 10^{3} \qquad V$$

Then, the voltage margin for overshoot during transient is

$$Vdc_{margin} := 2800 - Vdc_{max} \qquad Vdc_{margin} = 175 \qquad V$$

or allowed percent overshoot of

$$\frac{Vdc_{margin}}{Vdc} \cdot 100 = 7 \qquad \%$$

Coupling Transformer design:

The coupling transformer is modeled as an equivalent inductance. If the assumption is made that a standard transformer for a 13.8kV system is used, then the equivalent inductance for the transformer is between 0.035 per-unit and 0.12 per-unit.

Assume that the per-unit base of the coupling transformer is 0.10 per-unit.

$KV_{rating} := 13.8 \cdot 10^{3}$ $X_{pu} := 0.10$ $MVA_{rating} := \sqrt{3.0} \cdot Io \cdot Vinj\_line$

$$Z_B := \frac{Vinj\_line^2}{MVA_{rating}} \qquad MVA_{rating} = 5.3 \times 10^{6}$$

$Z_B = 1.1$

$X_{base} := X_{pu} \cdot Z_B$

$X_{base} = 113.1 \times 10^{-3}$ $L_{eq\_pu\_trans} := \frac{X_{base}}{2 \cdot \pi \cdot f}$

Let the transformer equivalent impedance is

$L_{eq\_pu\_trans} = 300.1 \times 10^{-6}$

Lets assume that Rs is 10% of coupling transformer impedance

$$R_s := \frac{X_{base}}{10}$$

$$R_{s\_pu\_trans} := \frac{R_s}{Z_B} \qquad R_{s\_pu\_trans} = 10 \times 10^{-3}$$

Coupling inductor design:

The maximum output current is generated, when the maximum M or minimum M is applied.

$$X_s := \frac{\frac{Vo\_max}{\sqrt{2}} - Vinj\_phase}{Io} \qquad X_s = 141.4 \times 10^{-3} \quad \Omega$$

Then, the required coupling inductance is

$$L_s := \frac{X_s}{2 \cdot \pi \cdot f} \qquad L_s = 375.1 \times 10^{-6} \quad H$$

Let assume, Rs is 10% of coupling inductor impedance.

$$R_s := \frac{X_s}{10} \qquad R_s = 14.1 \times 10^{-3} \quad \Omega$$

Per Unit Calculation

Let RMS line output votlage of the converter at M = 1 be base voltage

$$V_{base} := Vinj\_line \qquad V_{base} = 2.4 \times 10^{3}$$

And rated RMS output current of the converter is base current

$$I_{base} := Io \qquad I_{base} = 1.3 \times 10^{3}$$

Therefore base power is

$$S_{base} := \frac{V_{base}}{\sqrt{3}} \cdot I_{base} \qquad S_{base} = 1.8 \times 10^{6}$$

And base impedance is

$$Z_{base} := \frac{V_{base}}{\sqrt{3} \cdot I_{base}} \qquad Z_{base} = 1.1$$

Appendix B– Parks Transformation Matrix Definition

The purpose of the Park's transformation is to transfer a parameter in ABC coordinates to a new coordinate system called DQ0. In the case of the SSSC the Q-Axis stands for direct, D-Axis stands by quadrature, and 0 stands for zero. The advantage of this DQ0 transformation is that, under a balance three-phase system, a three-phase AC parameter in ABC coordinate system is represented by a two-phase DC parameter in DQ0. Consequently, the classical control technique, which is valid only in DC space, is applied in the AC environment.

A coordinate in the ABC coordinates can be represented by a vector. The direction points from the origin to its coordinate. The output voltage of the SSSC, for example, is represented as the following 3x1 matrix:

$$\vec{V}_{abc}(t) = \begin{bmatrix} v_a(t) \\ v_b(t) \\ v_c(t) \end{bmatrix},$$

Equation B.1

where $v_a(t)$, $v_b(t)$ and $v_c(t)$ are phase A, phase B and phase C output voltages of a SSSC.

Figure B-1 shows the location of vector $\vec{v}_{abc}$ in the ABC coordinates.

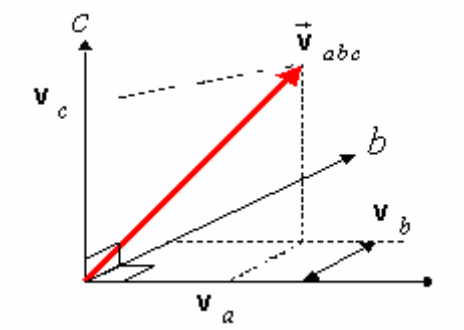


Figure B.1 - Vector $\vec{v}_{abc}$ represents an instantaneous output voltage of a SSSC.

The first step of the Park's transformation derivation begins with defining an intermediate coordinate system called $\alpha\beta\gamma$. The $\alpha\beta\gamma$ coordinates located in the ABC coordinate systems are shown in Figure B.2. The direction of the γ axis is in line with the vector (1,1,1) in the ABC coordinates.

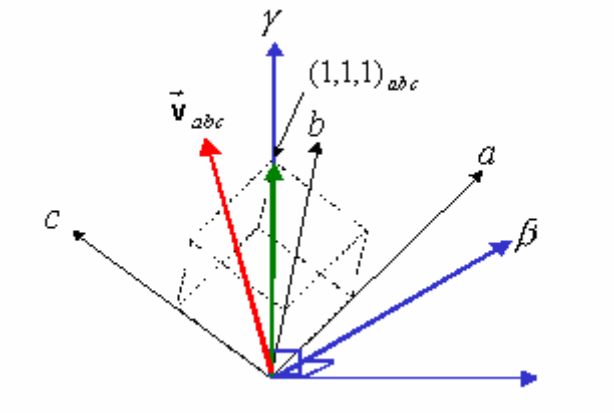


Figure B.2 - The $\alpha\beta\gamma$ coordinates located in the ABC coordinate system.

A vector in the ABC coordinates can be represented in the $\alpha\beta\gamma$ coordinates by applying the following equations:

$$\vec{v}_{\alpha\beta\gamma}(t) = \vec{T}_{\alpha\beta\gamma/abc} \cdot \vec{v}_{abc}(t),$$

Equation B.2

where

$$\vec{T}_{\alpha\beta\gamma/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix}$$

After the transformation, the components in γ-axis are always zero in the case of balanced-three-phase system. In other words, voltage vector $\vec{v}_{\alpha\beta\gamma}(t)$ is on the $\alpha\beta$ plane and rotates around the γ axis. As a result, a balanced-three-phase AC vector in the ABC coordinates can be represented by a two-phase AC vector in the $\alpha\beta\gamma$ coordinates. If the $\alpha\beta$ plane synchronously rotates along with vector $\vec{v}_{\alpha\beta\gamma}(t)$, $v_\alpha(t)$ and $v_\beta(t)$ then becomes constant. With this principle, the DQ0 coordinates is created. Figure B.3 illustrates vector $\vec{v}_{abc}$ in the DQ0 and $\alpha\beta\gamma$ coordinates. The D and Q axis rotates with the angular velocity of ω or $2\pi f$, f is the line frequency. Based on this approach, the Park's transformation matrix, $\vec{T}_{dq0/abc}$, is then derived to directly transform a vector from the ABC coordinate system to the DQ0 coordinate system. The transformation is shown in Equation B.3 and the Park's transformation matrix is shown in Equation B.4.

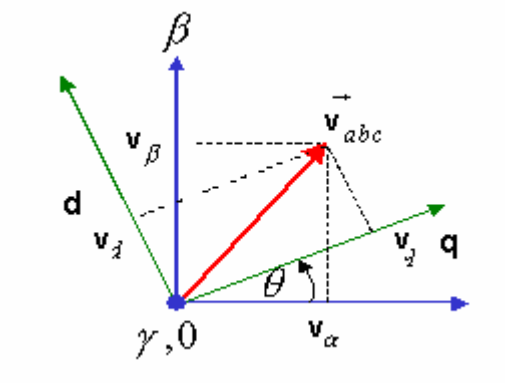


Figure B.3 - The rotating DQ0 coordinates with respect to the $\alpha\beta\gamma$ coordinates.

$$\vec{v}_{dq0} = \vec{T}_{dq0/abc} \cdot \vec{v}_{abc} .$$

Equation B.3

$$\vec{T}_{dq0/abc} = \sqrt{\frac{2}{3}} \begin{bmatrix} -\sin(\theta) & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \\ \cos(\theta) & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} & \frac{1}{\sqrt{2}} \end{bmatrix},$$

Equation B.4

where $\theta = \int_0^t \omega(\tau) d\tau + \theta(0)$.

The inverse Park's transformation matrix, as shown in **Error! Reference source not found.**, is used to convert a vector in the DQ0 coordinates back to the ABC coordinates.

$$\vec{v}_{abc} = \vec{T}^{-1}{}_{dq0/abc} \cdot \vec{v}_{dq0} .$$

Equation A.5

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