Scheduling of Wafer Test Processes in Semiconductor Manufacturing

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ABSTRACT

Scheduling is one of the most important issues in the planning of manufacturing systems. This research focuses on solving the test scheduling problem which arises in semiconductor manufacturing. Semiconductor wafer devices undergo a series of test processes conducted on computer-controlled test stations at various temperatures. A test process consists of both setup operations and processing operations on the test stations. The test operations occur in a specified order on the wafer devices, resulting in precedence constraints for the schedule. Furthermore, the assignment of the wafer devices to test stations and the sequence in which they are processed affects the time required to finish the test operations, resulting in sequence dependent setup times. The goal of this research is to develop a realistic model of the semiconductor wafer test scheduling problem and provide heuristics for scheduling the precedence constrained test operations with sequence dependent setup times.

A mathematical model is presented and two heuristics are developed to solve the scheduling problem with the objective of minimizing the makespan required to test all wafer devices on a set of test stations. The heuristic approaches generate a sorted list of wafer devices as a dispatching sequence and then schedule the wafer lots on test stations in order of appearance on the list.

An experimental analysis and two case studies are presented to validate the proposed solution approaches. In the two case studies, the heuristics are applied to actual data from a semiconductor manufacturing facility. The results of the heuristic approaches are compared to the actual schedule executed in the manufacturing facility. For both the case studies, the proposed solution approaches decreased the makespan by 23-45% compared to the makespan of actual schedule executed in the manufacturing facility. The solution approach developed in this research can be integrated with the planning software of a semiconductor manufacturing facility to improve productivity.

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CHAPTER I
INTRODUCTION

1.1 Overview of Semiconductor Manufacturing Process

Semiconductors are key components of many electronic products. As the prevalence and variety of electronic products increases, so do the requirements and complexity of semiconductor manufacturing. The worldwide revenues for semiconductor industry were about $204 billion in 2000. Although current industry trends suggest an 8% decrease in the worldwide market, analysts are predicting 20-25% growth for 2002 [26].

Semiconductor manufacturers produce many types of devices, such as computer chips and microprocessors, by etching thousands or even millions of transistors and other electronic components on several layers of the semiconductor wafers. Although the process of manufacturing these devices varies for different device types, the general process involves wafer manufacturing, wafer fabrication, and packaging and final test [30] [31]. The manufacturing process is summarized as follows:

- Wafer Manufacturing
    - Silicon polycrystalline growth
    - Wafer polishing
    - Epitaxy
- Wafer Fabrication
    - Photolithography
    - Etch and strip process
    - Diffusion, Implant, and Metallization
    - Chemical mechanical planarization (CMP)
- Packaging and Final Test
    - Wafer probe test
    - Packaging

- Final test

During wafer manufacturing, a seed silicon crystal is slowly pulled and grown into a silicon ingot. The ingot is sliced into wafers and one side of each wafer is polished to remove scratches and impurities. An ultra pure layer of silicon crystalline (*epi-layer)*, that is about 3% of the wafer thickness, is then grown on the wafer through an epitaxial process. This *epi-layer* provides a contaminant free substrate for constructing transistors.

In the wafer fabrication processes, the transistors are constructed and connected to build a circuit. To construct the transistors, the wafer with an *epi-layer* is first exposed to high temperature to grow an oxide layer (SiO_2) as a dielectric layer. Then the wafer is coated with photo-resistant material. A lithography process exposes light through a mask pattern on the photo-resistant material. The light hardens the exposed portions of the photo-resistant, and the unhardened photo-resistant is washed away. An etching process is used to remove the oxide (SiO_2) where photo-resistant is absent, leaving the hardened oxide pattern on the wafer. Then a diffusion and implant process is used to deposit dopant and ion to exposed silicon while the silicon oxide acts as a barrier in the other regions, to create regions with different conductivity of silicon semiconductor material. These lithography and diffusion and implant processes are repeated several times to build transistors on the wafers. Then a layer of aluminum or copper is deposited on the wafers in a metallization process. Excess aluminum (copper) on the wafer is etched away by another lithography process to provide desired interconnectivity. Another layer of dielectric oxide layer is deposited on the aluminum (copper) to isolate the first layer of aluminum form the next. At this point, each wafer is polished using a chemical mechanical planarization (CMP) process to provide the wafer a smooth surface. Then the next layer of aluminum (copper) is deposited, patterned, and etched to create another connecting layer. The process is repeated as many interconnect layers as are required for the chip design.

The fabrication processes are performed in a clean-room environment to prevent foreign materials from contaminating the wafers. The facility in which wafer fabrication takes place is often referred to as a *fab*. The *fab* is typically divided into *bays*, which are

groups of identical or similar fabrication resources. For example, the etch process equipment may be grouped together to form one *bay*, and the diffusion and implant equipment may be in another *bay*. The wafers move through the *bays* in lots, and generally each lot has same number of wafers.

The steps involved in wafer manufacturing and wafer assembly are shown in Figure 1-1 [2]. A typical wafer and the circuits on the wafer are shown on Figure 1-2 and Figure 1-3.

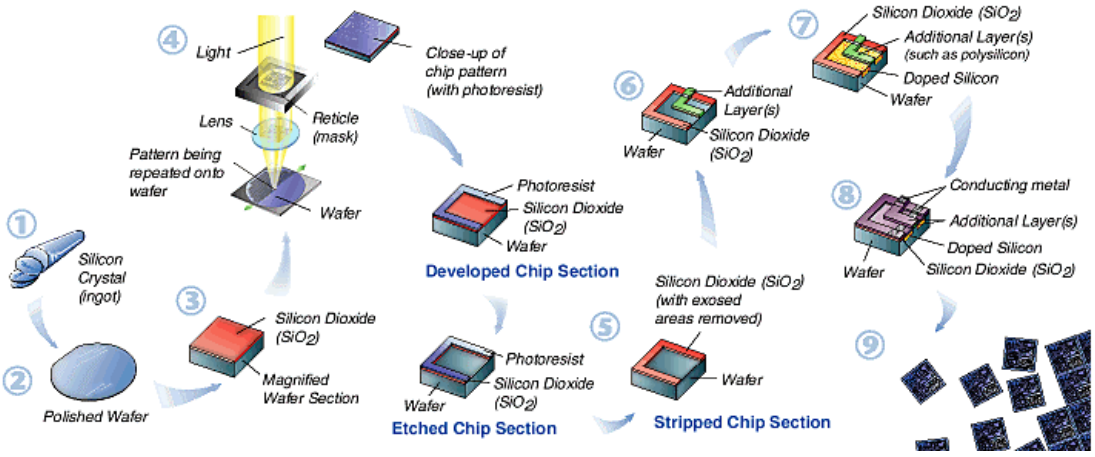


Figure 1-1.Semiconductor Manufacturing Process (adapted from www.sematech.org)

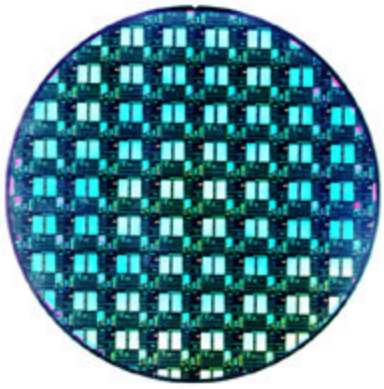


Figure 1-2. Wafer [27]

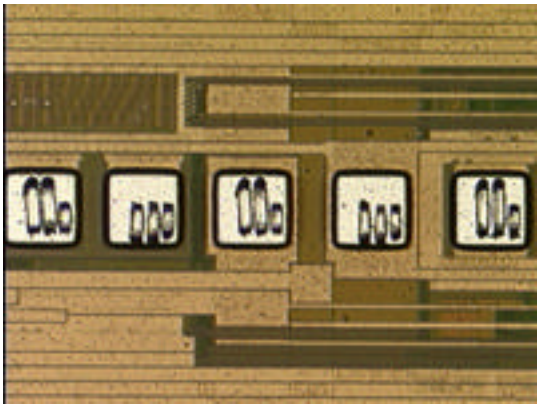


Figure 1-3. A Portion of Circuit on Wafer [27]

Following wafer manufacturing and wafer fabrication, individual chips on the wafer are tested for electrical performance according to specification. In the wafer probe test, each device on the wafer is tested electrically using a thin probe, and the chips that fail to meet specification are marked. The goal of the wafer probe testing is to ensure that customers receive a defect free product. This test is generally performed by using automated testing equipment to interrogate each integrated circuit and determine whether it is operating at the required specifications. The failing devices are marked with an ink dot and discarded. The good devices are then put into individual packages for protection and to provide the foot connections for the chips. Package styles include dual in-line package (DIP), QUAD, and ZIP packages.

Semiconductor test process can incur up to 25% of the semiconductor manufacturing cost [22]. Thus, improving the efficiency of the test process for semiconductor wafers has been an area of recent focus. One of the improvement efforts focuses on design for testability (DFT), which involves improving the wafer design to facilitate wafer tests. For example, one of the DFT techniques is a built-in self-test (BIST) in which test circuits or sets of vectors are built into the semiconductor chips to execute the test function. The BIST circuits have the ability to generate a pass or fail verdict for a tested chip and report additional information to narrow down the type and the location of the failure mode that is causing a failure [3]. With this method, the wafer test processing time is shortened. Another improvement effort focuses on increasing the efficiency of the test processes, with emphasis on optimizing the scheduling process for wafer testing [4]. Effective scheduling of the test process can improve throughput and decrease the capacity requirements of the test facility. This research addresses the wafer test scheduling problem for semiconductor manufacturing.

1.2 Motivation of Research

As the complexity of semiconductor chip increases, the cost and complexity of new semiconductor device manufacturing and test equipment has increased as well. This increasing equipment cost, along with the increasing market demand of semiconductor devices, often leads to limited capacity. The efficiency of semiconductor device manufacturing and testing, therefore, is a focal point of the semiconductor industry.

Scheduling is one of the most important issues in increasing the efficiency of manufacturing systems, and it has been studied for many decades. Many researchers, however, have identified the gap between theoretical progress and industrial practice and have concluded that there is a need for more realistic models of the scheduling problems and better scheduling algorithms [22]. This research focuses on solving the test scheduling problem which arises in the semiconductor test environment and is motivated by an actual industry problem.

This research problem was identified during discussions and visits with an international semiconductor manufacturing firm. The manager and planners at the factory described the complexity and importance of the scheduling problem and this led to a collaborative research project. Thus, the primary motivations for studying this test scheduling problem are:

- The problem is a complex planning problem at an actual industrial environment that has not been adequately addressed;
- Semiconductor test process may incur a substantial part of semiconductor manufacturing cost [22];
- Semiconductor test is important for ensuring quality control, and also provides important feedback for wafer fabrication improvement;
- Semiconductor test is the last step before the semiconductor devices leave the facility for packaging and final test; and

- Effective solution of the problem can reduce the cost of the test process by reducing the need to invest in new test equipment (each test station may cost up to $2 million).

The goal of this research is to develop a realistic model of the semiconductor wafer test scheduling problem and provide heuristics for scheduling the test operations. This research fills a gap between current academic research and actual industry requirements by developing an accurate model of the wafer test scheduling problem and providing a solution approach that can be implemented into an industrial application.

1.3 Organization of Thesis

The purpose of this research is to develop a new approach for scheduling test processes for semiconductor wafer on multiple test stations to minimize the maximum completion time of all wafer devices. An overview of the semiconductor manufacturing process and the need for conducting this research has been presented in Chapter I. An overview of the problem addressed in this research is presented in Chapter II. A detailed literature review of the latest research on similar problems is addressed in Chapter III. Chapter IV provides a mathematical model of the problem. Chapter V presents four heuristic solution approaches for addressing the scheduling problem. Chapter VI addresses the analyses of the heuristic approaches for a static production scenario. Chapter VII describes two case studies of the heuristics using industry data. Finally, Chapter VIII presents the conclusions of this thesis research and areas for future research.

CHAPTER II
PROBLEM DESCRIPTION

In the semiconductor test process, a series of tests are conducted on wafer devices using computer controlled testing equipment at various temperatures. The primary purpose of the testing process is to ensure quality wafer device are provided to customers. This chapter describes the test environment for semiconductor devices and presents the test scheduling problem.

2.1 Test Scheduling Problem

In a semiconductor test facility, multiple types of semiconductor wafer devices with required production quantities are processed across a set of test stations during a given time horizon. The wafer devices typically are processed through a series of test processes in lots of approximately 25 wafer devices. The test processes are conducted by automated test stations at specific temperatures using a specific prober card and a handler. The test process must occur in a specific sequence, thus resulting in precedence constrained processes. The processing times at each test station are known but the setup times are dependent on the previous configuration of the test station, resulting in sequence dependent setup times.

The test scheduling problem involves assigning each test process for each wafer device lot to a test station and sequencing each lot on the assigned test station. The objective is to maximize the throughput of the wafer devices by minimizing the makespan. The following sections provide additional description of the wafer devices, test processes, test stations, and the objective function.

2.1.1 Wafer Devices

Multiple types of wafer devices similar to the sample shown in Figure 1-2 may be tested. Typically the wafer devices are processed in lots of approximately 25 wafer devices and they often travel through the facility in boxes as shown in Figure 2-1.

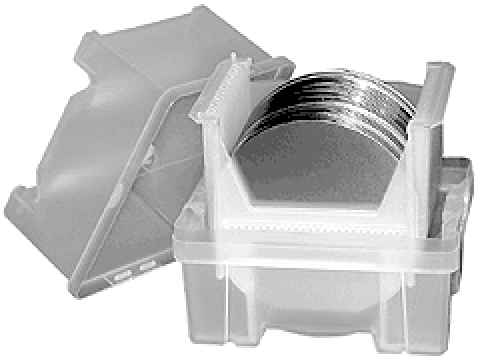


Figure 2-1. Example of Multiple Wafer Shipping Box [29]

2.1.2 Test Processes and Test Stations

A test process consists of both setup operations and processing operations on the test station. Setting up a test station to evaluate a certain type of wafer device involves:

- Obtaining an appropriate prober card and placing it on the test head;
- Bringing the test station and prober card to the required temperature for the test process; and
- Downloading the required software.

Processing a wafer on a test station may consist of:

- Electrical test: The electrical test is an operation to test the electronic performance of a semiconductor device against manufacturers' data book limits, such as *dielectric strength, dissipation factor, surface resistively* etc.
- Functional test: Functional test is an operation to exercise all of the chip's designed features under software control. Failure to meet the functional specification is identified by the test station and wafer device is identified as a reject.

- Package test: The package test is the final test for semiconductor devices after they have been packaged. All of the chip's designed features are tested under software control using automatic test equipment (ATE).

A semiconductor test facility commonly has a variety of test stations, and most of them have the capability to perform several different test processes with proper configuration. A test station consists of a computer system and at least one test head. The computer system is loaded with an automatic testing program, and the test head is loaded with the wafer device that needs to be tested. A handler is used to load (or unload) a wafer device on a test head. A prober card, composed of probe pins for testing the wafer device circuits, is installed in the test head in order perform the tests on the wafer device. For each type of wafer device, a different prober card and a handler are needed. As shown in Figure 2-2, a test station may contain multiple test heads. In this figure, and in the environment under study, there are two test heads on each test station.

Figure 2-2. Example of a Test Station. [28]

For a test station with multiple heads, a single lot of wafer devices is tested on each head and each head is independent in terms of loading and unloading the test device. The heads, however, must perform the same type of test processes at the same time. The setup strategy of one test head, therefore, influences the setup strategy of other test heads.

Setup time occurs when a test head has conducted a test on a device and a different device is loaded for testing. The setup of test heads may involve changes in hardware (such as a prober card), test head temperature, or software. The changeover time between different wafer devices or test processes can range from several minutes to several hours. For example, in the environment under study, installing a prober card requires approximately 30 minutes, downloading new software for a test process requires approximately 10 minutes, and changing the temperature requires 4 hours. Table 2-1 summarizes the test station setup scenarios for different situations.

Table 2-1. Setup Change Scenarios for a Test Station

Wafer Type	Process Change	Setup Steps
Same wafer type	Different test process at same temperature	Software download
Same wafer type	Different test process at different temperature	Software download Temperature change
Different wafer type	Same test process	Prober card change
Different wafer type	Different test process at same temperature	Software download Prober card change
Different wafer type	Different test process at different temperature	Software download Temperature change Prober card change

From Table 2-1, it is clear that the setup time of a device is dependent on the previous configuration of the test station. Thus, the time required to setup a device on a test station is considered sequence dependent.

2.1.3 Objectives of Test Scheduling

The main focus of wafer test scheduling is to minimize production cost and increase throughput while meeting delivery dates. Since these scheduling criteria may conflict with each other, it is important to understand the production environment.

The functional test operations are the last stage of the semiconductor fabrication process before the wafers leave the manufacturing facility. The outputs of the test processes are finished devices that are generally either made-to-order or made-to-stock. In the make-to-order environment, on-time delivery is important to ensure customer service. For example, in the Application Specific Integrated Circuit (ASIC) market, the circuits on the wafer devices are custom designed for customers with specific due date requirement. Therefore, minimizing the number of tardy jobs or minimizing maximum tardiness is often used as the criteria for scheduling in the made-to-order environment. Conversely, in the make-to-stock environment, maximizing throughput is a more common objective. Throughput is the number of finished lots in a certain time horizon. For example, in the DRAM market, the devices are standard products that are produced in high volume and a specific due date is often not associated with each wafer device. In this case, a major emphasis is placed on high throughput and equipment utilization, while reducing the mean and the variance of cycle times [6].

2.2 Summary of Test Scheduling Problem

The wafer test scheduling problem involves planning a variety of test processes on multiple wafer devices using a variety of test stations. Based on an analysis of the semiconductor test environment under study, the difficulties in solving the test-scheduling problem arise from a combination of the following process characteristics:

1. Multiple device types: More than one type of wafer device is tested in the facility.
2. Multiple test processes: Multiple test processes are required for each device.
3. Precedence constraints: The semiconductor devices must go through the test processes in a given sequence.

4. Sequence dependent setup times: A setup operation may require: prober card changeover, software download, or temperature adjustment. The setup operations required for a wafer device on a test head are dependent on the previous wafer device and test process on the test head.
5. Dependent multi-head test stations: A test station facility may have up to four testing heads [4]. These test heads cannot perform tests independently of each other. The setup strategy of one test head influences the setup strategy of the other test heads.
6. Alternative equipment types: There are different types of test stations that are capable of conducting the tests. Some wafer lots can be only tested on specific types of test stations, and this constraint may limit throughput.
7. Capacity limitations: Due to the high cost of test stations, the test capacity is often limited. In addition, each test for a wafer device requires a specific prober and handler and these resources may also be limited.

The combination of these characteristics results in a very complex job-shop scheduling problem. Thus, the test scheduling problem is related to the general job shop scheduling problem that is known to be NP-hard [5]. In the next section of this chapter, the scope of the scheduling problem addressed in this thesis is presented.

2.3 Scope of Scheduling Problem Presented

To successfully model a semiconductor test facility, we consider many of the characteristics of the test environment. The characteristics included in this research include: multiple device types, multiple test processes, precedence constraints, sequence dependent setup times, large production demands, and alternative equipment type. On the other hand, we choose to make some simplifying assumptions, either because the assumptions can be easily relaxed or they are very close to the actual test environments. For example, we do not consider the number of prober cards as a constraint. It is common to guarantee sufficient prober cards, since the test station utilization is often of high priority. When formulating the problem as a mathematical model, we assume that

each head of a multi-head test station is an independent tester. With this assumption, the mathematical model presents a situation that the test heads may be setup for different test process at the same time. The heuristic approaches discussed in Chapter V, however, ensure that the individual test heads of a test station work on the same test process at the same time.

2.4 Semiconductor Device Test Schedule Problem Statement

In this section, the description of the test scheduling problem is presented.

Given:

- A set of L semiconductor device lots (indexed by l=1, …, L);
- Each lot is characterized as a type of t of wafer (where t=1, …, T);
- A set of P test processes (indexed by p=1,…, P) required for each wafer device at specific temperatures with specific prober cards. The sequence of test processes is:
    1. pretest 1 (at 85°c),
    2. pretest 2 (at 40°c),
    3. fuse test,
    4. post fuse (at 85°c).
- A set of K test stations (indexed by k=1,…K) available during the time horizon;
- The lot size of each test on a tester is known (approximately 25 wafers).
- The sequence dependent changeover/setup times (S_{ij}) that occur when the test heads change device types or processes.

Assume:

The individual test heads of the same test station can work on different test process (in the mathematical model).

Determine:

The assignment of each lot l and process p to a test station k and the sequence that the jobs are processed on each test station k.

Objective:

To maximize the throughput and minimize the completion time of a set wafer devices (makespan).

Based on the above problem description, note that only pretest 1 (high), pretest 2 (low) and post-fuse (high) require the capacity of the test facility. Thus, in the model, we only consider these three tests, which are referred to as:

- Process 1: pretest 1 (high).
- Process 2: pretest 2 (low).
- Process 3: post-fuse (high).

2.5 Problem Summary

This problem can be classified as a multi-resource, precedent-constrained, sequence-dependent job-shop scheduling problem, with the objective of minimizing makespan. This is formally denoted as an m/Prec/Sij/C_{max} problem in scheduling literature [5]. Therefore, the problem is related to job shop-scheduling problems with precedence constraints and sequence dependent setup times. In the next chapter, the literature related to the wafer test scheduling problem is presented.

CHAPTER III

LITERATURE REVIEW

The literature related to scheduling the test processes for semiconductor device is addressed in this section. There has been considerable research on shop floor control of semiconductor device production, where most of it relates to wafer fabrication and burn-in processes rather than the testing process. The following sections first present a survey of the literature that discuss general planning problems in the semiconductor manufacturing and then a survey of research in the semiconductor test scheduling problem.

3.1 Survey of Semiconductor Planning and Scheduling Literature

Uzsoy *et al.* [6] [7] provide an extensive description of problems in the semiconductor manufacturing area. In one of their reviews on production planning and scheduling models in the semiconductor industry, Uzsoy *et al.* [6] point out that scheduling in the semiconductor manufacturing industry has generally focused on aggregate master planning. The master plan defines the production planning goals for a certain planning horizon according to actual customer orders, forecasts, and manufacturing capacity information. Then a more detailed shop floor level plan is developed within the constraints of the master plan. Therefore, the performance of the shop floor plan is constrained by the production planning decisions made at higher level. Uzsoy *et al.* [7] expand on this discussion by focusing on shop-floor scheduling problems in semiconductor industry. The authors indicate that three major approaches used in the shop floor control are:

1) Control-theoretic approaches and knowledge-based systems;
2) Deterministic scheduling algorithms; and
3) Input regulation and dispatching rules.

After a comprehensive review of literature of each approach category, the authors summarize the advantages and disadvantages for each approach and present areas for future research. For the control theory approach, the authors point out that the approach renders the complex scheduling problems more tractable, however the objective functions are in terms of long-term averages and hence cannot be used to track individual lots. With the deterministic scheduling approach, based on mathematical models, the system is difficult to model to the level of detail necessary for capturing the characteristics of the system. Even the simplified formulations used are often NP-hard and computationally intractable. The applicability of this method in an actual manufacturing setting is severely limited. Due to the complexity of the scheduling problem, the most common method has been the use of the dispatching and input regulations rules, which require less computational resources and time. The literature has shown that dispatching rules and input regulations methods can be used to reduce the mean and variance of a lot flow time on the shop floor. Most dispatching rules used in semiconductor manufacturing, however, do not take sequence-dependent setups into account [7]. Therefore it is important that future research has the ability to incorporate the sequence-dependent setups.

3.2 Semiconductor Test Scheduling Literature

In this section, the papers that discuss semiconductor test scheduling problem and the relevant operations research method for the test scheduling problem are presented. The articles on single machine problems are presented first followed by multiple machine problems.

Yoo and Martin-Vega [12] present a decomposition method for scheduling semiconductor test operations, with the objective of minimizing number of tardy jobs. The semiconductor test environment described in this publication consists of multiple test stations and one brand-workcenter. Each job is processed at a single test station and consists of several test operations at different temperatures. All lots have to be processed at brand-workcenter after the test operations. The decomposition method first decomposes the job shop into individual workcenters and assumes that the jobs processed

at each workcenter are known in advance. Then all jobs for each test station are sequenced independently of other test stations using the General Algorithm Framework (GAF). Based on the jobs completion times obtained in each test station, the branding operations for all the jobs are sequenced using GAF for the brand workcenter.

The GAF is an algorithm that solves a single machine problem to minimize the number of tardy jobs. In the first step, the algorithm identifies the jobs that cannot be completed on time regardless of the sequence and places them on the *removed* job list. The remaining jobs are then sequenced using EDD (Earliest Due Date) rules. In the second step, the sequenced jobs list is then divided into two sub-lists. The first list contains the jobs from the first job up to the first tardy job in the EDD sequence job, and the second job list contains the remaining jobs in the EDD job sequence. The first sub-list is re-sequenced to check if the tardy job can be finished on time. If there exist a new sequence that leads to no tardy jobs, then a job in the second sub-list is added to the first list and re-sequence again. This process continues until the first job list schedule contains one tardy job that cannot be re-sequenced to be finished on time. The first job list now consists one tardy job. In the next step, among the jobs in the first subsequence, candidate jobs are found, which are defined as the jobs whose removal allow the jobs in the second subsequence to be on time. Then among the candidate jobs, the job whose removal results in minimal completion time for the last job in the first sub-list is placed on to the *removed* job list. The two job lists are then joined, and the process starts from second step again until the list contains no tardy jobs. The final sequence is created by adding the removed jobs to the current sequence. The decomposition method presented in this publication is only suitable to the job shop environment where all the test operations of a lot must be completed at a single test station and the jobs to be processed on each test station are known in advance.

Freed and Leachman [18] address the scheduling problem for a single tester with multiple heads in a complex test job environment. The multi-head tester is assumed to be parallel testers and the devices in each tester head must be identical and must be loaded and unloaded together at the same time. In this parallel multi-head tester system, a CPU tests a single device from each of its processing heads in each cycle. The scheduling problem

in this test environment involves precedence constraints between operations, sequence dependent changeover times between jobs, and also incorporates the preventive maintenance (PM) schedule of the multi-head tester. The authors develop an enumeration method to solve the problem optimally by determining the allocation of lot operations to test stations and the sequence of configurations on each tester head during the shift to maximize the lot throughput. In a case study presented in the paper, the enumeration method takes 2.3 hours to get an optimum solution for ten lots on a single test station with three test heads.

Freed and Leachman [18] provide a complex model for the semiconductor device test operations which includes the following characteristics: multi-head tester, sequence-dependent setup time, precedence constrains among lot operations, and machine preventive maintenance schedule. The enumeration method also takes the priorities of each lot into consideration, which reflects an actual industrial objective. The proposed method, however, requires long execution times and significant computer memory (a problem with ten lots requires 3GB computer memory). As the authors point out, the extension of the enumeration program to the multiple test station with multi test heads problem is likely to be practical only for small problems.

Uzsoy *et al.* [10] presents several algorithms that address the single machine scheduling problem for semiconductor testing. These algorithms have different objectives such as: minimizing makespan, minimizing number of tardy jobs, or minimizing the maximum lateness. This publication models the lots of wafer devices as jobs that need a series of test operations at different temperature. The jobs have with precedence constraints and sequence dependent setup times. Two algorithms are presented to minimize makespan: LS Algorithm, and EJ Algorithm. At each step of the LS Algorithm, when a machine is free and there are one or more available operations, select one of the available operations and sequence it next. The operation to be selected can be specified using different criteria such as earliest due date or shortest processing time. At each step of algorithm the EJ Algorithm, when a machine is free and there are one or more available operations, sequence next operation with largest value of delivery time. Delivery time is defined as

the time required for each job to reach its destination after completing processing on the machine. The authors prove that the upper bound of these algorithm is 3C*, in which C* is the optimal makespan solution for the problem. In some special cases, the upper bound is 2C*. Two algorithms are presented to minimize the number of tardy jobs: NTH Algorithm and a dynamic programming procedure. The NTH Algorithm, which is based on Moore's algorithm [1], first obtains a solution to the L_{max} problem. This sequence is then examined up to the first tardy operation, and the lot that results in the largest time saving is deleted until L_{max} is nonpositive. The final sequence is then constructed by taking the current sequence and appending the deleted jobs to the end in any feasible order. The dynamic programming procedure presented in this publication gives optimal solution for the objective of minimizing number of tardy jobs. The number of iterations required in the dynamic programming approach are $m(N+1)^m n^S$, where N is the operations of a job, m is number of lots, and S is distinct setup time values.

In the publication, the authors analyze the approximation algorithms (LS, EJ, and NTH) in the presence of sequence-dependent setup times with different planning objectives. The authors show that, even with single machine and particular problem structure, the general problems have not, until now, been shown to have practical solutions. The complexity of the dynamic programming procedure in the article is polynomial in the number of operations and exponential in the number of lots. All of the algorithms presented in this publication, however, apply to a single machine environment and would need to be extended for practical industrial applications with multiple machines. The paper suggests using heuristics to develop new algorithms for similar problems of parallel identical test systems.

In another paper, Uzsoy *et al.* [11] address the job shop problem of semiconductor test scheduling with sequence-dependent setup time for multiple workcenters. The objective of the problem is to sequence the test jobs to minimize maximum lateness (L_{max}) on multiple tester stations. Each test job described in this research consists of several test operations. The operations are conducted in a predefined sequence at different temperatures that result in sequence dependent setup times. The authors model the job

shop using a disjunctive graph approach. With the disjunctive graph, a node corresponds to an operation for a job, a directed conjunctive arc between a pair of nodes represents a precedence constraint of operations, and a disjunctive arc between a pair of nodes represents operations that have no precedence relation. The approach divides the test facility into several workcenters and each workcenter is sequenced independently. A disjunctive graph representation at the entire facility is used to capture interactions between workcenters. The authors provide two algorithms to minimize maximum lateness for a single test station with sequence dependent setup times.

The first approach is Neighborhood Search Algorithm that provides a local optimal solution. Given the disjunctive graph for an initial sequence of operations for a test station, the algorithm examines pairwise exchanges between the adjacent nodes that have no precedence constraints. The exchanges that lead to an improvement of L_{max} are used to generate neighboring sequences, and this procedure is applied to all neighboring sequence until no further exchanges leading to improvement can be found. The second approach is a branch and bound algorithm that provides a global optimal solution. The branch and bound algorithm proceeds by partitioning all possible solutions into subsets. The subsets that have a lower bound value greater than the already obtained feasible solution are discarded, and the subset that has smaller lower bound value are further partitioned until all possible subsets are examined. This algorithm is guaranteed to obtain optimal solutions, although it is computationally time intensive.

Xiong and Zhou [13] propose and evaluate two Petri net based hybrid heuristic search strategies for the semiconductor test scheduling problem, with the objective of minimizing makespan on parallel test stations. In the paper, a Petri net is defined as a bipartite directed graph containing nodes, transitions, and directed arcs that connects nodes to transitions. A node represents either an operation of a job or a resource (test station), and each node is associated with a fixed time that defines the operation time. A transition represents the start or completion of the operation of a job. A directed arc connecting the node and transition defines the precedence constraints of the operation, and the directed arc connecting the resource (test station) and the transition represents the

loading/unloading event for a test station. For each job, a sub-Petri net is constructed by connecting the operations nodes, transitions, and resources. A complete Petri net model for the test environment is obtained by merging the sub Petri nets through the shared resources. Finding the schedule solution involves finding the operation path for all jobs using the Petri net. Two solution approaches are then proposed based on the Petri net model

The two approaches are based on two search algorithms: Best First (BF) and Backtracking (BT). The BF search algorithm starts by generating all the possible assignments for the first operation of each job based on the initial resource set up. This process involves examining the directed arcs sets that connect the transitions of a job with resources nodes. The set of arcs that have minimum f value, which is a function of makespan, is selected. The nodes for the selected directed arcs are then expanded. The nodes expansion process continues until the path for each job is created in the Petri net, which is the final optimal solution. The BT search algorithm explores only one possible set of directed arcs at each step until the final solution is generated. However, the BT algorithm sometimes will result in infeasible solution, on which a backtracking process is adopted until a feasible solution is generated. The BF algorithm guarantees optimal solution while it is very time consuming, and the BT algorithm saves time but does not guarantee optimality. The authors present two heuristic search methods that take advantage of these two algorithms: the BF-BT algorithm and the BT-BF algorithm. Basically the BF-BT algorithm uses BF as the main algorithm and adapts BT algorithm at certain steps when some criteria is met, whereas BT-BF algorithm uses BT as the main algorithm and adapts BF algorithm at certain steps when some criteria is met. The proposed algorithm is developed for a parallel machine environment, in which the machines setups do not change during the planning horizon. Moreover, sequence dependent setup times are not considered.

Chen and Hsia [14] model the scheduling problem of semiconductor test environment using a Lagrangian relaxation approach. The model described in this publication focuses on three operations (wafer sorting, pre burn-in, and post testing) that require testing

resources such as a test station, prober card, and handler. The objective of the model is to minimize the weighted quadratic tardiness subject to three constraints: resource constraints, precedence constraints, and processing time requirements. The planning horizon in the Lagrangian model is divided the into discrete time intervals. For each time interval, the resource availabilities such as the number of test stations, number of prober cards, quantity of handlers, and their related capacity are regarded as constraints. The Lagrangian approach presented in the paper does not guarantee an optimal, or even feasible solution. In some cases, certain stopping criteria need to be employed to terminate the program using conditions such as a fixed number of iterations has been reached, or the objective value remains almost unchanged for a certain number of iterations. This termination may result in an infeasible solution and a greedy heuristic procedure is employed to construct a feasible solution. The heuristic procedure proceeds first by constructing a sequence of operations (jobs) sorted according to the starting time in the infeasible schedule, and then each operation is scheduled in sequence considering the resource availability until all the operations are scheduled. Two test examples are presented in the paper. The first example has 5 jobs to be scheduled, and the test facility has 2 types of test stations, 2 types of prober cards, 2 types of handlers, and the planning horizon is 15 time units. The Lagrangian model solves this example problem optimally. The second example has 30 jobs (90 operations) to be scheduled, and the test facility has 4 types of test stations, 2 types of prober card, 5 types of handler, and the planning horizon is divided into 40 intervals. The setup time of the operations is fixed, and the solution has 4.87% gap to lower bound.

The Lagrangian model presented by Chen and Hsia [14] does not include sequence dependent setup time, instead the time between operations are fixed and the setup time of an operation is considered as a part of processing time. The model uses discrete intervals to represent the continuous time environment of the planning horizon. This modeling method may cause a gap or even infeasible solution for the continuous time environment. Moreover, as the planning horizon increases and has more time intervals, the size of the model formulations will increase rapidly.

Liu and Chang [15] develop a Lagrangian relaxation based approach for scheduling semiconductor test operations in a flexible flow shop (FFS) with sequence-dependent setup times. The objective of the problem is to minimize the setup time and WIP while meeting the order due date. Like Chen and Hsia [14], Liu *et al.* [15] model the planning horizon in units of discrete intervals in their integer program model. Thus, the processing times and setup times are in multiples of these intervals. The model is formulated as a separable integer programming problem with synchronization constraints: one part models the job scheduling, and the other part models the machine usage scheduling. The two parts are linked via a synchronized function that forces the units of machine usage to equal to the processing time units of all the jobs. The two sub-problems are solved using an algorithm developed by Luh *et al.* [16]. The schedules of the sub-problems solutions are compared, the matched schedule parts are retained and the unmatched parts are reevaluated using a heuristic developed by the authors to create a final schedule. The authors apply the model to a semiconductor device test scheduling problem, and the resulting schedule is better than the actual schedule. In the case study, the sequence-dependent setup time is ignored. Instead, the processing times are lengthened by 20% to incorporate the setup time and the setup time is assumed to be zero.

The Lagrangian relaxation method presented by Liu *et al.* [15] decomposes a complex integer programming model into two small sub-problems, which allow the original problem to be more solvable. However, due to the complexity of the original problem that involves sequence-dependent setup time and precedence constraint, the solutions of the sub-problems are often infeasible.

Chen, Chang, Chen, and Kao [17] present a Lagrangian relaxation approach for the scheduling problem of an semiconductor sort and test facility with preemption, with the objective to minimize the total weighted tardiness. The test environment has various probers and hardware that are used in conjunction with the test stations to perform the test operations. The resource constraints on test stations, probers, and hardware are considered in this publication. The resources are available for production on the night shift and only some of them are available during the day shift, since some machines may

be needed for other purposes, such as maintenance. Therefore, the jobs that are processed on these machines during night shift may have to be preempted at the beginning of the day shift. In this job shop environment, there are no precedence constraints between jobs or sequence dependent setup times. The authors use an integer programming formulation to the describe the environment. Four examples problem are presented and solved using the Lagrangian relaxation approach. The number of jobs range from 10 to 102, the numbers of test stations and prober cards range from 2 to 4, and the scheduling horizon ranges from 18 hours to 200 hours. The solutions for the example problem are 0.07%-5.22% above the lower bound.

Huang and Lin [9] present a shop floor interactive scheduler system for a wafer probe center in semiconductor manufacturing. Scheduling for the wafer test center must consider multiple issues: priority of wafer lot, number of lots completed per day, change over times, and wafer lot waiting time. The schedule must also take into account the planned maintenance of the test machine and the sequence dependent setup times between the test jobs. The authors indicate that computer decision support systems (DSS) with general dispatching rules are too rigid to incorporate multiple criteria and often do not generate satisfactory results. On the other hand, a manual approach based on human experience becomes inefficient if the production scale is large and product mix is complex. The authors present an interactive scheduling system that takes advantage of both of these approaches to solve the problem. The interactive scheduler works in three steps. In the first step, the scheduler system generates an initial schedule that has no changeover. In the second step, if the initial schedule is not satisfactory, the user changes the performance measures and control variables (such as the allowed number of changeovers or the allowed number of tardy jobs). In the third step, the interactive scheduler will regenerate a schedule according to the user input and a Scheduling Knowledge Base (SKB). The SKB is based on the dispatching rules developed by the authors. The SKB examines the parameterized dispatching formulation (PDF), the summation of weighted decision variables such as lot waiting time, changeover time, due date, and lot priority, etc. Once a machine is available, the dispatching rule selects the wafer lot that has largest PDF. This process continues until the user is satisfied with the

schedule obtained. In a case study, the authors compare the proposed interactive scheduler with the manual method and six other scheduling rules such as earliest due-date (EDD), no changeover (NCO), short processing-time (SPT), highest general-priority first (HGP), lowest hit-rate first (LHR), and least number of machines (LNM) that are capable of processing the lot. They find their scheduler outperforms all other method in terms of PDF and computation time. However, the scenarios presented in the case study do not include sequence-dependent changeover times, instead, the authors use the average setup time.

The performance of the interactive scheduler largely depends on user experience, because the schedule is generated based on a set of weighted performance measures input by the user. These inputs influence the quality and the feasibility of the results. Thus, only experienced users may take the full benefit of the interactive scheduler. Moreover, since the proposed dispatching approach does not address sequence-dependent setup time, the resulting schedule will likely result in additional setup time.

3.3 Related Scheduling Literature

This section presents some general heuristic approaches found in the scheduling literature. The methods have not been adapted to the semiconductor test problem yet, but appear in the area of scheduling problem in a multiprocessors computer network and may be applicable for the wafer device test scheduling problem.

Selvakumar *et al.* [19] present a classical multiprocessor communication-network scheduling problem that allows variations in the number of tasks, the execution times of the tasks, and number of processors. These assumptions result in a multitask, multi-machine job-shop environment. In addition, the multiprocessor scheduling problem considers inter-task communication that is not negligible. The inter-task communication time is variable, which can be regarded as sequence-dependent setup times. The communication tasks can be processed by any processor and can transfer through different processor with non-negligible inter-processor communication cost [19].

Therefore, the multiprocessor scheduling problem is analogous to a general classical job-shop problem, and is known to be NP-hard. Hence, the solution approaches that address similar multiprocessor network routing problem are promising to solve scheduling problem in multi-machine job-shop environment.

El-Rewini and Lewis [21] present a Mapping Heuristic (MP), and Sih and Lee [22] present a Dynamic Level Scheduler (DLS) for these type problems. Mapping Heuristic (MP) and Dynamic Level Scheduler (DLS) are two algorithms that address multiple processors problems that have N precedence-constrained tasks, which must be processed in order. For problems with N tasks, both of the heuristics, take exactly N scheduling steps to develop a solution. A sequence of computations is performed during which exactly one ready task will be scheduled to a processor (machine). A ready task is defined as a task which has no predecessors or all its predecessors have been scheduled. The priority of each ready task is computed by a certain criteria and the task with highest priority is selected and added to the current scheduling step such that it finishes earliest. The priority of each task is either calculated at the beginning the scheduling process, or calculated at each step of scheduling. If the priority of each task is calculated before the commencement of the scheduling process, the priority of each task remains unchanged for the entire scheduling algorithm. If the priorities are calculated during the scheduling, then, each task's priority is re-calculated at each step of the scheduling process.

The Mapping Heuristic computes the priorities before commencing the scheduling processes. The priorities are determined by the job's level, which is the sum of the execution times of all the tasks on the path of this job, plus the sum of necessary setup times of each task. If two jobs have the same level, then the task with more immediate successors will be assigned. If a tie still exists, the heuristic breaks the tie arbitrarily.

The Dynamic Level Scheduler Without Global Clock Heuristic constructs a priority list for each ready task at each scheduling step with respect to each processor (test head). The priority of a task is determined by following function:

$$DL\ (v_i) = SL(v_i) - \max\{(TF(p_i), DA(v_i, p_i))$$

Where *DL* (v_i), represents the dynamic level of job v_i. *SL* (v_i), the static level of v_i, is the length of the execution times from task v_i to the exit task. *TF* (p_i) gives the current time of processor p_i. *DA* (p_i, v_i) gives the time at which the prior tasks required by v_i are completed plus the preparation time of processors on v_i. The approach can be summarized as scheduling task v_m onto processor p_n, such that it finishes the earliest by the above criteria. In the comparative study presented in the paper, 150 random tasks are scheduled on eight processors. The performance of the algorithm is measured by speedup, which is the ratio of total completion time of tasks using sequential schedule over the completion time using the algorithm. Both MP and DLS algorithm have speedup value greater than 1, and DLS has a higher speedup value than MP.

3.4 Summary of Literature Review

The literature reviewed in this chapter includes articles on general semiconductor planning and scheduling issues, articles on semiconductor test scheduling methods, and articles on methods that may be applicable to the test scheduling problem. Since the test scheduling problem is classified as a $m/Prec/S_{ij}/C_{max}$ job shop problem, some publications that discuss similar job shop heuristics were also presented.

The publications that specifically address the scheduling problem of semiconductor device test facilities provide insight into the approaches and complexities for solving the semiconductor test scheduling problem. Table 3-1 briefly summarizes some of the articles presented in this chapter.

Table 3-1. Literature Review Summary

Author	Test Stations	Criteria	Prec	S_{ij}	Multiple Test Head	Method
Yoo *et al.* [12]	Single	Number of tardy jobs	No	No	No	Heuristic
Freed [18]	Single	Makespan	Yes	Yes	Yes	Enumeration
Uzsoy *et al.* [10]	Single	L_{max}	Yes	Yes	No	Heuristic
Uzsoy *et al.* [11]	Multiple	T_{max} and number of tardy jobs	Yes	Yes	No	Heuristic
Xiong *et al.* [13]	Parallel	T_{max}	Yes	No	No	Petri-net
Chen *et al.* [14]	Multiple	T_{max}	Yes	No	No	Formulation
Liu *et al.* [15]	Multiple	WIP, Due date	Yes	Yes	No	Formulation
Chen *et al.* [17]	Multiple	Number of tardy jobs	Yes	No	No	Formulation
Huang *et al.* [9]	Multiple	Hit rate of product, C_{max}, Idle time of machine, Number of change overs.	Yes	No	No	Heuristic

Due to the problem complexity, these articles develop solution approaches by making assumptions to simplify the problem, thus ignoring characteristics of the test processes and rending an inaccurate model. Some approaches in the literature only deal with single machines rather than multiple machines. Also, some of the approaches do not consider precedence constraints or ignore sequence dependent setup times. These assumptions limit the quality or applicability of solution. Because it is only recently that semiconductor test scheduling has attracted attention from industrial engineers and operation researchers, there is no model to date that incorporates all the characteristics of semiconductor test scheduling problem such as: multiple wafer devices, multiple test stations, sequence dependent setup time, precedence constraints, and multi-head test stations.

Some publications related to network technology address a similar scheduling problem. The heuristics are developed specifically for the communication network routing problem. The problem of scheduling communication tasks onto a multiprocessor involves scheduling precedence constrained tasks with sequence dependent inter-task

communication times in a way that minimizes the completion time. Since this is similar to the test scheduling problem, the solution approaches that address network routing problem may potentially be applied for solving similar scheduling problems in multi-machine job-shop environment.

Some research has focused on developing mathematical formulations and optimal solutions of generic problems. However, the complexity of the test scheduling problem renders the models intractable. As suggested by Uzsoy *et al.* [17], it is unrealistic to expect a generic scheduling algorithm to be implemented directly on a shop floor. In their review, the authors recommend that the future research should focus on specific applications and developing approaches to exploit the structure in an industrial context.

The research presented in the following chapters will develop an integer formulation for the semiconductor test problem. The integer program will take into account many of the important characters of the test environment. This mathematical model provides insights on the complexity of the problem. Subsequently, two heuristics for the scheduling problem are developed that focus on real industrial application. These algorithms could be essentially regarded as an improved version of the Dynamic Level Scheduler that applied to the scheduling of semiconductor device test problems.

CHAPTER IV

MATHEMATICAL MODEL

This chapter presents a mathematical model for the semiconductor test scheduling problem. To model the problem, a diagraph G (α, φ) is introduced to represent the scheduling environment. Consider a diagraph G consisting of a finite set of nodes α ($n_1, n_2, \ldots, n_n$) and a set of directed arcs φ {(n_1, n_2), (n_1, n_3),…. (n_m, n_n)} joining pairs of nodes in α. Arc (n_m, n_n) is directed from node *m* to node *n* when there is a *flow* between the pair of nodes. A node that supplies an arc is called source. A node that receives an arc is called sink.

This research associates each node in G with a test operation, where an operation involves a test process on a device. If one operation follows another operation, then the preceding node is the source node and the following node is the sink node. An arc is directed from a source node to a sink node. With the test scheduling problem, each node is associated with a device lot *l* and a test process *p*, and the nodes are identified accordingly. Thus, node (l,p) represents lot *l* undergoing test process *p*. For example, if lot 2 undergoing pre-test 1 (node(2,1)) follows lot 1 of pre-test 1 (node(1,1)), then an arc is connected from node (1,1) to node (2,1). Figure 4-1 presents a diagraph with four nodes and three arcs.

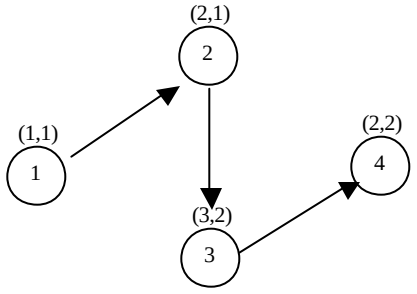


Figure 4-1. Diagraph with Four Nodes and Three Arcs

A sequence of arcs P = {(n_1,n_2)….. (n_{p-1},n_p)}, in which the initial node of each arc is the same as the terminal node of the preceding arc in the sequence and n_1……n_p are all distinct nodes, is called a *path* through the diagraph [5]. For the problem of semiconductor test, a path represents a series of operations that are assigned on a test station. For example, consider a problem with seven operations (n_1, n_2…, n_7) to be scheduled on 3 stations. With the diagraph representation method, three paths will be generated to represent the operation sequence on each station. Figure 4-2 illustrates one possible diagraph of the problem, where P_1={(n_1,n_6), (n_6,n_4)}, P_2={(n_3,n_2)}, and P_3={(n_7,n_5)}.

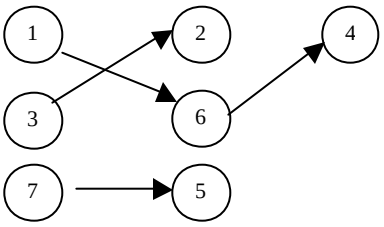


Figure 4-2. Diagraph for Seven Operations and Three Test Stations

For the test scheduling problem, the mathematical model introduces a dummy start job node *s*, and a dummy finish job node *t* to facilitate the formulation. Each sequence of test processes on a test station (path) starts with the dummy job node *s* and ends with the dummy job node *t*. The dummy job nodes *s* and *t* are essentially the origin and the destination point of all paths. The origin point can supply *K* arcs and the destination point requires *K* arcs, where *K* is the number of test stations. With these dummy job nodes, the problem shown in Figure 4-2 can be modeled as shown Figure 4-3.

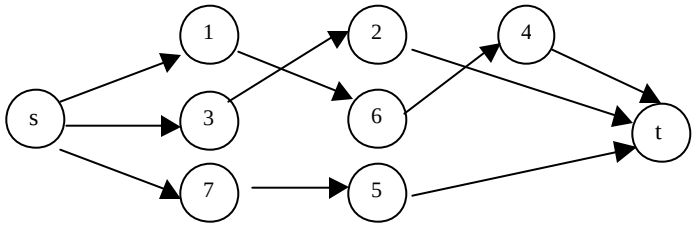


Figure 4-3. Diagraph with Dummy Nodes

As illustrated in Figure 4-3, the operations scheduling problem can be stated as follows: Connect origin node *s* with destination node *t* using the available number of paths with the objective of minimizing cost. A cost is associated with creating arcs between pairs of nodes. For semiconductor test scheduling, the nodes are the test operations (test processes on a device), the number of paths are equivalent to the number of test stations, and the cost of arcs is the setup times between the pair of operations. In addition, there are precedence constraints between the operations (nodes) for this problem, and precedence constraints are evaluated in terms of completion times for the constrained operations. In the next section, the mathematical model is presented and the formulation of the model is explained.

Parameters

i, l:	Index for lot
p,q:	Index for process
s:	Dummy jobs that are scheduled first on each test facility
t:	Dummy jobs that are scheduled last on each test facility
k:	Index for test head
$ST_{iq,lp}$:	Setup time of going from lot *i* process *q* to lot *l* process *p*
PT_{lp}:	Processing time of lot *l* process *p*

Variables

$X^{k}_{iq,lp}$ = { 1, if lot *l* and process *p* follows lot *i* and process *q* on test facility *k*; 0, otherwise

$X_{s,iq}$ = { 1, if lot *i* and process *q* follows the dummy job s; 0, otherwise

$X_{iq,t}$ = { 1, if lot *i* and process *q* scheduled before the dummy job *t*; 0, otherwise

CT_{lp} = Completion time of lot *l* process *p*

Formulation

Minimize $\sum_j CT_{jP}$ "P" is the post-fuse (high) test process of a job (4-1)

Subject to:

$$X_{s,lp} + \sum_k \sum_i \sum_q X^k_{iq,lp} = 1 \qquad \forall l, p \qquad (4\text{-}2)$$

$$\sum_k \sum_l \sum_p X^k_{iq,lp} + X_{iq,t} = 1 \qquad \forall i, q \qquad (4\text{-}3)$$

$$\sum_l \sum_p X_{s,lp} = K \qquad \forall s \qquad (4\text{-}4)$$

$$\sum_i \sum_q X_{iq,t} = K \qquad \forall t \qquad (4\text{-}5)$$

$$CT_{lp} - (CT_{iq} + ST_{iq,lp} + PT_{lp}) + M(1 - \sum_k X^k_{iq,lp}) \geq 0 \qquad \forall i, q, l, p \qquad (4\text{-}6)$$

$$CT_{lp} - PT_{lp} + M(1 - X_{s,lp}) \geq 0 \qquad \forall s, l, p \qquad (4\text{-}7)$$

$$CT_{l2} \geq CT_{l1} + PT_{l2} \qquad \forall l \qquad (4\text{-}8)$$

$$CT_{l3} \geq CT_{l2} + PT_{l3} \qquad \forall l \qquad (4\text{-}9)$$

$$CT_{lp}, ST_{iq,lp} \geq 0 \qquad \forall i, q, l, p \qquad (4\text{-}10)$$

$$X^k_{iq,lp}, X_{s,iq}, X_{lp,t} \in \{0,1\} \qquad \forall i, q, j, p, s, t \qquad (4\text{-}11)$$

The objective function (4-1) minimizes the completion time of the final operation (post-fuse test) of all the jobs. Constraints sets (4-2) and (4-3) ensure that each test job can be scheduled only once. The starting dummy job position *s* and completion job position *t* are introduced here to facilitate the formulation. Constraint set (4-2) requires that lot *l* and process *p*, node (l, p), should either be the first job that follows the dummy starting job or it is scheduled on one of the test stations (paths). The variables $X^k_{iq,lp}$ and $X_{s,lp}$ assume a value of either 1 or 0. Thus, this constraint set ensures that only one parameter is equal to 1 and that lot *l* process *p* is scheduled only once. To relate constraint set (2) to the diagraph, each node in the diagraph G has only one arc directed to the node. Likewise, constraint set (3) requires that each node can supply only one arc.

Constraints sets (4-4) and (4-5) ensure that there are K starting positions and K completion positions, since there are K test facilities available in the environment. To relate this to the diagraph, the dummy node s supplies K arcs and dummy node t receives K arcs. Since $X_{s,lp}, X_{iq,t} \in \{0,1\}$, these constraints ensure only K of the $X_{s,lp}$ and $X_{iq,t}$ variables will assume a value of 1.

Constraints sets (4-6) and (4-7) present the scheduling time constraints of the test jobs. The setup operation for a test station cannot be scheduled before the previous test operation on the test station is completed. The completion time for lot l and process p (CT_{lp}) is equal to the completion time for the previous lot i and process q (CT_{iq}) plus the setup time required to transition from lot i and process q to lot l and process p ($ST_{iq,lp}$) and the processing time for lot l and process p (PT_{lp}) assuming lot l process p follows lot i process q. Thus, the completion time for lot j process p can be stated as:

$$CT_{lp} \geq (CT_{iq} + ST_{iq,lp} + PT_{lp}) X^{k}_{iq,lp}$$

In order to linearize the formulation, a large positive number, M, is introduced, and constraint sets (4-6) and (4-7) are developed. If lot l process p follows lot i process q, then $\sum_k X^{k}_{iq,lp}$ equals to 1, and M(1- $\sum_k X^{k}_{iq,lp}$) equals 0. In this case, M has no influence on the completion formulation between operations. However, if lot l process p does not follow job i process q, then $\sum_k X^{k}_{iq,lp}$ equals 0. In this case, since M is a large positive number, the constraint sets (4-6) and (4-7) together with constraint set (4-10) allow CT_{lp} to be any number that is greater than or equal to zero. The objective function minimizes the completion time, however, so the values of the completion times are minimized to the extent possible. These constraints ensure that a setup operation for a job cannot be scheduled before the previous job on the test machine is finished.

Constraints sets (4-8) and (4-9) ensure the precedence constraints of the test processes. For any lot *l*, pretest 2 (low) must follow pretest 1 (high) such that the operation cannot be started before the previous test finishes on a test machine. Thus, the completion time of lot *l* process 2 (CT_{l2}) is greater or equal to the completion time of lot l process 1 (CT_{l1}) plus the processing time of lot *l* process 2 (PT_{l2}). In the same manner, post-fuse (high) must follow pre-test2.

The mathematical model presented in this chapter is a network flow model if there are no precedence constraints and sequence dependent setup times. While specialized solution approaches can be used to solve some network flow problems [5], the precedence constraints makes the problem NP-hard [7] and the sequence dependent setup times further complicates the problem. As the complexity of the problem indicates, the problem cannot be solved optimally in reasonable time for realistic size problems. Therefore, this research develops heuristic approaches to solve the problem.

CHAPTER V

OPTIMIZATION ALGORITHM PROCEDURE

This chapter presents a solution approach for scheduling semiconductor wafer tests across a set of test stations. As described, the scheduling problem of the semiconductor wafer testing problem is known to be NP-hard. With this complexity, it is difficult to ensure a mathematical optimum solution even for a small number of wafer lots test stations. Thus, heuristic approaches are developed to address the wafer test scheduling problem.

Four heuristic approaches developed in this research are:

- Lot optimization
- Lot optimization with tester constraint
- Process optimization
- Process optimization with tester constraint

The *lot optimization* solution approach focuses on reducing the flow time of each individual lot of wafer devices in an attempt to minimize makespan. The *process optimization* solution approach focuses on increasing the efficiency of the test stations in an attempt to minimize makespan. With this approach, similar test processes of the wafer lots are scheduled together in an effort to increase test station efficiency and reduce makespan.

The heuristics incorporate additional features not specifically included in the mathematical model. The heuristics ensure that each head of the test stations is configured for the same type of test process. In addition, the heuristics provide the capability to ensure that higher priority wafer lots are processed sooner.

In the actual manufacturing environment where this research is conducted, an additional test station constraint affects the scheduling strategy. This test station constraint requires that pretest 1 (high) and pretest 2 (low) test processes of a wafer lot must be processed on the same type of test station. The lot optimization and process optimization solution

approaches are modified to accommodate the test station constraint, generating two more solution approaches: *lot optimization approach with tester constraint* and *process optimization approach with tester constraint*.

A description of the lot optimization approach is presented in Section 5.1, and a description of the processing optimization approach is presented in Section 5.2. Section 5.3 introduces the issue of the tester constraint and presents the two solution approaches that incorporate the tester constraint. Section 5.4 describes the development of the suggested initial test station configuration and the lower bound for makespan. The performance of the solution approaches are tested in a case study in Chapter VI for a static situation, and in Chapter VII using actual industrial data. The results obtained by the solution approaches are compared to the lower bound and the actual schedules.

5.1 Lot Optimization Solution Approach

The lot optimization solution approach involves constructing an initial list of wafer device lots and then scheduling the wafer lots on the test stations using a scheduling algorithm. The initial list consists of the wafer lots that need to be scheduled and they are sorted using a special set of rules. The scheduling algorithm uses the sorted initial wafer lots list as a dispatching sequence and schedules the wafer lots in order of appearance on the list. An overview of the construction procedure of the initial wafer lot list and the scheduling algorithm are described below. In this algorithm, the term *lot* is used to refer to a set of wafers. Each lot is processed through a set of test processes and the term *job* is used to refer to a specific test process of a wafer lot.

5.1.1 Initial Wafer Lot List Construction Steps

Step 1: Sort the wafer lots by the following parameters:

- Current process status
- Wafer lot priority
- Shortest remaining processing time

The first sorting parameter is current process status. The wafer lots are categorized as in-process or waiting. The wafer lots that are in-process are first and the wafer lots that are waiting are next. The second sorting parameter is wafer lot priority. The lots with higher priority appear earlier in the list. The third sorting parameter is the shortest remaining processing time, which is the time required to complete all the remaining test process for the wafer lot. The lots that have the shortest remaining processing time appear earlier in the list.

Step 2: For the list generated in step 1, divide the wafer lots into jobs according to the remaining test processes of the wafer lot so that each job consists of only one test process for a wafer lot. For example, suppose a wafer lot has two remaining test process: pretest 2 (low) and post-fuse (high). In this case, two jobs are created, with one job for pretest 2 (low) test and one job for post-fuse (high) test respectively.

Using this initial list of jobs, the scheduling algorithm assigns the jobs to test heads until all the jobs are scheduled. The scheduling algorithm is described in the following section.

5.1.2 Scheduling Algorithm

Step 3: Set initial test station setup configuration

In order to apply the scheduling algorithm, a suggested initial test station configuration should be set. The initial test station configuration is described in Section 5.4.

Step 4: Choose the maximum allowed setup time (MAST)

This MAST value defines the maximum setup time that is allowed for the schedule. The possible MAST values are shown in Table 5-1. For example, if the MAST is chosen to be 0.65, then a prober card change and test program download, which takes 0.5 hours and 0.15 hours respectively, are allowed for a setup change on test heads.

Table 5-1. Maximum Allowed Setup Time (MAST)

MAST	Setup Action
0.00 hours	No setup
0.15 hours	Software download
0.50 hours	Prober card change
0.65 hours	Software download time and Prober card change
4.00 hours	Temperature change
4.65 hours	Allow all setup

Step 5: Calculate the setup time for each test head for the current job.

According to the test process and the wafer type of the job, the setup time is calculated for assigning the current job to each test head.

Step 6: Select candidate test heads

For the setup time obtained for each test head in Step 5, the test heads that have a setup time less than the value specified in Step 4 are selected as candidate test heads for assigning the current job.

Step 7: Assign the current job to a test head

For each candidate test head selected in Step 6, the completion time of the job is calculated. The job is assigned to the test head with minimum completion time. The completion time calculation method is discussed later in this section.

Step 8: Schedule the next job in the initial wafer lot list.

The subsequent jobs are scheduled using Step 5 to Step 7 until all the test jobs are scheduled.

For each wafer job in the initial list, the scheduling algorithm assigns the wafer job to a test head until all the wafer lots are scheduled. Figure 5-1 shows a flow chart of the steps of the *lot optimization* (LO) solution approach.

5.1.3 Wafer Lot Completion Time Calculation

The wafer lot completion time for each job (which is a specific test process for a specific wafer device lot) in Step (6) is obtained by adding the earliest possible starting time of the job for a test head to the processing time of the job and the setup time required for the job. The earliest possible starting time of the wafer a test head is obtained by comparing

the *test head available time* and *lot available time.* The completion time for lot *l* process *p* that follows lot *i* process on test station *k* is expressed as follows:

$$CT_{lp}^{k} = Max(LAT_{iq}, TAT_{k}) + PT_{lp} + ST_{iq,lp} \qquad (5\text{-}1)$$

where TAT_k is the *test head available time* and LAT_{iq} is the lot available time.

Lot Available Time

The *lot available time* is obtained using following function:

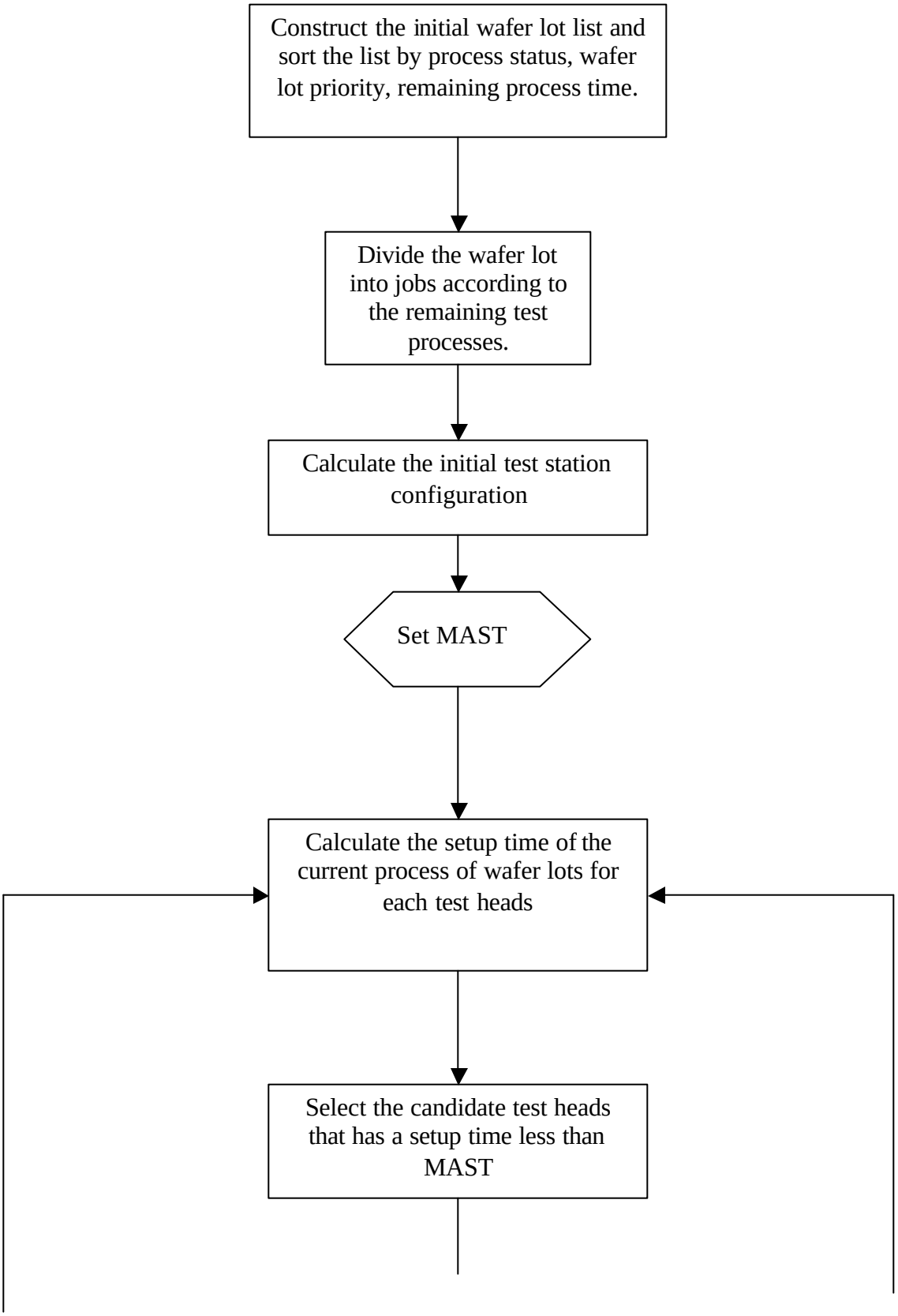
$$LAT_{iq} = \begin{cases} 0, & \text{if } q=1 \\ CT_{i(q-1)}, & \text{Otherwise} \end{cases} \qquad (5\text{-}2)$$

Test Head Available Time

The two test heads of the same test station must work on the same type of test process at the same time, and a setup to another test process on a test head cannot start until the other test head finishes its current lot. Therefore, the *test head available time* is determined by following method:

- If the current (previous) job on the test head is same as the wafer job test process that needs to be scheduled, then the available time of the test head is the completion time of the current (previous) test job on the test head.
- If the test head setup status is different from the wafer lots test process that needs to be scheduled, then the test head available time is the maximum completion time of the scheduled jobs on the two test heads.

LOT OPTIMIZATION HEURISTIC



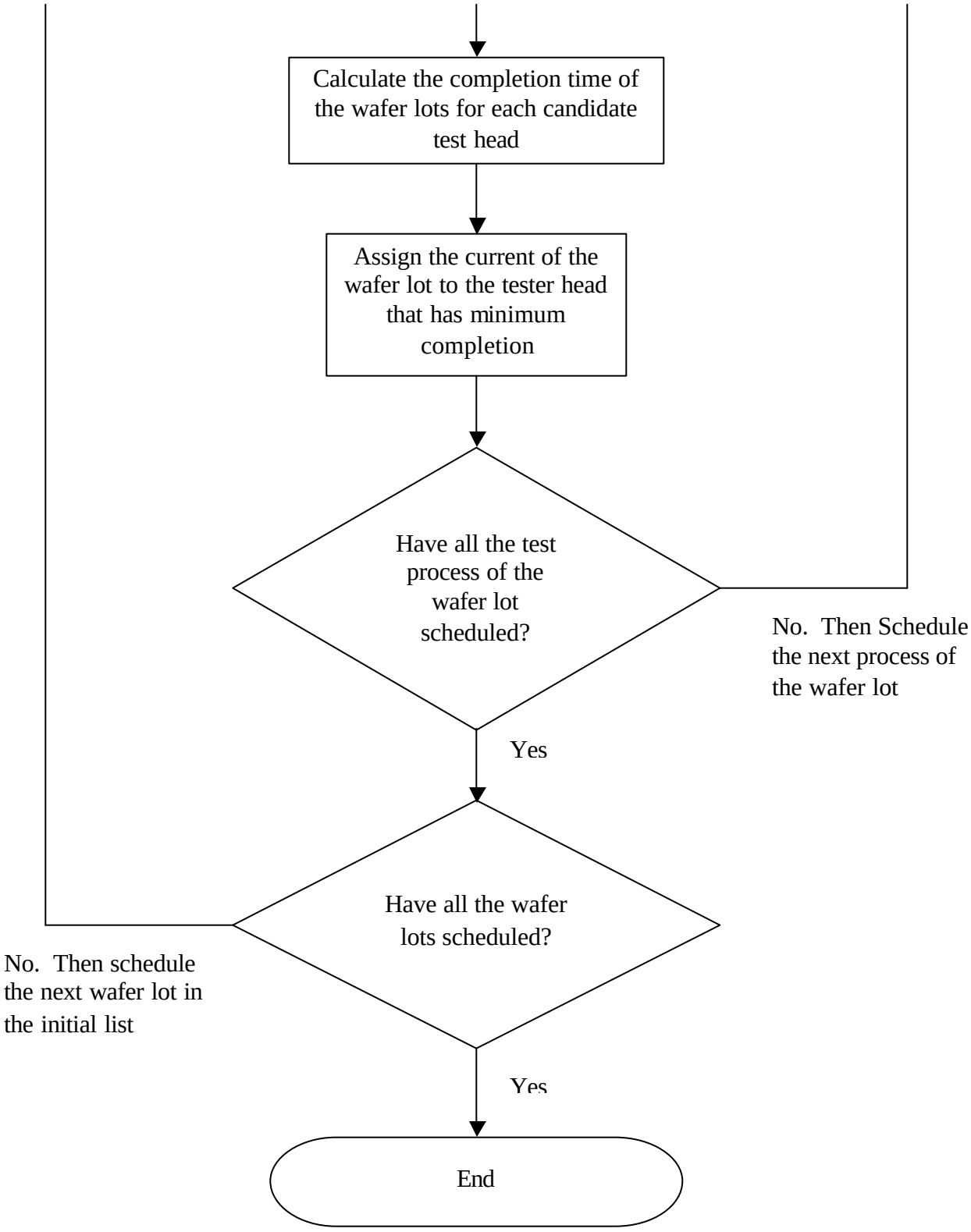


Figure 5-1. Lot Optimization Flow Chart

5.2 Processing Optimization (PO) Solution Approach

The process optimization approach focuses on maximizing the test station utilization by scheduling the same types of wafer test processes together. The process optimization method also involves constructing an initial list of wafer lots and then applying a scheduling algorithm. The primary difference between the lot optimization solution approach and the processing optimization approach is the sequence of the initial list of wafer lots. After the initial list developed, the scheduling algorithm then schedules the wafer devices lot by lot. An overview of the initial list construction and the scheduling algorithm are described below, with a flow chart provided in Figure 5-2.

Initial Wafer Lot List Construction Steps

Step 1: For each wafer lot, divide the wafer lots into jobs according to the remaining test processes of the wafer lot so that each job consists of only one test process. For example, suppose a wafer lot has three remaining test processes: pretest 1 (high), pretest 2 (low), and post-fuse (high). In this case, three jobs are created, with one job for pretest 1 (high), one job for pretest 2 (low), and one job for post-fuse (high) test respectively.

Step2: Sort the wafer jobs by following parameters:

- Process
- Current lot status
- Wafer lot priority
- Shortest remaining processing time

The first sorting parameter is the process type. The jobs are sorted in the following order: pretest 1, pretest 2, post-fuse. The second sorting parameter is current process status. The wafer lots that are in-process are first and the wafer lots that are waiting are next. The third sorting parameter is wafer lot priority. The lots with higher priority appear earlier in the list. The fourth sorting parameter is the shortest remaining processing time, which is the time required to complete all the remaining test process for the wafer lot. The lots that have the shortest remaining processing time appear earlier in the list.

After Step 2, an initial wafer lot list that consists of lots that need to be scheduled is sorted by test process, process status, wafer lot priority, and remaining processing time. The scheduling algorithm used for the process optimization solution approach is basically the same as the algorithm presented in Section 5.1. A brief overview of the scheduling algorithm is presented as follows:

Scheduling Algorithm

Step 3: Set the initial test station setup configuration

Step 4: Choose the maximum allowed setup time (MAST)

Step 5: Calculate the setup time for each test head for the current job.

Step 6: Select the candidate test heads.

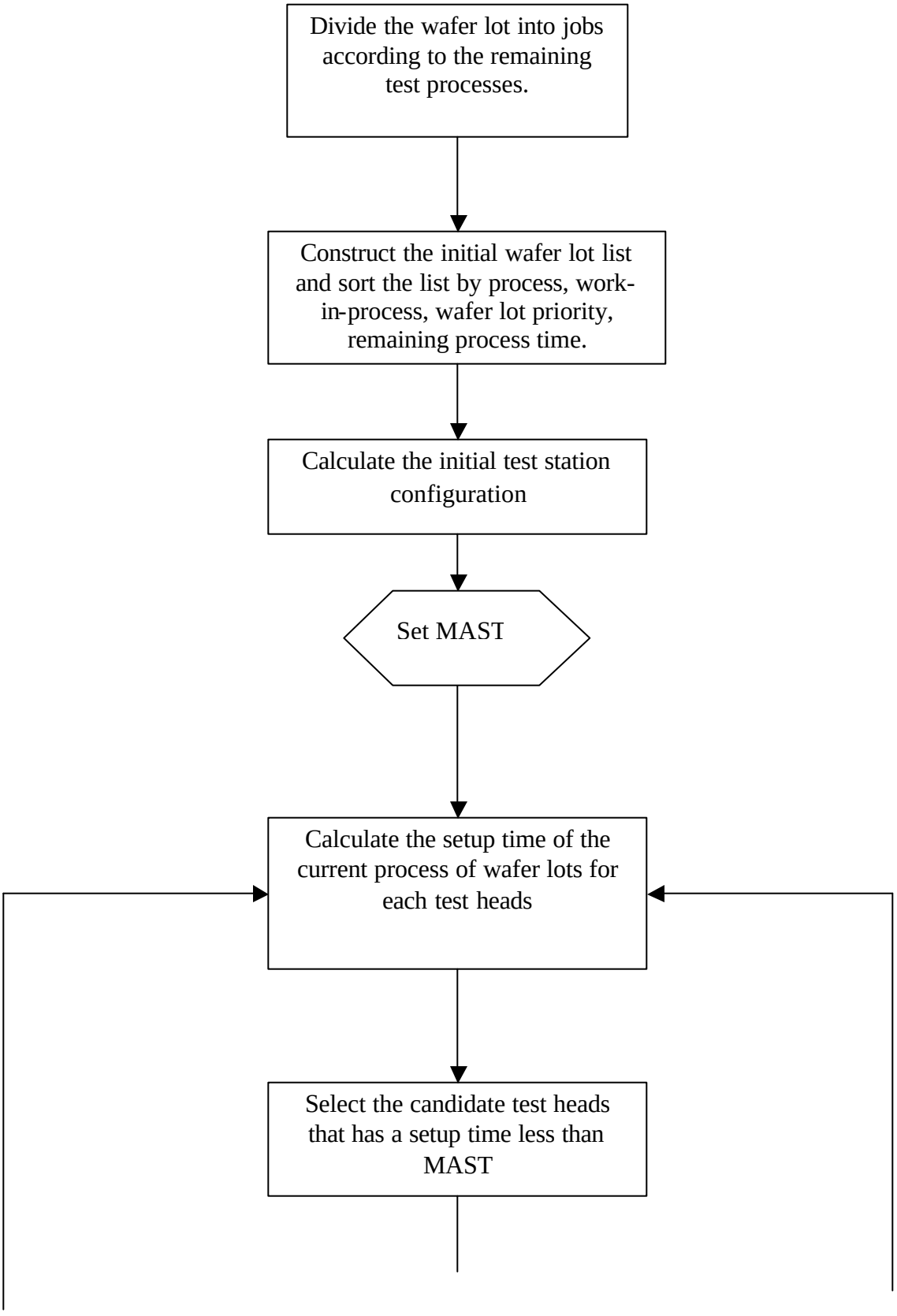
The candidate test heads that have setup times less than the value specified in Step 4 and are available for assigning the current job.

Step 7: Calculate the minimum completion time for each test head and assign the current job to test stations with minimum completion time

Step 8: Schedule the next job in the initial wafer lot list.

For each candidate test head selected in Step 6, the completion time of the job is calculated for each candidate test head. The current job is assigned to the test head with minimum completion time as determined by expression (5-1).

PROCESS OPTIMIZATION METHOD



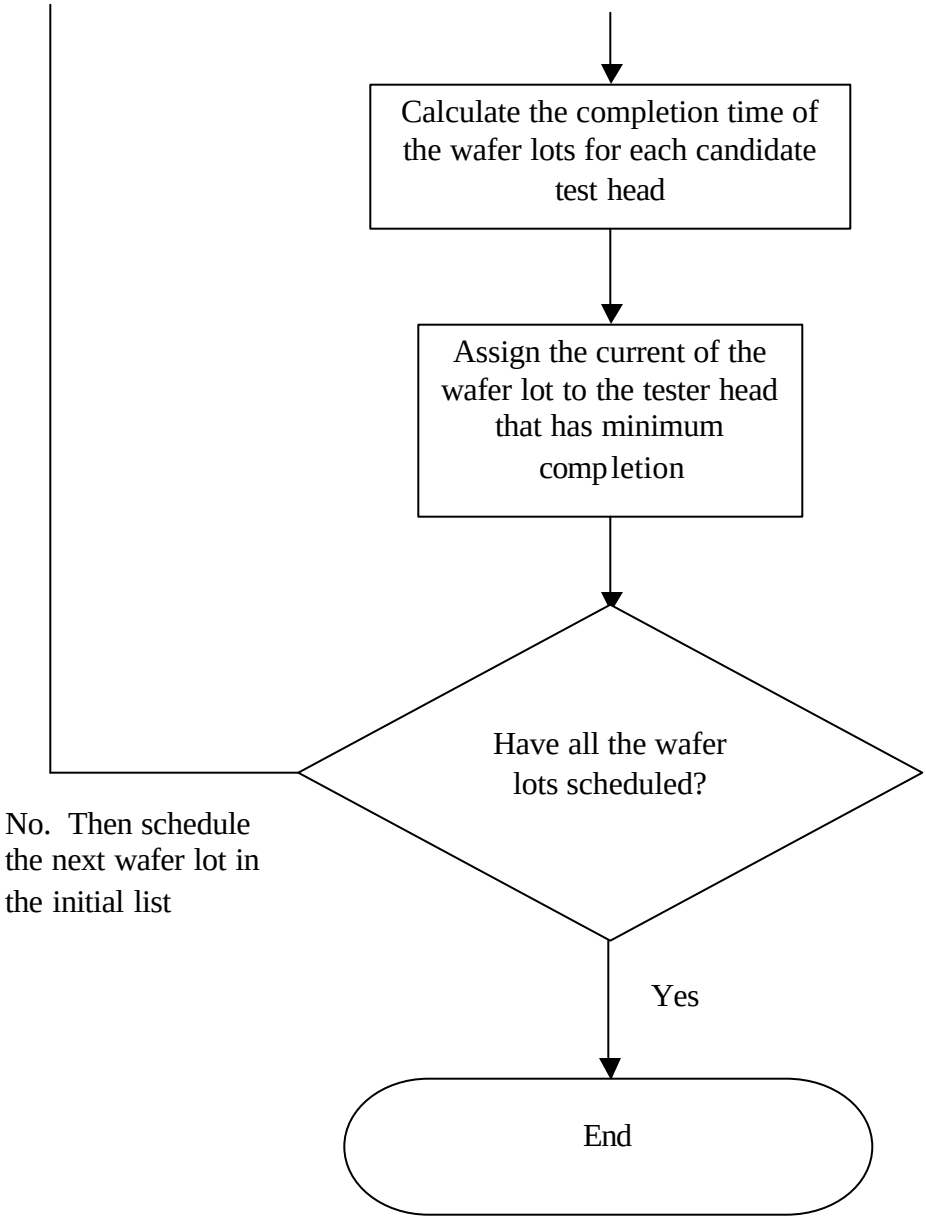


Figure 5-2. Processes Optimization Flow Chart

5.3 Solution Approaches With Tester Constraints

In the actual manufacturing environment, there are two types of test stations in the testing facility, Asia test station and Teradyne test stations. Because the specifications of these two types of test stations are different, a constraint is applied when assigning a wafer lot to the test stations. The constraint is described as follows:

- If the pretest 1 (high) of a wafer lot is performed on a specific test station type (such as Asia), then the pretest 2 (low) of the wafer lot must also be performed on the same type test station (such as Asia)
- The post-fuse (high) test of a wafer lot can be performed on either type of test stations regardless of the test station type of its previous test processes.

Thus, the pretest 2 (low) test process of a wafer lot must be performed on a test station that is the same type as the station where the pretest 1 (high) test process of the wafer lot is performed.

Due to this test station constraint, the selection criteria for the candidate test head is modified accordingly. When assigning a wafer lot to a test head for pretest 2 (low) test operation, the candidate test heads must be the same type as the test heads where the pretest 1 (high) test process of wafer lot was performed. This modification affects the scheduling of the test heads for both the lot optimization solution approach (Step 6) and process optimization solution approach (Step 6), and results in two additional solution approaches. The two solution approaches are *lot optimization solution approach with tester constraint* and *process optimization solution approach with tester constraint*. This test station constraint exists in the actual manufacturing environment at present, but will likely be relaxed soon. Thus, the two new solution approaches for the test station constraint are suitable for the actual shop floor for the moment, and the two solution approaches without tester constraint are suitable for the future.

5.4 Calculation of Suggested Test Station Configuration and Lower Bound

The solution approaches presented in this chapter generate different schedules based on the initial test station setup configuration. In order to use the solution approaches, a suggested initial test station setup configuration is required. The determination of the suggested test station configuration is presented in this section.

The basic idea for the suggested test station setup configuration is obtained from the situation when no setup up change is allowed. In this case, it is preferable to allocate the test stations in proportion to the processing time of each test operation for the waiting wafer lots. Thus, the general suggested initial test station configuration is to allocate the number of test stations for each test process in proportion to the remaining processing time for each of the processes.

The suggested initial number of test stations for wafer type t and process p (TS_{tp}) is calculated with the following expression:

$$TS_{tp} = K * \frac{\sum_{l \in L_t} PT_{lp}}{\sum_{L}\sum_{P} PT_{lp}} \qquad (5\text{-}3)$$

where

L= Indexed set of lots, **L**={1,2,…l..,L}

P= Indexed set of processes, **P**={1,2,…p..,P}

T= Indexed set of job types, **T**={1,2…t,…T}

$\mathbf{L_t}$= Indexed set of lots of type t

K= Number of test heads

PT_{lp}= Processing time of lot l process p

TS_{tp}=Number of test stations for wafer type t and test process p

For this research, the setup time required for a test station to change from pretest 1 (high) or post-fuse (high) to pretest 2 (low) test process is about 4 hours, whereas the setup time required for a test station to change between pretest 1 (high) and post-fuse (high) is only about 0.15 hours. In order to reduce setup time, the number of the test stations for pretest 2 (low) in expression 5-3 is rounded up to the nearest integer value to avoid the pretest 2 (low) test process becoming bottleneck (by requiring a test station setup and increasing the setup time.)

Expression (5-3) is suitable for a general production situation, in which the number of the wafer lots is more than half of the number of test heads. In the situation where the total number of wafer lots to be scheduled (L) is less than half the number of total test heads, the initial test station configuration can be constructed easily by assigning the number of test stations for pretest 1 (high) and pretest 2 (low) process equal to the number of wafer lots of each product, and the remaining test heads are set to post-fuse (high). The initial test station configuration for this situation is determined as follows:

$$TS_{tp} = \begin{cases} |L_t| & \text{for } p=1 \\ |L_t| & \text{for } p=2 \\ \{K - \sum_t (TS_{t1} + TS_{t2})\} * (L_t / L) & \text{for } p=3 \end{cases} \qquad (5\text{-}4)$$

where

L= Indexed set of lots**, L**={1,2,…,l,..,L}

P= Indexed set of processes, **P**={1,2,…,p,..,P}

T= Indexed set of job types, **T**={1,2…,t,…T}

L_t= Indexed set of lots of type *t*

K= Number of test heads

TS_{tp}=Number of test stations for wafer type *t* and test process *p*

Calculation of Lower Bound for Makespan

In this research, a lower bound is developed on the makespan required to complete the testing for a set of wafer devices. The lower bound is expressed as follows:

$$LB = Max\left\{ Max_l \left(PT_{l1} + PT_{l2} + PT_{l3} + PT_{l,\,fuse}\right),\ \frac{\sum_l \sum_p PT_{lp}}{K} \right\} \qquad (5\text{-}5)$$

The first part of the expression is the processing time of the wafer lot that has greatest remaining processing time. This expression assumes that no setup time is required and that sufficient test stations are available for processing the wafer lot simultaneously. The second part of the expression is the total processing time for the wafer lots across all the test heads, where *K* is the total number of test stations. The maximum value determines the lower bound of the problem. The lower bound is used for evaluating the results obtained using the solution approaches.

5.5 Implementation of Solution Approaches

This section describes the implementation of the solution approaches in the actual manufacturing environment. The four solution approaches are implemented in software application called *Wafer Test Scheduler (WTS)* using Visual Basic. The implementation of the *Wafer Test Scheduler* consists of interfacing the program with manufacturing databases so that the needed data can be downloaded automatically, designing a user graphical user interface for the program, and providing reports for the final scheduling results. The *WTS* was implemented in an international semiconductor firm and tested on the shop floor.

5.4.1 Link to Database

In order to provide real time wafer lot and test station data for the solution approaches, the program is linked to the manufacturing database so that all the needed information can be obtained automatically. The semiconductor firm uses IBM DB2 as their database platform, and the databases used to store the test station and wafer lot information table are: DB2. FHTOOLST, DB2.FHTOOL, and DB2.FHLLOTB, which stores test station

information and wafer lot information respectively. Visual Basic's ActiveX Data Object (ADO) is used to link the databases and Standard Query Language (SQL) is used to obtain the needed data.

The obtained data are then stored in two tables that are part of the WST program. The test station information is stored in the Current Tool Status (CTS) table. The wafer lot information is stored in the Current Lots Status (CLS) table. These data are directly downloaded from the firms IBM DB2 database to be used with the solution approaches. These two tables are displayed in the initial form of the Wafer Test Scheduler. Figure 5-3 shows such a form, where the upper table shows the test station status, and the lower table shows the wafer lots status.

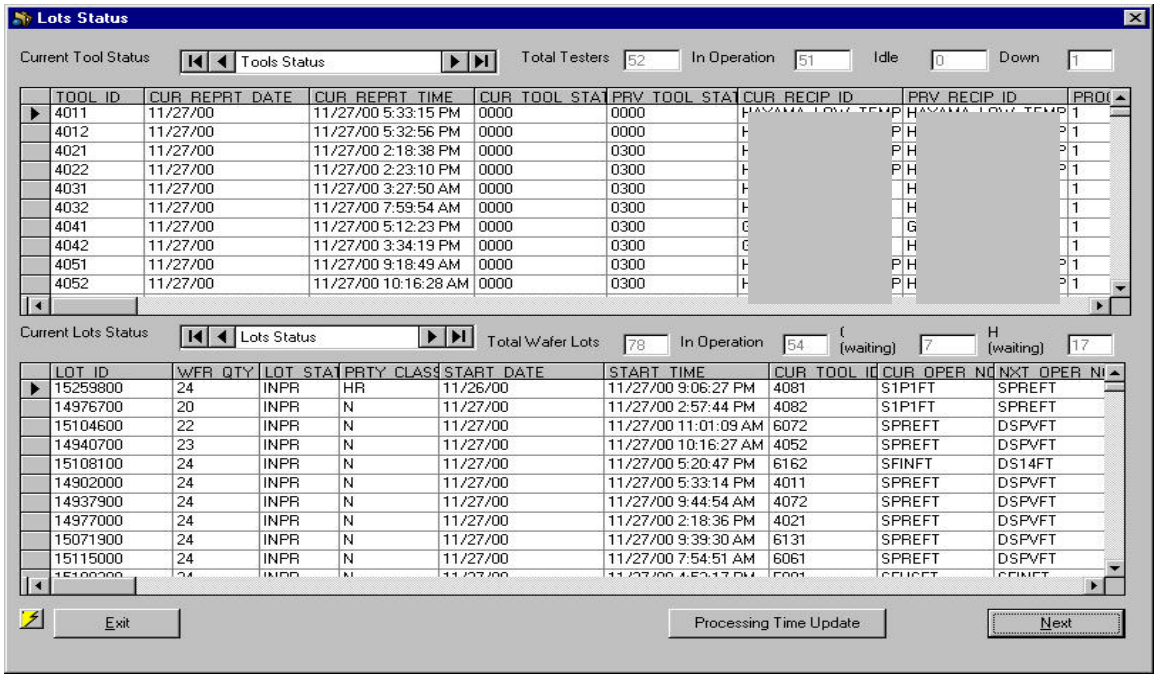


Figure 5-3. Initial Interface Form of Wafer Test Scheduler (WTS)

As shown in Figure 5-3, the basic information on the test heads displayed is total number test heads, number of test heads in operation, number of test heads idle, and number of test heads down. Likewise, the basic information on wafer lots is also shown including the number of wafer lots in process, number of Product G wafer lots that need to be scheduled, and number of Product H wafer lots that need to be scheduled.

5.4.2 Graphical User Interface for the Solution Approaches

A graphical user interface was developed to help the planners to use the four solution approaches as shown in Figure 5-4. The sections of the Graphical User Interface are labeled from A to H. The meaning of each labeled area is presented as follows:

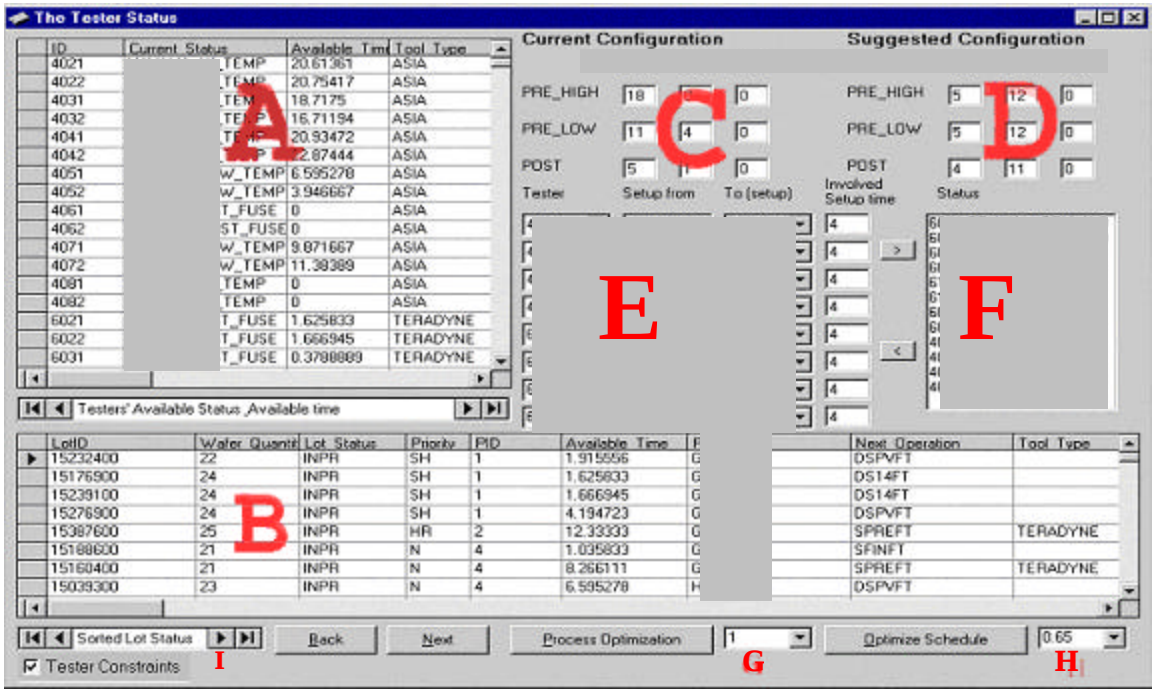


Figure 5-4. Graphical Interface for the Solution Approaches

A: Initial Test Heads Status

This table shows the needed test head information for the heuristic approaches. This table includes four fields: test head identifier, test head setup status, test head available time, and test head type. The test head available time is calculated based on wafer lot status and operation start time obtained from the two tables in the initial form as shown in Figure 5-3.

B: Initial Wafer Lot List

This table shows the sorted wafer lot list for the lot optimization solution approach as described in Section 5.1. When using the process optimization approach, this table will be re-sorted based on the rules presented in Section 5.2.

C: Current Test Head Setup Configuration

This area shows the current test head setup configuration, which is based on the information downloaded from the database.

D: Suggested Test Heads Setup Configuration

This area shows the suggested test heads setup configuration based on the information obtained from the table shown in area "B". The method for calculating the test head setup is presented in Section 5.4.

E: Choose Test Head to Change Setup

This area shows a set of *list box controls* to facilitate the setup change on selected test head to incorporate the suggested initial test head setup configuration. For example, when the current test heads setup configuration is different from the suggested test heads setup, the user uses these *list box controls* to change the setup status of certain test heads and enter the involved setup time for each selected test head.

F: Status of Setup Changes

This area shows the confirmed setup changes selected by the user. After selecting test heads for changing setup, the user clicks the button labeled ">"between areas "E" and "F" and the selected setup changes are added to area F. Another button labeled "<" is used to remove the undesired setup changes from the lists.

G: MAST Setting for Process Optimization

G is the list box control used for the selecting the MAST for the *process optimization approach*.

H: MAST Setting for Lot Optimization

H is the list box control used for the selecting the MAST for the *lot optimization approach*.

I: Tester Constraint Selection

Finally, the selection box in the lower left corner of Figure 5-4 is used to enable or disable the test station constraint for the solution approaches.

5.4.3 Scheduling Report

The Wafer Test Scheduler provides a scheduling report and Gantt chart after the scheduling approaches are executed. A sample of the report and Gantt chart are shown in Figure 5-5.

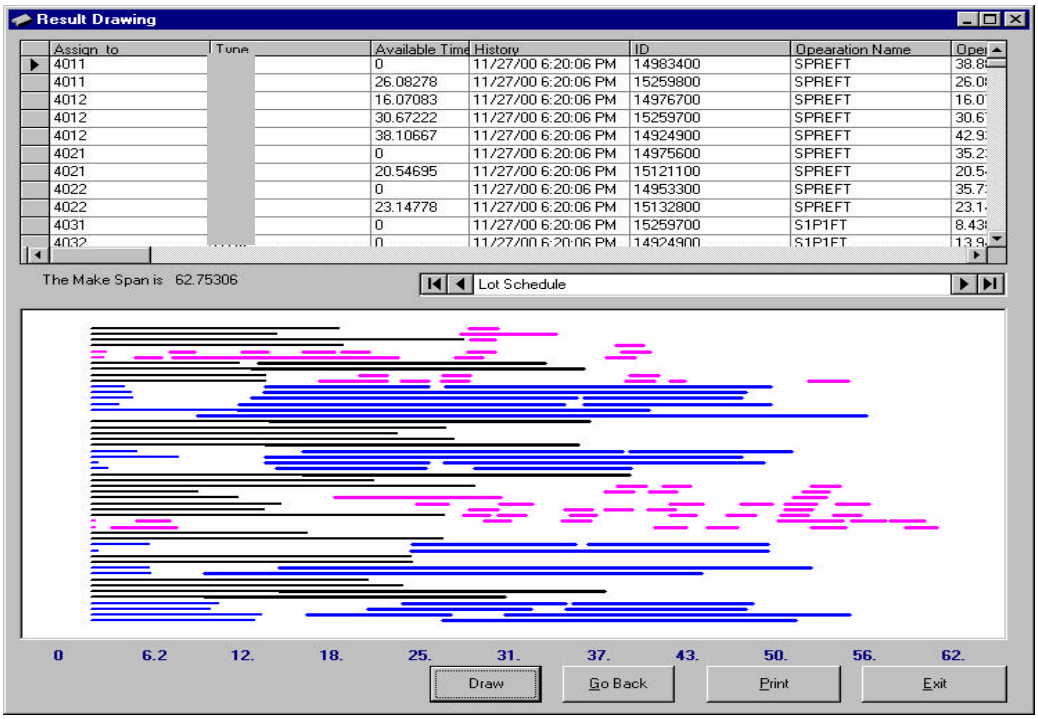


Figure 5-5. Resulting Scheduling Report

The remaining chapters of this thesis focus on evaluating the solution approaches using both experimental data and actual industrial data. Chapter VI presents a static case analysis in which the solution approaches are tested using experimental data. Chapter VII presents two case studies based on actual industrial data. The results obtained are then compared to the actual schedule implemented at the industrial site.

CHAPTER VI

ANALYSIS FOR STATIC SITUATION

In this chapter, a comprehensive analysis is conducted on the heuristics presented in the previous chapters. The primary purpose of the analysis is to determine the following for a given demand scenario:

1. Which heuristic performs best with respect makespan for a given demand scenario (demand level and product mix)?
2. For a given demand scenario and heuristic, what is the appropriate setting for the maximum allowed setup time (MAST) to minimize makespan?

The analysis is based on a static situation, where all the test stations are available and all the wafer devices are available for testing at the beginning of the horizon.

6.1 Analysis Profile

For this analysis, the scheduling scenario consists of 26 test stations, with 10 Asia test stations and 16 Teradyne test stations. Each test station has two test heads. Two different wafer types are evaluated in the analysis: Product G and Product H. Table 6-1 presents the test processing time for each wafer type for each test process. Each wafer lot may contain between 15 to 25 wafers.

Table 6-1. Test Processing Time for Each Wafer Type

Test Process	Product G	Product H
Pretest 1 (high)	58 minutes/wafer	58 minutes/wafer
Pretest 2 (low)	29 minutes/wafer	32 minutes/wafer
Fuse	5 minutes/wafer	6 minutes/wafer
Post-fuse (high)	7.2 minutes/wafer	7.2 minutes/wafer

The primary factors that impact the performance of the heuristics in developing test schedules are:

1. Product demand level;
2. Product mix of the demand; and
3. Maximum allowed setup time (MAST) for the schedule.

In order to determine how these factors affect the heuristic and the final schedule, experimental analyses are designed and conducted.

Product demand levels are varied to determine the impact of volume levels on the performance of the heuristics. The demand levels analyzed are 20 wafer lots, 60 wafer lots, and 100 wafer lots, which represent low, medium, and high product demand levels respectively. The two wafer types (Product H and Product G) are analyzed at varying mixes ((70% H, 30% G), (50% H, 50% G), (20% H, 80% G)). The following table summarizes product demand levels and product mixes.

Table 6-2. Product Demand Levels and Product Mixes

Product Demand	Product H	Product G
20 Wafer Lots	70%	30%
	50%	50%
	20%	80%
60 Wafer Lots	70%	30%
	50%	50%
	20%	80%
100 Wafer Lots	70%	30%
	50%	50%
	20%	70%

As described in Chapter II, setup time consists of prober card change time, temperature adapting time, and program download time. The maximum allowed setup time (MAST) is a parameter used in the heuristic that dictates the maximum setup time allowed for the schedule. Table 6-3 summarizes the maximum allowed setup time (MAST) used for the heuristics.

Table 6-3. Maximum Allowed Setup Time

MAST	Setup Time
0.00 hours	No setup time
0.15 hours	Software download time
0.50 hours	Prober card change time
0.65 hours	Software download time and Prober card change time
4.00 hours	Temperature change time
4.65 hours	Allow all setup

In this experimental analysis, a full factorial experiment results in 216 cases (3 demand levels, 3 product mixes, and 6 allowed setup times, and 4 heuristics). In each case, different product demand, product mix, and MAST are applied to generate schedules for each heuristic. The performance of the heuristics is evaluated using the following measures:

- Makespan
- Mean flow time (MFT)
- Average work in process (AWIP)

The makespan is the wafer lot completion time for a set of wafer lots. The mean flow time (MFT) is the average completion time of all the wafer lots. The average work-in-process (AWIP) is the number of wafer lots that are being processed in the testing facility. AWIP is estimated by summing the completion time of each wafer lot and dividing by the makespan.

Throughout this chapter, both graphical and statistical analysis are used to explain the experimental results. Graphical analysis illustrates the relationships between the factors and performance measures. Statistical analysis is used to confirm graphical results and provide conclusions regarding the best performing algorithm and appropriate MAST settings for the heuristics. Analysis of Variance (ANOVA) was performed to determine significant factors affecting each of the performance measure. Significance was determined for p-values ≤ 0.05. When appropriate, multiple comparisons of means were conducted using Tukey's pairwise comparisons to indicate relations between the factor

levels. MINITAB (Release 13.31) was used to perform the statistical analysis. The following sections describe the analysis for low demand, medium demand, and high demand level.

6.2 Analysis for Low Demand Levels

For low demand levels (20 wafer lots), each of the heuristics are evaluated for two wafer types (Product H and Product G) for three different product mixes (70% H, 30% G), (50% H, 50% G), and (20% H, 80% G).

6.2.1 Analysis for Low Demand and (70%, 30%) Product Mix

In this section, each of the four heuristics are analyzed for low demand with (70% H, 30% G) product mix. The suggested initial configuration is provided in Table 6-4. Since the number of wafer lots is less than half of the total number of test heads, the suggested initial test station configuration is determined by expression (5-4) and summarized in Table 6-4. For example, the number of test heads configured for pretest 1 (high) for Product H is obtained as:

$$TS_{H1} = \lceil L_H \rceil = 14$$

The number of test heads configured for pretest 1 (high) for Product G is obtained as:

$$TS_{G1} = \lceil L_G \rceil = 6$$

The method for setting the initial test configuration is shown in Figure 6-1. This suggested initial configuration will be used when analyzing the low demand with (70% H, 30% G) product mix.

Table 6-4. Suggested Initial Test Head Configuration for Low Demand with (70% H, 30% G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	14	6
Pretest 2 (low)	14	6
Post-fuse (high)	8	3

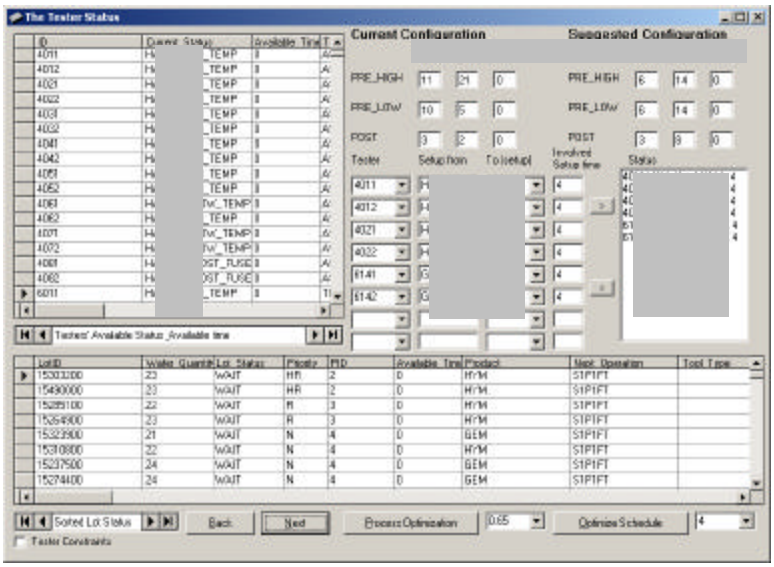


Figure 6-1. Setting the Initial Tester Configuration

As described in Chapter V, the lower bound of the makespan for this scenario is the total processing time of the wafer lot that has the greatest remaining processing time wafers. The lower bound assumes no setup time is required and that sufficient test stations are available for processing the wafer lots simultaneously. Thus, the lower bound is:

$$LB=\text{Max}\left\{ \text{Max}_l \left(PT_{l1}+PT_{l2}+PT_{l3}+PT_{l,\,fuse}\right),\ \frac{\sum_j \sum_p PT_{jp}}{K} \right\}$$

In this case, the lower bower bound is 43 hours. The makespan generated by the heuristics are compared to this lower bound. In the following sections, each of the four heuristics are analyzed for low demand with (70%, 30%) product mix using each of the six levels of MAST.

Lot Optimization Heuristic

The performance of the Lot Optimization (LO) Heuristic for all levels of MAST is summarized in Table 6-5. The LO Heuristic generates a schedule with a makespan of 43.65 hours at MAST settings of 0.65, 4.00, and 4.65 hours. This makespan is 1.51% away from the lower bound. The lower MAST settings appear to limit the flexibility and performance of the heuristic for a static situation. The larger MAST settings enable the

heuristic to consider additional alternatives and render better schedules. The MFT is also lower for the MAST settings for 0.65, 4.00, and 4.65 hours, whereas the AWIP levels are larger.

Table 6-5. Summary for Low Demand (70% H, 30% G) using LO Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	54.33	126.35%	44.79	16.49
0.15	54.33	126.35%	44.79	16.49
0.50	50.60	117.67%	44.79	17.70
0.65	43.65	101.51%	40.92	18.75
4.00	43.65	101.51%	40.92	18.75
4.65	43.65	101.51%	40.92	18.75

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-6. Again, the larger MAST settings generate the schedules with lower makespan. The MAST settings of 4.00 and 4.65 hours generate a makespan of 46.03 hours that is 7.05% above the lower bound. As expected, the makespan is longer than the makespan for the Lot Optimization Heuristic without the tester constraint. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, where as the AWIP levels are higher for these MAST settings.

Table 6-6. Summary for Low Demand (70% H, 30% G) using LOC Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	69.67	162.02%	47.75	13.71
0.15	69.67	162.02%	47.75	13.71
0.50	53.21	123.74%	45.50	17.10
0.65	51.83	120.53%	41.85	16.15
4.00	46.03	107.05%	41.27	17.93
4.65	46.03	107.05%	41.27	17.93

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-7. In this case, the PO Heuristic generates a schedule with a makespan of 43.65 hours. This makespan is 1.51% away from the lower bound and occurs with MAST settings of 0.5, 0.65, 4.00, and 4.65 hours. The lower MAST settings appear to limit the flexibility and performance of the heuristic for a static situation. The higher MAST settings enable the heuristic to consider additional alternatives and render better schedules. The MFT is lower and the AWIP levels are higher for these MAST settings. The makespan and MFT generated with PO Heuristic is the same as the makespan generated with LO Heuristic but the AWIP is higher.

Table 6-7. Summary for Low Demand (70% H, 30% G) using PO Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	51.83	120.53%	42.90	16.55
0.15	51.83	120.53%	42.90	16.55
0.50	43.65	101.51%	41.08	18.82
0.65	43.65	101.51%	41.08	18.82
4.00	43.65	101.51%	41.08	18.82
4.65	43.65	101.51%	41.08	18.82

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-8. In this case, the POC Heuristic generates a schedule with a makespan of 47 hours with MAST settings of 4.00 and 4.65 hours. This makespan is more than the makespan generated by LO Heuristic and the PO Heuristic (without tester constraint) and is 9.30% away from the lower bound. The MFT is lower for the MAST settings for 4.00 and 4.65 hours whereas the AWIP levels are higher for these settings.

Table 6-8. Summary for Low Demand (70% H, 30% G) using POC Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	66.98	155.77%	46.16	13.78
0.15	66.98	155.77%	46.16	13.78
0.50	51.88	120.65%	41.39	15.96
0.65	51.83	120.53%	41.39	15.97
4.00	47.00	109.30%	41.54	17.68
4.65	47.00	109.30%	41.54	17.68

Summary for the low demand (70%, 30%) scheduling with heuristic

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for low demand level with (70% H, 30% G) product mix. Figure 6-2 illustrates that both the LO and PO Heuristic generate schedules with low makespan and that the lowest makespans occur for the larger MAST settings. In fact, the LO and PO Heuristic generate schedules that are only 1.51% above the lower bound for makespan. This figure also illustrates that the heuristics with the tester constraint generate schedules with longer makespan than the heuristics without the tester constraint for comparable MAST settings. Figure 6-3 illustrates that the LO Heuristic generates schedules with lowest MFT and this occurs the higher MAST settings. Figure 6-4 illustrates that the heuristics generate schedules with higher AWIP levels at higher MAST settings.

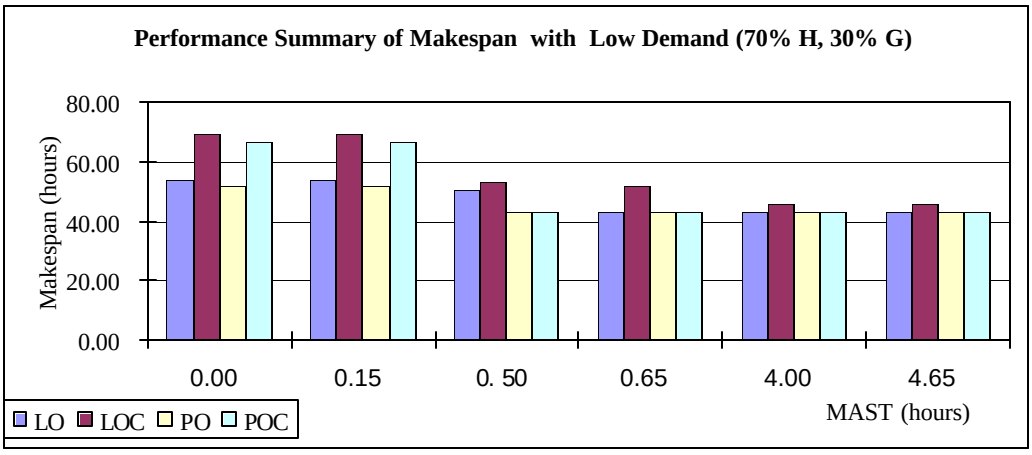


Figure 6-2. Summary of Makespan with Low Demand (70% H, 30% G)

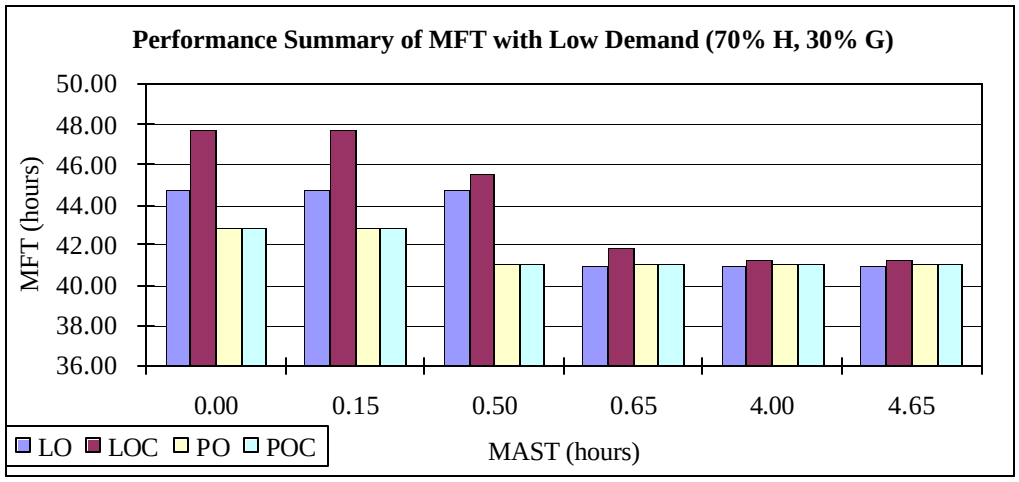


Figure 6-3. Summary of MFT with Low Demand (70% H, 30% G)

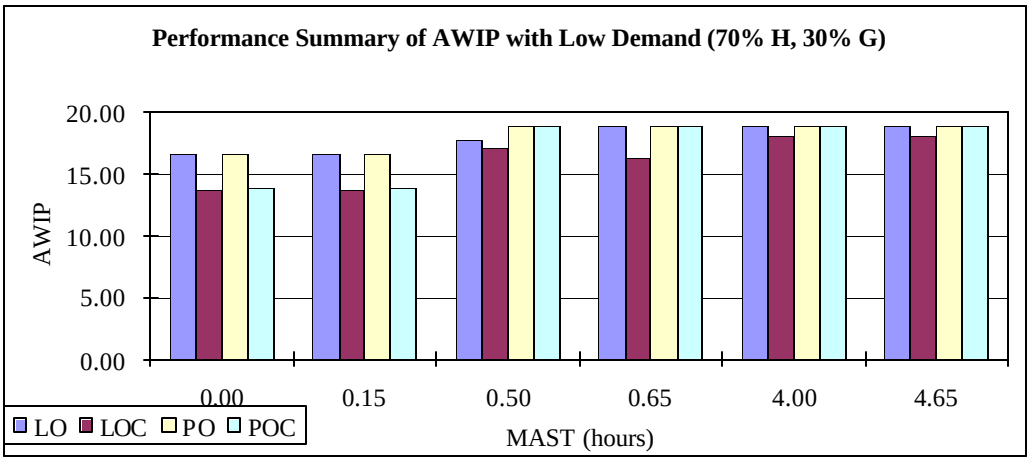


Figure 6-4. Summary of AWIP with Low Demand (70% H, 30% G)

From the above graphical analyses, we note that for low demand with a (70%, 30%) product mix:

1. Both LO and PO Heuristic methods generate schedules that are close to the lower bound with respect to the makespan (1.51% away from lower bound)
2. The tester constraint affects the heuristic and causes slightly longer makespan.
3. Higher MAST settings tend to generate better schedules with respect to makespan and MFT for the heuristics, but also result in higher AWIP.

To support the graphical analysis, analysis of variance (ANOVA) was conducted on the results for low demand with a (70%, 30%) product mix. The results indicate that both the heuristics (with p=0.009) and the MAST (with p=0.006) significantly affect makespan. Tukey's pairwise comparison indicates that the LO and PO Heuristics produce significantly lower values of makespan than the LOC Heuristic and POC Heuristics. Tukey's pairwise comparison also indicates that the higher MAST settings (0.5, 0.65, 4, and 4.65 hours) produce significantly lower values of makespan than the MAST settings of 0 and 0.15 hours.

6.2.2 Analysis for Low Demand and (50%, 50%) Product Mix

In the following sections, each of the four heuristics are analyzed for low demand with (50% H, 50% G) product mix. The initial tester configuration is determined by expression (5-4) and summarized in Table 6-9. For this case, the lower bound (as determined by expression (5-5)) is 43.00 hours.

Table 6-9. Suggested Initial Test Head Configuration for Low Demand with (50% H, 50%G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	10	10
Pretest 2 (low)	10	10
Post-fuse (high)	6	6

Lot Optimization Heuristics

The performance of the Lot Optimization Heuristic is summarized in Table 6-9. The LO Heuristic generates a schedule with a makespan of 43.15 hours. This makespan is 0.35% away from the lower bound and occurs with MAST settings of 0.65, 4.00, and 4.65 hours. This case analysis again illustrates that the LO Heuristic tends to generate the better schedules with respect to makespan when MAST is greater than or equal to 0.65 hours. The MFT is lower for the MAST settings of 0.65, 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-10. Summary for Low Demand (50% H, 50% G) using LO Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	51.83	120.53%	42.72	16.48
0.15	51.83	120.53%	42.72	16.48
0.50	50.04	116.02%	42.94	17.16
0.65	43.15	100.35%	40.49	18.77
4.00	43.15	100.35%	40.49	18.77
4.65	43.15	100.35%	40.49	18.77

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Test Constraint (LOC) Heuristic is summarized in Table 6-11. Again the larger MAST settings generate the schedules with lower makespan (47 hours). The makespan is longer than the makespan for the Lot Optimization Heuristic (without tester constraint) and is 9.30% away from the lower bound.

Table 6-11. Summary for Low Demand (50% H, 50% G) using LOC Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	56.33	131.00%	43.17	15.33
0.15	56.33	131.00%	43.17	15.33
0.50	52.68	122.51%	43.28	16.43
0.65	52.68	122.51%	41.40	15.72
4.00	47.00	109.30%	40.83	17.37
4.65	47.00	109.30%	40.83	17.37

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-12. In this case, the PO Heuristic generates a schedule with a makespan of 43.15 hours. This makespan is 0.35% away from the lower bound and occurs with MAST settings of 4.00 and 4.65 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-12. Summary for Low Demand (50% H, 50% G) using PO Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	48.68	113.21%	42.05	17.28
0.15	48.68	113.21%	42.05	17.28
0.50	47.36	110.14%	42.24	17.84
0.65	47.36	110.14%	42.24	17.84
4.00	43.15	100.35%	40.52	18.78
4.65	43.15	100.35%	40.52	18.78

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-13. In this case, the POC Heuristic generates a schedule with a makespan of 46.03 hours with MAST settings of 4.00 and 4.65 hours. This makespan is greater than the makespan generated by PO Heuristic (without tester constraint) and is 7.05% away from the lower bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas the AWIP levels are higher for these settings.

Table 6-13. Summary for Low Demand (50% H, 50% G) using POC Heuristic

MAST	Makespan	Performance Measure against Lower Bound	MFT	AWIP
0.00	54.33	126.35%	43.14	15.88
0.15	54.33	126.35%	43.14	15.88
0.50	51.83	120.53%	43.20	16.67
0.65	51.83	120.53%	43.20	16.67
4.00	46.03	107.05%	40.86	17.75
4.65	46.03	107.05%	40.86	17.75

Summary for Low Demand with (50%, 50%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for low demand level with (50% H, 50% G) product mix. Figure 6-5 illustrates that both the LO and PO heuristic generate schedules with low makespan and that lowest makespans occur at larger MAST settings. In fact, the LO and PO Heuristics generate schedules that are only 0.35% above the lower bound for makespan. This figure also

illustrates that the heuristics with the tester constraint generate schedules with longer makespan than the heuristics without the tester constraint. Figure 6-6 illustrates that the LO Heuristic generates schedules with lowest MFT and this occurs the higher MAST settings. Figure 6-7 illustrates that the heuristics generate schedules with higher AWIP at higher MAST settings.

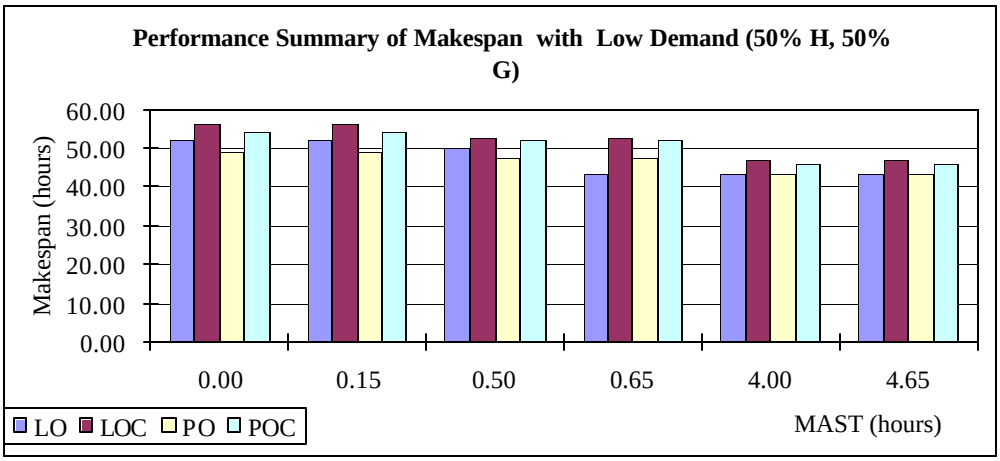


Figure 6-5. Summary of Makespan with Low Demand with (50% H, 50% G)

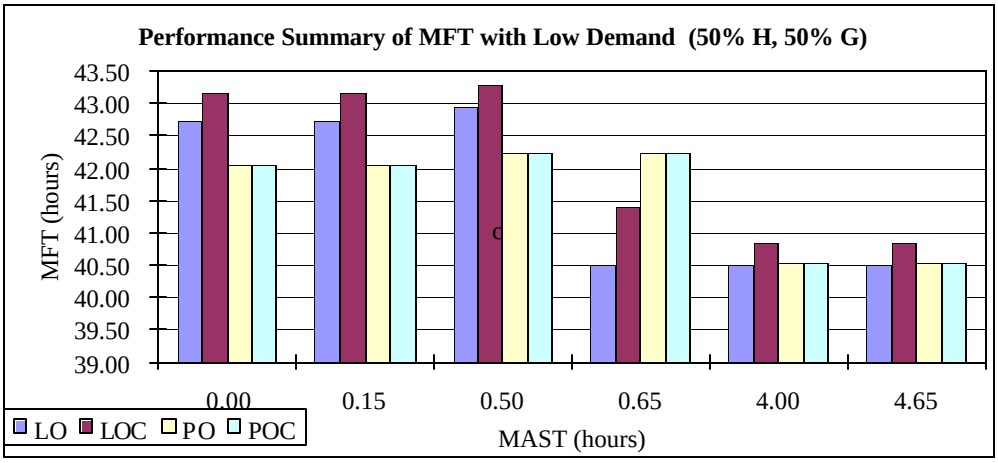


Figure 6-6. Summary of MFT with Low Demand with (50% H, 50% G)

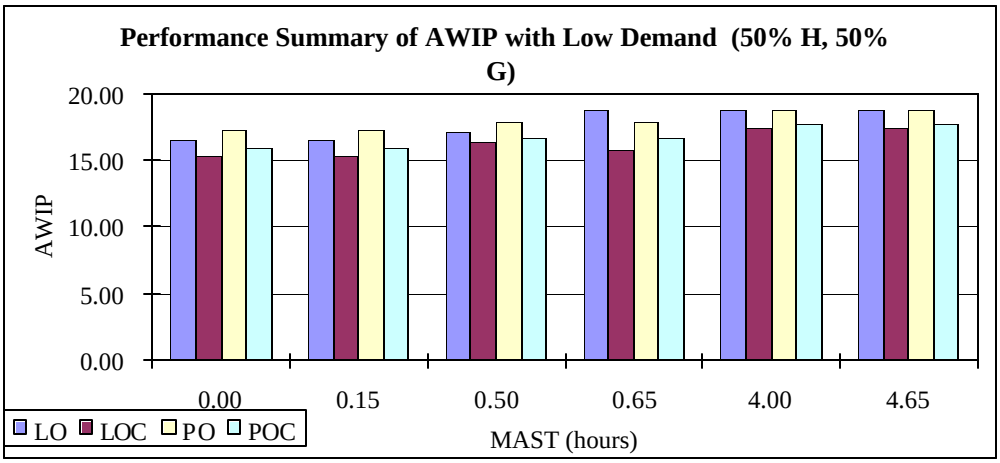


Figure 6-7. Summary of AWIP with Low Demand with (50% H, 50% G)

From the graphical analysis presented in this section, we note that for low demand level with a (50%, 50%) product mix:

1. Both the LO and PO Heuristic methods generate schedule that are close to the lower bound with respect to makespan (0.35% above the lower bound)
2. The tester constraint affects the heuristic and causes slightly longer makespan.
3. Allowing higher MAST tends to generate better schedules with respect to makespan for the heuristics whereas also cause higher AWIP.

To support the graphical analysis, analysis of variance (ANOVA) was conducted on the result for low demand with a (50%, 50%) product mix. The results indicate that both the heuristic (with p=0.009) and MAST (with p=0.006) significantly affect makespan. Tukey's pairwise compassion indicate that the LO and PO Heuristics produce significantly lower values of makespan than the LOC and POC Heuristics. Tukey's pairwise comparison also indicates that the MAST settings of 4.00 and 4.65 hours produce significantly lower values of makespan than the lower MAST settings of 0.65, 0.5, 0.15 and 0 hours.

6.2.3 Analysis for Low Demand and (20%, 80%) Product Mix

In the following sections, each of the four heuristics are analyzed for low demand with (20% H, 80% G) product mix. The initial tester configuration is determined by

expression (5-4) and summarized in Table 6-14. For this case, the lower bound (as determined by expression (5-5)) is 43.00 hours.

Table 6-14. Suggested Initial Test Head Configuration for Low Demand with (20% H, 80% G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	4	16
Pretest 2 (low)	4	16
Post-fuse (high)	2	10

Lot Optimization Heuristics

Table 6-15 summarizes the performance of the Lot Optimization Heuristic for this case. As before, MAST settings of 0.65, 4.00 and 4.65 hours generate the best schedules with respect to makespan. This makespan is 43.15 hours and is 0.35% away from the lower bound. The MFT is lower for the MAST settings of 0.65, 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-15. Summary for Low Demand (20% H, 80% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	64.58	150.18%	46.60	14.43
0.15	64.58	150.18%	46.60	14.43
0.50	49.28	114.60%	42.80	17.37
0.65	43.15	100.35%	40.49	18.77
4.00	43.15	100.35%	40.49	18.77
4.65	43.15	100.35%	40.49	18.77

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-16. Again the larger MAST settings generate the schedules with lowest makespan (45.83 hours). This makespan is greater than the makespan for the Lot Optimization Heuristic (without tester constraint) and is 6.58% away from the lower

bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-16. Summary for Low Demand (20% H, 80% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	64.68	150.42%	46.60	14.41
0.15	64.68	150.42%	46.60	14.41
0.50	53.67	124.81%	43.37	16.16
0.65	53.67	124.81%	41.32	15.40
4.00	45.83	106.58%	40.54	17.69
4.65	45.83	106.58%	40.54	17.69

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-17. In this case, the PO Heuristic generates a schedule with a makespan of 43.15 hours. This makespan is 0.35% away from the lower bound and occurs with MAST settings of 0.5, 0.65, 4.00, and 4.65 hours. The MFT is lower for the MAST settings of 0.5, 0.65, 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-17. Summary for Low Demand (20% H, 80% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	87.73	204.02%	58.10	13.25
0.15	65.79	153.00%	50.34	15.30
0.50	43.15	100.35%	40.23	18.65
0.65	43.15	100.35%	40.23	18.65
4.00	43.15	100.35%	40.23	18.65
4.65	43.15	100.35%	40.23	18.65

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-18. In this case, the POC Heuristic generates a schedule with a makespan of 41.06 hours. This makespan is 6.58% away from the lower bound and

occurs with MAST settings of 4.00 and 4.65 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-18. Summary for Low Demand (20% H, 80% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	87.73	204.02%	58.10	13.25
0.15	65.79	153.00%	50.34	15.30
0.50	53.67	124.81%	42.57	15.86
0.65	53.67	124.81%	42.57	15.86
4.00	45.83	106.58%	41.06	17.92
4.65	45.83	106.58%	41.06	17.92

Summary for Low Demand with (20%, 80%) Product Mix

The performance of the four heuristics are compared with respect to makespan, MFT, and AWIP for low demand level with (20% H, 80% G) product mix. Figure 6-8 illustrates that both the LO and PO Heuristics generate schedules with low makespan and the lowest makespans occur at larger MAST settings. In fact, the LO and PO Heuristics generate schedules that are only 0.35% above the lower bound for makespan. This figure also illustrates that the heuristics with the tester constraint generate schedules with larger makespan than the heuristics without the tester constraint. Figure 6-9 illustrates that the LO Heuristic generates schedules with lowest MFT and this occurs with the higher MAST settings. Figure 6-10 illustrates that the heuristics generate schedules with higher AWIP at larger MAST settings.

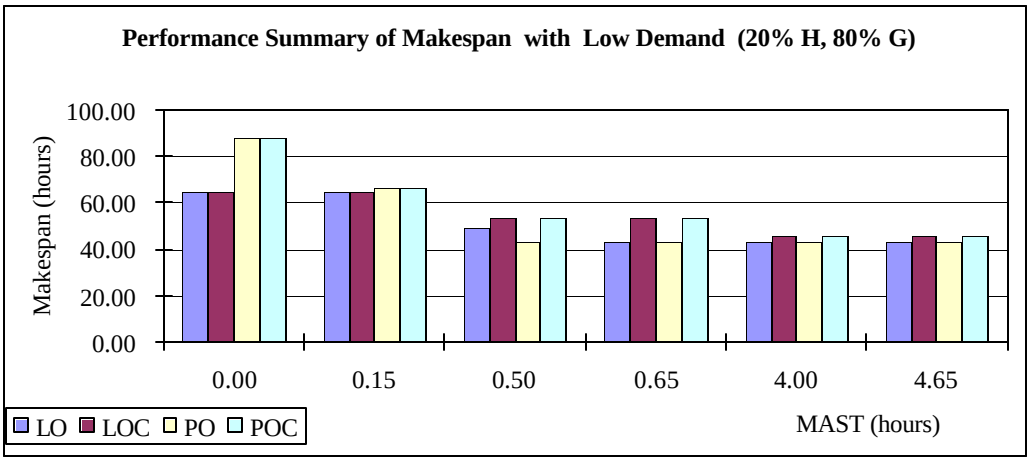


Figure 6-8. Summary of Makespan with Low Demand with (20% H, 80% G)

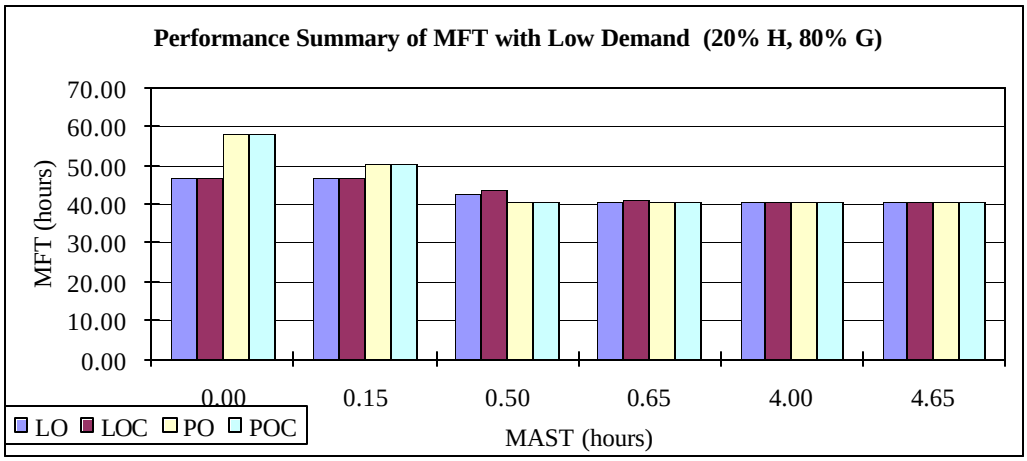


Figure 6-9. Summary of MFT with Low Demand with (20% H, 80% G)

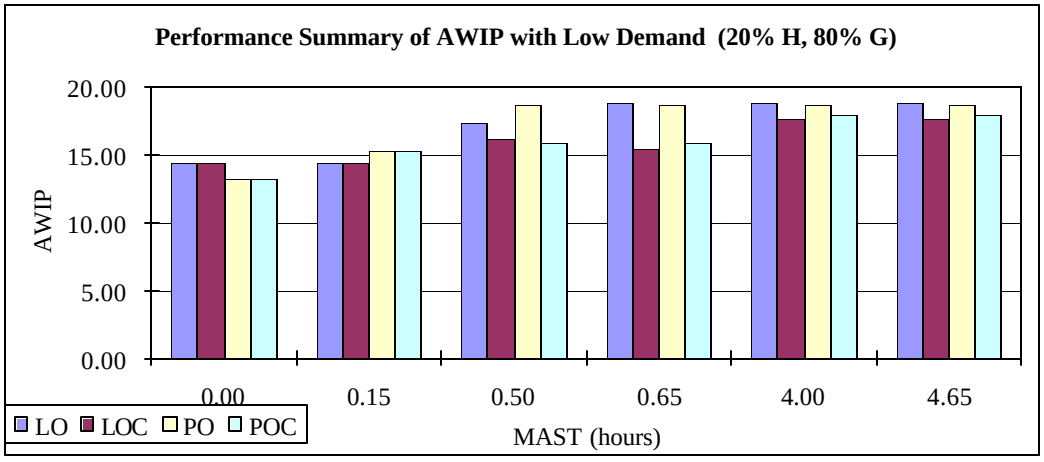


Figure 6-10. Summary of AWIP with Low Demand with (20% H, 80% G)

From the graphical analyses in this section, we note that for low demand level with a (20%, 80%) product mix

1. Both the LO and PO Heuristics generate schedules that are close to the lower bound with respect to makespan (0.35% above the lower bound)
2. Allowing a higher MAST tends to generate better schedule for both heuristics.

To support the graphical analysis, analysis of variance (ANOVA) was conducted on the results for low demand with (20%, 80%) product mix. The results indicate that the MAST level (with p=0.006) significantly affects makespan (The heuristic factor was significant at a p-value of 0.260). Tukey's pairwise comparison indicates that the MAST settings of 4.65, 4, 0.65 and 0.5 hours produces significantly lower values of makespan than the lower MAST settings of 0 and 0.15 hours.

6.2.4 Summary of Low Demand Analysis

The performance of the heuristic for low product demand across all three product mixes can be summarized as follows:

1. The heuristics can generate schedules that are very close to the lower bound, and an example schedule generated by the LO Heuristic is shown in Figure 6-14.
2. The tester constraint affects the heuristics and generates schedules with longer makespan.
3. Lower MAST limits the flexibility of the heuristics and causes longer makespan.

ANOVA was conducted for the data set of all experiments with low demand. The ANOVA results indicate that the interaction of product mix and MAST (p=0.000) significantly affect the makespan. Furthermore, the heuristic main effect (p=0.001) significantly affects makespan (along with the main effects of product mix and MAST). Tukey's pairwise comparison indicates that the LO and PO Heuristics produce significantly lower values of makespan than the LOC and POC Heuristics. Tukey's

pairwise comparison also indicates that for any mix, the higher MAST settings of 4 and 4.65 hours produce significantly lower values of makespan than the MAST setting of 0 hours.

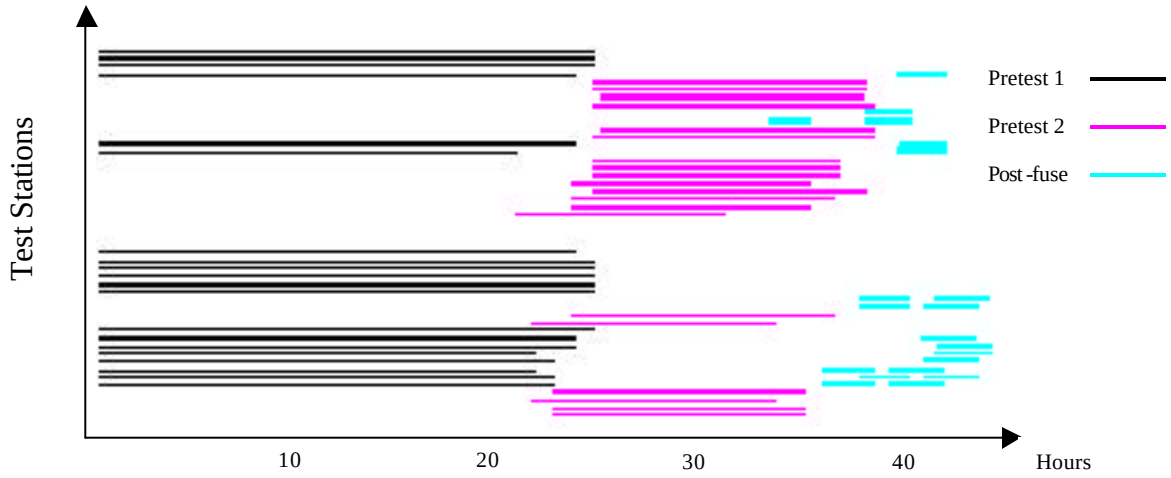


Figure 6-11. Schedule Generated for Low Demand (30% H , 70% G) using LO Heuristic with MAST=4.65 hours

6.3 Analysis for Medium Demand Levels

For medium demand levels (60 wafer lots), each of the heuristics are evaluated for two wafer types (Product H and Product G) for three product mixes (70% H, 30% G), (50% H, 50% G), and (20% H, 80% G). Since the number of the wafer lots is greater than the half the number of test heads (which is 26), the suggested initial test station configuration is obtained using expression (5-3). For each case analysis in this section, the initial test station configuration is set accordingly. Likewise, the lower bound for each case analysis is determined using expression (5-5).

6.3.1 Analysis for Medium Demand and (70%, 30%) Product Mix

In the following sections, each of the four heuristics are analyzed for medium demand with (70% H, 30%G) product mix. The initial tester configuration is determined by

expression (5-3) and summarized in Table 6-19. For this case, the lower bound (as determined by expression (5-5)) is 49.23 hours.

Table 6-19. Suggested Initial Test Head Configuration for Medium Demand with (70% H, 30% G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	22	10
Pretest 2 (low)	12	4
Post-fuse (high)	2	2

Lot Optimization Heuristics

The Summary of the Lot Optimization Heuristic is summarized in Table 6-20. The Lot Optimization Heuristic generates the lowest makespan schedule using a MAST setting of 0.5 hours, with a resulting makespan of 85.83 hours and AWIP of 44.02. The makespan is 74.34% away from the lower bound. The second best schedule with respect to makespan is generated using a MAST setting of 0.65 hours, with a resulting makespan of 90.37 hours and AWIP of 40.20. The lowest MFT occurs at a MAST setting of 0.65 hours while the highest AWIP levels occur at a MAST setting at 0.50 hours.

Table 6-20. Summary for Medium Demand (70% H, 30% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	101.97	207.13%	65.11	38.31
0.15	101.97	207.13%	65.11	38.31
0.50	85.83	174.34%	62.05	44.02
0.65	90.37	183.57%	60.55	40.20
4.00	98.89	200.87%	63.52	38.54
4.65	94.95	192.87%	63.39	40.06

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-21. As before, the MAST setting of 0.5 hours generates the schedule with best makespan (85.83 hours). The makespan is the same as the makespan

for the Lot Optimization Heuristic (without tester constraint) and is 74.34% away from the lower bound. The lowest MFT occurs at a MAST setting of 0.65 hours, while the highest AWIP level occur at a MAST setting of 0.50 hours.

Table 6-21. Summary for Medium Demand (70% H, 30% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	169.60	344.51%	85.37	30.20
0.15	169.60	344.51%	85.37	30.20
0.50	85.83	174.34%	63.15	44.15
0.65	96.91	196.85%	62.99	39.00
4.00	98.98	201.06%	64.56	39.14
4.65	94.65	192.26%	64.31	40.77

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-22. In this case, the PO Heuristic generates a schedule with a makespan of 65.23 hours. This makespan is 32.50% away from the lower bound and occurs with MAST settings of 4.00 hours and 4.65 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-22. Summary for Medium Demand (70% H, 30% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	92.27	187.43%	58.10	37.78
0.15	92.27	187.43%	50.34	32.73
0.50	79.65	161.79%	58.29	43.91
0.65	79.77	162.04%	57.71	43.41
4.00	65.23	132.50%	53.63	49.33
4.65	65.23	132.50%	53.63	49.33

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-23. In this case, the POC Heuristic generates a schedule with a

makespan of 68.95 hours using a MAST of 4.65 hours. This makespan is greater than the schedule than the schedule generated by PO Heuristic (without tester constraint) and is 40.06% away from the lower bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-23. Summary for Medium Demand (70% H, 30% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	107.10	217.55%	65.52	36.71
0.15	107.10	217.55%	63.10	35.35
0.50	81.93	166.42%	58.17	42.60
0.65	81.27	165.08%	58.53	43.21
4.00	69.73	141.64%	54.39	46.80
4.65	68.95	140.06%	54.17	47.14

Summary for Medium Demand with (70%, 30%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for medium demand level with (70% H, 30% G) product mix. Figure 6-12 illustrates that the PO Heuristic generates schedules with lower makespan across all MAST settings. The PO Heuristic generates schedules with lowest makespan at MAST setting of 4.00 and 4.65 hours and the LO Heuristic generates schedules with lowest makespan at a MAST setting of 0.5 hours. This figure also illustrates that the heuristics with the tester constraint generate schedules with longer makespan than the heuristics without the tester constraint. Figure 6-13 illustrates that the LO Heuristic generates schedules with lowest MFT with MAST setting of 0.5 hours. Figure 6-14 illustrates that the LO Heuristic has higher AWIP at MAST setting of 0.5 hours and PO Heuristic has higher AWIP at 4.65 hours setting.

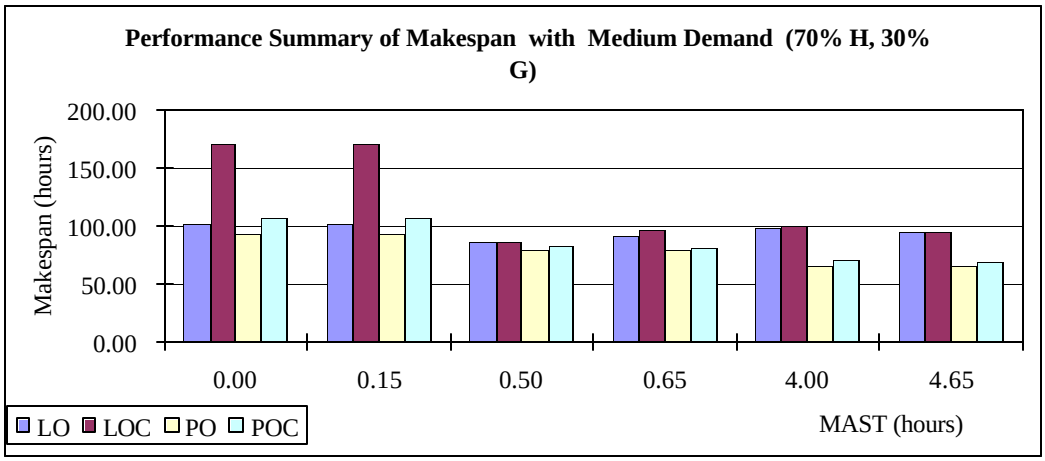


Figure 6-12. Summary of Makespan with Medium Demand with (70% H, 30% G)

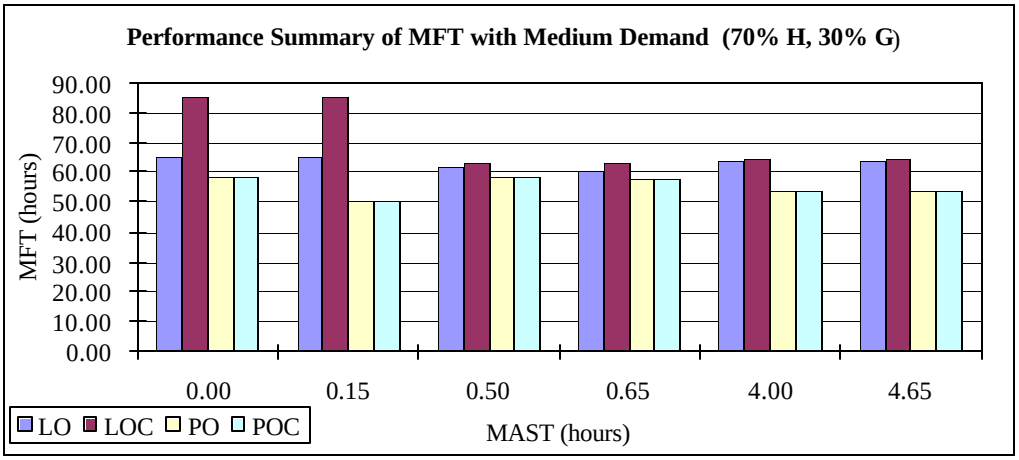


Figure 6-13. Summary of MFT with Medium Demand with (70% H, 30% G)

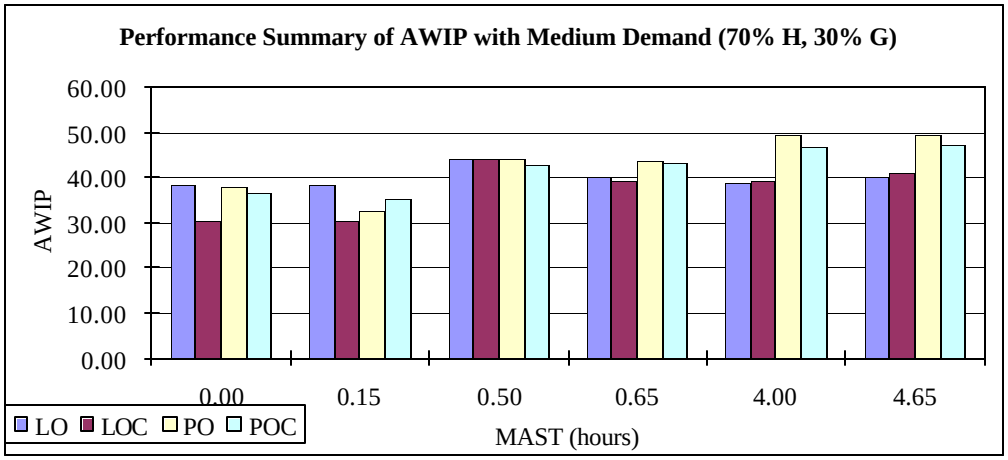


Figure 6-14. Summary of AWIP with Medium Demand with (70% H, 30% G)

From the above graphical analyses, we note that for medium demand with a (70%, 30%) product mix:

1. The PO Heuristic generates better schedule than LO Heuristics with respect to makespan for comparable MAST settings.
2. The PO Heuristics usually generate the best schedules with respect to makespan using a MAST of 4.00 hours or 4.65 hours.
3. The LO Heuristics usually generate the schedules with lower value of makespan using a MAST of 0.5 hours or 0.65 hours.

To support the graphical analysis, analysis of variance (ANOVA) was conducted on the results for medium demand with a (70%, 30%) product mix. The results indicate that both the heuristics (with p=0.003) and the MAST (with p=0.008) significantly affect makespan. Tukey's pairwise comparison indicates that the PO Heuristic and POC Heuristic produce significantly lower values of makespan than the LO Heuristic and LOC Heuristic.

6.3.2 Analysis for Medium Demand and (50%, 50%) Product Mix

In the following sections, each of the four heuristics are analyzed for medium demand with (50% H, 50%G) product mix. The initial tester configuration is determined by expression (5-3) and summarized in Table 6-24. For this case, the lower bound (as determined by expression (5-5)) is 49.62 hours.

Table 6-24. Suggested Initial Test Head Configuration for Medium Demand with (50% H, 50%G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	16	16
Pretest 2 (low)	8	8
Post-fuse (high)	2	2

Lot Optimization Heuristics

The performance of the Lot Optimization Heuristics is summarized in Table 6-25. The LO Heuristic generates a schedule with a makespan of 84.68 hours using a MAST setting of 0.5 hours. This makespan is 70.66% away from the lower bound. The second best schedule with respect to makespan is generated using a MAST setting of 0.65 hours, with resulting makespan of 89.95 hours and AWIP of 39.42. The lowest MFT occurs at a MAST setting of 0.65 hours, while the highest AWIP level occur at a MAST setting of 0.5 hours.

Table 6-25. Summary for Medium Demand (50% H, 50% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	89.00	179.36%	60.58	40.84
0.15	89.00	179.36%	60.58	40.84
0.50	84.68	170.66%	63.00	44.64
0.65	89.95	181.28%	59.70	39.82
4.00	99.95	201.43%	59.28	35.59
4.65	92.97	187.36%	62.37	40.25

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic for this case is summarized in Table 6-26. The LOC Heuristic generates a schedule with the lowest value of makespan (84.88 hours) using a MAST setting of 0.5 hours. The makespan is slightly higher than the makespan for the Lot Optimization Heuristic (without tester constraint) and is 71.06% away from the lower bound. The second best schedule with respect to makespan is generated using a MAST setting of 0.65 hours, with a resulting makespan of 92.33 hours and AWIP of 39.58. The lowest MFT occurs at a MAST setting of 0.65 hours, while the highest AWIP level occur at a MAST setting of 0.5 hours.

Table 6-26. Summary for Medium Demand (50% H, 50% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	133.23	268.50%	69.66	31.37
0.15	133.23	268.50%	69.66	31.37
0.50	84.88	171.06%	63.10	44.60
0.65	92.33	186.07%	60.91	39.58
4.00	103.53	208.65%	62.95	36.48
4.65	101.40	204.35%	62.95	37.25

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-27. In this case, the PO Heuristic generates a schedule with a makespan of 65.41 hours using a MAST setting of 4.65 hours. This makespan is 31.82% away from the lower bound. The second best schedule with respect to makespan is generated using a MAST setting of 4.00 hours, with resulting makespan at 65.88 hours. The MFT is lowest for the MAST settings of 4.00, whereas AWIP level is highest for a MAST setting at 4.65 hours.

Table 6-27. Summary for Medium Demand (50% H, 50% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	88.90	179.16%	62.83	42.40
0.15	86.30	173.92%	58.20	40.46
0.50	78.65	158.50%	57.79	44.09
0.65	78.65	158.50%	57.40	43.79
4.00	65.88	132.77%	53.55	48.77
4.65	65.41	131.82%	53.68	49.24

Process Optimization with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic for this case is summarized in Table 6-28. In this case, the schedule with lowest value of makespan is generated using a MAST setting of 4.65 hours, with resulting makespan of 65.38 hours. This makespan is slightly less than the schedule than the schedule generated

by PO Heuristic (without tester constraint) and is 31.76% away from the lower bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-28. Summary for Medium Demand (50% H, 50% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	170.88	344.38%	76.18	26.75
0.15	164.42	331.36%	70.98	25.90
0.50	79.70	160.62%	58.31	43.90
0.65	79.70	160.62%	58.27	43.87
4.00	65.88	132.77%	53.84	49.03
4.65	65.38	131.76%	53.74	49.32

Summary for Medium Demand (50%, 50%) Scheduling with Heuristics

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for medium demand level with (50% H, 50% G) product mix. Figure 6-15 illustrates that the PO Heuristic generates schedules with lower makespan across all MAST settings. The PO Heuristic generates schedules with lowest makespan at MAST setting of 4.65 hours and the LO Heuristic generates schedules with lowest makespan at MAST setting of 0.5 hours. This figure also illustrates that The PO and LO Heuristics with Tester Constraint has similar performance with respect to the lowest makespan as the PO and LO Heuristic without Tester Constraint for higher MAST settings. Figure 6-16 illustrates that the LO Heuristic generates schedules with lowest MFT with MAST setting of 0.65 hours and PO Heuristic generates schedules with lowest MFT with MAST setting of 4.00 hours. Figure 6-17 illustrates that the LO Heuristic generally has lower AWIP than he PO Heuristic at the comparable MAST settings. The highest AWIP levels occur for the PO and POC Heuristics at higher MAST settings.

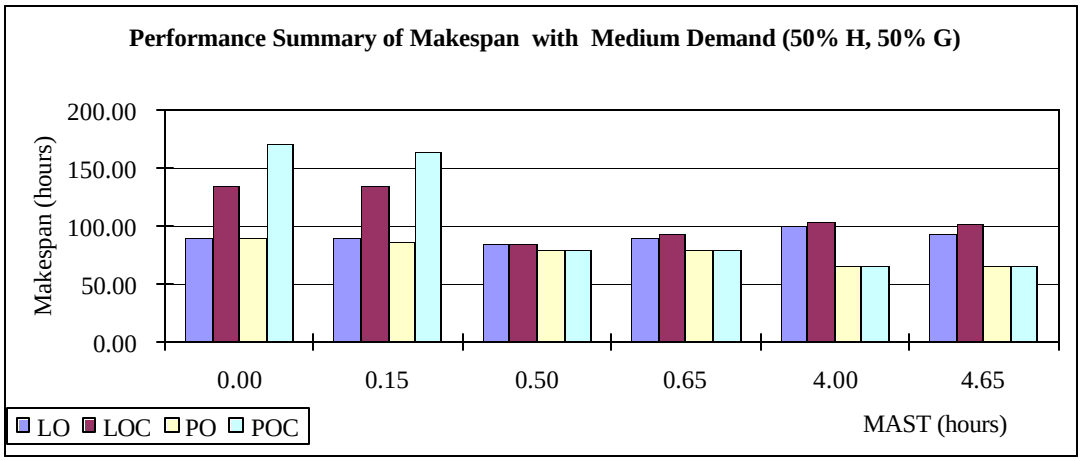


Figure 6-15. Summary of Makespan with Medium Demand with (50% H, 50% G)

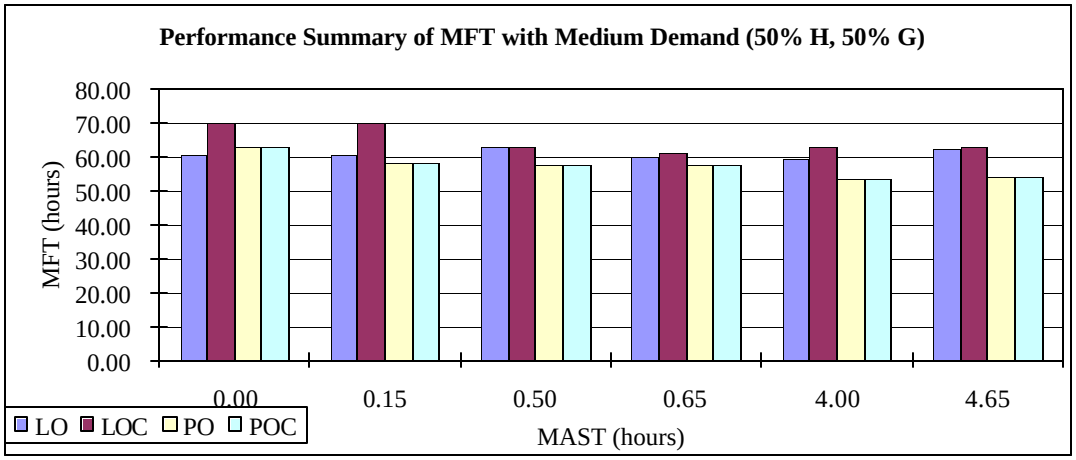


Figure 6-16. Summary of MFT with Medium Demand with (50% H, 50% G)

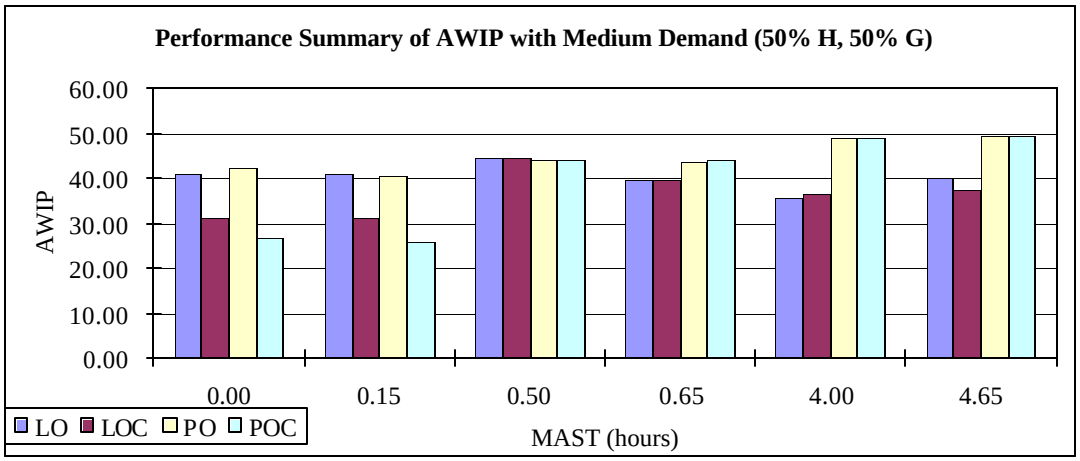


Figure 6-17. Summary of AWIP with Medium Demand with (50% H, 50% G)

From the graphical analysis, we note that for medium demand with (50%, 50%) product mix:

1. The PO Heuristics generates schedule with lower makespan than the LO Heuristics for comparable MAST settings.
2. The PO and LO Heuristics with Tester Constraint has similar performance with respect to the lowest makespan as the PO and LO Heuristic without Tester Constraint.

To supplement the graphical analysis, analysis of variance (ANOVA) was conducted on the results for medium demand with a (50%, 50%) product mix. The results indicate that neither MAST (with p=0.063) nor Heuristic (with p=0.127) significantly affect the makespan at a p-value of 0.05. Thus the differences noted in the graphical analysis are not statistically significant in this case.

6.3.3 Analysis for Medium Demand and (20%, 80%) Product Mix

In the following sections, each of the four heuristics are analyzed for medium demand with (20% H, 80% G) product mix. The initial tester configuration is determined by the expression (5-3) and summarized in Table 6-29. In this case, a lower bound of 50.19 hours (as determined by expression (5-5)) is used to compare with the makespan generated by the heuristics.

Table 6-29. Suggested Initial Test Head Configuration for Medium Demand with (20%, 80%)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	6	26
Pretest 2 (low)	4	12
Post-fuse (high)	2	2

Lot Optimization Heuristics

The performance of the Lot Optimization Heuristics is summarized in Table 6-30. The LO Heuristic generates a schedule with a makespan of 83.87 hours and AWIP of 43.98. This makespan is 67.10% away from the lower bound and occurs with a MAST setting of 0.5 hours. The second lowest value of makespan is generated using a MAST setting of 0.65 hours, with a resulting makespan of 88.70 hours and AWIP of 39.01. The lowest MFT occurs at a MAST setting of 0.65 hours, while the highest AWIP level occurs at a MAST setting of 0.5 hours.

Table 6-30. Summary for Medium Demand (20% H, 80% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	117.48	234.06%	72.62	37.09
0.15	117.48	234.06%	72.62	37.09
0.50	83.87	167.10%	61.48	43.98
0.65	88.70	176.72%	57.67	39.01
4.00	90.77	180.84%	59.75	39.50
4.65	90.77	180.84%	59.78	39.52

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-31. The lowest makespan is generated using a MAST setting of 0.5 hours, with resulting makespan of 83.87 hours. This makespan is the same as the makespan for the Lot Optimization Heuristic (without tester constraint) and is 67.10% away from the lower bound. The second lowest value of makespan is generated using a MAST setting of 0.65 hours, with resulting makespan of 89.70 hours and AWIP of 39.04. The lowest MFT occurs at a MAST setting of 0.65 hours, while the highest AWIP level occurs at a MAST setting of 0.5 hours.

Table 6-31. Summary for Medium Demand (20% H, 80% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	119.15	237.39%	75.58	38.06
0.15	119.15	237.39%	75.58	38.06
0.50	83.87	167.10%	61.56	44.04
0.65	89.70	178.71%	58.37	39.04
4.00	92.72	184.73%	60.37	39.07
4.65	92.72	184.73%	60.37	39.07

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-32. In this case, the PO Heuristic generates a schedule with a makespan of 63.57 hours using a MAST setting of 4.65 hours. This makespan is 26.65 % away from the lower bound. For this case, the MFT decreases as MAST increases, whereas AWIP increases as MAST increases. The lowest MFT and highest AWIP occurs at a MAST setting of 4.65 hours.

Table 6-32. Summary for Medium Demand (20% H, 80% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	135.10	269.16%	78.29	34.77
0.15	110.93	221.01%	67.43	36.47
0.50	77.63	154.67%	57.71	44.60
0.65	77.63	154.67%	57.71	44.60
4.00	65.18	129.86%	53.61	49.35
4.65	63.57	126.65%	52.69	49.73

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-33. In this case, the PO Heuristic generates a schedule with a makespan of 63.57 hours using a MAST setting of 4.65 hours. This makespan is the same as the makespan for the Process Optimization Heuristic (without tester constraint). For this case, the MFT generally decreases as MAST increases, whereas AWIP increases

as MAST increases. The lowest MFT and highest AWIP occurs at a MAST setting of 4.65 hours.

Table 6-33 Summary for Medium Demand (20% H, 80% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	135.10	269.16%	78.66	34.93
0.15	110.93	221.01%	77.82	42.09
0.50	128.73	256.47%	65.82	30.68
0.65	129.18	257.37%	70.08	32.55
4.00	67.58	134.64%	53.63	47.61
4.65	63.57	126.65%	52.46	49.51

Summary for Medium Demand with (20%, 80%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for medium demand with (20% H, 80% G) product mix. Figure 6-18 illustrates that the PO Heuristic generates the schedules with the lowest makespan at the higher MAST setting of 4.65 hours. The LO Heuristic generates schedules with lowest makespan at MAST setting of 0.5 hours but this makespan is greater than the best makespan generated by the PO Heuristic. This figure also illustrates that the POC and LOC Heuristics have similar performance with respect to the lowest makespan schedules generated as the PO and LO Heuristics. Figure 6-19 illustrates that the LO Heuristic generates schedules with lowest MFT with MAST setting of 0.65 hours and PO Heuristic generates schedules with lowest MFT with MAST settings of 4.00 and 4.65 hours. Figure 6-20 illustrates that the highest AWIP levels occur for the PO and POC Heuristics at the higher MAST settings of 4.00 and 4.65 hours.

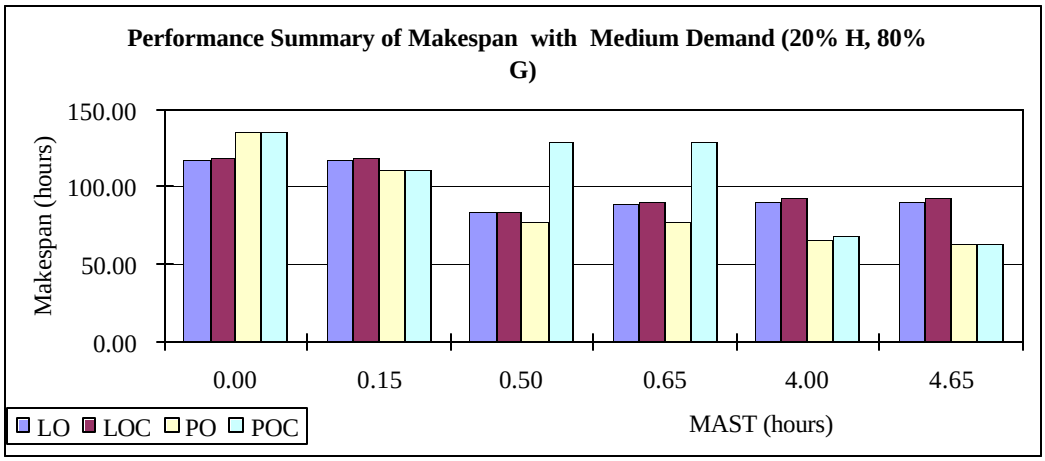


Figure 6-18. Summary of Makespan with Medium Demand with (20% H, 80% G)

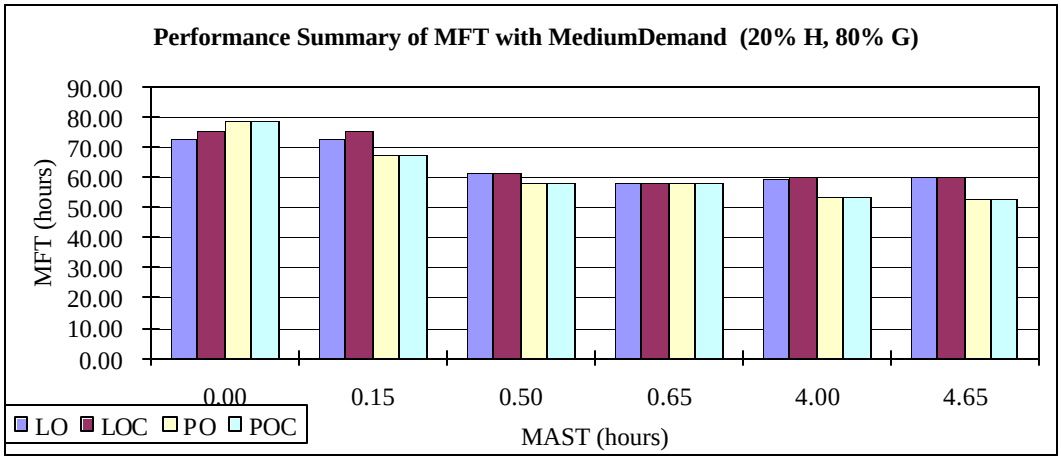


Figure 6-19. Summary of MFT with Medium Demand with (20% H, 80% G)

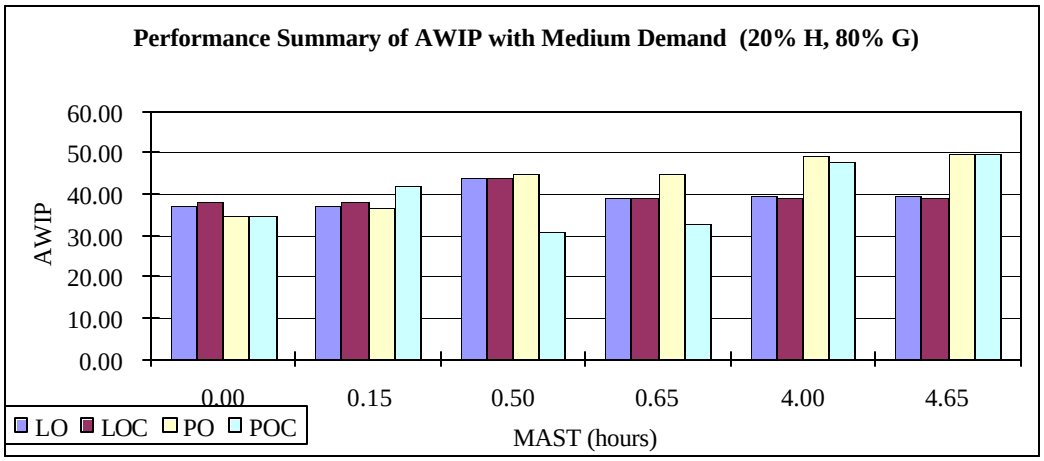


Figure 6-20. Summary of AWIP with Medium Demand with (20% H, 80% G)

From the graphical analysis, we note that for medium demand with (20%, 80%) product mix:

1. The PO Heuristics generates the best schedules with respect to makespan using a MAST of 4.00 hours or 4.65 hours.
2. The LO Heuristics usually generated the schedules with lower value of makespan using a MAST of 0.5 hours or 0.65 hours compare to other MAST settings.
3. The POC and LOC Heuristics have similar performance with respect to the lowest makespan schedule generated as the PO and LO Heuristics.

To support the graphical analysis, ANOVA was conducted on the results for the results for medium demand with a (20%, 80%) product mix. The results indicate that MAST (with p=0.008) significantly affects makespan (while the heuristic factor was only significant at the p =0.355 level). Tukey's pairwise comparison indicates that MAST settings of 4.00 and 4.65 hours are significantly better than MAST settings of 0, 0.15, 0.5 and 0.65 hours.

6.3.4 Summary for Medium Demand Analysis:

From the case analyses presented in this section, we summarize that for medium demand levels:

1. The PO Heuristic generates schedules with lower makespan than the LO Heuristic.
2. The PO Heuristic generates the best schedule with respect to makespan using MAST of 4.00 hours or 4.65 hours.
3. The heuristics have similar performance with respect to makespan on different product mix.

Typical schedules generated with MAST of 4.65 hours using PO Heuristic, and with MAST of 0.5 hours using LO Heuristic are shown in Figure 6-21 and Figure 6-22. ANOVA was conducted for the data set of all experiments with medium demand. The ANOVA results indicate that the heuristic (p=0.000) and MAST (p=0.000) factors significantly affect makespan. The mix factor was found to only be significant at a p-value of 0.793. Tukey's pairwise comparison indicates that the PO Heuristic produces

significantly lower values of makespan than POC or LOC Heuristic. Tukey's pairwise comparison also indicates that the MAST settings of 0.5, 0.65, 4, and 4.65 produce significantly lower values of makespan than 0 and 0.15 hours.

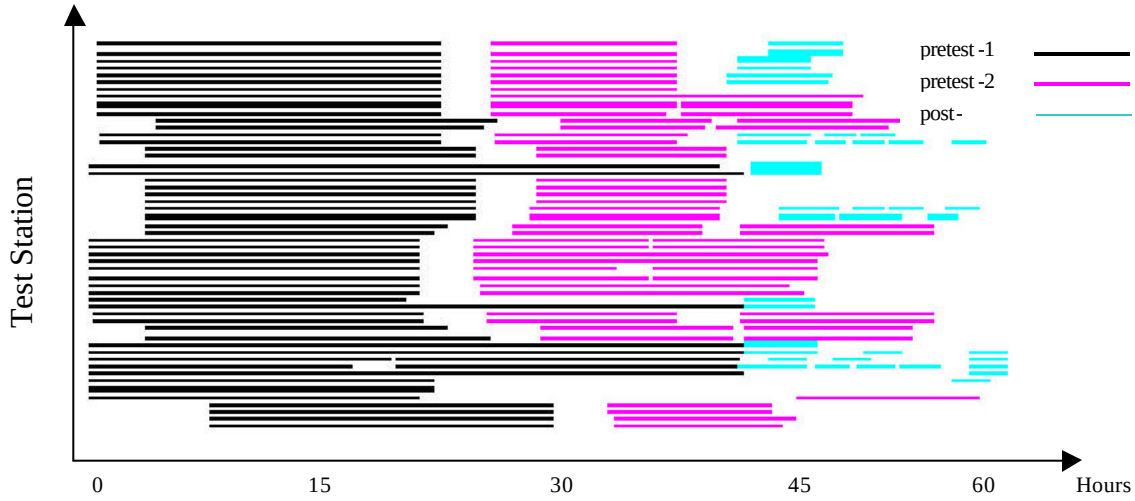


Figure 6-21. Schedule Generated for Medium Demand (20% H, 80% G) using PO Heuristic with a MAST of 4.65 hours

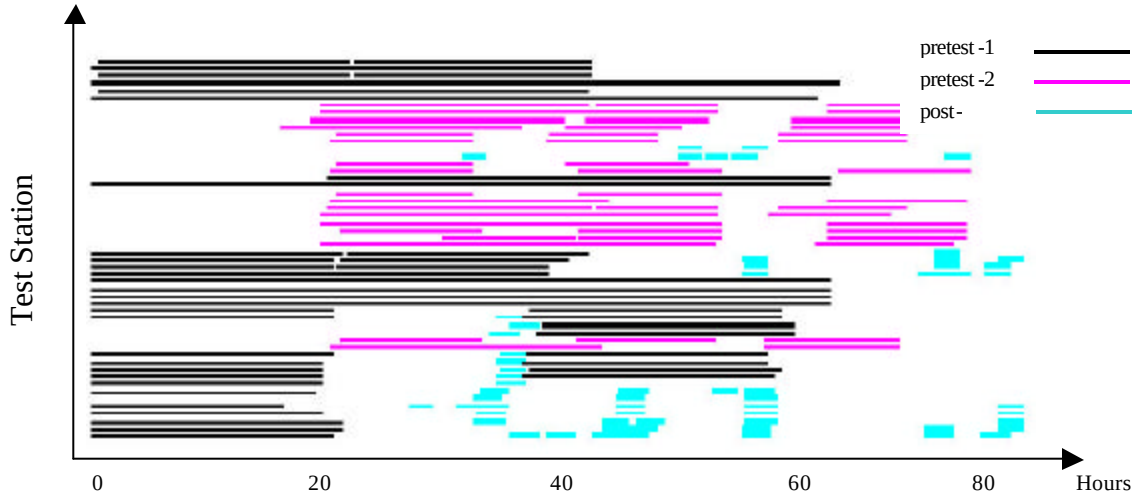


Figure 6-22. Schedule Generated for Medium Demand (20% H, 80% G) using LO Heuristic with a MAST of 0.5 hours

6.4 Analysis of High Demand Levels

For high demand levels (100 wafer lots), each of the heuristics are evaluated for two wafer type (Product H and Product G) for three different product mixes (70% H, 30% G), (50% H, 50% G), and (20% H, 80% G). The initial tester configuration is determined by the expression (5-3). For each case analysis in this section, the initial test station configuration is set accordingly. Likewise, the lower bound for each case analysis is determined using expression (5-5).

6.4.1 Analysis for High Demand and (70%, 30%) Product Mix

In the following sections, each of the four heuristics are analyzed for high demand with (70% H, 30% G) product mix. The initial tester configuration is determined by the expression (5-3) and summarized in Table 6-34. In this case, a lower bound of 82.05 hours (as determined by expression (5-5)) is used to compare with the makespan generated by the heuristics.

Table 6-34. Suggested Initial Test Head Configuration for High Demand with (70% H, 30%G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	24	8
Pretest 2 (low)	12	4
Post-fuse (high)	2	2

Lot Optimization Heuristic

The performance of the Lot Optimization Heuristics for all levels of MAST is summarized in Table 6-35. The best schedule with respect to makespan is generated using a MAST setting of 0.5 hours, with resulting makespan of 115.67 hours. The lowest MFT and the highest AWIP levels also occurs for the MAST setting of 0.5 hours.

Table 6-35. Summary for High Demand (70% H, 30% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	147.00	179.16%	86.46	58.82
0.15	147.00	179.16%	86.46	58.82
0.50	115.67	140.97%	77.08	66.64
0.65	135.33	164.93%	82.55	61.00
4.00	150.13	182.97%	89.21	59.42
4.65	150.13	182.97%	89.21	59.42

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table-36. The MAST setting of 0.5 hours generates the schedule with the lowest makespan (117.67 hours). The makespan is slightly greater than the makespan generated for the Lot Optimization Heuristic without the additional tester constraint and is 43.41% away from the lower bound. The lowest MFT and the highest AWIP levels also occurs for the MAST setting of 0.5 hours.

Table 6-36. Summary for High Demand (70% H, 30% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	146.87	179.00%	83.26	56.69
0.15	146.87	179.00%	83.26	56.69
0.50	117.67	143.41%	79.82	64.37
0.65	134.25	163.62%	81.46	56.47
4.00	152.38	185.71%	92.01	60.38
4.65	153.36	186.91%	92.42	60.26

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-37. In this case, the PO Heuristic generates a schedule with a makespan of 91.85 hours. This makespan is 11.08% away from the lower bound and occurs with a MAST setting of 4.0 hours. The second best makespan schedule is generated using a MAST setting of 4.65

hours, with resulting makespan of 92.28 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-37. Summary for High Demand (70% H, 30% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	132.6	161.61%	80.36	60.60
0.15	135.4	165.02%	80.18	59.22
0.50	107.15	130.59%	82.60	77.09
0.65	107.15	130.59%	82.44	76.94
4.00	91.85	111.94%	83.70	91.13
4.65	92.28	112.47%	84.78	91.87

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-38. In this case, the POC Heuristic generates a schedule with a makespan of 95.83 hours. This makespan is greater than the schedule than the schedule generated by PO Heuristic (without the tester constraint) and is 16.79% away from the lower bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-38. Summary for High Demand (70% H, 30% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	295.57	360.23%	113.17	38.29
0.15	282.23	343.97%	107.54	38.10
0.50	116.03	141.41%	83.41	71.89
0.65	116.03	141.41%	83.31	71.80
4.00	95.83	116.79%	84.16	87.82
4.65	96.71	117.87%	84.71	87.59

Summary for High Demand with (70%, 30%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for high demand level with (70% H, 30% G) product mix. Figure 6-23 illustrates

that the PO Heuristic generates schedules with lower values of makespan than the LO Heuristic for comparable MAST settings. The PO Heuristic generates schedules with lowest makespan at a MAST setting of 4.00 hours. The LO Heuristic generates schedules with lowest makespan at a MAST setting of 0.5 hours but this makespan is higher than the makespan generated by PO Heuristic. This figure also illustrates that the heuristics with the tester constraint generally generate schedules with longer makespan than the heuristics without the tester constraint. Figure 6-24 illustrates that the LO Heuristic generates schedules with lowest MFT at MAST setting of 0.5 hours. Figure 6-25 illustrates that the LO Heuristic has lower AWIP than the PO Heuristic at the comparable MAST settings. The highest AWIP levels occur for the PO and POC Heuristics at the higher MAST settings of 4.00 and 4.65 hours.

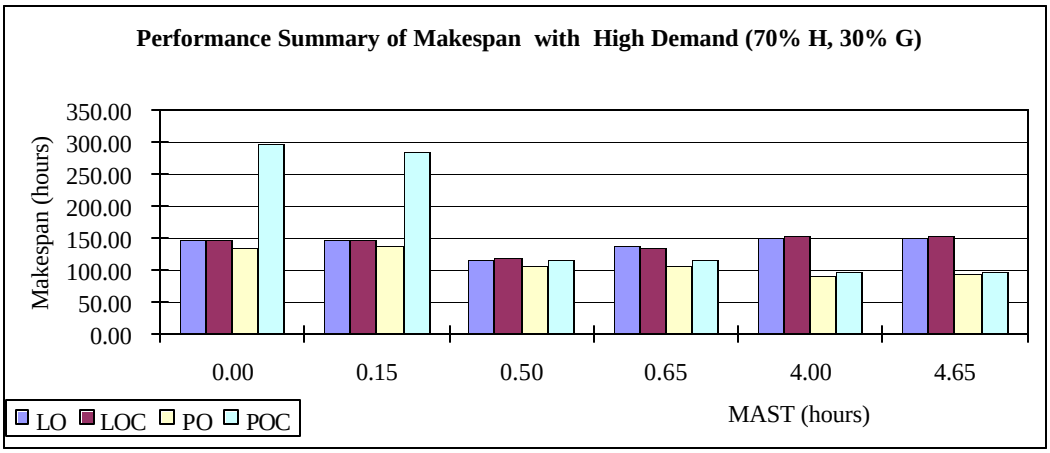


Figure 6-23. Summary of Makespan with High Demand with (70% H, 30% G)

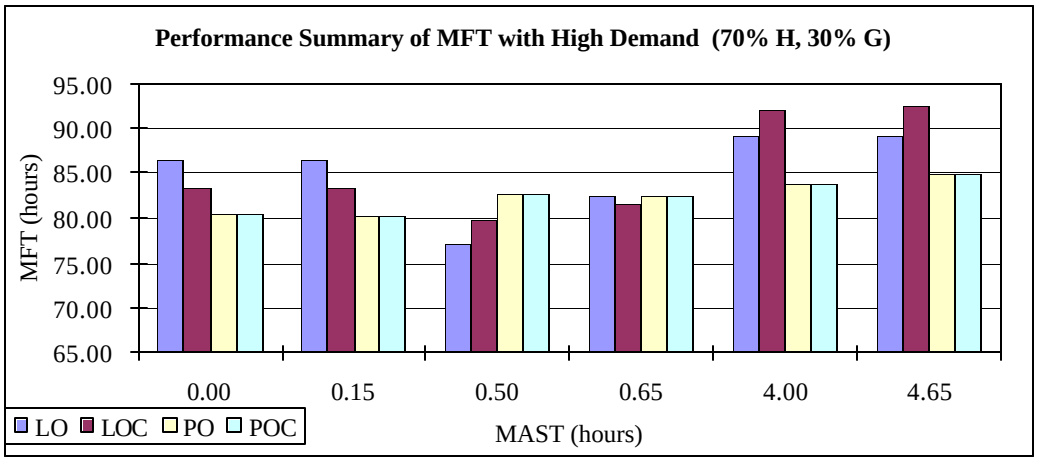


Figure 6-24. Summary of MFT with High Demand with (70% H, 30% G)

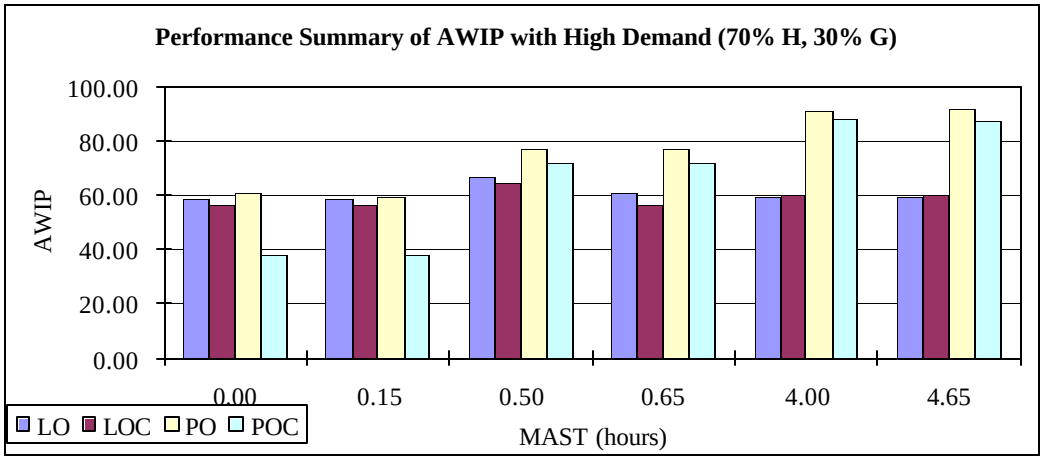


Figure 6-25. Summary of AWIP with High Demand with (70% H, 30% G)

From the above graphical analysis, we note that for high demand with a (70%, 30%) product mix:

1. The PO Heuristic has better performance with respect to makespan than the POC and LOC Heuristics.
2. The PO Heuristic generates the best schedules with respect to makespan using a MAST of 4.00 hours.
3. The LO Heuristic generate schedules with lower value of makespan values using a MAST of 0.5 hours.

To supplement the graphical analysis, analysis of variance (ANOVA) was conducted on the results for high demand with a (70%, 30%) product mix. The results indicate that neither heuristic nor MAST significantly affect makespan at a p-value of 0.05. This indicates that the differences noted in the graphical analysis are not statically significant.

6.4.2 Analysis for High Demand and (50%, 50%) Product Mix

In the following sections, each of the four heuristics are analyzed for high demand with (50% H, 50% G) product mix. The initial tester configuration is determined by the expression (5-3) and summarized in Table 6-39. A lower bound of 82.69 hours (as determined by expression (5-5)) is used to compare with the makespan generated by the heuristics.

Table 6-39. Suggested Initial Test Head Configuration for High Demand with (50% H, 50% G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	16	16
Pretest 2 (low)	8	8
Post-fuse (high)	2	2

Lot Optimization Heuristic

The performance of the Lot Optimization Heuristics for all levels of MAST is summarized in Table 6-40. The LO Heuristic generates a schedule with a makespan of 116.17 hours. This makespan is 40.48% away from the lower bound and occurs with a MAST setting of 0.5 hours. The lowest MFT and the highest AWIP also occurs with a MAST setting of 0.5 hours.

Table 6-40. Summary for High Demand (50% H, 50% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	130.02	157.23%	78.45	60.34
0.15	132.02	159.65%	78.45	59.42
0.50	116.17	140.48%	76.66	65.99
0.65	137.77	166.61%	81.80	59.37
4.00	145.27	175.68%	86.53	59.56
4.65	152.57	184.50%	88.44	57.97

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-41. The MAST setting of 0.5 hours generates the schedule with the lowest makespan (118.67 hours). The makespan is slightly greater than the makespan for the Lot Optimization without the tester constraint and is 43.51% away from the lower bound. The lowest MFT and the highest AWIP also occurs with a MAST setting of 0.5 hours.

Table 6-41. Summary for High Demand (50% H, 50% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	129.60	156.73%	78.29	60.41
0.15	129.60	156.73%	78.29	60.41
0.50	118.67	143.51%	77.53	65.33
0.65	144.25	174.44%	87.23	60.47
4.00	152.38	184.27%	90.42	59.34
4.65	148.28	179.32%	90.29	60.89

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-42. In this case, the best makespan schedule is generated using a MAST setting of 4.00 hours, with a resulting makespan of 91.85 hours. This makespan is 11.07% away from the lower bound. The second best schedule with respect to makespan occurs with a MAST setting of 4.65 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-42. Summary for High Demand (50% H, 50% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	134.13	162.20%	79.91	59.58
0.15	119.15	144.09%	77.50	65.04
0.50	108.10	130.73%	82.31	76.14
0.65	108.10	130.73%	82.24	76.08
4.00	91.85	111.07%	82.66	89.99
4.65	92.28	111.59%	82.58	89.49

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-43. In this case, the POC Heuristic generates a schedule with a makespan of 92.28 hours. This makespan is slightly higher than the schedule generated by PO Heuristic without the additional tester constraint and is 11.59% away from the lower bound. The second best schedule with respect to makespan occurs with a MAST setting of 4.00 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-43. Summary for High Demand (50% H, 50% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	221.33	267.65%	94.85	42.85
0.15	208.53	252.18%	90.83	43.56
0.50	114.04	137.91%	82.70	72.52
0.65	114.07	137.95%	82.80	72.59
4.00	92.38	111.72%	82.55	89.36
4.65	92.28	111.59%	81.67	88.50

Summary for High Demand with (50%, 50%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for high demand level with (50% H, 50% G) product mix. Figure 6-26 illustrates that the PO Heuristic usually generates schedules with lower values of makespan than the

LO Heuristic for comparable MAST settings. The PO Heuristic generates schedules with lowest makespan at higher MAST settings of 4.00 and 4.65 hours. The LO Heuristic generates schedules with lowest makespan at a MAST setting of 0.5 hours but these schedules have higher makespan than the best schedules generated by the PO Heuristic. Figure 6-27 illustrates that the LO Heuristic generates schedules with lowest MFT with MAST setting of 0.5 hours. Figure 6-28 illustrates that the LO Heuristic usually has lower AWIP than the PO Heuristic at comparable MAST settings. The highest AWIP levels occur for the PO and POC Heuristics at the higher MAST settings of 4.00 and 4.65 hours.

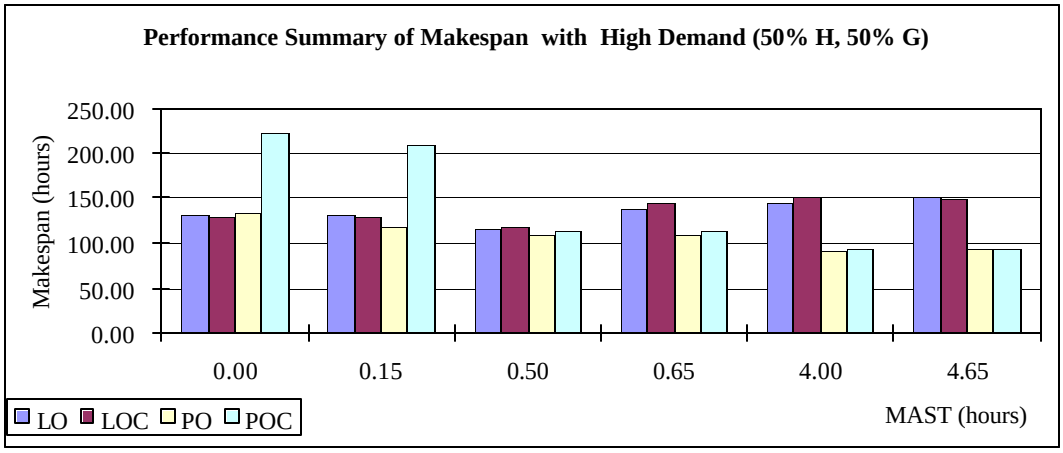


Figure 6-26. Summary of Makespan with High Demand with (50% H, 50% G)

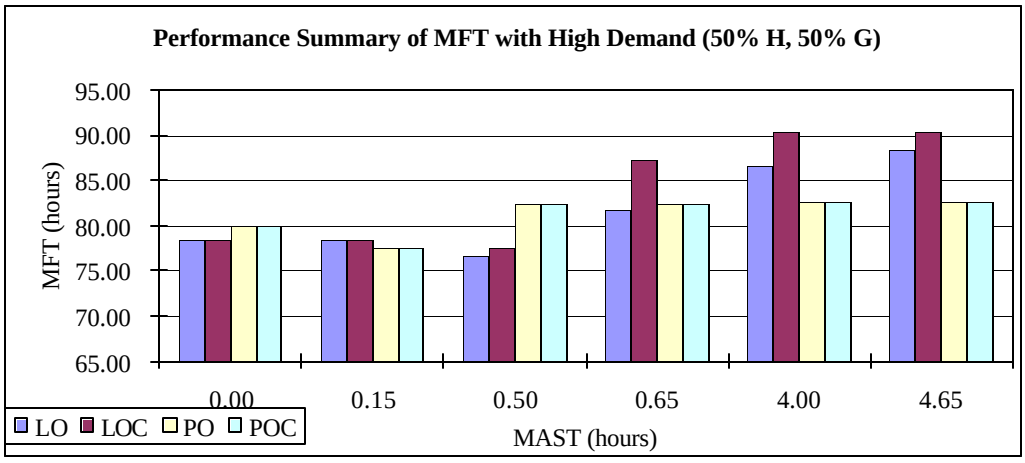


Figure 6-27. Summary of MFT with High Demand with (50% H, 50% G)

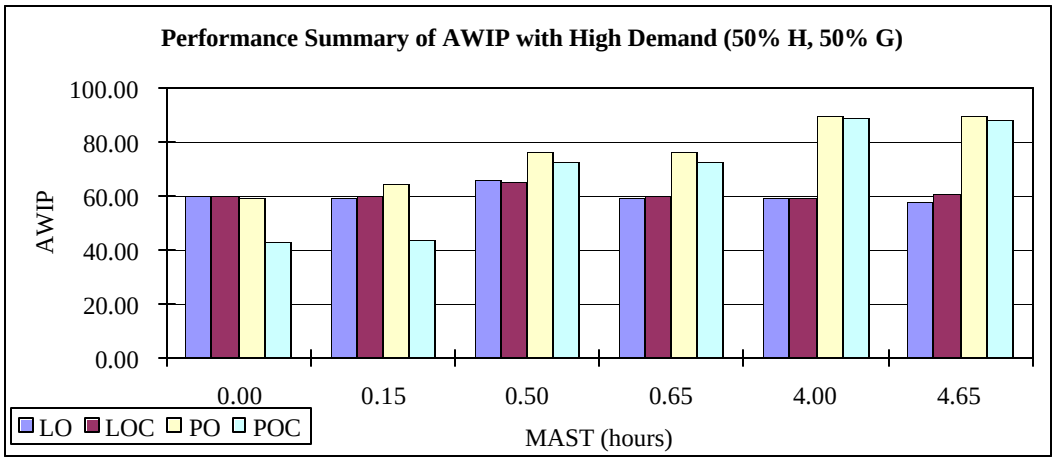


Figure 6-28. Summary of AWIP with High Demand with (50% H, 50% G)

From the above graphical analysis, we note that for high demand with a (50%, 50%) product mix:

1. The PO Heuristic generally outperforms LO and LOC Heuristics with respect to makespan for comparable MAST settings with this product mix (except for MAST of 0 hours).
2. The PO Heuristics generate the best schedules with respect to makespan using a MAST of 4.00 hours or 4.65 hours.
3. The LO Heuristics generate the schedules with lower value of makespan using a MAST of 0.5 hours.

To supplement the graphical analysis, analysis of variance (ANOVA) was conducted on the results for high demand with a (50%, 50%) product mix. The results indicate that neither heuristic nor MAST are considered significant in affecting makespan at a p-value of 0.05. Thus, the differences noted in the graphical analysis are not statically significant.

6.4.3 Analysis for High Demand and (20%, 80%) Product Mix

In the following sections, each of the four heuristics are analyzed for high demand with (20% H, 80% G) product mix. The initial tester configuration is determined by the expression (5-3) and summarized in Table 6-44. A lower bound of 83.65 hours (as

determined by expression (5-5)) is used to compare with the makespan generated by the heuristics.

Table 6-44. Suggested Initial Test Head Configuration for High Demand with (50% H, 50% G)

Test Process	Number of Test Heads for Product H	Number of Test Heads for Product G
Pretest 1 (high)	6	26
Pretest 2 (low)	4	12
Post-fuse (high)	2	2

Lot Optimization Heuristic

The performance of the Lot Optimization Heuristics is summarized in Table 6-45. The best makespan schedule is generated using a MAST setting of 0.5 hours, with a resulting makespan of 114.65 hours. This makespan is 37.05% away from the lower bound. The lowest MFT and the highest AWIP also occur for a MAST setting of 0.5 hours.

Table 6-45. Summary for High Demand (20% H, 80% G) using LO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	185.02	221.17%	99.96	54.03
0.15	185.02	221.17%	99.96	54.03
0.50	114.65	137.05%	74.31	64.81
0.65	124.22	148.49%	75.25	60.58
4.00	149.46	178.66%	84.85	56.77
4.65	140.32	167.74%	83.98	59.85

Lot Optimization Heuristic with Tester Constraint

The performance of the Lot Optimization with Tester Constraint (LOC) Heuristic is summarized in Table 6-46. The best makespan schedule is generated again using a MAST of 0.5 hours, with resulting makespan of 119.08 hours. The makespan is slightly greater than the makespan for the Lot Optimization without the tester constraint and is 42.35% away from the lower bound. The lowest MFT and highest AWIP levels also occur for MAST setting of 0.5 hours.

Table 6-46. Summary for High Demand (20% H, 80% G) using LOC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	185.82	222.13%	100.31	53.98
0.15	185.82	222.13%	100.31	53.98
0.50	119.08	142.35%	76.85	64.54
0.65	139.38	166.62%	83.39	59.83
4.00	154.36	184.52%	88.56	57.37
4.65	153.22	183.16%	87.95	57.40

Process Optimization Heuristic

The performance of the Process Optimization Heuristic is summarized in Table 6-47. In this case, the PO Heuristic generates a schedule with a makespan of 91.13 hours. This makespan is 8.94% away from the lower bound and occurs with MAST settings of 4.65 hours. The second best schedule with respect to makespan occurs with a MAST setting of 4.00 hours. The MFT is lower for the MAST settings of 4.00 and 4.65 hours, whereas AWIP levels are higher for these settings.

Table 6-47. Summary for High Demand (20% H, 80% G) using PO Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	200.83	240.07%	102.32	59.58
0.15	178.75	213.68%	92.01	65.04
0.50	109.23	130.57%	81.14	74.28
0.65	112.63	134.64%	81.33	72.21
4.00	91.85	109.80%	81.45	88.68
4.65	91.13	108.94%	81.56	89.50

Process Optimization Heuristic with Tester Constraint

The performance of the Process Optimization with Tester Constraint (POC) Heuristic is summarized in Table 6-48. In this case, the POC Heuristic generates a schedule with a makespan of 92.28 hours using a MAST setting of 4.65 hours. This makespan is slightly higher than the schedule than the schedule generated by PO Heuristic (without the tester

constraint) and is 10.31% away from the lower bound. The MFT is lower for the MAST settings of 4.00 and 4.65 hours whereas AWIP levels are higher for these settings.

Table 6-48. Summary for High Demand (20% H, 80% G) using POC Heuristic

MAST (hrs)	Makespan (hrs)	Performance Measure against Lower Bound	MFT (hrs)	AWIP
0.00	200.83	240.07%	102.32	59.58
0.15	178.75	213.68%	93.26	65.04
0.50	111.65	133.47%	81.7	73.18
0.65	112.63	134.64%	81.91	72.72
4.00	92.38	110.43%	79.97	86.57
4.65	92.28	110.31%	80.71	87.46

Summary for High Demand with (20%, 80%) Product Mix

The performance of the four heuristic are compared with respect to makespan, MFT, and AWIP for high demand level with (20% H, 80% G) product mix. Figure 6-29 illustrates that the PO Heuristic generates schedules with lower makespan and always outperforms the LO and LOC Heuristics. The PO Heuristic generates schedules with lowest makespan at a MAST setting of 4.65 hours. The LO Heuristic generates schedules with lowest makespan at a MAST setting of 0.5 hours but these schedules have higher makespan than the best schedules generated by the PO Heuristic. This figure also illustrates that the heuristic with the tester constraints generate schedules with larger makespan than the heuristic without the tester constraint. Figure 6-30 illustrates that the LO Heuristic generates schedules with lowest MFT with MAST setting of 0.5 hours. The PO Heuristic generates the lowest AWIP schedules at MAST settings of 4.00 and 4.65 hours. Figure 6-31 illustrates that the LO Heuristic has lower AWIP than the PO Heuristic at the comparable MAST settings.

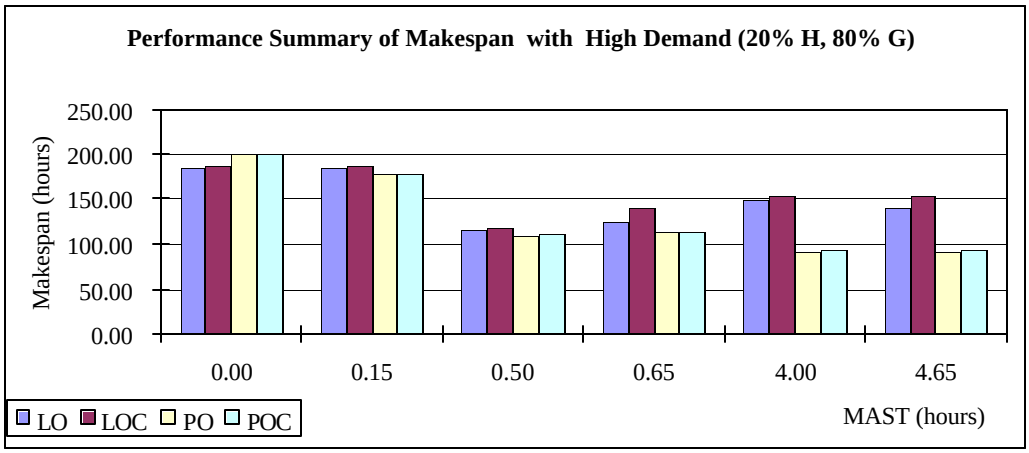


Figure 6-29. Summary of Makespan with High Demand with (20% H, 80% G)

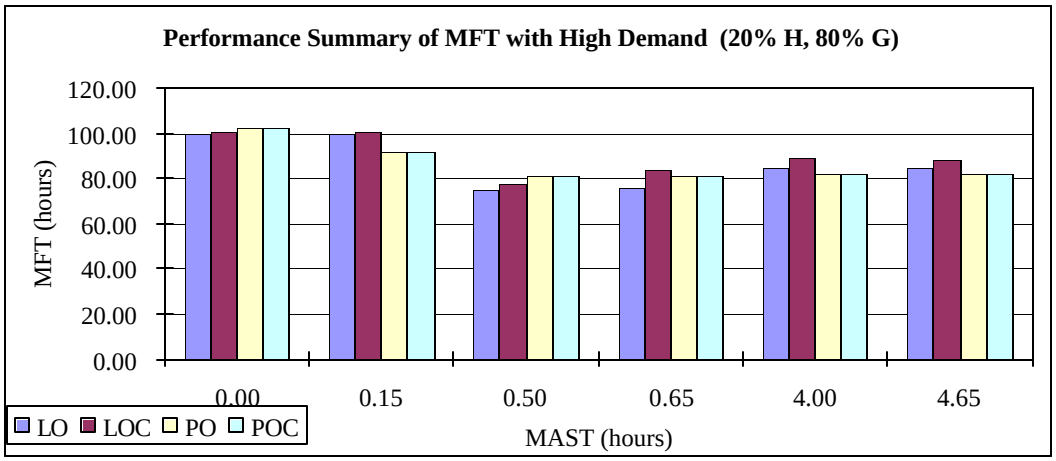


Figure 6-30. Summary of MFT with High Demand with (20% H, 80% G)

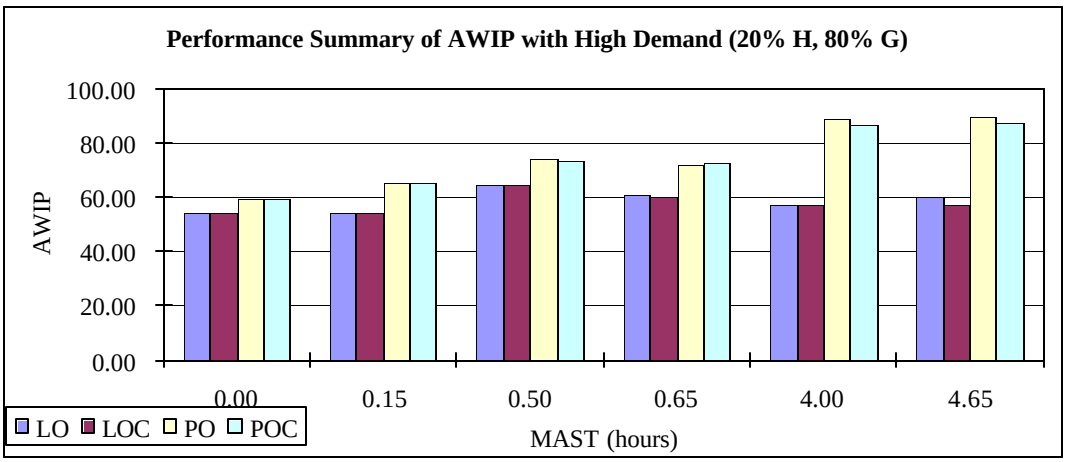


Figure 6-31. Summary of AWIP with High Demand with (20% H, 80% G)

From the above graphical analysis, we note that for high demand with a (20%, 80%) product mix:

1. The PO Heuristic has better performance with respect to makespan than the POC and LOC Heuristic.
2. The PO Heuristic generally outperforms LO and LOC Heuristics with respect to makespan for comparable MAST settings with this product mix (except for MAST of 0 hours).
3. The PO Heuristic generates the best schedules with respect to makespan using a MAST 4.65 hours.
4. The LO Heuristics generate the schedules with lower value of makespan using a MAST of 0.5 hours.

To support the graphical analysis, analysis of variance (ANOVA) was conducted on the results for high demand with a (20%, 80%) product mix. The results indicate that both heuristic ($p=0.047$) and MAST ($p=0.000$) significantly affect makespan. Tukey's pairwise comparison indicated that the MAST settings of 0.5, 0.65, 4.0, and 4.65 hours produce significantly lower makespan than MAST settings of 0 and 0.15 hours.

6.4.4 Summary for High Demand Analysis

The analysis for high demand can be summarized as follows:

1. The PO Heuristic generally outperforms the LO and LOC Heuristics with respect to makespan.
2. The PO heuristic generates the better schedule with respect to makespan using a MAST of 4.00 hours or 4.65 hours.
3. The LO Heuristic generates the best schedules using a MAST of 0.5 hours.

To support the graphical analysis, ANOVA was conducted for the data set of all experiments with high demand. The ANOVA results indicate that the interactions of heuristic and MAST ($p=0.000$) and heuristic and mix ($p=0.027$) significantly affect

makespan. The main effects of heuristic (p=0.000) and MAST (p=0.000) are also significant.

Schedules generated using the PO Heuristic with a MAST setting of 4.65 hours, and using LO Heuristic with MAST settings of 0.5 and 0.65 hours are shown in Figure 6-32, Figure 6-33 and Figure 6-34 respectively.

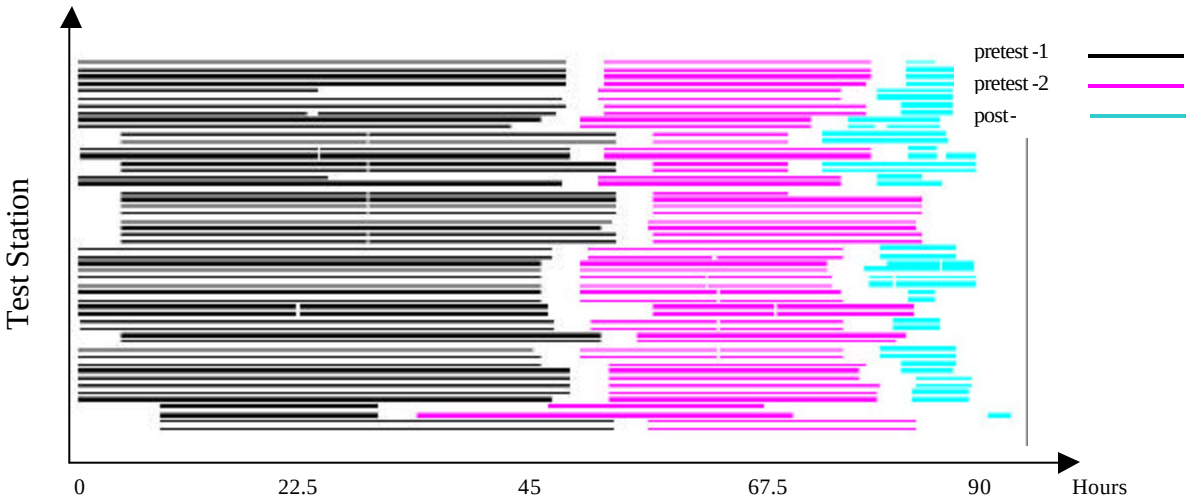


Figure 6-32. Schedule Generated for High Demand (50% H, 50% G) using PO Heuristic with MAST of 4.65 hours

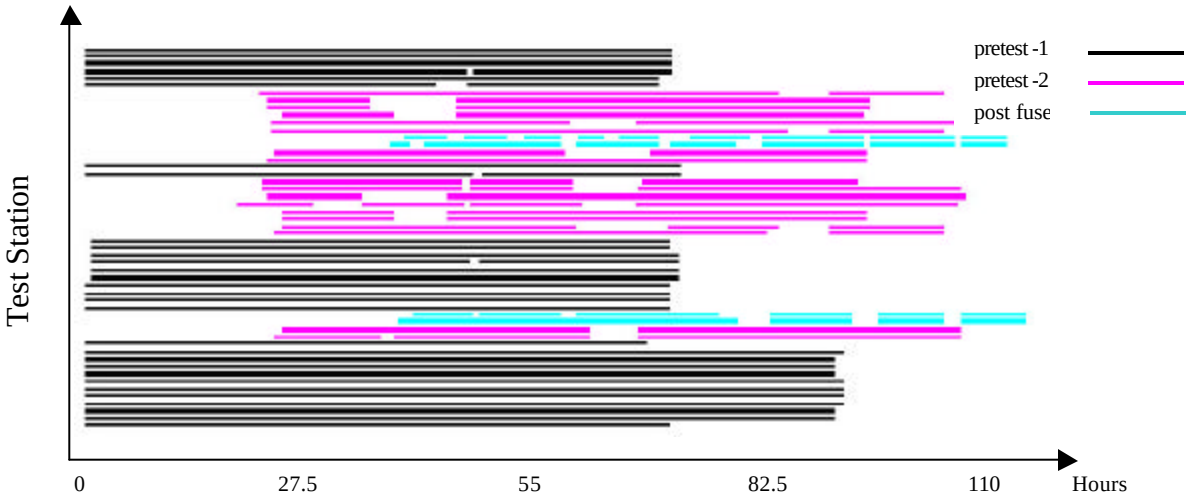


Figure 6-33. Schedule Generated for High Demand (20% H, 80% G) using LO Heuristic with MAST of 0.5 hours

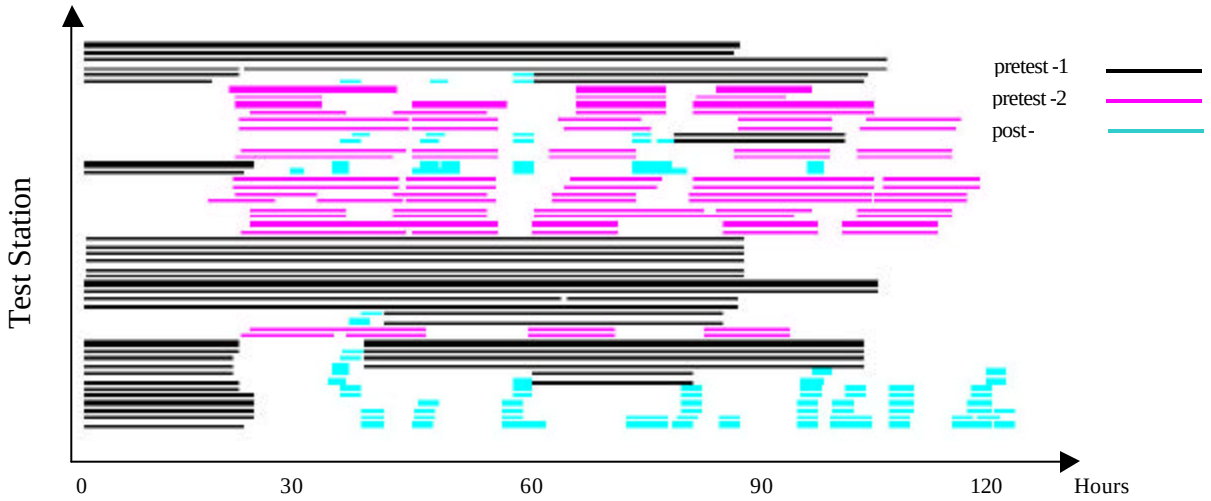


Figure 6-34. Schedule Generated for High Demand (20% H, 80% G) using LO Heuristic with MAST of 0.65 hours

6.5 Summary

In this chapter, we conducted a comprehensive analysis on the heuristics using a set of experimental data. Through the analysis, we are able to determine which heuristics perform better with respect to makespan for a given demand scenario (demand level and product mix), and select the appropriate settings for the maximum allowed set up time (MAST). The findings are summarized as follows:

- The PO Heuristic generally to outperforms both the LO and LOC Heuristics with respect to makespan for medium and high demand and has the same performance for low demand as LO Heuristics.
- The PO Heuristics generated lower makespan schedules at higher MAST for all demand levels.
- The LO Heuristics usually generated the lowest makespan schedule at the MAST setting of 0.5 hours for medium and high demand and generated the lowest makespan schedule at higher MAST settings for low demand.
- The schedules developed with the PO Heuristic with lowest makespan often results in high AWIP, especially when the product demand level is high.

These conclusions are obtained from the analysis that is based on the static situation, where all the test stations are available initially and all the wafer lots are available for process. However, these conclusions may not necessarily be suitable for a dynamic situation, where not all test stations are available at initial time and some jobs are processing at the test stations. In the next chapter, the heuristics are analyzed for two dynamic situations, which are obtained from an actual manufacturing environment.

CHAPTER VII

CASE STUDY ANALYSIS

In this chapter, two case studies are presented of the heuristics applied to an actual industrial environment. In these case studies, the status of the wafer lots and initial tester configuration are obtained from the actual manufacturing environment. Case Study I was based on the schedule for forty-one wafer lots at the beginning of the week (January 9th 2001), and Case Study II was taken at the middle of the week (December 12th 2000) in which fifty-one wafer lots are scheduled.

The actual initial test station configuration and wafer lot status are obtained by downloading the information from the manufacturing database using Standard Query Language (SQL). The information is stored in two tables and displayed on the initial interface form of the *Wafer Test Scheduler* as illustrated in Figure 7-1. The upper table shows current test station status and the lower table shows the wafer lot status. The heuristics are applied to generate schedules, and the schedules are compared to the actual schedule generated by the planners and executed in the testing facility.

In each case study, the heuristics with tester constraint are first applied, because the tester constraint exists in the actual manufacturing environment. Since the tester constraint is expected to be relaxed in the near future, the heuristics without tester constraint are also applied to demonstrate the potential improvement of relaxing the tester constraint.

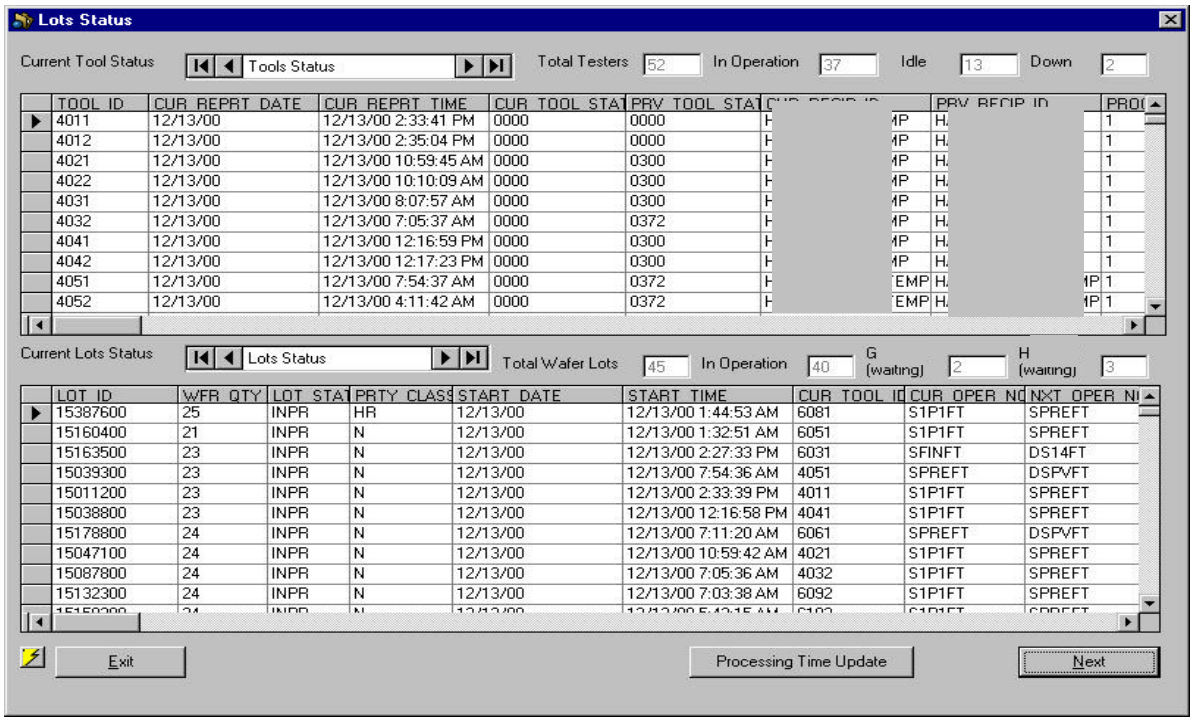


Figure 7-1. Case Study I - Actual Initial Configuration

7.1 Case Study I

In Case Study I, the manufacturing environment consists of 26 test stations, each with two test heads. At the time the case study is conducted, thirty-seven test heads are in operation, thirteen test heads are idle, and two test heads are down for maintenance. The two test heads that are down for maintenance are considered not available throughout the entire schedule period in this case analysis.

Forty-five lots of wafer devices need to be scheduled in this case (30 Product G, 15 Product H). Forty lots are already in process in the testing facility, and five wafer lots are waiting (2 Product G wafer lots and 3 Product H wafer lots). Three wafer lots out of the 40 wafer lots that are in process are in the fuse operation, which are not processed on the test stations under consideration. These three lots, however, need to be scheduled onto the test stations for post-fuse (high) after the fuse process, therefore, those three lots are included in the schedule list. Note that forty wafer lots are in processing, which is more

than the number of test heads that are in operation (thirty-seven test heads in operation). Thus, the initial test heads configuration is determined by the number of test heads in operation as described by expression (5-4). Table 7-1 summarizes the initial test head information, and Table 7-2 summarizes the demand for each test process. This demand falls between a low and medium demand level.

The following sections describe the actual schedule executed at the manufacturing site, the results of the lot optimization heuristic with tester constraint, and the result of the process optimization heuristic with tester constraint. In addition, the lot optimization heuristic and the process optimization heuristic (without tester constraint) are also included in order to evaluate the potential improvement of relaxing the tester constraint.

Table 7-1. Case Study I - Initial Test Station Configuration

	Test Heads		
In Operation	37	Pretest 1 (high)	16
		Pretest 2 (low)	14
		Post-fuse (high)	7
Idle	13	Pretest 1 (high)	7
		Pretest 2 (low)	4
		Post-fuse (high)	2
Down	2		

Table 7-2. Case Study I - Product Demand Summary

Test Process	**Product G**	**Product H**
Pretest 1 (high)	0	1
Pretest 2 (low)	14	10
Post-fuse (high)	30	15

7.1.1 Actual Schedule

The actual schedule that was executed in the manufacturing environment is obtained by downloading the schedule information from the database after all the wafer lots have been tested. The actual schedule is illustrated in Figure 7-2, where pretest 1 (high) is represented in black rectangular, pretest 2 (low) process is represented in blue rectangular, and the post-fuse (high) process is represented in magenta rectangular. In the actual schedule, no process change has been made on any of the test heads. In other words, the test stations initially set for pretest 1 (high) always performs a pretest 1 (high) test, and the test stations initially set for post-fuse (high) always perform post-fuse (high) test. This *no change* policy also applies to the actual schedule of Case Study II, and seems to be the company's scheduling policy. The makespan of the actual schedule is 66.25 hours.

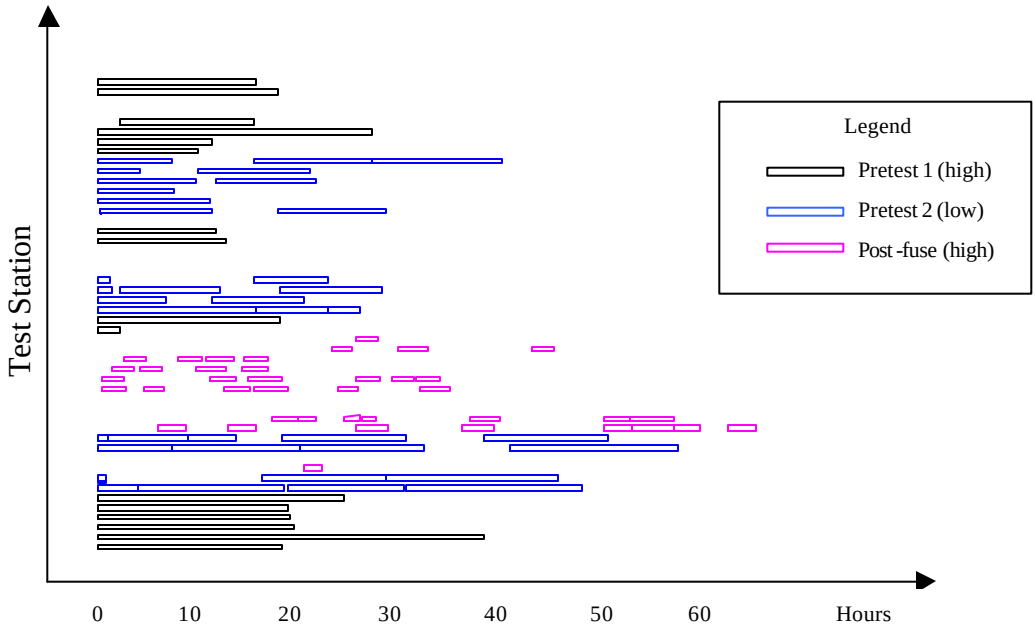


Figure 7-2. Case Study I - Actual Schedule Gantt-Chart (Makespan 66.25 Hours)

7.1.2 Lot Optimization Heuristic with Tester Constraint

The Lot Optimization with Tester Constraint (LOC) Heuristic schedules the wafers lot by lot until all the wafer lots are scheduled. While scheduling each wafer lot, the heuristic schedules each test process of a wafer lot in the required sequence until all the test

processes of the wafer lot are scheduled. The lot optimization heuristic uses the suggested initial test station configuration to schedule the wafer lots.

In this case study, the initial test head configuration and the suggested test station configuration are similar. The initial test station configuration and the suggested configuration are summarized in Table 7-3.

Table 7-3. Case Study I - Initial Tester Configuration and Suggested Tester Configuration

	Initial Configuration		**Suggested Configuration**	
	Product G	**Product H**	**Product G**	**Product H**
Pretest 1 (high)	22	6	18	4
Pretest 2 (low)	12	4	12	6
Post-fuse (high)	4	2	9	1

Two test heads are changed from a setup status of pretest 1 (high) to pretest 2 (low) for the initial setup according to the suggested initial test station configuration. Using the LOC Heuristic, the best makespan schedule is generated using a MAST setting of 0.65 hours, and the resulting makespan is 49.26 hours, which is 25.65% less than the actual schedule. Figure 7-3 illustrates the Gantt chart of the schedule.

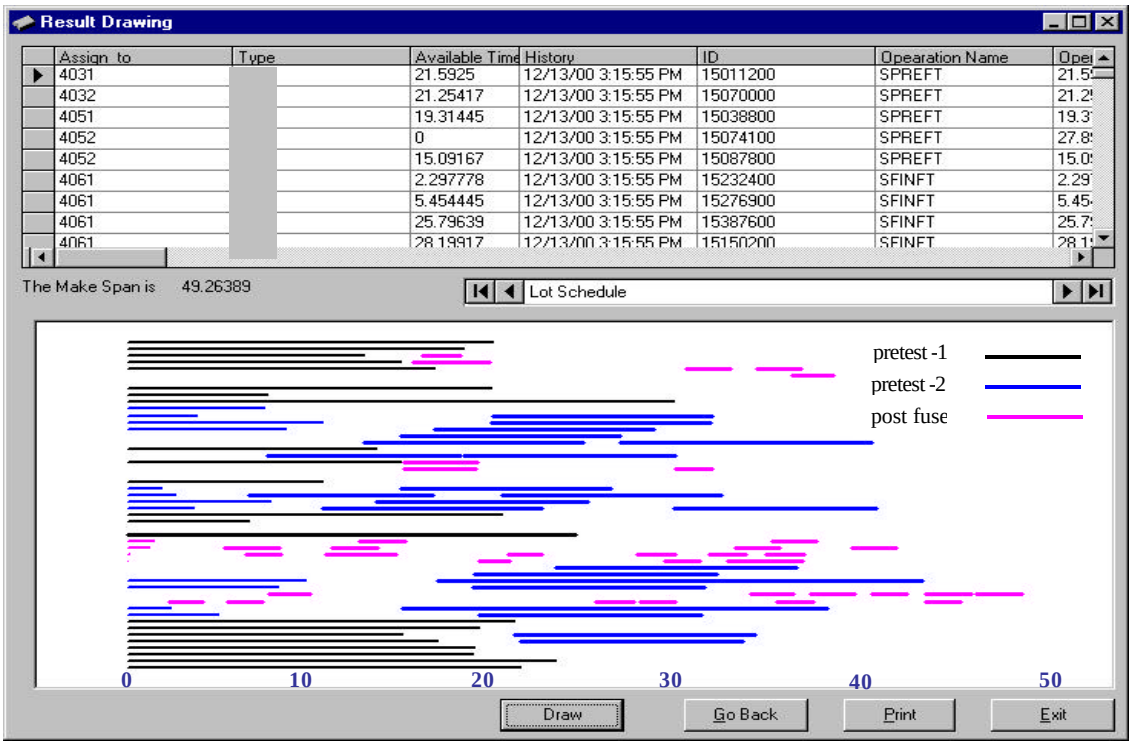


Figure 7-3. Case Study I – Schedule Generated by LOC Heuristic

7.1.3 Process Optimization Heuristic with Tester Constraint

The Process Optimization with Tester Constraint (POC) Heuristic first schedules all wafer lots that are currently waiting for pretest 1 (high) test process, then schedules the wafer lots that are ready for pretest 2 (low) test, and finally schedules the post-fuse (high) test of the wafer lots.

In this case study, the schedule resulting from the POC Heuristic is similar to the schedule for the LOC Heuristic. Since only one wafer lot needs to be scheduled for the pretest 1 (high) test, the initial dispatching sequence is similar to the initial dispatching sequence for the LOC Heuristic. The best schedule with respect to makespan is generated using a MAST setting of 0.65 hours with a resulting makespan of 50.41 hours. The makespan is 23.91% less than the actual schedule. The resulting schedule is illustrated in Figure 7-4.

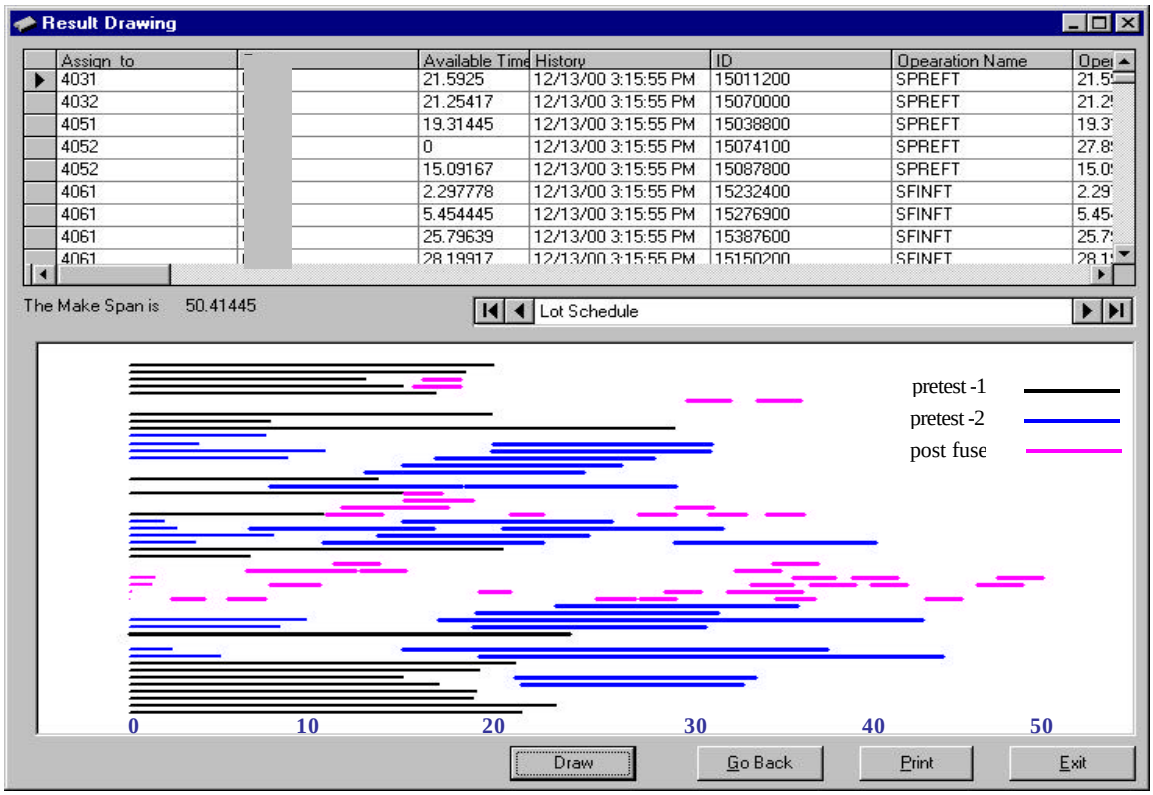


Figure 7-4. Case Study I - Schedule Generated by POC Heuristic

7.1.4 Lot Optimization Heuristic (without tester constraint)

The Lot Optimization Heuristic approach ignores the constraint that pretest 1 (high) test and pretest 2 (low) test of a wafer lot must be performed on the same type of test station. The constraint is caused by the difference between the testing software of the two types of test stations (*Teradyne* and *Asia*) and their specification. These differences are expected to be resolved in the future so that both types of test stations can process any wafer lots. Relaxing the tester constraints is expected to provide more flexibility and allow more efficient schedules.

Using the LO Heuristic, the best schedule with respect to makespan is generated using a MAST setting of 0.65 hours, with the resulting makespan of 46.725 hours. The makespan is 29.48% less than the actual schedule and is also 5.15% less than the

schedule generated with LOC Heuristic. The resulting schedule is illustrated in Figure 7-5.

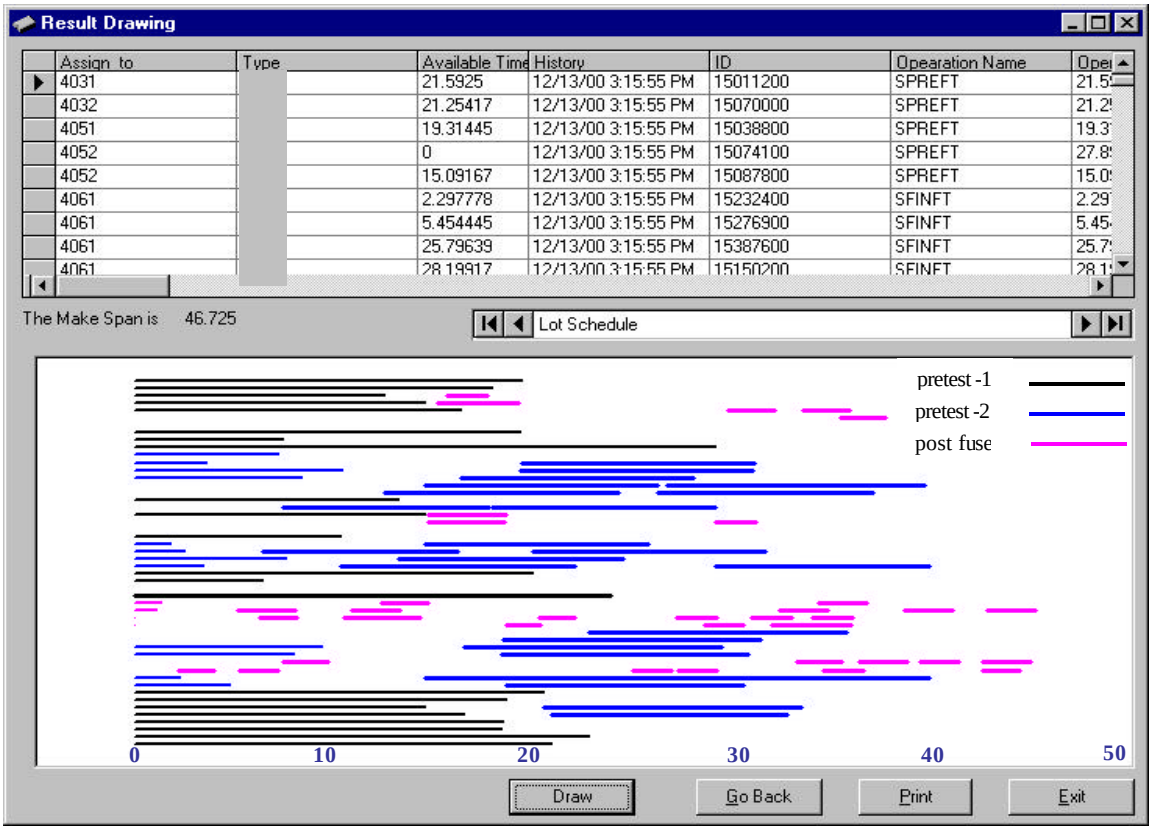


Figure 7-5. Case Study I - Schedule Generated by LO Heuristic

7.1.5 Process Optimization Heuristic (without Tester Constraint)

The Process Optimization Heuristic is also applied to the case study. Using the PO Heuristic, the best schedule with respect to makespan is generated using a MAST setting of 0.65 hours, with resulting makespan of 46.73 hours. Although the resulting schedule is slightly different from the schedule for LO Heuristic, the resulting makespan is the same as LO Heuristic. The makespan is 29.48% less than actual makespan and 7.31% less than the schedule generated with POC Heuristic. The resulting schedule is illustrated in Figure 7-6.

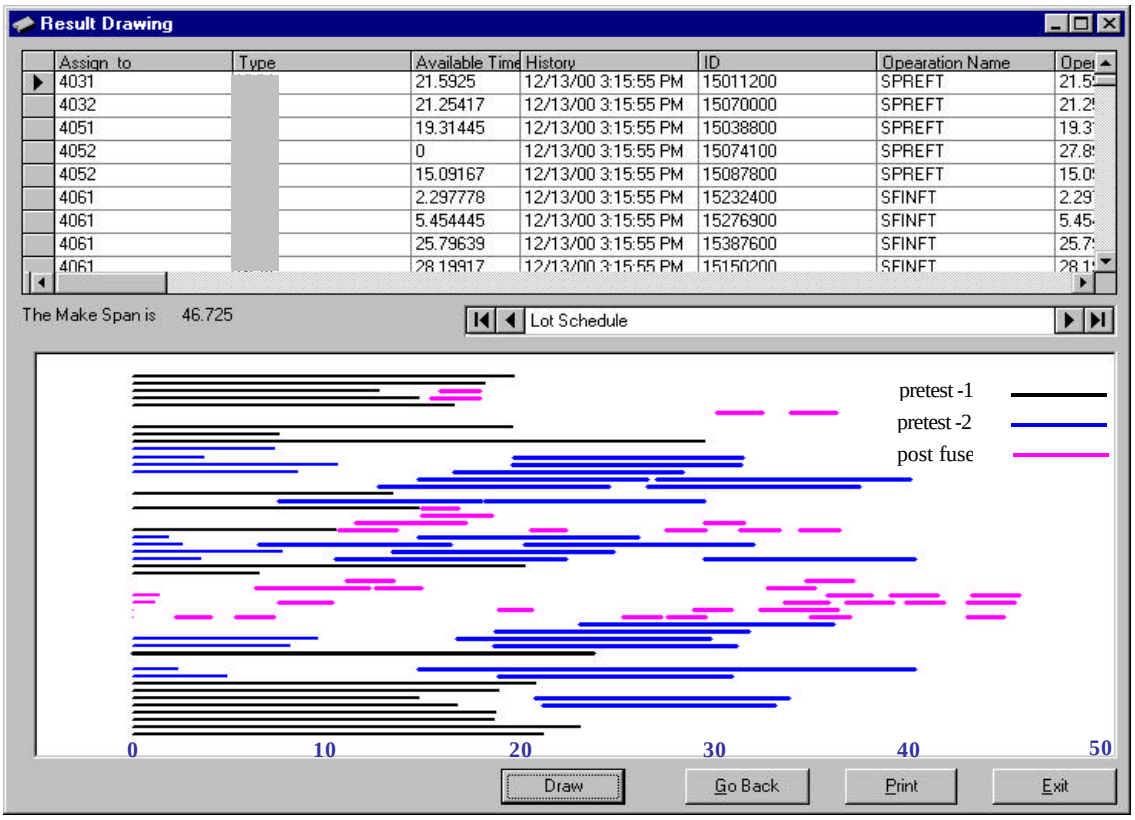


Figure 7-6. Case Study I - Schedule Generated by PO Heuristic

The following table summaries the results of each heuristic for Case Study I. In all cases, the heuristics generated makespans at least 23% less than the makespan realized in the actual schedule at the testing facility. Moreover, the LO Heuristic and PO Heuristic (without tester constraint) generate the best schedules with respect to makespan.

Table 7-4. Case Study I - Performance Summary

Heuristic	Makespan (hrs)	Improvement over Actual Schedule	MAST Setting
LOC	49.26	25.65%	0.65
POC	50.41	23.91%	0.65
LO	46.73	29.48%	0.65
PO	46.73	29.48%	0.65

7.2 Case Study II

In Case Study II, the manufacturing environment contains 52 test stations, each with two test heads. Forty-nine test heads are available for scheduling, among which 30 test heads are in operation, 19 test heads are idle, and 3 test head are down for maintenance Again, the three test heads that are currently down for maintenance are considered not available through out the entire schedule period. The initial test head status is summarized in Table 7-5.

Forty-eight wafer lots need to be scheduled in this case, of which thirty-two lots are in processing, and the rest are waiting. Table 7-6 summarizes the demand for each test process. From the product demand summary, note that this case is between a low demand and a medium demand level scheduling problem.

Table 7-5. Case Study II - Initial Test Station Configuration

	Test heads		
In operation	30	Pretest 1 (high)	23
		Pretest 2 (low)	6
		Post-fuse (high)	1
In idle	19	Pretest 1 (high)	6
		Pretest 2 (low)	9
		Post-fuse (high)	4
Down	3		

Table 7-6. Case Study II -Demand Summary

Test Process	**Product G**	**Product H**
Pretest 1 (high)	0	4
Pretest 2 (low)	6	34
Post-fuse (high)	7	41

7.2.1 Actual Schedule

The actual schedule executed in the manufacturing environment is obtained by downloading the schedule information from the database after all the wafer lots have been tested. The actual schedule is illustrated in Figure 7-7, with a makespan of 113.67 hours, where pretest 1 (high) is represented in black rectangular, pretest 2 (low) process is represented in blue rectangular, and the post-fuse (high) process is represented in magenta rectangular. It can be seen from the Figure 7-7 that one lot in the schedule is delayed significantly, which causes the makespan increases from 86.07 to 113.67 hours. In our case analyses, the makespan of 86.07 hours will be used to provide a conservative comparison with the heuristic results. As seen in the actual schedule, no process change setup has been made on any test head (except one setup change from pretest 1 (high) to post-fuse (high), which occurs on the third test head from the top as shown in Figure 7-7). This *no change* policy is used by the manufacturing to ensure that test stations are always available for new wafer devices that enter the facility.

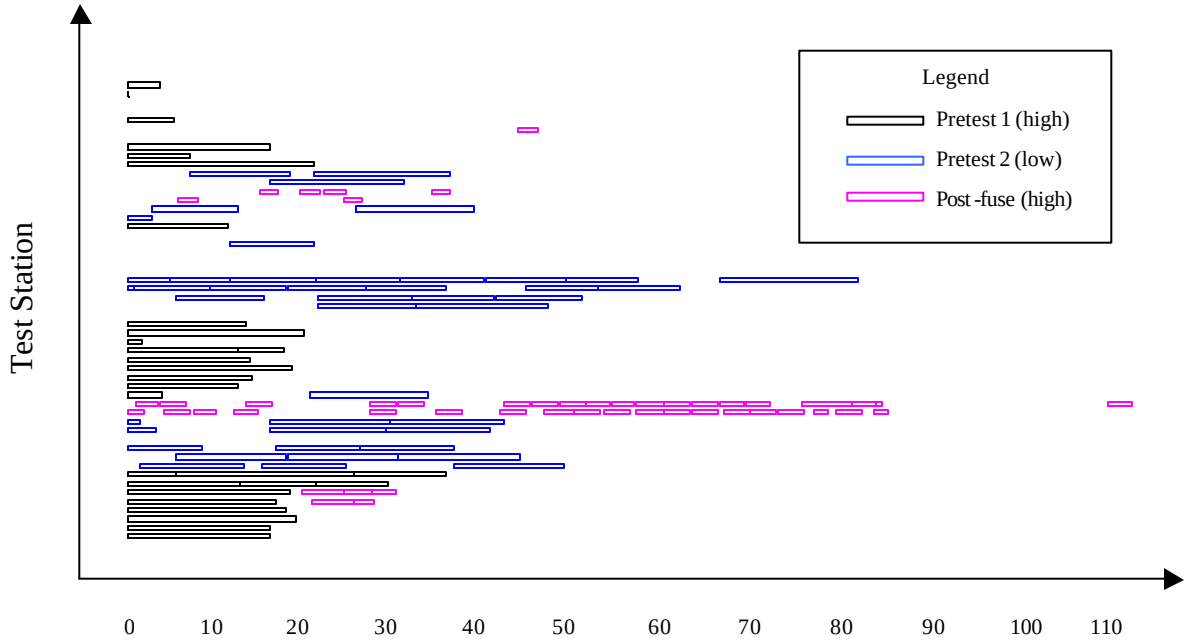


Figure 7-7. Cast Study II - Actual Schedule Gantt Chart (Makespan 86.07 hours)

7.2.2 Lot Optimization Heuristic with Tester Constraint

In this case study, the difference between the initial test head configuration and the suggested test station configuration is substantial. Table 7-7 summarizes the current test head configuration in the testing facility and the suggested initial configuration. As illustrated in Figure 7-8, 18 test stations are selected for changing setup. Ten test heads change from Product H pretest 1 (high) to Product H pretest 2 (low), 6 test heads change from Product G pretest 1 (high) to Product G post-fuse (high) and 2 heads change from Product G pretest 1 (high) to Product H pretest 2 (low).

Table 7-7. Case Study II - Initial Tester Configuration Information

	Current Configuration		Suggested Initial Configuration	
Test Process	**Product G**	**Product H**	**Product G**	**Product H**
Pretest 1 (high)	11	18	2	8
Pretest 2 (low)	10	5	4	24
Post-fuse (high)	3	2	2	8

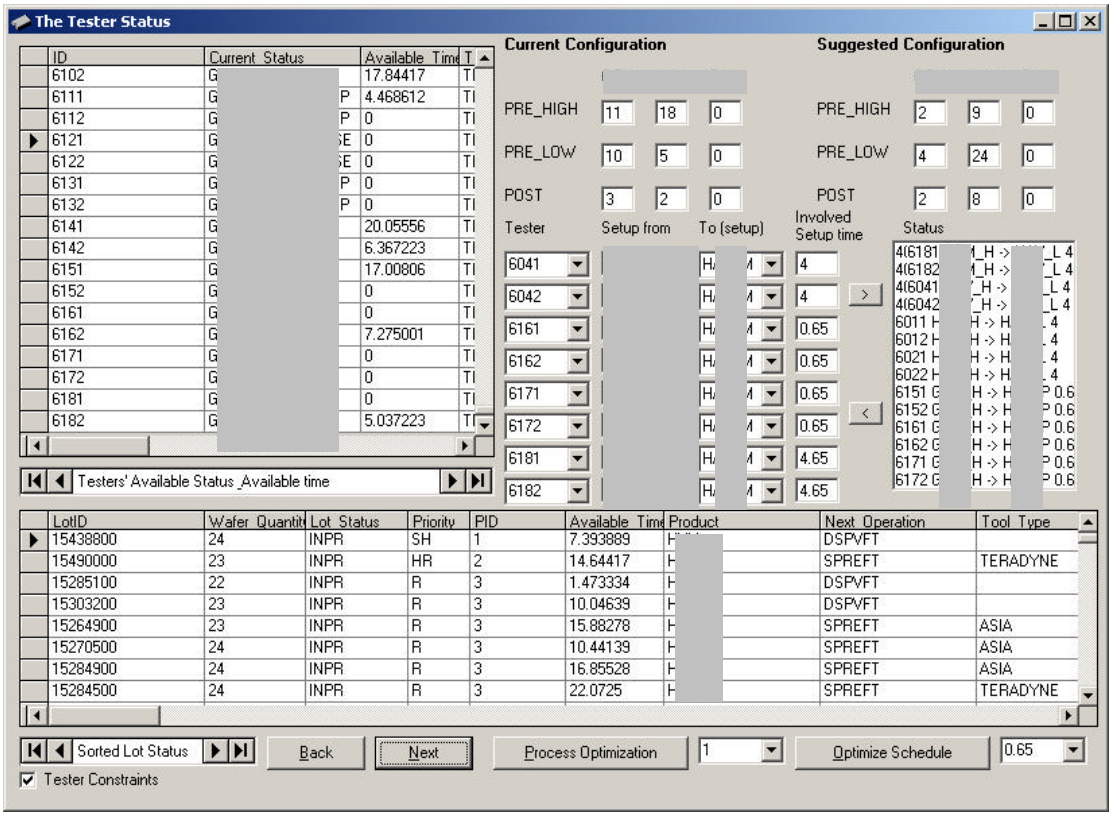


Figure 7-8. Case Study II - Initial Configuration Change

Using the Lot Optimization with Tester Constraint (LOC) Heuristic, the best makespan schedule is generated using a MAST setting of 0.65 hours, with resulting makespan of 58.88 hours. The makespan is 31.59% less than the actual schedule. The resulting schedule is illustrated in Figure 7-9.

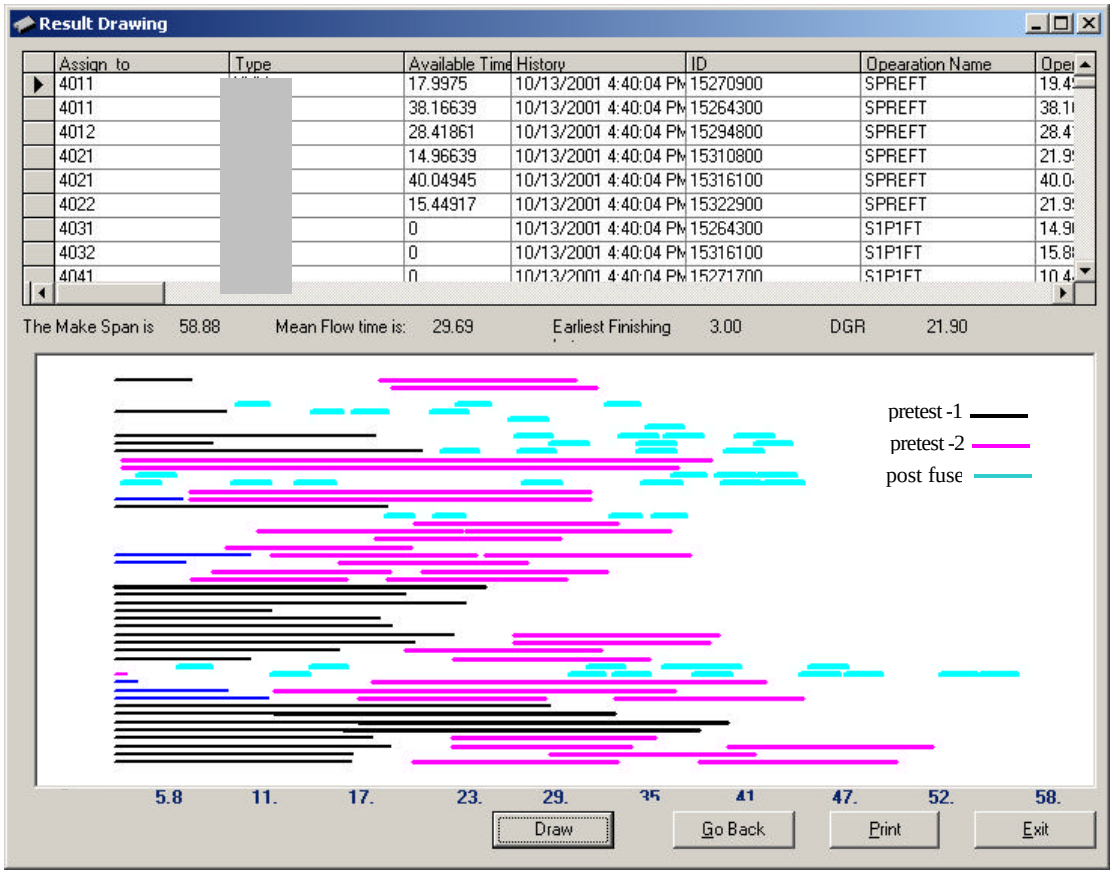


Figure 7-9. Case Study II - Schedule Generated by LOC Heuristic

Note that this schedule is also good for a continuous manufacturing environment where new products arrive continuously for testing because several test stations become idle at early stage of the schedule. In addition the schedule is more efficient with respect to makespan than the actual schedule.

7.2.3 Process Optimization Heuristic with Tester Constraint

For the Process Optimization with Tester Constraint (POC) Heuristic, the best makespan schedule is generated using MAST settings of 4.00 and 4.65 hours, with a resulting makespan of 47.25 hours (The schedule developed with MAST of 4.00 hours has a lower MFT than the schedule developed with MAST of 4.65 hours). The makespan is 45.10% less than the actual schedule. The resulting schedule is illustrated in Figure 7-10.

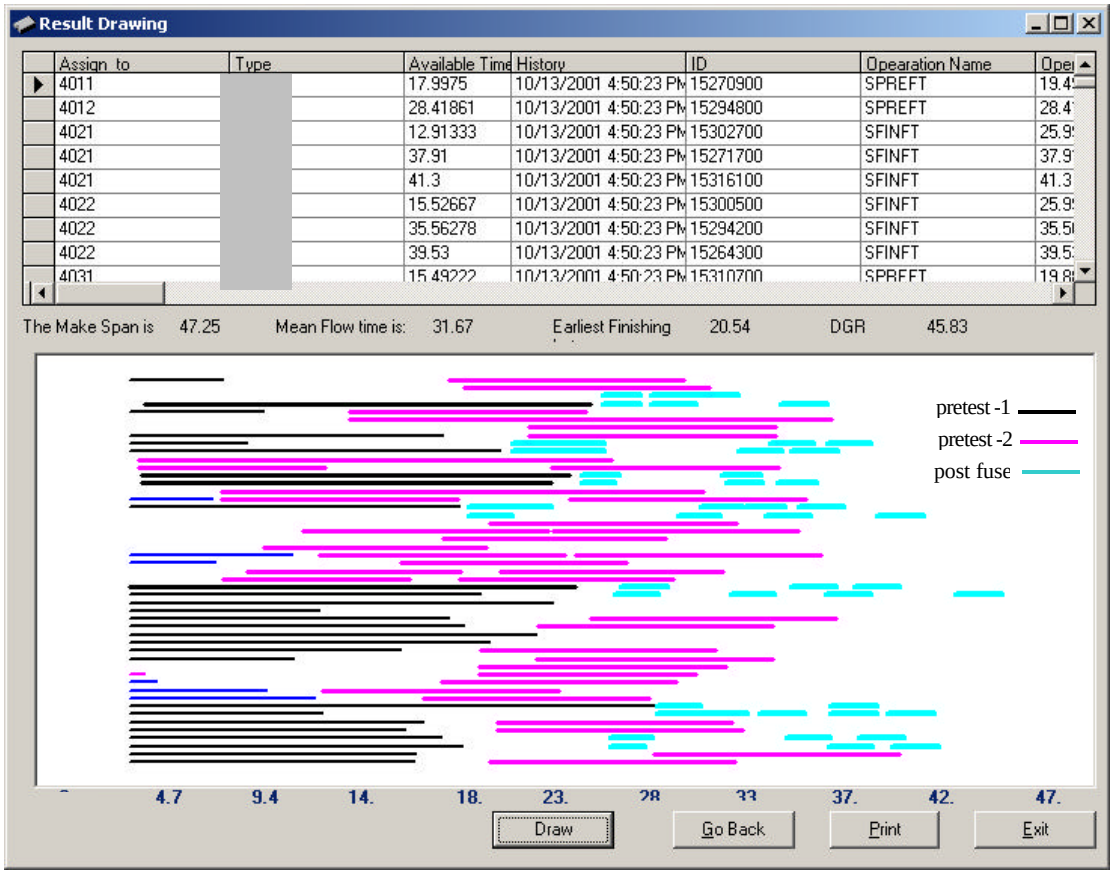


Figure 7-10. Case Study II - Schedule Generated by POC Heuristic

Although this schedule has a lower makespan than the schedule generated by LOC Heuristic, the schedule is less able to accommodate wafer lots that arrive during the scheduling horizon, since many of the test stations are available only at later stages of the schedule horizon. As a consequence, new wafer lots that arrive during the scheduling

horizon, which is 47.25 hours in this case, may have to wait until all the current wafer lots are completed.

7.2.4 Lot Optimization Heuristic

Lot Optimization Heuristic (without tester constraint) generates the best makespan schedule using a MAST setting of 0.5 and 0.65 hours with a resulting makespan of 58.88 hours. The makespan is the same as the schedule generated with the LO Heuristic with Tester Constraint and is 31.59% less than the actual schedule. The resulting schedule is illustrated in Figure 7-11.

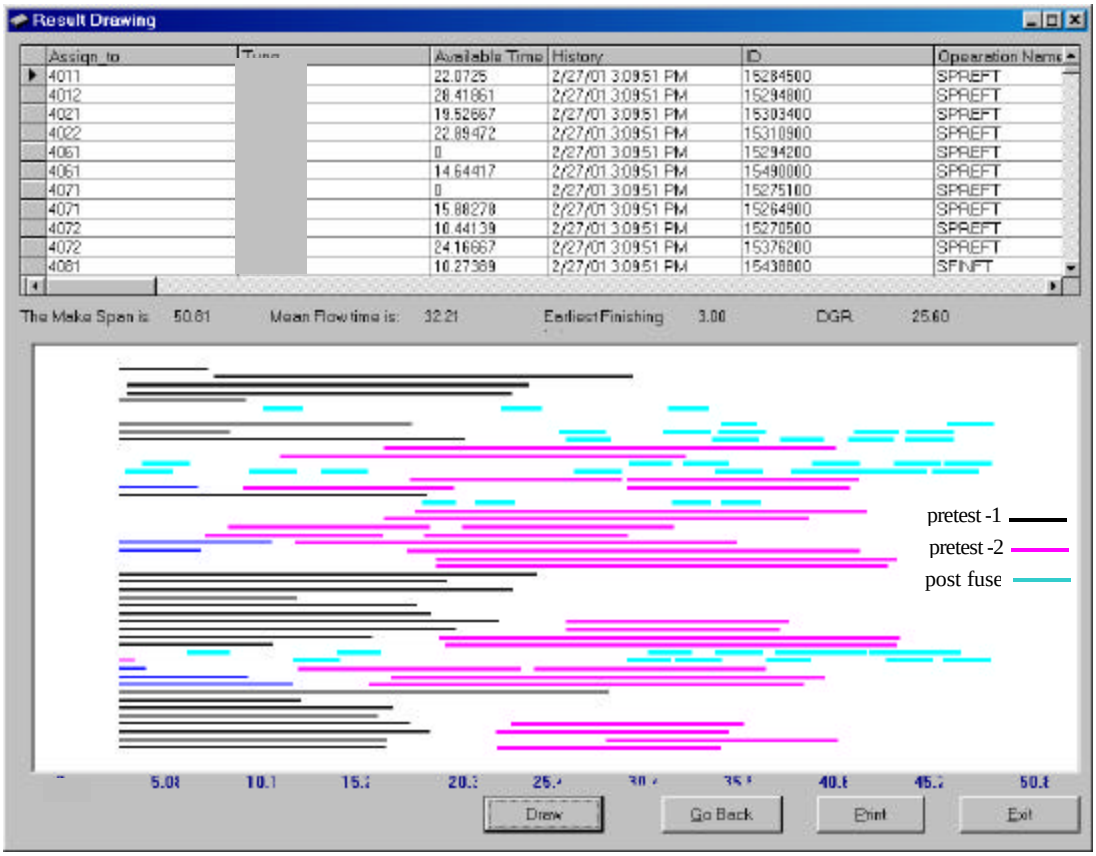


Figure 7-11. Case Study II - Schedule Generated by LO Heuristic

7.2.5 Process Optimization Heuristic

Using the Process Optimization Heuristics (without tester constraint), the best makespan schedule is generated using MAST settings of 4.00 and 4.65 hours, with resulting

makespan of 47.25 hours. This makespan is the same makespan of the schedule generated with the PO Heuristic with Tester Constraint, and is 45.10% less than the actual schedule. The resulting schedule is illustrated in Figure 7-12.

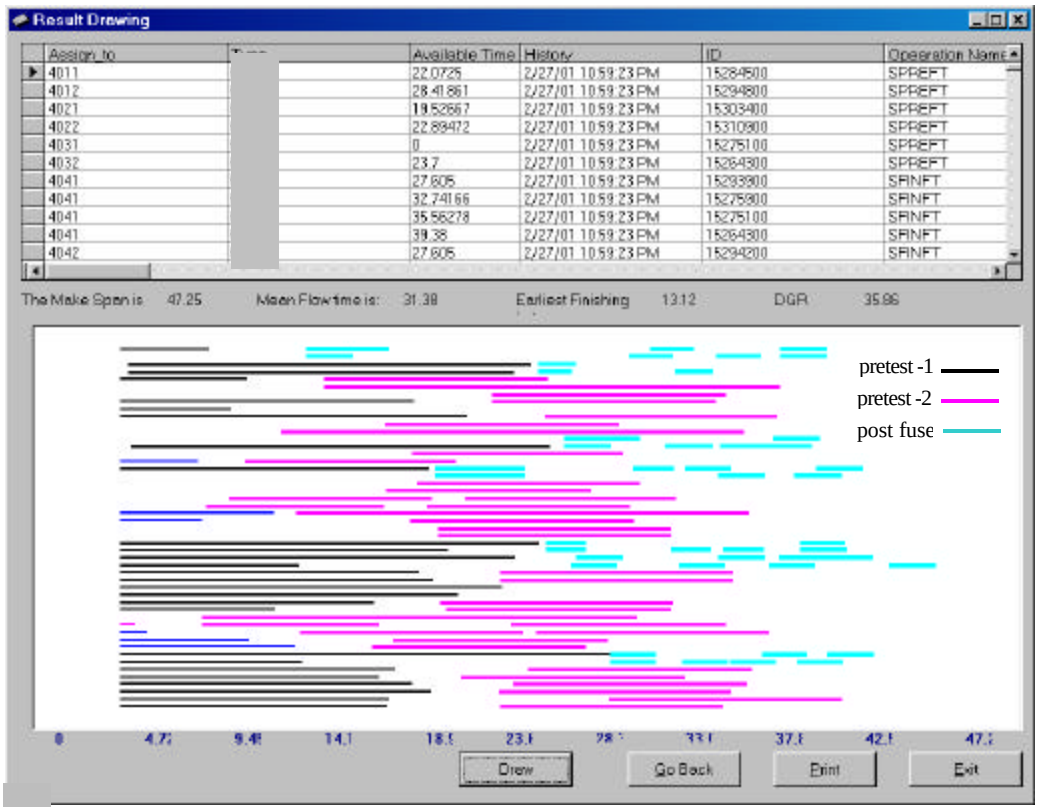


Figure 7-12. Case Study II - Schedule Generated by PO Heuristic

Table 7-8 summarizes the performance of the heuristic for Case Study II. As shown, the PO and POC Heuristics generate schedules with the lowest makespan. The makespan of the resulting schedules generated by the heuristics are at least 31% less than the makespan of the actual schedule.

Table 7-8. Case Study II - Performance Summary

Heuristic	Makespan (Hours)	Improvement over Actual Schedule	MAST Setting (Hours)
LO (wtc)	51.69	31.59%	0.65
PO(wtc)	47.25	45.10%	4.00, 4.65
LO	50.81	31.59%	0.50, 0.65
PO	47.25	45.10%	4.00, 4.65

7.3 Summary of Case Study Results

From the case studies presented in this chapter, we summarize our observation as follows:

- The heuristic approaches are able to address the tester constraints currently used by the manufacturing company. Although the tester constraint limits the flexibility of the scheduling process, the heuristics presented in this research appear to handle the situation.
- Both heuristics generate schedules that improve the makespan (by 23%-45%) compared to the actual schedule.
- The PO Heuristics generated better schedules with respect to makespan than the LO Heuristic, although the difference is not as large as the static case analyses.
- The PO Heuristic generated the lowest makespan with MAST settings at 0.65, 4.00, and 4.65 hours, which is slightly different than the static analysis (where the best schedules generated by the PO Heuristic usually occurred for MAST settings of 4.00 and 4.65 hours).
- Consistent with the static analysis, the LO Heuristic often generates the lowest makespan with MAST settings of 0.5 or 0.65 hours for low and medium demand level.

The heuristics are adaptable for a variety of initial configurations, including wafer lots in process and test stations with a variety of configurations. In addition, the makespan generated by the heuristics is significantly less than the actual schedule.

CHAPTER VIII

CONCLUSIONS AND FUTURE RESEARCH

This research has analyzed the semiconductor test scheduling problem. A mathematical model for the problem has been developed and two heuristics have been presented to solve the scheduling problem. The heuristic approaches have been studied and analyzed through both static analyses and dynamic case study analyses. This chapter summarizes some conclusions from the analyses and suggests future research directions in this field.

Through the literature review, it was found that no previous research addressed all the important characteristics arising from scheduling problem of semiconductor final test. In addition, most of the research has been theoretically oriented rather than focused on industrial application. With this mind, an in-depth study of the wafer testing process as well as the scheduling process for the semiconductor test facilities was undertaken.

The relevant research in the area of scheduling of semiconductor test can be divided into two main fields based on the scheduling objective: research with due date related objective and research with throughput related objective. The due date related objective is often applied to the ASIC market, in which meeting the customer specified delivery date is the most important criteria. Throughput related objective is often applied to standard IC device market, in which products are often made-to-stock. Because the scheduling problem of the semiconductor test process involves complex scheduling issues such as multiple machines, multiple machine type, multiple test heads, multiple job type, precedence constraint, and sequence dependent setup times, the research in this area has not addressed the full scale problem that include all the characteristics. The heuristics presented in this research address all the above characteristics in an effect to minimize makespan.

Two heuristics, Lot Optimization (LO) and Process Optimization (PO), were developed with the objective of minimizing the makespan required to finish all the wafer lots. An

experimented analysis was conducted to evaluate the heuristics in static situation. The analysis includes three production scenarios: low product demand, medium product demand and high product demand. The heuristics were applied using the suggested initial tester configuration developed in this research.

Based on this experimental analysis, it was concluded that in a static situation:

1. The schedules generated by PO Heuristic usually have lower makespan than the schedules generated by the LO and LOC Heuristics for all demand levels.
2. Both the LO and PO heuristics can generate schedules with makespan very close to the lower bound for low product demand (within 1.5%).
3. PO Heuristic normally generates lowest makespan schedule with MAST settings of 4.00 or 4.65 hours.
4. LO Heuristic normally generates lowest makespan schedule with MAST settings of 0.5 or 0.65 hours.

After the static analysis, two dynamic case studies were presented to address the heuristic performance in a dynamic manufacturing environment. The case study data were obtained from an actual manufacturing environment. The results of the heuristic approaches were compared to the actual schedule executed in the manufacturing facility. The conclusions drawn from the analyses are summarized as follows:

1. The schedules generated by the heuristics developed in this research reduced the makespan compared to the actual schedule. In the case analyses, the makespan of the schedules generated by the heuristics was 23% - 45% less than the makespan of actual schedule.
2. Although the tester constraint limits the flexibility of the manufacturing environment, the heuristics developed in this thesis research can incorporate the tester constraint and generate schedules that improve on the actual schedules with respect to makespan.

A decision support tool was developed in this research to obtain real-time information from the manufacturing database and provide real-time scheduling support for the company. A prototype version of the program, W*afer Test Scheduler*, has been tested on the test shop floor at an actual industrial facility.

Several areas of future research include:

- Developing cost measures to evaluate the cost of makespan and work-in-process levels and compare the performance of the heuristics using these measures;
- Developing heuristics that provide a compromise between makespan and
- Developing more refined initial optimum tester configuration that incorporates the expected test station available time (to incorporate expected down time and preventive maintenance);
- Implementing the heuristics as part of a decision support system, in which the manufacturing planner can modify the schedules developed by the heuristics before they are executed in the test facility;
- Developing the heuristics into a multi-tier client server application, in which planner can access the planning software and scheduling information through Internet; and
- Developing an animated simulation model of the testing facility so that the manufacturing planner can visualize the results of the schedules.

Other areas in which the study can be expanded are to consider a wider variety of product types products and new test stations, in which the new products can be tested on all test stations but the old products can be only tested on old test stations. In fact, this may be next scenario that the company faces.

In summary, the heuristics presented in this research have been developed, tested, analyzed and implemented successfully. A realistic scheduling method has been presented to improve the production scheduling of semiconductor test processes in an actual industrial application.

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APPENDIX A

RESULTS OF STATIC ANALYSIS

Table A-1. Results for Low Demand and (70% H, 30% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Against Lower Bound	MFT	AWIP
LOW	70%, 30%	LO	0.00	54.33	126.35%	44.79	16.49
	70%, 30%	LO	0.15	54.33	126.35%	44.79	16.49
	70%, 30%	LO	0.50	50.60	117.67%	44.79	17.70
	70%, 30%	LO	0.65	43.65	101.51%	40.92	18.75
	70%, 30%	LO	4.00	43.65	101.51%	40.92	18.75
	70%, 30%	LO	4.65	43.65	101.51%	40.92	18.75
	70%, 30%	LOc	0.00	69.67	162.02%	47.75	13.71
	70%, 30%	LOc	0.15	69.67	162.02%	47.75	13.71
	70%, 30%	LOc	0.50	53.21	123.74%	45.50	17.10
	70%, 30%	LOc	0.65	51.83	120.53%	41.85	16.15
	70%, 30%	LOc	4.00	46.03	107.05%	41.27	17.93
	70%, 30%	LOc	4.65	46.03	107.05%	41.27	17.93
	70%, 30%	PO	0.00	51.83	120.53%	42.90	16.55
	70%, 30%	PO	0.15	51.83	120.53%	42.90	16.55
	70%, 30%	PO	0.50	43.65	101.51%	41.08	18.82
	70%, 30%	PO	0.65	43.65	101.51%	41.08	18.82
	70%, 30%	PO	4.00	43.65	101.51%	41.08	18.82
	70%, 30%	PO	4.65	43.65	101.51%	41.08	18.82
	70%, 30%	POc	0.00	66.98	155.77%	46.16	13.78
	70%, 30%	POc	0.15	66.98	155.77%	46.16	13.78
	70%, 30%	POc	0.50	43.65	101.51%	41.08	18.82
	70%, 30%	POc	0.65	43.65	101.51%	41.08	18.82
	70%, 30%	POc	4.00	43.65	101.51%	41.08	18.82
	70%, 30%	POc	4.65	43.65	101.51%	41.08	18.82

Table A-2. Results for Low Demand and (50%H , 50% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
LOW	50%, 50%	LO	0.00	51.83	120.53%	42.72	16.48
	50%, 50%	LO	0.15	51.83	120.53%	42.72	16.48
	50%, 50%	LO	0.50	50.04	116.02%	42.94	17.16
	50%, 50%	LO	0.65	43.15	100.35%	40.49	18.77
	50%, 50%	LO	4.00	43.15	100.35%	40.49	18.77
	50%, 50%	LO	4.65	43.15	100.35%	40.49	18.77
	50%, 50%	LOc	0.00	56.33	131.00%	43.17	15.33
	50%, 50%	LOc	0.15	56.33	131.00%	43.17	15.33
	50%, 50%	LOc	0.50	52.68	122.51%	43.28	16.43
	50%, 50%	LOc	0.65	52.68	122.51%	41.40	15.72
	50%, 50%	LOc	4.00	47.00	109.30%	40.83	17.37
	50%, 50%	LOc	4.65	47.00	109.30%	40.83	17.37
	50%, 50%	PO	0.00	48.68	113.21%	42.05	17.28
	50%, 50%	PO	0.15	48.68	113.21%	42.05	17.28
	50%, 50%	PO	0.50	47.36	110.14%	42.24	17.84
	50%, 50%	PO	0.65	47.36	110.14%	42.24	17.84
	50%, 50%	PO	4.00	43.15	100.35%	40.52	18.78
	50%, 50%	PO	4.65	43.15	100.35%	40.52	18.78
	50%, 50%	POc	0.00	54.33	126.35%	43.14	15.88
	50%, 50%	POc	0.15	54.33	126.35%	43.14	15.88
	50%, 50%	POc	0.50	51.83	120.53%	43.20	16.67
	50%, 50%	POc	0.65	51.83	120.53%	43.20	16.67
	50%, 50%	POc	4.00	46.03	107.05%	40.86	17.75
	50%, 50%	POc	4.65	46.03	107.05%	40.86	17.75

Table A-3. Results for Low Demand and (20% H, 80% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
LOW	20%,80%	LO	0.00	64.58	150.18%	46.60	14.43
	20%,80%	LO	0.15	64.58	150.18%	46.60	14.43
	20%,80%	LO	0.50	49.28	114.60%	42.80	17.37
	20%,80%	LO	0.65	43.15	100.35%	40.49	18.77
	20%,80%	LO	4.00	43.15	100.35%	40.49	18.77
	20%,80%	LO	4.65	43.15	100.35%	40.49	18.77
	20%,80%	LOc	0.00	64.68	150.42%	46.60	14.41
	20%,80%	LOc	0.15	64.68	150.42%	46.60	14.41
	20%,80%	LOc	0.50	53.67	124.81%	43.37	16.16
	20%,80%	LOc	0.65	53.67	124.81%	41.32	15.40
	20%,80%	LOc	4.00	45.83	106.58%	40.54	17.69
	20%,80%	LOc	4.65	45.83	106.58%	40.54	17.69
	20%,80%	PO	0.00	87.73	204.02%	58.10	13.25
	20%,80%	PO	0.15	65.79	153.00%	50.34	15.30
	20%,80%	PO	0.50	43.15	100.35%	40.23	18.65
	20%,80%	PO	0.65	43.15	100.35%	40.23	18.65
	20%,80%	PO	4.00	43.15	100.35%	40.23	18.65
	20%,80%	PO	4.65	43.15	100.35%	40.23	18.65
	20%,80%	POc	0.00	87.73	204.02%	58.10	13.25
	20%,80%	POc	0.15	65.79	153.00%	50.34	15.30
	20%,80%	POc	0.50	53.67	124.81%	42.57	15.86
	20%,80%	POc	0.65	53.67	124.81%	42.57	15.86
	20%,80%	POc	4.00	45.83	106.58%	41.06	17.92
	20%,80%	POc	4.65	45.83	106.58%	41.06	17.92

Table A-4. Results for Medium Demand and (70% H, 30% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Against Lower Bound	MFT	AWIP
MEDIUM	70%, 30%	LO	0.00	101.97	207.13%	65.11	38.31
	70%, 30%	LO	0.15	101.97	207.13%	65.11	38.31
	70%, 30%	LO	0.50	85.83	174.34%	62.05	44.02
	70%, 30%	LO	0.65	90.37	183.57%	60.55	40.20
	70%, 30%	LO	4.00	98.89	200.87%	63.52	38.54
	70%, 30%	LO	4.65	94.95	192.87%	63.39	40.06
	70%, 30%	LOc	0.00	169.60	344.51%	85.37	30.20
	70%, 30%	LOc	0.15	169.60	344.51%	85.37	30.20
	70%, 30%	LOc	0.50	85.83	174.34%	63.15	44.15
	70%, 30%	LOc	0.65	96.91	196.85%	62.99	39.00
	70%, 30%	LOc	4.00	98.98	201.06%	64.56	39.14
	70%, 30%	LOc	4.65	94.65	192.26%	64.31	40.77
	70%, 30%	PO	0.00	92.27	187.43%	58.10	37.78
	70%, 30%	PO	0.15	92.27	187.43%	50.34	32.73
	70%, 30%	PO	0.50	79.65	161.79%	58.29	43.91
	70%, 30%	PO	0.65	79.77	162.04%	57.71	43.41
	70%, 30%	PO	4.00	65.23	132.50%	53.63	49.33
	70%, 30%	PO	4.65	65.23	132.50%	53.63	49.33
	70%, 30%	POc	0.00	107.10	217.55%	65.52	36.71
	70%, 30%	POc	0.15	107.10	217.55%	63.10	35.35
	70%, 30%	POc	0.50	81.93	166.42%	58.17	42.60
	70%, 30%	POc	0.65	81.27	165.08%	58.53	43.21
	70%, 30%	POc	4.00	69.73	141.64%	54.39	46.80
	70%, 30%	POc	4.65	68.95	140.06%	54.17	47.14

Table A-5. Results for Medium Demand and (50% H, 50% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
MEDIUM	50%, 50%	LO	0.00	89.00	179.38%	60.58	40.84
	50%, 50%	LO	0.15	89.00	179.38%	60.58	40.84
	50%, 50%	LO	0.50	84.68	170.67%	63.00	44.64
	50%, 50%	LO	0.65	89.95	181.30%	59.70	39.82
	50%, 50%	LO	4.00	99.95	201.45%	59.28	35.59
	50%, 50%	LO	4.65	92.97	187.38%	62.37	40.25
	50%, 50%	LOc	0.00	133.23	268.53%	69.66	31.37
	50%, 50%	LOc	0.15	133.23	268.53%	69.66	31.37
	50%, 50%	LOc	0.50	84.88	171.08%	63.10	44.60
	50%, 50%	LOc	0.65	92.33	186.09%	60.91	39.58
	50%, 50%	LOc	4.00	103.53	208.67%	62.95	36.48
	50%, 50%	LOc	4.65	101.40	204.37%	62.95	37.25
	50%, 50%	PO	0.00	88.90	179.18%	62.83	42.40
	50%, 50%	PO	0.15	86.30	173.94%	58.20	40.46
	50%, 50%	PO	0.50	78.65	158.52%	57.79	44.09
	50%, 50%	PO	0.65	78.65	158.52%	57.40	43.79
	50%, 50%	PO	4.00	65.88	132.78%	53.55	48.77
	50%, 50%	PO	4.65	65.41	131.84%	53.68	49.24
	50%, 50%	POc	0.00	170.88	344.41%	76.18	26.75
	50%, 50%	POc	0.15	164.42	331.39%	70.98	25.90
	50%, 50%	POc	0.50	79.70	160.64%	58.31	43.90
	50%, 50%	POc	0.65	79.70	160.64%	58.27	43.87
	50%, 50%	POc	4.00	65.88	132.78%	53.84	49.03
	50%, 50%	POc	4.65	65.38	131.77%	53.74	49.32

Table A-6. Results for Medium Demand and (20% H, 80% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
MEDIUM	20%,80%	LO	0.00	117.48	234.06%	72.62	37.09
	20%,80%	LO	0.15	117.48	234.06%	72.62	37.09
	20%,80%	LO	0.50	83.87	167.10%	61.48	43.98
	20%,80%	LO	0.65	88.70	176.72%	57.67	39.01
	20%,80%	LO	4.00	90.77	180.85%	59.75	39.50
	20%,80%	LO	4.65	90.77	180.85%	59.78	39.52
	20%,80%	LOc	0.00	119.15	237.39%	75.58	38.06
	20%,80%	LOc	0.15	119.15	237.39%	75.58	38.06
	20%,80%	LOc	0.50	83.87	167.10%	61.56	44.04
	20%,80%	LOc	0.65	89.70	178.71%	58.37	39.04
	20%,80%	LOc	4.00	92.72	184.73%	60.37	39.07
	20%,80%	LOc	4.65	92.72	184.73%	60.37	39.07
	20%,80%	PO	0.00	135.10	269.17%	78.29	34.77
	20%,80%	PO	0.15	110.93	221.01%	67.43	36.47
	20%,80%	PO	0.50	77.63	154.67%	57.71	44.60
	20%,80%	PO	0.65	77.63	154.67%	57.71	44.60
	20%,80%	PO	4.00	65.18	129.86%	53.61	49.35
	20%,80%	PO	4.65	63.57	126.65%	52.69	49.73
	20%,80%	POc	0.00	135.10	269.17%	78.66	34.93
	20%,80%	POc	0.15	110.93	221.01%	77.82	42.09
	20%,80%	POc	0.50	128.73	256.48%	65.82	30.68
	20%,80%	POc	0.65	129.18	257.37%	70.08	32.55
	20%,80%	POc	4.00	67.58	134.64%	53.63	47.61
	20%,80%	POc	4.65	63.57	126.65%	52.46	49.51

Table A-7. Results for High Demand and (70% H, 30% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
HIGH	70%, 30%	LO	0.00	147.00	179.16%	86.46	58.82
	70%, 30%	LO	0.15	147.00	179.16%	86.46	58.82
	70%, 30%	LO	0.50	115.67	140.98%	77.08	66.64
	70%, 30%	LO	0.65	135.33	164.94%	82.55	61.00
	70%, 30%	LO	4.00	150.13	182.97%	89.21	59.42
	70%, 30%	LO	4.65	150.13	182.97%	89.21	59.42
	70%, 30%	LOc	0.00	146.87	179.00%	83.26	56.69
	70%, 30%	LOc	0.15	146.87	179.00%	83.26	56.69
	70%, 30%	LOc	0.50	117.67	143.41%	79.82	64.37
	70%, 30%	LOc	0.65	134.25	163.62%	81.46	56.47
	70%, 30%	LOc	4.00	152.38	185.72%	92.01	60.38
	70%, 30%	LOc	4.65	153.36	186.91%	92.42	60.26
	70%, 30%	PO	0.00	132.60	161.61%	80.36	60.60
	70%, 30%	PO	0.15	135.40	165.02%	80.18	59.22
	70%, 30%	PO	0.50	107.15	130.59%	82.60	77.09
	70%, 30%	PO	0.65	107.15	130.59%	82.44	76.94
	70%, 30%	PO	4.00	91.85	111.94%	83.70	91.13
	70%, 30%	PO	4.65	92.28	112.47%	84.78	91.87
	70%, 30%	POc	0.00	295.57	360.23%	113.17	38.29
	70%, 30%	POc	0.15	282.23	343.97%	107.54	38.10
	70%, 30%	POc	0.50	116.03	141.41%	83.41	71.89
	70%, 30%	POc	0.65	116.03	141.41%	83.31	71.80
	70%, 30%	POc	4.00	95.83	116.79%	84.16	87.82
	70%, 30%	POc	4.65	96.71	117.87%	84.71	87.59

Table A-8. Results for High Demand and (50% H, 50% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
HIGH	50%, 50%	LO	0.00	130.02	157.24%	78.45	60.34
	50%, 50%	LO	0.15	132.02	159.66%	78.45	59.42
	50%, 50%	LO	0.50	116.17	140.49%	76.66	65.99
	50%, 50%	LO	0.65	137.77	166.61%	81.80	59.37
	50%, 50%	LO	4.00	145.27	175.68%	86.53	59.56
	50%, 50%	LO	4.65	152.57	184.51%	88.44	57.97
	50%, 50%	LOc	0.00	129.60	156.73%	78.29	60.41
	50%, 50%	LOc	0.15	129.60	156.73%	78.29	60.41
	50%, 50%	LOc	0.50	118.67	143.51%	77.53	65.33
	50%, 50%	LOc	0.65	144.25	174.45%	87.23	60.47
	50%, 50%	LOc	4.00	152.38	184.28%	90.42	59.34
	50%, 50%	LOc	4.65	148.28	179.32%	90.29	60.89
	50%, 50%	PO	0.00	134.13	162.21%	79.91	59.58
	50%, 50%	PO	0.15	119.15	144.09%	77.50	65.04
	50%, 50%	PO	0.50	108.10	130.73%	82.31	76.14
	50%, 50%	PO	0.65	108.10	130.73%	82.24	76.08
	50%, 50%	PO	4.00	91.85	111.08%	82.66	89.99
	50%, 50%	PO	4.65	92.28	111.60%	82.58	89.49
	50%, 50%	POc	0.00	221.33	267.66%	94.85	42.85
	50%, 50%	POc	0.15	208.53	252.18%	90.83	43.56
	50%, 50%	POc	0.50	114.04	137.91%	82.70	72.52
	50%, 50%	POc	0.65	114.07	137.95%	82.80	72.59
	50%, 50%	POc	4.00	92.38	111.72%	82.55	89.36
	50%, 50%	POc	4.65	92.28	111.60%	81.67	88.50

Table A-9. Results for High Demand and (20% H, 80% G) Product Mix

Demand	Mix	Heuristic	MAST	Makespan	Performance Measure Against Lower Bound	MFT	AWIP
HIGH	20%,80%	LO	0.00	185.02	221.18%	99.96	54.03
	20%,80%	LO	0.15	185.02	221.18%	99.96	54.03
	20%,80%	LO	0.50	114.65	137.06%	74.31	64.81
	20%,80%	LO	0.65	124.22	148.50%	75.25	60.58
	20%,80%	LO	4.00	149.46	178.67%	84.85	56.77
	20%,80%	LO	4.65	140.32	167.75%	83.98	59.85
	20%,80%	LOc	0.00	185.82	222.14%	100.31	53.98
	20%,80%	LOc	0.15	185.82	222.14%	100.31	53.98
	20%,80%	LOc	0.50	119.08	142.36%	76.85	64.54
	20%,80%	LOc	0.65	139.38	166.62%	83.39	59.83
	20%,80%	LOc	4.00	154.36	184.53%	88.56	57.37
	20%,80%	LOc	4.65	153.22	183.17%	87.95	57.40
	20%,80%	PO	0.00	200.83	240.08%	102.32	59.58
	20%,80%	PO	0.15	178.75	213.69%	92.01	65.04
	20%,80%	PO	0.50	109.23	130.58%	81.14	74.28
	20%,80%	PO	0.65	112.63	134.64%	81.33	72.21
	20%,80%	PO	4.00	91.85	109.80%	81.45	88.68
	20%,80%	PO	4.65	91.13	108.94%	81.56	89.50
	20%,80%	POc	0.00	200.83	240.08%	102.32	59.58
	20%,80%	POc	0.15	178.75	213.69%	93.26	65.04
	20%,80%	POc	0.50	111.65	133.47%	81.70	73.18
	20%,80%	POc	0.65	112.63	134.64%	81.91	72.72
	20%,80%	POc	4.00	92.38	110.44%	79.97	86.57
	20%,80%	POc	4.65	92.28	110.32%	80.71	87.46

APPENDIX B

RESULTS OF ANOVA AND TUKEY'S ANALYSIS

The following factors and levels are used in the statistical analysis.

Factor	Levels	Values	Real Meanings					
Demand	3	-1 0 1	Low	Medium	High			
Mix	3	-1 0 1	70/30	50/50	20/80			
Heuristic	4	-2 –1 1 2	Lo	Loc	Po	Poc		
MAST	6	-3,-2,-1,1,2,3	0	0.15	0.5	0.65	4	4.65

Split 1/9 – LOW demand with 70%30% mix(Demand = -1, Mix = -1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     320.71     320.71     106.90    5.57  0.009
MAST        5    1267.64    1267.64     253.53   13.21  0.000
Error      15     287.83     287.83      19.19
Total      23    1876.18

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     19.577     19.577      6.526    4.20  0.024
MAST        5     87.580     87.580     17.516   11.28  0.000
Error      15     23.292     23.292      1.553
Total      23    130.449

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3    14.0800    14.0800     4.6933    7.10  0.003
MAST        5    56.0937    56.0937    11.2187   16.97  0.000
Error      15     9.9162     9.9162     0.6611
Total      23    80.0899

Tukey 95.0% Simultaneous Confidence Intervals Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:
MAST     Lower    Center     Upper  -------+---------+---------+---------
-2     -10.05     -0.00    10.053                   (---------*---------)
-1     -22.98    -12.93    -2.872      (---------*---------)
 1     -25.06    -15.01    -4.954    (---------*---------)
 2     -26.51    -16.46    -6.404  (----------*---------)
 3     -26.51    -16.46    -6.404  (----------*---------)
                                  -------+---------+---------+---------
                                        -20       -10         0
MAST = -2 subtracted from:
MAST     Lower    Center     Upper  -------+---------+---------+---------
-1     -22.98    -12.92    -2.872      (---------*---------)
 1     -25.06    -15.01    -4.954    (---------*---------)
 2     -26.51    -16.46    -6.404  (----------*---------)
 3     -26.51    -16.46    -6.404  (----------*---------)
                                  -------+---------+---------+---------
                                        -20       -10         0
MAST = -1 subtracted from:
MAST     Lower    Center     Upper  -------+---------+---------+---------
 1     -12.14    -2.082     7.971                (---------*---------)
 2     -13.59    -3.532     6.521              (---------*----------)
 3     -13.59    -3.532     6.521              (---------*----------)
                                  -------+---------+---------+---------
                                        -20       -10         0
MAST = 1 subtracted from:
MAST     Lower    Center     Upper  -------+---------+---------+---------
 2     -11.50    -1.450     8.603                (----------*---------)
 3     -11.50    -1.450     8.603                (----------*---------)
                                  -------+---------+---------+---------
                                        -20       -10         0
MAST = 2 subtracted from:
MAST     Lower    Center     Upper  -------+---------+---------+---------
 3     -10.05 -0.000000     10.05                   (---------*---------)
                                  -------+---------+---------+---------
```

```
                                        -20       -10         0
Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
-2            -0.00       3.097    -0.000     1.0000
-1           -12.93       3.097    -4.173     0.0087
 1           -15.01       3.097    -4.845     0.0024
 2           -16.46       3.097    -5.313     0.0010
 3           -16.46       3.097    -5.313     0.0010

MAST = -2 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
-1           -12.92       3.097    -4.173     0.0087
 1           -15.01       3.097    -4.845     0.0024
 2           -16.46       3.097    -5.313     0.0010
 3           -16.46       3.097    -5.313     0.0010

MAST = -1 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 1           -2.082       3.097    -0.672     0.9825
 2           -3.532       3.097    -1.140     0.8570
 3           -3.532       3.097    -1.140     0.8570

MAST = 1 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 2           -1.450       3.097   -0.4681     0.9966
 3           -1.450       3.097   -0.4681     0.9966

MAST = 2 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 3        -0.000000       3.097 -0.000000      1.000
```

Split 2/9 – LOW demand with 50%50% mix(Demand = -1, Mix = 0)

General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3    132.207    132.207     44.069   20.90  0.000
MAST        5    262.826    262.826     52.565   24.93  0.000
Error      15     31.628     31.628      2.109
Total      23    426.661

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     2.6639     2.6639     0.8880    3.41  0.045
MAST        5    22.1617    22.1617     4.4323   17.04  0.000
Error      15     3.9008     3.9008     0.2601
Total      23    28.7265

Analysis of Variance for AWIP, using Adjusted SS for Tests
```

```
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3    11.7052    11.7052     3.9017   28.09  0.000
MAST        5    14.9480    14.9480     2.9896   21.52  0.000
Error      15     2.0838     2.0838     0.1389
Total      23    28.7370

Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
-2       -3.33    -0.000     3.333                     (-------*-------)
-1       -5.65    -2.315     1.018               (-------*--------)
 1       -7.37    -4.038    -0.705            (-------*-------)
 2      -11.29    -7.960    -4.627   (-------*-------)
 3      -11.29    -7.960    -4.627   (-------*-------)
                                    ---------+---------+---------+-------
                                           -8.0      -4.0       0.0


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
-1       -5.65    -2.315     1.018               (-------*--------)
 1       -7.37    -4.037    -0.705            (-------*-------)
 2      -11.29    -7.960    -4.627   (-------*-------)
 3      -11.29    -7.960    -4.627   (-------*-------)
                                    ---------+---------+---------+-------
                                           -8.0      -4.0       0.0


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
 1      -5.055    -1.723     1.610                (--------*-------)
 2      -8.978    -5.645    -2.312        (-------*-------)
 3      -8.978    -5.645    -2.312        (-------*-------)
                                    ---------+---------+---------+-------
                                           -8.0      -4.0       0.0



MAST = 1 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
 2      -7.255    -3.922   -0.5900            (-------*--------)
 3      -7.255    -3.922   -0.5900            (-------*--------)
                                    ---------+---------+---------+-------
                                           -8.0      -4.0       0.0

MAST = 2 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
 3      -3.333 -0.000000     3.333                     (-------*-------)
                                    ---------+---------+---------+-------
                                           -8.0      -4.0       0.0


Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST
```

```
MAST = -3 subtracted from:
Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
-2           -0.000       1.027    -0.000     1.0000
-1           -2.315       1.027    -2.255     0.2707
 1           -4.038       1.027    -3.932     0.0138
 2           -7.960       1.027    -7.752     0.0000
 3           -7.960       1.027    -7.752     0.0000

MAST = -2 subtracted from:

Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
-1           -2.315       1.027    -2.255     0.2707
 1           -4.037       1.027    -3.932     0.0138
 2           -7.960       1.027    -7.752     0.0000
 3           -7.960       1.027    -7.752     0.0000

MAST = -1 subtracted from:

Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 1           -1.723       1.027    -1.678     0.5649
 2           -5.645       1.027    -5.498     0.0007
 3           -5.645       1.027    -5.498     0.0007

MAST = 1 subtracted from:

Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 2           -3.922       1.027    -3.820     0.0170
 3           -3.922       1.027    -3.820     0.0170

MAST = 2 subtracted from:

Level    Difference       SE of             Adjusted
MAST       of Means  Difference   T-Value    P-Value
 3        -0.000000       1.027 -0.000000      1.000
```

Split 3/9 – LOW demand with 20%80% mix (Demand = -1, Mix = 1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     167.87     167.87      55.96    1.48  0.260
MAST        5    3369.96    3369.96     673.99   17.85  0.000
Error      15     566.50     566.50      37.77
Total      23    4104.33

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     37.666     37.666     12.555    1.59  0.233
MAST        5    495.913    495.913     99.183   12.57  0.000
Error      15    118.363    118.363      7.891
Total      23    651.942

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
```

```
Heuristi    3     7.9992     7.9992     2.6664    3.88  0.031
MAST        5    66.6123    66.6123    13.3225   19.38  0.000
Error      15    10.3134    10.3134     0.6876
Total      23    84.9250

Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
-2     -25.07    -10.97      3.13            (-------*------)
-1     -40.34    -26.24    -12.13     (------*------)
 1     -41.87    -27.77    -13.67    (------*------)
 2     -45.79    -31.69    -17.59  (------*------)
 3     -45.79    -31.69    -17.59  (------*------)
                                  ---+---------+---------+---------+---
                                    -40       -20         0        20



MAST = -2 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
-1     -29.37    -15.27    -1.164          (------*------)
 1     -30.90    -16.80    -2.696          (------*------)
 2     -34.82    -20.72    -6.616        (------*------)
 3     -34.82    -20.72    -6.616        (------*------)
                                  ---+---------+---------+---------+---
                                    -40       -20         0        20


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 1     -15.64    -1.532    12.571               (------*------)
 2     -19.56    -5.452     8.651             (------*------)
 3     -19.56    -5.452     8.651             (------*------)
                                  ---+---------+---------+---------+---
                                    -40       -20         0        20


MAST = 1 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 2     -18.02    -3.920     10.18               (------*------)
 3     -18.02    -3.920     10.18               (------*------)
                                  ---+---------+---------+---------+---
                                    -40       -20         0        20


MAST = 2 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 3     -14.10 -0.000000     14.10                 (------*------)
                                  ---+---------+---------+---------+---
                                    -40       -20         0        20

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST
```

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-10.97	4.345	-2.524	0.1779
-1	-26.24	4.345	-6.038	0.0003
1	-27.77	4.345	-6.391	0.0002
2	-31.69	4.345	-7.293	0.0000
3	-31.69	4.345	-7.293	0.0000

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-15.27	4.345	-3.513	0.0305
1	-16.80	4.345	-3.866	0.0156
2	-20.72	4.345	-4.768	0.0028
3	-20.72	4.345	-4.768	0.0028

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	-1.532	4.345	-0.353	0.9991
2	-5.452	4.345	-1.255	0.8038
3	-5.452	4.345	-1.255	0.8038

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-3.920	4.345	-0.9021	0.9400
3	-3.920	4.345	-0.9021	0.9400

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	-0.000000	4.345	-0.000000	1.000

🪶 Split 4/9 – MEDIUM demand with 70%30% mix (Demand = 0, Mix = -1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     5541.6     5541.6     1847.2    7.19  0.003
MAST        5     6279.0     6279.0     1255.8    4.89  0.008
Error      15     3855.6     3855.6      257.0
Total      23    15676.2

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     816.48     816.48     272.16    8.81  0.001
MAST        5     334.68     334.68      66.94    2.17  0.113
Error      15     463.62     463.62      30.91
Total      23    1614.79

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3    108.987    108.987     36.329    3.95  0.029
MAST        5    388.876    388.876     77.775    8.45  0.001
Error      15    138.119    138.119      9.208
Total      23    635.982


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
-2      -36.79     -0.00   36.7945             (----------*----------)
-1      -71.22    -34.43    2.3695    (---------*----------)
 1      -67.45    -30.66    6.1395     (---------*----------)
 2      -71.32    -34.53    2.2670    (---------*----------)
 3      -73.58    -36.79    0.0045   (---------*----------)
                                    --+---------+---------+---------+----
                                     -70       -35         0        35


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
-1      -71.22    -34.42   2.36954    (---------*----------)
 1      -67.45    -30.65   6.13954     (---------*----------)
 2      -71.32    -34.53   2.26704    (---------*----------)
 3      -73.58    -36.79   0.00454   (---------*----------)
                                    --+---------+---------+---------+----
                                     -70       -35         0        35


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
 1      -33.02     3.770     40.56              (---------*----------)
 2      -36.90    -0.103     36.69            (----------*---------)
 3      -39.16    -2.365     34.43            (---------*----------)
                                    --+---------+---------+---------+----
                                     -70       -35         0        35
```

MAST = 1 subtracted from:

```
MAST     Lower    Center     Upper  --+---------+---------+---------+----
 2      -40.67    -3.872     32.92            (----------*---------)
 3      -42.93    -6.135     30.66            (---------*----------)
                                    --+---------+---------+---------+----
                                     -70       -35         0        35
```

MAST = 2 subtracted from:

```
MAST     Lower    Center     Upper  --+---------+---------+---------+----
 3      -39.06    -2.263     34.53             (---------*----------)
                                    --+---------+---------+---------+----
                                     -70       -35         0        35
```

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-0.00	11.34	-0.000	1.0000
-1	-34.43	11.34	-3.037	0.0737
1	-30.66	11.34	-2.704	0.1320
2	-34.53	11.34	-3.046	0.0725
3	-36.79	11.34	-3.245	0.0504

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-34.42	11.34	-3.037	0.0737
1	-30.65	11.34	-2.704	0.1320
2	-34.53	11.34	-3.046	0.0725
3	-36.79	11.34	-3.245	0.0504

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	3.770	11.34	0.3325	0.9993
2	-0.103	11.34	-0.0090	1.0000
3	-2.365	11.34	-0.2086	0.9999

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-3.872	11.34	-0.3416	0.9992
3	-6.135	11.34	-0.5412	0.9934

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	-2.263	11.34	-0.1996	1.000

Split 5/9 – MEDIUM demand with 50%50% mix (Demand = 0, Mix = 0)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     3530.7     3530.7     1176.9    2.23  0.127
MAST        5     7079.4     7079.4     1415.9    2.69  0.063
Error      15     7909.8     7909.8      527.3
Total      23    18519.8

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     178.18     178.18      59.39    3.31  0.049
MAST        5     316.67     316.67      63.33    3.53  0.026
Error      15     269.01     269.01      17.93
Total      23     763.86

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     196.78     196.78      65.59    2.28  0.121
MAST        5     372.90     372.90      74.58    2.60  0.070
Error      15     431.08     431.08      28.74
Total      23    1000.75


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
-2      -54.97     -2.27     50.44           (------------*------------)
-1      -91.23    -38.53     14.18  (------------*------------)
 1      -88.05    -35.35     17.36   (------------*------------)
 2      -89.39    -36.69     16.01   (------------*------------)
 3      -91.91    -39.21     13.49  (------------*------------)
                                    ---+---------+---------+---------+---
                                      -80       -40         0        40


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
-1      -88.96    -36.26     16.44   (------------*------------)
 1      -85.78    -33.08     19.62    (------------*------------)
 2      -87.13    -34.43     18.27   (------------*------------)
 3      -89.65    -36.95     15.75   (------------*------------)
                                    ---+---------+---------+---------+---
                                      -80       -40         0        40


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 1      -49.52    3.1800     55.88            (------------*------------)
 2      -50.87    1.8325     54.53           (------------*------------)
 3      -53.39   -0.6875     52.01           (------------*------------)
                                    ---+---------+---------+---------+---
                                      -80       -40         0        40
```

MAST = 1 subtracted from:

```
MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 2      -54.05    -1.348     51.35           (-------------*------------)
 3      -56.57    -3.868     48.83           (------------*------------)
                                    ---+---------+---------+---------+---
                                      -80       -40         0        40
```

MAST = 2 subtracted from:

```
MAST     Lower    Center     Upper  ---+---------+---------+---------+---
 3      -55.22    -2.520     50.18           (------------*-------------)
                                    ---+---------+---------+---------+---
                                      -80       -40         0        40
```

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-2.27	16.24	-0.139	1.0000
-1	-38.53	16.24	-2.373	0.2264
1	-35.35	16.24	-2.177	0.3032
2	-36.69	16.24	-2.260	0.2686
3	-39.21	16.24	-2.415	0.2120

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-36.26	16.24	-2.233	0.2794
1	-33.08	16.24	-2.037	0.3677
2	-34.43	16.24	-2.120	0.3283
3	-36.95	16.24	-2.275	0.2624

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	3.1800	16.24	0.19584	1.000
2	1.8325	16.24	0.11286	1.000
3	-0.6875	16.24	-0.04234	1.000

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-1.348	16.24	-0.0830	1.0000
3	-3.868	16.24	-0.2382	0.9999

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	-2.520	16.24	-0.1552	1.000

Split 6/9 – MEDIUM demand with 20%80% mix (Demand = 0, Mix = 1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      944.1      944.1      314.7    1.17  0.355
MAST        5     7583.1     7583.1     1516.6    5.62  0.004
Error      15     4048.3     4048.3      269.9
Total      23    12575.5

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      89.49      89.49      29.83    1.89  0.175
MAST        5    1453.16    1453.16     290.63   18.40  0.000
Error      15     236.97     236.97      15.80
Total      23    1779.62

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      63.79      63.79      21.26    0.87  0.478
MAST        5     210.99     210.99      42.20    1.73  0.189
Error      15     366.52     366.52      24.43
Total      23     641.30


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  -----+---------+---------+---------+-
-2     -49.79    -12.09     25.62             (----------*---------)
-1     -70.89    -33.18      4.52       (----------*---------)
 1     -68.11    -30.41      7.30        (---------*----------)
 2     -85.35    -47.65     -9.94   (---------*----------)
 3     -86.75    -49.05    -11.35  (----------*----------)
                                  -----+---------+---------+---------+-
                                      -70       -35         0        35


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  -----+---------+---------+---------+-
-1     -58.80    -21.10   16.6054         (----------*----------)
 1     -56.02    -18.32   19.3829          (----------*----------)
 2     -73.26    -35.56    2.1429     (----------*----------)
 3     -74.67    -36.97    0.7379     (---------*----------)
                                  -----+---------+---------+---------+-
                                      -70       -35         0        35


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  -----+---------+---------+---------+-
 1     -34.93      2.78     40.48               (----------*----------)
 2     -52.17    -14.46     23.24           (----------*----------)
 3     -53.57    -15.87     21.84           (---------*----------)
                                  -----+---------+---------+---------+-
                                      -70       -35         0        35
```

MAST = 1 subtracted from:

```
MAST     Lower    Center     Upper  -----+---------+---------+---------+-
 2      -54.94    -17.24     20.46           (----------*----------)
 3      -56.35    -18.65     19.06           (----------*---------)
                                    -----+---------+---------+---------+-
                                        -70       -35         0        35
```

MAST = 2 subtracted from:

```
MAST     Lower    Center     Upper  -----+---------+---------+---------+-
 3      -39.11    -1.405     36.30                (----------*---------)
                                    -----+---------+---------+---------+-
                                        -70       -35         0        35
```

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-12.09	11.62	-1.040	0.8968
-1	-33.18	11.62	-2.856	0.1015
1	-30.41	11.62	-2.617	0.1527
2	-47.65	11.62	-4.101	0.0099
3	-49.05	11.62	-4.222	0.0079

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-21.10	11.62	-1.816	0.4849
1	-18.32	11.62	-1.577	0.6242
2	-35.56	11.62	-3.061	0.0705
3	-36.97	11.62	-3.182	0.0566

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	2.78	11.62	0.239	0.9999
2	-14.46	11.62	-1.245	0.8086
3	-15.87	11.62	-1.366	0.7455

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-17.24	11.62	-1.484	0.6787
3	-18.65	11.62	-1.605	0.6077

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	-1.405	11.62	-0.1209	1.000

Split 7/9 – HIGH demand with 70%30% mix (Demand = 1, Mix = -1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3       9442       9442       3147    1.56  0.240
MAST        5      18466      18466       3693    1.83  0.166
Error      15      30201      30201       2013
Total      23      58109

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     353.69     353.69     117.90    1.95  0.166
MAST        5     315.01     315.01      63.00    1.04  0.430
Error      15     909.02     909.02      60.60
Total      23    1577.72

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     1061.9     1061.9      354.0    3.10  0.059
MAST        5     1938.7     1938.7      387.7    3.39  0.030
Error      15     1714.6     1714.6      114.3
Total      23     4715.2


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
-2      -105.6     -2.64    100.34           (------------*------------)
-1      -169.4    -66.38     36.60   (------------*------------)
 1      -160.3    -57.32     45.66    (------------*------------)
 2      -160.9    -57.96     45.02    (------------*------------)
 3      -160.4    -57.39     45.59    (------------*------------)
                                    --+---------+---------+---------+----
                                    -160       -80         0        80


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
-1      -166.7    -63.74     39.23   (------------*------------)
 1      -157.7    -54.68     48.29    (------------*------------)
 2      -158.3    -55.33     47.65    (------------*------------)
 3      -157.7    -54.76     48.22    (------------*------------)
                                    --+---------+---------+---------+----
                                    -160       -80         0        80


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  --+---------+---------+---------+----
 1      -93.92     9.060     112.0            (------------*------------)
 2      -94.56     8.417     111.4            (------------*------------)
 3      -93.99     8.990     112.0            (------------*------------)
                                    --+---------+---------+---------+----
                                    -160       -80         0        80
```

MAST = 1 subtracted from:

MAST	Lower	Center	Upper	--+---------+---------+---------+----
2	-103.6	-0.6425	102.3	(------------*------------)
3	-103.0	-0.0700	102.9	(------------*------------)
				--+---------+---------+---------+----
				-160 -80 0 80

MAST = 2 subtracted from:

MAST	Lower	Center	Upper	--+---------+---------+---------+----
3	-102.4	0.5725	103.6	(------------*------------)
				--+---------+---------+---------+----
				-160 -80 0 80

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-2.64	31.73	-0.083	1.0000
-1	-66.38	31.73	-2.092	0.3414
1	-57.32	31.73	-1.807	0.4903
2	-57.96	31.73	-1.827	0.4789
3	-57.39	31.73	-1.809	0.4891

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-63.74	31.73	-2.009	0.3817
1	-54.68	31.73	-1.724	0.5381
2	-55.33	31.73	-1.744	0.5263
3	-54.76	31.73	-1.726	0.5368

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	9.060	31.73	0.2855	0.9997
2	8.417	31.73	0.2653	0.9998
3	8.990	31.73	0.2833	0.9997

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-0.6425	31.73	-0.02025	1.000
3	-0.0700	31.73	-0.00221	1.000

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	0.5725	31.73	0.01804	1.000

Split 8/9 – HIGH demand with 50%50% mix (Demand = 1, Mix = 0)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3       3805       3805       1268    1.27  0.321
MAST        5       5172       5172       1034    1.03  0.433
Error      15      15009      15009       1001
Total      23      23985

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      82.07      82.07      27.36    1.08  0.386
MAST        5     109.68     109.68      21.94    0.87  0.524
Error      15     378.34     378.34      25.22
Total      23     570.08

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      958.0      958.0      319.3    2.96  0.066
MAST        5     1359.6     1359.6      271.9    2.52  0.076
Error      15     1617.6     1617.6      107.8
Total      23     3935.2


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
-2       -79.0     -6.45     66.15        (-----------*-----------)
-1      -112.1    -39.53     33.07  (-----------*------------)
 1      -100.3    -27.72     44.87    (-----------*-----------)
 2      -105.9    -33.30     39.30   (-----------*------------)
 3      -105.0    -32.42     40.18   (------------*-----------)
                                    ---------+---------+---------+-------
                                           -60         0        60


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
-1      -105.7    -33.08     39.52   (-----------*------------)
 1       -93.9    -21.28     51.32     (-----------*------------)
 2       -99.5    -26.85     45.74    (------------*-----------)
 3       -98.6    -25.97     46.62     (-----------*-----------)
                                    ---------+---------+---------+-------
                                           -60         0        60


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  ---------+---------+---------+-------
 1      -60.79    11.802     84.40           (-----------*-----------)
 2      -66.37     6.225     78.82          (-----------*-----------)
 3      -65.49     7.107     79.70          (-----------*-----------)
                                    ---------+---------+---------+-------
                                           -60         0        60
```

MAST = 1 subtracted from:

```
MAST     Lower    Center     Upper  ---------+---------+---------+-------
 2      -78.17    -5.578     67.02        (-----------*-----------)
 3      -77.29    -4.695     67.90        (-----------*-----------)
                                    ---------+---------+---------+-------
                                           -60         0        60
```

MAST = 2 subtracted from:

```
MAST     Lower    Center     Upper  ---------+---------+---------+-------
 3      -71.71    0.8825     73.48         (-----------*-----------)
                                    ---------+---------+---------+-------
                                           -60         0        60
```

Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-6.45	22.37	-0.288	0.9997
-1	-39.53	22.37	-1.767	0.5129
1	-27.72	22.37	-1.239	0.8113
2	-33.30	22.37	-1.489	0.6760
3	-32.42	22.37	-1.449	0.6987

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-33.08	22.37	-1.479	0.6817
1	-21.28	22.37	-0.951	0.9263
2	-26.85	22.37	-1.201	0.8299
3	-25.97	22.37	-1.161	0.8479

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	11.802	22.37	0.5277	0.9941
2	6.225	22.37	0.2783	0.9997
3	7.107	22.37	0.3178	0.9995

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-5.578	22.37	-0.2494	0.9998
3	-4.695	22.37	-0.2099	0.9999

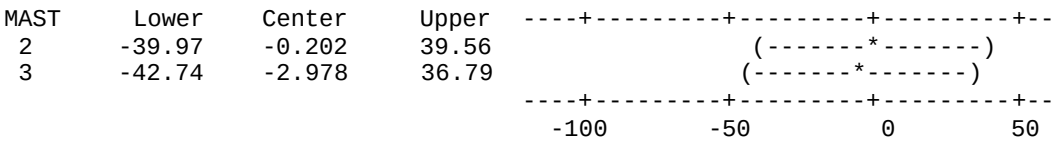
MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	0.8825	22.37	0.03946	1.000

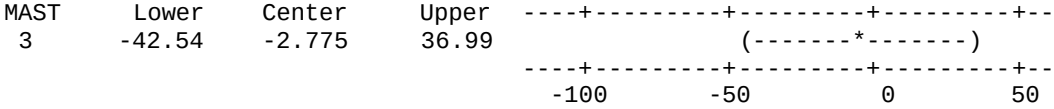
Split 9/9 – HIGH demand with 20%80% mix (Demand = 1, Mix = 1)
General Linear Model: Makespan, MFT, AWIP versus Heuristic, MAST

```
Analysis of Variance for Makespan, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3     3019.6     3019.6     1006.5    3.35  0.047
MAST        5    25332.9    25332.9     5066.6   16.88  0.000
Error      15     4503.1     4503.1      300.2
Total      23    32855.5

Analysis of Variance for MFT, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3      40.94      40.94      13.65    1.19  0.348
MAST        5    1710.28    1710.28     342.06   29.74  0.000
Error      15     172.55     172.55      11.50
Total      23    1923.77

Analysis of Variance for AWIP, using Adjusted SS for Tests
Source     DF     Seq SS     Adj SS     Adj MS       F      P
Heuristi    3    1614.24    1614.24     538.08   13.35  0.000
MAST        5     935.69     935.69     187.14    4.64  0.009
Error      15     604.39     604.39      40.29
Total      23    3154.32


Tukey 95.0% Simultaneous Confidence Intervals
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

MAST     Lower    Center     Upper  ----+---------+---------+---------+--
-2       -50.8    -11.04     28.72               (-------*-------)
-1      -119.2    -79.47    -39.71  (-------*-------)
 1      -110.7    -70.91    -31.15    (-------*-------)
 2      -110.9    -71.11    -31.35    (-------*-------)
 3      -113.7    -73.89    -34.12   (-------*-------)
                                   ----+---------+---------+---------+--
                                     -100       -50         0        50


MAST = -2 subtracted from:

MAST     Lower    Center     Upper  ----+---------+---------+---------+--
-1      -108.2    -68.43    -28.67    (-------*-------)
 1       -99.6    -59.87    -20.11      (-------*-------)
 2       -99.8    -60.07    -20.31      (-------*-------)
 3      -102.6    -62.85    -23.08     (-------*-------)
                                   ----+---------+---------+---------+--
                                     -100       -50         0        50


MAST = -1 subtracted from:

MAST     Lower    Center     Upper  ----+---------+---------+---------+--
 1      -31.20     8.563     48.33                   (-------*-------)
 2      -31.40     8.360     48.12                   (-------*-------)
 3      -34.18     5.585     45.35                  (-------*-------)
                                   ----+---------+---------+---------+--
                                     -100       -50         0        50
```

MAST = 1 subtracted from:



MAST = 2 subtracted from:



Tukey Simultaneous Tests
Response Variable Makespan
All Pairwise Comparisons among Levels of MAST

MAST = -3 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-2	-11.04	12.25	-0.901	0.9403
-1	-79.47	12.25	-6.487	0.0001
1	-70.91	12.25	-5.788	0.0004
2	-71.11	12.25	-5.804	0.0004
3	-73.89	12.25	-6.031	0.0003

MAST = -2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
-1	-68.43	12.25	-5.586	0.0006
1	-59.87	12.25	-4.887	0.0022
2	-60.07	12.25	-4.903	0.0022
3	-62.85	12.25	-5.130	0.0014

MAST = -1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
1	8.563	12.25	0.6989	0.9792
2	8.360	12.25	0.6824	0.9813
3	5.585	12.25	0.4559	0.9970

MAST = 1 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
2	-0.202	12.25	-0.0165	1.0000
3	-2.978	12.25	-0.2430	0.9999

MAST = 2 subtracted from:

Level MAST	Difference of Means	SE of Difference	T-Value	Adjusted P-Value
3	-2.775	12.25	-0.2265	0.9999

Results for: Demand = LOW

General Linear Model: Makespan versus Mix, Heuristic, MAST

```
Factor     Type Levels Values
Mix       fixed      3 -1  0  1
Heuristi  fixed      4 -2 -1  1  2
MAST      fixed      6 -3 -2 -1  1  2  3

Analysis of Variance for Makespan, using Adjusted SS for Tests
```

Source	DF	Seq SS	Adj SS	Adj MS	F	P	MC?
Mix	2	420.93	420.93	210.47	10.17	0.000	
Heuristi	3	445.04	445.04	148.35	7.17	0.001	✓
MAST	5	3832.91	3832.91	766.58	37.04	0.000	✓
Mix*Heuristi	6	175.75	175.75	29.29	1.42	0.241	
Mix*MAST	10	1067.52	1067.52	106.75	5.16	0.000	✓
Heuristi*MAST	15	265.09	265.09	17.67	0.85	0.616	✓
Error	30	620.87	620.87	20.70			
Total	71	6828.10					

Results for: Demand = MEDIUM

General Linear Model: Makespan versus Mix, Heuristic, MAST

```
Factor     Type Levels Values
Mix       fixed      3 -1  0  1
Heuristi  fixed      4 -2 -1  1  2
MAST      fixed      6 -3 -2 -1  1  2  3

Analysis of Variance for Makespan, using Adjusted SS for Tests
```

Source	DF	Seq SS	Adj SS	Adj MS	F	P	MC?
Mix	2	134.6	134.6	67.3	0.23	0.793	
Heuristi	3	6931.7	6931.7	2310.6	8.02	0.000	✓
MAST	5	20187.7	20187.7	4037.5	14.02	0.000	✓
Mix*Heuristi	6	3084.7	3084.7	514.1	1.78	0.136	
Mix*MAST	10	753.8	753.8	75.4	0.26	0.985	
Heuristi*MAST	15	7172.1	7172.1	478.1	1.66	0.116	✓
Error	30	8641.6	8641.6	288.1			
Total	71	46906.1					

Results for: Demand = HIGH

General Linear Model: Makespan versus Mix, Heuristic, MAST

```
Factor     Type Levels Values
Mix       fixed      3 -1  0  1
Heuristi  fixed      4 -2 -1  1  2
MAST      fixed      6 -3 -2 -1  1  2  3

Analysis of Variance for Makespan, using Adjusted SS for Tests
```

Source	DF	Seq SS	Adj SS	Adj MS	F	P	MC?
Mix	2	1840.0	1840.0	920.0	2.68	0.085	
Heuristi	3	10444.7	10444.7	3481.6	10.14	0.000	✓
MAST	5	44629.2	44629.2	8925.8	25.99	0.000	✓
Mix*Heuristi	6	5821.5	5821.5	970.3	2.83	0.027	
Mix*MAST	10	4341.7	4341.7	434.2	1.26	0.294	
Heuristi*MAST	15	39409.7	39409.7	2627.3	7.65	0.000	✓
Error	30	10302.6	10302.6	343.4			
Total	71	116789.5					

VITA

Yufeng Lu was born in Beijing, China. He graduated in July of 1995 from Tsinghua University in China with a Bachelor of Science degree in Mechanical Engineering. He joined Nestle (China) Ltd. as packaging engineer. While working at Nestle, he was active in several staff organizations and served as chairman of Nestle Club. In 1998, he came to U.S. and study at the Industrial And System Engineering Department of Virginia Tech. He received his Master of Science Degree in Industrial and Systems Engineering from Virginia Tech's Grado Department of Industrial and System Engineering in November of 2001.

Yufeng is a passionate "Go" player, a popular board chess game in China, Korea, and Japan. He won his first champion in a department tournament in Tsinghua University. He has remained active at Virginia Tech and assisted the organization of Yahoo SuperGo 2 Tournament in 2000. He likes swimming and playing computer games in his leisure time.