High Voltage Synchronous Rectifier Design Considerations

Oscar Nando Yu

Dissertation submitted to the faculty of the

Virginia Polytechnic Institute and State University
in partial fulfillment of the requirements for the
degree of

Doctor of Philosophy

In

Electrical Engineering

Jih-Sheng Lai, Chair

Qiang Li

John Michael Ruohoniemi

Steve C. Southward

Xiaoting Jia

March 16th, 2021

Blacksburg, Virginia

Keywords: llc-dcx, transformer, high voltage synchronous rectification, drain-source sensing, duty cycle rate limiting, sequential parallel switching, multilevel gate driving,

High Voltage Synchronous Rectifier Design Considerations

Oscar Nando Yu

(ABSTRACT)

The advent of wide band-gap semiconductors in power electronics has led to the scope of efficient power conversion being pushed further than ever before. This development has allowed for systems to operate at higher and higher voltages than previously achieved. One area of consideration during this high voltage transition is the synchronous rectifier, which is traditionally designed as an afterthought. Prior research in synchronous rectifiers have been limited to low voltage, high current converters. There is practically no research in high voltage synchronous rectification. Therefore, this dissertation focuses on discovering the unknown nuances behind high voltage synchronous rectifier design, and ultimately developing a practical, scalable solution. There are three main issues that must be addressed when designing a high voltage synchronous rectifier: (1) high voltage sensing; (2) light load effects; (3) accuracy.

The first hurdle to designing a high voltage SR system is the high voltage itself. Traditional methods of synchronous rectification (SR) attempt to directly sense voltage or current, which is not possible with high voltage. Therefore, a solution must be designed to limit the voltage seen by the sensing mechanism without sacrificing accuracy. In this dissertation, a novel blocking solution is proposed, analyzed, and tested to over 1-*kV*. The solution is practical enough to be implemented on practically any commercial drain-source SR controller.

The second hurdle is the light load effect of the SR system on the converter. A large amount of high voltage systems utilize a *LLC*-based DC transformers (DCX) to provide an

efficient means of energy conversion. The *LLC*-DCX's attractive attributes of soft-switching and high efficiency allure many architects to combine it with an SR system. However, direct implementation of SR on a *LLC*-DCX will result in a variety of light load oscillation issues, since the rectifier circuitry can excite the resonant tank through a false load transient phenomena. A universal limiting solution is proposed and analyzed, and is validated with a commercial SR controller.

The final hurdle is in optimizing the SR system itself. There is an inherent flaw with drain-source sensing, namely parasitic inductance in the drain-source sense loop. This parasitic inductance causes an error in the sensed voltage, resulting in early SR turn-off and increased losses through the parallel diode. The parasitic will always be present in the circuit, and current solutions are too complex to be implemented. Two solutions are proposed depending on the rectifier architecture: (1) multilevel gate driving for single switch rectifiers; (2) sequential parallel switching for parallel switch rectifiers.

In summary, this dissertation focuses on developing a practical and reliable high voltage SR solution for *LLC*-DCX converters. Three main issues are addressed: (1) high voltage sensing; (2) light load effects; (3) accuracy. Novel solutions are proposed for all three issues, and validated with commercial controllers.

High Voltage Synchronous Rectifier Design Considerations

Oscar Nando Yu

GENERAL AUDIENCE ABSTRACT

High voltage power electronics are becoming increasing popular in the electronics industry with the help of wide band-gap semiconductors. While high voltage power electronics research is prevalent, a key component of high voltage power converters, the synchronous rectifier, remains unexplored. Conventional synchronous rectifiers are implemented on high current circuits where diode losses are high. However, high voltage power electronics operate at much lower current levels, necessitating changes in current synchronous rectifier methods. This research aims to identify and tackle issues that will be faced by both systems and IC designers when attempting to implement high voltage synchronous rectifiers on *LLC*-DCXs. While development takes planes on a *LLC*-DCX, the research is applicable to most resonant converters and applications utilizing drain-source synchronous rectifier technology.

This dissertation focuses primarily on three areas of synchronous rectifier developments: (1) high voltage compatibility; (2) light load effects; (3) accuracy. The first issue opens the gate to high voltage synchronous rectifier research, by allowing high voltage sensing. The second issue explores issues that high voltage synchronous rectifiers can inadvertently influence on the *LLC*-DCX itself - a light load oscillation issue. The third issue explores novel methods of improving the sensing accuracy to further reduce losses for a single and parallel switch rectifier. In each of these areas, the underlying problem is root-caused, analyzed, and a solution proposed. The overarching goal of this dissertation is

to develop a practical, low-cost, universal synchronous rectifier system that can be scaled for commercial use.

To my parents,

Bang-er Shia

Yu-Liang Yu

Table of Contents

List of Figures

List of Tables

Chapter 1

Introduction

1.1 Background

With the worldwide developments in clean energy applications, electrification, electrification infrastructure, and information technology, emphasis on high efficiency high power electronics is greater than ever before. In information technology, the fast developing industry has fueled the needs in offline power supply development to keep up with the growing demands in the server industry. In the automotive industry, booming development in electric vehicle and self-driving development has fueled the need for novel automotive-qualified power electronics systems. For example, electric vehicles use power electronics in traction and battery systems. In turn, these developments push developments in electric vehicle infrastructure development, such as DC fast chargers. Another growing development is LiDAR, which has been widely adopted as a key tool in the self-driving automotive sector. Finally, we have high voltage utility power electronics, which aims to replace traditional means of power conversion with a more flexible, efficient solution. Fig. 1.1 highlights each of these ever-growing industries, the heart of which is powered by power electronics.

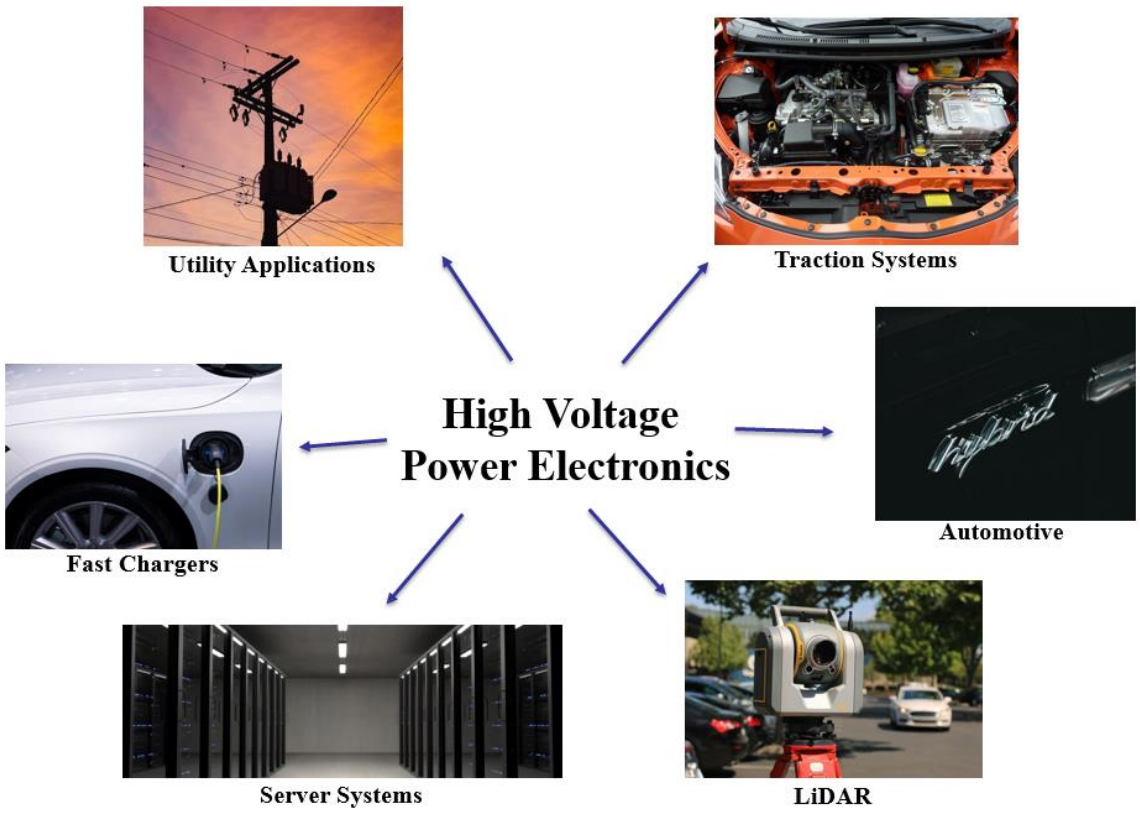

Fig. 1.1. Power electronics in developing technologies.

Wide band-gap semiconductors have played a key role in allowing for the widespread commercialization of high voltage power electronics. Wide band-gap semiconductor switches allow for smaller, faster, more efficient, and higher operating voltages than traditional silicon switches. The result has been widespread research, development, and subsequently use of high voltage power electronics in automotive electrification, electrification infrastructure, server system sectors, and utility power conversion, to name a few [1]-[7]. This development has been so widespread that analysts are estimating the potential Gallium Nitride (GaN) and Silicon Carbide (SiC) power semiconductor markets to surpass the $1 billion mark in 2021, fueled by electronics

demand and dropping prices [8]. This market consists of power MOSFETs, SiC JFETs, and SiC Schottky diodes – fundamentals of the power electronics world.

One subset of electronics design that has greatly benefitted from wide band-gap semiconductors is solid-state transformers (SST) research [9]-[12]. SSTs aim to replace traditional transformers with a carefully architected switch mode power supply (SMPS) circuit. Since SMPS circuits can be scaled in frequency, the necessary magnetics size can be massively decreased to boost power density of the system while increasing power efficiency and adding "smart" features. These features can include voltage regulation, constant unity power factor, overload protection, and many other benefits traditional wire wound transformers are unable to provide [9]-[12].

Since SSTs are composed of multiple discrete power converters modules, wide band-gap semiconductors allow for greater optimization of each module, aggregating to a large overall system improvement. An SST designed at the Future Energy Electronics Center (FEEC) at Virginia Tech supervised by Dr. Jih-Sheng Lai is shown in Fig. 1.2 (a), and its architecture shown in Fig. 1.2 (b). The SST aims to replace traditional medium voltage (MV) to low voltage (LV) utility transformers. This is a relatively new area of research, and careful considerations must be made when designing SST modules to operate at high voltage. One area of concern is the *LLC*-DCX converter used in the power stage module. A commonly overlooked portion of the power stage module, the synchronous rectifier, must be carefully designed when increasingly high voltages come into play.

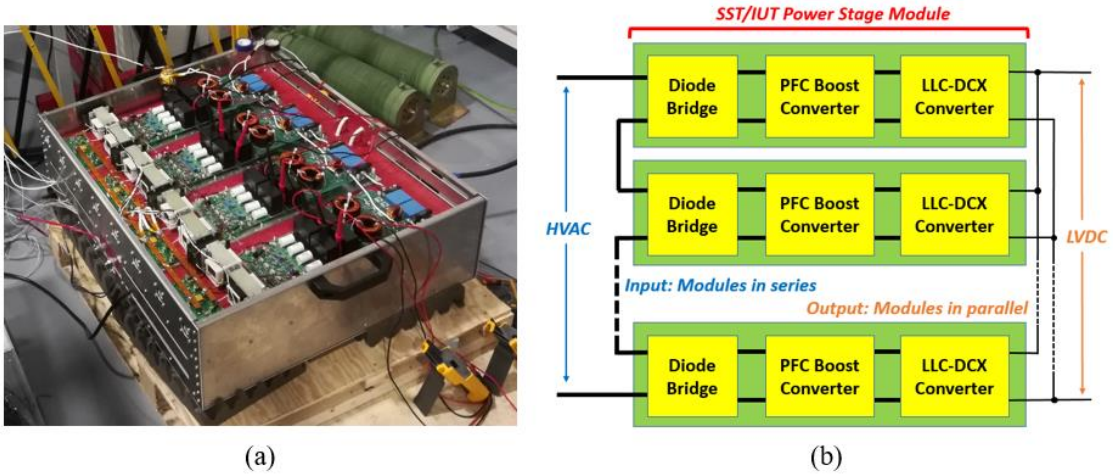

Fig 1.2. (a) FEEC's SST under test (b) FEEC SST module architecture.

1.2 Isolated DC-DC Converters

A key necessity for safety in an SST is voltage isolation; no conductive path must be present from the source to the load. This isolation must be designed into each module. Since the source of the SST is high voltage AC (HVAC), this can cause disastrous results for the downstream circuits and a critical safety issue when shorted to the dc output. This is the first key factor when selecting a power converter topology for the SST modules. Traditionally, isolation is designed at the input of the system through an isolation transformer shown in Fig. 1.3. Regulation is typically provided downstream by the AC-DC converter.

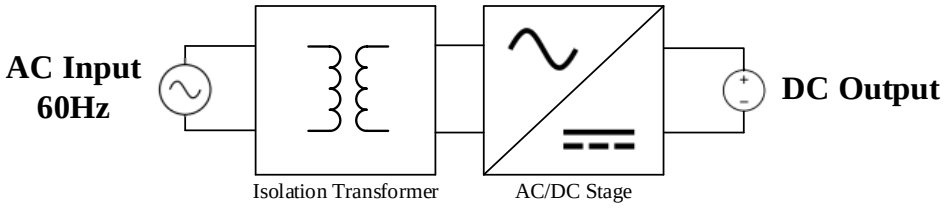

Fig 1.3. Traditional transformer isolation architecture.

Unfortunately, by placing the isolation transformer at the input, the size of the transformer is directly influenced by the input frequency. With power lines operating at low frequency, this results in a large, heavy transformer and poor power density. By moving the isolating mechanism to a portion of the module where the designer can dictate the frequency, the power density can be greatly improved. One topology that offers all of these benefits is the *LLC* resonant converter based DC-transformer circuit (*LLC*-DCX). The *LLC*-DCX is an isolated, soft switched DC-DC converter optimized at a fixed frequency. Galvanic isolation is provided by a transformer in the circuit, which can double as reactive components for the resonant tank. By setting the resonant frequency very high, the size of the transformer can be greatly reduced while still maintaining isolation benefits. The isolated module topology utilizing an *LLC*-DCX is shown below in Fig 1.4.

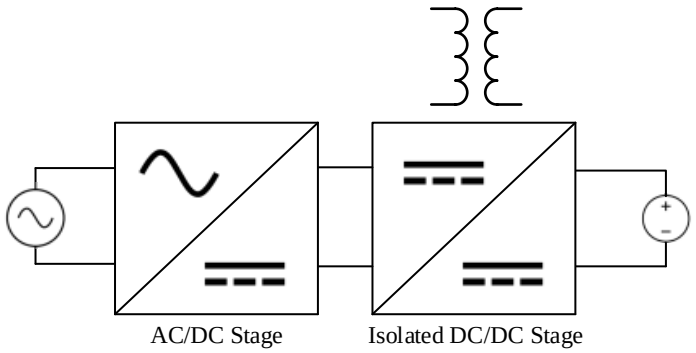

Fig 1.4. Isolation through an isolated DC/DC stage.

The *LLC*-DCX is a dc to dc converter with isolation capabilities which utilizes a resonant tank comprised of a transformer and capacitors to provide an efficient, soft-switched method of power conversion. The converter is run without feedback in open loop, therefore fixing the conversion ratio typically dictated by the transformer turns ratio. Fig. 1.5 (a) depicts the circuit of a *LLC*-DCX converter with half bridge primaries and a doubler

rectifier used in the SST modules. Fig. 1.5 (b) shows this circuit's key voltage and current waveforms during steady-state operation for one resonant cycle.

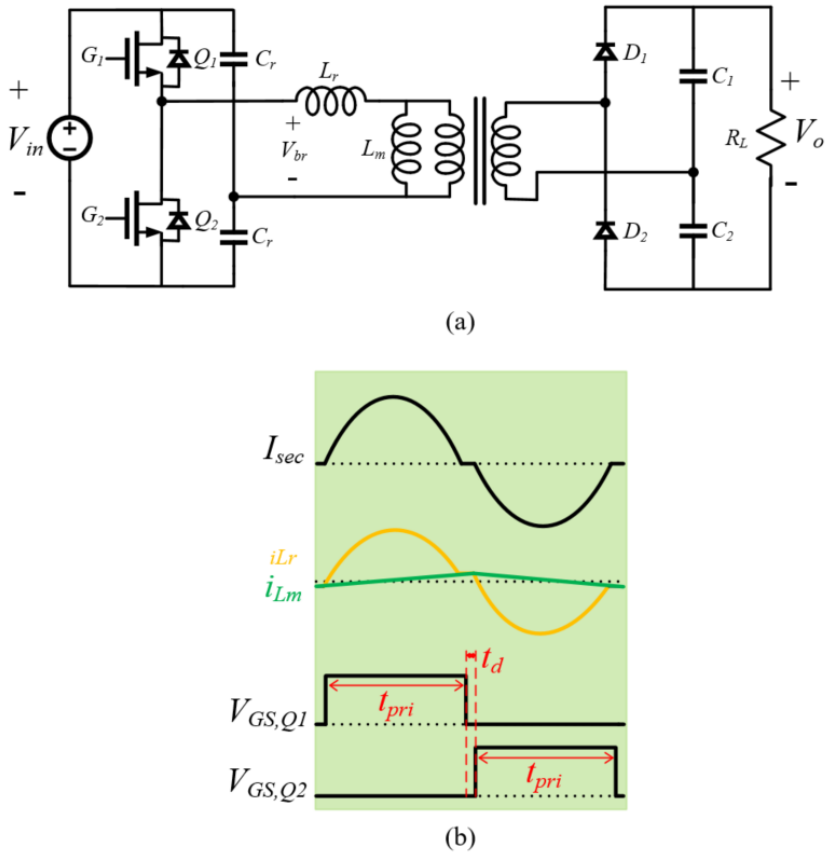

Fig 1.5. (a) *LLC* half-bridge converter and doubler rectifier (b) key circuit waveforms.

Here, the half-bridge primary side circuit excites the resonant tank comprised of L_r, L_m, and C_r. L_m and L_r are typically designed into the *LLC*'s transformer as the leakage and magnetizing inductance, respectively. The switches (Q_1, Q_2) are switched complementarily at near 50% duty cycle (t_{pri}), with some dead-time (t_d), at some switching frequency (f_s). This excitation results in a pseudo-sinusoidal current through the resonant tank, comprised of the magnetizing inductor current (i_{Lm}) and resonant inductor current (i_{Lr}) on the primary

side. The secondary side current (I_{sec}) is then sent through a rectifier to in order to output dc (V_o).

The *LLC* converter's resonant tank has two main frequencies associated with it, one higher and one lower. The higher frequency is generally referred to as the resonant frequency, or f_o, since $L_m > L_r$. L_r and C_r comprise the higher main resonant frequency, calculated by (1.2).

$$f_o = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{1.1}$$

The second resonant tank is comprised of the sum of L_m and L_r with C_r. This results in the second resonant tank frequency of (1.2).

$$f_{o2} = \frac{1}{2\pi\sqrt{(L_r+L_m)C_r}} \tag{1.2}$$

This second tank is typically unused in the design process since $L_m >> L_r$ and thus results in a much lower frequency than f_o. The main resonant tank is then excited at a certain switching frequency, which determines the power flow from input to output. For maximum efficiency the converter is operated at $f_s = f_o$. At this frequency, the converter can perform zero voltage switching (ZVS) across the primaries with a properly designed L_m value, and zero current switching (ZCS) for the secondary SR switches with synchronous rectification. To achieve soft-switching, L_m must be sized appropriately to fully discharge the primary switch's junction capacitance for ZVS. The junction capacitance, switching frequency, and dead time must be holistically analyzed for proper design of L_m.

Finally, a rectifier is employed to turn the resonant tank's ac output into dc. This is achieved here with a voltage doubler rectifier. This rectifier has two half cycles, one positive

and one negative depending on V_{sec} as shown in Fig. 1.6 (a) and (b), respectively. During the positive half cycle, the doubler capacitor C_1 is charged to the peak of $V_{sec} - V_F$, where V_F is the forward drop of rectifier diodes D_1 and D_2. During the negative half cycle, C_2 is charged to the peak of $V_{sec} - V_F$.

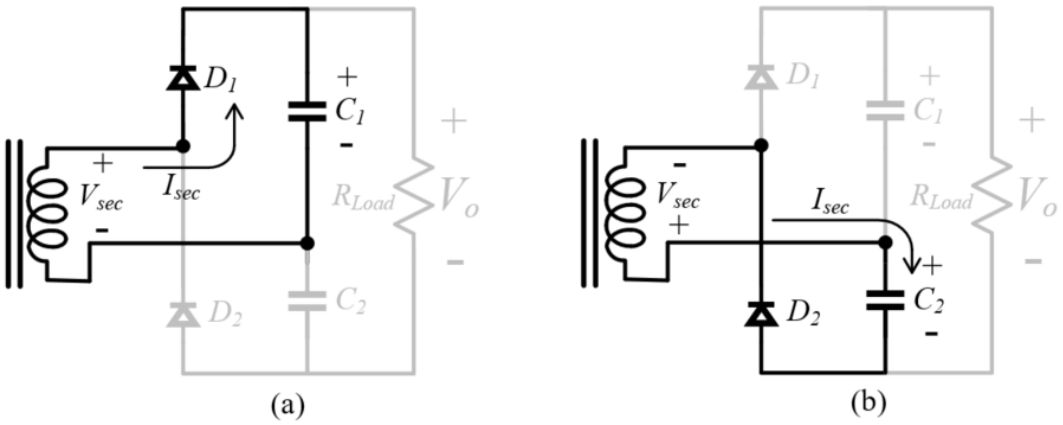

Fig 1.6. Voltage doubler operation during: (a) positive half cycle; (b) negative half cycle.

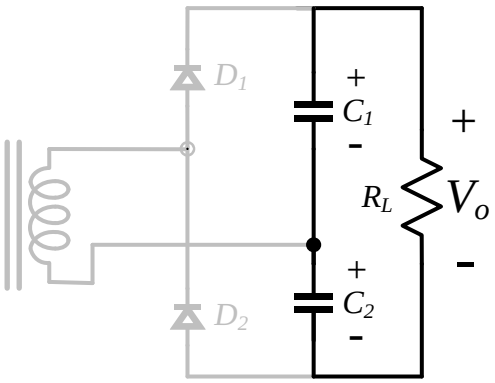

Fig 1.7. Voltage doubler rectifier output voltage.

The output voltage is the summation of the voltages across C_1 and C_2, or twice a full bridge rectifier output. Therefore, this rectifier negates the halved swing from using a half-bridge over a full-bridge primary side inverter. In conclusion, the output voltage is simply the product of the transformer turns ratio and the *LLC*'s input voltage, as shown in

(1.3). n_{pri} and n_{sec} is the number of primary and secondary transformer turns, respectively. Hence, the name of this *LLC* converter variant as a DC-transformer, or *LLC*-DCX.

$$V_o = \left(\frac{n_{pri}}{n_{sec}}\right) V_{in} \tag{1.3}$$

1.3 Synchronous Rectification Methods

Due to the resonant nature of this power converter, it needs a rectifier to convert the waveforms back to dc. Diodes traditionally used for rectification can become loss hotspots from the ohmic losses of the forward drop during diode conduction. In SST applications diode rectification loss is a significant portion of the total loss, shown in Fig. 1.8, and complicates the ability to passively cool the system when scaled in power density.

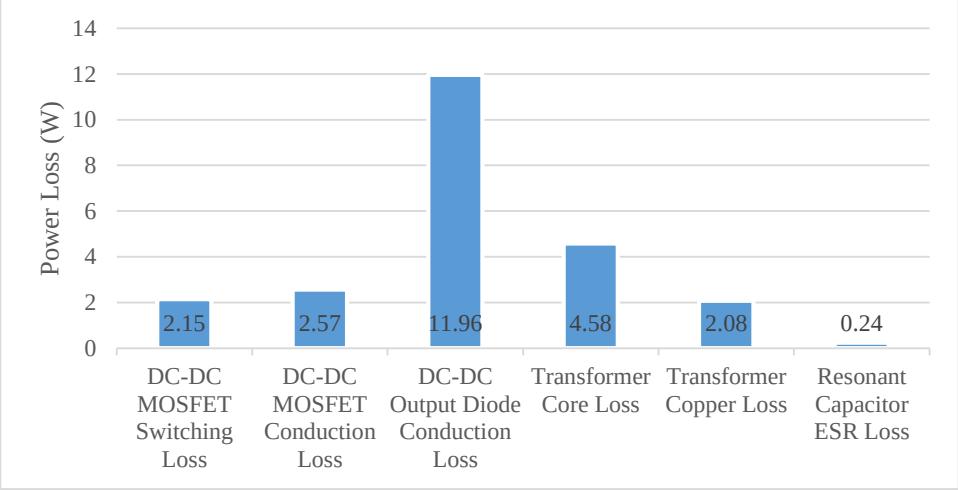

Fig 1.8. Loss breakdown of FEEC SST power stage module at 2.5kW load [13].

Synchronous rectification (SR) is a method to minimize the rectification loss incurred by replacement of rectifier diodes by a switch, typically a power MOSFET. By switching the power MOSFET synchronously with diode conduction, the current can be rectified through the switch's channel path, bypassing the diode and eliminating the

forward drop [14]-[16]. The half-bridge *LLC*-DCX with an SR voltage doubler is shown below in Fig. 1.9 (a), and key operating waveforms are depicted below in Fig. 1.9 (b).

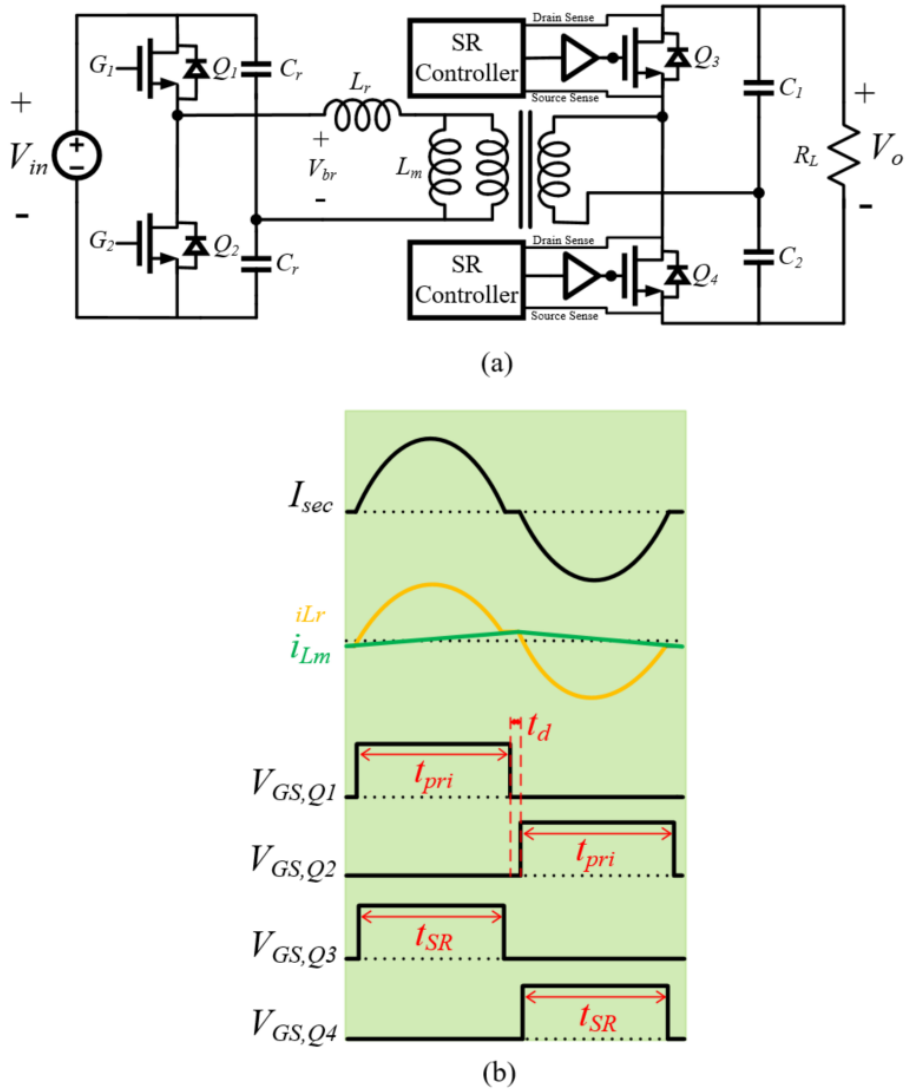

Fig 1.9. Half-bridge *LLC*-DCX with voltage doubler drain-source SR (a) circuit (b) key steady-state waveforms.

Q_3 and Q_4, the synchronous rectifier MOSFETs, are switched synchronously with diode conduction. I_{sec} is the secondary side transformer current, i_{Lr} the primary side resonant current, and i_{Lm} the primary side magnetizing current. t_{pri} represents the primary side switch (Q_1, Q_2) on-time and t_d the dead time between switches. t_{SR} represents the SR

conduction period. V_{GS} represents the gate-source voltage for each respective switch. Here, since $f_s = f_o$, the synchronous rectifier gate signals are in phase and typically windowed versions of the primary switch gate signals.

Many SR algorithms exist, such as open-loop [13], [17], current-sense [18]-[22], self-driven [23], and voltage sensed [24]-[29]. Open loop is the simplest method of SR; the secondary side SR switch signals are determined without feedback [13], [17]. In *LLC*-DCX systems, this is achieved by windowing the primary side signals to determine the SR switch signals, as shown in Fig. 1.10. While simple in implementation, the method is typically limited to systems with narrow load range and converters switching at $f_s = f_o$. Since the I_{sec} zero crossings varies across load, a fixed turn-on and turn-off moment is inaccurate across wide load ranges. Fig. 1.11 shows an aggregate simulation of the varying I_{sec} zero crossings across load for a wide load range *LLC*-DCX used in an SST. Since a power MOSFET permits bi-directional current flow, the late turn-off moment of an SR switch can result in a reversal of current conduction, reducing efficiency. Likewise, the early turn-off can result in increased parallel diode conduction time, reducing efficiency [13]. Open loop SR also becomes prohibitively expensive in high voltage systems due to voltage isolation requirements. While lower voltage systems can use off-the-shelf solutions such as signal isolators, high voltage necessitates a much more expensive solution such as fiber optics.

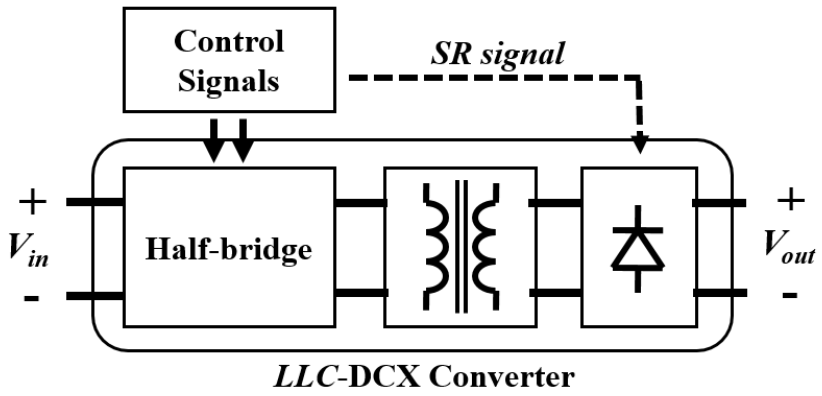

Fig 1.10. Half-bridge *LLC*-DCX with open-loop SR.

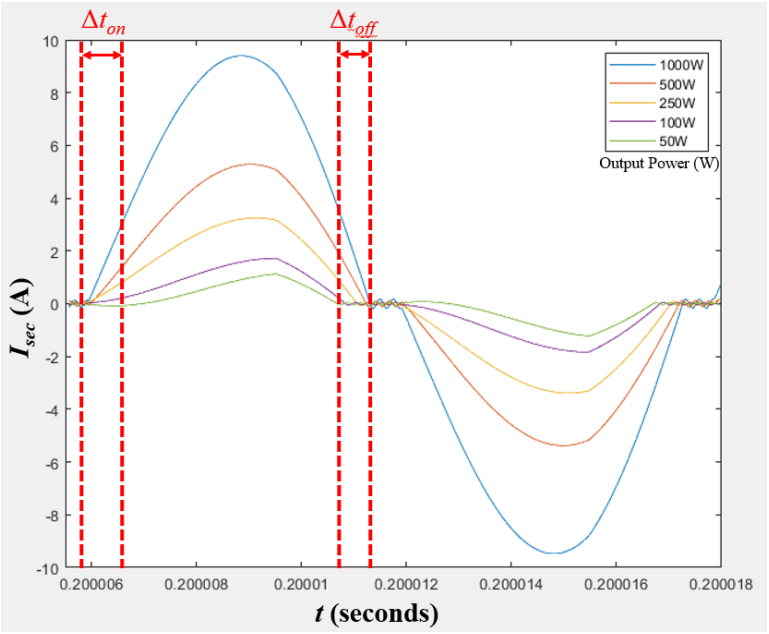

Fig 1.11. Varying I_{sec} zero crossing moments across output power.

Closed loop SR is most desirable and can be group into three main categories: (1) current-sensed; (2) self-driven; (3) voltage sensed. Current sensed methods utilize a current sensor to determine the correct SR signals [18]-[22], shown in Fig. 1.12. Since this method directly senses the moment the SR switch needs to turn on, it is extremely accurate.

However, the physical current sensor, cost of auxiliary components, and complexity of post-processing hardware make it cost prohibitive in most applications.

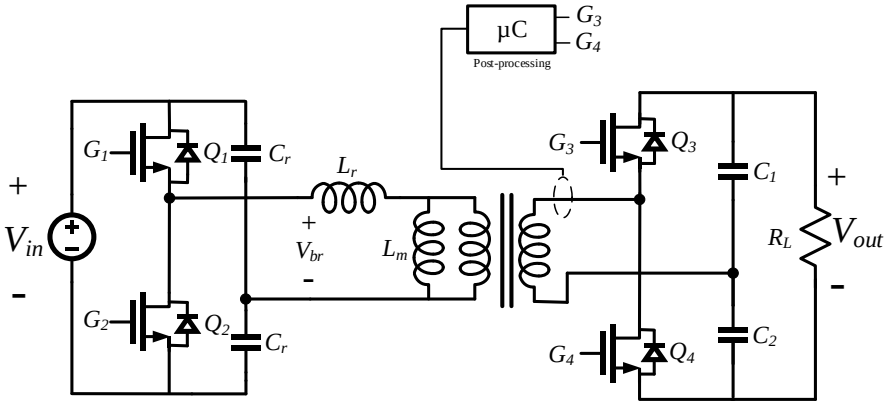

Fig 1.12. Half-bridge *LLC*-DCX with current-sense SR.

Self-driven SR systems are self-powered, typically through the transformer by an auxiliary winding. While simple, this method results in non-ideal gate drive signals [23]. Since no actual gate driving is used, the driving characteristics result in high loss and is difficult to adapt for high voltage.

Finally, we have voltage-sensed SR - the most mature method of SR available today. The two most common voltage-sensed SR algorithms are the volt-second method and drain-source. The volt-second method samples a switch's output and drain-source voltages to calculate the switching moments [30]. Since no primary side feedback is necessary, voltage isolation is not a concern. However, the turn-off algorithm for this method does not allow for voltage limiting or blocking, since the full voltage needs to be sampled to accurately predict turn-off. Therefore, this method cannot be adapted for high voltage operation due to inherent IC voltage limits.

This leaves drain-source SR, the other voltage sensed SR method. This method solely uses the drain-source voltage to decide the SR switching moments [31]-[37]. Therefore, like volt-second, voltage isolation is not a concern for this method. While the turn-on moment is very accurate, the turn-off accuracy is dependent on the signal-to-noise ratio (SNR) of the sensed drain-source signal. Since the drain-source algorithm determines the SR switch state when the drain-source voltage is low, high voltage can be blocked for use in high voltage converters. One drain-source SR-based method proposed in research which can possibly retrofitted for high voltage use was proposed in [38]. While not intended for high voltage operation, the blocking diode used in the paper can be replaced to achieve high voltage blocking. However, this method is not a fully closed-loop method – it operates with open-loop turn-on. Furthermore, this method requires many additional components for external compensation of the blocking diode, and the method has only been tested at 12V [38]. Since a diode and pull-up resistor is used as the blocking mechanism, a diode drop lies in the sensing loop and necessitates external compensation. Here, this is performed with an external voltage reference, exacerbating complexity and cost. An improved solution, an external self-biasing high voltage clamp in the form of a power MOSFET, can block high voltages as necessary but permit sensing at critical lower voltages. Because the key determining moments happen near or under zero volts, the proposed solution would preserve normal SR controller operation. This method is explored, analyzed, and tested in Section 2.

However, high voltage blocking only addresses one of the issues with drain-source SR. Two other issues exist: a light load oscillation issue, and sensing accuracy. SR was originally designed for lower voltage, high current systems. With high voltage systems,

light load conditions can lower the drain-source SNR to a point where a false duty cycle can result in current oscillations. Next, drain-source SR is susceptible to early SR switch turn-off from parasitic inductance present inside the sensing loop. High voltage blocking, light load oscillations, and sensing accuracy will be addressed in Sections 2, 3, and 4 respectively. Table 1.1 compares current SR algorithms across common metrics. Next, Table 1.2 compares the proposed improved HV drain-source SR method across the same metrics.

TABLE 1.1.
COMPARISON OF CURRENT SR METHODS.

SR Method	Traditional Drain-Source	Closed-loop turn-off w/ diode clamp	Current Sense (CT, sensor)	Open-Loop
Sensing Method	Voltage	Voltage	Current	None
Verified Experimental Voltage	230V (datasheet)	12V	380V	400V
# of Components	**Low**	**High**	**High**	**High**
Accuracy	**Medium** -Parasitic inductance issue	**Medium** -Inaccurate turn-on -Parasitic inductance issue	**High** -Very precise	**Low** -Inaccurate across load
Cost	**Low** -Requires few components	**High** -Requires expensive high speed comparators, precision voltage references	**High** -Requires high speed comparators, ADCs/DSPs	**High** -Requires expensive isolation methods (ie. fiber optics)
Complexity	**Low** -Closed-loop tuning by IC	**High** -Diode blocking is manually compensated	**Medium** -Current converted to voltage to sense	**Medium** -Additional external circuitry necessary for isolated gating

TABLE 1.2.
COMPARISON OF SR METHODS WITH PROPOSED IMPROVED DRAIN-SOURCE SR METHOD.

SR Method	Proposed: Drain-Source w/ Self-Biasing Clamp	Closed-loop turn-off w/ diode clamp	Current Sense (CT, sensor)	Open-Loop
Sensing Method	Voltage	Voltage	Current	None
Verified Experimental Voltage	kV+	12V	380V	400V
# of Components	**Low**	**High**	**High**	**High**
Accuracy	**High** -Parasitic effects mitigated with SPS or MLGD	**Medium** -Inaccurate turn-on -Parasitic inductance issue	**High** -Very precise	**Low** -Inaccurate across load
Cost	**Low** -Commercial ICs with minimal external components	**High** -Requires expensive high speed comparators, precision voltage references	**High** -Requires high speed comparators, ADCs/DSPs	**High** -Requires expensive isolation methods (ie. fiber optics)
Complexity	**Low** -Automatic tuning by IC	**High** -Diode blocking is manually compensated	**Medium** -Current converted to voltage to sense	**Medium** -Additional external circuitry necessary for isolated gating

1.4 Drain-Source SR

While a plethora of other SR methods are around in addition to the methods listed in Section 1.3, most methods are generally designed for lower voltage, high current rectifiers and are not worthwhile or practical to adapt for high voltage. However, drain-source SR is the most viable method for high voltage adaptation. However, commercially available drain-source ICs have low sensing limits, generally less than 200V. A list of the highest sensing rated drain-source SR controllers are listed below in Table 1.3 [30]-[37].

TABLE 1.3.
COMMERCIALLY AVAILABLE SR CONTROLLERS AND V_{DS} SENSING LIMITS

SR Controller	Rated V_{DS} Sensing Limit
Texas Instruments UCC24612	230V
International Rectifier IR1167	200V
OnSemi NCP4303/NCP4304	200V
Linear Technology LT8309	150V
Texas Instruments UCC24610	50V

These SR controllers sense the voltage on the drain to source terminals (V_{DS}) of the SR switch. The sequence of detected voltages identifies the state of the SR switch. The SR switch starts in an off state, with the sole conduction path through the body diode, shown in Fig. 1.13 (b). Once current flow begins, a negative diode drop occurs across V_{DS}, as shown in (1.4) and Fig. 1.13 (a). When this forward drop is detected, SR switch is turned on by the controller. This bypasses the diode, and eliminates the forward drop. The resulting voltage across the drain-source can be calculated by (1.5), where I_{DS} is dependent on I_{sec} in a *LLC*-DCX circuit. Ideally, this reduces the diode conduction loss shown in (1.6) to the much lower SR switch conduction loss, (1.7).

$$V_{DS} = -V_F \tag{1.4}$$

$$V_{DS} = -I_{DS} * R_{DS,on} \tag{1.5}$$

$$P_{SR\_loss} = R_{DS,on}\left(0.707 * I_{peak}\right)^2 \tag{1.6}$$

$$P_{diode\_loss} = V_F(0.637 * I_{peak}) \tag{1.7}$$

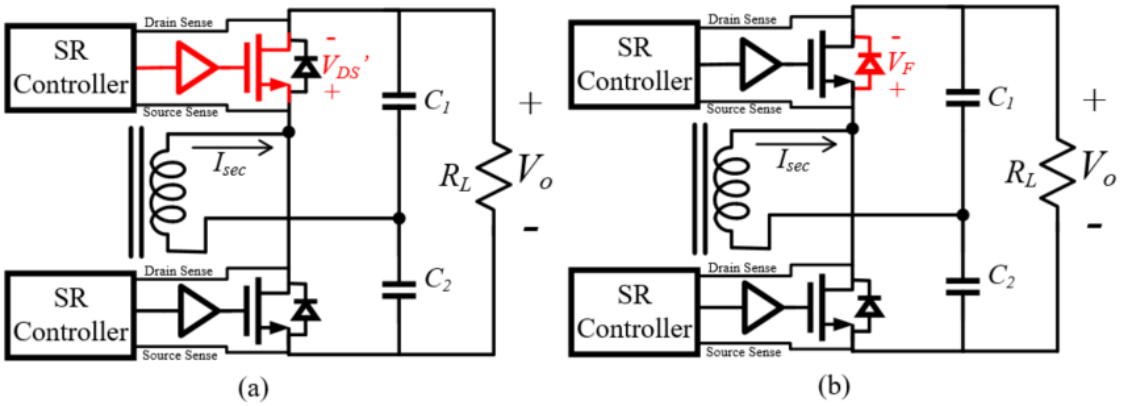

Fig. 1.13. Rectification path through the (a) body diode and (b) switch channel.

As I_{sec} approaches the zero crossing moment, the sensed V_{DS} voltage also nears zero as (1.5) shows. Once the voltage drops to a designated turn-off voltage, the controller turns off the SR switch. The specific turn-off voltage is dictated by the SR controller manufacturer, and varies between each controller. So far, the key transition moments all occur at or near zero voltage. Therefore, high voltages can be blocked while retaining full SR controller function.

Chapter 2

High Voltage Blocking

2.1 General Description

The drain-source controller's key decisive moments for turn-on and turn-off happen at very low voltages: (1) diode drop detection, $-V_F$, for turn-on; (2) near or at-zero voltage for turn-off. Therefore, full SR controller function is preserved when the greater of the two voltages are blocked. General high voltage blocking can be achieved with a diode, with a channel in parallel to bypass the diode. This description can be realized with a power MOSFET, and its body diode is used to block high voltage and the channel selectively turned on to bypass the diode. Fig. 2.1 shows an N-channel blocking power MOSFET in the drain-source SR sensing circuitry for both the high and low side SR switches.

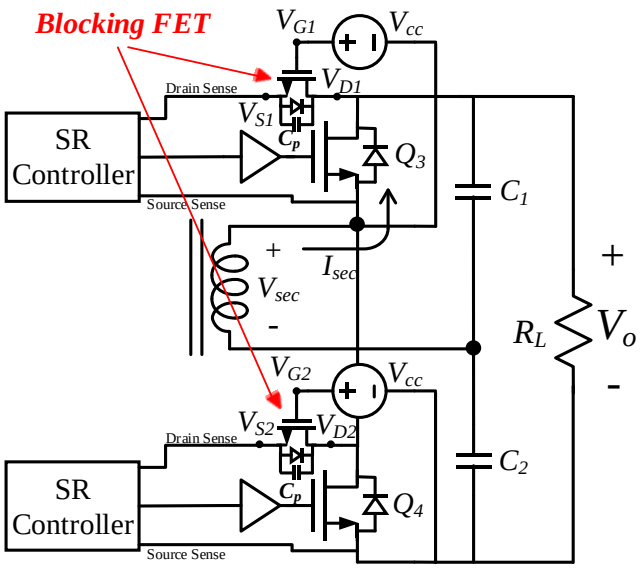

Fig. 2.1 Blocking power MOSFET placement in the drain-source sense path.

V_D, V_G, and V_S represent the drain, gate, and source voltage of each MOSFET, respectively. C_p represents the parasitic capacitance between the drain and source of the blocking MOSFET. V_{cc} is the voltage from the gate of the blocking MOSFET (abbreviated onwards as "blocking FET") relative to the source of its respective SR switch.

The body diode acts as the high voltage blocking, isolating mechanism until the blocking FET is turned on, which then allows the SR controller to detect the turn-on and turn-off moments. In order for the blocking FET to operate properly, the gate must be properly biased. This is achieved by a fixed voltage V_{cc} applied to the gate of the blocking FET with respect to the source of the SR switch (Q_3, Q_4). With the V_G is properly biased, the blocking FET becomes an automatic voltage clamp for the SR controller while retaining full controller function. This is shown next, where the blocking FET operation is analyzed in the following section.

2.2 Operating Principles of the Self-Biased Blocking MOSFET

To allow for the blocking FET to automatically self bias, the correct voltage needs to be applied across the V_{GS}, gate-source terminals to enable and disable the channel. At first glance, with the FET channel off, the source terminals (V_{S1}, V_{S2}) seems isolated and it appears the blocking FET will never turn on since V_{GS} does not rise above the threshold voltage, V_t. However, there is a coupling mechanism present from drain to source of the blocking FET – the parasitic capacitance, C_p, as shown in Fig. 2.1. The SR controller can also be modeled as a parasitic capacitor C_{SR} paralleled with a resistance, R_{SR}. Granted, since the controller input is very high impedance, R_{SR} is neglected [31]-[32]. The voltage on the

transformer's secondary terminals is an alternating current square wave in an *LLC* converter. Therefore, this induces a current through the C_p and C_{SR} as it is charged and discharged, which causes the voltage at V_{S2} to also rise and drop. This varying V_{S2} is the key in allowing the blocking FET to self-bias. The induced current across the varying SR switch drain-source voltage forces V_{S2} to actively follow V_{D2}, which naturally turns the blocking FET on and off. While off, the body diode is used as the blocking mechanism to limit voltage across the SR controller's sense pins. The blocking FET and gate voltage must be carefully selected based on the SR controller C_p.

Therefore, C_p and C_{SR} form a capacitor divider, and the voltage induced across the SR controller and blocking FET is a function of: (1) the capacitance values; (2) the initial voltage charge condition across C_{SR}. This initial voltage condition, $V_{SR,init}$, is a byproduct of the gate threshold voltage V_t of the blocking FET and gate bias voltage V_{cc}.

The critical issue for safe operation is the peak voltage across the drain-source sense pin. It is critical that the voltage here does not exceed the absolute maximum limit of the controller. As a result of the SR switch being in triode mode when the blocking FET's source pin drops below V_{cc}-V_t, the voltage at V_{S2} is directly linked to V_{cc} for this portion of the cycle, and V_t is the datasheet gate threshold voltage of the blocking FET. Therefore, the initial voltage condition across C_{SR} has significant influence to the peak induced voltage seen across the SR controller sense pin.

Fig. 2.2 and 2.3 depict one SR cycle (one-half resonant cycle) with a blocking FET and additional diode blocking solution. Between t_1 to t_3 the parallel diode conducts, which triggers the initial SR switch turn-on. From t_1 to t_2, SR controller is isolated and the blocking FET off since $V_{DS} > V_{cc}$-V_t. Between t_2 to t_3, the blocking FET is now on, which

allows the controller to directly sense the SR switch drain-source voltage. t_4 represents the moment the controller switches the SR switch off, when V_{DS} hits the turn-off voltage of the SR controller. t_4 to t_6 depicts the parallel diode conduction period, a result of an sensing parasitics. t_5 signifies the point where the blocking FET turns off in between, once again providing the SR controller isolation from high voltages. Between t_5 to t_6, V_{DS} rises and I_{sec} approaches zero, signaling conclusion of this SR cycle.

The blocking FET operates in one of two primary states: (1) with the channel conducting; (2) with the channel not conducting, shown in Fig. 2.4 (a) and (b), respectively. The off-on transition occurs at t_2 in Fig. 2.2 and 2.3 when V_{DS} drops. The on-off transition occurs at t_5 when V_{DS} rises. At periods before t_2 and after t_5 onwards, the blocking FET is off and the controller is isolated. From t_2 to t_5, the blocking FET is on, allowing sensing of the SR switch. This analysis shows that full SR controller function is preserved, since the critical V_{DS} sensing moments occur when the blocking FET is on.

Next, we look at the equivalent circuits with the blocking FET in each of the aforementioned states. With the blocking FET turned on, C_p is shorted away by the channel. The equivalent corresponding circuit is shown in Fig 2.5 (a). Some finite channel resistance from the operating the blocking FET within the linear region exists, but this is variable due to the varying gate-source voltage due to varying V_{S2}. This is left out of the following analysis from limited impact on blocking FET operation and voltage sensed by the SR controller. Since the blocking FET channel is coupling the drain and source together, an increase in V_{D2} can turn off the channel. This increase is shown from t_4 to t_5 in Fig. 2.3 and 2.3, and induces a bias current I_b in Fig. 2.4 (b). This current charges C_{SR} and causes the

blocking FET to automatically turn off by itself. The self turn-off occurs once (2.1) is satisfied, where V_t is the blocking FET threshold voltage, V_{cc} the blocking FET's bias voltage set by the designer with reference to the SR switch's source pin, and V_{S2} the source voltage of the blocking FET.

$$V_{S2} > V_{cc} - V_t \tag{2.1}$$

Based on (5), we see that the voltage across C_{SR} will rise to V_{cc}-V_t before the channel turns off. Once V_{S2} reaches V_{cc}-V_t, the SR switch V_{DS} is distributed across C_p and C_{SR} based on a capacitive divider. The resulting equivalent circuit with the blocking FET on and off is shown in Fig. 2.5 (a) and (b), respectively, with the initial C_{SR} voltage denoted as $V_{SR,init}$. Therefore, the C_{SR} to C_p ratio will dictate the final voltage across C_{SR} from this point forward. Between t_1 and t_3, V_{DS} falls which causes a negative I_b and which discharges C_{SR}. When V_{S2} drops under V_{cc}-V_t, the blocking FET is then turned back on. This cyclically repeats for the following SR cycles. In conclusion, the proposed blocking solution and operation is completely hands-off, passive, and necessitates no outside control to operate once properly designed. While the blocking FET itself is an adequate means of voltage blocking for most high voltage applications, additional voltage limiting methods in the form of external C_{SR} and a diode clamp can be added to further limit the voltage, which is discussed in Section 2.2.

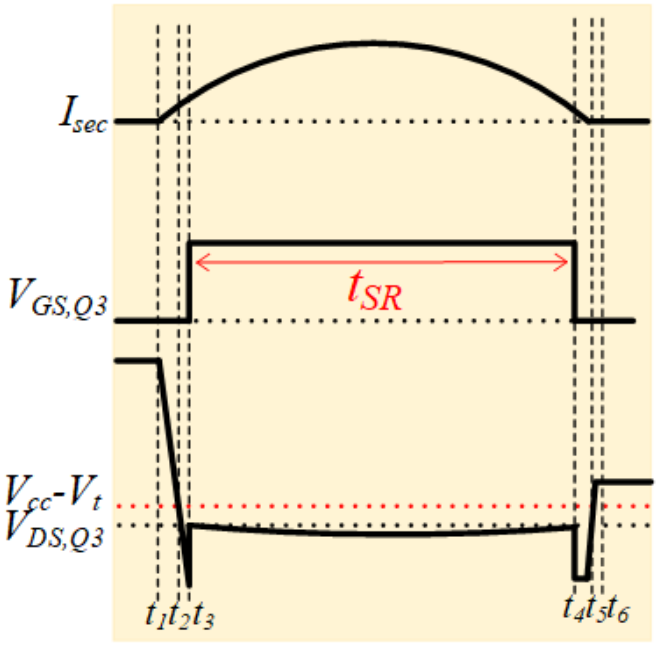

Fig. 2.2. Key secondary-side current and voltage waveforms during synchronous rectification.

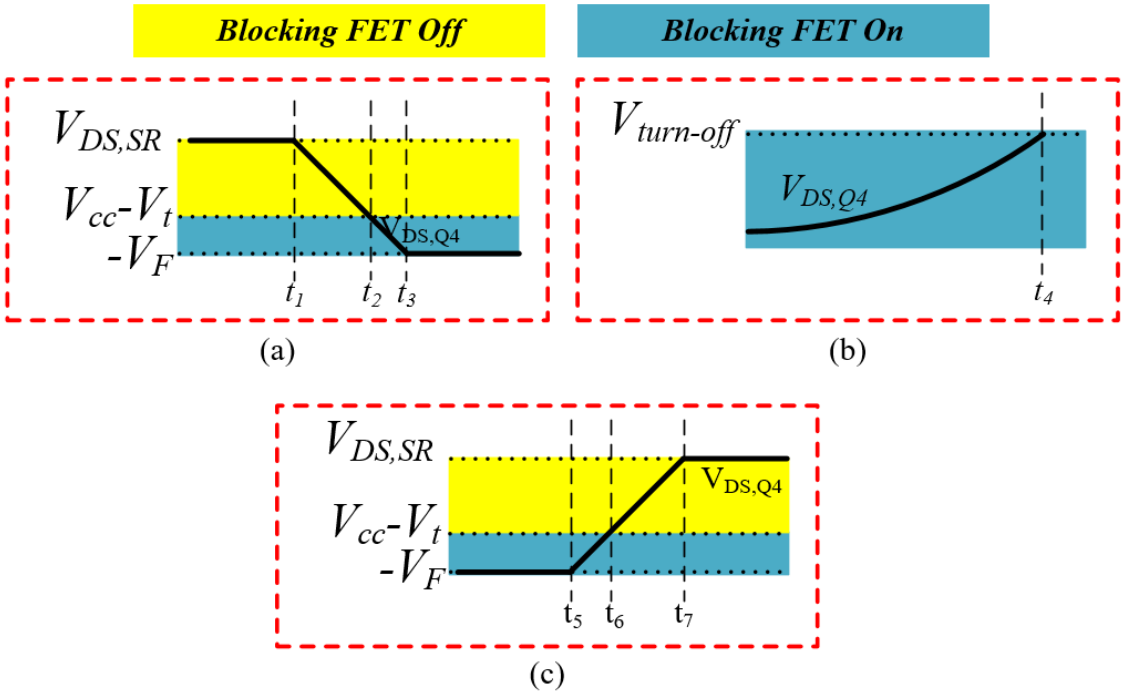

Fig. 2.3. Closeup of key blocking FET operating states across V_{DS}.

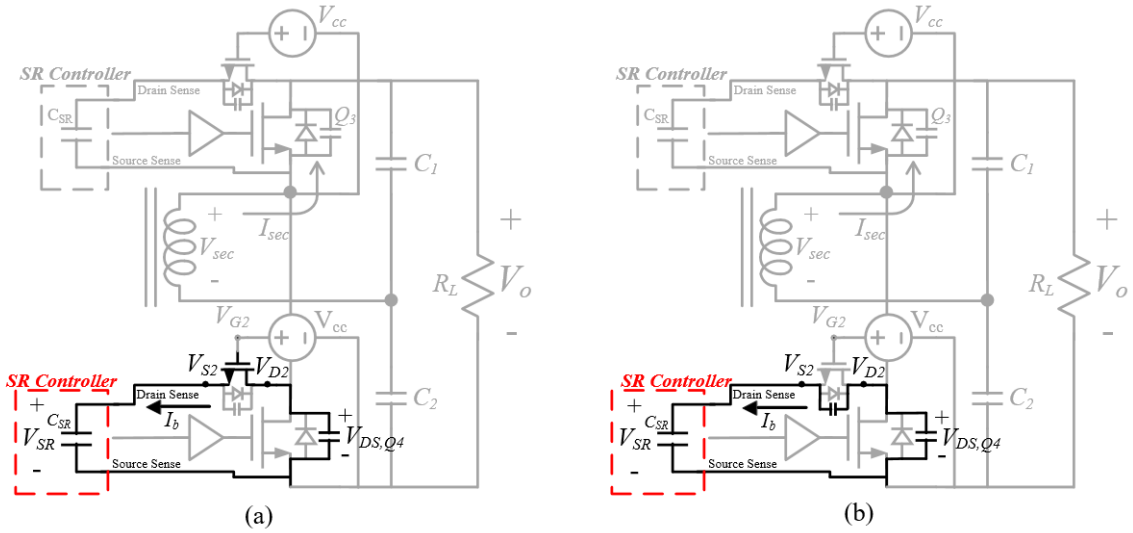

Fig. 2.4. Capacitor divider circuit with the blocking FET: (a) on; (b) off.

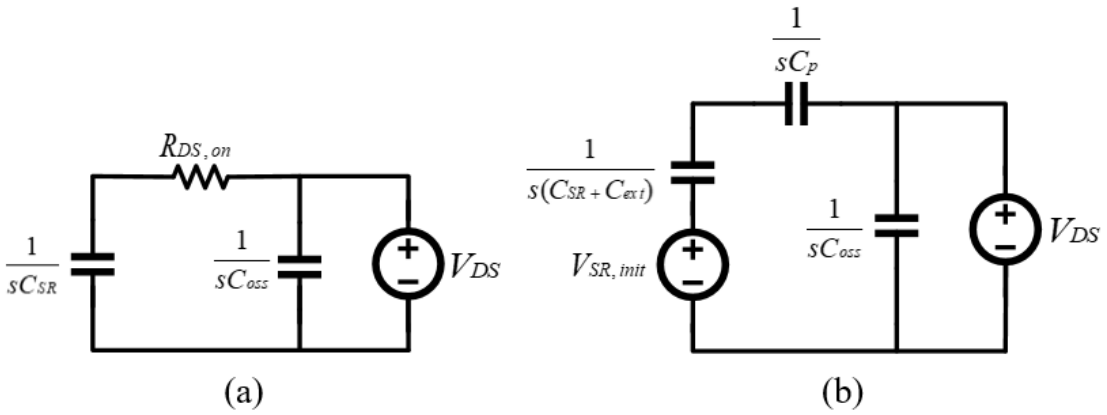

Fig. 2.5. Equivalent circuits of SR in the s-domain with the blocking FET: (a) on; (b) off.

2.3 Design for Safe High Voltage Operating Conditions

In this section, we will further analyze the elements that directly influence the peak voltage induced across C_{SR}. Limiting the voltage across C_{SR} is key in preventing overvoltage damage to the SR controller. All independent variables which impact the sensed voltage are presented here, including design equations developed. Additional limiting methods that piggyback onto the blocking FET are also proposed and analyzed.

Design side considerations for selecting the gate bias voltage, blocking FET, external diode clamps, and external parallel SR controller capacitance are all discussed below.

When the blocking FET is off, the capacitive divider formed with C_p, the blocking FET capacitor, and C_{SR}, the SR controller's internal parasitic capacitor, dictates the voltage across C_{SR}. Using reactance, the voltage across C_{SR} is expressed in (2.2). Reactance is frequency dependent, but our application is an *LLC*-DCX which operates at fixed frequency.

$$V_{SR} = V_{DS,pk}\left(\frac{X_{CSR} + X_{Cext}}{X_{CSR} + X_{Cext} + X_{Cp}}\right) \tag{2.2}$$

X_{CSR}, X_{Cext}, and X_{Cp} represent the reactance of C_{SR}, C_{ext}, and C_p respectively. C_{ext} is additional external capacitance in parallel with the SR controller sense pins, which can be used to further lower the sensed voltage. $V_{DS,pk}$ is the peak drain-source voltage sensed between the SR switches Q_3 and Q_4. Granted, the equation fails to compensate for the initial voltage condition of C_{SR}. This initial condition is determined through the smallest V_{S2} value where (2.1) is satisfied. By taking $V_{SR,\text{init}}$, the initial voltage condition of C_{SR}, into consideration (2.2) is expanded into (2.3).

$$V_{SR} = (V_{DS,pk} - V_{SR,init}) \times \left(\frac{X_{Cext} + X_{CSR}}{X_{Cext} + X_{CSR} + X_{Cp}}\right) + V_{SR,init} \tag{2.3}$$

Analysis of (2.3) shows that a lower C_p is desirable to reduce the sensed voltage at the SR controller. Therefore, the factors in selection of a blocking FET can be summarized into the two key metrics: (1) the V_{DS} rating; (2) the C_{oss} value. The first metric, the V_{DS} rating, is self-explanatory – the blocking FET must withstand the high voltages it is supposed to block. The second metric, the C_{oss}, while it typically varies with voltage, it

plateaus under higher voltages using energy related measurement methods. However, since the operating voltage is far past this C_{oss} plateau point, an accurate approximation of C_{oss} is achievable. Finally, it must be remembered that the voltage for gate bias should be minimized. While using an existing nearby voltage source is simplest in application, a bias voltage much greater than the blocking FET's threshold voltage will also increase the peak voltage sensed by the SR controller. Therefore, the gate bias voltage should be marginally greater than the blocking FET's worst-case absolute max V_t.

As previously mentioned, external capacitors placed in parallel with the SR controller sense terminals could be used to further drop the maximum voltage seen across the controller. Since the voltage gain is a function of C_{SR}, external C_{SR} can be added for a further reduction in voltage. However, this additional capacitance can cause a delay to propagate on signal sensing. Because the blocking FET operates within the linear region, there exists a finite channel resistance with the FET on, as noted in Fig. 2.5 (a) as $R_{DS,on}$. This channel resistance causes an RC time constant delay when discharging C_{SR}.

Nevertheless, a minute amount of C_{ext} (in the pico-farads) can still be useful to mimic the effects of a low pass filter for noise, which will have negligible effects on signal delay. In the majority of cases, a proper blocking FET setup will be adequate for high voltage blocking without any other modifications, such as using external additional capacitors. Granted in very high voltage conditions, additional diode clamping can be necessary. A possible alternative method to reducing C_{SR} voltage with C_{ext} is with a diode clamp from the drain-sense to the blocking FET gate. This resulting circuit is shown in Fig. 2.6, where D_1 and D_2 are the clamping diodes. Next, the equivalent circuit from using clamping diodes is shown in Fig. 2.7.

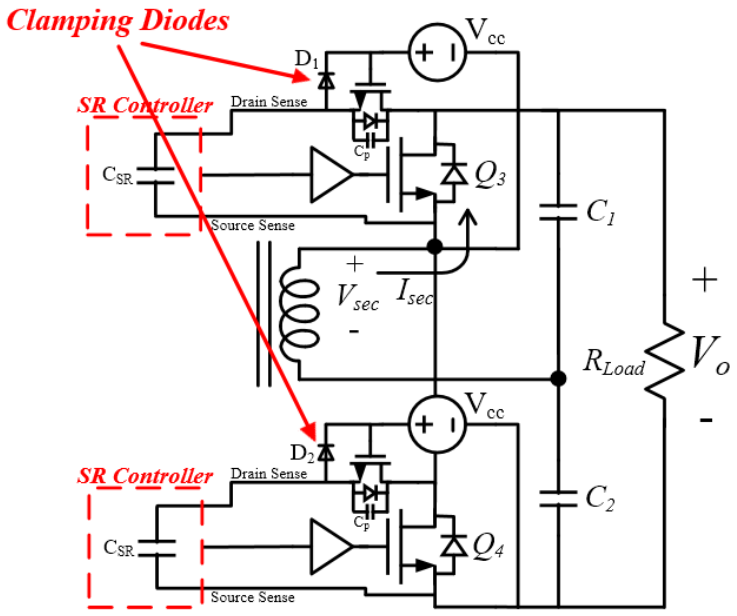

Fig. 2.6. Drain-source voltage diode clamps on voltage doubler rectifier.

The diodes clamp the drain-source sense voltage to V_{cc}. Therefore, V_{S2} will increase up to V_{cc}-V_t due to current I_2 in Fig. 2.7 and by (2.1) under channel conduction. During this point, I_1 is zero. The I_2 current will charge V_{S2} to V_{cc}, where current will flow through this bypass diode to V_{cc}, shown as I_1. Therefore, the maximum voltage sensed by the SR controller is only V_{cc}. The voltage across C_p can then be calculated by (2.4).

$$V_{Cp} = V_{DS,pk} - V_{cc} \tag{2.4}$$

In conclusion, the use of an additional clamping diode with the blocking FET, forces the majority of the voltage across the blocking FET.

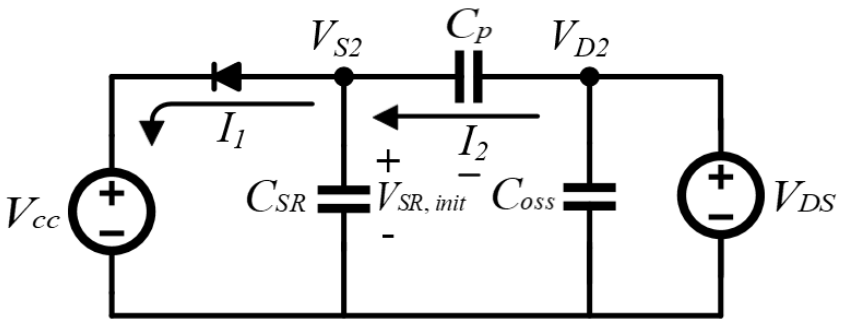

Fig. 2.7. Equivalent circuit of SR utilizing clamping diodes.

Two separate *LLC* converters were used to verify the proposed blocking FET voltage clamp: (1) a 84 kHz converter; (2) a 300 kHz converter. This was to check if any frequency dependency were present in the blocking FET design. Two SR controllers are used: (1) Texas Instruments UCC24610; (2) ON Semi NCP4303. The TI controller utilizes drain-source voltage sensing. However, the ON Semi controller injects current through the drain pin for voltage sensing. Here, both types of architecture are validated for full high voltage operation well in excess of absolute maximum ratings. The SR board built for verification on the 84 kHz converter is shown below in Fig. 2.8. This was used for testing both controllers on a 84 kHz, 2.5-*kW LLC*-DCX module, pictured below in Fig. 2.9. This module features an active front-end (AFE), which is bypassed by feeding DC power directly to the *LLC*-DCX input. The power stage parameters are noted below in Table 2.1. The SR design mimics the aforementioned doubler, with blocking FETs used for both SR controllers. The specific SR parameters are listed in Table 2.2.

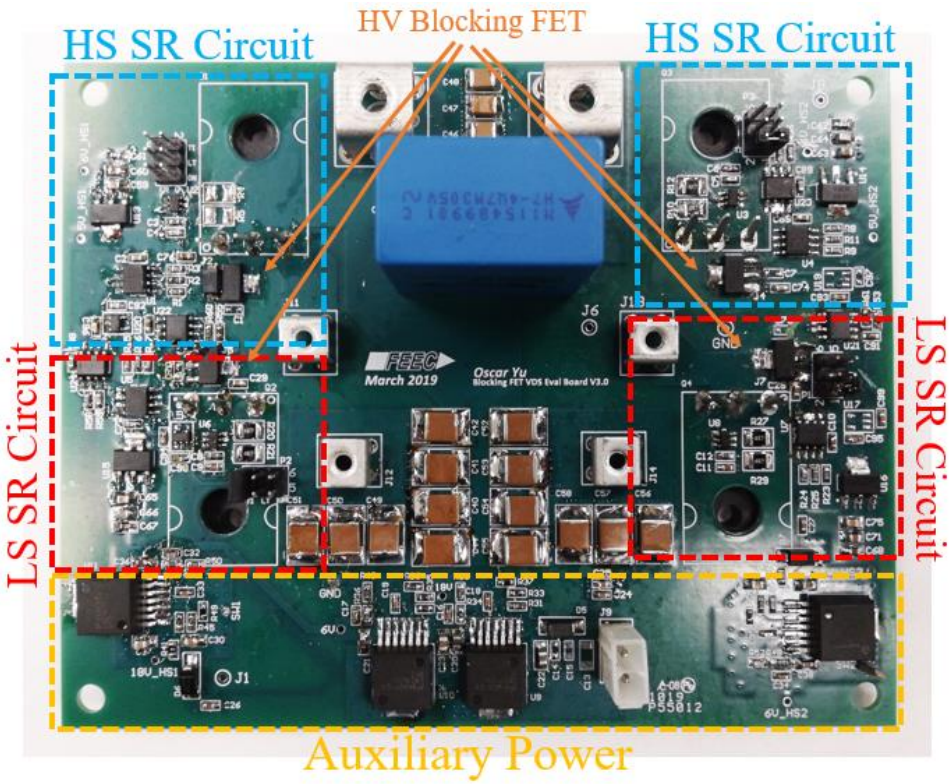

Fig. 2.8. Custom voltage doubler SR board with blocking FETs.

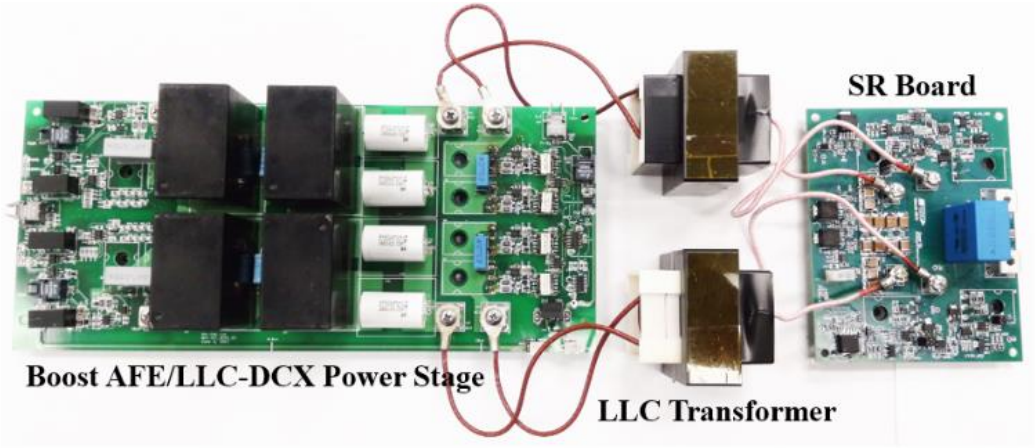

Fig. 2.9. *LLC*-DCX converter with primary power stage board (left), transformer (center), custom synchronous rectifier board (right).

TABLE 2.1
LLC-DCX MODULE POWER STAGE PARAMETERS

Component	Parameter
Resonant Inductance (L_r)	11.2 μH
Resonant Capacitance (C_r)	0.30 μH
Magnetizing Inductance (L_m)	760 μH
XFMR Turn Ratio (n_{pri}:n_{sec})	21:12
Switching Frequency (f_s)	84 kHz
Primary Switch	C2M0080120D

TABLE 2.2.
HV SR BOARD PARAMETERS

Component	Parameter
Gate Drive Voltage	18-V
Gate Driver	TI UCC27531
Synchronous Rectifier MOSFET	Rohm SCT3017
Blocking MOSFET	BSP300
Blocking MOSFET Gate Bias Voltage	5-V
Gate Resistance (on,off)	4.7 Ω
Maximum V_{DS} Voltage	348-V
C_{out}	6.12 μF

To verify equation (2.3), the voltages across both C_p and C_{SR} are attained with and without the external C_{SR}. The resulting systems of linear equations can be solved for C_p and C_{SR}, the two unknowns since C_{ext} is a known value. V_{SR} can then be analytically calculated using (2.3) across different C_{ext} values and blocking FET gate bias voltages. This is then graphed for the each controller, as depicted in Fig. 2.10 and 2.11. The controller's internal C_{SR} can also be calculated: 1.073 *nF* for the TI UCC24610 controller, 960 *pF* for the On Semi NCP4303 controller. C_p was calculated as 36 *pF* during testing of both SR controllers, similar to the datasheet C_{oss} specification of the BSP300 blocking FET [39]. The small deltas between calculation and testing is attributed to using the datasheet's averaged gate threshold value in calculation, which varies by FET. Furthermore, there is a parasitic 6 *pF* internal

capacitance in ADP305 and ADP300 differential probes used during measurements [40]. This parasitic would serve to further increase the delta between testing and calculation.

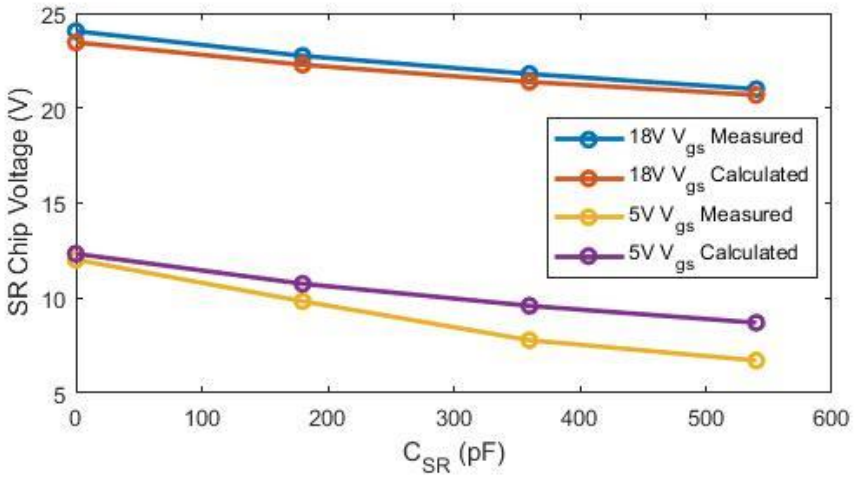

Fig. 2.10. UCC24610 SR controller measured vs. calculated sensed voltage.

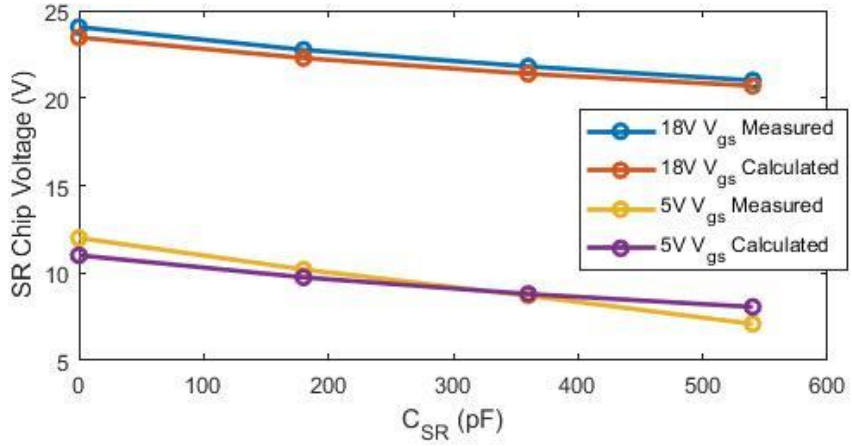

Fig. 2.11. NCP4303 SR controller measured vs. calculated sensed voltage.

As depicted in Fig. 2.10 and 2.11, the actual and calculated values match very well. With the addition of this blocking FET, both controllers were able to be safely operated at drain-source voltages close to 350-*V*, without any additional external clamping or C_{ext}. The time domain I_{sec}, V_{DS}, gate, and V_{SR} waveforms of the TI UCC24610 controller are shown below during a test in Fig. 2.12. I_{sec} is the secondary side transformer current, V_{SR} the

sensed SR controller drain-source voltage, $V_{DS,SR}$ the actual drain-source voltage of the SR switch, and $V_{GS,SR}$ the gate-source voltage of the SR switch. At 350-*V*, the Texas Instruments controller is operating at almost 7x the datasheet limit of the controller, and nearly 2x of the On Semi controller's limit [31]-[33].

With a 5-*V* blocking FET gate bias voltage and no C_{ext}, V_{SR} is measured to be 12.02-*V*, close to the value calculated of 12.33-*V*. Next, at a 18-*V* gate bias voltage, V_{SR} is measured to be 24.9-*V* while the calculated is 24.2-*V*. As we can see in both cases, (2.3) still remains accurate since the initial condition voltage is taken into account. Next, the tests are repeated for the NCP4303 SR controller. At a 5-*V* gate voltage without C_{ext}, the V_{SR} is measured to be 12.0-*V* with a calculated value was 11.0-*V*. With a 18-*V* gate voltage, V_{SR} is measured to be 24.0-*V* with a calculated voltage of 23.4-*V*. In all of these tests, the low voltage V_{DS} information is preserved, preserving normal controller operation as evidenced by the $V_{GS,SR}$ gate signal. In conclusion, both controllers are shown to operate normally even with the blocking FET. As also shown above, the experimental bench values matched well with the calculated values from derived equations. (2.3) can therefore be used to find the maximum voltage the SR controller will be subjected to once key variables are defined. Now, a blocking FET can be specifically selected for an optimized blocking solution which reduces overall component count. In a final test, the TI UCC24610 was used to test for total system efficiency on the 84 kHz power stage module, graphed in Fig. 2.13. The SR system boosted the *LLC*-DCX converter efficiency to a maximum of 98.91%. The SR was noted to be more efficient than the diode doubler above 300W of output power. Since no alternative closed-loop high voltage SR method exists, this method is the first of its kind.

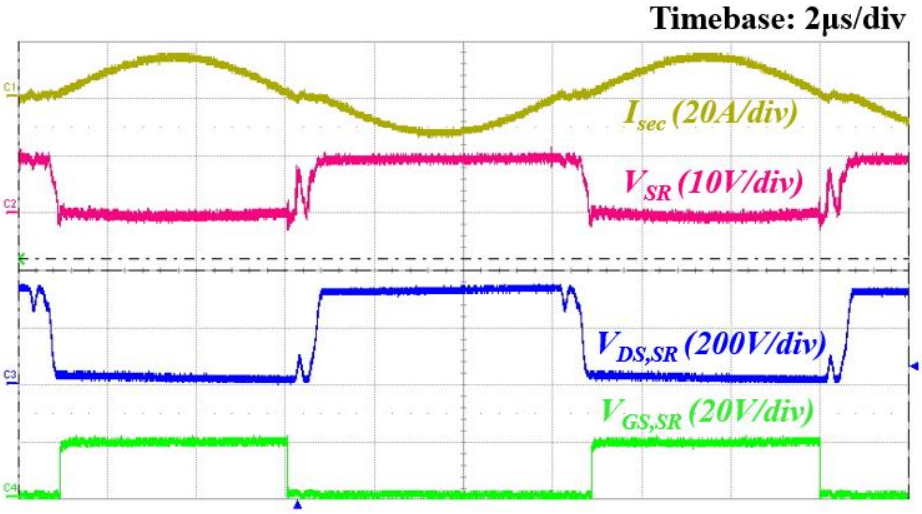

Fig. 2.12. UCC24610 SR controller steady state operational waveforms before and after blocking MOSFET.

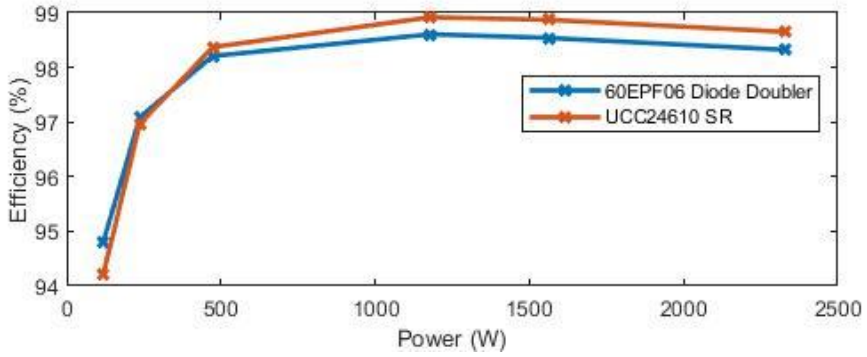

Fig. 2.13. Efficiency comparison before and after SR.

Next, an experiment with over 1-kV_{DS} is performed with a 300 *kHz* *LLC*-DCX converter. The converter parameters are shown below in Table 2.3. The SR board parameters are shown below in Table 2.4. The test bench setup is pictured in Fig. 2.14, with test waveforms depicted in Fig. 2.15. As shown, the blocking FET works perfectly even at over 1-kV_{DS} across the SR switch. Here, the V_{SR} is measured to be 20.7-*V*, with a calculated voltage of 22.4-*V*. These values match well when utilizing the proposed models and equations. Additionally, no visual effects were noted from the change in switching frequency on blocking FET performance, validating high frequency operation. The

frequency is only an issue when the ability to charge C_{SR} to the turn-on and turn-off thresholds is compromised, which is mainly reliant on the SR controller's internal capacitance alone. Here, the proposed solution does not add any discernable effect or delay to SR operation.

TABLE 2.3.
1-*kV LLC*-DCX MODULE POWER STAGE PARAMETERS

Component	Parameter
Resonant Inductance (L_r)	3 μH
Resonant Capacitance (C_r)	56 nF
Magnetizing Inductance (L_m)	32.1 μH
XFMR Ratio (n_{pri}:n_{sec})	9:11
Switching Frequency (f_s)	300 kHz
Primary Switch	GS66516T

TABLE 2.4.
1-*kV* SYNCHRONOUS RECTIFIER BOARD PARAMETERS

Component	Parameter
Gate Drive Voltage	18-V
Gate Driver	TI UCC27531
Synchronous Rectifier Controller	On Semi NCP4303
SR MOSFET	Rohm SCT3080KL
Blocking MOSFET	IXTA06N120P
Blocking MOSFET Gate Voltage	18-V
Gate Resistance (on, off)	4.7 Ω
Maximum V_{DS} Voltage	1.08-kV
C_{out}	470nF

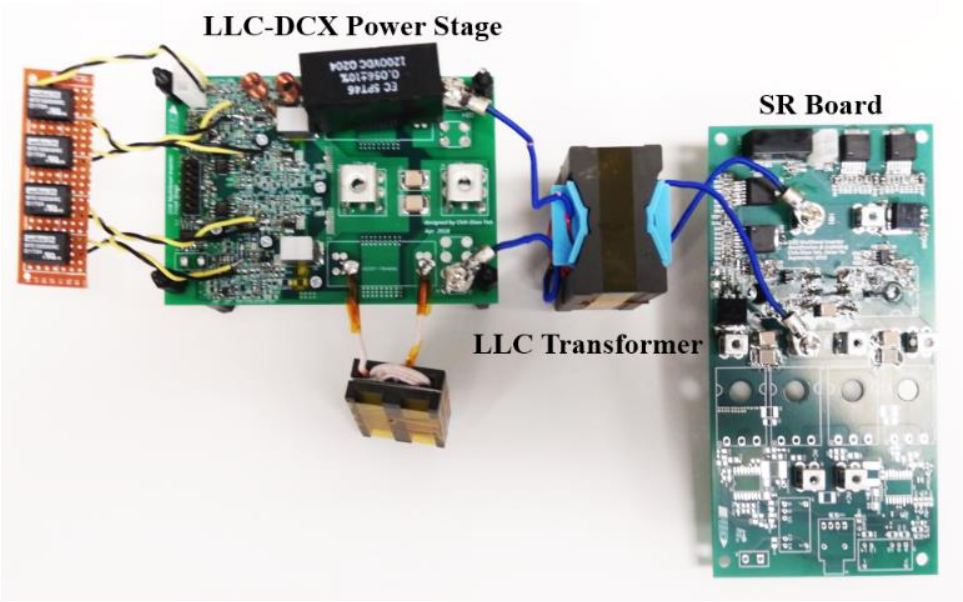

Fig. 2.14. 1-*kV*+ *LLC*-DCX SR test setup with NCP4304.

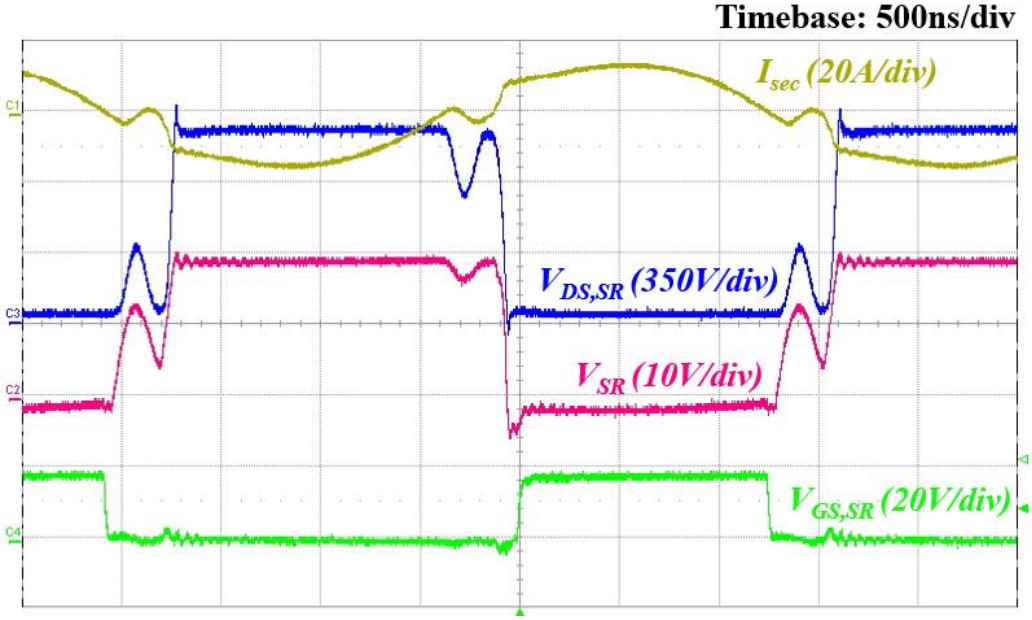

Fig. 2.15. Steady state waveforms of NCP4303 SR controller operating at 1-*kV*+ V_{DS}.

2.4 Summary

In this section, a simple blocking mechanism is proposed to prevent high voltage on drain-source SR controllers. Next, method of operation and design process is presented. Two additional methods to limit voltage are also presented and analyzed. Verification and

validation is performed on a custom SR boards with two different controllers. Testing is performed with two different converters: (1) 2.5-*kW*, 600-V_{in}/350-V_o *LLC*-DCX module; (2) a 1-k*W*, 380-V_{in}/1-kV_o *LLC*-DCX module. Here, the proposed blocking method is proved to preserve full SR controller function at over 1-kV_{DS}. Currently, there is no alternative or other high voltage SR solution that exists for comparison. Therefore, this proposed method method allows for easy and prevalent implementation of low-cost, closed-loop SR which has not been previously achievable. With the proposed blocking method, high voltage SR can be proliferated in many circuits.

Chapter 3

Current Oscillation Issue

3.1 General Description

This section details a current oscillation issue discovered on an *LLC* resonant converter with SR. A duty cycle increase from the SR controller results in a cyclic increase in resonant current (i_{Lr}), in an *LLC*-DCX circuit shown in Fig. 3.1 (a), with the waveforms shown in Fig. 3.1 (b). Here, a jump in the SR switch gate signals from t_{SR2} to t_{SR3} causes a cyclic increase in current and subsequent continuous current oscillations. i_{Lr} increases during this duty jump, which further increases the t_{SR}. This current increase will then propagate into a current oscillation envelope. This duty cycle increase is susceptible at light loads, as a result of poor signal sensing. While this issue was discovered on a drain-source SR system, it has been observed on other current-sense SR architectures as well. The oscillation issue is not specific to one SR algorithm, and thus must be properly root caused for robust design of both future SR controllers and *LLC* converters.

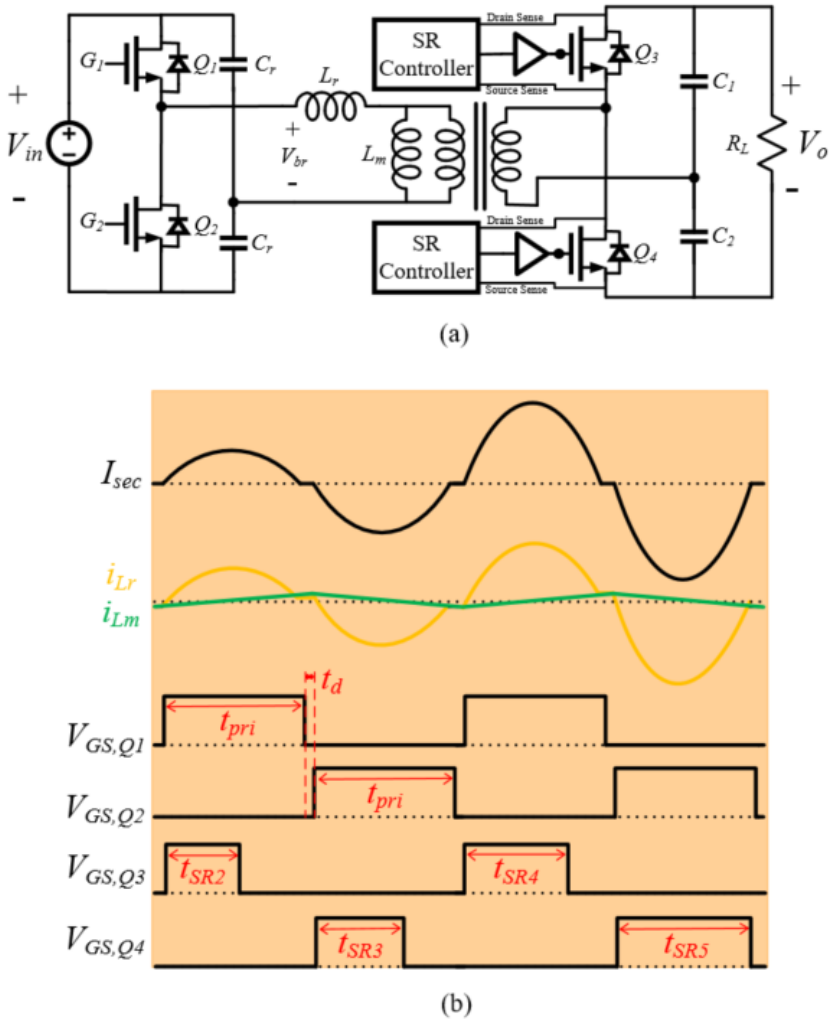

Fig. 3.1. Half-bridge *LLC*-DCX and voltage doubler SR: (a) circuit (b) key initial oscillation waveforms.

3.2 Current Oscillation Phenomena

The simplest solution is to disable SR when oscillating conditions are present. However, this is impractical in high voltage systems due to the voltage isolation requirements and due to the additional current sense circuitry necessary to detect light load conditions. Furthermore, disabling SR would further reduce rectifier efficiency and increase complexity due to the need for load-sensing mechanisms to determine when to disable to rectifier. The majority of commercial SR controllers integrate light load detection

and shutdown mechanisms by measuring the amount of on time [31]-[34]. However, these internal mechanisms actually result in cyclic duty cycle jumps [14]-[16], which also trigger oscillations.

3.2.1 Light Load Detection Mechanism Contributions

The light load detection mechanism is one of the key causes of the oscillations. During normal SR operation, when the switch on time drops under a specific period, the controller disables SR function. Typically, this period is the minimum on time set by the end user. Even so, the SR controller is briefly enabled to re-measure the duty cycle to determine if it is appropriate to turn back on. As a result, this still results in continuous SR duty jumps even in "disabled" conditions. This is further complicated by minimum on and off time controls that the majority of newer SR controllers have. The minimum on and off times are set by the end user through a resistor. However, this can also introduce duty cycle jumps. Take for example a V_{DS} waveform that crosses the $V_{DS,\text{turn-off}}$ right at the peak of the secondary side current, as shown in Fig. 3.2. This is around ~25% duty cycle, or half the SR cycle. If the current condition is below this point, the duty cycle is dictated by the minimum on time. Therefore, an incorrectly set minimum on time far below 25% can result in a large duty cycle jump from the minimum set value to 25% at light load conditions.

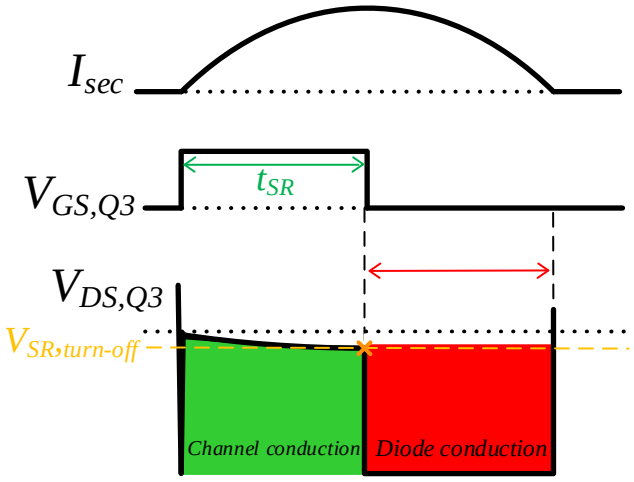

Fig. 3.2. Minimum SR duty cycle near the controller turn-off threshold.

3.2.2 Duty Jump Effects

Therefore, a current oscillation may always occur with existing SR algorithms. Here, we delve deeper into the cause of this oscillation issue for analysis. By understanding the root cause of the oscillation issue, we can propose a number of possible solutions and propose a universal solution that will prevent the oscillation from occurring altogether. Converters operating in light load conditions suffer from poor drain-source signal strength, since the sensed V_{DS} is based on the product of drain-source current and SR switch $R_{DS,on}$. When poor drain-source signal strength is present, the turn off moment is very susceptible to sensing perturbations. This change can initiate a current oscillation in *LLC* converters. Because SR controllers offer only cycle-by-cycle control with no sequential logic, the oscillation cannot be limited or prevented in *LLC*-type converters such as the *LLC*-DCX.

During SR, the SR switch duty cycle is ideally only a function of the secondary side current waveform, I_{sec}. Because this waveform varies across load, turn on and off moments also vary across load. However, this sensed signal can be corrupted by certain factors: (1)

parasitic inductance within drain-source loop; (2) noise from poor SNR. An early SR turn-off issue is present due to parasitics present within the drain-source sense loop, which results in an increase in parallel diode conduction [14]-[16]. An additional source of this unwanted diode conduction can be from the SR controller's sensing discrepancies caused by noise. The amount of this diode conduction directly relates to the converter's output current, forming a codependent network. Therefore, a current oscillation can be initiated between the *LLC* converter and SR controller due to this interdependency from a sudden increase in the SR duty cycle. A SR duty increase causes a cyclic increase in current, resulting in a further duty increase. This oscillation is more susceptible under noisy drain-source sensing conditions, where there is a greater chance of a duty cycle perturbation.

Fig. 3.3 identifies key SR waveforms during early SR turn-off and the resulting parallel diode conduction period. The amount of conduction time between the channel (t_{SR}) and parallel diode conduction (t_{diode}) is solely dependent on the drain-source voltage sensed by the controller. Initially, the controller will detect this parallel diode conduction for the turn-on moment. With the switch on, SR operation occurs. However as the SR switch current decreases, so does the sensed drain-source voltage, decreasing the SNR. When the V_{DS} voltage lowers to the turn-off voltage ($V_{SR,turn\text{-}off}$), shown at moments t_2 and t_4 in Fig. 3.3, then the SR switch is turned off. Any leftover current is rectified through the parallel diode. The turn-off voltages t_1 and t_3 are typically blanked with minimum on time to prevent an early turn-off moment at this moment.

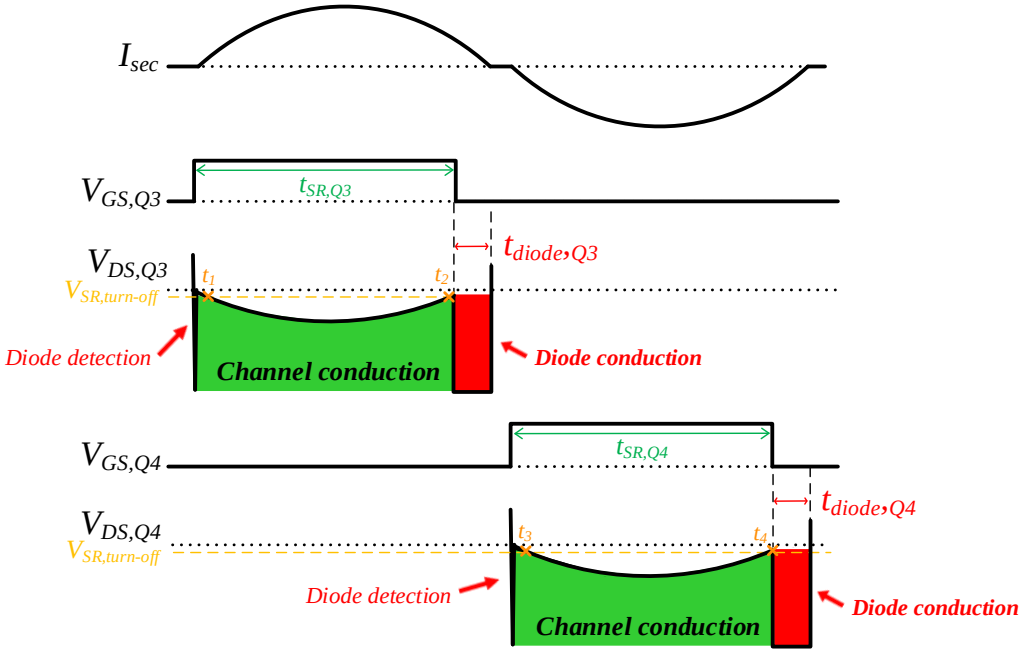

Fig. 3.3. Key SR waveforms during channel and body diode conduction moments.

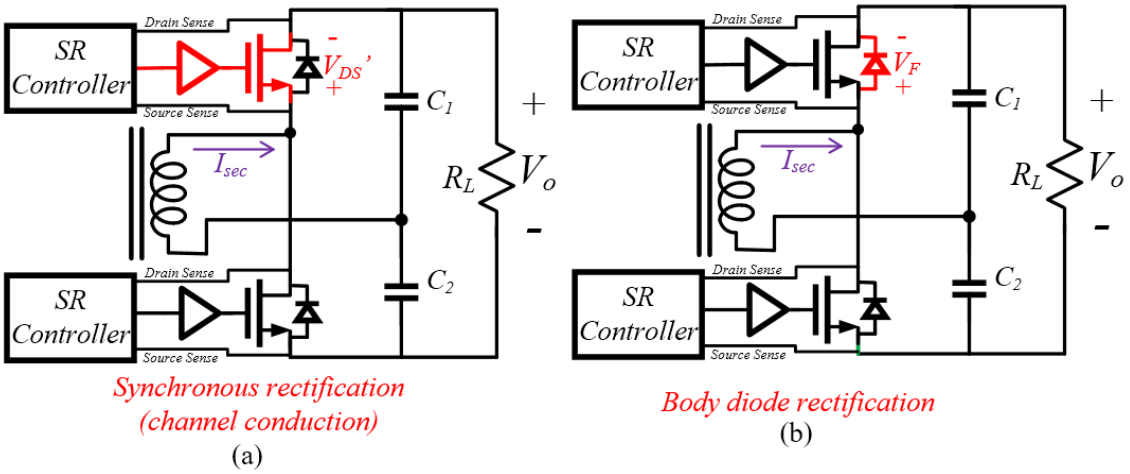

Fig. 3.4. Rectifier voltage drop incurred between: (a) synchronous rectification (b) diode rectification.

There are two rectification paths present: (1) channel-conduction during SR; (2) parallel (body) diode conduction. Every rectification path results in a specific voltage drop. In SR, there is a voltage drop of V_{DS}' in the rectifier loop, as shown in Fig. 3.4 (a). Here, V_{DS}' is the product drain-source current and channel resistance, (2). This is a very small

voltage drop, in the milli-volts. However V_F, the diode forward drop, is greater in magnitude. Because a greater channel conduction period results in more secondary side current, a rectifier with a large difference between $V_{DS'}$ and V_F results in an oscillation-prone system. Therefore, an increase in diode conduction time causes the output voltage to drop, and vice versa. A decrease in the amount of diode conduction time results in an effect in an *LLC* converter akin to a load transient.

Next, we will explain the difference in the conduction states' effect on an *LLC* converter with steady-state models and trajectories. The state trajectory of an *LLC* converter is a graphical depiction of the energy present within the resonant tank, which has direct relation to the amount of secondary side current. Certain assumptions are made to simplify analysis: (1) channel resistance and resonant tank loss is trivial; (2) the total output capacitance C_o is ignored because $C_o >> C_r$. Including SR operation, there results in four key operating modes during each SR cycle. Here, the output capacitance includes the bus capacitor C_o along with the doubler rectifier capacitors. Finally, the equivalent circuits in four different operating modes in the positive half-cycle is depicted in Fig. 3.5 (a)-(d). The models shown are for a half bridge primary, doubler rectifier *LLC* converter. Because the negative half cycle can also be derived in a similar method, it is not shown here.

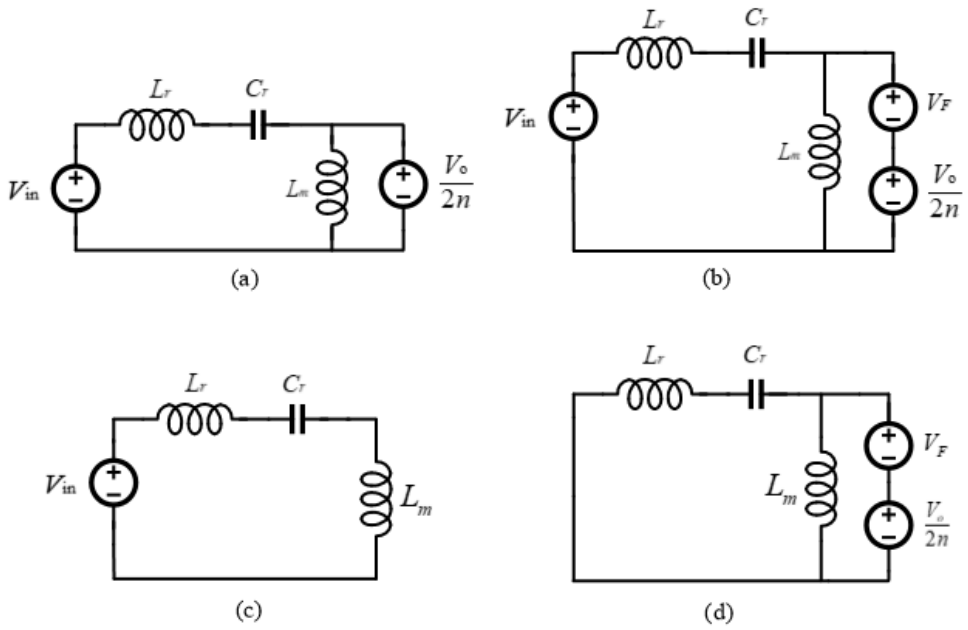

Fig. 3.5. Equivalent resulting *LLC* circuit models for: (a) Mode 1: Switch channel (SR) conduction, (b) Mode 2: Parallel diode conduction, (c) Mode 3: Discontinuous, and (d) Mode 4: Discharging.

In Mode 1, Q_1, the primary switch turns on and resonant current runs through Q_3, the secondary side switch's channel. Here, the magnetizing inductance L_m is clamped by the voltage at the output. The equivalent circuit is shown in Fig. 3.5 (a) [41]. Next, the resonant current i_{Lr} and resonant capacitor voltage v_{Cr} can be expressed as (3.1) and (3.2), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos(\omega_{r0}(t-t_0)) + \frac{\left(V_{in} - \frac{V_o}{2n} - v_{Cr0}\right)}{Z_{r0}}\sin(\omega_{r0}(t-t_0)) \tag{3.1}$$

$$v_{Cr}(t) = \left(V_{in} - \frac{V_o}{2n}\right) - \left(V_{in} - \frac{V_o}{2n} - v_{Cr0}\right)\cos(\omega_{r0}(t-t_0)) + Z_{r0}i_{Lr0}\sin(\omega_{r0}(t-t_0)) \tag{3.2}$$

V_{in} and V_o model the *LLC* converter's input and output voltage, respectively, with $\omega_{r0} = 1/\sqrt{L_r \cdot 2C_r}$ representing the resonant angular frequency and $Z_{r0} =$

$\sqrt{L_r/(2C_r)}$ the impedance of the resonant network. Based on (3.1) and (3.2), the resulting trajectory equation is shown in (3.3).

$$(v_{Cr}(t)-(V_{in}-\frac{V_o}{2n}))^2+(i_{Lr}(t)\cdot Z_{r0})^2=(V_{in}-\frac{V_o}{2n}-v_{Cr0})^2+(i_{Lr0}\cdot Z_{r0})^2 \tag{3.3}$$

(3.3) graphs as a circle with a center at ($V_{in} – V_o/2n$, 0), with radius R_1 dependent on the initial conditions v_{Cr0} and i_{Lr0} shown below in (3.4).

$$R_1=\sqrt{(V_{in}-\frac{V_o}{2n}-v_{Cr0})^2+(i_{Lr0}\cdot Z_{r0})^2} \tag{3.4}$$

In Mode 2, Q_1 the primary switch stays on, but the resonant current continues to run through the secondary side switch Q_3's parallel diode. This mimics Mode 1, but with the addition of the body diode voltage drop V_F in the resulting equivalent circuit shown in Fig. 3.5 (b). This results in the time domain equations for the state variables i_{Lr} and v_{Cr} for this mode of (3.5) and (3.6), respectively.

$$i_{Lr}(t)=i_{Lr0}\cos(\omega_{r0}(t-t_0))+\frac{\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n}\right)}{Z_{r0}}\sin(\omega_{r0}(t-t_0)) \tag{3.5}$$

$$v_{Cr}(t)=\left(V_{in}-\frac{V_o}{2n}-\frac{V_F}{n}\right)-\left(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n}\right)\cos(\omega_{r0}(t-t_0))+Z_{r0}i_{Lr0}\sin(\omega_{r0}(t-t_0)) \tag{3.6}$$

Also like Mode 1, the resulting trajectory is circular in nature, but with a center of ($V_{in} – V_o/2n – V_F/n$, 0), and a radius R_2 as shown in (3.7).

$$R_2=\sqrt{(V_{in}-\frac{V_o}{2n}-v_{Cr0}-\frac{V_F}{n})^2+(i_{Lr0}\cdot Z_{r0})^2} \tag{3.7}$$

Mode 3 happens whenever the resonant frequency is above the switching frequency. Here, Q_1 stays on but without any current flowing through to the secondaries. Here, the magnetizing inductor L_m also enters into the resonance, resulting in the equivalent circuit shown in Fig. 3.5 (c). Next, the time domain equations of state variables i_{Lr} and v_{Cr} for this specific mode are given below in (3.8) and (3.9), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos(\omega_{r1}(t-t_0)) + \frac{(V_{in} - v_{Cr0})}{Z_{r1}}\sin(\omega_{r1}(t-t_0)) \tag{3.8}$$

$$v_{Cr}(t) = V_{in} - (V_{in} - V_{Cr0})\cos(\omega_{r1}(t-t_0)) + Z_{r1}i_{Lr0}\sin(\omega_{r1}(t-t_0)) + Z_{r0}i_{Lr0}\sin(\omega_{r0}(t-t_0)) \tag{3.9}$$

Where $Z_{r1} = \sqrt{(L_r + L_m)/2C_r}$ defines the characteristic impedance, and $\omega_{r1} = 1/\sqrt{(L_r + L_m)\cdot 2C_r}$ represents the resonant frequency. Then, the resulting trajectory is derived from (3.8) and (3.9).

$$(v_{Cr}(t) - V_{in})^2 + \left(\frac{i_{Lr}(t)\cdot Z_{r0}}{Z_{r0}/Z_{r1}}\right)^2 = (v_{Cr0} - V_{in})^2 + (i_{Lr0}\cdot Z_{r1})^2 \tag{3.10}$$

Based on (18), we see that this graphs an ellipse centered at (V_{in}, 0). Finally, we have Mode 4 which occurs when the resonant frequency is below the switching frequency. Here, Q_1 turns off and Q_2 turns on. Because this follows Mode 2, the resonant current will also continue to flow through the secondary side switch's parallel diode. This resulting equivalent circuit is depicted in Fig. 3.5 (d), with the i_{Lr} and v_{Cr} time domain equations shown in (3.11) and (3.12), respectively.

$$i_{Lr}(t) = i_{Lr0}\cos(\omega_{r0}(t-t_0)) - \frac{\left(v_{Cr0} + \frac{V_F}{n} + \frac{V_o}{2n}\right)}{Z_{r0}}\sin(\omega_{r0}(t-t_0)) \tag{3.11}$$

$$v_{Cr}(t) = -\left(\frac{V_F}{n} + \frac{V_o}{2n}\right) + \left(v_{Cr0} + \frac{V_F}{n} + \frac{V_o}{2n}\right)\cos(\omega_{r0}(t - t_0)) + Z_{r0} i_{Lr0} \sin(\omega_{r0}(t - t_0))$$

(3.12)

Here, the trajectory is analogous to Mode 1 but with a centering at ($-V_o/2n - V_F/n$, 0) and with a radius dependent on initial conditions of V_{cr0} and I_{Lr0}.

The four derived modes are graphed below in Fig. 3.6 and compared with simulated trajectories to verify the equations (3.1)-(3.12) when the *LLC* operates in three conditions: (1) under resonant frequency, $f_s < f_o$; (2) at resonant frequency, $f_s = f_o$; (3) above resonant frequency, $f_s > f_o$. The steady state time-domain waveforms under the same operating conditions are also shown in Fig. 3.7. However, because the oscillation and its root cause originates under all three of these conditions, the $f_s = f_o$ model is utilized to analyze the state trajectory channel and parallel diode conduction.

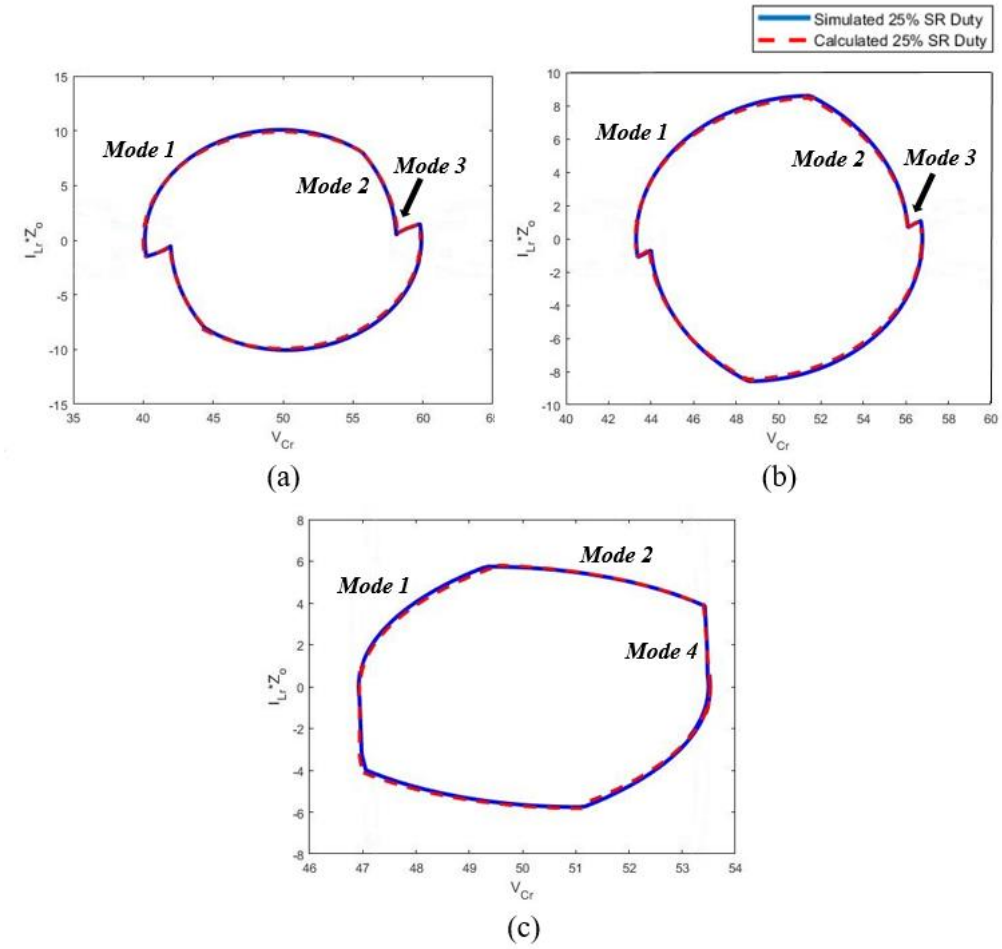

Fig. 3.6. Resonant tank state trajectory modes for 25% SR duty cycle for: (a) $f_s < f_o$, (b) $f_s = f_o$, (c) $f_s > f_o$.

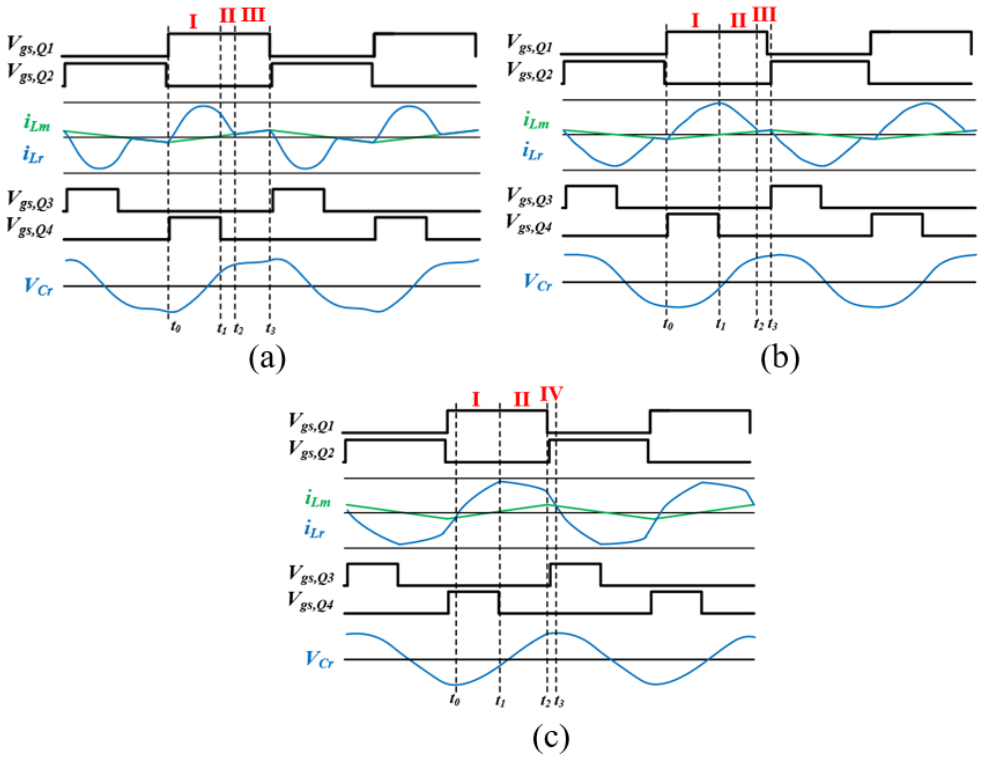

Fig. 3.7. *LLC* time-domain steady state waveforms for: (a) $f_s < f_o$, (b) $f_s = f_o$, (c) $f_s > f_o$.

Resonant tank energy is directly related to the radius of the state trajectory, (3.4) and (3.7). Here, the equations show that diode conduction decreases this energy, while channel conduction increases it. In turn, an increase in SR duty cycle causes a cyclic increase in tank current, and ΔV_{Cr}. The result is a progressively increase in R_1 from (3.4), which also raises the secondary side current magnitude and charges C_o, the net output capacitance, above the steady state voltage. Because a diode drop drops the output voltage, a rise in the SR duty cycle therefore also increases the output voltage. At some point the output voltage and current peaks, which results in the oscillation decaying. Here, this is coined the "false load transient" phenomena, where a ringing effect occurs between the resonant tank and C_o when the converter attempts to self-compensate for the step change in the output voltage. This is

extremely similar to an output load step condition [42]-[44]. Therefore, the net output capacitance has a direct impact on the period of the observed oscillation envelope.

In order to contrast the energy differences in Modes 1 and 2, the simulated trajectory is now plotted alongside the calculated trajectory for the $f_s = f_o$ case, shown in Fig. 3.8 (a). Here, simulations were made based on the converter specifications listed in the following section with a 100-*V* input voltage. The trajectories match well, and the figure clearly shows that the diode voltage drop raises the energy delta between the trajectories.

Next, Fig. 3.8 (b) shows a trajectory from 0 to 25% SR duty cycle. Here, this shows that an increase in the duty cycle boosts the radius trajectory, which is equivalent to an output load step. Therefore, this could cause an interdependency effect between the *LLC* converter and SR controller. The SR controller will increase the duty cycle since the *LLC* converter secondary side current increases. At SR duty cycles over 25%, the state trajectory marginally shrinks, graphed in Fig. 3.8 (c).

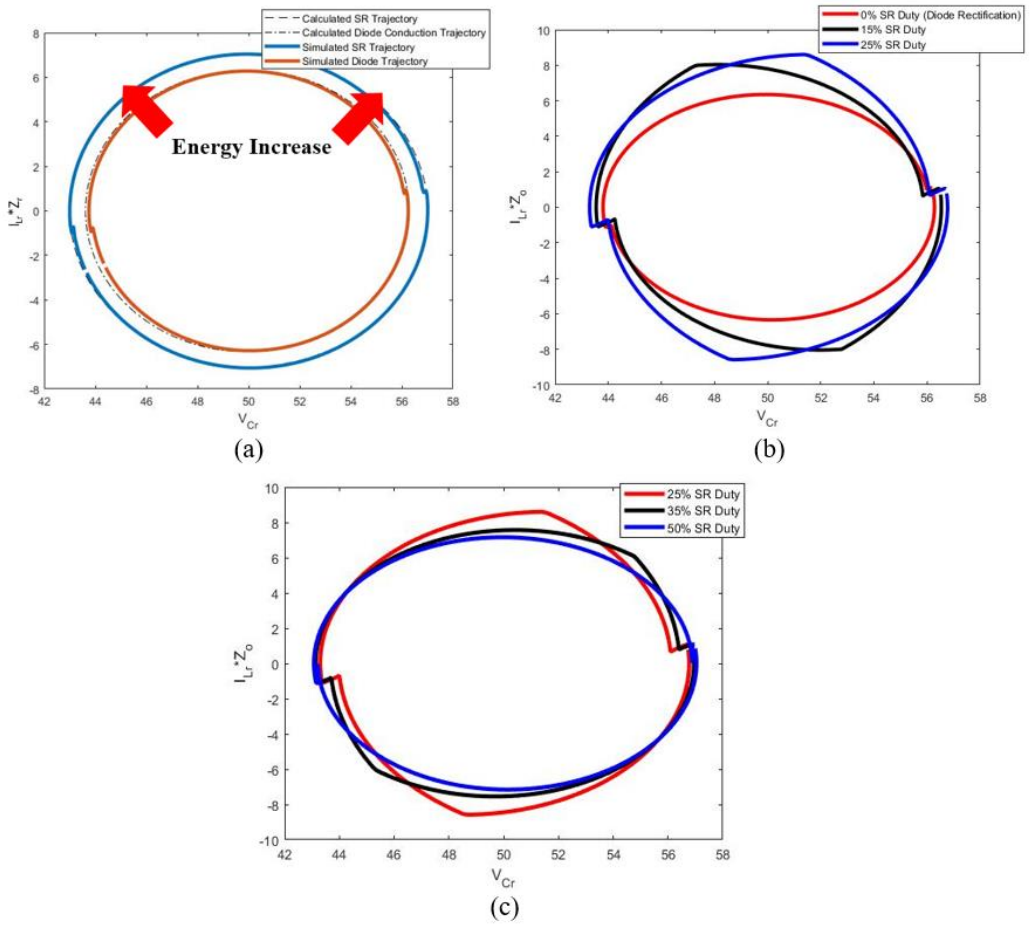

Fig. 3.8. Trajectory difference between: (a) simulated and calculated switch channel, diode conduction (b) 0 to 25% SR duty cycle (c) 25 to 50% SR duty cycle.

Finally, Fig. 3.9 puts everything discussed together and into one oscillation period, t_e. Again, the oscillation starts with a rogue increase in the SR duty cycle, which results in a cyclic current increase. This increase in current causes the output voltage to overshoot steady state values, which causes the current to cyclically decay. This causes a decrease in the SR duty cycle until the controller hits light load detection and stops triggering SR. When the output voltage drops and current increases again, the SR controller again turns on – causing a duty cycle jump, and reinitiating the oscillation.

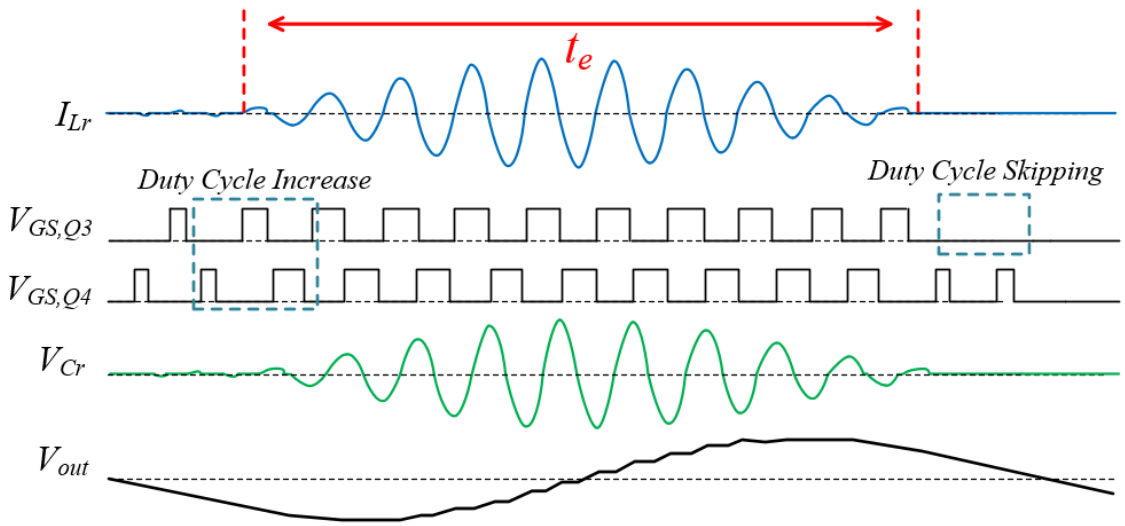

Fig. 3.9. Time-domain waveform of one oscillation period induced by a duty cycle increase.

3.2.3 SNR and Noise Effects

The initial turn-on of SR, noisy drain-source signals, and light load detection devices are all sources of potential SR duty cycle perturbations. The first two sources have been previously discussed, but now the focus is moved onto the third and final source - noise. Noise is the prominent issue at light load conditions, since the drain-source signal strength drops proportionally with $R_{DS,on}$ and current.

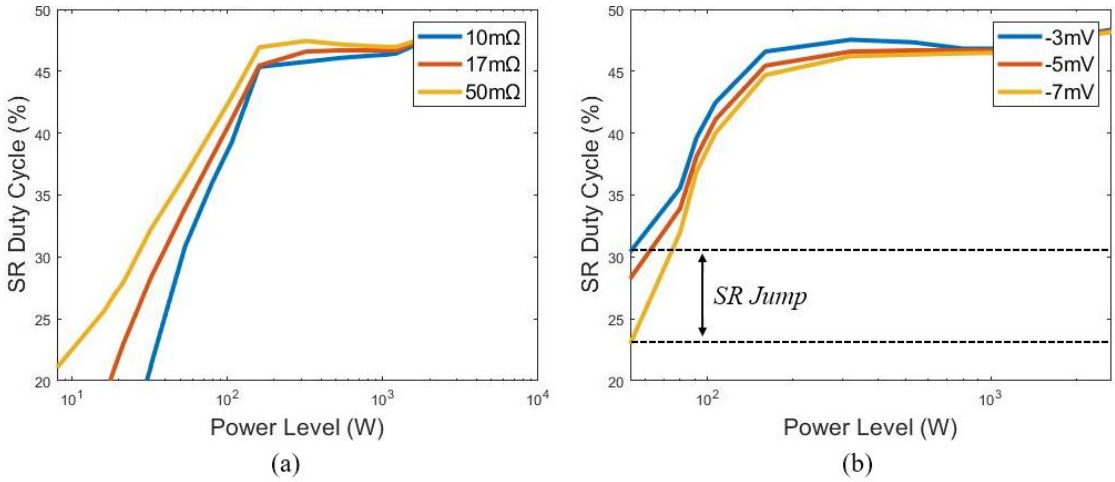

Fig. 3.10. Change in SR duty cycle over power across different (a) $R_{DS,on}$ and (b) turn-off voltage threshold, $V_{SR,turnoff}$.

Fig. 3.10 (a) graphs ideal SR switch duty over power across three different $R_{DS,on}$ switch values. We can observe that lower $R_{DS,on}$ switches result in much lower SR duty cycles across load, but predominantly at light load. Meanwhile, a higher $R_{DS,on}$ switch increases the SR duty cycle across load. Similarly, Fig. 3.10 (b) depicts a similar effect when the SR controller turn-off threshold, $V_{SR,turnoff}$, is varied. With only ±2-mV perturbation in turn-off voltage threshold, a ~15% duty cycle increase can be observed. Therefore, any noise superimposed on top of the sensed signal has a similar effect to changing the turn-off threshold. When modeling the secondary side current as sinusoid, (1.5) can be modified into (3.13) for one SR cycle. Because noise is superimposed onto (3.13), it is simply added on top to produce (3.14). V_n represents noise amplitude in volts, $I_{sec,pk}$ the secondary side current peak, $R_{DS,on}$ is the SR switch channel resistance when on, and $V_{DS,SR}$ the drain-source voltage waveform across the switch.

$$V_{DS,SR}(t) = -I_{\sec,pk}\sin(2\pi f_s t)R_{DS,on} \tag{3.13}$$

$$V_{DS,SR}(t) = -I_{\sec,pk}\sin(2\pi f_s t)R_{DS,on} \pm V_n \tag{3.14}$$

In conclusion, the oscillation phenomena is the result of a variety of factors including the SR controller characteristics, disappearing rectification diode drop, noise, and *LLC* converter load response characteristics. Since this dissertation focuses on developing a high voltage SR solution, the SR controller must be designed to suppress the oscillations. The key to eliminating the oscillations is removing the duty cycle perturbations. The next section discusses a novel method to eliminate such perturbations by limiting the output duty cycle across time.

3.3 Duty Cycle Rate Limiting

In this section, a digital rate limiting algorithm is designed and implemented to eliminate duty cycle perturbations from an SR controller. This method digitally stabilizes the duty cycle by effectively digitally limiting the sampling rate. This is achieved through a field programmable gate array (FPGA) in order to continuously and cyclically post-process SR controller gate signals.

The method of duty cycle rate limiting focuses on restricting the SR duty cycle's rate of change over time ($\Delta D/\Delta t$). Here, this is achieved by post processing the SR controller gate signals with an FPGA, shown by the systems level signal flow diagram in Fig. 3.11, and the simplified algorithm flowchart in Fig. 3.12. Fig. 3.13 shows how the FPGA is attached to the doubler rectifier to post-process the SR controller gate signals. At a high level, both the low and high side controller signals are synchronized and uniformly rate limited under one global FPGA clock. In order to achieve this, both SR controller signals communicate with the FPGA through discrete digital signal isolators for level shifting and isolation.

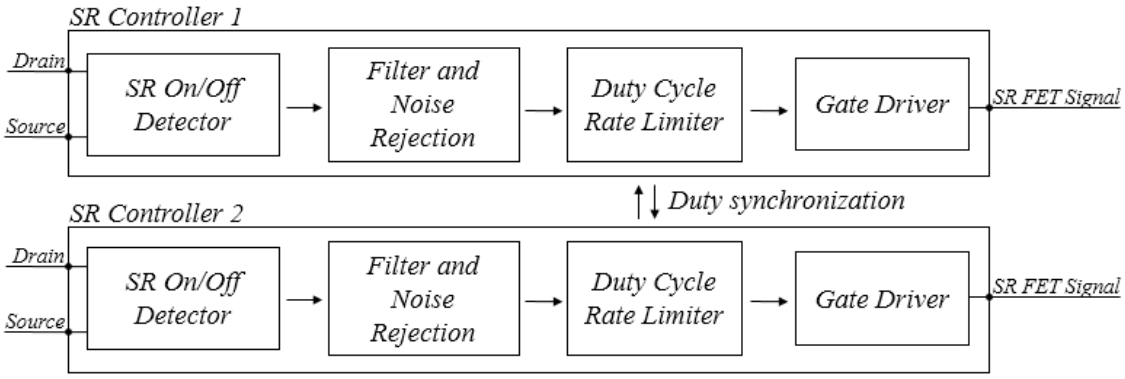

Fig. 3.11. Signal block diagram of proposed duty cycle rate limited SR controller.

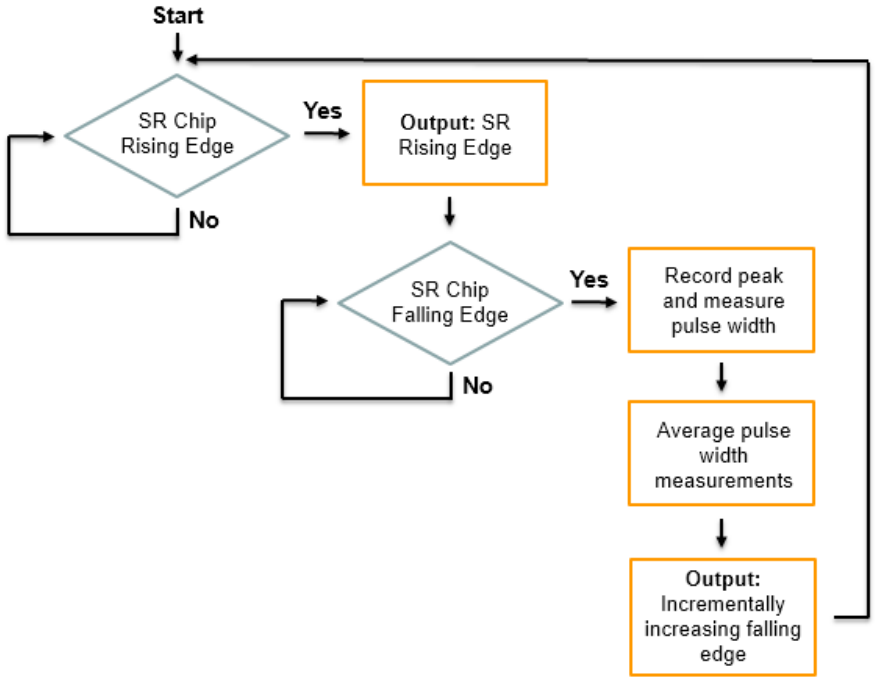

Fig. 3.12. Simplified duty cycle rate limiting algorithm flowchart.

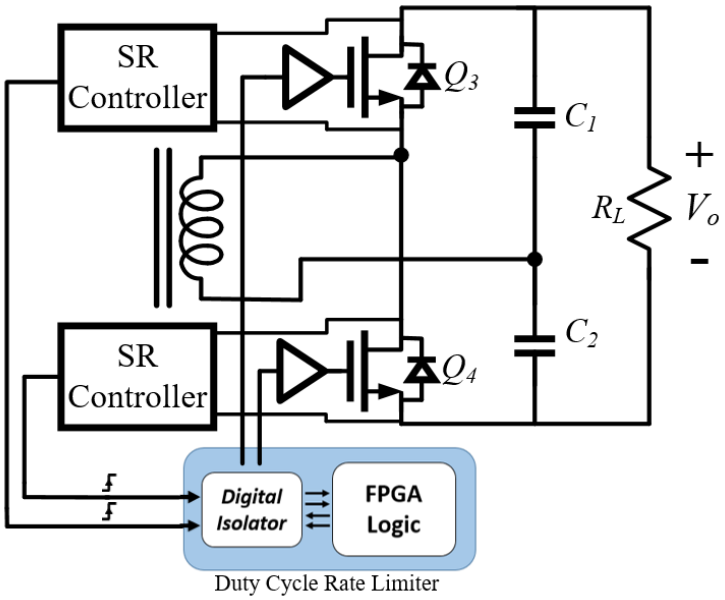

Fig. 3.13. Duty cycle rate limited drain-source doubler SR diagram.

In Fig. 3.11, the FPGA logic is composed of two separate sequential logic blocks, one for each controller - SR Controller 1 and 2. Each logic block is synchronized with the SR controller gate signal's rising edge. The first block shown inside is the SR on/off detector, which is the edge triggered block. Instead of using traditional signal sampling with ADCs, FPGA logic is used for cycle-by-cycle control and to minimize propagation delays. When this block senses a rising edge, it is simultaneously passed through the FPGA to the gate driver. This fully preserves the SR turn-on function. A counter begins counting at the rising edge up until thefalling edge is detected, with the FPGA measuring the amount of time passed between the two edges.

The second block is the noise rejection and filtering block. Here, filtering and noise rejection is achieved through a moving average filter. Based on the filter's sample size, this block will also reduce the effective $\Delta D/\Delta t$ rate in the next block due to the filter's moving

average delay. (3.15) represents the filter's output value based on *M*, the number of samples and *k*, the number of filter taps.

$$y[n] = \frac{1}{M}\sum_{k=0}^{M-1} x[n-k] \tag{3.15}$$

The third block, the rate limiter block, limits the positive $\Delta D/\Delta t$ by tracking time through a counter. The maximum duty cycle that can be achieved at any given time is limited by the prior moving average filter. The falling edge is limited in time until after the rate of delay has been achieved. Only after is a falling edge sent to both gate drivers to end the SR cycle.

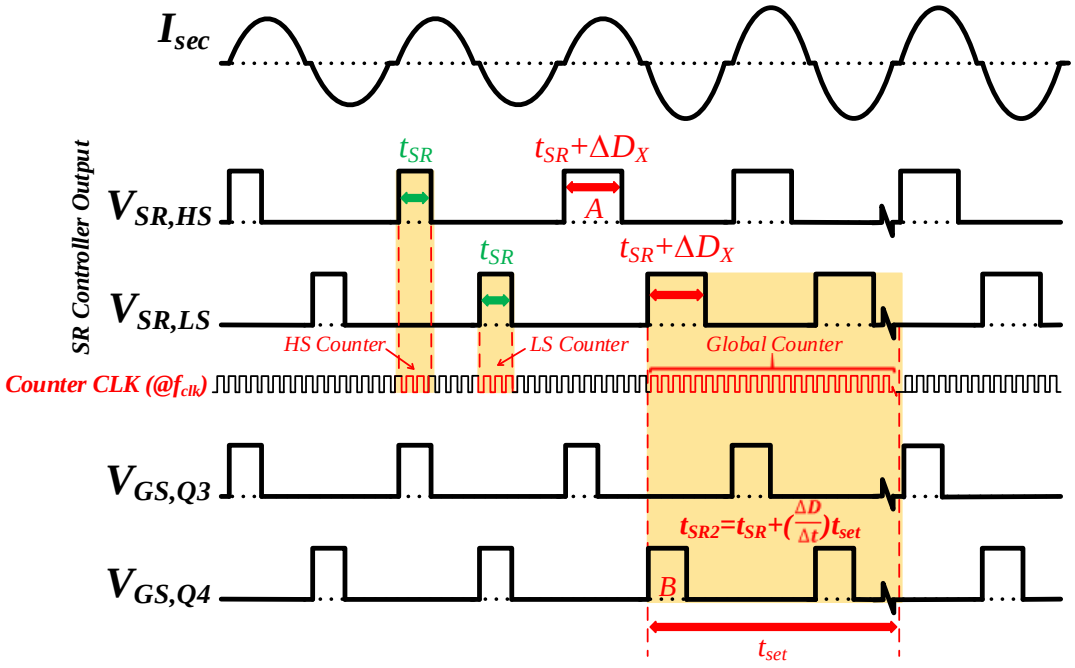

Fig. 3.14. Pre/post FPGA processed SR duty cycle waveforms.

Fig. 3.14 shows a snippet of the rate limiter operation during a duty step output. I_{sec} represents the secondary-side current, V_{SR} the SR controller gate signals, and V_{GS} the gate drive signals sent to the SR switches from the FPGA. t_{SR} represents the steady state output

signal from the SR controller. A continuous counter clock is run at frequency f_{clk} which measures time elapsed during rate limiting, and additional counters HS Counter and LS Counter to measure the duty cycle of the SR controller output in discrete time.

Pulse A represents the original steady state output signal, but increased by some ΔD_X, where ΔD_X is greater than the set ΔD. For simplicity in this example, it is assumed the averaging filter has a sample size of one and thus no delay. The duty cycle output to the SR switches are then incremented by a user-defined ΔD, with the falling edge delayed from the rising edge by a period defined by (19). ΔD can be derived as a function of the user defined $\Delta D/\Delta t$ value and f_{clk}, as discussed later. Here, t_{set} is a user-defined time delay constant. This results in an output of pulse *B* in the figure. The period of t_{set} is digitally counted in a global counter to allow for the secondary-side current to settle after the duty increase. After t_{set} has elapsed, the duty cycle can be increased again if ΔD_x was greater than the ΔD increment.

$$t_{SR2} = t_{SR} + \left(\frac{\Delta D}{\Delta t} \right) t_{set} \tag{3.16}$$

The $\Delta D/\Delta t$ value must be tuned for the *LLC* converters' transient operating characteristics. Anticipated maximum and minimum duty cycles can be extricated through Fig. 3.10 (a) to find the maximum ΔD across a certain load range. Next, the resolution can be calculated dependent on the clock frequency the logic is fed by, and on the amount of necessary time for settling the output. This time can be estimated based on the previous circuit analysis. Furthermore, the positive and negative $\Delta D/\Delta t$ rates can be tuned independently. The steady state duty cycle is still determined by the SR controller, the rate limiter specifically limits the duty cycle rate of change. During bench tests, a $\Delta D/\Delta t$ of 1%

per 10-*mS* is selected. This results in around 600 digital counter increments for each SR cycle, or 10-*nS*. A sample size of 4 is used, with continuous sampling.

3.3.1 Rectification Drop Oscillation Simulations

Initial simulations are performed to validate the theory of a larger diode drops increasing the susceptibility of oscillation, predominantly at light load conditions. This is achieved by modeling a drain-source SR controller and comparing two theoretical diode drops: 0.4-*V*, 5-*V*. This is simulated with three different SR switch channel resistances: 5$m\Omega$, 10$m\Omega$, and 20$m\Omega$. Light load detection is not modeled in this controller. Fig. 3.15 (a), 3.15 (c), and 3.15 (e) validates this theory and shows how a small diode drop voltage results in normal SR operation at light load across all tested $R_{DS,on}$ values. Next, we see in Fig. 3.15 (b) and (d) how a larger diode drop voltage when used with lower $R_{DS,on}$ switches results in a current oscillation issue. When $R_{DS,on}$ is high enough, operation returns to normal in Fig. 3.15 (f). These simulations validate the hypothesis that the diode drop magnitude has a great impact in causing current oscillations.

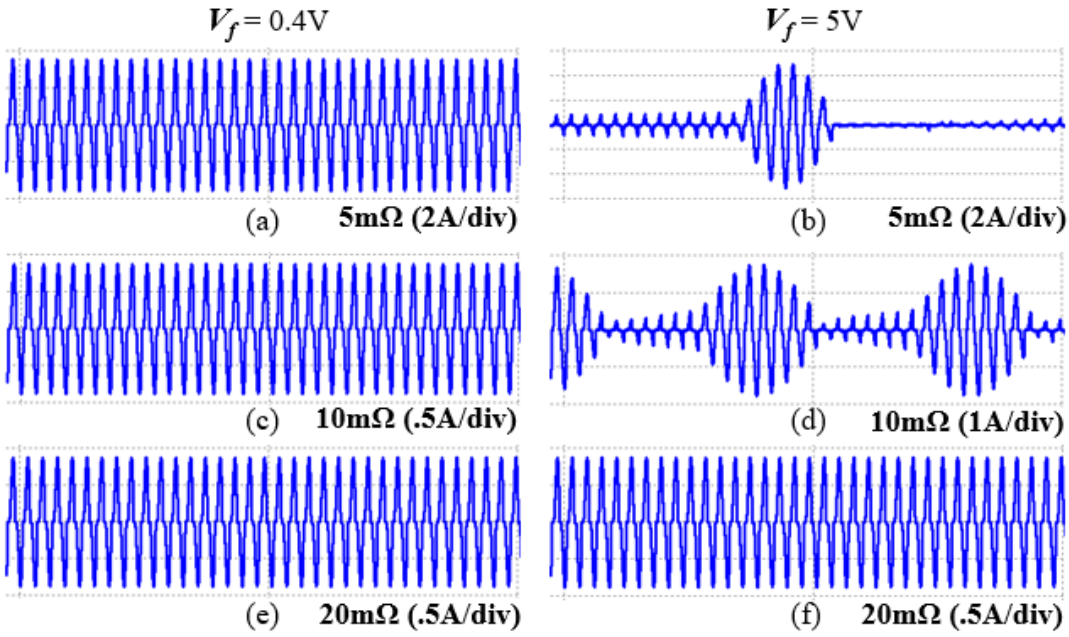

Fig. 3.15. Secondary side current waveform stability comparison at varying $R_{DS,on}$, V_f values.

3.3.2 Noise Measurements

This section will extrapolate on quantifying the effect of low signal-to-noise (SNR) on the SR controller through measurements. SNR is defined as the ratio between signal power and noise power, defined as (3.17) [45].

$$SNR = 20\log\left(\frac{V_{signal,RMS}}{V_{noise,RMS}}\right) \tag{3.17}$$

Here, the signal power in the drain-source voltage signal from the SR switch during SR and the noise power the additive noise in the sensing loop. With (3.14) we can model the signal power assuming ideal SR by calculating the root-mean-square (RMS) of the V_{DS} signal. Next, noise power is physically measured with the SR circuitry on, no *LLC* input voltage, at a 20MHz bandwidth, with a Tektronix MDO4104C oscilloscope. No probe attenuation was utilized, and measurements were taken with the probe ac-coupled and with

low inductance ground leads. The resulting noise RMS was measured to be 15.3-mV_{RMS} on the low side, and 19.9-mV_{RMS} on the high side. However, for accuracy, the noise of the scope probe itself must be removed. This can be achieved due to the relationship shown by (3.18), with the noise from the measured trace and noise of the probe assumed to be incoherent. The probe is grounded and the RMS noise is measured, which resulted in 130-μV_{RMS}. From (3.18), the true V_{RMS} of the noise signal can be calculated, which is found to be 15.299-mV_{RMS} for the low side, and 19.899-mV_{RMS} for the high side.

$$V_{RMS,measured}{}^2 = V_{RMS,signal}{}^2 + V_{RMS,noise}{}^2 \tag{3.18}$$

The SNR of the drain-source signal is calculated to be 5.27dB on the low side, and 2.98dB on the high side using an approximation of the secondary side current magnitude at a 50W load, where oscillations were noted during tests.

3.3.3 Bench Verification and Validation

Next, bench tests were performed to capture live waveforms of the current oscillation. At a 600-V_{in}, 340-V_o operating condition with 180-W load, oscillations can be found as shown in Fig. 3.16 (a). Likewise, the oscillation occurs at a 100-V_{in}, 35-W load condition depicted in Fig 3.16 (b). Specific SR board parameters are listed below in Table 3.2. Differences between the two oscillation envelopes are attributed to the differing levels of noise at each test condition, which is evidenced in the differing gate signals. Next, simulations are performed under the same test conditions with a SR controller model, which resulted in the same oscillation depicted in Fig. 3.16 (c). In conclusion, this oscillation issue can be found at numerous input voltage conditions since the oscillation is dependent on the SNR of the drain-source signal.

The proposed rate limiting solution is bench tested on a 2.5-kW, 600V_{in}, 340-V_o *LLC*-DCX. The *LLC* converter and SR board parameters are noted below in Table 3.1 and 3.2, respectively. The physical bench test setup is depicted in Fig. 3.17 and 3.18. During bench test, the FPGA duty cycle rate limiter is shown to work as intended, removing all current oscillations at previously unstable conditions. During testing, the SR controller resorted to the user-set minimum on time. This resulted in varying SR duty cycles of up to 50% tested. When given a SR duty increase, the FPGA rate limiter allowed for steady transient operation. As shown in Fig. 3.19 (a) to (c), the duty cycle increase over time until steady state is achieved. As evidenced through the stable, normal secondary side current, I_{sec}, and output voltage waveform $V_{o,ac\text{-}coupled}$, the oscillations are not present. Therefore, the proposed method of duty rate limiting allows for stable, consistent SR operation across load.

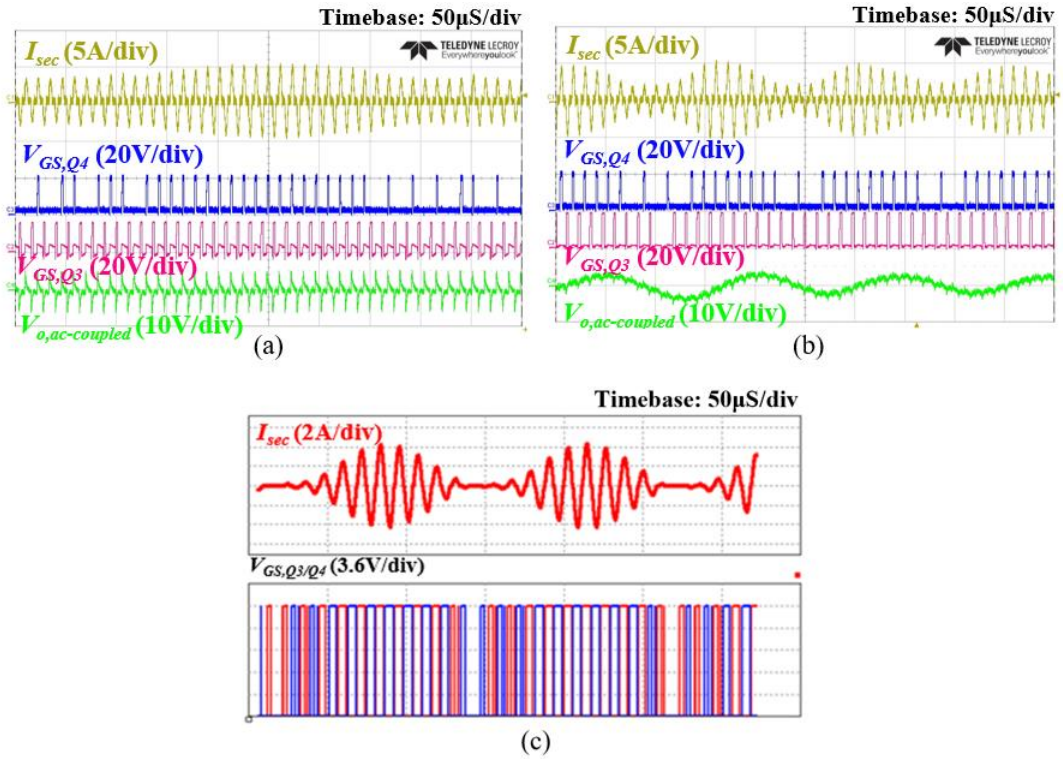

Fig. 3.16. Time-domain current oscillation waveforms during (a) full input voltage (b) reduced input voltage condition (c) under simulation.

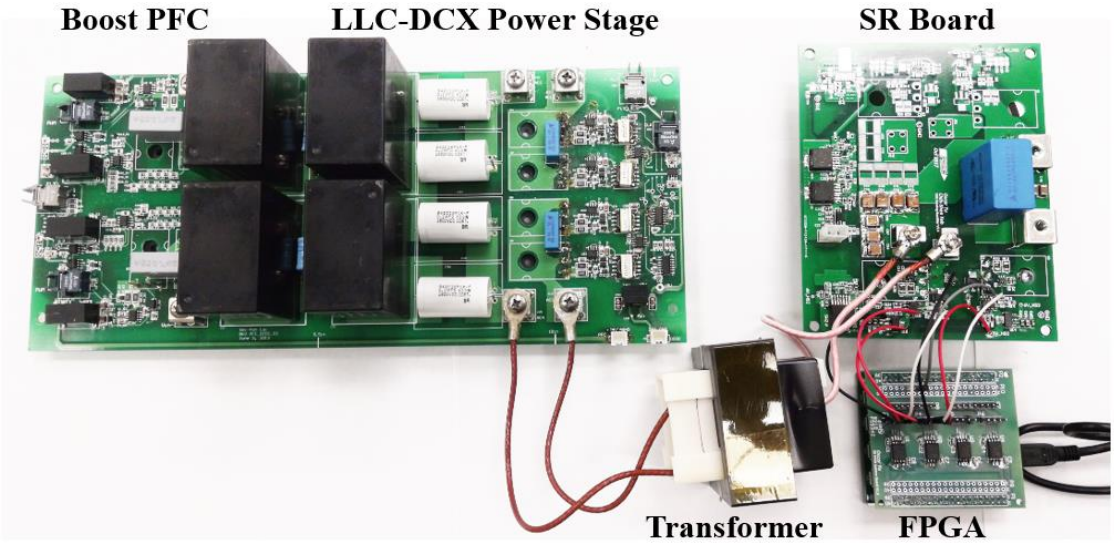

Fig. 3.17. Test bench *LLC*-DCX power stage module with SR and an FPGA.

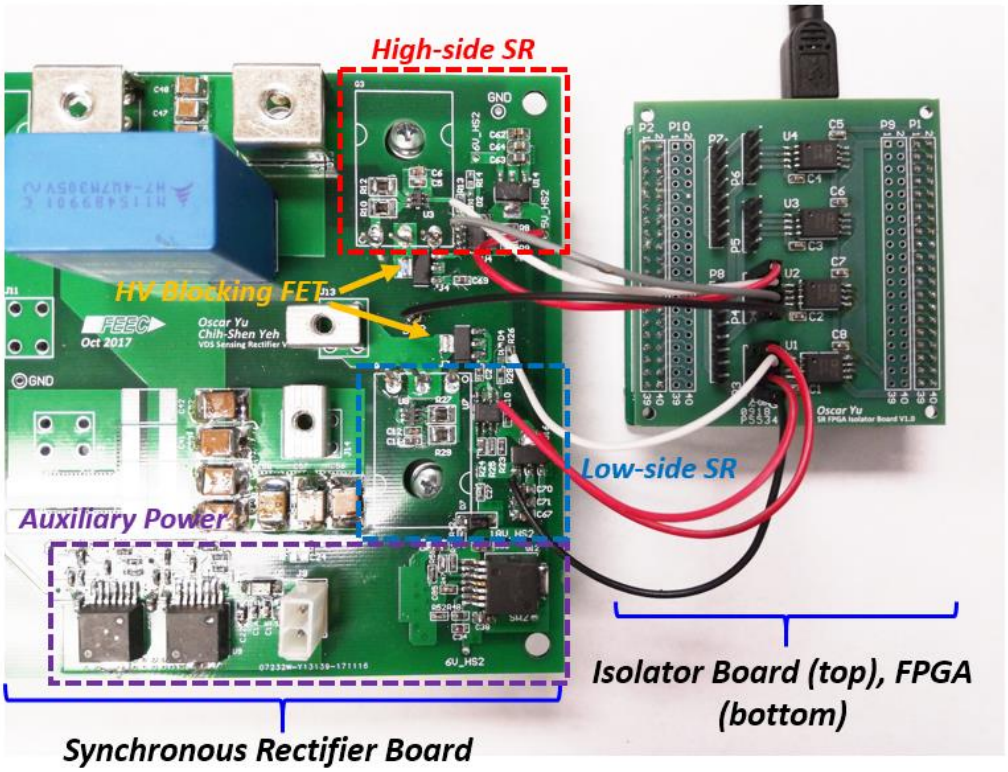

Fig. 3.18. Close up of SR doubler rectifier (left), isolator board and FPGA (right).

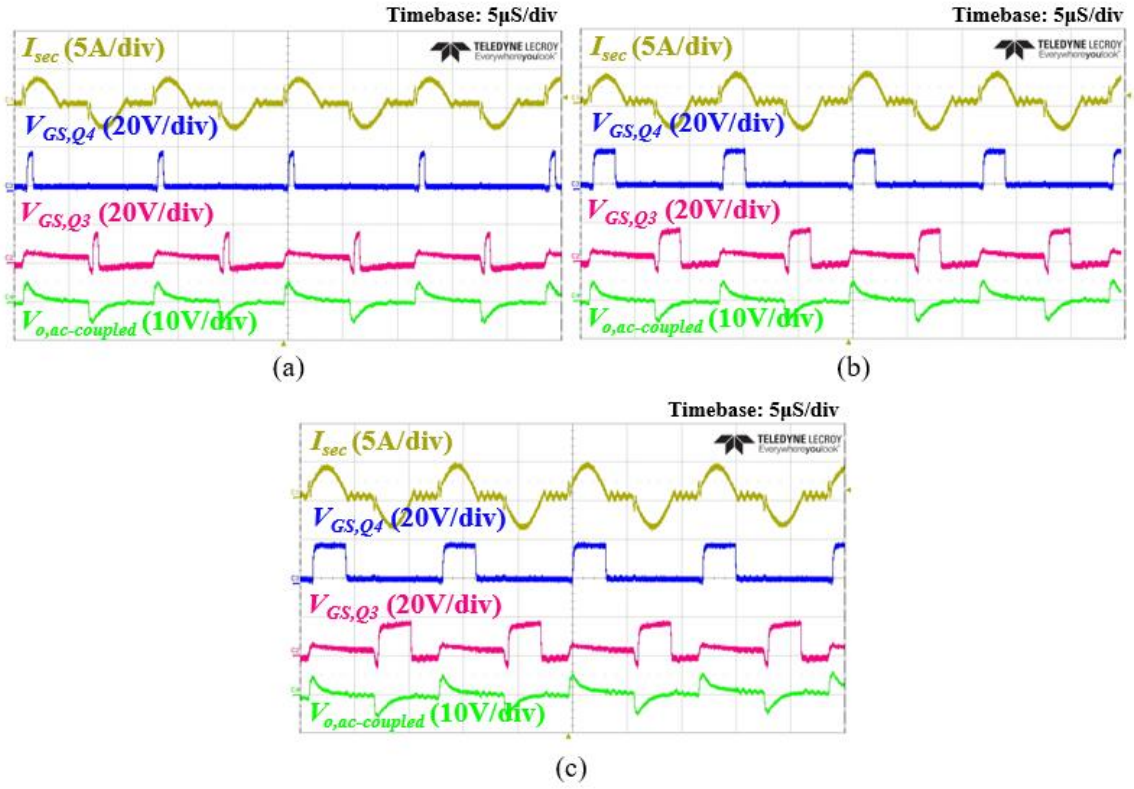

Fig. 3.19. Time-domain SR waveforms under duty rate limiting initiating from (a) start of duty step input (b) middle of rate limiting (c) under steady-state operation.

TABLE 3.1
LLC-DCX POWER STAGE PARAMETERS

Component	Parameter
Input Voltage	600-V
Output Voltage	340-V
Max Load	2.5 kW
Resonant Inductance (L_r)	11.2 µH
Resonant Capacitance (C_r)	0.30 µF
Magnetizing Inductance (L_m)	760 µH
Dead Time (T_d)	375 nS
XFMR Ratio (n_{pri}:n_{sec})	21:12
Switching Frequency (f_s)	84 kHz
Primary Switch	C2M0080120D

TABLE 3.2
SYNCHRONOUS RECTIFIER PARAMETERS

Component	Parameter
SR Switch	Rohm SCT3017
SR Controller	TI UCC24610
$R_{g(on,off)}$	4.7 Ω
$C_{doubler}(C_1,C_2)$	6.6 μF
C_{bus}	6.12 μF

3.4 Summary

In this section, a novel current oscillation issue is discovered, root-caused, and finally analyzed. This oscillation can output ripples, high EMI, and unwanted light load oscillations – limiting SR applicability in wide load range applications. The oscillation is a result of a changing rectification voltage drop, which can induce the oscillation effect when combining an *LLC* converter with SR. This section analyzes the issue, develops four operating models of the *LLC* converter with SR, and finally proposes a revised SR algorithm with duty cycle rate limiting. Here, the custom rate limiter is shown to condition SR controller's original output signals to remove the current oscillation issue. The rate limited SR controller allowed for consistent light load SR operation across previously oscillating test conditions.

Chapter 4

Early Turn-Off Issue

4.1 General Description

This section gives a deeper look into the early SR turn-off issue previously mentioned throughout the section. This is the final key area of improvement necessary to bulletproof the drain-source SR method for both stability and efficiency. As mentioned in Chapter 3, maximizing SR operation and minimizing parallel diode conduction is key for stability. Likewise, this is necessary for high rectifier efficiency.

Drain-source SR suffers from one main pitfall – decreased sensing accuracy from parasitic inductance present within the sensing loop. The parasitic inductance can be traced to the controller package, lead inductance, internal wire bonds, and PCB layout. This is shown below in Fig. 4.1, where the parasitic inductance is denoted as L_p. The inductance causes a phase shift in the sensed drain-source voltage, which results in the SR controller turning the SR switch off early. This increases the parallel diode losses, since SR ends earlier than expected. Currently, methods to fix this issue are overly complex and require end user tuning to optimize. These methods can involve adding additional external inductance [33], complex DSP digital controllers [45], or even additional switches [47]-[50]. These methods are therefore overly complex and difficult to scale in industry, especially for mass-produced systems where the inductance may vary across board spins.

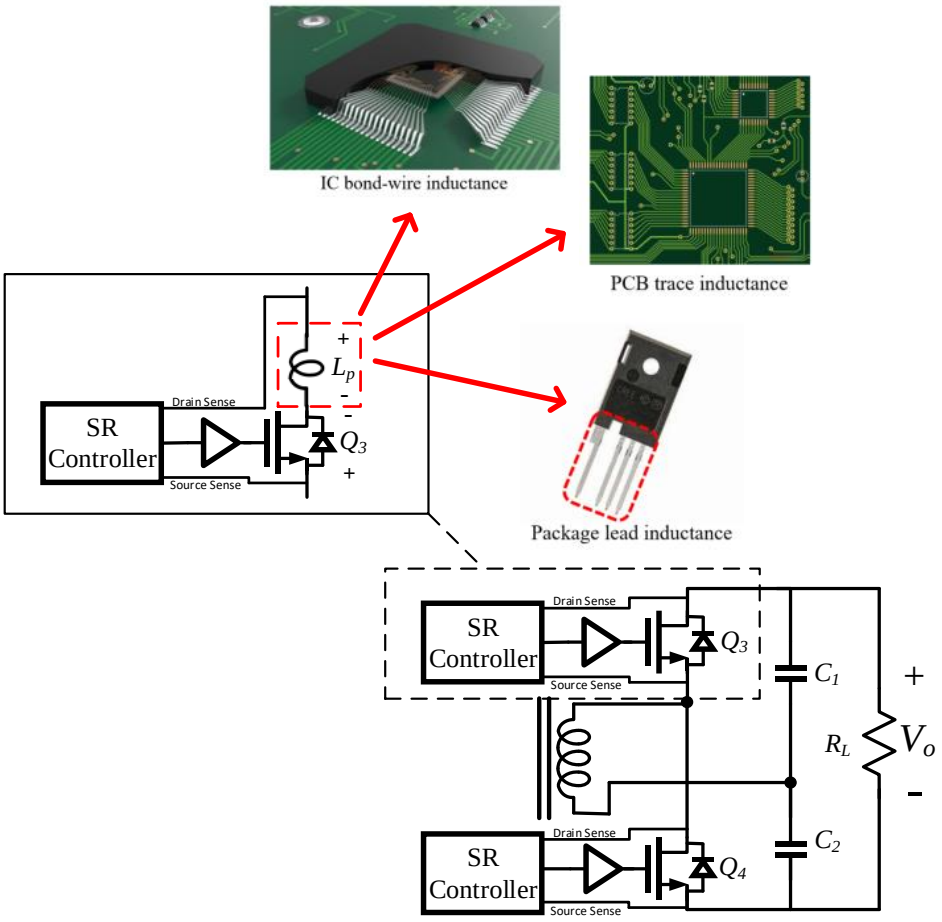

Fig. 4.1. Drain-source parasitic inductance L_p within sensing loop.

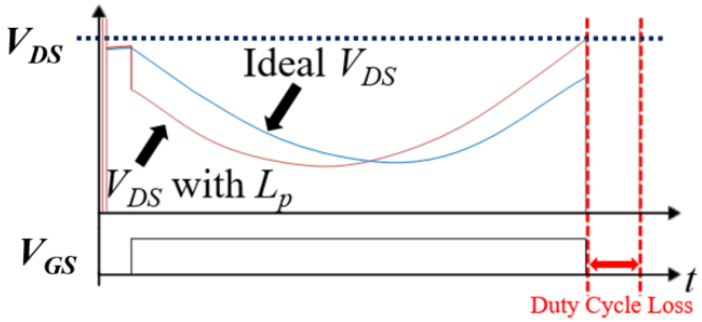

Fig. 4.2. V_{DS} phase shift effect from parasitic inductance L_p and resulting duty cycle loss.

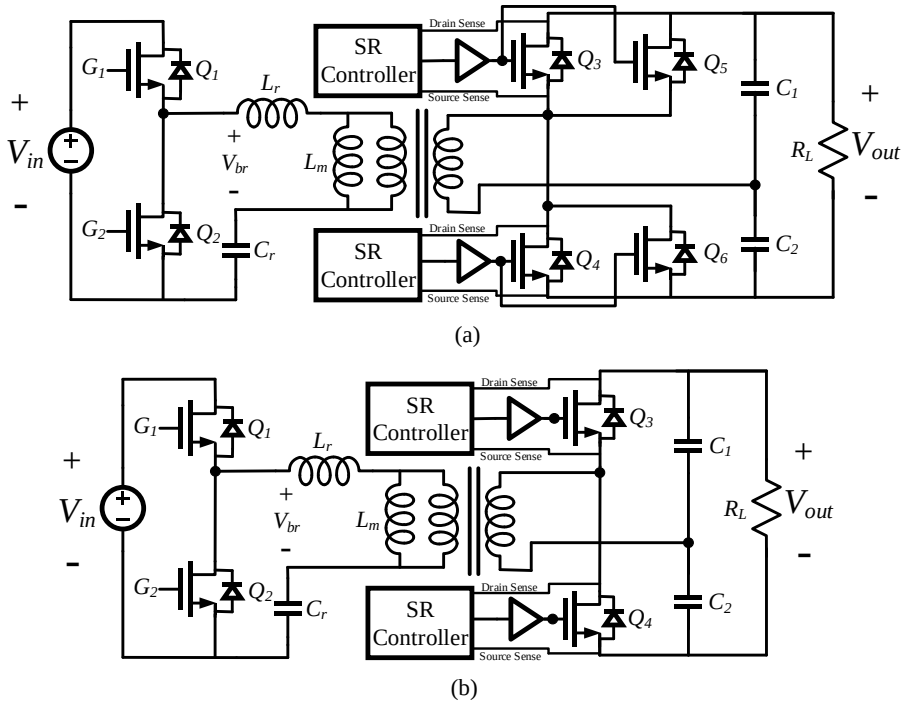

Fig. 4.3. *LLC*-DCX with (a) parallel switch rectifier (b) single switch rectifier.

This section focuses on developing a much simpler solution for two different rectifier topologies: (1) parallel switch rectifiers; (2) single switch rectifiers. Paralleled switch rectifiers are found in high current applications, where switches are commonly paralleled to reduce rectification loss and bolster a rectifier's current flow capabilities [51]-[52]. Fig. 4.3 (a) depicts a parallel switch rectifier with two paralleled switches on both the high and low sides of the doubler rectifier. Fig. 4.3 (b) shows a traditional single switch voltage doubler rectifier.

The parasitic inductance L_p adds a negative 90 degrees of reactive impedance that must be accounted for. This inductance results in the impedance triangle in the sensing loop shown by Fig. 4.4. Therefore, the approximate phase shift relative to the original signal, θ, is a simple trigonometric derivation based on the impedance triangle, (4.1).

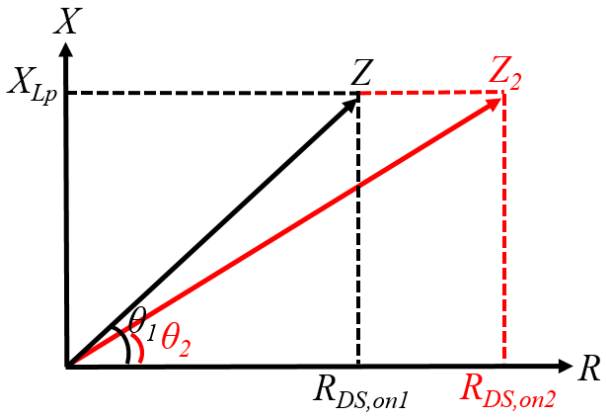

Fig. 4.4. Impedance triangle of phase shift effect with different $R_{DS,on}$ values.

$$\theta = \tan^{-1}\left(X_{Lp} \Big/ R_{DS,on} \right) \tag{4.1}$$

X_{Lp} is the reactance of the L_p, where $Xc_{Lp} = 2\pi f L_p$ where f, the frequency, is the converter switching frequency. The impedance magnitude, Z, must account for L_p, depicted in (4.2). This results in an increase in impedance magnitude, which increases the V_{DS} magnitude and decreases the phase shift angle θ.

$$Z = \sqrt{R_{DS,on}{}^2 + X_{Lp}{}^2} \tag{4.2}$$

(3.13) can then be combined with (4.1) and (4.2) to produce (4.3) [45]-[48].

$$V_{DS}(t) = -I_{\text{sec},pk} \sin\left[2\pi f_s t + \tan^{-1}\left(\frac{2\pi f_s L_p}{R_{DS,on}} \right) \right] \left| R_{DS,on} + j2\pi f_s L_p \right| \tag{4.3}$$

As shown in Fig. 4,4, the phase shift magnitude is related to the ratio of L_p and $R_{DS,on}$. Therefore, larger device packages typically have larger parasitics and worse early turn-off issues than smaller device packages. However, a higher $R_{DS,on}$ switch reduces the phase shift effect compared to lower $R_{DS,on}$ switch for the same given L_p. Given this fact, it

is tempting to choose a higher $R_{DS,on}$ switch to reduce the phase shift effect. However, higher $R_{DS,on}$ is not desirable for the full SR period – only near the end to boost the signal. This is the fundamental theory in which the following solution proposals are based on.

Since an increase in $R_{DS,on}$ is only desirable right before the normal turn-off moment, this can be achieved by sequential parallel switching (SPS) for parallel switch rectifiers, and adaptive multilevel gate driving (MLGD) for single switch rectifiers. The following sections explain the working principles behind SPS and adaptive multilevel gate driving. Analysis is performed for both methods, and subsequently validated at the board level on an *LLC*-DCX converter.

4.2 Sequential Parallel Switching

Sequential parallel switching (SPS) extends SR conduction by turning the parallel switches off sequentially rather than in batch. Here, batch mode is defined as switching all paralleled switches in parallel. By sequentially turning each switch off, the net rectification path $R_{DS,on}$ in increased in discrete steps. Fig. 4.5 shows key SPS waveforms for a two-parallel switch synchronous rectifier. I_{sec} is the secondary side transformer current, $V_{DS,turnoff}$ the SR controller turn-off voltage threshold, V_{DS} the phase shifted and actual drain-source voltage of the SR switches, and V_{GS} the gate-source voltage of the respective SR switches.

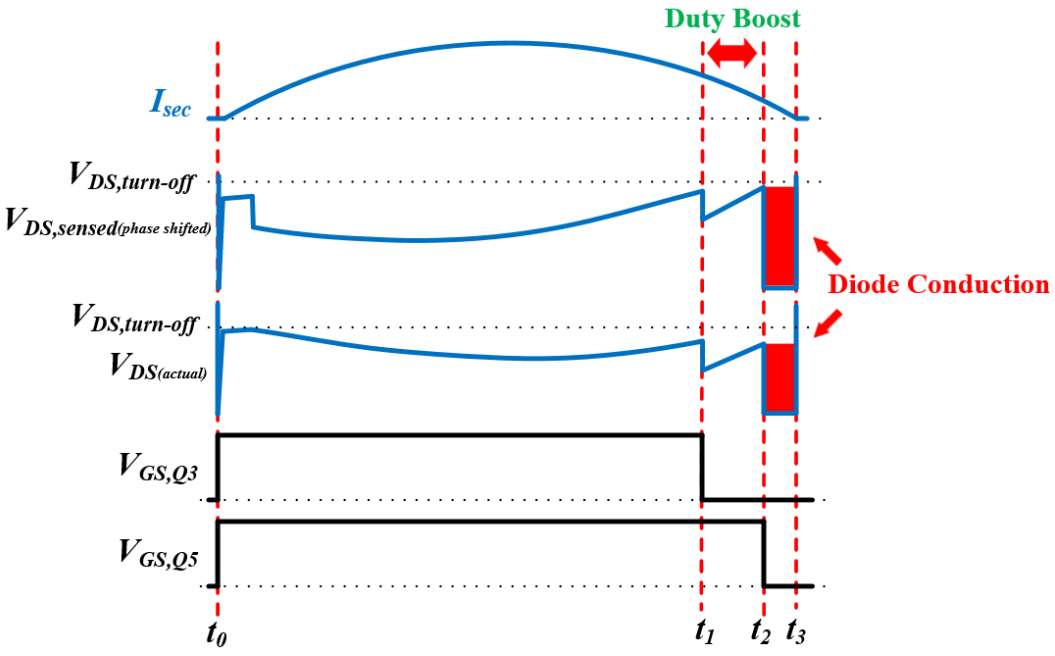

Fig. 4.5. Key sequential parallel switching (SPS) waveforms for duty cycle boost.

At time t_0, all paralleled switches (Q_3, Q_5) are turned on at the same time. At some time near the turn-off moment, t_1, one of the SR switches shuts off while the other remains on. This boosts the $V_{DS(actual)}$ signal magnitude, and decreases the phase shift as seen in $V_{DS,sensed(phase\ shifted)}$. Once the sensed V_{DS} drops to the turn-off threshold, t_2, the remaining switch is turned off. Any remaining current left to be rectified will go through the parallel diode, up until the end of the cycle t_3. The increase in duty cycle is the delta between t_1 and t_2, since t_1 is where the SR controller would normally turn-off if the switches were operated in batch mode.

While a two-parallel switch rectifier is shown here, multiple switches can be further paralleled to lessen conduction losses and bolster current capability. Therefore, the number of possible turn-off steps increases with the number of paralleled switches. With each additional step, the SR conduction period can be pushed closer to the ideal I_{sec} zero crossing

moment. While the channel conduction loss is increased marginally from the $R_{DS,on}$ increase, the increase in efficiency from the decrease in parallel diode conduction vastly outweighs this near the end of the SR cycle. SPS can thus greatly increase rectifier and converter efficiency when (4.4) is satisfied, where $R_{DS,on2}$ is the rectifier channel resistance at the point of interest.

$$\int {I_{DS}}^2(t)R_{DS,on2}dt < \int V_F I_{DS}(t)dt \tag{4.4}$$

Next, the total energy dissipated within one half of resonant cycle for a paralleled two switch SPS rectifier case is shown, (4.5).

$$E_{cond} = \int_{t_0}^{t_1} {I_{DS}}^2(t)R_{DS,on1}dt + \int_{t_1}^{t_2} {I_{DS}}^2(t)R_{DS,on2}dt + \int_{t_2}^{t_3} V_F I_{DS}(t)dt \tag{4.5}$$

Where V_F is the parallel diode forward voltage drop, $R_{DS,on1}$ the paralleled SR switch channel resistance, and $R_{DS,on2}$ the channel resistance with one SR switch on. For a two parallel switch rectifier, $R_{DS,on2} = 2*R_{DS,on1}$. With this, (4.5) can be expanded into (4.6) for the total conduction loss, which extrapolates to an M-switch rectifier where $M>2$.

$$E_{cond} = \int_{t_0}^{t_1} \frac{{I_{DS}}^2(t)R_{DS,on}}{n}dt + \int_{t_1}^{t_2} {I_{DS}}^2(t)R_{DS,on}dt + \int_{t_2}^{t_3} V_F I_{DS}(t)dt \tag{4.6}$$

4.2.1 Methods of Emulation

The SPS method is designed to be integrated into an integrated chip (IC). This is a simple architecture change, as it only requires at a minimum M-number of gate drivers and turn-off thresholds. The voltage delta between the turn-off thresholds needs to be minimized to maximize efficiency, but not minimized to such an extent that noise corrupts the sensed signal and results in erroneous batch turn-off. The turn-off thresholds can dictated at the IC level, or by the end user with adjustable sense-path resistors. The latter

is most practical, since each application has different needs. This method of implementation would therefore necessitate an *M*-number of drain sense pins for the IC.

With currently available SR controllers, there are two methods of emulating SPS at the board level: (1) minimum on time; (2) shifted turn-off thresholds. With minimum on time, there is a separate SR controller for each SR switch. The SR controller must have a minimum on time control, which will turn on the SR switch for a minimum set period as set by the end user. The minimum on time for one switch would be set slightly longer than the conduction time for the other switch. For example based on Fig. 4.5, the minimum on time of Q_5 would be set slightly greater than the t_1-t_0 period to blank the Q_5 SR controller from the Q_3 SR controller's turn-off moment. However, this method has the pitfall of only working correctly for a narrow load range. Nevertheless, it is usable to validate the concept of SPS.

The second method, with shifted turn-off thresholds, is far more robust. However, this method is only applicable to controllers that use a current injection voltage sense, such as the On Semi NCP4303 and NCP4304 [33]-[34]. A controller is again required for each SR switch, with a resistor R_{shift} in the drain sense path to shift the turn-off threshold, shown in Fig. 4.6. The R_{shift} value is calculated based on the same factors previously described for choosing different turn-off threshold voltages.

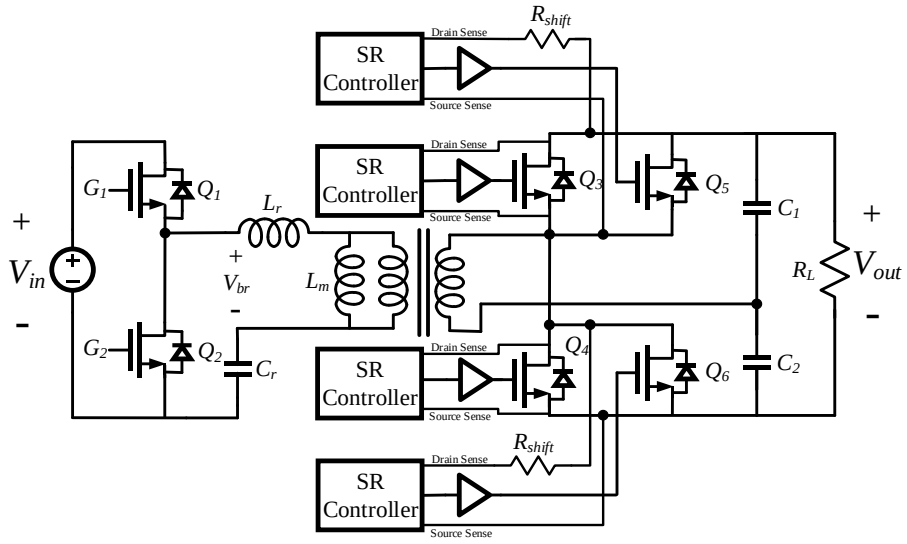

Fig. 4.6. *LLC*-DCX with a two parallel switch SR implemented with SPS and turn-off threshold shifting with $R_{shift.}$

4.2.2 Bench Validation

For verification, the duty cycle across load is measured extracted from an SR controller through bench testing and emulated with a FPGA to measure the efficiency gain. Fig. 4.7 depicts the bench test setup and custom SPS SR board consisting of paralleled Rohm SCT3017 SiC MOSFETs (x2) for the SR switches and a TI UCC24610 SR controller for the low and high-sides. The *LLC*-DCX module specifications used for verification is shown below in Table 4.1, and the SPS SR board specifications are listed in Table 4.2. Slightly different input conditions were run for a re-dated application utilizing the same power stage module.

The test waveforms at 180-W, 430-W, and 1-kW are captured below in Fig. 4.8 (a)-(c), respectively. $V_{GS,Q5}$ turns off before $V_{GS,Q3}$, reducing the signal phase shift and boosting the total SR conduction time. The efficiency of the converter is measured and plotted to compare batch turn-off and SPS turn-off in Fig. 4.9. As shown in the graph, there is an

efficiency increase throughout the power range, with maximum gains between light and medium load of over 0.5% total system efficiency increase.

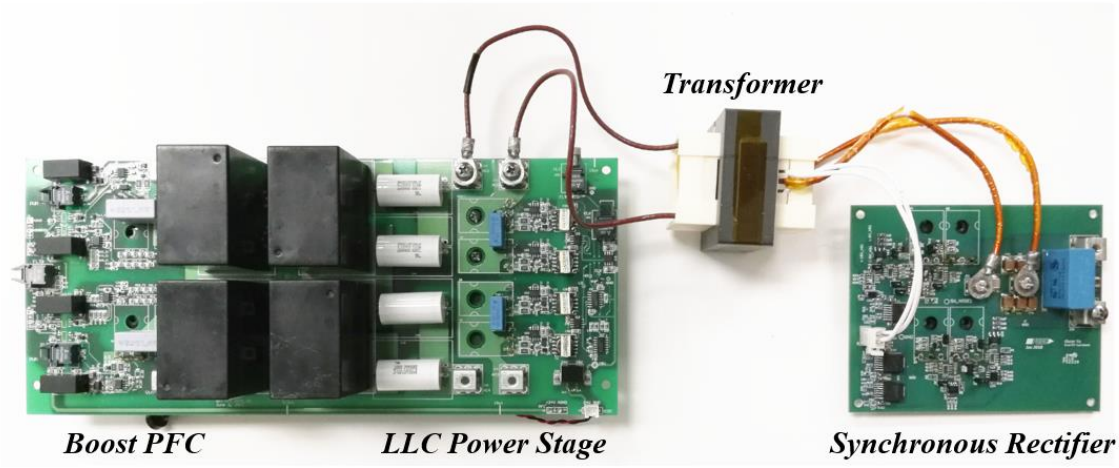

Fig. 4.7. Bench setup of *LLC*-DCX power stage module (left), transformer (center), and SPS SR board (right).

TABLE 4.1
LLC-DCX RESONANT CONVERTER PARAMETERS

Component	Parameter
Input Voltage (V_{in})	300-V
Output Voltage (V_o)	170-V
Resonant Inductance (L_r)	11.2 µH
Resonant Capacitance (C_r)	0.30 µF
Magnetizing Inductance (L_m)	760 µH
XFMR Ratio (n_{pri}:n_{sec})	21:12
Switching Frequency (f_s)	84 kHz
Primary Switch	C2M0080120D

TABLE 4.2
SPS RECTIFIER BOARD PARAMETERS

Component	Parameter
SR Switch	Paralleled (2x) Rohm SCT3017
SR Controller	TI UCC24610
Gate Driver	TI UCC27531
$R_{g(on,off)}$	4.7 Ω
$C_{doubler}$	6.6 µF
C_{bus}	6.12 µF

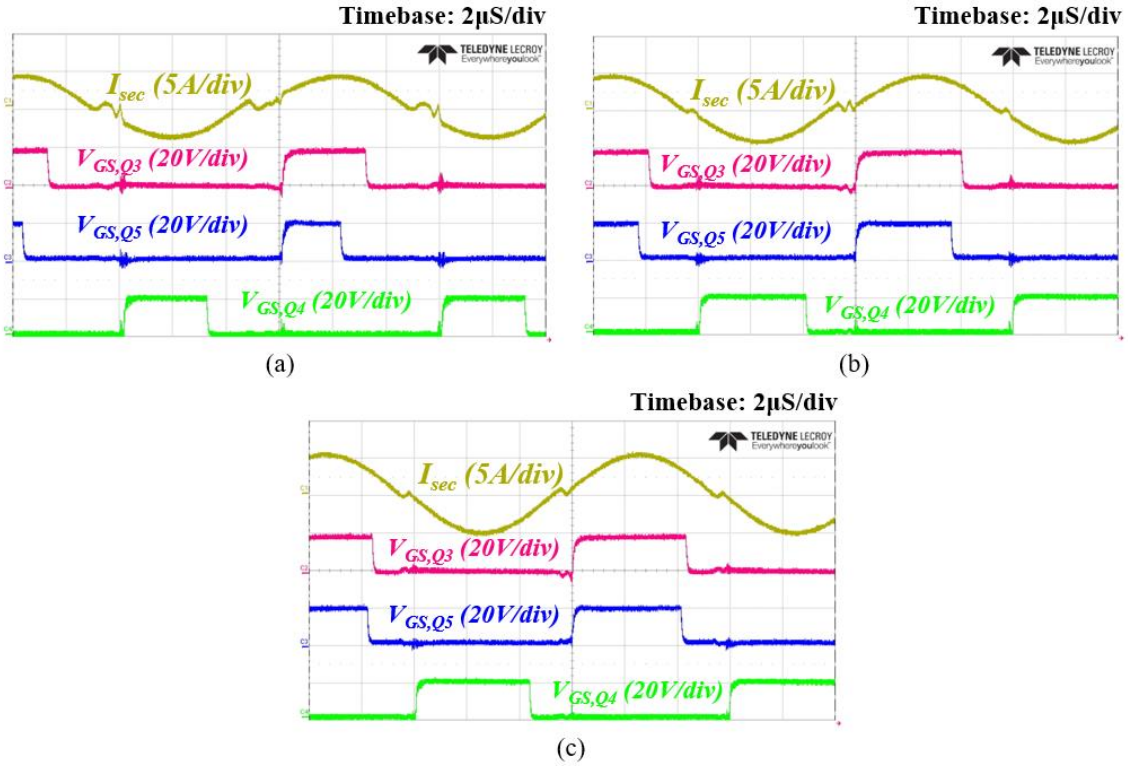

Fig. 4.8. Time-domain SPS waveforms at (a) light load (180-W) (b) medium load (430-W) (c) heavy load (1-kW).

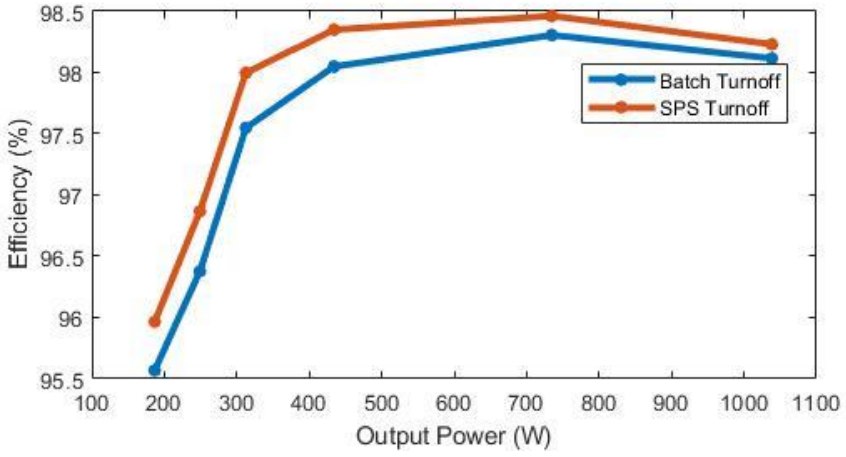

Fig. 4.9. SPS efficiency gain comparison on *LLC*-DCX.

Since the phase shift is a function of L_p and $R_{DS,on}$, the latter is a known value, the L_p can be calculated based on the turn-off moment $R_{DS,on}$ value. The test setup results in a paralleled switch $R_{DS,on}$ of 8.5mΩ, and 17mΩ with one switch on. By measuring the time

difference between the switch-off moment and the zero current moment, the V_{DS} phase shift angle can be calculated through (4.1). Here, the time difference at medium load with both switches on (8.5mΩ) is measured at 1.4μS, which corresponds to a 43^{o} phase shift angle. With one switch on (17mΩ), a time difference of 850nS is measured, or a phase shift of 25.7^{o}. From here, the parasitic inductance can be calculated using a system of equations and the two initial conditions, resulting in an L_p of 15.5 nH. This value is similar to other parasitics measurements with TO-247 devices [53]-[54], validating the equations and analysis.

4.3 Multilevel Gate Driving

For single switch rectifiers, adaptive multilevel gate drivers can be used to extend SR conduction time. As explained previously, an increase in SR switch $R_{DS,on}$ results in a boost of V_{DS} signal magnitude and phase shift error reduction. To achieve this with a single switch, the gate voltage of the switch can be reduced near the SR switch turn-off moment to increase the $R_{DS,on}$. This can also be combined with an adaptive gate driver to tune the optimal moment to reduce gate voltage, maximizing steady state efficiency. Similarly to SPS, the end goal is to integrate this technology at the IC level.

Key MLGD waveforms are shown below in Fig. 4.10. V_{DD1} and V_{DD2} depict the two separate gate drive sources, the sum of which is the full gate drive voltage (V_{DD1} + V_{DD2}). V_{GS} and V_{DS} are the gate and drain voltage with respect to source, respectively, $V_{DS,turn\text{-}off}$ the turn-off voltage, and I_{sec} the secondary side transformer current. t_{SR1} and t_{SR2} each represent the SR conduction time for a given drive voltage, and t_{diode} the parallel diode conduction time. The transition duty cycle, D_t, is defined as the duty cycle from t_0 to t_1, and

can be calculated by D_t = 100((t_1-t_0)/t_{sw}), where t_{sw} is the switching period (1/f_s). t_0 represents the turn-on moment for SR, t_1 the multilevel gate driver transition moment, t_2 the SR controller turn-off moment, and t_3 the end of the SR cycle.

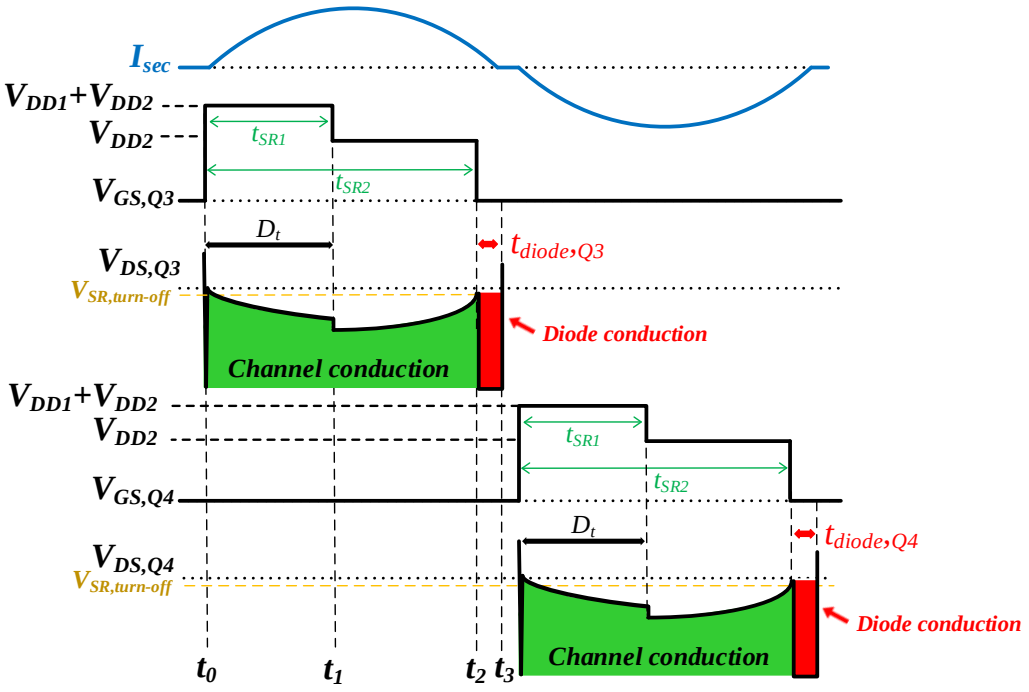

Fig. 4.10. Key multilevel gate driver waveforms.

The multilevel transition moment is critical for overall efficiency and needs to be optimized to minimize channel conduction loss. The optimization is achievable by timing the switching moment at the full drive voltage condition (V_{DD1}+V_{DD2}) to low voltage condition (V_{DD2}) as close as possible to the turn-off moment. The amount of efficiency improvement is wholly dependent on multiple factors: (1) the parallel diode voltage drop; (2) the secondary side current; (3) SR switch characteristics. Generally speaking, an efficiency boost is found when (4.7) is satisfied.

$$R_{DS,on} I^2_{DS} < V_F I_{DS} \tag{4.7}$$

$R_{DS,on}$ is the SR switch channel resistance at a given moment in time, I_{DS} the drain-source current through the switch, V_F the parallel diode drop. While switching t_1 too early is detrimental to efficiency, t_1 generally occurs near t_2, the end of the SR cycle, so (4.9) is typically satisfied. Adaptations of (4.6) from SPS analysis can be used for further analysis of the losses during multilevel gate driving, since the underlying theory of operation remains the same. Here, the major determining factors are the transition duty cycle (D_t) and the $R_{DS,on2}$ at V_{DD2}. A larger $R_{DS,on2}$ results in a longer SR conduction time as shown by (4.3). However, the increase in $R_{DS,on}$ must be weighed against the increase in channel conduction loss and achievable transition moment.

The question remains as to how the second gate drive voltage, V_{DD2}, is determined. A drop in gate voltage comes with an increase in $R_{DS,on}$ as shown by the typical output characteristics graph for a MOSFET (I_D vs V_{DS}), where I_D is the MOSFET drain current and V_{DS} is the drain-source voltage [55]. The gate voltage can be determined analytically with this graph to maximize SR conduction. First, the desired efficiency of the rectifier must be determined to determine the minimum SR conduction period necessary through loss analysis. Then, the desired V_{DD2}-level $R_{DS,on}$ can be derived by setting V_{DS} to $V_{DS,turnoff}$ in (4.3) and the $R_{DS,on}$ value solved for.

If the output characteristics graph is not available, the gate drive voltage can be calculated through the MOSFET drain-source current equation (4.8). (4.8) represents the drain-source current of a MOSFET in the linear region [56]. I_{DS} is the drain-source current of the MOSFET, μ_n the carrier mobility, C_{ox} the oxide capacitance per unit area, W/L the gate width to gate length ratio, V_t the threshold voltage, and λ the channel-length

modulation parameter. Through the combination of (4.8) and (4.9), the necessary V_{GS} can be extracted to determine the V_{DD2} for desired SR performance. Here, the limiting factor for the V_{DD2} voltage with bench test setup's MLGD is the under-voltage lockout limit of the gate driver chip. The proposed method is anticipated to be integrated into a commercial IC to eliminate this limitation in application.

$$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left[(V_{GS} - V_t)V_{DS} - \frac{V^2{}_{DS}}{2}\right](1 + \lambda V_{DS}) \tag{4.8}$$

$$R_{DS} = \frac{V_{DS}}{I_D} \tag{4.9}$$

4.3.1 Adaptive Gate Driver Design

A digitally adaptive MLGD is developed to mitigate the effects of parasitic inductance in the drain-source sense path. In industry, multilevel gate drivers do not offer any solutions for digital control or analog tuning. The purpose of commercial MLGD chips is to limit turn-off overvoltage in cases of short circuit conditions or overcurrent [59]-[60]. Furthermore, recent MLGD research has solely been focused only on driving wide band-gap devices for applications other than SR [61]-[63]. Therefore, it was opted to design a completely custom MLGD solution, including an adaptive delay block, to maximize flexibility in research and optimization. The method aims to piggyback onto existing drain-source SR controllers through digital tuning.

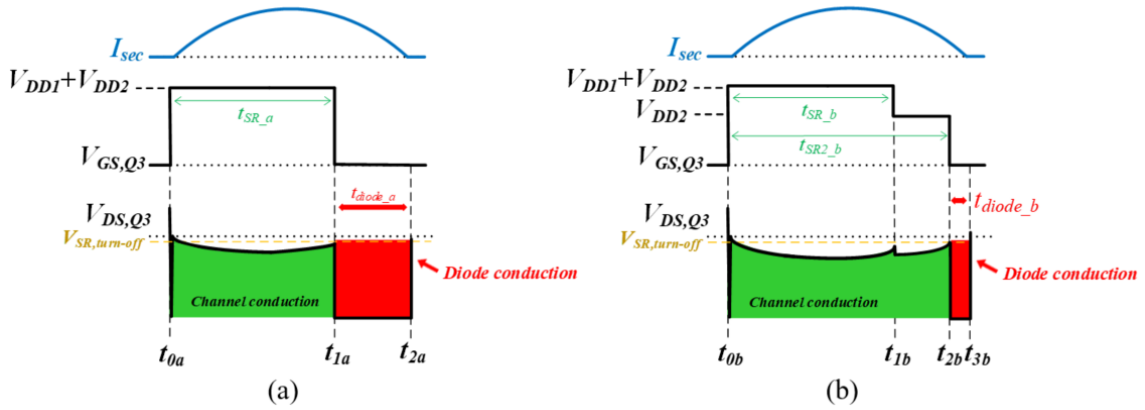

Fig. 4.11. Multilevel gate driver waveforms during (a) initial single-level driving (b) ideal multilevel-gate driving.

The transition duty cycle can be actively tuned in steady state with a digital controller. The SR controller determines the turn-on (t_0) and final turn-off (t_2) moments, and the adaptive delay block the transition point (t_1). In order to do this, a tuning mechanism can be used that will find the optimal t_1 moment, which is close to t_2. This is achieved by post-processing the gate driver signals with an FPGA, which acts as a digitally adaptive delay by determining when to switch the multilevel gate driver based on a variety of conditions.

First, the adaptive delay algorithm will observe the full gate drive voltage ($V_{DD1}+V_{DD2}$) SR conduction period as shown in Fig. 4.11 (a). The t_{1a} moment represents the latest moment where the multilevel gate driver can reduce the gate voltage without triggering the SR controller turn-off moment. In Fig. 4.11 (b), we see the two-level gate driver in action, with transition moment at t_{1b}. Therefore, the goal of the adaptive delay is to move t_{1a} as close to t_{1b} as possible, without triggering an early turn-off of the SR

controller. The flow diagram of the SR controller, FPGA, and signal isolators is shown below in Fig. 4.12.

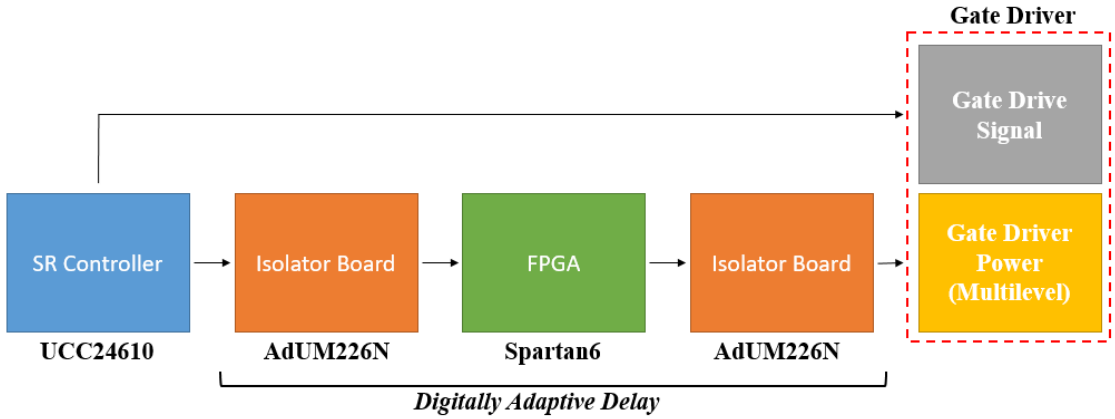

Fig. 4.12. Block flow diagram of adaptive multilevel gate driver consisting of FPGA, SR controller, signal isolators, and gate driver circuit.

The SR controller feeds these gating signals through digital signal isolators to the FPGA, a Xilinx Spartan 6. The FPGA measures the SR conduction period, t_0 to t_2, at the full V_{DD1}+V_{DD2} voltage. Measurements are achieved with digital counters in the FPGA, run by the global clock. Internal counters in the FPGA measure time in discrete time, which can be calculated based on the global clock frequency, f_{clk}, through (4.10). f_{clk} represents the clock frequency of the counter block, with $counter_{redge}$ (t_0) and $counter_{fedge}$ (t_2) the captured counter values of the SR duty cycle rising and falling edges, respectively.

$$t = \frac{counter_{redge} - counter_{fedge}}{f_{clk}} \tag{4.10}$$

The most important step in determining the t_1 switching moment is t_{blank}, the amount of blanking time needed for consistent SR operation. SR turn-off moments have a varying jitter, even in steady state operation due to noise and resulting sensing discrepancies. t_{blank} can be determined based on the magnitude of drain-source noise within the sensed V_{DS}

signal. As previously discussed in (3.14), noise emulates a shift in the SR controller turn-off threshold, (4.11). Noise measurements can be performed on the circuit to determine V_n, and the resulting tblank by solving for the minimum blanking duty cycle necessary. From here, the t_1 switching moment can be calculated by subtracting t_{blank} from t_2.

$$V_{DS}(t) \pm V_n = -I_{\sec,pk} \sin\left[2\pi f_s t + \tan^{-1}\left(\frac{2\pi f_s L_p}{R_{DS,on}}\right)\right] \left| R_{DS,on} + j2\pi f_s L_p \right| \tag{4.11}$$

In order to retain maximum tuning flexibility, the MLGD is built using two isolated power supplies (V_{DD1}, V_{DD2}) fed into a half-bridge, which powers a Texas Instruments UCC27531 gate driver. Fig. 4.13 shows the circuit block diagram and its interface with the FPGA and SR controllers.

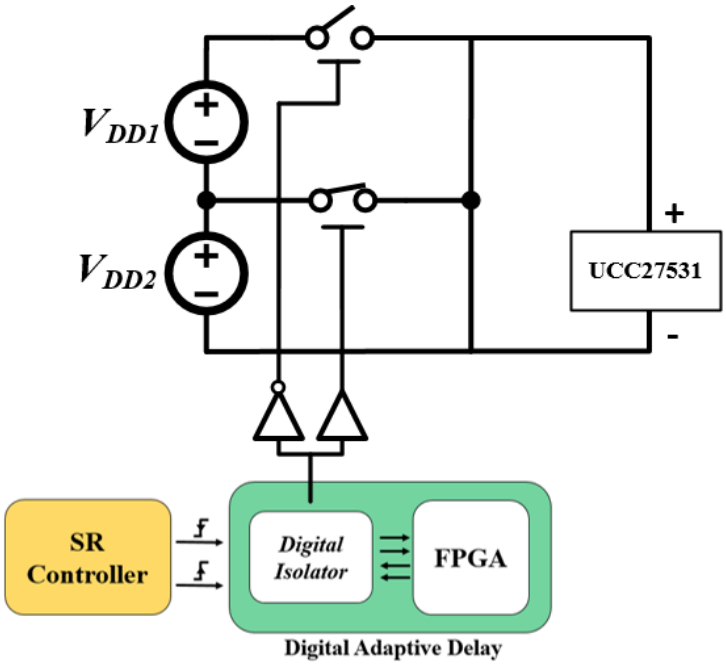

Fig. 4.13. Multilevel gate driver circuit.

4.3.2 Bench Validation

First, comprehensive gate driver simulations were built in LTSPICE to quantify the effect of the transition duty cycle. The SPICE model for the SR switch used in the MLGD SR board during bench test is used in simulation. Likewise, the same test conditions were emulated – a very light load condition of 40W. The result is shown in Fig. 4.14, validating the importance of maximizing the transition duty cycle to minimize conduction loss. Next, adaptive multilevel-gate driving is verified on the bench. A custom MLGD SR board is designed with the specifications listed in Table 4.3, and the test waveforms shown in Fig. 4.15. I_{sec} is the secondary side current, V_{GS} the gate source voltage of the SR switch driven by the MLGD, and V_{SR} the output of the SR controller.

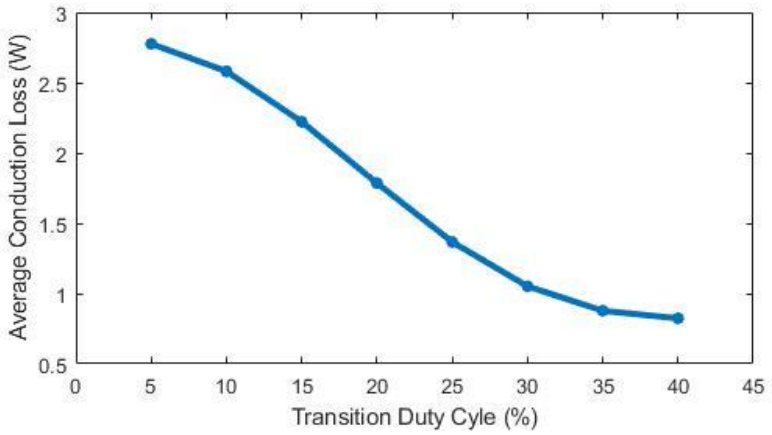

Fig. 4.14. Multilevel gate driver transition duty cycle conduction loss effect.

TABLE 4.3
MLGD SR BOARD PARAMETERS

Component	Parameter
SR Switch	Rohm SCT3017
SR Controller	TI UCC24610
Gate Driver	TI UCC27531
V_{DD1}	18-V
V_{DD2}	10-V
$R_{g(on,off)}$	4.7 Ω
$C_{doubler}$	6.6 µF
C_{bus}	6.12 µF
FPGA	Xilinx Spartan 6
Signal Isolator	Analog Devices AdUM226N

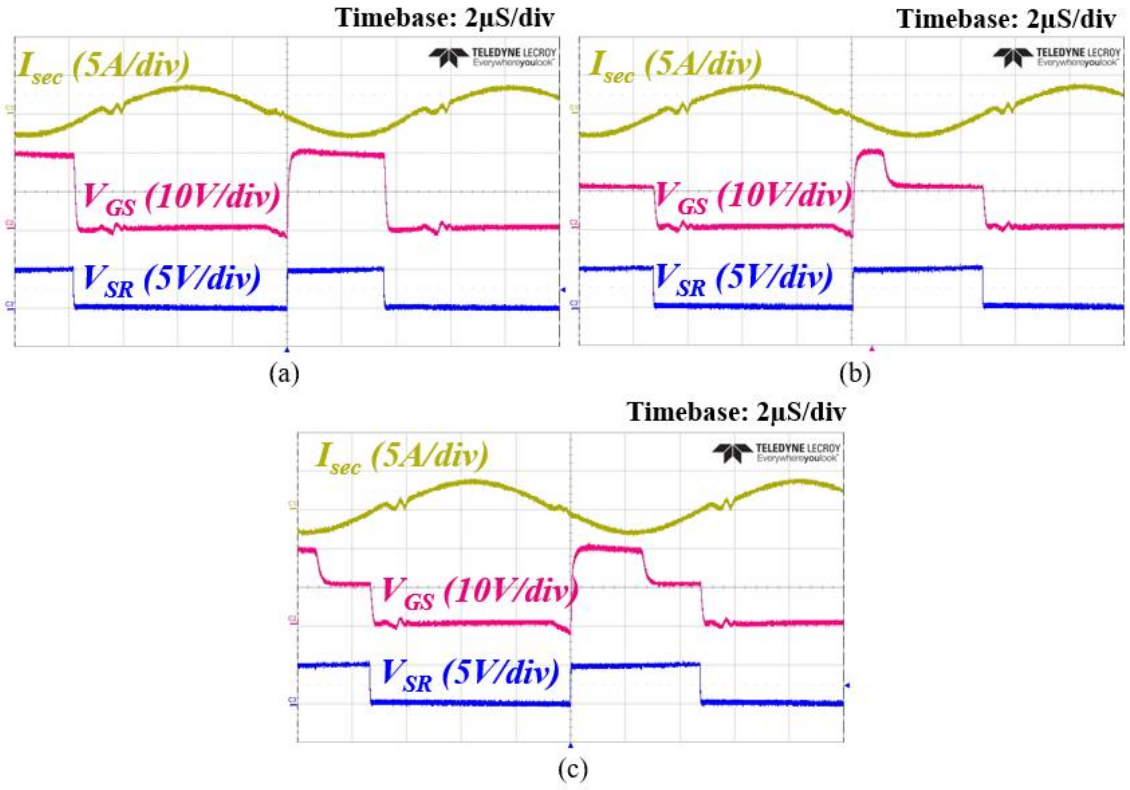

Fig. 4.15. Time-domain MLGD SR waveforms: (a) before MLGD (b) unoptimized MLGD transition moment (c) transition tuning near completion.

In order to quantify the gains of the MLGD, a comprehensive SPICE model of the converter and MLGD is created. With a 40W load condition, the SR's duty cycle is extended from the minimum measurement of 29% to a steady 43% with a 12.5% transition duty cycle, resulting in a 57% loss reduction (from 3.81W to 2.24W) in one SR cycle. When increasing the transition duty cycle from around 12.5% to 40%, conduction loss can be further reduced by a remarkable 66%. Therefore, an adaptive multilevel gate driver is incredibly helpful in reducing losses. In conclusion, two main benefits can be realized with an MLGD on a single switch SR: (1) SR duty extension and minimization of parallel diode conduction losses, and (2) an increase in drain-source signal strength near the turn-off moment to increase turn-off consistency.

4.4 Summary

In this section, two proposed methods of alleviating early turn-off are presented: sequential parallel switching (SPS) and adaptive multilevel gate driving. Each method is intended for a specific rectifier topology, either single or parallel switch. Both methods are also very simple to implement and integrate onto an IC to mitigate the early turn-off issue experienced by drain-source sensed SR from parasitic inductance. A phase shift results from this parasitic, which increases parallel-body diode conduction losses, decreasing rectifier efficiency and thus converter efficiency. Detailed analysis and design criteria are proposed for both methods, which are then validated at the board level on an *LLC*-DCX power converter. Both methods are successfully shown to greatly extend SR conduction time and boost efficiency across load.

Chapter 5

Conclusion and Future Work

5.1 Conclusion

In this dissertation, three issues regarding the traditional drain-source synchronous rectification (SR) method are identified: (1) high voltage sensing; (2) light load operation; (3) sensing accuracy. Each of these have posed an impediment to the widespread use of SR in high voltage, low current power converters. Therefore, this dissertation proposed a solution to each of the problems.

First, a self-biasing high voltage clamp was proposed in Chapter 2 to protect the SR controller from damage during high voltage operation. Furthermore, design equations were proposed and verified which allowed for accurate estimations of voltage across the SR controller. The equations and method were then verified on the bench to over 1-*kV* - a world first in SR.

Next, potential issues regarding light load operation were identified and analyzed. Since SR has traditionally only been utilized in high current rectifiers, low current rectifiers pose a new challenge – low SNR. With a low signal magnitude, the SR controller is at risk of exciting the resonant tank in ways that cause oscillations or overshoots. Analysis and simulations were performed to replicate and understand the issue, and SR architecture changes are proposed. Currently, no SR controller is able to limit this issue, so a method coined duty cycle rate limiting is proposed and tested on the bench to eliminate light load

oscillations. The method is shown to control the SR system better than before in poor SNR conditions.

Finally, two methods are proposed to improve sensing accuracy in drain-source SR: (1) sequential parallel switching; (2) adaptive multilevel gate driving. Sequential parallel switching (SPS) is designed to be used in rectifiers were switches are paralleled, and boosts the $R_{DS,\text{on}}$ of the SR switch path near the turn-off moment to increase V_{DS} SNR and SR duty cycle. SR controller architecture changes are proposed, and the method is validated at the board level to increase rectifier performance. Adaptive multilevel gate driving (MLGD) is proposed for single switch rectifiers, and also boosts the $R_{DS,\text{on}}$ of the SR switch near the turn-off moment to increase the V_{DS} SNR, and thus SR duty cycle. A simple adaptive controller is designed and piggybacked onto the MLGD to tune for an optimal gate driver switch point. This method is also validated at the board level, and simulations are performed to quantify the rectifier efficiency gains.

5.2 Future Work

Research is never ending – and here, this is also the case. With continuing adoption of high voltage low current SR, more developments can be made in specific areas.

(i) Further analysis on the effects of SR on other resonant converters must be performed. Since SR has not been widely adopted on high voltage low current resonant converters, the effects of SR have not been widely discussed or noted until now. This dissertation points out a multitude of issues that have gone ignored during SR implementation, but can no longer be. With higher and high voltages and future adoption of wide band-gap semiconductors, the issues will become more pronounced with time.

(ii) The improvement of SR algorithms must take into account the effects on the resonant converter. Analysis of the effect is one portion of the challenge, but the other half is designing algorithms and controllers that will be universally compatible with resonant converters – especially open loop converters, such as the *LLC*-DCX. These converters will be most susceptible to issues, due to the open loop nature.

(iii) Commercialization of the proposed methods will also be a large issue at the IC level. While the methods proposed are universally useful, resonant converters are still a small subset of the total power converters on the market. Therefore, IC companies will be hesitant to design customized controllers only applicable to these converters due to expensive overhead cost and limited sales revenue. Further research should be performed in developing universal IP that is applicable to the majority of converters, as well as to resonant converters.

REFERENCES

[1] C. Fei, R. Gadelrab, Q. Li and F. C. Lee, "High-Frequency Three-Phase Interleaved LLC Resonant Converter With GaN Devices and Integrated Planar Magnetics," in *IEEE Journal of Emerging and Selected Topics in Power Electronics*, vol. 7, no. 2, pp. 653-663, June 2019.

[2] J. Y. Lee, Y. S. Jeong, and B. M. Han, “An isolated DC/DC converter using high-frequency unregulated LLC resonant converter for fuel cell applications,” *IEEE Trans. Ind. Electron.*, vol. 58, no. 7, pp. 2926–2934, Jul. 2011.

[3] C. Fei, F. C. Lee and Q. Li, "High-Efficiency High-Power-Density LLC Converter With an Integrated Planar Matrix Transformer for High-Output Current Applications," in *IEEE Transactions on Industrial Electronics*, vol. 64, no. 11, pp. 9072-9082, Nov. 2017.

[4] S. Hu, J. Deng, C. Mi and M. Zhang, “LLC resonant converters for PHEV battery chargers,” *in* Proc. Conf. IEEE Appl. Power Electron. Conf. Expo., 2013, pp. 3051-3054.

[5] P. Choi, U. Radhakrishna, C. Boon, D. Antoniadis and L. Peh, "A Fully Integrated Inductor-Based GaN Boost Converter With Self-Generated Switching Signal for Vehicular Applications," in *IEEE Transactions on Power Electronics*, vol. 31, no. 8, pp. 5365-5368.

[6] J. Liu, S. Zhong, J. Zhang, Y. Ai, N. Zhao and J. Yang, "Auxiliary Power Supply for Medium-/High-Voltage and High-Power Solid-State Transformers," in *IEEE Transactions on Power Electronics*, vol. 35, no. 5, pp. 4791-4803.

[7] W. Lee, J. Kim, J. Lee and I. Lee, "Design of an Isolated DC/DC Topology With High Efficiency of Over 97% for EV Fast Chargers," in *IEEE Transactions on Vehicular Technology*, vol. 68, no. 12, pp. 11725-11737.

[8] S. Davis, *GaN and SiC Power Semiconductor Markets Set to Pass $1B Mark in 2021*, Semiconductor Digest, July. 2020. Accessed on: Jan. 5, 2021. [Online]. Available: https://www.semiconductor-digest.com/2020/07/01/gan-and-sic-power-semiconductor-markets-set-to-pass-1b-mark-in-2021/

[9] M. Rashidi, M. Sabbah, A. Bani-Ahmed, A. Nasiri and M. H. Balali, "Design and implementation of a series resonant solid state transformer," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 1282-1287.

[10] J.-S. Lai, J. M. Choe, C. Yeh, S. Moon, W. Lai and L. Zhang, “A modular front-end medium-voltage solid-state transformer,” *in Proc. Conf. Asian Conf. on Energy, Power and Transp. Electrif.*, 2017, pp. 1-6.

[11] J. Choe *et al*., "Controller and EMI filter design for modular front-end sold-state transformer," *2018* IEEE Applied Power Electronics Conference and Exposition (APEC), San Antonio, TX, 2018, pp. 188-192.

[12] J.-S. Lai, W. Lai, S. Moon, L. Zhang and A. Maitra, “A 15-kV class intelligent universal transformer for utility applications,” *in Proc. Conf. IEEE Appl. Power Electron. Conf. Expo., 2016*, pp. 1974-1981.

[13] C.-S. Yeh, L. Zhang, J.-M. Choe, C.-W. Chen, O. Yu, and J.-S. Lai, “Light-load efficiency improvement for LLC converter with synchronous rectification in solid-state transformer application,” in Proc. IEEE Appl. Power Electron. Conf. Expo., 2018, pp. 2142–2147

[14] O. Yu, C. Yeh and J. Lai, "Sequential Parallel Switching for Drain-Source Synchronous Rectifier Efficiency and Light-Load Stability Improvement," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 463-467.

[15] O. Yu, C. Chen, C. Yeh and J. Lai, "Cyclically Adaptive Multilevel Gate Driving for Drain-Source Synchronous Rectifier Efficiency Improvement and Range Extension," *2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, New Orleans, LA, USA, 2020, pp. 1582-1587.

[16] O. Yu, C. Yeh, M. Lee and J. Lai, "Drain-Source Synchronous Rectification Efficiency and Light-Load Stability Improvement through Multi-Level Turn-Off for LLC-based DC-DC Converters," *2019 IEEE Energy Conversion Congress and Exposition (ECCE)*, Baltimore, MD, USA, 2019, pp. 6462-6467.

[17] J. Wang and B. Lu, “Open loop synchronous rectifier driver for LLC resonant converter,” in Proc. 28th Auun. IEEE Appl. Power Electron. Conf. Expo. (APEC), Mar. 2013, pp. 2048–2051.

[18] J. Liao, J. Wang, J. Zhang, and Z. Qian, “A novel current driving scheme for LLC resonant converter with Synchronized voltage-doubler rectifier,” in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, Mar. 2011, pp. 566–570

[19] B. Acker, C. R. Sullivan, and S. R. Sanders, “Current-controlled synchronous rectification,” in *Proc. IEEE Appl. Power Electron. Conf. Expo. (APEC)*, vol. 1, Feb. 1994, pp. 185–191.

[20] J. Zhang, J. Liao, J. Wang, and Z. Qian, “A current-driving synchronous rectifier for an LLC resonant converter with voltage-doubler rectifier structure,” *IEEE Trans. Power Electron.*, vol. 27, no. 4, pp. 1894–1904, Apr. 2012.

[21] X. Zhao, C.-W. Chen, and J.-S. Lai, “A high-efficiency active-boostrectifier-based converter with a novel double-pulse duty cycle modulation for PV to DC microgrid applications,” *IEEE Trans. Power Electron.*, vol. 34, no. 8, pp. 7462–7473, Aug. 2019.

[22] X. Xie, J. C. P. Liu, F. N. K. Poon, and M. H. Pong, “A novel high frequency current-driven synchronous rectifier applicable to most switching topologies,” *IEEE Trans. Power Electron.*, vol. 16, no. 5, pp. 635–648, Sep. 2001.

[23] T. Qian, W. Song, and B. Lehman, “Self-driven synchronous rectification scheme without undesired gate-voltage discharge for DC-DC converters with symmetrically driven transformers,” *IEEE Trans. Power Electron.*, vol. 23, no. 1, pp. 506–510, Jan. 2008.

[24] M. Mohammadi and M. Ordonez, “Synchronous rectification of LLC resonant converters using homopolarity cycle modulation,” *IEEE Trans. Ind. Electron.*, vol. 66, no. 3, pp. 1781–1790, Mar. 2019.

[25] G. Y. Jeong, “High efficiency asymmetrical half-bridge flyback converter using a new voltage-driven synchronous rectifier,” *IET Power Electron.*, vol. 3, no. 1, pp. 18–32, Jan. 2010.

[26] D. Fu, Y. Liu, F. C. Lee, and M. Xu, “A novel driving scheme for synchronous rectifiers in LLC resonant converters,” *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[27] D. Fu, Y. Liu, F. C. Lee, and M. Xu, “An improved novel driving scheme of synchronous rectifiers for LLC resonant converters,” in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Feb. 2008, pp. 510–516.

[28] D. Fu, B. Lu, and F. C. Lee, “1 MHz High Efficiency LLC Resonant Converters with Synchronous Rectifier,” in *Proc. IEEE Power Electron. Spec. Conf.*, Jun. 2007, pp. 2404–2410.

[29] D. Wang and Y.-F. Liu, “A zero-crossing noise filter for driving synchronous rectifiers of LLC resonant converter,” *IEEE Trans. Power Electron.*, vol. 29, no. 4, pp. 1953–1965, Apr. 2014.

[30] (Mar. 2015). UCC24630 Synchronous Rectifier Controller With UltraLow-Standby Current. Texas Instruments. Dallas, TX, USA. [Online]. Available: http://www.ti.com/lit/ds/symlink/ucc24630.pdf

[31] (Oct. 2015). UCC24610 GREEN Rectifier Controller Device. Texas Instruments. Dallas, TX, USA. [Online]. Available: http://www.ti.com/ lit/ds/symlink/ucc24610.pdf

[32] (Feb. 2018). UCC24612 High Frequency Synchronous Rectifier Controller. Texas Instruments. Dallas, TX, USA. [Online]. Available: https://www.ti.com/lit/ds/symlink/ucc24612.pdf

[33] (Apr. 2015). NCP4303A, NCP4303B Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies. ON Semiconductor. Denver, CO, USA. [Online]. Available: https://www.onsemi. com/pub/Collateral/NCP4303-D.PDF

[34] (Mar. 2016). NCP4304A, NCP4304B Secondary Side Synchronous Rectification Driver for High Efficiency SMPS Topologies. ON Semiconductor. Denver, CO, USA. [Online]. Available: https://www.onsemi.com/pub/Collateral/NCP4304-D.PDF

[35] (Nov. 2013). IR1167(A,B)S SMARTRECTIFIERTM CONTROL IC. International Rectifier. El Segundo, CA, USA. [Online]. Available: https:// www.infineon.com/dgdl/ir1167aspbf.pdf?fileId= 5546d462533600a4015355c45d9c1655

[36] (2014). LT8309 Secondary-Side Synchronous Rectifier Driver Linear Technology. Milpitas, CA, USA. [Online]. Available: http://www. analog.com/media/en/technical-documentation/data-sheets/8309fa.pdf

[37] (Sep. 2018). Adaptive Synchronous Rectification Controller for LLC Resonant Converter. STMicroelectronics. [Online]. Available: https://www.st.com/resource/en/datasheet/srk2001a.pdf

[38] W. Feng, F. C. Lee, P. Mattavelli, and D. Huang, "A universal adaptive driving scheme for synchronous rectification in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 27, no. 8, pp. 3775–3781, Aug. 2012

[39] (2008). SIPMOS Small-Signal Transistor. Infineon. Munich, Germany. [Online]. Available: https://www.infineon.com/dgdl/Infineon-BSP300- DS-v02_02-en.pdf?fileId=db3a30433b47825b013b4c980bd0110d

[40] ADP300 ADP305 High Voltage Differential Probes. Teledyne Lecroy. [Online]. Available: http://cdn.teledynelecroy.com/files/pdf/adp3xxprobes-datasheet.pdf

[41] W. Feng, F. C. Lee and P. Mattavelli, "A hybrid strategy with Simplified Optimal Trajectory Control for LLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, 2012, pp. 1096-1103.

[42] C. Fei, F. C. Lee, and Q. Li, "Multi-step simplified optimal trajectory control (SOTC) for fast transient response of high frequency LLC converters," in *Proc. IEEE Energy Convers. Congr. Expo.*, 2015, pp. 2064– 2071.

[43] W. Feng, F. C. Lee, and P. Mattavelli, "Optimal trajectory control of burst mode for LLC resonant converter," *IEEE Trans. Power Electron.*, vol. 28, no. 1, pp. 457–466, Jan. 2013.

[44] W. Feng and F. C. Lee, "Optimal trajectory control of LLC resonant converters for soft start-up," *IEEE Trans. Power Electron.*, vol. 29, no. 3, pp. 1461–1468, Mar. 2014.

[45] (Oct. 2008). MT-001 Tutorial: Taking the Mystery out of the Infamous Formula, "SNR = 6.02N + 1.76dB," and Why You Should Care. Analog Devices. Norwood, MA, USA. [Online]. Available: https://www.analog.com/media/en/training-seminars/tutorials/MT-001.pdf

[46] C. Fei, F. C. Lee, and Q. Li, "Digital implementation of adaptive synchronous rectifier (SR) driving scheme for LLC resonant converters," in *Proc. IEEE Appl. Power Electron. Conf. Expo.*, Long Beach, CA, USA, 2016, pp. 322–328.

[47] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "A novel driving scheme for synchronous rectifiers in LLC resonant converters," *IEEE Trans. Power Electron.*, vol. 24, no. 5, pp. 1321–1329, May 2009.

[48] D. Fu, Y. Liu, F. C. Lee, and M. Xu, "An improved novel driving scheme of synchronous rectifiers for LLC resonant converters," in *Proc. 23rd Annu. IEEE Appl. Power Electron. Conf. Expo.*, Austin, TX, USA, 2008, pp. 510–516.

[49] P. Bernardi, R. Cicchetti, G. Pelosi, A. Reatti, S. Selleri, and M. Tatini, "An equivalent circuit for EMI prediction in printed circuit boards featuring a straight-to-bent microstrip line coupling," *Progr. Electromagn. Res. B*, vol. 5, pp. 107–118, Jan. 2008.

[50] D. Wang, L. Jia, Y.-F. Liu, and P. C. Sen, “An improved driving method for synchronous rectifier using drain-source voltage sensing,” in *Proc. 26th Annu. IEEE Appl. Power Electron. Conf. Expo.*, Fort Worth, TX, USA, 2011, pp. 1433–1438.

[51] C. Fei, F. C. Lee and Q. Li, "High-Efficiency High-Power-Density LLC Converter With an Integrated Planar Matrix Transformer for High-Output Current Applications," in *IEEE Trans. Ind. Electron.*, vol. 64, no. 11, pp. 9072-9082, Nov. 2017.

[52] M. H. Ahmed, A. Nabih, F. C. Lee and Q. Li, "High-efficiency, High-density Isolated/Regulated 48V Bus Converter with a Novel Planar Magnetic Structure," *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Anaheim, CA, USA, 2019, pp. 468-475.

[53] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu, and A. Q. Huang, “Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching,” in *Proc. IEEE 3rd Workshop Wide Bandgap Power Devices Appl. (WiPDA)*, Blacksburg, VA, USA, 2015, pp. 224–229.

[54] A. Anthon, J. C. Hernandez, Z. Zhang, and M. A. E. Andersen, “Switching investigations on a SiC MOSFET in a TO-247 package,” in *Proc. IECON 40th Annu. Conf. IEEE Ind. Electron. Soc.*, Dallas, TX, USA, 2014, pp. 1854–186.

[55] Rohm Semiconductor, “SCT3017AL N-channel SiC power MOSFET” Rohm Semiconductor, June 2018. [Online]. Available: https://d1d2qsbl8m0m72.cloudfront.net/en/products/databook/datasheet/discrete/sic/mosfet/sct3017al-e.pdf

[56] S. Manzoor, N. M. Karim, and N. Soin, “Analyzing p-MOSFET Lifetime by Employing R-D Model & MOS Device Theory,” Applied Mechanics and Materials, vol. 229-231, pp. 1626-1629.

[57] L. Zhang, S. Guo, X. Li, Y. Lei, W. Yu and A. Q. Huang, "Integrated SiC MOSFET module with ultra low parasitic inductance for noise free ultra high speed switching," *2015 IEEE 3rd Workshop on Wide Bandgap Power Devices and Applications (WiPDA)*, Blacksburg, VA, 2015, pp. 224-229.

[58] A. Anthon, J. C. Hernandez, Z. Zhang and M. A. E. Andersen, "Switching investigations on a SiC MOSFET in a TO-247 package," *IECON 2014 - 40th Annual Conference of the IEEE Industrial Electronics Society*, Dallas, TX, 2014, pp. 1854-186

[59] STMicroelectrics, “TD350 Advanced IGBT/MOSFET Driver” STMicroelectrics, USA, April 2010. [Online]. Available: https://www.st.com/resource/en/datasheet/cd00003358.pdf

[60] Infineon, “EiceDriver 1ED02I12-FT Single IGBT Driver IC” Infineon, Munich, Germany, July 2012. [Online]. Available: https://www.infineon.com/dgdl/Infineon-1ED020I12-FT-DS-v01_00-EN.pdf?fileId=5546d4624d6fc3d5014df660b42f4134

[61] A. Seidel and B. Wicht, "A fully integrated three-level 11.6nC gate driver supporting GaN gate injection transistors," *2018 IEEE International Solid - State Circuits Conference - (ISSCC)*, San Francisco, CA, 2018, pp. 384-386.

[62] H. C. P. Dymond, D. Liu, J. Wang, J. J. O. Dalton and B. H. Stark, "Multi-level active gate driver for SiC MOSFETs," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 5107-5112.

[63] Z. Zhang, Z. Dong, D. Hu, X. Zou and X. Ren, "Three-Level Gate Drivers for eGaN HEMTs in Resonant Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 7, pp. 5527-5538, July 2017.