Reliability Evaluation of Large-Area Sintered Direct Bonded Aluminum Substrates for Medium-Voltage Power Modules

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ABSTRACT

This thesis investigates techniques for prototyping and evaluation of medium voltage (MV) power module packages. Specific focus will be given to the utilization of silver sintering as a bonding method for high temperature, high density power modules. Nano-silver paste and preform will be examined in detail as enabling technologies for a new generation of power electronics. To accomplish this task, analysis and characterization of the metal-ceramic substrate and its structure is performed. First, finite element models are created to evaluate the fatigue behavior of the large area bonds in the substrate structure. Prototypes of these multi-layer substrates have also been fabricated and will be subjected to thermal cycling tests for experimental verification of the efficacy of their sintered silver bonds. Stacked direct-bonded aluminum (DBA) substrates have been found to withstand up to 1000 thermal cycles of –40 °C to 200 °C when attached with low pressure-assisted silver sintering. The thermal performance of 10 kV SiC power module utilizing multi-layer DBA substrates bonded with a large-area, low pressure-assisted sintered silver bond will also be examined to ensure the sintered bond is viable for the harsh operating conditions of MV modules. A junction-to-case thermal resistance of 0.142 °C/W is measured on a module prototype utilizing stacked DBA substrates. Finally, analysis of a double-sided cooling scheme enabled by large area sintering is
simulated and prototyped to demonstrate a 6.5 kV package for a MV power device. Residual stress failures induced by a highly rigid structure have been examined and mitigated through implementation of a 5 MPa pressure-assisted, double-sided silver sintering approach.
Reliability Evaluation of Large-Area Sintered Direct Bonded Aluminum Substrates for Medium-Voltage Power Modules

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GENERAL AUDIENCE ABSTRACT

Power modules are the building blocks of the electrical grid of the future. As society transitions to renewable energy to fight the crisis presented by climate change, the structure of the energy grid will have to change to accommodate the increase in solar, wind, geothermal, and other renewable sources of energy generation. A clean energy grid structure will contain ubiquitous opportunities to use power modules for medium-voltage (MV) applications, like managing the flow of electricity from solar panels and wind turbines to neighborhoods and office buildings. However, these MV power modules will need to be resilient to extreme temperature and electrical stresses inherent to these applications. Current technology must be improved in both performance and reliability to match the needs of this future grid. This thesis investigates, through both experiment and computer simulation, techniques for improving the reliability of MV power modules without sacrificing thermal or electrical performance. Techniques presented in this work have the potential to transform power modules, so they may operate at higher temperatures and efficiencies for a longer lifetime than the current state-of-the-art.
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Many thanks as well to Dr. Christina DiMarino, who has mentored and motivated me throughout my graduate school experience. Her guidance allowed me to learn more and push myself harder to tackle the exciting challenges of our work on electronics packaging.

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CHAPTER 1: INTRODUCTION

1.1 MOTIVATION AND APPLICATION BACKGROUND

Improvements in power electronics are critical for the future of consumer electronics, renewable energy, and transportation. Protecting public health and natural resources depends on the advancement of power electronics to use energy more sparingly to accomplish more. Traditionally, silicon (Si) power devices have been the foundation of power electronics. However, limitations in the temperature, switching speed, and voltage ratings of Si power transistors has led to the rise of more efficient, faster wide-bandgap (WBG) devices like silicon carbide (SiC) [2]–[5]. These devices target medium-voltage (MV) applications, such as data centers and wireless power transformers [6], [7]. The power electronics designed for these applications must be packaged with reliability in mind for their high power (megawatt and higher) dissipation. Conventional packaging technologies cannot withstand the high temperature and voltage operating conditions of MV devices [8]. For example, in [9] high frequency voltage transients and temperature degraded the breakdown performance of an epoxy resin in a power module.

Fig. 1: (a) A 10 kV "XHV-9" SiC power module from Wolfspeed and (b) a sub-module that can be paralleled in the XHV-9 configuration[1]
transformer. Reliability issues like these must be resolved without increasing the size or thermal resistance of the package. This thesis will evaluate packaging techniques and materials capable of withstanding the harsh operating environments of MV applications.

MV devices have the potential to drastically increase the power density of high-power systems. Silicon Carbide (SiC) has emerged as a likely candidate to replace conventional Si devices in MV applications. The higher thermal conductivity and high electric field of SiC suggest that it will replace Si where high operating temperature and power density are required [10].

Increased power density and efficiency afforded by SiC power devices are also critical for renewable energy and grid-scale power applications. Reduced switching losses due to increased carrier concentration allow for considerably improved converter efficiency in an interleaved DC-DC converter for renewable energy applications [11]. SiC converters also present advantages in reduced total harmonic distortion (THD) and filtering circuit size with the capability to switch at higher frequency [12].

The package for these devices must be designed with these performance benefits in mind. The focus of this thesis will be on evaluating MV package designs for optimal thermal performance and thermomechanical reliability.

1.2 RELIABILITY AND PERFORMANCE LIMITATIONS OF POWER MODULES

The current state-of-the-art for power modules packages employs an insulating ceramic substrate soldered to a baseplate for heat dissipation. One of the dominant failure modes of MV power modules is solder layer fatigue between the Direct-Bonded Copper (DBC) substrate and the baseplate or the power device. This interface is critical to the performance of the power module, as it is in the critical path for heat dissipation from the power devices [13]. The bottom side of the power devices are usually bonded to metal traces on the face of the ceramic substrate
to spread heat through the ceramic, away from the power device [14]. Investigations detailed in this thesis will present a silver sintering approach used on Direct-Bonded Aluminum (DBA) substrates to extend the reliability of the power module.

Several options exist for electrical connections to the devices. Wire bonds connecting the top side of the power device to the module terminals are a popular choice for power modules due to simple manufacturability, but long wire bonds contribute parasitic inductance to the electrical performance of the package (Fig. 2) [8]. Wire bonds can also degrade during the operating life of the module, resulting in bond wire lift-off, heel cracks, or bond wire cracks [16]. A design utilizing this structure with pin fins for baseplate cooling for a 7th generation IGBT power module achieves a maximum junction temperature under 150 °C with an inverter power output greater than 80 kW (Fig. 2). A similar structure for a 3.3 kV diode-less SiC MOSFET power module is able to achieve a maximum junction temperature of 175 °C at a current rating of 600 Arms [17], almost twice the current rating of the IGBT module in [15]. This performance was achieved in a standard power module footprint, referred to as nHPD² (Fig. 3).
Standard power modules are limited in switching speeds due to the parasitic inductance of the module package. Efforts have been made to improve the interconnect structures within the power module to reduce parasitic effects while also bolstering thermomechanical reliability. A 10 kV SiC power module is presented in [18] utilizing molybdenum (Mo) post interconnects to achieve switching transients of 260 V/ns. This is more than twice the maximum switching speed of a commercial, wire-bonded SiC power module that utilizes the same 10 kV MOSFETs [1]. Molybdenum also has a coefficient of thermal expansion (CTE) of 4.8 ppm/°C, which improves reliability by matching the CTE of other package materials [13] like silicon nitride (Si₃N₄) at 3.7 ppm/°C. The effects of thermomechanical fatigue and CTE mismatch will be further discussed in Chapter 4 of this thesis.

![Image of the nHPD2 open standard package with dimensions in mm][17]
1.3 IMPROVING RELIABILITY AND THERMAL PERFORMANCE IN POWER MODULES

The insulating substrate design for these power modules can be a limiting factor in the performance of the module in addition to limiting reliability. Previous works have demonstrated how utilizing stacked substrates can reduce switching transients and peak electric field intensity within the module, allowing for operation at higher voltages and switching frequencies. [19], [20] propose similar methods of redirecting current flowing through parasitic capacitances in the power module back to the dc power bus. Additionally, stacking the substrates in the power module can be used to reduce the peak electric field strength by grading the field across both insulation layers in the substrate stack. The 10 kV SiC module presented in [21] (Fig. 4) improves both on the common-mode screen implementation in [19], [20] while reducing the peak electric field in the module by connecting the mid-layer of the substrate stack to one-half of the dc bus voltage. This can improve the partial discharge performance of the module [22]–[24] and enable operation at the higher voltages required for MV power modules.

Fig. 4: A 10 kV SiC MOSFET module prototype utilizing multi-layer substrates for a common-mode screen and electric field grading [21]
This stacked substrate structure comes with the additional manufacturing challenge of fabricating the multi-layer structure. In particular, the large bonding area (greater than 1000 mm²) presents a challenge in creating a uniform, defect-free interface. Chapter 3 of this thesis will discuss the challenges of fabricating stacked substrates in greater depth.

As power modules increase in density and temperature rating, materials in the module are stressed to their reliability limit. Maintaining good thermal performance without sacrificing reliability is a key challenge in advancing power electronics packaging. Thermal cycling performance and lifetime analysis of solder bonds is well studied due to the maturity of the technology [25]–[29]. However, the melting temperature of solder is often below the maximum operating temperature of MV power modules. As a result, higher temperature bonding materials must be investigated for their reliability.

Sintered silver has emerged as a promising bonding material as it has exceptionally high thermal conductivity as compared to solder [30], [31]. This comes with the advantage of an exceptionally high melting temperature of 960 °C with a relatively low sintering temperature, close to 250 °C [32], [33]. Additionally, sintered silver shows promising reliability advantages over solder. Thermal cycling of solder and sintered silver die attach materials showed that sintered silver had a 10% advantage in thermal resistance increase when compared to equivalent solder bonds after 500 thermal cycles from –40 °C to 125 °C [29].

Improved die interface materials are used in conjunction with better insulating ceramic substrate materials to the overall thermal and reliability benefit of MV power modules. Silicon nitride (Si₃N₄), Alumina (Al₂O₃), and Aluminum Nitride (AlN) are all candidates for an insulating ceramic substrate depending on the cost, thermal conductivity, and reliability needs of a power module package [34]–[40]. These insulating substrates can be bonded into the multi-
layer configuration discussed in the previous section. The reliability of these bonded structures will be modeled in Chapter 2 and examined experimentally in Chapter 4.

1.4 ORGANIZATION OF THESIS

To present a thorough investigation into the advanced packaging techniques mentioned, this thesis will be organized as follows:

Thermal cycling performance and the reliability tradeoffs of different substrate configurations will be discussed using finite element modeling in Chapter 2. These results will be used in conjunction with physical experiments and prototypes to draw conclusions about the geometries modeled in simulation. Chapter 3 will detail the process of prototyping substrate samples using two, large-area, silver sintering techniques. These prototype samples will also be utilized for thermal cycling tests to evaluate the reliability of the large area bonding method developed in this chapter. Chapter 3 will also include a thermal resistance characterization of a module fabricated using the updated, large-area bonding techniques. This thermal evaluation will be compared to previous module prototypes as well as commercially available power modules. Results of thermal cycling tests and failure analysis on samples will be presented in Chapter 4. Both non-destructive and destructive techniques will be discussed as well as their respective levels of efficacy in examining the bonded interface of stacked substrates.

Some of the challenges with advanced package design will be presented through the design and prototyping of a double-sided cooled discrete power package in Chapter 5. An electrical and thermal co-design approach is employed using finite element analysis to create a high performance, low thermal resistance package for a 6.5 kV, 25 A application. This application of low pressure-assisted silver sintering incurs some residual stress in the package geometry that can cause early lifetime failures in a rigid package structure. Analysis of these
early lifetime failures, including mitigating strategies, will be presented along with experimental measurements of the package.
CHAPTER 2: THERMOMECHANICAL ANALYSIS

2.1 INTRODUCTION

This section will discuss thermomechanical modeling of the reliability of power packages. The models discussed will include structures related primarily to the insulating substrate structure of the power module. The goal of this modeling is to examine the fatigue behavior of large-area bonded interfaces for power module substrates. Finite element analysis has been performed using ANSYS Mechanical due to the reported accuracy of the software in existing literature [41], [42].

Modeling the thermomechanical behavior of the power module structure is an important aspect of a holistic reliability evaluation. Simulations provide insight into the location and magnitude of deformation induced in a power package during temperature changes [40], [43]. Qualitative comparisons between different materials and structures can then be made by varying those properties in the simulation. Of particular interest is the direct-bonded aluminum (DBA) substrate, which is used to fabricate the substrate stacks discussed in Chapters 2-4. Previous work has reported on the high thermal cycling reliability of single DBA substrates as compared to active metal-brazed (AMB) and direct-bonded copper (DBC) substrates [37], so modeling and evaluating DBA substrate stacks is of interest.

The effect of the deformation must also be characterized over time, as operating a power module inevitably induces cyclic heating and cooling during its life cycle [44]. Simulation methods can be employed to examine the fatigue behavior of bonds in the power module as they respond to this cyclic stress. The results of these simulations can then be presented along with empirical data to comment on the overall reliability of a power module structure, as is done in [45].
In this thesis, thermomechanical models in this chapter are presented along with thermal cycling tests described in Chapter 4. The modeling work in this chapter compares the thermomechanical behavior of large-area sintered multi-layer substrates to the more conventional structure of a single ceramic substrate soldered to a baseplate. Additionally, modeling of the stacked substrate structure in isolation will be compared to a model of a MV power module utilizing stacked DBA substrates.

2.2 MODELING METHODOLOGY

Modeling the fatigue behavior of the bonds in a power module requires evaluating both the elastic and inelastic behavior of the materials in the module structure. Components like the insulating ceramic of the substrate, substrate metal traces, and baseplate are modeled using linear-elastic properties since the deformation of those components induce the fatigue stress in the bond layers. The properties of the bonds in the module are defined from experiments on the material, used to create a constitutive model that describes the inelastic or plastic behavior of the material. Solder bonds can be modeled using the Anand constitutive model, [46] which describes the viscoplastic behavior of solder as it fatigues. The constitutive model properties can then be used to simulate the inelastic deformation of bonds in a power module as the joint fatigues during cyclic thermal stress [47]. The Anand model is selected as it uses a “single, scalar internal variable” which combines both rate-dependent and rate-independent plastic strain. The Anand model is also readily available in finite element software, and requires less CPU processing time than classical plastic flow and power law creep theories [47].

When simulating bonds using the Anand model, the proper mathematics must be employed to calculate how much a bond fatigues during thermal cycling. [28] presents a method of calculating inelastic strain using the volume-averaged strain energy density (SED) accumulated each thermal cycle. This volume-averaged parameter reduces the sensitivity of the
model to meshing by normalizing the plastic work done on each mesh element by the volume of that mesh element [48]. Both [25] and [45] implement this methodology and are the framework for thermomechanical analysis performed in this chapter.

As discussed in the introduction, this investigation is concerned with utilizing sintered silver as a large-area bonding method for power modules. Existing research has established an Anand model for sintered silver [49] enabling the same methodology. Modeling work presented in this chapter will use the Anand model established in [49] to calculate the SED per thermal cycle for sintered silver. The Anand model presents a set of constitutive equations that describe the creep behavior of metals during temperature-induced, mechanical stresses. The Anand model describes the kinematic hardening and plastic flow properties of “hot-worked” metals; which pertains to temperatures between 50 % and 90 % of the melting point and strain rates of between \(10^{-4}\) and \(10^{-3}\) sec\(^{-1}\). Typically, this model is applied to solders, but [49] has demonstrated an adaptation of the Anand model for sintered nano-silver structures.

2.3 THERMOMECHANICAL MODELING OF STACKED SUBSTRATES

As discussed in the introduction, MV power modules can benefit greatly when utilizing a stacked substrate geometry. The interface between the two insulating layers of the substrate stack is a large area to bond (greater than 1000 mm\(^2\)), and the thermomechanical stresses in the interface need to be analyzed. First, the location of the peak stress concentration in the bond must be identified. A quarter-symmetry model of a stacked substrate is built in ANSYS. The thickness of the metallization layer is 0.3 mm and the insulating ceramic is 1 mm thick. The simulated bonding layer thickness is 100 \(\mu\)m. These thicknesses and the dimensions of the substrates are based on the samples fabricated for testing in Chapters 3 and 4 and are part of the module design from [21]. The meshed model is shown in Fig. 5 below. The DBA stack is symmetrical lengthwise and widthwise, so the FEA model can be calculated on a quarter section of the stack.
All elements in the mesh are hexahedral, and sizing controls are implemented to refine the mesh at the corner of the sintered silver joint where the peak stress occurs. Perfectly elastic elements like the ceramic and aluminum metal layers are meshed more coarsely as the modeling focus is the sintered silver. The total mesh count was 13,992 elements and 118,671 nodes.

A single temperature cycle of –40°C to 200°C is applied to the substrate stack and the maximum shear stress is plotted across the surface of the sintered silver bond. This temperature range is selected based on a literature survey detailed in Chapter 4. Fig. 6 shows the stress profile of the sintered silver bond, indicating that the peak stress is at the 1-mm-radius rounded corner of the sintered layer. With the location of peak stress identified, thermal cycling of the model can be executed to calculate the SED per cycle at the peak stress location. Four thermal cycles of –40°C to 200°C are applied to the model and the strain energy density is calculated for each thermal cycle. Multiple cycles are applied to allow the model results to converge and to minimize the error in the SED calculation by averaging data from more thermal cycles.
Fig. 6: Stress plot of the sintered silver bonding layer of stacked substrates

Fig. 7 compares the SED per thermal cycle for a stacked DBA versus a stacked DBC and a DBC bonded to a baseplate. The modeling results in Fig. 7 are provided by Paul Paret from the National Renewable Energy Laboratory (NREL). Even at a less severe temperature profile of –40 °C to 150 °C, the baseplate-DBC configuration experiences 45 times greater strain energy density per thermal cycle than the stacked DBA configuration. The stacked DBC model experienced a slightly lower SED per cycle than the stacked DBA (0.07 MPa and 0.09 MPa respectively). However, this does not necessarily mean a stacked DBC configuration is more reliable than the stacked DBA. The slightly lower SED in a DBC stack does not alleviate the risk of copper traces delaminating from the ceramic as observed in [50] nor does it address the oxidation and cracking of DBCs reported in [36]. Because the CTE of copper (16.5 ppm/°C [51]) is less than the CTE of aluminum, (23.8 ppm/°C [52]) the DBC to DBC substrate stack model calculates less thermomechanical fatigue. This is because the properties of the metals in these...
simulations are perfectly linear-elastic, while in reality the aluminum would experience deformation and grain sliding during thermal cycling [53].

Aluminum is also softer than copper, and is potentially a strain relieving mechanism for the large area bond in the DBA stack. Thermal cycling tests discussed in Chapter 4 of this thesis will validate the reliability of two-layer DBA stacks with thermal cycling tests and failure analysis.

2.4 ANSYS THERMOMECHANICAL MODEL OF A 10 KV MODULE

Simulations of the stacked substrate geometry in isolation must be related to their behavior when incorporated in a module structure. A finite element model of the 10 kV SiC module design (Fig. 4) has been created to analyze the thermomechanical stress experienced by the two-layer substrate stack during thermal cycling. Using the same methodology as discussed in Chapter 2.3, the mean strain energy density per thermal cycle is determined on a large-area
sintered bond. There are two stacked substrates in the geometry of the 10 kV SiC power module: one bonded to the drain (bottom) side of the MOSFETs, and another bonded to post interconnects on the source and gate (on the top) of the MOSFETs. The more critical large-area bond of these two-layer substrates is that of the bottom DBA stack, bonded to the drain connections of the two MOSFETs. This DBA stack is in the primary heat conduction path for the module, and any degradation of the large-area bond will degrade the overall performance of the module severely.

First, the peak stress location in the lower DBA stack is identified for the 10-kV module just as with the standalone DBA stack. The model is meshed similarly to the standalone model of the DBA stack, where the mesh is refined at the corner of the sintered silver bond and simplified for the linear-elastic elements. The mesh is shown in Fig. 8 and contains 26,795 elements and 118,671 nodes. The model is subjected to a single thermal cycle from –40°C to 200°C to identify the location of peak stress in the sintered silver bond. The peak stress magnitude and location within the sintered bond is the same for both the standalone DBA stack model and the model of the entire 10 kV module structure. With the peak stress location confirmed, the 10-kV module model can be simulated through 4 thermal cycles to calculate the SED per thermal cycle.
A CAD model drawing of the SiC power module is shown in Fig. 9 with planes of symmetry showing where the model can be divided to reduce processing time in ANSYS. This allows the simulation to evaluate the effect of the entire module structure on the sintered bond layer without solving the stress conditions on the entire structure. Only one quarter needs to be

Fig. 8: Meshed model of a 10 kV SiC power module

Fig. 9: ANSYS model of the 10 kV SiC MOSFET module with planes of symmetry shown
computed, then that solution can be mirrored across the symmetry planes. The patterned metal traces on the surfaces of the top DBA are also simplified to reduce the meshing complexity of the model. Fig. 10 shows a side view of the model, indicating where the large-area bond of interest exists in the module.

Modeling the entire module structure is critical to examine how the die, post interconnects, and upper substrate stack affect the critical sintered silver bond at the base of the module. The CTE of 4H-SiC is between 4 and $4.5 \cdot 10^{-6}$ ppm/$^\circ$C [54] while the CTE of AlN can reach more than double that value at approximately $11 \cdot 10^{-6}$ ppm/$^\circ$C [55]. This mismatch, as well as the difference in expansion for aluminum, molybdenum, and silver will exacerbate the fatigue behavior of the module.

Results from the simulation show that the strain energy density per thermal cycle is equivalent for the model of the DBA two-layer stack model and the complete module. One
The explanation for this equivalence is the presence of the Mo post interconnects as a buffer between the lower and upper substrates. The low CTE of Mo (5.35 ppm/°C [51]) is a good match to the typical CTE of AlN (4.03 ppm/°C [52]). This will ensure that the deformation of the upper substrate stack is minimally influential on the lower substrate stack. It is therefore reasonable to conclude that the passive thermal cycling reliability of a DBA stack will not decrease when assembled in the power module. Table I compares the SED per thermal cycle for each of the simulated configurations in this investigation. The results presented support the hypothesis that a stacked substrate structure will be more reliable than a single substrate bonded to a baseplate.

Because the CTE of copper is less than the CTE of aluminum, the DBC to DBC substrate stack shows less thermomechanical fatigue than that of aluminum.

Chapter 4 will discuss thermal cycling tests and failure analysis performed on two-layer DBA substrate samples that can provide insight into the reliability of the 10 kV SiC module.

<table>
<thead>
<tr>
<th>Configuration</th>
<th>SED per Thermal Cycle (MPa)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DBC-Baseplate</td>
<td>3.2</td>
</tr>
<tr>
<td>DBC-DBC</td>
<td>0.07</td>
</tr>
<tr>
<td>DBA-DBA</td>
<td>0.09</td>
</tr>
<tr>
<td>DBA-DBA in a SiC Power Module</td>
<td>0.09</td>
</tr>
</tbody>
</table>
CHAPTER 3: LARGE-AREA, LOW PRESSURE-ASSISTED SINTERING

3.1 INTRODUCTION

As discussed in the introduction and Chapter 2, large bonding areas are necessary to fabricate two-layer and multi-layer ceramic substrates for power electronics. Bonds between insulating substrates are often greater than 1000 mm\(^2\) in area [56]. Maintaining a uniform bond over a larger surface area is challenging, and can require increased pressure or temperature during fabrication. Large area bonding must be achievable with reasonably low-pressure assistance and with moderate temperatures to become commercially adopted.

There is motivation for exploring silver sintering for large-area bonds for MV power modules. The high melting temperature and thermal conductivity of silver are beneficial, provided the bonded area can be increased from the scale of previous work [57]. This chapter will discuss the refinement and evaluation of low-pressure silver sintering processes for large bonded areas greater than 1000 mm\(^2\).

3.2 PREVIOUS WORK ON LARGE-AREA BONDING

Stacked substrates have yet to become easily available from commercial suppliers, but research has been conducted to examine viability of different methods. Solder, metal brazing, and sintered silver have been investigated for the large-area bonds between substrate stacks. Soldered AlN DBC substrates have been thermally cycled in [50] from –55 °C to 195 °C and failed severely before 125 cycles. Copper traces delaminated from the substrates, soldered bonds and the ceramic cracked from the cyclic temperature cycling. Another investigation utilizes metal brazing for a large-area bond [58]. Stacked Si\(_3\)N\(_4\) DBC substrates are fabricated for a SiC power module and thermally cycled from –55 °C to 195 °C. The brazed joint in the multi-layer DBC stack increases in thermal resistance and degrades rapidly when subjected to
thermomechanical stress. Both soldering and metal brazing therefore are not adequately reliable bonding methods for high density power modules that can experience severe thermomechanical stress.

Recent research has investigated the feasibility of large-area sintered substrates to create these multi-layer structures [26], [58], [59]. However, the quality of the sintered bond line using these techniques had wide variability. Achieving a high-quality bond is important to reduce the thermal resistance of the power module. Sintered silver has an inherent porosity that originates from the micro- and nano-scale particles that co-diffuse to form its structure [31]. The porosity of the sintered silver dictates its electrical and thermal resistivity, and is critical in establishing sintered silver as a viable bonding material [60], [61]. The porous structure of the sintered silver bond will be analyzed both in this chapter through examination of as-sintered samples and in Chapter 4 with analysis of samples exposed to cyclic thermal cycling tests.

A technique utilizing a nano-silver preform on a polyimide carrier film has been investigated in [62] as a more repeatable method of silver sintering. Sintered silver die attach using a nano-silver preform has been shown to have greater thermomechanical reliability than DBC substrates when exposed to 1000 thermal shocks from −55°C to 125°C [63]. While these results are encouraging regarding the reliability of sintered silver preform, there is little data on larger bonding areas. In a power module structure, the area of the insulating substrate must be used as an interface to a heat-spreading structure for thermal performance [8]. The silver preform work in [62] and [63] does not analyze any bonding areas larger than 5 mm by 5 mm.

3.3 PRESSURE-ASSISTED SINTERING PROCESS REFINEMENT

Two silver sintering processes were investigated and are described in detail in sections 3.3.1 and 3.3.2. These procedures were developed based on prior feasibility studies on large-area silver sintering [33], [64], [65] and aimed to find the lowest sintering pressure for an optimal
bond. In previous works, Confocal Scanning Acoustic Microscopy (C-SAM) has been utilized as a non-destructive technique for analyzing the quality of a sintered bond [25], [56], [66]. C-SAM uses the reflection time of a modulated ultrasonic pulse to measure the density of different materials in a laminate structure. Low density regions, like voids or cracks, are detectable based on how they delay the reflection of an ultrasonic signal to and from the transducer in the C-SAM. As with previous successful investigations, this work has been developed using AlN DBA substrates provided by DOWA Metaltech. The DBA substrates investigated are 23.1 mm in width by 49.2 mm in length; the same dimensions as the lower DBA substrate stack in the module presented in [21]. The total bonded area of the lower DBA stack is 1120 mm². The aluminum metal of the DBA is plated with nickel and silver for compatibility with both silver sintering and soldering. Nano-silver paste and preform are engineered and provided by NBE Tech and Dr. GQ Lu.

Samples were fabricated by the author and shipped to the National Renewable Energy Laboratory (NREL) for C-SAM scanning to evaluate the quality of the selected process. Results from C-SAM images aided in reforming the sintering process to achieve better results. Fig. 11 shows the most uniform C-SAM images of as-sintered samples for both bonding methods. Lighter regions in the image represent a lower density detected by the C-SAM, as indicated by a longer time of flight in the ultrasonic signal. Darker regions represent higher density, and a shorter time of flight.
In Fig. 11b, the image is a more uniform color, and therefore a more uniform density in the areas scanned. Fig. 11a has a large white region at the center, which is most likely a large system of voids or cracks in the nano-silver bond. The most uniform nano-silver paste sample was achieved with 1 MPa sintering pressure while the nano-silver paste presented the most uniform when sintered at 3 MPa pressure.

3.3.1 Sintering with Nano-Silver Paste

The nano-silver paste method uses a screen-printing technique to deposit a uniform layer of nano-silver paste 100-µm thick. A stainless-steel stencil is used to control the thickness of the paste, and a squeegee is used to spread the paste evenly across the DBA surface. A layer of nano-
silver paste is printed onto each DBA before drying on a hot plate at 125 °C for 90 minutes. The paste is dried using open-faced contact drying [64] to remove most of the organic binder so that voiding caused by its evaporation during sintering can be reduced [33], [64]. Fig. 12 shows the substrates drying on a hot plate with the nano-silver paste printed over the silver-plated aluminum metallization. Due to the high viscosity of the nano-silver paste, lifting the stainless-steel stencil can result in small, raised edges at the perimeter of the screen-printed paste layer. These edges can be observed on the DBA on the left of Fig. 12. Because the metal powder in the nano-silver paste is very soft before sintering, these edges are flattened and pressed away from the center of the bonding area during sintering. Evaluations of the as-sintered samples later in this chapter show no adverse effects from these raised edges.

Once the paste has dried, the two substrates are aligned together. The substrates are then sintered in a Carver bench-top auto press. The platens of the hot press are set to 200 °C at the top and 250 °C at the bottom to achieve a target temperature of 250 °C at the sintered silver bond.
Experiments using a thermocouple between two DBA samples confirm that the temperature reached 250 °C given this configuration. The substrate stack is then sintered with 1 MPa pressure applied for 1 hour. The stack is then cooled to room temperature by turning off the hot press without relaxing the pressure. This is done to mitigate any warping caused during sintering as is observed with similar sintering processes in [56].

3.3.2 Sintering with Nano-Silver Preform

The nano-silver preform bonding method utilizes a dried silver film on a mylar carrier sheet. The pre-dried film can be stamp-transferred and sintered without a drying step and at a much shorter sintering time than the nano-silver paste due to the lack of any organic binder in the preform.

First, the preform is cut to the size of the DBA substrate. Using the Carver hot press, nano-silver preform is stamped onto one of the DBA substrates using a pressure of 1 MPa for 60 seconds and a bottom platen temperature of 140 °C. A pressure-sensitive paper is placed under the DBA substrate to ensure pressure uniformity during this step. After transferring to the DBA surface, narrow strips of preform can hang over the edges of the DBA metal as shown in Fig. 13.

Fig. 13: DBA substrate with nano-silver preform stamp-transferred to the substrate metal surface
This excess preform can be carefully removed with a dental tool or scalpel by scraping the tool along the edge of the DBA metal. The excess preform must be removed before sintering, as it is significantly more difficult to trim after bonding the DBA stack. Excess preform extending beyond the edge of the DBA metal is also a partial discharge risk, as the distance of the DBA metal to the substrate edge is a carefully engineered creepage distance [21]. The substrates are then aligned, and sintered. The sintering process for this method is shown in Fig. 14. The substrates were sintered for 90 seconds under pressures varied from 1 MPa to 3 MPa. The platens of the hot press are set to 200 °C at the top and 250 °C at the bottom to achieve the same target temperature as the nano-silver paste method: 250 °C at the sintered silver bond. Experiments using the thermocouple between two DBA samples were repeated, and again confirmed that the temperature reached 250 °C given this configuration.

C-SAM images of substrate stacks showed a higher degree of uniformity when 3 MPa was applied [67]. Additionally, samples were fabricated using different pressure conditions while cooling. C-SAM comparisons of samples sintered and cooled under pressure showed no significant benefit in bond uniformity when compared to samples cooled pressure-less.

3.4 RESULTS OF PROCESS REFINEMENT

In previous investigations sintering with nano-silver paste, substrates were found to have cracked when subjected to more than 1 MPa pressure, [18] particularly those with vias. With the procedures described in 3.3.1 and 3.3.2, no substrates cracked during sintering. C-SAM scans of the fabricated samples suggested that a sintering pressure of 1 MPa for nano-silver paste and 3 MPa for nano-silver preform yielded the best results of the pressures tested. No sintering pressure above 5 MPa was tested, as the goal of refining this process was to reduce the sintering pressure without sacrificing bond quality.
Experiments were performed with a pressure-sensitive film during all of the pressure application steps to check for a uniform distribution of force on the substrate surface. Experiments including and excluding the silicone rubber in the sintering stack were performed to identify the configuration yielding more uniform pressure distribution. Fig. 15 shows the pressure-sensitive film from tests with and without silicone rubber in the sintering stack. The film shows the application of pressure by depositing red marks where the pressure applied.
exceeds 70 psi (approximately 0.48 MPa). A color chart is provided with the film to estimate the magnitude of pressure applied based on the darkness of the mark color. Fig. 15 shows that the magnitude of the pressure applied to the DBA face when no silicone is present in the stack is inconsistent, with very high concentrations in a few localized areas. Some regions show no response to the applied pressure at all. When the silicone is present in the sintering stack, the pressure-sensitive film produces a consistent, rectangular image in the shape of the DBA substrates used in testing. The color is fairly even throughout, but shows some clear darkening at the top of the film while the bottom of the mark is somewhat lighter. By correlating the color of the mark on the film to the color chart, the author estimates that the applied pressure varies from 2.4 MPa to 3.0 MPa. It is clear that the silicone rubber is essential in applying uniform pressure to the DBA surface. The thickness of the silicone rubber was not varied, a 1/8\textsuperscript{th} inch thick sheet was used for the bottom of the stack and a 1/16\textsuperscript{th} inch thick sheet for the top of the stack. It is possible that varying the thickness of the rubber could affect the quality of the bond, but further investigation is needed to test that hypothesis.

3.4.1 Cross-Section and Imaging Analysis

Two samples made under these processing conditions are fabricated for cross-sectioning and optical microscope imaging. The selected samples were fabricated by the author at Virginia Tech’s facilities in Arlington, Virginia, and then shipped to NREL in Golden, Colorado where more sophisticated analysis equipment was available. Analysis preparation was performed by Joshua Major (NREL). Samples were cast in an epoxy resin and cut with a dicing saw to expose the sintered silver bond between the DBA substrates. The cross-section face was then polished with a diamond particle slurry containing an average particle diameter of 20 µm.
Fig. 16 below shows optical microscope images of cross-sections from a nano-silver paste and nano-silver preform sample cut without any additional stresses applied post-fabrication. The sintered silver bond is uniform and dense with no signs of defects or cracking. Because the nano-silver preform sample showed greater uniformity in its C-SAM scan, and the sintering time is significantly shorter than that of the paste method, it was decided to dedicate

![Image](image1.png) (a)

![Image](image2.png) (b)

Fig. 16: Optical microscope images of (a) a nano-silver preform- and (b) a nano-silver paste-bonded DBA stack, cross-sectioned after sintering and polished with a diamond slurry.
more resources to analyzing the cross-section of the nano-silver preform sample. A scanning electron microscope (SEM) at NREL was used to prepare and image the sample surface. The sample surface was ion-milled at a voltage of 4 kV for 1 hour.

Fig. 17 shows an SEM image of the nano-silver preform sample at 1000x magnification. The sintered silver bond is uniform, dense, and free of any obvious defects or cracks. An image processing software tool is used by NREL to collect an estimate of the porosity of the sample. The software estimates that the porosity of the image in Fig. 17 is approximately 11%.

A lower magnification image of the bond indicates that the entire cross-section face is not
entirely uniform.

Fig. 18 shows an SEM image at 500x magnification, where voids between 10 and 15 µm in diameter are present in the sintered silver and the aluminum metal of the DBA. The source of these voids is unclear, and further investigation is needed to identify their cause. Optical microscope images, like those shown in Fig. 16, show no signs of this voiding despite the high resolution of the optical images. This suggests that the voids are either uncovered or caused by the ion milling process, as that is the only difference in sample preparation between the optical

Fig. 18: SEM image of a DBA stack sintered with nano-silver preform at 500x magnification
microscope and SEM images. SEM images of samples cross-sectioned after thermal cycling presented in Chapter 4 will show that these voids are not present in some other samples sintered under the same conditions.

3.4.2 Thermal measurements of stacked substrates

A thermal analysis is performed on a 10 kV SiC module prototype to determine the thermal resistance of the two-layer DBA stack. The prototype power module pictured in Fig. 19 was assembled using DBA stacks sintered with nano-silver preform using the method described in 3.3.2. The bottom DBA stack has two 10 kV SiC MOSFETs bonded to its top metal trace via pressure-less silver sintering.

![Stacked Ceramic Substrates](image)

**Fig. 19: A Wire bond-less 10 kV SiC power module**
The die placement on the bottom DBA stack is shown in Fig. 20. The placement of the dies and the patterning of the DBA metal are symmetrical, and the uniformity of the images shown in Fig. 11 and Fig. 17 are enough that the thermal resistance of the package will be identical for both of the SiC die packaged in this module. Additionally, since there is no designed path for cooling the SiC MOSFETs through the top of the device, any heat flow out of the top of the devices can be neglected. The heat conduction of the entire power module is therefore dominated overwhelmingly by the dissipation provided by the bottom DBA stack.

Thermal resistance measurements are taken on the Analysis Tech Phase 12B Thermal Analyzer and use the packaged SiC devices and their body diodes to monitor junction temperature during testing. A small measurement current of 20 mA forced through the body diode of the SiC MOSFET produces a temperature sensitive voltage known as the Temperature Sensitive Parameter (TSP) of the device [68].

TSP calibration is performed by placing the power module in an oven with a

![Image: A close-up of the DBA stack showing the dimensions 49.2 mm and 23.1 mm, with labels indicating silver-plated aluminum traces, 10 kV SiC MOSFETs, Mo post interconnects, and AlN ceramic.]

Fig. 20: 10 kV SiC MOSFETs bonded to a patterned DBA stack
thermocouple placed as close as possible to the MOSFET being measured. The module is also clamped to a large aluminum heatsink, which assists in distributing the temperature evenly in the heating chamber. The oven is brought up to 100 °C gradually so the power module can heat evenly throughout the package. Once the target temperature is achieved (as indicated by measuring at thermocouple) the oven chamber is allowed to cool naturally. Measurements of the TSP are taken periodically to record the linear relationship between the TSP and the junction temperature. By calibrating the TSP and monitoring the ambient temperature in a controlled environment, transient thermal resistance measurements can be collected with relative ease.

Fig. 21 demonstrates the setup for heating characterization and thermal resistance calculation, where the power module is clamped to a liquid-cooled plate via a pneumatic piston.

Fig. 21: Thermal resistance measurement fixture on the Analysis Tech Phase 12B Thermal Analyzer
A thermal interface material is applied to the base of the module to ensure good contact with the cooled heat sink. The module is mounted to an interface board to allow connections to each of the devices in the half-bridge with banana connectors. The temperature of the liquid coolant is monitored through the Phase 12B while a controlled power is applied to the MOSFET channel to heat the module. 120 µs after applying a heating pulse to the MOSFET, the 20-mA measurement current is applied to the body diode and a data point is collected including both the junction and ambient temperature. Once equilibrium is achieved, thermal resistance of the package can be calculated using the JEDEC 51-14 Transient $R_{jc}$ Determination [69]. The $R_{jc}$ determination requires two heating curves to be collected – one with a highly conductive thermal interface material and one with a highly insulating thermal interface material. This is done so that a divergence in the heating curves can be identified where the thermal interface material dominates the thermal impedance of the entire structure clamped to the analyzer. The divergence point of the two heating characterization curves is the junction-to-case thermal resistance of the package under test.
Fig. 22 shows the heating characterization curves for the SiC module. The thermal resistance of 0.142 °C/W compares favorably to commercially available power modules with much lower power density. As a reference, the 1200 V IGBT power module in [69] achieves a measured junction-to-case resistance of 0.88 °C/W. This measurement is also in close agreement with previous experiments performed on DBA substrate stacks [70]. The measured thermal resistance of those stacks varied from 0.11 °C/W to 0.14 °C/W. Table II summarizes thermal impedances of commercially available modules and packages.

Fig. 22: Heating characterization curves indicating the thermal resistance of the 10 kV SiC power module
The summarized values are similar to the measured thermal resistance of the power module prototype presented in this chapter, indicating that the large-area, silver sintering techniques used to fabricate the module are promising for MV power modules. Additionally, the low porosity estimate shown in Fig. 17 is supported by the low thermal resistance measurement collected on the power module prototype. The work in this chapter provides a foundation of evidence that sintered silver is a high-performance bonding solution for large area interfaces in MV power modules. The following chapter will examine the reliability of these sintered silver bonds during thermal cycling.

**Table II: Thermal resistance summary for different commercial and research packages**

<table>
<thead>
<tr>
<th>Package</th>
<th>Commercially Available (Y/N)</th>
<th>Rjc (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPES 10 kV SiC Module (2-die half-bridge)</td>
<td>N</td>
<td>0.14</td>
</tr>
<tr>
<td>CPES 10 kV SiC Module (6-die half-bridge)[70]</td>
<td>N</td>
<td>0.11-0.14</td>
</tr>
<tr>
<td>Single-sided cooling AMB power module[71]</td>
<td>N</td>
<td>0.14</td>
</tr>
<tr>
<td>Double-sided cooling AMB power module[71]</td>
<td>N</td>
<td>0.11</td>
</tr>
<tr>
<td>“Easypack” FS25R120W1T4 power module[69]</td>
<td>Y</td>
<td>0.88</td>
</tr>
<tr>
<td>1200 V IGBT Module GD50FFL120C5S[72]</td>
<td>Y</td>
<td>0.29</td>
</tr>
<tr>
<td>N-channel 1200V IGBT (TO-247 package)[73]</td>
<td>Y</td>
<td>0.57</td>
</tr>
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</table>
CHAPTER 4: THERMAL CYCLING AND FAILURE ANALYSIS

4.1 INTRODUCTION

The ceramic substrate is a critical component in the thermal impedance of a power module. The material and thickness of the substrate are constrained by the electrical design of the power module but directly influence the heat dissipation capabilities of the design. Additionally, design of the ceramic substrate affects the overall reliability of the module during temperature cycling and continuous operation. Cyclic heating and cooling of the power module is inevitable during normal operation. As the different materials in the package rise and fall in temperature, they expand and contract differently due to variations in the coefficient of thermal expansion (CTE) from one material to another [27]. This CTE mismatch induces fatigue that can eventually lead to cracking of solder joints, delamination of substrate traces, and consequent failure of the power module.

Finite element modeling is a useful tool for qualitative analysis, but it does not provide empirical data to evaluate and compare packages. The best method for evaluating resilience to these stresses is to perform thermal cycling tests. There is a standard method for testing discrete components, as defined by JEDEC, but for more advanced materials and structures it can be necessary to adjust the thermal cycling conditions [74]. Tests are executed in a thermal cycling chamber, pictured in Fig. 23, that controls the ramp rate, dwell time, and temperature peaks of the cycling profile.
This chapter will discuss how a temperature profile was selected and applied to evaluate the reliability of two-layer DBA stacks. Also included is a discussion of how a sample population was created to compare the sintering methods discussed in Chapter 3. Finally, failure analysis will be presented on samples that have degraded under cyclic thermal stress.

4.2 SINGLE SUBSTRATE RELIABILITY

4.2.1 Background

As MV power applications incorporate more power electronics, their packages must improve to tolerate higher electric field and thermal performance requirements. The insulating substrate is a critical component in higher voltage and power packages. Improvements to the reliability and thermal performance of the package are tied directly to improving the insulating substrate. In particular, partial discharge performance is a challenge for high voltage packages.
Increasing the thickness of the insulating ceramic provides diminishing returns on the Partial Discharge Inception Voltage (PDIV) while increasing the thermal resistance of the package [23]. Thus, careful design of the substrate and selection of the substrate materials are more critical to the performance of a high voltage power package [23], [24].

4.2.2 Existing Reliability Research for Single Substrates

Substantial reliability work has been performed on single-layer ceramic substrates as they represent the current state-of-the-art in high density power modules. Some finite element modeling of warpage and thermomechanical phenomena has been assessed in active metal-brazed (AMB) and DBC substrates [56], [75], but the majority of research on single substrates is experimental. Thermal shock and thermal cycling reliability tests comparing the performance of AMB and direct-bonded aluminum or copper (DBA, DBC respectively) substrates demonstrate that DBA and DBC are more resilient than their AMB counterparts [27],[29],[35].

Single Si$_3$N$_4$ DBC substrates subjected to thermal cycling from –40 °C to 250 °C showed no signs of delamination of the metal-ceramic interface even after 3000 thermal cycles [36]. However, substrates exhibited oxidation, cracking, and surface roughening of the copper metallization layer. Cracks averaged greater than 10 µm in length after 1000 thermal cycles. Single DBA substrates showed superior high temperature thermal cycling performance as compared to DBC [76], [38]. Although DBA substrates are seen to exhibit surface roughening during thermal cycling, [53] they are a promising solution for sintered silver bonds and high temperature wide-bandgap devices. [59], [77].
4.3 STACKED SUBSTRATE RELIABILITY

4.3.1 Background

One of the techniques for improving insulating substrate performance is to bond substrates in a multi-layer geometry [50], [58]. High voltage modules can produce high electric fields in excess of the insulating capabilities of a single ceramic layer [24]. By bonding two ceramic substrates in a multi-layer configuration, the module can grade the electric field across the substrate stack and reduce the peak electric field at the triple points [18], [21].

However, bonding two or more substrates to create this stacked configuration raises the need for a very large area bond. This thesis presents modeling and experimental evaluation of a large-area, low pressure-assisted bonding method for two-layer aluminum nitride (AlN) DBA substrates using sintered silver.

4.3.2 Existing Reliability Research for Stacked Substrates

Most of the thermal and thermomechanical analysis in this thesis centers on the design presented in [21] and the two-layer DBA substrates in a 10 kV silicon carbide (SiC) MOSFET package. The module design utilizes vias, as well as the stacked, multi-layer substrate approach to implement electric field grading and a common-mode screen for operation at the high voltage and switching speeds enabled by SiC MOSFETs. The two-layer DBA substrates are also in the primary heat conduction path of the module. The two-die, half bridge power module of this design is pictured in Fig. 19. This module was fabricated in part using large-area sintering techniques discussed in detail in Chapter 3 of this thesis. Thermal resistance measurements of the module structure are also presented in that chapter, and compared to the current state-of-the-art.
A cooling scheme for this module is presented in [70], where liquid coolant is directly impinged on the bottom surface of the two-layer DBA stack. This emphasizes the need for a low thermal resistance, high reliability bond to make this substrate geometry a viable solution for high voltage power modules. Thermal resistance of the two-layer DBA stack is also discussed in Chapter 3 of this thesis.

Other investigations have studied the viability and efficacy of sintered silver as a large-area bond [33], however, thorough reliability investigation has not been performed to evaluate the this methods. This chapter discusses modeling the effects of cyclic thermal cycling on the sintered silver bonded two-layer DBA substrates in a 10 kV SiC power module.

4.4 TEMPERATURE PROFILE SELECTION

The temperature profile for thermal cycling tests applies an accelerated stress condition to extrapolate lifetime reliability behavior from samples. By transitioning promptly from one temperature extreme to another in a controlled manner, a lifetime of cyclic stress can be emulated much more quickly. This is done by increasing the temperature peaks experienced by the samples during thermal cycling to amplify the stress of thermal expansion, fatiguing the sample more rapidly. It is important to avoid inducing artificial failure mechanisms with increased temperature stress that are not possible with normal operating temperatures. For example, the annealing temperature of aluminum is between 200 and 400 °C. Heating aluminum above this temperature will cause plastic deformation in the crystalline structure of the metal and can change the fatigue behavior of the metal [53]. If the application of the samples under test will never reach 200 °C or greater, it is inappropriate to test their reliability with an accelerated thermal stress above that temperature.

The temperature profile for the thermal cycling tests in this investigation is determined based on a survey of existing literature on silver sintering reliability combined with a careful
consideration of the applications of MV power devices (specifically SiC). Literature was reviewed on both single and stacked ceramic substrate thermal cycling tests to survey the most severe conditions studied on different geometries. Table III below summarizes a literature review of thermal cycling tests by organizing the temperature profiles by ceramic material type, substrate geometry, and substrate metallization.

It was found through literature that the dwell time at peak temperatures was largely inconsequential to the thermal cycling performance. Provided samples are given adequate time to heat and cool evenly at temperature extremes to avoid thermal shock, any dwell time can be selected. To the best of the author’s knowledge, no other thermal cycling tests have been performed on stacked substrates bonded with silver sintering. Additionally, With the consideration that SiC devices are a favorable choice for applications that exceed 200 °C in operating temperature, it is appropriate to reach that peak temperature in thermal cycling of DBA substrate stacks. For the purpose of comparison with other works with single substrates bonded to copper baseplates, [25], [56], [78], as well as those on stacked ceramic substrates bonded by soldering, [50] a temperature profile of –40 °C to 200 °C is selected for stacked DBA substrates bonded by silver sintering. A ramp rate of 6.45 °C/min is selected for the heating step of the profile with a rate of 7.75 °C/min for the cooling step.

Fig. 24 shows a simulated plot of the temperature profile with smoothed temperature transitions near the peak temperatures to avoid overshoot or undershoot of the temperature. A

<p>| Table III: Summary of Thermal Cycling Literature for Single and Stacked Ceramic Substrates |
|----------------------------------------|------------------------------|-----------------|-------------------|</p>
<table>
<thead>
<tr>
<th>Stacked (Y/N)</th>
<th>Ceramic Material</th>
<th>Metallization</th>
<th>Temperature Profile</th>
</tr>
</thead>
<tbody>
<tr>
<td>N</td>
<td>AlN</td>
<td>DBC</td>
<td>0 °C to 350 °C[37]</td>
</tr>
<tr>
<td>N</td>
<td>Al2O3</td>
<td>DBC</td>
<td>-55 °C to 250 °C[53]</td>
</tr>
<tr>
<td>N</td>
<td>Si3N4</td>
<td>DBC</td>
<td>0 °C to 350 °C[37]</td>
</tr>
<tr>
<td>Y</td>
<td>AlN</td>
<td>DBC</td>
<td>-55 °C to 195 °C[50]</td>
</tr>
<tr>
<td>Y</td>
<td>Si3N4</td>
<td>DBC</td>
<td>-55 °C to 195 °C[50]</td>
</tr>
</tbody>
</table>
dwell time of 5 minutes is selected to provide adequate time for any temperature variation in the sample to settle.

4.5 SAMPLE POPULATION FOR RELIABILITY TESTING

A sample population varying process conditions and sintering methods was created. During the evaluation of the sintering process described in Chapter 3.2, substrate stacks were kept after C-SAM imaging regardless of perceived bond quality. Three variables were adjusted during sample preparation (bonding method, sintering pressure, and cooling pressure) to examine the effects of each on thermomechanical reliability. Table IV describes the sample population and the variation of assembly parameters investigated through this testing.

![Temperature Profile](image)

**Fig. 24:** Plot of the temperature profile for thermal cycling tests of DBA substrate stacks
Sample pressure was varied from 1 MPa to 3 MPa in an effort to keep pressure assistance as minimal as possible. Cooling of nano-silver paste samples under pressure was maintained for all samples fabricated due to previous works detailing warping of substrates post-bonding [18].

C-SAM images of nano-silver preform samples sintered with 3 MPa pressure (Fig. 25) showed the highest uniformity from sample to sample. Additionally, the cooling pressure for samples sintered with nano-silver preform did not affect the C-SAM scan uniformity, nor did it yield any noticeable issues with sample warping. Samples were not fabricated with higher sintering pressure than 3 MPa as higher sintering pressure has been known to cause cracking in larger substrates with vias [18].

<table>
<thead>
<tr>
<th>Sample</th>
<th>Bonding Method</th>
<th>Sintering Pressure</th>
<th>Cooling Pressure</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Paste</td>
<td>1 MPa</td>
<td>1 MPa</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>1 MPa</td>
<td>1 MPa</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>1 MPa</td>
<td>1 MPa</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>1 MPa</td>
<td>1 MPa</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>1 MPa</td>
<td>0 MPa</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>3 MPa</td>
<td>3 MPa</td>
</tr>
<tr>
<td>7</td>
<td></td>
<td>3 MPa</td>
<td>3 MPa</td>
</tr>
<tr>
<td>8</td>
<td></td>
<td>3 MPa</td>
<td>3 MPa</td>
</tr>
<tr>
<td>9</td>
<td></td>
<td>1 MPa</td>
<td>0 MPa</td>
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<td>10</td>
<td></td>
<td>3 MPa</td>
<td>0 MPa</td>
</tr>
<tr>
<td>11</td>
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<td>3 MPa</td>
<td>3 MPa</td>
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<td>12</td>
<td></td>
<td>3 MPa</td>
<td>0 MPa</td>
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<td>13</td>
<td></td>
<td>3 MPa</td>
<td>0 MPa</td>
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<tr>
<td>14</td>
<td></td>
<td>3 MPa</td>
<td>0 MPa</td>
</tr>
<tr>
<td>15</td>
<td></td>
<td>3 MPa</td>
<td>0 MPa</td>
</tr>
</tbody>
</table>
4.6 NON-DESTRUCTIVE ANALYSIS

Samples were periodically removed from the thermal cycling chamber at regular intervals to scan with C-SAM. A small, sub-group of samples 3, 12, 14, and 15 were selected to scan after every 50 thermal cycles while the remainder of the population was scanned every 100 thermal cycles. While C-SAM was an effective method for evaluating samples in their initial, as-sintered state, high quality images were difficult to collect reliably during thermal cycling. C-SAM uses

Fig. 25: C-SAM images of samples sintered with nano-silver preform and 3 MPa sintering pressure
the reflection from acoustic waves projected onto a sample through a water bath to read changes in the density of the sample. This is an effective way to identify voids, cracks, or other low-density regions in a variety of planar electronic packages. However, focusing the beam of the ultrasonic transducer is not trivial. Even the most sophisticated acoustic microscopes can have trouble focusing on samples with complex, multi-layer structures and surface inconsistencies [79].

The C-SAM images of nano-silver paste samples in Fig. 26 show some of the distortion

![Image](image_url)

(a)

(b)

(c)

Fig. 26: C-SAM images of DBA stacks bonded with nano-silver paste after 100 thermal cycles from --40 °C to 200 °C
observed after just 100 thermal cycles from –40 °C to 200 °C. Cross-sectioning and analysis of these and some nano-silver preform samples will suggest that the surface roughening phenomenon experienced by DBA substrates [35], [37] is to blame for the poor image quality as the roughened surfaces scatter the acoustic beam. Additional processing of the samples was performed by sanding away the silver- and nickel-plating layers, as well as fully removing the aluminum metal of the substrate to attempt and simplify the imaging process. None of these attempts were successful, and the C-SAM images remained difficult to repeat.

Due to the challenges experienced with C-SAM, other non-destructive methods were investigated to monitor bond degradation during thermal cycling. Pursuing another imaging technique was intended to provide a reference to correlate the artifacts seen in the C-SAM with more reliable imaging. CT scan and 3D X-ray were identified as potential methods for analysis.

Fig. 27: CT scan image of the sintered silver bulk in DBA stack sample #14
Private 3D X-ray imaging services were investigated as NREL was unable to perform this examination. Upon receipt of quotes for these services, 3D X-ray was disqualified on the basis of excessive cost. Instead, a cheaper analysis procedure was pursued by utilizing the Colorado School of Mines’ CT scanner. Sample #14, bonded with nano-silver preform, was imaged via CT scan to evaluate the quality of the sintered silver interface after 250 thermal cycles. The scan revealed micro-cracks in the sintered bond, shown in Fig. 27, but no large cracks or delamination. It is unclear whether the micro-cracks are a consequence of thermal cycling, or are an artifact from the residual stress from sintering the DBA stack. Since this method is largely inconclusive in identifying failures or degradation, other methods of non-destructive analysis were pursued.

The sample is also placed on a profilometer to check for any warping of the substrate. After 250 thermal cycles, ±15 µm of warping is observed along the length of the substrate (Fig. 28). This is similar to the warping observed after substrates were sintered in a previous work [18], and is therefore inconclusive of any sign of sample degradation. With these methods of non-destructive analysis exhausted, it was decided to move on to destructive methods of analysis.

Fig. 28: Profilometer scan of DBA stack sample 14 after 250 thermal cycles
at regular thermal cycling intervals.

4.7 DESTRUCTIVE FAILURE ANALYSIS

The 15 samples in this investigation are selected at regular but increasingly distant numbers of thermal cycles for destructive analysis. When a sample is ready for analysis, it is cast in an epoxy resin and cut into cross-sections with a dicing saw. Fig. 29 shows the labeled sections of a sample after casting and dicing.

Samples are then polished with a diamond slurry with a mean particle diameter of 20 µm to remove any surface defects. Polished samples are then imaged with an optical microscope at 100X magnification. Optical microscopy is adequate for a qualitative analysis of the sintered bond, but does not provide enough resolution to analyze the microstructure or porosity of the sintered bond. Most critically, these optical microscope images are used to examine the progression of surface roughing within the bonded interface of the DBA stack.

4.7.1 Surface Roughness Calculation

This analysis is performed according to the methodology detailed in Fig. 30. The first

Fig. 29: Cross sections of a DBA stack, cut from a thermally-cycled sample cast in epoxy resin
The step in the analysis is to calibrate the image to set a scale. Because the thickness of the insulating ceramic does not change during thermal cycling, and is always a constant 1 mm thickness, this geometry can be used to set a scale for the image.

The open source software ImageJ is an effective tool for this image processing analysis. At 100X magnification, the scale for processing these DBA stacks is 2.25 µm/pixel. Once the scale is set, the DBA surface can be isolated in the cross-section image for surface roughness calculation. This isolation can be performed using image analysis because of the darker, nickel-plated layer that exists in optical images of the DBA stack cross-section. First, the image is converted to a 32-bit grayscale image using a built-in ImageJ tool so only the contrast of the image is used to distinguish between pixels. Next, another tool used to enhance the contrast of the image is utilized to further separate the grayscale of the nickel layer from the rest of the image. Once contrast is enhanced, the final step is to adjust the image threshold based on a window of grayscale values. Setting the threshold forces pixels outside of the threshold to a 32-bit grayscale value of either 0, or 255. If prior process steps have been executed correctly, the entire nickel layer should exist within a narrow band of 32-bit grayscale values. Setting the threshold is trivial and can be done manually through ImageJ. The result of this process is shown in Fig. 31 with the nickel layer of one DBA surface selected in a red outline.
This surface is planar at the time of sintering the stack, so any deviation from a straight line will indicate surface roughening. Mean surface roughness is calculated on the DBA surface using MATLAB. The X and Y coordinates of the nickel-plated DBA surface can be exported from ImageJ into MATLAB to measure the surface of the DBA. First, the average value of the DBA surface is calculated. Next, the distance from this average Y value is calculated for each X-coordinate point on the DBA surface. This difference is referred to as the normalized surface roughness. The normalized surface roughness plot can then be averaged to determine the mean surface roughness for the entire sample. This analysis is performed on DBA samples cross-sectioned after 0, 300, 400, and 500 thermal cycles to track changes in surface roughness during thermal cycling.

Fig. 31: Black and white image of a DBA stack cross-section with the nickel-plated surface selected in a red outline
Table V is a summary of the mean surface roughness calculated for both nano-silver preform and paste samples at these cycling milestones.

It is worth noting the high initial surface roughness of both the nano-silver paste and preform samples. It is possible this roughening is caused by the residual stress of sintering the sample, which is then allowed to anneal during the first few hundred thermal cycles. This is supported by the fact that the thermal cycling profile reaches the lower bound of the annealing temperature of aluminum: 200 °C [53]. The overall trend presented in Table V suggests that the surface roughening phenomenon is two-fold worse for nano-silver paste samples than for nano-silver preform. This could be induced by the thicker bond in the nano-silver paste samples. The thicker, porous silver in samples bonded with nano-silver paste could experience more deformation, allowing the aluminum surface to roughen. Specifically, the surface roughness for nano-silver paste samples was between 1.93 and 2.17 times more severe than a nano-silver preform sample cross-sectioned after the same number of thermal cycles. This relationship is best observed

<table>
<thead>
<tr>
<th>Bonding Method</th>
<th>No. of Thermal Cycles</th>
<th>Mean Surface Roughness (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Preform</td>
<td>0</td>
<td>7.5</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>4.6</td>
</tr>
<tr>
<td></td>
<td>400</td>
<td>6.0</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>5.3</td>
</tr>
<tr>
<td>Paste</td>
<td>0</td>
<td>7.9</td>
</tr>
<tr>
<td></td>
<td>300</td>
<td>9.9</td>
</tr>
<tr>
<td></td>
<td>400</td>
<td>11.6</td>
</tr>
<tr>
<td></td>
<td>500</td>
<td>11.3</td>
</tr>
</tbody>
</table>
visually in Fig. 32 and Fig. 33 where normalized surface plots of the nano-silver paste samples are compared to those of the nano-silver preform. A 3.3 mm length of the DBA bond is selected arbitrarily as the surface roughening is fairly uniform across the length of the DBA cross-section. Despite this increased surface roughening, none of these samples (Samples 1-3, sample 10, and samples 12-15) have exhibited signs of failure after 500 thermal cycles. Optical microscope images of these samples’ cross-sections are shown in Fig. 34 and Fig. 35. These images confirm that there are no severe cracks or voids present in the sintered silver bond or the aluminum metal of the DBA stack.
Fig. 32: Normalized surface plots of preform DBA stacks cross-sectioned after different thermal cycling intervals
Fig. 33: Normalized surface plots of paste DBA stacks cross-sectioned after different thermal cycling intervals
The sintered silver bonds are largely free of voids with the exception of the sample in Fig. 35b, which has a void of roughly 80 µm in diameter. However, with the presence of micro-

![Fig. 34: Optical microscope images taken from nano-silver paste samples at 300 (a), 400 (b), and 500 (c), thermal cycles from –40 °C to 200 °C](image1)

![Fig. 35: Optical microscope images taken from nano-silver preform samples at 300 (a), 400 (b), and 500 (c), thermal cycles from –40 °C to 200 °C](image2)
cracks in the CT scan discussed in Chapter 4.5, it is necessary to verify the bond quality of these cross-sectioned samples with more sophisticated imaging.

SEM images are taken of a nano-silver preform sample cross-sectioned after 500 thermal cycles to confirm the conclusions drawn from optical microscope images. The sample, pictured in Fig. 36, shows a small crack roughly 120 µm in length that could be the initiation site of an adhesive failure. Otherwise, the silver bond is intact and appears free of severe degradation. This is confirmed further through Energy Dispersive X-ray Spectroscopy (EDS), which maps the material composition of the SEM image to a color code as shown in Fig. 37. The EDS image shows a clear, uniform, sintered silver bond. The aluminum metal and nickel plating have not diffused or otherwise encroached into the silver layer.

Fig. 36: SEM image of a multi-layer DBA sample after 500 thermal cycles from –40 °C and 200 °C
Fig. 37: EDS analysis of a DBA sample cross-section after 500 thermal cycles showing location of silver (a), aluminum (b), and nickel (c) in the SEM image.
The microstructure of the sintered silver is unfortunately not clearly visible in Fig. 36 due to scratching of the surface from the diamond slurry polishing.

Another surface preparation method was needed to establish better planarity of the cross-section. Ion milling is selected as it is an effective method of sample planarization without leaving residue on the sample surface [80]. Fig. 38 shows the same sample after 2 hours of

![SEM image of a DBA stack after 500 thermal cycles from –40°C to 200°C at magnifications of 1000x (a) and 2000x (b)](image)

Fig. 38: SEM image of a DBA stack after 500 thermal cycles from –40°C to 200°C at magnifications of 1000x (a) and 2000x (b)
milling at 6 kV under a focused ion beam. The microstructure of the sintered layer is significantly clearer and the bond has showed a high level of resilience to the cyclic thermal stress. No signs of fatigue are visible.

A porosity analysis was performed on Fig. 38b at NREL using an image processing software. The volume fraction of porosity in the sintered sample is estimated to be 4 %, significantly lower than the as-sintered sample discussed in Chapter 3. Additionally, none of the voids shown in Fig. 18 are present in the SEM images in Fig. 38. Analysis must be performed on more as-sintered samples to identify the source of the voiding in question. It is clearly possible, however, to fabricate a very high-quality sintered bond with low voiding as evidenced by the sample in Fig. 38. Additional research must be performed to ensure that any variation in the sintered bond induced by the sintering process is mitigated.

If the sintering process can be made consistent, this is a very encouraging result. When compared to existing literature on as-sintered measurements of porosity, other examples have a much higher pore volume fraction even before any thermal cycling stress. In [30], it is shown that sintered silver with a volume fraction of porosity less than 10 % will closely approximate the thermal conductivity of bulk silver (~410 W·m⁻¹·K⁻¹). In [81], large area samples are only able to achieve a porosity of 7.73 % immediately after sintering. In [65], porosity of large area bonds is much higher at 17.6 %, highlighting the difficulty of achieving a reliable, high quality bond.

4.7.2 Failure Analysis

This reliability investigation defines failure as any cracking or voiding that exceeds 20% of the bonded area or, when examining cross-sections, 20% of the length of the bond (similar to the criteria defined in [61]). Because no failures are observed after 500 thermal cycles, samples are advanced to 1000 thermal cycles of stress with the intent of inducing a failure. Optical
microscope images are perfectly effective at finding failures. Cracks or voids are clearly identifiable through visual inspection of the high-quality optical microscope images.

Fig. 39 shows the first cross-sections of a sample exhibiting clear signs of failure after

![Optical microscope images of a DBA stack sample cross-sectioned after 1000 thermal cycles of -40 °C to 200 °C](image)

**Fig. 39**: Optical microscope images of a DBA stack sample cross-sectioned after 1000 thermal cycles of -40 °C to 200 °C

![Optical microscope images of a DBA stack sample cross-sectioned after 1500 thermal cycles of -40 °C to 200 °C](image)

**Fig. 40**: Optical microscope images of a DBA stack sample cross-sectioned after 1500 thermal cycles of -40 °C to 200 °C
1000 thermal cycles. The bonded area of the sample in Fig. 39 has delaminated along 28% of the interface between the DBA and sintered silver. Most failures are adhesive in nature, although some cracks have propagated perpendicular to the bonded interface.

Table VI summarizes the results of thermal cycling. After 1500 thermal cycles, all remaining samples showed signs of adhesive failure and cracking. Cracks are wider and more severe in both the planar and transverse direction when compared between samples at 1000 cycles and 1500 cycles. Comparing samples 9 and 11, (Fig. 39 and Fig. 40) the failure fraction is 1.82 times greater at 1500 cycles than at 1000 cycles. There is no clear trend with respect to bond failure fraction and the number of thermal cycles or the bonding method of the multi-layer stack. More data is needed to confirm that the initial bond quality of all samples in the population is equal. Additional samples will need to be fabricated and thermally cycled to estimate the lifetime of stacked DBA substrates bonded with these nano-silver materials. However, these results are

**Table VI: Summary of thermal cycling results**

<table>
<thead>
<tr>
<th>Sample</th>
<th>Bonding Method</th>
<th>Sintering Pressure (MPa)</th>
<th>Cross-Section Cycle Number</th>
<th>Bond Failure Fraction</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Paste</td>
<td>1</td>
<td>300</td>
<td>0 %</td>
</tr>
<tr>
<td>2</td>
<td></td>
<td>1</td>
<td>400</td>
<td>0 %</td>
</tr>
<tr>
<td>3</td>
<td></td>
<td>1</td>
<td>500</td>
<td>0 %</td>
</tr>
<tr>
<td>4</td>
<td></td>
<td>1</td>
<td>1500</td>
<td>10 %</td>
</tr>
<tr>
<td>5</td>
<td></td>
<td>1</td>
<td>1500</td>
<td>38 %</td>
</tr>
<tr>
<td>6</td>
<td></td>
<td>3</td>
<td>1500</td>
<td>0 %</td>
</tr>
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<td>3</td>
<td>1500</td>
<td>4 %</td>
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<td></td>
<td>3</td>
<td>1000</td>
<td>43 %</td>
</tr>
<tr>
<td>9</td>
<td>Preform</td>
<td>1</td>
<td>1000</td>
<td>28 %</td>
</tr>
<tr>
<td>10</td>
<td></td>
<td>3</td>
<td>500</td>
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<tr>
<td>15</td>
<td></td>
<td>3</td>
<td>300</td>
<td>0 %</td>
</tr>
</tbody>
</table>
encouraging, since no failures are observed before 1000 thermal cycles and samples 4, 6, and 7 survived 1500 thermal cycles without exceeding the 20 % bond failure threshold.

The evolution of the sintered silver microstructure during thermal cycling is also of interest in failure analysis. SEM images are also taken of samples 9 and 11 to correlate any changes in the microstructure with their bond failure fraction. Generally, sintered silver increases in porosity over its operating lifetime as a die attach or bonding material [82]. The same is true for the sintered silver bonds imaged in this investigation.

Fig. 41 and Fig. 42 show the SEM images of samples 9 and 11. It is not immediately clear if sample 11 has a higher voiding fraction than sample 9, even though sample 11 has

![SEM Image](image_url)

**Fig. 41**: SEM image of sample 9, a DBA stack sintered with nano-silver preform, cross-sectioned after 1000 thermal cycles
experienced 500 more thermal cycles. Porosity analysis estimates provided by NREL confirm this analysis, estimating a void fraction of 26% for sample 9 and 44% for sample 11. Porosity values for these samples are calculated without including the area of the voids from cracking and delamination.

There are also voids present in the aluminum metal of Fig. 42, similar to those observed in Fig. 18. It is unclear whether these voids have impacted thermal cycling performance of the sintered silver bond. Regardless, any voids in the metal layers of the DBA stack will diminish thermal performance, and future work should aim to mitigate voids in both the sintered silver and

Fig. 42: SEM image of sample 11, a DBA stack sintered with nano-silver preform, cross-sectioned after 1500 thermal cycles
the DBA metal. Even with the presence of voids in some of the samples, these large-area sintered bonds show similar reliability to investigations on smaller areas of silver sintering as seen in literature [63], [77], [82]. Provided the sintering process can be adjusted to reduce the presence of defects in the aluminum and sintered silver, it is a promising solution for MV power modules.
CHAPTER 5: SILVER SINTERING IMPLEMENTED IN A DOUBLE-SIDE COOLED POWER MODULE

5.1 INTRODUCTION

Thermal management strategies for MV power modules are increasingly critical as new devices develop the capability to operate at higher temperatures and power densities. In addition to incorporating materials with higher thermal conductivity, [83], [84] it is necessary to reimagine the structure of the power module. Innovations in planar module structures have been enabled by silver sintering, as the sintering temperature (between 200 °C and 300 °C) is significantly lower than the melting temperature (~960 °C) after sintering [32]. This means the module can go through multiple processing steps without melting or softening the bonded joints within the module. Thus, both sides of the package can be sintered to the power devices, allowing a cooling interface to the top and bottom of the power devices.

This chapter will review the design, fabrication, and testing of a double-sided cooled power module for 6.5 kV operation. Discussion of the challenges faced with this assembly will also be addressed, as residual stresses from fabricating the dual-sided structure resulted in unexpected, time-zero failures. A potential solution utilizing low-pressure assisted sintering is proposed to mitigate the high residual stress from fabrication.

5.1.1 Literature Review on Double-Sided Cooled Power Modules

Double-sided cooling is an effective way to increase the power density of a module design by dramatically reducing the overall thermal resistance of the package. In [85], double-sided cooling of a power module was found to have a 37 % improvement in total overall thermal resistance when utilizing AlN substrates (thermal conductivity of 285 W/m·K), and a 15 % improvement for Si3N4 substrates (thermal conductivity: 18.5 W/m·K). These results agree with
a finite element simulation of the thermal performance of that module design, which predicted a 15-42% reduction in resistance utilizing double-sided cooling [86]. An even greater thermal resistance improvement of 45% – 60% was achieved in another work by embedding the power device in the package [87].

Other research found that a double-sided cooled flip-chip package experienced a maximum junction temperature reduction of 55% while increasing the maximum power dissipation by 76% as compared to single-sided cooling [88].

Another investigation carefully analyzed the effect of porosity of sintered silver joints on the performance of a double-sided cooled power package [30]. Porous sintered silver layers were simulated to evaluate the effect of their reduced thermal conductivity on the overall thermal resistance of the package. Even with the reduced thermal conductivity of the porous silver, double-sided cooling produced a 45% thermal resistance decrease in the module design.

Current research has indicated that double-sided cooling is an excellent solution for reducing the overall thermal resistance of a planar package structure. When designed properly, the thermal design of double-sided cooling is an excellent complement to thoughtful electrical

Fig. 43: Cross-sections of a conventional power module structure using wire bond connections (a) and a double-sided cooling structure using "bump" interconnects [85]
This enables a new level of advanced package performance for MV power modules [89].

5.1.2 Design Specifications for a 6.5 kV SiC Power Module

A Statement of Project Objectives (SOPO) was written to define the operating conditions and size of the 6.5 kV module. First, a discrete device demonstration of the package was requested, with maximum dimensions of 5 x 5 x 1.5 cm³. The operating conditions for this device are summarized in Table VII.

Table VII: Performance objectives for a thin, 6.5 kV SiC MOSFET package

<table>
<thead>
<tr>
<th>Operating Condition</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Off-state blocking voltage</td>
<td>6.5 kV</td>
</tr>
<tr>
<td>Current capacity</td>
<td>25 A</td>
</tr>
<tr>
<td>Dimensions</td>
<td>5.0 x 5.0 x 1.5 cm³</td>
</tr>
<tr>
<td>Package parasitic inductance</td>
<td>5 nH</td>
</tr>
<tr>
<td>Heat flux</td>
<td>230 W/cm²</td>
</tr>
<tr>
<td>Maximum junction-case ΔT</td>
<td>30 °C</td>
</tr>
<tr>
<td>Continuous operating junction temperature</td>
<td>150 °C</td>
</tr>
</tbody>
</table>

To demonstrate this package, a 3rd generation 10 kV SiC MOSFET from Wolfspeed is selected as the rating of the device is capable of exceeding the performance specifications in Table VII. The MOSFET is 8.1 mm x 8.1 mm in area, so the power loss from the device at the heat flux specified in the SOPO is 150 W. These performance specifications have informed the simulations used in the co-design approach of this package design.

5.2 ITERATIVE CO-DESIGN APPROACH

The strategy for designing this package is an iterative approach based on cooperation between two designers. The author of this thesis chose to manage thermal design of the package while another student provided parasitic electrical and electrostatic modeling support. To begin, an initial draft of the package design is created using CAD software. The electrostatic
performance of the initial design is simulated and recorded for different variations of the insulating substrate and metal trace patterns in the package. In parallel, a representative model of the package is created in ANSYS Workbench to compare the tradeoffs of different material options for internal package components. Next, the initial CAD layout of the package design is simulated by the author to examine the effect of the electrostatic design considerations on the thermal performance. Tradeoffs are discussed between the two designers and the next CAD layout of the package is designed. This process continues iteratively until a package design is optimized with respect to the electrical and thermal parameters of the SOPO. An overview of this design process is shown in Fig. 44.

5.2.1 Electrostatic Design

The design of the insulating substrate of this package is first completed to manage the high electric fields from 6.5 kV operation. The lateral interconnects, insulating ceramic, and any electrically conductive elements in the stack-up of the package must be considered so that partial discharge is avoided during high voltage testing [22], [90].

![Diagram of the Co-Design Approach](image-url)
Ultimately, 2 design options for the insulating substrate were presented to the author to evaluate for thermal performance. Either a multi-layer stacked substrate could be employed to allow full encapsulation of the closest insulating ceramic layer, or a metal baseplate could be boned via sintering to allow this encapsulation. Those options are presented in Fig. 45 and their thermal simulations are discussed in 5.2.2. Labeled dimensions and sense points have been varied to minimize the peak electric field within the module’s triple points. The electrostatic performance of these designs is largely independent of material selection for the insulating ceramic, which allows for additional freedom in the design of the package stack.

Option 1 is immediately disqualified, as the triple point at “s3” measures an electric field gradient exceeding the dielectric breakdown strength of air (3kV/mm) [90]. Options 2 and 3 are electrostatically viable, as none of the measured triple points exceed the electric field strength that would cause a breakdown event in either the open air or the encapsulant. Option 2 and 3 both require a large-area sintered bond to attach the baseplate or second substrate. Additional electrostatic simulations showed that Option 3 is most effective at diminishing electric field at the trip points in air when x₂ > x₁. All thermal simulations results shown in section 5.2.2 for Option 3 have x₁ = 0.9 mm and x₂ = 1.8 mm. A selection of the superior option can be made by analyzing the performance tradeoff in thermal resistance and heat spreading presented by both

![Fig. 45: Substrate design options for 6.5 kV operation](image)
substrate geometries.

Fig. 46 shows a top-down view of the bottom substrate pattern with the 10 kV MOSFET location. It was found during ANSYS Q3D parasitic electrical simulations that the placement of the die was largely inconsequential to the overall inductance of the package. The die was therefore placed relative the edge of the substrate based on an optimal location for the thermal performance of the package. The dimension labeled “$y_1$” was varied in and simulated in ANSYS workbench. Results will be discussed in 5.2.2 with other options for thermal design.

5.2.2 Thermal Design

A representative model is drawn in ANSYS Workbench to qualitatively compare the thermal performance of the substrate variations presented in section 5.2.1. Fig. 47 shows an

![Fig. 46: Top-down view of the lower substrate design of a 6.5 kV double-sided cooled package](image)
image of the model with dimensions. The pictured model displays Option 3 for the substrate geometry, but other variations with Option 2 were examined as well. The encapsulant for the model is simulated as a silicone gel with a thermal conductivity of $0.2 \text{ W/m} \cdot \text{K}$ [91]. The 10 kV SiC MOSFET is placed in the middle of the representative geometry and assigned as the source of heating for the module. A convective heat transfer coefficient, “h” is applied to the top and bottom surfaces of the double-sided package and varied from 1500 W/m$^2$·K to 9000 W/m$^2$·K.

For Option 2, two ceramic thickness options are examined:

A. Dual, identical, 1 mm substrates bonded together

B. One 1 mm-thick substrate bonded to one 0.381 mm-thick substrate

Option 2B requires that the 1 mm ceramic in the stack be bonded directly to the 10 kV SiC MOSFET while the 0.381 mm ceramic be bonded to the opposite face of the 1 mm-thick insulator. This is so the closest insulating ceramic to the high electric fields produced by the device is the thicker of the two insulators in the multi-layer stack.

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**Fig. 47:** A representative model of the double-sided cooled package structure for thermal simulations of different substrate geometries. The Isometric View shows the top substrate assembly as transparent to show the position of the 10 kV MOSFET.
Materials for the post interconnects and insulating ceramic are selected for the best available thermal conductivity. Table VIII shows a summary of the materials selected with their thermal conductivities. The maximum temperature within the body of the SiC die is plotted against the h-value for each of the substrate configuration options. Fig. 48 shows the results of the simulation. The substrate-copper baseplate configuration shows the most promising thermal performance, with a 7% reduction in peak junction temperature ($T_j$) at the h-value of 4000 W/m²·K. It is also noteworthy that the stacked substrate configuration for Option 2A (dual substrates of 1 mm thickness) has better thermal performance than Option 2B (1 mm-thick substrate bonded to 0.381 mm-thick substrate). This indicates that the thermal conductivity of AlN is high enough that the lateral heat dissipation of the ceramic is a valuable contribution to the overall thermal conductivity of the package.

### Table VIII: Summary of material thermal conductivities for thermal modeling a representative package geometry

<table>
<thead>
<tr>
<th>Material</th>
<th>Package Components</th>
<th>Thermal Conductivity</th>
</tr>
</thead>
<tbody>
<tr>
<td>AlN</td>
<td>Insulating ceramic substrates</td>
<td>170 W/m·K</td>
</tr>
<tr>
<td>Al</td>
<td>Substrate metal traces</td>
<td>210 W/m·K</td>
</tr>
<tr>
<td>SilGel 612</td>
<td>Encapsulant</td>
<td>0.2 W/m·K</td>
</tr>
<tr>
<td>Cu</td>
<td>Post interconnects</td>
<td>390 W/m·K</td>
</tr>
<tr>
<td>SiC</td>
<td>10 kV MOSFET</td>
<td>370 W/m·K</td>
</tr>
</tbody>
</table>
The results in Fig. 48 clearly indicate that the optimal thermal design of those examined is Option 3. Now that an optimal substrate design is selected, modeling of a specific package layout can be discussed. First, the ideal die placement onto the bottom substrate stack must be established. The offset $x_1$ in Fig. 46 is varied and steady-state thermal simulations are executed with the same $h$-value bounds as Fig. 48. The results are shown in Fig. 49 and show that the

![Graph showing Max $T_j$ vs. heat transfer coefficient for different substrate geometry choices in a 6.5 kV double-sided cooled package](image)

**Fig. 48**: Max junction temperature vs. heat transfer coefficient for different substrate geometry choices in a 6.5 kV double-sided cooled package
optimal placement of the die is 2 mm from the edge of the metal trace.

With the placement of the die within the package determined, layout can be finalized. Fig. 50 shows an isometric view of the finalized package with the top baseplate and insulation layer removed to show the metal traces.

Fig. 49: Maximum junction temperature vs. heat transfer coefficient for different locations of the SiC MOSFET within its double-sided cooled package

Fig. 50: An isometric view of the finalized 6.5 kV SiC MOSFET package layout
This final layout was simulated across the same boundary conditions. To confirm the design is viable for prototyping, a moderate $h$ of 4500 W/m$^2$·K is selected. Commercially available cold plates capable of achieving this heat transfer coefficient are identified from Custom Thermoelectric [92], [93]. Two potential solutions and their respective thermal resistances are shown in Fig. 51.

**Fig. 51: Cold plate thermal resistances[92], [93]**
Steady-state thermal simulations are performed on this layout using the substrate stack configuration from Option 3. Fig. 52 and Fig. 53 confirm that the conditions from Table VII are met with the selected $h$ of 4500 W/m²·K.

**Fig. 52:** Cross-section view of a steady-state thermal simulation of the finalized, double-sided cooling package design.

**Fig. 53:** Cross-section view of the heat flux distribution in the double-sided cooled package.
Fig. 53 clearly shows a peak heat flux greater than 200 W/cm$^2$ while Fig. 52 demonstrates the peak die temperature of approximately 121.6 °C. Now that all of the design parameters are met in simulation, the package can be prototyped for testing.

5.3 UTILIZATION OF LARGE-AREA SINTERING

As mentioned in 5.2.1, a large-area sintered silver bond will be utilized to fabricate the substrate geometry for this double-sided cooled package. The bonding method utilizing nano-silver preform, described in 3.3.2, is selected. Short processing time and thinner silver bonding area makes the nano-silver preform a more preferable choice for fabricating these prototypes. 1 mm AlN DBA substrates from DOWA Metaltech are again selected as the Ni/Ag plating of the metal is sintering-compatible. Nano-silver preform is supplied by NBE Tech.

Initial copper baseplate-substrate samples were fabricated using 3 MPa sintering pressure and cooled without pressure applied. These samples immediately delaminated after cooling as the larger CTE of the copper caused it to warp away from the substrate [51]. Fig. 55 shows an

![Image of copper baseplate sintered to a DBA substrate with visible cracking at the sintered interface](image)

**Fig. 54:** Optical microscope image of a copper baseplate sintered to a DBA substrate with visible cracking at the sintered interface
optical microscope image of the baseplate-substrate interface. Visible cracks have already formed at the sintered interface. Immediately after the pictures were taken, the substrate and baseplate delaminated completely.

The sintering pressure and cooling conditions were changed to 5 MPa sintering pressure and 5 MPa of cooling pressure. This was done to ensure the copper baseplate maintained its flatness throughout the process. The result of this process change was a greatly improved sintered bond. No delamination or cracking was immediately visible at the baseplate-DBA interface. Samples using the modified, 5 MPa pressure-assisted sintering process were sent to NREL for C-SAM scanning to examine any undetected issues with the bond. Fig. 55 shows an optical microscope image of a successful substrate-DBA bonded interface.

Unfortunately, results of C-SAM images could not be reviewed in time to make necessary changes to the package structure before prototyping. Chapter 5.4 will discuss the impact of the residual stresses from this substrate geometry on the package fabrication.

![Optical microscope image of a copper baseplate-DBA bonded interface](image)

**Fig. 55: Optical microscope image of a copper baseplate-DBA bonded interface**
5.4 RESIDUAL STRESS ISSUES AND FABRICATION CHALLENGES

Fig. 56 summarizes the process of fabricating this SiC MOSFET package. From the organization of the assembly processes, it is immediately obvious how the residual stress from the baseplate-substrate assembly will affect the rest of the package fabrication steps. Each of the subsequent sintering and soldering steps will cause some degree of deformation induced by the CTE mismatch and asymmetric geometry of the copper baseplate-DBA substrate structure.

After the substrate structure is fabricated, X-type nano-silver paste from NBE Tech is screen-printed onto the surface of the bottom DBA stack. Paste is dried through open-faced contact drying at 95 °C for 15 minutes. Post interconnects and the 10 kV SiC MOSFET are then placed onto the substrate by hand and a Mark-10 force gauge is used to apply 5 MPa of pressure. Once pressure is fully applied, temperature is ramped up to 240 °C and held for 45 minutes. The sample is cooled with the pressure applied until it reaches room temperature. The result is shown in the pressure sintering step box of Fig. 56. The lower substrate assembly is soldered to the
upper substrate using a 96 % Sn, 4 % Ag solder paste. Two hot plates are used to apply the solder profile described in the third step of Fig. 56. This causes moderate cracking of the post interconnects due to the severity of the thermal shock in the solder profile (Fig. 57). Although cracking of this severity is qualified as a bond failure, package assembly continued in an effort to take experimental measurements of the prototype, despite its degradation. Lateral pin terminals were soldered to the package in a solder reflow oven using a Pb/Sn solder paste at the temperature conditions described in Fig. 56.

Unfortunately, severe delamination of the post interconnects occurred (Fig. 59) in addition to cracking and delamination at the corners of the SiC MOSFET bond (Fig. 58). This rendered the prototype too fragile for any additional stress and made it necessary to adjust the fabrication process to mitigate these thermomechanical stresses.

![Silver-plated copper interconnect post](image1)

![Cracks in sintered silver](image2)

![Ag-plated silver metal](image3)

![SiC MOSFET die](image4)

**Fig. 57:** Crack during solder reflow

**Fig. 58:** Optical microscope image of bond delamination under the SiC MOSFET
It was decided to replace the soldering process used to bond the top substrate stack to the rest of the package with a pressure-assisted sintering step. Because the package can be allowed to cool under pressure during sintering, instead of expanding and contracting freely and rapidly during the thermal shock of soldering, it is a preferable bonding technique. DBA substrates were not bonded to a copper baseplate to reduce the overall residual stress present in the module structure. This is justifiable, as other encapsulation techniques can be employed to ensure that the triple points on both sides of the substrate are encased with silicone gel. Thermal measurements presented in 5.5.2 will confirm that this is an acceptable configuration thermally as well. Additionally, a binder clip is clamped around the package during soldering of the spring-pin terminals to counteract the warping of the package during reflow. The adjusted assembly process is described in Fig. 60.

**Fig. 59: Delamination of the copper terminal block caused during soldering of spring-pin terminals**
Substituting the solder process with a pressure-assisted sintering process achieved a uniform, dense sinter joint that withstood all processing steps. Fig. 61 and Fig. 62 show microscope images of the post and die sinter bonds, confirming no visible cracks or gaps.

Fig. 60: Adjusted fabrication process overview for the double-sided cooled package
The finished package can then be fitted to a 3D printed housing and encapsulated in a silicone gel. The complete package with housing measures 3.1 x 3.2 x 0.7 cm³, which is 18.5 % of the total allowable volume of the package as defined in the SOPO. This translates to a power
density of 22 kW/cm$^3$. Fig. 63 shows the completed package both alone and mounted to twin PCB busbar interface boards for electrical testing.

5.5 EXPERIMENTAL MEASUREMENTS

5.5.1 Electrical Testing

After packaging, forward characteristics of the 10 kV SiC MOSFET are collected on a Keysight B1505A curve tracer. The SOPO defines a current rating of 25 A, so the I-V characteristics of the package are collected to that current limit. Fig. 64 shows the forward characteristics of the device after packaging.

![Fig. 64: Forward I-V characteristics of the packaged SiC MOSFET as measured on the B1505A curve tracer](image)
These results confirm that packaging was successful, bonds are high quality do not contribute high resistivity. Because 5 MPa pressure is applied to the die surface during sintering, this test is critical in confirming that the die has not suffered any internal damage. A reverse leakage characterization is performed next to ensure that both the package and device can withstand the blocking voltage of 6.5 kV specified in the SOPO. Fig. 65 shows the package mounted to its PCB busbar interface and the corresponding leakage current measured across the packaged MOSFET.

The maximum leakage measured up to 6.5 kV is within the noise margin of the measurement equipment, and does not exceed 20 nA. Therefore, we can declare the electrical testing of this package a success and move forward to thermal analysis.

5.5.2 Thermal Testing

Thermal characterization of this package is executed on the Analysis Tech Phase 12B just as with the 10 kV SiC power module analyzed in Chapter 3. Because the package is cooled through both the top and bottom of the package, resistance measurements must be taken on both sides. Then, a net package junction-to-case thermal resistance can be calculated using a thermal

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**Fig. 65: Reverse leakage measurement of the package up to 6.5 kV**
network approach as in [89]. The simple resistance network for a double-sided cooled package is drawn in Fig. 67, with \( T_j \) representing the device junction temperature and \( T_c \) representing the case temperature. The SOPO defines the operating junction temperature as 150 °C and a maximum junction-case temperature differential of 30 °C at a power loss of 150 W. It can therefore be calculated that the total package \( R_{jc} \) must be 0.2 °C/W or less.

Measurements taken on the thermal analyzer show that this has been successfully accomplished in the package prototype. The double-sided package is clamped down to the liquid-cooled plate on the bottom side first and measured as shown in Fig. 66. Measurements can be taken on an unencapsulated, unhoused package as air is an even equivalent thermal insulator to the silicone gel.

\[ \begin{align*}
T_j & \quad R_{jc,top} \quad T_c \\
R_{jc,bot} & \quad \quad \\
\end{align*} \]

**Fig. 67: Diagram of a parallel-path, double-sided cooling thermal resistance structure**

**Fig. 66: Unencapsulated double-sided cooling package mounted to the Phase 12B thermal analyzer**
After measuring the $R_{jc}$ for the bottom path, the package is flipped over and measured for the top side of the package. Fig. 68 shows the heating characterization curves recorded for the package, measuring thermal resistances of 0.253 °C/W and 0.573 °C/W for the bottom and top respectively.

Solving for the net thermal resistance of the package yields a total $R_{jc}$ of 0.17 °C/W, 15% less than the maximum acceptable value. This is further reinforced by the results of a continuous operation test, also performed on the Phase 12B using the setup pictured in Fig. 66. Continuous testing is achieved by specifying a steady-state junction temperature target to the thermal analyzer. The analyzer then monitors the junction temperature of the device under test and applies a semi-constant heating current to maintain that temperature indefinitely. The case temperature is monitored via thermocouple and plotted with the junction temperature to show that the package is continually dissipating heat as intended.

Fig. 69 shows that the double-sided package is capable of maintaining a junction

![Fig. 68: Heating characterization curves for the bottom (left) and top (right) heat flow paths of the double-sided package](image)
temperature just over 150 °C at an input power of 152 W using only single-sided cooling for an extended period of time. The test pictured in Fig. 69 is continued until 30 minutes without any disturbance to the thermal performance of the package.

With these results, the entire performance of the package has been tested and verified. All simulations match well to real-world measurements confirming the efficacy of the co-design methodology. The structural rigidity issues experienced during fabrication were mitigated by applying pressure during sintering and removing the copper baseplate to reduce CTE mismatches within the package.

Fig. 69: Continuous operation test at a constant junction temperature of 150 C
CHAPTER 6: SUMMARY

Thermomechanical simulations were performed in ANSYS Workbench to evaluate the reliability of multi-layer substrates. The mean strain energy density per thermal cycle for the bonds in stacked ceramic substrates was 45 times less than that of a conventional, power module structure. Simulations were scaled to include the entire structure of a MV power module to investigate the effect of the entire module structure on critical, large-area sintered bonds in the bottom substrate stack. No change was observed in the strain energy density accumulated per thermal cycle in the sintered silver layer when the entire module structure was simulated. Large-area, low-pressure assisted silver sintering was used to fabricate 15 multi-layer DBA substrate stacks. Substrates were subjected to 1500 thermal cycles from –40 °C to 200 °C and adhesive failures were first identified after 1000 thermal cycles. Failure analysis of the DBA stacks found that some samples had survived 1500 thermal cycles without exceeding the failure threshold of 20 % bond delamination or cracking. Thermal resistance measurements on a 10 kV SiC power module employing multi-layer DBA substrates were collected and a junction-to-case thermal resistance of 0.14 °C/W was recorded. The multi-layer stacks in the analyzed module were sintered using the same nano-silver preform bonding technique investigated in the reliability tests detailed in this thesis. Finally, A double-sided cooling structure for 6.5 kV, 25 A operation was designed, prototyped, and tested. The double-sided structure had a total thermal resistance of 0.17 °C/W and was capable of continuous operation at 150 °C while dissipating 152 W.
CHAPTER 7: CONCLUSIONS AND FUTURE WORK

7.1 CONCLUSIONS

Overall, the technologies and packaging designs in this work fulfilled their performance expectations with ease. Thermomechanical models of stacked substrate geometries compare favorably to the current state-of-the-art module which utilizes a ceramic substrate soldered to a baseplate. Models estimated mean strain energy density reductions of more than 45 times in modules with stacked substrates versus conventional power module designs.

The large-area, low-pressure assisted sintering technique discussed was able to create a high-quality, low-porosity silver bond with only 3 MPa of pressure assistance at 250 °C. DBA multi-layer substrates fabricated with this technique were capable of surviving up to 1000 thermal cycles of −40 °C to 200 °C before showing signs of adhesive failure. Thermal measurements on a power module using these multi-layer substrates recorded a $R_{jc}$ of 0.14 °C/W. This performance is excellent when compared to similar modules in both literature and available for commercial sale.

A double-sided cooling structure has been designed and prototyped for packaging a 10 kV SiC MOSFET. This design was successful in meeting its design parameters of 6.5 kV blocking, 25 A forward conduction, and a low $R_{jc}$ of 0.17 °C/W. The design can also operate at a continuous junction temperature of 150 °C at a dissipation of 152 W without difficulty. However, the original design and fabrication procedure needed modification as severe warping of the copper baseplate-DBA geometry caused time-zero failures of other bonds in the package. A 5 MPa pressure-assisted sintering process was utilized to temporarily mitigate these failures and analysis was performed to identify the root cause.
Ultimately, AlN DBA substrates were found to be a reliable, high-performance, silver sintering-compatible substrate option for MV power modules. This work suggests that utilization of silver sintering and its enabled packaging techniques will push forward MV devices forward in their power electronics applications.

7.2 FUTURE WORK

Building upon this work will require continued evaluation of the reliability of these advanced, silver-sintered module structures. Work is already underway to build planar module structures with porous sintered silver interconnects instead of the solid copper blocks with silver plating utilized in this thesis [94]. This porous structure is one potential solution for helping to relieve the rigidity of the planar package.

There is also growing commercial interest in sintered silver, with companies such as Haraeus and Kyocera providing nano-silver die attach materials in a sintered form. Haraeus mAgic PE338 is a screen-printable, pressure sintered paste that processes at 230 °C in air with a sintering pressure of > 10 MPa. It is described as “optimized for application with SiC power devices” and “suitable for SiC, GaN die attach on ceramic substrate”. However, the bonding area is limited to 15 x 15 mm.

Further reliability investigation on multi-layer substrates bonded via silver sintering are also necessary. To the author’s knowledge, the work described in this thesis is the only thermal cycling investigation on multi-layer substrates bonded with sintered silver. Future work on other multi-layer designs like DBC or AMB bonded with sintered silver will be useful in contextualizing the reliability of stacked DBAs. As of now, there is no data on other multi-layer substrates bonded with sintered silver with which to compare.

Finally, scaling the bonding area of the DBA stack to even greater sizes is necessary. The 10 kV SiC module in this investigation only packages two MOSFETs in a half bridge, and has a
bonding area of 11.27 cm². A 6-die version of this module is also designed in [18] with bonded areas of 20.92 cm², but no reliability data exists on sintered, multi-layer DBA substrates of that size. Samples fabricated in [56] are 25.81 cm² and are subjected to thermal cycling, but do not feature a multi-layer substrate design.
REFERENCES


H. Liang, J. Xue, and K. Lu, “The Auto-Focus Method on Scanning Acoustic Microscope Based on Wavelet Analysis,” in 2019 7th International Conference on Information,


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