Two-Stage Operational Amplifier Design by Using Direct and Indirect Feedback Compensations

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(ABSTRACT)

This paper states the stability requirements of the amplifier system, and then presents, and summarizes, the classic two stage CMOS Op-Amp design by employing several popular frequency compensation techniques including traditional Miller compensation, nulling resistor, voltage buffer, and current buffer. The advantages and disadvantages of all these compensation strategies are evaluated based on a standard performance which has a 70dB DC gain, a 60° phase margin, a 25MHz gain bandwidth, and a slew rate of 20 V/us requirements. All the designs and simulation results are based on a 180mm 1.8 V standard TSMC CMOS technology. Ultimately, the traditional Miller compensated Op-Amp (a single compensation capacitor amplifier) cannot meet all the requirements but all other techniques could with also a boost of performance in various aspects.

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(GENERAL AUDIENCE ABSTRACT)

Two-stage CMOS operational amplifier has two input pins and one output pin. it is used to amplify the differential inputs signal and transfer it to the output side. Usually the input signals are too weak to be processed by the rest of the system units. So the Op-Amp can amplify the weak input signals which then can either be further modified for some specific applications by the rest units of the system or be the final output of this entire system. The role of the Op-Amp in analog and digital systems is as the role of transformers in the power system. So the output signal is required to have fast and stable responses to the inputs. This paper states some standard requirements of the Op-Amp in aspects of gain, stability, and operating frequency. Due to the classic design of two-stage Op-Amp has poor performance of stability and operating frequency, some compensation techniques are applied as the feedback networks to improve its performance. These techniques include traditional Miller compensation, nulling resistor, voltage buffer, and current buffer. The advantages and disadvantages of all these compensation strategies are evaluated based on a 180mm 1.8 V standard TSMC CMOS technology.

Dedication

To my families for their support and advice.

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List of Abbreviations

ω The angular frequency

CMOS: Complementary Metal-Oxide-Semiconductor

CMRR Common mode rejection ratio

LHP: Left Hand Plane

Op-Amp: Operational Amplifier

PSRR Power supply rejection ratio

RHP: Right Hand Plane

LPH and RPH present where poles or zeros at when graphing complex number.

ω is the angular frequency which unit is rad/sec. 1Hz = 2π rad/sec.

Chapter 1

Introduction and Overview

1.1 Introduction

Over the last few years, CMOS technology including CMOS operational amplifier (Op-Amp) has been developed rapidly. CMOS Op-Amp is one of the most fundamental, versatile and integral circuit blocks of many analog and mixed-signal systems [28] [35] [23] [6]. They are widely used in many applications such as comparators, differentiators, dc bias applications and so on [26] [19]. For most of the cases, a single stage amplifier is not adequate due to its limited gain and output voltage range. So CMOS Operational Amplifier architectures that use two or more gain stages are developed and widely used [20]. However, more stages introduce more phase shifts that require frequency compensation networks to maintain the system stability. To increase the amplifier stability, multiple compensation approaches have been developed by IC designers in the recent decade.

In this paper, some of popular compensation methods will be summarized, evaluated and compared in the design of two-stage Op-Amp including direct and indirect compensations. Starting from the Miller Compensation, which is one the most popular approaches to stabilize the Op-Amp, an undesired right-hand-plane (RPH) zero will come out in the open-loop gain due to the direct connection of the feedback compensation capacitor from the output to input. To resolve this RPH zero, there are several methods can be applied including: Nulling Resistor, Voltage Buffer, and Current Buffer. Nulling Resistor is added in series with the

compensation capacitor to move the zero from RPH to left-hand-plane (LPH), which is the most popular and straightforward method among all others [30]. Voltage Buffer and Current Buffer techniques are used to remove this RPH zero by blocking the feed-forward current flow in the compensation circuit. Moreover, all the design processes will also be discussed further regarding the performance improvement of compensated two-stage Op-Amp. The Cadence designs and simulation results have been obtained by TSMC 180nm CMOS technology. All the compensation designs will also be discussed and compared based on a given standard Op-Amp performance.

1.2 Overview

Chapter 2 presents the significance of stability of Op-Amp and then states all the compensation techniques in the order of traditional Miller Compensation, Nulling Resistor, Voltage Buffer, and Current Buffer.

Chapter 3 depicts the Cadence design procedures and demonstrates the simulation results where evaluations, improvements, and comparisons among all techniques are stated.

Chapter 4 draws a conclusion from all the works presented in the previous chapters.

Chapter 2

Background and Conceptual Principle

2.1 Background of Amplifier System Stability

Two or more stages amplifiers can be implemented to achieve high gain and high output swing regardless of the limitations of the power supply voltage or power consumption compared to single stage amplifiers. However, multiple stage amplifiers are generally complicated to compensate. An uncompensated two-stage operational amplifier has a two-pole transfer function, and both poles are located below the unity gain frequency.

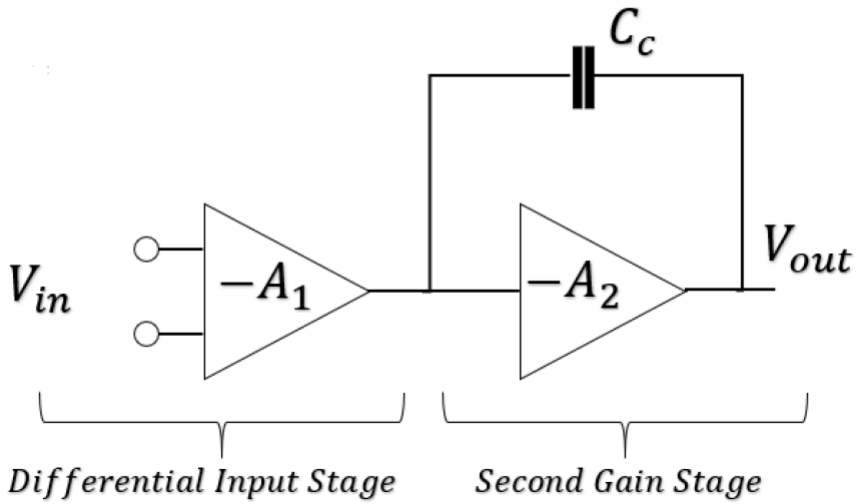


Figure 2.1: Block diagram of a Miller compensated operational amplifier [8]

Therefore, a compensation circuitry must be implemented to enlarge the phase margin so

does the stability, which will be talked further in this chapter. This compensation circuitry can also be called as a compensator or a feedback network in operational amplifiers design. As shown in the Figure 2.1, the Miller capacitor is used as a negative feedback network to compensate the system, which feeds a current back from the output to the middle of the two stages A1 and A2.

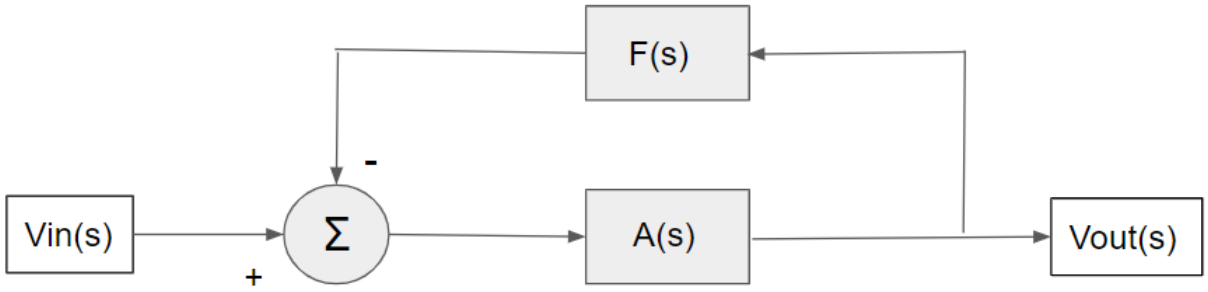


Figure 2.2: Block Diagram of a Single Loop Feedback System

However, Operational amplifiers operating on a close-loop with a negative-feedback system are susceptible to oscillation. The more oscillation it generates to the output, the more unstable the system is. Figure 2.2 depicts a general block diagram of an amplifier system with a single feedback network, which closely represents the compensated two-stage operational amplifier shown in Figure 2.1. In Figure 2.2, A(s) indicates the differential voltage gain of the operational amplifier, and F(s) indicates the feedback transfer function from the output back to the input. Some important loop gain definitions are shown in the following Equation 2.1 and 2.2:

$$OpenLoopGain = L(s) = -A(s)F(s) \tag{2.1}$$

$$CloseLoopGain = \frac{Vout(s)}{Vin(s)} = \frac{A(s)}{1 + A(s)F(s)} \tag{2.2}$$

$$|A(j\omega_1)F(\omega_1)| = 1 \tag{2.3}$$

$$\angle|A(\omega_1)F(\omega_1)| = -180^\circ \tag{2.4}$$

According to the Barkhausen's Criterion, the oscillation condition of such system needs to meet two requirements which are represented in Equation 2.3 and 2.4, where F(s) here is considered as a constant [29]. The total phase shift of the system is 360° at ω_1 because the negative feedback network introduces a 180° phase shift. In this case, the circuit can amplify its own noise until it eventually begins to oscillate at frequency ω_1 [29].

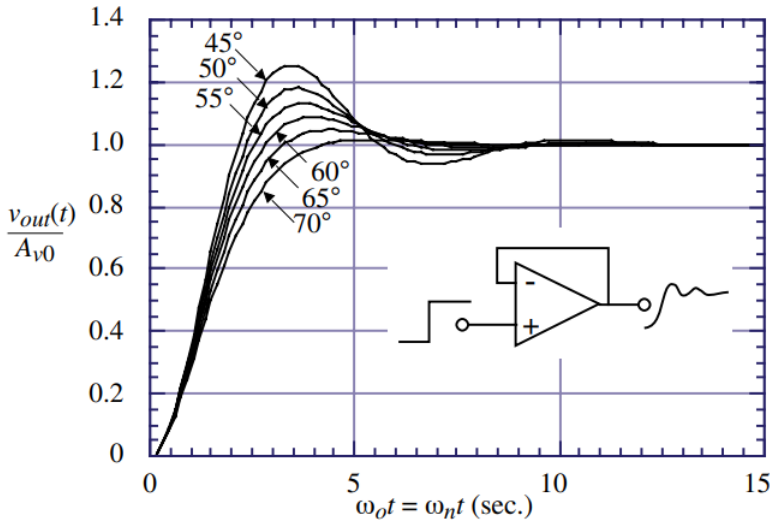


Figure 2.3: Phase Margin Demonstration [8]

$$PhaseMargin = \phi_M = Arg[-A(j\omega_{0dB})F(j\omega_{0dB})] = Arg[L(j\omega_{0dB})] \tag{2.5}$$

One major criterion to measure the stability of this system is the phase margin, which is the phase angle difference from the 0dB frequency to ±180° as shown in Equation 2.5 [7]. Phase margin indicates system relative stability, and the tendency of oscillation during its response to an input change such as a step function. Consider a step response of the second-order system which models the closed-loop gain of the two-stage operational amplifier. Shown on Figure 2.3, smaller phase margin tends to have larger overshoot and longer settling time to a

step response input while larger phase margin can settle the output down quicker and has less output oscillation. For most of the two-stage Op-Amp, designers want to settle the output down quickly instead of letting it oscillate, so a large phase margin of a system is preferred, which should be at least 45° and preferable 60° or larger. Also, too much overshoot has a risk of damaging the output device.

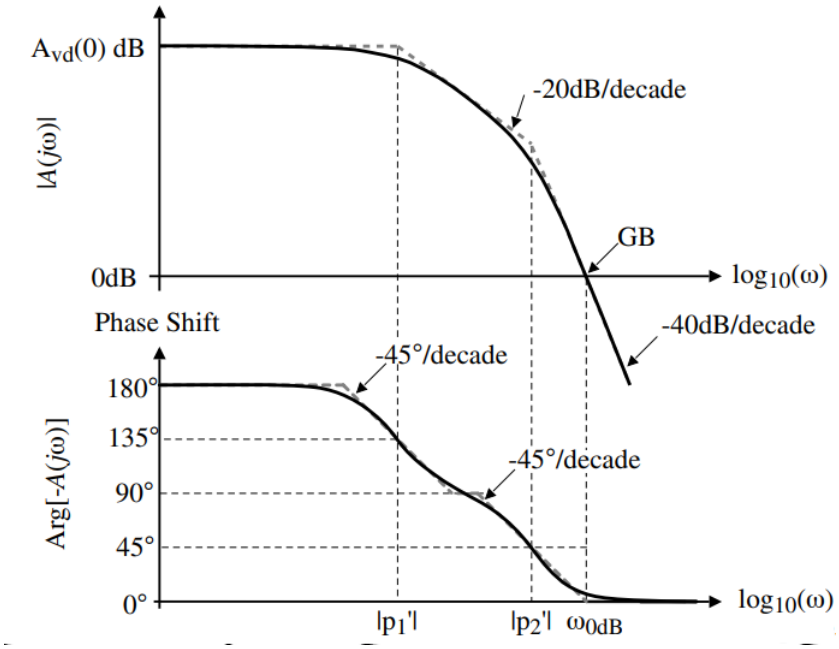


Figure 2.4: Uncompensated Frequency Response of Two Stage Operational Amplifier [8]

Shown in Figure 2.4, the phase margin at ω_{0dB} is close to 0° due to the two poles, which is generated by the two stage amplifier, are below the unity gain frequency. Even though p_2 is close to the unity gain frequency, it nearly drops another 90° to the phase margin. Due to this major issue, the amplifier must have a compensation network to enlarge its phase margin to at least 45° to ensure the stability of the whole system. One of the most common approaches to address this issue is called Miller Compensation.

2.2 Compensated Op-Amp Survey

Before talking about the Miller compensation and all other techniques, a summarized survey is listed below which includes and compares all the related topologies of compensations. This survey compares some typical compensation designs including Miller Compensation, Miller compensation with Nulling resistor, and Current buffer.

Referred paper work	Miller compensation[25]	Miller compensation with Nulling resistor[35]	Current buffer[28]
Supply Voltage(V)	2.9 - 3.7	5	3.3
DC Gain(dB)	98.98	77.25	78.21
Gain Bandwidth(MHz)	2.22	14.1	5.82
Phase Margin(°)	81.5	85.85	63.97
Slew Rate(V/μs)	1.37	9.4	5.58
Power Consumption (μW)	-	-	144.34
CMRR(dB)	104.22	81	89.05
PSRR(dB)	92.46	-	117.73

Table 2.1: Survey of various op amps topologies

Common mode rejection ratio (CMRR) is measured by: differential gain – common mode gain, where differential gain is the DC gain [29], [25]. By applying this equation to all three works, we can know the typical common mode gain range is around 4dB to 10dB. Power supply rejection ratio (PSRR) measures the power supply noise rejection ability of the amplifier, which are pretty high for all three designs (over 80dB). Due to the similarity and stability of CMRR and PSRR of two-stage operational amplifier, this two parameters will not be considered in the design and simulation in Chapter 3.

2.3 Miller Compensation Technique Principle

Miller compensation is one of the most popular techniques that is used to increase the stability of the Multi-stage amplifier. The design that is shown in Figure 2.5 is the configuration of Miller compensation. The first stage of this Op-Amp consists of NMOS differential inputs with a PMOS current mirror load, whereas the second stage is a PMOS common source amplifier with a NMOS current mirror load. The compensation capacitor is connected between the output of these two stages, so this Compensation Capacitor C_C is also called a Miller Capacitor [12] [33] [32]. This typology can also be referred as a single capacitor Miller compensation (SCMC) in some paper works [9]. Due to the direct connection of output and input of the second stage, SCMC can also be called as Direct Feedback Compensation [34].

The working principle of Miller compensation is to split the poles so a higher phase margin can be reached at the unity gain frequency [34]. However, a right-hand-plane (RHP) zero was generated due to a feed forward current from the output of the first stage to the output of the second stage [10]. Before compensating the circuit, the two stage operational amplifier has two poles which are located at $p_1 = \frac{1}{R_1 C_1}$, and $p_2 = \frac{1}{R_2 C_2}$, where R and C are the resistance and capacitance respectively at the corresponding nodes shown in the Figure 2.6. The capacitors C_1 and C_2 are mainly formed by the parasitic capacitance of corresponding connected MOSFETs of each node. After the implementation of the Miller Capacitor, the dominant pole and non-dominant pole are achieved due to the pole splitting. By using nodal analysis at both input (V_1) and output (V_2) nodes of the common source stage, the system gain equation can be generated as shown in equation 2.6, where the new positions of poles

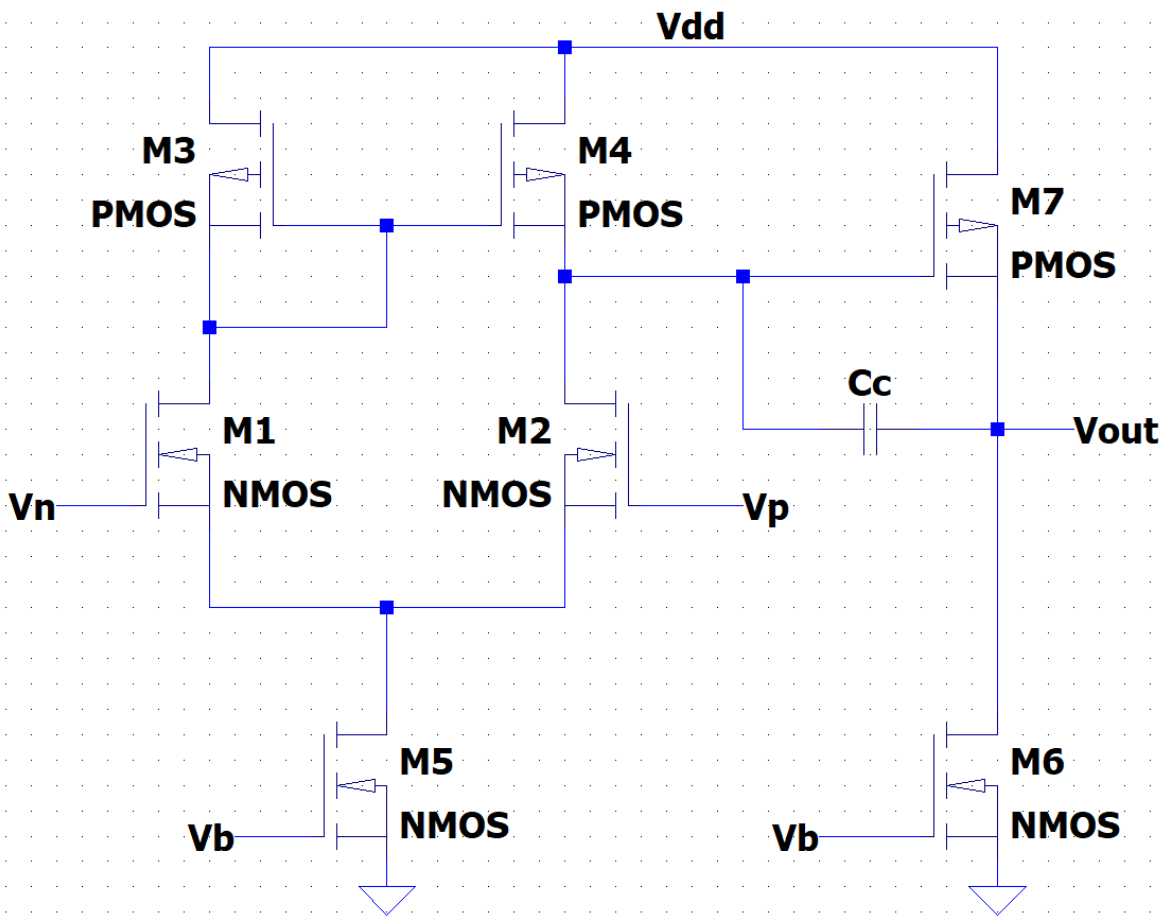


Figure 2.5: Two-Stage Op-Amp with Miller Compensation

and zero can also be found.

$$
\begin{aligned}
A_V(s) &= \frac{Vout(s)}{Vin(s)} = \frac{g_{m1}g_{m7}R_1R_2(1-\frac{sC_c}{g_{m7}})}{1+sa+s^2b} \\
a &= (C_2+C_C)R_2 + (C_1+C_C)R_1 + g_{m7}R_1R_2C_C, \\
b &= R_1R_2(C_1C_2+C_1C_C+C_2C_C)
\end{aligned}
\tag{2.6}
$$

In equation 2.6, the DC gain and the position of zero can be noticed directly. The amplifier DC gain is:

$$DC \quad gain = g_{m1}g_{m7}R_1R_2 \tag{2.7}$$

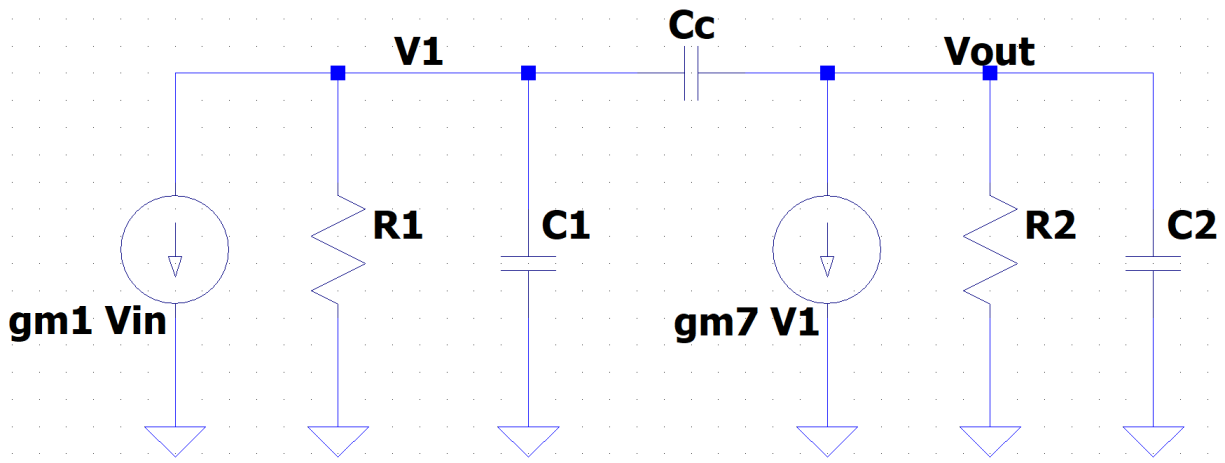


Figure 2.6: Small Signal Model of Miller Compensation Technique

The value of the RPH zero is:

$$z_1 = \frac{g_{m7}}{C_C} \tag{2.8}$$

To find the new positions of both poles, the denominator needs to be simplified. Assume the denominator of $A_V(s)$ is $D(s)$. In general, for quadratic equation like $D(s)$, it can be rewrote to the following form:

$$\begin{aligned} D(s) &= (1 - \frac{s}{p_1})(1 - \frac{s}{p_2}) \\ &= 1 - s(\frac{1}{p_1} + \frac{1}{p_2}) + \frac{s^2}{p_1 p_2} \\ &\cong 1 - \frac{s}{p_1} + \frac{s^2}{p_1 p_2} \quad for \quad |p_1| << |p_2| \end{aligned} \tag{2.9}$$

In order to get the precise and the simplified value of p_1 and p_2, the equation 2.9 needs to be matched with the denominator of the equation 2.6. So the value of the dominant pole p_1

is:

$$\begin{aligned} p_1 &= \frac{-1}{(C_2+C_C)R_2+(C_1+C_C)R_1+g_{m7}R_1R_2C_C} \\ &\cong \frac{-1}{g_{m7}R_1R_2C_C} \end{aligned} \tag{2.10}$$

The value of the non-dominant p_2 is:

$$\begin{aligned} p_2 &= -\frac{(C_2+C_C)R_2+(C_1+C_C)R_1+g_{m7}R_1R_2C_C}{R_1R_2(C_1C_2+C_1C_C+C_2C_C)} \\ &\cong -\frac{g_{m7}C_C}{C_1C_2+C_1C_C+C_2C_C} \\ &\cong -\frac{g_{m7}}{C_2+C_1} \quad or, \quad -\frac{g_{m7}}{C_2} \quad for \quad C_2>C_C>C_1 \end{aligned} \tag{2.11}$$

As shown in Figure 2.7, the original open-loop poles p_1', and p_2' are split to the new position

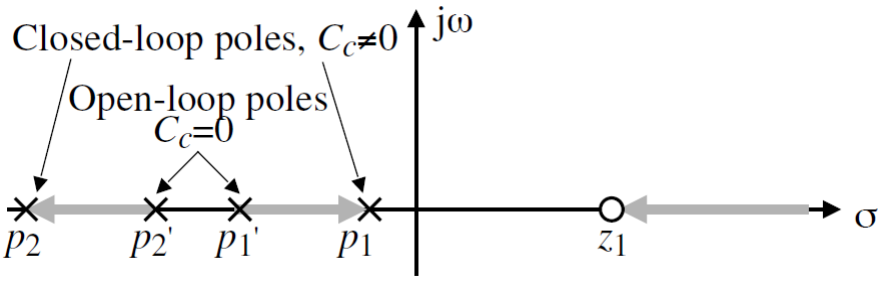


Figure 2.7: Pole Splitting Demonstration [2]

p_1 and p_2 due to the Miller Compensation, where their values are shown in Equation 2.10 and 2.11. p_1 becomes more dominant than it used to be, which results in the system starting to behave as a first order system in low frequency range. On the contrary, p_2 moves to the other direction which makes it more non-dominant. The goal of splitting both poles is achieved, however, a RHP zero z_1 is generated, which is undesirable because it boosts the

gain while decreasing the phase [22] [34]. One approach to address this issue is to make sure its frequency is 10 times larger than the unity gain bandwidth frequency by adjusting the corresponding parameter of z_1 which is shown in Equation 2.8. This is the main reason that the size of the compensation capacitor cannot be too large. To ensure at least 45° phase margin, the effective frequency of the second pole p_2 must be the same or larger than the unity gain bandwidth as illustrated in the Figure 2.8. To obtain a higher phase margin, p_2 needs to be moved to the left further in Figure 2.7 which is the high-frequency direction in Figure 2.8, so that p_2 has less effect of reducing the phase margin.

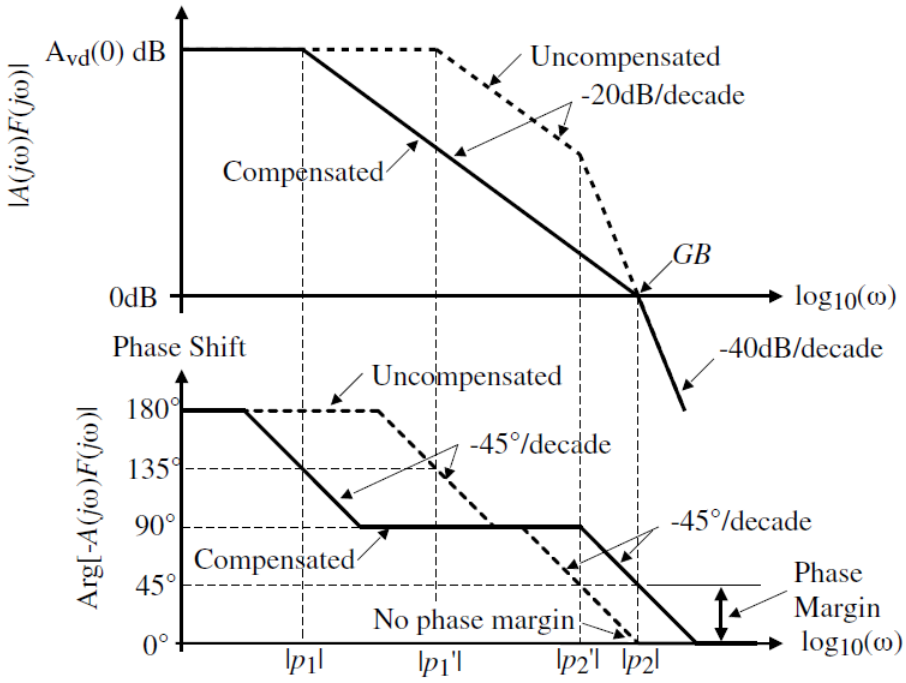


Figure 2.8: Compensated Frequency Response of Two Stage Operational Amplifier [2]

So the key point for now is to find the unity gain bandwidth shown as 'GB' in Figure 2.8, which is the value of 0dB frequency. In this graph, the location of 'GB' is only affected by the value of the dominant pole p_1, where the gain starts to drop as a slope of -20dB/decade.

So the relationship of these variables can be derived as the equation below:

$$\begin{aligned} 20log_{10}(A_V(0)) &= [log_{10}(GB) - log_{10}(|p_1|)] \times 20 \\ log_{10}(A_V(0)) &= log_{10}(\frac{GB}{|p_1|}) \\ GB &= A_V(0) \times |p_1| \\ GB &= \frac{g_{m1}g_{m7}R_1R_2}{g_{m7}R_1R_2C_C} \\ GB &= \frac{g_{m1}}{C_C} \end{aligned} \tag{2.12}$$

Suppose the required phase margin for stability is 60°, then the location of p_2 can be estimated from this phase requirement by using the following equation:

$$180° - tan^{-1}\frac{\omega}{|p_1|} - tan^{-1}\frac{\omega}{|p_2|} - tan^{-1}\frac{\omega}{|z_1|} = PM = 60° \tag{2.13}$$

Let ω be equal to the unity gain bandwidth frequency GB in the previous equation and assume z_1 is 10 times larger than GB, then the following equation can be obtained [2]. The main reason to let z_1 10 times larger than GB is to shrink its effect of phase margin.

$$\begin{aligned} &180° - tan^{-1}\frac{GB}{|p_1|} - tan^{-1}\frac{GB}{|p_2|} - tan^{-1}\frac{GB}{|z_1|} = PM = 60° \\ &180° - tan^{-1}A_V(0) - tan^{-1}\frac{GB}{|p_2|} - tan^{-1}(0.1) = 60° \\ &180° - 90° - 60° - 5.7 = tan^{-1}\frac{GB}{|p_2|} \\ &tan^{-1}\frac{GB}{|p_2|} = 24.3° \quad \rightarrow \quad \frac{GB}{|p_2|} = 0.452 \\ &|p_2| > 2.215 \times GB \end{aligned} \tag{2.14}$$

Then the relationship of the trans-conductance g_m of Mosfets can be obtained by applying the Equation 2.8, 2.11, and 2.12 to the assumption above. The relationship between g_{m7}

and g_{m1} is restricted by the assumption that z_1 is 10 times larger than GB, which is shown in the following equation.

$$\begin{aligned} z_1 &\geq 10 \times GB \\ \frac{g_{m7}}{C_C} &\geq 10 \times \frac{g_{m1}}{C_C} \\ g_{m7} &\geq 10 g_{m1} \end{aligned} \tag{2.15}$$

The value of the compensation capacitor C_C can be estimated through the relationship between p_2 and GB that is shown in Equation 2.16. Knowing that C_2 is the capacitance corresponding to the output node which parasitic capacitances are relatively small compared with the load capacitor C_L, so we can assume C_2 is equal to the load capacitor for easy calculations.

$$\begin{aligned} |p_2| &\geq 2.215 \times GB \\ \frac{g_{m7}}{C_2} &\geq 2.215 \times \frac{g_{m1}}{C_C} \\ \frac{10 g_{m1}}{C_2} &\geq 2.215 \times \frac{g_{m1}}{C_C} \\ C_C &\geq 0.2215 C_L \end{aligned} \tag{2.16}$$

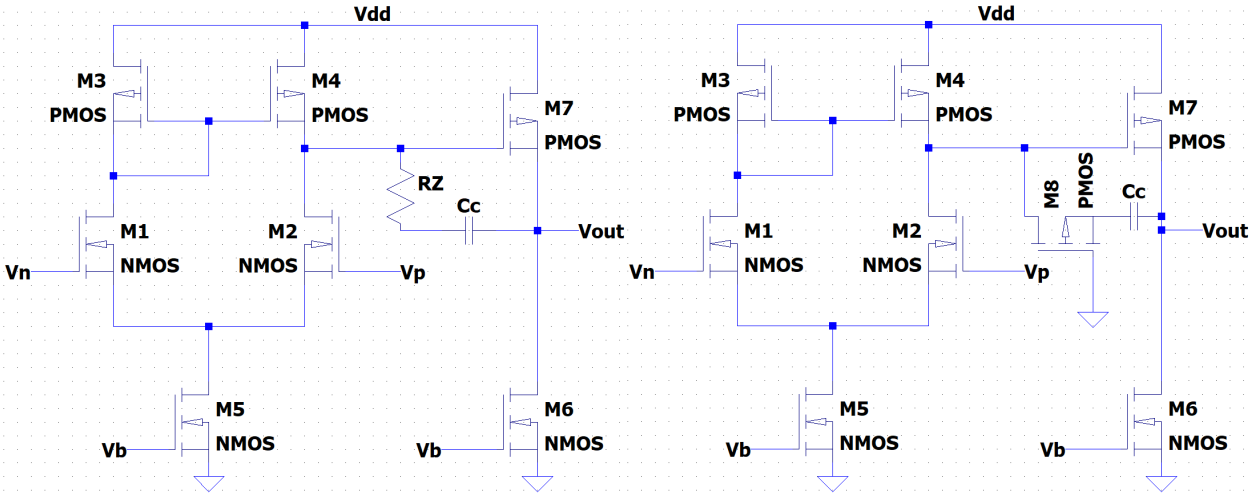
Overall, to obtain a phase margin at least 60° for stability, C_C needs to be the same or larger than the 0.2215 times C_2. Also, g_{m7} needs to be at least 10 times of g_{m1}. The positions of both poles and zero should be at the correct locations with respect to unity gain frequency. However, there are still several trade-offs in real world design of Two Stage Amplifiers. For example, increasing g_{m7} can separate the poles more but costs more power. Making the C_C too large may not help with the phase margin as ω_{z1} will reduce too. Large C_C could also

reduce the unity gain bandwidth. So to obtain a better stability of two-stage Op-Amps, the RHP zero must be addressed. There are several ways to get rid of this RHP zero, and one of the most common approaches is adding Nulling Resistor which could move this zero from the right plane to the left [22].

2.4 Nulling Resistor Technique Principle

2.4.1 Nulling Resistor Technique Background

As talked in the last section, adding a nulling resistor in series with the compensation capacitor is one of the most common approaches to eliminate the negative effect of the RHP zero by moving this zero to the LHP [21] [17] [14] [11]. Figure 2.10 depicts the pole splitting phenomenon and shows all the locations of poles and zero. This nulling resistor RZ can either be an actual resistor or a transistor as shown in Figure 2.9. The transistor used in



(a) Nulling Resistor with Actual Resistor (b) Nulling Resistor with Transistor

Figure 2.9: Compensated Two-Stage Op-Amp with Nulling Resistor

Figure 2.9b is PMOS, which can also be replaced by a NMOS transistor by connecting its

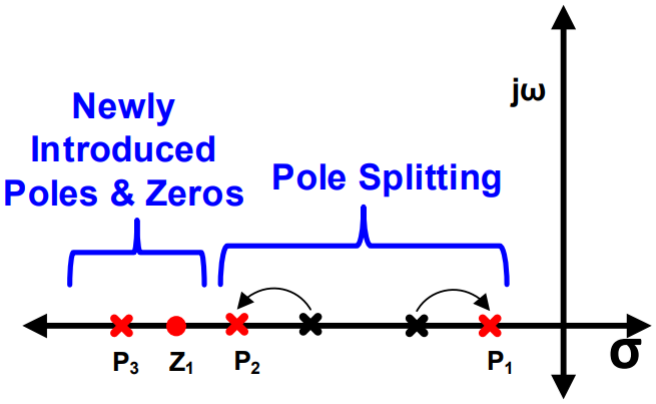


Figure 2.10: Locations of Ploes and the Zero [22]

gate terminal to Vdd. Instead of using a single transistor here, a CMOS switch can be used to avoid dynamic range limitation in some specific applications [18]. This CMOS technology switch is also known as a Transmission Gate that connects a NMOS and a PMOS transistor in parallel as illustrated in Figure 2.11.

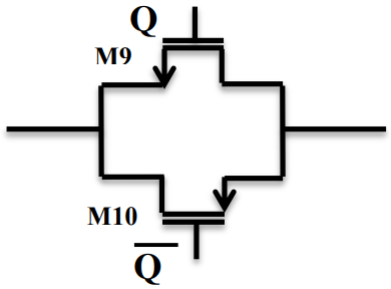


Figure 2.11: Transmission Gate [18]

For this configuration, when Q is low, both transistors are off, and the transmission gate is off. When Q is high, both transistors are on, creating a low resistance close loop circuit. So in this case, the signal Q is connected to a high voltage node which is usually the Vdd while the signal $\overline{Q}$ is connected to a low voltage node which is always the ground. The resistance values of the both PMOS and NMOS are obtained from Equation 2.17 and 2.18, which are derived in [29].

$$R_{ON} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{THn})} \tag{2.17}$$

$$R_{OP} = \frac{1}{\mu_p C_{ox} \frac{W}{L}(V_{SG} - V_{THp})} \tag{2.18}$$

For the PMOS and the NMOS transistors in this transmission gate, their overdrive voltages are much bigger than the absolute value of their drain to source voltages ($|V_{ds}|$). So both transistors work in deep triode regions which operate like voltage controlled resistors [29]. In this situation, the overdrive voltage is nearly stable so the resistance value can only be changed by adjusting the parameter $\frac{W}{L}$ based on the Equation 2.17 and 2.18. Both equations also work for a single MOSFET that is used as a nulling resistor in the compensation network.

2.4.2 Nulling Resistor Technique Frequency Response

Similar to the Miller Compensation Technique, to know the effect of the adding resistor, we need to find all the poles and zeros through the small signal analysis. By applying nodal

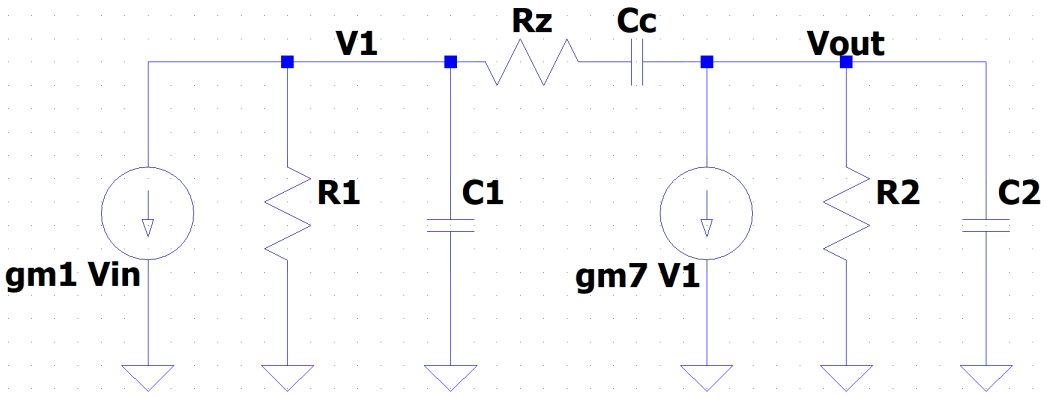


Figure 2.12: Small Signal Model of Nulling Resistor Technique

analysis to both V_1 and V_{out} nodes in Figure 2.12, the relationship of output and input signals can be derived, where we can find all the poles and zeros. The derivation is nearly the same

as the Miller Compensation Technique that is fully described in Section 2.3. The locations of both original poles are the same as Miller Compensation Technique that are listed in Equation 2.10 and 2.11 which are $p_1 = \frac{-1}{g_{m7}C_C R_1 R_2}$ and $p_2 = \frac{-g_{m7}}{C_2}$. The new position of zero is given in the following equation [34].

$$z_1 = \frac{1}{(\frac{1}{g_{m7}} - R_Z)C_C} \tag{2.19}$$

R_Z is the resistance value of the nulling resistor. For $R_Z > \frac{1}{g_{m7}}$, this zero will appear in LHP, which helps improve the phase margin thus the stability. This zero will vanish if R_Z is equal to $\frac{1}{g_{m7}}$ [18]. In fact, this resistor value can be further increased to place the z_1 on top of the p_2 which can eliminate its negative effect on phase margin.

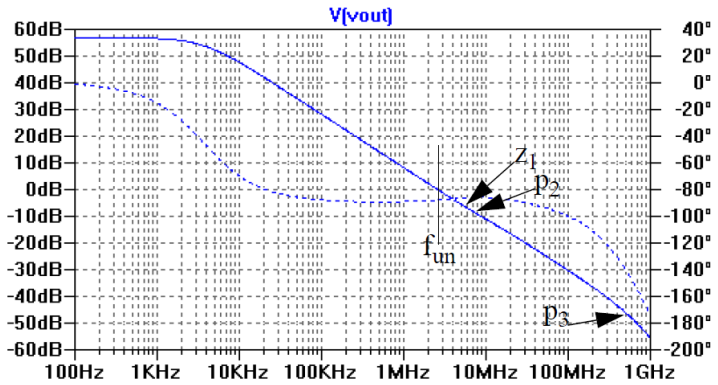


Figure 2.13: Frequency Response of the Miller Compensated Operational Amplifier with Nulling Resistor [34]

Another high-frequency pole p_3 is introduced at $p_3 \cong \frac{-1}{R_Z C_1}$ which is far away from both p_1 and p_2 [34] [18] [22]. Considering R_Z and C_1 are relatively small compared with the value of other resistors and capacitors, the effects of this newly introduced pole will not be considered in the Cadence design in Chapter 3. Figure 2.13 shows a sample frequency response of a Miller compensated Op-Amp with nulling resistor, where the locations of unity gain frequency, p_2, p_3, and z_1 are marked. This plot can also prove the above statement

regarding p_3, as the value of p_3 is over 100 times away from the unity gain frequency.

2.5 Voltage Buffer Technique Principle

Instead of changing the location of the RHP zero, a voltage buffer can be used to eliminate this zero by rejecting the feed-forward path through the Miller Capacitor in the feedback path [24] [16]. At the same time, the feedback network should work functionally. So a common gate amplifier can be used here as the voltage buffer which blocks the feed-forward current and allows the feedback current that flows from the output to the input of the second stage. Figure 2.14 is a block diagram of this methodology and Figure 2.15 is a sample schematic that is implemented by NMOS and PMOS transistors respectively.

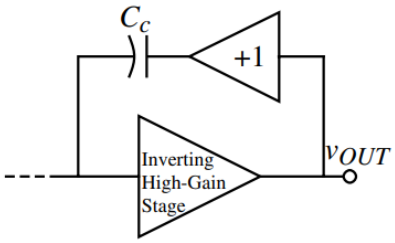


Figure 2.14: Block Diagram of Voltage Buffer Implementation [2]

One drawback of this method is one more path costs additional power and transistors. Also, there is a fixed voltage drop in the feedback network due to the use of the voltage follower [34]. This voltage could reduce the output voltage swing [34]. The maximum and the minimum $Vout$ of both cases is Vdd and ground, which means the source follower might work as a diode connected MOSFET but never in the triode region. So the feedback signal will never get broken down by large $Vout$ which is a opposite in [34]. One advantage is that this topology makes frequency response simple since the zero is removed and both poles

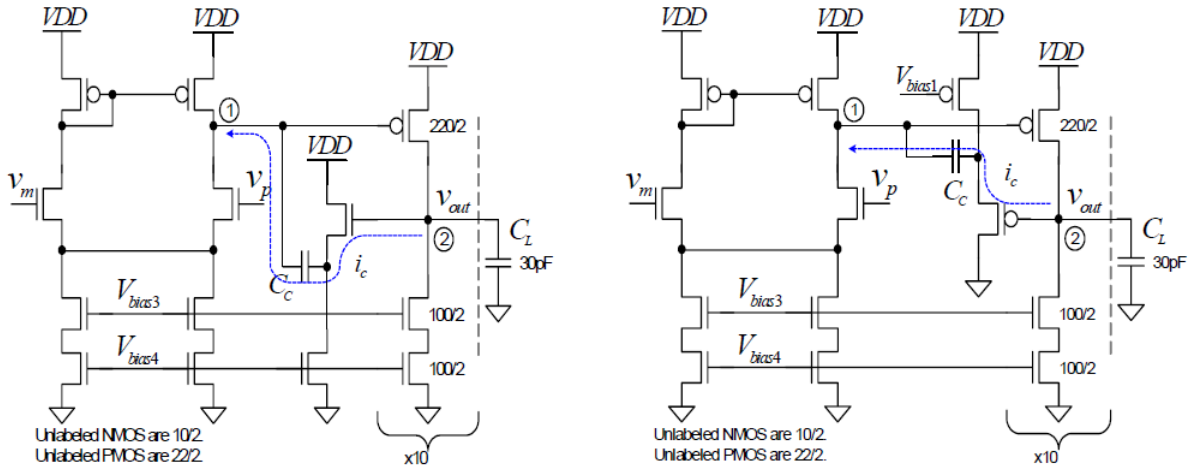


Figure 2.15: Compensated Two-Stage Op-Amp with Voltage Buffer [34]

remain at the same locations which are $p_1 = \frac{-1}{g_{m7}C_C R_1 R_2}$ and $p_2 = \frac{-g_{m7}}{C_2}$. Also, all the negative effects of this RHP zero disappear.

2.6 Indirect Compensation Technique Principle

2.6.1 Indirect Compensation Background

Miller compensation is achieved by connecting the feedback network directly from the output to the input of the second stage. This feedback network can also be fed back indirectly from the output to an internal high impedance node, which is called Indirect Feedback Compensation [34] [5]. The feedback path is connected to an internal low impedance node in the first stage, which allows indirect feedback of the compensation current from the output node to the internal high-impedance node which is the output of the first stage [31] [13]. Shown in Figure 2.16 is the block diagram of an indirect compensation 2-stage Op-Amp, where the low impedance node is marked as Z_{low}. Indirect compensation can be achieved by several approaches as long as a low impedance node can be found in the first stage, such as

adding a common gate stage, cascoded current mirror load, and cascoded differential inputs pair[31] [34].

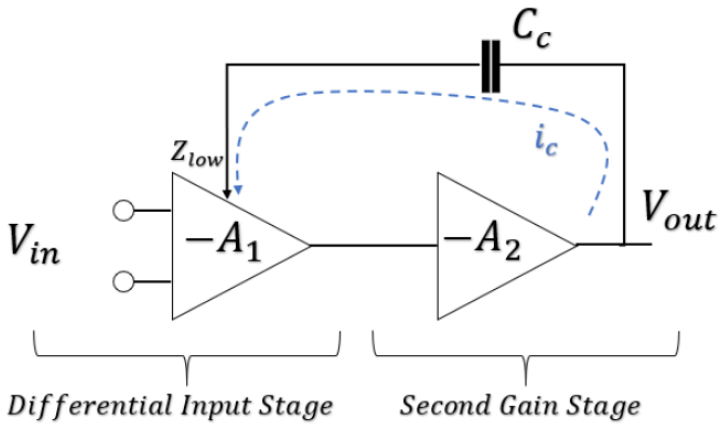


Figure 2.16: Block Diagram of Indirect Compensation [8]

2.6.2 Common Gate Stage (Current Buffer) Compensation

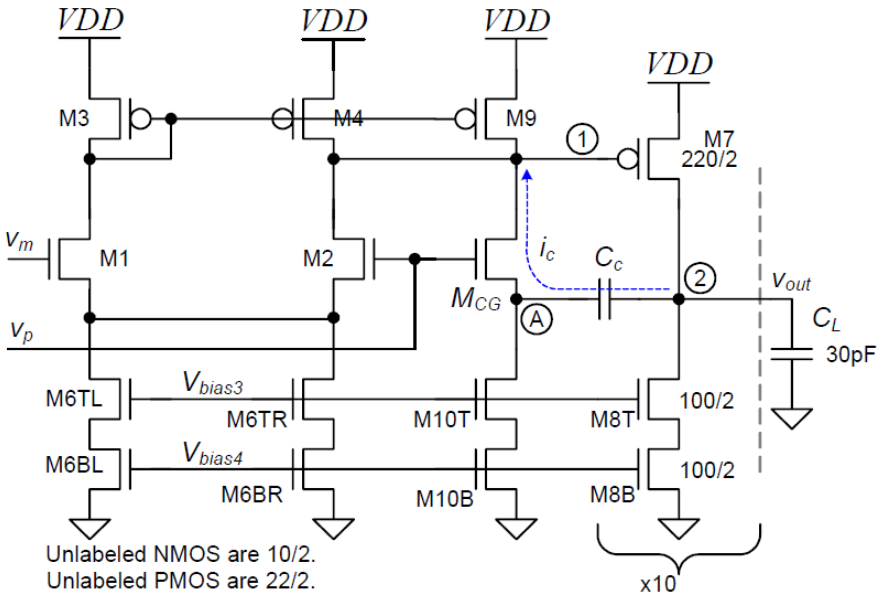


Figure 2.17: 2 Stage Op-Amp with Common Gate Stage Compensation [34]

As shown in Figure 2.17, the current sources $M9$, $M10$ and the common gate amplifier M_{CG} configures the indirect compensation stage. This idea is first introduced by Ahuja in his paper which was published in 1983 [1]. So this common gate compensation is also called Ahuja compensation. Since this stage does not share components with the original 2 stages of the Op-Amp, this stage can be referred to as a "separate, additional" stage [10]. This common gate stage can also block the feed-forward current path and allow the feedback current as the common drain stage [10] [34] [27]. So based on this statement, if the common gate stage is modeled as an ideal current buffer, the RHP zero could be eliminated [10]. However, in the following analysis, the current buffer is not assumed to be ideal. In order to obtain and analyze the relationship of the output and the input, the small signal model of this common gate stage Op-Amp is derived and shown in Figure 2.18, where R_A and C_A are the resistance and capacitance at the low impedance node A. Vs is denoted as the differential pair inputs which is equal to V_p - V_m.

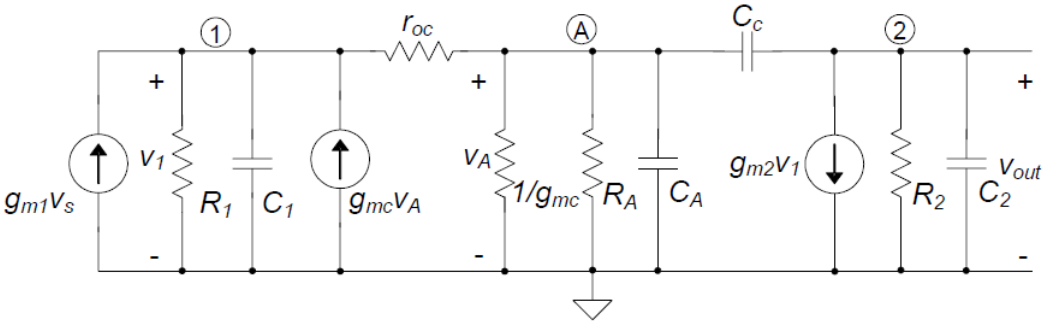


Figure 2.18: Small Signal Model of Common Gate Stage Compensation Op-Amp [34] [13] [10]

In all [34] [13], and [10], they all used the same small signal model in Figure 2.18, and all these papers were published before 2010. However, the equivalent small signal model is presented differently in a recent published paper [30]. The same design idea is also depicted in [15]. Shown in Figure 2.19a, the basic working idea is the same where the current source

MOSFETs are represented by the ideal current sources $I1$, and $I2$. But the small signal model is partially different regarding the common gate stage, which is in between of the 2-stage Op-Amp. More specifically, the overdrive voltage controlled current source ($g_{m9}V_{gs9}$) is placed between the source node (V_s9) and the drain node ($V1$) as shown in Figure 2.19b. However, in Figure 2.18 this dependent current source is connected from the $Vs9$ to ground. The second design is preferred in my opinion even though it does not consider the resistance of ideal current sources. However, all the estimated poles and zero locations are the same no matter what small signal models are used.

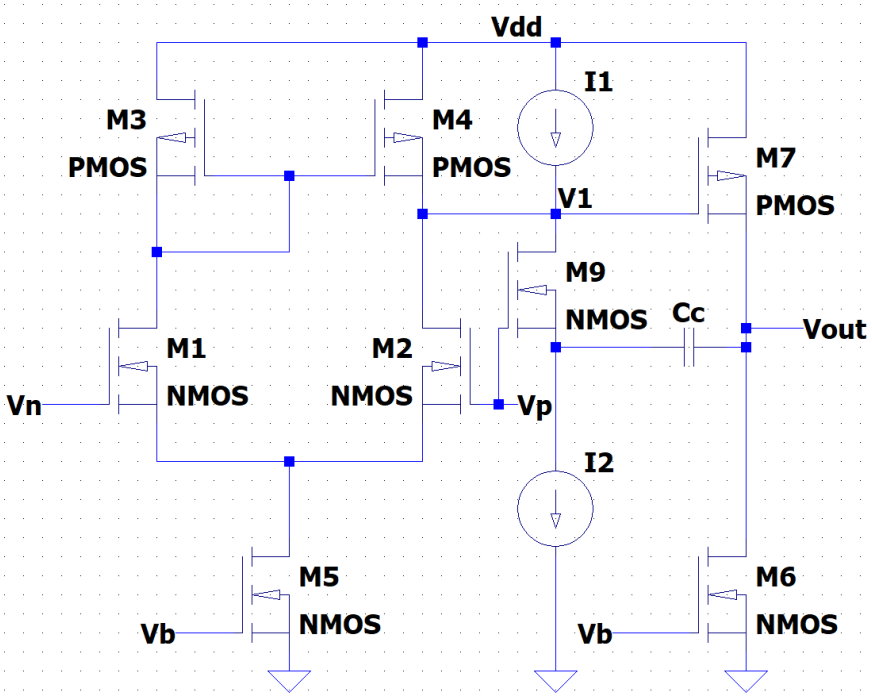
According to the small signal model in Figure 2.18, there are three voltage nodes and hence three dependent variables, $V1$, V_A, and $V2$ or $Vout$. So by applying the nodal analysis on each node, three equations of all these variables can be derived.

$$-g_{m1}V_s + \frac{V_1}{R_1} + V_1 sC_1 - g_{mc}V_A + \frac{V_1 - V_A}{r_O C} = 0 \tag{2.20}$$

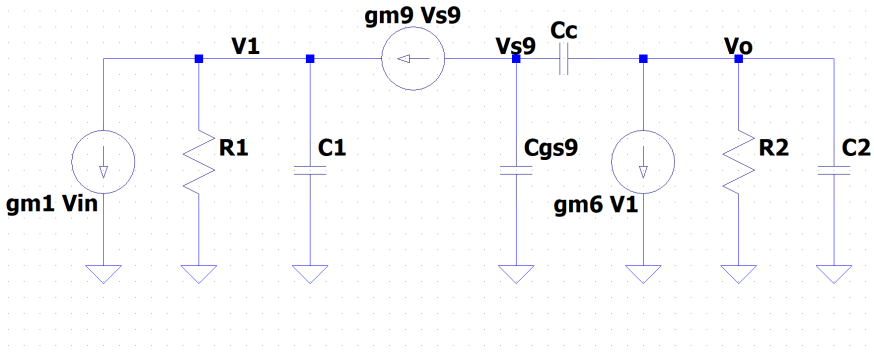
$$g_{m2}V_1 + \frac{V_{out}}{R_2} + V_{out}sC_2 + sC_C(V_{out} - V_A) = 0 \tag{2.21}$$

$$\frac{V_A - V_1}{r_{OC}} + g_{mc}V_A + \frac{V_A}{R_A} + V_A sC_A + sC_C(V_A - V_{out}) = 0 \tag{2.22}$$

The transfer function of the amplifier system can be obtained from these equations and its simplified from is shown in the following equation, where assumptions $C_2 \cong C_L$; and C_C, C_2



(a) 2 Stage Op-Amp with Common Gate Stage Compensation II



(b) Small Signal Model of Common Gate Stage Compensation Op-Amp II

Figure 2.19: 2 Stage Op-Amp with Common Gate Stage Compensation Design II [30] [15]

» C_1, C_A are applied [34].

$$\frac{V_{out}}{V_s} = A_V(\frac{b_0 + b_1 s}{a_0 + a_1 s + a_2 s^2 + a_3 s^3})$$

$$A_V = g_{m1} g_{m2} R_1 R_2$$

$$b_0 = g_{mc} R_A r_{OC}$$

$$b_1 = R_A r_{OC}(C_C + C_A)$$

$$a_0 = (g_{mc} R_A + 1) r_{OC}$$

$$a_1 = (g_{mc} R_A + 1) g_{m2} R_1 R_2 r_{OC} C_C$$

$$a_2 = (g_{mc} R_A + 1) R_1 R_2 r_{OC} C_1 (C_2 + C_C) + R_2 R_A C_2 [r_{OC}(C_C + C_A) + R_1(C_C + C_A + C_1)]$$

$$a_3 = R_1 R_2 R_A C_1 r_{OC}(C_2 C_A + C_2 C_C + C_C C_A) \tag{2.23}$$

The location of the zero can be obtained from the numerator of this transfer function which is at:

$$z_1 = -\frac{b_0}{b_1} = -\frac{g_{mc}}{C_C + C_A} \tag{2.24}$$

Obviously, this zero is located on the LHP and the key point here is this zero is on the LHP instead of RHP for a finite value of g_{mc} [10].

The amplifier has three poles from the denominator of the transfer function where the location of the dominant pole p_1 is derived in Equation 2.25 if the assumption $|p_1| \gg |p_2|, |p_3|$ is applied [10] [34] [13].

$$p_1 = -\frac{a_0}{a_1} = -\frac{1}{g_{m2} R_2 R_1 C_C} \tag{2.25}$$

By comparing this location with the p_1 from Miller Compensation in Equation 2.10, the dominant pole does not move. Based on the assumption that the other poles are far away from p_1, so for $s \gg p_1$, the denominator of the transfer function could be rewritten as:

$$D(s) \cong (1 - \frac{s}{p_1})(1 + \frac{a_2}{a_1}s + \frac{a_3}{a_1}s^2) \tag{2.26}$$

The second part of the denominator can be rewritten as a form showing the locations of p_2 and p_3, which is denoted as $D'(s)$.

$$\begin{aligned} D'(s) &= (1 - \frac{s}{p_2})(1 - \frac{s}{p_3}) \\ &= 1 - s(\frac{1}{p_2} + \frac{1}{p_3}) + \frac{s^2}{p_3 p_2} \\ &\cong 1 - \frac{s}{p_2} + \frac{s^2}{p_3 p_2} \quad for \quad |p_2| << |p_3| \end{aligned} \tag{2.27}$$

From the above equation, locations of the non-dominant poles p_2, and p_3 can be obtained.

$$p_2 = -\frac{a_1}{a_2} = -\frac{g_{m2}C_C}{C_1(C_C + C_2)} \cong \frac{g_{m2}C_C}{C_1 C_L} \tag{2.28}$$

$$p_3 = -\frac{a_2}{a_3} \cong -(\frac{g_{mc}}{C_2||C_C} + \frac{1}{C_1(R_1||R_{OC})}) \cong -\frac{g_{mc}}{C_2||C_C} \tag{2.29}$$

Comparing the second pole form the Miller Compensation in Equation 2.11. The second pole value is enlarged from $\frac{g_{m2}}{C_L}$ to $\frac{g_{m2}C_C}{C_1 C_L}$ by a factor of $\frac{C_C}{C_1}$. Also, to let the third pole p_3 be

far away from the second pole, the g_{mc} should be large as the equation shown below.

$$\begin{aligned} |p_3| &>> |p2| \\ \frac{g_{mc}}{C_2||C_C} &>> \frac{g_{m2}C_C}{C_1(C_C+C_2)} \\ g_{mc} &>> \frac{g_{m2}C_C(C_2||C_C)}{C_1(C_C+C_2)} \end{aligned} \tag{2.30}$$

So if $g_{mc} \to \infty$, then the third pole $p_3 \to \infty$ according to Equation 2.29 [1]. With the positive effect of the LHP zero, the phase margin could be increased. Since p_1 is the same as the one in Miller Compensation, p_2 is increased by a factor of $\frac{C_C}{C_1}$, and p_3 is far away from the unity gain bandwidth, the overall circuit design ideas and some performance trade-offs are nearly the same as talked in Section 2.3. One more consideration is the added common gate stage which includes g_{mc} and other related parameters from current sources. This stage gives more flexibility to choose their parameters values because this stage is additional and separate [10]. However, one restriction of g_{mc} that must be considered is shown in Equation 2.30. It signifies that the indirect path has to be much faster than the output stage which thus relocates non-dominant poles to higher frequency and thus improving the unity gain frequency [13].

Based on the further observation from Equation 2.24 and Equation 2.29, the non-dominant pole p_3 could be overlapped with the location of the only zero if the parasitic capacitance $C_A \ll C_C$ [13]. Then this Op-Amp works as a Miller Compensated Two-stage Op-Amp with the Voltage Buffer which is talked in Section 2.5.

This common gate stage is proved to deliver wider unity gain bandwidth, higher PSRR and faster response than the Miller compensation [30] [28]. It also overcomes one drawback of the voltage buffer technique that reduces the output swing of the Op-Amp [28]. Some drawbacks regarding this design are that extra transistors are needed to implement the common gate

stage. Also, mismatch between the current sources changes the bias currents in the input stage which affects the input-offset voltage of the op-amp [10].

Chapter 3

Two Stage Operational Amplifier Designs and Simulation Results

3.1 Design Specifications

The specifications that are shown in Table 3.1 will be used to design a two-stage operational amplifier. This table will be used as a standard performance to evaluate different compensation techniques including direct and indirect compensation feedback networks. All these techniques are demonstrated in detail in Chapter 2.

Parameter	Value
DC Gain	70 dB
Gain Bandwidth	$\geq$ 25 MHz
Phase Margin	$\geq 60^{\circ}$
Slew Rate	$\geq$ 15V/μs (preferably $\geq$ 20V/μs)
Power Consumption	0.3 nW

Table 3.1: Design Specifications of Two Stage Amplifier

3.2 Cadence Design and Simulation Result of Traditional Miller Compensation

3.2.1 Design Procedure

Listed below are some useful equations regarding design parameters that will be considered when designing the Miller compensation Op-Amp. Equations 3.2, 3.3, and 3.4 are derived in Section 2.3 as Equations 2.12, 2.15 and 2.16 respectively.

$$g_m = \sqrt{2\mu_{n,p}C_{ox}\frac{W}{L}I_d} \tag{3.1}$$

$$GB = \frac{g_{m1}}{C_C} \tag{3.2}$$

$$g_{m7} \geq 10g_{m1} \tag{3.3}$$

$$C_C \geq 0.2215C_2 \tag{3.4}$$

$$r_O = \frac{1}{I\lambda} \tag{3.5}$$

$$\begin{aligned} First \quad Stage \quad Gain \quad A_{V1} &= -g_{m1}(r_{O1,2}||r_{O3,4}) \\ &= \frac{-2g_{m1}}{I_5(\lambda_{1,2}+\lambda_{2,4})} \end{aligned} \tag{3.6}$$

$$\begin{aligned} Second \quad Stage \quad Gain \quad A_{V2} &= -g_{m7}(r_{O7}||r_{O6}) \\ &= \frac{-g_{m7}}{I_6(\lambda_7+\lambda_6)} \end{aligned} \tag{3.7}$$

$$Slew \quad Rate \quad = \frac{I_5}{C_C} \tag{3.8}$$

Generally, as stated in the last chapter, the main goal to design an amplifier is to have a high gain but also stable, which does not consume a lot of power but can also respond to

the input fast. A Two Stage Amplifier consists of a differential stage and a gain boost stage. Figure 3.1 is a schematic of an uncompensated two stage amplifier where M1-M5 consists of the differential stage and M6 and M7 consists of the gain stage. The first stage consists of NMOS differential inputs with active PMOS load followed by the second stage which is built by PMOS common source amplifier.

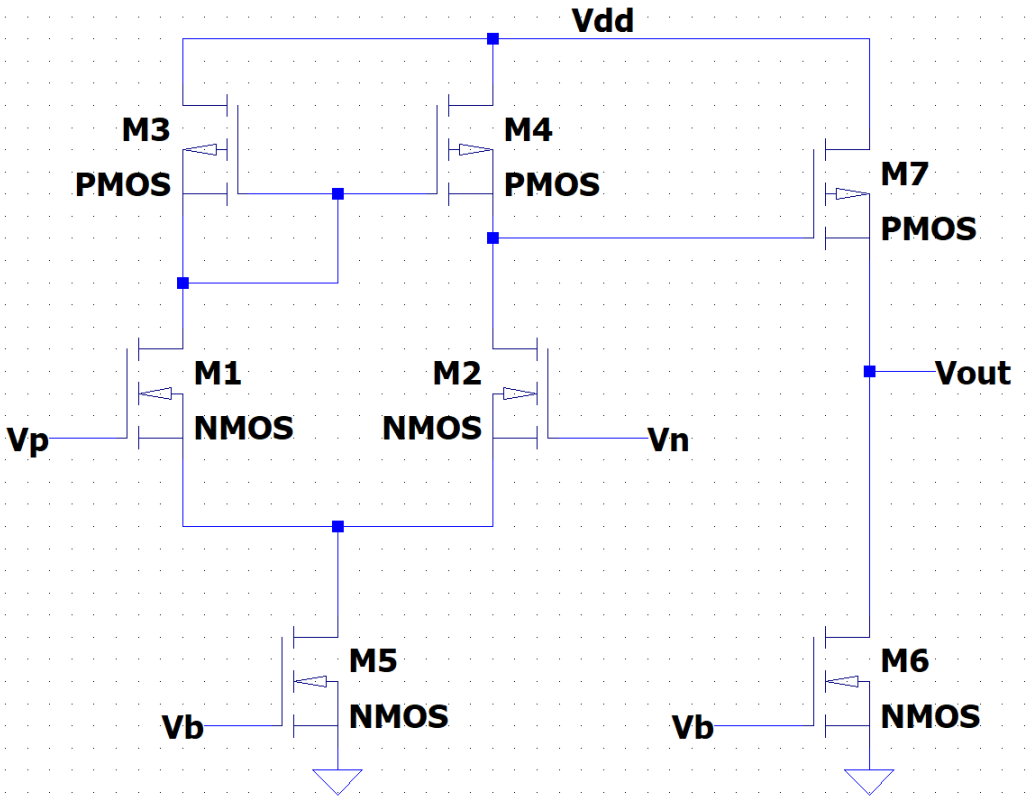


Figure 3.1: Uncompensated Two Stage Operational Amplifier

To obtain a higher gain, the corresponding g_m and r_O need to be increased according to Equation 3.6 and 3.7. Increasing the corresponding $\frac{W}{L}$ can increase both g_m and r_O. Larger g_{m1} can lead to a much larger g_{m7}, which increases the power consumption as a side effect. Increasing g_{m1} can also help provide a wide unity gain bandwidth. $M5$ works as the current source of the differential stage so the size of $M5$ doubles the size of $M1$ or $M2$. Compensation Capacitor C_C is connected between two stages that is shown in Figure 2.5. Increasing C_C

can stabilize the system more by enlarging the phase margin but can also shrink the unity gain bandwidth and decrease the slew rate. Another factor that needs to be considered is the voltage level including the gate voltage of the current source (V_b) and the common mode voltage (V_CM) of both inputs, which is also important to set all the MOSFETs in saturation region. Overall, the main design parameters are $\frac{W}{L}$ of all the MOSFETs and the compensation capacitor C_C, which will be adjusted in the process of Cadence design based on the statements above to reach the standard performance.

3.2.2 Cadence Design Result

Considering all the relationships and restrictions among all the parameters, all the design parameters are properly sized. The ratio of all the MOSFETs of the Miller compensated amplifier is shown in Table 3.2. The actual values of all the parameters are presented in the Cadence Schematic Design shown in Figure 3.2.

Transistor	$\frac{W}{L}$ ratio
M1, M2	15
M3, M4	20
M5	30
M6	50
M7	166.7

Table 3.2: Transistor Sizing

Figure 3.2 depicts the Miller Compensation Op-Amp where the compensation capacitor C_C is set to $500fF$ as the load capacitor is $1pF$ that is not shown in this figure. Also, both Vb and the common mode voltage of inputs are set to $500mV$.

All the results are listed in Table 3.3 after running the simulation. The DC gain and the positive edge slew rate meets the requirement, however, the phase margin trades off with

Parameter	Value
DC Gain	71.62 dB
Gain Bandwidth	22.43 MHz
Phase Margin	57.8°
Positive Edge Slew Rate (SR^+)	29.11V/μs
Negative Edge Slew Rate (SR^-)	15.6V/μs
Power Consumption	150 μW

Table 3.3: Results of Miller Compensation Amplifier

the Gain Bandwidth. Wider unity Gain Bandwidth always shrinks the phase margin which proves the statements in Section 2.3. Figure 3.3 shows the Bode Plot of gain and phase while the Figure 3.4 shows the output response of a step function where the slew rate is measured. Figure 3.5 depicts the Cadence Design test benches, where the load capacitor C_L is attached.

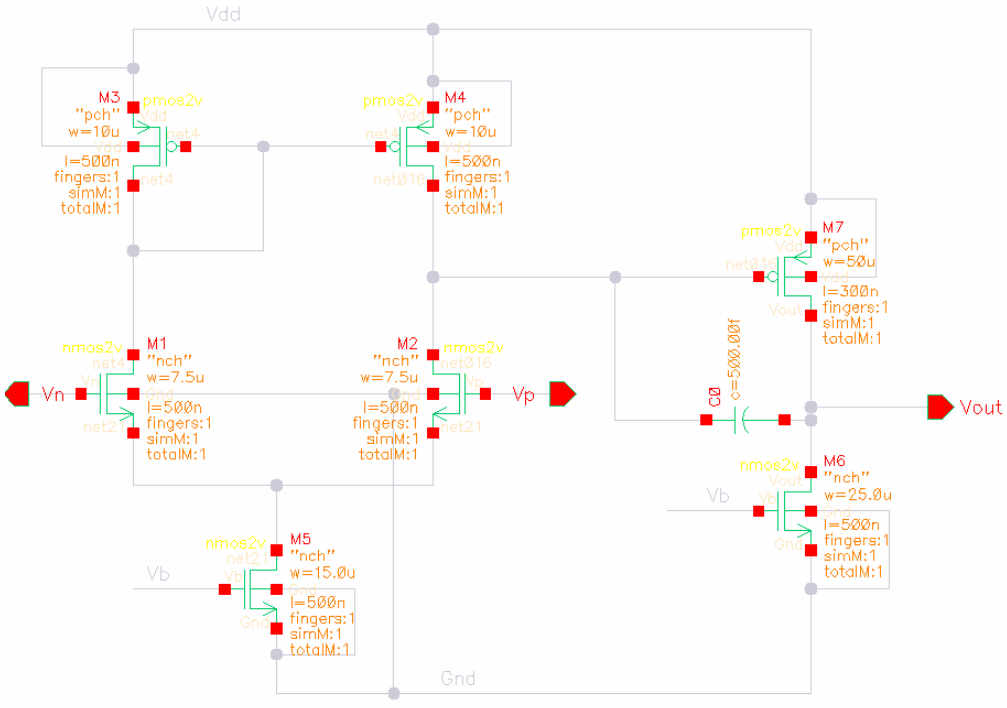


Figure 3.2: Design Schematic of Miller Compensation Amplifier

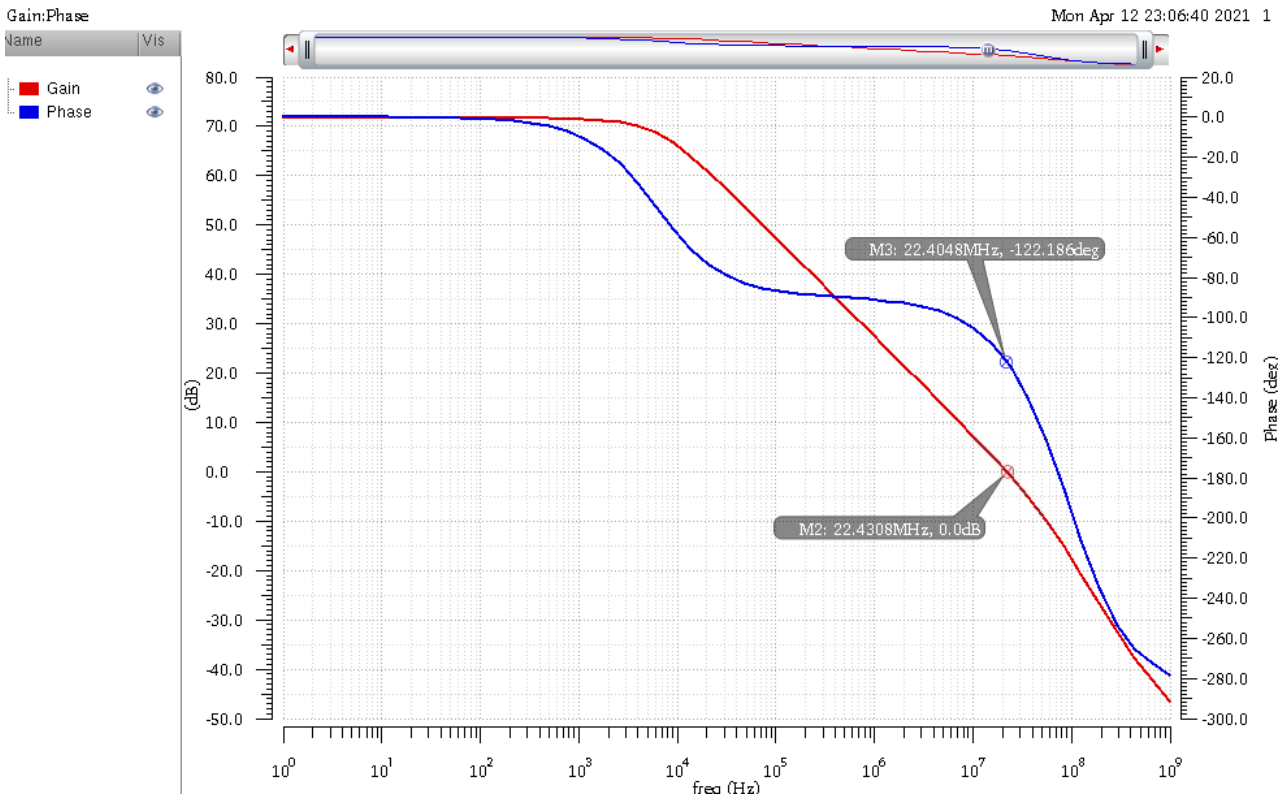


Figure 3.3: Frequency Response of Miller Compensation Amplifier

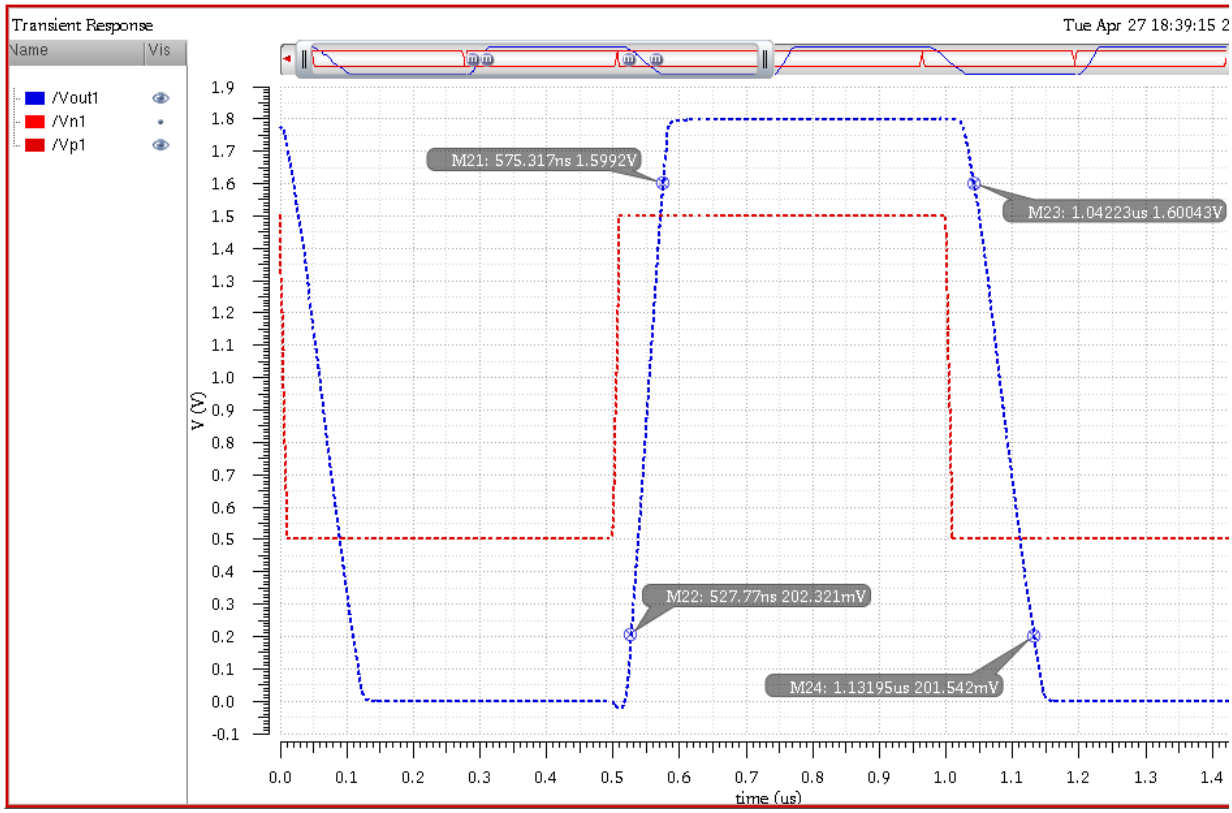


Figure 3.4: Output Response of a Step Function Input

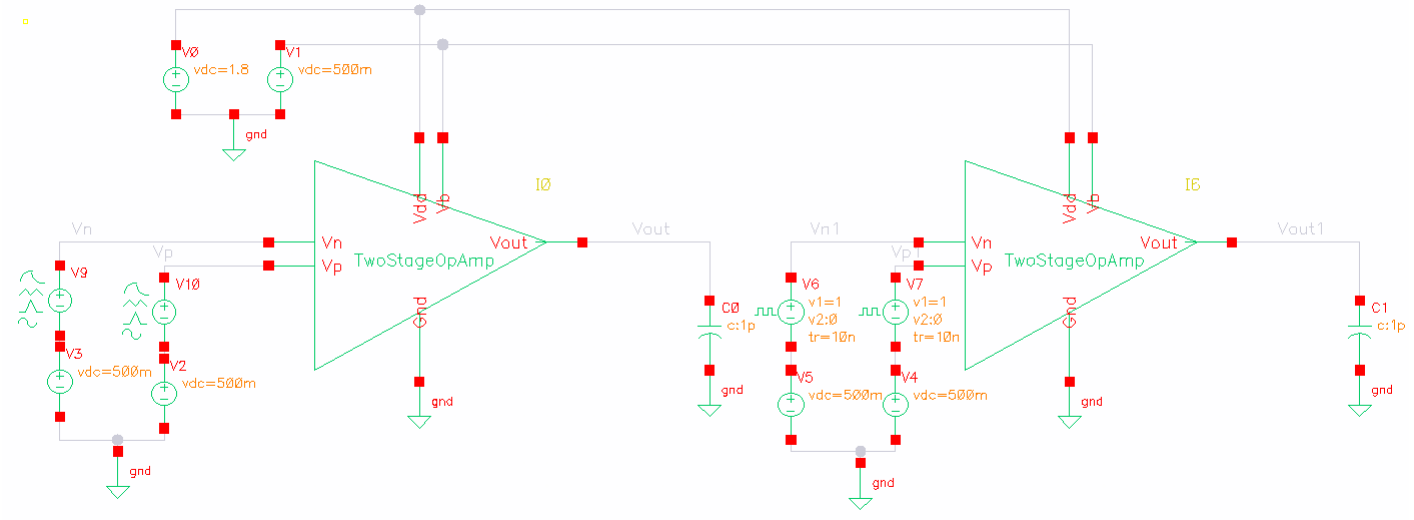


Figure 3.5: Test Bench of Miller Compensation Amplifier

3.3 Cadence Design and Simulation Result of Nulling Resistor Technique

3.3.1 Design Procedure

The whole design procedure is nearly the same as the previous section (traditional Miller compensation) instead of finding the proper position of z_1. Some useful equations that help locate the correct position of z_1 are listed below.

$$z_1 = \frac{1}{(\frac{1}{g_{m7}} - R_Z)C_C} \tag{3.9}$$

$$R_{ON} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_{THn})} \tag{3.10}$$

$$R_{OP} = \frac{1}{\mu_p C_{ox}\frac{W}{L}(V_{SG} - V_{THp})} \tag{3.11}$$

The MOS transistor is picked as R_Z in the whole design, which resistance depends on its overdrive voltage and $\frac{W}{L}$. Since the gate terminal is connected to either the Vdd or ground, the overdrive voltage is considered to be nearly stable. So the design parameters is $\frac{W}{L}$ of this transistor. To make sure the zero appears in the LHP, R_Z needs to be larger than $\frac{1}{g_{m7}}$, according to Equation 3.9. Further derivation is illustrated in the Equation 3.12.

$$\begin{aligned} R_Z &> \frac{1}{g_{m7}} \\ \frac{1}{\mu C_{ox}\frac{W}{L}(|V_{GS} - V_{TH})|} &> \frac{1}{\mu_p C_{ox}\frac{W}{L}(|V_{GS} - V_{TH})|} \\ \frac{1}{\mu\frac{W}{L}V_{od(RZ)}} &> \frac{1}{\mu_p\frac{W}{L}V_{od(M7)}} \\ \mu(\frac{W}{L})_{RZ}V_{od(RZ)} &< \mu_p(\frac{W}{L})_{RZ}V_{od(M7)} \end{aligned} \tag{3.12}$$

Based on this derivation, PMOS is preferred due to its smaller electron mobility μ compared with NMOS, so the ratio of $\frac{W}{L}$ is smaller for PMOS. This could help reduce the size of the design area. The overdrive voltage is depending on lots of parameters that is impossible to be precisely determined in this situation. In Equation 3.9, C_C is another factor that can change the position of this zero. Under this condition, C_C could be decreased to increase the unity gain bandwidth according to Equation 3.2. At the same time, the ratio of $\frac{W}{L}$ must be reduced so the zero can be kept at around the same spot. The advantage of this adjustment is increasing the phase margin and the unity gain bandwidth at the same time. So the main design parameter of the nulling resistor is the ratio $\frac{W}{L}$ of this added PMOS transistor.

3.3.2 Cadence Design Result

Knowing from Section 3.2.2, using one single Miller Capacitor in the feedback network is hard to meet all the required standards. However, adding a nulling resistor in series with the capacitor can improve the performance of the amplifier in stability and unity gain bandwidth. To reach all the requirements from Table 3.1, all the design parameters are properly adjusted and sized. The ratio of $\frac{W}{L}$ of each transistor is shown in Table 3.4.

Transistor	$\frac{W}{L}$ ratio
M1, M2	15
M3, M4	20
M5	30
M6	50
M7	166.7
M8	5.6

Table 3.4: Transistor Sizing

Figure 3.6 shows the Cadence design schematic of the Op-Amp where all the parameters are labeled. All transistors keep the same size but the size of the compensation capacitor is

reduced to $400fF$. The output capacitor is still $1pF$ that is now shown in this graph. Vdd and Vb keep the same, which are $1.8V$ and $500mV$ respectively.

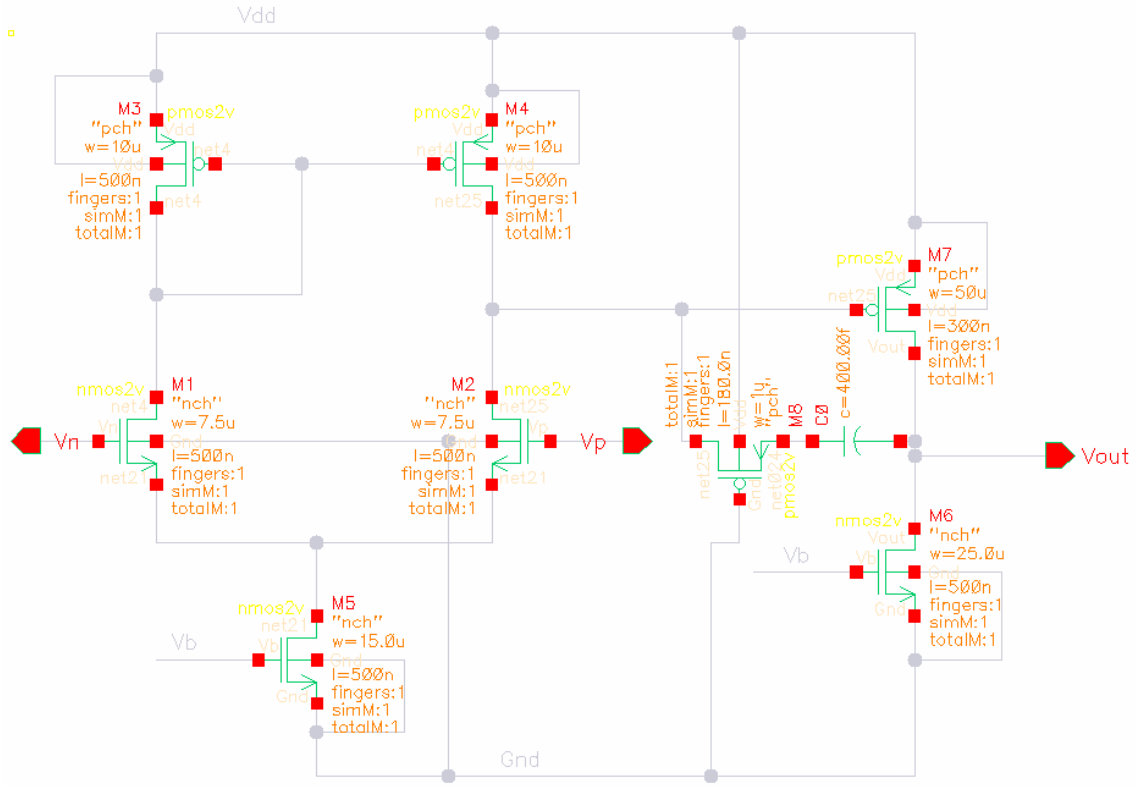


Figure 3.6: Design Schematic of Amplifier with Nulling Resistor

Parameter	Value
DC Gain	71.62 dB
Gain Bandwidth	27.1 MHz
Phase Margin	65.4°
Positive Edge Slew Rate (SR^+)	36.36V/μs
Negative Edge Slew Rate (SR^-)	16.55V/μs
Power Consumption	149.8 μW

Table 3.5: Results of 2 Stage Amplifier with Nulling Resistor

All the results, that are listed in Table 3.5, meet all the requirements. Figure 3.7 shows the

Bode Plot of gain and phase while the Figure 3.8 shows the output response of a step function where the slew rate is measured. Figure 3.9 depicts the Cadence design test benches where the load capacitor is added. Slew rate is increased compared with the Miller compensation result because the value of C_C is smaller. So overall, by comparing Table 3.5 with Table 3.3, adding a nulling resistor in series with the compensation capacitor improves the performance of the amplifier in phase margin, the unity gain bandwidth, and the positive edge slew rate.

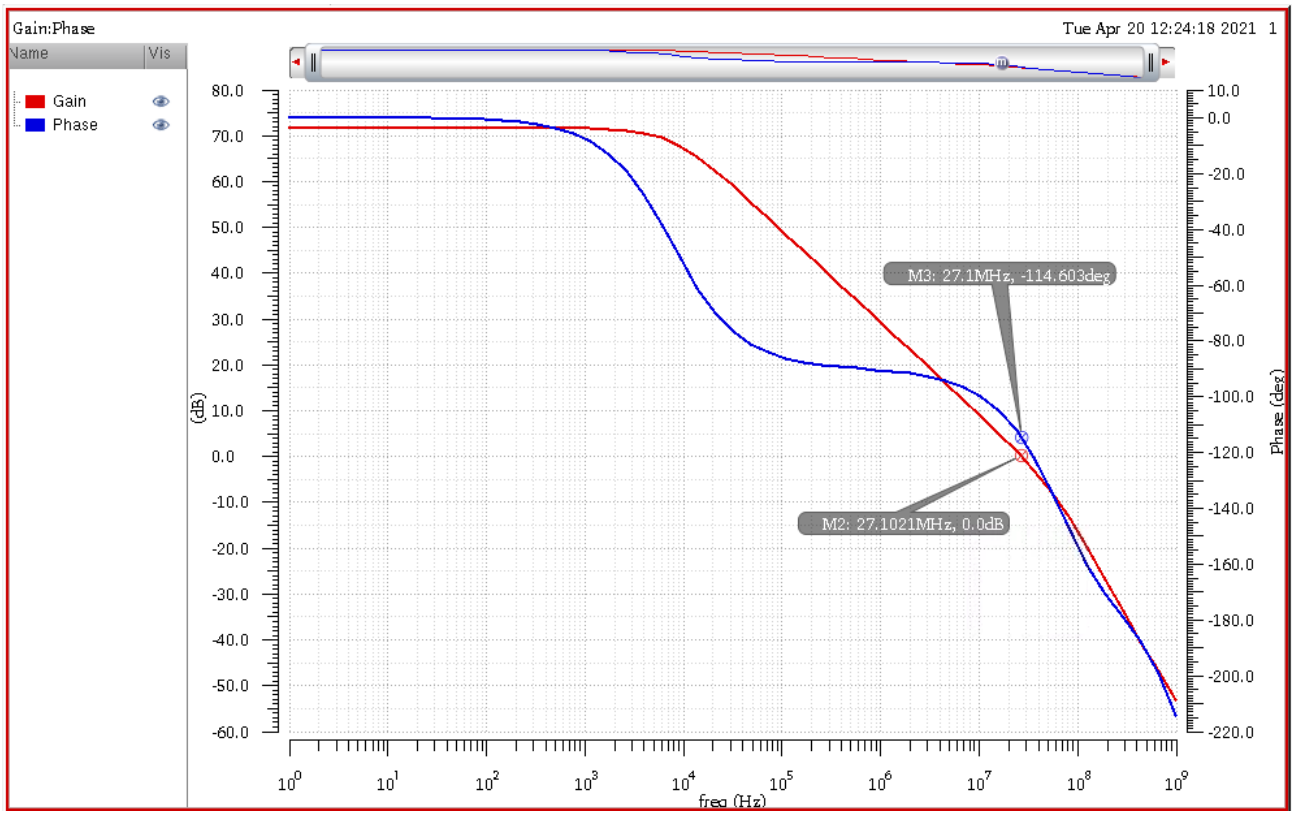


Figure 3.7: Frequency Response of Amplifier with Nulling Resistor

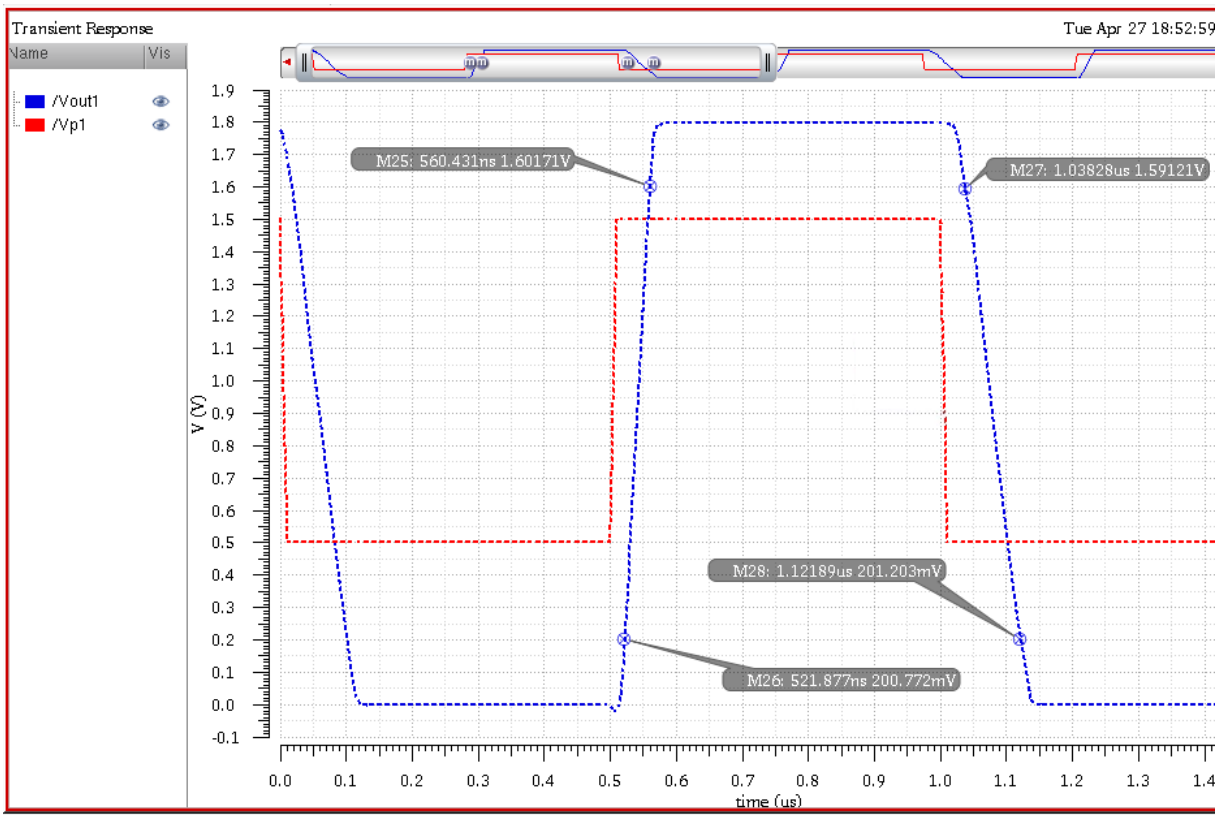


Figure 3.8: Output Response of a Step Function Input

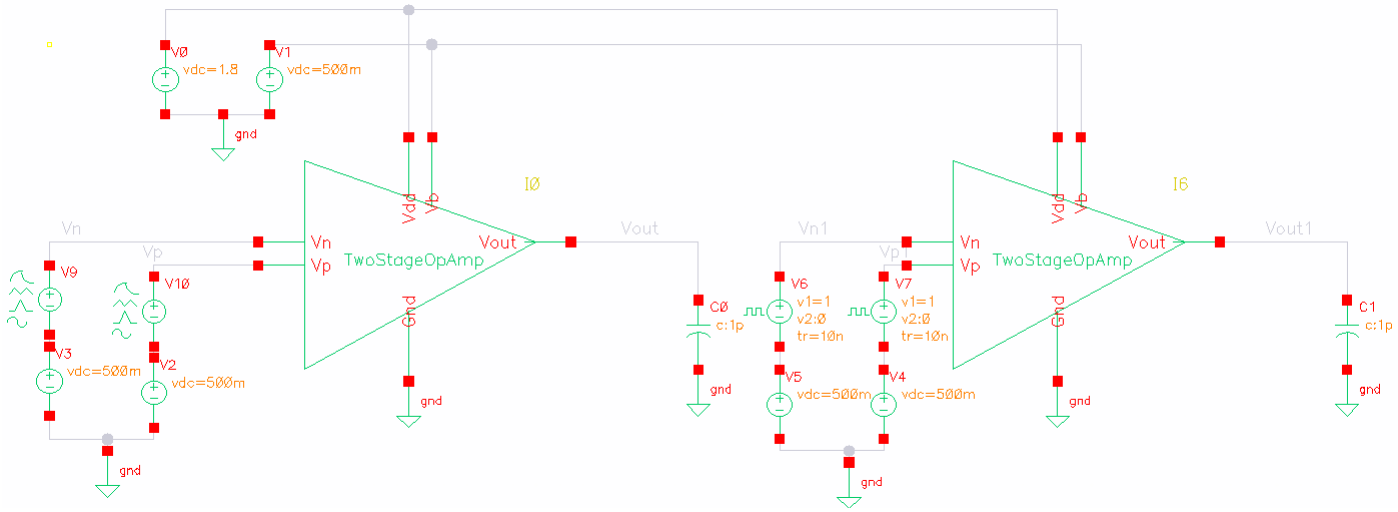


Figure 3.9: Test Bench of Miller Compensation Amplifier with Nulling Resistor

3.4 Cadence Design and Simulation Result of Voltage Buffer Technique

The implementation of the voltage buffer onto the Op-Amp is fully illustrated in Section 2.5. This voltage buffer can be achieved by either using a PMOS source follower or a NMOS source follower. NMOS source follower is picked in this design since the existing drive voltage of NMOS current source. Shown in the Figure 3.10, NMOS $M9$ and $M8$ have the same size which work as a current source and a source follower respectively. The size of all other transistors and the compensation capacitor is also presented in this schematic, which is the same as nulling resistor technique.

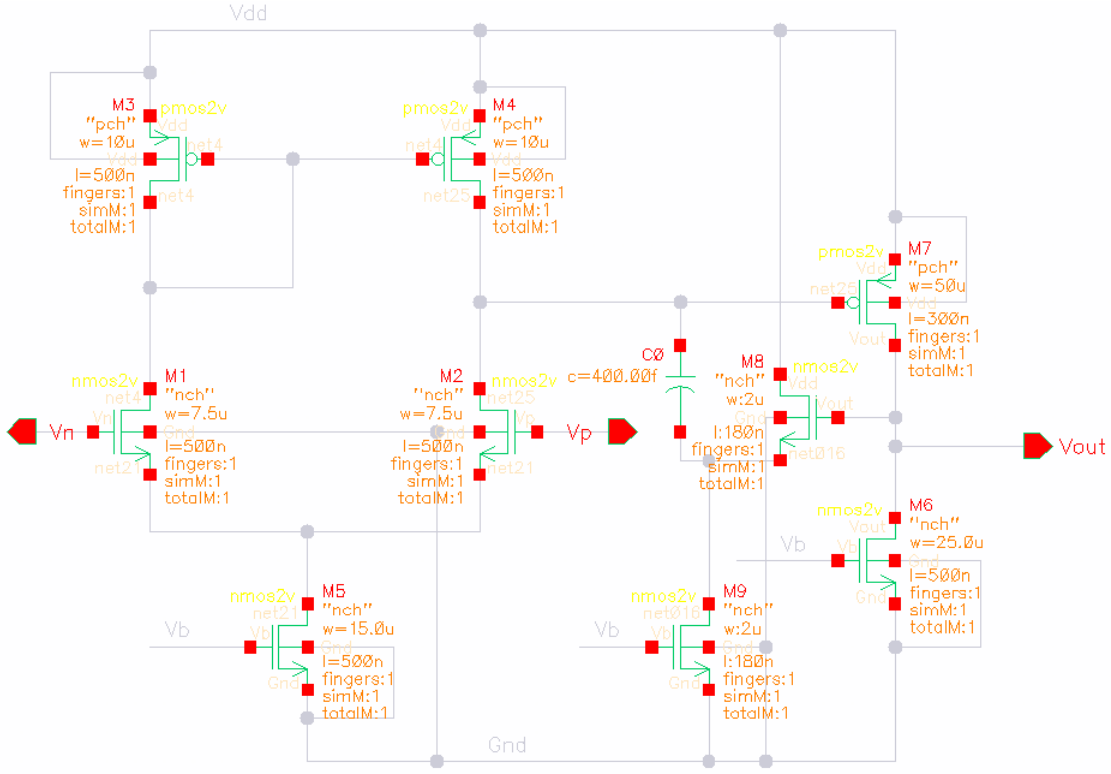


Figure 3.10: Design Schematic of Amplifier with Voltage Buffer

The ratio $\frac{W}{L}$ of each transistor is shown in Table 3.6. The compensation capacitor is set to

be $400fF$, while the output capacitor is set to be $1pF$ that is not presented in the schematic. Vdd and Vb keep the same, which are $1.8V$ and $500mV$ respectively.

Transistor	$\frac{W}{L}$ ratio
M1, M2	15
M3, M4	20
M5	30
M6	50
M7	166.7
M8	11.1
M9	11.1

Table 3.6: Transistor Sizing

All the results are listed in Table 3.7. The improvement of phase margin, unity gain bandwidth, and slew rate are dramatic. This result can also reflect how negatively the RHP zero affects. By removing this zero, this Op-Amp becomes more stable, has a wider range of application frequency, and is able to respond faster. The only drawback is more power consumption due to source follower path. All in all, the Op-amp with the source follower in the feedback network scores the best results so far.

Parameter	Value
DC Gain	71.62 dB
Gain Bandwidth	34.67 MHz
Phase Margin	74.19°
Positive Edge Slew Rate (SR^+)	57.88V/μs
Negative Edge Slew Rate (SR^-)	23.72V/μs
Power Consumption	180 μW

Table 3.7: Results of 2 Stage Amplifier with Voltage Buffer

Figure 3.11 shows the Bode Plot of gain and phase while Figure 3.12 shows the output response of a step function where the slew rate is measured. Test benches and the load

capacitor keep the same as the previous section.

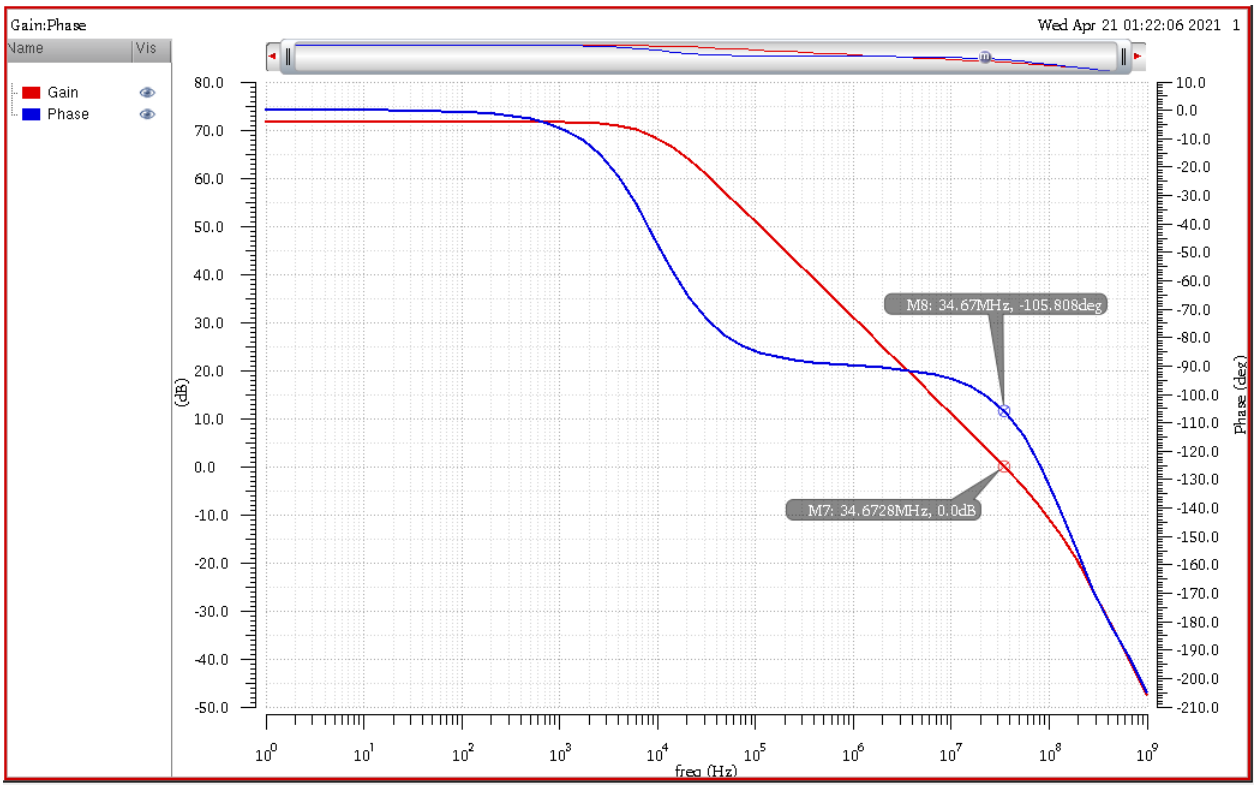


Figure 3.11: Frequency Response of Amplifier with Voltage Buffer

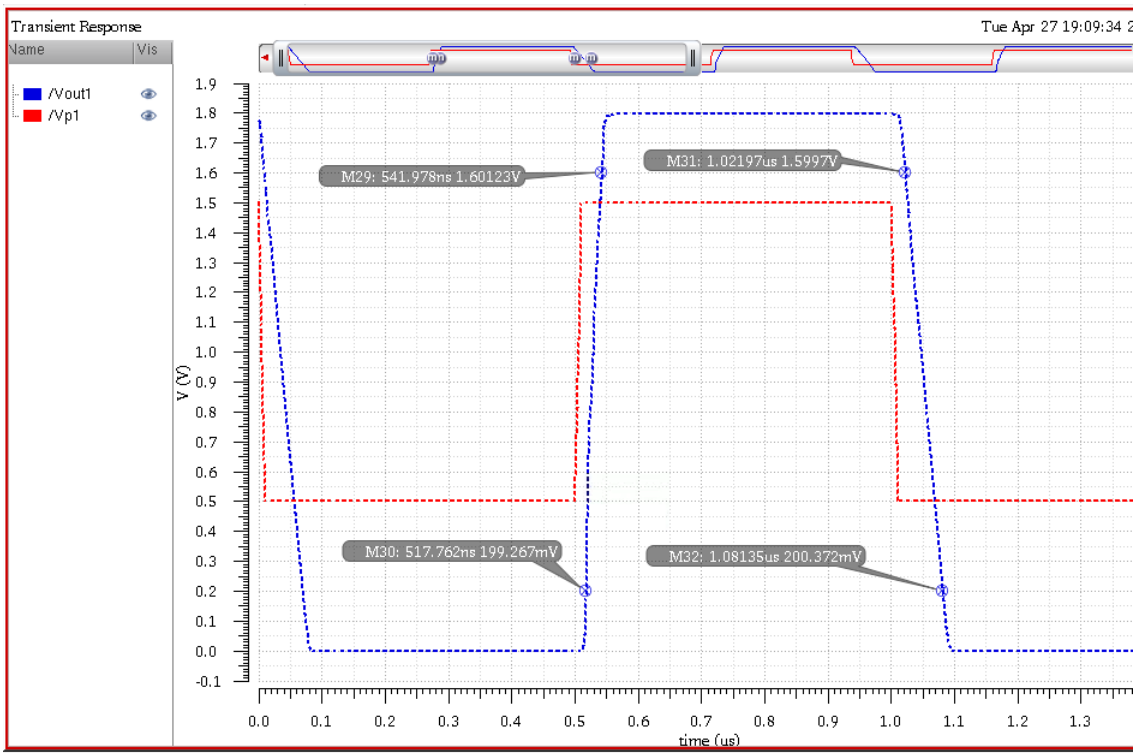


Figure 3.12: Output Response of a Step Function Input

3.5 Cadence Design and Simulation Result of Common Gate Compensation

The whole design idea of the common gate compensation is very similar to Miller Compensation instead of additional adjustments regarding the common gate compensation. Some useful equations are listed below which are derived in Section 2.6.2.

$$p_1 = -\frac{1}{g_{m2}R_2R_1C_C} \tag{3.13}$$

$$p_2 = -\frac{g_{m2}C_C}{C_1(C_C + C_2)} \cong \frac{g_{m2}C_C}{C_1C_L} \tag{3.14}$$

$$p_3 = -(\frac{g_{mc}}{C_2||C_C} + \frac{1}{C_1(R_1||R_{OC})}) \cong -\frac{g_{mc}}{C_2||C_C} \tag{3.15}$$

$$z_1 = -\frac{b_0}{b_1} = -\frac{g_{mc}}{C_C + C_A} \tag{3.16}$$

$$g_{mc} >> \frac{g_{m2}C_C(C_2||C_C)}{C_1(C_C + C_2)} \tag{3.17}$$

From Equation 3.15, 3.16, and some theories that are talked in Section 2.6.2, g_{mc} needs to be large so that p_3 and z_1 can be pushed away from the unity gain bandwidth so do their effects on phase margin. According to Equation 3.1, a large value of g_{mc} can be given by a large ratio of corresponding $\frac{W}{L}$ combined with large related current. So the corresponding two current sources (M_8, M_9) of this stage need to be adjusted to support this condition. During the design process, the value of the compensation capacitor C_C is also increased due to the position of p_2 and its negative effect on phase margin. So C_C is increased to $800fF$ to push p_2 away from the unity gain bandwidth. After increasing the value of the compensation capacitor, g_{mc} needs an equivalent increment based on Equation 3.17. The current loads M_3 and M_4, and the current mirror load M_6 are also adjusted to maintain the sufficient gain.

The entire schematic of common gate compensation two-stage Op-Amp is shown in Figure 3.13, where all the values of parameters are labeled.

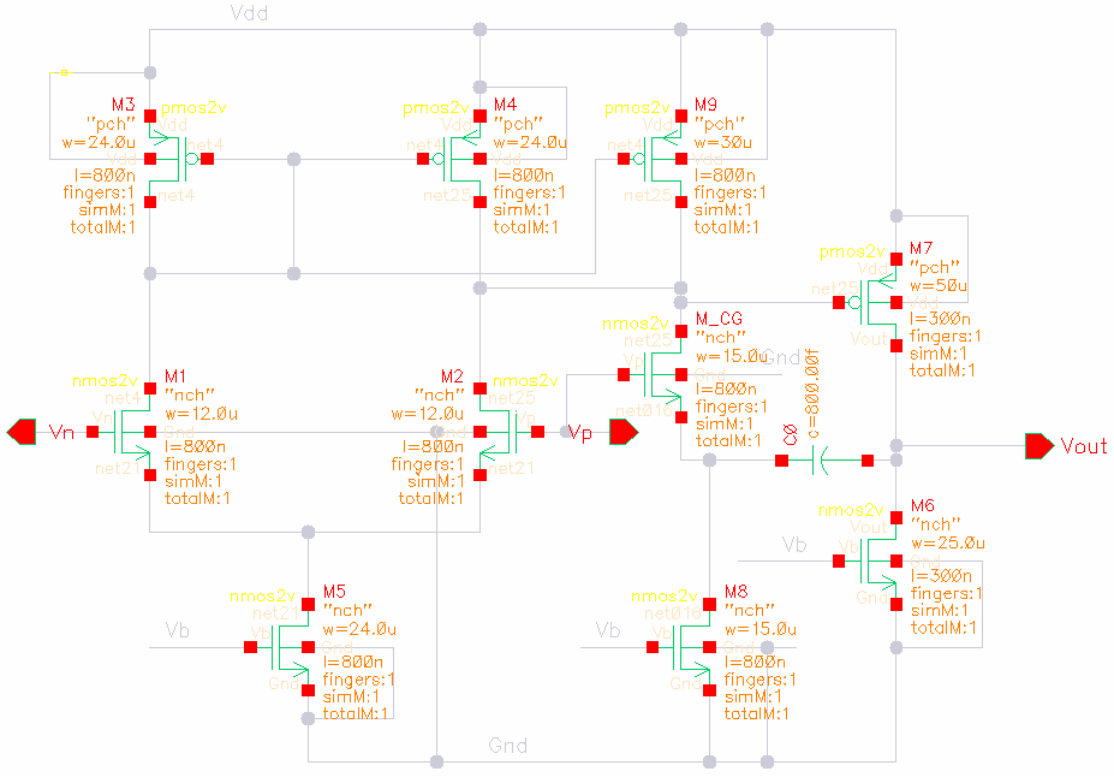


Figure 3.13: Design Schematic of Amplifier with Common Gate Compensation

Transistor	$\frac{W}{L}$ ratio
M1, M2	15
M3, M4	30
M5	30
M6	83.3
M7	166.7
M_{CG}	18.75
M8	18.75
M9	37.5

Table 3.8: Transistor Sizing

The ratio $\frac{W}{L}$ of each transistor is shown in Table 3.8. The compensation capacitor is set to be $800fF$, while the output capacitor is set to be $1pF$ that is not presented in the schematic.

Vdd and Vb keep the same, which are $1.8V$ and $500mV$ respectively. Figure 3.14 depicts the Bold Plot, and Figure 3.15 shows the output response of a step input function, where the slew rate is measured.

Parameter	Value
DC Gain	70.83 dB
Gain Bandwidth	85.4 MHz
Phase Margin	62.56°
Positive Edge Slew Rate (SR^+)	366.9V/μs
Negative Edge Slew Rate (SR^-)	21.74V/μs
Power Consumption	261u W

Table 3.9: Results of 2 Stage Amplifier with Voltage Buffer

Both DC gain and phase margin meets the standard requirements but the cost is increasing the size of C_C. The improvement of unity gain bandwidth is remarkable compared with Miller Compensation. The major reason of the unity gain bandwidth increment is because the dominant pole p_1 is pushed to the higher frequency direction by observing the frequency response of Miller Compensation and common gate compensation (Figure 3.3, and 3.14). This is mainly caused by increased C_C according to Equation 3.13. The non-dominant poles p_2 and p_3 with the zero z_1 are located at higher frequency regarding to unity gain frequency, however, they still have little effect on phase margin of the Op-Amp system by looking at the phase plot (Figure 3.14) at the unity gain frequency. The positive edge slew rate has a huge difference with the negative edge slew rate which is also caused by the increased value of the compensation capacitor C_C. Power Consumption is also increased due to this additional common gate stage. Further parameters adjustment of this strategy is needed to deliver a better performance.

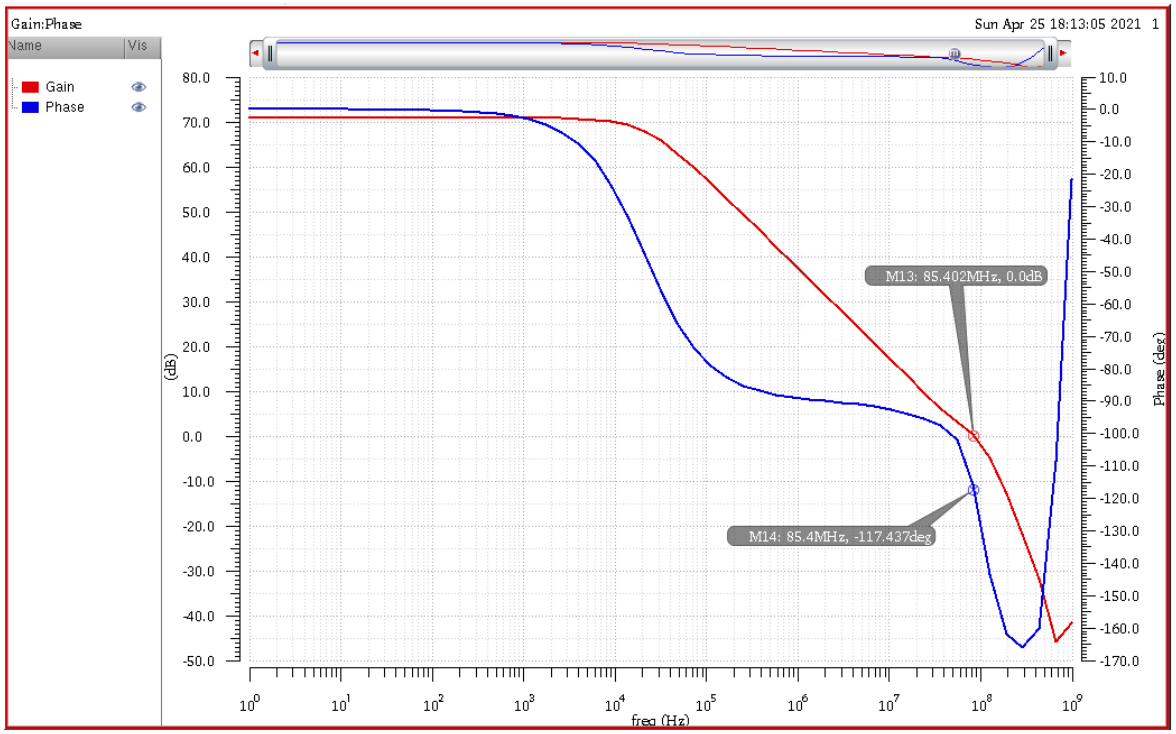


Figure 3.14: Frequency Response of Amplifier with Common Gate Compensation

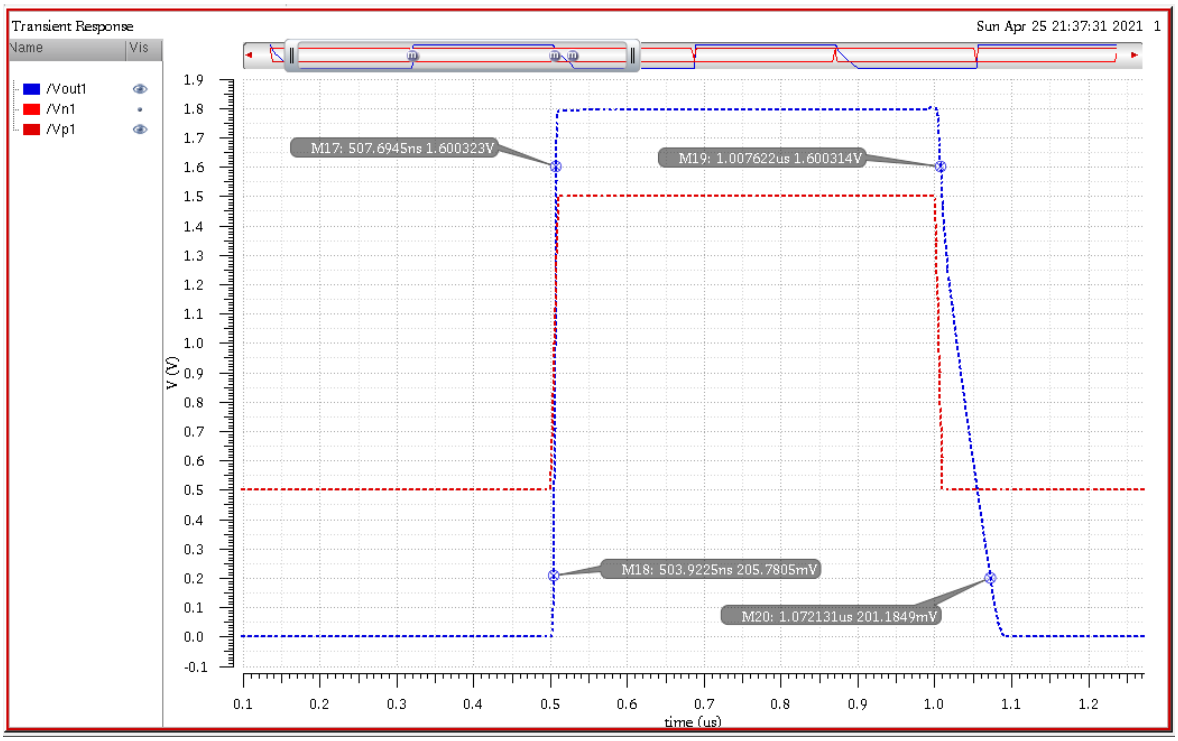


Figure 3.15: Output Response of a Step Function Input

Chapter 4

Conclusions

First, this paper states the reason why an uncompensated two-stage Op-Amp is unstable, and then discusses and demonstrates the compensation techniques including the Miller compensation, the nulling resistor, the voltage buffer, and the common gate stage. Besides the phase margin that affects the stability of operational amplifiers. There are several other performance factors that are taken into account in this paper when designing the two-stage Op-Amp, including DC gain, unity gain frequency, slew rate, and power consumption. Traditional Miller compensated amplifiers (a single compensation capacitor amplifier) have less phase margin, and smaller unity gain bandwidth, but it can provide sufficient DC gain. Keeping the size of all transistors and the compensation capacitor and adding a nulling resistor in series with the compensation capacitor, can improve the amplifier phase margin and the slew rate. In addition to improvements of the phase margin and the slew rate, voltage buffer implementation makes the unity gain bandwidth wider. However, voltage buffer technique costs more power due to the additional path from Vdd to ground. The common gate stage compensates the Op-Amp indirectly as a current buffer, which boosts the response speed and unity gain bandwidth but costs more power. Meanwhile, there are other compensation techniques that are not included in this paper and some of them have been developed specifically for their application. All in all, among all the compensation techniques talked in this paper, their advantages and disadvantages should be explored more in real world applications or as units of the entire design.

Chapter 5

Application and Future work

After talking with Dr. Yi and Kangjun, my designed Op-Amps could be used in several places of Neural Network research. Including: the delay calibration module in DFR [3], and the MAC operator of Neural Network [4]. Both related works are shown in Figure 5.1 and 5.2. Kangjun mentioned that the working frequency range of both works are relatively low, and also higher open loop gains are preferred. The good news is high gain trades off with unity gain bandwidth so the corresponding trans-conductance of the amplifier could be increased to enlarge the gain and decrease the gain bandwidth. Other enhancements and adjustments of the applied amplifiers will be applied after following up with Kangjun.

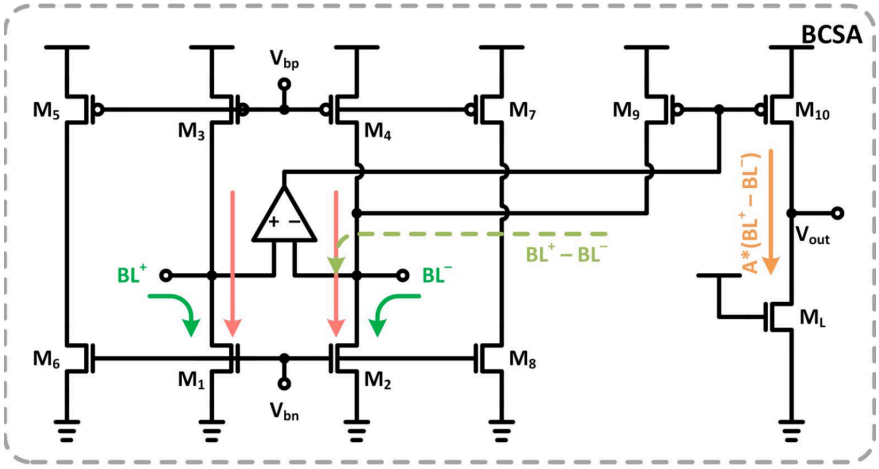


Figure 5.1: MAC Operator [4]

Another improvement of the designed op-amp is regarding the common gate amplifier. From

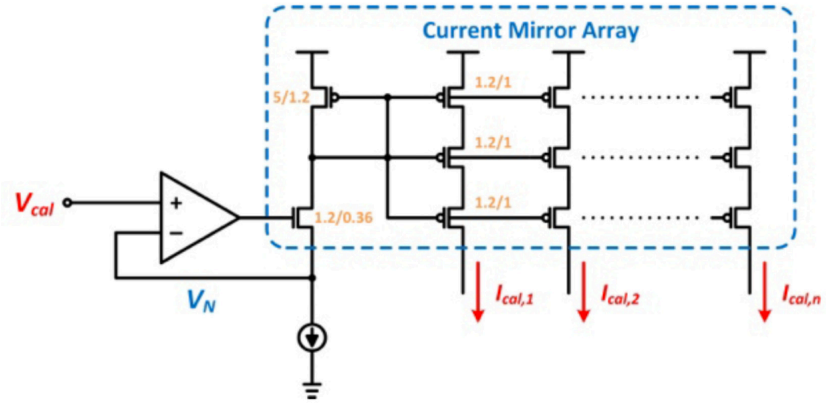


Figure 5.2: Delay Calibration Module [3]

Figure 3.14, the phase response of the Bode plot is increased dramatically at higher frequency range. This undesired situation might be caused by the added stage which increases the transition time to process the signal, so higher frequency can not provide enough process time for it to transfer the signal. Additionally, the compensation capacitor is increased to meet the op amp standard performance. So another future work regarding this common gate stage is adjusting the parameters of all the Mosfets to shrink the capacitor size that can deliver the same performance.

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