Enhanced Gate-Driver Techniques and SiC-based Power-cell Design and Assessment for Medium-Voltage Applications

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Dissertation submitted to the faculty of the Virginia Polytechnic Institute and State University in partial fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical Engineering

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December 1st, 2021
Blacksburg, Virginia

Keywords: SiC MOSFET, gate-driver, medium-voltage, power cell, junction temperature estimation, design and assessment, modular multilevel converter

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Due to the limitations of silicon (Si), there is a paradigm shift in research focusing on wide-bandgap-based (WBG) materials. SiC power semiconductors exhibit superiority in terms of switching speed, higher breakdown electric field, and high working temperature, slowly becoming a global solution in harsh medium-voltage (MV) high-power environments. However, to utilize the SiC MOSFET device to achieve those next-generation, high-density, high-efficiency power electronics converters, one must solve a plethora of challenges.

For the MV SiC MOSFET device, a high-performance gate-driver (GD) is a key component required to maximize the beneficial SiC MOSFET characteristics. GD units must overcome associated challenges of electro-magnetic interference (EMI) with regards to common-mode (CM) currents and cross-talk, low driving loop inductance required for fast switching, and device short-circuit (SC) protection. Developed GDs (for 1.2 kV, and 10 kV devices) are able to sustain $dv/dt$ higher than 100 V/ns, have less than 5 nH gate loop inductance, and SC protection, turning off the device within 1.5 $\mu s$.

Even with the introduction of SiC MOSFETs, power devices remain the most reliability-critical component in the converter, due to large junction temperature ($T_j$) fluctuations causing accelerated wear-out. Real-time (online) measurement of the $T_j$ can help improve long-term reliability by enabling active thermal control, monitoring, and prognostics. An online $T_j$ estimation is accomplished by generating integrated intelligence on the GD level. The
developed $T_j$ sensor exhibits a maximum error less than 5°C, having excellent repeatability of ±1.2°C. Additionally, degradation monitoring and an aging compensation scheme are discussed, in order to maintain the accuracy of the sensor throughout the device’s lifetime.

Since ultra high-voltage SiC MOSFET devices (>20 kV) are impractical, the modular multilevel converter (MMC) emerged as a prospective topology to achieve MV power conversion. If the kernal part of the power-cell (main constitutive part of the MMC converter) is an SiC MOSFET, the design is able to achieve very high-density and high-efficiency. To ensure a successful operation of the power-cell, a systematic design and assessment methodology (DAM) is explored, based on the 10 kV SiC MOSFET power-cell. It simultaneously addresses challenges of high-voltage insulation, high $dv/dt$ and EMI, component and system protections, as well as thermal management. The developed power-cell achieved high-power density of 11.9 kW/l, with measured peak efficiency of $\eta = 99.3\% @10$ kHz. It successfully operated at $V_{dc} = 6$ kV, $I = 84$ A, $f_{sw} \geq 5$ kHz, $T_j \leq 150$ °C and had high switching speeds over 100 V/ns.

Lastly, to achieve high-power density and high-efficiency on the MV converter level, challenges of high-voltage insulation, high-bandwidth control, EMI, and thermal management must be solved. Novel switching cycle control (SCC) and integrated capacitor blocked-transistor (ICBT) control methodologies were developed, overcoming the drawbacks of conventional MMC control. These novel types of control enable extreme reduction in passive component size, increase the efficiency, and can operate in dc/dc, dc/ac, mode, potentially opening the modular converter to applications in which it was not previously used. In order to explore the aforementioned benefits, a modular, scalable, 2-cell per arm, prototype MV converter based on the developed power-cell is constructed. The converter successfully operated at $V_{dc} = 12$ kV, $I = 28$ A, $f_{sw} = 10$ kHz, with high switching speeds, exhibiting high transient immunity in both SCC and ICBT.
Enhanced Gate-Driven Techniques and SiC-based Power-cell Design and Assessment for Medium-Voltage Applications

Slavko Moćević

GENERAL AUDIENCE ABSTRACT

In medium-voltage applications, such as an electric grid interface in highly populated areas, a ship dc system, a motor drive, renewable energy, etc., land and space can be very limited and expensive. This requires the attributes of high-density, high-efficiency, and reliable distribution by a power electronics converter, whose central piece is the semiconductor device. With the recent breakthrough of SiC devices, these characteristics are obtainable, due to SiC inherent superiority over conventional Si devices. However, to achieve them, several challenges must be overcome and are tackled by this dissertation. Firstly, as a key component required to maximize the beneficial SiC MOSFET characteristics, it is of utmost importance that the high-performance gate-driver be immune to interference issues caused by fast switching and be able to protect the device against a short-circuit, thus increasing the reliability of the system. Secondly, to prevent accelerated degradation of the semiconductor devices due to high-temperature fluctuations, real-time (online) measurement of the $T_j$ is developed on the gate-driver to help improve long-term reliability. Thirdly, to achieve medium-voltage high-power density, high-efficiency modular power conversion, a converter block (power-cell) is developed that simultaneously addresses the challenges of high-voltage insulation, high interference, component and system protections, and thermal management. Lastly, a full-scale medium-voltage modular converter is developed, exploiting the advantages of the fast commutation speed and high switching frequency offered by SiC, meanwhile exhibiting exceptional power density and efficiency.
To My Family

My Mother: Branka Moćević
My Father: Momčilo Moćević
My Sister: Ksenija Zečar

Thank you for your unconditional love and endless support.
First and foremost, I would like to express my deepest gratitude to my advisor, Dr. Dushan Boroyevich, for his invaluable guidance, continuous support, advice, and patience, as well as for the priceless opportunity and privilege to be a part of CPES. Dr. Boroyevich’s knowledge, abundant experience, creativity, and philosophy have helped me immensely and encouraged me to strive towards maximum excellence and improvement throughout my academic research and daily life. For that, I am forever grateful. Always smiling with an amazing attitude and a great sense of humor, it was my great honor having Dr. Boroyevich as an academic advisor.

Since day one in CPES, Dr. Rolando Burgos has been immensely understanding, helpful, and supportive throughout all of my endeavours, from relatively simple tasks through complex challenges. His guidance in research, his support, and his advice were instrumental in my quest to become a better engineer. Our discussions during weekly meetings were extremely beneficial and of most importance towards my degree and overcoming any research difficulties. I cannot thank him enough for believing and trusting in me, even when I did not believe in myself. It was my pleasure and honor having him as my co-adviser.

I am deeply indebted to Dr. Jun Wang. His guidance and advice in doing research, understanding lab equipment, and experimental testing, began from my first day in CPES; all of which I will carry and cherish all of my life. Thank you for all of your insight and for teaching me the importance of using a systematic approach to research problems. Dr. Wang immensely raised the quality of my work through his advice on preparing presentations and writing papers. I appreciate every single minute of our discussions and for always finding time for me, whether it was early morning or so late that it was already morning.

I would like to extend my sincere thanks to my committee members, including Dr. G.Q. Lu
and Dr. Virgilio Centeno, for their valuable comments, feedback, and insightful suggestions that helped me throughout my research, during the preliminary examination, as well as for the final defense.

I would like to thank the remaining CPES faculty who all invested some of their time and effort to help me achieve my professional and personal goals: Dr. Fred C. Lee, Dr. Khai Ngo, Dr. Qiang Li, Dr. Igor Cvetkovic, Dr. Christina Di Marino, Dr. Yuhao Zhang, Dr. Dong Dong, Dr. Boran Fan, Dr. Bo Wen, and Dr. Richard Zhang. I would also like to share my appreciation to the CPES staff who are instrumental to all of CPES and for being there for every silly request I made: David Gilham, Teresa Shaw, Linda Long, Marianne Hawthorn, Trish Rose, Lauren Shutt, Na Ren, Dennis Grove, Matthew Scanland, Neil Croy, Yan Sun, Audri Cunningham, Brandy Grim, Angela Diamon, and Ling Li.

In addition to the wonderful CPES staff, I had the pleasure of working with and learning from many remarkable individuals. All of them were essential in the success of this work. Dr. Joseph Kozak always provided insightful and valuable comments regardless of whether we were in the lab or having an outdoor break enjoying a glass of IPA, Mr. Jianghui Yu, Dr. Yue Xu, Dr. Keyao Sun, Mr. Joshua Stewart, Ms. Jiewen Hu, Ms. Ning Yan, Mr. He Song, Ms. Yu Rong, Mr. Vladimir Mitrovic, Mr. Nguyen Tam, Mr. Jayesh Kumar Motwani, Mr. Xiang Lin, Ms. Grace Watt, Mr. Ruizhe Zhang, Ms. Lakshmi Ravi, Mr. Yijie Bai, Mr. Minh Ngo, Mr. Gibong Sun, Mr. Shuo Wang, Mr. Feiyang Zhu, Mr. Cong Tu, and many others to name.

Finally, I must express my very profound gratitude to my parents Momcilo and Branka Mocevic, and to my sister Ksenija Zecar and her husband Goran Zecar, for providing me with unfailing support and continuous encouragement. Special thanks also goes to Slobodan Gataric for creating an initial spark of interest for power electronics, Milan Mocevic, Niloofar Heydarian, and the rest of my family and friends. This accomplishment would not have been possible without you. Thank you.
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Chapter 1

Introduction

1.1 Background: Penetration of WBG Devices into Medium-Voltage Applications

Currently, for medium-voltage (MV) applications, power semiconductor devices with high-voltage, high performance, high temperature operation capabilities, and high density are required \[1\]. With the limitations of Si in mind, including limited voltage ratings, slow switching speed, and predominantly large footprint, there is now a paradigm shift in research focus from Si material to wide-bandgap-based (WBG) material systems. This is especially true for SiC power semiconductors which are being rapidly developed \[2\]. Compared to Si, SiC material exhibits inherent superiority in terms of faster switching speed, lower specific on-state resistance, higher breakdown electric field, and high working temperature \[3\], \[4\]. For MV converters, SiC MOSFETs are directly replacing their Si counterparts, and SiC MOSFET modules are slowly becoming a global solution in harsh MV high-power environment, high-reliability power electronics systems.

In many systems, the MV SiC MOSFET can offer benefits in the following aspects:

1. Due to faster switching rates and low specific on-state resistance, the device exhibits low losses, ultimately leading to higher efficiency \[1, 5, 6, 7\]. This, combined with the device’s smaller footprint, can lead to reduced cooling requirements, thus exhibiting
higher power density. Furthermore, low losses and faster switching speed can lead to higher switching frequency. This ultimately reduces passive component size, leading to a reduction in size, volume, and weight, as well as cost \[6, 8\].

2. Due to a higher breakdown electric field, higher blocking voltage devices (such as 10 and 15 kV SiC MOSFETs) can enable converter topology simplifications. For example, for three- and five-level, neutral-point-clamped, cascaded H-bridge topologies, a simple two-level can be used, reducing the complexity of control schemes while preserving the overall harmonic performance with high switching frequency \[9, 10\].

3. The high working temperature nature of SiC enables its utilization in new applications that Si have not been able to penetrate, such as aviation, oil drilling, and electrical vehicle areas \[11, 12, 13, 14\].

4. Superior features of SiC can enable new or enhanced functionalities and applications \[9, 15\]. For example, with high switching speed and frequency, higher control bandwidth and faster dynamic response can be enabled \[2\]. These features can lead to new or enhanced functionalities in existing applications or even new applications. Furthermore, power quality can also be improved \[16\].

In the past decade or so, MV SiC converters have been extensively researched and utilized in a wide variety of applications. Some of them are smart-grid distribution and interface \[17, 18\], MVDC Microgrids \[19\], industrial motor drives \[8\], electric-ships \[20\], railway traction \[21, 22\], fast charging stations\[23, 24\], STATCOMs \[25\], renewable energy systems \[26, 27\], more electric aircraft \[13, 28\], and data centers \[29\].
1.2 Research Motivations and Objectives

1.2.1 SiC MOSFET Challenges in Medium-Voltage Applications

Compared to Si devices, special attention is required to utilize the SiC MOSFET in MV converters effectively and reliably, as those devices are much faster, smaller, and can block higher voltage.

The main critical challenge from an application point of view is the extremely fast switching nature of the SiC MOSFET device (mainly voltage slew rate $dv/dt$ and current slew rate $di/dt$). For SiC MOSFETs, $dv/dt$ can reach 250 V/ns [30] and $di/dt$ of 6 A/ns [5], which are tenfold faster when compared to Si IGBTs. Such high slew rates can cause an abundance of problems - especially on the gate-driver (GD), sensors and control, and electromagnetic interference (EMI) on the converter level, as shown on the simplified diagram in Fig. 1.1.

As the interface between the control and power stage, the GD is a key component. The main
components of every GD are isolated power supply, signal isolation, and driving mechanism, as well as gate resistance, and fault protection. These should be carefully designed to obtain maximum performance, especially since the high slew rates have a direct impact. For power, voltage isolation is necessary between the input and output. The coupling capacitance between them can be the cause of significant common-mode (CM) current ($i_{cm,pwr}$) under high $dv/dt$. Therefore, special attention must be devoted to the design of this power supply to lower this capacitance. Equally important, the control signal isolation needs isolation. This capacitance should be as low as possible to minimize CM current through the signal path ($i_{cm,sig}$). For MV applications, the best choice is fiber optic due to its high insulation voltage and $dv/dt$ immunity [2]. Survivability of silicon-carbide (SiC) MOSFET modules during shortcircuit (SC) is essential for modern power electronics systems. SiC MOSFET modules exhibit much narrower SC withstand times and generally much lower SC robustness than silicon (Si) IGBTs. The withstand capability difference is expected because the SiC MOSFETs have a limited dissipation capability, accumulating thermal stress faster, owing to their smaller chip areas and much higher SC currents. Noise immunity under high slew rates can also make SC detection problematic. This puts a critical concern on their utilization, further stressing the importance of reliable protection [31]. In the phase-leg configuration, cross-talk interference becomes more serious with increased $dv/dt$ rates of SiC. With complementary device switching transients, current $i_{Crss}$ injected into the device gate through the Miller capacitance $C_{rss}$, causes possible rise or fall of $v_{gs}$ due to presence of $R_g$. If positive spurious voltage is higher than threshold voltage, a shoot-through event is created. This event can significantly increase the device losses leading to destruction, or it can prevent the successful operation of the converter due to SC detection. If negative induced spurious voltage is lower than a minimum allowable negative gate voltage of the semiconductor device, this can lead to gate oxide over-stress and accelerated device degradation, compromising system reliability. Therefore, with an increase of $dv/dt$ for SiC MOSFETs, this implies that Miller-clamping
circuitry is essential on the GD for successful operation. Additionally, during switching transients, the GD IC or current booster stage should sink or source several (several tens of) amperes peak gate current ($i_{gd}$) to achieve fast switching. In [5] it is shown that compared to Si IGBTs, the switching speed and losses of SiC MOSFET modules vary greatly with gate resistances, especially for a turn-on event. Therefore, driving resistance should be selected based on the trade-off between the losses and $dv/dt$ susceptibility of the gate-driver or the system.

Also, the influence of the CM current caused by fast switching can reflect to control through either the GD ($i_{cm,gd}$) or through the sensing architecture ($i_{cm,sense}$) which is vital for feedback control. For example, a current sensor output could be severely distorted under high $dv/dt$ and high-frequency for SiC MOSFET converters. The capacitive coupling due to high $dv/dt$, and magnetic coupling due to high $di/dt$ from the switching node and loop, have adverse impacts on control effectiveness and can deteriorate current quality. Different methods can be considered to mitigate these effects such as location of sensor, different shielding techniques, etc., [32].

Because of the high $dv/dt$ and $di/dt$ and generally large parasitic capacitances due to the compact sizes (e.g., $C_{hs}$), both converters utilizing HV SiC devices and loads can suffer severe conducted and radiated EMI. Since both $dv/dt$ and high-frequency are generally much higher in SiC applications, an EMI filter is the key component to ensure converters satisfy the EMI requirements and regulations. For example, in motor drives, these filters are required to protect the motor from the voltage doubling effect on its terminals and larger shaft voltage and bearing current, which impact the motor’s reliability. In grid applications, EMI filters are needed to reduce conducted EMI and guarantee that the power conversion system meets the requirement for grid-connected converters [2, 33, 34]. However, this research is not the main focus of this dissertation.
Achieving high reliability of MV-systems is critical due to large economic implications or overall system cost. For SiC MOSFET-based converters, increased susceptibility to thermal cycling with high working temperatures ($\geq 125 \, ^\circ C$), combined with reduced converter sizes aiming for high density, can lead to accelerated degradation, thus reducing the reliability of the system. Therefore, knowledge of junction temperature and thermal management for SiC MOSFET converters becomes even more important than for Si IGBT applications.

Additionally, in high-power MV converters, the limited current rating of the single die of existing SiC MOSFETs dictates that many dies need to be paralleled (on the module-level), or power modules need to be paralleled (on the converter-level), to achieve desired power. The positive temperature coefficient of the SiC MOSFET’s $R_{ds,\text{on}}$ allows paralleled devices to achieve current sharing naturally during static state. However, during fast switching transients, one must ensure good dynamic current sharing. To ensure good thermal performance and avoid hot spots, significant current imbalance between devices must be avoided. Dynamic current balance is highly sensitive to mismatch in parasitic inductances in both the gate-loop and power-loop. Therefore, to ensure good dynamic current sharing, a symmetrical layout of both loops is critical.

In addition, packaging related challenges such as high electric fields and electrical insulation, minimization of module related parasitic inductances and capacitances, high temperature operation, and multi-die paralleling are of utmost importance in MV converters. However, these challenges are not the main focus of this dissertation.
1.2.2 Motivations

Junction Temperature Estimation

Power electronic devices are one of the most reliability-critical components in the power electronics system [35, 36], as shown in Fig. 1.2 (a). This is especially true in harsh environment power electronics systems, such as renewable energy generation and automotive and rail-traction applications, where the combination of environmental and load-derived thermal cycling results in large junction temperature ($T_j$) fluctuations. Repetitive thermal cycling, coupled with large differences between coefficients of thermal expansion (shown in Fig. 1.2 (b)), cause severe thermo-mechanical stresses between the different layers and materials of the power module and accelerate wear-out, which ultimately results in a failure [37]. Furthermore, power devices are highly susceptible to certain vibration loading directions (or angles) and frequencies, which can intensify the stresses on the power module, as shown in Fig. 1.2 (c), [38]. With the increase of input frequency and amplitude of random vibration input power spectral density, the solder joints become susceptible to failure since maximum peeling pressure increases dramatically. As can be seen, lower angles of loading direction and peeling stress increases can lead to accelerated degradation as well.
Typical module failure and degradation mechanisms are summarized in Fig. 1.3, [39, 40, 41, 42, 43, 44]. The aforementioned literature emphasizes dominant degradation mechanisms as wire-bond and solder fatigue, due to direct exposure and susceptibility to high temperature, load cycling, and high mechanical stresses. Deterioration of these, results in electrical and thermal parameter change, followed by the $T_j$ rise inside the module (self-heating). As a consequence, the aging process of the module will be accelerated. Hence, real-time (online) measurement or estimation of the $T_j$ can help improve long-term reliability of the converter. Real-time junction temperature information can enable active thermal control, monitoring, and prognostics, which are vital to indicate state-of-health of the devices, remaining useful life, maintenance scheduling, etc. For SiC converters, knowledge of junction temperature becomes even more important because of increased susceptibility to thermal cycling due to reduced converter sizes.

$T_j$ Estimation Methods

Two approaches exist for junction temperature estimation: modeling and measurements,
which can be either direct or indirect. Modeling consists of the development of an appropriate electro-thermal model \([45]\), implementable in real-time. In most cases, it is executed in a way that heatsink temperature is directly measured. Then, based on that, the \(T_j\) is calculated with the aid of the estimated losses of the device and a lumped thermal model. Cauer or Foster networks are typical thermal models, developed by exploiting the analogies between the thermal and electrical model, where a thermal resistance identifies a barrier to the propagation of heat in a material, while a thermal capacitance identifies the amount of heat stored by a physical object. However, both loss and thermal models are generally defined under known constant conditions and are a rough estimation. Any variation will result in significant inaccuracy, thus invalidating them throughout the entire life cycle \([46]\). Moreover, models are unable to incorporate the aging effect. Direct temperature measurement is possible via optical or physical contact methods \([47]\). Optical methods are based on the acquisition of the thermal image of the dies, either through a long established fiber optical sensor, thermal camera, or some novel method \([48]\). Physical methods utilize integrated thermo-sensitive sensors in direct contact with the chip. Even though they are potentially accurate and able to provide a thermal map and detect hotspots, both methods require access to the dies which implies removal of the dielectric gel or alterations to the module package. This ultimately leads to reduced reliability, which renders them inadequate for industrial applications. The cost and intrusiveness make these methods suitable only for laboratory testing conditions.

Indirect measurement consists of sensing the temperature sensitive electrical parameters (TSEP). This provides an accurate, practical, non-intrusive solution, and is easily implementable on the gate-driver. The major disadvantage is that only an average chip temperature can be determined (hotspots cannot be detected) and involves a complex calibration procedure in the case of some TSEPs. A significant number of TSEPs have the potential
to estimate junction temperature: on-state resistance $R_{ds, on}$ [49], gate-to-source threshold voltage $V_{gs, th}$ [50], turn-off and turn-on delay times ($t_{d, off}$ and $t_{d, on}$) [51, 52], rate of change of drain-to-source voltage $dV_{ds}/dt$ [53], rate-of-change of current during turn-on $dI_d/dt$ [54], internal gate resistance $R_{g, int}$ [55, 56], voltage across parasitic inductance between kelvin and power source ($V_{Lss}$) [57], gate current temperature dependence $I_g$ [58], etc.

Sensing TSEP is most suitable due to its accuracy, non-intrusiveness, practicality, and ability to detect degradation. However, not all TSEPs can be considered appropriate for online $T_j$ estimation. Extracting $T_j$ from TSEPs can be challenging due to the low sensitivity of certain TSEPs and their dependence on the loading conditions of power converters. Furthermore, the switching, noisy, harsh working environment of SiC converters can possibly add many inaccuracies to the measurement. For the SiC MOSFET, $R_{ds, on}$, and $V_{gs, th}$ have the highest sensitivity to temperature variation, repeatability, and linearity over a wide operating range [59]. The temperature dependence of $R_{ds, on}$ is current-dependent, requiring not just $V_{ds, on}$ but also current measurement in order to decouple the load dependence from thermal effects. Additionally, dominant degradation mechanisms lead to changes in internal resistance and terminal voltage drop during conduction, making $V_{ds, on}$ a valid indicator of device state-of-health. The potential benefit of $V_{gs, th}$ is load current independence; however, it cannot be used for monitoring an indicator of wire-bond and solder fatigue. It can potentially be used to detect defects in the oxide layer of the SiC MOSFETs [60].

**State-of-the-Art $T_j$ Estimations**

Most of the recent efforts in $T_j$ estimation are generally implemented on the converter level [49, 61, 62, 63] often monitoring status of only single switch, or as a measurement board in addition to the gate-driver (GD) [55, 57, 59, 64, 65], requiring additional power supplies and signal isolation to transmit the information back to the system controller. If the $T_j$ were to be enabled on the module GD level, this would enable the flexibility to utilize this
sensor for all switches in the power module and converter, for any converter type. State-of-the-art $T_j$ estimation at the GD level is proposed in several research papers. Wang [56] proposed internal gate resistance $R_{g,int}$ junction temperature monitoring where differences in junction temperature in the gate loop are reflected to the gate loop first current peak value. Niu [58] also utilizes gate current temperature dependence to detect the temperature variation of the junction. However, each method exhibits high sensing tolerance of $\pm 10^\circ C$, severely impacting the accuracy of the proposed method. Denk [66] proposed $T_j$ measurement with superimposing the negative gate voltage with the high-frequency identification signal and the measurement of the voltage drop across the external gate resistor. However, this method cannot be used for high frequency SiC MOSFET applications due to relatively slow measurement time. Zhang [67] embeds the turn-off time method to monitor the $T_j$ on the GD level. Nevertheless, this method requires exact current knowledge at transitions, and fundamentally is not a fully online real-time $T_j$ measurement method since it would severely impact the converter efficiency. A turn-on delay-based $T_j$ measurement for the SiC MOSFET is proposed by Yang [68, 69]. Even though it shows great promise regarding accuracy and linearity, it is not fully real-time, and $T_j$ has to be requested every several switching cycles. The reason for this is that the proposed method has an unfavourable impact on turn-on switching loss and can possibly limit converter frequency if called every switching cycle, since the turn-on delay transition times increased in order to increase the method’s accuracy. Furthermore, it is not applicable in synchronous and soft-switching applications. Schubert in [70] expands an already utilized inverter output voltage measurement circuit for flux-linkage estimation of an electric drive to now incorporate semiconductor temperature and condition monitoring. However, the proposed circuit is not fully integrated on the gate-driver, requiring an additional current sensor in combination with the main controller. Additionally, it is not able to recognize the distinction of a thermal increase of $R_{ds,on}$ and wire-bond liftoff using this sensing approach unless implemented on more switches (ideally an inverter). Nevertheless,
none of the implemented methods on the GD utilize $R_{\text{ds,on}}$ and $V_{\text{gs,th}}$ which have the best properties for the SiC MOSFET.

Addressing the above shortcomings and driven by the desire to know that the $T_j$ can provide the state-of-health status for SiC MOSFETs, Chapter II proposes a GD integrated $T_j$ estimation method, based on monitoring the output characteristics ($R_{\text{ds,on}}$) of the device. This is accomplished with bringing intelligence to the GD by providing the insight on real-time behavior of the device current ($I_d$) and $V_{\text{ds,on}}$ in every switching cycle during continuous operation.

**Gate-Driver for Medium-Voltage all-SiC MOSFET**

If the kernel part of the medium-voltage converter is the SiC MOSFET, the design will be capable of achieving high efficiency and high power density. For designs utilizing up to 1.7 kV SiC devices, gate-driver designs for them have been reported extensively in literature. Therefore, to further explore benefits and tackle challenges of the SiC MOSFET implementation, devices beyond 1.7 kV will be utilized.

Extensive research has been done on medium voltage ($\geq 3.3$ kV devices) all-SiC MOSFET devices in the recent years, and companies are slowly but surely perfecting their designs. Although none of them is of yet commercialized, the portfolio is increasing rapidly, as shown on Fig. 1.4. The current leader in these ranges is Cree|Wolfspeed with devices in range 3.3 kV–10 kV. The XHV-7 package can be utilized for both 3.3 kV [71, 72] and 6.5 kV [7, 73] while the XHV-6 [74, 75] and XHV-9 [76, 77] packages are utilized for 10 kV devices, exploiting new generation die presented in [78]. From Mitsubishi, the LV100 module is capable of blocking up to 3.3 kV [79, 80] and HV100 for voltage ranges from 3.3 kV–6.5 kV [81, 82] exist. Hitachi and Fuji have developed devices for only 3.3 kV in their nHPD2 [83, 84] and
CHAPTER 1. INTRODUCTION

Figure 1.4: Non-commercialized portfolio of medium voltage devices $\geq 3.3\, \text{kV}$ from industry research initiatives.

HPnC [85] packages, respectively. General Electric (GE) and Semicron Electric also have a 3.3 kV SiC MOSFET module [86, 87]. Furthermore, there is significant research conducted in academia to improve existing packaging techniques reducing parasitics influence, mitigating strong electric fields, and reducing EMI [30, 88, 89]. Due to its availability, and to fully explore the benefits of SiC MOSFET devices for MV high-power applications switching on high frequencies ($\geq 5\, \text{kHz}$), the latest 10 kV, 240 A (maximum current available) Gen-3 SiC MOSFET XHV-6 from CREE/Wolfspeed is selected. The module comprises 3 submodules in parallel, a total of 18 dies per switch position. Alternatively, it will be possible to use a 3 XHV-9, 6 die per switch position module. This module has the highest reported switching speeds and voltage slew rates of $\frac{dv}{dt} = 100\, \text{V/ns}$ [90], which could be extremely beneficial for novel types of high-frequency medium-voltage control methodologies.

Since the XHV-6 is not commercialized, a GD will have to be designed. For the selected device and final converter and control application, a high-performance GD is a key component which is required to maximize the utilization of the beneficial SiC MOSFET characteris-
tics. Based on the challenges described previously, the focus of the design will consist of the following:

- Power and signal architecture as the crucial step in achieving high CM transient immunity. During transitions in the power stage, high $dv/dt$ is the excitation of the CM noise current on the top-side GD channel. This CM current is the result of the existence of parasitic capacitance of the isolation barriers. It induces voltage spikes along different GD impedances, and as a result can cause a malfunction.
- Power supply isolation and minimization of the coupling capacitance between primary and secondary side of transformer in order to significantly reduce the CM currents under high $dv/dt$. This work is not the main focus of the dissertation; however, main design points and highlights will be referenced.
- High-current driving system with minimized loop-inductance. Due to the large number of dies in the selected module, high sink and source driving are required to achieve fast switching. Symmetrical design has to be achieved to ensure that the 3 submodules are driven synchronously, possibly achieving satisfactory current sharing between paralleled modules. Furthermore, minimized loop inductance should be pursued to reduce any unwanted oscillations in the gate loop causing possible delays, malfunction on GD level, or increased losses of device [91].
- Cross-talk suppression circuit, also called Miller-clamping, since interference becomes more serious with increased $dv/dt$ rates of SiC. Miller-clamping circuitry is essential on the GD for a successful operation.
- Fast short-circuit protection since SiC MOSFET modules exhibit more narrow SC withstand times and much lower SC robustness compared to Si IGBTs. In previous research, [31, 92], a high-bandwidth, Rogowski switch-current sensor is developed and integrated on the GD to serve as a short-circuit detection mechanism and ultimately for protection of the device. As stated in [15], the SCC requires accurate analog informa-
tion of the switch current to turn off the corresponding switches. Therefore, the same sensor will be utilized as well. It will serve as the peak-current-mode control and as a phase-current sensor, by sampling the switch current by an analog-to-digital converter (ADC) and ultimately sending it to the controller through the some communication protocol.

**Power-Cell Design and Assessment**

Many converter topologies are used in MV applications depending on the voltage range (4.16-, 6.9- and 13.8-kV). Among multilevel converters, the modular multilevel converter (MMC) is one of the state-of-the-art topologies [8]. Originally developed for high voltage dc transmission [93, 94, 95], the MMC is increasingly considered for other HV and MV applications, e.g., motor drives [96], automotive [97], and other grid applications [98, 99, 100]. This is due to its salient features such as high modularity, capability to operate at any given voltage level without any restriction - voltage scalability, transformerless operation, high power quality (low filter requirements), and resiliency.

The power-cell (sub-module) is the vital constitutive piece of a typical MMC converter. Another term that is often used is the power electronics building block (PEBB). A PEBB is a least replaceable unit (LRU) to construct modular converters [101]. A PEBB was defined as a universal power processor, exhibiting complete modularity, scalability both voltage- and current-wise (possibility to be connected both in series, parallel or multi-phase), with capabilities to reduce cost of inventory and maintenance, and for low losses, weight, and size as well. [102, 103]. The PEBB is a broad concept that incorporates individually or collectively progressive integration of power devices, gate drives, and other components to functional blocks for multiple applications [104].
With respect to the main power switches used in power cells, the successfully proven SiC MOSFET devices are gradually overtaking silicon (Si) IGBTs. Recent advances have been made in the design of power cells with 1.2 kV \([34, 105, 106]\), 1.7 kV \([107, 108, 109, 110, 111, 112, 113]\) and 10 kV SiC MOSFETs \([114, 115, 116, 117, 118]\). Although expected to achieve strikingly elevated power density and efficiency, the power cell design based on medium-voltage SiC MOSFETs is facing unprecedentedly intertwined challenges. High-voltage insulation \([119, 120, 121]\), high \(dV/dt\) and electromagnetic interference (EMI) \([117, 122]\), component and system protections \([116, 123]\), as well as thermal management \([124]\), are simultaneously imposed to the power cell design; failure to handle these issues can result in catastrophic destruction. To this end, a detailed systematic power-cell design and assessment methodology (DAM) to tackle those challenges and ensure system safety, as well as to fully explore its capabilities prior to converter-level implementation of the power cell, is of upmost importance. However, this topic has only been partially studied \([116]\) and never summarized completely. Given that, a major objective is to develop a systematic hierarchical PEBB DAM framework from the component-level to the PEBB level utilizing a 10 kV SiC MOSFET.

**Medium-Voltage Converter**

Conventional control of the MMC exhibits large cell capacitor voltage ripple especially at low-line-frequencies, which is mainly caused by the capacitive energy oscillation. Most conventional control only utilizes the dc circulating current ensuring the active power balance. As a result, the capacitor voltage ripple is inversely proportional to the fundamental frequency, which leads to large energy variation at low frequency. To improve performance, voltage ripple can be reduced by utilizing some of the control freedoms offered, such as the circulating current or the common-mode voltage \([125]\). Second order harmonic injection reduces capacitive energy fluctuation to the third order; however, it is still dominated by
the fundamental frequency, and the attenuation is not as significant. Using the circulating current and common-mode voltage in combination, high-frequency harmonic injection presented itself as an alternative approach pushing the arm power towards a higher frequency, eliminating the voltage ripple line-frequency dependence. However, the loss and insulation concern brought by the high-magnitude arm current and common-mode voltage, respectively, hinders the penetration of the proposed control in the industry.

Recently, a novel control of the MMC converter has been proposed by Wang; it is called switching cycle control (SCC) [126]. In this control method, previously unused switching states of the MMC converter, so called shoot-through states, are leveraged. This allows the fast change of phase-leg circulating current, enabling control of the power cell’s capacitor voltage ripple within one switching cycle, preventing its deviation. Additionally, this enables the dc-dc operation of the MMC. Given that innovation, significant reduction in the capacitor and inductor energy storage can be achieved, resulting in a shocking 23 times higher power density, and enabling the MMC to operate in dc/dc condition as well. Furthermore, due to the zero-voltage switching, the turn-on loss is nearly eliminated, reducing the total losses as compared to the classic control methodologies [15].

Eiloza, Canales, and Burgos proposed a topology called the integrated capacitor blocked transistor (ICBT) [127], which provides an alternative solution of transferring high power in MV applications, inverting their operating mode compared to MMC. This allows for the direct power flow between the input and output terminals of the converter without having to transiently store energy in them (unlike in MMCs where the power is transferred indirectly through the cell capacitors). Basically, one ICBT cell operates as a single device, while series-connected ICBT cells operate as series-connected devices; therefore, high cell capacitances are not required in ICBT cells. The size of the capacitors can be much smaller, while arm inductors are completely eliminated. In addition, each switching device always blocks the
corresponding cell capacitor voltage when not conducting. When connecting multiple ICBT cells in series, there is no balancing issue among devices as long as the capacitor voltages are regulated. The converter generates minimum additional losses and does not require fast balancing control. Furthermore, these converters exhibit the same modularity and scalability as the MMC but do not require high cell capacitances [128].

The potential of these control methodologies is enormous. First, these converters fully exploit the advantage of the fast commutation speed and high switching frequency offered by SiC, increasing power density and efficiency in MV applications. Higher voltage rating and the higher operating temperature of these devices reduce the number of power-cells and the cooling system requirements. Second, the converters can operate in both ac and dc power conversion modes. This is a highly sought attribute for modular converters, greatly desired in the future MV dc microgrids and HVDC grids, and applicable as well on shipboard MVDC distribution systems. Low frequency operation down to zero hertz also becomes an inherent attribute of these converters, which is desirable for MV motor drive applications. Third, the proposed control methodologies feature unrestricted voltage and current scaling capability. Fourth, the building block nature of the proposed converters favors the development of new circuit topologies, creating a new family of SiC-based modular power converters. Fifth, and lastly, all of these features can be attained using existent half-bridge 10 kV SiC MOSFET modules, eliminating the need to develop new semiconductor modules.

To summarize, these novel types of control enable extreme reduction in passive component size, increase the efficiency of the converter, and can operate in dc/dc, dc/ac, ac/dc mode, potentially opening the modular converter to applications in which it was not previously used. In order to explore the aforementioned benefits, a modular, scalable, high-power density, high-efficiency medium-voltage converter optimized for 10 kV SiC MOSFET devices will be developed, being able to operate in both ICBT and SCC control mode.
1.3 Dissertation Outline

In Chapter 1, the research background, challenges, and motivations are introduced. First, the impact of the SiC MOSFET on MV applications is discussed and benefits such as high-temperature operation, fast-switching, high-efficiency, and high power density are outlined. Following that, the challenges of $dv/dt$ impact on the GD circuit and system, increased susceptibility on thermal cycling, paralleling modules, etc., are discussed. The last part of this chapter discusses the research motivations in detail, emphasizing the need for online estimation of the $T_j$, detailed design and assessment procedure for power cells, and enhanced gate-driver technology for the 10 kV device that will overcome all challenges imposed by the device and control.

In Chapter 2, a systematic approach for $T_j$ estimation utilizing an enhanced gate-driver (eGD) is provided. The primary focus is on a comprehensive design procedure, practical implementation, accuracy aspects, and limitations of the proposed circuitry; all have been fully integrated on the GD. The preliminary degradation results and the impact of different wire-bond loss on the output characteristics of the device within a half-bridge (HB) module having a Kelvin-source connection are investigated. Conclusions of this investigation will drive the selected $V_{ds, on}$ monitoring circuit, implying that the voltage should be measured from the drain to the power-source of the device. A state-of-the-art literature survey and chosen sensor techniques (embedded two-diode on-state voltage measurement $V_{ds, on}$ and Rogowski switch-current sensor) and their verification are presented first, as well as a gate-driver prototype for the 62 mm commercial SiC MOSFET. Following that, a device calibration procedure for obtaining the look-up table necessary for online estimation is presented, together with its comparison with curve-tracer results, to establish accuracy. To demonstrate the operation and validate the approach, the $T_j$ sensor is utilized in both pulsed testing and continuous
operation. Additionally, a degradation monitoring and aging compensation scheme is proposed, in order to validate the $T_j$ estimation through the lifetime. Lastly, since developed measurements are capable of capturing output characteristics with high accuracy, a junction temperature measurement generalization is proposed, possibly avoiding every component’s individual characterization in the converter.

In Chapter 3, the selected XHV-6 device static characterization is presented to finalize the requirements for the development of the gate driver. Following, the enhanced GD design and prototype are introduced where the emphasis is put on the power and signal architecture, high-current driving system with minimized loop-inductance, cross-talk suppression circuit, and design of the Rogowski switch-current sensor. At the end of the chapter, the dynamic characterization of the switch is performed further, looking into the properties of the device, implications on converter (power-cell) operation, and dynamic current sharing.

In Chapter 4, a systematic design and assessment methodology (DAM) with an overall framework and detailed considerations and solutions from the component-level to the power-cell level is provided, based on desired power-cell specifications. The developed DAM addresses simultaneously the challenges of high-voltage insulation, high $dv/dt$ and electromagnetic interference (EMI), component and system protections, as well as thermal management. Firstly, power-cell component design and modeling are investigated regarding the power-switch, gate-driver, busbar, controller and auxiliary circuits, and cooling system. Secondly, piece-wise verification of components previously designed are performed, ensuring their successful operation in the fully assembled power-cell. The test performed includes insulation tests, static and dynamic characterization, protection and reliability testing, thermal, etc. Additionally, based on thermal design and dynamic tests, full characterization of the MV power-cell capabilities prior to converter-level implementation are performed, which is reflected in the defined safe-operating area. Thirdly, system level verification is performed at
the complete power-cell regarding operation at dc-dc/dc-ac. Thermal characterization, EMI characterization, and efficiency characterization are performed.

In Chapter 5, a 10 kV SiC MOSFET-based modular, scalable, high-power density, high-efficiency medium-voltage converter is presented, operating in SCC and ICBT control mode, along with design and experimental results. Firstly, converter integration based on a 10 kV SiC MOSFET-based Power-cell will be presented. Power-cell assembly and qualification study, control methodology, dc-bus assembly, and communication strategy will be discussed in detail. Secondly, a converter prototype having a 2-cell per arm configuration and its experimental validations will be discussed. A detailed description on the prototype, overall system, measurements, additional converter-level insulation testing, and ICBT/SCC experimental results will be shown. Thirdly, and lastly, converter comparisons in voltage ripple (imbalance), efficiency, total harmonic distortion, and output voltage $dv/dt$ are performed.

In Chapter 6, the conclusions and future research topics as a continuation of presented research in this dissertation are given.
Chapter 2

Enhanced Gate-Driven for Junction Temperature Estimation of 1.2 kV SiC MOSFET Half-Bridge Modules

2.1 Introduction

For SiC converters, knowledge of junction temperature becomes even more important than for IGBT applications, due to increased susceptibility to thermal cycling with high working temperatures combined with their reduced converter sizes aiming for high density.

Real-time $T_J$ information can enable two major aspects: 1) active thermal control, 2) condition monitoring and prognostics, which are vital to indicate state-of-health of the devices - remaining useful life, maintenance scheduling, etc. Table 2.1 includes possible $T_J$ applications from literature. The most important aspects of active thermal control are 1) possible load sharing with redundant or parallel systems, where it is shown that controlling power among converters can stabilize the thermal fluctuation of the power devices and ultimately improve the reliability of the power conversion system, and 2) power loss manipulations where limiting the thermal cycling, control techniques mostly utilize variable switching frequency control, control the gate driving voltages, device slew rates, etc. The most important aspects of condition monitoring are 1) device and converter state-of-health where online detecting of small changes in the failure indicators of the device and converter lead to an increase in thermal impedance, thus temperatures can be utilized for diagnostics and prognostics of the
Table 2.1: Real-Time $T_j$ Estimation Applications

<table>
<thead>
<tr>
<th>Condition Monitoring</th>
<th>Active Thermal Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>Monitoring</td>
<td></td>
</tr>
<tr>
<td>Active thermal control [129]</td>
<td>Sensor calibration</td>
</tr>
<tr>
<td>Device state-of-health [64]</td>
<td>Current sensor</td>
</tr>
<tr>
<td>Converter state-of-health [130]</td>
<td>Voltage sensor</td>
</tr>
<tr>
<td>Safe operation areas [129]</td>
<td>Any temperature dependent sensor</td>
</tr>
<tr>
<td></td>
<td>Converter control and power flow</td>
</tr>
<tr>
<td></td>
<td>Device stresses in converter</td>
</tr>
<tr>
<td>Prognostics</td>
<td></td>
</tr>
<tr>
<td>Lifetime predictions [131, 132, 133]</td>
<td>Load share (redundant or parallel systems) [134, 135]</td>
</tr>
<tr>
<td>Maintenance scheduling</td>
<td>Power loss manipulation (switch and conduction) [129, 136, 137]</td>
</tr>
<tr>
<td>Diagnostics (fault root cause analysis)</td>
<td></td>
</tr>
<tr>
<td>Early failure</td>
<td>Active gate driving</td>
</tr>
<tr>
<td></td>
<td>$dv/dt$ and $di/dt$ control [136]</td>
</tr>
<tr>
<td>Random failure</td>
<td>Output $V=f(I)$ characteristic alteration [137]</td>
</tr>
<tr>
<td>End-of-life failure</td>
<td>Protection [138]</td>
</tr>
</tbody>
</table>

power modules, and 2) lifetime predictions which are based on the extracted thermal cycles from a mission profile to suggest and calculate the correct lifetimes for power modules.

2.2 Influence of wire-bond degradation of $V_{ds,on}$

The GD is referenced to the kelvin-source (KS), and the $V_{ds,on}$ measurement will be integrated on the GD. Due to concerns presented in [61, 139, 140], the influence of wire-bond degradation on the output voltage that is potentially being measured between the drain and kelvin-source is investigated. The commercial CAS300M12BM2 SiC MOSFET module will be opened, and the wire-bonds of one of the switches (having 6 dies and diodes in parallel) will be cut to observe its effect on $R_{ds,on}$, thus on-state voltage. Since in most SiC MOSFET converter applications, synchronous driving is preferred over the diode conduction decreasing the power
conduction losses, the $R_{\text{ds,on}}$ measurement results and impact of wire-bond loss will be shown for both the 1st and 3rd quadrant, with driving voltage of $V_{\text{gs,on}} = 20$ V. Fig. 2.1 (a) shows the opened module with the indicated top and bottom switch. Fig. 2.1 (b) shows the zoom in section to observe the wire-bond connections, and Fig. 2.1 (c) shows a drawing of the SiC MOSFET die and SiC JBS diode.

To observe the different effects, two different results from wire-bond cutting will be illustrated, as reported in [141]. In case 1, all wire-bond cuts are the ones not located on the same source pad as the kelvin source connection; the wire-bond cuts are from source pads (b) and (c), as indicated in Fig. 2.2 (a). In case 2, all wire-bond cuts are the ones on the same source pad as the kelvin source connection; these are from the source pad (a), as indicated in Fig. 2.3 (a).

Portrayed in Fig. 2.2 (a) is case 1, where wire-bonds are cut in sequence as indicated. $R_{\text{ds,on}}$ measured with a curve tracer is the one from the drain-to-kelvin source $R_{\text{d–ks,on}}$ and from the drain-to-power source $R_{\text{d–ps,on}}$. Fig. 2.2 (b) shows that with cutting specified wire-bonds from both the drain-to-power source and drain-to-kelvin source, resistance during on-state is increasing. This gives the impression that only the voltage measurement circuit from the
kelvin-source to drain could potentially successfully monitor the switch degradation (both MOSFET and wire-bond degradation together).

Portrayed in Fig. 2.3 (a) is case 2, where wire-bonds are cut in sequence as indicated with $R_{d-ks, on}$ and $R_{d-ps, on}$ measured with a curve tracer. Fig. 2.3 (b) shows that with cutting specified wire-bonds, $R_{d-ks, on}$ during on state is now decreasing, while $R_{d-ps, on}$ is still increasing.

Figure 2.2: CAS300M12BM2 SiC MOSFET module wire-bond cut. (a) Sequence of cutting. (b) Experimental results showing increase in on-state resistances.

Figure 2.3: CAS300M12BM2 SiC MOSFET module wire-bond cut. (a) Sequence of cutting. (b) Experimental results showing decrease in on-state resistances from drain-to-kelvin source perspective.
The drop and rise in $R_{d-ks,\text{on}}$ when cutting wire bonds can be explained through the existence of the lateral resistance between the three source pads in the SiC MOSFET structure. Several reduced model simulations will be conducted to confirm this statement. Fig. 2.4 shows the reduced on-state dc model with two dies in parallel simulated in the LTSpice software. Since the utilized dies in the CAS300M12BM2 are 25 mΩ dies (CPM2-1200-0025B), one die will be represented with three $R_{\text{MOS}} = 75 \text{mΩ}$ resistances in parallel since it has three source pads. The single wire-bond resistance is modeled with the $R_{\text{WB}} = 5 \text{mΩ}$. ($R_{\text{WB1}}, R_{\text{WB6}}$ are on source pad (a), while $R_{\text{WB2-5}}, R_{\text{WB7-10}}$ are on source pads (b) and (c).) Additionally, $R_{\text{WB-KS}} = 5 \text{mΩ}$ is the resistance of the kelvin-source wire bond, and $R_{\text{LAT-SP}}$ is the lateral resistance between the source pads. Simulation is excited with a 100 A current source, and different voltages are observed: voltage between drain-to-kelvin source $V_{d-ks,\text{on}}$, voltage between drain-to-power source $V_{d-ps,\text{on}}$, and voltage between kelvin-to-power source $V_{ks-ps,\text{on}}$.

Table 2.2 summarizes the results of the simulation. When the $R_{\text{LAT-SP}} = 5 \text{mΩ}$, with the removal of resistors (represents wire-bond cut) $R_{\text{WB9}}, R_{\text{WB4}},$ and $R_{\text{WB5}}$ from the source pads (b) and (c), an increase in $V_{d-ks,\text{on}}, V_{d-ps,\text{on}},$ and $V_{ks-ps,\text{on}}$ can be observed. However, with removing $R_{\text{WB6}}$ and $R_{\text{WB1}}$ from the source pads (a), a drop in $V_{d-ks,\text{on}}$ is observed, while
Table 2.2: Simulation Results of Wire-Bond Cut Impact on Different Voltages

<table>
<thead>
<tr>
<th>Wire-cut</th>
<th>V(_{d-k_s}) [V]</th>
<th>V(_{d-ps}) [V]</th>
<th>V(_{k_s-ps}) [mV]</th>
</tr>
</thead>
<tbody>
<tr>
<td>-</td>
<td>1.242</td>
<td>1.308</td>
<td>65</td>
</tr>
<tr>
<td>R(_{WB9})</td>
<td>1.246 ↑</td>
<td>1.314 ↑</td>
<td>67 ↑</td>
</tr>
<tr>
<td>R(_{WB4})</td>
<td>1.250 ↑</td>
<td>1.320 ↑</td>
<td>69 ↑</td>
</tr>
<tr>
<td>R(_{WB6})</td>
<td>1.231 ↓</td>
<td>1.338 ↑</td>
<td>107 ↑</td>
</tr>
<tr>
<td>R(_{WB5})</td>
<td>1.246 ↑</td>
<td>1.362 ↑</td>
<td>116 ↑</td>
</tr>
<tr>
<td>R(_{WB1})</td>
<td>1.214 ↓</td>
<td>1.400 ↑</td>
<td>184 ↑</td>
</tr>
</tbody>
</table>

R\(_{LAT-SP}\) = 5 mΩ

R\(_{LAT-SP}\) = 0 mΩ

V\(_{d-ps, on}\) and V\(_{k_s-ps, on}\) are still increasing. When the R\(_{LAT-SP}\) = 0 mΩ, any wire bond cut in this case will not result in the increase or decrease of the V\(_{d-k_s, on}\), since the V\(_{d-ps, on}\) and V\(_{k_s-ps, on}\) are still increasing. With these simple simulations, experimental results (Fig. 2.2 and Fig. 2.3) are confirmed for the case when the R\(_{LAT-SP}\) ≠ 0 mΩ.

This is furthermore confirmed experimentally on a new device and shown on Fig. 2.5. The 6 wire-bond cuts were the ones on the same pad as the KS connection, and the remaining were from the other 2 pads of multiple dies. An increase or decrease of R\(_{d-k_s, on}\) is no longer observable, as the R\(_{d-k_s, on}\) as TSEP lost the capability to detect degradation. With these simple simulations and additional tests, experimental results (Fig. 2.2 and Fig. 2.3) are confirmed for the case when the R\(_{LAT-SP}\) ≠ 0 mΩ.

Experimental and simulation results imply that with different wire-bond loss in the module, R\(_{d-k_s, on}\) as a TSEP is not reliable, since it can both increase and decrease with the wire-bond loss when the lateral resistance between the different source pads is not negligible. However, from observed experiments, the R\(_{d-ps, on}\) has increasing trends with the loss of wire-bonds and can be used effectively. Ultimately, T\(_j\) monitoring and degradation for this module should not
be performed from drain-to-kelvin source terminals of the device, because the results might be masked with different wire-bond degradation effects. Therefore, to successfully monitor the temperature of the module with the aforementioned wire-bond technique, it is necessary to have both $V_{d-ks, on}$ and $V_{ks-ps, on}$ measurements. This is further confirmed through other research that has shown that different degradation mechanisms can have different impacts on the $R_{d-ks, on}$. Static bias-temperature instability (BTI) effects and high-electric fields (HEF) on the gate-source or drain-source have shown to cause shifts in the $V_{th}$ [142, 143, 144]. This can directly relate to changes in the $R_{d-ks, on}$, and in particular, the channel resistance and accumulation region resistance of the device [145]. The semiconductor focused stresses, like positive BTI (PBTI) or negative BTI (NBTI) on the gate, show positive or negative shifts in $V_{th}$ which would relate to a positive or negative shift in $R_{d-ks, on}$, respectively [142]. These semiconductor stressors do not impact the wire-bonds nor solder connections but can impact overall $R_{d-ps, on}$. Other reliability focused experiments like power cycling, a test most comparable to real converter operation, revealed the impact on the $R_{d-ps, on}$ as well. This was shown in terms of both a semiconductor and wire-bond resistance increase [146, 147], or in the case where the semiconductor resistance decreases while the wire-bond resistance

Figure 2.5: CAS300M12BM2 SiC MOSFET module wire-bond cut experimental results showing loss of sensing abilities from drain-to-kelvin source after removing 6 wire-bonds that are on the same pad as kelvin-source.
increases [148].

2.3 Gate-Drive Design Incorporating $T_j$ Estimation

Previously, an enhanced GD for half-bridge (HB) modules was developed for all-electric ship and electric vehicle applications by integrating PCB-embedded Rogowski coil switch-current sensors (RSCS) and fast digital-signal-processing enabled by a field-programmable gate array (FPGA) [31, 149, 150]. RSCSs collect two SiC MOSFET switch currents in a manner of high magnitude, high bandwidth and accuracy, and solid signal isolation. Switch-current signals are used for short-circuit detection under various fault impedances and various types of short-circuit, as well as for phase-current reconstruction on the gate driver itself. Due to the comprehensiveness of the aforementioned references, the design and implementation aspects of RSCS will not be discussed in detail.

Driven by an eagerness to learn of junction temperature and failure detection technologies for SiC MOSFETs to provide state-of-health status, an additional measurement will be integrated onto the existing GD design to potentially open the possibility for junction temperature measurement. To obtain $T_j$ estimation, the $V_{ds, on}$ measurement will be integrated on the GD and employed during continuous operation. Therefore, by knowing both $I_d$ and $V_{ds, on}$ on the GD level and knowing the temperature model obtained during the switch calibration procedure (prior-to converter operation), the online $T_j$ estimation will be possible via the output characteristics of the device. To clarify, this method is basically the same method as observing the $R_{ds, on}$, since generally $R_{ds, on}$ is extracted from output characteristics. The $T_j$ model (look-up table), will be stored in the FLASH memory on the GD, which the FPGA will help access, thus enabling real-time junction temperature monitoring for both devices in the SiC MOSFET HB module configuration on the GD level, originally proposed in [151].
2.3.1 On-state Drain-to-Source Voltage Sensor Circuit Design

The biggest challenge of implementing the online $V_{\text{ds, on}}$ sensor lies in its fundamental principle: blocking the high voltage swings over the switch during normal operation in the power stage, while enabling the measurement of low, several tens of millivolt, voltages over the device during on state. For WBG devices, in this case the SiC MOSFET, the accuracy and high bandwidth of the sensor is crucial and challenging as well, due to low $R_{\text{ds, on}}$ and high $f_s$. The utilized commercial 1.2 kV SiC MOSFET HB module (CAS300M12BM2), exhibits $R_{\text{ds, on}} = 4.2 \, \Omega$; for example, this means at $I_d = 100 \, A$, terminal voltage drop will only be $V_{\text{ds, on}} = 0.42 \, V$. Additionally, high resolution of the sensor and a sampling system are required for two reasons. First, even though the output characteristics temperature variation exhibits high sensitivity, it is still generally low. For example, the aforementioned SiC module exhibits sensitivity of only $2.6 \, mV/^\circ C$ at $100 \, A$. Second, according to [40], a 20% increase in output voltage from its initial values is considered a wear-out failure. In the case of the selected device, from healthy to wear-out failure at $25^\circ C$, the increase in output voltage would only be $84 \, mV$ at $100 \, A$.

$V_{\text{ds, on}}$ Measurement Circuits Literature Survey

A large number of circuits suitable for $V_{\text{ds, on}}$ measurement are proposed in literature. The principles of operation will not be described in detail, but important aspects will be emphasized.

Ji [64] proposed the limiting Zener diode method for $V_{\text{ds, on}}$ measurement. The circuit is straightforward with that simple operation principle. However, it exhibits a temperature dependent voltage offset and exhibits significant power dissipation. Furthermore, even though an additional diode is added in order to reduce the parasitic capacitance of the Zener diode,
the bandwidth will be very low due to huge resistance.

A resistor voltage divider circuit is proposed by Arribas [152] using a simple principle similar to the previous circuit, where a resistor is used instead of the Zener diode. A sensing current during on-state causes a temperature dependent offset and has to be designed to block high voltage, implying poor sensitivity of the circuit and a small signal-to-noise ratio (SNR), which will affect accuracy. Furthermore, a trace parasitic capacitance might present a serious problem due to the huge resistor values since it will create a strong low pass filter.

A desaturation sensing method principle, originally proposed in [153, 154] for Si IGBT protection, can also be used for $V_{ds,\text{on}}$ measurement. Current source that is only active during the on-state of the device enables drain-to-source voltage sensing of the switch by biasing the high-voltage diode. Potential problems are: 1) design of the controlled constant current source, 2) Influence of temperature on current source, and 3) Temperature dependence of offset voltage since it comprises of voltage over high-voltage diode and resistor. Furthermore, susceptibility to noise due to diode parasitic capacitance might present an issue.

A passive desaturation circuit operation is proposed by Badawi in [155]. Different from the desaturation circuit, the current source is not active (controlled) but rather passive circuitry with a capacitor behaving as a current source which is being charged during off-state. Even though it does not require any control, it exhibits a temperature dependent voltage offset. It is fairly complex since voltage balance in continuous operation has to be achieved. These types of circuits are generally very susceptible to noise due to diode parasitic capacitance which might be problematic in fast SiC applications.

A two-diode method is proposed by Beczkowski and Ghimire in [39, 156]. The difference compared to a desaturation circuit is that the voltage over the switch is measured across one of the high voltage diodes (HV diode). With the right choice of a resistor network, and
the assumption that both diodes have the same voltage drops, the measured voltage will be \( V_{ds,\text{on}} \) of the switch. The most important aspect of this design is that it does not exhibit voltage offset issues, and the controlled current source design does not have to be constant. However, diode tolerances in forward voltages and variation with temperature might result in errors, implying that diodes should be thermally coupled in order to avoid temperature mismatch, thus different voltage drops.

Arribas in [152] shows a low-voltage MOSFET decouple method utilization with a simple principle, similar to a resistor voltage divider. In this method, since the low voltage MOSFET (up to 100V) is blocking when the switch is off, higher values of resistance can be chosen to increase sensitivity multiple times. It exhibits very similar performance to the resistor voltage divider, and that SNR is a little bit better, but requires the control signal for the low-voltage MOSFET to be carefully chosen with a minimum output capacitance.

The depletion MOSFET method is proposed by Choi in [40]. Several important challenges are as follows: 1) power dissipation on the resistance, 2) a negative \( V_{gs} \) concern due to huge oscillations coming from the power stage, 3) depletion MOSFET with the 1.2 kV blocking voltage is rare, 4) the circuit exhibits small, but not negligible, offset and temperature dependency.

Koenig and Gelagaev in [157, 158] propose a high-voltage MOSFET decouple method. Important aspects are that the circuit exhibits very small, almost negligible, offset and influence of temperature. However, the detector MOSFET must be the same voltage rating as the power switch, and its integration might be problematic. Furthermore, the negative \( V_{gs} \) concern exists, due to huge oscillations coming from the power stage and non-idealities of the detector MOSFET, particularly \( C_{gd} \), as large current might be pulled out of the power supply.
Table 2.3: Comparison between Available Online $V_{\text{ds, on}}$ Measurement Circuits

<table>
<thead>
<tr>
<th>Design complexity</th>
<th>Zener limiting diode</th>
<th>Resistor voltage divider</th>
<th>Passive desturation</th>
<th>Desaturation</th>
<th>Two-diode</th>
<th>Low-voltage decouple</th>
<th>Depletion MOSFET</th>
<th>High-voltage decouple</th>
</tr>
</thead>
<tbody>
<tr>
<td>Component count</td>
<td>Simple</td>
<td>Simple</td>
<td>Complex</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>Medium</td>
<td>Small</td>
</tr>
<tr>
<td>Offset problem</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Temperature dependent offset</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Delay</td>
<td>&lt;3000 ns</td>
<td>&lt;500 ns</td>
<td>&lt;300 ns</td>
<td>&lt;300 ns</td>
<td>&lt;300 ns</td>
<td>&lt;500 ns</td>
<td>&lt;700 ns</td>
<td>&lt;300 ns</td>
</tr>
<tr>
<td>HV components and switches</td>
<td>Resistor</td>
<td>Resistor</td>
<td>HV Diodes</td>
<td>Diode</td>
<td>Diodes</td>
<td>Resistor</td>
<td>MOSFET and resistor</td>
<td>MOSFET</td>
</tr>
<tr>
<td>Noise influence</td>
<td>Minor</td>
<td>Minor</td>
<td>Major</td>
<td>Major</td>
<td>Major</td>
<td>Minor</td>
<td>Minor</td>
<td>Major</td>
</tr>
<tr>
<td>Significant losses</td>
<td>Yes</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
</tr>
<tr>
<td>Accuracy</td>
<td>Medium</td>
<td>Poor</td>
<td>Good</td>
<td>Good</td>
<td>Great</td>
<td>Poor</td>
<td>Good</td>
<td>Great</td>
</tr>
</tbody>
</table>

Table 2.3 is constructed based on results from presented literature review and observations, as well as simulation results performed.

The best possibilities for the $V_{\text{ds, on}}$ online measurement based on Table 2.3 are as follows: the two-diode method, the high voltage decoupling MOSFET, and either of the DeSat methods (passive or active). A necessary complicated on-line temperature dependent offset compensation, especially if a constant current source is not being used, renders desaturation methods unsuitable for accurate measurement. The high-voltage decoupling MOSFET method is very accurate, fast, and has negligible offset and temperature dependency. However, since integration on the gate driver is planned, this method cannot be considered, due to its very bulky high-voltage blocking switch which would not be practical and would significantly reduce the power density of the system. Therefore, the two-diode method presents the best option under the following assumption: both diodes will have the same forward voltage under the same current during on state (feature ensured by high input impedance OpAmp), and the temperature of both diodes is the same (diodes will be placed in close proximity).
Additionally, this circuit exhibits low losses, great accuracy, and sensitivity. One of the biggest concerns is the noise influence; this issue will be discussed during the design stage.

The final on-state voltage measurement circuit is designed, comprised of a two-diode circuit monitoring \( V_{d-ks,on} \), and an AD8429 instrumentation amplifier monitoring the voltage over wire-bonds directly (between kelvin source and power source) \( V_{ks-ps,on} \). This is depicted on Fig. 2.6. Apart from being able to aid in the temperature estimation task (monitoring \( V_{d-ks,on} \) and \( V_{ks-ps,on} \) together through a differential amplifier), the proposed circuit, if desired, can additionally monitor voltages \( V_{d-ks,on} \) and \( V_{ks-ps,on} \) separately. This enables the possibility to monitor and decouple different degradation mechanisms happening in regards to location - is it the device (chip) related degradation or the wire-bond related fatigue? How to possibly decouple the degradation location with the proposed GD is explained in more detail later in this chapter.

**Figure 2.6:** Complete on-state voltage measurement sensing circuit observing voltage from drain to power source.
Two-Diode Circuit

The two-diode $V_{d-ks, on}$ measurement circuit principle of operation is similar to a desaturation circuit, requiring current source during on-state of the device under test (DUT). Therefore, a simple gate-controlled current source is designed. Theoretically, the only thing required for this current source to operate is a gate signal and resistor $R_{cs}$. However, a voltage follower is implemented to decouple the current source from the DUT driving stage, preventing any potential mutual influence. Therefore, the gate-controlled current source is active when the device is on, enabling sensing with the $I_{cs}$ current. The developed current source is not a constant current source. As the current in the power stage increases, it will cause the voltage over the device to rise; thus, voltage on node 1 rises. However, this does not present any problem in the circuit operation. During on-state of the DUT, under the assumption that for the same $I_{cs}$ current, HV diodes will have the same forward voltage drop (diodes connected to a high impedance operational amplifier - OpAmp, at the same temperature), $V_{hv,d1} = V_{hv,d2} = V_{hv,d}$, and if $R_1 = R_2$, output voltage of the sensing system is $V_{out} = V_{d-ks, on}$. The resistor $R_3 = R_1 \parallel R_2$ is located in the positive node, and its purpose is to suppress the effect of the input bias current on the output voltage and does not play a part in the gain.

The output voltage of the OpAmp is filtered with the 28.3 MHz high frequency RC filter enabling the high bandwidth (BW) switch voltage measuring. To minimize the impact of the common-mode current noise injection through the HV diodes caused by the fast $dv_{ds}/dt$ of the DUT (assumption: $C_{hv,d1} = C_{hv,d2}$) based on

$$i_{2d, dvdt} = \frac{C_{hv,d1}}{2} \cdot \frac{dv_{ds}}{dt},$$

(2.1)
diodes are required to feature fast reverse-recovery and low junction capacitance $C_{hv,d}$. The selected HV diodes are SiC GB02SLT12-214 from GeneSiC (1.2 kV, 2 A). Its total capacitive
charge of only \( Q_c = 7 \text{nC} \) enables extremely low switching time, \( t_{sw} < 10 \text{ns} \), with almost no reverse-recovery. The diode’s low junction capacitance \( C_j < 10 \text{pF} \) minimizes the \( i_{2d,dvdt} \) which is further reduced by having two in series. However, to minimize the switching noise impact on the operation of the GD and sensing circuits even more, instead of each diode, two diodes are used, resulting in 4 diodes total in series.

Due to a possible parameter mismatch, even with the same batch of HV diodes, their voltage drops can be somewhat different, making the measurement partially incorrect, possibly resulting in a huge junction temperature estimation error. Since the only controllable variable is current through the diodes, tests are done in order to determine the best sensing current \( I_{cs} \) range, which will result in the lowest voltage discrepancy error between the two diodes. A simple test circuit was developed (Fig. 2.7 (a)) where current through the diodes was imposed and ranged between 1 mA-100 mA, on three different temperatures \( T_c[25, 75, 125] ^\circ C \) for three different samples of 2x2 diodes. Voltages were measured over the diodes \( V_{hv,d1} \) and \( V_{hv,d2} \), and their difference is calculated and plotted against the sensing current in Fig. 2.7 (b). The smallest discrepancy between \( V_{hv,d1} \) and \( V_{hv,d2} \) is when the sensing current is the lowest,
$I_{cs} \leq 5 \text{ mA}$, which implies less measurement error for $V_{d-ks, on}$. As the current rises, the discrepancy rises. This particular effect can be attributed to the output diode characteristics and the scattering between diodes from the same batch. With smaller currents, the smaller forward voltage diodes will have; thus, a smaller error can be expected. As the sensing currents rise, the diodes characteristic is closer to the knee so more discrepancy can be expected, which is observable from Fig. 2.7 (b). The same effect applies for higher temperatures as well, except that the voltage difference generally reduces as the temperature increases, since the diode knee voltage reduces with higher temperatures, making $V_{hv,d1}$ and $V_{hv,d2}$ smaller. Therefore, $R_{cs}$ from Fig. 2.6 is selected to be $R_{cs} = 2.5 \text{k}\Omega$, bounding sensing current to always be below $I_{cs} < 2 \text{ mA}$.

To make a two diode circuit operate for both positive and negative $V_{ds, on}$, the selected TI LM7372 OpAmp is supplied with bipolar voltage. The circuit will be operational as long as the gate-controlled current source voltage fulfils this inequality:

$$5 \text{ V} > V_{d-ks, on} + 2 \cdot V_{hv,d1} \quad (2.2)$$

The current source is disabled and bypassed during the off-state of the DUT with simple control circuitry for the signal MOSFET M1. Furthermore, this bypasses any $dv/dt$ related noise directly to the ground plane, preventing its possible influence on the measurement circuit and gate source voltage during transitions. During off-state of the DUT, HV diodes that are directly connected to the drain terminal will share and block the $V_{ds}$ voltage, since the Zener diode is connected in parallel with the other HV diodes, preventing them from blocking and protecting sensing circuitry.

For the instrumentation amplifier measuring $V_{ks-ps, on}$, according to the datasheet of instrumentation amplifier AD8429, if the $R_g >> 6 \text{k}\Omega$, gain will be 1; therefore, $R_G = 600 \text{k}\Omega$. 

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This voltage is then sent to a differential amplifier for summation. Signal MOSFETs M2 and M3 are turned on in order to transmit both $V_{d-ks, on}$ and $V_{ks-ps, on}$ to the differential amplifier; the purpose of M2 and M3 will be explained in Section VI. If all resistors are chosen to be the same ($R_5 = R_6 = R_7 = R_8 = 10 \text{k}\Omega$), the output of the differential OpAmp will be as follows: $V_{\text{diff.out}} = V_{d-ks, on} - V_{ks-ps, on} = V_{d-ps, on}$. With this, the complete voltage between drain-to-power source is being monitored. The proposed circuitry can be used for both bottom and top devices in the HB without any modifications.

The output of the differential amplifier $V_{d-ps, on}$ is processed through a low bandwidth filter with a cutoff frequency of 2.1 MHz to eliminate high frequency ringing during switching instances. $V_{ds,lbw}$ information is sent through a level shifter to a high precision 12 bit analog-to-digital converter (ADC) with a sample rate of 2.5 Msps communicating through a digital isolator (Diso) with the FPGA, which will perform temperature estimation tasks.

### 2.3.2 Gate-Driver Design and Prototype

**Gate-Driver Design**

The gate-driver design does not differ much from the one discussed in [159]. Presented here, is the final implemented sensing architecture, as a part of the implemented GD architecture shown in Fig. 2.8 (a), where the FPGA (Intel Max10-10M08SAE144) is the core of the developed gate driver.

The basic concept is that in every switching cycle, a digital 12-bit serial peripheral interface (SPI) communication from the ADCs (Analog Devices-LTC2315-12), sends values of $I_d$ from RSCS and $V_{d-ps, on}$ from the on-state voltage measurement system to the FPGA. Then, the FPGA forms a 24-bit address and through SPI will access the temperature model stored in a form of a look-up table (LUT) in the FLASH memory. The FLASH memory will return
the temperature information based on measured $I_d$ and $V_{d-ps, on}$. Afterwards, the FPGA can send that information directly to the main controller via an inter-integrated circuit ($I^2C$) communication protocol, or send it to the digital-to-analog converter (DAC - Texas Instruments DAC8811) to obtain analog information and then send it to the main controller. This information, will ultimately be used for $T_j$ control and degradation monitoring.

![Figure 2.8](image_url)

**Figure 2.8:** (a) Final simplified implemented sensing architecture. (b) Example principle of $T_j$ measurement with digital average filter.

Fig. 2.8 (b) shows an example of 30 kHz switching frequency with 50% duty cycle, for one device. The same procedure is applied for both devices in a half-bridge. Assumptions that during the $t = 1.6 \mu s$, $\Delta I_d$ will be negligible, and during $t = 3.4 \mu s$, $\Delta T_j$ is negligible (if there is no shoot-through), are valid in most of cases. Furthermore, after turn-on, the first couple of $\mu s$, either sampling or measurement should be avoided due to high frequency oscillations. This differs from setup-to-setup depending on the device used, parasitic inductance, current, voltage level, etc. To increase precision and reduce the impact of possible measurement noise, a simple average digital filter is implemented. The chosen point to start sampling is after $t = \frac{3}{4} T_{pwm}$ (at 50% of the on-state). The starting sampling point is chosen arbitrarily and can be selected any time after the switching oscillations pass. This starting point can be decided by either the main controller based on the sent duty cycle, or it can be decided...
by the FPGA based on the duty cycle reference communicated. It can also be constant for
dc-dc operation if the operation point can roughly be known. Four samples (value chosen
arbitrarily as well and can be both higher or lower, but it should be $2^x$, where $x$ is a positive
integer) are taken in the time duration of the $1.6 \mu$s, since the sampling frequency of the
ADC is set to be $f_{\text{samp}} = 2.5 \text{ Msps}$. The rest of the duty cycle is left to process the current,
voltage, communicate with FLASH, and return the temperature. After sampling the $I_d$ and
$V_{d_{\text{ps, on}}}$, an averaging of each is performed. That information is packaged in a form of a
24 bit address (12 bit current + 12 bit bit voltage). After packaging that information, the
FPGA accesses the FLASH memory (via SPI communication) with the previously formed
address; the task finished in $1.4 \mu$s. The FLASH memory returns the 8 bit information of
$T_j$, located on the accessed address (based on measured $I_d$ and $V_{ds_{\text{on}}}$). Upon receiving the
temperature information, the FPGA will access the 16 bit DAC via SPI communication (8 bit
temperature + 8 bit of ‘0’), which is finished in $0.4 \mu$s. After that, the analog version of the
$T_j$ based on the averaged current and voltage is known.

The final implemented architecture is shown on Fig. 2.9. Apart from the junction tem-
perature estimation for both switches in a half bridge, the FPGA is employed for digital
subtraction in order to reconstruct phase current, resetting, and turning off the RSCS when
the corresponding switch is not conducting. Furthermore, it programs, drives, and coordi-
nates the fault generation coming from the driver IC. The SC fault signal from the RSCS is
transferred through the Diso to the isolated side to trigger the soft turn-off option of the GD
IC. The chosen Diso is the six channel ISO7761 from Texas Instruments. It exhibits only
$C_{1/O} = 1 \text{ pF}$, greatly minimizing the impact of CM currents. The six channel Diso is neces-
sary since three channels are used for SPI communication with the ADC: two channels for
controlling M2 and M3, and one channel for the SC fault protection. To further strengthen
the signal path against the CM current, isolated power supplies with the minimum possible
parasitic capacitive are chosen (THB 6-1223 with $C_{I/O} = 7 \text{pF}$). The smaller the parasitic capacitance, the less CM current will be introduced, due to its larger impedance on higher frequencies. The main power traces that are providing power for GP2 and GP3 isolated grounds are laid out with the goal of bypassing CM noise current away from sensitive components (analog and digital circuitry for voltage processing, communication, and driving). The driver IC STGAP1AS is utilized for driving and protection. Since the STGAP1AS has a maximum driving/sinking current of 5.6 A, the external current booster stage is designed with max 30 A current, according to [160]. The current booster is able to work together with the STO functionality. Furthermore, Active Miller Clamping is employed as well, to absorb the Miller current and prevent partial shoot-through events.
Gate-Driver Prototype

An enhanced GD prototype with the indicated dimensions for the 62 mm commercial SiC MOSFET half-bridge module is shown in Fig. 2.10. The most important aspects of the enhanced GD are summarized in Table 2.4.

2.3.3 Gate-Driver Experimental Validations

Gate-driver Operation and RSCS Evaluation

The gate-driver operation will be verified at the same time as the functionality of the RSCS for both the high bandwidth (protection) loop and low bandwidth (control) loop, through
Table 2.4: Enhanced Gate-driver Specifications

<table>
<thead>
<tr>
<th>Property</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>9 V</td>
<td>18 V</td>
</tr>
<tr>
<td>Driving voltage</td>
<td>−8 V</td>
<td>22 V</td>
</tr>
<tr>
<td>Embedded switch current measurement</td>
<td>−800 A</td>
<td>800 A</td>
</tr>
<tr>
<td>Embedded phase current measurement</td>
<td>−800 A</td>
<td>800 A</td>
</tr>
<tr>
<td>Embedded switch on-state voltage measurement</td>
<td>−3 V</td>
<td>3 V</td>
</tr>
<tr>
<td>Embedded junction temperature estimation</td>
<td>−40 °C</td>
<td>150 °C</td>
</tr>
<tr>
<td>Driving current</td>
<td>±5.6 A</td>
<td>±30 A</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>-</td>
<td>100 kHz</td>
</tr>
<tr>
<td>CM transient immunity</td>
<td>-</td>
<td>±50 V/ns</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>-</td>
<td>1.2 kV</td>
</tr>
<tr>
<td>Configurable short-circuit threshold</td>
<td>100 A</td>
<td>800 A</td>
</tr>
<tr>
<td>Short-circuit detection time</td>
<td>-</td>
<td>80 ns</td>
</tr>
<tr>
<td>Configurable two-level turn-off</td>
<td>7 V, 500 ns</td>
<td>10 V, 3000 ns</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>-</td>
<td>110 ns</td>
</tr>
<tr>
<td>Active Miller clamp</td>
<td>5 A</td>
<td>20 A</td>
</tr>
<tr>
<td>Under voltage lock-out protection</td>
<td>11 V</td>
<td>15 V</td>
</tr>
</tbody>
</table>

the basic clamped inductive double-pulse (multiple-pulse) test. A multi-pulse signal is sent from the function generator to the gate drive IC of the bottom switch. The top switch is kept off with a gate-source voltage of −4 V. A test will be performed at \( V_{ds} = 600 \text{ V} \) under equal gate resistance for both turn-on and turn-off of \( R_{g,on} = R_{g,off} = 0.1 \Omega \). By briefly looking at [161], it can be seen that the internal resistance of the used device is \( R_{g,int} = 3 \Omega \). Comparing the \( R_{g,ext} \) to \( R_{g,int} \), the difference is over 30 times. This means that the \( R_{g,tot} \) is basically dominated by \( R_{g,int} \) which puts a limitation on how fast the switch can be turned on or turned off. Basically, the switch cannot be switched faster, since the elimination of 0.1Ω would only decrease total gate resistance by 3.3%. Therefore, the gate-driver circuit is already driving SiC MOSFET switches at it fastest, meaning that the circuit will be tested at the harshest conditions with respect to the possible influence of the common-mode currents created by \( \frac{dv}{dt} \). As for the RSCS (shown on Fig. 2.11 (a) with fundamentals of operation explained in Section 3.3.6), the output voltage of the integrator is filtered with the 28.3 MHz high
frequency RC filter enabling the RSCS to measure high bandwidth (BW), pulsating current with correct amplitude and high accuracy. This sensed current can be used for protection (high BW loop) as well as for phase current reconstruction and temperature estimation (low BW loop). High bandwidth sensed current is being sent to the comparator without introducing any blanking time, allowing ultra-fast short-circuit detection and protection. Low bandwidth current information (filtered with a cutoff frequency of 2.1 MHz to eliminate high frequency ringing during switching instances) is sent through a level shifter to a high precision 12 bit ADC with a sample rate of 2.5 Msps communicating with the FPGA, which performs phase current reconstruction and temperature estimation tasks.

![Diagram](image)

**Figure 2.11:** Rogowski switch-current sensor. (a) Circuit schematics. (b) Waveforms. [Probes]: Ch1 ($I_{PEM}$): PEM CWT-3b @30 MHz, Ch2 ($I_{hbw}$): TPP1000 @1 GHz, Ch3 ($I_{lbw}$): TPP1000 @1 GHz, Ch4 ($V_{ds}$): THDP0200 @200 MHz. [Time scale]: 1 µs/div.

Fig. 2.11 (b) verifies the gate driver operation in a multi-pulse test under $V_{dc} = 600$ V and $I_d = 400$ A on a CAS300M12BM2. Furthermore, it shows RSCS waveforms and a comparison with the commercial switch current measurement. The bottom-side SiC MOSFET is the device under test (DUT), and the measured variables are as labeled on Fig. 2.11 (a).
RSCS $I_{\text{lbw}}$ performs comparably to the commercial PEM CWT-3b Rogowski probe, with the integrator and filter stage precisely tuned, having a cutoff frequency of 28.3 MHz. Moreover, the low bandwidth waveform ($I_{\text{lbw}}$) of 2.1 MHz demonstrates that the RSCS exhibits the capability to perform as a current-control sensor and $T_j$ sensor. The current relative error is low and is around 1\% for frequencies higher than 10 kHz [150]. These results are promising for switching frequencies above 10 kHz, which are the intended SiC MOSFET device domain.

$V_{\text{ds, on}}$ Sensor Measurement Evaluation

The $V_{\text{d-ps, on}}$ voltage sensor performance has been verified against a commercial clip probe, The Clipper CLP1500V15A1 Measurement Probe (clips high voltages while enables measurement of low voltages < 2 V or 12 V depending on the range), in a pulse test with $f_{\text{sw}} = 30$ kHz. This is shown in Fig. 2.12. The bottom device of the HB SiC MOSFET is the DUT, and the measured variables are labeled in Fig. 2.6. The $V_{\text{d-ps, on}}$ measurement shows promising results, almost completely overlapping the results obtained with the CLP1500V15A1 after the switching oscillations pass. Inaccuracy during the switching transient is not important, since the temperature estimation will be performed during the rest of on-time, sampling the clean waveform. Nevertheless, since the first 4 $\mu$s after switching, the sampling voltage and current are not correct. This puts a limitation on the applicability when the switching frequency is high and for short duty cycles.

To further inspect the performance of $V_{\text{d-ps, on}}$ measurement, a series of tests have been performed by comparing it to a commercial voltage sensor. Fig. 2.13. (a) shows that the dc accuracy of the developed sensor is higher than 99\% when the measured voltage is $|V_{\text{ds, on}}| > 0.2$ V, at both room and elevated temperature. An error in this case is measured with the switch being constantly on, where the current through the switch is controlled to vary the measured voltage. Fig. 2.13. (b) shows the relative error during switching, with a frequency
of 30 kHz in a buck configuration under the different temperatures of the measurement circuit with varied current through the system. To force the currents through the bottom switch in the HB in both directions (negative and positive), the load connection is changed between a -dc and +dc bus connection. Referring to Fig. 2.12, accuracy is compared at the point of 4 \( \mu \text{s} \) for both positive and negative currents. Results indicate that the developed sensors exhibit relatively high accuracy (error < 2 \%) for voltages \(|V_{\text{ds,on}}| > 0.25 \text{ V}\) which corresponds to roughly 40 A, at room temperatures. Considering this, the developed \(V_{\text{ds,on}}\) and \(I_d\) sensors are valid for \(T_j\) estimation with relatively high accuracy when \(I_d > 40 \text{ A}\), and when the on-time is longer than 4 \(\mu \text{s}\).
2.4 Device Calibration Procedure for Obtaining $T_j$

Device Model

2.4.1 Procedure and Algorithm

To represent the $T_j$ device model, the output I-V characteristics (or $R_{ds,on}$ characteristics) throughout the whole temperature range $-40^\circ C - 150^\circ C$ are required. The simplest way is through double-pulse testing (DPT). The first pulse will be used to vary current throughout the procedure, while during the second pulse, $V_{d-ps, on}$ and $I_d$ will be recorded. If the same switch that is being calibrated is used for the rising inductor current, there is a strong possibility that the $T_j$ will rise above the intended temperature on the device that is being characterized, compromising the accuracy of the results. According to the module datasheet [161], the transient thermal impedance for $200 \mu s$ duration of the pulse is $Z_{th,je} = 3 \text{ m}^\circ C/\text{W}$, which means that for the worst case scenario of $300 \text{ A}$, $600 \text{ V}$, $150^\circ C$, switching every $200 \text{ ms}$,
junction temperature will increase for $\Delta T_j = 2.3^\circ C$. Depicted in Fig. 2.14, with the simple utilization of “full-bridge”, possible heating of the device during calibration is avoided. Fig. 2.14 (a) illustrates the procedure when $I_d > 0$ A for the bottom switch in the HB. The first pulse ($t_1$) increases the inductor current to the desired value using switch $S2$, while the second pulse ($t_3$) is on the $S4$, which is DUT. Thus, calibration of the device takes place by recording the current from the RSCS and on-state voltage from the two-diode circuit. The second pulse, $t_3 = 10 \mu s$, is long enough for the switching transient to pass, making measurements stable, and short enough not to make significant current rise, thus keeping the $T_j$ unchanged. After this pulse, a 200 ms break is inserted to make sure that the current in the inductor reduces to 0 A. This sequence of events is repeated 16 times for each current, and then the results are averaged. Every following $t_1$ is increased by 1 µs, increasing the current by 1 A, at the 600 V dc bus.

For the negative current direction through the device, the top device is used to increase the current in the system (shown in Fig. 2.14 (b)). During the freewheeling period, DUT is turned on, enabling the capture of $V_{ds, on}$ and $I_d$, thus obtaining the output characteristics. For the
characterization of the top device, the procedure is similar and is shown in Fig. 2.14 (c) and Fig. 2.14 (d). All tests are performed under $V_{gs, on} = 20$ V.

The previously described procedure is just a part of a complete calibration algorithm, which is depicted in Fig. 2.15. Reflecting to an algorithm, before the actual calibration takes place, a selection is made which device in full bridge will be characterized, after which an offset compensation is performed to minimize the effect of possible inaccuracies. Then, current direction is chosen. Calibration is performed for every $\Delta T_j = 5$ °C, as shown in Fig. 2.15. Calibration is performed up to 135 °C, incorporating the 10% margin usually considered in converter continuous operation. The assumption is that $T_j$ is equal to baseplate temperature $T_{DBC}$ during heating, since the device is heated constantly, and measurements are taken after the system reaches thermal equilibrium.

Calibration hardware is shown in Fig. 2.16. The inductor is designed in such a way that the value is high enough to make the current stable during the second pulse, but not too high to discharge the capacitor bank during the first pulse and see non-linear current rise. Therefore, the inductor is selected to be $L = 600 \mu H$. The busbar and capacitor bank were designed according to the instruction in [162]. Overall stray inductance of the power loop is $L_{stray} < 20$ nH with total dc capacitance of $C_{dc} = 110 \mu F$. Both modules will be mounted on the hot-plate for temperature control with thermal couple. A custom control board containing a TI LAUNCHXL-F28379D controller and a custom-made signal processing board is developed for better control and acquisition of signals coming from the GD of the characterized device. Since the output I-V characteristics (or $R_{ds, on}$ characteristics) are not dependent on the applied voltage over the drain-source in off-state, the calibration procedure will be executed only at $V_{dc} = 600$ V. After the complete characterization is finalized, the collected data in the control board is sent to a personal computer for data manipulation and interpolation. After that, the obtained device thermal model or LUT is downloaded back to
the FLASH memory on the GD of the calibrated device.

### 2.4.2 Calibration Results and Comparison with Curve Tracer

Since maximum $T_j$ of the CAS300M12BM2 module is $T_j = 150\, ^\circ C$, for estimation, thus control, a margin of 10\% is incorporated. Therefore, the maximum value written in memory will be $T_j = 135\, ^\circ C$, which is the maximum temperature under which the device is characterized. For now, minimum values are set to be $30\, ^\circ C$, which for different applications can vary...
For now, to verify the methodology and accuracy of the approach, only the bottom device of the HB module will be calibrated. Calibration results for $T_j \epsilon (30 ^\circ C - 135 ^\circ C)$ are shown in Fig. 2.17 (a) and Fig. 2.17 (b), for negative and positive currents, respectively. The measurements exhibit temperature sensitivity though the whole temperature range and show great potential for the $T_j$ model, verifying the initial statement that SiC MOSFETs exhibit significant $V_{ds, on}$ temperature dependency. In this case, sensitivity of 4.5 mV/°C at 200 A, through the tested temperature range is observed.

One way to validate the measurements obtained by the GD and get insight in the accuracy in a meaningful way, would be to compare the $R_{ds, on}$ results with the curve-tracer results for the same device (due to better resolution, rather than comparing output characteristics directly). The comparison between $R_{ds, on}$ measured with the curve-tracer, and the ones
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Figure 2.17: Calibration results at different temperatures. (a) Output characteristics for negative currents. (b) Output characteristics for positive currents.

Figure 2.18: Comparison of calibration results at different temperatures between gate-driver and the Keysight Agilent B1505A curve tracer. SiC MOSFET module heated in a same manner for curve tracer as for gate-driver calibration.
measured with eGD are shown in Fig. 2.18. The results show great overlapping with the curve-tracer measurement of the $R_{ds,on}$ throughout the complete temperature range. One possible issue with utilizing the developed $T_j$ model for the temperature estimation in this format, could possibly arise within currents $|I_d| < 40$ A, since the accuracy of the sensors for low currents and voltages is lower than 98%. Therefore, these current ranges will be excluded for the temperature measurement. This should not be an issue due to the high current nature of the module, and the fact that under low currents, temperature is most likely not as severe. One more slight concern is that in the 3rd quadrant, when the JBS diode of the switch starts conduction, the diode characteristics have much smaller temperature dependence, and clustering of characteristics is observed. However, even though the GD measurements were able to capture and distinguish all of the different characteristics, accuracy in this region might be compromised since the temperature sensitivity is only $1.43 \text{ mV/°C at } -200 \text{ A}$.

Additionally, the initial assumption is that the $T_j = T_{DBC}$ during heating is checked, in order to verify that the proposed calibration method yields acceptable results and that the assumption is relatively valid. Since there is no way to monitor inside die temperature without opening and removing dielectric gel, it is impossible to quantify how much of a difference exists, if any. However, it can be roughly checked, based on the calibration data in Fig. 2.18 and $R_{ds,on} = f(T_j)$ provided in the datasheet [161]. Comparison results are shown in Fig. 2.19. The experimental results are very close to the ones provided by the datasheet dependence of $R_{ds,on}$ as a function of temperature. According to the the graph, maximum discrepancy can be observed around 90-120 degrees Celsius. If we quantify it,

$$
\Delta R_{ds,on,norm,90 \degree C} = R_{ds,on,\text{meas},90 \degree C} - R_{ds,on,norm,90 \degree C} = 0.023.
$$

(2.3)

Multiplying this p.u. value with the base value of resistance for this particular switch of
4.555 mΩ, measured at 25 °C, 150 A, $V_{gs} = 20$ V,

$$\Delta R_{ds, \text{on,} 90 \, ^\circ \text{C}} = \Delta R_{ds, \text{on, norm,} 90 \, ^\circ \text{C}} \cdot 4.555 \, \text{mΩ} = 0.103 \, \text{mΩ}. \quad (2.4)$$

Variation of the on-state resistance of 0.103 mΩ relates to only $2 \, ^\circ \text{C} - 2.5 \, ^\circ \text{C}$ at that range of temperatures ($\geq 90 \, ^\circ \text{C}$). This represents a possible discrepancy between the pre-set and what is believed to be $T_j$ according to provided datasheet $R_{ds, \text{on}} = f(T_j)$ graph and measured $R_{ds, \text{on}}$. Since the discrepancy can only reach $2.5 \, ^\circ \text{C}$ at high temperatures, the initial assumption is not invalidated, considering that the difference is relatively minor.

![Normalized Rds,on vs Temperature](image)

*Figure 2.19:* Comparison results between datasheet $R_{ds, \text{on}} = f(T_j)$ and normalized calibration data.

Generally, the comparison shows that if we know the device output characteristics, due to the great accuracy of the current and voltage sensor, the device does not even need to be calibrated. However, the question remains how would one know the device characteristics of the device without characterization or calibration? This will be addressed in Section 2.7.
2.4.3 Data Manipulation and Thermal Model of the Device

Prior to importing the obtained $T_j$ model from the calibration procedure to FLASH memory, data must be manipulated in a meaningful way in order to be utilized for real-time $T_j$ estimation. Data will be reorganized on a PC to form a 4096x4096 (16 Mb) look-up table (LUT) which will be downloaded into FLASH memory. Fig. 2.20 (a) illustrates the 2D mapping. From previous discussion, for $I_d < 40 \text{ A}$, temperature estimation will be disabled, and the LUT will be populated with 0 °C. Temperature values higher than 135 °C, are populated with 135 °C for both positive and negative currents. Therefore, in the experiments when the estimated temperature has the maximum value written in memory ($T_j = 135 \text{ °C}$), it can be recognized easily as the condition where the over-temperature condition exists. After that, the experimental data (output curves) are interpolated using a bilinear interpolation. The reason was to obtain a more detailed data-set and to get the points between characterized curves to increase the accuracy of measurements, rather than having 5 degree steps in measurement only as the possibility. Just like before, temperatures lower than 30 °C, are populated with 30 °C for both positive and negative currents. The remaining points in the LUT will indicate a measurement error, since for positive currents, voltages cannot be negative and vice-versa. A temperature of 15 °C will indicate a junction temperature estimation error in measurement, which can be a helpful indicator if any of the measurements malfunction. This finalizes the LUT used for $T_j$ estimation. Fig. 2.20 (b) shows the 3D map (LUT) downloaded to FLASH memory. For the implemented map in its final form, inputs will be $I_d$ and $V_{ds, on}$ values (these values form a 24 bit address) which will ultimately return $T_j$ (value of the targeted address), that will be observable on the output DAC, as described in Section 2.3.2.

The previous discussion is done for one device in HB to verify the methodology. However, for the final implementation, both devices within HB will have junction temperature estimation...
capability on the GD. In that case, the same FLASH memory will be utilized since there is plenty of memory left for utilization. From Fig. 2.20 (a), quadrants of LUT for positive currents-negative voltages and vice-versa were utilized as temperature measurement error indications. Instead of that, these two areas in the memory can serve as the memory for the top device, as shown in Fig. 2.21. To access these when the top device temperature estimation is required, a simple manipulation on the FPGA is necessary to change the voltage polarity. Since the values in the FPGA are binary, this is executed by a simple complement of voltage values.

### 2.5 Converter Level Verification

#### 2.5.1 Double-Pulse Test Verification of $T_J$ Estimation

Before implementing the proposed solution on the converter, it must be verified via double pulse testing (DPT). The same setup that is used for device calibration is used for DPT.
verification of $T_{j,\text{est}}$. DPT is performed at 600 V, for currents 0 A–250 A and for hotplate ranges of 30 °C–135 °C. The same assumption regarding equal $T_j$ and the baseplate temperature $T_{D\text{BC}}$ in the DPT during heating of the hotplate is applied, since the device is heated constantly, and measurements are all taken after the system reaches thermal equilibrium.

Fig. 2.22 shows DPT results at 100 °C, 200 A, and 600 V. The waveforms indicated are $I_d$, $V_{\text{ds, on}}$, and $T_j$ waveforms. At 100 °C, for $I_d = 200$ A (Ch2), on-state voltage is $V_{\text{ds, on}} \approx 1.25$ V (Ch1), which can be confirmed as well, based on Fig. 2.18. Furthermore, the sequence of the $T_j$ estimation procedure is also indicated, as described in Section 2.3.2. For this particular case, sampling will start at 50% of the second pulse, and four samples are taken. After accessing FLASH and retrieving the $T_j$ based on current and voltage, the DAC (Ch3) is accessed, and output is measured at $-0.954$ V. According to design, (2.5) shows that junction temperature is $T_{j,\text{est}} = 98.2$ °C.
Figure 2.22: Double-pulse test verification at 100°C. Ch1 is $V_{ds,\text{on}}$ measured with TPP1000 @250 MHz. Ch2 is $I_d$ measured with PEM Ultra Mini Rogowski coil CWT06 @500 MHz. Ch3 is $T_j$ measured with TIVH08L+MMCX50 @800 MHz. Time scale: 2.5 µs/div.

This simple DPT test verifies the approach; however, accuracy and precision (repeatability) have to be investigated throughout the complete temperature range for better insight.

Fig. 2.23 shows accuracy and repeatability throughout the complete temperature range 30°C–135°C. At each temperature, the device is tested under 4 different values of $I_d\epsilon\{50, 100, 150, 200A\}$. Fig.2.23 (a) shows that absolute average error increases with the temperature with the maximum absolute error up to 5°C. Furthermore, the average relative error is around 2% while the maximum is 3.2% at the highest tested temperatures. One of the most important aspects of the measurement system is repeatability. Fig.2.23 (b) shows absolute repeatability of every measured point around the averaged absolute value of those
points. It can be seen that great clustering is obtained and absolute repeatability is $\pm 1.2^\circ\text{C}$.

### 2.5.2 $T_j$ Estimation in Continuous Operation

Since the performance of all sensors have been shown in the previous sections, the last step is to validate the temperature estimation performance in a continuous operation. The same setup used for calibration, and DPTs will be used to verify the temperature estimation in continuous operation; however, it will be operated in a pump-back platform \cite{163}, recirculating energy between the two HBs, drawing only losses from the dc source. The system operated in the closed-loop, where the current in the system was controlled based on the developed phase current sensor ($I_{\text{ind}}^{\text{RCS}}$) feedback coming from the DUT GD. The system (and thus DUT) operated under $V_{\text{dc}} = 500\text{ V}$, positive $I_{\text{ind}} = I_d = 100\text{ A}$, switching frequency of $f_{\text{sw}} = 10\text{ kHz}$, duty cycle $D = 0.5$, and circulating 25 kW power in the system for 1 h sitting on the heatsink. The waveforms are shown in Fig. 2.24 (a). After the modules and the heatsink reached thermal equilibrium, the temperature measured with the developed sensor is $T_{\text{estim}} = 71.6^\circ\text{C}$. The maximum baseplate temperature on the DUT measured with the thermal camera is $64.3^\circ\text{C}$, as shown in Fig. 2.24 (b). To observe the DUT $T_j$ with a thermal camera would require opening the module and the removal of the dielectric gel. This would
reduce the reliable operation and limit the operation of the module with regards to the maximum blocking voltage; therefore, to verify the obtained results, $T_j$ is estimated through a rough thermal model. Since the baseplate (case) temperature is directly measured, the $T_j$ is roughly calculated with an aid of the estimated losses and the junction to case thermal resistance $R_{th,j-b,DUT} = 0.07 \, \text{K/W}$. Both are provided in the datasheet of the device. This type of verification is possible since device switching, conduction losses, and the thermal model are generally known under constant conditions in the pump-back. Furthermore the SiC MOSFET power module was at the beginning of its lifetime, thus there was no developing degradation. The maximum junction temperature is estimated to be $T_{j,DUT} = 69.3 \, ^\circ\text{C}$, according to (4.9),

$$T_{j,DUT} = P_{tot,DUT} \cdot R_{th,j-b,DUT} + T_{b,\text{max},DUT}$$

(2.6)

where $P_{tot,DUT} \approx 68 \, \text{W}$ are total DUT losses incorporating conduction, turn-on and turn-off switching losses, and $T_{b,\text{max},DUT}$ is the maximum baseplate temperature on the DUT.

It can be seen that both the calculated temperature (based on the thermal model) and the measured one with the developed temperature sensor are very similar, with the difference
of only $\approx 2.3^\circ C$. With this, the performance of the developed $T_j$ sensor is verified in the continuous operation. This implies that it can be utilized successfully for any active thermal control no matter how sophisticated it is, as well as for the condition monitoring of the SiC MOSFET device such as state-of-health, remaining useful life, and maintenance scheduling.

### 2.6 Discussion about Degradation Monitoring and Aging Compensation Scheme

#### 2.6.1 Degradation Monitoring

During the lifetime of the converter, the power semiconductor switches degrade or age. This can affect the thermal and electrical parameters of the device. In this case, it is the I-V ($R_{ds,\text{on}}$) characteristics that make the junction temperature measurement inaccurate and unreliable over the aging process. As Section II showed, different degradation mechanisms can have different impacts on the $R_{ds,\text{on}}$. This makes the degradation detection of the $R_{ds,\text{on}}$ essential to the implementation of an aging compensation scheme, which would enable an accurate measurement of $T_j$ during its lifetime. In this work, degradation detection will be based on the detection in changes of $V_{d-\text{ps,}\text{on}}$.

The proposed circuit in Fig. 2.6 can enable degradation monitoring, and if desired, can decouple degradation occurring at different locations. That is, is it the semiconductor related degradation or the wire-bond related fatigue? This can be executed by separately monitoring voltages $V_{d-\text{ks,}\text{on}}$ and $V_{\text{ks-ps,}\text{on}}$ with the control of the signal MOSFET switches M2 and M3. As shown on Fig. 2.25 (a), if the M2 and M3 are both on, the output of the measurement circuit is measuring the complete on-state drain-to-power source voltage $V_{d-\text{ps,}\text{on}}$ according to (2.7), if $R_5 = R_6 = R_7 = R_8$. As shown in Fig. 2.25 (b), if the switch M2 is on and M3
is off, the output of the measurement circuit measures the on-state drain-to-kelvin source voltage proportional to $V_{d-ks,on}$ according to (2.8). As shown in Fig. 2.25 (c), if the switch M2 is off and M3 is on, the output of the measurement circuit is measuring the negative voltage drop over the wire-bonds $V_{ks-ps,on}$ according to (2.9)

$$V_{\text{diff,out}} = V_{d-ks,on} - V_{ks-ps,on} = V_{d-ps,on}, \quad (2.7)$$

$$V_{\text{diff,out}} = 1/2 \cdot V_{d-ks,on}, \quad (2.8)$$

$$V_{\text{diff,out}} = -V_{ks-ps,on}. \quad (2.9)$$

**Figure 2.25:** Different configurations of the differential operational amplifier with controlling M2 and M3 signal MOSFETs. (a) M2=ON, M3=ON measuring complete on-state drain-to-power source voltage. (b) M2=ON, M3=OFF measuring on-state drain-to-kelvin source voltage. (c) M2=OFF, M3=ON measuring voltage drop over the wire-bonds.

As for most degradation monitoring techniques, the baseline values of TSEPs are required. Therefore, prior to the converter operation and after the calibration procedure, the baseline values of $V_{d-ks,on,\text{base}}$, $V_{ks-ps,on,\text{base}}$, and $V_{d-ps,on,\text{base}}$ are extracted at the baseline conditions (at certain environment temperature and current). The degradation assessment can be executed when the converter stops operation, or it is in idle state. Since the FPGA has
If $V_{d-\text{ps},\text{on}} < V_{d-\text{ps},\text{on,base}}$
&
if $V_{k_{s}-\text{ps, on}} = V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} < V_{d-k_s,\text{on,base}}$
\quad No wire-bond degradation
\quad Semiconductor degradation exist
if $V_{k_s-\text{ps, on}} > V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} < V_{d-k_s,\text{on,base}}$
\quad Wire-bond degradation exist
\quad Semiconductor degradation exist

If $V_{d-\text{ps, on}} > V_{d-\text{ps, on, base}}$
&
if $V_{k_{s}-\text{ps, on}} = V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} > V_{d-k_s,\text{on,base}}$
\quad No wire-bond degradation
\quad Semiconductor degradation exist
if $V_{k_s-\text{ps, on}} > V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} < V_{d-k_s,\text{on,base}}$
\quad Wire-bond degradation exist
\quad Semiconductor degradation exist
if $V_{k_s-\text{ps, on}} = V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} = V_{d-k_s,\text{on,base}}$
\quad No semiconductor degradation

If $V_{d-\text{ps, on}} = V_{d-\text{ps, on, base}}$
&
if $V_{k_{s}-\text{ps, on}} = V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} < V_{d-k_s,\text{on,base}}$
\quad No wire-bond degradation
\quad No semiconductor degradation
if $V_{k_s-\text{ps, on}} > V_{k_{s}-\text{ps, on, base}}$
\quad $V_{d-k_s,\text{on}} < V_{d-k_s,\text{on,base}}$
\quad Wire-bond degradation exist
\quad Semiconductor degradation exist

Figure 2.26: Possibilities of degradation location for different values of measured $V_{d-\text{ps, on}}$, $V_{d-k_s,\text{on}}$ and $V_{k_s-\text{ps, on}}$ voltages.

Information of the switch current (through RSCS) under the same conditions as the baseline measurement, the first step in the degradation assessment is to measure $V_{d-\text{ps, on}}$, and compare it to the baseline value of $V_{d-\text{ps, on, base}}$. In the next instances, $V_{k_s-\text{ps, on}}$ and $V_{d-k_s,\text{on}}$ can be measured and compared to baseline values $V_{k_s-\text{ps, on, base}}$ and $V_{d-k_s,\text{on, base}}$, respectively. With this, it is possible to determine the location of the degradation. Fig. 2.26 summarizes possible degradation locations for the different values of measured voltages. Measured $V_{k_s-\text{ps, on}}$ under the baseline conditions cannot be smaller than $V_{k_s-\text{ps, on, base}}$ since the degradation of wire-bonds can only increase the value of $V_{k_s-\text{ps, on}}$.

Therefore, Fig. 2.26 shows that the flexibility of measuring $V_{d-\text{ps, on}}$, $V_{d-k_s,\text{on}}$ and $V_{k_s-\text{ps, on}}$ is beneficial and can enable the user to determine the location of degradation (semiconductor or wire-bonds) within the power module, as well as to quantify the degradation intensity.
2.6.2 Aging Compensation Scheme

The process of degradation assessment can help in degradation quantification from the $V_{d_{-}ps_{-}on}$ perspective. This information is extremely important in order to implement an aging compensation scheme and to have an accurate measurement of $T_j$ during the lifetime of the device.

Prior to converter operation and after the calibration procedure, the baseline thermal model of the healthy device in the form of a 16Mb (128M-bit) look-up table is known, as shown in Fig. 2.20. If, for instance, 1024Mb (8G-bit) FLASH memory is chosen for implementation on the enhanced gate-driver (instead of the original W25Q128JV 128M-bit in the WSON8 package, use the TH58CVG3S0HRAIJ 8G-bit in the WSON8 as a direct replacement, or the MT29F8G01ADBFD12 in the alternative package), there will be enough memory for 64 thermal models with different degrees and direction of degradation to store.

In FLASH memory, the user can store 1 thermal map (TM) for the healthy device obtained from the calibration procedure (TM ID#32), 32 thermal maps that have higher $V_{d_{-}ps_{-}on}$ than the $V_{d_{-}ps_{-}on_{-}base}$ (TM ID#33-64), and 31 thermal maps that have lower $V_{d_{-}ps_{-}on}$ than the $V_{d_{-}ps_{-}on_{-}base}$ (TM ID#1-31). The thermal maps TM ID#1 and TM ID#64 stored can possibly be the ones before the request for maintenance due to severe degradation. According to [40], a 20% increase in on-state voltage from its initial values can be considered as a wear-out failure for a power device. This means that eventually each TM in the memory will be shifted for $0.62\% \cdot V_{d_{-}ps_{-}on_{-}base}$ “up” or $0.64\% \cdot V_{d_{-}ps_{-}on_{-}base}$ “down” from the previous one, starting from the TM ID#32 (healthy device). With this implementation, the aging compensation is able to compensate for degradation changes of $0.62\%$ for positive $V_{d_{-}ps_{-}on}$ degradation and $0.64\%$ for negative $V_{d_{-}ps_{-}on}$. Fig. 2.27 depicts the simplified process of degradation and aging compensation in an enhanced gate driver where thermal maps are
As mentioned earlier, the degradation assessment can be executed when the converter stops operation, or it is in idle state. This is done by executing 3 switching cycles under the same baseline conditions: sampling current $I_d$, and three different on-state voltages ($V_{d-ps,on}$, $V_{d-ks,on}$, and $V_{ks-ps,on}$). The process of aging compensation is fairly simple. After the degradation assessment, the algorithm decides which, if any, degradation occurred and where, and the degradation quantification is executed. In this step, the difference between the baseline measurement and the current state-of-health of the device is known (basically $\Delta V_{d-ps,on} = V_{d-ps,on} - V_{d-ps,on,base}$). Based on that difference, the TM ID (any ID between...
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#1-#64) is generated. During normal converter operation, this information is utilized in combination with the switch current $I_d$ and on-state voltage $V_{d\text{-ps,on}}$ in every switching cycle to form the correct address for accessing the FLASH memory. With this, different TMs, with different amounts of degradation, can be accessed, thus effectively compensating for the device aging, and enabling accurate measurement of $T_j$ during its lifetime. Additionally, the degradation’s magnitude, location, and number of aging compensations should be monitored from the main system controller, since $V_{k\text{-ds, on}}$ and $V_{k\text{ps, on}}$ can possibly degrade in opposite directions. Maintenance should be scheduled as soon as either of them degrade for more than 20%.

2.7 Junction Temperature Measurement Generalization

2.7.1 Background

As claimed in [164], datasheet information cannot be used directly for estimating the junction temperature due to device tolerances, measurement inaccuracies, etc. For example, for the selected CAS300M12BM2, rated $R_{d\text{on}} = 4.2 \, \text{mΩ}$ with a given tolerance of $1.1 \, \text{mΩ}$. This implies that by implementing the datasheet extracted $R_{d\text{on}}$ temperature map for positive currents (1st quadrant operation), an error expected can be up to $50^\circ\text{C}$–$55^\circ\text{C}$, and for negative currents, when the diode conducts, up to $190^\circ\text{C}$. Therefore, every component must be individually characterized. However, Fig. 2.18 shows that the developed measurement is capable of capturing output characteristics with high accuracy for currents over $40 \, \text{A}$. This opens the possibility for generalization of the proposed method, thus possibly avoiding every component individual characterization. Here, a generalized method is proposed under the assumption that any data from the semiconductor device characterization will be known.
either from the manufacturer or the pre-converter device static characterization. The generalized method consists of two parts. First, the extraction of the output characteristics or $R_{ds, on}$ temperature map from the datasheet is performed, while the second is basic functionality qualification curve tracer data if no data is known about this particular device from the manufacturer.

### 2.7.2 $R_{ds}$ (I-V) Map Datasheet Extraction

The first step in generalization is the output characteristics (or $R_{ds, on}$) thermal map datasheet extraction.

From the datasheet, I-V curves shown in Fig. 2.28 are extracted point by point. These points are then reconfigured to form a $R_{ds, on}$ temperature map. For positive current range, each data-set is described with a quadratic polynomial function. For negative current range, during MOSFET conduction, each data-set is described with a quadratic polynomial function;
while during diode conduction, each is described with the 4th degree polynomial function. A diode knee equation can also be extracted from the three points (where MOSFET conduction stops, and diode begins) in the form of a quadratic polynomial function. These equations and regions are indicated in Fig. 2.29. Now, a complete thermal map must be extracted, and different $R_{ds,on}$ curves every 5 °C will populate the map. After this is complete, the same approach as before will take place, linearly interpolating points to obtain a smooth 3D distribution of points, suitable for FLASH LUT.

For MOSFET conduction regions (until the diode knee curve), from datasheet normalized on-resistance vs. temperature curve at rated current (in this case 300 A), dependence can be extracted in the form of a quadratic polynomial function, as shown in (2.10):

$$R_{ds,on,I_{d,\text{rtd}}} = a \cdot T_j^2 + b \cdot T_j + c.$$  \hspace{1cm} (2.10)

Under the assumption that the same $R_{ds,on}$ distribution can be applied throughout the complete MOSFET conduction range, and to obtain a temperature map for the MOSFET...
regions, scaling of the (2.10) function when the current $I_d \neq I_{d,rtd}(300 \text{ A})$ will be performed. The principle is very simple, and it is referred to as linear scaling of the quadratic equation, described with (2.11), (2.12):

$$R_{ds,on}(T_j, I_d) = R_{ds,on,I_d,rtd} \cdot \frac{R_{ds,on,I_d,rtd}@150^\circ C - R_{ds,on,I_d,rtd}@-40^\circ C}{R_{ds,on,I_d}@150^\circ C - R_{ds,on,I_d}@-40^\circ C} + OFFSET$$

(2.11)

$$OFFSET = R_{ds,on,I_d}@-40^\circ C - R_{ds,on,I_d,rtd}@-40^\circ C.$$  

(2.12)

With this approach, a complete MOSFET conduction region $R_{ds,on}$ map can easily be generated.

For the diode conduction region, extracted $R_{ds,on} = f(T_j)@ - I_{d,rtd}$ will be utilized to obtain the $R_{ds,on}$ map for the diode conduction piece. Similar as before, under the assumption that extracted $R_{ds,on}$ distribution can be applied throughout the complete diode conduction current range, scaling of the new quadratic on-state resistance vs. temperature at negative rated current function will be performed. With this approach, a negative current range $R_{ds,on}$ map can now be fully generated. Fig. 2.30 shows a complete datasheet extracted thermal $R_{ds,on}$ every 5 $^\circ C$.

2.7.3 Scaling the Extracted Datasheet Map and Results

The second step is scaling the datasheet extracted $R_{ds,on}$ thermal map according to the pre-converter basic functionality static test of the module.

A relatively simple datasheet thermal map extraction and the capability of GD embedded
measurements to faithfully represent output characteristics dictate that the generalization can rely mostly on them and the manufacturer’s ability to produce modules very close to datasheet values. Prior to implementing the desired module or device into the converter, a simple curve-tracer basic static functionality test is performed (threshold voltage, transfer characteristic, output characteristic, breakdown voltage, etc.,) at room temperature to qualify the module. If the output characteristics are known from either the manufacturer or by performing an actual characterization, the datasheet extracted map can be scaled up or down according to measured $R_{ds,on}$ at the characterized temperature. To illustrate the idea, a new CAS300M12BM2 module sample is characterized at 25 °C, and the $R_{ds,on}$ is extracted. Fig. 2.31 (a) shows that it differs from the ideal $R_{ds,on}$ datasheet value for 0.4 mΩ, but it is within given datasheet tolerance. Therefore, a complete datasheet $R_{ds,on}$ map will be shifted up until the two characteristics (experimental and datasheet ones) on 25 °C overlap, as shown of Fig. 2.31 (b). With this manipulation, the thermal map can now be finalized. The same approach as described in Section 2.4.3 takes place: linearly interpolating points to obtain smooth 3D distribution of points and downloading the map into the FLASH on the
Figure 2.31: (a) Difference between the datasheet extracted and the curve tracer measured $R_{ds, on}$. (b) Datasheet extracted thermal $R_{ds, on}$ scaled based on the curve tracer module qualification experimental results on 25°C.

Once the thermal map based on output characteristics is downloaded onto the FLASH on the gate-driver, preliminary testing is performed to evaluate the validity of this approach. Compared to implementing the purely datasheet extracted thermal map, errors are reduced immensely. For example at 200 A, 100 °C for a purely datasheet extracted map, the measurement would return $T_j = 118 °C$, while with scaled it returns 95 °C.

2.8 Summary

For SiC converters having reduced converter sizes, the knowledge of the junction temperature $T_j$ is important due to their high susceptibility to thermal cycling. This chapter provides a systematic approach for $T_j$ estimation, utilizing an enhanced gate-driver (eGD) with the embedded Rogowski switch-current sensor (RSCS) and the two-diode on-state voltage measurement $V_{ds, on}$. The developed sensors exhibit high accuracy (> 99 %) for the currents higher
than 40 A, at both high and low temperature, at the switching frequencies $f_{sw} \geq 10$ kHz, and after turn-on switching oscillations pass, which in the implemented converter is after initial $4 \mu s$. The calibration procedure is developed avoiding potential increases of the $T_j$ during the procedure. The calibration results showed great promise and are validated against the baseline curve-tracer measurements, showing great potential for accurate $T_j$ estimation. The $T_j$ model is developed with incorporated limitations. After pulse validations, $T_j$ exhibits relatively high accuracy with a maximum error of 5 °C at high temperatures and high repeatability with a maximum difference of ±1.2 °C. The $T_j$ sensor is furthermore verified in continuous operation showing promising results. Compared to estimated $T_j$ by the classical method (calculation based on losses of the device and measured heatsink temperature), a discrepancy exists, but is $\approx 2.3$ °C, which validates the approach. Considering the degradation in the SiC MOSFET during its lifetime, a degradation detection method with the ability to locate the degradation to either the semiconductor or wire-bonds is proposed, as well as an aging compensation scheme to improve and mitigate the aging’s effect on $T_j$ measurement accuracy. Additionally, generalized junction temperature monitoring is proposed, potentially avoiding often complicated calibration procedures. With all of this being said, $T_j$ integrated on an eGD can enable active thermal control, including dynamic rating control, parallel converter current sharing, and condition monitoring, along with detection of wear-out, abnormal operations, maintenance scheduling, over-temperature detection, etc.
Chapter 3

Enhanced Gate-Driven and Device Characterization of 10 kV High-Current SiC MOSFET Half-Bridge Modules

3.1 Introduction

The device chosen as a kernel part of the power cell is a 10 kV, 240 A Gen-3 SiC MOSFET XHV-6 from CREE/Wolfspeed. As previously mentioned, the GD must be designed since there is no commercial one available. Fig. 3.1 shows the state-of-the-art GDs utilized for 10 kV SiC MOSFET devices with an emphasis on blocking voltage, capacitance, and general comments about size, intelligence, and driving capabilities [116, 117, 165, 166, 167, 168, 169, 170, 171].

First, as shown from Fig. 3.1, none of the GDs have sufficient intelligence and the high-speed communications necessary to satisfy the requirements imposed by the intended novel control methodologies i.e., SCC and ICBT. Second, most of the GD designs have $\leq 4\, \text{pF}$ isolation capacitance, highly desirable to minimize the CM current caused by the $dv/dt$ point of view, as well as high isolation voltage that is $\geq 10\, \text{kV}$. From purely common-mode transient immunity (CMTI) and general isolation perspectives, the ideal choice would be to utilize power over the fiber technology proposed by [169], with a redesign and additional intelligence necessary for control. This solution exhibits no isolation capacitance and has the
possibility to achieve extremely high maximum isolation voltage, even though the authors tested only 20 kV. However, this solution has only 0.5 W with an extremely large primary side and large gate-loop inductance $L_{gs}$, which renders it unsuitable for use. Third, most of the gate drivers utilize DeSat protection. This can possibly present an issue since the protection requires a long blanking-time to filter out the severe drain-source ringing at turn-on due to the high $dv_{ds}/dt$ noises from the power stage. Long blanking-time is not suitable for most SiC MOSFET modules since they evidence much lower SC robustness [31]. This makes DeSat protection for SiC MOSFETs extremely difficult to tune. It often requires additional noise suppression circuits due to high $dv_{ds}/dt$ and requires special attention for different applications. In [166], fast 200 ns current transformer-based detection is employed for SC protection; however, the transformer size as well as creepage and clearance requirements for the top device in a half-bridge configuration, may prevent its usage. Furthermore, it might severely increase the stray power-loop inductance, degrading switch performance. Fourth,
many presented solutions are not high density and are very bulky due to strict clearance and creepage requirements. An innovative solution was presented in [170], where the single primary side can supply multiple secondary sides, meanwhile preserving high power density, and exhibiting very low coupling capacitance.

Therefore, due to the necessity for an enhanced GD with low coupling capacitance and sufficient intelligence for SCC and ICBT control (local current measurement for SC protection and control, peak-current mode control, and fast communications with the controller), a GD will be designed. The design proposed in [172] will be expanded, where the Rogowski coil switch-current sensor (RSCS) [149, 150] will be used as the switch current measurement. Furthermore, the solution proposed in [170] for the power supply will be further improved and employed, trying to achieve $\leq 3$ pF supplying power to both gate drivers and sensors in the future power-cells. Before the GD design, the XHV-6 device will be statically characterized to obtain further information necessary (i.e., parasitic capacitances, threshold voltage) for the design, and to obtain additional details of the device that will define its behavior during operation.

### 3.2 High-Voltage SiC MOSFET Device Static Characterization

#### 3.2.1 Equipment and Procedure

A high-voltage, high-current XHV-6 18 die SiC MOSFET is under development, and due to the absence of a complete datasheet, it is necessary to completely characterize and fully evaluate its potential and estimate its performance in converter systems. The static characterizations will be carried out mounted on a hotplate to regulate its junction temperature
from 25°C–175°C. To achieve 240 A, all three submodules are shorted both power- and control-wise. The device will be characterized for output (I-V) characteristics and on-state resistances, transfer characteristics, junction parasitic capacitances, threshold voltage, and breakdown voltage. All static characteristics of the XHV-6 18 die SiC MOSFET are measured using the Keysight B1505A curve tracer with a N1273A capacitance test fixture and high-voltage expander for high-voltage breakdown voltage characterization. The experimental setup is shown in Fig. 3.2.

![Experimental setup for static characterization of the XHV-6 device.](image)

**Figure 3.2:** Experimental setup for static characterization of the XHV-6 device.

### 3.2.2 Experimental Results

#### Output Characteristics and On-state Resistances

The first quadrant output characteristics, shown in Fig. 3.3, are measured under different gate voltage $V_{gs}$ up to 20 V. These characteristics are typical for an SiC MOSFET and as can be seen with temperature, the device becomes more lossy as the on-state resistance becomes significantly higher. This will be shown later.

The third quadrant output characteristics, shown in Fig. 3.4, are measured under different...
$V_{gs}$ starting from $-5$ V–20 V. The characterization of 10 kV SiC MOSFETs revealed a higher $V_{ds, on}$ for positive $V_{gs}$ than the one at negative $V_{gs}$ under high temperatures for the same currents. This behavior is contrary to that of 1.2 kV devices and has not been reported in the literature. Typically (for lower voltage devices), in this reverse conduction case, the slope of the drain-source current (i.e., on-state resistance) is similar to the on-state resistance in the forward conduction state, for the low current cases. However, at higher currents, the body-diode starts to influence the MOSFET channel conduction, and the inherent body-diode starts supporting the reverse conduction of the MOSFET channel. At the highest currents, the MOSFET characteristics almost completely merge with the diode characteristics. From Fig. 3.4, it can be seen that the MOSFET characteristics and MOSFET body diode characteristics intersect at high temperature for the characterized device. This phenomenon is thoroughly explained in [173]. It is stated that with the increase in the device voltage rating, the percentage of drift region resistance $R_{drift}$ in $R_{ds, on}$ increases, and the turn-on voltage of body diode $V_{bd, on}$ increases. For the 10 kV MOSFET, as $R_{drift}$ dominates $R_{ds, on}$, when the MOSFET channel is on, $V_{bd, on}$ is very high, and the body diode cannot turn on in a safe $V_{ds, on}$ operation range. At higher temperatures, the diode knee decreases, and this factor lowers the voltage drop of the body diode at higher temperatures, while the MOSFET channel
voltage drop severely increases; this makes this effect more observable. According to this, a standard synchronous rectifier control might not be optimal at high temperatures and high currents, since the lower resistance in the body diode path compensates its higher turn-on voltage, leading to a lower 3rd quadrant voltage drop and conduction loss for a negative $V_{gs}$ control.

Figure 3.4: Third quadrant output (I-V) characteristics of the XHV-6 SiC MOSFET as dependence of $V_{gs}$, $I_d$, and $T_j$.

Fig. 4.3 shows $R_{ds,on}$ of the 18 die XHV-6 and its temperature dependence.

Figure 3.5: On-state resistance vs. current and temperature for 1st and 3rd quadrant, $V_{gs} = 18$ V.
Compared to low-voltage 1.2 kV SiC MOSFET devices, with temperature-dependent $R_{\text{ds,on}}$ being no more than 200% from 25 °C to 175 °C [174], the characterized 10 kV device evidences much higher dependence of 340% for the same temperature range (21 mΩ @25 °C, 84 A and 72 mΩ @175 °C, 84 A). Thus, the 10 kV device conduction loss is significantly impacted by its junction temperature. The reason behind that is, for the HV SiC MOSFET devices, the output characteristics are dominated by the drift resistance $R_{\text{drift}}$ in the device structure, whose effect is further amplified at elevated $T_j$, for the same $V_{\text{gs}}$ [175]. $R_{\text{ds,on}} = f(I_d, T_j)$ is roughly similar for the 3rd quadrant operation, slightly lower compared to the 1st quadrant at higher temperatures and high currents. Even though the MOSFET channel is mostly conducting, the effect of the MOSFET body diode can still be slightly observed.

**Transfer Characteristics**

Fig. 3.6 shows the transfer characteristic and transconductance and their dependence from junction temperature. The peak transconductance is in the range of 35 S at room temperature. With similar trends, as shown in [176], it shows an increasing trend with an increase in temperature from 36 S@25 °C - 40 S@175 °C.

**Parasitic Capacitances**

The device parasitic capacitors provide better insight into the dynamics of the device. Input capacitance $C_{\text{iss}}$, consisting of gate-to-source $C_{\text{gs}}$ and reverse transfer $C_{\text{rss}}$ capacitance, will largely determine the device turn-on and turn-off transient behaviour [177]. Output capacitance $C_{\text{oss}}$ will aid in obtaining the correct switching losses of the device. Inability to measure $C_{\text{oss}}$ charge and discharge currents results in the experimentally measured current $I_d$ underestimating the turn-on energy $E_{\text{sw,on}}$, while overestimating turn-off energy $E_{\text{sw,off}}$,
since the channel current $I_{ch}$ is significantly different during the switching intervals from $I_d$ [178]. Based on Fig. 3.7, $E_{oss} = 1/2 \cdot C_{oss} V_{ds}^2 = 9 \text{ mJ}$ will be added to the measured $E_{sw, on}$ while it will be subtracted from the measured $E_{sw, off}$ in the following subsection. Apart from the device loses, $C_{oss}$ can provide additional information about transient times, and plays a critical role for zero-voltage-switching (ZVS) applications. $C_{rss}$, crucial in determining in device transient behaviour (part of $C_{oss}$ and $C_{iss}$), plays a detrimental role in cross-talk between the two switches in the HB configuration. According to estimated $C_{rss} = 0.2 \text{nF}$, under high $dv/dt$, high currents will be injected into the gate of the device, raising the importance of the cross-talk suppression, Miller-clamping, circuitry. Device junction capacitances are insensitive to the temperature [179]; therefore, all tests are only performed on 25 °C.

Threshold Voltage

Threshold voltage is the minimum $V_{gs}$ needed to create a conducting path between the source and drain terminals (for the device to be able to conduct device current). Threshold voltage influences device dynamics and plays an important role from the EMI per-
Figure 3.7: XHV-6 SiC MOSFET $C_{iss}$, $C_{oss}$, and $C_{rss}$ parasitic capacitance. Experimental results up to 3 kV measured with Agilent B1505A curve tracer with N1273A capacitance test fixture, estimation from 3 kV–10 kV. $C_{iss} = 92.8$ nF considered linear since $C_{iss} \gg C_{rss}$, $C_{oss}(6 \text{kV}) = 0.501$ nF, $C_{rss}(6 \text{kV}) = 0.2$ nF.

Spective of power module operation (cross-talk). Threshold voltage $V_{gs, \text{thrs}}$ distribution is shown in Fig. 3.8. The characterized $V_{gs, \text{thrs}}$ varies with the junction temperature between 3.36 V@175 °C - 4.58 V@25 °C. The extracted $V_{gs, \text{thrs}}$ reduced for 1.22 V indicates the temperature coefficient of 8.13 mV/°C. The threshold voltage $V_{gs, \text{thrs}}$ basically decreases with increasing temperature as expected.

Figure 3.8: Threshold voltage vs. temperature.
Breakdown Voltage

The Keysight Agilent B1505A curve tracer with a high-voltage expander is used to measure the high-voltage SiC MOSFET leakage current and the blocking voltage characteristics. No bias was applied at the gate-source terminals of the device. The maximum voltage up to which a device can be characterized is 10 kV. This test is necessary to ensure the robustness and quality of the manufactured devices. According to the preliminary datasheet, utilized dies have a defined breakdown at 1 mA; therefore, for the characterized 18 die XHV-6 per switch position, the breakdown is defined at 18 mA. Fig. 3.9 shows the breakdown characteristics. The characterized device is well below 18 mA for the entire voltage range and for the entire temperature range as well. This indicates a good blocking capability of the device at rated voltage, and it is clear that it fulfils the prerequisites to be used in high-temperature, harsh environment applications.

![Figure 3.9: Threshold voltage vs. temperature.](image)
3.3 Enhanced Gate-Driver

3.3.1 Background and Specific Requirements

As mentioned earlier, a high-performance GD is a key component that is required to maximize the utilization of the beneficial XHV-6 10 kV, 240 A SiC MOSFET characteristics. Based on the challenges and design focus described in Section 1.2, an initial layout of the gate driver is provided in Fig. 3.10 with the most crucial challenges indicated.

High \( \frac{dv}{dt} \) presents the excitation for the CM noise current due to the existence of the parasitic capacitance of isolation barriers. Power supply coupling capacitance minimization between the primary and secondary side of the transformer is crucial in order to significantly reduce the CM currents. Therefore, the power supply should be designed such that it has \( C_{\text{MTI}} \geq 100 \text{ V/ns} \), meanwhile \( C_{\text{io}} \leq 3 \text{ pF} \). Regarding the high-current driving system with minimized loop-inductance, the maximum driving current will be selected to be \( I_{\text{gs,max}} = 90 \text{ A} \) with a constraint on \( L_{\text{gs,max}} \leq 15 \text{ nH} \) to ensure fast and synchronous driving between the submodules. Additionally, a cross-talk suppression circuit, also called active Miller-clamping,
is essential on the GD for successful operation, and it will be designed. Fast short-circuit protection will be ensured with a high-bandwidth, Rogowski switch-current sensor, and it will also address current control.

3.3.2 Isolated Power Supply

The comprehensive details about this piece of the gate-driver design can be found in [180], and [181], based on research presented in [170]. In this section, just a brief description will be given.

The current transformer-based (CT-based) gate driver power supply (GDPS) design single-turn primary winding approach enables the possibility to achieve low $C_{io}$ in an effective way. This is a fundamental advantage for the CT-based GDPS to minimize the CM currents, suppressing and containing the EMI generated by the 10-kV SiC devices. Furthermore, this design maintains a high power density. Another benefit of the CT-based GDPS is it can supply multiple GDs that can be easily connected in series using the same current source (single-turn) primary cable from a single primary side. In this manner, the operation between different loads (GDs and other sensors) remains independent, providing excellent resiliency to faults. Additionally, its easy and direct insulation can also provide a flexible hardware arrangement, such as changing the number of loads and adjusting the location of the transformer cores. Consequently, due to all of these advantages over the classical voltage transformer-based design, a CT-based design is adopted for the 10-kV SiC MOSFET gate-drive application, as shown in Fig. 3.11 (a), and Fig. 3.11 (b).

The GDPS circuit topology selected is the LCCL-LC soft-switching resonant converter topology, as shown in Fig. 3.11 (a). The circuit operates at the megahertz range as it can deliver a constant high-frequency current to the receiving regulators via a current transformer. The
challenges of the traditional design of LCCL-LC topology are overcome, ensuring zero-voltage switching (ZVS) all of the time for the sending-side devices by making the turn-off current load independent of the number of channels and wiring shapes.

The voltage regulation stage should be designed on each receiving side in order to maintain a desired output voltage over a wide load range. As shown in Fig. 3.11 (a), the hysteresis controller is employed for its simplicity and good dynamic response. In order to prevent the switch S3 operating at a very high frequency, a large $C_o$ is selected, making the switching frequency of S3 much lower, compared to the switching frequency of the switches in the primary side. When an open circuit happens, S3 turns on all of the time to bypass the faulty load while not interfering with other load operations.

The primary side of the converter and air-insulated hardware implementation of the secondary side is shown in Fig. 3.11 (c). As shown in [180], this solution has great transient response and resiliency to open- and short-circuit faults. The proposed design guarantees ZVS all of the time with a load-independent turn-off current, has core temperature that reaches a maximum of 41 celsius, and has PDIV of 5.47 kV with the threshold discharge
value of 10 pC. This is sufficient for future power-cell design since the primary side of the converter will be referenced to the midpoint of the power-cell and has only coupling capacitance $C_{io} = 1.9 \, \text{pF}$.

### 3.3.3 Power Architecture

Apart from the GDPS, the power architecture is one of the most crucial design aspects because it has to be designed to “fight” high CM current caused by the fast $dv/dt$. Basically, the architecture has to be able to bypass CM noise current away from sensitive components. Since a smart gate driver is being developed, this becomes even more critical due to the abundance of analog and digital processing circuitry on the board. In some cases, even the smallest noise voltage is high enough to cause inaccurate sensing, malfunction in communication, false triggering, etc. The implemented architecture is proposed in [172], further elaborated in [160], and shown here in Fig. 3.12.

![Implemented gate-driver architecture](image)

**Figure 3.12:** Implemented gate-driver architecture. GDPS: ISO5125I-120 (4 pF in datasheet, 3.4 pF measured) for 10 kV, or CT-based GDPS (2 pF). GDIC: STGAP1AS (1.6 pF). FPGA: Altera MAX10 10M08SAM153. Digital isolator (Diso): Analog devices ADuM1100.

As shown, blocks with different colors denote different potentials, GP1, GP2, and GP3. GP1
is the potential of the primary side of the utilized GDPS, which can be ground potential, or some local power-cell ground, depending on the overall auxiliary power supply network approach. On the red plane (GP2), the components located are the ones providing the driving current, and creating driving voltages of $20\,\text{V}$ and $-5\,\text{V}$. On the green plane (GP3), sensitive analog and digital signal processing components and logic units with voltages at $\pm 5\,\text{V}$, and $3.3\,\text{V}$ are located. With such placing, the architecture implements an impedance control technique. The components on the GP2 are much less sensitive to CM noise than those on the GP3; therefore, it is preferred that the CM noise current primarily flows through the red plane to the input power connector at the high side. This is achieved by making the CM impedance of the GP2 dominated by a few nH trace inductances, whereas the CM impedance of the GP3 is determined by a few pF input-output capacitances of the isolated power supplies, the GDIC, and digital isolator (Diso). The CM impedance of the green path is considerably higher than the red. Hence, the major part of the CM noise current is now directed through the GP2 (power path) instead of the GP1. In this case, the sensitive processing signal circuits will be subjected to greatly reduced CM noises and protected from the malfunction of logic. For excellent electromagnetic compatibility, single-point low-impedance interconnections should be made between GP3 and GP2, either by a $0-\Omega$ resistor (or a short trace) across an isolated power supply, or a non-isolated power supply can simply be used. By implementing this, the signal isolation barrier (including GDIC and Diso) is leveraged, but no voltage stress is imposed to it.

### 3.3.4 Signal Architecture

The FPGA is the core of the developed enhanced gate-driver. The FPGA manages multiple functionalities such as GDIC programming, RSCS reset, analog/digital conversions (ADC), and communication to the controller and other GD units, as shown in Fig. 3.13. The output
signals from the Rogowski coils are processed by an operational amplifier (OpAmp) in the integrator configuration. After recovering the current, the signal is being used for 3 purposes: 1) shortcircuit (SC) protection with high bandwidth RC filtering, 2) for peak current mode (PCM) control, 3) sent to the FPGA through ADC for purposes of RSCS calibration or sending the current values to the controller. The SC signals from the 3 parallel switches are processed by a “OR” gate, and then fed to the gate driver IC (GDIC) via a Diso, and sent to the FPGA for a post-fault reaction if required. The GDIC will activate short-circuit protection immediately. For the PCM control (required for SCC), three current sensor outputs are first sent to the summation circuit, after which a signal is sent to the comparator. It is then compared with the value set by the control through the FPGA and then the DAC. The PCM signal is then sent to the FPGA for processing, and consequent switching actions. Furthermore, three current sensor outputs are fed to three ADC blocks via buffers. The ADC blocks sample the three switch currents as commanded by the FPGA for two purposes. The first purpose is the RSCS calibration with a digital potentiometer (DPOT) at the system
startup, eliminating the input offset error of the integrator OpAmp. The FPGA senses the off-state drift of OpAmp via the ADC and adjusts the resistance value of a DPOT until the value sensed by the ADC drops below a very low threshold (comprehensive study in Section 3.3.7). The second purpose is for control; in the sense that the GD knows the value of the current of the switch and can communicate it to the main controller. For communication with the controller and other GDs, 5 fiber-optic input/output terminals are dedicated. The FPGA initializes and configures the GDIC each time the board is powered on. There are many programmable options with the selected GDIC (STGAP1AS), some of which are desaturation (DeSat) protection threshold level, DeSat protection current source magnitude, SENSE pin threshold level, two level turn-off (2LTO) voltage levels and time duration, under/over voltage lockout protection management, deadtime, etc. Besides the above-mentioned tasks, the FPGA has an external clock (CLK), hardware programmable PWM (average mode, or PCM mode), and test points. Overall, 120 out of 150 FPGA I/Os have been used.

3.3.5 High-current driving system with minimized loop-inductance

Decoupling Capacitance Design

The design of the decoupling (or bypass) capacitance is one of the crucial steps, since it directly provides the gate current to drive the gate of the SiC MOSFET device and is dedicated to stabilizing the driving voltages. If this capacitance has too low of a value, it can compromise the successful operation of the device during transitions. These capacitors must be placed close, preferably directly across the bias and reference connection of the gate-driver. Two current components that are supplied by those bypass capacitors should be considered according to [182]. The first one is called the quiescent current during the fully
on and off states of the device. Even though the driver’s quiescent current is higher when its input is driven high, this current is extremely low for MOSFET applications, so it can be omitted. The second one is the ripple component of the gate current happening at the transitions. The voltage ripple across the bypass capacitors can be determined based on the value of the gate charge of the semiconductor device (3.1):

\[ \Delta V_{CC} = \frac{Q_{g,\text{tot}}}{C_{\text{dec}}} \]  

where \( \Delta V_{CC} \) is change in supply voltage, \( Q_{g,\text{tot}} \) is total gate charge, and \( C_{\text{dec}} \) is the bypass capacitor value. At the turn-on, this charge is transferred from the bypass capacitors to the SiC MOSFET input capacitances. Accordingly, the minimum bypass capacitor value for a tolerable ripple voltage (\( \Delta V_{CC,\text{max}} \)) can be found by using (3.2)

\[ C_{\text{dec, min}} = \frac{Q_{g,\text{tot}}}{\Delta V_{CC,\text{max}}}. \]  

Since the datasheet values of \( Q_{g,\text{tot}} \) are not known, and the curve-tracer in the current configuration cannot perform these tests, \( Q_{g,\text{tot}} \) will be estimated through the known passive parameters of \( C_{\text{iss}} \) and \( C_{\text{rss}} \) capacitance. The principle on how to estimate the gate charge through the MOSFET capacitances is shown in detail in [183] and summarized here in Fig. 3.14.

Based on (3.3) given in Fig. 3.14 and combining it with the parasitic capacitor curve tracer results shown in Fig. 3.7, it can be estimated that the total gate charge (combined charges from region 1-3) is \( Q_{g,\text{tot}} \approx 5.5 \, \mu\text{C} \).
The conditions on which $Q_{g,\text{tot}}$ is calculated is $V_{dc} = 6\, \text{kV}$, $I_d = 120\, \text{A}$, $V_{CC} = 20\, \text{V}$. The Miller plateau voltage $V_{\text{plateau}}$ is estimated based on (3.5) from [182]

$$V_{\text{plateau}} = V_{th} + \frac{I_d}{g_{fs}} \tag{3.4}$$

where $V_{th} = 4.58\, \text{V}$ is the worst case threshold voltage @ 175°C from Fig. 3.8, and $g_{fs} \approx 40\, \text{S}$ is the peak transconductance at @ 175°C, as seen in Fig. 3.6.

Therefore, based on (3.2) and the imposed requirement $\Delta V_{CC,\text{max}} = 0.05\, \text{V}$, the calculated minimum bypass capacitance is $C_{\text{dec, min}} = 110\, \mu\text{F}$. It is well known that in ceramic capacitors (in this case X7R), the capacitance may differ from the rated value when a DC voltage is
applied. The larger the DC voltage applied to the high dielectric constant capacitors, the more the effective capacitance is reduced. The rule of thumb dictates that ceramic capacitors DC bias characteristics can de-rate up to 50%. For the chosen ceramic capacitor X7R, 35 V, package case 1206, valued at 10 $\mu$F with part number C3216X7R1V106K160AC, 24 of them will be put in parallel, giving a total $C_{dec} = 240 \mu$F.

Additionally, with knowing $Q_{g,tot} \approx 5.5 \mu$C, the power dissipation (the gate charge losses) can be calculated based on (3.5)

$$P_{Q_g} = Q_{g,tot}V_{drv}f_s \approx 15.4 \text{ W}$$

for the $V_{drv} = 28 \text{ V}$, which is the maximum voltage from negative to positive driving the voltage rail, and $f_s = 100 \text{ kHz}$ is the maximum switching frequency. The power dissipation does not depend on time, or how quickly the charge is delivered to the gate. This power to drive the SiC MOSFET is dissipated in the gate drive circuitry on the components identified as the combination of the ohmic impedances in series in the path according to their resistance ratio. At every switching cycle, the gate charge passes through the driver chip output impedance, the external gate resistor, and the internal gate resistance. The designed booster and gate resistors have to be able to sustain this power.

**Current Booster Design**

The gate loop inductance is required to be very low in order to minimize gate oscillations and high impedance at high frequencies. Such a design ensures that high frequency gate current required to drive the device fast will not be compromised. The STMicro STGAP1AS is the main gate driver IC. This driver IC is not able to provide the required 90 A driving current for the three paralleled submodules. Therefore, an external current booster stage is
designed to supply this peak current, ensuring an extremely fast switching transient. Since the solution proposed in [160] is applicable to drive paralleled SiC MOSFET modules, the design in this dissertation follows that one. A solution with nine (3x3) paralleled bipolar junction transistors (BJT) cells was designed as shown in Fig. 3.15 (a) to drive the three paralleled submodules. \( R_b \) is used to limit the input current to driving the BJT transistors, to eliminate the impact of the mismatched current gain \( \beta \), and to improve the current sharing between the three paralleled booster stages for one submodule. \( R_b \) should be chosen in such a way that it is low enough to mitigate the \( \beta \) mismatch impact and high enough to limit the high base currents and overheating. Additionally, \( R_{com} \) is used to balance the current sharing of the nine current booster channels. The three driving channels are connected jointly at the common junction "COM" to guarantee the three driving voltages are the same, ensuring synchronous driving of the paralleled devices. \( R_{g,ext1} \) and \( R_{g,ext2} \) are driving gate resistors designed in split fashion to mitigate the resonance between the three paralleled gate loops. \( R_{g,ext1} \) determines the turn-on speed, while if the diode is soldered, \( R_{g,ext1} \) and \( R_{g,ext2} \) jointly

Figure 3.15: (a) Paralleled current booster circuit block diagram for three submodules, (b) PCB layout to minimize the gate-loop inductance with cross-sectional view of the PCB layout, top view of the PCB layout, and bottom view of the PCB layout.
determine the turn-off speed. From now until the end, the diode is not included in the circuit, and $R_{g,\text{ext}}$ refers to the external gate resistor used for both turn-on and turn-off. These gate resistors, decoupling capacitors $C_{\text{dec}}$, and transistor chip T1&2 (including T1 and T2) are placed back-to-back to minimize the gate-loop inductance, as shown in Fig. 3.15(b) [160]. Furthermore, in order to keep the turn-on and turn-off gate-loop inductance extremely low, GDIC out, ”COM”, gate connection, and kelvin-source are all planes rather than the traces. Three current-booster banks are placed in a wide area adjacent to a MCX gate/source connector.

The low inductance driving loop is verified in Fig. 3.16(a). The external gate-loop impedance $Z_{g,\text{ext}}$ is measured across “g” and “s”. Since the impedance analyzer does not work with semiconductor components, they are replaced by two 0-Ω SMD 0603 resistors because of their comparable footprint and parasitic inductance. The turn-on and turn-off gate loop inductance was below 5 nH for all three submodules S1, S2, and S3, respectively.

![Figure 3.16](image_url)

**Figure 3.16:** (a) External gate-loop impedance $Z_{g,\text{ext}}$ comparison for 3 submodules with populated $R_b = 5 \Omega$, $R_{\text{com}} = 0.3 \Omega$, $R_{g,\text{ext},\text{S1}} = R_{g,\text{ext},\text{S2}} = R_{g,\text{ext},\text{S3}} = 0.33 \Omega$, and $C_{\text{dec}} = 240 \mu F$. Measured by Agilent 4294 A. (b) Current sharing of three current booster banks for three submodules. (c) Zoom in of waveforms of the same experiment. [Probes] Low-voltage passive probes TPP1000 @ 1GHz.
Regarding the gate current sharing of the three submodules, which is the first step in ensuring synchronous driving of the paralleled devices, results can be seen in Fig. 3.16 (b) and Fig. 3.16 (c). The gate driving currents of submodules S1, S2, and S3 have been obtained by measuring the voltages across the three gate resistors $R_{g,ext,Sx}$ using passive probes. Very little mismatch can be observed (less than 1%), and it can be said that the three gate currents are overlapping with each-other, giving the total turn-on current peak of 36 A, and the total turn-off peak current of 48 A (for the mismatched $R_{g,ext,1}$, and $R_{g,ext,2}$).

**Active Miller Clamping**

In the phase-leg configuration, cross-talk interference becomes more serious with increased $dv/dt$ rates of SiC. With complementary device switching transients, current $i_{rss}$ injected into the device gate through the Miller capacitance $C_{rss}$, according to (3.6)

$$i_{rss} = C_{rss} \cdot \frac{dv_{ds}}{dt}$$

(3.6)

and causes a possible rise of $v_{gs}$ due to the presence of $R_{g,ttl} = R_{g,int} + R_{g,ext}$, as discussed in [184]

$$\Delta V_{gs} = R_{g,ttl} \cdot i_{rss} \cdot (1 - e^{-\frac{t_{slp}}{\tau}})$$

(3.7)

where the time constant is $\tau = R_{g,ttl}C_{iss}$, $t_{slp}$ is the rise/fall time of $v_{ds}$, $R_{g,ttl}$ is total gate resistance consisting of external $R_{g,ext}$ and internal $R_{g,int}$ gate resistance ($R_{g,int} = 0.11 \Omega = \frac{2\Omega (R_{g,int,die})}{18}$).

According to estimated $C_{rss} = 0.2 \text{ nF}$, under $dv/dt = 100 \text{ V/ns}$, there will be 20 A injected into the gate of device S2 during turn-on of S1, which in combination with the assumed $R_{g,ttl} = 1 \Omega$, $t_{slp} = 60 \text{ ns}$ will create $\Delta V_{gs,s2} \approx 9.73 \text{ V}$. $\Delta V_{gs,s2}$ this high, combined with the characterized gate threshold voltage distributed between $3.3 \text{ V@175°C} - 4.6 \text{ V@25°C}$, will
create possible shoot-through current, which will eventually be fatal to the system due to significant switching losses and enormous dissipated heat. For the turn-off event of S1, a negative $\Delta V_{gs,2} \approx 6.5 \text{ V} @ \left[ \frac{dv}{dt} = 40 \text{ V/ns} \& t_{slp} = 150 \text{ ns} \right]$ would be induced, leading to gate oxide over-stress and accelerated degradation if the maximum allowable negative-biased gate voltage is exceeded. This implies that Miller-clamping circuitry is essential on the GD for a successful operation. Furthermore, with the increase of current and temperature in the system, $\frac{dv}{dt}$ for both turn-on and turn-off are becoming faster (confirmed through dynamic characterization in Section 3.4), further implying that Miller-clamping circuitry is essential for successful device operation.

An active Miller clamp (AMC) provides a low-impedance path to sink the current. It gets active when the device turns off (gate voltage $< V_{th}$), bypassing the gate $\frac{dv}{dt}$ current to negative rail, and the design is shown in Fig. 3.17 (a) More details about the circuit can be found in [15, 159]. Here, parameters chosen are $R_{AMC} = 100 \\Omega$ and $C_{AMC} = 1 \text{ nF}$ based on the parameter sweep shown in Fig. 3.17 (b).

![Figure 3.17: Active Miller Clamping. (a) Circuit. (b) Performance of AMC from gate voltage perspective with parameter sweep.](image_url)

The cross-talk influence and performance of the AMC will be evaluated in Chapter 4.
3.3.6 Rogowski Switch-Current Sensor

Due to its excellent performance as both a short-circuit detector and current sensor for control [159], RSCS will be employed. It will serve on a 10 kV eGD as a short-circuit detection mechanism, a peak-current-mode control sensor, and as a phase-current sensor, by sampling the switch current with an analog-to-digital converter (ADC) and sending it to the local FPGA, and later the controller, through a communication protocol. Each switch position requires 3 current sensors (3 submodules paralleled) or a total of 6 RSCS per power-cell that will be designed. First, the fundamentals will be explained for only 1 RSCS.

Fundamentals

The switch-current sensor is composed of a Rogowski coil and a signal processing circuit (Fig. 3.18). The Rogowski coil consists of a helical coil of wire with the lead from one end returning through the centre of the coil to the other, ending at the same end. The coil is wrapped around the straight conductor (sensed busbar) whose current is to be measured. The signal processing circuit is comprised mainly of an integrator circuit and a reset switch. The voltage induced at the output of the Rogowski coil, according to the lumped coil model,
can be found in the transfer function (3.8),

$$\frac{V_{in}}{i_d} = \frac{sM}{s^2 L_s C_s + s \left( \frac{L_s}{R_d} + C_s R_s \right) + \left( 1 + \frac{R_s}{R_d} \right)}$$

where $L_s$ is coil inductance, $M$ is the mutual inductance, $C_s$ is coil self-capacitance, $R_s$ is the coil resistance, while the $R_d$ is the damping resistor. In most cases, the load effects of the self-inductance and self-capacitance (self-resonance effect of the sensor) are negligible until very high frequencies $\geq 60$ MHz occur. This is considered sufficient during the RSCS design process because the switching oscillation frequency for the chosen SiC MOSFET module is predicted to be much less than that. Therefore, the following approximation holds: the Rogowski coil voltage is proportional to the $di_d/dt$ of the sensed current, scaled by a factor of the mutual inductance, as shown in

$$V_{in} = M \frac{di_d}{dt}$$

(3.9)

The integrator is employed with the coil to convert the $di_d/dt$ to the voltage containing the current information, described with

$$V_{out} = \frac{1}{R_{i1} C_f} \int V_{in} dt = G_{rscs} i_d + V_{err}$$

(3.10)

where $R_{i1}$ and $C_f$ are integrator resistance and capacitance, respectively, $V_{err}$ is the accumulated integration error, $G_{rscs} = \frac{M}{R_{i1} C_f}$ is sensor gain, and $M$ is the mutual inductance between the Rogowski coil and sensed busbar.

An active integrator is employed instead of a passive RC integrator, to reduce the low-frequency bandwidth and extend the coil measurement range [185].
Two fundamental issues in this configuration contribute to the $V_{\text{err}}$; both are related to the non-idealities of the integrator circuit. This error must be eliminated in order to sense the correct switch current values. First, the sensor’s dc gain decays from its initial value at a time constant $\tau = R_f C_f$ and eventually into zero [160]. This problem is solved with an active reset switch employed with an integrator, controlled with $S_{\text{rst}}$, which has $R_{\text{rst,on}} = 6.25 \Omega$. The active reset switch resets the output to zero when the SiC MOSFET is switched off, thus avoiding the drifting of the sensor. The reset switch is active for only 200 ns, which is sufficient time for the chosen integrator capacitor $C_i$ to discharge, according to (3.11) and (3.12) where $V_{0,\text{max}} = \pm 5 \text{V}$:

$$V(t) = V_0 e^{-t/\tau}, \quad (3.11)$$

$$\tau = R_{\text{rst,on}} C_i = 12.5 \text{ ns}. \quad (3.12)$$

The second issue is related to the impact of the input offset voltage $V_{os}$ and input bias current $I_B$. For example, when $V_{\text{in}} = 0 \text{V}$ and $S_{\text{rst}} = 1$, the reset is open (integrator operates), giving an output of

$$V_{\text{out}} \approx \left( \frac{R_f}{R_{i1}} V_{os} + I_B R_f \right) (1 - e^{-t/\tau}) \quad (3.13)$$

where $R_f >> R_{i1}$, which in practice is always true. Basically, the sensor output is drifting and can lead to severe inaccuracies or even saturation of the OpAmp. To solve that issue, an offset compensation circuit (offset trimming) is implemented to reduce the output error by injecting a small offset voltage into the non-inverting input by means of an analog potentiometer and voltage divider, as shown in Fig. 3.18 (b), [186]. The resistor $R_{i2}$ plays a crucial role, where it is selected as $R_{i2} = R_f || R_{i1} \approx R_{i1}$ in order to eliminate the impact of bias current. Further, voltage on the resistor $R_{i2}$

$$V_{R_{i2}} = \frac{R_{i2}}{R_3 + R_{i2}} V_{\text{APOT}} \quad (3.14)$$
is used to eliminate the input offset voltage.

Eventually, the switch current sensor can sense pulsating current with correct amplitude and high accuracy. The output voltage of the integrator is filtered with the 28.3 MHz high frequency RC filter. This sensed current can be used for protection and peak-current mode (PCM) control (high BW loop), as well as for phase current control through the controller (low BW loop). High bandwidth sensed current is being sent to the comparator without introducing any blanking time, allowing ultra-fast short-circuit detection and protection. Low bandwidth current information (filtered with a cutoff frequency of 2.1 MHz to eliminate high frequency ringing during switching instances), is sent through a level shifter to a high precision 12 bit ADC with a sample rate of 2.5 Msps communicating with the FPGA, which can potentially do the switch current reconstruction by summing the three submodule currents and sending that information to the main controller for phase current control.

Current sensing architecture for the complete switch is in Fig. 3.19. As indicated, the current sensing system can be used for the following:

1. Protection - a fast short-circuit detection system able to detect short-circuits below 86 ns.

2. System level phase-current control - sampling the switch current during the conduction period with an ADC and sending it to the local FPGA. In FPGA, digital summation is performed through the communication protocol, and that information is then given to the controller,

3. Peak-current-mode control sensor - finds utilization in the SCC (or any other peak current mode control operated converter).
Rogowski Coil Board Design

The PCB-integrated Rogowski coil design procedure is heavily discussed in [160, 187]; therefore, fewer details will be shown here. Regarding the top switch, for the PCB-embedded RSCS, an anticipated shield (screen) that is a necessity against \( \frac{dv}{dt} \), is previously proposed; however, it is not experimentally proven. Therefore, one of the later objectives of the power-cell characterization will be to evaluate the performance of un-shielded and shielded Rogowski coils (shown in detail in Section 4.4.5). To that end, two versions will be produced.

The printed circuit board (PCB) Rogowski coil board, located between the XHV-6 module and busbar, senses the current of each submodule switch. The first step in the design that should be carefully analyzed is the external insulation, or E-field distribution in the air that will be encircled by the Rogowski coils. It can possibly violate the voltage distribution intended by the device manufacturer, by introducing source potential directly around the drain terminal of the device. Therefore, the interconnection among the power module,
laminated bus, copper bars, and PCB Rogowski coil sensing board is one of the critical design pieces to ensure a successful operation at the rated voltage, due to different voltage potentials along all of the metal parts and limited space. The E-field intensity in the air around such interconnection regions can be high, which can be enough for initiating tremendous PD.

The potential design of the 3D top view of the assembly (Rogowski coil board, module, ac-bar) is shown in Fig. 3.20 (a).

Figure 3.20: Critical air gaps interconnection among power module, laminated bus, copper bars and PCB Rogowski coil sensing board. (a) Top 3D view of the structure. (b) Critical air gaps and possible geometrical adjustments. (c) Iterative design process.

The E-field intensity in the air window between the positive DC interconnector and its adjacent Rogowski coil should be analyzed when the bottom device is on. By comparison, if the top device is on, the critical design region in the air would be along the output connector edges, which are towards the negative DC terminals. The critical regions for the external
insulation design in this assembly can be further demonstrated in Fig. 3.20 (b). Geometrical based methods should be applied in order to adjust the E-field distribution in such areas. As indicated in Fig. 3.20 (b), with the pink rectangle, two dimensions X and Y should be further explored to manage the maximum E-field intensity in air. For the worst case consideration, the potential on positive terminals is 10 kV, while negative terminals are at 0 kV. Fig. 3.20 (c) shows the iterative process of the Rogowski coil and spacer/interconnector design. First, FEA analysis showed that the distances of 6 mm and 8 mm have been selected for X and Y individually. The reason is that the field between the coil and interconector will be less than 2 kV/mm. Additionally, it is shown that smoothing the edges of the interconector further reduces the field in the window to acceptable values. Second, the distance between the Rogowski board and the power module is selected as 6 mm based on previous FEA simulation results. Moreover, an asymmetric design has been applied to the power module AC terminal connectors [188].

The coils and complete interconnection structure are verified to be PD-free for the intended rated voltage operation (6 kV). The results and testing methodology are shown in Section 4.3.3.

The second step is the layout design of both the un-shielded and shielded Rogowski coils, shown in Fig. 3.21, designed on a 6-layer PCB and 8-layer structure, respectively. To further enhance the insulation design, the complete coils (and shield) are embedded in the inner layers of the PCB, eliminating creepage paths between the HV primary-side conductor and the secondary-side coil. The uniform winding distance and the high turn number are required to increase the sensitivity of the sensor (the mutual inductance M). Accordingly, 202 turns of windings have been designed, maximizing the turn number in the PCB for the predefined area that can be achieved by regular PCB fabrication techniques. The winding height is limited by the PCB thickness. The windings are designed in four internal layers. In the
Figure 3.21: Un-shielded Rogowski coil design. (a) Layout and PCB board layer stack. (b) Complete board with 6 coils. Shielded Rogowski coil design. (c) Layout and PCB board layer stack. (d) Complete board with 6 coils.
case of the un-shielded version, the second and the fifth layers are used to construct the multi-turn winding, and the third and the fourth layers are used to form the single-turn compensation winding. In the case of the shielded version, the coils are buried one more level in, while the second and seventh layers are used to construct the shield which is only connected in one point. The single ended buried vias go from the second and seventh layer to form a shield wall without creating eddy current loops.

3.3.7 Rogowski Switch-Current Sensor Self-Calibration

Previous Calibration Solution

Implementing an offset compensation circuit to reduce output errors in the integrator output by injecting a small offset voltage into the non-inverting input, by means of an analog potentiometer and voltage divider (shown in Fig. 3.18), is not desired. The reasons are performance related concerns with the potentiometer due to temperature swings and vibrations. This often requires new adjustments since $V_{os}$ is temperature dependent. For the intended application of MMC where a single power-cell has 6 RSCS, this potential problem would require a great amount of effort to re-tune every time conditions change, basically making it impractical. Furthermore, the mechanical parts, wiper oxidation, aging, and wear raise reliability concerns over time and can possibly reduce the usable lifetime.

Proposed Solution

Generally, electrical parts are more reliable and have a longer lifetime than mechanical; therefore, a simple change would be to incorporate a digital potentiometer instead of an analog. However, this solution requires programming. On the gate driver that is being developed, the requirements of fast computing, sampling current, and communication will
be handled with the FPGA. Therefore, this solution seems viable [189].

![Diagram](image)

**Figure 3.22**: Rogowski switch-current sensor. (a) Fundamentals and digital offset calibration. (b) Waveforms of implemented digital offset calibration.

Fig. 3.22 (a) shows the proposed calibration circuit with the ADC, FPGA, DPOT, and waveforms. The principle will be explained for one RSCS out of the three integrated on the GD at the power up stage (which can also be requested by the main controller), while a complete current sensing diagram will be shown later. Since the system is in start-up sequence, there will be no current through the switch; therefore, $V_{in} = 0\, V$. During the calibration procedure, the PWM signal is kept low until all 3 RSCSs are calibrated (offset compensated).

Fig. 3.22 (b) shows the waveforms of the implemented digital offset calibration. The reset sequence is initiated by controlling $S_{rst}$ with certain frequency and on time. In this case, we can assume $f_{S_{rst}} = 10\, kHz$ while the integrator is turned-on and integrating for $t_{on,S_{rst}} = 95\, \mu s$ and turned-off for $t_{off,S_{rst}} = 5\, \mu s$. At this stage, $V_{os}$ (assumed to be positive) is not compensated due to the integration effect on the output. We will see the ramp increasing until the reset occurs $S_{rst} = 0$. If there is no reset, this ramp would continue until $V_{out} \approx R_f/R_{i1}V_{os}$ or saturation of OpAmp. Towards the end of the period when $S_{rst} = 1$, the integration error will be at the highest, giving better resolution and ultimately better compensation results for higher turn on-times (or frequencies). If the sampled value of the $V_{out}$ is higher than
the maximum allowable error, the FPGA will reconfigure the digital potentiometer (DPOT) in a way that the voltage on $V_{R_{i2}}$ is lower, opposing the $V_{os}$, thus reducing its influence in the next reset cycle. This process will be repeated until the $V_{out}$ becomes smaller than the maximum allowable error ($\Delta \epsilon$). After the FPGA determines that the calibration is done for all 3 RSCS, the GD can be used for the normal operation of driving the switch and measuring currents with high bandwidth and correct amplitude without the drifting caused by non-idealities of OpAmp. This approach, called the linear or fixed step approach, exhibits relatively slow dynamics compared to other approaches such as sectional steps (high step with large errors and small step with lower errors), or a solution with the PI controller that has the best dynamics and can possibly reduce the time of self calibration.

**Utilized Hardware Components**

The self-calibration accuracy of the RSCS may be affected adversely due to the availability of today’s DPOT resolutions, which can present a challenge since the DPOT’s resolution dictates how fine the offset can be trimmed. Therefore, special attention has to be dedicated to hardware selection and is presented here to explain in detail, the limitation of the approach with the selected components.

First, from previous research on RSCS, the OpAmp TI LM7372 is selected with $R_{i1} = 50\Omega$ and $C_f = 2\,\text{nF}$. This OpAmp has a typical offset voltage of $V_{os} = \pm 2.2\,\text{mV}$, while the maximum can be $V_{os,\text{max}} = \pm 10\,\text{mV}$. Incorporating the temperature dependence of the voltage offset, the real maximum one is $V_{os,\text{max}} = \pm 12.28\,\text{mV}$, since $\pm 12\,\mu\text{V/°C}$ is the offset voltage temperature dependence for the temperature range of $-40\,\text{°C}$–$150\,\text{°C}$. Self-calibration must eliminate that offset in all cases. The selected FPGA is the one from the Intel Altera MAX10 series. Second, the ADC selected is a 12 bit, high speed, Linear Technology LTC2315-12 with an input range from 0-4.096 V, implying resolution of $V_{\text{res}}^{\text{adc}} = \ldots$
1 mV. Third, the DPOT from Analog Devices AD5260 is selected. It is 8 bits, being supplied with ±4.5 V rails, meaning that its voltage step at the output is $\Delta V_{\text{step}} \approx 35.2 \text{ mV}$. The voltage step of the DPOT is much higher than the range of offsets; thus, in the fourth step, the voltage divider has to be employed for fine tuning. To eliminate the impact of bias currents, $R_{i2} = R_{i1} = 50 \, \Omega$. $R_3$ is selected such that it satisfies the following inequality

$$\frac{R_{i2}}{R_3 + R_{i2}} \cdot \Delta V_{\text{step}} \cdot 256 \geq 24.56 \, \text{mV}$$  \hspace{1cm} (3.15)

where 256 is the number of taps of the DPOT (8 bit), and 24.56 mV is ±12.28 mV is the range of offset voltage. According to that, $R_3 \leq 18.29 \, k\Omega$. Thus, selected is the E96 standard resistor closest to 18.29 kΩ, which is $R_3 = 17.8 \, k\Omega$, to fully utilize the range and have high resolution so even the smallest offsets can be trimmed. According to that, $V^\text{max}_{R_{i2}} = \pm 12.62 \, \text{mV}$ with a resolution of $\Delta V_{R_{i2}} = \pm 98.6 \, \mu\text{V}$. The maximum time of the self-calibration is defined with

$$t_{\text{calib,max}} = \frac{256}{2} \cdot (t_{\text{on},S_{\text{rst}}} + t_{\text{off},S_{\text{rst}}}) \cdot \frac{V_{\text{os,max}}}{V^\text{max}_{R_{i2}}}.$$ \hspace{1cm} (3.16)

**Self-calibration Algorithm**

Before going into the details of self-calibration, the FPGA Finite State Machine (FSM) is shown in Fig. 3.23. In the system reset state (virtual reset), after programming the FPGA from internal memory, a 1.25 ms delay is implemented before the code starts executing. In the FPGA power-up stage, there is an additional delay of 1.25 ms for the rest of the voltages in the system to reach their intended values. In the GDIC Configuration stage, the FPGA programs the gate-driver IC with pre-loaded settings through SPI communication (e.g., two-level turn-off voltage level and time duration, SC protection level, active Miller clamping,
etc.). In the RSCS Calibration stage, the automatic calibration of the three Rogowski switch-current sensors is executed with an initial delay of 25 ms until the voltages of the decoupling capacitors for the OpAmp finish charging. Once the calibration stage is finalized, the FPGA enters the FPGA BUSY stage in which all main controller commands will be executed such as current sensing, PWM, peak-current mode control, resetting of sensor, etc. From this state, the state can change to go either in 1) FPGA Fault state - if there is any fault coming from GDIC and remaining in this state until the fault is cleared, after which it goes to FPGA Power-up, or 2) RSCS Calibration stage - if requested by the main controller.

![Simplified FPGA finite state machine.](image)

**Figure 3.23:** Simplified FPGA finite state machine.

The RSCS Calibration algorithm is shown in Fig. 3.24. The self-calibration piece is explained for 1 out of 3 RSCSs, since it is completely symmetrical. The first step consists of the initialization of the self-calibration. The maximum error with which sampled $V_{\text{out}}$ will be compared is defined to be $\Delta \epsilon_{\text{max}} = \pm 50 \text{ mV}$, which roughly corresponds to $\Delta I_d \approx 2.5 \text{ A}$. As stated previously, the reset frequency set to be 10 kHz with an integration time of $t_{\text{on}} = 95 \mu\text{s}$, do observe higher values of integration error. The ADC will sample $V_{\text{out}}$ at a time of $t = 94 \mu\text{s}$.

In the second step, $S_{\text{rst}}$ pulse is initiated, and after which, the first decision block arrives. If the calibration of S1 (or S2 or S3) is already finished, that particular RSCS calibration is skipped. However, if it is not, the output is sampled with ADC which is at the start of
the third step. After that instance, the sampled value is checked against both $\Delta \epsilon_{\text{max}}$ and $\Delta \epsilon_{\text{min}}$. Both are necessary since the offset can be both positive and negative. If, for example, $V_{\text{out},S1} \geq \Delta \epsilon_{\text{max}}$, then the voltage on the $V_{R_{i2}}$ has to be decreased. To achieve this, the voltage output of the DPOT now has to reduce by $\Delta V_{\text{step}}$:

$$V_{\text{DPOT},S1} = V_{\text{DPOT},S1} - \Delta V_{\text{step}}.$$  \hfill (3.17)

After that, the DPOT is activated to execute the task. This process continues until the output voltage falls into the range of $V_{\text{out},x} \in [\Delta \epsilon_{\text{min}} - \Delta \epsilon_{\text{max}}]$, where $x$ can be S1, S2, and S3, (all three of the RSCS on the gate driver).

**Experimental Verification**

Before going into the experimental verification of the self-calibration, note the final current sensing architecture shown in Fig. 3.25 incorporates the feedback loop for the self-calibration.
of the RSCS.

**Figure 3.25:** Current sensing architecture for 3 switch currents in parallel with digital potentiometer as a part of self-calibration methodology, integrated on a single enhanced gate-driver.

Now, the self-calibration experimental verification will be shown on a novel gate driver, whose prototype will be introduced in the next subsection. Fig. 3.26 (a) shows the start-up of the GD. Before the calibration stage, there exists a brief period of time where the FPGA is not operational since the voltage is less than 3.3 V: the FPGA programming stage, system reset stage, FPGA power-up stage and GDIC configuration stage. After the calibration is finished, the FPGA enters the FPGA_BUSY stage, where the PWM output can now change its state based on the signal coming from the controller. Fig. 3.26 (b) shows the zoomed-in waveforms during the self-calibration stage at the startup of the GD. The analog measurement consists of a yellow waveform which is the RSCSs $S_{rst}$ signal, cyan is $V_{out,S1}$, pink is $V_{out,S2}$, and green is $V_{out,S3}$. The digital measurement consists of measured signals from self-calibration algorithms that were put on the FPGA testing points. They are as follows: S1_done, S2_done, and S3_done which are the indicators of when the calibration is done for the RSCS of S1, S2, and S3, respectively. Calib_done is the indicator when
complete calibration is performed, and the PWM is the switch driving signal going to the GDIC from the controller. Once RSCS self-calibration starts, $\overline{S_{rst}}$ is initiated and $V_{out,s1(S2,S3)}$ is getting sampled and compared with $\Delta \epsilon_{\text{max}}$ and $\Delta \epsilon_{\text{min}}$. Once each $V_{out}$ falls into the range of $[\Delta \epsilon_{\text{min}} - \Delta \epsilon_{\text{max}}]$, then signal $Sx_{\text{done}}$ is generated and calibration for that sensor is done, while others are still calibrating. In this case, the first sensor to finish is S3, followed by S2, and then S1. Upon finishing, the calib_done signal is generated which allows the FPGA to exit the calibration state of the FSM. The total self-calibration time was $t_{\text{calib}} = 4.6 \text{ ms}$.

![Image](image.png)

**Figure 3.26:** Self-calibration experimental results (a) at startup of GD, and (b) zoomed-in view on calibration stage. [Probes] Ch1 - Ch4: TPP1000 @1 GHz. D0 - D4: P6616 Logic Probe. [Time scale]: 5 ms/div.

### 3.3.8 Gate-Driven Prototype

The enhanced GD prototype for both switches for the 10 kV half-bridge XHV6 SiC MOSFET module with the indicated dimensions and important constitutive parts is shown in Fig. 3.27.

Some of the most important aspects of the enhanced GD are summarized in Table 3.1.

The designed GD operation will be verified in Section 3.4 in the double pulse test and in the continuous operation in subsection 4.4.2. Additionally, it will be verified for active Miller clamping effectiveness and characterized for the CM noise current influence on the top gate.
driver in subsection 4.4.3. Furthermore, RSCS accuracy for both the top and bottom switch in the half-bridge will be assessed in subsection 4.4.5.

### 3.4 High-Voltage SiC MOSFET Device Dynamic Characterization

Compared to the Si IGBT, the SiC MOSFET's inherent fast switching speed characteristics and small losses make it the preferred choice for a high switching frequency, high power density application. However, this fast switching speed poses significant challenges EMI-wise to design engineers, due to its very high $dv/dt$ and $di/dt$. This makes them crucial parameters during the design stages [190]. To fully investigate the benefits brought by the SiC MOSFET, dynamic characterization will be performed.
Table 3.1: 10 kV Enhanced Gate-Driven Specifications

<table>
<thead>
<tr>
<th>Property</th>
<th>Minimum</th>
<th>Maximum</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>20 V</td>
<td>30 V</td>
</tr>
<tr>
<td>Driving voltage range</td>
<td>−8 V</td>
<td>22 V</td>
</tr>
<tr>
<td>Embedded switch current measurement</td>
<td>−150 A</td>
<td>150 A</td>
</tr>
<tr>
<td>Driving current</td>
<td>±5.6 A</td>
<td>±90 A</td>
</tr>
<tr>
<td>Switching frequency</td>
<td>-</td>
<td>100 kHz</td>
</tr>
<tr>
<td>CM transient immunity</td>
<td>-</td>
<td>≥100 V/ns</td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>-</td>
<td>≥10 kV</td>
</tr>
<tr>
<td>Configurable short-circuit threshold</td>
<td>100 A</td>
<td>250 A</td>
</tr>
<tr>
<td>Short-circuit detection time</td>
<td>-</td>
<td>80 ns</td>
</tr>
<tr>
<td>Configurable two-level turn-off</td>
<td>7 V, 500 ns</td>
<td>10 V, 3000 ns</td>
</tr>
<tr>
<td>Propagation delay</td>
<td>-</td>
<td>110 ns</td>
</tr>
<tr>
<td>Active Miller clamp</td>
<td>5 A</td>
<td>20 A</td>
</tr>
<tr>
<td>Under voltage lock-out protection</td>
<td>11 V</td>
<td>15 V</td>
</tr>
</tbody>
</table>

Historically, the double-pulse-test (DPT) with inductive load is used for the characterization of high power devices such as Si IGBT or SiC transistors. The DPT can mimic converter behavior, and at the same time offers better insight into the device under test (DUT) by having a simple design, optimized layout, and designed space for measurement [191]. Moreover, the DPT excludes the self-heating problem since the DUT only switches four times (two times for recording), making the analysis independent of the junction temperature. The DPT will provide and quantify the switching performance of the SiC MOSFET, thus providing the basis and insights for converter design, such as switching speed, frequency, dead-time, efficiency estimation, and thermal management.

3.4.1 Equipment and Procedure

The DPT is a dynamic testing mechanism where two pulses are sent to the DUT in a clamped inductive circuit, as indicated in Fig. 3.28(a). With the regulation of dc-bus voltage and pulse duration, switching transients can be captured at any desired condition (different
voltages and currents), at the end of the first pulse and the beginning of the second pulse, as shown in Fig. 3.28(b).

The DPT assembly includes a dc capacitor bank, gate-driver circuits, power devices, dc voltage supply, load inductor, and probes. As can be seen from Fig. 3.28(a), there is no additional freewheeling diode used for device dynamic characterization. The used diode is the body diode of the upper switch in the half-bridge module to incorporate all effects that can occur in the module. The experimental setup is placed in the room temperature environment, while only the heatsink and SiC MOSFET are heated by a hotplate, controlling the junction temperature externally to study the temperature-dependent switching characteristics. The baseplate temperature is measured, and the junction temperature is assumed to be similar, since there will be no additional heating from the test itself. An electrically isolated, thermal conductive sheet is placed between the hotplate and baseplate since the baseplate will be on the dc-bus midpoint. The function generator and fiber optic board will be utilized to send
control signals and the TDK Lambda capacitor charger to provide power.

The drain-to-source voltage $V_{ds}$ was measured by the high-voltage differential probe THDP0100. Even though Rogowski coils (RC) are not ideal for the switch current measurement due to lower bandwidth [192] and possible CM related issues [193], the currents of the three submodules were measured by the three current probes PEM Ultra Mini Rogowski coil (RC) probe, CWT06. The chosen probes have 30 MHz bandwidth (high enough based on [75]) and are placed around the source of the device, which is at the same potential as the oscilloscope. This prevents the flow of CM currents since $dV/dt$ does not exist. Since $V_{gs}$ is not being measured, due to scope channel limitations, the device turn-on and turn-off delay will be excluded from the dynamic characterization, thus discussion.

### 3.4.2 Experimental Results

Double-pulse-tests are performed at the dc-link voltage of 6 kV, sweeping currents from 20 A–120 A and temperature from 25 °C–125 °C, to obtain switching results. The turn-on and turn-off external gate resistance $R_{g,ext}$ was varied from $0.66 - 1.33 \, \Omega$. The switching parameters discussed are the switching losses, $dv/dt$, $di/dt$, switching times, and current sharing between submodules. These parameters are necessary for the cooling system design, noise-immunity, and insulation design for a high-voltage power-converter design. A typical DPT waveform is shown in Fig. 3.29.

#### Switching Losses

In most application notes and datasheets [194], switching times are defined through gate- and drain-to-source voltage. Due to the inability to measure gate voltage, the turn-on time $t_{on}$ is defined as the time from $I_d$ reaching 10% of the steady-state current to $V_{ds}$ falling
to 10% of the dc-bus voltage. The turn-off time $t_{\text{off}}$ is defined as the time from when $V_{ds}$ rises to 10% of the bus voltage to the drain current falling to 10% of the load current. The definitions are the same as in [176]. Hence, as indicated in Fig. 3.29, the turn-on switching energy $E_{\text{sw, on}}$ and turn-off energy $E_{\text{sw, off}}$ are integrals of the product of $I_d$ and $V_{ds}$ over $t_{\text{on}}$ and $t_{\text{off}}$, respectively.

Fig. 3.30 (a), Fig. 3.30 (b), and Fig. 3.30 (c) show the switching $E_{\text{sw, on}}$ and $E_{\text{sw, off}}$ loss distributions. As discussed in Section 3.2.2, $E_{\text{oss}} = 9 \text{ mJ}$ is added to the measured $E_{\text{sw, on}}$, while it is subtracted from the measured $E_{\text{sw, off}}$. Comparing the two losses, $E_{\text{sw, on}}$ is significantly higher than $E_{\text{sw, off}}$. This huge discrepancy cannot be attributed to the influence of the utilized experimental setup:

1. For the Gen-3 10 kV SiC MOSFET dies, the body diode (freewheeling diode of DPT) reverse recovery effect can be neglected [175, 195].

2. The influence of $C_{\text{epc}}$ of the DPT inductor is negligible. The Keysight/Agilent 4294A Precision Impedance Analyzer measured $C_{\text{ind}}(EPC) = 16 \text{ pF}$, which results in $E_{\text{epc}} =$
Figure 3.30: Switching losses dependency vs current and $R_{g,\text{ext}}$. a) Turn-on and turn-off energy losses. b) Zoomed-in turn-off energy losses. c) Switching losses dependency vs junction temperature $T_j$.

Rather, the discrepancy is contributed to the inherent behaviour of the SiC MOSFET HB module:

1. It does not have the turn-off tail current compared to Si IGBTs [196].
2. There is the influence of the parasitic capacitor's $C_{oss}$ charging/discharging during transients [178, 195, 197].
3. The high Miller Plateau voltage level [198], confirmed by the experimental switching waveforms including $V_{gs}$, will be shown in Section 4.4.3.
The $E_{sw, on}$ is highly dependent from both the load current $i_{ind}$ and $R_{g, ext}$. As expected, $E_{sw, on}$ increases with $i_{ind}$ linearly, (e.g., at $R_{g, ext} = 0.83 \, \Omega$, losses increase from 78 mJ at 20 A to 128 mJ at 100 A), while decreasing with reduced $R_{g, ext}$, (e.g., from 143 mJ at $R_{g, ext} = 1.33 \, \Omega$ to 108 mJ at $R_{g, ext} = 0.66 \, \Omega$ for 84 A). The impact of junction temperature $T_j$ on $E_{sw, on}$ is not severe; however, it is not negligible. Fig. 3.30 (c) indicates roughly a 10% decrease in losses from 25 °C to 150 °C, showing similar trends as in [75]. An explanation for this phenomenon can be found in [184], where it is claimed that due to junction capacitances insensitivity to the temperature, that this behavior is more closely related to the temperature dependence of the transconductance and threshold voltage of the SiC MOSFET. This is confirmed in Section 3.2.2, where it can be seen that the transconductance increases with temperature, while the threshold voltage decreases, as well as Miller Plateau voltage level. This leads to faster $di/dt$ and $dv/dt$ and reduced turn-on losses with increase of temperature (this will be confirmed in the next subsections.) The $E_{sw, off}$, shown on Fig. 3.30 (b), exhibits significant dependence on load current, 5 to 6 times from 20 A to 120 A. Furthermore, it evinces a noticeable dependency on $R_{g, ext}$. However, it is not severe magnitude-wise as the loss dependence on $R_{g, ext}$ that $E_{on}$ exhibits. Since the almost complete MOSFET’s current during the turn-off, charges the parasitic capacitors [175] which are temperature independent, $E_{sw, off}$ shows no dependence through the whole temperature range.

**Voltage Slew Rates - $dv/dt$**

Fig. 3.31 (a) and Fig. 3.31 (b) show the turn-on and turn-off $dv/dt$ distributions. Turn-on $dv/dt$ is mainly determined by the $R_{g, ext}$ while showing negligible decrease with the increase of $i_{ind}$. For example, at $R_{g, ext} = 0.67 \, \Omega$, $dv/dt = 73 \, V/\text{ns}$, which increased from 44 V/ns at $R_{g, ext} = 1.33 \, \Omega$; this is an increase of 66% for the almost complete current range. Turn-on $dv/dt$ also significantly depends on temperature, showing a linearly increasing trend
with rising temperature, e.g., $dv/dt$ increased for 28 V/ns for $R_{g,ext} = 0.67 \, \Omega$ from 25°C to 150°C. Different from turn-on $dv/dt$, turn-off $dv/dt$ is mainly determined by the $i_{ind}$ and nearly independent from $R_{g,ext}$. The impact of elevated $T_j$ on turn-off $dv/dt$ is negligible.

![Figure 3.31](image1)

**Figure 3.31:** (a) $dv/dt$ dependency vs current and $R_{g,ext}$. (b) $dv/dt$ dependency vs $T_j$ for $I_d = 84 \, A$.

**Current Slew Rates - $di/dt$**

![Figure 3.32](image2)

**Figure 3.32:** (a) $di/dt$ dependency vs current and $R_{g,ext}$. (b) $di/dt$ dependency vs $T_j$ for $I_d = 84 \, A$.

Fig. 3.32 (a) and Fig. 3.32 (b) show the turn-on and turn-off $di/dt$ distributions. Turn-on $di/dt$ is determined by the $R_{g,ext}$ while showing considerable dependence from the load current $i_{ind}$ as well. For $R_{g,ext} = 0.67 \, \Omega$, $di/dt = 3.08 \, A/\text{ns}$ which increased from 1.3 A/ns at $R_{g,ext} = 1.33 \, \Omega$. This is an increase of 132% at the $I_{ind} = 84 \, A$. As for the current dependence of turn-on $di/dt$, for all used $R_{g,ext}$, it increases over 41% over the whole characterized current range. Also, turn-on $di/dt$ depends on temperature significantly, showing
quite a linear increasing trend with rising temperature, e.g., $di/dt$ increased from 1.75 A/ns to 3 A/ns for $R_{g,ext} = 1 \Omega$ from 25°C to 150°C. This behavior is closely related to the increase of transconductance with temperature, as shown in Section 3.2.2, which implies faster transitions. Different from turn-on $di/dt$, turn-off $di/dt$ is determined by the $i_{ind}$ and nearly independent from $R_{g,ext}$, at least for these low values of gate resistance. The impact of elevated $T_j$ on turn-off $di/dt$ is negligible as well.

**Switching Times**

Switching times, as defined at the beginning of this section, and their dependencies on device current, temperature, and gate resistor, are shown in Fig. 3.33.

![Figure 3.33](image)

*Figure 3.33:* (a) Switching time dependency vs current and $R_{g,ext}$. (b) Switching time dependency vs $T_j$ for $I_d = 84$ A.

$t_{on}$ exhibits similar trends for both $dv/dt$ and $di/dt$ and is determined by the $R_{g,ext}$ and $i_{ind}$. Basically, $t_{on}$ is getting faster with a decrease of $R_{g,ext}$ resistance, while it exhibits a slight rise with the rise of the current through the device. With the increase of temperature, $t_{on}$ is decreasing, by which the conclusion could have been made solely based on previously shown $dv/dt$ and $di/dt$ trends. $t_{off}$ shows nearly independent behavior with changing $R_{g,ext}$ and elevated $T_j$; however, it shows strong dependence on the current through the device.
Submodules Current Sharing

To ensure good thermal performance and to avoid hot spots, relatively balanced current sharing between the three submodules is of the utmost importance and must be checked. Homogeneous current sharing is also the key to maintain high ruggedness of the whole converter, and it allows an optimal utilisation of the power modules with a minimal derating.

![Dynamic and static turn-off current sharing](image)

**Figure 3.34:** Experimental current sharing waveforms of three submodules at $V_{ds} = 6$ kV, $I_d = 120$ A, $T_j = 25$ °C, for external gate resistors $R_{g,ext} \in [1.33, 1, 0.67]$ Ω. (a) Static and dynamic turn-off current sharing. (b) Dynamic turn-on current sharing.

Fig. 3.34 shows the dynamic and static current sharing for different $R_{g,ext}$ at the same $T_j = 25$ °C. With reducing $R_{g,ext}$, current sharing behaviour generally worsens, especially during the turn-on transition where the mismatch jumps from 5% for $R_{g,ext} = 1.33$ Ω to 15% for $R_{g,ext} = 0.67$ Ω. The turn-off transition and on-state are more moderate, almost negligible. These effects are explained easily by looking at Fig. 3.32 (a), where it can be seen that $di/dt$ during turn-on severely increases with the reduction of $R_{g,ext}$, while for turn-off that increase is small, almost negligible.

Fig. 3.35 shows dynamic and static current sharing for different $T_j$ at the same $R_{g,ext}$. The
impact of elevated $T_j$ on static and dynamic turn-off events has similar values as the impact of $R_{g,ext}$ reduction, while for turn-on, current sharing throughout the complete temperature range slightly worsens. Turn-on current unbalance worsening can be explained through threshold voltages $V_{gs,th}$ of the submodules in combination with the severely increasing $di/dt$. Fig. 3.36 (a) shows that the imbalance of the $V_{gs,th}$ of different submodules still exists at the higher temperature. It can be observed that the difference between $V_{gs,th,sub1}$, $V_{gs,th,sub2}$, $V_{gs,th,sub3}$ at 125 °C is smaller than for 25 °C. However, it is believed that at 125 °C this existing difference between $V_{gs,th}$, together with the impact of higher $di/dt$ (Fig. 3.32 (b)), impacts the current balance adversely, since all events in the transients happen faster than at 25 °C. Therefore, different submodules hit the threshold faster than for the ambient temperature case, resulting in higher current imbalance. On the positive side, with higher temperature, the switching speed gets faster (Fig. 3.33 (b)), resulting in the magnitude and difference of switching losses decreasing between submodules. This means that even though current sharing is worse, switching losses are smaller, so overall the resulting temperature will be smaller. Static current sharing deteriorated with an increase of $T_j$. These tests were
performed through the DPTs, where all of the dies of all submodules were assumed to be at the same temperature. In that case, under the assumption that during duration of the DPTs sequence $T_j$ does not change, static sharing is purely dominated by the $R_{ds,\text{on}}$ values. Fig. 3.36 (b) shows the three submodules at the same temperatures do not have the same $R_{ds,\text{on}}$, and the difference between them usually becomes worse at elevated temperature. However, during continuous operation, the positive temperature coefficient of the SiC MOSFET’s $R_{ds,\text{on}}$ will contribute to a smaller current sharing imbalance since 3 submodule’s $R_{ds,\text{on}}$s will naturally balance out. As a result, this effect should not present a huge impact.

![Figure 3.36](image)

**Figure 3.36:** Additional static characterization results for each of the XHV-6 3 submodules. (a) Threshold voltage dependence at different temperatures. (b) On-state resistance vs. current and temperature for 1st quadrant, $V_{gs} = 18$ V where $R_{ds,\text{on}}$ measured with Agilent B1505A curve tracer.

It can be confirmed that good thermal performance can be ensured, that the developed eGD drives them almost synchronously, and all mismatches can be contributed to the device and module used. With this, hot spots will be avoided, due to relatively balanced current sharing among the three submodules with the usage of reasonable $R_{g,\text{ext}}$. Regardless, based on the chosen $R_{g,\text{ext}}$ and maximum temperature for the intended application module, de-rating based on current sharing has to implemented into defining the safe operating area.
3.5 Summary

This chapter consists of the static characterization of the 10 kV, 240 A Gen-3 SiC MOSFET XHV-6 from the CREE/Wolfspeed device, development of an enhanced GD unit, and device dynamic characterization. Through static characterization of the XHV-6 device, it is found that the device exhibits low $R_{ds,\text{on}} = 21 \, \Omega$ @ 25 °C. $R_{ds,\text{on}}$ has a high dependence on temperature of around 340% from 25 °C to 175 °C, peak transconductance of 40 S @ 175 °C, and parasitic capacitances of $C_{\text{iss}} = 92.8 \, \text{nF}$, $C_{\text{oss}}(6 \, \text{kV}) = 0.501 \, \text{nF}$, and $C_{\text{rss}}(6 \, \text{kV}) = 0.2 \, \text{nF}$. The most important characteristics of the developed GD are as follows:

- The power supply utilized is the air insulated CT-based GDPS with a PDIV of 5.47 kV and input output capacitance of $C_{\text{io}} = 1.9 \, \text{pF}$.
- The power and signal architecture is designed in a way to "fight" CM noise by an impedance mismatch technique, redirecting noise from sensitive signal circuitry; the design can sustain $dv/dt \geq 100 \, \text{V/ns}$.
- The driving stage is capable of providing up to 90 A with near perfect gate current sharing for three submodules while keeping the driving loop inductance below 5 nH.
- An active Miller clamp circuit is implemented to suppress potential cross-talk issues.
- The Rogowski switch-current sensor is designed for protection of the SiC device and control of the system, while not compromising voltage distribution or introducing any PD under rated voltage.
- A digital potentiometer (DPOT) is proposed as a part of the closed-loop self-calibration process for a Rogowski switch-current sensor (RSCS). It achieves good resolution of the system of 98.6 $\mu \text{V}$ to eliminate input offset voltages, with a maximum error of the system of $\pm 2.5 \, \text{A}$ per RSCS. It finished relatively quickly during start-up, within 12.4 ms maximum.
As expected, dynamic characterization device losses are relatively small, especially compared to an IGBT at similar conditions. Interestingly, the total losses reduce with an increase in temperature, due to an increase in both $dv/dt$ and $di/dt$ of the device, and consequently, a reduction of switching times. Additionally, it is shown that the current sharing between the submodules is satisfactory with a maximum mismatch observed of 15%, at very low $R_{g,exy}$, and high $T_j$. 
Chapter 4

Design and Assessment of a Half-Bridge Power-Cell based on a High-Current 10 kV SiC MOSFET Module

4.1 Introduction

Configuration-wise, apart from the basic half-bridge topology of the power cell, multiple others exist, such as the full-bridge, flying capacitor, diode-clamped, T-type 1, T-type 2, single-clamped, clamped-double, cross-connected, asymmetrical, mix-connected \[199\], NTSM \[200\], and Semi-Full-Bridge \[201\]. Even though the MMC has an inherent dc-fault problem, the half-bridge is most often used due to its smaller number of active devices, as well as its passive components, straightforward capacitor voltage balancing, lower cost, and lower losses \[199\]. The half-bridge (HB) power cell architecture, adopted in this dissertation (from now on referred to as HB-PEBB), is shown on Fig. 4.1. The power stage is comprised of two power switches in a totem-pole configuration, a laminated dc bus, dc-link capacitors, and a phase inductor. The fiber-optic-based digital sensing and control system includes a controller, isolated digital sensors, and enhanced gate-drivers. The listed circuitry is powered by a wireless power transfer auxiliary power supply (WPT-APS), as opposed to a conventional dc-link fed auxiliary power supply. The HB-PEBB architecture exhibits complete modularity, excellent noise immunity, and a high degree of intelligence, making it capable for more
advanced functionalities [115].

The power cell design based on the selected 10 kV SiC MOSFET will face an abundance of intertwined challenges, such as high-voltage insulation, high $dv/dt$, component and system protections, as well as thermal management. To tackle these potential operation stoppers and to ensure system safety, a detailed systematic power-cell design and assessment methodology (DAM) is of upmost importance. Furthermore, the DAM should fully explore the HB-PEBB capabilities prior to converter-level implementation. This chapter explains in more detail the research presented in [163, 202].

### 4.2 Overview of Design and Assessment Methodology (DAM)

The systematic hierarchical HB-PEBB DAM framework from the component-level to the HB-PEBB level, is shown in Fig. 4.2. The HB-PEBB specifications are first defined as follows:
dc-bus voltage $V_{dc} = 6 \text{kV}$, phase current $I = 84 \text{A}$, switching frequency $f_{sw} \geq 5 \text{kHz}$, device junction temperature $T_j \leq 150^\circ \text{C}$ (preserving margin of $25^\circ \text{C}$), power-cell power density $\geq 10 \text{kW/l}$, efficiency $\eta \geq 99\%$ ($\eta \geq 97\%$ at light load), and unrestricted voltage and current scaling without galvanic isolation. The HB-PEBB should be designed to operate in both dc-dc and dc-ac conversion mode, suitable for the switching-cycle control (SCC) of the MMC [15, 126] and for the integrated capacitor-blocked transistor (ICBT) topologies [127], as previously mentioned.

Subsequently, a comprehensive component-level DAM follows, detailing the design and modeling challenges and solutions. The first step of the component-level DAM is to select the
power device if available, to fit the HB-PEBB intended specifications or design a prototype device. After that will come the design pieces, such as the gate-driver (either a commercial or a custom designed one with specific additional properties), dc busbar (either laminated or PCB planar bus), controller and auxiliary circuits (commercial or custom designed ones) and cooling system (cooling medium, heatsink design, modeling etc.). After modeling and fabrication, piece-wise verification is the next step which consists of assessment instruments, procedures, and experimental results. To be more explicit, the static characterization of the device should perform as well as the basic functionality tests of the electrical equipment. Additionally, after passing the insulation assessment (both partial discharge and breakdown) for all individual components and the HB-PEBB as a whole, the cooling system thermal testing and verification should be performed, either through an extensive simulation or in a mock-up structure with roughly nominal losses. The final step for piece-wise verification is the pulsed switching under rated voltage and power-device dynamic characterization, over-current and short-circuit protection verification, as well as the busbar thermal and SC tests. As seen in Fig. 4.2, all component-level design workflows will eventually merge into a decision block to determine if the component designs need to be iterated before they enter the next step.

If piece-wise verification is passed, the DAM expands to the power-cell level to characterize the capabilities of the power cell, as well as to explore its boundaries (safe operating area) and limitations. In system-level verification, the first step is to choose a proper type of continuous test, regenerative or non-regenerative. For MV high-power converters, a non-regenerative direct load test at rated power is challenging, due to limited grid and load capabilities, and huge energy expenditure. Before starting the continuous tests, it is important to identify the thermal safe operating area (SOA) to know the thermal limit of the HB-PEBB at the different conditions. After that, a series of continuous tests are conducted to verify thermal, $dv/dt$ transient immunity, and efficiency performance. Again, another decision will be made
at the end of the power-cell-level DAM to determine if the component designs will be iterated. If it passes, the power-cell design is completed.

It should be noted that to conserve space, the failed design revisions will be omitted, and only the finalized designs will be elaborated.

4.3 Component-Level DAM with Design Details

4.3.1 Semiconductor Device and Gate-Driver

Semiconductor Device

The first step of the component-level DAM is to select and characterize the power device. To fully explore the benefits of SiC MOSFET devices for MV high-power applications switching on high frequency (≥ 5 kHz), the power-cell design is pursued using the latest 10 kV, 240 A (maximum current available) Gen-3 SiC MOSFET XHV-6 from CREE/Wolfspeed [78]. The module is comprised of 3 submodules in parallel, a total of 18 dies per switch position [74], and is the kernel part of the power cell.

Static characterization of the module has been performed at 25 °C, 75 °C, 125 °C, and 175 °C to observe device parameters and the temperature influence on them. These results are shown in Section 3.2. For loss estimation and SOA definition, the crucial parameters are output characteristics and parasitic capacitance.

The output (I-V) characteristics contain on-state resistance $R_{\text{ds,on}}$ information and its temperature dependence, which are crucial parameters in defining conduction losses $P_{\text{cond}}$ of the device. Fig. 4.3 shows $R_{\text{ds,on}}$ and $P_{\text{cond}}$ of the XHV-6. The 10 kV device conduction loss is significantly impacted by its junction temperature, and the influence of the temperature
must be used properly to obtain the correct loss model, thus SOA. The $P_{\text{cond}}$ example shown is for the square wave current through switch with a 50% duty cycle. Conduction losses for this case are defined through

$$P_{\text{cond}} = R_{\text{ds, on}} \cdot I_{\text{rms}}^2$$

(4.1)

$$I_{\text{rms}} = \int_0^T \sqrt{i^2} dt = \frac{I_{\text{peak}}}{\sqrt{2}}.$$  

(4.2)

![Figure 4.3: On-state resistance and switch conduction loss dependency vs. current and temperature for 1st and 3rd quadrant, $V_{\text{gs}} = 18\, V$. $R_{\text{ds, on}}$ measured with Agilent B1505A curve tracer. $P_{\text{cond}}$ calculated for 50\% duty cycle.](image)

The device parasitic capacitors provide better insight into the dynamics of the device. How the device parasitic capacitors influence the dynamics and thus losses of the device are shown in Section 3.2 and Section 3.4.

**Enhanced Gate-Driver**

An enhanced GD (eGD) is designed and tested as shown in Section 3.3. The results verify excellent gate current sharing between the different submodules, and the power current sharing under different gate resistors and temperatures is shown as well. The effectiveness of the implemented architecture, considering the bypassing of the CM noise current, active
Miller current, as well as the high-bandwidth-and-accuracy Rogowski switch-current sensor (RSCS) for protection and control, will be shown in later sections when the continuous operation results are shown.

4.3.2 Individual Component Insulation Design and Coordination

The components insulation system used in the designed MV power cell must be partial discharge (PD) free under converter normal operation; otherwise, the lifetime will be significantly reduced \cite{203}. Moreover, excessive PD in the air can damage the sensitive ICs and power modules directly, which further leads to cascaded failures in the converter system \cite{204}.

In general, the MV power cell has a dry-type insulation system, which only contains solid insulation materials and air. The solid material system, comprised of insulation films (polymer, GPO3, FR4, etc.) and the adhesive or encapsulation material, are applied into individual components to meet their own insulation requirements, while air is usually among the components for satisfying the clearance and creepage requirements. Therefore, the PD free design target can be divided into two categories. First, there should be no PD inside of the solid material (i.e., voids, defects in adhesive and/or encapsulation regions). Thus, the solid material system without internal discharges can be considered as the internal insulation design. For the internal insulation design, the guidelines followed for thicknesses are dependent on the material dielectric strength and the manufacturer recommendation considering aging, e.g. 20kV/mm for a FR4 PCB. Reflecting back to Fig. 4.1, two major pieces exist that should be considered in the internal insulation design: the busbar and the shielded inductor. By comparison, no PD should occur in air, especially along the metal or insulator to air interfaces since these widely exist in MV applications and converters. To
effectively satisfy the external insulation requirements along such interfaces, a large distance in air is usually applied, significantly impairing power density. For novel SiC-based converters, which are seeking high-power density, these large distances are contradictory and usually non-acceptable. As PD in air is traditionally called external discharge, this type of insulation design will be referred to as external insulation design. Summarized well in [121], based on the discharge location and the corresponding hazard to the converter system, the possible external discharge events inside the PEBB converter prototype can be divided into 4 types. Type 1 are the discharges between the interconnections among the power module, laminated bus, copper bars and PCB Rogowski coil sensing board. Type 2 are the discharges occurring on the power stage (busbar connections, and inductor triple point). Type 3 are the discharges occurring on the PCB of the driving and control circuits (gate-driver, controller and sensors). Type 4 discharges can occur in the isolated auxiliary power supply system, such as between the primary and secondary winding of the transformer. Each of these types can lead to inrush current through the control or power terminals of the power module and can destroy the modules, as well as the rest of circuitry inside the HV-PEBB. For the external insulation design, the general design guideline used is E-field \( \leq 2 \text{kV/mm} \), relying on the Finite Element Analysis (FEA), approach widely used in HVDC applications [205, 206]. For individual components, PD free internal insulation design is more challenging, while for insulation coordination among components, PD free external insulation design would be the major task. Two examples are given as representative, in order to demonstrate the quite different considerations for internal and external insulation design, respectively, as well as the individual component and power cell level assessments.
Internal Insulation Design Example–Multilayer PCB Planar Bus

The first version of the conventional laminated busbar with its layer design and fabrication details can be found in [115]. GPO3 insulation plates are implemented between positive (+dc) and negative (-dc) layers with a thickness of 5 mm, while a 2.5 mm insulation layer is between the positive or negative and adjacent middle (mid) layers. Adhesive and encapsulating material is applied to attach the layers together, as well as sealing the bus edges. According to [119], this design failed initial PD testing. It exhibits around 1 nF discharge at only 4 kV rms between the positive and negative layers, where the general requirement allows less than 10 pC discharge at the designed operation voltage. Furthermore, to achieve a compact and reliable insulation, an additional analysis has been applied in areas for the interconnection with the coaxial cylindrical structure, such as screws and capacitor connections. If tremendous defects in the adhesive layers and encapsulation along the edges exist, together with air pockets along the interconnection regions, a great amount of internal discharge can be introduced even at relative low excitation. As a result, both fabrication and design must be improved [119].

Thanks to the mature PCB industry, for the bus size and intended current rating, a PCB based laminated bus can be fabricated, ensuring low parasitic inductance and high PD inception voltage. Due to the vacuum hot pressing, defects and air pockets causing problems in the previous design can be eliminated to a large extent. Moreover, PCB designs exhibit very accurate metal and insulation fabrication, enabling the implementation of multiple E-field management methods during design. As an example, the 2D section view of the PCB based bus along one of its interconnection regions is shown in Fig. 4.4(a). Compared to the conventional laminated bus, almost all insulation and metal dimensions can be precisely controlled in PCBs. As prepreg and vacuum hot pressing help remove air bubbles in the adhesive layer, plated-through holes avoid any air pockets along the interconnectors. Moreover, thin metal
pads or layers can be applied and only serve as an E-field shielding purpose in the PCB.

As shown in Fig. 4.4 (a), by adding one more middle layer, the positive layer is entirely sandwiched and shielded by the two middle layers. Then, by adjusting the insulation thickness 1 and offset 2, the E-field intensity at the positive layer edges can be controlled, as marked by region 1 in the same figure. Similarly, by changing the offset 1 and additional core thickness, the E-field intensity of region 2 and region 3 can be adjustable. Finally, the exposed metal pad should increase until the sharp edges on the metal connector (region 4) are well shielded.

The design methodology of the PCB planar bus is discussed in [207].

Via FEA simulation, E-field distribution analysis is completed, individually, for all of the critical regions. During simulation, the potential on the positive layer is 10 kV and 0 kV on the negative layer while 5 kV is applied for all middle layers. With all of the E-field management methodologies, in the final design, the maximum E-field intensity inside the PCB is lower than 20 kV/mm with no more than 2 kV/mm in the air around it [207]. After fabrication, the new PCB based laminated bus is only about 5 mm thick (shown in Fig. 4.4(b)), while the conventional one should be about 30 mm thick to meet the same PD free requirement. Compared to conventional laminated bus design which has 36.2 nH power loop inductance, the multilayer PCB planar bus has only 8.8 nH; both values are obtained
with the ANSYS Q3D Extractor via FEA simulation. The parasitic capacitance between
the +dc and mid layer, as well as between the -dc and mid layer is around 12 nF, due to
symmetric PCB design. The PCB planar bus is designed for a maximum 84 A rms (120 A
peak), which defines its thermal limit. Keeping in mind the desired high power density and
intended application of the power cell for the SCC mode MMC converter and ICBT, the
chosen capacitor bank is only $C_{dc} = 32.5 \mu F$. This results in a lower limit for the switching
frequency of $f_{sw} = 5 \text{kHz}$ for a maximum allowable voltage ripple at the dc-link capacitor.

**External Insulation Design Example–Interconnection among Power Module, Laminated Bus, Copper Bars, and PCB Rogowski Coil Sensing Board**

Due to different voltage potentials along all metal parts and limited space, the E-field inten-
sity in the air around such interconnection regions can be high, which can be enough for
initiating tremendous PD. The external insulation should be very carefully analyzed. One
of the regions in the HB-PEBB is the interconnection among the power module, laminated
bus, copper bars, and PCB Rogowski coil sensing board within the power cell. However,
this particular piece was already discussed in detail in 3.3.6.

**4.3.3 Insulation Assessment**

Although this should be eliminated by the design, fabrication issues (defects inside the
material), inaccurate geometry dimensions (mechanical tolerance, metal surface roughness),
and air or solid material property variations, etc., are possible, which could result in massive
internal and external PD. Therefore, an experimental insulation assessment must be applied
before any converter level power tests. After the experimental insulation assessment tests, if
the insulation fails the PD free requirement, further insulation diagnosis and improvements
must be applied during the redesign. Therefore, the insulation design and assessment should always be an iterative process until all issues have been solved, and the final designs pass the test. Standard IEC 60664 is fully followed during the experimental assessment (PD tests) for both internal and external design. For the two examples described previously, the experimental test setup and results are described in this section.

**Internal Insulation Assessment Example—Multilayer PCB Planar Bus**

![Diagram of internal insulation assessment of a multilayer PCB planar bus.](image)

**Figure 4.5:** Internal insulation assessment of a multilayer PCB planar bus. (a) Experimental setup with bus under test. High frequency current transformer (HFCT): ETS-lindgren 91550-1. PD detection and workstation: Doble PD-Smart Partial Discharge Analyzer. (b) Experimental results at 6 kV rms.

The multilayer dc PCB planar bus in the converter operation is subject to dc voltage. However, by using the 60 Hz ac excitation, compared to the dc test, the internal PD can be excited at a lower excitation magnitude, due to the low permittivity of air in the defects. As the excitation polarity periodically alternates, a higher PD repetitive rate is expected, which helps the PD experimental measurement. Moreover, insulation diagnosis methods, which are usually based on a phase resolved PD (PRPD) pattern, can be applied. Thus, the ac test, shown in Fig. 4.5 (a), has been completed for the multilayer PCB planar bus to evaluate its internal insulation design.

When the middle layers are connected to high voltage and the +dc and dc- layers are grounded, its PDIV is around 5.5 kV rms (discharges ≥ 10 pC) where the designed value
is 5 kV peak. In order to form a clear vision, 6 kV rms is applied with the typical Phase Resolved PD (PRPD) pattern shown in Fig. 4.5 (b). Based on the PRPD pattern, most of the PD is surface discharge instead of internal discharge, according to the analysis in [208]. This means that the external insulation design limits the PD performance of this bus, as PD mostly happens in air first. Then, the positive layer is connected to high voltage, and the negative layer is shorted to ground. Although the middle layers are floating, due to the well balanced parasitic capacitance, the middle layer should still get half of the total excitation voltage. The PDIV is about 8.5 kV rms (12 kV peak) under this connection. Moreover, the entire bus is later checked by a dc test at rated voltage for confirmation, and there is no obvious PD under 10 kV dc excitation.

As a summary, this PCB based laminated bus is PD free at normal operation voltage of 6 kV as well as for the extreme condition of 10 kV. If a higher insulation rating is necessary, the external design should be improved first, as it limits the bus PD performance.

External Insulation Assessment Example–Interconnection Among Power Module, Laminated Bus, Copper Bars, and PCB Rogowski Coil Sensing Board

![Diagram](image.png)

**Figure 4.6:** External insulation assessment for interconnection among power module, laminated bus, copper bars and PCB Rogowski coil sensing board (PCB busbar hidden in this picture for better view). (a) Experimental setup top view. SiPM sensor: Hamamatsu C13366-1350GA. (b) PD measurement system schematic with indicated detection method for external discharges under PWM excitation. (c) PRPD pattern for the assembly under test with negative unipolar PWM excitation with external charges captured by SiPM.
Targeting the external discharge free design approaches that reflect the relationship between the insulation structures and square wave excitation parameters, is highly demanded.

In real operation of the HB-PEBB, interconnections are subjected to a square wave (PWM) excitation; therefore, a commercial high voltage square wave excitation generator is utilized to provide adjustable square wave excitation. A 3D printed plastic power module is configured with a real PCB Rogowski coil sensing board and metal connectors, to create the same insulation structure as in the real unit, as shown in Fig. 4.6 (a). For PD detection under square wave excitation, during the switching transition, the PD impulse current can be easily overwhelmed by the displacement pulse current in both time and frequency domains. Therefore, the Si photomultiplier (SiPM) based external optical discharge sensor is used. Through the detection of photons introduced by external discharges, the PD events can be separated from the displacement current correctly and effectively. The structure, working principle, and performance of this optical sensor are discussed in detail in [121]. The HFCT method is applied simultaneously, which can help quantify the PD events. The assembly under test with all sensors is then placed inside a sealed electromagnetic compatibility (EMC) chamber, as shown in Fig. 4.6 (b). All power and communication cables go through an opening on the chamber wall, while all gaps are carefully covered and sealed to block any light leakage. For the interconnections shown in Fig. 4.6 (a), only the unipolar square wave excitation will appear during the converter real operation. Because of the polarity effect and considering the worst scenario, negative unipolar square wave excitation is used for the metal connectors while its adjacent Rogowski coil is grounded. Under this condition for this assembly, its typical PRPD pattern is shown in Fig. 4.6 (c), and the PDIV is around 11 kV (for pulse width of around 100 μs). This assembly is also checked by 60 Hz AC excitation, and the PDIV is around 7.5 kV rms.

With this, the described internal and external insulation designs are confirmed to be PD free
under rated voltage of 6 kV with a strong indication that this condition would be maintained, even under extreme 10 kV excitation. The insulation design for other parts inside the power cell will follow the same design and assessment methodology as described.

4.3.4 Cooling System

Cooling Solution

Cooling methods for power electronics converters are divided into several groups, depending on the working medium (air/water/insulation liquid), flow direction (indirect/direct), channel sizes (micro/regular), and whether it contains phase-change cooling (single/two) [209]. The XHV-6 HB module (18 die per switch position) exhibits a relatively small junction to case thermal resistance per die ($R_{th, j-b} = 0.468 \text{K/W}$). The equivalent junction to ambient thermal resistance $R_{th, j-a}$ only needs to be around 1 W/K for the temperature rise of $\Delta T_j = 125 \text{C}$, with assumed uniformly distributed heat flux of 200 W/cm$^2$ per die. Considering the $R_{th, j-a}$ and availability of fans to provide sufficient air flow, a conventional forced air-cooling system with a parallel-fin heatsink, presents a possibility. With a similar cooling system, thermal resistance can be further reduced. The heatsink can be replaced by a vapor chamber or a thermal pyrolytic graphite (TPG) enhanced heatsink, which achieves higher thermal conductivity with less weight [210]. Also, high speed compact compressors with jets under impingement mode can be used to reach a better convective condition [211]. Admittedly, this design can utilize liquid cooling as well, to be more efficient. However, complicated liquid circulating system design, reliability concerns, scalability, and flexibility of the MMC system for MV applications makes it unsuitable. The combination of different cooling methods can result in a higher convective coefficient. For example, with combined micro-channel, two phase, impinging cooling, the heat transfer coefficient can reach 43 kW/m$^2$K and handle
a heat flux of 910 W/cm² [212]. However, such cooling systems bring challenges to module packaging, requiring extremely high thermal conductivity of packaging materials to form a very small thermal resistance inside the packaging. Otherwise, under a high convective condition, the heat spreading area inside the module will shrink significantly, which limits the entire thermal performance and wastes the efforts in the cooling system. Furthermore, phenomena like local dry-out have been reported in such cases [213]. As a result, the entire cooling performance is limited by the power module packaging, regardless of the cooling system.

Therefore, conventional forced air-cooling with a commercially available fan and heatsink is designed. For the heatsink material, two options are generally adopted: copper and aluminum. Even though copper (Cu) exhibits higher thermal conductivity than aluminum (Al) ($k_{\text{Cu}} = 413$ W/mK and $k_{\text{Al}} = 237$ W/mK), the weight, availability, price, and manufacturing process of a heatsink for the power module of this size (due to the softness of Cu) makes it unsuitable. Shown in Fig. 4.7 (a) and Fig. 4.7 (b), the best commercially available aluminum heatsink and fan providing an air flow of 500 CFM, are chosen.

To verify the thermal design and estimate the cooling performance under different power cell operation modes, an FEA thermal model is developed in Ansys Icepak, as indicated in Fig. 4.7 (c). The air ducts are comprised of several rectangular adiabatic walls. There is a circular opening for an air duct inlet, and the air outlet is completely open without any fairings. The flow region defined by this duct will be the same as in the real setup. The XHV-6 power module is placed on the top side. Packaging materials and their layer thickness are provided by the manufacturer with the properties listed in Table 4.1. For thermal conductivity, except SiC, all are from datasheets and do not change greatly with a temperature range of 25°C to 150°C. SiC thermal conductivity can be quite different depending on the temperature [214], and a typical value under 150°C is selected.
Cooling Verification

To verify that the chosen heatsink and fan combination can deal with the assumed losses, the developed model is put through a series of simulations. Fig. 4.7 (d) shows simulation results
Table 4.1: Packaging Material Thermal Performance Related Properties

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal conductivity $k$ (W/mK)</th>
<th>Density $\rho$ (kg/m$^3$)</th>
<th>Specific heat $c$ (J/kg°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Carbide</td>
<td>245</td>
<td>3210</td>
<td>750</td>
</tr>
<tr>
<td>Aluminum Nitride</td>
<td>170</td>
<td>3259</td>
<td>734</td>
</tr>
<tr>
<td>Copper</td>
<td>360</td>
<td>8933</td>
<td>385</td>
</tr>
<tr>
<td>Aluminum</td>
<td>200</td>
<td>2700</td>
<td>900</td>
</tr>
<tr>
<td>Die Attachment</td>
<td>150</td>
<td>8900</td>
<td>235</td>
</tr>
</tbody>
</table>

for the 4 kW case where the heat flux 170 W/cm$^2$ per die is uniformly assigned. The results show that the junction temperature is $T_{j,max} = 153^\circ$C for the assigned losses, which are lower for about 30 W/cm$^2$ than the design requirement. Even though a small discrepancy exists, the origin is generally unknown and difficult to investigate without experimental verification. The developed model shows that the designed cooling system should handle close to assumed losses, which is considered good at this point. Since the cooling condition in use is different from the assumption applied by the power module manufacturer, experimental verification of the model and thermal modeling methodology have to be done on the system level test with the power cell in continuous operation. The FEA simulation and experimental test results comparison under the same loss distribution is provided in Section 4.4.2.

4.3.5 Common Mode Voltage Power-Cell Insulation Assessment

Both internal and external differential voltage insulation designs are confirmed to be PD-free under voltage of 6 kV. However, before any converter level power tests, an experimental insulation assessment must be applied for the complete power cell to find the maximum common-mode (CM) voltage PD-free limit. To find the maximum CM voltage PD-free limit, the converter frame and cooling system-fans will be on earth GND, while the power cell parts are shorted and placed on high voltage potential. Again, Standard IEC 60664 is
fully followed during the experimental assessment (PD tests).

To perform this high voltage partial discharge testing, the in-house setup used is shown in Fig. 4.6 (b) where the assembly under test is the power cell. The 60 Hz AC PD test will be performed, and the PD-events can be easily captured with the high frequency current transformer (HFCT). The setup schematic shown in Fig. 4.6 (b) is PD-free up to a 48 kV peak. The power cell connected to the setup is shown in Fig. 4.8 (a).

The investigation of the complete power-cell maximum PD-free level has been done sequentially, starting with just the frame and fans on GND potential and the heatsink on high voltage. A systematic approach was used so that the main power stage components below the bus were added first with the bus and components above it. The cables used to interconnect other power cells were also tested. The rest of the parts were added after each test: ac side, dc side, above the PCB dc-bus electronics (GDs, sensors, UPS, etc.). Through the PD tests, it is confirmed that the complete power-cell maintains a PD-free condition until $V = 33.2 \text{kV}$, as shown in Fig. 4.8 (b). After these tests, it can be concluded that 4 of these power-cell units can be safely put in series without PD or insulation breakdowns when the frame and fans (they are part of the cabinet) are on earth (GND) potential, and the rest of the power-cell is on high voltage.
4.3.6 Digital Control System and Sensing

The conventional converter control and sensing system has been changed to overcome issues brought by the fast $dv/dt$ and $di/dt$ for SiC MOSFET applications [107]. The power cell digital control system, shown in Fig. 4.9, includes the local controller board, gate-drivers, and isolated digital sensors (IDS). Each of the three partitions has a main FPGA that handles all communications among them. All communications are realized with fiber optic cables (FOC) which have extremely high CM impedance. With this communication structure, CM noise can be greatly reduced, and noise related issues in the controllers can be significantly mitigated. The local controller is built on a popular MCU-and-FPGA based architecture. A Communication Network Interface (CNI) card is plugged onto the main controller. The CNI is connected to the MCU external memory bus, providing functionalities necessary to form an upper-level control network. Additional research in the area of distributed control systems is being conducted in [215]. The power supply voltage potential of the control board sits on the local ground which is the middle point of the dc bus. Low-profile isolated digital sensors (IDS) are developed for the current, voltage, and temperature, transmitting signals back to the controller with FOC [108]. The auxiliary power for the IDS uses the same type of converter as an eGD and is fed from WPT-APS. Piece-wise verification and basic functionality of the controller and sensors, as well as their accuracy, have already been presented in [107], [108], and thus omitted in this dissertation.

The architecture of the auxiliary power supply structure and circuits, such as the wireless power transfer auxiliary power supply (WPT-APS), charge and discharge, are explained in detail in [216, 217, 218]. All of the circuits passed basic functionality tests and required insulation level testing, thus will be omitted in this paper. The integrated shielded inductor is further elaborated in [219].
4.3.7 Switching, protection and reliability testing

Device Dynamic Characterization

Switching characterization is necessary during the power-cell piece-wise verification to verify the designed gate-driver performance and to obtain device dynamic characterization results if they are not known from the datasheet. Dynamic characterization of the switch was performed at 25 °C, 75 °C, and 125 °C to evaluate the switching performance. Critical parameters for the power-cell are switching losses and \( \frac{dv}{dt} \); these are necessary to know for cooling system design, SOA determination, noise-immunity, and insulation design. To ensure trustworthiness of the results, the developed HB power cell (shown in 4.3.8), with all of its parasitics, is used for dynamic characterization. Results are summarized in Section 3.4.
Losses vs Switching Speed Discussion

Ideally, $R_{g,\text{ext}} = 0 \, \Omega$ is desired to have the fastest switching speed and minimum switching losses since the highest gate driving current is provided. However, in practice, this is often difficult to implement due to tremendous ringing during transients and increased EMI related issues (\(dv/dt\) immunity of GD, cross-stalk, CM currents, EMI effect on sensors, etc.). Furthermore, parallel submodules current sharing is crucial to avoid hot spots and temperature imbalance among them. Thus, a proper $R_{g,\text{ext}}$ should be chosen, ensuring the converter’s highest possible efficiency, reliable operation, and balanced submodule currents. From previous discussions, with the decrease of $R_{g,\text{ext}}$, turn-on time is getting faster, as well as with increase of temperature, while possible $dv/dt$ related issues are getting worse. Considering that the GD has been designed to sustain beyond 100 V/ns, minimal $R_{g,\text{ext}}$ is possible. However, current sharing is getting progressively worse with reducing $R_{g,\text{ext}}$ and increasing temperature, as seen in Section 3.4.2. Therefore, the chosen resistance is $R_{g,\text{ext}} = 0.71 \, \Omega$ to ensure acceptable current sharing (difference <10\%) and low losses, while the expected $dv/dt \leq 100 \, \text{V/ns}$ in all cases. Moreover, lower values of $R_{g,\text{ext}}$ will further aid with Miller effect cross-talk suppression, further discussed in Section 4.4.3. Voltage overshoot, often one of the main restrictions in determining the switching speed, is not included in the switching speed discussion for two reasons: 1) extremely low PCB planar bus power loop inductance (only 8.8 nH), and 2) 4 kV margin from the rated voltage of the 10 kV SiC device.

Shortcircuit and Reliability Testing

The Rogowski coil-switch current measurement will be validated in subsection 4.4.5, and an accuracy investigation will be performed to observe the impact of severe $dv/dt$. The performance for over-current and short-circuit (SC) protection was already examined in
[31, 150, 220], showing ultra-fast fault detection of 86 ns. Thus, SC protection will not be further investigated in this work. PCB planar busbar reliability tests (thermal and SC) are currently in progress, showing sufficient robustness, and great potential for MV applications.

### 4.3.8 Power-Cell Integration and Prototype

With the previous tests successfully passed, the design and piece-wise verification of all parts of the power cell is done. The final assembly of the HB-PEBB is shown in Fig. 4.10 (a) with all of its constitutive parts.

Fig. 4.10 (b) shows the power cell enclosure with the indicated dimensions. The power stage interfaces are at the left side (DC) and right side (AC). The interface for the optical fiber connections is at the back side, and the front of the HB-PEBB is for the human-machine interface when developed. Designed in this manner, the HB-PEBB can sustain 30 kV CM voltage, 6.5 kV differential-mode (DM) voltage, and can be installed or replaced by plug and-play, which is highly desirable for maintenance or reconfiguration.

The next section discusses the details of the system-level verification for the power cell to verify the thermal model and performance, as well as EMI and efficiency performance.

### 4.4 Power-Cell-Level DAM

#### 4.4.1 System-level Testing of Power Cell

For MV high-power converters, a non-regenerative direct load test at rated power is challenging, due to the limited grid and load capabilities, and the huge energy expenditure. Regenerative or circulating power tests circulate rated power, only drawing the losses from
Figure 4.10: Photographs of the 10 kV SiC MOSFET-based half-bridge power cell. a) Power cell with constitutive parts outside enclosure. b) Power cell enclosure. Power density: 11.9 kW/L (195 W/in³), calculated based on maximum input values. Insulation assessment followed standard IEC 60664 to ensure PD free requirement.
the power source. A mirror converter (pumpback) test is utilized to verify the performance of the power cell at the rated power, having two identical HB power cells at the same dc bus voltage. The pumpback is chosen over the reactive test type, since the power cell operation has to be verified in both dc-dc and dc-ac conversion mode. The output current is controlled by adjusting the gating signals of the switches. Usually, the gate signals in one HB are generated by an open-loop control to achieve a desired output voltage, while the gate signals in the other HB are generated by a closed-loop current control to achieve a desired output current [221, 222, 223]. The pumpback test is summarized in four switching states, according to [112], shown in Fig. 4.11.

![Figure 4.11: Pumpback operation states. (a) State I - current rise. (b) State II - freewheeling. (c) State III - current drop. (d) State IV - freewheeling.](image)

During State I, the dc bus voltage is applied on the load inductor, increasing the output current. During State III, the negative the dc bus voltage is applied on the load inductor, decreasing the output current. During State II and State IV, the current flows through the inductor, as well as either two top or bottom switches, slowly decreasing due to resistance of the loop. As the output current changes significantly only in State I and State III, the time duration of these two switching states is controlled to regulate the output current to be as desired.
System-level Testing: Experimental Setup

Two developed power cells are put in a back-to-back manner, indicated in Fig. 4.12 (a), to evaluate the thermal performance and thermal model, EMI, and efficiency.

![Diagram](image)

**Figure 4.12:** Power stage pumpback. (a) Hardware prototype in back-to-back configuration utilizing two of the developed power cells. (b) Circuit diagram with measured waveforms. (c) Developed thermal model for FEA simulations.

For simplicity and to reduce the cost of the prototype, only one fan is installed, with the same characteristics as for only one power cell. This implies a change in cooling characteristics, due to a different cooling channel size and prolonged air duct. The air flow at the back heatsink side (air duct outlet) is measured by a Fluke 922, giving an average air flow of 13.23 m³/min, which presents a significant difference from 9.94 m³/min for a single power cell. To ensure the simulation model in use can represent the real test structure, the prolonged air duct has to be modeled. Because of the pressure drop along the air duct in the real setup, the compensated blower curve and its operation point are determined by the following. First, the heatsink is removed, and the average air flow measured at the outlet of the air duct is 14.12 m³/min. Based on the blower original operation curve (blue line) in Fig. 4.7 (b),
around 180 Pa pressure drops along the air duct. Therefore, during the FEA simulation, the blower operation curve is shifted down by 180 Pa, in order to compensate for such pressure loss, as demonstrated by the red line in Fig. 4.7 (b). As a result, after compensation, the simulation result shows that the fan should operate at the point around 13.62 m³/min and 250 Pa. The difference between the simulation and measurements in the air flow is less than 3 %, which indicates the fluid dynamic model in use is quite precise. The developed thermal model for the pumpback is indicated in Fig. 4.12 (c).

4.4.2 Thermal Characterization through Continuous Operation

In this section, thermal characterization through continuous operation of the power cell in the pumpback, will be performed. First, the SOA will be defined for the chosen cooling solution in a 50 % duty cycle, dc-dc converter operation, after which, a developed thermal model will be verified. This condition exhibits a non-uniform loss distribution which is inherently thermally worse, exhibiting higher power losses concentrated on a single switch in a HB, compared to uniform loss distribution in a line cycle for the dc-ac case.

Loss Assessment

To aid in defining the SOA and finding the thermal limit of the power cell, a loss model has to be developed. For a maximum allowable device junction temperature of 150 °C, taking into account the device characterization results at $V_{ds} = 6$ kV, $V_{gs} = 18$ V, $R_{g,ext} = 0.71$ Ω, and converter operation (dc-dc pumpback 50 % duty cycle), $P_{\text{loss}} = f(I_d, f_{sw})$ can be expressed as follows:

$$P_{\text{cond,1st}} = 0.032 \cdot I_d^2 [A] - 0.032 \cdot I_d [A] + 0.4 \ [W] \quad (4.3)$$

$$P_{\text{cond,3rd}} = 0.025 \cdot I_d^2 [A] - 0.022 \cdot I_d [A] + 0.5 \ [W] \quad (4.4)$$
\[
P_{\text{sw, on}} = (0.54 \cdot I_d [A] + 60) \cdot f_{\text{sw}} [kHz] \ [W] \quad (4.5)
\]
\[
P_{\text{sw, off}} = (0.055 \cdot I_d [A] + 0.32) \cdot f_{\text{sw}} [kHz] \ [W] \quad (4.6)
\]
where \( P_{\text{cond, 1st}} \) and \( P_{\text{cond, 3rd}} \) are the 1st and 3rd quadrant device conduction losses, respectively, expressed as a quadratic function of \( I_d \) as seen in Fig. 4.3. \( P_{\text{sw, on}} \) and \( P_{\text{sw, off}} \) are turn-on and turn-off switching losses, respectively, described as linear equations based on Fig. 3.30 (a), Fig. 3.30 (b), Fig. 3.30 (c). \( f_{\text{sw}} \) is switching frequency.

As indicated in Section 3.4, for Gen-3 10 kV SiC MOSFET dies, the body diode reverse recovery effect can be neglected. This completes the loss model, and it can now be utilized in order to find the thermal limit.

**Thermal Limit and Power-Cell Safe Operating Area**

Non-uniform loss distribution in the dc-dc pumpback will furthermore be influenced by different operation points - various \( f_{\text{sw}} \) and \( i_d \). As a result, different non-uniformity levels will define different thermal limits since the switches will not be loaded in the same manner, and the influence will change from one switch to another in the HB. The thermal limit will mostly be determined by the hard-switching position in a HB, due to the significant influence of switching losses, especially at higher frequencies. However, for the lower frequency - high current case, quadratic dependence of the conduction losses will lead to the soft switching position having a significant influence on the baseplate; thus junction temperature. Therefore, for unevenly distributed losses in the dc-dc pumpback, maximum losses have to be determined for each individual frequency. The developed loss model will be used to assign losses to each switch in the pumpback configuration to find out what are the maximum allowable losses for the hard-switching positions to reach 150 °C. Thermal limits under different switching frequencies will be determined through thermal FEA simulation with the
pumpback model developed in the previous section.

Non-homogeneous current sharing between submodules causes loss imbalance with higher losses in the module that takes more current. Consequently, this needs to be considered in defining the safe operating area. From Fig. 3.34 and Fig. 3.35, quadratic dependencies for turn-on current sharing are derived since the turn-off imbalance is almost negligible and can be ignored, and static current sharing will be relatively well balanced due to the positive temperature coefficient of the SiC MOSFETs. Based on the chosen $R_{g,ext} = 0.71 \, \Omega$ and defined maximum operation temperature of $150 \, ^\circ\text{C}$, the resulting imbalance during turn-on is

$$\Delta I_{d,\text{tot}} = \Delta I_{d,\text{res}} + \Delta I_{d,\text{temp}} = 10.7\% + 2.5\% = 13.2\% \quad (4.7)$$

where $\Delta I_{d,\text{res}}$ is the imbalance due to the chosen $R_{g,ext}$, and $\Delta I_{d,\text{temp}}$ due to the temperature effect. This imbalance will be incorporated into the simulation, where the middle submodule S2 will have higher turn-on power losses than S1 and S4 for $13.2\%$.

Table 4.2 shows the power of the switches in the power cells, which at certain frequency results in $150 \, ^\circ\text{C}$ with a total power per switch defined as follows:

$$P_{\text{tot,sn}} = P_{\text{cond,m}} + P_{\text{sw,\text{on}}} + P_{\text{sw,\text{off}}} \quad (4.8)$$

where $n$ defines the switch position in the pumpback, and $m$ defines the quadrant operation according to Fig. 4.12 (b).

Table 4.2 shows with increase in frequency, maximum current drops dramatically, while the maximum power loss allowed, decreases slowly. The decrease of the maximum power loss is a direct result of further pronounced non-uniform distributions having higher frequencies.
in the system, since the losses become more and more concentrated on the hard switching position. At 40 kHz, for only 1 A, the losses become so excessive for the designed cooling system that temperature rises to 159 °C. In all cases, the maximum junction temperature was on the submodule S2 due to loss imbalance with the maximum difference in all cases of $\Delta T_j \epsilon [1 ^\circ C–7 ^\circ C]$.

With thermal limits imposed by the defined cooling system, utilized device, and de-rating based on current sharing, the SOA can be assessed. Apart from these, the power cell SOA will be defined with maximum current carrying capability $I_{sys,\text{max}}$, minimum $f_{sw,\text{min}}$ and maximum $f_{sw,\text{max}}$ switching frequency. The power cell $I_{sys,\text{max}} = 84$ A is the limitation imposed by the busbar while $f_{sw,\text{min}} = 5$ kHz comes from the maximum allowable voltage ripple at the dc-link capacitors. The $f_{sw,\text{max}} = 40$ kHz limit comes from the maximum power that the GD power supply can provide. Fig. 4.13 presents the SOA of the converter, defining possible power cell continuous operation points.

---

### Table 4.2: Thermal Limits with Different Frequencies

<table>
<thead>
<tr>
<th>$f_{sw}$ [kHz]</th>
<th>$I_d$ [A]</th>
<th>$P_{tot,s1}$ [W]</th>
<th>$P_{tot,s2}$ [W]</th>
<th>$P_{tot,s3}$ [W]</th>
<th>$P_{tot,s4}$ [W]</th>
<th>$T_j$ [°C]</th>
</tr>
</thead>
<tbody>
<tr>
<td>5</td>
<td>180</td>
<td>1870</td>
<td>806</td>
<td>806</td>
<td>1870</td>
<td>150</td>
</tr>
<tr>
<td>10</td>
<td>136</td>
<td>2000</td>
<td>460</td>
<td>460</td>
<td>2000</td>
<td>149</td>
</tr>
<tr>
<td>15</td>
<td>100</td>
<td>2115</td>
<td>250</td>
<td>250</td>
<td>2115</td>
<td>149</td>
</tr>
<tr>
<td>20</td>
<td>70</td>
<td>2195</td>
<td>121</td>
<td>121</td>
<td>2195</td>
<td>149</td>
</tr>
<tr>
<td>25</td>
<td>45</td>
<td>2241</td>
<td>50</td>
<td>50</td>
<td>2241</td>
<td>150</td>
</tr>
<tr>
<td>30</td>
<td>24</td>
<td>2256</td>
<td>14</td>
<td>14</td>
<td>2256</td>
<td>149</td>
</tr>
<tr>
<td>35</td>
<td>7</td>
<td>2259</td>
<td>1</td>
<td>1</td>
<td>2259</td>
<td>151</td>
</tr>
<tr>
<td>40</td>
<td>1</td>
<td>2422</td>
<td>1</td>
<td>1</td>
<td>2422</td>
<td>159</td>
</tr>
</tbody>
</table>
Developed Thermal Model Verification

Based on Fig. 4.13, the chosen testing point to verify the power cell operation is described in Table 4.3. The pumpback prototype, shown in Fig. 4.12 (a), and the circuit with the indicated waveforms at Fig. 4.12 (b), have operated under 6 kV, 84 A, 10 kHz, circulating 252 kW power in the system for 2 h. The power-stage waveforms are shown in Fig. 4.14.

After the initial 20 minutes, the power cells and XHV-6 modules reached thermal steady-states, and the maximum baseplate temperatures measured are 72.9 °C and 64.5 °C for HB-I and HB-II, respectively, as shown in Fig. 4.15 (a) and Fig. 4.15 (b). The maximum junction temperatures are estimated to be $T_{j,s1} = 108°C$ and $T_{j,s1} = 100°C$, according to (4.9), based on the junction to case thermal resistance $R_{th,j-b,s1} = 0.026$ K/W provided by the manufacturer.

$$
\begin{align*}
T_{j,s1} &= P_{tot,s1} \cdot R_{th,j-b} + T_{b,bb1}, \\
T_{j,s4} &= P_{tot,s4} \cdot R_{th,j-b} + T_{b,bb2}. 
\end{align*}
$$

Comparing the two $T_b$ of the two power cells, the temperature is different for the same losses.
The reason is that the heat-source, dies of S4, for the HB-2 are physically farther from the edge of the base-plate (for around 15 %), where the temperature is measured. Therefore, it is reasonable that the temperature is lower. This can be confirmed through the simulation with the assigned switch losses listed in Table 4.4. The results in Fig. 4.15 (c) and Fig. 4.15 (d) show that the difference between the same two baseplate points matches the experimentally measured ones. The simulation model shows generally lower $T_{b, hb1}$ and $T_{b, hb2}$ than the experimentally measured ones. Differences between the simulation and experimental temperatures are between 4 – 8 °C. The different trend for submodule 2 (Sub-II) can be explained with Fig. 3.34 and Fig. 3.35, implying higher losses of SUB-II, due to higher current during the turn-on transition. Comparing $T_j$ between the simulation model and estimated value calculated with (4.9) shows a similar discrepancy as for $T_j$ of around 4 °C. For better insight into thermal model behavior and its accuracy, model $T_{b, sim}$ and $T_{j, sim}$ have been compared in multiple points to the measured $T_{b, meas}$ and estimated $T_{j, est}$ for HB-I; the

### Table 4.3: Parameters of the DC Pumpback Tests

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC-link voltage ($V_{dc}$)</td>
<td>6 kV</td>
</tr>
<tr>
<td>Phase current average value ($I_{ind}$)</td>
<td>84 A</td>
</tr>
<tr>
<td>Circulating power between HBs ($P_{cir}$)</td>
<td>252 kW</td>
</tr>
<tr>
<td>DUT switching frequency ($f_{sw}$)</td>
<td>10 kHz</td>
</tr>
<tr>
<td>DC-link capacitance, each ($C_{dc}$)</td>
<td>65 μF</td>
</tr>
<tr>
<td>Phase inductance ($L_{ph}$)</td>
<td>470 μH</td>
</tr>
<tr>
<td>Total external gate resistance ($R_{g, ext, ttl}$)</td>
<td>0.71 Ω for on and off</td>
</tr>
<tr>
<td>GDPS coupling capacitance ($C_{cp, pwr}$)</td>
<td>3.4 pF (meas.)</td>
</tr>
<tr>
<td>Ambient temperature ($T_a$)</td>
<td>23 °C</td>
</tr>
<tr>
<td>Airflow at the air-duct inlet</td>
<td>500 CFM @0.05 psi</td>
</tr>
<tr>
<td>Thermal resistance ($R_{th, j-b}$)</td>
<td>0.026 K/W (manuf.)</td>
</tr>
</tbody>
</table>
results are shown in Fig. 4.16. The model shows the same trends with the measurement and estimated values, with a maximum difference of 8 °C, which is acceptable, considering the complexity of the system and its cooling. From a practical standpoint, having a thermal model that is 90% accurate is extremely valuable, due to the difficulty developing models that are correct more than 95% in all possible scenarios. This inaccuracy should be carefully considered when assessing the developed SOA.

Table 4.4: Estimated Losses Distribution

<table>
<thead>
<tr>
<th>Losses @ 84 A 110°C, 10 kHz</th>
<th>Half-bridge I</th>
<th>Half-bridge II</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>S1</td>
<td>S2</td>
</tr>
<tr>
<td>$P_{\text{cond}}$ [W]</td>
<td>180</td>
<td>175</td>
</tr>
<tr>
<td>$P_{\text{sw, on}}$ [W]</td>
<td>1090</td>
<td>0</td>
</tr>
<tr>
<td>$P_{\text{sw, off}}$ [W]</td>
<td>51</td>
<td>0</td>
</tr>
</tbody>
</table>
Furthermore, the pumpback configuration is put into the dc-ac mode to verify the developed closed loop control algorithm and verify the power cell dc-ac operation. Since in dc-ac mode, losses in a line cycle are uniformly distributed over both switches for the same processing power of the cell as in the dc-dc case, the thermal-wise condition is inherently better. Therefore, the developed SOA will not be violated. Fig. 4.17 shows the power cell dc-ac closed-loop operation, for a step response current reference.
Figure 4.16: Multi-point thermal model verification. Results contain simulation and measurement for $T_b$ and simulation and estimation for $T_j$ for 5 kHz and 10 kHz. $T_{j, est}$ calculated according to equation (4.9).

4.4.3 EMI Characterization

From an HB-PEBB perspective, the most detrimental impact EMI-wise to a successful operation is $dV/dt$ related issues: cross-talk and gate-driver common-mode transient immunity. These issues are possible operation stoppers since they either cause partial shoot-through, a short circuit, or a control malfunction of the power cell.

Cross-talk Evaluation

The performance and effectiveness of the implemented active Miller-clamping circuit is shown in Fig. 4.14, where the described effect will be observed on the HB-I, bottom switch $V_{gs,s2}$. In the dc-dc pumpback, with the current direction indicated in Fig. 4.12 (b), all of the switching events in the HB-I are driven by the top switch. Under the extreme condition of a $v_{ds}$ slew rate of 102 V/ns for the turn-on event of S1, the cross-talk voltage spike on $V_{gs,s2}$ reached 0.3 V, which is considered safe; this is below the gate threshold voltage for all temperatures. Even though $R_{g,ext}$ is effectively bypassed, the increase in $\Delta V_{gs,s2}$ of 5.3 V exists mainly due
Figure 4.17: Power stage continuous dc-ac pumpback test waveforms with the inductor current step response from 40 Arms to 80 Arms at $V_{dc} = 6\,\text{kV}$, $f_{sw} = 10\,\text{kHz}$, $f_{line} = 60\,\text{Hz}$. [Probes]: Ch1: THDP0100 @100 MHz, Ch2: THDP0100 @100 MHz, Ch3: Tektronix A6303 @15 MHz, Ch4: TIVH08L+MMCX50 @250 MHz. [Time scale]: 5 ms/div.

The performance of the eGD that drives $S_1$ has been investigated at the rated condition and thermal steady-state. This particular switch position is hard-switched and on the jumping (ac) node, making that eGD most vulnerable to CM current. The developed gate-driver enables extremely fast switching transients.

**Gate-driver Common-mode Transient Immunity Evaluation**

The performance of the eGD that drives $S_1$ has been investigated at the rated condition and thermal steady-state. This particular switch position is hard-switched and on the jumping (ac) node, making that eGD most vulnerable to CM current. The developed gate-driver enables extremely fast switching transients.
The first step in evaluating the CM currents through the eGD will be with a commercial gate-driver power supply with indicated coupling capacitance as in Table 4.3. The primary side of this power supply will be referenced to the earth ground. These tests will be benchmarked. Later ones will incorporate the intended configuration of the HB-PEBB with a novel WPT-APS and novel current transformer-based gate-driver power supply (CT-based GDPS), in order to observe performance. No CM chokes were used during these tests.

Shown in Fig. 4.18, the hard-switching turn-on of $S_1$ is completed in 42.5 ns with a $v_{ds}$ slew rate of 102 V/ns. The $dv/dt$ transient produces a top-side total CM current $i_{cm,s1}$ of 320 mA peak without any CM chokes along the GDPS path. On the other hand, the hard-switching turn-off process in Fig. 4.19 demonstrates slower dynamics, with 108 ns switching time, and 38 V/ns slew rate causing $i_{cm,s1} = -140$ mA at first, before the resonance due to switching occurs. These values correspond to expected values, since the measured GDPS coupling capacitance is $C_{cp,pwr} = 3.4$ pF, as indicated in Table 4.3. According to the eGD design, part of this measured CM current should go through the signal circuitry, signal CM current $i_{cm,sig}$. Even though $i_{cm,sig}$ is inaccessible, the top-side power bus voltage $V_{3.3V}$ for signal processing is measured. It exhibits an exceptionally noise-free performance with a slight variation of $\Delta V_{3.3V} \leq 100$ mV for both turn-on and turn-off events, retaining its stable and clean performance upon the transients.

Additionally, 3 more test cases were performed. In Case 2, the commercial gate-driver power supply is exchanged with the in-house CT-based GDPS directly where the primary side is referenced to earth ground. In Case 3, the WPT-APS is inserted between the bench-top power supply and CT-based GDPS, where the primary side of the WPT-APS is referenced to earth ground, while the secondary is left floating. In Case 4, the WPT-APS is inserted between the bench-top power supply and CT-based GDPS, where the primary side of the WPT-APS is referenced to earth ground, while the secondary is tied to the local PEBB.
Figure 4.18: \(S_1\) and eGD performance at hard turn-on in the continuous pumpback test without CM chokes. [Probes]: Ch1: THDP0100 \(\oplus\)100 MHz, Ch2: TIVH08L+MMCX10 \(\oplus\)800 MHz, Ch3: 91550-1 \(\oplus\)10 kHz–100 MHz, Ch4: TIVH08L+MMCX50 \(\oplus\)250 MHz. [Time scale]: 250 ns/div.

ground. A summary of results comparing these to the benchmark test is shown in Fig. 4.20. For Case 2, with the simple change of power supply, the CT-based GDPS shows superiority since the CM current measured is lower, resulting in smaller barrier \(C_{io}\) capacitance. In Case 3, with the insertion of the WPT-APS, total barrier capacitance is expected to be lower, since the input-output capacitance of the WPT-APS and CT-based GDPS are in series. Based on the measurement, this is confirmed, since the CM current measured is lower than the previous case, and is around 216 mA. For Case 4, with tying the secondary side of the WTP-APS to local ground, the CM current jumped significantly to over 500 mA. However, even with this significant jump in CM current, this configuration is preferred due to benefits it brings such as the following. 1) The WPT-APS provides the necessary isolation for the HV-PEBB (secondary receiver side has to be tied to local ground to fix the potential). 2) CM current mostly circulates within the HV-PEBB and does not flow to earth ground, thus preventing possible disruptions of control. 3) By using a CT-based GDPS, CM currents are reduced as compared to a commercial power supply. 4) A CT-based GDPS enables multiple
This verifies that the 10 kV eGD and HB power cell have realized a CM noise transient immunity up to 102 V/ns. This gives a good estimation about power cell limits before implementing it on the converter level.

### 4.4.4 Efficiency Characterization

Constantly seeking high values, the crucial performance indicator of power electronics converters is efficiency. With the utilization of SiC MOSFETs in MV applications, this feature is available even in the high-frequency ($\geq 5$ kHz), hard-switching operation of the converter. Energy losses are always directly related to increased operation cost and environmental pollution, especially for converters of such power. For example, just a 1 % decrease in efficiency of the designed power cell, relates to 2.52 kW of additional losses. Therefore, high-efficiency of the power cell is essential to ensure converter-level best performance.
The efficiency of the power cell can be estimated since a complete characterization of the HB power cell has been performed (static, dynamic, and thermal). However, to fully investigate the performance of the HB power cell and validate the developed loss models and efficiency estimation, measurement of the efficiency should be completed. Since the classical electrical method of efficiency measurement by measuring input and output power cannot achieve the required accuracy, the focus is on thermal calorimetric efficiency measurement [224]. Even though it shows great potential and accuracy, developing such a complex experimental bench for the power cell of these ratings renders it difficult. As suggested by [221], converter efficiency can be assessed with high accuracy with the pumpback method directly, since the power supply only supports the losses of the system, which can be directly measured.

Fig. 4.21 shows the efficiency measurement process. To obtain accurate results, probe calibration, offset, and range adjustment are of most importance [225]. The measured values
are the input pumpback and HB-I output power. For the dc-dc converter case, the measured values are average on both the input and output. For the dc-ac case, the input values are average, while the output quantities should be rms. To know the losses of each power cell, the inductor power losses and loss distribution between power cells are necessary. The designed load inductor is in-house made, and all parameters are known, enabling loss estimation. Losses can be accurately calculated by the model described in [226], and [227], by knowing the inductor (output) average current, current ripple, frequency, and rise time. Parameter x, indicated in Fig. 4.21, represents the loss distribution between power cells, and it is determined according to the characterization of the power cells and for the dc-dc case, duty cycle.

Efficiency is measured for the d=50% dc-dc pumpback, at \( V_{ds} = 6 \text{kV} \) for \( f_{sw} \in [5 \text{kHz}, 10 \text{kHz}] \), after thermal steady-state is reached. Since \( d = 50\% \) and utilized power cells are identical (devices, \( R_{g,ext}, V_{gs}, \) etc.), the parameter \( x = 0.5 \). Fig. 4.22 shows estimated and measured efficiency of the HB-I. The HB-I losses include the device losses, bleeding/balancing resistor losses, gate-driver losses, and auxiliary circuit losses. To establish the credibility of the efficiency measurement, the accuracy of the efficiency measurement by incorporating probe inaccuracies has to be included. Indicated efficiency accuracy boundaries are calculated.
according to [225].

![Figure 4.22: Comparison between estimated and measured power cell efficiency for variable current range, $V_{ds} = 6$ kV, duty cycle $d = 50\%$ in dc-dc pumpback, at 5 kHz and 10 kHz.]

As shown in Fig. 4.22, the measured efficiency is close to the estimated value, with certain discrepancies existing. Discrepancies can be attributed to parts of the setup and their parasitics that were not considered (busbar, capacitors, connections, etc.,) as well as probes accuracy. The maximum discrepancy is in the order of 0.35\%, which verifies the accuracy of the developed loss model and gives confidence in the device characterization methodology and results. For tested conditions, not all output power ranges satisfy the desired efficiency of the power cell of $\eta \geq 99\%$. Based on the measured efficiency, for 5 kHz, this design specification is met after 60 kW with the peak efficiency of $\eta = 99.6\%$. For 10 kHz, $\eta \geq 99\%$ is met at powers higher than 110 kW with the peak efficiency of $\eta = 99.3\%$. The same efficiency measurement methodology can be applied for all cases of dc-dc (different duty cycles) and dc-ac conversion, where instead of average values, rms values will be considered.
In the HB-PEBB there exits a digital temperature, voltage, and current sensor as the RSCS on the GD. In this section, there will be a thorough investigation on the accuracy of the RSCS since it is directly impacted by the $dv/dt$.

First, the accuracy of the bottom switch of the RSCS will be investigated. Fig. 4.23 (a) shows the validation of the RSCS of one of the submodules, implying its potential accuracy. Fig. 4.23 (b) shows the validation of the summation circuit at 6 kV, 80 A, and 10 kHz. During the turn-on dynamic transition, the sensor exhibits only a 3 A error, which is not significant. This means that its information is useful and will be utilized later for peak current-mode control in the SCC. During the period when the device is turned on, drifting does exist ($\approx 3$ A), but that is expected since the offset voltage cannot be compensated completely. The drifting falls within $\pm 7.5$ A boundaries for all 3 RSCS. Additionally, the bottom switch RSCS is evaluated at the whole current range 10 A–85 A with different dc-bus voltages 1 kV–6 kV to investigate the accuracy. It was seen that the maximum error is $\pm 3.2$ A, and as expected, it does not exhibit $dv/dt$ dependency. This information during on-state can be successfully utilized for control purposes (average current-mode control) for both SCC and ICBT operation modes.
Regarding the top switch for the PCB-embedded RSCS, the necessity of an anticipated
shield (screen) against $dv/dt$ is proposed by Dr. Wang in [186] in 2016; however, it is
not experimentally proven. Compared to the shielded version, the non-shielded version is
less complex and cheaper, especially for MV applications due to stricter requirements for
clearance and creepage. From 2016, seven literature references [228, 229, 230, 231, 232, 233,
234] do not discuss the shield, and instead, propose the non-shielded version. Therefore,
the necessity of a $dv/dt$ shield will be independently checked through experimentation at
the turn-on of the top switch. Fig. 4.24 shows the results of the un-shielded Rogowski coil.
From Fig. 4.24 (c), it can clearly be seen that with increasing $dv/dt$, significant errors in
measured current exist and are rising linearly. The maximum error is 25 A for the measured
20 A at 100 V/ns, which renders this un-shielded coil unsuitable for these fast switching
applications with high $dv/dt$. The reason for this lies in the existence of the coupling
capacitance between the one turn conductor and the Rogowski coil which is sensing current
through that conductor. Excited by the high $dv/dt$, the high common mode current is
Slavko Moćević  

CHAPTER 4. SiC-based Power-Cell Design and Assessment

\[ i_{\text{CM,RSCS}} = C_{\text{CP}} \frac{dV_{\text{ds}}}{dt} \]

\( C_{\text{CP}} \) - lumped coupling capacitance

**Figure 4.25:** Impact of the induced common mode current noise to Rogowski Coil current sensing approach.

injected in the coil, disrupting the accurate information of the current.

To investigate the benefits and look into speculated elimination of the impact of the \( \frac{dv}{dt} \), the exact same experiments are repeated for the shielded version of the Rogowski coil board. The shielded Rogowski coil’s main goal is to bypass the injected common mode current away from the sensing circuitry to the MOSFET source potential, as shown in Fig. 4.25.

The shielded Rogowski coil results are shown in Fig. 4.26. From Fig. 4.26 (c), it can clearly be seen that the influence of the rising \( \frac{dv}{dt} \) is not completely eliminated, and errors in the measured current still exist. However, the maximum error is reduced 5 times, compared to the un-shielded version measured at 100 V/ns. Now, these results with shielded coils are much more acceptable and can be utilized for the necessary controls easily, but the inaccuracies and possibly resolving them on the main control-level must be kept in mind.

Furthermore, validation of the proposed peak current-mode integrated on the gate-driver (shown in Fig. 3.25) is required for the SCC. The peak-current mode performance of the
RSCS is verified in a single cell configuration, as shown in Fig. 4.27 (a) in continuous operation. Information about the enabled switching, average current or peak current-mode control, current boundaries, and faults are shared with the GD by the local controller via a developed communication protocol. Fig. 4.27 (b) shows the RSCS peak current-mode verification at 6 kV and 80 A where just one piece of the fundamental cycle is shown. The top and bottom switch current boundaries are set as 60 Adc with an addition of a sinusoidal 20 A peak with a frequency of 60 Hz. The switching moments are determined when the switch currents $I_{S1}$ and $I_{S2}$ reach preset current boundaries. The output current $I_{load}$ is indeed limited in the desired current boundaries, therefore effectively validating the performance of the RSCS.
Figure 4.27: Power-cell peak-current mode RSCS verification. (a) Test schematics and monitored waveforms. (b) Experimental RSCS verification at 6 kV and 80 A.

4.5 Summary

This chapter provides a systematic design and assessment methodology (DAM) with the overall framework, detailed considerations, and solutions to address the challenges in the MV power cell design, based on a 10 kV SiC MOSFET module. The whole methodology is bottom-up, from a component-level DAM to the power-cell level, featuring abundant verification work to reduce the chances of destruction. Critical insulation design considerations and testing procedures are described. Through insulation assessment procedures fully following the IEC 60664 standard, the partial-discharge-free operation for both internal and external insulation systems is confirmed at rated voltage of the power cell. A safe operating area is derived for a single dc-dc case with a duty cycle of 50 % for a designed cooling system. However, the described procedure will be the same for any other case either in dc-dc or dc-ac operation mode. The thermal model is 90 % accurate, showing an acceptable maximum dif-
ference of 8 °C, which considering the complexity of the system and its cooling is extremely valuable, proving the thermal modeling methodology. The designed enhanced gate-driver successfully deals with electromagnetic interference issues caused by having high slew rate voltage transients. The designed medium-voltage power cell for utilization in a modular multilevel converter application having the latest 10 kV SiC MOSFET half-bridge module, achieved a power density ≥ 11.9 kW/l, with measured peak efficiency of \( \eta = 99.6\% @5\text{kHz} \) and \( \eta = 99.3\% @10\text{kHz} \). The power cell successfully operated at \( V_{dc} = 6\text{kV} \), \( I = 84\text{A} \), \( f_{sw} \geq 5\text{kHz} \), \( T_j \leq 150^\circ\text{C} \), in both dc-dc and dc-ac mode, and had high switching speeds over 100 V/ns, exhibiting high transient immunity. Additionally, the RSCS accuracy was investigated, and it was concluded that the shielded version must be employed for a successful and relatively accurate current measurement.
Chapter 5

10 kV SiC MOSFET-based Modular, Scalable, High Power Density Converter for Medium Voltage Applications

5.1 Introduction

The simultaneously imposed challenges of high-voltage insulation, high dv/dt, high-switching frequency, fast protection, and thermal management associated with the adoption of the 10 kV SiC MOSFET, often pose nearly insurmountable barriers to potential users, undoubtedly hindering their penetration in medium-voltage (MV) power conversion markets. Key novel technologies such as the enhanced gate-driver, auxiliary power supply network, PCB planar dc-bus, and high-density inductor were already presented, enabling the SiC-based designs in MV converters to overcome the aforementioned challenges.

State-of-the-art converters in medium and high voltage applications are mostly multilevel, designed specifically to overcome the limitations of Si in terms of breakdown voltage, switching frequency, and efficiency. The most prominent voltage-source converter (VSC) topologies are the following: two-level with series-connected devices (SCD), multilevel-level neutral point -clamped (NPC), active neutral point clamped five-level (ANPC-5L) converter, cascaded H-bridge (CHB), flying capacitor converter (FCC), and modular multilevel converter (MMC). After the introduction of the MMC, it is increasingly considered in MV applications due to
its features of modularity and voltage scalability, transformerless operation (eliminates the need for galvanic isolation), high power quality, and resiliency. Its difficulties in operating at low line frequency and its inability to operate in dc mode have prevented its adoption in MV motor drive and grid applications. However, purely substituting an SiC design instead of Si-based ones in modular MV converters would yield only minor gains.

Therefore, to further elevate SiC-based designs, novel high-bandwidth control strategies, such as switching cycle control (SCC) and integrated capacitor-blocked transistor (ICBT), as well as a high-performance/high-bandwidth communication network, are developed. All of these technologies combined, will overcome barriers posed by state-of-the-art Si designs and unlock system level benefits such as very high power density, high-efficiency, fast dynamic response, unrestricted line frequency operation, and improved power quality. In this chapter, the development of a converter will be presented that demonstrates all of those benefits in its system operation - in both SCC and ICBT in dc-dc and dc-ac mode. It will have switching speeds (up to 100 V/ns per power-cell) and high-switching frequency (10 kHz), meanwhile exhibiting high common-mode transient immunity and high-efficiency.

5.2 Converter Integration based on 10 kV SiC MOSFET-based Power-cell

5.2.1 Modular Converter Architectures and Approach

As seen, there is a manifest lack of circuital solutions enabling the full utilization of SiC devices in MV applications. Keeping in mind that the maximum common-mode voltage insulation capability of the HB-PEBB is 33.2 kV, it would be completely safe to have a maximum 4 units put in series (in one converter arm) without insulation breakdown or
arching. Therefore, several potential topologies can be explored such as the following:

- A nine-level SCC converter can be achieved with only one phase leg constructed either as a step-down buck dc-dc converter or step-up boost dc-dc converter. For dc-ac applications, a single phase inverter is possible with 2 phase-legs as well as a three phase inverter with three phase legs.

- A two-level ICBT inverter for dc-ac applications can be achieved with having more than one phase leg. A buck or boost can be constructed if only one phase-leg is available.

- A three-level ICBT inverter can be constructed in an NPC configuration with the simple addition of diodes.

The converter built will be in a single-phase H-bridge configuration for the sake of cost mitigation and simplicity, without any detriment to its validity as a multi-phase circuit solution. With this configuration, the user can test and validate the following: SCC dc-dc operation in pump-back where one phase-leg will be buck and the other, boost; SCC dc-ac single phase operation, ICBT dc-dc operation in pump-back where one phase-leg will be buck and the other, boost; ICBT dc-ac single phase operation. ICBT will only be tested in a two-level configuration. The HB-PEBB design for converter-level verification will be built using Gen3 10 kV SiC MOSFET modules from Cree, and for cost control purposes, a reduced current module (40 A) will be utilized. Accordingly, the HB-PEBBs will be rated at 6kV, 28 Arms, with a target switching frequency $\geq 5$ kHz. The nominal specifications of all power converters, depending on the number of power cells, will be $V_{\text{rated}} = N \cdot 6\text{kV}$, $I_{\text{rated}} = 28\text{A}$, and $P_{\text{rated}} = N \cdot 6\text{kV} \cdot 28\text{A}$, where N is the number of utilized power cells in one arm.

Since a modular converter concept will be pursued, the desired converter will be built and
tested in stages from one-cell to four-cell per arm, in both SCC and ICBT, dc-dc and dc-ac modes, as shown in Fig. 5.1.

![Diagram showing pumpback configurations](image)

**Figure 5.1:** (a) One-cell-per-arm pumpback configuration. (b) Two-cell-per-arm pumpback configuration. (c) Three-cell-per-arm pumpback configuration. (d) Four-cell-per-arm pumpback configuration.

Starting from the one-cell-arm, the goal is to anticipate issues and challenges and clear them, meanwhile monitoring the most relevant waveforms such as dc-bus voltage, HB-PEBB dc-bus voltage and its balancing, HB-PEBB output and gate voltages, phase current, arm currents, switch currents, and HB-PEBB temperatures. In this dissertation, the results shown will be for the two-cell-per-arm case, and the solved implementation issues will be discussed for both one and two-cell-per-arm cases.
5.2.2 Power-cell Assembly and Qualification Study

Power-cell Assembly

To manufacture the modular converter consisting of multiple (in this case eight) HB-PEBB cells, a reliable in-house production assembly procedure is developed, consisting of twenty exact steps, as shown in Fig. 5.2.

The first step consists of assembling the aluminum frame which is part of the modular converter structure. It is important to short them to be at the same voltage potential, which will later be connected to Earth GND. Simply connecting them together will not be sufficient, since all of the aluminum bars are coated. Therefore, each aluminum bar is drilled and connected with screwed in wires. The next piece is assembling the black HB-PEBB holder board on top. In this step it is important to use Torlon screws in 4 corners, meanwhile avoiding metal screws. This pushes the GND potential further away from high voltage. The third step, as well as the first two, is a piece of the converter structure, comprising primarily of assembling the HB-PEBB cooling channel. In the process of assembly, polycarbonate screws

Figure 5.2: Twenty steps in MV HB-PEBB cell construction.
(not metal) are used, for the same reasons as previously mentioned. Step four consists of embedding the thermal couples into the heatsink. The aluminum heatsink was designed and manufactured to have channels for embedding the thermal couples. The location of these channels is in close proximity to the device baseplate. They are located between, and on the sides of the XHV-9 modules, resulting in a total of four channels for embedding eight thermal couples. To embed the thermal couples, the thermal epoxy MR 2000 from Loctite is used at 1000 °C, which cures in 7h. After the curing finishes, the heatsink is placed into a cooling channel. The next piece is the capacitor and MV connector holder, assembled relatively easy by being placed on top of the heatsink and screwed on with metal M6 screws. Since high-voltage operation of the MV converter is one of the crucial challenges, moving forward, it is decided for initial testing, that only one out of the three XHV-9 modules will be used in the HB-PEBB construction. The reason for this is fairly simple. Due to the limited number of highly priced XHV-9 SiC MOSFET modules, if any potential destructive event occurs, only one module would be destroyed instead of three as per the original design. This will give an additional buffer for repair and further testing after root-cause analysis. Hence, in step six only 1 CREE 10 kV XHV9 3 die per switch module is assembled. To help support the structure and for mechanical stability of the Rogowski coil board and gate-drivers, 2 "dummy" 3D printed modules were placed. The material used to print them is ABS plastic to increase the melting temperature compared to PLA plastic that is usually used. The thermal interface used is the indium thermal pad instead of classical thermal paste, since it has better thermal conductivity as long as enough pressure is ensured. Furthermore, it is a much cleaner approach. Step seven consists of placing the developed HB-PEBB inductor into the cell, interconnecting it between the ac terminal of the module and the HB-PEBB AC out terminal. The inductor shield is connected to the midpoint of the dc bus, through a series RC network for minimization of the CM currents. Prior to assembly, the inductor PDIV was tested, and it is confirmed that it is PD-free until roughly 4 kV peak, which is
sufficient considering it will see a maximum of ±3 kV in rated HB-PEBB operation. Step eight is assembly of the wireless power transfer auxiliary power supply (WPT-APS). For this piece, the receiver part must be assembled first into the holder after which the primary is assembled. Prior to assembly, the latest iteration of the WPT-APS is tested to obtain the PDIV. WPT-APS is PD-free under operation up to 30 kV. Step nine consists of the assembly of the pre-charge circuit. Step ten is tedious, and it is the assembly of the dc-bus with capacitors. One must make sure that 1) everything is aligned properly in order for the dc-bus to be screwed in the modules, and that the negative terminal of the dc-bus can be properly connected to the negative output terminal of HB-PEBB; 2) dc-capacitor cases should be tied to midpoint in order to fix their potential, preventing their floating; 3) heatsink should be tied to midpoint as well, 4) precharge + and - wires should be connected to the appropriate connections of the capacitors. Step eleven is simple and consists of placing the plastic component holder onto the dc-bus. Steps twelve and thirteen consist of placing the gate drivers and the current transformer-based power supply. One must make sure that the gate-drivers are properly plugged into the gate source terminals and Rogowski terminals, while being held from above with holders to prevent any mechanical instabilities. The next two steps consist of placing the voltage sensor and discharge circuit onto the holder. They must connect to the dc-bus at dedicated terminals so they can measure bus voltage and discharge the bus when required. Step sixteen consists of placing the uninterruptible power supply (UPS) bus. This board is currently not operating as an UPS, but rather just as a low voltage bus distribution, due to a thermal issue. Step seventeen is placing a temperature sensor on the component holder. After placing it, thermal couples should be numerated, soldered on the connectors, and attached to the temperature sensor. Step eighteen is simple and consists of placing the controller. The last two steps consist of placing the wiring, electrical, and optical. For the electrical wiring, the output of WPT-APS is connected to the UPS bus, while the other electronics are connected from there. One must make sure
the negative rail is referenced to the dc-bus midpoint to fix the voltage potential. The fully assembled HB-PEBB power-cell is shown in Fig. 5.3.

![Fully assembled HB-PEBB Power Cell](image)

(a) (b)

Figure 5.3: Fully assembled HB-PEBB Power Cell. (a) Side view. (b) Top view.

**Power-cell Qualifications**

The testing of MMC’s power-cells are essential to the successful performance and operation of a MMC converter [235]. The comprehensive testing and qualification of the MMC power-cell is required to ensure the robust operation of the MMC converter in both ICBT and SCC. Additionally, these comprehensive tests are desirable to potentially reveal problems that can be found at the power-cell level before assembling and testing the full converter, considering its complexity over one power-cell. A comprehensive test scheme should be devised in a way to qualify the HB-PEBB based on 10 kV SiC MOSFETs that includes thermal design, insulation design, and operation under high \( \frac{dv}{dt} \), component protection, and system protection.

Compared to lower voltage or Si design, the qualification of the MMC’s HB-PEBB based on 10 kV SiC MOSFETs is more crucial, considering the high HB-PEBB voltage and very
high $dv/dt$. These are simultaneously imposed to the HB-PEBB and failure to handle these issues can result in the catastrophic destruction of the power-cell, thus converter. The test scheme for the HB-PEBB based on 10 kV SiC MOSFETs should be able to provide a condition similar to the real condition, such as dc-voltage, device current, $dv/dt$, and so on. Specifically, the test scheme should fully validate its thermal performance, insulation design, and the capability to withstand high $dv/dt$ when the power-cell operates as part of an ICBT and SCC converter. For example, high $dv/dt$ can distort PWM signals and falsely trigger protections, and such issues should be found during qualification, rather than during converter testing when the system is more complex and there can potentially be influence from one cell to another.

Before the qualification procedure, each individual component should be tested and its functionality verified before the submodule assembly, including the gate driver, voltage sensor, temperature sensor, MOSFETs, inductor, wireless auxiliary supply, local controller, auxiliary circuits, and busbar. For example, initial tests are conducted to check the gate loop and gate driver functions, functionality of sensors, WPT-APS, etc. Components that are subjected to high-voltage should be checked for insulation robustness and basically checked until they are PD-free. Additionally, each power module should be checked for basic functionality on the curve tracer such as output, transconductance, threshold voltage, 3rd quadrant, and most importantly - breakdown voltage (leakage current) characteristics. These steps will further ensure a successful operation. After that, the power-cells should be assembled.

The proposed qualification test scheme for an SiC-based HB-PEBB is a seven-step process, shown on Fig. 5.4.

The seven steps are comprised of auxiliary power testing, blocking voltage test, pre-charge and dis-charge test, gate signals converter check, pulsing testing check, and the converter dc-dc and dc-ac continuous operation. The proposed test scheme does not require the typical
double pulse test (DPT) and short circuit test for each MOSFET, hence is much simpler, less time-consuming, and more efficient, which is important when many power-cells and converters need to be tested. It is acceptable to skip a short circuit test since the 10 kV/45 A SiC MOSFET and its package in the submodule have become a bit more mature. To qualify the assembled power-cell, the pumpback configuration, described in the previous chapter, will be utilized. One HB-PEBB is the older version, previously and completely tested with verified functionality, able to operate 6 kV, 84 A, 10 kHz - named testbed PEBB. The other one is the HB-PEBB under test for qualification which should be tested under hard-switching conditions, under high $dv/dt$ operating at maximum 6 kV, 28 A, 10 kHz, meanwhile not exceeding 150 °C - named DUT PEBB.

The first step is to check if all auxiliary are working together powered from the WPT-APS. It is left operating for 2h in order to make sure there are no thermal instabilities while driving the gate drivers with 10 kHz switching frequency, without any main power. The second step, named the blocking voltage test, is conducted in order to make sure that the assembled HB-PEBB can successfully hold the rated operation voltage and does not exhibit any E-field issues. Tests are conducted from 1 kV to 6 kV, and in each operation point, is left a minimum

Figure 5.4: Power-cell qualification steps.
15 min. The next step is testing pre-charge and dis-charge circuit functionalities. Tests are conducted from 1 kV to 6 kV, charging and discharging the cell. Before going into the pulsing and continuous operation check, the communication and gate-driver signals are thoroughly checked to ensure the devices will be switched successfully, and that two power-cells will have the required phase delay (as described in Section 4.4). Step five is the pulsing check, very similar to the basic double pulse test, but it is done while the system is configured in the pumpback configuration. Tests are conducted from 1 kV to 6 kV, changing switching currents from $-30$ A to 30 A. The purpose is to ensure that all devices can switch, and the gate-drivers are operating successfully up to the rated voltage and current of the HB-PEBB.

The sixth step is the most crucial one. It is the continuous dc-dc pumpback where the DUT PEBB will ultimately operate under its rated conditions of 6 kV, 28 A, switching at 10 kHz, with an elevated junction temperature, having $dv/dt \approx 100$ V/ns. Tests will start again at 1 kV to 6 kV, changing switching currents from 5 A to 28 A, measuring the temperature throughout with both thermal camera and thermal couples, simultaneously, to ensure that there will be no thermal instabilities. Furthermore, the power source current and voltage will be monitored as well, so the losses can be estimated to estimate junction temperature and efficiency. The seventh step, and last one, is repeating the sixth step, just for the ac output current. Representative current waveforms for the HB-PEBB 2 are shown in Fig. 5.5. The system operated for 2 h until it reached thermal equilibrium in each dc-dc and dc-ac case. Maximum $dv/dt$ was 105 V/ns during turn-on, maximum baseplate temperature measured was 41.1 °C, which based on the measured HB-PEBB losses and known junction-to-baseplate thermal resistance of $R_{th,j-b} = 0.156$ K/W results in an estimated junction temperature of $T_j = 86$ °C. These comprehensive tests show that the designed and manufactured power-cell can successfully overcome the challenges of medium-voltage, thermal management and operation under high $dv/dt$. With these, the HB-PEBB can successfully be integrated into the converter structure.
Additionally, close attention should be paid towards the consistency of results and their distribution between the different HB-PEBBs. Results that will be compared are $dv/dt$ during on ($dv/dt_{on}$) and off ($dv/dt_{off}$) transitions, maximum baseplate temperature ($T_{base}$), losses ($P_{loss}$), and estimated junction temperatures ($T_j$). These results can potentially reveal additional issues such as large differences between HB-PEBB losses, higher temperatures, significantly different $dv/dt$ which can potentially be problematic when implementing ICBT control, etc. Results shown in Fig. 5.6 shows the distribution of results for 16 different HB-PEBBs with indicated mean ($\mu$) and standard deviation values ($\sigma$).

Fig. 5.6 indicates that the distribution of parameters for all of the HB-PEBBs are very close to each other in all relevant characteristics. Most of them fall within one standard deviation, or are very close to that boundary. One HB-PEBB (PEBB5) exhibits lower switching speeds ($dv/dt_{off} = 51 \text{ V/ns}$, $dv/dt_{on} = 86 \text{ V/ns}$) resulting in higher losses ($P_{loss} = 428 \text{ W}$) giving elevated baseplate ($T_{base} = 41.3 \degree\text{C}$) and junction temperature ($T_j = 101 \degree\text{C}$). This HB-PEBB can potentially be excluded from the converter integration, due to different performance than
5.2.3 DC-bus Assembly

Keeping in mind the desired high power density and intended application of the HB-PEBB (SCC mode MMC converter and ICBT) through the simulation study, it is confirmed that the minimum capacitor bank required should be $C_{dc} \geq 1 \mu F$. Thanks to the mature PCB industry, a 24kV PCB based laminated bus can be fabricated, ensuring low parasitic in-

the others which could potentially bring issues, especially when all three XHV-9 modules will eventually be put in the HB-PEBB. This distribution of data, especially regarding the $dv/dt_{on}$ and $dv/dt_{off}$, could help in better pairing of HB-PEBBs for ICBT operation, since the requirement for that control is very synchronized switching within the same cells in an arm.
ductance and high PD inception voltage. However, the approach will be slightly changed compared to the HB-PEBB dc-bus. A complete dc-bus will be constructed based on the planar 24 kV PCB motherboard, where eight 3 kV PCB daughtercards carrying dc-bus capacitance will be inserted in series to achieve the desired capacitance and to reach the desired voltage [236]. This idea is shown in Fig. 5.7 (a).

![Diagram of 24 kV PCB-based Bus Motherboard](image)

**Figure 5.7:** (a) 24 kV dc-bus 3D design with indicated dimensions. (b) Cross section of the developed dc-bus with indicated layers. (c) DC-bus assembly hardware.

PCB designs exhibit very accurate metal and insulation fabrication, enabling the implementation of multiple E-field management methods during design. The same FEA simulation techniques applied to the study and design of the 6 kV HB-PEBB dc-bus [207] can be translated and utilized for 24 kV. Once E-field distribution analysis is completed one by one,
for all of the critical regions, the maximum E-field intensity inside the PCB is lower than 20 kV/mm with no more than 2 kV/mm in air around it in the final design. The layer breakdown for the PCB dc-bus motherboard is shown in Fig. 5.7 (b). The full bus voltage is split between 9 potentials (including earth GND - 0 V) so that the maximum differential between any two adjacent layers is still 3 kV. Considering the full converter assembly, several aluminum frames referenced to GND (part of the modular converter structure) will be in close proximity to the dc-bus. To increase flexibility with the converter assembly, the 0 V layers were placed as the outer most planes with the 24 kV layer in the middle. In total, the final board is 22 layers and 10.8 mm thick. PCB daughtercards with a metallized polypropylene film capacitor design are selected instead of utilizing can film capacitor solutions. This is due to the benefits of reduced ESL by 88%, footprint by 66%, and volume by 80%. A 3 kV capacitor board will be built using 2 series, 3 parallel 1.5 kV, 6 µF film capacitors from Kemet (C4AQSBW4600A3FJ).

The complete converter level DC-bus assembly is shown in Fig. 5.7 (c) where each phase leg has one DC-bus with capacitance 1.1 µF and are interconnected in parallel. This 2 dc-bus in parallel approach is chosen over a single one due to practicality in terms of cost and size. The converter level DC-bus assembly consists of the following: 1) Aluminum frame railings which are part of the modular structure interlocking with the HB-PEBBs. This part also contains Delrin boards on which the dc-bus container will be mounted. 2) A container for the DC bus mounted on and strapped to Delrin boards with non-conductive materials, as a result of the close proximity with the dc-bus. Due to the large size of the container, it could not have been built from a single piece, but rather from 6 individual pieces that are connected with strong epoxy and plastic reinforcement rods. 3) There are two 24 kV dc-bus motherboards, each having 8x3 kV PCB daughtercards. 4) There are interconnections between the dc-bus motherboards. Due to high voltage, plastic standoff was inserted to create necessary
support and provide the required distance (set distance is 15 cm). 5) Metal parts of the HV connectors that distribute the voltage to HB-PEBBs are on the same potential as the wire to avoid floating potentials. 6) Input connectors are connected with the DC-bus with wires, as well as with 14 AWG wire, since only system losses will be provided.

PD tests are done in accordance to guidelines provided in Section 4.3.3. Following is a brief summary of the critical PD results: 1) Each layer of the dc-bus has $PDIV > 3 \text{kV}$ ($PDIV_{\text{min}} = 5.4 \text{kV}$). 2) There is PDIV between the positive and negative terminal of the dc-bus $PDIV = 28.6 \text{kV}$. 3) The daughtercard design has $PDIV > 3 \text{kV}$ (Corona Inception/Flashover Voltage 7.8 kV). 4) For the dc-bus assembly (motherboard + daughtercards), $PDIV = 27.3 \text{kV}$. The daughtercards are raised for 3 mm with additional spacers due to initial flashover occurring at 18 kV. 5) ± DC terminals (multiple rings and cutouts added to increase creepage between connectors) have $PDIV = 29.32 \text{kV}$. 6) The complete dc-bus assembly from Fig. 5.7 (c) is PD-free @ 24 kV in both the AC test and DC Hipot tests. After that, dc-bus voltage was increased to $V_{\text{rated}} + 0.1 \cdot V_{\text{rated}} = 26.4 \text{kV}$ and held for one hour, and no flashovers or breakdown issues were observed.

5.2.4 High-Speed, High-Performance Communication Network

The high switching frequency and modularity jointly present a significant challenge to the communication and control systems implemented in modular converters. For these converters, distributed control with high scalability is preferred [237]. Emerging large-scale modular converters are pursuing high-performance distributed control systems (DCSs) that feature minimal synchronization accuracy (SA), high data rate, and advanced control schemes [238, 239]. The following discussion presents the effective synchronization techniques that tackle this challenge, particularly the CPES PESNet, which has evolved from its first gener-
ation in 1999 to PESNet 3.0 today. PESNet 3.0 achieves a ±1 ms SA, 300 ns node-to-node latency, and reinforced resilience with a novel network topology. More details about distribution, control layer partition and its mapping, with physical control hardware, synchronization, and temporal sequencing can be found in [240].

**Inter-PEBB Layer**

The power electronics system network (PESNet) 3.0 is a next-generation communication network designed and optimized for DCSs [241]. Accompanied by the growing availability of MV wide-bandgap devices, fast-switching-enabled novel control schemes raise a high SA requirement for PESNet 3.0 [125, 128]. PESNet 3.0 contains an Inter-PEBB layer and an inner-cell layer. A custom-made controller supporting PESNet 3.0 is shown in Fig. 5.8 (a). The White Rabbit technology, originally developed for the Large Hadron Collider accelerator chain at the European Organization for Nuclear Research [242, 243], has been embedded in the PESNet 3.0 Inter-PEBB layer to achieve a Sub-nanosecond (sub-ns) SA for distributed power conversion systems for the first time. The PESNet 3.0 Inter-PEBB layer contains the main controller and cell controllers. They share the same hardware using the high-end Xilinx 7000 as the control device and communicate in a tree topology with a 5 Gbps data rate. Sub-ns SA is achieved by utilizing a PLL on the controllers to lock both the frequency and phase of the local time with each other.

To evaluate the PESNet 3.0 Inter-PEBB layer synchronization performance, a communication network is built, shown in Fig. 5.8 (b). A local time counter is generated based on each controller’s own clock. A square wave based on the local time counter is utilized to measure the SA, as shown in Fig. 5.8 (c). The channel-to-channel delay measurement data is further extracted from the oscilloscope, as shown in Fig. 5.8 (d). Setting the main controller as the benchmark, all of the measurement data for the 16 cell controllers are within ±0.5 ns, which
verifies the sub-ns SA.

Figure 5.8: (a) Controller prototype. (b) PESNet 3.0 Inter-PEBB layer with 17 controllers in a tree topology. Controller 0 is the main, and 1 to 16 are the cell controllers. (c) Synchronization test waveform for the main and 7 cell controllers. This test is repeated with the other 9 cell controllers. (d) Synchronization accuracy distribution referred to the benchmark main controller for all the 16 cell controllers.

Inside-PEBB Layer

Apart from communicating with other controllers in the Inter-PEBB layer, the HP-PEBB controller is simultaneously communicating with the digital voltage and temperature sensor, and two eGDs forming an Inside-PEBB layer, as shown in Fig. 5.9 (a). A clock for synchronization purposes is physically distributed between the controller and eGDs using an additional fiber optic transceiver, achieving excellent synchronization using relatively inexpensive communication hardware. Regarding the communication protocol, it is heavily influenced by 10BASE-T Ethernet and EtherCAT [244, 245, 246]. By reducing the minimum payload size (12 octets) and doubling the speed (25Mbps), the communication is improved in order for required data to be exchanged within one control cycle (switching cycle). Research [215, 239] heavily influenced communication and synchronization development as well. The developed communication protocol is utilized for both sending (duty cycle, current reference, dynamic dead-time, phase shift, etc.) and receiving information (current, voltage, temperature, short-circuit faults, communication errors, etc.). To prevent data corruption
during switching instances due to high conductive and radiated EMI noise, communication transmission pauses in those transitions for $\approx 2 \mu s$.

![Diagram](image)

**Figure 5.9:** (a) Inside-PEBB communication layer. (b) Testbed for synchronization verification. (c) Synchronization test waveform for four eGDs.

To verify communication and synchronization, a testbed (shown in the Fig. 5.9 (b)), is built consisting of a main controller communicating with two HB-PEBB controllers, and each is communicating with two eGDs. The eGD’s task is to generate a synchronization pulse at a defining moment if communication and synchronization are successful. Fig. 5.9 (c) shows that synchronization pulses are within $\pm 1$ ns, which further verifies the sub-ns SA. Consequently, all actions at any moment will happen synchronously across all of the communication network.

### 5.2.5 High-bandwidth Control Methodologies

**Integrated Capacitor-Blocked Transistor Control**

The ICBT converter [127] provides another solution to achieve high power density with modular MV converters. An ICBT-based converter arm consists of multiple series-connected ICBT cells, similar to a converter arm in MMCs, except that the arm inductor is eliminated. ICBT-based converters have modularity and scalability features like MMCs. The configura-
tion of an ICBT cell is the same as the HB-PEBB of MMCs proposed in Fig. 4.1, except the inductor will be bypassed.

Unlike the control for MMCs, the ICBT-based converters have a simple control principle. The HB-PEBBs in the same arm operate synchronously, and the HB-PEBBs in the opposite arms operate complementary. As shown in Fig. 5.10 (a) for a two-cell-per-arm configuration, when the bottom switch is on, the HB-PEBB is in the on-state and can conduct a bidirectional current. When the top switch is on, the HB-PEBB capacitor is connected in series with the other HB-PEBB capacitors in the same arm, and together to the converter dc bus. Due to only parasitic inductance in the arm, the arm current reduces rapidly to zero, and the cells block the converter dc-bus voltage, as shown in Fig. 5.10 (b). This is the off-state of the HB-PEBB and the consecutive converter arm. As a result of low HB-PEBB capacitor currents, the HB-PEBB capacitor voltages have low ripples, largely reducing the requirement.
of capacitances in both dc and ac applications.

The capacitor voltage balance is critical, ensuring the safe operation of all switching devices and HB-PEBB capacitors. The existence of parasitic capacitance between the device terminals and corresponding heatsinks can compromise the HB-PEBB voltage balance [247]. During the fast switching transients, the parasitic capacitors are subjected to fast voltage change, resulting in charging or discharging currents through them. Although the magnitudes of those currents are small, they cause the HB-PEBBs with synchronous control signals to operate with different switching speeds, leading to capacitor voltage difference. The voltage difference develops slowly but will accumulate over time, thus has to be controlled. The HB-PEBB capacitor voltage control [128] can be achieved by applying delays to gate signals to some of the series-connected ICBT cells, forcing different cell capacitor currents for short periods of time during switching transitions. The closed-loop control requires the sensing of cell capacitors and phase leg output current.

**Switching-Cycle Control**

To possibly overcome the MMC conventional control drawbacks of large capacitor voltage ripple, existing attenuation approaches such as the second order or high-frequency harmonic injections are designed, based on average models limiting the achievable performance [248, 249]. The proposed switching-cycle control (SCC) [125] aims to greatly increase the control time resolution and form the control in the timescale of a switching-cycle. This critical alternation equips the MMC with the capability to achieve voltage balancing in a single switching-cycle, shifting the MMC from a long-deemed ‘line-cycle balancing’ converter to a ‘switching-cycle balancing’ converter.

The key reason for the large capacitor voltage deviation in the conventional control is that
the arm currents have the same value in one switching period, accumulating voltage deviations in the same direction. To prevent this, it is necessary to meaningfully re-assign arm currents within one switching period instead of keeping the same value. With that, the capacitor voltages can be balanced in a single switching period with the derived arm current patterns, preventing capacitor voltage deviations, as shown in Fig. 5.11 for a two-cell-per-arm converter. To achieve this arm current pattern, the switching actions between the upper and lower arm cells are not complimentary as in the conventional control. Instead, a delay is applied on the cell output voltages to create ‘shoot-through’ periods inducing high \( \frac{di}{dt} \), instantly shaping the arm current. By adjusting the duration of the ‘shoot-through’ periods, arm currents can be arbitrarily shaped. Current boundaries can be derived from closed loop control based on phase current and capacitor voltage imbalance. Peak current
mode (PCM) modulation is used to determine the duration of the shoot-through periods. It is worth mentioning that due to the inserted ‘shoot-through’ periods, an additional voltage level is observed on the output voltage. In contrast to the conventional control, since there is no capacitor voltage deviation by the end of the switching period, this makes the dc-dc operation of the MMC possible. Furthermore, due to the zero-voltage switching, the turn-on loss is nearly eliminated, reducing the total losses compared to the classic control methodologies.

5.3 Converter Prototype and Experimental Validations

5.3.1 Prototype

Eight out of sixteen qualified 10 kV SiC MOSFET-based HB-PEBBs are chosen for constructing the two-cell-per-arm, two phase-leg, modular, scalable converter custom-built prototype. The schematic of the setup is shown in Fig. 5.12 (a), and the prototype is shown in Fig. 5.12 (b). The distributed control system as described is adopted, forming a tree topology with one primary (master) main controller and 8 secondary (slave) PEBB controllers. The experimental setup is capable of operating at a maximum 12 kV dc-bus. Again, two phase legs will be operated in a pumpback configuration to relax the required active power drawn from the high voltage dc source. The power-cell has a minimal \( C_{\text{cell}} = 32.5 \mu \text{F} \) capacitance. Regarding the magnetics in the system, the load inductor is \( L_{\text{load}} = 3 \text{ mH} \), able to operate at max 24 kV, up to 125 A without saturation. The additional arm inductance is designed as \( L_{\text{arm}} = 160 \mu \text{H} \) to ensure the total duration of the ‘shoot-through’ periods is shorter than 10% of a switching period in SCC. These arm inductors will be submerged into an oil tank in order to achieve converter rated voltage operation. Unlike for the SCC, arm
inductor components are not required in ICBT based converters. These arm inductors have to be removed/bypassed in the ICBT, and in that case, the remaining arm inductance will be parasitic from the PEBB and dc-bus interconnections, which is estimated to be around \( L_{\text{para}} = 2 \mu \text{H} \) per converter arm. Between the power source and converter, a filter stage is inserted for 2 reasons. Firstly, the purpose of the insertion of differential and common-mode filters is to break the input ground loop of the power supply in case of ground-fault which should significantly reduce ground currents, potentially saving the equipment. Secondly, CM filters are necessary to prevent source over-current faults, due to high \( dv/dt \) in the system. A common mode choke is custom-built with a nano-crystalline core. It is important there be sectional winding instead of bi-filar in order to achieve high-voltage and be PD-free. Additionally, low voltage 48 V auxiliary power is supplied with a Meanwell RST-10000 power supply. The key specifications are summarized in Table 5.1.

![Diagram](image)

**Figure 5.12:** (a) Modular converter pump-back test configuration schematic diagram. (b) Prototype of 10 kV SiC MOSFET-based two-cell-per-arm converter in pump-back test configuration.

As mentioned previously, the cooling system per cell was redesigned from the one utilized in Chapter 4. Instead of utilizing a huge AC fan to cool 2 cells, push-pull arrays of dc-
Table 5.1: Parameters of the MV Converter in Pumpback Configuration

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell Capacitance</td>
<td>$C_{cell}$</td>
<td>$32.5 \mu F$</td>
</tr>
<tr>
<td>DC-link Capacitance</td>
<td>$C_{dc}$</td>
<td>$2.2 \mu F$</td>
</tr>
<tr>
<td>DC-link Voltage</td>
<td>$V_{dc}$</td>
<td>$6 \text{kV}; 12 \text{kV}$</td>
</tr>
<tr>
<td>Maximum Output Current</td>
<td>$i_L$</td>
<td>$28 \text{A}$</td>
</tr>
<tr>
<td>Arm Inductance</td>
<td>$L_{arm,sc};L_{para,icbt}$</td>
<td>$160 \mu H; 2 \mu H$</td>
</tr>
<tr>
<td>Load Inductance</td>
<td>$L_{load}$</td>
<td>$3 \text{mH}$</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>$F_{sw}$</td>
<td>$10 \text{kHz}$</td>
</tr>
<tr>
<td>Ambient temperature</td>
<td>$T_a$</td>
<td>$23 \degree C$</td>
</tr>
<tr>
<td>Power Source (a.l.e. systems model 303)</td>
<td>$P_s; V_s$</td>
<td>$100 \text{kW}; 30 \text{kV}$</td>
</tr>
<tr>
<td>Filter Resistor</td>
<td>$R_f$</td>
<td>$100 \Omega$</td>
</tr>
<tr>
<td>Filter Choke</td>
<td>$L_f$</td>
<td>$6.1 \text{mH}$</td>
</tr>
<tr>
<td>Auxiliary Power</td>
<td>$P_{aux}; V_{aux}$</td>
<td>$10 \text{kW}; 48 \text{V}$</td>
</tr>
</tbody>
</table>

fans are installed to achieve similar air-flow and cooling characteristics. The arrays consist of 6 dc-fans working in parallel. Each fan (OD8038-48HBXE10A) is supplied with 48 V, with power of 55 W, spinning with 13 500 RPM, having air flow of 141.2 CFM. Two arrays were installed per cell, push-and-pull, as indicated in Fig. 5.13 (a). Converter level cooling under full-power operation should be handled as indicated in Fig. 5.13 (b). Mixing of the cold (room temperature) and hot air is prevented in this way, by taking hot air through a modular pipe system (mounted on the pull fan array) to the ventilation system directly. Fig. 5.13 (c) shows the current state of the backside of the converter, indicating how the low voltage distribution was routed. Currently, there is no modular pipe system mounted, since only one out of three XHV9 modules is being used, meaning that generated heat is not as severe and is not needed to be extracted thorough them.
5.3.2 Experimental Validations

For both ICBT and SCC, results shown will be at 6 kV and 12 kV for both dc/dc and dc/ac conversion modes. Results on 6 kV, which is half the rated voltage, will be shown in order to display all relevant measured waveforms, since they cannot be measured on rated voltage due to high common-mode voltages. Only the bottom cell (L2A and L2B) output voltage is measured once the dc-bus values exceed 6 kV. Results on 12 kV will verify the proposed conversion methods. Current probes used are the Tektronix A6303+TM502A @ 15 MHz. Two of them measuring bottom arm currents in two phase legs, are placed bellow cell $L_{2A}$ to avoid any CM voltage issues. The one that is measuring the inductor (or output) current is placed at the output of the phase leg A. This probe is submerged into the oil container in order to resolve issues of breakdown with high voltage swings, since the probe can only sustain 600 V with the bare conductor. To measure output cell voltages, two different types of differential probes are used. The first type is the same as previously utilized, the Tektronix THDP0100 @100 MHz, able to measure up to 6 kV DM voltage, meanwhile able to sustain up to the same CM voltage. The second type used is the Powertek DP-40k, which according
to the datasheet, is able to measure ±20 kV DM voltage and able to sustain 10 kV maximum CM voltage to ground. However, to ensure that cell voltages do not diverge and to quantify balancing effectiveness, the HB-PEBB internal voltage sensor information will be monitored and utilized for control purposes through a high-speed, high-performance communication network. This information will be sampled once per switching cycle. The same is true for the temperature sensor and current shunt sensor.

**Integrated Capacitor-Blocked Transistor Control**

Since ICBT does not require them for operation, the arm inductors were bypassed. First, the dc-dc operation mode will be explored. The two switching cycle testing results under 6 kV dc-link with output voltage reference of 3 kV, and output current reference of $i_L = 25$ A are shown in Fig. 5.14 (a). The waveforms from top to bottom are phase leg A cell L1/L2 output voltage ($V_{L1A}$, $V_{L2A}$), cell U1/U2 output voltage ($V_{U1A}$, $V_{U2A}$), arm and output currents ($i_{UA}$, $i_{BA}$, and $i_L$), and the output voltage ($V_{out,A}$). The operation of the ICBT is successful in the dc-dc mode, resembling the 2 level converter operation with minor differences, mostly related to arm currents. Due to the existence of parasitic inductances $L_{\text{para}}$ in the loops, the arm currents are not perfectly rectangular and have a slight sinusoidal response as a result of the resonance of $L_{\text{para}}$ with the system capacitances. Regarding the voltage balancing, the power-cells are very well balanced with negligible differences of less than 40 V, which potentially could be gain differences between the probes. The system successfully operates and is able to control the current under different duty cycles, maintaining great voltage balancing. Fig. 5.14 (b) shows the results at the 12 kV dc-link with output voltage reference of 6 kV, and output current reference of $i_L = 25$ A, verifying that the converter works at rated voltage for the 2-cell per arm. Regarding the voltage balancing in this case, the power-cells are very well balanced with minor differences of a maximum 40 V, which is again, superb.
Figure 5.14: (a) ICBT dc-dc operation mode having 6 kV dc-link with $V_{\text{out}} = 3$ kV, $i_L = 25$ A. (b) ICBT dc-dc operation mode having 12 kV dc-link with $V_{\text{out}} = 6$ kV, $i_L = 25$ A, where power-cell voltages were collected through communication network.

Regarding the dc-ac operation mode, 60 Hz line cycle testing results under 12 kV dc-link with output current reference of $i_L = 26$ A are shown in Fig. 5.15 (a), demonstrating the successful operation at rated voltage for the 2-cell per arm. Regarding the voltage balancing in this case, shown in Fig. 5.15 (b), the power-cells are very well balanced, exhibiting only minor line frequency ripple of 45 V. Additionally, during zero-crossing of the current, minimal spikes in the phase leg A arm currents are observed, showing that sub-ns SA between the cells is achieved. Thus, the distributed communication network PESNet 3.0 with sub-ns SA is successfully demonstrated on the modular converter. Regarding the inductor current shape, it is much better (more sinusoidal - lower THD) compared to the SCC; however, non-idealities do exist due to the generally small inductive load, and minor control imperfections.
Figure 5.15: (a) ICBT dc-ac operation mode having 12 kV dc-link with variable duty cycle, $i_L = 26$ A. (b) Power-cell voltages collected through communication network.

Switching Cycle Control

Fig. 5.16 demonstrates the successful dc-dc operation modes of SCC in the converter prototype and validates the effectiveness of the proposed control. Two switching cycle testing results under 6 kV dc-link with output voltage reference of 1.5 kV ($D = 0.25, PH = 180^\circ$), 3 kV ($D = 0.5, PH = 90^\circ$ and $PH = 270^\circ$), and 4.5 kV ($D = 0.75, PH = 180^\circ$), are shown respectively, in Fig. 5.16 (a), (b), and (c). The output current reference of $i_L = 25$ A is kept for all three test cases.

The waveforms from top to bottom are phase leg A cell L1/U1 output voltage ($V_{L1A}, V_{U1A}$), cell L2/U2 output voltage ($V_{L2A}, V_{U2A}$), arm and output currents ($i_{UA}, i_{BA},$ and $i_L$), and the output voltage ($V_{out,A}$). As described previously, the operation of the SCC in the dc-dc mode is enabled by different values of the arm currents in one switching period, instead of keeping the same value as in conventional control. All three test results have a good agreement with the theoretical waveform. Regarding the voltage balancing in this case, power-cells are very well balanced with minor differences of less than 50 V, where the worst balancing is seen for
**Figure 5.16:** SCC dc-dc operation mode at \( V_{dc} = 6 \text{kV} \) and \( i_L = 25 \text{ A} \). (a) \( D = 0.25, \ PH = 180^\circ \). (b) \( D = 0.5, \ PH = 90^\circ \) and \( PH = 270^\circ \). (c) \( D = 0.75, \ PH = 180^\circ \).

the \( D = 0.5 \), due to the requirement of phase shift between \( PH = 90^\circ \) and \( PH = 270^\circ \).

**Figure 5.17:** SCC dc-dc operation mode at \( V_{dc} = 12 \text{kV} \) and \( i_L = 24 \text{ A} \) at \( D = 0.5, \ PH = 90^\circ \) and \( PH = 270^\circ \): (a) Waveforms, (b) Power-cell voltages collected through communication network. SCC dc-ac operation mode at \( V_{dc} = 12 \text{kV} \) and \( i_L = 24 \text{ A} \): (c) Waveforms, (d) Power-cell voltages collected through communication network.

Fig. 5.17 (a) shows the results at the 12 kV dc-link voltage with \( V_{out} = 6 \text{kV}(D = 0.5) \) and of \( i_L = 24 \text{ A} \) in order to verify that the converter will work at rated voltage for the 2-cell per arm.
Additionally, voltage balancing of the power-cells, of one of the phase legs, is shown on the graph below, where data is collected through the developed digital sensors which sends the data to the GUI, since the voltages cannot be measured with probes. Regarding the voltage balancing in this case, the power-cells are very well balanced with minor differences of around 200 V, which is superb, considering that each power cell has only 32.5 $\mu$F capacitance.

Regarding the dc-ac operation mode, several 60 Hz line cycle testing results under the 12 kV dc-link with output current reference of $i_L = 24$ A are shown in Fig. 5.17 (c), demonstrating a successful operation. Fig. 5.17 (d) shows voltage balancing results of 300 V difference. As it can be seen, output current is not ideally sinusoidal, containing different harmonics which can be attributed to 1) a very small value of 3 mH of the load inductor, making the system current difficult to control in some cases; 2) difficulty to control currents around zero-crossing in the SCC because of the peak-current mode control and accuracy of the integrated Rogowski coil current sensors.

**Solved Implementation Issues**

Prior to reaching operation at rated voltage in the ICBT, certain issues were observed that can be linked to a communication malfunction. Fig. 5.18 (a) shows an example of the observed phenomenon. Prior to the generated CRC Error indicator on the HB-PEBB U2B, the system was operating successfully at around 3.4 kV operation with 20 A. Suddenly, the converter stopped operating, and it was observable through the GUI that there is a communication fault. At one of the turn-on events of the HB-PEBB L1A, it can be seen that a Cyclic Redundancy Check (CRC) error occurs at the 4th packet, after which, the converter goes into a standard 3 cycle shut-down procedure (cannot be faster due to the nature of the implemented distributed communication approach). The reason for this most likely comes from data corruption during switching instances, due to either high conductive CM currents
caused by very high \( \frac{dv}{dt} \), or high radiated EMI noise caused by high current slew rates, or a combination of both. The implemented solution to bolster the data transmission to the GD is shown in Fig. 5.18 (b). The problem with the data corruption and consequent CRC error reporting is simply resolved by pausing the data transmission and receiving during the switching instances of the cell. After the communication issues were resolved, the system was pushed to higher voltages.

For the SCC, two major issues were cleared at the beginning of testing with the one-cell-per-arm configuration. The first issue is revealed at initial testing in a pulsed configuration without voltage balancing capacitor loops at 700 V, 30 A and considers the GD sensing and driving delay. The results are shown in Fig. 5.19 (a). Since the voltage balancing capacitor loops were not utilized for these pulsing tests, the PCM control boundaries are 0 A and \(-30\) A for the bottom arm. However, Fig. 5.19 (a) shows that those current boundaries are not followed properly, exceeding boundaries for more than 10 A, presenting implementation issues at lower current values and causing increased conduction losses. The reason for this

![Figure 5.18:](image-url) (a) ICBT dc-dc operation at 3.4 kV dc-link having communication malfunction. (b) Implemented solution resolving the communication malfunction by stopping data packet transmission during switching.
is summarized in Fig. 5.19 (b) and due to excessive GD sensing and driving delay compared to low inductance in the arm, thus very high $di/dt$.

The potential solution is presented in Fig. 5.19 (c), where this delay can be easily compensated with altering the current boundary at the known operation voltage and known fixed phase-leg inductance. Originally, the designed total phase-leg-inductance was $L_{\text{arm}} = 16 \mu\text{s}$. This means that operating at 700 V, compensated current should be

$$
\Delta I = V_{\text{dc}} \cdot \frac{t_d}{L_{\text{arm}}} = 700 \cdot \frac{275 \cdot 10^{-9}}{16 \cdot 10^{-6}} = 12 \text{ A}.
$$

More or less, this is reasonable current that can easily be compensated. However, operating voltage is just a fraction of the rated one. On rated voltage, compensated current should be 103 A. That means for the system to successfully operate in PCM mode, the operation current should be higher than 103 A; otherwise, shoot-through events will not happen. For the system designed to operate at max 84 Arms, this is not feasible. This requires that phase-leg inductance (and consequently the PEBB inductor) needs to be increased to slow down...
the di/dt up to values that the GD delays will not matter that much, and can easily make the compensated current in a reasonable range at rated power-cell voltage. The additional inductance required to slow down the di/dt is calculated based on the requirement that the maximum compensated current should be 8 A (10% of maximum load). This implies that inductance needs to be higher than ≥ 206 µH. The designed inductor is \( L_{\text{arm}} = 160 \mu\text{H} \), which gives a total of 320 µH per phase-leg. Therefore, the sensing and propagation delay brings another constraint into the design of minimum SCC arm inductance to ensure an operable PCM.

The second issue could potentially impact the zero voltage switching capability characteristics of the SCC and reduce the efficiency of the converter. In the initial tests, the constant value of dead-time was used, and it was set to be \( T_{\text{dt}} = 900 \text{ ns} \). As can be seen from Fig. 5.20 (a), when the dead-time is longer than the shoot-through time, either upper or lower arm cell voltage output is determined by arm current polarity. This means that the HB-PEBB voltage can actually change, further impacting the desired arm current behavior. This behaviour is shown in Fig. 5.20 (b) when the system is operating at 700 V, 30 A.

---

**Figure 5.20:** (a) Potential issues with elongated dead-time. (b) Experimental verification of impact of improperly designed dead-time.
Intuitively, the problem can be solved with having dynamic dead-time in the system for better controllability and higher efficiency. However, to calculate dead-time values at different current and voltage conditions, one must know the value of output MOSFET capacitance. It is widely known that the parasitic output capacitance $C_{\text{oss}}$ of MOSFETs is nonlinear, exhibiting dependence on the applied drain–source voltage $V_{\text{ds}}$, as shown in Fig. 3.7. To simplify, a linear charge-equivalent capacitance $C_{\text{oss,eq}}$ can be introduced, exhibiting the same amount of stored charge as the nonlinear capacitance at a given drain–source voltage [250]. Based on that, the discharge/charge time of capacitors can be calculated at different current and voltage conditions. Consequently, minimum values of dead-time can dynamically be calculated in the local controller and sent to the GD to implement dead-time between the switches. After solutions for the previous two issues were implemented, the system was pushed to higher voltages.

5.4 Converter Comparisons

Crucial aspects of the two control modes, SCC and ICBT, will be compared to evaluate performance such as the following: voltage balancing in dc-dc and dc-ac conversion, converter efficiency, output converter $dv/dt$, and total harmonic distortion (THD). This will be performed for a 2-cell-per-arm converter.

5.4.1 Voltage Balancing

The two control modes will be compared regarding the voltage balancing efficacy. Prior to the system operation, it is essential that the accuracy of all of the power-cell dc-bus voltage sensors are investigated. It is acceptable if the sensor’s inaccuracies are smaller than ($< 1\%$),
which is relatively easy to obtain, since they mostly consist of the resistor divider, OpAmp, filters, and digital circuitry. All eight power cell voltages are monitored, and Fig. 5.21 (a) and Fig. 5.21 (b) show an example test case where voltage of the power cells is collected from the GUI through the communication network coming from the voltage sensors in the HB-PEBBs. The converter is operating at 12 kV, 10 kHz, 25 A, 60 Hz, in both ICBT and SCC. The ICBT control exhibits superior voltage balancing under the same loading conditions, having only a small fraction of ripple ($\Delta V = 45$ V), as compared to the SCC control where the ripple is $\Delta V = 290$ V.

Figure 5.21: HB-PEBBs voltages collected from the GUI through communication network coming from the voltage sensors at 12 kV, 10 kHz, 25 A, 60 Hz converter operation. (a) ICBT. (b) SCC.

For completeness of the comparison, voltage balancing will be compared at different loading conditions, dc-bus voltage levels, and operation modes. Comparison results for the dc-dc case are shown in Fig. 5.22 while the dc-ac case is shown in Fig. 5.23.

In dc-dc mode, as shown in Fig. 5.22, the voltage imbalances of the ICBT control mode are generally 5 times smaller than the ones in SCC. The maximum voltage imbalance in ICBT is $\Delta V = 45$ V while in SCC is $\Delta V = 230$ V. In ICBT, control voltage imbalances are rising linearly with the current and dc-bus voltage as expected. For SCC, the voltage imbalance only rises with voltage. For the current, it has a worse balancing performance at low and high currents, but for the middle current range, it exhibits better balancing. The
Figure 5.22: Comparison of voltage imbalances in dc-dc operation mode. (a) ICBT. (b) SCC.

Figure 5.23: Comparison of voltage imbalances in dc-ac operation mode. (a) ICBT. (b) SCC.

reason for having worse balancing at lower currents is because at lower arm currents, there is not enough energy to have better balancing, while for high currents, a significant part of time in one switching cycle is consumed by shoot-through states, and that time cannot be compensated by the implemented control. Fig. 5.23 shows the comparison in dc-ac mode, where the voltage imbalances of the ICBT control mode are generally 6 times smaller than the ones in SCC. The maximum voltage imbalance in ICBT is $\Delta V = 45\text{ V}$ while in SCC is $\Delta V = 290\text{ V}$, as shown as shown in Fig. 5.21. The additional increase of voltage imbalance...
in SCC, compared to the dc-dc case, can be attributed to control difficulties around current zero crossing which causes the voltages of the capacitors to fluctuate with fundamental frequency, ultimately meaning that it cannot be completely balanced within one switching cycle. Regardless of that, SCC has substantially better voltage balancing (over six times) than what conventional MMC control would have for the same converter parameters. If one compares ICBT to conventional MMC control, improvement would be over 30 times. In this state, neither control methods can operate at very low loading conditions (≤ 8 A).

5.4.2 Efficiency

As shown in Chapter IV, the HB-PEBB has excellent efficiency at 5 kHz with peak efficiency of $\eta = 99.6\%$, while at 10 kHz, it has peak efficiency of $\eta = 99.3\%$. This implies that the converter itself, will exhibit very high efficiency switching at high frequency, regardless of hard-switching or soft-switching. The efficiency of the converter cell can be estimated as well, since a complete characterization of the HB power cell has been performed (static, dynamic, and thermal), and the operation of the HB-PEBBs within the converter is well defined. However, to fully investigate the performance of the converter, a measurement of efficiency should be performed. Converter efficiency can be assessed with high accuracy with the pumpback method directly, since the power supply only supports the losses of the system and can be directly measured.

The procedure is similar to the one in Chapter IV. Efficiency is again measured for the $D = 0.5$ dc-dc pumpback, at variable dc-bus voltage and for $f_{sw} = 10$ kHz, after thermal steady-state is reached. Fig. 5.24 (a) shows measured efficiency of the phase leg 1 in ICBT and Fig. 5.24 (b) shows measured efficiency of phase leg 1 in SCC.

The maximum efficiency for the ICBT converter happens at 6 kV, 20 A, and it is 99.3\%,
which is very similar to the power-cell efficiency from previous experiments. At 12 kV, the peak efficiency of 99.2% happens at the highest current of 25 A. The ICBT converter delivers, having very high efficiency (even switching at high frequencies), meanwhile preserving the high-density of the converter. The maximum efficiency for the SCC converter happens at 12 kV, 22 A, and it is 98.7%. At highest loading conditions, efficiency of 98.65% is observed. The reason for having lower efficiency in SCC rather than in the ICBT converter is due to the existence of additional arm inductors. Inductors that were used are not suitable for high frequency operation, thus exhibit large losses. However, efficiency is still very high considering the converter’s high-frequency operation. Currently, as observed, ICBT is a more efficient topology in all conditions, able to reach $\eta > 99\%$ at high loading conditions.

### 5.4.3 Output Voltage $dv/dt$

Output voltage $dv/dt$ is one of the crucial parameters describing performance, especially if the converter is to be used for motor control. Output voltage $dv/dt$ can adversely impact the insulation of inverter-driven ac machines and accelerate their degradation. Immense stresses can happen on the insulation system due to fast rising voltage PWM waves applied to the
machine and the resulting over-voltages at the end of a sufficiently long cable. Modern power semiconductor devices implemented in inverters can have $dv/dt$ beyond 10 V/ns, especially for medium voltage devices where it can go beyond 100 V/ns as observed previously. Depending on the cable length, even leads as short as 10 m–20 m can create a motor terminal voltage doubling [251, 252]. These excessive values of voltages, apart from insulation stress, can also create increases in bearing currents, eddy current losses in the core, and skin-effect losses in the winding. Therefore, it is of utmost importance to maintain the $dv/dt$ below some recommended values, depending on the machine and its insulation. To potentially address and solve this problem in the system, several different options can potentially be used, which will be stated later. From previous discussion, it is important that future converter designers be familiar with the nature of output $dv/dt$ for these two control modes.

Fig. 5.25 shows example waveforms of the converter $dv/dt$ in both the ICBT and SCC.

![Waveforms](image)

**Figure 5.25:** Converter output voltage for $D=50\%$ within one switching cycle. (a) ICBT. (b) SCC.

Due to fundamental differences between these converter operation modes, output $dv/dt$ will be significantly different. For ICBT, since it is basically a 2 level converter, the output con-
verter voltage will be roughly the summation of the bottom 2 cell voltage, or approximately twice the cell, as shown in (5.2)

\[ \text{\( V_{\text{out,ICBT}} = V_{L1} + V_{L2} \implies \frac{dV_{\text{out}}}{dt} \approx 2 \cdot \frac{dV_{L1}}{dt} \) or \( \frac{dV_{\text{out}}}{dt} \approx 2 \cdot \frac{dV_{L2}}{dt} \).} \]

(5.2)

From the output voltage perspective, this means that the transitions will be doubled, potentially raising the concern about extremely high \( dV/dt \), given that the power cell already has really fast transitions. However, for the SCC, this is reversed, due to the fundamental multilevel operation and existence of shoot-through states. The output converter voltage can be calculated simply, as shown in 5.3, showing that the output is basically half the HB-PEBB voltage.

\[ V_{\text{out,SCC}} = \frac{V_{dc} - (V_{U1} + V_{U2}) + (V_{L1} + V_{L2})}{2} \implies \frac{dV_{\text{out}}}{dt} \approx \frac{dV_{xy}}{2}. \]

(5.3)

Equation 5.3 is calculated under the assumption that both arm inductors have the same voltage drop, where \( V_{xy} \) is the voltage of any of the HB-PEBB in the phase leg. This ultimately means that the transition speed will be roughly half of the individual power-cell \( dV/dt \).

Fig. 5.26 shows the output converter \( dV/dt \) distribution for ICBT and SCC under different converter dc-bus voltages and its comparison to \( dV/dt \) of the power-cell, under 25 A, in dc/dc conditions, switching under 10 kHz.

The ICBT converter has 4-5 times higher \( dV/dt \) on the output of the converter than what SCC has at the same operating conditions. The maximum \( dV/dt \) in ICBT reaches almost 200 V/ns, while for SCC, that value is below 50 V/ns which is a huge difference. If for ICBT converter high output voltage \( dV/dt \) is potentially detrimental in certain applications, it is of utmost importance to maintain the \( dV/dt \) below recommended values, by heavily mitigating
it. One way to reduce the converter output voltage is by reducing the device \( \frac{dv}{dt} \) through increase of the resistance of the gate loop. However, a higher value of resistance increases switching losses of the semiconductor, thus sacrificing the efficiency [253]. Different passive and active methods of increasing the Miller capacitor value or injecting additional current through it can be used as well [254, 255, 256], however they share a similar problem in reducing the efficiency. Another \( \frac{dv}{dt} \) control method adds RC snubbers in parallel to the switches for both high side and low side [254], with penalty of increased losses in snubber and device. Additionally, controlling the \( \frac{dv}{dt} \) could potentially be solved with using different \( \frac{dv}{dt} \) filtering techniques. Even though filtering techniques do not have an impact on the switching losses on the device, they will introduce additional loss in the filters, increase the cost of the system, and reduce power-density [251, 253].

5.4.4 Total Harmonic Distortion

Total Harmonic Distortion (THD) is one of the most crucial characteristics to quantify the quality of the delivered power to the load, and it should be kept as low as possible. Lower THD is in a direct relationship with lower peak currents, higher power factor, and
higher efficiency. Firstly, the two control modes will be compared regarding the THD of the converter output current.

Fig. 5.27 shows the behavior of the output current THD in 2 control modes. For completeness of the comparison, they are compared through different loading conditions and different dc-bus voltages.

ICBT generally has lower output current THD owing to much easier control of the current around the zero crossing. Subsequently, it impacts the capacitor voltage ripples adversely, which does not reflect back on the output current shape. This is confirmed with Fig. 5.15. Maximum values of THD for ICBT is 11.9% for lower voltage cases while at rated voltage does not surpass 10%. Comparing the SCC to those values, maximum THD is 22%, more than double at the rated voltage. This means that from a current perspective, SCC would need stronger filters compared to ICBT, which implies higher volume and increased cost.

Secondly, the two control modes will be compared regarding the converter output voltage THD.

Fig. 5.28 shows the behavior of the output phase leg voltage THD in 2 control modes. The
comparison is shown for the 60 Hz, 12 kV dc-bus, 28 A, switching at 10 kHz, with the same modulation index.

Due to a 2-level fundamental operation, it is expected that at the same conditions, the ICBT converter has larger output voltage THD than the multilevel voltage output of SCC. This can be confirmed from Fig. 5.28. The output voltage THD value for ICBT is 215 % with the peak harmonic on the switching frequency while for SCC is 126 % with the peak harmonic on double the switching frequency. For n cells, it will be on \( n \cdot f_{sw} \), if we exclude the dc harmonic content which in polyphase systems on the load side does not exist ideally. This means that from a voltage perspective, ICBT would need stronger filters compared to SCC, which implies higher volume and increased cost. With more cells per arm, this effect is amplified since the SCC harmonics move to higher frequencies which are then able to be filtered with even smaller passives.

Fig. 5.29 summarizes the crucial converter parameters comparison. The ICBT control has superior voltage balancing due to control simplicity, higher efficiency at full load for 0.55 %
(it has lower losses for 1.7 times at same conditions), meanwhile having comparable low load efficiency. Furthermore, ICBT exhibits lower output current THD for 2.2 times. It lacks in performance compared to SCC in output converter slew rates \( \frac{dv}{dt} \) - extremely high \( \frac{dv}{dt} \) over 4 times of the one observed in SCC, and output voltage THD, since in ICBT, the output voltage is 2 level.

**Figure 5.29:** Summary of crucial converter parameters and their comparison between ICBT and SCC.

### 5.5 Summary

Medium-voltage (MV) applications such as grid-tied inverters, dc-dc converters for MVDC microgrids, and motor drives would immensely benefit from high-efficiency, high-density, and high-frequency converters. At the core of the proposed approach and innovation are the following: 1) high-voltage printed circuit board (PCB) planar dc-bus with minimized loop inductances and weight, 2) switching-cycle control (SCC), 3) integrated capacitor-blocked transistor (ICBT) converter control, 4) and a required high-performance/high-bandwidth communication network with synchronization accuracy of \(< 1 \text{ ns}\), enabling the proposed controls. Prior to the converter build, detailed power-cell assembly and qualification proce-
dures are developed. Sixteen power-cells are constructed and qualified, out of which eight were used to construct a two-cell per arm prototype. The converter operates successfully in both SCC and ICBT in dc-dc and dc-ac mode without the necessity for outside passives, having switching speeds (up to 100 V/ns per power-cell) and high-switching frequency (10 kHz), meanwhile exhibiting high common-mode transient immunity and high-efficiency ($\eta_{\text{ICBT}} = 99.2\%$ and $\eta_{\text{SCC}} = 98.65\%$). The converter designed in this way successfully overcomes the challenges of high-voltage insulation, high $dv/dt$ and electromagnetic interference (EMI), and high-switching frequency, providing the system with benefits of high power density, high-efficiency, fast dynamic response, unrestricted line frequency operation, and improved power quality. Comparing the two, ICBT control has superior voltage balancing due to control simplicity, higher efficiency at full load for 0.55\% (it has lower losses for 1.7 times at same conditions), meanwhile having comparable low load efficiency. Furthermore, ICBT exhibits lower output current THD for 2.2 times. It lacks in performance compared to SCC in output converter slew rates $dv/dt$ - extremely high $dv/dt$ over 4 times of the one observed in SCC, and output voltage THD, since in ICBT, the output voltage is 2 level.
Chapter 6

Summary and Future Work

6.1 Summary

This dissertation encompasses the work performed to enable the utilization of an SiC MOSFET device in medium-voltage (MV) applications with the aim of achieving next-generation, high-density, high-efficiency, highly reliable power electronics converters. First, real-time (online) measurement of the junction temperature is developed which helps improve long-term reliability by enabling active thermal control, monitoring, and prognostics. It is accomplished by generating integrated intelligence on the gate-driver (GD) level with a maximum error of less than 5 °C, having excellent repeatability of ±1.2 °C. Additionally, a degradation monitoring and aging compensation scheme are explored. Second, for the MV SiC MOSFET device, a high-performance gate-driver overcomes the challenges of electro-magnetic interference (EMI) concerning common-mode (CM) currents and cross-talk, low driving loop inductance required for fast switching, and device short-circuit (SC) protection. The developed GD (for 10 kV devices) is able to sustain \( \frac{dv}{dt} \) higher than 100 V/ns, less than 5 nH gate loop inductance, and SC protection - turning off the device within 1.5 \( \mu \)s. In addition, a comprehensive device characterization is performed in order to better understand the device behavior for the MV applications. Third, to ensure a successful operation of the power-cell incorporating the 10 kV SiC MOSFET, a systematic design and assessment methodology is explored. Challenges are addressed, including high-voltage insulation, high \( \frac{dv}{dt} \) and EMI, component and system protections, as well as thermal management. The
developed power-cell achieved a high-power density of 11.9 kW/l, with measured peak efficiency of $\eta = 99.3\% @ 10$ kHz. It successfully operated at $V_{dc} = 6$ kV, $I = 84$ A, $f_{sw} \geq 5$ kHz, $T_j \leq 150$ °C and had high switching speeds over 100 V/ns. Lastly, to showcase the high-power density and high-efficiency on the MV converter level, challenges of high-voltage insulation, high-bandwidth control, EMI, and thermal management were solved. To explore the aforementioned benefits, a modular, scalable, 2-cell per arm, prototype MV converter based on the developed power-cell is constructed. The converter successfully operated at $V_{dc} = 12$ kV, $I = 28$ A, $f_{sw} = 10$ kHz, with high switching speeds, exhibiting high transient immunity in both switching-cycle control and integrated capacitor-blocked transistor configuration, in both dc-dc and dc-ac mode.

### 6.2 Future Work

As many of the technologies in this dissertation were proposed and used for the first time, more work can be done in order to better understand their behavior and to investigate new aspects.

Regarding the enhanced gate-drivers, future research topics can include:

1. Generalization of the proposed junction temperature monitoring scheme in order to avoid calibration of every device prior to operation.
2. Investigation of the feasibility of proposed degradation monitoring and aging compensation scheme.
3. Rogowski coil integration in the power-modules or the PCB planar busbar.
4. Gate-driver sensing and propagation delays minimization in order to reduce the required inductances in switching-cycle control.
Regarding the 6 kV power-cell and medium-voltage converter, future research topics can include:

1. Power-cell and converter conductive and radiated electromagnetic interference (EMI) studies.

2. 0 V enclosure power-cell insulation and thermal studies.

3. Full SCC and ICBT converter (with output filters) design and optimization for target applications.

4. Further exploration of scalability of the approach from control and high-voltage aspects.
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