High Performance RF Circuit Design: High Temperature, Ultra-Low Phase Noise, and Low Complexity

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ABSTRACT

Advanced achievements in the area of RF circuit design led to a significant increase in availability of wireless communications in everyday life. However, the rapid growth in utilizing the RF equipment has brought several challenges in different aspects of RF circuit design. This has been motivating researchers to introduce solution to cope with these challenges and further improve the performance of the RF circuits. In this dissertation, we focus on the improvements in three aspects of the circuit design. High temperature and temperature compensated transmitter design, ultra-low phase noise signal generators, and compact and low complexity polar transmitter design.

Increase in the ambient temperature can impact the performance of the entire communication system. However, the RF hardware is main part of the system that is under the impact of the temperature variations in which it can change the characteristics of the individual building blocks of the RF chain. Moreover, transistors are the main elements in the circuit whose performance variation must be consider when the design target is compensating the temperature effects. The influence of the temperature variation is studied on the transistors and the building blocks in order to find the most effective approaches to compensate these variations and stabilize the performance of the RF chain at temperatures up to 220 $^{\circ}C$. A temperature sensor is designed to sense these variations and adjust the characteristics of the circuit components (e.g. bias voltages), accordingly. Further, a new variable gain phase shifter (VGPS) architecture is introduced toward minimizing the temperature impact on its performance in a phased-array transmitter architecture. Finally, a power amplifier as

the last stage in a transmitter chain is designed and the variation in its performance with temperature is compensated through the VGPS stage. The transmitter is prototyped to evaluate its performance in practice.

Another contribution of this dissertation is to introduce a novel voltage-controlled oscillator (VCO) structure to reduce the phase noise level below state-of-the-art. The noise to phase noise mechanism in the introduced doubly tuned oscillator is studied using linear time-variant (LTV) theory to identify the dominant noise sources and either eliminate or suppress these noise sources by introducing effective mechanism such as impedance scaling. The designed VCO is fabricated and measurement results are carried out that justified the accuracy of the analyses and effectiveness of the introduced design approach.

Lastly, we introduce a compact and simple polar transmitter architecture. This type of transmitters was firstly proposed to overcome the serious shortcomings in the IQ transmitters, such as IQ imbalance and carrier leakage. However, there is still several challenges in their design. We introduce a transmitter architecture that operates based on charge to phase translation mechanism in the oscillator. This leads to significantly reduction in the design complexity, die area, and power dissipation. Further, it eliminates a number of serious issues in the design such as sampling rate of the DACs. comprehensive post-layout simulations were also performed to evaluate its performance.

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General Audience Abstract

To keep up with the ever-growing demand for exchanging information through a radio frequency (RF) wireless network, the specification of the communication hardware (i.e. transmitter and receiver) must be improved as the bottleneck of the system. This has been motivating engineers to introduce new and efficient approaches toward this goal. In this dissertation however, we study three aspects of the circuit design. First, variation in the ambient temperature can significantly degrade the performance of the communication system. Therefore, we study these variations on the performance of the transmitter at high temperature (i.e. above 200 $^{\circ}C$). Then, the temperature compensation approaches are introduced to minimize the impact of the temperature changes. The effectiveness of the introduced techniques are validated through measurements of the prototyped transmitter. Second, signal generators (i.e. oscillators) are the inseparable blocks of the transmitters. Phase noise is one of the most important specifications of the oscillators that can directly be translated to the quality and data rate of the communication. A new oscillator structure targeting ultra-low phase noise is introduced in the second part of this dissertation. The designed oscillator is fabricated and measured to evaluate its performance. Finally, a new polar transmitter architecture for low power applications is introduced. The transmitter offers design simplicity and compact size compared to other polar transmitter architectures while high performance.

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The completion of this dissertation would not have been possible without support of my family. I thank my beloved parents and brothers for their uncoditional love , care, and sacrifice that they dedicated to me in my life.

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Chapter 1

Introduction

1.1 Motivation

The overwhelming statistics show the demand for mobile communications equipment and services has been growing rapidly in the last three decades. The increase in the density of the users has brought new challenges toward achieving advancements in this field that has been a motivation for the engineers to introduce solutions to address these design challenges. Numerous number of works have been introduced in this regard, however, this dissertation focuses on three improvement aspects in RF hardware design (i.e. RF transmitters); temperature impacts and its compensation methods in transmitter design, RF frequency generators (i.e. oscillator) and polar transmitter design.

1.1.1 High Temperature RFIC Design

Operating temperature in high temperature applications such as oil and gas well logging, military, geothermal energy exploitation and space exploration can exceed 200 °C [6]. This

necessitates the need for high temperature electronics that can reliably operate at those temperatures with adequate lifetime. The circuits on silicon do not meet the requirements at temperatures above 200 °C or higher due to temperature runaway. The failure rate of silicon-based circuits doubles for every 10 °C increase in the temperature above 200 °C [6]. On the other hand, gallium nitride (GaN) on silicon carbide (SiC) transistors can operate reliably at temperatures up to 450 °C, thanks to their larger energy band gap compare to silicon devices [7]. Phased array transceivers are widely used in a vast number of telecommunication applications due to their capabilities for achieving high speed communication and fast beam steering [8]. The advantages of the phased arrays can be utilized for high temperature applications. However, to date, all the proposed high temperature circuits and systems published in the open literature are designed for traditional RF frontends (i.e. single transceivers). An important consideration arises when a phased array operates at mm-wave and the power efficiency of the power amplifiers drop drastically. Hence, more power must be dissipated to provide sufficient radiated power that further heats the circuit. Therefore, temperature compensation approaches that can reliably minimize the impact of the temperature on the specifications of individual components and hence, the overall system, becomes necessary. We propose a phased-array transmitter architecture including efficient temperature compensation circuitry that adaptively adjust the characteristics of the active devices and suppress the performance variation with temperature. The compensation techniques offer a reasonable compromise between power dissipation, size, design complexity and performance.

1.1.2 Ultra-low phase noise voltage-controlled oscillator (VCO)

Signal generators are inseparable blocks in RF transceiver architectures that their performance impact the overall functionality of the communication system. Figure 1.1 shows the architecture of a phased-array transceiver. Local (LO) signal generator is responsible for

providing the mixer for up/down converting the baseband (BB)/RF signal. Typically, the LO signal generator is composed of a VCO along with a phase-locked loop (PLL) to stabilize the generated frequency. Phase noise is one of the most important specifications of the LO signal that has a direct impact the performance of the transceiver, affecting bit error rate (BER) and hence, data rate. Although the PLL can suppress phase noise of the LO signal at close-in frequency region, the VCO block still dominates the phase noise level at far-out frequencies and becomes the bottleneck of the phase noise performance. Therefore, lowering the phase noise of the VCO is a necessity for achieving low BER with high data rate.

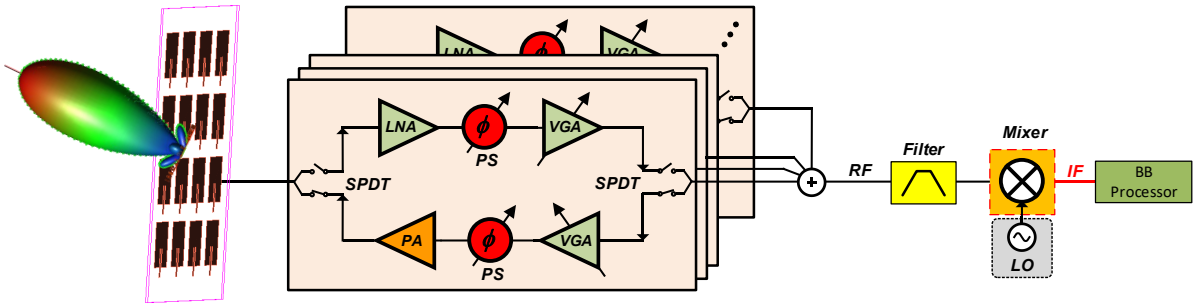


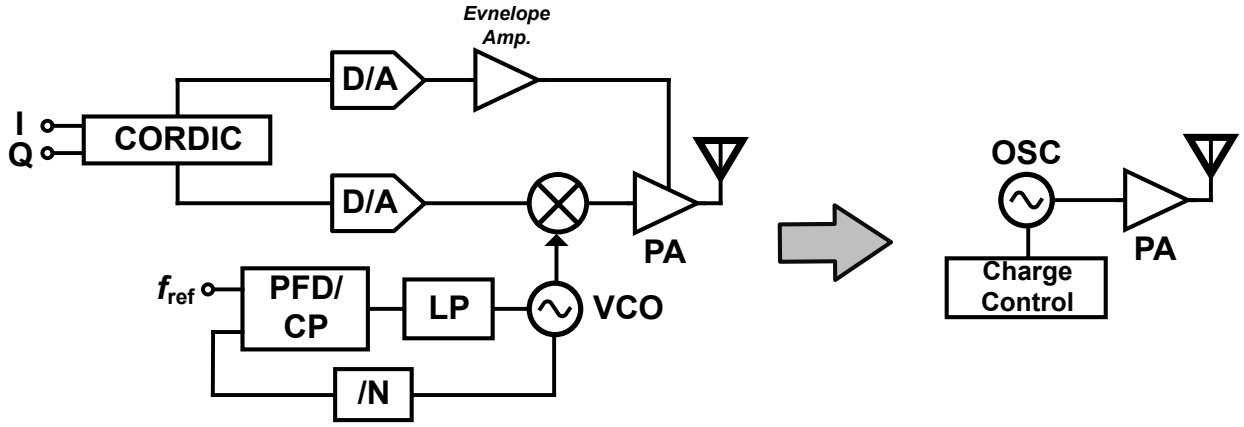
Figure 1.1. Typical architecture of a phased-array time division duplex (TDD) transceiver.

Several works have been recently introduced to push the phase noise level toward its minimum thermodynamic limit. However, they achieved low phase noise level at the cost of larger die area, higher power dissipation and added design complexity. This is a motivation to propose a new oscillator structure that offers an ultra-low phase noise without sacrificing other important specifications of the oscillator.

1.1.3 Polar Transmitter Design

Integration of the radio-frequency identification (RFID) and internet of things (IoT) transceivers in general, is a necessity toward minimizing the cost of the mass production of the products for these applications [9]. The scaling down advantage of CMOS technology process makes it

a suitable candidate for integration of such circuits. However, a fully integrated transceiver includes high power blocks such as power amplifier (PA). Further, most of the IoT tags use amplitude modulated signals to transfer data and communicate with adjacent nodes and gadgets. This indicates that PA block as the last stage in the transmitters with high output power has to provide a highly linear performance. However, a high linear characteristic for the PA can be achieved at the cost of operating at sub-optimum region of power efficiency. Therefore, researchers introduced several approaches to improve the power efficiency while preserving high linearity. Among the introduced approaches, polar transmitter architecture has been proven to be an efficient solution to address the aforementioned issue. Figure 1.2 (a) shows the block diagram of a typical polar transmitter [10]. The PLL including a VCO is responsible of shift change in the output signal of the PA while the envelope amplifier adjusts the amplitude of the output signal by changing the supply voltage of the PA. On the other hand, Figure 1.2 (b) shows the block diagram of the proposed polar transmitter composed of an oscillator and a buffer (PA). Compared to the conventional polar transmitter, the proposed one offers compact size, lower power dissipation and significantly lower design complexity.



(a) (b)

Figure 1.2. (a) block diagram of a typical polar transmitter, and (b) proposed architecture.

1.2 Contribution and Dissertation Structure

1.2.1 Chapter2

In chapter 2 of this dissertation, the necessary preliminaries related to the scopes of this research are reviewed. The typical phased-array transmitter architecture is discussed and its specifications are represented. The potential impact of the temperature on the critical characteristics of individual building blocks and the overall transmitter chain is also reviewed. Different aspects of available process technologies are compared to find a suitable candidate for high temperature RF circuit design. Gallium nitride (GaN) on silicon carbide (SiC) high electron mobility transistors (HEMTs) as the main component of the transmitter building blocks and their characteristics are investigated.

1.2.2 Chapter 3

In order to gain more insight into the design procedure of the high temperature building blocks of the phased-array transmitter, design steps of a variable gain phase shifter and class-AB and -F[1] PAs are described. Moreover, the impact of the temperature on the characteristics on the active and passive devices, and hence the individual building blocks, is investigated. The introduced structures of the building blocks are then modified and their performance is optimized to be used in a high temperature phased-array transmitter architecture. Design expressions are derived for the transmitter blocks and simulation results are introduced. The measurement results of the prototyped transmitter are shown and discussed in this chapter. Furthermore, the reliability of the system is also investigated for estimating the reliable life-time of the transmitter.

1.2.3 Chapter 4

In this chapter, the design challenges of the ultra-low phase noise oscillators and related previously published works are reviewed. A new doubly-tuned oscillator structure is proposed and design expression are derived. Phase noise performance of the oscillator is studied using closed-form expressions at far-out offset frequencies while the impact of the circuit components on phase noise is studied in detail. The fabricated circuit is measured to evaluate its phase noise performance and power efficiency.

1.2.4 Chapter 5

A polar transmitter with a new operation mechanism is introduced in this chapter. First, the charge to phase translation mechanism as the foundation of the proposed polar transmitter is introduced. The concept of the variable phase oscillator is elaborated and its detailed design is introduced. A digitally controlled charge unit is design to adjust the phase shift of the oscillator and its logic is explained. A buffer stage is also designed and completed transmitter is laid out in CMOS process technology to consider the effect of the parasitics of the circuit components on its performance. The simulation results are carried out to evaluate the performance of the transmitter including data rate and corresponding error vector magnitude (EVM).

Chapter 2

Preliminaries

In this chapter, we review the preliminaries related to the technical aspects of this dissertation. First, we review the phase array architecture and its building blocks. Next, the fundamentals of high temperature circuit design are discussed, followed by the VCO classes and phase noise theory.

2.1 Phased-Array Transceiver

The unique advantages of phased array transceivers makes them attractive for many applications. Unlike the traditional mechanically beam forming mechanism, phased arrays electronically change the beam angle that significantly speed up the beam forming process. Broadcasting, Radar, Space probe communication, Weather research usage, RFID and mobile communication are examples of phased array applications. Figure 2.7 shows several popular architecture of phased array transceivers.

2.1.1 Phased Array Architectures

Figure 2.7 (a) shows the *digital beamforming* architecture. It consists of multiple identical RF chains. The BB amplitude and phase signals are weighted and fed into the RF chains in which each individual antenna produces a specific beam pattern. Therefore, added beams can produce different beam patterns. This architecture offers excellent flexibility in shaping the antenna array beam. However, it requires high number of RF chains that results in high power consumption.

On the other hand, *analog beamforming* technique is represented in Figure 2.7 (b). It is composed of a single RF chain while the analog beamformer includes phase shifters and attenuators. The processed BB signal is up/down converted and amplified by passing through the RF chain. Then, the analog beamformer adjusts the phase and amplitude of the signal and finally delivers the modified signals to the antenna array. Therefore, it can provide a single beam pattern at a time while digital beam forming is able to create multiple beams. Moreover, the analog beamforming is more power efficient compared to digital one, since it has only one RF chain. It should be noted that using active phase shifters and variable gain amplifiers (VGA) instead of attenuator can increase the power consumption of the transceiver.

Third category of the phased array trasceivers are *hybrid*. This type of transceivers take advantage of the benefits of both aforementioned architectures by combining digital and analog beam forming techniques to reduce the design complexity and improve power efficiency. Figure 2.7 (c) and (d) shows two different types of hybrid transceivers. The difference is the connectivity of the analog beamformers. In partially connected architecture, the beamformer is connected to a subset of phase shifters while in fully connected architecture the beamformers are connected to all of the phase shifters. Compared to partially connected transceiver, fully connected transceiver provides higher gain at the cost of higher design complexity and

power dissipation.

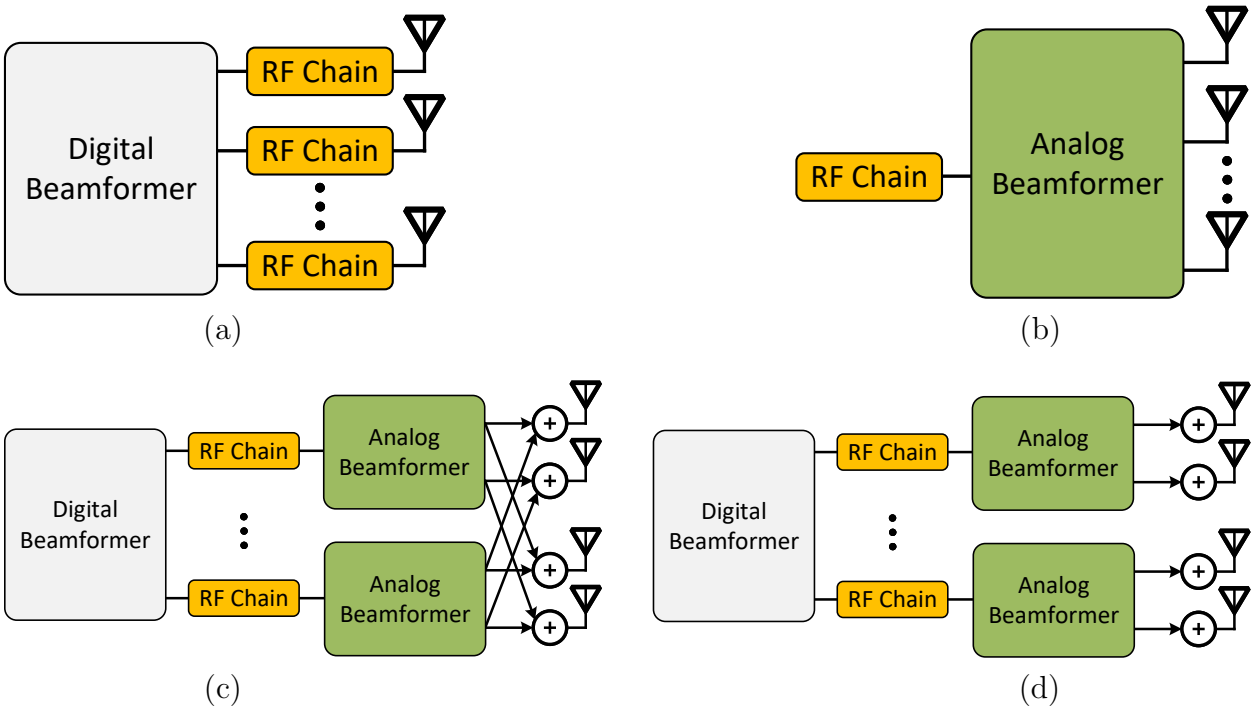


Figure 2.1. (a) block diagram of a typical polar transmitter, and (b) proposed architecture [1].

2.1.2 Transmitter Architectures

The main task of an transmitter frontend is performing modulation, upconverting the BB signals, adjusting the gain and phase shift of the RF signal and finally amplifying and delivering it to the antenna. Depending on the design needs and system requirement, several transmitter architectures have been proposed. Direct conversion (zero IF) and heterodyne are two popular transmitter architectures [11]. Figure 2.2 (a) shows the conventional direct conversion transmitter. In-phase (I) and quadrature (Q) BB signals are multiplied by the quadrature LO signals to be up-converted. Two quadrature paths are combined as a single RF stream. Depending on the application and the phased array architecture, the phase shifter (PS) and VGA blocks can be eliminated or relocated in the chain. The phase shifter block add a relative phase shift in a passive or active manner. The VGA block then adjust

its gain an delivers the RF signal to the PA. Further. the PA block provide a sufficient gain level to the signal. Lastly, the duplexer block switch between receiver and transmitter chains. Although this architecture offers a compact size and clean output spectrum (i.e. only desired frequency content), it has several drawbacks.

Firstly, any mismatch between BB I and Q signals can cause an error in amplitude and phase of the up-converted signal and hence, its EVM. Second, the dc offset at the BB port of the up-conversion mixers create unmodulated carriers at their outputs. This results in a shift in the signal constellation. Third, since the transmitted (TX) signal carries high power, the linearity of individual building blocks become important. Therefore, design of the building blocks with high linearity is necessary, as it will be discussed in more details later in this chapter. Another critical issue in direct conversion architecture is oscillator pulling. Since the PA is generating a very high power signal, it can leak through the substrate and couples to the local oscillator. This is an important issue since the transmitter output contains a frequency spectrum around the LO frequency that increases the chance of pulling.

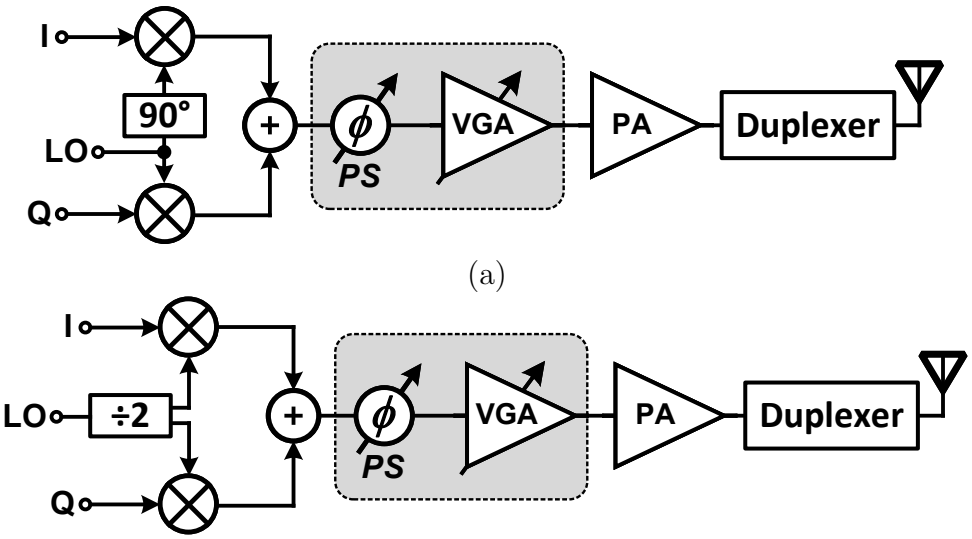


Figure 2.2. (a) block diagram of traditional direct conversion transmitter, and (b) its modern version.

In order to minimize the pulling effect, the transmitter architecture in Figure 2.2 (b) can

be adopted. As it can be seen in the figure, the main local oscillator generates a frequency to times higher than the carrier frequency and then is divided by two to be used for up-conversion. This has two benefits; reducing pulling effect and providing quadrature LO signals by the divider. This architecture is not able to completely eliminate the pulling effect since PA produces higher order harmonics (e.g. second order harmonic) due to its limited linearity. However, the amount of power at higher order harmonics are sufficiently lower than its power at fundamental harmonics. Moreover, the pulling effect can be further suppressed using layout techniques.

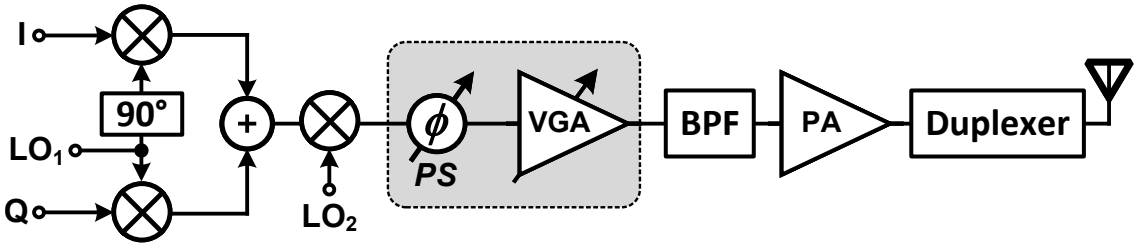


Figure 2.3. Block diagram of heterodyne transmitter.

Another approach to cope the pulling effect is two step up-conversion. Figure 2.3 shows the alternative transmitter architecture called *heterodyne transmitter*. The BB signals are up-converted to an intermediate frequency (IF) and in second step to RF. Although this architecture eliminates the pulling effect, it has another series issue. The second mixer (RF mixer) produces and additional sidebands around LO_2. This *image* spectrum needs to be removed from the RF signal before transmitting it. Therefore an auxiliary image reject filter or advanced mixer topology is required for this purpose. Compared to direct conversion transmitter, heterodyne architecture consumes higher power while has more design complexity.

2.2 Transmitter Building blocks

2.2.1 Phase Shifter

Phase shifters are responsible of making a permanent phase shift in its input signal. Passive and active are two main categories of electrical phase shifters. Although both phase shifter structures provide phase shift, active circuits provides additional gain with compact size compared to passive phase shifters. Figure 2.4 (a) shows one of the most common phase shifter structures. It is composed of a series of weighted all pass networks (APNs). The bypass path shorts input and output of the phase shifting element, while the second path including all pass filer applies a relative phase shift to the input signal. N number of weighted series of the phase shifting elements can provide 2^N discrete phase shift states. This structure offers high linearity, low noise figure, reasonable accuracy and ultra-low power due to the leakage current. However, it requires a large die area since it includes atleast N number of inductors. Figure 2.4 (a) shows an alternative compact passive phase shifter. It is composed of a single APN where the fixed capacitors are replaced with variable capacitance capacitors (varactors). This enables the phase shifter to continuously change the phase of the input signal. Adopting varactors in its structure can reduce the linearity of the phase shifter and increase the distortion in the output signal due to non-linear characteristic of the varactors. Moreover, using transistor based varactors adds to the effective output noise.

Two common structures of active phase shifters are shown in Figure 2.5. The active APN phase shifter [Figure 2.5 (a)] creates the characteristic of a APN by combining signals of two paths. This structure is able to provide continuous phase shift by adopting a tunable all pass filter, similar to Figure 2.4 (b). Further, both buffer and adder blocks can amplify the signal and provide gain in the transmitter chain. Compared to the passive structures, active phase shifters offer voltage gain and compact size, at the cost of high noise and power

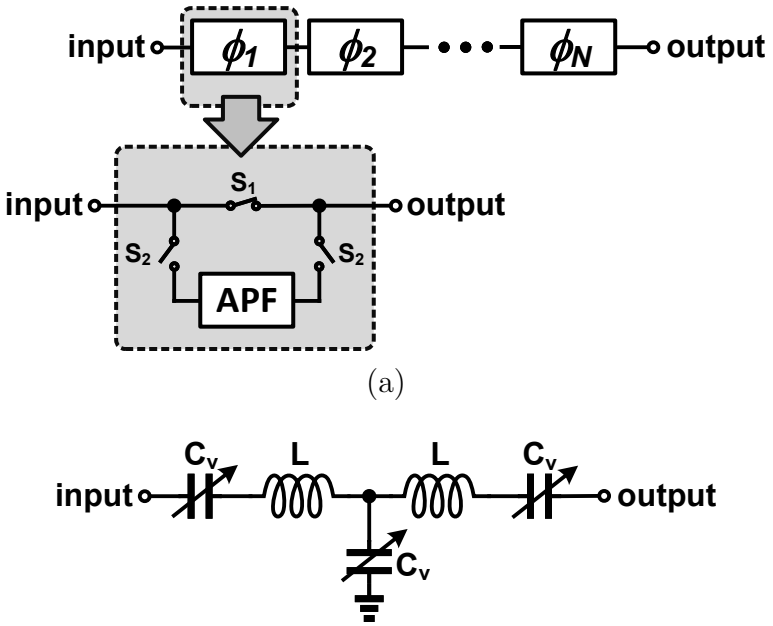
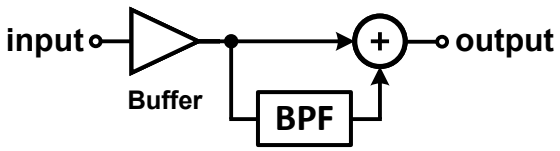


Figure 2.4. Simplified schematic of passive (a) all pass network, and (b) varactor based tunable phase shifters.

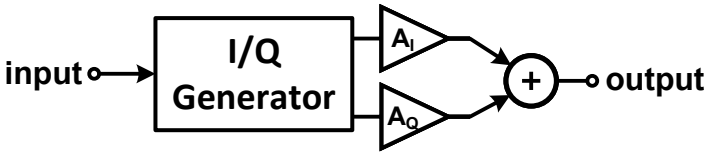
dissipation and less linearity. Figure 2.5 (b) shows another active phase shifter structure known as *phase interpolation* phase shifter. The IQ generator splits the input signal into to in-phse and quadrature outputs. Two variable gain amplifiers then fed the quadrature outputs to an adder block with different weights. The applied phase shift is depending on the gain of the amplifier (i.e. A_I and A_Q). Although this structure provides an excellent accuracy, it is highly sensitive to the mismatch between I and Q paths. Furthermore, its design complexity is considerably higher than the APN active structure.

2.2.2 Variable Gain Amplifier

Most of the VGA circuits introduced in the literature can be categorize under current controlled and current steering [12,13]. The basic operation mechanism of the current controlled VGA is demonstrated in Figure 2.6 (a). Transistor (M_2) controls the dc current flowing into the gain transistor (M_1) and hence, control its transconductance (g_m). The gain of this



(a)



(b)

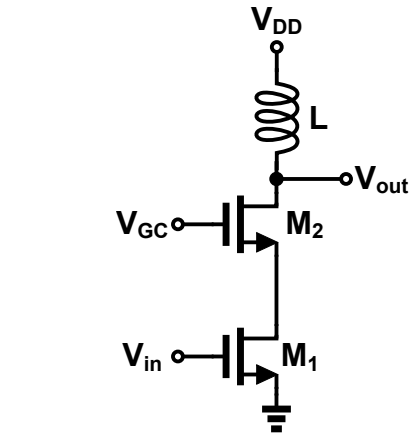
Figure 2.5. Simplified schematic of active (a) all pass network, and (b) phase interpolation phase shifters.

structure can be discretely or continuously controlled through gain control voltage (V_{CG}). The major drawback of this structure is variation in the output matching with gain. This becomes critical when the output impedance must match to the input of the next stage. The output impedance of the current steering structure on the other hand [Figure 2.6 (b)], is less sensitive to the gain variations. However this is achieved at the cost of higher design complexity.

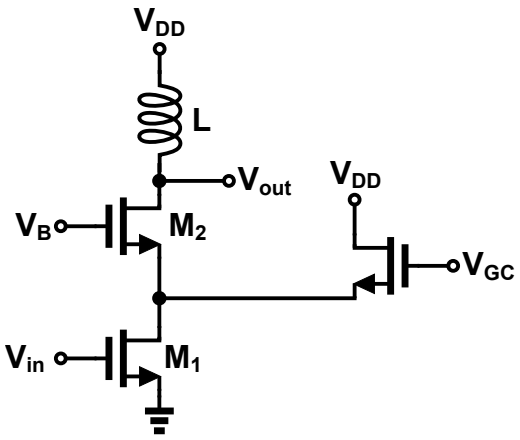
2.2.3 Power Amplifier

PA is one of the most important blocks in the transmitter chain whose specifications can significantly effect the overall performance of the communication system. Linearity and power efficiency are two main specifications of the PAs. Numerous works have been introduce with different designs toward improving these specifications. However, two popular PA classes, that are exploited to the design of the high temperature transmitter in Chapter 3, will be reviewed in this chapter.

Figure 2.7 (a) shows the schematic of the class-A, -B, -AB, and -C PAs. Input and output matching networks (IMN, OMN) are designed to match the input and output of the PA to the source and load impedances, respectively. Furthermore, source and load pull is required



(a)

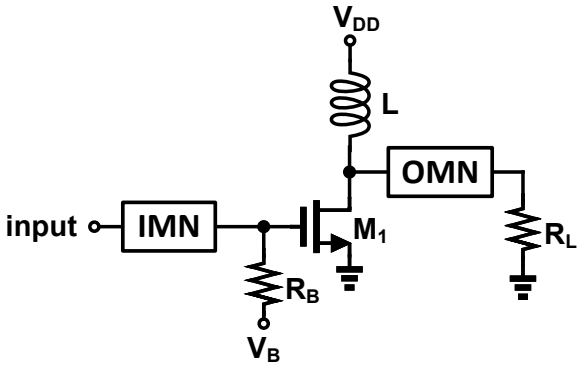


(b)

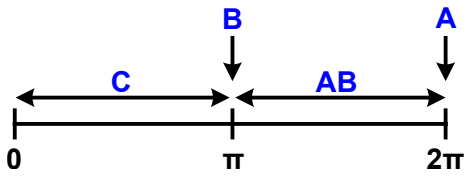
Figure 2.6. Simplified schematic of (a) current controlled, and (b) current steering VGAs.

to find the optimum impedance at the source and load sides. Different operation classes can be obtained by adjusting the bias voltage (V_B) and hence, conduction angle of the transistor. As it is shown in Figure 2.7 (b), class-A PA conducts the signal over the entire signal period while class-B only conducts over half a cycle. Therefore class-B offers a better power efficiency since the current and voltage waveforms have smaller overlap compared to class-A. In order to increase the power efficiency of class-AB, the conduction angle can be further decreased to conduct in a smaller portion of a cycle at the cost of lower output power. Figure 2.7 (c) demonstrates the trade off between power efficiency and linearity of the PA classes. As it can be ssen in the figure, moving from class-A to class-C, power efficiency increases at the cost of lower output power while linearity decreases. In conclusion, class-AB provides a sufficient linearity for most of the communication standards while high output power and moderate power efficiency.

Unlike the previously mentioned PA classes that the transistor behaves as a transconductance amplifier, in inverse class-F PA structure the transistor behaves as a switch (similar to class-E PA). However, its output is tune in the sense it provides non-overlap current and voltage waveform. This indicates that ideally, the power efficiency can reach 100% while the output power is higher than class-C PA (similar to class-D PA). Figure 2.8 shows the simplified schematic of inverse class-F PA. The output port of the transistor (i.e. Drain) is terminated to an optimum impedance of Z_1 while open and short at even and odd harmonics, respectively. Inverse class-F power amplifier provides an exceptional power efficiency with high output power and moderate linearity compared to class-AB.



(a)



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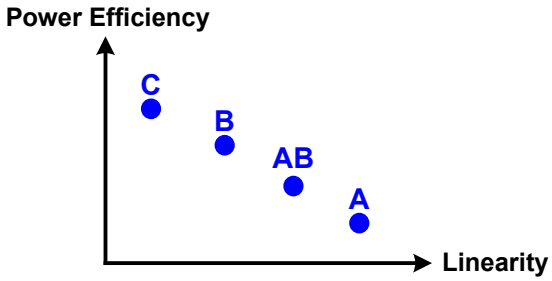


(c)

Figure 2.7. (a) Simplified schematic of class-A, -B, -AB, and -C PAs, (b) their corresponding conduction angle, and (c) linearity versus power efficiency trade off.

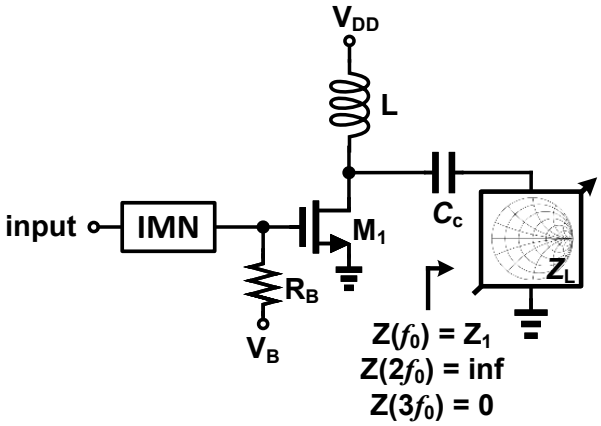


Figure 2.8. Simplified schematic of inverse class-F PA.

2.3 High Temperature Process Technology

Variation in the ambient temperature has a significant impact on the performance of the circuit. Therefore, the temperature effect must be considered when the target application includes operating at high temperature. The most important consideration is choosing a proper process technology that can reliably operate at high temperature while satisfy other system requirements such as operating frequency, power consumption, linearity and output power. Several technologies are available with capability of integration.

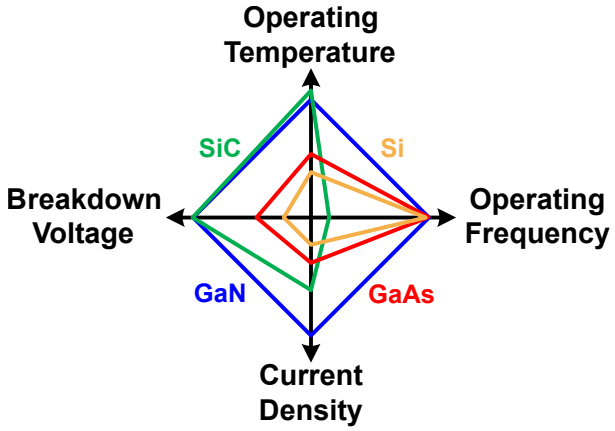


Figure 2.9. Comparison of process technologies [2].

Figure 2.9 compares important characteristics of different process technologies toward designing RF transmitter. Since the target operating temperature can exceed 200 °C, both gallium nitride (GaN) and silicon carbide (SiC) may be suitable candidates. However, GaN technology offers high operating frequency due to small parasitics of the transistors and higher current density owes to high electron density in the 2-dimensional electron gas (2DEG) layer of the GaN structure, as it is shown in Figure 2.10. These advantages makes GaN technology suitable for RF and high power circuit design for high temperature applications.

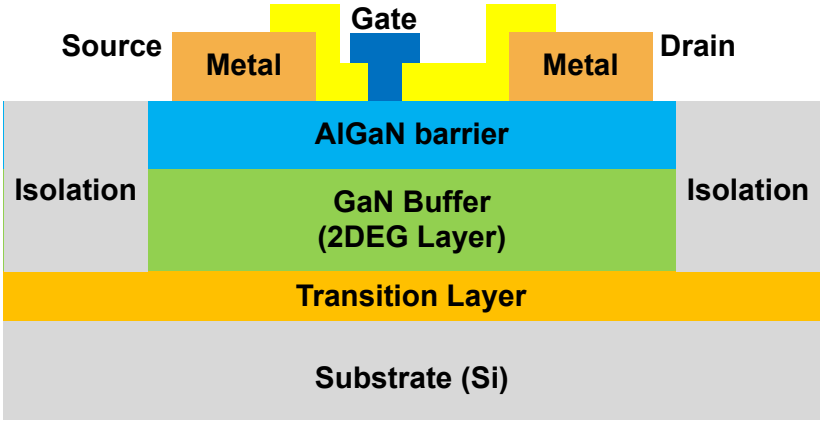


Figure 2.10. GaN Substrate cross section.

2.4 Voltage-Controlled Oscillators

In this section, we review the most practical VCO architectures and their operation mechanism. Then, the linear time variant (LTV) phase noise theory is briefly discussed that will be used in Chapter 4 for analysing the phase noise performance of the proposed oscillator.

2.4.1 Oscillator Structures

Oscillator is one of the main building blocks of the RF transceivers. It is responsible of generating a local frequency for up/down converting the BB/RF signals. In order to minimize the frequency drift of the oscillators, a PLL will be adopted to stabilize its output frequency. Figure 2.11 represents the concept of an electrical oscillator. The following criteria, known as *Barkhausen criteria* must be met that makes the loop unstable and enables it to start oscillation [14].

$$|A \cdot H| = 1 \tag{2.1a}$$

$$\angle A \cdot H = 180^\circ \tag{2.1b}$$

Figure 2.11 shows the schematic of ring oscillator which one of the basic oscillator structures that operates based on Barkhausen criteria. It is composed of odd number of inverters. The oscillation loop must provide sufficient loop gain and phase to meet the criteria in (2.1). The oscillation frequency can be controlled by adjusting the gain of individual inverters through their dc current. This structure is suitable for low power applications since its power dissipation can be as low as a couple of μ-Watts. However, due to high amount of produced jitter by the inverters and lack of a filtering mechanism, its phase noise is not satisfying for low phase noise applications.

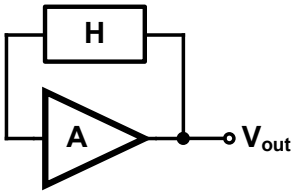


Figure 2.11. Oscillation loop.

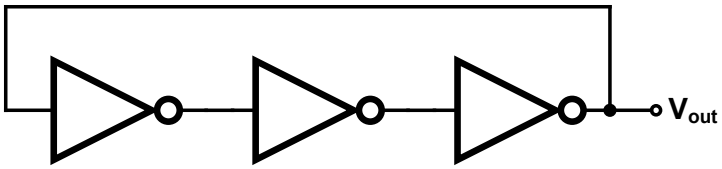


Figure 2.12. Simplified block diagram of ring oscillator.

Figure 2.11 shows the concept of another type of electrical oscillators known as *negative resistance oscillators*. The oscillator structure consists of a passive resonator (e.g. a parallel LC resonator) and a negative resistance part that compensates the loss of the passive network to maintain the oscillation. Generally, negative resistance oscillators offer a better phase noise performance compared to the ring oscillator. The following oscillator structure operates based on the negative resistance mechanism.

Class-B oscillator as one of the basic structures of negative resistance oscillators is shown in Figure 2.14 [15]. The parallel LC tank is tuned at a desired oscillation frequency. The cross couple transistors provide a negative resistance to compensate for the loss of the LC network

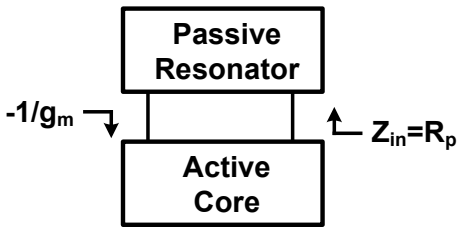


Figure 2.13. Negative resistance oscillator.

and sustain the oscillation. The current source is also adopted to control the amount of current flowing into the transistors and hence, power consumption of the oscillator. The output waveform of the oscillator is similar to class-AB PA. Therefore, it has a moderate power efficiency as well as its phase noise performance.

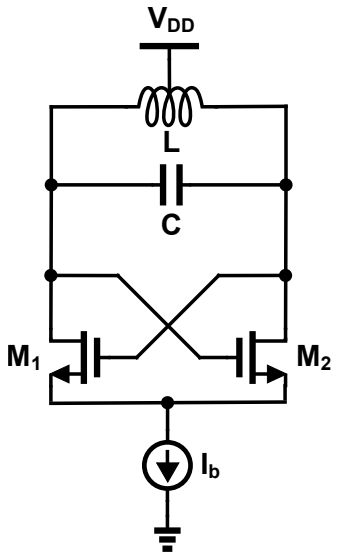


Figure 2.14. Schematic of class-B oscillator.

On the other hand, class-C oscillator [Figure 2.15] offers a better efficiency since the cross couple transistors are biased to operate in a small portion of each oscillation cycle [16]. This makes the output voltage waveform similar to class-C PA that indicates better power efficiency compared to class-B oscillator. However, it could cause start-up issues since the loop gain may not be sufficiently great to start the oscillation. Further, the output voltage swing is limited since the transistor must operate in the saturation region and excess voltage swing across gate-drain of the core transistor pushes them into triode region. As a result,

the charge in the tank is drained into the ground through the tail capacitor and reduce the quality factor of the tank. Thus the phase noise of the oscillator significantly increases.

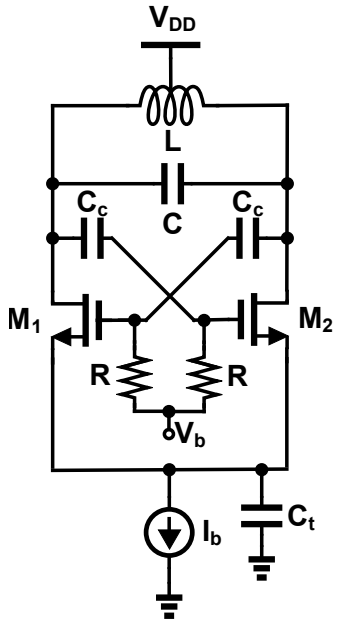


Figure 2.15. Schematic of class-C oscillator.

Figure 2.16 shows the schematic of class-D oscillator [17]. The operation mechanism of this structure is similar to switching class-D PA. The size of the cross coupled transistors must be sufficiently large so that they can behave close to ideal switches. In this way, the overlap between current and voltage at the drain of the transistors across the passive tank minimizes that maximizes the power efficiency. Although the transistors generates large amount of noise by their on resistance when they completely turned on, the generated noise does not translate to the phase noise, as it will be discussed in the next section. Therefore, this oscillator class provide an excellent phase noise performance, however, its operating frequency is limited since the switches must behave as ideal switches that is not feasible at high frequency due to parasitics of the transistors.

Figure 2.16 shows class-F oscillator structure with more complex design [18]. The oscillation tank is composed of a coupled transformer that is able to provide high impedance at first

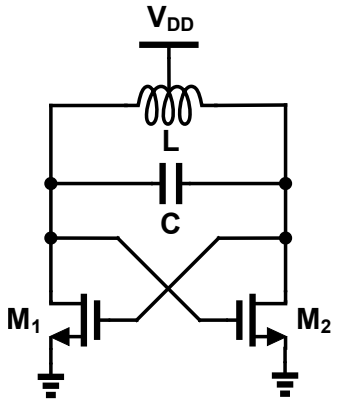


Figure 2.16. Schematic of class-D oscillator.

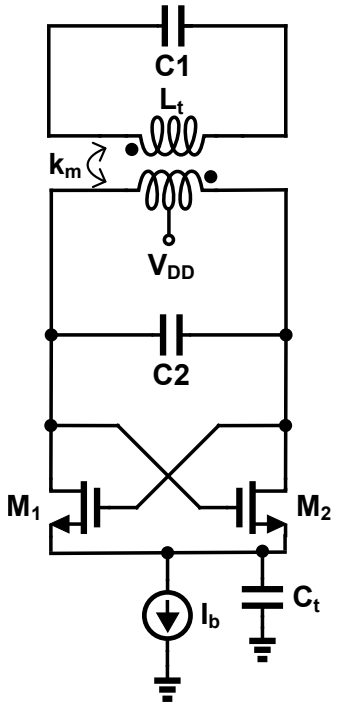


Figure 2.17. Schematic of class-F oscillator.

and third harmonics. Therefore the shape of the voltage at the drain of the transistors becomes square shaped waveform. This makes the rising and falling edges of the voltage waveform sharp and reduces the effective time of the noise to phase noise translation and hence, reduces the phase noise. This is achieved at the cost of additional design complexity.

2.4.2 Linear Time Variant Phase Noise Theory

In order to evaluate the phase noise performance of the electrical oscillators the phase noise theory introduce in [19] can be used. The following equation expresses the phase noise of the oscillator.

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{\sum_i N_{L,i}}{2\Delta\omega^2 C^2 A_{sw}^2}\right) \tag{2.2}$$

where $\Delta\omega$ is the offset frequency from the carrier, C is the equivalent capacitance at the output node of the oscillator and A_{sw} is the output voltage swing. $N_{L,i}$ is also the noise contribution of i^{th} device in the total phase noise defined as

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} \Gamma_i^2(t)\bar{i_{n,i}^2}(t)dt \tag{2.3}$$

where $i_{n,i}$ is the generated noise by i^{th} device and Γ_i is a dimensionless periodic function called *impulse sensitivity function (ISF)* that shows the sensitivity of the phase of the voltage waveform to the injected noise across an oscillation cycle. Figure 2.18 demonstrates how ISF is calculated. The noise of the tank and the main transistor is modeled using a current source (i.e. i_{tr} and i_t). Now, let's assume the current sources inject a current pulse into the output node of the oscillator [see Figure 2.19]. It can be seen that the resultant phase shift in the voltage waveform is dependent on the applying time of the pulses. If the pulse is applied at

its peak, it does not affect the phase of the waveform. However, applying the pulse around zero crossing can have a significant impact on the phase of the output voltage. Repeating the same procedure at different times across an oscillation cycle results in ISF waveform that identifies the sensitivity of the oscillator output to the injected current pulses.

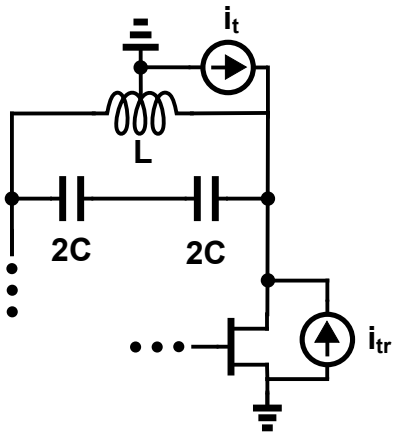


Figure 2.18. Noise injection model.

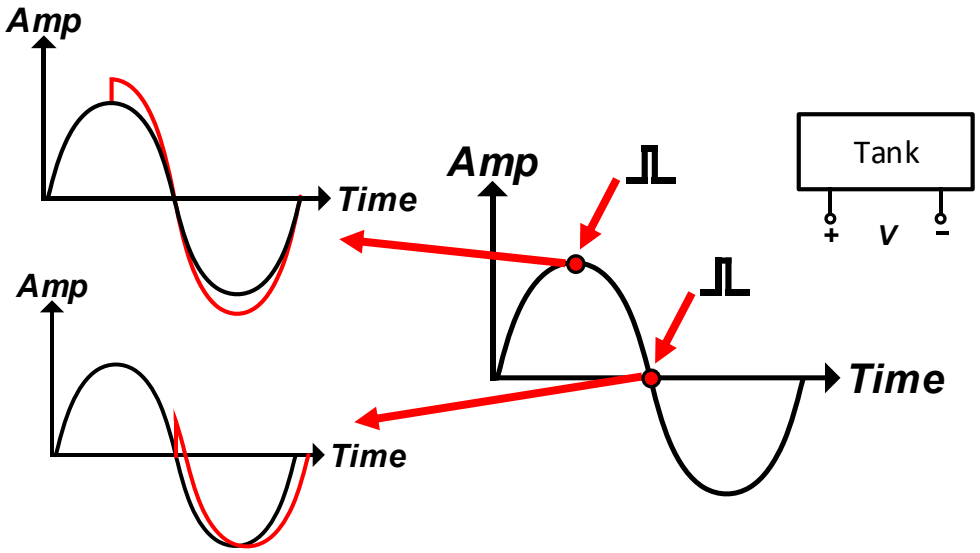


Figure 2.19. Impact of the injected noise on the output voltage waveform.

The ISF function of a parallel LC tank in class-B oscillator structure is shown in Figure 2.20. It can be seen that it is a sinusoidal waveform with 90° phase different with the original voltage waveform that indicates the sensitivity of the output voltage to the noise around its zero crossings.

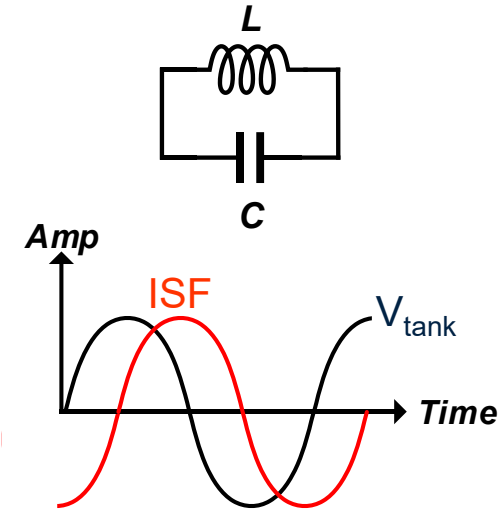


Figure 2.20. ISF of the LC tank in class-B oscillator.

Chapter 3

Temperature Compensated Transmitter Design for Phased-Array Applications

3.1 Introduction

High temperature electronic applications include but are not limited to; fuel industry, military, aviation, space exploration and geothermal energy exploitation [20–22]. The operating temperatures in the aforementioned applications can exceed 200 $^{\circ}C$, creating severe reliability and operation concerns at the circuit level. In the standard silicon-based electronics (i.e. CMOS), the increase in the ambient temperature results in a significant variation in the circuit performance. Their failure rate also doubles for every 10 $^{\circ}C$ increase in the operating temperature above 200 $^{\circ}C$ [6]. This makes the CMOS circuits impractical for high temperature applications.

Furthermore, the requirements of advanced communication systems push the circuit design approaches toward more dense architectures (i.e. phased array transceivers) [23, 24]. Thus, the excess heat produced by the dense power amplifier (PA) array can severely degrade the overall performance of the RF frontend (e.g. output power and gain) and hence, the communication system. Therefore, conventional heat extraction techniques have been used to compensate for temperature variation that require a significant increase in complexity, weight, and power consumption.

Unlike CMOS electronics, gallium-nitride (GaN) on silicon carbide (SiC) high electron mobility transistors (HEMTs) are promising candidates for high temperature RF circuit design [6]. The GaN HEMT offers a reliable operating lifetime at ambient temperatures up to 300 $^{\circ}C$ due to their large bandgap voltage (E_g). Further, high breakdown voltage and transition frequency (f_T) make the GaN HEMT suitable for RF and high power electronics. Although GaN HEMTs can reliably operate at high temperature, they, similar to other process technologies are susceptible to temperature variation. Therefore, compensation techniques are required to minimize the temperature impact on the performance of the circuit. Several temperature compensated building blocks of the traditional RF transceivers have been previously proposed [25–33]. In this dissertation however, we seek a transmitter design and its building block for RF phased array applications that can reliably operate at temperatures up to 220 $^{\circ}C$. We investigate the temperature effects on the performance of each individual building blocks and propose temperature compensation approaches that offer a feasible compromise between complexity, power and compensation effectiveness.

The rest of this chapter is organized as follows. The design procedure of a temperature compensated PA is discussed in Section 3.2.

3.2 Design of a 5 GHz temperature compensated PA

Variation in the performance of the PAs over temperature can significantly reduce the reliability and stability of the system at high temperature due to change in characteristics of the active components [34]. Several works have been represented to compensate the temperature effects on the specifications of the PA [35–38]. In [35], a temperature sensor composed of diodes and resistors is proposed to adjust the gate bias of the power transistors. By increasing ambient temperature, the sensor compensates the reduction in drain current by increasing the gate bias voltage. However, the variation in diode current is limited to 1 mV/°C, hence, several diodes must be used to provide enough voltage increasing rate with temperature at the gate of the power transistors. This increases the complexity of the circuit, since each diode should be biased at a desired dc voltage. In [36], a more complicated sensor along with an amplification stage is introduced to tune the gate bias with temperature. A transistor is used as an amplifier to boost the output voltage of the temperature sensor and deliver it to the gate of the power transistor. The proposed approach is capable of suppressing the gain variation of the amplifier by only 40 percent and the gain of the PA still shows a significant variation over temperature range.

An adjustable digital attenuator is used to compensate for temperature variation in [37]. The compensation is performed by adjusting the PA input power level by applying high attenuation on the input powers at low temperatures and the attenuation level reduces as the temperature increases. The attenuation at the input of the PA reduces the PAE since all of the input power is not delivered to the transistor of the first stage. This is not desired in many applications since the PA offers a limited PAE. In addition, the proposed PA needs a logic circuit and a temperature sensor to update the logic of the attenuator with temperature and resultantly makes it very complicated to design and implement.

In [38], a compensation circuit using a temperature diode sensor and off-chip modules have been proposed to regulate gate bias of the transistor in order to increase the drain current at high temperature and keep the gain constant. However, employing modules that are implemented in different technologies makes integration of the proposed gate biasing in the target process infeasible. A temperature compensated class-AB PA with two stages on BiCMOS Hetero-junction Bipolar Transistor (HBT) is presented in [39]. A voltage control unit is used at the gate of the main transistor of each stage to control the overall power gain of the PA. Although the proposed compensated circuit is able to control the gain, using two compensation units adds to the complexity of the design. Further, adopting the introduces approach for the PA structures with only one stage may not provide enough compensation over the temperature. The maximum temperature range in all of the aforementioned approaches are limited to 120 °C.

To address the shortcomings in the previous works, a novel compensation method is presented in this paper to reduce the variation in the PA performance over a wide range of temperatures. The proposed method takes advantage of temperature effects on the drain current of the transistors. The sensor amplifies these variations to produce a dc voltage that is proportional to temperature changes. Then, the generated dc voltage will apply to the gate of the main transistors to adjust the drain current and achieve a stable gain and output power performance over temperature.

3.2.1 Temperature Dependency of the Transistor Characteristics

Threshold voltage (V_T) and electron mobility (μ_n) of the transistor are two key factors that determine the specifications of a PA, such as gain, output power, linearity, efficiency, etc. [39, 40]. Furthermore, by increasing the temperature both of these parameters decrease and hence, output power and gain of the PA [34,41]. To investigate the performance variation

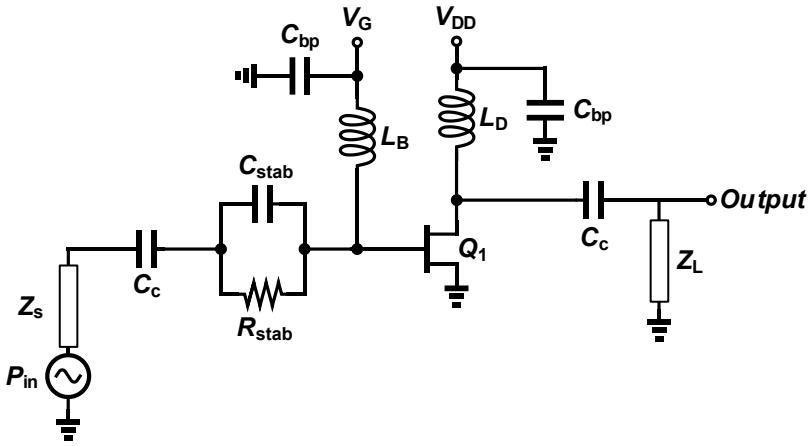


Figure 3.1. Schematic of the setup used for transistor simulations.

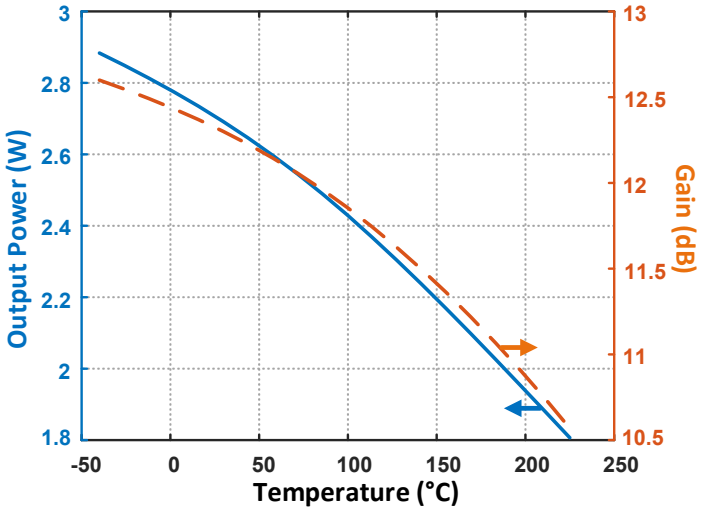


Figure 3.2. Variation in output power and gain of the transistor in the setup shown in Figure 3.1, versus temperature.

of the PA, the following steps have been followed:

1. Load pull (LP) and source pull (SP) simulations are performed to determine the transistor sizing and the optimum impedances at the load and source sides of the transistor to obtain the target power at the drain of the transistor at room temperature.
2. The load and source impedances are fixed at the optimum values from step 1.
3. By sweeping the ambient temperature, the variation in characteristics of the transistor are measured through harmonic balance (HB) simulation.

Figure 3.1 shows the schematic of the simulation setup including a stabilization circuit composed of the parallel combination of Rstab (3 Ω) and C_{stab} (2 pF) in series with the gate of the transistor. The transistor is a Wolfspeed Cree 28 V GaN HEMT and its non-linear model including self-heating mechanism is provided by the foundry. The gate bias voltage (V_G) is set to be -2.5 V to make sure that the amplifier operates under class-AB. Figure 2 shows the variation of the output power and gain of the transistor versus temperature at the input frequency of 5 GHz for a 4×250 μm transistor with the gate length of 0.4 μm. It can be seen from Figure 3.2 a significant reduction in the gain and output power of the transistor while ambient temperature increases from -40 °C to 225 °C due to increase in V_T that results decrease in the dc component of the drain current.

3.2.2 Proposed Compensation Circuit

In order to compensate the reduction in drain current of the transistor, V_G can be tuned to cancel out the effect of the temperature on V_T. The compensated V_G can be simply given by

$$V_G(T) = \alpha(T - T_0) + V_{G0} \tag{3.1}$$

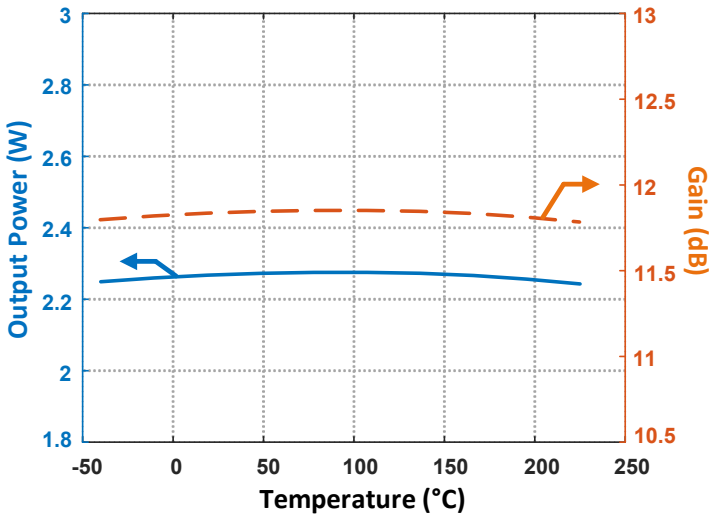


Figure 3.3. Variation in output power and gain of the transistor in the setup shown in Figure 3.1 using adaptive gate voltage in (3.1) with $\alpha = 6\ mV/°C$ versus temperature.

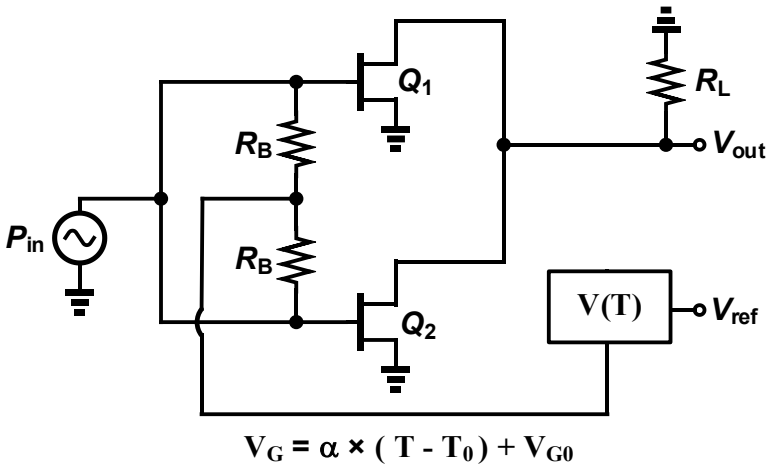


Figure 3.4. Simplified schematic of the proposed compensation circuit.

where, α is the increasing rate of V_G with temperature, T is temperature and V_{G0} is the gate dc voltage at minimum temperature, T_0. Figure 3.3 shows the output power and gain over temperature range using adaptive bias in (3.1) for the transistor in Figure 3.1. To achieve the maximum gain and power flatness, α is estimated from the simulations to be 7 $mV/°C$. This means, to use the proposed compensation circuit in [35], seven diodes would be needed to provide enough variation in bias voltage for each transistor. This would significantly increase the complexity and area of the circuit. The variation over the wide temperature range is only 0.07 W for the output power and 0.1 dB for the gain of the transistor. Additionally, unlike the previous works, the output power of the proposed PA at its maximum temperature of 225 $°C$ is equal to the output power at the minimum temperature of -40 $°C$. Figure 3.4 shows the simplified schematic of the PA incorporating the proposed compensation block.

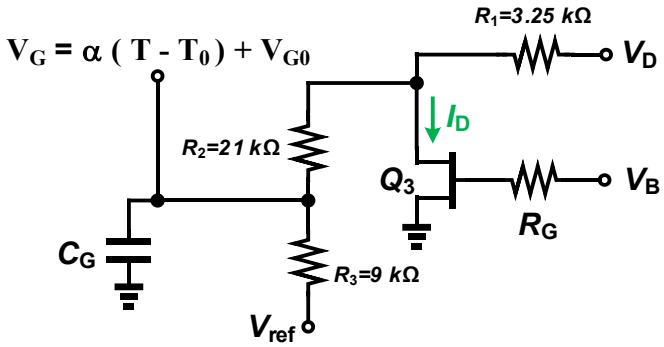


Figure 3.5. Schematic of the temperature sensor.

As the first improvement, two transistors, with the half width of the transistor shown in Figure 3.1, are used in the main stage. This allows the temperature, produced by dc power dissipated inside the transistor, to distribute between the two transistors and prevents of accumulation of heat in a single transistor. Accumulation of heat increases the junction temperature and could cause thermal runaway and transistor failure [6]. The sensor block, $V(T)$, generates the desired dc bias voltage, V_G in (3.1) and delivers it to the gate of the transistors $Q_{1,2}$ through bias resistors R_B. The reference voltage, V_{Ref} is used to tune the initial bias voltage, V_{G0} at the temperature of -40 $°C$. Figure **??** represents the schematic

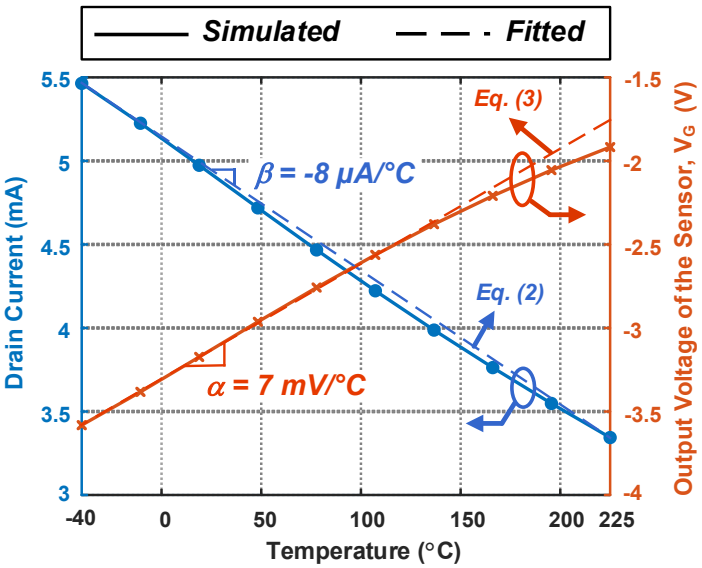


Figure 3.6. Simulated drain current of Q_3 and output voltage of the sensor versus temperature.

of the temperature sensor. The transistor, Q_3 represents a temperature dependent current source which can be modeled at the linear region as following.

$$I_D(T) = \beta(T - T_0) + I_{D0} \tag{3.2}$$

where, β is the reducing rate in the drain current of the transistor versus temperature and I_D0 is the drain current at the minimum temperature, T_0. β in (3.2) is governed by V_B and sizing of the transistor [39]. Q_3 is biased at its peak transconductance ($g_{m,MAX}$) point in which the drain current of the transistor has its maximum sensitivity to the temperature variation and maximizes β. Figure 3.6 shows simulated drain current of Q_3 versus temperature. β can be approximated from slope of the fitted line to the I_D curve to be -8 $\mu A/°C$. The approximation causes only 4% error in the drain current in (3.2) compared to the simulated I_D. V_G is simply driven from Figure 3.5 to be

$$V_{G0}(T) = \frac{R_3}{R_1 + R_2 + R_3}\left(\frac{R_1 + R_2}{R_3}V_{ref} + V_D - R_1 I_D(T)\right) \tag{3.3}$$

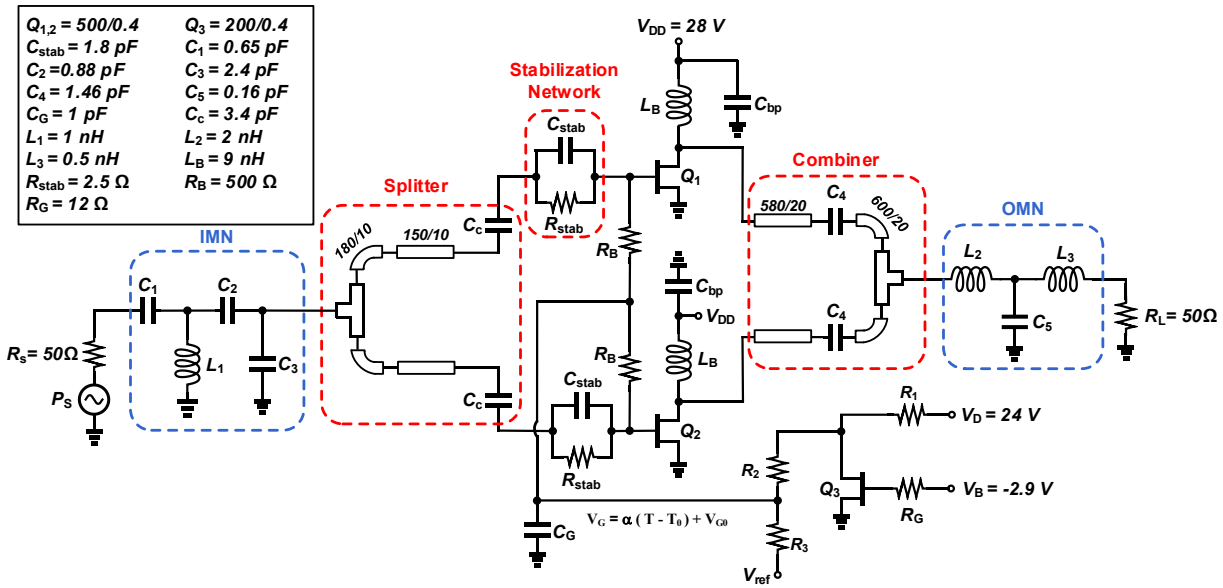


Figure 3.7. Schematic of the proposed PA including temperature compensation circuit.

It can be noticed from (3.2) that increase in temperature results in decrease in I_D, since β has a negative value. Furthermore, by decreasing I_D, V_G in (3.3) increases and hence, drain current of the power transistors. Equation (3.3) is plotted in Figure 3.6. By substituting (3.2) in (3.3), V_{G0} in (3.1) is found to be

$$V_{G0}(T) = \frac{R_3}{R_1 + R_2 + R_3}\left(\frac{R_1 + R_2}{R_3}V_{ref} + V_D + R_1(\beta T_0 - I_{D0})\right) \tag{3.4}$$

As it is obvious from (3.4), initial bias voltage. V_{G0} can be tuned using V_{ref}. α in (3.1) also can be calculated from (3.3) to be

$$\alpha = \frac{-R_1 R_3}{R_1 + R_2 + R_3}\beta = 7\ mV/^{\circ}C \tag{3.5}$$

As it can be seen in Figure 3.6, compensating the output power variation over a wide range of temperatures requires large increasing rate (α) of V_G that indicates incapability of the previous compensation approaches. Figure 3.7 shows the schematic of the proposed PA. The input matching network (IMN) and output matching network (OMN) are composed of

transmission lines and lumped elements. These elements, along with the power splitter and power divider, are designed to deliver the maximum efficiency at desired output power of 2.5 W (34 dBm) at the frequency range from 4.5 GHz to 5.5 GHz. The IMN and OMN introduce 0.38 dB and 0.43 dB loss, respectively over the frequency range. Output voltage of the temperature sensor is fed into the gate of the main transistors through resistors, R_B.

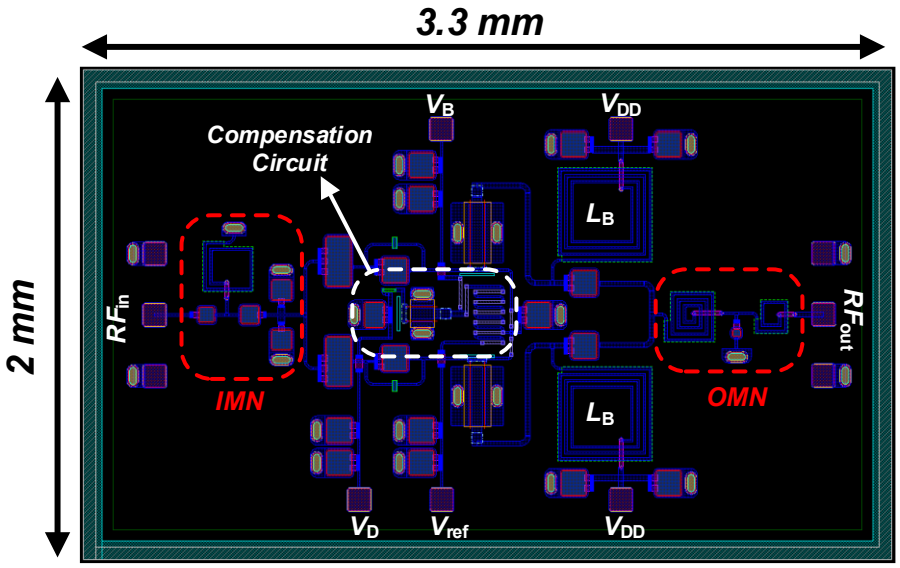


Figure 3.8. Layout of the proposed PA.

3.2.3 Post-Layout Simulation Results

The layout of the PA is shown in Figure 3.8. Electromagnetic (EM) simulations are performed in Keysight EEsof EDA, Advanced Design System (ADS) to consider the parasitic and coupling effects in the circuit. The simulation results for the efficiency and output power are shown in Figure 3.9 (a). The compensated PA introduces 78% less output power variation compared to the uncompensated one.

In addition, to compensate the temperature effect in the drain current, the PA dissipates higher dc power in the main transistors as their gate bias voltage (V_G) increases by increase in the temperature. Higher dc power dissipation causes reduction in the power added efficiency

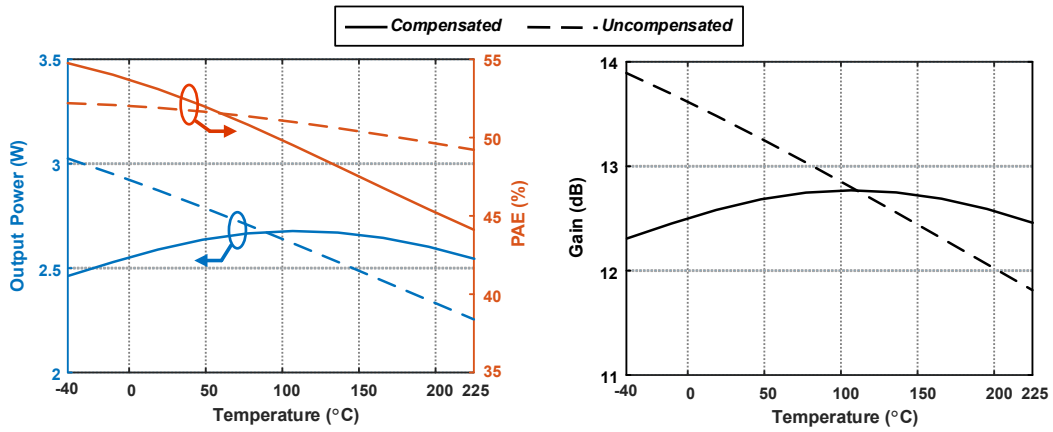


Figure 3.9. Simulated (a) output power, PAE and (b) gain of the proposed temperature compensated PA at 5 GHz.

(PAE) with temperature while the power gain remains constant. It is noteworthy that the power consumption of the sensor does not considerably affect PAE, since it consumes only 2% of the total DC power consumption of the circuit. Figure 3.9 (b) shows the power gain of the PA. 12.5 dB gain is achieved with the help of parallel combination of two power transistors with 0.4 dB variation over the temperature range.

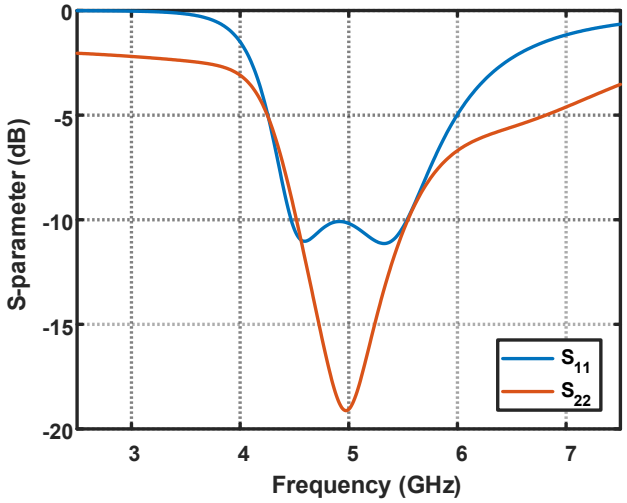


Figure 3.10. Input and output S-parameters of the PA at 225 °C.

The simulated S-parameters at the input and output of the PA at 225 °C are presented in Figure 3.10. The matching network are optimized to match the PA at its input and

output over the frequency range from 4.5 to 5.5 GHz. It is worth noting that variation in temperature changes input and output impedances of the PA and hence, S-parameters. However, the changes in the S-parameters do not cause significant variation in the output power as it is shown in Figure 3.11. It can be seen that the output power shows only 7% variation over the temperature and frequency range.

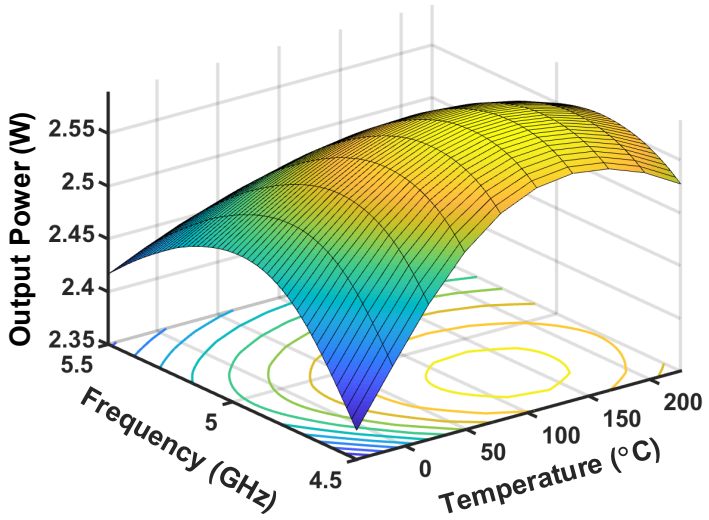


Figure 3.11. Output power of the PA versus temperature and frequency.

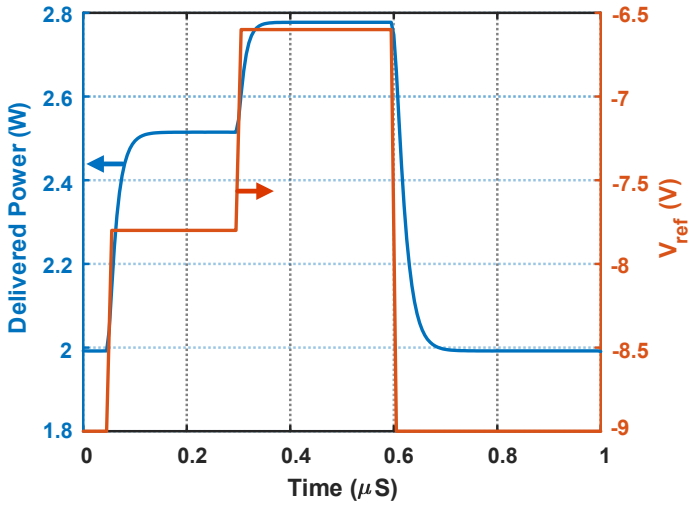


Figure 3.12. Applied step voltage of V_{ref} and output power response at 5 GHz.

Although the compensation sensor is a low frequency open loop circuit, envelope simulation has been performed to assure the stable performance of the PA incorporating temperature

sensor. For this purpose, a step function is applied to the reference voltage input of the sensor and fundamental component of the output power is measured. Figure 3.12 shows the step function and the output power of the PA. It can be seen that PA responses to the voltage steps like a single pole system since the dominant pole is intentionally located at low frequency by adding capacitors (C_G) at the gate feeding path. Upper and lower side band third intercept points (IP3) at the output of the PA over the temperature range is shown in Figure 3.13. The reduction in OIP3 with temperature is mostly due to the fact that the fundamental component of the transconductance of the main transistors, $Q_{1,2}$ decrease by increasing the temperature [42]. The proposed PA introduces approximately, 2 dB variation in OIP3 with the minimum of 34 dBm at 225 $°C$. Table 3.1 compares the proposed PA with previous high temperature PAs. The proposed approach is able to compensate the temperature effect in the gain of the PA over widest temperature range while introduce lowest variation in the gain among high power MMIC PAs.

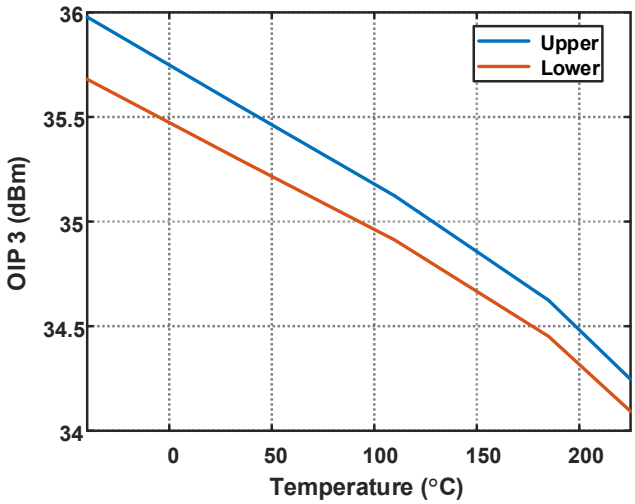


Figure 3.13. Upper and lower side output IP3.

Table 3.1: Comparison of Temperature Compensated PAs

Ref.	Process	V_{DD} (V)	Frequency (GHz)	P_{out} (dBm)	PAE (%)	Area (mm^2)	Temperature Range (°C)	Gain Variation (dB)[b]
[35]	GaAs MESFET	7	6.5 – 10.5	23.5	37	12.58	-10 / +80	1.3 @ 30 dBm
[36]	GaAs pHEMT	3	8 - 16	[c]N/A	N/A	1.17	-25 / +75	1 @ 17.8 dBm
[37]	GaAS pHEMT	4	74 - 82	12	8	0.12	-20 / +100	2.1 @ 15 dBm
[38]	GaAs	9	13.7 - 14.2	43	17	N/A	+40 / +80	N/A
[39]	BiCMOS HBT	3.85	5 - 6	16.5	N/A	0.01	+25 / +180	0.2 @ 26.3 dBm
This Work[a]	GaN HEMT	28	4.5 – 5.5	35	55	6.6	-40 / +225	0.5 @ 12.5 dBm

[a] Post-layout simulation results. [b] Over temperature range. [c] N/A indicates not available.

3.3 Design and Performance Investigation of a Temperature Compensated Transmitter with GaN HEMTs for Phased-Array Applications

In this chapter, the detailed design of a temperature compensated transmitter is described. The transmitter is composed of a tunable and active variable gain phase shifter along with an inverse class-F PA. Furthermore, the procedure of establishing transconductance zero temperature coefficient is discussed. The temperature effect on the individual blocks and the quality of the communication (e.g. EVM) is investigated through simulation and measurements results.

3.3.1 Temperature effect on the transconductance of GaN HEMT

Although GaN HEMT process technology is suitable for high temperature RF circuit design, the variation in its charachteristics can cause a significant variation in the overall performance of the system and a failure in extreme scenarios with wide operating temperature range. The drain current (I_D) and its corresponding transconductance (g_m) are among the most

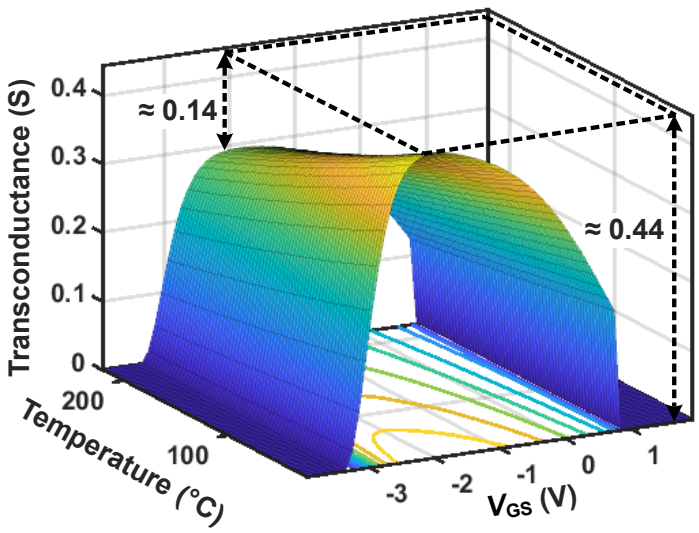


Figure 3.14. Simulated variation in the transconductance of the GaN HEMT versus temperature. The simulation is performed using the large signal model of a Cree CGH40006P packaged GaN on SiC HEMT with $V_{DS} = 5\ V$.

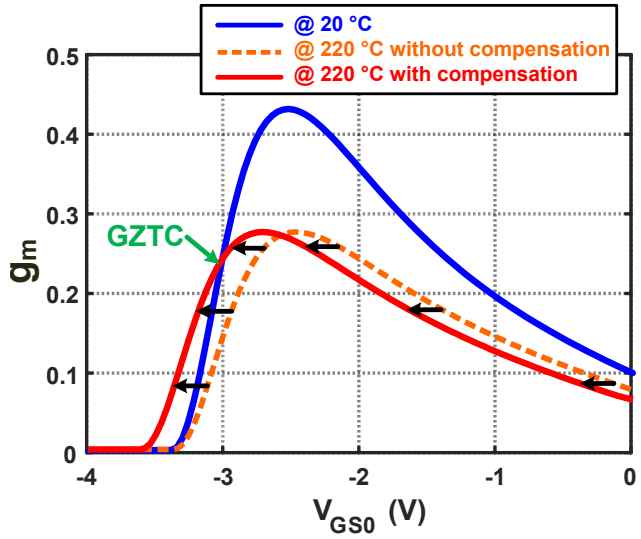


Figure 3.15. Establishing the GZTC bias point of GaN HEMT.

important properties of the transistor. Thus, their variation with temperature must be studied in order to gain a proper insight into design procedure of the transmitter and further compensation techniques.

Figure 3.14 shows the drain current of the GaN HEMT versus temperature and gate-source bias voltage. As it can be seen, g_m of the transistor reduces by 32% when temperature increases from room temperature to 220 °C. This reduction can be explained by reviewing the physics of the GaN HEMT. The increase in the temperature of the transistor substrate causes a decrease in the 2-DEG sheet charge density and the electrons saturation velocity [7]. This reduction in the drain current results in a reduction in g_m of the transistor that leads to a decrease in the voltage gain of the individual building blocks.

3.3.2 Establishing transconductance ZTC

Unlike CMOS and gallium-arsenide (GaAs) process technologies, GaN HEMT does not offer transconductance ZTC (GZTC) [43, 44]. Thus, regardless of the bias voltage, the drain current and its corresponding g_m vary with temperature as it is shown in Figure 3.15. Now, let's assume the gate of the transistor is biased by a temperature dependent dc voltage source as

$$V_{GS}(T) = V_{GS_0} + (T - T_0) \cdot \alpha \tag{3.6}$$

where, V_{GS_0} is the dc voltage across gate-source of the transistor at room temperature (T_0), T is absolute temperature, and α is the increasing ratio of V_{GS} with temperature. The temperature dependent term in (3.6) makes a relative shift equal to $(T - T_0) \cdot \alpha$ in the g_m curve, as it is illustrated in Figure 3.15. It can be seen in the figure that the relative shift in the g_m curve by increasing temperature introduces a ZTC point at the cross point of the g_m curves at 20°C and 220°C. Furthermore, the bias voltage in which the GZTC point occurs at, can be moved toward higher or lower bias voltages by adjusting α to obtain a desired temperature independent g_m value.

In order to provide the temperature dependent bias of the transistors, an auxiliary temperature sensor can be utilized. Figure 3.16 shows the schematic of the temperature sensor and the dc level shifter [29]. Since the transistor (Q_S) experiences the same temperature variation as the main transistors in the circuit, its drain current can be given by a linear function of the temperature [7]

$$I_{DS}(T) = I_{DS_0} + (T - T_0) \cdot \beta_S \tag{3.7}$$

where, I_{DS_0} is the drain current of the sensor transistor Q_S at room temperature, and β_S is the decreasing factor of the drain current with temperature. Hence, the output voltage of the sensor can be calculated as

$$\begin{aligned} V_S(T) = & \left[\frac{V_{ref}(R_{S1} + R_{S2}) + V_{DS} - R_{S1}R_{S3}I_{DS_0}}{R_{S1} + R_{S2} + R_{S3}} \right] \\ & + (T - T_0) \cdot \left[\frac{-R_{S1}R_{S3}\beta_S}{R_{S1} + R_{S2} + R_{S3}} \right] \end{aligned} \tag{3.8}$$

Finally, α and V_{GS_0} can be calculated by comparing (3.8) with (3.6).

$$V_{GS_0} = \frac{V_{ref}(R_{S1} + R_{S2}) + V_{DS} - R_{S1}R_{S3}I_{DS_0}}{R_{S1} + R_{S2} + R_{S3}} \tag{3.9}$$

$$\alpha = \frac{-R_{S1}R_{S3}\beta_S}{R_{S1} + R_{S2} + R_{S3}} \tag{3.10}$$

It can be noticed from (3.9) and (3.10) that α can be independently controlled through β_S

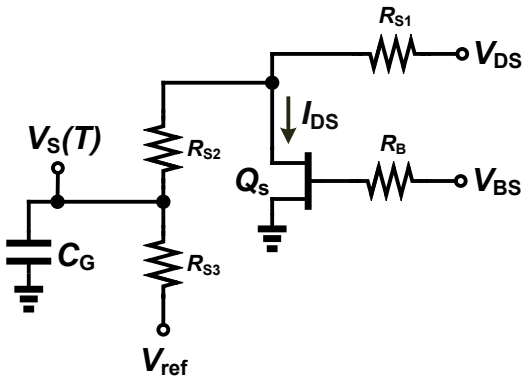


Figure 3.16. Schematic of the temperature sensor.

while V_{ref} is used to adjust V_{GS_0} at room temperature. It should be noted that β_S can be adjusted through dc bias and size of the transistor.

3.3.3 Proposed transmitter

We introduce the design methodology of a variable gain phase shifter (VGPS) in this section. The temperature effects on the performance of the building blocks including PA are investigated and the compensation techniques are adopted for minimizing the temperature impact on the circuit performance.

3.3.4 Evolution toward variable gain phase shifter

Phase shifters are inseparable blocks in phased array transceivers and their performance determine the key specifications of the communication system. Compact size, high insertion gain, wide range of insertion phase are the properties that make active phase shifters attractive for phased array applications [45]. However, the use of active components in their structure dictates the necessity of compensation techniques to suppress the impact of the temperature on their characteristics and thus, the performance of the circuit. The phase

shifters based on I/Q vector modulator and all-pass network are two popular categories of active phase shifters [46–53]. The vector-based phase shifters offer excellent phase and gain accuracy. However, their implementation requires complex circuitry and thus, adopting the temperature compensation approaches becomes impractical. On the other hand, the phase shifters based on all-pass filter offer a reasonable accuracy while requiring simpler circuit architecture. Therefore, the temperature compensation methods can be beneficial for minimizing the temperature effects on its performance.

Figure 3.17 (a) shows the simplified schematic of the introduced phase shifter. This structure was firstly introduced as an active all-pass filter using a transmission line (Z) with a fixed electrical length in the feed through path [54]. Viveiros et. al modified the circuit by replacing the transmission line with a series LC resonator [3]. The series capacitance was implemented using a GaN transistor with its source and drain connected together to form a Schottky varactor as it is shown in Figure 3.17 (b). This enables the phase shifter to change the insertion phase by adjusting the capacitance of the varactor.

By observing the gain and insertion phase of the circuit, it can be noticed that a trade-off between the gain and phase sensitivity ($\partial \angle S_{21}/\partial C_v$) pose a design challenge to the phase shifter. In other words, a large capacitance range is required to achieve wide range of phase shift with a relatively high gain. However, since the capacitance range of the varactor is proportional to its size, a large transistor must be employed for implementing the varactor. This leads to an impractically small inductor and larger parasitics of the transistor. The design trade-off is illustrated in Figure 3.18. It can be seen that increasing gain results in decreasing the phase sensitivity.

In order to overcome the aforementioned issue, we propose an alternative parallel LC tank for Z as shown in Figure 3.17 (c). Using the same simplified transistor model as in [3], the voltage transfer function of the phase shifter can be calculated as

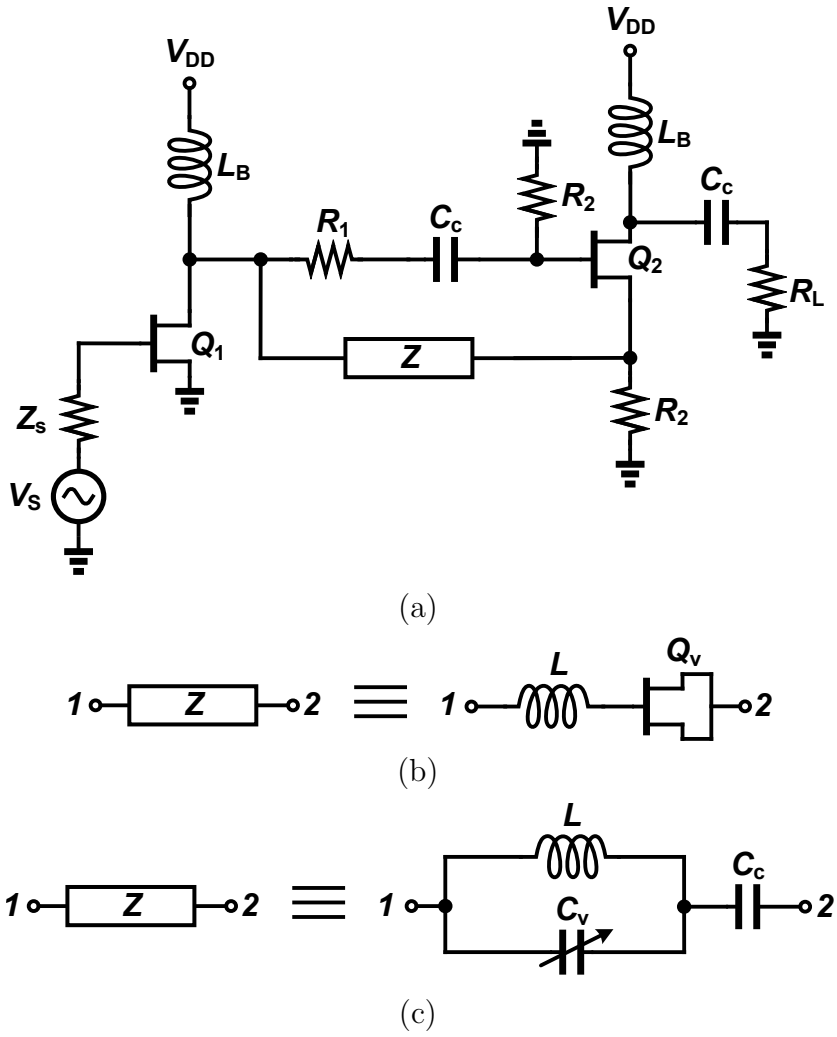


Figure 3.17. (a) Preliminary schematic of the phase shifter, and equivalent impedance for Z in (b) [3] and (c) proposed phase shifter.

$$S_{21} = K \cdot \frac{s^2 - \frac{R_2}{CR_1R_3}s + \omega_0}{s^2 + \frac{1+g_{m2}R_3}{C(R_1+R_2+R_3+g_{m2}R_1R_3)}s + \omega_0} \tag{3.11}$$

with

$$K = \frac{g_{m1}g_{m2}R_1R_3R_L}{R_1 + R_2 + R_3 + g_{m2}R_1R_3} \tag{3.12}$$

where, g_{m_1} and g_{m_2} are the transconductance of the transistors Q_1 and Q_2, respectively, and ω_0 is the the natural frequency of the filter. By comparing (3.11) with the standard form of the transfer function of the all-pass filter in (3.13)

$$S_{21} = \frac{s^2 - \frac{\omega_0}{Q}s + \omega_0}{s^2 + \frac{\omega_0}{Q}s + \omega_0}, \tag{3.13}$$

where, Q is the quality factor of the filter, the following criteria must be met in order to make the circuit in Figure 3.17 (a) to behave as an all-pass filter.

$$R_1 = \frac{R_2(R_2 + R_3)}{(R_3 - R_2)(1 + g_{m2}R_3)} \tag{3.14}$$

The insertion phase of the phase shifter can also be computed using (3.11) as

$$\phi = 2\tan^{-1}\left[Q\left(\frac{\omega}{\omega_0} - \frac{\omega_0}{\omega}\right)\right] \tag{3.15}$$

where, ω is the frequency of the input RF signal and Q can be calculated by comparing (3.11) and (3.13) as

$$Q = \frac{C\omega_0(R_1 + R_2 + R_3 + g_{m2}R_1R_3)}{1 + g_{m2}R_3} \tag{3.16}$$

To investigate the trade-off in the design, we calculate the phase sensitivity of the proposed circuit by substituting (3.14) in (3.16) and (3.16) in (3.15) and taking a derivation from (3.15). Figure 3.18 shows the gain and phase sensitivity of the introduced circuit in [3] and the proposed one. The resistance of R_1 is negative in the hachured area since R_2 becomes larger than R_3 in (3.14) at $f_0 = 2$ GHz. Both circuits offer the same amount of the voltage

gain while their corresponding phase sensitivity is different. As it can be seen, the phase sensitivity decreases by increasing the gain for the phase shifter circuit with equivalent Z in Figure 3.17 (b), while it increases with gain by replacing Z with the parallel LC tank. Thus, the maximum gain and phase shift, near the edge of the hachured area, can be achieved in the proposed circuit.

To study the performance variation of the phase shifter with temperature, we need to investigate the variation of the design parameters in (3.11) over the entire temperature range from 20 $^{\circ}C$ to 220 $^{\circ}C$. We assume the neutral frequency of the filter $f_0 = 2\ GHz$ and temperature coefficient (TC) of 500 $ppm/^{\circ}C$ for the lumped components which is sufficiently greater than what is for the typical high temperature commercial-off-the-shelf (COTS) components [55–57]. The inductor however, is implemented using microstrip transmission line (TL) on RO4003C hydrocarbon ceramic laminate due to unavailability of discrete lumped high temperature inductor. The thermal properties of high temperature RO4003C substrate such as thermal coefficient ε_r, 3D coefficient of thermal expansion (CTE) and thermal conductivity are considered in the temperature dependent simulations.

The TC of the varactor network is also measured and shown in Figure 3.19 along with its equivalent capacitance. The varactor network provides approximately 1.05 pF of capacitance range by sweeping the bias voltage V_{GS} inside the hachured area. Further, by choosing a transconductance of 250 mS for the transistors $Q_{1,2}$ at 20 $^{\circ}C$, their g_m drop by $\approx$ 30 % at 220 $^{\circ}C$, as it was shown in Figure 3.14. As it can be seen in Figure 3.20 (a), $g_{m1,2}$ has the major contribution in the variation of the gain with temperature. On the other hand, all circuit parameters in (S_{21}/K) expression contribute to the phase variation of the circuit with temperature as it is shown in Figure 3.20 (b).

A proper strategy to minimize the temperature impact on the gain and insertion phase of the circuit is minimizing the variation in $g_{m1,2}$ by adopting an adaptive gate bias voltage for

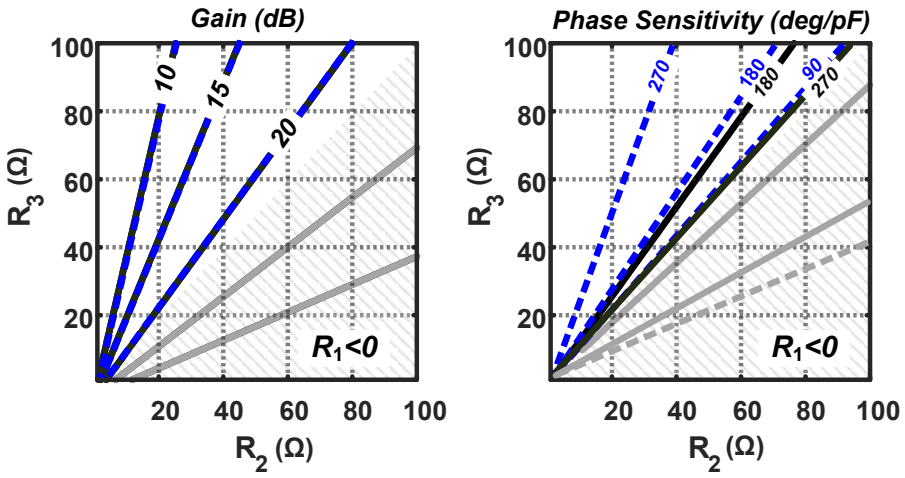


Figure 3.18. Calculated (a) gain, and (b) phase sensitivity of the introduced circuit in [3] (dashed line) and our proposed one (solid line).

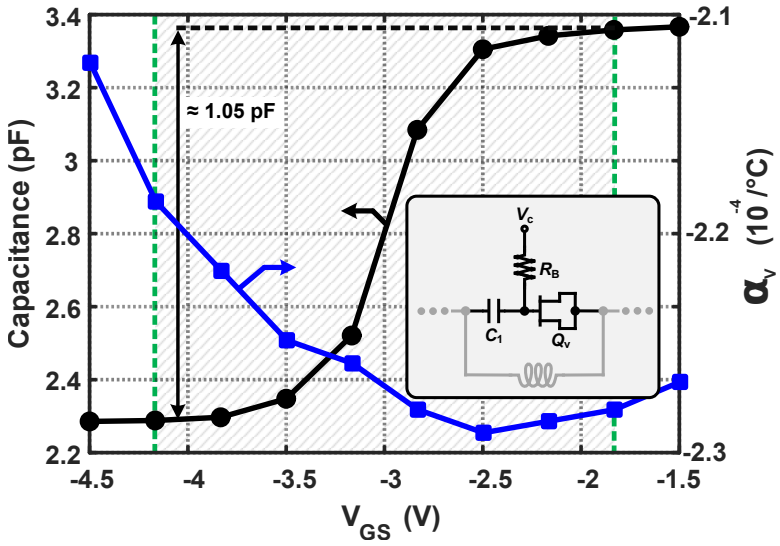


Figure 3.19. Measured equivalent capacitance of the varactor at room temperature and its corresponding TC.

$Q_{1,2}$ to form a GZTC bias point, as discussed in Section 3.3.2. This makes the capacitance of the varactor (C_v) a function of the ambient temperature as

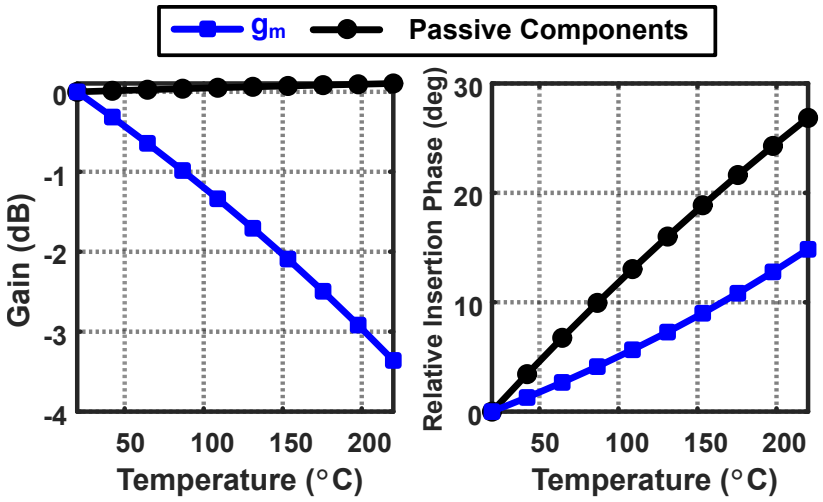


Figure 3.20. Calculated variation in (a) gain, and (b) insertion phase of the phase shifter versus temperature.

$$C_v(T) = (1 + (T - T_0) \cdot \alpha_v) \cdot C_{v_0} \tag{3.17}$$

where, C_{v_0} is the capacitance of the varactor at room temperature, T is absolute temperature, and α_v is the voltage dependent TC of the varactor's capacitance. As it can be seen in Figure 3.19, α_v has negative values in the bias voltage range of interest that can be attributed to the reduction of the number of charges under the gate [58]. Moreover, α_v can be estimated by a constant (≈ -2.2) since its variation with V_{GS} is negligible. In order to compensate the impact of the variation in the varactor capacitance and other passive components on the insertion phase of the phase shifter, the equivalent capacitance of the varactor can be adjusted through its bias voltage, V_{GS} as

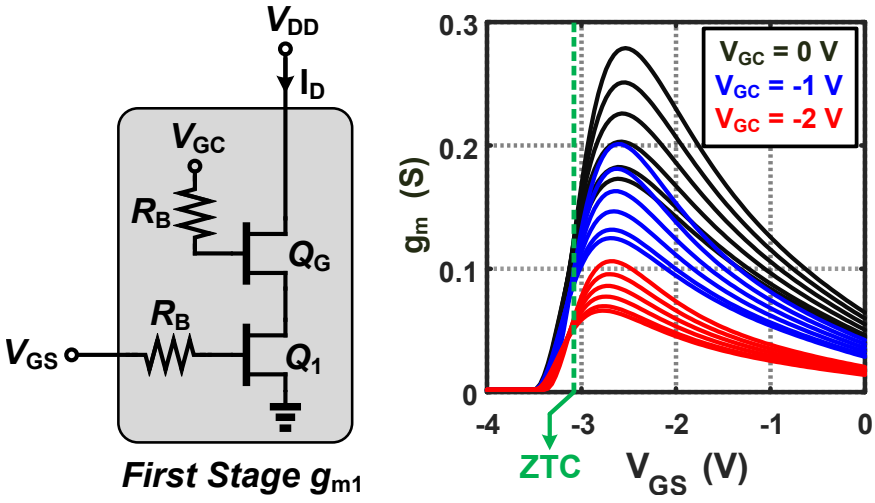
$$V_{GS}(T) = V_{GS_0} + (T - T_0) \cdot \beta_V \tag{3.18}$$

where β_V is the required increasing ratio in V_{GS} to completely compensate the variation of the

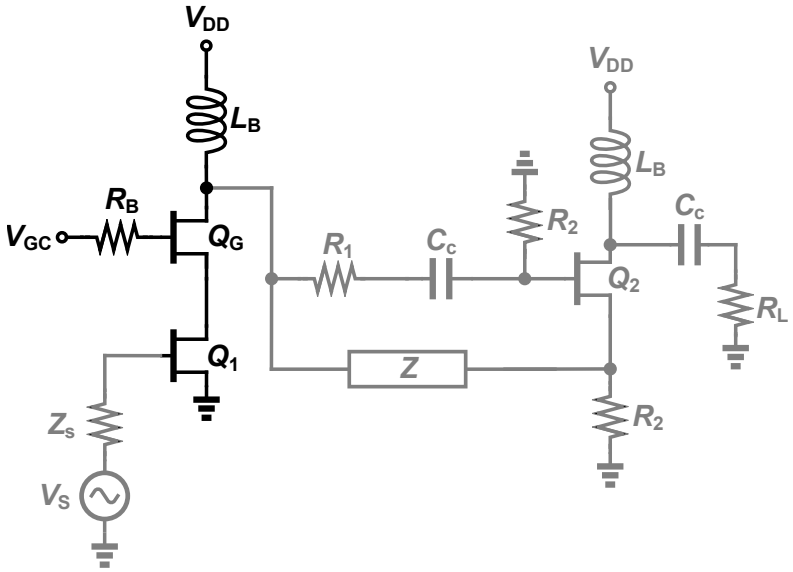
insertion phase with temperature due to the change in the value of the passive components. Simulation results showed that a $\beta_V = 1.4\ mV/^{\circ}C$ minimizes the variation in the insertion phase with temperature and is provided through temperature sensor.

Adopting a variable gain amplifier (VGA) stage in the transmit path is required to adjust the gain of the up-converted base-band (BB) signal before delivering it to the power amplifier. Several temperature compensated VGA blocks have been proposed previously [32, 59–61]. Although they offer a satisfactory performance in terms of reliability and gain stability, having a separate VGA block adds to the complexity of the temperature compensation circuitry, power dissipation and size of the circuit. Thus, we seek a solution to reduce the complexity of the circuit by merging the phase shifter and VGA stages into a single block.

By investigating in (3.11), we notice that the gain of the transfer function (TF) of the phase shifter is a function of $g_{m_{1,2}}$ while its insertion phase is a function of g_{m_2} but independent of g_{m_1}. Therefore, the transconductance of Q_1 can be utilized to change the gain of the phase shifter without any impact on the insertion phase of the circuit. The first solution is controlling g_{m_1} through gate bias voltage of Q_1, however, deviating the bias voltage from ZTC point could cause a significant variation in the gain with temperature. In order to mitigate this issue, the cascode structure in Figure 3.21 (a) is utilized as the first stage of the variable gain phase shifter (VGPS). As it is shown in Figure 3.21 (b), the GZTC point stays fixed by changing the gain control voltage (V_{GC}) of the cascaded transistor Q_G, while the equivalent g_m of the first stage can be independently controlled. Measurement results of a single GaN HEMT showed that the channel resistance of Q_G tends to increase with temperature, which is in an agreement with the results in [62]. This can affect the small-signal gain of the VGPS, however, it can be simply compensated by biasing Q_1 at slightly higher voltage than the GZTC (i.e. under-compensating). The modified schematic of the variable gain phase shifter is shown in Figure 3.21 (c) where the first stage is replaced by



(a) (b)



(c)

Figure 3.21. (a) Schematic of the first stage of the VGPS, and (b) its corresponding equivalent transconductance. (c) the simplified schematic of the proposed VGPS.

the cascode structure in Figure 3.21 (a).

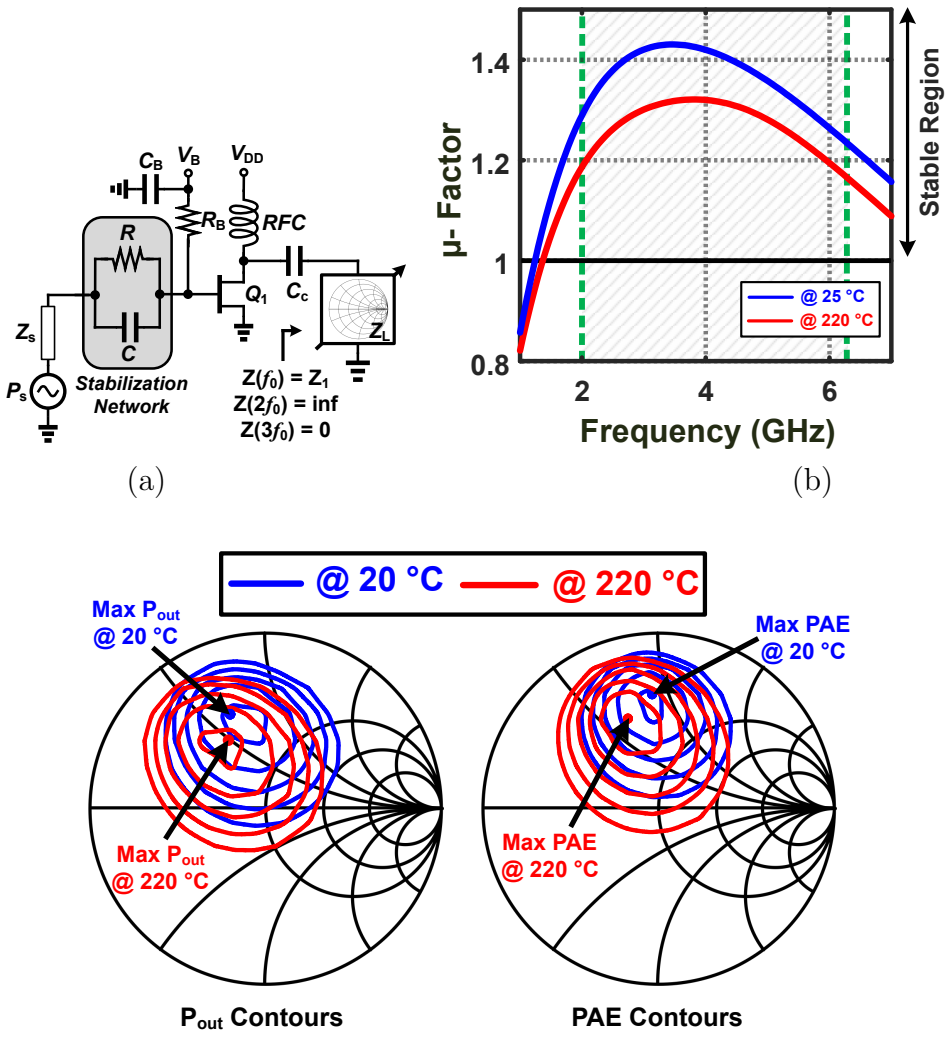


Figure 3.22. (a) Schematic of the load-pull test bench, (b) stability μ-factor of the transistor, and (c) corresponding inverse class-F load-pull contours.

3.3.5 High temperature PA design

As the final stage in the transmitter chain, the PA must provide a stable performance against temperature variation. However, the performance of a PA design without an implemented compensation technique is sensitive to temperature change that can result in a performance degradation. The previous PA designs that emphasized on temperature considerations tried

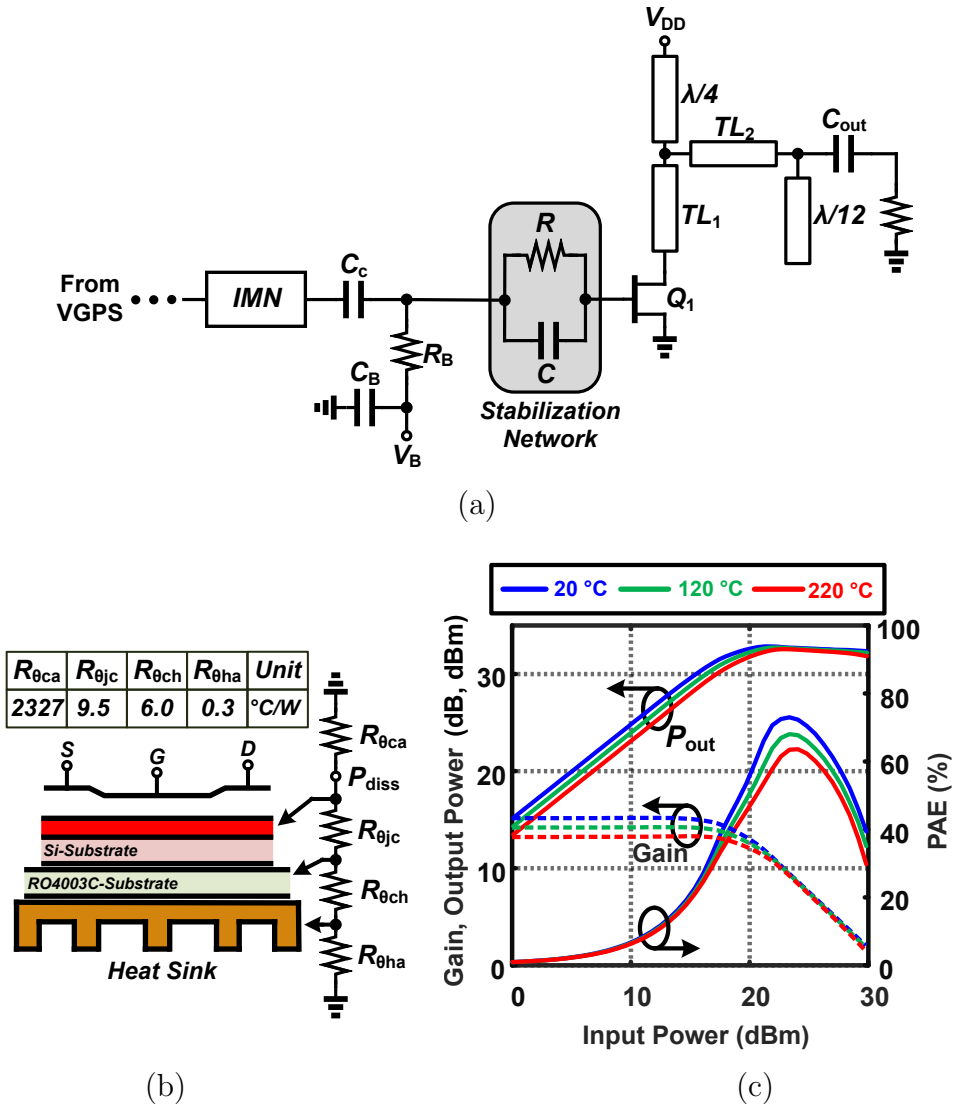


Figure 3.23. Schematic of the inverse class-F, and (b) its simulated output power, large signal gain and PAE.

to introduce a reliable performance and minimize the impact of the temperature on key specifications of the circuit such as gain, output power, and power added efficiency (PAE) [27, 29, 31, 63–65]. Although they offer reliable performance with temperature, they do not provide high PAE at temperatures above 200 $°C$. This is important since the PAs with low PAE must dissipate higher dc power to generate the same level of output power compared to the PAs with high PAE that results further performance degradation due to self-heating

effect [66]. Moreover, the demand for high energy efficient transceivers necessitates PAs with high PAE, since they have major contribution in total power dissipation of the system, that limits their applications in advanced communication systems. Thus, it is required to exploit a high efficiency structure to the PA design. Among several high efficiency PAs introduced previously, class-F PA offers a proper compromise between PAE, output power and linearity [67]. Further, due to presence of a relatively large parasitic capacitance at the drain of the transistor, the design of the termination network of class-F^{-1} is more practical than class-F PA [68].

The superior performance of class-F^{-1} is achieved at the cost of more sensitive input/output matching condition. Figure 3.22 (a) and (b) shows the schematic of the load-pull (LP) setup and stability factor ($\mu - factor$), respectively. The parallel RC network is utilized to unconditionally stabilize the transistor at the target frequency range. It can be seen in Figure 3.22 (b) that the transistor has a stable transfer function at three first harmonics (i.e. 2, 4 and 6 GHz). It should be noted that the stability at first two harmonics is more crucial since the termination impedance at third harmonic is negligible and hence, the voltage amplitude. Further, the increase in temperature results in a reduction in stability due to the change in the gate to drain impedance [62]. The output power and PAE contours are shown in Figure 3.22 (c). The optimum PAE and output power deviates from their initial values when temperature is elevated. This can be attributed to the change in the channel resistance and parasitics at the drain and gate of the transistor [62].

Figure 3.23 (a) shows the schematic of the PA. The microstrip transmission line TL_1 at the drain of the transistor is used to absorb the equivalent shunt capacitance [68]. The $\lambda/4$ and $\lambda/12$ TLs provide open and short impedances at the drain of the transistor, respectively. Further, the total length of the TL_1, TL_2 and $\lambda/12$ is set to be $\lambda/6$, to create a large impedance at second harmonic at drain of the transistor. Figure 3.23 (b) shows the

variation in the output power, gain and PAE of the PA with temperature. Similar to the components used in VGPS circuit design, a TC of 500 $ppm/^{\circ}C$ is assumed for the capacitors and resistors. Moreover, the transmission lines are simulated on RO4003C substrate and its thermal properties are considered in the temperature dependent electromagnetic (EM) simulations.

Since the excess dc power dissipation in the transistor increases junction temperature, the maximum output power of the PA, as the bottleneck of the chain, must be determined to guarantee a reliable performance of the PA over time. As we will discuss later in Section 3.3.6, we assume a maximum junction temperature of 300 $^{\circ}C$ for a reliable lifetime of the transistor. Hence, the maximum output power of PA can be determined using the following equation [69]

$$P_{out,max} = \frac{T_j - T_A}{R_{\theta ca}||(R_{\theta jc} + R_{\theta ch} + R_{\theta ha})} \tag{3.19}$$

where T_j and T_A are the junction and ambient temperature, respectively. $R_{\theta ca}$, $R_{\theta jc}$, $R_{\theta ch}$, and $R_{\theta ha}$ are thermal resistivity of case to air, junction to the case of transistor, case to heat sink, and heat sink to air, respectively, as shown in Figure 3.23 (b). Assuming the maximum junction temperature of 300 $^{\circ}C$, $P_{out,max}$ obtained to be 4.8 W at ambient temperature of 220 $^{\circ}C$. Therefore, the drain bias voltage is reduced to 20 V from standard bias voltage of 28 V, to keep the dissipated power in the transistor junction below 4.8 W. Figure 3.23 (c) shows the simulated output power (P_{out}), gain and PAE of the PA. The maximum output power is approximately 33 dBm while the maximum gain is 15 dB. The output power and gain have about 2 dB of reduction when temperature increases from room temperature up to 220 $^{\circ}C$.

The increase in the rate of carrier trapping in GaN HEMT with temperature results a

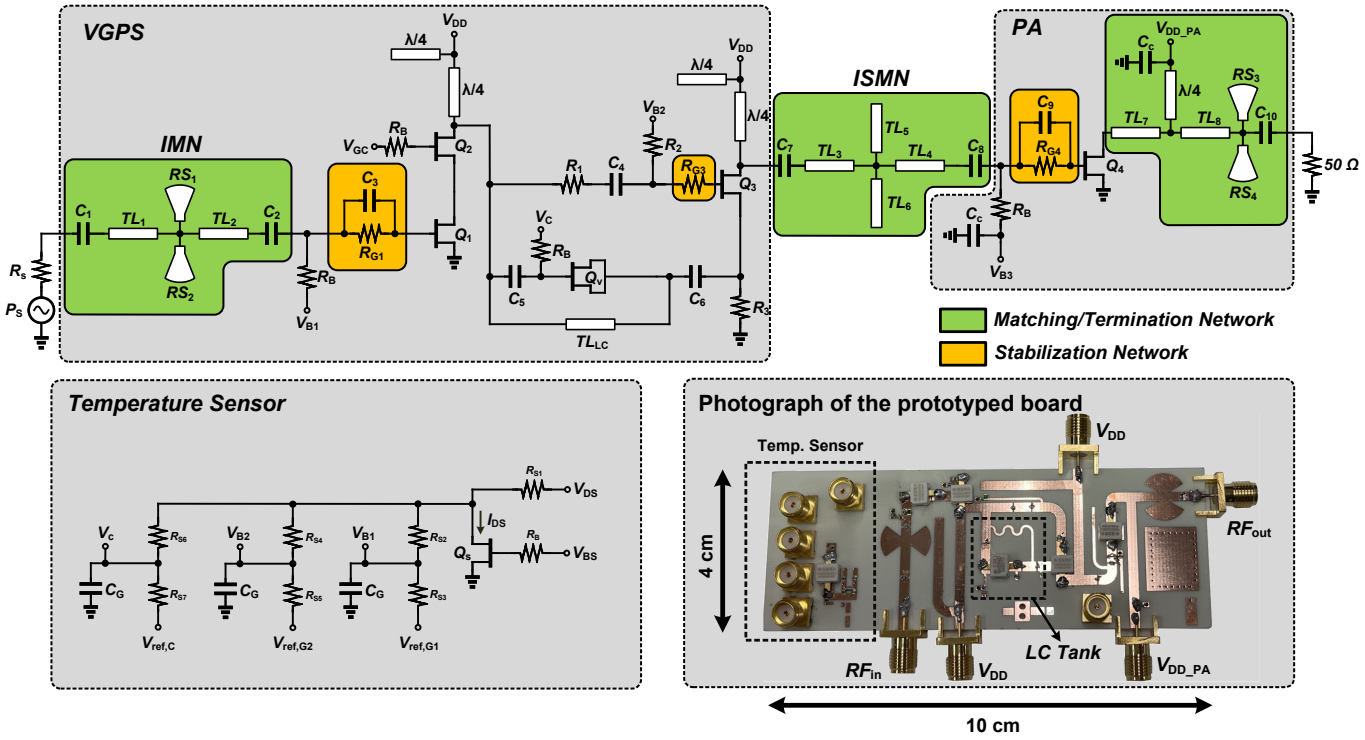


Figure 3.24. Complete schematic of the transmitter, and photograph of its prototype.

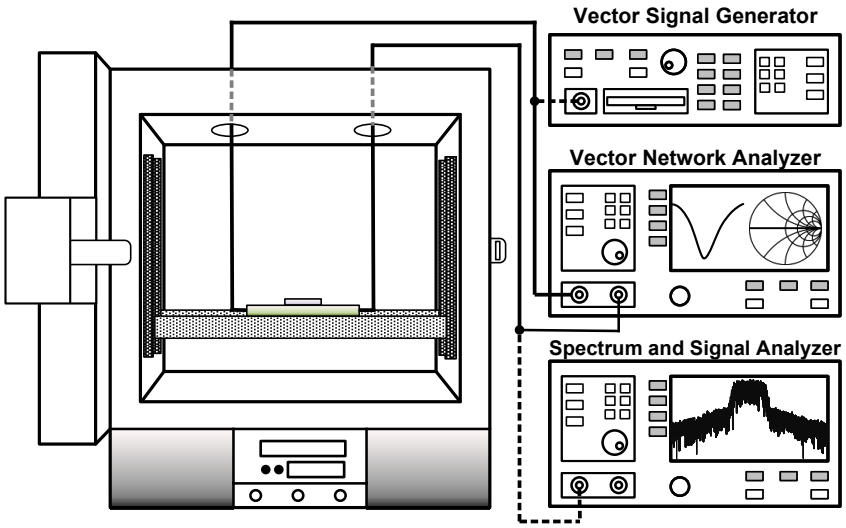


Figure 3.25. Measurement Setup. Dashed lines are the connections for large signal, EVM and ACPR measurements. The solid lines are connected for measuring the small-signal characteristics.

reduction in the number of electrons available in the conduction 2-DEG layer [7]. Thus, a slight bend appears in the drain current at high temperature and the knee voltage drafts to higher V_{GS} voltages, which is also known as "*knee walkout*".Therefore, the reduction in the PAE can be justified using the following equation for class-F^{-1} PA [67].

$$\eta_{D,max} \propto \left(1 - \frac{V_{knee}}{V_{DC}}\right) \tag{3.20}$$

where, $\eta_{D,max}$ is the maximum drain efficiency, V_{knee} is the knee voltage and V_{DC} is the supply voltage. From (3.20), it can be concluded that the *knee walkout* effects along with the shift in the optimum output impedance at maximum PAE, as it is shown in Figure 3.22, result in lower PAE at high temperature. In order to minimize the variation in the characteristics of the PA, one strategy could be employing an adaptive gate bias, similar to that in the VGPS circuit. However, it could cause the transistor bias to deviate from its optimum operational condition. Moreover, by increasing the gate bias voltage with temperature to compensate the output power requires dissipating higher dc power and further reduction in the PAE and producing additional heat at the transistor junction. Thus, compensating the gain reduction of the PA through VGPS stage is a better approach that does not exhibit the drawbacks of adaptive gate biasing.

The PA temperature compensation can be performed by adjusting the increasing factor of the gate-source voltage of Q_1 (α_1). Simulation results showed that $\approx 20\%$ of increase in α_1 results the minimum variation in gain and output power of the PA.

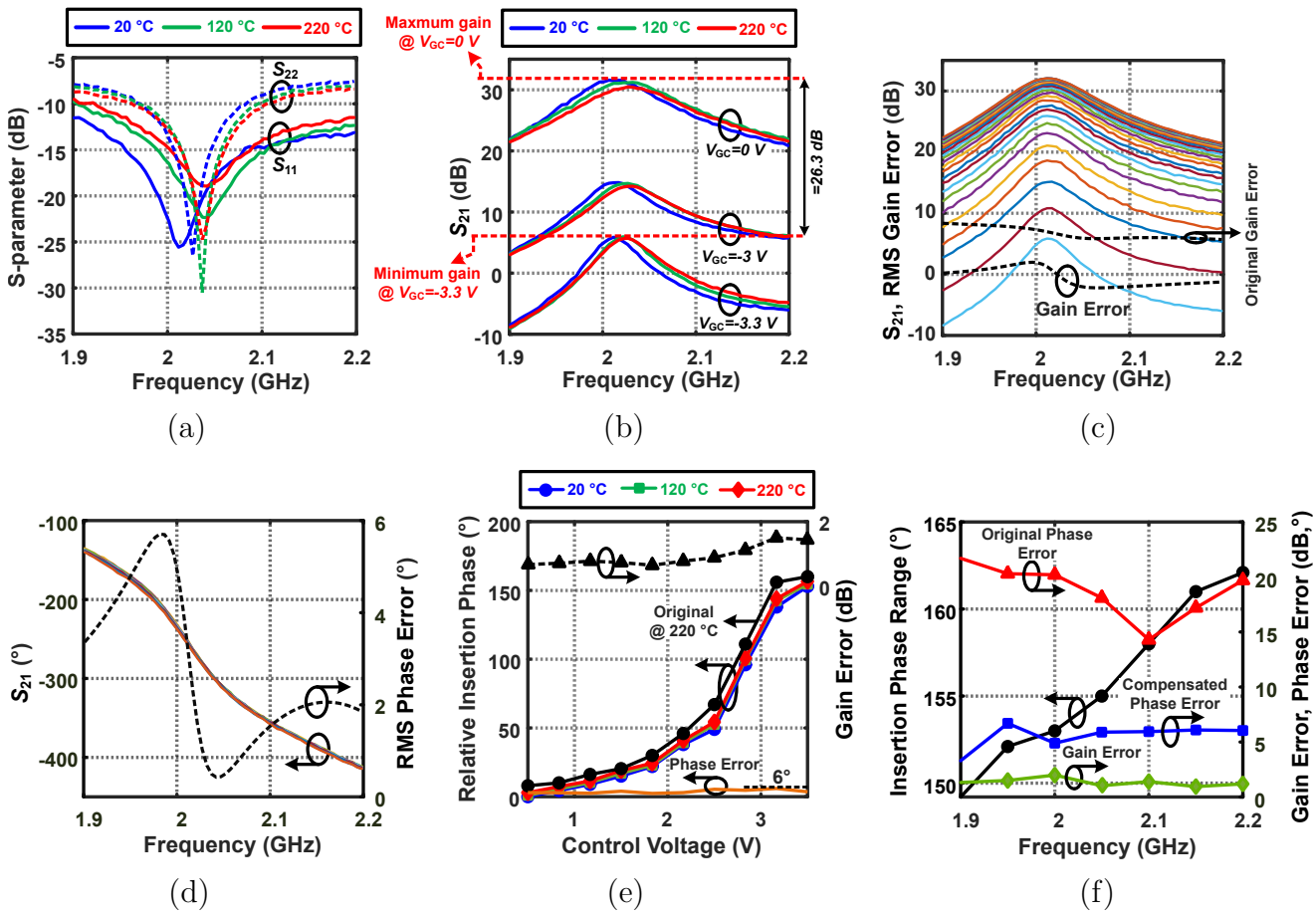


Figure 3.26. Measured (a)-(b) S-parameters of the transmitter, (c) gain stages of the VGPS and corresponding RMS error with temperature for the compensated and uncompensated circuits. (d) the phase of S_{21} and its RMS error with temperature. The measured relative insertion phase versus (e) control voltage, and (f) frequency and their corresponding gain and phase error with temperature.

3.3.6 Experimental Results

Figure 3.24 shows the complete schematic of the transmitter. The drain bias and matching networks are implemented using capacitors and transmission lines. Due to unavailability of high temperature inductor, the parallel inductor of LC tank is also implemented utilizing a transmission line. The stabilizing network for two gain transistors of $Q_{1,3}$ is also implemented to unconditionally stabilize the transistors at the cost of lower gain. Moreover, the stability of inner nodes of the transmitter are investigated through transient simulations to identify

any possibility of parametric oscillation [70].

The adaptive bias voltage of $Q_{1,3}$ and Q_v are provided through temperature sensor block. The resistive voltage dividers shift the drain voltage of Q_s and deliver it to the gate of the transistors. The sensor block consumes an average dc power of ≈13.5 mW across the temperature range from the supply voltage of $V_{DS} = 5V$.

A proof of concept is prototyped on a piece of Rogers 4003C hydrocarbon ceramic laminate as the substrate with a low thermal conductivity of 0.71 $W/m/^{\circ}K$ [71]. The photograph of prototyped board is shown in Figure 3.24. The high transition temperature of the substrate enables the circuit to operate at ambient temperatures up to 280 $^{\circ}C$ with small 3D Coefficient of Thermal Expansion. Cree CGH40006P discrete GaN on SiC HEMT transistor is adopted to implement the transistors and can deliver maximum RF power of 6 W at center frequency of 2.05 GHz. The bias traces from the sensor are drawn at the bottom layer of the board to avert the trace crossing at the top layer of the board and minimize its size. A compact Wakefield-Vette 423K heat sink is attached on the back of the board under the power transistor (Q_4) to increase the series thermal conductivity, as discussed in Section 3.3.5.

In order to measure the performance of the manufactured circuit, it is placed in a natural convection oven (Yamato DX302C) as a temperature-controlled environment, as shown in Figure 3.25. For every change in the circuit parameters, 10-15 minutes were allocated to allow the board to gain the same temperature as the ambient. The instruments are also calibrated before each measurement to eliminate the change in the loss of the cables and connectors due to temperature.

The measured input and output S-parameters at different temperatures are shown in Figure 3.26 (a). Although increasing temperature causes a change in the matching condition, S_{11} remains below -10 dB across the target frequency range from 2 to 2.1 GHz at maximum

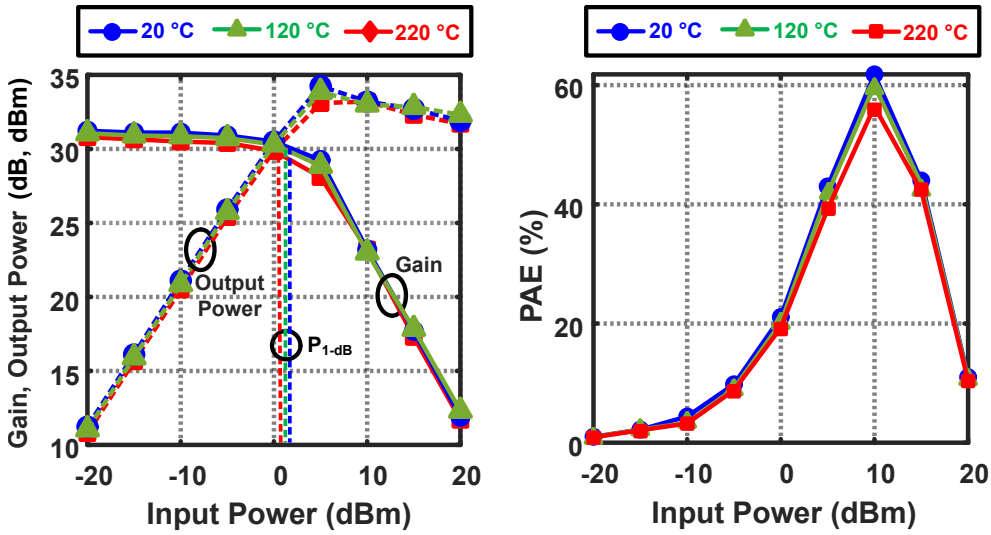


Figure 3.27. (a) measured output power and large signal gain, and (b) PAE of the PA at three different ambient temperatures.

temperature of 220 °C while S_{22} is below -9 dB. The change in the input matching condition of the transmitter due to the variations in the characteristics of the lumped components, substrate and mostly the transistor parasitics, affects the voltage gain (S_{21}) and shifts its peak by increasing the temperature. Figure 3.26 (b) shows S_{21} at three gain levels. It can be seen that for each individual gain level, the difference in the peak gain increases (to maximum of $\approx 1.5\ dB$) as the gain increases. This is mainly due to two reasons; first, the difference in the increasing ratio of the transconductance and decreasing ratio of the output impedance of the first stage of the VGPS with temperature at different gain levels could cause a change in the small-signal gain deviation with temperature, as it was discussed in Section 3.3.4. Second, since no external cooling mechanism (e.g. heat sink) has been exploited to the VGPS design, the self-heating effect can slightly reduce the transconductance of the main transistors ($Q_{1,3}$) at high gain levels where more dc power is dissipated in the transistors [66]. Further, the variable gain stage ($Q_{1,2}$) is able to provide a continues gain range of $\approx$26 dB for the applied gain control voltage (V_{GC}) ranging from -3.3 V to 0 V.

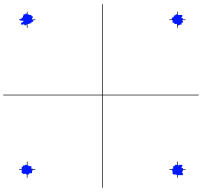
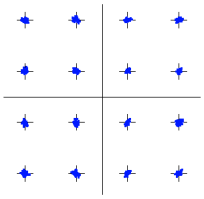
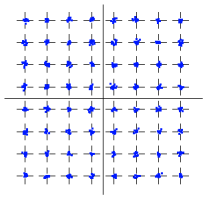
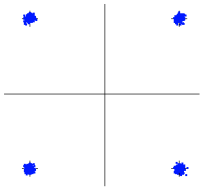
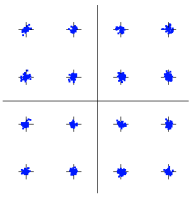
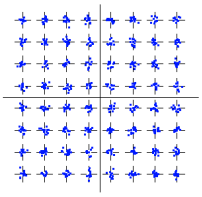
	Modulation	QPSK	16-QAM	64-QAM
At 20 °C	Constellation			
	Data Rate	40 Mbps	80 Mbps	120 Mbps
	EVM	3.2 %	3.2 %	3.4 %
	ACPR	-34 dB	-36 dB	-34 dB
At 220 °C	Constellation			
	Data Rate	40 Mbps	80 Mbps	120 Mbps
	EVM	3.8 %	3.7 %	3.9 %
	ACPR	-33 dB	-34 dB	-33 dB

Figure 3.28. Measured constellation, EVM and ACPR of the transmitter for three modulation schemes at $f_c = 2.03\ GHz$ and input power of 0 dBm and the gain level of 30 dB.

The S_{21} at room temperature versus frequency is measured by sweeping V_{GC} as shown in Figure 3.26 (c). The maximum gain of 31.5 dB and minimum gain of 5.2 dB is achieved at $V_{GC} = 0\ V$ and $V_{GC} = -3.3\ V$, respectively. The RMS gain error for the compensated transmitter and the original one without compensation circuit is also shown in the figure. It can be seen that the gain variation is reduced by atleast 4 dB. It is worth noting that by re-tuning the input matching network, the improvement can increase up to 6 dB.

As we discussed in Section 3.3.4, the design equations (3.11) and (3.12) suggest that the insertion phase remains constant at each specific ambient temperature, when the voltage gain is changing through V_{GC}. However, the non-idealities of the varactor and voltage dependent capacitances of the active devices could cause a change in the insertion phase of the circuit. Figure 3.26 (d) shows $\angle S_{21}$ and its corresponding RMS phase error. The phase error is below 6.5° across the desired frequency range of 2-2.1 GHz.

Figure 3.26 (e) shows the phase tuning curves at different temperatures for compensated and original circuits at carrier frequency of 2.02 GHz. As it is shown in the figure, the insertion phase of the compensated circuit has a maximum variation of 6° across the control voltage range while the total voltage gain change is below 2 dB. A part of this gain variation is due to the aforementioned reasons related to Figure 3.26 (b) and is independent from the variations in the varactor impedance. To gain more insight into the temperature dependent variations of the transmitter gain and insertion phase with control voltage, the experiment in Figure 3.26 (e) was repeated at different operation frequencies and 4 gain levels. The insertion phase range and gain and phase errors are plotted in Figure 3.26 (f). The first observation is that the insertion phase range increases by frequency. This is not an unexpected result since the equivalent capacitance of the varactor is frequency dependent that causes this change in the insertion phase, as (3.15) and (3.16) indicate. However, the minimum phase range is more that 150° inside the target frequency range. It should be noted that greater phase range is achievable using a varactor with smaller fixed capacitance (e.g. bare die transistor). Furthermore, the amount of improvement in the RMS phase variation with temperature and control voltage is represented in the figure. The compensated circuit has an average of ≈65% less variation in the insertion phase compared to the original circuit. Finally, the RMS gain error remains below 2.3 dB across the frequency, temperature and gain control voltage.

The large signal characteristics of the transmitter is also measured and shown in Figure 3.27. It can be seen that the large-signal gain shows a small change (<1.5 dB) across the temperature range. However, the amount of excess dissipated dc power causes a reduction in the PAE, as it is shown in Figure 3.27 (b). Although the variation in the large-signal characteristics of the transmitter is small, it still can affect the quality of the communication. Figure 3.28 shows the measured output constellation, error vector magnitude (EVM) and adjacent channel power ratio (ACPR) for QPSK, 16- and 64-QAM input signals. It can be noticed that the EVM and linearity performance are slightly degraded with temperature.

Table 3.2: Performance Summary and Comparison With Relevant building blocks

	This Work			Temp. Compensated VGA			Varactor based PS		Temp. Compensated PA	
	TX	VGPS*	PA*	JSSC'12 [32]	ISCAS'17 [59]	TCAS-I'19 [61]	MWCL'06[#] [51]	TMTT'18 [53]	MWCL'15 [33]	HiTEN'17 [27]
Process Technology	GaN HEMT			130-nm SiGe BiCMOS	GaN HEMT	55-nm CMOS	Bipolar with BST Varactor	GaN HEMT	GaN HEMT	GaN HEMT
Frequency (MHz)	2000~2100			0.2~7500	97.5	10~740	200~1100	3000~7000	2000	200~300
Temp. Range (°C)	20~220			-20~200	25~230	-20~80	N/A[§]	N/A	27~150	25~230
Gain (dB)	5.2~31.5	-8.1~18.2	13.3	-10~30	-2.5~27	-31~14	2	-1	24	13
Max. Gain Error (dB)	2.3 RMS	2.1 RMS	0.2 RMS[‡]	5	3	4	0.6[†]	1.6[†]	2.1	5
Phase Range (°)	155	155	N/A	N/A	N/A	N/A	100	180	N/A	N/A
Output Power (dBm)	33	N/A	33	N/A	N/A	N/A	N/A	N/A	35.6	32.2
PAE (%)[¶]	58	N/A	58	N/A	N/A	N/A	N/A	N/A	62.4	25

* estimated by comparing simulation and measurement results
[§] indicates not available
[#] results at 1 GHz
[†] excluding temperature effect
[‡] after compensation
[¶] at maximum operating temperature

This can be attributed to the shift in the bias voltage of the VGPS transistors toward non-linear region when the temperature sensor is adjusting the dc bias of the active transistors. Further, as it was explained earlier in Section 3.3.5, the VGPS delivers larger power at higher temperatures to compensate the PA's gain drop with temperature which can push the PA into the non-linear region at high output power. Even though the EVM performance of the transmitter is slightly degraded with temperature, its performance is satisfactory and is able to transmit 64-QAM signals with a data rate of 120 Mbps.

Table 4.1 summarizes the performance of the transmitter. A fair comparison with other related works is difficult due to differences such as different process technologies, target temperature range, frequency range. Having said this, the performance of the individual building blocks of the transmitter are estimated by comparing the measurement and simulation results to be comparable with previously published standalone blocks. The maximum operating temperature of the proposed circuit is higher than the other temperature compensated circuits except the VGA in [59]. The proposed transmitter also offers minimum gain variation across the temperature range between the temperature compensated building blocks in the table. Furthermore, the output power of the PA in [33] is higher than the proposed one at the cost of considerably lower maximum operating temperature.

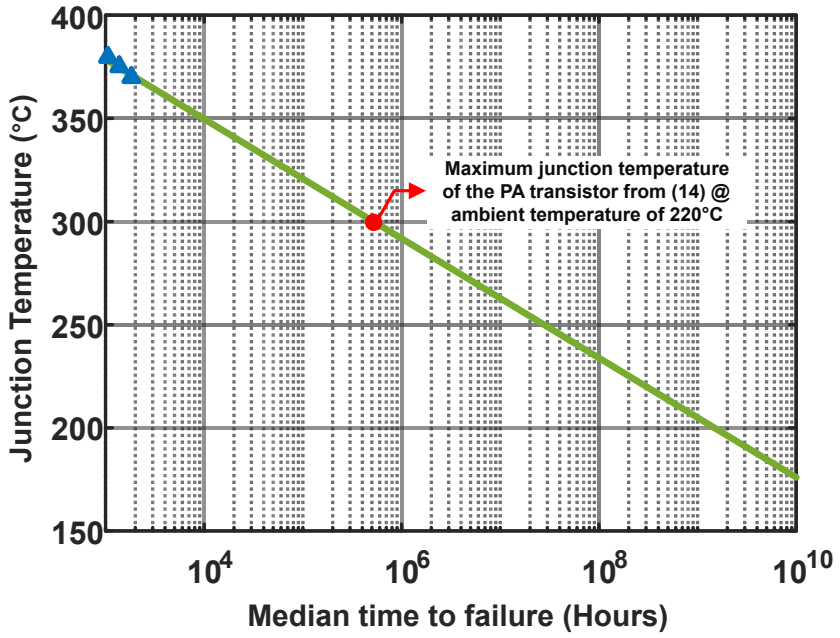


Figure 3.29. Measured (triangles) and its extrapolation lifetime of the GaN HEMT [4, 5].

In order to estimate the functional lifetime of the circuit, the reliability of individual components must be investigated. According to the characteristics of the high temperature PCB materials used in this work, its proper functionality can be excepted over the entire operation time of the circuit [71]. The reliability of the lumped components, however, depends on the availability of the high temperature COTS components and their failure time might become the bottleneck of the reliable lifetime of the transmitter. Figure 3.29 shows the median time to failure of the GaN HEMT against its junction temperature. As it is shown in the figure, by setting the maximum junction temperature of 300°, the transistor can have a reliable performance over its entire lifetime. This suggests that one might utilize GaN HEMTs as fixed capacitors and resistors to guarantee a sufficient lifetime for the transmitter. However, as the transistors are non-linear components, it can cause a degradation in the performance of the circuit. Moreover, additional compensation circuit would be required to compensate the variations of their characteristics, that further adds to the design complexity.

3.4 Conclusion

In this chapter, we introduced the design of the building blocks of a temperature compensated phased-array transmitter. A temperature sensor is designed to establish transconductance zero temperature coefficient for the active GaN HEMTs. Further, impact of the temperature elevation on the characteristics of individual building blocks, including variable gain phase shifter and power amplifier, and the transmitter chain was investigated. The designed transmitter was prototyped on a peace of Rogers substrate as a proof of concept. The measurement results were carried out that showed the reliability of the transmitter at high temperature. The specifications of the transmitter was also measure for different modulation schemes and their variation with temperature were investigated.

Chapter 4

Design and Analysis of an Ultra-Low Phase Noise Dual Tank Oscillator

4.1 Introduction

The increasing demand for utilizing spectrum efficient modulation schemes in new generation of communication necessitates high-purity oscillators. However, the traditional oscillator architectures with second order LC resonators mostly fail to meet the requirements of some of the advanced communication standards due to the limited minimum attainable phase noise levels. This can be further investigated using the phase noise expression at offset frequency of $\Delta\omega$ [72],

$$\mathcal{L}(\Delta\omega) = 10 \cdot \log\left(\frac{k_B T R_p}{Q^2 V_{osc}^2} \cdot F \cdot \left(\frac{\omega_0}{\Delta\omega}\right)^2\right) \tag{4.1}$$

where k_B is Boltzmann's constant, T is the absolute temperature, F is the phase noise

factor of the active devices, and ω_0 is the oscillation frequency. According to (4.1), the oscillation amplitude (V_{osc}) needs to be maximized to reduce the phase noise level. However, the maximum V_{osc} is limited by the supply voltage and breakdown voltage of the active devices. The technology constraints in advanced fabrication processes also limits the quality factor of the inductors and hence the tank (Q). The equivalent parallel resistance of the tank (R_p) in (4.1) is another key parameter that has a significant impact on the phase noise performance of the oscillator. A proper strategy for lowering the effective noise of the tank loss is decreasing its R_p by reducing the size of the inductor(s). However, due to the technology constraints, excessive reduction in the inductor size degrades the quality factor of the individual inductors. This is illustrated in Figure 4.1. It can be seen that continuous reduction in the inductance value results in a drastic decrease in quality factor when the loss of the vias and routing parasitics become dominant. The reduction in Q results in a considerable degrade in Figure-of-Merit (FoM) of the oscillator [73]

$$FoM = 10 \cdot \log \left(\frac{Q^2 \eta}{\sum F} \cdot \frac{2 \times 10^{-3}}{K_B T} \right) \tag{4.2}$$

where η is the power efficiency of the oscillator (i.e. P_{RF}/P_{DC}). Therefore, the designers have been motivated to introduce alternative approaches to reduce R_p.

Ahmadi-Mehr et al. proposed a dual core class-C oscillator targeted on decreasing R_p of the tank [74]. Instead of reducing the inductor size, two oscillators are connected in parallel. This reduces R_p by half with equal voltage swing across the tank compared to a single core oscillator. The extra core adds considerably to the die area and double the dc power dissipation.

Babaie et al. introduced a doubly tuned class-F_2 tank composed of two 1:2 transformers [75]. The tank scales down the equivalent resistance seen by the core transistors which is

proportional to the primary/secondary ratio of the transformer. However, the interwoven configuration of the multi turn transformers suffers from a low quality factor of the multi-turn primary/secondary winding. This can be attributed to the relatively large spacing between primary and secondary traces and under-passing trace(s) in primary/secondary winding, as it is shown in Figure 4.2. It can be seen in Figure 4.2 (a) that the quality factor drops by increasing the gap between turns. This is an inevitable degradation in the quality factor since the large spacing is required to implement the primary winding. Further, to avoid crossing between primary and secondary, the traces must pass to lower layers at cross section(s). This results in a drastic decrease in the quality factor of individual windings and hence, the transformer. Figure 4.2 (b) represents the simulated decrease in the quality factor of a single turn inductor. It can be seen that passing the traces from top metal layer (i.e. M_6) to a lower layer (e.g. M_5 or M_4) causes a decreases in the quality factor. The reduction becomes significant by reducing the size of the inductor which makes it a design challenge since a small size inductor with low series resistance is desired for low phase noise oscillator design, as discussed earlier.

In another effort, Lim et al. proposed a transformer based resonator with complementary core transistors [76] that is able to scale down R_p while providing two resonance frequencies at f_0 and $2f_0$. The concentric transformer is optimized to have a low coupling factor between primary and secondary windings to maximize the quality factor of the tank at two resonance frequencies. However, this results in a reduced overall quality factor of the transformer as their introduced transformer configuration has a relatively lower quality factor compared to a 1:1 high coupling factor transformer [77]. Resultantly, the phase noise improvement is limited since the phase noise is a strong function of the quality factor of the resonator at both harmonics [78].

Recently, El-Aassar et al. introduced a stacked-complementary structure that utilizes two

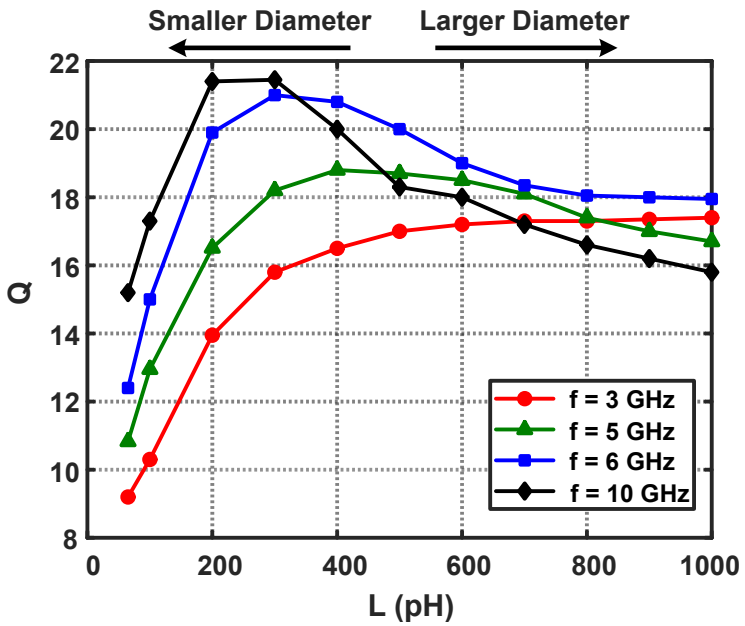


Figure 4.1. The impact of scaling down the inductor on its quality factor.

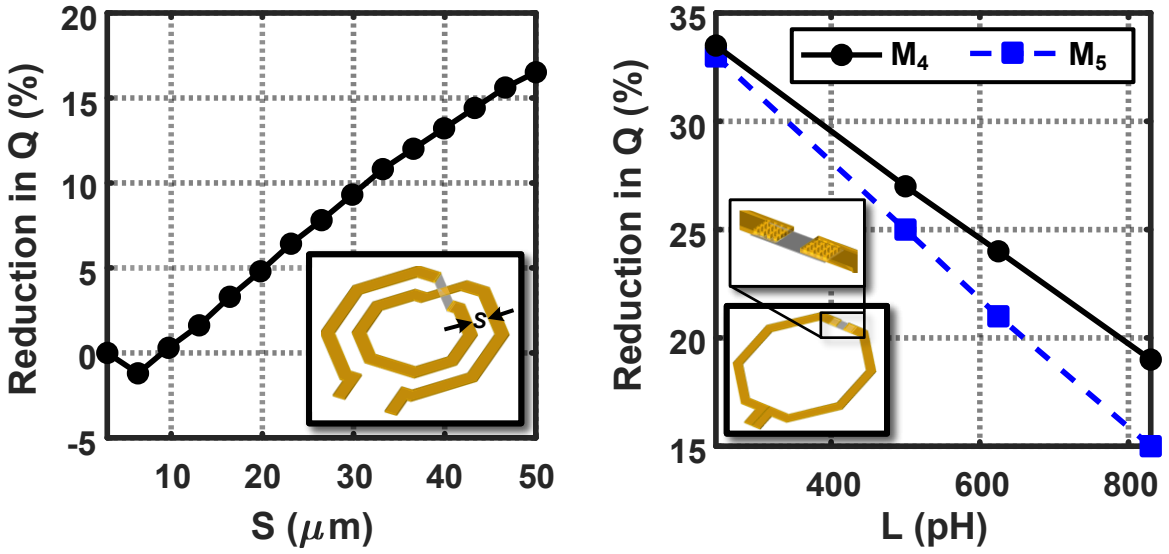


Figure 4.2. The simulated impact of (a) line spacing, and (b) under-passing interconnection on the quality factor for an inductor with the line width of 15 μm.

single-turn 1:1 transformer to achieve high quality factor at f_0 and $2f_0$ While scaling down R_p [79]. The spacing between the resonators was increased to reduce their magnetic coupling

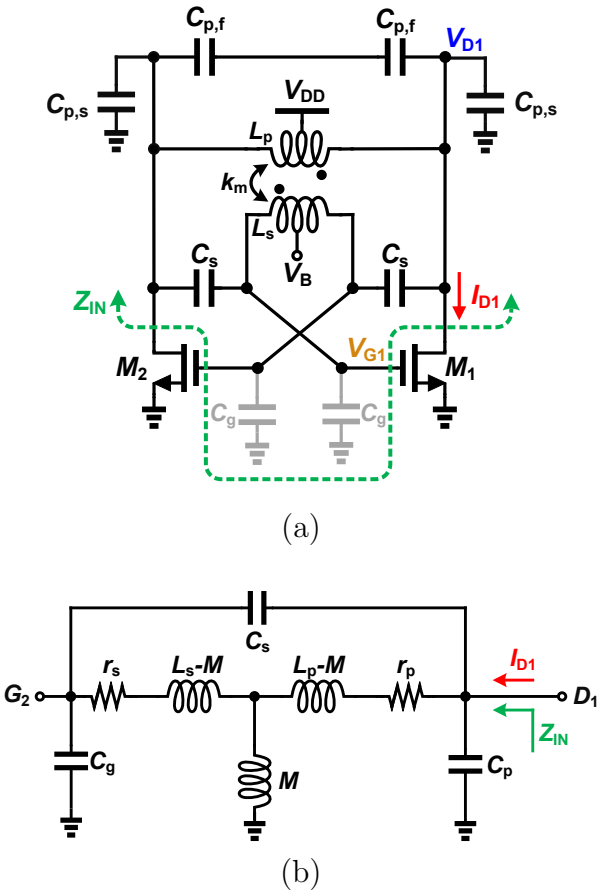


Figure 4.3. (a) the preliminary schematic of the dual tank oscillator, and (b) equivalent circuit of the its tank.

at the cost of a larger die area. A broadside single-turn configuration is utilized to layout the main transformer that increases the effective surface area and maximizes the coupling factor. However, achieving high quality factor at primary and secondary demands two thick metal layers to implement the transformer, which is not accessible through typical CMOS technologies.

$$\omega_{1,2}^2 = \omega_s^2 \cdot \left. \frac{(X+Y)+2(1-k_m)+\sqrt{(X^2+Y^2)-4k_m(X+Y)(1-k_m)+2XY(2k_m^2-1)+4(1-k_m)^2}}{2(X+Y+XY)(1-k_m^2)} \right|_{X_{1,2}} \tag{4.3}$$

To address the aforementioned issues and break the limit on the minimum achievable R_p, we propose a new doubly-tuned oscillator structure. The proposed tank is able to provide an effective R_p of the tank, several times smaller than R_p of each individual inductor without sacrificing the quality factor, size or FoM of the oscillator. This allows us to choose the inductors values at their peak quality factor, while the effective R_p can be considerably scaled down to obtain an ultra low phase noise with a high FoM. Moreover, the harmonics at the drain of the core transistors are managed to locate at f_0 and $2f_0$ to minimize the effective impulse sensitivity function (ISF) of the transistors while their generated noise is considerable and resultantly, the overall phase noise improves.

This paper is organized as follows. Section 4.2 describes an analysis on the proposed dual tank oscillator. Section 4.3 investigates the phase noise performance of the oscillator. The measurement results are discussed in Section 4.4. Finally, Section 4.5 concludes this work.

4.2 Dual Tank Operation

Figure 4.3 (a) shows the schematic of the proposed oscillator. The 1:1 transformer is composed of the parallel (L_p) and series (L_s) inductors while they provide the bias path for the transistors $M_{1,2}$. The equivalent circuit of the oscillator tank is shown in Figure 4.3 (b). C_g is the parasitic capacitance at the gate of the core transistors and C_p ($= C_{p,s} + C_{p,f}$) represents the equivalent capacitance at the drain of $M_{1,2}$. The coupled transformer is also modeled with its equivalent T-network, where the magnetic coupling is $M = -k_m\sqrt{L_pL_s}$. The input impedance of the tank Z_{in}, can be expressed by a fourth order impedance characteristic, with two resonance frequencies. However, it can be shown that the phase condition for satisfying the oscillation criteria is not fulfilled at lower resonance frequency. Assuming equal primary and secondary inductors (i.e. $L_p = L_s$), the resonance frequencies of the tank at ω_1 can be

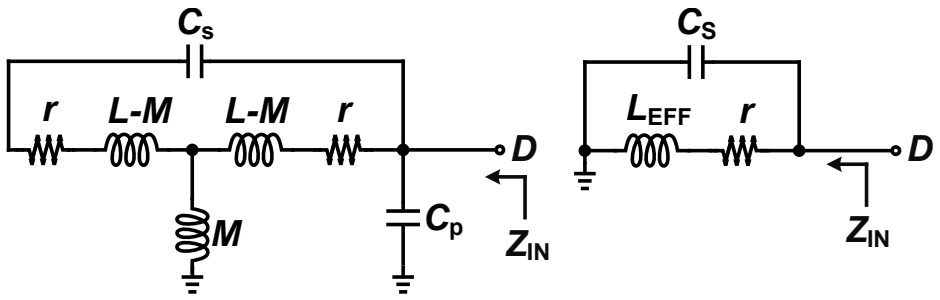


Figure 4.4. Second order equivalent of the proposed tank.

calculated as (4.3) with

$$\omega_s = 1/\sqrt{L_s C_s} \tag{4.4a}$$

$$X_1 = (C_{p,s} + C_{p,f})/C_s \tag{4.4b}$$

$$Y = C_g/C_s \tag{4.4c}$$

For the sake of simplicity, we will further make the following assumptions: i) the inductance and quality factor of the primary and secondary windings of the transformer are equal (i.e. $L = L_p = L_s$ and $Q = Q_p = Q_s$) unless it is noted otherwise; ii) the parasitic capacitance at the gate of $M_{1,2}$ is sufficiently smaller than the equivalent single-ended capacitance at the drain of $M_{1,2}$ (i.e. $Y \ll X_2$). It should be noted that the latter assumption remains valid for the proposed oscillator.

4.2.1 Impedance Scaling Mechanism of the Proposed Tank

To gain insight into the impedance scaling mechanism of the proposed tank, lets suppose we want to recreate the characteristics of the proposed tank at ω_1 using a second-order parallel LC tank. Figure 4.4 shows the DM equivalent circuit of a second order tank and the proposed

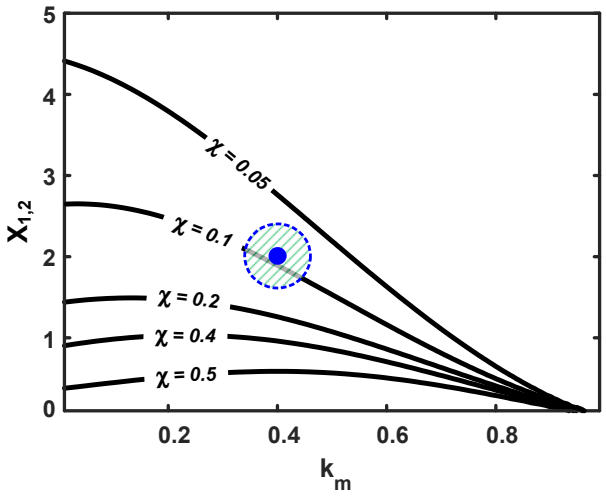


Figure 4.5. Impedance scaling factor χ, calculated using (4.5).

one.

To have a fair comparison between two tanks, three main characteristics of the second order tank including quality factor of the resonator, resonance frequency, and equivalent parallel resistance must match the corresponding characteristics of the proposed tank. Furthermore, we assume that the inductances of the proposed tank are identical ($L = L_s = L_p$ and $r = r_s = r_p$). This results in unique component values of the LC tank. Finally, the ratio of the inductance of the second order tank (L_{EFF}) to the inductance of the proposed tank can be obtained as

$$\frac{L_{EFF}}{L} = \chi(X_1, k_m) = \frac{1}{2\left(\frac{\omega_1}{\omega_s}\right)^2} \cdot \frac{\left(\frac{\omega_1}{\omega_s}\right)^2 (1 - k_m^2) - 1}{\left(\frac{\omega_1}{\omega_s}\right)^2 X - \left(1 + \frac{X_1}{2}\right)} \tag{4.5}$$

where (ω_1/ω_s) can be determined using (4.3), as a function of X_1 and k_m. Figure 4.5 plots the scaling factor contours, χ with respect to X_1 and k_m. As it is obvious from the figure, effective inductance of the tank (L_{EFF}) can be scaled down by increasing X_1. This is an

interesting result since the size of the inductors can be arbitrarily chosen to obtain the maximum quality factor [see Figure 4.1] while the effective inductance is scaled down to a desired value. The scaling factor can also be investigated from a different perspective by calculating equivalent parallel resistance at oscillation frequency of ω_1 (R_{p1}).

Assuming the inductors are the major source of the loss in the tank (i.e. $Q_L \gg Q_C$), R_{p1} can be calculated as

$$R_{p1} \approx Q \cdot \left[\frac{1}{2\omega_1 C_s} \cdot \frac{\left(\frac{\omega_1}{\omega_s}\right)^2 (1 - k_m^2) - 1}{\left(\frac{\omega_1}{\omega_s}\right)^2 X_1 - \left(1 + \frac{X_1}{2}\right)} \right] \tag{4.6}$$

where $Q = r_p/L_p\omega = r_s/L_s\omega$. By recasting (4.6) we have

$$R_{p1} \approx \chi(X_1, k_m) \cdot r \tag{4.7}$$

Equation (4.7) indicates that R_p of the proposed tank is scaled down by the factor of χ compared to series resistance of the individual indoctors (r_s and r_p). However, the minimum achievable scaling factor is restricted by the power budget and start-up criteria of the oscillator.

The scaling factor χ is desired to be small to scale down R_{p1} targeting minimum achievable phase noise. The impact of X on the effective quality factor of the tank must be studied to guarantee a proper power efficiency for small scaling factors. The quality factor of the tank can be calculated at resonance frequency using the following equation.

$$Q_1 = \frac{\omega_1}{2} \cdot \left| \frac{\partial \angle Z_{in}(j\omega)}{\partial \omega} \right|_{\omega_1} . \tag{4.8}$$

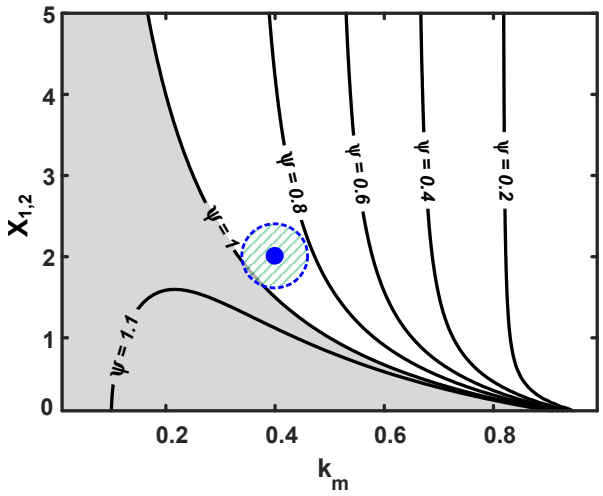


Figure 4.6. Calculated ψ from (4.10).

where Z_{in} is the input impedance of the tank. By carrying out the straightforward math, equivalent quality factor of the tank is calculated to be

$$Q_1 = \psi(X_1, k_m) \cdot Q \tag{4.9}$$

with

$$\psi(X_1, k_m) = \frac{\left(\frac{\omega_1}{\omega_s}\right)^2 (1 - k_m^2) - \left(\frac{1-k_m}{X_1} + \frac{1}{2}\right)}{\left(\frac{\omega_1}{\omega_s}\right)^2 - \left(\frac{1}{X_1} + \frac{1}{2}\right)} \tag{4.10}$$

Figure 4.6 shows ψ contours versus X and k_m. For the tank with a weakly coupled transformer, ψ increases by increasing X up to a certain point at the edge of the shaded area, and then starts to decrease. On the other hand, referring to Figure 4.5, increasing X is desired for lowering R_p. This can pose a design challenge for a tank with relatively large k_m, since excessive increase in X decreases the equivalent quality factor of the tank. This trade-off could be a limiting factor for large coupling factors ($k_m > 0.5$). Therefore, minimizing k_m

(ideally, separate inductors with $k_m = 0$) is preferred when a very small χ (e.g. $\chi < 0.1$) is desired, at the cost of larger die area. Having said this, a ($0 < k_m < 0.5$) is beneficial to the equivalent quality factor for a reasonable scaling factor (e.g. $\chi \geq 0.1$). It should be noted that for a very small coupling factors (i.e. $k_m \approx 0$), ψ converges to $\psi = 1$ and becomes independent from X.

4.2.2 Drain to Gate Passive Gain

The introduced tank also provides a passive gain from the drain of the core transistors to their gate. This brings two important advantages for the oscillator. First, the reduced equivalent parallel resistance of the tank could cause start-up issues since it reduces the loop gain. Therefore, the passive gain can compensate for the decrease of the loop gain. Moreover, the passive gain favors the suppression of the effective noise of the core transistors as it will be discussed in next section. Assuming the input current to the gate of $M_{1,2}$ is negligible, the passive gain at oscillation frequency can be computed as

$$A_{v1}(j\omega) \approx \frac{(1-k_m^2) - \left(\frac{\omega_1}{\omega_s}\right)^2 k_m - j\left(\frac{2}{Q}\right)}{(1-k_m^2) + \left(\frac{\omega_1}{\omega_s}\right)^2 + j\frac{(\frac{\omega_1}{\omega_s})^2 - 2}{Q}} \tag{4.11}$$

Figure 4.7 shows the magnitude of the passive gain in (4.11). It can be noticed that $|A_v|$ increases by increasing X for relatively small coupling factors and becomes independent from X for a highly coupled transformer. Similar to the equivalent quality factor of the tank, a relatively small k_m is beneficial to the passive gain for any specific value of X, as it can be noticed from the figure.

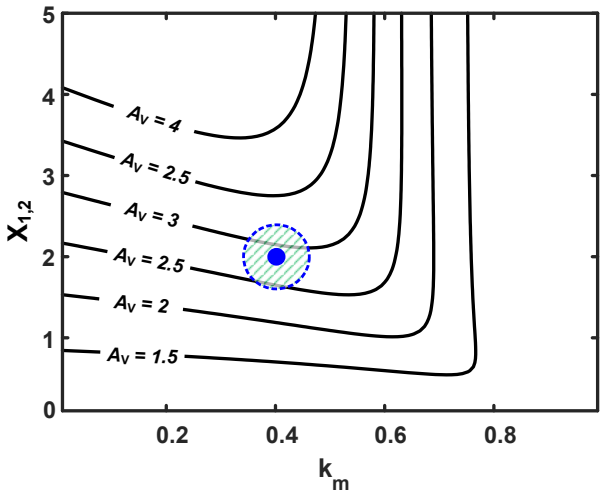


Figure 4.7. Passive gain of the proposed tank for $Q_s = Q_p = 20$, obtained from (4.11).

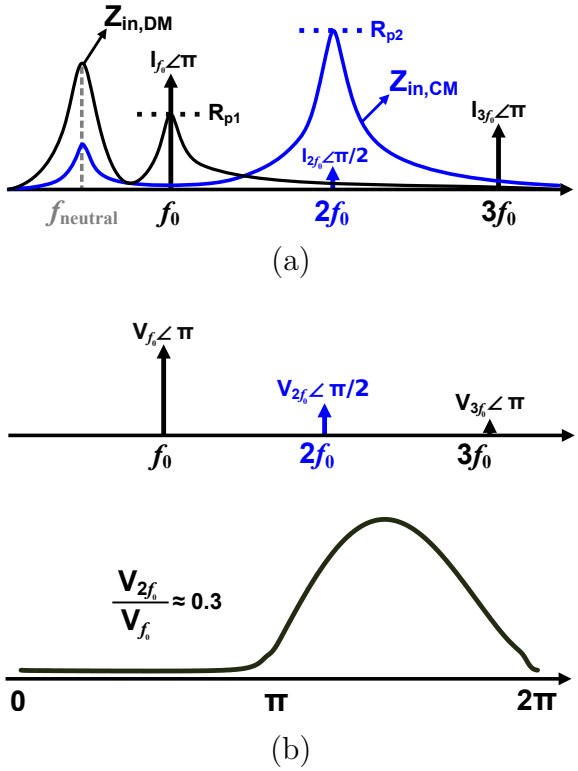


Figure 4.8. (a) Frequency response of the tank, and frequency components of the drain current. (b) frequency components of the drain voltage (top) and its corresponding time domain waveform (bottom).

4.2.3 Dual-Mode Tank

The large voltage amplitude across gate-drain of the core transistors push them partially from saturation into triode over each oscillation cycle. Thus, the drain current contains higher order harmonics in addition to the fundamental, due to non-linear operation of the active devices and their parasitics. However, the first and second harmonics appear with different phases at the drain of the transistors, in which the fundamental harmonic appears mutually out of phase (i.e. Deferential-Mode) while the second harmonic in-phase (i.e. Common-Mode). This enables the oscillator to shape the voltage waveform at the drain of the core transistors if the tank provides sufficient impedance at specific harmonics.

Figure 4.8 (a) shows input impedance of the tank. By tuning the ratio of single-ended to the float capacitances (i.e. $C_{p,f}/C_{p,s}$), DM and CM impedance peaks can be located at f_0 and $2f_0$. Therefore, the fundamental harmonic of the drain current flows into the tank and generates the fundamental harmonic of the voltage (i.e. $V_{f_0} = I_{f_0} R_{p,1}$) while the second harmonic of the current flows into the CM equivalent impedance of the tank and produces the second harmonic component of the drain voltage, as it is shown in Figure 4.8 (b). The higher order harmonics of the drain current however, are filtered out and the voltage spectrum only contains two first harmonics. It should be noted that the phase condition of oscillation criteria is not satisfied at first impedance peak (i.e. $f_{neutral}$ in 4.8 (a)). The flat area in the voltage waveform makes the impulse sensitivity function negligible in the area that the core transistors generate considerable amount of noise. This indicates that the generated noise by the transistors across the flat area of the voltage waveform will not be translated to the phase noise, as it will be discussed in the next section.

Since we are interested in the ratio of the CM to DM resonance frequencies (ω_2/ω_1), it can be calculated using (4.3) with

$$X_2 = C_{p,s}/C_s \tag{4.12}$$

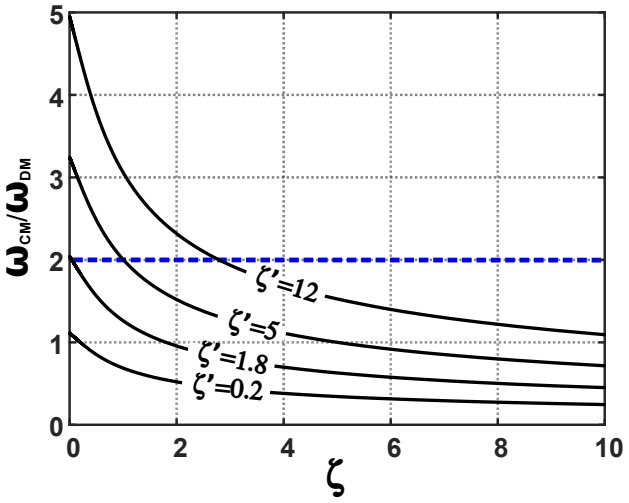


Figure 4.9. The frequency ratio criteria of the tank.

that results

$$\left(\frac{\omega_{CM}}{\omega_{DM}}\right)^2 = \left(\frac{\omega_2}{\omega_1}\right)^2 \approx \frac{1+2\zeta^{'}+\sqrt{1+4\zeta^{'2}}}{1+2\zeta+\sqrt{1+4\zeta^2}} \tag{4.13}$$

where $\zeta = (1-k_m)/X_1$ and $\zeta^{'} = (1-k_m)/X_2$ and assuming the inductors are weakly coupled (i.e. $0 < k_m < 0.5$). Figure 4.9 illustrates the criteria in (4.13) that must be met. This criteria allows the DM and CM impedance peaks to be located at f_0 and $2f_0$ by adjusting $X_{1,2}$ and k_m. It shows that $\zeta^{'}$ must be at least 1.8 or greater to obtain the desired tank characteristic. However, for $\zeta^{'}$ smaller than 1.8, the proposed tank becomes similar to a single resonance frequency tank. It is worth noting that all of the design expressions derived in this section are valid at $2f_0$ (ω_2) and can be used by replacing ω_1 and X_1 with ω_2 and X_2, respectively. This results the same plots as in Figure 4.5-4.7.

As a design example, let's assume that a reasonably small impedance scaling factor $\chi \approx 0.1$ is desired at ω_1 which is specified in a circular area in Figure 4.5. Assuming $k_m \approx 0.4$, X_1 is found to be ≈ 2 from the figure. However, it slightly reduces the equivalent quality factor

of the tank ($< 10\%$), as shown in Figure 4.6. Moreover, the tank provides a passive gain of ≈ 2.8 that favors satisfying the start-up condition and suppressing noise to phase noise translation of the active devices as discussed earlier.

The same logic is applicable at second harmonic (ω_2). However, since X_2 is always smaller than X_1, χ_2 and ψ_2 become larger than χ_1 and ψ_2, respectively. We will further investigate this properties of the tank in Section 4.3. Moreover, A_v is smaller at ω_2 compared to the passive gain at fundamental frequency that makes the voltage at the gate closer to a pure sinusoidal than the drain waveform [see Figure 4.8 (b)]. This helps the core transistors with faster transition and thus, a smaller portion of the generated noise by the transistors will be translated to the phase noise [18, 80].

4.2.4 Implementation of the Transformer

Figure 4.10 shows the layout of the transformer. It is composed of two center-tapped inductors, where the secondary inductor is laid out inside the primary one. The spacing between primary and secondary is chosen to obtain a coupling factor of $k_m < 0.5$ with approximately equal inductances. The direction of the current flow is indicated with arrows for DM and CM excitations. It can be shown that the electric flux due to the induced current in primary and secondary add constructively for both DM and CM excitations. Thus, no flux cancellation mechanism presents in the proposed configuration and the quality factor of the inductors will be preserved [81].

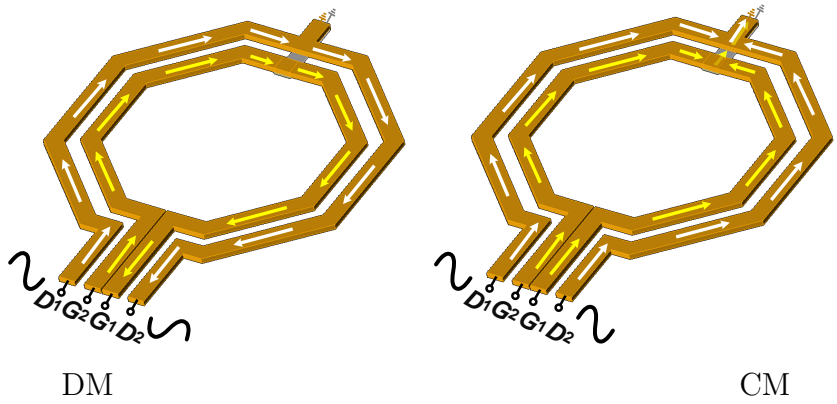


Figure 4.10. Implementation of the transformer.

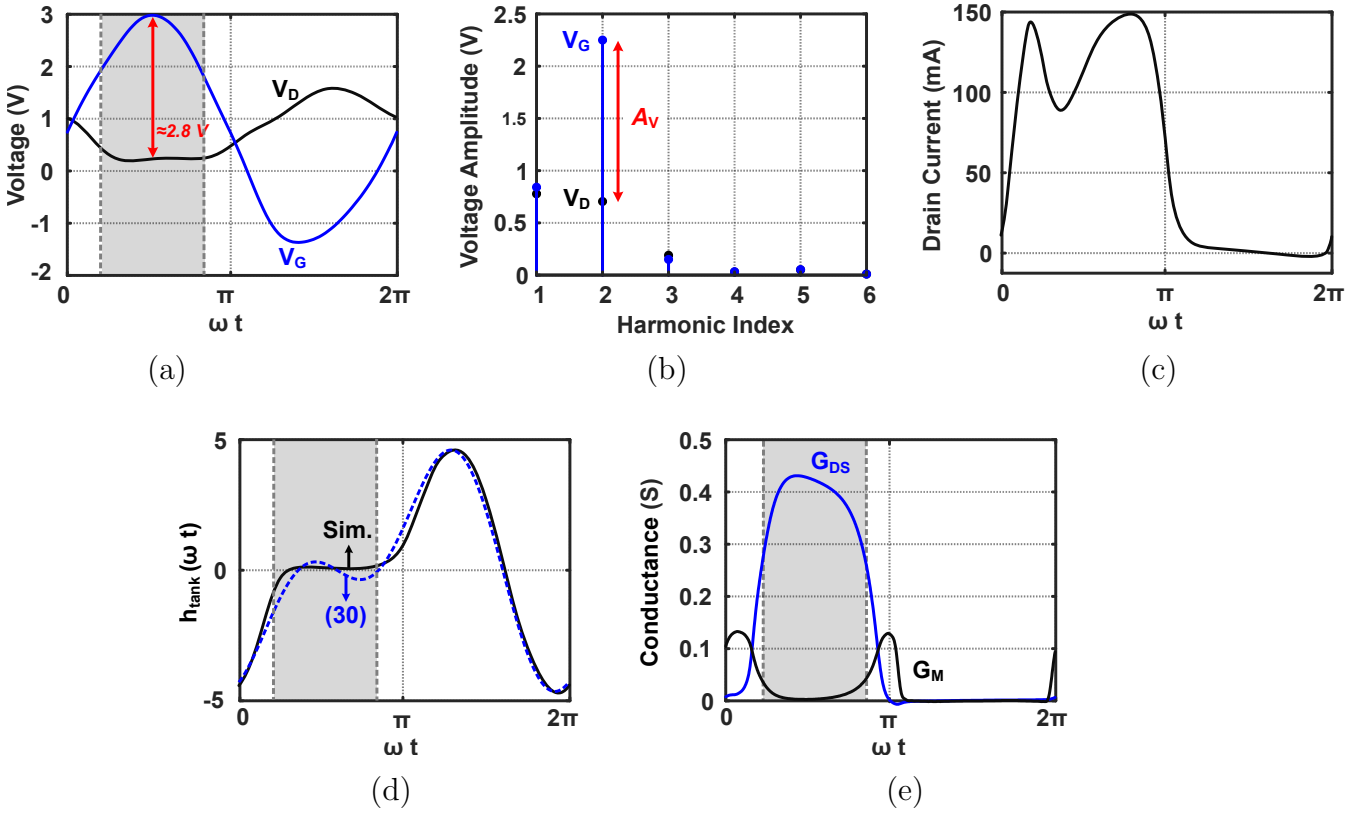


Figure 4.11. (a) Voltage waveforms at drain and gate of the core transistors, and (b) their corresponding harmonic contents. (c) drain current waveform of the core transistors. (d) simulated and calculated [from (4.17)] ISF of the tank. (e) transconductance and channel conductance of the core transistors.

4.3 Phase Noise Analysis

The phase noise performance of the proposed oscillator can be studied using the linear time-variant (LTV) method introduced by Hajimiri et al. [82]. Hence, the phase noise of the oscillator at an offset frequency of $\Delta\omega$ can be estimated by

$$L(\Delta\omega) = 10\log_{10}\left(\frac{\sum_i N_{L,i}}{2(\Delta\omega)^2}\right) \tag{4.14}$$

where $N_{L,i}$ is the effective noise generated by i^{th} device, given by

$$N_{L,i} = \frac{1}{2\pi}\int_0^{2\pi} h_i^2(t)\ \overline{i_{n,i}^2(t)}\ dt \tag{4.15}$$

with $\overline{i_{n,i}^2(t)}$ the white current noise power spectral density of i^{th} noise source and $h_i(t)$ its corresponding impulse phase response given by

$$h(t) = \frac{\Gamma(t)}{q_{max}^2} \tag{4.16}$$

where $\Gamma(t)$ is the periodic impulse sensitivity function (ISF) and q_{max} is the maximum charge displacement across the equivalent output capacitance. Pepe et al. introduced a small signal approach around periodic steady state (PSS) of the oscillator to determine $h(t)$ corresponding to the tank of a generic doubly-tuned oscillator [78]. Thus, by limiting the analysis to first two harmonics, $h(t)$ can be given by

$$h(t) = \frac{|V_1|sin(\omega_0 t + \angle V_1) + 2|V_2|sin(2\omega_0 t + \angle V_2)}{\left(\frac{|V_1|^2}{R_{p1}}\right)Q_1 + 2\left(\frac{|V_2|^2}{R_{p2}}\right)Q_2} \tag{4.17}$$

where V_1 and V_2 are the first and second terms of the unilateral spectrum of the output voltage, respectively. This is a valid result for the proposed tank as long as the contribution of the loss of the tank capacitors (C_s, $C_{p,f}$, and $C_{p,s}$) are sufficiently smaller than the share of the inductor's loss in the overall phase noise. The aforementioned argument indicates that the equivalent loss of the tank can be modeled by a parallel resistance that is in an agreement with the simulations results [83].

The first intuitive conclusion from (4.17) is that reducing $R_{p1,2}$ by increasing X, results in a reduction in $h(t)$ and hence, the overall phase noise. Moreover, the high $Q_{1,2}$ minimizes $h(t)$ since there is no quality factor degeneration mechanism presents in the transformer configuration.

Figure 4.11 (a)-(c) show the simulated voltage and current waveforms of the oscillator. The gate-drain voltage amplitude is kept below 3 V by lowering the supply voltage. This guarantees a 10+ years of reliable lifetime for the active devices [75]. The ratio (X_1/X_2) must be large enough in order to ensure that the voltage waveform is flat when the transistors are operating in the triode region. The flat voltage waveform results in $h(t)$ being negligible minimizing the contribution of the transistors in the overall phase noise [82]. Furthermore, the passive gain of (≈ 3) between drain and gate of the core transistors is achieved at ω_0 by choosing $X = 2$ and $k_m = 0.4$, while its second harmonic is not amplified, as indicated in Figure 4.11 (b). This allows us to consider the voltage at the gate of $M_{1,2}$ as a single tone sinusoidal. Consequently, the equivalent parallel resistance and quality factor at two resonance frequencies are obtained to be ($R_{p1} = 15.5\ \Omega$), ($R_{p2} = 52\ \Omega$) and $Q_1 = 16.4$, $Q_2 = 21.5$ for $Q_s = Q_p = 18$.

Figure 4.11 (d) shows the simulated impulse response corresponding to the tank and its calculated waveform from (4.17). The figure shows that the simulated and calculated waveforms are in a good agreement. Thus, the effective noise contribution of the tank can be

calculated by substituting (4.17) into (4.15).

$$N_{tank} = \frac{4k_BT(P_1 + 4P_2)}{(P_1Q_1 + 2P_2Q_2)^2} \tag{4.18}$$

with

$$P_1 = \frac{|V_1|^2}{2R_{p1}} \tag{4.19a}$$

$$P_2 = \frac{|V_2|^2}{2R_{p2}} \tag{4.19b}$$

Assuming the ratio of $|V_2/V_1| = 0.3$ for having the flat region in the drain voltage waveform, the ratio of (P_2/P_1) in (4.19) can be estimated using (4.6) to be (≈ 0.02). This is mostly due to the fact that the ratio of (X_1/X_2) is chosen relatively large and hence, the ratio of $(R_{p,2}/R_{p,1})$. Therefore, (4.18) is simplified to

$$N_{tank} \approx \frac{4k_BT}{P_1Q_1} \tag{4.20}$$

The ratio between contribution of the loss of the individual inductors in the effective noise of the tank can also be calculated from (4.9) and (4.20) at oscillation frequency as

$$\frac{N_{tank}|_{r_p=0}}{N_{tank}|_{r_s=0}} = \frac{L_p}{L_s} \cdot \frac{V_1^2|_{r_s=0}}{V_1^2|_{r_p=0}} \tag{4.21}$$

Assuming $L_p = L_s$, it is found from simulations that the ratio of the voltages at the right hand side of (4.21) is equal to ≈ 1.45 which can be translated to the effective noise ratio of 1.58 dB. This suggests that the phase noise performance of the oscillator is sensitive to

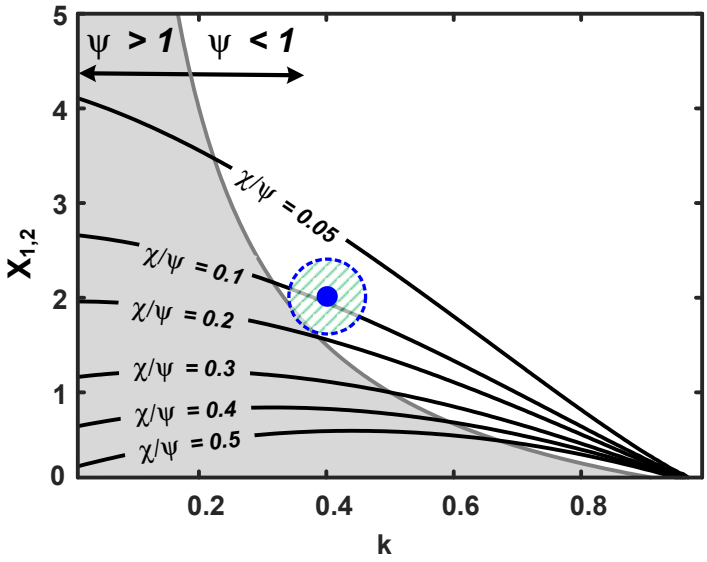


Figure 4.12. Improvement in the phase noise contribution of the tank.

L_s more than L_p. Comparing (4.20) with its equivalent for a second order tank with equal resonance frequency, their ratio can be given by

$$\frac{N_{tank}}{N_{tank,SO}} = \frac{\chi_1}{\psi_1} \tag{4.22}$$

where $N_{tank,SO}$ is the effective noise of the equivalent second order tank. By choosing $X = 2$ and $k_m = 0.4$, χ and ψ can be extracted from Figure 4.5 and Figure 4.6 to be (≈ 0.1) and (≈ 0.95), respectively, and thus, the ratio of ($N_{tank}/N_{tank,SO}$) becomes 0.1. In other words, the noise of the tank in the proposed oscillator is reduced by 90%, compared to its equivalent second order tank. The phase noise improvement described in (4.22) is shown in Figure 4.12. It can be seen that the contribution of the tank loss in the overall phase noise decreases by increasing X. However, from a certain point at the edge of the shaded area, ψ starts to decrease and hence, the power efficiency of the oscillator. Therefore, to minimize the noise contribution of the tank and preserve the oscillator power efficiency, it is preferred to choose the design point close to the edge of the shaded area for each specific k_m. However, for a low

power application that maximizing the power efficiency is desired, X needs to be relatively small for a tank with a weakly coupled transformer.

To calculate the noise contribution of the core transistors, their transconductance (G_M) and channel conductance (G_{DS}) are considered as their dominant noise sources. The effective noise contribution of the transistor due to its G_M is given by

$$\begin{aligned} N_{G_M} &= \frac{1}{\pi}\int_0^{2\pi} h^2(t)\cdot\Big(4k_BT\gamma G_M(t)\Big)dt \\ &\approx 8k_BT\gamma h_{rms}^2 G_{M,EFF} \end{aligned} \tag{4.23}$$

where γ is the excess noise factor of the transistors. Since the effective negative transconductance of the cross coupled pair must compensate the loss of the tank and its own channel resistance at ω_0, it can be expressed by

$$G_{M,EFF} = \frac{1}{A_v}\left(\frac{1}{R_{p,1}} + G_{DS,EFF}\right) \tag{4.24}$$

where $G_{DS,EFF}$ is the effective channel conductance of the core transistors [84]. The output noise due to the channel conductance can be computed similar to the G_M and therefore, the total noise contribution of the transistors can be given by

$$N_{trans} \approx \frac{8k_BTh_{rms}^2}{R_{p,1}}\left[\left(1+\frac{\gamma}{A_v}\right)\left(1+R_{p1}G_{DS,EFF}\right)-1\right] \tag{4.25}$$

First, it can be noticed that the noise contribution due to the transconductance of the core transistors is suppressed by the ratio of $(1/A_v)$. Referring to Figure 4.7, it can be seen that

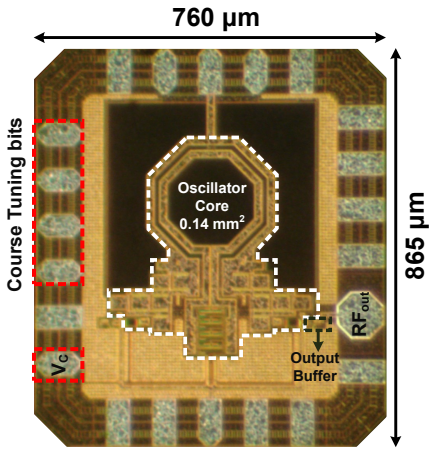


Figure 4.13. Die photograph of the dual tank oscillator.

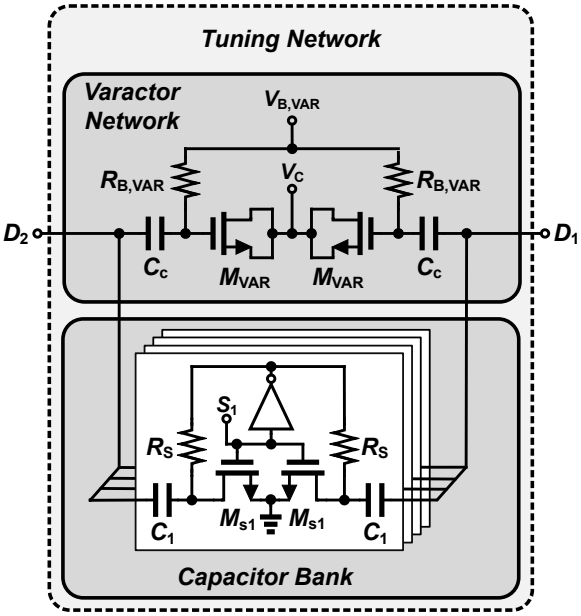


Figure 4.14. Schematic of the varactor network and capacitor bank.

increasing X as well as a relatively small coupling factor reduce the noise contribution of G_M. Furthermore, the channel resistance can have a significant contribution in the output noise since the transistors operate in deep triode region (the shaded area in Figure 4.11) for a considerable portion of a oscillation cycle and hence, G_{DS} becomes large. However, thanks to the flat area in the voltage waveform at the drain, it coincides with the negligible

Table 4.1: Performance Summary and Comparison With Relevant State-of-the-Art LC Oscillators

	This Work	SSCL'20 [79]	JSSC'19 [85]	TCAS-I'16 [86]	JSSC'16 [81]	JSSC'15 [75]	JSSC'14 [80]	JSSC'13 [18]	ISSCC'12 [17]
CMOS Technology	**180 nm**	22 nm	130 nm	65 nm	40 nm	65 nm	65 nm	65 nm	130 nm
Topology	**Dual Tank**	Stacked Comp.	Noise Circ.	Dual Core	Class F_{23}	Class F_2	Hard Clipping	Class F_3	Class B/C
Tuning Range (%)	**10.7**	12.8	18.6	19	25	19	10.2	25	31.4
Center Frequency (GHz)	**5.08**	5.07	2.35	4.07	6.2	4.35	3.92	3.7	3.97
Supply Voltage (V)	**0.85**	0.6	1.2	2.15	1	1.3	1.5	1.25	1.5
Power Consumption (mW)	**71**	15.2	2.58	126.8	11	41.6	48	15	27
PN @ 100 kHz (dBc/Hz)	**-110.2**	-102	-109.8	-114†	-104†	-109†	N/A	-104†	-104†
PN @ 3 MHz (dBc/Hz)	**-146.5**	-139.5†	-137†	-146.7	-135.3†	-144.8	-147.7†	-142.2	-141†
Norm. PN (dBc/Hz)*	**-161.4**	-154.4	-145.2	-159.7	-152	-158.3	-157.2	-154.3	-153.7
FoM @ 100 kHz (dBc/Hz)	**187.1**	185	193.1	185.9	189	185.5	N/A	183.6	181.7
FoM @ 3 MHz (dBc/Hz)	**192.5**	190	195.4	189	187.2	191.8	190.1	192.2	198.1
Freq. Pushing (MHz/V)	**82**	20	<1000	N/A‡	23	N/A	16	50	N/A
Core Area (mm^2)	**0.12**	0.2	0.36	0.37	0.13	0.2	0.19	0.12	0.49
Number of Passives	**1 xfmr**	3 inductors	1 xfmr	2 inductors	1 xfmr	2 xfmr	2 xfmr	1 xfmr	1 inductor

*at 3 MHz offset frequency normalized to 915 MHz carrier frequency.
†estimated from phase noise plot.
‡N/A indicates not available.

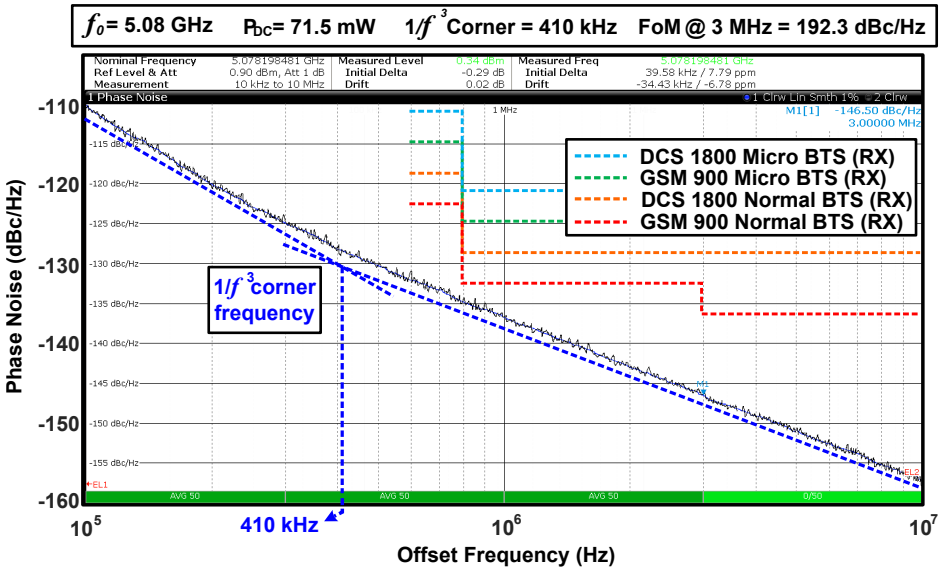
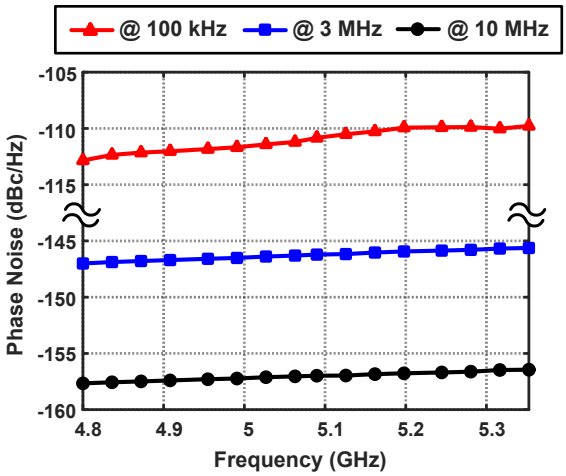
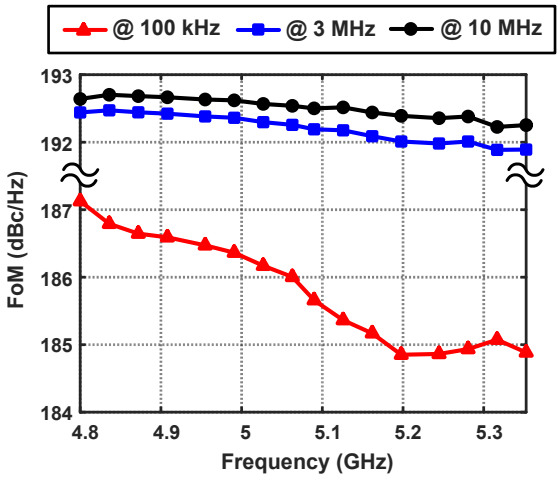


Figure 4.15. Measured phase noise at center frequency of $f_0 = 5.08\ GHz$. Mobile station (MS) and basestation (BTS) requirements are normalized to the carrier frequency.

$h(t)$ span. In other words, the generated noise by the channel resistance does not translate to the phase noise while the transistors are operating in deep triode region. Moreover, the



(a)



(b)

Figure 4.16. Measured (a) phase noise, and (b) FoM versus oscillation frequency.

large voltage swing at the gate of the transistors results in a swift rising and falling edges in the drain current. Therefore, the time span of the non-zero G_M is shrunk and consequently, their contribution in the overall phase noise is reduced.

4.4 Measurement Results

A proof of concept dual tank oscillator is prototyped in $180-nm$ CMOS process technology. The die photograph is shown in Figure 4.13 with a core size of 0.12 mm^2. The technology offers 6 metal layers with an ultra-thick (4.4 μm) top metal layer where the two center-tapped inductors are laid out in. Electromagnetic (EM) simulations showed that the DM and CM quality factors of the primary and secondary are 17.4 and 16.9 while their inductances are 290 pH and 259 pH, respectively. The DM and CM magnetic coupling factors are also found to be 0.41 and 0.45, respectively. The difference can be attributed to the additional length of the center taps that are seen when the tank excitation is CM while are not by DM excitation.

The fixed capacitors $C_{p,f}$, $C_{p,s}$ and C_s are implemented using standard metal-insulator-metal (MIM) capacitors provided by the technology with a capacitance density of 1.13 $fF/\mu m^2$. A 4-bit switchable capacitor bank with a resolution of 120 fF along with a differential varactor network is adopted for course and fine frequency tuning, respectively. The tuning network is able to provide ($\approx$ 11 %) of tuning range. The schematic of the varactor network and capacitor bank are shown in Figure 4.14. The size of the varactors (M_{VAR}) and switches (M_{s1-4}) are optimized so that their losses do not dominate the loss of the tank. However, by switching them on and off, a small change in the equivalent quality factor was observed in the simulations since the quality factor of the capacitors are finite due to the loss of the switches. Further, turning on the individual bits of the capacitor bank adds to X, therefore, $\chi_1(X, k_m)$ increases and an improvement in the phase noise is expected according to (4.12). On the other hand, the ratio of (ω_2/ω_1) deviates from the desired value of 2 resulting in a lower R_{p2} value. This could affect the flatness of the voltage waveform when the transistors are operating in triode region [see Figure 4.11 (a)] and their corresponding ISF. Despite the negative impacts of the capacitor bank on the phase noise, a slight improvement ($\approx 0.2\ dB$) in the normalized phase noise to the center frequency was observed from simulations over

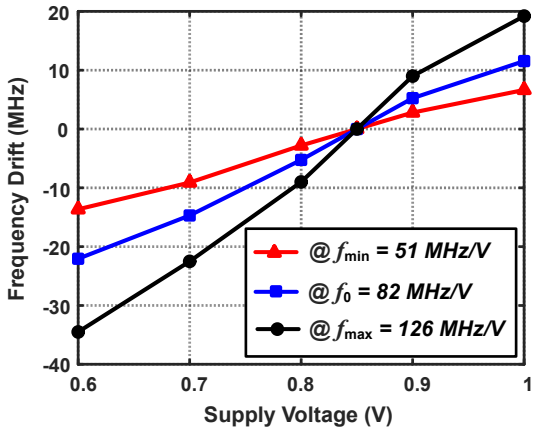


Figure 4.17. Measured frequency pushing versus supply voltage.

the entire tuning range.

The core transistors are implemented using thin-oxide devices of 2 (76 μm/0.18 μm) dimension. The drain and the gate of the transistors are biased through the center tap of the primary and secondary inductors, respectively. The output of the oscillator is connected to the G-S-G RF pad through an open-drain buffer to prevent the loading effect of the measurement instrument on the tank. A parallel combination of three off-chip commercial-of-the-shelf (COTS) capacitors with different self-oscillation frequencies is employed to filter out the noise of the dc bias voltages and tuning codes.

The VCO draws a dc current of 85 mA from a 0.85 V dc supply voltage at center frequency of $f_0 = 5.08\ GHz$. The total dc power dissipation varies from 71.6 to 76.5 mW over the entire tuning range from $f_{min} = 4.8\ GHz$ to $f_{max} = 5.34\ GHz$. Figure 4.15 shows the phase noise spectrum of the VCO. The communication requirements are normalized to the oscillation frequency of $f_0 = 5.08\ GHz$. The phase noise of the oscillator passes the DCS and GSM requirements for micro base-station with a wide margin of ($\approx 8\ dB$). It also meets the though requirements for DCS and GSM normal base-stations with a safe margin of ($\approx 2\ dB$). These requirements are met without sacrificing the reliability of the active

devices or die area.

Figure 4.16 (a) shows the measured phase noise and FoM of the VCO across the frequency tuning range. By normalizing the phase noise to f_0, it can be shown that the phase noise is improved by ($\approx 0.43\ dB$) from f_{max} to f_{min}, as expected from simulations and (4.22). The $1/f^3$ corner frequency of 410 kHz was measured at center frequency of 5.08 GHz. Moreover, it can be seen that the phase noise of the VCO meets the strictest cellular base-station (BTS) and mobile (MS) communication standard of GSM900 with ($\approx 2\ dB$) of margin. To the authors knowledge, this is the lowest phase noise level ever reported in open literature achieved by an oscillator in CMOS IC. It is worth noting that by increasing X and dissipating more dc power, even lower phase noise levels are achievable. Simulation results showed that by increasing the voltage supply to 1 V, causing a 15 % increase in stress across the active devices, phase noise was improved by ($\approx 1\ \ dB$). This is in an agreement with measurement results that showed the same amount of improvement by increasing supply voltage.

Equation (4.26) has been widely used for benchmarking the overall performance of the electrical oscillators in terms of phase noise, power consumption and oscillation frequency [85].

$$FoM = -L(\Delta\omega) + 20 \cdot \log_{10}\left(\frac{\omega_0}{\Delta\omega}\right) - 10 \cdot \log_{10}(P_{dc,mW}) \tag{4.26}$$

where $P_{dc,mW}$ is the total power consumption in mW. The FoM of the VCO at 10 MHz offset frequency stays above 192 dBc/Hz over the entire frequency range where it varies between 192.2 and 192.6 dBc/Hz. The greatest $1/f^3$ corner frequency of 500 kHz is occurred at f_{max} which is about 2 times higher than what was obtained from simulations. The sensitivity of the oscillation frequency to the supply voltage is also measured and shown in Figure4.16 (b). The rate of the frequency drift with change in the supply voltage increases from 51 to 126

MHz/V at f_{min} and f_{max}, respectively.

Table-I summarizes the performance of the dual tank oscillator and compares it with the state-of-the-art low phase noise oscillators. The proposed oscillator offers the lowest normalize phase noise among all of the previously published works while has a high FoM. The size of the VCO is also among the compact designs. Achieving such a low phase noise level was mostly owed to the small equivalent parallel resistance of the tank that necessitates relatively high dc power to produce a sufficient voltage amplitude across the tank. As it was mentioned earlier, for low power application, the design parameter X can be decreased to achieve higher R_p and power efficiency and thus, lower power consumption.

4.5 Conclusion

A new dual tank oscillator structure was introduced in this paper. The common-mode impedance peak was tuned at the second harmonic to form a doubly-tuned tank. This shapes the ISF corresponding to the core transistors that results in a significant reduction in their noise contribution in overall phase noise. A passive gain from the also favors the suppression of the nose translation of the active devices. Further, it has shown that a impedance scaling mechanism in the tank structure decreases the equivalent parallel resistance of the tank and hence its noise contribution. The phase noise performance of the oscillator was analyzed in depth to investigate the impact of different design parameters on the total phase noise. In addition, it has been shown that the oscillator can be optimized for low power applications with a superior power efficiency. The oscillator was implemented and measurement results showed it can achieve a state-of-the-art phase noise level in practice.

Chapter 5

A M-PSK Modulated Polar Transmitter for IoT Applications

5.1 Introduction

By rapidly growing the number of connected devices and nodes to the internet of things (IoT) network, there has been an increasing demand for compact, long range and low power with sufficiently high data rate designs targeting massive production of IoT gadgets [86–88]. This has motivated the researchers to introduce novel approaches to overcome the design challenges and pave the way toward responding the demands [89].

Figure 5.1 represents the typical architecture of a self-sustainable IoT transmitter [90, 91]. The energy harvesting (EH) unit is responsible of providing a sufficient level of dc power for the μ-controller and the transmitter (TX) blocks to properly operate. The μ-controller programs the transmitter thorough the process of collecting information from the sensors and translate them into base-band (BB) signals. Finally, the BB signals are up-converted in the form of modulated signals and transmitted through the transmitting antenna. A battery

is also adopted in the battery-assisted architecture that guaranties a continuous operation of the transmitter when the amount of the received power by EH block is not sufficient to supply the tag.

Several works have been introduced to improve the specifications of the transmitter such as communication range, power consumption, data rate and size [90–101]. Passive architectures offer design simplicity, ultra-low power dissipation with a moderate data rate [90–95]. The transmitter modulates the amplitude and phase of the received signal by adjusting the termination impedance. However, the structure introduces a considerable power loss due to their passive nature that limits the amplitude resolution of the modulated backscatter signal and hence, the data rate and communication range. Furthermore, the passive transmitters are unable to transmit at different frequency from the received signal. This can cause a self-jamming issue at the receiver or transmitter side and requires auxiliary circuits and additional power dissipation to suppress the jamming effect [102]. On the other hand, the active transmitters offer higher transmit power that makes them suitable for long range (LoRa) communication [98–100]. Moreover, they are able to transmit at a different frequency band from the received signal that alleviate the self-jamming issue presents in the passive architectures. The active transmitters mostly utilize frequency modulated (FM) signals to transmit the data that necessitates a stable frequency generator. However, the frequency drift free-running oscillators causes distortion in the transmitted signal and reduces the quality of the communication. Moreover, increasing the data rate requires higher frequency bandwidth that is not freely available in most of the dense frequency bands [103, 104]. It should be noted that this issue can be controlled and suppressed by employing a frequency control loop to stabilize the output frequency of the oscillator at the cost of more design complexity and power dissipation [105].

In this paper, we propose a phase modulated (PM) transmitter architecture. It is composed of

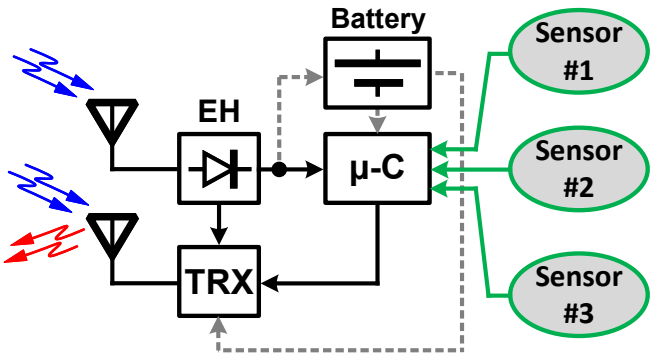


Figure 5.1. Block diagram of a typical IoT tag.

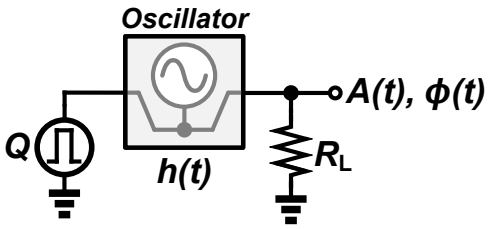


Figure 5.2. Two port model of the oscillator.

an oscillator along with an auxiliary control circuitry to draw a controlled amount of charge from a node in the signal path. Resultantly, the oscillation loop temporally changes the oscillation frequency that leads to a permanent shift in the phase of the output waveform. Therefore, the BB data can be transmitted using the phase modulated signals through a narrower frequency bandwidth. Further, the frequency drift of the free-running oscillator does not cause a significant error in transmitted signal, since it is negligible when translated to the oscillation phase.

This chapter is organized as follows. Section 5.2 explains the preliminaries, describing the general linear time-varying analysis approach of the oscillator. Further, it presents the design methodology of the transmitter, and Section 5.3 shows the post-layout simulation results. Finally, the paper is concluded in Section Section 5.4.

5.2 Design methodology

In this section, we briefly discuss the charge to phase shift translation mechanism in the oscillator structure. We also present the detailed design methodology of the transmitter.

5.2.1 Preliminaries

Figure 5.2 shows the two port model of an oscillator. The linear time-varying function of $h(t)$ describes the impulse response of the oscillator core. The input impulse charge of Q is injected to the output node of the oscillator, in the oscillation feedback loop. $A(t)$ and $\Phi(t)$ are the amplitude and phase response of the oscillator to the injected charge into the output port, respectively. However, due to the presence of the amplitude limiting mechanism in the oscillator structure, $A(t)$ will ultimately vanish and only a permanent phase shift of $\Phi(t)$ in the output waveform is remained [106]. The phase response can be related to the excess injected current at the output using the following equation [19].

$$\Phi(t) = \int_{-\infty}^{t} h(\tau) i(\tau) d\tau \tag{5.1}$$

Equation (5.1) will be used in the next section to determine the relative phase shift in the output waveform of the oscillator and establish the foundation of the transmitter.

5.2.2 Transmitter Design

Figure 5.3 shows the simplified schematic of the transmitter core. It is composed of a ring oscillator and a charge sinking circuit. Five inverter stages are cascaded to provide sufficient gain and phase shift in the feedback loop to satisfy the oscillation criteria [105]. The charge

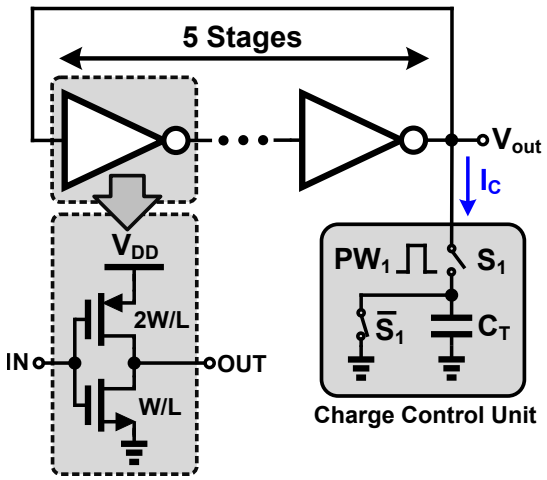
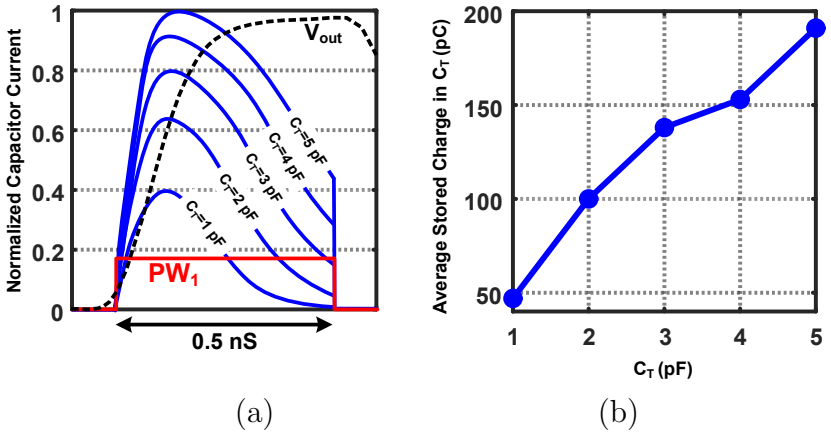


Figure 5.3. Preliminary schematic of the transmitter.



(a) (b)

Figure 5.4. (a) simulated current flowing into C_T, and (b) its corresponding stored charge.

control unit is responsible for drawing a controlled amount of current from output node of the oscillator. The drawn current charges the capacitor through switch S_1, controlled by PW_1. Therefore, the amount of the charge can be adjusted by PW_1, and the capacitance value of C_T. However, utilizing variable capacitance is a more promising approach, due to the time varying nature of the oscillator, as will be discussed later in this section.

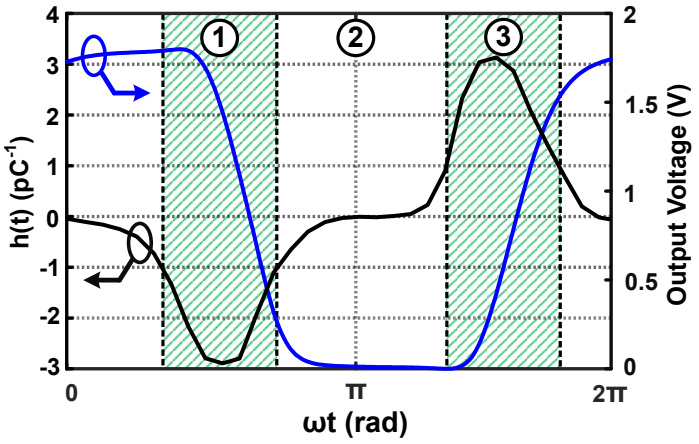
Figure 5.4 (a) shows current flowing into C_T. The control pulse (PW_1) is appplied at the rising edge of the output voltage V_{out}. It can be noticed that the amount of the current increases by the value of C_T, as long as the sinking current is not limited by the last inverter

stage. The resultant charge stored in the capacitor corresponding to I_C is shown in Figure 5.4 (b). It can be seen that the charge increases by increasing C_T, as expected from Figure 5.4 (a). This indicates that the auxiliary charge control circuit is able to adjust the amount of the sunk charge from the output node of the oscillator, and hence can be exploited to the design of a variable phase oscillator.

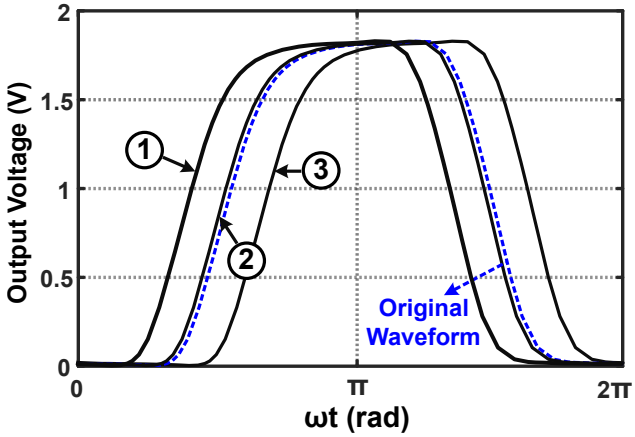
In order to determine the impact of the sunk charge by C_T on the phase of the output waveform, the relationship between them must be studied. As it was discussed in Section 5.2.1, the translation mechanism of I_C and the phase of the output waveform can be determined using (5.1). However, the impulse response $h(t)$ is required to be found for (5.1) to be used to calculate the amount of the phase shift.

Figure 5.5 (a) shows the simulated $h(t)$ by injecting current impulses across an oscillation period into the output node of the oscillator and measuring the phase shift the voltage waveform. It shows the sensitivity of the output voltage to the injected/extracted current ($i(t)$). It can be seen that the voltage waveform is more sensitive to $i(t)$ around the rising and falling edges (hachured areas), while its sensitivity is negligible elsewhere in the voltage waveform. Figure 5.5 (b) represents the impact of extracted current in different time windows in Figure 5.5 (a). It can be seen that applying the control pulse (PW_1) in the flat areas of the voltage waveform causes a negligible phase shift in the waveform. On the other hand, sinking current in the areas near the rising and falling edges (i.e. 1 and 3) has significant impact on the phase of the voltage waveform. Furthermore, sinking current at the rising and falling edges make a lagging and leading phase shift, respectively, corresponding to the sign of $h(t)$. Therefore, it is necessary to synchronize the applying time of PW_1 to desensitize the amount of phase shift to it.

The detailed design of the control circuit is shown in Figure 5.6 (a) and its corresponding logic in Figure 5.6 (b). $V_{o(n)}$ and $V_{o(n-1)}$ are the voltages at the output of n^{th} and $(n-1)^{th}$



(a)



(b)

Figure 5.5. Simulated (a) phase impulse response and its corresponding output voltage waveform of the oscillator, and (b) phase shift in the output voltage due to the extracted current at three different time windows.

stages, respectively, and D_1 represents the inverter delay time. The control pulse with an arbitrary width is applied at an arbitrary time (T_1). The switch M_3 connects $V_{o(n-1)}$ when the control pulse is applied that toggles the output of the latch at rising edge of $V_{o(n-1)}$. However, the change in the state of $\bar{Q_1}$ occurs with a delay equal to D_2. The complementary output of the latch then is fed into the second latch to toggle its output (Q_2). Finally, a NOR block creates a pulse with a width of D_2 when the output of the second lath toggles. In this way, the pulse width of PW_1 is always remains constant and equal to D_2 that can be controlled by adjusting the delay of the latch blocks. Furthermore, it is independent

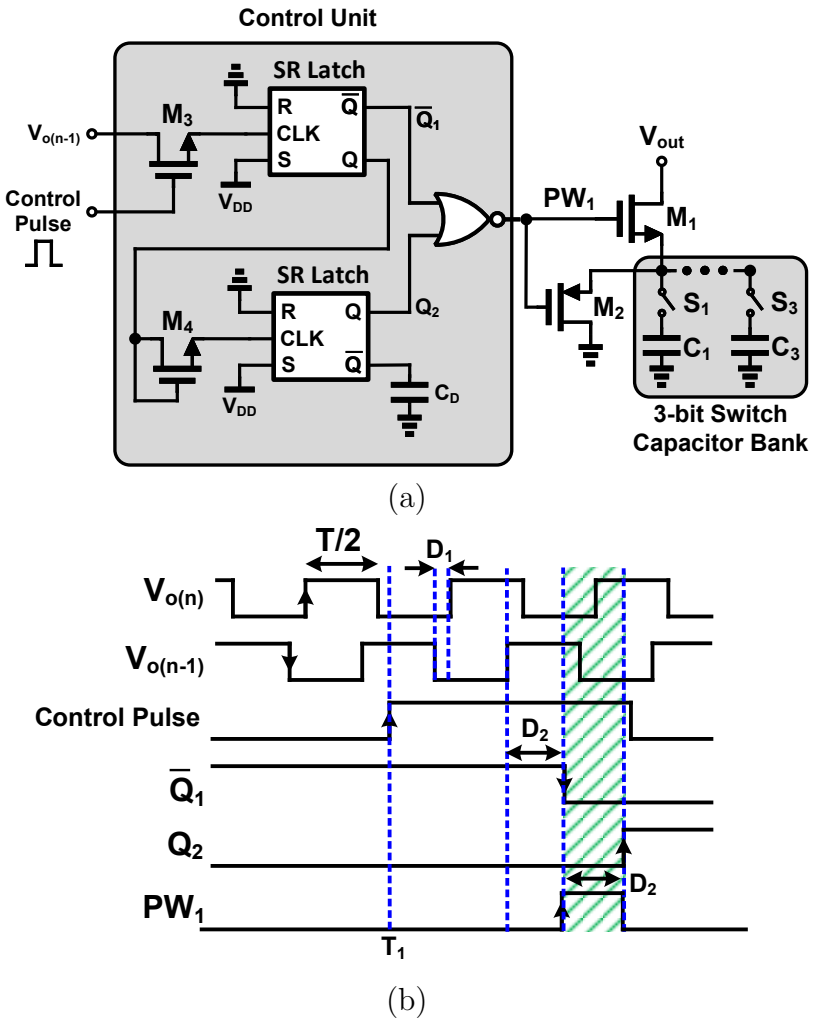


Figure 5.6. (a) schematic of the charge control circuit (excluding the reset circuitry), and (b) its corresponding functioning logic.

from the applying time of the control pulse and its width as long as its width is longer that ($T = 1/f_{OSC}$).

As it can be seen in Figure 5.6 (b), PW_1 spans around the rising edge of the output voltage waveform ($V_{o(n)}$). This maximizes the amount of phase shift due to the extracted charge from the output node of the oscillator, according to Figure 5.5. Moreover, PW_1 is independent from the width and applying time of the control pulse. This relaxes the requirements of the μ-controller whose responsible of generating the pulse.

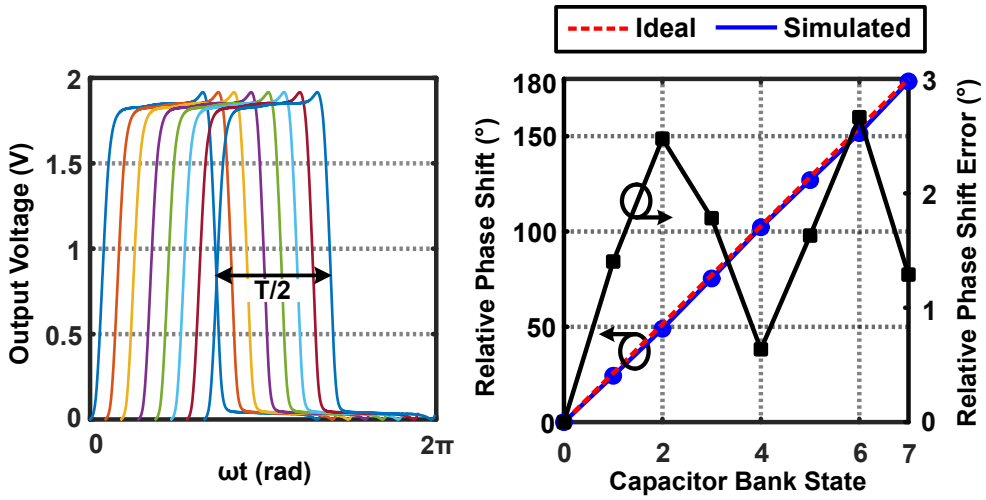
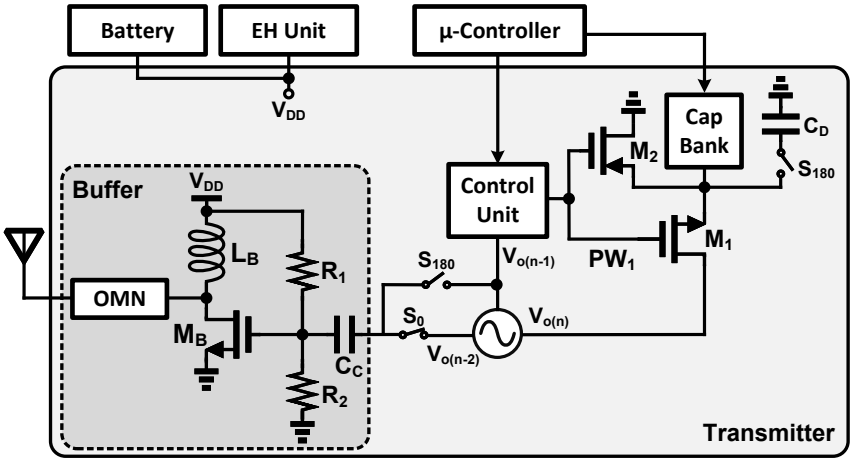
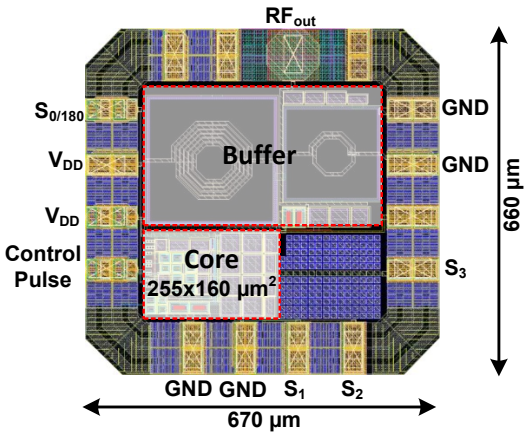


Figure 5.7. (a) simulated time delay in the output waveform for 16 states of the capacitor bank, and (b) its corresponding relative phase shift.

A 3-bit capacitor bank is adopted to tune the charging capacitance and hence, the amount of phase shift. Figure 5.7 (a) shows the time domain output waveform of the oscillator for 8 states of the capacitor bank. Each individual bit is optimized to achieve the minimum the time delay error. The corresponding phase shift due to the drawn charge into the capacitor bank is shown in Figure 5.7 (b). It can be seen that the the maximum error of less than 3 degrees is obtained. This results in a relatively small value of error vector magnitude (EVM), as it will be discussed in the next section. It should be noted that the rate of the phase change is mostly depending on two parameters: i) clock frequency of the μ-controller or base-band (BB) processor, ii) settling time of the oscillator waveform. The former parameter is a limiting factor in both active and passive transmitter categories mentioned earlier in Section 5.1, while the former parameter only affect the performance of the active ones. Simulation results showed that the oscillator reaches its steady state after 3 oscillation period.



(a)



(b)

Figure 5.8. (a) complete schematic of the transmitter, and (b) its layout.

5.3 Post-Layout Simulation Results

The complete schematic of the transmitter is shown in Figure 5.8 (a). The switches S_0 and S_{180} are added to the schematic of Figure 5.3 to double the phase shift range by switching between two complementary waveforms. Capacitor C_D is also added to compensate the delay of the inverter between the complementary nodes (D_1 in Figure 5.6 (b)). The core oscillator is designed at the center frequency of 1 GHz. The buffer block is also designed to isolate the output of the oscillator from the antenna impedance. It should be noted that the buffer circuit can be eliminated according to the power budget of the tag.

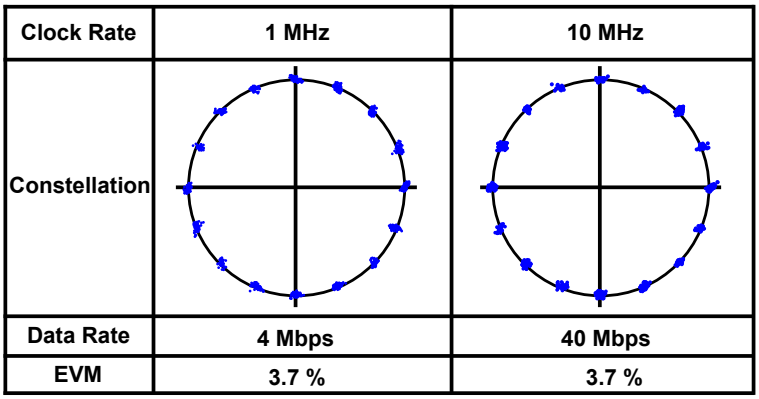


Figure 5.9. Simulated 16-PSK constellation diagram and its corresponding EVM for different μ-controller output clock frequency.

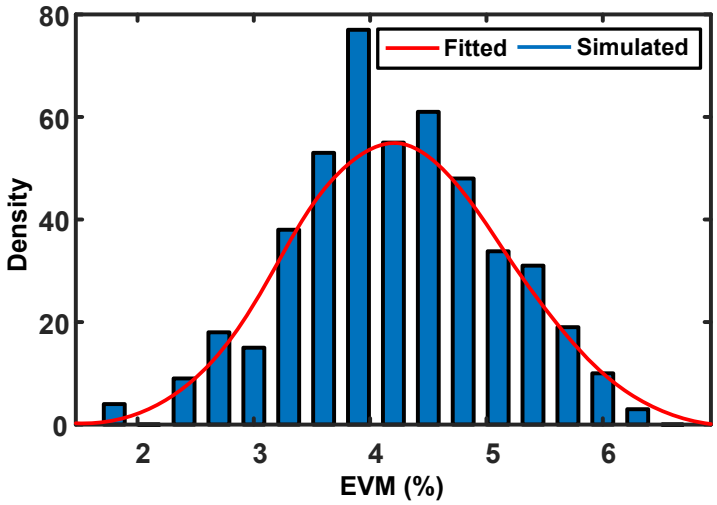


Figure 5.10. Monte-Carlo simulation result for 16-PSK modulated signal and the clock rate of 10 MHz.

The transmitter circuit is laid out in standard TSMC 180-nm CMOS process technology to consider for the parasitics of the active devices and interconnections, as shown in Figure 5.8 (b). The core size is 0.04 mm^2 while the total size of the layout is 0.44 mm^2. The oscillator core dissipates a steady state dc power of 870 μW. This low power dissipation is beneficial for inteligent next generation of communications [107–112]. Figure 5.9 represents the simulated constellation diagram of the output RF signal for 16- phase shift keying (PSK) input BB signal. Assuming an ultra-low power μ-controller with an output clock frequency of 1 MHz, a data rate of 4 Mbps is obtained with an EVM of 3.7 %. In order to evaluate the

performance of the transmitter and its sensitivity to the control pulse [see Figure 5.6], its frequency increased to 10 MHz. It can be seen that a data rate of 40 Mpbs is achieved while the EVM remains unchanged. This indicates the independency of the modulated signal to the width of the control pulse as it was discussed in Section 5.2.2. The transmitter owes this feature to the fast settling time of the oscillator which is shorter than $3T$.

The Monte-Carlo simulation is also performed to investigate the impact of the device mismatches on the EVM performance. As it can be seen in Figure 5.10, the EVM varies from 1.8 to 6.3% following a normal distribution with the standard deviation and mean of 1.1 and 4.2, respectively. Although the mismatch causes increasing in the EVM value, it is still satisfying for most of the applications.

5.4 Conclusion

The design of a polar transmitter was described based on the LTV theory. In order to desensitize the amount of the drawn charge from the output node of the oscillator, a synchronizing circuit was designed. A 3-bit capacitor bank was also adopted to digitally control the time delay of the output waveform and hence, its corresponding phase shift. The transmitter circuit was laid out and post layout simulation results were performed that showed the capability of the transmitter to achieve a data rate of 40 Mbps with an EVM of 3.7 %.

Chapter 6

Conclusion and Open Problems

6.1 Conclusion

In the first part of this dissertation, the impact of the temperature variations was thoroughly studied on the performance of a phased-array transmitter. The compensation techniques including temperature sensor and establishing transconductance zero temperature coefficient were introduced. The designed transmitter was prototyped on a PCB and its performance was measured. Second, a new tank structure was introduced to be used in a transconductance based oscillator circuit. The oscillator's performance was investigated using the derived expression to identify the noise sources and their effect on the overall phase noise. The introduced oscillator is able to provide an ultra low phase noise output waveform with state-of-the-art FoM. Lastly, the design procedure of a low power and compact polar transmitter composed of an oscillator and a PA was described. The transmitter is able to transmit high data rates limited to the clock rate of the BB processor.

6.2 Open Problems

- Studying the impact of the temperature on the integrated GaN HEMT technology, since it is more favorable for nowadays compact applications.
- Implementing the high temperature array of transmitter including antenna array and investigate the impact of temperature on the substrate coupling and antenna pattern.
- Introducing a systematic approach for designing the transformer in the oscillator structure.
- Implementing the designed polar transmitter.
- Applying the mechanism of charge to phase translation to other oscillator classes.
- Extending the introduced polar transmitter design to phased-array architecture.

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