Design and Implementation of Silicon-Carbide-based Four-Switch Buck-Boost DC-DC Converter for DC Microgrid Applications

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ABSTRACT

With the increasing demand for clean and renewable energy, new distribution network concepts, such as DC microgrids and distributed power generation networks, are being developed. One key component of such networks is the grid-interfacing DC-DC power converter that can transfer power bi-directionally while having a wide range of voltage step-up and step-down capabilities. Also, with the proliferated demand for electric vehicle chargers, battery energy storage systems, and solid-state transformers (SST), the bi-directional high-power DC-DC converter plays a more significant role in the renewable energy industry.

To satisfy the requirements of the high-power bi-directional wide-range DC-DC converter, different topologies have been compared in this thesis, and the four-switch buck-boost (FSBB) converter topology has been selected as the candidate. This work investigates the operation principle of the FSBB converter, and a digital real-time low-loss quadrangle current mode(QCM) control implementation, which satisfies the zero-voltage-switching (ZVS) requirements, is proposed. With the QCM control method, the FSBB converter efficiency can be further increased by reducing the inductor RMS current and device switching loss compared to traditional continuous current mode(CCM) control and discontinuous current mode(DCM) control. Although the small signal model has been derived for FSBB under CCM control, the small ripple approximation that was previously used in the CCM model no longer applies in the QCM model and causing the model to be different. To aid the

closed-loop control system compensator design, QCM small signal model is desired. In this thesis, a small signal model for FSBB under QCM control is proposed.

A 50 kW silicon carbide (SiC) based grid-interfacing converter prototype was constructed to verify the QCM control implementation and small signal model of the FSBB converter. For driving the 1.2kV SiC modules, an enhanced gate driver with fiber optic (FO) based digital communication capability was designed. Digital on-state and off-state drain-source voltage sensors and Rogowski coil-based current sensors are embedded in the gate driver to minimize the requirement for external sensors, thus increasing the power density of the converter unit. Also, Rogowski-coil-based current protection and drain-source voltage-based current protection is embedded in the gate driver to prevent SiC switching device from damage.

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GENERAL AUDIENCE ABSTRACT

The renewable energy sector is driving the development of new distribution networks, such as DC microgrids and distributed power generation networks. One crucial component of these networks is the grid-interfacing DC-DC power converter, which can transfer power in both directions while maintaining a wide voltage range. This study evaluates various topologies and selects the four-switch buck-boost (FSBB) converter topology to meet the demands of high-power, bi-directional, and wide-range DC-DC converters. This work analyzed the operation of the FSBB converter and proposed a novel simplified quadrangle current mode (QCM) control implementation. With the QCM control method, the FSBB converter efficiency can be further improved by reducing losses compared to conventional control methods. This study also provides a small signal model, which can be used to aid the control loop compensator design where application of FSBB converter is required.

A 50 kW silicon carbide (SiC) based grid-interfacing converter prototype, which was constructed to validate the proposed QCM control implementation and small signal model of the FSBB converter. As part of the converter unit,the enhanced gate driver design and implementation is presented in this thesis. This gate driver is designed with fiber optic-based digital communication, drives the wide bandgap SiC modules. The gate driver also features embedded digital on-state and off-state drain-source voltage sensors and non-intrusive current sensors to minimize external sensor requirements, thereby increasing the power density

of the converter unit. The gate driver also incorporates high bandwidth current protection and drain-source voltage-based current protection to protect the SiC switching device from damage.

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Chapter 1

Introduction

1.1 Application Background

Since the first industrial revolution and the invention of steam engines in the 19th century, fossil fuels consumption has been steadily growing in the previous centuries. But burning fossil fuels releases carbon dioxide, which is known as one of the greenhouse gases that contribute to climate change. The concern of global warming has significantly accelerated the energy industry to transition from fossil fuels to renewable energy.

1.2 Micro-grid Power Systems

Alternative energy generation, such as solar energy, geothermal, and wind power generation, is gaining more attention in recent decades. Different from the traditional power generation stations that have single large plant energy generation capabilities, renewable energy generation can be implemented in a distributed manner. For example, residential and commercial solar panels can be installed without first being delivered to the power grid. The solar energy industry has also been aggressively expanding in recent years. But the traditional power grid system is not designed for distributed power generation. An illustration of the traditional power distribution network is shown in Figure 1.1. In traditional power distribution networks, the different voltage levels are converted by transformer-based sub-

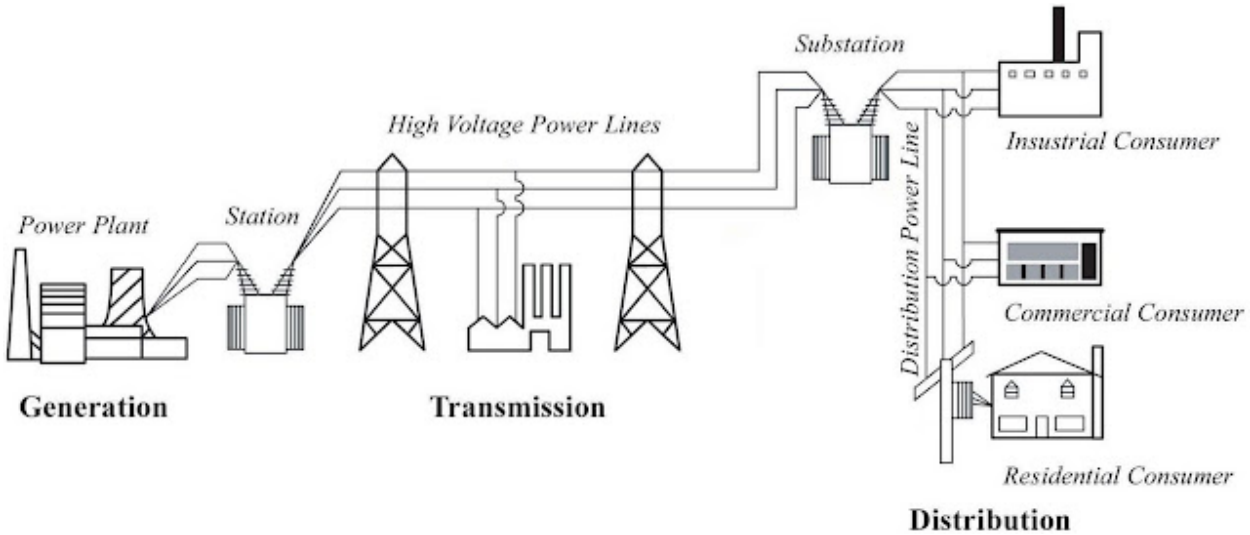


Figure 1.1: Conventional power grid topology

stations. Transformer-based substations only support unidirectional power flow. Micro-grid is one of the solutions to this problem. The micro-grid could utilize the locally generated energy, therefore reducing the transmission and conversion loss, as shown in Figure 1.2. Also, the microgrid can operate in islanding mode, which does not depend on the external utility connection, or in grid-connected mode, consuming or supplying energy to the utility grid, based on local energy generation status, such as solar intensity for photovoltaic panels. As a result, a bi-directional, grid-interfacing substation converter between the microgrid and utility grid is required.

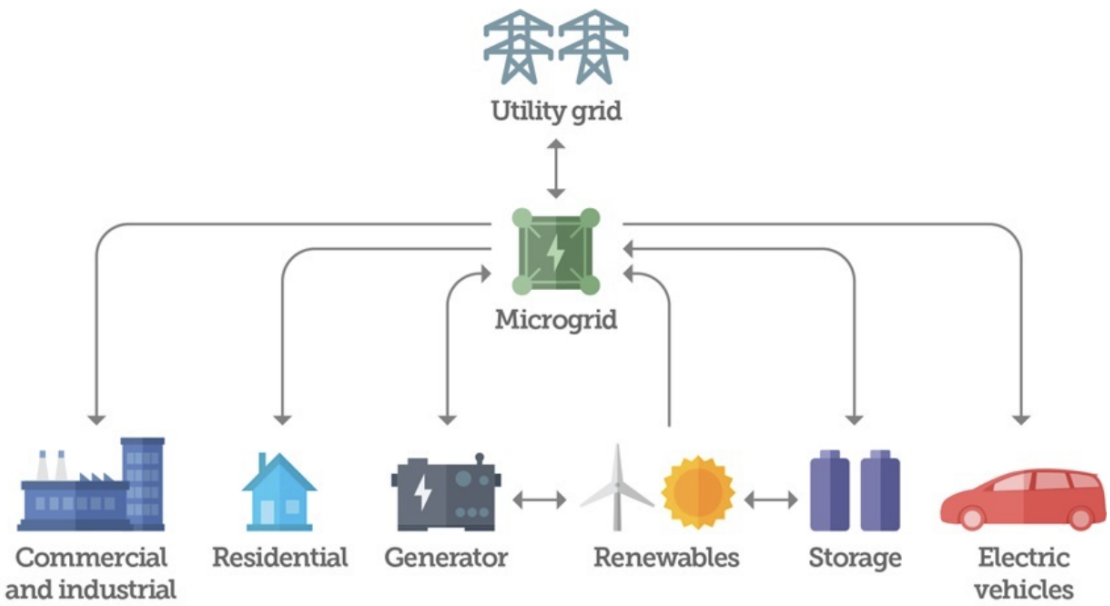


Figure 1.2: Micro-grid topology

1.3 DC Micro-grid

1.3.1 Electric Vehicles

Sales of plug-in electric vehicles (PEVs) have proliferated in the past decade. With the increasing demand for PEVs, fast EV charging technologies are also required. With the traditional AC charger, an onboard rectifying charger is required, therefore creating a limit for the charging speed. DC fast charging eliminates the requirement of an on-board charger and can directly charge the batteries and bypass the on-board charger limitation[1][2][3]. Therefore, the DC charging stations standard has been adopted, creating the need for DC power networks.

1.3.2 Energy Storage for Renewable Energy Systems

Unlike traditional electricity generation power plants with constant generation capacity all day, solar generation is highly dependent on solar radiation intensity, which will peak at noon, and no energy can be generated overnight. This creates the duck curve phenomenon, which requires some amount of energy generated by traditional power plants. This means that the conventional power plant's capacity is still crucial during the evening to supply the peak. As a result, during peak solar intensity hours, over-generation can happen. One of the ways to flatten the curve is battery energy storage infrastructure. The energy storage infrastructures can store energy that has been over-generated and supply the power grid during peak hours. Similar to EV charging, since the battery only stores and provides DC power, if the power networks utilize DC, the rectifying and inverting stage will no longer be required, increasing the total energy storage system efficiency[4].

It is very clear that a power electronics converter system that can interface between the DC source or DC micro-grid and the existing ac grid is very crucial. Particularly, a bi-directional DC-DC converter with wide-range voltage regulation is desired. In general, there are two types of DC-DC converters: non-isolated and isolated types. The isolated DC-DC requires the design and implementation of a high-frequency transformer and corresponding converter stages, leading to more costs and losses due to a greater number of conversion stages[5]. However, non-isolated DC-DC converters can be much simpler and more efficient[6]. Due to many systems offering galvanic isolation by the ac transformer, non-isolated bi-directional DC-DC converters with wide-range voltage regulation as the interface to DC microgrid will be very attractive in these types of system applications.

1.4 Non-isolated Bi-directional Buck-Boost DC-DC Converter Topology Survey

In order to fulfill the specification of a bi-directional, non-isolated DC-DC converter topology with a wide step-up and step-down range, a comparison of different bi-directional buck-boost converters has been conducted. Each of the converter topologies will be evaluated in 7 parameters: efficiency, number of passive devices, number of switching devices, voltage conversion ratio, control simplicity, magnetic component size, and high power scalability. Each of the parameters will be evaluated in 0 to 5 score range, a higher score represents the topology is more desirable. Since the converter with minimal components are more desirable, and in this evaluation, all topologies require minimum of 3 passive devices and 2 switching devices, therefore topologies with 3 passive devices or 2 switching devices will have a 5 score, and additional components will have a lower score.

1.4.1 Inverting Bi-directional Buck-boost Converter

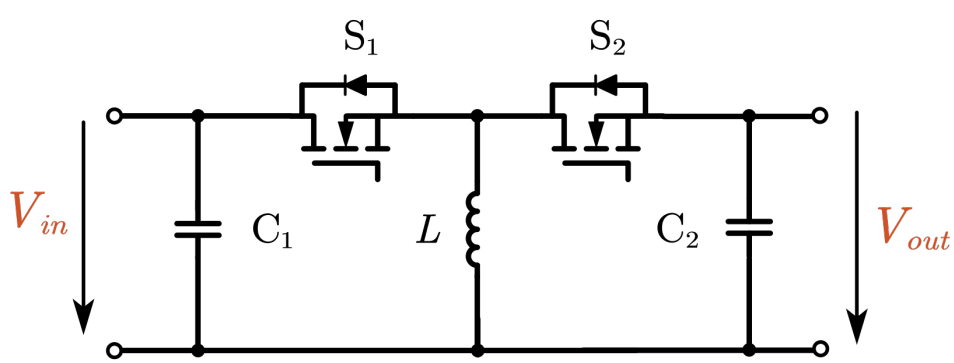


Figure 1.3: Inverting bi-directional buck-boost converter

The inverting bi-directional buck-boost converter (IBBBC), as shown in Figure 1.3 is one of the basic topologies derived by the unidirectional buck-boost converter by replacing the diode with a switching device. Therefore only two switching devices are required. This

topology operates exactly as a unidirectional buck-boost converter, and the symmetrical topology makes sharing forward and reversed biased control logic possible, which makes it simple to control. Also, this topology only requires three passive components, two capacitors, and one inductor. For the voltage translation ratio as shown in eq.1.1, the IBBBC has an inverting voltage polarity, which is undesired in most high-power applications. The IBBBC cannot achieve ZVS without additional resonance or an active clamp circuit; thus, switching loss is considered high. The radar chart of IBBBC is shown as in Figure 1.4.

$$\frac{V_{in}}{V_{out}} = -\frac{D}{1-D} \tag{1.1}$$

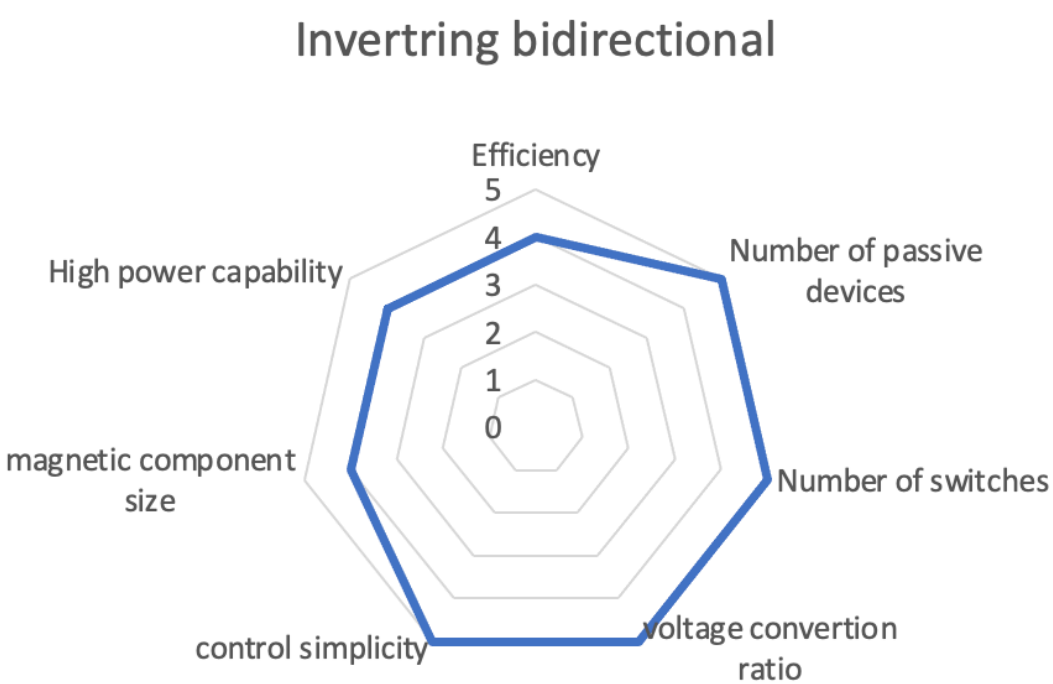


Figure 1.4: Radar chart of Inverter bidirectional

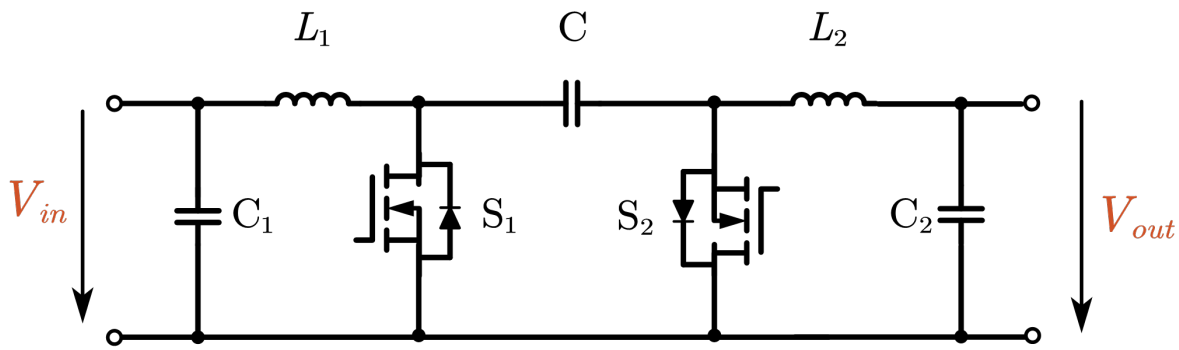


Figure 1.5: Cuk converter topology

1.4.2 Cuk Converter

Similar to IBBBC, bi-directional Cuk, as shown in Figure 1.5 converters are derived from uni-directional Cuk converters by replacing the diode with switching devices. The Cuk converter only requires two switching devices but requires five passive components, two inductors, and three capacitors. Especially for the mutual coupling capacitor between two switching devices, the capacitance is required to be large because it is used for transferring energy, which makes it undesired for high-power applications. The Cuk converter also needs external circuits for achieving ZVS, and the voltage conversion ratio can be described as in eq.1.2 , the voltage polarity is inversed, which is also undesired for most high-power applications. The radar chart for Cuk converter evaluation is shown in Figure 1.6.

$$\frac{V_{in}}{V_{out}} = -\frac{D}{1-D} \tag{1.2}$$

1.4.3 SEPIC/ZETA Converter

As Figure 1.7 show the SEPIC/ZETA converter is a rearrangement of the Cuk converter. In order to deliver a positive voltage polarity and make it more desirable in high-power

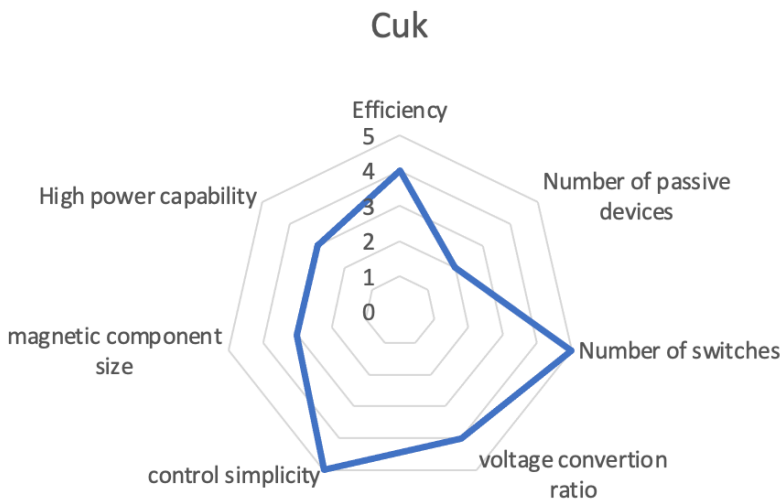


Figure 1.6: Radar chart of Cuk converter

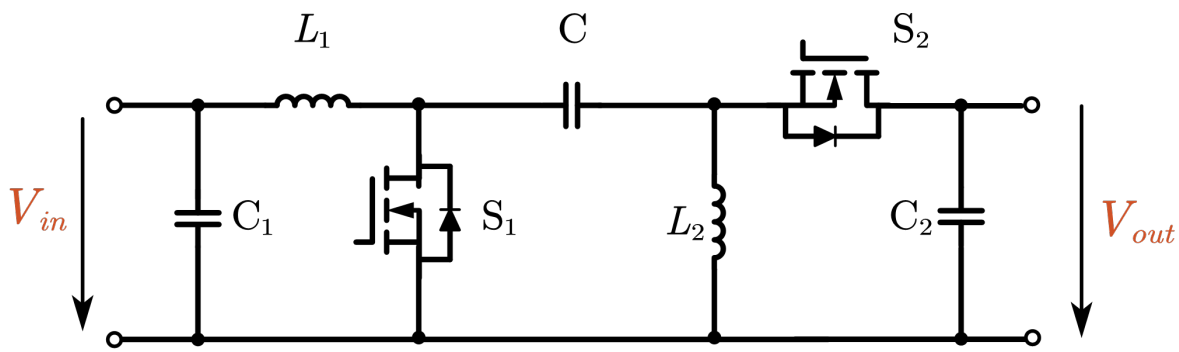


Figure 1.7: SEPIC/ZETA converter topology

applications. The voltage conversion ratio of the SEPIC/ZETA converter is shown in eq.1.3. Because of the rearrangement, the converter topology is no longer symmetrical. As a result, the control algorithm for forwarding and reversed bias operation must be designed separately. In the meantime, the SEPIC/ZETA converter shares the same disadvantages, such as more passive components and high mutual capacitor capacitance are required, and ZVS cannot be natively achieved. The radar chart for SEPIC/ZETA converter evaluation is shown in Figure 1.8.

$$\frac{V_{in}}{V_{out}} = \frac{D}{1-D} \tag{1.3}$$

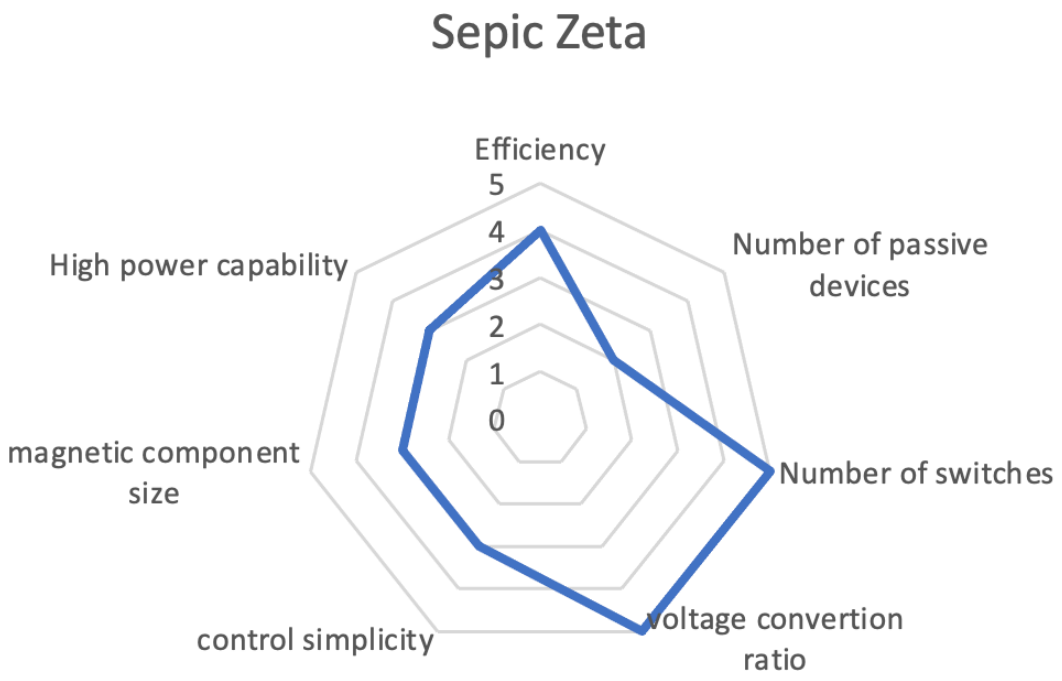


Figure 1.8: Radar chart of SEPIC/ZETA converter

1.4.4 Combined Half-bridge Converter

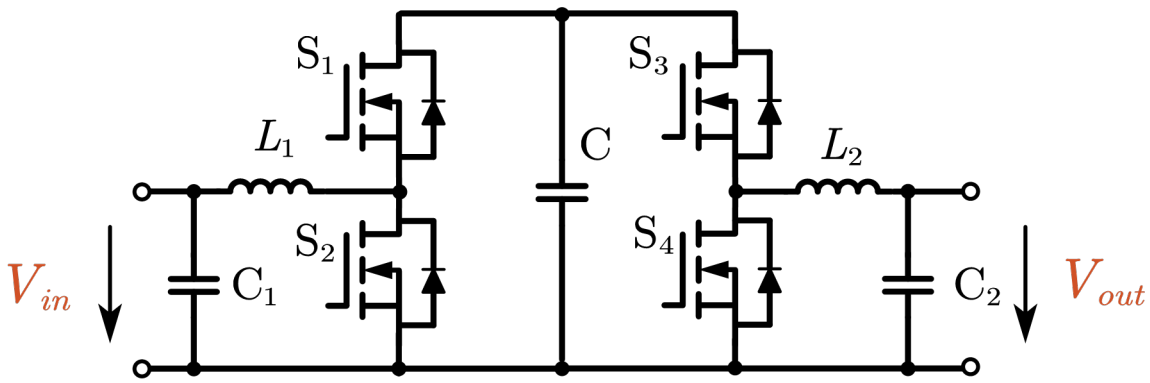


Figure 1.9: Combined Half-bridge Converter topology

The combined half-bridge converter (CHB) is one of the most common bi-directional converters, as the topology is shown in Figure 1.9. The CHB converter can be considered a two-stage with an internal DC bus. When the CHB converter operates in forwarding bias, the power flows from input to output, the input half-bridge operates as a boost converter, and the output half-bridge operates as a buck converter. This converter has a non-inverting output voltage and requires five passive switching devices, three inductors, and two capacitors. Also, this converter topology can not achieve ZVS without additional components. Since the CHB converter has a symmetrical topology, the control algorithm can be shared for both forward and reverse operations, reducing the control complexity. The radar chart for the CHB converter is depicted in Figure 1.10.

$$\frac{V_{in}}{V_{out}} = \frac{D}{1-D} \tag{1.4}$$

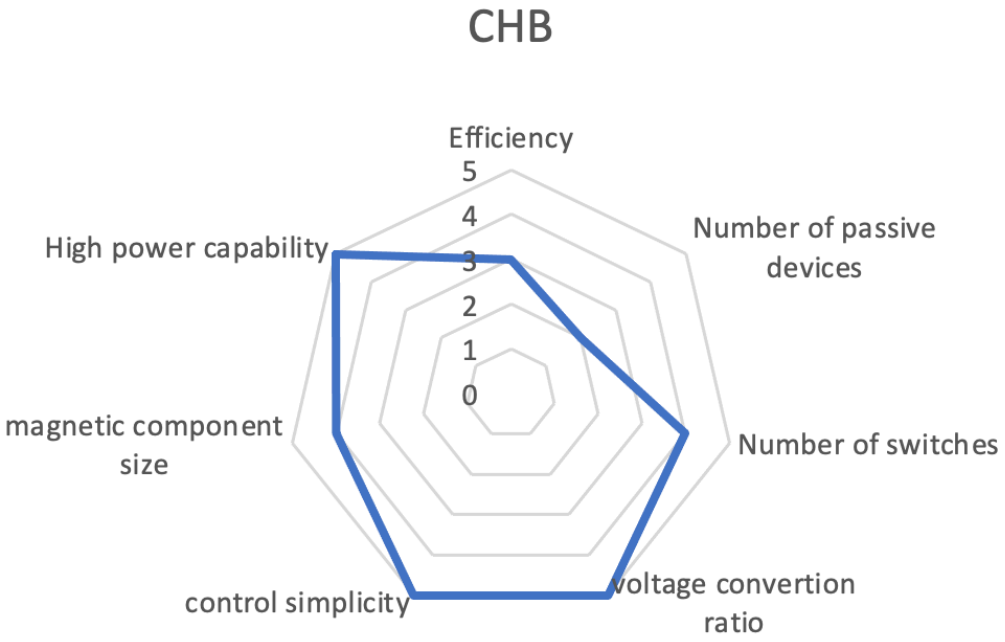


Figure 1.10: Radar chart of CHB

1.4.5 Four-Switch Buck-Boost Converter

The four-switch buck-boost (FSBB) converter has been a popular area of research in recent years. The topology of an FSBB converter shows in Figure 1.11. The only disadvantage of the FSBB converter is that it requires four switching devices, which its benefits can offset. The FSBB converter reduces switching loss by achieving ZVS inherently without any external components. The FSBB converter requires only three passive devices, one inductor as well as input and output capacitors. Due to its symmetrical topology, the control is relatively simple since the same control algorithm can be used for bi-directional operation. This topology is also a competitive candidate for scaling up for high-power applications because a low inductor inductance value is required for ZVS operation, further enhancing the power density.

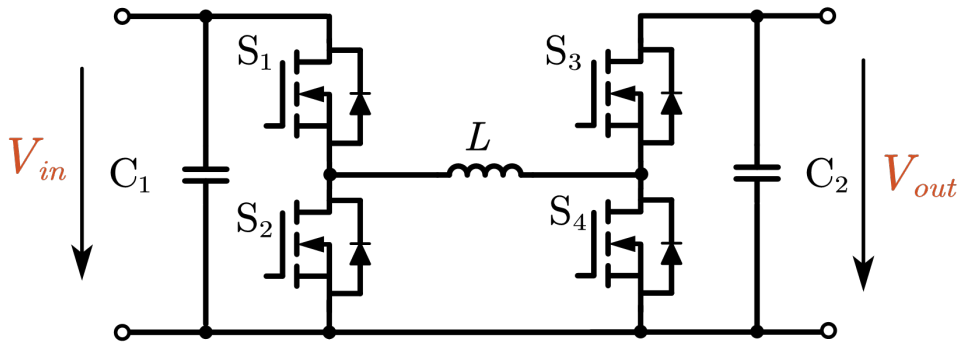


Figure 1.11: Four-Switch Buck-Boost converter topology

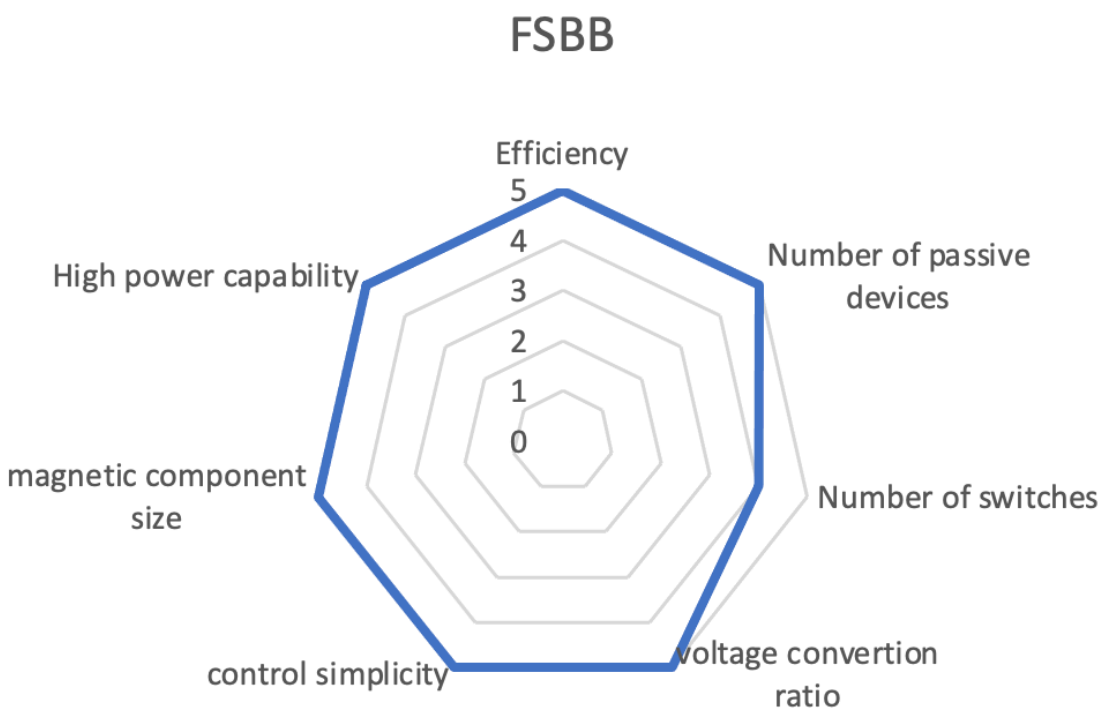


Figure 1.12: Radar chart of FSBB

1.4.6 Switched Capacitor

Switching capacitor topology is also widely used for battery energy storage applications. The topology utilizes only one inductor but four capacitors for its operation. The switched capacitor topology has a dedicated high-voltage side and a low-voltage side. Although it has a high step-up/step-down ratio range, this topology cannot achieve both step-up and

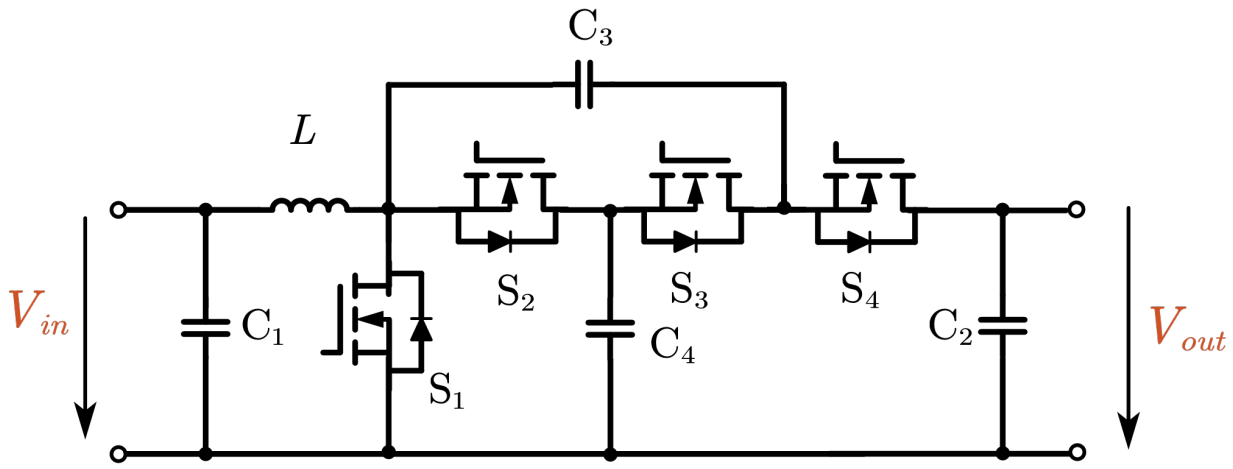


Figure 1.13: Switching capacitor topology

step-down bi-directionally. The converter can achieve ZVS without external circuits, and the efficiency of the converter is high.

1.4.7 Summary of Non-isolated Bi-directional DC-DC Converter Topologies

When comparing all six non-isolated bi-directional DC-DC converters, all of the converter topologies except the switching capacitor converter can step up or down the voltage bi-directionally. Other topologies, such as switching inductor converters, are not included in this comparison because those topologies lack the capability to step up and step down in both directions. The radar chart of all converter topologies that compared above has been summarized and compared in Figure 1.15. Only FSBB and switching capacitor topology can achieve ZVS natively using a single inductor. In terms of passive components,the IBBBC and FSBB converter have the lowest component count. The Cuk converter, IBBBC, CHB converter, and FSBB converter have symmetrical layouts, eliminating the need to design two separate controllers for bi-directional operation. As a result, the FSBB converters are

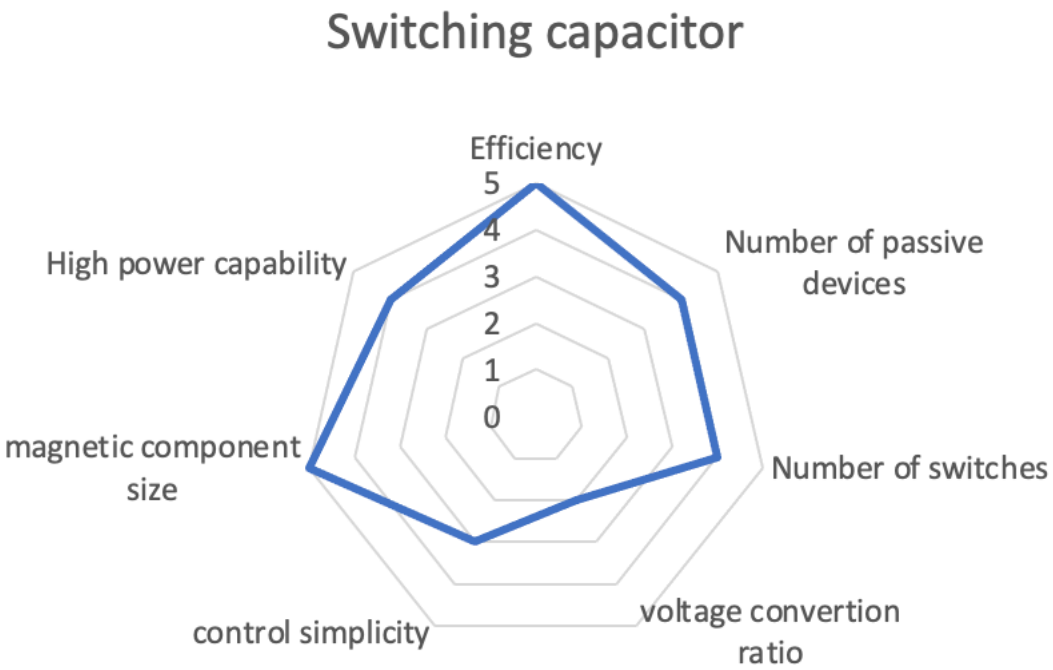


Figure 1.14: Radar chart of Switching capacitor

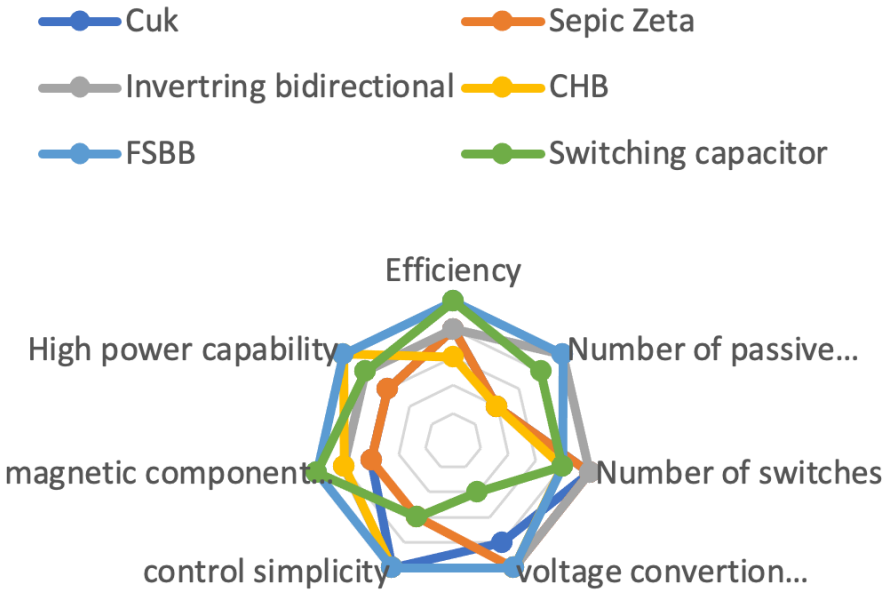


Figure 1.15: Radar chart of non-isolated bi-directional DC-DC converter

selected for the DC-DC stage implementation of the grid interfacing converter unit.

For high power application of the FSBB converters, turn off loss is significant especially with fast switching SiC MOSFETS. As a result, a controlling method that can reduce the inductor current of FSBB converter operation is desired. The detailed analysis of operation principles and high-efficiency control methods is discussed in chapter 2. Also with the new modulation method (QCM modulation), the small signal model that was previously proposed for CCM will no longer be applied. As a result, a new small signal model for QCM modulation is proposed in Chapter 4.

1.5 Silicon Carbide Gate Driver

With the demand for higher power density, higher efficiency, and higher operation voltage, Silicon carbide (SiC) MOSFET has gained more popularity because SiC MOSFET has the characteristics of high blocking voltage, low on-resistance, and low output capacitance (C_{oss}), and fast-switching characteristic (high dv/dt). But those characteristics create challenges for gate driving circuit design, specifically for the protection circuit design and EMI/ EMC of the signal processing circuits design. Also, with the development of the integrated circuits industry, more and more functionalities can be integrated into the gate driver circuits board without increasing the board's footprint. Specifically, the integrated sensor of the voltage and current sensors on the gate driver board can significantly reduce the number of external sensors required, which can substantially increase the converter's power density. Previous work has been done on high speed SiC gate drivers and the EMI and EMC designs in [7][8][9], and the gate driver embedded Rogowski coil current sensor has been presented in [10] and [11]. Furthermore, the gate driver based on-state voltage measurement capability and junction temperature estimation has been discussed in [12], and the phase current reconstruction with

Rogowski coil sensors has been presented in [13].

But an universal gate driver design that includes all of those sensing capabilities and can adapt different SiC modules has not been designed previously. The design and implementation of an enhanced universal gate driver are discussed in Chapter 3 of this thesis.

1.6 Motivation

The motivation and objective of this thesis are to further explore the four-switch buck-boost (FSBB) converter that utilizes silicon carbide MOSFET for high power grid interfacing converter unit applications. A high efficiency controlling method is desired for such converter units. Also for designing the closed-loop control of the FSBB converter, a small signal model is required to aid the compensator design for better system stability.

For the grid interfacing converter, a complete and universal gate driver design that includes all sensors and can be utilized on different topologies as well as different SiC MOSFET modules, up to 1.2 kV rating has not been implemented before. Therefore, this thesis will explore and propose an implementation of such an universal gate driver.

1.7 Thesis Outline

In Chapter 2, the different topology of non-isolated buck-boost converter topology is compared. The operation principle of the four-switch buck-boost converter and the quadrangle current mode control method is explained. The implementation of the QCM real-time control method (min RMS ZVS block) is introduced, and the open loop performance is verified.

In Chapter 3, the three-board gate driver design is introduced. The V_{ds} based current sensing protection and Rogowski coil protection are compared. The gate driver embedded voltage

sensor and Rogowski-coil-based current sensor operation principle are explained. The gate driver sensors and protection are verified with testing. Further improvements for gate drivers are listed.

Future work relating to the FSBB converter is discussed in Chapter 4. To aid the design of the FSBB converter closed-loop control, a small signal describe model under QCM operation has been proposed.

Chapter 2

FSBB Converter Quadrangle Current Mode Control

2.1 Operation of the Buck-Boost Converter

Two-switch buck-boost converters (as depicted in Figure 2.1) can operate in buck mode, boost mode, or buck-boost mode. In buck-boost mode, Device S_1 and S_2 share the same control signal. The duty cycle for both devices is denoted as D when both devices are turned on, and during $1-D$ both switching devices are turned off. Therefore the topology has two switching states. When both S_1 and S_2 are turned on, the input voltage V_{in} is applied to

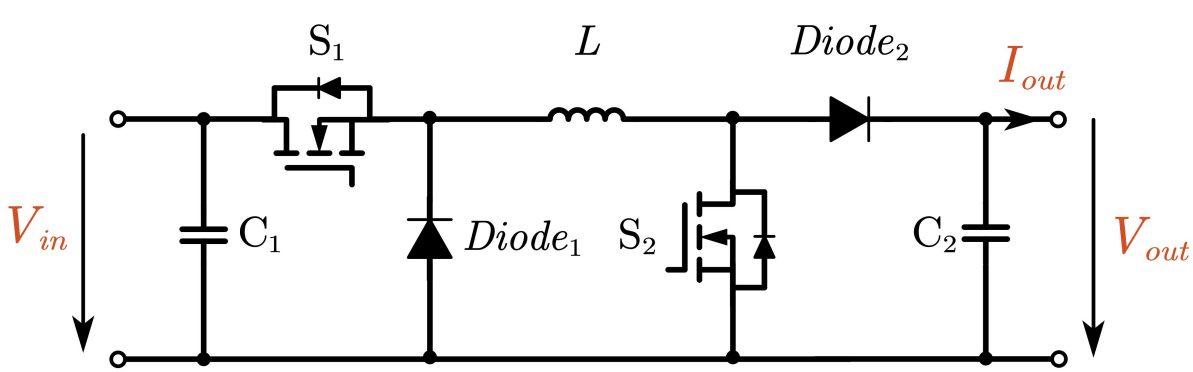


Figure 2.1: Two-Switch buck-boost converter
c

the inductor, storing the energy from the source into the inductor, both $Diode_1$ and $Diode_2$

block the voltage and current since they are reverse biased. In the meantime, the output capacitor discharges, supplying the output current I_{out}. The DC transfer function between V_{in} and V_{out} under ideal conditions can be described as eq.2.1[14]. The control and current waveform of the two-switch buck-boost converter is shown in Figure 2.2.

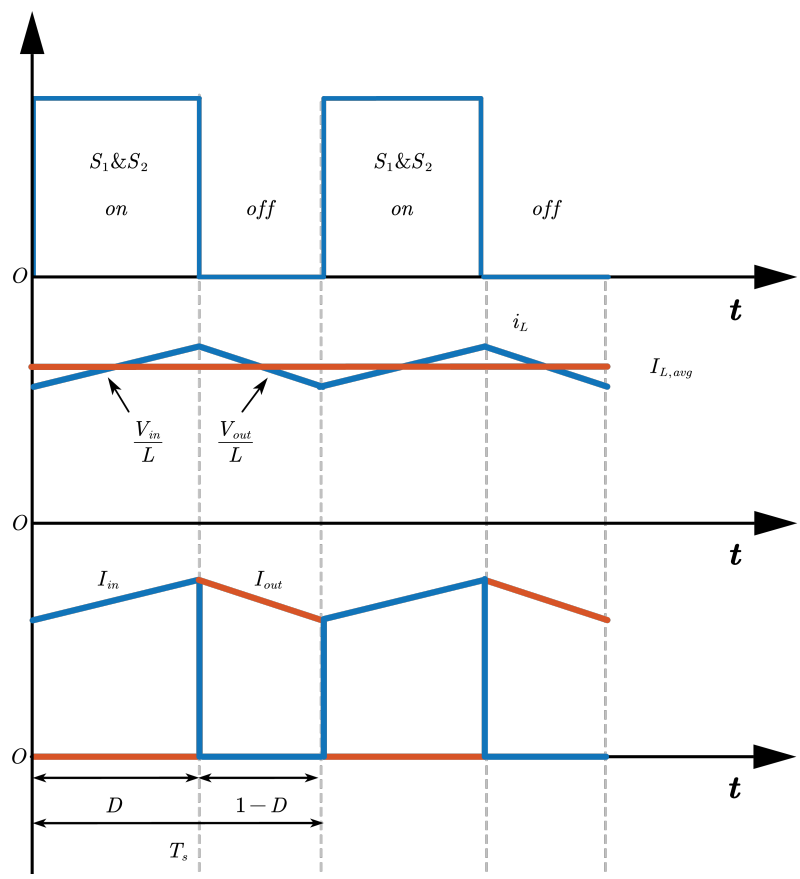


Figure 2.2: Control and current waveform two-switch buck-boost converter

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{2.1}$$

In this topology, $Diode_1$ and $Diode_2$ will generate loss when the diode is in forwarding bias operation, where the input current and output current of the topology are denoted as I_{in} and I_{out} as in Figure 2.1. Assuming both diodes have the same voltage drop V_f and ignoring

the I_{in} and I_{out} ripples since it is operated in CCM mode, the diode conduction loss can be represented with eq.2.2.

$$P_{fwdloss} = V_f \times (1 - D)(I_{in} + I_{out}) \tag{2.2}$$

2.2 Four-Switch Buck-Boost Converter Operation

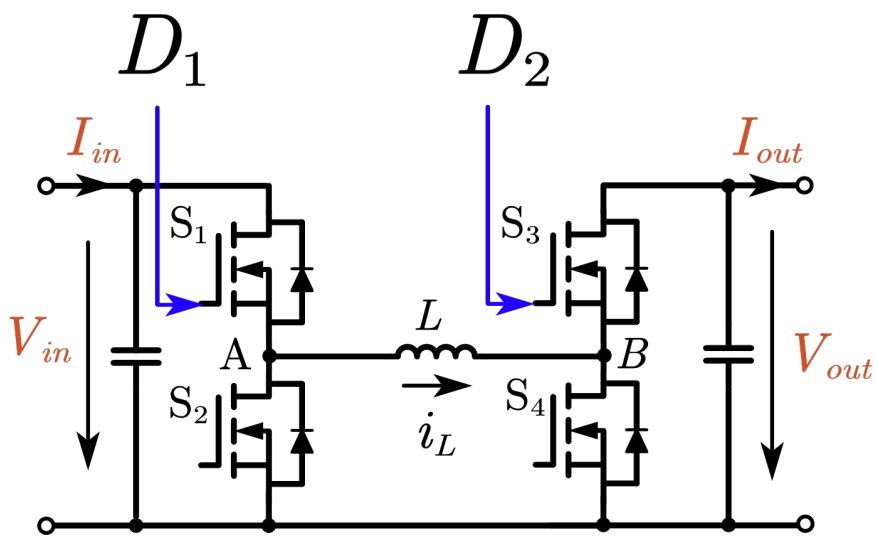


Figure 2.3: Four switch buck-boost converter

2.2.1 Traditional CCM Control of FSBB converter

To reduce the conduction loss, $Diode_1$ and $Diode_2$ shown in Figure 2.1 can be replaced by active switching devices, as depicted in Figure 2.3. Four switch buck-boost converter can be controlled as a traditional buck-boost converter, in this this traditional modulation, both S_1, S_4 has the same duty cycle D, where $D_1 = (1 - D_2) = D$. In traditional CCM modulation, the FSBB converter has two switching states, and the working principle is the same as the two-switch buck-boost converter. The ideal current and voltage waveform is shown in Figure 2.4. In this modulation method, the voltage conversion ratio follows the

same transfer function as the two-switch buck-boost converter as in eq.2.1. In the FSBB

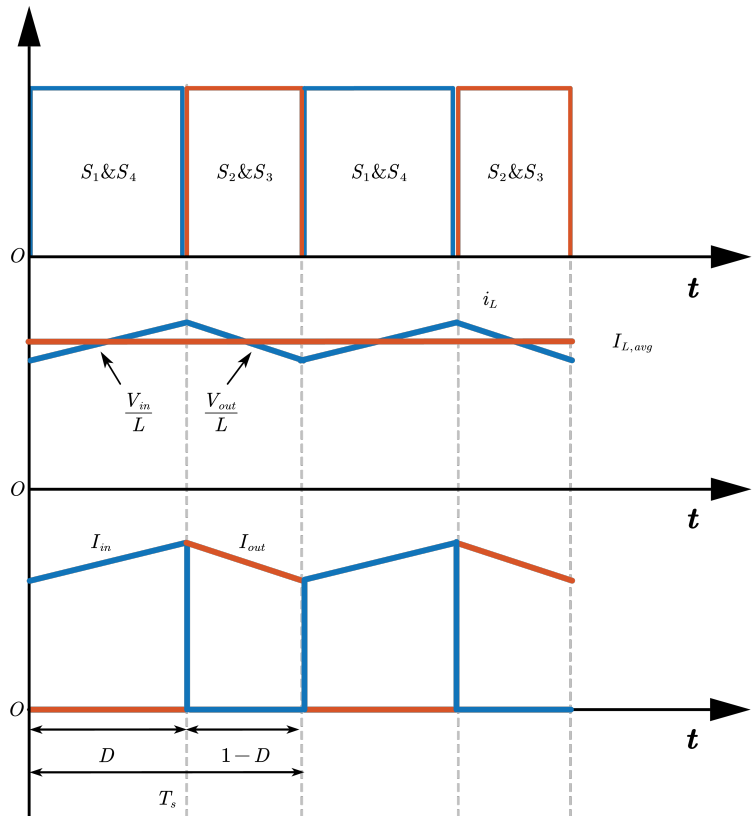


Figure 2.4: Control and current waveform for traditional CCM modulation of FSBB converter

converter under CCM modulation, S_2 and S_3 act as synchronous rectifiers. The complement duty cycle of S_1/S_4 is applied to those switches. The loss of S_2 and S_3 can be calculated as eq.2.3-2.5.

$$P_{srloss} = (1 - D)\left(I_{in} + I_{out}\right)^2 R_{dson} \tag{2.3}$$

$$P_{srloss} = (1 - D)\left(I_{in} + I_{out}\right)^2 R_{dson} \tag{2.4}$$

$$V_{srfwd} = (I_{in} + I_{out}) \times R_{dson} \tag{2.5}$$

Compare eq.2.2 with eq.2.5, the conduction loss is determined by the forward voltage drop. Since the on-resistance of MOSFET is usually very low, the forward voltage drop of the

MOSFET is much smaller than diodes, reducing the conduction loss of the rectifier. As a result, the FSBB converter is more desirable than TSBB, especially in high voltage and high current applications.

2.3 Quadrangle Current Mode Control of FSBB Converter

In order to modulate the FSBB converter, the switching device S_1 and S_2 must have the complement control signal, and the same rule applies to S_3 and S_4. The duty cycle D_1 is applied to S_1 and D_2 is applied to S_3, and as a result the duty cycle applied to S_2 will be $(1 - D_1)$ and duty cycle applied to S_4 will be $(1 - D_2)$. There's another degree of freedom which is the phase shift between D_1 and D_2 denoted as ϕ. The FSBB converter can achieve a total of four switching states. The switching state is shown in Figure 2.6 and a sample of the control signal and current waveform utilizing all four switching states is shown in 2.9, and the switching time $t_1 - t_4$ are labeled in this waveform. The analysis of each switching mode is performed assuming that no ESR and the switching device is ideal. The voltage applied on the inductor during each state is shown in eq.2.6-2.9.

$$V_{L(0-t_1)} = V_{in} \tag{2.6}$$

$$V_{L(t_1-t_2)} = V_{in} - V_{out} \tag{2.7}$$

$$V_{L(t_2-t_3)} = -V_{out} \tag{2.8}$$

$$V_{L(t_3-t_4)} = 0 \tag{2.9}$$

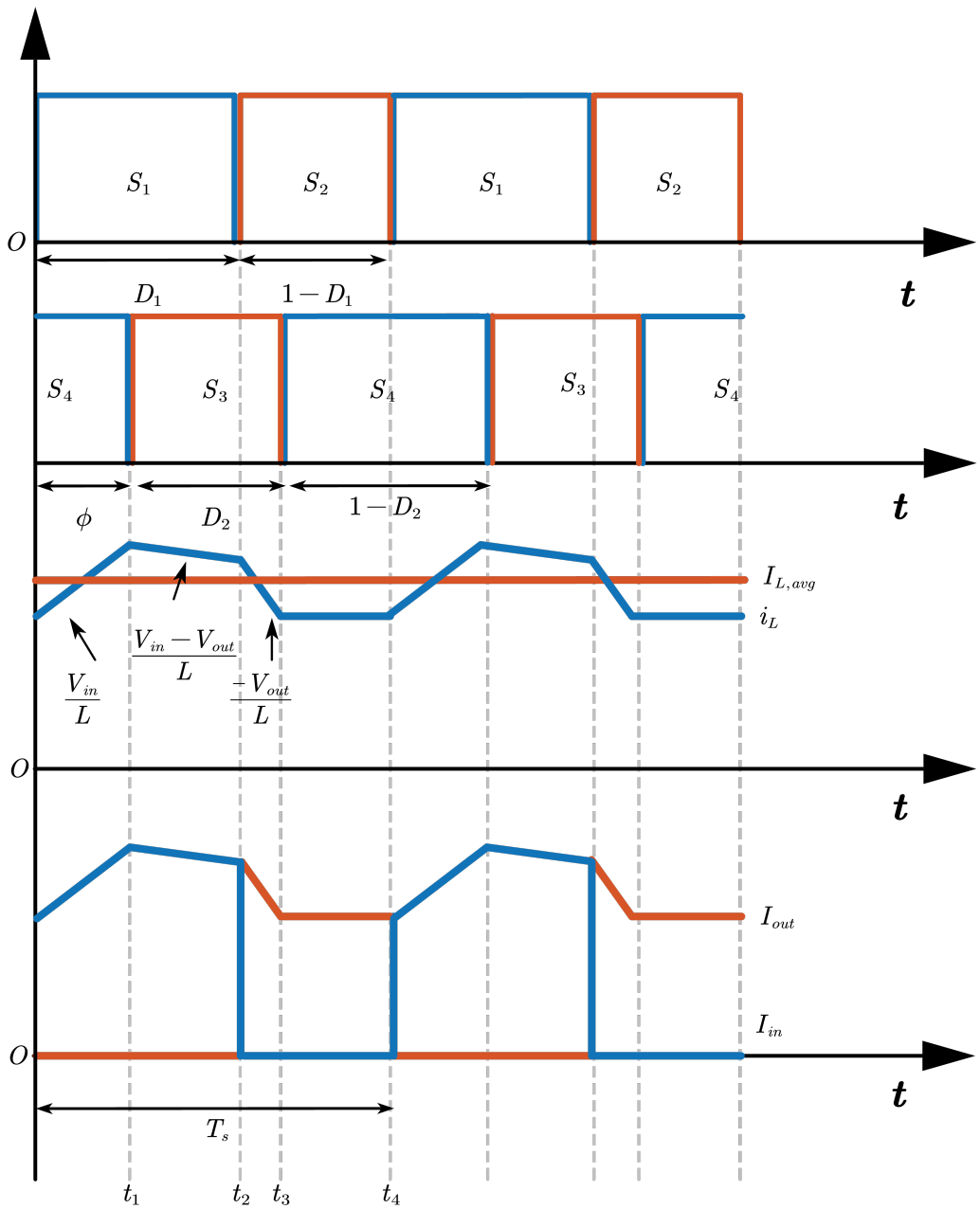


Figure 2.5: FSBB converter waveforms utilizing all four switching states

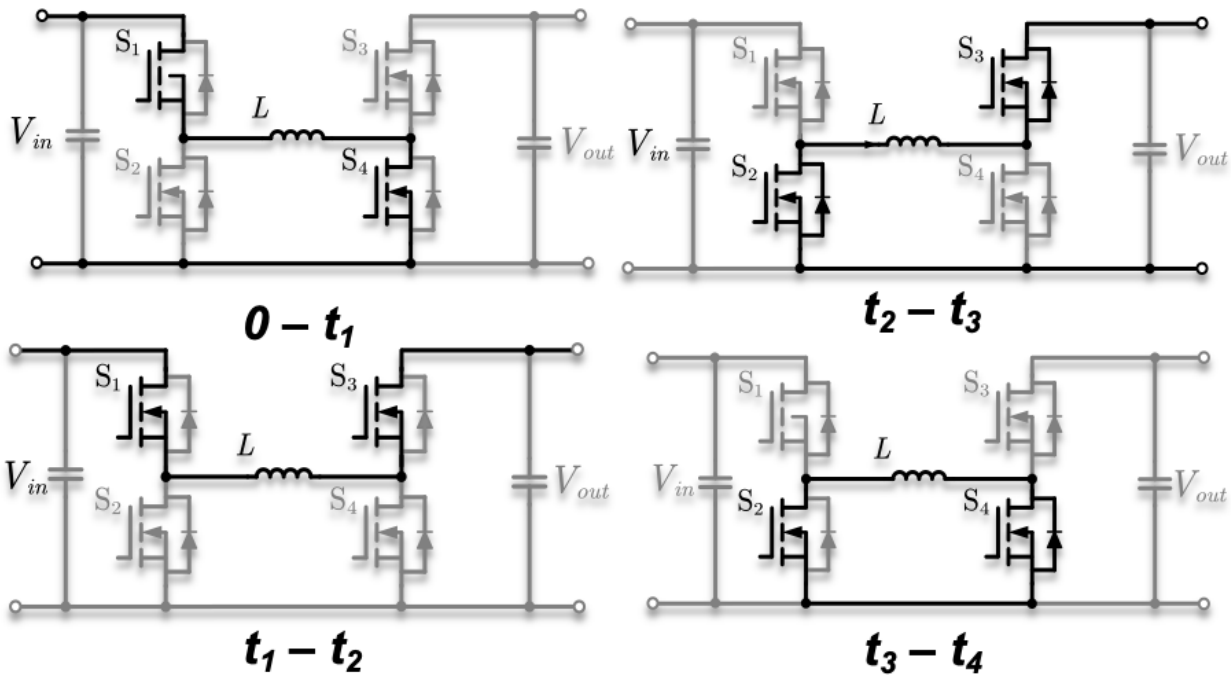


Figure 2.6: Switching states of FSBB converter

2.3.1 Mode 1 $(0 - t_1)$:

During time from 0 to t_1, switching devices S_1 and S_4 are turned on. The inductor L is connected to the input side, and the input voltage is applied to the inductor as described in eq.2.6, therefore the inductor current increases with the rate of $\frac{V_{in}}{L}$, storing energy into the inductor. The output is connected to the output capacitor only, and the output capacitor is discharging and supplying the output load.

2.3.2 Mode 2 $(t_1 - t_2)$:

During the time from t_1 to t_2, switch S_1 and S_3 are turned on and S_2, S_4 are blocking. The inductor is connected to both the input side and the output side. The voltage applied on the inductor can be described as in eq.2.7. The change of inductor current depends on the input and output voltage relationship. If the converter operates in step-down mode, $V_{in} > V_{out}$,

the inductor current in this mode will increase. If the converter operates in step-up mode, $V_{in} < V_{out}$, the inductor current in this mode will decrease. Suppose the converter has a unit gain, $V_{in} = V_{out}$, the inductor current will maintain constant.

2.3.3 Mode 3 ($t_2 - t_3$):

During time from t_2 to t_3, switch S_2 and S_3 are turned on. In this mode, the voltage on the inductor is described by eq.2.8. The energy stored in the inductor is transferred to the load and output capacitor while the inductor current is decreasing at with slope of $\frac{-V_{out}}{L}$. The inductor is only connected to the output side, while the load current is supplied by both the inductor current and the capacitor in this mode.

2.3.4 Mode 4 ($t_3 - t_4$):

During the time from t_3 to t_4, switch S_2 and S_4 are turned on, and the inductor is neither connected to the input nor the output as depicted in eq.2.9. The current is freewheeling between S_2, S_4 and the inductor. In this mode, if ignoring the ESR of the inductor and R_{dson} of the MOSFET, the inductor current will maintain constant.

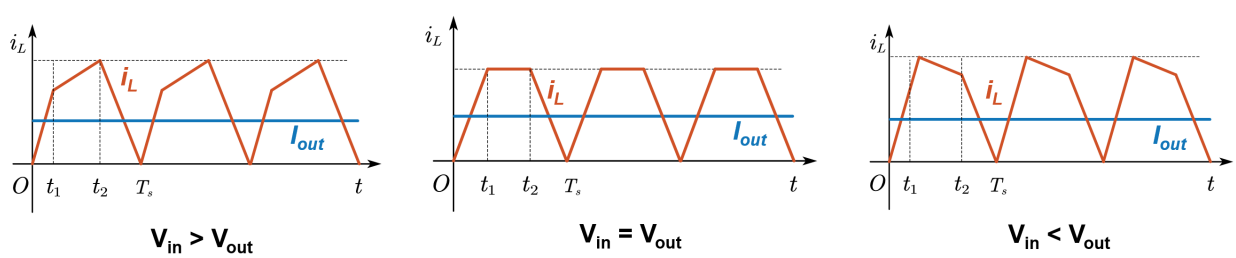


Figure 2.7: Quadrangle current mode inductor current waveform

Suppose the devices switch in the sequence described above. In that case, the inductor current waveform will form a quadrangle shape, as shown in Figure 2.7. Therefore, the modulation method is quadrangle current mode (QCM) modulation.

2.4 Zero Voltage Switching of FSBB Converter in Quadrangle Current Modulation

The FSBB converter can achieve Zero Voltage Switching (ZVS) if the following conditions are met:

1. The sequence of the switching device S_1, S_3, S_2, S_4 is as shown in Figure 2.6.

2. At the time between t_3 and t_4, a negative current flows in the inductor (I_0), and at t_1, t_2, the inductor current is flowing in the positive direction.

3. The deadtime is sufficient to charge the device output capacitance C_{oss}, depending on the current of the inductor and the device's characteristics.

The implementation of ZVS and equivalent circuits of FSBB are shown in Figure 2.9, along with the explanation of how each switching device achieves ZVS[15]. The assumption of ideal MOSFETs, inductors, and capacitors will be used in the following ZVS analysis. An example of inductor current waveform of the FSBB converter under such condition is shown in Figure 2.8

Before time t_1, the converter is in the states shown as in Figure 2.9(b). When at time t_1, S_4 is turned off. During the deadtime, the inductor current charges up the output capacitor of S_4, C_4, and the voltage across the capacitor C_3 decreases, as shown in Figure 2.9(c). After C_3 is depleted, the reverse diode of the MOSFET S_3 will start to conduct, as shown in Figure 2.9(d). When turning on MOSFET S_3, zero voltage switching can be achieved, and the converter will operate as shown in Figure 2.9(e).

At the time t_2, the MOSFET S_1 is first turned off because the inductor current is in the positive direction, C_2, the parasitic capacitor of S_2, is being discharged, as shown in Figure

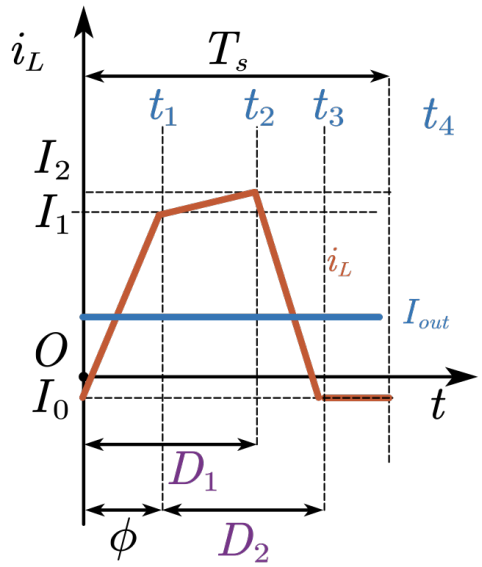


Figure 2.8: Sample inductor current waveform for ZVS analysis

2.9(f). After the C_2 is depleted, the current will conduct through the reverse diode of S_2, and ZVS of S_2 can be achieved.

At the time t_3, the inductor current must be in the reverse direction to achieve ZVS. When the inductor current is flowing in the negative direction, the switching device S_3 is turned off in Figure 2.9(i); during the deadtime, before S_4 turns on, the inductor current discharges C_4, the parasitic capacitor of S_4, until current flows through the reverse diode of S_4 in Figure 2.9(j). Turning on the switching device S_4 when the reverse diode is conducting can achieve ZVS.

At the time t_4, since the inductor current is flowing in the negative direction, when switching device S_3 is turned off, the inductor current will charge up C_2 as shown in Figure 2.9(k). As the voltage of C_2 reaches input voltage, the reverse diode of S_1 will start conducting as illustrated in Figure 2.9(l); therefore, ZVS of S_1 can be achieved.

At the time t_3 and t_4, the amplitude of the inductor I_0 current is relatively small. Therefore

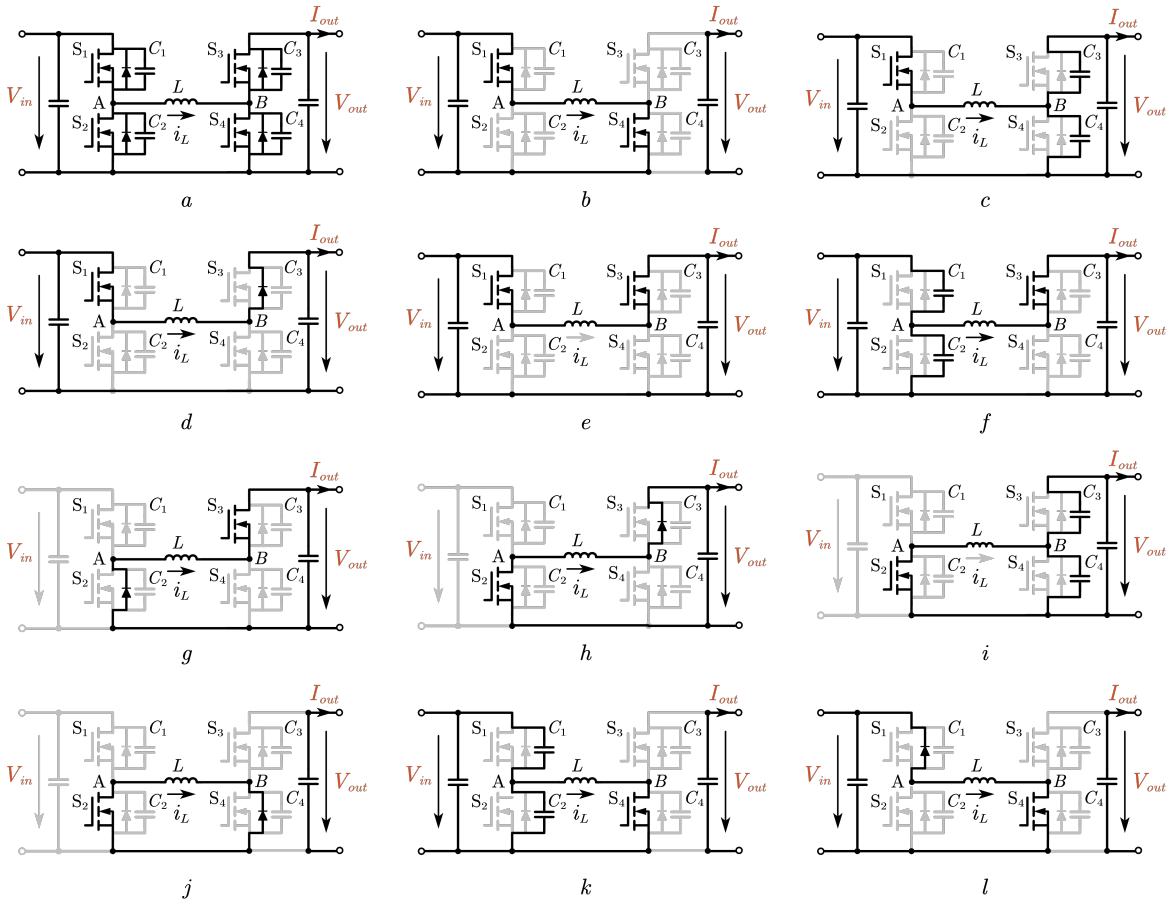


Figure 2.9: Zero voltage switching implementation for FSBB converter

S3 and S4 can be considered to be zero current switching (ZCS).

With the ZVS of all devices and ZCS of 2 devices in the FSBB converter, the switching loss of the devices can be significantly reduced compared to the traditional CCM control method.

2.5 Quadrangle Current Mode Control Method with Reduced Loss

For controlling the FSBB converter, three variables can control input, duty ratioD_1, D_2, and phase shift ϕ. The switching time relationship between t_1, t_2, t_3 and duty cycle D_1, D_2 and phase shift ϕ can be represented in eq.2.10-2.12 :

$$D_1 = \frac{t_2}{T_s} \tag{2.10}$$

$$D_2 = \frac{t_3 - t_1}{T_s} \tag{2.11}$$

$$\phi = \frac{t_1}{T_s} \tag{2.12}$$

The FSBB converter operation point can be defined by the following operation condition V_{in}, V_{out} and the power transfer P_{tr}. Based on the relationship between the inductor current and applied voltage:

$$V_L = L\frac{d_{iL}}{d_t} \tag{2.13}$$

The inductor current waveform in one duty cycle is shown in Figure 2.8 can describe the

relationship between switching time, voltage, and current as eq.2.14-2.16.

$$t_1 = L \times \frac{I_0 + I_1}{V_{in}} \tag{2.14}$$

$$t_2 - t_1 = L \times \frac{I_2 - I_1}{V_{in} - V_{out}} \tag{2.15}$$

$$t_3 - t_2 = L \times \frac{I_0 - I_2}{V_{out}} \tag{2.16}$$

Where t_1, t_2, t_3 are the time that device S3, S2, S4 turn on, I_1, I_2 are the inductor currents at the time t_1, t_2 turn on; and I_0 is the negative inductor current at t_3, t_4. The Inductor current I_1, I_2 can be derived with eq.2.17-2.18.

$$I_1 = \frac{T_s\, V_{in}\, \phi}{L} - I_0 \tag{2.17}$$

$$I_2 = \frac{T_s\, V_{in}\, \phi}{L} - I_0 + \frac{T_s\, (V_{in} - V_{out})\, (D_1 - \phi)}{L} \tag{2.18}$$

Also, the power of the converter at a steady state at the specific operating point can be calculated with the eq.2.19[16]:

$$P_{tr} = \frac{V_{in}}{2T_s}((I_1 + I_2) \times t_2 - (I_0 + I_2) \times t_1) \tag{2.19}$$

The large-signal transfer function of the FSBB converter can be obtained:

$$\frac{V_{out}}{V_{in}} = \frac{D_1}{D_2} \tag{2.20}$$

By inspecting eq.2.20, the voltage conversion ratio is defined by the ratio of D_1 and D_2. By analyzing eq.2.19 and eq.2.20, for any specific operation point of the FSBB converter, there are three control variables D_1, D_2, ϕ, and there are two control targets V_{out} and P_{tr}, which

means that for any specific operation point, there are multiple combinations of the control variable that can satisfy both control targets. An example of an inductor current waveform is shown in Figure 2.10.

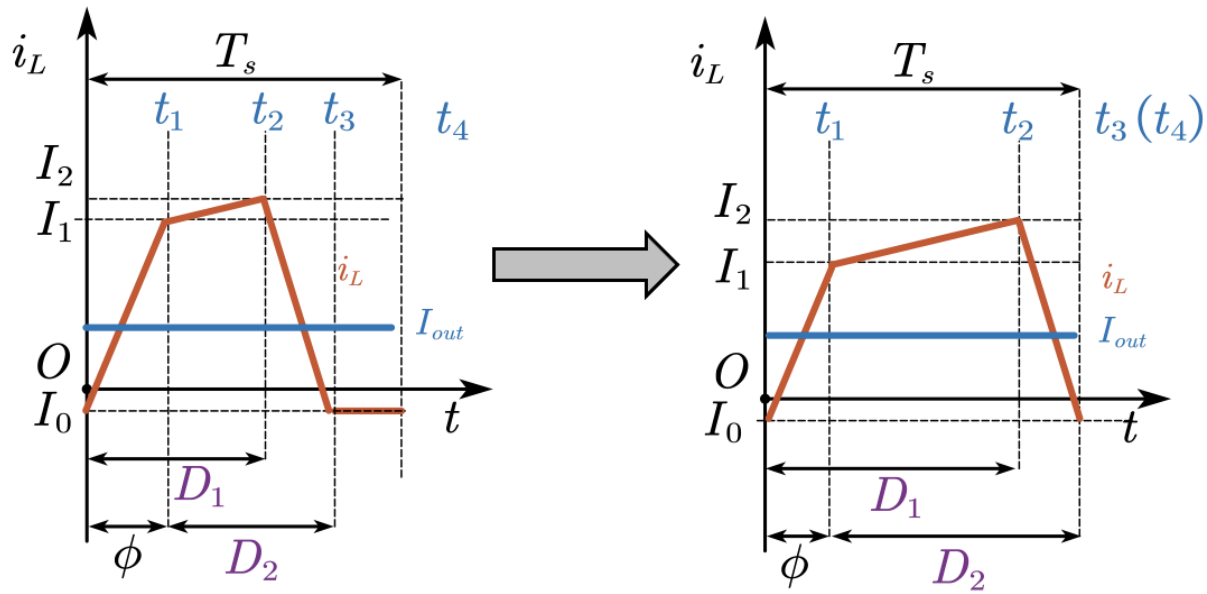


Figure 2.10: Inductor current waveform with same operation point

Comparing Figure 2.10(a) with Figure 2.10(b), although two sets of the control variables are different, the voltage conversion ratio $\frac{V_{in}}{V_{out}}$ is the same, and the average inductor current I_{out} is also the same. But the peak inductor current I_1, I_2 of Figure 2.10(a) is higher than Figure 2.10(b). Also, the RMS current of Figure 2.10(a) is higher than Figure 2.10(b).

Since the turn-off loss of the switching devices S_4, S_1 is directly related to the current passing through the device at the time of turning off I_1, I_2. Therefore the switching pattern of Figure 2.10(b) is more desirable. Nevertheless, the inductor current of Figure 2.10(b) has a lower RMS value; therefore, the conduction loss of the inductor and core loss of the inductor is lower if the switching combination shown in Figure 2.10(b) is implemented.

In order to find the optimized efficiency switching pattern, both the ZVS requirements and reducing inductor RMS current reduction conditions should be met. By implementing both requirements, an unique optimal switching parameter at any operation point can be found.

2.6 Real-time Calculation of Quadrangle Mode Control (Min-RMS ZVS Block)

To achieve real-time control of the FSBB converter that will ensure the converter has minimum RMS current while maintaining the ZVS condition of all switches, the function that can calculate switching parameters based on the current operation point is necessary to be derived. This function block is named Min-RMS ZVS block. The method of minimizing the inductor current under QCM control of FSBB converter was first introduced in[16]. In step down operation, when $t_3 = t_4$ and $t_1 = 0$, the converter is operates in marginal power state (Figure 2.11(b)). Eq.2.21 shows the power transfer of the converter that operates in marginal power mode, based on the input voltage, output voltage, and inductor inductance.

$$P_{margin,step-down} = \frac{T_s {V_{out}}^2 (V_{in} - V_{out})}{2LV_{in}} \tag{2.21}$$

Similarly, when the converter operates in step-up mode, the marginal power can be calculated when $t_2 = t_3 = t_4$. The marginal power of the converter operating in step-up mode can be calculated as eq.2.22.

$$P_{margin,step-up} = \frac{-2I_0 LV_{in}V_{out} + T_s {V_{in}}^2 V_{out} - T_s {V_{in}}^3}{2LV_{out}} \tag{2.22}$$

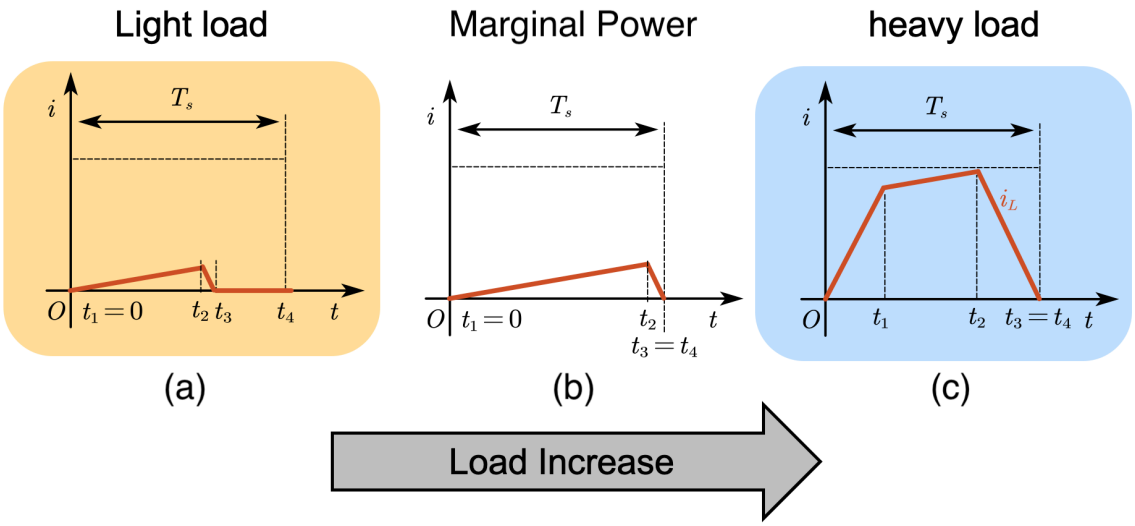


Figure 2.11: Inductor current waveform under different load

Also, the boundary current $I_{out,boundary}$, which is the load current when the converter operates in marginal power mode can be calculated by eq.2.23

$$I_{out,boundary} = \frac{P_{margin}}{V_{out}} \tag{2.23}$$

In order to derive the Min-RMS ZVS block, the converter operation can be divided into four operating regions. Based on the converter input and output voltage ratio, the converter can be divided into a step-up operation region and a step-down operation region. Based on the power transfer, if the power delivered is lower than the marginal power for the input voltage, the converter is operated in light load mode; if the power exceeds marginal power, the converter operates in the heavy load region. Figure 2.12 show the four converter operation regions under input voltage $V_{in} = 900\,V$ and the inductor $L = 33.5\,\mu H$. For each operation region, the analytical solution of D_1, D_2, ϕ has been derived. The result of the step-up heavy-load region and step-down heavy-load region is the same. Therefore the Min-RMS ZVS block can be illustrated as in Figure 2.13. And the analytical solution in each region

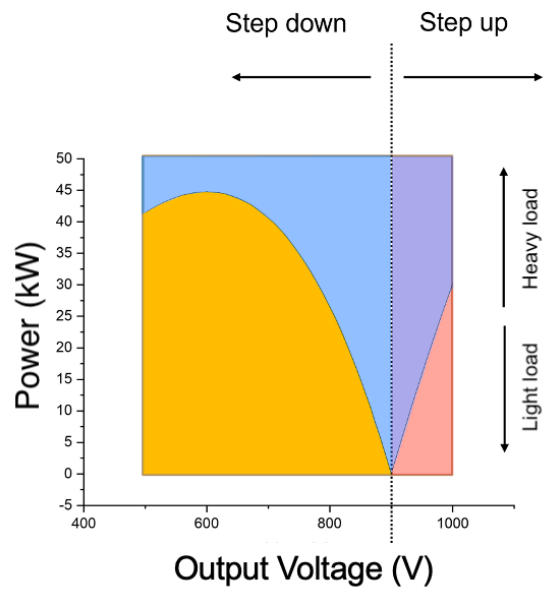


Figure 2.12: Four operation regions of FSBB converter with minimized RMS inductor current

for D_1, D_2, and ϕ are shown in eq.2.24-2.32. For both step-up heavy-load and step-down

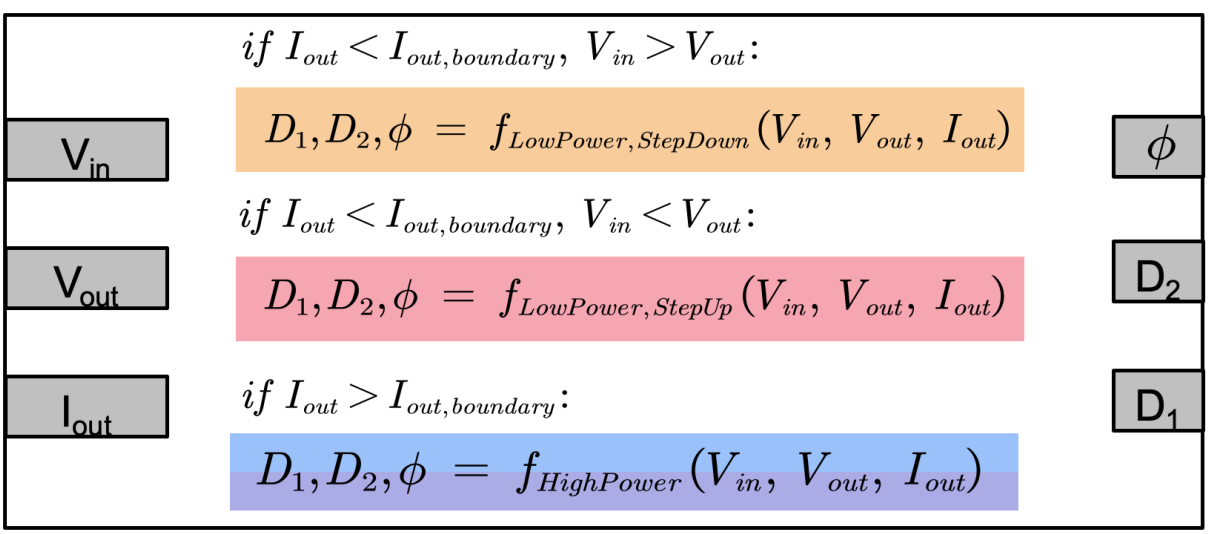


Figure 2.13: Min RMS ZVS block

heavy-load regions:

$$D_1 = \frac{T_s V_{in} V_{out}(V_{in} + V_{out}) - \sqrt{T_s V_{in} {V_{out}}^2 \left(T_s {V_{in}}^2 V_{out} - 2 I_{out} L \left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)\right)}}{V_{in}\left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)} \tag{2.24}$$

$$D_2 = \frac{T_s V_{in} V_{out}(V_{in} + V_{out}) - \sqrt{T_s V_{in} {V_{out}}^2 \left(T_s {V_{in}}^2 V_{out} - 2 I_{out} L \left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)\right)}}{V_{out}\left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)} \tag{2.25}$$

$$\phi = \frac{\sqrt{T_s V_{in} {V_{out}}^2 \left(T_s {V_{in}}^2 V_{out} - 2 I_{out} L \left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)\right)} + T_s {V_{out}}^3}{V_{out}\left({V_{in}}^2 + V_{in} V_{out} + {V_{out}}^2\right)} \tag{2.26}$$

For step-down light-load region:

$$D_1 = \frac{\sqrt{2}\sqrt{L}\sqrt{T_s}\sqrt{I_{out} V_{out}}}{\sqrt{V_{in}(V_{in} - V_{out})}} \tag{2.27}$$

$$D_2 = \frac{\sqrt{2 L T_s} I_{out} V_{in}}{\sqrt{I_{out} V_{out}}\sqrt{V_{in}(V_{in} - V_{out})}} \tag{2.28}$$

$$\phi = 0 \tag{2.29}$$

For step-up light load region:

$$D_1 = \frac{\sqrt{2}\sqrt{L}\sqrt{T_s}\sqrt{V_{out}}\sqrt{I_{out} V_{out}}}{\sqrt{{V_{in}}^2 (V_{out} - V_{in})}} \tag{2.30}$$

$$D_2 = \frac{\sqrt{2}\sqrt{L}\sqrt{T_s} V_{in}\sqrt{I_{out} V_{out}}}{\sqrt{V_{out}}\sqrt{{V_{in}}^2 (V_{out} - V_{in})}} \tag{2.31}$$

$$\phi = \frac{\sqrt{2}\sqrt{L}\sqrt{T_s}\sqrt{I_{out} V_{out}}\sqrt{{V_{in}}^2 (V_{out} - V_{in})}}{{V_{in}}^2\sqrt{V_{out}}} \tag{2.32}$$

2.6.1 FSBB Inductor Design of FSBB

According to the FSBB QCM operation the ZVS requirement depends on the inductor inductance L, operation voltage V_{in}, V_{out}, switching frequency f_{sw}, and power transfer P_{tr}. The maximum inductor inductance that allows the converter to operate in QCM mode while maintaining ZVS conditions for all converter desired operation points has been calculated. Figure 2.14 shows the simulation result. and Table.2.1 is the simulation sweep condition. The MATLAB program for generating table is attached in Appendix A.

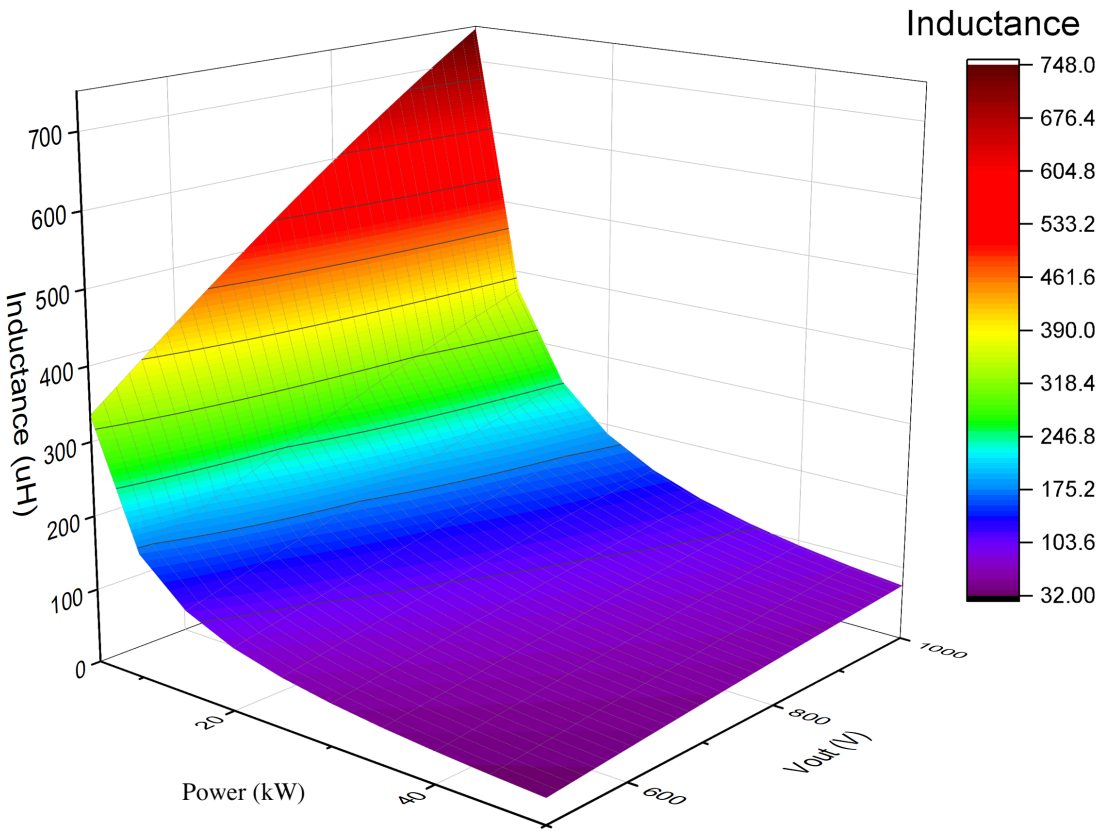


Figure 2.14: Maximum inductance allowed for ZVS

Table 2.1: FSBB inductor sweep condition

Parameter	Value
V_{in}	$900\,V$
V_{out}	$500\,V$ - $1\,kV$
P_{tr}	$0 - 50\,kW$
F_{sw}	$20\,kHz$

Simulation parameter for maximum inductor value plot According to the simulation result in Figure 2.14 , the Maximum inductance value L decrease as the power transfer P_{tr} increases, and the Maximum inductance L decreases as the output voltage V_{out} increases. To ensure the FSBB converter can achieve ZVS in all designed operation regions, the minimum value appears when the input voltage $V_{in} = 500\,V$ and $P_{tr} = 50\,kW$. The inductance selected $L = 33.5\,\mu H$. The inductor design of the converter unit is explained in [17].

2.7 Open-Loop Verification of Min-RMS Block

In order to verify the min-RMS ZVS block, Simulation was performed and a hardware platform was built[18][19]. The simulated waveforms are shown in Figure 2.16, 2.18, 2.20. The testing circuit diagram is shown in Figure 2.15. The input voltage V_{in} and output voltage V_{out} were measured with THDP0200 high voltage differential probe, and the inductor current i_L were measured with TCP303 DC current probe. The testing condition and results for three tests have been summarized in Table 2.2.

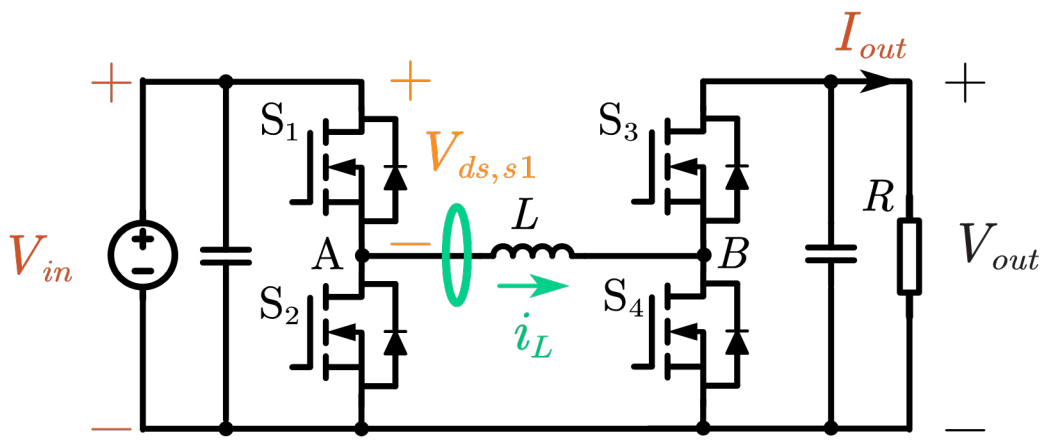


Figure 2.15: Min RMS ZVS block testing circuit diagram

Table 2.2: Min RMS ZVS testing condition and result

	Experiment 1	Experiment 2	Experiment 3
	Testing Condition		
Voltage conversion	Step Down	Step Up	Unit Gain
Operation region	Light load	Heavy load	Heavy load
Input Voltage(V_{in})	$150\,V$	$150\,V$	$150\,V$
Reference Output Voltage(V_{out})	$100\,V$	$200\,V$	$150\,V$
Load resistance (R)	$10\,\Omega$	$10\,\Omega$	$10\,\Omega$
Inductor Inductance (L)	$33.5\,\mu H$	$33.5\,\mu H$	$33.5\,\mu H$
	Expected Value (Simulation)		
Output Voltage (V_{out})	$100\,V$	$200\,V$	$150\,V$
Peak Current ($I_{L,Max}$)	$25\,A$	$50\,A$	$22\,A$
Duty Cycle 1 (D_1)	37%	23%	18%
	Testing Result (Hardware)		
Output Voltage(V_{out})	$94.1\,V$	$199.5\,V$	$154.2\,V$
Peak Current($I_{L,Max}$)	$23\,A$	$49\,A$	$25\,A$
Duty Cycle 1 (D_1)	36.6%	24%	20%

The Min RMS ZVS block is implemented in C language inside Xilinx Zynq SoC. The C program of Min RMS ZVS block function is attached in Appendix B.

For the following tests, the input voltage of the converter $V_{in} = 150\,V$, and the output load resistor $R = 10\,\Omega$. The output current I_{out} used for Min RMS ZVS calculation is calculated with reference V_{out} and R, where $I_{out} = \frac{V_{in}}{R}$.

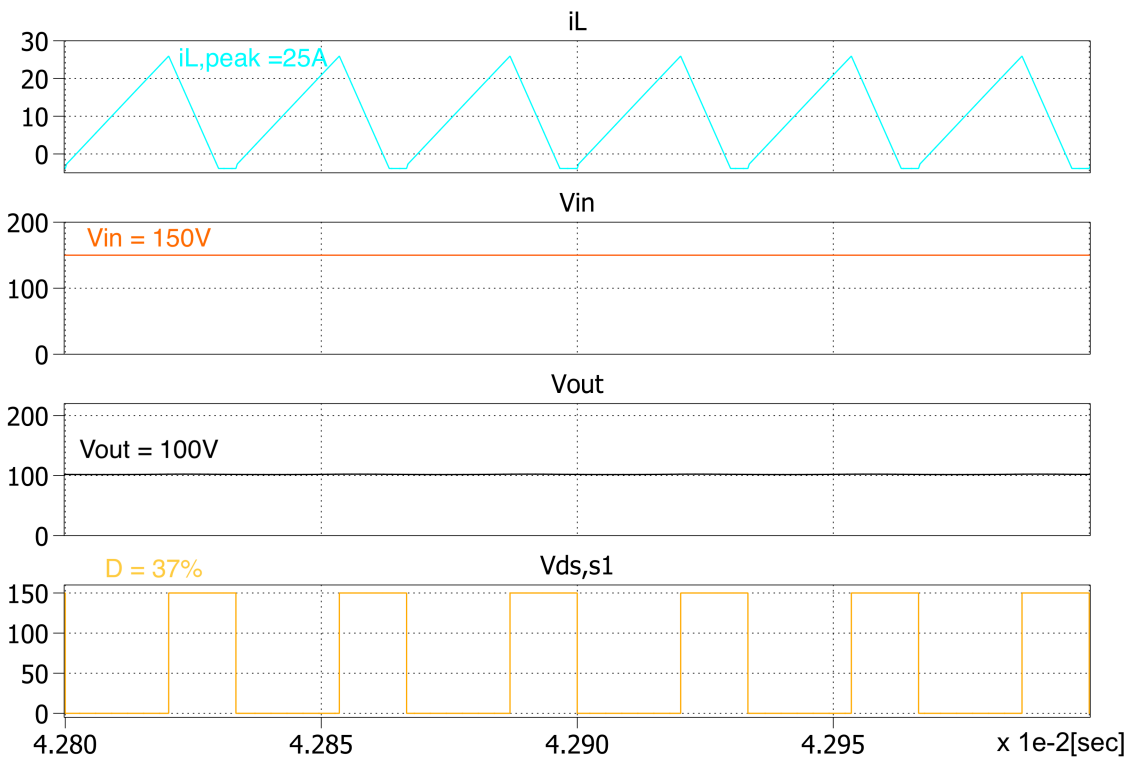


Figure 2.16: Simulation waveform of Min RMS ZVS block in step-down light load operation

Figure 2.19, 2.19, 2.21 shows the hardware testing result of the Min RMS ZVS block working in step-down light load($V_{out} = 100\,V$), step-up heavy load ($V_{out} = 200\,V$), and unit gain ($V_{out} = 150\,V$) cases. In all test cases, channel 8 (C8) is the inductor current waveform, and channel 5 (C5) shows the drain-source voltage of MOSFET S_1 (V_{ds,S_1}). From the testing result, the inductor current becomes negative in each switching period when S1 is turned on (falling edge of V_{ds,S_1}), which satisfies the ZVS requirement for all switching devices. In

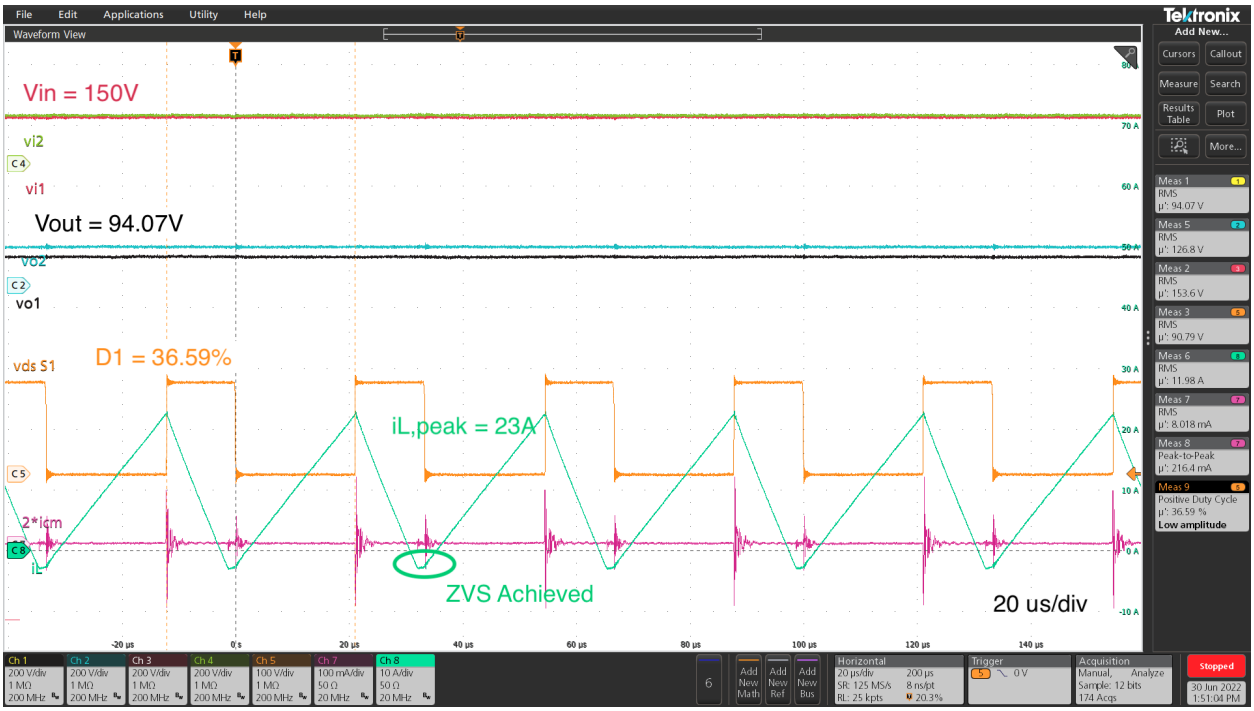


Figure 2.17: Hardware Min RMS ZVS block in step down light load operation waveform

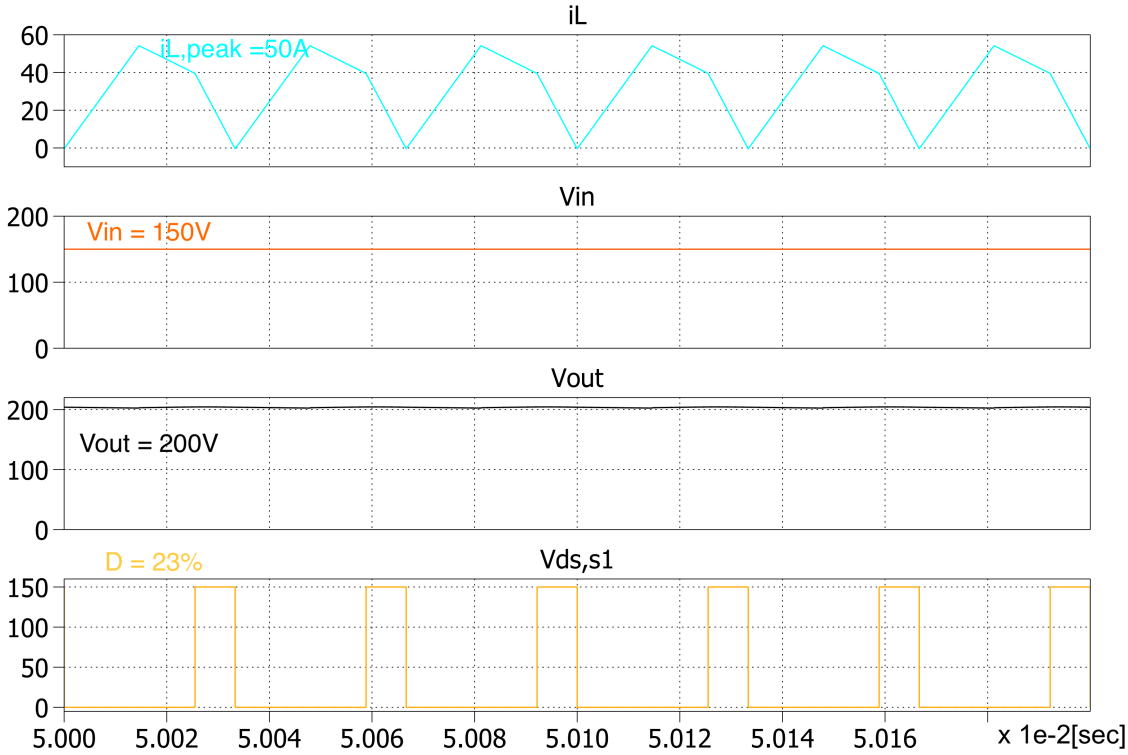


Figure 2.18: Simulation waveform of Min RMS ZVS block in step-up heavy load operation

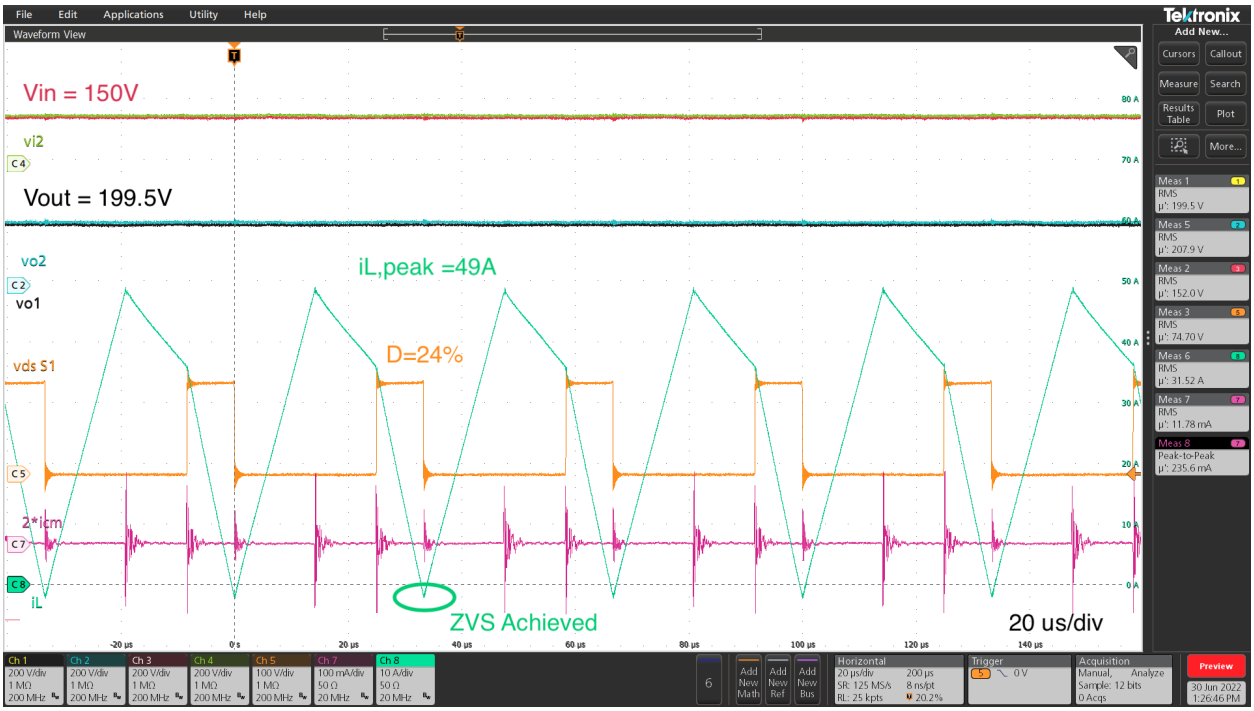


Figure 2.19: Hardware Min RMS ZVS block in step-up light load operation waveform

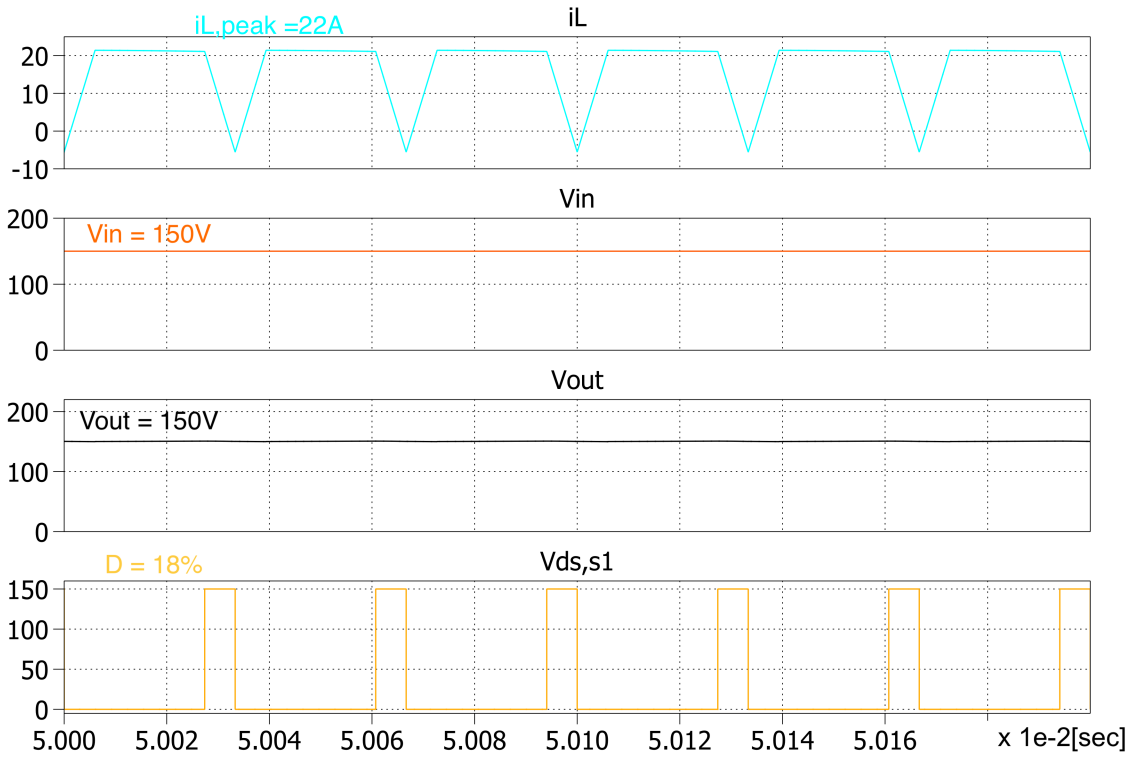


Figure 2.20: Simulation waveform of Min RMS ZVS block in unit gain heavy load operation

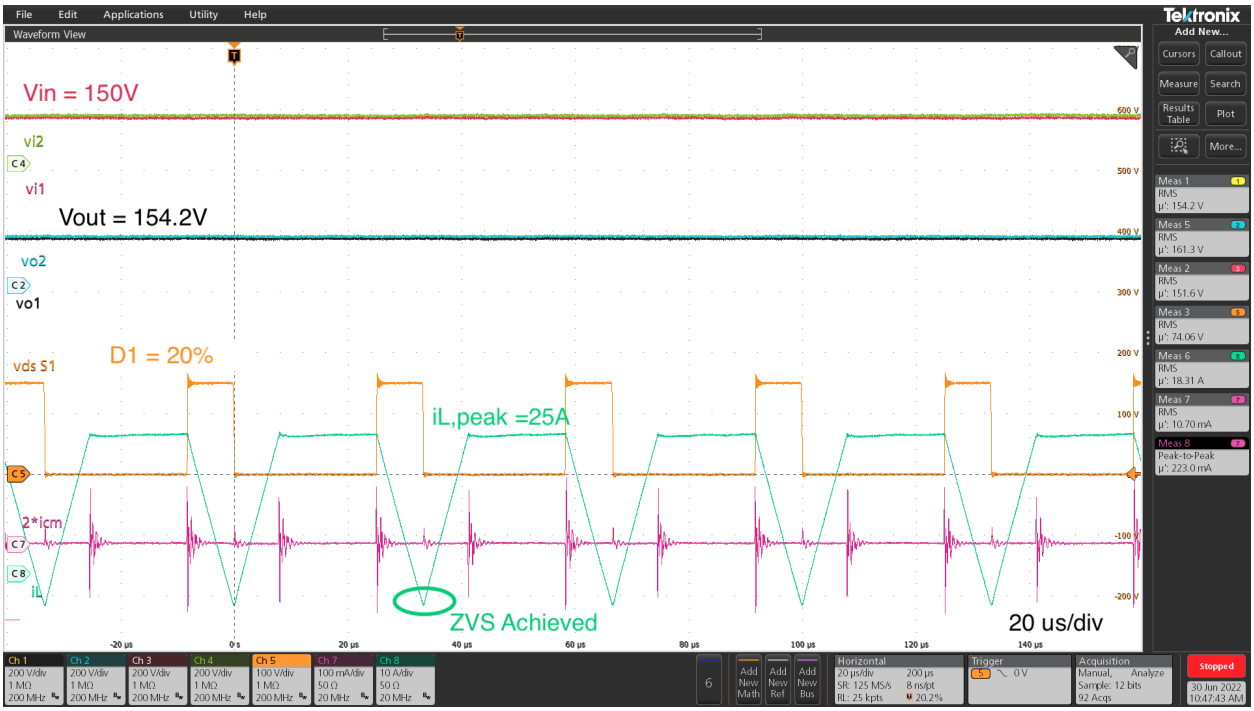


Figure 2.21: Hardware Min RMS ZVS block in step down heavy load operation waveform

all tests, the min-RMS ZVS block was provided with the desired V_{in}, V_{out}, $I_{out}(\frac{V_{in}}{R})$, and the calculated switching parameter were used to control the switching devices. Observing the output voltage, V_{out} matches the desired reference voltage used for calculation. Also, compare inductor current waveforms and the $V_{ds,s1}$ waveforms from the simulation and the hardware testing result, the two waveforms shows agreement between each other. Therefore the Min-RMS ZVS block open loop operation point calculation has been verified.

Chapter 3

SiC Gate Driver Design

3.1 Gate Driver Design of SiC MOSFET Half-bridge Modules.

With the demand for higher power density, higher efficiency, and higher operation voltage, Silicon carbide (SiC) MOSFET has gained more popularity because SiC MOSFET has the characteristic of high blocking voltage, low on-resistance, and low output capacitance (C_{oss}), and fast switching characteristic (high dv/dt). But those characteristics create challenges for gate driving circuit design, specifically for the protection circuit design and EMI/ EMC of the signal processing circuits design. Also, with the development of the integrated circuits industry, more and more functionality can be integrated into the gate driver circuits board without increasing the board's footprint. Specifically, the integrated sensor of the voltage and current sensors on the gate driver board can significantly reduce the number of external sensors required, which can substantially increase the converter's power density.

3.2 Overview of Gate Driver Features

The main feature of the gate driver circuit is to control the gate signal. For microgrid applications, the converter's reliability is crucial. Therefore an online switching device health monitoring feature that can detect MOSFET degradation in the early stage and send this

information out for the maintenance request is highly desired. The faulty device can be replaced without any power interruption. The switching device health monitoring is achieved by sensing the device's on-state voltage V_{ds-on} and the device's on-state current I_{device}. With that information, the device's on-state resistance R_{ds-on} can be calculated, and the change of R_{ds-on} over an extended period of time can be used to indicate MOSFET health status.

The gate driver system block diagram is shown in Figure 3.1 [20].

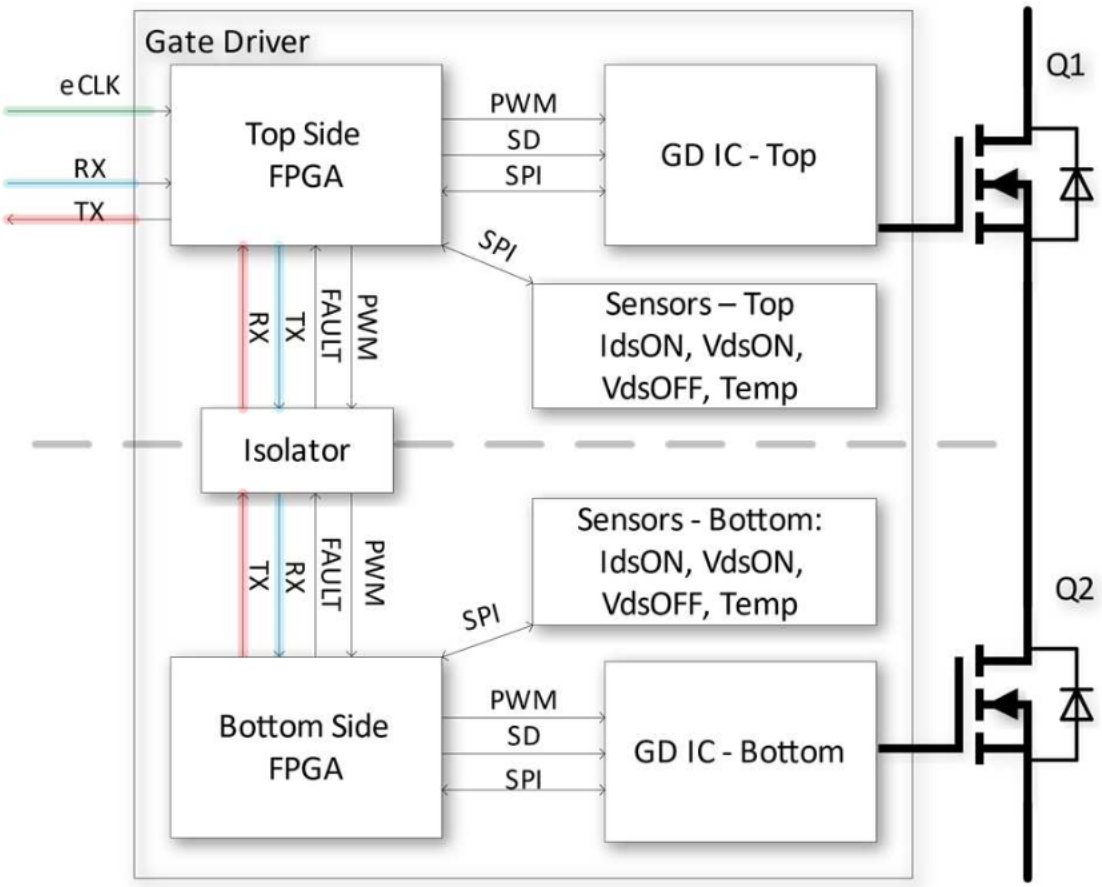


Figure 3.1: Gate driver function blcok diagram

Each gate driver board is divided into two parts, and each part is dedicated to controlling one swtiching MOSFET of the converter. The top and bottom side of the gate driver FPGA

is communicated through a digital isolator chip, which has two communication channels in each direction. On each side of the gate driver, embedded sensors are implemented, such as on-state voltage measurement off state voltage measurement, and devices' on-state current measurements. The detailed circuit implementation will be discussed in this chapter.

3.2.1 Gate Driving Function

On each side of the gate driver, a gate driver control chip (GDIC) is implemented. Since during the design of gate drivers, there's a limited selection of GDIC is commercially available. The GDIC STGAP1AS, designed for N-channel silicon MOSFETs and IGBTs, was selected because the comprehensive protection functions such as the Miller clamp, V_{ds} based current sensing detection, and dedicated sense pin for overcurrent detection that can be used for Rogowski coil sensor implementation are integrated. Both top and bottom side gate-driving PWM signal is generated inside the top side GDIC and sent to the top side GDIC directly. The bottom side PWM signal is sent from FPGA to the bottom GDIC through a digital isolator to the bottom side FPGA and then sent to the bottom side GDIC. Because of the longer signal transmission path of the bottom PWM signal, propagation delay must be considered. Therefore compensation for propagation delay has been added to GD FPGA to achieve top and bottom side gate signal synchronization. The gate driving current capability of this GDIC chip is rated at $5\,A$.

But since the SiC MOSFET has a much faster turn-on and turn-off capability, the maximum GDIC output current is insufficient for SiC MOSFETs. A current booster stage was added to the gate driver between the output of the GDIC and the device Gate. For each MOSFET, three parallel current booster IC, which each can boost the current up to $10\,A$, are implemented, providing a total of $30\,A$ maximum gate current. The GDIC has an SPI communication channel that is connected to the FPGA. During the start-up sequence

of the gate driver, the FPGA programs the configurable registers inside the GDIC. This includes enabling GDIC output, enabling the GDIC protection functions, setting the protection threshold for V_{ds} based current sensing protection, and setting the negative output voltage to $-5\,V$ during device turn-off. Also, suppose the GDIC has a fault triggered, utilizing the SPI communication channel. In that case, the FPGA is capable of reading out the fault type triggered by the protection by reading out the fault code latching registers.

3.2.2 Power Topology of the Gate Driver

Besides the high gate current required for turning on and off, the SiC MOSFET, with its fast switching characteristic, significantly increases the switching noise due to the high rate of voltage change dv/dt and current change di/dt. This high rate of change creates EMI noises during switching, and even with the low parasitic capacitance of the gate driver components, the common mode (CM) can still create malfunction of gate driver circuits and cause improper gating signal and device failure. Therefore the gate driver power topology puts special consideration into minimizing the effect of CM noise. The gate driver power and

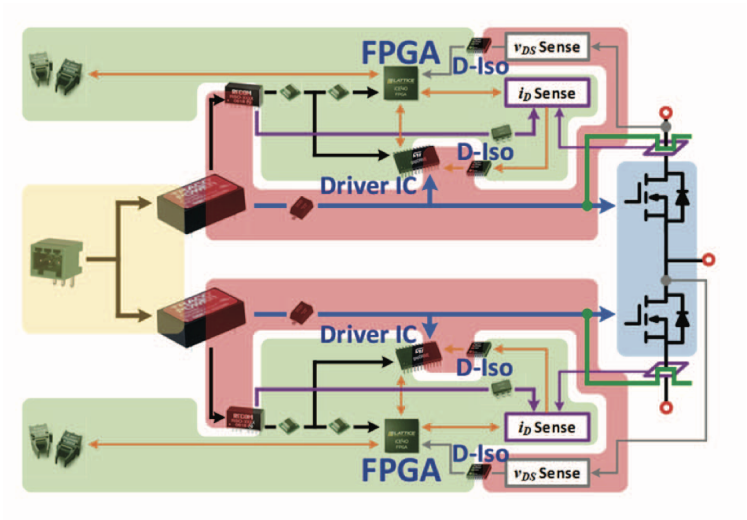


Figure 3.2: Power and ground topology of gate driver design

ground topology are shown in Figure 3.2. On each gate driver, there are three main types of ground, isolated high power ground, input power ground, and sensitive signal ground. The isolated power ground and the signal ground are implemented separately and symmetrically for each side of the gate driver. The Gate driver PCB board grounding layout design is shown in Figure 3.3, where sensitive digital signal ground is depicted in green and isolated high power ground is shown in red.

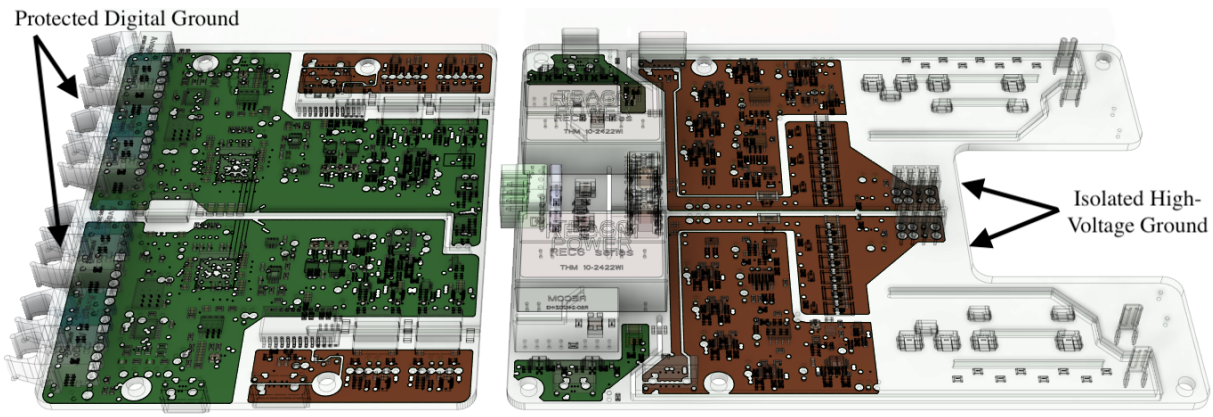


Figure 3.3: Gate Driver Board Grounding Layout

Input Ground

The input ground is represented in yellow in Figure 3.2. Both the top and bottom sides of the gate driver share the same input ground. This ground is only connected to two isolated power supply modules THM 10-4822, each supplying the $+20\,V$ and $-4\,V$ for the isolated ground of each side of the gate driver.

Isolated Power Ground

The red ground is the isolated power ground, which is directly connected to the kelvin source of the controlled SiC MOSFET. Therefore, components, such as GDIC high power side, on-state voltage, and off-state voltage sensors that require electrical connections to power MOSFET, are implemented on this ground. The data collected from the sensors located on

the isolated power ground is sent to FPGA on the signal ground via digital isolators with SPI communication protocol.

Protected Sensitive Signal Ground

The green ground is the protected ground. Sensitive components such as signal processing circuits for Rogowski coil sensors, low power side of GDIC, FPGA, and fiber optic communication interfaces are located on this ground. The on this ground, the power is supplied from the isolated ground with an isolated power supply module RS2409D, providing $\pm 5\,V$. A non-isolated $5\,V$ to $3.3\,V$ power supply is located to provide $3.3\,V$ for the FPGA.[21]

3.3 Drain-Source Voltage based Current Protection

3.3.1 Protection Overview

The Rogowski coil current sensors and Drain-Source Voltage based Current sensing protection in short circuit event has been compared in [22] . For SiC MOSFETs, both V_{ds} based current sensing protection and the Rogowski coil protection method can effectively protect the switching devices. Still, Rogowski-coil protection has a faster response time, reducing the overall energy dissipation during short circuit faults. Nevertheless, the Rogowski coil sensors directly sense the device current instead of device V_{ds}, which depends on the device's operating temperature.

For the designed gate driver, both V_{ds} based current sensing protection and the Rogowski coil current sensor based protection has been implemented. Each protection method can be individually enable and disable by programming the gate driver IC. For continuouse operation, both protection method are enabled and set to same protection current threashold, ensuring the switching device is protected from overcurrent. For evaluation of each protection,

only the protection method under test were enabled.The operation principle and performance of the V_{ds} based current sensing protection will be discussed in this subsection and the Rogowski coil based protection will be discussed in next subsection.

3.3.2 Operation Principle of Drain-Source Voltage based Current Protection

The V_{ds} based current sensing protection circuit was designed as shown in Figure 3.4. The V_{ds}

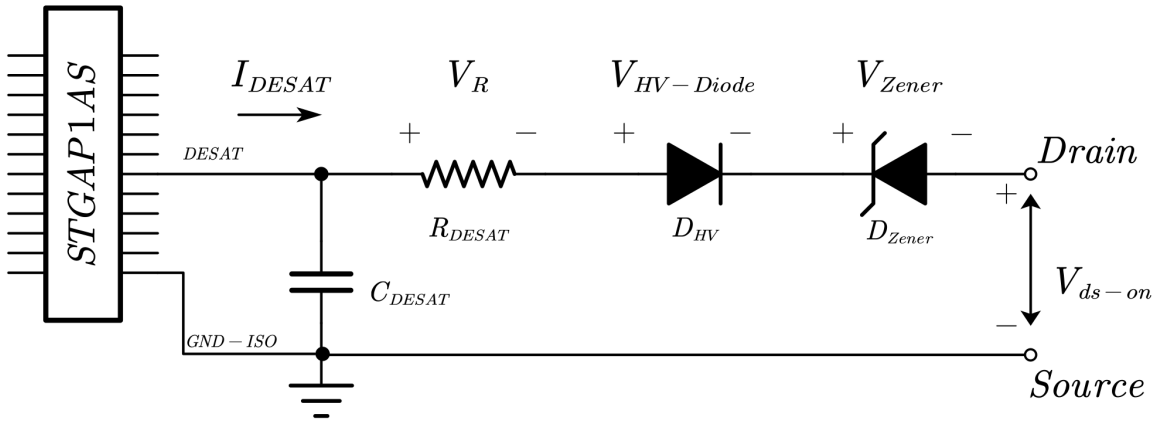


Figure 3.4: V_{ds} based current sensing protection circuits

based current sensing protection circuits include four passive components, A Zener diode, a high voltage diode, a resistor, and a capacitor. The SC Fault pin is connected to the de-sat pin on the gate driver IC STGAP1AS. Since the GDIC was designed for IGBT switching devices, this pin was used for de-sat protections, which functions similarly as V_{ds} based current sensing. When the power MOSFET is turned off, the high voltage diode will block the high voltage potential between drain and source, protecting the gate driver IC from damage from high voltage. In this state, the detection current from GDIC is blocked internally, $I_{DESAT} = 0\,A$. When power MOSFET is turned on, the GDIC protection first enters a blanking

time. This blanking time has a typical value of $250\,ns$. The detection current I_{DESAT} was programmed to be $500\,\mu A$ during gate driver start-up, together with the threshold voltage $V_{fault,th} = 9\,V$. After the blanking time, if the de-sat pin voltage V_{fault} exceeds the threshold voltage, the fault will be latched into the GDIC register, and the gate signal will be turned off.

3.3.3 Design of V_{ds} based Current Sensing Circuits

Assuming the power MOSFET has a drain-source current I_{device}, the drain-source voltage V_{ds} can be estimated with eq.3.1.

$$V_{ds} = R_{ds-on} \times I_{device} \tag{3.1}$$

The de-sat pin voltageV_{fault} can be calculated with eq.3.2.

$$V_{fault} = I_{device} * R_{ds-on} + V_{zener} + V_{HV-diode} \ + R_{desat} * I_{DESAT} \tag{3.2}$$

The detection resistor R_{de-sat} can be calculated with eq.3.3.

$$R_{desat} = \frac{V_{fault,th} - V_{ds} - V_{zener} - V_{HV-diode}}{I_{DESAT}} \tag{3.3}$$

The selected components' part numbers and related ratings are shown in Table.3.1

Table 3.1: Component selection and rating for V_{ds} based current sensing protection

Component	Parts Number	Rating
Power MOSFET	GE12047CCA3	$R_{ds-on} = 4.4\,m\Omega$
HV diode	STTH112A	$V_{HV-diode} = 1.0\,V$ @$250\,\mu A$
Zener diode	1SMA5913BT3	$V_{zener} = 1.0\,V$ @$250\,\mu A$

With the parameters, the resistance R_{DESAT} can be calculated as in eq.3.4-3.5, assuming the desired current threshold $I_{device,th} = 300\,A$

$$R_{desat} = \frac{7\,V - 4.4\,m\Omega \times 400\,A - 1.0\,V - 1.0\,V}{250\,\mu A} \tag{3.4}$$

$$R_{desat} = 13k\,\Omega \tag{3.5}$$

3.3.4 Testing of V_{ds} based Current Sensing Protection

The testing of V_{ds} based current sensing protection was performed, and the circuit diagram of the testing setup shown in Figure 3.5. Single pulse test was performed to verify the protection. The testing result is shown in Figure 3.6.

Table 3.2: V_{ds} based current sensing protection test condition

Parameter	Value
Input Voltage V_{bus}	$400\,V$
Inductance L_{Load}	$100\,\mu H$
Current threshold $i_{ds,th}$	$400\,A$
Power MOSFET	GE12047CCA3
Gate resistance	$3.3\,\Omega$

As shown in Figure 3.6. where channel 1 is the drain-source voltage V_{ds}, channel 2 is the device current I_{device}, and channel 3 is the inductor current I_L. As the MOSFET turns on, V_{ds} decreases from input voltage to ~$0\,V$, and the current increases as the voltage are applied to the inductor. During the device on-time, the inductor current is the same as the device current. When I_{device} reaches $384\,A$, the V_{ds} based current sensing protection is triggered, and the GDIC pulls the gate voltage to $-4\,V$, turning off the power MOSFET

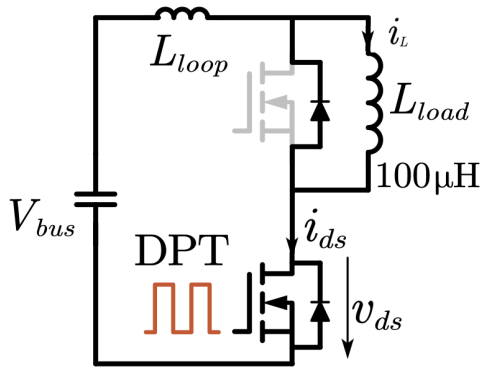


Figure 3.5: Double Pulse test Rogowski coil sensor

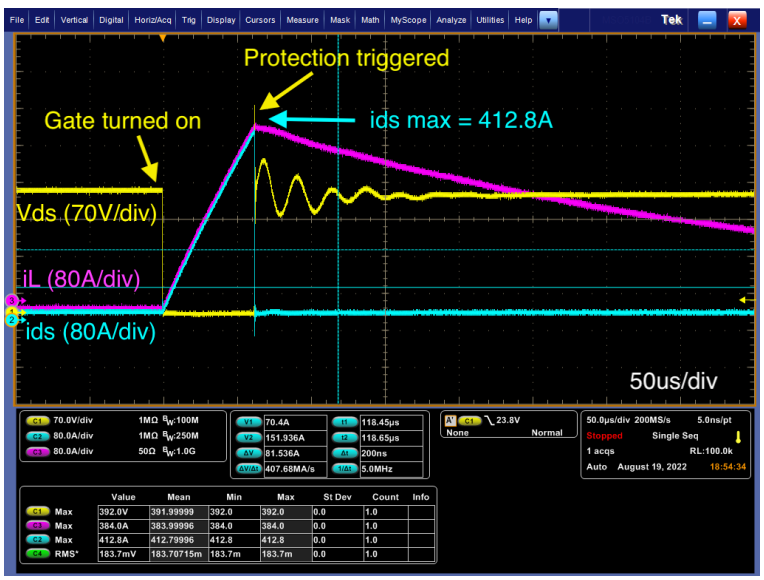


Figure 3.6: V_{ds} based current sensing protection testing result

and preventing the device from being damaged by high current.

3.4 Rogowski-coil Based Current Sensor and Protection

3.4.1 Rogowski Coil Design

A Rogowski coil is an air-core coil for measuring alternating current. Based on Ampere's law and Faraday's law, when the current $I(t)$ changes in the main conductor, the induced magnetic field will also change. As a result, the change of magnetic field will induce a voltage between both ends of the Rogowski coil[23]. The relationship between change of current $\frac{dI(t)}{dt}$ and induced voltage V_{coil} follows eq.3.6.

$$V_{coil} = M \times \frac{dI(t)}{dt} \tag{3.6}$$

Where M is the mutual inductance between the Rogowski coil and the main current conductor, The designed Rogowski coil for gate driver is shown in Figure 3.7 and 3.8

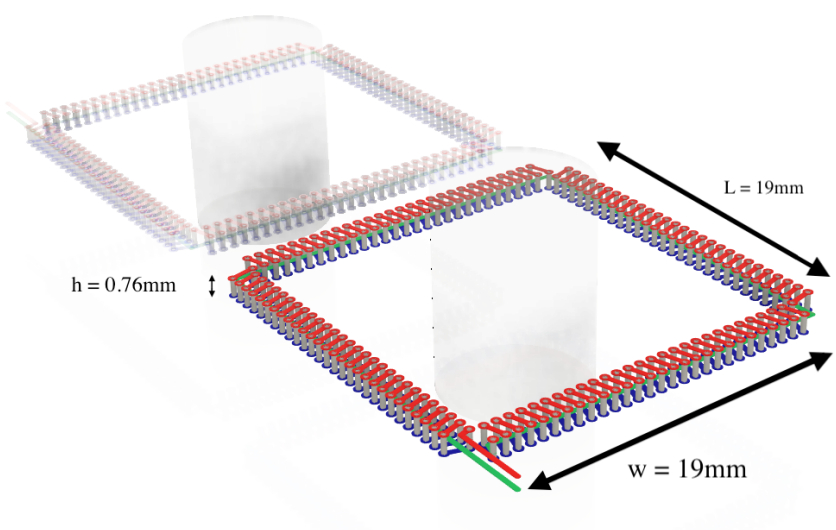


Figure 3.7: Rogowski coil design

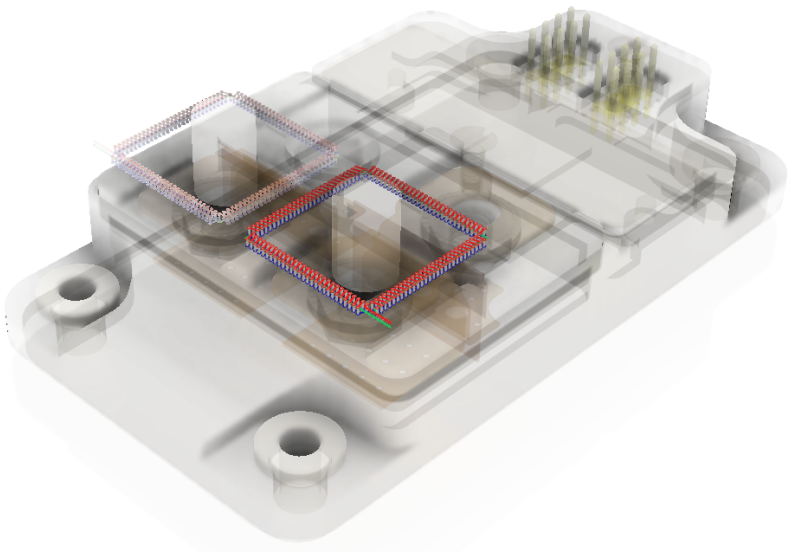


Figure 3.8: Rogowski coil design for GE module

Mutual Inductance of Rogowski Coil

The Rogowski coil interfacing board was manufactured and the mutual inductance was tested with pulse tests, the testing setup is shown in Figure 3.9.

The mutual inductance can be calculated as eq.3.7

$$M = \frac{dI(t)}{dt} \div V_{coil} \tag{3.7}$$

The mutual inductance of the coil on the interfacing board $M = 2.5\,nH$. The integrated Rogowski coil current I_{coil} shows as in eq.3.8 is compared with commercial current probe measurement.

$$I_{coil} = \frac{\int V_{coil}}{M} \tag{3.8}$$

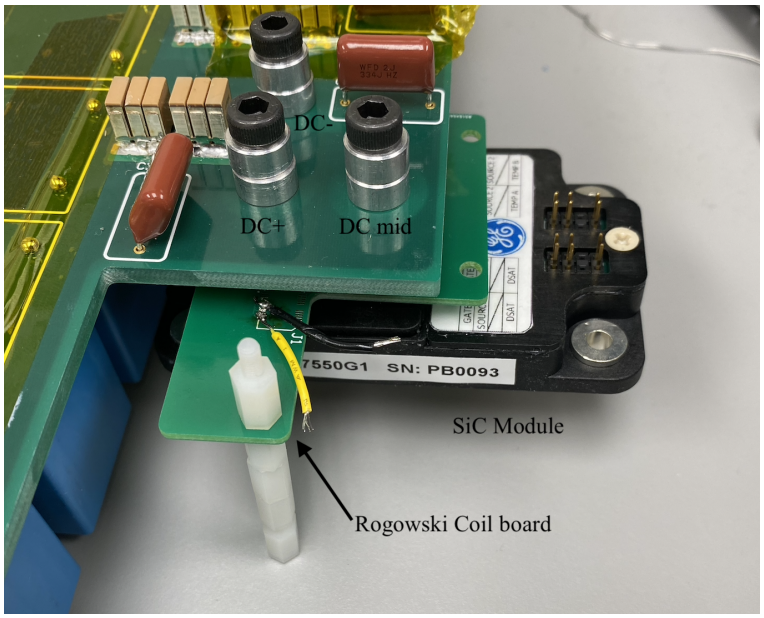


Figure 3.9: DPT setup for Rogowski coil Mutual inductance test

3.4.2 Design of Rogowski Coil Conditioning Circuits

The designed Rogowski coil current sensors circuit diagram is shown in Figure 3.10. The Rogowski coil sensor gate driver implementation can be divided into three parts, From top to bottom, Rogowski coil integrator conditioning circuit, analog high bandwidth loop short circuit protection, and digital over current protection circuits.

Integrator Design

An analog integrator was designed for integrating the output of the Rogowski coil voltage output. The main design criteria for the integration circuit is to design the gain ($G_{rog,VI}$) of the integrator according to the sensor design range while maintaining a high bandwidth. For instance, since the GE12047CCA3 SiC module's rated current is $400\,A$, the maximum current sensing range of the Rogowski coil current sensor was determined to be $1000\,A$. Furthermore, since the voltage range of the ADC and protection circuit is designed to be

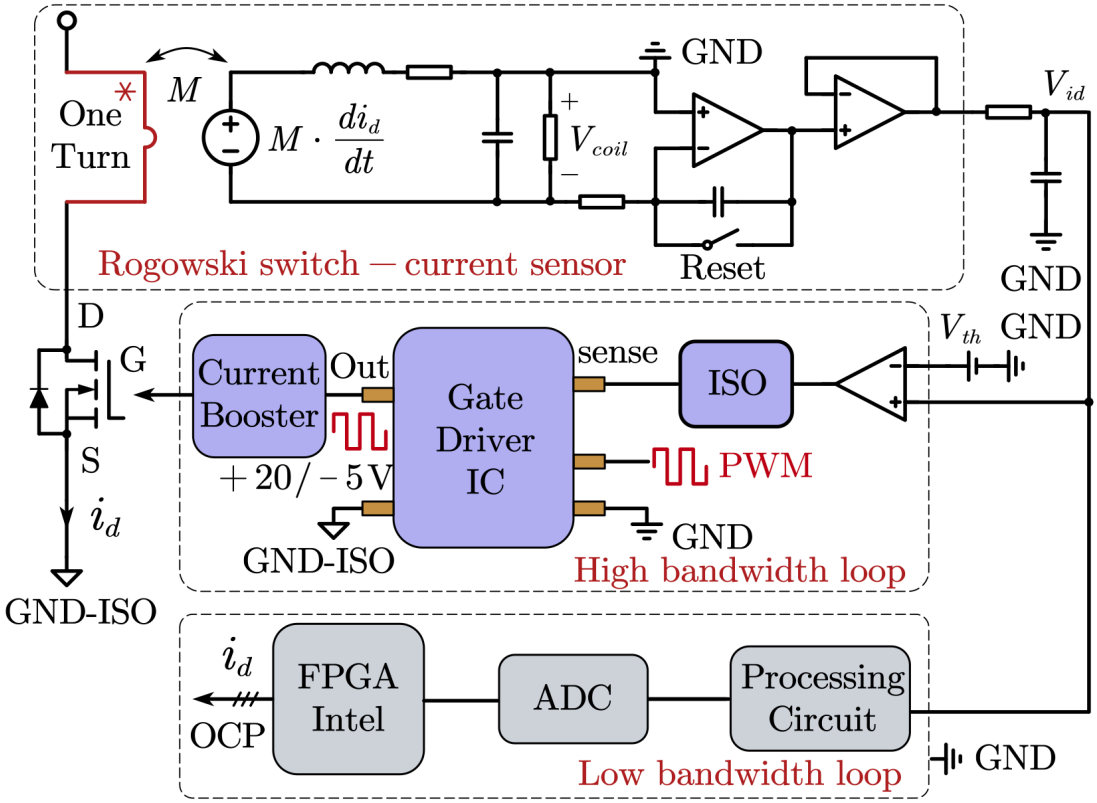


Figure 3.10: Rogowski coil current sensor gate driver circuit diagram

$0\,V - 5\,V$, the sensor gain can be calculated as eq.3.9.

$$G_{rog,VI} = \frac{I_{max}}{V_{max}} = \frac{1000\,A}{5\,V} = 200\,A/V \tag{3.9}$$

Since the ideal Op-amp does not exist in practice, the steady state leakage current of the op-amp will cause sensor error for the integrator, and the error will slowly accumulate on the integrator. Two methods were implemented to mitigate this issue, a potentiometer was added to compensate for the leakage current of the integrator offset, and an integrator reset MOSFET was added to discharge the integrator capacitor. The detailed calibration process of this potentiometer will be explained in the next subsection.

During the power MOSFET was switched off; based on the modulation scheme of the half-

bridge modules, the time period of the device current that has both been blocked by the MOSFET and its reverse current can be determined. The integrator reset MOSFET will be turned on during such a time period.

In order for the Rogowski coil sensor to capture the turn-on transient of the device current, the integrator reset MOSFET must be turned off prior to turning on the power MOSFET; and the integrator reset MOSFET must be turned off after the power MOSFET for capturing the turn off transient. The timing of the integrator reset signal (Channel 4) and gate signal of the power MOSFET is shown in Figure 3.11.

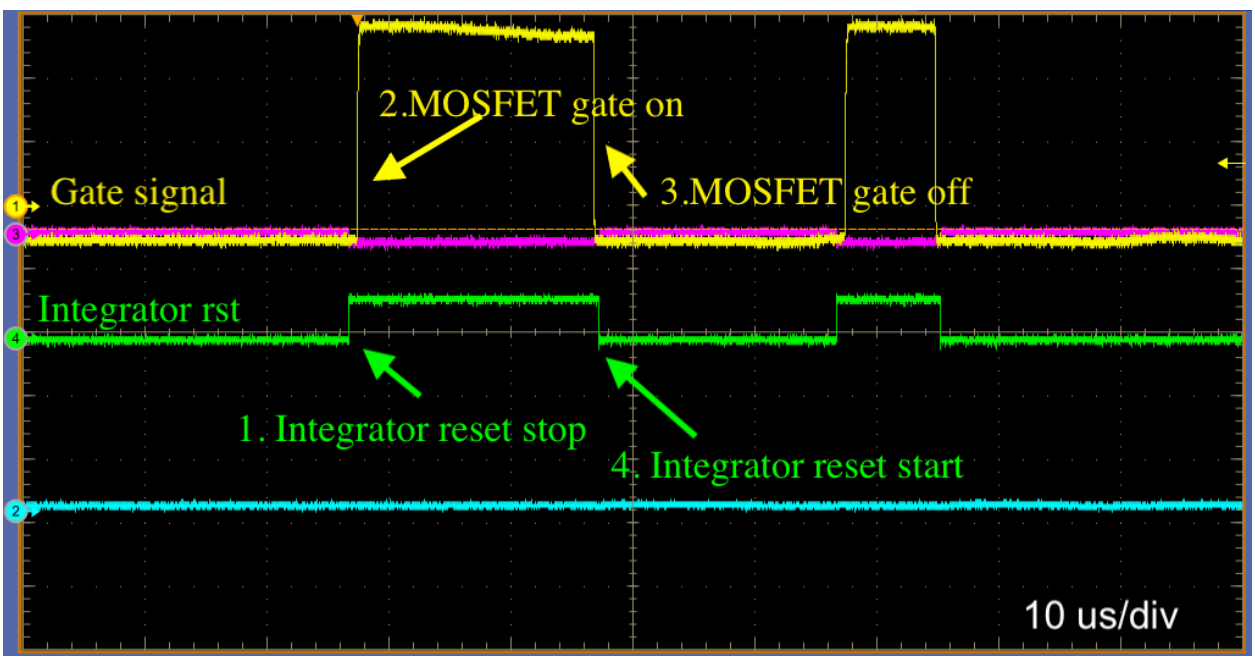


Figure 3.11: Timing of integrator reset MOSFET and power MOSFET

3.4.3 Testing of Rogowski Coil Current Sensor Accuracy

A double pulse test was performed to verify the conditioning circuits of the Rogowski coil integrator. Table 3.3 shows the testing condition of the double pulse test, and Figure 3.12 shows the testing result.

Table 3.3: Rogowski coil current sensor test condition

Parameter	Value
Input Voltage (V_{bus})	$480\,V$
Inductance (L_{Load})	$100\,\mu H$
Max current ($i_{ds,max}$)	$188\,A$
Power MOSFET	GE12047CCA3
Gate resistance	$3.3\,\Omega$

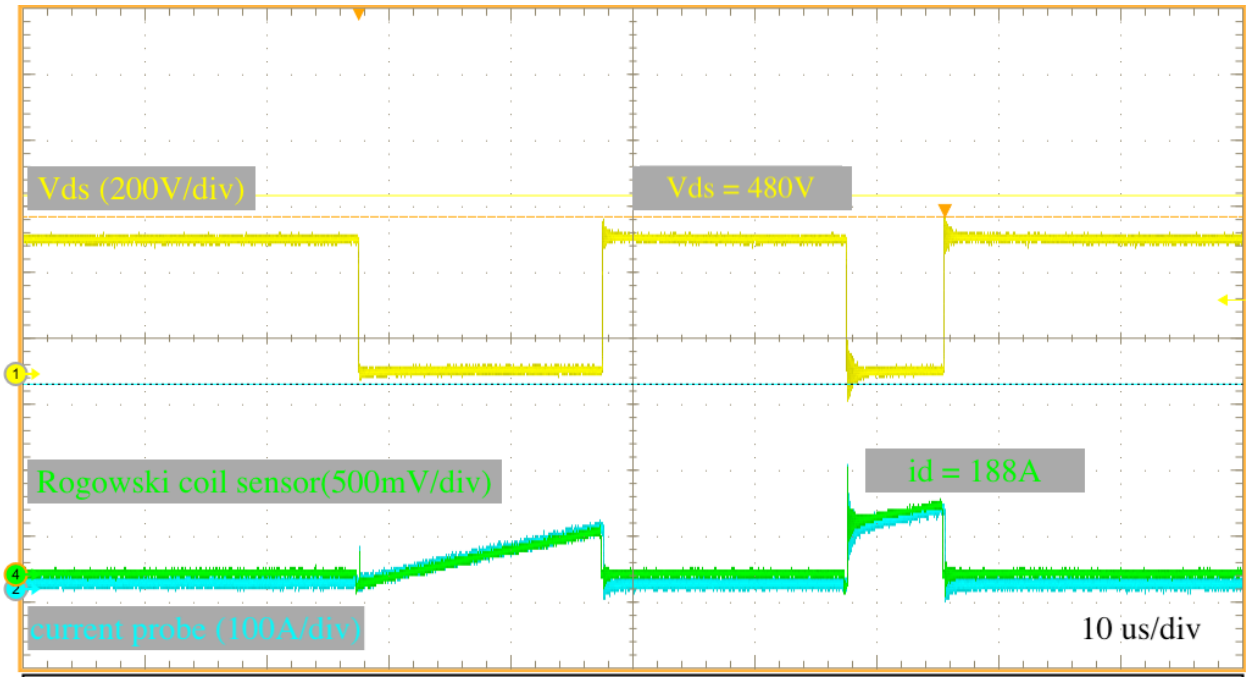


Figure 3.12: A testing result of analog Rogowski coil sensor conditioning circuits

As shown in Figure 3.12, where Channel1 is the waveform of V_{ds}, channel 2 is the device current measured with PEM CWT 3 UM commercial Rogowski coil probe, and channel 4 is the gate driver embedded Rogowski coil sensor voltage output V_{id}. Comparing the commercial Rogowski coil output with the gate driver Rogowski coil sensor output, the two waveforms show a good agreement.

3.4.4 Short Circuit Protection with Analog High-Bandwidth Loop

The high bandwidth loop short circuit protection utilizes the output voltage signal from the conditioning circuit V_{id}, which is connected to an op-amp comparator. This voltage signal is compared with a voltage threshold V_{th} to generate a fault signal. The desired threshold voltage V_{th} can be calculated with device threshold current $I_{device,th}$ as eq.3.10

$$V_{th} = \frac{I_{device,th}}{G_{rog,VI}} \tag{3.10}$$

When the device current exceeds the $I_{device,th}$, the sensor output voltage eV_{id} will exceed V_{th}. As a result, the output of the comparator will be logic level high. This signal is sent to the gate driver IC sense through a digital isolator. If the gate driver IC receives a high input signal, a fault will be latched into the gate driver, and the gate signal will be forced to $-4\,V$ to turn off the power MOSFET.

Table 3.4: Rogowski coil current sensor protection test condition

Parameter	Value
Input Voltage (V_{bus})	$600\,V$
Inductance (L_{Load})	$100\,\mu H$
Current threshold ($i_{ds,th}$)	$400\,A$
Power MOSFET	GE12047CCA3
Gate resistance	$3.3\,\Omega$

A double pulse test was performed to verify the effectiveness of the Rogowski coil. The testing result of the Rogowski coil-based short circuit protection is shown in Figure 3.13 and the testing condition is shown in Table 3.4. In this testing waveform, channel 1 is the V_{ds} voltage, channel 2 is the control gate signal that is sent to the gate driver, and channel 4 is the device current I_{device}. The threshold voltage V_{th} was set to $2\,V$, which the corresponding $I_{device,th} = 400\,A$. From the testing waveform, when I_{device} reaches $400\,A$, the short circuit

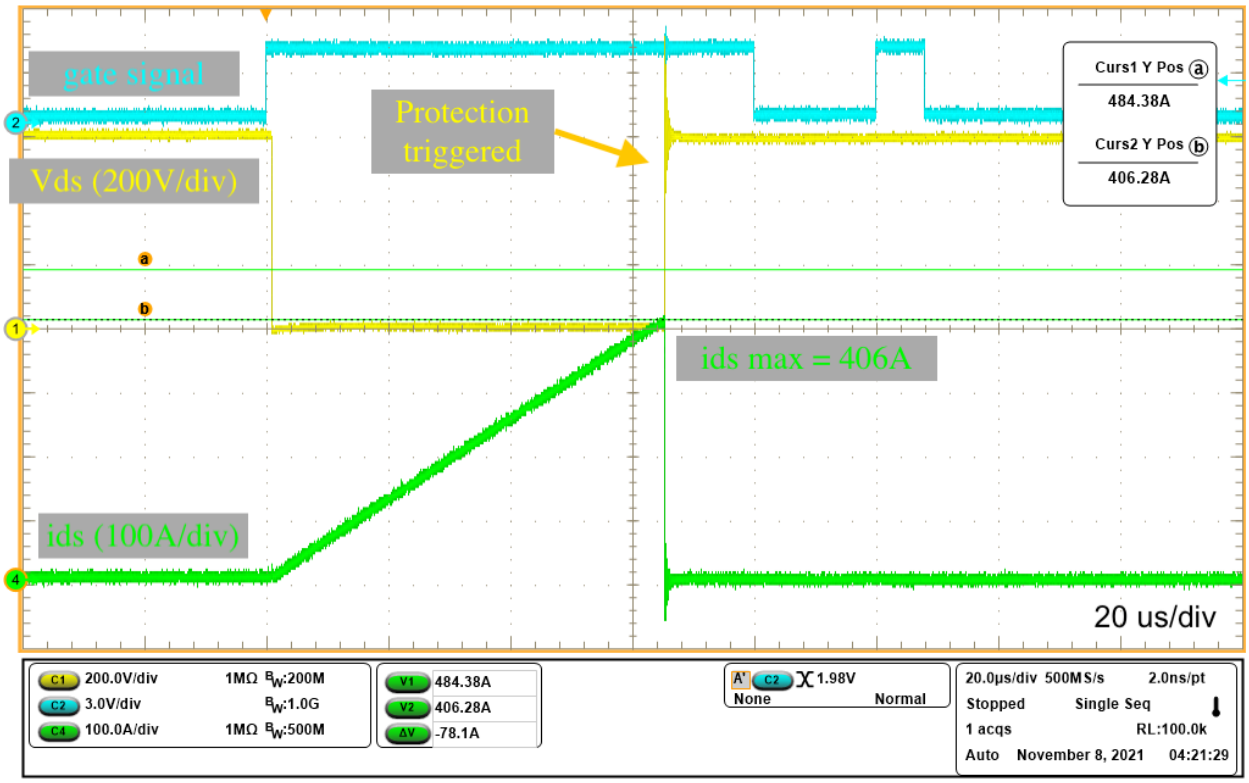


Figure 3.13: Rogowski coil sensor short circuit protection test

fault protection was triggered, V_{ds} increased to the bus voltage, indicating the device was turned off, and the device current dropped to $0\,A$.

3.4.5 Rogowski Coil Digital Current Sensor

A digital device sensor was also implemented with the Rogowski Coil output V_{id}. This sensor output is sent to an analog-to-digital converter (ADC) via a low-pass filter. The filter frequency is designed based on the sampling rate of the ADC. The ADC samples the sensor voltage and sends the data to FPGA via digital isolators via SPI communication protocols.

Double pulse tests were used to verify the accuracy of the digitally sampled data. First, the SPI communication packet was sampled with a digital analyzer, and the communication packet was decoded. This data is then plotted together with data gathered from the com-

mercial current probe. As Figure 3.14 indicates, the GD embedded digital sensor has a good agreement compared to the commercial Rogowski current probe.

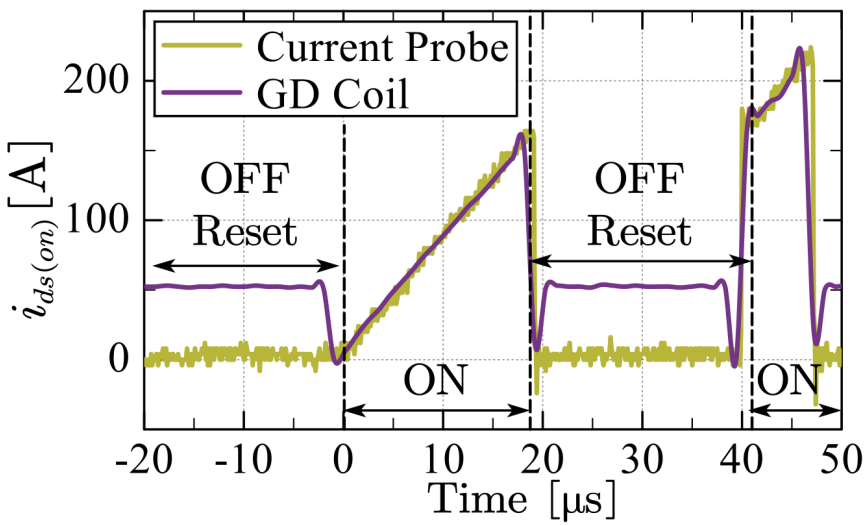


Figure 3.14: Comparison between current probe and digital GD Coil sensor

3.5 Rogowski Coil Current Sensor Calibration Process

A calibration process was required to compensate for the non-ideal characteristic of the integrator opamp, such as bias current. During calibration, the gate signal and the integrator reset signal are directly controlled by the fiber optic receivers on the gate driver.

When calibrating the Rogowski coil, the gate signal is constantly focused to high, and the integrator reset MOSFET is turned off. Under this condition, the potentiometer is adjusted until the output $V_{id} = 0\,V$.

3.6 Gate Driver Embedded On-State Drain-Source Voltage Sensor

In order to measure the device's on-state resistance, the on-state drain-source voltage sensor is implemented on the gate driver. The challenge of such sensor design is to block the high drain-source voltage when the power MOSFET is off V_{ds-off} while maintaining a high sensing resolution.

3.6.1 Operation Principle of Two Diode On-state Measurement Circuit

Two diode methods were implemented for sensing the on-state voltage of power MOSFET [12]. The two-diode method sensor circuit diagram is shown in Figure 3.15. The two-diode

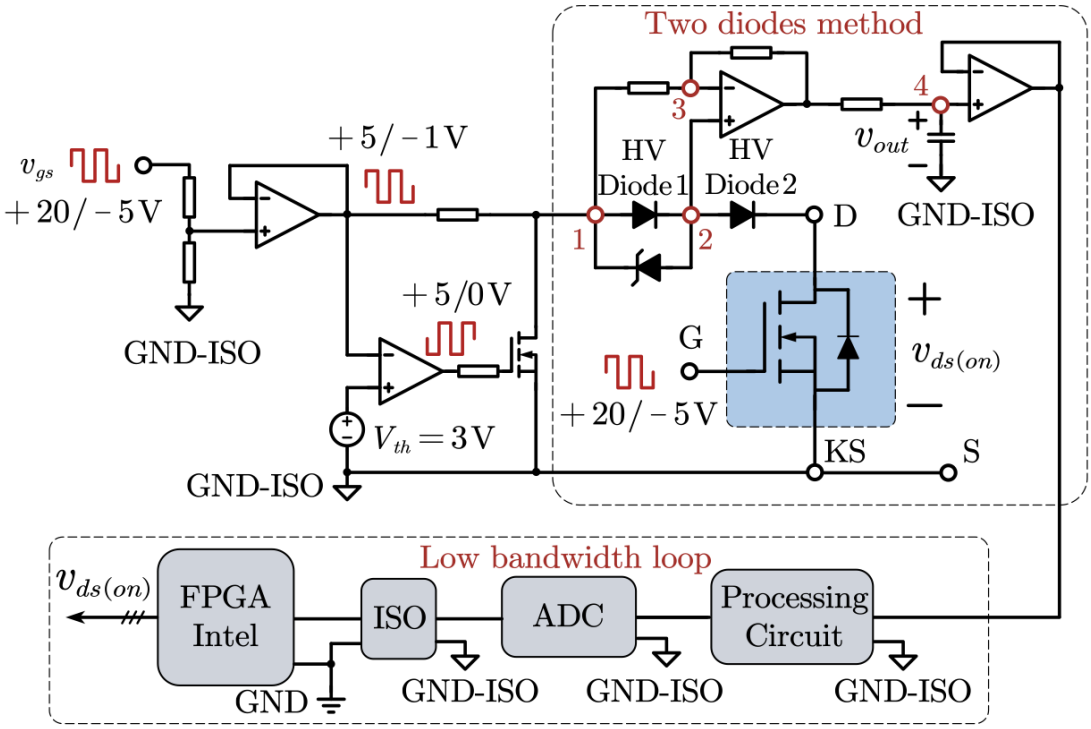


Figure 3.15: Two diode method on state voltage measurement circuit

method consists of two high-voltage diodes HV Diode 1 and HV Diode 2. Both diodes

are designed to utilize the same components. During the PCB layout of such circuits, HV diode 1 and HV diode 2 are placed as close as possible; therefore, the assumption of the same operation ambient temperature can be safely made. As a result, both diodes can be assumed to have the same forward voltage. Also, the resistors R1 and R2 are designed to have the same value.

When the gate signal V_{gs} is logic low, the MOSFET is turned on, and node 1 is pulled to the source of power MOSFET. HV diode 2 will block the V_{ds-off}, and the Zener diode will limit the maximum voltage drop between node 1 and node 2, protecting the sensing circuits.

When the gate signal is high, the MOSFET is turned off. Therefore the op-amp act as a constant current source, forcing both HV diodes into forwarding bias. Since the forward voltage of both HV diodes is the same, the voltage drop between node 1 and node 2, $V_{1,2}$ is equal to the voltage drop between node2 and Drain, $V_{2,D}$. Since $R_1 = R_2$, the voltage drop between node 1 and node 3, $V_{1,3}$ is equal to voltage between node 3 and node 4, $V_{3,4}$. Since for the op-amp circuit, node 3 and node 2 have the same voltage potential, therefore

$$V_{1,2} = V_{2,D} = V_{1,3} = V_{3,4} \tag{3.11}$$

The voltage of Node 4 can be solved as in eq.3.12. This signal is then sent to a processing circuit and then sent to ADC

$$V_4 = V_D \tag{3.12}$$

The performance of the two diode method on state measurement has been tested with a double pulse test. For measuring the V_{ds-on} of the device, a clipper probe in series with a Tek Isovu isolated differential probe was used as represented in Figure 3.16 and the testing condition is shown in Table3.5. The testing result is shown in Figure 3.17. The two diode

sensor samples match well compared to the scope measurements.

Table 3.5: Two diode on state voltage sensor test condition

Parameter	Value
Input Voltage (V_{bus})	$900\,V$
Inductance (L_{Load})	$100\,\mu H$
Max Current ($i_{ds,max}$)	$200\,A$
Power MOSFET	GE12047CCA3
Gate resistance	$3.3\,\Omega$

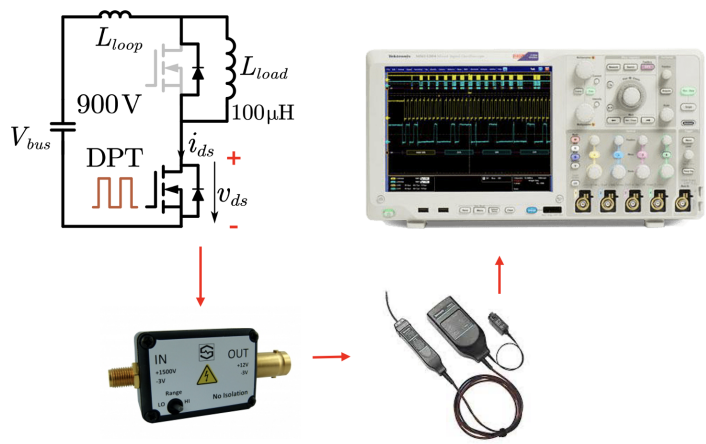


Figure 3.16: Testing setup for on state voltage sensor

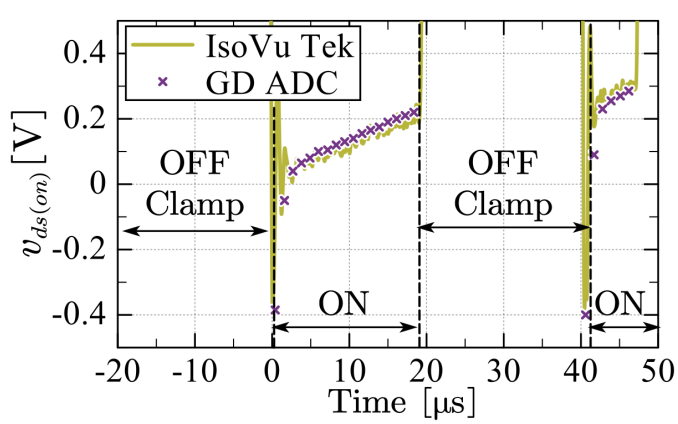


Figure 3.17: Testing result of two diodes on-state measurement compared with IsoVu scope measurement

3.7 Gate Driver Design Overview

3.7.1 Three-Board Design of Gate Driver

One of the design goals of this gate driver is to design a gate driver that can be adapted to different SiC MOSFET half-bridge modules from multiple manufacturers. To achieve this goal, the gate driver has been split into three boards, a digital processing board, an analog signal processing board, and an interfacing board. The gate driver has been designed based on previous researches[21][10][13]. For each gate driver board, the board driving the upper device is separated from the one driving the bottom device by a cutout on the board. Each side of the gate driver is grounded to the source of the power device with the isolated power ground. The gate driver is designed for GE 1.2 kV half-bridge modules GE12047CCA3 were manufactured, and the photo of the assembled gate driver is shown in Figure 3.18

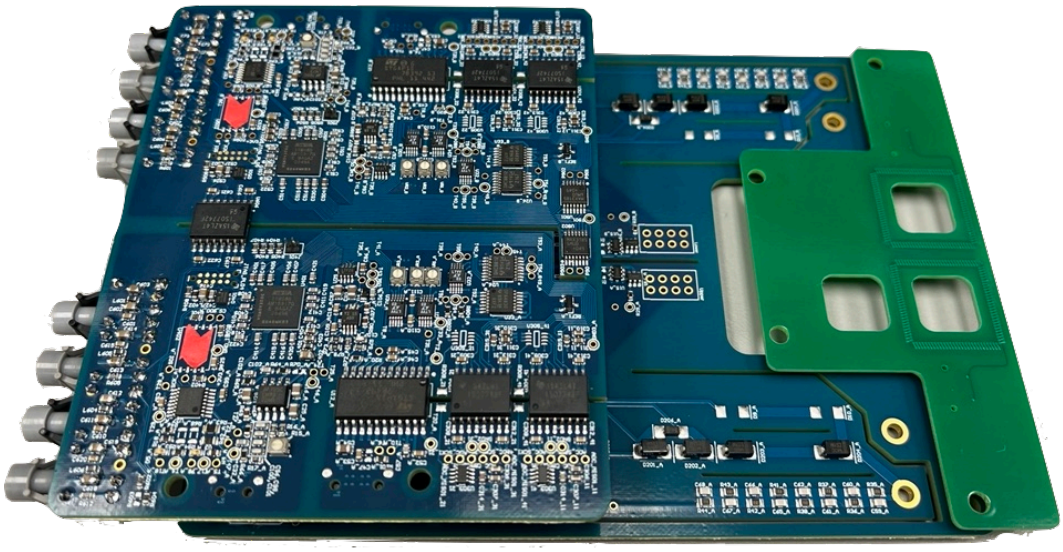


Figure 3.18: Assembled Enhanced Gate Driver boards for GE half-bridge modules

3.7.2 Interfacing Board

The interfacing board is used to adapt to the different mechanical designs of half bride modules from different manufacturers. Although in this version of the gate driver design, only the Rogowski coil is implemented on this board, the MOSFET control terminals, such as gate, kelvin source, and V_{ds} based current sensing protection pins are still located on the analog control board. In the future design, all connections between the gate driver and MOSFET modules are expected to be moved to the interfacing board. Therefore the digital signal processing board and analog signal processing can be universal. A detailed explanation of the Rogowski coil and related signal processing circuits will be discussed in this chapter. Figure 3.19 shows the interface design of the gate driver for GE SiC modules.

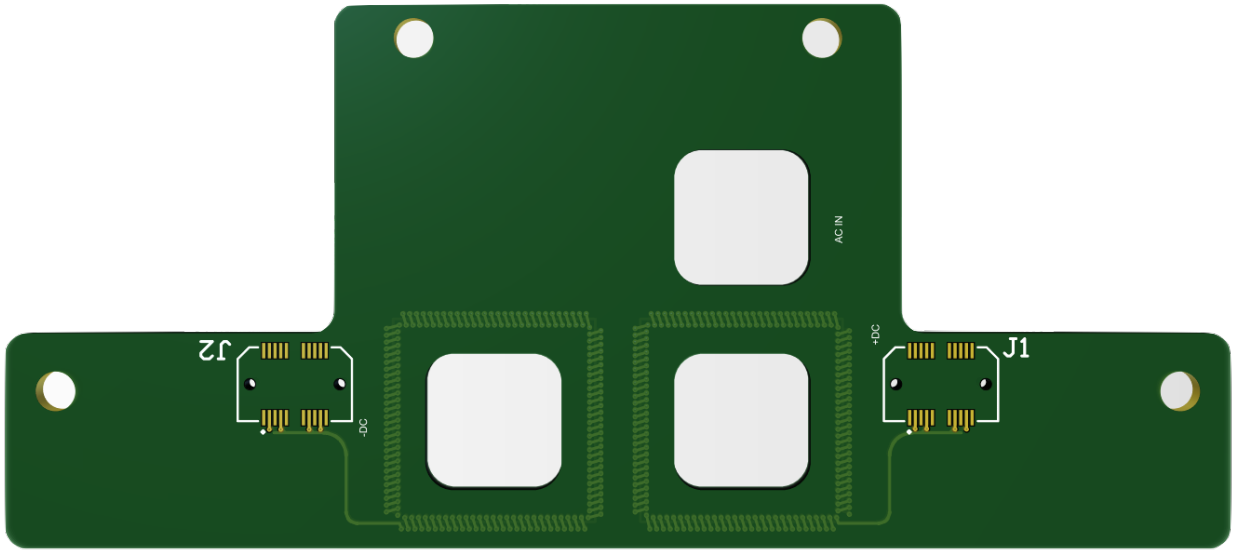


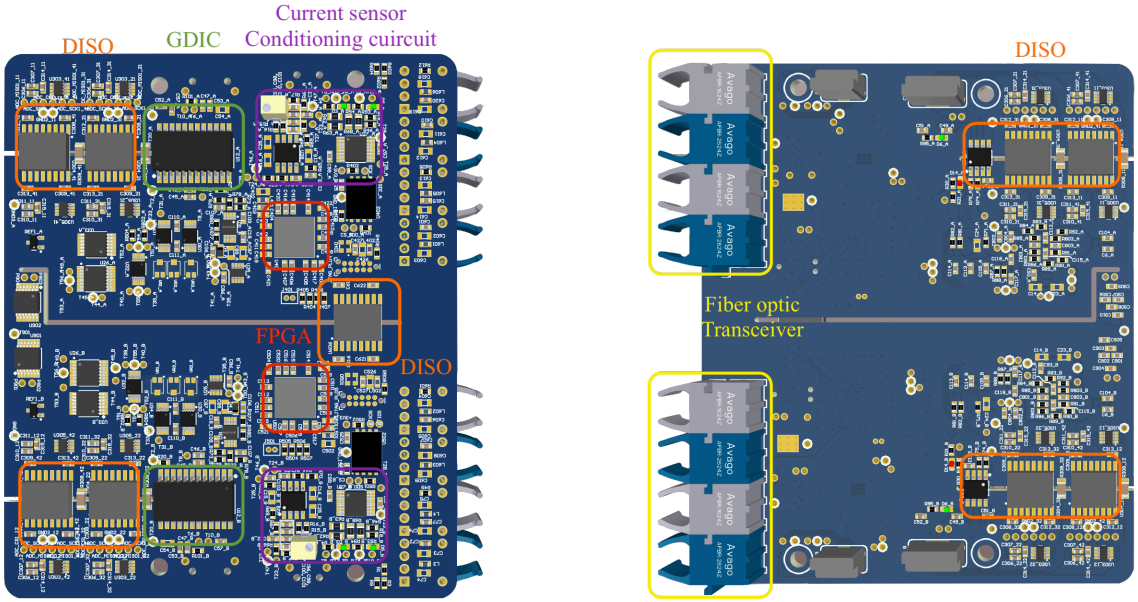
Figure 3.19: Interfacing design of gate driver

3.7.3 Digital Signal Processing Board

On digital signal processing board is shown in Figure 3.20. On the digital signal processing board, the FPGA is located. The FPGA of the gate driver is used for collecting sensor data

from the analog signal processing board, controlling the gate driving signal that is sent to the gate driver integrated controller chip (GDIC), and performing over-current protection based on the sensor data. Also, the FPGA is connected to the GDIC SPI pins. The FPGA will program the GDIC through SPI communication protocols by setting up the corresponding registers during the start-up procedure. Also, the fiber optics transmitter and receiver are located on the digital signal board. These fiber optic ports allow the upper-level controller to send switching command and synchronization pulses to the FPGA on the gate driver and enable the gate driver to send its sensor data back to the upper-level controller[24][25].

In the event of gate driver short circuit protection, over-current protection, or over-voltage protection being triggered, the onboard FPGA will collect the fault code from GDIC through SPI communication and then send the fault signal together with the corresponding fault code to the upper-level controller. The details about protections will be explained in the following subsections.



(a) Top (b) Bottom

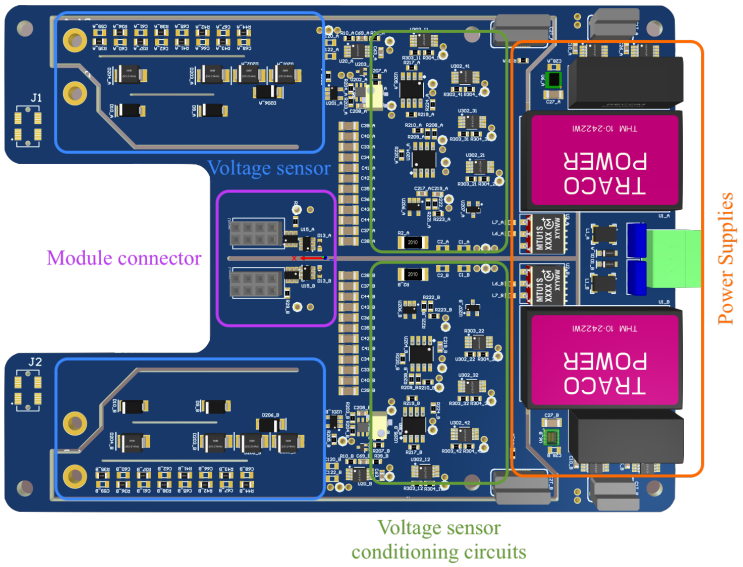
Figure 3.20: Digital signal processing board design of gate driver

3.7.4 Analog Signal Processing Board

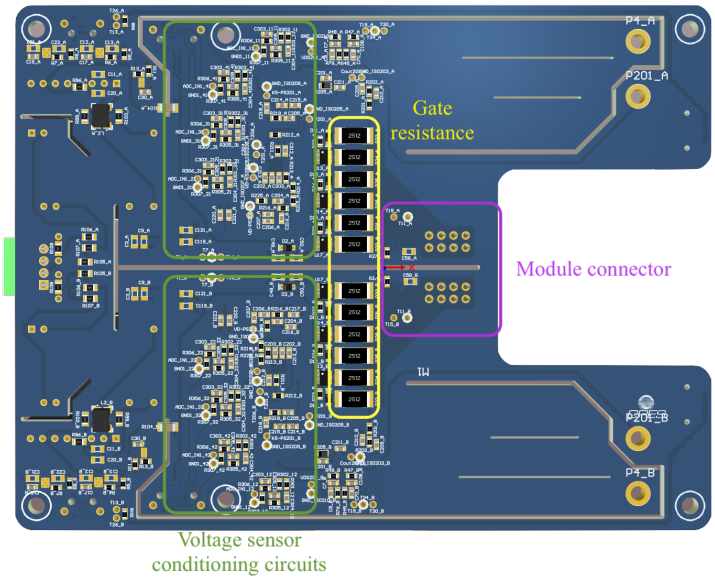
The analog board is placed between the digital signal board and the interface board. As its name suggests, this board will process the analog signal for all the gate driver-based sensors. The power supplies for all power buses are located on this board. This includes $+20\,V$ and $-4\,V$ that are isolated and used for driving the gate signal of the MOSFET, isolated $+5\,V$ and $-5\,V$ for signal processing operational amplifiers, $3.3\,V$ for FPGA and non-isolated $+5\,V$ and $-5\,V$ for analog to digital converters. On the analog board, the current booster that is used for providing high current up to $30\,A$ is also located, as well as the gate driving resistors. The design of the analog signal processing board is shown in Figure 3.21.

3.7.5 Three board Design of Gate Driver for Different Half-bridge Modules

The three-board design of the gate driver board allows minimal changes for adapting different half-bridge module connections. The digital board and analog sensors can remain unmodified; this will reduce the chance of potential issues caused by modifying related circuits. The different gate driver design that adapts to Wolfspeed half-bridge modules are shown in Figure 3.22, and the gate driver that is compatible with General electric SiC half-bridge modules are shown in Figure 3.23.



(a) Top



(b) Bottom

Figure 3.21: Analog signal processing board of gate driver

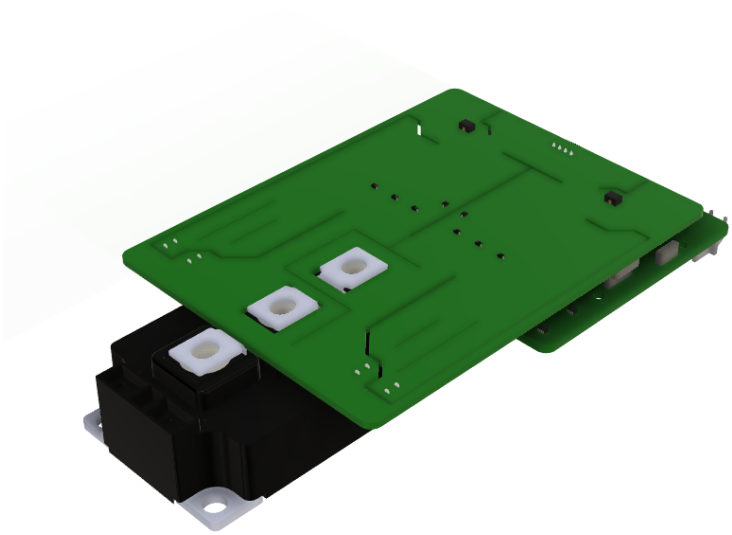


Figure 3.22: Three Board Gate Driver design for Wolfspeed Modules(modules attached)

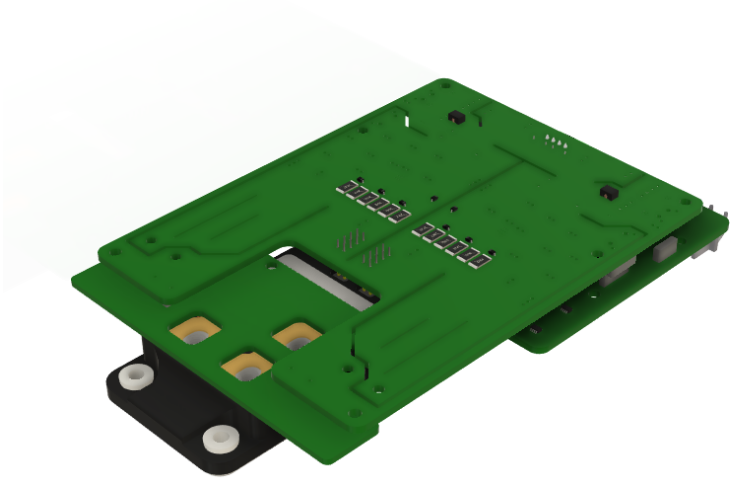


Figure 3.23: Three Board Gate Driver design for GE Modules (Modules attached)

3.8 Mechanical Design of Gate Driver

Since the gate driver includes the voltage sensing capability, the drain and source power terminal must be connected between the gate driver and the bus bar. The gate driver was designed to include four mounting holes that electrically connect to the drain and source. When assembling the busbar with a switching device, the gate driver can be first mounted to the busbar. Therefore those mounting holes can also be used as mechanical support structures for assembly.

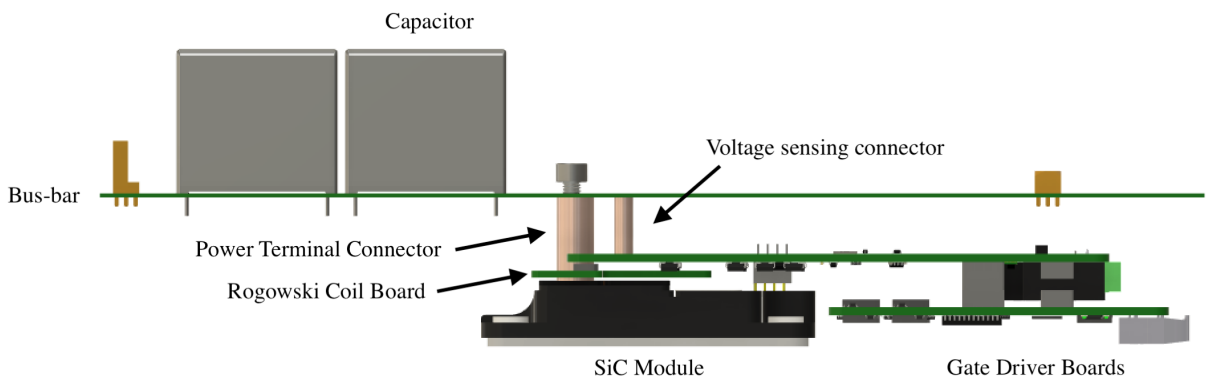


Figure 3.24: Busbar gate driver and module assemby

Chapter 4

Small Signal Model of FSBB Converter and Future Work

4.1 Small Signal Modeling of FSBB Converter

Power electronics switching devices have greatly changed the power industry by increasing power efficiency and power density of power converters. But the non-linearity of the switching device has created challenges for modeling and controlling the power electronics converter. A small signal model is an essential tool that approximates the non-linear switching power electronic circuit AC circuit behavior with a linear equation. With the help of the small signal model, the closed-loop control compensator can be easily designed. The small signal model for FSBB converter 4.1 under CCM operation was derived [26] .

However, the existing small signal model derivation process has implemented the small ripple approximation, which is only valid for traditional CCM operations. The inductor current of the QCM control method requires the inductor current to become negative to maintain the ZVS requriement. Also, the existing small signal does not consider the phase shift between the input half-bridge and the output half-bridge operation. Therefore a new small signal model that can be applied to the FSBB converter under QCM operation control is necessary.

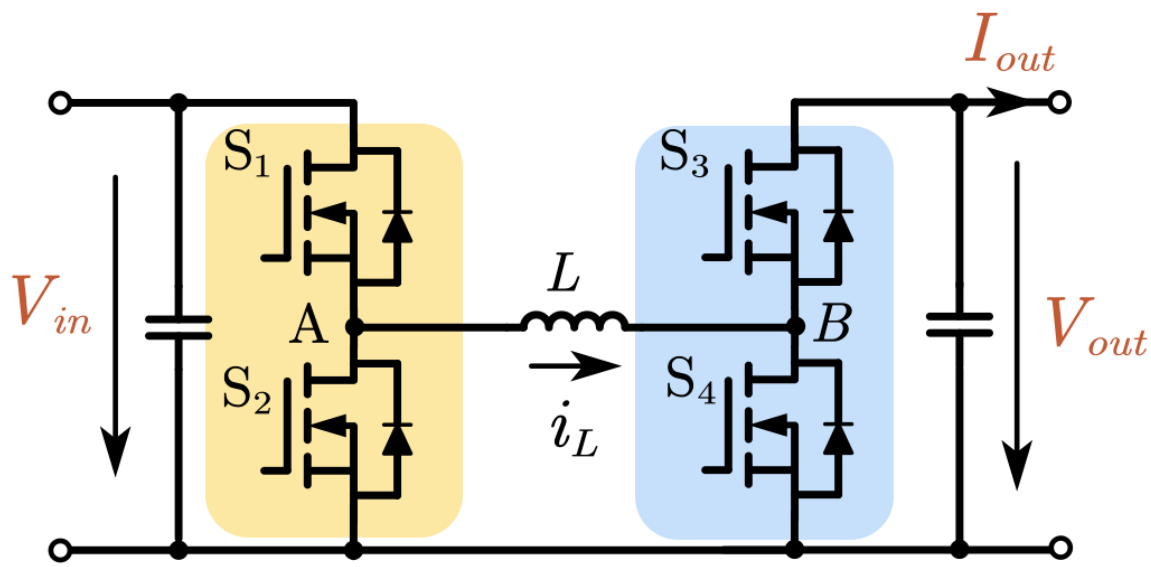


Figure 4.1: FSBB converter topology

4.2 Average Model of FSBB Converter

To simplify the derivation process, the input capacitor is ignored, and all parasitic of the components, such as equivalent series resistor (ESR) of inductor and output capacitor are ignored. Also, the switching MOSFETs are considered ideal switches. Also, assuming the output side is directly connected to a resistive load, the resistance R will not change. In order to obtain the small signal model, the switching circuit needs to be first linearized and obtain an average model. The three-terminal linearize method was used to linearize the input half-bridge and the output half bridge separately, as shown in Figure 4.2. By inspecting the average circuit model, both the input half-bridge and output bridge voltage source is connected to the inductor. Therefore the interference between the input half-bridge and output half-bridge on the inductor current must be considered.

By applying the three terminal model, the average switching model of the FSBB converter

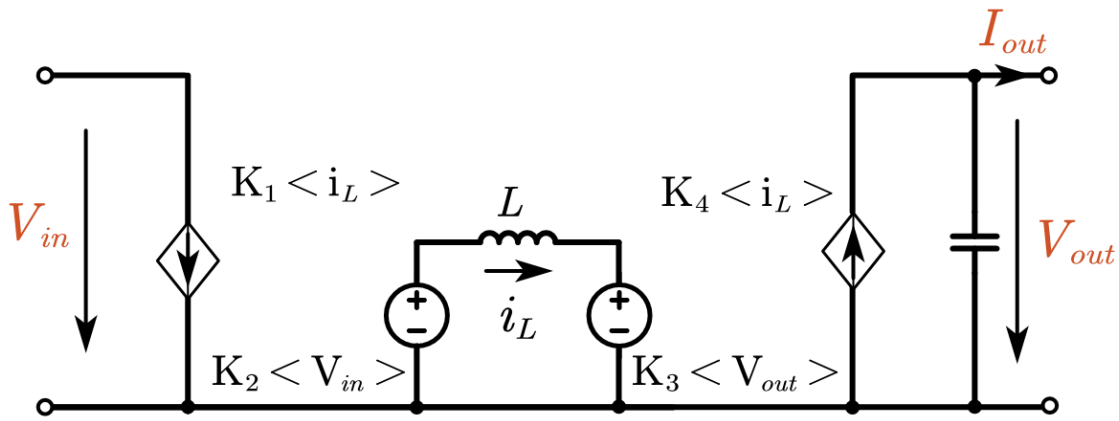


Figure 4.2: Average model of FSBB converter

is shown in Figure. 4.2[27]. The mathematical representation of four dependent sources that need to derive. The current source K_1, K_4 represents the relationship between input and output current with respect to the inductor current. The voltage source K_2, K_3 represents the terminal A and terminal B respect to V_{in} and V_{out}. In CCM FSBB converter, the small ripple approximation can be made to obtain the relationship between input currnet and inductor currnetas as Figure. 4.3. Eq.4.1-4.2 shows the value of K_2 and K_3 by applying small ripple approximation.

$$K_{2,smallripple} = D_1 \tag{4.1}$$

$$K_{3,smallripple} = D_2 \tag{4.2}$$

The input current waveform and inductor current waveform under the QCM step down operation in each switching period is shown in Figure 4.4. By analyzing the inductor current waveform, because of the quadrangle shape of the inductor current waveform and the existance of freewheeling period, the relationship between average input current and average inductor current no longer simply follows the duty ratio D_1, the interference of the output half bridge should also be considered. I_0 is the free wheeling current during $t_3 - t_4$. To ob-

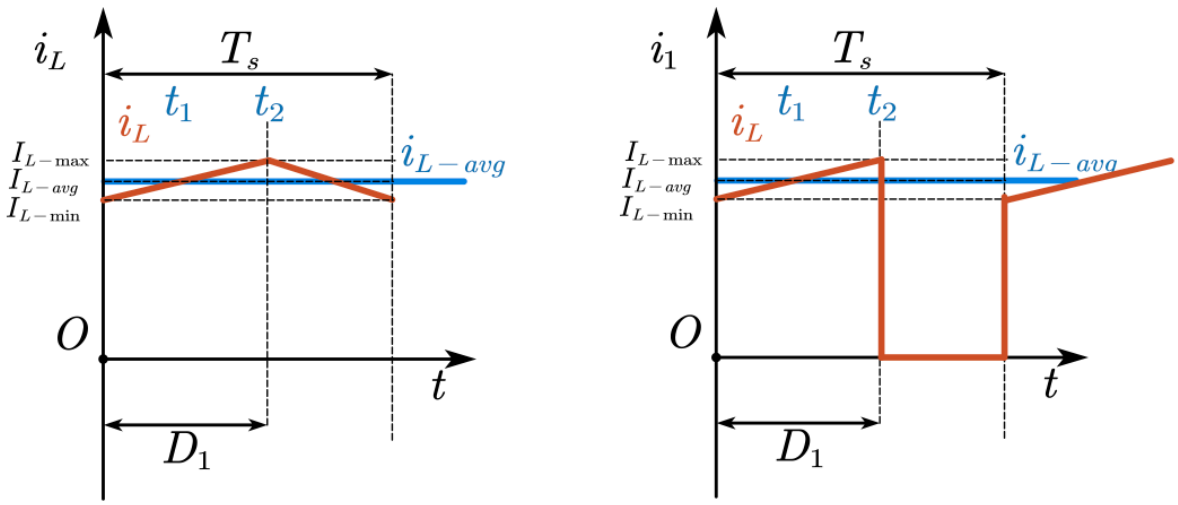


Figure 4.3: Input current and indcutor current waveform under CCM modulation

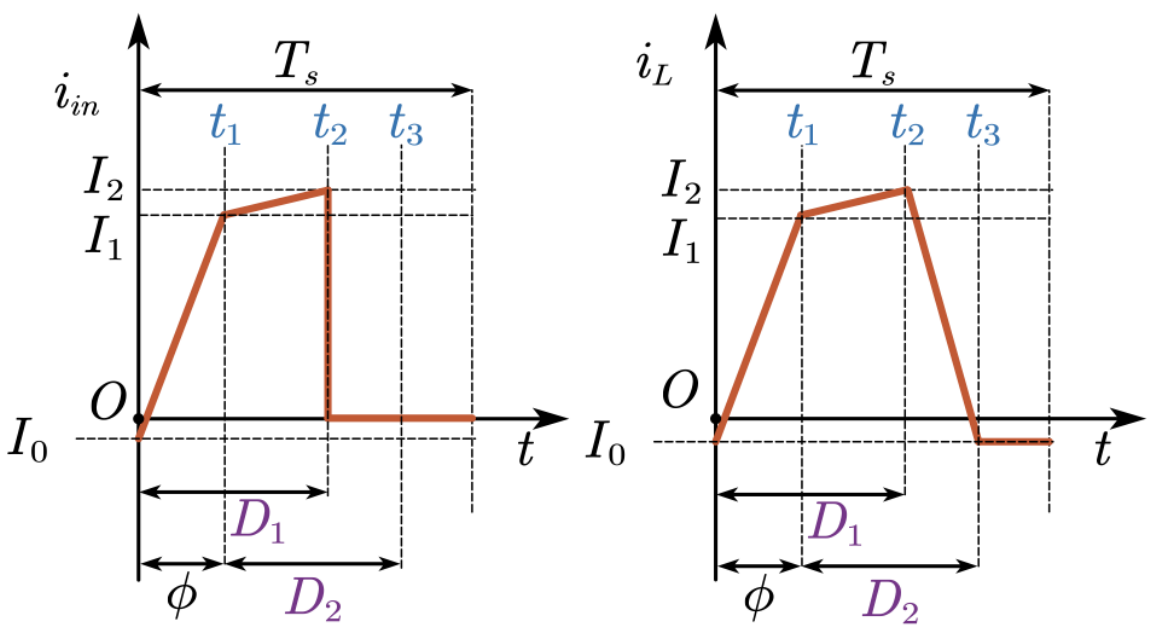


Figure 4.4: Input current waveform and inductor current waveform under QCM modulation

tain the accurate relationship between average inductor current and input or output current, the continuous time equation describing input current, output current and inductor current is necessary. According to the QCM control introduced in Chapter.2, the inductor current waveform mathematical equation can be derived as in eq.4.3

$$i_{in}(t) = \begin{cases} \frac{V_{in}t}{L} - I_0 & (0 < t < t_1) \\ \frac{(V_{\text{in}} - V_{\text{out}})(t-\phi)}{L} + \frac{T_s V_{\text{in}}}{L} - 2I_0 & (t_1 < t < t_2) \\ \frac{T_s(V_{\text{in}} - V_{\text{out}})(D_1-\phi)}{L} + \frac{T_s \phi V_{\text{in}}}{L} - 3I_0 - \frac{V_{out}(t-D_1)}{L} & (t_2 < t < t_3) \\ -I_o & (t_3 < t < t_4) \end{cases} \tag{4.3}$$

Also, by analyzing the input half-bridge operation, During the period D_1, the switch S_1 is turned on, and the input is connected to the inductor, therefore the input current is equal to the inductor current form $0 - t_2$. During D_1', the switch S_1 is turned off, the input current is blocked, therefore the input current is 0, the input current equation can be expressed as eq. 4.4.

$$i_{in}(t) = \begin{cases} \frac{V_{in}t}{L} - I_0 & (0 < t < t_1) \\ \frac{(V_{\text{in}} - V_{\text{out}})(t-\phi)}{L} + \frac{T_s V_{\text{in}}}{L} - 2I_0 & (t_1 < t < t_2) \\ 0 & (t_2 < t < T_s) \end{cases} \tag{4.4}$$

To obtain K_1, the average value of the inductor current and input current in each period needs to be calculated as eq. 4.5-4.8.

$$< i_{in} >= \int_0^{T_s} i_{in}(t)\, dt \tag{4.5}$$

$$< i_{in} >= -\frac{T_s}{2L}\Big(4D_1 I_0 L - 2I_0 L\phi - {D_1}^2 T_s V_{in} + {D_1}^2 T_s V_{out} + T_s V_{out}\phi^2 - 2D_1 T_s V_{out}\phi\Big) \tag{4.6}$$

$$< i_L >= \int_0^{T_s} i_L(t)\, dt \tag{4.7}$$

$$< i_L >= -\frac{T_s}{2L}(2I_0L - 2D_1I_0L + 4D_2I_0L + 2I_0L\phi + {D_1}^2T_sV_{in} + {D_2}^2T_sV_{out} - 2D_1D_2T_sV_{in} - 2D_1T_sV_{in}\phi) \quad (4.8)$$

Similarly, the average output current $< i_{out} >$ can be derived.

$$< i_{out} >= \int_0^{T_s} i_{out}(t)\,dt \quad (4.9)$$

$$< i_{out} >= -\frac{T_s}{2L}(T_sV_{in}{D_1}^2 - 2T_sV_{in}D_1D_2 - 2T_sV_{in}D_1\phi - 2I_0LD_1 + T_sV_{out}{D_2}^2 + 6I_0LD_2 + T_sV_{in}\phi^2 + 2I_0L\phi) \quad (4.10)$$

Therefore the controlled source K1 can be derived as eq. 4.12.

$$K_1 = \frac{< I_{in} >}{< I_L >} \quad (4.11)$$

$$K_1 = \frac{4D_1I_0L - 2I_0L\phi - \sigma_1 + {D_1}^2T_sV_{out} + T_sV_{out}\phi^2 - 2D_1T_sV_{out}\phi}{2I_0L - 2D_1I_0L + 4D_2I_0L + 2I_0L\phi + \sigma_1 + {D_2}^2T_sV_{out} - 2D_1D_2T_sV_{in} - 2D_1T_sV_{in}\phi} \quad (4.12)$$

where

$$\sigma_1 = {D_1}^2T_sV_{in} \quad (4.13)$$

Similarly, the output half bridge average model current source can be derived as eq. 4.14.

$$K_4 = \frac{< I_{out} >}{< I_L >} \quad (4.14)$$

$$K_4 = \frac{\begin{array}{r} T_s V_{in} {D_1}^2 - 2T_s V_{in} D_1 D_2 - 2T_s V_{in} D_1 \phi - 2I_0 L D_1 + T_s V_{out} {D_2}^2 \\ + 6I_0 L D_2 + T_s V_{in} \phi^2 + 2I_0 L \phi \end{array}}{\begin{array}{r} 2I_0 L - 2D_1 I_0 L + 4D_2 I_0 L + 2I_0 L\phi + {D_1}^2 T_s V_{in} + {D_2}^2 T_s V_{out} \\ -2D_1 D_2 T_s V_{in} - 2D_1 T_s V_{in} \phi \end{array}} \tag{4.15}$$

The voltage source in the average model describes the relationship between terminal voltage A and be in relationship to V_{in}, V_{out}. The terminal voltages are expressed in eq.4.16-4.17.

$$V_A(t) = \begin{cases} V_{in} & (0 < t < t_2) \\ 0 & (t_2 < t < T_s) \end{cases} \tag{4.16}$$

$$V_B(t) = \begin{cases} V_{out} & (t_1 < t < t_3) \\ 0 & (0 < t < t_1)\&(t_3 < t < T_s) \end{cases} \tag{4.17}$$

The inductor voltage and input terminal voltage V_A, V_B are shown in Figure 4.5

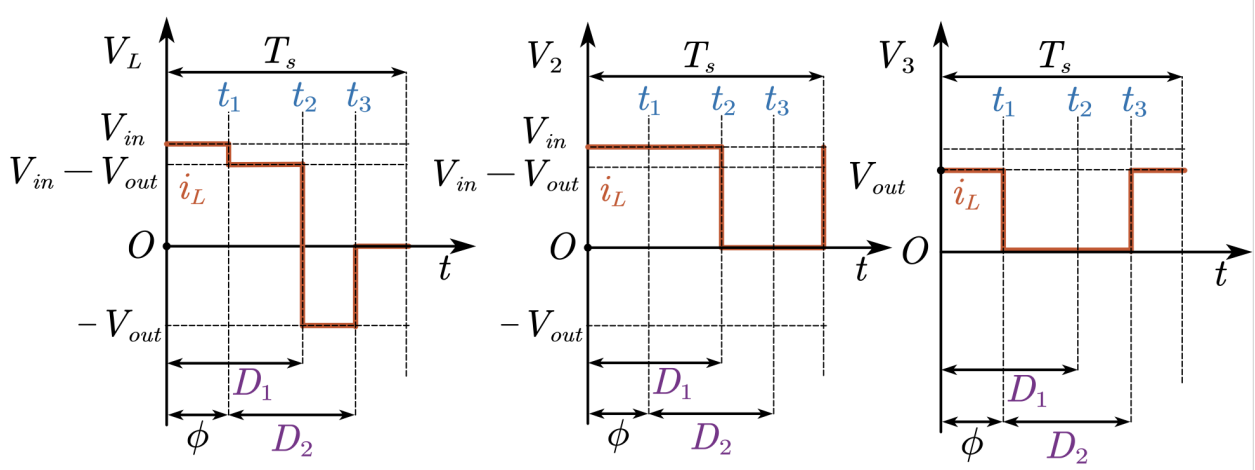


Figure 4.5: Inductor, node A B voltage waveforms

notation v2/v3 to VA VB The average voltage of V_A, V_B in each switching period $< V_A >$, $< V_B >$ can be solved as eq 4.18- 4.21.

$$< V_A >= \int_0^{T_s} V_A \, dt \tag{4.18}$$

$$< V_A >= D_1 V_{in} \tag{4.19}$$

$$< V_B >= \int_0^{T_s} V_B \, dt \tag{4.20}$$

$$< V_B >= D_2 V_{out} \tag{4.21}$$

The dependent voltage source K_2, K_3 can be solved in eq 4.22 -4.25 .

$$K_2 = \frac{< V_A >}{< V_{in} >} \tag{4.22}$$

$$K_2 = D_1 \tag{4.23}$$

$$K_3 = \frac{< V_B >}{< V_{out} >} \tag{4.24}$$

$$K_3 = D_2 \tag{4.25}$$

Therefore the complete average model of FSBB converter under QCM control method is obtained. The complete Average model of FSBB converter is shwon in eq.4.26

$$\begin{cases} K_1 = \frac{4D_1 I_0 L - 2I_0 L\phi - \sigma_1 + {D_1}^2 T_s V_{out} + T_s V_{out}\phi^2 - 2D_1 T_s V_{out}\phi}{2I_0 L - 2D_1 I_0 L + 4D_2 I_0 L + 2I_0 L\phi + \sigma_1 + {D_2}^2 T_s V_{out} - 2D_1 D_2 T_s V_{in} - 2D_1 T_s V_{in}\phi} \\ K_2 = D_1 \\ K_3 = D_2 \\ K_4 = \dfrac{\begin{array}{r} T_s V_{in} {D_1}^2 - 2T_s V_{in} D_1 D_2 - 2T_s V_{in} D_1 \phi - 2I_0 L D_1 + T_s V_{out} {D_2}^2 \\ + 6I_0 L D_2 + T_s V_{in}\phi^2 + 2I_0 L\phi \end{array}}{\begin{array}{r} 2I_0 L - 2D_1 I_0 L + 4D_2 I_0 L + 2I_0 L\phi + {D_1}^2 T_s V_{in} + {D_2}^2 T_s V_{out} \\ -2D_1 D_2 T_s V_{in} - 2D_1 T_s V_{in}\phi \end{array}} \end{cases} \tag{4.26}$$

4.3 Small Signal Model of FSBB Converter

The small signal model is obtained by injecting perturbation to control variables and state variables $D_1, D_2, \phi, V_{in}, V_{out}, I_{out}$, as eq. 4.27-4.31

$$< D_1 >= D_1 + \hat{d}_1 \tag{4.27}$$

$$< D_2 >= D_2 + \hat{d}_2 \tag{4.28}$$

$$< \phi >= \phi + \hat{\phi} \tag{4.29}$$

$$< V_{in} >= V_{in} + \hat{v_{in}} \tag{4.30}$$

$$< V_{out} >= V_{out} + \hat{v_{out}} \tag{4.31}$$

And the inductor current i_L is used for the intermediate term. The DC terms and non-linear terms can be ignored[28]. To aid the design of the compensator, the control to output transfer function $\frac{\hat{V_{out}}}{\hat{D}_1}$ is desired and the the equivalent small signal model circuit can be shown in Figure 4.6 with the perturbation of input voltage $\hat{V_{in}}$ and control parameter $\hat{D}_2$ are set to 0. To obtain the transfer the function of using KVL to solve inductor current

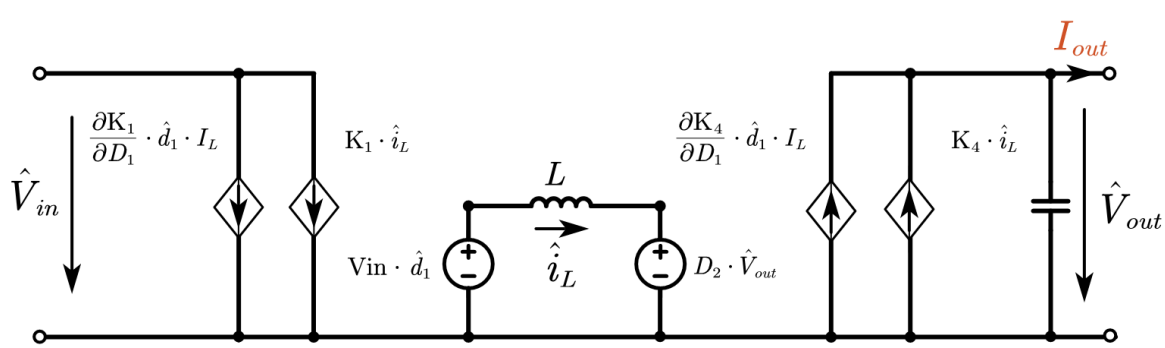


Figure 4.6: Small signal model of $\hat{d}_1$ to V_{out}

between controlled voltage source and the inductor:

$$\hat{i_L} = \frac{V_{in}\,\hat{d}_1 + D_1 - D_2\,\hat{V_{out}}}{L\,s} \tag{4.32}$$

And the output side can be solved by using KVL.

$$\frac{\partial K_4}{\partial D_1}\hat{d}_1 I_L + \frac{\partial K_4}{\partial i_L}\hat{i_L} = \frac{\hat{V_{out}}}{Z_{load}} \tag{4.33}$$

where

$$Z_{load} = \frac{1}{C_{out}\,s + \frac{1}{R}} \tag{4.34}$$

Substitute i_L in eq.4.33 with eq.4.32 and rearrange the function, the transfer function $\frac{\hat{V_{out}}}{\hat{D}_1}$ can be obtained. The complete transfer function is provided in the appendix.

$$\frac{\hat{V_{out}}}{\hat{D}_1} = f(V_{out}, D2, \phi, V_{in}, V_{out}, I_{out}, R, C_{out}) \tag{4.35}$$

Similar procedure can be followed to obtain control to output transfer function $\frac{\hat{V_{out}}}{\hat{D}_2}$ and input to output transfer function $\frac{\hat{V_{out}}}{\hat{V_{in}}}$. The derived transfer function will be shown in Appendix. Also, the Matlab symbolic toolbox LiveScript used for derivation will be shown in Appendix.

4.4 Simulation Verification

The simulation was used to verify the small signal model of the FSBB converter under QCM control. The simulation was set up with PLECS simulation software. The simulation model was built as depicted in Figure 4.7. In the simulation, the steady state switching parameter was first calculated with the Min RMS ZVS calculation block, and PWM for

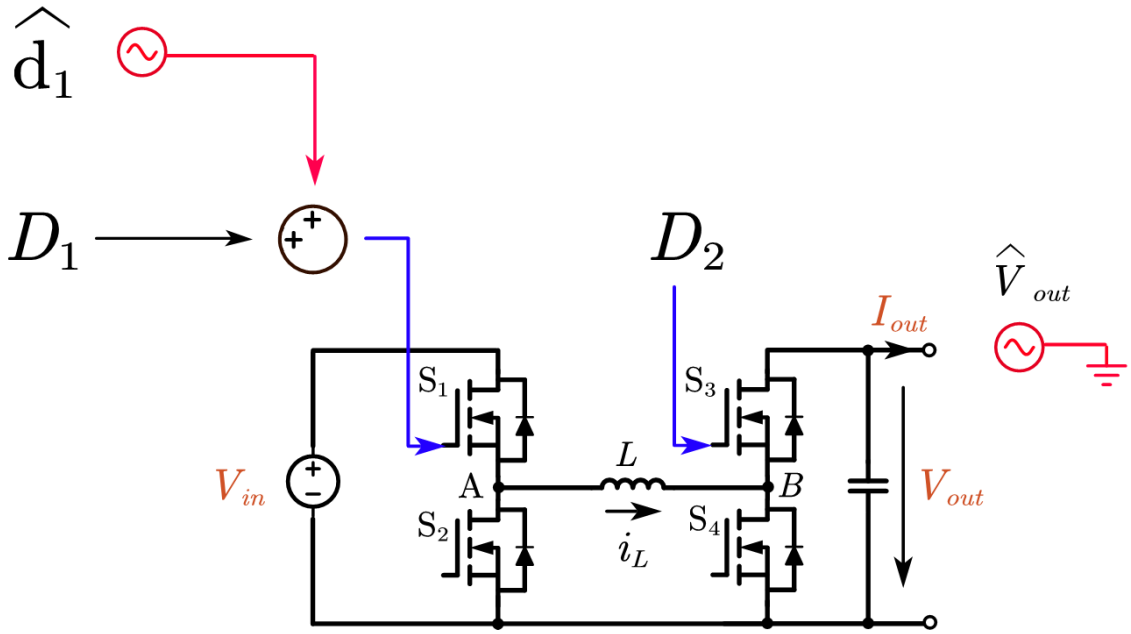


Figure 4.7: Simulation model for small signal verification

MOSFET switching was generated by the PWM generation block and sent to the gate of the corresponding MOSFET. A perturbation $\hat{d}_1$ was added to the system, and the output perturbation $\hat{V_{out}}$ was measured, and the transfer function was obtained. The small signal model under three operation zones as shown in Figure 4.8, heavy load step-up, heavy load step-down, and heavy load unit-gain zone, was verified between mathematically derived small signal model and simulation generated transfer function. The light load step-up and step-down cases will be discussed in the next section. For each operation zone, three transfer functions have been compared between the mathematical model and simulation result $\frac{\hat{V_{out}}}{\hat{D}_1}$, $\frac{\hat{V_{out}}}{\hat{D}_2}$, and $\frac{\hat{V_{out}}}{\hat{V_{in}}}$. Bode plot for each transfer function was generated up to half switching frequency from $100\,Hz$ to $10\,kHz$. The results are shown in Figure 4.9-4.11, and the test cases parameter is shown in Table. 4.1 In each figure, a sample inductor current waveform of the testing operation point is shown, and the Bode plot is presented.

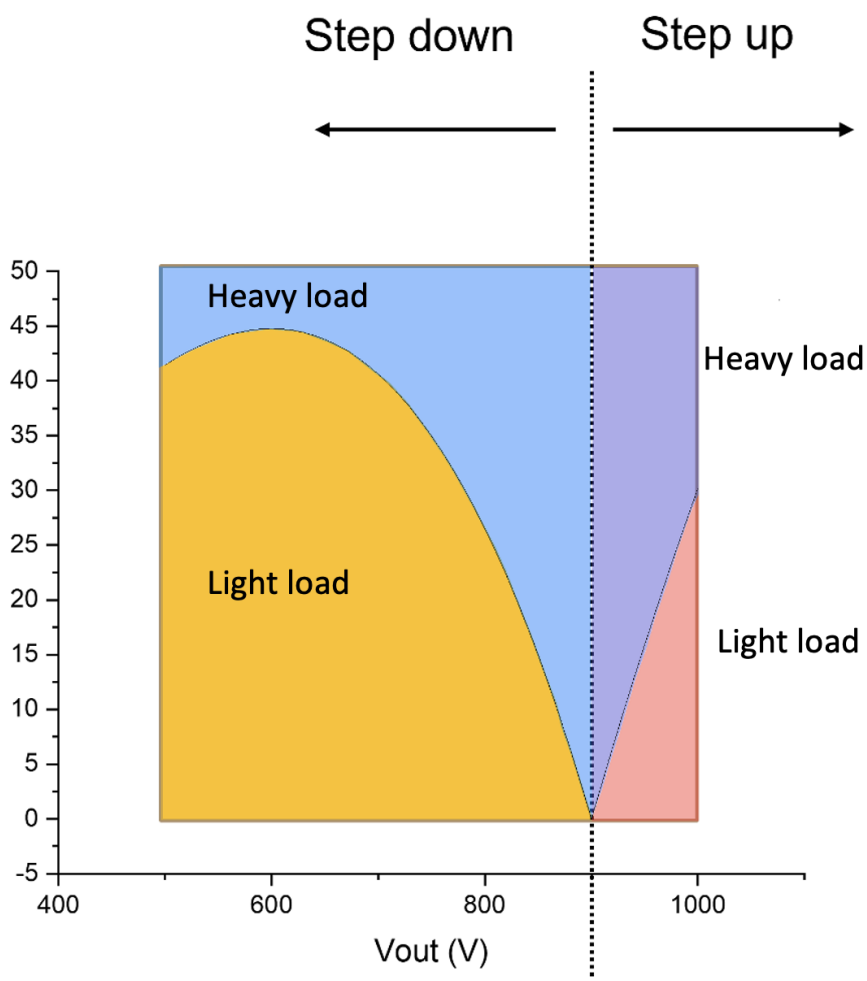


Figure 4.8: Operation zone of FSBB converter

Table 4.1: Small signal model simulation test case

Case	1	2	3
switching frequency	$20\,kHz$	$20\,kHz$	$20\,kHz$
Load condition	heavy load	heavy load	heavy load
input out put voltage ratio	step up	step down	unit gain
V_{in}	$450\,V$	$450\,V$	$450\,V$
V_{out}	$500\,V$	$350\,V$	$450\,V$
L	$33.5\,\mu H$	$33.5\,\mu H$	$33.5\,\mu H$
I_{out}	$50\,A$	$70\,A$	$30\,A$

Table 4.1: Small signal model simulation test case

Case	1	2	3
D_1	0.9611	0.7533	0.09519
D_2	0.865	0.9686	0.09519
phase shift ϕ	0.135	0.0314	0.0481
R_{load}	$10\,\Omega$	$5\,\Omega$	$15\,\Omega$
C_{out}	$150\,\mu F$	$150\,\mu F$	$150\,\mu F$

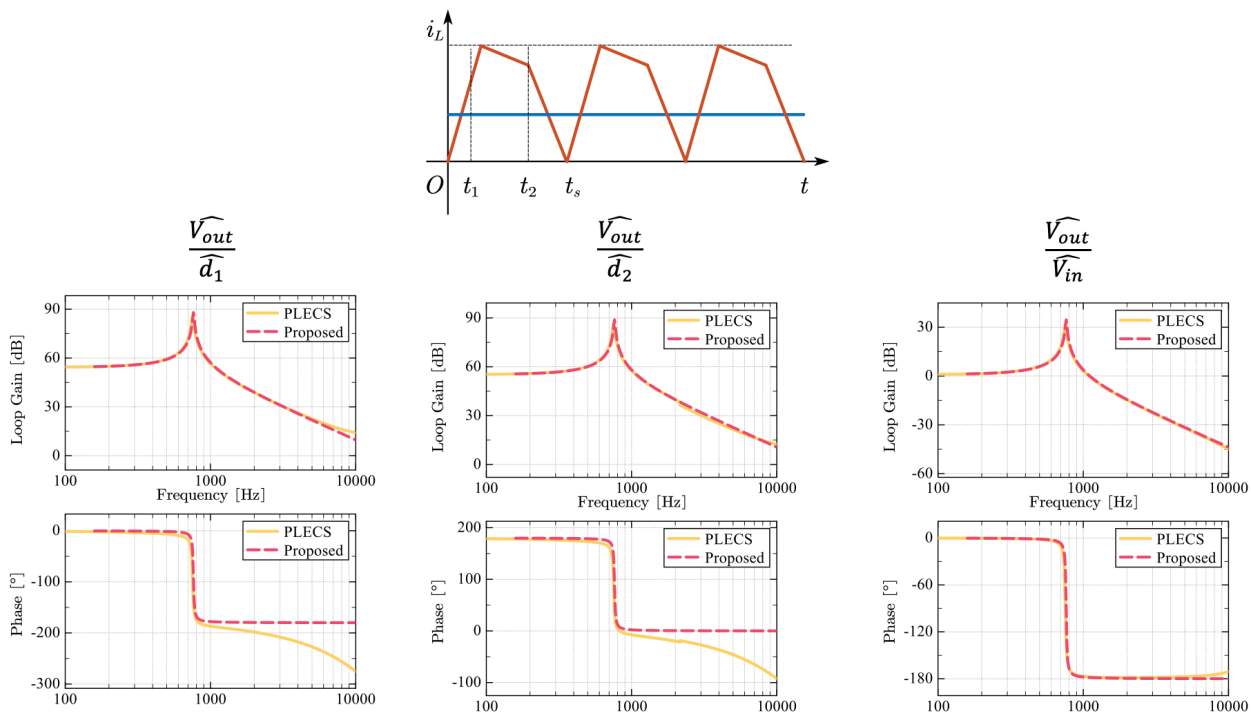


Figure 4.9: Heavy load step down transfer function bode plot

In the bode plot, the yellow line plots the simulation generated Bode plot, and the read dash line indicates the Bode plot from the derived small signal model. From the testing result, the double pole frequency of the derived small signal model matches the simulation. Both result show agreement on the gain amplitude and phase.

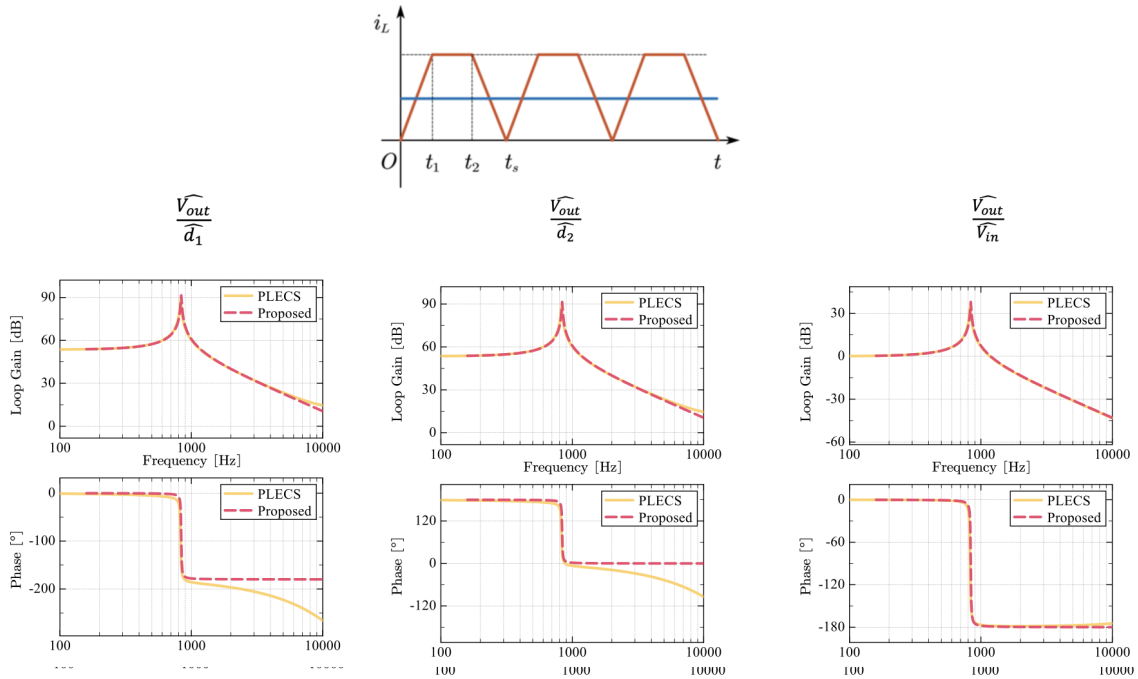


Figure 4.10: Heavy load unit gain transfer function bode plot

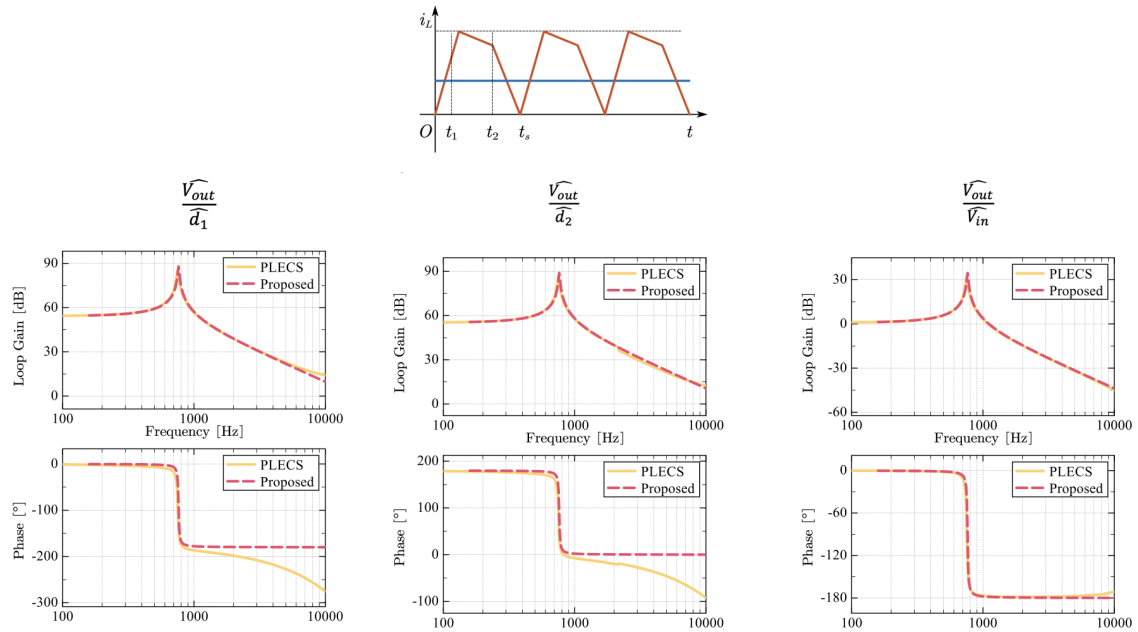


Figure 4.11: Heavy load step up transfer function bode plot

4.5 Small Signal Model with Freewheeling Period and Future Work

4.5.1 Model Double Pole Frequency Mismatch

In chapter 2, the four switching states of the FSBB converter have been discussed. When Switch S_2 and S_4 are turned on, the converter operates in freewheeling mode. The freewheeling mode is only utilized during light load regions. The small signal model of the FSBB converter has been compared with simulation under light load regions to verify the model with the freewheeling period. The testing condition is shown in Table.4.2 and the comparison is shown in Figure 4.12-4.13.

Table 4.2: Small signal model simulation test case with freewheeling period

Case	1	2
switching frequency	$20\,kHz$	$20\,kHz$
Load condition	light load	light load
input out put voltage ratio	step down	step up
V_{in}	$450\,V$	$450\,V$
V_{out}	$350\,V$	$500\,V$
L	$33.5\mu H$	$33.5\mu H$
I_{out}	$10\,A$	$10\,A$
D_1	0.3228	0.71644513
D_2	0.4151	0.64478062
phase shift ϕ	0	0.07166451
R_{load}	$35\,\Omega$	$50\,\Omega$
C_{out}	$150\,\mu F$	$150\,\mu F$

Inspecting the bode plot result of FSBB small signal model verification, a double pole frequency mismatch can be observed.

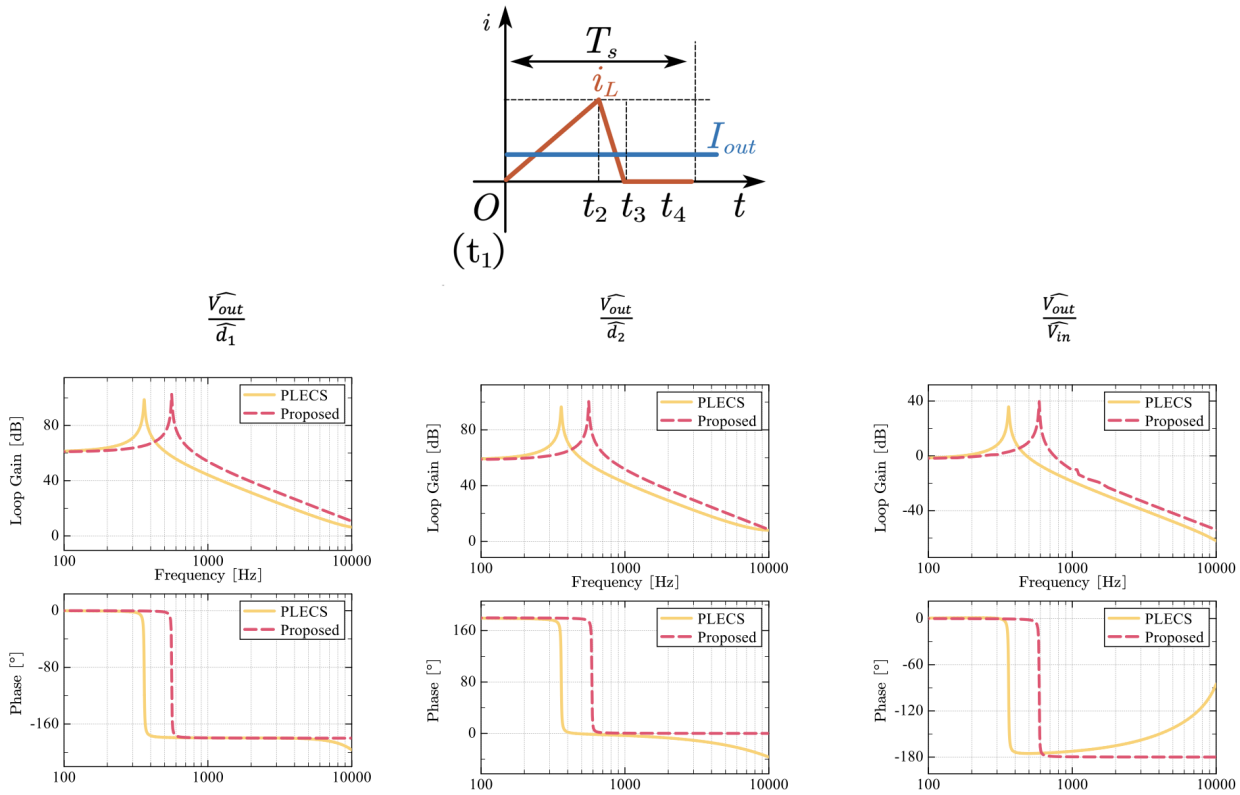


Figure 4.12: Light load step down transfer function bode plot

4.5.2 Proposed Scaling Factor of FSBB Small Signal Model with Freewheeling Period

Inspecting the switching state circuit diagram in Figure 4.14, during the freewheeling period, no voltage is applied to the inductor, the inductor shorted with switching device S_2 and S_4, therefore no energy is transferred to or from the inductor, which is similar to DCM idle period operation of converters. But different from the DCM mode of the buck/boost converter, in the freewheeling period, the inductor is neither connected to the input nor the output, which makes this a special. A discovery was made when investigating the simulation mismatch issue. When solving the small signal circuit diagram to obtain the transfer function, if a scaling factor of $D_2 + \phi$ is multiplied with the intermediate variable i_L, the derived mathematical

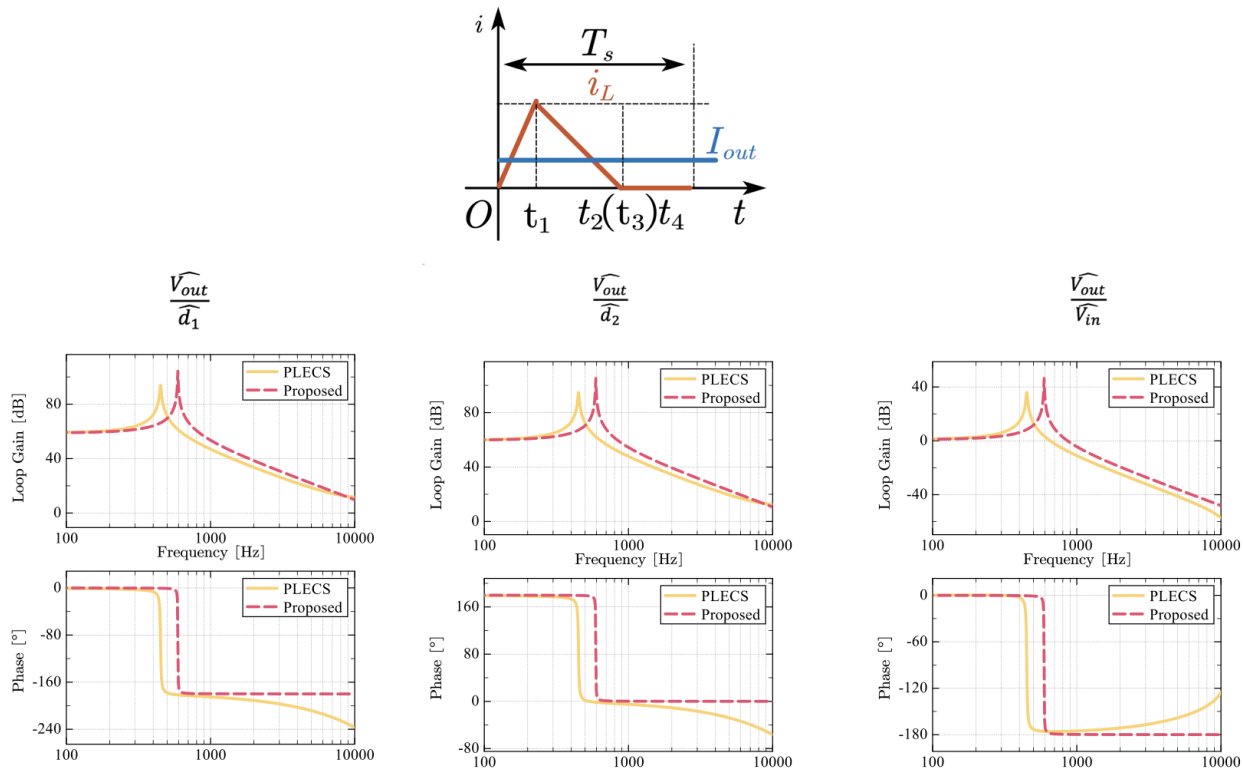


Figure 4.13: Light load step up transfer function bode plot

model can be matched with simulation, where $D_2 + \phi = 1 - D_{freewheeling}$. The Derivation process for the small signal model with the scaling factor is shown in eq. 4.36-4.38.

$$\hat{i_L} = \frac{V_{in}\,\hat{d_1} + D_1 - D_2\,\hat{V_{out}}}{L\,s} \tag{4.36}$$

The scaled small signal AC equation is

$$\hat{i}_{L,scale} = \frac{V_{in}\,\hat{d_1} + D_1 - D_2\,\hat{V_{out}}}{L\,s} \times (D_2 + \phi) \tag{4.37}$$

And the output side can be solved by using KVL

$$\frac{\hat{V_{out}}}{Z_{load}} = \frac{\partial K_4}{\partial D_1}\hat{d_1} I_L + \frac{\partial K_4}{\partial i_L}\hat{i}_{L,scale} \tag{4.38}$$

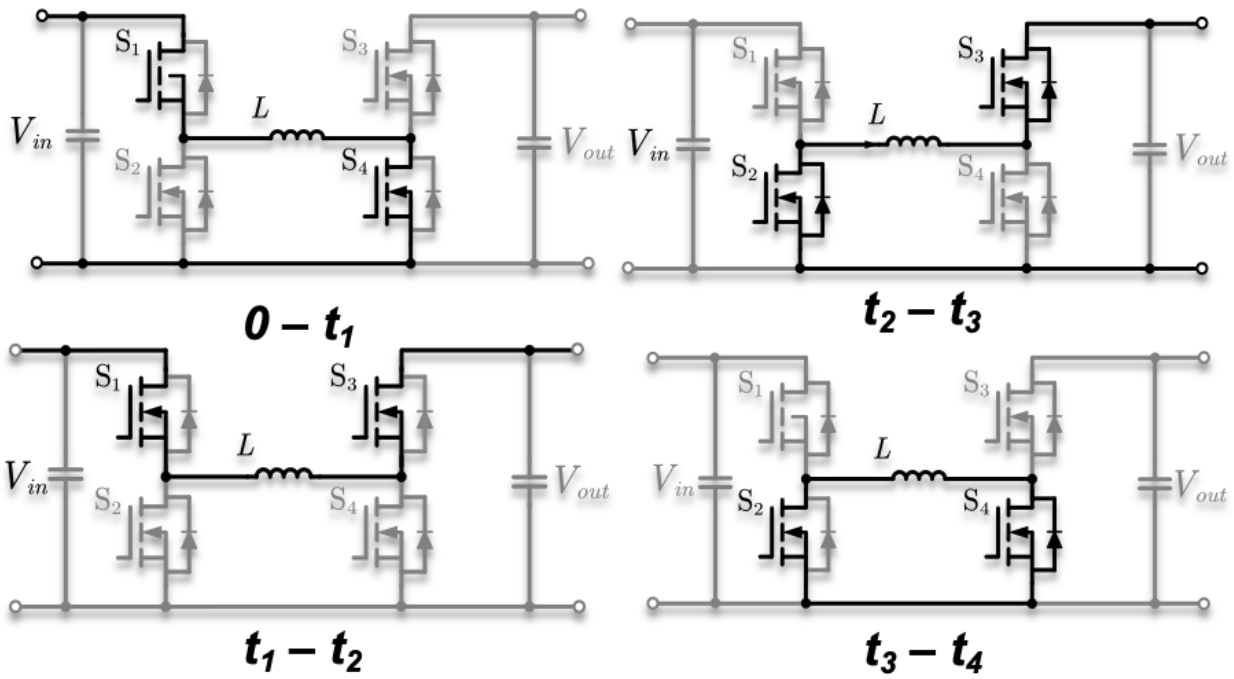


Figure 4.14: Switching state of FSBB converter

The transfer function derived from the scaling factor was compared with the simulation in Figure 4.15. The double pole frequency of the simulation matches with the small signal model with a scaling factor added. Further investigation of the small signal model and mathematical and physical explanation of small signal model freewheeling factor is required for completing the small signal model.

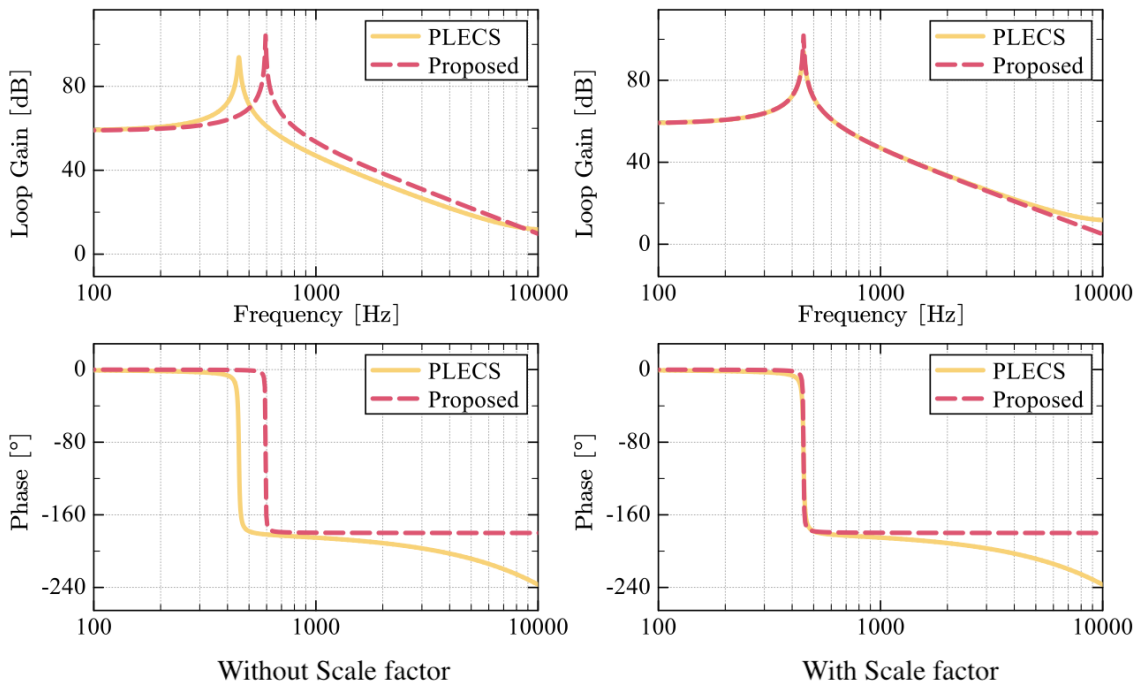


Figure 4.15: Light load step up transfer function with scale factor bode plot

4.6 Summary and Conclusion

In this chapter, previous approaches to obtaining FSBB converter CCM operation mode small signal model with small ripple approximation have been discussed. The derivation process of a new small signal that can be applied for FSBB QCM operation has been presented. The new model has been verified with simulation under heavy load conditions. Under light load conditions and a scaling factor related to the freewheeling period has been proposed and the model with a scaling factor has been verified with simulation. Further exploration of this scaling factor is required to explain the physical meaning of this scaling factor.

Appendices

Appendix A

MATLAB Program for Calculating Maximum Inductor Size for FSBB Converter in QCM

```
Full_P = 50e3/2
powerlist = [Full_P*0.25, Full_P*0.5 Full_P*0.75 Full_P]
Voutlist = 500:1:1000;
Rlist = [5 11.25 20]; % full power
Vin_list = [750 900]
flist  = []
%Calculate max power inductor needed by assuming t1 = t2
for x = 1:1:2
    Vin = Vin_list(x)/2
for outputV = 2:1:length(Voutlist)
F_s = 20e3
Ts = 1/F_s
P = 50e3/2
Vout = Voutlist(outputV)/2
L = (Vin*Vout*Ts)^2/(2*P*Ts*(Vin^2+Vin*Vout+Vout^2))
```

```
inductor_(outputV,x) = L *1e6
outputV_(outputV,x) = Voutlist(outputV)
t1 = (Vout^2* Ts)/(Vin^2+Vin*Vout+Vout^2)
t2 = (Vout^2+Vin*Vout)* Ts/(Vin^2+Vin*Vout+Vout^2)
t1_ (outputV) = t1
t2_ (outputV) = t2
duty1 = t2/Ts
duty2 = 1-duty1
duty3 = 1-t1/Ts
duty4 = t1/Ts
D1(outputV) = duty1
D2(outputV) = duty2
D3(outputV) = duty3
D4(outputV) = duty4
phase1 = 0
phase2 = t2
phase3 = t1
phase4 = Ts
delay(outputV) = phase1
delay(outputV) = phase2
delay(outputV) = phase3
delay(outputV) = phase4
end
end
%T = table(Voutlist,inductor,D1,D2,D3,D4,phase1,phase2,phase3,phase4,t1_,t2_);
% T(3:3,:)
```

```
T = table(outputV_,inductor_);

filename = 'NLLM_inductor.xlsx';

writetable(T,filename)
```

Appendix B

Min RMS ZVS Block C Language Implementation

```
  void FSBB_calc (FSBB *s) {

  long double a, b, c, d, D1, D2, t1, t2, t3;
  // used for intermediate calcualtion step
  // be sure to use long double to avoid losing accuracy during calcualtion
  //find marginal power at spcific Vin/Vout/I
long double maxI = s->Ts * s->Vin * s->Vin * s->Vout /
 (2.* s->L * (s->Vin * s->Vin + s->Vin * s->Vout + s->Vout * s->Vout));
long double Iout = 0; //I for calculation
//check if maximum power exceed
if (s->Iout > maxI) {
    //system exceed maxmum power output for ZVS
    Iout = maxI;
}
else
{
    Iout = s->Iout;
```

```
}

  //calculate current boundary between high power region and low power region
  long double marginalI;
if (s->Vin == s->Vout)
marginalI = 0;
else if (s->Vin > s->Vout)
marginalI = fabs(s->Ts * s->Vout * (s->Vin - s->Vout) / (2 * s->L * s->Vin));
else
marginalI = fabs(s->Ts * s->Vin * s->Vin * (s->Vin - s->Vout) /
 (2 * s->L * s->Vout * s->Vout));

  //check if solution in High power region
  if (Iout > marginalI) {
    //High power region
    a = (s->Ts * s->Vin * pow(s->Vout, 2)) / (s->L * (pow(s->Vin, 2)
  + s->Vin * s->Vout + pow(s->Vout, 2)));
  b = -sqrt((-2.0 * Iout * s->L * s->Ts * pow(s->Vin, 5)
  - 2.*Iout * s->L * s->Ts * pow(s->Vin, 4) * s->Vout + pow(s->Ts, 2)
   * pow(s->Vin, 5) * s->Vout - 2.*Iout * s->L * s->Ts * pow(s->Vin, 3)
   * pow(s->Vout, 2))) ;
d = s->L * (pow(s->Vin, 2) + s->Vin * s->Vout + pow(s->Vout, 2));
if (b != b) {
    b = 0;
}
c = s->L * (a + b / d);
```

```
t1 = c / s->Vin;
  D2 = ( s->Ts - t1) / s->Ts;
  D1 = D2 * s->Vout / s->Vin;
/*
a =(Ts*(double)Vin*pow(Vout,2))/(L*(pow(Vin,2)+(double)Vin*Vout+pow(Vout,2)));
b = -sqrt((-2.0*Iout*L*Ts*pow(Vin,5)-2.*Iout*L*Ts*pow(Vin,4)*Vout
+pow(Ts,2)*pow(Vin,5)*Vout-2.*Iout*L*Ts*pow(Vin,3)*pow(Vout,2))) ;
d = L*(pow(Vin,2)+Vin*Vout+pow(Vout,2));
if(b != b){
    b =0;
}
c = L*(a+b/d);
t1 = c/Vin;
D2 =( Ts - t1)/Ts;
D1 = D2*Vout/Vin;
*/
}
  else {
    //LOW power region
    //check if the converter working in step up mode or in step down mode
if (s->Vin < s->Vout) {
    // step up mode
    b = sqrt((Iout * s->Ts * (s->Vout - s->Vin)) / s->L);
a = -((sqrt(2) * s->L * b) / (s->Vin - s->Vout));
D2 = a / s->Ts;
D1 = D2 * s->Vout / s->Vin;
```

```
t1 = (a * s->Vout / s->Vin - a);
//t1 = t1-(fmod(t1,0.0000001));
}
else { // TODO: check for unit gain cases
    //step down mode
      a = 2.*s->L * s->Vout * Iout * s->Ts;
  b = s->Vin * s->Vin - s->Vin * s->Vout;
t2 = (long double)sqrt (a / b);
t3 = (t2 * s->Vin) / s->Vout;
D1 = t2 / s->Ts; //D1
D2 = t3 / s->Ts; // D2
// in low power step down mode alpha = t1 = 0
t1 = 0;
}
}
  s->D1 = D1;
  s->D2 = D2;
s->phase = t1 / s->Ts;
}
```

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