Design and Testing of a SiC-based Solid-State Bypass Switch for 1 kV Power Electronics Building Blocks

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ABSTRACT

Over the past two decades, power consumption has increased exponentially worldwide, posing new challenges to power grids to meet the load requirements. With this growing power demand, the need for efficient high-density medium-voltage (MV) power converters has increased to support flexible power distribution grids. The modular multilevel converters (MMC) became the most typical MV power converters in applications from 2010. This topology has many advantages, such as voltage scalability, excellent output performance, and low voltage ratings for switching devices. However, without the excellent reliability of the MMC, applications cannot reap these benefits.

The MMC topology comprises several series-connected submodules (typically a half-bridge or a full-bridge inverter). As a result of increased switching devices, the converter becomes vulnerable since a single device fault can disrupt the whole converter operation. Therefore, fault-tolerant strategies to replace faulty SM with a redundant SM are developed using additional bypass switches. Conventionally TRIACs and vacuum switches are employed as bypass switches that operate in the range of 2-10 microseconds.

Despite having performance advantages, MMCs are still not fully employed in aerospace and naval industries due to their enormous size. Many Power Electronics Building Blocks (PEBB)

are proposed, with size optimization, as submodules for modular converters. The PEBB1000, a 1000 V- PEBB proposed by Dr. Jun Wang, achieved a significant size reduction of 80% with a novel switching cycle control (SCC) scheme. This novel control scheme requires high switching frequency and high *di/dt*-currents for MMC operation. Due to di/dt-rate limitations, TRIAC-based switch cannot perform bypass operation. Therefore, research work has been conducted on bypass switches for PEBB1000 using wide-bandgap SiC devices.

This thesis presents the design of a SiC MOSFET-based bypass switch for PEBB1000 in MMC application. A detailed fault case analysis is presented to show the feasibility of the bypass operation for 90% PEBB-level faults. Significant variations in PEBB1000 bypass requirements are observed through SCC-based MMC simulations. Accordingly, a 1700 V, 100 A bypass switch has been designed using the anti-series topology of MOSFETs. Various specifications, such as 142 nanoseconds operation time, 500 nanoseconds bypass commutation time, and 277A transient current conduction capability, are validated through practical tests. Results prove that SiC-MOSFETs work better than TRIACs in high di/dt-current conduction and operation times. For future work, false-triggering endurance has to be analyzed for 1000 V switching voltage.

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GENERAL AUDIENCE ABSTRACT

When a building is on fire, the safety of people inside depends on the timely arrival of the fire rescue departments. Similarly, for an electrical fault, the safety of electrical systems depends on fast and secure fault protection devices.

This thesis presents work on one such fault-protection device used in the power distribution grid: solid-state bypass switch. Distribution grids supply power majorly to households and industries at the city or state level. They employ medium-voltage (MV) converters to step down the voltages to meet the distribution requirements. In MV converters, several low-voltage modules are connected in series to achieve the high-voltage power conversion.

When a fault occurs at one of the low-voltage modules in MV converters, power flow gets disrupted due to a series connection like a chain. Therefore, bypass switches are connected in parallel to low-voltage modules for an alternate power flow path. Conventionally used bypass switches have 2-10 microseconds operation time.

Recent advancements in semiconductor devices, SiC MOSFETs, allow operation times less than one microsecond. Therefore, research work has been conducted on bypass switches using SiC MOSFETs. Finally, the SiC-MOSFET based bypass switch is built and tested according to

converter requirements. Results proved that the designed switch operates in 142 nanoseconds, ten times faster than a conventional switch.

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Table of Contents

List of Figures

List of Tables

Chapter 1 Introduction

1.1 Background

Medium-voltage (MV) converters topic has been an ever-evolving research area since the 1970s due to concerns regarding their efficiency, reliability, size, and performance as they handle high powers in the range of 100s of kilowatts to megawatts. Such high-power levels demand large transformers, capacitor banks, and other passive components that are bulky and expensive. Therefore, even a small design improvement that reduces the component count or size can exponentially reduce converter costs.

In 2002, Lesnicar and Marquardt [1] introduced the idea of multi-modular converters (MMCs), where several submodules at lower voltage ratings are connected in series to achieve MV power conversion, as shown in **Figure 1 - 1**. These converters offer many other advantages, such as modularity, scalability, high efficiency, and high-quality output voltage. Due to these advantages, MMC topology is being widely employed as MV converters in grid applications.

There are many topologies in consideration for the submodule; however, the traditional half-bridge inverter and full-bridge inverter (shown in **Figure 1 - 1**) are typically used. In the MMC, each phase consists of a mid-point connected DC bus 'V_{DC}', upper arm, lower arm, and the output load. In general, both arms consist of the same number 'N' of submodules, and each submodule is a full-bridge circuit with a charged capacitor at 'V_{DC}/N' voltage. The output is connected at the mid-point between the upper arm and lower arm.

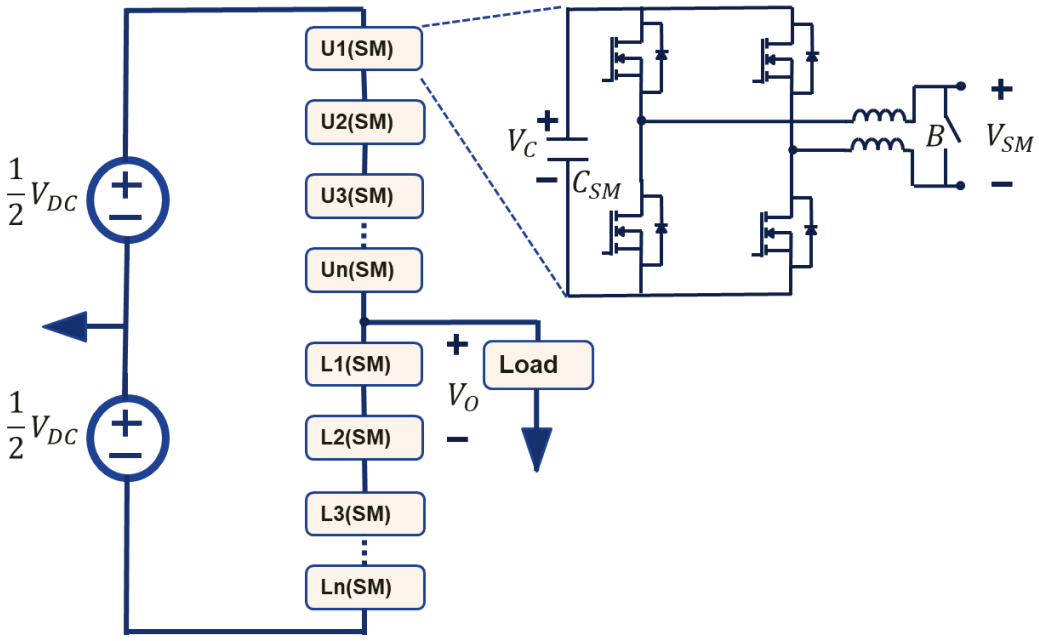

Figure 1 - 1. Modular multilevel converter structure using full-bridge submodules.

Ideally, each submodule should have a capacitor voltage of Vdc/N and should act as a constant voltage source. Based on the modulation scheme, the voltage at the load (Node M) is determined through SM capacitor insertion combinations.

An illustration of conventional MMC operation is presented by taking an MMC model with four submodules (SMs) per arm. The top arm (U1, U2, U3, and U4) and bottom arm (L1, L2, L3, and L4) consist of four SMs as shown in **Figure 1 - 2** with 1000 V charged SM capacitor and 4000 V input DC-link voltage.

At any instant, the modulation scheme inserts four out of the eight SMs into the arm. The other four SMs are kept in the bypassed state so that the total arm voltage becomes equal to the DC-bus voltage. Due to the voltage balancing, the circulating current that flows between the power supply and the SMs gets reduced.

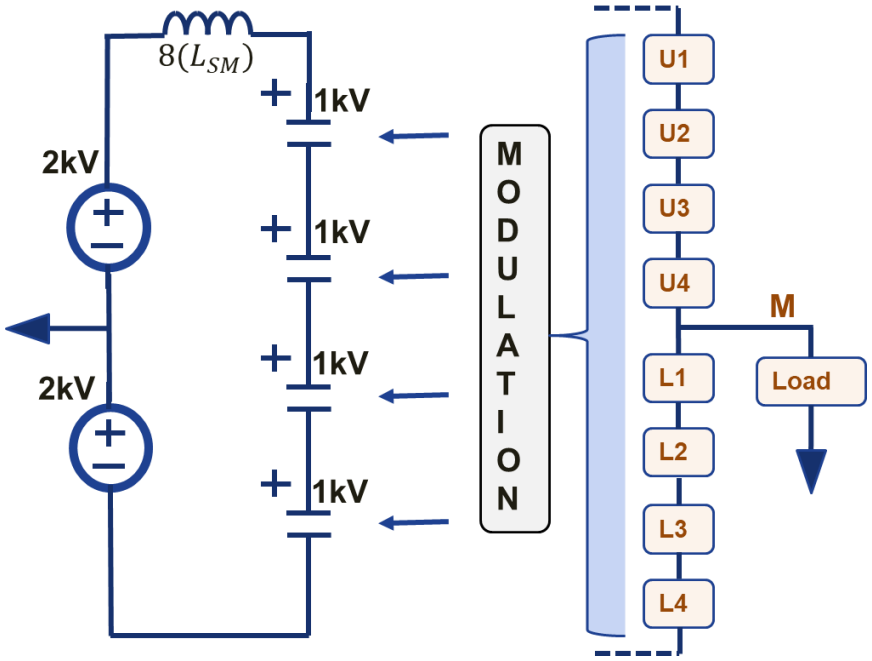

Figure 1 - 2. Conventional modulation strategy of an MMC with four SMs per arm.

SM selection is varied accordingly to adjust the voltage profile required at output node M. If U1, U2, U3, and U4 capacitors are inserted, the voltage at node M becomes -2000 V. Alternatively, if L1, L2, L3, and L4 capacitors are inserted, the voltage at node M becomes +2000 V. Likewise, -2000 V, -1000 V, 0 V,1000 V, and 2000 V are the five possible voltage levels for the MMC with four PEBBs per arm, as shown in **Figure 1 - 3**.

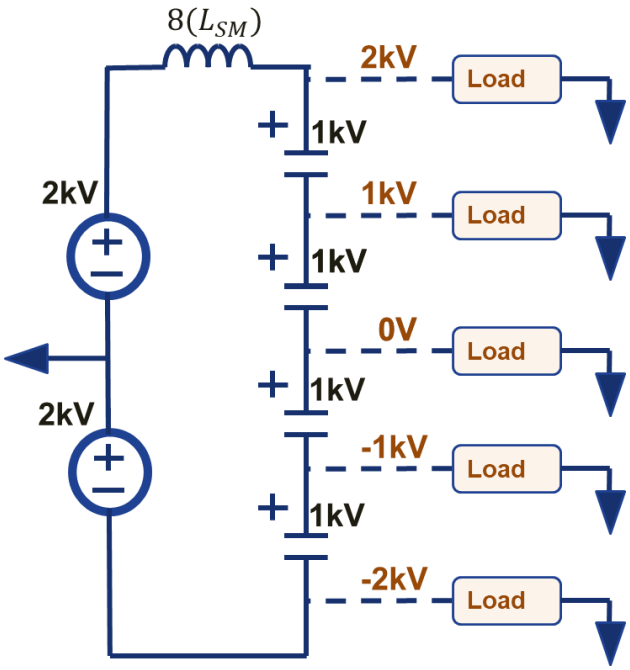

Figure 1 - 3. Output voltage levels of the MMC with four SMs per arm.

The conventional MMC application requires switching frequencies between 500 Hz and 5 kHz to achieve a high-quality voltage waveform. As mentioned earlier, SM capacitors should act like constant voltage sources to achieve output voltage with the least harmonics. However, in the application, SM capacitor voltages are varied due to the flow of arm current. Therefore, arm current is modulated to be an alternating current with both positive and negative magnitudes to ensure the charge-balancing of the SM capacitor.

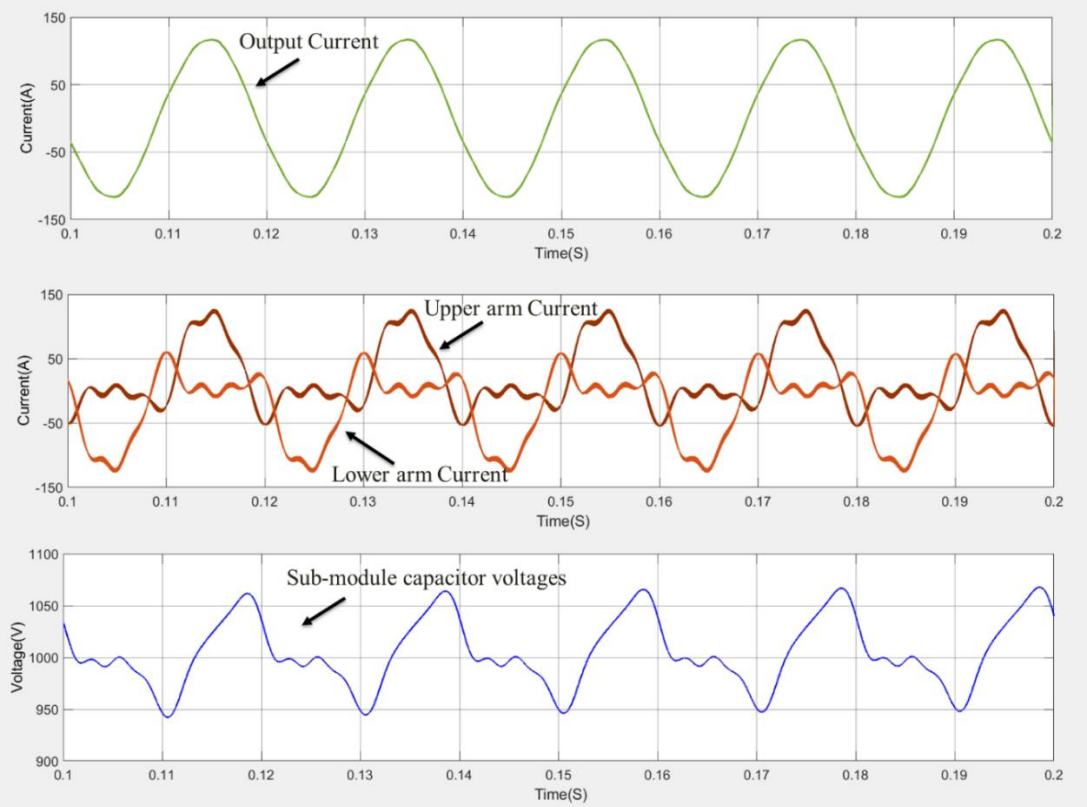

Figure 1 - 4. Simulation result of conventional MMC with four PEBBs per arm.

The MMC SIMULINK model has been developed with conventional phase-shifter carrier wave modulation (PS-CWM) [2] with an input DC-bus voltage of 4000 V and SM capacitor voltage of 1000 V. Simulation waveforms of output current, arm currents, and upper SM capacitor voltages are shown in **Figure 1 - 4.**

The positive arm current charges the upper SM capacitors and increases their voltages. Alternatively, the negative arm current discharges the upper SM capacitors and decreases their voltages. Therefore, submodule capacitance should be high enough to limit the SM capacitor voltage variation below ten percent to avoid the output voltage distortion.

1.2 MMC Bypassing Strategies

For MMC converters to be implemented in MV power grid applications, continuous operation is pivotal as they can affect the balance of grids. Regardless of the advantages of MMC, the primary concern has been the reliability of the converter as it comprises many switching devices such as IGBTs / MOSFETs in which each switch is a potential failure point. Moreover, the series connection of submodules leaves no alternative but to completely stall the converter operation even for a single SM fault. For the past 5-10 years, significant research has gone into finding alternatives to SM fault protection of the MMC. The usage of redundant SMs in each arm, which can substitute for the faulty SMs, has gained more prominence. For implementing redundant SMs, each SM should be equipped with an additional bypass switch across its terminals. After the occurrence of a fault, the controller should detect the fault location and bypass the faulty SM. Several fault-detection techniques and fault-tolerant control methods have been proposed to advance this strategy.

Some researchers [3]–[5] have proposed the cold-storage fault-tolerant methods in which redundant submodules are always in the bypassed state, with their capacitors uncharged until faults occur, as shown in **Figure 1 - 5**. When a fault occurs within a submodule, the bypass switch bypasses the faulty SM, followed by the insertion of redundant SM into the arm as a substitute. After insertion, the redundant SM capacitor gets charged from zero volts to its DC reference value. This method has drawbacks of long transient times (around 100-150 milliseconds) to settle at a new operating point.

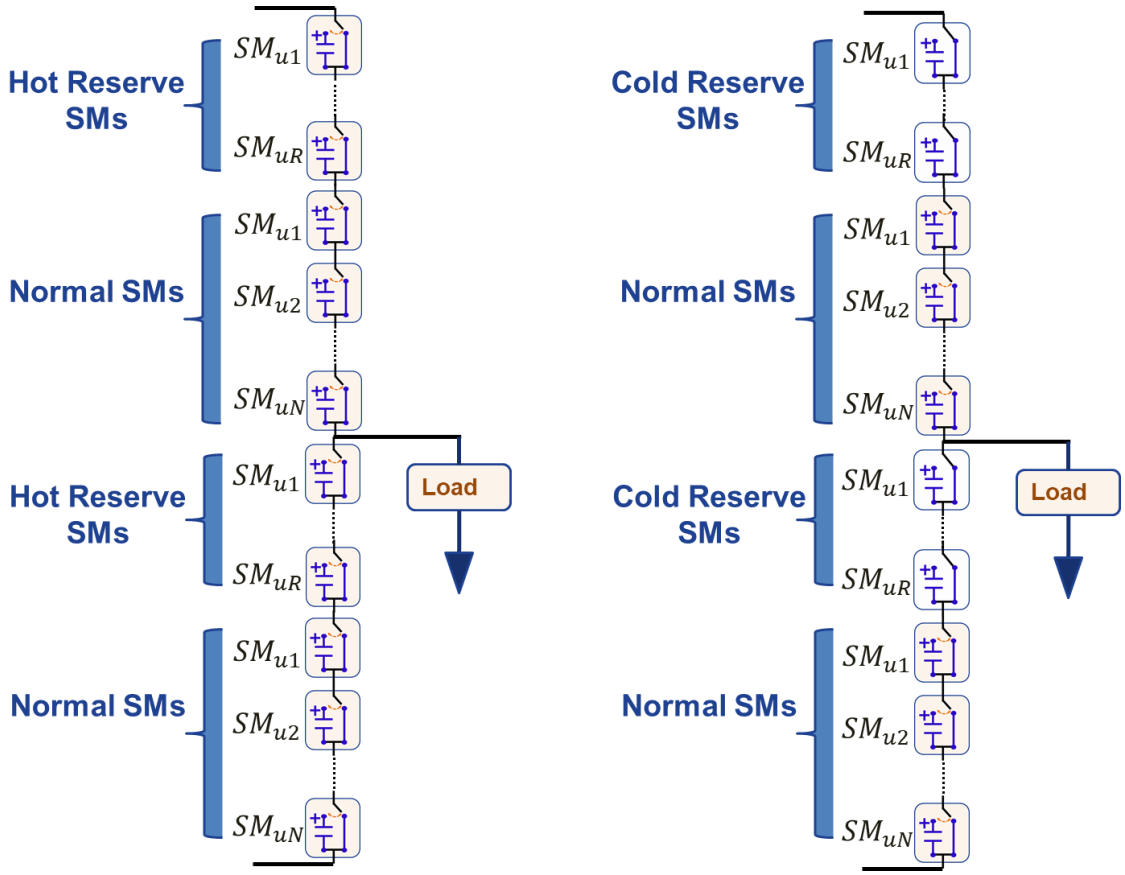

Figure 1 - 5. Hot storage and cold storage redundant SMs in the MMC.

To overcome those drawbacks, [6]–[8] proposed the hot storage method in which redundant SMs also work as normal SMs. Initially, all SM capacitors operate at a lower voltage than the reference level. When a fault occurs, the faulty SM is bypassed, and all other working SM capacitor voltages get increased to the standard reference level. This method has the advantages of using redundant SMs to their full potential along with reduced voltage stress. The transient times also got reduced to 10-50 milliseconds by implementing the hot storage method.

Even though high-bandwidth voltage and current sensors are available to monitor voltages and currents in the submodules, computational methods [9], [10] through controllers are preferred for fault detection to avoid bulky sensors. The latest computational techniques were able to detect and locate the faulty SM within 10 -15 microseconds. Due to their bidirectional conduction and

blocking capabilities, SCR thyristor-based TRIACs and vacuum switches [11], [12] are employed as external bypass switches. Since the arm current acts like a low-frequency alternating current in the conventional modulation, the *di/dt* rate of the arm currents falls in the operating range of the TRIACs. The latest features of conventional MMCs equipped with redundant SMs are surveyed and presented in **Table 1 - 1.**

Table 1 - 1. Features of Conventional MMC with redundant SMs.

Features	Submodule (Conventional)
Submodule Capacitance	700 – 3000 μF
Submodule Inductance	50 – 700 μH
Switching Frequency	500 Hz – 5 kHz
Fault Detection Time	5-10 Microseconds
Bypass Operation Time	2-5 Microseconds
Transient Times	10-50 Milliseconds
Bypass Switch	TRIAC, Vacuum Switch

1.3 Switching Cycle Control and PEBB1000

Even after using a modular approach for MMCs, the SM capacitance value is still high (milli-farads) to maintain the capacitor voltage ripple less than 10%. Available capacitors at the required voltage and currents of 1000 V and 100 A are bulky in size and occupy 75% of the SM volume, and in turn, act as a size limit for the entire multi-modular converter.

To address the size issue of passive components in MMCs, Dr. Jun Wang developed a novel modulation scheme [11], referred to as switching cycle control (SCC). This modulation scheme proposed a new charge-balancing technique through which the capacitor charge-balancing can be achieved in a switching cycle instead of a line cycle. This technique is implemented by altering the arm current polarity (positive to negative and negative to positive) in each switching period. This advancement significantly reduced the balancing charge to less than $1/10^{th}$ of the conventional modulation, reducing capacitor size to 7%.

For understanding, the MMC operation principle with switching cycle control is illustrated with four SMs per arm MMC. The top arm (U1, U2, U3, and U4) and bottom arm (L1, L2, L3, and L4) consist of four SMs with 1000 V capacitor voltage and 4000 V input DC-link voltage.

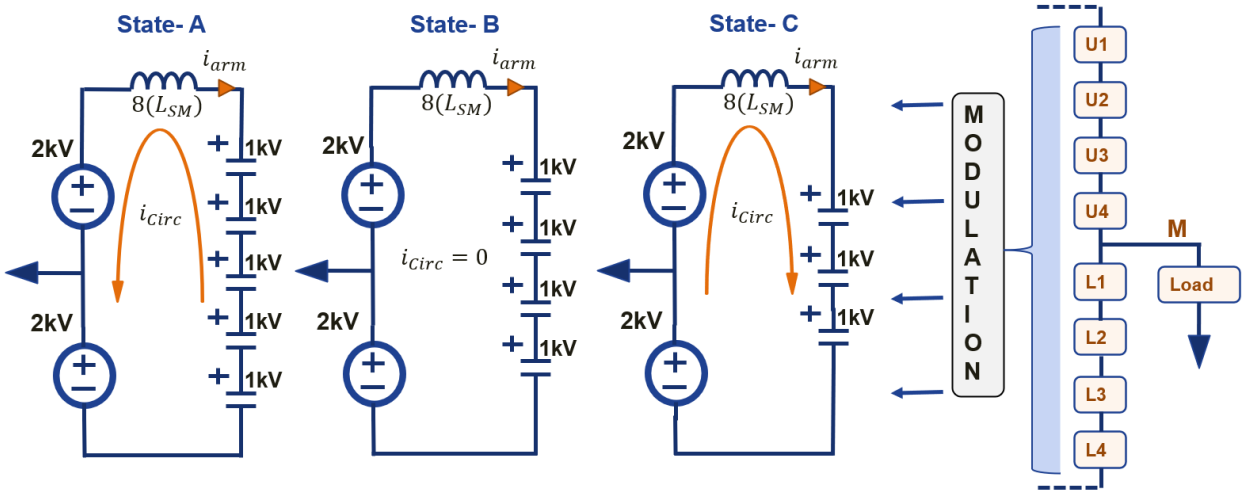

Figure 1 - 6. Modulation states of the novel switching cycle control.

Compared to the conventional modulation scheme, SCC utilizes two additional modulation states, A and C, to facilitate the arm current polarity shift, as shown in **Figure 1 - 6.** Modulation state A inserts 5 SM capacitors into the arm path, generating the total SM capacitors' voltage of 5000 V. This results in a negative voltage drop of 1000 V across the total loop inductance, and the

arm current is forced to flow into the DC power supply. On the other hand, modulation state C inserts 3 SMs into the arm path, generating the total SM capacitors' voltage of 3000 V. This leads to a positive voltage drop of 1000 V across the total loop inductance, and arm current will be forced to flow into the SMs. These additional modulation states are used to alter the arm current polarity in every switching period to balance the SM capacitor charge.

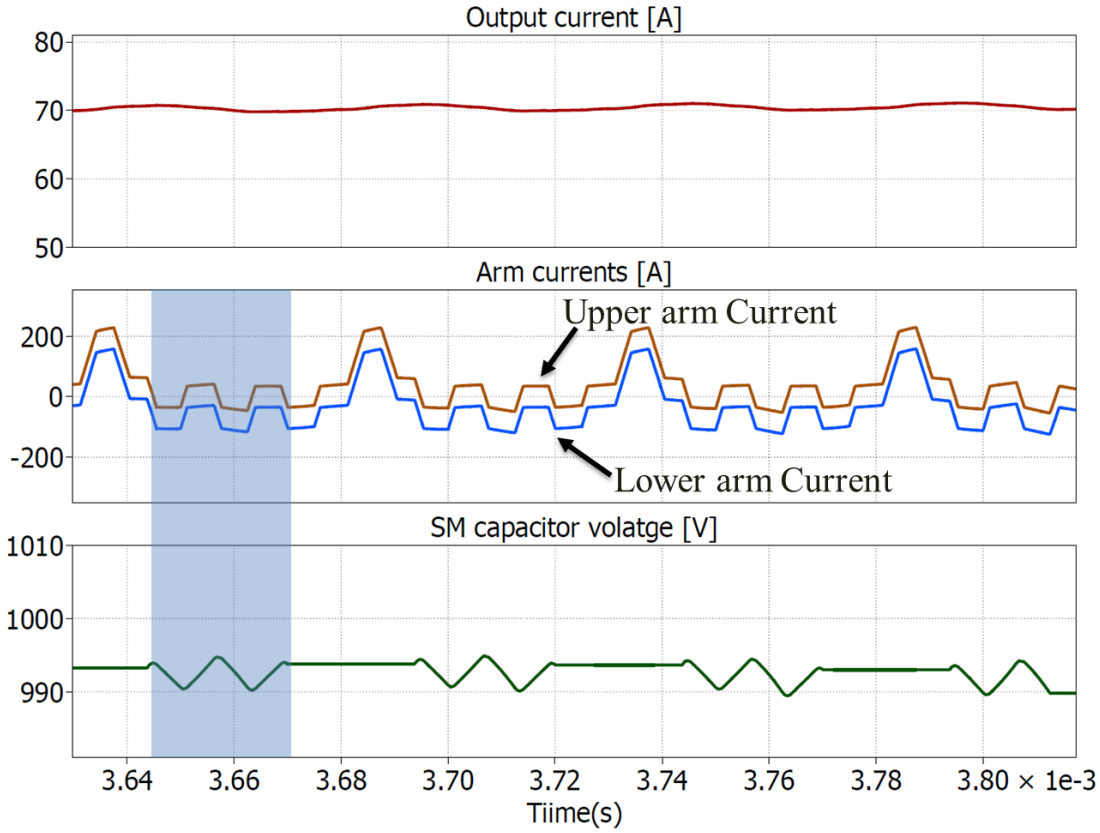

Figure 1 - 7. Simulation result of SCC- MMC with four PEBBs per arm.

The MMC PLECS simulation model has been developed with switching cycle control modulation (SCC) with 4000 V input DC-bus voltage and 1000 V SM capacitor voltage. Simulation waveforms of output current, arm currents, and upper SM capacitor voltages are shown in **Figure 1 - 7.**

The 1kV Power Electronics Building Block (PEBB1000) was built to validate the SCC modulation [12], equipped with advanced features such as gate driver embedded Rogowski Coil Current Sensor and high bandwidth sensors. **Figure 1 - 8** shows the internal structure of the PEBB1000. Using the PEBB1000 as an SM, the MMC operation has been validated for a converter with one PEBB/arm.

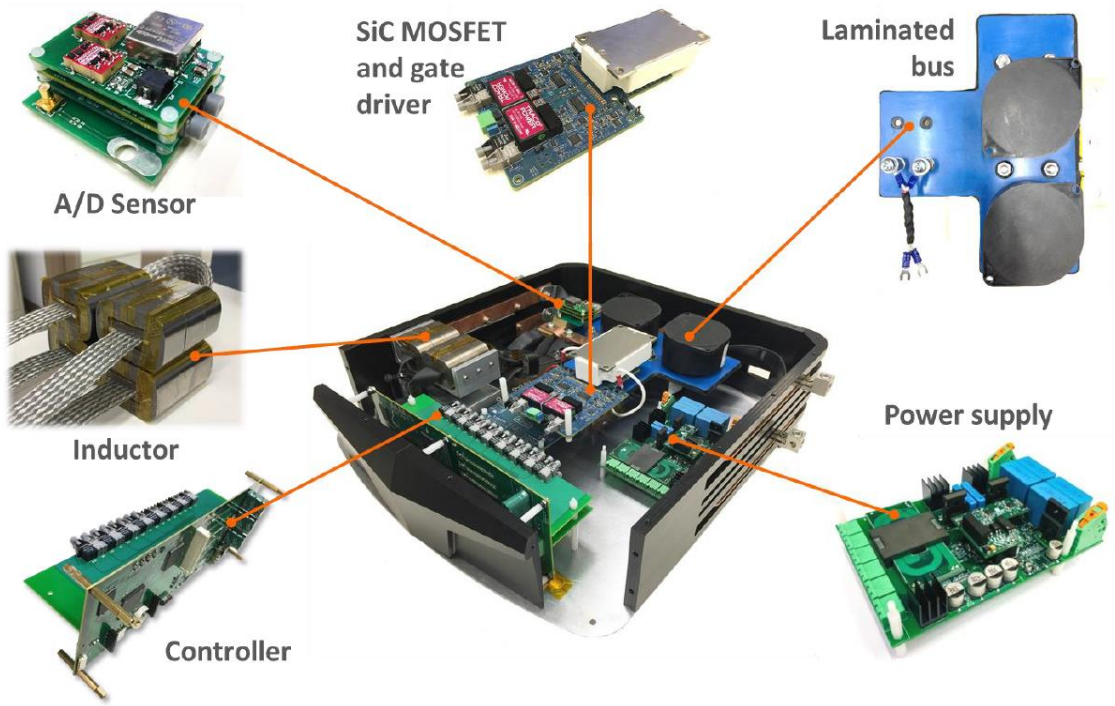

Figure 1 - 8. The internal structure of the Power Electronics Building Block 1000.

Experimental validation of switching cycle control for SCC-based MMC with multiple SMs per arm is still in progress. Extending from 1 PEBB/arm to multiple PEBBs/arm MMC raises concerns about the design of the solid-state bypass switch for fault protection. A feature comparison between the conventional SMs and the PEBB1000 SMs is presented in **Table 1 - 2.**

Table 1 - 2. Features comparison between conventional SM and PEBB1000.

Features	Submodule (Conventional)	Submodule (PEBB1000)
Submodule Capacitance	700 – 3000 μF	45 – 75 μF
Submodule Inductance	50 – 700 μH	2 – 5 μH
Switching Frequency	500 Hz – 5 kHz	10 kHz- 60 kHz
Fault Detection Time	5-10 Microseconds	0.2 – 0.5 Microseconds
Submodule Bypass Turn-on	2-5 Microseconds	-
Bypass Switch	TRIAC, Vacuum Switch	-
Transient Times	50-100 Milliseconds	-

Advancements of the PEBB1000 are apparent from **Table 1 - 2**, in that PEBB capacitance and inductance values became smaller than 20% of those of conventional SM. Apart from that, PEBB1000 high-speed fault detection occurs within 500 nanoseconds. High switching frequency ensures excellent output voltage quality with low harmonics. The bypass switch should have a similar operating speed to take full advantage of this high-speed fault detection. However, commercially available TRIACs and vacuum switches have operating times above two microseconds.

1.4 Motivation

Major concerns for TRIACs to be used as bypass switches for the PEBB1000 are presented below.

1. Dv/dt-voltage rate endurance of TRIACs

   Commercially available TRIACs at 1000V rating have acceptable OFF state *dv/dt*-voltage rates up to 5 V/ns. This *dv/dt*-voltage rate is acceptable at frequencies below 5 kHz as conduction losses are more at low frequencies. Since PEBB1000 is designed to operate at frequencies above 10 kHz, a high *dv/dt*-voltage rate is essential for reducing switching losses. The PEBB1000 gate driver can turn-on SiC MOSFETs at a speed of 30 V/ns, which is way beyond the reach of the TRIACs endurance region.

2. Turn-on

   The device starts conducting the current before spreading across the entire junction region when the TRIAC turns on. The high *di/dt* currents can overheat certain spots in the junction region and damage the device [13] in the turn-on interval. Therefore, TRIACs are not suitable for conducting high *di/dt* arm currents in SCC-MMC.

Moreover, fault detection time in the PEBB1000 has been improved below 500 ns, using Rogowski Coil Current Sensor (RCCS) and high-speed fiber-optic communication. Fault protection devices should also have similar operation times to utilize these technical advancements. The fastest turn-on times of advanced TRIACs are still around a few microseconds. Therefore, it is beneficial to consider faster-operating devices for the bypass switch.

3. Turn-off

Unlike IGBT and MOSFETs, the thyristor cannot be autonomously turned-off using gate control. Instead, the load current flowing through the TRIAC should be brought below the holding current and sustained until the TRIAC is turned-off. The simulated PEBB10000 arm currents do not support the holding-current requirements for TRIAC turn-off. Therefore, it may not be possible to turn-off the TRIAC switch once turned-on until the MMC operation stalls.

For the above reasons, TRIACs might not be the best option as a bypass switch for the PEBB1000. Therefore, more advanced wide-bandgap devices such as IGBTs and MOSFETs should be explored against PEBB1000 bypass switch requirements. SiC MOSFETs had already been in use as bidirectional switches in matrix converters applications [14]–[16], solid-state circuit breakers [17], [18]. This thesis presents the feasibility of SiC MOSFETs for the MMC bypass switch application and validated by experiments.

1.5 Thesis Outline

In Chapter 2, the fault study to derive the feasibility of bypass operation against PEBB1000 faults is presented. The bypass switch design requirements extracted through SCC-MMC simulations are discussed in Chapter 3. The design of the bypass switch is discussed in Chapter 4, which includes device selection, topology selection, and gate driver PCB design. Chapter 5 presents the testing results of the bypass switch against the design targets. Chapter 6 concludes the overall summary and future work.

Chapter 2 Fault Case Analysis and Bypass Feasibility

2.1 Background

As the bypass switch has to be designed for protection against faulty PEBBs, it is essential to understand the PEBB fault possibilities. The PEBB1000 was designed with a full-bridge inverter topology, which provides advantages such as bidirectional insertion and DC-link short circuit fault blocking in the MMC. However, having four SiC MOSFETs in the full-bridge topology leads to numerous fault possibilities per PEBB compared to the half-bridge topology. Most fault-tolerant MMC strategies were developed, considering half-bridge structure. Only some research [21], [22] has been conducted on full-bridge topology fault analysis and tolerant strategies.

Various faults can occur within a PEBB due to maloperation of gate drivers, SiC MOSFETS, and heatsinks. For example, the thermal resistance of the heatsink gets increased abruptly when cooling mechanisms do not work correctly. This increased thermal resistance leads to a sharp rise in MOSFET junction temperatures, eventually burning out the modules and resulting in permanent failure. However, in MOSFETs, they can be damaged for many reasons, including over-voltage, high junction temperatures, and improper voltage isolation. As SiC MOSFET switch failures directly impact MMC operation, conducting a PEBB-level fault study and its impacts is more beneficial.

2.2 PEBB Switching Faults

For the fault case analysis, three functional states of MOSFET are assumed, namely "Working," "Open," and "Short," as shown in **Figure 2 - 1,** -- as an indication of MOSFET operating status.

"Working" represents the regular operation of the MOSFET, where it can be either turned-on or OFF, driven and controlled by the gate driver.

"Open" represents the open-circuit failure, where MOSFET has no connection between its drain and source terminals, unresponsive to gate driver control.

"Short" represents the short-circuit failure, where the MOSFET drain and source terminals are shorted, unresponsive to gate driver control.

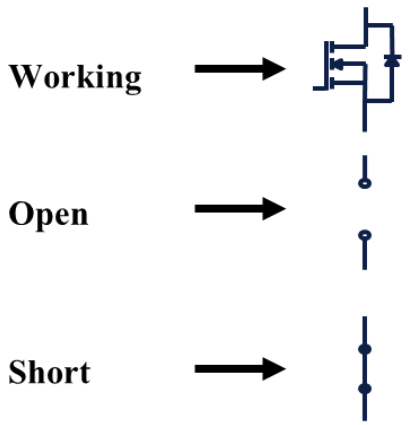

Figure 2 - 1. Operating States of the SiC MOSFET as the switch.

For ease of indexing, the full-bridge circuit is referred to as two half-bridges, A and B, as shown in **Figure 2 - 2.**

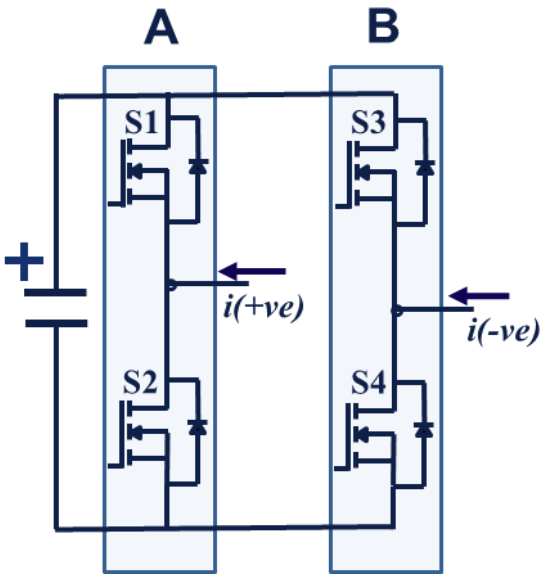

Figure 2 - 2. Full-bridge topology.

Table 2 - 1. Faulty states in a half-bridge topology.

Fault States (Half-Bridge)	S(Top)	S(Bottom)
1	Working	Working
2	Working	Open
3	Working	Short
4	Open	Working
5	Open	Open
6	Open	Short
7	Short	Working
8	Short	Open
9	Short	Short

According to the MOSFET operating states described, nine faulty states are possible in a half-bridge, as shown in **Table 2 - 1.** These nine faulty states can be attributed either to half-bridge A or B, indicated as A1-A9 and B1-B9 in **Table 2 - 2,** respectively.

Table 2 - 2. Indexed faulty states in half-bridges A and B.

Faulty States	
Half-Bridge(A)	**Half-Bridge(B)**
A1	B1
A2	B2
A3	B3
A4	B4
A5	B5
A6	B6
A7	B7
A8	B8
A9	B9

Table 2 - 3. Possible faulty states in a full-bridge topology.

Faulty States in a Full-Bridge Topology								
A1-B1	A2-B1	A3-B1	A4-B1	A5-B1	A6-B1	A7-B1	A8-B1	A9-B1
A1-B2	A2-B2	A3-B2	A4-B2	A5-B2	A6-B2	A7-B2	A8-B2	A9-B2
A1-B3	A2-B3	A3-B3	A4-B3	A5-B3	A6-B3	A7-B3	A8-B3	A9-B3
A1-B4	A2-B4	A3-B4	A4-B4	A5-B4	A6-B4	A7-B4	A8-B4	A9-B4
A1-B5	A2-B5	A-B5	A4-B5	A5-B5	A6-B5	A7-B5	A8-B5	A9-B5
A1-B6	A2-B6	A3-B6	A4-B6	A5-B6	A6-B6	A7-B6	A8-B6	A9-B6
A1-B7	A2-B7	A3-B7	A4-B7	A5-B7	A6-B7	A7-B7	A8-B7	A9-B7
A1-B8	A2-B8	A3-B8	A4-B8	A5-B8	A6-B8	A7-B8	A8-B8	A9-B8
A1-B9	A2-B9	A3-B9	A4-B9	A5-B9	A6-B9	A7-B9	A8-B9	A9-B9

The permutations between A1-A9 and B1-B9 further gave rise to 81 individual faulty states, as presented in **Table 2 - 3.** A detailed analysis is conducted for all eighty-one faulty states. As an illustration, the analysis of “A1-B1” and “A2-B1” is presented to show the methodology followed.

A1-B1 (Normal Operation)

A1-B1 is the only functional case in which all MOSFETs are in working condition. The gate driver can either insert or bypass the PEBB capacitor into the MMC path according to the modulation scheme.

Figure 2 - 3 shows the current paths according to switching modulation. Switches S1-S3 or S2-S4 shall be turned-on to keep the PEBB in bypassed mode. For positive capacitor insertion, switches S1-S4 shall be turned-on. On the contrary, switches S2-S3 shall be turned-on for negative capacitor insertion. The modulation schemes strictly avoid the turn-on of switches S1-S2 or S3-S4 as they short the SM capacitor, leading to a dangerous shoot-through event.

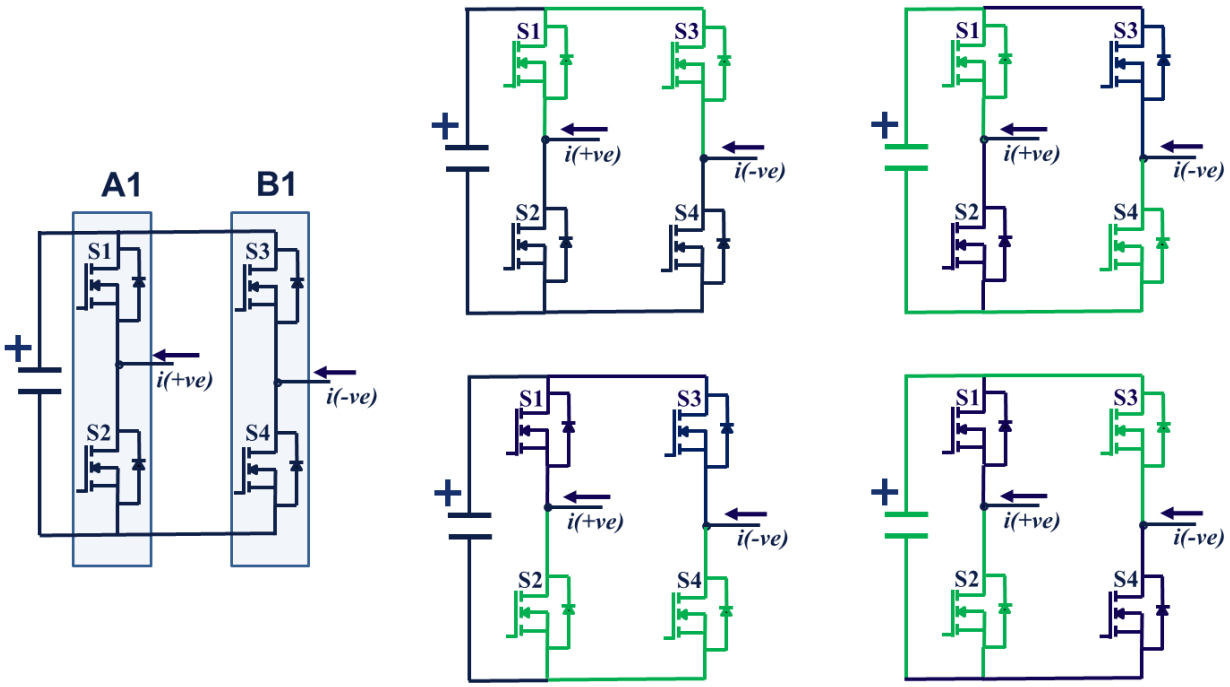

Figure 2 - 3. Current paths according to modulation in normal operation.

In the capacitor inserted states, the polarity of arm currents determines the charging and discharging of the capacitor. **Table 2 - 4** summarizes the effects of modulation states on capacitor voltage and PEBB states, according to arm current direction.

Table 2 - 4. Summary of PEBB states versus modulation in normal operation.

Arm Current	Switching States	Capacitor Voltage	PEBB
Positive	S1, S4	Increases	Inserted(+ve)
	S2, S3	Decreases	Inserted(-ve)
	S2, S4	Constant	Bypassed
	S1, S3	Constant	Bypassed
Negative	S1, S4	Decreases	Inserted(+ve)
	S2, S3	Increases	Inserted(-ve)
	S1, S3	Constant	Bypassed
	S2, S4	Constant	Bypassed

A2-B1 (Faulty Operation)

The A1-B2 faulty state represents the condition when switches S1, S3, and S4 are working, whereas the S2 switch is in open-circuit failure, as shown in **Figure 2 - 4.**

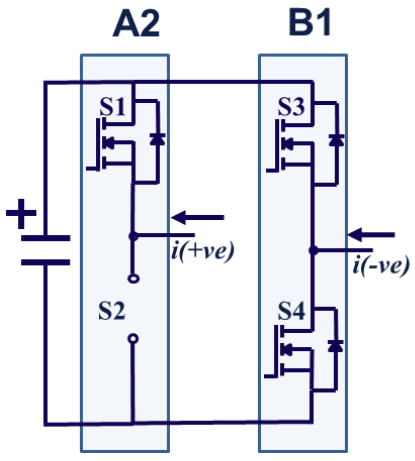

Figure 2 - 4. A2-B1 faulty state of the full-bridge topology.

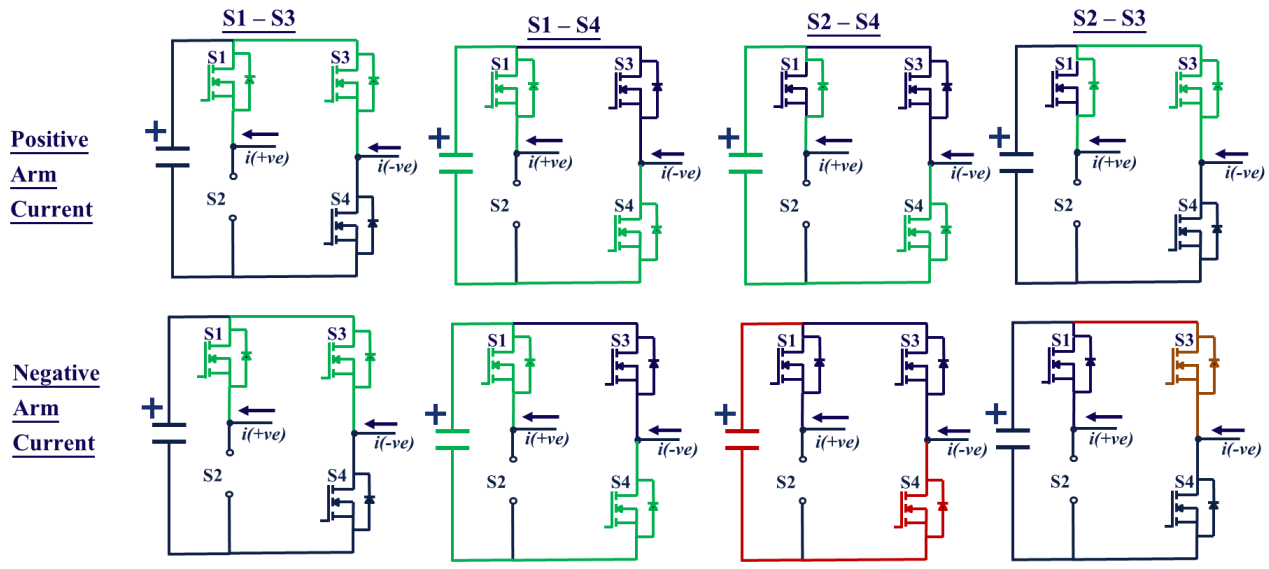

Figure 2 - 5. Current paths according to modulation in faulty operation.

In best practice, the gate driver should shut down the PEBB operation as soon as the fault gets detected. However, the gate driver is assumed to continue its modulation (as in normal operation) to estimate the worst-case impacts on MMC. **Figure 2 - 5** shows the current paths in A2-B1 according to switching modulation. Deviations are observed in the arm current paths and PEBB states as compared to normal operation. There is no path available in modulation states S2-S3 and S2-S4 for negative arm current to flow, and the PEBB entered blocking mode. The summary of A2-B1 is presented in **Table 2 - 5** to show the comparison with A1-B1.

Table 2 - 5. Summary of PEBB states according to modulation in faulty operation.

Arm Current	Event	Switching States	Capacitor Voltage	PEBB
Positive	1	S1, S4	Increases	Inserted(+ve)
	2	S2, S3	Constant	Bypassed
	3	S2, S4	Increases	Inserted(+ve)
	4	S1, S3	Constant	Bypassed
Negative	1	S1, S4	Decreases	Inserted(+ve)
	2	S2, S3	Constant	Blocking
	3	S1, S3	Constant	Bypassed
	4	S2, S4	Constant	Blocking

The analysis has been conducted on all the 80 faulty states using the same analytical approach. A full-bridge PEBB can have four major MMC modes: blocking mode, bypassing mode, positive insertion mode, and negative inserted mode. Any working or faulty states of switches can only result in one of these four PEBB states, as shown in **Figure 2 - 6.**

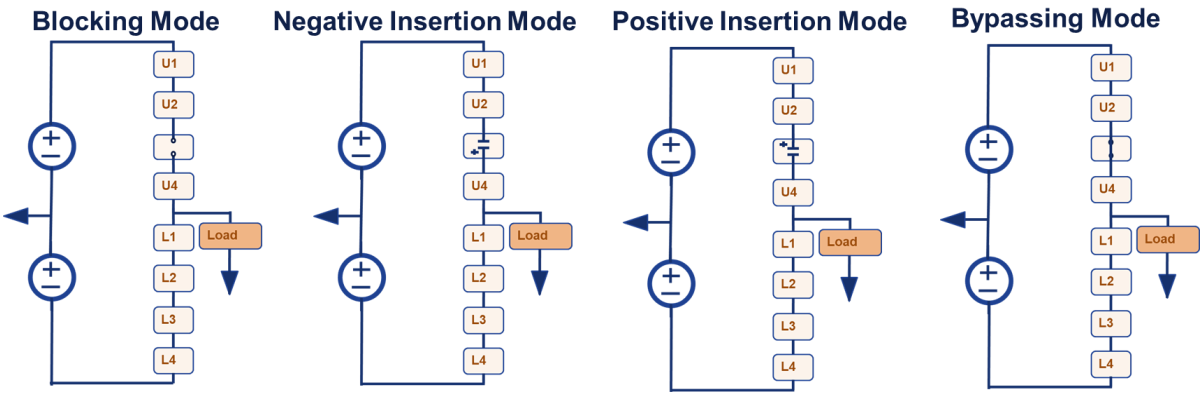

Figure 2 - 6. Current paths according to modulation in faulty operation.

From fault case analysis of all 80 faulty states, segregation of faulty states has been made based on their deviated PEBB states from normal operation, as shown in **Table 2 - 6.** The table shows that 44 faulty states (>50%) can result in the blocking mode of the PEBB, and 26 faulty states can result in the bypassing mode of the PEBB.

The shoot-through event, where the PEBB capacitor gets shorted through S1-S2 or S3-S4 switches, can occur in the table's 42 faulty states highlighted in red. The effects of shoot-through events can be fatal, leading to fire casualty by burning the power modules. [23] Dr. Jun Wang developed the embedded Rogowski Coil Current Sensor (RSCS) into the PEBB1000 gate driver for shoot-through prevention. This embedded current sensor directly senses the current flowing through the MOSFETs and informs the PEBB1000 gate driver.

Table 2 - 6. Impact-based segregation of all full-bridge faulty states.

Blocking	Inserted (-ve)	Inserted(+ve)	Bypassed
(A1-B2), (A1-B4), (A1-B5), (A2-B1), (A4-B1), (A5-B1), (A2-B2), (A2-B4), (A2-B5), (A2-B6), (A2-B8), (A4-B2), (A4-B4), (A4-B5), (A4-B6), (A5-B2), (A5-B4), (A5-B5), (A5-B6), (A5-B8), (A6-B4), (A6-B5), (A8-B2), (A8-B4), (A8-B5), (A9-B3), (A4-B8), (A6-B2), (A2-B9), (A3-B2), (A3-B4), (A3-B5), (A4-B3), (A4-B7), (A4-B9), (A5-B3), (A5-B7), (A5-B9), (A7-B2), (A7-B4), (A7-B5), (A9-B2), (A9-B4), (A9-B5)	(A1-B8), (A6-B1), (A6-B8), (A3-B7) (A6-B7)	(A8-B6) (A1-B6), (A8-B1) (A7-B3) (A7-B6)	(A6-B6), (A8-B8) (A1-B3), (A1-B7), (A1-B9), (A3-B1), (A7-B1), (A9-B1), (A2-B3), (A2-B7), (A3-B3), (A3-B6), (A3-B8), (A3-B9), (A6-B3), (A6-B9), (A7-B7), (A7-B8), (A7-B9), (A8-B3), (A8-B7), (A8-B9), (A9-B6), (A9-B7), (A9-B8), (A9-B9),
28 + 16 (44)	3+2 (5)	3+2(5)	2+24(26)

When a short circuit fault happens at the bottom switch, the corresponding top switch is turned-off quickly (within 500 nanoseconds) by the gate driver using the RCCS feedback. This breaks the current path for capacitor discharge and prevents shoot-through events. The body diode of the top switch enters a reverse-biased state due to an anti-parallel connection with the PEBB capacitor. Therefore, the top switch can be considered an open circuit, and the faulty state of the half-bridge becomes identical to faulty state #6 in **Table 2 - 1.** Similarly, for a short circuit fault at the top switch, the bottom switch is turned-off by the gate driver and considered an open circuit, identical to faulty state #8 in **Table 2 - 1**. These variations in topologies due to RCCS protection are shown in **Figure 2 - 7.**

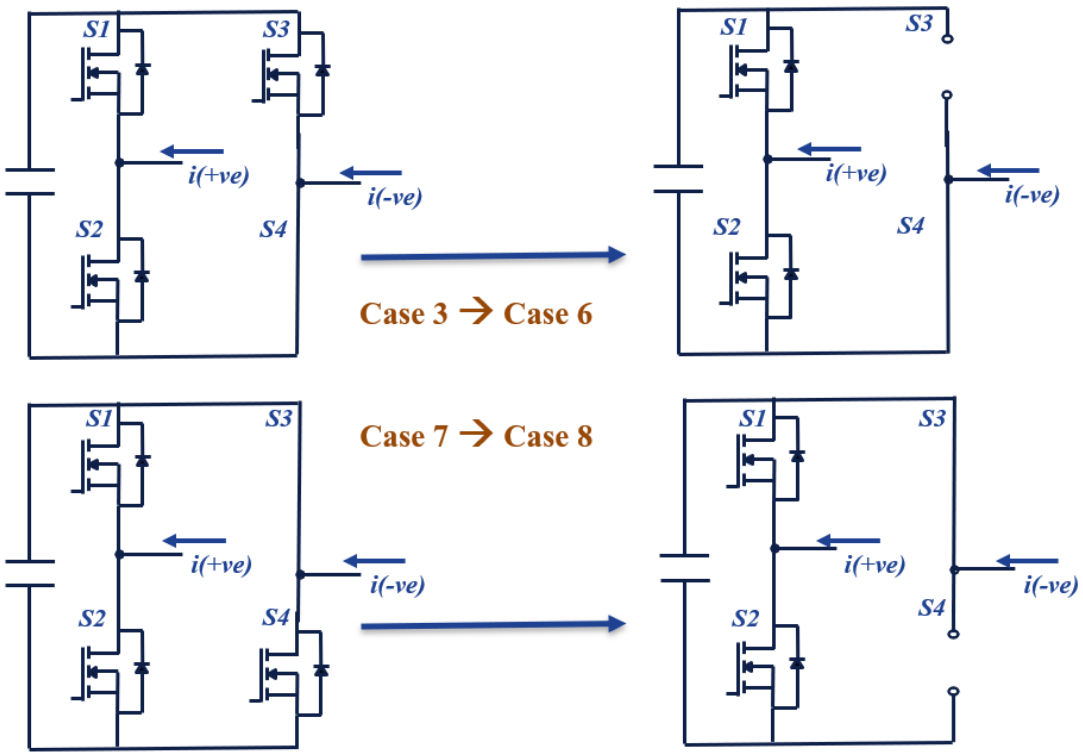

Figure 2 - 7. Changes in faulty states due to RCCS gate driver protection.

Several shoot-through events have been prevented by applying the RCCS modifications in the fault case analysis. The revised faulty state segregation after RCCS modifications is presented in **Table 2 - 7.**

Table 2 - 7. Impact-based segregation of all full-bridge faulty states with RCCS.

Blocking	Inserted (-ve)	Inserted(+ve)	Bypassed
(A1-B2), (A1-B4), (A1-B5), (A2-B1), (A4-B1), (A5-B1), (A2-B2), (A2-B4), (A2-B5), (A2-B6), (A2-B8), (A4-B2), (A4-B4), (A4-B5), (A4-B6), (A5-B2), (A5-B4), (A5-B5), (A5-B6), (A5-B8), (A6-B4), (A6-B5), (A8-B2), (A8-B4), (A8-B5), (A4-B8), (A6-B2), (A2-B3), (A2-B7), (A3-B4), (A3-B5), (A4-B3), (A5-B3), (A7-B2), (A7-B4), (A7-B5), (A5-B7), (A3-B2), (A4-B7), (A2-B9), (A4-B9), (A5-B9), (A9- B2), (A9-B4), (A9-B5)	(A1-B8), (A6-B1), (A6-B8), (A3-B1), (A1-B7), (A3-B7), (A3-B8), (A6-B7),	(A8-B6) (A1-B6), (A8-B1), (A1-B3), (A7-B1), (A7-B6), (A8-B3), (A7-B3)	(A6-B6), (A8-B8), (A3-B3), (A3-B6), (A6-B3), (A7-B7), (A7-B8), (A8-B7), (A1-B9), (A9-B1), (A3-B9), (A6-B9), (A7-B9), (A9-B3), (A9-B6), (A9-B7), (A9-B8), (A9-B9). (A8-B9),
39+6 (45)	8	8	8+11 (19)

2.3 Conclusions

After making these RCCS changes, shoot-through events got reduced to 17 faulty states (highlighted in red) from 42. Shoot-through events are inevitable in these 17 faulty states as they represent the full-bridge faults where either one of the half-bridges is short-circuited. In summary, PEBB enters blocking state for 45 faulty states, positive inserted state for 8 faulty states, negative inserted state for 8 faulty states and bypassed mode in the remaining 19 faulty states.

PEBB in blocking state or bypassed state is suitable for bypass operation. The PEBB in positive insertion or negative insertion states should not be bypassed as it results in shoot-through events. The shoot-through paths for capacitor inserted states with external bypassing are shown in **Figure 2 - 8**.

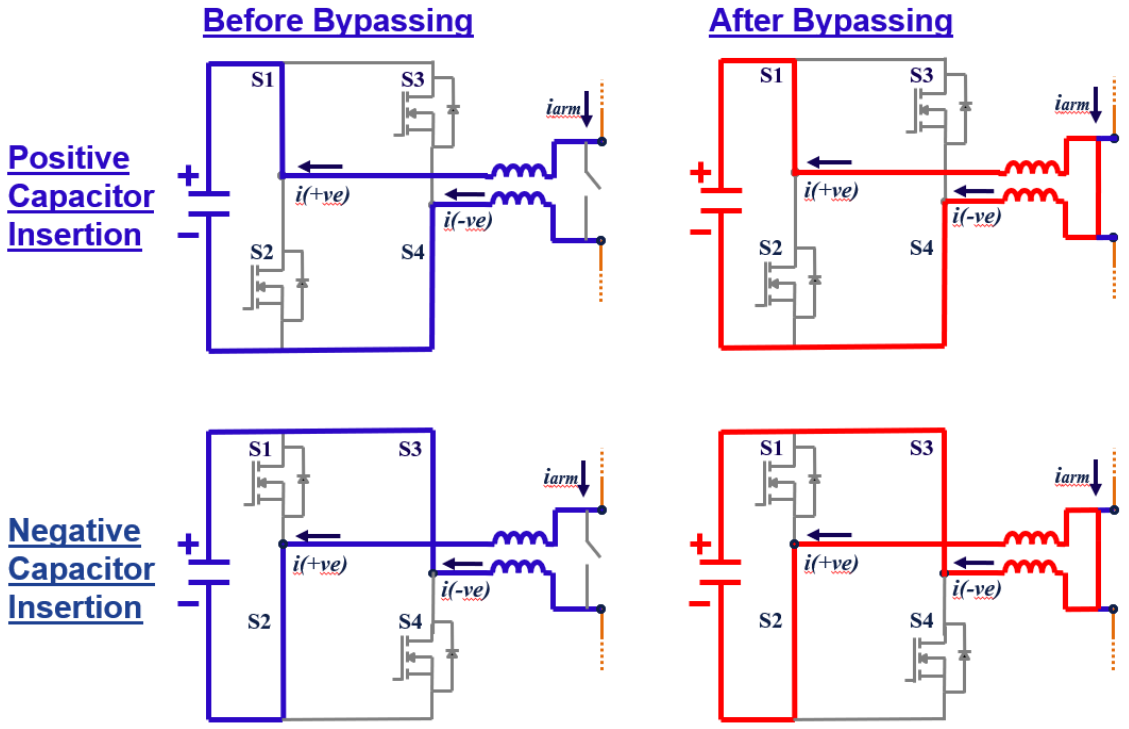

Figure 2 - 8. Shoot-Thorugh paths provided by bypass switch in PEBB capacitor inserted states.

Therefore 16 faulty states (positive insertion and negative insertion) in **Table 2 - 7** are not feasible for a bypass operation if the gate driver continues normal modulation. Upon considering gate driver shutdown of MOSFETs after a fault detection, eight faulty states (A6-B7, A6-B8, A3-B7, A3-B8, A7-B3, A7-B6, A8-B3, A8-B6) still lead to the shoot-through event when bypassed. In summary, 72 (90%) out of 80 faulty states, PEBB can be bypassed to continue the MMC operation.

Chapter 3 Design Requirements

3.1 Introduction

As discussed in Chapter 1, switching cycle control adds advantages to MMC, such as reduced size and cost of the PEBBs. However, this control requires high switching frequency and high *di/dt* current conduction capabilities. Therefore, this chapter focuses on extracting the detailed bypass switch requirements of PEBB1000 through SCC-based MMC simulations.

Figure 3 - 1 shows the full-bridge structure of PEBB1000 along with the additional switches. The switches highlighted in blue are electro-mechanical (EM) relays used for reconfiguration and interconnection with neighboring PEBBs. Moreover, the switch highlighted in green is the solid-state switch for bypassing the PEBB.

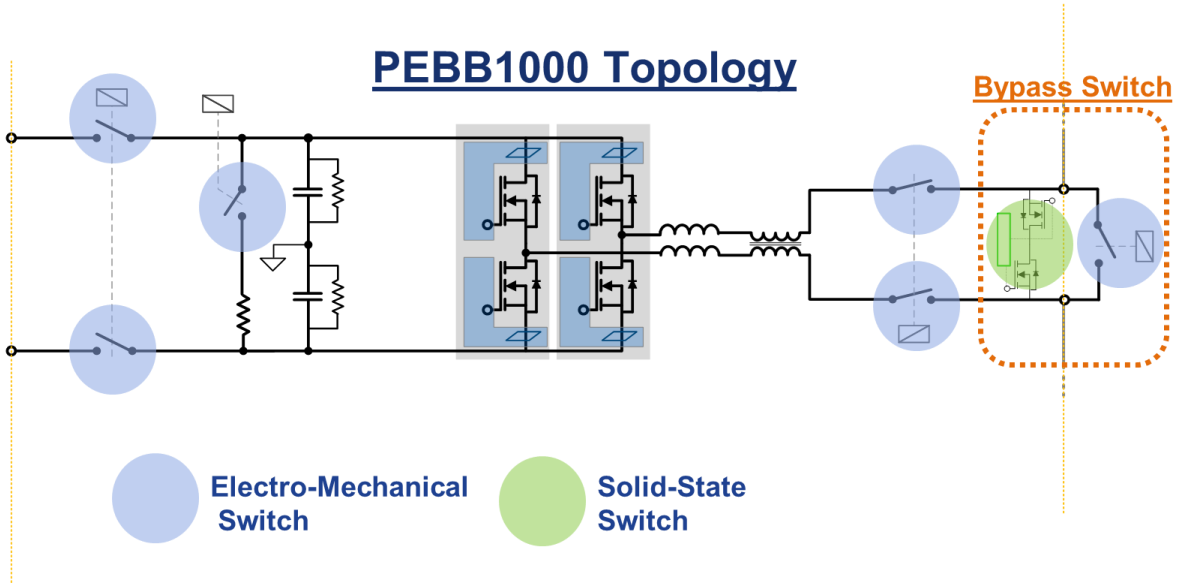

Figure 3 - 1. Circuit topology of PEBB1000.

Even though solid-state switches have operation times less than 500 nanoseconds, they incur high power losses around 200-300 W for continuous conduction of 100 amperes. On the

other hand, EM relays have slower operation times between 10 - 70 milliseconds but provide low power losses (less than 10 W). Therefore, a parallel combination of an EM relay and a solid-state switch is chosen as the external bypass switch to achieve both fast operation and low losses. When EM relay and solid-state switch are in ON state, the arm current majorly flows through the EM relay due to smaller ON resistance. Therefore, the solid-state switch design can be limited to 100 A conduction capability for the operating time of EM relays.

3.2 Electro-Mechanical Relays

The total conduction time of the solid-state bypass switch is dependent on the Electro-Mechanical relays. Also, practical verification of the solid-state bypass switch requires an EM relay connected in parallel for accurate assessment. Therefore, commercially available EM relays are surveyed to finalize the best fit. Accordingly, a compact relay actuator has been designed for control purposes.

3.2.1 Relay Selection

EM relays have an input coil to control the make or break of the switch. When 24 V is applied to the input coil of a normally closed relay, the coil draws current to break the switch and vice-versa. The input coil draws high inrush currents initially in the range of 1.5 amperes level and settles back to holing currents at 100 milliamperes level. According to PEBB1000 specifications of 1000 V, 100 A, and 24 V low-voltage power supply, commercially available EM relays are shortlisted, as shown in **Table 3 - 1.** IHVA200-H3D24V-BF relay is not selected due to longer operating times. DCNEVT350-CA has similar features to HXNC241, like operating times and coil currents, but is expensive due to the higher current rating. Therefore, the HXNC241 normally-connected contactor is finalized as PEBB1000 EM-relay. For solid-state switch requirements, 20

milliseconds of conduction time is sufficient for the HXNC241CAB relay to turn-on. For better compatibility with most of the existing EM relays, 80 milliseconds of conduction time is chosen as a design specification for a solid-state bypass switch.

Table 3 - 1. Shortlisted Electro-Mechanical Relays for PEBB1000

Device	**Max Voltage**	**Rated Current**	**Turn-on Time**	**Turn-off Time**	**Coil Current**	**Auxiliary Contacts**
IHVA200-H3D24V-BF	1500 V	200 A	65 ms	20 ms	Not Available	Yes
HXNC241CAB	1500 V	200 A	20 ms	13 ms	1.6 A (Inrush) 97 mA (Holding)	Yes
DCNEVT350-CA	1800 V	350 A	18 ms	15 ms	1.8 A (Inrush) 110 mA (Holding)	Yes

3.2.2 Relay Actuator Design

As explained before, EM relay turn-on and turn-off are controlled by the voltage across the input coil. For HXNC241, the relay stays ON when no voltage is applied to the coil and stays OFF when 24 V is applied. For facilitating control, an optocoupler switch is connected in series with the relay input coil, as shown in **Figure 3 - 2(a).** The coil's positive terminal is connected to 24 V**,** and coil current flows only when the optocoupler is turned-on. A low voltage 3.3 V digital signal can be used as the control signal for the optocoupler. A D-latch is added between the controller and optocoupler to safeguard the relay against noise perturbations.

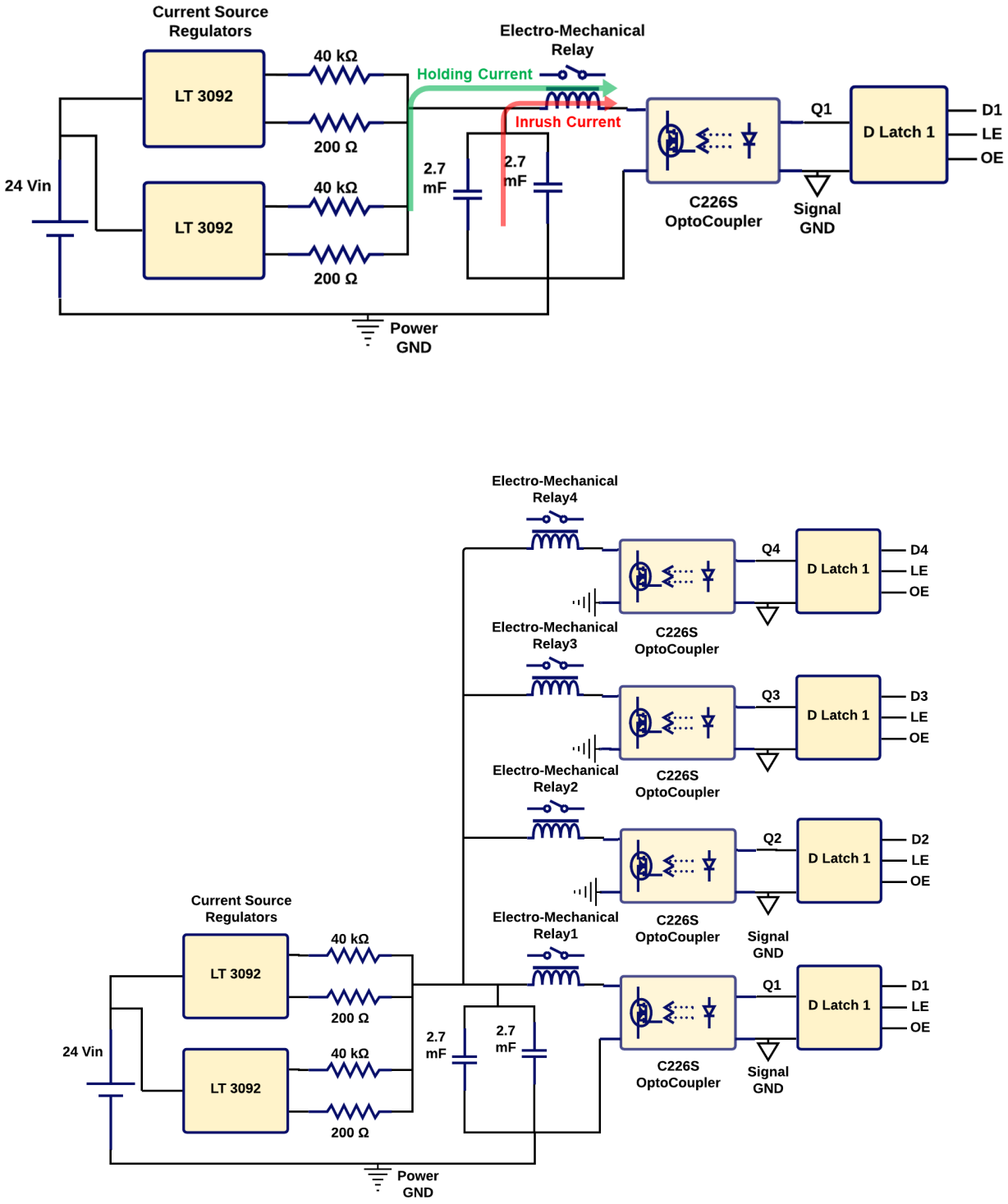

Figure 3 - 2. Relay Actuator Schematic for a) single EM relay, b) four relays.

Since the coil inrush current is significantly high compared to its holding current, 38.4 W instantaneous power is required during the inrush period. The PEBB1000 uses a standard 24 V power supply to power all the control and sensor circuitry. The power fluctuations of EM relays can cause an imbalance in the power supply. Therefore, current source limiters are employed between the 24 V power supply and the relay coil to avoid imbalance. Two current source regulators of 200 mA are selected to limit the maximum input current to 400 mA (> holding current of the EM relays). Electrolytic capacitors are connected after current source blocks to supply the inrush energy required. For achieving high power density, four relays are controlled from a single board by optimizing current source regulators and electrolytic capacitor values.

3.2.3 Relay Actuator Validation

The relay actuator Printed Circuit Board (PCB) shown in **Figure 3 - 3** is developed according to the schematic for design validation. The dimensions of the PCB are finalized at 4 cm by 5 cm after compact placement of components.

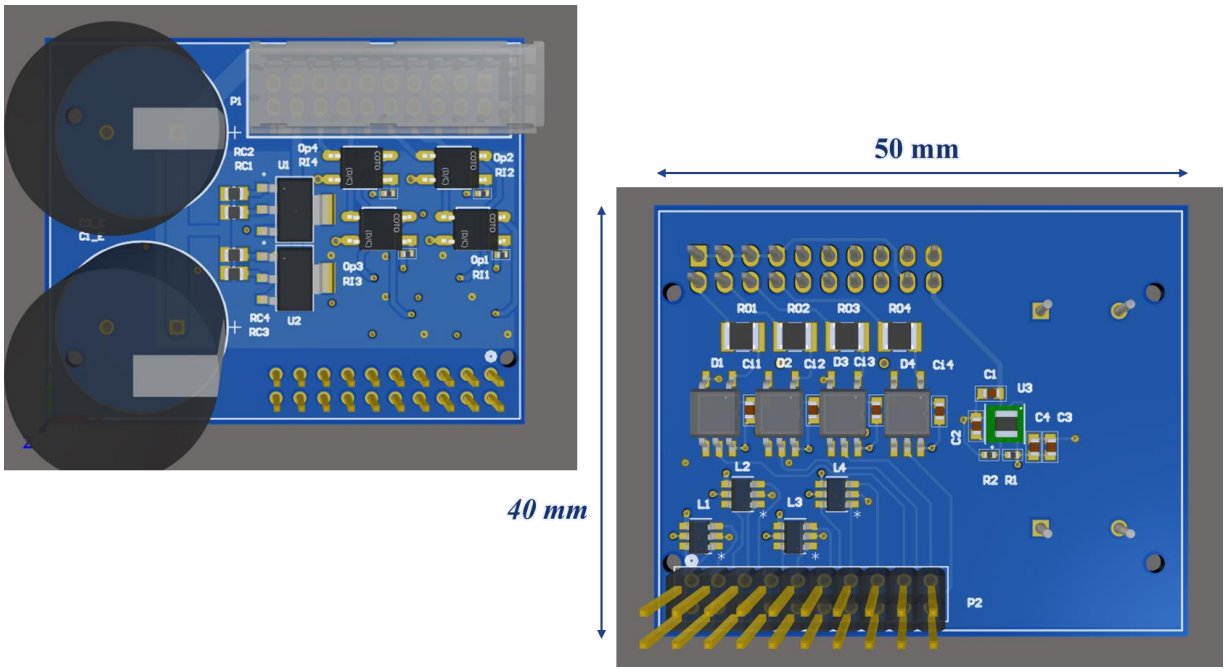

Figure 3 - 3. PCB design of the relay actuator.

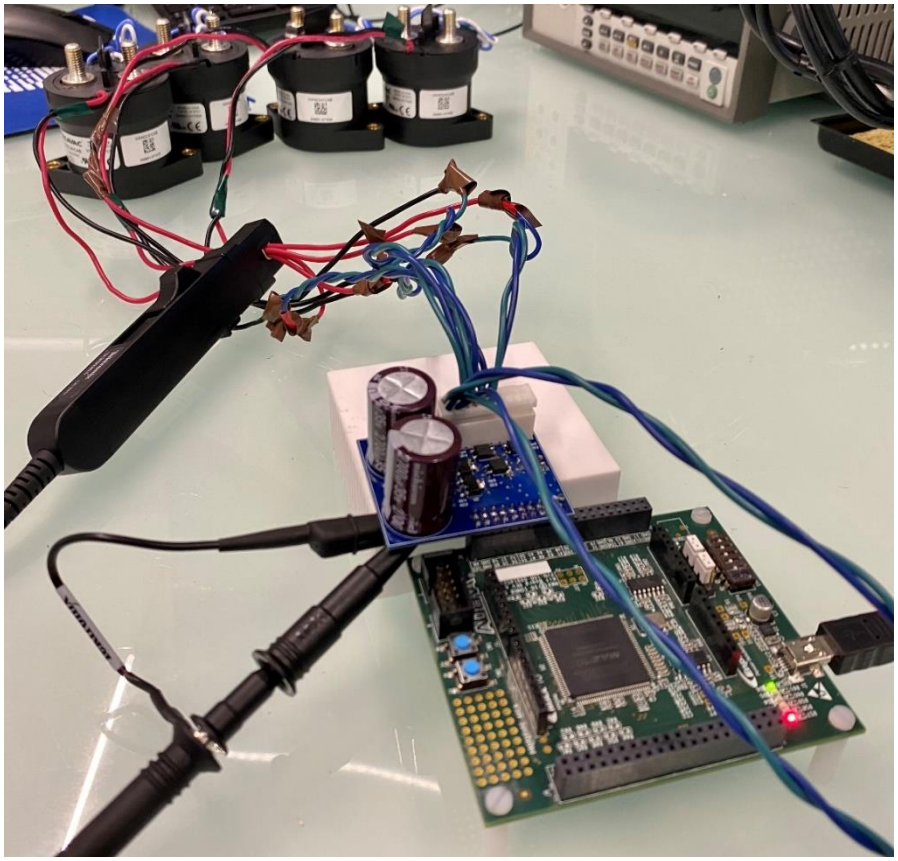

Figure 3 - 4. Test Validation of Relay Actuator Board

Figure 3 - 4 shows the test setup to validate the operation of the relay actuator. A Max10 FPGA board has been utilized to provide digital control signals. All four relays are turned-on and OFF simultaneously by synchronizing control signals. Input supply current and collective coil currents are observed to verify the effectiveness of current source regulators. Input voltage and capacitor voltage are also measured to estimate the power consumption of relays. The observed test waveforms are shown in **Figure 3 - 5.**

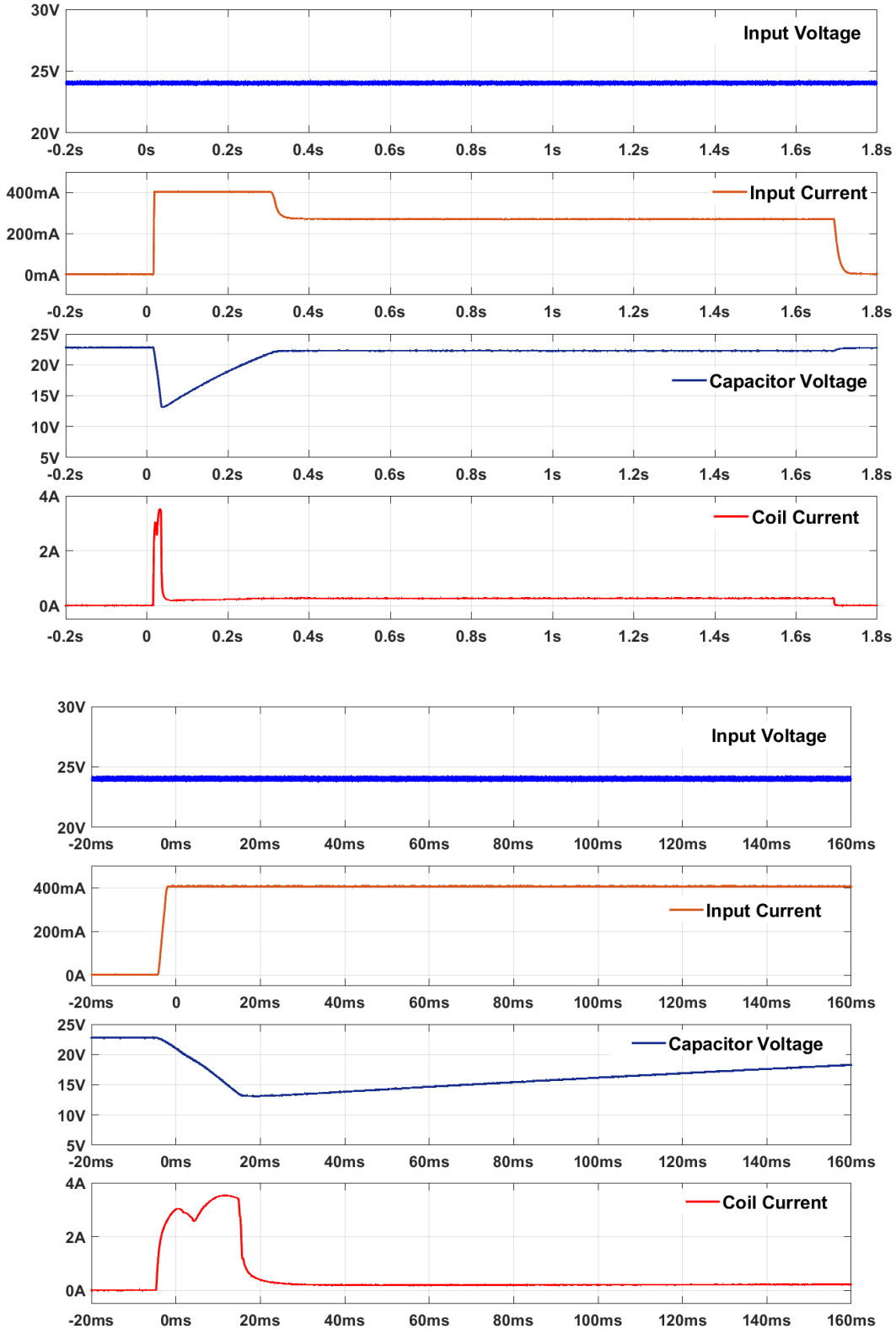

Figure 3 - 5. Test results of the relay actuator PCB a) one switch cycle b) Turn-off

From the test results, it can be observed that inrush current is mainly supplied from electrolytic capacitor's stored energy. **Figure 3 - 5 (b)** clearly shows the capacitor voltage drop until coil current settles back from inrush current to holding current. The input supply current is limited to 400 milliamperes, according to the design. The maximum instantaneous coil power required to drive four relays is 57 watts at the inrush current period. Due to the effectiveness of current source regulators, the maximum input power is limited to 9.6 watts. This relay actuator board is used to control bypass EM relay for overall validation of external bypass switch design.

3.3 MMC Modeling with Switching Cycle Control

A four PEBBs/arm MMC model has been developed in PLECS software, using switching cycle control. The critical parameters of the modeled MMC are presented in **Table 3 - 2,** complying with PEBB1000 specifications.

Table 3 - 2. MMC PLECS model parameters.

Parameters	**MMC PLECS MODEL (Switching Cycle control)**
PEBB Capacitance	60 μF
PEBB Capacitor Voltage	1000 V
Submodule Inductance	3 μH
Switching Frequency	20 kHz
DC-Link Voltage	4000 V
Load Inductance	10 mH
Load Current	83 A DC
Load Resistance	10 Ohms

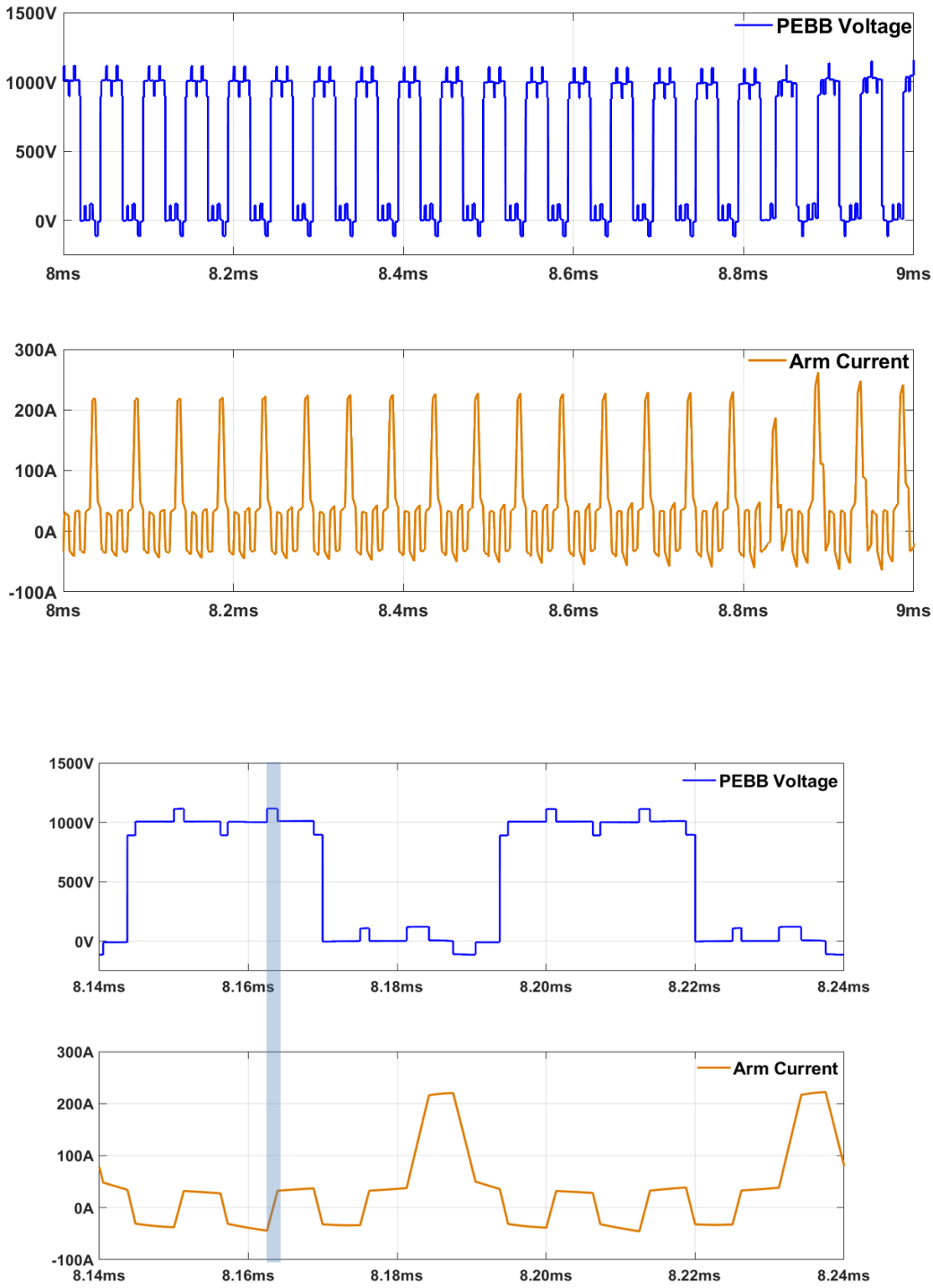

Figure 3 - 6. PEBB terminal voltage and arm currents.

As the bypass switch has to be connected across the AC terminals of the PEBB, the PEBB terminal voltage and arm current waveforms are monitored, as shown in **Figure 3 - 6**. The arm current polarity shifts due to switching cycle control can be noticed in every switching period. Also, the arm current's high *di/dt*-current rate resulted in an additional +/- 100-200 V drop across the PEBB inductance during these polarity shift events. As a result, the terminal voltage consists of additional voltage variations apart from 1000 V switching pulses. Therefore, the breakdown voltage of the external bypass switch should be higher than 1200 V. The breakdown voltage requirement of the bypass switch is finalized to be 1500 V (1200 V+300 V) to provide a safety margin of 25%.

In case of bypass switch current requirements, the arm current flows through the bypass switch after turn-on. For an 83 A RMS arm current, repetitive peak values up to 250 A are observed in each switching period. After considering safety margins, the solid-state switch should be designed for 100 A mean current and 300 A repetitive pulse current capability.

3.4 Arm Current Transients for PEBB Faulty Conditions

According to the fault case study discussed in Chapter-2, a full-bridge PEBB can have four faulty modes: positive insertion, negative insertion, bypassing, and blocking modes. In regular operation, only positive insertion and bypassing modes are utilized according to the modulation scheme.

As the external bypass switch is operated after the fault occurrence, it is essential to assess variations in PEBB1000 parameters after fault occurrence. It is complicated to analyze exact variations in arm current and PEBB terminal voltage for all 80 unique faults. Therefore, a simple

analysis has been conducted considering four worst-case faults, where PEBB stays in one of the four-fault modes continuously unresponsive to gate-driver modulation. The transients observed in each faulty mode are presented below.

1. PEBB bypassing mode.

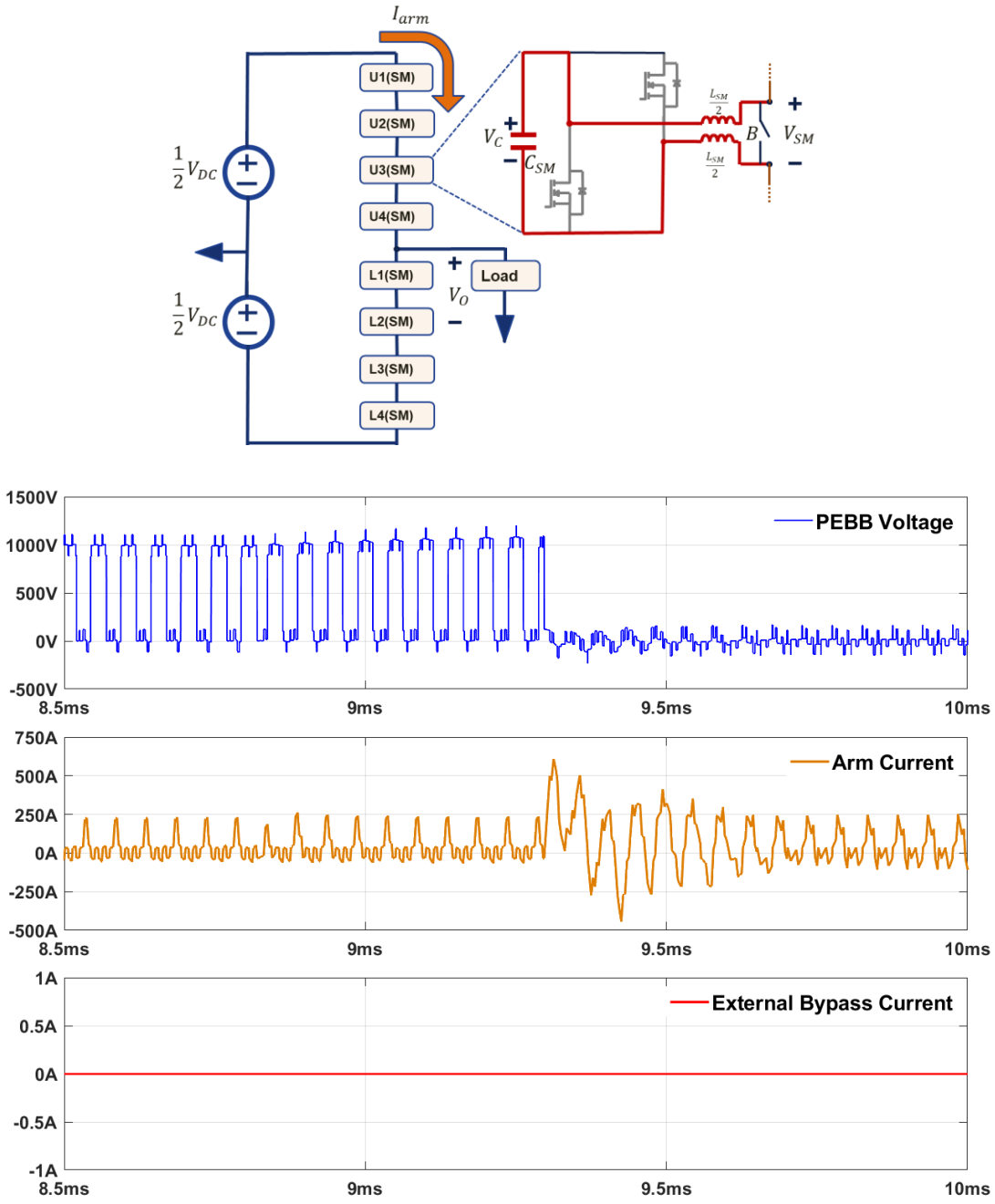

Figure 3 - 7. Fault transients for PEBB bypassing a) Circuit topology b) Faulty PEBB waveforms

2. PEBB Positive Insertion mode.

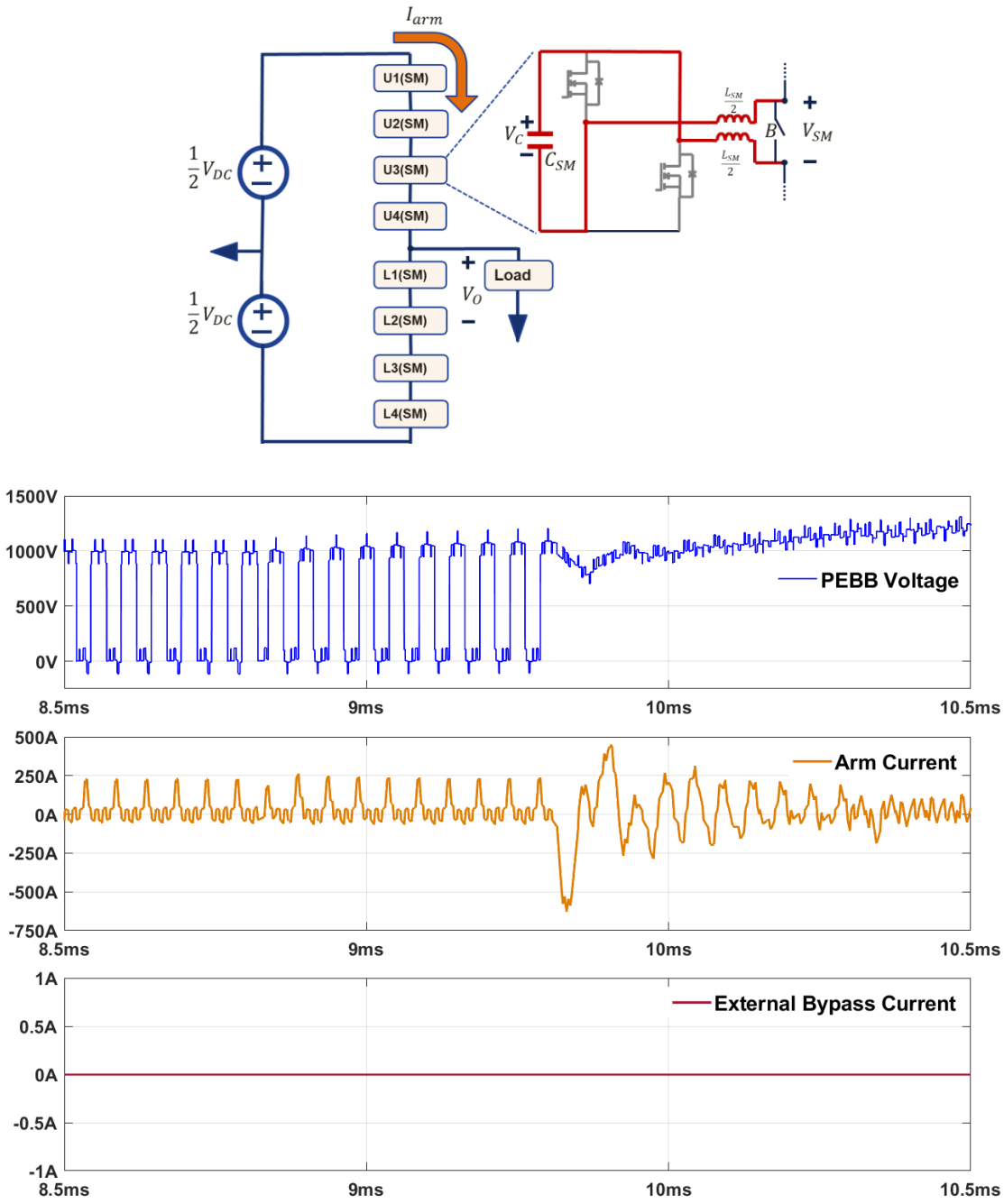

Figure 3 - 8. Fault transients for PEBB positive insertion a) Circuit topology b) Faulty PEBB waveforms

3. PEBB Negative Insertion mode.

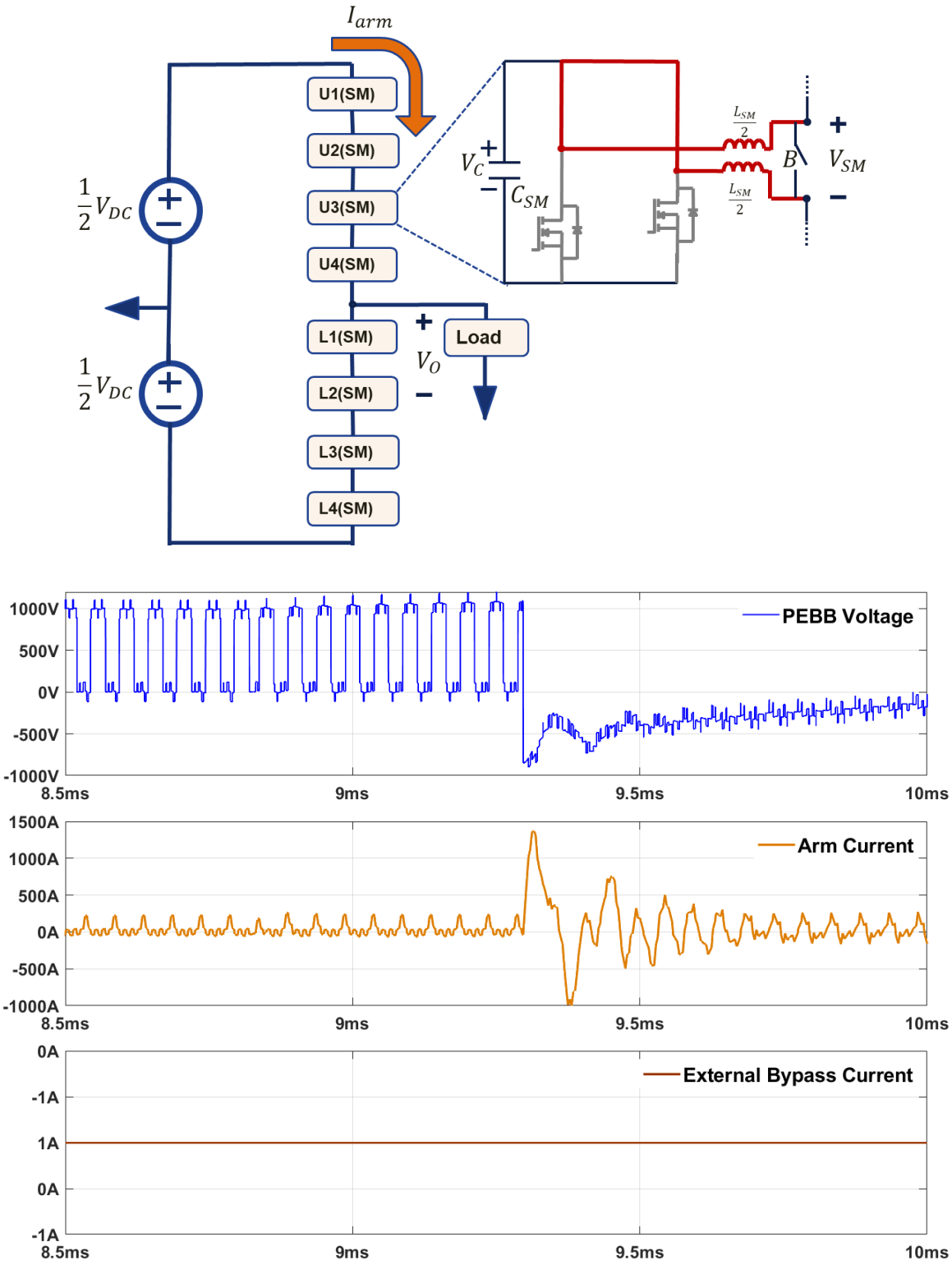

Figure 3 - 9. Fault transients for PEBB negative insertion a) Circuit topology b) Faulty PEBB waveforms

4. PEBB Blocking mode.

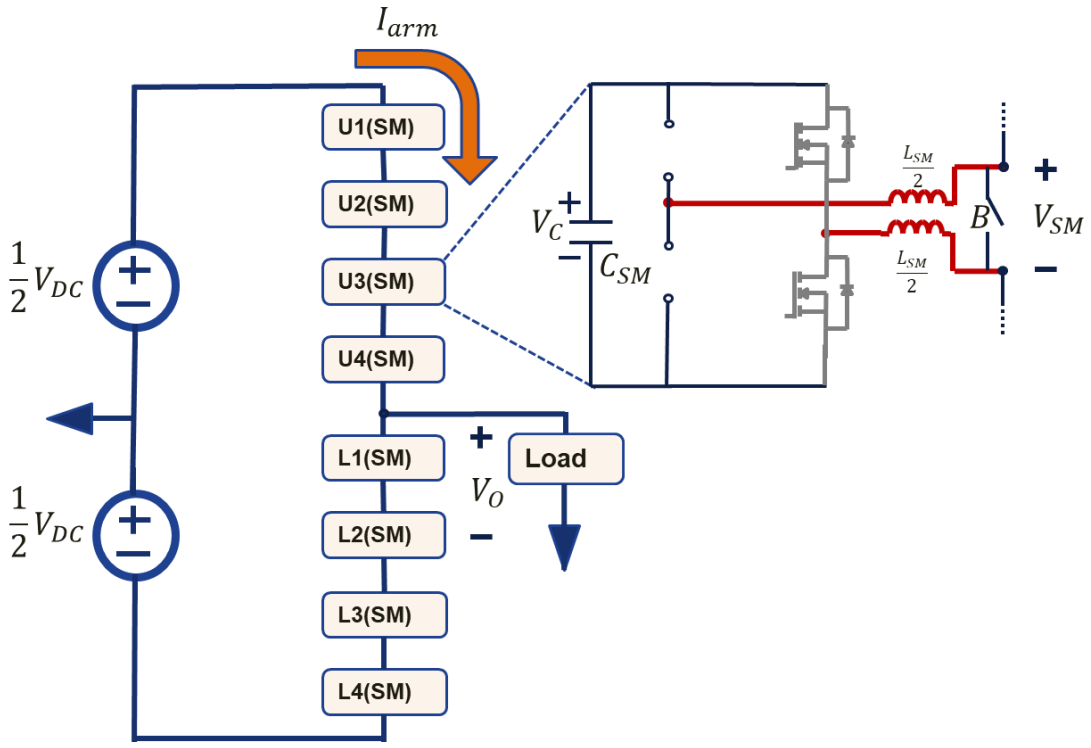

Figure 3 - 10. MMC topology for PEBB blocking mode.

Table 3 - 3. The additional voltage drop across total arm inductance due to faulty PEBB modes.

			Working state	
			Insertion (+1 kV)	Bypassing (0 V)
Faulty State	Bypassing Mode	0 V	Voltage Drop = +1 kV	Voltage Drop = 0 V
	Positive Insertion Mode	+1 kV	Voltage Drop = 0 V	Voltage Drop = -1 kV
	Negative Insertion Mode	-1 kV	Voltage Drop = +2 kV	Voltage Drop = +1 kV

MMC simulations have been performed with a faulty PEBB (U3, upper arm 3rd PEBB) according to topologies shown in **Figure 3 - 7(a), Figure 3 - 8(a), Figure 3 - 9(a),** and **Figure 3 - 10** respectively. The PEBB faulty modes creates a voltage mismatch between DC-link voltage and total inserted SM capacitors voltages. This mismatch voltage appears across the total arm inductance leading to different transients. **Table 3 - 3** shows the voltage drops across total arm inductance for different faulty PEBB modes.

Figure 3 - 7(b) shows the arm current and PEBB (U3) terminal voltage variation when the topology shifts from normal operation to continuous bypassing mode. This led to a voltage mismatch of 1000 V and caused current transients to charge the remaining PEBB capacitors to a higher voltage. The duration of current transients is noticed to be around 200 µs with peak currents up to 610 A.

Figure 3 - 8(b) shows the arm current and PEBB (U3) terminal voltage variation when the topology shifts from normal operation to continuous positive capacitor insertion mode. This led to a voltage mismatch of -1000 V and caused negative current transients initially. The duration of current transients is observed to be around 200 µs with peak currents up to -580 A. Due to positive load current and high DC link voltage, currents returned to normal values from transients. However, this is an unstable MMC operation as the faulty PEBB capacitor is continuously charged, increasing its voltage.

Figure 3 - 9(b) shows the arm current and PEBB (U3) terminal voltage variation when the topology shifts from normal operation to continuous negative capacitor insertion mode. This led to a voltage mismatch of +2000 V and caused current transients twice to that of bypassing mode. The duration of current transients is noticed to be around 200 µs with peak currents up to 1400 A. Due to positive load current and high DC link voltage, currents returned to normal values from the

transients. The negatively inserted capacitor is charged by arm current until its negative charge is nullified. This provides a possibility for achieving stable operation.

MMC Simulations could not be conducted after PEBB blocking mode, as in **Figure 3 - 10**, because of sudden disruption of arm current path. It could be understood from the basic inductor equations that high voltage will appear across the faulty PEBB terminals. The stored energy in all PEBB inductances in the arm will induce a high voltage across the open terminals. As the voltage reaches the breakdown voltage of MOSFETs in the faulty PEBB, avalanche breakdown will take place, causing permanent damage to all PEBB MOSFETs. This damage should be prevented by effective design of bypass switch providing an additional current path as the fault occurs.

Adding a Metal Oxide Varistor (MOV) parallel with an external bypass switch can limit the maximum voltage. An appropriate selection of MOV with clamping voltage between 1200 V and 1700 V is required for protection against PEBB blocking mode. Since MOVs cannot continuously conduct current, a fast external bypass switch operation within 2 μs is required.

3.5 Proposed Turn-on Sequence

After the detailed understanding of the PEBB1000 and the gate driver's internal communication interface, the following turn-on sequence presented in **Figure 3 - 11** is proposed. This turn-on sequence can achieve synchronous operation of the bypass switch and PEBB MOSFETs to achieve the lowest arm current deviations.

Most faults, such as over-voltage and over-current, can be directly monitored by the PEBB1000 gate driver through voltage, current, and temperature sensors. If a fault is observed, the gate driver reports back to the PEBB controller in 180 nanoseconds. Then within 120 ns, the PEBB main controller decides whether to shut down the faulty PEBB or not. A termination signal

is sent to the gate drivers and fault-protection devices if the decision is to shut down. The PEBB MOSFETs must be turned-off before turning-on the bypass switch to avoid the shoot-through events explained in chapter-2. Therefore, a wait time of 250-350 nanoseconds should be added to delay the bypass turn-on. This value is deduced by comparing driver IC delays, as well as MOSFET turn-on and turn-off times. The wait time can be better assessed from experiments.

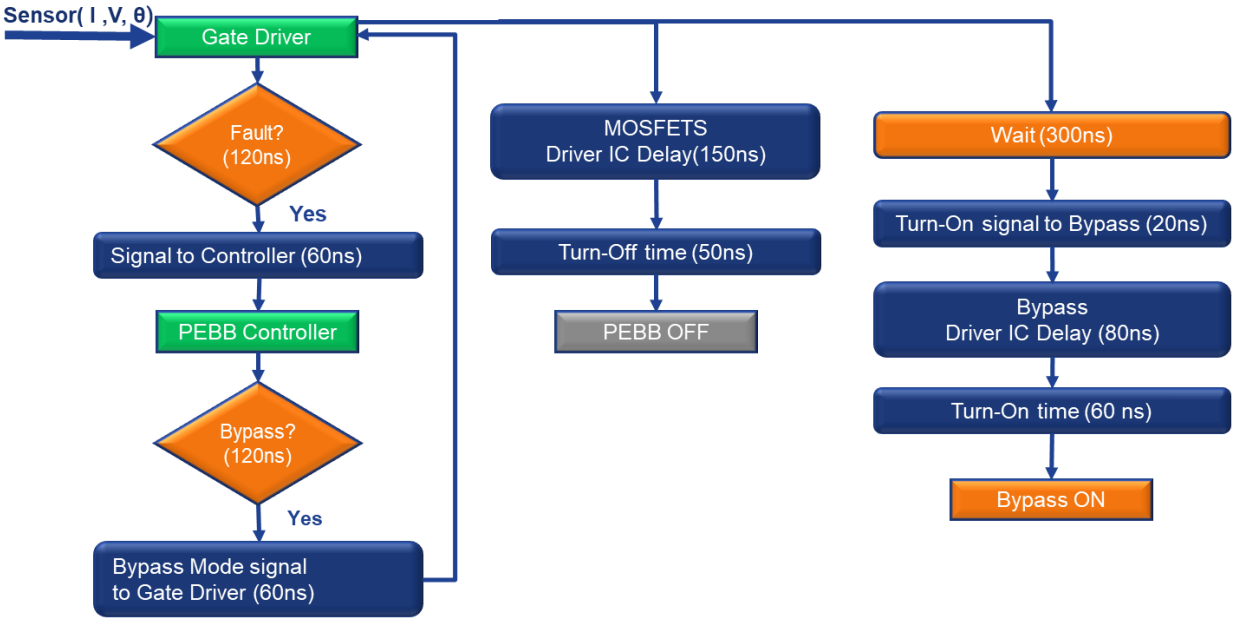

Figure 3 - 11. Fault response state machine for PEBB1000.

3.6 Arm Current Transients for External Bypass operation.

According to the proposed turn-on sequence, the bypass operation has been simulated. **Figure 3 - 12** shows the transition of arm current from PEBB to bypass switch. After the bypass switch takes over the arm current, transient currents arise due to the voltage mismatch of 1000 V between the arm voltage and the DC-link voltage. According to the hot storage strategy, all the working PEBB capacitor voltages are increased due to the transients. For the selected PEBB capacitances and inductances, these transients have peak currents of up to 800 amperes but a fast-settling time of 200 microseconds. These peak values of transient currents in SCC are 2-4 times

higher than peak currents observed in phase-shifted carrier wave modulation (PS-CWM). This variation is due to the low PEBB inductance of two microhenries.

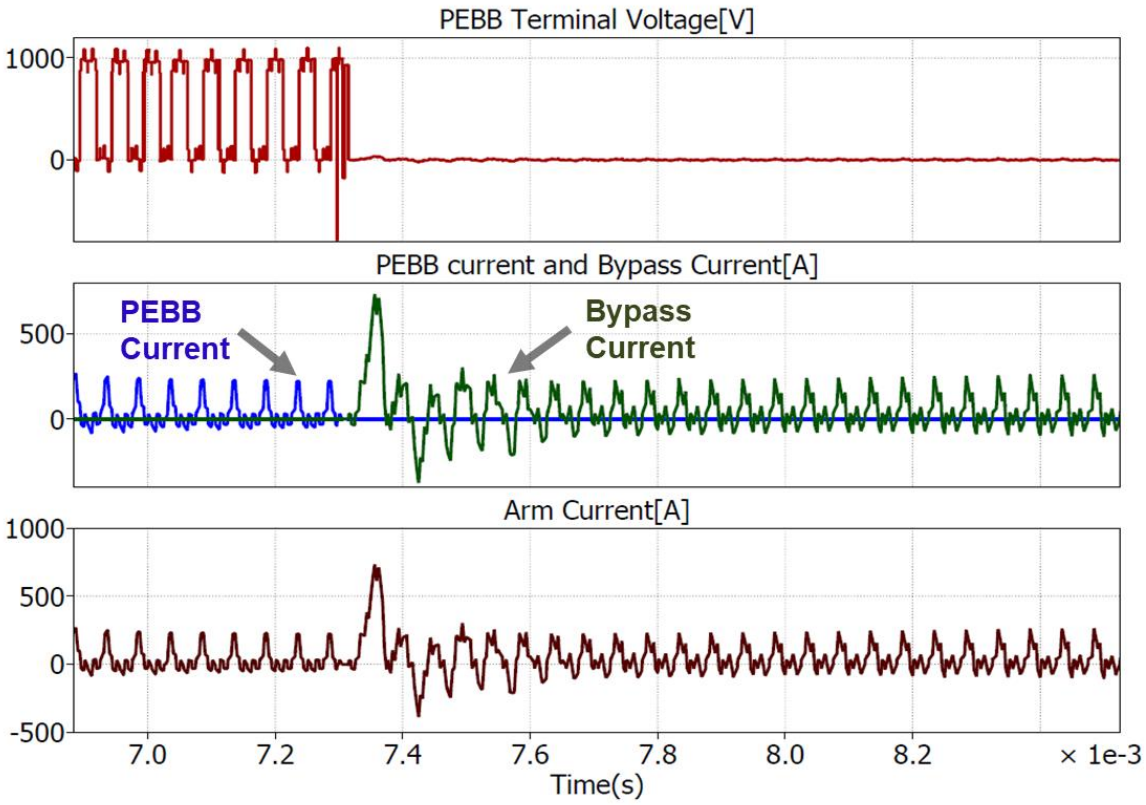

Figure 3 - 12. Commutation between PEBB and Bypass switch according to proposed turn-on sequence.

3.6 Bypass Design Requirements

From the observed waveforms and transients, extracted bypass switch design targets are presented in **Table 3 - 3.** Due to extra voltage fluctuations caused by the PEBB inductor, it would no longer be safe to use 1200 V devices. Therefore, the bypass switch must have a minimum of 1500 V OFF-state voltage blocking. Also, Metal Oxide Varistor (MOV) with clamping voltage between 1300-1700 volts should be connected in parallel to the bypass switch. The MOV can protect PEBB devices against over-voltage when the PEBB enters the blocking mode. Also, the

switch should be able to conduct transient currents with 260 A RMS current for 200 microseconds. As a critical design specification, the overall operation time of the switch must be achieved below 300 nanoseconds.

Table 3 - 4. Bypass switch design challenges for the PEBB1000-based SCC-MMC.

Parameter	Design Target
Blocking Voltage	1500 V
Continuous Current	300 A Peak 100 A RMS @ 80 Milliseconds
Transient Current	800 A Peak 260 A RMS @ 200 Microseconds
Operation Time	< 300 Nanoseconds
VGS @ 50 V/ns	VEE +/- 2 V
Maximum Clamping Voltage	1300 -1700 V

Chapter 4 Bypass Switch Design

4.1 Device Selection

According to the design challenges presented in Chapter 3, a survey has been conducted of commercially available solid-state switches with a minimum breakdown voltage of 1500 V. Si IGBT and SiC MOSFET discrete devices with 1700 volts breakdown voltage are shortlisted to provide the necessary terminal voltage. **Table 4 - 1** shows the shortlisted device parameters influencing false triggering, power loss, and turn-on time.

Table 4 - 1. Shortlist of IGBTs and MOSFETS for the bypass switch.

MOSFETS	**Vds (Br)**	**Cgs Cge**	**Rg(int)**	**ΔVgs @ 50v/ns**	**I_DS**	**R_DS ON**	**T_ON**	**T_OFF**
C2M0045170P	1700 V	6.7 pF, 3.66 nF	1.3 Ω	+/- 0.8V	48A @100°C	40 mΩ	48 ns	56 ns
G3R45MT17K	1700 V	15.3 pF, 3.18 nF	1.3 Ω	+/- 1.5V	34 A @100°C	50 mΩ	76 ns	58 ns
IGBT	**Vce**	**Cge Cgc**	**Rg(int)**	**ΔVgs @ 50v/ns**	**I_C**	**VCE ON**	**T_ON**	**T_OFF**
IXYH30N170C	1700 V	55 pF, 3.1 nF	2.8 Ω	+/- 4 V	30 A @110°C	5.2 V @40 A	52 ns	238 ns
IXGH24N170-ND	1700 V	40 pF, 3.5 nF	2.7 Ω	+/- 3.5 V	32 A @90°C	3.6 V @40 A	83 ns	520 ns

Where VDS(Br) – Drain-to-Source Breakdown Voltage

Cgs – Gate-to-Source Capacitance

Cgd – Gate-to-Drain Capacitance

Rg(Int) – Internal Gate Resistance

ΔVgs – Gate-to-Source Voltage Ripple

RDS(ON) – ON-state Drain-to-Source Resistance

TON, TOFF – Turn-on, Turn-off time

Vce_Br – Collector-to-Emitter Breakdown Voltage

Cge – Gate-to-Emitter Capacitance

Cgc – Gate-to-Collector Capacitance

ΔVge – Gate-to-Emitter Voltage Ripple

VCE_ON – ON-State Collector-to-Emitter Voltage Drop

False-triggering [21] or false turn-on of the devices happens when the Miller current flows through the gate resistance, causing a voltage drop that makes the gate-source voltage higher than the device threshold value. The Miller current is generated due to the high *dv/dt*-voltage rate across the device through parasitic capacitance Cgd or Cgc, as shown in **Figure 4 - 1**. Using a Miller clamp and negative gate voltage, this effect can be mitigated to an extent. Assuming the application of the Miller clamp, ΔVgs is estimated according to the equation in **Figure 4 - 1** for the shortlisted devices. SiC MOSFETs show lower voltage ripple for Miller currents due to a low value of Cgd.

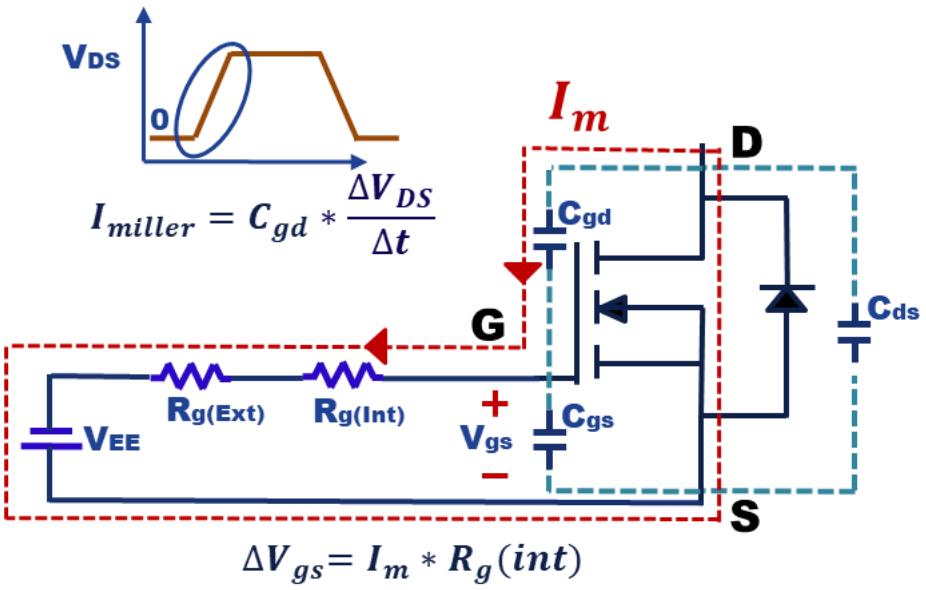

Figure 4 - 1. Miller current due to drain-source *dv/dt*-voltage rate.

Also, conduction losses of IGBTs are twice that of MOSFETs. Since the bypass switch stays in parallel to the PEBB, the ON-state voltage drop of the bypass switch should be in close range to that of the PEBB MOSFETs to have a better current sharing. Turn-on times are similar for all devices (around 50-80 nanoseconds, including delays).

Giving priority to *dv/dt*-voltage rate endurance and the ON-state voltage drop, SiC MOSFETs are preferred over IGBTs. Amongst the MOSFETs, the C2M0045170P Cree MOSFET offers superior performance in all aspects presented, with 52 ns turn-on time, 160 A pulsed current capability, and a lower voltage drop of 1.6 volts across the device for 40 amperes continuous current. Therefore, the C2M0045170P has been selected as the base device for the bypass switch topology. Since 1.7 kV devices can only continuously conduct up to 40 amperes, devices should be paralleled to meet the 100 amperes design requirement.

4.2 Topology Selection

A bypass switch is primarily a bidirectional switch capable of conducting in both directions in the ON state and capable of blocking voltage in both directions in the OFF state. A TRIAC switch is a bidirectional switch by itself with required blocking and conduction features. However, the SiC MOSFET has bidirectional conduction but not bidirectional blocking features. The anti-parallel body diode starts conducting for negative voltage across the device. For the required bidirectional voltage blocking, a diode bridge or anti-series topologies shown in **Figure 4 - 2** can be used.

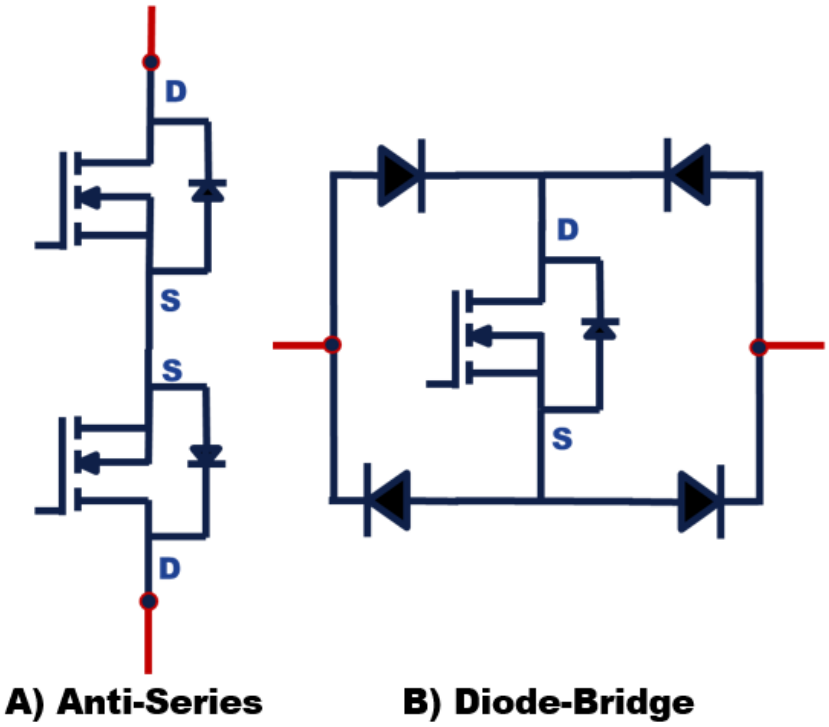

Figure 4 - 2. Bidirectional switch topologies using MOSFETs.

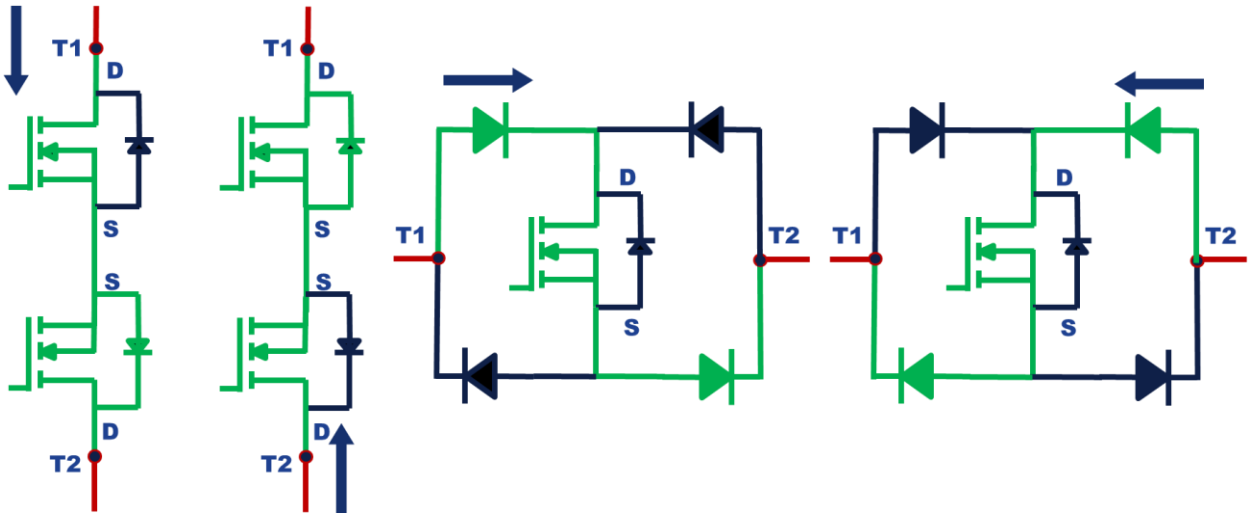

Figure 4 - 3. Bidirectional conduction paths for diode-bridge and anti-series topologies.

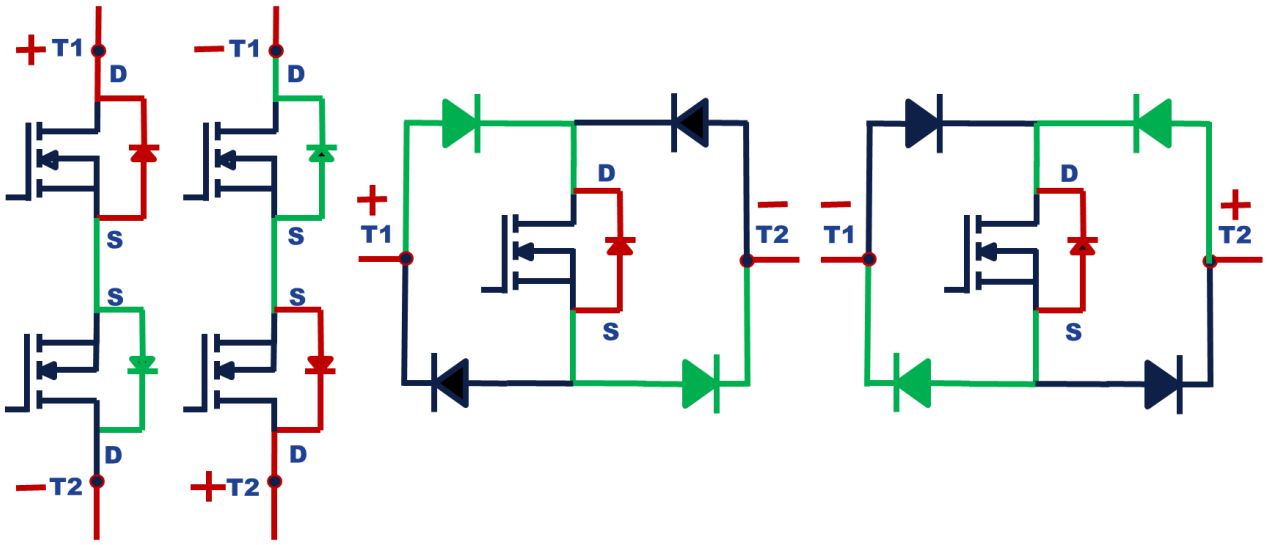

Figure 4 - 4. Bidirectional voltage-blocking paths for diode-bridge and anti-series topologies.

Current conduction paths in both directions for the two topologies, highlighted in green, are illustrated in **Figure 4 - 3**. Also, voltage-blocking paths in both directions for the two topologies, highlighted in red, are shown in **Figure 4 - 4.**

These topologies cannot support 100 A conduction because of the 40 A current limitation of Cree MOSFETs. So, the three devices should be parallel to achieve the design requirements of 100 A (3*33.34 A) and 300 A pulsed current (3*160=480 A), specifically, to meet the transient currents of up to 800 amperes. **Figure 4 - 5** shows the modified anti-series topology with three devices in parallel to meet the design requirements.

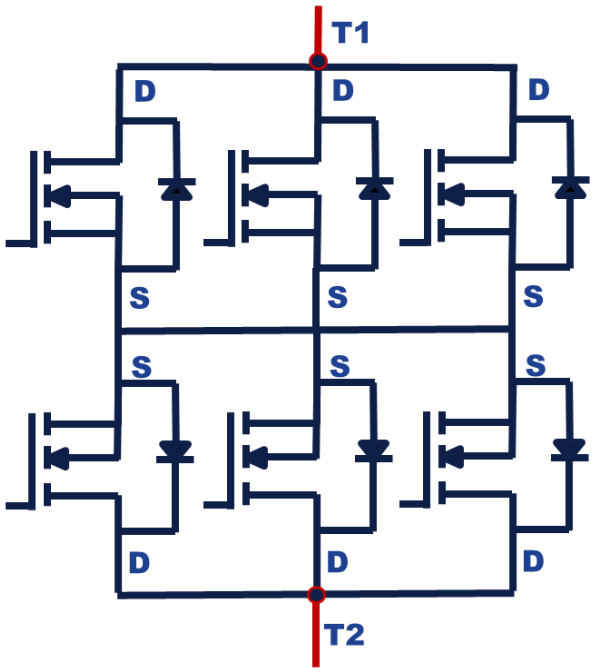

Figure 4 - 5. Modified anti-series topology with parallel MOSFETs.

For a diode-bridge topology, the diode VS-90EPS16L-M3 (Vishay semiconductor) is selected based on available diodes with 100 amperes forward current rating and 1600 volts reverse

blocking voltage. **Figure 4 - 6** shows the applicable diode-bridge topology after modification to meet the design requirements.

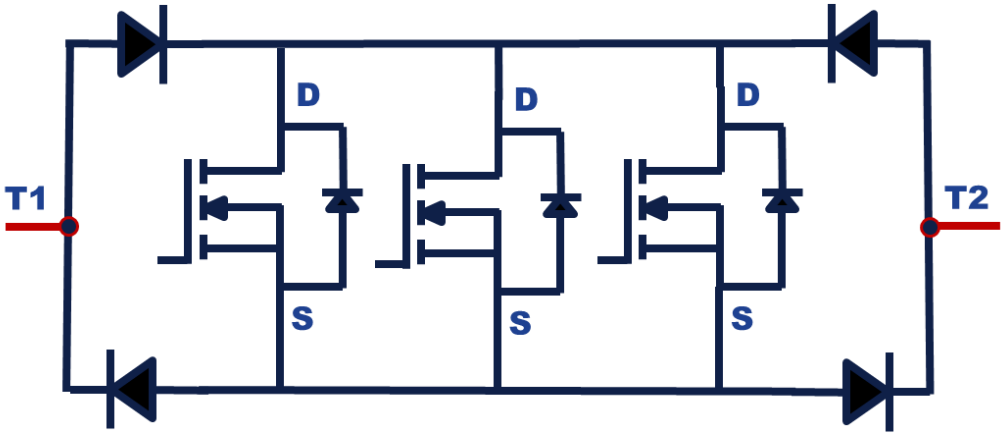

Figure 4 - 6. Modified diode-bridge topology with parallel MOSFETs.

Table 4 - 2. Comparison of parameters between diode-bridge topology and anti-series topology.

	Diode-Bridge Topology	**Anti-Series Topology**
Device Count:	7	6
Voltage Drop(@100A):	4.3 V	3V
Total Losses:	430 W	300 W
Switching Devices:	3	6
Voltage Stress (MOSFETs):	1000 V	1000 V

Table 4 - 2 compares the key differences between the bypass switch topologies in terms of performance. The diode-bridge topology cannot provide high power density because of its higher device count and power losses. However, this topology has the advantage of fewer switching devices, which reduces switching losses compared to the anti-series topology. As the bypass switch requires only one turn-on event when a fault occurs, switching losses are considered a lower

priority than power density. Therefore, the anti-series topology is selected over the diode-bridge topology for the bypass switch to achieve high power density and low power loss.

4.3 Gate Driver Design

Paralleling MOSFETs have advantages such as lower power losses and better redundancy for power conduction. However, on the control side, paralleling the devices negatively impacts the overall turn-on time of the devices, as the gate driver has to supply energy for six devices instead of two. [24] emphasizes the drawbacks of driving parallel MOSFETs with common gate-source connection; the issues include longer turn-on time and circulating currents in the parallel gate-source loops. Therefore, the design of the gate driver should overcome these drawbacks. Also, essential features such as solid control-output voltage isolation and active Miller clamp should be provided.

4.3.1 Signal Architecture

As the bypass switch terminal voltage has *dv/dt*-voltage rates in the range of 10-50 V/ns, there is a strong possibility for high-frequency noise injection into the gate driver circuitry. Without proper isolation, this noise can perturb the control inputs of the gate driver and can lead the gate driver to send unnecessary turn-on signals. Therefore, Driver ICs and power supplies must have strong voltage isolation above 1.7 kV, ensuring the reliable operation of control signals and analog power signals.

Every driver IC typically requires two different power supplies, which are 5 V and 24 V. The 24 V analog voltage is connected to the gate driver's output side, serving as high (VPP) and low voltage (VEE) levels. Therefore, the analog power supply must have high-voltage isolation to

block common-mode noise. Accordingly, a THM 10-2422 24 V/24 V DC/DC converter with 5 kV input-output capacitive isolation is selected after surveying the available power converters.

Another analog power supply of 3.3 V or 5 V is required on the input side of the driver IC. As Driver ICs already contain input-output isolation, an isolated power supply is not necessary. Therefore, MTU2S2405MC 24 V/5 V converter with low 1kV DC input-output isolation is finalized to provide 5 V voltage.

4.3.2 Driving Circuit

The fast operation of bypass switch mainly depends on the selection of driver IC with small delays and good driving strength. After screening many available driver ICs, the UCC21710-QDWQ1 is finalized due to its excellent merits. It provides a small propagation delay of 80-130 ns, 5.7 kV_{RMS} input-to-output voltage isolation, and additional features like a two-level soft turn-off, VEE+2 V active Miller clamp, under-voltage lockout, over-voltage lockout, and 10A drive strength.

Control signals for the driver IC should come from the PEBB1000 gate driver. As a best practice to avoid interference between the boards, fiber optic transceivers and receivers are employed as the communication interface between the PEBB1000 gate driver and the bypass gate driver. The overall signal architecture of the bypass switch gate driver is illustrated in **Figure 4 - 7.**

If a single driver IC has to drive all MOSFETs directly, the driving current for each MOSFET should be limited to 1.67 A (one-sixth of 10 A). With a low driving current of 1.6 A, the turn-on process of MOSFETs gets significantly delayed. Therefore, the topology shown in

Figure 4 - 8 is designed using current boosters and decoupling capacitors to increase driving strength for MOSFETs.

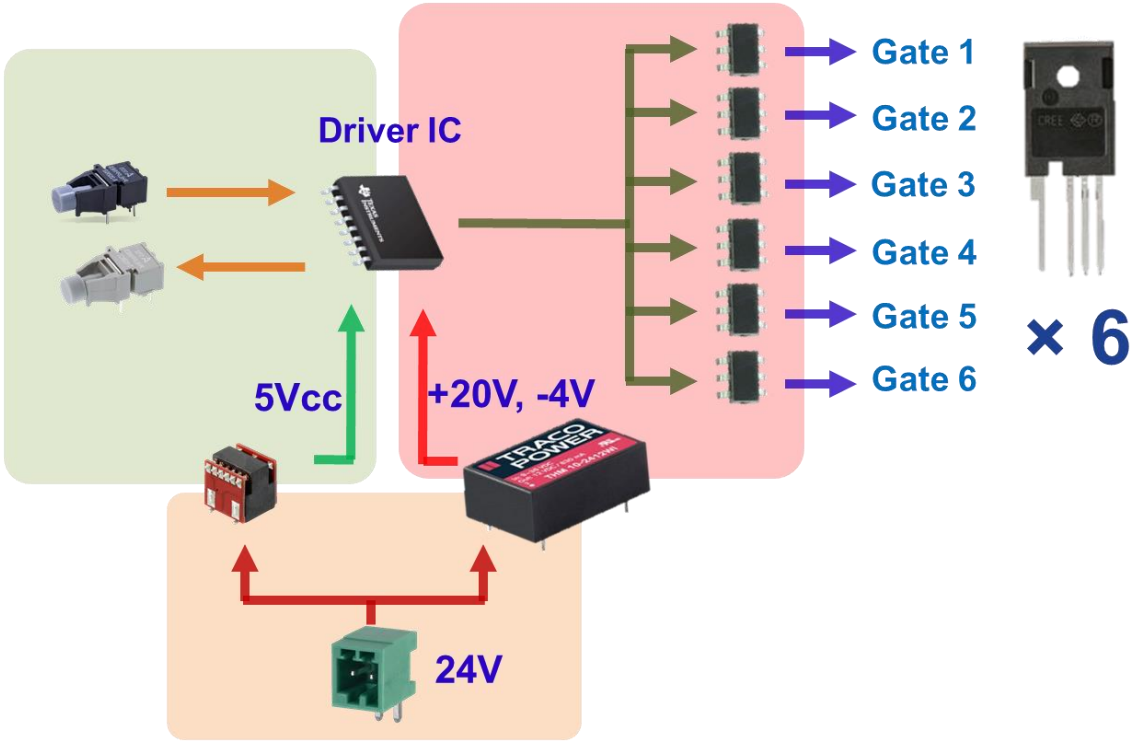

Figure 4 - 7. The architecture of gate driver for driving multiple MOSFETs.

Current boosters ZXGD3006 are selected for their compact size and superior driving current strength up to 10 A. After considering the safe limits, two current boosters are paralleled to provide a maximum driving strength of 13 A (6.5 A each) by selecting gate resistance of 2.2 Ohms**.** This 13 A driving current is achieved only with sufficient decoupling capacitors with appropriate placement close to current boosters. For the designed drive strength of 13 A, the turn-on time of each MOSFET is estimated to be below 50 nanoseconds.

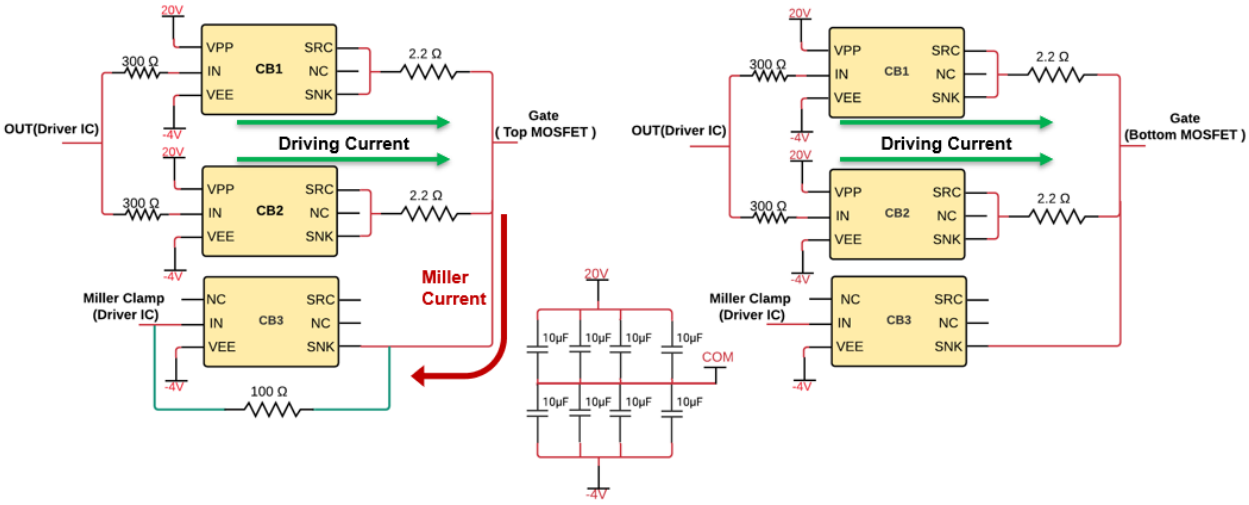

Figure 4 - 8. Gate driving circuit using current boosters.

4.3.3 Active Miller Clamp

The active Miller clamp technique is used to mitigate the negative effects of the Miller current by shorting the external gate resistor when the device is in the OFF state. In general, the driver IC Miller clamp pin is connected to the MOSFET gate, and it monitors the voltage using an internal comparator. When the gate voltage falls below VEE+2.0 V, the Miller clamp pin gets clamped to VEE, and as a result, the external gate resistor is shorted or bypassed. Due to lower resistance, the voltage generated by the Miller current also gets lowered. This helps in reducing the voltage variations of Vgs due to the Miller current.

In case of bypass switch, it is not possible to connect the gates of all six MOSFETs close to the Miller clamp pin of the driver IC. The long traces add resistance and parasitic inductance, which can dilute the effectiveness of the Miller clamp. To address this, [25], [26] implemented the external Miller clamp circuit using current boosters.

Following a similar approach, the external Miller clamp circuit is extended for all six devices. A 100 ohms resistance is connected between the Miller clamp pin of the driver IC and the

MOSFET gate to monitor the voltage. When the Miller clamp pin is clamped to VEE, it acts as a turn-on signal for the current booster. As a consequence, the current booster clamps the MOSFET gate to VEE. The advantage of this external clamp circuit is that current boosters can be placed close to MOSFET gates. It should also be noted that gate voltage monitoring is required only for the top MOSFETs, as shown in **Figure 4 - 4.**

4.4 Heat Sink

In general, efficient thermal management is essential for the heat dissipation of all electrical and electronic devices. In power semiconductor devices, heatsink design is a challenging task due to higher power losses. The selected CREE SiC MOSFETs have TO247 packages with 150°C maximum junction temperature. With poor thermal management, device junction temperature rises above 150 °C leading to permanent device failure. On the other hand, heatsinks occupy more space, decreasing the overall power density. Therefore, application-specific thermal analysis and heatsink optimization is required.

As discussed in Chapter 3, a solid-state bypass switch is required to conduct 100A current for 80ms. After 80ms, the major portion of current flows through bypass EM relay due to its lower ON resistance. So, a thermal analysis is performed for 80 milliseconds of the conduction time. According to TO247 package specifications, case-ambient thermal capacitance is much higher than junction-case thermal capacitance. As a result, case temperature doesn't increase for the first 200 milliseconds of heat flow [25]. Only junction temperature varies with respect to the case temperature for conduction times below 200 milliseconds.

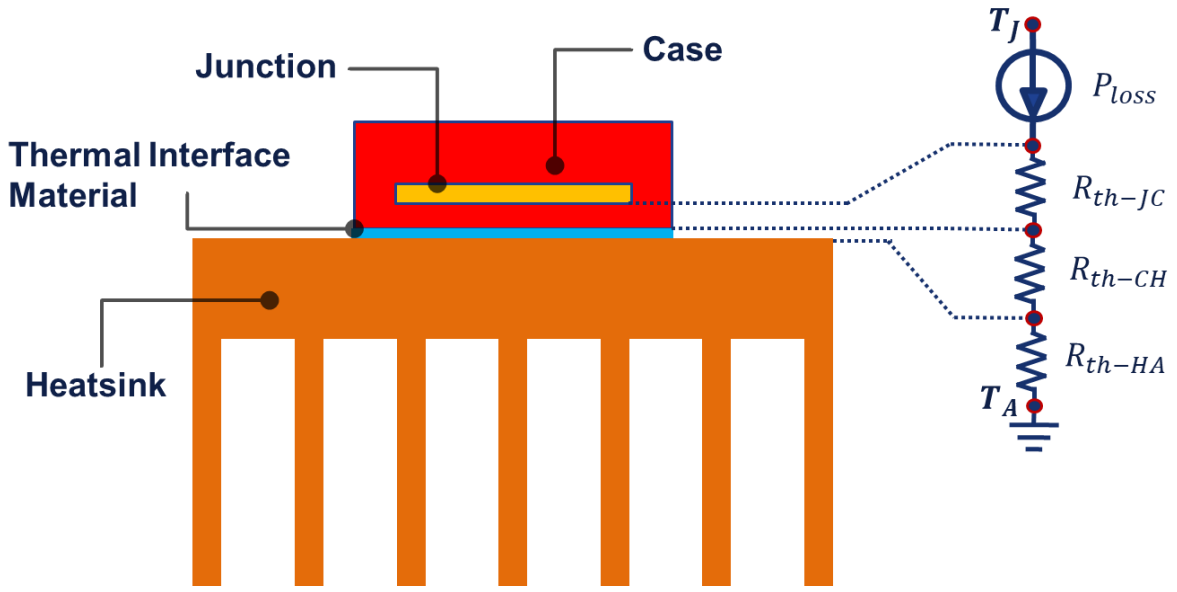

Figure 4 - 9. Thermal pathway for heat dissipation of TO247 packages.

A general steady-state thermal network is assumed for a simpler junction temperature estimation, as shown in **Figure 4 - 9.**

Where:

T_J	is the junction temperature
T_A	is the ambient temperature
P_{loss}	is the heat dissipated from the heat source
R_{th-JC}	is the junction to case thermal resistance
R_{th-CH}	is the thermal interface material resistance
R_{th-HA}	is the heatsink thermal resistance

The power loss of each device is estimated to be 73.5 W using equation (4-1), considering a current flow of 35 A (one-third of 100 A) and 60 milliohms MOSFET ON resistance.

$$I = 35\ Amps,\ R_{DS} = 60\ millohms.$$

(5-1)

$$Power\ Loss = I^2 * R_{DS}$$

$$P_{Loss} = 35^2 * 0.06 = 73.5\ W$$

As case temperature doesn't increase for the first 200 milliseconds of heat dissipation, case temperature stays at the ambient temperature of 50 °C. The case temperature can be maintained at ambient temperature by assuming thermal resistances of the heatsink and thermal interface material to be zero, as shown in the equations (5-2). For 73.5 W power loss and 0.27 °C/W junction-to-case thermal resistance, the maximum junction temperature of the die is calculated to be 70 °C with revised equations.

$$T_J = T_A + \left(R_{th-JC} + R_{th-CH} + R_{th-HA}\right) * P$$

$$T_C = T_A = 50\ ^oC,$$

(5-2)

$$R_{th-CH}, R_{th-HA} = 0, and\ R_{th-HA} = 0.27\ ^oC/W$$

$$T_J = 50 + 73.5(0.27) = 70\ ^oC$$

From thermal analysis, it is concluded that a heatsink is not strictly required for conduction times below 200 milliseconds. A ceramic heatsink is designed for the safety of tests, as shown in **Figure 4 - 10.** As ceramic material is an electrical insulator, MOSFETs can be directly mounted on the heatsink without thermal interface materials. Also, the heatsink maintains case temperature for all MOSFETs at the same value, which supports equal arm current sharing amongst three parallel MOSFETs. As a future study, the heatsink can be improved to support continuous current conduction by varying dimensions and providing forced air cooling.

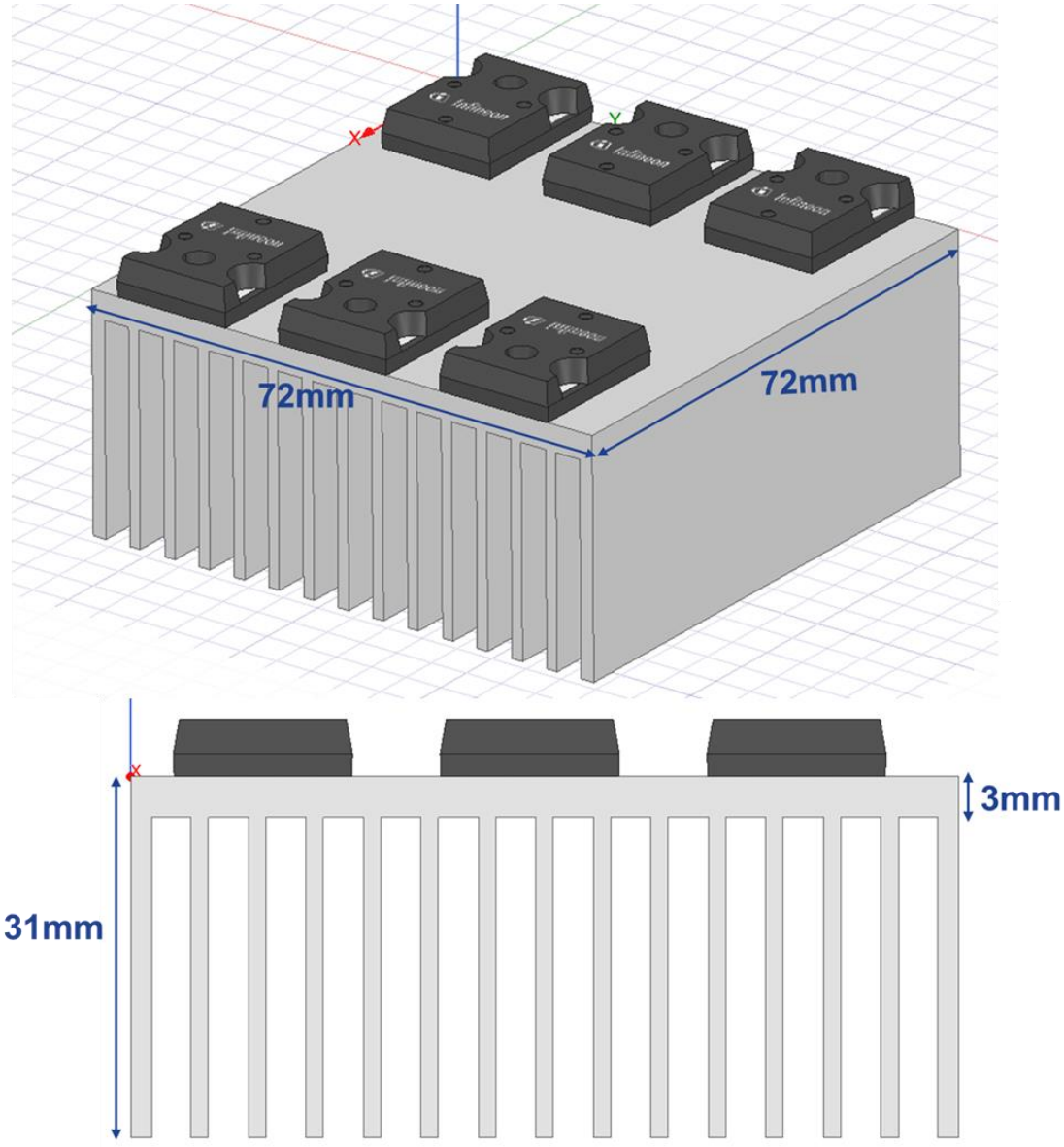

Figure 4 - 10. Ceramic heatsink design for the bypass switch

Chapter 5 Bypass Switch Testing

5.1 Introduction

The bypass gate driver and bypass power PCBs have been fabricated according to the design explained in Chapter 4. Practical tests have been conducted to validate the effectiveness of the design. The bypass switch is not tested directly with MMC due to the limited laboratory facilities and risks involved with high-voltage testing. Instead, equivalent testbeds are designed and built to verify various design targets, such as transient currents, *dv/dt*-voltage rate endurance, and bypass commutation with the PEBB1000.

5.2 PCB Design

Following the schematic presented in Chapter 4, the gate driver PCB for the bypass switch has been designed using the Altium designer. Each MOSFET gate is driven with separate current boosters and decoupling caps, as shown in **Figure 5 - 1.** This compact placement ensures less interference between parallel driving paths alongside shorter current loops with less parasitic inductance.

Design regulations from the IPC-221 have been practiced providing sufficient trace widths according to the current magnitudes. Circular and rectangular board cutouts are made on the PCB to allow MOVs and power terminals from the power board for a compact board stack. Also, all gate driver components are placed at least 7 mm apart from the power terminals to maintain clearance distance to account for the high voltage differences (1.5 kV). For the interface with the controller, driver IC status is sent back to the main controller via an optical transceiver, and an actuating signal for the bypass switch is received through an optical receiver.

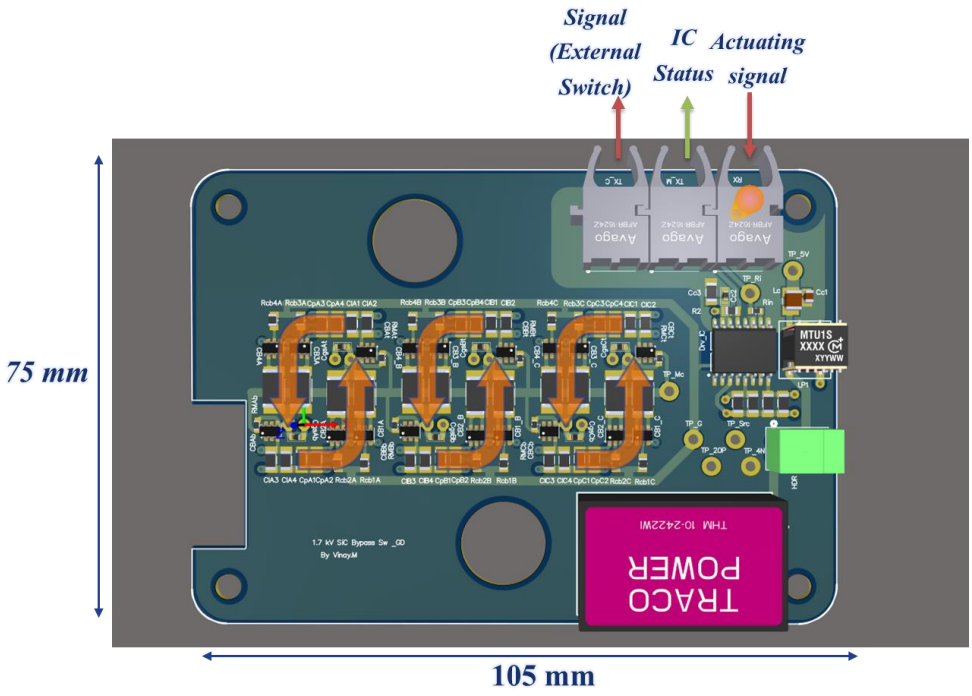

Figure 5 - 1. Gate driver PCB for bypass switch.

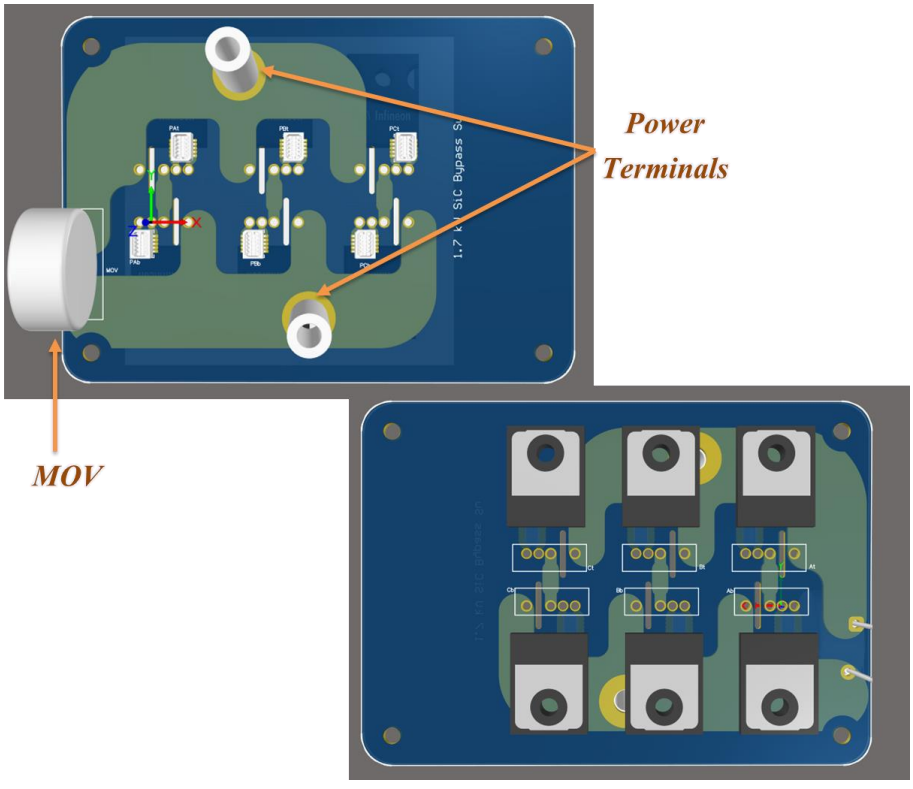

Figure 5 - 2. Power PCB for the bypass switch.

An additional optical transceiver is incorporated into the gate driver to send the bypass EM relay an actuating signal. In summary, the designed gate driver PCB, 10.5 cm * 7.5 cm, should be capable of driving six MOSFETs in the anti-series topology with a common source connection. The turn-on time of the bypass switch is estimated to be around 55 ns as per the design.

The common source connection between top and bottom MOSFETs is made on the bypass power board, as shown in **Figure 5 - 2**. Parallel traces of 4-ounce copper are placed on the top and bottom layers of the PCB to achieve a continuous conduction capability of 100 amperes without overheating the PCB. MOV-20D112K is selected as the varistor to limit the maximum terminal voltage at times of fault; with a maximum clamping voltage of 1600 V. According to the V-I characteristics from the datasheets, paralleling two MOVs would reduce the clamping voltage to 1500V due to smaller currents of 50 amperes through each MOV. The addition of MOVs increases the reliability of the bypass switch operation and reduces voltage stress on PEBB MOSFETs.

The Mezzanine connectors with a 50Vac rating are selected to interconnect gate-source connections between the gate driver and the power boards. These connectors allow fast current conduction while providing good mechanical support**. Figure 5 - 3** shows the overall stack of the fabricated and populated gate driver and power PCBs. Slots have been placed between the drain and source pads on the power board to increase the creepage distance from 4mm to 10mm. These slots are filled with garolite sheets to provide a similar clearance distance in the air medium.

Figure 5 - 3. Complete bypass switch PCB stack with control circuitry.

5.3 Test Plan

Validation of the bypass switch through tests is a challenging task since it requires an entire MMC with multiple PEBBs. Due to the limited laboratory resources of one PEBB/arm MMC, bypass switch testing could not be performed at the MMC level. Instead, three equivalent tests are designed to verify the design targets finalized in Chapter 3: the surge pulse test, the current commutation test, and the *dv/dt*-voltage rate endurance test.

The purpose of the surge pulse test is to validate that the bypass switch could safely conduct the observed transient currents during bypass operation. The test setup should be able to generate high currents up to 800 A for a duration of about 200 µs.

The purpose of the current commutation test is to verify that the major features of the bypass switch -- such as the proposed turn-on sequence, commutation between PEBB and bypass switch and 100A conduction for 80 ms. The testbed should replicate the PEBB operation in parallel with the bypass switch, with an arm current of 100 amperes.

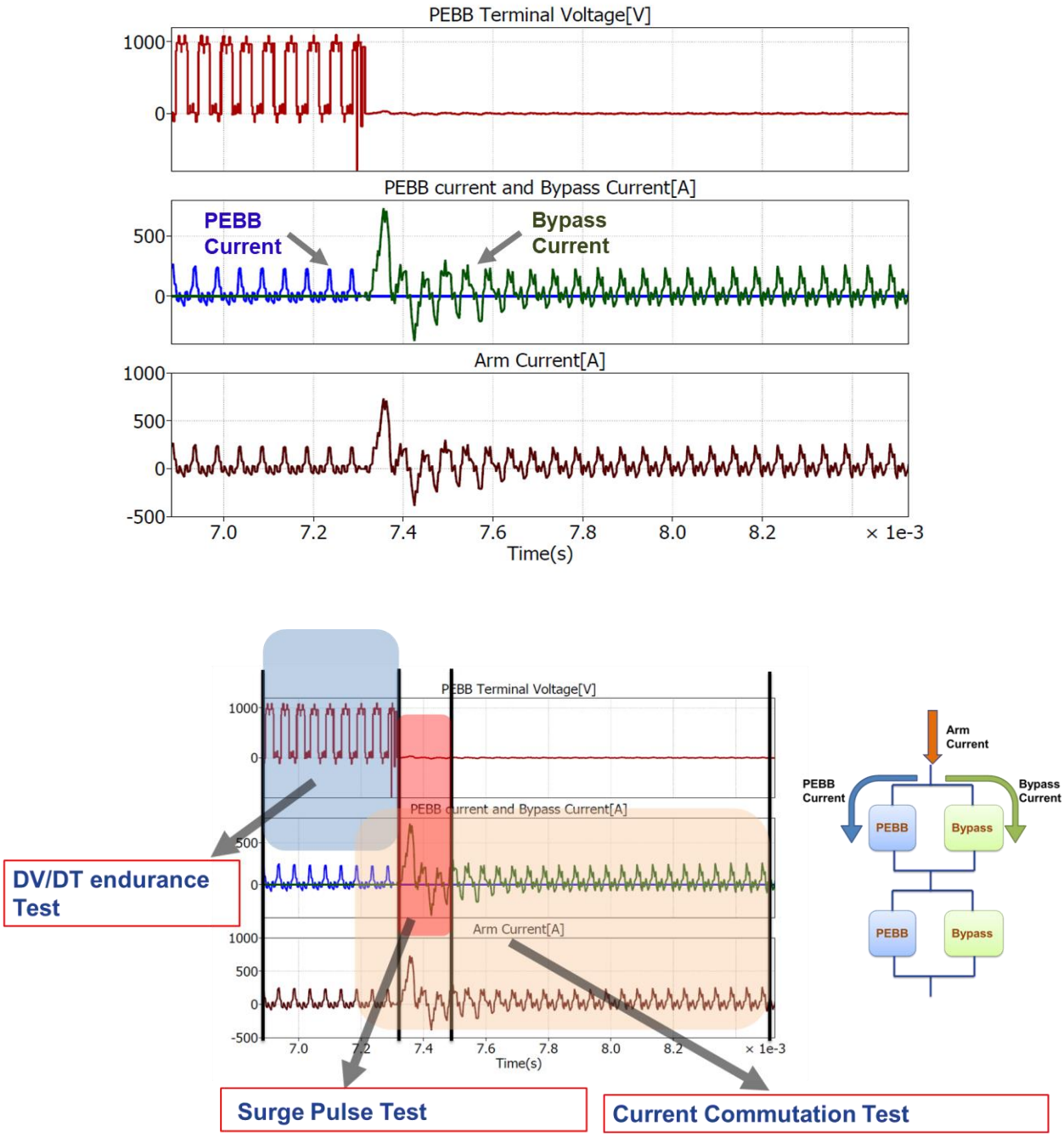

Figure 5 - 4. Test plan to validate transient current, commutation, and OFF-state blocking capabilities.

The purpose of the *dv/dt*-voltage rate endurance test is to verify that the *dv/dt*-voltage rate induced false-triggering and leakage currents of the bypass switch in the OFF-state. The test setup

should generate switching voltage across the terminals of the bypass switch at frequencies higher than 10 kHz.

5.4 Surge Pulse Test

A standard test topology presented in **Figure 5 - 5** has been used for the surge pulse test. The capacitor discharge experiment is implemented to generate the required surge currents. This setup mainly consists of a capacitor bank, a damping resistor, and the equipment under test (EUT). The capacitor bank is pre-charged initially and then discharged through the EUT in series with damping resistance and inductor. The discharge current can be estimated from the RLC second-order system equations, assuming the bypass switch acts as an ideal switch. The 56 µF PEBB capacitor bank, 20 µH inductance, and 1 Ω damping resistance are selected to generate the 200 µs surge pulse, as verified through the RLC step response equations (5-1):

(5-1)

$$\begin{cases} natural\ frequency\ , \omega_n = \dfrac{1}{\sqrt{LC}} = 29.8\ kHz, \\ damping\ ratio, \zeta = \dfrac{R}{2}\sqrt{\dfrac{C}{L}} = 0.83,\ and \\ transient\ settling\ time, \tau_s = \dfrac{5}{\omega_n . \zeta} = \dfrac{10L}{R} = \dfrac{10(20\ \mu H)}{1\Omega} = 200\ \mu s. \end{cases}$$

Initially, the bypass switch stays in the OFF state, and the input power supply charges the 56 µF PEBB capacitor bank up to 1000 V. Once charged, the input power supply is disconnected using a power relay. After disconnecting the power supply, the gate driver will turn-on the bypass switch, which initiates capacitor discharge. By increasing the pre-charged capacitor voltage, surge currents can be increased accordingly without varying the pulse width.

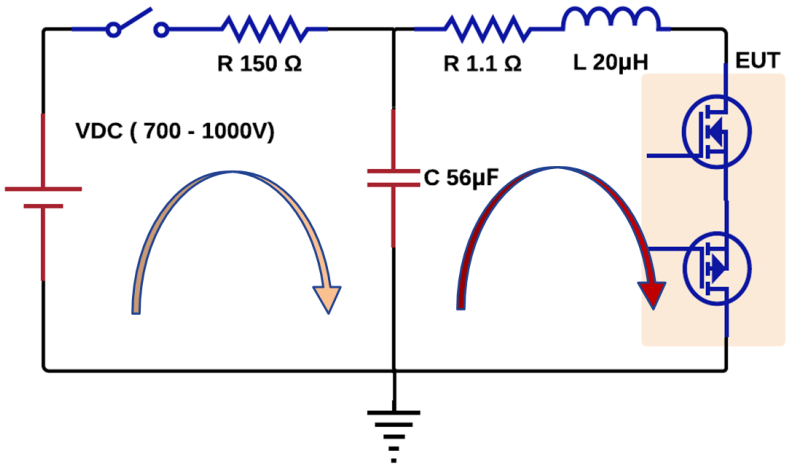

Figure 5 - 5. Surge pulse test topology.

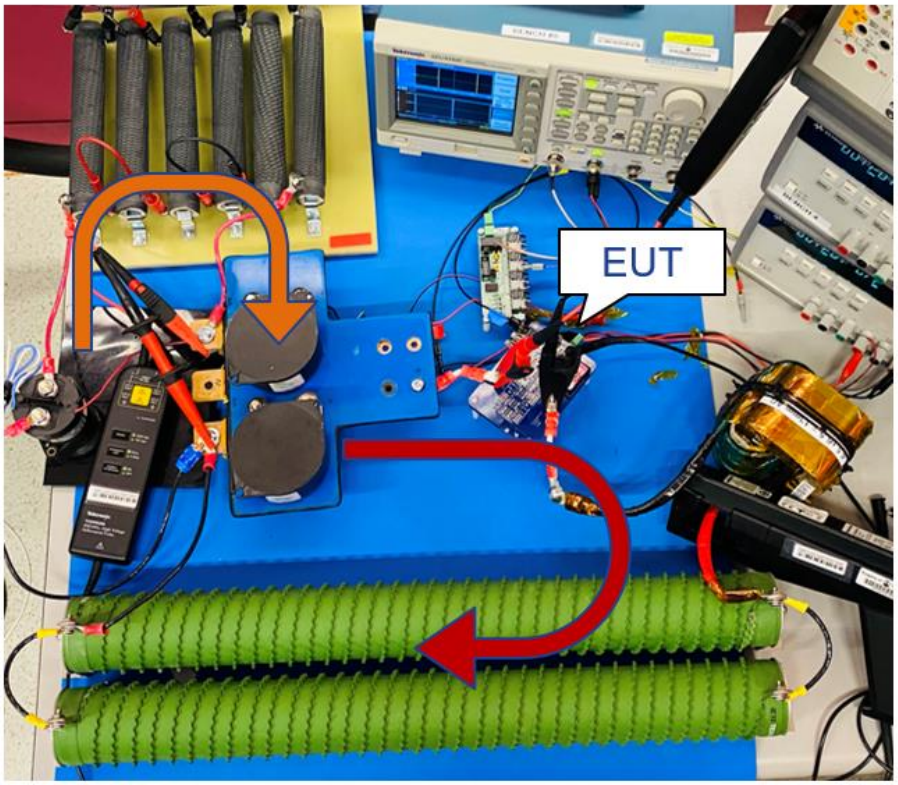

Figure 5 - 6. Surge pulse test setup.

Tests have been conducted using the testbed shown in **Figure 5 - 6** for capacitor pre-charge voltages of 700 V, 800 V, 900 V, and 1000 V. Corresponding discharge current waveforms observed are illustrated in **Figure 5 - 7**, reaching up to 612 A peak current for the 1000 V capacitor pre-charge voltage. Variation in capacitor voltages changed the surge current peak values by maintaining constant pulse durations of around 200 µs.

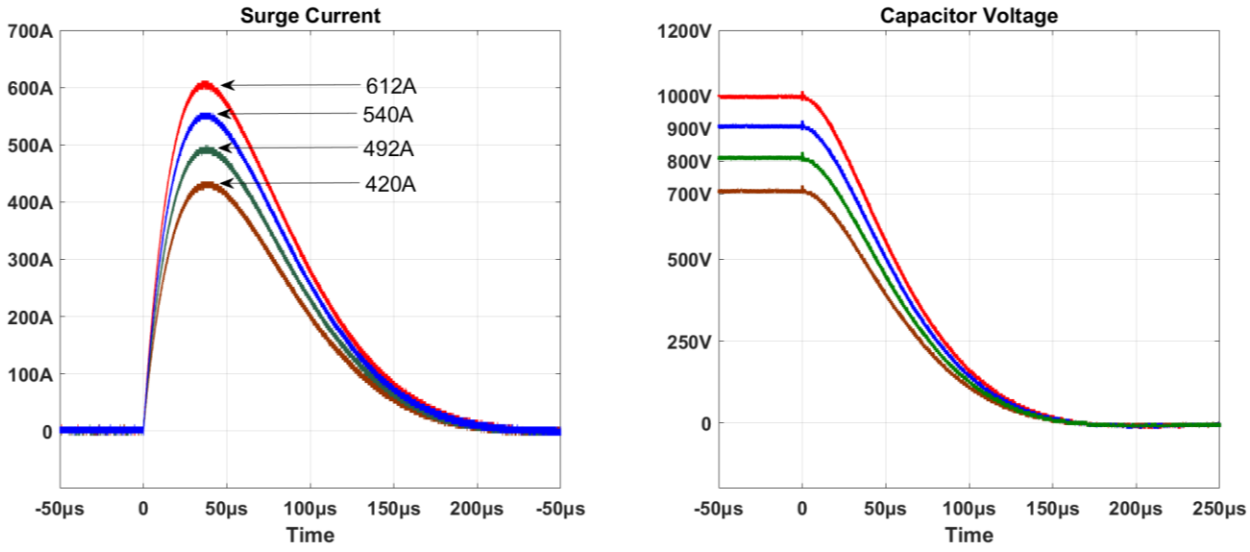

Figure 5 - 7. Surge currents for different pre-charged capacitor voltages.

For the 1000 V pre-charged capacitor voltage test case, the detailed waveforms for bypass switch parameters, such as gate voltage, terminal voltage, switch current, and instantaneous power loss of switch, is presented in **Figure 5 - 8**. The instantaneous power loss of the bypass switch reached up to 27.5 kW, which means a 6.875 kW power loss across individual MOSFETs for equal sharing of current. According to the transient thermal resistance data provided in the MOSFET datasheets, the junction temperature of the devices reaches 150 °C for 7 kW instantaneous power for a single pulse of 200 µs. For the safety of the devices, the maximum surge current through the bypass switch is limited at 612 A.

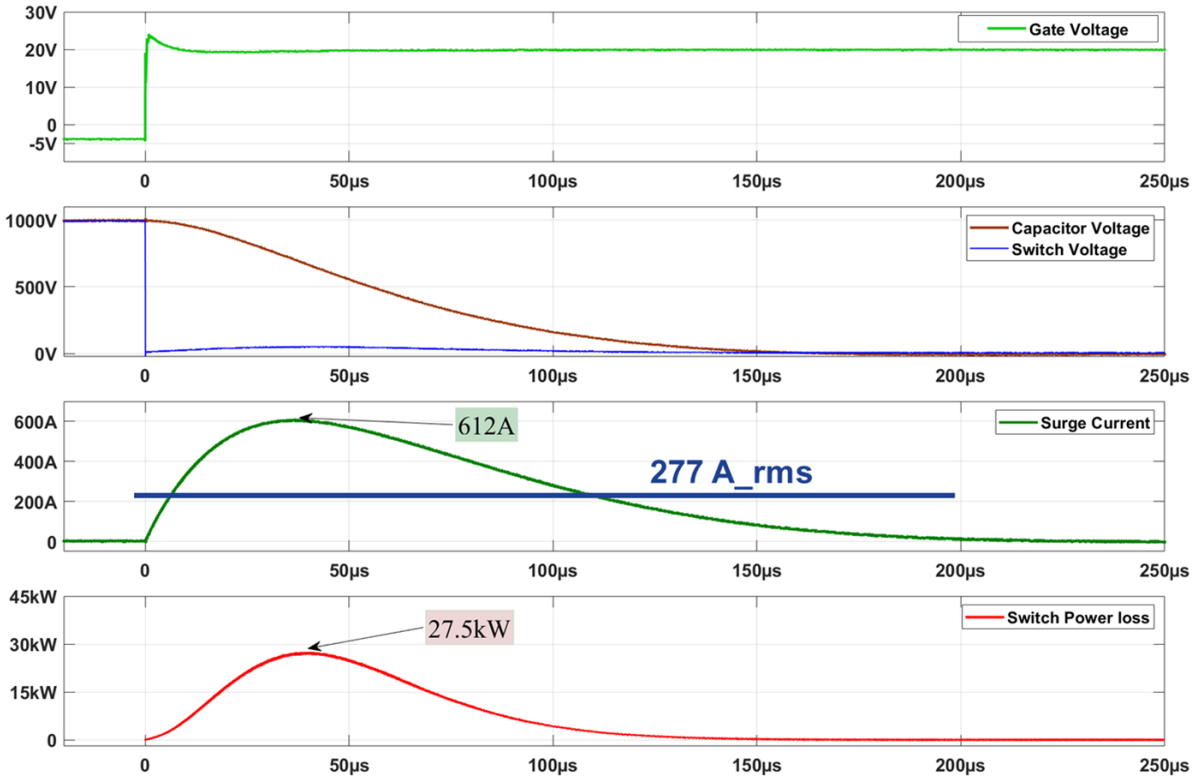

Figure 5 - 8. Surge pulse test results for 1000 V pre-charged capacitor voltage.

5.5 Current Commutation Test

The topology presented in **Figure 5 - 9** has been developed for the current commutation test to replicate the commutation between the PEBB and the bypass switch. To resemble an 'N' PEBBs/arm MMC, input voltage VDC and load resistance R_L will be adjusted to generate the load current with the same RMS value of MMC arm current. L_{PEBB} represents the PEBB inductance, and L_{LOOP} represents the total loop inductance of the remaining 2N-1 PEBBs in the upper and lower arms. Circuitry highlighted in blue represents an equivalent of PEBB, and circuitry highlighted in green represents the designed bypass switch with varistor and mechanical switch in parallel.

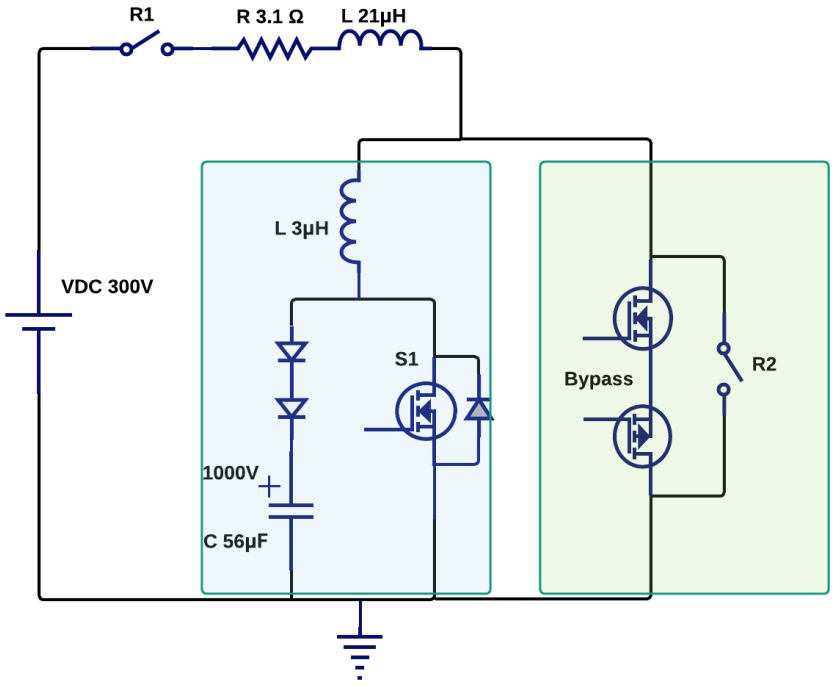

Figure 5 - 9. Current commutation test topology.

The bypassing strategy for faulty PEBB explained in **Figure 3 - 11** in Chapter 3 has been implemented in this experimental setup. Two main events in the strategy are the PEBB shutdown

and bypass turn-on. The arm current path variations for the strategy are clearly shown in **Figure 5 - 10**, along with their equivalent path in the test topology.

For normal operation, the current flowing through switches S1-S3 in the full-bridge is represented by the current through MOSFET S1 in the test topology. Upon an occurrence of a fault, all MOSFETs in the full-bridge circuit will be turned-off, and the arm current will be forced to flow through the MOSFET body diodes and the PEBB capacitor. Similarly, the load current in the test topology will flow through the two diodes and the 1000 V pre-charged capacitor when the S1 switch is turned-off. Once the current starts flowing through body diodes, the bypass switch will be turned-on to provide a low-impedance path for the arm current. This leads to a current commutation between the PEBB and the bypass switch until the PEBB current becomes zero. These commutation paths are identical for actual MMC and the test topology, as highlighted in **Figure 5 - 10 c.**

The topology parameters are chosen based on a four-PEBBs/arm MMC with PEBB capacitance of 56 microfarads and 3 microhenry PEBB inductor (L_{PEBB}). Loop inductance (L_{Loop})is determined as 21 microhenries as a total inductance (7*3 µH) of the remaining seven PEBBs. Load resistance of 3 ohms and a VDC of 300 volts is selected to generate a load of 100 amperes. The **Figure 5 - 11** testbed has been built with the specified component values to validate the commutation between diode current and bypass current.

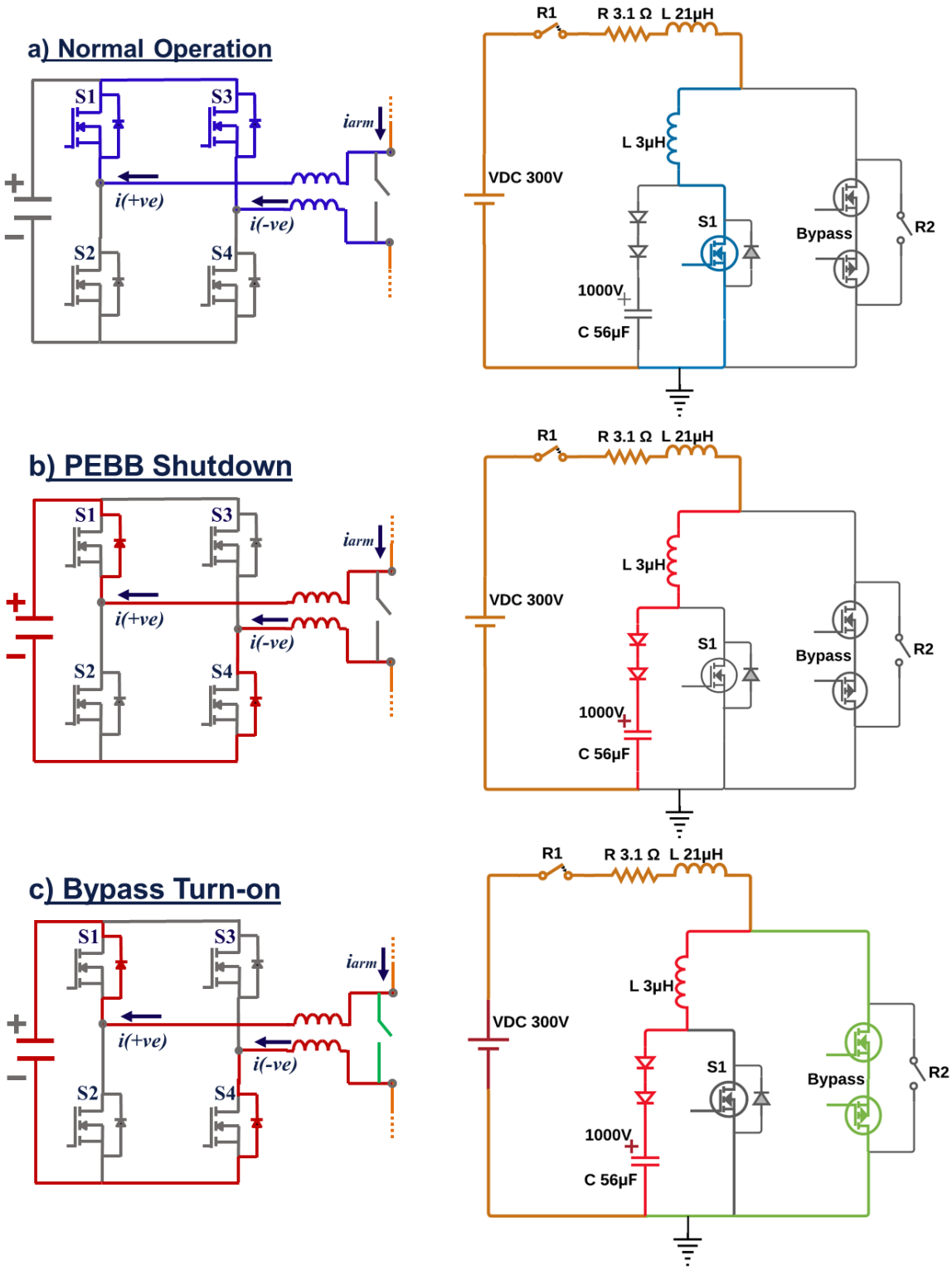

Figure 5 - 10. Equivalent commutation paths of arm current for: a) normal operation, b) PEBB shutdown, and c) bypass turn-on.

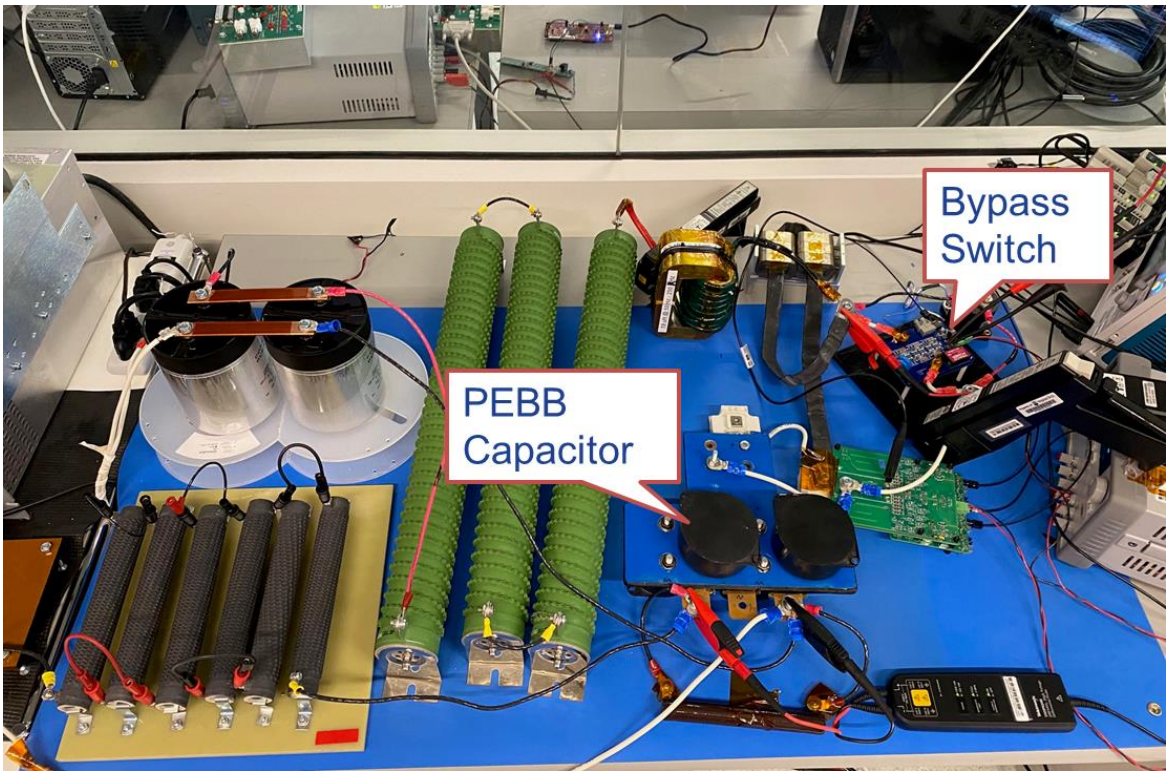

Figure 5 - 11. Current commutation testbed.

The PEBB capacitor will be pre-charged up to 1000 volts using an additional voltage source, keeping all switches and relays in the OFF state. Once the PEBB capacitor is charged, relay R1 and MOSFET S1 will be turned-on to generate 100 amperes current through the 3-ohm load resistor. After 25 milliseconds, MOSFET S1 will be turned-off by the PEBB gate driver. As a result, the load current starts flowing through the diodes into the charged capacitor. Once the load current is transferred from switch S1 to the diodes, the bypass switch should be turned-on as fast as possible to isolate the PEBB quickly.

Tests have been conducted according to the procedure described above. The gate signals of the S1 switch and bypass switch, load current, PEBB current and bypass current, and PEBB capacitor voltage waveforms are presented in **Figure 5 - 12**. The turn-on signal to the bypass switch is given at t=0s. From these waveforms, it can be observed that the load current flows

through the PEBB for 25 milliseconds and transfers to the bypass switch at t=0s. For the next 80 milliseconds, from t = 0s, load current flows through the solid-state bypass switch alone. At t=0.08s, mechanical relay HXNC241 starts conducting, and the solid-state bypass switch is turned-off at 0.09 seconds.

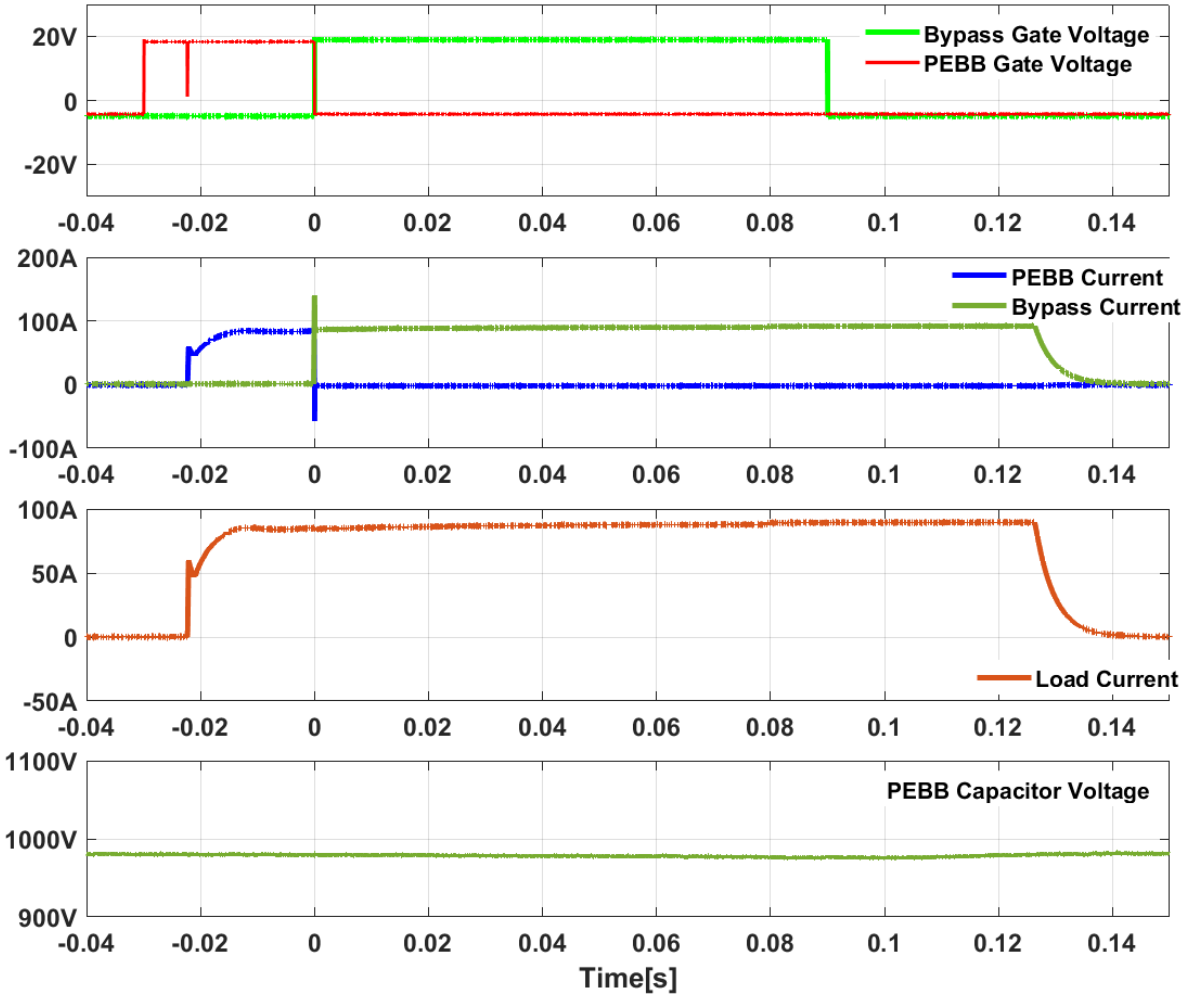

Figure 5 - 12. PEBB and bypass currents according to the proposed bypassing sequence.

The commutation times between PEBB and bypass switch currents are observed in the two microseconds interval between t = -1 µs and t = 1 µs, as presented in **Figure 5 - 13**. As the gate voltage rises to +20 V at t=0s, the bypass switch turns-on and starts conducting current within 52

nanoseconds from t=0.052 µs. The bypass current increases from 0 A to +145 A with a 350 A/µs rise rate, whereas the PEBB current decreases from 85 A to -50 A with a 350 A/µs fall rate in the same interval. This additional sixty amperes (145-85) in bypass current is caused by the reverse recovery current of the body diodes in the power module. A negligible impact is observed by the recovery current on the load current, as the current is circulating between the PEBB and the bypass switch.

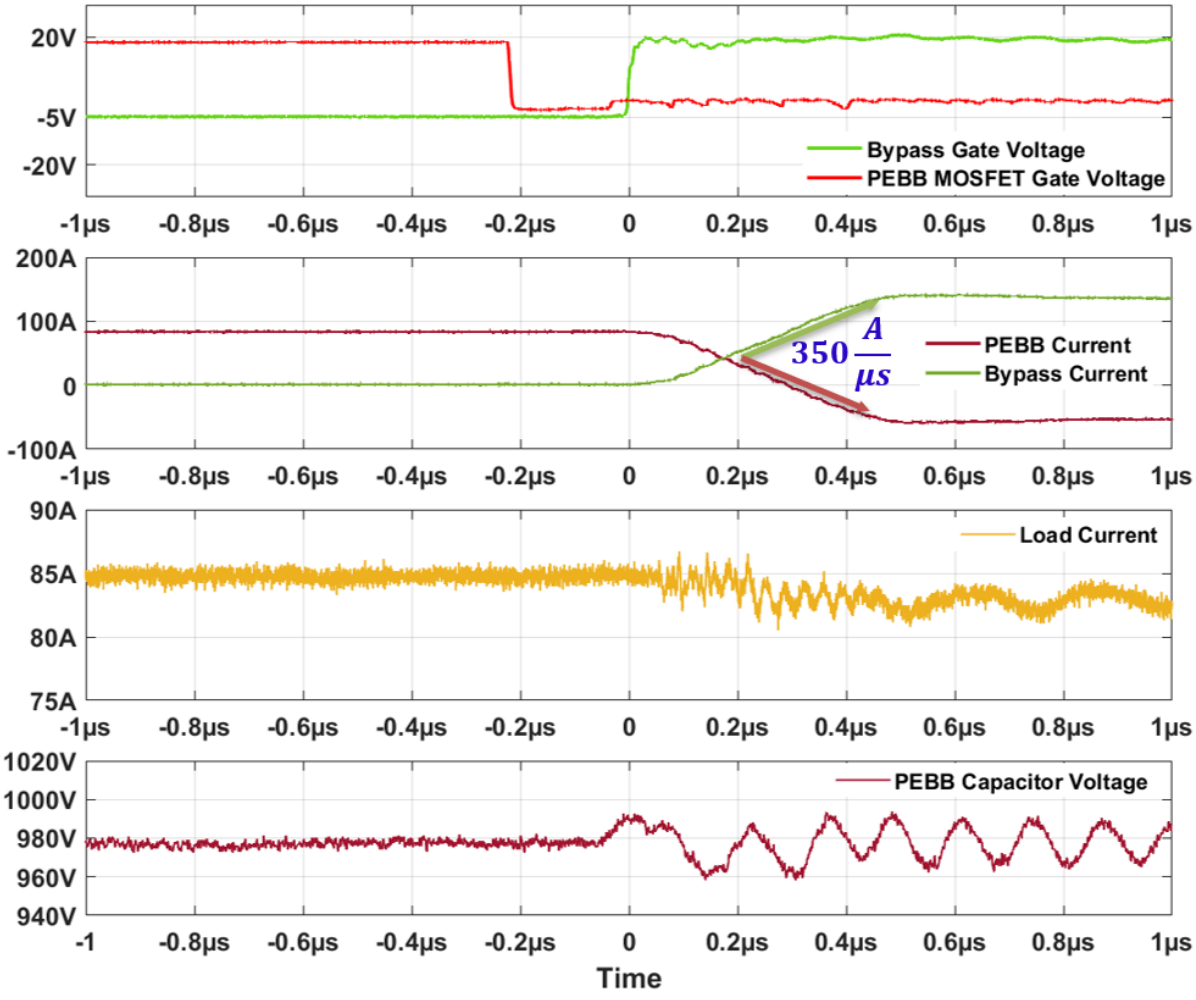

Figure 5 - 13. Commutation between PEBB current and bypass current at t = 0s.

In between t = 0.052 µs and 0.46 µs, the PEBB capacitor voltage 1000 V appeared across the 3 µH PEBB inductance, as the bypass switch voltage is turned-on. Therefore, the bypass

current is dependent on PEBB inductance 3 microhenry and PEBB capacitor voltage, according to (5-2):

(5-2) $$\frac{\Delta i}{\Delta t} = \frac{V_C}{L_{PEBB}} = \frac{1000\,V}{3\,\mu H} = 333.4\ \frac{A}{\mu s}.$$

In summary, the successful operation of the bypassing strategy and the bypass switch operation is verified. The conducting capability of the solid-state bypass switch of 100 amperes current for 80 milliseconds is achieved heatsinks. The total commutation time is 460 nanoseconds (52 + 408), with 52 ns bypass switch turn-on time and 408 nanoseconds for current transfer between the PEBB and the bypass switch. Even though reverse-recovery current increases the current through the bypass switch, the load current is maintained constant at 100 A with a 2 A current ripple.

5.6 Dv/dt-Voltage rate Endurance Test

The topology of the *dv/dt*-voltage rate endurance test is a buck inverter with the bypass switch connected as EUT across the AC switching terminals, as shown in Figure 5 - 14. The bypass switch is kept in the OFF state throughout the test by clamping the gate voltage to the VEE. While the half-bridge inverter operates, switching pulse between zero and DC input voltage appears across the AC terminals. When the AC terminal voltage varies from zero to VDC and VDC to zero, the voltage rise rate and fall rates are high enough to induce Miller currents through MOSFETs. Therefore, connecting bypass switch as EUT between the buck converter AC terminals can act as a good test setup to test false triggering of the devices.

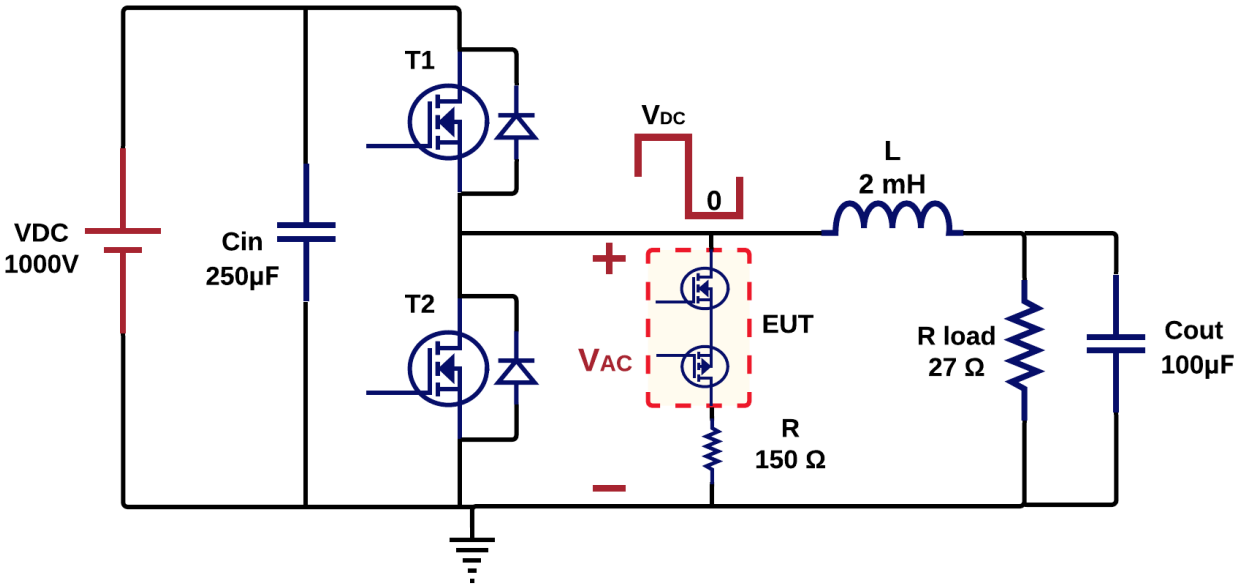

Figure 5 - 14. Dv/dt-voltage rate endurance test circuit topology.

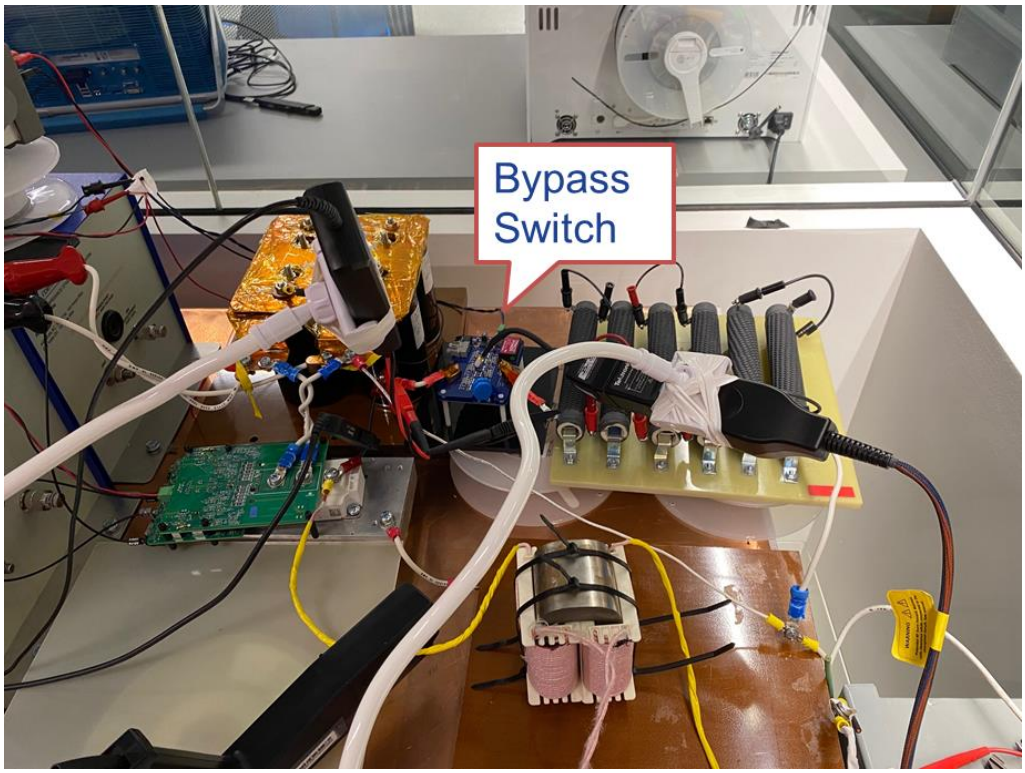

Figure 5 - 15. Dv/dt-voltage rate endurance test setup.

The testbed has been built with the inverter, as shown in **Figure 5 - 15**. DC voltage of 1000 V has been applied to the input capacitor 250 microfarads capacitance. A Cree half-bridge module has been used as switching devices operating at 10 kHz frequency with 50% duty cycle. Filter inductance of 2 mH, output capacitance of 100 µF and 27-ohm load resistor. According to the test plan, the bypass switch is connected as the EUT between AC terminals along with150 ohms series resistor to limit the maximum current through EUT if false triggered.

Tests have been conducted at 50% duty cycle and 10 kHz switching frequency. Bypass switch parameters, such as the terminal voltage, switch current, and bypass gate voltage, are monitored in oscilloscope and waveforms presented in **Figure 5 - 16** are observed. The terminal voltage increased to 400 volts from zero around t = 0s, with a positive *dv/dt* rate of 1 volt per nanosecond. For the duration of this voltage ramp, the positive *dv/dt*-voltage rate across switch terminals induced a maximum leakage current of 1.4 amperes through parasitic capacitances. As this leakage current flows through gate resistance of MOSFETs, gate-source voltage varied from -4.7 V to -4.1 V.

Alternatively, the terminal voltage decreased from 400 volts back to zero volts around t = 50 µs, with a negative *dv/dt*-voltage rate of 0.8 volts per nanosecond. For the duration of this voltage ramp, the negative *dv/dt*-voltage rate across switch terminals induced a maximum negative leakage current of 1.4 amperes through parasitic capacitances. As this leakage current flows through gate resistance of MOSFETs, gate-source voltage varied from -4.7 V to -5.2 V.

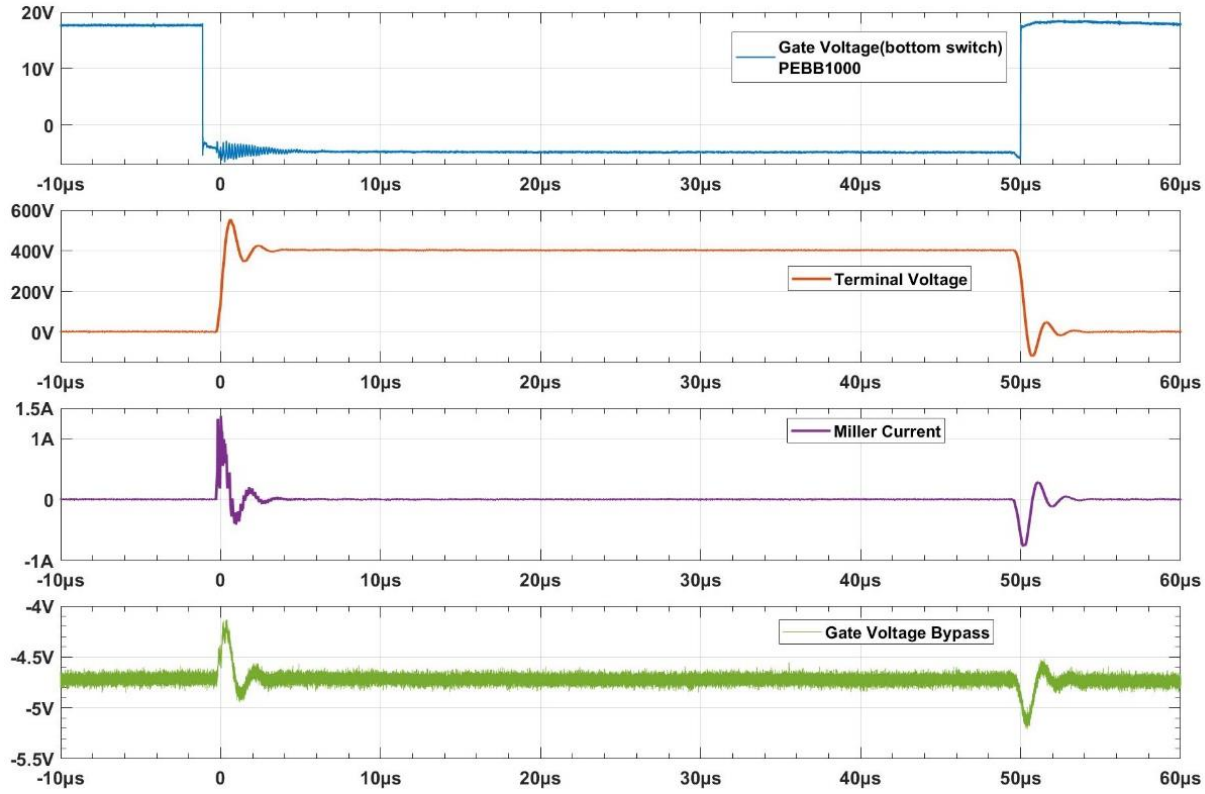

Figure 5 - 16. Gate voltage variation for *dv/dt*-voltage rate across switch terminals.

By analyzing the observed waveforms, a simple estimate of Vgs drop for the 50 V/ns required ramp rate shows that Vgs can vary VEE+/- 30 V (0.6*50) with leakage currents up to 50 A. If the estimate is accurate, the leakage currents and gate voltages are not acceptable, and the bypass switch could be easily false-triggered.

Higher leakage currents have been observed for *dv/dt*-voltage rates deviating from the design. Eventually, these high currents resulted in increased gate-source voltage drops. Test setups should be improved to provide the 50 V/ns *dv/dt*-voltage rate. Suppose the problem persists at 50 V/ns *dv/dt* rate, parasitic capacitance tests should be conducted for the designed bypass switch to analyze variations in parasitic capacitances for terminal voltages from 0 V to 1700 V. According

to the observed parasitic capacitances, a proper snubber must be designed to reduce the leakage currents.

In summary, no false triggering was observed with the testbed for 1 V/ns terminal voltage *dv/dt* rate. However, estimation of Vgs at 50 V/ns voltage rate shows high chances of false-triggering and high leakage currents. Test setups must be improved to provide a 50 V/ns terminal voltage *dv/dt* rate for future work. Static characterization of devices should be conducted to account for variations in leakages currents from the design.

5.7 Conclusions

The test results show that the bypass switch tested with 4 MOSFETs met most design requirements, such as 142 ns operation time and transient current capability up to 600 A. At the same time, the continuous current capability of 100 A for 100 milliseconds and current commutation with the faulty PEBB is validated through the current commutation test. From these test results, the total time for bypassing PEBB from the time of fault is estimated to be 1240 nanoseconds according to PEBB1000 control circuitry. Due to limited resources, the *dv/dt*-voltage rate endurance test is conducted at a 1V/ns *dv/dt* rate, which results in a gate voltage variation of 0.6 volts. Comparison of the observed test results with the design targets from Chapter 3 is presented in **Table 5 - 1**.

Table 5 - 1. Comparison between design targets and test results.

Parameter	Design Targets (6MOSFETs)	Test results (4 MOSFETs)
Blocking Voltage	1500 V	1700 V
Continuous Current	300 A Peak 100 A RMS @ 80 ms	85A RMS @ 90 ms
Transient Current	800 A Peak 260 A RMS @ 200 µs	600 A Peak 277 A RMS @ 200 µs
Operation Time	< 300 ns	142 ns Td 80 ns + Ton 62 ns
VGS @ 50 V/ns	VEE +/- 2 V	VEE +/- 0.6 V @ 1 V/ns.
Maximum Clamping Voltage	1300V-1700 V.	1500 V

Chapter 6 Summary and Future work

This thesis presents the design of SiC-MOSFET based bypass switch for 1000V Power Electronics Building Block (PEBB1000) as a submodule in Modular Multilevel Converter (MMC). PEBB1000 is designed for Switching Cycle Control (SCC), with reduced passive components such as capacitors and inductors. This control scheme modulates arm current polarity in every switching cycle at high-*di/dt* rates, can damage traditional TRIAC-based bypass switches. Therefore, a bypass switch has been developed using SiC MOSFETs to meet the challenges set forth by SCC and tested experimentally to prove the effectiveness of the design.

A four PEBBs/arm SCC-MMC model has been developed in PLECS simulation software to extract the design challenges for the bypass switch. Alongside high-*di/dt* rate currents, 260 A current transients and 1.5 kV clamping varistor requirements are observed.

An anti-series topology of 1.7 kV SiC MOSFETs has been developed to meet the design targets, along with a compact gate driver and MOV. Through various experiments, the effectiveness of the designed switch has been validated. The test results proved that the bypass switch could operate in 142 ns, ten times faster using SiC MOSFETs than thyristors-based TRIACs. Also, 100 A current operating current and 277 A transient current capabilities are achieved.

This thesis work mainly focuses on proving the effectiveness of SiC MOSFETs for the initial bypass requirements extracted from SCC- based MMC. Therefore, more research can be conducted to understand design requirements better and improve the bypass switch design.

On the bypass switch, further research can be continued in the following topics:

- Development of SCC modulation scheme after bypassing one of the faulty PEBBs.

- Analysis of the bypass switch characteristics with improved test setups that emulate faulty PEBBs.
- Design of snubber circuit to avoid high *dv/dt*-voltage rate across the bypass switch terminals.
- Design of heatsink to achieve continuous conduction capability as a bidirectional switch.
- Health monitoring of the bypass switch by incorporating a high-bandwidth current sensor in the bypass gate driver.

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