Thermo-mechanical Analysis of a Custom PCB-DBC Hybrid Package for a (650 V, 150 A) e-GaN HEMT

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ABSTRACT

With the potential to improve upon silicon (Si) based power electronics exhausted, the push for improvement now lies with wide bandgap (WBG) materials like gallium nitride (GaN). With a larger bandgap, higher electron mobility, and higher electrical field strength than Si, GaN high electron mobility transistors (HEMTs) can have lower on-state losses and higher switching frequencies in a smaller package. This makes GaN HEMTs an attractive choice for compact, high efficiency power devices.

However, the package designs used for Si cannot be used for GaN HEMTs, requiring novel, chip-scale designs that are optimized for low electrical parasitics and low thermal resistance. Recent Center for Power Electronics (CPES) research culminated in a printed circuit board-direct bonded copper (PCB-DBC) hybrid package to house a 650 V, 150 A GaN HEMT. Called the PCB-Interposer-on-DBC package, it utilizes a DBC for heat extraction while using vertical pin interconnects to minimize electrical parasitics.

Previous work did not investigate the design's locations of expected failure or reliability. With thermally generated mechanical fatigue a consistent cause of electronics failure, it must be investigated for the design to move beyond the prototyping phase. Thermo-mechanical fatigue failure is the brittle fracture of bonds caused by thermally induced warpage. The thermal warpage is the consequence of the bonded package components having a coefficient of expansion (CTE) mismatch while being subjected to temperature changes during operation. Multiphysics simulation software have previously quantified the fatigue placed on bonds exposed to these cyclic conditions, with a common metric being the volume-averaged inelastic strain energy density gained per cycle (ΔW_{avg}). ΔW_{avg} can identify which bonds are subjected to the greatest amount of fatigue and will thus fail first, and then quantify the effect of design alterations on those vulnerable bonds. A common design alteration seen in solder ball packaging is adding a

polymeric material that encapsulates the bonds. If the polymer has a CTE like that of the package substrates and an elastic modulus (E) exceeding 1 GPa, it constrains the thermal warpage and lowers bond fatigue.

This thesis uses thermo-mechanical simulations to provide evidence on which bonds fail first in the package, and that material-based methods of fatigue reduction used in solder ball packing apply to this novel package. Chapter 1 explains how a desire to reduce the cost and increase the performance of electric vehicles led to the development of the PCB-Interposer-on-DBC design, and that the package's response to thermo-mechanical fatigue is unknown. The concepts of thermo-mechanical fatigue and using encapsulants to reduce it are established, along with how simulations are used to study said fatigue. Chapter 2 serves two purposes, the first being an explanation of the simulation settings and metrics used to establish the quality and assumptions used, and the second being a beginners guide on how to create these simulations.

Chapter 3 identifies the most probable locations of initial package failure and identifies what encapsulants minimize ΔW_{avg} on those locations. The sintered silver bond expected to fail first is the Internal Gate bond, and an encapsulant with the maximum possible E and 8 ppm/°C minimizes ΔW_{avg}. The Sn60Pb40 bond expected to fail first is the External Source 4 bond and using an encapsulant with the maximum possible E and a CTE of 24 ppm/°C minimizes ΔW_{avg}. While ΔW_{avg} cannot determine which of the two bonds fails first as they are made of different materials, the Internal Gate is prioritized as it has a higher per-cycle fatigue and to prevent loss of the gate signal.

Chapter 4 demonstrates how to perform a brief encapsulant study while ranking the expected cycles to failure when using four different encapsulant options. The first two options are to use no encapsulant or silicone gel. As the elastic modulus of silicone gels are too low to restrict or couple the thermally generated warpage, using silicone gel results in a ΔW_{avg} comparable to using no encapsulant. The rigid encapsulant with the properties most like the optimal encapsulant identified for Internal Gate has the lowest

ΔW_{avg} of the encapsulants tested. Guidelines are established for what properties an encapsulant must have to outperform said rigid encapsulant.

This work uses simulations to provide evidence that encapsulant methods used in ball grid array (BGA) packaging to reduce fatigue apply to a novel GaN HEMT package. By identifying the first-failure locations of the package, establishing what existing encapsulant should be used, and what encapsulation it should eventually be replaced with, these results provide the groundwork for both experimental temperatures cycling and more complex simulations. Such work fills the gap in understanding the reliable lifetime and common failure mechanisms of the PCB-Interposer-on-DBC package.

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GENERAL AUDIENCE ABSTRACT

In modern engineering, the cause of failure in a well-designed electronic device is typically not a single event. Rather, it is the culmination of many smaller events that each cause a minor amount of damage. This cycle of repeated, minor damage is called fatigue.

When working with power or IC electronics, the most common type of fatigue occurs due to the device's changing temperature. Electronics undergo continuously changing temperatures due to the environment and their own energy losses, causing repeated cycles of heating and cooling. All materials expand upon heating and contract upon cooling , and the magnitude of this change is the coefficient of thermal expansion (CTE). Electronic devices are comprised of dissimilar materials, so disparate components will expand and contract at different rates. Holding these disparate materials together are bonds, which in the process of holding this warped structure together, also deform. This deformation causes permanent damage, which accumulates in the bonds until they break. As these bonds often serve as pathways for the electrical signal or heat extraction, their failure either degrades or breaks the electrical devices.

While preventing bond fatigue is impractical, there are strategies to extend the operating lifetime. A common option used elsewhere is to encase the bonds with a polymer. If the polymer's properties are carefully selected, they can reduce the structural warpage, thereby reducing the fatigue on the bonds.

Previous Center for Power Electronics (CPES) research has culminated in a new electronics device called the Printed Circuit Board-Interposer-on-Direct Bonded Copper package (PCB-Interposer-on-DBC package). While general trends suggest which bonds will fail first and what kind of polymers reduce fatigue, this information has not yet been

confirmed. This thesis uses computer simulations to identify which bonds will likely fail first, and to provide evidence that existing methods for reducing fatigue are viable for this unique package. The simulations work by subjecting a 3D model to a cycle of heating and cooling, called a temperature cycle, and quantifying the damage sustained by the bonds for every cycle.

Chapter 1 describes the relevant details leading to this package design, the importance of thermo-mechanical reliability in the design of electronics, and how to use simulation software to quantify reductions in bond fatigue. Chapter 2 explains how to set up these simulations and evaluate their quality. Chapter 3 identifies the initial locations of package failure and identifies what are the most optimal encapsulants to use. Chapter 4 identifies what existing encapsulant will maximize the package lifetime in experimental temperature cycling.

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Chapter 1. Introduction

1.1 Purpose of Chapter 1

The purpose of this chapter is to introduce a broad goal, the reduction of greenhouse gases to combat climate change, and then narrow it to a specific set of objectives that this work seeks to complete, a simulation-based investigation into using encapsulants to increase the cycles to failure of bonds in a novel GaN HEMT package.

Section 1.2 addresses the role of the transportation industry as the United States' single largest contributor of carbon dioxide. While replacing combustion vehicles with electrical vehicles would resolve the issue, convincing consumers to switch means making electric vehicles more appealing. One issue is that the electric powertrain is too expensive, too large, and lacks the power to scale to larger vehicles, resulting in electric vehicles that are more expensive and have worse performance versus combustion vehicles.

Section 1.3 focuses on correcting this issue. Replacing the silicon power electronics used in the powertrain with wide bandgap electronics will rectify the mentioned issues but introduce new ones. Regarding gallium nitride as a silicon replacement, the issue is that commercial, high power gallium nitride technology is not mature. While high output power is possible, it requires an undesired amount of complexity. However, a die of greater output power is available, but must be packaged before use.

Section 1.4 describes the PCB-Interposer-on-DBC package, a design created to package this die. A synopsis of the structure is included, along with what is still unknown about the package, which includes the failure mechanisms and operating lifetime.

Section 1.5 describes why fatigue failure commonly limits package reliability, and how it often manifests as cracked bonds. The advantages and disadvantages of exploring this failure using

experimental temperature cycling or simulations are discussed, with this thesis work being a simulation analysis with expected verification in future work.

Section 1.6 explains how the material properties of the polymeric encapsulants have been utilized in other packages to reduce the thermal fatigue on the bonds expected to fail first. A list of both commercial and academic encapsulants with their material properties are listed to highlight the expected properties of various materials. Of the choices listed, ME-531 is utilized in Chapter 3 because it is the original encapsulant used, while EP-2000 is an available material expected to outperform ME-531 due to a lower CTE mismatch and higher stiffness.

Section 1.7 is a summary of the thesis objectives and outcomes.

1.2 Using Electric Vehicles to Reduce Greenhouse Gases

This section focuses on the steps that the United States federal government and partnered companies are undertaking to reduce the greenhouse emissions that come from the transportation sector. The main thrust of decarbonizing transportation is the replacement of internal combustion engine vehicles with either electric or hybrid vehicles. To both improve these vehicles and their market penetration, a 2017 roadmap established that the size and cost of the internal electrical components must be brought down. To achieve these requirements, the internal power electronics must become smaller, less expensive, and have increased power density.

The Intergovernmental Panel on Climate Change concluded that 'the likely range of human-induced warming in global-mean surface air temperature in 2010–2019 relative to 1850–1900 is 0.8°C–1.3°C', with greenhouse gases (GHGs) being a contributing factor [1]. Carbon dioxide (CO_2) is the most common GHG, with it accounting for 79 % of all GHGs generated within the United States in 2021 [2]. Due to the consumption required by industrialization and higher living standards, the concentration of atmospheric carbon dioxide (CO_2) has increased 44 % between 1850 and 2021 [3].

Identifying CO_2 emission sources is the first step to mitigating the effects of GHGs on the environment. The US Department of Transportation identified the transportation sector as a 'significant source' of GHGs, and that finding alternative fuel sources and decreasing vehicle miles traveled are necessary to reduce those emissions [4]. The US Energy Information Administration determined that transportation was the single largest emitter of CO_2 within the US in 2021, accounting for 37 % of all CO_2 emissions. The use of petroleum products accounted for 97 % of that CO_2 generated [2].

One method to decarbonize the transportation industry is the mass replacement of personal internal combustion engine (ICE) cars with electric drive vehicles (EDVs). EDVs are classified as any vehicle using an electric motor and inverter, which includes both hybrid and battery electric vehicles (BEV). Current electrification efforts focus on the light duty vehicles (LDVs), which are the largest consumers of energy [5] and generators of CO_2 [6]. Wide-scale

replacement of combustion LDVs with EDVs is needed to reduce the GHG generation of the transportation sector, and current EDVs already have the capability to function as replacements. While acknowledging there are financial, hardware, and infrastructure roadblocks to mass adoption, [7] determined that a 2013 Nissan Leaf BEV using a single charge would satisfy the driving requirements placed on 87 % of LDVs, which would reduce US personal gasoline usage by 61 %. However, to reap these benefits, consumers must actively choose EDVs over ICEs.

For consumers to embrace EDVs, they must be competitive versus ICE vehicles in price and performance. Both parameters for an EDV depend heavily on the powertrain, which consists of an energy supply and the means to turn it into vehicle motion. In a BEV, the powertrain contains a battery and charging system, a DC-AC inverter that supplies the electric motor and transmission, and several DC-DC converters. This work is concerned with the electric traction drive system (ETDS), a powertrain subgroup that can be seen in Fig. 1-1. The EDTS is responsible for converting the battery's DC signal into an AC signal that drives the engine and provides torque to spin the wheels.

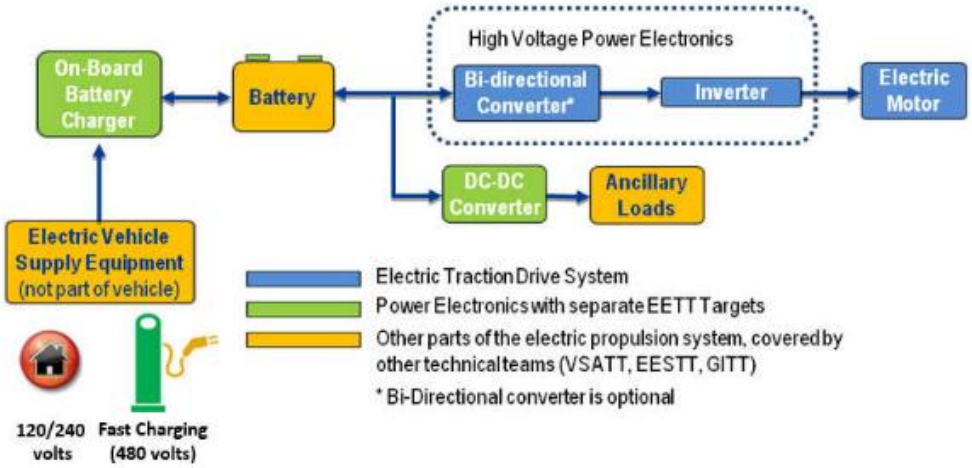


Fig. 1-1. A BEV power train. The blue boxes are the ETDS components, with this thesis primarily focused on the power electronics used in the converters and inverter [8].

The Electrical and Electronics Tech Team (EETT), a Department of Energy subgroup, designs ETDS that meet or exceed ICE vehicle performance. To make EDVs that are both economic and on-par with ICE performance, EETT released a 2017 roadmap outlining what improvements to the ETDS they desire by 2025. Specifically, they want an ETDS capable of handling a 100-kW

peak system with a power density of 33 kW/L and cost of $6/kW [8]. The increase in peak power is desired for improved performance and the electrification of heavier vehicles. However, the crucial outcome is a more compact ETDS at lower cost. The entire powertrain must fit inside a vehicle chassis like in Fig. 1-2, placing a premium on size and weight.

Fig. 1-2. A Skateboard Chassis that contains the electric powertrain, including the ETDS [8].

The roadmap also establishes how the ETDS will be altered to meet said goals. As power semiconductor devices are the heart of the ETDS inverter and converters, the cost and power density of these switches influence the size and cost of the ETDS. Table 1-1 compares the commercial 2017 parameters against the desired 2025 parameters for a 100-kW inverter module, while Table 1-2 compared the state-of-the-art 2017 inverter technology against the desired 2025 inverter. The primary objectives are to reduce inverter size and cost, which means size and cost reductions in both the internal power electronics packaging and surrounding electrical and thermal systems. The secondary objective is to increase the output power for improved performance.

Table 1-1. 2017 Commercial Power Electronics Parameters Compared To The Desired 2025 Parameters [8]

Parameters	On-road in 2017	2025 R&D Target	% Difference
Cost ($/kW)	10	2.7	-67 %
Power Density (kW/L)	18	100	+455 %

Table 1-2. Current State-of-Art Inverter Specifications Compared to the Desired $270, 1 Liter 2025 Inverter [8]

Requirement	State-of-Art (WBG)	Integrated Inverter 2025
Peak Power (kW)	30	100
Continuous Power (kW)	15	55
Voltage Rating (V)	900 – 1,200	900
Maximum Device Current (A)	100	200
Device Metallization - Top	No	No
Device Metallization - Bottom	Yes	Yes
Maximum Junction Temperature	180	250

1.3 Utilizing Existing GaN HEMTs to Accomplish 2025 Objectives

This section focuses on the replacement of silicon power semiconductors with wide bandgap materials like gallium nitride. This change will result in smaller power packages and smaller supporting systems at a net decrease in cost. This helps achieve the 2025 EDTS goals of reducing size and cost. While the existing output power of commercial gallium nitride packages requires an expensive and complex inverter building block design, there are unpackaged dies that could reduce the cost and complexity. However, they must be packaged to use them.

Achieving the objectives listed in Tables 1-1 and 1-2 with conventional silicon (Si) power electronics is unlikely, as they are currently insufficient and are reaching their material limits. Therefore, the use of wide bandgap (WBG) power devices, such as silicon carbide (SiC) metal oxide field effect transistors (MOSFETs) or gallium nitride (GaN) high electron mobility transistors (HEMTs) is necessary. Table 1-3 details the improved material properties of SiC and GaN over Si, while Fig. 1-3 shows the achieved and theoretical values of Baliga's figure of merit for several packages. A wider bandgap allows for operation under more extreme thermal or electrical conditions, which can be leveraged for the high-temperature operation expected in EDVs. When combined with its greater electron mobility and higher electrical field strength, GaN can operate with lower on-state losses and higher switching frequency than Si [8], [9], [10], [11]. In summary, GaN chips can be smaller, have lower on- and off-state losses, and operate at higher temperatures than a Si chip in the same scenario. The higher operating frequency reduces the size of passive electrical components in the inverter, while higher operating temperatures can reduce the size of thermal management systems. While current WBG semiconductors are more expensive than Si, a net reduction in system cost is expected due to the improvements described above [8], [12]. As EETT's primary goals are a reduction in cost and size of the ETDS components, replacing Si with WBG materials like GaN is appealing.

Table 1-3. Comparison of Si Material Properties Against SiC and GaN [9], [12]

Parameter	Si	SiC	GaN
Bandgap (eV)	1.1	3.26	3.49
Electron Mobility (cm^2/V s)	1500	700	2000
Electron Saturation Velocity	1.0	2.0	2.8
Electric Breakdown Field	0.4	2	3.3
Thermal Conductivity (W/cm^2	1.5	4.5	>1.5
Relative Permittivity (ε_r)	11.8	10.8	9.0
Manufacturing Cost	1.0	1.7 → 1.0	*GaN-on-Si:* 1.0 → 0.6

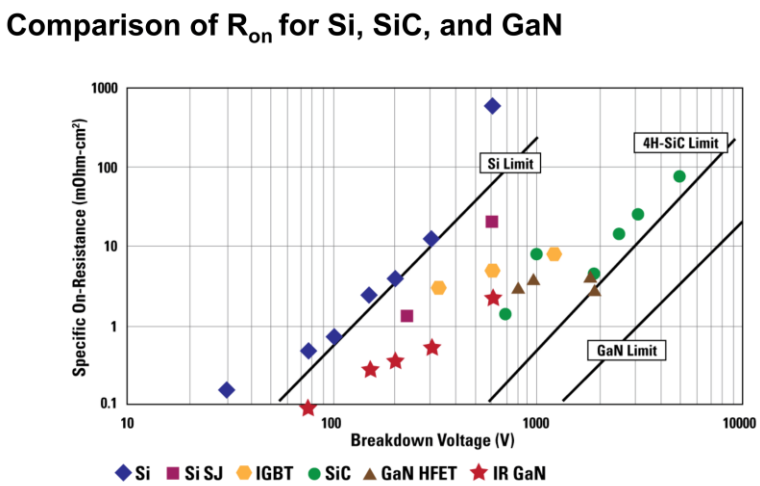


Fig. 1-3. Comparison of Baliga's Figure of Merit for Si, SiC, and GaN. Breakdown voltage and resistance are related as increasing the distance over which the blocking electrical field is sustained increases both the allowable voltage and the electrical resistance of a current passing over that distance [13].

Referring to Fig. 1-4, the 100-kW region lies firmly within the predicted domain of SiC, not GaN. While SiC appears to be the optimal solution, the following section focuses on the potential of a GaN HEMT solution for two reasons. The first is that investigation of high power GaN is useful for establishing GaN's upper limits. The second reason is that this work regarding the thermo-mechanical redesign of GaN package is applicable regardless of how the package is used.

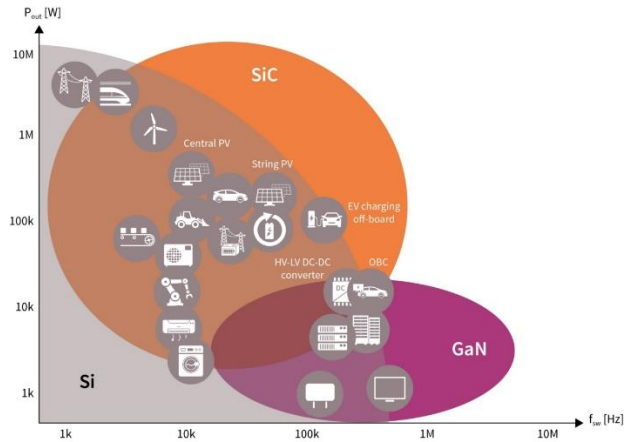


Fig. 1-4. Expected output power and frequency ranges for Si, SiC, and GaN. The EETT guidelines request a 100-kW inverter [14].

A direct way of evaluating GaN's current commercial ability is to design EETT's desired inverter using commercial GaN HEMT packages. Using GaN System's GS66516T package rated for 650 V and 60 A at ambient temperature, [15] builds a half-bridge building block and identifies a lack of output power as a major constraint in using commercial HEMT packages. Fig. 1-5 shows the 3-phase inverter building block. When considering the three-phase inverter, if V is the line-to-line voltage, I is the RMS current, and pf is the power factor, then the output power P of the three-phase inverter is

$$P = \sqrt{3} * pf * V * I. \tag{1}$$

With a desired output power of 100 kW, a desired line-to-line voltage of 520 V, and an arbitrary power factor of 1, the required RMS and peak currents are 111 A and 157 A, respectively. As the GS66516T has a peak current rating of 47 A at an operating temperature of 100 °C, the half bridge needs at least four sets of parallel devices for a total of eight HEMTs. While the 100-kW objective was met, the need for eight packages increases the cost and leads to challenges in matching and minimizing electrical parasitics. To mitigate these issues, a HEMT package with greater output power is required.

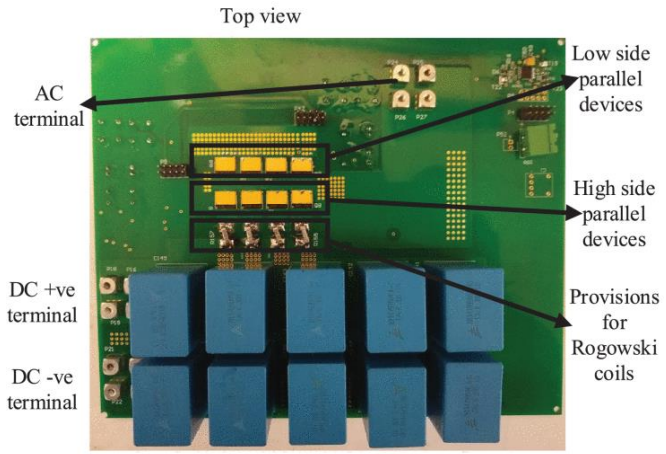


Fig. 1-5. The half bridge building block rated at for the EETT inverter. Eight GS66516T packages are required to achieve the peak requirement of 100 kW [15], [16].

While 60 A is the maximum rating for commercial HEMT packages as of writing, there are unpackaged HEMT dies with higher current ratings. Specifically, the GS-065-150-1-D2 die from GaN Systems is rated for 650 V and 150 A at ambient temperatures, and is shown in Fig. 1-6 [17]. If the packaged die is used in place of the 60 A package, the building block would require fewer parallel HEMTs, reducing the design complexity. However, the GS-065-150-1-D2 is only sold as a die, so it must be packaged before it can be used, which is a non-trivial task.

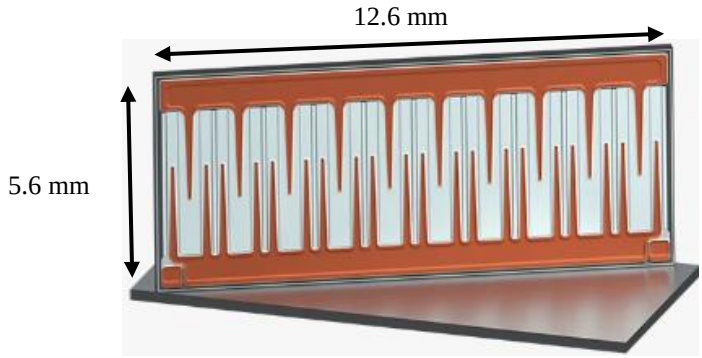


Fig. 1-6. The GS-065-150-1-D2 die [17].

1.4 The PCB-Interposer-on-DBC Design

This section focuses on the advantages and unknowns of the design utilized to package the 150 A die. While the electrical performance has been experimentally validated and the thermal performance predicted using simulations, the failure mechanisms of the package have not been studied. How this package fails and what mechanisms resist this failure need to be understood.

The five considerations when designing GaN packaging are a minimization of electrical parasitics to operate at higher frequency and reduce heat loss, a minimization of thermal resistance to reduce size and increase operating lifetime, minimization of package size, avoidance of design choices to reduce reliability, and feasibility of construction. For a more comprehensive discussion of these parameters and how various packaging designs compare, see Chapters 1.3 and 1.4 of [18]. To summarize, the Si-based packaging designs severely limit the capabilities of the GaN HEMTs while the die-embedded-in-PCB methods are either inaccessible, require non-standard fabrication, or are vulnerable to thermo-mechanical fatigue due to a coefficient of thermal expansion (CTE) mismatch and high thermal resistance. However, the fabrication, CTE, and thermal resistance issues of the die-embedded packaging could be improved if the die is kept close to the PCB instead of inside it. This is the premise of the new design.

To retain the parasitic advantages of the die-embedding while improving the heat extraction and manufacturability, a new design called the PCB-Interposer-on-DBC was built to house the 150 A die [18], [19]. While [18] contains multiple 150 A designs, this analysis is restricted to the single chip, single-side cooled package that uses pins for all electrical interconnects. To pre-empt confusion, the original HEMT packaged in [19] was rated for 120 A, but the die's rating has since increased to 150 A without any dimensional change. Fig. 1-13 shows both a completed package and a cross-sectional diagram. Table 1-4 compares PCB-Interposer to the 60 A GaN*PX* package.

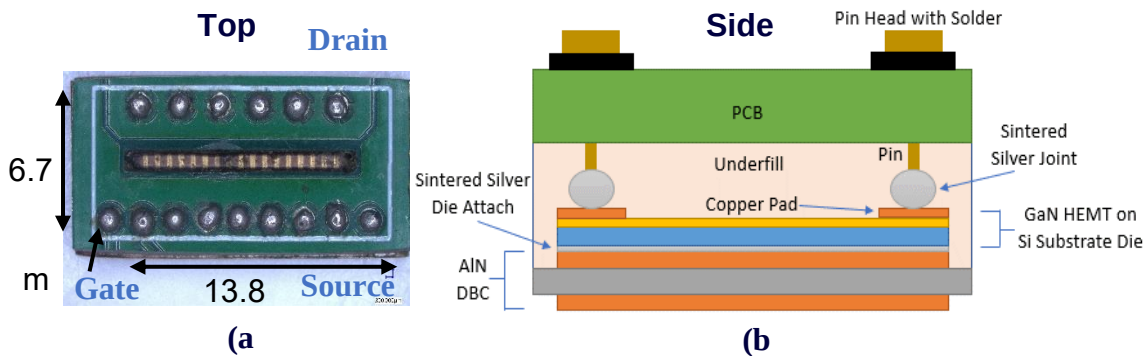


Fig. 1-7. (a) Top and (b) side views of the PCB-Interposer-on-DBC design. Heat extraction is through the bottom DBC, while the nickel pins are used as lateral interconnects. While the prototype used PCB pads for external bonding, the pin heads themselves are intended to be the point of external connection and are shown in (a) [18], [19].

Table 1-4. Comparison of PCB-Interposer with the GS66516T [18], [20]

Package	Current Rating (A)	Size (mm)	$R_{th\text{-}JC}$ (°C/W)	Specific $R_{th\text{-}JC}$ (°C*mm^2/W)	Current/Surface Area (A/mm^2)
GaN*PX*	60 (maximum)	9.0 x 7.6 x 0.54	0.27	18.47	0.88
PCB-Interposer	150	13.8 x 6.7 x 2.8	0.14	12.94	1.62

Sintered silver (Ag) is used for both the die attach and the die-to-pin connection to create robust bonds with a thermal conductivity exceeding 100 W/m*°C . The combination of a sintered Ag die attach and DBC substrate gives a simulated $R_{th\text{-}JC}$ of 0.14 °C/W while granting electrical isolation from the heat sink. Gold-plated nickel pins are inserted into the PCB, bonded to the die using sintered Ag, and secured in place with a pin-head-to-PCB solder bond. This gives a simulated drain-to-source inductance of 1.2 nH and a measured on-resistance of 14 mΩ.

While the previous work studied the thermal and electrical properties of the PCB-Interposer and the impact of power cycling on a simplified package, no work regarding the reliability or failure mechanisms of this specific package has been done. Therefore, the mechanism and location of failure, along with the expected lifetime of the package are unknown. Until explored, the package viability in an extreme application like an EV is uncertain. Extensive knowledge of

those topics allows for design alterations that protect the locations of first failure and lifetime models that predict the impact of design or environmental changes.

1.5 Thermo-mechanical Fatigue and Testing Methodologies

The purpose of this section is to explain how variations in temperature lead to mechanical fatigue in packages, and why this is a primary failure mechanism. Then, the advantages and limitations of using simulations to study this behavior are discussed. This thesis will use temperature cycling simulations to study the bond fatigue in the PCB-Interposer-on-DBC package, with future experimental work used to validate the results.

Mechanical fatigue is the process by which repeated loading of a structure causes failure through the initiation and growth of cracks. While the applied load can cause either elastic (reversible) or inelastic (irreversible) structural deformation, it is less than the load expected to cause the material to break (ultimate strength). As most components experience repeated loading or vibration during use, the American Society of Metals estimated "that fatigue contributes to approximately 90% of all mechanical service failures" [21]. While mechanical failure is often a culmination of factors including chemical reactions or creep, the prevalence of fatigue requires any investigation of mechanical failure to either acknowledge it or rule it out.

In electronics packaging, temperature is either a contributing or dominant cause of package failure [22]. Increased operating temperatures increase the failure rate associated with chemical or creep-related processes. However, the impact of temperature is not limited to the operating temperature, but also includes cyclic changes in the operating temperature as the package heats and cools. The heating is from die losses or the surrounding environment, with this heat being extracted by the thermal management systems attached to the package. All materials possess a coefficient of thermal expansion (CTE), which dictates the amount that a material will expand or contract due to a temperature change. Therefore, cyclic temperature changes cause cyclic component deformation which in turn causes cyclic mechanical loading. This thermally generated fatigue is the focus of thermo-mechanical failure and is the primary focus of this section.

The mechanism of thermal fatigue and how it causes thermo-mechanical fatigue is as follows [23]. All electronics packages use a combination of metals, ceramics, and polymers to achieve the desired electrical and thermal capabilities. As each material has a different CTE, there is an

inherent CTE mismatch (ΔCTE) within the structure. These mismatched components are held together by bonds, which prevent any component from deforming freely.

At the stress-free temperature, all components are undeformed, resulting in no applied load. Any deviation from this stress-free temperature causes the components in the package to elastically expand or contract. The bonds holding the structure together constrain this geometry change, resulting in the package warping. Figure 1-14 illustrates this process with a simplified solder ball structure. While the deformation experienced by any component can be approximated as purely elastic, the resulting deformation of the bonds is inelastic, resulting in permanent deformation. By holding the package together through thermally induced warpage, the bonds are damaged. All materials have some density of defects within their crystal structure, and the plastic deformation causes new dislocations to generate and move until they become pinned in place by other dislocations. As this cycle repeats, more defects are generated and become increasingly concentrated due to the pinning. These regions of high defect density degrade the lattice and function as stress concentrators, leading to crack initiation and propagation which breaks the bond.

Cyclic temperature changes generate cyclic mechanical loading on the bonds, which repeats until the bond fails and thus can no longer transmit electrical signals or extract heat from the package. Depending on the bond's purpose, this will degrade performance or cause complete package failure. Therefore, package thermo-mechanics is the study of how thermal cycling leads to bond fatigue failure and the methods to counteract this behavior.

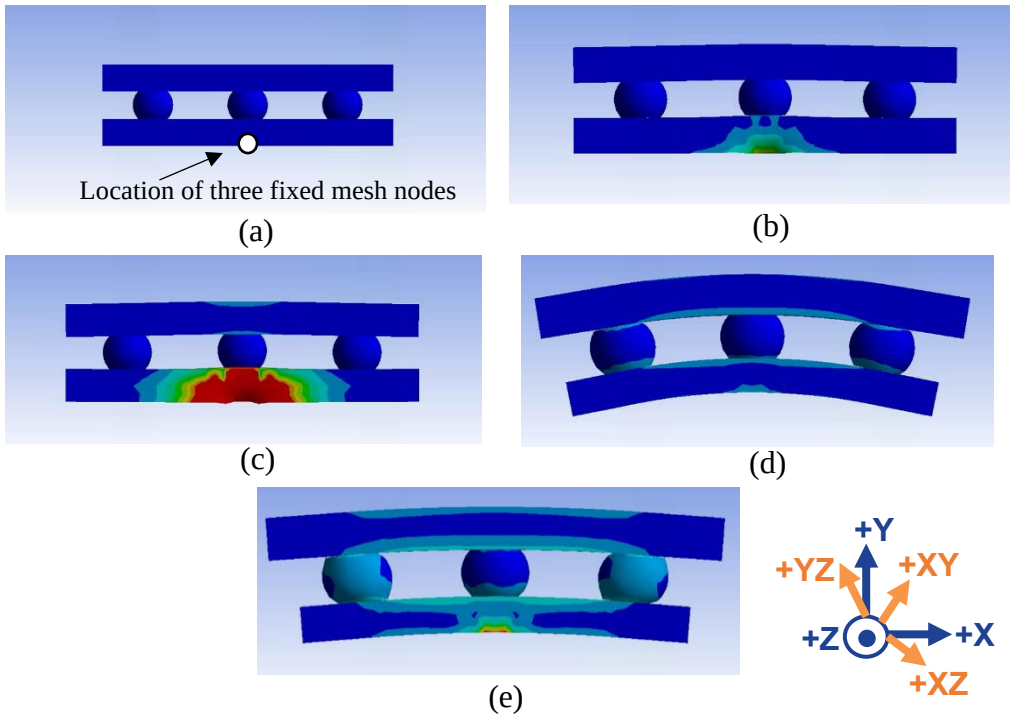


Fig. 1-8. A demonstration of how differences in CTE, elastic modulus (E), and Poisson's Ratio (ν) alter the stress in three solder bonds holding two different substrates together. All deformation is exaggerated, and the contour plots show Von Mises stress using the same scale. (a) The undeformed package at a designated stress-free temperature of 25 °C. (b) The deformed package at 125 °C. All components have the same material properties, resulting in no deformation or stress beyond what the fixed points introduce. (c) The same structure at 125 °C, but now the top substrate, bottom substrate, and bonds are three unique materials. They all possess the same CTE, but have different values of E and ν. The bonds are minimally impacted. (d) The same structure at 125 °C, but now the three materials have different CTE, but identical values of E and ν. Substrate bending is apparent, with increased stress on the solder bond edges. (e) The same structure at 125 °C, but now all three materials have unique values of E, ν, and CTE. The Von Mises stresses in the bonds are highest in (d) and (e) due to the XY shear, displaying the relationship between bond stresses and CTE mismatch.

The causes of this bond fatigue are the CTE mismatches in the package, and the temperature changes during the device's lifetime. While the CTE mismatch and temperature changes can be minimized, neither can be practically removed. Therefore, our strategies for countering thermal fatigue as package designers focus on minimizing the consequences of fatigue as opposed to preventing it.

There are two methods for evaluating package thermal fatigue. The first is using accelerated lifetime experiments, in which manufactured packages are subjected to different methods of heating and cooling until failure or degradation is observed. The tests are "accelerated" because the test conditions are more extreme than what is experienced in operation, which reduces testing

time by causing failures to occur sooner. Table 1-5 estimates the operational thermal cycles to failure of electronics based on the package surviving a given accelerated test profile.

The most basic experiment is temperature cycling, where packages are placed in furnace and subjected to an environmental thermal cycle. An example of this thermal cycle profile is in Fig. 1-15. At designated intervals, the packages are removed from the furnace and their properties are evaluated against a baseline, with the package failing if it falls outside a given range. Thermal shock experiments are similar, except the profile has more extreme ramping and shorter dwell periods to investigate the impact of thermal transients. A third experiment, power cycling, studies the effect of thermal transients by using die losses to heat the package, as opposed to the environmental heating of the previous two methods.

Table 1-5. The 2007 JESD47G Standards from JECEC [24]. The Use Condition Requirements list the expected reliable lifetime and the temperature cycling expected in each scenario. The following columns estimate how many cycles the device will survive in said operation, if it withstands the listed temperature cycling conditions.

Use Condition	**Use Condition Requirement**	**Equivalent Condition B -55 °C to +125 °C 700 cycles**	**Equivalent Condition G -40 °C to +125 °C 850 cycles**	**Equivalent Condition J 0 °C to +100 °C 2300 cycles**
Desktop 5 yr Life	ΔT 40 °C 2000 cy	14,175 cy (12,475 cy)* (11,057 cy)**	14,463 cy (12,761 cy)* (11,332 cy)**	14,375 cy (12,675 cy)* (11,250 cy)**
Mobile 4 yr Life	ΔT 15 °C 1500 cy	100,800 cy	102,850 cy	102,221 cy
Server 11 yr Life	ΔT 40 °C 44 cy	14,175 cy	14,463 cy	14,375 cy
Telecom (uncontrolled) / Avionics Controlled 15 yr Life	ΔT 25 °C 5500 cy	36,288 cy	37,026 cy	36,800 cy
Telecom (controlled) 15 yr Life	ΔT 6 °C 5500 cy	630,000 cy	642,812 cy	638,889 cy
Networking 10 year Life	ΔT 30 °C 3000 cy	25,200 cy	25,712 cy	25,557 cy

*JESD94, Table 1, Consider desktop with add'l ΔT 8 °C for 31,025 cycles and ΔT 20 °C for 1828 cycles

** Consider Desktop with additional ΔT 10 °C for 50,000 cycles

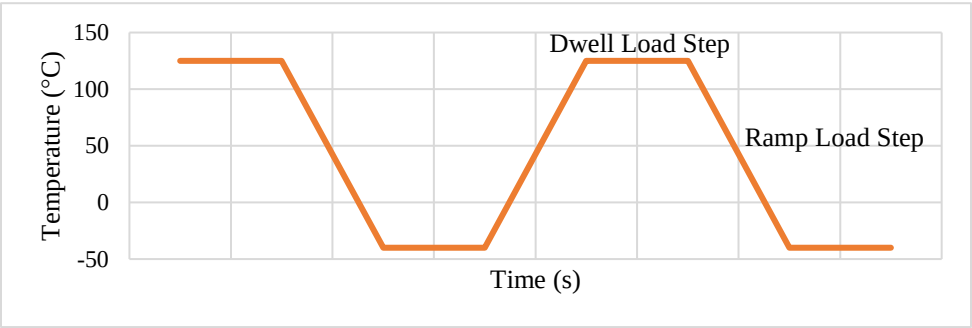


Fig. 1-9. An example of a thermal cycle for either temperature cycling or thermal shock. The major difference between them is that thermal shocking uses higher ramp rates to induce thermal transients in the structure.

The second method of thermo-mechanical evaluation is using computer simulations to replicate the package and the conditions it would experience in an accelerated lifetime test. All three experiments mentioned can be duplicated using software like ANSYS.

There are advantages and disadvantages to both mechanisms. Starting with the experimental accelerated lifetime tests, the main advantages are the experimental outcomes, while the primary disadvantage is the cost of achieving those outcomes. When a package fails after experimental testing, the two crucial pieces of information are the number of thermal cycles the package withstood before failure, and the mechanism of failure. If a statistically sizable number of packages are evaluated, the reliable lifetime of the design can be predicted along with the probable failure mechanism. These conclusions are necessary in any complete reliability evaluation and allow for future redesigns based on first principles. However, the disadvantages are in the time and resource cost of achieving statistically meaningful conclusions, especially across multiple designs. For statistically valid results of even a single design, multiple samples must be evaluated. For groups without dedicated packaging engineers and equipment, the time and resource cost of creating a single package are meaningful and grows with package complexity or sample number. Because of increasing complexity, it is difficult to predict the outcome of a redesign. While a single experiment establishes the validity of one design, an additional experiment is needed for each redesign.

Regarding simulations, the main advantages are the reduced resource cost and the ability to compare redesigns using engineering mechanics. While experimental work requires building samples and subjecting them to potentially thousands of cycles, simulation work requires a CAD model and a simulation program. Simulations allow you to explore how the package reacts to stimuli in terms of stress, strain, and energy, which is not possible in experimental work. While there are back-of-the-envelope calculations for estimating the shear force on bonds in [23], the bonds are exposed to complex multi-axial stress states that cannot be replicated by hand. The quantitative values gained, such as the inelastic strain or energy, allow for faster redesigns than what is possible doing only experimental work. The major limitations of simulations are that they should be validated with experiments, and that they cannot conclusively establish failure mechanisms or cycles to failure like experimental work. A simulation approximates reality, requiring assumptions about the package failure mechanism and the behavior of the system. Therefore, a conclusive study must have the critical regions identified by simulations be validated by experimental failure locations. Another limitation is that while simulations can identify regions of high fatigue, they cannot determine how the fatigue results in failure. Therefore, simulations are most effective as a tool that assists and expands upon experimental work by explaining failure mechanisms and enabling faster redesigns.

The ideal thermal fatigue study uses both experimental and simulation methods. The advantage of doing both is the possibility of generating an empirical equation that predicts cycles to failure based on simulation metrics. For example, Darveaux's model correlates the volume averaged inelastic work density per thermal cycle (ΔW_{avg}) in a bond to the thermal cycles needed to both initiate and then propagate a crack through the bond [25]. However, as this requires both simulation and experimental work, it requires the most time and resources to complete.

This thesis will focus on using temperature cycle simulations to investigate the fatigue generated in the package bonds, with future work being the experimental temperature cycling to verify the results and collect the cycle to failure data. The reason for performing temperature cycling instead of another method is to simplify the initial analysis. If greater complexity is desired, that can be accomplished with future work. The reason for using simulations over

experimental testing is due to the lower barrier to entry and resource cost of simulation work versus packaging and experimental temperature cycling.

1.6 Using Encapsulation Materials to Lower Bond Fatigue

The purpose of this section is to show the common encapsulants used in power module packaging, and how proper selection reduces the thermo-mechanical fatigue on the most vulnerable bonds. Rigid encapsulants, which are commonly epoxy polymers, have both a comparatively low CTE and high *E*. If the epoxy CTE has minimal mismatch with the package, then it reduces bond fatigue. Soft encapsulants, typically silicone gels, have comparatively high CTE and low *E*. Their low *E* results in them having minimal impact on bond fatigue. The specific encapsulants studied in this thesis, ME-531 and EP-2000, are chosen because they are predicted to reduce fatigue and are utilized by our research group. However, EP-3500 epoxy and the Resbond 920 cement are appealing choices for future study. For a comprehensive analysis, [26] and [27] are recommended for further reading on both the current state of polymeric encapsulants and the push for other encapsulation materials.

In electronics packaging, polymeric encapsulants are used to provide electrical insulation, protection against mechanical loading from both external loading and provide an inert environment that protects against environmental hazards like gases, radiation, and moisture [27]. There is a myriad of factors that should be considered when choosing an encapsulant, such if the encapsulant processing will damage any other package component, adhesion to package materials, the component voltage, and the expected temperature and chemical environment the package is placed in. However, this work is not intended to be comprehensive guide for choosing an encapsulant, it only focuses on the thermo-mechanical consequences of using certain encapsulants. The minimum material properties to model temperature independent encapsulant are CTE, Elastic Modulus (E), Poisson's Ratio (ν), which are explained in Section 2.5. Therefore, the following discussions will focus primarily on the CTE and *E* of the encapsulants and how they can be used for the PCB-Interposer-on-DBC. A more in-depth discussion of how encapsulant CTE and *E* relate to bond fatigue is in Sections 3.2 and 4.2.

The concept of using encapsulant to increase the lifetime of flip chip solder bonds is demonstrated in [28], which showed that using a silica-filled resin with CTE like the solder drastically improved the solder lifetime by redistributing stresses from the peripheral solder

joints to the rest of the package [29]. This solution allowed flip chip packages to be mounted on organic substrates instead of the previously used ceramic or silicon substrates. While more expensive, the CTE mismatch between the silicon dies and ceramic was lower than with the organic substrates, lowering the shear stress placed on the peripheral solder joints. Further work like [30], [31], [32], and [33] continued to build upon this work, studying different encapsulants, the effects of cure temperature and moisture, and how the encapsulant altered the strain placed on the bonds in simulation models. While this concept of fatigue reduction applies to other packages, the body of work dedicated to flip chip solder bond reliability is well established.

Encapsulants are primarily polymers, which can be generally lumped into two categories [26], [27]. The first is rigid encapsulants, which may be called underfills if they encapsulate only the bonds, or molding compounds if they encapsulate an entire package. These are the materials used in flip chip packaging to reduce and redistribute thermo-mechanical loads caused by the CTE mismatch. These materials have a CTE $\leq$ 30 ppm/°C to minimize the CTE mismatch, and an $E >$ 1 GPa to have the necessary stiffness to influence the package. If the CTE exceeds this limit, the encapsulant becomes more likely to increase the thermo-mechanical stress instead of countering it. Epoxies with ceramic fillers are common commercial rigid encapsulants, with biopolymer and cyanate ester variants being explored in literature.

The second category are soft encapsulants, which are used as potting materials and glob tops. These materials provide an inert environment and electrical isolation but have a significant CTE mismatch with all package components. However, their low E prevents the encapsulant from contributing to bond fatigue. Therefore, while soft encapsulants are unable to reduce bond fatigue relative to a scenario where no encapsulation is used, they also cannot increase bond fatigue relative to that scenario.

Generally, a package made of materials with similar CTE and E will warp more uniformly and have lower bond fatigue relative to a package with significant mismatch. The addition of an encapsulant with a well-matched CTE and requisite E pins the mismatched structure together, forcing it to warp more uniformly. The CTE of epoxy resins can mimic that of metals and composites used in packaging, with higher elastic moduli than those available to the original

researchers studying BGA bond reliability. While reaching even lower CTEs and higher *E* should better match the packaging materials, polymers are currently limited to CTEs ≥ 10 ppm/°C and E ≤ 20 GPa. While generating new polymers that breach these limits is not impossible, another option is to replace polymer encapsulants with other materials that meet these requirements. Options being investigated are glasses and cement.

Table 1-6 contains material properties for commercial and academic encapsulants. While there are many encapsulants, most do not list the mechanical properties required to perform these simulations. As such, one option for future work is identifying the temperature dependent CTE and *E* for future simulations.

Chapter 3 focuses on the effects of using ME-531 and EP-2000 epoxies, which the encapsulant property sweeps also model using silicone gel. These three materials are modeled because they are previously tested encapsulant choices available for the future experimental temperature cycling. However, with the results of Chapter 4 identifying an 8 ppm/°C encapsulant as optimal for protecting the Internal Gate bond, EP-3500 is the most optimal polymer encapsulant choice listed. However, as this group has not worked with EP-3500 before and [34] is the only documented case of it being used, implementing EP-3500 requires both shear strength and processing tests to confirm that it is a viable encapsulant. Therefore, future work must decide if it should be also included.

The other materials are not evaluated for three main reasons. The first reason is that their CTE mismatch is expected to render them a sub-optimal choice for reducing bond fatigue relative to ME-531 and EP-2000, which disqualifies options like SolEpoxy and Durapot. The second reason is that they are not commercially available, which disqualifies the EMC encapsulant. The final reason is that the encapsulant is either incompatible with or needs significant study before using with the PCB-Interposer package. The lead glass must be poured into the package at 500 °C, which is incompatible with the maximum possible glass transition temperature of the PCB (180 °C). The low CTE of the Resbond 920 cement is appealing but has a considerable number of unknowns. While the true tensile strength of this cement is unknown, ANSYS Granta lists an aggregate tensile strength of calcium oxide cements of 2.1 MPa, which is an order of magnitude

lower than the principal stresses experienced by the encapsulant in this design. It also lacks the necessary material data for simulations, and its adhesion and interactions with other packaging materials is uncertain. As cement is a promising replacement for polymers in high-temperature packaging, more study is expected, so it may be revisited when more is known.

Table 1-6. List of Both Commercial and Literature Encapsulants. The Storage Modulus is Approximated as the Elastic Modulus if Only it is Available. The Maximum Temperature is the Glass Transition Temperature for Epoxies.

Encapsulant	Material	Product that is sold?	Linear CTE (ppm/°C)	Elastic Modulus (GPa)	Maximum Temperature (°C)	Source
TSE3062	Silicone	Yes	1000	Unlisted	200	[35]
SilGel 612	Silicone	Yes	300	0.01	180	[36]
DOWSIL CN-6015	Silicone	Yes	108	Unlisted	200	[37]
Vanillin Resin	Benzo-polymer	No	60.9	3.89	400	[38]
Lead Glass	Glass	Yes	10.3	Unlisted	322	[39]
Resbond 920	Cement	Yes	8.1	Unlisted	1650	[40], [41]
Rigid-Rod Epoxy	Epoxy with Cyanate ester	No	73.8	2.5	253	[42]
EMC	Epoxy with Cyanate ester	No	14.39	15.5	240	[43]
Durapot 865	Epoxy	Yes	68	Unlisted	260	[44]
SolEpoxy MH20-01	Epoxy	Yes	32	4.8	145	[45]
ER2220	Epoxy	Yes	30	Unlisted	130	[46]
Silica Epoxy Blend	Epoxy	No	22.79	Unlisted	185	[47]
ME-531	Epoxy	Yes	21	6	140	[48]
EP-2000	Epoxy	Yes	14.9	17.5	204	[49]
EP-3500	Epoxy	Yes	10.4	20	206	[50]

1.7 Summary of Thesis

Chapter 2 provides the necessary information to evaluate simulation quality along with a guide for performing thermo-mechanical simulations inside of ANSYS Workbench. For simulation evaluation, the boundary conditions and mesh quality are described. The bond groups, which identify what bonds can be compared using ΔW_{avg}, are also discussed.

Chapter 3 establishes which bonds in the package are likely locations of first failure, and uses parameter sweeps to establish what the relationship between the encapsulant properties and ΔW_{avg} is for that first failure locations. The Internal Gate bond is the sintered Ag bond expected to fail before all other sintered Ag bonds, which include the internal pin bonds and the die attach. The External Source 4 solder is the solder bond expected to fail first. As the Internal Gate bond is subjected to a greater magnitude of per-cycle fatigue versus the External Source 4, and the loss of the Internal Gate bond means complete package failure, further analysis will focus on the Internal Gate bond.

Chapter 4 looks at how four available encapsulant choices interact with the Internal Gate bond. The possibilities of soft and rigid encapsulant are studied, with EP-2000 being the best available encapsulant for the PCB-Interposer package. A material with a lower CTE and higher E versus EP-2000 would further reducing Internal Gate ΔW_{avg}, setting up guidelines for what encapsulants should replace EP-2000. It also establishes that the E of silicone encapsulants is too low to meaningfully interact with the package, with an outcome like the No Encapsulant scenario.

Chapter 5 summarizes the results of the previous chapters and addresses future work.

Chapter 2. Performing Temperature Cycle Simulations in ANSYS Workbench 2021 R2

2.1 Purpose of Chapter 2

The purpose of describing the setup required to run a thermo-mechanical simulation is two-fold. The first reason is that it provides others with the means to evaluate the assumptions made and result quality. For simulations, evaluation tools include mesh convergence studies and descriptions of boundary conditions used. The second reason is a lack of comprehensive guides for completing such work within literature. While a surmountable barrier, it can be lowered with guidance.

Section 2.2 is the guide for creating a thermo-mechanical simulation using ANSYS Workbench. It is a step-by-step guide that describes all relevant components and settings, as well as the dimensions of the PCB-Interposer package. While the guide is not universally applicable, the author hopes that this explanation allows others to make educated decisions on whether to replicate these steps.

Section 2.3 describes the boundary conditions used for all chapters in this work. The two groups are the mechanical boundary conditions that restrict undesired motion, and the thermal condition that applies thermal cycling to the package.

Section 2.4 describes the mesh quality on the bonds expected to fail first based on this analysis. Both convergence studies and mesh skewness are reported for each bond.

Section 2.5 describes the engineering mechanics models used to represent the materials. This analysis uses the common assumption that inelastic deformation in all non-bond structures is negligible, while the Anand Constitutive Model is used for the Sn60Pb40 and sintered silver bonds.

Section 2.6 describes the quantitative metric of fatigue used in the simulations; volume averaged inelastic strain energy density (ΔW_{avg}). Both the means of calculating it within ANSYS and the stipulations in using it as a relative metric of fatigue between bonds are discussed.

Section 2.7 describes the bond groups that arise from the stipulations of using ΔW_{avg} to compare the fatigue on different bonds. The ΔW_{avg} of entities within a bond group can be compared, and the entity with the largest value is expected to fail first out of all entities within the group. This bond or region is denoted as the first failure bond of the group.

2.2 Setting Up a Temperature Cycle Simulation in ANSYS Mechanical

2.2.1 The CAD Model and Importing it into ANSYS Mechanical

This section will explain the CAD model utilized in the simulation, as well as best practices for making such a model and implementing it into ANSYS Workbench.

The CAD model was built in SOLIDWORKS 2021 and imported into Workbench, with all symmetry cutting done in ANSYS DesignModeler. Importing a SOLIDWORKS file in ANSYS SpaceClaim is not recommended due to various body errors that occur.

Regarding the CAD model itself, it is a recreation of the original PCB-Interposer-on-DBC design shown in [18] and [19]. As no measurements of the original design were available, PCB and DBC geometries were estimated using leftover components. The conclusions of this work are not expected to change based on minor geometrical discrepancies, a useful lesson to learn for those starting simulation work.

Table 2-1 is a list of the components, geometries, and materials used for the package. Fig. 2-1 shows the geometry of the package, while Fig. 2-2 shows the bond geometry. Regarding Fig. 2-1, the package is a half model, which means that only half of the full model is generated to reduce the computation cost. This is acceptable, provided that the proper boundary conditions are implemented.

There are two more relevant lessons regarding CAD design. The first lesson, like the lesson of slight geometrical differences, in that the addition of minor details like pin coatings or die passivation layers do not change the results but increase the work required. Thin layers require fine meshes to properly model, which increases the time and memory required to run a simulation. While the decision of what structures to remove is case-dependent, there are guidelines. If a single component is comprised of multiple material layers, it is reasonable to remove layers that are at least an order of magnitude smaller than larger ones. For example, a GaN-on-Si die may be comprised of a 0.23 mm Si substrate, a 0.005 mm GaN/AlGaN layer, a 0.02 mm SiN passivation layer, an 0.005 mm polyimide layer, and 0.008 mm Cu pads. As the Si

substrate comprises most of the body's volume, it is reasonable to approximate this die using either the Si layer alone or both the Si and SiN layer. These thinner layers lack the necessary volume to influence the structure but require additional computational resources to properly model.

The second lesson is to remove sharp corners and edges in crucial regions like bonds. The sharp edges and corners can generate stress singularities, which is a point in the mesh where the stress is both unusually high and does not converge upon further mesh refinement. The simplest way to prevent this is to ensure that all critical and neighboring bodies in the model have rounded edges and points. This will convert the stress singularity into a stress concentration point, which is expected even at rounded edges.

Table 2-1. Components, figure symbol, dimensions, and material for all components in the simulation.

Component	Symbol	Dimensions (mm)	Material
Solder	A	D_1 = 1.2, D_2 = 0.76, H = 0.17	Sn60Pb40
4184-0-00-15-00-00-33-0 Pins	B	D_1 = 0.01, D_2 = 0.03, H_1 = 0.07, H_2 = 0.01	Gold-plated Nickel
PCB	C	6.8 x 6.7 x 1.18	FR4
Encapsulant	D	Fills space between die and PCB	Varies, see Chapters 3 & 4
Sintered Silver Bond Material	E	Die Attach: 6.325 x 5.6 x 0.03 Pin Joints: D_1 = 0.35, D_2 = 0.253, H_1 = 0.03, H_2 = 0.013	Nano-silver paste
GaN Systems GS-065-150-1-D2 Die	F	6.3 x 5.6 x 0.246	Si substrate, with SiN and Cu RDL
AlN DBC Substrate	G	AlN: 6.9 x 6.7 x 0.3 Cu: 6.52 x 5.94 x 0.3	AlN between Cu plates

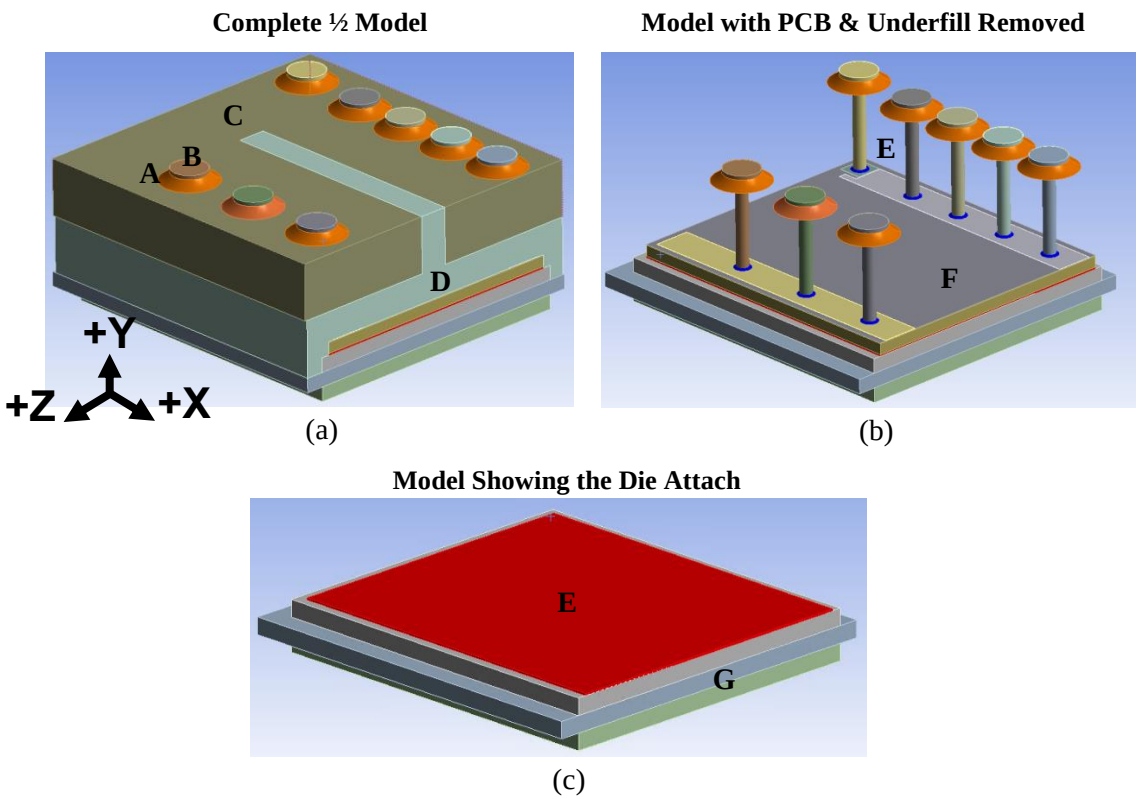


Fig. 2-1. The PCB-Interposer-on-DBC CAD model, using Table 2-1 letter designations. (a) The complete package. The eight External bonds are colored orange and are made of Sn60Pb40. (b) The package with the top section removed to show the die and base of the pins. The eight Internal bonds are blue and are made of sintered Ag. (c) The package with the die removed to show the die attach and DBC substrate. The die attach is red and is made of sintered Ag.

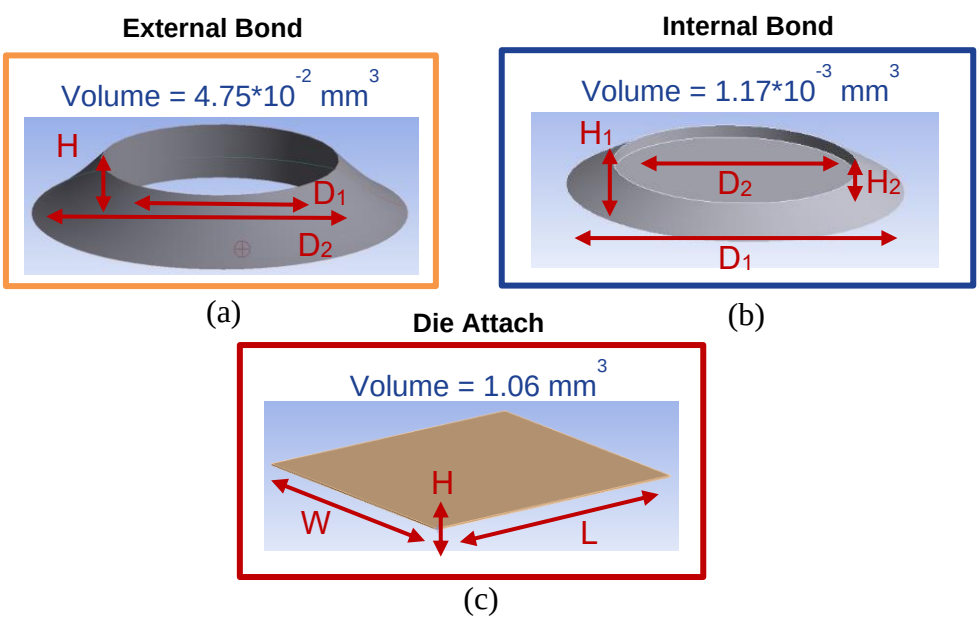


Fig. 2-2. The bonds and dimensions used. (a) The External bond that connects the pin to the PCB. (b) The Internal bond that connects the pin to the die. (c) The Die Attach that connects the die to the DBC.

2.2.2 Setting up A Temperature Cycling Simulation

This section details the procedure for creating a temperature cycling simulation. This is intended as a summary to give inexperienced users the tools and language to begin simulation work, along with identifying crucial settings that alter the results. This will not replace more detailed guides, like the ANSYS Static Structural Analysis guide located in ANSYS Help documentation [51]. This guide assumes the user is working in ANSYS Workbench 2021 R2, which is the multi-physics platform that hosts ANSYS Mechanical.

The first assumption made is that all inertia and damping effects on the structure are not significant. This means Essentially, changes to the boundary conditions occur so slowly that the effects of overcoming inertia and the resulting vibrations do not need to be considered [52]. Therefore, this analysis is treated as a Static Structural simulation, which simplifies the analysis. While there is no definitive cutoff between what qualifies as a Static or Transient Structural simulation, loads that significantly vary over a timeframe measured in seconds (Thermal Shock) would be a Transient situation, while timeframes measured in minutes can be treated as a Static situation. If the answer is still unclear, then start with a Transient simulation. Fig. 2-3 displays the Static Structural Analysis System inside of ANSYS Workbench.

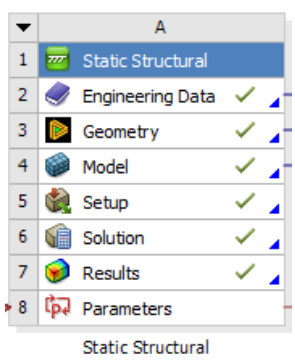


Fig. 2-3. The Static Structural Analysis System.

Once the system is placed into the Project Schematic, the procedure follows the order of topics listed in Fig. 2-3. Engineering Data is the materials library that contains the material properties.. Geometry opens ANSYS CAD software where you can build or alter your imported CAD model.

Model through Results opens up ANSYS Mechanical, while Parameters allows alteration of model inputs and viewing of designated outputs.

Fig. 2-4 is the Engineering Data menu. The actual materials are separated into different libraries, which can be selected for further viewing. To generate new material, first create or edit an existing library, then select the relevant material properties from the left-hand menu. If a simulation is missing required material properties, ANSYS will identify the missing properties in an error message and abort the simulation.

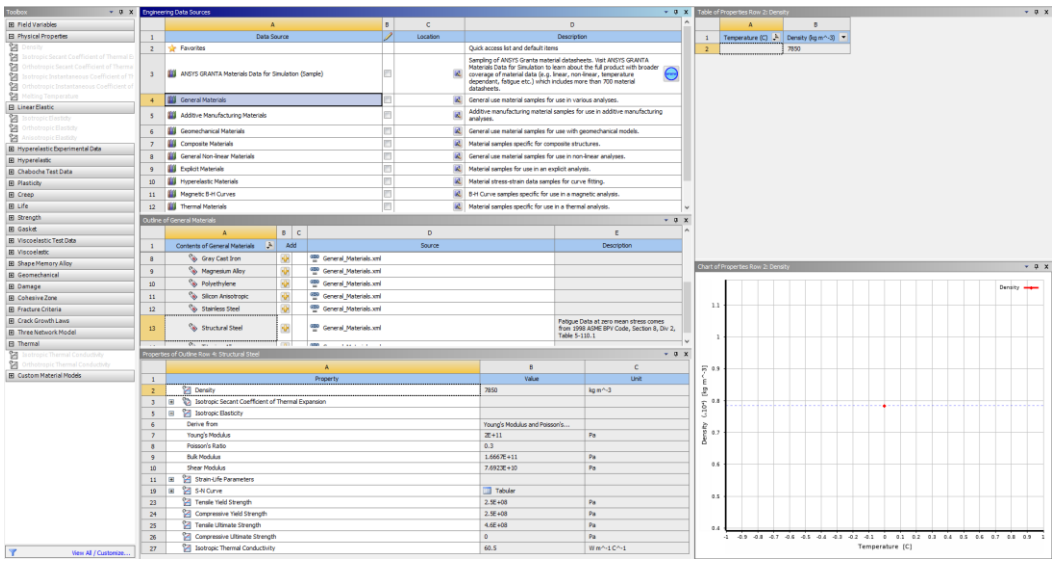


Fig. 2-4. The Engineering Data menu. From left to right, a drop-down menu that allows you to define specific material properties, a list of the libraries with their contents and respective material properties, and both table and graphical representation of how the material properties vary with respect to temperature.

Fig. 2-5 shows DesignModeler, one of the two CAD software usable in the Geometry tab. If you import a full structure into Workbench, the Slice and Symmetry commands in this program can turn the full model into a half or quarter symmetrical model.

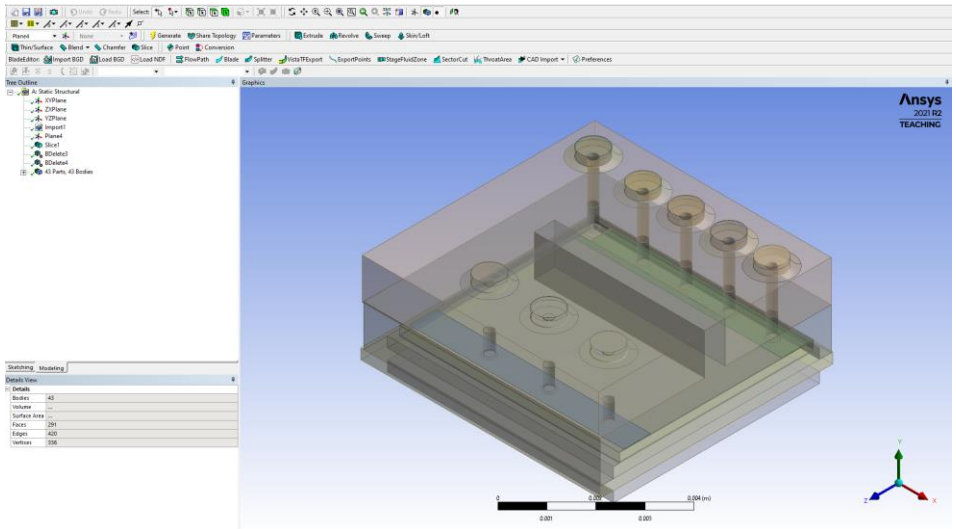
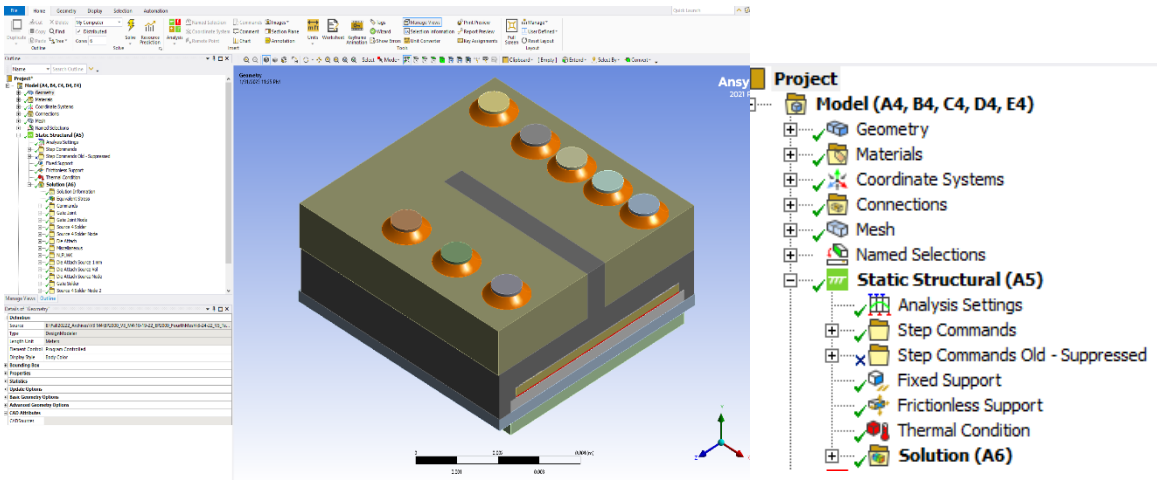


Fig. 2-5. ANSYS DesignModeler CAD software. If the model is imported, the Symmetry Tool allows for cutting the body into half models while automatically applying the Frictionless Support boundary condition to the cut plane.

The simulation is run using ANSYS Mechanical, shown in Fig. 2-6. For setting up the simulation, the relevant menus are the Outline tree and the Details table. The Outline tree is where the user adds simulation inputs and outputs, while Details edits those inputs and outputs. The following paragraphs walk through each Outline topic in Fig. 2-6(b).



(a) (b)

Fig. 2-6. The main interface for ANSYS Mechanical. (a) For this guide, the most important menus are the Outline (left) and Details (bottom left). (b) This guide walks through each topic shown in the Outline.

The first topic is Geometry, which determines the behavior applied to a given body. To simplify this and future Connection checking, it is recommended that each body receives a

unique name. Fig. 2-7 displays the settings for Geometry. The relevant settings for thermal fatigue are the “Stiffness Behavior” and all settings under “Material”. For the body to deform, “Stiffness Behavior” must be set to “Flexible”. For settings under “Material”, you must manually assign the body’s material and turn on both non-linear effects and thermal strain. If your body lacks the material properties required to implement non-linear (inelastic) effects, then this setting will have no impact. Selecting the check box converts that input into a parameter, which can then only be altered from the Workbench Parameter menu. Returning to Fig. 2-6(b), “Materials” are defined in Engineering Data and “Coordinate Systems” does not need altering.

Graphics Properties	
Visible	Yes
Transparency	1
Color	
Definition	
Suppressed	No
Stiffness Behavior	Flexible
Coordinate System	Default Coordinate System
Reference Temperature	By Environment
Treatment	None
Material	
P Assignment	FR4
Nonlinear Effects	Yes
Thermal Strain Effects	Yes
Bounding Box	
Length X	6.816e-003 m
Length Y	1.18e-003 m
Length Z	6.701e-003 m
Properties	
Volume	4.9925e-008 m^3
Mass	9.4857e-005 kg
Centroid X	4.1011e-003 m
Centroid Y	1.4545e-003 m
Centroid Z	9.0641e-003 m
Moment of Inertia ...	3.8912e-010 $kg{\cdot}m^2$
Moment of Inertia ...	7.5177e-010 $kg{\cdot}m^2$
Moment of Inertia ...	3.8466e-010 $kg{\cdot}m^2$
Statistics	
Nodes	11008
Elements	2092
Mesh Metric	None

Fig. 2-7. Details table for Geometry.

The next topic is “Connections”, which uses the proximity of two bodies to define whether they are in physical contact. It is recommended to make a list of all the bodies in the model to manually check each listed connection. Previously naming the bodies reduces the potential for human error during checking. Even if Mechanical correctly acknowledges contact between two bodies, the exact contact faces may be incorrect and thus require manual correction. The correction can be done in the graphic interface shown in Fig. 2-8. To disable but not delete undesired contacts, you may suppress the contact and place it in a separate subfolder.

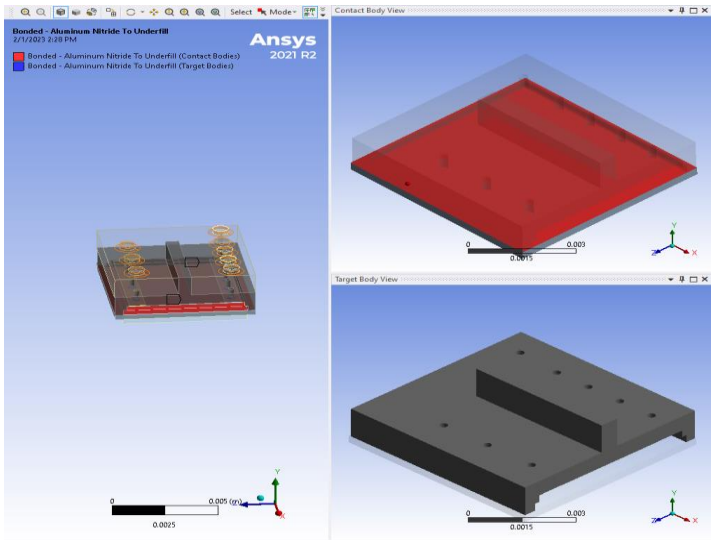
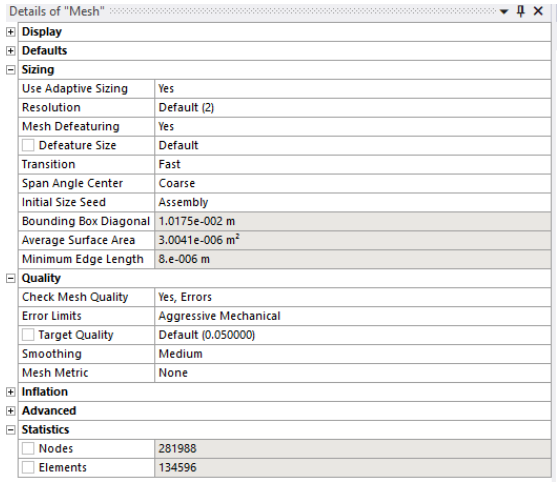


Fig. 2-8. The main graphical interface and the contact/target body interface. Contact faces are brightly colored to make verification easier.

"Mesh" is the most difficult of Outline topics, as it is an iterative process requiring manual input. It is recommended to read ANSYS documentation and other sources on meshing due to its complexity. The primary goal when meshing is to use the least dense mesh whose results cannot be meaningfully altered by increasing the mesh density. This convergence maximizes accuracy for the minimum necessary computational cost. The minimum mesh density needed on each body depends on the body's role. For a body that is not a bond or connected to one, a lower quality mesh achieved through global settings is acceptable. For bodies connected to bonds, their mesh density should increase in the regions contacting the bonds, which requires manual input. For the bonds themselves, their mesh density should be high enough to reach result convergence. This guide focuses on how to alter the mesh, with mesh quality metrics discussed in Section 2.4.

Fig. 2-9 shows the global and general mesh settings most applicable to a first-time user. To alter the global mesh applied to all bodies, increase the value of "Resolution". To view mesh quality metrics, switch "Mesh Metric" to the desired metric. The total number of elements and nodes is in "Statistics", while the numbers for a single body are in Geometry, which can be seen in the bottom of Fig. 2-7.



Details of "Mesh"	
Display	
Defaults	
Sizing	
Use Adaptive Sizing	Yes
Resolution	Default (2)
Mesh Defeaturing	Yes
Defeature Size	Default
Transition	Fast
Span Angle Center	Coarse
Initial Size Seed	Assembly
Bounding Box Diagonal	1.0175e-002 m
Average Surface Area	3.0041e-006 m²
Minimum Edge Length	8.e-006 m
Quality	
Check Mesh Quality	Yes, Errors
Error Limits	Aggressive Mechanical
Target Quality	Default (0.050000)
Smoothing	Medium
Mesh Metric	None
Inflation	
Advanced	
Statistics	
Nodes	281988
Elements	134596

Fig. 2-9. Part of the Mesh Details menu.

The three basic tools for manually altering the global mesh are Sizing, Refinement, and Contact Sizing. Sizing is used to define either the element size in a body, the number of elements along an edge, or the element size within a specified sphere of influence. Refinement reduces the size of elements on faces, edges, and vertices. Contact sizing is useful for the bodies in contact with bonds, as it increases mesh density in and around the faces defined as contact surfaces in the connections.

The final general Outline topic is “Named Selection”. A named selection is a set of geometrical or mesh entities that are grouped together for convenient reference elsewhere. To reference all External bonds, one could create a named selection containing all External bonds and then scope to the named selection instead of manually selecting all External bonds every time.

Moving to the Outline topics under “Static Structural (A5)” in Fig. 2-6(b), the first important setting is in the “Static Structural” Details menu, shown in Fig. 2-10. The Environment Temperature is the designated “stress-free” temperature, at which the entire structure experiences no thermal strain. Deviations from this temperature cause thermal strain. The assumption made in this section is that the stress-free temperature is 25 °C to simplify the analysis. For improved accuracy, the reference temperature is often the encapsulant curing temperature, as the subsequent cooling causes the encapsulant to compress, generating internal stresses and loads on nearby materials.

Definition	
Physics Type	Structural
Analysis Type	Static Structural
Solver Target	Mechanical APDL
Options	
Environment Temperature	25. °C
Generate Input Only	No

Fig. 2-10. The Details menu for Static Structural.

Fig. 2-11 shows the relevant settings in “Analysis Settings”. In “Step Controls”, you define the number of simulation steps and the time that each step ends at. In “Solver Controls”, Large Deflection should be turned on. This non-linear setting alters the stiffness of a body depending on its deformation and should be turned on unless a comparative study shows it is unnecessary. For “Restart Controls”, the shown settings will generate a restart file after every load step. This allows for simulation restarts in the event of failures that can be fixed by altering the sub-step number. “Non-linear Controls” should all be program-controlled, and “Output Controls” determines what information is saved after a simulation. Failing to save the proper data will cause the output codes to fail. The author recommends saving all data for post processing.

Step Controls	
Number Of Steps	19.
Current Step Number	19.
Step End Time	21900 s
Auto Time Stepping	Program Controlled
Solver Controls	
Solver Type	Program Controlled
Weak Springs	Off
Solver Pivot Checking	Program Controlled
Large Deflection	On
Inertia Relief	Off
Quasi-Static Solution	Off
Rotordynamics Controls	
Restart Controls	
Generate Restart Points	Manual
Load Step	All
Substep	Last
Retain Files After Full Solve	No
Combine Restart Files	Program Controlled
Nonlinear Controls	
Advanced	
Output Controls	
Stress	Yes
Surface Stress	Yes
Back Stress	Yes
Strain	Yes
Contact Data	Yes
Nonlinear Data	Yes
Nodal Forces	Yes
Volume and Energy	Yes
Euler Angles	Yes
General Miscellaneous	Yes
Contact Miscellaneous	Yes
Store Results At	All Time Points
Result File Compression	Program Controlled
Analysis Data Management	
Visibility	

Fig. 2-11. The Details menu for Analysis Settings.

“Step Commands” are custom commands utilizing Ansys Parametric Design Language (APDL) to define the simulation settings for each step. These settings include the number of attempted solutions, the type of solver used, the sub-steps used per step, and the convergence criteria. The Details menu is used to select which step the code is applied to. The input APDL code is in Appendix B.

File	
File Name	C:\Users\carl176\Documents\A6\NoUnderfill\ANSYSWorkbench\Code\Pre...
File Status	File not found
Definition	
Suppressed	No
Step Selection Mode	By Number
Step Number	5.
Target	Mechanical APDL
Issue Solve Command	Yes
Input Arguments	
ARG1	
ARG2	
ARG3	
ARG4	
ARG5	
ARG6	
ARG7	
ARG8	
ARG9	

Fig. 2-12. The Detail menu for the input APDL command.

The “Fixed Support” and “Frictionless Support” topics are boundary conditions that prevent the body from translating, rotating, or moving into space that would be occupied by the missing model half. Fixed supports lock the specified node in place and using at least two prevents the whole body from translating or rotating. Frictionless supports are used with symmetry models to prevent the model from moving into space occupied by the missing segment. “Thermal Condition” is the boundary condition that applies thermal cycling by raising and lowering the temperature of the entire package. These specific boundary conditions are discussed in Section 2.3. These are the input conditions that subject the package to a load and restrict it to only deforming in 3D space.

Regarding outputs, the relevant topics are the “Solution Information” and the APDL output code that calculates ΔW_{avg}. “Solution Information” is a text file that contains the results of every sub step in the simulation, along with the input and output APDL codes. It is useful for debugging failed simulations and collecting values calculated by the codes but that are not among the outputs.. It can be accessed from the “Scratch” folder that Workbench generates

during solving to study the solution progress. Like the input code, the output code is imported into an output "Commands" topic to solve for ΔW_{avg}. To simultaneously view and export all ΔW_{avg} values, it is recommended that you parameterize the output as shown in Fig. 2-13. The output code is in Appendix B.

File	
File Name	C:\Users\carl176\Documents\A6\8-24-22_V3_NoUnd...
File Status	File not found
Definition	
Suppressed	No
Output Search Prefix	my_
Invalidate Solution	No
Target	Mechanical APDL
Input Arguments	
ARG1	
ARG2	
ARG3	
ARG4	
ARG5	
ARG6	
ARG7	
ARG8	
ARG9	
Results	
P my_SED_FINAL_DIEATTACH1MMSOURCE	1.0534e+005

Fig. 2-13. The Details menu of the APDL output code.

2.3 Boundary Conditions

The purpose of this section is to describe the two mechanical and one thermal boundary condition used in this simulation. The three fixed nodes at the bottom center of the package prevent package translation and rotation, but not prevent warpage. The frictionless support on the cut plane acknowledges that the unmodeled half of the package does exist and prevents the modeled half from expanding into that space. The temperature cycling is applied using a Thermal Condition, which uniformly raises and lowers the temperature of all bodies.

Boundary conditions provide the loads and constraints that are required to generate a solution. Improper conditions or their application results in unexpected behavior that degrades simulation quality. It is recommended to study the consequences of a boundary condition before full implementation, like with a test run.

The first boundary condition is the fixed support applied to the three nodes in the bottom center of the package, as shown in Fig. 2-14. A fixed node cannot move from that location in the global coordinate system, so a single fixed node in a model with all contacts defined as “bonded” (no slipping or separation) means the package cannot translate in space. However, the model can rotate about the single fixed node, so fixing at least one more node is required to prevent rotation about any fixed node. Regarding the choice of nodes in the package center, a material experiencing thermal strain will grow or shrink relative to the body’s center. Therefore, the thermal strain and resulting warpage are not expected to occur in the chosen node location.

The second boundary condition is the frictionless support applied to the center or “cut plane” of the package, which is shown in Fig. 2-15. Part of simulation work is identifying acceptable tradeoffs between computational cost and accuracy. If you are modeling a symmetric structure, only modeling the smallest repeatable unit with the proper boundary conditions has minimal impact on the results while lowering simulation run times and file sizes. However, when modeling only half of the structure, it cannot be allowed to deform into the space where the missing half would occupy. To prevent this, a frictionless support is applied to all faces on the cut plane, which prevents that face from deforming in a direction normal to the face. This

boundary condition is automatically applied if the “Symmetry” tool in DesignModeler is used to remove the undesired sections.

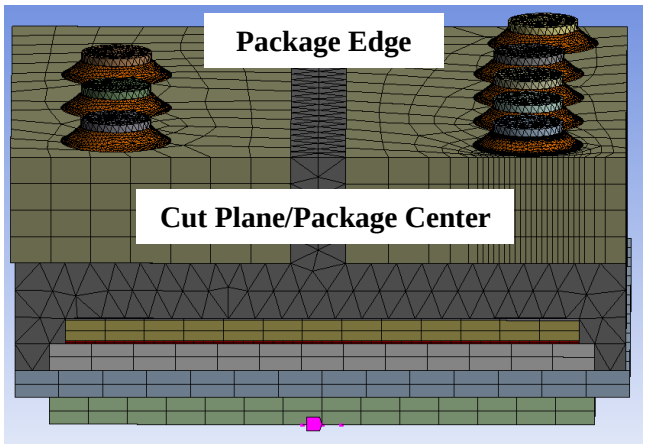


Fig. 2-14. The three pink nodes with the fixed support boundary condition.

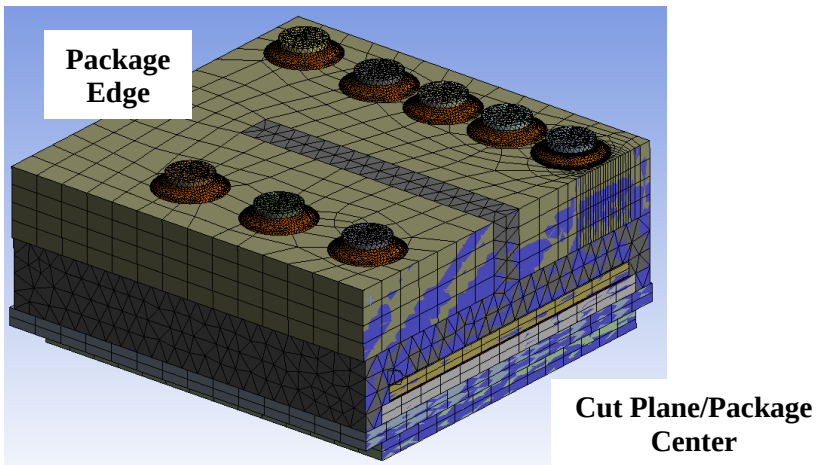
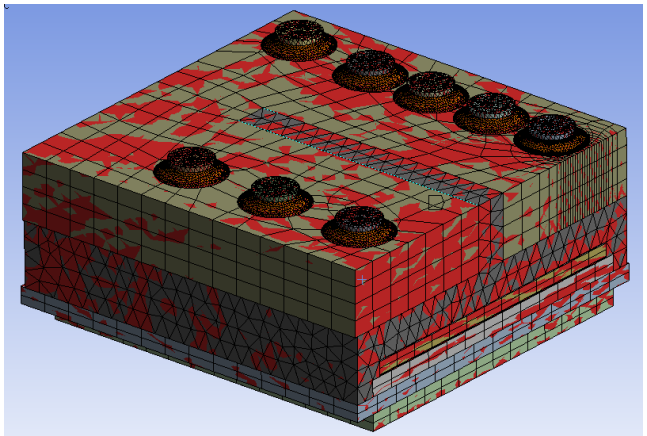


Fig. 2-15. The purple shaded cut plane with the frictionless support boundary condition.

The final boundary condition is the Thermal Condition, which applies the thermal cycling to the package. The Thermal Condition defines the temperature of a body and how it changes over time. In this work, the Thermal Condition controls the temperature of all bodies, so the package temperature remains uniform throughout cycling. The uniform temperature simplification is used because modeling the thermal transients increases computational costs without meaningfully altering the results. The ramp and dwell parameters are taken from JEDEC standards on solder joint fatigue, which are designed to avoid thermal gradients greater than several degrees within the sample [24]. The maximum suggested ramp rate is 15 °C/min, while the simulation ramp rate

is 5 °C/minute. In combination with the package's simulated thermal resistance of 0.14 °C/W, thermal transients are considered negligible and are removed from the analysis. However, for power cycling or thermal shock simulations, this assumption should be re-evaluated. Fig. 2-16 shows the thermal boundary condition and the tabular data, while Table 2-3 summarizes the thermal cycle parameters used.



Steps	Time [s]	✔ Temperature [°C]
1	0.	25.
1	1.	25.
2	60.	25.
3	1260.	125.
4	1860.	125.
5	3840.	-40.
6	4440.	-40.
7	6420.	125.
8	7020.	125.
9	9000.	-40.
10	9600.	-40.
11	11580	125.
12	12180	125.
13	14160	-40.
14	14760	-40.
15	16740	125.
16	17340	125.
17	19320	-40.
18	19920	-40.
19	21900	125.

(a) (b)

Fig. 2-16. All bodies in (a) follow the ramp and dwell temperature profile in (b).

Table 2-2. The Thermal Cycle Parameters in Accordance with JEDEC standards [24].

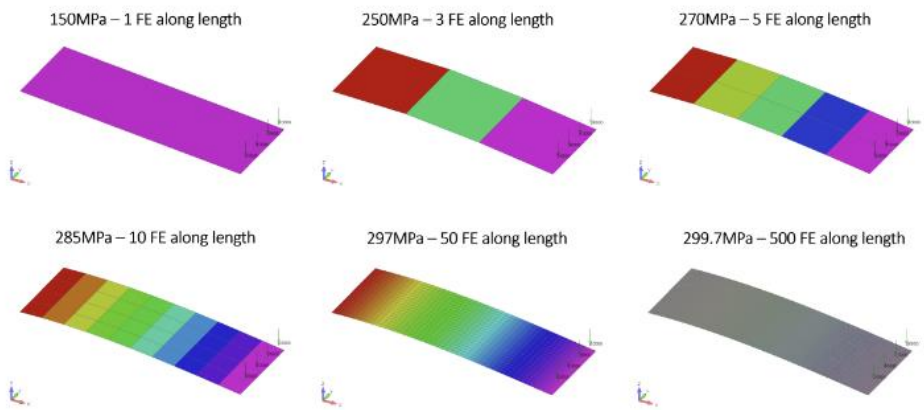
Parameter	Value
Range	-40 °C to 125 °C
Ramp Rate	5 °C/minute
Dwell Time	10 minutes
Cycles to Convergence	4 Cycles
Stress-Free Temperature	25 °C

2.4 Mesh Quality

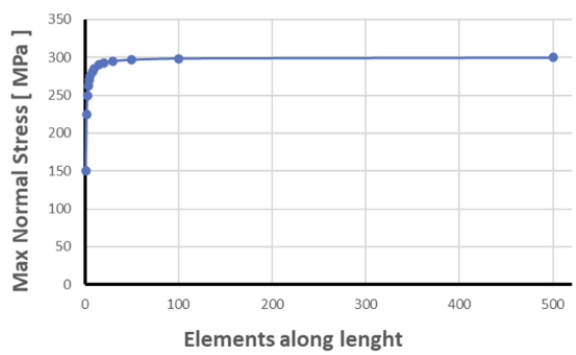
The purpose of this section is to establish the importance of mesh convergence and to show the mesh used has converged. The mesh discretizes the 3D model into a network of interconnected nodes that can solve the relevant equations to calculate stress and strain. Therefore, confirming that the result is independent of the chosen mesh is necessary for simulation work. For the bonds expected to fail first, ΔW_{avg} is calculated using iterative local meshes to find the minimum mesh quality needed to achieve convergence.

To perform a simulation, the program must solve a series of equations across the entire model to calculate the outputs. However, as there are an infinite number of bodies that can be simulated, the program must be able to convert any body into a general form over which the equations can be solved. This general form is called the mesh, which converts the body into a set of coordinates called nodes. Based on how these nodes change position for each sub-step, the simulation can solve for the strain and stress experienced by each node. These nodes are coupled into 3D shapes called elements, which extrapolate the node results over the element volume. While the equations and mesh behavior are beyond the scope of this work, the crucial point is that the equations rely on the mesh to generate solutions, and that failure to include enough nodes or improper use of certain element shapes will impact the solution.

As the solution is mesh-dependent, it is crucial to determine what is the minimum mesh quality required to achieve a consistent result. In general, increasing the mesh in a simulation will alter the output up to a certain point. After this point, the output becomes insensitive to the mesh density, and further increases to the density will increase computational cost without meaningfully altering the output. An example of this output convergence is shown in Fig. 2-17. To determine the minimum mesh density required to reach convergence, at least three simulations with varying mesh densities are run, with an output of interest recorded for each one. This process is repeated until the output difference between the iterations is approximately 5 % or less, with the lower density mesh becoming the final mesh. During this process, only the local mesh density in the region of interest should be increased, not the total model mesh.



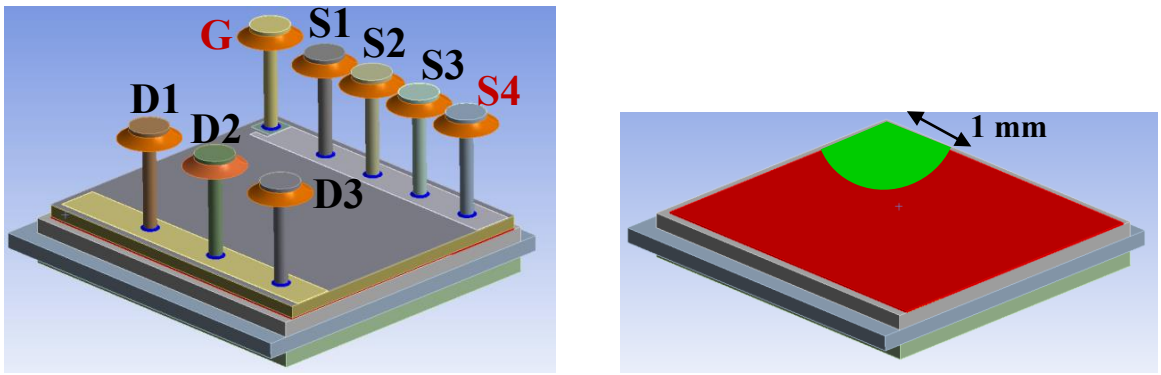
(a)



(b)

Fig. 2-17. Example of a mesh convergence study on a cantilever beam fixed at one end and loaded on the other. (a) A visual depiction of several mesh densities used for testing. The number of elements along the beam's long axis is used as the mesh density metric. (b) The output, in this case the maximum normal stress placed on the beam, converging as the mesh density increases. As the maximum stress has less than a 5 % difference between the 50, 100, and 500 element densities, the normal stress has converged and the 50 element mesh should be used [53].

This mesh convergence study focuses on the bonds expected to fail first within their respective bond groups. For more information on the bond groups, see Section 2.7. For the solder bonds, Source 4 has the highest ΔW_{avg} and is designated as the first solder bond to fail. For the sintered Ag Internal bonds, the Internal Gate has the highest ΔW_{avg} and designated as the first sintered Ag bond to fail. For the sintered Ag Die Attach, the 1 mm Annular region is the expected first failure location. For all scenarios in the coming chapters, these are the three likely points of first bond failure in the package and are highlighted in Fig. 2-18. The following section provides the mesh details and convergence study for each bond using the package with EP-2000 encapsulant.

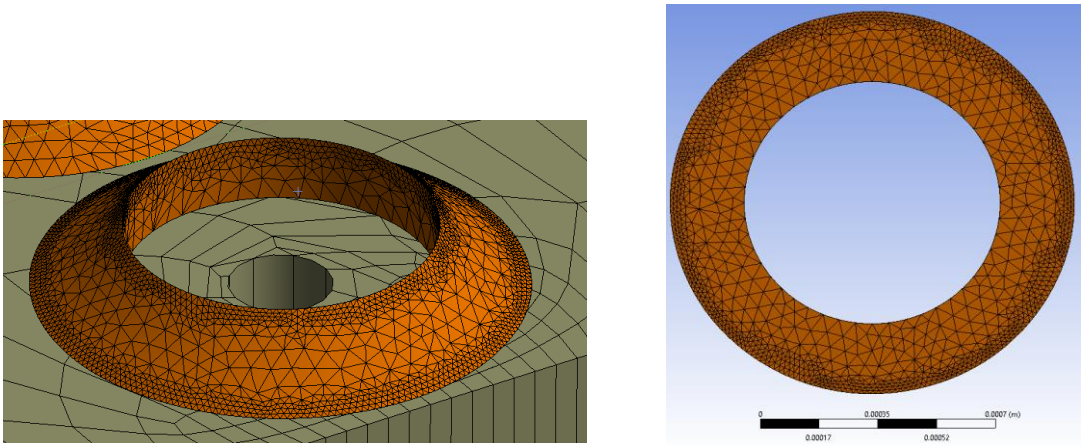


(a) (b)

Fig. 2-18. The labeled bonds in the package. (a) The External (orange) and Internal (blue) pin bonds. Regarding designations, G is for gate, S is for source, and D is for drain. The pins with first failure bonds are marked in red. (b) The 1 mm Annular region on the Die Attach is marked in green.

Regarding the full package, it is meshed with SOLID187 Tet10 and SOLID186 Hex20 elements. For the simulations used in Chapters 3 and 5, there are 281,988 nodes and 134,596 elements. 60 and 80 ppm/°C simulations in Chapter 3 increase the mesh on the Source 4 External bond to compensate for higher deformation and are not covered here. The global mesh is used everywhere with the exceptions of the bonds, the sections of bodies in contact with bonds, and several thin layers throughout the structure.

The Source 4 External bond (S4) is meshed using 20,656 SOLID187 Tet10 elements with 35,799 nodes. Fig. 2-19 displays the bond and Fig. 2-20 displays the mesh convergence plot. Mesh density was primarily increased on the S4 bond, but localized refinement on PCB face was also done. A 5.05 % variation between the second and fourth mesh iteration demonstrates convergence, and the second mesh iteration was used for the study. The average element skewness is 0.46 with a standard deviation of 0.286 on a scale of 0 (best) to 1 (worst), with ANSYS documentation defining 0.25 - 0.5 as good and 0.5 – 0.75 as fair.



(a) (b)

Fig. 2-19. The Source 4 External bond. Both images use the same scale bar of 0.7 mm maximum. (a) The top and sides of the bond with the increased PCB mesh. (b) The bottom of the bond.

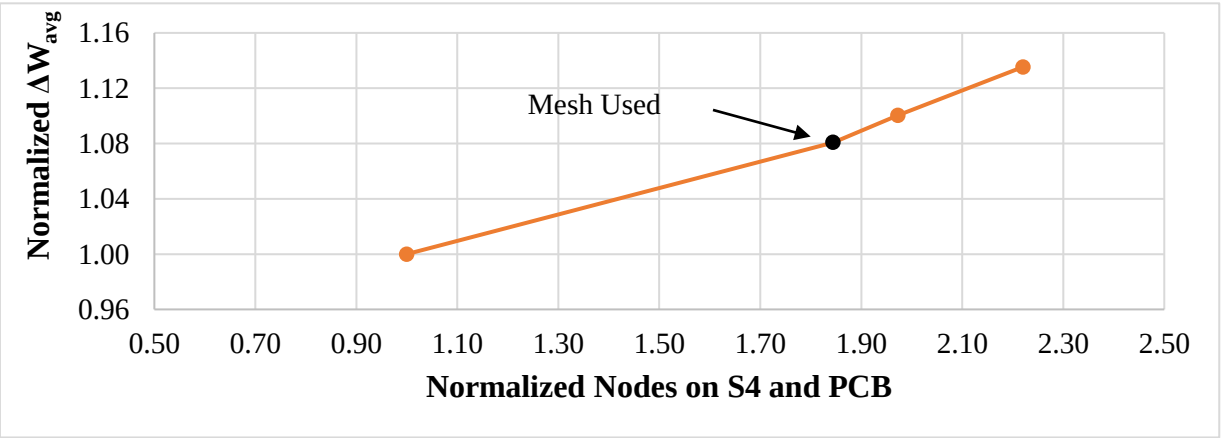
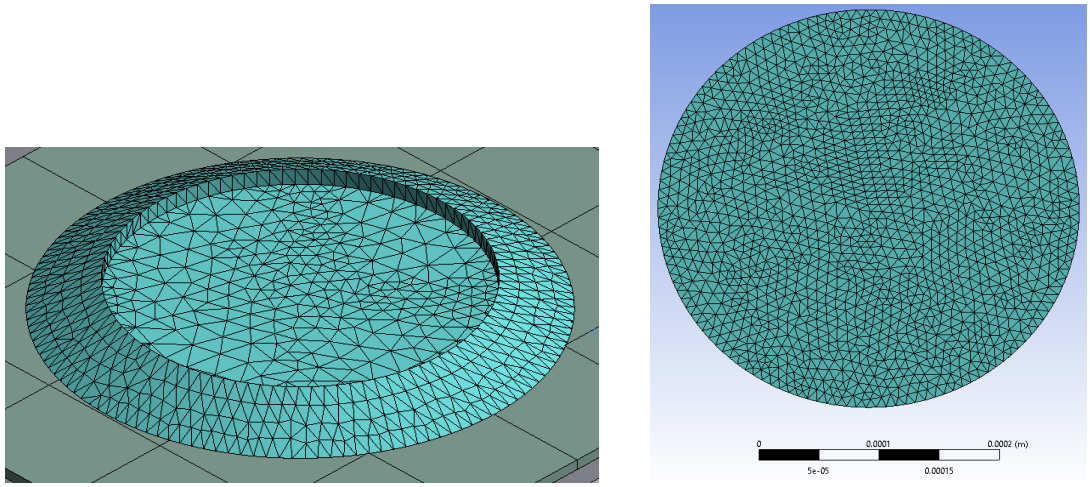


Fig. 2-20. vergence study on External Source 4 bond. The second mesh iteration is used as it has a 5.05 % difference versus the fourth mesh iteration.

The Gate Internal bond (G) is meshed using 16,403 SOLID187 Tet10 elements with 26,848 nodes. Fig. 2-21 displays the bond and Fig. 2-22 displays the mesh convergence plot. Mesh density was primarily increased on the Gate bond, but localized refinement on the encapsulant and the pin were also performed. A 4.98 % variation between the third and fourth mesh iteration demonstrates convergence with the third mesh iteration used. The average element skewness is 0.34 with a standard deviation of 0.20.



(a) (b)

Fig. 2-21. The Internal Gate joint recolored from dark blue for greater contrast. Both images use the same scale bar of 0.2 mm. (a) The top and sides of the bond. (b) The bottom of the bond.

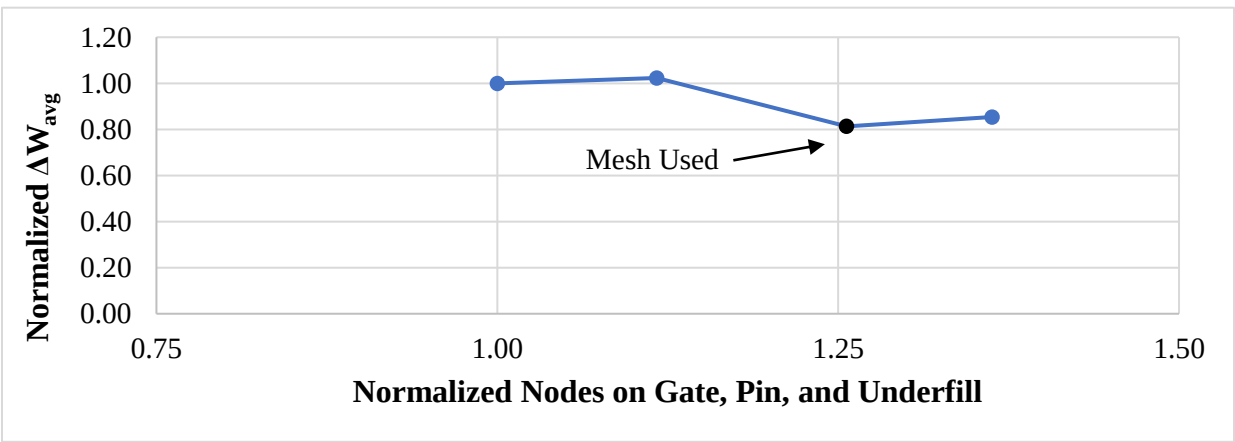


Fig. 2-22. Convergence study on Internal Gate bond. The third mesh iteration is used as it has a 4.98 % difference versus the fourth mesh iteration.

The Die Attach (DA) is meshed using 4,368 SOLID186 Hex20 elements with 24,781 nodes. Fig. 2-23 displays the bond and Fig. 2-24 displays the mesh convergence plot for the 1 mm Annular region. Mesh density was primarily increased on the Die Attach, but extra mesh layers were also added to the Si substrate and the DBC geometry. A 2.47 % variation between the fourth and fifth mesh iteration demonstrates convergence with the fourth mesh iteration used. The average element skewness is 0.02 with a standard deviation of 0.01.

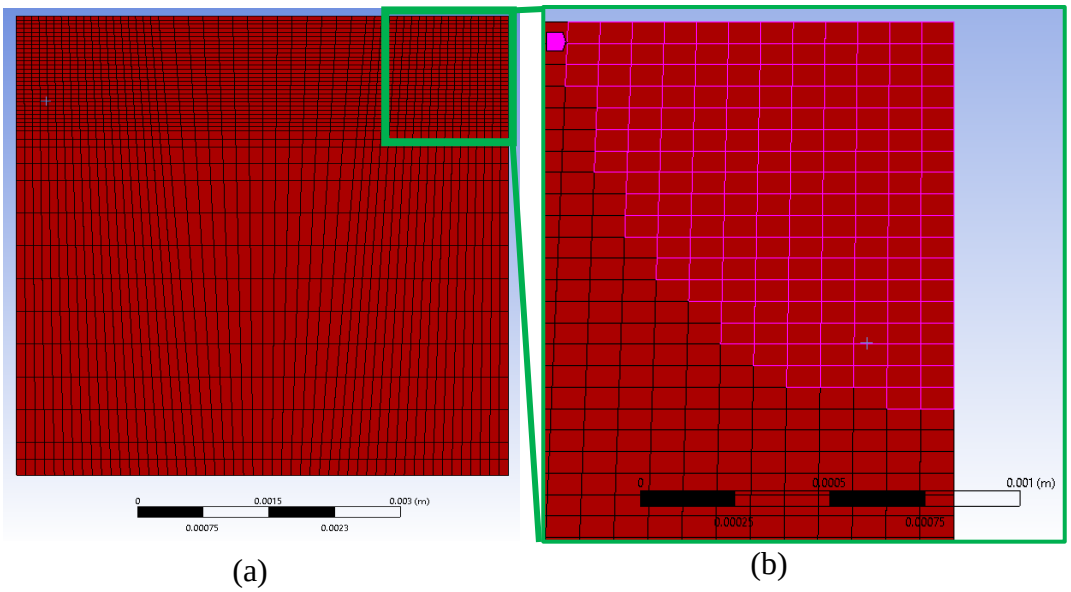


Fig. 2-23. The Die Attach. (a) The full Die Attach, with the mesh concentrated on the edge corners. The scale bar is 3 mm. (b) The 1 mm Annular region highlighted in pink. The scale bar is 1 mm.

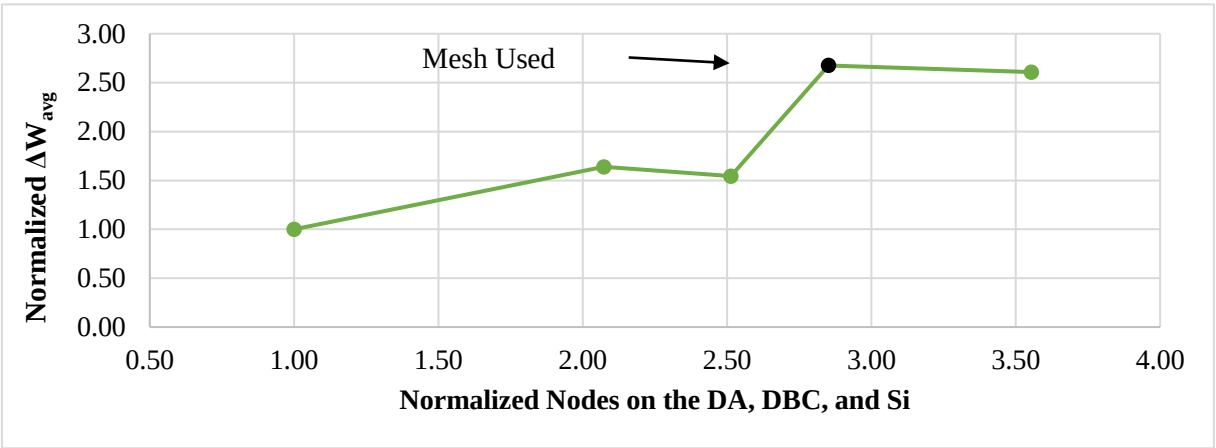


Fig. 2-24. Convergence study on the Die Attach 1mm Annular Region. The fourth mesh iteration is used as it has a 2.47 % difference versus the fifth mesh iteration.

2.5 Material Models

The purpose of this section is to list the material properties used in the simulations and explain the choice of constitutive models used for them. All non-bond materials are represented as isotropic, linearly elastic materials that undergo no plastic deformation. While this is reasonable for metals and ceramics, this is a simplification, as the PCB has both orthotropic behavior and behaves differently at high temperature. The bond materials use both the isotropic, linearly elastic model and the Anand constitutive model. The Anand model is a common viscoplastic model used to study the fatigue of solder and sintered Ag under thermal cycling.

This work utilizes two separate material models. For the material not expected to fail, the first model treats it as linearly elastic and isotropic. Therefore, the material parameters required to model them are the CTE (α), the elastic modulus (E), and the Poisson's ratio (ν). As the Thermal Condition alters the body's temperature instead of generating heat, the material's thermal conductivity is not necessary. The thermal expansion of the material is the basis of thermal strain, hence why CTE is required.

E and ν are the minimum number of constants required to model a material's elastic behavior. By approximating the body's response to stress as identical in all directions (isotropic), the number of constants required to describe the body's elastic behavior reduces from a potential maximum of twenty-one down to three, of which only two must be known. The first material property is E, which relates the applied uniaxial stress (σ_x) to the resulting uniaxial strain (ε_x) through

$$E_{isotropic} = E_x = \frac{\sigma_x}{\varepsilon_x}. \tag{2}$$

Likewise, the shear modulus (G) relates the shear stress (τ_{xy}) to the shear strain (γ_{xy}) through

$$G_{isotropic} = G_{xy} = \frac{\tau_{xy}}{\gamma_{xy}}. \tag{3}$$

The third material property is ν, which relates E and G through

$$E_{isotropic} = 2G_{isotropic}(1 + \nu). \tag{4}$$

E is a common property on data sheets, and v can be approximated if it is missing. While isotropy is a reasonable assumption for most metals and ceramics, it is a simplification for composites like FR4, who's in-plane fiber reinforcement give $E_{in\text{-}plane} > E_{out\text{-}of\text{-}plane}$ and $\mathrm{CTE}_{\text{in-plane}} < \mathrm{CTE}_{\text{out-of-plane}}$.

The final model assumption is that any plastic deformation experienced by the materials will not influence the bond fatigue, so the material is treated as purely elastic. This is a common assumption for metals and ceramics, as the high melting temperature and yield strengths lowers the probability of plastic and creep deformation. For polymers like the encapsulants or FR4, this assumption is weaker due to the low glass transition temperature and prevalence of creep at elevated temperatures. However, the polymers are treated as temperature independent elastic for simplicity, as the temperature dependent properties or models to acknowledge the viscoelastic behavior do not exist. The isotropic, linearly elastic material properties for all materials are in Tables 2-4. If available, temperature dependent properties are used. The only estimated properties are v for the encapsulants, with 0.35 being chosen as a reasonable polymer value. Encapsulant material properties are taken from their respective data sheets, while ANSYS Granta is used for all other material properties.

The second model, representing the inelastic behavior of the bonds, is the Anand constitutive model [54], [55]. In conjunction with the elastic properties, it forms an isotropic, elastic-viscoplastic model used for modeling low cycle fatigue. Its widespread use for modeling bond fatigue in is due to both the accuracy and the convenience of the model. Studies like [56], [57], [58], and [59] have determined the material constants required to represent various solders and sintered Ag with the Anand model, while studies like [25], [60], [61], [62] [63], [64], [65], [66], [67], [68], [69], and [70] use it to represent the bond material in ANSYS simulations.

When discussing the inelastic deformation and cracking of bond materials, we are discussing the generation, motion, and pinning of dislocations in the metal's crystal lattice. Dislocations are discrepancies in the expected crystal structure, and a certain density of them within a material is expected. While a discussion of dislocation types and behavior is beyond the scope of this work,

it is by the generation and movement of these dislocations that a material inelastically deforms. This inelastic deformation, and thus dislocation behavior, can be separated into plastic (rate-independent) and creep (rate-dependent) behaviors. Plastic deformation refers to the near instantaneous dislocation generation and motion in a material that occurs when the applied stress exceeds the material's yield strength. Further dislocation activity can occur over time depending on factors like temperature and applied stress and is called creep deformation. Whether creep is appreciable depends on temperature, as amorphous materials like glasses and polymers show appreciable creep at their glass transition temperature while crystalline materials like metals and ceramics show appreciable creep at temperatures 30-60 % of their absolute melting temperature. Due to the intentionally low melting temperatures of both lead and non-lead solders, they experience creep at room temperatures. Therefore, any constitutive model representing solder in a thermo-mechanical simulation must account for both plastic and creep deformation in a unified viscoplastic model. In addition, inelastic behavior depends on the interactions between the dislocations and the material microstructure. While an explanation of material behavior involving strain hardening or dynamic recovery is also beyond the scope of this work, it is necessary to acknowledge that inelastic deformation alters the microstructure, which then alters future inelastic deformation. Therefore, any viscoplastic model must also evolve in response to deformation already applied.

The Anand model meets the listed concerns while also being feasible to use. To identify the properties required to use this model, a series of constant true strain rate uniaxial compression or DMA tests are performed at varying temperatures. These tests give nine material constants, which allow use of the governing flow equation and three evolution equations that comprise the Anand model. These equations "account for the physical phenomena of strain-rate and temperature sensitivity, strain rate history effects, strain hardening, and the restoration process of dynamic recovery" [62]. They do this using a single scalar value that represents the material's isotropic resistance to inelastic flow. This resistance comes from strengthening mechanisms like dislocation density, grain size effects and solid solution strengthening. As inelastic deformation alters the microstructure, the evolution equations compensate for resulting parameters changes. The model does not use any specific yield conditions or any loading or unloading criteria. The model also assumes inelastic deformation occurs at any non-zero stress state. If $\frac{d\varepsilon_p}{dt}$ is the time

dependent change in the inelastic strain, $\frac{ds}{dt}$ is the time dependent change in the isotropic resistance to inelastic flow, and the rest of the constants are defined in Table 2-6, then the flow and three evolution equations are

$$\frac{d\varepsilon_p}{dt} = A * \exp\left(\frac{Q}{RT}\right)(\sinh[\zeta\sigma * s^{-1}])^{\frac{1}{m}}, \tag{5}$$

$$\frac{ds}{dt} = \left\{h_0|B|^a \frac{B}{|B|}\right\}\left(\frac{d\varepsilon_p}{dt}\right), \tag{6}$$

$$B = 1 - \frac{s}{s^*}, \tag{7}$$

$$s^* = \hat{s}\left(\frac{d\varepsilon_p/dt}{A} * \exp\left[\frac{Q}{RT}\right]\right)^n. \tag{8}$$

The convenience of the Anand model is that it is already present in ANSYS, and only requires nine material properties. The manual implementation of other constitutive models into ANSYS is complex and time consuming, resulting in the Anand model becoming common in simulation fatigue literature.

Table 2-3. The Isotropic, Linearly Elastic Material Properties Between -40 °C and 125. Designates an Estimation.*

Material	Young's Modulus (GPa)	CTE (ppm/°C)	Poisson's Ratio (unitless)
Copper	129 - 119	16.2 – 17.4	0.35
Aluminum nitride	341 - 338	4.8	0.27
Sintered silver	9.01 – 2.64	19.6	0.37
Silicon	163 - 162	2.14 – 2.92	0.275
Silicon nitride	314 - 312	3.88 – 4.09	0.26
Gold	77 - 74	13.5 – 14.2	0.425
Nickel	208 - 200	11.9 – 13.3	0.315
FR4	24.6	15.5	0.136
Sn60Pb40 solder	30	24	0.4
ME-531 Encapsulant	6	21	0.35*
EP-2000 Encapsulant	17.5	14.9	0.35*

Table 2-4. The Anand Material Properties for Solder and Sintered Ag, Adapted From [68].

Constant	Sintered Ag [59]	Sn60Pb40 [58]	Definition
s_o (MPa)	2.768	56.33	Initial value of deformation resistance
Q/R (K)	5706	10830	Activation energy divided by the Boltzmann constant
A (s^{-1})	9.81	$1.49 * 10^7$	Pre-exponential factor
ζ	11	11	Stress multiplier
m	0.6572	0.303	Strain rate sensitivity of stress
h_0 (MPa)	15800	2640.8	Hardening constant
$\hat{s}$ (MPa)	67.389	80.42	Coefficient of deformation resistance saturation value
n	0.00326	0.0231	Strain rate sensitivity of saturation value
a	1	1.34	Strain rate sensitivity of hardening

2.6 Using ΔW_{avg} as a Simulation Metric of Fatigue

The section introduces the simulation metric used to quantify the per-cycle thermal fatigue generated in the bonds. Initial remarks focus on the physical and mathematical meaning of ΔW_{avg}, and how it has been applied in previous literature. Final remarks focus on the stipulations for comparing bond fatigue using ΔW_{avg}.

While experimental work quantifies the cycles to failure and qualifies the failure mechanism, simulation work qualifies the stress, strain, and related values in the package. Specifically, it quantifies metrics that allow comparisons of fatigue both within and across simulations. By calculating and comparing a single value, you can evaluate design variants at a faster rate than experimental methods.

The metric of fatigue evaluation in this thesis is volume-averaged inelastic strain energy density per cycle (ΔW_{avg}). In this work, ΔW_{avg} is used interchangeably with the term "per-cycle fatigue". It measures the average inelastic work performed on a set of mesh elements over a single thermal cycle due to the elements undergoing both rate-independent and rate-dependent inelastic deformation. Volume averaging diminishes the effects of stress singularities and meshing on ΔW_{avg}. Bond failure through thermal cycling is a type of low cycle fatigue, as the bond undergoes inelastic deformation each cycle. Therefore, this work focuses only on inelastic behavior of the bonds. To prevent confusion, the definition of "inelastic" in this work is the same as "plastic" in ANSYS and "viscoplastic" in the Anand constitutive model, in that it represents both plastic and creep deformation. Inelastic strain energy measures the work utilized to permanently deform the material, while converting to strain energy density accounts for the bond geometry. It is measured on a per-cycle basis to measure crack initiation and propagation on a per-cycle basis.

When studying a single mesh element, if σ_x and ε_x^{inel} represent the normal stress and inelastic strain placed on the element along the x axis, while τ_{xy} and γ_{xy}^{inel} represent the shear stress and inelastic strain placed on the element along the x-y axis, then the total inelastic strain energy density (W_i) on that element is

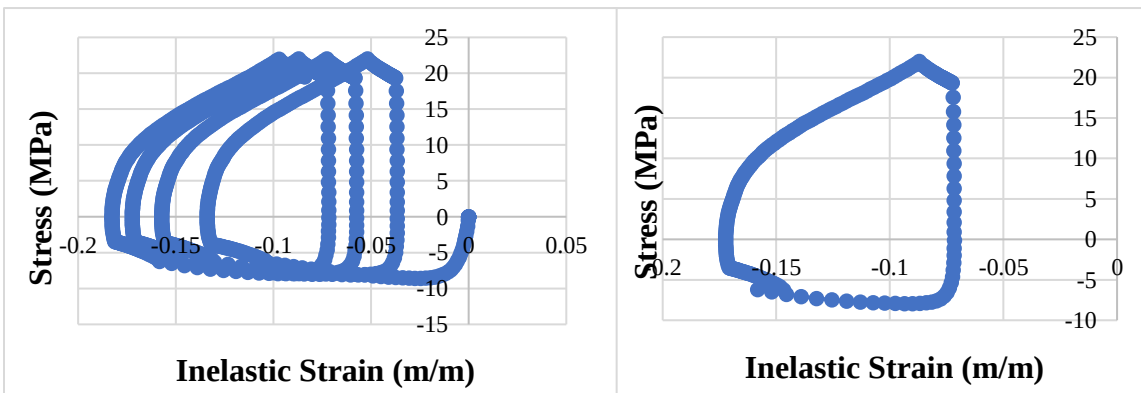
$$W_i = \int \sigma_x \varepsilon_x^{inel} + \int \sigma_y \varepsilon_y^{inel} + \int \sigma_z \varepsilon_z^{inel} + \int \tau_{xy} \gamma_{xy}^{inel} + \int \tau_{yz} \gamma_{yz}^{inel} + \int \tau_{xz} \gamma_{xz}^{inel}. \quad (9)$$

This is equivalent to summing the area inside of all six stress-strain hysteresis loops representing that element over all temperature cycles, like the one shown in Fig. 1-16(a). If V_i is the volume of each element in the body being studied, then the total volume-averaged inelastic strain energy density of the element set being studied is

$$W_{avg} = \frac{\sum_{i=1}^{i=n}(W_i * V_i)}{\sum_{i=1}^{i=n}(V_i)}. \quad (10)$$

As we are interested in the per cycle increase of W_{avg} instead the total value, the last step is to convert it into a per cycle value with

$$\Delta W_{avg} = W_{avg-cycle\ end} - W_{avg-cycle\ start}. \quad (11)$$



(a) (b)

Fig. 2-25. Example of a stress-inelastic strain hysteresis plot. (a) A plot displaying the XY shear stress and strain over four thermal cycles for a single node, with the starting value being (0, 0). (b) A single cycle of (a) to emphasize how these results often appear as "ratcheting" loops. The contribution of XY shear to the ΔW_{avg} of a single node or element is equal to the absolute area inside the curve in (b).

ΔW_{avg} is the basis of energy-based solder fatigue models discussed in [71]. This paper specifically focuses on Darveaux's model, which is detailed in [25] and [72]. The fundamental relationship of Darveaux's model is that an increase in ΔW_{avg} will reduce the number of cycles to both crack initiation and propagation. If N_0 represents thermal cycles to initiate a crack in a bond,

and K_1 and K_2 are positive and negative line-fitting constants respectively, then the relationship between the simulation metric ΔW_{avg} and the experimental N_0 is

$$N_0 = K_1 * \left(\Delta W_{avg}\right)^{K_2}. \tag{12}$$

A similar equation relates crack growth to ΔW_{avg}. If a is the crack length, $\frac{da}{dN}$ is the crack growth per thermal cycle, and K_3 and K_4 are again line-fitting parameters, then the relationship proposed by Darveaux is

$$\frac{da}{dN} = K_3 * \left(\Delta W_{avg}\right)^{K_4}. \tag{13}$$

While these relationships were originally proposed for $Sn_{62}Pb_{36}Ag_2$ solder balls in ball grid array packages, Darveaux's model has been used elsewhere. For example, [73] uses an unspecified solder in strips instead of solder balls, [60] applies the model to a single large-area $Sn_{63}Pb_{37}$ bond, and [61] applies the model to a single large-area sintered Ag bond. While this thesis does not utilize Darveaux's relationships, ΔW_{avg} is used as a simulation metric with the expectation that future experimental work will evaluate if Darveaux's relationships are applicable to this package.

However, there are other fatigue models besides Darveaux's model in literature [71]. One example is the Coffin-Manson model, which correlates the plastic (rate-independent) shear strain amplitude to the cycles to bond failure. While not identical, the Solomon and Engelmaier models also relate shear strain, either plastic or total, to the cycles to failure. Another type of model focuses exclusively on creep strain in solder, which is appreciable at room temperature and significant in loading due to temperature cycling. Two models that use this behavior are the Syed model and the Knecht and Fox model. The main disadvantage of all the listed models above is that they only consider one of the two sources of inelastic deformation in bond materials. By considering both creep and plastic strain of bond materials using the Anand model, energy-based models are more accurate than the previously listed models. As the creep and plastic strains cannot be individually calculated in ANSYS, the use of this model also disqualifies the previously listed models.

To use ΔW_{avg}, select a group of mesh elements, whether that represents a bond or a smaller section. Using (4), (5), and (6), the output code in Appendix B calculates ΔW_{avg} for that region.

If two bonds comparable, the bond with the larger value of ΔW_{avg} is expected to crack and fail first. There are three stipulations to using ΔW_{avg} as a relative fatigue metric to compare bonds both within and across simulations. The first is a general rule, that comparisons across simulations only work if the boundary conditions are identical. The second and third rules are inherent to ΔW_{avg} and are consequences of material properties and volume averaging, respectively. The second rule is that ΔW_{avg} can only be compared between bonds that are the same material. As the element strain is dependent on elastic and inelastic material properties, an identical bond made of different materials will give different values of ΔW_{avg}. Without experimental tests to establish which material fails first, there is no way to conclude which material would endure a greater number of cycles based on ΔW_{avg} alone, even if the values are different. The third stipulation is the volume of the regions being compared should be as similar as possible. As ΔW_{avg} averages the total inelastic strain energy of a region across its volume, the comparison quality degrades when comparing regions of significantly different volume. Rules #2 and #3 determine which bonds can be compared against one another and are the basis of bond groups discussed in Section 2.7.

2.7 Bond Groups and Identifying Which Bonds Fail First

This section focuses on how to use ΔW_{avg} to identify which bonds are expected to fail first. All bonds and regions within a bond group have the same volume and material, so the region with the highest ΔW_{avg} in a group will be the first bond in the group to fail. As the simulation model is only applicable to a package with no failed bonds, the purpose of the simulation is to identify the first failure bonds in each group and reduce their ΔW_{avg}. For the PCB-Interposer package, there will be a sintered Ag bond and solder bond that fails first, with no way to determine which one fails before the other. As later analysis shows, one of the two possible locations of package failure would disrupt the gate signal, so supporting that bond takes priority.

If two regions have the same volume and are made of the same material, then the region with the higher value of ΔW_{avg} will fail first through crack initiation and propagation. Recall from Section 2.6 that the two regions can only be compared if they are made of the same material and volume. A bond group is a set of regions that conform to these rules, so ΔW_{avg} of any one region in the group can be compared against any other within the group. The region with the highest ΔW_{avg} in a bond group will fail before all other regions in the group. This bond is designated as the first failure bond. Once the first failure bond undergoes crack initiation and propagation, the real package no longer matches the simulation model and has degraded performance. Therefore, the focus of this simulation work is to identify the first failure bonds and reduce the fatigue placed on them.

If two bonds of identical volume are made of different material, it is impossible to determine which bond fails first using only a comparison of ΔW_{avg}. Likewise, a large and a small bond made of identical material also cannot be compared. However, if a critical region of the larger bond is chosen such that it has the same volume as the smaller bond, it may be possible to make a ΔW_{avg} comparison. While this concept has not yet been explored in literature to the best of the author's knowledge, it will be utilized to compare sintered Ag bonds of different sizes. Experimental verification of this concept is left to future work.

If all the package bonds all have the same volume and material, then a thermo-mechanical analysis is straightforward. The bond with the highest ΔW_{avg} is both the first failure bond in the

group and in the package, and our efforts to improve reliability focus on lowering the fatigue on the package's first failure bond. However, if there are multiple bond groups, each group will have a first failure bond. As the two values of ΔW_{avg} are not comparable, simulations cannot predict what is the true location of initial package failure. Therefore, a simulation with three bond groups will report three potential failure locations, with experimental testing required to identify which of the three will fail first. Without experimental work, it is up to the engineer's judgement to determine what potential failure location is most crucial to reduce fatigue in.

The limitations of multiple bond groups apply to the PCB-Interposer-on-DBC package. From largest in volume to smallest, the three bond geometries in the package are the die attach, the External pin bonds, and the Internal pin bonds. To further complicate comparison, the die attach and Internal bonds are made of sintered Ag, while the External bonds are made of Sn60Pb40. Based on the stipulation of identical bond volume, there are three unique bond groups, resulting in three possible locations of first failure. However, by to the identical material stipulation, there are only two bond groups, which are the first sintered Ag bond and the first Sn60Pb40 bond to fail. If one could select a region of the die attach such that it has comparable volume to the Internal bonds, then the fatigue between the two different bond geometries could be compared.

That conclusion is the basis of the Die Attach Comparable Region, which is the die attach region that is comparable to the Internal bonds. The selection of the die attach corner is an intentional overestimation of the die attach fatigue, as Fig. 2-26 shows inelastic work placed on the corners is higher than the bulk. By comparing the Internal bonds to the Comparable region, the entity with the highest ΔW_{avg} is the sintered Ag bond expected to fail first. The bond groups used in this thesis are shown in Fig. 2-27.

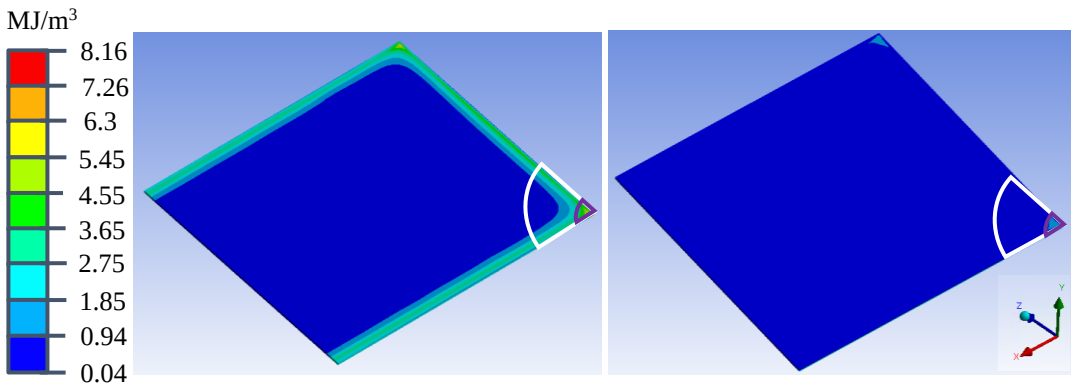


Fig. 2-26. Discrepancy between the element inelastic work density in the Die Attach bulk and edges. The white outline represents the Edge region, while the purple outline is the Comparable region. (a) In the No Encapsulant scenario, the edge elements have 5-100x greater inelastic energy density than the bulk. (b) In the EP-2000 underfill scenario, the underfill lowers the inelastic work on the edges, but the corners remain high work regions.

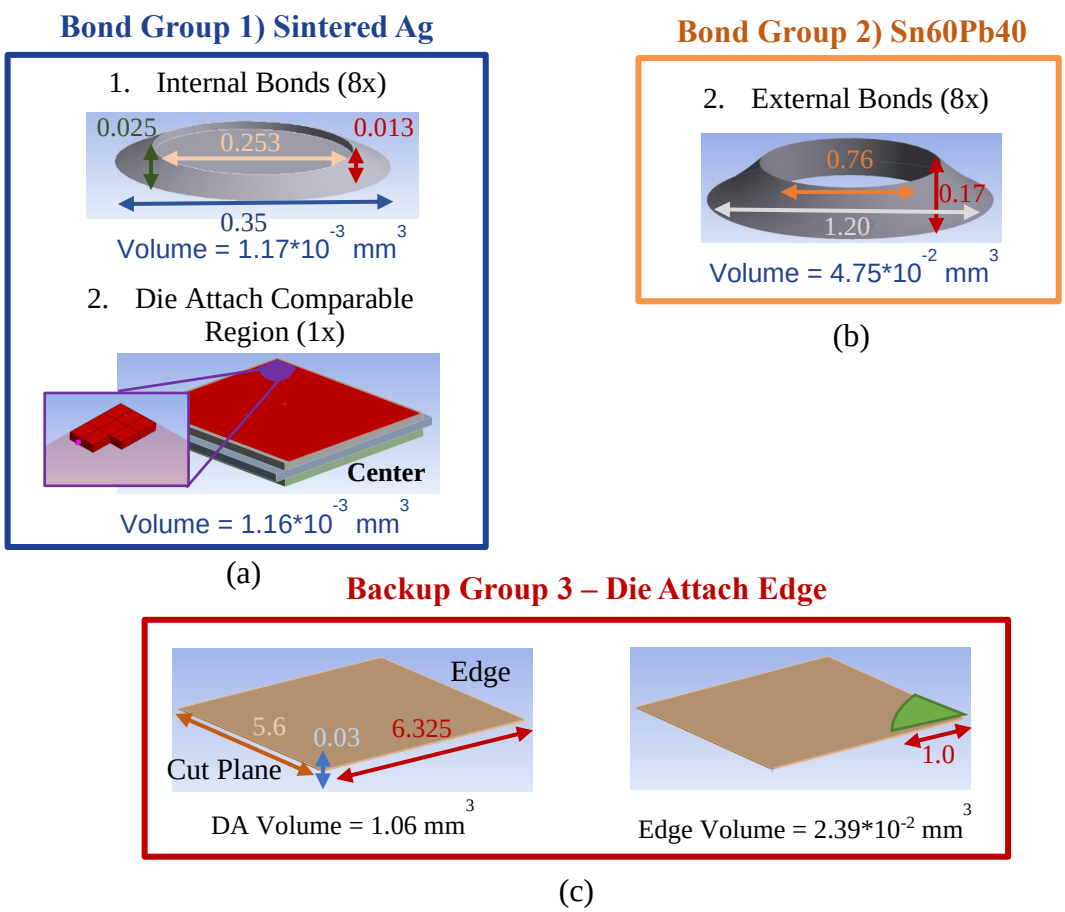


Fig. 2-27. The two primary and single backup bond group. (a) The first sintered Ag bond to fail is either one of the eight Internal bonds or is the die attach corner. (b) The first Sn60Pb40 bond to fail is one of the eight External bonds. (c) The 1 mm Edge region is also studied if the Comparable region analysis is not valid.

There are two assumptions in this analysis. First, the bond with the greatest ΔW_{avg} within a group is the first bond to crack and fail. Second, a smaller bond can be compared against a part of a larger bond if they are of the same material. Regarding the first assumption, both [62] and [73] showed ΔW_{avg} correctly predicting which bond will fail first in experimental thermal cycling. Regarding the second assumption, while the stipulations for comparing ΔW_{avg} are met, this concept has not yet been explored in literature. Previous work focused on the comparing identical bonds in various situations like in [25], or comparing different diameter bonds in [60]. While it is left to future experimental work to validate this comparison, an analysis of the Die Attach Edge region is also included in this thesis. If the Comparable region assumption is invalid, then Bond Group 1 in Fig. 2-27 becomes the Internal bond group, Bond Group 2 remains as is, and Bond Group 3 becomes a potential location of initial package failure.

When comparing the per-cycle fatigue on the Internal bonds versus the edge of the die attach, the volume difference between the Internal and total die attach is significant. Specifically, the Internal bond volume is only 0.1 % of the total die attach. If a crack initiates in the die attach corner, it will initially have only minor impact on $R_{th,JC}$. For it to become significant, it must propagate first through the edges of the die attach, and then through the bulk. Meanwhile, the Internal bond is the entire region of interest, so any crack initiation or propagation is liable to destroy the electrical connection to the die. If the die attach is both an overestimation of bond fatigue and requires significantly more crack propagation than the Internal bond for module degradation, this adds stipulations to the first Sintered Ag bond analysis. If the Die Attach Comparable region has a greater ΔW_{avg} than the Internal bonds, then the analysis cannot determine whether the module fails through an Internal bond failure or die attach failure. However, if an Internal bond has a greater ΔW_{avg} than the DA Comparable region, then that Internal bond will definitively fail before the die attach.

Regarding the use of the Die Attach 1 mm Edge region instead of the Total Die attach, the reasoning lies in Fig. 2-26. While the edge is only a fraction of the total volume, the work density is 5-100x greater than the bulk in the No Encapsulant scenario. The corner is chosen

because it is the expected location of first failure for the die attach and is sensitive to the design changes made in this work.

The process for determining what is the first failure bond of each group is detailed here, with Fig. 2-28 acting as a reference. For the sintered Ag bonds, the Internal G, S1, S4, D1, and D3 bonds are compared alongside the Die Attach Comparable region. While the full analysis is in Chapter 3, the Internal Gate bond has the highest ΔW_{avg} in all scenarios and is thus the first sintered Ag bond to fail. For the External solder bonds, ΔW_{avg} of the External G, S1, S4, D1, and D3 is calculated and compared against one another. While the full analysis is also in Chapter 3, the conclusion is that the Source 4 has the highest ΔW_{avg} in all scenarios and is thus the first solder bond to fail. Without experimental work, it is impossible to determine if the Internal Gate bond fails before or after the External Source 4 bond. However, as loss of the Source bonds will only degrade signal, and loss of the Gate bonds will cause complete package failure, the Internal Gate takes priority.

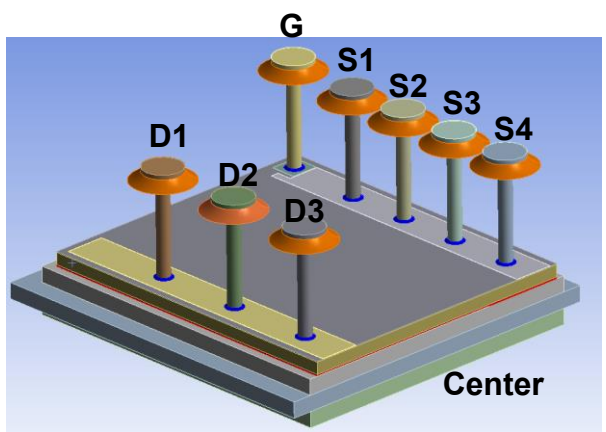


Fig. 2-28. The package with all bond designations labeled. G stands for Gate, S stands for Source, and D stands for Drain. In this thesis, ΔW_{avg} is calculated for all Internal and External bonds except S2, S3, and D2, as they are between the bonds closest (S4, D3) and furthest (G, D1) from the center cut plane.

Chapter 3. Identifying Vulnerable Bonds and Parameter Sweeps

3.1 Purpose of Chapter 3

The objective of Chapter 3 is to identify which bonds in the PCB-Interposer package will fail first and establish the relationship between encapsulant properties and those first failure bonds. As any cracked bonds will degrade or break the package, identifying which bonds fail first and extending their lifetime is necessary. The bonds that fail first are those that experience the largest per-cycle fatigue, ΔW_{avg}, within their bond group. Once the most vulnerable bonds are established, the relationship between the encapsulant material properties and the bond's ΔW_{avg} is explored through parameter sweeps.

Section 3.2 provides the background for how encapsulant CTE and *E* alters bond fatigue in BGA packaging. The solder balls expected to fail first show reduced per-cycle fatigue if the encapsulant CTE is matched to the substrates held together by the balls. Further reduction in per-cycle fatigue occurs as the encapsulant becomes stiffer. Therefore, the thermo-mechanically optimal encapsulant in a BGA package has a CTE like the package components (< 25 ppm/°C) with the highest possible elastic modulus (> 1 GPa). While the PCB-Interposer is not a BGA package, it is hypothesized that the same concepts of matching CTE and maximizing *E* apply to the PCB-Interposer. To identify the optimal CTE and *E* properties, encapsulant parameter sweeps are performed.

Section 3.3 outlines the simulation setup, which is discussed in greater detail in Chapter 2.

Section 3.4 identifies the sintered Ag bond expected to fail first and what encapsulant properties minimize fatigue. The Internal Gate is the expected first failure sintered Ag bond and per-cycle fatigue is minimized using an encapsulant with a CTE equal to 8 ppm/°C and maximum *E*. Reducing *E* or deviating from this CTE increases the per-cycle fatigue on the Internal Gate. The location of the Internal Gate bond within the package and the contributions of

shear to the inelastic work align with literature trends. Losing the Internal Gate bond will cause package failure.

Section 3.5 identifies the Sn60Pb40 bond expected to fail first and what encapsulant properties minimize fatigue. The External Source 4 bond is the expected first failure solder bond and per-cycle fatigue is minimized using an encapsulant with a CTE equal to 24 ppm/°C and maximum *E*. Reducing *E* or deviating from this CTE increases the per-cycle fatigue on External Source 4. While the first failure bond location and structure are unique in literature, the conclusion is that the minimal deflection of the pins closest to the package center cause high inelastic work on the bonds closest to the package center. Loss of the External Source 4 bond will degrade package performance.

Section 3.6 summarizes the effects of the encapsulant on the die attach. While the die attach is not expected to be a primary failure location, it is included to demonstrate the benefits of encapsulation. Using encapsulant with a CTE like Cu (16 ppm/°C) minimizes per-cycle fatigue as it constrains the expansion of the Cu plate on the DBC. Maximizing *E* further reduces the per-cycle fatigue.

Section 3.7 discussing the chapter conclusions. The primary conclusion is that the sintered Ag Internal Gate bond is both a crucial bond to protect and the most likely location of initial package. It has both the highest per-cycle fatigue of all bonds and causes package failure if it breaks. Therefore, Chapter 4 focuses on the Internal Gate when studying real encapsulants. However, experimental temperature cycling is required to confirm if the Internal Gate sintered Ag bond will fail before the External Source 4 solder bond.

3.2 How Encapsulant CTE and E Influence Bond Fatigue

This section's objective is to summarize the relationship between encapsulants and solder fatigue in BGA packaging, and how to demonstrate if a similar relationship applies to the PCB-Interposer package. In BGA packaging, using encapsulants with a CTE matching the package substrates and the maximum allowable elastic modulus minimizes per-cycle fatigue. Even though the PCB-Interposer is different from a BGA package, the concept of a low CTE mismatch, high *E* encapsulant reducing per-cycle fatigue is hypothesized to also apply to the novel package. To evaluate this hypothesis, the first failure bonds must first be identified, as they are what limits the reliable lifetime of package. As ΔW_{avg} cannot be compared across different bond materials, there will be a sintered Ag bond that fails before all other sintered Ag bonds, and a solder bond that fails before all other solder bonds, with no way to identify which is the true location of first failure using only simulations. Once these locations of first failure are identified, parameter sweeps of encapsulant CTE and *E* can be performed to establish what encapsulants minimize the per-cycle fatigue on those vulnerable bonds.

The concept of using encapsulants to reduce thermal fatigue in BGA is discussed in [62], [70], [74], [75], [76], [77], and [78]. The following paragraphs primarily focus on [70] and [74].

Fig. 3-1 displays the simulation geometry and the encapsulant property sweep results from [70]. This example shows how encapsulant CTE and *E* alter the bond fatigue. If N_f is the thermal cycles to failure and is used to calculate the normalized fatigue life and *C* is an experimental constant not specified in [70], then the relationship relating N_f and ΔW_{avg} in Fig. 3.1(b) is

$$N_f = C * \Delta W_{avg}^{-1} \;\rightarrow\; N_f \propto \frac{1}{\Delta W_{avg}}\,. \tag{14}$$

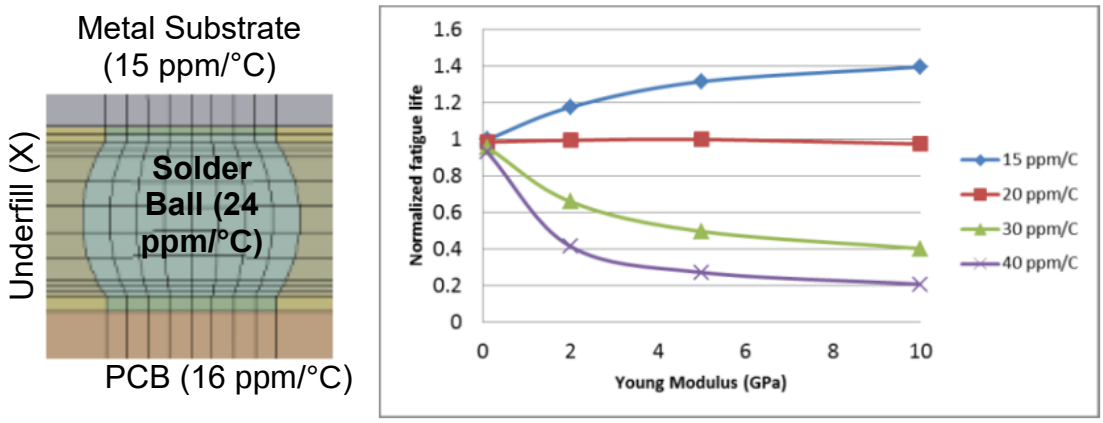
Regardless of the encapsulant CTE, the solder ball has a near-constant lifetime is all encapsulants have *E* = 0.1 GPa. As *E* increases, the encapsulant's CTE becomes relevant. If the encapsulant CTE is like the metal substate and PCB, the solder fatigue decreases relative to the No Encapsulant scenario, and the lifetime increases. However, if the encapsulation CTE is dissimilar to the substrates, increasing *E* further increases bond fatigue. While the 20 ppm/°C encapsulant is most like the solder balls, using that encapsulant has only minor effect, so

matching the CTE of the solder does not lead to the best outcome. This is an important distinction, as older BGA encapsulation papers specifically claim that matching the CTE of the solder is most optimal. This conclusion arises from their lowest CTE encapsulants (~25 ppm/°C) having the highest cycles until failure in thermo-mechanical testing. As these papers do not perform parameter sweeps, it is unknown if their low CTE encapsulation is most optimal because it matches the CTE of the solder balls, or if it is the CTE with the lowest substrate mismatch.

To summarize, the CTE mismatch of the encapsulant to the package substrates determines if encapsulant adds or subtracts from the per-cycle bond fatigue. If the stiff encapsulant CTE is matched to one or both substrates (15 ppm/°C), the encapsulant couples the thermal warpage of the substates, resulting in more uniform thermal warpage and reducing per-cycle bond fatigue. A mismatched encapsulant (40 ppm/°C) results in both greater and less uniform warpage, raising the per-cycle fatigue. [74] found that encapsulants reduced the shear and bending stresses placed on the solder balls, but the CTE primarily altered the normal stresses. Using a CTE comparable or lower than the solder compressed the solder balls, eliminating tensile stress concentrations and lowering bending stress. When the CTE increases above the solder balls, tensile stresses were introduced at the joint edges, which increased per-cycle fatigue. While pinning the substates together and coupling their warpage does increase the stress placed on the substrates, this magnitude is not enough to introduce plastic deformation or cracking. What CTEs qualify as helpful or harmful depends on the simulation materials and geometry. [70] identifies CTE of 30 ppm/°C and higher as increasing fatigue, while [75] shows a corner glue with CTE of 30-50 ppm/°C as lowering fatigue.

While the CTE mismatch determines if the encapsulant is harmful or helpful, the encapsulant stiffness determines the magnitude of that effect. Defined as a material's resistance to elastic deformation, stiffness is dependent on component shape and elastic modulus (E). As the geometry is constant, this thesis focuses only on E. Referring to Fig. 3-1, bond lifetime is constant if $E = 0.1$ GPa. Regardless of the CTE mismatch, the soft encapsulant is too mechanically weak to couple the substrate warpage or alter the forces placed on the bond, so the outcome is like not using any encapsulant. In general, an encapsulant with an $E \geq 1$ GPa can alter the bond fatigue. If the CTE mismatch is minimal, the encapsulant acts as second "bond" pinning

the structure together and reducing the strain, particularly the shear strain, placed on the bond during cycling. If the mismatch is significant, the encapsulant pushes on the bonds and substrates, increasing per-cycle bond fatigue. Fig. 3-2 summarizes these conclusions in a matrix.



(a) (b)

Fig. 3-1. How the underfill CTE and E influenced ΔW_{avg} in a BGA package. (a) A part of the simulation geometry showing a solder ball holding together a PCB and metal substrate while encased in encapsulant. The CTEs for each structure are included. (b) A CTE and E sweep of the encapsulant vs the predicted fatigue lifetime of the solder bond. The most optimal outcome tested is a 15 ppm/°C encapsulant with the maximum E.

Encapsulant Properties vs. BGA Bond Fatigue

	Low E (Soft)	High E (Rigid)
CTE Closely Matched	No Impact	Fatigue Reduction Vs No Encapsulant
CTE Not Matched	No Impact	Fatigue Increase vs No Encapsulant

Fig. 3-2. A matrix summarizing the effects of encapsulant. Determining the cutoff between E and CTE requires extensive underfill CTE and E sweeps.

While the use of specific encapsulants to increase solder ball lifetime is well established, the exact mechanical relationship between the input and output variables is not well established. For example, the package material geometry, CTE, E, and v will influence ΔW_{avg}, but no comprehensive model relating these factors to a fatigue metric like ΔW_{avg} or shear strain range exists. A basic model relating the solder bond geometry and component CTE is in Fig. 3-3 and

equation (15). If γ is the shear strain, *DNP* is the distance between the most exterior solder ball and the center of the package, *h* is the height of the solder ball, then the shear strain experienced by the outermost solder ball due to a CTE mismatch and temperature change is

$$\gamma = \left(\frac{DNP}{h}\right)\left(CTE_{Board} - CTE_{Chip}\right)(\Delta T). \tag{15}$$

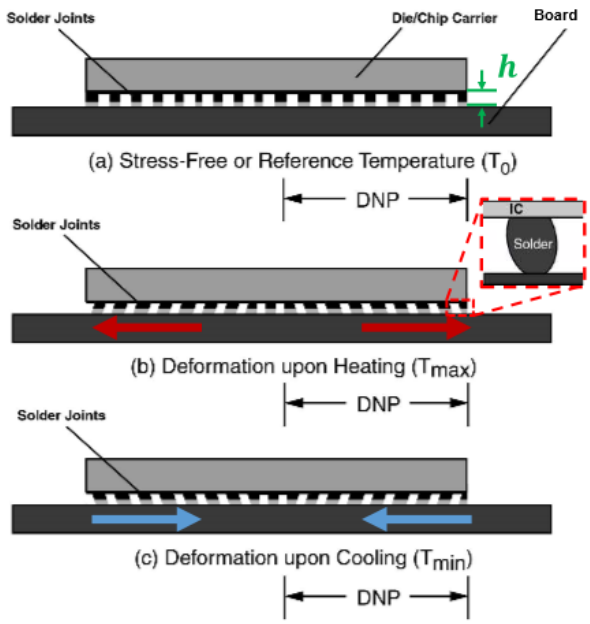


Fig. 3-3. Diagram used for approximating the shear strain placed on the outermost solder ball holding a semiconductor chip to a substrate.

Therefore, there is a lack of information regarding how bonds or an entire package respond to changes in the package design. This results in a two-fold problem. The first is that either experimental or simulation studies are required to study the effect of all design changes, which becomes significant as the number of design variations increases. Second, there is not an established understanding for how packages react due to component or encapsulant changes beyond bond fatigue metrics like ΔW_{avg} or shear strain range. For an example of studying factors besides bond fatigue metrics, [76] studies both the effect of encapsulation properties on the peel and shear stress on the interface between the encapsulant and the substrates. While the purpose of this work is not to correlate package deformation or another metric to ΔW_{avg}, it should be acknowledged that there is a lack of study regarding how package components respond to encapsulation properties in the way of stress reduction, warpage reduction, or by causing more

uniform warpage. Therefore, analysis of how the package responds to temperature cycling primarily focuses on the bonds themselves, both due to the bonds being the point of failure and the response of the surrounding structure not well studied. Therefore, metrics of study are either ΔW_{avg} of the entire bond or of a node in the bond within a high work region.

To summarize, encapsulants with a CTE like the package substates and higher E reduce the per-cycle fatigue in BGA packaging by reducing the bending and shear stresses placed on the bond while minimizing tensile stresses. While the package geometry and the materials involved vary between BGA designs and the PCB-Interposer, the concept of certain encapsulants reducing bond fatigue may apply. While the Internal bonds are connected to a pin instead of a substrate and the External bonds are not encapsulated, the concept of coupling the warpage of the DBC substrate, silicon die, and PCB could still be applicable. Therefore, identifying how critical bonds react to the encapsulant properties through parameter sweeps will determine if certain property combinations minimize per-cycle bond fatigue. Based on Table 1-6 in Section 1.6, the encapsulant CTE sweep is between 1 and 80 ppm/°C, and E sweep is between 17.5 MPa and 70 GPa. While not all these values are realistic for polymeric encapsulants, Chapter 4 will study realistic materials to provide ΔW_{avg} values for future experimental work.

However, the focus of these simulations must be on the bond that will fail first in the package. As mentioned in Section 2.7, a limitation of ΔW_{avg} is that it cannot compare across different bond materials. As there are sintered Ag bonds and solder bonds in the package, there will be a sintered Ag bond that will fail before all other sintered Ag bonds, and a solder bond that will fail before all other solder bonds. There is no way to conclusively determine which bond is the true first failure bond without experimental work, but arguments can be made for which bond is most important. After establishing the first failure bond in each group, parameter sweeps can be run on that bond to determine the relationship between that bond's ΔW_{avg} and the encapsulant properties.

3.3 Simulation Methodology

The objective of this section is to summarize the relevant simulation settings and the methodology. If more detail on the simulation setup is desired, see Chapter 2.

A half model of the PCB-Interposer package undergoes temperature cycling using a Static Structural simulation inside ANSYS Workbench 2021R2. To fix the package in place and prevent it from expanding into the space occupied by the missing half of the package, the package's cut plane has both a frictionless support and fixed support applied to it. The temperature cycling is applied using a Thermal Condition that follows the parameters in Table 3-1. Four is the minimum number of temperature cycles that demonstrates ΔW_{avg} convergence for all bonds evaluated, which is defined as a 5 % or smaller difference between the third and fourth cycle ΔW_{avg}.

The most relevant simulation assumptions are the material models used for the PCB and encapsulants. The PCB is modeled as isotropic and temperature-independent elastic, with a more realistic model being that it is orthotropic and has temperature-dependent properties. Generally, heating a polymer will raise its CTE and lower its E. This simplification underestimates the true value of ΔW_{avg} by reducing the CTE mismatch. However, it is adequate for an initial study examining the relationship between encapsulant properties and the per-cycle fatigue on the bonds.

Similarly, the encapsulant is modeled as isotropic and temperature-independent elastic, with a more accurate model being temperature-dependent viscoelastic. Due to complexity of determining and modeling viscoelastic behavior, a compromise is to model the polymer as temperature-dependent elastic. Like the PCB assumption, this assumption underestimates ΔW_{avg} by underestimating the encapsulant CTE and overestimating the stiffness. Like the previous assumption, it is adequate for an initial study examining the relationship between encapsulant properties and the per-cycle fatigue on the bonds.

For each bond studied, ΔW_{avg} from the fourth cycle is compared against the other bonds within the bond group to identify the first failure bond. The two bond groups are the sintered Ag bonds (Internal Bonds and Die Attach Comparable region) and the Sn60Pb40 bonds (External Bonds). The Internal bond or die attach corner with the largest ΔW_{avg} is the sintered Ag bond expected to crack first, so efforts to reduce the fatigue will focus on that specific bond. The same concept applies to the External solder bonds. A diagram of those bonds is in Fig. 3-4, while the exact bonds and geometry are in Fig. 2-27.

The methodology for Chapter 3 is as follows. First, to identify which bonds are expected to fail first in their material group, the ΔW_{avg} of the bonds closest and furthest from the package center are calculated using one soft and two rigid polymeric encapsulants. This quickly identifies which bonds are most vulnerable to focus our analysis. Once the important bonds are identified, parameter sweeps that vary the elastic modulus and CTE of the encapsulant are performed to identify the relationship between the properties and the bond's ΔW_{avg}. We can identify what encapsulants minimize ΔW_{avg} and why they are most optimal. Further study focuses on why using certain encapsulants changes the stress, strain, and deformation in the package.

Table 3-1. The Temperature Cycle Parameters in Accordance with JEDEC Standards [24].

Parameter	Value
Range	-40 °C to 125 °C
Ramp Rate	5 °C/minute
Dwell Time	10 minutes
Cycles to Convergence	4 Cycles
Stress-Free Temperature	25 °C

Table 3-2. Encapsulant Choices Used to Identify the First Failure Bonds.

Material	Elastic Modulus (GPa)	CTE (ppm/°C)
Silicone Gel	0.0175	80
ME-531	6	21
EP-2000	17.5	14.9

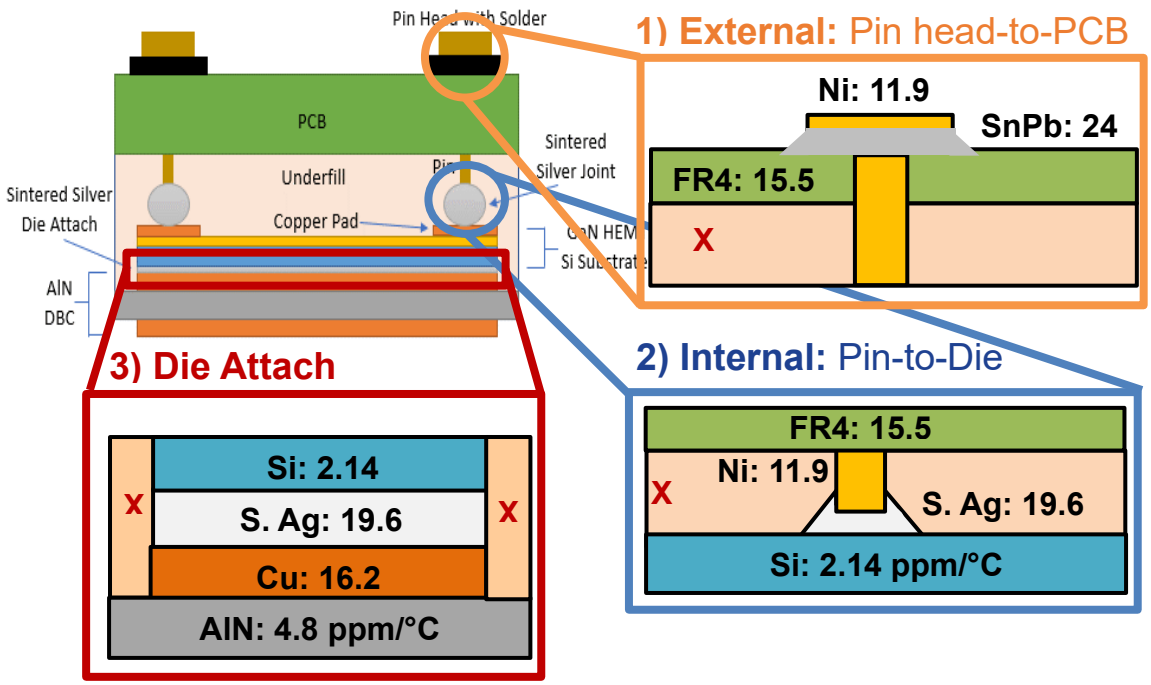
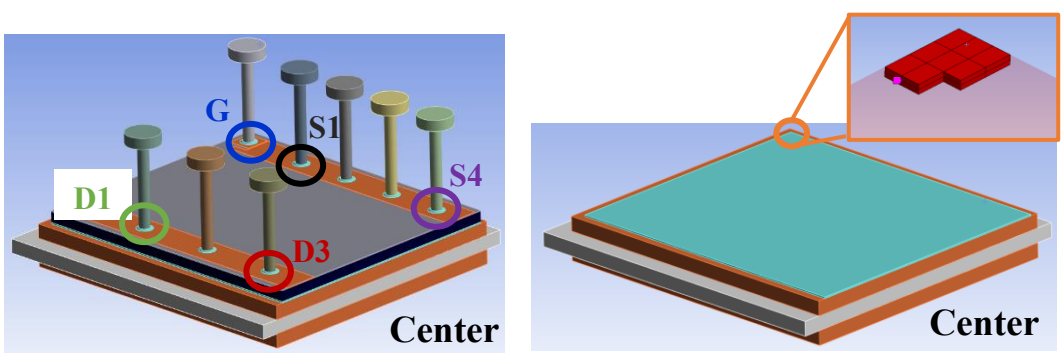


Fig. 3-4. Diagrams of all three bond regions, and with the CTE of each component listed. Solder is used for the External Bonds, while sintered Ag is used for the Internal Bonds and the Die Attach.

3.4 The First Sintered Silver Bond to Fail

The objective of this section is to establish that the sintered Ag bond expected to fail first in all scenarios is the Internal Gate bond. First, the ΔW_{avg} of all sintered Ag bonds with all encapsulants is compared, establishing that the Internal Gate has the highest ΔW_{avg} in all scenarios. As the Internal Gate is the bond furthest from the package center, this agrees with trends seen in BGA literature. The most optimal encapsulant to use has a CTE of 8 ppm/°C and the highest available elastic modulus. Using proper rigid encapsulation reduces the deflection of the gate pin during thermal cycling, which in turn minimizes two regions of high inelastic work on the Internal Gate bond.

As discussed in both Section 2.7, ΔW_{avg} can be compared between bonds if they are of the same material and have similar volumes. While both the die attach and Internal pin bonds are made of sintered Ag, the die attach volume is 906x larger than an Internal pin bond. To determine which sintered Ag bond fails first, the Internal bonds are compared against the Die Attach Comparable Region, which is a high stress corner of the die attach with the same volume as an Internal bond. Fig. 3-5 displays these bonds within the package. Fig. 3-4 displays a diagram of the region surrounding the bond.



(a) (b)

Fig. 3-5. A color-coded guide to the sintered Ag bonds. (a) The Internal pin bonds are the blue bonds at the base of the pins. The geometry can be viewed in Fig. 2-27. The bonds of interest are marked with "S" standing for Source and "D" standing for Drain. (b) The Die attach, with the Die Attach Comparable Region, which is on the Source side.

To identify the first failure bond within the group, three encapsulants are considered. These are a package with silicone gel, ME-531, and EP-2000. Their properties are in Table 3-2. The expectation is that using silicone gel results in a higher per-cycle fatigue than a rigid encapsulant like EP-2000, as it lacks the elastic modulus to either constrain or couple the thermal warpage of the package.

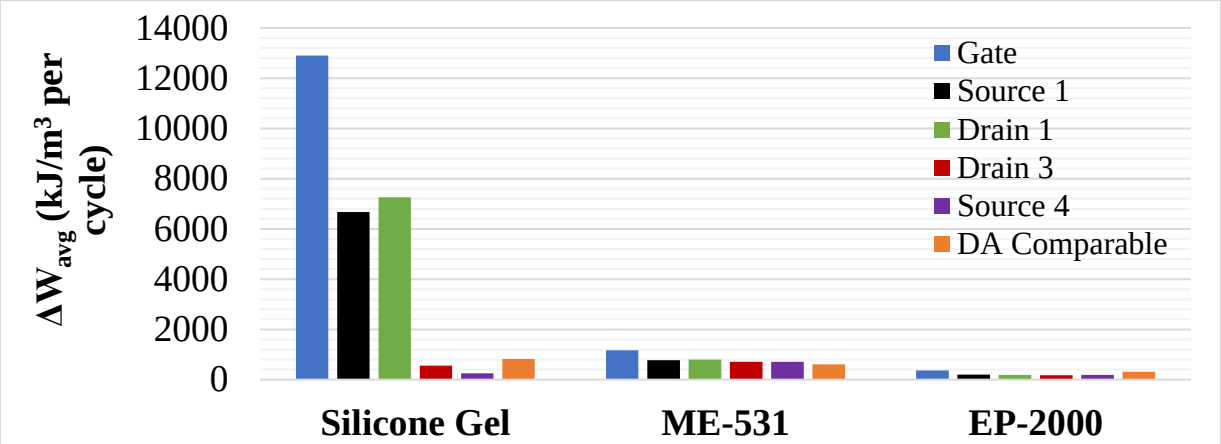


Fig. 3-6. The per-cycle fatigue of the Sintered Ag bonds for all three encapsulant scenarios. The Internal Gate has the highest fatigue in all scenarios. Compared to the Silicone Gel scenario, using ME-531 reduces the Internal Gate fatigue by 90.9 % while EP-2000 reduces it by 97.1 %.

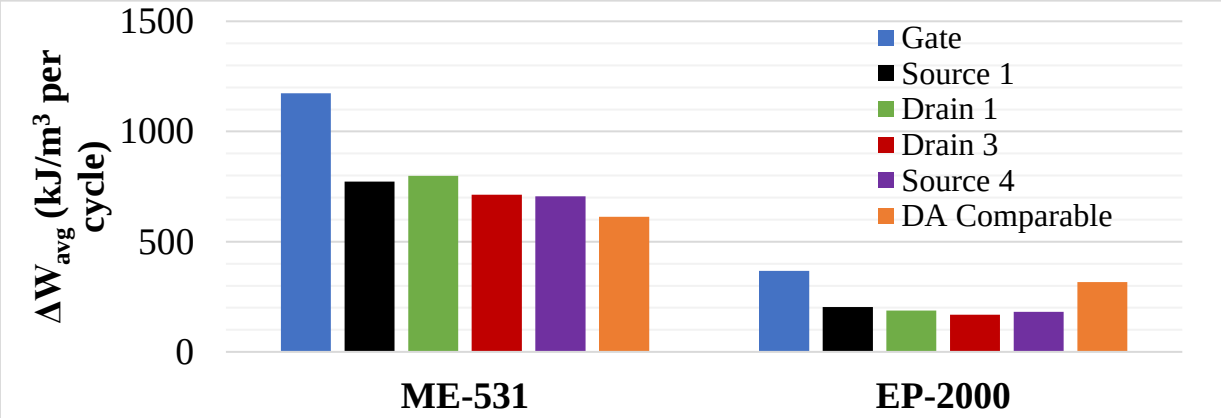


Fig. 3-7. The per-cycle fatigue from Fig. 3-6, but with the silicone gel scenario removed to show the difference between the two rigid encapsulants. Replacing ME-531 with EP-2000 reduces the Internal Gate ΔW_{avg} by 68.7 %.

The result of the three scenarios are in Fig. 3-6 and 3-7. In the three scenarios shown, the Internal Gate bond has the highest per-cycle fatigue and is therefore the sintered Ag bond

expected to fail first in the package. This also determines that the Internal Gate is expected to show crack initiation and propagation before the die attach.

Fig. 3-8 is the parameter sweep of the encapsulant CTE and *E* versus the Internal Gate bond's ΔW_{avg}. The first conclusion is that the Internal Gate ΔW_{avg} is the most sensitive bond in the package to the choice of encapsulation. While experimental work is required to determine the cycles to failure difference between using no encapsulant and a low CTE encapsulant, the magnitude by which ΔW_{avg} changes is not seen in any other bond in this package.

The second conclusion is the shape of the curves in Fig. 3-8. When sweeping the encapsulant CTE, a low elastic modulus like 0.0175 GPa results in a flat line, meaning that the bond is insensitive to changes in encapsulant CTE. As *E* increases, the flat line becomes more like a parabola that curves down as the CTE approaches the most optimal values. When the CTE is well-matched to the region surrounding the bond or is not the dominant factor, maximizing *E* pushes the line further down the graph. An example of this is in Fig. 3-16. In Fig. 3-8, increasing *E* at both matched and mismatched CTEs lowers Internal Gate ΔW_{avg}. This is due to the encapsulant restricting the gate pin deflection even at higher CTEs, which is discussed later in this section.

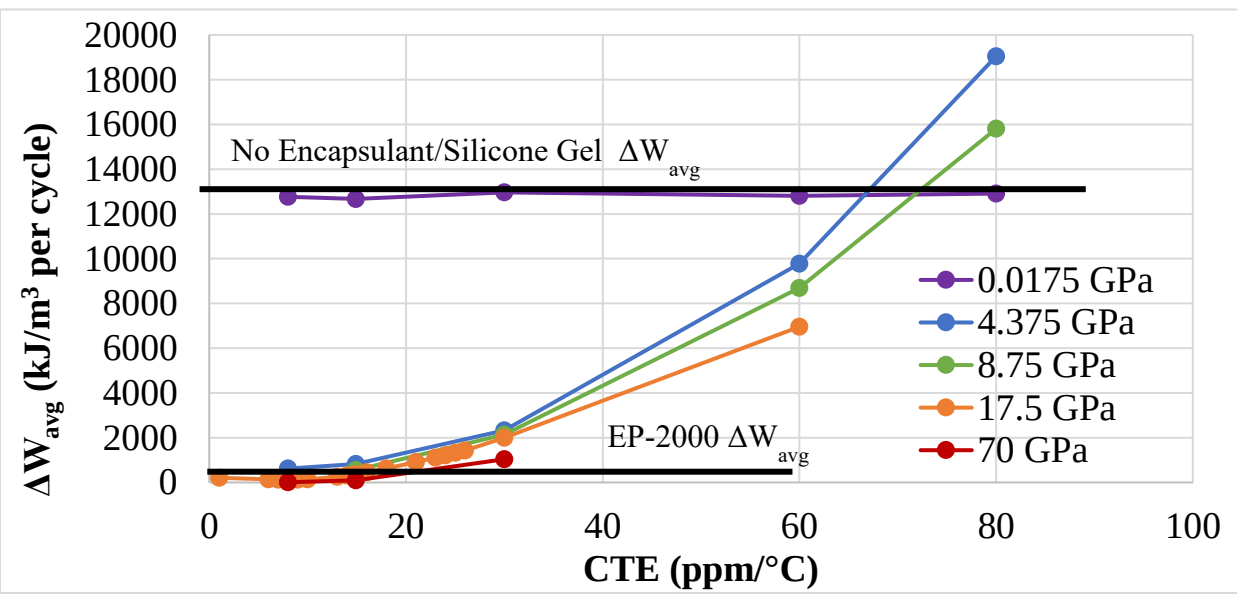


Fig. 3-8. The encapsulant parameter sweep versus the sintered Ag Internal Gate bond's ΔW_{avg}. The outcomes when using no encapsulant, soft encapsulant (silicone), and rigid encapsulant with low CTE mismatch (EP-2000) are marked. The local minima at 8 ppm/°C, and maximizing E reduces the Internal Gate ΔW_{avg} at CTEs ≤ 30 ppm/°C. For a close-up of the low CTE region, see Fig. 4-2.

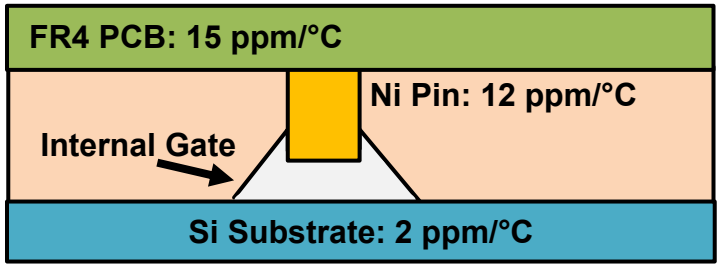


Fig. 3-9. A diagram of the Internal pin bond and the surrounding materials, including the material and CTE of the components.

The third conclusion is that using an encapsulant CTE of 8 ppm/°C results in the lowest ΔW_{avg} value when swept at a constant *E*, and increasing *E* further reduces ΔW_{avg}. The explanation for why 8 ppm/°C is the most optimal lies with Fig. 3-9, which is a diagram of the Internal Gate bond and the surrounding region. An encapsulant CTE of 8 ppm/°C is about midway between that of the PCB and Si substrates, representing a compromise between them. While the optimal CTE compromises between the Si and PCB, the primary cause of inelastic work on the Internal Gate is the gate pin due to the PCB warpage.

Fig. 3-10 looks at how the package deforms in response to heating and cooling, and how that alters the structure relative to the Internal Gate bond. While the warpage of the silicon die and DBC is not negligible, the primary concern is the effect of the PCB on the deflection of the gate pin. In both Fig. 3-10(a) and 3-10(b), the PCB pushes and pulls on the pin. This pin rocking generates two regions of high inelastic work, which can be seen in Fig. 3-11(b). Fig. 3-11 shows the inelastic work density contour plots of the Internal Gate bond, and Fig. 3-11(b) shows two "half-moon" regions generated by the rocking of the pin. Therefore, constraining the rocking of this pin will reduce Internal Gate ΔW_{avg}. This is why increasing the stiffness of encapsulants with a high CTE mismatch (80 ppm/°C) in Fig. 3-8 reduces ΔW_{avg} as opposed to increasing it, as increasing encapsulant stiffness constrains the pin deflection.

The use of CTE-matched rigid encapsulants both couples the thermal warpage of the structure, resulting in a more uniform bending not seen in Fig. 3-10(a) and 3-10(b), and reduces its magnitude. Looking at Fig. 3-10(c) and 3-10(d), the warpage is reduced for both the Si and PCB substrates. The gate pin not only warps in sync with the other two structures, but its magnitude of

deformation is reduced. For values on how the gate pin deformation reduces, see Fig. 3-22. While the pin still deflects, Fig. 3-11(c) and 3-11(d) show that the resulting inelastic work is reduced, which demonstrates how using these rigid encapsulants reduces the Internal Gate ΔW_{avg}.

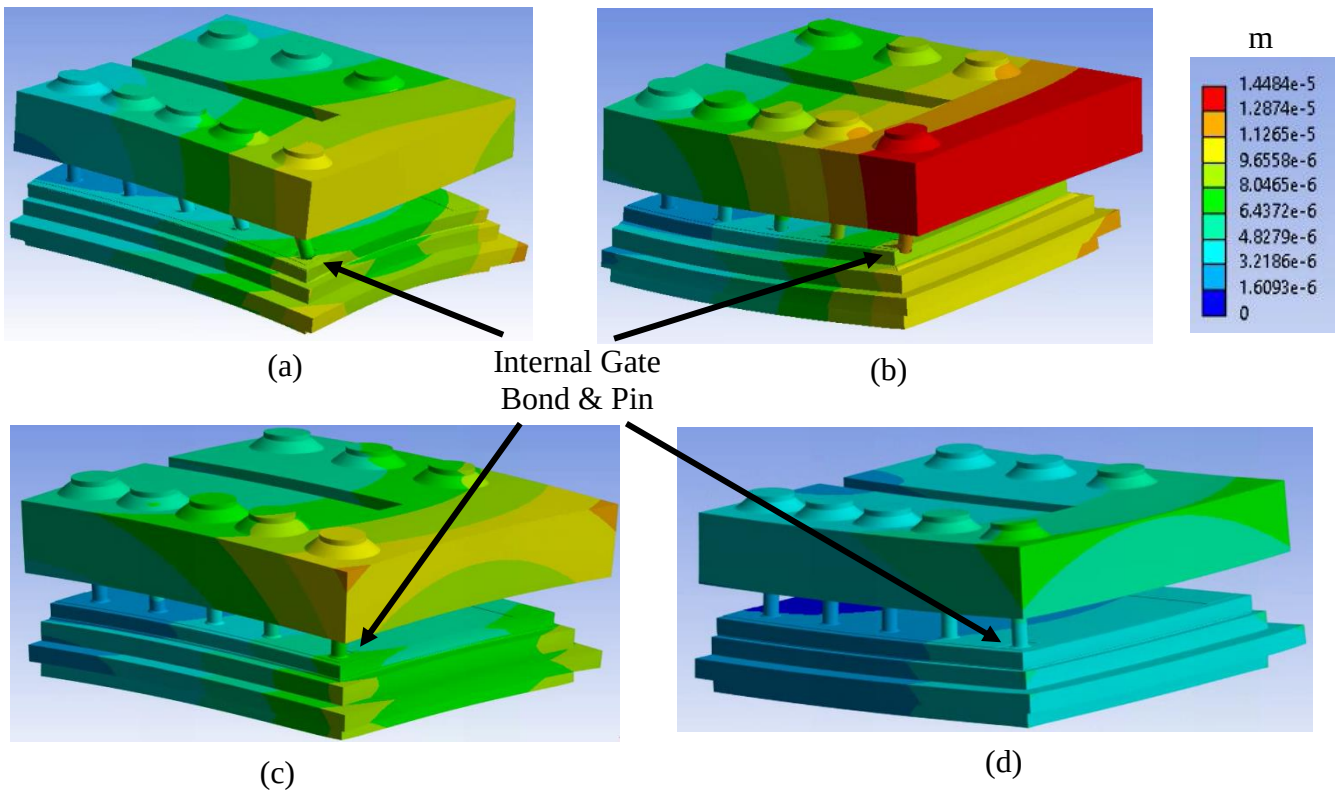


Fig. 3-10. Deformation contour plot of the PCB-Interposer package. All four images use the shown contour scale. The encapsulant is hidden to show the pins and Internal bonds. The deformation is exaggerated, causing the visual glitch that shows the gate pin disconnecting from the silicon die in the second image. (a) The deformation of the gate pin in the No Encapsulant/Silicone Gel scenario at the start of a cold dwell. The bending of the PCB pulls on the gate pin, causing it to "lift up" from the bond. While the perfect adhesion between all touching components prevents the pin from disconnecting from the gate bond, it does result in a region of high inelastic work on the Internal Gate bond. (b) The deformation of the gate pin in the No Encapsulant/Silicone Gel scenario at the start of a hot dwell. The gate pin is now bent in the opposite direction, causing the opposite edge of the pin to "lift off", generating a second region of high inelastic work on the Internal Gate bond. (c) The deformation of the gate pin in the EP-2000 scenario at the start of a cold dwell. The rigid encapsulant reduces the thermal warpage and couples the PCB and silicon substrate warpage. The result in that the PCB-induced pin deflection is reduced, which reduces the inelastic work on the Internal Gate bond. (d) The deformation of the gate pin in the EP-2000 scenario at the start of a hot dwell. Once again, warpage is both reduced and coupled, which reduces pin deflection, which reduces the inelastic work on the Internal Gate.

In BGA packaging, the bonds furthest from the undisturbed center of the package are subjected to the greatest shear stresses and strains due to thermal warpage, which causes them to fail first

[62], [75]. Shear strain is such a reliable metric of fatigue failure that older failure models such as Coffin-Manson use the shear strain range in their evaluation.

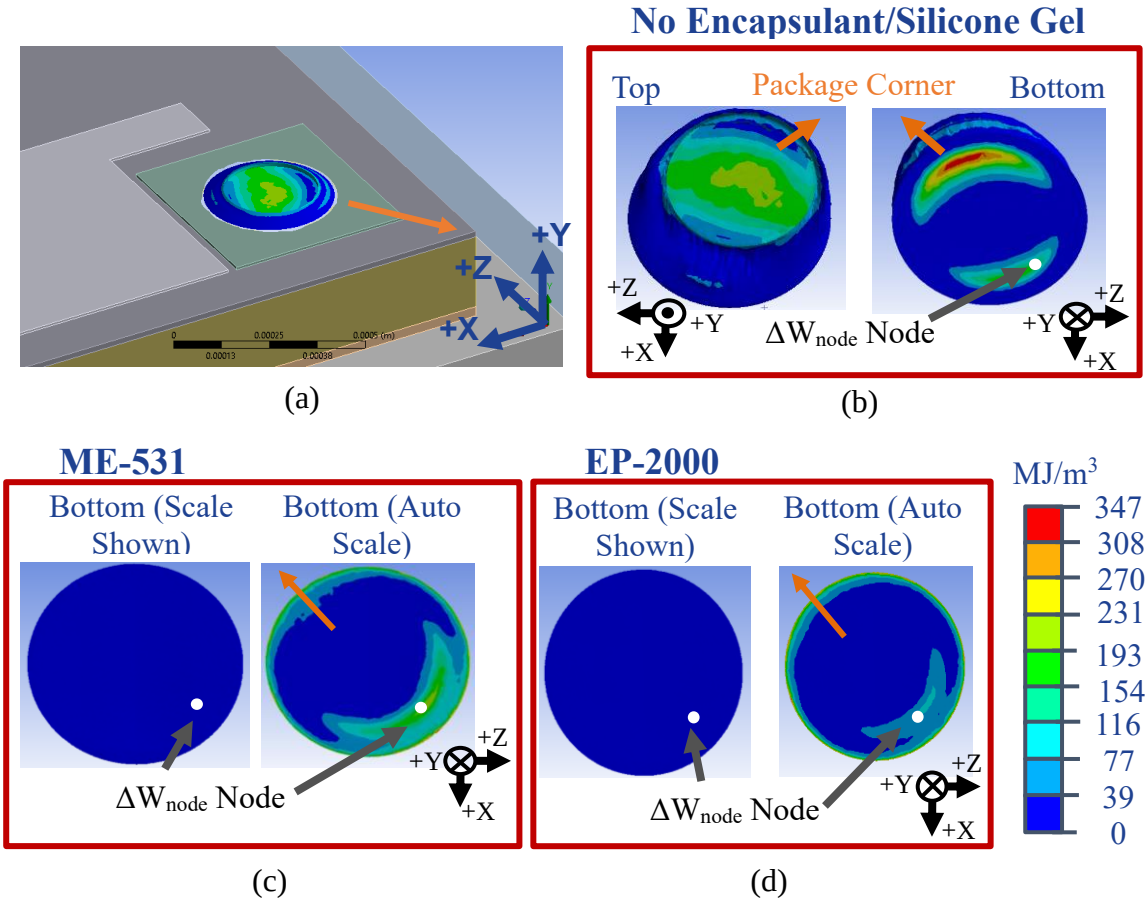


Fig. 3-11. The inelastic work density (NLPLWK) contour plots of the Internal Gate bond. This is also used to select the Internal Gate node. (a) The orientation of the gate bond, with the orange arrows pointing to the package corner. (b) The No Encapsulant/Silicone Gel scenario, which is what the contour scale is based on. As the pin bends towards and away from the package corner, it "lifts" off the gate bond, creating two regions of high work. The region that remains across all encapsulants has a node selected from it for ΔW_{node} analysis. (b) The ME-531 scenario, while the inelastic work is lower, an auto-scaled contour plot shows the high work region. (c) The EP-2000 scenario, which is like the ME-531 scenario.

While the PCB-Interposer structure and bonds are different from the BGA package, the first failure bond is the furthest from the package center. Therefore, it is prudent to determine if out-of-plane shear is a significant factor in causing the inelastic work on the Internal Gate.

In this work, the X and Z-axis define the horizontal plane, while the Y-axis is the vertical axis. Therefore, XZ shear is defined as in-plane shear. XZ shear are not discussed in this work, as their contributions to inelastic work are negligible in comparison to other shear and normal

components. XY and YZ shear elements are thus defined as out-of-plane (OoP) shear. Fig 3-12 provides an example of these axes. The following paragraphs explain how ΔW_{node} and the contributions of various stress/strain elements are calculated.

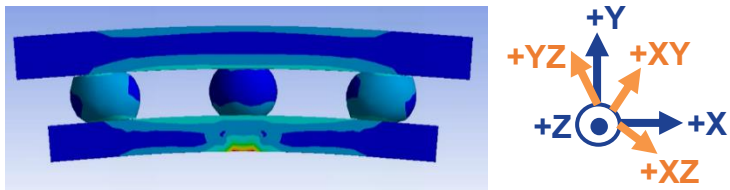


Fig. 3-12. The axis orientation used in this work. OoP shear refers to both XY and YZ shear and are within the plane of the paper like the X and Y axes. In-plane shear refers to XZ shear and is negligible. OoP normal force refers to the Y axis, while the in-plane normal forces are the X and Z axes.

To quantify the contribution of OoP shear to the total work performed on the Internal Gate, a node in a high-work region of the bond is selected. This node is the white dot in Fig. 3-11. The nodal stresses and inelastic strains in all axes are extracted to generate hysteresis loops, such as in Fig. 2-25. If τ_{xy} and γ_{xy}^{inel} represent the XY shear stress and inelastic strain placed on the node, then then the work performed by XY shear on the node over a temperature cycle ($\Delta W_{node,xy}$) is

$$\Delta W_{node,xy} = \int_{Cycle\ Start}^{Cycle\ End} \tau_{xy}\gamma_{xy}^{inel}. \tag{16}$$

Therefore, the total work performed on that node per cycle is

$$\Delta W_{node} = \Delta W_{node,x} + \Delta W_{node,y} + \Delta W_{node,z} + \Delta W_{node,xy} + \Delta W_{node,yz} + \Delta W_{node,xz}. \tag{17}$$

The contribution of OoP shear is

$$\Delta W_{node,OoP} = \Delta W_{node,xy} + \Delta W_{node,yz}. \tag{18}$$

By calculating the area inside of the hysteresis loops, the contribution of all normal and shear forces on the node can be determined. Therefore, both the total work on the node and the OoP shear contributions can be quantified for all scenarios.

To summarize the results of Table 3-3 and Fig. 3-13, 60 – 80 % of the total work performed on the node is from OoP shear in all scenarios, and 60 % of the total work reduction from

encapsulation is from a reduction in shear. Therefore, shear is both a primary cause of inelastic work on the Internal Gate bond, and using encapsulant reduces this shear. The use of encapsulant also reduces the inelastic work from the vertical axis, specially by reducing both the compressive inelastic strain and both the tensile and compressive stresses placed on the node.

To conclude Section 3.4, the Internal Gate bond is expected to be the first sintered Ag bond to fail under temperature cycling. The use of 8 ppm/°C, high *E* encapsulant reduce the bond's ΔW_{avg} by at least 90 %, which matches the principle in BGA encapsulation of using low CTE mismatch, high *E* encapsulants. This encapsulant reduces the per-cycle fatigue by coupling and constraining the thermal warpage of the Si and PCB substrate. While the PCB is not in contact with the Internal Gate bond, it can cause significant deflection of the gate pin, which in turn generates significant inelastic work on the bond. This inelastic work is primarily out-of-plane shear, which is the predominant factor in BGA ball failure. While the PCB-Interposer package is not a BGA structure, it also follows the principle low CTE mismatch, high *E* encapsulants reducing fatigue on the most vulnerable bonds.

Table 3-3. ΔWavg Analysis on the Internal Gate Bond Node

Scenario	ΔW_{node} **(kJ/m³ per cycle)**	$\Delta W_{node,\ OoP}$ **(kJ/m³ per cycle)**	**% Reduction from OoP Shear**	$\Delta W_{node,\ Y}$ **(kJ/m³ per cycle)**	**% Reduction from Y Normal**
None/ Silicone Gel	33,070.0	21,016.1		6108.99	
		63.6 % of ΔW_{node}		18.47 % of ΔW_{node}	
ME-531	6,348.0	5,051.2	**59.7 %**	641.33	**20.47 %**
	80.8 % ↓	79.6 % of ΔW_{node}		10.1 % of ΔW_{node}	
EP-2000	1,390.5	1,098.5	**62.9 %**	175.95	**18.47 %**
	95.8 % ↓	79.0 % of ΔW_{node}		12.7 % of ΔW_{node}	

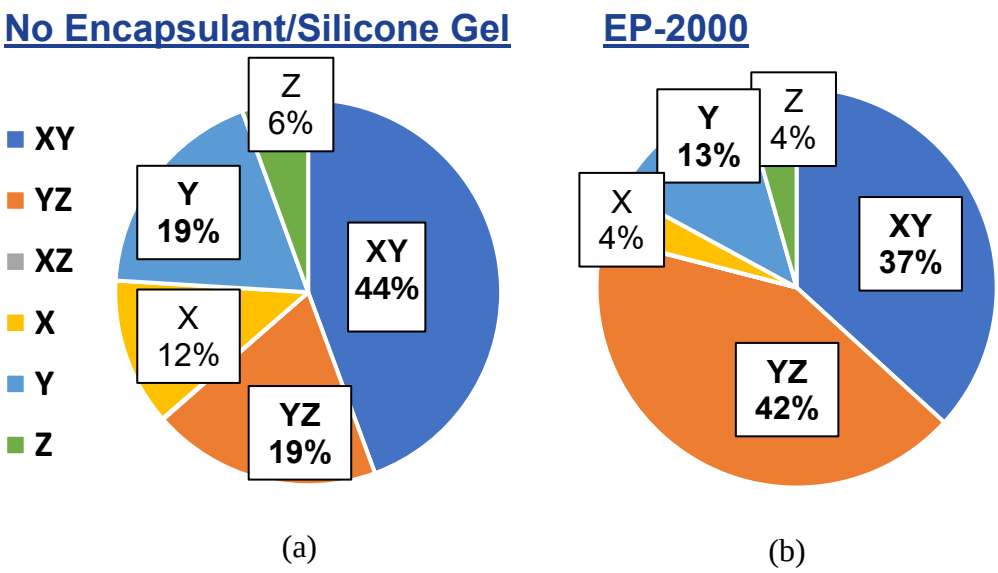


Fig. 3-13. Contributions of each stress/strain element to the Internal Gate ΔW_{node}. In both scenarios, the primary causes are out-of-plane (XY and YZ) shear and Y normal. (a) The contributions in the No Encapsulant/Silicone Gel scenario. (b) The contributions in the EP-2000 scenario.

3.5 The First Solder Bond to Fail

The purpose of this section is to establish that the Sn60Pb40 bond with the highest per-cycle fatigue is the External Source 4 bond, and that using a 24 ppm/°C encapsulant with highest possible elastic modulus minimizes ΔW_{avg}. However, the location of the first failure bond relative to the other External bonds is the opposite of BGA expectations, which is that the most external bond subjected to a CTE mismatch fails first. The hypothesis for why this occurs is that the minimal deflection of the Source 4 pin results in mismatched thermal warpage, which in turn generates high stress regions that fatigue the External Source 4 bond.

As discussed in Section 2.7, ΔW_{avg} can be compared between bonds if they are of the same material and have similar volumes. Also discussed in Section 2.7, only the External bonds use solder. Fig. 3-14 displays the bonds, while Fig. 3-4 shows a diagram of the bonds and Fig. 2-27 shows the bond geometry.

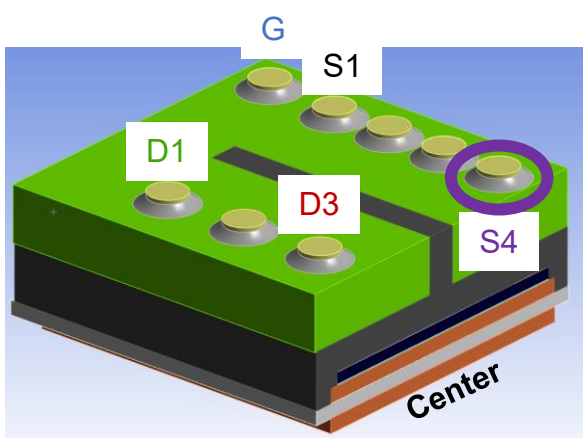


Fig. 3-14. A color-coded guide to the External pin bonds. The External pin bonds are the orange rings at the top of the pins. The bonds for which ΔW_{avg} is measured are marked, with "S" standing for Source and "D" standing for Drain. All External bonds are made with solder. The green body is the PCB, the yellow-brown bodies are the pin, the grey bodies are the solder, and the dark grey body is the encapsulant.

To identify the first failure bond within the group, three encapsulants are considered. These are a package with silicone gel, ME-531, and EP-2000. Their properties are in Table 3-2. The purposes of studying the bond ΔW_{avg} in these scenarios is to establish which External solder bond is likely to crack first, and to record ΔW_{avg} for future experiments. Once the first failure bond is established, the encapsulant parameter sweep can then be executed for that bond.

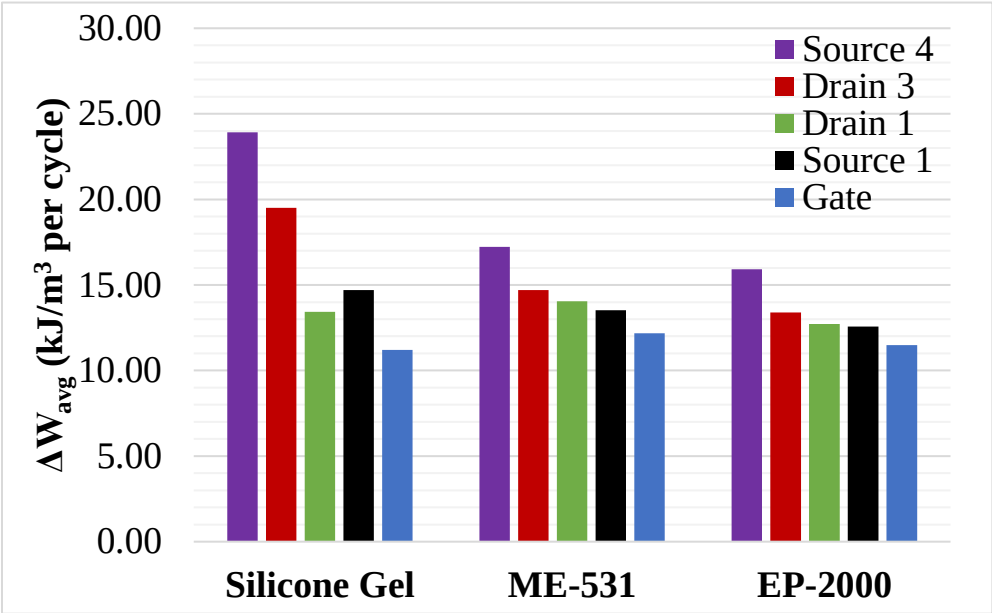


Fig. 3-15. The per-cycle fatigue of the external solder bonds examined for all three scenarios. The External Source 4 has the highest fatigue in all scenarios. Compared to the No Underfill scenario, using ME-531 reduces the Source 4 fatigue by 28.0 %, while EP-2000 reduces it by 33.4 %.

The results of the three scenarios are in Fig. 3-15. Regarding the first question, the External Source 4 bond has the largest ΔW_{avg} in all three scenarios. However, the difference between Source 4 and Drain 3 is 2.5 – 4 kJ/m^3 per cycle, which is smaller than the differences between the sintered Ag bonds. Whether this magnitude is relevant requires experimental testing, but it may mean that manufacturing variables like shape and flaws could alter the first failure bond.

The bonds closest to the center of the package experience the highest ΔW_{avg}, which is opposite of what is expected in the BGA packaging and shown in Section 3.4. The order of highest to lowest bond fatigue is the same as the order of bonds closest to furthest from the package cut plane along the X-axis, removing the possibility of an errant data point. While identifying why this pattern exists is not necessary for relating the encapsulant properties to the External Source 4 ΔW_{avg}, an analysis is included after the parameter sweep.

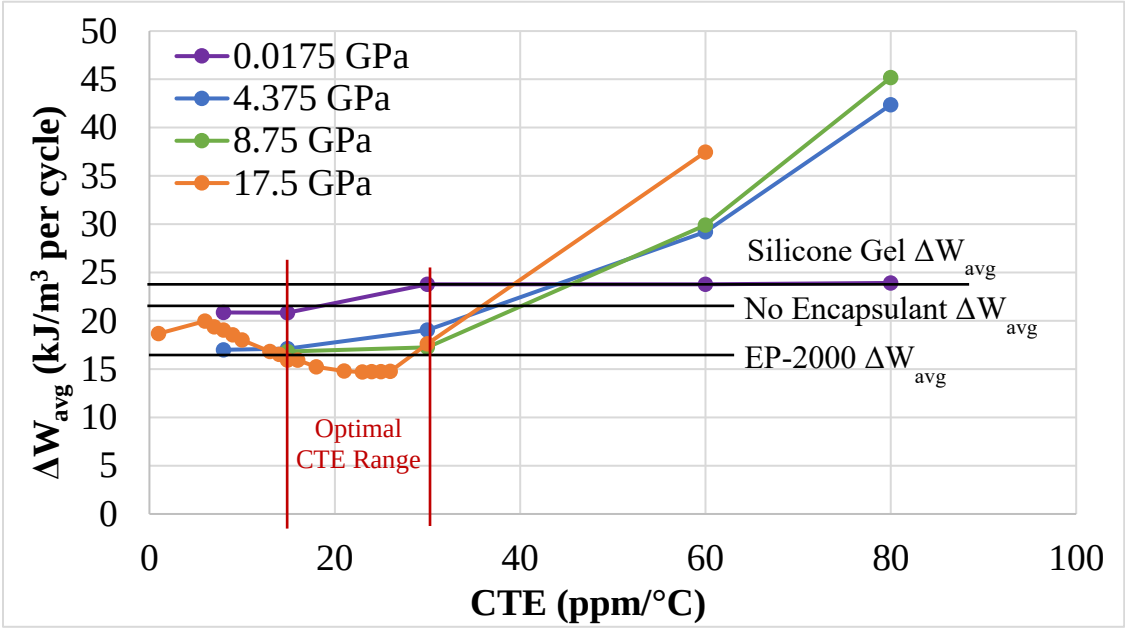


Fig. 3-16. CTE sweep at various values of E for the External Source 4 solder bond. The outcomes of using soft encapsulant (silicone), rigid encapsulant (EP-2000), and no encapsulant are marked. There are two local minima values, one at 24 ppm/°C and another between 1 – 6 ppm/°C. Maximizing E within the range of 15 -30 ppm/°C reduces ΔW_{avg}. The second minima was not explored as no commercial polymer encapsulant possess a CTE below 8 ppm/°C.

Fig. 3-16 is the parameter sweep of the encapsulant CTE and *E* versus the External Source 4 bond's ΔW_{avg}. The first conclusion is that, when compared to the Internal Gate or Die Attach, the magnitude of ΔW_{avg} and its range due to encapsulant changes is smaller. The reduced magnitude is because this bond is on the outside of the package and is thus subjected only the warpage of the pin and PCB, as opposed to multiple components each with their own mismatch. The reduced influence of the encapsulant is reasonable as the solder bonds are not encapsulated.

The second conclusion is that there are two optimal encapsulant combinations for minimizing the External Source 4 ΔW_{avg}. The first minima on the chart occurs at 24 ppm/°C, which is the CTE of the Sn60Pb40 solder. Maximizing *E* within between 15 and 30 ppm/°C also minimizes ΔW_{avg}, which agrees with the principle in BGA encapsulation that the encapsulant *E* should be maximized if there is a low encapsulant-to-package CTE mismatch. The second minima is located between 1 and 6 ppm/°C. As there are no polymers that exist with such a CTE, and the only materials that possess that low of a CTE are ceramics, this region was not explored.

To conclude the parameter sweep, the BGA concept of a low CTE mismatch, high *E* encapsulant reducing bond fatigue does apply to the External Source 4 bond. The conditions under which it applies for polymeric encapsulants are at CTE values like the solder. While another region may exist below 6 ppm/°C, experimental observation of this point requires a ceramic encapsulant, which is impractical.

The remainder of this section will explore why the bonds closest to the center of the package have the highest ΔW_{avg}, instead of the bonds furthest from the package center. The hypothesis is that the pins closest to the package center have minimal deflection from their original position during temperature cycling, resulting in high stress being placed on the solder bond and the PCB. The lack of pin deflection generates a high inelastic work region on the top of the External Source 4 bond, while the resulting high stress region in the PCB generates a high inelastic work region on the outer bottom ring of the External Source 4 bond.

The expectation of the furthest bond subjected to CTE mismatch is based on both the geometry and location of the bond in the package, as seen in Fig. 3-17. It is typically a spherical shape located between two warping substrates, while solder bond in the PCB-Interposer is a ring that holds the pin head to the PCB. This shape is in Fig. 1-7(b), 2-1 and 2-2. In the BGA packaging, the solder bond fatigue is due to both substrates warping, forcing the bond to inelastically deform. For the PCB-Interposer, it is the PCB that warps during temperature cycling, applying loads to both the pins and the solder bonds. The induced warpage on the pins by the PCB is most apparent on the Gate bond, which is in Fig. 3-10. With different bond geometry and package location, it is unknown if the assumptions applied to solder balls apply for this unique structure.

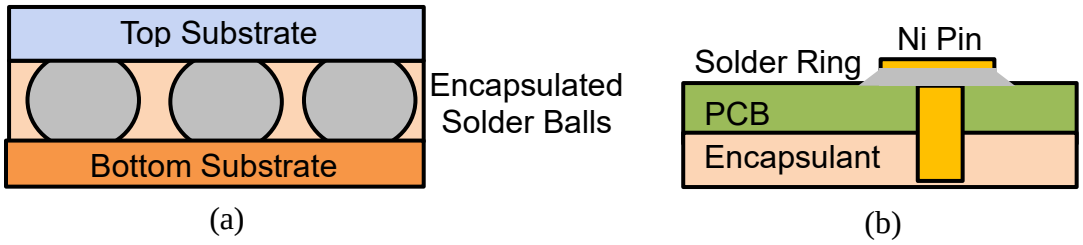


Fig. 3-17. The difference in geometry between the solder bonds. (a) In BGA packaging, the solder bonds are situated between two substrates. Thermal warpage of the substrates, which is most extreme at the edges of the package, causes failure. (b) The solder ring is not in between two substrates, rather it holds the pin head to the PCB. Of the two structures that the solder bond interacts with, the PCB undergoes the greatest warpage during cycling, applying loads to both the solder bonds and pins.

To identify why the External Source 4 solder bond has the highest ΔW_{avg}, the following section will compare it to the External Gate solder bond, as that is the most external solder bond and possesses the lowest ΔW_{avg}. The first step is looking at the inelastic work contour plots of the Source 4 and Gate solder bonds to identify what is causing the inelastic work. This analysis shows that the Source 4 bond has high work regions on its edges due to both solder-pinhead interactions and solder-PCB interactions, and that the intensity of these regions reduce when moving to the Gate bond. The hypothesis for this reduction is that the minimal deflection of the Source 4 pin generates the top region of inelastic work on the Source 4 bond, and a region of high stress in the PCB. This region of high stress impacts the solder-PCB interface, generating the other high inelastic work region on the Source 4 bond. The Gate bond has greater deflection and thus a more uniform warpage with the PCB, resulting in it having a lower ΔW_{avg}. The addition of encapsulant reduces the stress in the solder-PCB interface, which is why using a rigid encapsulant reduces the ΔW_{avg} on the External Source 4 bond.

Fig. 3-18 and Fig. 3-19 are the images of the Source 4 and Gate bonds in the No Encapsulant and EP-2000 encapsulant scenarios, respectively. Using silicone gel gives results like the No Encapsulant scenario and using ME-531 gives results like using EP-2000. The first major conclusion is how using EP-2000 reduces ΔW_{avg} on the Source 4 bond. Looking at Fig. 3-18(b) and 3-19(a), the inelastic work on the base edges of the Source 4 bond decreases in magnitude. Table 3-4 and Fig. 3-20 looks at the contributions of normal and shear forces at a node inside this region and shows that the primary force components causing that high work region are XY shear and X normal forces, and that using EP-2000 reduces these components.

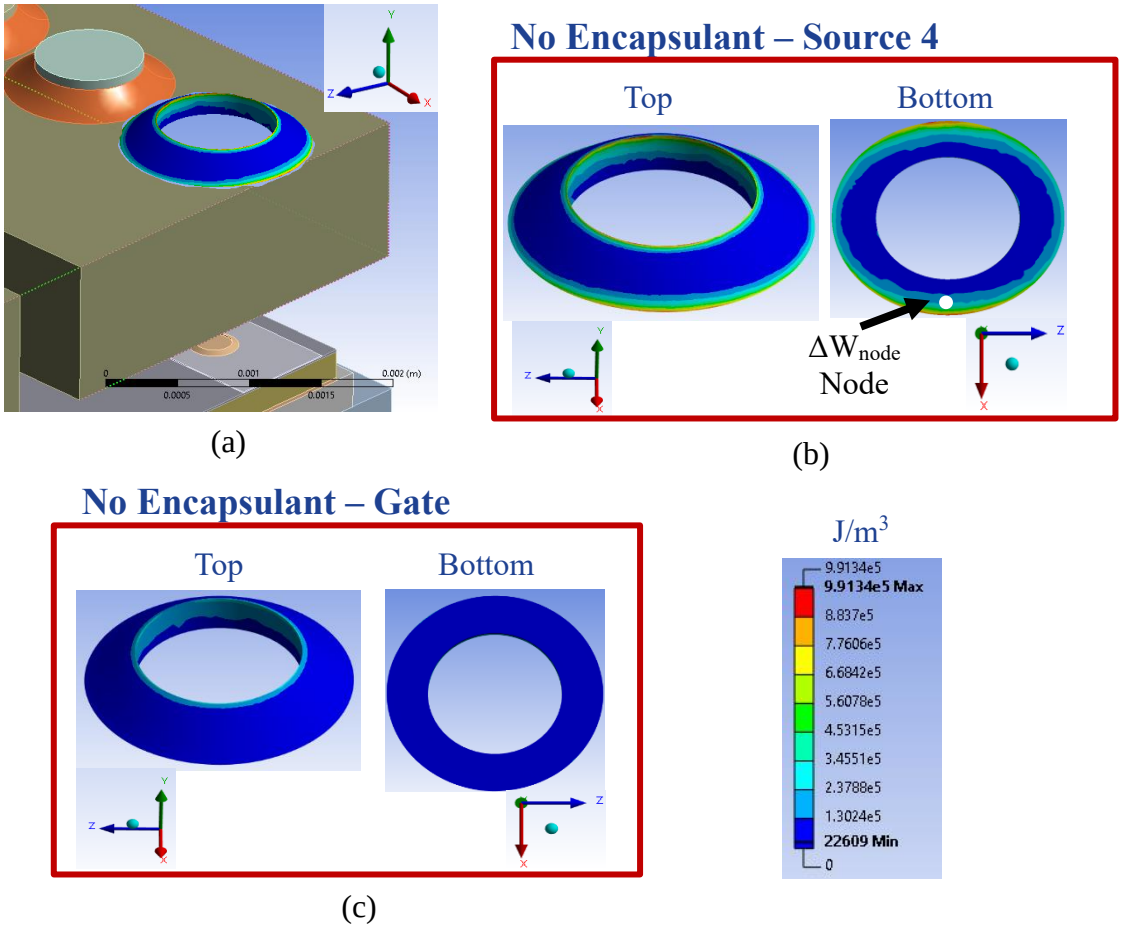
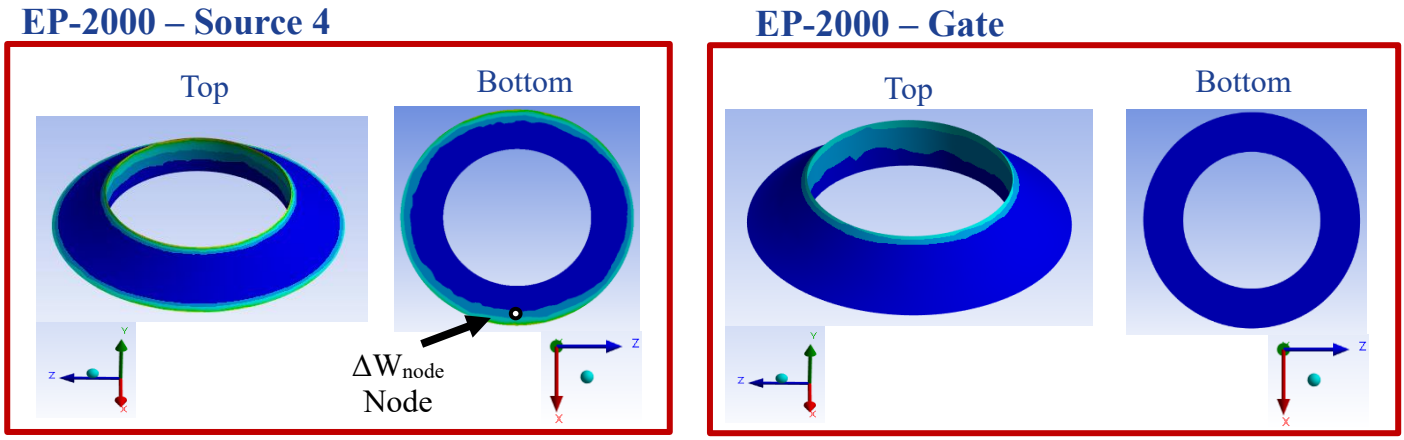


Fig. 3-18. Inelastic work contour plots of the External Source 4 and Gate solder bonds for the No Encapsulant scenario. All plots use the same scale pictured. (a) Location and orientation of the Source 4 bond. (b) The top and bottom of the Source 4 bond. The two regions of high inelastic work are the top and bottom edges of the bond, which are the solder-pinhead region and the solder-PCB region respectively. (c) When moving to the Gate bond, the bottom region is no longer visible with this contour scale, and the work in the top region is significantly reduced.



(a) (b)

Fig. 3-19. Inelastic work contour plots of the External Source 4 and Gate solder bonds for the EP-2000 encapsulant scenario. All plots use the same scale as in Fig. 3-18. (a) The top and bottom of the Source 4 bond. The two regions of high inelastic work are the top and bottom edges of the bond, which are the solder-pinhead region and the solder-PCB region respectively. Compared to the No Encapsulant scenario, the inelastic work in the solder-PCB region is reduced, which is how using encapsulant reduces ΔW_{avg} on the Source 4 bond. (B) When moving to the Gate bond, the bottom region is no longer visible with this contour scale, and the work in the top region is significantly reduced. As the Gate bonds have nearly identical ΔW_{avg} regardless of the encapsulant used, the gate looks similar in both figures.

Table 3-4. ΔW_{node} Analysis of External Source 4 Node.

Encapsulant	ΔW_{node} (kJ/m^3 per cycle)	$\Delta W_{node, XY}$ (kJ/m^3 per cycle)	% Reduction by XY Shear	$\Delta W_{node, X}$ (kJ/m^3 per cycle)	% Reduction from X Normal
No Encapsulant/ Silicone Gel	161.1	76.0		56.8	
		47.2 % of ΔW_{node}		35.2 % of ΔW_{node}	
ME-531	77.3 52.0 % ↓	30.2	**54.7 %**	24.4	**36.2 %**
		39.0 % of ΔW_{node}		31.6 % of ΔW_{node}	
EP-2000	74.9 53.5 % ↓	30.4	**52.9 %**	23.3	**37.8 %**
		40.6 % of ΔW_{node}		31.0 % of ΔW_{node}	

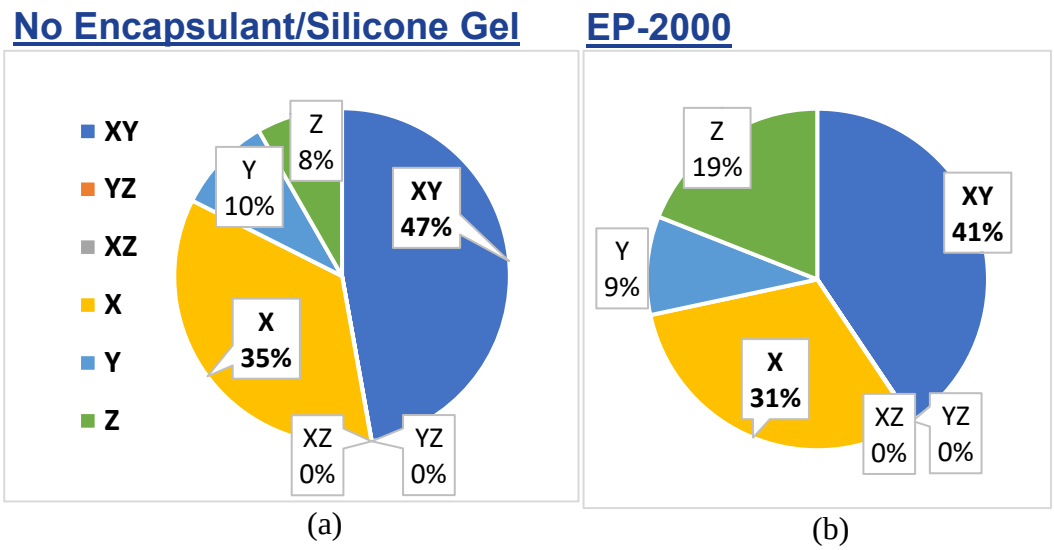


Fig. 3-20. Contributions of each stress/strain element to the External Source 4 ΔW_{node}. In both scenarios, the primary causes are XY shear and X normal. (a) The contributions in the No Encapsulant/Silicone Gel scenario. (b) The contributions in the EP-2000 scenario.

The second conclusion is that the Source 4 solder bond has higher ΔW_{avg} than the Gate because it has two regions of high inelastic work, one generated by the solder-pinhead interactions at the top of the bond, and another by the solder-PCB interactions at the base of the bond. Identifying why these regions occur will explain why the bonds closest to the package center are expected to fail first.

Regarding the pinhead-to-solder interaction point, Fig. 3-21 shows that the Source 4 pins in both encapsulation scenarios have a higher Von Mises stress than the Gate pins in the areas they are bonded to the solder bonds. The hypothesis for the difference is that the warpage of the Source 4 pin relative to the Source 4 bond and the PCB is mismatched, leading to stress concentrations that fatigue the Source 4 bond. Conversely, the thermal warpage of the Gate bond, the gate pin, and the PCB is more uniform, resulting in lower ΔW_{avg}. The difference in pin deflection/warpage is in Fig. 3-22.

The high stress region at the solder-PCB interface is studied in Fig. 3-23 and 3-24. In the EP-2000 encapsulant scenario in Fig. 3-23, the primary cause of the high stress region is the shear stress generated as the FR4 substrate attempts to warp while being constrained by the Source 4

pin. As seen in Fig. 3-18, the Source 4 pin does not significantly deflect during temperature cycling, which places significant stress on the PCB as they pull on one another. The combination of the PCB shear region becoming less intense with pins closer to the package edge (Fig. 3-23) coupled with the pin deflection increasing the closer the pin is to the package edge (Fig. 3-22) is likely correlated. As the pins closer to the package edge deflect more, the PCB-pin-solder warpage is more uniform, reducing the inelastic work on the bond. A comparable situation is observable in Fig. 3-24, but with greater stresses placed on either side of the solder bond along the X-axis. These are generated by the PCB bending. Regarding the concentration located on the cut plane, a full model would be needed to investigate if the frictionless support impacted these results. However, as the hypothesis is that the mismatched warpage of the PCB and the Source 4 pin is causing the Source 4 bond to have the highest ΔW_{avg}, this behavior is also be expected in a full model.

The conclusion is that the Source 4 bond has the highest ΔW_{avg} because of the Source 4 pin and PCB do not uniformly warp during temperature cycling, leading to high stress regions that fatigue the External Source 4 solder bond. While it is impossible to determine if the solder or sintered Ag bond is the true first point of failure based on simulations alone, the Internal Gate is subjected to a ΔW_{avg} at least twenty times greater than the External Gate. The amount of inelastic energy spent deforming the Internal Gate is greater, leading to the expectation that it will be the first location of failure.

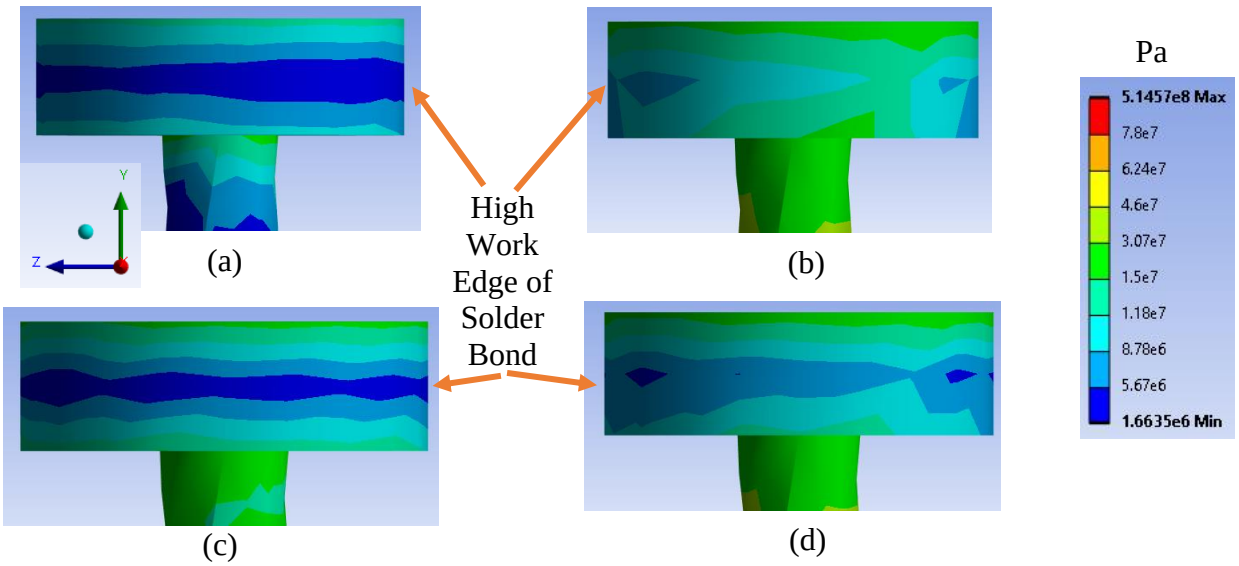


Fig. 3-21. The Von Mises stress on the Gate and Source 4 pins at the start of the hot dwell period. All contour plots have the same scale. (a) Gate pin in the No Encapsulant Scenario. (b) Source 4 pin in the No Encapsulant Scenario. (c) Gate pin in the EP-2000 scenario. (d) Source 4 pin in the EP-2000 scenario. In both encapsulant scenarios, the location where the high inelastic work solder edge is bonded to the pin has a much higher stress in the Source 4 pin versus the Gate pin.

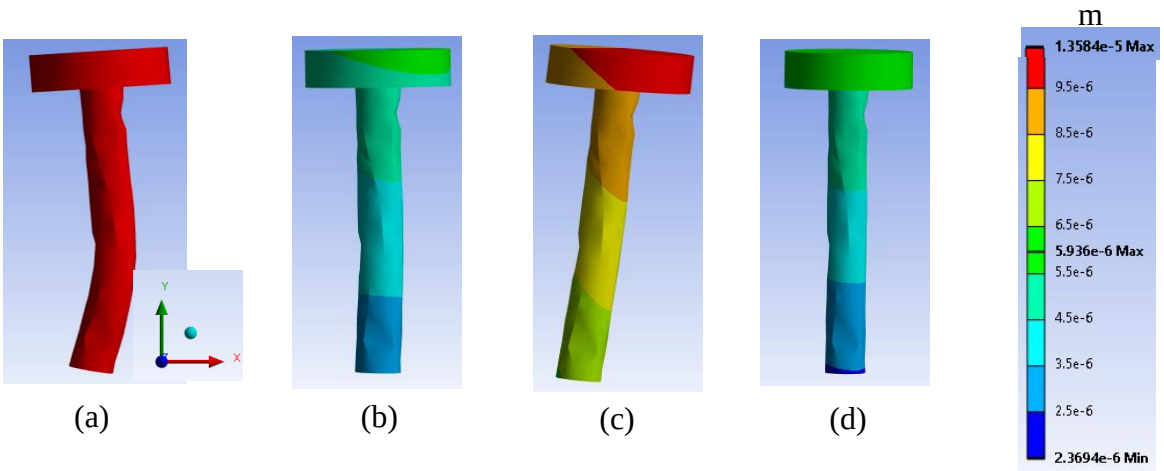


Fig. 3-22. The deformation of the Source 4 and Gate pins at the beginning of a hot dwell. All contour plots follow the same scale (a) The Gate pin in the No Encapsulant scenario. (b) The Source 4 pin in the No Encapsulant scenario. (c) The Gate pin in the EP-2000 encapsulant scenario. (d) The Source 4 pin in the EP-2000 encapsulant scenario. In both scenarios, the Gate pin deforms more than the Source 4 pin, which is believed to reduce stress on the solder bond and PCB.

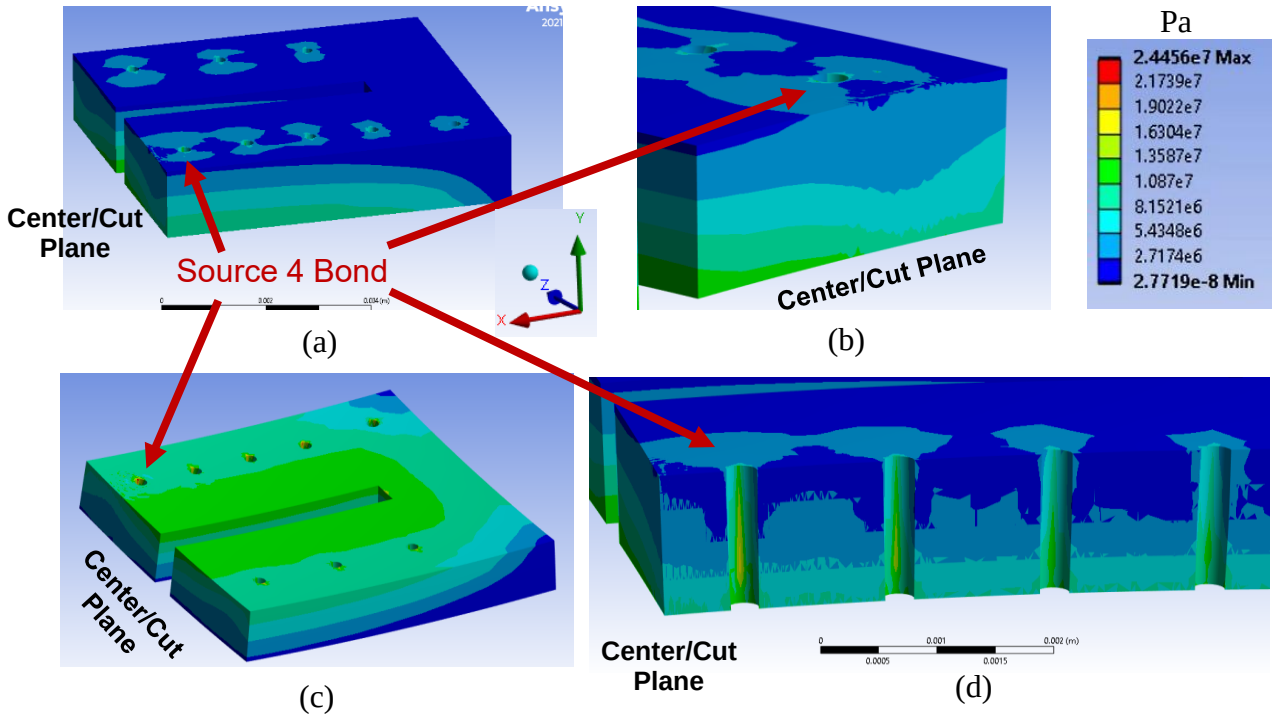
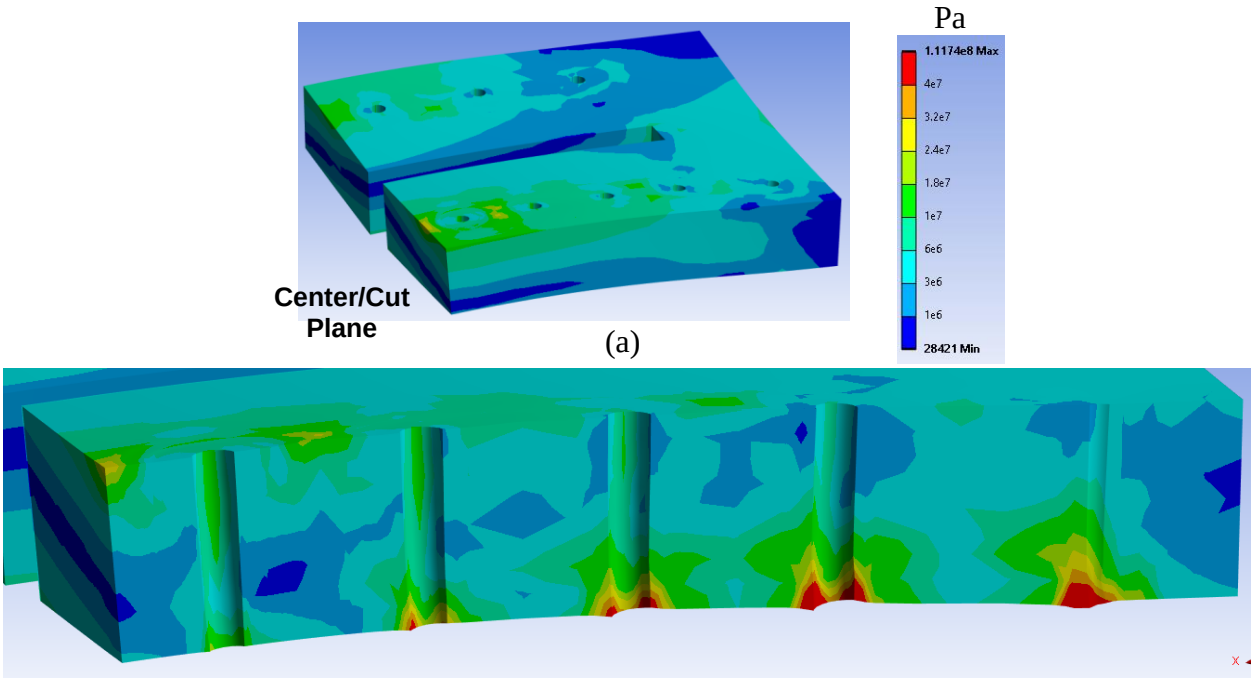


Fig. 3-23. Von Mises stress contour plot of the PCB using EP-2000 encapsulant at the beginning of a hot dwell. (a) Isometric view, with the center on the left and the package edge on the right. The high stress regions are located are the encapsulant interface, the interface with Ni pin, and under the External Source 4 bond. (b) The stress generated from the encapsulant-PCB interface results in a gradient that reaches the External Source 4 (c) Looking at the bottom of the PCB that is bonded to the encapsulant, the stress caused by the encapsulant interface is most prominent in the center of the package. (d) Cutting open the PCB to see the pin-to-PCB interface, the regions of high PCB stress are parallel to the X-axis, which is the axis that the PCB bends along. This high stress region is generated by shear stresses from the PCB attempting to expand along the X-axis while being restricted by the infinitely strong bond between it and the Source 4 pin. This region of high shear reduces in magnitude the further the pin is from the package center.



(a)

(b)

Fig. 3-24. Von Mises stress contour plot of the PCB in the No Encapsulant Scenario at the beginning of a cold dwell. (a) An isometric view. The Source 4 solder-PCB interface is teal to light green, while the area around this bond is green and yellow. Therefore, both the solder-PCB interface and the area around this interface are at higher stresses than almost the entirety of the bulk. (b) Looking at the PCB-pin interface, the high stress region generated by shear is also present and diminishes the further the pin is to the edge of the package. While not the focus, the high stress regions at the base of the pin channel are significant in the No Encapsulant scenario, which is an additional reason why this scenario is undesirable.

3.6 Die Attach Analysis

The objective of this section is to establish that the Source Edge is the likely region of crack initiation in the die attach, and that using a low CTE mismatch, high *E* encapsulant is optimal. EP-2000 is the existing encapsulant expected to perform most optimally, and it reduces the high work regions on the exterior edges of the die attach. While it is not an expected location of initial failure because the Die Attach Comparable Region has lower fatigue than the Internal Gate, this section is included if the Die Attach Comparable region is not valid.

As discussed in Section 2.7, ΔW_{avg} can be compared between bonds if they are of the same material and have similar volumes. In this bond group, only the Source and Drain corners regions can be compared, while the Die Attach Total is used to confirm general trends. The Die Attach Comparable region, which is the edge of the Source corner, is used in Section 3.4 to argue that the Internal Gate will crack before the die attach. Fig. 3-24 displays the bonds being studied, while Fig. 3-25 displays a diagram with the CTEs of the surrounding structure.

To identify the first failure bond within the group, three encapsulants are considered. These are a package with silicone gel, ME-531, and EP-2000. Their properties are in Table 3-2. The purposes of studying the bond ΔW_{avg} in these scenarios is to first establish which corner is more likely to crack first, and to record ΔW_{avg} for future experiments. Once the first failure bond is established, the encapsulant parameter sweep can then be executed for that region.

The results of the three scenarios are in Fig. 3-27. The Source Edge has the largest ΔW_{avg} in the three scenarios and is thus the more likely region of crack initiation. However, the difference in ΔW_{avg} between the two edges when using ME-531 and EP-200 is 4.3 % and 3.3 % respectively. Whether this magnitude is relevant requires experimental testing, but the failure corner may switch in experimental testing depending on manufacturing variables like the shape of the die attach or flaws.

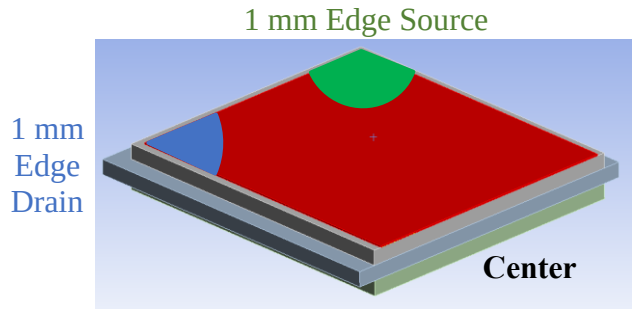


Fig. 3-25. A color-coded guide to the die attach. The edge regions have a 1 mm radius and occupy the far corners.

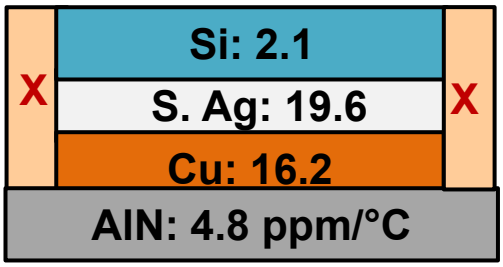


Fig. 3-26. The material layers and CTEs around the sintered Ag die attach.

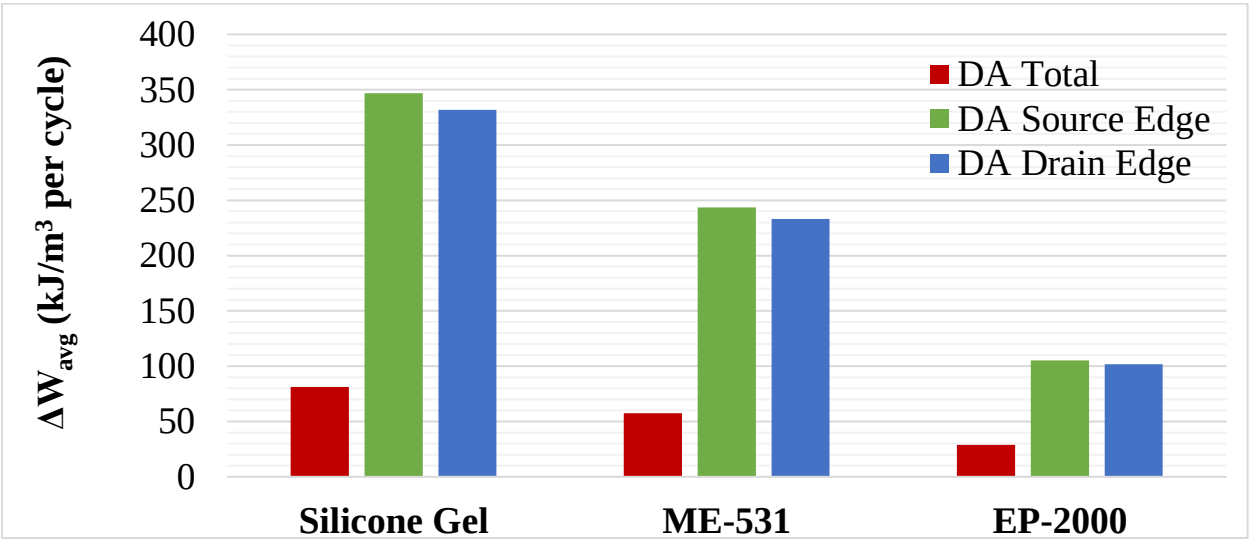


Fig. 3-27. The per-cycle fatigue of the die attach regions. The Source side has higher ΔW_{avg} than Drain side, so it is the region of interest. The Die Attach Total is included to show the total work placed on the body decreases. Compared to the Silicone Gel scenario, using ME-531 reduces the Source Edge fatigue by 29.8 %, while EP-2000 reduces it by 69.6 %.

This chart also states that using EP-2000 should result in the lowest per-cycle fatigue on the die attach. While experimental confirmation is required, this conclusion agrees with the premise of reducing fatigue using low CTE mismatch, high *E* encapsulants. EP-2000 has the lowest CTE mismatch with the various layers in Fig. 3-26. Fig. 3-28 expands on this with a parameter sweep showing how different encapsulants alter the per-cycle fatigue on the Die Attach Source 1 mm Edge.

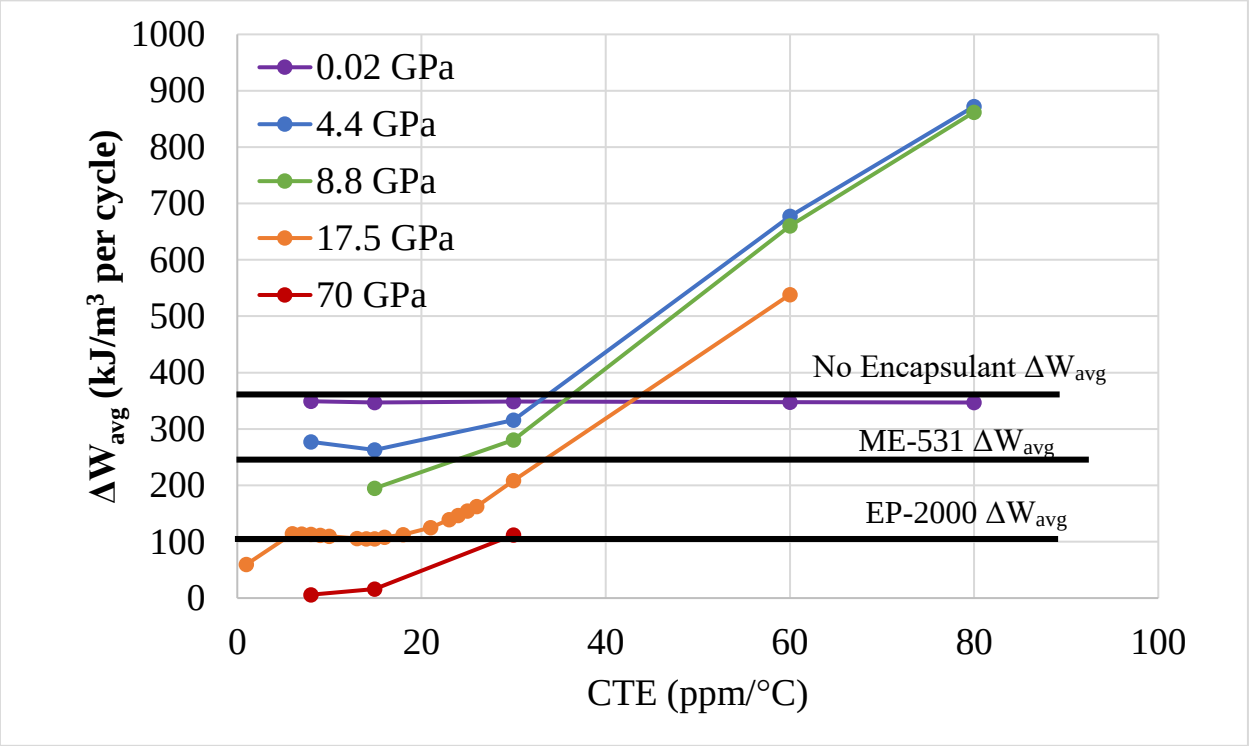


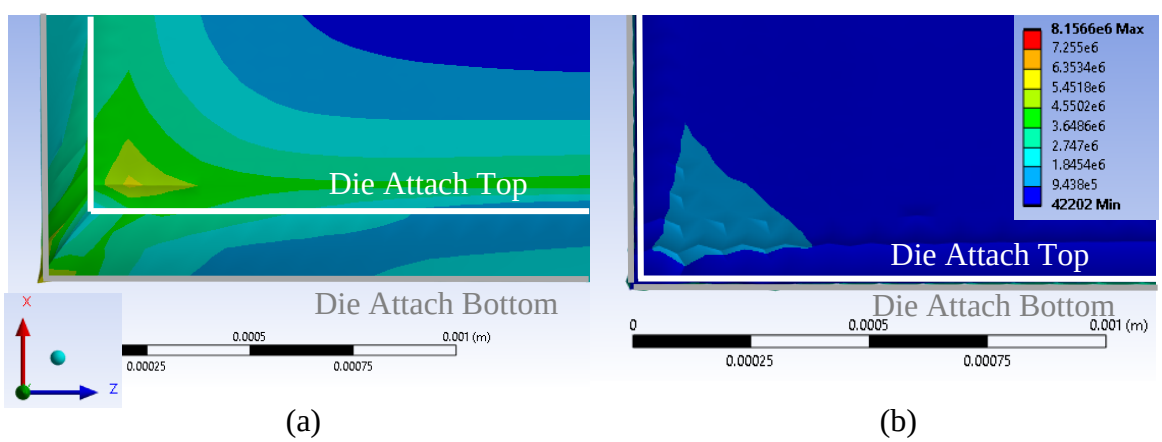
Fig. 3-28. CTE sweep at constant elastic modulus for the Die Attach Source 1 mm Edge. There are two local minima in the CTE sweep, the first at 15 ppm/°C, and the second around 1 ppm/°C. The 15 ppm/°C corresponds with the CTE of the Cu DBC layer bonded to the die attach, while the minima around 1 ppm/°C corresponds to the silicon die and AlN substrate. Using a silicone gel results in no improvement relative to the No Encapsulant scenario, as depicted by the 0.0175 GPa line in purple.

The major takeaways are that silicone gels have no impact on the die attach, and there are two optimal CTEs for the die attach that minimize fatigue. While silicone gels can have a CTE as high as 1000 ppm/°C, the controlling factor in this situation is its elastic modulus, which is approximated as 17.5 MPa in this sweep. At that low magnitude, the encapsulant is unable to restrict or couple the deformation of the various substates into a more uniform warpage, resulting in an outcome like using no encapsulant at all. Therefore, silicone gel is a sub-optimal choice if the goal is to reduce the per-cycle fatigue on the die attach.

The first optimal CTE is at 15 ppm/°C, which is like the Cu substate of the DBC. As seen in Fig. 3-29, the thermal warpage of the Cu substrate causes significant shear strain between the top and the bottom of the die attach layer, which generates the per-cycle fatigue. Using the EP-2000 encapsulant (CTE of 14.9 ppm/°C), removes this shear strain.

However, the more optimal CTE to match to is a value close to 1 ppm/°C, which is seen with the 17.5 GPa and 70 GPa sweeps. Not enough data points exist to identify the optimal CTE value, but it is between 2-5 ppm/°C as those are the CTE values of the silicon die and AlN substrates, respectively. However, as the lowest CTE observed in a commercial polymer is 8 ppm/°C, that region is currently inaccessible. Therefore, using the EP-2000 encapsulant is optimal, with a better encapsulant either having a higher elastic modulus, or a CTE < 6 ppm/°C.

Fig. 3-30 shows the total inelastic work contour plot for the die attach, and the nodes taken for ΔW_{node}. Using the encapsulant removes the high inelastic work regions on the edges of the die attach, which is from a reduction in the out-of-plane shear that generated these high work regions.



(a) (b)

Fig. 3-29. Non-linear inelastic work contour plot of the Die Attach Source 1 mm Edge in units of J/m^3, with both photos using the same scale and contour bar. We are looking at the top of the die attach, which is bonded to the silicon die. (a) The No Encapsulant/Silicone Gel scenario, which shows appreciable shear strain between the top and bottom of the die attach. (b) The EP-2000 scenario, which removes the shear strain.

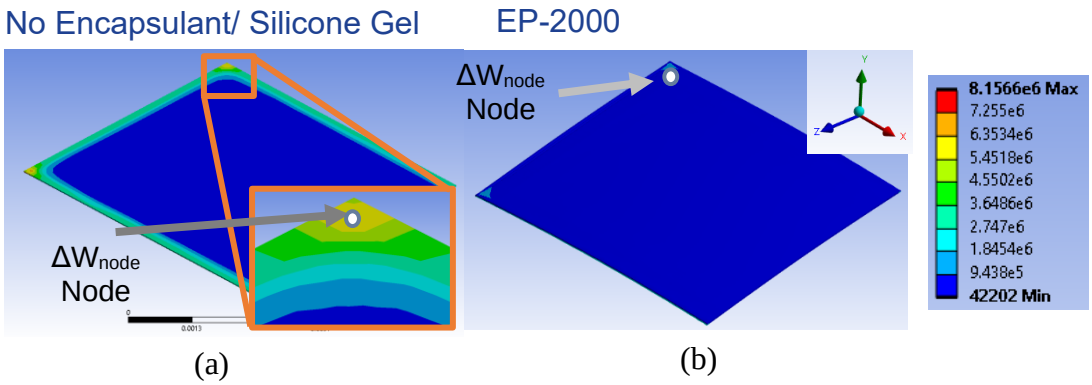
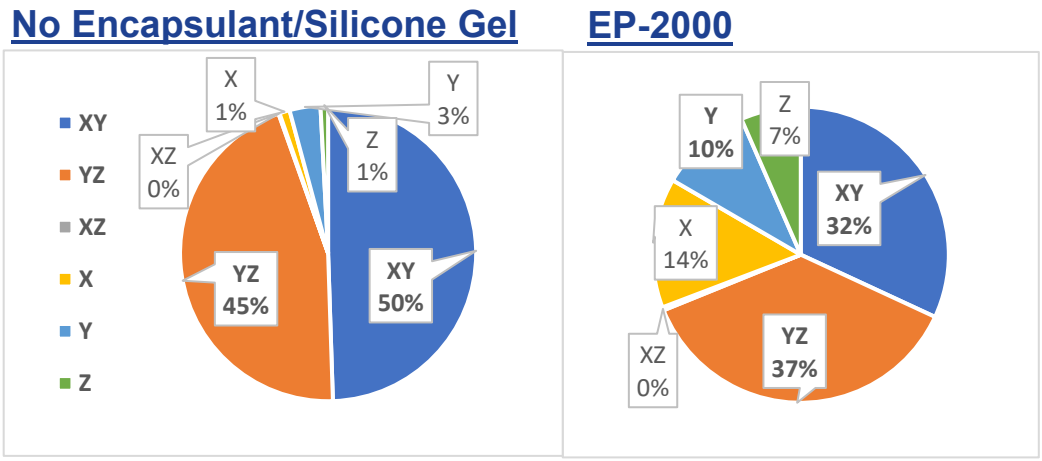


Fig. 3-30. The non-linear work contour plots for the die attach with units of J/m^3, with the Source 1 mm Edge being the back corner with ΔW_{node}. Both charts use the same contour range and scale. (a) The silicone gel scenario. (b) The EP-2000 scenario, using the rigid encapsulant removes the high work edges on the die attach.

Table 3-5 and Fig. 3-31 show what normal and shear forces contribute to ΔW_{node} in the node selected in Fig. 3-30. By using a rigid encapsulant, we reduce the magnitude of ΔW_{node} almost entirely by reducing the out-of-plane shear. This is the outcome expected from the reduction in shear deformation observable from Fig. 3-29.

Table 3-5. Reduction in ΔW_{node} and what Stress/Strain Elements are Responsible for the Reduction

Encapsulant	ΔW_{node} (kJ/m^3)	% Reduction from XY & YZ Shear
No Encapsulant/ Silicone Gel	1230.2	
ME-531	803.7 (34.7 % ↓)	100 %
EP-2000	351.0 (71.5 % ↓)	99.8 %



(a) (b)

Fig. 3-31. The contributions of each inelastic shear and normal element to the die attach ΔW_{node}. The primary sources of inelastic work are from the out-of-plane shear forces XY and YZ, which are responsible for the shear strain observed around the edges of the die attach. (a) The contributions in the No Encapsulant/Silicone Gel scenario. (b) The contributions in the EP-2000 scenario. The increased percentage of the non-shear components is due to a reduction in the shear, as opposed to an increase in their value.

3.7 Conclusions

The objective of Chapter 3 is to identify which bonds in the PCB-Interposer package will fail first and establish the relationship between encapsulant properties and those first failure bonds. The first step is to determine which bonds will fail first, as they have the highest ΔW_{avg} within their bond group. Three encapsulants are evaluated to identify the first failure bond in each group, and then a parameter sweep is executed to compare the encapsulant properties and the per-cycle fatigue. Optimal encapsulants to use for each bond are identified. Further study of this relationship includes looking at the inelastic work contour plots and the contributions of shear to the ΔW_{avg}.

The Internal Gate bond is determined to the be the first sintered Ag bond to fail, while the External Source 4 bond is the first solder bond to fail. Without experimental testing, it is impossible to conclude which of these two bonds will be the first bond that will fail in the package. However, there are two reasons why the sintered Ag Internal Gate bond is more important.

The first reason is the cost of failure. The loss of the Source 4 pin will degrade performance, but the loss of the Gate pin causes complete failure. The second reason is that the per-cycle fatigue placed on the Internal Gate is at minimum twenty-three times higher than the External Source 4 bond, which is shown in Fig. 3-32. While this is not conclusive proof that the Internal Gate fails first, a bond with smaller volume being exposed to a higher ΔW_{avg} that causes complete failure upon cracking is a reasonable location to protect until conclusive proof is obtained.

The behavior of the first failure bonds is also compared to literature trends. The Internal Gate bond is of similar shape and purpose to conventional bonds in literature, and correspondingly shares similar traits like the first failure bond being the furthest from the package center and OoP shear being a dominate cause of fatigue. The External Source 4 solder bond is unique in shape and purpose, and a comparable structure in literature does not exist. However, the lack of

deflection in the Source 4 pin relative to the more exterior pins explains why the central bonds have a higher ΔW_{avg} than the exterior bonds.

As all three encapsulant choices are possible experimental temperature cycling options, these outcomes can be verified with experimental work. This testing would also determine the cycles to package failure for each design, which in turn allows for empirical equations that can predict cycles to failure based on ΔW_{avg}. All values of ΔW_{avg} are in Appendix A.

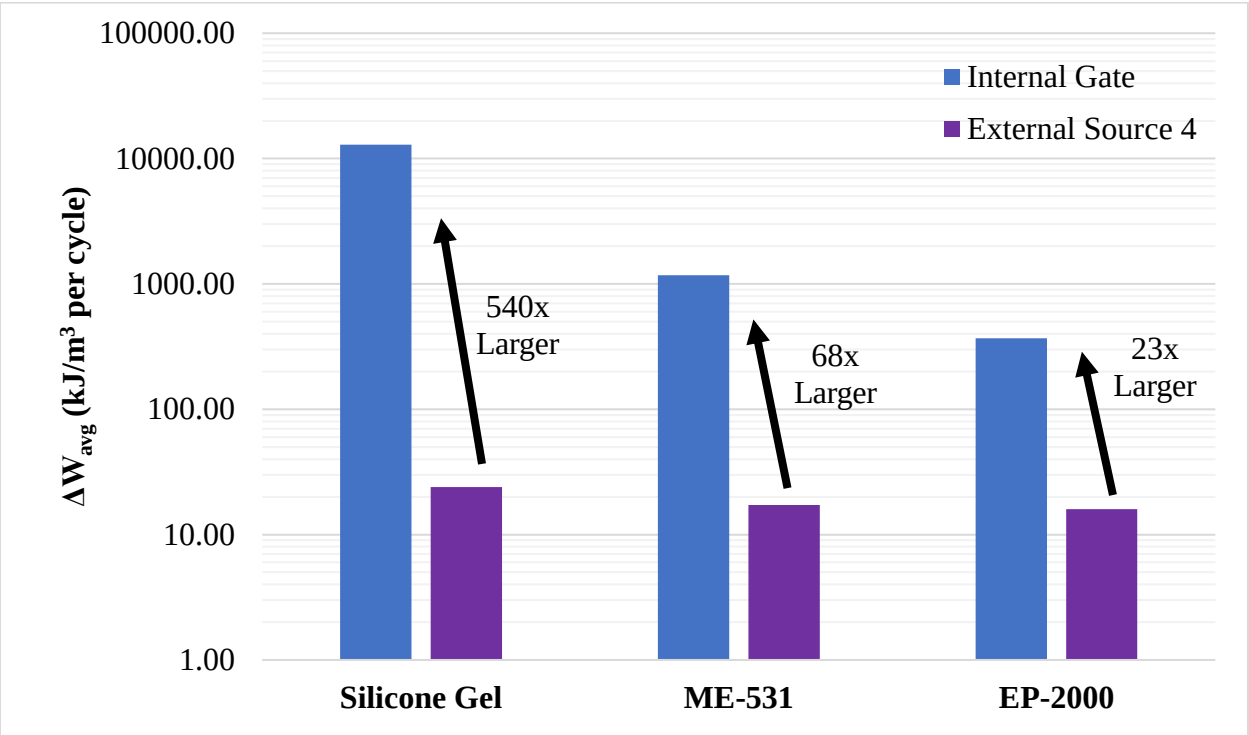


Fig. 3-32. Comparison of the per-cycle fatigue for the sintered Ag Internal Gate and the solder External Source 4 bond. In all scenarios, the Internal Gate volume is 40.6x smaller than the External Source 4, while higher a higher per-cycle fatigue. To conclusively determine which bond is the true location of initial failure, experimental work is required.

Chapter 4. Experimentally Available Encapsulants & the Internal Gate Bond

4.1 Purpose of Chapter 4

The objective of Chapter 4 is to establish the outcomes of the four encapsulant choices that will be used in future experimental temperature cycling. If the encapsulant properties are known, they can be simulated to calculate the first failure bond's ΔW_{avg}. The encapsulant that results in the highest number of cycles to failure in experimental work should have the lowest ΔW_{avg} on the first failure bond. Therefore, if all tested encapsulants have known material properties, it is possible to rank the relative lifetime of the package with each encapsulant, which can be verified by experimental temperature cycling. In conjunction with the parameter sweeps from Chapter 3, we can identify what the most optimal encapsulant on hand is and predict what materials will outperform our current encapsulants.

Section 4.2 discusses how to perform this abbreviated study of encapsulant properties, within the context of identifying how various real encapsulants will alter the Internal Gate in the PCB-Interposer. For package structures that are not as unique as the PCB-Interposer, there are expectations for what is the first failure bond and how various encapsulants will perform. If so, the Chapter 3 analysis may not be necessary, and a shortened study ranking the available encapsulant is sufficient. Experimental temperature cycling is the next step in this project, and based upon the knowledge we have from BGA packaging and Chapter 3, we can predict how our four encapsulant choices will perform relative to one another.

There are two categories of polymeric encapsulant. The first are soft encapsulants, with silicone gel being the most common example. Prized for their processability and flexibility, their low modulus provides a chemically inert, vibration dampening environment that applies minimal mechanical loads to the encapsulated components. While these gels have significant encapsulant-to-package CTE mismatch, their low E is expected to limit the Internal Gate fatigue to a value

comparable to the No Encapsulant scenario. The first of the three possible encapsulants, a silicone gel, is studied in Section 4.3.

The second category are rigid encapsulants. These structures have an *E* high enough to influence the package warpage, so proper CTE matching is necessary to ensure the encapsulant protects the bonds instead of harming them. Two rigid encapsulants, ME-531 and EP-2000, are studied in Section 4.4. Of the two rigid encapsulants, EP-2000 is predicted to have the greater number of thermal cycles to failure. As the best encapsulant on hand, we can establish what material properties a material must possess to improve on EP-2000. Once the improved properties are known, other materials can be evaluated as potential replacements.

Section 4.5 summarizes and concludes the chapter.

4.2 Practical Applications of Thermo-Mechanical Simulations

The purpose of Section 4.2 is to illustrate how to apply the simulation outcomes to experimental temperature cycling in the context of an abbreviated encapsulant study. After discussing specific encapsulants being studied and their expected outcomes, the methodology of the abbreviated study is discussed.

The purpose of Chapter 4 arises from the conclusions of Chapter 3. Chapter 3 identifies the Internal Gate as the expected first failure bond, and the most optimal encapsulant in this thermo-mechanical model has a CTE of 8 ppm/°C and the maximum possible *E*. While evidence of the first failure bond is needed, that study does not tell us if one existing encapsulant results in a greater number of cycles to failure than another. To be able to predict which encapsulants are better than one another, a simulation needs to be run with each individual encapsulant to calculate the Internal Gate's ΔW_{avg}. Like the logic of which bond within the bond group is expected to fail first, the realistic encapsulant with the lowest first failure ΔW_{avg} is expected to last the greatest number of cycles to failure. However, without experimental work to determine the number of temperature cycles to failure, we are limited to knowing that one encapsulant should last longer versus another, but not how much longer it may last.

Table 4-1. Common Encapsulant Properties According to ANSYS Granta.

Material	Classification	Elastic Modulus (GPa)	CTE (ppm/°C)
Silicone (No filler)	Soft Encapsulant	0.005 – 0.05	250 – 300
Silicone (VQM, 40 – 70 % Mineral Filler)	Soft Encapsulant	0.0075 – 0.018	150 – 165
Epoxy (No Filler)	Rigid Encapsulant	2.35 – 2.47	81 – 117
Epoxy (20 – 40 % Mineral Filler)	Rigid Encapsulant	8 – 12	24 – 26

Table 4-2. Encapsulants Expected to be Used in PCB-Interposer-on-DBC Temperature Cycling.

Encapsulant Used	Classification	Elastic Modulus (GPa)	CTE (ppm/°C)
No Encapsulant	None	N/A	N/A
Wacker SilGel 612	Soft Encapsulant	0.01	300
ME-531	Rigid Encapsulant	6	21
EP-2000	Rigid Encapsulant	17.5	14.9

Therefore, the purpose of Chapter 4 is to repeat the simulation with encapsulant properties that match those in encapsulants that are likely to be used in the future experimental work. Not only will having the ΔW_{avg} from each scenario allow for ranking, but it also allows experimental work to identify if Darveaux's Model applies. If it does, then future simulation work can predict what the experimental cycles to failure of the package are based on the value of ΔW_{avg}. For greater detail, see Section 2.6.

There are many available options for polymeric encapsulation. Table 4-1 summarizes reasonable material properties for these options, while Table 1-6 provides a list of commercial and academic materials. While Section 4.5 will study the possibility of using encapsulants that are not polymer matrices, the following discussion focuses specifically on polymeric encapsulants. The four encapsulation options expected to be used during the experimental temperature cycling are shown in Table 4-2.

The first option is using no encapsulant, which is suboptimal for reasons including thermo-mechanical. It is included to serve as a comparison for the second option, Wacker Silgel 612. While this silicone gel possesses a significant CTE mismatch with all package components, the outcome of using this gel is expected to be like the No Encapsulant scenario. As mentioned in Section 3.2 with Fig. 3-1, encapsulants with a low enough E will have no effect on the ΔW_{avg} of vulnerable bonds, as they lack the stiffness to either constrain or couple the package thermal warpage. Silgel 612 has an E similar to the silicone gel stand-in used in [70], so it is tested to determine if silicone gel behaves in a similar manner in this novel package.

The third and fourth encapsulant options, ME-531 and EP-2000, are rigid encapsulants. Commonly referred to as underfills when they only fill in the gaps between two substrates, these encapsulants typically possess an $E > 1$ GPa and a CTE < 100 ppm/°C. Generally, an encapsulant of at least 1 GPa should influence the package behavior. ME-531 and EP-2000 are particularly extreme examples of high E, low CTE materials, with EP-2000 having the second lowest CTE and second highest E of all polymeric materials studied.

The expected outcome of using either ME-531 or EP-2000 is a reduction in the Internal Gate ΔW_{avg}. While rigid encapsulants can increase bond fatigue if they have a CTE mismatch with the local package components, both encapsulants possess a CTE expected of a metal. Therefore, they are expected to be an improvement versus using no encapsulant or silicone gel.

Of the two encapsulants, EP-2000 is expected to have the lower Internal Gate ΔW_{avg}, but the magnitude of improvement is uncertain. The reason is it has a smaller CTE mismatch with all packaging components except for the bond material. While matching the bond material CTE may be optimal for certain bonds in specific package, matching the warping substrates is expected to have a more optimal outcome. Many BGA papers from the 1990s claim that the most optimal encapsulant has a CTE matched to the solder balls. However, the encapsulant with the lowest CTE evaluated was often like solder (24 ppm/°C), so it is uncertain if the 24 ppm/°C encapsulant was the most optimal encapsulant or just the best option available at that time. Regarding the elastic modulus, the general principle is to maximize E if the CTE is considered well-matched, so EP-2000 should also be superior in this regard.

With the knowledge of the most optimal encapsulant for the Internal Gate from Chapter 3, the fact that EP-2000 is more like the ideal encapsulant is also evidence that it will be superior. However, Chapter 4 is also meant to serve as a blueprint for a brief encapsulant investigation. This brief investigation consists of running as few simulations as possible, with each simulation using an existing commercial encapsulant. Parameter sweeps would be unlikely, and the focus of this work would be to identify the best encapsulant to use out of a predetermined set. While it requires less time and computational resources versus a full simulation study, the downside of this approach is that package behavior is not well established and the most optimal encapsulant

properties are uncertain. However, if performed alongside experimental temperature cycling, these issues are either solved or become less significant.

The format of the brief study is as follows. The simulation setup from Chapter 2 is required, particularly because an incorrect simulation setup is harder to notice if a study is not being performed. This includes the multiple runs required to both confirm mesh convergence, and to establish the minimum number of temperature cycles needed within a simulation to show ΔW_{avg} converging. This also assumes you have either experimental confirmation or a logical guess as to which bond in the package is the location of first failure. If you are unsure, collect ΔW_{avg} for as many bonds as possible, which will marginally increase post-processing time. The difference between this study and the one performed in Chapter 3 are in the number and purpose of simulation runs. In Chapter 3, the intention is to sweep CTE and E values that could represent common encapsulant materials. The intention is to determine what encapsulant CTE values reduce or increase fatigue, what is the minimum E required for the encapsulant to have an effect, and what encapsulant properties minimize ΔW_{avg} on your first failure bond.

In this sweep, you are either identifying what is the best encapsulant to use out of a pre-determined set, or you are collecting ΔW_{avg} values to apply Darveaux's Model to an ongoing temperature cycle experiment. For either option, you must collect the material properties for each encapsulant you wish to evaluate and run as many simulations as encapsulants in your set. Ideally, you should evaluate a variety of soft and rigid encapsulants to get a range of ΔW_{avg} values. While you may not know what the most optimal encapsulant is, general principles should give you a reasonable set of expectations.

Using no encapsulant will likely have the highest ΔW_{avg}. The only encapsulants that will have a meaningfully higher ΔW_{avg} versus No Encapsulant are rigid encapsulants with a significant CTE mismatch, which you should be avoiding except for experimental testing.

Silicone gels will have a ΔW_{avg} that will be at most ±10 % different versus using no encapsulant. While the soft encapsulant can slightly change the outcome, its low elastic modulus prevents any major deviations from the No Encapsulant scenario. Simulating an encapsulant with

a CTE higher than 100 ppm/°C can cause errors, so a reasonable approximation would be to use two different encapsulants, each with a low *E* (~20 MPa) but one with a low CTE (10 ppm/°C) and the other with a high CTE (80 ppm/°C). If the *E* is too low to mechanically influence the warpage, then both results will have similar values of ΔW_{avg}, even if the low CTE encapsulant is well-matched.

Rigid encapsulants, possessing an *E* large enough to influence the package, can either be better or worse than silicone gel. The key is their degree of CTE mismatch. While each package is unique and thus will possess different rules, two tenants are consistent. First, when comparing two encapsulants with the same CTE, increasing *E* will intensify the outcome, whether positive or negative. Second, when comparing two encapsulants with the same *E*, the one with the CTE closer to that of the package substrates (2-15 ppm/°C for the PCB-Interposer package) should have a lower ΔW_{avg}. The CTE mismatch allowed with the substrates before an encapsulant becomes harmful is also package dependent, but a mismatch greater than 20 ppm/°C with the higher CTE material is a reasonable rule of thumb for when the encapsulant becomes harmful. However, this will vary for each scenario.

Finally, the best way to increase confidence is to simulate a variety of encapsulants, even ones you may not be testing. If the results are dissimilar to the above conclusions, then there is a problem with the simulation setup.

4.3 Quantifying the Impact of Soft Encapsulants

The objective of this section is to confirm that encapsulants possessing an E expected of silicone gels results in Internal Gate fatigue comparable to not using any encapsulant. A CTE sweep between 8 and 80 ppm/°C at E = 17.5 MPa results in a near-constant Internal Gate ΔW_{avg} that is at best 5.6 % lower than the No Encapsulant scenario. Therefore, using silicone gel instead of a rigid encapsulant sacrifices significant reduction in Internal Gate ΔW_{avg}.

The purpose of this section is to demonstrate the outcomes of using either no encapsulant or silicone gel. The expectation from Section 4.2 is that the results will be similar, as neither option is expected to provide the mechanical support to couple or restrict the thermal warpage of the substrate. While this analysis can be done without the study from Section 3.4, the data from the sweeps are included to help demonstrate the concepts illustrated.

The following simulations are performed using the same settings as in Chapter 3. A summary is in Section 3.3, while a detailed discussion is in Chapter 2. To evaluate the No Encapsulant scenario, the encapsulant geometry was suppressed. To evaluate the effect of a soft encapsulant, five different encapsulants were simulated over a range of 8 – 80 ppm/°C. This was done for two reasons. The first is that using materials with a CTE greater than 100 ppm/°C can result in convergence issues, which can be fixed but require additional computational time and resources to do so. The second reason is that if the encapsulant stiffness is too low, then the CTE mismatch is irrelevant and all flexible encapsulants should have the same outcome. Therefore, to both avoid convergence issues and confirm that flexible encapsulants result in the same outcome regardless of CTE mismatch, five encapsulants are evaluated to determine the effect of using SilGel 612. The Poisson's ratio of all encapsulants is approximated as 0.35, which is a reasonable value for polymers. The results of this section are not dependent on the value chosen.

Fig. 4-1 contains the single value solution of the No Encapsulant Scenario and the CTE sweep at a silicone gel E of 17.5 MPa. A second sweep at an elastic modulus of 4.75 GPa is included as a comparison. The conclusion is that the outcome expected in BGA packaging, silicone gel having minimal thermo-mechanical effect, is demonstrated in the simulation model for the PCB-

Interposer package. As demonstrated with the 4.75 GPa sweep, an encapsulant with the proper stiffness should reduce the Internal Gate ΔW_{avg} if it has a CTE ≤ 60 ppm/°C. However, all five encapsulants with an E of 17.5 MPa have identical outcomes. Therefore, the CTE mismatch has negligible impact for silicone gels as they lack the stiffness to influence the structure. Therefore, while it is useful to experimentally temperature cycle the package with either no encapsulant or SilGel 612 to relate cycles to failure to ΔW_{avg}, the package should not use either encapsulant option in any real-life scenario.

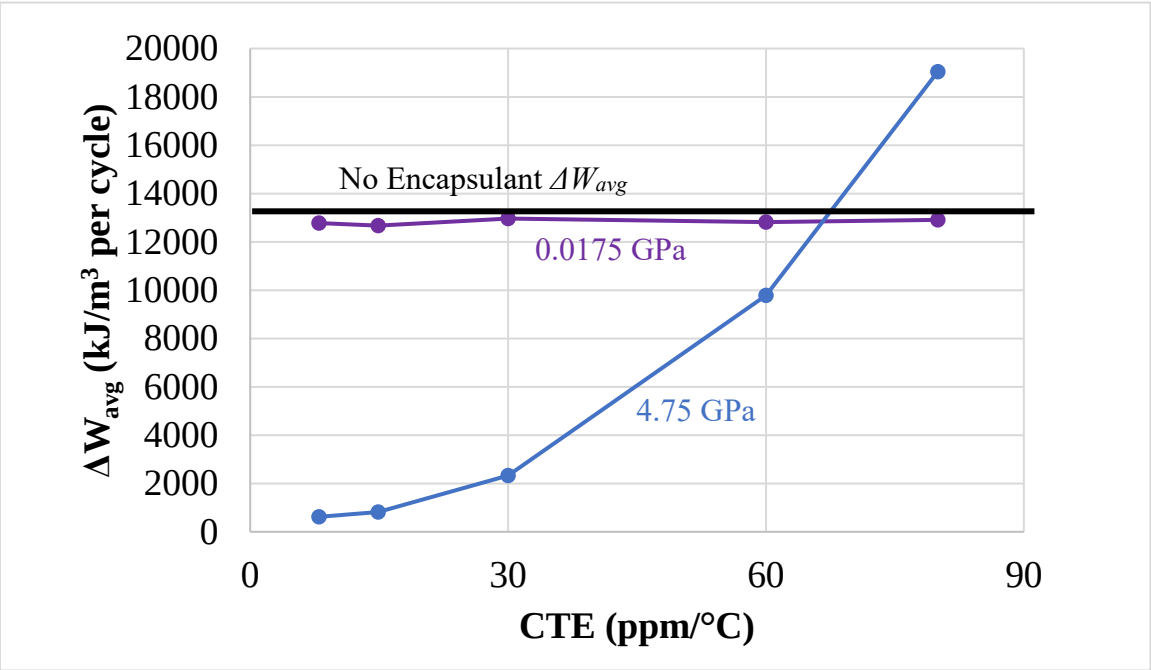


Fig. 4-1. The effects of using either No Encapsulant, an encapsulant with an elastic modulus common to silicone gel (0.0175 GPa), and a rigid encapsulant (4.75 GPa) on the Internal Gate. This is a condensed version of Fig. 3-8. At best, using a silicone encapsulant results in a 5.6 % reduction versus the No Encapsulant scenario.

4.4 Quantifying the Impact of Using Rigid Encapsulants

The objective of this section is to quantify the outcomes of using two available rigid encapsulants, ME-531 and EP-2000. In comparison to the No Encapsulant scenario, using ME-531 reduces the Internal Gate ΔW_{avg} by 91.3 %, while using EP-2000 reduces Internal Gate ΔW_{avg} by 97.3 %. Any material that has both a lower CTE and higher E than EP-2000 should further reduce Internal Gate ΔW_{avg}. However, while there are several types of materials that meet this requirement, only one is a polymer material that does not require significant study before use.

The purpose of this section is to demonstrate the outcomes of using two rigid encapsulants with CTEs well-matched to the package components. The expectation from Section 4.2 is both encapsulants will have a lower ΔW_{avg} than the No Encapsulant scenario as they have a minimal CTE mismatch and high E. EP-2000 is expected to be the better encapsulant as it has both a smaller CTE mismatch with the package substrates and an elastic modulus three times larger than ME-531. The comparison between ME-531 and EP-2000 can be done without the results from Section 3.4, but the identification of better encapsulants requires the parameter sweeps.

The following simulations are performed using the same settings as in Chapter 3. A summary is in Section 3.3, while a detailed discussion is in Chapter 2. The material properties for ME-531 and EP-2000 are in Table 4-2. Material data sheets supplied the necessary material properties except for the Poisson's ratio, which is approximated at a reasonable polymer value of 0.35. Equation (4) shows that reducing the value of ν will increase the shear modulus of the material, which in turn makes it stiffer and further reduces Internal Gate ΔW_{avg} in testing. While altering ν will change the exact value of ΔW_{avg}, it is not expected to meaningfully alter the conclusions of this section.

Fig. 4-2 contains the low CTE region of the Internal Gate parameter sweep for the Internal Gate, with the ΔW_{avg} values of ME-531 and EP-2000 superimposed onto it. As expected, replacing ME-531 with EP-2000 reduces ΔW_{avg} by 806.5 kJ/m^3 per cycle, a reduction of 68.7 %.

However, until experimental work is conducted, the improvement in terms of increased cycles to failure is uncertain.

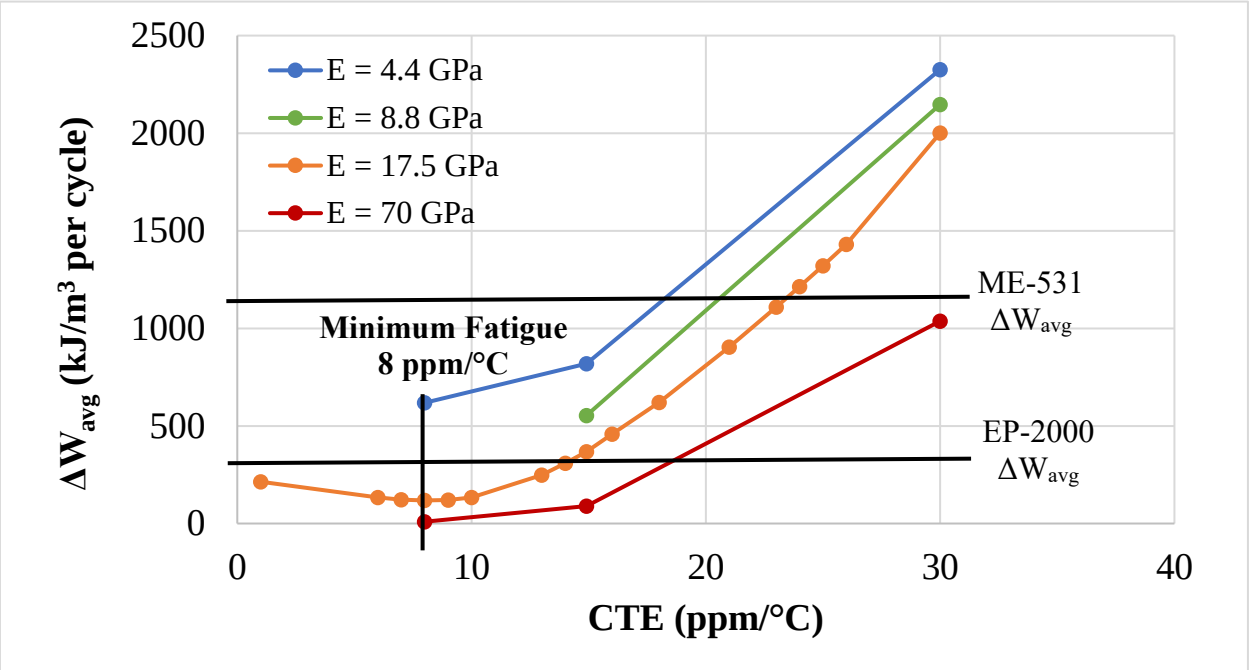


Fig. 4-2. The CTE sweep from Fig. 3-8, focusing only on 30 ppm/°C and below. The ME-531 and EP-2000 encapsulants are included. The difference between ΔW_{avg} at 14.9 ppm/°C (EP-2000) and 8 ppm/°C (minima) is a 67.8 % reduction.

According to the simulation model, EP-2000 is the best encapsulant that we possess for encapsulating the PCB-Interposer package. However, it is not the most optimal encapsulant, as 8 ppm/°C is the minima and deviating from that value either up or down increases ΔW_{avg}. The orange dot at 1 ppm/°C is a non-existent material, but it its value does make logical sense. The encapsulant is now well-matched to the Si die and AlN substrate, while possessing a 15 ppm/°C mismatch with the Cu and FR4 substrate. The curve is not expected to return to the No Encapsulant ΔW_{avg} as the encapsulant CTE → 0 ppm/°C, as the CTE mismatch between the encapsulant and package components can only be as large as the CTE of the package components.

Based on Fig. 4-2, any material that has both a CTE lower than EP-2000 (14.9 ppm/°C) and an *E* greater than EP-2000 (17.5 GPa) should reduce the Internal Gate ΔW_{avg} relative to EP-2000. As the elastic modulus is a measure of the amount of mechanical energy required to strain a

material by one unit, and a material's CTE is the amount of strain a material experiences per unit of thermal energy, *E* and CTE tend to be inversely related. For example, the addition of fillers to polymer matrices both lowers the matrix's CTE and increases its *E* [79]. Therefore, most materials that meet one of those requirements will also meet the other.

Referring to Table 1-6, there are three materials that can meet these requirements. While most ceramics and some metals meet the stipulations listed above, they are not included, as using these materials for encapsulation are both impractical and have not been explored. The first option is lead glass, which [39] investigated as a high temperature encapsulant. However, this material is non-viable for our application for two reasons. The first is that all layers required a polyimide buffer layer to prevent the glass from cracking upon cooling, which is a non-conventional practice. The second and more crucial reason is that the glass is poured into the package as a 500 °C liquid, which far exceeds the allowable temperature of the FR4 PCB.

The second option is to use cement. [41] investigated the use of Resbond 920 cement as a potential high-temperature encapsulation and found that the encapsulated package passed both thermal shock testing and high temperature reverse bias testing. However, information on the use of cement as an encapsulant is limited. Therefore, the use of cement would necessitate multiple tests on the adherence of the cement to various materials, its chemical reactivity with the various materials, and its insulation capabilities. Unless such an undertaking is acceptable, the use of cement is not advised.

The final option is EP-3500, which is a polymer encapsulant produced alongside EP-2000 by Parker Lord. As it is a two-part epoxy resin that can utilize EP-2000's hardener material, it is like EP-2000 in both chemical composition and adhesion to other packaging components. Of the options presented, EP-3500 has the fewest hurdles to implementation, so it is recommended for further investigation as a potential PCB-Interposer encapsulant.

Table 4-3. Three Materials That Could Outperform EP-2000.

Encapsulant	Material	Linear CTE (ppm/°C)	Elastic Modulus (GPa)	Maximum Temperature (°C)
Lead Glass	Glass	10.3	Unlisted	322
Resbond 920	Cement	8.1	Unlisted	1650
EP-3500	Epoxy	10.4	20	206

4.5 Conclusions

The objective of Chapter 4 is to establish the outcomes of the four encapsulant choices that will be utilized in future experimental temperature cycling. It is done in the context of an abbreviated encapsulant study in whose purpose is either to rank several potential encapsulants or to apply Darveaux's Model to the outcome of experimental temperature cycling. Expectations based on first principles were outlined, then verified using simulation work.

Section 4.3 confirmed that using encapsulants with an elastic modulus like silicone gels resulted in a negligible improvement versus using no encapsulant at all. Therefore, a package encapsulated with silicone gel are expected to perform only marginally better than a package with no encapsulant in experimental temperature cycling. Therefore, silicone gel encapsulation is not recommended if the intended goal is to increase the lifetime of the package.

Section 4.4 confirmed that two encapsulants with minimal CTE mismatch and high E reduce ΔW_{avg} relative to using silicone or no encapsulant at all. A package encapsulated with EP-2000 is expected to survive the longest out of the four encapsulant options during temperature cycling. However, encapsulants with a lower CTE and higher E will lower Internal Gate ΔW_{avg} versus EP-2000, which will increase the cycles to failure. The only practical replacement currently is its sister material, EP-3500. As it is expected to behave similarly to EP-2000, it is recommended for further investigation.

A brief encapsulant study like the one described in Section 4.2 is only recommended if either computational resources are limited, or experimental work is being conducted in tandem. To ensure that the simulations are giving logical results, you should at least simulate a package without encapsulant, two packages that use low E encapsulants, and two packages that use significantly different rigid encapsulants. Therefore, the relative results are predictable based on the first principles, which increases model confidence.

Chapter 5. Summary and Future Work

5.1 Main Objectives

This thesis has two overarching objectives. The first objective is to use simulations to provide evidence for a materials-based method of increasing the thermo-mechanical reliability of a new GaN HEMT package. Parameter sweeps illustrate the relationship between the encapsulant material properties and the first failure bond's per-cycle fatigue. Commercially available rigid encapsulants have the material properties necessary to reduce the per-cycle fatigue, which should extend the reliable lifetime of the PCB-Interposer package. The next step is to verify the results of this simulation by performing experimental temperature cycling on the package with the commercially available encapsulants.

The second objective is to explain how to perform a thermo-mechanical simulation using ANSYS Workbench 2021R2 to someone without a mechanical or materials engineering background. This is to fill the literature gap regarding comprehensive guides on performing this type of work. Each step of preparing the encapsulation study is explained in Chapter 2, and Chapters 3 and 4 interpret the simulation outputs.

5.2 Chapter 1 Summary

Chapter 1 summarizes how a desire to increase the output power and density of electrical vehicle (EV) power electronics resulted in the PCB-Interposer-on-DBC package and this thermo-mechanical design evaluation. This is both to provide the necessary context for the "how" and "why" of Main Objective #1.

The basis for this work lies in the Electrical and Electronics Tech Team's 2017 roadmap for future EV design. The roadmap quantifies the improvements needed to make EVs both affordable and comparable in performance to combustion vehicles. To meet the parameters for a smaller 100 kW inverter, silicone power transistors will be replaced with wide bandgap materials like gallium nitride (GaN).

However, GaN power electronics are not mature, with limited output power being one consequence. While commercial packages are limited to 650 V and 60 A, GaN Systems produces an unpackaged 650 V, 150 A GaN HEMT. Previous work culminated in the PCB-Interposer-on-DBC design, which is a chip-scale package with a simulated thermal resistance of 0.14 °C/W and simulated parasitic inductance of 1.2 nH. However, no reliability evaluation was performed during the design process.

The most common type of failure in any application is fatigue failure, in which repeated loading gradually initiates and propagates a crack. In power electronics, high operating temperatures in conjunction with a coefficient of thermal expansion (CTE) mismatch between bonded components leads to package warpage and eventual fatigue failure. The failure occurs in the bonding structures that provide the physical and electrical connections within the package, with two bonding materials being solder and sintered silver (Ag). To evaluate how long a package will survive in each application and establish the first point of failure, a package undergoes temperature cycling, in which it is repeatedly heated and cooled until the bonds fail.

While experimental testing identifies the location of failure and the number of cycles to failure, it requires both existing packages and months of experiments. A useful starting point is to use

thermo-mechanical simulations to establish expected failure locations and optimal designs, then perform experimental cycling to confirm the simulation results and establish the cycles to failure. This thesis only focuses on simulation work, with the experimental thermal cycling as expected future work.

A common method in flip chip packaging to reduce thermal fatigue is to encapsulate the bonds using specific polymeric materials. Along with the benefits of a chemically inert environment and electrical insulation, rigid encapsulants with a low package-to-encapsulant CTE mismatch and high elastic modulus (*E)* will reduce fatigue on the bonds expected to fail first. Soft encapsulants like silicone will provide similar chemical and electrical benefits but lack the stiffness to alter the bond fatigue. As encapsulant can be used to increase the vulnerable bond lifetime without altering any of the thermal or electrical properties of the PCB-Interposer package, the thermo-mechanical simulations focus on investigating how these encapsulants alter bond fatigue.

As the future experimental temperature cycling is expected to use polymer encapsulants currently in use by this research group, ME-531 and EP-2000 are specifically selected for study in Chapters 3 and 4. However, as Chapter 4 results indicate that using EP-3500 in place of EP-2000 will further reduce the fatigue placed on the Internal Gate, it is advisable to investigate use of EP-3500.

5.3 Chapter 2 Summary

The objective of Chapter 2 is to provide the information necessary for evaluate the simulation setup and assumptions in a way that is understandable to someone learning about thermo-mechanical simulations. Each section covers an important topic in setting up, running, and evaluating a thermo-mechanical simulation. This is in service of Main Objective #2.

Section 2.2 provides a step-by-step guide for setting up a simulation in ANSYS Workbench 2021R2. Section 2.3 discusses the boundary conditions that provide the necessary mechanical support and heating to simulate temperature cycling. The consequences of the simulation ignoring thermal transients are also discussed. Section 2.4 discusses how to perform a mesh convergence study, along with the quality of the mesh used in this work. Section 2.5 discusses how treating all non-bond materials as isotropic and linearly elastic is a useful assumption, and why the bonds are represented with the elastic-viscoplastic Anand constitutive model. Section 2.6 explains how volume-averaged inelastic strain energy density per cycle (ΔW_{avg}) represents the inelastic work performed on the structure per thermal cycling and why it is used as a metric of fatigue. Section 2.7 establishes how to use ΔW_{avg} to compare the relative lifetime between two bonds. It also establishes the assumption that the edge of the die attach, called the Die Attach Comparable region, can be compared against the Internal bonds to identify which sintered Ag bond fails first. As all Sn60Pb40 bonds are identical, no such assumption is required.

5.4 Chapter 3 Summary

The objective of Chapter 3 is to identify which bonds in the PCB-Interposer package will fail first and relate the encapsulant properties to the first failure bond's ΔW_{avg}. As any cracked bonds will degrade or break the package, identifying which bonds fail first and extending their lifetime is necessary. While primarily in service of Main Objective #1, the explanation of results assists with Main Objective #2.

Previous work with BGA solder balls found that using a high E encapsulant with a CTE like the package substrates extends the lifetime of the most vulnerable bonds. As this materials-based method could improve the reliability of the PCB-Interposer without a redesign that could compromise its optimal traits, simulations are used to investigate the validity of this method. For this method to be viable, parameter sweeps on the bonds expected to fail first must show that using certain encapsulants would reduce the per-cycle fatigue, ΔW_{avg}, on said bond. Based on BGA literature, the encapsulants expected to minimize ΔW_{avg} have a CTE like the package components (< 30 ppm/°C) and an E > 1 GPa.

The first step is to identify which bonds are expected to fail first. A stipulation of using ΔW_{avg} is that the comparison of two bonds is only valid if the bond material and volume is identical. Therefore, all sintered Ag bonds can be compared to identify what sintered Ag bond will fail first, and all solder bonds can be compared to identify what solder bond will fail first, but we cannot determine which is the true first failure bond without experimental work. To identify which bonds are the potential locations of first failure, temperature cycle simulations using three encapsulants are completed. The first conclusion is that the sintered Ag bond with highest ΔW_{avg} is the Internal Gate bond. As it is the encapsulated Internal bond furthest from the package center, and out-of-plane shear is the majority contributor to the inelastic work, then the simulation follows expected trends from literature.

The second conclusion is that the solder bond with the highest ΔW_{avg} is the External Source 4 bond. As it has a unique shape, is not in-between the components it is bonded to, and is not encapsulated, it does not have a comparable structure in literature. However, the reason for the

solder bond closest to the package center failing first is that the lack of pin deflection generates high stress regions that fatigue the bond.

Parameter sweeps identify what encapsulants minimize the ΔW_{avg} on each of these two potential locations of first failure. The encapsulant that minimizes the Internal Gate ΔW_{avg} has a CTE that compromises between the PCB and silicon die, and maximizing the stiffness of the encapsulant further reduces ΔW_{avg}. The encapsulant that minimizes the External Source 4 ΔW_{avg} has a CTE equal to the solder bond, and maximizing the stiffness of the encapsulant further reduces ΔW_{avg}.

While experimental testing is required to determine which is the true location of package initial failure, the rest of this work will focus on the Internal Gate bond instead of the External Source 4 bond. The first reason is that losing the External Source 4 bond will degrade the package performance, but losing the Internal Gate bond will cause complete package failure. The second reason is that that the strain energy density gained by the Internal Gate per cycle is at least twenty times higher than the External Source 4 bond. While this does not conclusively mean that the Internal Gate will fail first, such a difference suggests this conclusion.

5.5 Chapter 4 Summary

The objective of this chapter is to establish the outcomes of the four encapsulant choices that will be utilized in future experimental temperature cycling. While primarily in service of Main Objective #1, this section also describes how to perform an abbreviated simulation study to assist Main Objective #2.

While Chapter 3 describes what encapsulants minimize Internal Gate ΔW_{avg} and why these encapsulants help, it does not explicitly evaluate encapsulants that will be used in experimental work. Calculating ΔW_{avg} for each of these scenarios is crucial for two reasons. First, the encapsulated package with the lowest ΔW_{avg} is expected to last the longest during experimental temperature cycling, so this presents a way to verify the simulation results presented in this paper. Second, if enough samples are evaluated, it may be possible to apply Darveaux's Model, which relates ΔW_{avg} to the cycles to failure of the package. If applicable, this relationship would allow for simulation redesigns to predict how the package would perform without more experimental testing.

Section 4.3 looks at the outcomes when using either no encapsulant or an encapsulant with an elastic modulus common to silicone gels. Regardless of the encapsulant CTE, the low E encapsulant had at best a 5 % reduction in the Internal Gate ΔW_{avg} versus the No Encapsulant scenario. This is the outcome expected of using silicone gel, as it is marketed specifically for lack of stiffness.

Section 4.4 looks at the outcomes of using two rigid encapsulants and identifies what properties a material would need to be superior to the two options. Using either encapsulant reduces the Internal Gate ΔW_{avg} by at least 90 % relative to the No Encapsulant scenario. Of the two options, EP-2000 has a lower ΔW_{avg} and is thus the recommended encapsulant for packaging the PCB-Interposer. If a greater thermo-mechanical reliability is desired, using a lower CTE, higher E material should further reduce the Internal Gate ΔW_{avg}. The most practical replacement is EP-3500, a polymer encapsulant expected to behave like EP-2000.

5.6 Future Work

This project is intended as the groundwork for experimental temperature cycling of the package. However, once completed, more detailed simulations are recommended.

1. **Experimental Temperature Cycling:** Chapter 3 established that the first sintered Ag bond to fail is the Internal Gate, while the first Sn60Pb40 bond to fail is the External Source 4 bond. Chapter 4 predicted the relative lifetimes of using four different encapsulation options. The first step of experimental thermal cycling work will be to establish what is the true first failure bond in the package, and if that relative encapsulant ranking is correct. This would validate the simulation model and establish the expected cycles to failure of the package in various scenarios. This work can also explore if Darveaux's model is applicable, which predicts the cycles to failure of the package based on the ΔW_{avg} values from simulations.

2. **Remove Model Assumptions that Underestimate the true value of ΔW_{avg}:** Section 1.6 discusses how encapsulant mechanical properties are often unreported, resulting in encapsulant models that are incomplete and ignore the temperature dependance of these polymers. Heating polymers increases their CTE and lowers their *E*, so this assumption will underestimate the ΔW_{avg} of critical bonds. If Darveaux's model is applicable to the first failure bonds, collecting temperature dependent properties for EP-2000 increases the accuracy of ΔW_{avg}. A dilatometer or thermo-mechanical analyzer (TMA) can determine the CTE(T) of a polymer, while a dynamic mechanical analyzer (DMA) can determine the storage modulus (E') of a polymer. At temperatures where the phase lag (δ) between stress and strain is small, the storage modulus can be approximated as the elastic modulus.

Appendices

Appendix A – ΔW_{avg} Values for All Simulations

All ΔW_{avg} are in kJ/m^3 per cycle.

Material	Notes	Young's Modulus (GPa)	CTE (ppm/°C)	Internal Gate	Drain 1 Joint	Source 1 Joint	Drain 3 Joint	Source 4 Joint
All Solder	V3 M4	N/A	N/A	12427.00	8606.90	7988.70	472.68	232.56
All Sintered Ag	V3 M4	N/A	N/A	13445.00	7415.40	6806.70	299.72	119.30
All Solder w/ EP-2000	M4 V3 Short	17.50	14.90	500.31	312.96	327.20	295.00	326.93
No Underfill	V3 M4	0.00	0.00	13426.00	7365.40	6769.90	302.04	120.49
ME-531	V3 M4	6.00	21.00	1173.50	798.70	773.35	712.49	706.17
26 ppm/°C	V3 M4	17.50	26.00	1431.00	1156.90	1189.10	1164.90	1171.10
25 ppm/°C	V3 M4	17.50	25.00	1321.50	1048.00	1080.60	1052.30	1062.60
24 ppm/°C	V3.2 M4.2	17.50	24.00	1214.20	942.27	975.05	943.61	957.60
23 ppm/°C	V3 M4	17.50	23.00	1108.70	839.93	871.96	838.76	855.34
21 ppm/°C	V3.2 M4.2	17.50	21.00	904.46	647.79	677.40	641.80	660.13
18 ppm/°C	M4 V3 Short	17.50	18.00	621.17	395.73	418.99	381.07	399.84
16 ppm/°C	M4 V3 Short	17.50	16.00	458.94	253.42	273.56	235.25	252.44
EP-2000	M4 V3	17.50	14.90	367.88	187.70	203.20	169.33	182.42
14 ppm/°C	M4 V3 Short	17.50	14.00	309.77	142.59	154.62	124.72	134.99
13 ppm/°C	M4 V3 Short	17.50	13.00	247.63	100.31	108.94	84.18	91.86
10 ppm/°C	M4 V3 Short	17.50	10.00	133.50	31.71	34.81	27.90	30.98
9 ppm/°C	M4 V3 Short	17.50	9.00	120.89	28.45	30.49	28.08	30.46
8 ppm/°C	M4 V3 Short	17.50	8.00	118.32	31.26	32.81	32.74	34.33
7 ppm/°C	M4 V3 Short	17.50	7.00	122.77	37.51	39.13	41.24	41.13
6 ppm/°C	M4 V3 Short	17.50	6.00	132.94	48.82	50.38	55.47	53.29
1 ppm/°C	M4 V3 Short	17.50	1.00	214.04	186.81	192.26	213.24	197.86
17.5*10^-6 GPa	M4 V3	0.00	14.90	13609.00	7362.30	6771.40	301.71	120.56
17.5*10^-3 GPa	M4 V3	0.02	14.90	12672.00	6771.00	6230.50	292.21	135.46
4.375 GPa	M4 V3 Short	4.38	14.90	819.75	364.37	346.46	250.64	256.72
8.75 GPa	M4 V3 Short	8.75	14.90	553.27	260.82	251.90	214.45	214.76
EP-2000	M4 V3	17.50	14.90	367.88	187.70	203.20	169.33	182.42
26.75 Gpa	M4.2 V3.2	26.75	14.90	272.98	177.20	192.48	164.54	176.31
28 Gpa	M4.2 V3.2	28.00	14.90	262.73	174.70	189.84	162.50	174.01
30 Gpa	M4.2 V3.2	30.00	14.90	247.65	170.99	185.04	159.10	169.52
32 Gpa	M4 V3.2	32.00	14.90	230.01	166.11	179.94	154.91	164.79
35 GPa	(V2) M4 V3 Short	35.00	14.90	211.36	158.66	171.42	148.40	156.98
52.5 GPa	(V2) M4.2 V3 Medium	52.50	14.90	133.07	107.11	115.91	101.33	104.97
70 Gpa	(V2) M4.2 V3 Medium	70.00	14.90	89.52	77.17	83.41	73.74	75.10
8 ppm/°C 17.5 MPa	M4? V3?	0.02	8.00	12771.00	6837.70	6244.60	284.83	127.97
8 ppm/°C 4.375 GPa	M4? V3?	4.38	8.00	618.75	186.28	174.96	136.03	136.97
8 ppm/°C 17.5 Gpa	M4 V3 Short	17.50	8.00	118.32	31.26	32.81	32.74	34.33
8 ppm/°C 35 Gpa	M4? V3?	35.00	8.00	26.03	13.38	12.14	13.99	13.52
8 ppm/°C 70 Gpa	M4? V3?	70.00	8.00	9.33	6.51	5.82	7.00	6.82
10 ppm/°C 8.75 Gpa	M4 V3 Short	8.75	10.00	318.03	83.15	79.22	65.96	68.63
10 ppm/°C 17.50 Gpa	M4 V3 Short	17.50	10.00	133.50	31.71	34.81	27.90	30.98
30 ppm/°C 17.5 Mpa	M4.5 V3.5	0.02	30.00	12963.00	6911.90	6458.80	410.15	157.45
30 ppm/°C 750 MPa	M4.5 V3.5	0.75	30.00	3748.70	2366.80	2007.20	1311.40	946.73
30 ppm/°C 4.375 Gpa	M4.2 V3.2	4.38	30.00	2326.10	1914.90	1838.80	1786.80	1745.20
30 ppm/°C 8.75 Gpa	M4.2 V3.2	8.75	30.00	2147.00	1827.40	1789.30	1820.50	1782.40
30 ppm/°C 13 Gpa	M4.5 V3.5	13.00	30.00	2131.30	1678.70	1687.70	1842.80	1725.20
30 ppm/°C 17.5 Gpa Attempt 2	M4.2 V3.2	17.50	30.00	2001.00	1696.20	1707.90	1846.20	1749.40
30 ppm/°C 70 Gpa	M4.2 V3.2	70.00	30.00	1037.10	1325.90	1320.40	1375.60	1288.40
60 ppm/°C 17.5 MPa	M4.3 V3.3	0.02	60.00	12816.00	7032.20	6556.80	487.93	206.34
60 ppm/°C 750 MPa	M4.3 V3.3	0.75	60.00	7547.10	7816.30	5838.20	6340.50	4640.70
60 ppm/°C 4.375 GPa	M4.3 V3.3	4.38	60.00	9784.10	8157.10	7779.60	8754.00	8052.70
60 ppm/°C 8.75 Gpa	M4.3 V3.3	8.75	60.00	8691.00	7791.10	7656.90	8395.00	7875.60
60 ppm/°C 17.50 Gpa	M4.4 V3.4	17.50	60.00	6958.00	6557.80	6636.80	6883.90	6457.90
80 ppm/°C 17.5 MPa	M4.5 V3.5	0.02	60.00	12904.00	7259.10	6673.90	556.94	247.64
80 ppm/°C 4.375 Gpa	M4.4 V3.4	4.38	80.00	19044.00	14740.00	13866.00	15445.00	14374.00
80 ppm/°C 8.75 Gpa	M4.4 V3.4	8.75	80.00	15806.00	13835.00	13287.00	14293.00	13537.00

Total Die Attach	Die Attach - Source Edge	Die Attach - Drain Edge	1 mm Source Edge	1 mm Drain Edge
220.67	956.67	988.47	532.10	504.57
81.50	883.57	883.57	346.51	321.79
147.49	524.29	530.74	303.85	302.18
81.576	833.86	883.93	347.9	322.03
57.65	612.55	604.80	243.70	233.06
36.16	507.12	463.59	162.30	135.45
35.03	477.36	436.49	154.31	129.73
33.99	450.35	413.23	146.61	124.53
33.03	425.21	392.50	139.04	119.73
31.48	379.71	358.94	125.19	112.36
29.81	335.14	327.14	112.41	105.44
29.30	319.14	315.64	107.72	103.06
28.95	316.76	315.39	105.34	101.84
29.02	320.95	320.31	105.39	102.68
29.04	325.61	326.11	105.54	103.56
29.66	336.54	344.46	109.78	109.01
29.96	336.26	348.06	111.52	111.17
30.23	333.69	349.48	112.92	113.02
30.34	328.97	348.47	113.44	113.97
30.59	324.54	347.80	114.41	115.45
16.89	194.20	208.07	59.77	44.71
81.31	830.50	875.92	347.49	321.03
80.67	814.95	861.94	346.97	320.02
60.01	627.58	633.63	262.74	257.26
46.66	517.08	516.72	194.66	191.43
28.95	316.76	315.39	105.34	101.84
16.58	157.53	159.02	48.39	46.41
15.67	144.56	146.20	44.31	42.45
14.57	126.55	128.33	38.98	37.36
13.52	111.46	112.38	34.53	33.00
12.31	91.06	92.07	29.45	28.05
9.19	35.85	36.28	17.62	16.68
8.52	25.15	25.21	15.93	15.16
80.27	809.31	856.13	349.17	320.67
57.17	630.43	643.70	277.06	261.89
30.23	333.69	349.48	112.92	113.02
11.56	50.32	54.89	14.64	15.23
10.00	3.01	3.14	6.00	6.37
46.35	533.23	545.16	204.70	200.61
29.66	336.54	344.46	109.78	109.01
80.62	814.05	861.10	348.64	324.35
87.71	862.25	858.92	369.13	357.44
71.12	804.67	744.62	315.50	281.85
58.58	766.70	706.38	280.79	231.76
49.39	724.89	646.08	244.39	195.31
41.77	657.49	589.39	208.56	159.52
22.31	273.13	259.57	112.17	96.55
80.97	823.21	869.39	347.71	329.02
99.32	1167.00	949.69	469.88	381.64
121.83	1706.50	1404.60	677.46	450.66
121.19	1710.50	1480.60	660.40	470.96
106.67	1204.50	1440.00	538.32	390.80
81.15	829.26	874.61	346.91	331.81
164.57	1731.20	2133.70	872.29	587.12
171.81	1824.80	2150.70	862.09	627.79

Gate Solder	Drain 1 Solder	Drain 3 Solder	Source 1 Solder	External Source 4
10.81	11.44	17.21	14.46	21.34
0.36	0.36	0.48	0.40	0.64
11.47	13.07	13.60	12.92	16.16
10.851	11.461	16.742	13.924	21.025
12.18	14.04	14.70	13.52	17.23
13.08	12.69	12.89	12.51	14.78
12.92	12.60	12.81	12.41	14.72
12.76	12.53	12.75	12.33	14.72
12.60	12.47	12.72	12.26	14.69
12.31	12.42	12.73	12.20	14.80
11.91	12.48	12.94	12.29	15.23
11.62	12.61	13.21	12.45	15.93
11.49	12.71	13.40	12.57	15.92
11.37	12.83	13.61	12.71	16.52
11.26	12.98	13.86	12.88	16.81
10.97	13.61	14.81	13.60	18.00
10.90	13.87	15.23	13.89	18.55
10.83	14.16	15.68	14.20	19.06
10.77	14.45	16.05	14.51	19.36
10.72	14.80	16.55	14.89	19.98
10.05	12.02	18.16	12.25	18.67
10.89	11.46	16.74	13.93	21.03
10.87	11.59	16.66	13.86	20.84
11.53	13.30	14.35	13.15	17.11
11.33	13.17	14.00	12.99	16.82
11.49	12.71	13.40	12.57	15.92
11.50	12.32	12.84	12.21	15.21
11.50	12.27	12.77	12.17	15.13
11.51	12.19	12.69	12.10	15.02
11.51	12.13	12.59	12.04	14.89
11.49	12.03	12.45	11.95	14.72
11.43	11.60	11.86	11.56	13.89
11.38	11.34	11.48	11.32	13.35
10.84	11.44	16.59	13.78	20.85
10.91	12.66	13.99	12.89	17.00
10.83	14.16	15.68	14.20	19.06
10.72	14.49	20.22	14.54	20.26
11.13	16.42	23.34	16.40	23.38
10.78	13.15	14.28	13.19	17.32
10.97	13.61	14.81	13.60	18.00
10.97	11.89	18.98	13.98	23.78
11.97	15.63	19.17	14.71	22.73
13.83	16.27	16.65	15.06	19.05
14.20	14.76	15.01	14.04	17.25
16.20	13.37	14.46	13.26	17.69
15.83	12.93	13.74	12.99	17.60
13.39	13.18	15.82	19.01	28.76
11.10	12.72	19.30	14.39	23.78
16.22	26.05	24.20	19.84	27.31
24.62	26.33	24.26	23.26	29.20
25.38	23.76	22.54	22.75	29.90
23.21	21.20	23.12	15.68	37.47
11.20	13.42	19.51	14.70	23.92
33.29	38.63	32.52	33.66	42.37
34.47	32.23	31.63	34.25	45.19

Appendix B – ANSYS APDL Codes

The following two documents and attached comments are the APDL codes provided with permission by Paul Paret of the National Renewable Energy Laboratory (NREL). These codes were utilized in [60] and [61].

The first code is an input code that is applied to a single time step in the simulation and must be duplicated for every time step (20 sub steps requires 20 input codes). Use the “Detail” menu in the bottom left corner of ANSYS to designate which step the code applies to. This document ensures the proper settings are enabled for each step, including convergence values that the solver abides by. The author recommends copying and pasting the following text into a Notepad file and then importing it into ANSYS, as opposed to directly copying it into ANSYS. As the linked file can be refreshed once it is imported into ANSYS, this enables a single file to be used for multiple steps. For reference, “!” is the APDL command for comment.

The Input APDL File (Copy Below this Line)

```
/PREP7
TOFFST,273.15   ! Temperature Offset
/SOLU
STAT
NROPT,FULL,,ON  ! Newton - Raphson
SOLCON,ON
SSTIF,OFF
RATE,ON         ! Turning rate dependence ON - important for creep analysis.
NEQIT,100       ! Equilibrium iteration
PRED,ON
AUTOTS,ON       ! Auto Time Stepping
NSUBST,110,,110  ! Sets the starting, maximum, and minimum number of sub-steps for the load step
EQSLV,SPARSE    ! Using the Sparse solver
CNVTOL,F,,0.5,2,1   ! Force convergence criterion
CNVTOL,U,1,1E-3,0   ! Displacement convergence criterion
OUTRES,ALL,ALL      ! Save all results at all load steps and sub steps
```

The second code used is an output code that converts the stress-strain information into ΔW_{avg}. This code requires that the set of elements (either a full body or only part) be a Named Selection, as that allows it to be referenced in this calculation. The author recommends that each bond should have a unique Named Selection designation.

To utilize this code, there are two items that must be altered for your setup. First, ensure the Named Selection you wish to reference is in the code. The code below is written for a Named Selection called **DIEATTACH**. To use with another Named Selection, replace the six bolded term in the code with the name of the desired Named Selection.

The second item is that the code must be altered for each unique thermal cycle setup, with the crucial details being the step that you begin the thermal cycle on, the number of thermal cycles that you will perform, and the number of time steps that make up a thermal cycle. These values are marked in blue on the following code. The number 4 is used for both the number of temperature cycles used (use the fewest cycles possible that show convergence), and the number of time steps in a thermal cycle (dwell at hot, ramp to cold, dwell at cold, ramp to hot). The number 5 is used as you need to calculate the total inelastic energy density one more time than the number of thermal cycles. The number 3 is used because that is the final time step before the thermal cycle begins, and the number 19 is used because that is the final time step in the fourth and final thermal cycle.

The Output File (Copy Below this Line)

```
!Strain Energy Density Calculation at the Die Attach

/POST1

CMSEL,S,DIEATTACH    ! Select the desired Named Selection

*DIM,DIEATTACH,,5       ! Creating an array named 'DIEATTACH' that can take in 5 entries.
The 0 entry (no cycles), and an entry after each cycle.
*DIM,SED_PER_CYCLE,,4   ! Creating an array named 'SED_PER_CYCLE' that can take in 4
entries. Value 1 is the difference between DIEATTACH 1 and 0, Value 2 is the difference
between DIEATTACH 2 and 1, etc.
COUNT = 1

*DO,I,3,19,4                    ! FOR Loop. This tells the code that steps 4-7, 8-11, 12-15, and 16-
19 are each a thermal cycle 4 steps long. Selecting step 3 along with the following "LAST"
command sets that as the entry 0 in the DIEATTACH array, with the entry 1 starting with step 4.
SET,I,LAST,1

ETABLE,VOLUME,VOLU            ! Creating an elemental table with volume
ETABLE,SE_DENS,NL,PLWK        ! Elemental table with strain energy density
SMULT,SENERGY,VOLUME,SE_DENS   ! Elemental table with strain Energy (product of the
two tables above)
SSUM                          ! Calculating the total Volume, total strain energy density, and total strain
energy
*GET,SUMSE,SSUM,,ITEM,SENERGY
*GET,SUMVOLU,SSUM,,ITEM,VOLUME
SED = SUMSE/SUMVOLU           ! Total Strain Energy/Total Volume (Volume Averaged)

DIEATTACH(COUNT) = SED     ! Place the total inelastic SED at a given cycle (start of
simulation, end of thermal cycle X) in the array to later calculate SED/cycle.
COUNT = COUNT + 1

*ENDDO                                ! End of the do loop

*DO,I,1,4
SED_PER_CYCLE(I) = DIEATTACH(I+1) - DIEATTACH(I)  ! Calculating volume averaged
strain energy density per cycle
*ENDDO

*STATUS, SED_PER_CYCLE
my_SED_FINAL_DIEATTACH = SED_PER_CYCLE(4) ! Outputting the volume averaged
strain energy density per cycle of the final thermal cycle. I recommend setting this as a parameter
in the "Details" menu for easy access.
```

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