Design of High-Density Filter Building Blocks for SiC-Based Three-Phase Power Converters

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Abstract

The advent of wide-bandgap (WBG) devices like silicon carbide (SiC) MOSFETs has resulted in a paradigm shift toward high-density and high-efficiency integration of power electronics systems. This being the result of relatively high switching frequencies (>10 kHz) compared to conventional Si IGBT counterparts, which reportedly can minimize the size of passive components such as DC-link capacitors and line harmonic filters. Unfortunately, with faster switching speeds and high slew rates, the common-mode (CM) and differential-mode (DM) conducted emissions interference (EMI) noise is worsened. The effects are manifested at the utility interface with grid-tied applications (three-phase rectifiers or back-to-back converters) in the form of high CM and DM emissions, total harmonic distortion (THD) and current harmonics. While at the motor end, long cable and bearing/leakage current effects are prevalent. As such, typically bulky passive filters are recommended to comply with industry regulations and allow safe and reliable system operation, which can be detrimental on the overall system power density. Hence, it is imperative to minimize the filter volume/weight contribution to fully utilize the benefits of WBG power converters. As an added feature, modular filter building block (FBB) configurations inspired by the building block nature of power electronics converters are needed to address scalability to higher power levels (through interleaving or paralleling) without the need for significant filter redesign.
As such, for grid-tied applications (AC-DC converters), the interleaving of parallel converters adopted to achieve superior harmonic attenuation for grid-side currents at the expense of low harmonic filter volume. Therefore, interleaved converters are explored in Chapters 2 and 3. However, to block inter-channel circulation, additional use of coupled inductors (CI) can outweigh the benefits of interleaving. Therefore, modular FBB architectures with unique methods to handle circulating currents are proposed. At the same time, the FBB is designed to meet power quality and EMI limits for any given number of channels, up to the maximum number of channels, $N$, allowed at the point of common coupling (PCC). Consequently, a qualitative and quantitative comparison of FBB candidates is performed, and the indirectly coupled FBB using a secondary loop interconnection is proposed as a viable modular FBB candidate.

Correspondingly, for DC-AC inverters, modular filters can be realized using a masked impedance and decoupling approach. The test case being a DC-fed motor drive for aircraft propulsion systems. Techniques, such as optimized parallel RC dampers to reduce the peak bearing current and CM/DM magnetic integration of a DC side filter with an embedded DC current sensor and embedded decoupling path with gate driver for high frequency commutation, are implemented to reduce the overall weight of the system. The challenges with low temperature rise margin due to high ambient temperature and low peak Partial Discharge Inception Voltage (PDIV) are addressed. In addition, a novel pulse with modulation (PWM) scheme is proposed to further enhance the bandwidth of the proposed AC filter, specifically targeted to reduce the peak bearing current and improve the specific power and motor lifetime.
A negative consequence of high-density filter integration is the impact of self and mutual parasitic couplings of filter sub-components on filter attenuation, which is studied on a back-to-back converter system (AC-AC). Simplified lumped models that are representative of the high frequency filter behavior are developed to desensitize the impact of individual filter sub-components. Thereafter, unique winding and placement techniques are proposed to compensate for the impact of self and mutual parasitic couplings on the noise spectrum.

Overall, this work presents potential FBB topologies for varying modes of power conversion (AC-DC, DC-AC, and AC-AC), ultimately aimed at reducing the volume/weight of the system. Methods to minimize the passive component volume/weight from the point of view of topology, magnetic integration, and PWM techniques are discussed, while the implications of a high-density integration at high frequency is presented. Generalized practical design guidelines are formulated to aid in accurate high-density filter design for WBG converters.
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General Audience Abstract

With the ever-increasing use of switching converters, either AC-DC, DC-AC, or DC-DC converters, electromagnetic interference issues can affect the overall system performance, which necessitates the use of filters. This is especially true with more and more point-of-load applications (parallel converters in charging stations, industries, and residential loads), distributed energy sources (solar power, wind power, and battery storage systems), and primary sources (power plants) being integrated together into a super grid. Similarly, transportation applications (electric vehicles, more-electric aircrafts) demand strict filtering requirements, due to the prime importance of reliability. Therefore, three-phase power quality and EMI filters are an integral part of any power conversion system, from low to high power applications.

First, novel techniques to address the scalability and modularity of filters with parallel converters are considered (grid-tied application), where the benefits of interleaving and challenges in circulating current mitigation are addressed. The idea is simply to design one filter that can be used with any given number of converters running in parallel, which promotes rapid manufacturability to meet the ever-increasing demand. Thereafter a highly integrated and optimized filter structure is demonstrated for a traction inverter used in aerospace propulsion. Challenges pertaining to compact filter design are addressed, and new methods are proposed to overcome some of the critical issues that come with high-altitude operation, such as reliability, high temperature, and partial discharge-free operation. Lastly,
the effect of non-idealities on filters that can lead to deteriorated performance is explored. As such, solutions to compensate for these effects are proposed and verified.

Clearly, there is a need to optimize filters as well, minimizing their volume and weight contribution within a power converter. This aspect is considered throughout the work where design guidelines are proposed to optimize the given filter topology, filter parameter selection, and form factors for different applications, ranging from AC-DC converters to DC-AC traction motor drives.
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Chapter 1. Introduction

1.1 Review of State-of-the-Art Filter Building Blocks

A brief survey of existing competitive low-voltage (LV) converter/filter architectures (< 480 VAC) is shown in Fig 1.1. The trend with power rating and power density (highlighted within the gray box) shows that filter volume is a major contributor to overall system volume, regardless of system power level and power density. Therefore, methods to minimize filter volume is the primary research focus of this dissertation. The two prototypes covered in this dissertation are shown in the solid box, details of which are presented in Chapters 2, 3 and 4. The test bed in Chapter 5 is not optimized for power density, but merely a means to understand the high frequency effects of filter blocks; therefore it is excluded from the chart in Fig. 1.1.
Table 1-1 Summary of state-of-the-art, grid-tied power converter prototypes in Fig. 1.1

<table>
<thead>
<tr>
<th>Converter topology</th>
<th>$F_{sw}$</th>
<th>Rating</th>
<th>Filter topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>[1] Three-phase, three-level, six-switch Vienna rectifier</td>
<td>400 kHz</td>
<td>10 kW, 400 V$_{RMS}$</td>
<td>Two-stage LCLC for DM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Three-stage LCLC for CM</td>
</tr>
<tr>
<td>[2] Integrated active filter w/ buck type PFC</td>
<td>28 kHz</td>
<td>8 kW, 230 V$_{RMS}$</td>
<td>CM+DM LC filter stage at AC-side</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>CM-LC filter stage at DC-side</td>
</tr>
<tr>
<td>[3] Three-level T-type inverter</td>
<td>8 kHz</td>
<td>10 kW, 650 V$_{DC}$</td>
<td>Two-stage LCLC for DM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Three-stage LCLC for CM</td>
</tr>
<tr>
<td>[4] Two-level ultra-high speed GaN-based inverter</td>
<td>400 kHz</td>
<td>1.1 kW, 80 V</td>
<td>Two-stage LCLC for DM+CM</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Full sine wave output filter</td>
</tr>
<tr>
<td>[5] Five-level T-type inverter interleaved</td>
<td>50 kHz</td>
<td>60 kW, 480 V$_{RMS}$</td>
<td>Inter-cell transformer for circulating</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>current mitigation</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>Three-stage LCLC for CM</td>
</tr>
</tbody>
</table>

From a topological standpoint, filter structures are selected per the criteria of impedance mismatch [8] at the source and load terminals, as shown in Fig 1.2. Various methods of interconnection can be used to divert and control the flow of specific noise harmonics [9]. Primary motive is either to shunt or block noise components propagating in the noise path, or to utilize balancing circuits such as Wheatstone bridge [10][11].

Fig 1.2 Bare-bones topology breakdown based on impedance mismatch criteria.
Table 1-2 Inductor configurations

<table>
<thead>
<tr>
<th>Physical impression</th>
<th>Types</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Single phase discrete</td>
</tr>
<tr>
<td></td>
<td>Three Limb DM inductor</td>
</tr>
<tr>
<td></td>
<td>Three-phase CM inductor</td>
</tr>
<tr>
<td></td>
<td>Single phase Integrated DM+CM</td>
</tr>
</tbody>
</table>

To block noise components, discrete inductors, CM-DM inductors, or integrated CM+DM, inductors are employed as passive solutions [12][13][14][15][16]. Active cancellation techniques such as VSVC (voltage sense voltage compensation) or CSVC (current sense voltage compensation) [17] are other alternatives, particularly used for low power/voltage applications [18][19][20][21]. Similarly, passive shunt methods using discrete film capacitors or embedded capacitors [22][23][24] can be used. Due to limited bandwidth of active schemes, typically a combination of both (i.e. hybrid methods) are implemented [17] to get the best of both techniques. Other active schemes include direct pulse width modulation (PWM) techniques [25][26][27][28][29][30], which are implemented at the source.

Additional filter stages can also be added to enhance attenuation [31]. However, the parameter selection process can be cumbersome. Filter parameters (LC) for a multi-stage filter are typically selected using either closed form expressions or iterative design procedures. Generally, a trade-off exists between inductive and capacitive volume and loss, which typically results in a valley point that yields the lowest system volume.

To this end, this dissertation targets the application and research on low voltage (LV - < 800 V_{dc}) filter solutions, with power levels between 50 kW – 200 kW, targeting grid tied converters and DC-fed motor drives.
1.2 Filtering Requirements and Standards

1.2.1 Electromagnetic Interference (EMI) noise source and propagation

A. Power converter switching transients: To design an effective filter, the nature of noise source and propagation must be understood. The converter is the primary aggressor that can be modeled using terminal capacitances and a representative voltage source. Specifically, the per phase CM-equivalent circuit is derived per [32][33], which can be used in filter design. Most of the work in this dissertation is focused around the 3L converters, i.e., T-type and neutral point clamped (NPC) variants. So as an example, the three-level NPC module from Microsemi with terminal capacitances marked in schematic and module is shown in Fig 1.3. The terminal capacitances can be calculated through die area measurements per Table 1-3. Besides these capacitances, another aspect is the mixed frequency resonance [34] produced during switching transients, as shown in Fig 1.4, appearing as corresponding resonant modes in high frequency. This requires careful layout aimed at minimizing the commutation loop inductance.

Fig 1.3 Three-level NPC module and terminal capacitances (a) Detailed schematic and (b) Representative side-top profile of module (APTMC60TLM55CT3AG)
Table 1-3 Three-level NPC module and terminal capacitances

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Die Area (mm$^2$)</th>
<th>Measured capacitance (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{p1}$</td>
<td>180.5</td>
<td>56</td>
</tr>
<tr>
<td>$C_{p2}$</td>
<td>200.8</td>
<td>62.3</td>
</tr>
<tr>
<td>$C_{p3}$</td>
<td>112.0</td>
<td>35</td>
</tr>
<tr>
<td>$C_{p4}$</td>
<td>171.1</td>
<td>53.1</td>
</tr>
<tr>
<td>$C_{p5}$</td>
<td>150.8</td>
<td>46.8</td>
</tr>
</tbody>
</table>

Fig 1.4 Correlation between measured turn-off transient and measured CMV ringing frequency, (a) Turn of $dv/dt$ of Q1 and Q2 including resonant frequency and (c) Corresponding CMV frequency spectrum.

B. Propagation paths While the PWM voltage source is identified as the major contributor of EMI noise, the adjoining propagation path creates additional resonance and changes the noise profile significantly depending on the transfer gain. A typical example is shown in Fig 1.5(a) for a DC-fed motor drive, feeding an induction motor that is represented per [33]. The product of transfer gain of the circuit in Fig 1.5 (Note: Parameters of the circuit will be described in Chapter 4) and the Fast
Fourier Transform (FFT) of the CM voltage (CMV) noise source yields the measured CM spectrum in Fig 1.5. Clearly the dominant resonant modes in the transfer gain can be correlated with the observed resonance in the noise spectrum, meaning the propagation path has a significant impact on the noise profile. Filters can be essentially used to tweak the transfer gain to our advantage, such that these resonant modes can be suppressed, and an overall decaying slope (negative slope) can be achieved with increasing frequency along the x-axis.

Fig 1.5 (a) CM-equivalent circuit for a DC-fed motor drive, (b) Correlation between propagation path and the noise spectrum.

\[
i_{cm}(s) = \frac{i_{cm}(s)}{v_{cm}(s)} \otimes v_{cm}(s)
\]

C. Signal integrity: Another challenge brought by the high \(dv/dt\) is the EMI generated in the power loop and the CM current spikes induced in the auxiliary network, comprised of gate drivers, isolators/buffers, isolated power supplies [35], DSP control card, etc. A typical system architecture is shown in Fig 1.6, where the high \(dv/dt\) CM current propagation path from the isolated device ground
toward the control ground can be seen. Optical isolation for PWM and fault signals, galvanic isolation of LV auxiliary power supplies, and isolators/buffers featuring high common mode transient immunity (CMTI) are the preferred choice for SiC-based PWM converters in order to enhance signal integrity.

In summary, a detailed understanding of the generic EMI noise source and propagation path characteristics is a must for optimal filter parameter selection.

1.2.2 Filtering requirements

A pre-requisite for filter parameter selection is to first identify the design targets pertaining to specific standards, in order to build modular compact filter building blocks (FBBs). As an example,
Chapters 2 and 3 deal with the IEC-61000-3/12 for conducted emissions compliance, current harmonic, and THD specifications per IEEE-519/1594 (grid code). The former concerns mostly high frequency harmonics (typically 150 kHz – 30 MHz), while the latter deals with low frequency harmonics (<4 kHz). Note that there is no hard limit on the peak circulating current (CC) requirement; therefore, the system losses (i.e., converter and filter losses) are considered as the deciding criterion for CC filter design.

Chapter 4 deals with aerospace application, therefore the DO-160G standard is adopted as the conducted emissions standard. Additionally, for reliability considerations, the peak motor bearing current density is limited to 0.5 A/mm$^2$, obtained from lifetime calculations [36]. A maximum $dv/dt$ constraint is also imposed on the motor winding voltage stress, which is ensured by the proper selection of gate resistors (Note: The motor is adjacent to the motor control unit (MCU), so long cable effects are ignored here).

Chapter 5 considers IEC–61800-3-12 and CISPR-11, i.e., Class A (first environment public, LV network) standards. The specific requirement here is to comply with C2 emission levels for the grid-side. Again, from a reliability aspect, the full sinewave filter is adopted on the inverter end of the Back-To-Back system to mitigate reflected wave phenomenon due to the long variable frequency drive (VFD) cable, while a bridge-interconnection is implemented to account for the low frequency emissions.
1.3 Filter Optimization Workflow

A high-level design and optimization workflow for filter designs is shown in Fig 1.7. It starts with the control of the aggressor, i.e., the converter noise source either using pulse with modulation (PWM) schemes or topological changes such as interleaving. Thereafter, changing the propagation impedance characteristics that typically involve filter topology selection or damping of resonant modes can be explored. At this point, the filter parameters are determined based on the down-selected topology. The immediate next step would be form-factor optimization involving loss-volume map. This is followed by part placement, and hardware integration. Each of these aspects are covered in this dissertation.
Another key component is design of optimal inductors. A generic inductor design guide is presented in Fig 1.8, which is referred to throughout this dissertation. This generic flowchart can be used to optimize any given inductor shape such as a three-limb DM core or a nanocrystalline core using iterative form factor tuning. Round conductors are adopted in most cases but can be extended to printed circuit board (PCB) windings, foil windings, or Litz wire type windings as well. Typically, inductor design methodology has three stages. The first stage is concerned with parameter definitions and initializations. Subsequent terms, such as core and winding parameters, are calculated in the second stage. Material properties, type of winding, and physical core and winding dimensions are inputs in this stage. The third stage deals with loss and volume computations using closed-form expressions [37][38][39][40]. A typical example of form-factor optimization, i.e. stages 1 and 2 in Fig 1.8, is shown in Fig 1.9 and Fig 1.10, where a toroidal core and a boost inductor design are illustrated respectively.

While in this case, customization is feasible, it is imperative to note that in some cases vendors would provide the available form-factors per their inventory. The search space of the design optimization problem needs to be modified accordingly. Core material selection and winding geometry mostly depends on the frequency range and power level. Throughout the dissertation, different winding and core geometries will be demonstrated.

Customized magnetic design procedures help in optimizing complicated assemblies, such as the monolithic structure presented in Chapter 3 or an integrated DM+CM core in Chapter 4. The key is to identify the relationship between inductor dimensions and losses and volume.
Fig 1.9 A typical CM inductor design guide

START

\[ L_{cm}, I, T_{max}, K_a \]

Sweep \( \mu \)

Sweep \( A_L \)

\[ n = \frac{L}{A_L} \quad \text{Ratio} = \frac{L}{A_L} = \frac{\mu}{A_L} \]

Sweep \( A_e \)

\[ I_e = \text{Ratio} \cdot A_e \]

Sweep Depth Ratio

\[ IR = \frac{I_e}{2\pi} \cdot \frac{1}{2} \sqrt{A_e} \quad x_e = \sqrt{\frac{A_e}{\text{Depth Ratio}}} \quad \text{Depth Ratio} = \frac{\text{Depth}}{x_e} \]

\[ A_e = \frac{K_e \pi IR^2}{3n} \quad \text{MLT} = 2\pi \left( \frac{\sqrt{A_e} + IR}{\pi} \right) \]

Determine \( \text{AWG} \quad R_{wire} \quad P_{wire} \quad P_{core} \quad T_{cw} \quad \text{Boxed Volume} \)

Calculate \( B \)

\[ B = \frac{L_{cm}}{A_{en}} \]

Check if solution is within 75\(^\circ\)C OR \( B < B_{MAX} \) OR \( J < 8 \text{ A/mm}^2 \)

Yes, Store solution
No, Flag Error

End Sweep Depth Ratio

End Sweep \( A_e \)

End Sweep \( A_L \)

End Sweep \( \mu \)

END

For Volume Estimation a cylinder enclosing the choke is considered
1.3.1 Analytical formulations for loss and volume calculations

It is critical to estimate the loss and volume of inductive components based on analytical rules during the design process. The inductive losses are divided into core and winding loss. Core loss is estimated using the iGSE formulation as per [37][38], while the AC winding loss is estimated using Bessel functions [37]. While capacitors typically depict root mean square (RMS), current losses are induced across the equivalent series resistor (ESR), which can be obtained from loss tangent.
expression. The inductive and capacitive volume can be estimated directly from dimensions obtained iteratively or through vendor datasheet specifications, an example of which is demonstrated in [41][42].

1.3.2 Modular filter converter co-design

While converter and filter design are two different facets, they must be integrated into the same workflow, as shown in Fig 1.11. A bi-level linear-programing approach is adopted per [43], wherein the design procedure is divided into two stages. The first stage is concerned with parameter selection, while the second stage deals with actual physical design with loss and volume calculations. This optimization flow is adopted in Chapter 2 and 3 for the down-selection of FBB candidates. Although, alternate evolutionary computation-based algorithms could be used, the BLLP approach is simpler and would suffice for this study [44][45].

Fig 1.11 Bi-level linear programing approach adopted for system optimization studies as reported in [43]
1.4 Dissertation Outline

To tackle the challenges described in Sections 1.2 and 1.3 and present the analysis and design procedures aimed at minimizing filter volume/weight contributions, this dissertation is organized as follows.

In Chapter 2, the indirectly coupled filter building block (FBB), namely the secondary loop FBB (SL-FBB) with inserted impedance is proposed. The fundamental operating principle with inserted impedance, analysis of the Differential Mode Coupled Inductor (DMCI), design of three-limb boost, and grid-side inductors for an LCL filter, along with the design of a two-stage LCLC filter for CM-EMI compliance are presented in detail. A pareto-front-based optimization process is incorporated for final parameter extraction. Three-level NPC modules from Microsemi are adopted for converter assembly and integrated with FBBs for up to three channels interleaved. The experimental results including efficiency, circulating current suppression, power density, thermal distribution, EMI test and characterization, and loading effect are shown afterwards. A bypass switch mechanism is proposed to handle $N-1$ operation mode, which is unique to this topology.

In Chapter 3, the FBB idea is extended to cover alternate topologies. The key differentiator is the way the circulating current is suppressed. Particularly, the idea of localization of circulation and magnetic interconnection (using integrated coupled inductor (CI) + boost inductor) is proposed. Design guidelines pertaining to each variant are developed to compare the performance against the indirectly coupled FBB described in Chapter 2. A qualitative and quantitative comparison is drawn to understand the shortcomings of each variant.

Chapter 4 extends the idea of modular FBB to a DC-fed high-speed motor drive application for aerospace propulsion. A single turn AC filter with optimized RC network is developed to mitigate peak motor bearing currents. Modularity is ensured by masking the motor/load impedance via. the AC filter.
Surely the single turn inductor structure is preferred for weight-sensitive applications, such as more electric aircraft (MEA) architectures. Since the AC filter together with the motor load can affect the time constant of the load impedance, an abnormal operating condition was observed with short duty cycles, wherein the peak bearing currents would jump to approximately twice the nominal value. To account for this, a staggered PWM scheme is implemented on the converter end. The filter structure is extended over to the DC-side, where an integrated DM-CM core using a multi-turn heavy copper PCB solution is proposed. A novel DC busbar and filter assembly is developed to minimize ground inductance for Y-capacitors on DC-side. Static and dynamic tests on a 200-kW based three-level T-type inverter is conducted for functional verification and characterization.

A downside to high-density packaging and integration of a modular FBB is the impact on the high-frequency noise spectrum due to the influence of self and mutual filter parasitic elements. Chapter 5 presents these aspects through systematic design guidelines and simplified lumped models that can accurately capture high-frequency parasitic behavior, up to several tens of MHz. Analytical expressions for static capacitance and non-linear inductance calculations are used to develop multi-port models for single and coupled three-limb cores, toroidal cores, long cables, and motors (also shown in Chapter 4). A three-phase, three-level NPC-based back-to-back (BTB) bridge topology is used as the test case to perform sensitivity studies on the filter structure. Critical filter parameters that have stronger effects on the high frequency spectrum are identified and methods to desensitize these filter sub-components are proposed and tested.

Chapter 6 summarizes the dissertation and lists the conclusion based on the presented research.
Chapter 2. Secondary Loop Based Filter Building Block

This chapter presents the analysis and realization of a modular interconnected filter building block (FBB) operating under a single and multi-channel (parallel three-phase converter blocks) configuration without loss of attenuation to any harmonic components. Emphasis is given on the design of the CI and boost inductor. To achieve a modular scheme with interleaved operation, indirect coupling between converters is realized using the secondary loop (SL)-based interconnection with inserted impedance. Here SL serves as an additional path for average grid-side currents for N channels. A building block type configuration has been proposed using this topology, inspired by the power electronics building block (PEBB) nature. The purpose of the loop is to interconnect the parallel converters in series using an arrangement of CI. In addition, a boost inductor has been introduced in the secondary loop to realize a power factor correction (PFC) rectifier operation. The CI serves as the circulating current filter while reflecting channel currents toward the secondary loop. To meet conducted EMI limits, a two-stage LCLC filter has been integrated with the FBB by introducing the point of common coupling (PCC) connection between two stages. A design procedure is presented to meet power quality, circulating current, and EMI limits as per industry standards (EN-55011 and IEEE-519/1594). The proposed FBB has been characterized using 3L-NPC converters enabled with 1.2 kV SiC-based modules with comprehensive performance validation of up to three channels in parallel with a 15-kW power rating per channel.
2.1 Modeling for N Channels

2.1. Per-phase per-inverter sub-circuit modeling (for interconnected and non-interconnected structures)

As the work presented targets modular converters, the approach for modularity is taken using per-phase circuits. Two difficulties present to design a filter for N-parallel converter. First, level of attenuation for harmonics may change according to N. Especially, in practice, the number of modular converters is determined by the customer’s requirement and, in general, not known at the design stage. A state-space representation through $N \times N$ matrix offers an accurate mathematical description [46]. However, an approach with equivalent circuits can provide a physical insight for filter designers. Second, literature has investigated different filter topologies for paralleled converters, such as conventional CI [47], integration between boost inductor and CI [48][49][50], or integrated CIs [51]. For a comparative evaluation, a design must find filter parameters that can provide similar harmonic attenuation. This may not be straightforward considering flux-coupling of different structures. Furthermore, definition of terminologies such as circulating current or interpretation of flux-coupling vary depending on literature and may confuse readers.

\[
v_x(t) = \sum_{n=1}^{\infty} V_{0,n} \cos(n \omega_0 t + n \theta_0) + \sum_{m=1}^{\infty} V_{m,0} \cos(m \omega_c t + m \theta_c) + \sum_{m=1}^{\infty} \sum_{n=-\infty}^{\infty} V_{m,n} \cos((m \omega_c + n \omega_0) t + m \theta_c + n \theta_0)
\]  

(2.1)

\[
MI = \frac{V_{0,1}}{V_{dc}/2}
\]  

(2.2)

Holmes and Lipo [52] showed an analytical solution of carrier-based modulation as (2.1) where output frequency is $f_0 (= \omega_0/2\pi)$ and carrier frequency is $f_c (= \omega_c/2\pi)$. The phase of $f_0$ term is noted as $\theta_0$, and the phase of the carrier is noted as $\theta_c$. The magnitude of voltage at $mf_c+nf_0$ is labeled as $V_{m,n}$.
Modulation index \((MI)\) is defined as in (2.2). Any frequency component of pulse width modulation (PWM) voltage can be classified according to symmetrical component theory. Equation (2.1) shows that \(\theta_0(= 0, 2\pi/3, -2\pi/3)\) impacts the phase of harmonics. When \(n = 3p \pm 1\) (‘\(p\)’ is a nonzero integer), these frequency components form \(v^+_(x)(t)\). When \(n = 3p\), three-phase voltages are in-phase and form \(v^0_x(t)\). Therefore, any frequency component of PWM voltage can be classified according to symmetrical component theory. A frequency spectrum of PWM voltage with three-level space vector PWM (SVPWM) is shown in Fig 2.1. So, in time-domain waveforms, (2.3) holds for both \(v^+_(a)(t)\) and \(v^-_(a)(t)\), and the response of the circuit is similar between the two. They are often labeled as DM components.

\[
v^+_(a)(t) + v^+_(b)(t) + v^+_(c)(t) = 0 \tag{2.3}
\]

Equation (2.4) holds for \(v^0_(x)(t)\). The high frequency parts may disturb other equipment, and EMI standards refer to this as CM noise of a three-phase system.

\[
v^0_(a)(t) = v^0_(b)(t) = v^0_(c)(t) \tag{2.4}
\]

![Fig 2.1](image)

Fig 2.1 (a) Phasor diagrams for (a) positive, (b) negative, (c) zero sequence components, (d) three symmetrical components on frequency spectrum of PWM voltage
When the impedance is balanced, per phase analysis simplifies the circuit. An example circuit is shown in Fig 2.2(a). For DM currents ($i^{\pm}_x(t)$), there is no path for neutral nodes and these nodes are considered as the zero-potential, as shown in Fig 2.2(b). Note that the leakage inductance of CM choke
is neglected in Fig 2.2(b-left). The circuit for zero-sequence current \( i^0_x(t) \) can be similarly derived as Fig 2.2(b-right). Note that \( i^0_x(t) \) is defined as the zero-sequence current per-phase, and \( 3i^0_x(t) \) flows in the equivalent circuit. The phase-x current will be a combination of these two components as

\[
i_x(t) = i^+_x(t) + i^0_x(t)
\]

(2.5)

Fig 2.3 Phasor components for N-parallel converters

With the symmetrical interleaving, \( \theta_c \) in (2.1) is set to \( (j-1)2\pi N \) for \( j^{\text{th}} \) converter. As an example, the phasor diagram at \( f_{sw} \) is drawn in Fig 2.3. Only at multiple of \( NF_{sw} \), the phase of harmonic voltages is in-phase as Fig 2.3(b). The symmetrical component theory can be extended to any poly-phase system, including paralleled converters [53]. With \( N \)-parallel converters, there exist \( N \)-symmetrical components as shown in Fig 2.3. Among them, \( N-1 \) components are classified as circulating component \( (v_{\text{cir},xj}(t)) \) and (2.6) holds similar to (2.3). Only harmonics at \( qNF_{sw} \) (\( q \) is a positive integer) are in-phase \( (v_{\text{out},xj}(t)) \) and (2.7) holds similar to (2.4).

\[
\sum_{j=1}^{N} v_{\text{cir},xj}(t) = 0, x = a, b, c
\]

(2.6)

\[
v_{\text{out},xi}(t) = v_{\text{out},x2}(t) = ... v_{\text{out},xc}(t).
\]

(2.7)
Therefore, the per-converter circuit can be derived using symmetrical component theory like the per-phase circuit. For the positive and negative sequence circulating components \((v_{\text{cir},xj}^\pm(t))\), the node of ac bus in Fig 2.2(c) is zero-potential if the impedance of each converter is balanced. It can be converted into a single-phase circuit. In a similar manner, the same for zero sequence circulating components \((v_{\text{cir},xj}^0(t))\) can be derived from Fig 2.3(c). The per-converter circuit for \(v_{\text{out},xj}^\pm(t)\) and \(v_{\text{out},xj}^0(t)\) can also be easily derived. Combining the per-phase circuits and per-converter circuit, the proposed per-phase circuits are as shown in Fig 2.2(c). Using (2.3), (2.4), (2.6), and (2.7), the voltage source for each circuit can be derived from PWM voltage.

2.1.2 Example based on four per-phase circuits.

The per-phase circuit modeling procedure can be used for the estimation of peak value for circulating components. While the low frequency components of \(i_{\text{cir},xj}^\pm\) or \(i_{\text{cir},xj}^0\) are mitigated by control, the peak value of the high frequency components impacts the design of intercell transformers (CIs). The analytical solutions are derived for \(N = 2\) [50], [51], and \(N = 3\) [49] for a specific topology and modulation. However, it is not easy to derive the peak values for any \(N\) or each of topology and modulation schemes. Thanks to the simplicity of the proposed equivalent circuit approach, this can be easily estimated. With interleaving, all harmonics will become \(v_{\text{cir},xj}^\pm(t)\) or \(v_{\text{cir},xj}^0(t)\) in Fig 2.4, when \(N \to \infty\). For \(v_{\text{out},xj}^\pm(t)\) and \(v_{\text{out},xj}^0(t)\), DM voltage reference \((v_{\text{out},xj}^\pm)\) from kVA command, and zero sequence voltage reference \((v_{\text{out},xj}^0)\) will determine the magnitude and phase.

\[
\begin{align*}
\lim_{N \to \infty} v_{\text{cir},xj}^0(t) &= v_{c}^0(t) - v_{c}^0(t) \\
\lim_{N \to \infty} v_{\text{cir},xj}^\pm(t) &= v_{c}^\pm(t) - v_{c}^\pm(t)
\end{align*}
\]  

(2.8)

The integration of (2.8) is the flux-linkage corresponding to the circulating current when \(N \to \infty\) (\(\lim_{N \to \infty} \lambda_{\text{cir},xj}^0\), \(\lim_{N \to \infty} \lambda_{\text{cir},xj}^\pm\)). Based on PLECS® simulation result, Fig 2.4 compares the peak of \(\lambda_{\text{cir},xj}^0\) and \(\lambda_{\text{cir},xj}^\pm\) from \(N = 2\)–\(9\) to that of \(N \to \infty\) under three-level SVPWM.
Fig 2.4 Peak circulating current flux vs. Number of parallel converters

Fig 2.5 Structure of magnetic circuit and effective impedance table for $i_{out,x}$, $i_{in,x}$, $i_{circ,x1}$, and $i_{circ,x2}$. (a) DM CI [6]. (b) Four-limb CI with integrated boost inductance [5]. (c) Monolithic configuration of CI with integrated boost inductance [4].
The proposed $N$-parallel converter modeling procedure is verified using CM circulating currents as an example for two and three channels. The peak CM circulating current (CMCC) obtained from per-phase models can match well with the experimental results in Fig 2.7.

Fig 2.6 (a) Simulation waveforms of $i_{\text{out},x1}$, $i_{\text{circ},x1}$, and $i_{\text{circ},x1}$ for different $N$.

Fig 2.7 Experimental waveforms of currents for $N=2$ and $N=3$

The per-phase models can be used for qualitative comparison of interleaved/parallel filter structures.

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2.1.3 Modular filter topology selection – Review of state-of-the-art

An example of a modular parallel system employing LCL filter is shown in Fig. 2.8. Here the LCL filter is constructed using a DM-equivalent circuit, with the LCL components denoted by $M_{dm1}$, $M_{dm2}$, $C_{dm1}$ and $R_d$. Ideally, a harmonic line filter for a single converter can also be used with a parallel (non-interleaved) multi-converter system. To reduce the size of such harmonic filters, interleaving is commonly used to achieve superior total harmonic distortion (THD) performance at the expense of high circulating current. The impact of interleaving on passive component weight has been studied extensively in [48][54]. In essence, the principle of harmonic cancellation due to interleaving therefore creates avenues for filter size reduction [55]. Both the LCL filter first stage inductor ($M_{dm1}$) and damping resistor ($R_d$) along with the size of DM capacitor ($C_{dm1}$) can be reduced by placing them on the grid-side as shown in Fig. 2.8. But to solve the problem of inter-channel circulating current, inter-channel transformers (ICTs), or coupled inductors (CIs) with mutual inductance ($M_{ci}$), are added in Fig. 2.8, which imposes a higher weight and volume requirement on the converter-side filter. Gohil et. al. proposed unique magnetic integration schemes [49][50][56] to deal with circulating current. If unchecked, this component can create additional losses on the converter-side, mostly conduction loss, which could compromise system efficiency. As such, three-phase filters for interleaved converters occupy roughly 40-50% of the total system volume in a conventional grid-tied system. A key driver for modular interleaved FBB is a modular circulating current filter. Prior articles [57][58][59][60] describe ways to handle the circulating current between converters, either using inter-channel magnetic coupling in [59], or using a localized circulation mechanism through an LC trap method as proposed in [60]. However, due to the imposing limitations of these methods specified in Table 2-1 and [61][62], the indirect form of coupling using secondary loop interconnection has been investigated as a potential modular FBB for interleaved converters. Besides circulating current, the EMI filter consumes a major chunk of total filter volume. While several EMI filter structures are proposed [63][64][65][66] to
handle low and high frequency CM noise, the implications with interleaving and trade-offs in design with CM circulation are not considered in detail. Additionally, the behavior with paralleling and impact from asymmetry on CM circulation and EMI are neglected.

Fig. 2.8 Conventional multi-channel interleaved converters using magnetic coupling – DM equivalent circuit.

Table 2-1 State of the Art filter structures for interleaved converters.

<table>
<thead>
<tr>
<th>Topology</th>
<th>Feature</th>
<th>Limitation</th>
<th>Modularity</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cyclic cascade/shunt[72]</td>
<td>Cyclic arrangement of CI</td>
<td>At least three channels needed for valid arrangement</td>
<td>No</td>
</tr>
<tr>
<td>Baseline LCL [57][72]</td>
<td>Simple implementation, no CI</td>
<td>High volume of boost inductor for circulating current mitigation</td>
<td>Yes</td>
</tr>
<tr>
<td>Monolithic [59][78]</td>
<td>Multi-channel CI and boost integration</td>
<td>Loss of attenuation due to airgaps between CIs</td>
<td>Partially</td>
</tr>
<tr>
<td>Whiffletree</td>
<td>Multi-channel CI and boost integration</td>
<td>Loss of attenuation and only valid when channels can be reduced in the form $2^N$</td>
<td>No</td>
</tr>
<tr>
<td>LC Shunt / Localization [60]</td>
<td>Localize circulation between channels</td>
<td>Low frequency component on inner first stage CM choke</td>
<td>Partially</td>
</tr>
<tr>
<td>Secondary loop [77]</td>
<td>Bypass load harmonics</td>
<td>Careful design of magnetic coupler is needed</td>
<td>Yes</td>
</tr>
</tbody>
</table>
Fig 2.9 Two-channel CI configurations (a) Cyclic cascade, (b) Cyclic-shunt, (c) Whiffletree and (d) Secondary loop

Table 2-2 Design specifications and parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>System Rating</td>
<td>460 VAC / 60 Hz</td>
</tr>
<tr>
<td>Rated Power</td>
<td>45 kW (3 X 15 kW)</td>
</tr>
<tr>
<td>DC Link Voltage</td>
<td>750 V</td>
</tr>
<tr>
<td>Modulation Scheme</td>
<td>SVPWM</td>
</tr>
<tr>
<td>System Rating</td>
<td>460 VAC / 60 Hz</td>
</tr>
<tr>
<td>Rated Power</td>
<td>45 kW (3 X 15 kW)</td>
</tr>
</tbody>
</table>

Fig 2.10 Modular SL-FBB structure with DM and filter CM components, circuit with $N = 3$

2.1.3 Basic principle and impedance insertion of secondary loop

First, the concept of indirect coupling and benefits are reviewed. The DM circuit of the converter-side FBB is shown in Fig 2.11. For simplicity, two channels ‘x’ and ‘x+1’ are shown. Each channel has a CI, which provides an indirect coupling between converters using the secondary winding, hence the
name secondary loop. This winding connects all CIs in series. Note that a boost inductor is inserted in series with the secondary loop as well.

Fig 2.11 Conventional multi-channel interleaved converters using magnetic coupling – DM equivalent circuit

The basic principle of secondary loop filter structure is to reflect the main channel currents toward the secondary winding, such that the phase shifted harmonics within the loop cancel out. This results in a scalable filter topology, which results in lower filter loss as the number of parallel converters increases. To understand this, first the structure of the CI is evaluated. The inter-channel coupling is achieved using the mutual inductance of the differential mode CI (DMCI) \([51]\), \(M_{\text{dmci}}\) in Fig 2.11(b). Notably, other variations of the CI such as common mode CI (CMCI) or single-phase CI can be used as well. A DMCI, however, can decouple the flux components created by low and high frequency zero-sequence circulating components. In this regard, only the DM harmonics are translated toward the secondary loop due to the three-limb structure. Consequently, certain DM harmonics can be blocked by adding a boost inductor \(M_{\text{dm1}}\) within the loop. The design of DMCI is an integral aspect for proper
functioning of this structure, mainly because it caters to blocking circulation, as well as reflecting channel currents.

The six windings, three for main channel currents \( (i_{dm,Ax}, i_{dm,Bx} \text{ and } i_{dm,Cx}) \) and three for secondary loop currents \( (i_{sec,A}, i_{sec,B} \text{ and } i_{sec,C}) \), are used to construct the DMCI as shown in Fig 2.11(b). While the windings corresponding to the same phase have 100% coupling, the windings between adjacent phases have 50% coupling. This results in the impedance matrix, with ‘k’ being the coupling coefficient between windings is defined as per (2.9). Here \( L_s \) is the self-inductance of each winding given by the expression in (2.10). \( M_{dmci} \) is defined in (2.10) and is the effective mutual inductance to DM circulating components. The reluctance of each vertical limb and T-bar is given by \( R_{leg} \) and \( R_t \) respectively, as per Fig 2.11(b). It was found that the impact from T-bars can be neglected, considering a single layer winding structure with relatively larger legs. The DMCI in this case behaves like a transformer, such that the mutual inductance or magnetizing inductance couples the primary side DM current of channel ‘x’ \( i_{dm,Ax} \) to the secondary side as \( i_{sec,A} \), shown in Fig 2.12. The same is true for other phases as well. Note that the turns ratio between the primary and secondary side of the DMCI is assumed as unity but can be extended to any turns ratio. Considering only DM components, the channel and secondary loop currents follow the rule in (2.11).

\[
\begin{bmatrix}
\lambda_{phiAx}^s \\
\lambda_{phiBx}^s \\
\lambda_{phiCx}^s \\
\lambda_{secAx}^s \\
\lambda_{secBx}^s \\
\lambda_{secCx}^s
\end{bmatrix} = \begin{bmatrix}
L_s & (k-0.5)L_s & (k-0.5)L_s & (k-0.5)L_s & (k-0.5)L_s & (0.5-k)L_s \\
(k-0.5)L_s & L_s & (k-0.5)L_s & (k-0.5)L_s & (k-0.5)L_s & (0.5-k)L_s \\
(k-0.5)L_s & (k-0.5)L_s & L_s & (0.5-k)L_s & (0.5-k)L_s & (k-0.5)L_s \\
(k-1)L_s & (0.5-k)L_s & (0.5-k)L_s & L_s & (k-0.5)L_s & (k-0.5)L_s \\
(0.5-k)L_s & (k-1)L_s & (0.5-k)L_s & (0.5-k)L_s & L_s & (k-0.5)L_s \\
(0.5-k)L_s & (0.5-k)L_s & (k-1)L_s & (0.5-k)L_s & (k-0.5)L_s & L_s
\end{bmatrix} \begin{bmatrix}
i_{dm,Ax} \\
i_{dm,Bx} \\
i_{dm,Cx} \\
i_{sec,A} \\
i_{sec,B} \\
i_{sec,C}
\end{bmatrix}
\]

\( 0 < k < 1/2 \)
\[
L_s = \frac{2}{3} \frac{N_n^2}{R_{leg}}; \quad R_{leg} \gg R_i
\]
\[
Let \quad M_{dmci} = \frac{N_n^2}{R_{leg}}; \quad M_{dmci} = \frac{3}{2} L_s
\]

Using (2.11) and simplifying the matrix in (2.9), the expression for flux linkage \(\lambda_{sec, A}\) due to phase A of secondary winding of channel ‘x’ can be written as shown in (2.12).

\[
\begin{align*}
(i_{dm, Ax} + i_{dm, Bx} + i_{dm, Cx}) &= 0 \\
(i_{sec, A} + i_{sec, B} + i_{sec, C}) &= 0 \\
\lambda_{PriA,x} &= -\lambda_{SecA,x} \\
\lambda_{SecA,x} &= M_{dmci}i_{sec, A} - M_{dmci}i_{dm, Ax} = M_{dmci}i_{dm, A, x(circ)}
\end{align*}
\]

Fig 2.12 DM circuit for secondary loop-based interconnection
The expression in (2.12) for phase A can be rewritten for all channels (N). Using circuit simplification, the final expression for secondary loop current is given by (2.13). From this expression, it can be seen that the total current in the secondary loop \(i_{sec,A}\) is the average current on the grid-side, \(i_{dm,A,grid}/N\), which is also the load current per channel. This can be visualized from the phasor diagram in Fig 2.13. Since the phase-shifted circulating currents are cancelled within the loop (green phasor in Fig 2.13), only the load harmonics are present and constitute the secondary loop current.

\[
i_{sec,A} = \sum_{1}^{N} \frac{i_{dm,A,x}}{N} = i_{dm,A,x(load)} = \frac{i_{dm,A,grid}}{N}
\]

Substituting (2.13) back into (2.12), we have the expression in (2.14),

\[
\lambda_{Sec,A,x} = M_{dmci} \frac{\sum_{1}^{N} i_{dm,A,x}}{N} - M_{dmci}i_{dm,A,x} = M_{dmci}i_{dm,A,x(circ)}
\]

Equation (2.14) implies that the mutual inductance of the DMCI, \(M_{dmci}\), provides attenuation to the DM circulating current, \(i_{dm,A,x(circ)}\), seen by phase A of channel ‘x’ and is constant irrespective of the number of channels. This is crucial from the point of view of modularity in FBBs.
2.2 Design for Circulating Current Control and THD Compliance

2.2.1 Design of magnetic coupler using DMCI and DM inductor

Since the secondary loop current is ripple free and comprised of only the fundamental grid-side components, it is possible to add a boost inductor in the loop at the expense of lower loss. However, this imposes a design constraint on the DMCI, which will be evaluated in this section. The net voltage drop across phase A secondary windings of all channels adds up to zero as per (2.15).

\[
\frac{d}{dt} \sum_{1}^{N} \lambda_{\text{Sec},A,x} + N M_{dm1} \frac{d}{dt} i_{\text{sec},A} = 0
\]  

(2.15)

Using (2.13) in (2.15), we have Equation (2.16)

\[
i_{\text{sec},A} = \frac{M_{dmci}}{M_{dmci} + M_{dm1}} i_{dm,Ax} \approx i_{dm,Ax} \bigg|_{M_{dmci} >> M_{dm1}}
\]  

(2.16)

Eq. (2.16) is used to describe the dynamics of secondary loop current with inserted impedance, \(M_{dm1}\) per channel. Under the condition that the magnetizing impedance \(M_{dmci}\) is large enough compared to inserted boost impedance, the secondary loop current (\(i_{\text{sec},A}\)) and channel currents (\(i_{dm,Ax}\)) are the same as shown in the simplification in (2.16). Another important result is that the secondary loop current is free from circulating harmonics under symmetric interleaved operation and only comprised of the average grid-side current (\(i_{dm,Agrid}/N\)). As a result of this, the core losses [37][38] on the boost inductor in the loop can be smaller, due to absence of dominant switching ripple besides the \(N^{th}\) switching harmonic ripple [55] (which are in-phase). If the circulating current is blocked by the mutual inductance of the DMCI, then the channel current will be reflected on the secondary loop current as shown in Fig 2.14 under two-channel operation.
Fig 2.14 Measured channel currents and secondary loop currents with loading ratio of 10 ($f_{sw} = 31.25$ kHz)

From Fig 2.14, the secondary loop and channel currents have the same effective switching ripple and the dominant first order switching ripple is absent. Since the secondary loop current also generates the volt-second across the boost inductor, the corresponding flux ripple and the rate of change of flux will be lower.

**For the design of DMCI two main considerations are as under:**

1. Selection of magnetizing impedance of the DMCI – based on the circulating current requirement and loading effect

2. Selection of boost inductor based on the THD and loading effect of DMCI.
2.2.2 Impact of loading effect and leakage inductance

Due to the loading effect, the DMCI should be carefully designed to avoid any possible saturation due to low frequency (fundamental) components. From simulation and experimental studies in Fig 2.15, it was found that the minimum value of the loading ratio ($M_{dmci}/M_{dm1}$) can be set to 10 for reasonable performance. The impact of a boost inductor on the flux density across phase A limb of DMCI, i.e., $B_{dmci}$, can be seen from (2.17). The loading impact is shown in simulation and quantifies well with the analytical value per Fig 2.15.

$$B_{dmci} = \frac{M_{dm1}M_{dmci}}{(M_{dmci} + M_{dm1})} n_A i_{dm, Ax}$$  \hspace{1cm} (2.17)

![Fig 2.15](image)

Fig 2.15 Peak flux density of DMCI as a function of loading ratio (a) Time domain plot for two cases with different loading ratios, (b) Correlation between simulated and calculated peak flux density and (c) Impact of non-linear permeability and switching frequency on loading ratio compared to original design at 32 kHz.

Where $A_e$ is the core area, the fundamental component ($i_{load, dm, Ax}$) through the secondary winding does not change, but the circulating harmonic content ($i_{circ, dm, Ax}$) depends on the number of channels and changes within the loop. Ideally, as $N$ increases, the circulating flux components within DMCI will increase. It is interesting to note that due to the non-linear nature of permeability with frequency, the
magnetizing inductance decreases with the switching frequency per Fig 2.15(b). This can result in imperfect cancellation of higher-order switching harmonics within the loop as the mutual inductance drops significantly. Thereby the higher-order switching harmonics are not reflected completely to the secondary side.

While the analysis in the previous section(s) assumes tight coupling between phases, it is interesting to note the behavior in the presence of leakage inductance between phases. The leakage coefficient ‘k’ is shown in (2.18) and is used to define the loss of coupling between phases. Based on these definitions, the effective magnetizing impedance and boost impedance due to leakage coefficient ‘k’ is defined in (2.19, 2.20). Note that the effective impedance to circulation does not change as the leakage inductance provides additional impedance to circulation. The impact of leakage is seen on the peak-peak current ripple, and the loading effect shown in Fig 2.16. The increase in peak $B_{pk}$, DMCI is due to lower loading ratio produced by higher $M_{dmci, eff}$ (2.19), while the decrease in peak-peak ripple comes from higher $M_{dm1, eff}$ (2.20).

\[
\begin{bmatrix}
\hat{\lambda}_{PhIAx} \\
\hat{\lambda}_{PhBX} \\
\hat{\lambda}_{PhCA} \\
\hat{\lambda}_{SecAX} \\
\hat{\lambda}_{SecBX} \\
\hat{\lambda}_{SecCA}
\end{bmatrix} = 
\begin{bmatrix}
L_i & (k-0.5)L_i & (k-0.5)L_i & (k-1)L_i & (0.5-k)L_i & (0.5-k)L_i \\
(k-0.5)L_i & L_i & (k-0.5)L_i & (k-1)L_i & (0.5-k)L_i & (0.5-k)L_i \\
(k-0.5)L_i & (k-0.5)L_i & L_i & (0.5-k)L_i & (k-1)L_i & (0.5-k)L_i \\
(k-1)L_i & (0.5-k)L_i & (0.5-k)L_i & L_i & (k-0.5)L_i & (k-1)L_i \\
(0.5-k)L_i & (k-1)L_i & (0.5-k)L_i & (k-0.5)L_i & L_i & (k-0.5)L_i \\
(0.5-k)L_i & (0.5-k)L_i & (k-1)L_i & (0.5-k)L_i & (k-0.5)L_i & L_i
\end{bmatrix}
\begin{bmatrix}
i_{dm,IA} \\
i_{dm,BX} \\
i_{dm,CI} \\
i_{sec,A} \\
i_{sec,B} \\
i_{sec,C}
\end{bmatrix}
\]

(2.18)

\[
0 < k < 1/2
\]

\[
M_{dmci, eff} = M_{dmci} \left(1 - \frac{2}{3}k\right)
\]

(2.19)

\[
M_{dm1, eff} = M_{dm1} + \frac{2}{3}kM_{dmci}
\]

(2.20)
Fig 2.16 (a) Peak flux density of DMCI as a function of leakage inductance, (b) Peak-peak switching ripple as a function of leakage inductance.

2.2.3  Impact on THD

This section covers how $L_{sec}$ may change according to N. The size of the filter inductor should be designed to meet the THD limit and to provide sufficient slope for current control. When the controllability does not significantly influence the design, there are two factors that dominantly impact the size of $L_{sec}$. First, with increasing N, interleaving leads to more cancellation of harmonic current. Thus, a smaller value of $L_{sec}$ may meet the THD limit. On the other hand, the equivalent inductance per channel decreases by $1/N$. If this factor dominates, more inductors must be inserted to meet the THD limit. A simulation study is performed to analyze a change of $L_{sec}$ to meet the same THD. The simulation setup per Table 2-2 is used. The value for total $M_{dmi}$ in the loop is set to be 320 $\mu$H. For different numbers of the converters, the THD with an open loop control is simulated. Frequency domain waveforms are shown in Fig 2.17(a) for $N = 2$ and $N = 9$. A summary of THD values for different N is shown in Fig 2.17(b). From a modular filter design point of view, clearly $N=1$ is the worst case for sizing of the boost inductor in the loop.
Table 2-3 Filter parameter definitions

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{dmci}$</td>
<td>Mutual inductance between phases of CI</td>
</tr>
<tr>
<td>$M_{dm1}$</td>
<td>Mutual inductance between phases of first stage LCL DM inductor</td>
</tr>
<tr>
<td>$M_{cm1}$</td>
<td>CM inductance of first stage CM choke</td>
</tr>
<tr>
<td>$M_{dm2}$</td>
<td>Mutual inductance between phases of second stage LCL DM inductor</td>
</tr>
<tr>
<td>$M_{cm2}$</td>
<td>CM inductance of second stage CM choke</td>
</tr>
<tr>
<td>$C_{dm1}$</td>
<td>First stage DM capacitor</td>
</tr>
<tr>
<td>$C_{dm2}$</td>
<td>Second stage DM capacitor</td>
</tr>
<tr>
<td>$C_{cm1}$</td>
<td>First stage CM capacitor</td>
</tr>
<tr>
<td>$C_{cm2}$</td>
<td>Second stage CM capacitor</td>
</tr>
<tr>
<td>$R_d$</td>
<td>Damping resistor</td>
</tr>
<tr>
<td>$C_{stray}, L_{stray}$</td>
<td>Stray load capacitance and inductance</td>
</tr>
<tr>
<td>$C_{AC-GND}, C_{HS-GND}$</td>
<td>Equivalent AC node and heat-sink to ground capacitance</td>
</tr>
</tbody>
</table>

2.2.4 Impact on CM and DM circulation

The circulating current problem is mitigated by the DMCI $M_{dmci}$ (for DM circulation) and CM choke $M_{cm1}$ (for CM circulation), which are parts of converter-side FBB. The effective impedance to circulation does not change significantly and as such, the peak circulating current is the same with respect to N. This is shown in detail in reference [9]. It was found that the peak circulating flux lies
between ±3% error band beyond four channels in parallel. Hence N=2, (shown in previous section) is considered as the worst case for circulating current filter design. Since there is no standard that defines the peak circulating current limit, the semiconductor conduction loss and filter loss can be used to design the optimal circulating current filter. The trade-off between losses and CMCC filter volume (for example: $M_{cm1}$) is shown in Fig 2.18. While the semiconductor losses decrease with higher $M_{cm1}$ due to drop in peak CMCC, the total loss and volume of $M_{cm1}$ increases. The impact of switching frequency is evident as well. So there exists an inverse relationship between volume of $M_{cm1}$ and converter losses. Note that the first stage CM choke is prone to low frequency / DC bias due to inter-channel asymmetry. For this reason, a special grade of nanocrystalline core FT-8K50D is recommended, where the drop in permeance with frequency is relatively lower than other grades. A similar trend is also seen with DMCI for DM circulation.

![Driving factor for circulating current filter parameter selection](image)

Fig 2.18 Driving factor for circulating current filter parameter selection, (a) Loss volume map of CM inductors (b) Trade-off between converter and circulating current filter loss

As for the DMCI, the design is based on peak DM circulating current (DMCC) minimization and high loading ratio. Ideally, higher $M_{dmci}$ can achieve both. For high efficiency consideration with hard switching, the switching frequency is usually limited to less than 100 kHz. Since the permeability of the magnetic material for the DMCI should not drop significantly until 100 kHz, amorphous cores from
METGLAS are selected to construct the DMCI. Based on the parametric sweep per Fig 2.19, the optimal design point lies near 32 kHz. From Fig 2.19, the filter losses and volume decrease with higher switching frequency. However, increase in switching losses with switching frequency limits the design point near 32 kHz.

![Fig 2.19](image)

Fig 2.19 (a) Loss-volume map of the DMCI and boost inductor for N = 3, (b) Trade-off between DMCI and converter loss vs. switching frequency for fixed value of DMCI and $M_{dm1}$

2.3 Design for EMI Mitigation using Two-stage LCLC Filter

2.3.1 Parameter selection for LCLC filter

A two-stage LCLC filter is chosen due to superior attenuation at high frequency [67]. Based on the per-phase, per-inverter circuit in Fig 2.20(a), where the converter parasitic capacitances were measured using a similar approach in [9], the first stage CM choke $M_{cm1}$ provides impedance to CM circulation and CM load frequency components. The remaining grid-side parameters ($M_{cm2}$, $C_{cm2}$ and $C_{cm1}$) are
adjusted to meet the EMI noise limit at higher frequency (per EN-55011 Class A). Fig 2.20 shows the calculated attenuation $G_{cm}$ of the CM filter, which decreases gradually up to the several MHz range, beyond which the EPC of CM chokes ($EPC_{cm1}$ $EPC_{cm2}$) and ESL of CM capacitors ($ESL_{cm1}$, $ESL_{cm2}$) comes into play. The grid-side CM filter parameters alter the attenuation in low frequency range (150 kHz – 5 MHz); therefore, these values are swept in the optimization routine to determine the best combination in terms of lowest volume and EMI noise margin. Note that only self-parasitic components are considered, and reasonable values are assumed for the design optimization process. Since this design shall yield a larger value for the first stage CM choke $M_{cm1}$ (targeted toward CM circulation) compared to $M_{cm2}$ (targeted toward higher frequency attenuation), the EPC of $M_{cm1}$ tends to be larger than $M_{cm2}$.

![Fig 2.20 (a) CM equivalent circuit for $N$ channel system, (b) Calculated attenuation for combinations of $M_{cm2}$ and (c) $C_{cm1}/C_{cm2}$, for fixed $M_{cm1} = 4$ mH](image)

$$v_{cm,load} = \frac{1}{N} \sum_{x=1}^{N} v_{cm,x}$$

$$f_{ref1}, f_{ref2}, f_{ref3}, f_{ref4}$$

$$C_{cm1} = C_{cm2} = 16.75 \text{ nF}$$

$$C_{cm1} = 2 \text{ mH}, 0.2 \text{ mH}$$

$$C_{cm2} = 33 \text{ nF}, 3.5 \text{ nF}, 1.2 \text{ mH}$$

$$M_{cm1} = 4 \text{ mH}$$
The behavior with number of channels ‘N’ is studied in Fig 2.21 to determine the worst-case channel count from an EMI filtering aspect. With paralleling, the effective impedance to CM noise decreases is evident from the calculated CM transfer gain $H_{cm}$ of the filter and converter, with respect to $N$ per Fig 2.21(b). The simulation results in Fig 2.21(a) corroborates this effect. So, $N = N_{max}$ is chosen as the selected worst-case operating point for CM-EMI filter parameter calculation for modularity.

![Simulated CM noise spectra for variable N](image1)

**Fig 2.21 (a) Simulated CM noise spectra for variable N (b) Calculated transfer gains for variable N**

The design process for $N = N_{max}$ follows as under:

1) **Solution sets for $M_{cm1}$**: The parameter $M_{cm1}$ is dictated by CMCC shown earlier. It is driven by Fig 2.18, where the conduction loss on the module dictates the size of the first stage CM choke. Since there is no hard limit on peak-CMCC, a loss-volume map is obtained.
2) **Selection of** \( M_{cm2} \): Subsequently, the calculated attenuation for combinations of \( C_{cm1} \), \( C_{cm2} \), and \( M_{cm2} \) under fixed value of \( M_{cm1} \) can be calculated and shown in Fig 2.20. The maximum CM capacitance to ground was set to 33 nF.

3) **Combine 1) and 2)** under different peak-CMCC conditions and \( f_{sw} \). The loss-volume map will dictate the final CM parameter selection.

The evaluation results for \( N_{max} = 3 \) presented in Fig 2.22. Strictly from EMI mitigation point of view (seen from Fig 2.22(a)), a switching frequency closer to 48 kHz results in the highest attenuation. This is because the dominant harmonics (6\( f_{sw} \)) appear relatively in the mid-frequency range, where the attenuation is significantly higher compared to other switching frequencies. Therefore, at 48 kHz frequency, the second stage CM filter volume for any given \( M_{cm1} \) can be lowest. In addition, \( M_{cm1} \) itself can be lower due to lower peak CMCC \( (i_{cm,Ax,(circ)}) \) compared to 16 kHz and 32 kHz options. From a system optimization point of view, the device losses should be accounted for as well, which will eventually dictate the filter parameters. Lower switching frequency is ideal in this regard (low switching loss), but contributes to high \( M_{cm1} \) volume/value and losses due to higher peak \( i_{cm,Ax,(circ)} \). Consequently, a larger \( M_{cm1} \) results in lower \( M_{cm2} \) to meet the EMI standard under the same noise margin. Fig 2.22(b) shows this effect.

The trade-offs and the trajectory of optimal CM filter volumes under different switching frequencies, peak-CMCC and same noise margin requirements is shown in Fig 2.22(c). The parabolic nature of the CM choke volume and loss occurs due to two main reasons. First, a higher switching frequency yields the lowest CM filter volume but highest switching loss; therefore, the overall system loss is high. Second, the lowest switching frequency yields the highest CM filter volume, therefore, higher filter loss resulting in larger converter loss. The minimum occurs near 32 kHz where a good balance between
converter and filter loss is achieved. The trajectory of solutions for different switching frequencies is shown by solid lines in Fig 2.22(c).

![Graph showing parametric variation of CM noise attenuation with respect to \( M_{cm2} \) and \( f_{sw} \).](image)

**Fig 2.22 (a)** Parametric variation of CM noise attenuation with respect to \( M_{cm2} \) and \( f_{sw} \), (b) Volume map of CM inductors vs. \( f_{sw} \) and (c) Loss-volume map of CM inductors vs. total converter loss

### 2.3.2 Core material and PCC location impact

The implications of the split-up between grid-side and converter-side FBB through the PCC can be seen on the EMI spectrum under asymmetric operating conditions. Besides providing a low impedance pass for circulating current, the additional CM filter stage beyond the PCC compensates for the effect of inter-channel asymmetry. A simplified representation of the CM circuit is shown in Fig 2.23(a). Such
simplification allows for the intuitive understanding of the impact of asymmetry between converter-
side impedance $\Delta Z_{\text{cm,conv}}$.

$$i_{\text{CM, LISN}} = \frac{v_{\text{cm,x,load}} + \left( \frac{N\sum_{x=2}^{N} v_{\text{cm,x}}}{Z_{\text{eq,conv}}} + \frac{N\Delta Z_{\text{cm,conv}}}{Z_{\text{eq,conv}}} \right)}{Z_{\text{eq,grid}} \left( N + (N-1) \frac{\Delta Z_{\text{cm,conv}}}{Z_{\text{eq,conv}}} + \frac{\Delta Z_{\text{cm,conv}}}{Z_{\text{eq,grid}}} \right)}$$

$$(2.21)$$

$$Z_{\text{eq,grid}} = \frac{Z_{\text{cm,grid}}}{N} + \frac{1}{N} \sum_{x=2}^{N} v_{\text{cm,x}}$$

Circulating component = $$\frac{\Delta Z_{\text{cm,conv}}}{Z_{\text{cm,conv}}} \sum_{x=2}^{N} v_{\text{cm,x}}$$

$$(2.22)$$

The total LISN CM noise is given by the expressions in (2.21, 2.22). Where net grid-side CM impedance is represented by $Z_{\text{eq,grid}}$ defined in (2.22), $Z_{\text{LISN}}$ being the equivalent per phase LISN impedance, $Z_{\text{cm,grid}}$ is the second stage grid-side equivalent per phase CM impedance and $Z_{\text{cm,conv}}$ is the equivalent per-phase converter-side CM impedance. From (2.21), the numerator indicates that a non-circulating component given by (2.22) will be seen on the LISN terminal. A MATLAB-based EMI simulation was performed on $N_{\text{max}} = 3$, with asymmetry induced on one of the channels in the form of a higher CM impedance (+5%).

The resulting spectrum shows that certain circulating harmonics will be seen on the LISN terminal, which is contrary to the ideal case. By placing an additional second stage LC filter ($M_{\text{cm2}}$ and $C_{\text{cm2}}$) on the grid-side, which is representative of $Z_{\text{cm,grid}}$ in Fig 2.23(a), those circulating harmonics on LISN-side can be compensated as shown in Fig 2.23(b). Therefore, splitting the FBB into grid-and converter-side is recommended for loss minimization and compensation of asymmetry.
Fig 2.23 (a) Simplified CM-equivalent circuit for N channel system, (b) Impact of asymmetry and compensation using grid-side impedance (N=3).

Fig 2.24 (a) Impact of mismatched FBB on circulating current suppression (b) Impact of mismatched FBBs on EMI spectrum.

As for the core material, it was found through experimental results that the low frequency circulating components (caused by filter and converter parameter mismatch) can potentially result in saturation of
converter-side CM choke \( M_{cm1} \). A specific grade of commercial nanocrystalline core with constant permeability (low initial permeability) over wide-band frequencies and relatively lower drop-in permeability with DC bias is recommended for the converter-side choke \( M_{cm1} \). The impact is seen from Fig 2.24(a) between two different variants of nanocrystalline core, but with the same permeability and area product.

2.3.3 System assembly and packaging

The optimal switching frequency of 32 kHz was chosen based on efficiency and power density requirements c.f. Fig 2.25, while at the same time meeting the power quality and EMI standard with low filter volume. A prototype using a 3L-NPC converter, rated at 15 kW per channel, was tested using the proposed topology, per the filter parameters obtained from the optimization in Table 2-4. The key building block architecture is highlighted in Fig 2.26. The external secondary loop interconnections can be reconfigured using cables based on the number of channels.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>( M_{dmi} )</td>
<td>600 ( \mu )H (Amorphous 3-Limb customized)</td>
</tr>
<tr>
<td>( M_{dm1} )</td>
<td>50 ( \mu )H (Amorphous 3-Limb customized) per</td>
</tr>
<tr>
<td>( M_{cm1} )</td>
<td>4 mH (FT-8K50D F7555G Nanocrystalline)</td>
</tr>
<tr>
<td>( M_{dm2} )</td>
<td>20 ( \mu )H (Amorphous 3-Limb customized)</td>
</tr>
<tr>
<td>( M_{cm2} )</td>
<td>800 ( \mu )H (FT-3KL F3724E, Nanocrystalline)</td>
</tr>
<tr>
<td>( C_{dmi} )</td>
<td>3.5 ( \mu )F (B32674D1405K Film Capacitor)</td>
</tr>
<tr>
<td>( C_{dm2} )</td>
<td>68 nF (R413I222050M1M Film Capacitor)</td>
</tr>
<tr>
<td>( C_{cm1} )</td>
<td>22 nF (F881BC153M300C Film Capacitor)</td>
</tr>
<tr>
<td>( C_{cm2} )</td>
<td>13 nF (R474I268050A2K Film Capacitor)</td>
</tr>
<tr>
<td>( R_d )</td>
<td>0.25 ( \Omega ) (Damping Resistor)</td>
</tr>
</tbody>
</table>
Due to this form of electrical interconnection using secondary winding, the disadvantages from a mechanical interconnection can be avoided [59]. The internal structure is shown in Fig 2.26(c). A vertical stack-up was found to be the most optimal assembly option for the design, considering the per-channel FBB layout and the interconnections.

![Graph showing Power Density vs. Efficiency Map for N = 3, (Theoretical) near the selected design point](image1)

![Loss Breakdown for SL-FBB Components](image2)

Fig 2.25 (a) Loss-Volume map for the proposed topology, Power Density vs. Efficiency Map for N = 3, (Theoretical) near the selected design point, (b) Loss breakdown of filter and converter
Fig 2.26 (a) FBB and converter block per channel (b) Secondary loop FBB with three channels – Top: Version 2.0 with packaged FBB and converter block and Bottom: Version 1.0 internal structure of FBB(s) showing the interconnection
2.4 Static and Dynamic Characterization

2.4.1 Electrical characteristics

A grid-side average current control scheme was adopted in this dissertation [67]. A dead time of 200 ns and switching frequency of 32 kHz were used. To account for larger drift in Neutral Point Voltage (NPV) during transient load changes, the scheme from [68] was used. The three-phase operating waveforms under three channels is shown in Fig 2.27(top). The measured phase A current THD is shown in Fig 2.27(bottom), and as expected, it improves with higher channels.

The phase A currents under variable channels is shown in Fig 2.28, along with the peak-peak ripple content in the zoomed subplots for each case. Firstly, from Fig 2.28, it can be seen that the lower order harmonics for the converter current decreases as the number of converters in parallel increases, i.e. the converter current THD improves with N. Secondly, the secondary loop current ripple is identical to the converter current ripple seen from the zoomed shots. These two points are indicative of the reduction in current ripple in the converter current, as the number of parallel converters increases from N=2 to N=3, indicating the DMCI and CM choke provide sufficient attenuation to block circulating harmonics. This implies that the voltage and current stress on the LCL filter capacitor and damping resistor will be smaller with higher N, since the secondary loop current is essentially the load-side current from (2.13). Lower ripple also implies lower conduction loss and filter loss, which improve scalability to higher power/channels.
Fig 2.27 THD under different channel configurations

Fig 2.28 Phase A currents under (a) Single channel operation, (b) Two-channel operation (c) Three-channel operation (15 kW per channel) - Definitions in Fig. 2.10
Fig 2.29 Measured peak-peak flux ripple across the boost inductor $M_{\text{dm1}}$, at $f_{\text{sw}} = 32$ kHz and $V_{\text{dc}} = 750$ V (Note: Phase shift is not real—measurement offset)

Based on previous analysis, the DMCI is meant to block DM circulating harmonics and reflect channel currents toward the loop. The flux density waveforms in Fig 2.29(a) and corresponding frequency spectra in Fig 2.29(b) indicate the presence of rich circulating harmonics as $N$ increases. In addition, a low frequency component due to loading of DMCI is also recorded. The peak low frequency flux component does not change with $N$, therefore the size of DMCI need not change with $N$ because the loading ratio is constant as more channels are added in parallel and is verified in Fig 2.29.

Fig 2.30 (a) Frequency spectra for converter-side channel currents $N = 2$ (b) $N = 3$ (c) Frequency spectra of circulating current for $N = 2$ and (d) $N = 3$
From the frequency spectrum for channel and circulating currents in Fig 2.30, it can be seen that the peak circulating currents at $N_{f_{sw}}$ follow the trend per Fig 2.4, where $N = 3$ exhibits the highest CM flux. The peak circulating current (CC) is maintained with respect to $N$, hence modularity is retained.

### 2.4.2 EMI measurements

Lastly, the filter block is designed to meet emission limits over the desired frequency range (150 kHz – 30 MHz) using the proposed design process. The test setup is illustrated in Fig 2.31. The measured spectra for single and multi-channel configurations are shown in Fig 2.32. The measurements reveal the effectiveness of a two-stage LCLC filter on CM noise mitigation. The impact from EPC of $M_{cm1}$ can be seen on the frequency spectrum where the attenuation due to $M_{cm1}$ is lost at higher frequencies. To account for this, the additional LC stages can be used on the grid-side as shown in Fig 2.32. Comparatively, the grid-side CM choke has a lower EPC due to smaller size catered toward high frequency attenuation, so the effect is not so prominent as the first stage CM choke $M_{cm1}$.

![Fig 2.31 Test setup for LISN terminal noise measurement, controller highlighted in yellow](image)

Upon comparison between $N=2$ and $N=3$, it can be found that $N=3$ has the lowest margin (c.f Fig 2.32(b,c)) corresponding to the $N_{th}$ switching frequency harmonic, which is in accordance with the analysis shown earlier. The impact of interleaving can be seen from the absence of circulating...
harmonics, although in some cases it is not fully suppressed (i.e. part of the circulating harmonics is observed on the load frequency spectrum). The impact of inter-channel converter FBB asymmetry can be attributed to this phenomenon, as presented previously in section 2.3.2. It is a notable challenging to ensure a low mismatch between phase currents. Note that asymmetry between grid-side FBB can also result in low frequency components, which could result in saturation of $M_{cm2}$.

Fig 2.32 (a) Partial measurements for single channel operation (b) two channel and (c) three channel interleaved/parallel (non-interleaved) mode comparison
2.4.3 Thermal measurements

Fig 2.33 (a) Steady-state temperature of FBB for single channel (b) Twochannel interleaved (c), Three-channel interleaved and (d) Temperature breakdown of each component

2.4.4 N-1 operation mode

An added benefit of the SL-FBB is the fault tolerance aspect shown in Fig 2.34, with the use of bypass switches enabling N-1 operation, which is briefly discussed in [69][70]. This differentiates it from other traditional magnetically interconnected schemes [59][49][50]. The purpose of the bypass switches (S1, S2 and S3) in Fig 2.34(b) is to provide a pass for secondary loop current to prevent any unwanted loading effect on other CIs when one of the channels is disconnected. By enabling the bypass switch S1 at the same time as channel A1 is open under a fault scenario in Fig 2.34(b), the loop is retained for N-1 channels. The incremental flux density of CI on other channels is shown in Fig 2.34(b), based on simulation and experimental results respectively. The measured flux component in CI is extracted through post-processing of measured winding currents. This scheme can avoid saturation of
CI and the system can potentially function without any interruption. The bypass switch is realized using a solid-state relay.

Fig 2.34 (a) Experimental waveforms for N-1 operation mode under low power setup (Vdc = 400 V) (b) Flux density of CI (c) Corresponding test schematic and (d) Hardware setup using SCR for bypass mechanism
2.5 Summary and Conclusion

A novel FBB concept is introduced, much like a modular PEBB. The key challenges in designing such a modular block are addressed as follows:

1. A shift from conventional multi-channel CIs to a two-channel CI is recommended to handle peak circulating current and address modularity.

2. The magnetic coupler is realized using a DMCI with a DM boost inductor inserted within the loop, resulting in scalable architecture for THD and lower losses for the boost inductor with N. Design challenges, such as loading effect, are discussed and the structure is optimized for high power density.

3. A two-stage LCLC filter is integrated in the design process to meet CM conducted emissions compliance. The filter parameters are optimized according to the trade-off between CM circulation and CM-EMI mitigation.

Practical aspects on design, i.e. the impact of inter-channel asymmetry, are studied and solutions are proposed to compensate for such effects.

In conclusion, the operating principle of the FBB is presented in detail and the effective realization of subcomponents is achieved. The performance of the FBB is verified to meet the power quality limits such as THD, circulating current, and CM-EMI, besides the basic functionality verification for up to three channels interleaved, with each channel rated for 15 kW.
Chapter 3. Alternative FBB Topologies

In the most general sense, FBBs can be classified into two forms: interconnected and non-interconnected variants as shown below, according to the nature of electrical connections between the filters of each channel. Circulating current control remains the key issue to be addressed with parallel converters. For each of these variants, novel methods to handle circulation are proposed. Two primary methods are discussed: the local trap scheme, which falls under the non-interconnected type, and the monolithic scheme, which falls under the interconnected type.

![Fig 3.1 Two variants of FBB structures (a) Non-interconnected and (b) Interconnected](image)

3.1 Localization of CM Circulation

The majority of interleaved converter applications require inter-channel CIs to block circulating currents between converters, the primary advantages being smaller size and weight. However, a standalone filter (i.e., no interconnection between filters of parallel modules), such as an LCL-DM and LCLC-CM filter, is preferred due to their fault tolerance and modularity compared to inter-channel CIs. The downside is the bigger boost inductor and CM choke volume needed to account for circulation. To utilize such a standalone filter to its full potential with interleaved systems, some of the key problems with the direct use of LCL-based filter topologies and variants with interleaved converters are identified. Analysis is limited to CM circulation, and the limitations of conventional CM...
filter topologies when used with interleaved operation are identified. Consequently, a novel scheme to localize CM circulation within the converter itself is proposed to improve loss density of CM choke. An experimental prototype is constructed for two channels to demonstrate the proposed concept. The LCLC filter in Fig 3.2(a) utilizes the benefit from two-stage attenuation (80 dB/dec) for conducted emissions compliance. When this topology is used with SiC-based converters and interleaving, there is a CM circulating flux within the first and second stage choke, which causes a significant overdesign compared to a conventional single channel LCLC filter. The CM chokes in stages 1 and 2 provide impedance for CMCC. The ground path is not seen by CMCC, therefore is excluded from the equivalent circuit in Fig 3.4. In this case there exists only one CM circulating component denoting inner, outer, and shunt component, respectively. For this LCLC topology, it can be seen from Fig. 3.2(a) that the inner and outer loop CM currents are the same.

Fig 3.2 (a) Baseline two-stage LCLC structure and (b) Shunt pass to DC mid-point

\[ i_{cm1} = i_{cm0} \quad (3.1) \]

A variant of this LCLC filter can be obtained by connecting the star point of the LCL filter to the DC bus mid-point via a CM capacitor [42]. With this filter arrangement, the equivalent circuit for CMCC will have a shunt component through the capacitor \( C_{cm1} \) as shown in Fig 3.2(b). The CMCC can be bypassed by tuning the resonant frequency to be low enough compared to the switching frequency \( (f_{res} < f_{sw}) \) where,
With this arrangement, the inner loop CMCC increases due to the low value of inner loop impedance and high value of outer loop impedance. This occurs due to a relatively larger value of inner loop capacitance, since there is no leakage current concern. This introduces additional core loss on inner choke $M_{cm1}$, which will effect the system efficiency. To be able to effectively shunt and minimize the inner loop CMCC, the impedance of the inner choke will have to be increased by several orders of magnitude that will contribute to additional winding loss.

3.1.1 Circuit design guideline of local trap filter for CM circulation localization

A coupled trap filter is proposed to solve the problem of CM choke over-design with CM shunt topology in Fig 3.3[60]. This filter topology works on the principle of impedance mismatch between the inner and outer loop. The inner loop comprises the shunt pass network between converters through the neutral point. The outer loop comprises the second stage CM choke $M_{cm2}$. A four winding CM choke can be implemented on the inner loop to provide coupling between the first stage CM choke $M_{cm1}$ and self-inductance $L_{trap}$ of the trap winding, created by the neutral shunt pass as shown in Fig 3.3 and Fig 3.4. The primary objective is to localize all the CMCC components in the inner loop. This way $i_{cm0}$ can be reduced, which can minimize the losses and volume of $M_{cm2}$, while $i_{cmi}$ is reduced by providing mutual inductance $M_{trap1}$. As a result, the total circulating current is minimized as per (3.3).

$$i_{cm0} = i_{cmi} + i_{cms} \quad (3.3)$$
Fig 3.3 Improved capacitive shunt circuit

Fig 3.4 Per-inverter circuits for CM circulating components

For analysis purposes, the system parameters are used per Table 3-1. To analyze the coupled trap circuit, a decoupled equivalent circuit can be created as shown in Fig 3.5. Since the fundamental circulating harmonics occur at the switching frequency, the criteria for a coupled trap circuit to successfully shunt the CMCC is given by the equations (3.4) and (3.5).

Table 3-1 System parameters under study

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>System</td>
<td>480 VAC, 60 Hz</td>
</tr>
<tr>
<td>Power Rating</td>
<td>15 kW per channel</td>
</tr>
<tr>
<td>DC Bus Voltage</td>
<td>750 - 800 VDC</td>
</tr>
<tr>
<td>$f_{sw}$</td>
<td>32 kHz</td>
</tr>
</tbody>
</table>
Where the switching frequency $f_{sw}$ is set to be the trap frequency $f_{trap}$, as per the decoupled circuit from Fig 3.5 (bottom) and where the mutual inductance $M_{trap}$ between self-inductance of the primary winding and trap winding is given by (3.5).

$$f_{trap} = \frac{f_{sw}}{2\pi} \frac{\frac{1}{C_{trap} (M_{trap} + L_{trap})}}{}$$

$$M_{trap} = k\sqrt{L_{trap}L_{cm1}} \approx k\sqrt{L_{trap}M_{cm1}}$$

$$M_{trap} = sM_{cm2} ; s \in \{0,1\}$$

The benefit of this topology can be exploited if the inner loop circulating current impedance is mostly provided by the trap winding. This is because the trap winding will not carry any fundamental current, and hence its cross section can be much smaller [60] compared to the case where most impedance will be provided by the three-phase winding $M_{cm1}$. From this idea, we can arrive at the condition in (3.6). This also defines the impedance mismatch between the inner and outer loop.

$$M_{cm2} \gg M_{cm1}$$

(3.6)
The impedance matrix for a four winding CM choke and the total flux linkage is shown in Equation (3.7), for the inductance parameters and CM current defined in (3.8) and (3.9), respectively.

\[
\begin{bmatrix}
\lambda_{ax} \\
\lambda_{bx} \\
\lambda_{cx} \\
\lambda_{trapx}
\end{bmatrix} =
\begin{bmatrix}
L_{cm1} & M_{cm1} & M_{trap} & M_{trap} \\
M_{cm1} & L_{cm1} & M_{trap} & M_{trap} \\
M_{cm1} & M_{cm1} & L_{cm1} & M_{trap} \\
M_{trap} & M_{trap} & M_{trap} & L_{trap}
\end{bmatrix}
\begin{bmatrix}
i_{ax} \\
i_{bx} \\
i_{cx} \\
i_{trap}
\end{bmatrix}
\]

(3.7)

And from the basic magnetic circuit the following expressions can be defined,

\[
L_{trap} = \frac{n_{trap}^2}{R_c}; \quad L_{cm1} = \frac{n_{cm}^2}{R_c}
\]

(3.8)

\[
i_{cm1} = i_{ax} + i_{bx} + i_{cx}
\]

(3.9)

Where \(n_{trap}\) is the number of turns for trap winding, \(M_{cm1}\) is the reluctance of the CM choke. To study the effect of parameters on the trap filter performance, some metrics are defined as per (3.10) and (3.11), where \(L_{trap}\) is the self-inductance of the trap coil and ‘k’ is the coupling coefficient. The factor ‘s’ decides the amount of circulation that will be diverted from the outer loop toward the inner loop. By sweeping the parameters from (3.5), i.e., varying ‘s’ and keeping \(k = 0.98\) for tightly coupled choke, the attenuation vs. frequency response from Fig 3.6 can be obtained. It is important to note that there is a resistor in series with the shunt branch, which provides damping for LCL DM resonant frequency (not shown in Fig 3.6). This will also inherently contribute to the impedance of the shunt branch at trap frequency.

\[
k^2 L_{cm1} L_{trap} = s^2 M_{cm2}^2; \quad s \in \{0, 1\}
\]

(3.10)

\[
\text{Attenuation} = 20 \log \left| \frac{i_{cm1, pk}}{i_{cmo, pk}} \right|
\]

(3.11)
As seen from Fig 3.6 (left) and Fig 3.6 (right), the split ratio will affect the attenuation at the switching frequency ($f_{sw} = 32$ kHz for example), which will affect the amount of current bypassed through the inner loop. From Fig 3.6, as the value of split ratio ‘s’ increases, the attenuation decreases.

Fig 3.6 (left) Attenuation vs. frequency for different values of split ratio ‘s’ (right) Effect of trap action on CMCC attenuation, comparison between other decoupled topologies.

This is because in the decoupled circuit, the outer loop impedance $M_{cm2} - M_{trap}$ tends to zero with increase in ‘s’. This will create a low impedance pass through the outer loop and the benefit of the shunt path is lost. However, if ‘s’ decreases the attenuation improves. But for a low value of ‘s’, the required trap impedance, $L_{trap}$, is going to be very high from (3.5) and (3.6), which could add more volume. In addition, the benefit of coupling will be lost, since the additional impedance to circulation $M_{cm1} + M_{trap}$ will be small and tend to $M_{cm1}$. This will affect the losses on the converter-side, which need to be minimized.
Table 3-2 Parameters for the studied variants

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Details</th>
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</thead>
<tbody>
<tr>
<td>$M_{cm1}$</td>
<td>0.440 mH</td>
<td>$n = 4$, $A_L = 27 \mu H/T^2$, AWG 14</td>
</tr>
<tr>
<td>$M_{cm2}$</td>
<td>5.0 mH</td>
<td>$n = 9$, $A_L = 61 \mu H/T^2$, AWG 14</td>
</tr>
<tr>
<td>$L_{trap}$</td>
<td>5.5 mH</td>
<td>$n = 14$, $A_L = 27 \mu H/T^2$, AWG 22</td>
</tr>
<tr>
<td>$C_{dmi}$</td>
<td>4.0 uF</td>
<td>B32674D1335K000</td>
</tr>
<tr>
<td>$C_{trap}$</td>
<td>3.3 nF</td>
<td>F464BC332F2K5A</td>
</tr>
</tbody>
</table>

Therefore, further optimization of this scheme can be performed to select the optimal value of ‘s’ based on total CM inductor loss and volume map. In this research, the value of ‘s’ is selected to be 0.5 based on a parametric study. The simulated CM currents from parameters in Table 3-2 are shown in Fig 3.7.

3.1.2 Experimental verification of the design

The hardware prototype is shown in Fig 3.8. Three boost inductors are added in series with the filter to provide impedance for control purposes (not included in the prototype board and impedance to DM circulation, which is out of scope in this dissertation). Nanocrystalline cores for the first and second stages are used to construct the prototype with polypropylene DM and CM film capacitors for setting the resonant frequency. The parameters are listed in Table 3-2. The trap winding is made using AWG 22 wire with 17 turns, while the three-phase winding is made using AWG 14 wire with 4 turns. Fig 3.8(a) shows the prototype test board that was used with the two-channel configuration. By setting the resonant frequency to be equal to the trap frequency per Equation (3.4), and shown from the input
impedance of the filter in Fig 3.9, we can effectively shunt the CMCC through the trap winding toward the neutral point, as shown in the time domain experimental waveforms from Fig 3.9. This is also seen from the trap current and the inner loop current spectra. The experimental results indicate a reduction in outer loop current from Fig 3.9. The FFT plot shows the switching frequency harmonic reduction, i.e. circulating harmonic component. This also matches well with the simulation in Fig 3.7. Details on simulation settings and comparison with other prospective filter structures is shown in [72].
3.2 Integration of Circulating Current Filter and DM Load Harmonic Filter

Magnetic interphase coupling between converters is a well-known technique to mitigate the problem of inter-channel circulation due to interleaved carriers. But such direct magnetic CIs contribute to additional volume and loss. Since interleaving does not cancel the $N^{th}$ order harmonics, where $N$ is the number of parallel converters, consequently an additional boost inductor is added after the PCC to meet the power quality standards. In conjunction, the total filter volume defeats the purpose of interleaving. Thanks to the use of SiC devices, the switching frequency barrier can be extended, and the size of magnetics can be reduced dramatically. Herein lies the benefit of using a magnetically-coupled structure with an integrated boost inductor. A hybrid core structure using a combination of amorphous and nanocrystalline materials has been proposed to maximize the power density of a monolithic filter building block (M-FBB) compared to a conventional Si-steel counterpart for IGBT applications. A complete experimental evaluation using a 45 kW 3-L NPC converter is presented for design verification.

3.2.1 Review of state-of-the-art magnetic integration techniques

Gohil et. al. presented an interesting approach using an integrated DM and CM structure [72] that provides attenuation to circulating and load frequency harmonics. This was demonstrated with an Si-IGBT-based converter, however this structure by itself is not modular and requires some modifications to improve the power density. Several variants of this structure can be used to exploit different CM and DM flux paths within the assembly. Each CM/DM component will provide attenuation to a specific group of harmonics [9]. A detailed study is presented in [9], showing the trade-offs between the variants and the final design. Furthermore, to fully optimize the structure, it is required to have a hybrid integration scheme, as will be explained later. The hybrid structure also simplifies the design process considerably. A design guideline is presented with validation between measured and simulated flux
densities for a 30 kW (N = 2) and 45 kW (N = 3), 3L-NPC converter under symmetric interleaving (\(\theta = \pi\) and \(\frac{2\pi}{3}\)).

3.2.2 Design of the modular monolithic structure using hybrid magnetics

The main filter structure under consideration is shown in Fig 3.10. It is comprised of three 3L-NPC converters with phases interleaved between channels and directly coupled with each other in the form of inter-channel CI. Three main components make up the monolithic structure, i.e. yoke \(\mathcal{R}_y\), limb \(\mathcal{R}_l\), and bridge yokes \(\mathcal{R}_{\text{bridge, yoke}}\), where \(\mathcal{R}_x\) denotes the reluctance of the specific magnetic component ‘x’. The bridge yoke is considered low reluctance for simplicity and is replaced with the reluctance of air gap instead. Each limb provides impedance to line/load frequency harmonics and circulating components; yokes provide coupling between channels and contribute to additional reluctance for inter-channel CI, while the bridge yokes are used provide a pass for line frequency flux. With these points in mind, there exists an air gap, \(\mathcal{R}_g\), between the bridge yokes and individual limbs to avoid saturation due to line frequency flux component. The CI(s) however do not need an air gap. An important aspect of this design is modularity, i.e. the monolithic arrangement should not see any major difference in flux components as more converters are added in parallel. The grid-side filter provides impedance to average load components \((A_{\text{total}}, B_{\text{total}}, C_{\text{total}})\) and must be constructed in a parallel configuration to ensure that the peak flux density on the boost inductor does not change significantly with different channels. This structure inherently allows the paralleling feature as shown in Fig 3.10(a).
The basic monolithic filter structure is shown in Fig 3.11 with its two possible variants. Each channel has a DM three-limb inductor \( R_l \) to provide attenuation to load frequency harmonics (60 Hz), while each of the phases are coupled via inter-channel yokes (DM and CM) for circulating current attenuation. This can be understood by the phase sequence between channel currents of the same phase (e.g. A\(_1\), A\(_2\), A\(_3\)) and the phases (e.g. A, B, C) of each channel. However, the monolithic structure by itself does not provide impedance for CM-EMI components. Hence, additional modifications are needed to add a CM choke or change the structure of the monolithic block itself. Based on this requirement, the two possible variants of the monolithic structure are as follows:

* **a) With integrated CM limb, b) Without integrated CM limb, separate CM choke**
Depending on the effective reluctance provided by each variant, using basic geometrical analysis it was found that a separate CM choke will provide the highest power density for the monolithic block. This primarily comes from the high reluctance of additional limbs (longer magnetic length), which results in a higher turn number requirement to produce the same CM impedance as a separate CM choke, as shown in (1). Therefore, the rest of the dissertation will analyze the monolithic structure with a separate CM choke shown in Fig 3.11(b).

\[ M_{cm,(a)} = \frac{N^2}{\Re_{\text{limb}(a)}} ; \Re_{\text{limb}(a)} \gg \Re_{\text{choke(b)}} \]

\[ M_{cm,(a)} \ll M_{cm,(b)} \]  

(3.12)

In order to fully utilize the benefit from WBG devices, it is possible to shrink the size of the magnetic core using a combination of different magnetic materials. The material selection is primarily done using four equivalent circuit models [9]. Another criterion is the comparison between saturation flux density and core loss as per Fig 3.12.
Fig 3.12 Material selection for a hybrid monolithic structure based on decomposed flux components

From Fig 3.12 it can be deduced that nanocrystalline cores (*Vitroperm* 500F) will provide the highest attenuation per unit volume with low core loss, for DM and CM circulating currents. METGLAS® is considered for line/load frequency harmonics because of high $B_{SAT}$ values compared to *KoolMu*® and lower core loss when compared with Si-steel. Therefore, a hybrid structure can be proposed for SiC applications as shown in Fig 3.13. It comprises amorphous-based limbs, bridge yokes, and nanocrystalline inter-channel yokes. The nanocrystalline yokes provide a low reluctance path for high frequency circulating components and increase the effective mutual inductance for circulation, $M_{ci,\text{effective}}$, as per (3.13). Two-thirds of this effective mutual inductance contributes to DM circulating current impedance, while 1/3 of this component contributes to CM impedance.

$$M_{ci,\text{effective}} = \frac{N^2}{(R_y + R_l)}; \quad R_y \ll R_{\text{limb}}$$

(3.13)

$$M_{ci,\text{effective}} = \frac{N^2}{R_{\text{limb}}}$$

The impedance for load frequency harmonics $M_{dm1,\text{effective}}$ shown in (3.14).
Based on this simplification of the magnetic structure, it was found that the effective power density can be increased, while the loss density is reduced compared to using a conventional Si-steel monolithic structure as per Fig 3.13.

Typically, such a structure can be designed based on an iterative procedure with dimensions being swept every iteration. The optimal parameters for the structure are selected from the pareto curve plot between the power density and efficiency for the entire system (converter and filter block), which is typically the designer’s intent. The optimization process has two stages, where the first is to create a subset of FBB parameters that would satisfy the circulating current requirement. The second is to physically design the monolithic structure and optimize the dimensions of the structure. A step-by-step design procedure is presented in Fig 3.14. The most important consideration for loss calculation is to analytically compute the flux densities and core volume through each section of the monolithic block. The effective frequency and core loss through the section under consideration is calculated as per (3.15).
\[ P_v = k f_e \alpha B_e^\beta \quad ; \quad f_e = \frac{\int_0^T d^2B}{2\pi \int_0^T dt} \] (3.15)

\[ J_{calc} = \frac{2Ni_{max}}{A_eK_e} \] (3.16); Each window has 2 windings

The reluctance of the limb is a function of the limb geometry and permeability, which is iteratively swept. **There are some underlying assumptions in the design process, which are stated below.**

a) Cross-sectional areas for different block cores are equal \( A_{e,\text{limb}} = A_{e,\text{yoke}} = A_{e,\text{bridge yoke}} = A_e \).

b) Square cross-sections are considered to provide maximum power density. This assumption is valid, considering that a cube will provide the lowest volume for a three-dimensional (3D) block.

c) The maximum current density \( J_{\text{max}} \) per (3.16) of each winding is set to be 6A/mm\(^2\).

d) The maximum temperature rise for the entire structure is set at 75\(^\circ\)C (including the winding and core)

e) Inductor volume is considered as a boxed volume in this case.
3.2.3 Experimental verification of the design

In this section, detailed waveforms and analysis on circulating current and channel current waveforms are performed. The test circuits are composed of 3L-NPC converters under symmetrical interleaved PWM mode, with CM chokes (added to block CM circulation) and the proposed monolithic filter block (to block DM load and DM+CM circulating components). The design parameters are taken from Table 3-1 and Table 3-2, obtained from a multi-variable optimization process. Inverter mode and rectifier mode operational tests were performed, and the details are shown in the following subsections.
As per Fig 3.15 (a,b), RL load testing under a 45 kW, 800 V\textsubscript{DC} rated power condition was performed to evaluate the proposed monolithic structure. A symmetrical sinusoidal waveform can be obtained under RL load, indicating a balanced inductance $M_{\text{dm1}}$ produced by limbs and bridge yokes. Due to interleaving, the total output current has $N^{th}$ switching frequency harmonic, where $N$ is the number of converters connected in parallel. The circulating current was effectively blocked, yielding only twice the switching harmonic for the channel currents as well. This is demonstrated by the FFT results on total circulating current and channel currents in Fig 3.15. With the filter, the circulating current is effectively minimized to a small value (0.2 A as per optimal design parameter).

![Fig 3.15](image)

Fig 3.15 (a) Two-channel configuration monolithic (b) Channels 1, 2, and total output current phase waveforms (c) Three-channel configuration monolithic (d) Channels 1, 2, and 3, and total output current phase waveforms

Flux density through the CIs is post-processed by taking the high frequency measured CI flux component shown in Fig 3.16. This eliminates the low frequency circulation and gives better
correlation with simulation results. As per [11], it was verified that the peak circulation does not change significantly as number of channels change. This is validated in this section as well, since the peak flux density across yokes does not change as the number of parallel converters change, as seen from Fig 3.16.

![Fig 3.16 (a) Flux density through yoke (N=2) (b) Flux density through yoke (N=3)](image)

A fully-integrated monolithic block with LCL filter is shown in Fig 3.17 (a,b). It is composed of the first stage CM choke, the monolithic coupler with integrated boost inductor, and the second stage of the LCL filters on the grid-side. By designing the second stages to provide high frequency attenuation for EMI and additional harmonic attenuation for THD, the overall performance of the structure can be seen from Fig 3.17 (c,d), where the THD performance of the LCL filter is shown under rectifier mode.
In summary, a modular-monolithic integrated filter block is presented for use with an SiC-based three-phase AC-DC converters. The effectiveness of hybrid-integrated magnetics with interleaved converters to provide high power density and attenuation (with negligible trade-off) has been demonstrated. The structure is modular, as the flux density within the yokes and DM limbs does not change with the number of channels. A prototype using a 45-kW rated power and 480 VAC/60 Hz system was constructed and tested to verify the design process. A significantly higher power density of over 8 kW/l for the system and more than 15 kW/l for the monolithic coupler was achieved. Despite these advantages, the use of nanocrystalline yokes imposes challenges, such as loss in attenuation at higher frequencies. To avoid these problems a maximum switching frequency of 30 kHz for SiC applications and a high bandwidth, low frequency circulating controller is recommended. Additional details on performance trade-offs are presented in the subsequent section.
3.3 Full-Scale Comparison of Alternative FBBs with Secondary Loop FBB

3.3.1 Trade-offs from optimization results

In this section, the interconnected topologies presented earlier are evaluated for power density and efficiency.

![Fig 3.18](image)

Per Fig 3.18, it is observed that with an increase in switching frequency, the overall size of the filter block decreases, due to a smaller circulating current filter requirement. Since the switching losses and switching frequency (neglecting the low reverse recovery loss) have a linear relationship, the lowest switching frequency is ideal for low loss. The downside is that the filter volume increases significantly, mostly dominated by the volume of the circulating current filter. Based on this, the optimal point is selected in the mid-frequency range (32 kHz) when sweeping between 16–48 kHz. The filter volume distribution at this frequency (highlighted in Fig 3.18 (c,d)) provides some insight into the relationship between the groups of harmonics being attenuated and filter component volume, as shown in Fig 3.18(c,d).
1) For the SL-FBB, the loading effect and circulating harmonics within the loop contribute to large DMCI, while the cancellation of switching harmonics within the loop lead to a small boost inductor ($M_{dm1}$) volume, as seen from Fig 3.18(c).

2) In case of the monolithic structure, the combined weight of the boost inductor and CI ($M_{dm1}$ and $M_{ci}$) can be found to be smaller than the other topologies (a benefit of high density integration, as phase limbs share circulating and load flux) seen from Fig 3.18(c).

3) The volume contribution of a second-stage DM inductor of LCL filter ($M_{dm2}$) is small because a Si-steel core can be used to reduce core area (high $B_{sat}$) without the concern of core loss, due to the absence of switching ripple harmonics.

Table 3-3 shows the final filter parameters for both FBBs. The interconnected topologies are experimentally evaluated further, to clearly understand the differences in hardware implementation between the two. The prototypes for the interconnected topologies were shown in Fig 3.9 and Fig 3.17. Unlike the magnetic interconnection, the electrical interconnection provides a seamless plug-and-play architecture with a reconfigurable secondary loop-based interconnection using electrical cables based on number of channels (N). This is desirable from the modularity point of view.

<table>
<thead>
<tr>
<th></th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic Interconnection (M-FBB)</td>
<td></td>
</tr>
<tr>
<td>$M_{ci}$</td>
<td>600 µH</td>
</tr>
<tr>
<td>$M_{dm1}$</td>
<td>85 µH</td>
</tr>
<tr>
<td>$C_{dm1}$</td>
<td>2.3 µF</td>
</tr>
<tr>
<td>Electrical Interconnection (SL-FBB)</td>
<td></td>
</tr>
<tr>
<td>$M_{ci}$</td>
<td>600 µH</td>
</tr>
<tr>
<td>$M_{dm1}$</td>
<td>50 µH</td>
</tr>
<tr>
<td>$C_{dm1}$</td>
<td>3.3 µF</td>
</tr>
</tbody>
</table>
3.3.2 THD, circulation and N-1 operation mode characterization

The steady-state waveforms for single, double, and triple-channel configurations of both interconnected variants are shown in Fig 3.19. Based on the THD performance in Fig 3.20, the THD for SL-FBB improves with a higher number of channels, while the M-FBB degrades from $N = 2$ to $N = 3$. The upper and lower DC link capacitor voltages and neutral point voltage (capacitor voltage deviation) are shown in Fig 3.19(c).
From the experimental results for circulating and load current ripple in Fig 3.21, the converter current ripple for the M-FBB is approximately two times lower than the SL-FBB. This comes from the design guideline presented earlier and shown in Table 3-4. In simple terms, the large value $M_{ci}$ for circulating current mitigation also enforces a larger value of boost inductor for the M-FBB, since they are integrated on the same limb.

Table 3-4 Summary of CI and boost inductor component selection criteria

<table>
<thead>
<tr>
<th>Topology</th>
<th>Guideline</th>
</tr>
</thead>
<tbody>
<tr>
<td>Magnetic Interconnection</td>
<td>$n = \sqrt{M_{ci} R_i} ; l_g = \frac{n^2 \mu_0 A_e}{M_{dm1}}$</td>
</tr>
<tr>
<td>Interconnection (Monolithic)</td>
<td></td>
</tr>
<tr>
<td>Electrical Interconnection</td>
<td>$\frac{M_{dmc1}}{M_{dm1}} &gt; 10$</td>
</tr>
<tr>
<td>(Secondary Loop)</td>
<td></td>
</tr>
</tbody>
</table>

Fig 3.20. THD comparison: M-FBB (Top) and SL-FBB (Bottom)
On the other hand, the smaller boost inductor requirement for the secondary loop topology comes from the loading effect constraint on the CI (Table 3-4), which could potentially saturate the core if not designed for a larger core area. As such, the value of $M_{dm1}$ is typically low with the SL-FBB compared to the M-FBB. By adding more channels, the effective converter load current ripple is reduced, as seen from the spectra in Fig 3.21. However, a higher circulating current ripple is seen at $N = 3$ for the monolithic structure corresponding to $2f_{sw}$ harmonic component.

![Fig 3.21 Converter current ripple evaluation for phase A current of channel 1, under different number of parallel converters (N)](image)

The higher circulating current ripple at $N = 3$ for the M-FBB is due to the selection of nanocrystalline core for the inter-channel yokes. The benefit was seen from low volume requirement compared to pure amorphous or Si-steel counterparts. However, it also resulted in a significant drop in permeability at higher frequencies per Fig 3.22. Note the drop in permeability across the yoke in Fig 3.22(a), which results in an increase in reluctance for the inter-channel yokes $\mathcal{R}_{yoke}(\mu(f))$ with frequency to an extent that the net impedance to circulation drops per (10). The net reluctance to circulation $\mathcal{R}_1 = \mathcal{R}_{limb} + \mathcal{R}_{yoke}(\mu(f))$ increases at higher frequencies. Fig 3.22(b) reflects the impact of this behavior on
circulating current spectra. Air gaps between yoke and limbs due to imperfect mechanical assembly can lead to a similar problem.

Fig 3.22 (a) Loss in attenuation of nanocrystalline yoke for M-FBB (b) Comparison of FFT for circulating current 
\((N = 2, f_{sw} = 32 \text{ kHz})\)

An added benefit of the SL-FBB is the fault tolerance aspect, with the use of bypass switches enabling N-1 operation, briefly discussed in the previous chapter. This differentiates it from other traditional magnetically interconnected schemes. The purpose of the bypass switches (S1, S2, and S3) in Fig 3.23 (b) is to provide a pass for the secondary loop current to prevent any unwanted loading effect on other CIs when one of the channels is disconnected. This operation mode cannot be used with magnetic interconnection schemes, due to the direct coupling between channels. A saturation of the CI results in abnormal operation of boost inductor, which is integrated with the CI. A simulation result showing the impact of N-1 mode on the two variants is shown in Fig 3.23.
3.3.3 Loss efficiency and thermal characterization

Fig 3.23 (a) M-FBB under N-1 operation (b) SL-FBB: bypass switch implementation under N-1 operation, (c) N-1 mode for M-FBB and (d) N-1 mode for SL-FBB using bypass switch

Fig 3.24 (a) Steady-state temperature for the SL-FBB, (b) M-FBB, (c) Efficiency with N, (d) Experimental loss breakdown for M-FBB (magnetically interconnected version) (e) Loss breakdown SL-FBB (electrically interconnected version)
The steady state operating temperature are verified to be within the maximum operating limit of the components. Some of the key observations are discussed in this section. The CI has the highest peak temperature out of all the FBB subcomponents. Interestingly, the temperature of CI for M-FBB increases as N increases, per Fig 3.24 (b), which is quite opposite to the case in Fig 3.24(a) for SL-FBB, where the CI has consistent temperature across N. The difference in temperature is suspected to be caused by low frequency flux components enhancing the core loss within CI. The grid-side FBB components have the lowest temperature due to the absence of switching ripple.

A notable finding is that the efficiency of the electrical interconnection scheme increases with the number of channels, N, due to the drop in the core loss across the boost inductor. As observed earlier from Fig 3.21, the high DM ripple (at $f_{sw}$ harmonic for N = 1) within the boost inductor for the SL-FBB results in highest losses under a single channel configuration. This ripple gradually decreases with the increase in N.

While with the magnetic interconnection, the inadvertent presence of an air gap between inter-channel CI or loss of attenuation with higher frequencies due to nanocrystalline yokes increase the circulating current ripple, and losses with increase in N, seen from Fig 3.24(d, e). It is indeed arduous to guarantee a perfectly scalable CI with any N using such a magnetic interconnection scheme due to presence of air gaps. Therefore, the loss of attenuation to circulating components for higher N with the M-FBB results in poor efficiency.

Considering these points, the electrical interconnection scheme using SL-FBB is deemed suitable for high power applications, since the CI is only connected between the loop and the main channel, irrespective of N. Table 3-5 provides a qualitative comparison between the two variants.
Table 3-6 provides a quantitative summary of the candidates based on the experimental results of the constructed prototypes.

Table 3-5 Summary of evaluation for 460VAC, 15 kW per channel for three channels (45 kW total)

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Electrical Interconnection</th>
<th>Magnetic Interconnection</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>N = 2</td>
<td>N = 3</td>
</tr>
<tr>
<td>THD (%)</td>
<td>2.82</td>
<td>2.21</td>
</tr>
<tr>
<td>Peak Circulating Current</td>
<td>0.8</td>
<td>1</td>
</tr>
<tr>
<td>Efficiency (%)</td>
<td>97.5</td>
<td>97.75</td>
</tr>
<tr>
<td>Peak Temperature (°C) –</td>
<td>98.7</td>
<td>96</td>
</tr>
<tr>
<td>Peak Flux Density for different filter</td>
<td>$M_{dm1}$ $M_{ci}$ $M_{dm1}$ $M_{ci}$ $M_{dm1}$ $M_{ci}$ $M_{dm1}$ $M_{ci}$</td>
<td>$0.8$ $0.5$ $0.7$ $0.5$ $0.5$ $0.55$ $0.51$ $0.5$</td>
</tr>
</tbody>
</table>

Table 3-6 Qualitative comparison between candidates

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Electrical Interconnection</th>
<th>Magnetic Interconnection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power</td>
<td>Low</td>
<td>High</td>
</tr>
<tr>
<td>Efficiency</td>
<td>Higher for higher number of channels</td>
<td>Lower for higher number of channels</td>
</tr>
<tr>
<td>Assembly</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>Scalability</td>
<td>Good</td>
<td>Poor</td>
</tr>
<tr>
<td>N-1</td>
<td>Good</td>
<td>Poor</td>
</tr>
</tbody>
</table>
3.4 Summary and Conclusion

Two types of modular, interconnected FBB candidates are evaluated for high power density and efficiency. A systematic design procedure is formulated by considering the worst-case design criteria for each group of harmonics, i.e., \( N = 1 \) for THD, \( N = N_{\text{max}} \) for EMI, and \( N = 2 \) for circulation. Out of the interconnected topology variants, the magnetic interconnection schemes suffer from asymmetry and challenges in physical assembly. The inevitable air gaps between inter-channel CI cause loss in attenuation, due to circulating components and low frequency grid-side harmonics, resulting in higher THD as \( N \) increases. A major drawback of magnetic interconnection is the inability to operate under N-1 mode. Contrary to this, the electrical interconnection schemes are easier to implement, design, and manufacture. The attenuation to circulating current is retained with lower impact from asymmetry in CI. This also results in lower THD with larger \( N \). An N-1 operation under fault conditions can be enabled through a bypass switch mechanism. This minimizes the size increment on the CI that is imposed if a magnetically coupled FBB must handle N-1 operation. Consequently, the electrical interconnection using the SL-FBB is -favorable because it provides all the modular features of a building block.
Chapter 4. Design of a Modular FBB for Aerospace Applications

Lately, SiC technology has penetrated the high-power traction motor drive application space [74], resulting in ultra-dense inverter solutions [75][76][77][78]. There have been major systemic technological advancements that enable the use of SiC devices for high power applications. Particularly, the use of Rogowski coil-based current sensing [79][80], widely adopted as a non-intrusive current sensing scheme for short circuit protection, helps realize such high-density designs by eliminating the need for bulky current sensors. Multi-level and parallel/interleaved inverter and filter topologies [77][78] can limit the $\text{dv/dt}$ at the switching node, thereby shrinking filter size, providing superior power quality and improving power density. Packaging technologies for SiC devices enable high temperature and high current operation feasible in a compact package, with low on-state resistance ($R_{DS,ON}$) and stray inductance [81][82]. Novel mechanical and thermal integration challenges have been addressed using heavy copper PCB technology, which allows better control during design, stack-up, and assembly. However, such features in a compact design introduce additional complexities in handling noise propagation, which needs to be addressed in detail [83][84][85]. For instance, a well-known problem with high-power, SiC-based inverters is the commutation loop resonance and high $\text{di/dt}$. This stems from the use of large standoffs and interconnections between module and bus bar, which limits the switching speeds [86][87] to avoid severe voltage overshoots. The problem is exacerbated by introducing the Rogowski coil-based sensor between the module and bus bar assembly to measure device current, resulting in a larger clearance, hence a larger loop inductance.

Although the power density in this case is superior due to absence of bulky hall current sensors [88], the DM and CM noise limit on the DC side in the very high frequency (VHF) range, which refers to emissions beyond 30 MHz, is violated. The device turn-off voltage overshoot is even higher, thereby
stressing the modules. This is particularly damaging in aerospace applications with strict DO-160 emissions standards and high reliability requirements [89].

In addition, the motor unit provides an additional path for CM currents via the stator to frame, rotor to frame, and bearing [85]. The effects manifest in the form of low-and mid-frequency resonance of DC-side CM currents. Ground loop impedance, together with the filter and inverter parasitics, also influence the emissions spectra on the DC-side [83][85][84]. Hence, conducted noise mitigation on DC-side, given the strict DO-160 and military standards for transportation applications, is challenging. Clearly, there is a need for novel filter and inverter integration schemes with ultra-low parasitic impact to meet such a wide-band frequency limit line, and at the same time respect the thermal and partial discharge limitations (as seen with MV power converters [90][91][92][93][94][95][96], which is an added constraint with high altitude operation [97][98][99][100].

Besides conducted emissions at the DC terminal, bearing and leakage current phenomenon due to the high slew rate of SiC devices must be considered to maintain motor lifetime and reliability goals [94]. Eventually, high switching frequency and dv/dt affects the size of AC filters (i.e. dv/dt filters) significantly [101][102][103]. Although AC filters (such as a pure CM inductor) are commonplace, their bandwidth to block such peak CM currents is limited, which calls for novel circuitry to enhance the performance of AC filters. A single turn inductor is recommended with improved damping performance to minimize the overall system weight. In addition, the coupled nature of CM noise between the AC and DC-sides for DC-fed motor drives adds complexity in design. Therefore, a decoupled method is preferred to simplify the design process and improve noise attenuation of DC CM currents [104].
Fig 4.1 Three-phase 3LT-type inverter with motor circuit (with filter and parasitic load components highlighted here) – The proposed AC filter is within the highlighted box.

Furthermore, CM noise propagation to analog and digital circuitry, due to induced voltage/current at the Rogowski coil, can cause signal integrity concerns on the controller-side [105]. It has been demonstrated that multiple paths of coupling exist between the high-power node of the coil output to the control ground. Adding to this, the presence of long ribbon cables for signal transmission (with high edge rates) can create additional mutual coupling effects [106]. This may lead to nuisance tripping of the inverter due to crosstalk. Although fiber optics signal transmission is a known feasible solution, it is not cost effective. Hence, a stable grounding scheme compatible with short ribbon cables with good signal fidelity is required, keeping costs to a minimum.

To summarize, novel passive component integration and layout techniques within the inverter are required to address the issues listed so far. Fig 4.1 shows the proposed hardware of a high-power inverter.
(211 kW unit) for an aircraft propulsion system and the associated sub-components for noise mitigation. Although numerous state-of-the-art propulsion inverter prototypes have reported high densities and specific power, the implications of such high-power designs on noise propagation and the impact on additional filtering is not fully addressed. Therefore, this dissertation bridges the knowledge gap with a comprehensive characterization of different resonant modes produced by the propagation impedance, filters, and inverter.

**This chapter also proposes and demonstrates the following hardware techniques:**

a) An improved AC CM filter with optimized damping resistor for peak bearing current and DC CM noise mitigation.

b) A unique inverter assembly and filter integration scheme with edge plating technique, feedthrough cable [107], and ferrite beads for high frequency attenuation.

c) A decoupling board with AC layer and localized high frequency commutation path with embedded Rogowski coil-based current sensing.

d) Optimized system layout for signal integrity and the inclusion of isolation layers for minimal CM noise coupling.

### 4.1 Design for AC Bearing Current Minimization.

#### 4.1.1 Review and challenges of state-of-the-art AC filters

With the advent of SiC devices, a high dv/dt switching environment can further degrade the bearing insulation and intensify the circulating current through the bearing [83]. Notably, the damage occurs due to localized heating near asperity contacts. In addition, the stator to frame and rotor to frame capacitances contribute to additional CM pass to ground, resulting in significant CM current [84].

Among the state-of-the-art filters designed to mitigate such CM currents [108][109][110][111], the primary drawback of those schemes is the high passive component weight requirement. For instance, the active and passive CMV cancellation in [108][109] imposes a high magnetizing inductance
requirement, resulting in larger window area. The LC topology in [110] results in large volt-second due to inner loop circulating 3rd harmonic components. The series damper across the AC choke in [111] necessitates the use of a large magnetizing inductance. Relying on the resistive losses of a conventional CM core can offer natural damping [112]; however, the dispensed core loss results in low efficiency and creates thermal management issues. Furthermore, the natural resistance is proportional to square of the number of turns, which implies higher turns for a high damping coefficient, thereby increasing winding loss. To make matters worse, using a standalone CM choke for peak CM current mitigation can lead to potential self-resonance effects in a VFD system [113], which can be solved through passive damping [108][114].

In some applications, damping is attributed to reduced system efficiency and degraded harmonic attenuation performance [115][116][117]. Alternatively, feed-forward capacitor current/voltage feedback was demonstrated to improve the filter performance [118][119], specifically for CM circulating currents and leakage currents. Notwithstanding, the proposed active methods have limited bandwidth and cannot be applied to high frequency CM current (CM current in the switching harmonics range) mitigation, which is the region of interest in this article.

4.1.2 Design guideline for AC CM filter with optimized damper

To simplify the design of the AC filter, the circuit in Fig 4.2(a) must be decoupled. In this regard, the CM capacitors from DC terminals to ground (C_{cm,DC}) are selected to be 750 nF each. This ensures the condition for impedance mismatch as per (4.1). Equation (4.1) implies that the CM circuit on the DC side can be decoupled from the AC side of the inverter, depending on the CM capacitor to ground C_{cm,DC}. Additionally, this can also be achieved by grounding the mid-point of the DC link. As a result of this condition, the analysis can be shifted purely to the AC side.
<table>
<thead>
<tr>
<th>Motor parameters</th>
<th>Motor parameters</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type</td>
<td>PMSM, 12 pole</td>
</tr>
<tr>
<td>$C_{\text{wdg}}$, $R_{\text{wdg}}$, $R_{\text{AC}}$</td>
<td>$200\ \text{pF}, 1\ \text{k}\Omega, 5\ \text{m}\Omega$</td>
</tr>
<tr>
<td>$C_{\text{b}}$, $C_{\text{rf}}$, $C_{\text{wr}}$, $L_{\text{sdc}}$, $C_{\text{src-gnd}}$</td>
<td>$30\ \text{nF}, 1\ \text{nF}, 2\ \text{nF}, 10\ \text{nF}, 1\ \mu\text{H}, 500\ \text{nF}$</td>
</tr>
<tr>
<td>$dv/dt, f_{\text{sw}}, f_{\text{op}}$</td>
<td>$25\ \text{kV/\mu s}, 20\ \text{kHz}, 1.75\ \text{kHz}$</td>
</tr>
<tr>
<td>$i_{\text{cm,AC}}$ (pk)</td>
<td>$0.5\ \text{A}$</td>
</tr>
<tr>
<td>$V_{\text{dc}}$, $P_{\text{rated}}$</td>
<td>$850\ \text{V}, 211\ \text{kW}$</td>
</tr>
</tbody>
</table>

\[
\frac{i_{\text{cm,dc}}}{v_{\text{cm}}} < \frac{i_{\text{cm,ac}}}{v_{\text{cm}}} \quad (4.1)
\]

\[
\begin{align*}
C_{g_2} &= (C_b + C_{rf}) || C_{wr} \\
C_{g_1} &\approx C_{rf} \\
C_{g,\text{eq}} &\approx C_{g_1} + C_{g_2}
\end{align*} \quad (4.2)
\]

Fig 4.2 CM-equivalent synthesis (a) Exact CM-equivalent circuit (b) Decoupled CM circuit with parasitic components (c) Simplified reduced order AC-CM circuit – The proposed filter is highlighted in red.

Fig 4.3 Impact of $C_{\text{cm,DC}}$ on AC-CM current response (red/blue curves). A higher $C_{\text{cm,DC}}$ results in decoupled operation seen from blue curve - system parameters per Table 4-1.
The impact of adding a large $C_{cm,DC}$ is seen from DC and AC-CM transfer gain (admittance) in the frequency domain per Fig 4.3, based on a motor rated at 400 kW and system parameters from Table 4-1. In this article, the motor parameters were directly supplied by the vendor. The detailed motor CM model in Fig 4.2(a) can be transformed into a reduced order model. For low values of $C_{cm,DC}$, the AC-side CM current is affected by the DC-side LC resonance created by $M_{cm,DC}$ and $C_{src-gnd}$. This is shown in the blue curve in Fig 4.3, where resonance component $f_{res,dc}$ is seen. Increasing $C_{cm,DC}$ can avoid this resonance (seen from red curve), since most of the AC-CM current would be bypassed by $C_{cm,DC}$ (Note: the selection of $C_{cm,DC}$ stems from lightning and safety requirements, and depends on application and standards). Consequently, the circuit in Fig 4.2(b) can be deduced from Fig 4.2(a), where the DC source impedance effect can be bypassed. The circuit from Fig 4.2(b) can be simplified further to a reduced order model in Fig 4.2(c) under special conditions. The AC-CM current transfer gain of the circuit in Fig 4.2(b) shows the existence of multiple resonant points, i.e. $f_{res1}$ and $f_{res,high}$ shown in Fig 4.4(a). The peak value of the AC-CM current occurs at these resonant points. While resonance due to $C_{cm,AC}$, $C_{g2}$, $M_{cm,AC}$ and $C_{g1}$ constitutes mid-frequency resonance $f_{res}$, the high frequency component $f_{res,high}$ stems from the equivalent parasitic capacitance of stator winding $C_{wdg}$ and leakage inductance $L_{lk}$. If $M_{cm,AC}$ is large enough, the transfer gain of the reduced order model in Fig 4.2(c) can match with the full-scale model of Fig 4.2(b) near the mid-frequency range, as illustrated in Fig 4.4(a).

Here the transfer gain of the two models is indicated by dashed and solid lines and plotted as a function of the ratio between $M_{cm,AC}$ and $L_{lk}$. A higher ratio implies that $M_{cm,AC}$ dominates over the $L_{lk}$, and that $L_{lk}$ can be neglected in the reduced order model because the peak component at $f_{res,high}$ gets relatively lower at higher values of $M_{cm,AC}$. For instance, the transfer gain magnitude at the high frequency component $f_{res,high}$ is much lower than at $f_{res}$ for larger ratios (> 2), per Fig 4.4(a), and can be ignored for peak AC-CM current calculation. This is further exemplified by the comparison of AC-CM time domain waveforms of the reduced order and the full-scale model under different ratios in Fig
The difference in peak values and resonant frequencies at a lower ratio can be clearly seen in Fig 4.4(b); the right plot correlates with the AC transfer gain plot. To quantify the impact of this ratio, the peak value and resonant frequency for the two models are compared further in Fig 4.5, showing the impact of this ratio on the accuracy of the model. Beyond a ratio of 2, the peak value of CM currents and resonant frequencies $f_{\text{res}}$ can match for the two models within 5% tolerance. Note that the chaotic behavior is found to be an artifact of simulation and does not affect the results, since the error is found to be consistently decreasing. In summary, the leakage inductance $L_{\text{lk}}$, $C_{\text{wdg}}$, and damping resistor can be neglected in the reduced order circuit. As it has minimal effect on peak CM current value if $M_{\text{cm,AC}}$ is larger by a factor of 2.

Fig 4.4 (a) Impact of $L_{\text{lk}}$ on AC-CM current response (b) Corresponding difference in time domain under two cases
- Left: $M_{\text{cm,AC}} \gg L_{\text{lk}}$ and Right: $M_{\text{cm,AC}} < L_{\text{lk}} - R_d$ is set to high impedance and $C_{\text{cm,AC}}$ is set to 5 nF and system parameters per Table 4.1.
Fig 4.5 Comparison of peak values and resonant frequencies for the reduced order and actual CM-equivalent circuit model, based on parameters in Table 4.1.

Note that the reduced order model is used to further optimize the selection of $M_{cm,AC}$ in conjunction with the RC filter parameters $R_d$ and $C_{cm,AC}$. This simplification results in a relatively easier mathematical formulation for optimizing the damping resistor.

$$f_{res} = \left\{ \begin{array}{ll} \frac{1}{2\pi \sqrt{M_{cm,AC} (C_{cm,AC} + C_{g,eq})}} & R_d = 0 \\ \frac{1}{2\pi \sqrt{M_{cm,AC} C_{g,eq}}} & R_d = \infty \end{array} \right. \quad (4.3)$$

A family of AC transfer gains are plotted with a different damping resistor parameter for each case in Fig 4.6(a). From the trajectory of the peak AC-CM current (marked in blue), the location and magnitude of this peak CM current depends on $R_d$ as it transitions between two resonant points, $f_{res,R_d=0}$ and $f_{res,R_d=\infty}$, as described in (4.3). The transfer gain is plotted per the expression in (4.4). These points correspond to two resonant frequencies involving the two loops marked in Fig 4.2(c). Furthermore, the resonant frequency and optimal damping resistor value can be deduced by solving the differential Equations in (4.5) and (4.6), respectively.
Equation (4.5) yields the resonant frequency $f_{\text{res}}$ at which the transfer gain is the highest, using the condition for global optimum. Substituting this value in Equation (4.6) leads to the corresponding value of the damping resistor at this resonant frequency, indicated in (4.7). The equivalent motor-side parasitic capacitance is defined in (4.2). Clearly, for a given value of $M_{\text{cm,AC}}$ and $C_{\text{cm,AC}}$, there is an optimized value of $R_d^{\text{optimal}}$, given by (4.7). This value corresponds to the lowest point indicated by the dashed blue line in Fig 4.6(a). If $R_d$ is selected per (4.7), it is possible to achieve the lowest peak CM current for a given value of $M_{\text{cm,AC}}$ and $C_{\text{cm,AC}}$. From Fig 4.6(b), there exists a family of peak CM current transfer gains (corresponding to optimal $R_d$) for each LC parameter. As $M_{\text{cm,AC}}$ and $C_{\text{cm,AC}}$ increase, the peak CM current and the resonant frequency reduce gradually.
As per the analysis in previous sections, it can be concluded that an iterative design process is feasible starting with the smallest value of AC inductance and capacitance \( \{M_{cm,AC}, C_{cm,AC}\} \), and incrementing the values every iteration until the desired peak CM current limit is met. The lowest peak CM current for each LC parameter will be ensured according to the derived condition for \( R_d \) in (4.7). A family of LC filter solutions exists and is shown in Fig 4.7. Since the resonant frequency
\( f_{\text{res}} \) is almost constant for all LC parameters, an inverse relationship is obvious. With higher peak CM current requirements, a larger LC parameter is needed, as shown in Fig 4.7.

After all prospective LC parameters are identified, the final solution point is extracted using the loss-weight map of the AC inductor, capacitor, and damping resistor. The relationship between the size of reactive components (\( M_{\text{cm,AC}}, C_{\text{cm,AC}} \)) and real component (\( R_d \)) can provide some insight into the loss-weight map. A larger \( C_{\text{cm,AC}} \) will contribute to higher capacitive DM and CM charging currents (due to low impedance of \( C_{\text{cm,AC}} \)), resulting in higher loss at the expense of the lower weight of \( M_{\text{cm,AC}} \) and vice-versa. Similarly, if \( M_{\text{cm,AC}} \) increases, so does the weight, while the losses on the damping resistor decrease, and vice-versa. The losses across the damping resistor are mainly dictated by sideband and dominant harmonics around \( f_{\text{res}} \). An overestimation would be to take the time integral of energy stored in the capacitor over a switching period. Since there are two charge/discharge cycles in one period, the total power loss \( P_{Rd} \) across the resistors for three phases is given by (4.8). The expression implies that the power loss across the damping resistor increases with switching frequency and DC bus voltage, just as semiconductor losses would. As a result, the damping scheme and CM filter structure are only viable for LV and high current applications.

\[
P_{Rd} \approx C_{\text{cm,AC}} V_{dc}^2 f_{sw} \tag{4.8}
\]
The values of $M_{\text{cm,AC}}$, $C_{\text{cm,AC}}$, and $R_d$ can be estimated per the design procedure from Fig 4.8(a). The system parameters from Table 4-1 are used for trade-off analysis in Fig 4.8(b). The peak CM current is set to 0.5 A, according to motor lifetime requirements illustrated in [10], and several solutions of optimized AC filter combinations are shown. The loss-weight trend of the LCR parameter map from Fig 4.8(b) is shown in Fig 4.8(c). The parameter itself has a direct impact on the system-specific weight. For the case at hand, the design target of the converter was set to 20 kW/kg, which yields the filter parameters in Table 4-2. For the sake of simplicity, the converter design aspect is left out of scope in this dissertation.
4.1.3 Design optimization and experimental verification

A 3D solution map between permeability, weight, and losses of AC choke is obtained from the algorithm specified in Fig 4.9(a), and the results are shown in Fig 4.9 (c,d). The goal is to select the most optimal dimensions that would yield the lowest weight for $M_{cm,AC}$. The constraint in this case is to meet the desired permeability of the core at 10 kHz i.e., $\mu_r = 10000$, typical for FINEMET® cores. The current density of the core winding is fixed at 3.5 A/mm$^2$ for a maximum allowable temperature rise of 25°C under natural convection at high altitude (25,000 ft.). For the same inductance requirement, the effective length $l_e$ can be lower if the PCB winding thickness is higher, as seen from Fig 4.9(c, d). This would result in a lower permeability core requirement. On the contrary, a thinner winding would result in higher $l_e$, since the winding width would have to be increased to maintain the same current density. Consequently, the permeability of the core would have to be increased as well. In this regard, the thickness of the PCB winding should be as high as possible to be within an acceptable permeability range. In addition, an extended core, i.e. higher core depth, is favorable leading to a larger core area $A_e$, at the expense of lower effective length $l_e$.

Table 4-2 Proposed filter parameters

<table>
<thead>
<tr>
<th>Component</th>
<th>Value</th>
<th>Part No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{cm,AC}$</td>
<td>10 $\mu$H @ 10 kHz 30 $\mu$H @ 400</td>
<td>$n = 1, \mu_r = 10000, A_e = 550 \text{ mm}^2, l_e = 224 \text{ mm}$</td>
</tr>
<tr>
<td>$C_{cm,AC}$</td>
<td>1.8 nF per phase</td>
<td>ECQ-UBAF122V5</td>
</tr>
<tr>
<td>$R_d$</td>
<td>400 $\Omega$ per phase</td>
<td>THE series (Ohmite) Chassis mount</td>
</tr>
</tbody>
</table>
The final parameter is chosen from Fig 4.9, indicated by the dashed lines. Three cases with 3-, 6-, and 9-mm total PCB thickness are plotted. Notice that the dashed lines represent the core and winding parameters that would yield the lowest weight. This occurs when the core permeability and PCB thickness has reached closest to the maximum limit specified by the vendor.

The trajectory of peak CM current with respect to $R_d$ is shown according to the test results in Fig 4.10. Three distinct test cases corresponding to different values of $R_d$ are used to assess the performance of the proposed technique. The corresponding time and frequency domain results indicate the peak value and the resonant frequency, respectively. The experimental trajectory of the peak harmonics in frequency domain is indicated in Fig 4.10 (right), with 400 $\Omega$ per phase yielding the lowest peak CM
current out of the three test cases. This is in accordance with the original design criterion. This is further exemplified by the low peak CM current magnitude in time domain, shown in Fig 4.19 (left).

Chassis mount resistors from Ohmite® are mounted on a customized microchannel cold plate [124] next to the SiC power modules (arranged in T-type configuration), as shown in Fig 4.11 (a). The performance of the resistor was evaluated under system and filter parameters from Table 4-1 and Table 4-2, respectively. The steady-state temperature was recorded at 25°C, which was below the maximum case temperature of 100°C for the chassis mount resistor, per Fig 4.11. Water was used as the preferred choice of coolant in this case, although special compounds would be used for high altitude applications. The instantaneous voltage and current waveforms indicate a pulse power of approximately 1 kW dissipated across the resistors. The AC filter interconnections were the focal point for thermal hotspots. A copper block with a 2XM8 screw/nut assembly allows better thermal dissipation, evinced by the rated power thermal test results shown in Fig 4.11. The peak temperature was measured at 66°C and at 21°C ambient.
Finally, a comparison with the state-of-the-art filter structures reveals superior performance of the single turn AC inductor with optimized damper circuit, compared to the existent commercial solutions shown in Table 4-3.
### Table 4-3 Comparison with State-of-the-Art Inverter Output Filters

<table>
<thead>
<tr>
<th>Candidate</th>
<th>Cost</th>
<th>Weight (kg)</th>
<th>Topology</th>
</tr>
</thead>
<tbody>
<tr>
<td>Schaffner line $dv/dt$ filter VW3A5303 [112]</td>
<td>High</td>
<td>29</td>
<td>Multi-stage LCLC</td>
</tr>
<tr>
<td>Schneider [113]</td>
<td>High</td>
<td>2.19</td>
<td>L filter</td>
</tr>
<tr>
<td>CoolBLUE [114]</td>
<td>Low</td>
<td>3.5</td>
<td>Single turn Core</td>
</tr>
<tr>
<td>MTE-DVSG0065E [120]</td>
<td>High</td>
<td>18</td>
<td>DM-CM Integrated inductor</td>
</tr>
<tr>
<td>Invertek drives OPT-2-M3300-00 [121]</td>
<td>High</td>
<td>48</td>
<td>DM-CM Three single phase</td>
</tr>
<tr>
<td>Integrated dampers in busbar [122]</td>
<td>High</td>
<td>NA</td>
<td>Multi-layer bus bar structure</td>
</tr>
<tr>
<td>Parallel LR filter with motor side capacitor</td>
<td>Low</td>
<td>NA</td>
<td>Parallel RL and C filter</td>
</tr>
<tr>
<td>[123]</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>A low inductance based $dv/dt$ filter [123]</td>
<td>Low</td>
<td>1.4</td>
<td>RLC filter using stray inductance</td>
</tr>
<tr>
<td>Proposed CM Filter</td>
<td>Low</td>
<td>1.4</td>
<td>CM inductor with optimized</td>
</tr>
</tbody>
</table>

*Table shows a variety of commercial and laboratory prototypes rated for specified voltage rating from Table 1*

#### 4.1.4 Staggered PWM Scheme for peak bearing current minimization

In this section, the impact of small duty cycles on peak AC-side CM current is discussed. The peak CM current depends on the effective $dv/dt$ at the motor capacitive terminal $C_g$. This can be seen from the experimental result in Fig 4.12(a) with a conventional SPWM scheme. The experiment is conducted using a 3L converter feeding a resistive-inductive (RL) load with an AC CM filter and CM load capacitance to ground. The circuit in Fig 4.2 (c) and test parameters in Table 4-1 ($V_{DC} = 600V$) are followed. The CM current $i_{cm,AC}$ is measured, along with the CMV. In addition, simulation results in MATLAB using forced response for linear time invariant (LTI) state-space model for the circuit in Fig 4.2 (c) are shown in Fig 4.12 (b) with a stepped multi-pulse source as $v_{cm}$ to emulate the staircase pattern of CMV. The turn-on rise time is 20 ns (typical for SiC devices) with $dv/dt$ of 25 V/ns. The variable step times between two consecutive steps $T_x$ are varied.
Due to a small duty cycle between consecutive switching events, the net $\frac{dv}{dt}$ across $C_g$ increases when $T_x$ is small, resulting in a large capacitive CM current. This is shown per encircled markings in Fig 4.12 (a). Approximately, an increase of two times the peak CM current over the expected result can be seen, both in experiment and simulation.

According to the simulation and experiments in time domain, this condition is found to occur when the time difference between two consecutive rising edges of CMV, $T_x$, is lower than the time required to reach the steady-state CM load capacitance voltage ($v_{Cg}$) during the first transient instance denoted by $T_{RC}$. This is also defined as the rise time of the AC filter. As an example, the point marked 1 in Fig 4.12 (b) is used to denote the case when $T_x$ is less than $T_{RC}$. Point 2 represents the case when $T_x = T_{RC}$. From the simulation waveforms in Fig 4.12(b), it can be seen that for Case 1, the second rising edge of $v_{cm}$ occurs before the CMV $v_{Cg,1}$ reaches $\bar{v}_{Cg}$. While for Case 2, the second CMV pulse occurs when the CMV $v_{Cg,2}$ has already reached $\bar{v}_{Cg}$. Here $v_{Cg,x}$ is the voltage across $C_g$ under case ‘x’. It is shown that the peak CM current for Point 1 is higher than Point 2, and this is true for all cases where $T_x$ is less than $T_{RC}$. A similar behavior was studied in [30]. Theoretically, the time step between two consecutive
pulses should be greater than the rise time of the CMV after the filter, as per (4.9), to avoid a jump in peak CM current. Note the rise time can change depending on the structure of the AC filter. The topology per Fig 4.2(c) is referred to in this dissertation.

\[ T_x > T_{RC} \]

\[ T_{RC} \equiv \pi \sqrt{M_{cm,AC} C_{cm,AC}} \]  

(4.9)

Fig 4.13 Simulation spectrum of (a) CMV and CM current \( i_{cm,AC} \) as a function of \( T_x \) (b) CM current transfer gain in dB (A/V)

The frequency domain analysis can be adopted to understand this behavior further. The expression for CM current is given by the transfer function in (4.10), which is plotted in Fig 4.13. From this plot, the peak CM current occurs at the resonant point \( f_{res1} \), given by (4.7). Equation 4.10 implies that a lower peak CM current will either result from lower transfer gain or lower CMV harmonics at the resonant frequency \( f_{res1} \).
\[ G(s) = \frac{sC_g + s^2 R_d C_g C_{cm,AC}}{1 + sR_d C_{cm,AC} + s^2 M_{cm,AC} (C_g + C_{cm,AC}) + s^2 M_{cm,AC} R_d C_g C_{cm,AC}} \]  

\[ i_{cm,AC}(s) = v_{cm}(s)G(s) \]  

(4.10)

Fig 4.14 (a) T-type phase leg (b) 3L switching vector diagram, illustration of the compensation (c) Case 1: between med and max/min vectors of opposite carrier (d) Case 2: between med and max/min vector of same carrier

Next, the conditions for high dv/dt are identified within the switching time \( T_{sw} \). Two cases that result in this phenomenon per carrier shifted PWM are discussed in Fig 4.14. The switching instants corresponding to these events occur during synchronous switching between two phases. As an
example, in Fig 4.14 (a), synchronous switching is observed between Phases B and C, identified as the med and min vector respectively. The corresponding time instants when such transitions (N→O, O→P) occur are given by (4.11).

\[
T_{\text{med},O\rightarrow P} = \frac{2\left|\frac{V_{\text{med}}}{V_{dc}}\right|}{T_{\text{sw}}} \\
T_{\text{min},N\rightarrow O} = \frac{2\left(\frac{v_{dc}}{2} - \left|\frac{v_{\text{min}/\text{max}}}{v_{dc}}\right|\right)}{T_{\text{sw}}}
\]

(4.11)

In real application, however, the step time between two consecutive pulses will fall within a range of \(T_{RC}\) per (4.13). To reduce the \(dv/dt\) at this point, a small duty cycle \(\Delta d\) is injected on two voltage vectors with reverse polarity, per Fig 4.14. This extends the time interval between two consecutive pulses to \(T_{x} > T_{RC}\) and reduces the effective \(dv/dt\) as shown in Fig 4.14. Hence, if \(T_{x}\) is greater than \(T_{RC}\) then the high effective \(dv/dt\) condition can be avoided per (4.13).

Fig 4.15 Impact of dead time on CMV (a, b, c) Transition modes between P-O (d) Phase voltage with and without dead time (e) Impact of phase current polarity on phase voltages and CMV pulses
During implementation, the impact of dead time needs to be considered [125] as it would dictate the polarity of the injected duty cycle. For example, as per Fig 4.15, considering the case when there is a voltage transition of Phase A leg from O to P. The switching states for S1–S4 are shown in Fig 4.15(d) and compared with and without dead time effect. The impact of dead time is seen when S3 turns off (Fig 4.15(b)) and the free-wheeling diode of S1 starts conducting depending on the direction of output current $i_{out}$. This results in two cases for the output voltage, depending on current polarity ($i_{out} > 0$ and $i_{out} < 0$) as per Fig 4.15 (d). Now let’s say another transition occurs for Phase C from O to N, and Phase B is held at a constant state (no switching). Then the impact of dead time is seen in the form of CMV glitches, illustrated in Fig 4.15(e). The period of this glitch is the dead time $T_d$. An example of dead time compensation is demonstrated in [126] with the common mode voltage elimination (CME) modulation scheme to account for such glitches.

The dead time $T_d$ will naturally increase the $dv/dt$. As such, its effect must be compensated. This is illustrated in Fig 4.16. Depending on the current polarity of med and min/max current vectors, the polarity of the injected duty cycle $\Delta d_z$ for the corresponding med and min/max voltages can be decided. In either case, the dead time will result in an increase of the step time between consecutive pulses, as shown in Fig 4.16(a, b) by time interval $T_d$. 

\[
T_{\text{min},N\rightarrow O} - T_{\text{med},O\rightarrow P} \rightarrow 0
\]  

\[
T_{\text{min},N\rightarrow O} - T_{\text{med},O\rightarrow P} > T_{RC}
\]
Fig 4.16 Impact of dead time on staggered CMV (a) Negative injection for $v_{bo}$, (b) Positive injection for $v_{co}$
(example of implementation from Fig 4.14(a))

To compensate for the impact of dead time, the expression per (4.14) is obtained, where the additional time difference between two consecutive steps (i.e. $T_d$) is added to the original expression to account for dead time effect in (4.13). Simply put, when the time steps of med and min vectors are equal, the time difference is $T_d$. The deciding criteria is therefore modified per (4.14-4.15), and the final compensation scheme is implemented as per Fig 4.17. The goal is to contain the time step between two signals to be greater than or equal to $T_{RC}$, as per Fig 4.17 (a), such that the jump in peak CM current does not occur. Subsequently, the minimum amount of injected duty cycle can be calculated per (4.16) for Case (a) in Fig 4.16 and can be extended to Case (b) as well. Note that the polarity of injected voltage $\Delta d_z$ does not depend on the sampling method, i.e. direction of carrier after each interrupt is invoked.
\[
\left| v_{\text{med}} \right| - \left( \frac{v_{\text{dc}}}{2} - \left| v_{\min/\max} \right| \right) T_{\text{sw}} + T_d < T_{RC}
\]

\[
\left| v_{\text{med}} \right| - \left| v_{\min/\max} \right| T_{\text{sw}} + T_d < T_{RC}
\]

\[
\Delta d_z = \frac{T_{RC} - T_d}{T_{\text{sw}}} - \left| v_{\text{med}} \right| - \left( \frac{v_{\text{dc}}}{2} - \left| v_{\min/\max} \right| \right)
\]

\[
n_{\text{out,med}} > 0
\]

\[
n_{\text{out,min}} < 0
\]

\[
(13) \text{ satisfied?}
\]

\[
\text{Yes}
\]

\[
\begin{align*}
|d_{\text{med}}| &= d_{\text{med}} + \Delta d_z \\
|d_{\text{min}}| &= d_{\text{min}} - \Delta d_z \\
\end{align*}
\]

\[
|d_{\text{med}}| = d_{\text{med}} - \Delta d_z \\
|d_{\text{min}}| = d_{\text{min}} + \Delta d_z \\
\]

\[
(14) \text{ satisfied?}
\]

\[
\text{Yes}
\]

\[
|d_{\text{med}}| = d_{\text{med}} + \Delta d_z \\
|d_{\text{min}}| = d_{\text{min}} - \Delta d_z \\
\]

The range of injected duty cycle, $\Delta d_z$, depends on the AC CM filter parameters and dead time. Typically, dead time for SiC applications lies between 150 – 300 ns, while the rise time of the AC CM filter lies between 1–3 µs, resulting in an injected duty cycle range between 0.02- 0.05. This slight variation in duty cycle was found to have negligible effect on THD. A simulation example using MATLAB and PLECS Blockset is shown in Fig 4.18 representing Case (a) from Fig 4.16. The three-level T-type inverter prototype used for verification is shown in Fig 4.1 (top). The filter and converter parameters are shown in Table 4-1 and Table 4-2. The three-phase RL load test setup is used where the CM load impedance is added to mimic stray load capacitance and inductance, as per Fig 4.1 and Fig 4.2.
The inverter CMV and corresponding CM current profile is shown in Fig 4.18 (right) for DC bus voltage of 740 VDC and line frequency of 1.75 kHz.

Fig 4.18 Left: Simulation example for Case (1) from Fig 4.14 Right: Experimental result for CM current (top) Experimental result for CMV (bottom)

Table 4-4 summarizes the selected PWM schemes and the corresponding conditions when transitions would occur. The algorithm can be scaled accordingly based on these conditions.

**Table 4-4 Extension of staggered switching pattern**

<table>
<thead>
<tr>
<th>PWM Scheme</th>
<th>Condition for staggered switching</th>
</tr>
</thead>
<tbody>
<tr>
<td>LMZVM</td>
<td>(2\left</td>
</tr>
<tr>
<td>MMS-LMZVM (exception of zero crossing of med vector)</td>
<td>(2\left</td>
</tr>
</tbody>
</table>
4.2 Design of DC-Side Integrated DM-CM Filter

4.2.1 Guidelines for DC-side CM/DM noise reduction, using simplified equivalent circuits for 3L T-type configuration.

Considering the given power rating, device availability, CMV levels, and efficiency requirements, SiC modules from GE (i.e. GE12047BCA3) were used in this study in a T-type inverter configuration. The detailed schematic of the three-phase motor drive under study is shown in Fig 4.19. The inverter is categorized into three sections. The DC filter and bus bar assembly are denoted as Section A, the module and gate driver assembly as Section B, and the AC filter as Section C. Lumped RLC elements are used to denote the high frequency parasitic influence. Each section is systematically evaluated in the following sub-sections. Initially, the resonant modes from the simulated CM and DM noise transfer gains, shown in Fig 4.20, are analyzed.

Fig 4.19 Detailed schematic of high-power three-phase, three-level T-type inverter with parasitic components highlighted

From the DM circuit, the inverter and decoupling board high frequency lumped model for three-phases are highlighted in gray, green, and pink in Fig 4.21(a). Three pulsed current sources are used to generate the device currents for S1, S2/S3, and S4, and hence three-phase load currents and a DC-side
DM current component can be reproduced. A lumped LC model for the DC bus bar and decoupling board captures the two resonant modes, $f_{\text{res}4}$ and $f_{\text{res}5}$, arising from the commutation loop mixed frequency resonance during switching transient. The decoupling board is designed to localize the high frequency commutation loop of the switching transient, and therefore shift the high frequency resonant component $f_{\text{res}5}$, possibly beyond 30 MHz by tuning the AC layer inductance (since there is a less stringent DO-160 limit line beyond 30 MHz). Details on the decoupling mechanism are provided in [127][128]. To further suppress both low and high frequency modes [129][130] eventually in the EMI spectrum, 3rd order DC-side DM filters represented by $M_{\text{dm,DC1}}, C_{\text{dm,DC1}}$, and $C_{\text{dm,DC2}}$ are added. The inductance of the leading cable can also be used to suppress the high frequency noise components.

Fig 4.20 (a) DM noise transfer gain (b) CM noise transfer gain of the proposed filter-inverter structure without second stages ($M_{\text{cm,DC2}}$ and $C_{\text{cm,DC2}}$).
Similarly, the CM noise transfer gain reveals the resonant modes produced by the interaction between DC-side, motor (AC load), and AC filter impedance i.e., $f_{res1}$ and $f_{res3}$. As expected, the magnitude of the transfer gain is lower with additional CM filtering elements. The coupled nature of the AC and DC-side is evinced by the simultaneous reduction in DC-CM noise transfer gain with additional AC and DC filter stages. Note that the commutation loop resonant component is absent from the simulated CM noise transfer gain, as an ideal source is considered for CMV excitation in Fig 4.21(b). The correlation between these resonant modes and measured spectrum will be discussed later in section 4.2.4. First, the hardware realization and characterization of each DC filter design feature is presented in the following subsections. The challenges pertaining to high altitude design and the recommended solutions are discussed as well.
4.2.2 Compact integrated DM-CM filter using PCB-embedded AMR current sensor

The DC-side filter design process follows a sequential design flow, starting with an AC CM filter design, followed by the DC CM filter design. The coupled nature of CM noise between the AC and DC-sides is considered by first adding a Y-capacitor ($C_{cm,DC1}$) from the DC terminal to ground, which yields the circuit in Fig 4.2(c). After the AC filter ($M_{cm,AC}$ and $C_{cm,AC}$) are designed, the DC-side CM parameter ($M_{cm,DC1}$) can be sized from the corner frequency computation, per the equivalent circuit in Fig 4.21 (b) (ignoring second stage CM filter – $C_{cm,DC2}$). The DM filter design follows after the CM filter parameters (AC and DC) are identified. Here, the equivalent network in Fig 4.21 (a) is used to derive the raw DM noise, attenuation requirement, and compute the required corner frequency. The DM LC parameters can be identified as a result.

![Diagram](image)

Fig 4.22 High-level design methodology for integrated DM-CM filter parameter extraction (b) Simulated CM noise spectrum (d) Simulated DM noise spectrum
The DM and CM LC parameter selection is based on conventional design rules per [31], and is elucidated in Fig 4.22. From the LC parameters, the required form factor is based on the same idea as was expressed in the previous section with the AC filter. Fig 4.23 illustrates the high-level iterative flow-chart for the design of the proposed DM + CM integrated structure. Details on the hardware realization for the DM and CM conducted emissions, i.e. the DC filter block along with the AC filter, are presented in [104].

The DC filter hardware comprises an integrated DM-CM core with a multi-winding PCB arrangement, combined with the DC bus bar shown in Fig 4.24. The DC bus bar houses the bulk DC capacitors $C_{bus}$ and the first stage CM DC capacitor to ground $C_{cm,DC1}$. The rest of the DC filters are housed in the DC filter block per Fig 4.24(a), containing an integrated DM-CM core ($M_{dm,DC1}$, $M_{cm,DC1}$), DM capacitors ($C_{dm,DC1}$, $C_{dm,DC2}$) and second stage CM capacitor $C_{cm,DC2}$. From the stack-up of the DC bus bar and filter, shown in Fig 4.24, ground layers are added on the top and bottom layers, which act as shielding for electric field control (grading along the edges) [96]. Complementing this, the ground
layers serve as an access point for external grounding of the CM capacitors. The grounding of CM capacitors is realized using a novel edge plating technique per Fig 4.24 (a, b, c), wherein an exposed conductive solder-mask around the periphery of the PCB is bonded to the aluminum enclosure. The path for CM currents to ground is highlighted in Fig 4.24(b). The shortest path to ground ensures the lowest inductance, and therefore superior high frequency attenuation. This is particularly important to avoid ground impedance coupling on the LISN terminal at the input. However, the ESL of film capacitors itself produces a low self-resonant frequency (< 1 MHz), which can deteriorate the filter performance at high frequencies. To compensate for the parasitic effects of the first stage CM capacitor ($C_{cm,DC1}$), an additional second stage CM capacitor $C_{cm,DC2}$ (surface mount film capacitor with low ESL) is placed near the DC input terminal after the CM choke $M_{cm,DC1}$, as shown in Fig 4.24 (b). These capacitors additionally are useful to suppress the mixed mode resonance $f_{res,5}$, due to high frequency switching transients as discussed earlier. Note that the ground impedance of this leading capacitor and the grounding network in general near the DC input terminal is critical to ensure a sufficient wide-band attenuation performance to avoid amplification of noise at lower and mid-frequency [131]. Nanocrystalline cores are preferred for the main filter block, due to their high attenuation per unit volume.
The AMR sensor technology is incorporated for DC-side current sensing as an added feature and is shown in Fig 4.24. The U-shaped busbar feature results in differential H-fields along the x- and y-axis, which is proportional to the current flowing through the bar. The sensor CFS1000 from Sensitec [132] is used, due to its high bandwidth (500 kHz) and immunity to stray magnetic fields. The corresponding output current from the IC is then fed to the signal conditioning circuit, where the output from three sensors is added and transmitted to the controller using a SCI, SPI, or SDFM interface. In this case, the SCI communication protocol was favorable, due to lower device count and the use of only one fiber channel to transmit data between signal conditioning circuit and controller. The architecture of the AMR sensor is shown in Fig 4.25. Note that the AMR sensor pads are also exposed to peak E-field due to the HV (high voltage) bus bar at the bottom node. This problem can be avoided by adding a ground shielding layer underneath the pads but not under the IC. A notch is created to avoid interference with the IC (eddy currents induced on the ground plane) per the illustration in Fig 4.25.
4.2.3 Impact of decoupling board, edge plating, feed-through connection

The power stage design is critical for this LV, high current application to minimize voltage overshoots and maximize commutation loop ringing frequency. For clearance and creepage requirements (especially in aerospace applications), the interconnection between the module and DC bus bar terminals is relatively large. This implies that the use of longer standoffs with higher stray inductance would result in large undamped device voltage oscillations while switching. The commutation loop resonant frequencies during such transients determine the DM spectrum frequency components, i.e. $f_{res2}$, $f_{res4}$ and $f_{res5}$ in Fig 4.20 (a). Consequently, the resonant frequencies (especially the higher end $f_{res,5}$) would be low and would appear around the mid-high frequency band of the EMI spectrum, potentially resulting in failure to meet the EMI standard. To account for these components in the spectrum, a unique arrangement of the AC decoupling layer, DC and AC bus bar, is proposed as illustrated in Fig 4.26(a). Crucially, the Rogowski coil-based current sensor can be embedded in this decoupling board for device current measurements. A localized commutation loop is generated close to the power module as illustrated in Fig 4.26(b). Two loops, namely the long loop involving DC bus ($C_{bus}$) and decoupling capacitors ($C_{dec}$), and the short loop with a decoupling capacitor and $C_{oss}$ of S3 are generated. During the turn on of S1, $C_{oss}$ of S2 charges to $V_{dc}/2$, resulting in the two loops
mentioned above. The decoupling board provides a path for the short loop, described in detail in [105] and denoted by the red trace in Fig 4.26(b). The AC layer is shown in the top layers of the decoupling board. The transient current is measured during the transition from the O- P state, i.e. turn on of S1 in Fig 4.26(c). The corresponding frequency spectrum shows the high frequency attenuation provided by the decoupling path.

The loop inductance provided by the AC layer on the decoupling board is smaller than the DC bus bar, and in combination with the total loop inductance per (1), the mixed frequency commutation loop resonances $f_{\text{res},4}$ and $f_{\text{res},5}$ can be deduced as (4.18). Where $L_{\text{loop\_short}}$ and $L_{\text{loop\_long}}$ are the equivalent loop inductances of the short and long loops respectively and can be expressed as (4.17). Note that in (4.18), the impact of $C_{\text{dec}}$ is neglected because it is relatively larger than $C_{\text{oss}}$ and lies in series with it. Ideally the decoupling capacitor, placed on the decoupling board, must be selected to ensure the two frequencies are separated by at least a decade (i.e., $f_{\text{res},5} > 10f_{\text{res},4}$). And the inner resonant frequency ($f_{\text{res},5}$) is beyond the EMI frequency band upper limit (30 MHz, for frequencies > 30 MHz a 30 dB limit is used) with this arrangement. However, this is also limited by the $C_{\text{oss}}$ and module stray inductances. In this application, $f_{\text{res},5}$ of 27 MHz is achieved. The decoupling board is realized using a heavy copper PCB. The use of a single laminated bus bar [133] is cumbersome with this arrangement, due to the need for embedding the sensing coil within the laminate.
Fig 4.26 (a) Decoupling board and module arrangement using dual module GE12047BCA3 rated for 1.2 kV/475A (b) Commutation loop illustration O-P state with decoupled path (c) Impact of decoupling path on loop resonance – Measured device current and outer loop current using commercial Rogowski coil and corresponding FFT signature

\[
\begin{align*}
L_{\text{loop short}} &= L_{\text{Cdec}} + L_{\text{ac1}} + L_{\text{ac2}} \\
L_{\text{loop long}} &= L_{\text{Chas}} + L_{\text{Neutral}} + L_{\text{Cdec}} \\
\end{align*}
\]

(4.17)

\[
\begin{align*}
f_{\text{res,4}} &= \frac{1}{2\pi} \sqrt{\frac{1}{C_{\text{dec}} L_{\text{loop long}}}} \\
f_{\text{res,5}} &= \frac{1}{2\pi} \sqrt{\frac{1}{C_{\text{out}} L_{\text{loop short}}}} \\
\end{align*}
\]

(4.18)

The edge plating technique is proposed to improve ground impedance characteristics (close to ideal ground), and the impact is shown in Fig 4.27. A significant improvement around high frequency (near 10 MHz) is seen, as well as for the switching resonant components in the VHF band near 30 MHz. A comparison is drawn with a previous version of the prototype shown in Fig 4.27 (b), where a 5 cm long round conductor is used to ground the first stage CM capacitor \( C_{\text{cm,DC1}} \) via the DC filter box. The inductance of the wire contributes to significant ground inductance, thereby enhancing the ground path impedance, the effects of which are discussed in detail in [131].
Fig 4.27 Impact of (a) Edge plating for filter and bus bar grounding (b) version 1 grounding, (c) version 2 grounding scheme

For the second version, edge plating on the PCB is bonded with the enclosure throughout the four edges to ensure a $360^\circ$ termination, bypassing the ground wire. The measured inductance of the ground wire was 8 nH, compared to the PCB planar inductance of 3.48 nH using planar rectangular sheet approximation [134].

The feedthrough cable provides a transmission line filtering effect in conjunction with ferrite clamp cores [135]. Overall, a high frequency component can be mitigated using this assembly. A shielded high-power connector and cable assembly is added after the second stage CM capacitor, as shown in Fig 4.28 (a). A $360^\circ$ shield jacket termination is the most reliable and low impedance grounding solution. Using this 1m feedthrough cable integrated within the assembly, the net second stage CM capacitance is enhanced only by 0.2 nF for a AWG2 cable. Although this value is only marginal, the net impact on the spectrum can be significant, as seen in Fig 4.28 (b). Particularly if the ground impedance between
the enclosure and DC filter block is high, the feedthrough cable can provide the path of least resistance for CM ground currents and improve mid and high frequency attenuation. The shield wire can be tied directly to the edge plating on the PCB. The resulting effect on CM noise transfer gain is shown in Fig 4.28(c). Again, the plots here are color-coded and consistent with the measurements. A gradual reduction in noise level is seen with the addition of a feedthrough cable and ferrite cores [136]. Note that the shielded cables are also mandatory for radiated emissions compliance (though out of scope in this dissertation).

Fig 4.28 (a) Feedthrough cable and grounding of outer shield jacket (b) Impact of feedthrough cable and CM capacitor (C_{cm,DC2}) (c) Correlation with DC-CM noise transfer gain
4.2.4 Characterization and dynamic test results

A detailed characterization of the inverter/filter for CM and DM noise propagation is performed. Power cables and instrumentation lines are lifted off the ground plane. The enclosure and test setup are shown in Fig 4.29. Prior to power line noise measurements, the background noise is ensured to be well below the standard limit. Conducted noise measurements (current) are taken using a high frequency current transformer (HFCT) with a bandwidth of 1.25 GHz, under the CM and DM configurations in Fig 4.21. The saturation limit of the HFCT (300 A) is well above the target DC-side current rating. The tests are performed on a 200-kW unit at 740 VDC bus, with a rated output frequency of 400 Hz, switching at 20 kHz. The inverter output dv/dt is set at 25 V/ns.

<table>
<thead>
<tr>
<th>Mode</th>
<th>Calculated</th>
<th>Measured</th>
<th>% Error</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{res,1}$ (AC load and filter)</td>
<td>500 kHz</td>
<td>450 kHz</td>
<td>10</td>
</tr>
<tr>
<td>$f_{res,2}$ (DC bus resonance)</td>
<td>1 MHz</td>
<td>900 kHz</td>
<td>11.11</td>
</tr>
<tr>
<td>$f_{res,3}$ (AC load and filter)</td>
<td>2 MHz</td>
<td>2.1 MHz</td>
<td>5</td>
</tr>
<tr>
<td>$f_{res,4}$ (outer commutation)</td>
<td>540 kHz</td>
<td>Unremarkable</td>
<td>NA</td>
</tr>
<tr>
<td>$f_{res,5}$ (inner commutation)</td>
<td>27 MHz</td>
<td>20-25 MHz</td>
<td>7.04 – 10</td>
</tr>
</tbody>
</table>

The impact on the CM noise spectrum due to the addition of each filter subcomponent is investigated in Fig 4.30. A correlation with computed transfer per Fig 4.20 is made. The resonant modes from the simulated transfer gains are compared against the experimental findings in Table 4-5. In most cases, the error is within 10%, however it also depends on measurement accuracy. As expected, the attenuation to CM noise improves with the addition of each successive filter stage.

Partial noise measurements reveal the most suitable filter configuration that can minimize the conducted emissions and meet the limit lines as closely as possible. The final measured CM and DM emissions at the DC terminal are shown in Fig 4.31(a), while the rated power operation is demonstrated in Fig 4.31(b). The filter weight breakdown of the proposed solution is shown in Table 4-6.
Fig 4.29 EMI test setup for compliance testing

Fig 4.30 Passive emissions measurement (a) Impact of first stage CM capacitor on CM noise (b) Impact of full DC-side filter on CM noise (c) Impact of full AC and DC-side filter on CM noise

Fig 4.31 Measured (a) CM noise spectra at the LISN terminal based on the proposed solution (b) DM noise spectra at the LISN terminal based on the proposed solution (c) Rated power operation under reactive load
Table 4-6 Filter weight breakdown for a 211 kW inverter

<table>
<thead>
<tr>
<th>Component</th>
<th>Weight</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>AC Filter Assembly (M_{cm,AC}, R_d, ) (C_{cm,AC})</td>
<td>1.4</td>
<td>(M_{cm,AC} = 41 , \mu\text{H} ) Single turn nanocrystalline oval core, (\mu_r = 20000) at 10 kHz  (R_d = 500 , \Omega) per phase TGHDX1K00JE, Chassis mount resistors (C_{cm,AC} = 5 , \text{nF} ) per phase – PME295RB4470MR30  (M_{cm,DC1} = 100 , \mu\text{H}, ) integrated DM-CM core, (\mu_r = 20000) at 10 kHz</td>
</tr>
<tr>
<td>DC Filter Assembly (M_{cm,DC1}, C_{cm,DC2}, M_{dm,DC1}, C_{dm,DC1/2})</td>
<td>2.2</td>
<td>(C_{cm,DC2} = 1.5 , \mu\text{F}, ) 80-CKC21X682JJGCAUTO, Ceramic Capacitors  (M_{dm,DC1} = 1 , \mu\text{H}, ) integrated DM-CM core  (C_{dm,DC1} = 30 , \text{nF}, ) C4AQQBU4500A11J, Film Capacitors</td>
</tr>
<tr>
<td>DC Bus bar (C_{bus}, C_{cm,DC1})</td>
<td>2</td>
<td>(C_{bus} = 300 , \mu\text{F} ) total, B32776Z5506K000, Film Capacitors  (C_{cm,DC1} = 1.5 , \mu\text{F}, ) B32023A3154M189, Film Capacitors</td>
</tr>
<tr>
<td>Feedthrough cable and clamp on ferrite cores</td>
<td>1</td>
<td>Heavy Duty Power Connectors/Male, 654-PL182X-301-70  Heavy Duty Power Connectors/Female, 654-PL082X-301-10D8  Ferrite clamp on cores, 80-ESD-SR-110G</td>
</tr>
<tr>
<td>Decoupling board (C_{dec})</td>
<td>0.7</td>
<td>0.75 , \mu\text{F} 700 , \text{V}, B58035U9754M062</td>
</tr>
<tr>
<td>Total filter weight with Al Enclosure</td>
<td>12.3</td>
<td>As per Fig. 4.1</td>
</tr>
</tbody>
</table>
4.2.4 Partial discharge mitigation and test results

One of the aspects to consider while designing airborne applications is the severity of the partial discharge (PD) phenomenon with higher altitude in Paschen’s law [137]. The peak limit for an electric field in the air with a 50% allowable margin comes to be 700 V/mm for an altitude of 25000 ft. This condition must be guaranteed for safe and reliable system operation. Shielding strategies, such as field grading techniques, are employed to handle the peak electric field (surface electric field). As an example, the PD mitigation strategy for a core and winding arrangement in the integrated DM+CM filter structure is shown in Fig 4.32. A potential gradient exists between the grounded core and the HV winding, which would exceed the peak limit per Fig 4.32.

Fig 4.32 (a) Electric field simulation along core edge (b) Shielding principle (c) PD test results in altitude chamber
Notably, the PCB-FR4 material can handle much higher peak E-field levels compared to air, irrespective of altitude; as such, the idea is to localize the peak electric field within the PCB dielectric. This is achieved by field grading using multiple traces of opposing potential (in this case, GND net) to avoid peak surface E-field in the air [138][139][140][141]. The result is a much lower peak E-field (<700 V/mm), which meets the criterion. A high-altitude test result (phase resolved PD plot in Fig 4.32 (c)) indicates that the voltage across DC bus to ground net can reach up to 1.8 kV\textsubscript{RMS} without any noticeable signs of failure or breakdown. Note that for certain applications, the DC bus to ground potential can be a safety issue, in which case special conditioning circuits are used to discharge the bus after shutdown [142].

### 4.3 Summary and Conclusion

This section presents characterization and mitigation of conducted emissions at the inverter and filter sub-system level for a high-power motor drive. Specifically, the application to high altitude airborne motor control unit is shown. Design practices are suggested to better control the emissions within the inverter such as integration of a DC bus bar with a unique high current multi-turn PCB-based DC-EMI filter, edge plating and feedthrough cable for low ground impedance, optimal damping of motor load resonant modes using an AC filter with RC shunt network, and ferrite clamp cores for impedance mismatch at the VHF band. In addition, a decoupling board embedded with the gate driver is proposed to minimize effective loop inductances, significantly suppressing switching transient resonant modes at the DC terminal. A low-cost system grounding and control architecture for reliable and safe operation at rated power is presented. The proposed design practices are implemented and characterized on a 200 kW inverter. However, there are obvious limitations of the proposed solutions as stated below.
First, the upper constraint on the maximum allowable Y-capacitor ($C_{cm,DC1}$) for a given application can have a significant impact on weight distribution. Efforts to relax the DO-160 standard or leakage current limit could alleviate this constraint.

While the low frequency content can be estimated prior to hardware design, the high frequency noise components require additional efforts, either through trial-and-error or behavioral/terminal modeling [143]. Typically, additional stages using multi-layer ceramic capacitors or ferrite core clamps are favorable. However, customized clamps rated for high currents would be required to avoid saturation from leakage / stray H-fields.

From the DM noise measurements, it was evident that commutation loop resonance could not be shifted further toward the VHF range, since it is limited by package stray inductance and form factor of the assembly. As such, a leading DM inductor at the system input is recommended in the form of a cable or a discrete inductor (depending on the value). Since EMI signature is highly sensitive to the VFD installation scheme [144], final system assembly should be closely representative to the EMI test bed.

In summary, the impact of filter and converter parasitics on the high frequency range of the EMI spectrum cannot be neglected. Efforts to address these issues during the design phase must be enforced. An example is shown in Chapter 5 with a back-to-back converter arrangement.
Chapter 5. Desensitization of Critical Filter Parasitic Elements

The design of high-density FBBs have been demonstrated and validated in the previous chapters successfully. Nevertheless, a highly integrated FBB can result in pronounced parasitic effects, which could outweigh the benefits of filter design and optimization. Therefore, analytical methods to estimate filter parasitics, for example as shown in [145], and their inclusion in lumped models to capture high frequency behavior in simulations (deterioration of attenuation, resonance, etc.) is performed. In addition, techniques to mitigate high frequency effects have been demonstrated.

First, this chapter proposes a systematic design methodology for a back-to-back (BtB) bridge filter structure to be used with three-phase bidirectional AC-AC converters (active front end), feeding a motor with long unshielded cables. The bridge provides a path for circulating low frequency CM harmonics, resulting in low motor bearing voltage, suppression of motor winding over-voltage, superior low frequency conducted emissions attenuation, and wide bandwidth performance. The proposed filter structure is designed using simplified sets of derived analytical attenuation pertaining to different groups of harmonics. Consequently, each filter component is optimized for low weight, using specific core materials depending on current ripple content. Following the physical design, parasitic models for the converter, filter, motor, and long cables are developed in the time domain to allow prediction of CM and DM voltages to assess their impact on high frequency emissions. The overall design methodology is validated through emissions characterization using a 15 kW rated 3L-NPC converter in a BtB configuration.

Measures to compensate for parasitic effects, such as a reducing mutual coupling between inductor and capacitor, avoiding anti-resonance of the boost inductor and optimizing FBB layout are proposed. These measures would serve as design guidelines for filter design considering parasitic impact on HF emissions.
5.1 Sensitivity Analysis on Filter Subcomponents

Fig 5.1 (a) State-of-the-art BtB system under consideration (b) Conducted emissions standard used in this study, the IEC–61800-3-12, Class A (first environment public low-voltage network) – Standard C2 (industrial application – solid blue line); grid interface follows CISPR-11 regulations

First, the BtB system is described. In prior articles, the typical subsystem of a motor drive system in Fig 5.1(a) is discussed at length. The long cable, motor, and converters generate parasitic CM currents that can compromise the motor bearings and winding insulation, induce device over-voltages and stress, as well as affect the conducted and radiated emissions at the AC input terminal [146][147][148]. Surely, separate characterization of inverter and grid-side filters has been discussed in prior literature. For instance, Jouanne et. al [149] performed a systematic characterization for a permanent magnet synchronous machine (PMSM) drive, while the impact of long cable has been studied by Huang in [150]. Separate grid and inverter-side filters are formulated and analyzed in [151][152]. The earliest known filter structure for AC-AC systems was proposed by Akagi [146] and is traditionally adopted as the benchmark filter for BtB systems. Structural modification of this baseline topology, by providing a low impedance shunt pass toward the DC bus midpoint, was found to be feasible for low frequency attenuation as demonstrated in [152]. Notwithstanding the above, very few articles have reported the behavior of a BtB system with long cables on conducted emissions.

Traditionally, long cables have been studied extensively in literature as a potent contributor of conducted and radiated emissions. The effects are pronounced with longer cable lengths in terms of voltage reflection, charging currents [148], and EMI noise [150]. In this regard, high frequency cable
models have been developed to better understand and quantify the impact of long cables on the overall system power quality.

To facilitate the design of the proposed filter structure, a representative full system wide-band frequency model, which includes the converter high frequency models [153][154][155], models for propagation impedances [156], and filter sub-component models, is desired. High frequency models for CM inductors [157], multi-winding transformers [145], and half-bridge modules are discussed in prior articles, but their implications on the full three-phase BtB system are not covered. Furthermore, improving the bandwidth of these models, the impact of non-linear frequency effects, and extending to other core types can be considered. Following this point, the developed lumped parasitic models should be able to capture the low, mid, and high-frequency phenomena for accurate filter parameter selection. This dissertation uses pre-existing concepts and leverages them to design and optimize a bridge filter interconnection scheme for a BtB system.

5.1.1 Bridge topology for BtB AC-AC systems

The schematic of the three-phase motor drive with relevant parasitic components under study is shown in Fig 5.2 also described in detail in [158]. The system and filter parameters are listed in Table 5-1 and Table 5-2, respectively. The structure in Fig 5.2 comprises the bridge connection, which aids in circulation of low frequency CM current components between the rectifier and inverter through the star-point of the DM capacitor arrangements (C_{dm1,grid} and C_{dm1,motor}) on either side. To suppress the low frequency CM circulating components within the inner loop, either during start-up or low speed operation, an additional DC CM inductor L_{cm,DC} is added as shown in Fig 5.2. Clearly, the bridge connection can provide superior low frequency attenuation, but it is rendered useless when CM ground currents are generated by the converter as seen from the per-phase equivalent circuit in Fig 5.2 (b). Hence, the grid-side CM filter components, i.e. L_{cm1,grid}, L_{cm2,grid} and C_{cm1,grid}, are added for high
frequency CM-EMI attenuation from the converter ground current, as well as cable and motor leakage currents.

Another aspect includes the motor bearing CMV reduction facilitated by the circulation of CM current through the bridge interconnection. In addition, the DM filter inductor and capacitor \( \{L_{dm1,motor} \text{ and } C_{dm1,motor}\} \) network at the inverter output terminal serves as a sine filter for reflected wave mitigation. Hence, a seamless integration of the DM filter at the inverter output and rectifier input through CM bridge interconnection is feasible for this application. The grid-side DM filter composed of \( L_{dm1,grid}, C_{dm1,grid} \text{ and } L_{dm2,grid} \) is designed to meet the power quality and DM-EMI noise limits at the LISN terminal. The boundary conditions for a typical LCL filter are followed as stated in Table 5-2, per [159][160].

### Table 5-1 System parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Rating</td>
<td>15 kW</td>
</tr>
<tr>
<td>Phase-Phase Voltage</td>
<td>400 VAC</td>
</tr>
<tr>
<td>DC-Bus Voltage</td>
<td>700 V</td>
</tr>
<tr>
<td>Line Frequency</td>
<td>60 Hz</td>
</tr>
<tr>
<td>Switching Frequency</td>
<td>48 kHz</td>
</tr>
</tbody>
</table>

### Table 5-2 Filter parameters and boundary values under consideration

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Boundary Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>DC CM inductance (mutual)</td>
<td>(L_{cm,DC})</td>
<td>Peak-to-peak CM current ripple at (f_{bridge}) = 125% (I_{comp,PK})</td>
</tr>
<tr>
<td>First stage LCL inductance (per-phase)</td>
<td>(L_{dm1,grid})</td>
<td>Peak-to-peak DM current ripple = 25% (I_{comp,PK})</td>
</tr>
<tr>
<td>Second stage LCL inductance (per-phase)</td>
<td>(L_{dm2,grid})</td>
<td>Req. DM attenuation and current harmonics limit[159][160]</td>
</tr>
<tr>
<td>First stage CM inductance on grid-side (mutual)</td>
<td>(L_{cm1,grid})</td>
<td>Attenuation requirement from second stage per eq: (3)</td>
</tr>
<tr>
<td>Second stage CM inductance on grid-side (mutual)</td>
<td>(L_{cm2,grid})</td>
<td>Attenuation requirement from second stage per eq: (3)</td>
</tr>
<tr>
<td>Motor side inductance (per-phase)</td>
<td>(L_{dm1,motor})</td>
<td>(dv/dt) limit at motor terminal, (T_{rise}) of (V_{line-line})</td>
</tr>
<tr>
<td>Grid-side first stage DM capacitance</td>
<td>(C_{cm1})</td>
<td>5% Reactive power compensation</td>
</tr>
<tr>
<td>Grid-side second stage DM capacitance</td>
<td>(C_{cm2})</td>
<td>Req. DM attenuation [157][159] &amp; CM attenuation per eq: (4)</td>
</tr>
<tr>
<td>Grid-side CM capacitance to ground</td>
<td>(C_{cm,grid})</td>
<td>Max leakage current limit (</td>
</tr>
<tr>
<td>Lumped converter parasitic capacitance to ground</td>
<td>(V_{cm,rec})</td>
<td>Extracted from [9]</td>
</tr>
<tr>
<td></td>
<td>(V_{cm,inv})</td>
<td>Rectifier CMV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Inverter CMV</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>NA</td>
</tr>
</tbody>
</table>

* Maximum permeability degradation for powder core is taken to be 10% from initial value at 1 kHz
Fig 5.2 (a) Schematic of the proposed bridge structure for three-phase BtB motor drive with high frequency parasitic models for converter, filter, long cable, and motor (b) Per-phase simplified CM-equivalent circuit of the proposed structure

The DM and CM component design guidelines are described in brief below:

The DM filter at inverter output \{L_{dm1,motor}, C_{dm1,motor}\} is selected according to the $dv/dt$ constraint for motor line-to-line voltage. It follows that based on a specific voltage rise time, $t_r$, the DM filter inductor and capacitor selection can be tuned per Equation (5.1). Here the corner frequency $f_c$ is chosen to provide attenuation greater than 3 dB for the rising edge of inverter line-to-line voltage, i.e. $f_c >> f_r$, where $f_r$ is the inverse of step voltage rise time. The motor nameplate data can be used to verify loss calculations across LC filter at the inverter output terminal as shown in [161], and can be used as an added constraint for this LC parameter tuning.

$$20 \log_{10} \left| 1 - \omega_c^2 \frac{L_{dm1,motor}}{C_{dm1,motor}} \right| > 3dB;$$

$$\omega_c = 2\pi f_c, \quad f_r = 1/t_r$$

(5.1)
The selection of grid-side boost inductor \( L_{d\text{m1},\text{grid}} \) is done according to peak DM ripple constraint \( \Delta i_{pk,\text{dm}} \) \cite{159,160}, set to be 17 A \( [20\% \times \sqrt{2} \times 20 \text{ A} \) c.f. Table 5-2] under zero crossing. The CM ripple contribution, due to bridge interconnection, must be considered while sizing the boost inductor. In this study, \( \Delta i_{pk,\text{cm}} \) is calculated per (5.2), selected to be 4 A \( [15\% \times \sqrt{2} \times 20 \text{ A} \) c.f. Table 5-2] at bridge resonant frequency. The capacitor \( C_{d\text{m1},\text{grid}} \) is designed to meet maximum reactive power compensation \( (Q_{\text{max}} = 5\% \times P_{\text{rated}}) \) and by setting the peak DM and CM ripple through the capacitor to 10 A \( [35\% \times \sqrt{2} \times 20 \text{ A} \). The LCL resonant frequency is maintained below half the switching frequency and >10 times the fundamental frequency for stability considerations \cite{159} and is an added constraint. Typically, the selected resonant frequency is considered sufficient for wide impedance variation on the source side \cite{161}.

The inner loop CM inductor \( \{L_{cm,\text{DC}}\} \) can be designed to meet the peak bridge current limit (4 A in this case) set per (5.2) (c.f. Fig 5.3 (a)) at the bridge resonant frequency. Thereafter, the CM noise attenuation provided by inner loop components is calculated using (5.3), and is an added constraint in the design of inner loop components \( \{L_{\text{d\text{m1,motor}}} , L_{\text{d\text{m1,grid}}} , L_{cm,\text{DC}} , C_{d\text{m1,grid}} , C_{d\text{m1,motor}} \} \). Fortunately, it is possible to calculate these parameters from (5.1, 5.2, and 5.3) and LCL resonant frequency constraint.

\[
\left\{ \begin{array}{c}
\frac{i_{\text{bridge}}(s)}{v_{\text{cm,ref}}(s) - v'_{\text{cm,cm}}(s)}_{\text{r-frame}} = \frac{j C_{\text{inner}} \theta_{\text{bridge}}}{1 - C_{\text{inner}} (L_{\text{d\text{m1,grid}}} + L_{\text{d\text{m1,motor}}} + L_{cm,\text{dc}}) \theta_{\text{bridge}}^2 + j C_{\text{inner}} R_d \theta_{\text{bridge}} \theta_{\text{bridge}}^{-1} \sqrt{\frac{1}{C_{\text{inner}} \omega_{\text{inner}}}}} \\
\text{Where } C_{\text{inner}} = 3C_{d\text{m1,grid}} \parallel 3C_{d\text{m1,motor}}
\end{array} \right. \quad (5.2)
\]

\[
\text{Attn}(s)_{L\text{\text{-bridge}}} = \frac{1 + C_{\text{cm,grid}} C_{\text{inner}} C_{\text{load}} L_{\text{cm,grid}}^2 L_{\text{d\text{m1,motor}}}^2 s^8 + (1 + C_{\text{cm,grid}} C_{\text{inner}} (C_{\text{load}} + C_{p2}) L_{\text{load,grid}} L_{\text{d\text{m1,motor}}}^2 s^8)^2}{(1 + C_{\text{inner}} L_{\text{load,grid}} C_{p2} L_{\text{d\text{m1,motor}}}^2 s^8) \left(1 + C_{\text{inner}} L_{\text{load,grid}} C_{p2} L_{\text{d\text{m1,motor}}}^2 s^8\right)} \quad (5.3)
\]

Where \( L_{\text{load}} = L_{\text{d\text{m1,grid}}} + L_{\text{d\text{m1,motor}}} \)
Importantly, the fundamental frequency phase shift between inverter and rectifier output will affect the peak volt-second on the inner loop components, made up of $L_{d1,\text{grid}}$, $L_{d1,\text{motor}}$, and $L_{cm,\text{DC}}$. Based on simulation results, a 3D map of peak volt-second, modulation index (MI), and phase shift is shown in Fig 5.4, which yields a $90^\circ$ phase-shift at the highest MI of 1.0 as the worst case for peak volt-second. This condition is used for physical sizing and optimization of the inner loop magnetics.
While the inner loop passive components provide almost constant attenuation to low frequency emissions (c.f. Fig 5.3 (b)), the high frequency performance is affected due to converter and cable ground currents, i.e. the outer loop contribution is significant per Fig 5.3 (b). Therefore, these components must be designed to meet the high frequency conducted emissions standard EN-61800-3.

The required CM filter attenuation due to grid-side CM-LCL stage \( \{ C_{cm1,grid}, L_{cm1,grid}, L_{cm2,grid}\} \) can be calculated per the expression in (5.4) (c.f. Fig. 5.3(c)), wherein the inner loop components \( (C_{inner}, L_{inner}) \) are defined per (5.2). The expression in (5.4) shows higher sensitivity to \( C_{cm1,grid} \). Therefore, the CM ground capacitance is set to the highest limit \( C_{cm1,grid} = C_{cm,upper} = 2 \, \mu F \) in this study (c.f. Table 5-2), resulting in smaller volume of equally split grid-side CM inductors \( (L_{cm1,grid} = L_{cm2,grid}) \). Similarly, the additional DM attenuation at high frequency is provided by \( C_{dm2,grid} \), calculated per [160]. In summary, these closed form expressions are suitable for low and mid-frequency evaluation and rough estimation of filter parameters. Equation (5.4) can be simplified further per (5.5).

\[
\text{Attn}(s)_{CM-grid(LCL)} \approx \frac{C_{load}(C_{load} + C_{p2} + C_{load}C_{p2}(L_{cm1,dc} + L_{dm1,motor})s^2)(1 + C_{inner}L_{ncs}s^2)^2}{(L_{cm1,dc} + L_{dm1,motor})(C_{inner}^2C_{p2}^2(L_{dm1,grid} + L_{cm1,dc})s^4)} \tag{5.4}
\]

Following the parameter identification stage, the physical form factor optimization is carried out. Powder cores from MICROMETALS® are used for the inner loop magnetic component design, due to their superior core loss characteristics and lower fringing field effects (since the inner loop is exposed to a high frequency switching ripple and bridge current resonance, per (5.2)). Note that an iterative design process to account for drop-in permeability with peak H-field must be considered while selecting powder cores. On the contrary, Si-steel or iron-amorphous cores can be used for the design of outer loop grid-side DM inductors, due to absence of a high frequency ripple, thereby getting the benefit of high saturation flux density limits for these cores. Nanocrystalline toroidal cores are
preferred for CM inductors because of their high permeability per unit volume. The loss-weight map of every subcomponent is shown in Fig 5.5 under the worst-case phase angle criterion discussed earlier in Fig 5.4. The design corresponding to lowest weight is selected for demonstration, however, can be extended to low volume designs as well. Based on the available components in the market, the final form factor of the winding (round conductors) and core was selected accordingly. From the selected design points in Fig 5.5, the corresponding filter subcomponents are analyzed in high frequency using analytical formulations.

![Fig 5.5 Loss-weight map of: (a) boost inductor, L_{dm1,grid}, (b) DM filter inductor, L_{dm1,motor}, (c) grid-side DM inductor, L_{dm2,grid}, and (d) grid-side CM inductors, L_{cm1,grid}.

5.1.2 Simplified analytical formulations for wide-band filter models.

The converter, being the aggressor in the EMI model, must be represented to mimic the high frequency behavior using wide-band frequency models. The high frequency converter lumped model is derived using the proposed method, discussed in [9]. As such, this section covers the accurate modeling procedure for single layer toroidal cores, multi-layer boost inductors and three-limb cores, the three most prominent structures used in three-phase applications.

**Single layer toroidal cores:** Three-phase AC CM inductors \{L_{cm1,grid}, L_{cm2,grid}\} and DC CM inductors \{L_{cm,DC}\} in Fig 5.2 are modeled in the high frequency domain. The frequency dependent
impedance \( \hat{Z} \) is derived from Maxwell’s equations [163], in terms of complex vectors expressed as Bessel functions of first order \( J_1 \) and zero order \( J_0 \), as shown in (5.6).

\[
\hat{Z} = -\frac{4\pi}{\mu_{rc}} fL_{dc} \text{Im} \left\{ \frac{\hat{\mu}_{rc}}{j^{3/2} \sqrt{\frac{r_0^2}{\delta}}} \frac{J_1\left(j^{3/2} \sqrt{\frac{r_0^2}{\delta}}\right)}{j^{3/2} \sqrt{\frac{r_0^2}{\delta}}} J_0\left(j^{3/2} \sqrt{\frac{r_0^2}{\delta}}\right) \right\} \tag{5.6}
\]

Where \( \hat{\mu}_{rc} \) is the complex permeability, \( \delta \) is the conductor skin depth, \( r_0 \) is the radius of conductor, ‘\( L_{dc} \)’ is the DC self-inductance and ‘\( f \)’ is the frequency. A-priori knowledge of core material, dimensions, and parameter from Fig 5.5 can facilitate in complex impedance calculation per (5.6). From (5.6), the real and reactive terms \( L_{ac} \) and \( R_{ac} \) are deduced, shown in (5.7) and (5.8).

\[
L_{ac} = \text{Re}\left(\hat{Z}\right); \quad R_{ac} = \frac{\text{Im}\left(\hat{Z}\right)}{2\pi f} \tag{5.7}
\]

\[
R_{w,ac} = R_{w,dc} \left[ \frac{e^{2A} - e^{-2A} + 2\sin(2A)}{e^{2A} + e^{-2A} - 2\cos(2A)} \right] + \frac{2N_t^2 - 1}{3} \left( \frac{e^{2A} - e^{-2A} + 2\sin(2A)}{e^{2A} + e^{-2A} - 2\cos(2A)} \right) \tag{5.8}
\]

Analytical static capacitance calculations [164][165] are performed at this point. Physical dimensions, such as inter-turn, turn-core, layer-layer separation, thickness of core/winding insulation (assumed), core dimensions, etc., can be obtained from the selected design point in Fig 5.5. A basic two turn/winding cell and turn-core cell is shown in Fig 5.7, with illustration of the orthogonal electric field leading to parasitic capacitance. For instance, the static capacitance between single turn to core is expressed in (5.9) from [165]. Where, \( L_t \) is the mean length parallel to the core face and winding
section, \(D_0\) and \(D_i\) are outer and inner diameters of the wire respectively, \(\delta_{tt,\text{reg}}\) is the turn-to-turn distance in the specified region (c.f. Fig 5.7), \(\delta_{tc,\text{reg}}\) is the turn-to-core distance in the specified region, \(\delta_{\text{ins-core}}\) is the insulation thickness of core, \(\varepsilon_0\) is the permittivity of vacuum, \(\varepsilon_{\text{core}}\) is the permittivity of core insulation, and \(\phi\) is the angle made by the vector orthogonal to the conductor insulation surface in Fig 5.7. Similarly, the turn-to-core capacitance is expressed as (5.10).

\[
\begin{align*}
C_{tc,\text{reg}} &= \frac{\varepsilon_0 D_0}{2} L_t \times \\
&\left\{ \frac{\pi}{2} \int_{-\pi/2}^{\pi/2} \left( \frac{1}{\left( \frac{\delta_{tc,\text{reg}} + D_0}{2} \left( 1 - \cos \phi \right) \right)} \left( \frac{1}{\sin \phi} + \frac{\delta_{\text{ins-core}}}{\varepsilon_{\text{core}}} \right) d\phi \right\} \\
C_{tc,\text{ins}} &= \frac{\pi \varepsilon_0 \varepsilon_{\text{wire}}}{\ln(D_0/D_i)} L_t \\
C_{tt,\text{reg}} &= \frac{\varepsilon_0 D_0}{2} L_t \int_{-\pi/2}^{\pi/2} \left( \frac{\sin \phi}{\left( \frac{\delta_{tt,\text{reg}} + D_0}{2} \left( 1 - \cos \phi \right) \right)} \right) d\phi
\end{align*}
\] (5.9) (5.10)

Next, the equivalent lumped single turn capacitance is calculated in (5.11) from (5.9-5.10). Remaining constant, definitions can be found in [164][165] and are excluded from this article.

\[
C_{tc} = \sum_{x=1}^{n} C_{tc,\text{reg},x}, C_{tt} = \sum_{x=1}^{m} C_{tt,\text{reg},x} \\
C_{eq} = f(C_{tc}, C_{tt})
\] (5.11)

Lastly, the obtained frequency domain model per Fig 5.6 (a, top) is converted to the time domain lumped equivalent model shown in Fig 5.6 (a, bottom). Note that multiple RL segments in parallel are used to represent the frequency dependent effect of permeability in the time domain simulation.
The additional RL branches \( (R_1, L_1, R_2, L_2) \) can be tuned to allow a gradual transition to resistive core behavior using metaheuristic optimization techniques [166]. Consequently, the core permeability characteristics with respect to frequency must be known.

![Diagram](image)

**Fig 5.6 Proposed/revised lumped models for:** (a) three-phase CM choke (b. i) Three-phase boost inductor (b. ii) Three-limb DM inductor (c) Three-phase distributed cable model

**Multi-winding single phase boost inductors:** The lumped high frequency models for boost and three-limb DM inductors are selected based on an analogy with the multi-winding transformer models [167][168][169]. The two-port equivalent capacitor network can be used to realize a multi-layer/multi-winding scheme. First, the simplified wide-band frequency models of two layer wound boost inductors for \( L_{\text{dm1,grid}} \) and \( L_{\text{dm1,motor}} \) are shown in Fig 5.6. The inner capacitor \( C_2 \) and \( C_3 \) represents the cumulative effect of turn-to-turn \( (C_n) \) and turn-to-core capacitance \( (C_{nc}) \) of the inner layer and between the two layers respectively. Outer capacitor \( C_1 \) represents the inter-layer...
capacitance. The sequential winding pattern (for voltage gradient calculations [169]) is considered in this study.

![Diagram of winding patterns](image)

Fig 5.7 Geometric illustrations for: (a) Single-layer winding on a core (b) Turn-to-core capacitance (c) Selected winding pattern for equivalent turn-to-core capacitance (d) Turn-to-turn capacitance

According to (5.10), the turn-to-turn capacitance ($C_{tt}$) and turn-to-core capacitances ($C_{tc}$) can be calculated and the equivalent energy in the stored windings can be expressed by $W_1$ per (5.12), shown in Fig 5.6 (b, i). Where $v_p$ and $v_s$ are the static voltage drop across primary and secondary windings respectively, $N$ is the number of turns per layer, $L_3$ and $L_4$ are simply the self-inductances contributed by the two layers.

$$W_1 = \frac{1}{2} C_1 v_p^2 + \frac{1}{2} C_2 (v_p + v_s)^2$$

(5.12)

The energy in the stored windings of the distributed network can be derived as follows. For a boost inductor, three regions are defined as shown in Fig 5.8. The total capacitance is the sum of the
capacitance obtained from the three regions between any two turns, i.e. either inter-layer (between ‘p’ and ‘s’) or intra-layer (between ‘p’ and ‘p’ or ‘s’ and ‘s’).

![Diagram showing regions for capacitance](image)

Fig 5.8 (a) Three regions to obtain distributed capacitances i.e. first turn-to-core and turn-to-turn capacitances (b) Net voltage distribution for capacitance calculation in distributed network.

Therefore, the distributed capacitances for different regions can be calculated according to the expressions in (5.13) and (5.14). Here the terms $C_{tt}$ and $C_{tc}$ can be calculated analytically, as shown earlier.

\[
\begin{align*}
    i, j \neq (1, N, N + 1, 2N) & \quad \begin{cases}
        C_{pipj} = C_{tt, reg1} \parallel 2C_{tc, reg2} \\
        C_{sisj} = C_{tt, reg2} \parallel 2C_{tc, reg3} \\
        C_{pisj} = C_{tt, reg3} \parallel (C_{tc, reg2} + C_{tc, reg3})
    \end{cases} \\
    i, j = (1, N, N + 1, 2N) & \quad \begin{cases}
        C_{pipj} = C_{tt, reg1} \parallel (2C_{tc, reg2} + mC_{tc, reg1}) \\
        C_{sisj} = C_{tt, reg2} \parallel (2C_{tc, reg3} + mC_{tc, reg1}) \\
        C_{pisj} = C_{tt, reg3} \parallel (C_{tc, reg2} + C_{tc, reg3} + mC_{tc, reg1})
    \end{cases}
\]

Where ‘m’ satisfies the condition from (5.15).
Clearly, the capacitance is highly sensitive to the top and bottom most turns according to these expressions. This is verified using 3D simulation plots showing the distribution of capacitances of each turn. From Fig 5.9, it is evident that the capacitance of top and bottom layers dominates in the form of turn-to-core capacitance, while the bottom turn exhibits the highest net turn-turn capacitance. In addition, the turn-to-core capacitance is clearly a function of the material permittivity, unlike the turn-turn capacitance. In the real scenario, the presence of the bobbin makes the high frequency performance more susceptible to parasitics.

\[
m = \begin{cases} 
1, & \text{if either } i \text{ or } j = (1, N, N+1, 2N) \\
2, & \text{if both } i \text{ and } j = (1, N, N+1, 2N) 
\end{cases}
\] (5.15)

Fig 5.9 Distributed capacitance network and arrangement of a boost inductor (a) Illustration of turns (b) Distributed turn-to-core capacitance (c) Distributed turn-to-turn capacitance
The energy in the stored windings of the distributed network can be derived per Fig. 5.6 (b,i) and is given by $W_2$ per (5.16) for the selected winding pattern per Fig. 5.6(c). It includes the intra-turn (same layer) and inter-turn (adjacent layer) contributions.

\[
W_{21} = \frac{1}{2} C_{pisj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{N-i}{N-1} v_p + \frac{N-j}{N-1} v_s \right)^2 \\
W_{22} = \frac{1}{2} C_{pipj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{i-j}{N-1} v_p \right)^2 \\
W_{23} = \frac{1}{2} C_{sisj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{i-j}{N-1} v_s \right)^2 \\
W_2 = W_{21} + W_{22} + W_{23}
\]

(5.16)

By equating the two energies, the simplified lumped capacitors $C_1$ and $C_2$ can be computed and given by the expressions in (5.17).

\[
C_1 = \frac{1}{2} \left( C_{pisj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{i-j}{N-1} \right)^2 + C_{pisj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{N-i}{N-1} \right)^2 - C_2 \right) \\
C_2 = \frac{1}{2} C_{pisj} \sum_{i=1}^{N} \sum_{j=1}^{N} \left( \frac{N-i}{N-1} \frac{N-j}{N-1} \right)
\]

(5.17)

**The three-limb DM iron core**: This structure adopted for $L_{dm2,grid}$, by default, should not provide any CM impedance except for leakage inductance in series with the equivalent CM capacitance obtained from the network ($C_4$, $C_5$, and $C_6$). A single winding/layer solution is adopted in this study and the equivalent lumped model is derived in a similar manner, as shown in (5.12-5.17), using
the energy equivalence concept. The three-limb DM parasitic network per Fig 5.6 (b,ii) is obtained subsequently per the methodology in [169], which was demonstrated for flyback transformers.

Capacitor parasitic models are obtained from datasheet specifications (loss tangent) or physical impedance measurements for accurate equivalent series inductance (ESL). The terms $\text{ESL}_{\text{Cdm1/2,grid}}$, $\text{ESL}_{\text{Ccm1,grid}}$ are obtained thereafter labeled in Fig 5.2.

![Image](image_url)

Fig 5.10 Measured and analytical impedance response of filter subcomponents: (a) $L_{\text{cm1/2,grid}}$ (b) Boost inductor $L_{\text{dm1,grid}}$ (c) 15m long unshielded cable.

Long cable models are extracted using the cable modeling toolkit in ANSYS simulation environment and translated to lumped transmission line model [170] to be directly used in the time domain simulation platform in MATLAB. This model can be scaled according to cable length, by tuning sectional ($L_6$, $C_7$) parameters, and the number of distributed sections $n_{\text{sections}}$ in Fig 5.7 (c). The motor model is derived from an existent induction motor impedance characteristic using the method proposed in [171][172]. Together, the cable and motor represent the equivalent CM load impedance in
Fig 5.2. Additional information from either vendor datasheets or impedance measurements can assist in accurate modeling of the load impedance.

5.1.3 Boost inductor, ground layer and LCL structure impact studies

The impact and sensitivity of parasitics will be studied in this section. Per the design of the boost inductor described in Section 5.1.2, the impact of anti-resonance is seen as shown below, using three single phase boost inductors and converter (rectifier) for demonstration, per Fig 5.11.

![Three-phase grid-tied rectifier test bed.](image)

![Fig 5.12 (a) Equivalent terminal model (b) Transfer gain (c) Correlation between measurement and simulation (using estimated capacitances)](image)
The corresponding lumped equivalent circuit is developed as shown in Fig 5.12(a). Here $V_{cm}$ is calculated from the measured phase to DC bus mid-point voltages during the experiment. Load and LISN parameters are known from Table 5-1. The lumped parasitic capacitors are obtained from the methods described earlier. Then the CM current transfer gain is calculated as a function of the terminal capacitors and load impedance, shown in Fig 5.12(b). The circuit is also simulated in the time domain to produce the CMV spectrum across LISN resistor $R_{lisn}$. A key observation is the mid-frequency resonant component $f_{res2}$. This anti-resonance effect is seen in the EMI spectrum as a peak around the same frequency. It is therefore critical to ensure that $f_{res,2}$ is controlled in such a way that it appears beyond the 30 MHz range. The proposed model can accurately capture this anti-resonant effect. Therefore, the boost inductor anti-resonant effect must be eliminated, which will be shown later.

Fig 5.13 (a) Layout of baseline grid-side BtB filter structure (indicating overlap of power traces and ground plane) (b) Equivalent representation in schematic ($C_{PCB}$-denotes coupling via ground plane and $C_{coupling}$- Coupling in air)

Secondly, the ground layer on the filter PCB provides a feed-forward effect. As an example, consider the filter PCB constructed as shown in Fig 5.13, where a ground plane on the top and bottom layers is added for grid-side component (LCL-$L_{cm1,grid} / L_{cm2,grid}$ and $C_{cm1,grid}$).
As a result of the layout, the lumped model and the corresponding impact is shown in Fig 5.14. The component $C_{PCB}$ is used to denote the coupling capacitance between the high-power traces between $M_{cm1}$ and $M_{cm2}$, and the ground plane as shown in the layout per Fig 5.13. A close correspondence between the simulated and measured spectrum (around the mid-frequency band from 1–10 MHz) can be seen in Fig 5.14, where the noise content increases at 5 MHz due to the interaction between ground plane on the PCB and the traces. The anti-resonance effect is also seen here. The extracted parasitics were obtained from ANSYS Q3D simulation results. Therefore, it is recommended to eliminate the ground plane underneath the power traces to avoid capacitive coupling effects.

The third factor is the grid-side CM LCL structure comprising of CM inductors $L_{cm1/2,grid}$ and star-capacitor network $C_{cm1,grid}$. These components exhibit significant coupling effects, particularly T-type coupling and LC coupling, and are critical for high frequency attenuation. Therefore, optimal layout scheme for the T-network is studied.

![Fig 5.14 Simulated / Measured CM noise with rectifier and grid-side BtB filter stage (with coupled parasitic capacitances included)](image-url)
Typically, the self-parasitics of the choke (EPC) and capacitor (ESL), along with mutual inductive coupling between two capacitors, two inductors, and one component of each of them could affect the high frequency noise content. Several test cases using a network analyzer setup per Fig 5.15 (a, b) were conducted, and the impact study is shown below. First, the impact of LC coupling is studied. The placement configuration per 2/3 provides the best results.

Fig 5.16 Comparative study of voltage gains of various configurations
Next, the T-network was evaluated per Fig 5.17, and the corresponding results reveal that the coupling along the ‘z’-axis, i.e. the left most case in Fig 5.17(b), is preferred for the selected CMC evident from results in Fig 5.18 (with form factor such that the depth of the core is greater than the width).

![Fig 5.17](image1.png)

**Fig 5.17** (a) Test schematic for T-type coupling (b) Different orientations under study (c) Setup with capacitive shielding

![Fig 5.18](image2.png)

**Fig 5.18** Impact of orientations on voltage gain

While such placement configurations were analyzed for single phase and DC-DC converter applications in [173][174], no such work has been reported in three-phase systems. These sensitivity studies and identified critical nodes will be considered eventually to revise the present design for the
next version. Due to limited scope, only the boost inductor impact will be analyzed further in the following sections.

5.2 Characterization of a BTB Filter Structure

5.2.1 Functional tests and performance verification

The grid- and inverter-side filters are constructed and assembled with 15 kW rated 3L-NPC converter units arranged in a BtB fashion, shown in Fig 5.19(a,b,c). The cable and load bank are added externally per Fig 5.19(d), while a benchtop oscilloscope is used to measure the LISN phase voltages and post-processed to compute the DM and CM frequency spectrum. The start-up transient using v/f control on the inverter side and active front end control on rectifier side is demonstrated in Fig 5.20, wherein the CM current inrush across the bridge interconnection is minimal, due to the DC-CM chokes added between the two units. The steady-state plot shows the 6 kHz inner loop resonant component in the bridge current. From the time domain plots and frequency domain spectra in Fig 5.20(c), the bridge current component in the time domain and frequency domain is verified with the analysis presented earlier. The bridge resonant frequency component of approximately 6 kHz is seen in the inner loop.
Fig 5.19 (a) Grid- and inverter-side filter blocks ($C_{dm1,grid}$, $C_{cm2,grid}$ placed on top side) (b) 15 kW BtB prototype with bridge connection (c) DC CM choke arranged between two units (d) Experimental setup (15 m long unshielded cable used as an example)

Fig 5.20 BtB operation with the proposed bridge configuration: (a) Start-up, (b) Steady-state operation (c) Bridge current in time domain and frequency spectrum.
The filter CM transfer gain plots in Fig 5.21 (a) show the measured and simulated filter voltage gains, which follow almost the same trend, except for DM filter response at high frequency. A discrepancy in anti-resonance effect in simulated and measured DM voltage gain can be seen.

![Fig 5.21 (a) Measured and simulated voltage gains](image)

![Fig 5.21 (b) Measured DM and CM noise voltage spectrum at the LISN terminal](image)

From the measured DM and CMV spectrum in Fig 5.21(b), the EMI limits are met based on operating conditions from Table 5-2. The impact of the bridge interconnection on peak bearing voltage can be seen in time and frequency domain in Fig 5.22 (a, b). As discussed earlier, the attenuation is improved under ungrounded converter configuration due to the absence of parasitic path to ground via the two converters. This is evinced from Fig 5.22 (c), where an overall improvement in spectra is seen. The attenuation to bridge current components is expected to be approximately 20 dB in the mid-frequency range as seen from Equation (5.3). The measured attenuation is smaller and reduces with high frequency due to parasitic effects of cable and grid-side CM capacitor $C_{cm1,grid}$. 
Fig 5.22 (a) Bearing voltage without bridge (b) With bridge connection (c) Impact of bridge connection on CM noise voltage at LISN terminal.

Fig 5.23 (a) Motor terminal line-to-line overvoltage due to long cable effect (b) DM-LC filter impact on the line-to-line voltage
The DM filtering performance on the inverter side is evinced from the sine filter response of $L_{dm1,motor}$ and $C_{dm1,motor}$ in Fig 5.23, which shows the mitigation of motor side over-voltage seen from the long cable effect. The high frequency ripple across $L_{dm1,motor}$ is verified to be contributed by harmonics at $f_{sw}$ and $2f_{sw}$.

5.2.2 Proposed layout for reduced impact of high frequency effects

While the proposed BtB filter structure can meet the EMI compliance, the filter parasitic influence (shown earlier in Section 5.1) on the spectrum must be desensitized. This section focuses on eliminating the anti-resonance effect of the boost inductor seen earlier from experimental results in Fig 5.12. Two winding techniques are proposed:

a) **Single layer edge-wound coils** and b) **Multi-layer Zig-Zag pattern**

The illustration of these techniques is shown in Fig 5.24 (b, c). Due to the presence of a single layer edge winding scheme, the equivalent lumped network is a reduced order (second order) network, yielding only a single resonant point unlike the baseline sequential winding pattern (used in Fig 5.12), shown in Fig 5.24 (a). If a multi-turn solution is to be used, the zig-zag pattern is proposed where the layer-to-layer capacitance is reduced drastically due to staggered voltage distribution between adjacent turns, unlike the sequential multi-winding pattern for the baseline boost inductor. The impact is shown in Fig 5.25 using the PEMAG tool, a 3D modeling tool for designing inductors. The impedance plots are obtained using the network data explorer toolbox in ANSYS. A good agreement between measured and simulated impedance plots can be noted. In addition, the anti-resonant frequency is absent from the impedance characteristics.
The proposed inductors in Fig 5.24(b) were tested in a three-phase rectifier test-bed under the same conditions and the test setup as in Fig 5.12. The measured spectrum for these cases is compared in Fig 5.26. The edge-wound solution outperforms the zig-zag/’zz’-wound solution because of higher spectral peaks around 30 MHz, with the latter evident from Fig 5.26 (b).
Additional improvements over the existent design were proposed earlier in section (5.1) as part of future research and are therefore excluded from this dissertation.

5.3 Summary and conclusion

This chapter has presented a complete design consideration and analysis for a BtB filter structure for minimal high-frequency effects. A systematic procedure to design filters with high frequency effects in mind is developed that can be used to decide if the impact of parasitics generated by the filter are within acceptable limits. This is achieved using distributed passive component modeling through static capacitance calculations and translation into lumped models. Critical components that produced prominent changes in the high frequency noise spectrum are identified, i.e. boost inductor, ground plane, mutual coupling between CM chokes and capacitors, and effective stray inductance through the Y-capacitor to ground.
Subsequently, methods to compensate/control peak noise harmonics at high frequency are proposed. The following suggestions are recommended:

1) Use of a single layer edge-wound or ‘zig-zag’ wound ‘multi-layer’ boost inductor to solve anti-resonance phenomenon.

2) Use of three-limb DM core instead of single phase inductors. Adding low leakage inductance for first stage \( L_{dm1,grid} \) can mitigate the anti-resonance issue.

3) Magnetic shielding of boost inductor from grid-side CM-LCL filter stage is crucial.

4) Star-network for grid-side CM LCL stage for minimized coupling. Two CMCs to be aligned along the ‘zz-axis.’ This provides the lowest mutual inductive coupling. Capacitive shielding between two CM stages shows significant improvement.

5) Single layer nanocrystalline chokes for grid-side LCL network are preferred with split-wound winding technique to reduce magnetic coupling along ‘zz-axis.’ Particularly useful when cores with larger core depth compared to core width is used.

6) Elimination of ground plane underneath traces to avoid feed-forward coupling effects.

7) Low ground impedance from Y-capacitor to the system ground plane underneath using zig-zag capacitor placement and edge plating technique.
Chapter 6. Conclusion

Modularity in filters is deemed necessary to avoid redesign and retain attenuation to targeted groups of harmonics. In this regard, alternate FBB architectures for interleaved/parallel converters are proposed and a systematic comparison between magnetically interconnected (M-FBB), electrically interconnected (SL-FBB), localized (local trap FBB) and non-interconnected baseline FBB is made. This is facilitated by introducing the per-inverter, per-phase models for parallel and interleaved converters, which allows for breakdown into four equivalent circuits; consequently, a quantitative comparison of attenuation can be made. The electrical interconnection, i.e. using indirectly coupled CI and inserted boost inductor, is recommended as a prospective modular FBB for grid-tied power conversion systems. Additionally, design considerations for two stage LCLC filter are presented to maintain attenuation with any number of parallel modules. Primarily, the impact of asymmetry between channels was found to saturate the inner loop and outer loop CM inductors, which affects the EMI filtering performance. CM inductors with low permeance and low drop in permeability with DC bias are recommended. The proposed FBB topologies are optimized for high power density, functionally tested and verified.

For DC-fed motor drive systems, modularity is ensured using a masked impedance approach wherein a single turn AC filter with optimized RC damper is proposed at the inverter output terminal. The impedance of an AC filter is selected to mask any motor impedance that could be used. The AC filter mitigates peak bearing current at the motor terminal and introduces additional attenuation for the DC-side CM noise. To further enhance the bandwidth of the filter, a staggered PWM scheme is introduced to suppress peak bearing currents arising from closely spaced switching events without significantly affecting other operating features such as THD, DM noise, etc. An integrated DM+CM core and multi-turn heavy copper PCB-based solution is proposed for DC-side DM-CM filtering. A
decoupling board feature is combined with the gate driver to localize the high frequency commutation at the module terminal and push the mixed frequency resonance at high frequency beyond the 30 MHz limit line. In addition, a highly compact and novel mechanical assembly using edge plating for a DC bus bar and filter is proposed to provide 360° termination and low impedance pass for ground currents. To handle the low partial discharge inception voltage (PDIV) levels resulting from high altitude operation, shielding techniques are proposed that can localize the peak E-field within the PCB dielectric. A high active specific power of 20 kW/kg is realized using the T-type inverter and the proposed filter structure.

A negative consequence of high-density packaging and integration is the influence of the filter itself and mutual parasitics on the high frequency spectrum. To account for these effects, systematic lumped models are derived for CM and DM inductors. For instance, the impact of non-linear permeability with CM inductors is captured using parallel RLC networks. The anti-resonance effect and frequency response of multi-layered boost inductor and three-limb DM cores is captured using three and six port models, respectively. Consequently, edge-wound single layered winding and zig-zag multi-layered windings are recommended to avoid the anti-resonant effect. The impact of a grid-side LCL filter is desensitized using the proposed star layout network. A bridge topology for a BtB converter is adopted as the test case for analysis and characterization. Finally, a set of design guidelines for the BtB network are formulated.

In general, design guidelines for specific FBB topology (grid-tied converter, DC-fed motor drive, BtB bridge interconnection) and form factor optimization routines in conjunction with analytical estimation of parasitics are developed to facilitate the realization of modular FBBs.
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