Electro-Thermal Device-Package Co-Design for a High-Temperature Ultra-Wide-Bandgap Gallium Oxide Power Module

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Power electronic systems and components that can operate in environments with ambient temperatures exceeding 250 °C are needed for innovation in automotive, aerospace, and down-hole applications. With the imminent mass electrification of transportation and industry, the high-temperature electronics market value is anticipated to grow to $15 billion by the end of 2023. Conventionally, silicon (Si)-based converters are used in these applications; however, as operating temperatures continue to increase, the inherent limits of these systems are being met. The primary limitations for the high-temperature operation of semiconductor devices is the intrinsic carrier concentration, dictated primarily by the bandgap of the material, which increases with temperature. Wide-bandgap (WBG) power semiconductors, primarily silicon carbide (SiC) and gallium nitride (GaN), have been adopted for use in these applications, but exhibit a degradation in performance at elevated temperatures. As such, gallium oxide (Ga$_2$O$_3$), an ultrawide-bandgap (UWBG) material with controllable doping and the potential for inexpensive substrates, has presented itself as a potential contender for use in high-temperature power electronics applications.

The UWBG of Ga$_2$O$_3$, 4.8 eV compared to 1.1 eV for Si, 3.2 eV for SiC, and 3.4 eV for GaN, allows it to achieve nearly $10^{33}$ lower intrinsic carrier concentration than Si, permitting Ga$_2$O$_3$ power devices to theoretically operate at significantly higher temperatures. In addition, unipolar Ga$_2$O$_3$ devices have a better theoretical limit with respect to the relationship between on-resistance and breakdown voltage, which could enable higher power density and power conversion efficiency. While Ga$_2$O$_3$ exhibits potential in these regards, its low thermal conductivity (11–27.0 W/m·K compared to 148 W/m·K for Si, 350 W/m·K for SiC, and 130 W/m·K) means that standard packaging and cooling techniques are not suitable or effective. Furthermore, conventional polymeric and organic encapsulant materials are typically limited to operating temperatures of 200 °C and novel materials must be evaluated.

This work outlines and evaluates an electro-thermal device-package co-design modeling platform that can be utilized for the efficient and accurate modeling of Ga$_2$O$_3$ devices and their associated packaging, with the goal of overcoming the challenges of the low thermal conductivity of Ga$_2$O$_3$. This permits for the electrical and thermal performance of the devices and the package to be designed in tandem for an effective design. Next, six high-temperature encapsulation materials are evaluated and conclusions are drawn about each material’s feasibility for use as a dielectric encapsulation material for a power module operating at temperatures exceeding 250 °C. This simulation platform and material analysis was then used to design and fabricate a 300 °C, 1.2 kV half-bridge power module utilizing Ga$_2$O$_3$ diodes to assess thermal and electrical performance.
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GENERAL AUDIENCE ABSTRACT

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Chapter 1. Introduction

1.1 Motivation, Application, and Background

With the world’s electricity generation expected to exceed 45 trillion kilowatt-hours (kWh) by 2050, due in part to the elimination of fossil fuel use in transportation and industry [1], the need for efficient, flexible, and reliable power electronics for power conversion and delivery has never been higher. As power density demand increases there is particular interest in power electronic systems and components that can operate at temperatures exceeding 250 °C [2] [3]. However, the junction temperature ($T_j$) of commercial power devices and modules are typically limited to below 175 °C [4] and as such require complex and large cooling systems to maintain safe operating temperatures, lowering reliability and detracting from the power density of the system.

Aerospace is one industry that can reap great benefits from high-temperature power electronics. In recent years, there have been numerous initiatives and programs to replace complex, weighty mechanical systems, striving for an increase in efficiency and power density [5]. In order to increase the amount of electrical distribution and actuation while maintaining meaningful efficiency, these systems need to be physically near the loads that they serve. As such, systems placed near engines may experience ambient temperatures in excess of 225 °C [6]. While rigorous cooling could be implemented in order to reduce temperatures to the safe operating range of existing power electronics systems, this would counteract the benefits, adding complexity, weight, and reducing overall power density.

Similar to aerospace, both commercial and passenger vehicles have high-temperature electronics that can be used in mechatronic systems aiming to replace conventional mechanical and hydraulic systems [7]. In transportation applications, high power density is a critical design
target for the power electronics because the volume and weight of the systems onboard have a
great impact on the transport capability and fuel economy of the vehicles. A way toward higher
power density is through operating power semiconductor devices at higher temperatures, which
require smaller and lighter cooling systems, thus reducing a major weight contributor in power
converters [8]. To go a step further, the rapid electrification of the automotive industry will pose
new strains as high-energy density converters, traction controls, and charging infrastructure will
also drive the high-temperature operation needs of all onboard electronics to increase.

Lastly, while oil and gas drilling are predicted to decline with an increased share of
renewables in the energy generation mix [1], it should be noted that these down-hole applications
are subject to high ambient temperatures exceeding 225 °C. That, in tandem with an expected
system lifetime of 5 years, places a lot of stress on the system, showing a blatant desire for
reliable high-temperature power electronics [9].

In these applications, 900–1200 V power modules are typically needed for traction and
power conversion [10] [11]. However, these needs are challenging the fundamental limit of
conventional silicon (Si)-based converters. The fundamental limit for the high-temperature
operation of semiconductors is the concentration of intrinsic carriers \( n_i \), which increases as a
function of temperature per:

\[
n_i = N_s \exp \left( \frac{-E_g}{2k_BT} \right)
\]  

(1)

Where \( N_s \) is the available states per unit volume, \( E_g \) is the bandgap of the material, \( k_B \) is the
Boltzmann constant, and \( T \) is the steady-state temperature. For semiconductor switch and voltage
blocking operation, this value cannot exceed \( 5 \times 10^{12} \text{ cm}^{-3} \). It can be observed in Equation 1
that as the bandgap of a given material increases, it can help maintain a lower intrinsic carrier
concentration at elevated temperatures.
Wide-bandgap (WBG) materials, particularly silicon carbide (SiC) and gallium nitride (GaN), have been introduced as promising alternatives to Si, but have shown significant degradation in performance when exposed to temperatures of 250 °C and above [12]. In the last several years, an ultrawide-bandgap (UWBG) semiconductor, gallium oxide (Ga₂O₃), has emerged as a viable candidate for high-temperature power electronics. Its capabilities are beyond those of existing technologies, due to its large bandgap, controllable doping, and the availability of large diameter, relatively inexpensive substrates [13].

1.2 Ga₂O₃ as a Power Semiconductor

As can be seen in Figure 1, the UWBG of Ga₂O₃ has 4.8 eV, and compared to 1.1 eV for Si, 3.2 eV for SiC, and 3.4 eV for GaN, this value allows it to achieve nearly 10⁻³³ lower intrinsic carrier concentration than Si, permitting Ga₂O₃ devices to theoretically operate at significantly higher temperatures, making it suitable for high-temperature operation.

![Figure 1. Intrinsic carrier concentration of selected semiconductor materials and their related high-temperature operating limits [14]](image-url)
In addition, when compared to Si, SiC and GaN devices, unipolar Ga$_2$O$_3$ devices also have a superior theoretical limit for the trade-off between on-resistance ($R_{on}$) and breakdown voltage (Figure 2) for a given device area, enabling a higher power conversion efficiency and power density.

![Graph](image)

**Figure 2. Specific on-resistance versus breakdown voltage at room temperature [13]**

Despite maintaining relatively low $R_{on}$, conduction and switching losses are still experienced during operation and are dissipated as heat. In general, it is preferred to minimize this temperature rise, as it could degrade device performance, as well as the reliability of both the device and the package. This poses a significant challenge for WBG and UWBG power devices as the combination of smaller desirable device sizes, an increase in potential current density, and a higher electric field can cause large heat fluxes within these devices, which could potentially lead to hot-spots within the device and in turn, local thermal runaway [15]. The thermal management of Ga$_2$O$_3$ power devices is especially difficult due to its low thermal conductivity of 11–27 $\frac{W}{mK}$ [16]. The thermal conductivity of commonly investigated WBG and UWBG materials are compared in Table I below.
Table I. Thermal conductivity of selected semiconductor materials [17]

<table>
<thead>
<tr>
<th>Material</th>
<th>Thermal conductivity (W m⁻¹ K⁻¹)</th>
<th>Material</th>
<th>Thermal conductivity (W m⁻¹ K⁻¹)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>150</td>
<td>SiC</td>
<td>400</td>
</tr>
<tr>
<td>GaN</td>
<td>200</td>
<td>Diamond</td>
<td>2200</td>
</tr>
<tr>
<td>[100] Ga₂O₃</td>
<td>11</td>
<td>[010] Ga₂O₃</td>
<td>27</td>
</tr>
<tr>
<td>AlₓGa₁₋ₓN</td>
<td>~10</td>
<td>AlN</td>
<td>319</td>
</tr>
</tbody>
</table>

Failing to implement proper thermal management and heat removal can severely limit the potential electrical performance of WBG and UWBG devices. If not addressed, derating of devices or an increase in device area (therefore decreasing power density) may be necessary to maintain an acceptable $T_j$ [18]. This work will explore the challenges associated with the packaging of Ga₂O₃ power devices and strategies for extracting the theoretically superior high-temperature performance of this UWBG material.

1.3 Packaging Challenges

As it stands, there are two primary hurdles for the packaging of Ga₂O₃ power devices for high-temperature applications. First is the thermal management of the devices, and the second is creating a high-temperature stable and reliable packaging configuration. Figure 3 (a) depicts a typical package for a power device, in which the primary heat flow path is through the bulk substrate of the device where the bottom contact is affixed to a high thermal conductivity substrate, and then in turn to a convective-based cooling solution.

A good figure of merit for the effectiveness of available cooling to a packaged device is the thermal resistance ($R_{th}$) observed between the junction of the device, where the majority of heat is generated during operation, and the environment, also referred to as the junction-to-ambient thermal resistance ($R_{th-j-a}$) [19] [20]. The calculation of this thermal resistance network
can be quite complex, depending on the $R_{th}$ of each material in the stack up, their interfaces, as well as the dimensions of the heat generated and the available heat spreading area [21]. As a simplification, an equivalent thermal resistance network can be built analogous to an electrical circuit [22], as seen in Figure 3 (b).

![Figure 3](image)

**Figure 3.** (a) Typical packaging configuration for a bottom-side cooled power device and (b) equivalent thermal resistance network

If we treat temperature as a voltage source, the device losses (which are a combination of switching and conduction losses) as a current source, and the $R_{th}$ of each material as a network of resistances, we can derive an expression for the junction temperature of our device in a given cooling configuration as [23]:

$$T_j = R_{th} \times P_{loss} + T_{ambient}$$  \hspace{1cm} (2)

With the high contribution of the Ga$_2$O$_3$ device (due to its low thermal conductivity) to the overall $R_{th-j-a}$ of this bottom-side cooled configuration, it is self-evident that without improved packaging and cooling solutions, a Ga$_2$O$_3$ device will have higher $T_j$ (70 °C more in an example from [17]) when dissipating the same power density as another WBG device. This could cause
the Ga$_2$O$_3$ device to exceed its safe operating temperature, which is limited by either the gate
dielectric or the packaging materials of the device.

The primary limitation for reliable high-temperature operation of a power module
package is the encapsulation. Encapsulation materials must play several critical roles to achieve
successful operation and reliability of power electronics modules. They provide protections
against electrical breakdown, chemical erosion, moisture absorption, hazardous radiation, as well
as relief of mechanical stresses and shock [21]. Though WBG and UWBG devices theoretically
have a much higher high-temperature operating limit, conventional packages use polymeric
encapsulation materials, which are typically restricted to an operating temperature of 175 °C
(based on the use of Si semiconductor devices) [24]. Commonly used acrylic, polyurethane,
epoxy, and silicone encapsulation materials are limited by their glass transition temperature ($T_g$)
and thermal decomposition [25] [26] with significant mechanical deformation at higher
temperatures, drastically reducing their insulation performance [27] [28].

1.4 Strategy and Objectives

There is reasonable concern that the self-heating associated with the low thermal
conductivity of Ga$_2$O$_3$ may compromise its performance and in turn, its commercial viability. An
integrated device-package co-design framework is necessary to develop an optimal solution that
will enable Ga$_2$O$_3$ to achieve superior performance to GaN and SiC. Co-design will enable
informed device and package designs that together will yield a configuration suitable for high-
temperature, medium/high voltage operation. In [29], an electro-thermal model was developed to
predict the characteristics of Ga$_2$O$_3$ field-effect transistors(FETs). The electro-thermal model
employed a technology computer-aided design (TCAD) device model and electro-thermal
HSPICE model to simulate the Ga$_2$O$_3$ FETs performance in a boost converter. It was found that
the converter efficiency with the Ga$_2$O$_3$ FETs was more than 10% lower than for GaN or SiC FETs. This was attributed to the significant self-heating caused by the poor thermal conductivity of Ga$_2$O$_3$. Even with expensive, high-thermal-conductivity bulk substrates, such as diamond and sapphire, the simulated converter efficiency with the Ga$_2$O$_3$ device was still more than 4% lower than for GaN or SiC. It was therefore concluded in [29] that the low thermal conductivity of Ga$_2$O$_3$ would hinder its commercial adoption. However, this work did not consider the influence of the package and cooling strategy on the performance of the Ga$_2$O$_3$. In [30], various package materials and cooling strategies were evaluated to design a package for theoretical Ga$_2$O$_3$ devices. Contrary to [29], in [30] no device model was used, and so the electrical characteristics were not considered. Instead, thermal and thermo-mechanical finite element analysis (FEA) simulations were performed using a solid Ga$_2$O$_3$ block in place of the device. It was concluded in [30] that novel packaging structures and advanced cooling strategies, such as double-sided cooling, can improve Ga$_2$O$_3$ device performance. In this work, an electro-thermal device-package co-design framework was designed and evaluated. The design framework is oriented toward enabling the Ga$_2$O$_3$ power module to operate at elevated temperatures in a power converter while tracking the electrical, thermal, and thermo-mechanical concerns that may arise with high-temperature operation. Through this framework, various device parameters, material combinations, package architectures and layouts, and heat dissipation strategies were explored for their effectiveness in offering optimal electrical and thermal performance for a Ga$_2$O$_3$ power module.

Once a platform is built for the accurate and efficient modeling of Ga$_2$O$_3$ power devices and their associated packaging, the issue of the high-temperature capabilities of the package must be addressed. To date, the majority of high-temperature power modules proposed in the literature
are limited to 250 °C and are bottom-side cooled [31] [32] [33]. The constraints imposed by traditional packages will not permit the full high-temperature, high-speed, high-voltage benefits of Ga₂O₃ power devices to come to fruition. These can be achieved by utilizing new encapsulation materials, heat dissipation strategies, and 3D interconnect technologies. A survey of high-temperature-capable die attaches, substrate, and interconnect materials and methods was performed, and their effectiveness for use in this Ga₂O₃ power module was assessed.

As it is considered to be the most immediate limitation for the reliable operation of high-temperature power electronics packaging [34], particular care was taken in the selection and experimental validation of novel encapsulation materials. In this work, six materials were identified and evaluated as candidates for use as encapsulants for operation and high-voltage insulation at and above 250 °C. Gas pycnometry was utilized to evaluate the voiding concentration of each material, as these pockets of entrapped gas can create areas of lower dielectric strength, both directly after processing and after exposure to elevated temperature. Each material was also processed onto a commonly used metal-ceramic substrate to evaluate compatibility and processability for use in a power module. Lastly, the insulation capability of each material was evaluated by testing the partial discharge inception voltage (PDIV) and electrical breakdown strength across a 1 mm gap etched in the substrate. The high-temperature storage life of the dielectric stability was then tested by soaking the materials in air heated to 250 °C for various intervals and observing the degradation of their PDIVs, electrical breakdown strengths and qualitative mechanical stability.

Leveraging the learnings from the simulation, literature survey, and material evaluation, a half-bridge power module containing Ga₂O₃ diodes targeting operation at 300 °C, 1.2 kV
blocking capability, and nanosecond-range switching was designed, fabricated, and tested against state-of-the-art SiC-based devices.

1.5 Thesis Organization

Chapter 2 of this thesis describes the current status of Ga$_2$O$_3$ devices in order to highlight the current benefits and limitations that are in place at the device level. Furthermore, it contains a survey of high-temperature packaging materials, configurations, and cooling strategies presented in literature and industry examples that may help to unlock the full potential of Ga$_2$O$_3$ devices. Chapter 3 contains an extensive survey, as well as the experimental evaluation of several potential high-temperature encapsulation materials. Chapter 4 details the development and potential uses for an electro-thermal device/package co-design platform. Chapters 5 and 6 detail the iterative design, modeling, fabrication plan, and testing plan of the Ga$_2$O$_3$ half-bridge module. Lastly, Chapter 7 lists key conclusions and ideas for future work and innovation on high-temperature Ga$_2$O$_3$ packaging.
Chapter 2. Review of Current Technologies

2.1 Ga₂O₃ as a Power Semiconductor

Though first synthesized in the 1950s [35], economical and effective growth methods were not demonstrated until the late 1990s and early 2000s [36] [37] [38]. β-Ga₂O₃ has proven to be of particular interest, as it is the most stable of the known polymorphs of Ga₂O₃ [39]. In addition, the development of consistent large area and high-volume-scalable edge fed growth (EFG) methods of Sn- and Fe-doped 2 inch and 4 inch β-Ga₂O₃ substrates has contributed to increased research efforts and a general belief of eventual commercial viability [40].

![Diagram of EFG process and resulting β-Ga₂O₃ bulk crystal]

Figure 4. (a) EFG process described in [39] (b) Resulting β-Ga₂O₃ bulk crystal

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With the contemporary development of commercially available substrates, there has been an uptick in interest in the use of Ga₂O₃ for power electronics applications [41] [42]. In order to establish its viability as a power semiconductor against existing technologies, several figures of merit and material properties are summarized in Table II below.
As can be seen, Ga$_2$O$_3$-based devices can theoretically outperform other WBG semiconductor materials on the merits of high-frequency, high-voltage, and manufacturability. As an immature technology, there are several difficulties in device fabrication and optimization that fall outside the scope of this work (i.e., defect density of wafers and a lack of native p-type) [16]; however, thermal management remains the primary discernible hurdle for the adoption of Ga$_2$O$_3$ power semiconductors [45] [46]. Consequently, many efforts have been focused on device-level techniques for either reducing the specific thermal resistance or improving the heat extraction from large-area Ga$_2$O$_3$ power devices.

Heterogeneous integration of Ga$_2$O$_3$ epitaxy and thin films on to higher thermal conductivity substrates such as SiC [47] and diamond [48] have both been demonstrated as an effective method for reducing the impact of self-heating. Ga$_2$O$_3$ on SiC Schottky barrier diodes (SBDs) fabricated in [49] showed a 75% reduction in thermal resistance when compared to devices fabricated on native Ga$_2$O$_3$. As this is a relatively mature strategy, used commercially for Si-on-insulator (SOI) [50] and GaN-on-Si [51] semiconductors, significant efforts have been made to investigate this avenue for the reduction of the specific thermal resistance of Ga$_2$O$_3$ power devices.
Currently, commercially available Ga$_2$O$_3$ substrates range in thickness between 500 µm to 700 µm [52]. Device substrate thinning through chemical-mechanical planarization is another proven method of reducing the specific thermal resistance of the die. In [53], reducing the substrate thickness of a SOI GaN high-electron-mobility transistor (HEMT) power device from 500 µm to 100 µm yielded a 35% reduction in self-heating thermal resistance. This has also been demonstrated for β-Ga$_2$O$_3$ SBDs, showing a reduction of 34% in the specific thermal resistance as the substrate was thinned to 200 µm [54]. These tactics will be critical to maintain safe operating temperatures for the gate dielectric and package as high-temperature applications are targeted. While device-level thermal management strategies may help to alleviate the impacts of device self-heating imposed by the low thermal conductivity of Ga$_2$O$_3$, they increase device complexity and manufacturing costs. As such, both device-and packaging-level cooling strategies should be employed in tandem.

### 2.2 Improved cooling strategies

With trends in power electronics moving toward higher power density, much can be learned from the improved cooling methodologies being employed both in academia and industry examples. The dimensions, arrangement, and thermal conductivities of each material within the package can affect the overall device-to-case thermal resistance ($R_{th.j-c}$) and in turn, the dimension of the package and its interface to the external cooling structure (i.e., heat sink, cold plate, etc.) dictates the remaining contribution to $R_{th.j-a}$. Figure 4 below depicts three of the most common types of packaging/cooling strategies utilized for power module applications.
While these power module configurations have differing interconnect strategies, they share some key components. Each involves the bonding of the power semiconductor die(s) to a substrate, which is in turn attached to some secondary cooling structure (pictured in Figure 4 as a heat sink). Each module is also encapsulated to protect the module as well as serving as critical electric field management.

When confronted with the task of extracting heat generated at the junction of a Ga$_2$O$_3$ power device, it is important to understand and minimize the effect that its low thermal conductivity contributes to the overall $R_{th,j-c}$. Ignoring any effects that thermal coupling may contribute (i.e. in a multi-chip power module), an analysis of a BSC configuration is conducted in [17]. This study indicated that for a high thermal conductivity device ($> 400 \frac{W}{mK}$, e.g. SiC or
diamond) the $R_{th,j-a}$ is primarily determined by the package. For a device with moderate thermal conductivity ($400 \frac{W}{mK} > k > 150 \frac{W}{mK}$ e.g. GaN or Si) the $R_{th,j-a}$ shows a strong dependence on the available cooling provided by the heat transfer coefficient (HTC) at the secondary cooling element (e.g., heat sink or cold plate). Lastly, for a device with a low thermal conductivity ($< 150 \frac{W}{mK}$ e.g. Ga$_2$O$_3$), the overall $R_{th,j-a}$ is primarily dictated by the specific thermal resistance of that device. This indicates that while BSC configurations may be appropriate for the heat removal of semiconductor devices with higher thermal conductivities, their effectiveness steeply declines for devices with lower thermal conductivities [55] [56].

Junction-side cooling (JSC)—sometimes referred to as top-side cooling (TSC)—and pictured in Figure 5 (b), no longer requires the primary heat flow path to be through the bulk substrate of the die. Instead the junction of the device (where the majority of the heat is generated during operation) is directly fixed to the substrate, allowing for a significant reduction in the overall $R_{th,j-c}$ of the package [57]. While this strategy allows for greater heat extraction and power density when compared to BSC [58], the thermo-mechanical stresses observed due to a mismatch of the coefficient of thermal expansions (CTE) of the device and substrate can reduce overall reliability of the die attach and the device [59]. Moreover, depending on the operating voltage and edge termination style of the device, the small distance between the electrically active areas of the device and the metal substrate can lead to difficulties in controlling the electric-field distribution, which may in turn lead to device derating and poor reliability [60] [61].

Lastly, double-side cooled (DSC) packaging, pictured in Figure 5(c), makes use of heat extraction through both junction- and bottom-side paths and has been proven to be an effective way to further reduce the overall $R_{th,j-c}$ of the package [62]. However, this strategy suffers from
the same weaknesses described for JSC packages in addition to increased complexity, which makes this configuration further inclined to yield and reliability issues. It should also be noted that the results from the packaged SBD presented in [19] suggest that due to the low thermal conductivity of Ga$_2$O$_3$-on-Ga$_2$O devices, a minimal benefit is seen over JSC configurations.

With the lower $R_{th,j-c}$ offered by both JSC and DSC packaging configurations, the influence of the cooling method external to the package must be taken in to account to establish the overall $R_{th,j-a}$ of the system. Figure 6 below highlights a few commonly used cooling approaches and their effective heat transfer coefficient for the different packaging configurations described in [58]. After establishing the $R_{th,j-c}$, this can be used as a general guideline for finding an appropriate HTC to design for a target $T_j$ for a power module. For example, two-phase, jet impingement and immersion cooling, among others, can improve upon the performance of the conventional finned heat sinks and liquid cold plates [63].

![Figure 6. Junction-to-ambient thermal resistances for a Ga$_2$O$_3$ SBD under various packaging configurations and cooling techniques [58]](image-url)
2.3 High-Temperature Packaging Materials

Moving to higher-temperature operation and higher power densities exacerbates the need for robust and reliable packaging materials. While the strategies discussed in the previous sections can help to extract the heat generated by the devices, high-temperature ambient environments and increased power density necessitate stability and support from all packaging materials at elevated temperatures. The reliability of conventional packaging components, namely die attach, interconnects, substrates, and encapsulation materials must be evaluated, and their limitations addressed, for successful high-temperature operation.

2.3.1 Die attach

The die attach of the package is tasked with providing a reliable connection between the device and its associated substrate(s), while maintaining high electrical and thermal conductivities [64]. Defects in the die attach can lead to heightened $R_{th,j-c}$, which will cause an increase in temperatures inside the package, leading to potential degradation and failure of both the package and the device [65]. When moving to operating temperatures surpassing 250 °C, commonly used tin- and lead-based solders will either surpass their safe working temperatures or degrade significantly [34]. In addition, careful consideration must be made to match the CTE of the die attach to that of the chip and the substrate in order to minimize heightened thermo-mechanical stresses that will be compounded by high-temperature operation [59] [66]. Table III below identifies the key properties of commonly used methods and potential high-temperature die attach materials.
Sintered nano Ag has a superior maximum operating temperature, thermal and electrical conductivities, improved thermal cycling reliability, and a CTE closer to that of many WBG and UWBG semiconductor materials (e.g., $3.77 \times 10^{-6} \, ^\circ C^{-1}$ of Ga$_2$O devices [67]) when compared to conventionally used solder materials, making it a suitable choice as a high-temperature die attach material [68] [69]. In addition, large-area silver sintering allows for the reliable construction of multi-layer substrates for electric field control [70] [71] and bonding of substrates to baseplates, enabling novel packaging configurations to assist in thermal management and mechanical reliability [72].

### 2.3.2 Package Substrate(s)

Metal-laminated-ceramic substrates are commonly used in power module packaging, as they provide a good combination of electrical interconnection and isolation while maintaining relatively high thermal conductivities; contributing less overall to the $R_{th\,j-c}$ than a typical isolating thermal interface material [73]. The substrate is also critical for heat extraction, in many instances serving as a first-level heat extraction and spreading layer. However, when operating at elevated temperatures, thermal cycling of the substrate can cause cracking, warping that leads to the shearing of the die attach layers, and/or delamination of the layers, all of which are severe reliability concerns [74]. As such, a careful selection of packaging materials with similar CTEs
to minimize stresses seen across and throughout the substrate is essential. Table IV below summarizes some commonly used metal ceramic substrate technologies and their relevant material properties.

Table IV: Critical properties of metal-ceramic substrates [75] [76]

<table>
<thead>
<tr>
<th>Property</th>
<th>DBC/Al₂O₃</th>
<th>DBC/AlN</th>
<th>DBA/Si₃N₄</th>
</tr>
</thead>
<tbody>
<tr>
<td>Electrical</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric strength (kV mm⁻¹)</td>
<td>15</td>
<td>15–20</td>
<td>18</td>
</tr>
<tr>
<td>Mechanical</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Young’s modulus (GPa)</td>
<td>340</td>
<td>302–348</td>
<td>260–320</td>
</tr>
<tr>
<td>Flexural strength (MPa)</td>
<td>350</td>
<td>320</td>
<td>900</td>
</tr>
<tr>
<td>Thermal</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CTE (ppm K⁻¹ at room temperature)</td>
<td>7.5</td>
<td>4.6</td>
<td>3.4</td>
</tr>
<tr>
<td>Thermal conductivity (W m⁻¹ °C⁻¹)</td>
<td>19–26</td>
<td>180</td>
<td>90</td>
</tr>
<tr>
<td>Thermal cycles to failure (100°C–350°C)</td>
<td>50–75</td>
<td>100</td>
<td>&gt;1380</td>
</tr>
</tbody>
</table>

While more expensive, the improved reliability and well-matched CTE of the direct-bonded aluminum (DBA) silicon nitride (Si₃N₄) substrates seem to be the logical choice for high-temperature operation of WBG and UWBG-based power modules.

2.3.3 Interconnects

As was highlighted in section 2.1, to effectively extract the heat from Ga₂O₃ devices junction-cooling is desirable. Therefore, the power and signal interconnects within the package must be able to conduct heat in addition to providing low-resistance, low-inductance electrical paths. The most commonly used interconnect in power modules are wire bonds; however, this technology generally only permits for bottom-side cooling so alternatives must be investigated.

As demonstrated in [77], solder bumps or solder balls can be used to in a flip-chip bonding configuration to allow for a direct attach of the junction of the device to the high-thermal conductivity substrate. While this reduced the parasitic resistance by 24% and the loop inductances by 3 times over a traditional wire-bonded module, due to limited working temperatures of solder alloys this is unfortunately not a viable option for high-temperature operation.
Along the same lines solid metallic interposers (also referred to as posts) using silver sinter attach between the junction of the device and the substrate have been shown to be an effective high-temperature alternative to solder-based flip chip bonding.

**Figure 7. 2D cross-section of double-side cooled module using metal interposers**

The use of molybdenum (Mo) posts was demonstrated in [78], resulting in 4.4 nH and 3.8 nH power- and gate-loop inductances, respectively. In addition, the low CTE of Mo is well matched to that of the aforementioned WBG and UWBG semiconductors, making it a great candidate for high-temperature operation. In [79], porous silver posts are used, which results in a further reduction of junction-temperature for the same power loss over Cu and Mo posts, due to the higher thermal conductivity of Ag. In addition, the lower elastic modulus of the soft silver posts may help to mitigate heightened thermo-mechanical stresses associated with high-temperature operation.

Another potential interposer material is thermal pyrolytic graphite (TPG). TPG is a relatively new material used in high-performance heat spreaders and heat sinks. TPG has high in-plane thermal conductivity exceeding $1,100 \frac{W}{mK}$, comparable to that of CVD diamond but with a low thru-plane thermal conductivity at only $10 \frac{W}{mK}$. This anisotropic thermal conductivity allows for directed and controllable heat flow [80]. It can be used to minimize thermal coupling between
adjacent dies, thereby reducing the maximum junction temperature of each. Furthermore, TPG has an in-plane CTE of -1 ppm/K and a relatively low elastic modulus, which can help to alleviate thermo-mechanical stresses. The low modulus, moderate CTE, and high thermal conductivity make TPG a compelling candidate to address the thermo-mechanical stress and heat-spreading concerns associated with the thermal management of Ga$_2$O$_3$ devices.

**Table V. Critical properties of potential interposer materials [79] [80]**

<table>
<thead>
<tr>
<th>Material</th>
<th>Elastic modulus (GPa)</th>
<th>CTE (ppm/K)</th>
<th>Thermal conductivity (W/mK)</th>
<th>Density (kg/m$^3$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cu</td>
<td>128</td>
<td>16.5</td>
<td>385</td>
<td>8960</td>
</tr>
<tr>
<td>Mo</td>
<td>320</td>
<td>4.9</td>
<td>142</td>
<td>10200</td>
</tr>
<tr>
<td>Sintered-Ag</td>
<td>6</td>
<td>18.9</td>
<td>175</td>
<td>8500</td>
</tr>
<tr>
<td>TPG</td>
<td>133</td>
<td>-1</td>
<td>1500</td>
<td>1300-2265</td>
</tr>
</tbody>
</table>
Chapter 3. High Temperature Encapsulation Investigation [81]

The aspect of packaging that arguably requires the most innovation for high-temperature operation is the encapsulation material. Conventional polymeric encapsulation materials are inexpensive and exhibit excellent insulation properties; however, they are limited due to their $T_g$ and thermal decomposition points, degrading significantly and losing both their dielectric and mechanical properties at temperatures exceed 150 °C – 200 °C [82]. Keeping in mind the aforementioned roles of an encapsulation material from Chapter 1—protections against electrical breakdown, chemical erosion, moisture absorption, and hazardous radiation, as well as relief of mechanical stresses and shock [21]—Table VI below details critical properties for an encapsulation material for a 1.2 kV, 300 °C Ga$_2$O$_3$ power module.

Table VI: Critical properties of encapsulation materials for a high-temperature medium voltage power module [81]

<table>
<thead>
<tr>
<th>Property</th>
<th>Desired Value</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Electrical</strong></td>
<td></td>
</tr>
<tr>
<td>Dielectric strength</td>
<td>$\geq$ 10 kV/mm (Or as needed for application)</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>$&lt; 5$</td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td></td>
</tr>
<tr>
<td>Glass transition temperature $(T_g)$</td>
<td>$&gt; \text{Working temperature (°C)}$</td>
</tr>
<tr>
<td>Thermal conductivity $(k)$</td>
<td>$&gt; 1 \text{ (W/mK)}$ (As high as possible)</td>
</tr>
<tr>
<td>Processing temperature</td>
<td>$&lt; \text{Safe component temperature}$</td>
</tr>
<tr>
<td><strong>Mechanical</strong></td>
<td></td>
</tr>
<tr>
<td>Coefficient of thermal expansion $(\alpha)$</td>
<td>Matched to device, die attach and substrate (ppm/K)</td>
</tr>
<tr>
<td>Elastic modulus $(E)$</td>
<td>4-10 (GPa)</td>
</tr>
<tr>
<td>Viscosity $(\eta)$</td>
<td>$&lt; 20 \text{ Pa-sec for underfill (50 for encapsulation)}$</td>
</tr>
</tbody>
</table>
The standard IEC 61287-1 defines testing requirements for the partial discharge inception voltage (PDIV) and breakdown strength of dielectric materials for use in power module and converter applications [83]. These values must be scaled accordingly with the maximum operating voltage of the application and the minimum spacing between potentials in the given configuration. When designing for high-temperature operation special consideration should be made, as the PDIV of some dielectric materials have been experimentally shown to degrade by up to 53% over a temperature range of 25 °C – 250 °C [26] and should be tested appropriately.

As for the thermal design, it is self-evident that the working temperature of the encapsulation material, normally either dictated by the $T_g$ or thermal decomposition point of the material, must be higher than that of the expected operating temperature of the module. Similarly, the processing and/or curing temperature should be kept well below a safe temperature for all other components of the package (i.e., interconnect melting temperature, device annealing temperature, etc.). As described in Chapter 2, each component in the package contributes to the overall $R_{th_{j-c}}$. Conventional encapsulants, such as epoxy molding compounds and silicone gels, have low thermal conductivities; typically between $1 - 5 \frac{W}{mK}$. For packages targeting higher power density, a material with higher thermal conductivity could assist in maintaining the temperature below component maximums, and in turn mitigating the thermomechanical stresses inside the package [15]. The addition of high thermal conductivity fillers, such as silica [84] and hexagonal boron nitride [85], has been demonstrated as an effective way to increase the bulk thermal conductivity of conventional polymeric encapsulation materials. This strategy has the drawback of an increase in viscosity that may limit the composite material’s use for a DSC or flip-chip configuration where the encapsulation material has to flow under small facets and areas that require electric-field control.
The final category to be considered is the mechanical properties of the encapsulation material. The material’s CTE should be matched as closely as possible to the other module components (i.e. devices, die attach, substrate), as CTE mismatch is the primary source of thermo-mechanical stresses in a package when operating at elevated temperatures [86]. While the low elastic modulus of soft encapsulants such as silicone gels help in reducing thermo-mechanical stresses in conventional BSC configurations, recent studies have suggested that using materials of a higher elastic modulus (between 4 GPa - 10 GPa) can be beneficial to increasing the reliability of TSC and DSC packaging configurations, as they can better distribute the thermo-mechanical stresses [87] [88]. Finally, to facilitate DSC packaging configurations, an uncured viscosity of 20 Pa-sec is desirable so that the encapsulant can flow under the smallest facet of the package while being sufficiently degassed [89].

3.1 Material Survey and Selection

With the criteria established, a survey of candidates for an encapsulation material for a 1.2 kV, 300 °C Ga₂O₃ power module was conducted. The materials were selected to attempt to match the CTE of Ga₂O₃ in an attempt to minimize the thermomechanical stresses seen between the die and the dielectric. In addition, as a TSC configuration will be employed (details on the module design in the following sections), the uncured viscosity should be sufficiently low to facilitate flow and outgassing under a 0.5 mm facet. In this work, six materials were identified and evaluated as candidates for use as high-temperature encapsulants. High-temperature silicone gel was used as a reference material and was compared to five novel encapsulants including an epoxy resin, a hydro-set cement, two low melting point (LMP) glass compounds, and a ceramic potting compound. The results of the survey are summarized in Table VII below.
In addition, cyanate ester resin [90] and benzocyclobutene [91] were identified as potential candidates due to their high glass transition temperatures; however, they were not included in the testing process due to limited commercial availability.

Table VII. Potential encapsulation materials for a 1.2 kV, 300 °C Ga₂O₃ power module

<table>
<thead>
<tr>
<th>Property</th>
<th>Desired Value</th>
<th>Silicone Gel (NuSil 2188)</th>
<th>Epoxy Resin (Durapat 863)</th>
<th>Hydrosel Cement (Ceramacast 675-N)</th>
<th>Ceramic Potting Compound (Durapat 801)</th>
<th>LMP Glass (Schott 339)</th>
<th>LMP Glass (Schott 393)</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Electrical</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Dielectric strength (kV/mm)</td>
<td>≥10</td>
<td>19.5</td>
<td>21.65</td>
<td>11.81</td>
<td>13.78</td>
<td>N/A (assumed high)</td>
<td>N/A (assumed high)</td>
</tr>
<tr>
<td>Dielectric constant</td>
<td>&lt;5</td>
<td>2.9</td>
<td>3.5</td>
<td>-</td>
<td>-</td>
<td>8.4</td>
<td>11.6</td>
</tr>
<tr>
<td><strong>Thermal</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Glass transition/operating temp</td>
<td>&gt;300</td>
<td>250</td>
<td>314</td>
<td>1100</td>
<td>N/A</td>
<td>325</td>
<td>325</td>
</tr>
<tr>
<td>Thermal conductivity (W/mK)</td>
<td>&gt;1 (high as possible)</td>
<td>N/A</td>
<td>1.3</td>
<td>N/A (assumed high)</td>
<td>1.15</td>
<td>N/A</td>
<td>N/A</td>
</tr>
<tr>
<td>CTE (ppm/K)</td>
<td>3.77 ± 1.0</td>
<td>N/A</td>
<td>3.4</td>
<td>5.6</td>
<td>4.3</td>
<td>4.7</td>
<td>4.7</td>
</tr>
<tr>
<td>Elastic Modulus (GPa)</td>
<td>4-10</td>
<td>&lt;1</td>
<td>2.65</td>
<td>N/A (assumed high)</td>
<td>N/A</td>
<td>58</td>
<td>58</td>
</tr>
<tr>
<td>Viscosity (Pa·sec)</td>
<td>&lt; 20</td>
<td>13</td>
<td>2</td>
<td>15</td>
<td>2.8</td>
<td>50+</td>
<td>50+</td>
</tr>
<tr>
<td>Processing temperature (°C)</td>
<td>&lt;300</td>
<td>150</td>
<td>350</td>
<td>22</td>
<td>22</td>
<td>510-600</td>
<td>420-500</td>
</tr>
</tbody>
</table>
3.2 Testing Procedure and Rationale

3.2.1 Gas Pycnometry with Thermal Aging

Unless processed in an inert environment, pockets of entrapped air in dielectric materials (commonly referred to as voids) represent areas of lower dielectric strength that can lower the reliability of a power module [92] [93]. Void-free processing of the encapsulation material is a key component of power module packaging for predictable and reliable insulation. In order to establish the voiding content of a sample, gas pycnometry can be employed. Testing was carried out per the standard USP 699 [94]. Helium gas, used due to its small particle size, is flowed into a sample chamber of known volume, and occupies the voids of the sample. The change in pressure in the system can then be used to calculate the porosity of the sample. Each sample was then aged for 50 hours in 250 °C air to track the change in voiding concentration when exposed to elevated temperatures. This will later be used to correlate to any degradation in high temperature storage life (HTSL) dielectric strength during the PDIV and breakdown testing.

There are two limitations to this setup from a power module perspective. First, the sample size is limited to 1.85 cm x 3.95 cm, which does not allow for testing of the voiding concentration in a complete module configuration. Second, if there are any hermetic voids entrapped with openings smaller than that of a helium particle, they may not be included in the relative density calculation. If further voiding is evident or suspected, scanning electron microscopy (SEM) or x-ray imaging may be necessary to garner a more exact result. Figure 8 below depicts the test setup and relevant porosity calculation, and Table VIII contains the results from that testing.
Figure 8. Gas pycnometry setup and relative density calculation [95]

Table VIII. Gas pycnometry with thermal aging test results

<table>
<thead>
<tr>
<th>Material</th>
<th>Porosity Unaged</th>
<th>Porosity 50 Hour Soak at 250 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone Gel (NuSil 2188)</td>
<td>13.6%</td>
<td>15.3%</td>
</tr>
<tr>
<td>Epoxy Resin (Durapat 863)</td>
<td>13.3%</td>
<td>18.3%</td>
</tr>
<tr>
<td>Hydroset Cement (Ceramacast 675-N)</td>
<td>40.7%</td>
<td>45.4%</td>
</tr>
<tr>
<td>Ceramic Potting Compound (Durapat 801)</td>
<td>34.5%</td>
<td>46.55%</td>
</tr>
<tr>
<td>LMP Glass (Schott 339)</td>
<td>19.1%</td>
<td>19.3%</td>
</tr>
<tr>
<td>LMP Glass (Schott 393)</td>
<td>32.1%</td>
<td>32.7%</td>
</tr>
</tbody>
</table>

As anticipated, the porosity of the liquid binder ceramic-based materials (ceramic potting compound and hydroset cement) was higher because of the larger particulate size and because the degassing was performed before and not during the cure, which allowed gasses to be entrapped as the liquid evaporated during the curing process. All other materials experienced a nominal increase in porosity as they were thermally aged, with the only considerable degradation observed being the ceramic potting compound; exhibiting a 12% increase in average porosity. Additionally, the second LMP glass composite (Schott 393) had a higher nominal voiding content as cracking occurred during the fusing of the glass frit.
3.2.2 Substrate Compatibility and Processability

In the survey of high-temperature capable substrate materials, DBA substrates were identified as a good candidate. In order for successful power module fabrication and operation, proper adhesion must be made between the encapsulation and substrate. A qualitative processability test was performed, where each material was processed by potting a 3 mm thick layer onto a 27 mm x 15 mm DBA substrate in a polyimide tape-coated aluminum foil boat, (seen in Figure 9 below) in order to establish the feasibility of each material for use in a power module. The subsequent section summarizes the processing and curing processes of each material and the results of the tests.

![Figure 9. Test coupon for substrate compatibility and processability](image)

Table IX. Processing profiles and substrate compatibility test results

<table>
<thead>
<tr>
<th>Material</th>
<th>Max Processing Temperature (°C)</th>
<th>Processing Time</th>
<th>Outcome/Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone Gel (NuSil 2188)</td>
<td>150</td>
<td>30 minutes</td>
<td>Void free/good substrate adhesion</td>
</tr>
<tr>
<td>Epoxy Resin (Durapot 863)</td>
<td>175</td>
<td>3-4 hours</td>
<td>Void free/good substrate adhesion</td>
</tr>
<tr>
<td>Hydroset Cement (Ceramacast 675-N)</td>
<td>230</td>
<td>2-4 hours</td>
<td>Good substrate adhesion</td>
</tr>
<tr>
<td>Ceramic Potting Compound (Durapot 801)</td>
<td>100</td>
<td>4 hours</td>
<td>Outgas not possible/major cracking</td>
</tr>
<tr>
<td>---------------------------------------</td>
<td>-----</td>
<td>---------</td>
<td>-----------------------------------</td>
</tr>
<tr>
<td>LMP Glass (Schott 339)</td>
<td>510</td>
<td>2.5 hours</td>
<td>Outgas not possible/major cracking</td>
</tr>
<tr>
<td>LMP Glass (Schott 393)</td>
<td>420</td>
<td>2.5 hours</td>
<td>Outgas not possible/major cracking</td>
</tr>
</tbody>
</table>

Both the silicone gel and epoxy resin were easily outgassed in a vacuum chamber at 28 in/Mg with no visible voids in the semi-transparent materials. In addition, they both exhibited sufficiently low viscosity to fill the 1mm gap between pads, a spacing commonly found between potentials in power module applications. Similarly, the hydroset cement showed a low enough viscosity to fill the small facet and had a long enough potting life to be outgassed in the vacuum chamber. All three of these materials also displayed good mechanical adhesion to the substrate, with only small surface dimples forming in the hydroset cement after curing.

The ceramic potting compound was unable to be degassed due a very short potting life that caused it to harden in the vacuum chamber, forming large pockets of air inside the material. In addition, the material formed deep cracks during the cure profile, losing its adhesion to the substrate and falling away. As such, the ceramic potting compound was also deemed inadequate for use in a power module and was not investigated for its electrical properties in the subsequent section.

Finally, the LMP glass compounds proved very difficult to process as they have significantly higher processing temperatures, 420 °C and 510 °C, respectively. Even with pre-heating substrates and a slow cooling time, large cracks formed through both glass samples similar to what was observed in [27]. In addition, when pouring the molten glass was still quite viscous, with no opportunity to degas without a high-temperature vacuum furnace. While polyimide CTE buffers and other manufacturing techniques could be implemented to potentially
use these materials successfully, they were eliminated from contention as their processability was too low for reliable fabrication.

3.2.3 Partial Discharge, Breakdown, and High-Temperature Storage Life Reliability

Between the results of the gas pycnometry and processability testing the set of potential candidates was down to the silicone gel, the epoxy resin, and the hydroset cement. Next, the dielectric capabilities of these three materials had to be evaluated. PDIV is a good metric for the performance of electrical insulation in power modules, as it represents the ability of the system to recover from heightened potential and/or over voltage events [26]. In addition, knowing the breakdown strength of a potential passivation material is critical, as it gives a guideline that your nominal operating voltage should be significantly below. In order to characterize the electrical insulation of each material, test coupons were fabricated, as shown in Figure 9. Two bent silver leads were sintered to a DBA substrate; a 1 mm gap—a common spacing in power modules—was etched between the conductive pads of metal on the top side, and the encapsulation was then processed on top. The bottom metallization was not removed, as this is commonly used for connection to a baseplate.

![Figure 9. Test coupon for PDIV and breakdown testing](image)

Tests were performed by an Omicron MPD600 system following the method described in IEC60664 [96]. One of the Ag leads was connected to the HV electrode, while the other lead and the bottom metal were grounded. The sample was then submerged in electrical insulation oil, in
order to ensure that the PD and breakdown occurred between the conducting traces on the substrate. A 60-Hz sinusoidal-signal was applied and ramped from 0 V at approximately 100 V/s. This was monitored and recorded through the MPD software to track PD events with a 10 pC threshold, as well as breakdown.

**Figure 10. PDIV and breakdown test configuration**

To test the high-temperature stability of each encapsulant, identical samples were fabricated and soaked at 250 °C in air. Subsets of three samples were tested at different intervals—unaged, 50 hours, and 100 hours—to test the high-temperature storage life reliability of the encapsulation materials. The results from these tests, as well as photos of the samples, can be seen in Table X and Table XI, respectively.
Table X. PDIV and breakdown test results

<table>
<thead>
<tr>
<th>Material</th>
<th>Unaged PDIV</th>
<th>Aged 50 Hours at 250 °C PDIV</th>
<th>Aged 100 Hours at 250 °C PDIV</th>
<th>Unaged Breakdown</th>
<th>Aged 50 Hours at 250 °C Breakdown</th>
<th>Aged 100 Hours at 250 °C Breakdown</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone Gel (NuSil 2188)</td>
<td>8.13 kV</td>
<td>7.90 kV</td>
<td>5.28 kV</td>
<td>12.78 kV</td>
<td>12.15 kV</td>
<td>13.27 kV</td>
</tr>
<tr>
<td>Epoxy Resin (Durapot 863)</td>
<td>6.37 kV</td>
<td>4.31 kV</td>
<td>4.76 kV</td>
<td>11.18 kV</td>
<td>7.25 kV</td>
<td>7.92 kV</td>
</tr>
<tr>
<td>Hydroset Cement (Ceramacast 675-N)</td>
<td>-</td>
<td>-</td>
<td>-</td>
<td>1.62 kV</td>
<td>2.01 kV</td>
<td>1.94 kV</td>
</tr>
</tbody>
</table>

Table XI. PDIV and breakdown samples unaged versus aged 100 hours at 250 °C

<table>
<thead>
<tr>
<th>Material</th>
<th>Unaged</th>
<th>100 Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicone Gel (NuSil 2188)</td>
<td><img src="image1.png" alt="Image" /></td>
<td><img src="image2.png" alt="Image" /></td>
</tr>
<tr>
<td>Epoxy Resin (Durapot 863)</td>
<td><img src="image3.png" alt="Image" /></td>
<td><img src="image4.png" alt="Image" /></td>
</tr>
<tr>
<td>Hydroset Cement (Ceramacast 675-N)</td>
<td><img src="image5.png" alt="Image" /></td>
<td><img src="image6.png" alt="Image" /></td>
</tr>
</tbody>
</table>

The PDIV of the silicone gel degraded by 35%, as was in line with previous works on polymeric encapsulations [26]. Interestingly, the breakdown strength was largely unaffected, even increasing slightly after being aged. This is theorized to be due to further vulcanization of the rubber, but further investigation is necessary to confirm this hypothesis [97]. Next, the epoxy resin saw an initial drop of 32% for the PDIV and 35% for the breakdown strength, but no further degradation was observed between the 50- and 100-hour aging steps, suggesting a good sustained electrical performance event when exposed to elevated temperatures after the initial
burn-in period. Lastly, the hydroset cement exhibited no PD events, instead reaching breakdown at ~2 kV. While this was significantly lower than the other materials tested, no degradation was observed, once again highlighting its potential as a high-temperature stable encapsulation material that may be suitable for a lower voltage, elevated temperature application.

From a visual and mechanical standpoint, slight discoloration of the silicone gel can be seen with aging, but no visible cracking or deformation occurred. The epoxy resin grew significantly darker in color and some cracks appeared along the surface surrounding the terminals, but none penetrated to the substrate. Lastly, the cement saw no real observable changes, which was anticipated due to its high-temperature stability rating from the manufacturer.

3.3 Results and Implications

While initially selected as a reference material, the silicone gel performed adequately for use in a power module configuration with temperatures up to 250 °C, exhibiting PDIV and breakdown strengths after aging of 5.28 kV and 13.27 kV, respectively. Though some surface cracking did occur, the epoxy resin was also identified as a good candidate for these high-temperature applications, effectively showing no degradation between the 50- and 100-hour aging interval, which can be correlated to the 5% increase in its porosity. Finally, the hydroset cement seems to be limited to lower voltages than the other materials, assumedly due to its high porosity, exhibiting breakdown at ~2 kV; however, it is very thermally stable and has an assumedly higher thermal conductivity than the other materials tested, as it contains a high content of Al₂O₃ ceramic.

As a continuation of this work, testing at higher-temperatures and/or for longer thermal soak times should help in establishing the high-temperature reliability of the selected materials.
In addition, performing the PDIV testing at elevated temperatures and over repeated partial discharge events should garner a clearer image of the electrical stability of these materials at high temperatures. To better understand the mechanical resilience of the materials, thermal gravimetric analysis could be implemented to establish the decomposition point of each material to observe the upper limits of their potential operating temperatures. Finally, testing the adhesion strength between the encapsulation material and the substrate through the use of shear tests with thermal aging intervals could be an effective way to establish the high-temperature mechanical reliability of the encapsulation/substrate interface. To close, encapsulation materials were identified and tested for use in tandem with UWBG semiconductor materials for high-temperature power module applications, which will assist in unlocking the full benefits of next generation devices.
Chapter 4. Electro-Thermal Modeling for Ga$_2$O$_3$ Device/Package Co-Design

[98]

4.1 Background and Challenges

To reiterate, for WBG and UWBG power devices, the combination of smaller desirable device sizes, an increase in potential current density, and a higher electric field can cause large heat fluxes within the devices, potentially leading to hot-spots within the device and in turn, local thermal runaway [15]. This in tandem with the low thermal conductivity of Ga$_2$O$_3$ exacerbates the need for design tools that can accurately observe the thermal interactions in the device(s) and package, as well the electrical performance of the device(s).

In the design of the package, multiphysics 3D-FEA tools (i.e., ANSYS or COMSOL) are typically used. These models usually assume an averaged power dissipation over the junction side of the device—reducing it to simply a block of its thermal and mechanical properties—and measure the resulting temperature distribution due to joule heating while neglecting the electro-thermal effects that occur in the sub-micron device structures. These simulations are widely used due to their relatively low computational demands and ability to model not only the heat interactions between material interfaces, but also realistic thermal boundary conditions (such as convective cooling). Finally, these tools also typically have a self-contained thermo-mechanical model that is especially important when targeting complex packaging schemes and high-temperature operation.

Conversely, the typical physics-based 2D-TCAD simulations (i.e., Silvaco or Sentaurus) used in semiconductor device design accurately model the electro-thermal behaviors within the device by solving the current continuity, drift-diffusion, heat generation, and the heat diffusion equations—many of which are temperature dependent—to derive the electrostatic potential,
electron concentration, and lattice temperature [99]. However, the packaging and external cooling structures are simplified to a nominal boundary thermal resistance or heat extraction coefficients, neglecting larger packaging elements in the heat flow path (e.g., the substrate and baseplate) and the dimensionality of heat spreading and transfer [29] [100]. 3D-TCAD models can mitigate these 2-D heat-spreading errors but require much more involved meshing, which can add to the complexity and duration of the design process. In addition, between their iterative method physics-based solvers and the large difference in length scales between the electrically-active regions (e.g., nanometer-sized edge termination structures and drift regions) and the thermal diffusion regions (e.g., millimeter-sized packaging structures), the computational demands, and in turn solve times, tend to be much higher [101]. Furthermore, these programs do not have thermo-mechanical modeling, which limits their use as a device/package co-design tool.

4.2 Modeling Method Comparison

Despite being common electro-thermal simulation tools, a direct comparison between the models still holds value in evaluating whether or not the higher computational demands of the physics-based TCAD models are warranted, or if a sufficiently accurate temperature distribution is attainable from a 3D-FEA model. This comparison will be made by applying identical structures, loads and thermal boundary conditions. The results of these simulations will be used to evaluate the benefits and limitations of the 3D-FEA, 2D-TCAD, and 3D-TCAD tools and to ascertain if some new or combined methodology is needed.

In order to evaluate the models against one another, the lack of thermal boundary conditions in the TCAD models must be addressed. As such, an additional body was added to the TCAD simulations to emulate the thermal boundary condition; henceforth referred to as a thermal node (similar to that described in [102]). The heat transfer coefficient for the thermal node is found by
taking the power dissipated and dividing by the temperature at the thermal boundary of the FEA simulation, and then again at some known distance away from the boundary, taking the difference and multiplying by the area (3).

\[ k = \frac{P}{(T_{\text{boundary}} - T_{\text{node}})l_{\text{node}}w_{\text{node}}} \]  

(3)

Where \( k \) is the heat transfer coefficient, \( P \) is the power dissipation, \( T_{\text{boundary}} \) is the peak temperature at the applied thermal boundary condition, \( T_{\text{node}} \) is the peak temperature on the bottom surface of the thermal node, \( l_{\text{node}} \) is the length of the thermal node, and \( w_{\text{node}} \) is the width of the thermal node.

As a base case for evaluation, a large Ga\( _2 \)O\( _3 \) SBD with die thickness of 500 \( \mu \)m, an area of 25 mm\(^2\), and anode diameter of 3 mm. This device, presented in [103], was fabricated during a recent study at the Center for Power Electronics Systems at Virginia Tech, and could be used to experimentally validate simulation results in the future. The device was then bonded to a commonly used AlN direct bond copper (DBC) in a BSC configuration, the dimensions of which were selected based on a common 45\(^\circ\) heat spreading assumption, such that the full heat interaction between the device and the first-level packaging could be observed. A load condition of 10 W was selected, as this is the approximate loss for a diode operating in a 1.2 kV module in a buck converter configuration.

To find an appropriate thermal boundary condition for the comparison, the effect that the convection coefficient and the thermal conductivity of the die have on the heat flux through the center of the die and through the temperature distribution across the anode surface were evaluated in ANSYS Workbench. The aforementioned Ga\( _2 \)O\( _3 \) (thermal conductivity of 14 W/mK) and a SiC diode of the same dimensions (thermal conductivity of 370 W/mK) were simulated at the same loss,
and a parametric sweep of the convection coefficient for both was performed. The results are shown in Figure 12.

![Graphs showing temperature difference versus convection coefficient](image)

**Figure 12.** Temperature difference versus convection coefficient (a) across the anode surface (from the center of the die to the edge of the die) and (b) vertically through the center of the die for Ga$_2$O$_3$ and SiC

From the resulting temperature distributions, it was found that comparable trends were found for convection coefficients between 500 W/m$^2$K – 5,000 W/m$^2$K. While the magnitudes differ, the similarity in trends show a range on which the relative effectiveness of the cooling between the two semiconductor materials corresponds, which will be meaningful for a comparison between the two materials in the next section. For this reason, a convection coefficient of 500 W/m$^2$K and equivalent thermal node HTC were used in the remaining simulations. With all parameters now well-defined, the structure, load, and boundary conditions for the comparison are detailed in Figure 13.
Figure 13. Dimensions, load conditions, and boundary conditions used in modeling comparison simulations

Figures 14 and 15 show cross sections; the simulated device structure and a TCAD model, respectively. The device has a Ni/Au Schottky contact with SiO₂ edge termination structures and a Ti/Au ohmic contact. The n⁻ epi layer has a doping concentration of 2.1 x 10¹⁶ cm⁻³, while the n⁺ bulk substrate has a doping concentration of 1.3 x 10¹⁹ cm⁻³ [103]. All together the device has a total thickness of just over 500 μm.

Figure 14. Simulated large area Ga₂O₃ Schottky barrier diode
For fair comparison between the 3D-FEA and TCAD models, the mesh sensitivity of both simulations needed to be in close agreement. The electrically active areas of the TCAD models, not present in the 3D-FEA simulation, were meshed with a triangular element of 3 μm² to accurately solve the current continuity, drift-diffusion, and lattice heating equations. A mesh sensitivity study was then conducted in ANSYS Workbench, and it was found that an element size of 150 μm² triangular elements was the minimum point of convergence for a steady state thermal simulation with the structure, load, and boundary conditions described in Figure 13. This mesh was then matched in the TCAD simulations as well.

The resulting temperature distributions (both across the surface of the die and vertically through the center of the die) from the steady-state electro-thermal simulations are plotted in Figure 16. The peak junction temperature of each fall within 2% of one another, giving confidence that the models are well calibrated to each other, and that the thermal node is emulating the desired thermal boundary condition accurately.
Though the $\Delta T$ across the Ga$_2$O$_3$ diode surface and vertically through the device for the 3D-FEA and 3D TCAD simulations were in close agreement, the 2D TCAD simulation showed more than a 30% and 10% difference, respectively. This emphasizes the aforementioned 2D heat spreading margin of error. In addition, the temperature distribution across the anode area in the 3D-FEA model shows a steeper decline compared to the TCAD models; showing ~30 °C lower temperature at the outer edge of the device anode compared to the TCAD models. This discrepancy can be attributed to the lattice heating constants and electron scattering effects that are accounted for in the physics-based TCAD simulations, which are neglected by the 3D-FEA simulation. Finally, the 3D-TCAD model, assumed to have the most accurate heating model, shows a much lower heat flux through the die. Table XII summarizes key results and takeaways from this comparison study.
Table XII. Modeling method comparison results

<table>
<thead>
<tr>
<th>Method</th>
<th>Solve Time</th>
<th>Peak Temperature</th>
<th>ΔT Across Ga2O3 Diode Surface</th>
<th>ΔT Through Ga2O3 Diode</th>
</tr>
</thead>
<tbody>
<tr>
<td>ANSYS Workbench</td>
<td>~2 minutes</td>
<td>358 °C</td>
<td>85 °C</td>
<td>65 °C</td>
</tr>
<tr>
<td>Silvaco TCAD 2D</td>
<td>~7 minutes</td>
<td>351 °C</td>
<td>59 °C</td>
<td>59 °C</td>
</tr>
<tr>
<td>Silvaco TCAD 3D</td>
<td>~13 minutes</td>
<td>358 °C</td>
<td>85 °C</td>
<td>28 °C</td>
</tr>
</tbody>
</table>

Based on this study, conventional 3D-FEA simulations may not sufficiently depict hot spots and the thermal distribution of Ga2O3 devices. This is especially important when higher power and higher-temperature operation is desired, as these are the areas most likely to experience heightened levels of thermo-mechanical stress and strain. For example, in [30] a 20% difference in maximum versus minimum strain energy density was observed in the die attach layer as a result of the temperature variations. This indicates that a differing thermal distribution can influence the thermo-mechanical stress and strain induced in a package, and should be accounted for as accurately as possible during the design stage. Additionally, this hot spotting may cause local thermal runaway and degraded electrical performance that must addressed in the design process [104].

4.3 Co-Design Platform Definition

It has been proposed in literature that some combination of packaging-scale 3D-FEA and device-level TCAD simulation could be utilized to create a self-contained device/package co-design platform for the accurate and efficient design of power modules [101]. This work aims to create and evaluate a self-contained simulation framework that would incorporate the accurate electro-thermal modeling of the device performance and thermal distribution provided by TCAD.
simulations, while reducing the overall computational demands by utilizing the efficient thermal and thermo-mechanical models found in 3D-FEA programs.

In the proposed method, 2D-TCAD is used to design for electrical parameters (e.g., edge termination and breakdown voltage). Next, the device model is transferred to a 3D TCAD model to account for 2D-heat spreading errors while maintaining the physics-based electro-thermal effects. A first iteration package is then built, and the thermal boundary conditions extracted per the thermal node method described in the previous section. The 2D- and 3D-TCAD models are then run again with the realistic thermal boundary conditions and the electrical performance of the device(s) noted. The resulting device temperature distribution is then exported and used as a load condition in the 3D-FEA simulation for full package thermal and thermo-mechanical simulations. This would be an iterative design process, allowing for adjustments of both the device and package in tandem to further optimize electrical and thermal performance. The co-design process flow is shown in Figure 17 below. Additionally, a summary of the discussed and proposed modeling methodologies can be seen in Table XIII below.
Table XIII. Modeling methodologies benefits and limitations

<table>
<thead>
<tr>
<th>Method</th>
<th>Benefit(s)</th>
<th>Limitation(s)</th>
</tr>
</thead>
<tbody>
<tr>
<td>3D-FEA</td>
<td>Quick solve time/ability to model convection coefficient</td>
<td>No electron scattering/no micro or nano scale device structures</td>
</tr>
<tr>
<td>Silvaco TCAD 2D</td>
<td>Accurate electro-thermal interactions</td>
<td>Potential 2D-3D heat spreading differences/no convection model</td>
</tr>
<tr>
<td>Silvaco TCAD 3D</td>
<td>Accurate electro-thermal interactions</td>
<td>Very long solve time/no convection model</td>
</tr>
<tr>
<td>TCAD → 3D-FEA</td>
<td>Quick solve time/accurate device level electro-thermal interactions</td>
<td>Static junction temperature in full package model</td>
</tr>
</tbody>
</table>

Figure 17. Proposed co-design process
4.4 Device Level Thermal Management Assessment

As Ga₂O₃ power devices are still a relatively immature technology, there is no definitively optimized design. One core benefit to the co-design strategy is the ability to alter both the device and the package in an attempt to improve thermal and electrical performance and accurately observe the interactions between the two. This permits analysis of the relationship between device structure dimensions and the resulting junction temperature and thermal distribution. As an example, in [105] the influence of the device substrate thickness and crystal orientation on the device temperature was evaluated. However, only the device was modeled, and the only thermal boundary condition applied was the thermal conductivity of the device bulk substrate, which may not be representative of the thermal distribution that occurs when the device is packaged.

In this work, realistic heat spreading and thermal boundary conditions were applied and parametric sweeps of the device thickness, chip side length, and anode diameter were performed. The same load and boundary conditions as in the previous section were applied (as pictured in Figure 13). In addition, both Ga₂O₃ (thermal conductivity of 14 W/mK) and SiC (thermal conductivity of 370 W/mK) devices were modeled for each case to observe if these device-scale modifications followed similar trends in junction temperature reduction for semiconductor materials with vastly different thermal conductivities.

4.4.1 Device Substrate Thickness

As was highlighted in Chapter 2, thinning the bulk substrate of a power semiconductor device is a proven method of reducing the overall $R_{th,j-c}$ of a packaged device. For instance, in [53] thinning the substrate of a SOI GaN HEMT from 500 µm to 100 µm yielded a 35% reduction of the self-heating thermal resistance. Using our calibrated TCAD simulation platform,
the diode substrate thicknesses was simulated from 500 µm - 100 µm, the results of which can be seen in Figure 18.

**Figure 18. Device substrate thickness versus junction temperature of Ga$_2$O$_3$ and SiC SBDs**

As anticipated, after thinning the substrate, and in turn the $R_{th-j-c}$, yields a significant reduction of 20% of the $T_j$ was observed in the case of the Ga$_2$O$_3$ SBD. A similar trend, but of lesser magnitude, is both expected and observed for the SiC SBD, as its intrinsic thermal resistance is significantly lower.

**4.4.2 Device Area**

Increasing the chip-side length, and in turn the area of the device, is another proven method to reduce the overall $R_{th-j-c}$. It was observed in [106] that an increase of the chip length (and in turn the available area for heat spreading) from 0.5 mm to 1 mm while maintaining a set contact size reduced the thermal resistance of a GaN LED by 50%. In this study, the side length, and in turn the device area as we assume a square die, was varied from 5 mm$^2$ to 8 mm$^2$, while all other simulation parameters were held constant. The output from this parametric sweep is seen in Figure 19.
Due to the low thermal conductivity of the Ga$_2$O$_3$ device, the addition of a wider area to spread the heat had negligible improvement on the $T_j$. On the other hand, the SiC SBD saw a ~15% reduction in $T_j$, due to an improved heat-spreading angle through the high thermal conductivity bulk substrate.

### 4.4.3 Device Contact Area

The last strategy that was investigated was to increase the contact area, and in turn the electrically active region of the device. While intuitive, for the same power dissipation this will decrease the loss seen and logically lower lattice heating per unit area. This was demonstrated in [107] as an effective method of reducing the overall junction temperature and avoiding localized self-heating. Here the anode diameter was swept from 2 mm to 5 mm, while keeping all other parameters static. The resulting junction temperatures are recorded in Figure 20.
Figure 20. Device contact area versus junction temperature of Ga$_2$O$_3$ and SiC SBDs

Similar trends are observed in both the Ga$_2$O$_3$ and SiC devices, with a stark decrease in $T_j$, both nearly converging to the ambient temperature defined by the thermal boundary condition. This suggests that increasing the relative size of the contact area for a set chip size and power loss can be an effective way of reducing $T_j$.

4.5 Modeling Investigation Results and Implications

While the magnitude of the Ga$_2$O$_3$ junction temperatures was higher, the resulting $T_j$ when making device-dimension modifications for both Ga$_2$O$_3$ and SiC devices follow similar trends. The substrate thinning is relatively more effective for the Ga$_2$O$_3$ device due to the low thermal resistance, which reduces the overall $R_{th,j-c}$ in a more meaningful way. Increasing the device contact area proved to be a very effective strategy to $T_j$, reducing the temperature of the Ga$_2$O$_3$ to the same temperature as the SiC when the full top surface of the device was utilized. This will also prove to be even more effective when TSC or DSC is employed, as it will further increase the heat spreading angle to the high-thermal conductivity substrate. Table XIV summarizes the effectiveness of the different device structure modifications that were simulated.
Table XIV. Impact of Ga$_2$O$_3$ device dimension modifications on thermal performance

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Base Case</th>
<th>Range</th>
<th>Min. Junction Temperature</th>
<th>Reduction from Base Case</th>
</tr>
</thead>
<tbody>
<tr>
<td>Substrate Thickness</td>
<td>500 µm</td>
<td>100 – 50 µm</td>
<td>274 °C (at 100 µm)</td>
<td>20 %</td>
</tr>
<tr>
<td>Device Area</td>
<td>5 mm$^2$</td>
<td>5 – 8 mm$^2$</td>
<td>343 °C (at 8 mm$^2$)</td>
<td>&lt;1 %</td>
</tr>
<tr>
<td>Contact Area</td>
<td>3 mm$^2$</td>
<td>2 – 5 mm$^2$</td>
<td>58 °C (at 5 mm$^2$)</td>
<td>84 %</td>
</tr>
</tbody>
</table>

This chapter outlines and evaluates an electro-thermal device/package co-design model. This process can be utilized for the efficient and accurate modeling of a Ga$_2$O$_3$ device(s) including any hot spots caused by self-heating and their effects on device electrical performance and associated packaging. This platform will be utilized in the subsequent section to aid in the design of a 1.2 kV, 300 °C half-bridge module utilizing Ga$_2$O$_3$ diodes.
Chapter 5. Ga$_2$O$_3$ Module Design

5.1 Design Targets and Rationale

To assess the potential of Ga$_2$O$_3$ power devices for high-temperature applications, a power module was designed for 1.2 kV, 300 °C operation. As discussed in Chapter 1, 900 V – 1200 V power modules are typically needed for traction and power conversion. For automotive and aerospace applications, the temperature target is driven by a desire for increased power density, a reduction of heavy and power-hungry cooling systems, and a preference for point load power conversion and actuation for both power density and efficiency, which may be directly against high-temperature engines and turbines. In addition, there is a desire for extreme environment capabilities in down-hole drilling (i.e., oil, gas, and geothermal), as well as space applications where the expected ambient operating temperatures exceed 250 °C [2].

In order to ensure reliable operation of the module at the desired temperature, rigorous thermal, electrical, and thermo-mechanical design was performed utilizing the co-design framework and material surveys conducted in previous sections. To highlight the potential benefits, this module design also permits for the replacement of Ga$_2$O$_3$ power devices with SiC devices in order to garner a fair comparison with state-of-the-art technologies. This comparison will evaluate the interdependencies of the devices’ electrical performance at high-temperature (i.e., a rise in on-resistance, lowering of breakdown voltage, leakage, etc.). The electrical, thermal, and reliability characteristics of the module will provide valuable insight into the prospects and challenges for Ga$_2$O$_3$-based high-temperature power electronics.
5.2 Topology and Device Selection

A half-bridge topology, consisting of two switching devices and two diodes, was selected for the module design for two primary reasons. First, half-bridge modules are widely used in power conversion for traction inverters and other drives and actuators in the aforementioned industries that would benefit from an increase of the available operating temperatures [108]. Second, the electrical behavior of the half-bridge module is well documented. For instance, the impacts that the parasitics and device characteristics have on the switching dynamics and overall behavior of the module are well known [109]. Having a good grasp on the mechanisms that contribute to the overall performance of the module is critical in the analysis and evaluation of the performance of the devices.

Due to the incredibly flat valance band Ga$_2$O$_3$, the implantation of shallow acceptors has not yet been demonstrated [16]. As such, the p–n junction necessary for switching devices is much harder to achieve; it instead relies on either ionized deep acceptor traps (e.g. nitrogen) or other WBG p-type materials (e.g., NiO, PtO, etc.) to enable switching [15] [110]. As this technology is quite complex and still immature, no switching Ga$_2$O$_3$ devices were available to us at this time and a high-temperature stable alternative was necessary. While the industry standard, SiC MOSFETs degrade significantly at high-temperatures, failing within 132 hours under high-temperature reverse bias (HTRB) testing at 250 °C and 80% breakdown voltage [12]. HTRB testing for 600-V SiC vertical-channel junction field effect transistors (JFET) has shown stable drain and gate leakage currents up to 1000 hours at 200 °C and 80% breakdown voltage [111], and threshold voltage stability up to 525 °C [112]. Therefore, the final topology will be a half-
bridge employing SiC JFETs as the high-temperature switch and Ga$_2$O$_3$ free-wheeling diodes, as shown in Figure 21 below.

![Figure 21. Half-bridge topology with SiC JFETS](image)

The JFET selected for use is the \textit{UF3N120140} 1200 V, 14 A, $R_{DS-ON}$ of 142 mΩ, SiC normally-on JFET from United SiC. This is quite a small die, which can help to increase overall power density while still exhibiting superior high-temperature characteristics when compared to its MOSFET counterparts. The dimensions of the die can be seen in Figure 22, with a thickness of 150 µm.
The Ga$_2$O$_3$ free-wheeling diodes used in the design process were developed internally to the Virginia Tech Center for Power Electronics Systems (CPES). These 600 V SBDs are a result of some novel NiO junction termination extension (JTE) edge termination work, detailed in [114]. The final device dimensions are 5 mm x 5 mm die with a thickness of 630 µm and an anode area of 3 mm x 3 mm. This device will be discussed in further detail in the subsequent section. Lastly, the SiC diode used for comparison is the CPW4-1200-S020B SBD from Cree. This 1200 V, 20 A device was the closest in area and anode size, 3.08 mm x 3.08 mm and 2.51 mm x 2.51 mm respectively, to the Ga$_2$O$_3$ used and is commercially available.

### 5.3 Electro-thermal Device Modeling

To reiterate, the low thermal conductivity and high electric field of Ga$_2$O$_3$ power devices can cause large heat fluxes within the devices, potentially leading to hot-spots within the device and in turn local thermal runaway [15]. This exacerbates the need for design tools that can accurately observe the thermal interactions in the device(s) and package, as well as the electrical performance of the device(s). As such, the co-design tool described in Chapter 4 was utilized to evaluate the packaging configuration and the electric field control for the Ga$_2$O$_3$ diodes, in order to design for favorable thermal and electrical performance of the devices and in turn the module.
as a whole. The final device design utilized for the module, as described in [114], is shown below.

Figure 23. Ga$_2$O$_3$ SBD with novel NiO junction termination extension

5.3.1. Bottom-side versus Junction-side Cooling

Between the current thickness of Ga$_2$O$_3$ power devices in tandem with the low thermal conductivity, bottom-side cooled configurations that rely on the bulk substrate of the device for heat extraction are ineffective [15]. Therefore, junction-side cooling should be employed in order to minimize the effect of the device on the overall $R_{th-j-c}$. A base case utilizing the same load and boundary conditions from Chapter 4 (10 W power loss and a 1,000 W/m$^2$K convection coefficient) was utilized to compare the effectiveness of TSC for SiC and Ga$_2$O$_3$ power devices. As can be seen in Figure 23, not only does junction-side cooling reduce the observed $T_j$ of the Ga$_2$O$_3$ diode by 23%, but also puts it within 1.5% of a SiC diode of the same dimensions, given the same cooling configuration. In addition, the thermal distributions in both cases (and also for the TCAD models) were almost identical between the SiC and Ga$_2$O$_3$ diodes, suggesting that
with a TSC configuration, the effects of the low thermal conductivity of Ga$_2$O$_3$ power devices is largely mitigated.

![Image of SiC and Ga$_2$O$_3$ diodes with different cooling configurations](image)

**Figure 24. Bottom-side cooled versus junction-side cooled SiC and Ga$_2$O$_3$ diodes**

### 5.3.2 Interposer for Electric Field Control

The JTE of the device poses an interesting challenge when managing the electric field within the package. If no interposer is present at the anode of the device, a triple point is formed between the edge termination, Ga$_2$O$_3$ epi-layer, and the encapsulation material (here modeled as a silicone gel). This results in a peak electric field of 12.9 kV/mm inside the encapsulant, which is higher than the PDIV and breakdown strength of any of the tested encapsulation materials when they are exposed to elevated temperatures [81].
Figure 25. Electric field distribution of device without interposer

The addition of an interposer extends the potential seen at the anode of the device, and in turn moves the triple point between two mesas of the edge termination and the Ga$_2$O$_3$ epi-layer. This significantly reduces the peak electric field to 3.5 kV/mm, which is contained inside the epi-layer of the device; only 1.6 kV/mm is observed in the encapsulation material, which is within the bounds prescribed by the evaluated encapsulation materials.

Figure 26. Electric field distribution of device with interposer
The addition of the post results in an additional thermal resistance along the $R_{th\ j-c}$ path. In this case, a Mo post was selected due to its CTE ($4.8 \times 10^{-6} / \text{K}$), which is close to that of Ga$_2$O$_3$ ($3.7 \times 10^{-6} / \text{K}$). Figure 27 shows that while the addition of a post slightly increases $T_j$ (2-5% for a 0.25 mm - 1 mm tall post), it is still a preferable cooling solution compared to the 16% higher $T_j$ observed in the BSC configuration.

(a)

![5 mm Die](5 mm Die)

![3 mm Anode](3 mm Anode)

![2.5 mm Post](2.5 mm Post)

(b)

Figure 27. (a) Die and post structure used in simulation (b) Thermal impact on post height
5.4. Package Thermal Design

Now that the required $\text{Ga}_2\text{O}_3$ device-level thermal and electric field management techniques are established, the full package design can begin. Based on the material survey and encapsulation investigation, three initial decisions can be made. First, since sintered nano-Ag has been demonstrated to maintain high-shear strength when exposed to temperatures up to 600 °C, it was selected for use as the die attach material [79]. The chosen sinter was a paste from NBE Tech, as it is screen printable and fabricated and supplied by a fellow member of CPES.

Second, through the encapsulation investigation and evaluation conducted in Chapter 3, the epoxy resin Durapot 863 was selected due to its adequate PDIV (4.5 kV) and dielectric breakdown strength with thermal aging (6.5 kV). In addition, the high glass transition temperature of 315 °C and a CTE of $3.4 \times 10^{-6} / \text{K}$ that is well matched to that of $\text{Ga}_2\text{O}_3$ makes it a suitable candidate for both the temperature range, as well as a minimization of the CTE mismatch that may contribute to heightened thermo-mechanical stresses [115]. Recent studies have suggested that using materials of a higher elastic modulus, between 4 GPa - 10 GPa, can be beneficial in increasing the reliability of TSC and DSC packaging configurations, as they can better distribute thermo-mechanical stresses [87] [88]. So, with an estimated elastic modulus of ~ 4 GPa for this inorganic/organic epoxy resin compound, it should help further reduce the thermo-mechanical stresses associated with high-temperature operation.

Lastly, 0.5 mm tall Mo posts were selected as the interposer material for the $\text{Ga}_2\text{O}_3$ diodes, due to their minimal impact on the thermal performance in combination with a CTE of $4.8 \times 10^{-6} / \text{K}$; this is close to that of $\text{Ga}_2\text{O}_3$ and helps to minimize the CTE mismatch within the package. A footprint of 2.5 mm x 2.5 mm will be utilized, as it can be adhered to the anode area of both the $\text{Ga}_2\text{O}_3$ and SiC diodes without infringing on the passivation of the device. Now that
the device, die attach, encapsulation, and interposer materials and dimensions have been
identified, the full package thermal design can begin.

5.4.1 Device Spacing

As this package is to serve as an evaluation platform for the high-temperature capability
of Ga$_2$O$_3$, the best chance for thermal and in turn electrical performance must be given to each
device. Thermal coupling between devices in a multi-chip module can lead to a rise in $T_j$ in each
device that is not attributed to its associated self-heating, and the thermal performance of an
individual device would be affected and difficult to track [116]. As such, it is desirable to
minimize or eliminate thermal coupling in the package, such that the high-temperature
performance of the Ga$_2$O$_3$ devices can be tracked without the impacts of the self-heating of the
other devices.

A commonly used 45° heat-spreading angle can be used to estimate the distance required
between the devices. With a heat dissipation area of 2.5 mm x 2.5 mm for the Ga$_2$O$_3$ devices,
dictated by the post area and an area of 1.6 mm x 1.8 mm for the SiC devices, we can calculate
that for a common substrate thickness of 1.5 mm, ~10 mm spacing must be maintained between
the devices to avoid thermal coupling. In addition, this calculation reveals that a minimum radius
of 10 mm from the heat dissipation area will be necessary to provide optimal cooling. Figure 28
shows simulation validation of these calculations using a nominal 10 W loss on each device on a
30 x 30 mm, 1.5 mm thick copper substrate and a convection cooling coefficient of 1,000
W/m$^2$K. The location of the devices was swept diagonally inwards and as anticipated, the
spacing of 10 mm from the outside edge and 10 mm between the active area of the devices
provided the best thermal performance overall.
Figure 28. (a) Thermal coupling sweep performed (b) Thermal results of device spacing
While this spacing provides optimal thermal performance, it should be noted that this will lead to longer interconnects that will contribute to heightened parasitic inductances within the module. This tradeoff will be evaluated and strategies for mitigation will be explored in a subsequent section.

5.4.2. Substrate Evaluation

When selecting a substrate material, three main factors must be considered. First is the effective heat extraction provided, determining whether or not the safe operating temperature of the devices can be achieved for a given cooling configuration. Second is whether or not electrical isolation of the package is necessary, and what magnitude of insulation is necessary for the application. Last is the overall cost of the substrate. With the low-cost potential of Ga\textsubscript{2}O\textsubscript{3} (due to its ability to be grown through an EFG process) [39], it is desirable to keep packaging solutions at a lower cost to further incentivize commercial adoption.

Keeping with a low-cost approach, a Cu leadframe commonly used in inexpensive IC packaging was compared with an Al\textsubscript{2}O\textsubscript{3} DBC, one of the cheapest available metal/ceramic bonded substrate materials. It should be noted that the leadframe requires an insulating thermal interface material (TIM) that exhibits a low thermal conductivity, while the DBC is naturally isolated so an electrically conductive TIM that also has a higher thermal conductivity can be used. The effectiveness of their cooling was evaluated by sweeping the convection coefficient from 100 - of 1,000 W/m\textsuperscript{2}K. The spacing of the devices and area of the substrate from the previous section is maintained, while the loss values are ascertained from a 100 kHz buck converter operation (a typical use case for a half-bridge module). The simulation parameters and results can be seen in Table XV and Figure 29, respectively.
Table XV. Simulation parameters for substrate evaluation

<table>
<thead>
<tr>
<th>Test Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>JFET Loss</td>
<td>25 W</td>
</tr>
<tr>
<td>Diode Loss</td>
<td>10 W</td>
</tr>
<tr>
<td>Leadframe thickness</td>
<td>1.6mm</td>
</tr>
<tr>
<td>Ag Sinter die attach thickness</td>
<td>0.05 mm</td>
</tr>
<tr>
<td>Insulating TIM</td>
<td></td>
</tr>
<tr>
<td>Thickness/Thermal Conductivity</td>
<td>0.25mm/ 0.9W/mK</td>
</tr>
<tr>
<td>DBC Thickness (Cu/Al₂O₃/Cu)</td>
<td>0.305mm/ 0.635mm/0.305mm</td>
</tr>
<tr>
<td>Conductive TIM</td>
<td></td>
</tr>
<tr>
<td>Thickness/Thermal Conductivity</td>
<td>0.5mm/ 4.9W/mK</td>
</tr>
</tbody>
</table>

Figure 29. Convection coefficient vs. temperature for a Cu leadframe and an Al₂O₃ DBC
The thickness of the leadframe was selected because it was the minimum thickness available for laser cut substrates with the required 1 mm gap for isolation between conducting traces (discussed in a later section). As can be seen, while the average and maximum temperatures converge at higher cooling magnitudes, the leadframe actually outperforms the DBC up to that point, exhibiting a 5-10% lower peak temperature between 100-500 W/m²K (a typical cooling for a heat sink/fan combination). In addition, with the maximum operating voltage of the system expected at only 1.2 kV, an insulating TIM should provide sufficient isolation. It should be noted that these substrates must also be Ag-plated with a diffusion barrier, such as Ni, in order to facilitate sintering and prevent oxidation.

The cost of the substrate is the final consideration to be made in the selection process. For low volume manufacturing and quick prototyping, the leadframe is the clear winner at about 10% of the cost of the DBC [117]. As such, a leadframe with a thickness of 1.6 mm was decided upon and utilized for the module design and fabrication.

5.4.3 Interconnect Evaluation

While TSC the Ga₂O₃ has been shown as an effective way of reducing the junction temperature of the device, further improvements can be made by implementing new interconnect methods. Planar interconnects like the ones discussed in Chapter 2 can provide higher reliability, lower $R_{th,j-c}$, and lower parasitic inductances compared to conventionally used wire-bonds [118]. To keep with a low-cost approach, Cu clips were implemented as an inexpensive option to implement the planar interconnects to the Ga₂O₃ diodes.

To evaluate the thermal behavior of the clips, the same layout and simulation parameters as the substrate evaluation section were utilized with a convection coefficient of 300 W/m²K.
The inclusion of this additional copper in the package assisted in heat dissipation, lowering the maximum temperature observed in the package by ~4%. In addition, the clips assisted in reducing the temperature gradient within the package, leading to a 22% reduction in maximum principal stress and a 2.5% reduction in maximum shear stress seen in the package. This reduction in stresses may be of particular importance due to the quasi-2D nature of Ga$_2$O$_3$, which makes it very brittle.

![Thermal performance of (a) wire-bond package (b) package using Cu clips](image)

Figure 30. Thermal performance of (a) wire-bond package (b) package using Cu clips
Table XVI. Wire-bonds versus Cu clips maximum principal and shear stress results

<table>
<thead>
<tr>
<th>Max Principal Stress WB</th>
<th>Max Principal Stress CuClip</th>
<th>Percent Difference</th>
<th>Max Shear Stress WB (location)</th>
<th>Max Shear Stress CuClip (location)</th>
<th>Percent Difference</th>
</tr>
</thead>
<tbody>
<tr>
<td>43.7 MPa (Diode 1 post attach)</td>
<td>33.9 MPa (JFET 1 die attach)</td>
<td>22% decrease</td>
<td>22.4 MPa (Diode 1 post attach)</td>
<td>21.9 MPa (JFET 1 die attach)</td>
<td>2.5% lower</td>
</tr>
</tbody>
</table>

5.4.4 Cooling Requirements

The final consideration in the thermal design was to establish secondary cooling needs and select an appropriate method to achieve the thermal design targets. This was done by performing another HTC sweep of the full package design with the target of a maximum temperature of 300℃. As can be seen in Figure 31, this target is met with a convection coefficient of ~150 W/m²K. This can be easily achieved with a common aluminum-finned heat sink and a fan, achieving upwards of 500 W/m²K at low cost [119].
5.5 Electrical Analysis

Thermal performance has been seen as the primary bottleneck to the adoption of Ga$_2$O$_3$ devices, and as such a rigorous thermal design was performed in order to extract adequate heat from the devices to meet maximum temperature targets. However, the long spacing introduces heightened parasitic inductances and resistances that must be accounted for and minimized wherever possible. In addition, adequate electric field control and electrical isolation is paramount to safe and reliable operation of the power module.

5.5.1 Parasitic Design

Electrical parasitics, dominated primarily by the inductances and resistances of the interconnects and terminals of a package, can have adverse impacts on the electrical performance of a module. As a rule of thumb, it is good to keep the power loop inductances as low as possible.
to reduce switching losses and avoid voltage overshoots [120]. In addition, the inductances seen in the gate loop can lead to a highly conducted electromagnetic interference (EMI), causing false turn-ons as well as limiting the switching speeds of a module [121]. It is also best practice to keep conductor lengths to a minimum, as the parasitic resistances contribute to higher conduction losses and a further reduction of efficiency. To minimize the length of the interconnects while keeping the maximum copper for thermal spreading and providing isolation between the different electrical potentials of the module, the layout seen in Figure 32 was developed. In addition, a quad flat pack no-lead (QFN) structure was implemented to facilitate TSC while keeping the terminal length to a minimum to further reduce parasitics. Lastly, the inclusion of a kelvin source (KS) gives a parallel path for the gate-loop, reducing the overall parasitic resistance and inductances.

Figure 32. Final module layout
In order to justify the increase in fabrication complexity associated with using copper clips, ANSYS Electronics Desktop was used to extract the parasitics of both a module that used all wire bonding, as well as one with copper clips. Figure 33 (a) shows a reduction of 10.5% in power loop 1 inductance; Figure 33 (b) shows a reduction of 8.5% in power loop 2 inductance. Altogether a combined power loop inductance of 4.2 nH is achieved, which is nearly 10 times lower than an equivalent TO-247 packaged half-bridge [122]. This shows that even with several wire bonds in parallel, planar interconnects of the same length have less parasitic contribution.
5.5.2 Passivation and Electric Field Control

With a maximum operating voltage of 1.2 kV, proper control of the electric field must be made to avoid PDIV and breakdown internally to the module, as well as arcing and shorts externally. There are three areas that must be addressed:

1. Internal conductors of different potentials.
2. The exposed back-side of the power module.
3. The external potentials exposed by the cutting of the leadframe/encapsulation material.

The internal field management is the most straightforward. With a PDIV of 4.5 kV exhibited over the 1 mm gap evaluated experimentally at our expected operating temperature [81], the epoxy resin should provide adequate isolation between the different potentials even in
the case of overvoltage events as long as this spacing is maintained. In addition, rounding corners helps alleviate electric field crowding seen in sharp corners, as well as reducing the overall magnitude [123]. This technique has the added benefit of thermo-mechanical relief, avoiding corner stresses that can represent areas of high stress and strain [62].

For the exposed back-side of the power module, a gap filler pad will be employed similarly to [124]. This will serve two purposes; first, it will provide adequate isolation between the exposed conductive traces and the outside environment. Second, it will serve as a thermal interface material between the module and the heat sink to ensure that good thermal contact is made.

Finally, per IEC/ISO 60601, the minimum creepage and clearance distances between exposed conductors at a 1.2 kV potential difference in the air is 3 mm [125]. As such, the leadframe was designed to maintain this 3 mm spacing after the leadframe is cut away. If any unwanted arcing occurs, Kapton tape can be utilized for passivation, as it is not on the primary heat flow path and will not have any impact on module performance.
Chapter 6. Module Fabrication and Test Plan

Now that the thermal, electrical, and thermo-mechanical design has been completed, the final module design can be seen in Figure 34 below.

![Final module design](image)

Figure 34. Final module design (a) Bottom view (b) Affixed to PCB
6.1 Fabrication Procedure and Evaluation

The fabrication of the module will follow the assembly steps outlined in Figure 35. The materials used are the same as those identified in Chapter 5. Screen printing will be utilized to form a sinter layer of 0.05 mm, used for the clip and die attachments. Modules with SiC diodes will also be fabricated for comparison.

![Module fabrication process](image)

**Figure 35. Module fabrication process**

Mechanical tests will be utilized to evaluate the success and quality of the package. Shear tests to establish the maximum shear strength of each sinter bond will be performed and compared to the shear stress seen in the thermo-mechanical models. Also, wire-bond pull tests will be performed to ensure that proper ultra-sonic bonds are being made between the devices and the substrates.
6.2 Testing Procedure and Rationale

This module will serve as a platform to evaluate the high-temperature capabilities of Ga$_2$O$_3$ diodes against SOA SiC diodes. First, static characterization will be performed from 25 °C - 300 °C using a Tektronix 371b curve tracer to establish the relationship between the on-resistance and temperature for the packaged diodes. A positive temperature coefficient (PTC) heating element will be used to heat the package, and pulsed measurements will be taken every 25 °C and the resulting IV-curves recorded.

To characterize the switching performance of the devices, a heated double pulse test (DPT) will be performed. Using a gate drive design adapted from [126], LabView, and a function generator, DPTs of various load currents, dc voltages, and output inductances can be easily run. The configuration shown in Figure 36 will permit for the safe heating of the module and testing over the same intervals as the static testing will be performed. The switching losses can be extracted for each heating interval and compared between the Ga$_2$O$_3$ and SiC devices. This testing will highlight the high-temperature capabilities and degradation of the devices.

Figure 36. Heated DPT setup
Chapter 7. Summary, Conclusions, and Future Work

7.1 Summary and Conclusions

Power electronic systems and components that can operate in environments with ambient temperatures exceeding 250 °C are needed for innovation in automotive, aerospace, and downhole applications. The UWBG of Ga$_2$O$_3$ allows it to achieve a nearly $10^{33}$ lower intrinsic carrier concentration than Si, permitting Ga$_2$O$_3$ devices to theoretically operate at significantly higher temperatures. However, the thermal management of Ga$_2$O$_3$ power devices is especially difficult due to their low thermal conductivity of $11\text{–}27 \frac{W}{mk}$. As such, rigorous design is required to unlock the high-temperature potential of Ga$_2$O$_3$ power devices. All of the work in this thesis was performed with the end objective of the modeling, design, fabrication, and evaluation of a 300 °C, 1.2 kV half-bridge power module utilizing Ga$_2$O$_3$ diodes to assess their thermal and electrical performance.

An extensive literature review was conducted surrounding packaging strategies for high-temperature operation and methodologies for improved heat extraction from the Ga$_2$O$_3$ devices. Conventionally used polymeric encapsulation materials were identified as the most immediate limitation to the reliable high-temperature operation of power modules. A thorough survey of high-temperature encapsulation candidates was performed, and six encapsulation materials were evaluated experimentally for >250 °C operation. After soaking at 250 °C for 100 hours in air, an inorganic/organic epoxy resin showed both stable PDIV and an electrical breakdown strength of 4.5 kV and 6.5 kV respectively, which in combination with its glass transition temperature of 315 °C made it an excellent candidate for high-temperature module applications.

The low thermal conductivity of Ga$_2$O$_3$ can cause large heat fluxes within the devices, potentially leading to hot spots within the device, and in turn local thermal runaway. As such, it
is paramount to have an accurate methodology for modeling the heat interactions between the device and package, as well as the temperature-dependent electrical performance of the device. A device/package co-design framework utilizing Silvaco TCAD for device-level electrical simulations and ANSYS workbench is proposed as an iterative design tool that permits for the accurate and efficient modeling of a device’s physics level electrical performance, as well as the thermal and thermo-mechanical ramifications on the package as a whole. This was used to demonstrate device dimension modifications that can help to reduce the junction temperature of a packaged device by up to 84%. In addition, this platform was utilized to show that by junction-side cooling, a Ga₂O₃ device thermal performance within 1.5% of SiC can be achieved with the same device dimensions and power loss.

Finally, leveraging the co-design platform and the material review/evaluation a 300 °C, 1.2 kV half-bridge power module utilizing Ga₂O₃ diodes and SiC JFETs was designed. This QFN-style package utilizes copper clips for a low power loop inductance of 4 nH. The diodes utilize a TSC configuration for good thermal performance, and the design permits for a 1:1 swap between the Ga₂O₃ diodes and SiC diodes to allow for fair comparison. A method for the static and dynamic characterization of the module both at room temperature and elevated temperatures to evaluate the high-temperature capabilities of Ga₂O₃ devices was also proposed.

7.2 Future Work

As a continuation of the encapsulation work, it would be meaningful to extend the temperature range of the thermal soaks (and/or for longer thermal soak times) to help to establish the high-temperature reliability of the selected materials. In addition, performing the PDIV
testing at elevated temperatures and over repeated partial discharge events should garner a clearer image of the electrical stability of these materials at high-temperature. To better understand the mechanical resilience of the materials, thermal gravimetric analysis could be implemented to establish the decomposition point of each material to observe the upper limits of potential operating temperatures. Finally, testing the adhesion strength between the encapsulation material and the substrate through the use of shear tests with thermal aging intervals could be an effective way to establish the high-temperature mechanical reliability of the encapsulation/substrate interface.

Experimental validation of the device/package co-design framework is necessary to evaluate its efficacy as a design tool. This can be done by using a thermal impedance analyzer that can track a temperature sensitive electrical parameter in a given packaging configuration and provide the accurate electrical and thermal performance of a packaged device. Additionally, the high-temperature capability of Ga$_2$O$_3$ must be evaluated through fabrication, static, and dynamic characterization of the proposed module. Lastly, the high-temperature reliability of this Ga$_2$O$_3$-based module must be evaluated through the use of thermal- and power-cycling to expose any potential failure modes and refine the high-temperature packaging design.
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