

Packaging of a High Power Density Point of Load Converter

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ABSTRACT

Due to the power requirements for today's microprocessors, point of load converter packaging is becoming an important issue. Traditional thermal management techniques involved in removing heat from a printed circuit board are being tested as today's technologies require small footprint and volume from all electrical systems. While heat sinks are traditionally used to spread heat, ceramic substrates are gaining in popularity for their superior thermal qualities which can dissipate heat without the use of a heat sink. 3D integration techniques are needed to realize a solution that incorporates the active and components together. The objective of this research is to explore the packaging of a high current, high power density, high frequency DC/DC converter using ceramic substrates to create a low profile converter to meet the needs of current technologies.

One issue with current converters is the large volume of the passive components. Increasing the switching frequency to the megahertz range is one way to reduce to volume of these components. The other way is to fundamentally change the way these inductors are designed. This work will explore the use of low temperature co-fired ceramic (LTCC) tapes in the magnetic design to allow a low profile planar inductor to be used as a substrate. LTCC tapes have excellent properties in the 1-10 MHz range that allow for a high permeability, low loss solution. These tapes are co-fired with a silver paste as the conductor. This paper looks at ways to reduce dc resistance in the inductor design through packaging methods which in turn allow for

higher current operation and better heavy load efficiency. Fundamental limits for LTCC technologies are pushed past their limits during this work. This work also explores fabrication of LTCC inductors using two theoretical ideas: vertical flux and lateral flux. Issues are presented and methods are conceived for both types of designs. The lateral flux inductor gives much better inductance density which results in a much thinner design.

It is found that the active devices must be shielded from the magnetic substrate interference so active layer designs are discussed. Alumina and Aluminum Nitride substrates are used to form a complete 3D integration scheme that gives excellent thermal management even in natural convection. This work discusses the use of a stacked power technique which embeds the devices in the substrate to give double sided cooling capabilities. This fabrication goes away from traditional photoresist and solder-masking techniques and simplifies the entire process so that it can be transferred to industry. Time consuming sputtering and electroplating processes are removed and replaced by a direct bonded copper substrate which can have up to 8 mil thick copper layers allowing for even greater thermal capability in the substrate. The result is small footprint and volume with a power density 3X greater than any commercial product with comparable output currents. A two phase coupled inductor version using stacked power is also presented to achieve even higher power density.

As better device technologies come to the marketplace, higher power density designs can be achieved. This paper will introduce a 3D integration design that includes the use of Gallium Nitride devices. Gallium Nitride is rapidly becoming the popular device for high frequency designs due to its high electron mobility properties compared to silicon. This allows for lower switching losses and thus better thermal characteristics at high frequency. The knowledge learned from the stacked power processes gives insight into creating a small footprint, high

current ceramic substrate design. A 3D integrated design is presented using GaN devices along with a lateral flux inductor. Shielded and Non-Shielded power loop designs are compared to show the effect on overall converter efficiency. Thermal designs and comparisons to PCB are made using thermal imaging. The result is a footprint reduction of 40% from previous designs and power densities reaching close to 900W/in³.

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I would also like to thank the staff at CPES. Dan Huff helped me learn some of the intricate details of electronic packaging in the packaging lab. There are some wonderful people who I will also mention: Teresa Shaw, who seems to have endless energy and passion for her job; Linda Long, who has helped me a lot with financial details for my studies and my position; Trish Rose, my office neighbor for a few years, who I almost consider family at this point; Marianne Hawthorne, who has helped me with lots of paperwork and scheduling. I have also

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To My Wife Amy

To My Daughter Kelly

To My Son Joel

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Disclaimer

This work was done in conjunction with multiple doctorate students at the Center for Power Electronic Systems as my job being a research associate. It is necessary to provide some background information from other authors to help lay the groundwork for this work so it is in context. Most of the paper is work that is done exclusively by the author or as part of a project team. Distinctions will be made in section headings as well as including traditional references to the work. References will also be included in captions for images. While this is not a usual practice in these types of documents, clear distinctions must be made to avoid any plagiarism.

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Chapter 1: Introduction

1.1 Background of Point of Load Converters

Point of load converters are voltage supplies that are placed close to the load and provide low voltage and high current to microprocessors in computers and hand held devices. As new generations of microprocessors have increased power demands, the industry has had to develop new methods in circuit design, integration, and packaging to keep pace. In 1997, CPES proposed a multiphase voltage regulator module in response to Intel's request [1]-[3]. This module was design to improve efficiency, transient performance, and power density. Today every processor is powered by this type of multi-phase converter and has increased from 1 phase ten years ago to 10 phases today providing up to 180A. To keep the efficiency high, the current converters operate at lower switching frequencies ranging from 200-600 kHz. The drawback is the passive components are large and bulky. Figure 1.1 shows how much footprint the point of load components can take up on a computer motherboard [4].

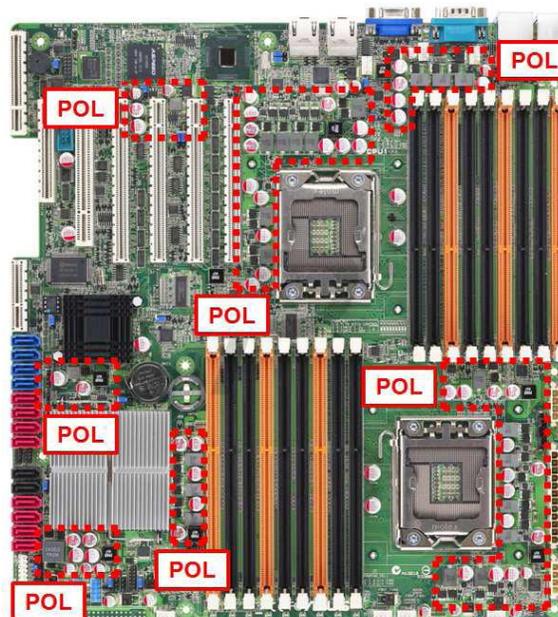


Figure 1.1 POL Converters occupy 30% of a server motherboard [4].

In response to the problem, industry leaders have proposed using power plug in modules to replace the embedded power layouts in the board itself. This allows the designers to choose an optimized power block for the power stage while leaving the control and output capacitor on the board. Board footprint can be dramatically reduced, while giving the flexibility for design by choosing power modules from a wide variety of manufacturers based on the requirements of the processor.

With this shift in the thinking, it brings about more challenges in the design of the power modules. While the increase in switching frequency reduces the passive components, it poses problems in the electronic packaging of the converter. The main goal is to consume less board footprint and have high power density which brings thermal management to the forefront of packaging research. To meet the new requirements, improved circuit substrates, better device technology, parasitic inductance reduction through circuit layout, and magnetic materials are the main concepts that will be looked at in future generations of power modules.

1.2 Overview of Electronic Packaging

While electronic packaging has many levels of interconnect, from chip level to multi system integration, concentration in this paper will be on the first (chip or component level) and second (board level) levels in the packaging hierarchy. With the increase in switching frequency at the forefront of industry, device improvement has been a driving force. Power device technology has recently gone from a Silicon dominated industry to III-IV compound semiconductors such as Silicon Carbide (SiC) and Gallium Nitride (GaN) gaining more traction. Figure 1.2 shows how silicon has reached its theoretical limit and how GaN devices will provide large benefits compared to silicon for the power management industry as the technology matures. GaN based high electron mobility transistors (HEMT) are gaining popularity in high frequency

applications due to better carrier mobility, higher electron velocity, and higher critical field compared to silicon. In fact, GaN device sales are expected to grow by 64% over the next 10 years to almost a 2 billion dollar industry due to the low and medium voltage market penetration [5].

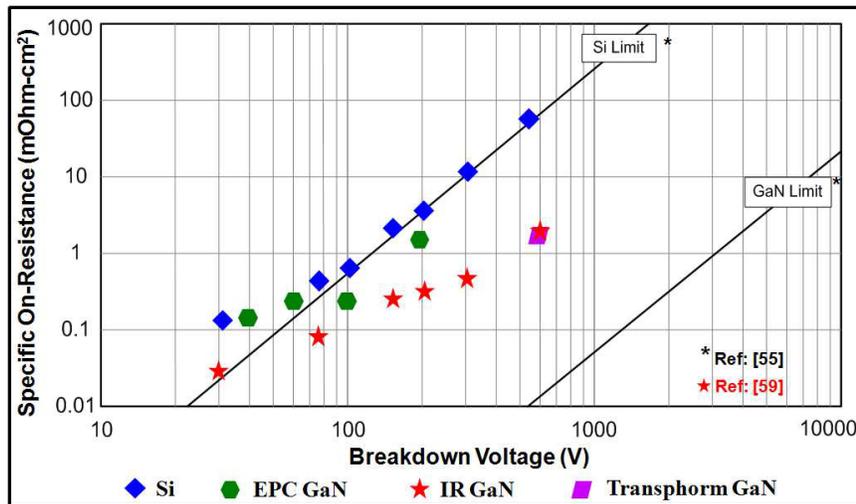


Figure 1.2. Comparison of Specific On Resistance for Si and GaN [6].

In addition to device improvement, attention must be paid to circuit layout and device interconnects if high switching frequency is to be obtained. Most electronic packaging involves wire bonding the device connections to the circuit which introduces large parasitic inductances. As device packaging technology gets better and better, reducing connection parasitic inductances becomes much more important. This paper will also discuss methods of making planar connections to the device rather than using wire bonds.

Thermal management has also become a major concern for packaging engineers today. While power densities have remained low, designs are comfortably in the thermal margin for devices. Many designs also rely on large heat sinks and fans to keep the devices under the maximum junction temperature. With higher switching frequency and higher power density sought after in the industry, even standard printed circuit boards will not be able to keep the

devices underneath their max junction temperatures. Ceramic substrates will have to replace the traditional PCBs if high power density is to be reached. These substrates can effectively spread the heat across the board and reduce the temperature that the device itself sees.

1.2.1 Power Semiconductor Technologies

To keep up with the push for higher switching frequency, the power semiconductor industry has continued to develop new generations of MOSFET technology. The VDMOS, which was commercialized in the 80's and is known for its V- shaped gate region, is generally used for applications with large currents and voltages greater than 30V.

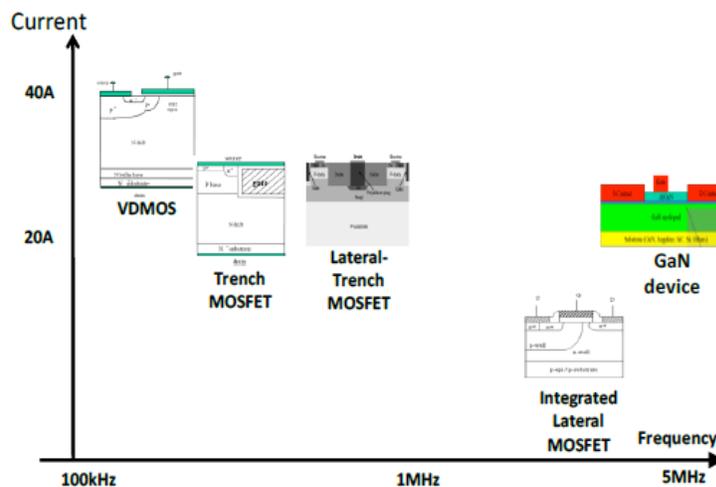


Figure 1.3. Semiconductor Devices showing current vs. frequency [6].

In the 90's, the trench MOSFET was introduced to improve switching speed while reducing on resistance. The trench and lateral trench MOSFETs are widely used in POL applications where the voltage is less than 30V. When the lateral trench device was released in 2008, it was intended to fill the gap between the lateral and trench MOSFETs by taking the best of both. Its figure of merit (FOM) is half of the trench MOSFET at the same current level and is used in the voltage range from 15 to 25V. Once Gallium Nitride devices were released in 2010 by companies such as International Rectifier (IR) and Efficient Power Conversion (EPC), higher switching frequency i.e. 5 MHz was now obtainable. The wide band gap semiconductor

properties improve the switching characteristics while lowering the FOM even in the first generations of devices as shown in Figure 1.4 [6]. This thesis will discuss the use of EPC devices to develop high frequency, high current active layers for POL applications.

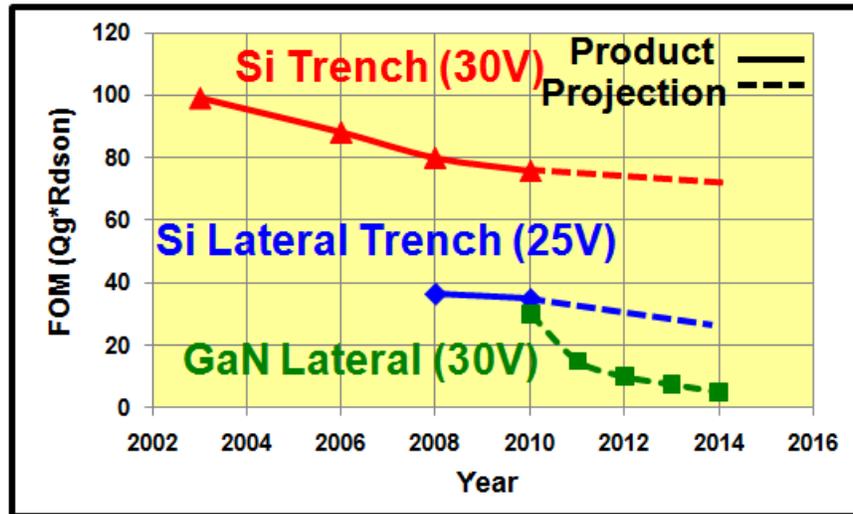


Figure 1.4. FOM for Si and GaN by year [6].

1.2.2 Chip Level Interconnect Technologies

Performance of die technology is important in the power electronics field. But packaging of dies also plays a vital role in how that die performs in circuit. It is known that the package can contribute significant drawbacks to the performance if package parasitics are not limited.

Small outline packages were the first to be used in power applications to connect the trench MOSFET to the board. One example is the SO-8, which provides a small overall thickness because of the minimal standoff, but provides the highest package parasitics because of its use of wire bonding to connect the source and gate to the lead frame. When the LFPACK was introduced, it removed the need for wire bonding by directly soldering the chip to the lead frame on both sides increasing the thermal capability. The package still suffered from high gate and source inductance but dramatically improved upon the SO-8. The orientation of the devices always had the drain connected to the board and the source and gate connected to the lead frame.

The IR DirectFET changed the orientation by flipping the chip, having the source and gate connections connecting down and the drain connected to a lead frame or what they called a “can”, essentially reducing the gate and source parasitics [7]. Figure 1.5 shows the chip interconnect evolution [6].

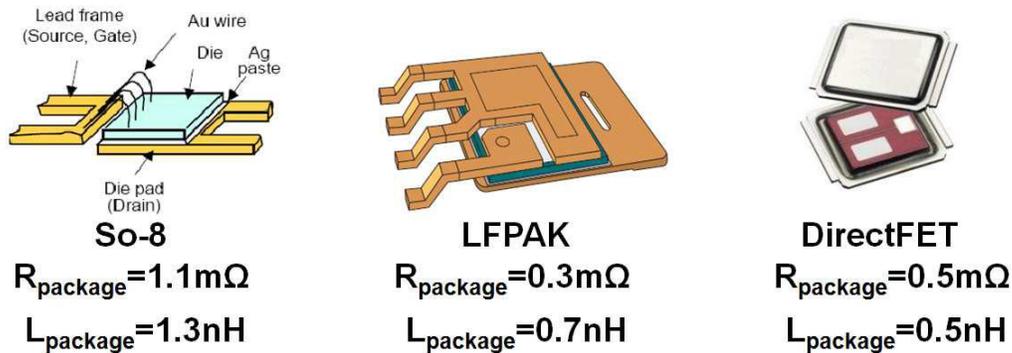
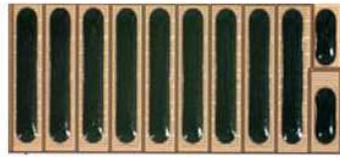


Figure 1.5. Commercial Trench Packaging Techniques for SO-8, LFPACK, and DirectFET [6].

All the devices shown above suffer from the same fate of higher parasitics due to the trench type of die, which puts a limit on how much parasitic reduction can occur. The push for higher frequency also puts a bind on this type of die as parasitics only increase with frequency. This brought a move to a lateral device with all terminations on one side. Fast switching speeds are possible because the electrons can flow from drain to source as soon as the gate opens. There is also no parasitic or body diode from the p to n region, like a trench device, which eliminates reverse recovery loss and reduces switching loss. EPC introduced a Linear Grid Array (LGA) package which interleaves source and drain connections and reduces parasitic inductances. These devices are in an unpackaged form and solder bumped for direct connection to the board. Figure 1.6 shows the solder bumped side of an EPC 1015 or 2015 lead free version.



$$R_{\text{package}}=0.2\text{m}\Omega$$

$$L_{\text{package}}=0.15\text{nH}$$

LGA

Figure 1.6. LGA package and parasitics [6].

GaN devices can offer a 2.5 times reduction in the package resistance and 3.5 times reduction in the package inductance. This can have a significant positive impact on the high frequency characteristics of a converter. The drawback is that the onus falls on the circuit designer who must now improve the layout of the circuit namely keeping the high frequency loop from contributing large inductances which will affect overall efficiency.

1.3 State of the Art POL Modules

In order to better understand how to improve on aspects of commercially available modules, some study was done. There are three types of modules are found on the market that pertains to this research: Discrete, Co-packaged, and Integrated. The discrete modules are generally built from discrete packaged parts found from different manufacturers which suit the circuit layout. These types of modules operate at lower switching frequencies, such as 200-600 kHz, but can handle large currents although the power density is also very low. There are trends that can be seen in industry today. If you want high current modules, then you must tradeoff high power density and use discrete modules. If you want high power density, then you can purchase an integrated module which sacrifices current handling capability. The next section will discuss a co-packaged solution which finds some middle ground between the discrete and integrated versions.

1.3.1 Co-packaged Modules

Since the discrete modules have individually packaged parts, there are high resistances and inductances present in the system. The co-packaged module uses a different approach in that it uses bare dies for the switching and IC components while sticking with discrete passive components. The bare dies have a direct solder connection for the drain to the board and utilize many wire bonds to connect the gate and source pads to the board. The result is the decrease in parasitics which increases the applicable switching frequency up to 1 MHz and decreases the size of the passive components compared to the discrete versions. Figure 1.7 shows an X-ray of a commercial co-packaged module [8]. It can be seen that the inductor volume is still much larger than any other component and is hindering the move to higher power density.

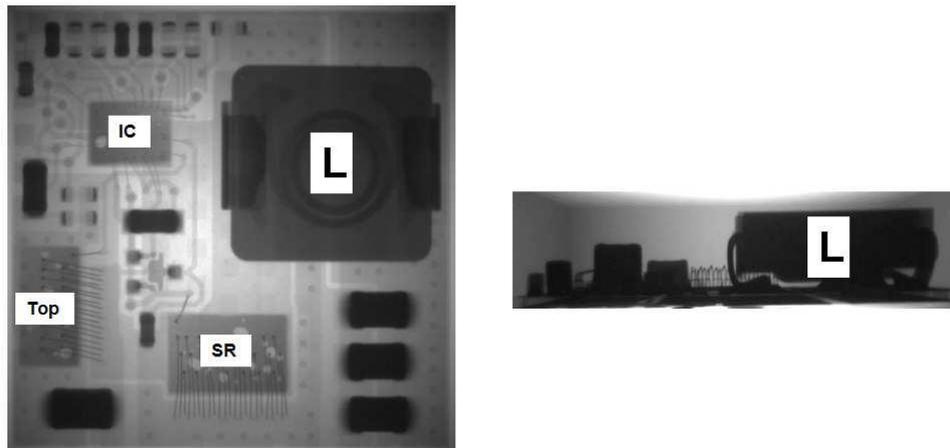


Figure 1.7. Linear Technology's LTM 4601 co-packaged solution. $V_{in}=12V$ $F_s = 800kHz$ $I_o=12A$. Top View (left) Side View (right). Images by author.

The inductor is a multi-turn spiral winding conductor through the two halves of the magnetic core. This limits the current capability of the inductor as the DC resistance is high. The module above has separate dies for the top and SR switches, and the IC. Another version of a co-packaged module monolithically integrates these devices together onto a single chip [9]. This

again reduces the parasitic inductance and allows moving to a higher switching frequency up to 5 MHz. The inductor has the flat copper conductor wrapped around a single piece of magnetic core and uses board traces underneath to complete the loop. But it can be seen that the inductor still dominates the volume and curbs higher power densities.

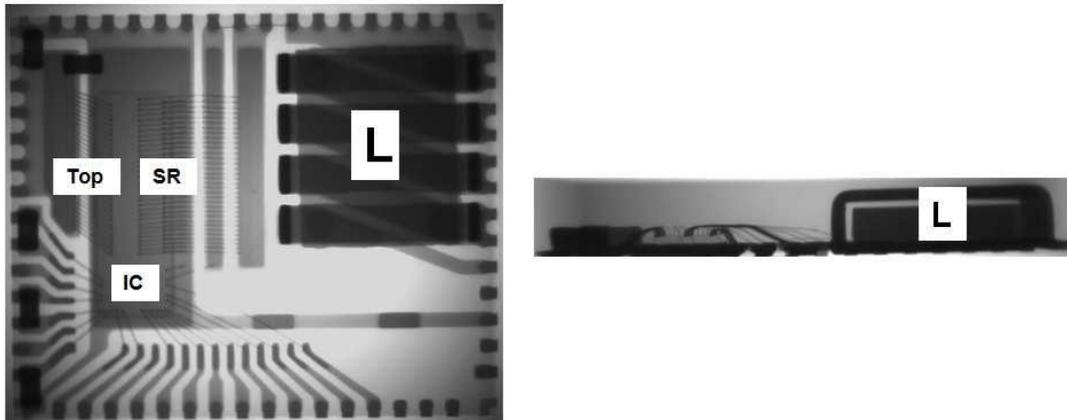


Figure 1.8. Enpirion 5396QI co-packaged solution. $V_{in}=5V$ $F_s=5MHz$ $I_o=9A$. Top View (left) Side View (right). Images by author.

Judging by the above co-packaged modules, there is a clear need to shrink the footprint to increase the power density. One module on the market aims to do this [10]. It stacks the inductor on top of the monolithically integrated drive and switches. But to get the required inductance, the inductor is multi-turn which again limits the output current to around 4-5A.

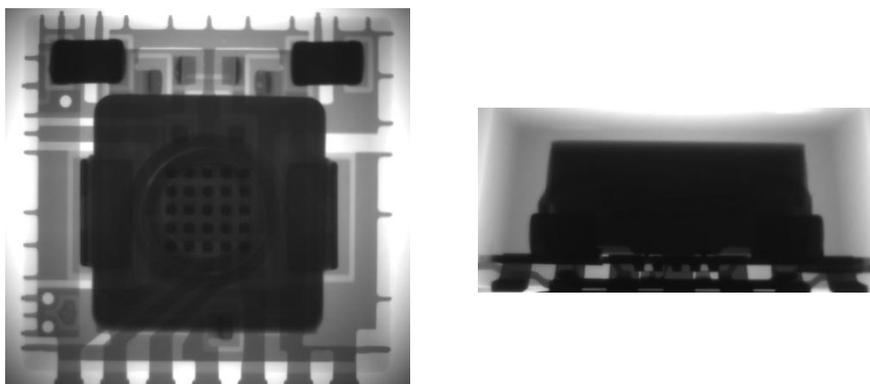


Figure 1.9. National/Texas Instruments LM10505 co-packaged module. $V_{in}=5V$ $F_s=2MHz$ $I_o=4A$. Images by author.

There is a definite tradeoff in output current, switching frequency, and power density. It can be seen that the module must move to an integrated scheme in order to increase all those variables together.

1.3.2 Integrated Modules

The integrated module tries to improve on one aspect that the co-packaged solutions lack – power density. As seen above, the inductor packaged next the chip is limiting the power density of the module due to the footprint. There are examples of integrated modules on the market that offer much better power density [11]. This module mounts the packaged active devices on top of the inductor which dramatically reduces the footprint of the converter. Switching frequency is also higher, reducing the size of the inductor. The module utilizes a LTCC inductor with electroplated terminals for the chip. The large winding resistance effect limits the output current below 1A.

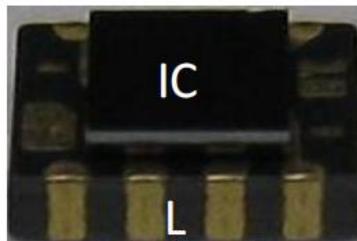


Figure 1.10. National LM3218 Integrated Module. $V_{in}=5V$ $F_s=2MHz$
 $I_o=650mA$ 2uH LTCC Inductor

There are other examples of integrated modules. Enpirion manufactures a line of 4MHz, 5V, low current ($> 2A$) modules that use an integrated inductor [12]. They use an electroplating process with CoNiFeP as the material for the magnetic core. The process wraps the copper conductor around the electroplated core to complete the inductor. It is a thin film process but uses greater than 40 turns for the conductor which limits its current rating.

Fuji also manufactures a line of integrated modules which have an output current of 500mA and integrates a ferrite inductor into the silicon IC [13]. Most integrated modules have a limited output current below 6A but can keep the switching frequency high which increases power density based on smaller passives. The roadmap below shows the general trend of industry and the need to fill the high current, high power density area in the graph. This can only be done by integrated solutions moving towards system on a chip. This research will concentrate in that high current, high power density area by combining active and passive layer packaging techniques to reduce footprint while increasing power density.

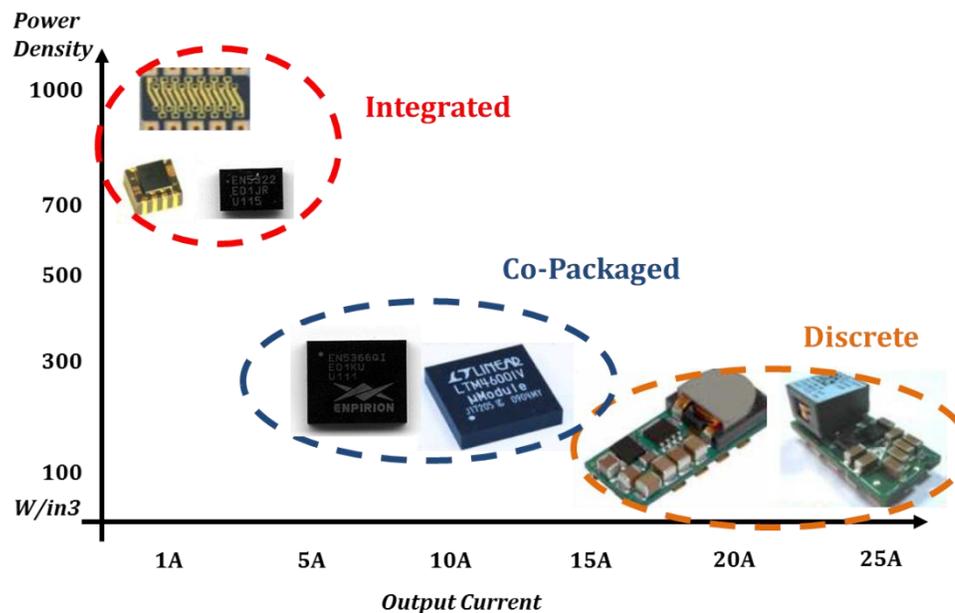


Figure 1.11. Today's POL Products. Images by author.

1.4 State of the Art Magnetic Material

While most of the work being done today is improving device technology, magnetics have become the bottleneck to reaching higher power density and integration. As seen in the previous section, the magnetic components occupy significant footprint. Most of today's inductors are made with iron or ferrite based powders. Materials like MnZn, which was commercialized in the 1930's, are only now reaching their theoretical frequency limits (5MHz).

Magnetic materials are a hot topic as requirements for increased frequency and reduced footprint are being introduced. Frequency introduces the need for low loss materials while a shrinking footprint requires the materials to have higher permeability. This section will look at materials currently being used as well as materials that can be used in the future.

A survey of magnetic materials, by the author, shows that there are a variety of materials being used in commercial power conversion products today. Figure 1.12 shows which materials are being used in actual products and their applicable frequency ranges. There is only one company that is currently producing modules that are greater than 1MHz and utilize MnZn ferrite as its magnetic core. The same company also manufactures modules that utilize an electroplated CoNiFe as its magnetic core (although it is in the low current range $<2A$). It is also a thin film process meaning multiple layers must be built up with insulation between to achieve enough inductance.

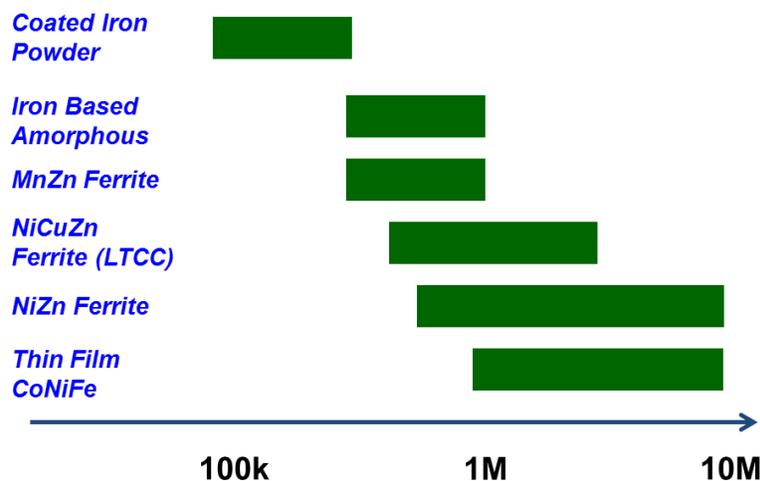


Figure 1.12. Magnetic Materials used in actual power conversion products on the market and emerging technologies. Applicable Frequency Ranges. Image by Author.

Coated Iron Powder and Iron based amorphous powders (containing Si and Cr) are the most widely used magnetic materials on the market today. These powders are cheaper alternatives to the ferrites that are available. The assumption with this graph is that companies

are only producing magnetic materials for the frequency ranges they need. But as switching frequencies are approaching 5 MHz, the need for new materials only becomes that much more important. Shown below is a listing of some suitable candidates for high frequency operation[14].

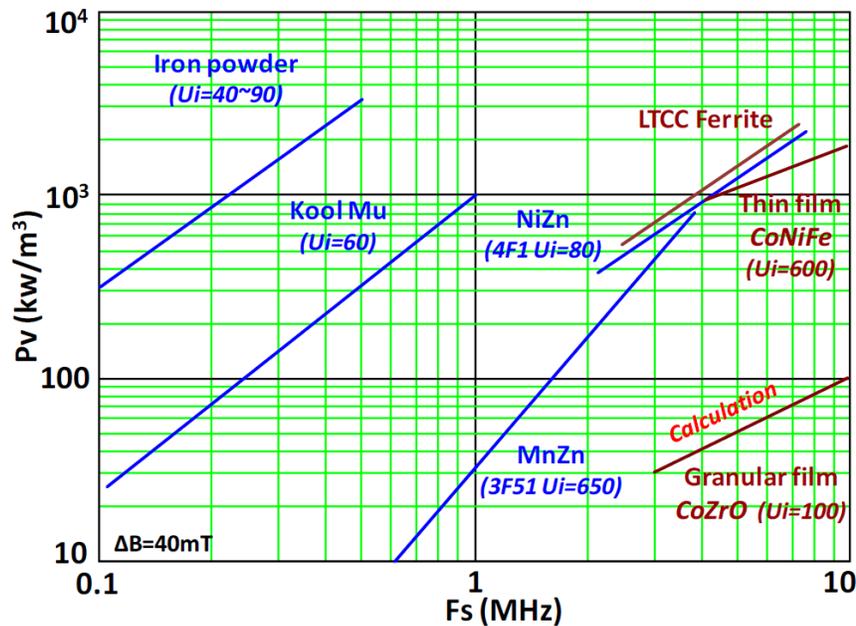


Figure 1.13. Core Loss Density for different materials [14].

Eventually MnZn ferrite must be replaced as its resistivity is not high enough to be suitable at frequencies above 5 MHz. NiZn, LTCC, and Ferrite Polymers seem to be suitable replacements for MnZn. NiZn is manufactured similarly to MnZn in that it uses a high temperature sintering process. NiCuZn is a Low Temperature Co-Fired Ceramic that starts as a green tape and is stacked in layers to form a structure which is then sintered at a slightly lower temperature than NiZn. Ferrite polymers are made similarly to a magnetic green tape but are left in the unsintered state which increases the inherent resistivity and removes the need for high temperature. This process can be included into the traditional PCB process. It lacks the permeability though that the ferrites have due to the magnetic particles being farther apart than

the fully dense ferrite. There are some examples of ferrite polymers being used for integration in power conversion modules [15].

The group at the Philips Company developed a converter in which the ferrite polymer layers that made up the inductor, were embedded into the PCB. This process followed the traditional standards for the PCB process and kept it at low temperature. The inductor was formed by using the MagLam polymer for the magnetic core and the PCB traces for the copper conductor.

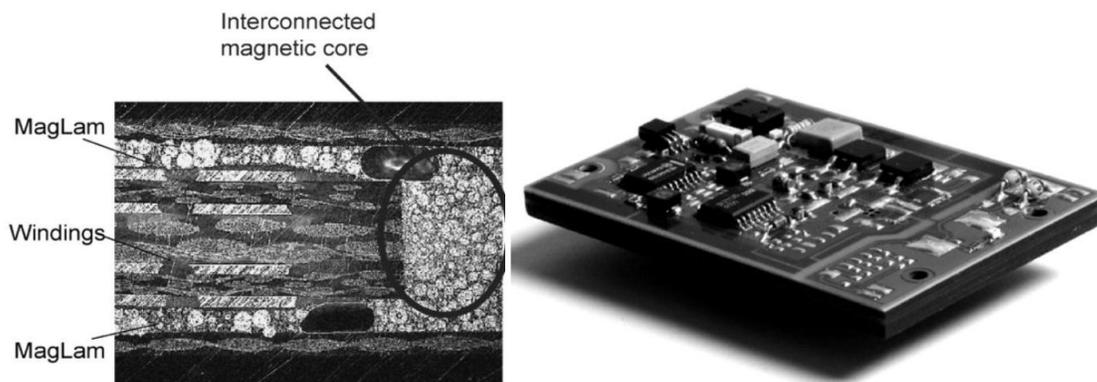


Figure 1.14. Philips Integrated PCB structure. Inductor (Left), PCB (Right) [16].

In summary, the need is present to have a high frequency, high output current material to form an inductor that can also increase the power density of the converter. Our belief at CPES is that a planar LTCC inductor as a magnetic substrate can fulfill all of these requirements.

1.5 Background of CPES 3D integration

The challenge is how to design and fabricate a point of load converter that can give high output current along with high power density. The previous sections presented solutions that either gave high output current or gave high power density. The inductor volume is the bottleneck to achieving both. CPES has worked for many years to develop a converter that uses a planar inductor substrate. This section will introduce some of those developments.

1.5.1 Basic Concept of 3D Integration

In order to maximize the power density of the converter, a 3D integration scheme must be used. The basic concept of the proposed structure is shown in Figure 1.15. It starts with a planar inductor substrate employing LTCC technology and having the same dimensions as the active layer.

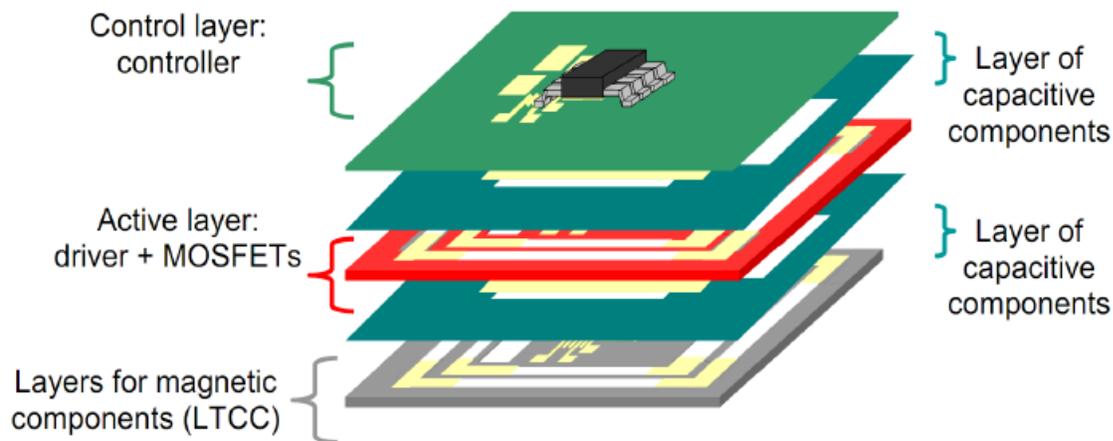


Figure 1.15. Concept of 3D integration proposed at CPES.

The LTCC technology was chosen as the magnetic for its beneficial thermal properties and decent high frequency characteristics. With its thermal conductivity being 4 W/mK, it is ten times higher than that of traditional FR-4 PCB materials. Also, LTCC has a coefficient of thermal expansion (CTE) that is closely matched to that of silicon which makes it easy to integrate the substrate and devices together. Table 1.1 below shows the comparison of materials that would be used to form a 3D integrated converter.

Table 1.1. Thermal-Mechanical Properties of Materials used in integrated converter packaging

	<i>LTCC</i>	<i>FR-4</i>	<i>Copper</i>	<i>Silicon</i>
Thermal Conductivity (W/mK)	4	0.4	17	149
CTE (ppm/C)	4	17	16.7	2.6

With these values in mind, an integrated converter design is feasible and could prove to be reliable. The next section will discuss such a design.

1.5.2 3D Integration with Inductor Substrate

A structure was proposed at CPES that utilizes a planar inductor substrate is shown in Figure 1.16 [16]. The buck converter circuit was screen printed directly onto the magnetic using a silver based paste as the conductor. The circuit was designed to have an output current of 16A with a 5V input voltage. The switching frequency was set at 2MHz. It was seen that the contact between the circuit and the magnetic structure had adverse effects on the efficiency of the converter. This was caused by magnified parasitic inductances which cause ringing during turn on and turn off. A need presented itself in the form of shielding the circuit from the magnetic.

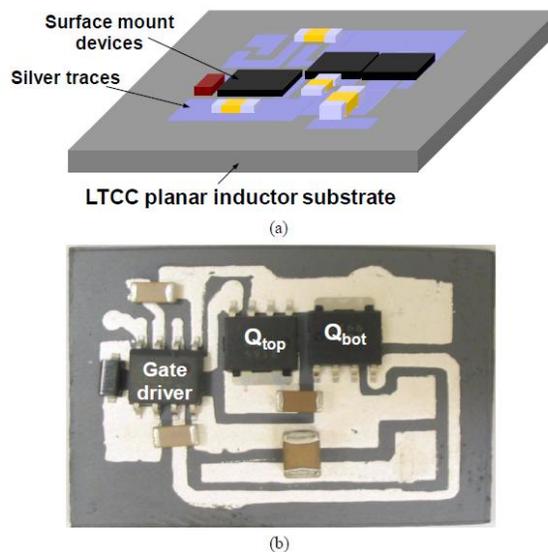


Figure 1.16. Buck Converter employing a planar inductor substrate. Concept (a) Prototype (b) [16].

The previous section showed the need for shielding the circuit from the inductor substrate. An active layer acting as an insulator was proposed with the concept drawing shown below. This substrate used Pyralux by DuPont, which is kapton tape sandwiched between two thin layers of copper. The idea is to use copper to shield the power traces from the magnetic.

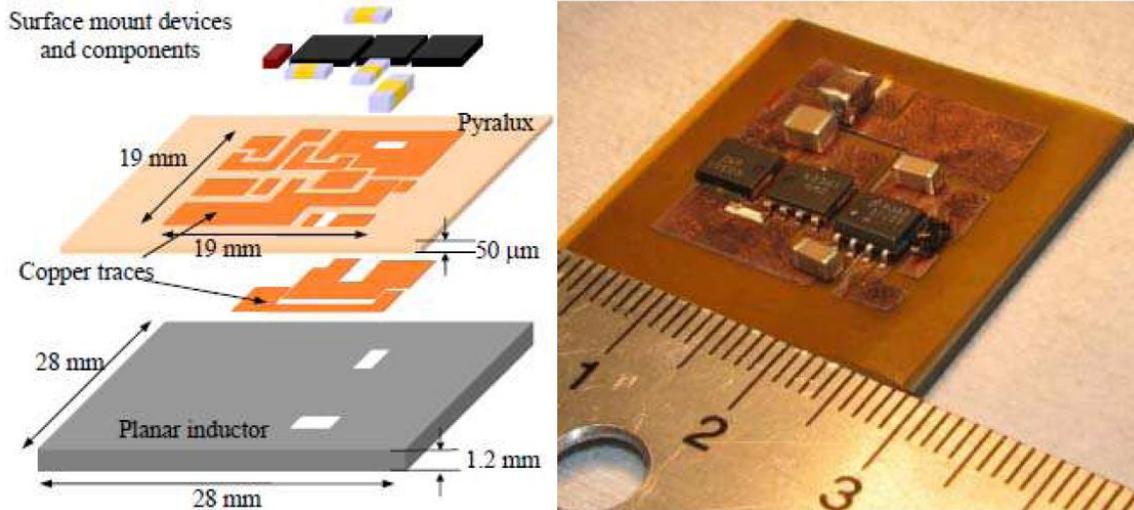


Figure 1.17. Buck Converter with Planar Magnetic Substrate and Pyralux Active Layer. Concept Drawing (Left), Actual prototype (Right) [16].

Figure 1.18 below shows the switching waveform and illustrates the difference between Generation 1 and Generation 2. The shield layer dramatically reduces the ringing and will increase the overall efficiency of the converter as shown in Figure 1.19.

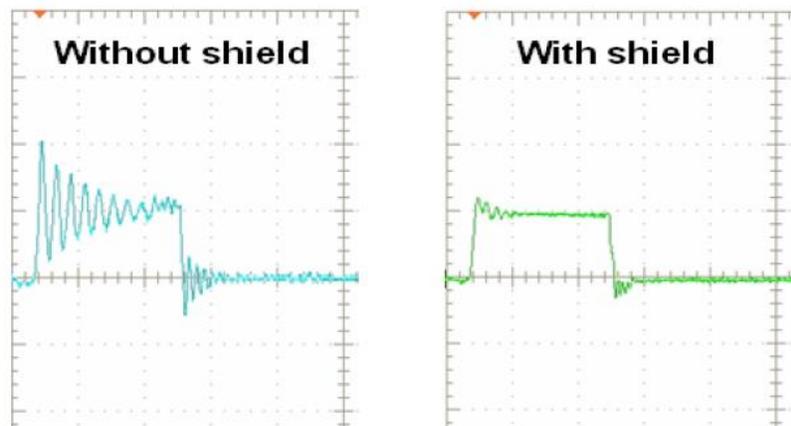


Figure 1.18. Switching waveforms of CPES integrated POL converter without and with shield layer [16].

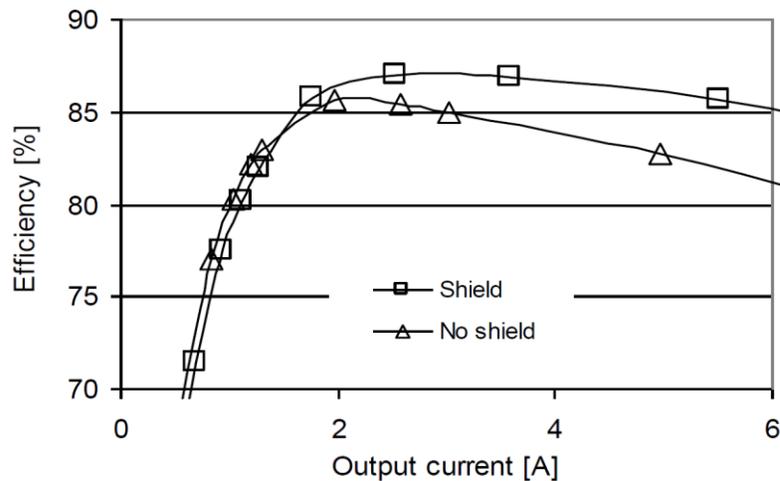


Figure 1.19. Efficiency Test Results of CPES Integrated Converter [16].

The results show that the use of a shield under the power traces can improve the overall efficiency of the converter and proves the need of a standalone active layer to insulate the devices from the magnetic substrate. Although, the efficiency of the converter still falls below the standards set by the traditional PCB versions. The results show a need to improve all aspects of the integrated converter including the design of the inductor substrate and the layout of the active layer.

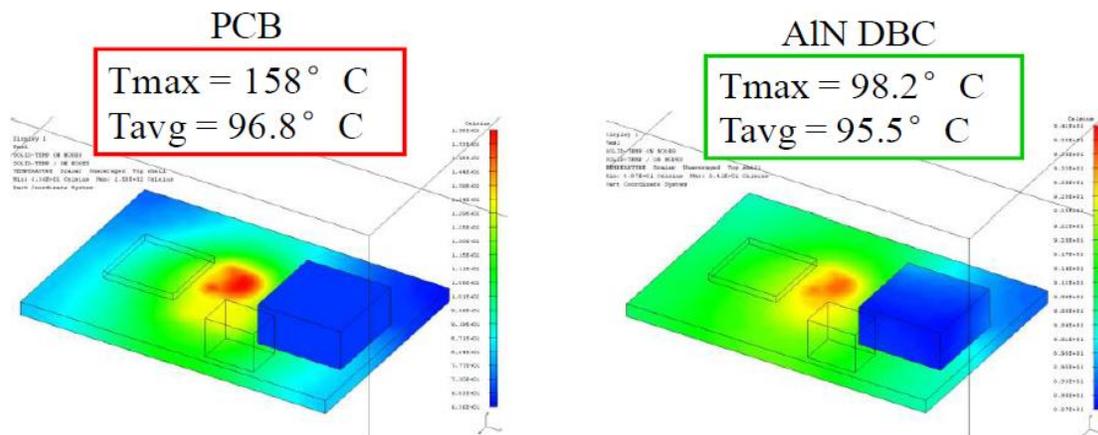
1.5.3 3D Integration with DBC Substrate

To meet the demands of the microprocessor, the output current of the converter must be in the 15-20A range. The previous design was for 16A but it was shown that the efficiency, even at 6A, was far below what is required. The need presented itself to redesign the inductor and the active layer in order to get closer to the demands of industry. Another issue that would come into play is the thermal design of the active layer, because of the high current output of the converter. We know the thermal conductivity is low for traditional PCB materials which would cause localized heating of the board around the switching devices. Table 1.2 shows a comparison of materials that can be used for the active layer substrate.

Table 1.2. Thermal-Mechanical Properties of Substrate Materials for Active Layers

	<i>FR-4</i>	<i>Al2O3</i>	<i>AlN</i>
Thermal Conductivity (W/mK)	0.4	24	180
CTE (ppm/C)	17	6.8	4.7

It can be seen that even using Alumina can dramatically increase the thermal capabilities of the active layer substrate. The ceramic substrate materials can be purchased from a company called Curamik which is now owned by Rogers Corporation. They have a proprietary process called Direct Bonded Copper (DBC) in which two layers of copper sandwich the ceramic substrate. To illustrate the benefits of using DBC for thermal reasons, a simulation is shown below [17]. It shows the effect of the ceramic substrate thermal conductivity actively spreading the heat across the surface. The PCB substrate tends to localize the heat which creates a hot spot and instigates thermal runaway in the device junction.

**Figure 1.20.** Thermal Simulations of PCB (Left) and DBC (Right) [17].

Using the principles shown above, an active layer was redesigned to take advantage of the ceramic substrate [17]. In addition to thermal management, the circuit parasitic inductances were addressed. Wire bonds were avoided to lower the parasitic inductances and a stacked power structure was introduced to make planar copper connections along with double sided

cooling of the devices. It is shown that the power loop inductance is dramatically reduced compared to previous designs.

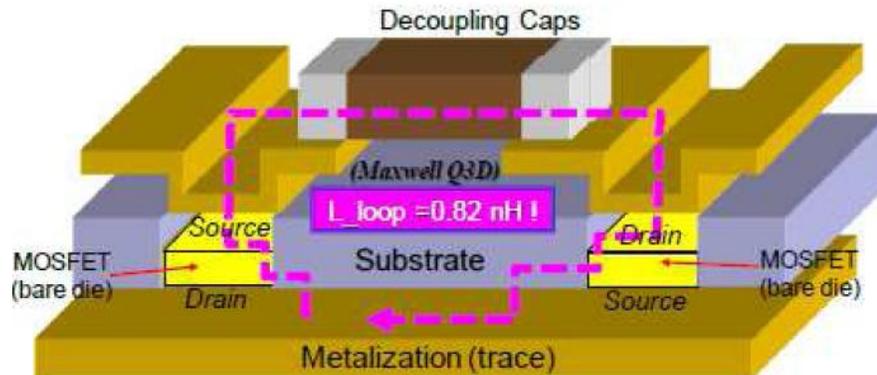


Figure 1.21. Simulation showing lower parasitic loop inductance in stacked power structure [17].

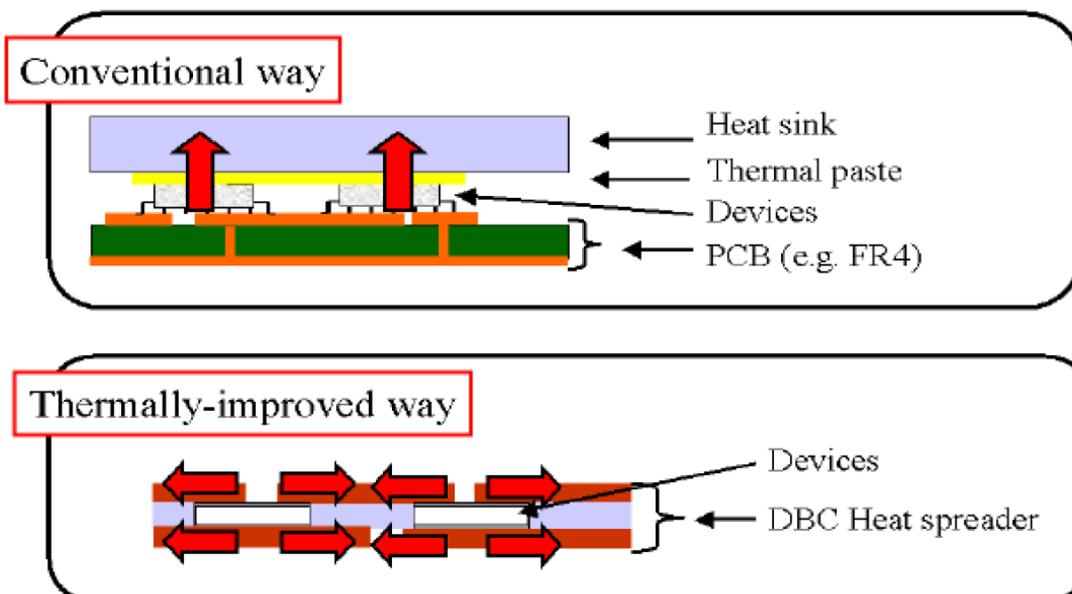


Figure 1.22. Traditional thermal management of PCB (Top) and Stacked Power using DBC (Bottom) [17].

Multiple generations were fabricated to take advantage of the stacked power structure. Generation 1 utilized an inductor similar to the one shown above with the Pyralux active layer. In Generation 2, the inductor was redesigned using a higher permeability LTCC tape in order to shrink the footprint and increase power density. The power density went from 50 W/in³ to 250

W/in^3 in the second generation. Also, the DCR of the second generation inductor was dramatically reduced which increased the full load efficiency of the converter by 2%. The drawback of shrinking the footprint of the inductor is the increase in thickness by 20% to keep the inductance needed for the design.

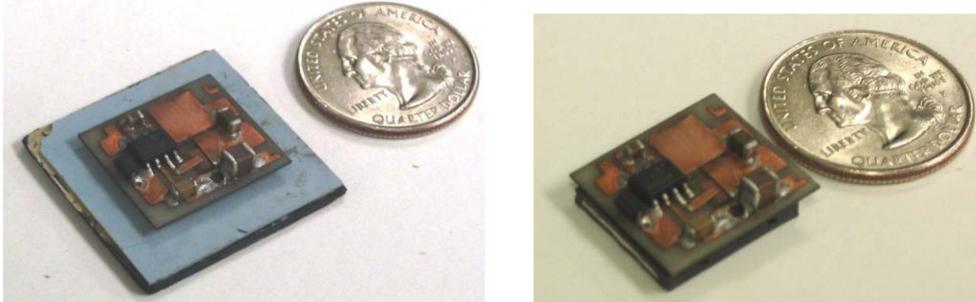


Figure 1.23. Generation 1 (Left) and Generation 2 (Right) [17]. Active layer fabricated by Author. Gen 1 inductor by Michele Lim, Gen 2 inductor by Author.

1.5.4 2 Phase 3D integration Incorporating a Coupled Inductor

The next generation of the stacked power structure was designed to use a two phase converter with a coupled inductor. The advantage of using a coupled inductor is a boost in light load efficiency because of the high inductance and faster transient speeds at heavier loads. This can reduce the size of the inductor although it presents the problem of controlling the coupling coefficient. The inductor structure was designed using a vertical flux pattern as before at CPES [18]. The active layer was made as small as possible to achieve the highest power density coming in at 9mm x 23mm. While the details of the inductor design will be discussed in Chapter 2, the fabrication of the inductor proved to be quite difficult. In order to stay in the same footprint as the active layer, the inductor thickness was reaching a theoretical limit for fabrication. While the footprint of the inductor was 51% smaller than the non-coupled version, the thickness went from 1.7mm to 3.4mm. A 3.4mm LTCC inductor had never been fabricated before according to literature surveys. Even an application engineer at the tape manufacturer had

said we had gone beyond anything he had seen. The fabrication was successful eventhough special considerations had to be made. Those details will be discussed in Chapter 2. Shown below is the prototype. The results showed that there was increase in light load efficiency by 2 % while keeping the heavy load efficiency the same. The power density went from 250W/in³ in Generation 2 to 500W/in³ for the 2 phase version.

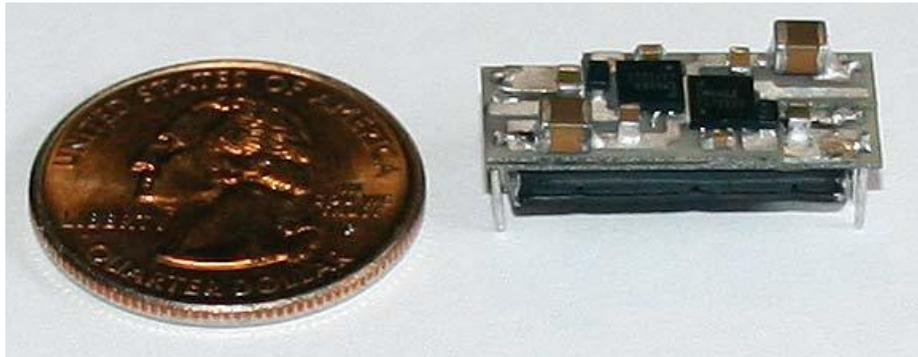


Figure 1.24. 2 phase POL with coupled inductor [17][18]. Fabrication by Author.

This work showed that we were reaching a limit for the fabrication of the inductor. The thickness was already larger than the converter active layer which employed two DBC layers. A fundamental change was needed to continue to push the power density. The next section will discuss the use of a lateral flux inductor and how that can be utilized to continue to push for higher power density.

1.5.5 3D Integration Using a Lateral Flux Inductor

Since the height of the vertical flux inductor varies as the conductor height varies, it is difficult to make the inductor thinner to push power density. A lateral flux inductor was proposed at CPES to increase the inductance density of the structure thus eliminating the thickness problem of the vertical flux inductor [14]. The graph below shows how the lateral flux inductor can maintain more inductance per volume over a wide range of core thicknesses which leads to opportunity to decrease the footprint and thickness of the core.

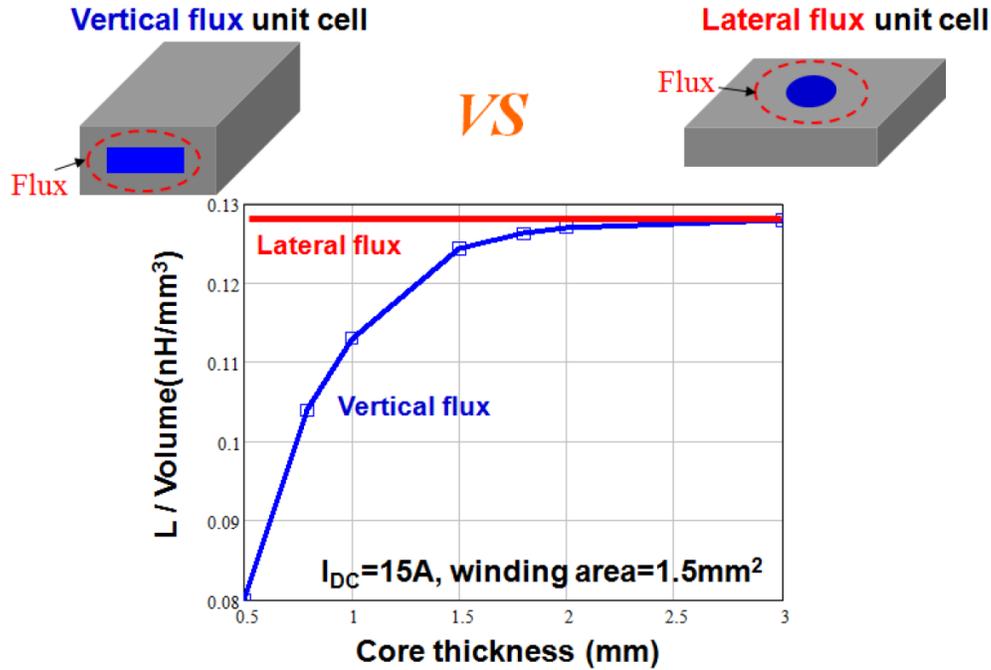


Figure 1.25. Lateral Flux Inductor Inductance Density vs Core Thickness compared to Vertical Flux [14].

At the time that the lateral flux inductor was being developed at CPES, industry was beginning to release Gallium Nitride parts. CPES would begin to explore ways of rethinking the design of the buck converter to take advantage of the lateral flux structure to make a very high power density converter. Chapter 3 will discuss the processing and fabrication of a DBC version using GaN devices to achieve power densities in the 700-900 W/in³ range. The GaN devices come in an unpackaged form which can offer much lower parasitic inductances compared with traditional packaged devices such as the SO-8 or LFPAK. Below shows the PCB versions that were fabricated and tested to learn how to mount and design converters with GaN devices [6].

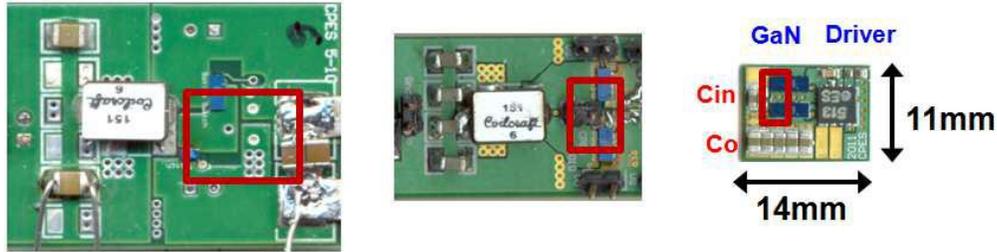


Figure 1.26. GaN Modules Gen 1 (Left), Gen 2 (Middle), Gen 3 (Right) [6].

Each generation was used as a learning tool for GaN devices. Generation 1 was used to learn how to drive the devices as well as how to mount them from a packaging aspect. GaN devices have a small margin for gate voltage (6V) so limiting overshoot is highly important. Generation 2 improved upon the layout to further reduce layout parasitic inductance to improve overall efficiency. Generation 3 combined the knowledge from previous generations to provide an optimal layout for the device and drivers used. The graph below shows results and proves that circuit layout and design can greatly improve the efficiency when using these types of devices [6].

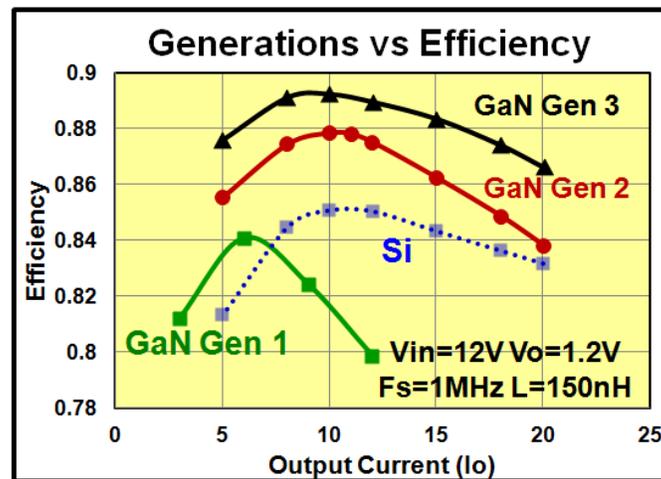


Figure 1.27. Efficiency vs Output Current for GaN Generations 1-3 compared to State of the Art Silicon [6].

The graph above obviously is based on PCB and discrete inductor technologies. Chapter 3 will discuss the processing and fabrication of a DBC version using GaN devices and the lateral

flux inductor to achieve power densities in the 700-900 W/in³ range. This fabrication will focus on the Generation 3 version.

1.6 Research Objectives

The objective of this thesis is to study and improve the fabrication and processing of a high current, high power density point of load converter.

Chapter 1 introduces the background for the work that will be done in this thesis. It details what is being done in industry and how the device and passive components are changing in the current landscape. There has been much work done to implement new device technologies to increase switching capabilities and achieve higher frequencies. Passive components are still the bottleneck in the converter design because of large footprints or large DCR.

Chapter 2 will introduce the planar magnetic substrate using LTCC technology and how it can improve the power density of the converter. First we look at the vertical flux inductor and how to improve it to give the same inductance in a smaller footprint while decreasing the DCR to give higher efficiency at full load. To decrease the DCR, a pure silver conductor paste is used in place of the existing Ag/Pt paste. This new paste is incompatible with the existing LTCC process, so careful considerations had to be addressed in order to achieve compatibility. The second part of the chapter looks at the lateral flux inductor which can achieve similar permeabilities as the vertical flux inductor in a much thinner substrate. It also avoids the material incompatibilities the vertical flux inductor suffered from to ease processing.

Chapter 3 discusses the fabrication of active layers using direct bonded copper substrates that can improve the thermal management of the converter. Increasing the switching frequency means the switches are more stressed and puts more thermal strain on the system. That coupled with the higher current means the substrate has more responsibility to spread the heat and

prevent thermal breakdown. This chapter will show how different device technologies can be integrated into a ceramic substrate to improve efficiency and thermal management. The first part is using a stacked power idea to embed the silicon devices into the substrate for double sided cooling. The second part uses Gallium Nitride devices to create a POL that can dramatically improve the power density.

Chapter 4 is the summary of this work and presents future work.

Chapter 2: Point of Load Converter Passive Layer Packaging

2.1 Magnetic Substrate

2.1.1 LTCC Background

The Low Temperature Co-Fired Ceramic (LTCC) process has been well established in industry; although most research has been done using dielectric tapes instead of magnetic based solutions. Dielectric tapes have been used for many years because of their excellent high frequency properties. This makes these types of tapes ideal for RF applications such as Bluetooth [19]-[20]. Magnetic tape research is very limited due to the small number of companies that produce the tapes. One such company is Electrosience Labs located in Pennsylvania. They produce 3 types of magnetic tapes with varying levels of permeability: 50, 200, and 500.

The tape casting process is identical to that of the dielectric tapes. The graphic below shows the flow chart of the process. You start with a magnetic particle powder (in this case it is a ferrite particle in order to have high electrical resistivity for high frequency applications) and mix that with some type of solvent.

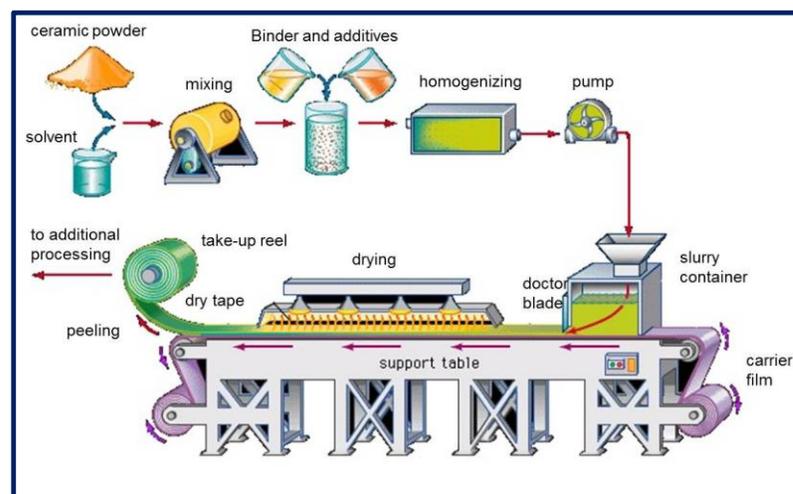


Figure 2.1. General Tape casting process

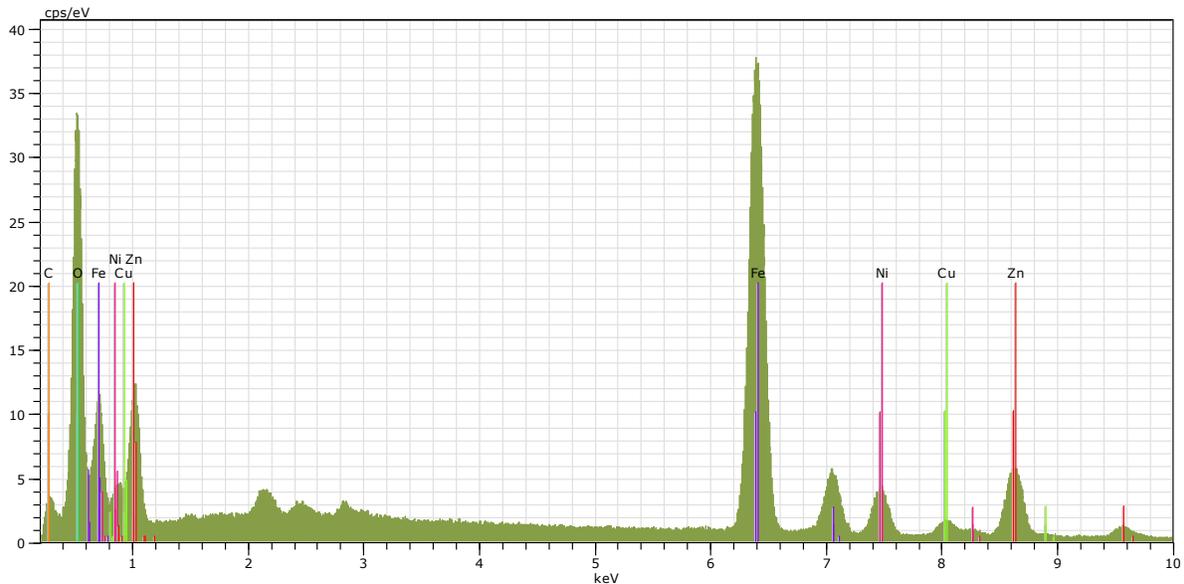
Then organic binders are added to create a slurry. This mixture is fed into the tape casting machine. A doctor blade system is used to control the tape thickness as the slurry is spread onto a Mylar backing. The tape is then fed through the drying section to evaporate the solvent and rolled for shipment or use.

Literature discusses several mechanisms that tape sintering can fall under [21]. The two mechanisms that will be discussed in this paper include solid state sintering and liquid phase sintering. These sintering mechanisms lead to densification for polycrystalline materials which are used in this research. There are three stages that constitute the sintering process: initial, intermediate, and final. Some literature will consider particle adhesion as a stage zero but we will consider adhesion as part of the initial stage.

The initial stage is dominated by particle neck growth by diffusion. This stage lasts until the neck growth is around 40-50% of the particle radius. The shrinkage in this stage is about 3 to 5% when you consider the entire shrinkage of the system is 17- 20% [22]. The intermediate stage is where most of the sintering and shrinkage occurs. Densification is occurring as the porosity between the particles is shrinking. This leaves isolated pores throughout the system. The stage ends with the density being around 90% of the theoretical. The final stage just includes the continued and almost complete removal of the leftover pores.

Since this research will be discussing the use of the green ferrite tape supplied by Electroscience Labs, Inc., there are a few things to point out about these tapes. The graph shown below is an analysis of the green tape using an Energy Dispersive Spectroscopy (EDS) system. This analysis was done at the Nanoscale Characterization and Fabrication Lab at the Virginia Tech Corporate Research Center. Note the presence of copper in the system which represents a change in the traditionally used NiZn ferrites for electronics. The copper presence, coupled with

the proprietary organic binders that are in the system, makes this system a low temperature co-fired ceramic product. The aim is to be able to sinter the tape under 900° Celsius. The reason we need a low temperature sintering is the ability to co-fire the tape with a silver based conductor which allows for the fabrication of a planar inductor.



Mass percent (%)

Spectrum	C	O	Fe	Ni	Cu	Zn
Sample 2	8.62	26.39	39.77	5.96	3.13	16.14
Sample 2	8.90	26.71	39.45	5.96	3.02	15.97

Figure 2.2. Energy Dispersive Spectroscopy of LTCC tape and element breakdown. Image by Author.

To further characterize the tapes supplied by ESL, a permeability vs. frequency graph is needed to investigate the tapes usefulness in the power electronics field. The permeability number is needed later in the design and the applicable frequency must be checked to ensure a high q . To do this, a toroid is fabricated with the dimensions of 14.5mm outer diameter and 9.7 inner diameter with a thickness of 2mm. This is a thin ring toroid that we can assume has uniform flux distribution. The toroid is then placed in an Agilent 16454A test fixture. This test

fixture creates a single turn through the toroid and is attached to an Agilent 4294A impedance analyzer. Using software written for the test fixture, you can sweep the permeability vs. frequency.

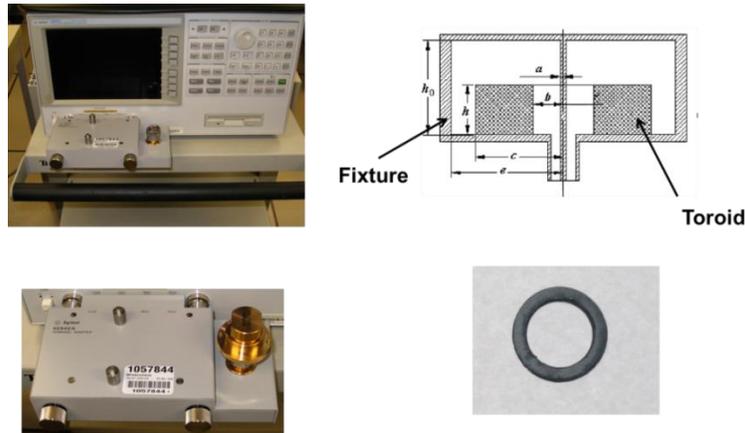


Figure 2.3. Impedance Analyzer (Top Left), Concept Drawing of Test Fixture (Top Right), Test Fixture (Bottom Left), Test Toroid (Bottom Right). Image by Author.

It can be seen that the 50 tape has a permeability around 47 while the 200 tape is actually 200 or slightly above. The frequency range we are looking at is 1.3 MHz so the u'' is still sufficiently low to give us a high q inductor. It shows that the q value is actually higher for the 200 tape in that frequency range. The 200 tape could be used to 4-5 MHz.

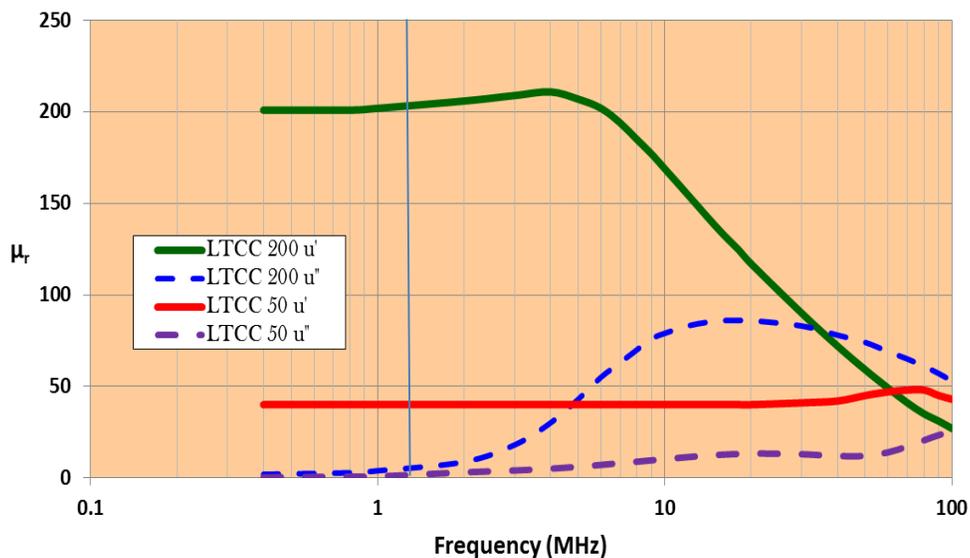


Figure 2.4. Permeability vs. Frequency for LTCC 50 and 200. Image by Author

In industry, the LTCC fabrication process consists of blanking the tape, via punching and filling, and conductor printing. The structure is then stacked, laminated and co-fired. In this research we will consider using a CO₂ laser machining system as shown below for inductor fabrication. Figure 2.14 shows the actual laser machine found in the CPES packaging lab on the left and a depiction of the laser interaction with the material on the right. The laser method has its advantages and disadvantages in the research field. Using a CO₂ machining laser to cut the tapes allows for multiple design variations and small sample sizes. It also has some inherent drawbacks such as material heating (in the case of soft ferrite tapes – burning) and optical diffraction across the material thickness resulting in a non-vertical cut wall.

2.2 Magnetic Substrate with Vertical Flux Pattern

As seen in the introduction, the planar magnetic inductor is feasible. Since there is a need to separate the active and passive layers for shielding, the inductor will be redesigned. This section will discuss the design and fabrication of an inductor substrate with a vertical flux pattern. Figure 2.5 shows a depiction of a vertical flux inductor on the left and the design parameters on the right. Note that the conductor is embedded in the ferrite tape which is a key point in this section. The vertical flux pattern is perpendicular to the substrate. Section 2.2 is done with Michele Lim, Arthur Ball, and Yan Dong at CPES.

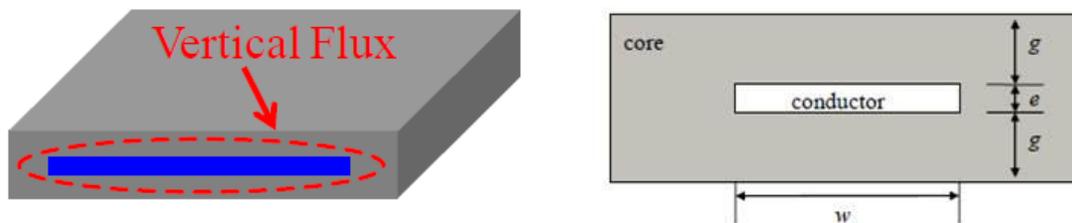


Figure 2.5. Depiction of a Vertical Flux Structure (Left), Cross Section (Right) [16].

2.2.1 Previous Work

All the work presented in section 2.2.1 and 2.2.2 was done at CPES by Michele Lim [16]. The design of the inductor is reported with a single turn conductor and based on the parameters shown in Figure 2.5 (b). Without going into a lot of detail, an empirical model was developed for inductor structures using LTCC tape and rectangular conductors embedded in the structure. Equation [2.1] shows the results and also takes into account the non-linear behavior of the LTCC tape with respect to changing DC current.

$$\frac{L}{l} = \frac{U_r \mu_0}{2\pi} \ln\left(\frac{\frac{w+e}{2} + 2g + \sqrt{\frac{w^2 + e^2}{2} + 4g^2} + 2g(w+e)}{\frac{w+e}{2} + \sqrt{\frac{w^2 + e^2}{2}}}\right)$$

$$\text{where } U_r = 10^{4w(I_{DC}+5.4)+0.037(46.4-I_{DC})}$$

Eq. 2.1

μ_0 is the permeability of air, w is conductor width, e is conductor thickness, g is core thickness, l is conductor length and L is inductance. Using this empirical model and the initial inputs of $L_0 = 100\text{nH}$, $I_{dc} = 16\text{A}$ and the footprint dimensions of $28\text{mm} \times 28\text{mm} \times 1.7\text{mm}$, the inductor was designed.

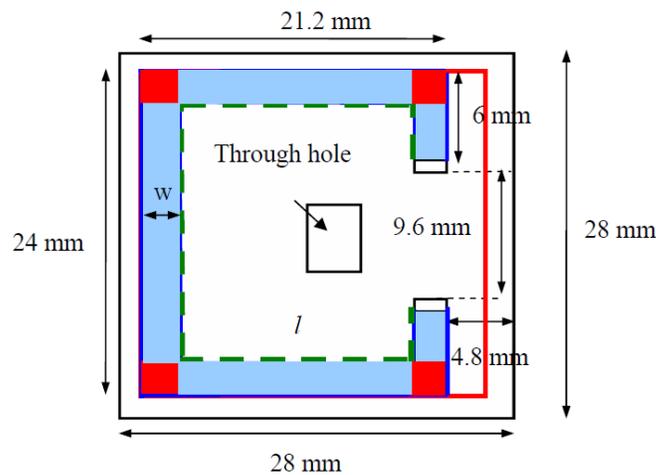


Figure 2.6. Design Layout of the Inductor [16].

2.2.1.1 Fabrication

The fabrication process for an LTCC inductor is a simple one yet there must be attention paid to the details or the structure will fail during sintering. The technique presented in the following section will be a common theme throughout the chapter. The Electroscience Labs LTCC tape with a permeability of 50 is used. The conductor material is 953 silver/platinum (Ag/Pt) paste which is also supplied by ESL and has a conductivity of $5.88 \times 10^{-8} \Omega\text{m}$. The inductor is fabricated in three separate stages. First the top, middle, and bottom rectangular pieces are cut to size from the green tape and laminated separately using a uniaxial press for 15min at 70°C . The middle layer is then laser cut to form the conductor paste “well” and is then laminated to the bottom piece. The paste is then printed into the well in four steps with a drying step accompanying. The drying step (80°C) allows the paste to settle into the well and remove any trapped air. Subsequent printing steps continue to fill the gap until it is uniform with the top of the well. The top piece, which has electrode spaces cut out of it, is then laminated to the other two pieces. The electrodes are then printed with conductor paste. The whole inductor is then sintered in air using the profile in figure 2.7(a) and the finished product is found in figure 2.7(b).

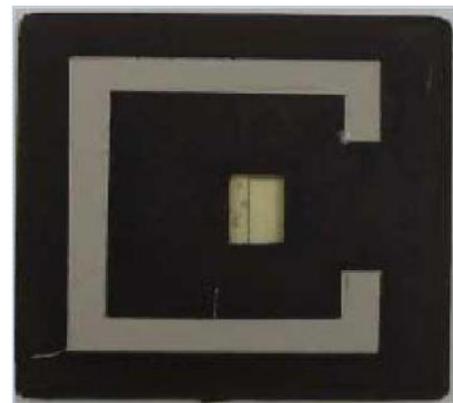
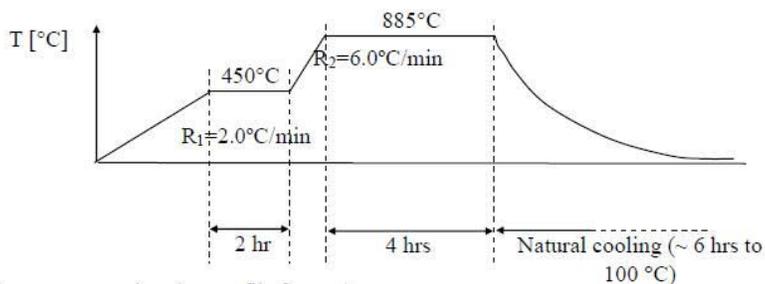


Figure 2.7. Sintering Profile (left) and Generation 1 Inductor Prototype (right) [16].

The final measurements of the inductor are 28mm x 28mm x 1.7mm thick. Another important aspect of the design is the DCR of the sintered conductor. The simple DCR equation is found below. R is the resistance in ohms, ρ is the conductivity in Ωm , l is the length of the conductor, w is the width, and t is the thickness.

$$R = \rho \frac{l}{wt} \quad \text{Eq. 2.2}$$

Using this equation with the values from the design and a ρ of $5.88 \times 10^{-8} \Omega\text{m}$, the final DCR of this structure is around $2\text{m}\Omega$. Considering that a discrete inductor with a straight bar conductor has a DCR of $0.2\text{m}\Omega$, this represents a significant drawback to the Generation 1 planar inductor design.

2.2.2 Improving Original Design

The design shown above proved the theory of a planar magnetic substrate. However the volume of the inductor dramatically decreased the power density of the converter. This section will discuss the improvements that were made to increase the power density. The work presented from this point to section 2.3 is that of the author in conjunction with graduate students in CPES – Arthur Ball and Michele Lim if the heading is underlined.

We start with the single bar inductor to learn how much inductance can be achieved using the tape with the increased permeability. The single bar inductor is chosen in order to keep the lowest DCR which affects overall converter efficiency especially at heavy load. We will assume the $I_{\text{max}} = 20\text{A}$, $I_{\text{dc}} = 20\text{A}$, $V_{\text{out}} = 1.2\text{V}$, $f_s = 1.3 \text{ MHz}$, $e = 0.7\text{mm}$, $g = 1\text{mm}$, and total width = 9mm .

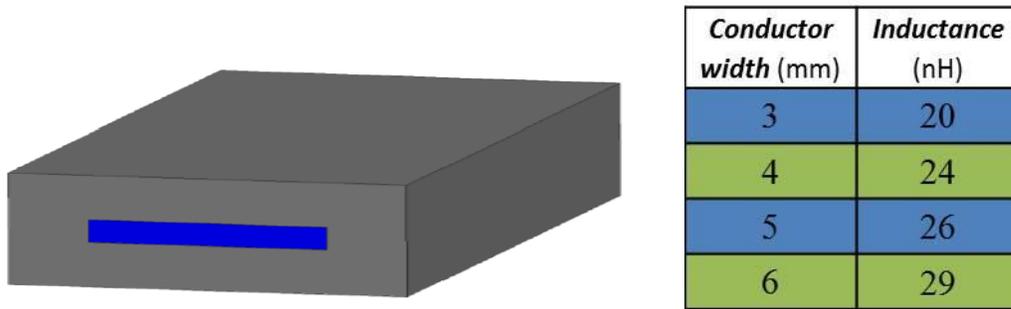


Figure 2.8. Depiction of a Single Bar Inductor and the calculated inductances based on varying conductor width. Image by Author.

Using the equation 2.1 above, we can vary the conductor width for a given footprint and calculate the inductance. The table shows the calculated results. Now that we have the calculated inductance, samples were fabricated, according to the procedure outlined above, to compare the theoretical to the real value. The testing setup is using a buck demo board from Renesas that uses a Dr. Mos chip for the switching stage. Figure 2.9 shows the setup.



Figure 2.9. Inductor Test Setup using Buck Converter Demo Board from Renesas [16].

The inductance can be found using the simple equation that is shown below.

$$L_{sim} = \frac{V \cdot \Delta t}{\Delta i} \quad \text{Eq. 2.3}$$

The waveforms shown in Figure 2.10 are found using a rogowski coil wrapped around one leg of the inductor and measuring the inductor current [23]. We are looking at the change in current over time and assuming the current is linear although there is some slight skewing of the waveform during the larger load measurement. This example is for the 3mm conductor width. Similar measurements were made for each of the conductor widths.

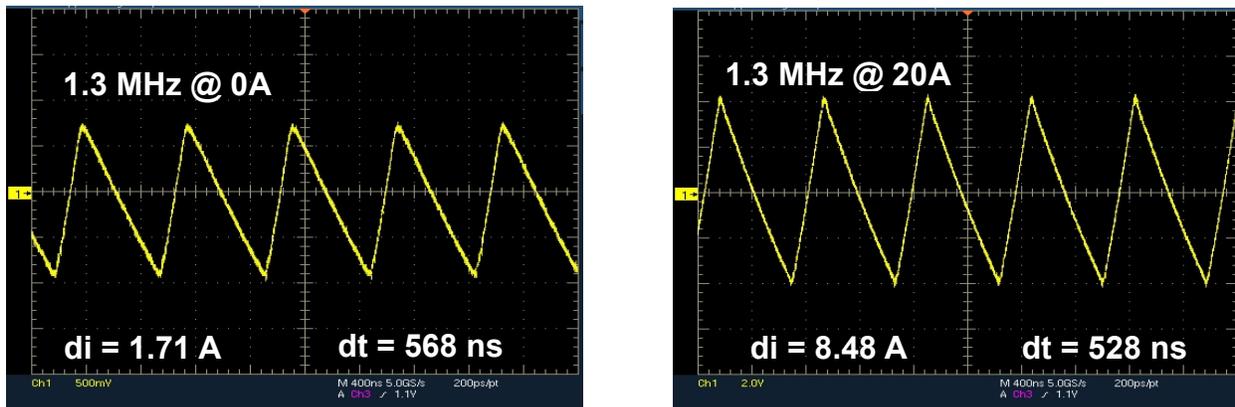


Figure 2.10. Light Load (Left) and Heavy Load (Right) Inductor Current Measurements. Image by Author.

<i>Conductor width</i> (mm)	<i>Calculated Inductance</i> (nH)	<i>Measured Inductance</i> (nH)
3	20	19.2
4	24	23.7
5	26	25.6
6	29	29.2

Table 2.1. Calculated and Measured Inductance for Single Bar Inductor

So we can use equation 2.1 to closely predict the inductance for a given inductor structure using LTCC tape. The next step is to design an inductor that meets the requirements for the buck converter design [17]. The footprint of the converter is the same as shown above and is given to be 400mm^2 . The optimal inductor design would be the same footprint as the active layer to achieve the maximum power density.

2.2.3 Generation 2 Inductor Design

The Generation 2 design is aimed at improving the footprint and the DCR from the inductor in Generation 1 shown above. The requirements are 60nH at 20A, a footprint of 400mm² and the lowest DCR possible. From the previous results in the previous section, the single bar inductor with a conductor width of 6mm and overall length of 20mm, achieves an inductance of 29.2nH at 20A. So the logical next step was to series two single bar inductors together to hopefully get the desired full load inductance. This would take care of the first and second requirements of the inductor. Figure 2.11 shows the depiction and measurements of the inductor.

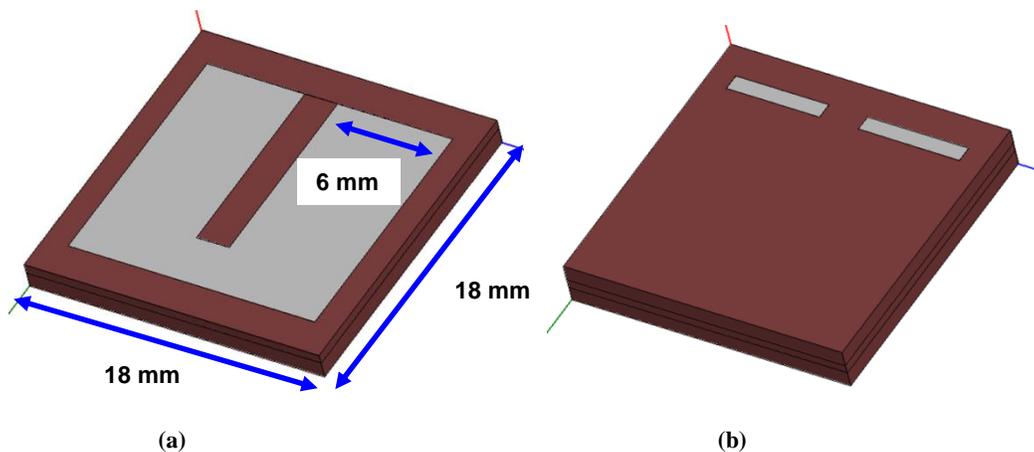


Figure 2.11. Generation 2 inductor without (a) and with top (b) layers. Image by Author.

The design was simulated to check the viability of the structure as far as flux flow. The structure was built using Ansoft Maxwell 3D and simulated with a DC bias of 20A. We can see that the flux around the connection of the 2 single bar inductors is essentially pinched causing some saturation and low permeability. There is also little inductance contribution from the bottom corners of the structure, so they can almost be removed with no consequence.

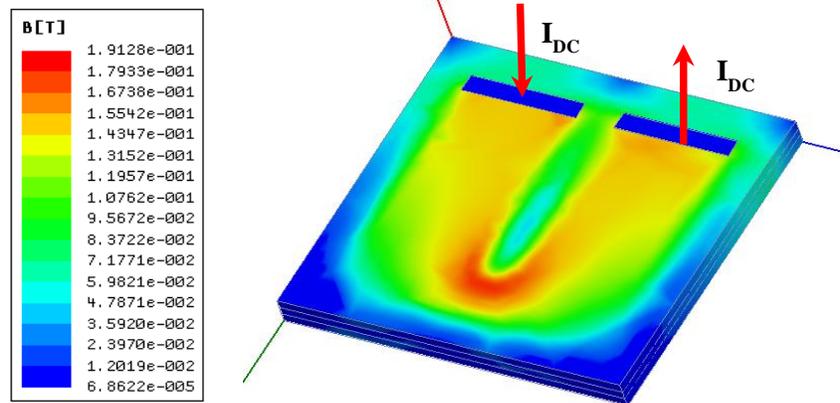


Figure 2.12. Simulation of Flux in Gen 2 design using Ansoft Maxwell. Image by Author.

The estimated inductance value for the design is 65nH. The simulated value of this structure came out to be 70nH. So the requirements for the circuit design could be met with this inductor design. The next step is to fabricate the design.

2.2.4 Fabrication of Generation 2 Inductor

The inductor is fabricated in the same way as the first generation. It consists of a bottom, middle, and top layer with the conductor embedded between the top and bottom layers. This fabrication used the ESL 953 paste as the Generation 1 design did. We know the inductance value of the design is good but a comparison in DCR to Generation 1 is needed.

First the bottom layer is cut from the Mylar tape carrier. One must be careful to include the future shrinkage during sintering so 20% is added to the green tape cut. During trial and error of fabricating these structures, it is found that cutting the green tape to the exact design size is not a good idea. When stacking and pressing the layers, uneven edges will lead to cracking during sintering. Thus it is found to add an additional 10% to the initial green tape cut which will be removed with the laser during the process. The laser is putting sufficient energy into the system to essentially burn or sinter the edges of the soft tape and create a smooth even edge.

This helps the process as it eases the stacking of the bottom and center layers and then the bottom/center layer to the top layer.

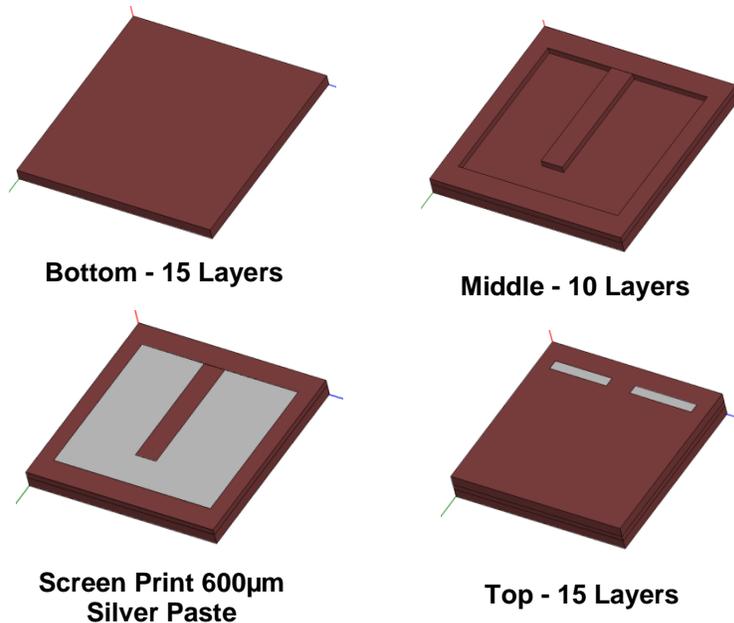
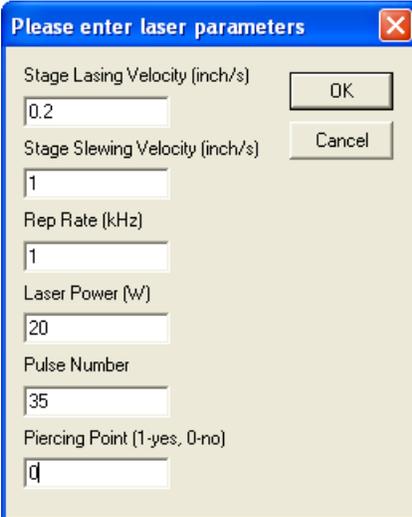


Figure 2.13. Generation 2 Inductor Fabrication Concept. Image by Author.

So the 15 layers for the bottom layer are cut from the roll of green tape. The layers are then stacked by rotating each successive layer 90 degrees. This will ensure there are no grain boundary problems during sintering. The layers are then pressed in a uniaxial hydraulic press as shown below. The layers must be pressed at 2000psi for 15 minutes with a 90 degree rotation in the first 5 minutes to give even pressure across the entire layer surface which ensures that the lamination is uniform. The same is done for the middle and top layers to have 3 layers that are the same and ready to be laser cut.

soft material, it is placed on a piece of Alumina tile for strength which had to be factored into the focusing process. The laser program has the following parameters that can be variable: Stage Lasing Velocity (in/s), Stage Slewing Velocity (in/s), Rep Rate (kHz), Laser Power (W), and Pulse Number. All these values had to be found to optimally cut the structure.

The stage lasing velocity is the speed at which the stage moves during the on time of the laser. The stage slewing velocity is the speed at which the stage moves during the off time of the laser. Rep Rate controls the pulse width of the laser. Laser Power is the amplitude of the laser wave and Pulse Number is the amount of pulses in a particular cycle. For ferrite green tape the parameters are shown below keeping in mind that the laser power needs to be 1 W per layer and pulse number needs to be 2x the laser power. So this example is for a 20 layer structure.



The image shows a Windows-style dialog box titled "Please enter laser parameters" with a close button (X) in the top right corner. The dialog contains several input fields and two buttons: "OK" and "Cancel". The parameters are as follows:

Parameter	Value
Stage Lasing Velocity (inch/s)	0.2
Stage Slewing Velocity (inch/s)	1
Rep Rate (kHz)	1
Laser Power (W)	20
Pulse Number	35
Piercing Point (1=yes, 0=no)	0

Figure 2.16. Laser Parameters for cutting ferrite green tape. Image by Author.

The bottom layer is trimmed to the design dimensions including the 20% shrinkage rate. The center layer is trimmed to the same dimensions as the bottom layer and then the well is created by a second round through the laser. The center layer was covered in kapton tape prior to cutting so that the layer will be protected during the screen print step. The top layer follows the same procedure including a second laser cut for the electrodes. The bottom and center layers

are then sent to the hydraulic press for lamination. This lamination step is very important and differs from the original lamination because of the change in surface area of the center layer. Instead of 2000psi for 15 min, this step is 500psi for 1 min. Anything longer or with more pressure will result in the center layer being pressed into the bottom layer. The well for the conductor paste will no longer be present and the structure will go back to step one.

Once the lamination is done, it is time for the screen printing of the conductor paste. Since the center layer already has kapton tape protecting it, all that is needed is to tape the structure to a piece of Alumina for transporting. The paste is then screen printed into the well and placed on a hot plate at 80 °C for at least four hours but overnight is better. This is due to the large area that is being printed and air removal is vitally important. Once that is dry, successive prints are done and dried for an hour each until the well is completely level. The final bottom and center laminated structure with embedded conductor paste is shown below. The top is then laminated unto the bottom/center layer and the electrodes are screen printed and dried.

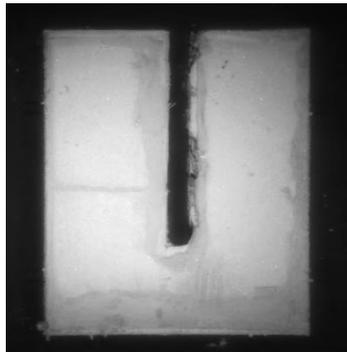


Figure 2.17. Center Layer of Actual Prototype for the Gen 2 inductor using ESL 953 Paste. Image by Author.

The inductor has a total of 45 layers which makes its total thickness around 2.7mm or 40% thicker than the previous design. The outside of the center layer is 2mm while the center leg of that layer is 1mm.

Next, we will look at the DCR comparisons from the first and second generations. Equation 2.2 is used to find the resistance. The redesign of the inductor leads to a decrease of 45% in the DC resistance. But the drawback is the DCR is still 5x that of a commercial chip inductor. This will still affect the heavy load efficiency of the converter.

Table 2.2. Comparison of DCR between Gen 1 and Gen2 inductor

	DCR
Generation 1	2m Ω
Generation 2	1.1m Ω

More study needed to be done to find a suitable replacement for the ESL 953 paste which could lead to lower DCR values. The next section will discuss this situation.

2.2.5 New Silver Paste Selection and Characterization

The first step is to search products available on the market that could be suitable for the planar inductor structure. The paste must also be similar to the ESL 953 paste in that it must be close in sintering temperature to the LTCC tape, otherwise it will lead to significant problems during sintering that might not be possible to overcome. A search through literature leads to the table that is listed below. This includes suitable candidates and compares those to traditionally used materials.

Table 2.3. List of Suitable Conductor Pastes

Material	Manufacturer	Sheet Resistance @ 25 μm thickness	Sintering Temp	Sintering Ambient	Comment
<i>Elemental Cu</i>	--	0.68 m Ω / \square	--	Reduction or Inert	--
<i>2312 Cu Paste</i>	Electroscience	1.5m Ω / \square	980°C	Inert	Thick Film
<i>953 Ag/Pt Paste</i>	Electroscience	6m Ω / \square	875°C	Air	Top or Internal Metallization
<i>903 Ag Paste</i>	Electroscience	2m Ω / \square	875°C	Air	Internal Metallization
<i>903-D Ag Paste</i>	Electroscience	2m Ω / \square	875°C	Air	Top Metallization
<i>7740 Ag Paste</i>	Dupont	0.84m Ω / \square	850°C	Air	Internal Metallization, High Current
<i>6148 Ag Paste</i>	Dupont	8m Ω / \square	850°C	Air	Internal Ground
<i>6145 Ag Paste</i>	Dupont	3m Ω / \square	850°C	Air	Internal Signal

Judging by the table, two candidates could be chosen to meet the requirements for our design – ESL 903 and DuPont 7740. In fairness to Michele, the 903 paste was not available from ESL at the time of her dissertation so she was limited to the 953 paste. The decision had to be made on which product was to be used. Since the lowest DCR is what we were after, the DuPont 7740 silver paste was chosen [25].

2.2.5.1 Characterization of DuPont Silver Paste

Verification of the resistance was needed since the datasheet value is listed at a thickness of 25 μm . The recommended total fired thickness according to the datasheet is 170 μm . This could pose a problem since our design is for a conductor thickness 750-800 μm . This issue would have to be handled in future processing. The verification process was done by cutting a channel in a piece of Alumina with a known height and included probe points. The paste was screen printed and dried at 80 °C as the 953 paste had been. The structure was then fired using the same sintering profile as the ESL paste. This would also reveal some information about shrinkage as well. Copper straps were soldered to the conductor to allow connections to the measurement tools.

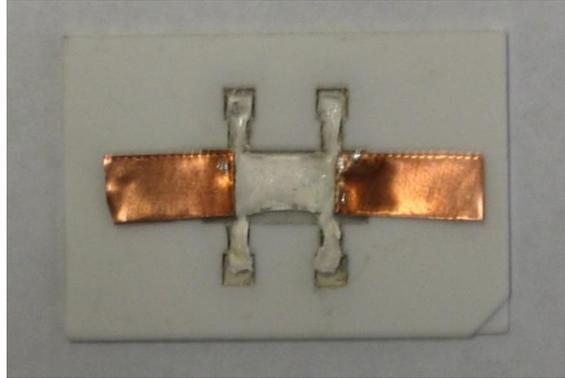


Figure 2.18. Silver Paste Characterization Structure.
Image by Author.

To ensure an accurate resistance measurement, a Kelvin four wire technique is used. The principle of the technique is to avoid measuring the resistance in the wire while measuring the resistance in the subject. The four wire measurement uses a voltmeter and ammeter together. This allows the voltmeter to carry miniscule current thus the voltmeter wire connections are not contributing to any voltage drop across the subject. An accurate measurement should be found even though alligator clips are used instead of Kelvin clips. Shown below is the Agilent 34970A which is used for the test. The results show that the conductivity is almost 3x less than the 953 paste. It makes sense that it is lower since the DuPont 7740 is pure silver compared to the ESL 953 being a silver platinum paste. It is found to be $2.1 \times 10^{-8} \Omega\text{m}$.

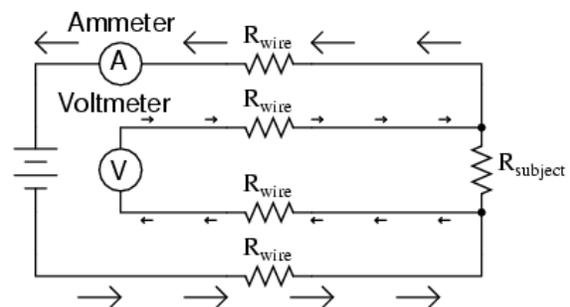


Figure 2.19. Agilent 34970A 4 wire measurement equipment (Left), Concept of four wire measurement (Right). Image by Author.

2.2.6 Compatibility Issues Between LTCC Tape and DuPont Silver Paste

Now that the silver paste has been characterized, it is time to fabricate the generation two inductor again with the new paste. It will follow the same technique that was shown above. There are some preliminary issues that can be automatically seen from the datasheet. It is clear that the sintering profile is drastically different than the profile for the LTCC tape.

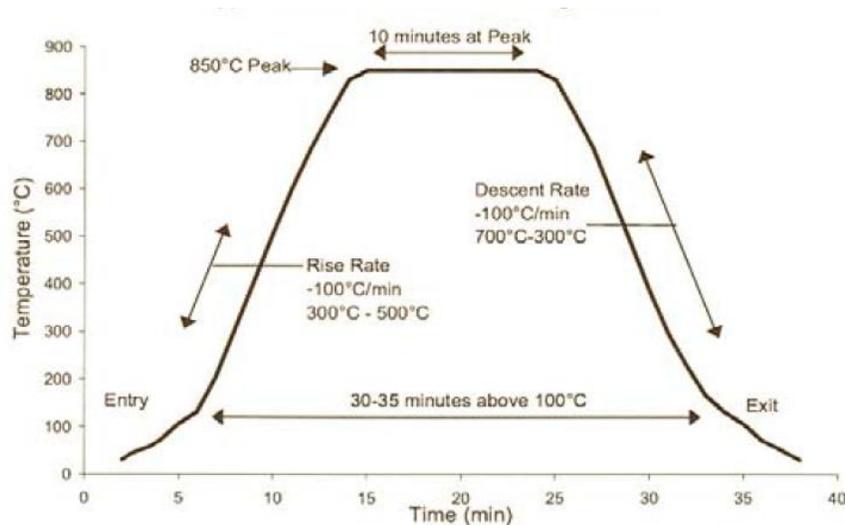


Figure 2.20. DuPont 7740 sintering profile. From datasheet.

The paste is sintered at 850°C for 10 min with a total profile time of 30 min. So the paste sintering must fit into the LTCC profile not the other way around. Initial results show that there are some compatibility issues between the silver paste and the LTCC tape. There is extensive cracking present that represents stresses in the system during sintering. The assumption is that there are differing outgassing times for the paste and tape. The tape has binder burnout at 450°C but it is not known when the binder burnout occurs for the paste. It can be seen that the rise rate for the paste is very high which tells the user that the binder burnout is occurring quickly before the sinter temperature. Another theory states that there is a CTE mismatch in the metal-ceramic system. The picture below shows a corner of the inductor and how the cracking is occurring.

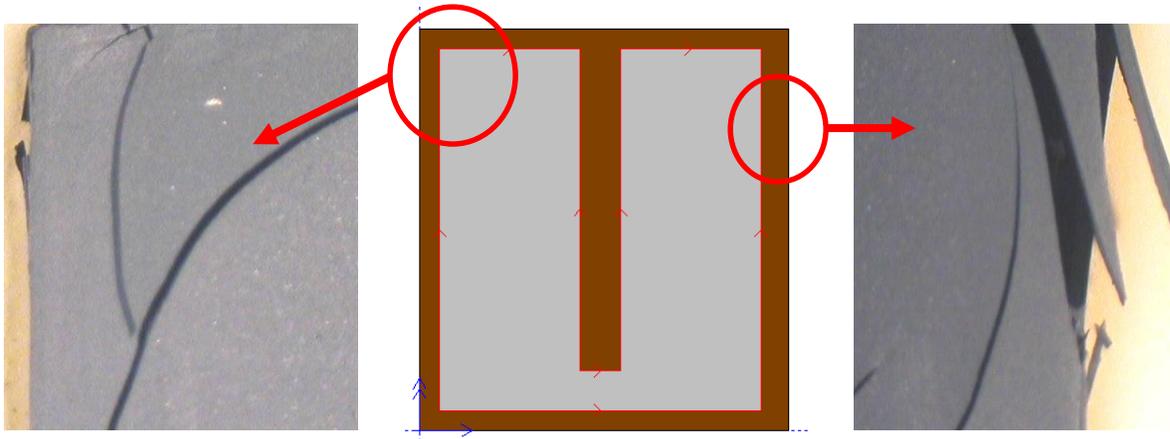


Figure 2.21. Cracking of Inductor due to material incompatibility. Image by Author.

Obviously there is severe mismatch between the conductor paste and the LTCC ferrite tape. It is known from literature that residual stresses can cause cracking in a metal-ceramic system [26]. The hypothesis is that there are two possible scenarios occurring. The first is that the binder burnout and subsequent sintering of the conductor paste is causing pressure build up inside the embedded structure which forces its way out of the tape like a tree root under a sidewalk. The second scenario determines that the conductor is self-heating after sintering which induces different cooling rates and causes pressure build up which forces its way out. Both of them would be considered residual stresses. The next two sections will introduce ways to offset the stress build up in the embedded structure through fabrication.

2.2.7 Gas Channels in Middle Layers

By observation, there are cracking problems at all four corners of the Generation 2 inductor. The design had to be changed to address this specific issue. During a conversation in a project meeting, the idea was discussed to add channels in the structure to allow a relief of pressure for the conductor. The hope was to also assist in binder burnout of the embedded conductor paste. In addition to the channels, the ends of the inductor could be removed as shown

in Figure 2.12. The Maxwell simulation showed that the flux in the inductor did not travel through the ends, thus there is not a lot of inductance contribution in those parts.

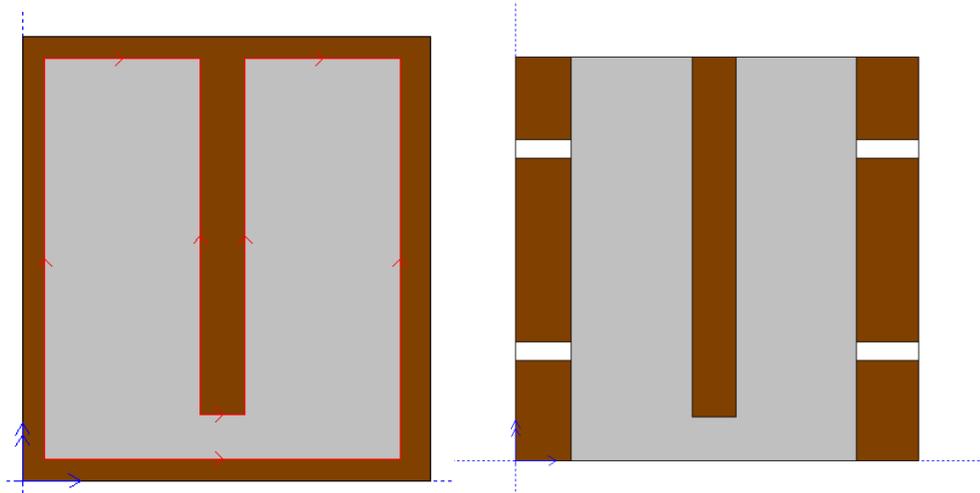


Figure 2.22. Changes in the inductor structure to combat material mismatch. Image by Author.

The changes are applied to the middle layer only. As can be seen above, the ends of the tape are removed from the structure. This, along with the channels cut from the sides, allows the burnout to occur through six channels. It can also be seen that there was 1 mm added to each side of the structure while the conductor structure stays the same. This allows a larger surface area for lamination since the end surface area has been removed. Essentially, the volume of the inductor stays the same but shifts the structure to help with the conductor paste compatibility. The electrodes are no longer cut through the top layer. The paste is now printed on the outside of the top layer and wrapped around to make contact to the middle layer.



Figure 2.23. Side view of inductor showing gas channel. Image by Author.

2.2.8 Changes in Sintering Profile

The change in the inductor structure was the first of two changes. There was also an apparent need to change the sintering profile shown in Figure 2.9 to assist with the material compatibility. The original sintering profile was given by ESL for the co-firing of their LTCC tape and their conductor paste products. Adjustments needed to be made when using the DuPont silver paste with the LTCC tape. We know from sintering theory that the initial stage occurs before binder burnout. This means that only 5% of the shrinkage occurs in the initial stage and less stress on the structure is the result. While speaking with Dr. Kathy Lu from the material science department at Virginia Tech during a powder processing class, she suggested speeding up the rate before binder burnout because the stress is low. Most of the stress is occurring between binder burnout at 450°C and the end of sintering at 885°C. Thus it was suggested by Dr. Lu to also slow down the rate between those stages. So the rates were adjusted from the original sintering profile by trial and error until the profile is found below.

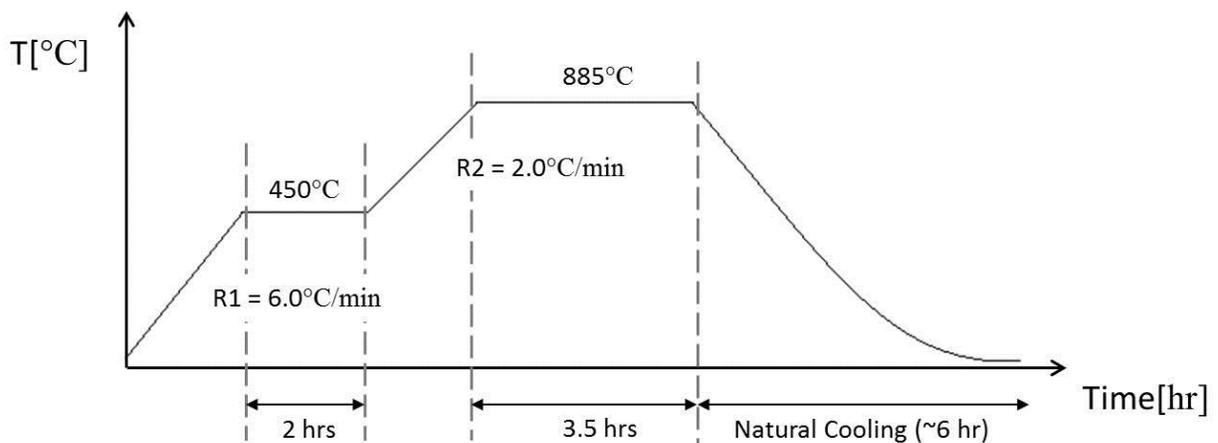


Figure 2.24. New sintering profile for DuPont paste and LTCC tape. Image by Author.

As seen from the profile, the rate to binder burnout went from 2.0°C/min to 6.0°C/min and the rate from burnout to sintering went from 6.0°C/min to 2.0°C/min. The result is a sintered structure that is free from cracking and warping and has a throughput of almost 80%. It is also shown that the structure is also 40% smaller than the original inductor.

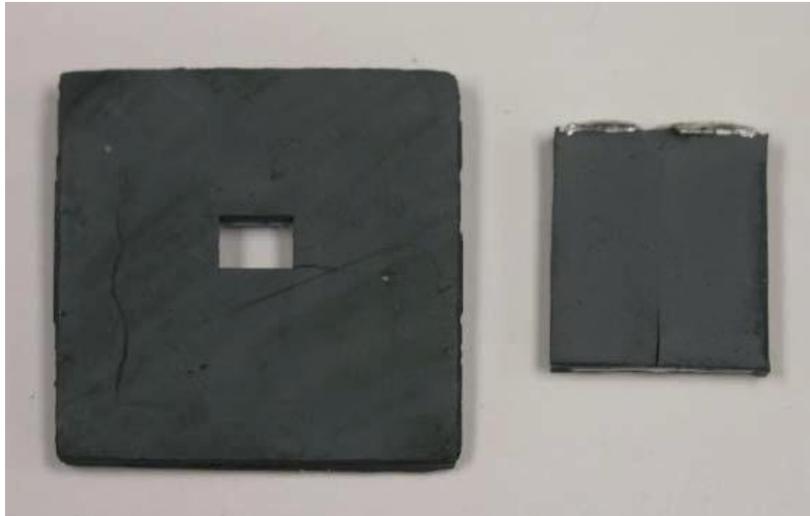


Figure 2.25. Generation 1 (Left), Generation 2 (Right). [17]

2.2.9 Characterization of Inductor

Now that the inductor is successfully sintered, we have to verify that the structure is still electrically verifiable compared to the same inductor with ESL paste. We need to know if the gas channels affect the inductance of the structure. Using the same procedure as before, the two structures are measured versus current. The graph of the results is shown below. The blue line represents the inductor with the gas channels and the pink line is the inductor that has ESL paste. It is shown that there is very little difference between the two. This was expected as the gas channels are parallel to the flux pattern and the simulation verified that there was little inductance contribution in the ends. The DCR was also measured as above and used the conductivity number that was found.

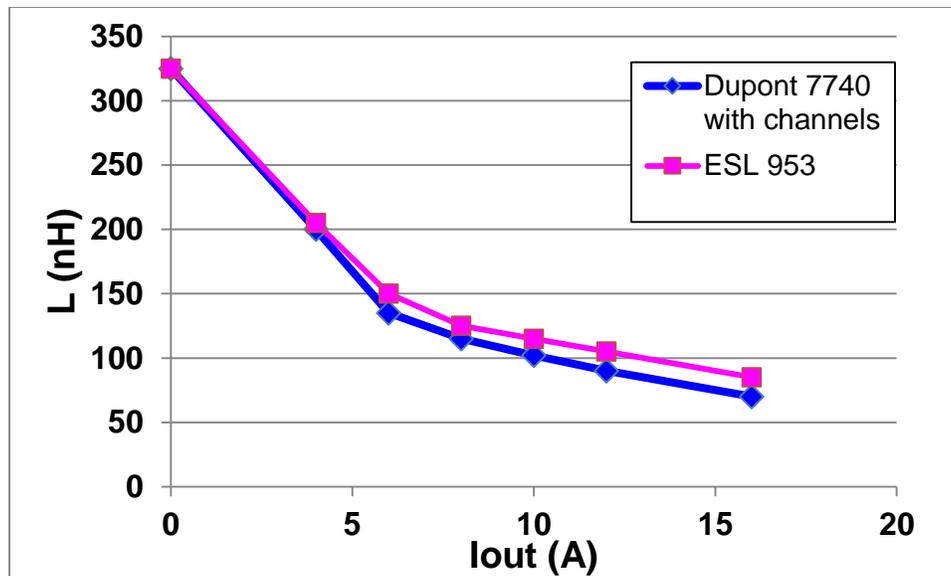


Figure 2.26. Graph of Inductance vs. Current for Structure with and without gas channels. Image by Author.

Another graph shows that the change in tape permeability increases the non-linearity of the inductor. The generation 2 inductor is graphed against the generation 1 inductor and against the standard discrete inductor. It suffers very little at heavy load but gives a much higher inductance at light load.

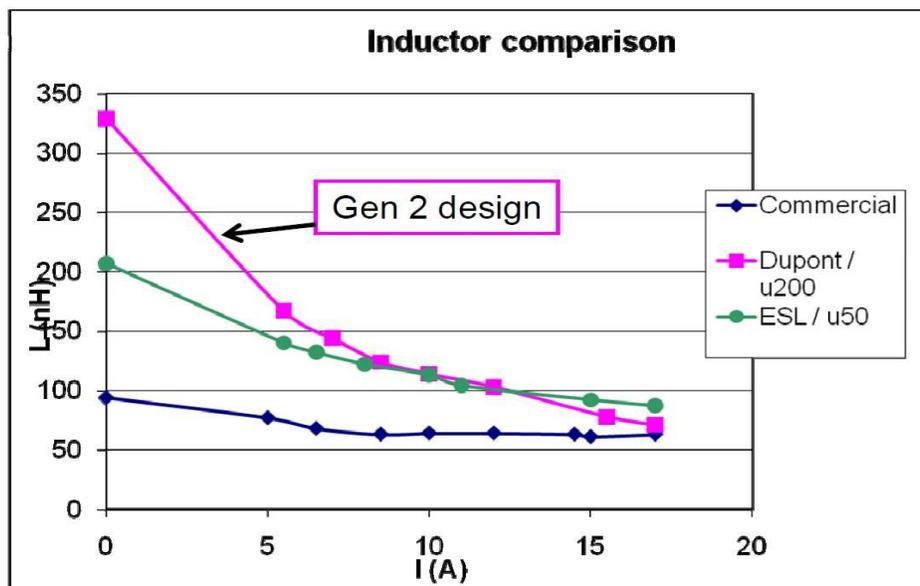


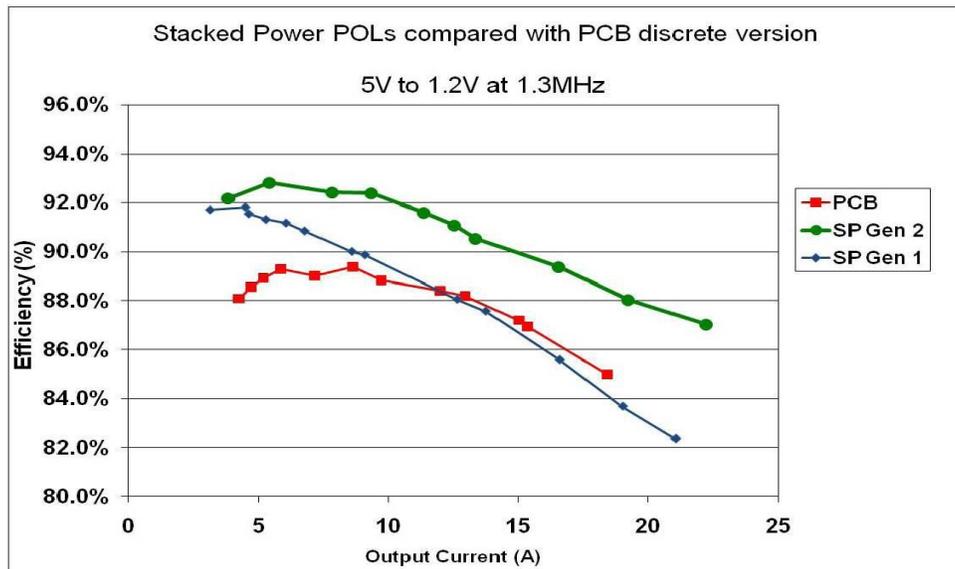
Figure 2.27. Graph of Inductance vs. Current for various inductors. Image by Author.

Table 2.4. DCR findings for each generation inductor

	DCR
Generation 1	2m Ω
Generation 2 ESL	1.1m Ω
Generation 2 DuPont	0.37m Ω

2.2.10 Converter Results Showing Improvement From Inductor

We have seen that the Generation 2 inductor meets the inductance requirements at heavy load, decreases footprint, and lowers the DCR compared to previous generations. The key to all this work though is how it actually performs in circuit. The hope was to increase the overall efficiency of the converter. The inductor was attached to the same active layer as the Generation 1 inductor to give a fair comparison. The active layer will be discussed in Chapter 3 of this thesis.



change	η	$\Delta \eta$
Gen 1	85.0%	----
Change inductor design	87.5%	2.5%

Figure 2.28. Graph of Efficiency and Percentage Table for Generation 2 inductor compared to previous inductors [17].

The Generation 2 inductor was very successful in improving the overall efficiency of the converter. The efficiency increased across the whole load graph especially in the heavy loads. The table shows that the inductor itself contributes an increase of 2.5% to the efficiency. The heavy load efficiency benefits especially from the change in conductor material and the subsequent lowering of the DCR.

2.3 Coupled Inductor For 2 Phase Stacked Power POL

Since the process was successful using the DuPont paste with the ESL tape, a coupled inductor was proposed at CPES to take advantage of these materials [18]. The following section will discuss the process changes that were made to fabricate such a structure. This work was done in conjunction with Arthur Ball and Yan Dong.

2.3.1 Background

As discussed in the introduction, the POL industry is moving to multiple phases to supply the necessary current levels to microprocessors. There is also the other side of the problem which is the push for miniaturization, mainly with the inductor. One way to address both issues is to couple the inductor between 2 phases for example in order to keep the inductor footprint small.

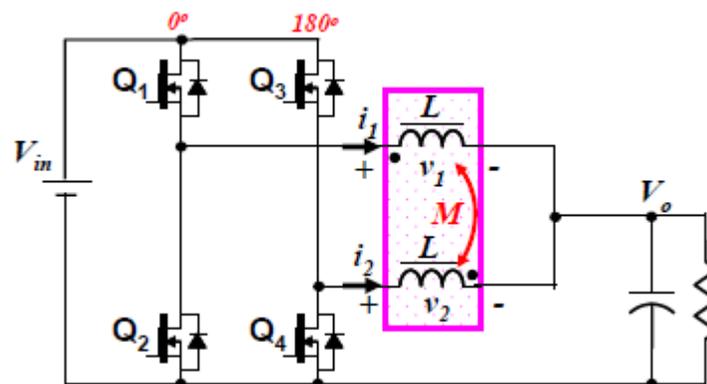


Figure 2.29. Two phase coupled inductor buck circuit [18].

While the theory is discussed in multiple dissertations [17],[18], the aim here is how to apply what we learned with the LTCC inductor process to fabricate this type of structure. The essential idea is that inverse coupling cancels the flux in the outer legs which in turn minimizes the structure footprint.

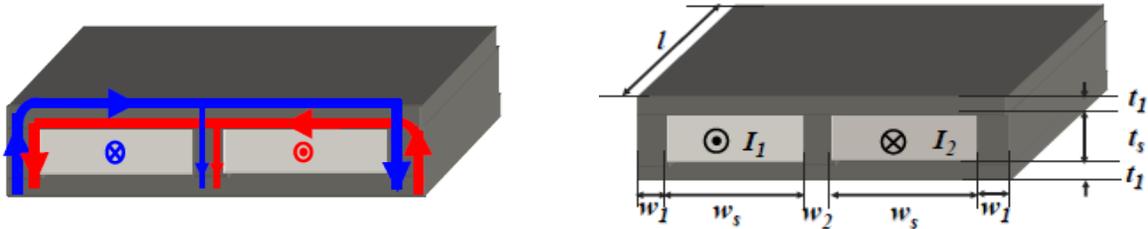


Figure 2.30. Inverse coupling concept for the coupled inductor(Left), Structure design parameters (Right) [18].

The structure parameters are shown above in Figure 2.30. The active layer footprint that the inductor was designed to mimic was 9x23mm. So this sets the length value initially. The w_2 value is what sets the coupling coefficient α . This design was striving for a coupling coefficient of 0.6 where perfect coupling has a value of 1 or essentially creating a transformer. The inductor current is set to be 20A. The main concern from a process standpoint is the w_1 and t_s value. Obviously the total width could only be 9mm so we knew going in that the w_1 values were going to be small in order to keep the w_s value high enough to handle the 20A current. This poses a problem since we saw from the Generation 2 inductor that the outside width had to be large enough surface area wise to hold the structure together during sintering. Another issue again has to do with the current handling capability of the inductor. The t_s value also has to be larger because of the small footprint. This was going to push the theoretical thickness limit of the LTCC process.

The final design was based on the smallest thickness and volume that could be achieved while keeping the inductance sufficiently high and the coupling coefficient near 0.6. This led to $w_1=1\text{mm}$, $w_2=1\text{mm}$, $w_s=1.5\text{mm}$, $t_1=0.7\text{mm}$, $t_s=2\text{mm}$, and $l=20\text{mm}$. So the total thickness was to be 3.4mm or 20% bigger than the Generation 2 inductor. The next section will discuss how to fabricate the structure.

2.3.2 Fabrication Compared to Single Phase Inductor

Taking into account the t_s value, it is double that of the Generation 2 inductor. As we have seen in section 2.2, gas channels were added to the structure to assist with binder burnout and pressure relief during sintering. So we went about fabricating this structure the same way with differing results. The design was changed slightly from the previous inductor in that there are 3 gas channels on each side. The sintering process remained the same.

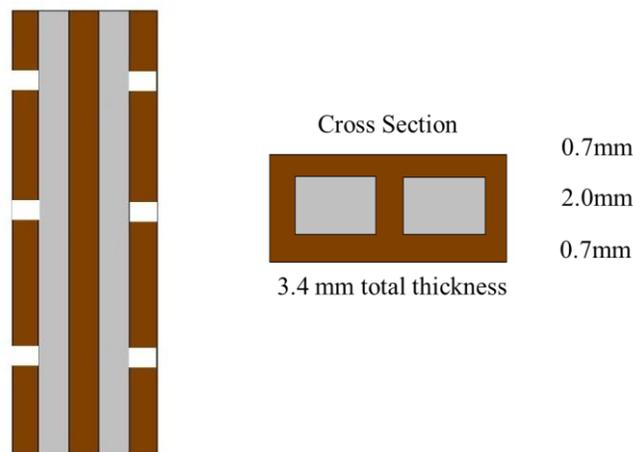


Figure 2.31. Concept drawing for the coupled inductor $w_1=1\text{mm}$, $w_s=1.5\text{mm}$, $w_2=1\text{mm}$, $t_s=2\text{mm}$, $t_1=0.7\text{mm}$. Image by Author.

The sintering results were initially very poor. There is not widespread cracking as we had in the generation 2 inductor, but issues with de-lamination between layers. The belief is that the large volume of conductor paste embedded in the structure was the cause. The gas channels

were not sufficient enough to allow adequate binder burnout and pressure relief so the pressure was forcing its way between the layers especially between the top and middle layers.



Figure 2.32. Top View and Side View showing de-lamination [18].

Therefore, it was proposed to add additional measures to assist with the process. Small vias were drilled through the top layer during laser cutting of the green tape. Also, vias were drilled through the entire middle leg in the same manner. The de-lamination forced the outer legs to also be widened. The outer leg, w_1 , went from 1mm to 2mm and the total width was now 8mm instead of 6mm. The conceptual drawing is shown below.

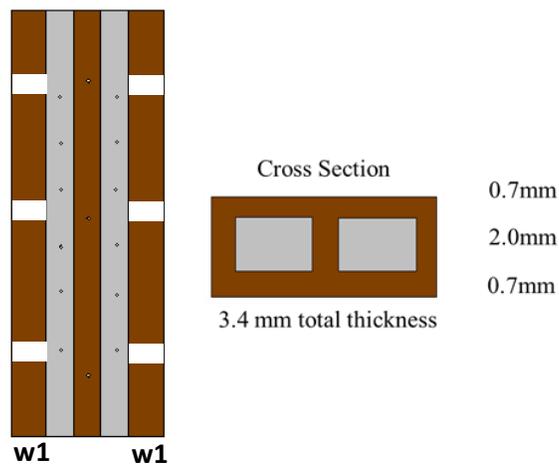


Figure 1.33. Improved Concept- Top View (Left), Cross Section (Right). $w_1 = 2\text{mm}$, $w_2 = 1.5\text{mm}$, $w_s = 1.5\text{mm}$, $t_s = 2\text{mm}$, $t_l = 0.7\text{mm}$.
Image by Author.

The sintering results with the incorporated top gas vias were promising. Figure 2.39 shows how the de-lamination is very slight with some very slight warping. The throughput for this type of structure was still very low at 15-20%. No matter what else was done with this structure it still did not result in many successful prototypes.

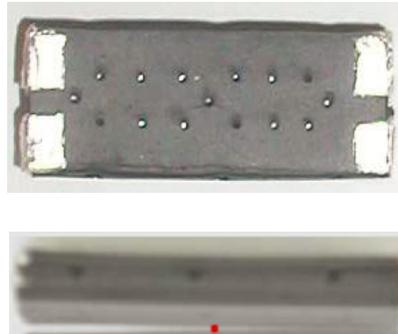


Figure 2.34. Top view and Side View of Prototype [18].

2.3.3 Results

Although the fabrication of the coupled inductor proved to be difficult, the results prove the concept that the inductor can be miniaturized while keeping adequate inductance. It is shown below that there is a significant reduction in size compared to the single phase inductor.



Figure 2.35. Reduction of footprint from 2 non-coupled inductors to coupled inductor [18]

It is also shown that the coupled inductor gives higher light load inductance while keeping the heavy load inductance similar to 2 non-coupled inductors. This allows for faster transient speeds in the light load range and keeps sufficient inductance at heavy load to control the ripple.

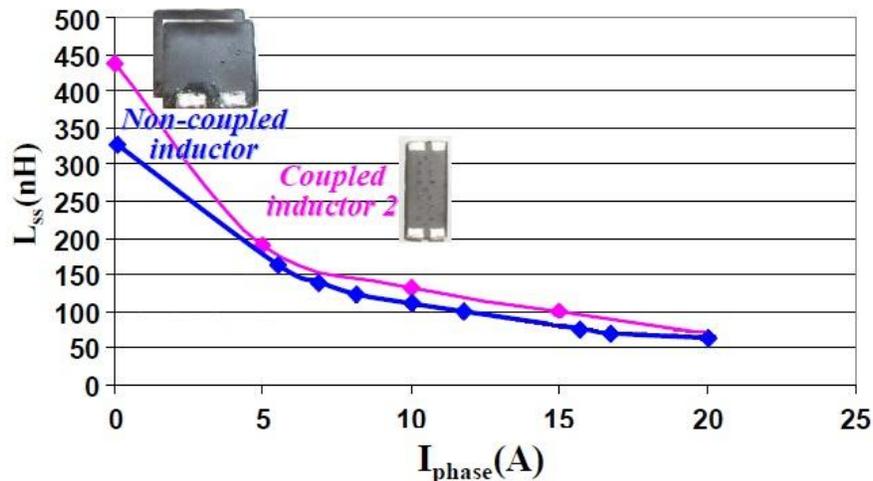


Figure 2.36. Inductance vs Current for coupled and non-coupled inductors [18].

2.3.4 Challenges to Future Vertical Flux Inductors

It is shown that vertical flux inductors can be fabricated successfully. Thickness can be pushed even beyond theoretical limits in literature. The problem is the throughput when a thickness of 3.4mm is to be achieved. The throughput for the Generation 2 inductor at 2.7mm is around 80%. The coupled inductor only had a throughput of 15-20%. It was found to be very difficult to process that structure. The challenge is how to continue to successfully process inductors beyond a thickness limit of around 3mm. Another way to handle the challenge is to change the methodology for the design of the inductor. The next section will discuss the change to the lateral flux inductor topology which eliminates the need for large thickness to achieve adequate inductance.

2.4 Magnetic Substrate with Lateral Flux Pattern

As seen in the previous sections with the vertical flux inductor designs, thickness is proving to be a roadblock that is stopping the move to higher power density. Although the power density went from $50\text{W}/\text{in}^3$ with the generation 1 design to $500\text{W}/\text{in}^3$ with the coupled inductor design, the full potential of the integrated 3D converter had not yet been reached. Therefore it was proposed at CPES to move to an inductor with a theoretically different flux pattern – the lateral flux inductor [14] [27] [28]. This work was done with Qiang Li.

2.4.1 Background

The fundamental idea of the lateral flux inductor is the change in the flux pattern. Instead of the flux being perpendicular to the substrate as in the vertical flux inductor, it would now be parallel to the substrate. This structure has multiple benefits to the integrated converter. First, the core height is no longer a slave to the embedded conductor height which allows for a thinner core design.

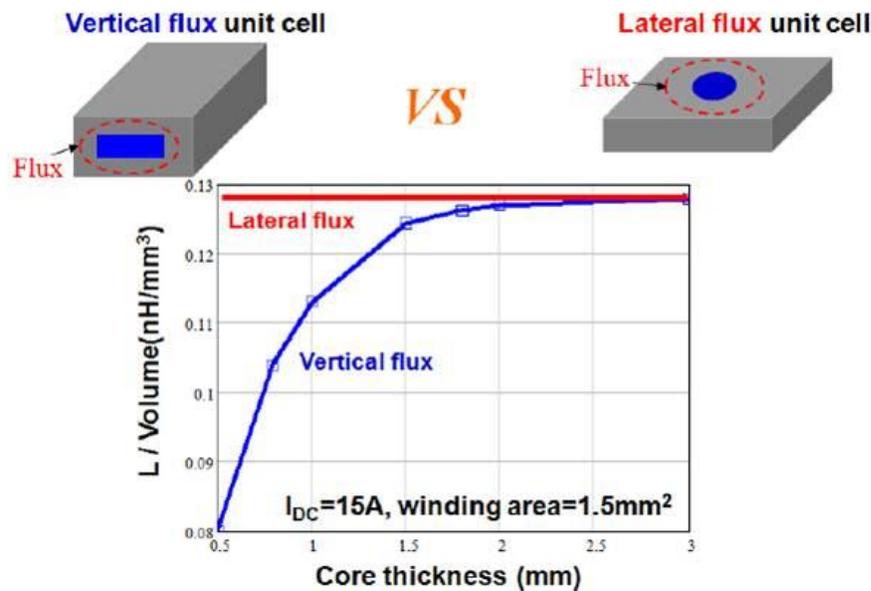


Figure 2.37. Inductance Density vs. Core Thickness for Vertical and Lateral Flux Cells [14].

Second, the magnetic interference is reduced as the flux is also parallel to the active layer above the magnetic substrate. Third, the inductance density of the lateral structure is much better than that of the vertical structure, especially at smaller core thicknesses.

2.4.2 Fabrication Process of Lateral Flux Inductor

Since the lateral flux structure is inherently different than the vertical flux structure, we have to investigate the changes in fabrication. The vertical flux structure includes multiple layers to build up the embedded conductor structure. The lateral flux structure does not embed a conductor so the layering can be a singular structure. But the laser cutting effects have to be considered and handled to efficiently and successfully fabricate the inductor. The following sections will discuss the changes in fabrication to build the lateral flux inductor with basis in the vertical flux structure.

2.4.2.1 Laser Cutting Effects on LTCC Tape

The LTCC tape being a soft material is drastically affected by using a laser to cut the material as is seen earlier in the chapter. This structure would benefit more in production as via punching is better for a uniform via wall. Although, research prototyping is much easier with a laser as tooling is not needed.

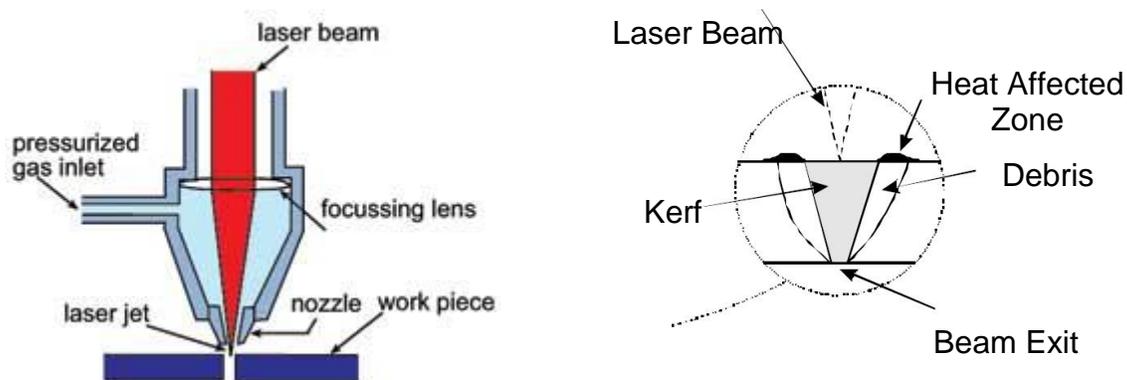


Figure 2.38. Conceptual Drawings of Laser Focusing (Left), and Laser Beam Effects on Material (Right)

It can be seen that the laser is essentially burning the material so there is material loss that must be considered in the design. Also, the thickness of the material will greatly impact the verticality of the via wall. The next section will discuss ways to mitigate some of these effects.

2.4.2.2 Layer Groupings to Reduce Impact of Laser Cutting

Let's consider that we have many sets of layer groupings of LTCC tape that need to be cut using a laser. We will have sets ranging from 2 pressed layers up to 20 pressed layers. How will the laser affect these layer sets. The prediction is that the laser has little effect on the thin layers while the thick layers will be greatly affected. Samples were fabricated to make measurements to back that prediction. The sample layers had a series of 1.5mm vias cut in them and the final via size was measured to find the cutting loss. Also, the via was measured at the top and bottom surface to find how much taper occurs for that given layer grouping. The graph below shows the results.

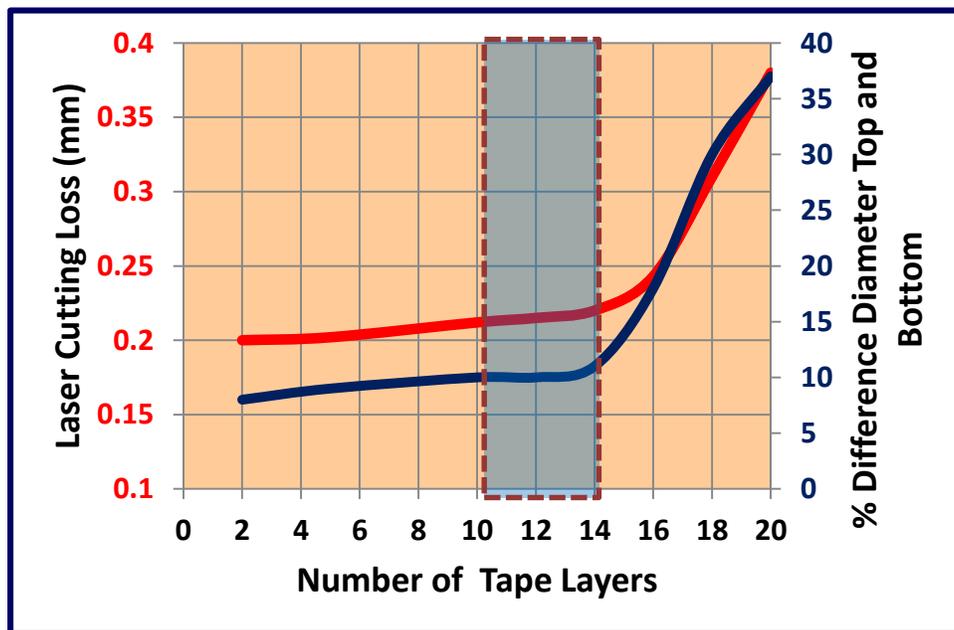
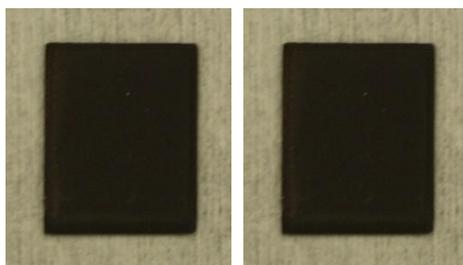


Figure 2.39. Graph showing laser cutting loss in red and the kerf taper in blue. Image by Author.

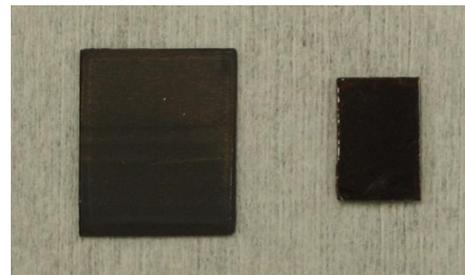
There is an optimal layer grouping range in the graph. It is better to press 10-14 layers together before cutting as it is almost the same as using 2 layers. This will help prototype processing time as you will only have to have 2-3 groups of layers as opposed to pressing and cutting each individual layer. Based on all this data, it is found that the spacing between the vias has a minimum of 0.4mm, which was used in all the designs.

2.4.2.3 Process and Sintering

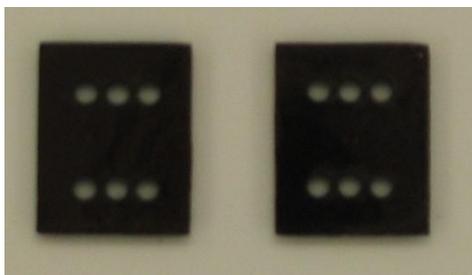
Now that the laser effects are known, the process is very similar to the vertical flux inductor. It starts with blank laminates which are covered in a kapton tape. Those are trimmed down to size as before to create a smooth edge. Then the vias are cut and the complete structure is laminated again using the reduced pressure. Then the DuPont silver paste is printed and dried in the vias and the structure is sintered using the same improved sintering profile in Figure 2.28.



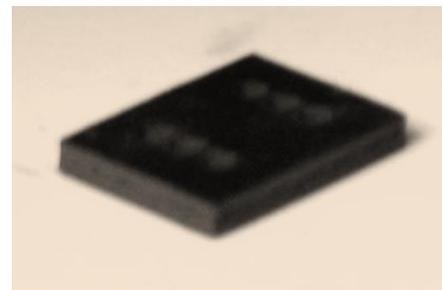
Blank Laminates



Blanks cut to size



Laser Cut Pattern



Second Stage Lamination

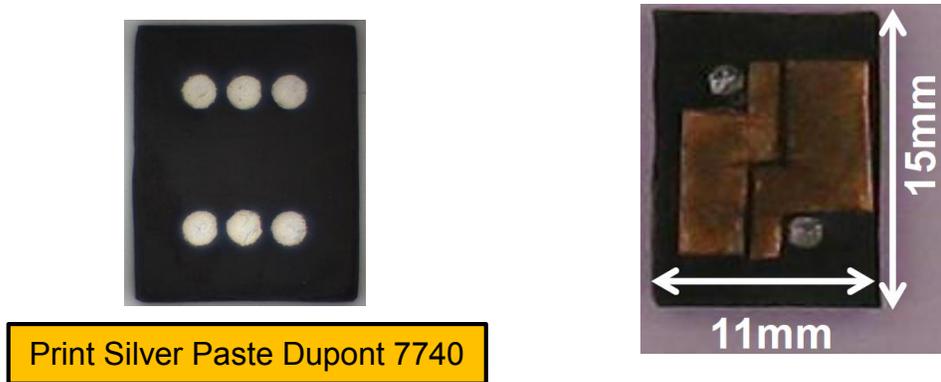


Figure 2.40. Process to fabricate lateral flux inductor and the result with copper connections. Images by Author.

2.4.3 Results

The results show prove that the calculations in Figure 2.37 are correct, the smaller lateral flux inductor can result in larger inductance. The key is that this structure can use a thinner profile compared to the vertical flux structure. This would lead to increased power densities for 3D integrated converters.

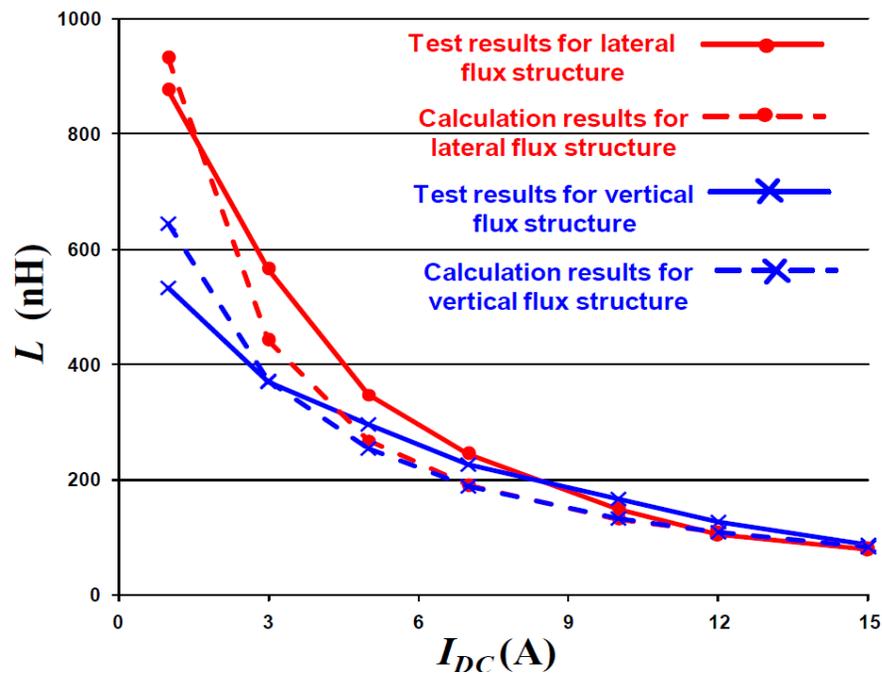


Figure 2.41. Inductance Test and Calculation Results for Inductor prototypes [14].

2.5 Conclusion

In this chapter, the discussion is centered on the 3D integration concept more specifically on the passive layer fabrication. The previous work found that the active layer must be shielded from the magnetic substrate in order to reduce parasitic ringing and increase efficiency. All the inductor designs from that point were for an integration scheme with the active layer. The first design yielded a large footprint and a large DCR which killed efficiency at heavy load. The redesign was aimed at reducing the footprint by changing to a higher permeability tape and decreasing DCR by changing to a pure silver conductor paste. The footprint was reduced by 40% and the DCR was reduced from $2\text{m}\Omega$ to $0.37\text{m}\Omega$. This increased the power density from $50\text{W}/\text{in}^3$ to $250\text{W}/\text{in}^3$ and increased the efficiency by 2.5% alone. The material mismatch issues were solved by introducing gas channels in the structure to allow for better binder burnout and pressure relief.

The vertical flux structure was also used to create a coupled inductor which was utilized in a 2 phase design. The footprint was further reduced by 50% over a non-coupled version while keeping the same inductance, converter efficiency, and increasing the power density to $500\text{W}/\text{in}^3$. The vertical flux structure had reached its limits at this point with a 3.4mm thick structure. A proposal was made to switch to a lateral flux inductor structure which could theoretically increase inductance density especially at thinner core thicknesses. The result is a smaller footprint which could lead to much higher power densities. The next chapter will look at how the active layers were formed and how the passive layer designs helped push the power densities higher.

Chapter 3: Point of Load Converter Active Layer Packaging

3.1 Background and Previous Work

This chapter is dedicated to the study of fabricating the active layer for the 3D integrated converter. As shown in Chapter 1, there is a need to isolate the power devices from the magnetic substrate to prevent excessive ringing which destroys efficiency. The question is what type of substrate to use in order to do this. Traditionally, in industry, an FR-4 material is used because of the low cost associated with it. This entails putting in a ground layer internally which protects the devices from interference. But the drawback is the very poor thermal conductivity that FR-4 has. This chapter will discuss the use of Direct Bond Copper (DBC) substrates as a thermal alternative to FR-4 PCB. While it does cost more, the high temperature benefits outweigh that cost.

3.1.1 Stacked Power Packaging for Thermal Considerations

A proposal was made at CPES to try to achieve double sided cooling of power devices embedded in a ceramic substrate [17]. Traditional PCB designs include packaged power devices which only allow single sided cooling as the thermal resistance to air is high, essentially pushing all the heat into the board or to a heat sink if present.

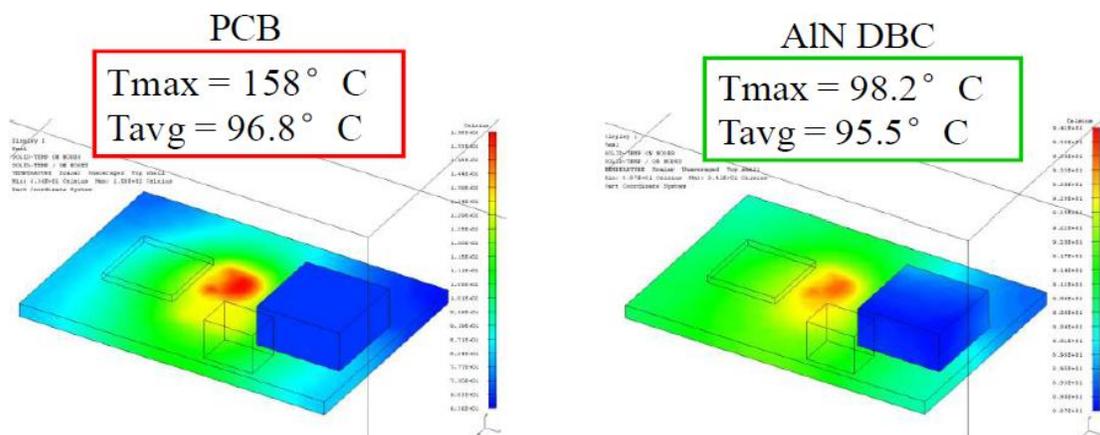


Figure 3.1. Thermal Simulations of PCB (Left) and DBC (Right)

FR-4 having very poor conductivity means heat spreading is only limited to the presence of copper in the form of circuit traces. This limits the ability of PCB designs to spread heat and creates hot spots in the board as evidenced in Figure 3.1. The idea behind stacked power is to create multiple avenues for the heat to travel away from the device. The FR-4 thermal conductivity is 0.35W/mK where ceramics such as Alumina can offer $25\text{-}30\text{W/mK}$ and can dramatically improve thermal management in the substrate. The DBC acts as a heat spreader which also reduces the volume of the converter and improves power density by removing the need for a heat sink.

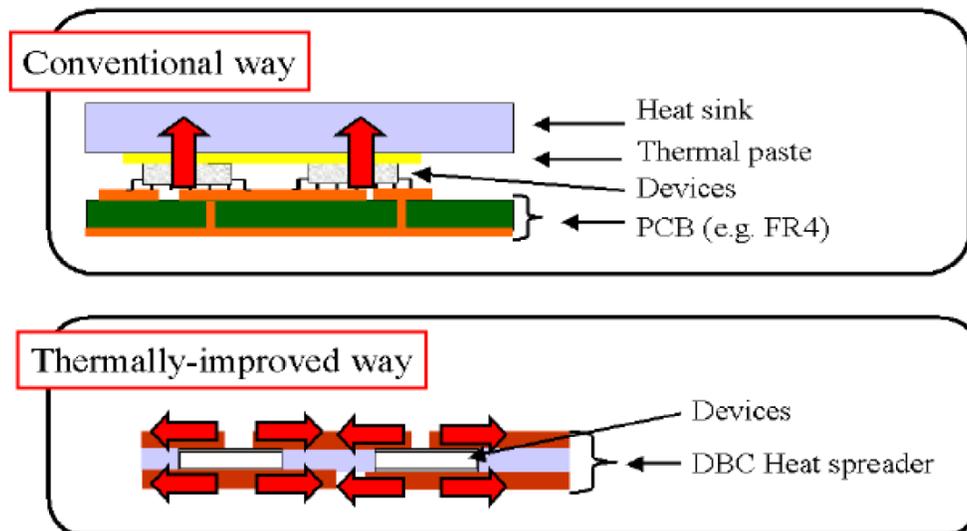


Figure 3.2. Traditional Thermal in PCB (Top), Stacked Power (Bottom)

Another key to the stacked power idea is the elimination of wire bonds for device connection. All connections become planar as the devices are embedded in the substrate which exposes both sides of the device. This, in addition to helping thermally, reduces parasitic inductances that come with wire bonds by using copper straps. Embedding the devices in a ceramic substrate also creates better heat spreading which allows for higher current operation or a smaller footprint.

3.2 Stacked Power using Silicon Devices on DBC

The stacked power idea is built on the use of Direct Bonded Copper which is supplied by Curamik which is now a division of Rogers Corporation [29]. As seen in the introduction, the DirectFET by IR is a good choice of device for this particular application [30]. The device has two source pads and one gate pad on top with the whole bottom being a drain pad. Typically the DirectFET has an attached ‘can’ for the drain so the device can be surface mounted on a board. But in our case the device will be embedded which means both sides need to be accessible. IR sent us an unpackaged form of the device without the can.

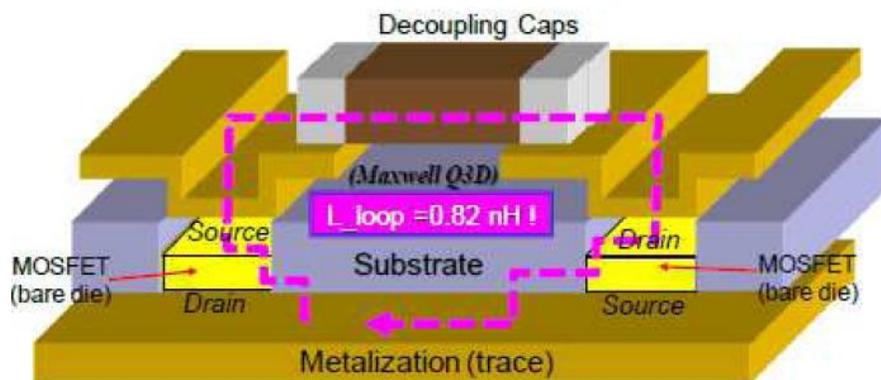


Figure 3.3. Concept drawing showing the packaging structure of a stacked power converter

The devices are placed as to find a minimum value for the loop inductance. It can be seen that the left device has the source and gate oriented up while the right device is flipped. The smaller loop inductance leads to less ringing at the switch node of the converter. Less ringing means less loss which in turn means less heat generation. So the thermal and electrical aspects of the converter design go hand in hand. The figure below shows a comparison of ringing with different loop inductances. Even just a modest reduction of 30% of the loop inductance creates a huge difference in performance.

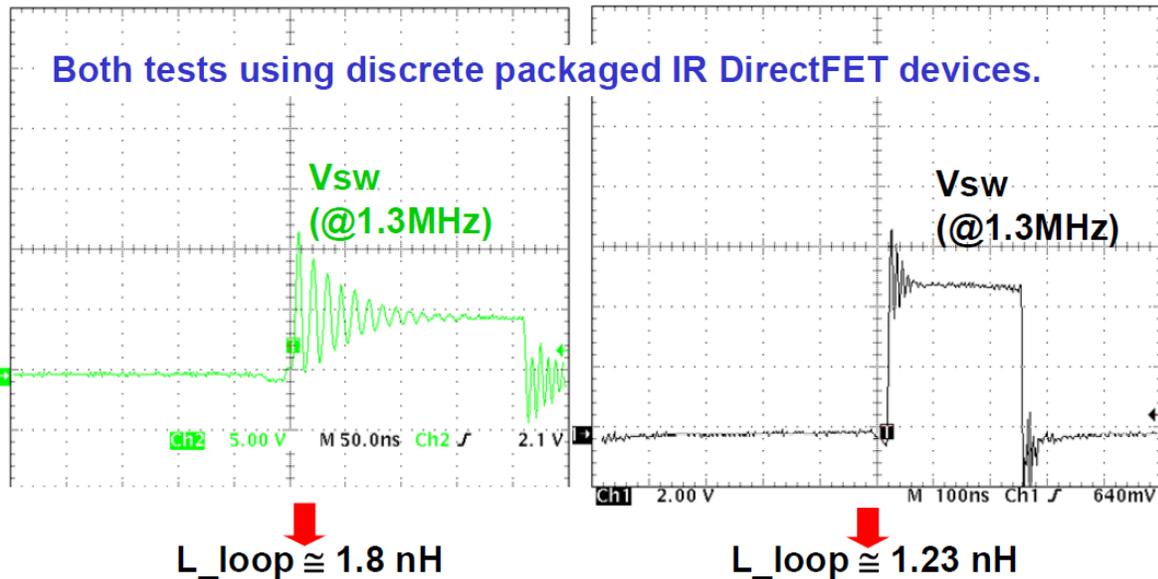


Figure 3.4. Effect of loop inductance on converter performance. Comparison made with two different PCB layouts [17].

The placement of the input decoupling capacitor becomes an important key to higher efficiency with this structure. The ideal case is the capacitor being placed directly on top of the switches to minimize the loop inductance. The simulation in Figure 3.3 shows that the loop inductance can be 0.82nH if the cap is directly on top. The design will include this factor.

3.2.1 Laser Cutting Parameter Development

The first step in fabrication is to develop the laser cutting parameters for cutting the ceramic substrates. This particular converter design was using Aluminum Nitride DBC which carries a high thermal conductivity value of 150 W/mk. That can prove to be very difficult to cut using a laser machining system which uses heat to cut through the sample. Blank samples of Aluminum Nitride were used to develop the laser cutting parameters. The substrate itself is 15 mils thick so samples of similar thickness were used. The development follows the same path as we did in Chapter 2 with the green ferrite tape.

It is found that the power, the pulse number and the pulse spacing are the only differences from cutting the ferrite tape. To cut the 15 mil thick ceramic, the power needs to be 75-80W while the pulse number has to be 500-600. The pulse spacing needs to be 0.0004 inches. Even with these high values, multiple passes have to be made to cut completely through the substrate. Another factor that didn't have to be considered with cutting the green tape is the cooling air. The laser system has an air system that is used to cool the sample during cutting. This must be set fairly high to prevent the ceramic from cracking from high localized heat.

3.2.2 DBC Fabrication Process

3.2.2.1 Card Preparation

The first step in the fabrication process is to cut blanks out of the 5" x 7" DBC card. The card is covered in kapton tape and then sections of tape are cut out to expose the copper. That copper is etched away using a ferric chloride wet etcher so the laser can have access to the ceramic. Using the laser parameters from above, the card is cut to leave 2 pieces for active layer fabrication.



Figure 3.5. DBC Card masked with kapton tape (Left), copper etched (Middle), laser cut (Right). Images by Author.

3.2.2.2 Circuit Layout

The cut pieces of DBC are now ready to send to the laser to cut the circuit pattern for the converter. This part can be tricky as the alignment is the key for the whole fabrication. If the alignment is off by even a millimeter, the stacking of the two layers becomes very difficult. There are pins that make connections between the two layers so the alignment must be fairly exact. The way to do this is to set an artificial origin based on measurement. Marks are made on

each side of the DBC piece to be used later in the laser alignment. For example, an origin is set at 5mm in and 5mm up from the bottom corner of the ceramic. The piece is then flipped and the same measurements are made from the same reference corner. Another key is to understand how much the optical alignment of the laser is off. The camera can be bumped which causes the optical origin to be different from the mechanical origin; this offset must be compensated for. The pieces are then ready to be sent to the laser for the circuit pattern to be cut in the kapton masking. While the ceramic needs 80 W of power to cut, the kapton only requires 2 W to cut the mask. The design was drawn in AutoCAD and the layer designs are shown below.

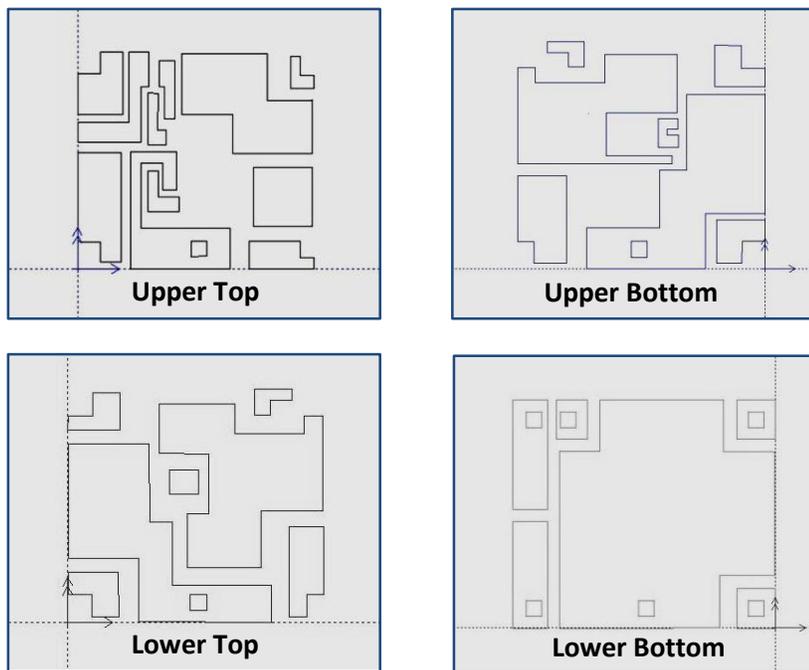


Figure 3.6. AutoCAD Drawings for Gen 2 Active Layer. Images by Author.

It can be seen that the devices are embedded in the upper layer with the lower layer used for making electrical connections and having large ground planes. The lower top layer includes

a ground plane running underneath the driver. Once the masking is cut, the extra tape is removed and the pieces are ready for wet etching.

3.2.2.3 Wet Etching

Wet etching is done with a bench top etcher filled with ferric chloride used for copper etching. The model shown below is the Kepro BTD 201B (now owned by Dalpro) which allows the sample to be suspended while the pump system sprays it. There must be fluid movement across the sample to effectively etch the copper, the sample cannot just be submersed in the fluid. The etching occurs at about 1 mil per minute depending on the fluid temperature and the freshness of the fluid. A cold fluid or a fluid that is saturated with copper will dramatically decrease the etching rate. Based on a fresh fluid, the resolution that can be achieved for an 8 mil copper cladding is around 0.3 mm between features and 0.3 mm trace width. Careful attention must be paid during etching as any extra time left in the fluid will effectively begin to remove narrower traces. Once the etching is completely, a thorough rinse cycle with water is needed.



Figure 3.7. Kepro Bench Top Etcher. Image by Author.

3.2.2.4 Laser Cutting and Device Placement

Now that the etching is complete, the DBC goes back to the laser machine. Since the copper has been removed, the slots for the devices and the vias can be cut in the ceramic. The devices that are used are the IRF6633 for the top switch (2 x 2.6 mm x 10mils thick) and the IRF6691 for the bottom switch (3.4 x 4 mm x 10mils thick). The laser cutting parameters were shown above for cutting the ceramic. The figure below shows the progression of the process.

The top active layer is shown as the example.

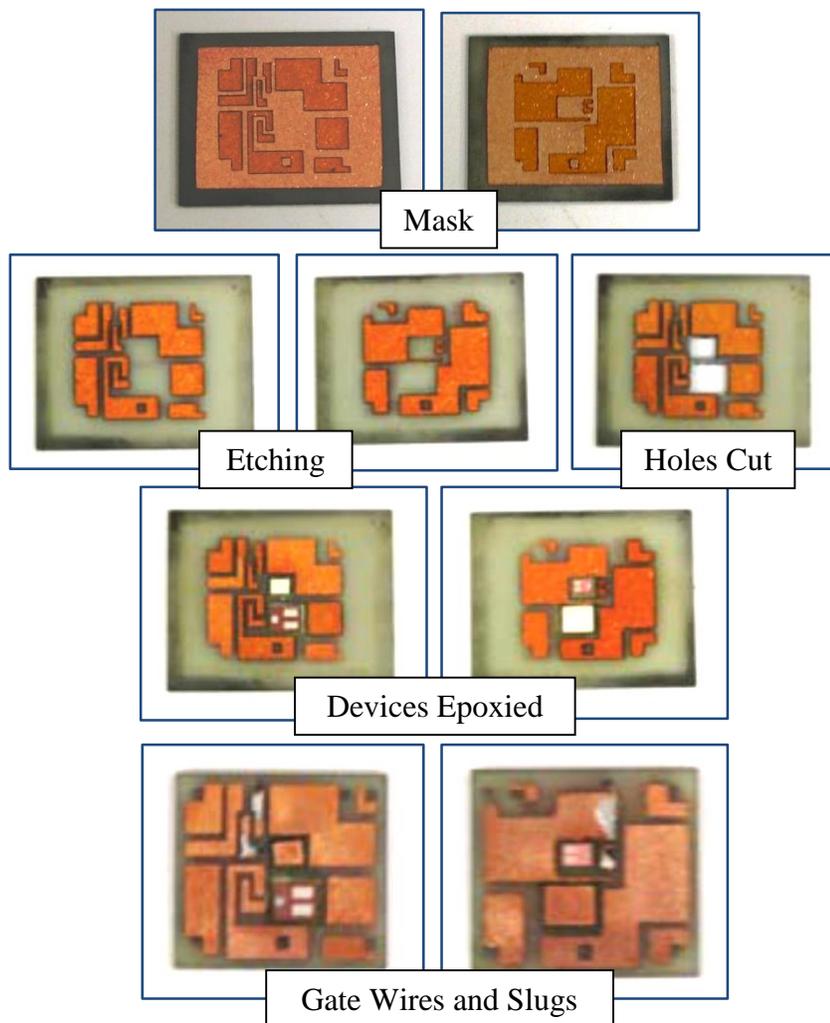


Figure 3.8. DBC process for Generation 2 Buck Converter. Images by Author.

The devices are epoxied in place using EP3HT which is made by Masterbond [31]. A kapton tape layer is placed over the traces of the circuit on one side first. This will create a flush surface for the device to the traces. The device is placed onto the adhesive of the kapton tape within the ceramic well. The epoxy is then applied to the gap between the ceramic and the device with a syringe. Air bubbles must be removed using a small pin or the like as they will burnout during curing and create a gap which destroys the integrity of the bond. The board is then placed in a furnace (same furnace as used in Chapter 2 for sintering of LTCC tapes) and a curing cycle is initiated. The curing temperature is 150°C for 7 minutes with a ramp rate of 10°C/min and natural cooling. It takes around 30 minutes per device. The bottom switch is placed in the same way as the top switch.

Taking into consideration that the devices are 10 mils thick and the substrate with traces is 31 mils thick, copper slugs are used to fill the gap between the device and ceramic. These slugs are soldered to the drain of each device so that it is planar to the traces on the other side. It works out to use 2 x 8 mil copper pieces along with solder paste between to build up the thickness. The figure below is a concept drawing for the structure. The epoxy is shown in blue, the devices are pink, the copper traces are brown, the solder paste is silver, and the slugs are light brown.

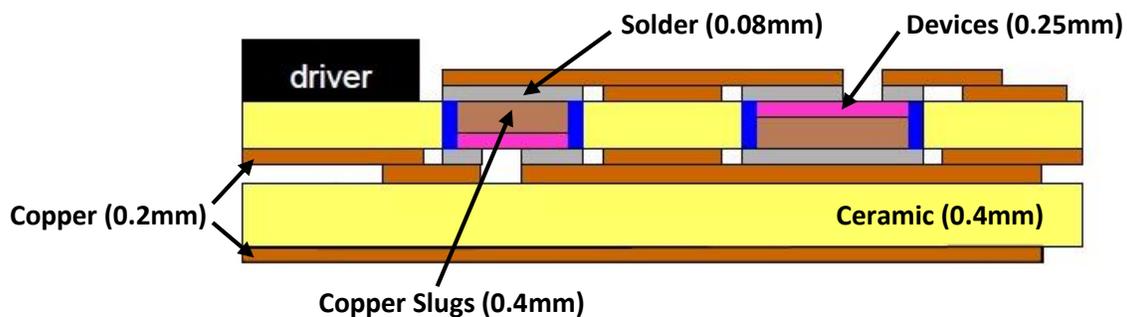


Figure 3.9. Schematic of the DBC structure with embedded dies [17].

The solder paste used in this assembly is a low temperature 43Pb/43Sn/14Bi. The lower temperature paste is used to keep the reflow temperature below the breakdown temperature for the devices. While the inclusion of the Bismuth is intended to lower the liquidus temperature at 163°C, it does have lower creep resistance than the traditional eutectic paste. The benefits outweigh this by giving low temperature and good fatigue properties [32]. The paste can be brittle when used in high quantities which could impair reliability. This paste is used to solder the copper slugs to the devices as well as the SMT components to the board. The gate wires are placed and soldered to prepare for the other DBC layer.

Once the slugs are in place, the additional DBC layer is soldered to the active top layer by using the profile shown below [33]. We used the Sikama reflow belt to achieve the stages needed for the solder paste. The preheat temp is set at 120°C, the soak temp is 160°C, the reflow stage temp is set at 200°C, and cool down goes from 160°C to 120°C to natural cooling at the final stage. The belt is set to move 15 in/min. The temperatures include the loss to the air that occurs with an open belt.

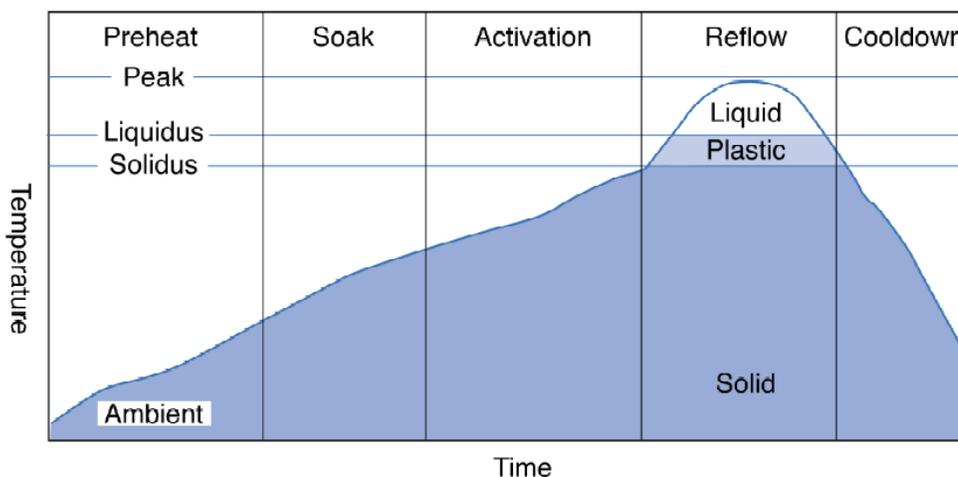


Figure 3.10. Solder Reflow Profile provided by EFD Nordson for 43/43/14 solder paste. From datasheet.



Figure 3.11. Sikama Reflow Belt. Image by Author.

Now that the 2 layers of DBC are soldered together, the SMT components are ready to be attached. This design includes an LM27222 driver from National [34], a bootstrap capacitor (0.33uF MLCC), a diode (16V B3K), an input capacitor (22uF MLCC), and an output capacitor (100uF MLCC). Copper straps are also placed to connect the top switch gate and source pads to the board. The low temperature solder is used as before and follows the same profile. The reflow temperature also affects these parts as the interconnection thermal resistance is low so the parts will see higher temperature more than a PCB application. A pause is needed at the peak temperature as it allows the high percentage of organics in the paste to burn off and keep voids at a minimum.

3.2.3 Results

The figure below shows the complete Generation 2 active layer along with the Generation 2 inductor that was discussed in Chapter 2. This layout with active and passive layer increased the power density from 50W/in³ in Generation 1 to 250W/in³ in Generation 2 through improved packaging techniques.

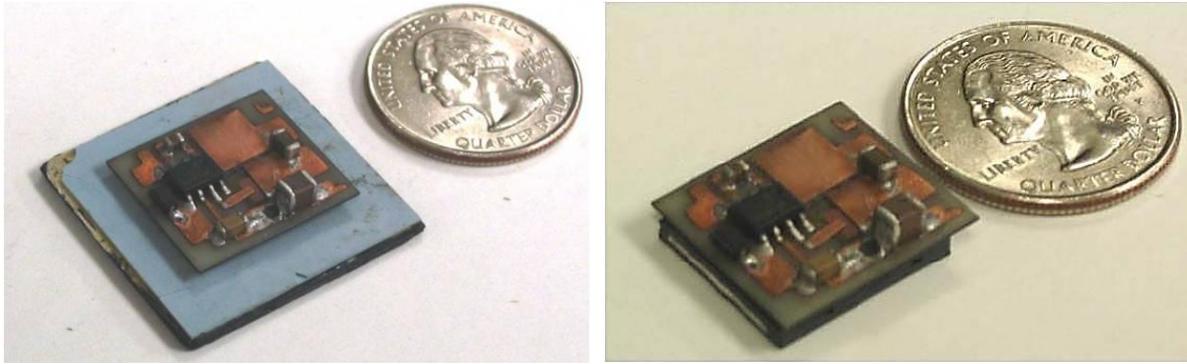


Figure 3.12. Generation 1 Converter (Left), Generation 2 Converter (Right) using Stacked Power Techniques and LTCC Inductor

The key to the Generation 2 converter is the inclusion of the improved LTCC Inductor. Otherwise the circuit layout is essentially the same. With the new inductor, there was an improvement of 2.5% in heavy load efficiency due to the much improved DCR. Overall the converter is much better across the whole range of output current compared to Generation 1 and the state of the art PCB. The next section will discuss the thermal analysis of the Generation 2 design.

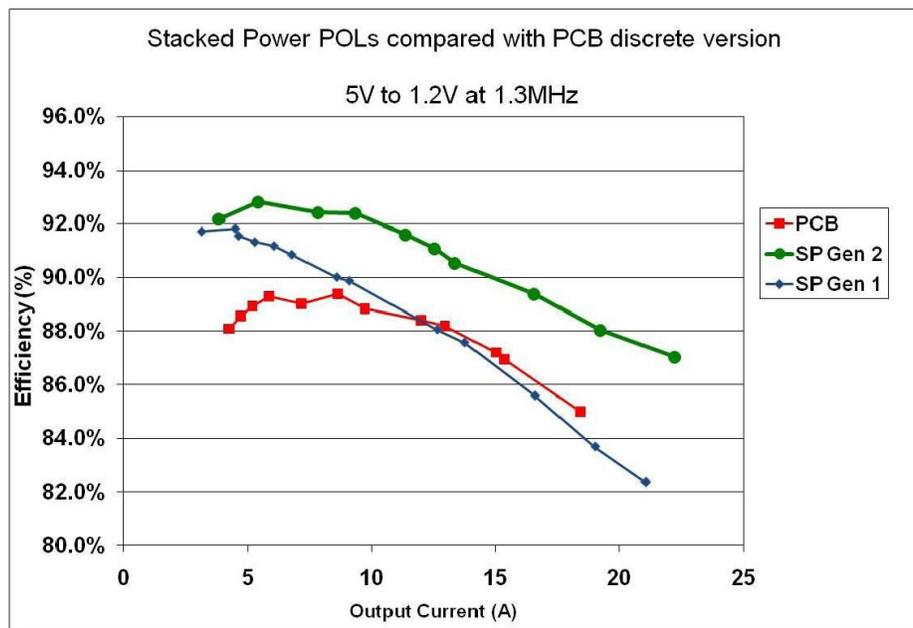


Figure 3.13. Efficiency Graph vs. Output Current for PCB, Generation 1, and Generation 2 Converters [17].

3.2.4 Thermal Analysis

The most important part of the design for the Generation 2 converter using stacked power is the thermal improvements over PCB. That is the reason to switch to a ceramic substrate. The dual sided cooling allows for greater thermal handling capacity compared to an encapsulated discrete module. The process for obtaining a thermal image of the converter will be discussed in this section.

In CPES, a FLIR thermal camera is used to obtain thermal images [35]. The software in the camera is based on a global emissivity value that is set by the user. This value can greatly affect the thermal numbers that are given by the camera.

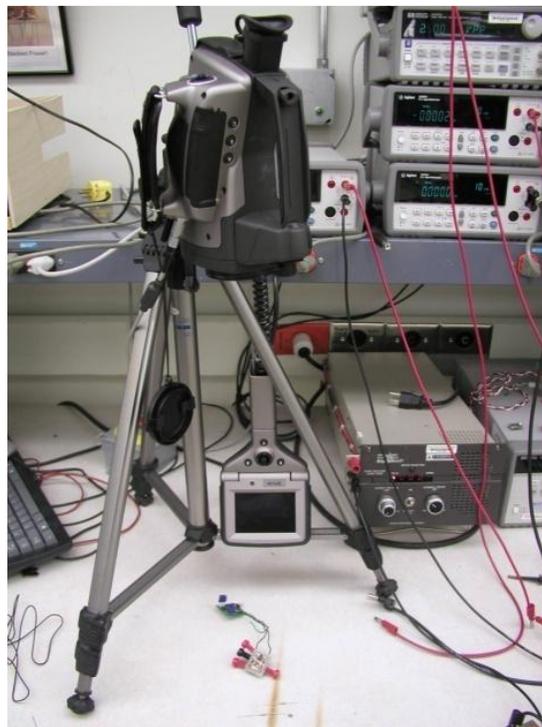


Figure 3.14. Thermal Camera made by FLIR used for thermal imaging. Image by Author.

The initial readings came from a type-k thermocouple to ensure accurate measurements from the thermal camera. Once the temperatures are known from the thermocouple, the emissivity value can be adjusted accordingly. We will focus on the copper emissivity because of its large

presence in the converter design. The driver is the only encapsulated device in the circuit. It is known from literature that polished copper has an emissivity value of .05 while oxidized copper has a value of 0.8 [36]. Black plastic has a value of around 0.9 but we are more concerned with the substrate temperatures and will assume the driver temperature is slightly off. We found a value of 0.67 for the emissivity to be a good compromise between established values in literature and values found with the thermocouple. Ideally you would want the converter painted flat black to give a uniform emissivity but that coating artificially raises temperatures. The inductor below the converter has very poor thermal conductivity values but was measured to be only a 40°C temperature rise so no thermal images were taken.

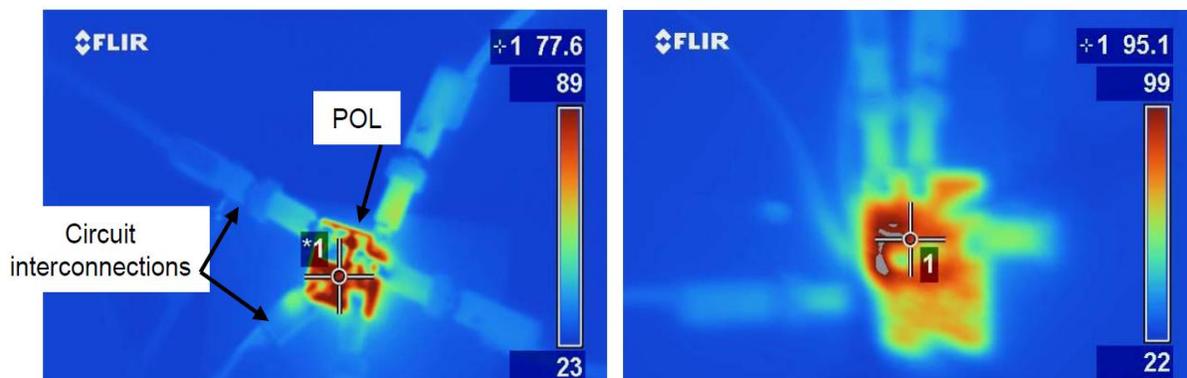


Figure 3.15. Thermal Image for Generation 2 DBC (Left) and PCB (Right). [17] with Author.

It is shown that there is very good heat spreading across the DBC surface while there are localized hot spots in the PCB. The thermal images are shown with some inherent assumptions being made. The DBC module on the left is 20 x 20 mm and has an output current of 17A in natural convection. The PCB module on the right has a much larger footprint at 40 x 30 mm with 6 layers of 2 oz. copper, and is running with an output current of 14A in natural convection. The figure below shows the improvements of the successive generations using the stacked power technique.

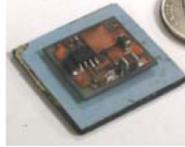
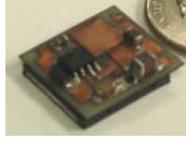
Generation:	1 	2 
Thermal: natural convection and 50 C ambient	15A max	17A max
Electrical:	91.5% at 5A 79.8% at 20A	90% at 10A 86% at 22A
Power density: In natural conv:	28 x 28 x 7 mm 54 W/in ³	20 x 18 x 7 mm 225 W/in ³
At 20A & 200LFM:	73 W/in ³	260 W/in ³

Figure 3.16. Breakdown of statistics for Generation 1 and 2 POL converters [17].

A significant improvement between the generations was the LTCC inductor that is discussed in Chapter 2. The research done by the author greatly contributed to the improvements in the converter. The power density quadrupled and the heavy load efficiency increased. This also led to the increased thermal capability of the circuit in natural convection.

The thermal analysis of the DBC structure shows that the ceramic substrate can greatly improve the thermal management of the module even without a heat sink or fan. This theory will be applied to future generations of DBC converters as even higher power density is sought after.

3.3 2 phase Point of Load Converter Based on Stacked Power

A two phase point of load converter was also proposed at CPES to shrink the footprint of the converter and increase power density [17] [18]. It was sought after to fabricate an active layer as small as possible using the same components as the single phase version shown above.

Based on the active layer size, the coupled LTCC inductor was designed. This design and fabrication was discussed in Chapter 2.

3.3.1 Fabrication Process

The main difference between the single phase and two phase versions is the footprint. The circuit layout by Arthur Ball, which was extensively discussed with the author, ended up with a footprint of 9 x 23 mm. So it was about half the size of the single phase converter while containing twice as many components. This leads to tolerance issues with the fabrication. The alignment of the four circuit layers must be exact as there are connections being made through the whole board.

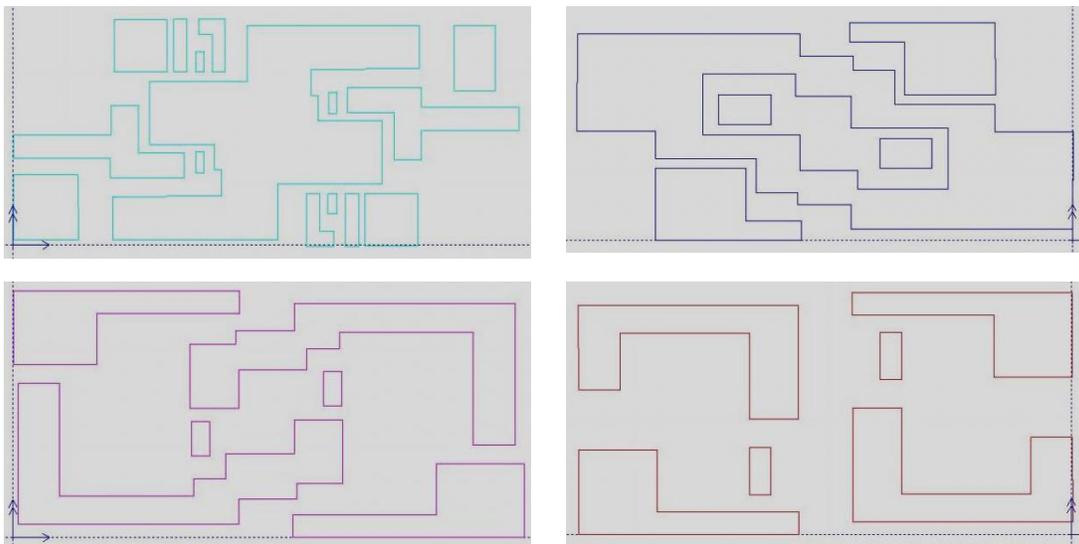


Figure 3.17. AutoCAD Layout for 2 phase POL. Upper Top layer (top left), Upper Bottom layer (top right), Lower Top layer (bottom left), Lower Bottom Layer (bottom right). Image by Author.

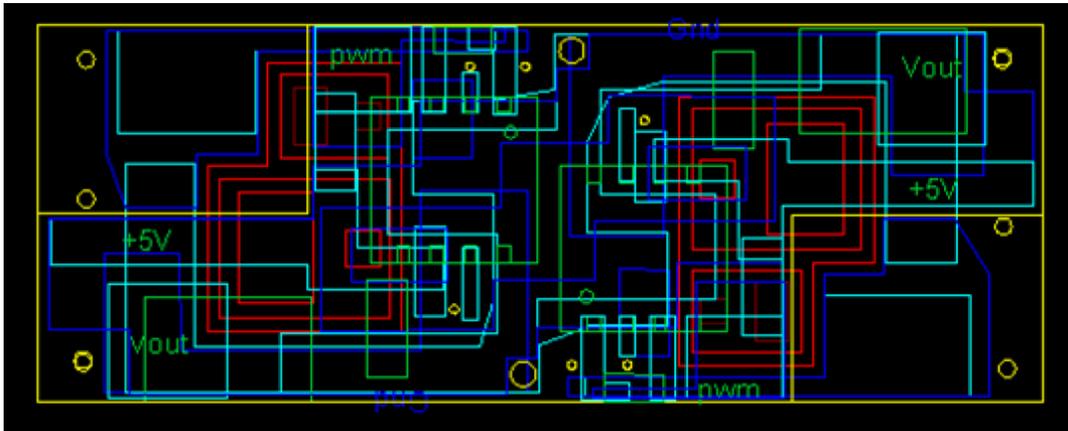


Figure 3.18. Two active layers on top of each other in AutoCAD [17].

It can be seen that the top layer is cut into an S-shape as shown in the yellow outline. This exposes the pads underneath to solder the output capacitor to the lower layer. The entire layout was tweaked in order to include the new tolerances found by the author in the fabrication process. All the vias are tighter than they were in the previous Generation 2 design in order to get the small layout to work. This made it infinitely harder to fabricate as the alignment had to be right on. Measurements were made with the optical system on the laser after cutting the mask to ensure the correct results. Once the masks were laser cut, it went through the same process as the previous generation: etching, cutting the ceramic, embedding the devices, feeding the gate wires, soldering the layers together, and soldering the components in place. The figure below shows the complete converter with the coupled inductor substrate.

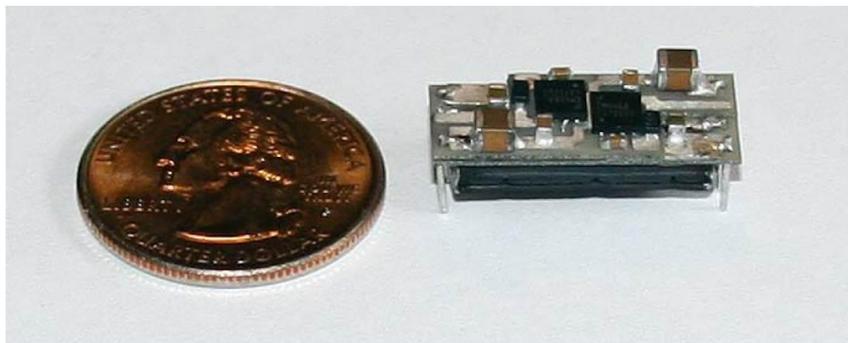


Figure 3.19. 2 phase POL converter using stacked power technique with LTCC coupled inductor [17].
Fabrication by Author.

3.3.2 Results

The idea behind the 2 phase POL is to increase the light load efficiency, keep the heavy load efficiency similar to Generation 2, and shrink the footprint to increase power density. The footprint was reduced from 400mm² to 207mm² which took the power density from 250W/in³ to 500W/in³, a significant finding. The question is the efficiency results and how the thermal capability would affect the current output.

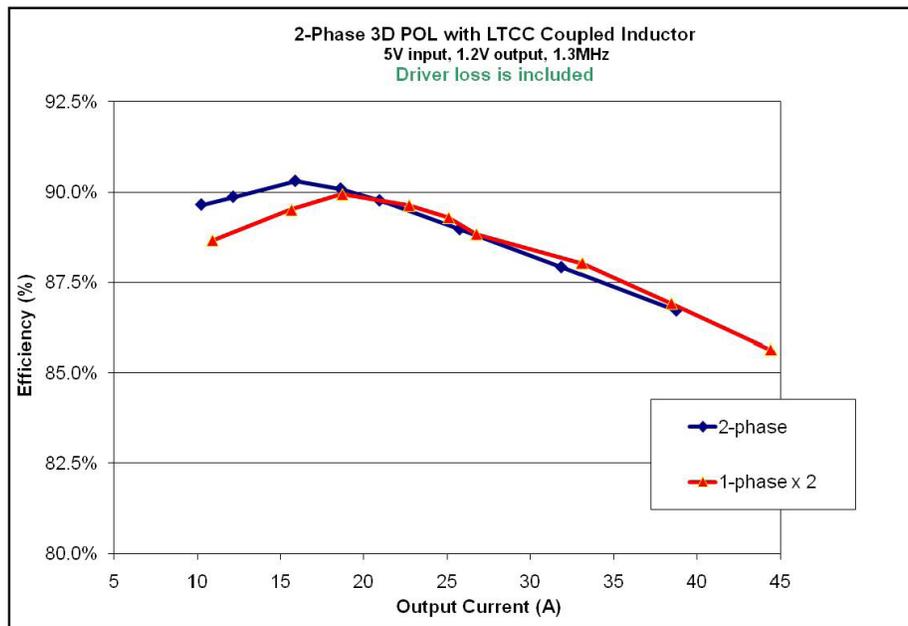


Figure 3.20. Efficiency vs. Output Current for 2 phase POL and 2 x 1 phase POLs [18].

So the light load efficiency is increased by 2 % which is expected from the coupled inductor design. The heavy load efficiency is also similar to Generation 2. The concern is the decreased surface area of the 2 phase converter compared to the much larger Generation 2 board and how that affects the thermal aspects. In natural convection, the 2 phase converter can only handle 13A per phase while the Generation 2 board could handle 17A, which is to be expected. The loss of the converter at heavy loads though is very similar because of the efficiency improvements. At 20A, the single phase version has about 3.4W of loss while the 2 phase version has a loss of 3.7W at 25A. So the fundamental results show that improvements in layout

and circuit parasitics play a large role in efficiency which goes hand in hand with the thermal management of the substrate. The next section will discuss the use of Gallium Nitride devices to continue to shrink the size of the converter for increased power density while using what we learned from the stacked power techniques.

3.4 Packaging of a Converter with Gallium Nitride Devices

The emergence of Gallium Nitride devices is allowing the move to higher frequencies that isn't possible with Silicon devices. This chapter will explore the use of GaN devices in a 3D integrated POL converter. The topics discussed will be the structure of the GaN device, the layout of the circuit and how it affects the performance of the converter and the packaging of the transistor including mounting the device. This chapter will also discuss using the device in a DBC substrate and the thermal aspects of the GaN devices.

3.4.1 Background on Gallium Nitride Devices

Gallium Nitride devices are high electron mobility transistors (HEMT) that offer better performance at higher frequencies. The key to the technology is the wide band gap GaN built on a silicon substrate for lower cost. The table below shows the material characteristics comparisons with silicon and silicon carbide [37] [38].

Table 3.1. Material Characteristics for Si, SiC, and GaN

	<i>Si</i>	<i>SiC</i>	<i>GaN on Si</i>
Band Gap (eV)	1.1	3.2	3.4
Electron Mobility (cm²/V-sec)	1450	900	2000
Electron Saturation Velocity (10⁶ cm/sec)	10	22	25
Thermal conductivity (W/mK)	1.5	5	1.3
Critical Field (10⁶ V/cm)	0.3	3	3.5
Coefficient of Thermal Expansion (CTE)	2.6	4.2	5.6

It must be noted that the current technology has Gallium Nitride being grown on Silicon to keep the cost low for commercialization. This has the tradeoff of the wide band gap performance of Gallium Nitride with the low thermal conductivity of Silicon. The figure below shows the basic structure of a GaN transistor [39] [40]. It is shown that the lateral device also includes an isolation layer between the pure GaN and Si to prevent leakage that would affect the performance of the device. The electron gas (2DEG) develops due to the reaction of the un-doped GaN with the AlGaN layer.

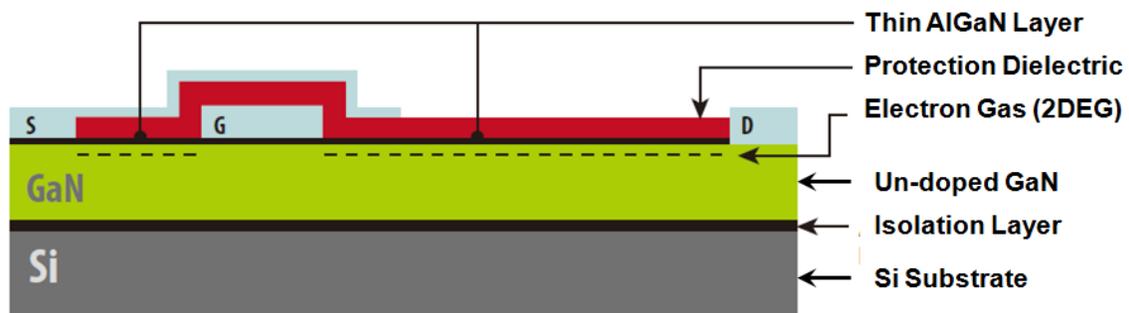


Figure 3.21. Concept drawing of a GaN transistor

3.4.1.1 Packaging Considerations

The use of EPC GaN devices in a 3D integrated converter will be considered in this part of the chapter. There are some things that need to be discussed when packaging an enhancement mode or normally off device. One consideration that needs to be made is how to drive the device. The discussion of driving an enhancement mode device was made at CPES [6]. The main point that must be made is there is a safe range for the device to be driven at. The maximum voltage that the device can see is 6V which is low compared to a silicon device that can handle up to 20V. The gate voltage ringing, which is affected by the driver turn on resistance, package parasitics such as gate resistance and inductance, input capacitance, and PCB layout, must be controlled to operate the enhancement mode devices safely.

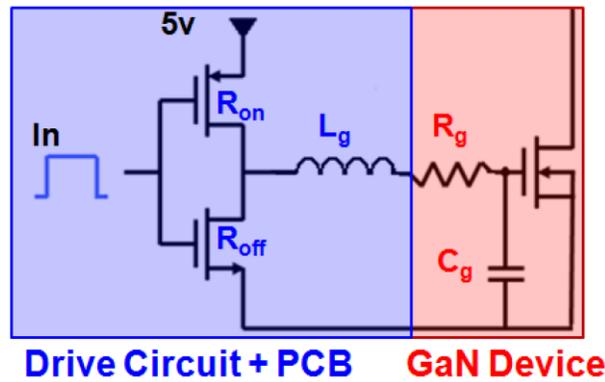


Figure 3.22. Equivalent circuit for Gate Ringing [6].

Prior to the author's work, there were 2 generations of PCB designs that were used to solve the gate overvoltage issue [6]. The first generation used the same driver as the generation 2 stacked power design along with the EPC 1014 for the top switch and the EPC 1015 for the bottom switch. It was found that the overshoot from the gate voltage ringing was outside the safe range and the devices were failing. The second generation improved upon the first by using new drivers from Intersil that would slow down the turn on because of higher resistances. This brought the overshoot closer to the 6V limit but was still outside at 6.3V. There was a revision of the second generation which used another driver by National. It has a higher on resistance along with a lower gate inductance which effectively damps the ringing and brings it into the safe operating range at 4.9V which is shown in Figure 3.23.

Table 3.2. Gate Drive Parameters for GaN Generations 1 and 2

	Generation 1	Generation 2a	Generation 2b
Top Switch	EPC1014	EPC1015	EPC1015
Driver	1xLM2722	2xISL89163	1xLM5113
R _{on} (Ω)	0.9	1	2
R _{off} (Ω)	0.4	1	0.6
L _{gate} (nH)	11	10	5
R _g (Ω)	0.4	0.4	0.4
C _{iss} (nF)	0.28	1.1	1.1

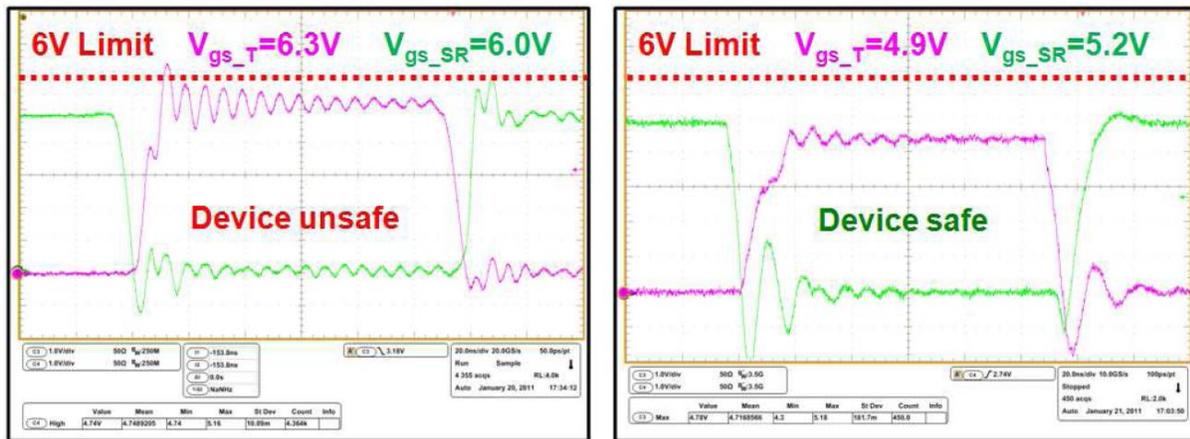


Figure 3.23. Gate Waveforms for Generation 2a (Left) and Generation 2b (Right) [6].

Another consideration that is made for packaging GaN devices is the use of a schottky diode in parallel to the synchronous rectifier. As dead time control is essential to driving an enhancement mode GaN device, the diode helps keep the device safe as it has no internal body diode. The use of the diode is a tradeoff between high efficiency and device safety.

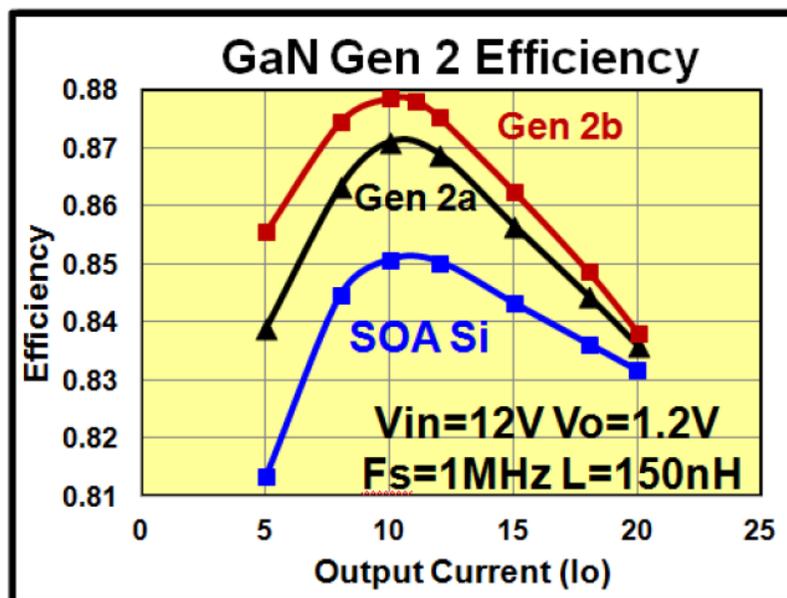


Figure 3.24. Efficiency for the Generation 2 designs [6].

The EPC devices utilize a linear grid array (LGA) pattern to keep the package parasitics to a minimum by interleaving the source and drain pads. The pads are directly solder bumped to the package which limits the external lead frames that hinder the SO-8 package for example.

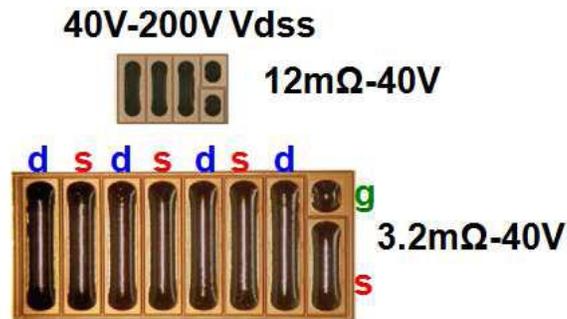


Figure 3.25. EPC LGA GaN transistors. From datasheet.

Some study was done to see how the package parasitics affect the switching loss of the converter [6]. Obviously limiting switching loss is of great importance when dealing with high frequency conversion. The study compared that package and die related switching loss with the SO-8, LFPACK, DirectFET, and LGA package types. The figure below shows the results of the breakdown of switching losses for those packages using a loss breakdown model.

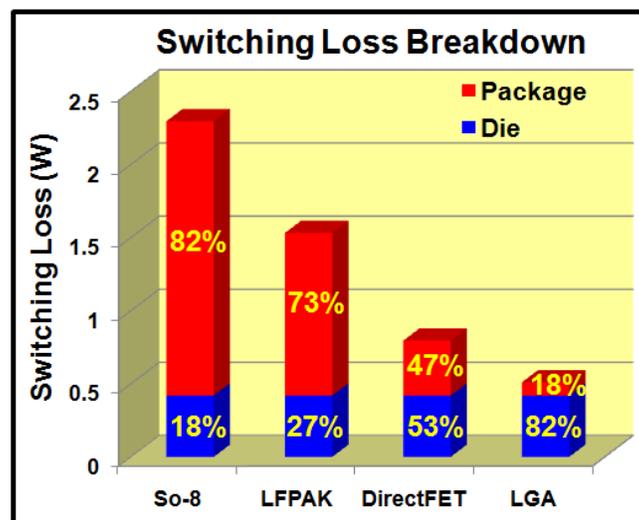


Figure 3.26. Loss Breakdown for different packages ($F_s=1\text{MHz}$, $V_{in}=12\text{V}$, $V_o=1.2\text{V}$, $I_o=20\text{A}$, $L=150\text{nH}$) [6].

It can be seen that the device package can greatly improve the performance of the converter. The next section will begin the authors input by creating a DBC version of the GaN converter to improve the thermal management.

3.4.2 GaN Device Mounting

The first order of business with the GaN device packaging is how to successfully mount the device on PCB and then on DBC. This section will discuss the issues that presented themselves during the mounting of these types of devices. The reduction of footprint of the GaN device as compared to the silicon devices presented some real challenges to ensure reliability while mounting the device.

3.4.2.1 Method and Solder Reflow Considerations

Placement of devices is traditionally done with a pick and place machine and in the case of CPES, we use a Model 860 die bonder manufactured by Semiconductor Equipment Corporation [41].



Figure 3.27. Semiconductor Equipment Corporation Model 860 Die Bonder.
Image by Author.

This machine uses multiple stages for pick and place. The first stage uses a vacuum tip to pick up the device and move it to the placement stage. There is a dual angle camera that allows the user to see the bumped side of the device along with the board pads. The software visually transposes the two images to allow for accurate placement. Once the device is placed, the board can be moved to a solder reflow station.

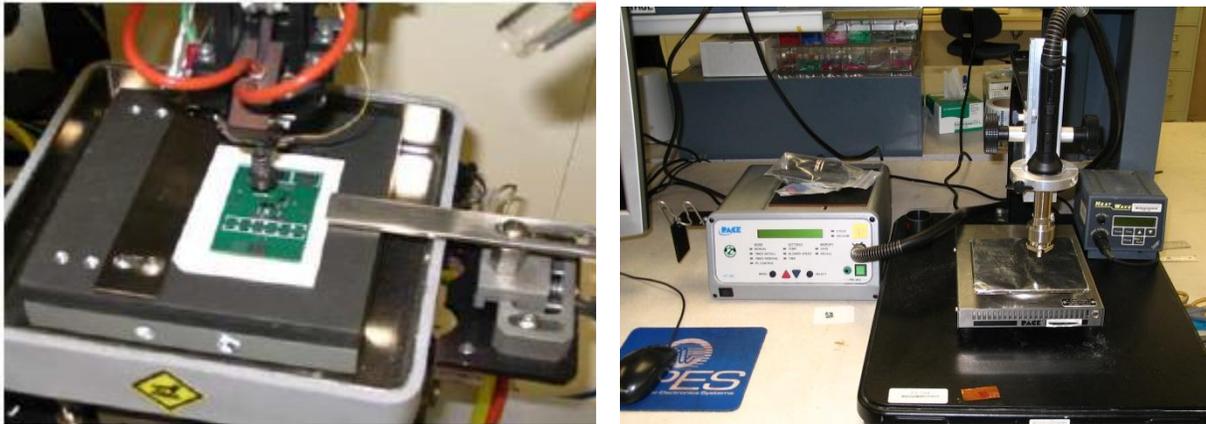


Figure 3.28. Pick and Place (left), Solder Reflow Setup (right). Image by Author.

The station includes a nozzle, controller and a computer for the software. The software allows the user to set up to 25 reflow profiles including preheat, soak, and reflow temperatures along with the timing. This equipment is manufactured by PACE worldwide [42].

The solder reflow profile had to be fine-tuned in order to ensure a solid, limited void solder connection. Many tests were run to find the profile and it was verified using non-destructive X-ray techniques. The profile for the SAC 405 solder is universally known but the controller profile had to be found. It differs from the solder profile in that there is loss to the air between the nozzle tip and the top of the device along with the thermal resistance through the device to the solder bumps. The temperatures were measured using a thermocouple throughout the profile. The main concern is to find the correct reflow temperature to minimize voiding. The

application notes for mounting an EPC device gives a figure of what the voiding volume should look like for a successful profile.

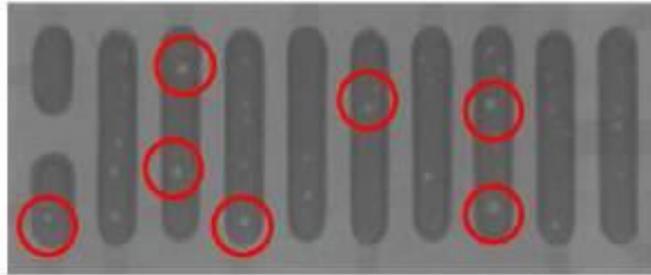


Figure 3.29. EPC X-ray from application notes showing voiding

The application notes describe two ways to mount a device. The first involves using a solder stencil to apply a solder paste to the board pads. Then the device is placed and reflowed. This procedure gave us constant shorts due to the small distance between pads. This was verified in our lab along with an outside vendor. We went with the second way which uses a tacky flux to hold the device during reflow and just uses the solder bumps on the package. This process gave us consistent results. The tacky flux that is recommended is the Kester TSF6502 [43]. Kester also makes a TSF6592 for lead free packages such as the EPC 2015. The figure below shows the concept of mounting with tacky flux. Careful attention must be paid to the application of the tacky flux. Only a small amount is needed, otherwise it doesn't fully burnoff during reflow.

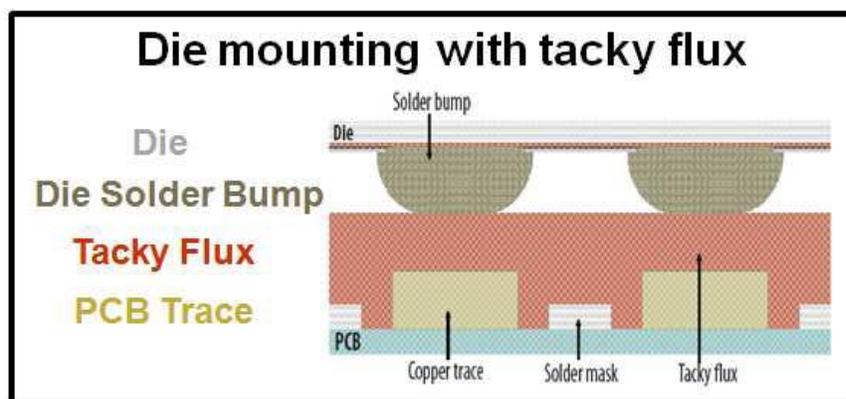


Figure 3.30. Die mounting concept with tacky flux. From EPC application notes.

After many profiles were run keeping the peak reflow temperature as the variable, a profile for the reflow controller was built. The discrepancy between the reflow program and the device temperature is due to the heat loss. The X-ray shows that very little voids occur with this program and even looks better than EPC's X-ray in the application notes. This profile was used for all boards that were fabricated with EPC devices.

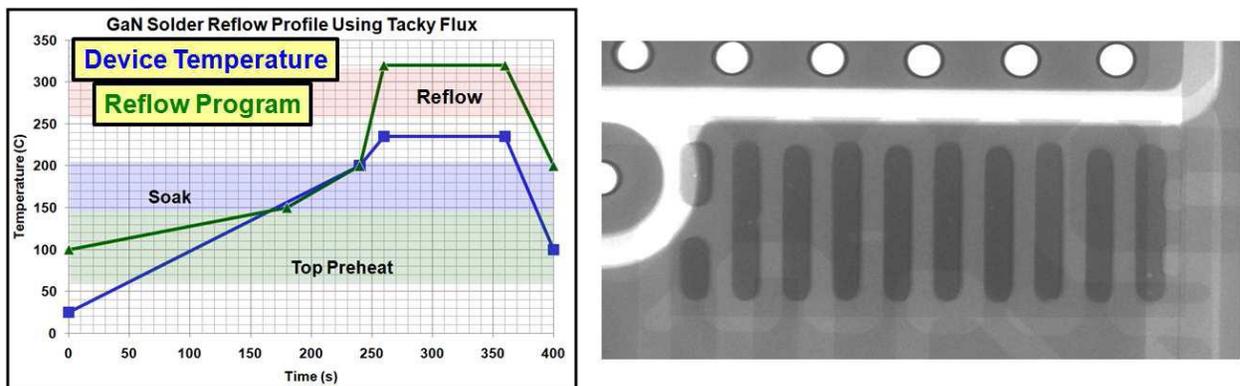


Figure 3.31. Solder reflow profile for EPC GaN devices (left), X-ray of mounted EPC GaN Device on PCB (right). Images by Author

3.4.3 Fabrication Process for GaN DBC

Now that all the mounting details are taken care of, it is time to begin fabricating a GaN POL converter on a ceramic substrate. In the stacked power technique, the limiting factor for layout was the SO-8 driver with a pin pitch of 800um. The limiting factor would now become the GaN device itself as it has a pitch of 400um.

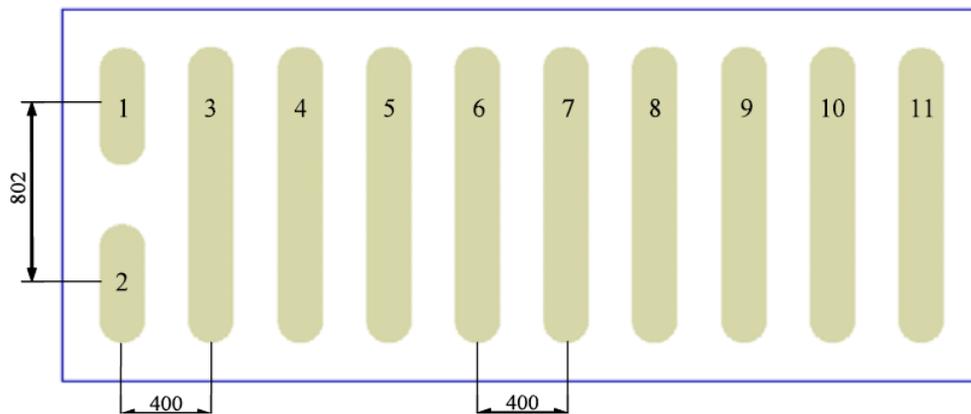


Figure 3.32. Land Pattern for the EPC 1015 bottom switch. From datasheet.

This presented a significant challenge compared to the SO-8 package layout. The initial assumption was that a copper thickness of 8 mils, as before, would not be possible for a pitch of 400um and a line width of 200um. Some study was needed to determine the optimal parameters for this device.

3.4.3.1 Pitch and Line Width Development vs. Copper Thickness

The pitch and line width on a circuit board are dependent on the copper thickness present during a wet etching process. Wet etching typically has a 20% horizontal loss compared with the vertical thickness. To determine the optimal parameters needed for the EPC GaN device, samples were fabricated with a constant thickness but varying the line width and pitch.

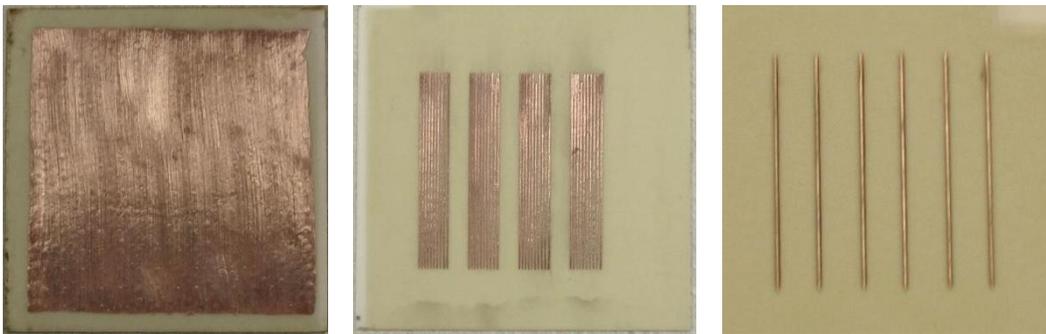


Figure 3.33. Blank DBC (left), Pitch Test on DBC (middle), Line width test (Right). Images by Author.

Once the etching was complete, a conclusion was made as to what is the optimal thickness for the copper. It was found to be 2-3 mils. The DBC from Curamik comes in 8 mil thicknesses so it had to be etched down in order to use for the circuit pattern. The blank piece of DBC is covered in kapton tape first and one side is removed to expose the copper. The piece is then put in the etchant, keeping in mind that the copper etches at 1 mil/min. Every minute the piece is rotated in the machine to keep the fluid flow and etching uniform. The thickness is checked with a micrometer. It is found that the uniformity across the copper surface is +/- 0.5% which is fairly good considering the simplicity of the etching machine.

3.4.3.2 Pin Through Ceramic for Electrical and Thermal Connections

Before embarking on the fabrication of the circuit, a consideration had to be made for connecting the two copper layers of the DBC. Electrical and thermal parameters had to be taken into account when choosing the best method. Curamik Electronics published a paper that has suggested a few ways of making these types of connections through the ceramic [44]. The connections are usually made by etching the copper around the via and laser cutting a hole through the via. Then a copper ball or block is placed in the via space and covered with a piece of copper sheeting. The connection is then made by mechanically pressing and welding the copper together. This involves having specialized equipment to do the job.

We considered doing the via in a different and simpler way at CPES. It was proposed to using a PCB mounting pin to make the connection from the top to the bottom layer. The pins are manufactured by Robison Electronics and are labeled as dummy mounting pins [45]. It essentially looks like a standard nail with a 40mil diameter head and a 22mil diameter body. The length is no concern as the pins can be trimmed to fit. The copper around the vias would be etched and the via hole is laser cut out of the ceramic as Curamik has done. From this point the pins are placed, soldered to the bottom layer of copper, trimmed, and then grinded down with a Dremel tool to have a smooth surface.

3.4.3.3 Circuit Fabrication

The PCB layout was done by David Reusch for the Generation 3 GaN buck converter [6]. This is the basis for the DBC design that is done by the author. The start of the fabrication is to convert the PCB design from Altium into an AutoCAD layout. This is done by saving the design in Altium as a dwg file. It must be noted that the design does not transfer cleanly and requires a good amount of fixing to get to a point of being able to re-draw for DBC. Contained in the

AutoCAD layout is all the parameters that were learned from the stacked power techniques, those that were found in study for the GaN layout, and the ones for the pins through the ceramic.

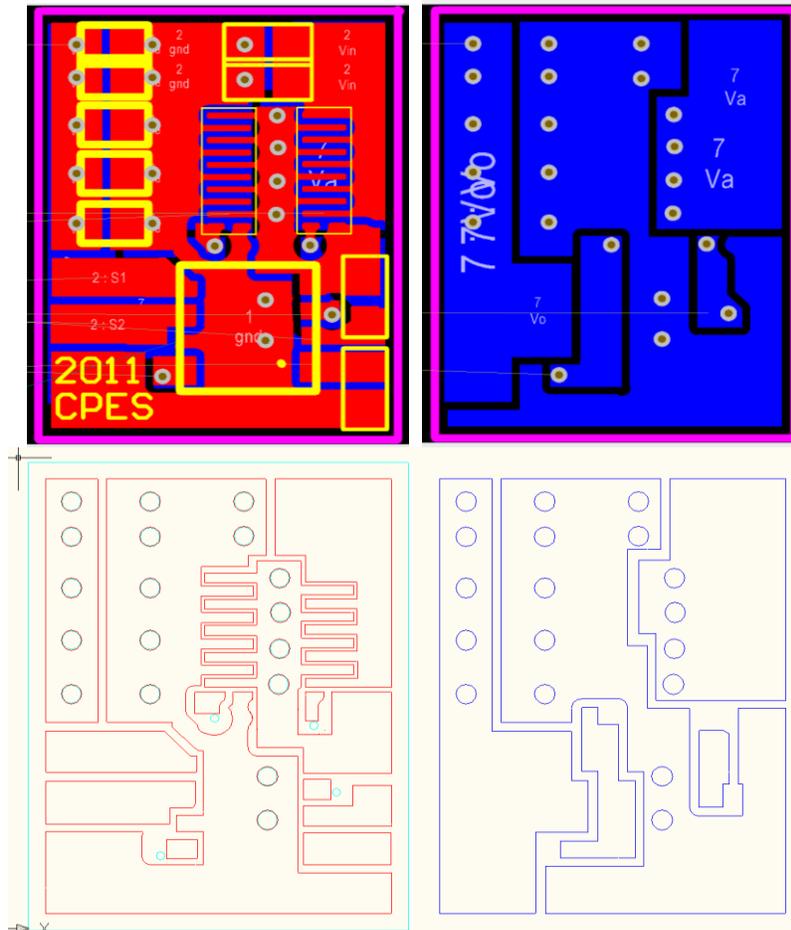


Figure 3.34. PCB Layout (top), AutoCAD layout (bottom). Images by Author.

The main differences in the layouts are the tolerances. The AutoCAD layout is drawn to take into account the losses that occur in our wet etching process. These tolerances were tested to ensure the proper pitch and line width could be achieved. Pin placement was discussed to optimal electrical and thermal characteristics. The four pins between the GaN devices are for the switching node and also to facilitate heat transfer from the small surface area. Now that the layout is done it is time to fabricate the DBC circuit.

The process for fabricating the GaN DBC circuit follows the previous techniques. A blank piece of DBC is cut and masked with Kapton tape. The circuit pattern is cut using the laser and the file that is shown above in Figure 3.34. The mask is removed to expose the copper to be etched. Mask removal is slightly different than in previous generations. Careful attention must be paid to the area around the GaN traces as a residue is left from the adhesive of the Kapton tape. This residue has to be removed under a microscope with a sharp utility knife to ensure complete etching of the copper. The figure below shows a slightly different layout but concentrates on the same residue problem. The left half has the residue present and the right half is cleaned. The copper is then wet etched to arrive at the circuit pattern.

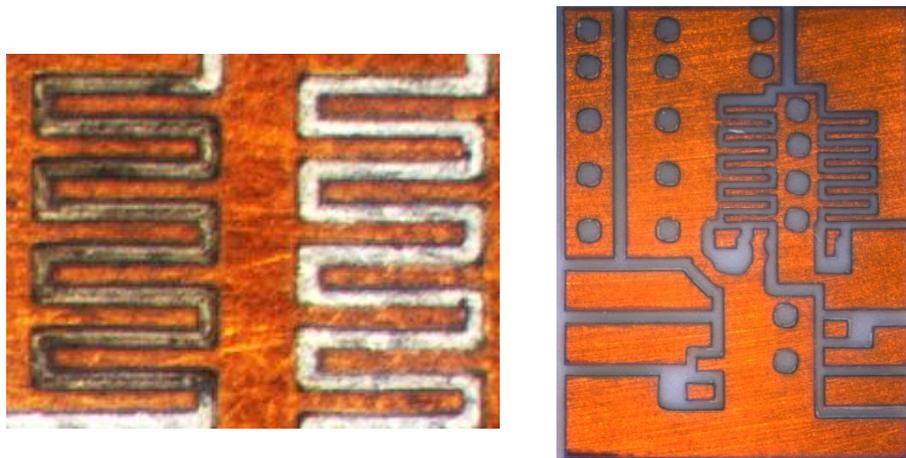


Figure 3.35. Kapton residue removal from GaN (left), Wet etched (right) traces. Images by Author.

The ceramic is then laser cut to prepare for the pin placement and gate wires. The pins are soldered using two types of solder paste. The four pins between the devices were soldered using a 95Pb 5Sn solder paste with a reflow temperature of 310°C. This is done to prevent the pins from de-soldering during the reflow of the devices. The rest of the pins are soldered using a bismuth infused solder paste 43Pb 43Sn 14Bi with a reflow temperature of 163°C. The gate wires are threaded and soldered and the GaN devices are then placed and reflowed including the

tacky flux. The final stage is to solder reflow the capacitors and the driver in place using the Sikama reflow belt.

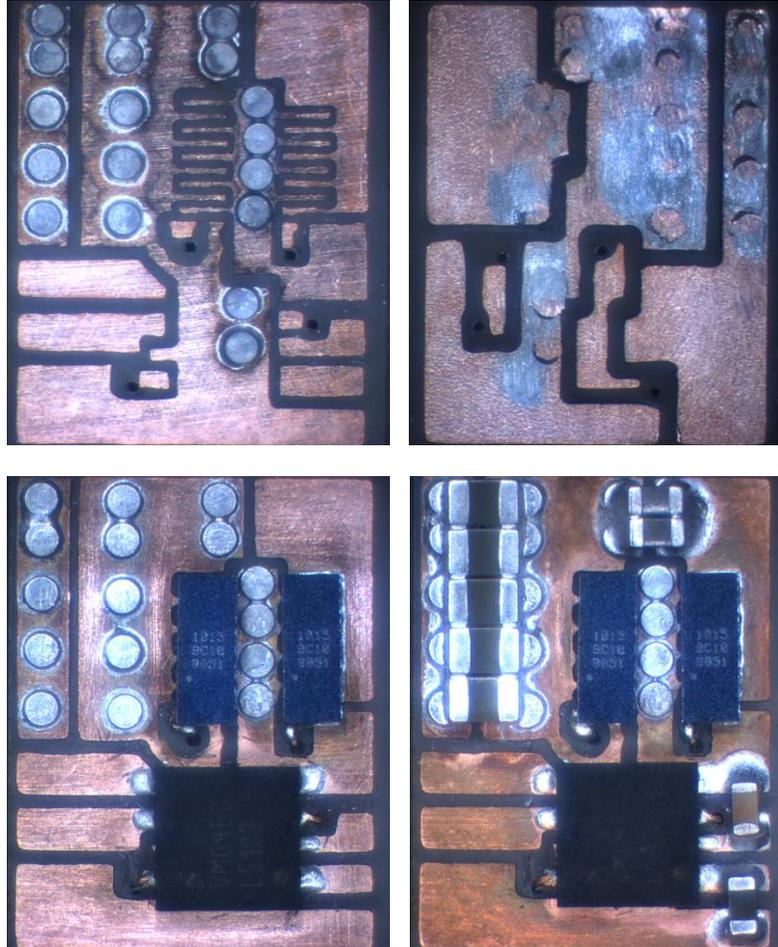


Figure 3.36. Top with Pins (top left), Bottom with Pins (top right), Devices with Driver and gate wires (bottom left), Full module (bottom right). Images by Author.

3.4.4 DBC GaN POL with Lateral Flux Magnetic Substrate

The GaN DBC module is integrated with the lateral flux inductor from Chapter 2. The module has a footprint of 11mm x 14mm and a power density of 700W/in³ or 30% higher than the two phase stacked power module. The figure below shows the comparison of the Gen 3 6 layer PCB version next to the Alumina 2 layer DBC version.

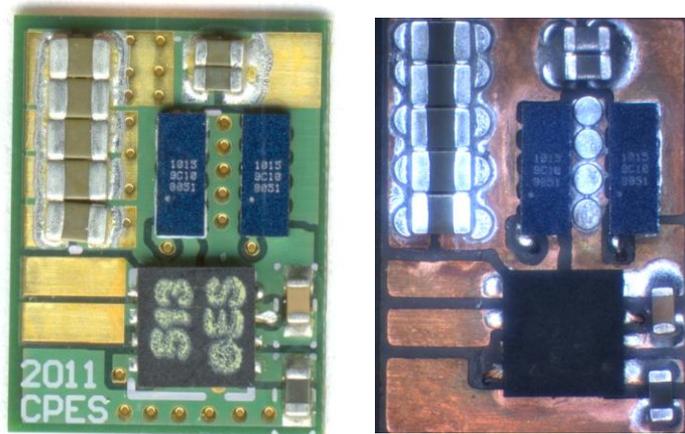


Figure 3.37. Comparison of PCB and DBC versions. Images by Author.

3.4.4.1 Power Loop Shielding

The objective of the exercise of comparing the PCB and DBC versions is to explore the effects of copper layers on the efficiency of the converter. Is it feasible to use a 2 layer DBC and still operate the same as the 6 layer PCB version? The simple answer is no. The efficiency is 2% lower across the board and 2.5% lower at heavy load.

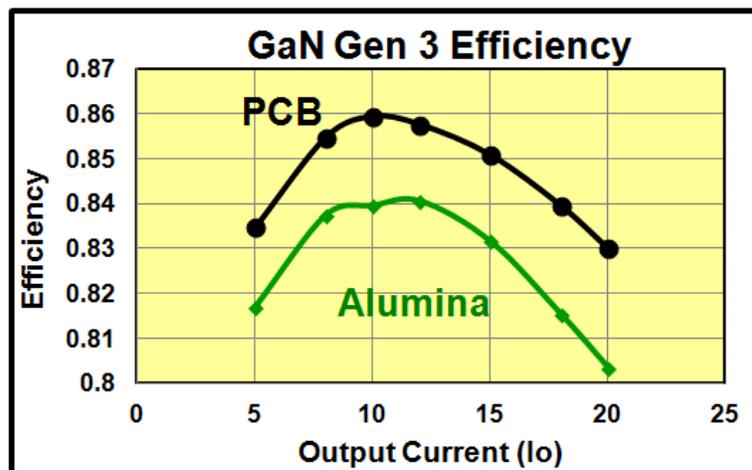


Figure 3.38. Efficiency Comparison between PCB and DBC [6].

Question is what is causing the drop in efficiency and how can it be addressed. As shown in work at CPES, it is generally caused by the power loop shielding and the interference that is caused by the magnetic substrate below [6] [16]. It is seen in Figure 3.33 and 3.35 that the

bottom layer does not have a complete ground underneath the power loop which means the flux effects are not cancelled and the efficiency drops. This paper will not concentrate on the theory that is behind this but what was done to prevent this from happening. The theory is explained in the papers that were referenced above. In a 4 or 6 layer PCB layout, multiple layers of copper can be used as ground planes, essentially removing the magnetic flux interference from the power loop above. That is not the case in a 2 layer DBC structure. So it is proposed to add an external copper layer soldered to the ground trace (including Kapton tape for insulation from other traces) to the DBC structure to mimic a PCB layout.

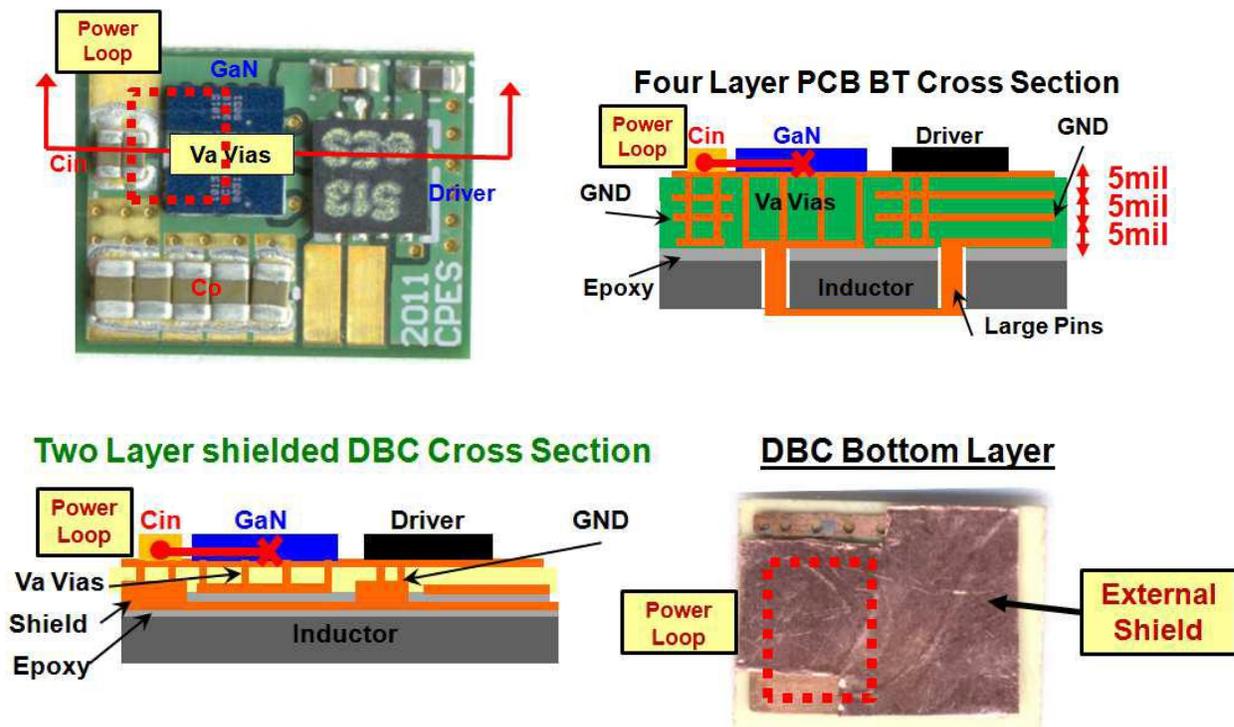


Figure 3.39. 4 layer PCB and cross section (top), 2 layer DBC and cross section (bottom). [6] with Author.

Seeing that the shield is essentially ground, the copper must be insulated from the magnetic traces below. This can be done experimentally with Kapton tape but other means must be researched to effectively do this. One proposal is made by the author to use an epoxy based thermally conductive paste to do the job. This would mechanically hold the substrates together

while providing some thermal conductivity while maintaining electrical isolation. This will be discussed further as future work.

The results from adding the shield layer show that the efficiency is increased by 1% but still not as efficient as a PCB layout. This is due to the proximity of the shield layer to the devices. In the case of PCB it is 5 mils where the DBC version it is 15 mils. This is the tradeoff of using DBC versus PCB. Curamik has since released an 10 mil ceramic DBC which would bring the efficiency closer to PCB.

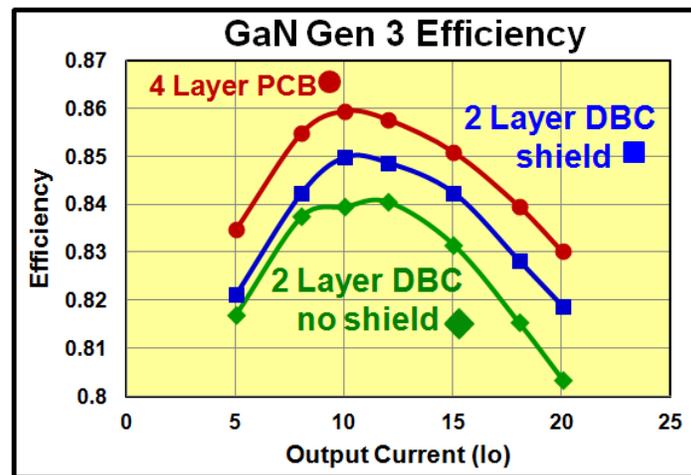


Figure 3.40. 4 layer PCB vs. 2 layer DBC with and without shield [6].

3.4.4.2 Thermal Analysis of Generation 3

A thermal analysis is needed to compare the PCB and DBC versions to prove the usefulness of a ceramic substrate. This is especially important as the footprint is shrinking and the power density is increasing. This is also needed to confirm the use of the mounting pins in the DBC version. It needs to be checked to make sure the heat is still spreading effectively throughout the ceramic substrate.

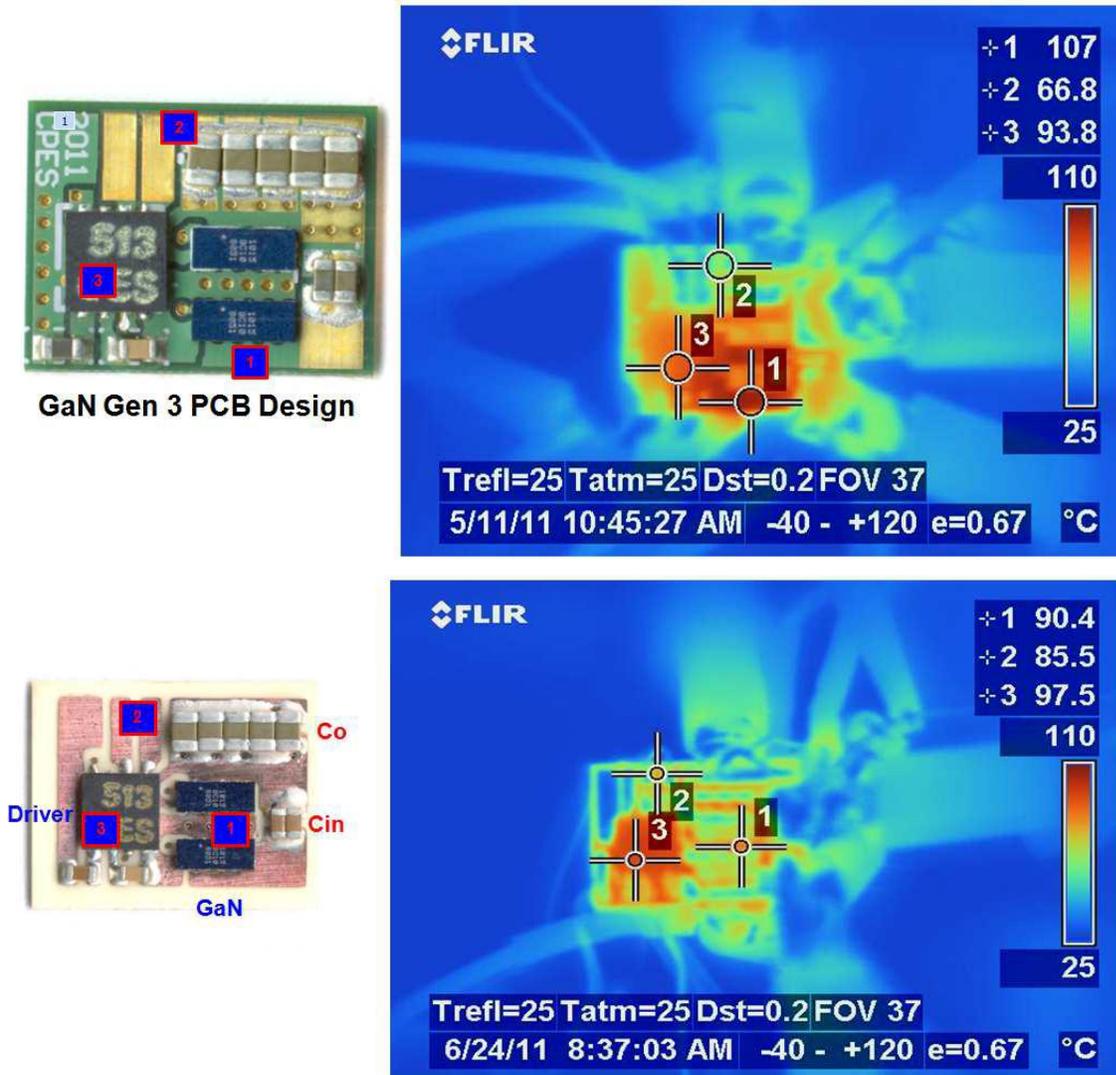


Figure 3.41. PCB thermal image (top), Gen 3 DBC thermal image (bottom). [6] with Author.

It can be seen that the PCB layout has hot spots around the devices while the board at point two remains relatively cool approximately at 27 degrees lower than the hot spot. The DBC at point two is essentially the same temperature as the rest of the board and the peak temperature is 17 degrees lower than that of the PCB. It must be noted that the board test conditions are the same and are run with the same amount of power loss. The third points on the thermal graph are on the driver itself. The emissivity point is set to get more accurate values on the copper so the

driver temps are probably on the high side. We can't ignore the values but must keep in mind that they are 3-5 degrees too high.

3.4.4.3 Improved Layout for Shield-less Design

Seeing that a shield needs to be incorporated to improve the efficiency of the converter, a different layout was proposed to improve on the Gen 3 DBC design [6]. First, the driver was changed from the LM5103 to the LM5113 which is a BGA package rather than a LLP. This allowed for a smaller footprint as the driver is only 2x2 mm instead of 4x5 mm. The main packaging change is the movement of the four pins for the Va node. In Gen 3, they were located between the devices but thermal analysis shows that they can be moved without significant penalty. This allows the power loop to be smaller for higher efficiency because the devices are closer together. The packaging and fabrication is essentially the same as Gen 3. The pins next to the bottom switch allow for the power loop to be vertical and return to the input caps through the bottom layer as shown below. This effectively cancels the flux induced by the power loop path.

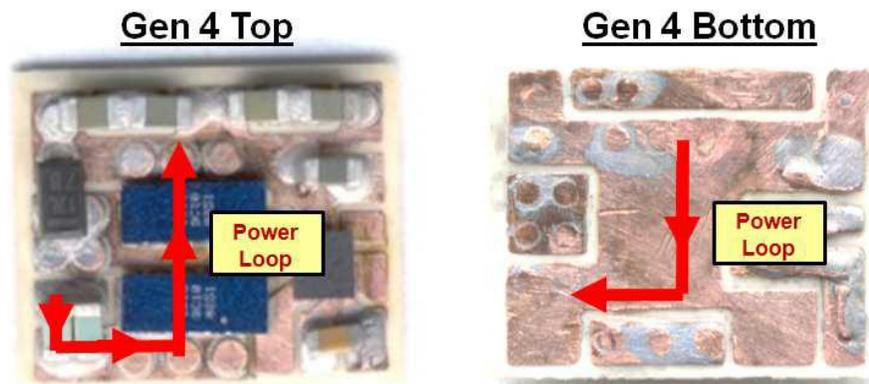


Figure 3.42. Gen 4 top and bottom layers showing the power loop path. [6] with Author.

The result in this design is a 45% reduction in footprint and an increase to 900W/in³ for power density. Generation 4 gives a better efficiency than that of the Generation 3. It can be seen in the figure below that even without a shield, it out performs the Generation 3 design

electrically. But the heavy load efficiency is slightly worse than Generation 3. This will have an effect on the overall thermal management so there will be inherent tradeoffs.

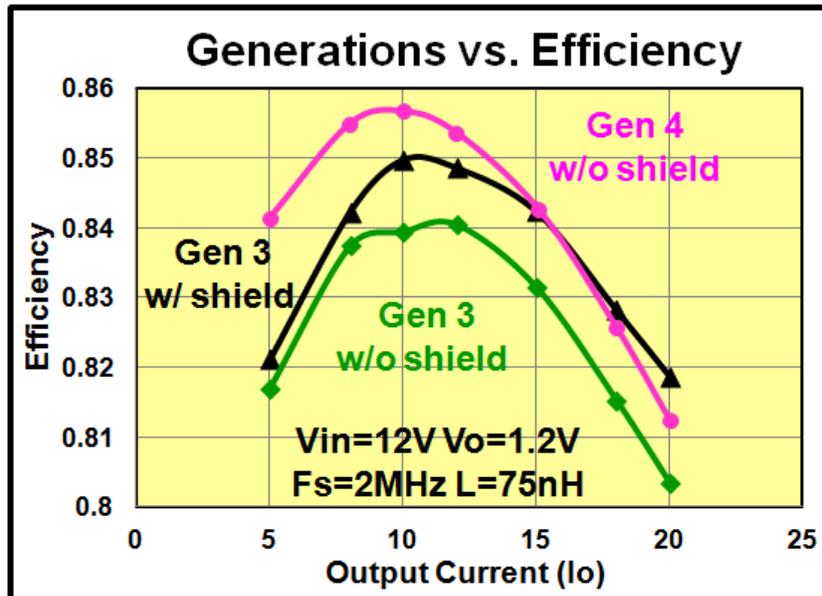


Figure 3.43. Gen 3 and Gen 4 efficiency comparisons [6].

The cause of the higher load efficiency drop is the placement of the Va node pins. While the power loop is smaller due to the moving of those pins, it gives a higher resistance value. Since it is the Va node, the full current flows through that node to the inductor. It was simulated at CPES and is shown below [6]. The flux is concentrated more on two pins in Generation 4 where it is distributed among 4 pins in Generation 3.

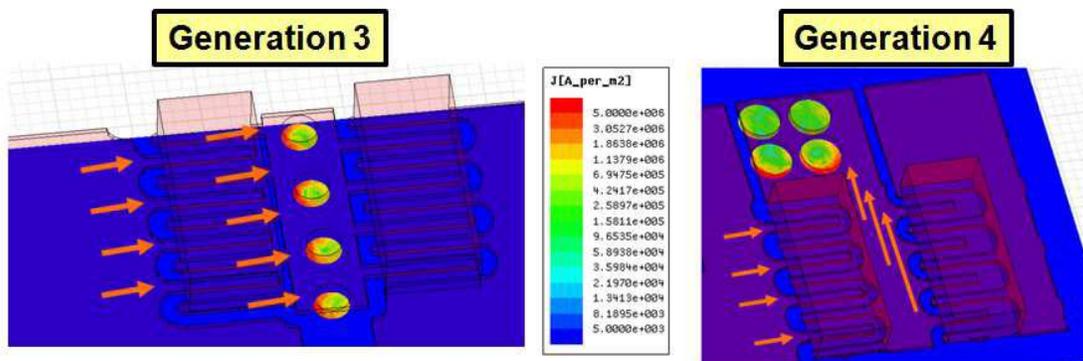


Figure 3.44. Generation 3 and 4 inductor current flow and flux mapping [6].

3.4.4.4 Thermal Analysis of Improved Design

It can be assumed that the thermal management of this layout would have to be slightly poorer than that of Generation 3 just based on footprint size. So there are some inherent tradeoffs between the two designs. Generation 3 would give better thermal performance while Generation 4 would be slightly better electrically. The graph below shows that Generation 3 can handle more power loss than Generation 4. So you can rate Generation 3 as being able to handle 18A while Generation 4 can handle around 15A. It can be noted that the Generation 3 BT PCB could handle about 13A.

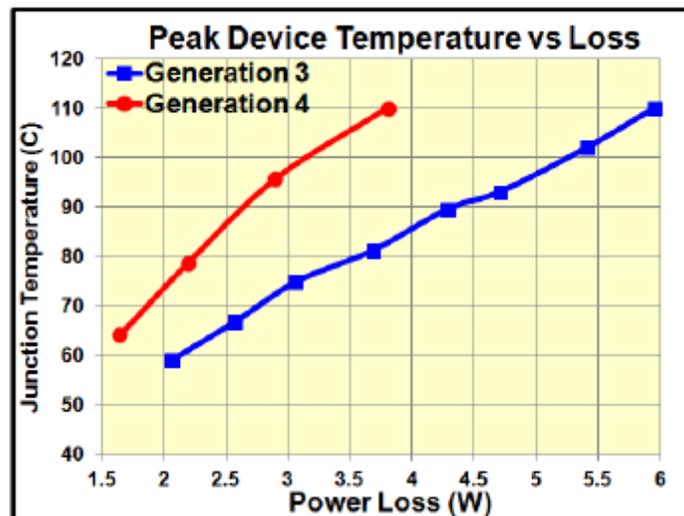


Figure 3.45. Generation 3 and 4 comparisons of Power loss handling capability [6].

3.5 Conclusion

This chapter discusses techniques and processes to build integrated POL converters. The first section concentrated on the stacked power theory and how it applies to a ceramic DBC substrate. The use of bare unpackaged DirectFET devices led to a dual sided cooling converter with excellent thermal management. Using this technique gave an output current capability of up to 20A with a power density of 250W/in³. This represented an increase of 5-10x the power density of current industry products. It also became the basis of all CPES DBC generations to come.

Using the stacked power technique, the footprint could be reduced further by implementing a two phase converter with a coupled inductor. While the fabrication processes were similar, it represented its challenges in laser cutting to ensure accurate alignments between the two layers. Due to the detail oriented work done with the process, a decrease in footprint of 40% was achieved. A power density of $500\text{W}/\text{in}^3$ was demonstrated with a total output current of 40A. Using aluminum nitride as the ceramic, the substrate was able to handle the full current in natural convection.

With the success of the stacked power techniques with silicon devices, a higher power density was sought after using Gallium Nitride devices. The lower parasitic package gave an opportunity to also move to a higher 12V input and still keep the efficiency high. Keeping the efficiency high led to lower losses which in turn allowed for smaller footprint and better thermal management. Processes had to be changed to allow for the mounting of a LGA style device package. The main concern is the 200 um pitch for the GaN pads along with the 400 um trace width. This led to a copper thickness of 2 mil which was accurately achieved using traditional wet etching techniques.

Two generations of a DBC GaN POL converter were fabricated and successfully demonstrated. The first gave the opportunity to work out the details for the fabrication of the circuit and the GaN mounting process. This generation demonstrated a footprint of 11 x 14mm and achieved a power density of $700\text{W}/\text{in}^3$ while having an output current of 18A. It also showed the need for a shield for the power loop to give better efficiencies. This led to the second DBC GaN generation with a better layout to completely shield the power loop. It gave a power density of $900\text{W}/\text{in}^3$ or almost 4x higher than the first stacked power converter. While the first generation had better output current capability, the footprint for the second generation was

decreased by 30%. The figure below shows a summary of the power density achievements and how the author has contributed to the research objectives of CPES.

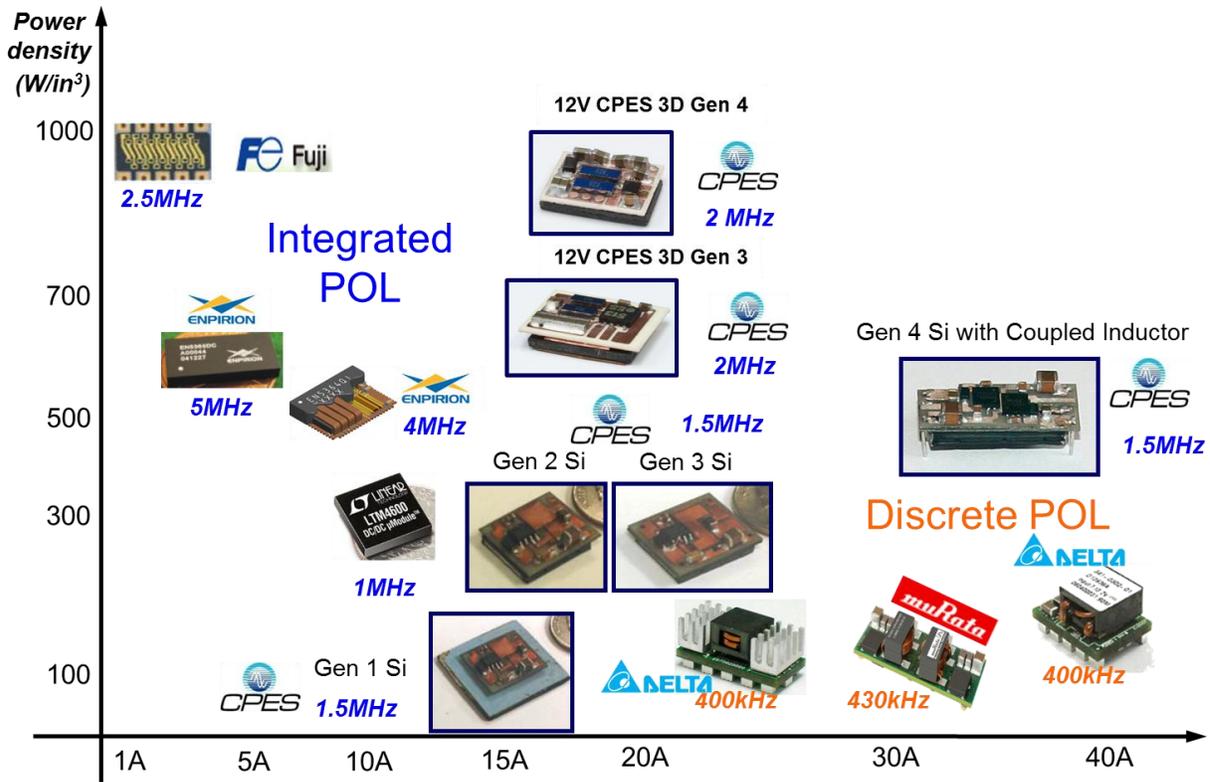


Figure 3.46. Power Density vs. Output Current for Industry products and CPES Research modules. Images by Author.

Chapter 4: Conclusion and Future Work

4.1 Conclusion

The focus of this paper is the packaging techniques that have led to improved processes which created higher power density POL converters. Industry products could achieve high power densities at low currents or lower power densities at higher currents. A void could be found in the high power density and high current regions. The research objectives at CPES were to design and fabricate POL converters in this range. Conventional techniques were not able to meet these requirements so new techniques were studied. Ceramic substrates using DBC technology could help fulfill what researchers were looking for. The high thermal conductivity of the alumina or aluminum nitride could help shrink footprints while maintaining the excellent thermal management needed to handle high output current. Focus was also paid to revising LTCC techniques to realize smaller magnetic sizes and thicknesses.

Chapter 2 discussed the processes of fabricating passive layers used as magnetic substrates. The current LTCC inductor fabricated at CPES was too large to realize high power densities and had to be re-designed including a change in LTCC tape permeability and conductor paste. The higher permeability tape led to smaller footprint while the conductor paste led to smaller DCR values for reduced losses at heavy load. The inductor fabrication proved to be tricky as the conductor paste and tape sintering profiles were incompatible. Gas channels were proposed to alleviate binder burnout problems along with pressure build up. DCR values were decreased by 80% and footprint was decreased by 40% leading to a power density increase of 5 times.

Also in Chapter 2, a coupled inductor was introduced to use as a magnetic substrate for a two phase converter. The techniques were the same as the previous inductor with the addition of

top vias to help with sintering. While the footprint was decreased dramatically to increase the power density, the thickness of the inductor became a limiting factor. The 3.4 mm thickness was as far as the technology could be pushed.

A lateral flux inductor was introduced to give better inductance density at smaller thicknesses to alleviate the problem that the vertical flux inductor has. Fabrication processes were changed to successfully package this type of inductor while using the same conductor paste. Layer groupings were introduced to give more vertical via walls and fix problems that laser cutting introduces with this type of structure.

Chapter 3 focused on the active layer fabrication processes that would lead to significant improvements in power density. The stacked power techniques led to better thermal management in the package and high output current capability. Many small details were worked out to successfully fabricate this structure using DBC substrates. A two phase converter was also fabricated to utilize the coupled inductor discussed in chapter two.

With the knowledge gained from the stacked power techniques with silicon devices, Gallium nitride devices were studied for use in a DBC substrate. Two generations were studied to learn how to fabricate efficient, high power density converters. The first worked out the details for the circuit layout including how to simply and successfully connect the two copper layers. It also gave the opportunity to study the GaN mounting procedures. This generation revealed the problem with power loop shielding from the magnetic substrate and led to the second generation.

Power densities went from 50W/in³ in the very first DBC/LTCC generation to 900W/in³ for the last GaN DBC generation. This was all during the time the author was involved in the project. This shows the importance of packaging involvement in a research project. Without the

author, the circuit layouts and theory might have improved but it would have been difficult to demonstrate the hardware without the improvement in fabrication.

4.2 Future Work

With the release of a thinner ceramic DBC, additional work can be done to improve the shielding effects in the structure. Theory has already proven that a ground plane closer to the power loop will result in better efficiency. Structures just need to be fabricated with the new ceramic to prove the theory.

Further integration of these converters also needs to be investigated in the future. All this work was demonstrated by directly soldering the magnetic substrate traces to the active layers. These two substrates need to be reliably integrated together mechanically and electrically. One hypothesis by the author is to use a thermally conductive but electrically insulating paste that can be cured to provide a mechanical bond. This has to be investigated to see if it can handle thermal cycling set by JEDEC standards. It also has to be seen how the paste layer would handle the high current temperatures involved with this work and how it affects the thermal travel through the converter.

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