An Isolated Micro-Converter for Next-Generation Photovoltaic Infrastructure

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Photovoltaic (PV) systems are a rapidly growing segment in the renewable energy industry. Though they have humble origins and an uncertain future, the commercial viability of PV has significantly increased, especially in the past decade. In order to make PV useful, however, significant effort has to go into the power conditioning systems that take the low-voltage dc from the panel and create utility compatible ac output. Popular architectures for this process include the centralized inverter and the distributed micro-inverter, each with its own advantages and disadvantages. One attempt to retain the advantages of both architectures is to centralize the inverter function but construct PV panel-level micro-converters which optimize the panel output and condition the power for the inverter. The main focus of this work is to explore the technical challenges that face the evolution of the dc-dc micro-converter and to use them as a template for a vertically integrated design procedure.

The individual chapters focus on different levels of the process: topology, modulation and control, transient mitigation, and steady-state optimization. Chapter 2 introduces a new dc-dc topology, the Integrated Boost Resonant (IBR) converter, born out of the natural design requirements for the micro-converter, such as high CEC efficiency, simple structure, and inherent Galvanic isolation. The circuit is a combination of a traditional PWM boost converter and a discontinuous conduction mode (DCM), series resonant circuit. The DCM

operation of the high-frequency transformer possesses much lower circulating energy when compared to the traditional CCM behavior. When combined with zero-current-switching (ZCS) for the output diode, it results in a circuit with a high weighted efficiency of 96.8%. Chapter 3 improves upon that topology by adding an optimized modulation scheme to the control strategy. This improves the power stage efficiency at nominal input and enhances the available operating range. The new, hybrid-frequency method utilizes areas where the modulator operates in constant-on, constant-off, and fixed-frequency conditions depending on duty cycle, the resonant period length, and the desired input range. The method extends the operating range as wide as 12-48V and improves the CEC efficiency to 97.2% in the 250-W prototype. Chapter 4 considers the soft-start of the proposed system, which can have a very large capacitive load from the inverter. A new capacitor-transient limited (CTL) soft-start method senses the ac transient across the resonant capacitor, prematurely ending the lower switch on-time in order to prevent an excessive current spike. A prototype design is then applied to the IBR system, allowing safe system startup with a range of capacitive loads from 2μF to 500μF and a consistent peak current without the need for current sensing. Chapter 5 further investigates the impact of voltage ripple on the PV output power. A new method for analyzing the maximum power point tracking (MPPT) efficiency is proposed based on panel-derived models. From the panel model, an expression demonstrating the MPPT efficiency is derived, along with a ripple "budget" for the harmonic sources. These ripple sources are then analyzed and suggestions for controlling their contributions are proposed that enable circuit designers to make informed and cost-effective design decisions. Chapter 6 illustrates

how results from a previous iteration can provide a basis for the next generation's design. A zero-voltage-switching (ZVS) version of the circuit in Chapter 2 is proposed, requiring only two additional MOSFETs and one inductor on the low-voltage side. The maximum switching frequency is then increased from 70kHz to 170kHz, allowing for a 46% reduction in converter volume (from 430cm^3 to 230cm^3) while retaining greater than 97% weighted efficiency.

Dedication

In memory of my grandfather, William L. York (1921-2005), whose courageous example continues to encourage and inspire.

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As this kind of endeavor would be impossible without incredible guidance, I would like to thank my advisor, Jason Lai, and my committee members, Virgilio Centeno, Douglas Nelson, Kathleen Meehan, and Wensong Yu for their direction and support throughout this process. Equally impossible would be this pursuit without financial support, which has been wonderfully provided by the U.S. Department of Energy's SunShot Initiative. I have had the pleasure of working with DOE representatives Holly Thomas, Alvin Razon, and Kevin Lynn, whose interest and enthusiasm have been a great boon to my studies. In the first few years of my graduate studies, I was the grateful recipient of a fellowship from the Bradley Foundation, which allowed me to focus solely on research from an early point.

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Finally, I am eternally grateful to my Lord and Savior Jesus Christ who is the way, the truth, and the life.

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Nomenclature

$\%r_{bus}$	Percent ripple measured at the inverter dc-link
α, β, γ	PV current-voltage curve fitting coefficients
ΔE	Energy transferred during one-half inverter line cycle
ΔQ_{C2}	Charge leaving C_2 during mode 1
Δt_{1-2}	Decay time for primary current after mode 1
ΔV	Inverter dc-link ripple voltage
ΔV_{C2}	Voltage change across C_2 during mode 1
ΔV_{C2}^{*}	Expected Voltage change across C_2
ΔV_{C4}	Change in C_4 voltage per switching cycle
η_{MPPT}	Converter MPPT efficiency
ω_C	Cut-off frequency of filter circuit
$\widehat{v}_{C2}$	Ac magnitude of capacitor transient
$\widehat{v}_{sense}$	Ac magnitude of sensed voltage transient
A_c	Transformer core cross-sectional area [cm^2]
B_{ac}	Transformer ac flux density [T]
C_b	Inverter dc-link capacitance
C_1, C_2	Primary-side resonant capacitors
C_3, C_4	Secondary-side resonant capacitors
C_5	Output Capacitance

C_B	Dc blocking and filter capacitor
C_{in}	Micro-converter input capacitance
C_{oss}	MOSFET drain-source parasitic capacitance
C_{pri}, C_{sec}	Value of high- and low-side resonant capacitors (equal C design)
D	Duty cycle of lower MOSFET (Q_2)
D_1,D_2	Independent switching leg duty cycles (IBR-Z)
D_1, D_2	Upper and lower output diodes
$D_{\max}$, $D_{\min}$	Maximum and minimum required values of duty cycle
F_{sw}	Converter switching frequency
G_{vd}	Boost converter duty-input transfer function
G_{vv}	Boost converter "grid susceptibility"
H_{comp}	Input voltage compensator transfer function
I_m	Inverter output current magnitude
i_{grid}	Inverter output current
$I_{L,avg}$, $I_{L,RMS}$	Average and rms values of the inductor current
$I_{LK,pk-}$	Negative peak of transformer primary current
I_{LK}	Transformer primary-side (leakage) current
I_L	Input (boost) inductor current
$i_{pk,-}$	Negative peak of the input inductor currents (IBR-Z)
i_{pri}, i_{sec}	Transformer primary and secondary currents
L	Input (boost) inductor
L_1, L_2	Interleaved input inductors (IBR-Z)
L_K	Transformer leakage inductance
n	Transformer turns ratio
n_{pri}, n_{sec}	Number of primary and secondary turns on the transformer

p_{bus}	Power transferred from the inverter's dc bus
P_{mpp}	Maximum power available the MPP
P_{out}	Converter output power
$P_{PV,avg}$	Average power extracted from the PV panel
$P_{SW,Q1}$, $P_{SW,Q2}$	MOSFET switching loss
Q_3, Q_4	Additional primary-side MOSFETs (IBR-Z)
Q_{1-2}	Charge transferred through L_K during modes 1-2
Q_1, Q_2	Upper and lower primary-side MOSFETs
Q_{oss}	MOSFET output charge
Q_X, Q_Y	Boost stage MOSFETs
r_r	Ripple rejection ratio from converter output to input
R_A, R_B	Filtering and bias resistors
R_{load}	Secondary-side load resistance
r_s	PV panel effective series resistance
$T_{\max}$, $T_{\min}$	Maximum and minimum switching periods (hybrid frequency)
t_{del}	Time delay in trip circuit
T_{on}, T_{off}	Conduction time for Q_2 and Q_1, respectively
$T_{res1,\max}$, $T_{res2,\max}$	Maximum limits on the resonant period lengths
T_{res1}, T_{res2}	Lengths of operating modes 1 and 2
t_{RI}, t_{FI}	Rise and fall times of MOSFET drain current
t_{RV}, t_{FV}	Rise and fall times of MOSFET drain-source voltage
T_{sw}	Switching period ($1/F_{sw}$)
V_m	Inverter output voltage magnitude
V_{avg}	Average inverter dc-link voltage
V_{bus}	Voltage at the intermediate bus (across C_1 and C_2)

V_{C1}, V_{C2}	Primary-side capacitor voltages
V_{C3}, V_{C4}	Secondary-side capacitor voltages
V_{core}	Transformer core volume [cm^3]
V_{DB}	Voltage drop across protection diode
V_{DD}	Sensing or logic voltage level
v_{grid}	Inverter output voltage (at PCC)
$V_{in,\max}$, $V_{in,\min}$	Maximum and minimum required input voltage
V_{in}, V_{out}	Steady-state input and output voltage
V_{mpp}, I_{mpp}	PV maximum power point voltage and current
V_n	PV voltage ripple harmonic amplitude
V_{oc}, I_{sc}	PV open-circuit voltage and short-circuit current
$V_{out,pk-pk}$	Output voltage ripple, measured peak to peak
V_{sense}	Bias level of sensing circuit
V_{step}	MPPT algorithm minimum step-size
V_{sw1},V_{sw2}	Independent switch-node voltages (IBR-Z)
v_{sw}	Switch-node voltage
v_{track}	MPPT ripple voltage
V_{trip}	Trip sensitivity of capacitor transient
V_{TRK}	MPPT ripple harmonic summation
VS_{peak}	Transformer peak volt-second product

Subscripts

avg	Average value
pk	Peak value
RMS	Root-mean-square value

Acronyms

AFCI	Arc-fault current interrupter
CCM	Continuous Conduction Mode
CTL	Capacitor Transient Limited (soft-start)
DCM	Discontinuous Conduction Mode
DCX	Unregulated dc-dc transformer
DLF	Double-line frequency
EMI	Electro-magnetic interference
HF	Hybrid-Frequency (modulation)
IBR	Integrated Boost Resonant (converter)
IBR-Z	Integrated Boost Resonant (converter) with ZVS
IncCond	Incremental conductance
MPP	Maximum power point
MPPT	Maximum power point tracking
NOCT	Normal Operating Cell Temperature
P&O	Perturb and observe
PCC	Point-of-common-coupling
PCS	Power conditioning system
PV	Photovoltaic
RCC	Ripple correlation control
THD	Total harmonic distortion
ZCS	Zero-current-switching
ZVS	Zero-voltage-switching

Chapter 1

Introduction

Edmund Becquerel discovered the photovoltaic effect in 1839, demonstrating the production of a device that, when exposed to light, would generate electric current. Over a century later, scientists at Bell Labs built the first silicon solar cell, ushering in a decades-long struggle in a fight for clean, renewable energy. [1] In more recent history, the last decade or so has seen a tremendous amount of growth in the photovoltaic (PV) industry. Rising prices for traditional fossil fuel sources, coupled with rapidly falling prices for poly-crystalline silicon panels, has resulted in an increased adoption rate for PV systems.

In order to bring PV systems from the realm of intellectual curiosity to viable energy source, creating a method to extract, convert, and distribute the harvested energy is paramount. Though remote, or stand-alone, applications of PV panels are appropriate in some instances, general and widespread usability of PV requires connection to the electric

utility system. In the overwhelming majority of locales, this utility network consists of alternating current (ac) generation, transmission, and distribution. This poses some difficulty since PV panels naturally produce direct current (dc). In order to adapt the dc source to the ac system, a power conditioning system (PCS) is required.

1.1 PV System Architectures

In order to connect a PV system to the utility, the fundamental required unit is the inverter, which directly creates an ac output from a dc input. At the large scale (>100kW) the centralized inverter, shown in Fig. 1.1, is far and away the most popular approach. With this type of inverter, all of the source PV panels are combined in a series-parallel configuration, up to the inverter's maximum power rating. These inverters are physically quite large, and often have their own dedicated line-frequency transformers for isolation and voltage scaling. This solution has the benefit of the lowest PCS cost in dollars-per-kilowatt ($/kW) as well as the least complex to operate and maintain.

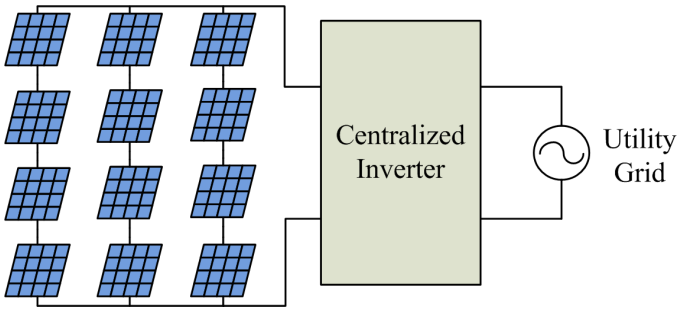

Figure 1.1: Centralized inverter structure

However, their are quite a few drawbacks to centralizing the entire PCS. Perhaps

the most significant stems from an inability to individually optimize the output from each panel. From the PV cell current-voltage characteristic, it is clear that there is one operating point which produces the largest output power, which is known as the cell's (or panel's) maximum power point (MPP). This MPP, however, varies significantly based on factors such as cell construction, temperature, shading, or light intensity (irradiance). Because these characteristics are not uniform across all of the cells in the system, and a centralized inverter can only select one operating point for the entire array, the globally achievable optimum power can be significantly less than the sum of the individual panels' optimum power [2]–[4]. A similar effect occurs if the panel age, type cell counts, or power levels are mismatched. Considering the rapid evolution of PV technology, it is unlikely that the same panel model will be available even a year after it is introduced. This implies a significant performance penalty to the centralized system if the panels are bought piecemeal. Scalability of centralized systems, given the inherently large power level, is also of interest. This may not pose a problem for large, utility-scale installations, but it makes the centralized solution somewhat unwieldy for more modest commercial or residential sites.

Another critical issue with the centralized inverter approach is the difficulty of detecting, isolating, and repairing faults at the panel level. With the large number of panels in such a system, additional dedicated hardware, such as an arc-fault current interrupter (AFCI), is required just to detect PV faults. Even if the fault is successfully detected, it is very difficult to isolate and repair. The entire PV system must cease operation until the fault is cleared. During repairs, technicians must work around relatively high dc voltages

(> 400V) as the unaffected panels are still connected, even if they are not sending power to the grid.

Similar to the centralized inverter, the string inverter, shown in Fig. 1.2, attempts to isolate a single "string" of panels, thus all of the panels are connected in series rather than series-parallel. These inverters typically have a lower power rating (< 20kW) and may (or may not) have internal isolation. The hardware cost is typically higher than the centralized inverter but typically features improved energy harvesting, scalability, and fault detection/isolation.

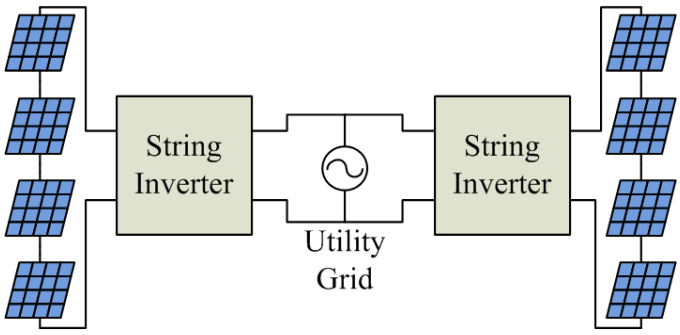

Figure 1.2: String inverter structure

Counter to both the centralized and string inverters is the so-called micro-inverter, shown in Fig. 1.3. This type of structure places a dedicated, low-power inverter on each panel, connecting the output directly to the utility, using an ac interconnect. This approach provides the best practical energy harvest, short of applying a PCS directly to the individual cells. [5] This approach is also ideal for handling mismatched panels, providing a nearly infinite scalability. However, this technique suffers from a relatively high PCS hardware cost, making it difficult to justify for more developed installations. Control and monitoring

also becomes more challenging as each panel maintains its own grid connection. There are also concerns with regard to PCS maintenance and lifetime. An inverter generates a double-line-frequency ripple voltage on the dc side, which can only be mitigated by using additional capacitance as an energy buffer. In order to acquire enough capacitive energy storage, inverters must often rely on electrolytic capacitors, which have noted lifetime concerns when exposed to the extreme temperature and climate variations common in outdoor installations.

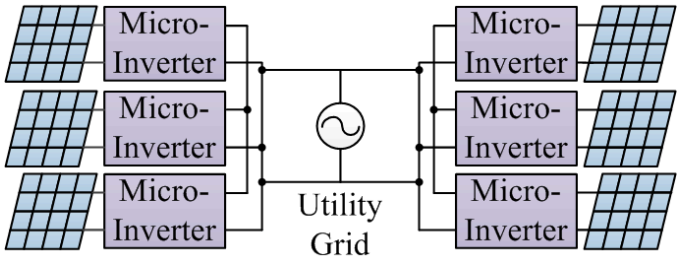

Figure 1.3: Micro-inverter structure

Stepping back from an individual configuration, in order to be effective any PV PCS needs to implement a certain feature-set focused around transferring energy safely and reliably. A summary list is provided in Table 1.1, but it should not be considered exhaustive. These functions fall into three categories: panel management, interconnect, and utility interaction. Some of these features, such as maximum power point tracking (MPPT) or arc-fault isolation, are best implemented in a distributed network. Other features, such as inversion or smart grid communication, do not need distribution and are more cost-effective when implemented centrally. In order to take advantage of having distributed PCS, while being able to centralize and reduce cost and complexity on other functions, a hybrid solution seems most advantageous.

Table 1.1: Required PV PCS System Functions

Panel Management	**Combination/Adjustment**	**Utility Connection**
MPPT	Combination	AC Conversion
Cell Bypass	Voltage Stabilization	Synchronization
Panel Protection	Arc Fault Isolation	Ride-through
Instrumentation		Smart Grid Functions

A hybrid solution of this type requires two elements, a distributed network of dc-dc power converters and a centralized dc-ac inverter. How to organize the network, and subsequently design the elements, is of significant importance. One option that has gained some commercial viability is the series dc-dc optimizer. These converters are typically low-cost and non-isolated, with outputs nominally equal to the individual panel input level (< 80V). These outputs are then connected in series to form a new type of PV "string." This solution provides the distributed MPPT and instrumentation but suffers from two critical disadvantages. One is that the ability to isolate and repair faults remains similar to the string inverter, as the remaining converters must be disconnected from the inverter in order to perform maintenance. Secondly, the converters cannot provide full output power at a constant voltage in the presence of panel mismatch. [6] Thus, the output of one panel still impacts the surrounding panels without complex control and communication.

An alternative to the series dc-dc optimizer is a massively parallel network of dc-dc converters which individually generate the full voltage required for the inverter's utility connection. This type of converter (henceforth referred to as a "micro-converter" and shown in Fig. 1.4) provides the distributed functions required, allows for panel fault isolation, and removes any coupling effect between panel outputs. This approach has seen little traction

in the commercial space, but is the subject some technical literature, most notably [7]–[9], and at least two recent patents [10] and [11].

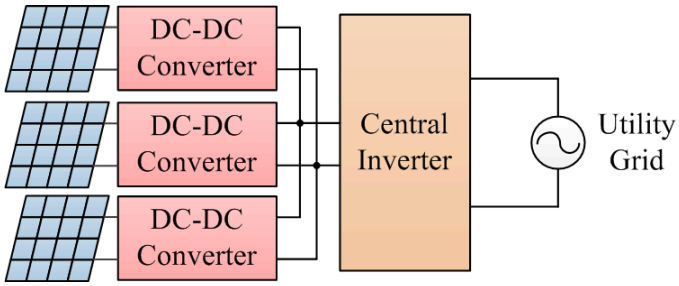

Figure 1.4: Micro-converter structure

1.2 Motivation for Research

Among the various solutions to the PV infrastructure problem, two camps seem to emerge, centralized and distributed. Both groups are significantly developed with proponents of either method. The micro-converter architecture provides the best opportunity to maintain the key advantages of both groups. However, the requirements for these distributed micro-converters are non-trivial. They must provide a high boost-ratio in order to generate an inverter-compatible dc-link voltage. They must also handle a wide range of input voltage and power levels, doing so with high efficiency and reliability. Due to the unique challenges presented by this application, it is difficult to adapt an existing converter technique to suit. Rather, it is advantageous to develop new techniques based on the characteristics inherent to the problem itself. Moreover, a successful design requires application-oriented design on several levels, with a certain degree of vertical integration. The circuit topology must be

developed such that it fulfills the required input and output characteristics, and does so efficiently. The modulation and control techniques must optimize the behaviors of that individual topology and enable it to operate effectively in-system. Care must be taken to handle transient conditions, such as start-up and shut-down, as well as to optimize the steady-state behavior of the system. Therefore, it is the goal of this research not only to demonstrate an effective micro-converter, but also to develop effective application-oriented technologies in an integrated manner. Specifically, the desired micro-converter characteristics should be as follows:

- High weighted efficiency (>97%)
- Small size (<250cm^3)
- Current-limited startup of inverter system (with bus capacitance >500μF)
- Improved MPPT efficiency (>99.8%)

This work begins with a discussion of micro-converter circuit requirements, and the proposal of a new topology (Chapter 2) and a unique modulation scheme (Chapter 3), in order to achieve the desired power stage efficiency. Chapter 4 introduces a unique soft-start method, to allow even a single micro-converter to successfully charge even a large inverters bus capacitance. A new modeling method for evaluating MPPT efficiency is provided in Chapter 5, which allows circuit designers to cost-effectively meet the desired goals for PCS ripple. Finally, the initial topology is augmented in Chapter 6 with a soft-switching technique that allows for significant size reduction, down to the targeted converter volume.

Chapter 2

The Integrated Boost Resonant Converter

Power conversion for photovoltaic (PV) applications, as opposed to more conventional dc-dc converter configurations, requires an adaptable system that is capable of responding to a wide range of input voltage and current conditions. As previously stated in literature, PV voltage varies significantly with panel construction and operating temperature, while the PV current changes largely due to solar irradiance and shading conditions [12]. If a converter is designed only for high peak efficiency, oftentimes the range of conditions common to many PV installations will force the converter into another operating region where it is much less efficient. In 2004, the California Energy Commission (CEC) introduced a weighting system for efficiency based on statistical climate data for the Southwestern United States. Their intention was to develop a standard metric for informing consumers about the effectiveness

of PV inverters in conditions similar to Southern California, hoping to capture PV output variation over the course of an average day. Since that time, CEC efficiency has become the de-facto standard for evaluating PV related equipment, at least in the US marketplace. Weighting coefficients for calculating CEC efficiency are provided in Table 2.1. From the published weights, clear emphasis is placed on efficiency in the mid-power region (50 % and 75% count for nearly three-fourths of the weighted value) and light-load efficiency clearly over heavy load. For a generated report, data is taken at the lowest rated input voltage, a nominal input, and the highest rated input. However, the single number that is classified as the official CEC efficiency only consists of data taken at the nominal input. This encourages equipment manufacturers to push for a wide operating range, but to ensure that efficiency is optimal at the median input voltage and in the middle of the power range. [13], [14].

Table 2.1: CEC Efficiency Weighting

Power	**Weight**
10%	0.04
20%	0.05
30%	0.12
50%	0.21
75%	0.53
100%	0.05

Also of interest in the PV PCS design process is the necessity of galvanic isolation between the PV panel and the electric utility system. While an ungrounded, grid-connected PV array is permitted by many electric codes, galvanic isolation can be preferred for several reasons. Because the center-tap of the transformer at the utility point-of-common-coupling (PCC) is typically connected to earth ground, the PV panel must remain electrically "float-

ing" with respect to ground. The metal frame surrounding the PV cells, on the other hand, must be grounded for safety and protection against lightning surge. This makes the PV panel susceptible to high-frequency switching currents that propagate through the frame-panel parasitic capacitance, as shown in Fig. 2.1. This capacitive loop effect can result in additional electro-magnetic interference (EMI), loss in passive components, and total harmonic distortion (THD) in the grid current. Secondly, much like the value of line-frequency transformers in traditional ac systems, an isolation transformer in a dc-dc converter allows much greater voltage gain, without residual impact on the primary-side voltage stress. Finally, because there is no direct electrical connection between the primary and secondary sides of the transformer, the PV panel is completely disconnected from the rest of the system while the converter is off. This allows for a much higher degree of safety for the PV panel, as well as any repair technician, during abnormal operating or fault conditions. [15]–[17]

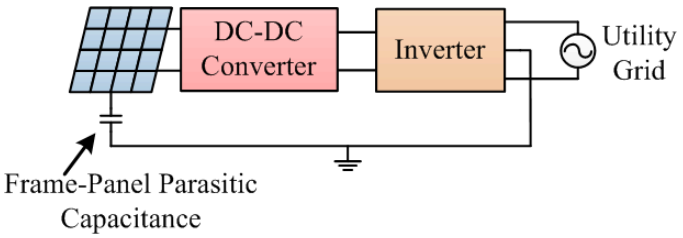

Figure 2.1: Frame-PV capacitive loop effect

It is this combination of high CEC efficiency, galvanic isolation, and a localized, distributed approach to energy conversion that has prompted the proceeding technical development. In literature there have been a variety of different methods proposed for micro-conversion, both isolated and non-isolated [18]–[23]. For reasons mentioned previously, the proceeding discussion is limited to isolated topologies.

In the distributed PV PCS, the isolated dc-dc stage must operate efficiently at full-power, while maintaining high performance at light load, across a range of PV voltages. In order to maintain high efficiency under low power conditions, it is necessary to minimize the amount of circulating energy in the system. An alternate definition of this characteristic would be producing a system with a high "power factor" at the isolation transformer. Also critical to light load efficiency is mitigating the device switching loss. Finally, reduction of the control and gate drive complexity allows for lower fixed losses due to auxiliary power requirements. When considering potential PV conversion solutions, addressing these loss mechanisms is critical to a successful design.

One popular option for the dc-dc conversion stage is a simple continuous-current-mode (CCM) flyback converter [24], [25], shown in Fig. 2.2. It has the benefit of simple construction and low circulating energy. However, the switching loss for both the primary switch and the diode can be quite large, and the overall system efficiency is typically low ($< 90\%$). Improvements in flyback efficiency can be made using variants such as zero-voltage-transition (ZVT) or Active Clamp, both of which use the transformer leakage inductance as a resonant element to achieve zero-voltage-switching (ZVS) across the main device [26], [27]. However, this effectively trades switching loss for circulating energy, reducing efficiency at high line or low power.

Other options are the series-resonant converter (SRC) and more recently the LLC resonant converter shown in Fig. 2.3, both of which operate on a similar principle and typically use a variable frequency control to adjust the output voltage [28]–[30]. When the SRC or LLC

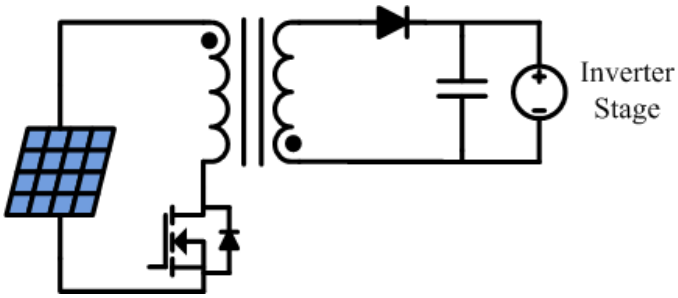

Figure 2.2: Flyback converter circuit

converter is operated near the resonant frequency of the tank circuit, the converter achieves nearly zero-voltage and zero-current switching with very low circulating energy, giving it a high peak efficiency. Traditional voltage and current waveforms for an SRC are provided in Fig. 2.4. Control of the converter's voltage gain is achieved by interrupting the current into the transformer; thus, the greater the switching frequency, the more dramatically the transformer's natural resonance is interrupted. As the switching frequency diverges further from the resonant frequency, the amount of circulating energy increases. Unfortunately the normal conditions for PV conversion will often push the converter significantly away from the optimum switching frequency, causing the CEC efficiency to suffer. Several authors have proposed methods to extend the line and load range of the LLC, once again complicating the circuit topology and control [31]–[33].

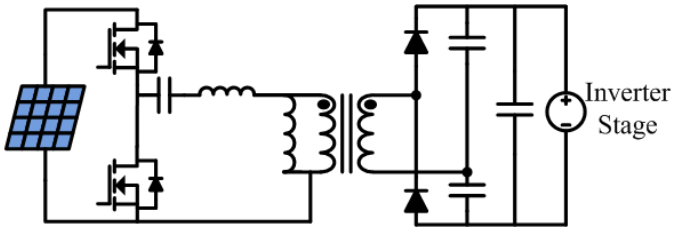

Figure 2.3: LLC resonant converter circuit

Other authors have proposed using the series-resonant converter as an unregulated dc-

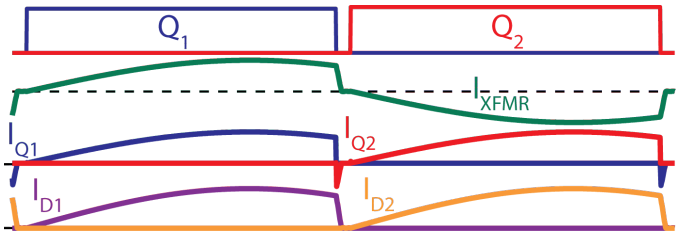

Figure 2.4: SRC converter sample waveforms

dc transformer (DCX) [34], [35]. The DCX behavior is achieved in the SRC by allowing the resonant period to fully complete. Once the resonance is finished, the output diodes prevent any continued resonance, which causes the circuit to operating in a kind of discontinuous conduction mode (DCM). Typical waveforms of the series-resonant DCX are shown in Fig. 2.5. This approach has the benefit of almost no switching loss, little or no circulating energy, very high peak efficiency, and integrated isolation. However, the inverter stage must be able to regulate over a wide input range because the PV voltage fluctuates so dramatically, causing extremely poor overall system efficiency.

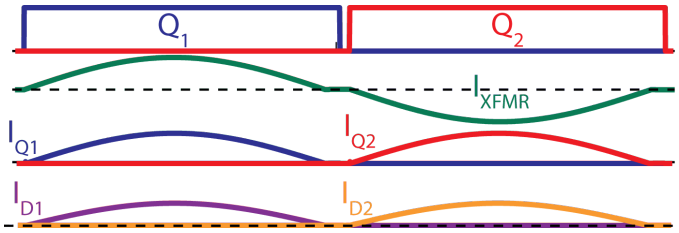

Figure 2.5: DCX sample waveforms

This concept of using the series-resonant DCX is not without merit, but the system requires an additional element to provide regulation capability. The method proposed in the following section integrates a traditional boost converter element into the DCX with only the addition of a single inductor. The overall design is straightforward and may be

controlled using simple fixed-frequency PWM with only the need to observe limitations on the maximum and minimum duty cycle. For PV applications, this circuit satisfies the need for galvanic isolation, low switching loss (the output diodes achieve zero-current switching (ZCS)), minimal circulating energy, as well as simple gate drive and control.

2.1 Converter Synthesis and Operation

When considering the series-resonant DCX, it is important to notice the half-wave resonant behavior by which it operates. During the on-period of either switch a resonant circuit is formed by a combination of the input-side capacitors, the output-side capacitors, and the transformer leakage inductance. The unidirectional nature of the output diodes prevents this circuit from resonating perpetually, and instead only a resonant period consisting of one half-sine wave is visible. Provided that this resonant period is allowed to complete fully before the primary-side switches change states, the series-resonant circuit is naturally soft-switching on both turn-on and turn-off (ZVS and ZCS). If both resonant periods are allowed to fully complete, the system has no method by which to regulate the output, and the output is simply a reflection of the input. Hence, the necessary addition of another "regulating element", in this case a boost converter, is shown in Fig. 2.6. The boost converter regulates the effective input voltage to the series-resonant converter, allowing it to run as a DCX with high efficiency. The cost is two additional transistors, with their associated gate drive requirements, and some additional switching and conduction loss.

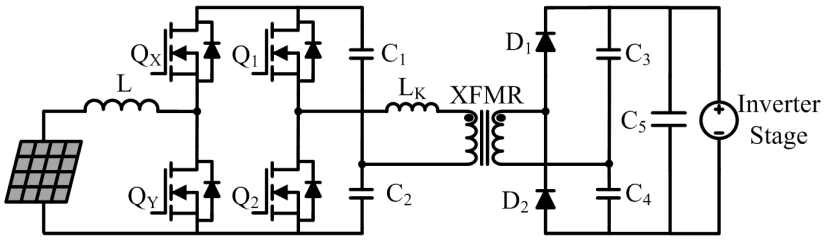

Figure 2.6: Resonant half-bridge with separate boost input stage

This circuit may be further simplified by integrating the system so that the boost converter function is implemented by the original two MOSFETs. A straightforward method to understand this is to directly tie the input inductor to the midpoints of both active switching legs simultaneously. Note that this change directly ties the inductor to one terminal of the transformer. This additional connection renders the upper MOSFETs (Q_X and Q_1) as well as the lower MOSFETs (Q_Y and Q_2) in parallel, so long as their switching patterns are synchronized. Thus, the circuit may be simplified, with the additional connection and the removal of Q_X and Q_Y, into the topology shown in Fig. 2.7. Because the now single upper and lower FETs (Q_1 and Q_2) are effectively replacing two parallel FETs, they carry the combined current from the original four switches. Also, as long as the resonant behavior is allowed to complete, the output diodes, D_1 and D_2, still achieve ZCS.

This particular circuit topology is similar to that of the "Boost Half-Bridge" (BHB) [36]–[40] and the circuit in [41]; however, the actual operation of this circuit is quite different. In the BHB, the operating currents are that of the hard-switching half-bridge, giving the converter a poor power factor at the transformer. This makes it difficult for the converter to achieve a wide-range of operation, even with ZVS. Also, the voltage transfer ratio is highly non-linear, leading to much more complex control requirements. Unlike the circuit in [41],

this circuit is unidirectional and can be operated under strictly PWM.

On the other hand, this new circuit features a very simple voltage transfer ratio, given in (2.1), where n is the transformer turns ratio, and D is the duty cycle of the lower switch, Q_2. Unlike the BHB, this transfer ratio is constant over input, load, and frequency.

$$\frac{V_{out}}{V_{in}} = \frac{n}{1-D} \tag{2.1}$$

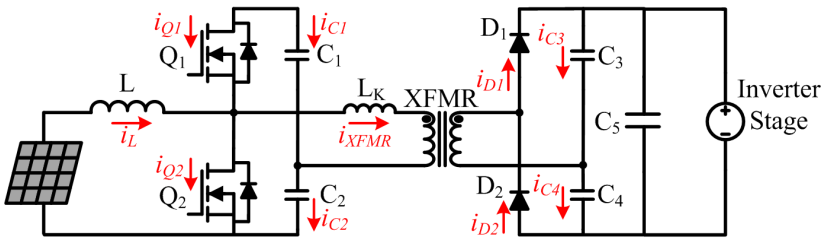

Figure 2.7: Integrated boost resonant (IBR) converter

This voltage transfer ratio (2.1) is identical between the circuit shown in Fig. 2.6 and Fig. 2.7, indicating that only one pair of switches is necessary to provide controllability. Also, the transfer characteristic is similar to that of a continuous conduction mode (CCM) boost converter, simply multiplied by n. The new topology can be effectively broken down into four distinct operating modes, shown in schematic form in Fig. 2.8(a)-(d), and as sections in the timing diagram provided in Fig. 2.9.

Mode 1 *[$t_0 < t < t_1$,* ***see Fig. 2.8(a)****]*:

Beginning with the turn-off of Q_2 prior to t_0, the current in the input inductor, L,

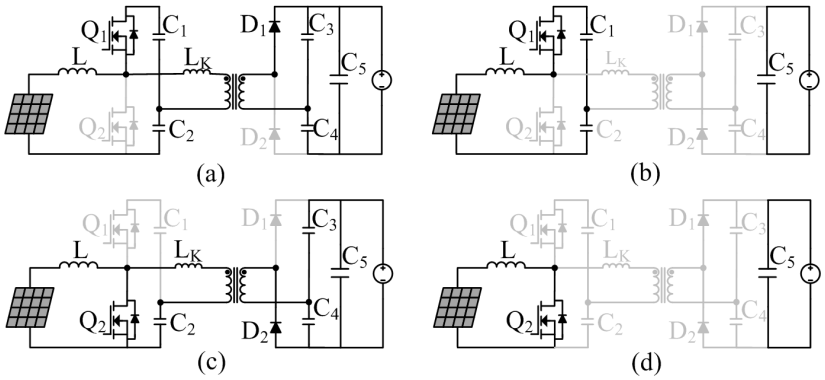

Figure 2.8: Integrated boost resonant converter operating modes

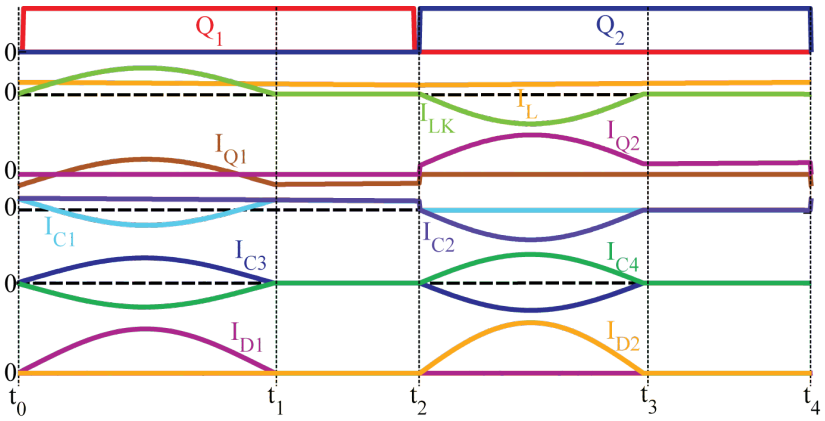

Figure 2.9: Timing diagram showing circuit operating modes

flows into the body diode of Q_1, discharging its parasitic capacitance. This allows Q_1 to be turned on under ZVS conditions at t_0. At this time the upper input-side capacitor, C_1, begins resonating with the transformer leakage inductance, L_K, and the output-side capacitors, C_3 and C_4, through D_1. Simultaneously, the input current begins charging the series combination of C_1 and C_2. During this phase, Q_1 carries the difference between the transformer current, flowing from C_1 through the positive terminal of the transformer and the input current. Once the transformer current resonates back to zero, D_1 prevents the continued resonating in the reverse direction, ending mode 1. The length of mode 1 is given

by (2.2).

$$T_{res1} = \pi\sqrt{L_K\left[\frac{n^2(C_1+C_2)(C_3+C_4)}{C_1+C_2+n^2(C_3+C_4)}\right]} \tag{2.2}$$

***Mode 2** [$t_1 < t < t_2$**, see Fig. 2.8(b)**]*:

Q_1 is still active, yet it is only conducting the input inductor current, which is still decreasing, a pathway which is shown in Fig. 2.8(b). The resonant elements all conduct zero current during this interval. Only C_5 continues discharging into the load at this time. Mode 2 ends with the turn-off of Q_1 and the subsequent turn-on of Q_2.

***Mode 3** [$t_2 < t < t_3$**, see Fig. 2.8(c)**]*:

After the turn-off of Q_1, but prior the turn-on of Q_2, the inductor current is still shunted into charging the series combination of C_1 and C_2, this time through the body diode of Q_1, and still decreasing almost linearly. When Q_2 is turned on, the body diode of Q_1 is hard-commutated, causing some switching loss. At t_2, C_2 begins to resonate with L_K and the parallel combination of C_3 and C_4, through the diode D_2. Simultaneously, the inductor current also flows through Q_2, increasing linearly. During this interval, Q_2 carries the sum of the transformer current and the inductor current. Thus, the rms current through Q_2 is significantly larger than that of Q_1, which carries the difference of the two currents. Once the transformer current resonates back to zero, D_2 blocks the continued oscillation, marking the end of mode 3. The total time interval of mode 3 is determined by the length of the resonant period, given in (2.3).

$$T_{res2} = \pi\sqrt{\frac{n^2 L_K C_2(C_3 + C_4)}{C_2 + n^2(C_3 + C_4)}} \tag{2.3}$$

Mode 4 *[$t_3 < t < t_4$,* ***see Fig. 2.8(d)****]*:

The inductor current continues to flow through the lower device, increasing until Q_2 is turned off and the circuit returns to mode 1. Also, during both modes 3 and 4, Q_1 effectively isolates the upper capacitor from charging or discharging.

Note that there is a significant difference in the circuit behavior between the two resonant modes (1 & 3). During mode 3, C_1 is effectively isolated from the rest of the circuit due to the presence of Q_1. However, during mode 1, C_2 has an ac discharge path through the PV source and the input inductor, allowing the two input capacitors (C_1 and C_2) to appear in parallel, though the resonant current is not shared evenly between them. Thus, the length of mode 1 can be significantly longer than mode 3, depending on the relative sizing of C_1-C_4 and the transformer turns ratio, n. Optimizing the resonant period length will be a core component of the design procedure outlined in the proceeding section.

2.2 Design Procedure and Loss Analysis

1. *Determine Duty Cycle Limits from Input Requirements*

   The most critical element of this design procedure is the identification of the input voltage requirements, so that the duty cycle range is fully utilized. With this converter

there is a direct trade-off between increased input range and lower rms currents in the circuit. The most basic method involves setting the maximum and minimum duty ratios such that the middle of the input range results in a 50% duty cycle at the converter, an approach provided via (2.4) and (2.5).

$$D_{\max} = \frac{V_{in,\max}}{V_{in,\min} + V_{in,\max}} \tag{2.4}$$

$$D_{\min} = 1 - D_{\max} \tag{2.5}$$

With the nominal input assigned to have a 50% duty cycle, the bus voltage, V_{bus}, which is measured across C_1 and C_2 can be calculated by (2.6).

$$V_{bus} = V_{in,\max} + V_{in,\min} \tag{2.6}$$

However, it may be necessary to adjust Vbus to accommodate voltage stress requirements on devices or to meet certain standards. If this is necessary, V_{bus}, D_{max}, and D_{min} can be altered by using (2.7), (2.8), and (2.9), respectively.

$$V_{bus} = V_{in,\max} + V_{in,\min} \tag{2.7}$$

$$D_{\max,adj} = 1 - \frac{V_{in,\min}}{V_{bus,adj}} \tag{2.8}$$

$$D_{\min,adj} = 1 - \frac{V_{in,\max}}{V_{bus,adj}} \tag{2.9}$$

2. *Determine Maximum Resonant Period Lengths*

   With the maximum and minimum duty ratios known, the limits for the resonant periods T_{res1} and T_{res2} may be calculated based on the desired switching period T_{sw} utilizing (2.10) and (2.11).

$$T_{res1,\max} = (1 - D_{\max})\, T_{sw} \tag{2.10}$$

$$T_{res2,\max} = D_{\min} T_{sw} \tag{2.11}$$

3. *Design Transformer*

   Based on the calculated Vbus and the desired output voltage, Vout, (2.12) can be used to calculate the necessary transformer turns ratio, n.

$$n = \frac{n_{\sec}}{n_{pri}} = \frac{V_{out}}{V_{bus}} \tag{2.12}$$

The transformer design process can be carried out under a number of different procedures, however, the peak V-s product, provided in (2.13), is often a useful quantity

when determining the transformer flux density, core size, and number of primary turns.

$$VS_{peak} = V_{bus}T_{sw}/4,\ [V \cdot s] \tag{2.13}$$

When determining the winding current density, and therefore the required winding gauge and copper loss, the rms current through the primary and secondary windings may be determined from (2.14) and (2.15). These equations were derived by integrating the square of the transformer currents over one switching cycle. Note that R_{load} is the load resistance for a given output power level. At this stage, the maximum values for T_{res1} and T_{res2}, as calculated in step 2 may be used. They may be replaced once the values are determined more specifically in step 5.

$$i_{RMS,XFMR,pri} = \frac{\pi}{2}\left(\frac{nV_{out}}{R_{load}}\right)\sqrt{\frac{T_{sw}}{2}}\left(\sqrt{\frac{1}{T_{res1}} + \frac{1}{T_{res2}}}\right) \tag{2.14}$$

$$i_{RMS,XFMR,\text{sec}} = \frac{\pi}{2}\left(\frac{V_{out}}{R_{load}}\right)\sqrt{\frac{T_{sw}}{2}}\left(\sqrt{\frac{1}{T_{res1}} + \frac{1}{T_{res2}}}\right) \tag{2.15}$$

4. *Design Input Inductor based on allowable current ripple*

Multiple criteria may be used for designing the input inductor. In PV applications, especially for accurate MPPT, the inductor current ripple must be regulated. The equation (2.16) specifies the input inductance based on the maximum allowable current

ripple (which occurs at $D = 0.5$).

$$L = \frac{V_{bus} T_{sw}}{4 I_{L,avg} \%_{ripple,\max}}, \text{ [H]} \tag{2.16}$$

For both inductor design and loss analysis, the rms current through the inductor may be calculated by (2.17), once again with the maximum rms for a given $I_{L,avg}$ occurring at a 0.5 duty ratio. This equation was derived by integrating the square of the inductor current over one switching cycle.

$$I_{L,RMS} = \sqrt{{I_{L,avg}}^2 + \frac{D^2 {V_{in}}^2 {T_{sw}}^2}{12 L^2}} \tag{2.17}$$

5. *Resonant Capacitor Design*

With the magnetics design complete, it is now possible to design the resonant capacitors $C_1 - C_4$. In order to reduce the rms currents in the circuit, the resonant period needs to be as close to the calculated maximum as possible. Because the leakage inductance of the transformer, L_K, is involved in the resonant circuit and is a consequence of the transformer design in step 3, it is left as a constant here. The full equation for calculating T_{res1} is given in (2). In order to simplify the design process, C_1 and C_2 as well as C_3 and C_4 may be set to equal values, C_{pri} and C_{sec}, respectively, simplifying the result from (2) into (2.18). If the duty cycle was not adjusted as in the second half of step 1, then T_{res2} is not necessary to design. Otherwise, T_{res2} may be calculated

fully in (3) or with "equal C's" in (2.19).

$$T_{res1} = \pi\sqrt{L_k\left[\frac{2\left(C_{pri}\right)\left(n^2C_{sec}\right)}{C_{pri}+n^2C_{sec}}\right]} < T_{res1,\max} \tag{2.18}$$

$$T_{res2} = \pi\sqrt{\frac{2L_kn^2C_{pri}C_{sec}}{C_{pri}+2n^2C_{sec}}} < T_{res2,\max} \tag{2.19}$$

In order to calculate the conduction losses in each of the capacitors, rms current calculations are provided in (2.20)-(2.23). These equations were derived by integrating the square of the capacitor current waveforms (C_3 and C_4 being purely resonant, while C_1 and C_2 are the combination of the inductor and transformer currents), over one switching cycle.

$$i_{RMS,C1} = \sqrt{\left(1-D\right){I_{L,avg}}^2 + \frac{\pi^2}{8}\left(\frac{nV_{out}}{R_{load}}\right)^2\frac{T_{sw}}{T_{res1}} - 2\left(\frac{nV_{out}}{R_{load}}\right)I_{L,avg}} \tag{2.20}$$

$$i_{RMS,C2} = \sqrt{\left(1-D\right){I_{L,avg}}^2 + 2\frac{T_{sw}}{T_{res2}}\left(\frac{n\pi}{4}\left(\frac{V_{out}}{R_{load}}\right)\right)^2} \tag{2.21}$$

$$i_{RMS,C3} = \frac{\pi}{4}\left(\frac{V_{out}}{R_{load}}\right)\sqrt{\frac{T_{sw}}{2}}\left(\sqrt{\frac{1}{T_{res1}}+\frac{1}{T_{res2}}}\right) \tag{2.22}$$

$$i_{RMS,C4} = \frac{\pi}{4}\left(\frac{V_{out}}{R_{load}}\right)\sqrt{\frac{T_{sw}}{2}}\left(\sqrt{\frac{1}{T_{res1}}+\frac{1}{T_{res2}}}\right) \tag{2.23}$$

A dc path exists between the input terminal and C_2, which causes the average voltage

across C_2 to be equal to V_{in}. The average voltage across C_1 can thus be written as in (2.24).

$$V_{C1,avg} = \frac{DV_{in}}{1-D} \tag{2.24}$$

6. *Output Capacitance*

The required output capacitance, C_5, can be determined from the allowable output ripple on the dc-link voltage, specified by (2.25). This equation is approximate, based on taking the average value of the resonant output current during one-half resonant period, subtracting the load current, dividing by the output capacitance, and multiplying by the resonant period length.

$$V_{out,pk-pk} = \frac{V_{out}}{R_{load}} \left(\frac{T_{sw}}{2T_{res2}} - 1 \right) \frac{T_{res2}}{C_5} \tag{2.25}$$

7. *MOSFET and Diode Selection*

Both of the primary side MOSFETs have a maximum voltage stress of Vbus and rms current stresses given by (2.26) and (2.26). Note that the current stress in Q_2 is much larger than that in Q_1, and that both current stresses are related to the ratio of T_{sw} and $T_{res1,2}$. These equations were derived by integrating the square of the MOSFET currents (each being the combination of the inductor and transformer currents) over one switching cycle.

$$I_{rms\_Q1} = \sqrt{\frac{T_{sw}}{2T_{res1}} \left(\frac{\pi n V_{out}}{2R_{load}} \right)^2 - \frac{2ni_{L,avg}V_{out}}{R_{load}} + {i_{L,avg}}^2 (1-D)} \tag{2.26}$$

$$I_{rms\_Q2} = \sqrt{\frac{T_{sw}}{2T_{res2}}\left(\frac{\pi n V_{out}}{2R_{load}}\right)^2 + \frac{2ni_{L,avg}V_{out}}{R_{load}} + {i_{L,avg}}^2 D} \tag{2.27}$$

Because Q_1 obtains ZVS naturally, it's switching loss is limited to only turn-off loss. Q_2, however, has both turn-on and turn-off loss. Of note here is that because modes 1 and 3, with lengths of T_{res1} and T_{res2}, are complete by the time that either Q_1 or Q_2 switches off, the current-related switching losses are only due to the input inductor current. The loss equations, (2.28) and (2.29), are modified triangle approximations with time values representing the rise and fall of the device voltage and current, and ΔI_L representing the inductor current ripple [42]. Also incorporated is the charge-related switching loss. Diode reverse recovery loss is not included in the loss equation (2.29), but could be significant in some applications.

$$P_{SW,Q1} = \frac{(t_{FI} + t_{RV})}{2T_{sw}} V_{bus}\left(I_{L,avg} - \frac{\Delta I_L}{2}\right) \tag{2.28}$$

$$P_{SW,Q2} = \frac{(t_{RI} + t_{FV})}{2T_{sw}} V_{bus}\left(I_{L,avg} - \frac{\Delta I_L}{2}\right) + \frac{(t_{FI} + t_{RV})}{2T_{sw}} V_{bus}\left(I_{L,avg} + \frac{\Delta I_L}{2}\right) + \frac{1}{T_{sw}} Q_{oss,Q2} V_{bus} \tag{2.29}$$

Because the output rectifier is a voltage-doubler, each output diode must carry the full output current on average (2.30). The upper diode current is a piecewise combination of a half-sine wave during the resonant period and zero elsewhere. From an integral definition of the average current (2.31), the peak current through the upper diode D1 can be written as (2.32). From a similar approach, the peak current in D_2 can be

written as (2.33).

$$I_{D1,avg} = \frac{P_{out}}{V_{out}} \tag{2.30}$$

$$\frac{P_{out}}{V_{out}} = \frac{1}{T_{sw}} \int_0^{T_{res1}} I_{D1,pk} \sin\left(\frac{\pi}{T_{res1}} t\right) dt \tag{2.31}$$

$$I_{D1,pk} = \frac{\pi P_{out} T_{sw}}{2 V_{out} T_{res1}} \tag{2.32}$$

$$I_{D2,pk} = \frac{\pi P_{out} T_{sw}}{2 V_{out} T_{res2}} \tag{2.33}$$

Similarly, the rms current through D_1 can be written from the definition (2.34), which simplifies to (2.35). Similarly, the rms current through D_1 is given in (2.36).

$$I_{D1,RMS} = \sqrt{\frac{1}{T_{sw}} \int_0^{T_{res1}} {I_{D1,pk}}^2 \sin^2\left(\frac{\pi}{T_{res1}} t\right) dt} \tag{2.34}$$

$$I_{D1,RMS} = \frac{\pi}{2\sqrt{2}} \frac{P_{out}}{V_{out}} \sqrt{\frac{T_{sw}}{T_{res1}}} \tag{2.35}$$

$$I_{D2,RMS} = \frac{\pi}{2\sqrt{2}} \frac{P_{out}}{V_{out}} \sqrt{\frac{T_{sw}}{T_{res2}}} \tag{2.36}$$

8. *Loss Analysis*

Utilizing the equations defined above in conjunction with the characteristics of the experimental circuit defined in the proceeding section (Tables I, II, III, and IV), a loss analysis graph is provided in Fig. 2.10 showing the system loss at a nominal input of 30V and at a full load capacity of 250W. In the circuit, the principle losses belong to

Q_2 and the output diodes.

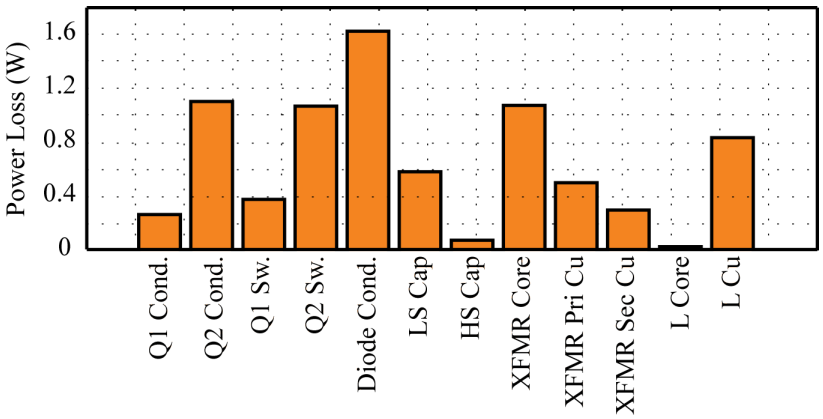

Figure 2.10: Circuit loss analysis at 30V input, 250W output (full load)

2.3 A Note on Control

Quite obviously, the goal of the dc-dc micro-converter is to maximize the PV panel's output power while simultaneously providing a dc voltage compatible with the dc-ac centralized inverter. However, only one control variable is available to accomplish these tasks, the duty cycle D. How to select the correct duty cycle in a given operating condition is certainly a matter for debate. The voltage boost function is a direct product of the transformer turns ratio, and the responsibility of dc-link regulation may be passed on to the inverter. This leaves the dc-dc to primarily focus on optimization. Early methods of MPPT revolved around the perturbation of the duty cycle and the monitoring of the corresponding change in operating point (and thus, output power) [43]–[46]. This process has many variants and is described in much detail in literature. While the IBR is certainly compatible with these direct duty

control methods, they come a few concerns. The dynamic response and stability margins for these systems are largely unmodeled, as well as their handling of external disturbances. One alternative to directly controlling the duty cycle is to set up closed-loop control for one of the input variables, voltage [47] or current [48], and perturbing the variable's reference rather than the control parameter.

This allows for straightforward modeling processes [42], known dynamics, and disturbance rejection (covered in Chapter 5). Because high-bandwidth voltage sensing is typically easier to implement with lower cost and higher accuracy than the corresponding current sensor, input voltage control was selected as an appropriate method for the IBR. A basic block diagram [49], [50] for the control structure is shown in Fig. 2.11. From here, the MPPT algorithm can be selected from many different options without needing to alter the internal loop. The internal loop functions by comparing the actual input voltage with the desired reference (from the MPPT controller), and creating an error signal for the compensator. Because an increase in the duty cycle results in a decrease in the input voltage (resulting in a negative plant gain), either a negative sign must be included in the compensator, or the polarity of the summation block must be reversed.

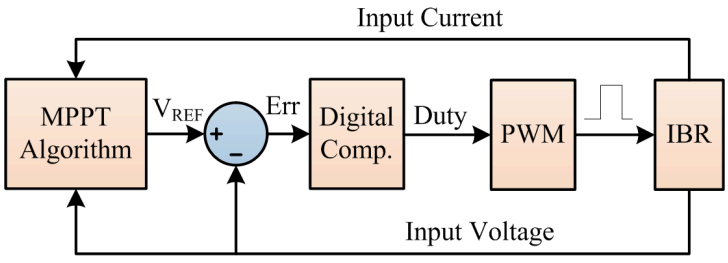

Figure 2.11: Closed-loop control block diagram

2.4 Experimental Results

During the course of this development, a 250W prototype converter was designed and built in order to validate the presented analysis and to serve as a core element in a new distributed PV generation system. Some specifications for the circuit are listed in Tables 2.2 and 2.3, while the semiconductor device content is summarized in Table 2.4. Table 2.5 includes the switching data for Q_1 and Q_2 used in the calculations loss analysis above. The magnetic components (the input inductor and transformer) are each comprised of two PQ32/20 cores either in series (for the inductor) or series-parallel (for the transformer). The inductors were wound with 0.014 thick copper foil to better utilize the core window area. The transformers were wound with 20AWG equivalent Litz wire to improve the ac resistance of the windings. The system control was implemented digitally on a Texas Instruments TMS320F28026 microcontroller simply for flexibility and rapid implementation. Control of the MOSFET gates passed directly from the PWM module on the MCU directly to a Fairchild FAN7390 gate driver IC. In practice, a dedicated PWM or MPPT controller would also function well. A photograph of the prototype is provided in Fig. 2.12. Fig. 2.13

Table 2.2: Power Stage Element Values for 250W Prototype

Element	**Value**	**Resistance**	I_{rms} **at 250W**
L	100μH	11mΩ	8.6A
C_1, C_2	10μF	4mΩ	11.46A, 6.64A
C_3, C_4	100nF	50mΩ	0.89A
n_{pri}	7 turns	3.5mΩ	12.84A
n_{sec}	46 turns	46mΩ	1.74A
Q_1	N/A	4.9mΩ	6.64A
Q_2	N/A	4.9mΩ	13.95A
D_1, D_2	1.3V	N/A	0.625A

Table 2.3: Power Stage Design Parameters for 250W Prototype

Element	Value	Element	Value
T_{res1}	4.61μs	$V_{in,\min}$	20V
T_{res2}	4.03μs	$V_{in,\max}$	40V
T_{sw}	14.3μs	V_{out}	400V
F_{sw}	70kHz	V_{bus}	60V
$D_{\min}$	0.33	P_{out}	250W
$D_{\max}$	0.67		

Table 2.4: Semiconductor Data for 250W Prototype

Element	Value
Q_1, Q_2	Infineon IPB049NE7N3
D_1, D_2	Vishay HFA04SD60

Table 2.5: Switching Loss Calculation Data

Element	Value	Element	Value
t_{RV}	12.7ns	t_{FI}	8ns
t_{FV}	15.7ns	t_{RI}	11ns
Q_{oss}	71nC		

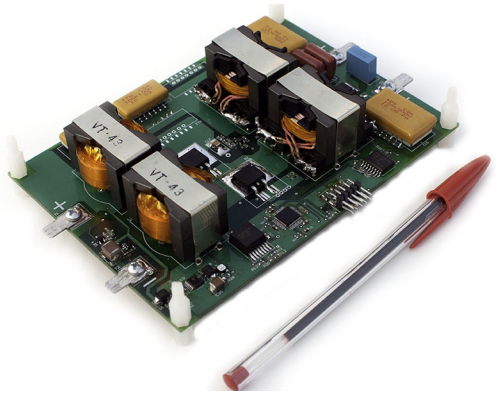

Figure 2.12: The 250W experimental prototype

and Fig. 2.14 demonstrate the consistency of the converter operation over both high and low power. Under each condition, both the inductor current and the transformer current retain

their general wave-shape while demonstrating CCM and resonant behavior, respectively. This consistency and simplicity is further demonstrated by the voltage transfer ratio plot in Fig. 2.15, which shows the relationship of the voltage transfer ratio given in (1), as compared to experimental measurement at low and high power. As anticipated, the magnitude of the voltage transfer ratio varies only slightly with power level as a result of increased converter loss. In order for the converter to achieve high efficiency, two other critical components were mentioned, mitigating switching loss and improving transformer power factor. One definitive aspect of managing the converter switching loss is the ability of the output diodes to achieve ZCS. Experimental evidence of this is provided in Fig. 2.16, even at high power (> 225W). Also, the fully resonant behavior at the transformer allows the converter to achieve a high power factor, as evidenced in Fig. 2.17. Here it is shown that the transformer current is continually in-phase with the transformer voltage, indicating very low circulating energy.

Utilizing the TI microcontroller, a simple PV voltage control loop with perturb-and-observe (P & O) MPPT logic was implemented, similar to [38]. At startup, the converter starts at the open-circuit voltage of the PV panel and attempts to locate the MPP by changing the input voltage reference and measuring the corresponding change in input power. An experimental waveform showing the proposed Integrated Boost Resonant (IBR) converter operation during startup (via connecting the converter to the PV panel), MPPT operation, as well as shutdown (via forcibly disconnecting the PV panel from the input) is shown in Fig. 2.18. For the test recorded in the figure, a BP Solar SX6165N polycrystalline SiN PV panel was used as the input source, which has characteristics recorded in Table 2.6.

As the final step in the verification process, an experiment to demonstrate the efficiency of the proposed converter was conducted. Projections for the converter efficiency, based on the procedure outlined in section 2.2, are given in Fig. 2.19. Shown in Fig. 2.20 is the measured power stage efficiency, which includes all loss elements aside from controller and gate drive losses, for a range of input and load conditions. Power measurements were taken using four Fluke Model 287 digital multimeters which have a dc voltage accuracy of 0.025% and a dc current accuracy of 0.06%. The experimental and theoretical results match well overall, with some discrepancies at full power due to unmodeled circuit parasitics. Another issue is the variation in the device switching times under different current conditions, causing a low estimate of the efficiency at the low-voltage conditions. However, the converter achieves a CEC efficiency of 96.8% and an overall peak efficiency of 97.4%.

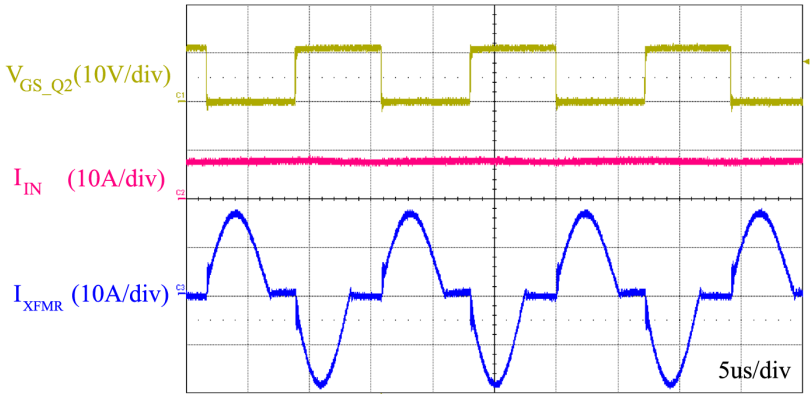

Figure 2.13: Key converter operational waveforms at 30Vdc input and 225W / 400Vdc output

Table 2.6: BP Solar SX6165N PV Panel Ratings

Element	Value	Element	Value
V_{oc}	44.2V	I_{mpp}	4.69A
I_{sc}	5.1A	$NOCT$	47°C
V_{mpp}	35.2V		

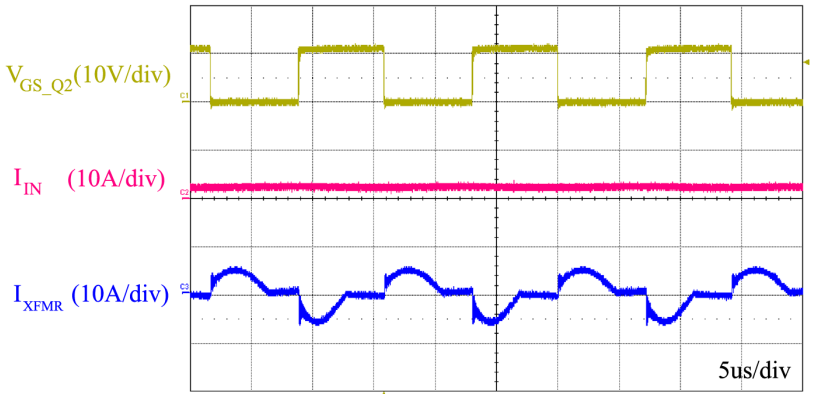

Figure 2.14: Key converter operational waveforms at 30Vdc input and 67W / 400Vdc output

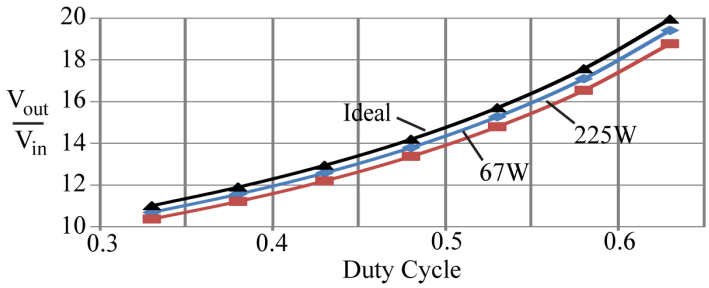

Figure 2.15: Experimental voltage transfer ratio vs. duty cycle

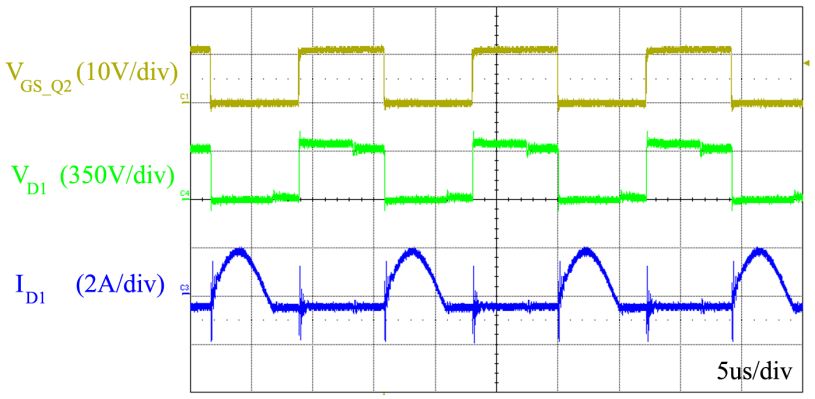

Figure 2.16: Output diode ZCS

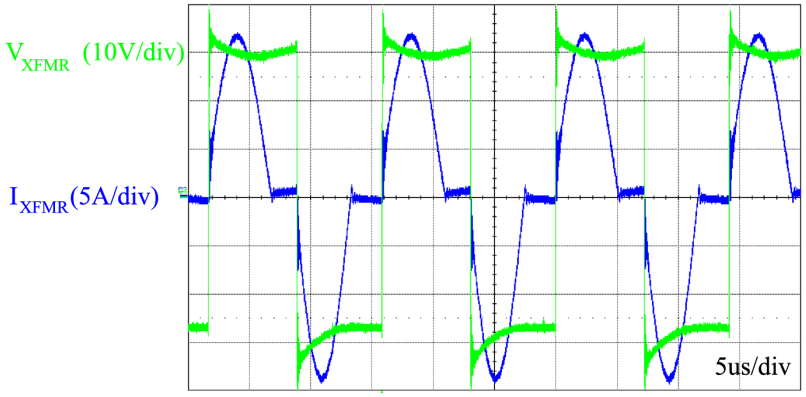

Figure 2.17: Transformer V-I relationship (30Vdc input and 400Vdc/225W output)

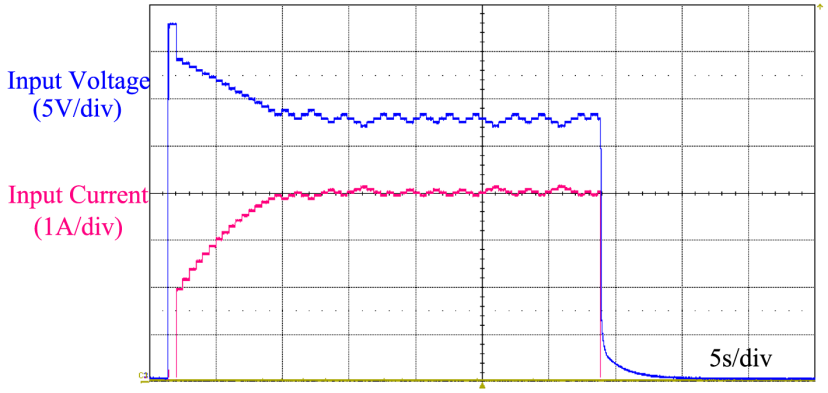

Figure 2.18: Input voltage and current during startup, P & O MPPT, and shutdown using a BP Solar SX6165N 165W PV panel (112W operating power) (400Vdc output)

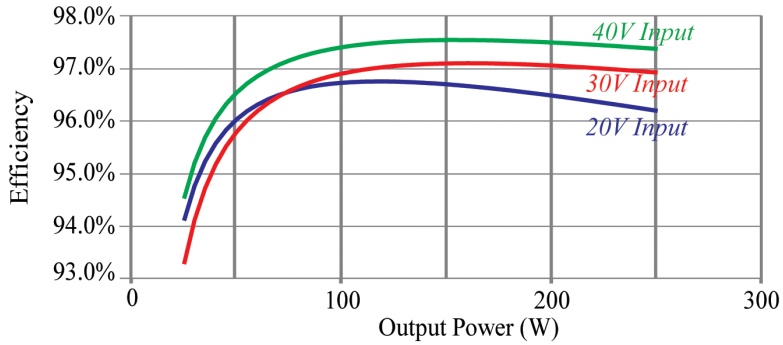

Figure 2.19: Projected power stage efficiency (400Vdc output)

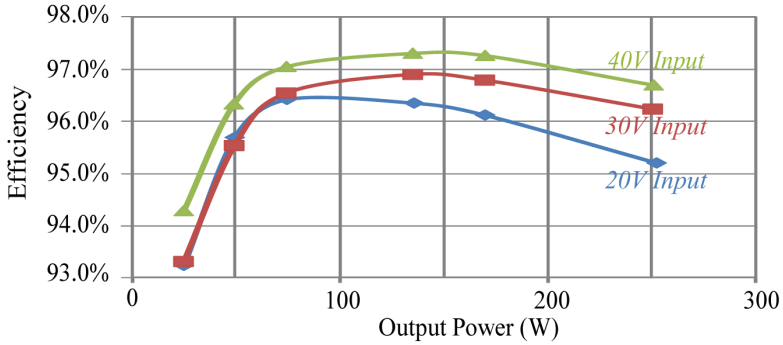

Figure 2.20: Measured power stage experimental efficiency (400Vdc output)

2.5 Summary

As a solution for providing efficient, distributed PV conversion, an isolated boost resonant converter has been proposed. The system is a hybrid between a traditional CCM boost converter and a series resonant half-bridge, employing only two active switches. The synthesis of the converter was described along with the circuit operating modes and key waveforms. The design process was then defined, with a focus on the unique combined resonant and PWM behavior. The result was a simple process, requiring only consideration

of the resonant period length in selecting a valid converter duty cycle range. Also provided was a detailed theoretical loss analysis, along with formulas for calculating the rms values of important waveforms. Finally, the loss and theoretical analysis were verified by the design, construction, and testing of a 250W experimental prototype. The principle advantages of utilizing this topology were as follows:

1. High weighted efficiency because of low circulating energy and reduced switching loss with resonant energy transfer and output diode ZCS.

2. Low potential cost due to minimal number of active devices and a small overall component count.

3. Galvanic isolation allows for the use of high efficiency inverter stages without additional concern over ground leakage current.

4. Reduced control complexity provides lower auxiliary power loss and simpler controller IC configurations.

Chapter 3

Hybrid-Frequency Modulation

In the introduction to the previous chapter, the motivation, procedures, and implications of CEC efficiency were introduced. Though the IBR topology fulfills many of the requirements for the micro-converter based system architecture, two issues stand out specifically when examining the performance of the converter:

- The operating range of the converter is inversely proportional to the nominal efficiency
- The nominal efficiency is typically less than the efficiency at the high-voltage input

In many cases, extending the input range of a converter requires sacrificing conversion efficiency [51], or else adding a significant number of additional components [31], [52], [53]. With additional emphasis placed on "weighted" converter efficiency [13], [14] and cost, especially in photovoltaic (PV) applications, efficient, low-cost enhancements to improve converter efficiency are desirable. One such method of enhancing converter operation is the selection of

an appropriate modulation scheme. Basic examples of modulation schemes are well known in literature, such as traditional pulse-width modulation (PWM) or phase-shift-control, and have an inherently fixed switching frequency. Other traditional methods have an inherently variable switching frequency [54], [55], such as constant-on [56], constant-off [57], or hysteretic control [58], [59]. In these methods, either a portion of the switching interval or bounds on a control variable are kept constant, while the switching frequency is allowed to vary. Other more recent adaptations have involved hybrid switching schemes such as PWM plus Phase Shift (PPS) [60]. Also in literature are hybrid modulation schemes of constant-frequency and constant-off [61] as well as constant-on and constant-off [62]. In this chapter, a unique dc-dc converter modulation scheme is proposed for a class of converters that integrate pulse-width-modulation (PWM) stages into unregulated resonant converters. The resonant stage provides galvanic isolation with high efficiency, while the PWM stage provides the necessary regulation. Though the efficiency is good with a narrow input range and fixed frequency PWM, it is still possible to extend the operating range while maintaining high efficiency. This new method, a hybrid between constant-on, constant-off, and fixed-frequency modulation, optimizes the converter efficiency at the nominal line input while allowing an extended input range. Though both this method and the one in [62] share the same root elements, the base concept, application, and implementation differ significantly. In support of this new modulation method, a detailed justification is provided based on converter operation and desired characteristics. A detailed theoretical loss analysis and comparison with traditional fixed-frequency PWM is also presented. Information on implementation with a digital con-

trol system is provided along with experimental verification with an 180-W prototype dc-dc converter.

3.1 Proposed Modulation Scheme

The proposed modulation scheme is developed primarily for circuits that employ this integration of PWM and resonant conversion, such as the IBR converter. The operating modes for the IBR converter are re-printed in Fig. 3.1 (a)-(d), corresponding to the theoretical waveforms shown in Fig. 3.2. Because Q_1 and Q_2 are both MOSFETs, and are switched complementary to one another, the input inductor L operates in the continuous conduction mode (CCM) and never becomes discontinuous. The inductor current increases linearly during modes 3 and 4, and decreases linearly during modes 1 and 2. The energy transfer between the combinations of C_1, C_2 and C_3, C_4 is resonant, occurring only during modes 1 and 3. Though the boost converter is integrated into the resonant circuit, the two elements are effectively decoupled as long as the resonant modes are allowed to fully complete. Thus the resulting voltage gain is simply the product of a boost converter voltage gain and the gain of the resonant stage. Since the boost converter always operates under CCM, its gain is affected only by the duty cycle of Q_2. Secondly, because the resonant modes are allowed to fully complete and the transformer magnetizing current is negligible, the average secondary current is equal to the average of the primary-side current. The resonant stage gain is therefore equal to the turns ratio, n, and is independent of duty cycle, switching

frequency, and power level. However, because the resonant action must be allowed to complete during each half-cycle, the maximum and minimum duty ratio for Q_2 under traditional PWM control are limited by the length of each resonant period, as shown in (2.4) and (2.5). The lengths of each resonant period (T_{res1} and T_{res2}) were provided in (2.2) and (2.3). In order to accommodate a larger duty cycle range, the resonant period length must be reduced with respect to the overall switching period. With a reduced resonant period, and less of the conduction period utilized, the peak amplitude of the resonant current must increase in order to transfer the same amount of power to the output. This results in an increase in the rms current through all of the devices involved in the resonant operation, and thus an increase in overall conduction loss. Therefore, having the resonant periods equal to the switch on and off-times would result in the lowest rms current. The waveforms in Fig 3.2(a)

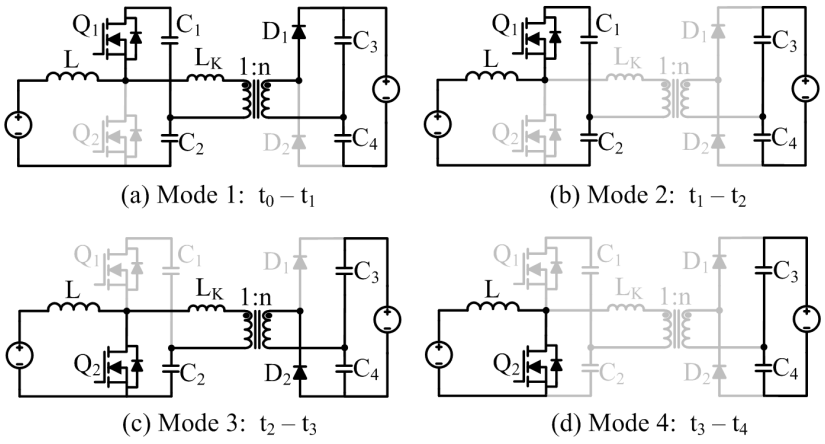

Figure 3.1: Operating modes of the IBR converter

show the resonant operation of the IBR converter operating at 50% duty cycle with an optimized switching frequency. Under this condition, the resonant action occupies the majority of the switching period, and the peak currents are reduced. Alternatively, Fig. 3.2(b) shows

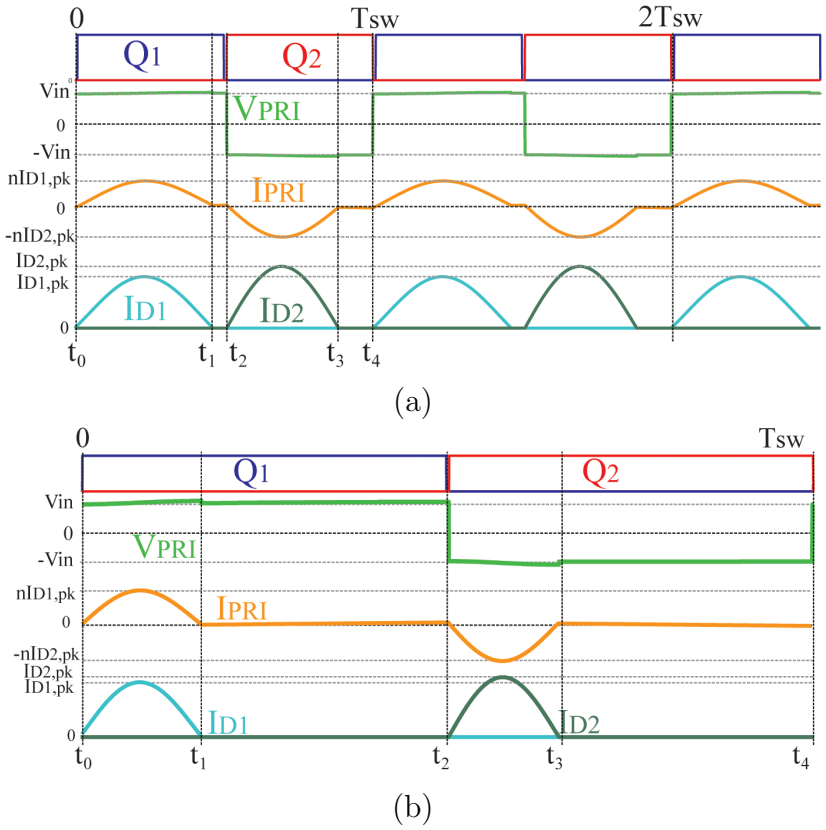

Figure 3.2: Theoretical IBR operation at 50% duty with (a) optimized switching frequency and (b) fixed-frequency (4:1 input ratio)

the converter operating under the fixed-frequency condition with a wide-input range. The resonant action occupies very little of the switching period, and the peak currents increase by 150% of their optimized value. Another issue with fixed-frequency operation in the IBR converter is the management of the core loss in the transformer. In order to accommodate a wide duty cycle range, the switching frequency must be reduced much below optimum, which increases the applied volt-seconds, and therefore the ac flux density, at the transformer. Because the applied volt-second product is increased at 50% duty cycle, the ac flux density is also increased at the middle of the input voltage range. For a fixed switching frequency, the peak in ac flux density would coincide with a peak in the transformer core loss. In order

to overcome the drawbacks to traditional PWM, other modulation methods have been proposed, three of the most popular being constant-on, constant-off, and hysteretic control. For the IBR, constant-on modulation (demonstrated in Fig. 3.3) provides a selectable minimum on-time that can ensure ZCS during at least one-half cycle. There is no controllable off-time, however, therefore ZCS is only guaranteed for the output diode for duty cycles greater than 50%. Also, constant-on control requires an extremely wide frequency range, with the maximum frequency occurring only at the minimum input voltage. Similarly, constant-off control (demonstrated in Fig. 3.4) provides only a selectable off-time, guaranteed ZCS for only duty cycles less than 50%, with the maximum frequency occurring at the maximum input voltage. With hysteretic control, there is no minimum on or off-time and no guarantee of ZCS. In order to improve the utilization and efficiency of the IBR converter under a

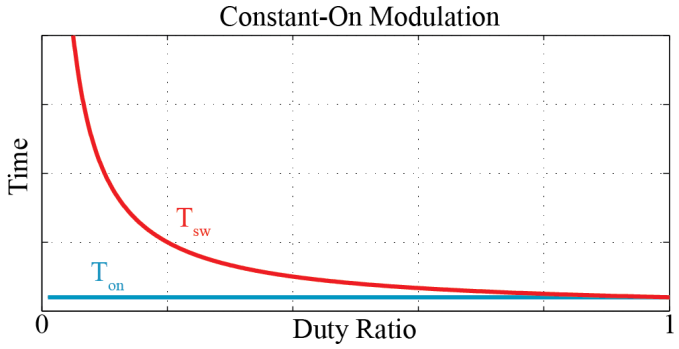

Figure 3.3: Example of constant-on modulation.

wide load range, the designed modulation scheme needs to have a selectable minimum on- and off-time, guaranteed ZCS across the operating range, narrow operating frequency band, and maximum frequency occurring at 50% duty cycle so as to minimize the transformer core loss. The modulation scheme would also need to be compatible with traditional PWM

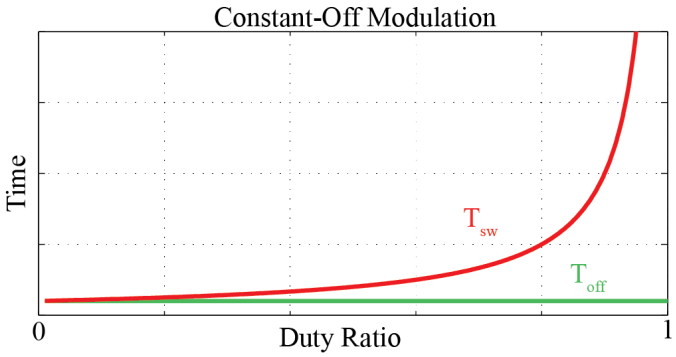

Figure 3.4: Example of constant-off modulation.

techniques, so that traditional voltage and/or current control could be utilized. Fig. 3.5 shows the control loop block diagram from the previous chapter with the hybrid-frequency modulator inserted. The normal output of the digital compensator is the only required input to the hybrid-frequency modulator, and the output works naturally with a PWM comparator that requires both a switching period length and a value for the main switch on-time. The desired effects can be achieved through a hybrid of fixed-frequency, constant on-, and

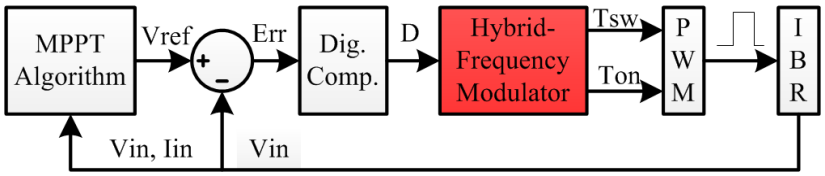

Figure 3.5: Example control system block diagram (MPPT dc-dc converter).

constant off-time control as shown in Fig. 3.6. For an operating range between $D_{\min}$ and $D_{\max}$, the converter operates in constant on-time control for duty ratios less than 50%, and constant off-time control for duty ratios greater than 50%. This ensures that across the designed operating range, neither the on or the off time will decrease below a specified minimum. The total switching period, defined as the sum of the on and off times, reaches a

minimum at 50% duty cycle, reducing the ac flux density in the transformer. For duty ratios outside the desired operating range, the converter operates in fixed-frequency. This prevents potential saturation of the magnetic components, as well as undesirable acoustic noise. The

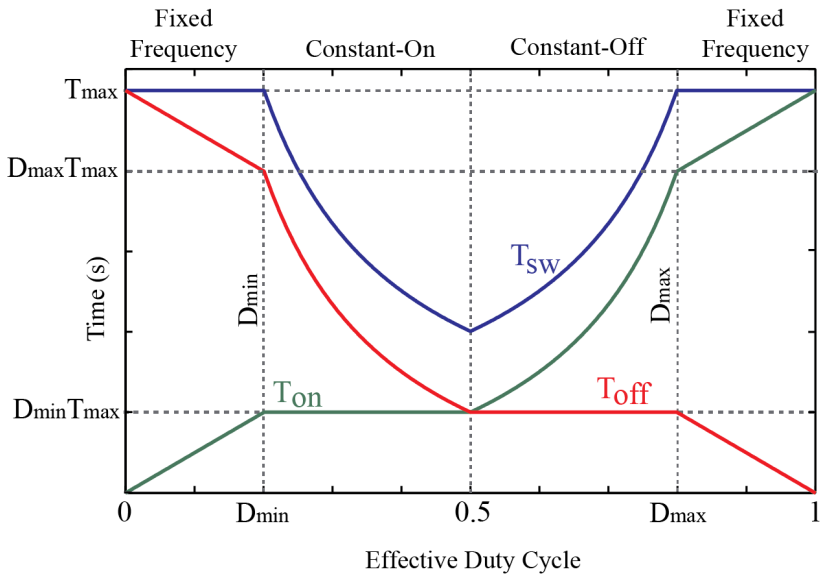

Figure 3.6: Switching period analysis under proposed modulation.

governing equations for this modulation method are straightforward, and provided for the fixed frequency (3.1)-(3.3), constant-on (3.4)-(3.6), and constant-off (3.7)-(3.9) regions.

$$\text{Fixed-Frequency, } D \in [0, D_{\min}] \cup [D_{\max}, 1]$$

$$T_{sw} = T_{\max} \tag{3.1}$$

$$T_{on} = D \cdot T_{\max} \tag{3.2}$$

$$T_{off} = (1 - D) T_{\max} \tag{3.3}$$

$$\text{Constant-On, } D \in [D_{\min}, 0.5]$$

$$T_{sw} = \frac{T_{\max} D_{\min}}{D} \tag{3.4}$$

$$T_{on} = D_{\min} T_{\max} \tag{3.5}$$

$$T_{off} = T_{\max} D_{\min} \left(\frac{1 - D}{D} \right) \tag{3.6}$$

Constant-Off, $D \in [0.5, D_{\max}]$

$$T_{sw} = \frac{T_{\max} D_{\min}}{(1 - D)} \tag{3.7}$$

$$T_{on} = T_{\max} D_{\min} \left(\frac{D}{1 - D} \right) \tag{3.8}$$

$$T_{off} = T_{\max} D_{\min} \tag{3.9}$$

Unlike many other variable frequency modulation techniques, once the required on-time and the maximum switching period are determined, each individual duty ratio corresponds to one switching period and on-time combination. This provides the circuit designer with a great deal of flexibility with implementation, especially when utilizing a modern microcontroller (MCU) or digital signal processor (DSP) for control. Three options for implementation:

1. Calculate the on-time and period during each switching cycle

    - Allows for minimum storage requirements
    - Duty cycle precision only restricted by numeric capability and PWM resolution
    - Requires a division operator (Not practical on a low-power DSP)

2. Calculate the required period for each duty cycle and populate a table of the required switching periods.

    - Allows for a small storage requirement (2KB for 0.1% resolution)
    - Requires only add, subtract, or multiply during each switching cycle

3. Complete Off-line Computation

    - Populate a 2-D table of switching periods and on-times at converter startup
    - Additional storage requirement (4KB RAM for 0.1%)
    - Requires only array lookup at run-time

For either of the tabular methods, an integer equivalent of the desired duty ratio serves as the array index for the lookup table. Either of the latter two methods are generally practical for most low-power MCUs, depending on the speed and general complexity required of the rest of the control loop. Fig. 3.7 is an example flow chart for populating the lookup table in an off-line setting.

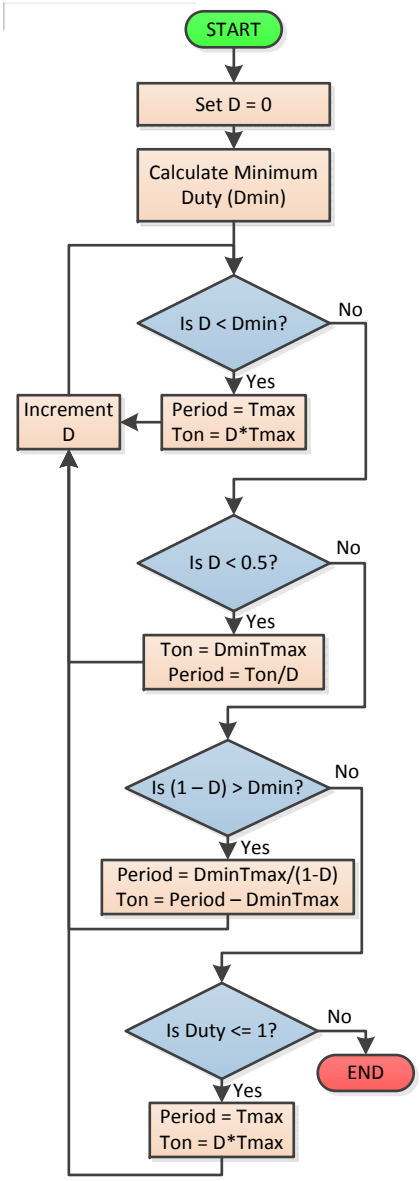

Figure 3.7: Hybrid-frequency flow chart for off-line array population

3.2 Analysis and Theoretical Results

In order to support the proceeding theoretical analysis, specifications for a 180-W IBR converter are provided in Table 3.1, component values in Table 3.2, and semiconductor data in Table 3.3. With these key characteristics determined, it is possible to estimate the

Table 3.1: Power Stage Design Parameters for 180-W Prototype

Element	**Value**	**Element**	**Value**
T_{res1}	6.23μs	V_{in}	12-48V
T_{res2}	5.41μs	$T_{\max}$	33.33μs
T_{min}	13.33μs	V_{out}	400V
$D_{\min} - D_{\max}$	0.2-0.8	P_{out}	180W

Table 3.2: Power Stage Element Values for 180-W Prototype

Element	**Value**	**Resistance**
L	100μH	11mΩ
C_1, C_2	20μF	4mΩ
C_3, C_4	200nF	43mΩ
L_K	300nH	N/A
n_{pri}	7 turns	3.5mΩ
n_{sec}	46 turns	46mΩ
Q_1, Q_2	N/A	4.9mΩ
D_1, D_2	1.3V	N/A

Table 3.3: Semiconductor Data for 180-W Prototype

Element	**Value**
Q_1, Q_2	Infineon IPB049NE7N3
D_1, D_2	Vishay HFA04SD60

impact of the hybrid-frequency modulation with respect to traditional PWM. Though many loss factors are impacted by the change in modulation technique, some deterministic ones are defined and explained in the proceeding section. One of the most significant loss factors impacted by the modulation change is the transformer core loss. This value is determined by the ac flux density, which itself is a product of the applied volt-seconds, and is given in (3.10) [63].

$$B_{ac} = \frac{V_{in}\left(\frac{V_{out}}{n_sec} - \frac{V_{in}}{n_pri}\right) \cdot 10^4}{2T_{sw}A_cV_{out}}, \text{ [T]} \tag{3.10}$$

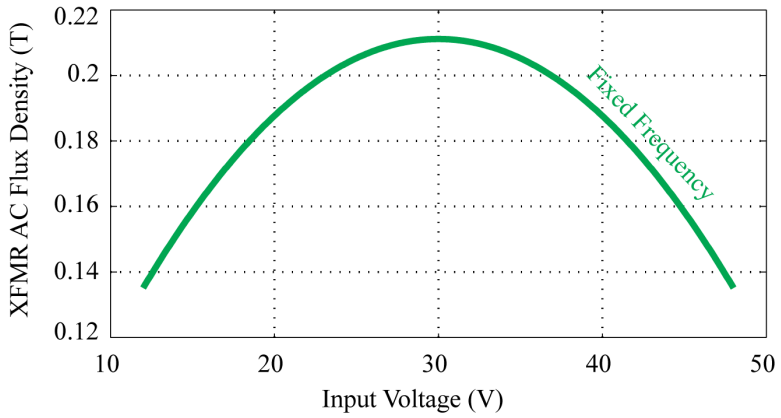

Figure 3.8: Transformer ac flux density under fixed-frequency operation.

Note that A_c is the core area in cm^2, while n_{pri} and n_{sec} are the number of primary and secondary turns. The resulting plot of (3.10) for the analyzed converter under fixed frequency is shown in Fig. 3.8. Under normal operation V_{out} is held constant as V_{in} is allowed to vary. With the ac flux determined at a given operating point, it is possible to determine the core loss from (3.11) , where f_{sw} is the switching frequency and V_{core} is the core volume. The exact magnitude of the coefficients k, c, and d vary based on material type and desired units. Example data for Magnetics, Inc. P-Material is provided in Table 3.4 [63]. This implies that increasing the operating frequency in order to reduce the ac flux density results in a net decrease in core loss. This is also demonstrated in the estimated core loss comparison provided in Fig. 3.9. As shown in the figure, using the proposed algorithm reduces the core loss at nominal input by more than 70

$$P_{core} = V_{core} k {f_{sw}}^{c} {B_{ac}}^{d} \tag{3.11}$$

Another significant impact of the proposed hybrid-frequency algorithm is the reduction of

Table 3.4: Magnetics Inc. P-Material Properties 30°C

Element	**Value**
Material	P
Temperature	30°C
Volume	$2 \times 9.44\text{cm}^3$
k	2.86×10^{-5} W/cm^3
c	1.36
d	2.86

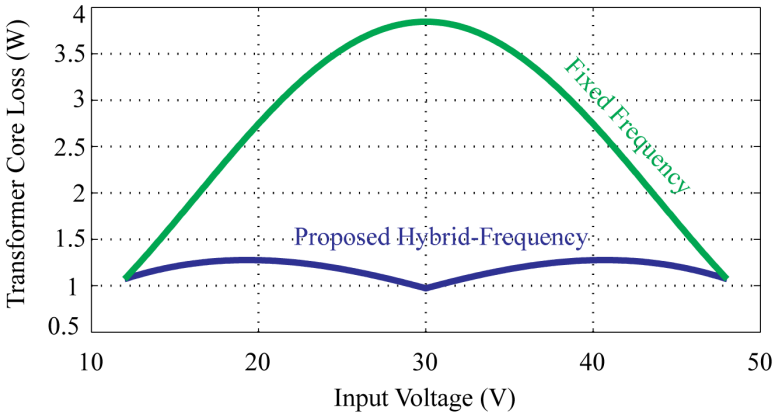

Figure 3.9: Theoretical core loss comparison (180W).

overall conduction loss by improving the utilization of the switching period by the resonant circuit. Because all of the rms values of the device currents depend strongly on the peak magnitude of the resonant current, the defining equations all contain a dependency on the ratio of the resonant period and the total switching period. Some examples are the output diode currents (2.35) and (2.36), the upper high-side capacitor current (2.22), the transformer primary current (2.14), the upper low-side capacitor (C_1) current (2.20). Each of these equations can be derived by integrating the square of the current and taking the square-root, as given by the rms definition. Also modeled, but not shown are the MOSFET currents, the

other resonant capacitor currents, the output diode currents, and the input inductor current. Note that the inductor and diode currents do not show a strong dependency on frequency, as their losses are dominated by average rather than rms current values. The conduction loss at full load as a function of input voltage is given in Fig. 3.10. Because the output rectifier is a voltage-doubler, each output diode must carry the full output current on average (2.30). The secondary-side capacitors (C_3 and C_4) each carry one-half of the diode current during each resonant period and zero current elsewhere, as reflected in the rms current definition given in (2.22). The transformer identically carries the sum of the currents in C_3 and C_4 on the secondary side, with the primary-side magnitude increased by the transformer turns ratio (2.14). The capacitors on the primary-side each carry a combination of the triangular inductor current and the resonant current during portions of the cycle, shown in (2.20).

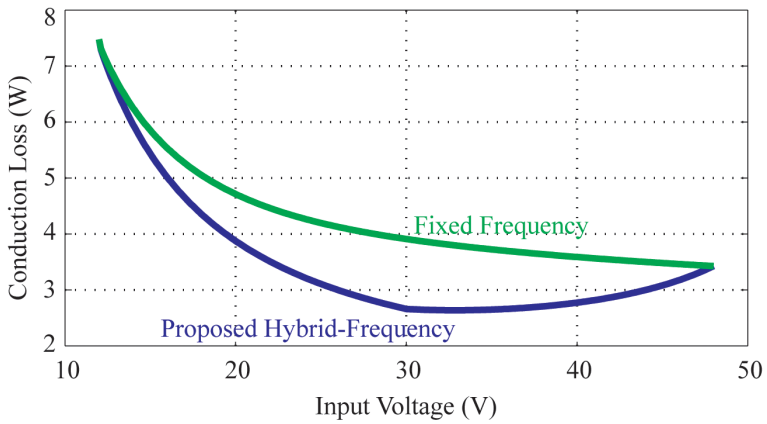

Figure 3.10: Theoretical total conduction loss comparison (180W).

However, applying hybrid-frequency control does not improve every converter loss factor. There is a definite trade-off between core and conduction loss, with switching and other frequency dependent losses, such as diode capacitance loss. The upper and lower

MOSFET switching losses can be calculated by a method such as (2.28) and (2.29) [42]. Note that because the upper MOSFET (Q_1) achieves ZVS through the natural free-wheeling of the inductor current, it has less than half of the switching loss of lower MOSFET Q_2. A plot of total MOSFET switching loss versus input voltage at full power is provided in Fig. 3.11. Note that even though the relative increase in switching loss is significant, the total additional loss is much less than the amount of power saved from either the core or conduction losses.

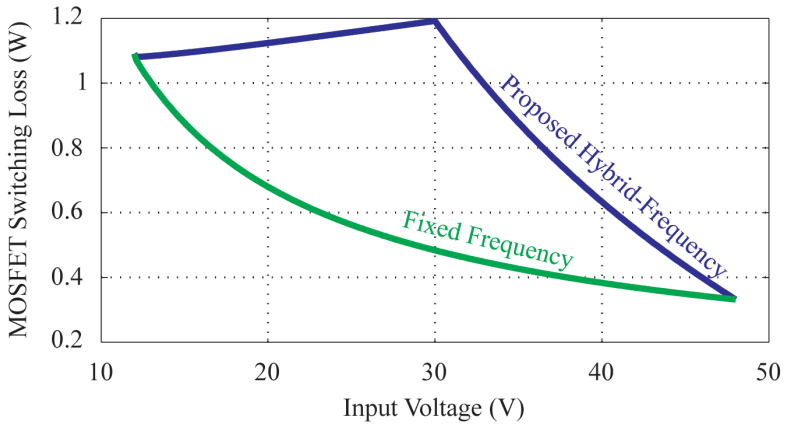

Figure 3.11: Theoretical switching loss (Q_1 + Q_2) comparison (180W).

With some of the key loss elements broken down, the overall converter loss at full load is shown in Fig. 3.12, while the converter efficiency at full load is shown in Fig. 3.13. From Fig. 3.12 the strong influence of both the conduction loss at low voltage input, as well as the impact of core loss around the nominal input, may be observed. A theoretical loss breakdown is provided in Fig. 3.14.

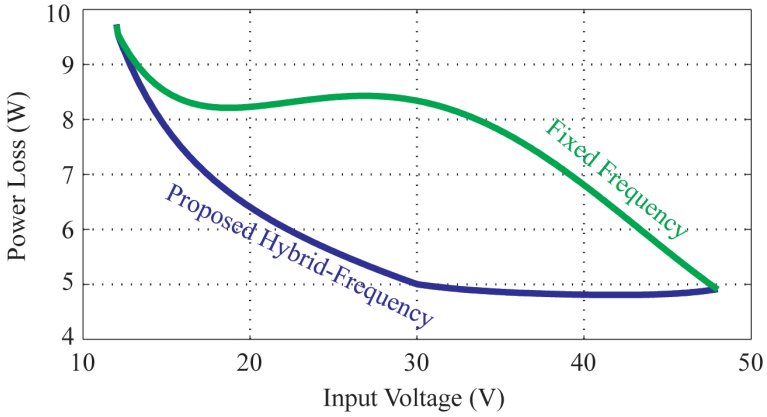

Figure 3.12: Theoretical power loss comparison (180W).

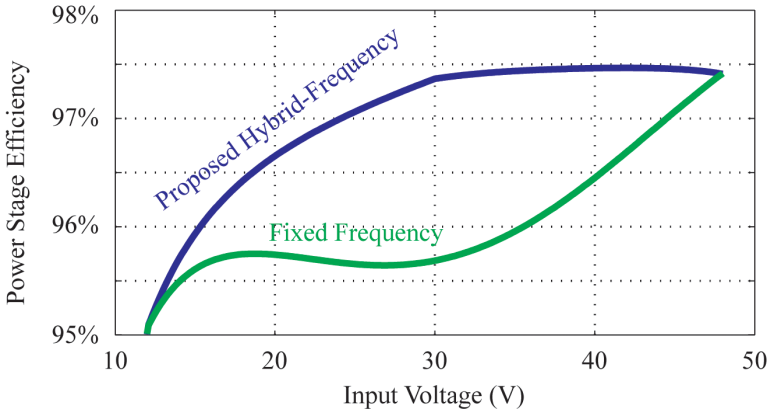

Figure 3.13: Theoretical power stage efficiency comparison (180W).

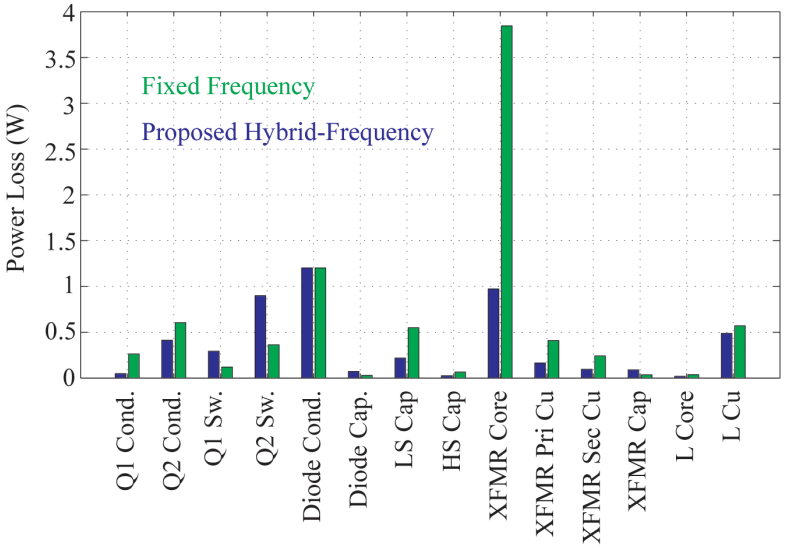

Figure 3.14: Theoretical loss breakdown (30V - 180W).

3.3 Experimental Results

In order to verify the proposed modulation method, the algorithm was programmed into a prototype IBR converter with specifications as given in the preceding sections. The algorithm was implemented on a Texas Instruments (TI) TMS320F28026 MCU using a full switching period and on-time lookup table. Experimental waveforms from the 30V input condition are shown for both the proposed control method, Fig. 3.15, and the traditional fixed-frequency method in Fig. 3.16. Experimental waveforms capture for fixed-frequency and hybrid frequency are also shown at the 20V input (Fig. 3.17 and Fig. 3.18), as well as 40V input (Fig. 3.19 and Fig. 3.20). At the nominal input (30V input), the improvement of the hybrid-frequency modulation is most pronounced. However, at the other operating conditions (20V and 40V input), the converter performance is still improved. These waveforms match well with the expected behavior from the modulation technique development. In an attempt to both prove the usefulness of the proposed modulation method and verify the analysis from the prior section, efficiency tests at full output power and various input voltage levels were conducted. The measured power loss is provided in Fig. 3.21, and the measured power stage efficiency is provided in Fig. 3.22. Both Figs. 3.21 and 3.22 show the influence of the high conduction loss at 12V, as well as the strong impact of core loss around 30V input. Overall, the results match well with the preceding analysis, except for some deviation around 12V and 48V input, where the measured loss exceeds the estimate. As the input current at 12V is quite high, or the applied volt-seconds at the transformer in the case of 48V input, these errors are likely due to an aggravated parasitic condition.

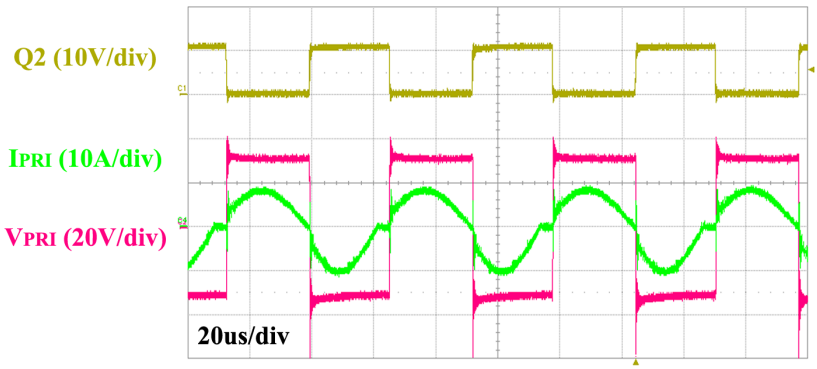

Figure 3.15: Experimental waveforms with hybrid-frequency modulation under 30V input, 400V output, and 180W load conditions.

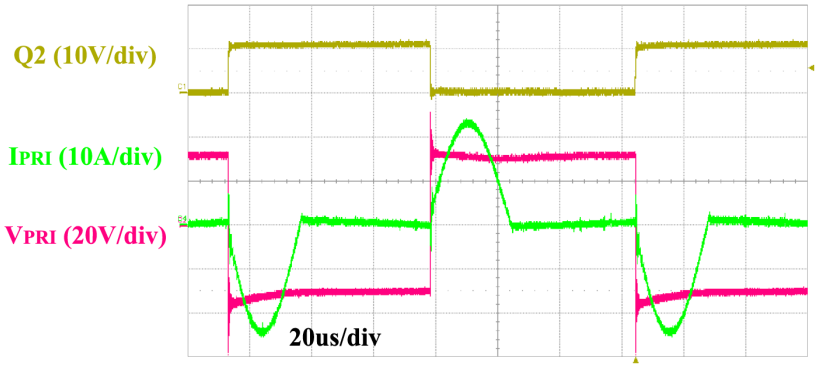

Figure 3.16: Experimental waveforms with fixed-frequency modulation under 30V input, 400V output, and 180W load conditions.

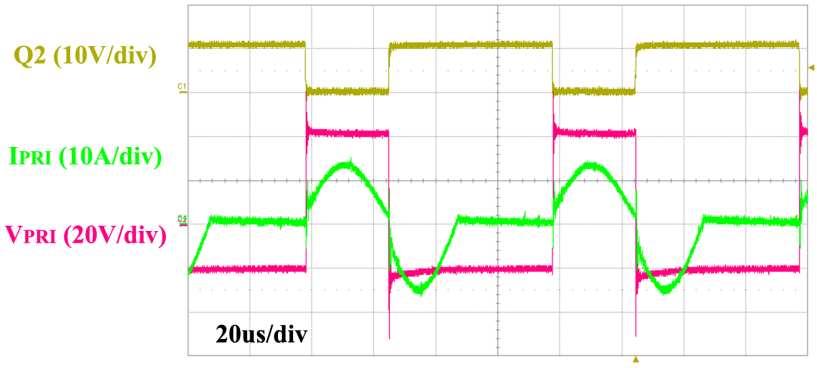

Figure 3.17: Experimental waveforms with hybrid-frequency modulation under 20V input, 400V output, and 180W load conditions.

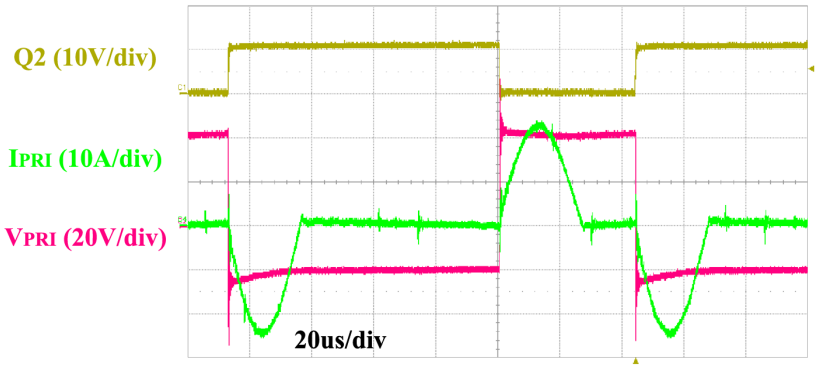

Figure 3.18: Experimental waveforms with fixed-frequency modulation under 20V input, 400V output, and 180W load conditions.

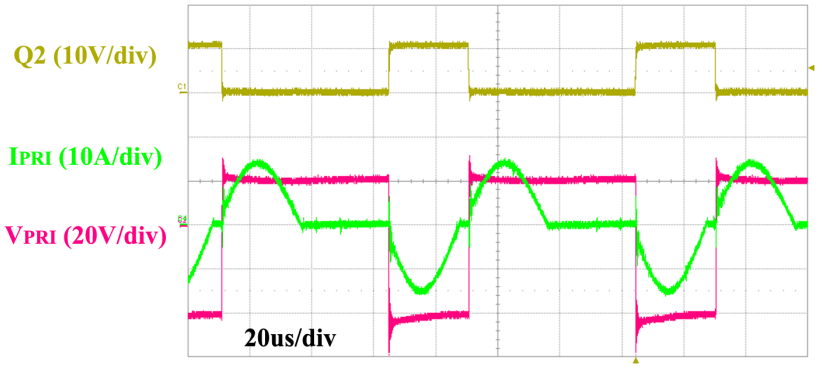

Figure 3.19: Experimental waveforms with hybrid-frequency modulation under 40V input, 400V output, and 180W load conditions.

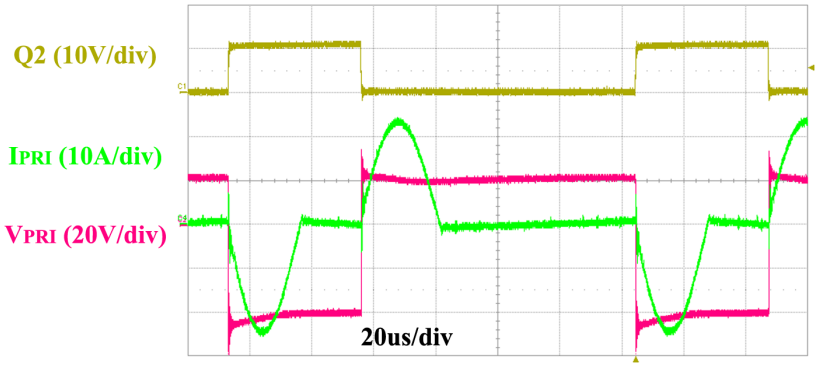

Figure 3.20: Experimental waveforms with fixed-frequency modulation under 40V input, 400V output, and 180W load conditions.

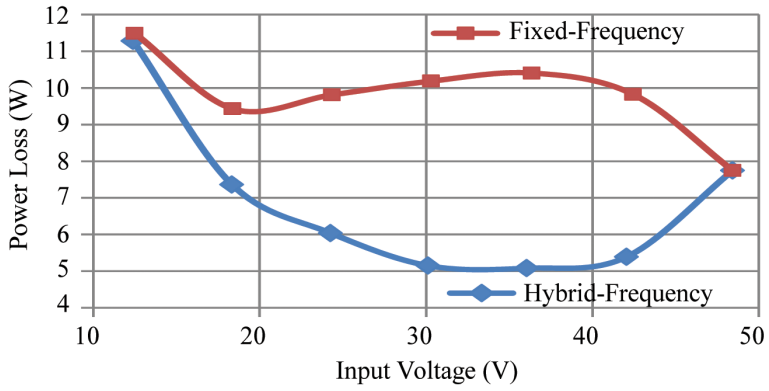

Figure 3.21: Experimental loss comparison (180W)

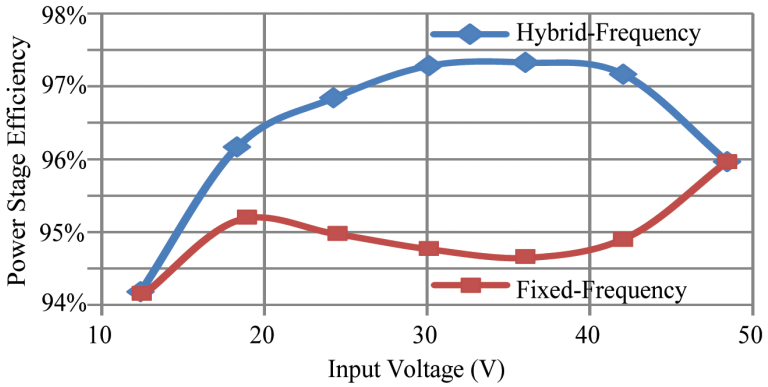

Figure 3.22: Experimental efficiency comparison (180W)

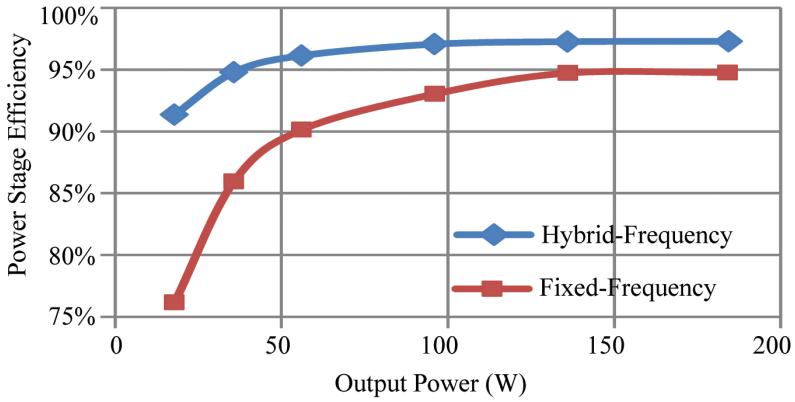

Figure 3.23: Experimental efficiency comparison (30V Input)

Also, a full (10-100%) sweep of the efficiency curve was conducted at the nominal input voltage of 30V. The results provided in Fig. 3.23 clearly demonstrate the improvement of the hybrid-frequency algorithm at all points across the output power range. Using the proposed modulation method a weighted efficiency gain of over 4% (92.6% - 96.7%) was realized. If considering the converter performance under the California Energy Commission (CEC) techniques [14], the average weighted efficiency increases from 94.1% to 95.5%. The efficiency data for the CEC analysis is given in Figs. 3.24 and 3.25. Once again, power measurements were taken using four Fluke Model 287 digital multimeters.

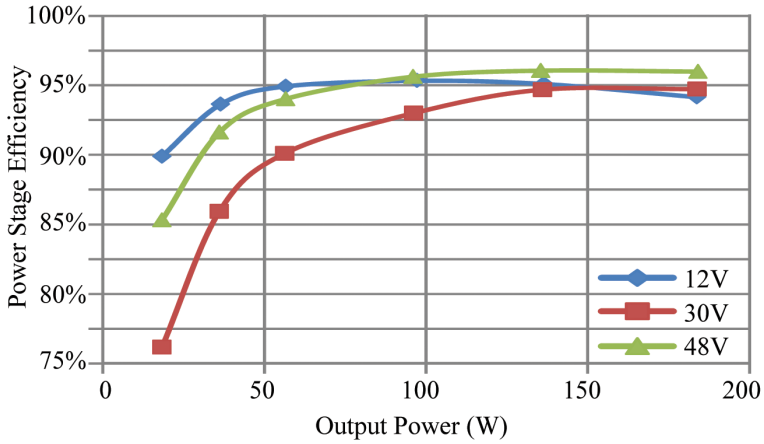

Figure 3.24: Experimental efficiency (fixed-frequency)

For the majority of PV systems, such a wide range is unnecessary. Restricting the range to a more reasonable $25 - 35V$ allows for increasing the rated power to the original 250W level, the CEC efficiency, with curves shown in Fig. 3.26 rating increases to 97.2%, a 0.4% improvement over the traditional PWM methods.

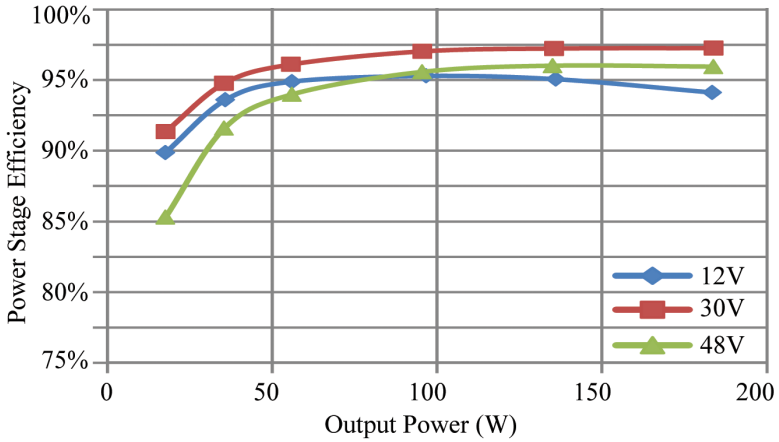

Figure 3.25: Experimental efficiency (hybrid-frequency)

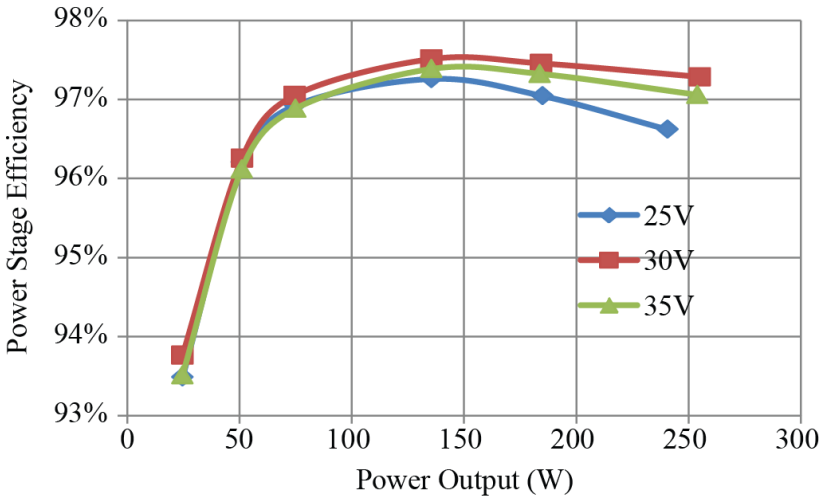

Figure 3.26: Experimental efficiency over full-power (hybrid-frequency)

3.4 Summary

In order to extend the line range of the IBR converter while maintaining high weighted efficiency, a special hybrid-frequency modulation scheme is proposed. The scheme reduces core and conduction loss dramatically by decreasing the applied volt-seconds at the transformer and improving the switching period utilization. With hybrid-frequency control, the

circuit also maintains ZCS for the output diodes, minimizes switching loss, and eliminates circulating energy at the transformer across the entire operating range. It also allows for a predictable voltage gain dependent only on duty cycle and transformer turns ratio. The algorithm uses fixed-frequency, constant-on, and constant-off techniques depending only on the required duty cycle. At extremely high or low duty cycles, the converter operates under fixed-frequency control to limit the maximum switching period and prevent magnetic saturation. At a duty cycle less than 50%, but above the specified minimum, the converter operates under constant-on control, ensuring that the resonant period fully completes. Likewise, for duty cycles greater than 50%, the converter operates under constant-off, ensuring complete resonance. Under this method, dramatic reductions in transformer core loss and converter conduction loss are possible for a small increase in switching-related losses. In support of this algorithm, a theoretical analysis was provided that matches well with experimental data for the majority of line and load conditions. Implementation of the algorithm is straightforward on a modern MCU or DSP, with flexibility available to the designer with regard to computational complexity and data storage. If so desired, all of the necessary computation may be performed off-line and the modulator becomes a simple look-up operation. Regardless, an algorithm for either on-line computation of look-up table population was presented, along with justification for at least three different methods of implementation. Finally, experimental verification of the efficiency improvements with the proposed modulation method over the fixed frequency method were also presented. At the nominal voltage, the CEC efficiency is improved by 4%. With the average of low, nominal, and high input voltage, the CEC

efficiency is improved by 1.5%. When the power rating is increased to 250-W, the CEC efficiency is 97.2%. It should be noted that such a significant efficiency improvement was achieved with no other circuit changes.

Chapter 4

Capacitor Transient Limited Soft-Start

The past two chapters have revolved around optimizing converter efficiency in the presence of technical challenges common to distributed PV systems in a static sense. A circuit topology and modulation scheme have been developed that are capable of operating the required system functions, such as MPPT and fault handling. Shifting focus somewhat to a more dynamic problem, this chapter investigates a significant issue in distributed micro-converter based PV systems known as startup. The centralized inverter, by virtue of converting dc to ac, injects a significant amount of ripple energy into the PV side of the system. The magnitude and nature of this ripple energy depends on several factors, such as the nature of the utility interface (single-phase or three-phase), line frequency, power level, and modulation index. The only way for the inverter to deal with this ripple energy is

through increasing the size of the dc-link capacitance, which appears also as a shared output capacitor from the point-of-view of the micro-converter network. As the size and power level of the inverter increases, so does this necessary capacitance, to a point where it can be many times larger than the micro-converter's nominal on-board output filter. Many of these inverters, either by topology or control, are inherently unidirectional, meaning that power is only allowed to flow out to the utility, not in reverse. This implies no "pre-charging" of the dc-link capacitor is possible, and also implies that all of the initial energy plus the inverter's auxiliary losses must be supplied from the PV array through the micro-converters. Thus the micro-converters must start up with zero output voltage, looking into a capacitive load so large that it is a virtual short-circuit. This is especially true given that without synchronization of micro-converter startup, the first unit on-line will have to drive the entire capacitive load by itself. Needless to say, such conditions are less than optimal. And many converters, especially bridge, resonant, or quasi-resonant topologies have defined operating regions with drastically different behavior if conditions are not optimal, leading to the necessity of "soft-start" to prevent potential device over-stress or thermal failure. Specifically in dc-dc converters, there are a number of proposed soft-start schemes, ranging from duty cycle ramps to dedicated soft-start circuits. In isolated converters, soft-start is further complicated by the fact that no energy transfer occurs between the primary and secondary sides until the converter begins switching. Couple this with an unknown, but very large, capacitive load, and the startup problem becomes quite complex. Though discussion of soft-start is rare, methods have been presented for bridge topologies, such as high-frequency regulation [64],

[65], pulse-width control [66], [67], the addition of an external clamp circuit [68], [69], or the use of an external pre-regulator [70]. A few authors tout the inherent soft-start and overload behavior of the series or LLC resonant converters as a reason to avoid traditional soft-start [39], [71], [72]. However, without sufficient large leakage inductance in the transformer or significant over-rating of the semiconductor devices, omission of soft-start could lead to disastrous consequences [73]–[75]. Though there are a number of soft-start techniques available, one cannot blindly apply a method and expect correct behavior. Moreover, when investigating a new topology, it is prudent to consider the exact nature of its operating in order to develop an effective soft-start algorithm. The validity of this concept will be demonstrated through analysis of the Integrated Boost Resonant (IBR) converter, especially in comparison to its more traditional counterpart, the series or LLC resonant converter. From that analysis, it is possible to both model the behavior of the converter during the transient period, as well as determine effective methods implementing startup control. Out of the fundamental analysis in the proceeding sections, a capacitor transient limited (CTL) soft-start method is proposed. The method utilizes the high-frequency transient appearing across the lower primary-side resonant capacitor to indicate an over-current condition during startup. The sensing circuit schematic and related design procedure are outlined, along with specific information regarding handling comparator, PWM, and gate drive delay. Limiting the transient current using this method allows for reliable control without expensive or lossy isolated sensing. The resulting soft-start mechanism is demonstrated experimentally with a 250-W IBR prototype over a wide output capacitance range from 2μF - 500μF, under

operating conditions that would otherwise result in a converter failure.

4.1 Initial Condition Evaluation

In order to determine the appropriate soft-start method, it is critical to determine the circuit's initial conditions with both input and load, but without device switching. As an example, an LLC (or series resonant) half-bridge is shown in Fig. 4.1. Rather than having a single resonant capacitor on the primary side, it is split into two that are in series from a dc perspective, but appear in parallel at higher frequencies. Assuming the two capacitors are equal, potential applied at the input terminals is distributed evenly across both capacitors. On the other hand, without any secondary voltage initially, the potential across either high-side capacitor is identically zero, as shown in Fig. 4.2. Once the primary-side MOSFETs, Q_1 and Q_2, begin switching, the secondary-side capacitors begin to charge through the transformer. With no load, the converter reaches an equilibrium where the output is a direct reflection of the input, shown in Fig. 4.2(b). With load, the equilibrium solution will vary based on output current, switching frequency, duty ratio, and resonant component values. During startup, the converter transitions between the initial case and the equilibrium case, requiring energy transfer from the primary to the secondary side. The rate at which the circuit approaches equilibrium is directly dependent on the magnitude of energy transferred through the resonant circuit. For a soft-start, it is desirable to control the rate of change in the secondary side such that the resonant circuit does not become over-loaded. With

no resistive load on the secondary-side, the upper capacitors mirror each other, while the lower capacitors mirror each other. Thus, it is necessary to control the amount of charge transferred per switching cycle, or the current, flowing out of both the upper capacitor and the lower capacitor during each half-cycle. This can be accomplished through a variety of means, such as pulse-width control, high-frequency modulation, or an auxiliary startup circuit.

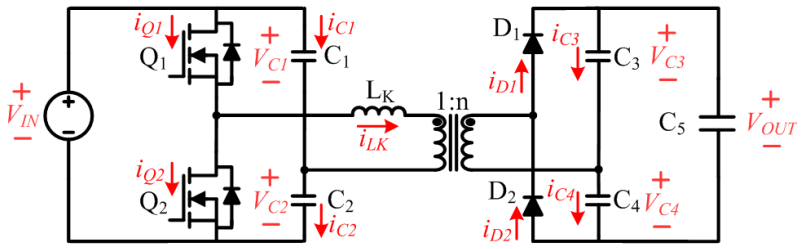

Figure 4.1: Series resonant converter topology

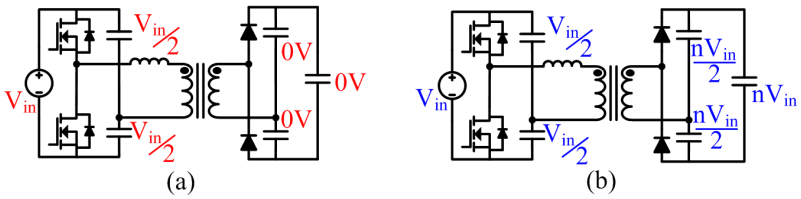

Figure 4.2: Series resonant converter initial and equilibrium states

On the other hand, consider the IBR converter shown again in Fig. 4.3. This circuit is a hybrid between the series resonant converter shown previously and a synchronous boost converter, sharing the two primary-side MOSFETs. Unlike the traditional SRC, the IBR can be controlled with complementary pulse-width-modulation (PWM). Because of the hybrid strategy, a dc path is formed between the input source and the lower primary-side capacitor, which allows the capacitor to charge up to the full input voltage as shown in Fig. 4.4(a). Consequently, there is zero voltage across the upper primary-side capacitor or either of the

secondary-side capacitors. Once the primary-side MOSFETs begin switching, the circuit transitions to the equilibrium solution shown in Fig. 4.4(b). Notice that the voltage across the lower primary-side capacitor remains at V_{in}, while the voltage across C_1 is dependent on the converter duty cycle, D, which is referenced to Q_2. In the same way as the series resonant converter, the secondary-side capacitors mirror the voltage from the primary-side.

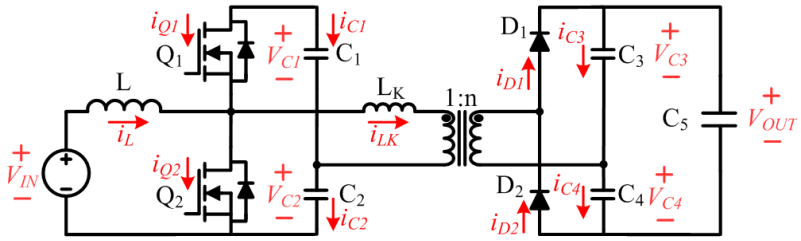

Figure 4.3: IBR converter topology

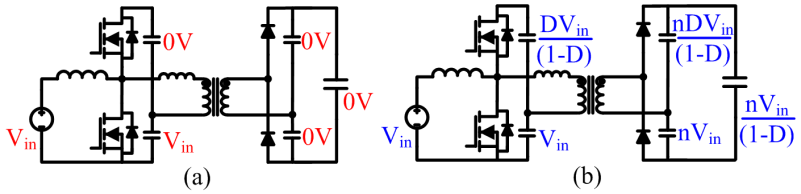

Figure 4.4: IBR converter initial and equilibrium states

Unlike the traditional series resonant converter, the IBR only has one output capacitor whose equilibrium voltage is independent of duty cycle. Thus, in order to control the current in the resonant loop, it is only necessary to regulate the current (or charge) that flows out of C_2. During startup, it is possible to limit the overall peak current in the system by simply controlling the on-time of the lower switch, without any regard to how long the upper switch is on. This allows the IBR to eschew more complex startup methods, such as pulse-width or high-frequency control, in favor of basic duty cycle limitation.

Though the resonant current may be controlled through the lower switch duty cycle,

selecting the proper duty cycle value for a given instant in time is paramount. One traditional method to soft-start PWM converters is a time-based ramping limit on the duty cycle. This is especially effective in systems where the output capacitance and loading is known, and thus the length of the startup transient. In situations where the output capacitance and loading is unknown, a blind duty cycle ramp could still result in an overcurrent situation or a failed startup attempt. Rather than a duty cycle ramp, it is also possible to provide a small, fixed duty cycle until the converter reaches equilibrium. Afterwards, the duty ratio can be increased further, up to the desired operating value. However, this method is extremely slow and still requires secondary-side sensing in order to determine if an equilibrium has been reached.

Other popular over-current protection schemes involve directly monitoring the peak current in the transformer. This is often implemented using either a hall-effect sensor, a current transformer (CT), a current-sense resistor, or a sensor across a floating capacitor [76], [77]. These methods are often too slow (hall-effect), too costly (CT), or lossy and difficult to measure (resistor or floating resonant capacitor) to implement in many cases [78], [79].

4.2 IBR Startup Transient Analysis

As it was unwise and inefficient to blindly apply a soft-start control mechanism, so also the sensing method must be derived from the circuit behavior. For lower switch on-times less than the resonant period, circuit operating modes are shown in Fig. 4.5 and a timing

diagram in Fig. 4.6. Note that this set of operating modes assumes a short on-time for Q_2, which is not the normal operating condition for the IBR.

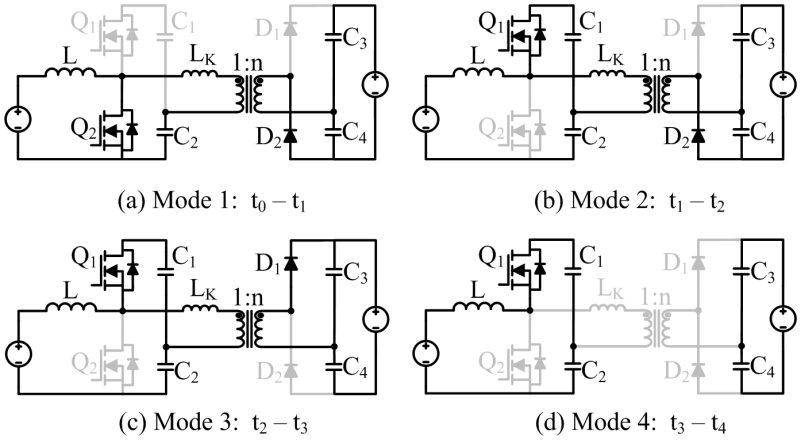

Figure 4.5: IBR startup-transient operating modes

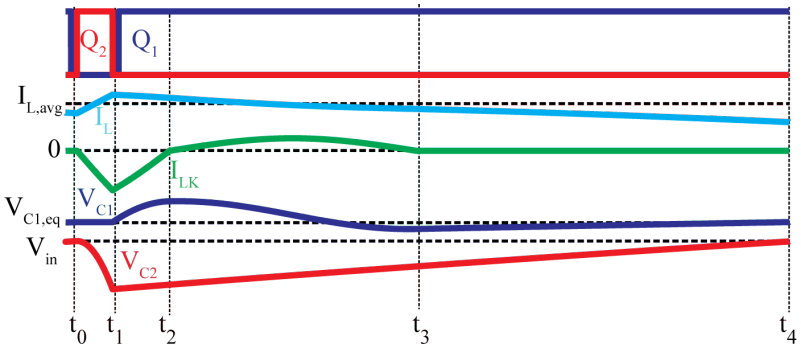

Figure 4.6: IBR startup-transient timing diagram

4.2.1 Mode 1: (Q_2 and D_2 active; $t_0 - t_1$)

When Q_2 is turned on, C_2 begins discharging into the output through L_K and D_2. This discharge rate is dependent on the voltage difference between C_2 and C_4, which is typically largest in the initial pulses. Separately, the input inductor current, I_L, increases linearly, based on the input voltage. This mode ends when Q_2 is turned off. The final current

in the transformer primary (at time t_1) in this operating mode, can be written as:

$$i_{LK,pk-} = -\left(V_{C2} - \frac{V_{C4}}{n}\right)\sqrt{\frac{C_{eq}}{L_K}}\sin\left(\frac{DT_{sw}}{\sqrt{C_{eq}L_K}}\right) \tag{4.1}$$

4.2.2 Mode 2: (Q_1/D_{Q1} and D_2 active; $t_1 - t_2$)

When Q2 is turned off, the transformer current free-wheels through the body diode of Q_1 (D_{Q1}), charging C_1. During this interval, the current in the input inductor also freewheels through the diode, charging both C_1 and C_2 in series. Q_1 may then be turned-on under ZVS. This period ends once the current in L_K decays to zero, and D_2 is naturally commutated. The length of this interval is given by the following equation:

$$\Delta t_{1-2} = -i_{LK,pk-}\left(\frac{L_K}{V_{C1} + \frac{V_{C4}}{n}}\right) \tag{4.2}$$

The total charge transferred during modes 1 and 2 can be written as:

$$Q_{1-2} = -\int_{t_0}^{t_2} i_{LK}(t)dt \tag{4.3}$$

$$Q_{1-2} = \left(V_{C2} - \frac{V_{C4}}{n}\right) C_{eq} \left(1 - cos\left(\frac{DT_{sw}}{\sqrt{C_{eq}L_K}}\right)\right) - i_{LK,pk-}\left(\frac{\Delta t_{1-2}}{2}\right) \tag{4.4}$$

4.2.3 Mode 3: (Q_1 and D_1 active; $t_2 - t_3$)

With Q_1 remaining on, the current begins to flow resonantly from C_1, through the transformer and through the output. The input current continues to charge the series combination of C_1 and C_2. This continues until the current in L_K resonates back to zero, and D_1 turns off.

4.2.4 Mode 4: (Q_1 active; $t_3 - t_4$)

Both secondary-side diodes are off, and the transformer current is zero. The input current continues to charge C_1 and C_2 linearly until Q_1 is turned off and D_{Q1} is hard-commutated by Q_2 turning on, thus completing the switching cycle. In order to guarantee zero dc current in the transformer, the amount of charge transferred during modes 1 and 2, must equal the charge transferred to the secondary-side during mode 3 (no charge is transferred during mode 4). However, because of the voltage doubler configuration, only half of the total charge is transferred to the output capacitor. Thus, the gain in voltage for the lower output capacitor C_4, and consequently V_{out}, over the entire cycle may be

approximated as:

$$\Delta V_{C4} \approx \frac{Q_{1-2}}{nC_o} - \frac{V_{out}T_{sw}}{R_{load}} \tag{4.5}$$

Some key points to note from this discussion of operating modes:

1. The only time that C_2 is discharged is when Q_2 is on, and the charge flowing through the transformer (and the output) during this interval is entirely from C_2.

2. Because the conduction interval for Q_1 is much longer than Q_2, and a lack of dc bias on the transformer, the overall peak current is directly controlled by Q_2

3. The total charge transferred to the output, thus the rms current in the resonant loop, is directly dependent on the charge delivered from C_2.

Thus, it is possible to control not only the peak current in the transformer (and resonant loop), but also the total charge transferred to the output simply by controlling the amount of charge transferred from C_2 during Mode 1. From basic physical principles, the charge leaving C_2 is proportional to the voltage drop during that interval.

$$\Delta Q_{C2} = C_2 \Delta V_{C2} \tag{4.6}$$

This gives a theoretical basis for a new soft-start method, capacitor transient-limited (CTL) soft-start.

4.3 CTL Sensing Circuit and Design Procedure

Two principle issues with regard to implementing CTL startup:

1. Design and implementation of a suitable circuit for sensing the capacitor transient in the presence of dc voltage, low-frequency oscillation, and high-frequency switch-node ringing.

2. Selection of an appropriate trip point which limits the resonant current to an acceptable level during startup. (Covered in the next section)

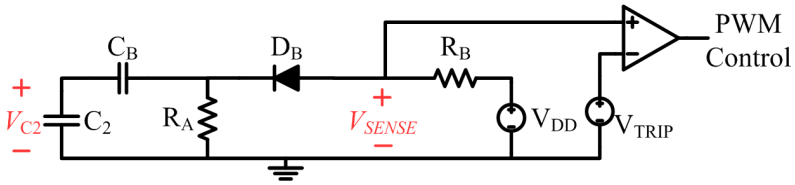

Figure 4.7: CTL sensing circuit diagram

Developing an effective, low-cost sensing circuit for this method is reasonably straightforward, a diagram of which is shown in Fig. 4.7. This type of circuit is in some ways analagous to the lossless current sensing developed for low-voltage dc-dc converters [80], [81]. First, a blocking capacitor, C_B, is necessary to remove the dc-component, as well as any low-frequency transients from the sensed signal. The resulting ac transient can be seen across a load resistance, R_A. However, because the measured transient goes below the steady-state value, the measured voltage across R_A is negative. Thus, the remaining components are added as a level-shift to bring the signal up to a compatible level for single-supply digital logic. The reverse blocking diode, D_B, prevents a potential transient voltage from damaging

the low-voltage signal-processing, and also adds additional level shifting. The logic-level dc rail is used as a supply to power the reference (often 3.3 or 5V). The comparator may be an external circuit, or a dedicated portion of the control IC, such as the internal comparator of a digital signal processor (DSP). The output signal from the comparator goes low when the capacitor transient drops below the threshold, V_{trip}, a signal that can be combined with the PWM output for Q_2 using AND logic.

In order to design an effective sensing circuit, the following design procedure is recommended:

1. Select the resistors R_A and R_B in order to provide sufficient dc-bias such that the ac-transient is within the operating range of the comparator logic. Also, the resistors should be small enough that the leakage current of the diode doesn't have a significant impact on the measurements (the experimental circuit had a diode bias of 1mA). An expression for the dc-bias voltage at the positive comparator input is provided in (4.7).

$$V_{sense} = \frac{V_{DD}R_A + V_{DB}R_B}{R_A + R_B} \tag{4.7}$$

2. Select the filter cut-off frequency, by selecting C_B, such that the dc-component and low-frequency ripple is removed, but the high-frequency transient is not attenuated. The ac transfer function of the circuit in Fig. 4.7 is given in (4.8), with an angular cut-off frequency provided in (4.9). In order to sufficiently filter out low-frequency oscillation with a first-order filter, the authors recommend setting the cut-off frequency at a value

of $2\pi f_{sw}$.

$$\frac{\widehat{v}_{sense}}{\widehat{v}_{C2}} = \frac{s/\omega_C}{s/\omega_C + 1} \tag{4.8}$$

$$\omega_C = \frac{R_A + R_B}{R_A R_B C_B} \tag{4.9}$$

Also of concern in some systems is the high-frequency ringing that often accompanies switching transients. Several options are available to mitigate the effect of switch-node ringing: finding a comparator with a sufficient hysteresis band, low-pass filtering the comparator output, or adding blanking time in the immediate area around the switching transition.

4.4 Transient Trip Level Selection

Equally significant is the selection of the proper V_{trip} level, inorder to limit the resonant current to an acceptable value at startup. Assuming the designed filter doesn't attenuate the capacitor transient, the desired transient limit is merely the difference between the selected bias level from the previous section and the trip limit, shown in (4.10). Depending on the voltage across C_4 (related to the energy already transferred to the output), this capacitor transient may be directly related to the peak current seen at the transformer, as shown in the first term of (4.11). However, the detection system does not react instantly to a trip event, and has some measureable delay. This delay can be attributed to a number

of factors: filter phase delay, comparator hysteresis or output delay, PWM logic delay, gate drive propagation, and MOSFET turn-off delay. In the experimental system, the most significant of these was gate-drive propagation delay and MOSFET turn-off delay, resolving to a delay of at least 200ns in the experimental system.

$$\Delta V_{C2}^{*} = V_{sense} - V_{trip} \tag{4.10}$$

This extra delay results in the actual peak current being larger than the expected value, represented by the addition of the second term in (4.11). This effect becomes more prominent with increased input voltage, and must be accounted for in the protection system design. As another byproduct of the delay, a minimum threshold on the peak current limit is imposed, restricting the potential effectiveness of the technique. If tight control of the peak current is desired, this delay should be reduced. By introducing a separately driven turn-off NPN BJT to the gate of Q_2, driven with inverted logic, the primary gate driver could be bypassed, reducing the total delay from 350ns to 220ns in the experimental system.

$$i_{L,pk-} = \sqrt{\frac{2\Delta V_{C2}^{*} C_2 \left(V_{C2} - \frac{V_{C4}}{n}\right)}{L_K}} + \frac{\left(V_{C2} - \frac{V_{C4}}{n}\right)}{L_K} t_{del} \tag{4.11}$$

For the purposes of design, it is simpler and potentially more relevant to focus on the overall peak current during the startup transient, rather than at each individual point. The overall peak current generally occurs at the first gate pulse, when the lower output capacitor

has zero voltage across it. This simplifies the peak current expression to the value shown in (4.12).

$$i_{L,pk-}(1) = \sqrt{\frac{2\Delta V_{C2}^{*} C_2 V_{in}}{L_K}} + \frac{V_{in}}{L_K} t_{del} \tag{4.12}$$

In the interest of completeness an expression regarding the deviation of the capacitor transient from the designed value has been provided in (4.13). Thus, the envelope seen around the measured v_{sense} can be significantly larger than the expected v_{trip} value, if the delay is large.

$$\Delta V_{C2} = \Delta V_{C2}^{*} + \frac{t_{del}}{C_2}\left(i_{L,pk-} - \frac{\left(V_{C2} - \frac{V_{C4}}{n}\right)}{L_K} t_{del}\right) \tag{4.13}$$

However, though the delay is a negative impact, its effect can be mitigated through understanding of the delay sources and careful design. A prototype system with has been developed using this design procedure, and the results are outlined in the proceeding section.

4.5 Experimental Results

In order to demonstrate the effectiveness of the CTL soft-start method, the scheme was implemented on a 250-W prototype IBR converter. The system parameters for the prototype are provided in Table 4.1. In order to implement the PWM logic and general

control laws, a Texas Instruments TI320F28026 micro-controller unit (MCU) was utilized. The comparator circuit was implemented using one of the dedicated comparator subsections, which allows the negative input pin to be driven by an internal digital-to-analog converter (DAC). The output of the comparator is applied to the PWM output signal for the lower device using the Tripzone subsystem. Once the comparator output goes low (indicating that the capacitor voltage has dropped below the specified threshold) the command to Q_2 goes low while Q_1 is turned-on. The comparator output also triggers a cycle-by-cycle trip event that holds the gate of Q_2 low until the next switching cycle begins.

Table 4.1: IBR Prototype Parameters

Parameter	**Value**	**Parameter**	**Value**
Input	20-40V	Output	400V
L	100μH	C_1, C_2	10μF
C_3, C_4	100nF	L_K	350nH
n	6.67	F_{sw}	70kHz
D	33%-67%	C_5	2-500μF

Surrounding the comparator and PWM logic in the MCU is the CTL sensing circuit, with parameters outlined in Table 4.2.

Table 4.2: CTL Sensing Circuit Parameters

Parameter	**Value**	**Parameter**	**Value**
R_A	1kΩ	R_B	750Ω
C_B	10nF	V_{DB}	0.5V
V_{DD}	3.3V	V_{sense}	2.1V
V_{trip}	1.77V	ω_C	233krad/s

The true benefit of this scheme, however, is demonstrated by the experimental behavior. In order to be effective, the CTL soft-start method needs to well limit the startup current regardless of input voltage or output capacitance. For the experiment, only a small

load ($< 1\%$ of rated load) was added for safety as a bleeding resistor. For the experiment, the controller was given a fixed duty cycle command, according to the applied input voltage, which would produce a 400V output. The converter was then allowed to startup, reaching steady-state at the desired output voltage with no further commands. If the CTL soft-start logic was not active, there was a high probability of converter failure. The converter transient response of one such failed attempt is included in Fig. 4.8. With 30V input and 46uF output capacitance (similar conditions to Fig. 4.13, the output voltage increased only to 10% of the rated output before the greater than 150A resonant current caused Q_2 to fail.

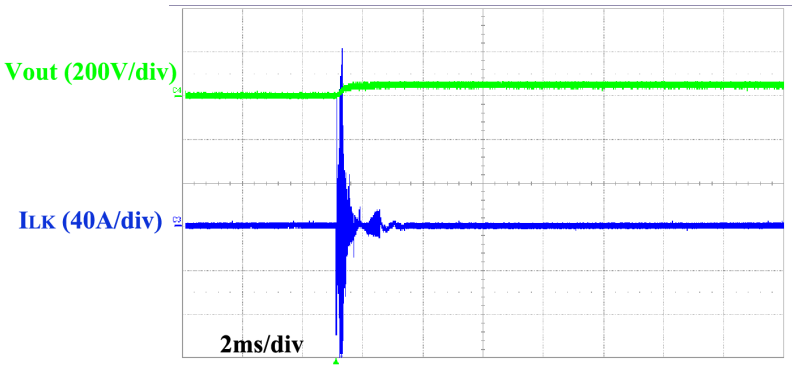

Figure 4.8: Experimental failed startup (30V input / 46uF output capacitance)

However, the CTL circuit was active to limit the applied duty cycle, and therefore the resonant current. The experiment was then repeated at three input voltage levels (20V, 30V and 40V), and three output capacitance values (2μF, 46μF and 500μF). In accordance with the analysis in the previous section, there is a slight variability between the three input voltage levels, shown in Figs. 4.9, 4.10, and 4.11, due to the impact of t_{del}, though the peak current remains well-regulated. The waveforms match well with the theoretical analysis, plotted in Fig. 4.12 for reference. On the other hand, the behavior between the three

capacitance values remains quite consistent, as shown in Figs. 4.11, 4.13, and 4.14, even though the output capacitance is increased over 250 times the original (on-board) value.

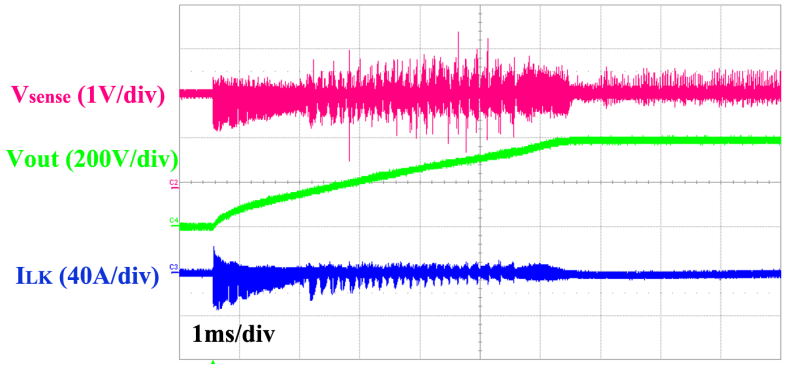

Figure 4.9: Experimental waveforms (20V input/400V output/ 2μF output capacitance)

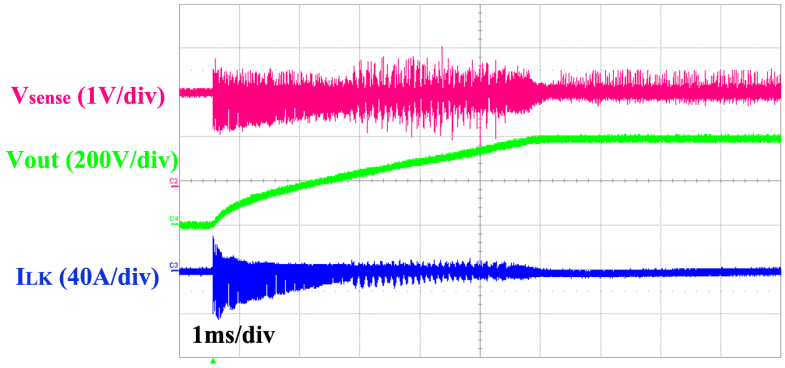

Figure 4.10: Experimental waveforms (30V input/400V output/ 2μF output capacitance)

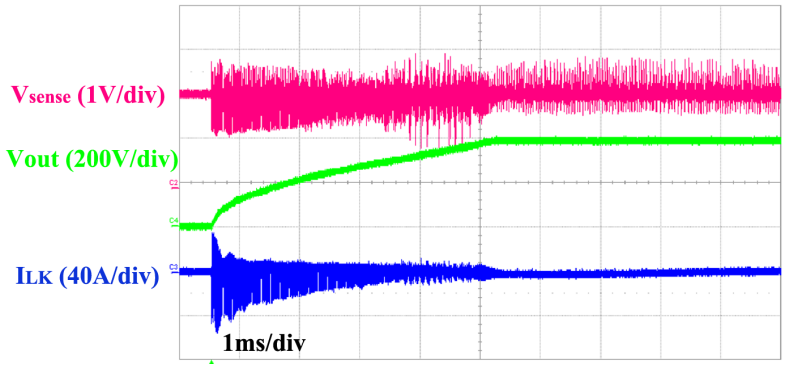

Figure 4.11: Experimental waveforms (40V input/400V output/ 2μF output capacitance)

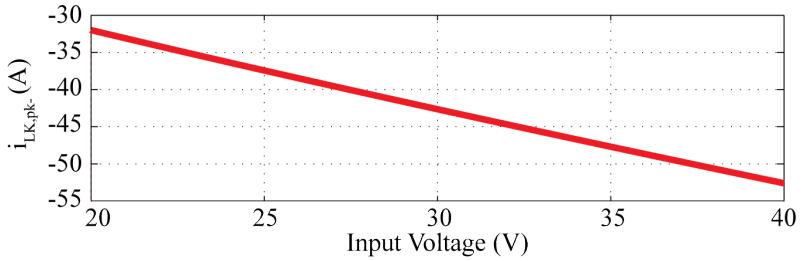

Figure 4.12: Theoretical negative peak current in the transformer

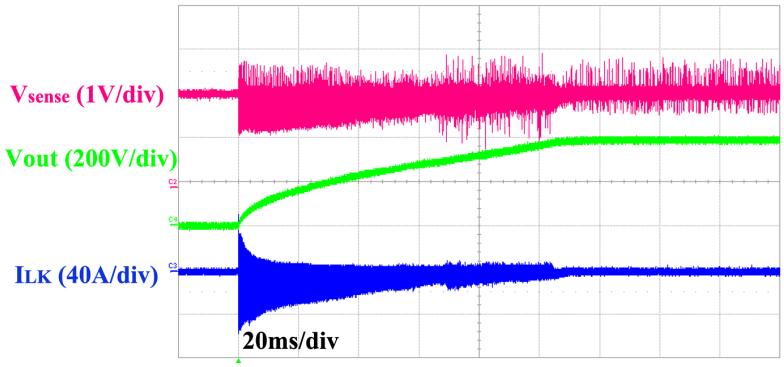

Figure 4.13: Experimental waveforms (40V input/400V output/ 46μF output capacitance)

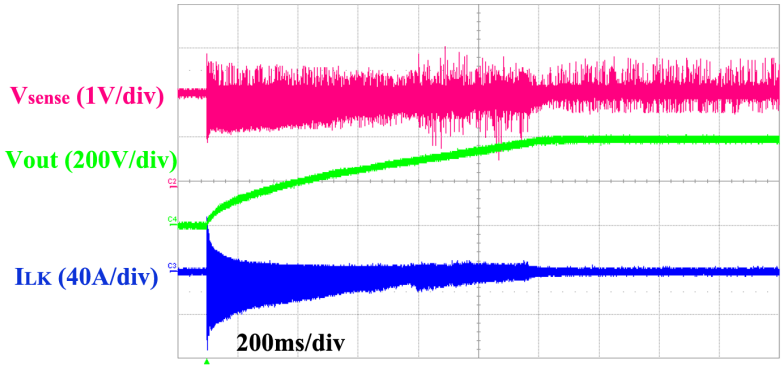

Figure 4.14: Experimental waveforms (40V input/400V output/ 500μF output capacitance)

4.6 Summary

When regulating the rate of change between the initial and equilibrium states in the IBR converter, it is necessary to implement a soft-start mechanism in order to avoid a potential over-stress or thermal failure situation. Unlike the traditional series resonant or LLC converters, the IBR doesn't require a special soft-start mechanism, such as high-frequency or pulse-width control, because only one output capacitor has an equilibrium voltage value that is independent of duty cycle. This allows for converter startup under traditional duty cycle control. When selecting the appropriate duty cycle, however, the proposed CTL soft-start method has nearly zero loss and is extremely low-cost compared to other traditional methods. The CTL method can handle a wide range of input or output conditions, including a 250x increase in output capacitance. Implementation of the CTL circuit is straightforward, requiring only a small, blocking capacitor, two resistors, a protection diode and a comparator (which may be integrated into the control IC). The CTL method regulates the resonant current by limiting the high-frequency transient across the lower primary-side capacitor, turning off Q_2 early if the situation requires it. Design procedures for both the sensing circuit and the trip level were outlined, taking into account the intrinsic delay of the semiconductor components.

Finally, the effectiveness of the circuit was demonstrated by implementation on a 250-W prototype IBR converter. Detailed system and circuit parameters were provided, along with a description of the implementation on a TI MCU. Experimental waveforms

demonstrating a consistent response across both input voltage and output load conditions were shown, verifying the efficacy of the proposed method.

Chapter 5

Model-Driven Optimization of MPPT Efficiency

Though many criteria may be established for evaluating PV PCS, the entire problem can be quickly boiled down to one quantity, kilowatt-hours (kWh). How much energy is finally output to the utility, given array and weather conditions, is truly the most critical value to the equipment owner. Because this criteria is extremely difficult to compare and make relative evaluations in-system, other criteria is often substituted, such as CEC efficiency of PCS equipment. In isolation, such substitutions have wildly varying accuracy with regard to predicting relative energy harvest. The PCS efficiency only measures how much energy the PCS loses internally to the converter, but it gives no indication of the capability of the converter at extracting energy from the actual PV panel. As mentioned previously, extracting the maximum available energy from a PV panel requires the ability to accurately locate the

maximum power point. Efforts to quantify this capability have established a quantity known as MPPT efficiency [82] to represent the steady-state accuracy of the MPPT algorithm. Others argue that because the actual MPP is significantly dynamic, this measurement should be augmented with efforts to evaluate dynamic MPPT ability [83], especially in the presence of noise [84]. Whether or not this characterization is helpful, a potentially more critical question in many cases is the evaluation of the ability of the converter to maintain operation at the MPP once it is located. Even if the MPP is established, ripple in the panel voltage or current will carry the panel operating point away from the established optimum. Regardless of the frequency of this ripple, the average displacement from the PV MPP results in a net reduction in the harvested energy. If the ripple is large enough, this can result in a significant decrease in PV power. There are three primary contributors to PV ripple: converter or inverter switching ripple, maximum power point tracking (MPPT) ripple, and double line-frequency ripple in grid-connected systems [85]. Before [86] and [87], authors considered only one ripple source, at the exclusion of all others, and had yet to produce a model to assess the impact of ripple sources operating simultaneously. In [88] the authors work to verify an approximate PV model in a more formalized method than in [89], testing the model at several frequencies, but do not demonstrate model validity with simultaneous ripple.

More important than the specific model chosen is the ability to make appropriate design decisions for PCS equipment. These decisions are best informed by specific insight offered by PV modeling. These design decisions include passive component selection, the

quality of sensing and filter circuits, as well as control system complexity and performance. Rather than being superfluous portions of the design sequence, these types of decisions have a direct impact on the energy harvesting capability of the PCS. This chapter is an attempt to consolidate existing treatments of PV ripple related issues and direct the analysis in a direction consistent with the preceding micro-converter discussion.

5.1 PV Modeling Extension

The variety of PV models available in literature is astounding, and it ranges from the alarmingly simple to the outrageously complex. By far the most popular PV model involves a single current source in parallel with a diode, as well as a parasitic series and shunt resistance, as shown in Fig. 5.1. The nonlinearity of the junction diode makes the PV cell remarkably difficult to analyze, especially with traditional tools for linear system analysis. Some efforts to model ripple-related losses have attempted to utilize the non-linear model [90] with certain simplifying assumptions, such as neglecting the series resistance. Specifically in [91], the authors solution is a series of Bessel functions which can become quite cumbersome. A more reasonable solution is presented in [19], where the authors attempt to model the PV cell as a quadratic function of the cell voltage. This approach is confirmed by the authors of [88], who use a Taylor series expansion of the ideal PV equation to generate a quadratic function with alternate definitions for the coefficients. The quadratic model shows good correlation to the non-linear model within the neighborhood of the MPP, with the

size of the neighborhood depending dramatically on the sharpness of the knee of the power curve [89]. For a tested mono-crystalline silicon PV panel, the authors report high model accuracy within 3V of the MPP (or 10% of the MPP voltage). When estimating the ripple-related power loss, however, the authors of [19], [89] limit their analysis to injected ripple of a single frequency, their intention being to model the loss due to double-line frequency ripple only. In order to assess the combined losses due to multiple ripple sources, an extension to their analysis is necessary. Beginning with analysis similar to [89], the PV output current can be written as a function of PV terminal voltage in the form of (5.1), where α, β, and γ are constants determined either analytically or through fitting the PV panel I-V curve at the MPP. The methods required to extend this analysis to multiple frequencies is explained in detail in Appendix A., with the resultant expression shown in (5.2).

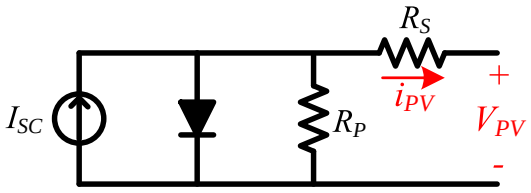

Figure 5.1: PV cell equivalent circuit

$$I_{PV} = \alpha V_{PV}^2 + \beta V_{PV} + \gamma, \text{ [A]} \tag{5.1}$$

$$P_{PV,avg} = P_{mpp} + \left(\frac{3\alpha V_{mpp} + \beta}{2}\right)\left(\sum_{n=1}^{m} {V_n}^2\right) \tag{5.2}$$

The result in (5.2) implies that the actual frequencies of the ripple sources are largely immaterial to the overall PV power loss. The important quantities are merely the PV

voltage-current characteristics (specifically α and β) as well as the square of the amplitude of each ripple frequency, regardless of the source. The Canadian Solar CS6P series (a common residential level panel at the time of this writing) will be used as a baseline case for the analysis in this chapter. The CS6P is rated at roughly 250W output at 1000W/m^2, and has I-V characteristics as shown in Fig. 5.2 and a power curve shown in Fig. 5.3. For this analysis, the quadratic curve fit was carried out in a neighborhood of $\pm$2V of the MPP, as shown in Fig. 5.4, with the results summarized in Table 5.1.

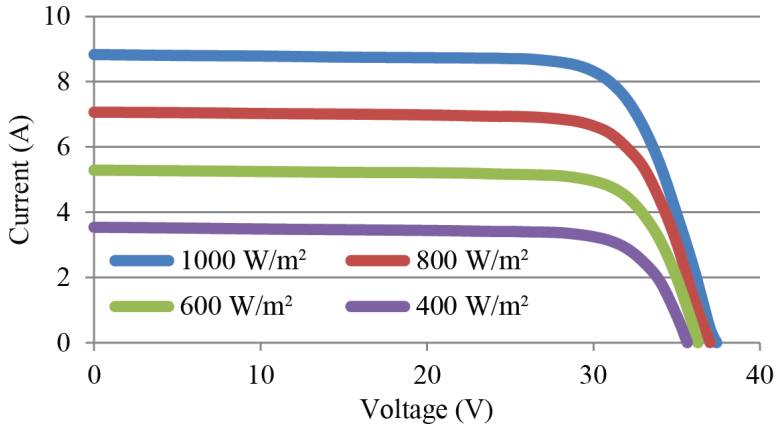

Figure 5.2: Canadian Solar CS6P I-V curve

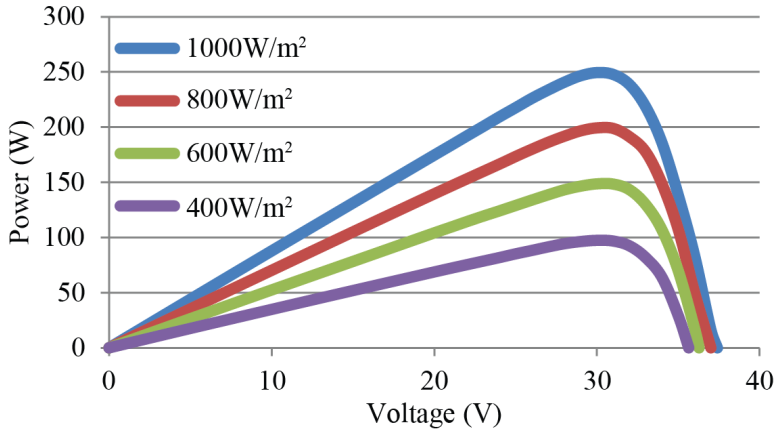

Figure 5.3: Canadian Solar CS6P power-voltage curve

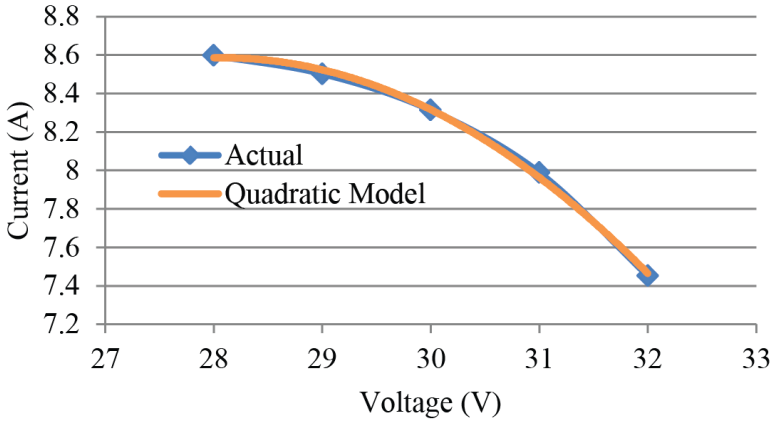

Figure 5.4: Canadian Solar CS6P quadratic curve fit

Table 5.1: CS6P Model Data

Irradiance	**Alpha**	**Beta**	**Gamma**	**V^2 (η_{MPPT}=99.8%)**
1000W/m^2	-0.0728	4.085	-48.76	0.4044
800W/m^2	-0.0593	3.345	-40.35	0.4336
600W/m^2	-0.0403	2.263	-26.67	0.4712
400W/m^2	-0.0301	1.691	-20.36	0.4505

Though the term's history is complex and it's uses are multiple, it makes sense to adopt the term MPPT efficiency (η_{MPPT}) to refer simply to the amount of power extracted from the PV panel versus the total power available at the MPP. Based on the PV model in (5.2), the MPPT efficiency is directly dependent on the sum of the squares of the ripple magnitudes, as illustrated directly in (5.3).

$$\eta_{MPPT} = 1 + \frac{\left(\frac{3\alpha V_{mpp}+\beta}{2}\right)\left(\sum_{n=1}^{\infty} V_n^2\right)}{P_{mpp}} \tag{5.3}$$

For a given panel, this creates a "ripple budget" of sorts if a given MPPT efficiency is to be maintained. The amount of ripple allowed depends on the "softness" of the knee

around the MPP. For the CS6P, as the irradiance is decreased the knee becomes softer, allowing for more ripple voltage without significant reduction in η_{MPPT}. This places the emphasis for design on the high power (1000W/m^2) conditions as the limiting case. Ripple budgets based on irradiance for a 99.8% η_{MPPT} are provided in the last column of Table 5.1. In the proceeding sections the focus will be on estimating and designing around the three major ripple sources while attempting to distribute the ripple budget between them.

5.2 Micro-Converter Switching Ripple

With any switch-mode power converter, there is a switching node which oscillates between two voltage levels. In a boost-type converter, these values are ground (zero potential) and the output level (V_{out}). In the case of the IBR the effective V_{out} is reduced by the transformer turns ratio and is referred subsequently at V_{bus}. Because the two transistors in the IBR are complimentary-controlled, the waveform depends also on the duty ratio, D, of the lower switch. From an ac perspective, this ripple is then filtered by the input inductor, L, and the input capacitor, C_{in}, determining the switching ripple that propagates to the PV terminals and thus effects the panel output. In order to determine the frequency content in the switching node voltage, the definition of a Fourier series [92], is given in (5.4) with coefficients as in (5.5).

$$v_{sw}(t) = \sum_{n=-\infty}^{\infty} A_n e^{\frac{2\pi n j}{T_{sw}} t} \tag{5.4}$$

$$A_n = \frac{1}{T_{sw}} \int_{-T_{sw}/2}^{T_{sw}/2} v_{sw}(t) e^{-jn\frac{2\pi}{T_{sw}}t} dt \tag{5.5}$$

Specifically in a boost converter, the switch-node voltage can be described piece-wise linearly in the time domain as in (5.6).

$$v_{sw}(t) = \begin{cases} V_{bus} & |t| < \frac{(1-D)T_{sw}}{2} \\ 0 & \frac{(1-D)T_{sw}}{2} < |t| < \frac{T_{sw}}{2} \end{cases} \tag{5.6}$$

This reduces the integral in (5.5) to the form in (5.7).

$$A_n = \frac{V_{bus}}{T_{sw}} \int_{-\frac{(1-D)T_{sw}}{2}}^{\frac{(1-D)T_{sw}}{2}} e^{-jn\frac{2\pi}{T_{sw}}t} dt \tag{5.7}$$

Evaluating the integral with trigonometric substitution leads to the result in (5.8):

$$A_n = \left(\frac{V_{bus}}{\pi n}\right) \sin(n\pi(1-D)) \tag{5.8}$$

Obviously, the dc term must be defined separately (to avoid dividing by zero), and is given in (5.9)

$$A_0 = V_{bus}(1-D) \tag{5.9}$$

Note that the Fourier series is defined over both positive and negative harmonics of T_{sw}, which add constructively reducing the series definition to (5.10):

$$V_{sw}(t) = V_{bus}(1-D) + \sum_{n=1}^{\infty} \frac{2V_{bus}}{n\pi} \sin(n\pi(1-D)) \cos\left(\frac{2\pi n}{T_{sw}} t\right) \tag{5.10}$$

The input inductor and capacitor form an LC-filter between the switch-node and the PV terminal, allowing the magnitude of the ripple at each frequency to be expressed as a simple voltage divider, leading to the result in (5.11).

$$V_{in}(t) = \left(\frac{V_{sw}(t)}{-LC_{in}(2\pi n f_{sw})^2 + 1}\right) \tag{5.11}$$

Combining the definition of the switch-node voltage with the filtering effects of the input inductor and capacitor, the sum of the squares of the harmonic voltages can be written as in (5.12), giving the required input for estimating the MPPT efficiency.

$$\sum {V_{IN}}^2 = \sum_{n=1}^{\infty} \frac{4}{\pi^2 n^2} \frac{{V_{bus}}^2 \sin^2(n\pi(1-D))}{\left(1 - LC_{in}(2\pi n f_{sw})^2\right)^2} \tag{5.12}$$

Many of the variables in (5.12) are not changeable at this phase of the design procedure and are subject to other design parameters previously defined. The only degree of freedom available typically is the sizing of the input capacitor (C_{in}). For the converter in Chapter 1, a plot showing $\sum V_{IN}^2$ versus C_{in} is given in Fig. 5.5. From this plot, for example, it can be determined that 5μF establishes the square of the switching ripple at or below 0.13V^2, or

below one-third of the ripple budget at full power.

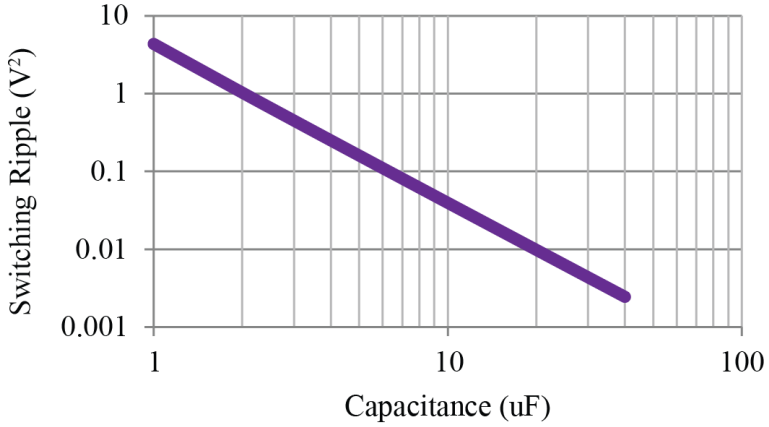

Figure 5.5: Required input capacitance for IBR

If other panel types and sizes are anticipated for the designed micro-converter, requiring that the voltage range be extended, the hybrid-frequency modulation from Chapter 2 can have an impact on the perceived switching ripple. Maintaining the same ripple threshold across the operating range could require additional input capacitance, as shown in Fig. 5.6.

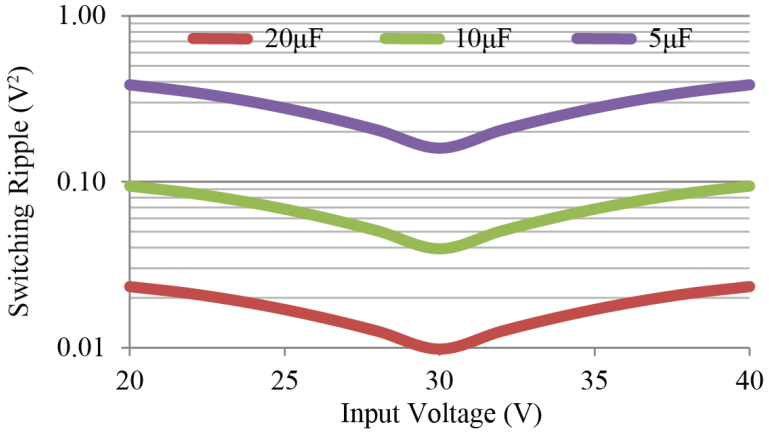

Figure 5.6: Required input capacitance for IBR with HF modulation

5.3 MPPT Ripple Evaluation

MPPT is quite possibly the most discussed and least agreed upon issue in dealing with PV systems and their operation. Techniques range wildly in their approach, complexity, accuracy, and dynamic characteristics. Perhaps the most simplistic of all is constant voltage control [82], which has little or no dynamic issues, but struggles with accuracy, in that the MPP is rarely, if ever, at the voltage (or current) set-point. Another popular option is Ripple Correlation Control (RCC) [93]–[97], which uses a kind of hysteretic non-linear control to determine the operating point. The correlation is based on the inherent switching ripple of the converter, eliminating the need for perturbing the PV voltage. Implementation of this method is complex, however, and highly susceptible to external noise (such as line-frequency ripple).

Though more complex MPPT methods exist, by far the most popular methods are perturbation-based, where one or more of the system variables are intentionally varied so that the localized slope of the PV current-voltage curve may be determined. In this category belong the traditional methods of perturb-and-observe (P&O), incremental conduction (IncCond), as well as their associated variants [98]–[102]. Traditional P&O and IncCond involves altering the duty cycle of the converter or inverter and observing the related change in input (some combination of voltage, current, conductance, or power) and determining the next duty cycle command based on those results. This evaluation is conducted on some predetermined interval, with the magnitude of the step change either permanently fixed or

variable based on the rate of change. Ideally, a variable-step MPPT algorithm selects a step size proportional to the change in power or conductance, and is therefore taking very small steps at or around the MPP (where these incremental changes are also small) and has negligible steady-state ripple. The fixed-step version, however, will settle out to a repeating waveform of fixed-amplitude. The most commonly observed is a three-step waveform, with one step above the MPP, one step at or near the MPP, and one step below the MPP. Though the traditional waveform would resolve to steps in converter duty cycle, for reasons explained in the next section, this control technique can be added to the input voltage control shown in Chapter 2. This results in a steady-state oscillation in PV voltage, rather than converter duty cycle, as shown in Fig. 5.7. Just as the switching ripple effected the PV panel out-

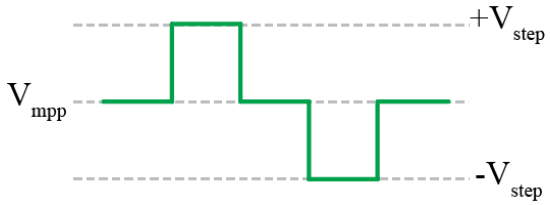

Figure 5.7: MPPT P&O steady-state ripple

put power, this steady-state MPPT ripple also has an impact. This three-level step can be decomposed into two square waves which have opposite sign and a phase difference of 90 degrees. The integral form of the Fourier coefficients for one of the square waves may be written as in (5.13), simplified as in (5.14), and applied to form a time-domain expression as in (5.15).

$$A_n = \frac{1}{2\pi} \int_{-\pi/2}^{\pi/2} V_{step} e^{-jn\theta} d\theta \tag{5.13}$$

$$A_n = \frac{V_{step}}{\pi n} \sin\left(\frac{n\pi}{2}\right) \tag{5.14}$$

$$v_{track}(t) = \sum_{n=-\infty}^{\infty} A_n e^{jn\omega_m t}\left(1 - e^{jn\frac{\pi}{2}}\right) \tag{5.15}$$

Similarly to the result from the previous section, the positive and negative frequency terms add constructively, so v_{track} may be simplified to only positive frequency terms:

$$v_{track}(t) = \sum_{n=1}^{\infty} 2A_n e^{jn\omega_m t}\left(1 - e^{jn\frac{\pi}{2}}\right) \tag{5.16}$$

With some trigonometric simplification, the complex exponential terms simplify to:

$$v_{track}(t) = \sum_{n=1}^{\infty} 2A_n\sqrt{2}\cos\left(n\omega_m t + \frac{\pi}{4}(-1)^{(n-1)/2}\right) \tag{5.17}$$

Because of the form of A_n the even harmonics of v_{track} are identically zero, leaving the final expression:

$$v_{track}(t) = \sum_{n=1,3,5\ldots}^{\infty} \frac{V_{step}2\sqrt{2}}{\pi n} \sin\left(\frac{n\pi}{2}\right)\cos\left(n\omega_m t + \frac{\pi}{4}(-1)^{\frac{(n-1)}{2}}\right) \tag{5.18}$$

For the analysis in the previous sections, we are interested in the summation of the square of each of the harmonic magnitudes:

$$\sum {V_{TRK}}^2 = \sum_{n=1,3,5\ldots}^{\infty} \frac{8}{\pi^2 n^2} {V_{step}}^2 \tag{5.19}$$

This summation can be rewritten to include both odd and even terms (the even terms are zero):

$$\sum {V_{TRK}}^2 = \sum_{n=1}^{\infty} \frac{8}{\pi^2 n^2} {V_{step}}^2 \left(\frac{1-(-1)^n}{2} \right) \tag{5.20}$$

This can be expanded into a difference of two summations:

$$\sum {V_{TRK}}^2 = \frac{4{V_{step}}^2}{\pi^2} \left(\sum_{n=1}^{\infty} \frac{1}{n^2} - \sum_{n=1}^{\infty} \frac{(-1)^n}{n^2} \right) \tag{5.21}$$

The first summation term is a convergent p-series, while the second is a convergent alternating series. These two converge to known values:

$$\sum {V_{TRK}}^2 = \frac{4{V_{step}}^2}{\pi^2} \left(\frac{\pi^2}{6} - \frac{-\pi^2}{12} \right) \tag{5.22}$$

Thus, the series summation converges to a final value of:

$$\sum {V_{TRK}}^2 = {V_{step}}^2 \tag{5.23}$$

This is a simple result, which also has interesting implications. The steady-state power loss related to MPPT ripple is solely dependent on the size of the voltage step required, not the frequency of the step. This places a premium on sensor accuracy and noise immunity, but not on MPPT bandwidth. For the CS6P baseline case, the step size must be limited to 0.36V in order for the MPPT ripple to occupy one-third of the ripple budget.

5.4 Line Frequency Ripple Reduction

The last, but certainly not the least important, of the three primary ripple sources is the double line frequency ripple propagating from the dc-ac inverter. From the utility perspective, the inverter output is considered to be constant if it does not vary from cycle to cycle. However, from the viewpoint of any dc system component, a constant inverter output is anything but. In order to deliver unity power factor, the inverter's output current must increase and decrease completely in phase with the grid voltage. Power being the instantaneous product of grid current and voltage, the inverter delivers full instantaneous power at the positive or negative peak of the grid voltage, and zero power when the grid voltage reaches a zero crossing. Thus, the instantaneous output power from the inverter moves from zero to full power at a rate of twice per line cycle (or 120Hz in US systems). This power ripple produces an energy ripple at the dc link capacitor, which corresponds to a ripple in the dc bus voltage. This ripple, if untreated, can propagate through the dc-dc micro-converter and onto the PV terminals, as shown in Fig. 5.8. Identifying the magnitude of the ripple is a straightforward process as follows. Assume grid current and voltage with

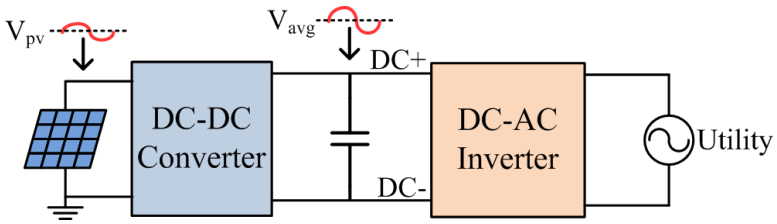

Figure 5.8: Double-line-frequency ripple propagation

an arbitrary current phase angle θ.

$$v_{grid}(t) = V_m \cos(\omega t) \tag{5.24}$$

$$i_{grid}(t) = I_m \cos(\omega t + \phi) \tag{5.25}$$

The power transferred from the dc-bus can be expressed as (5.26).

$$p_{bus}(t) = v_{grid}(t)\, i_{grid}(t) = V_m I_m \cos(\omega t) \cos(\omega t + \phi) \tag{5.26}$$

Which may be resolved into a dc component and a double-line frequency ac component:

$$p_{bus}(t) = \frac{V_m I_m}{2} \cos(\phi) + \frac{V_m I_m}{2} \cos(2\omega t + \phi) \tag{5.27}$$

Note that the magnitude of the double-line component depends only on the apparent power, while the dc component is equivalent to the real-power output only. Considering only the double-line (2ω) frequency portion, the amount of energy in the ripple can be written as in (5.28).

$$\Delta E = \frac{V_m I_m}{2} \int_{\phi/2\omega}^{\frac{\phi+\pi/2}{2\omega}} \cos(2\omega t + \phi)\, dt \tag{5.28}$$

Utilizing a change of variables, the integral can be evaluated as in (5.29), and with the expansion in (5.30), the ripple amplitude (ΔV) can be written as (5.31).

$$\Delta E = \frac{V_m I_m}{4\omega} \left(\sin\left(u\right) du\right)\Big|_0^{\pi/2} = \frac{V_m I_m}{4\omega} = \frac{1}{2} C_b \left({V_{\max}}^2 - {V_{\min}}^2\right) \tag{5.29}$$

$${V_{\max}}^2 - {V_{\min}}^2 = \left(V_{\max} + V_{\min}\right)\left(V_{\max} - V_{\min}\right) = 2 V_{avg} \Delta V \tag{5.30}$$

$$\Delta V = \frac{V_m I_m}{4\omega C_b V_{avg}} \tag{5.31}$$

For analytical purposes, the ripple at the dc-link can be normalized to the average dc voltage to determine a percent ripple ($\%r_{bus}$).

$$\%r_{bus} = \frac{\Delta V}{V_{avg}} = \frac{V_m I_m}{4\omega C_b {V_{avg}}^2} \tag{5.32}$$

From this analysis, the contributing factors to this dc-link ripple quickly stand out. Obviously, as the apparent power ($V_m I_m$) or the modulation index (V_m / V_{avg}) increases, so does the ripple voltage. The inverter has no control over this ripple if a good power factor or low output distortion is desired. The only mechanism to reduce the ripple voltage is to increase the bulk capacitance [103], a method that generally results in lower expected lifetime and higher cost. As long as the inverter can operate successfully with elevated ripple, a high ripple condition is not a problem per se. It only becomes an issue if the ripple is able to propagate to the PV terminals. Preventing this from occurring has been the motivation for some unique research, such as a method for shunting the ripple to a separate ac-link [104],

[105] or adjustments to traditional P&O methods in order to compensate for current variation [106]. However, a much simpler solution to the line-frequency ripple problem may be available. The effect that ac variations in the input supply have on the converter's output (often referred to as audio susceptibility) has been developed and researched for some time [42]. However, as there is an input-to-output relationship for a switch-mode converter, there is also an output-to-input relationship (hereby referred to as grid susceptibility). This issue is often ignored in a point-of-load scenario because the input supply is much less important to the circuit designer than the power quality at the load. As demonstrated in the preceding sections, however, quite the opposite is true for a micro-converter application. Much like audio susceptibility, grid susceptibility of the boost converter (G_{vv}) can be determined from the same approach as outlined in Chapter 2, and is shown in (5.33).

$$G_{vv} = \frac{\hat{v}_{in}}{\hat{v}_{out}} = \left(\frac{1-D}{n}\right) \frac{1}{LC_{in}s^2 + \frac{L}{r_s}s + 1} \tag{5.33}$$

As an aside, at this juncture it is relevant to point out a serious weakness in the duty-cycle based MPPT methods (such as the original P&O or IncCond). By definition, the percent ripple in either one of the voltages (V_{in} or V_{out}) is equal to (5.34).

$$\%r_x = \frac{\hat{v_x}}{V_x} \tag{5.34}$$

To aid in comparison, a metric known as a ripple ratio can be defined as (5.35)

$$r_r = \frac{\%r_{V_{in}}}{\%r_{V_{out}}} \tag{5.35}$$

With traditional MPPT (i.e. limited or low frequency feedback)

$$r_r = \frac{V_{out}}{V_{in}} G_{vv} \tag{5.36}$$

Because the converter dynamics are typically at a much higher frequency that 120Hz, G_{vv} can be approximated:

$$r_r \approx \frac{1-D}{n} = \frac{V_{in}}{V_{out}} \tag{5.37}$$

Thus, with this traditional control technique,

$$r_r = 1 \tag{5.38}$$

Which indicates that there is little or no reduction in the percent ripple at the PV input with these traditional methods, and the dc-dc converter provides little or no benefit in dealing with dc-link ripple. However, using input-voltage control, combined with MPPT techniques provides a way to decrease (improve) the ripple ratio without sacrificing the tracking behavior or artificially increasing the input capacitance. A block diagram demonstrating the control system network is provided in Fig. 5.9. The closed-loop path that includes the compensator gain, H_{comp}, and the duty-to-input plant function (G_{vd}) forms the control system described in

Chapter 2. Variations in the output propagate naturally through the aforementioned output-to-input function (G_{vv}). With the feedback system in place, closed-loop grid susceptibility can be written as (5.39). However, because the denominators (or characteristic polynomials) of G_{vv} and G_{vd} are identical, (5.39) may be re-written as (5.40).

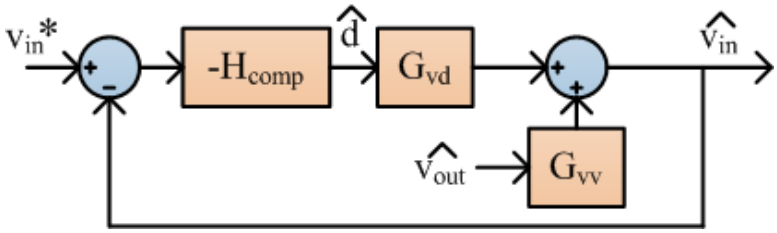

Figure 5.9: Grid susceptibility closed-loop diagram

$$G_{vv-CL} = \frac{\hat{v}_{in}}{\hat{v}_{out}} = \frac{G_{vv}}{1 - G_{vd}H_{comp}} \tag{5.39}$$

$$G_{vv-CL} = \frac{(1-D)}{P(s) + V_{out}H_{comp}} \tag{5.40}$$

Because the converter dynamics, once again, are at a much higher frequency than the double-line frequency, $P(s)$ is unity over the region of interest, reducing the closed-loop G_{vv-CL} to (5.41), with the compensator gain evaluated at the double-line frequency (2ω)

$$G_{vv-CL}\big|_{2\omega} = \frac{(1-D)}{1 + V_{out}H_{comp}\big|_{2\omega}} \tag{5.41}$$

Using the ripple-ratio quantity, the ripple rejection ability of the dc-dc micro-converter can be established:

$$r_r = \frac{1}{|1 + \frac{V_{out}}{n}\left(H_{comp}\big|_{2\omega}\right)|} \tag{5.42}$$

Combining the analysis from this section, the double-line-frequency ripple that reaches the PV terminals can be written as in (5.43). From this expression, it is evident that part of the double-line-frequency ripple depends on the inverter and the other on the micro-converter's controller. If the inverter is designed for a given percent ripple at full-power (Eg. 10%), the required compensator gain at 120Hz can be plotted as a function of irradiance, as shown in Fig. 5.10. In order to occupy one-third of the ripple budget, the compensator gain must be approximately 0.14 (or -17dB) at 120Hz.

$$V_{DLF} = \frac{V_m I_m V_{MPP}}{4\omega C_b {V_{bus}}^2 \left(1 + {V_{bus}}/{\eta} H_{comp}|_{2\omega}\right)} \tag{5.43}$$

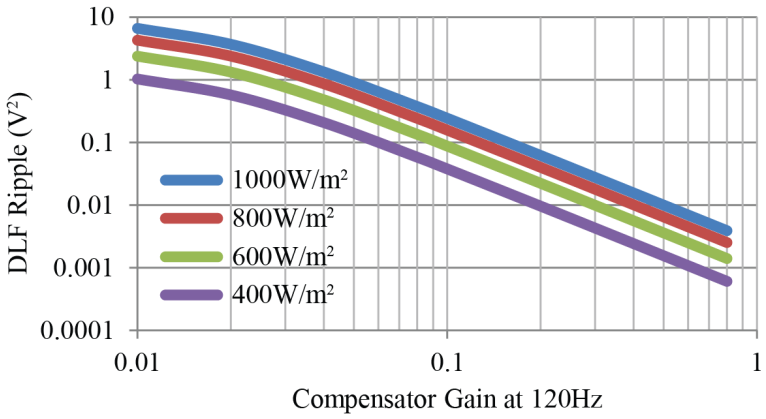

Figure 5.10: Required 120Hz compensator gain with inverter designed for 10% maximum ripple

5.5 Simulation and Experimental Results

With the theoretical analysis put forward, attempting at least a partial verification through simulation is beneficial. Beginning with the line-frequency ripple problem, an example micro-converter and inverter system can be constructed in order to evaluate the line-frequency related behavior. For the micro-converter portion, specifications similar to the previous chapters would be prudent. The inverter, in order to simplify the simulation, may be scaled down in power to be a one-to-one match with the micro-converter. The resulting system specifications are summarized in Table 5.2. Without input voltage control on the micro-converter, the ripple voltage on the dc-link capacitor propagates unrestricted to the PV terminals, as shown in Fig. 5.11. Using input voltage control in lieu of traditional P&O or IncCond allows for a reduction in the PV terminal ripple without increasing the size of the filter capacitors. The example in Fig. 5.12 shows a nearly 10x reduction in converter ripple from the dc-link value. The plots in Figs. 5.11 and 5.12 are normalized to the input or output dc voltage values for ease of comparison. Though the dc-link ripple in the Figs. appears to be entirely at 2ω (120Hz), harmonics of that ripple frequency are also present in the waveform. When the fundamental frequency is rejected by the compensator loop, the higher frequency terms remain in the PV voltage ripple, leading to the slightly distorted waveform in Fig. 5.12. Improvements in inverter control can mitigate the presence of these harmonics without impacting the normal power flow. As discussed in the previous section, the controller gain at 120Hz directly effects the ripple ratio. As the gain increases, the ripple ratio decreases, indicating reduced ripple at the PV terminals. This impact can be shown both

Table 5.2: Ripple Rejection Simulation Data

Element	Value	Element	Value
V_{in}	30V	V_{out}	400V
C_{in}	$10\mu F$	C_{bus}	$20\mu F$
n	6.67	$H_{comp}\|_{2\omega}$	0.144
P_{out}	$250W$	F_{sw}	$60kHz$
Th. DC Bus Ripple	10.1%	Sim. DC Bus Ripple	9.89%
Th. PV Ripple	1.17%	Sim. PV Ripple	1.08%

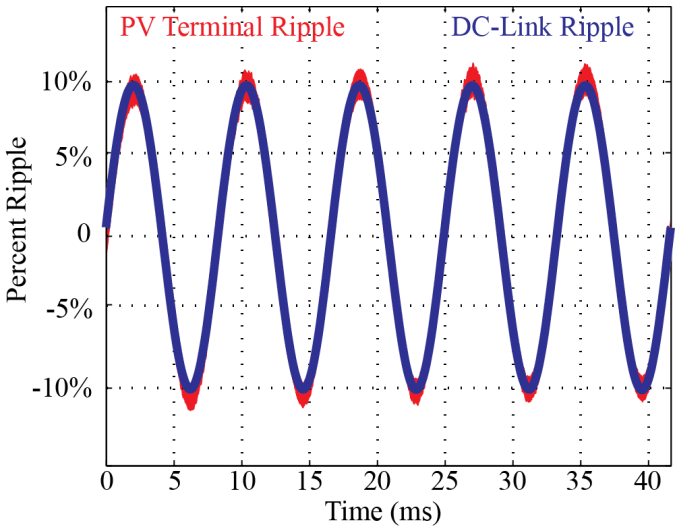

Figure 5.11: PV terminal ripple without input voltage control

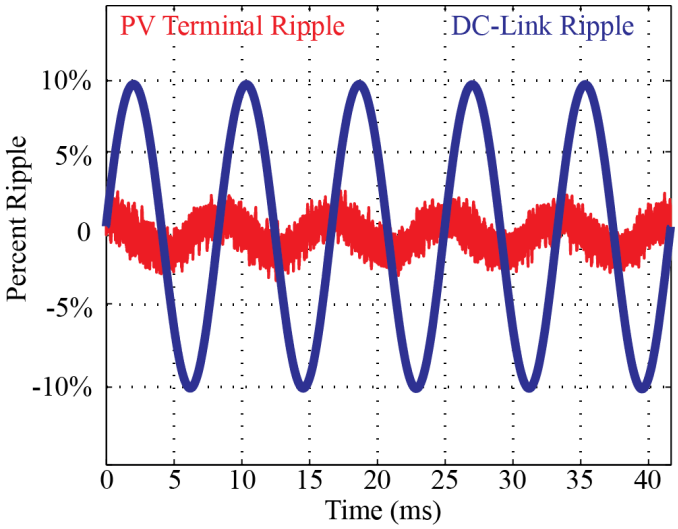

Figure 5.12: PV terminal ripple with input voltage control

analytically (as in the previous section), or through simulation, with excellent agreement evidenced in Fig. 5.13. A unique result was also provided for calculating the cumulative

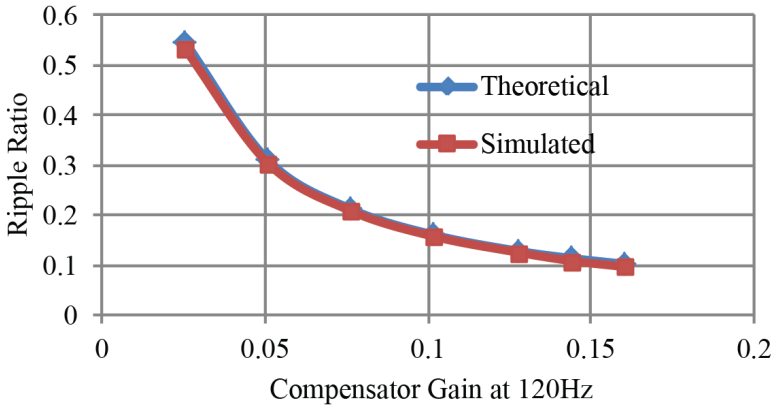

Figure 5.13: Comparison of micro-converter ripple ratio vs. compensator gain

impact of the MPPT steady-state ripple. As stated previously, the sum of the squares of the MPPT ripple harmonics identically add to be equal to the square of the MPPT step size. For a step size of unity, the square of the MPPT harmonic spectrum is given in Fig. 5.14. Regardless of amplitude or frequency, the first through the ninth harmonics account for nearly 96% of the harmonic content in the steady-state MPPT ripple. With the individual

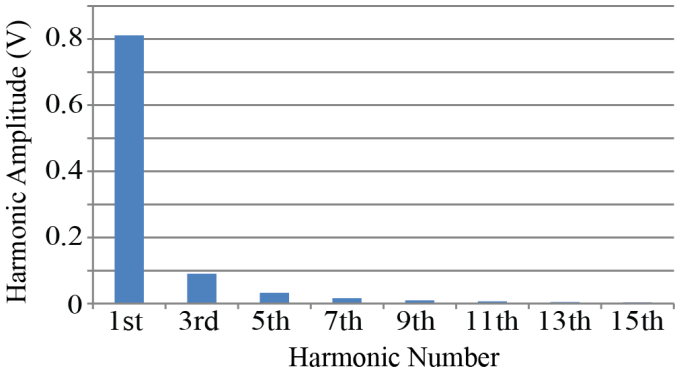

Figure 5.14: Harmonic spectrum of MPPT ripple (step magnitude = 1V)

ripple sources analyzed, it is possible to evaluate the combined effects on the PV model.

Test cases for this is summarized in Table 5.3, with simulation results plotted for $\eta_{MPPT} =$ 99.6% in Figs. 5.15 and 5.16. Figs. 5.17 and 5.18 show the aggregate of the three principle ripple sources with expected MPPT efficiency of 99.9%. The instantaneous power harvested varies significantly, with the average output power being somewhat less than the maximum, and in good correlation with the preceding analysis.

Table 5.3: Aggregate Ripple Simulation Data

Designed η_{MPPT}	**99.9%**	**99.8%**	**99.6%**
Ripple Budget (V^2)	0.2021	0.4042	0.8083
Max. Ripple Per Source (V)	0.2595	0.3670	0.5191
Simulated Power Output (W)	248.10	247.85	247.60
Simulated η_{MPPT}	0.99905	0.99804	0.99604

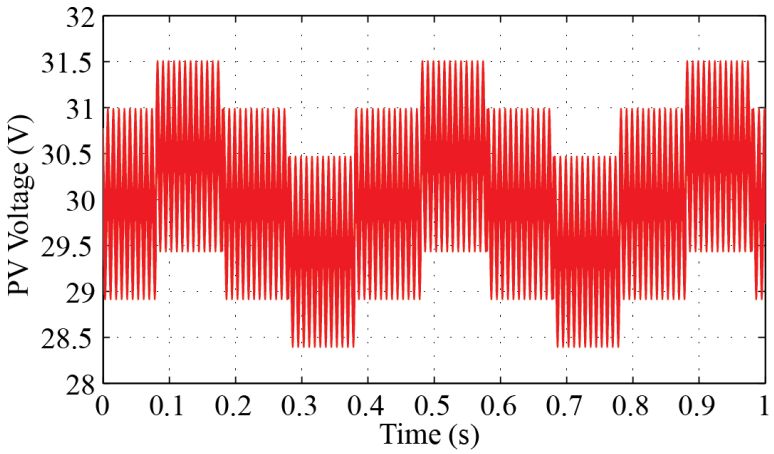

Figure 5.15: Simulated PV voltage ripple at $\eta_{MPPT} = 99.6\%$

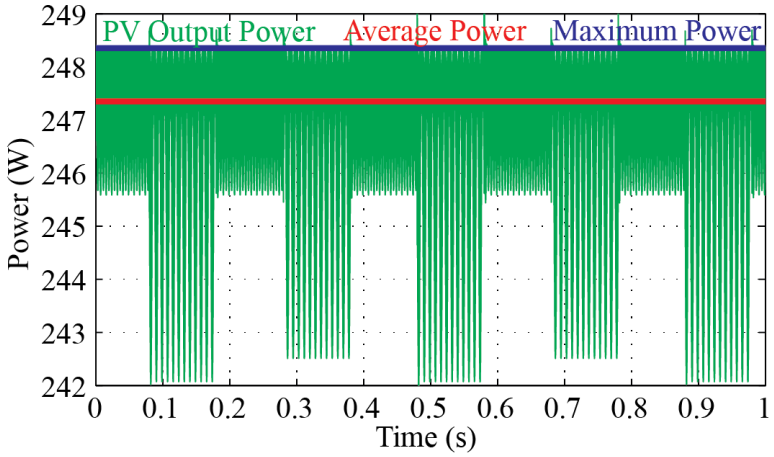

Figure 5.16: Simulated PV power ripple at $\eta_{MPPT} = 99.6\%$

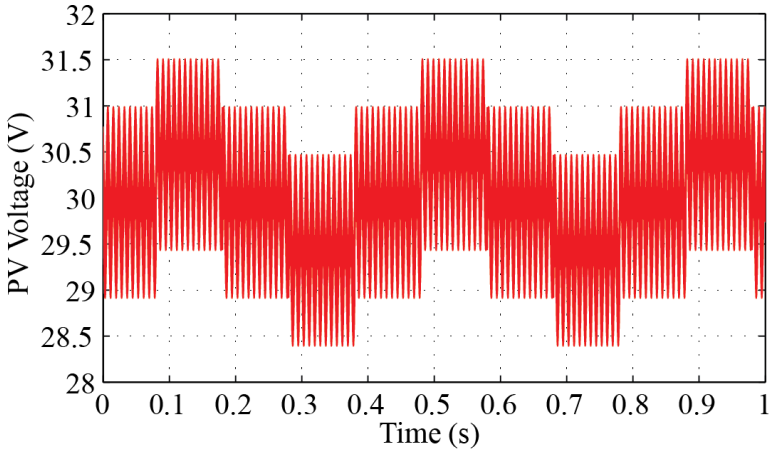

Figure 5.17: Simulated PV voltage ripple at $\eta_{MPPT} = 99.9\%$

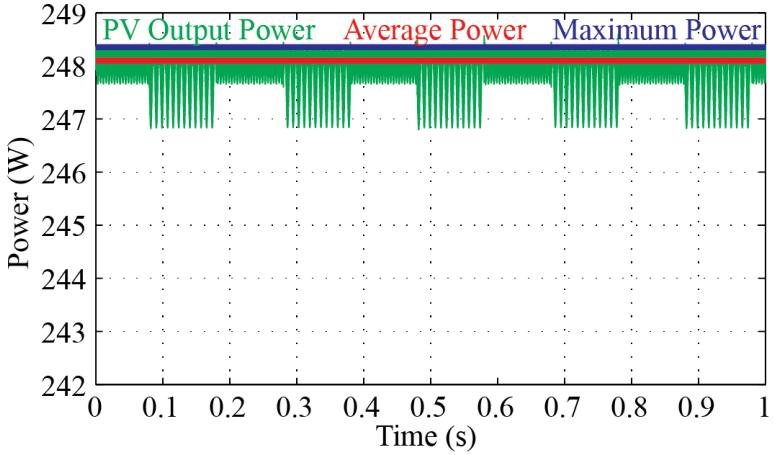

Figure 5.18: Simulated PV power ripple at $\eta_{MPPT} = 99.9\%$

The preceding simulation results may also be verified through experiment. Utilizing an small inverter circuit to process the extracted power, the ripple rejection and aggregate ripple conditions were investigated. The experimental ripple rejection ratio is compared against the theoretical analysis in Fig. 5.19, along with experimental waveforms showing the input ripple without input voltage control (Fig 5.20) and with input voltage control (Fig 5.21).

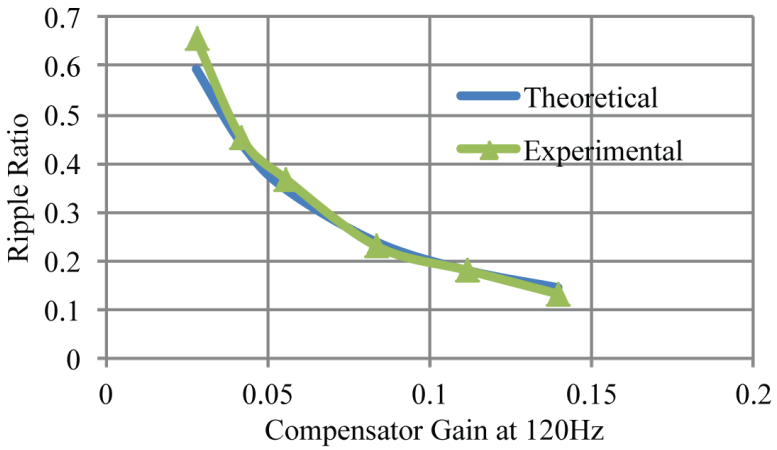

Figure 5.19: Experimental ripple ratio compared to theoretical analysis

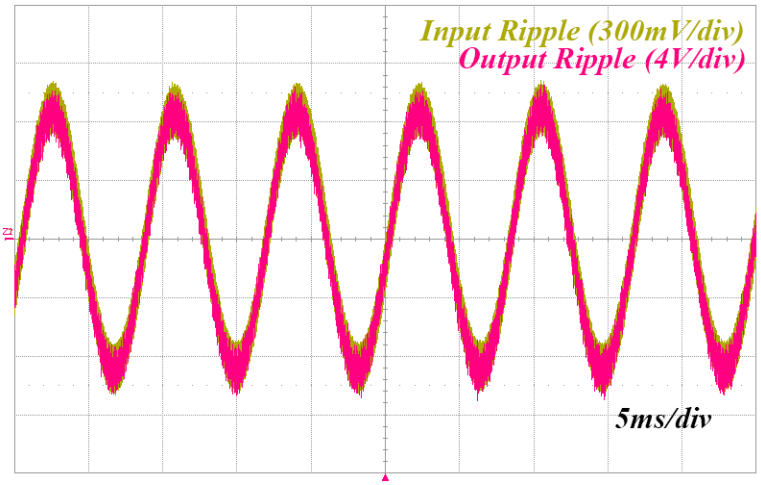

Figure 5.20: Experimental ripple without input voltage control

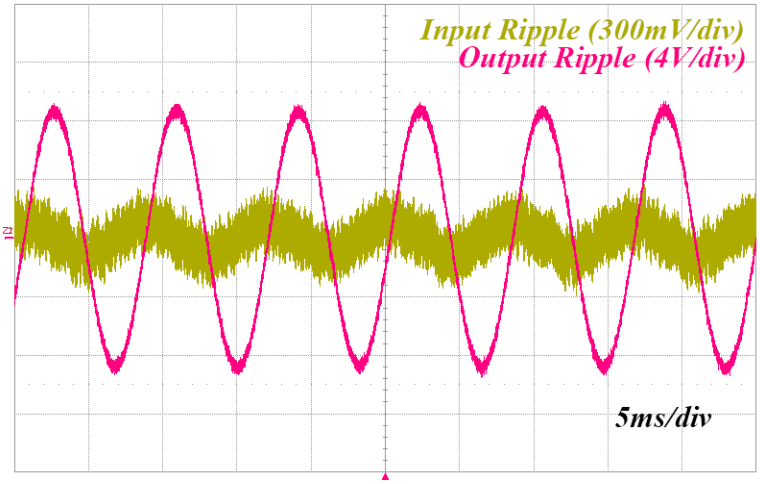

Figure 5.21: Experimental ripple with input voltage control ($H_{comp} = 0.1273$)

Likewise, the degradation of the power output with respect to voltage ripple can also be investigated experimentally. A test case for the inverter system operating with the Canadian Solar CS6P is summarized in Table 5.4, with ripple voltage and power waveforms shown in Figs. 5.22 and 5.23. The results suffer from a reasonable amount of error, due to very slight variations in the MPP voltage and available power even within a small sampling window on an extremely clear day.

Table 5.4: Aggregate Ripple Experimental Data

Element	**Value**	**Element**	**Value**
Cell Temp.	35°C	Sw. Ripple	0.3V
Alpha	-0.0821	MPPT Step	0.35V
Beta	4.426	DLF Ripple	0.2V
Max. Power	248.8W	Avg. Power	248.3W
Th. η_{MPPT}	99.86%	Exp. η_{MPPT}	99.80%

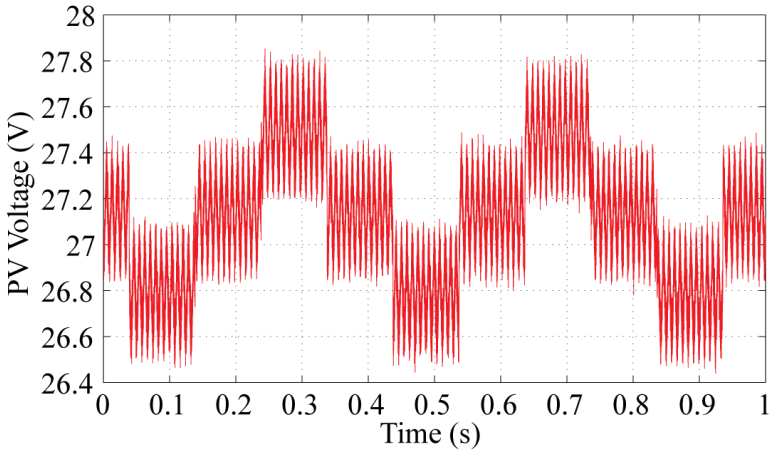

Figure 5.22: Aggregate experimental voltage ripple

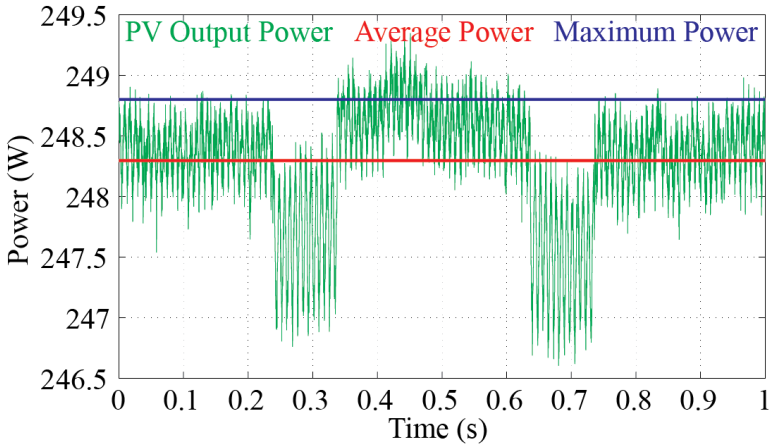

Figure 5.23: Aggregate experimental power ripple

5.6 Summary

Though several authors have attempted to evaluate the impact of disturbing ripple on PV performance, the extension to full-scale systems has been somewhat tenuous. This chapter established a link between PV modeling and PCS design, which allowed for appropriate system development. The converter's MPPT efficiency was defined as the amount of energy harvested from the PV panel as compared to the maximum power available at

that point. This established a ripple "budget" for steady-state disturbances. The three forms of PV ripple—PCS switching, MPPT steady-state, and double line-frequency ripple—were evaluated against the PV model. Manipulation of the ripple magnitudes was possible through increasing the input capacitance to prevent switching noise, selecting appropriate sensing and conditioning to reduce MPPT step size, and adding input voltage control with high-compensator gain to reject double-line-frequency ripple. Rejection of the double-line frequency ripple, as well as the general degradation of PV output power were demonstrated through both simulation and experiment. The end result of this section was a unified analysis of PV ripple, suitable for the converter design process, along with suggestions for improving the MPPT efficiency of the micro-converter system.

Chapter 6

The ZVS Integrated Boost Resonant Converter

The previous chapters have worked along the four major focus areas outlined in the introduction: topology, modulation/control, transient protection, and steady-state optimization. The vertically-integrated approach allowed insight into the proper structure of design and allowed informed decision-making under each category. As this procedure has come full circle, the original decisions that defined this approach can be revisited. If improvements can be made to advance the lowest level component, this vertical process can begin again. With forward progress, this circular momentum forms a helix of continuous design improvement. The aim of this chapter is to demonstrate this sort of process through advancements in topology, allowing the other design categories to adjust accordingly.

As discussed earlier, efficiency of the PCS equipment is a key motivator in new designs. However, both size and cost are also major factors, which often run in opposition to higher efficiency. At the heart of this conflict lies the converter switching frequency. As the switching frequency is increased, the required value of passive components, such as the input inductor, resonant capacitors, and the isolation transformer, can be significantly reduced. This generally results in large size and cost savings in both components and packaging material. However, with this frequency increase, the main device switching loss, a major component of the recorded loss in Chapter 2, also increases. This reduces the overall efficiency as a result. Therefore, a successful design of an IBR-based micro-converter hinges upon a balancing of size, weight, and cost in the selection of an appropriate switching frequency.

This balancing act, however, would change significantly if the impact of the switching frequency on the overall efficiency were lessened, indicative of a so-called soft-switching condition. In the case of a MOSFET switch, soft-switching is typically understood as the removal of the device blocking voltage (and resulting output charge) prior to device turn-on, a process known as zero-voltage-switching (ZVS) [107]–[109]. ZVS can be considered as the opposing condition to zero-current-switching (ZCS) which typically occurs at the device turn-off event. In a modern power MOSFET, the turn-on process often results in much more loss than the turn-off scenario, making ZVS (as opposed to ZCS) a highly desirable operating characteristic.

Achieving ZVS is one of the most often discussed topics in modern power electronics,

with a plethora of schemes, circuits, and systems in place to promote the condition. There is at least one common characteristic for all such methods, though: the need to generate a current through the main switching device that is in the opposing direction to the desired load current. This is a "reverse" current that can sweep the charge from the main device junction capacitance prior to the devices turn-on event. Rather than adding more circuit components at the outset, one of the original methods for generating ZVS in a synchronous converter (employing two active switches in lieu of a switch-diode combination) is to increase the principal inductor current ripple such that the input (or output) current swings both positive and negative (forward and reverse) in one switching cycle. Note that this condition is only achievable when an active switch is in both positions, as a traditional power diode will not allow the necessary reverse current for ZVS. At a given switching frequency, this high-ripple condition is achieved simply by reducing the value of the input inductance below a critical value.

In the case of the IBR, this approach is directly applicable. Two active switches are already required for proper resonant operation; thus the only requirement is the reduction of the input inductance. Unfortunately, there is a major issue with this approach. The high current ripple, without impractically increased input capacitance, results in severe input voltage ripple at the converter switching frequency. From the analysis in the previous chapter (Chapter 5), increases in this switching ripple would negatively impact the overall energy harvesting (and potentially the converter lifetime as well). Reducing the input ripple with this type of ZVS approach is a long-standing issue with a common solution: interleaving

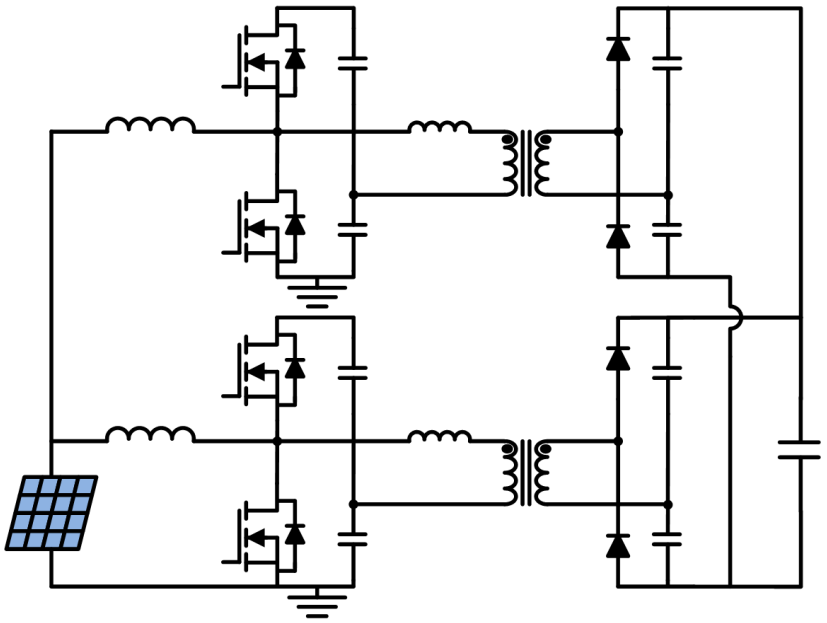

Figure 6.1: An interleaved IBR

[110]–[112]. Adding one or more additional phases, or interleaved inputs, to a PCS allows the overall input ripple to be significantly reduced [113]. Rather than duplicate the entire converter, shown in Fig. 6.1, and following similar lines as in [114], the original procedure in Chapter 2 can be revisited. The IBR, by definition, is the integration of a single boost converter with a DCM series-resonant isolation stage. The high-ripple requirement for ZVS, however, is only an issue for the boost converter portion, and doesnt significantly impact any design for the resonant stage. Thus, the need for interleaving applies only to the boost converter, allowing one resonant stage to serve multiple input phases.

By connecting the isolation transformer between the two switching nodes (one from either of two input stages), an ac voltage can be applied across the transformer terminals, which can then transfer energy to the output. Also, because the capacitor midpoints are unused, the upper and lower primary-side capacitors can be combined, leading to the final

circuit, the IBR-Z, shown in Fig. 6.2. This circuit allows for the desired ZVS approach to be implemented, providing soft-switching for all of the primary-side active devices with only the addition of two MOSFET switches and an extra input inductor. Due to the soft-switching behavior, the switching frequency can be increased with minimal penalty (from 70kHz to 175kHz). This allows for a 60% reduction in ferrite volume, producing a significant decrease in both size and cost with a slight increase in converter efficiency. With this change in

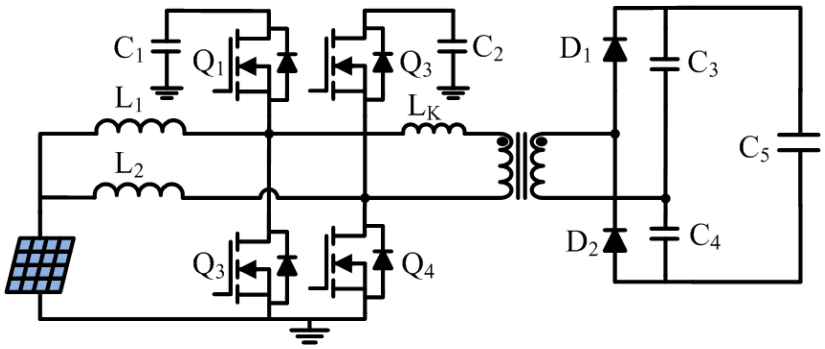

Figure 6.2: IBR-Z circuit diagram

circuit topology comes related adjustments in approach to the remaining design categories. The goal of this chapter is to not only introduce the initial design adjustments, but also to demonstrate the validity of the vertical process experimentally in the proceeding sections.

6.1 Topology

Though the fundamental operation of the IBR-Z is similar to the original IBR, the exact operation is slightly altered. The synchronous boost converters are modulated 180 degrees out-of-phase and each produce an intermediate (or bus) voltage equal to (6.1) across

both C_1 and C_2.

$$\frac{V_{out}}{V_{in}} = \frac{1}{1-D} \tag{6.1}$$

This is equivalent to the standard steady-state voltage gain for a CCM boost converter [42]. The DCM resonant stage creates a voltage mirror, in which C_3 and C_4 reflect the voltage across C_1 and C_2, respectively, by the transformer turns raio, n. (This effect is identical to the original IBR.) In the IBR, the sum of the voltage across C_1 and C_2 is equal to the intermediate bus voltage. This produces a voltage gain of (6.2), allowing the turns ratio to be one-half the required value of the original IBR.

$$\frac{V_{out}}{V_{in}} = \frac{2n}{1-D} \tag{6.2}$$

The operating modes for the IBR-Z are shown graphically in Fig. 6.3, following the timing diagram in Fig. 6.4.

Mode 1 $(t_0 - t_1)$**:**

With both upper devices (Q_1 and Q_2) on, the current through the input inductors decreases linearly, however, the current in L_2 reverses and begins flowing back into the source (or the input capacitor) at a point close to t_1. Because both C_1 and C_2 have approximately equal voltage, there is zero applied voltage across the transformer, leaving the resonant stage inactive during this interval.

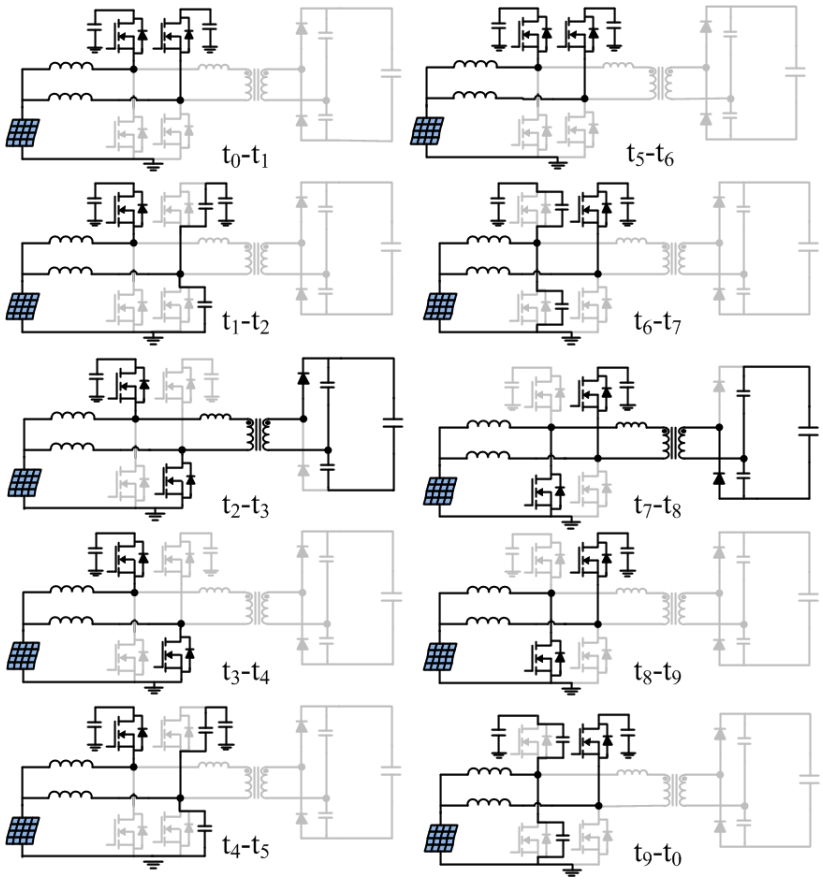

Figure 6.3: IBR-Z converter operating modes

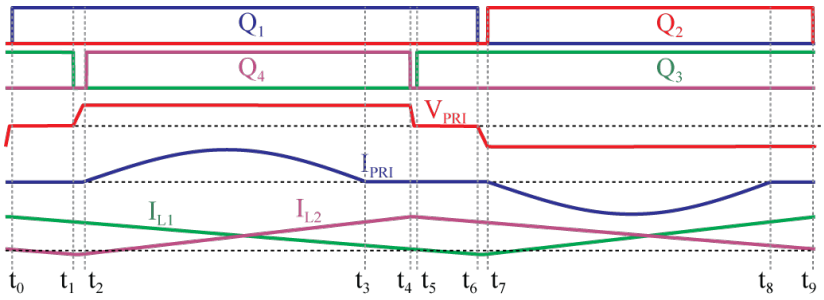

Figure 6.4: IBR-Z timing diagram

Mode 2 $(t_1 - t_2)$**:**

At time t_1, the gate voltage is removed from Q_3, turning the main channel of the device off. The current, however, continues flowing through he junction capacitance,

removing the charge stored in the C_{oss} of Q_4 and replacing it in the C_{oss} of Q_3. This process continues until the voltage across Q_3 is clamped to C_2. While this takes place, the reverse energy stored in L_2 is depleted, reducing the inductor current to zero. Once the voltage across Q_4 drops to zero (an event that occurs simultaneously with the clamping of the voltage across Q_3 at t_2), Q_4 may be turned on under ZVS.

Mode 3 $(t_2 - t_3)$**:**

With Q_1 and Q_4 now on, the bus voltage across C_1 is directly applied across the transformer primary. The leakage inductance, L_K, resonates with the secondary-side capacitors (C_3 and C_4), transferring energy to the output through D_1. Once the transformer current resonates back to zero, D_1 prevents any further resonance, ending Mode 3. The length of Mode 3 is equal to the resonant period length, given by (6.3).

$$T_{res1} = \pi\sqrt{\frac{L_K C_1 n^2 (C_3 + C_4)}{C_1 + n^2(C_3 + C4)}} \tag{6.3}$$

Also during this interval, the input inductor currents are flowing from the source toward the bus capacitors, however, the current in L_1 is decreasing while the current in L_2 is now increasing.

Mode 4 $(t_3 - t_4)$**:**

If the overlap of the switches Q_1 and Q_4 don't match the resonant period exactly, this interval arises as a result. The resonant action is completed by t_3, leaving the voltage applied at the transformer primary with zero current flowing. This area is undesirable,

as it results in increased conduction and transformer core loss.

Mode 5 $(t_4 - t_5)$**:**

At time t_4, the gate signal is now removed from Q_4. The current, however, still flows from the input, but now it flows into C_2, discharging the C_{oss} of Q_3 while charging the C_{oss} of Q_4. The voltage across Q_4 is clamped at t_5, allowing Q_3 to turn on under ZVS. Because the magnitude of the current is much larger at the positvie peak than at the negative peak, this process can be much faster for Q_3 than it was for Q_4.

Mode 6 $(t_5 - t_6)$**:**

Q_1 and Q_3 overlap agian here, creating a similar effect to that of Mode 1. This time, the inductor currents are flowing, with I_{L1} decreasing below zero (reversing direction) near t_4.

Mode 7 $(t_6 - t_7)$**:**

A mirror of Mode 2. The voltage across Q_2 reaches zero by the end of the interval, allowing a ZVS transition.

Mode 8 $(t_7 - t_8)$**:**

The opposite of Mode 3, with the resonant current delivered from C_2, through the output diode D_2, with L_K, C_3 and C_4 forming the resonant tank. The length of this interval is simply:

$$T_{res2} = \pi \sqrt{\frac{L_K C_2 n^2 (C_3 + C_4)}{C_2 + n^2 (C_3 + C4)}} \tag{6.4}$$

Mode 9 $(t_8 - t_9)$**:**

A mirror of Mode 4, this time with I_{L1} increasing and I_{L2} decreasing.

Mode 10 $(t_9 - t_0)$**:**

The gate signal is removed from Q_2 and the current in L_1 forces the resonant charge and discharge of Q_2 and Q_1 respectively, allowing Q_1 to turn on under ZVS and the system return to the initial state.

6.2 Loss Analysis

Investigating the slight variation in the resonant period lengths (T_{res1} and T_{res2}) between Chapter 2 and the previous section reveals an interesting piece of information. Because the dc path from the input to the transformer no longer includes either of the low-side capacitors, the resonant periods can be of equal length so long as C_1 and C_2 have equal value. Thus, a simplified version, mostly, of the design procedure in Chapter 2 can be used for the IBR-Z, with the following qualifications.

1. As noted previously, the applied voltage to the transformer primary is doubled, so the turns ratio must be halved in order to compensate.

2. The resonant stage currents (transformer, output diodes, and secondary-side capacitors) may be calculated with $T_{res1} = T_{res2} = T_{res}$.

3. Rather than designing for a fixed inductor current ripple, the input inductor should be

designed such that L_1 and L_2 solve the following simultaneous expressions, (6.5) and (6.6).

$$Li_{pk,-}^2 > 2C_{oss}V_{bus}^2 \tag{6.5}$$

$$i_{pk,-} = \frac{P_{out}}{2V_{in}} - \frac{DT_{sw}V_{in}}{2L} \tag{6.6}$$

4. The RMS currents flowing in the primary-side capacitors, due to their new configuration and high PWM ripple, can be written as (6.7).

$$I_{C,RMS} = \sqrt{\begin{array}{l}(1-D)\left({i_{pk,L}}^2 - \frac{v_{in}D}{L}i_{pk,L}T_{sw} + \frac{{v_{in}}^2}{3L^2}D^2{T_{sw}}^2\right) \\ + \frac{n\pi P_{out}}{2V_{out}}\left(\frac{\pi n P_{out}T_{sw}}{4V_{out}T_{res}} + \frac{2v_{in}T_{res}}{\pi L}\left(\frac{D}{1-D}\right) - \frac{4i_{pk,L}}{\pi}\right)\end{array}} \tag{6.7}$$

5. The RMS currents in the upper MOSFETs (Q_1 and Q_3) are identical to the primary-side capacitor currents. The lower device RMS currents (I_{Q2} and I_{Q4}) can be written as in (6.8)

$$I_{Q,Lower} = \sqrt{\begin{array}{l}{i_{L,pk}}^2 D - i_{L,pk}\frac{V_{in}}{L}\left(D^2T_{sw}\right) + \frac{{V_{in}}^2}{3L^2}D(DT_{sw})^2 \\ + \left(\frac{nP_{out}}{V_{out}}\right)\left(\frac{\pi^2 n P_{out}T_{sw}}{8V_{out}T_{res}} + 2i_{L,pk} - \frac{2V_{in}DT_{sw}}{L} + \frac{V_{in}T_{res}}{L}\right)\end{array}} \tag{6.8}$$

6. Device turn-on loss and capacitive switching loss are zero, by the definition of ZVS. Upper and lower device turn-off loss follows the form introduced in Chapter 2.

7. The transformer volt-second calculation must be altered, because the primary voltage

waveform now includes increased peak voltage but shortened interval of application (see Fig. 6.4.) The volt-second product at the transformer can be written as in (6.9)

$$VS_{peak} = \frac{V_{in}T_{sw}}{1-D}\left(\frac{1-|D-0.5|}{2}\right), [V \cdot s] \tag{6.9}$$

Because the current ripple in the input inductors (and thus the corresponding ac flux density in their respective cores) is much greater than in the IBR, core loss in the inductor must be considered also [63].

For a prototype IBR-Z with a power rating of 250W, critical values of passive components are provided in Table 6.1 and semiconductors in Table 6.2. A theoretical loss breakdown at 75% power rating (187.5W) is provided in Fig. 6.5.

Table 6.1: Passive Component Data for 250W IBR-Z Prototype

Element	**Value**
L_1, L_2	$8\mu H$
C_1, C_2	$10\mu F$
C_3, C_4	$22nF$
n_{pri}	9 turns
n_{sec}	30 turns

Table 6.2: Semiconductor Data for 250W Prototype

Element	**Value**
Q_1, Q_3	Infineon IPB049NE7N3
Q_2, Q_4	Infineon IPB031NE7N3
D_1, D_2	NXP BYV29-500

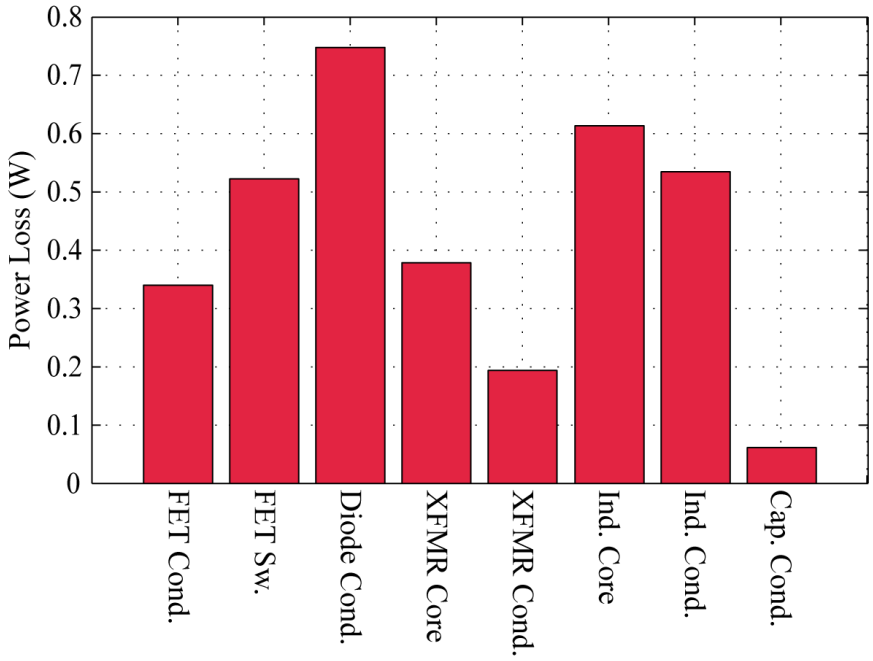

Figure 6.5: IBR-Z loss breakdown (30V input / 75% power)

6.3 Modulation

Judging from Fig. 6.4, the issue of switching period utilization carries over from the original IBR. In Chapter 3, the desire to optimize the converter efficiency at nominal input and to lessen the dependence of the efficiency on the operating range was expressed. Because the resonant conduction occurs only when the corner pairs of switches overlap, the situation is slightly more complicated than the two-switch case (as in the IBR). However, if the two phases are properly synchronized, this amounts to the same limitations on D and $(1 - D)$ that were described previously. The product of the minimum of D or $(1 - D)$ and the switching period T_{sw} must be greater than the established resonant period. Therefore, the Hybrid-Frequency modulation scheme still applies in the IBR-Z.

There is another wrinkle to consider in this decision-making process: the ZVS condition. As the operating frequency is increased, the amount of energy available for the ZVS process decreases as a result. Also, as the input power level (and thus the average current) increases, the ZVS energy decreases. Once either of these two conditions causes the energy in the input inductor to be less than the MOSFET C_{oss} energy, the ZVS condition is lost.

In general, violating the ZCS condition is a poor idea. The additional MOSFET turn-off loss and especially the diode reverse-recovery loss causes a sizeable deviation in the operating efficiency. The lone exception to this occurs when the current transient induced by the output diode junction capacitance is a significant portion of the resonant current waveform (typically restricted to very light load). This shortens the effective resonant period length and allows the violation of the typical ZCS criterion without penalty. However, the benefits derived from increasing the switching frequency in this instance were minimal due to the associated increase in gate drive loss.

If the limitations imposed by the ZCS criteria must be obeyed, the only design criteria available to manipulate is the input inductance. In general, decreasing the input inductance increased the circulating energy, allowing for ZVS at lower input voltages and higher power levels. The appropriate value for the input inductance, however, is subject to the greater design criteria. As discussed in Chapter 2, CEC efficiency places the greatest emphasis on nominal input voltage and 75% power. From the expressions introduced in the design procedure, an expression providing the minimum switching period required for ZVS is given in (6.10) resulting in a summary plot in Fig. 6.6. As this is a function of several variables, the

requirements for three critical power levels are plotted alongside the minimum requirement for ZCS. The switching period lengths required for ZVS vary with input inductance, so this plot demonstrates the variance over input with a fixed inductance. In order to optimize the design for the CEC case, the ZCS curve should intersect the ZVS curve for 75% power at the 50% duty cycle (or nominal input) point. This establishes the most critical operating point in the evaluation guidelines as the point with lowest circulating energy, lowest core loss, ZVS, ZCS, and optimized switching period utilization, leading to the highest efficiency that is achievable at that operating point.

$$T_{sw} = \frac{2L}{DV_{in}} \left(\frac{P_{in}}{V_{in}} + V_{bus} \sqrt{\frac{2C_{oss}}{L}} \right) \tag{6.10}$$

As shown in the above figure (Fig. 6.6), placing the optimized point at the nominal input

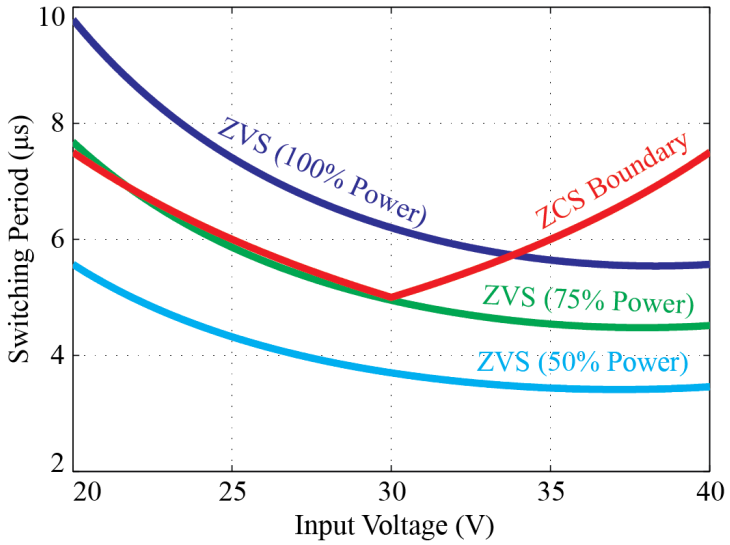

Figure 6.6: IBR-Z ZVS and ZCS boundaries

voltage has some drawbacks. When the converter is at nominal input, it loses ZVS above 75%

power, resulting in an associated decrease in efficiency. However, because the CEC weighting factor on full-load efficiency is only 5% of the total score, this is not a significant impact on the reported efficiency. Because the shape of the ZVS and ZCS curves follow a similar trajectory at voltages less than the nominal input, ZVS can be maintained at 75% power for nearly any input voltage, though full-power ZVS is only achieved near the upper bound on the input range (around 35V). At low line the increased switching frequency (relative to the ZVS requirement) and its associated rms current reduction counteracts the added switching loss. At the high end of the input range, ZVS can be maintained across the power range, although the rms current is significantly increased.

6.4 CTL Soft-Start

As discussed in Chapter 4, the first step to designing an appropriate soft-start technique is to determine the initial (before switching begins) and the equilibrium (steady-state) conditions that are unique to the circuit topology. In the original IBR, because one of the low-side capacitors was included in the dc loop, that capacitor charged up to the input voltage initially, while the upper capacitor had zero voltage across it. In the IBR-Z, two independent (at least initially) dc loops are formed, each including one of the low-side capacitors. This results in an initial voltage of V_{in} on both capacitors, as shown in Fig. 6.7. Note that the isolation transformer prevents any initial secondary voltage in either the IBR (Fig. 4.4) or the IBR-Z. The equilibrium conditions in the IBR-Z are shown in Fig. 6.8.

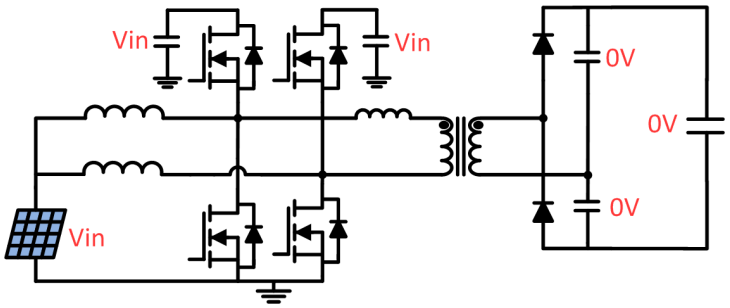

Figure 6.7: IBR-Z initial conditions

The secondary-side capacitors mirror the voltages across the primary-side capacitors, as in the original IBR. Unfortunately, this leaves the IBR-Z with the same startup issues as the original IBR, except with two low-side capacitors with initial voltage, rather than just one. Another issue to consider is the volt-second balance of the transformer during start-up. Un-

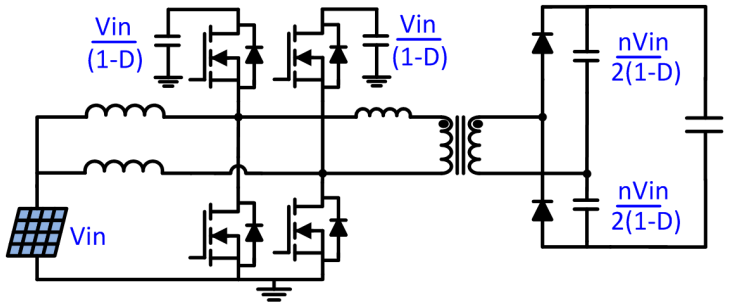

Figure 6.8: IBR-Z equilibrium conditions

like the circuit in [115], the IBR-Z is capable of maintaining volt-second balance regardless of any duty cycle mismatch on the switching legs. Proof of this can be demonstrated by considering the two fundamental cases, one with the sum of the two duty cycles (D_1 and D_2) greater than 1, and the other with a sum less than 1. With the large duty ratios (sum greater than 1), there is a period of time in which the transformer primary voltage is equal to V_{C1}, another in which it is equal to V_{C2}, while the last interval has an applied voltage of zero, in which the lower devices (Q_2 and Q_4) overlap. From the basic boost converter

voltage gain, a voltage balance expression for the transformer primary may be written:

$$\frac{V_{in}T_{sw}}{(1-D_1)}(1-D_1) - \frac{V_{in}T_{sw}}{(1-D_2)}(1-D_2) + 0\cdot(D_1+D_2-1) \tag{6.11}$$

which is identically zero for all cases in which $1 < D_1 + D_2 < 2$.

The second case to consider is when the duty cycles are less than 1 when they are added together. Instead of the lower switches overlapping, now the upper devices overlap (Q_1 and Q_3). During this interval, the difference between V_{C1} and V_{C2} is applied to the transformer, rather than zero volts, leading to a balance expression:

$$V_{in}T_{sw}\left(\frac{D_2}{1-D_1}\right) - V_{in}T_{sw}\left(\frac{D_1}{1-D_2}\right) + V_{in}T_{sw}\left(\frac{1}{1-D_1} - \frac{1}{1-D_2}\right)(1-D_1-D_2) \tag{6.12}$$

With some algebraic reduction, the above expression can also be shown to be identically zero for all duty cycles D_1 and D_2 on the interval $0 < D_1 + D_2 < 1$. These two cases together demonstrate that D_1 and D_2 may be controlled independently during start-up at any operating point, without fear of jeopardizing the transformer.

Finally, from the earlier discussion of operating modes, it is clear that the output, or resonant, stage is only active when the corner pairs of switches are on, specifically modes 3 and 8. By limiting the on-time of the lower devices, the relative lengths of Mode 3 and Mode 8 are also limited (Modes 4 and 9 do not exist if the resonant periods are not allowed to complete). This allows both the intermediate bus voltage and the output current to

be effectively limited by simply controlling the lower switches, similar to the methods in Chapter 4. Thus, with two independent CTL systems, the startup current in the IBR-Z may be controlled adequately.

6.5 Switching Ripple in the IBR-Z

From the static power loss analysis in the previous chapter, it was shown that the power loss from both the MPPT ripple and the double-line frequency ripple depended not on the converter dynamics, but rather MPPT step size and controller bandwidth respectively. Therefore, the transition to the IBR-Z from the original IBR impacts only the switching ripple, not the other components of the static power loss. By augmenting the methods in Chapter 5 with an appropriate analysis of the IBR-Z switching ripple, estimation of the static power loss can be extended to this topology as well.

In the IBR, a single switching node was identified (between Q_1 and Q_2), while in the IBR-Z there are two (between Q_1 and Q_2 as well as Q_3 and Q_4). Fourier series definitions for both switch node voltages are provided in (6.13) and (6.14) showing the only difference is the addition of a phase delay of $n\pi$ to the lagging leg voltage equation (6.14). Assuming that L_1 and L_2 are equal (represented by L), the input ripple may be written as in (6.15).

$$V_{sw1}(t) = V_{bus}(1-D) + \sum_{n=1}^{\infty} \frac{2V_{bus}}{n\pi} \sin(n\pi(1-D)) \cos\left(\frac{2\pi n}{T_{sw}} t\right) \tag{6.13}$$

$$V_{sw2}(t) = V_{bus}(1-D) + \sum_{n=1}^{\infty} \frac{2V_{bus}}{n\pi} \sin(n\pi(1-D)) \cos\left(\frac{2\pi n}{T_{sw}} t + n\pi\right) \tag{6.14}$$

$$V_{in}(t) = V_{IN} + \sum_{n=1}^{\infty} \left(\frac{\frac{2V_{bus}}{n\pi} \sin(n\pi(1-D)) \left[\cos\left(\frac{2\pi n}{T_{sw}} t\right) + \cos\left(\frac{2\pi n}{T_{sw}} t + n\pi\right)\right]}{-LC_{in}(2\pi n f_s)^2 + 1} \right) \tag{6.15}$$

It is readily apparent from the two cosine terms in (6.15) that:

1. Odd harmonics are effectively canceled out.

   $(\cos x + \cos(x+\pi) = 0)$

2. Even harmonics are effectively doubled.

   $(\cos x + \cos(x+2\pi) = 2\cos x)$

The resulting Fourier series may be re-written as (6.16). Because the odd harmonic terms are now zero, the voltage ripple at the nominal input ($D = 0.5$) is also identically zero. As the duty cycle moves further away from the nominal point, the ripple increases from there, as shown in the simulation results Figs. 6.9 and 6.10.

$$\sum {V_{in}}^2 = \sum_{n=2,4,6\ldots}^{\infty} \frac{4{V_{bus}}^2 \sin^2(n\pi(1-D))}{\left(1 - LC_{in}(2\pi n f_{sw})^2\right)^2} \tag{6.16}$$

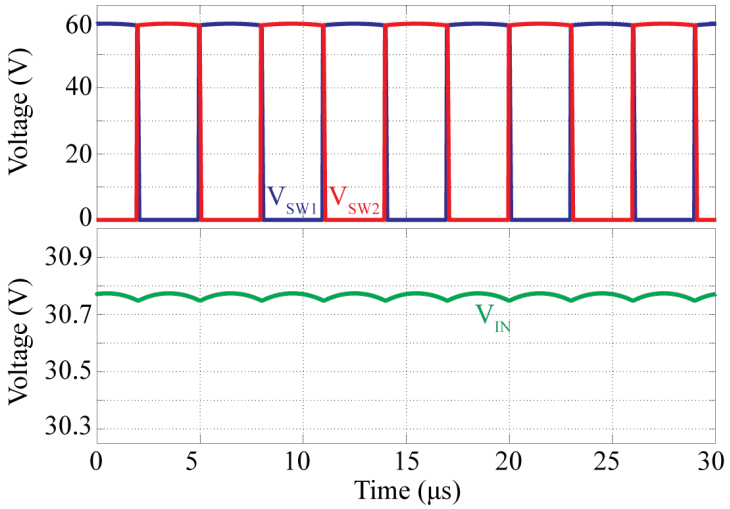

Figure 6.9: IBR-Z input ripple simulation (30V input)

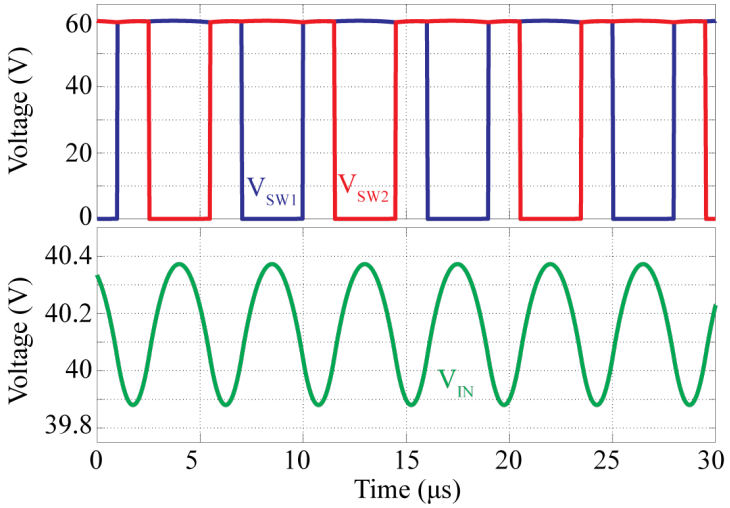

Figure 6.10: IBR-Z input ripple simulation (40V input)

6.6 Experimental Results

According to the modified design procedure, a 250-W IBR-Z prototype was designed and built with the specifications provided in Tables 6.1 and 6.2. The prototype has 60% less ferrite and is a 46% reduction in volume (430cm^3 to 230cm^3) from the original IBR, fulfilling the volumetric requirement. A photograph of the prototype is shown in Fig. 6.11. Once

again, the control system was implemented using a TI TMS320F28026 MCU, utilizing its four internal PWM submodules. The natural current and voltage balancing is shown in Fig. 6.12, along with the inherent current ripple cancellation.

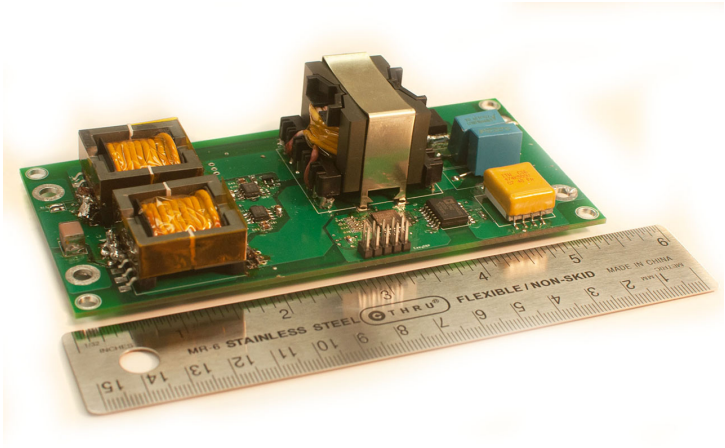

Figure 6.11: IBR-Z experimental prototype)

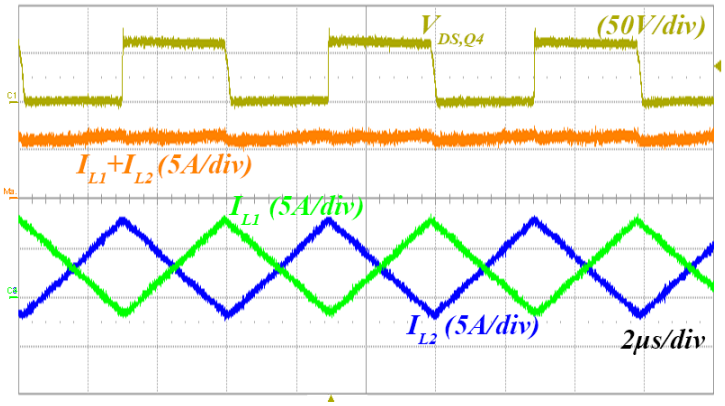

Figure 6.12: IBR-Z input current (30V input/75% power)

Light load performance of the transformer is shown in Figs. 6.13 and 6.14, also demonstrating the relative impact of the diode capacitance.

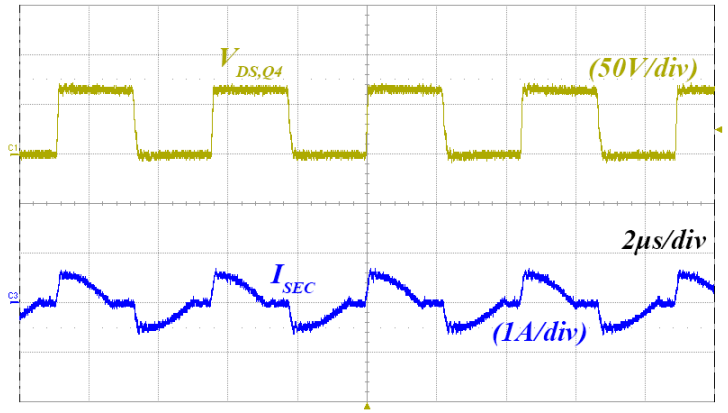

Figure 6.13: IBR-Z transformer current (30V input/20% power)

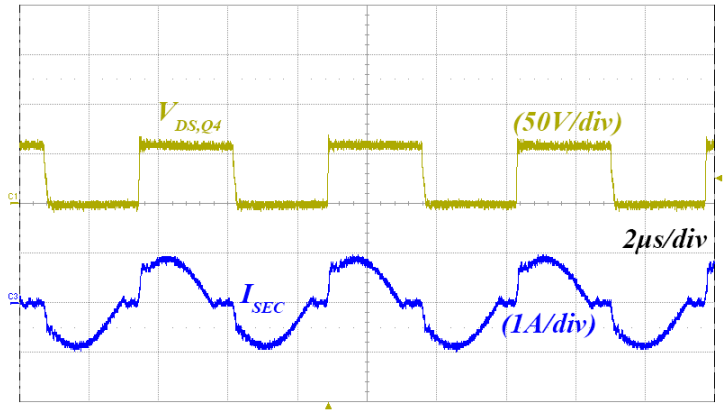

Figure 6.14: IBR-Z transformer current (30V input/40% power)

Like the original IBR, the transformer maintains a high power factor at nominal input (Fig. 6.15), high-line input (Fig. 6.16), and low-line input (Fig. 6.17). Diode ZCS is maintained even at high switching frequency and high power output (Fig. 6.18).

The impact of the ripple cancellation on the switching frequency ripple is clearly shown in Figs. 6.19 and 6.20. Fig. 6.19 shows the nearly complete cancellation of the input ripple at the nominal input, while Fig. 6.20 shows the worst operating case at high-line input.

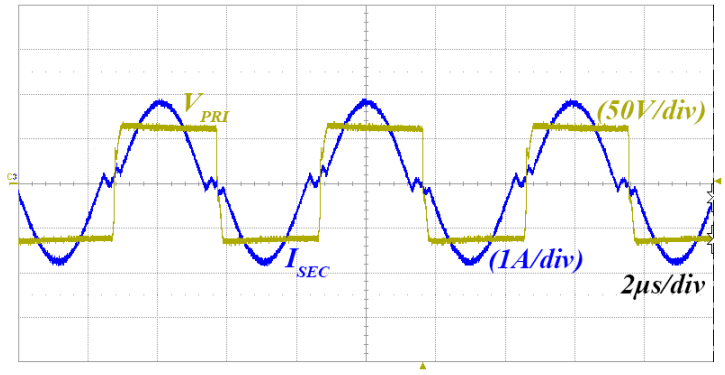

Figure 6.15: IBR-Z nominal transformer voltage and current (30V input/75% power)

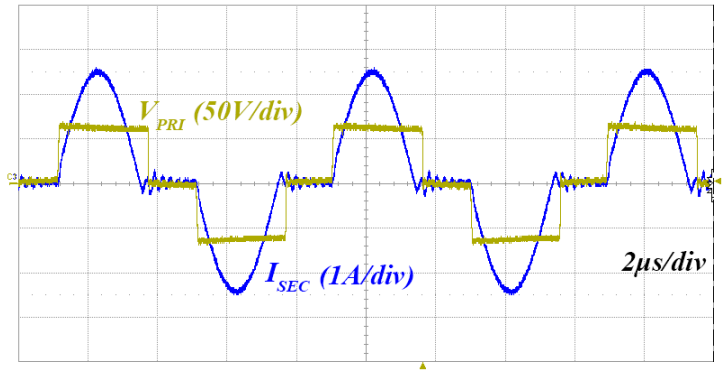

Figure 6.16: IBR-Z high line transformer voltage and current (40V input/75% power)

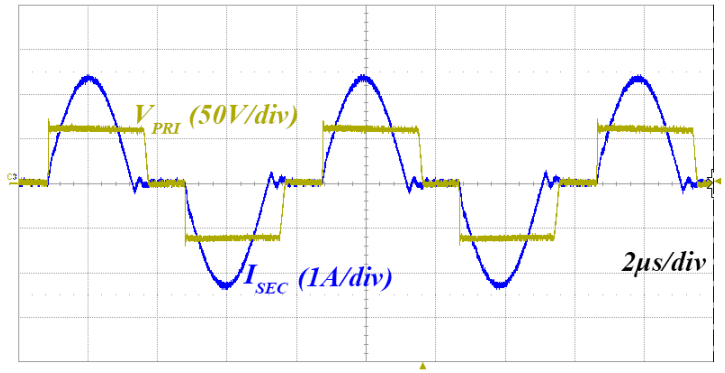

Figure 6.17: IBR-Z low line transformer voltage and current (20V input/75% power)

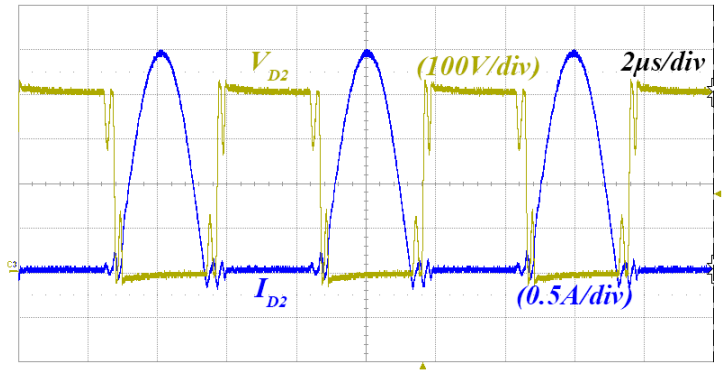

Figure 6.18: IBR-Z nominal input / full-power diode ZCS (30V input/100% power)

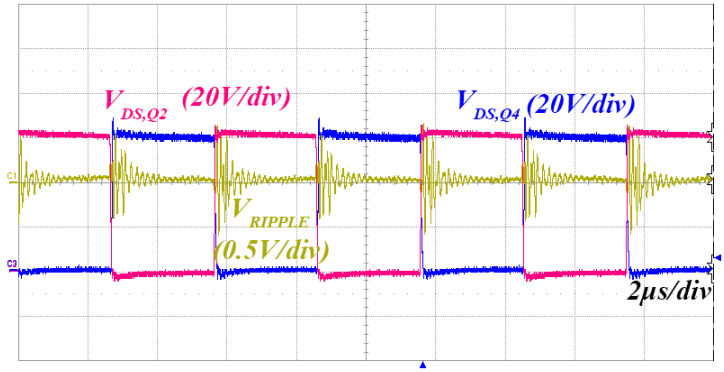

Figure 6.19: IBR-Z nominal input voltage ripple (30V input/75% power)

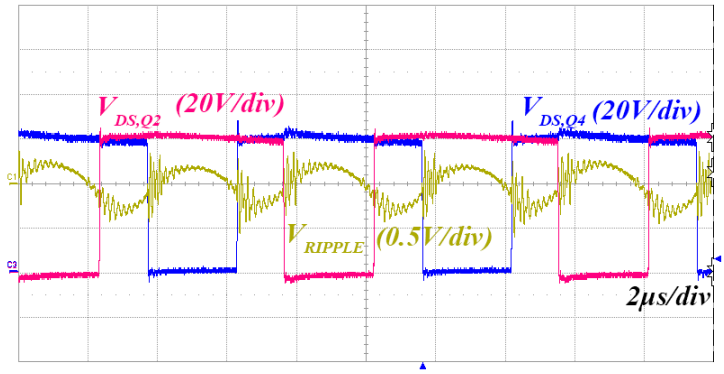

Figure 6.20: IBR-Z high line input voltage ripple (40V input/75% power)

Implementing the CTL soft-start method also improves converter performance, allowing for safe operation even with an extremely large output capacitance. This allows normal initialization of a centralized inverter with only a single micro-converter unit operating. Experimental results with a moderate (40μF) and an extremely heavy (690μF) output capacitance are shown in Figs. 6.21 and 6.22.

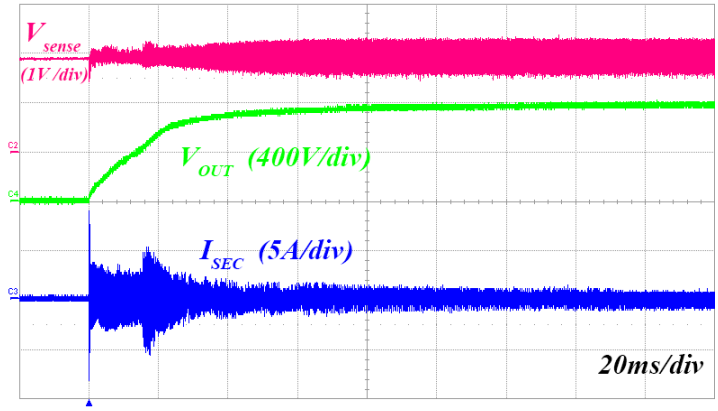

Figure 6.21: IBR-Z CTL startup (30V input/400V output/40μF output capacitance)

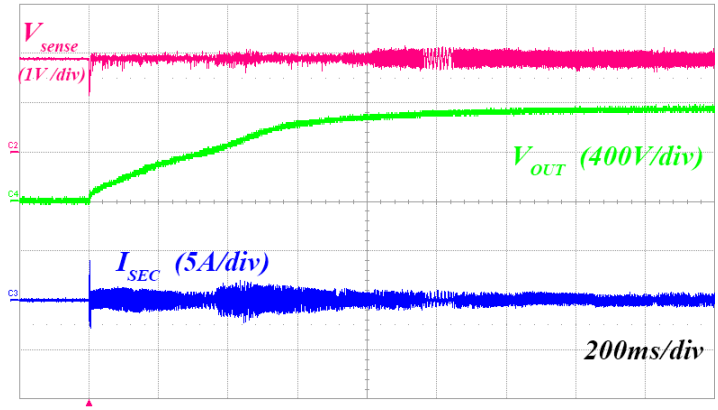

Figure 6.22: IBR-Z CTL startup (30V input/400V output/690μF output capacitance)

Utilizing the IBR-Z structure, combined with the hybrid-frequency modulation, produces a power stage efficiency shown in Fig. 6.23. As in previous chapters, power measure-

ments were taken using four Fluke Model 287 digital multimeters. At the nominal input (30V), the resultant power stage CEC efficiency is 97.5% (and 97.2% with auxiliary loss included), an improvement on the previous IBR.

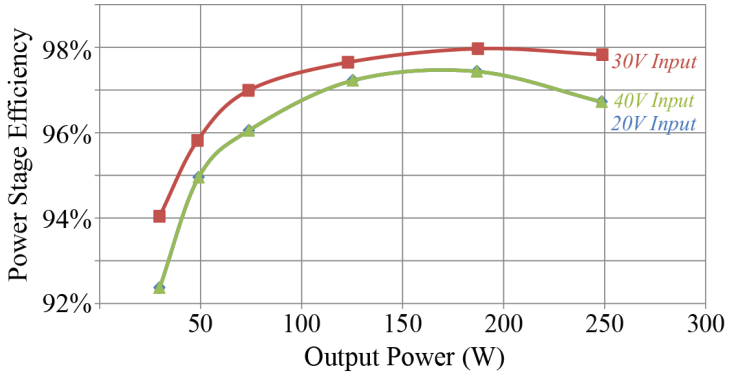

Figure 6.23: IBR-Z experimental power stage efficiency

6.7 Summary

Returning to the first portion of the micro-converter discussion led to the continued evolution of the system design. Using the insight gained into the dominant loss elements and component sizing issues led to the desire to remove the switching frequency barrier from the converter design. From the ZVS process definition, and the basic concepts used in the initial converter synthesis (Chapter 2), a new converter structure, the IBR-Z, was developed. This converter uses many of the same operating principles as the original IBR, but it uses the ripple-based ZVS technique to allow for significantly increased switching frequencies. The design criteria and loss analysis from Chapter 2 was adapted in order to correctly account for these new techniques.

Because of the strong influence of the original IBR design and the vertically integrated nature of the modulation, transient mitigation, and steady-state optimization, these additional design concepts (Chapters 3-5) were carried over to the IBR-Z with some modification. With the hybrid-frequency modulation, handling the circulating energy in the input inductance became a priority, as well as optimizing for 75% load and nominal input voltage. Through demonstrating the inherent volt-second balance of the transformer, the CTL soft-start method was extended to the IBR-Z by applying independent control to the two phase legs. Finally, switching ripple cancellation was evaluated in the IBR-Z by examining the interaction between the two switch-node voltages in steady-state. Experimentally, a 250-W prototype IBR-Z was developed, which demonstrated a 97.5% CEC efficiency alongside a 60% reduction in ferrite material and a 50% reduction in overall converter volume.

Chapter 7

Conclusion

Power electronic systems are often complex, multifaceted systems, especially when placed in an application as variable and demanding as PV. In order for the system to be effective, a number of features must cooperate to form the end behavior. Due to the nature of such a system, the circuit topology drives much of the discussion, but not all of it. Focusing on topology at the expense of control, or modulation at the expense of optimization, creates a design structure that is prohibitively out of balance. Using the PV problem as a backdrop for an integrated design procedure has been a consistent theme throughout this work.

The focus of this dissertation was to develop a dc-dc micro-converter circuit and its associated control systems that would fulfill its required role in the distributed PV PCS. Because the system uses a parallel architecture with a roughly 400V dc bus, each converter needed to maintain a high boost ratio from the panel-level (roughly 30V) input. Also, because

of the heavy emphasis on weighted (CEC) efficiency for PV equipment, the circuit needed to be optimized for nominal panel input, with an emphasis on light- to medium-load efficiency. Though Galvanic isolation was not required by electric code, it is desirable in order to prevent ground currents and injected EMI in the system. From these objectives, a new topology, the Integrated Boost Resonant (IBR) converter was developed. The circuit is a combination of a traditional PWM boost converter and a DCM-operated, series resonant circuit. The DCM operation of the high-frequency transformer possessed much lower circulating energy compared to traditional CCM behavior. When combined with ZCS for the output diode, this resulted in a circuit with a high weighted efficiency of 96.8%. Because the boost and series-resonant functions could be compressed into a single switch-node, the active device count could be reduced to two complementary MOSFETs, leading to simple control and gate drive systems. The topology can natively handle a variety of control implementations, including input voltage control. A design procedure was also developed along with a theoretical loss analysis.

With the topology developed, the next goal was to utilize control and modulation to improve the performance of the system, specifically optimizing the efficiency at nominal input and decoupling the weighted efficiency from the operating range. This is accomplished primarily by optimizing the switching period utilization by the resonant stage. However, existing modulation methods only provided, at most, benefits in one-half of the operating range and never optimized for the nominal input, the most crucial for CEC evaluation. In order to accomplish these targets, a new modulation scheme was proposed. The new, hybrid-

frequency method utilized areas where the modulator operated in constant-on, constant-off, and fixed-frequency conditions depending on duty cycle, the resonant period length, and the desired input range. This new method extended the operating range as wide as 12-48V and improved the CEC efficiency to 97.2% in the 250-W prototype. These gains were mostly impacted by large reductions in core loss and conduction loss at the nominal input voltage, with only a small increase in switching loss.

In the distributed dc-dc PCS architecture, one major concern was the startup procedure. The inverter system, with its large (greater than 500μF) bus capacitor presented a heavy load when it was completely discharged. In the IBR converter, the lower primary-side capacitor began with full input voltage seen across it. As the converter reached equilibrium, the capacitor voltage maintained the same potential, regardless of duty cycle. The lower secondary-side capacitor was a reflection of the input voltage at equilibrium but began with zero voltage initially. The transient current involved in charging this capacitor was found to be potentially destructive when left uncorrected. By monitoring the ac transient voltage across the lower primary-side capacitor, the amount of energy flowing in the system could be controlled. Thus, a new capacitor-transient limited (CTL) soft-start method was developed, limiting the capacitor discharge by prematurely ending the lower switch on-time in order to prevent an excessive current transient. In support of this method, analysis of the transient operation of the IBR, including the voltage transient, was provided. Using the internal circuitry of the TI TMS320F28026 MCU, a sensing circuit including a high-pass filter and a dc-restore circuit was presented, along with design guidelines for the circuit elements. Un-

fortunately, the control and gate drive systems were not capable of instantaneous action and instead incorporate some delay into the transient behavior. Though this presented a minimum value for the limited peak current, it was accounted for in the final design equations. A prototype design was then applied to the IBR system, allowing safe system startup with a range of capacitive loads from 2μF to 500μF, with a consistent peak current without the need for current sensing.

Also relevant to the system design was the ability to consistently extract the maximum available power from the PV panel. This ability was defined as the MPPT efficiency and based on the injected ripple in the PV voltage. A new method for analyzing the PCS MPPT efficiency was proposed based on panel-derived models. From the panel model, an expression demonstrating the MPPT efficiency was derived, and a ripple "budget" for the harmonic sources was determined. These ripple voltages were generated by three main sources: the MPPT algorithm, PCS switching, and inverter double-line-frequency ripple. The ripple sources were then analyzed and suggestions for controlling their contributions were proposed, enabling circuit designers to make informed and cost-effective design decisions. The switching ripple behavior was analyzed in the frequency domain, and because most of the power stage elements were determined already, the input capacitance was the only variable free to correct for the switching ripple contribution. For the 250-W prototype only 5μF of input capacitance was sufficient for a 99.8% MPPT efficiency. Similarly the tri-level ripple from the MPPT algorithm was analyzed and, through significant simplification effort, the ripple contribution resolved to simply the square of the step size, regardless of MPPT update rate. This placed

a premium on MPPT sensing accuracy, filtering, and granularity over pure speed. A step size of 0.36V was sufficient for the 99.8% efficiency test case. Due to the addition of input voltage control, the double-line frequency that propagated to the PV terminals could be reduced without additional capacitance. The amount of ripple rejected was dependent on the compensator gain at 120Hz, the test case requiring a gain of -17dB. Greater ripple rejection would require advanced control, greater bandwidth, or faster processing capability. Verification of these methods was provided in both simulation and experiment.

In the IBR circuit, one of the major limitations was the hard-switching behavior of the primary-side MOSFETs. This prevented increasing the switching frequency, which in turn prevented further reduction in converter volume without prohibitively increased loss. As a solution, a modification to the IBR topology was proposed that achieved soft-switching (ZVS) on the active devices and allowed the increase of the switching frequency. Consequently, the increase in current ripple associated with this method required the interleaving of two phases of the boost converter. With some simplification, this enhancement only included two additional MOSFETs and one inductor on the low-voltage side. The maximum switching frequency could then be increased from 70kHz to 170kHz. This allowed for a 46% reduction in converter volume (from 430cm^3 to 230cm^3) while retaining greater than 97% weighted efficiency. The design procedure was augmented to accommodate this new structure, with few additional computations necessary. The hybrid-frequency, CTL soft-start, and MPPT efficiency methods were each extended to this new topology, continuing the development cycle.

7.1 Major Contributions

In summary, the major technical contributions of this work were:

1. **Developed of a new dc-dc micro-converter topology, the Integrated Boost Resonant (IBR) converter.** A combination of a PWM boost converter and a DCM series-resonant half-bridge, this circuit achieves high CEC efficiency through minimizing circulating energy and diode loss. With inherent isolation, simple control, and minimal device count, it is uniquely suited for this application.

2. **Created an unique modulation method for PWM-integrated resonant converters.** Based on optimizing the switching period utilization, this hybrid-frequency modulation is a combination of constant-on, constant-off, and fixed-frequency control. It improves the converter efficiency at nominal input and allows for increasingly wider input range without additional loss.

3. **Synthesized a new soft-start technique based on limiting capacitor transients.** Rather than continue applying an existing technique, startup conditions specific to the IBR converter were explored. By limiting the ac transient across a nominally dc capacitor voltage with little additional cost, the initial behavior of the converter was successfully controlled in the presence of large capacitive loads.

4. **Optimized micro-converter energy extraction through model-based techniques.** By expanding upon previously available models, understanding of the effect

of voltage ripple on MPPT efficiency was improved. The various ripple sources were evaluated, and methods for controlling their contributions were established, allowing circuit designers to make cost-effective design decisions.

5. **Expanded upon the IBR principle through combining with soft-switching techniques.** By removing the prohibitive switching loss, the size of the micro-converter was dramatically reduced, and it requires only one additional inductor and two low-voltage MOSFETs. Because it is based on the same operating principles as the original IBR, the modulation, soft-start, and ripple optimization techniques were also extended to this new circuit.

Ultimately, the desired outcomes of developing an isolated micro-converter system were achieved, including:

- High weighted efficiency (>97%)
- Small size (<250cm^3)
- Current-limited startup of inverter system (with bus capacitance >500μF)
- Improved MPPT efficiency (>99.8%)

7.2 Future Work

Future work in the micro-converter area revolves around two principal objectives—efficiency improvement/size reduction and system-level investigation. Demonstrated in this work was specifically the benefits of PWM and resonant circuit integration along with the use of optimized modulation. Integration of the magnetic components should be achieved to further reduce the size of the converter. If the size of the converter can be reduced without sacrificing efficiency, this will certainly improve the marketability of the micro-converter solution. Eventually, the co-packaging of the converter with a PV panel during manufacture would be a productive goal. Another hardware-related issue is the use of smaller micro-converter circuits designed to operate on the sub-panel level. This would further improve MPPT efficiency and optimization by breaking a larger panel down into smaller units more likely to have uniform irradiance. In larger scale systems, a higher bus voltage (>400V) may be desirable in order to prevent excessive conduction loss between the micro-converters and the centralized inverter. This would also increase compatibility with industrial-level distribution, such as 480-V three-phase systems.

The second major area, system-level optimization, is also of major interest going forward. Though the micro-converter provides natural (Galvanic) isolation in the event of a fault, plans for its implementation under existing arc- and ground-fault protection schemes remain unresolved. With advanced inverter functions such as Volt-VAR and Volt-Watt control becoming critical issues for PV adoption at the utility-level, micro-converter

compatibility with these methods must also be explored. Finally, the effect of PCS ripple on other panel types, such as organic cell or high concentration (such as CdTe) systems, is also relevant to future research efforts.

Appendix A

Derivation of Multi-Frequency PV Model

Beginning with analysis similar to [89], the PV output current can be written as a function of PV terminal voltage in the form of (A.1). Where α, β, and γ are constants determined either analytically or through fitting the PV panel I-V curve at the MPP.

$$I_{PV} = \alpha V_{PV}^2 + \beta V_{PV} + \gamma, \text{ [A]} \tag{A.1}$$

The instantaneous power output of the panel can then be written as in (A.2).

$$P_{PV} = V_{PV} I_{PV} = V_{PV} \left(\alpha V_{PV}^2 + \beta V_{PV} + \gamma \right), \text{ [W]} \tag{A.2}$$

Assuming perfect tracking of the MPP with no dc offset, the instantaneous voltage can be written as a summation of ac ripple terms, rather than a single ripple frequency, as given in (A.3). This is where the proposed analysis begins to differ from [89], which assumes only a single ripple frequency:

$$V_{PV} = V_{MPP} + \sum_{n=1}^{m} V_n \cos(\omega_n t), \text{ [V]} \tag{A.3}$$

With the expression for PV voltage, the instantaneous PV power output may be re-written as (A.4).

$$\begin{aligned} P_{PV} = \left(V_{MPP} + \sum_{n=1}^{m} V_n \cos(\omega_n t) \right) \Bigg[& \alpha \left(V_{MPP} + \sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 \\ & + \beta \left(V_{MPP} + \sum_{n=1}^{m} V_n \cos(\omega_n t) \right) + \gamma \Bigg] \end{aligned} \tag{A.4}$$

Expanding some of the terms:

$$\begin{aligned} P_{PV} = {} & V_{mpp} \left(\alpha {V_{mpp}}^2 + \beta V_{mpp} + \gamma \right) + 3\alpha {V_{mpp}}^2 \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) \\ & + 3\alpha V_{mpp} \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 + 2\beta V_{mpp} \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) \\ & + \beta \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 + \gamma \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) \end{aligned} \tag{A.5}$$

From the definition of the model in (A.2)

$$P_{mpp} = V_{mpp} I_{mpp} = V_{mpp} \left(\alpha {V_{mpp}}^2 + \beta V_{mpp} + \gamma \right) \tag{A.6}$$

Thus (A.5) can be re-written as (A.7)

$$\begin{aligned} P_{PV} =& P_{mpp} + 3\alpha {V_{mpp}}^2 \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) + 3\alpha V_{mpp} \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 + \\ & 2\beta V_{mpp} \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) + \beta \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 + \gamma \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right) \end{aligned} \tag{A.7}$$

At this juncture, it is prudent to refine the analysis to only quantities which carry a non-zero average over an infinite length of time. Seeing that the average value of the cosine function, given in (A.8) is identically zero as the period of interest becomes infinitely long, the majority of the terms in (A.7) may be neglected. This leaves the analysis much less complicated, and shown in (A.9).

$$f_{avg} = \lim_{T \to \infty} \frac{1}{T} \int_0^T \cos(\omega t)\, dt = 0 \tag{A.8}$$

$$P_{PV} = P_{mpp} + (3\alpha V_{mpp} + \beta) \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 \tag{A.9}$$

Considering only the squared summation term in (A.9), a partial expansion is given in (A.10). Notice that the result is a series of squared cosine terms at each of the ripple frequencies, plus an infinite number of beat frequencies, creating a varied and complex harmonic spectrum. However, each of these beat frequencies, similar to the majority of the terms in (A.7) has a zero average value over an infinitely long period.

$$\begin{aligned} \left(\sum_{n=1}^{m} V_n \cos(\omega_n t) \right)^2 =& \sum_{n=1}^{m} {V_n}^2 \cos^2(\omega_n t) \\ & + 2 \sum_{k=1}^{m} \sum_{n=2}^{m} \left(\frac{V_n V_k}{2} \cos((\omega_n - \omega_k)\, t) + \frac{V_n V_k}{2} \cos((\omega_n + \omega_k)\, t) \right) \end{aligned} \tag{A.10}$$

This further simplifies (A.9) into (A.11)

$$P_{PV} = P_{mpp} + (3\alpha V_{mpp} + \beta)\left(\sum_{n=1}^{m} {V_n}^2 \cos^2(\omega_n t)\right) \tag{A.11}$$

This expression can be further simplified, given that the average of the square of the cosine function is identically , as shown in (A.12).

$$f_{avg} = \lim_{T\to\infty} \frac{1}{T} \int_0^T \cos^2(\omega t)\, dt = \frac{1}{2} \tag{A.12}$$

Thus, the final expression for the average power output of the PV panel is given in (A.13).

$$P_{PV,avg} = P_{mpp} + \left(\frac{3\alpha V_{mpp} + \beta}{2}\right)\left(\sum_{n=1}^{m} {V_n}^2\right) \tag{A.13}$$

If considering only one harmonic frequency, it can easily be shown that (A.13) reduces to the result provided in [19], [89]. With a model for the average power of the PV panel developed for multiple ripple frequencies, the proceeding sections will evaluate the contributions from the various ripple sources in a distributed MPPT PV system.

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