State-Trajectory Analysis and Control of LLC Resonant Converters

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ABSTRACT

With the fast development of communication systems, computers and consumer electronics, the power supplies for telecoms, servers, desktops, laptops, flat-panel TVs, LED lighting, etc. are required for more power delivery with smaller spaces. The LLC resonant converter has been widely adopted for these applications due to the advantages in high efficiency, high power density and holdup time operation capability.

However, unlike PWM converters, the control of the LLC resonant converter is much more difficult because of the fast dynamic characteristic of the resonant tank. In some highly dynamic processes like the load transient, start-up, over-load protection and burst operation, it is hard to control the current and voltage stresses and oscillations in the resonant tank. Moreover, to meet the high power density requirement, the LLC is required to operate at a high switching frequency. Thus the driving of the synchronous rectifier (SR) poses a design challenge as well.

To analyze the fast dynamic characteristic, a graphic state-plane technique has been adopted for a class of resonant converters. In this work, it has been extended to the LLC resonant converter. First of all, the LLC steady state and dynamic behaviors are analyzed in the state plane. After that, a simplified implementation of the optimal trajectory control

is proposed to significantly improve the load transient response: the new steady state can be tracked in the minimal period of time.

With the advantages of the state-trajectory analysis and digital control, the LLC soft start-up is optimized as well. The current and voltage stress is limited in the resonant tank during the start-up process. The output voltage is built up quickly and smoothly.

Furthermore, the LLC burst mode is investigated and optimized in the state plane. Several optimal switching patterns are proposed to improve the light load efficiency and minimize the dynamic oscillations. During the burst on-time, the LLC can be controlled to track the steady state of the best efficiency load condition in one-pulse time. Thus, high light-load efficiency is accomplished.

Finally, an intelligent SR driving scheme is proposed and its simple digital implementation is introduced. By sensing the SR drain to source voltage and detecting the paralleled body diode conduction, the SR gate driving signal can be tuned within all operating frequency regions.

In conclusion, this work not only solves some major academic problems about analysis and control of the LLC resonant converter based on the graphic state plane, but also makes significant contributions to the industry by improving the LLC transient responses and overall efficiency.

To My Family:

My parents: Guoqiang Feng

Yuzhen Fan

My wife: Rongrong Mao

My daughter: Ke Feng

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Chapter 1. Introduction

This chapter presents the motivations and objectives of this work. The advantages of LLC resonant converters and its wide applications are investigated. The challenges in controlling the fast dynamic response of the resonant tank and limiting the circulating energy are described. A literature review in this field is provided, followed by the dissertation outline and the scope of research.

1.1 Background

With the explosive development of information technology, the communication and computing systems, such as telecoms, servers, desktops, laptops and notebooks have become a large market for the power supply industry. For the advance of the integrated circuit technology, the density and functionality of computer systems are continually increasing, which requires more power delivery while smaller size on power suppliers [A.1-A.15]. For consumer electronics, such as flat-panel TVs and LED lighting, high reliability, low cost and high efficiency power supplies are demanded [A.16-A.19].

Ac-dc front-end converters as shown in Fig. 1.1 are widely adopted by these applications. Driven strongly by economic and environmental concerns, high efficiency is becoming more and more desired for ac-dc front-end converters. The 80 PLUS programs provide a class of efficiency requirements as shown in Fig. 1.2 [A.13]. Take the 80 PLUS TITANIUM program as an example, it provides the highest efficiency requirement for the front-end converters nowadays. The certified power supplies are expected to achieve 91% efficiency at 100% load, 96%

efficiency at 50% load, 94% efficiency at 20% load, and 90% efficiency at 10% load when converting 230V ac power from electric utilities to dc power used in most electronics. The efficiency requirement at the dc-dc stage is even higher to meet the overall efficiency from ac input to the load.

In addition to the efficiency requirement, the power density of front-end converters is continuously increasing as well [A.6]. Higher power density will eventually reduce the converter cost and allow for accommodating more equipment in the existing infrastructures. As shown in Fig. 1.3, in the past ten years, the power density of front-end commercial converters has increased by seven times. This will continuously increase in the future because of the fast developments in new devices, magnetic materials and so on [A.20-A.23].

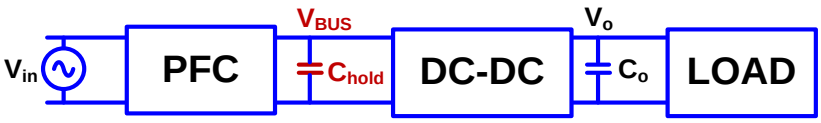


Fig. 1.1 Ac-dc front-end converter structure

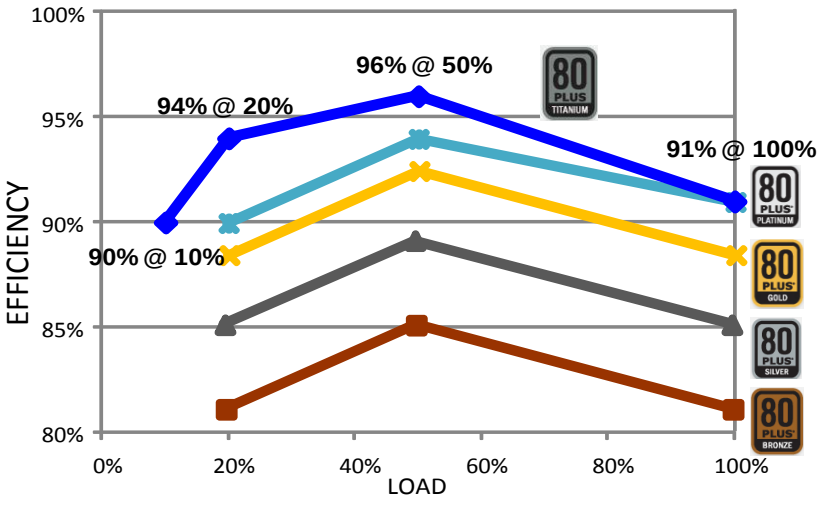


Fig. 1.2 Efficiency requirement for ac-dc front-end converters

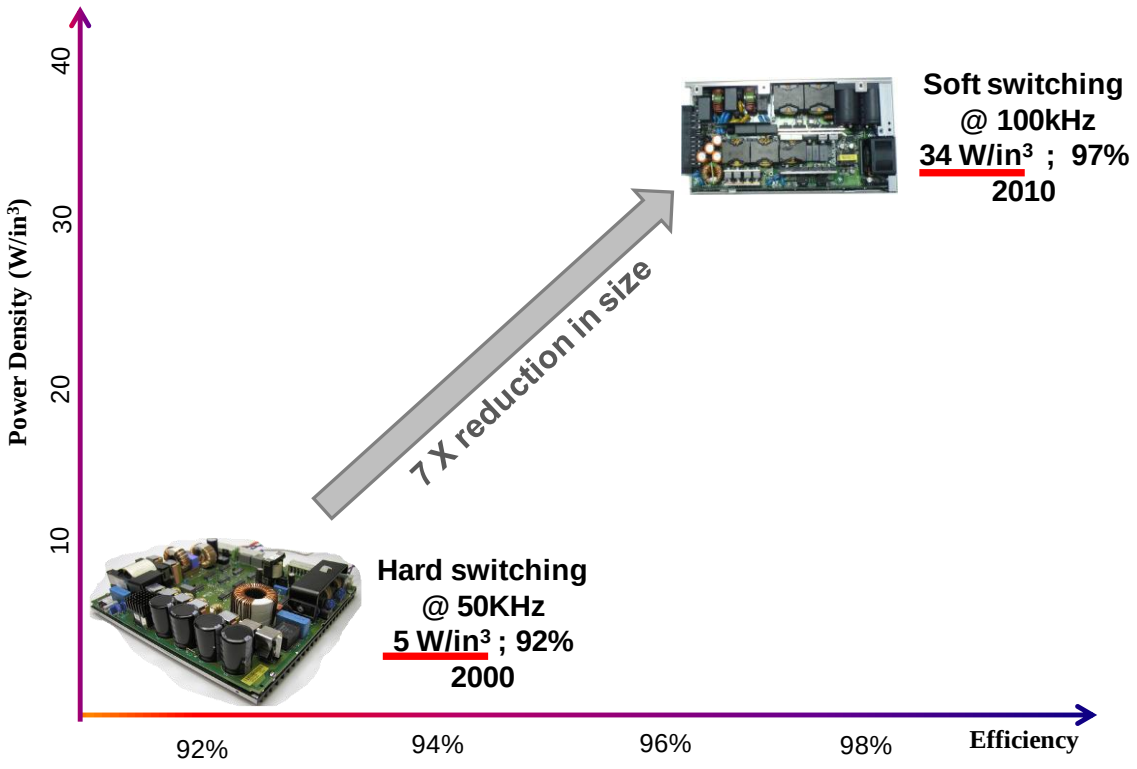


Fig. 1.3 Power density requirement for ac-dc front-end converters

Moreover, the holdup time operation poses another major design challenge. As shown in Fig. 1.4, the front-end ac-dc converters are required to maintain the regulated output voltage for about 20ms when the input ac line is lost [A.24]. As shown in Fig. 1.1, during the holdup time, all the energy transported to the load comes from the holdup capacitor C_{hold}. The requirement of C_{hold} is determined by the system power level and the input voltage range of the dc-dc converter. Apparently, the wider the dc-dc stage input voltage range is, the fewer bulky holdup time capacitors are required, and the higher power density will be. Therefore, to meet the holdup time operation requirement, the capability of operating within a wide input voltage range is required for the dc-dc stage in front-end converters.

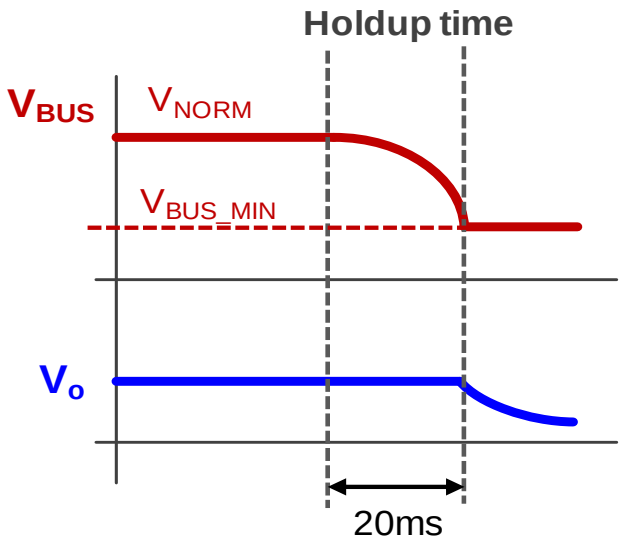


Fig. 1.4 Holdup time operation of ac-dc front-end converters

Hard-switching PWM converters [A.25] cannot meet higher efficiency and high-power-density requirements at the same time, since hard switching leads to high switching loss for high frequency operation.

Soft-switching PWM circuits, such as the phase-shift full-bridge PWM converter and the asymmetrical half-bridge PWM converter, are widely used for the front-end dc-dc conversion [A.26-A.28]. The bulky capacitors are used to provide energy during the holdup time. Enlarging the operation range of the dc-dc stage can reduce the holdup capacitors. However, the PWM converters have to sacrifice normal operation efficiency to extend their operation range. Normally, the duty cycle is designed to be as high as possible to handle the holdup time operation, so when it comes to normal conditions, the duty cycle is much smaller. The primary side to secondary side transformer turns ratio is small, which leads to a high primary side current.

Both conduction loss and switching loss increase. Consequently, the efficiency suffers at normal operation conditions.

Resonant converters can achieve very a low switching loss, thus enabling them to operate at high switching frequencies in order to keep power density high while maintaining good efficiency [A.29-A.31]. Recently, the LLC resonant converter (LLC) as shown in Fig. 1.5 has received a lot of attention [A.5] [A.7] [A.8] [A.11] [A.32-A.37].

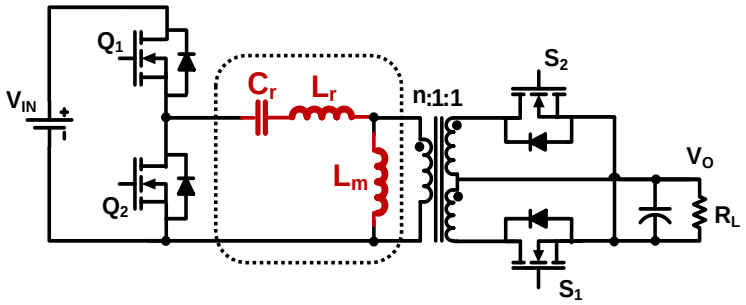


Fig. 1.5 LLC resonant converter

The voltage gain of the LLC resonant converter is shown in Fig. 1.6.

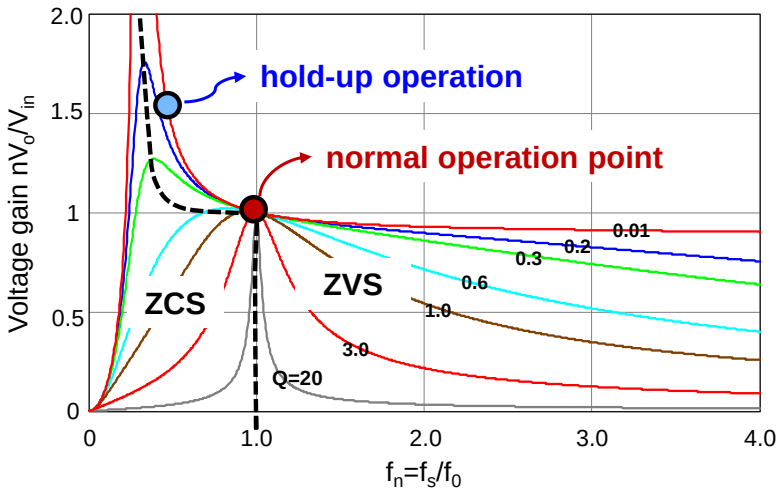


Fig. 1.6 Voltage gain of LLC resonant converter

Under nominal conditions, the LLC operates near the resonant frequency point (f_s=f_0) to achieve high efficiency, because of zero-voltage-switching (ZVS) for the main switches and zero-current-switching (ZCS) for the output rectifiers. In addition, voltage gains of different Q converge at this point. Thus, the LLC resonant tank can be optimized to achieve good efficiency for a wide load range. By reducing the LLC switching frequency, high voltage gain is achievable, which is desired for the holdup time operation. Thus, the holdup time extension capability is accomplished without sacrificing the efficiency under the nominal operating condition. Therefore, the LLC resonant converter has been a very popular topology for the front-end power supplies in computing systems and consumer electronics systems.

In today's market, many commercial controllers (as shown in Fig. 1.7) have been released [A.38-A.44]. Like other resonant topologies, the switching frequency is controlled to regulate the LLC output voltage or output current. These controllers also provide some supplementary functions, such as over current protection, over voltage protection, under voltage lockout, burst mode, soft start-up, etc.

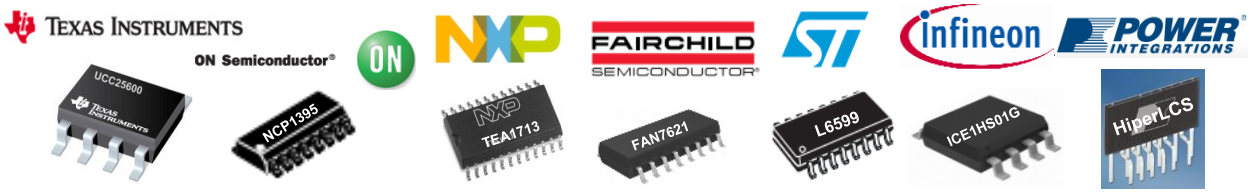


Fig. 1.7 Commercial controllers for the LLC resonant converters

However, the control of the LLC resonant converter is much more complex than that of PWM converters due to the fast dynamic characteristics of the resonant tank. The natural frequency of the output filter for PWM converters is much lower than the switching frequency.

When it comes to the LLC resonant converter, the natural frequency of the resonant tank is close to the switching frequency. Therefore, it is difficult to describe and control the resonant tank dynamic behavior. In order to get a good dynamic performance and limit the resonant circulating energy, there are many issues related to the control of the LLC resonant converter.

1.2 Dissertation Motivation and Objective

1.2.1 State-trajectory analysis for LLC resonant converters

For PWM converters, the state-space average method can provide a simple and accurate small-signal model to analyze the dynamic behavior [B.1] [B.2]. For resonant converters, the natural frequency of the resonant tank is close to the switching frequency. Since the average modeling method will eliminate the information of the switching frequency, it cannot predict the dynamic performance of the resonant tank. Therefore, some other approaches such as an extended describing function [B.3] [B.4], a multi-frequency averaging method [B.5], and a simulation-based method [A.5] [B.6] are required. But all of them require extensive computation effort. Moreover, due to the limitations of the small-signal model, these methods are only valid around a particular operation point. Thus, they cannot ensure high performance under large load variations. In addition, to the soft start-up and over-load protection, the switching frequency varies in a wide range, thus the tank behavior cannot be explained by the small-signal model as well.

Compared with the complicated modeling derivation and the limited performance of the small-signal models, the graphical state-trajectory analysis is much clear and useful to analyze the resonant converters [B.7-B.19].

Take the series resonant converters (SRC) as an example, the state-trajectory analysis has been present to describe its steady state and transient behaviors [B.7] [B.8]. The resonant capacitor C_r and the resonant inductor L_r are in series as shown in Fig. 1.8. The equivalent voltage V_E across the resonant tank changes under different conduction stages as illustrated in Table 1.1. By normalizing the resonant capacitor voltage v_{Cr} with the voltage factor V_s, and resonant current i_{Lr} with the current factor V_s/Z_0 (i.e. Z_0 is the characteristic impedance $Z_0 = \sqrt{L_r/C_r}$), the state-trajectory is shown in Fig. 1.9, where N refers to the normalized variables.

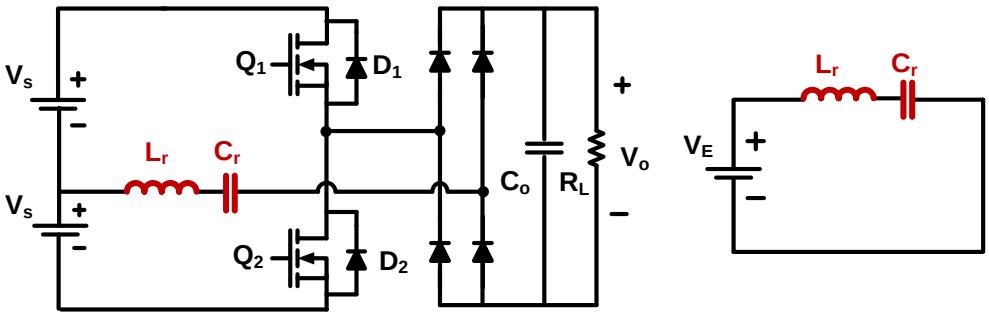


Fig. 1.8 SRC topology and its equivalent circuit

Table 1.1 SRC equivalent voltages under different conduction status

Conduction	**V_E**	**V_{EN}**
Q_1	V_s-V_o	1-V_{oN}
D_1	V_s+V_o	1+V_{oN}
Q_2	-V_s+V_o	-1+V_{oN}
D_2	-V_s-V_o	-1-V_{oN}

In the state-plane, the normalized voltages across the resonant tank V_{EN} determine the trajectory centers, and the radiuses reflect the energy in the resonant tank. For the control law,

the variable R is continuously monitored, the power switches are turned on at the instant when R becomes equal to the control reference R_{ref}.

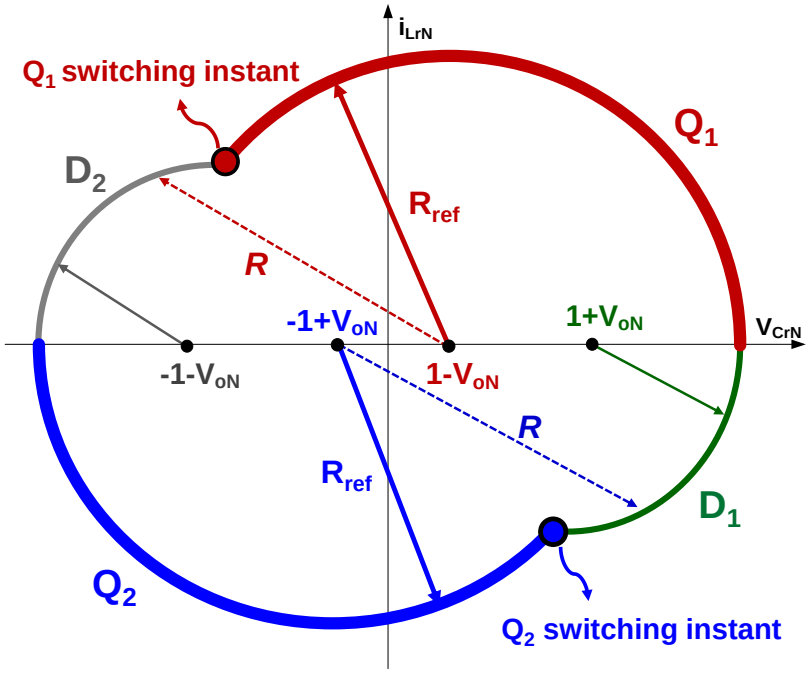


Fig. 1.9 SRC state-trajectory

During the load step-down transient, the control reference will change from the heavy-load large radius (R_{ref_H}) to the light-load small radius (R_{ref_L}) as shown in Fig. 1.10. Thus, the operation status will stay in D_2 trajectory until it hits the new control law of R_{ref_L}. As the load steps up, the control reference will change from R_{ref_L} to R_{ref_H} at the transient moment. The operation status in D_2 trajectory is interrupted, and it follows Q_1 trajectory as it touches the circle with the new control reference R_{ref_H}.

By forcing the state variables to track the desired trajectory, this approach is named optimal trajectory control (OTC). It guarantees that the time required to reach the new steady state is

minimal and the overshoot is avoided. Compared with linear control methods based on the small-signal model as shown in Fig. 1.11, it shows a much better dynamic performance.

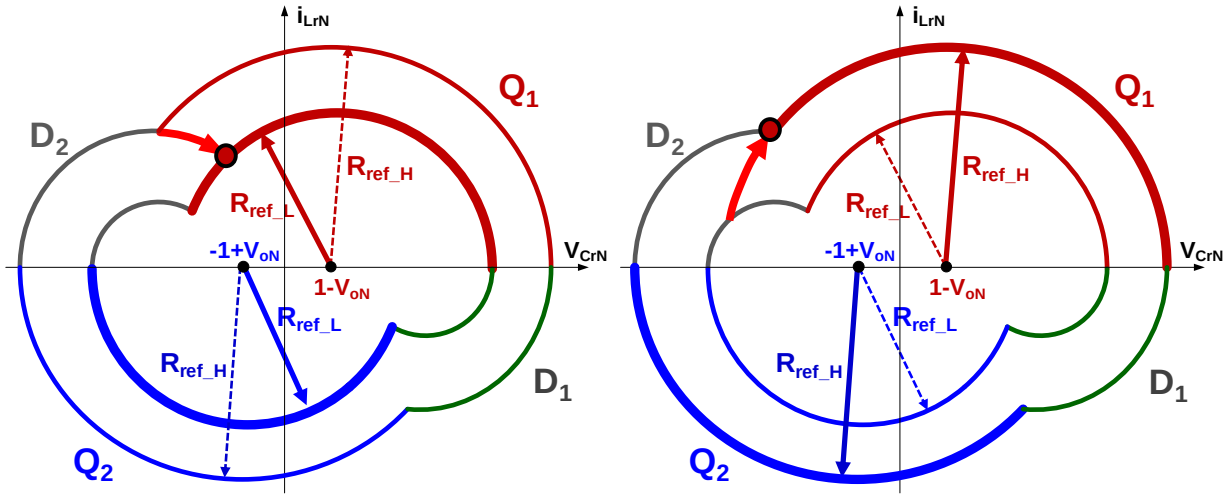


Fig. 1.10 Optimal trajectory control of SRC in load step-down and step-up

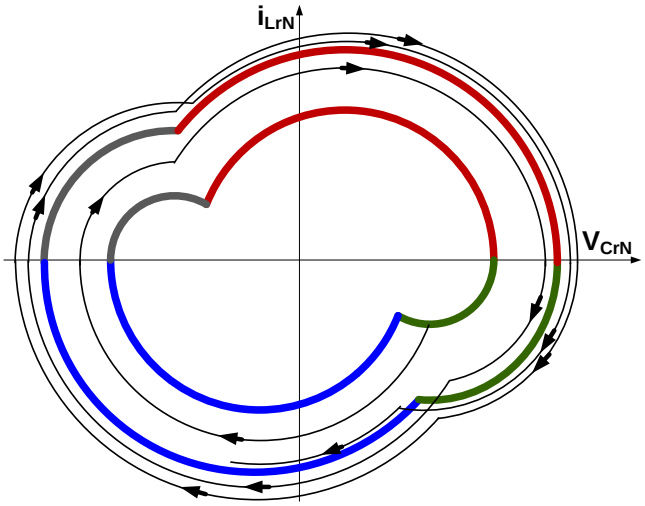


Fig. 1.11 Linear compensator control of SRC in load step-up

However, when it comes to multi-element resonant converters, there are more than two state variables that need to be represented. In [B.19], the three-dimensional (3D) state-space trajectory

of the series-parallel resonant converter (SPRC) is illustrated. For the LLC resonant converter, a 3D state-space trajectory is shown in Fig. 1.12 to represent all the resonant capacitor voltage v_{Cr}, resonant inductor current i_{Lr}, and magnetizing inductor current i_{Lm}. However, from the visual point of view, it is much more difficult to understand the trajectory loci in the 3D state-space than in the 2D state-plane. Moreover, it is complicated to get the trajectory's mathematic expression in the state-space.

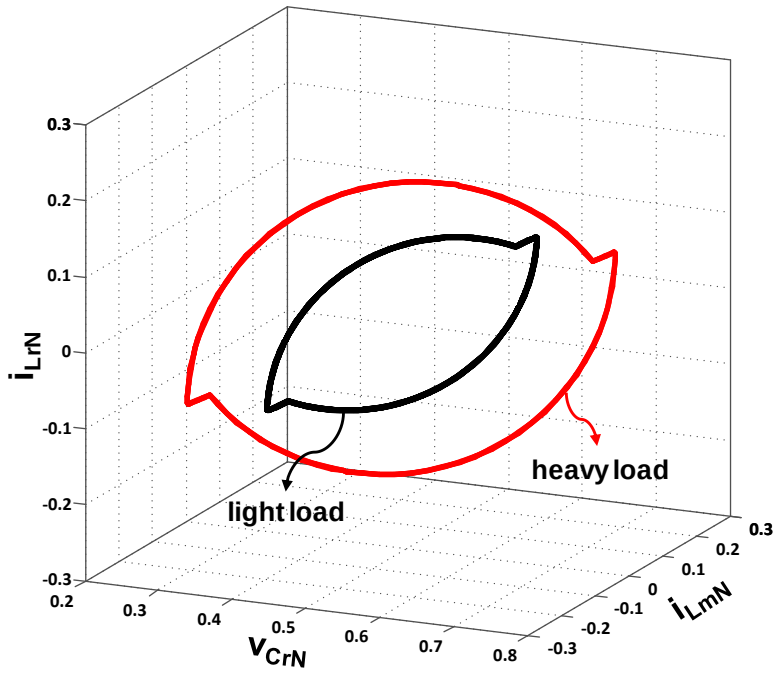


Fig. 1.12 3D state-space of LLC resonant converter

Therefore, it is better to illustrate all state variables of multi-element resonant converters in a 2D state-plane. Fig. 1.13 shows a LLC-type series resonant converter. When it works at a certain frequency point, the 3-element resonant tank can be simplified to a series resonant tank with an equivalent resonant inductor L_{eq}. Thus, the resonant capacitor voltage v_{Cp} and the resonant current through the equivalent inductor i_{Leq} can be represented in a 2D state-plane [B.12].

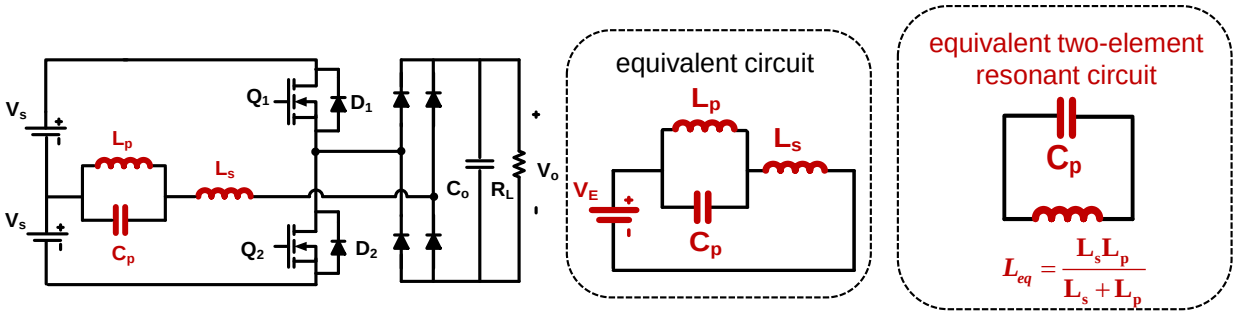


Fig. 1.13 Simplification of LLC-type series resonant converter to a series resonant converter

Similarly, a LCC-type parallel resonant converter can be simplified as well at a certain frequency point as shown in Fig. 1.14 [B.13].

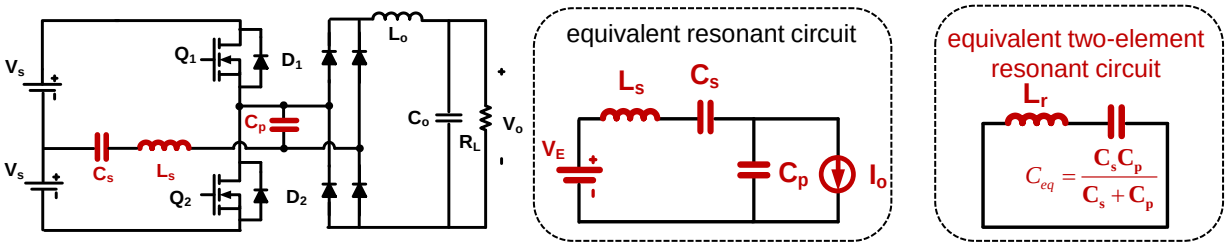


Fig. 1.14 Simplification of LCC-type parallel resonant converter to a series resonant converter

However, to analyze the LLC steady-state, load transient response, soft start-up, over-load protection, etc., the dynamic behavior of the LLC resonant tank should be investigated under all operation frequency regions, which cannot be simplified into a series resonant converter with an equivalent resonant inductor and a resonant capacitor. It is a challenge to find an approach to represent all state variables (i.e. v_{Cr}, i_{Lr} and i_{Lm}) clearly on a 2D state-plane under all operation conditions.

1.2.2 LLC transient response improvement

The optimal trajectory control (OTC) shows the best dynamic performance for the SRC under load transients. However, the realization of OTC is difficult to implement [B.8] [B.10]. As shown in Fig. 1.15, the centers of Q_1 and Q_2 conduction trajectory loci need to be determined by sensing the input voltage v_s and the output voltage v_o using analog-to-digital conversions (AD). The control variable R also needs to be calculated at every instantaneous value of the resonant current i_{Lr}, the resonant voltage v_{Cr}. Q_1 and Q_2 are turned on at the instants when R becomes equal to the reference R_{ref}. Since the on-line computation of variable R is nonlinear and complicated, it is hard to be implemented.

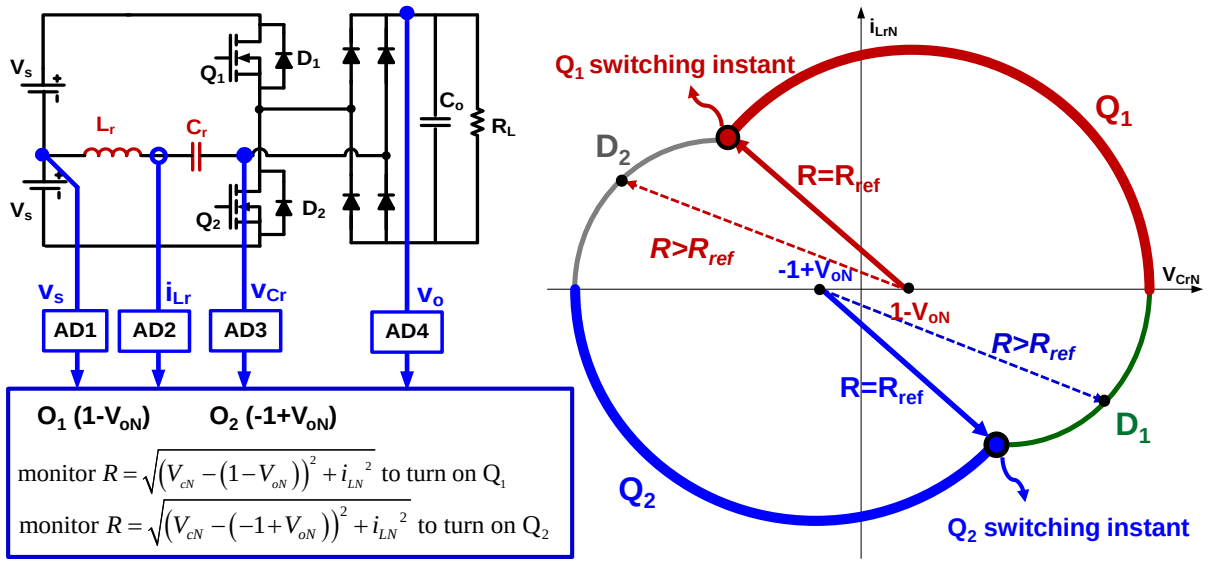


Fig. 1.15 Complicated implementation of OTC with nonlinear calculation of R

In order to reduce the control complexity, some simplified methods have been proposed for SRC. In [B.14] [B.16], the pseudo-linear form of the control variable R is introduced. In addition, some other linear combinations of the state variables to determine switching instants are proposed in [B.18].

When it comes to the multi-element resonant converters, such as the series-parallel resonant converter in [B.19], more state variables need to be sensed and a more complicated calculation is required., For the LLC resonant converter shown in Fig. 1.16, not only do the input voltage v_{in}, the output voltage v_o, the resonant current i_{Lr} and the resonant voltage v_{Cr} need to be sensed to determine the switching instants, but the magnetizing current i_{Lm} also needs to be sensed. Moreover, there are more operation modes in the LLC resonant converter, which increases the implementation complexity of the OTC.

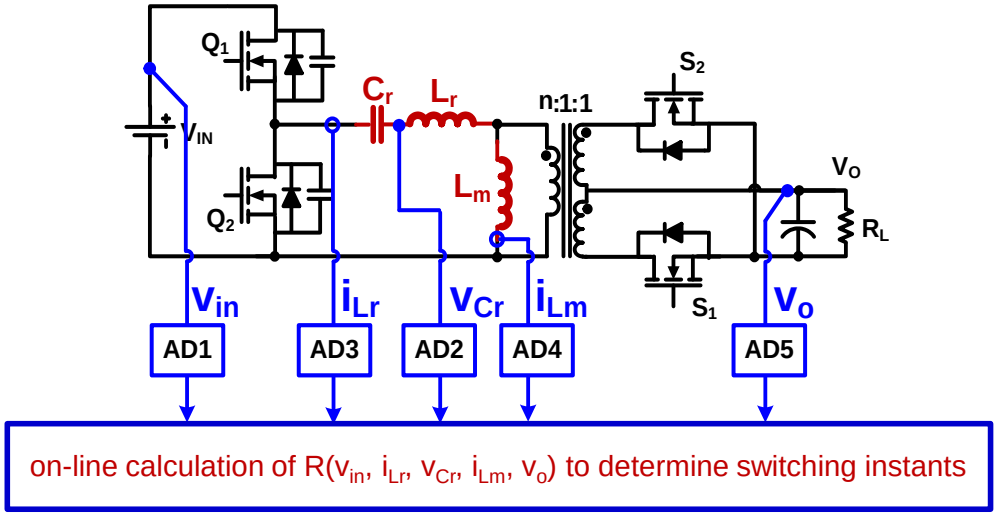


Fig. 1.16 Complicated implementation of OTC for LLC resonant converter

Therefore, a simplified realization of optimal trajectory control is needed. It is a challenge to find an implementation which can reduce the state variable sensors and eliminate the complicated nonlinear calculation while having a similar dynamic performance.

Besides the load transient, the LLC soft start-up is a highly dynamic process. The switching frequency has a wide range of variation during the soft start-up process. Initially, the switching frequency is pushed to a high value ($f_s>f_0$), to reduce the voltage and current stress in the

resonant tank. Then f_s decreases step by step, gradually moving to the resonant frequency point ($f_s=f_0$) to build up the output voltage.

The switching frequency f_s can be controlled to decrease linearly, piecewise-linearly or nonlinearly as shown in Fig. 1.17 [A.38-A.44]. Since the output voltage has been built up close to the steady state, the closed loop control signal f_{FB} will take over.

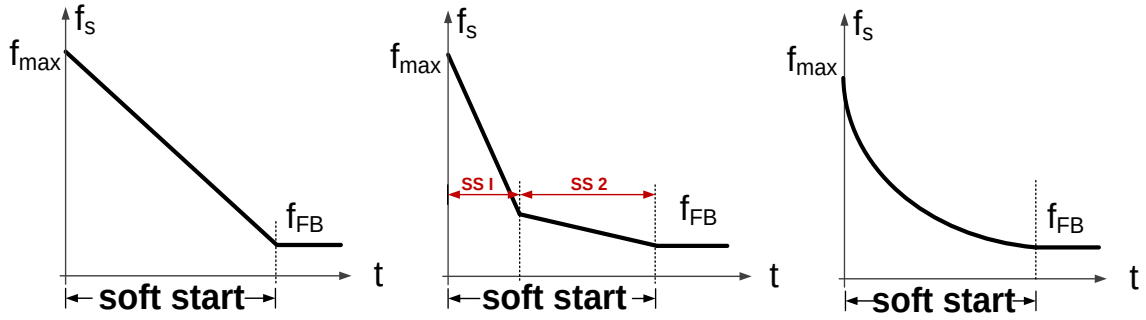


Fig. 1.17 Switching frequency arrangement during soft start-up

If the start-up frequency (f_{max}) is not high enough, there will be large voltage and current stress in the resonant tank at the start-up moment. Fig. 1.18 shows the experimental test of [A.38] [A.39], where the voltage and current stress is large in the resonant tank if starting-up with $1.5f_0$.

If the LLC starts up with a higher frequency ($f_{max}=5f_0$ as shown in Fig. 1.19) [A.40], at the beginning, the voltage and current stress is small. However, since the switching frequency (f_s) decreases too quick, large voltage and current stresses can still happen in the middle of the start-up process, which will trigger the over-current-protection (OCP). As a result, f_s will increase a bit to limit the stress, and then decreases smoothly to finish the soft start process. If f_s decreases slowly from $5f_0$, the stress will stay small, but the output voltage will build up slowly, which means the soft start-up process will take much longer.

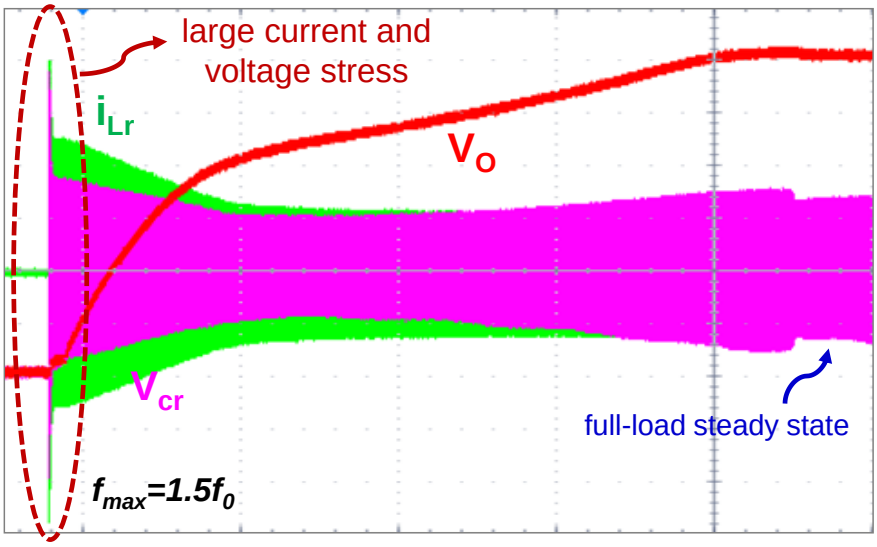


Fig. 1.18 LLC soft starts up with a low frequency

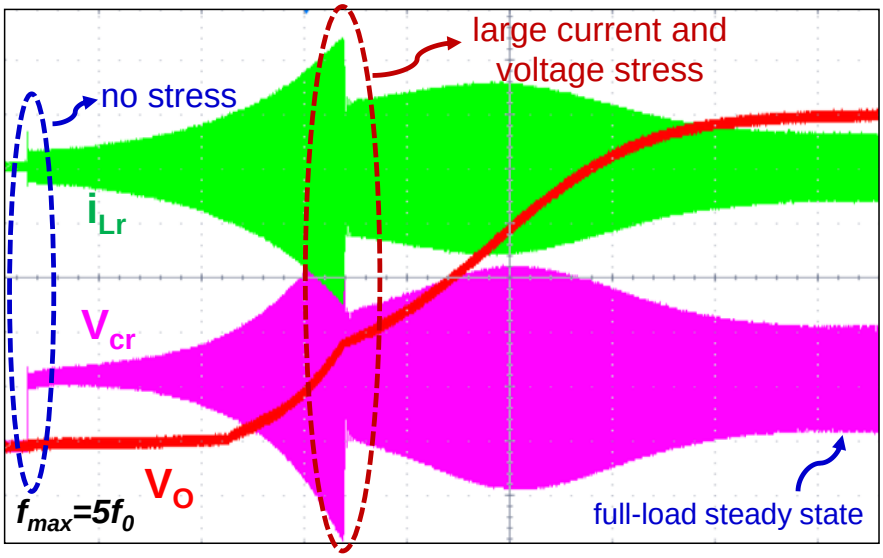


Fig. 1.19 LLC soft starts up with a high frequency

To limit the current and voltage stress while keeping switching frequency low, some phase-shifted controls [A.26] [A.27] and a PWM duty-cycle control [A.28] have been proposed for the LLC resonant converters. However, compared with frequency control, the LLC will lose zero-voltage-switching (ZVS) in the soft start-up duration.

Therefore, the dynamic behavior of the LLC soft start-up needs to be investigated. An optimal soft start-up process is required. Voltage and current stress should be limited during the soft start-up. Meanwhile, the output voltage should be built up smoothly and fast.

1.2.3 Light-load efficiency improvement

With the explosive increase in consumer electronics and IT equipment, the efficiency requirement of power converters is becoming higher and higher. Moreover, the efficiency demand is not only focused on the heavy load but also on the light load [A.13-A.15].

The LLC resonant converter can achieve very high efficiency under normal load conditions, because of ZVS for primary-side switches and ZCS for secondary-side rectifiers. However, the light-load efficiency still cannot meet the increasingly strict requirements, since certain load-independent losses such as driving losses and magnetic component core losses possess a much higher ratio under the light load condition.

Variable frequency control methods have been widely used to improve the light load efficiency in PWM converters, e.g. PWM/PFM control [C.1] [C.2], constant and adaptive on-time control [C.3], and burst mode control [C.4] [C.5]. The idea is to decrease the switching frequency or equivalent switching frequency, to reduce these load independent losses. To the LLC resonant converter, the burst mode control has been used to improve the light load efficiency, by periodically blocking the switch gate driving signals V_{gsQ1} and V_{gsQ2} as shown in Fig. 1.20.

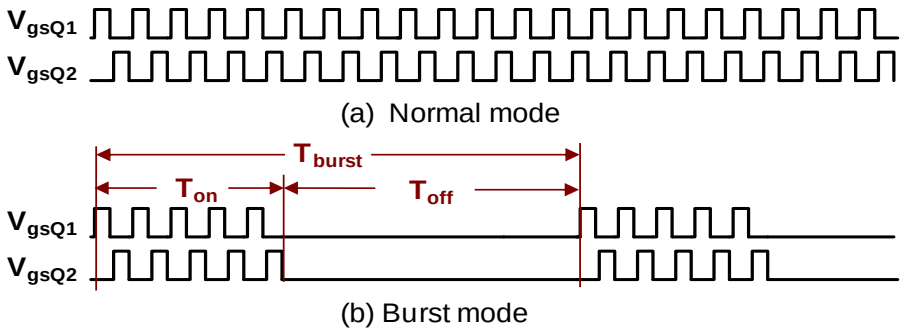


Fig. 1.20 Normal operation mode vs. burst mode

In the hysteresis burst mode [A.38-A.44] [C.5], the switches are periodically on and off, determined by the comparison between the feedback control command (f_{FB}) and the hysteresis band. When the load decreases, f_{FB} increases, that is, the LLC switching frequency (f_s) increases to regulate the output voltage. Until f_{FB} hits the hysteresis band ceiling, the LLC enters the burst mode, and the switches stop working. Then f_{FB} will decrease correspondingly. When it hits the band bottom, the switches start to work again. Although the implementation is simple, using f_{FB} to determine the light load condition is not accurate. Since it is influenced by the input voltage V_{in} and resonant tank parameters such as resonant inductor L_r, magnetizing inductor L_m, and resonant capacitor C_r. With different V_{in} and tank parameters, the light load conditions triggering the burst mode are different. Moreover, the design of the hysteresis band is critical. Large band induces a large output voltage ripple, and small band leads to low burst efficiency.

[C.6] [C.7] proposed the burst mode for the best light-load efficiency. Fig. 1.21 shows a typical efficiency curve of a LLC resonant converter. The best efficiency is achieved at I_{OPT} load point. When it comes to the light load I_{light}, if the burst duty D_{burst} is determined as

$$D_{burst} = \frac{T_{on}}{T_{burst}} = \frac{I_{light}}{I_{OPT}}, \tag{1.1}$$

where T_{on} is the burst on-time, T_{burst} the burst period as shown in Fig. 1.20, the LLC will treat the equivalent load as I_{OPT} during the burst on-time. Thus, the best efficiency can be achieved under the light load conditions.

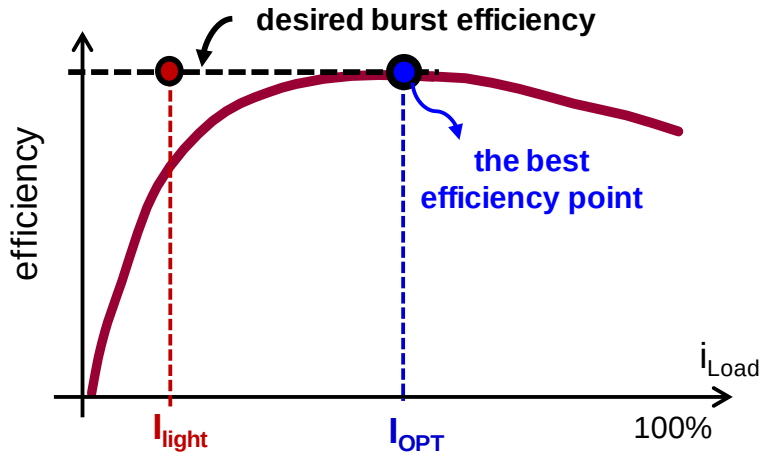


Fig. 1.21 Desired burst efficiency

However, as shown in Fig. 1.22, due to the fast dynamic characteristic of the resonant tank, there is a serious oscillation when LLC starts to work from the burst-off idle status. The LLC equivalently works from heavy load I_{eq1} to light load I_{eq5}, and the steady state of the optimal load I_{OPT} cannot be fixed. Consequently, the burst efficiency is the average efficiency from the load I_{eq1} to I_{eq5}, which is $\Delta\eta$ less than the desired value.

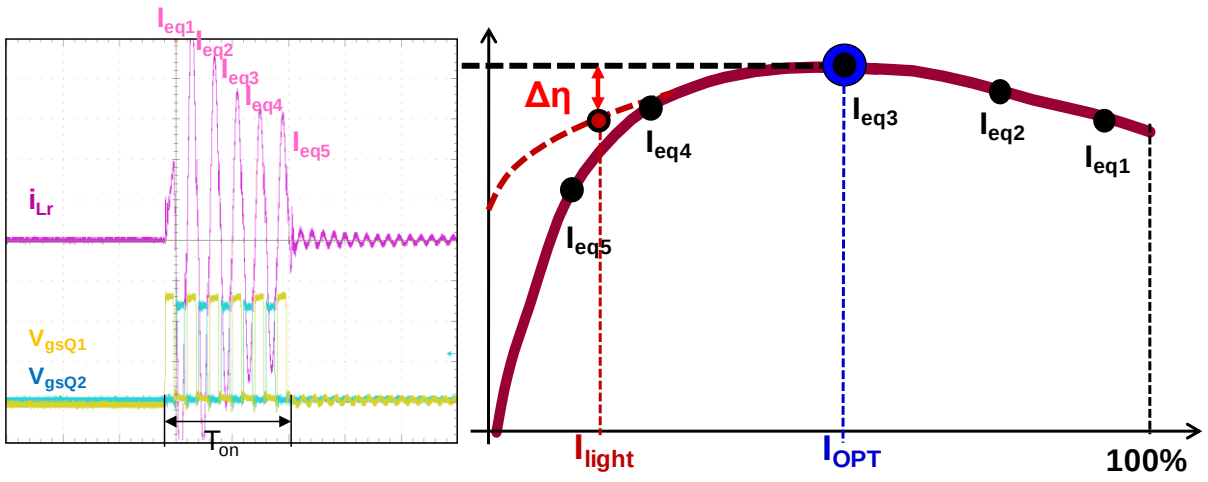


Fig. 1.22 Dynamic oscillation during burst-on time

Moreover, if the burst period T_{burst} stays constant, when the light load becomes heavy, T_{on} will increase according to (1.1), resulting in a large output voltage ripple. Therefore, an additional low-pass filter needs to be added on the output side. In another burst control method [C.8], the burst on-time stays constant, but the off-time is modulated according to different light loads, so the output voltage ripple stays the same. However, without considering (1.1), it cannot treat equivalent load as I_{OPT} to maintain good efficiency.

Therefore, to achieve good light-load efficiency, the challenge is how to design the burst mode to make the LLC always operate at the best efficiency load point. Meanwhile, the output voltage low frequency ripple should be minimized.

Besides a voltage-source power supply, the LLC resonant converter can well serve as constant current source. Fig. 1.23 shows a multi-channel constant current (MC^3) LLC resonant converter for LED driver [A.19]. The multiple transformer structure (primary windings are in series and secondary windings are in parallel) enables the cross regulation by only controlling

one LED channel. The voltage-doubler configuration allows each transformer to driver two LED strings at the same time and hence reduces the number of transformers by half. The DC block capacitor (C_{dc}) is used for the purpose of precise current sharing between two neighboring LED channels.

Like the conventional voltage source LLC resonant converter, the switching frequency (f_s) is controlled to achieve different dimming ratios [A.19]. Normally, under the full-load condition, the MC^3 LLC resonant converter is designed to operate near the resonant frequency point (f_s=f_0) to achieve the best efficiency. When the switching frequency f_s increases, the LED dimming ratio becomes low, that is, it comes to the light load condition. However, as shown in Fig. 1.24, the current gain becomes flat as f_s increases. Even when pushing f_s to as high as $5f_0$, only 18% full load dimming is achieved. Meanwhile, the efficiency drops quickly as the dimming ratio decreases, since the switching losses and driving losses increases dramatically.

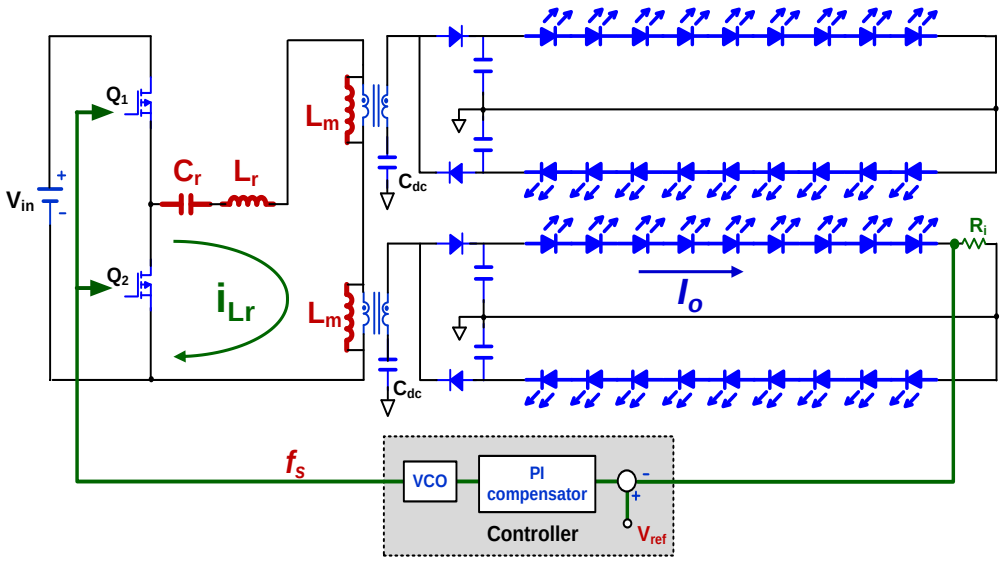


Fig. 1.23 MC^3 LLC resonant LED driver

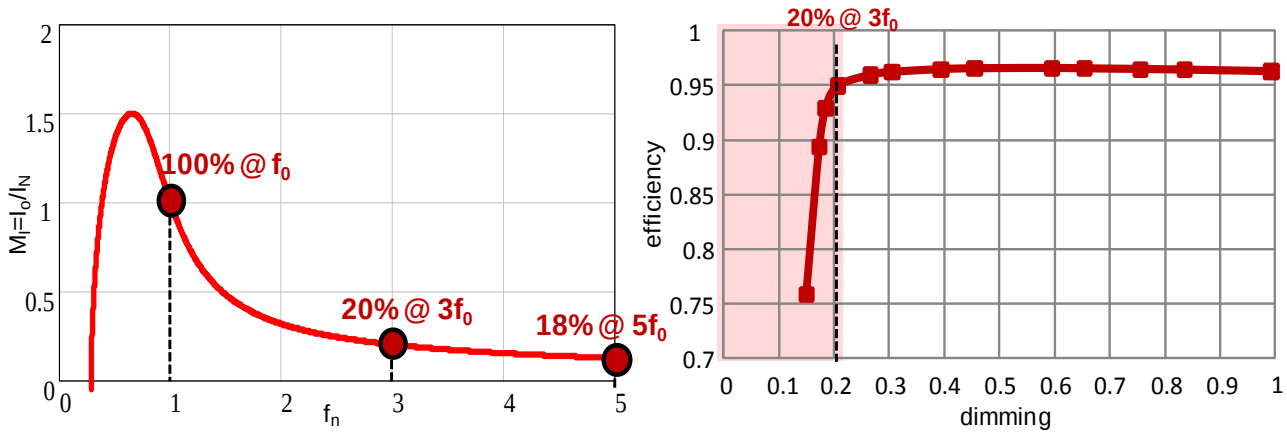


Fig. 1.24 Low efficiency under low dimming ratio

Compared with the switching frequency controlled analog dimming, the PWM dimming approach can achieve much a lower dimming ratio by minimizing the PWM duty cycle D_{PWM}, as shown in Fig. 1.25. Moreover, the LLC can always operate under the full-load condition during the PWM dimming on-time, thus the efficiency stays higher even if the dimming ratio becomes very low. In addition, there is no chromaticity shift when using the PWM dimming [D.5].

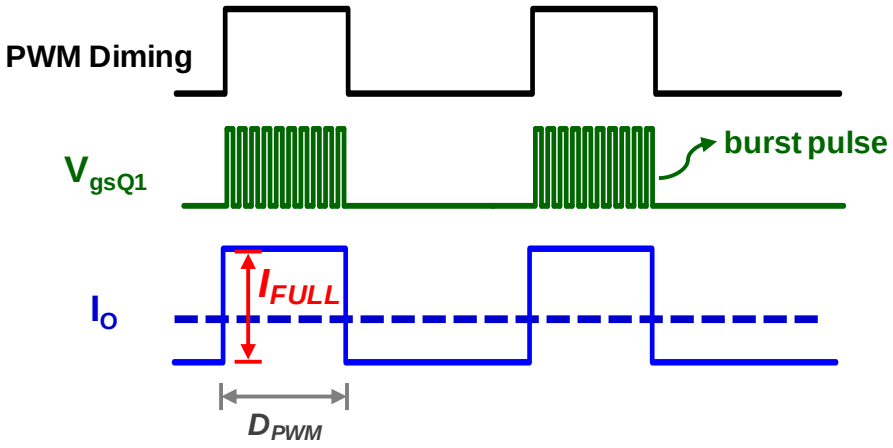


Fig. 1.25 LED PWM dimming

However, as is similar to the burst mode shown in Fig. 1.22, due to the fast dynamic characteristics of the LLC resonant tank, there will be oscillations as the MC^3 LLC LED driver switches between the working status and the idle status. As shown in Fig. 1.26, the oscillation of the resonant current i_{Lr} will increase the RMS value, which produces additional conduction losses. Moreover, the oscillation on the output current will reduce the control accuracy of the LED intensity.

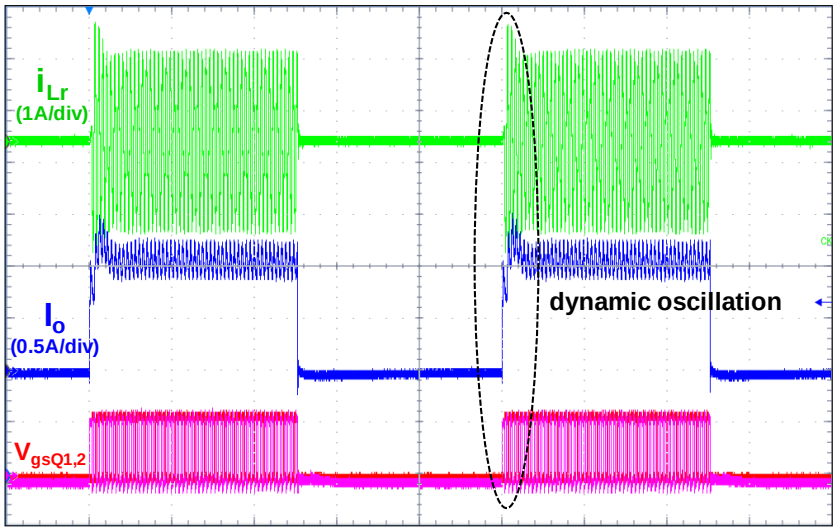


Fig. 1.26 LLC LED driver dynamic oscillation in PWM dimming

In order to maintain the high efficiency and control the LED lighting intensity accurately within the whole dimming range, the burst pulse pattern during the PWM dimming on-time needs to be optimized to minimize the dynamic oscillation.

1.2.4 Inteligent synchrnous rectifier (SR) driving scheme

To improve the LLC resonant converter overall efficiency, the synchronous rectifiers (SR) should be employed. The desired SR gate driving signals for the LLC resonant converter are

shown in Fig. 1.27. In different switching frequency regions, when the primary main switches Q_1 and Q_2 are turned on, the secondary side current i_{SEC} starts to go through the SRs, thus the SRs should be turned on synchronously with the main switches. However, the turn-off times of the SRs and the main switches are not exactly in phase. When operating below the resonant frequency (i.e. $f_s<f_0$), the SR should be turned off earlier than the main switch. Otherwise, the SR would conduct circulating energy, namely a reverse current from the load to the source, thus producing a greater increase in the RMS currents and turn-off current, and causing efficiency to deteriorate dramatically. When operating above the resonant frequency ($f_s>f_0$), the SR should be turned off a bit later than the main switch. Otherwise, the sharply decreased current would go through the paralleled body diode, resulting in a serious reverse recovery.

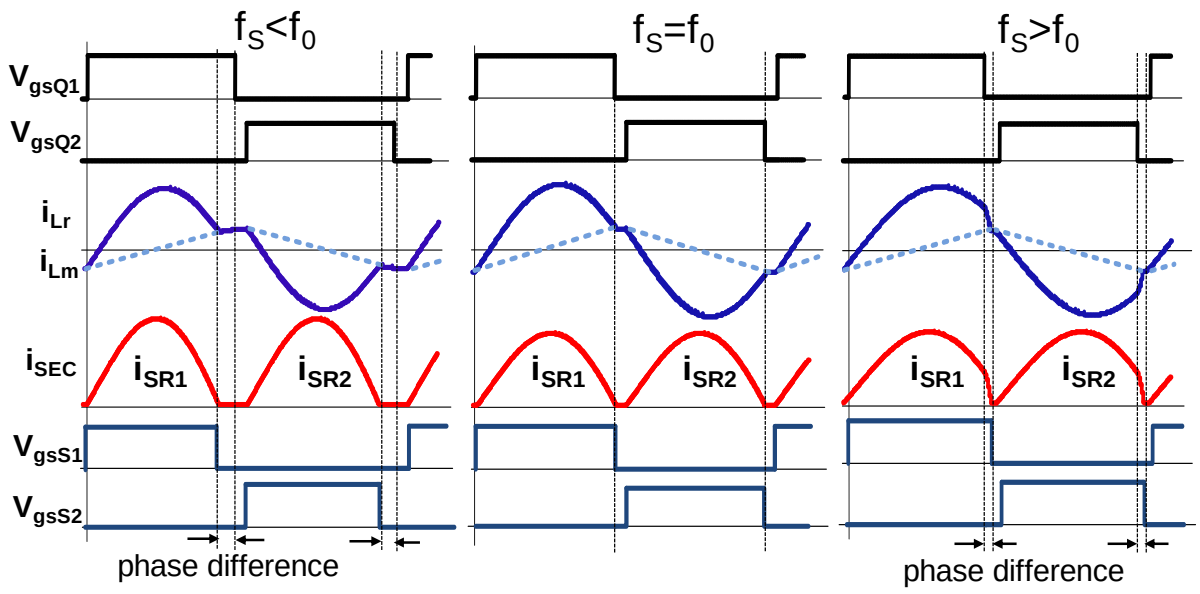


Fig. 1.27 Desired SR gate driving signals in different switching frequency regions

Therefore, the gate driving signals of SRs and main switches cannot derive from the same signal for controlling the conduction times as those in the PWM converters, so a special driving arrangement for the SR is required for the LLC resonant converters [E.1]-[E.8].

One solution [E.1] is based on the SR current i_{SR} sensing by transformers to generate the SR driving signal. The method is precise, but due to the large current on the secondary side, it requires a large size current transformer and it presents a lower efficiency due to the extra resistance of the transformer windings.

An alternative solution [E.2] is sensing current through the transformer's primary side winding. Provided that the inductance L_r and L_m are external to the main transformer, the primary side current is a precise replica of the secondary side current. Although a smaller loss could be achieved when compared to the secondary side current sensing, three magnetic components are needed, losing the integration of leakage, magnetizing inductors and transformer in a single element.

In [E.3], the author proposed a novel primary side resonant current i_{Lr} sensing method to determine the SR gate driving signals. However, it needs to decouple the magnetizing current i_{Lm}, and thus an additional complicated circuit is added.

A promising driving method is based on the SR drain to source voltage. The sensed SR V_{ds} is processed by the control circuits as follows [E.4]:

- before the SR is turned on, the paralleled body diode conducts shortly and there is a large forward voltage drop, which is compared with a threshold voltage V_{th_on} to turn on the SR;

- when the SR current is decreasing toward zero, the SR V_{ds} also becomes small, which is then compared with another threshold voltage V_{th_off} to turn off the SR.

However, the accuracy of this driving scheme is highly affected by the SR package [E.5] [E.6]. Due to the inevitable package inductance, the sensed terminal drain to source voltage of the SR is actually the sum of the MOSFET's on status resistive voltage drop and the package inductive voltage drop. Fig. 1.28 shows that the sensed $V_{d's'}$ of the SR terminal deviates greatly from the purely resistive voltage drop V_{ds} of the MOSFET. Thus, the actual SR drive signal V_{gsSR} is significantly shorter than the expected value.

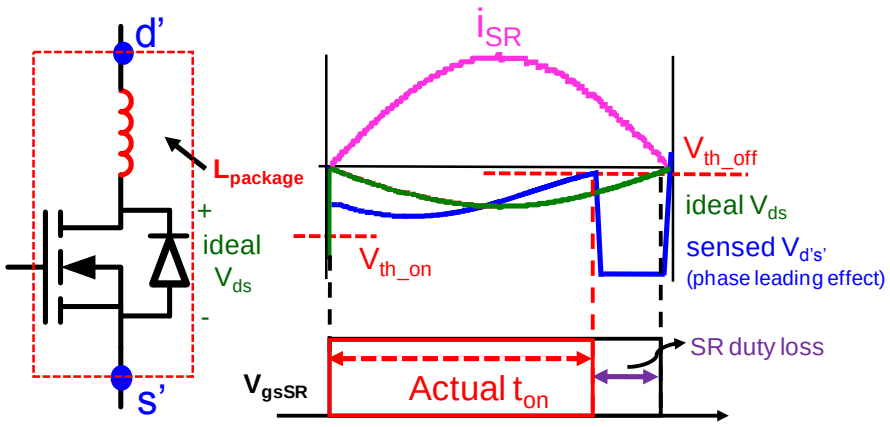


Fig. 1.28 Early turn-off effect of package inductance

To compensate for the inductive characteristic of the sensed $V_{d's'}$, a carefully designed capacitive network can be connected to the sensed terminals [E.6], as shown in Fig. 1.29.

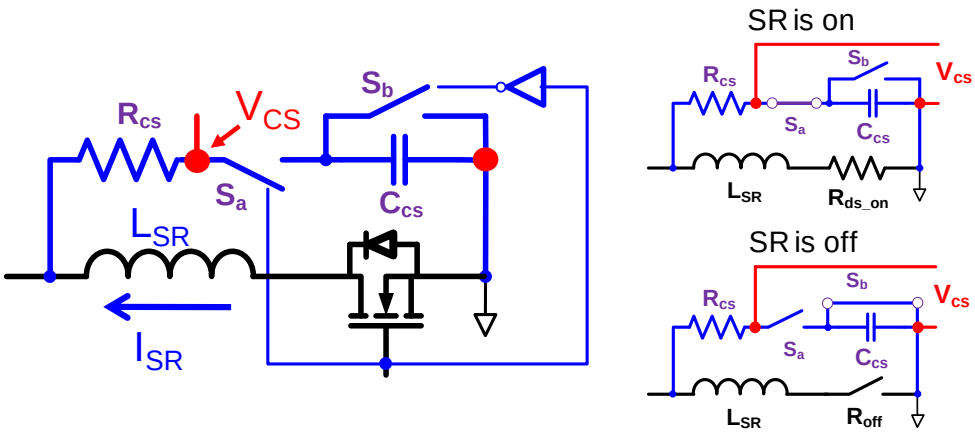


Fig. 1.29 The capacitive compensator network

However, the package inductance L_{SR} and the pure resistor R_{ds_on} need to be determined in advance to calculate the parameters of the components: C_{CS} and R_{CS} in the capacitive network. Although the inductive phase lead influence is diminished, the design and the parameter tuning are complicated.

Different from the above mentioned V_{ds} sensing, in [E.7],[E.8] the SR body diode forward voltage drop is detected to tune the gate driving signal. As shown in Fig. 1.30, V_{gsQ} is the primary main switch driving signal, and it synchronizes the sawtooth waveform V_{saw}, which is then compared with a control signal V_c to generate the SR driving signal V_{gsSR}. If the body diode conducts, the large forward voltage drop is sensed by the valley detection circuit; then V_c increases, and V_{gsSR} pulse width increases accordingly. Finally, the SR is tuned until the circuit cannot detect the body diode conduction. However, the maximum pulse width of the SR driving signal cannot be larger than that of the main switch, and thus it cannot be used when $f_s>f_0$. As shown in Fig. 1.27, the SR pulse width should be tuned slightly larger than the main switch when $f_s>f_{0.}$ Moreover, the design process of the analog compensator to generate V_c is complicated.

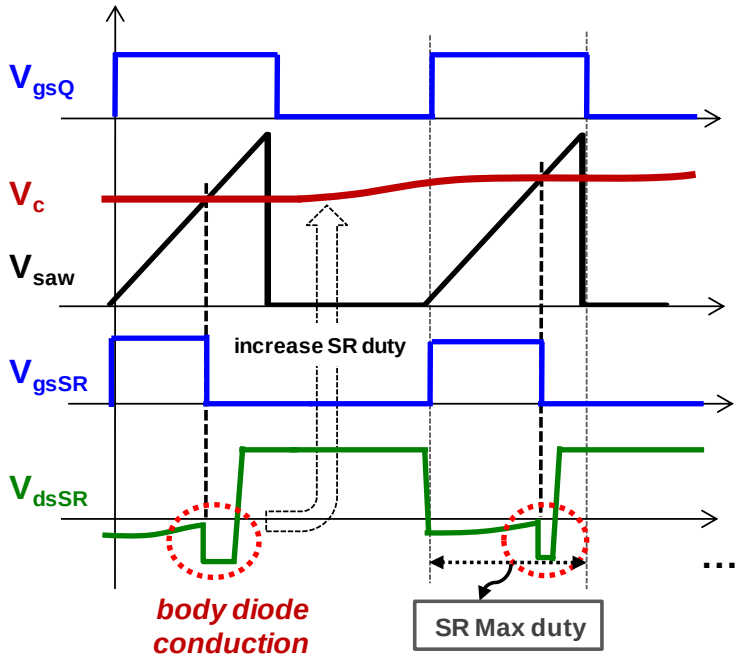


Fig. 1.30 Paralleled body diode conduction elimination for SR tuning

Therefore, an intelligent SR driving scheme is required, which can control the SR gate driving signal in the whole switching frequency regions with simple implementation.

1.2.5 Resonant frequency tracking for unregulated LLC (LLC-DCX)

In the typical distributed power architecture, the power delivery path from the input to the load subsystems is generally equipped with a front-end converter and multiple point-of-load converters (POLs). Previously, the front-end converter has been a fully-regulated multiple-output power supply for providing the power to the system board, the hard drives and the cooling fans. However, the system board employs many POLs to locally regulate the load subsystem voltages. Thus, the front-end converter is no longer involved in the voltage regulation of the load. From this configuration, we can see that the front-end power supply does not need to be a fully regulated power supply. The traditional front-end converter could be replaced by a dc-dc

transformer (DCX); that is, a semi-regulated or unregulated single-output dc-dc converter. POLs on the system board generally accept the input of 12V ±10%. Being a single-output design with a standard voltage of 12V, the DCX can be made as a standard product. In addition, the modular design concept allows for system expansion without entirely re-designing the unit.

The ever-present trend for distributed power systems is the pursuit of higher efficiency and power density. Recently, Intel proposed a 400 Vdc direct-distribution bus for data center applications in order to reduce the number of power conversion stages and the power loss in the power distribution path [A.1] [A.2] [A.9] [A.10] [A.12]. By eliminating an AC uninterruptible power supply (UPS) and a transformer in the power distribution unit (PDU), the overall efficiency can be improved by 3-5%. With the emerging 400 Vdc bus and the proposed front-end unit based on DCX, the alternative power architecture can be depicted using Fig. 1.31.

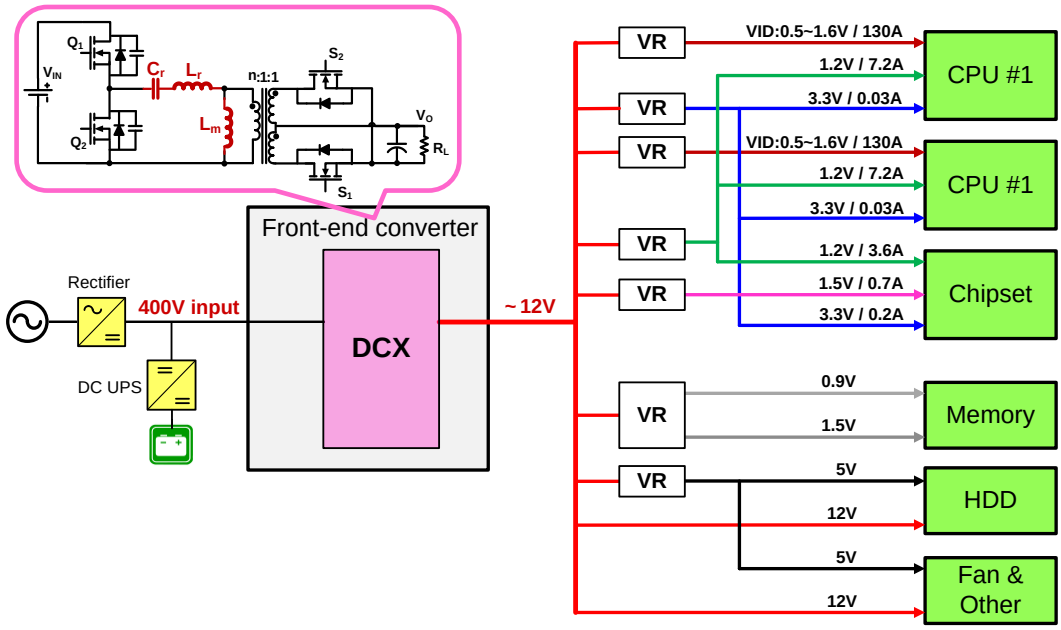


Fig. 1.31 400 Vdc distributed power architecture based on the modularly designed DCX

Serving as a DCX, the LLC has no feedback loop to maintain the output voltage. Thus, it is better to fix f_s exactly at the resonant frequency point ($f_s=f_0$) to achieve the best efficiency [A.33] [A.37] [F.1-F.4]. As shown in Fig. 1.32, with the same output power, if the LLC-DCX works below the resonant frequency ($f_s<f_0$), there is more circulating energy in the resonant tank. As a result, the switches will conduct more RMS current, producing more conduction losses. If the LLC-DCX works above the resonant frequency ($f_s>f_0$), the main switches will turn off with a higher current, resulting in more switching losses. More seriously, sharply decreased secondary-side current will cause some reverse-recovery in the SR paralleled body diode, further reducing the efficiency. Therefore, the LLC-DCX should work at point f_0 ($f_s=f_0$) to achieve the best efficiency.

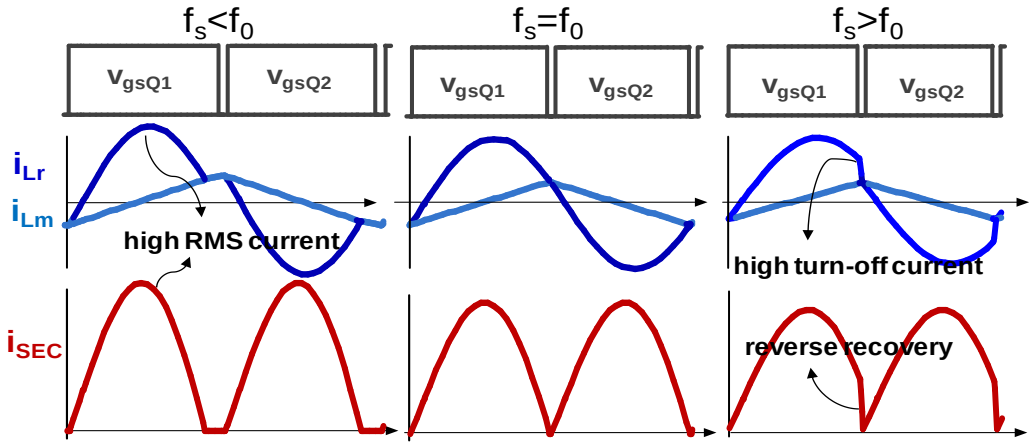


Fig. 1.32 Illustration of the best efficiency at the resonant frequency point

In the ideal condition, the LLC resonant frequency f_0 can be calculated as

$$f_0 = \frac{1}{2\pi\sqrt{L_r C_r}}, \tag{1.2}$$

where L_r and C_r are the resonant inductor and resonant capacitor, respectively.

However, in practical mass production, L_r and C_r always have some tolerances and aging effect. As a result, it is impossible to operate exactly at point f_0 all the time with the calculated value in (1.2). Therefore, the resonant frequency f_0 needs to track automatically.

Phase-locked loops (PLLs) have been widely used in parallel resonant converters (PRC) and serial resonant converters (SRC) for resonant frequency tracking [F.5],[F.6]. The resonant frequency is tracked by tuning the switching frequency to eliminate the phase difference between the resonant current and the main switch gate driving signals. However, as shown in Fig. 1.33, in the LLC resonant converter, due to the magnetizing current i_{Lm}, when working at the resonant frequency point ($f_s=f_0$), the resonant current i_{Lr} is not in phase with V_{gsQ1} and V_{gsQ2} ($\Delta\Phi$ is the difference). Thus, the PLL method cannot be used to track the LLC resonant frequency.

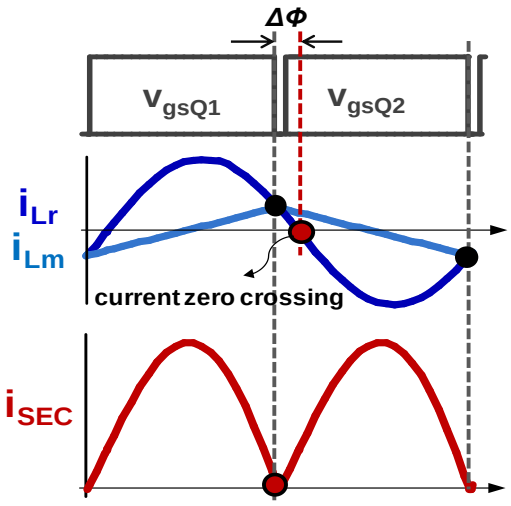


Fig. 1.33 Phase difference between the resonant current and driving signal in LLC

As show in Fig. 1.32, if $f_s=f_0$, and at the moment Q_1 and Q_2 are turned off, the resonant current i_{Lr} touches the magnetizing current i_{Lm}. Thus, these touching points can be sensed to turn

off Q_1 and Q_2. But i_{Lm} cannot be physically detected, since the magnetizing inductor L_m is always integrated with the transformer. Consequently, some other complicated circuits are proposed to predict i_{Lm} in [F.3], [F.4]. However, L_m will have a certain tolerance, as will L_r and C_r, thus the prediction of the touching point is not accurate.

Although the resonant current i_{Lr} is not in phase with the Q_1 and Q_2 gate-driving signals, the secondary-side current i_{SEC} is in phase with V_{gsQ1} and V_{gsQ2} when $f_s=f_{0,}$ as shown in Fig. 1.33. Therefore, the secondary-side current zero-across point can be sensed to track f_0. This method is precise, but due to the large current on the secondary side, it requires a large current transformer and is less efficient due to the extra resistance of the transformer windings.

Therefore, an automatic resonant frequency tracking method is required to let the LLC-DCX always operate at the optimal switching point ($f_s=f_0$).

1.3 Dissertation Outline

Taking into account the challenges raised during the review of the existing literature on the control of LLC resonant converters, several issues have been addressed in this dissertation.

Chapter 1: Research background, motivation, and literature review.

Chapter 2:

2-1. The 2D state-plane analysis for LLC resonant converters is proposed;

2-2 The steady-state and transient trajectories are presented in the state plane.

Chapter 3:

3-1.To improve the load transient response, a simplified optimal trajectory control (SOTC) is proposed;

3-2. The hybrid control scheme of SOTC is implemented in a digital controller.

Chapter 4:

4-1. At the start-up moment, several switching patterns are proposed for initial condition settling of the LLC resonant tank.

4-2. During the soft start-up process, the optimal switching frequency is estimated based on a graphical state-trajectory analysis.

Chapter 5:

5-1. To improve the LLC light-load efficiency, an optimal burst mode is implemented for the best light-load efficiency.

5-2. For the PWM dimming of the LLC resonant LED driver, the burst pulses during the PWM dimming on-time are optimized to minimize dynamic oscillations.

Chapter 6:

6-1. An intelligent synchronous rectifier (SR) driving scheme is proposed for the LLC full-range operation by eliminating the SR paralleled body diode conduction.

6-2. For LLC-DCX applications, the resonant frequency is automatically tracked based on the well-tuned SR gate-driving signal.

Chapter 7: Conclusion and future work.

Chapter 2. State-Plane Analysis of LLC Resonant Converters

In this chapter, the operation of LLC resonant converter is introduced. The LLC trajectory in the three-dimension (3D) state-space is simplified to the trajectory in the 2D state-plane, while keeping all state variable information. The steady-state and dynamic trajectories are illustrated.

2.1 Introduction

The state plane has been verified as a useful tool to analyze the steady state and transient behaviors of a class of resonant converters [B.7-B.19]. For the two-element resonant converters, such as the series resonant converter (SRC) and the parallel resonant converter (PRC), there are only two state variables (i.e. i_{Lr} and v_{Cr}) in the resonant circuits. Thus, it is easy to present the state-trajectory in a 2D state-plane [B.7]. After that, some optimal trajectory control approaches can be implemented to improve the dynamic performance [B.8] [B.9].

When it comes to multi-element resonant converters, like series-parallel resonant converters (SPRC), LCC-type parallel resonant converters, and etc., there are more than two state variables in the resonant circuits. Therefore, more than two dimension coordinates are required to present all the state variables [B.19]. However, it is much more difficult to understand and mathematically analyze the trajectory loci in the multi-dimension state-space than in the 2D state-plane. Some simplification methods have been applied to get the equivalent resonant capacitor or the resonant inductor, but they are only valid in certain operating points [B.12-B.13].

To analyze the LLC steady-state, load transient response, soft start-up, over-load protection, etc., the behavior of LLC resonant tank should be investigated in all operation frequency regions. Fig. 2.1 shows the operation of the LLC resonant converter. When it works at and above the resonant frequency point ($f_s=f_0$ & $f_s>f_0$), the magnetizing inductor L_m is clamped by the output voltage, which is decoupled from the resonance. Thus, the resonant tank behaves a series resonant circuit of C_r and L_r. When the LLC works in below the resonant frequency region ($f_s<f_0$), during some intervals, L_m is in series with L_r, joining in the resonance. Therefore, the LLC resonant tank cannot be simply treated as a two-element resonant circuit with an equivalent resonant inductor and a resonant capacitor.

Therefore, a new approach should be investigated to represent all state variables (i.e. v_{Cr}, i_{Lr} and i_{Lm}) clearly in a 2D state-plane under all operation conditions.

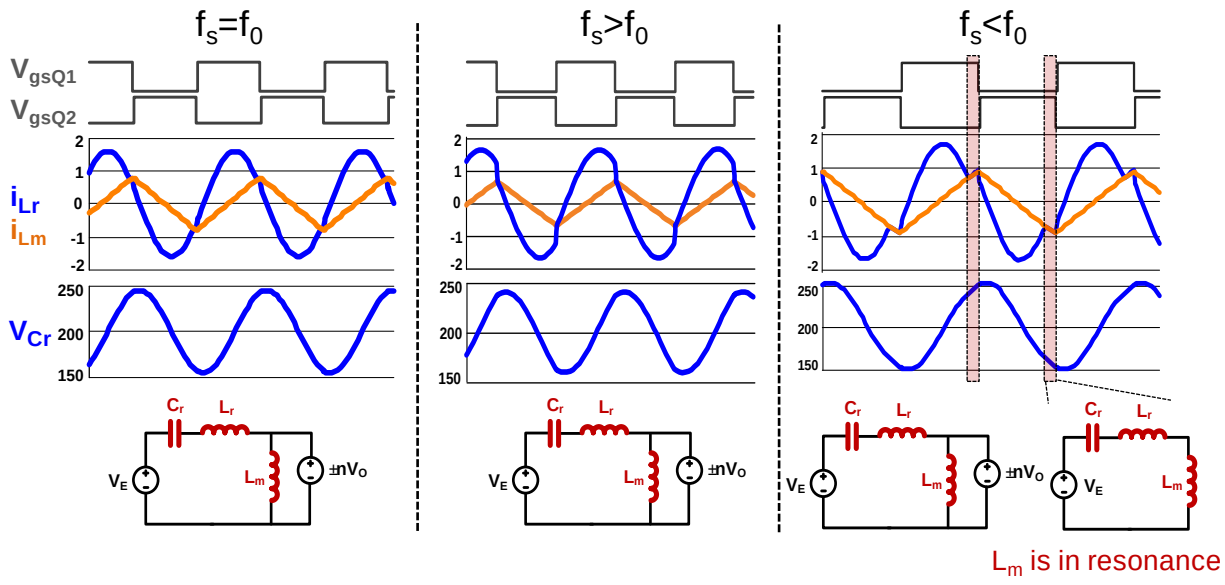


Fig. 2.1 Operation of LLC resonant converter

2.2 LLC Steady-State Trajectory in 2D State-Plane

From the operation of the LLC resonant converter as in Fig. 2.1, when the magnetizing inductor L_m is clamped by the output voltage, the magnetizing current i_{Lm} is linearly controlled by the output voltage V_o. When L_m is in the resonant interval, it is in series with L_r, thus i_{Lm} is equal with the resonant current i_{Lr}. Instead of an independent state variable, i_{Lm} can be represented by V_o and i_{Lr}. Therefore, a 2D state-plane trajectory is possible to analyze all state variables in the LLC resonant tank. As shown in Fig. 2.2, by projecting the state-space trajectory to the i_{LrN}-v_{CrN} state-plane, both i_{Lr} and v_{Cr} state variable information are kept. Meanwhile, the i_{Lm} can be represented by i_{Lr} when L_m is in the resonant process.

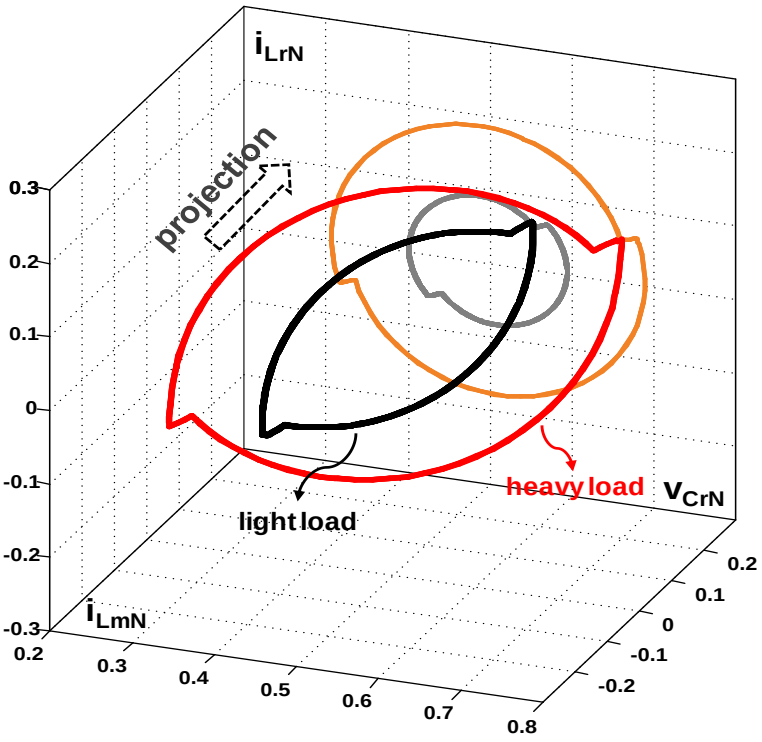


Fig. 2.2 Simplification of 3D state-space to 2D state-plane trajectory

To simplify the i_{Lr}-v_{Cr} state-plane analysis, it is assumed that the output capacitor is large enough so that the output voltage (V_o) remains constant. A second assumption is that the circuit losses, including the resonant tank, switch and filter losses, are negligible.

Within the whole switching frequency region, the LLC resonant converter can be viewed as a piecewise linear system switching among six possible operation modes. When Q_1 is on, there are three operation modes as shown in Fig. 2.3.

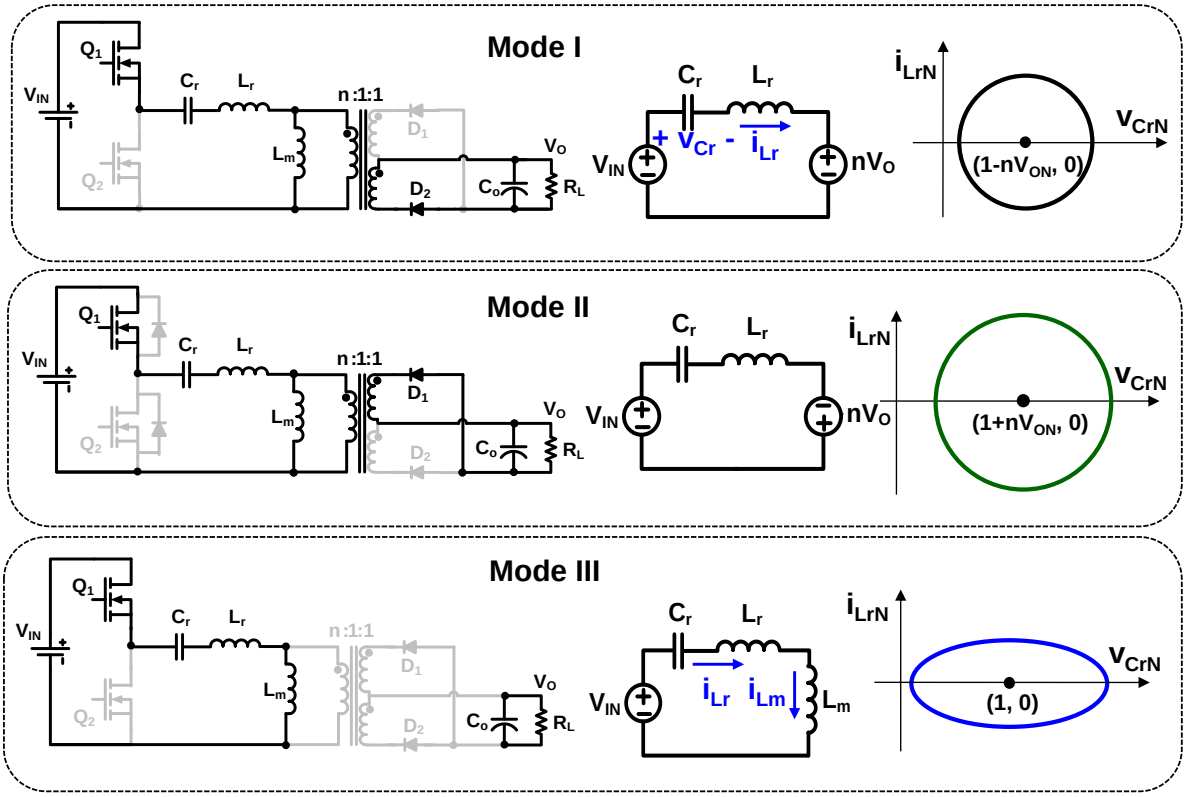


Fig. 2.3 Operation modes and corresponding trajectories when Q_1 is on

- Mode I:

The primary switch Q_1 turns on, and the resonant current flows through the secondary-side rectifier D_2. In this mode, the magnetizing inductor L_m is clamped by the output voltage. The

equivalent circuit is shown in Fig. 2.3, where the resonant capacitor C_r and the resonant inductor L_r form the series resonant tank. The source voltage across the resonant tank is V_{in}-nV_o.

Thus, we can write:

$$\dot{v}_{Cr} = \frac{1}{C_r} i_{Lr} \tag{2.1}$$

$$\dot{i}_{Lr} = -\frac{1}{L_r} v_{Cr} + \frac{1}{L_r}(V_{in} - nV_o) \tag{2.2}$$

where v_{Cr} and i_{Lr} are the resonant capacitor voltage and resonant inductor current. Combining (2.1) and (2.2), v_{Cr} and i_{Lr} can be expressed as:

$$v_{Cr} - (V_{in} - nV_o) = I_{Lr0} \cdot Z_0 \cdot \sin[\omega_0(t - t_0)] + [V_{Cr0} - (V_{in} - nV_o)] \cdot \cos[\omega_0(t - t_0)] \tag{2.3}$$

$$i_{Lr} = I_{Lr0} \cdot \cos[\omega_0(t - t_0)] - \frac{V_{Cr0} - (V_{in} - nV_o)}{Z_0} \cdot \sin[\omega_0(t - t_0)]. \tag{2.4}$$

where V_{Cr0} and I_{Lr0} are the initial conditions at time $t=t_0$, $Z_0 = \sqrt{L_r / C_r}$ is the characteristic impedance, and $\omega_0 = 1/\sqrt{L_r C_r}$ is the resonant frequency.

By normalizing all voltages with the voltage factor V_{in}, and all currents with the current factor V_{in}/Z_0 in (2.3) and (2.4), the following expressions are derived:

$$v_{CrN} - (1 - nV_{oN}) = I_{Lr0N} \cdot \sin[\omega_0(t - t_0)] + [V_{Cr0N} - (1 - nV_{oN})] \cdot \cos[\omega_0(t - t_0)] \tag{2.5}$$

$$i_{LrN} = I_{Lr0N} \cdot \cos[\omega_0(t - t_0)] - [V_{Cr0N} - (1 - nV_{oN})] \cdot \sin[\omega_0(t - t_0)]. \tag{2.6}$$

The subscript N in (2.5) and (2.6) refers to normalized circuit variables.

From (2.5) and (2.6), the trajectory equation is given by:

$$\left[v_{CrN} - \left(1 - nV_{oN}\right)\right]^2 + {i_{LrN}}^2 = \left[V_{Cr0N} - \left(1 - nV_{oN}\right)\right]^2 + {I_{Lr0N}}^2 , \tag{2.7}$$

which behaves as a circle as shown in Fig. 2.3. The center ($1-nV_{oN}$, 0) is determined by the source voltage across the tank, and radius depends on the initial conditions: V_{Cr0} and I_{Lr0}, which reflects the energy in the resonant tank.

- Mode II

In Mode II, Q_1 is on, but the current flowing through the secondary side changes its direction. This occurs when the switching frequency is larger than the resonant frequency (i.e. $f_s > f_0$). This mode is similar to Mode I, but the source voltage across the resonant tank changes to $V_{in} + nV_o$.

Similar to Mode I, the trajectory expression is given by:

$$\left[v_{CrN} - \left(1 + nV_{oN}\right)\right]^2 + {i_{LrN}}^2 = \left[V_{Cr0N} - \left(1 + nV_{oN}\right)\right]^2 + {I_{Lr0N}}^2 , \tag{2.8}$$

which behaves as a circle as well, but the center changes to ($1+nV_{oN}$, 0).

- Mode III:

In Mode III, Q_1 is on, but there is no current flowing through the secondary side. This mode occurs when $f_s < f_0$. In this mode, the magnetizing inductor L_m joins the resonance, and the

magnetizing current i_{Lm} can be represented by i_{Lr}. The source voltage across the resonant tank is V_{in}, and:

$$\dot{v}_{Cr} = \frac{1}{C_r} i_{Lr} \tag{2.9}$$

$$\dot{i}_{Lr} = -\frac{1}{L_r + L_m} v_{Cr} + \frac{1}{L_r + L_m} V_{in} \tag{2.10}$$

From (2.9) and (2.10), v_{Cr} and i_{Lr} in Mode III are given by:

$$v_{Cr} - V_{in} = I_{Lr0} \cdot Z_1 \cdot \sin[\omega_1 (t - t_0)] + (V_{Cr0} - V_{in}) \cdot \cos[\omega_1 (t - t_0)] \tag{2.11}$$

$$i_{Lr} = I_{Lr0} \cdot \cos[\omega_1 (t - t_0)] - \frac{V_{Cr0} - V_{in}}{Z_1} \cdot \sin[\omega_1 (t - t_0)], \tag{2.12}$$

where $Z_1 = \sqrt{(L_r + L_m)/C_r}$ is the characteristic impedance, and $\omega_1 = 1/\sqrt{(L_r + L_m)C_r}$ is the resonant frequency when L_m is in the resonance.

If representing the trajectory on the same state plane, the same normalization factors should be employed. Thus, the normalized forms of v_{Cr} and i_{Lr} are

$$v_{CrN} - 1 = \frac{I_{Lr0N}}{Z_0/Z_1} \cdot \sin[\omega_1 (t - t_0)] + (V_{Cr0N} - 1) \cdot \cos[\omega_1 (t - t_0)] \tag{2.13}$$

$$\frac{i_{LrN}}{Z_0/Z_1} = \frac{I_{Lr0N}}{Z_0/Z_1} \cdot \cos[\omega_1 (t - t_0)] - (V_{Cr0N} - 1) \cdot \sin[\omega_1 (t - t_0)]. \tag{2.14}$$

The trajectory is obtained from (2.13) and (2.14):

$$\left(v_{CrN}-1\right)^2+\left(\frac{i_{LrN}}{Z_0/Z_1}\right)^2=\left(V_{Cr0N}-1\right)^2+\left(\frac{i_{Lr0N}}{Z_0/Z_1}\right)^2, \tag{2.15}$$

which behaves as an ellipse with a center (1,0). Since L_m participates in the resonance, the characteristic impedance Z_1 becomes large ($Z_1>Z_0$). If it is normalized with the same current factor V_{in}/Z_0, the trajectory looks like a circle been compressed, which is an ellipse, as shown in Fig. 2.3.

If the switch Q_1 is off and Q_2 turns on, there are another three operation modes as shown in Fig. 2.4.

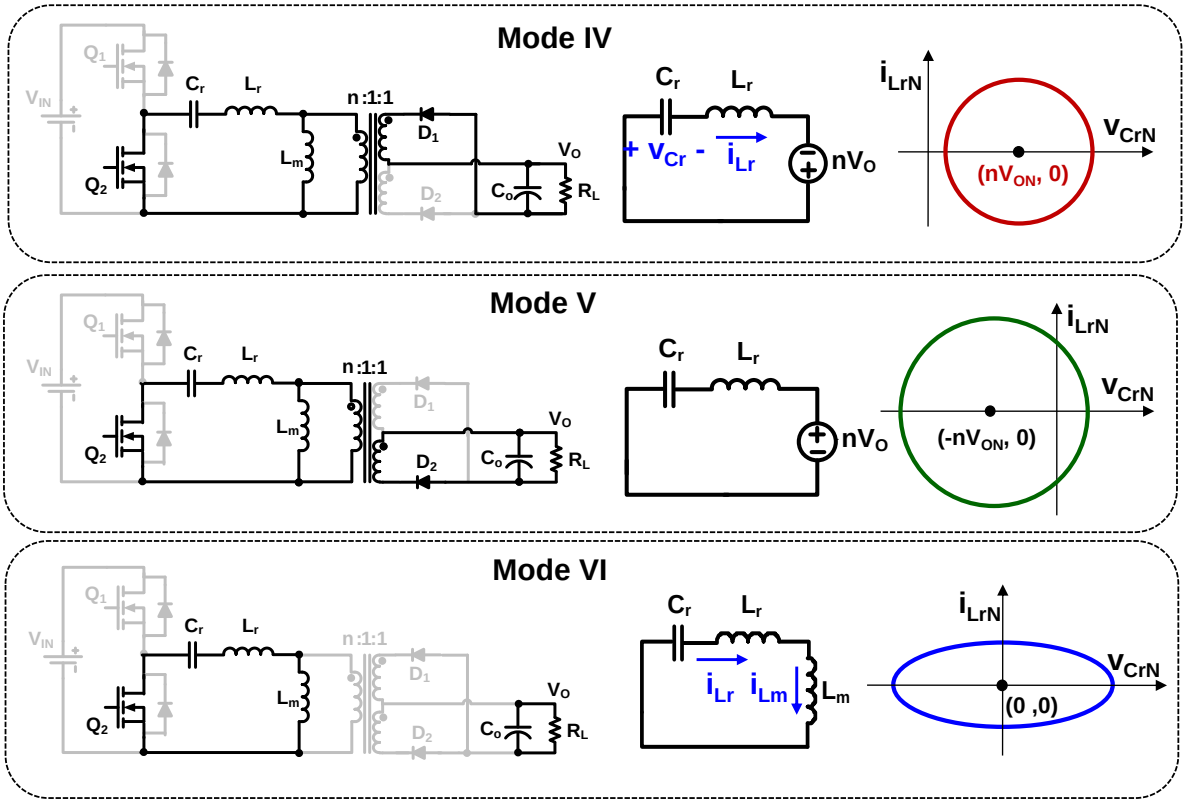


Fig. 2.4 Operation modes and corresponding trajectories when Q_2 is on

- Mode IV

In Mode IV, the primary-side main switch Q_2 turns on, and the resonant current flows through the secondary-side rectifier D_1 as shown in Fig. 2.4. The only difference from Mode I is the source voltage across resonant tank becomes nV_o. Deriving the normalized equation for the state trajectory, we get:

$$\left(v_{CrN} - nV_{oN}\right)^2 + {i_{LrN}}^2 = \left(V_{Cr0N} - nV_{oN}\right)^2 + {I_{Lr0N}}^2 , \tag{2.16}$$

and thus, the circle center changes to (nV_{oN}, 0).

- Mode V

In Mode V, Q_2 is on, but the current on the secondary side changes its direction, flowing through D_2, as shown in Fig. 2.4. This occurs when $f_s>f_0$, similar to Mode II. The normalized expression for the trajectory is:

$$\left(v_{CrN} + nV_{oN}\right)^2 + {i_{LrN}}^2 = \left(V_{Cr0N} + nV_{oN}\right)^2 + {I_{Lr0N}}^2 . \tag{2.17}$$

Now the circle center changes to ($-nV_{oN}$, 0).

- Mode VI

In Mode VI, Q_2 is on, but there is no current flowing through the secondary side. This mode happens when $f_s<f_0$. Like in Mode III, C_r, L_r and L_m form the series resonant tank. But the source voltage across the resonant tank changes to 0. The trajectory after normalization is:

$$v_{CrN}{}^2 + \left(\frac{i_{LrN}}{Z_0/Z_1}\right)^2 = V_{Cr0N}{}^2 + \left(\frac{I_{Lr0N}}{Z_0/Z_1}\right)^2, \quad (2.18)$$

which is an ellipse as in Mode III, but with a center (0, 0).

The LLC steady-state trajectory is the combination of the above six operation modes. Fig. 2.5 to Fig. 2.10 show the steady-state time-domain waveforms and corresponding trajectory loci when $f_s=f_0$, $f_s<f_0$ and $f_s>f_0$ respectively.

Fig. 2.5 shows the time-domain waveforms when the LLC operates at the resonant frequency point ($f_s=f_0$). At time t_0, the resonant current i_{Lr} equals to the magnetizing current i_{Lm} (i.e. $i_{Lr}=i_{Lm}$). From t_0 to t_1, it equivalently operates under Mode I: L_m is clamped by the output voltage, which is decoupled from the resonance; and C_r and L_r form the series resonant tank. Then from t_1 to t_2, the LLC operates under Mode IV. The amplitudes of i_{Lr} and v_{Cr} is determined by the load conditions. The heavier the load is, the larger the amplitudes will be.

Fig. 2.6 shows the corresponding trajectory when mapping the normalized resonant current i_{LrN} and resonant voltage v_{CrN} to the state plane. To the half-bridge LLC topology, when $f_s=f_0$, the voltage gain is one; that is, $nV_{oN}=0.5$. Therefore, the center of operation Mode I ($1-nV_{oN}$, 0) equals to (0.5, 0), and the center of operation Mode IV (nV_{oN}, 0) equals to (0.5, 0). Thus, the two half circles of Mode I and Mode IV have the same center (0.5, 0), which combine to form one whole circle as shown in Fig. 2.5. The connecting points at t_0 and t_1 are the points where i_{Lr} equals to i_{Lm}. In the state plane, the heavier the load is, the larger the radius ρ will be.

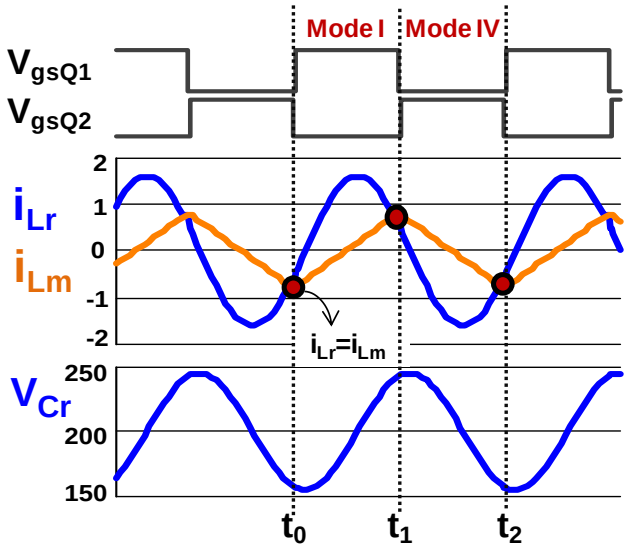


Fig. 2.5 Steady-state time-domain waveforms when $f_s=f_0$

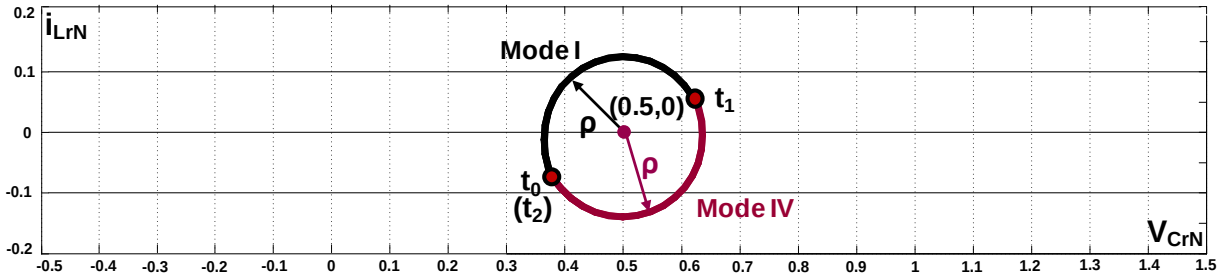


Fig 2.6 Steady-state trajectory when $f_s=f_0$

Fig. 2.7 shows the time-domain waveforms when the LLC operates below the resonant frequency point ($f_s<f_0$). From times t_0 to t_1 and t_2 to t_3, similar to the operation at $f_s=f_0$, it equivalently works under Mode I and Mode IV. From t_1 to t_2 and t_3 to t_4, the magnetizing inductor L_m participates in the resonance. When mapping to the state plane in Fig. 2.8, there are two partial ellipse trajectory loci of Mode III and Mode VI, connecting two half circles of Mode I and Mode IV with split centers. In fact, when $f_s<f_0$, the voltage gain is larger than one (i.e.

nV_{oN}>0.5), and the circle center of Mode I is on the left of (0.5, 0), since 1-nV_{oN}<0.5; and the circle center of Mode IV is on the right of (0.5, 0), since nV_{oN}>0.5.

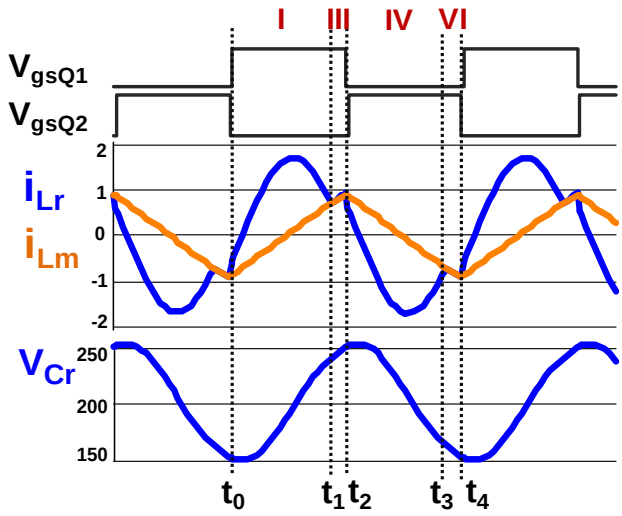


Fig. 2.7 Steady-state time-domain waveforms when f_s<f_0

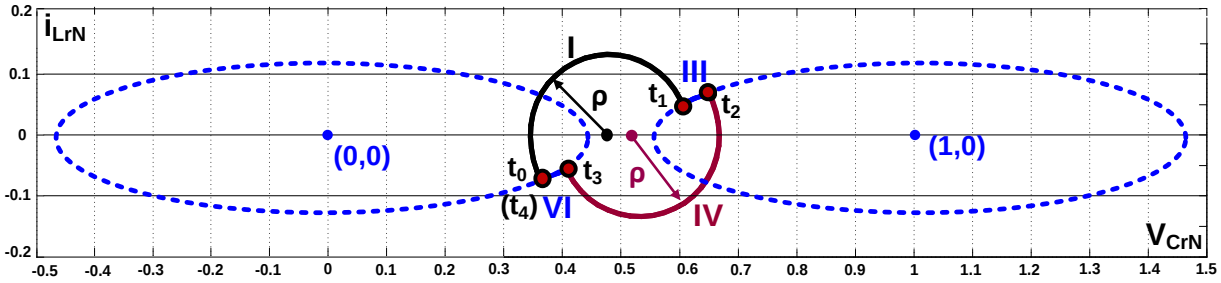


Fig. 2.8 Steady-state trajectory when f_s<f_0

In Fig. 2.9 and Fig. 2.10, the LLC operates in above the resonant frequency region (f_s>f_0). At t_0 moment, i_{Lr} equals to i_{Lm}. From times t_0 to t_1 and t_2 to t_3, it equivalently works under Mode I and Mode IV. Now, the voltage gain is smaller than one (i.e. nV_{oN}<0.5), thus, the circle center of Mode I (1-nV_{oN}, 0) is on the right of (0.5, 0); and the circle center of Mode IV (nV_{oN}, 0) is on the left of (0.5, 0). From times t_1 to t_2, i_{Lr} sharply decreases as under Mode V. It corresponds to the

partial locus of the large circle with center ($-nV_{oN}$, 0). Similarly, from t_3 to t_4, it operates under Mode II, corresponding to the partial locus of another large circle with center ($1+ nV_{oN}$, 0).

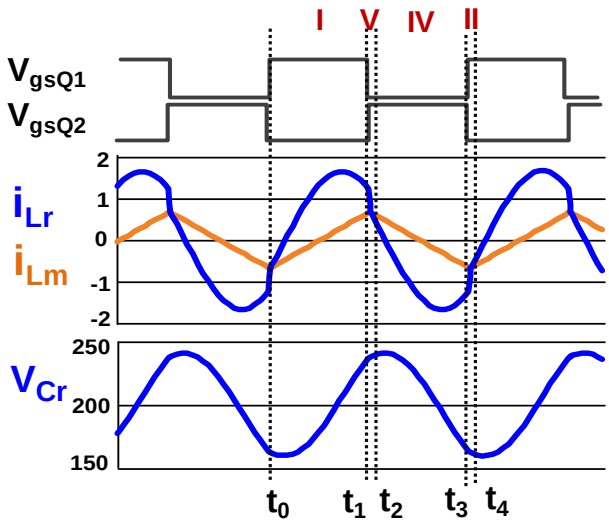


Fig. 2.9 Steady-state time-domain waveforms when $f_s>f_0$

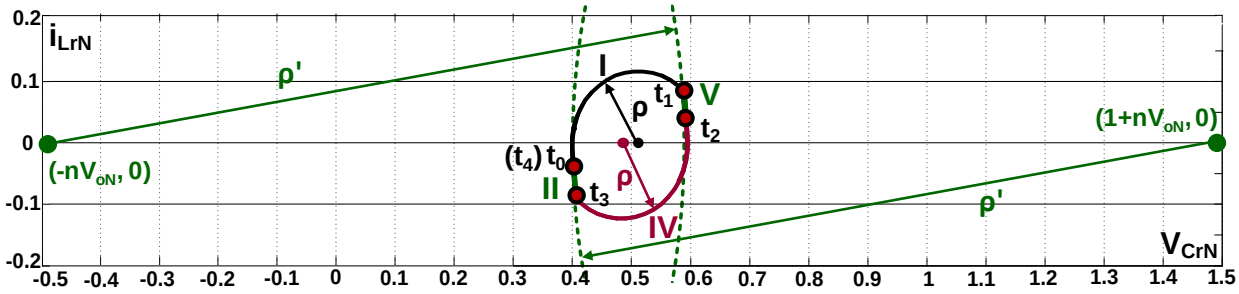


Fig. 2.10 Steady-state trajectory when $f_s>f_0$

Besides the illustration of LLC operation, the steady-state trajectory can explain the energy in the resonant tank as well. When $f_s<f_0$, the ellipse loci will extend the trajectory area in the state plane as shown in Fig. 2.8, which means that resonant tank energy increases. This is the reason why the voltage gain can be boosted as $f_s<f_0$. During the holdup operation, the LLC should work in this region. If $f_s>f_0$, the larger partial circle loci will cut the trajectory area as shown in Fig.

2.10, which means the reduced resonant tank energy. Thus, during the soft start-up and over-load protection, the LLC is required to work above the resonant frequency point to minimize the resonant current and voltage stress.

2.3 LLC Dynamic Trajectories in State-Plane

Normally the LLC resonant converter is designed to operate near the resonant frequency to achieve the best efficiency. Thus, the steady-state trajectory is close to a whole circle as shown in Fig. 2.6. The graphic state-plane analysis of dynamic responses during the load transient, start-up process, and burst mode are illustrated in this section.

2.3.1 Load transient state trajectory

With a conventional linear compensator, like PI or PID, the switching frequency is controlled to regulate the output voltage [B.20-B.25]. Fig. 2.11 shows the control scheme. If the closed-loop compensator is designed with a large bandwidth, the load-transient response will be fast, but there will be dynamic oscillations due to the small phase margin. As shown in Fig. 2.12, when the load steps up, there are many dynamic trajectories between the light-load and heavy-load steady states. Firstly, the circle will extend, and then shrink, and then extend again. Finally, it will approach to the heavy-load steady-state large circle.

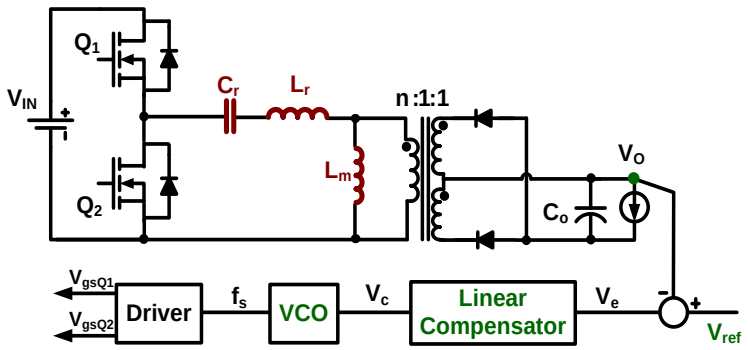


Fig 2.11 LLC resonant converter with a linear compensator

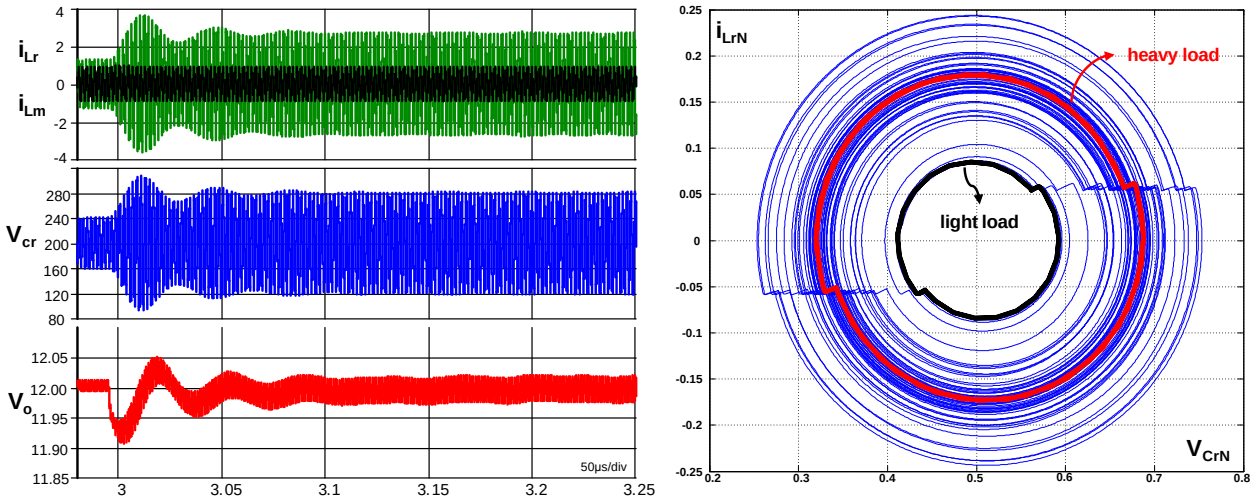


Fig. 2.12 Load-step-up response of a linear compensator with high bandwidth and small phase margin

Fig. 2.13 shows the dynamic response of a linear compensator with a bit lower bandwidth and larger phase margin. The oscillation is eliminated, but the response is much slower. From the state plane, there are many trajectory loci when jumping from the small light-load circle to the large heavy-load circle.

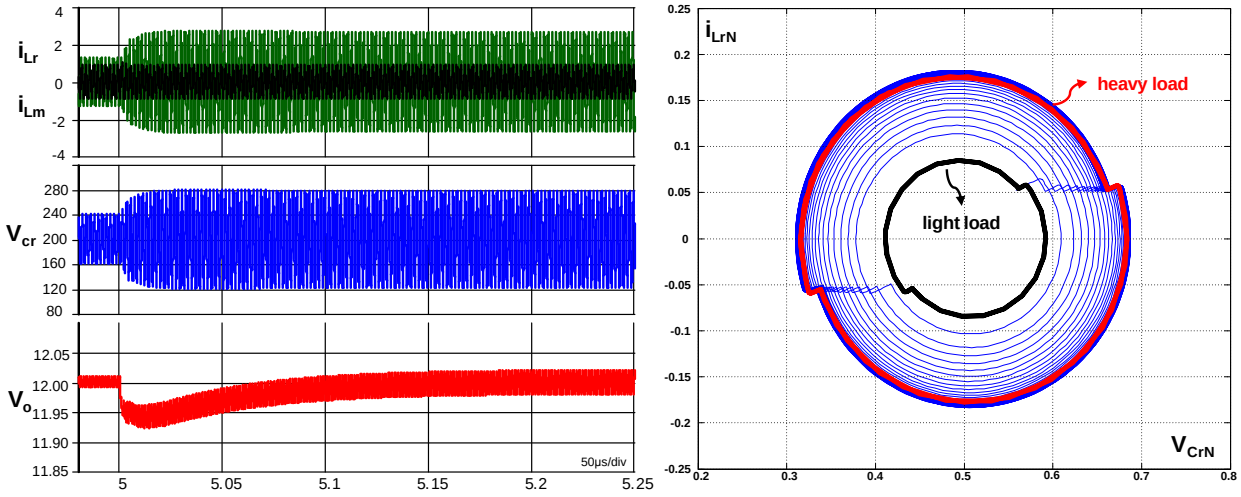


Fig. 2.13 Load-step-up response of a linear compensator with low bandwidth and large phase margin

Therefore, a new control strategy is required to improve the load-transient dynamic performance, while having a simple implementation. From the graphic state plane point of view, the oscillation circles should be eliminated when jumping between light-load small circle and heavy-load large circle.

2.3.2 Start-up transient state trajectory

Different from the steady state, at the start-up moment, there is no energy in the resonant tank, which means that the resonant inductor current and the capacitor voltage both are zero (i.e. i_{Lr}=0, v_{Cr}=0). Thus, on the state plane, the initial point is (0, 0). Before running, the LLC output voltage is zero (i.e. V_o=0). When the LLC up-side switch Q_1 firstly turns on, the equivalent circuit is shown in Fig. 2.14. The voltage across the resonant tank is V_{in}. After normalized with the voltage factor V_{in}, the trajectory is a circle with center (1, 0) as shown in Fig. 2.15. Then Q_2 turns on, since the output voltage has not been built up yet, the voltage across the resonant tank is zero. Correspondingly, on the state plane, the trajectory circle center is (0, 0). Thus, if starting up

at the normal operating point ($f_s=f_0$), Q_1 trajectory will go through half circle from the initial point (0, 0), and then the Q_2 trajectory will go through another half circle from previous final status (2, 0). As shown in Fig. 2.15, the circles will become larger and larger, which means extreme current and voltage stresses in the resonant tank.

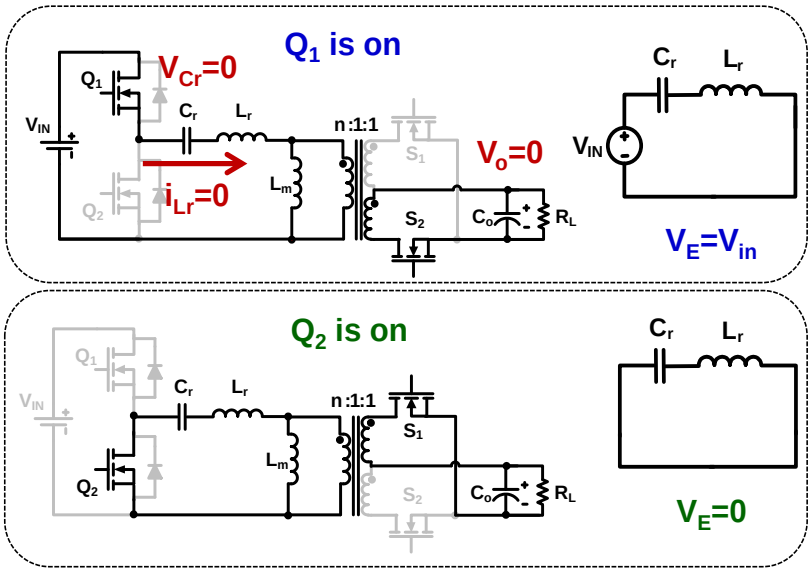


Fig. 2.14 Equivalent circuits when LLC starts up

If the LLC resonant converter starts up with $5f_0$ as shown in Fig. 2.16, the voltage and current stresses in the resonant tank will be much smaller. But at Q_1 second switching instant, ZVS will be lost. Thus, the Q_1 MOSFET will be much more fragile to be damaged.

Therefore, an optimal control approach is required for the LLC soft start-up based on the state-trajectory analysis. The current and voltage stresses should be limited; the ZVS should be guaranteed; and the output voltage should be built up smoothly and quickly.

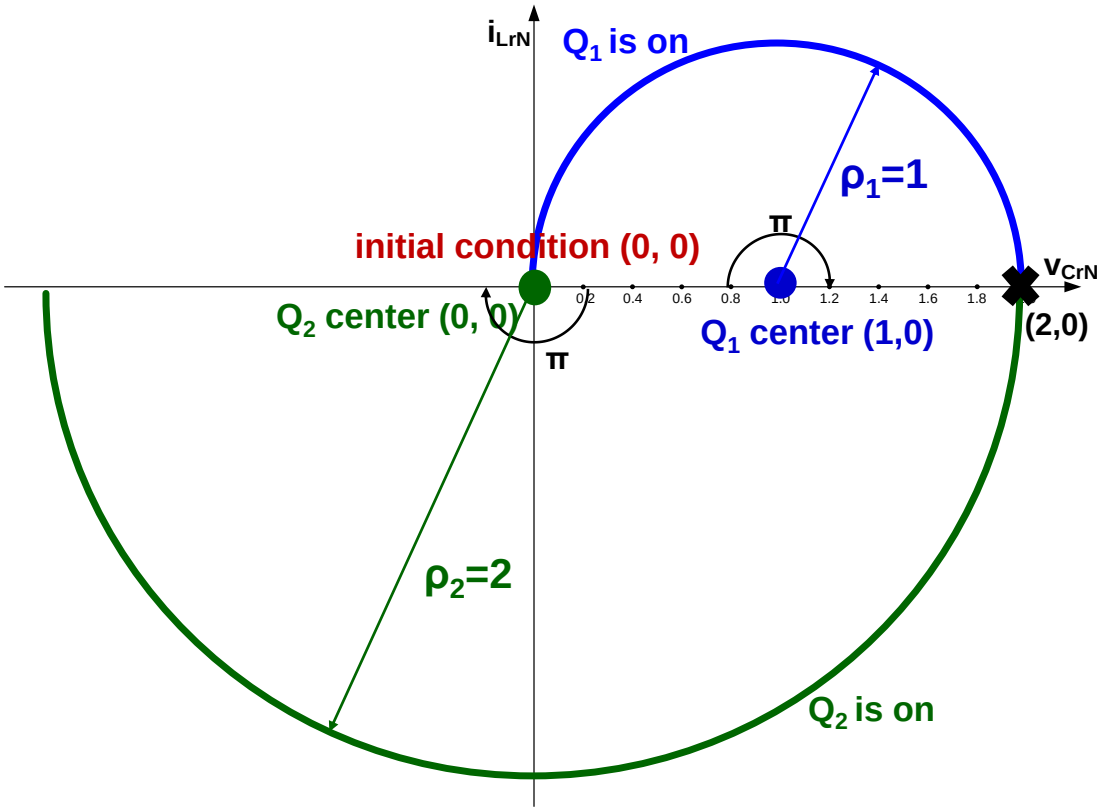


Fig. 2.15 Initial trajectory when LLC starts up at $f_s=f_0$

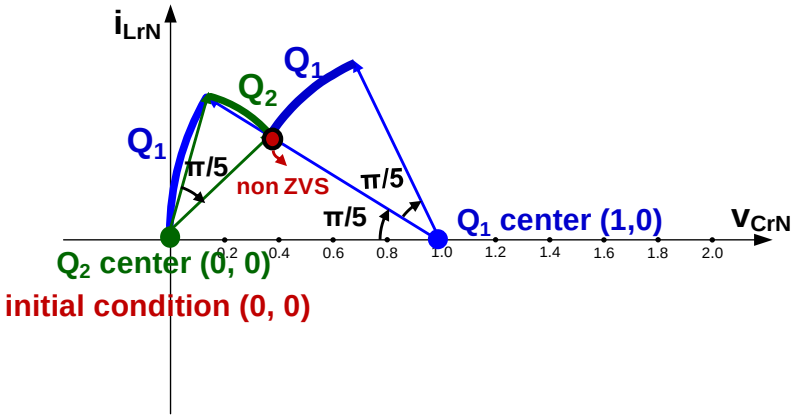


Fig. 2.16 Initial trajectory when LLC starts up at $f_s=5f_0$

2.3.3 Burst mode dynamic state trajectory

The burst mode for LLC light load efficiency improvement is a highly dynamic process as well. Since the LLC resonant converter is always alternate between the idle status and working status. Thus, it is not easy to fix to the optimal load (I_{OPT}) steady state during the burst on-time to achieve best efficiency. As illustrated in Fig. 1.22 and 2.17, there will be oscillated current in the resonant tank.

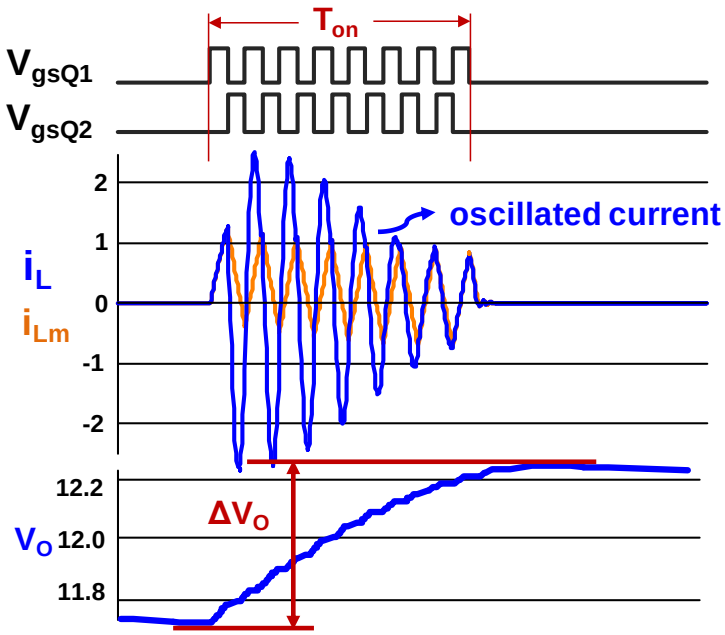


Fig. 2.17 Oscillating resonant current during the burst on-time

Different from the normal operating condition, the output voltage V_o is regulated to be constant, in the burst mode, V_o has a low frequency ripple as shown in Fig. 2.17. During the burst on-time, switches Q_1 and Q_2 conduct alternatively to charge the output capacitor, thus the output voltage is increased by ΔV_o. When Q_1 conducts as Mode I, the source voltage across the

resonant tank will change to V_{in}-nV_o-$n\Delta V_o$; and when Q_2 conducts as Mode IV, the source voltage across the resonant tank will change to nV_o+$n\Delta V_o$. Therefore, on the state plane, during the burst on-time as shown in Fig. 2.18, center O_1 at Mode I will move to left, from (0.5, 0) to (0.5-$n\Delta V_{oN}$, 0); and O_2 at Mode IV will move to right, from (0.5, 0) to (0.5+$n\Delta V_{oN}$, 0). As a result, the circle radius ρ will decrease step by step, which means that the instantaneous energy of the resonant tank will shrink step by step. From the time-domain waveforms, as V_o increases, and resonant current i_{Lr} will decrease step by step equivalently from the heavy load to the light load, never fixing at the I_{OPT} steady state as desired. This dynamic oscillation increases the I_{RMS} value, thus reducing the burst efficiency.

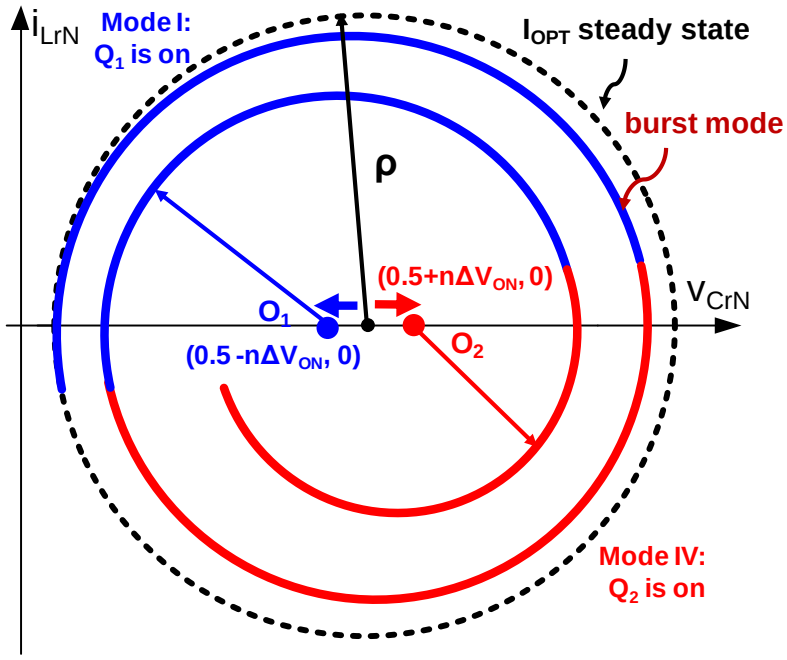


Fig. 2.18 Oscillating circles during the burst on-time

Therefore, an optimal burst mode is required to let the LLC always operate at the best efficiency point during the burst on-time. From the state-trajectory analysis, the output voltage variation should be minimized firstly to avoid the oscillation.

2.4 Conclusion

For the LLC resonant converter, the two-dimension (2D) state-plane trajectory analysis is proposed. Even with 2D trajectory loci, all the resonant tank information such as the resonant capacitor voltage v_{Cr}, the resonant inductor current i_{Lr}, and the magnetizing inductor current i_{Lm} can be clearly presented. The steady-state trajectories within the whole operation region are described. The dynamic trajectories during the load transients, start-up and the burst operation are illustrated as well. To improve these dynamic performances, some optimal control approaches will be presented based on the graphic state-plane analysis in the remaining chapters.

Chapter 3. Dynamic Improvement I: Simplified Optimal Trajectory Control (SOTC) for Load Transient

In this chapter, a simplified optimal trajectory control (SOTC) for the LLC resonant converter is proposed. During the steady state, a linear compensator such as PI or PID is used, controlling the switching frequency (f_s) to eliminate the steady-state error. However, during load transients, the optimal trajectory control (OTC) method takes over, immediately changing the pulse widths of the gate-driving signals. Using the graphic state-plane analysis, the pulse widths are estimated, letting the state variables track the optimal trajectory loci in the minimum period of time. The proposed solution is implemented in a digital controller, and experimental results show that while the digital logic requirement is very small, the performance improvement is significant.

3.1 Introduction

Compared with PWM converters, the LLC control characteristic is more complex due to the fast dynamic characteristic of the resonant tank. For PWM converters, the natural frequency of the output filter is much lower than the switching frequency. Thus, the state-space average method can provide simple and accurate small-signal model [B.1] [B.2]. However, for the LLC resonant converter, the natural frequency of the resonant tank is close to the switching frequency. Since the average method will eliminate the information of switching frequency, it cannot predict the LLC dynamic performance. Therefore, some other approaches such as extend describing function [B.3] [B.4], multi-frequency averaging method [B.5], simulation-based method [B.6]

are required. And all of them need extensive effort of computation. According to these models, a linear compensator like PI or PID [B.20] [B.21] is designed, as shown in Fig. 3.1. Recently, some current-mode controls [B.22-B.25] were proposed to obtain better performance. However, due to the limitations of small-signal models, all of these methods are only valid around a particular operation point.

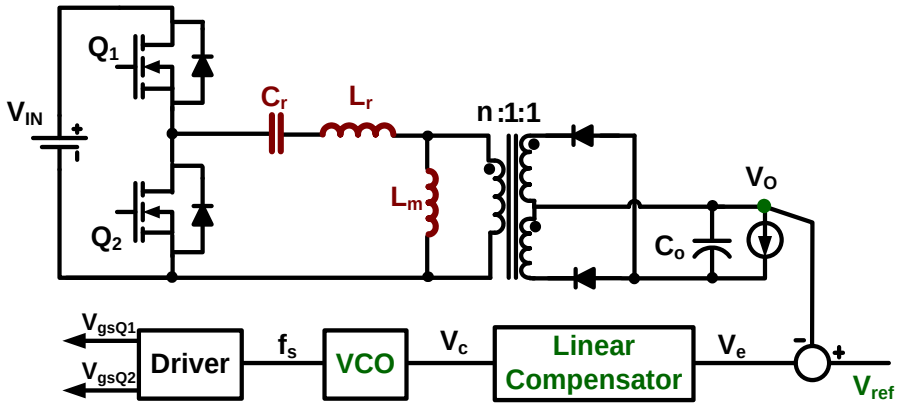


Fig. 3.1 LLC resonant converter with a linear compensator

Compared with the complicated modeling derivation and the limited performance of linear control methods, some non-linear control approaches were proposed based on the graphical state-plane analysis [B.7-B.19]. For the series resonant converters (SRC), the optimal trajectory control (OTC) has been demonstrated to have the best dynamic performance [B.8] [B.10]. The control circuit calculates the variable R at every instantaneous value of the resonant current i_{Lr}, the resonant voltage v_{Cr}, the input voltage v_S and the output voltage v_o. Based on state-plane analysis, the power switches turn on at the instant when the variable R becomes equal to the control reference R_{ref}. By forcing the state variables to track the desired trajectory, this approach guarantees that the time required to reach the steady state is minimal and overshoot is avoided, thus ensuring optimal dynamic performance. However, the on-line computation of variable R is

nonlinear and complicated, and thus difficult to implement. In order to reduce the control complexity, some simplified methods have been proposed for SRC. In [B.14] [B.16], the pseudo-linear form of the control variable R is introduced. In addition, some other linear combinations of the state variables to determine switching instants are proposed in [B.18].

When it comes to the LLC resonant converter as shown in Fig. 3.2, like the OTC for SRC, firstly, the circle centers O_1 and O_2 need to be determined by the equivalent voltage across the resonant tank, thus the input voltage V_{in} and the output voltage V_o need to be sensed. And then, the radius R is calculated at the every instantaneous value of the state variables. The switches turn on at the moments when R is equal to R_{ref} as shown in Fig. 3.3. As illustrated in Chapter 2, the LLC state-plane trajectory is much more complicated than that of the SRC. Moreover, there are more operation modes in the LLC resonant converter. All of these will increase the implementation complexity of the OTC.

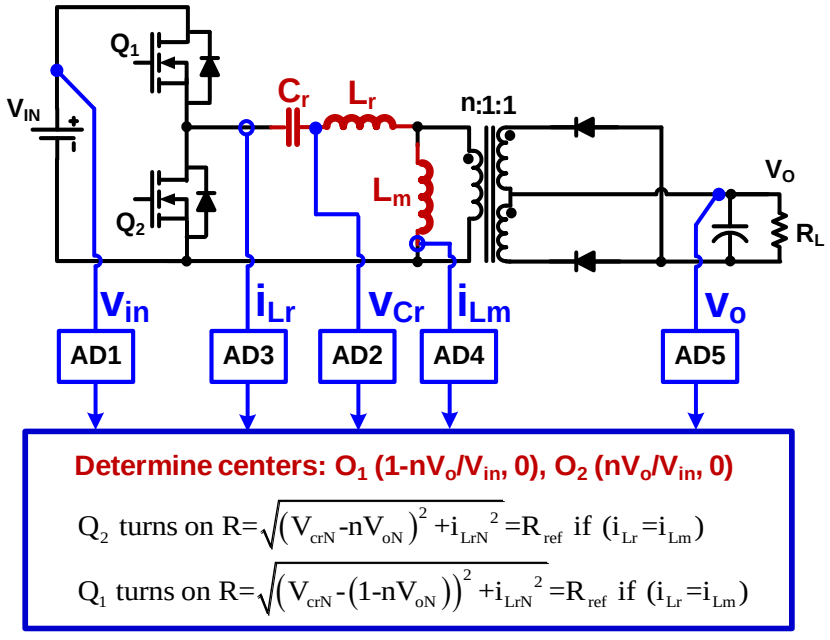


Fig. 3.2 Complicated implementation of conventional OTC for LLC

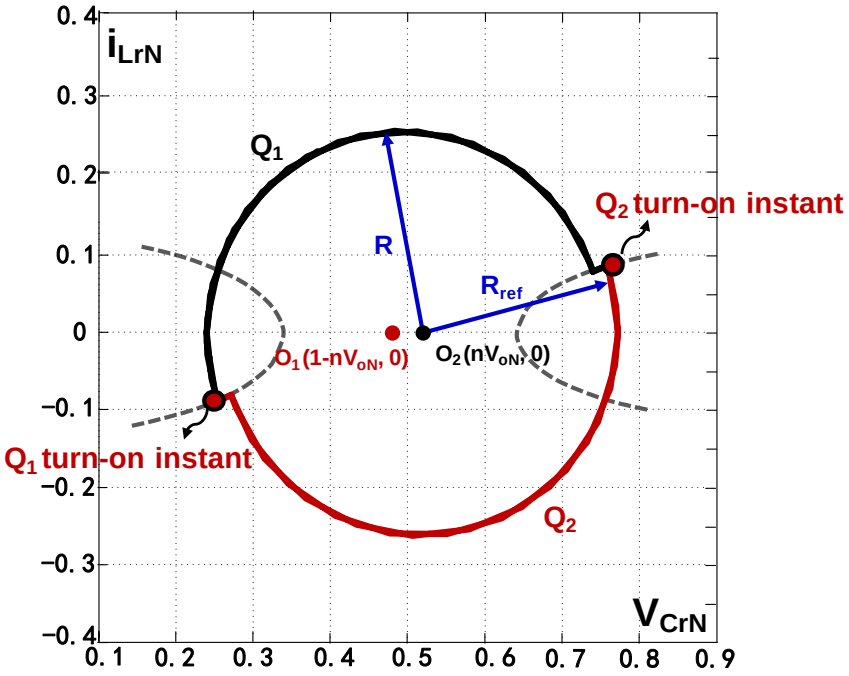


Fig. 3.3 Switching instance capture with conventional OTC

In this chapter, a digital simplified optimal trajectory control (SOTC) is proposed for the LLC resonant converter. During the steady state, the linear regulator is used. At the transient instant, the optimal trajectory control is applied by changing the pulse widths of the driving signals to force the state variables to hit the desired trajectory. Thus, the SOTC will significantly improve the transient response while preserving the closed-loop stability. In this approach, only the load current sensing is needed to determine the optimal pulse widths.

3.2 SOTC in Load Step-up Transient

In this section, the simplified optimal trajectory control (SOTC) is illustrated in detail. With the advantage of digital implementation, it enables more intelligent power control during load transients.

Fig. 3.4 shows the control block diagram. Under the steady state, a conventional linear regulator, such as PI or PID compensator, controls the switching frequency (f_s) to regulate the output voltage (V_o). In addition, the load current (i_{Load}) is sensed to monitor the transient moment. When the load steps up or down, the SOTC will immediately respond, determining the required pulse widths (ΔT_{INC} /ΔT_{DEC}) to follow the optimal trajectory.

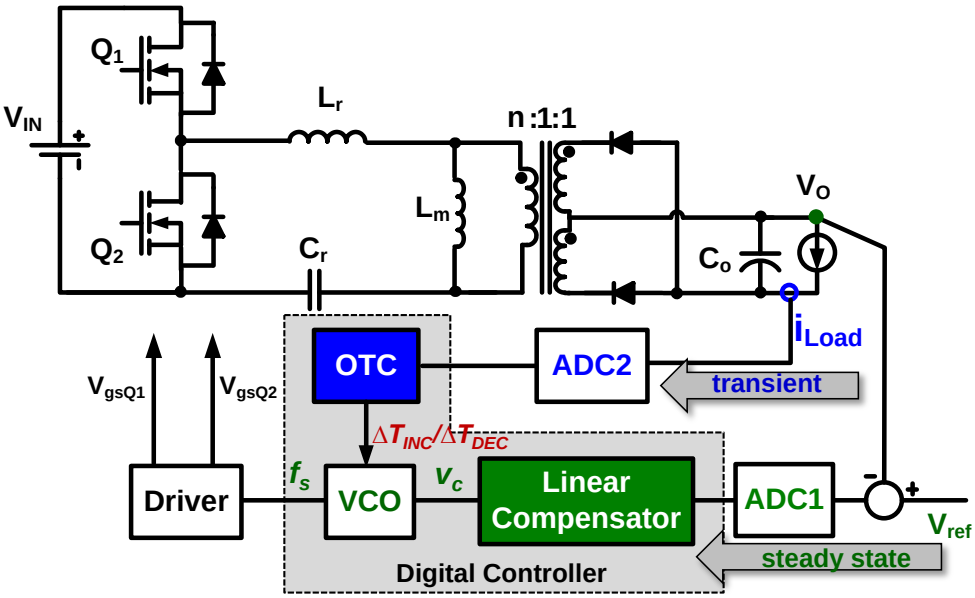


Fig. 3.4 SOTC control blocks for LLC resonant converter

In order to achieve the best efficiency, the LLC resonant converter is designed to operate near the resonant frequency point (f_s=f_0), and thus the steady-state trajectory lies on a circle, as presented in Fig. 3.5. The heavier the load is, the larger the circle radius will be. When the load steps up from the light load (I_{LL}) to the heavy load (I_{HL}), as shown in Fig. 3.5, the OTC approach will increase the pulse width of the up-switch gate-driving signals (V_{gsQ1}), letting L_m join the resonance from times t_1 to t_2, as in Mode III. If mapped to the state plane, one partial ellipse trajectory will connect two circles.

Although at t_2 moment, the resonant inductor current i_{Lr} and resonant capacitor voltage v_{Cr} are settled to the heavy load steady state. Due to the increase of one pulse width, the magnetizing inductor current i_{Lm} is unbalanced as shown in the shaded area in Fig. 3.5. Since the magnetizing inductor L_m is always large, after OTC jumping one pulse, the linear compensator like PI control needs take a lot of switching cycles to eliminate the steady-status error. As shown in Fig. 3.5 state-plane drawing, there are many dynamic trajectory circles near the final heavy load steady state.

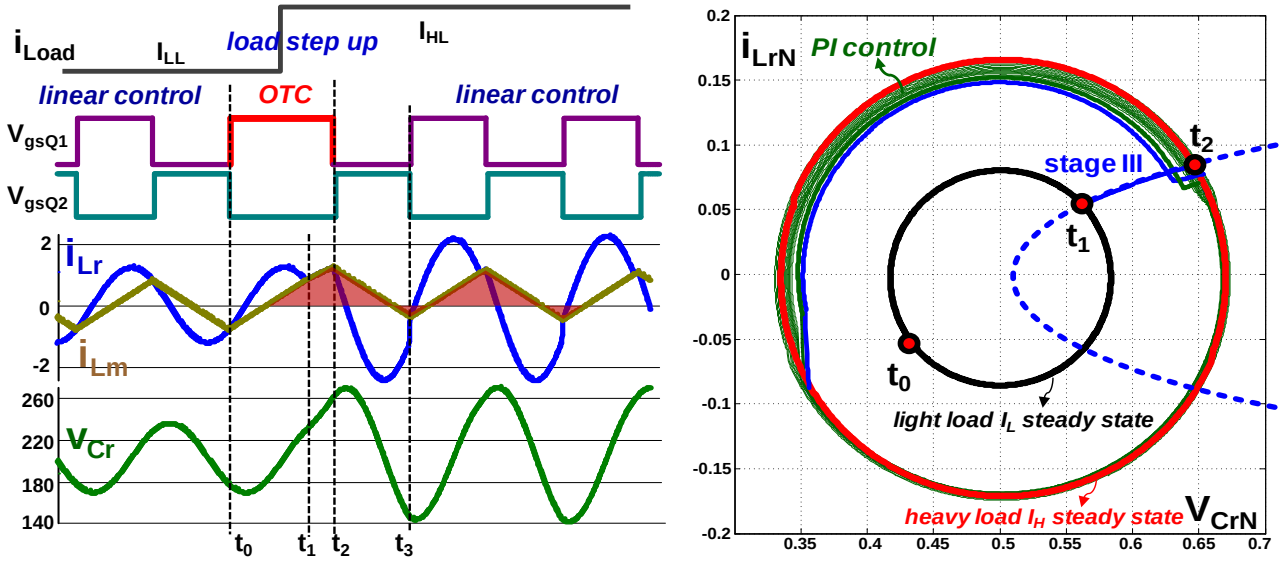


Fig. 3.5 One-step SOTC during the load-step-up

To settle all the state variables (i_{Lr}, v_{Cr} and i_{Lm}), OTC should employ two-pulse jump when the load steps up. As shown in Fig. 3.6, the SOTC approach will increase the pulse widths of V_{gsQ1} and V_{gsQ2}, letting L_m join the resonance from times t_1 to t_2 and t_3 to t_4, as in Mode III and Mode VI. If mapped to the state plane, by going through these two ellipse loci and the transitional half circle, all state variables will hit the final steady-state heavy-load circle at time t_4. After that, the PI compensator takes over to eliminate the steady-state error. Since all state

variables are almost settled at t_4 moment, the PI compensator takes less effort. The trajectory is almost fixed to the heady-load steady state.

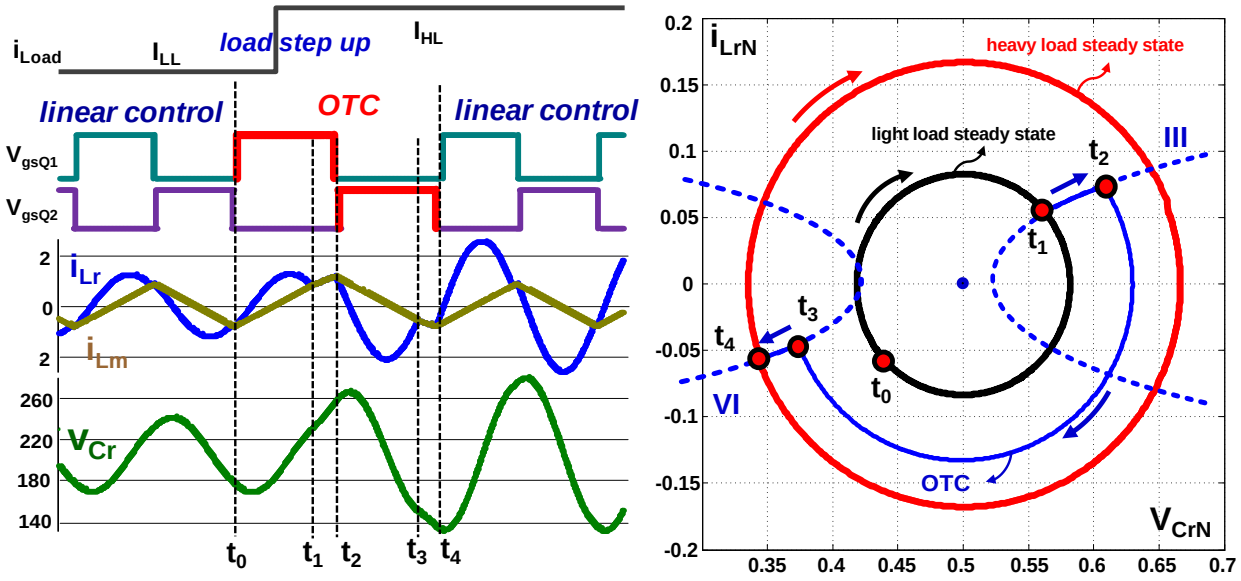


Fig. 3.6 Two-step SOTC during the load-step-up

By sensing the load current i_{Load} and using the state-plane graph, the increased pulse widths can be estimated at the load step-up moment. The calculation process is shown in detail below.

From [A.33], near the resonant frequency point, the expression of RMS value (I_{RMS}) of the resonant current i_{Lr} is

$$I_{RMS} = \frac{1}{4\sqrt{2}} \cdot \frac{V_o}{nR_L} \sqrt{\frac{n^4 R_L{}^2 T^2}{L_m{}^2} + 4\pi^2} = \frac{1}{4\sqrt{2}} \sqrt{\frac{n^2 V_o{}^2 T^2}{L_m{}^2} + 4\pi^2 \cdot \left(\frac{i_{Load}}{n}\right)^2}, \tag{3.1}$$

where n is the transformer turn ratio, T is the resonant period ($T=2\pi/\omega_0$), and i_{Load} is the load condition.

As shown in Fig. 3.7, the circle radius ρ in the state-plane is the normalized current peak value:

$$\rho = \frac{\sqrt{2} I_{RMS}}{V_{in}/Z_0}. \tag{3.2}$$

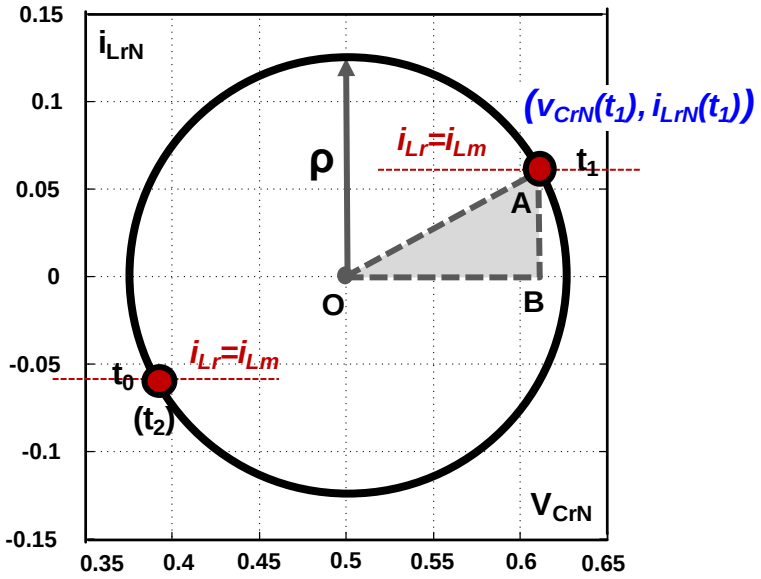


Fig. 3.7 Steady-state trajectory analysis when $f_s=f_0$

From times t_0 to t_1, the magnetizing inductor L_m is clamped by the output voltage; thus i_{Lm} increases linearly as shown in Fig. 3.6. At time t_1, the resonant current i_{Lr} is equal to i_{Lm}:

$$i_{Lr}(t_1) = i_{Lm}(t_1) = \frac{nV_o}{L_m} \cdot \frac{T}{4}. \tag{3.3}$$

The normalized form is

$$i_{LrN}(t_1) = i_{LmN}(t_1) = \frac{nV_o}{L_m} \cdot \frac{T}{4} \cdot \frac{1}{V_{in}/Z_0}. \tag{3.4}$$

Solving the right triangle ΔABO in Fig. 3.7, the normalized resonant capacitor voltage at t_1, which is when Q_1 turns off, is obtained:

$$v_{CN}(t_1) = \sqrt{\rho^2 - i_{LrN}(t_1)^2} + 0.5 = \frac{\pi}{2} \cdot \frac{i_{Load}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5, \tag{3.5}$$

where the resonant capacitor voltage at time t_1 is related to the load current i_{Load}.

Therefore, under the light-load condition, the resonant capacitor voltage at time t_1 is

$$v_{CrN}(t_1) = \frac{\pi}{2} \cdot \frac{I_{LL}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5\,, \tag{3.6}$$

where I_{LL} is the light-load current.

When the load steps up, by sensing the load current, the resonant capacitor voltage at time t_4 can be predicted as

$$v_{CrN}(t_4) = -\frac{\pi}{2} \cdot \frac{I_{HL}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5\,, \tag{3.7}$$

where I_{HL} is the heavy-load current.

As shown in Fig. 3.6, the transitional half circle from t_2 to t_3 can be approximated to be at the middle of two circles; the inner circle corresponding at light load and the outer circle at the heavy load. Thus, the normalized capacitor voltage at t_2 can be calculated as

$$v_{CrN}(t_2) = \frac{v_{CrN}(t_1) + (1 - v_{CrN}(t_4))}{2} = \frac{\pi}{2} \frac{(I_{LL} + I_{HL})/2}{n} \frac{1}{V_{in}/Z_0} + 0.5 . \tag{3.8}$$

Since the magnetizing inductor L_m is much larger than the resonant inductor L_r, from times t_1 to t_2, the current can be treated as a constant I; i.e.:

$$I = i_{Lr}(t_1) = i_{Lm}(t_1) = \frac{nV_o}{L_m} \cdot \frac{T}{4} = \frac{V_{in}}{L_m} \cdot \frac{T}{8} . \tag{3.9}$$

This constant current charges the resonant capacitor C_r from t_1 to t_2 to achieve the SOTC. Thus, the increased pulse width is

$$\Delta T_{INC} = t_2 - t_1 = \frac{C_r \cdot (v_{CrN}(t_2) - v_{CrN}(t_1)) \cdot V_{in}}{I} = \frac{L_m \cdot (I_{HL} - I_{LL})/n}{V_{in}} , \tag{3.10}$$

which can be determined by load sensing (I_{HL} and I_{LL}) and digital calculation.

Since the transitional circle locates at the middle of two steady-state circles, the time duration from t_3 to t_4 is the same with ΔT_{INC} from t_1 to t_2. Thus, when the load steps up, the SOTC will increases two pulse widths of driving signals V_{gsQ1} and V_{gsQ2} by ΔT_{INC} to follow the optimal trajectory as plotted in Fig. 3.6.

As a comparison, the simulated dynamic response with a conventional linear compensator is given in Fig. 3.8. The response is fast, but there will be some dynamic oscillations. From the state plane, there are many trajectory loci when jumping from the small light-load circle to the large heavy-load circle.

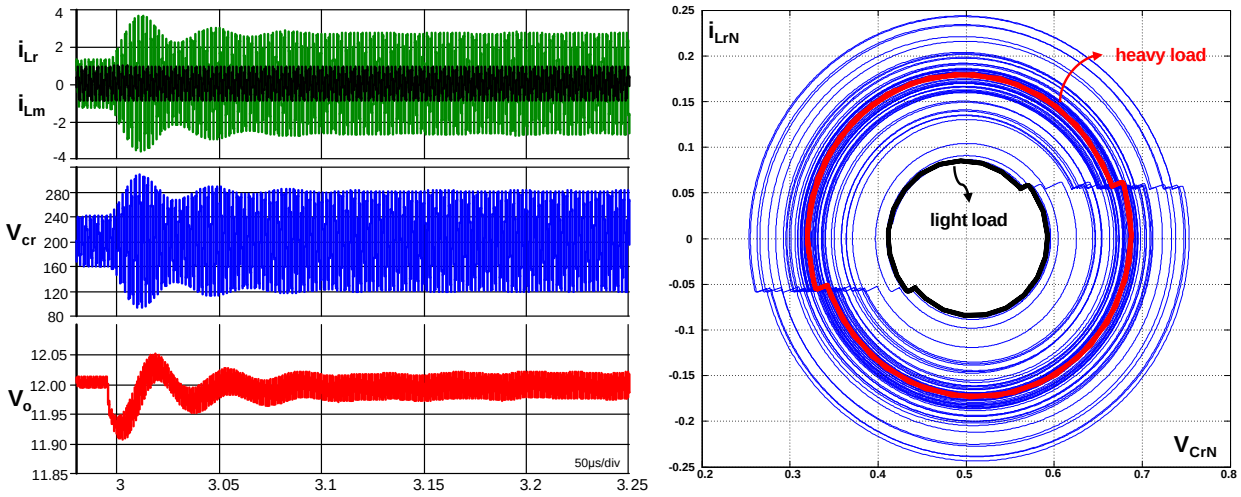


Fig. 3.8 Load-step-up response of a linear compensator

If with the proposed SOTC, Fig. 3.9 shows that there is almost no dynamic oscillation. All the state variables (i_{Lr}, i_{Lm} and v_{Cr}) settle to the new steady state quickly. After two pulses jump, the dynamic trajectory is quite clean. The linear compensator takes less effort to converge to the new steady state by getting rid of the steady-state error.

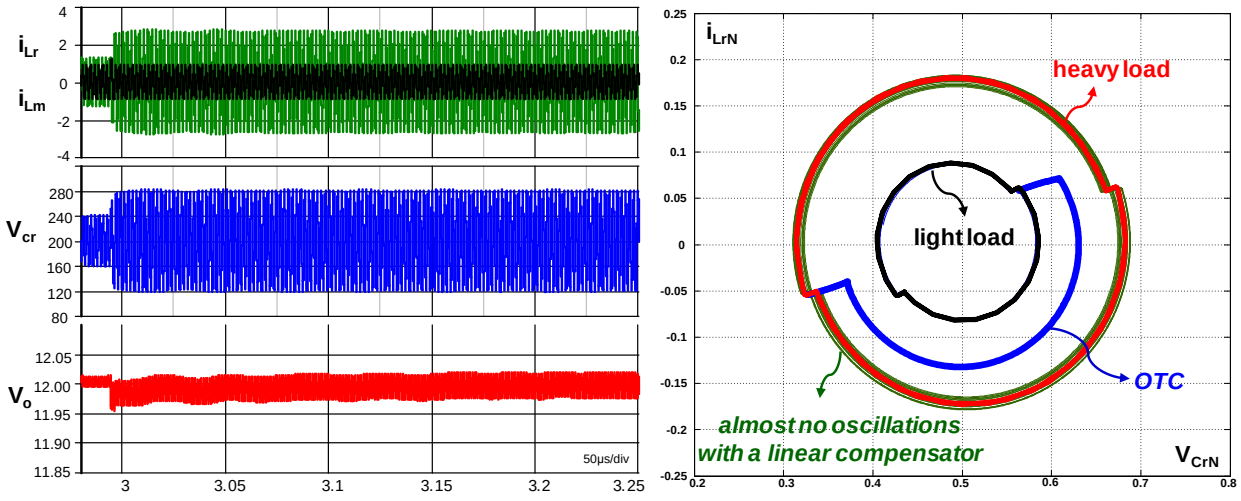


Fig. 3.9 Load-step-up response of the SOTC

As in (3.10), the accurate prediction of ΔT_{INC} depends on knowing V_{in}, L_m and load conditions (I_{HL} and I_{LL}). However, the input voltage V_{in} may have a variation; L_m may have a tolerance; and the sensing results of I_{HL} and I_{LL} may have an error. All of these will reduce the accuracy of ΔT_{INC}. Take the load sensing error as an example. At the load step-up moment, if the sensing results are 20% smaller than the real loads, the actual ΔT_{INC} will be 20% smaller than the required one. Fig. 3.10 shows that the linear compensator will take a bit more effort to converge to the new steady state after two pulses jump. In terms of the state plane, there are a bit more oscillations near the heavy-load steady circle. But the dynamic performance is still much better than that of a conventional linear compensator.

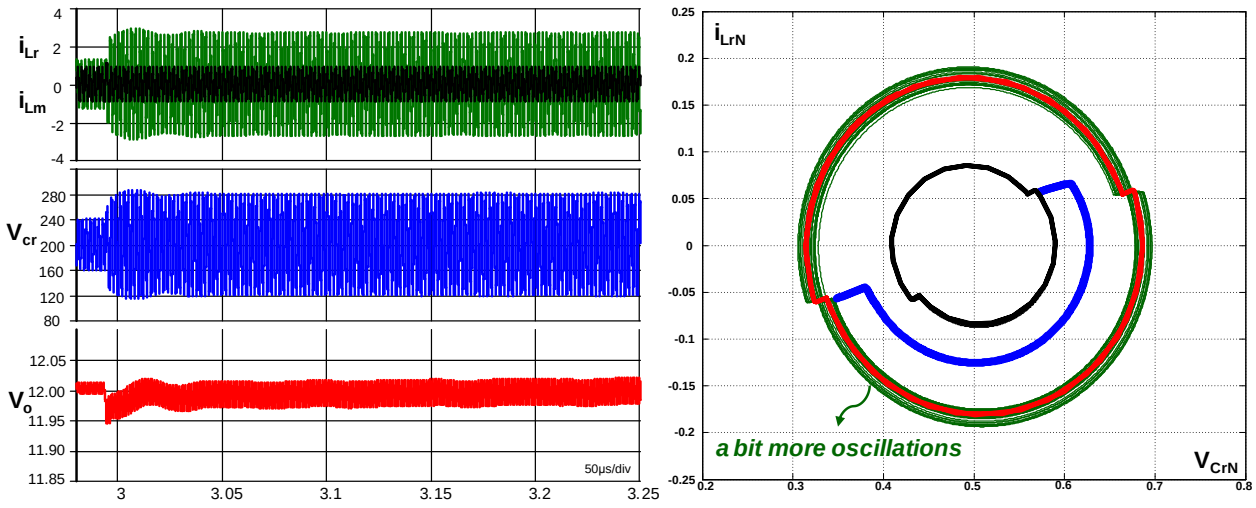


Fig. 3.10 Load-step-up response of the SOTC with 20% load sensing mismatch

In addition, ΔT_{INC} is obtained with the assumption that the LLC operates near the resonant frequency point. However, if the LLC is connected to a PFC, the input voltage has a low-frequency variation. When the actual input voltage is 10% smaller than the normal V_{in}, the linear compensator will regulate f_s to below the resonant frequency point. As shown in Fig. 3.11, after

two pulses jump with ΔT_{INC}, the SOTC presents a bit of oscillations. But compared with the dynamic response only using a linear compensator, the transient improvement is still significant.

Therefore, the estimation of ΔT_{INC} in (3.10) has a good error-tolerance for the parameter variations.

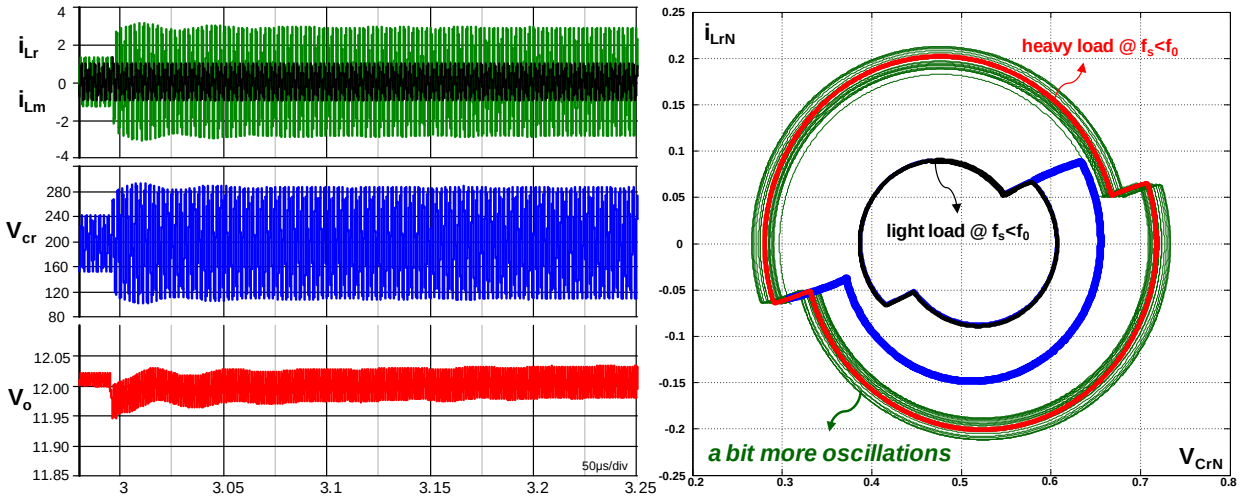


Fig. 3.11 Load-step-up response of the SOTC when V_{in} is 10% smaller

In the distributed power architecture, the LLC output is usually fed to the point of load converters (POLs). Thus the LLC output load might slowly steps up as shown in Fig. 3.12. A multi-step SOTC strategy is employed. The pulse widths of the gate driving signals increase step by step according to the load step change in each switching cycle. From the state-plane, it will go through several ellipse loci and transitional circles, finally approaching the heavy load steady state. After that, the PI compensator takes over to get rid of the steady-state error.

If the LLC load steps up more slowly, a linear compensator can converge to the new steady state with few oscillations and less settling time. It is unnecessary to adopt the SOTC to improve

the load transient dynamic response. Thus, a threshold load-step change (I_{th}) is set to trigger the SOTC. Fig. 3.13 shows the control flowchart implemented in the digital controller.

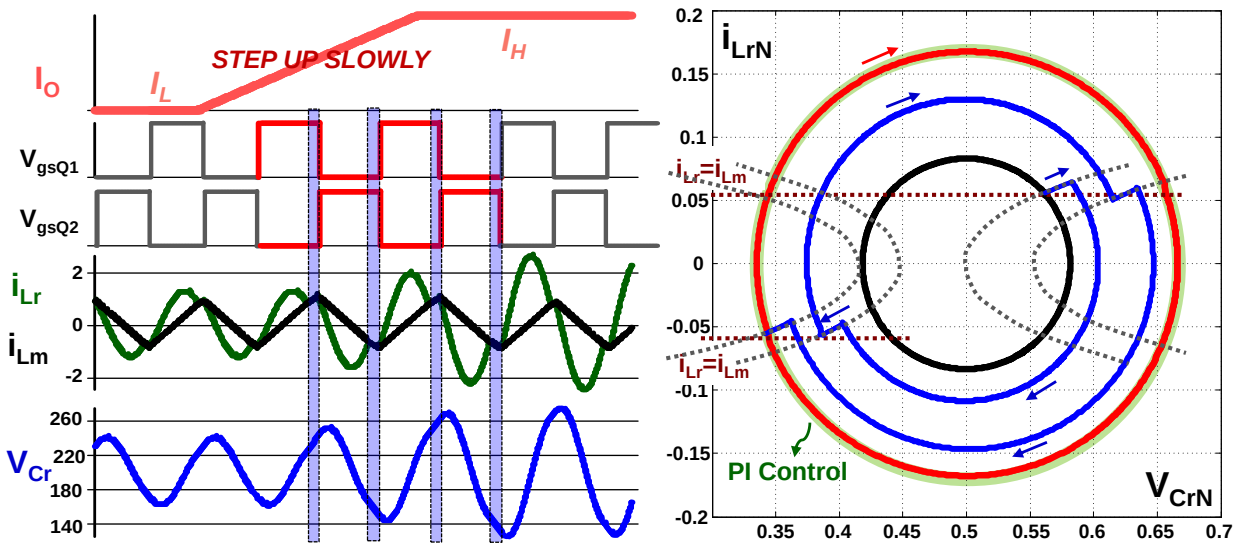


Fig. 3.12 Muli-step SOTC for slowly changed load

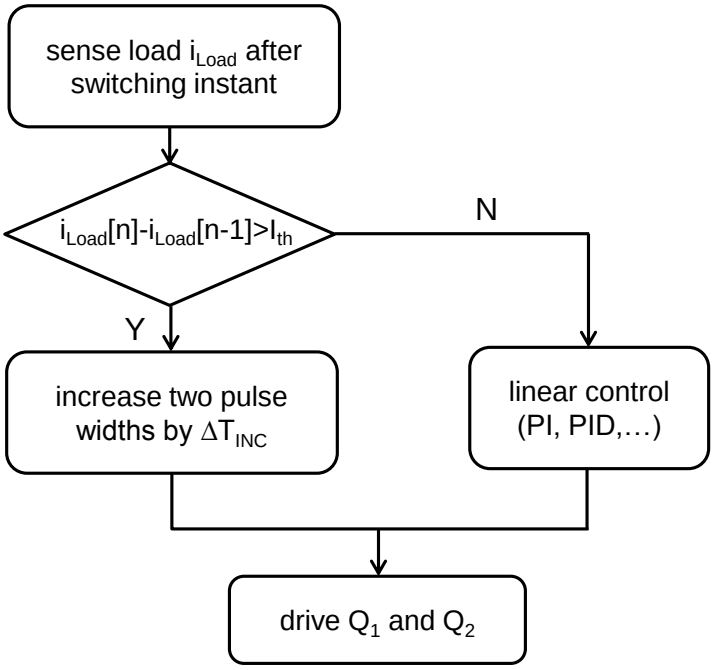


Fig. 3.13 Control flowchart of the SOTC

3.3 SOTC in Load Step-down Transient

On the other hand, if the load steps down, the SOTC will decrease the pulse widths of the driving signals. In Fig. 3.14, at the transient instant, from times t_1 to t_2 and t_3 to t_4, the SOTC controls the state variables going through trajectories of Mode V and II, jumping from the initial heavy-load large circle to the final light-load small circle within the time of two pulse widths.

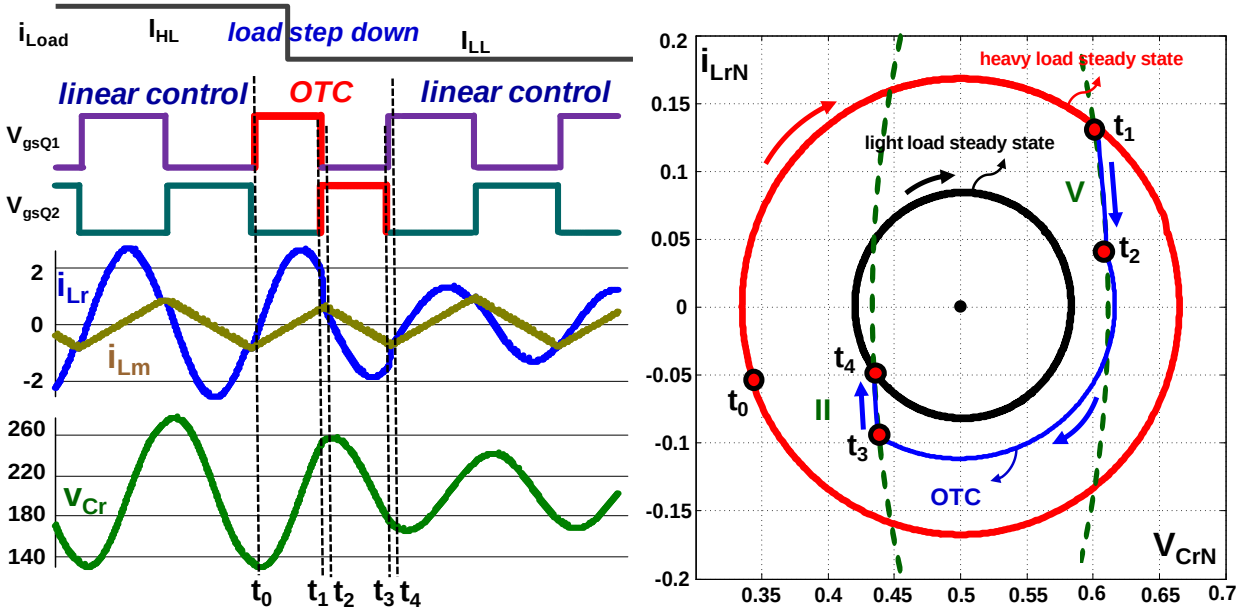


Fig. 3.14 SOTC during the load-step-down

By sensing the load current i_{Load} and using the state-plane graph, the decreased pulse widths can be estimated at the load step-down moment as well. The detailed calculation process is shown below.

Similar to (3.7), the resonant capacitor voltage at t_0 is:

$$v_{CrN}(t_0) = -\frac{\pi}{2} \cdot \frac{I_{HL}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5\,. \tag{3.11}$$

When the load steps down, the resonant capacitor voltage at time t_4 is predicted:

$$v_{CrN}(t_4) = -\frac{\pi}{2} \cdot \frac{I_{LL}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5\,. \tag{3.12}$$

Since the circles of Mode V and II are much larger, as illustrated in Fig. 2.9 in Chapter 2, the partial circles from times t_1 to t_2 and t_3 to t_4 could be assumed to be the lines shown in Fig. 3.15. Thus,

$$v_{CrN}(t_1) = v_{CrN}(t_2) \tag{3.13}$$

$$v_{CrN}(t_3) = v_{CrN}(t_4). \tag{3.14}$$

Within the OTC duration, the magnetizing inductor L_m is always clamped by the output voltage nV_o. In order to settle the magnetizing current i_{Lm} ($i_{Lm}(t_4) = i_{Lm}(t_0)$), the pulse width of V_{gsQ1} and V_{gsQ2} should be equal. In terms of the state plane, the angle (α_1) from t_0 to t_1 should be the same of angle (α_2) from t_2 to t_3 (i.e. $\alpha_1 = \alpha_2$).

Solving the two similar triangles shaded in Fig. 3.15, we obtain:

$$\frac{v_{CrN}(t_2) - 0.5}{0.5 - v_{CrN}(t_0)} = \frac{0.5 - v_{CrN}(t_3)}{v_{CrN}(t_1) - 0.5} = \frac{i_{LmN}(t_2)}{-i_{LmN}(t_0)} \tag{3.15}$$

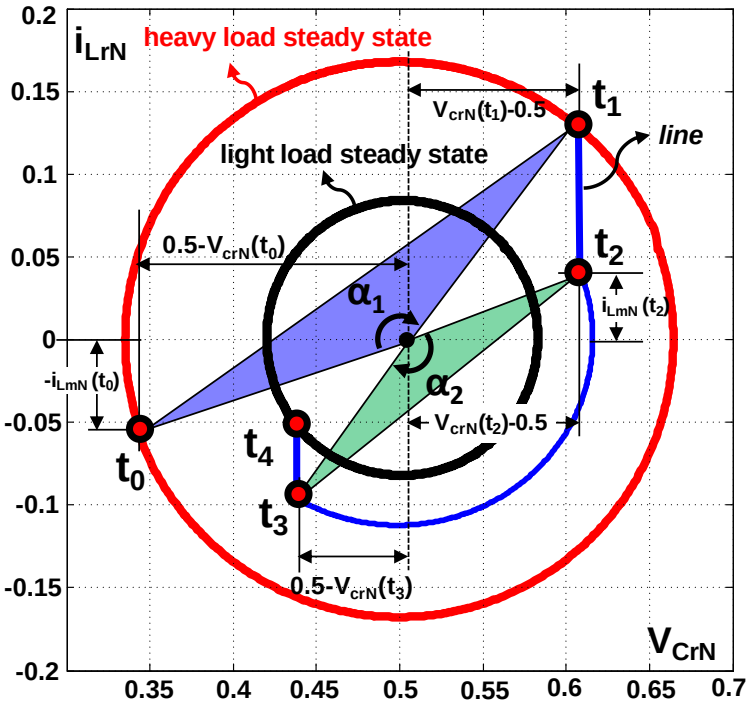


Fig. 3.15 Simplified analysis of SOTC during load step-down

Using (3.11) to (3.15), the resonant capacitor voltage at switching instant t_2 can be determined as

$$v_{CrN}(t_2) = \sqrt{(0.5 - v_{CrN}(t_0)) \cdot (0.5 - v_{CrN}(t_3))} + 0.5 = \frac{\pi}{2} \frac{\sqrt{I_{HL} \cdot I_{LL}}}{n} \frac{1}{V_{in}/Z_0} + 0.5 . \tag{3.16}$$

At t_0, the resonant current i_{Lr} is equal to the magnetizing current i_{Lm}, which is similar to (3.4):

$$i_{LrN}(t_0) = i_{LmN}(t_0) = -\frac{nV_o}{L_m} \cdot \frac{T}{4} \cdot \frac{1}{V_{in}/Z_0} . \tag{3.17}$$

From (3.11), (3.15) to (3.17), the magnetizing current at t_2 instant can be solved as:

$$i_{LmN}(t_2) = -i_{LmN}(t_0) \cdot \frac{v_{CrN}(t_2) - 0.5}{0.5 - v_{CrN}(t_0)} = \frac{nV_o}{L_m} \cdot \frac{T}{4} \cdot \frac{1}{V_{in}/Z_0} \cdot \sqrt{\frac{I_{LL}}{I_{HL}}} \,. \tag{3.18}$$

From times t_0 to t_2, the magnetizing inductor L_m is clamped by the output voltage as shown in Fig. 3.14, thus i_{Lm} is linearly increased. The time duration from t_0 to t_2 can be obtained as follow:

$$T' = t_2 - t_0 = \frac{L_m \cdot \left(i_{LmN}(t_2) - i_{LmN}(t_0)\right) \cdot V_{in}/Z_0}{nV_o} = \left(1 + \sqrt{\frac{I_{LL}}{I_{HL}}}\right) \cdot \frac{T}{4} \,. \tag{3.19}$$

Since the time duration from t_1 to t_2 is negligible, the decreased pulse width to achieve the optimal trajectory is

$$\Delta T_{DEC} = \frac{T}{2} - T' = \left(1 - \sqrt{\frac{I_{LL}}{I_{HL}}}\right) \cdot \frac{T}{4} \,, \tag{3.20}$$

when the load steps down, as shown in Fig. 3.14.

Figs. 3.16, 3.17 and 3.18 provide a comparison of the load-step-down responses between the conventional linear compensators and the proposed SOTC. Fig. 3.16 shows some dynamic oscillations when using a fast compensator with high bandwidth and small phase margin. In addition, Fig. 3.17 shows the response of a linear compensator with a bit lower bandwidth but larger phase margin. The oscillation is eliminated, but the response is slower. In terms of the state plane, there are many trajectories when jumping from the large heavy-load circle to the small light-load circle in both linear compensator designs.

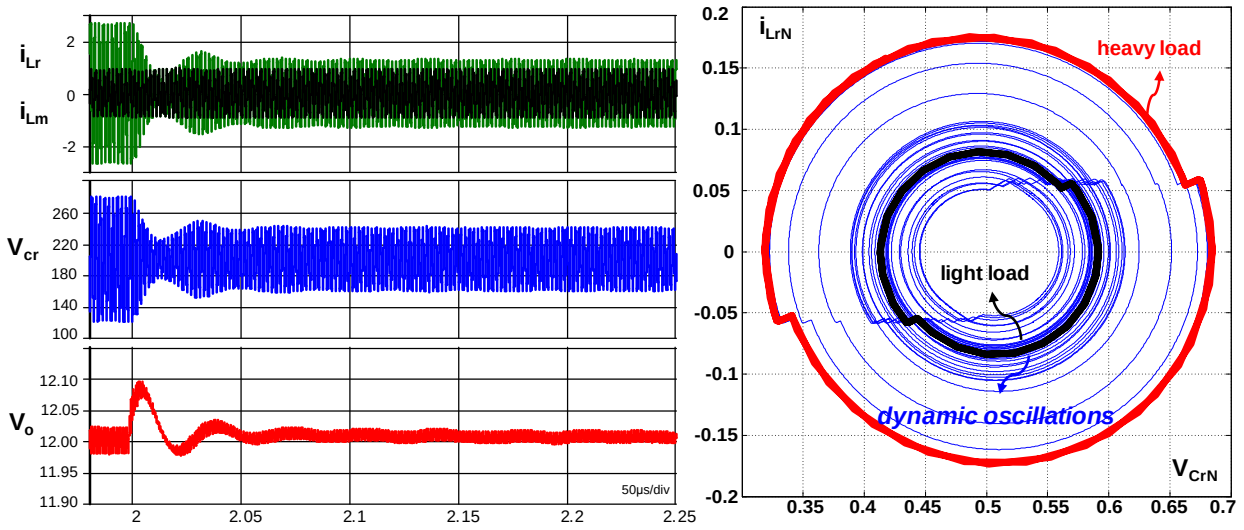


Fig. 3.16 Load-step-down response of a linear compensator with high bandwidth and small phase margin

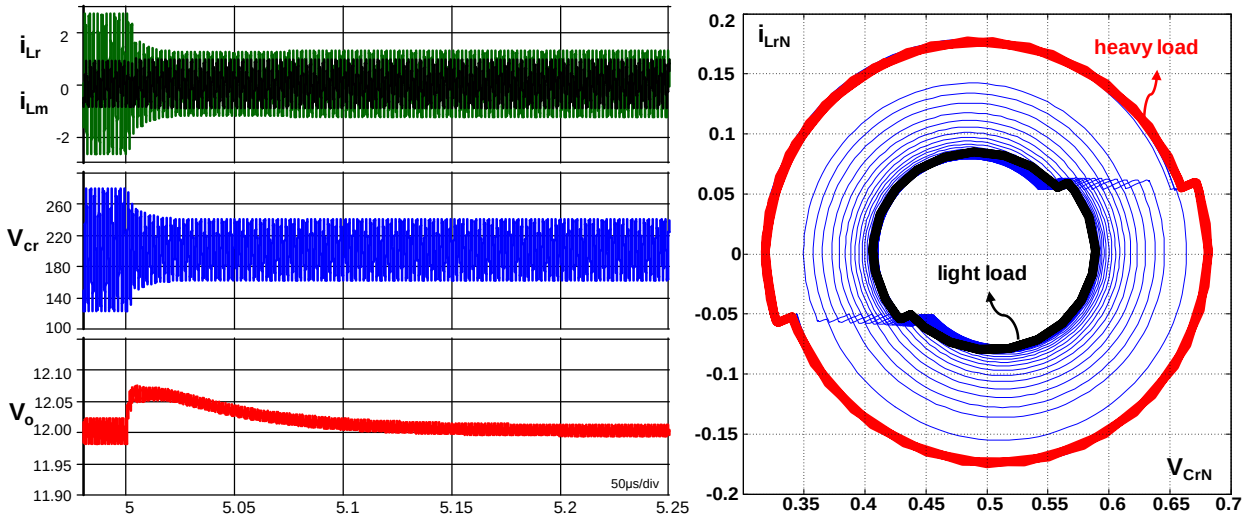


Fig. 3.17 Load-step-down response of a linear compensator with low bandwidth and large phase margin

If the SOTC is employed, Fig. 3.18 shows that there is almost no dynamic oscillation, and all the state variables quickly settle to the new light-load steady state. After the SOTC two-pulses tuning, the linear compensator takes less effort to converge to the new light-load steady state. Obviously, the trajectory is quite clean compared with that of the linear controls.

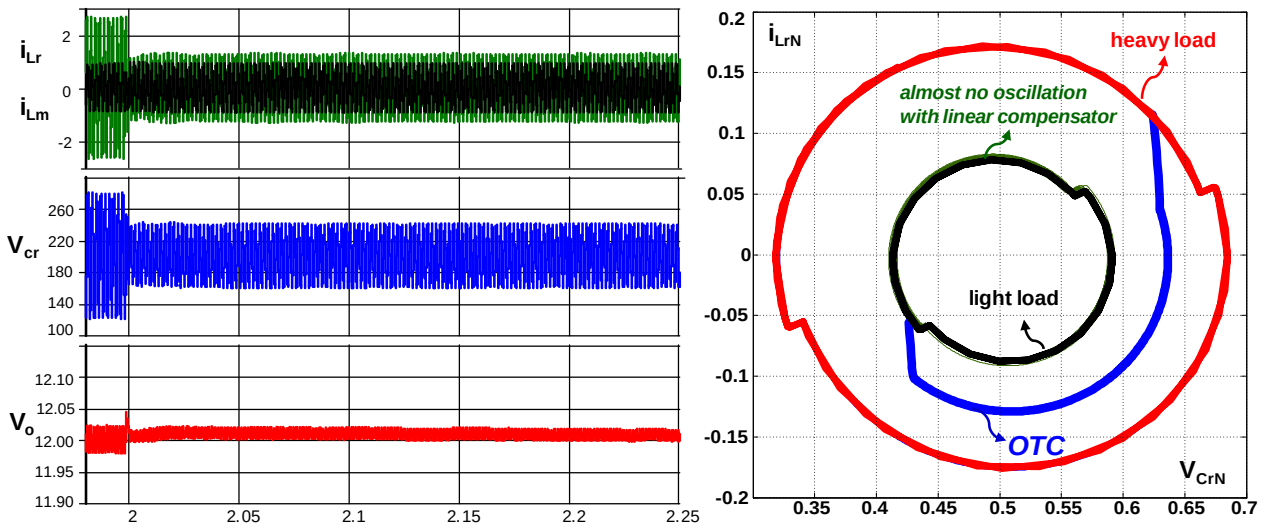


Fig. 3.18 Load-step-down response of the SOTC

3.4 Experimental Results

The experiment is carried out on a 300W 400V/12V half-bridge LLC resonant converter. The main converter parameters are shown in Table 3.1. The switching frequency is about 120 kHz under the steady state. The hybrid control system is built in the Cyclone III series FPGA. The converter prototype is shown in Fig. 3.19.

Table 3.1 The parameters of LLC resonant converter

Designed parameters	**Parameter Values**
Input Voltage (V_{in})	400V
Output Voltage (V_o)	12V
Resonant Capacitor (C_r)	24nF
Resonant Inductor (L_r)	60 μH
Transformer Magnetizing Inductor (L_m)	300 μH
Turns Ratio (n)	17:1:1
Output Capacitor (C_o)	440 μF

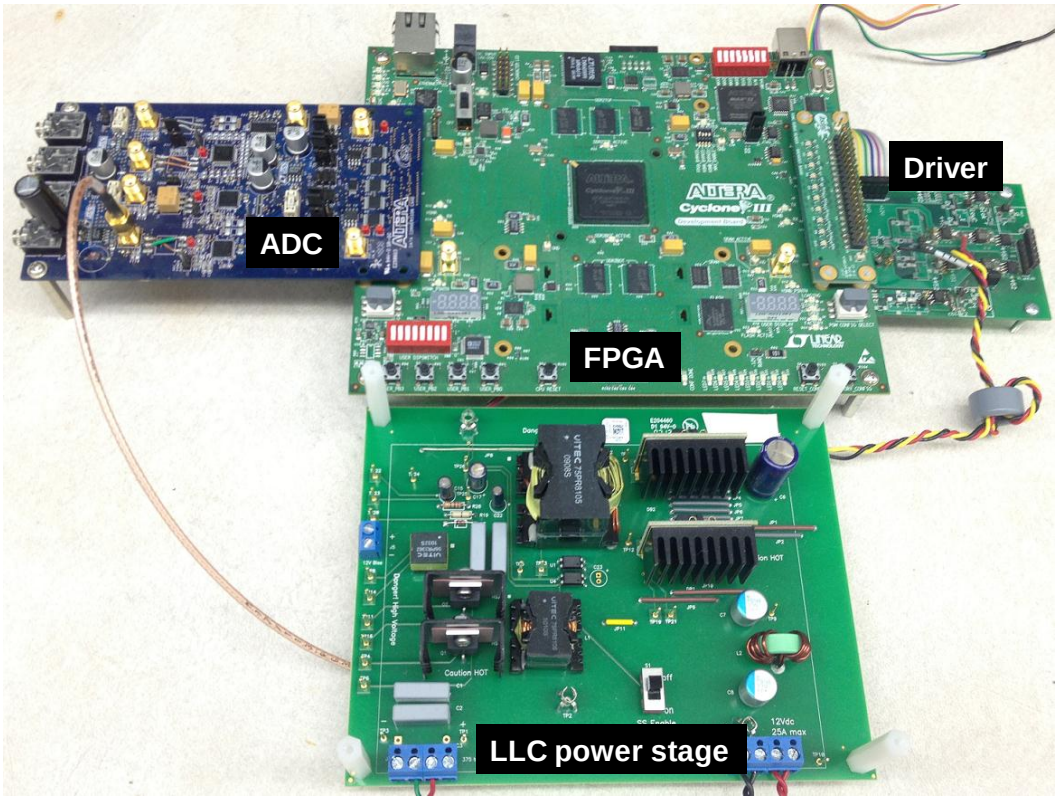


Fig. 3.19 Converter prototype

Besides the linear compensator, the total number of logic gates for the SOTC is only around 1400 in the FPGA. Thus, the hybrid digital implementation of Fig. 3.4 is very simple, but the performance improvement shown below is significant.

For the purpose of comparison, a conventional PI linear compensator has been designed with about 6kHz bandwidth and 45 ° phase margin. The transient response of load step-up from 5A to 15A is shown in Fig. 3.20, and some dynamic oscillations are presented.

When the SOTC is employed, the pulse width of the driving signal is increased about 0.45μs according to (3.10). After the load-step-up, the state variables follow the heavy-load steady state. Fig. 3.21 shows the dynamic improvement with less overshoot and smaller settling time.

The enlarged waveform at the load step-up transition is shown in Fig. 3.22. With the OTC, the pulse widths increase immediately. The resonant inductor current i_{Lr} settles to the heavy-load steady-state condition in the minimum time.

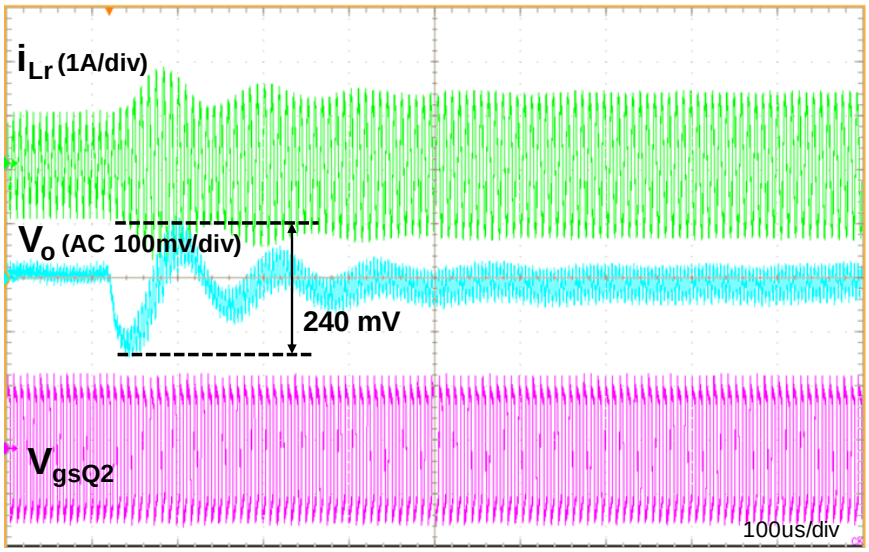


Fig. 3.20 Load step-up oscillation with a linear compensator

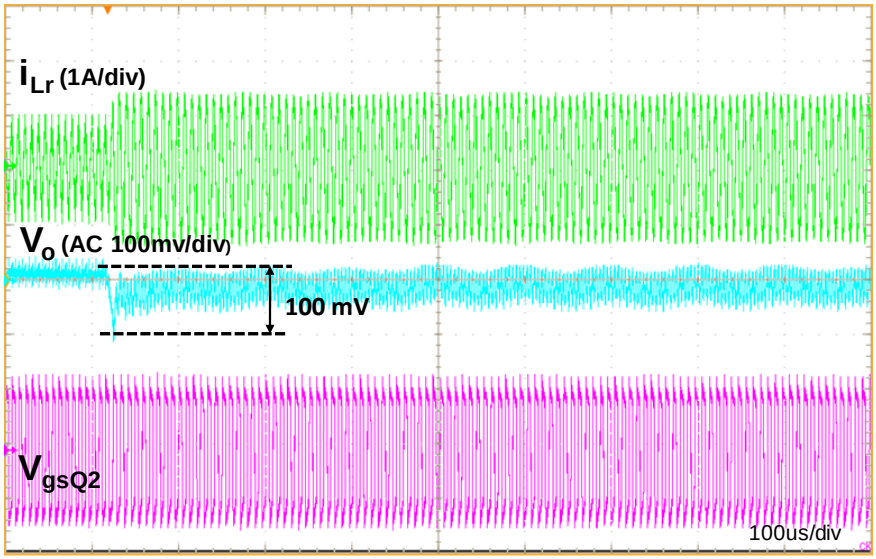


Fig. 3.21 Improved load step-up response with the SOTC

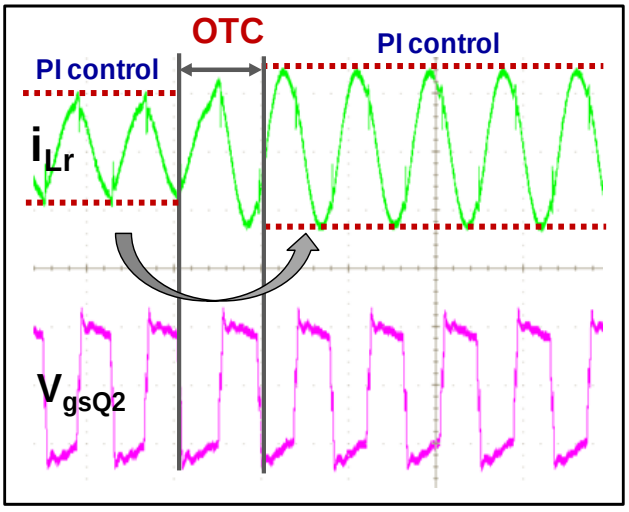


Fig. 3.22 Detailed waveform of the SOTC at the load-step-up moment

The transient response of the load step-down from 15A to 5A with the same PI compensator is shown in Fig. 3.23. Fig. 3.24 shows that the SOTC significantly improves the dynamic performance, reducing the overshoot to 100mV.

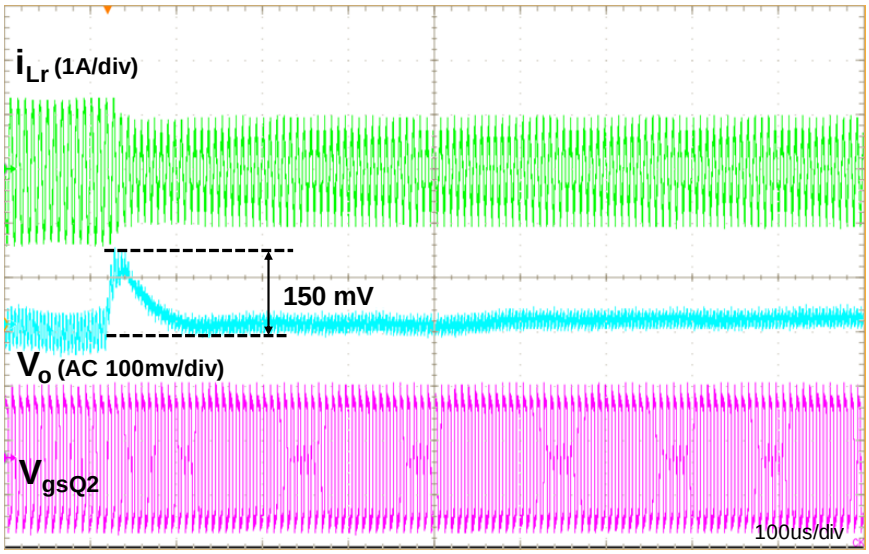


Fig. 3.23 Load step-down response with a linear compensator

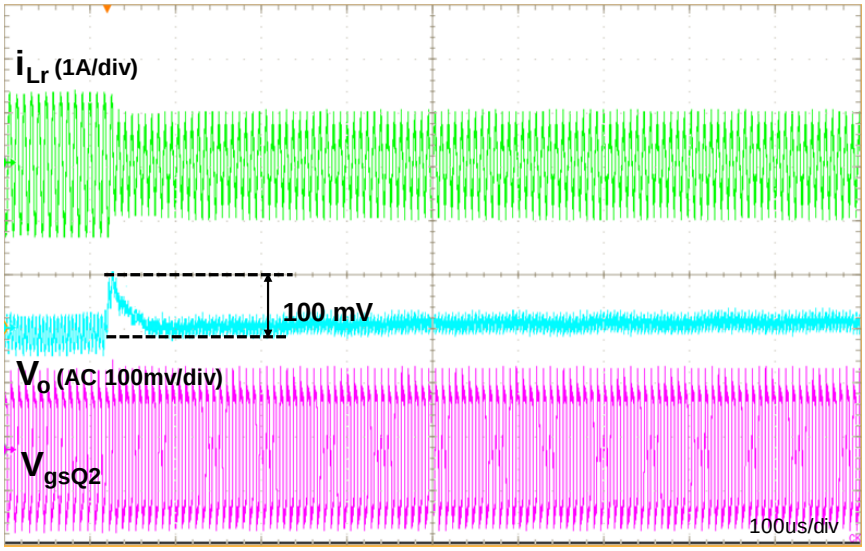


Fig. 3.24 Improved load step-down response with the SOTC

Finally, Fig. 3.25 illustrates that within the OTC, at the step-down instant, the pulse widths decrease about 0.9μs according to (3.20). Following the optimal trajectory in Fig. 3.14, the resonant inductor current i_{Lr} can settle to the light-load steady-state condition within the minimal period of time.

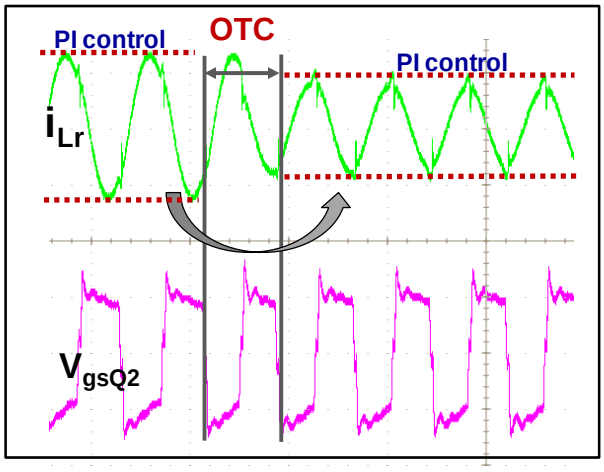


Fig. 3.25 Detailed waveform of the SOTC at the load-step-down moment

3.5 Conclusion

A simplified optimal trajectory control (SOTC) for LLC resonant converters is proposed. During steady-state conditions, a linear compensator is used, controlling the switching frequency to eliminate the steady-state error. During load transients, the optimal trajectory control (OTC) takes over, tuning the pulse widths of the gate driving signals based on the sensed load current. Using the state plane analysis, the pulse widths are calculated, letting the state variables track the desired trajectory within the minimum period of time. For the purpose of rapid prototyping, the proposed approach has been implemented in FPGA. It features simple implementation, dramatic improvement in load-step response and easy integration with existing controllers.

Chapter 4. Dynamic Improvement II: Optimal Trajectory Control for Soft Start-Up and Over-Load Protection

In this chapter, the soft start-up process for the LLC resonant converter is investigated and optimized based on a graphical state-trajectory analysis. By setting a current limitation band, several optimal switching patterns are proposed to settle the initial condition. After that, by sensing the output voltage, the optimal switching frequency is determined within the current limiting band. This virtually guarantees that there will be no current and voltage stress in the resonant tank during the soft start-up process and over-load protection. Meanwhile, the output voltage is built up quickly and smoothly. When it comes to the over-load protection, it is a reverse operation of the soft start-up. By applying the similar switching pattern, the resonant current and voltage stress is limited under the over-load condition.

4.1 Introduction

Fig. 4.1 shows the DC characteristic of the LLC resonant converter. Normally, the LLC operates near the resonant frequency point ($f_s=f_0$) to keep the best efficiency. During the hold-up time operation, the input voltage decreases while the output voltage should stay constant, thus the switching frequency decreases ($f_s<f_0$) to boost the voltage-gain. Under the soft start-up condition, the output voltage needs be built up from zero to the steady-state value, in order to prevent from entering the zero-current-switching (ZCS) zone, the LLC should work in above resonant frequency region ($f_s>f_0$).

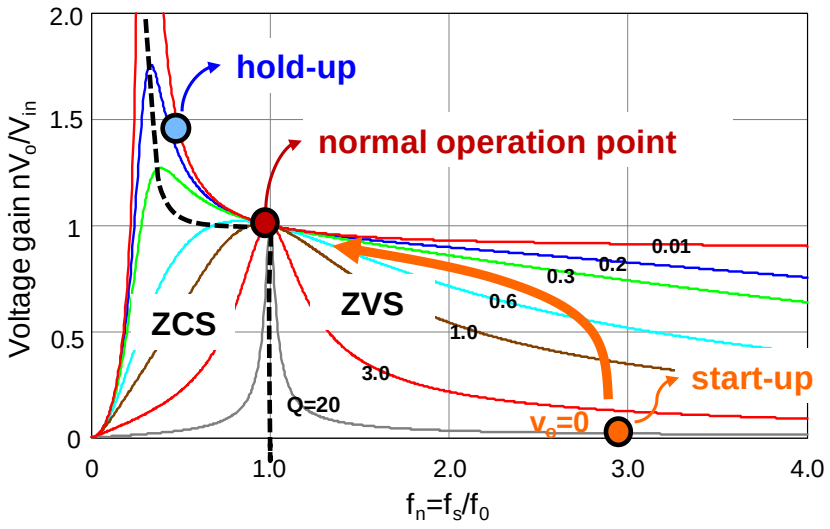


Fig. 4.1 DC characteristic of the LLC resonant converter

However, as shown in Fig. 4.2, if the start-up switching frequency (f_s) is not high enough as in [A.38-A.49], large voltage and current stress can happen at the start-up moment. Otherwise, as shown in Fig. 4.3, if the LLC starts up with a higher frequency [A.40-A.41], at the beginning, the voltage and current stress will be small. However, during the soft start-up process, if f_s decreases too quickly, large voltage and current stress can still happen, which will trigger the over-current-protection. As a result, f_s will increase a bit to limit the stress, and then decreases smoothly to finish the soft start process. If f_s decreases slowly, the stress will stay small, but the output voltage will build up slowly, which means, the soft start-up process will take much longer.

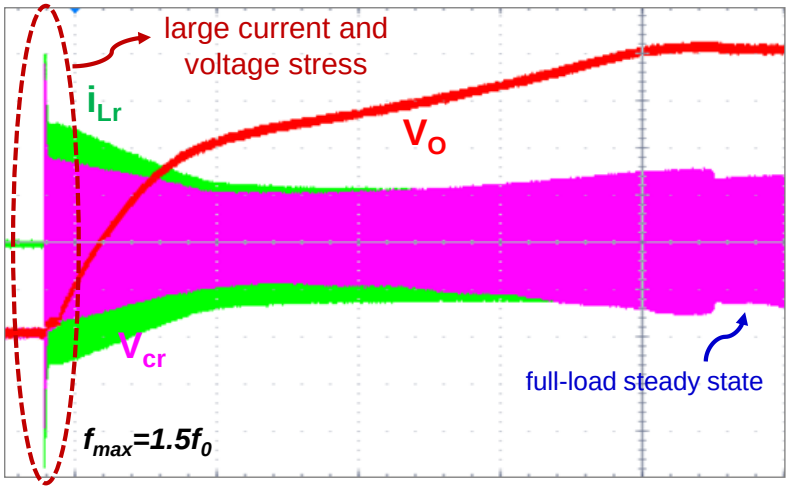


Fig. 4.2 Soft start-up with a low switching frequency

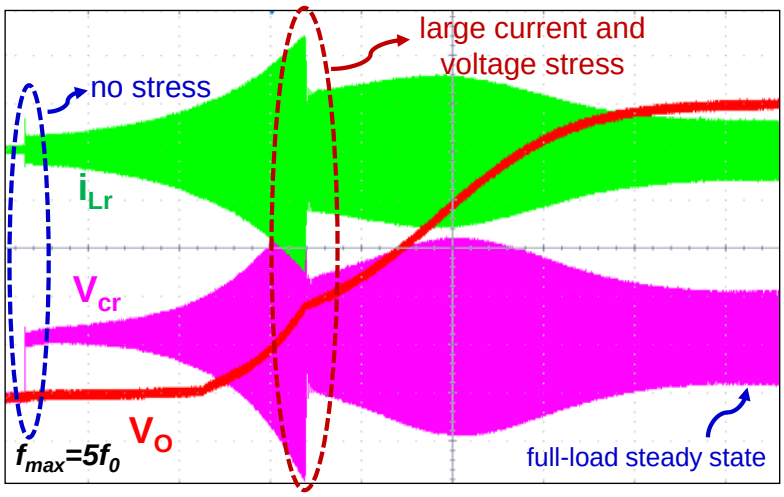


Fig. 4.3 Soft start-up with a high switching frequency

Besides the frequency control, phase-shifted control can be used in full-bridge LLC to limit the voltage and current stress during the soft start process. Fig. 4.4 shows steady state waveforms when $f_s=2f_0$ with $\pi/2$ phase shift. For the leading leg (Q_1 and Q_3), it is easy to realize ZVS, since the resonant current is large at the turn-off moment. However, for the lagging leg (Q_2 and Q_4), it

is hard to achieve ZVS due to the lower current to charge the junction capacitors at the turn-off instant.

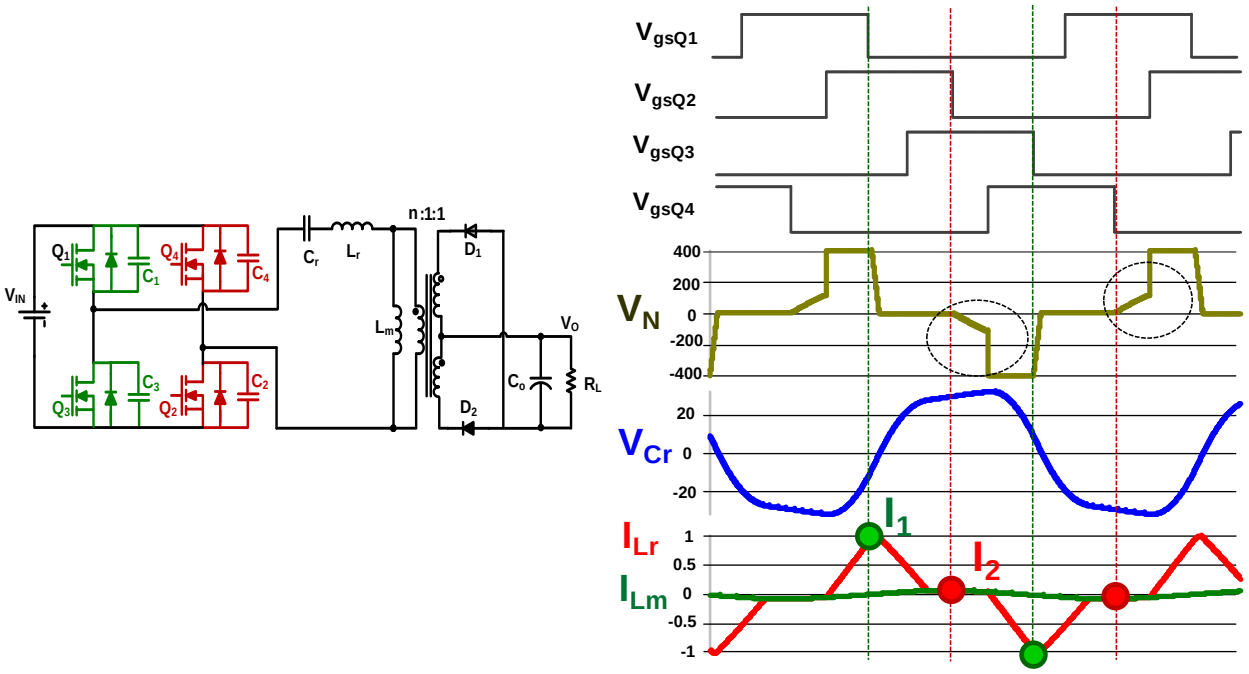


Fig. 4.4 Phase-shifted control in full-bridge LLC ($f_s=2f_0$, $\Phi=\pi/2$)

Under the normal operation condition ($f_s=f_0$), at each switching instant, the resonant current i_{Lr} is equal to the magnetizing current i_{Lm}. The dead-time is designed to realize ZVS by charging and discharging the MOSFET junction capacitors with $i_{ZVS}=i_{Lm}$. If the switching instant current is smaller than i_{Lm}, ZVS cannot be fully achieved. As shown in Fig. 4.5, when mapping the steady state resonant voltage and current in Fig. 4.4 to the state plane, the lagging leg switching instants locate in the ZVS lost zone.

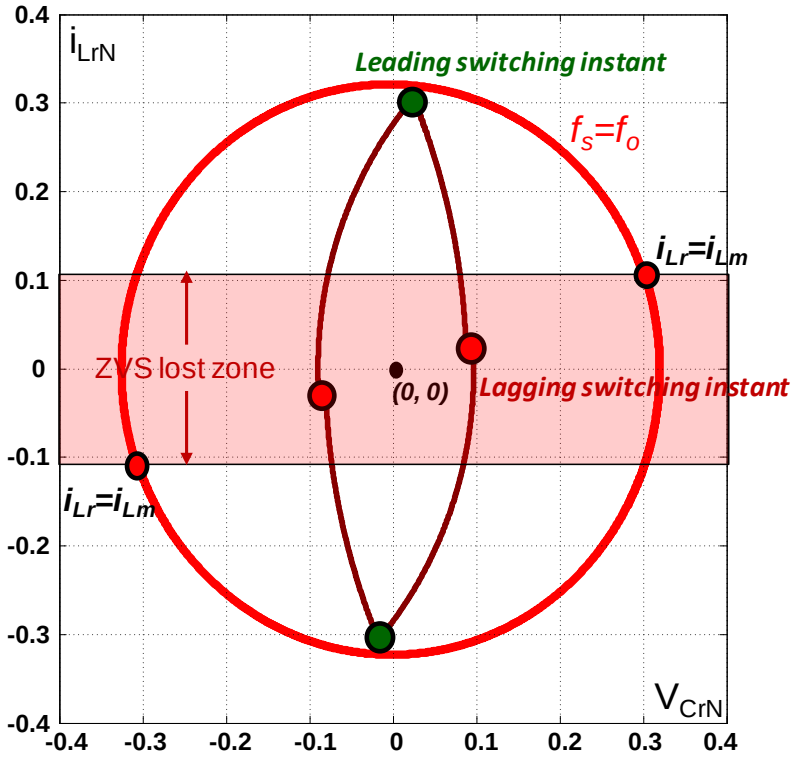


Fig. 4.5 State-trajectory of phase-shifted control ($f_s=2f_0$, $\Phi=\pi/2$)

Fig. 4.6 shows the simulated soft start-up process with the phase-shifted control. Initially, the maximum switching frequency is limited to $2f_0$, and the shifted phase is maximum (i.e. $\Phi=\pi$). As the shifted phase decreases, the resonant voltage v_{Cr}, resonant current i_{Lr} and output voltage Vo increase smoothly, and there is no stress. However, at the start-up moment, the whole trajectory is in the ZVS lost zone, because i_{Lr} is too small to achieve ZVS. In addition, in the start-up process, for the lagging leg switches, it is hard to fully realize ZVS due to the small switching current.

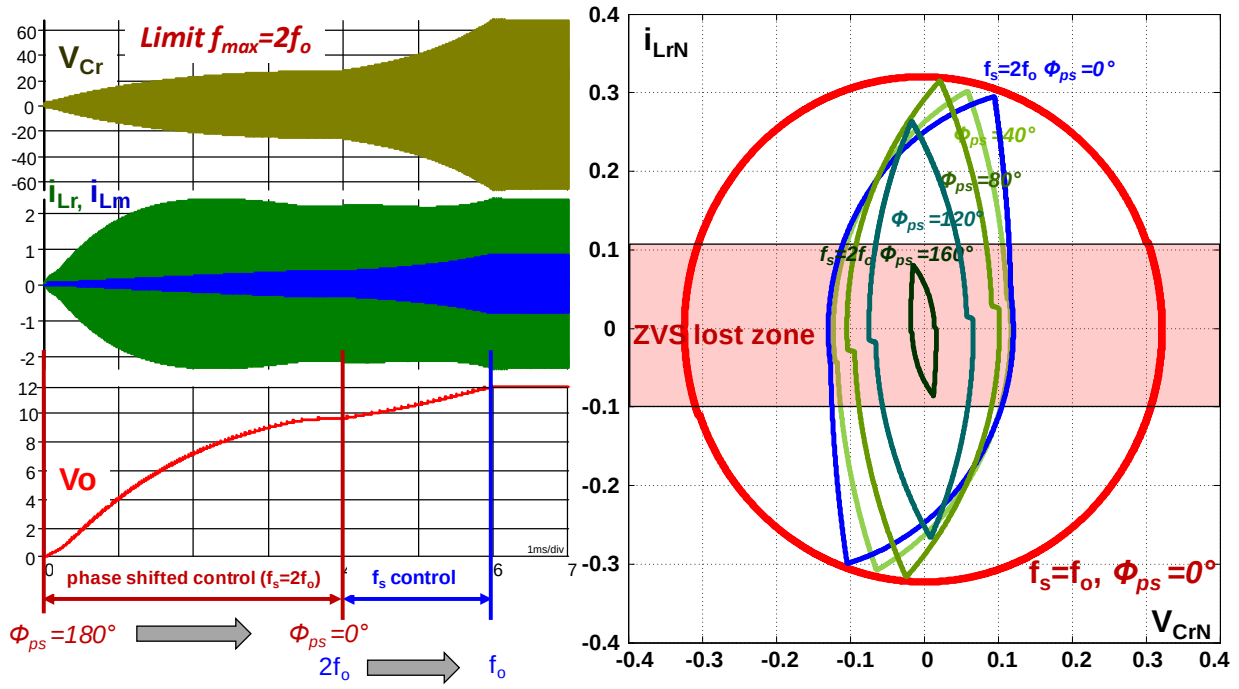


Fig. 4.6 Soft start-up with phase-shifted control

Therefore, an optimal control is required for the LLC soft start-up. The resonant voltage and current stress should be limited, the output voltage should be built up quickly and smoothly, and the ZVS of all switches should be guaranteed.

4.2 Optimal Switching Patterns Settling Initial Condition

To limit the stress, a resonant current limitation band is set. During the soft start-up, all current stress is limited to this band, and thus, the resonant voltage stress is limited as well. As shown in Fig. 4.7, under the steady state, when LLC operates near the resonant frequency point, the current is sinusoid. When the LLC starts up in above resonant frequency region, the initial current is triangle.

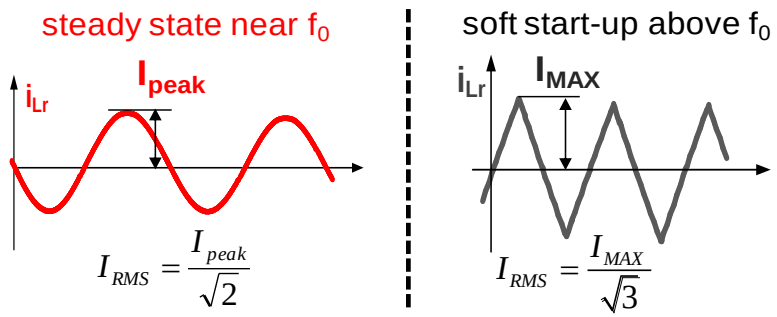


Fig. 4.7 Waveform difference under steady-state and start-up

To guarantee the LLC is operating in the safe zone, from the loss point of view, the same RMS value of sinusoid and triangle waveforms is desired. Thus, the current limitation band can be determined as

$$I_{MAX} = \frac{\sqrt{3}}{\sqrt{2}} I_{peak}, \tag{4.1}$$

where I_{peak} is the peak resonant current under the full-load steady state. As shown in Fig. 4.8, on the state plane, the red circle represents the full-load steady-state trajectory, with center (0.5, 0) and radius I_{peakN}. The up and bottom limits as in (4.1) determine the current limitation band. The subscript *N* means the normalized value.

At the start-up moment, there is no energy in the resonant tank, which means that the resonant inductor current and the capacitor voltage both are zero (i.e. i_{Lr}=0, v_{Cr}=0). Thus, on the state plane, the initial point is (0, 0). Before running, the LLC output voltage is zero (i.e. V_o=0). Fig. 4.8 shows the equivalent circuit at the start-up moment.

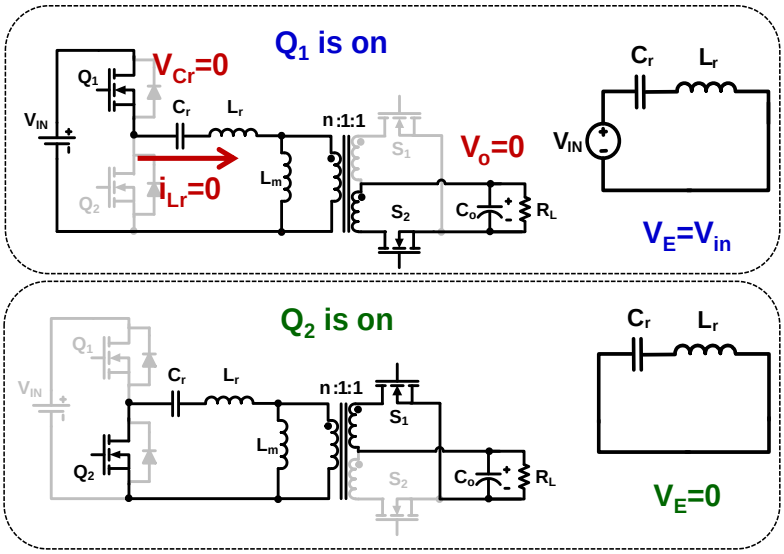


Fig. 4.8 Equivalent circuits when LLC starts up

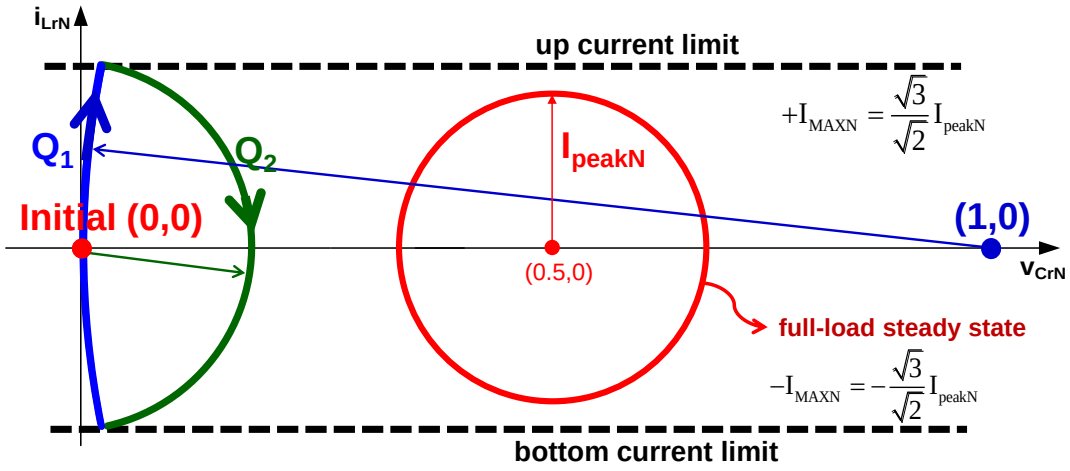


Fig. 4.9 Initial trajectories within the symmetrical current limiting band

As shown in Fig. 4.9, when the LLC firstly starts up, the up-side switch Q_1 conducts, going through the partial circle with center (1, 0) from the initial point (0, 0). By limiting i_{Lr} to the current band, when it hits the up-limit ($+I_{MAXN}$), Q_1 is turned off. After that, Q_2 is turned on, and the center of the trajectory circle changes to (0, 0) as illustrated in Fig. 4.9. When the trajectory hits the bottom limit ($-I_{MAXN}$), Q_2 is turned off, and then Q_1 conducts again. Since the initial point

is (0, 0), if within the symmetrical band ($\pm I_{MAXN}$), from the graphic trajectory, the state variables are fixed to these two partial circles, which are far away from the final steady-state circle with center (0.5, 0).

Then the energy transports to the load gradually, and the output voltage V_o starts to increase. Compared with two modes in Fig. 4.8 at the start-up moment, there will be four operation modes as shown in Fig. 4.10. From the state-plane, previous two centers (0, 0) and (1, 0) will split into four centers such as ($-V_{oN}$, 0), (V_{oN}, 0), ($1-V_{oN}$, 0) and ($1+V_{oN}$, 0) when V_o increases, and trajectory is made up of four partial circles as shown in Fig. 4.11. By limiting i_{Lr} to the symmetrical current band, the trajectory will gradually approach to the steady state circle.

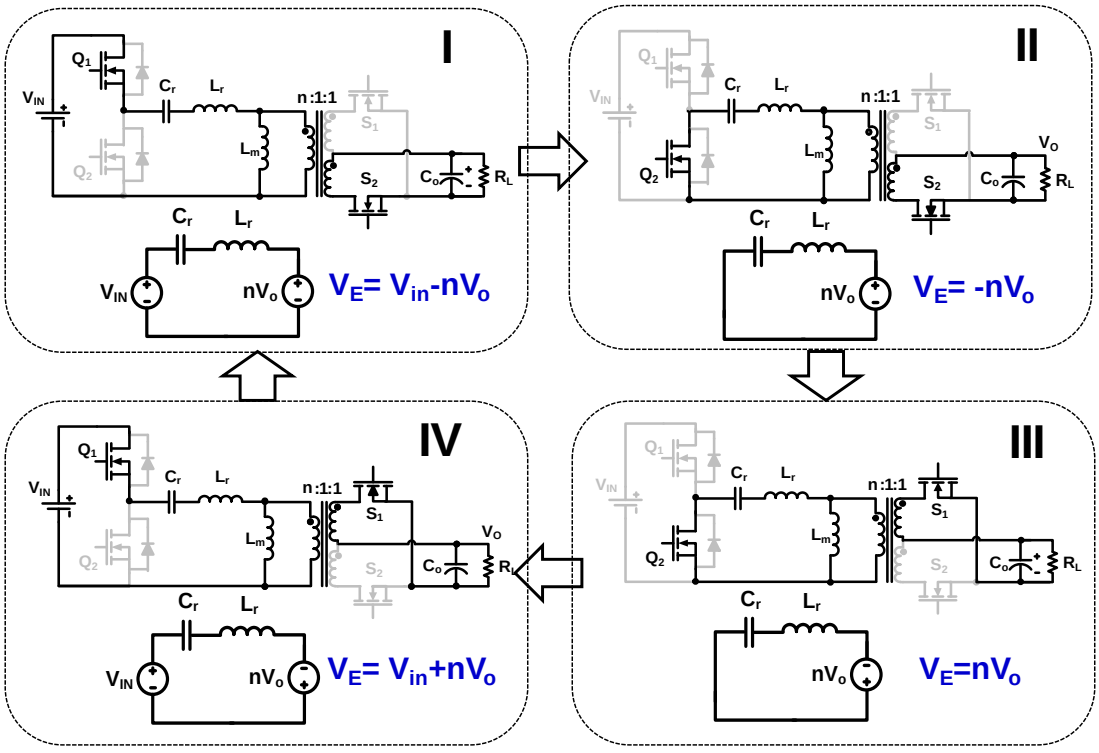


Fig. 4.10 Four operation modes when V_o increases

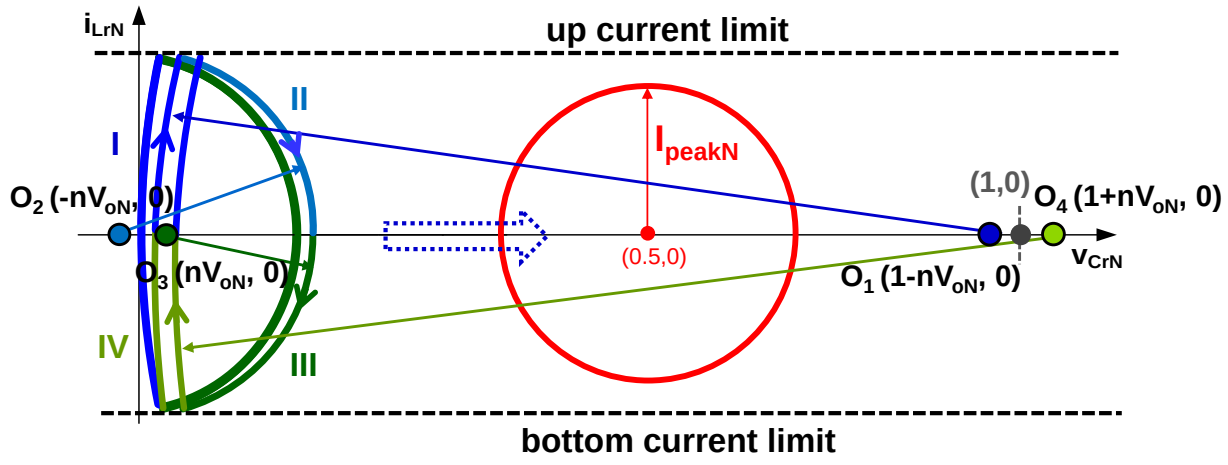


Fig. 4.11 Trajectory movement as V_o increases

However, as shown in Fig. 4.12, if limiting the resonant current i_{Lr} to the symmetrical band, as the output voltage increases, it takes lots of switching cycles to settle the resonant capacitor voltage to $V_{in}/2$. The corresponding trajectory is shown in Fig. 4.13.

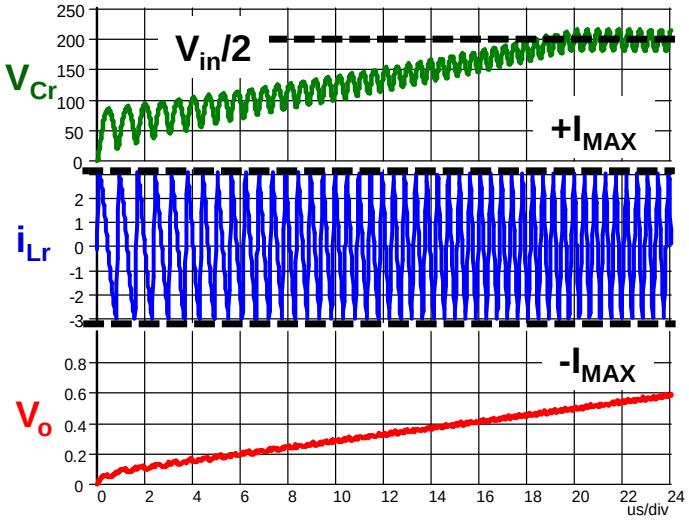


Fig. 4.12 Simulated time-domain waveforms of initial condition settling within symmetrical band

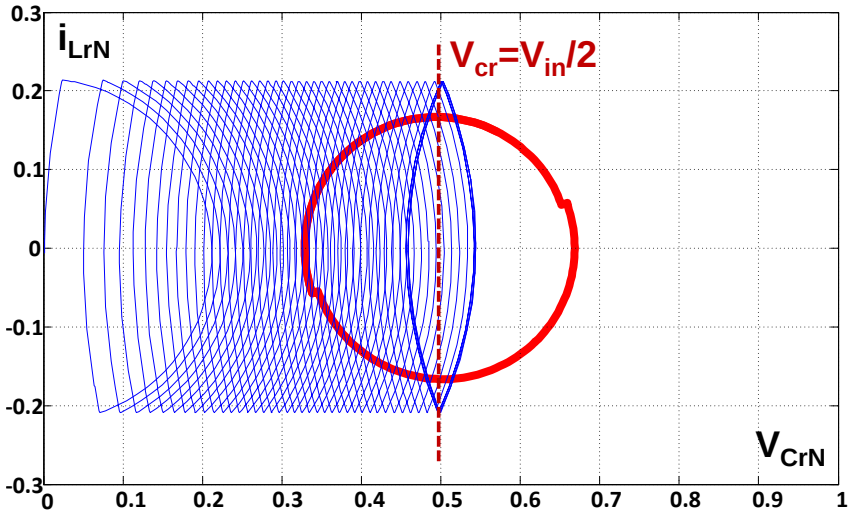


Fig. 4.13 State-trajectory within the symmetrical band to settle initial condition

Therefore, an unsymmetrical current limiting band is employed to speed the resonant capacitor voltage settling. As shown in Fig. 4.14, to fulfill ZVS, the low limit is set to be the switching instant current under the steady state (i.e. $-I_{Lm}$). The simulated time-domain waveform and state-trajectory are shown in Fig. 4.15. Obviously, within the unsymmetrical band, the initial state variables will converge to (0.5, 0) quickly.

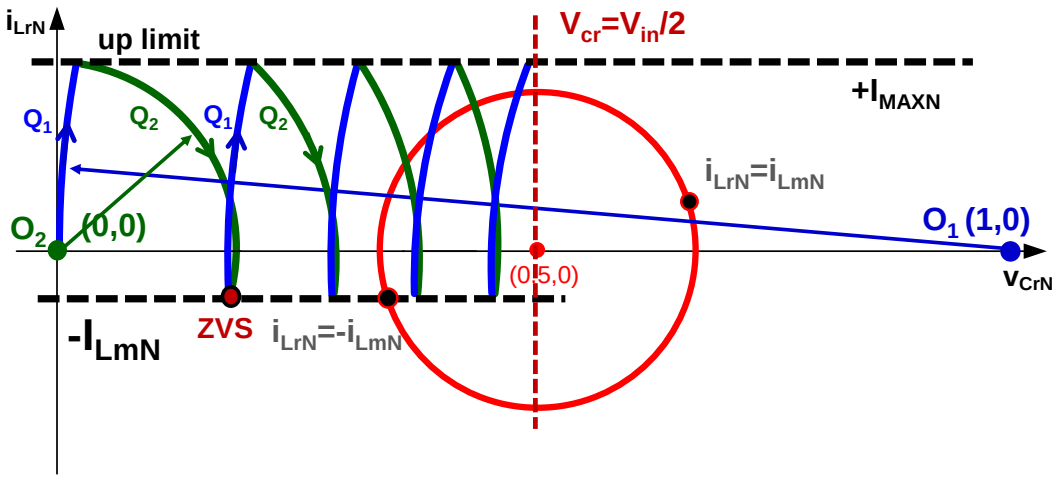


Fig. 4.14 Initial trajectories within the unsymmetrical current limiting band

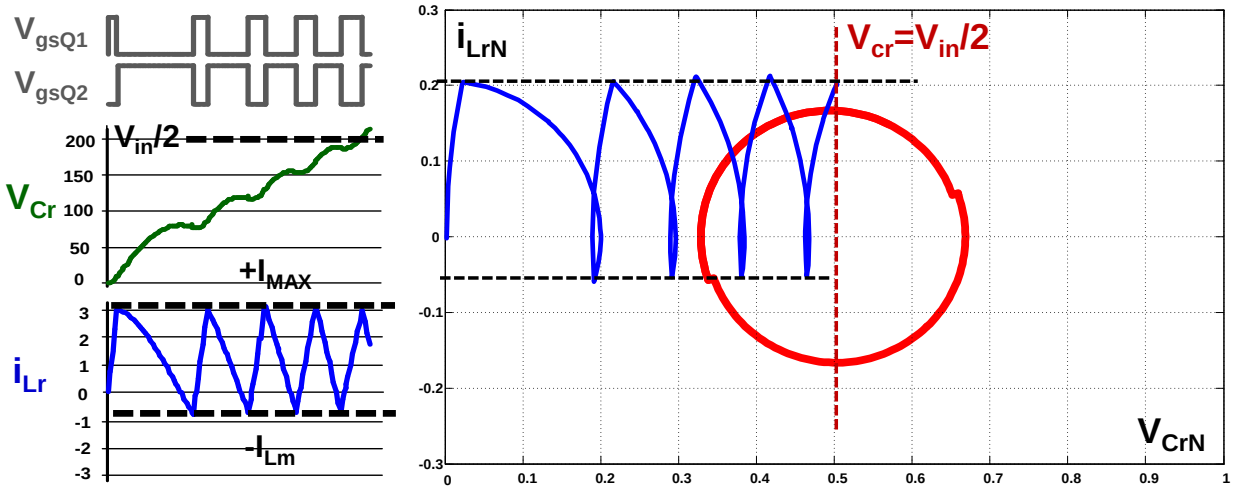


Fig. 4.15 Simulated time-domain waveform and state trajectory with unsymmetrical band

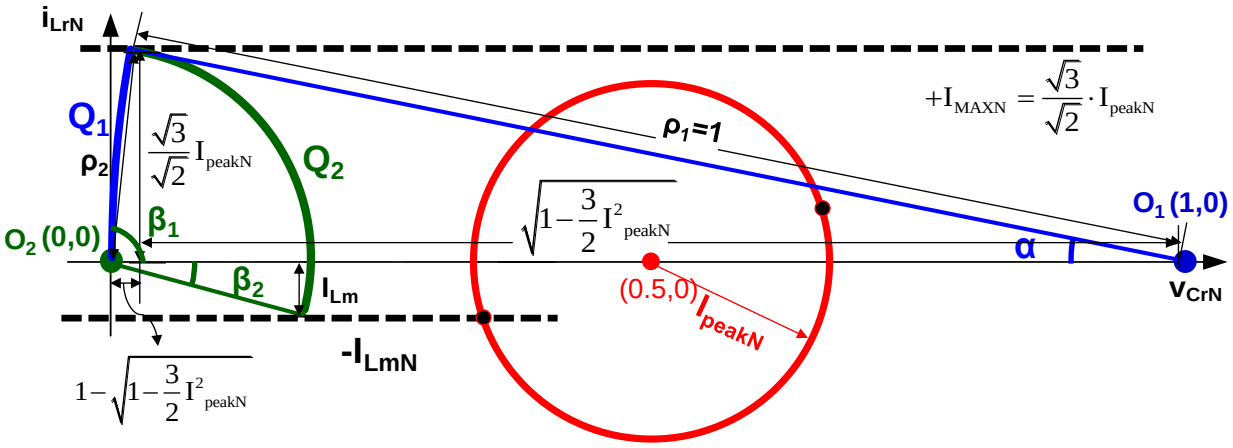


Fig. 4.16 Calculation of the optimal switch pattern in the unsymmetrical band

Based on the graphic trajectory analysis as shown in Fig. 4.16, the optimal pulse widths of Q_1 and Q_2 to settle the initial condition can be calculated below.

From [A.33], when $f_s=f_0$, the expression of peak value (I_{peakN}) of the resonant current is

$$I_{peakN} = \frac{1}{4}\frac{V_o}{nR_L}\sqrt{\frac{n^4 R_L{}^2 T^2}{L_m{}^2} + 4\pi^2} \Big/ \frac{V_{in}}{Z}, \tag{4.2}$$

where n is the transformer turn ratio, R_L is the full-load resistor, and T is the resonant period, L_m is the magnetizing inductor, $Z = \sqrt{L_r / C_r}$ is the resonant tank impedance.

Thus, according to (4.1) and (4.2), the current limitation band $\pm I_{MAXN}$ can be pre-determined.

As shown in Fig. 4.16, Q_1 conducts first. On the state plane, since the radius of Q_1 trajectory circle is 1 (i.e. ρ_1=1), the conduction angle α can be calculated as

$$\alpha = \sin^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN} \Big/ \rho_1\right) = \sin^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right). \tag{4.3}$$

To determine Q_1 first pulse width, convert the state-plane angle α to the time-domain conduction time ΔT_1:

$$\Delta T_1 = \frac{\alpha}{\omega_0}, \tag{4.4}$$

where ω_0 is the resonant frequency $\omega_0 = 1/\sqrt{L_r C_r}$.

From the state plane shown in Fig. 4.16, the radius of Q_2 partial circle (ρ_2) can be calculated as

$$\rho_2 = \sqrt{\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2 + \left(1 - \sqrt{1 - \left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2}\right)^2} = \sqrt{2 - 2\sqrt{1 - \left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2}}. \tag{4.5}$$

Thus Q_2 conduction angle β is

$$\beta = \beta_1 + \beta_2 = \sin^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN} \Big/ \rho_2\right) + \sin^{-1}\left(I_{LmN} / \rho_2\right), \tag{4.6}$$

where I_{LmN} is the normalized current at the switching instant under the steady-state operation, that is,

$$I_{LmN} = \frac{nV_o}{L_m} \cdot \frac{T}{4} \Big/ \frac{V_{in}}{Z}. \tag{4.7}$$

Similarly, converting the state-plane angle β to the time-domain, the first pulse width of Q_2, that is the conduction time ΔT_2, can be estimated as

$$\Delta T_2 = \frac{\beta}{\omega_0}. \tag{4.8}$$

As this process continues, the left pulse widths of Q_1 and Q_2 as shown in Fig. 4.15 are calculated step-by-step, until the resonant capacitor voltage has been built up close to $V_{in}/2$.

In order to settle the initial condition quickly, the one-cycle control is proposed as shown in Fig. 4.17. With similar calculation steps from (4.1) to (4.8), after Q_1 and Q_2 conduct for one switching cycle, the resonant capacitor voltage can be built to $V_{in}/2$ in the minimum time. However, when compared with unsymmetrical band settling as in Fig. 4.14, there will be a bit

more current stress. In order to accelerate the converging process to $V_{in}/2$, while reducing the current stress, a slope band is applied as shown in Fig. 4.18.

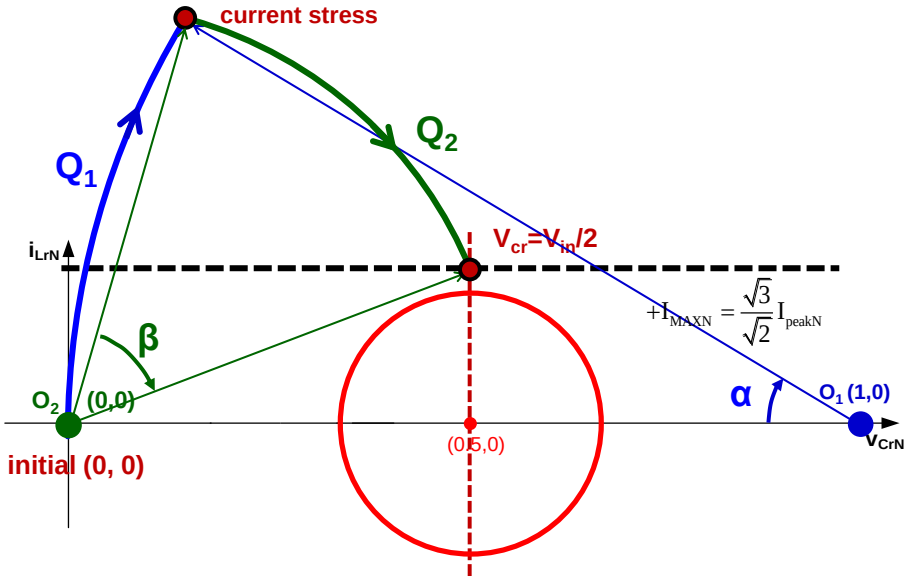


Fig. 4.17 Initial condition settling with one-cycle approach

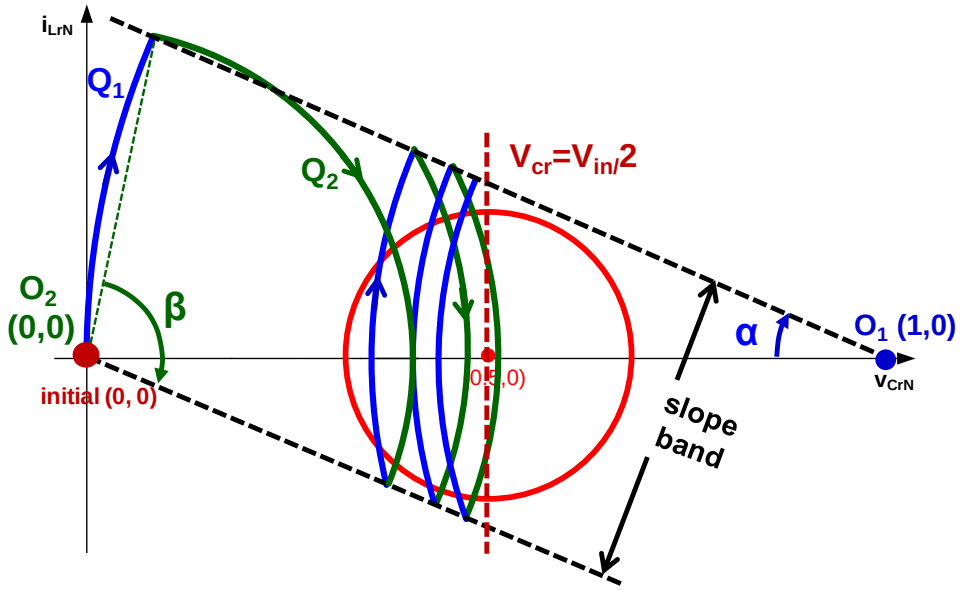


Fig. 4.18 Initial condition settling with slope-band approach

4.3 Optimal Trajectory Control during Soft Start-up

After settling the initial condition by building the resonant capacitor voltage to $V_{in}/2$, the current limitation band is changed to be symmetrical ($\pm I_{MAXN}$) to maximally transport the energy. At the beginning, since the output voltage has not been built up yet (i.e. V_o=0), the centers of the trajectory circles locate at (0, 0) and (1, 0) respectively. To limit the resonant current i_{Lr} into the symmetrical band, two partial circles could be uniquely determined as shown in Fig. 4.19. And the conduction angle φ could be determined as:

$$\varphi = \tan^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN} \Big/ 0.5\right). \tag{4.9}$$

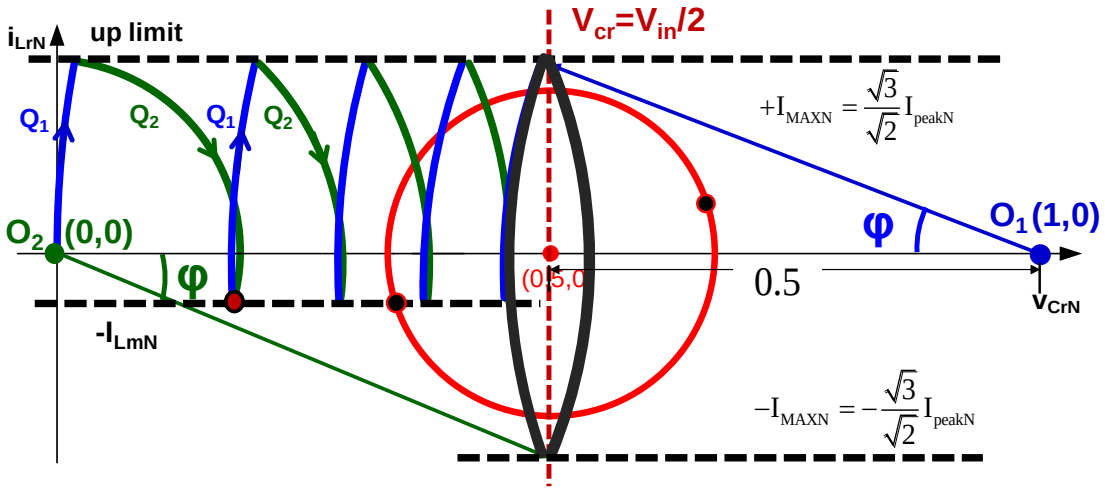


Fig. 4.19 Optimal switching frequency after settling the initial condition

At this moment, the conduction time of Q_1 and Q_2 is the same, which is

$$T_1 = T_2 = \frac{2\varphi}{\omega_0}. \tag{4.10}$$

Thus, after building the resonant capacitor voltage to $V_{in}/2$, the initial switching frequency at the start-up moment can be determined as

$$f_{ss\_ini} = \frac{1}{T_1 + T_2}. \tag{4.11}$$

The corresponding time-domain waveform is shown in Fig. 4.20. The unsymmetrical band is set to build the resonant capacitor voltage to $V_{in}/2$ as described in Section 4.2. After that, the current limitation is changed to the symmetrical band. The optimal start-up frequency is determined from (4.9) to (4.11). The resonant current i_{Lr} is well limited to the pre-determined band.

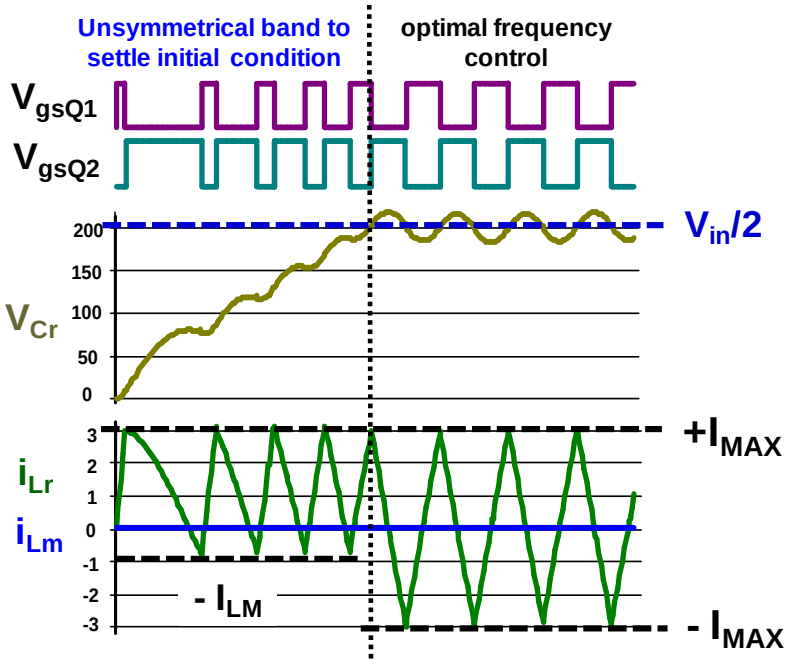


Fig. 4.20 Optimal trajectory control at the start-up moment

When the soft start-up continues, the output voltage V_o starts to increase smoothly. There will be four operation modes as shown in Fig. 4.10. By limiting i_{Lr} into the symmetrical current band, the trajectory is uniquely determined as well, made up of four partial circles as shown in Fig. 4.21.

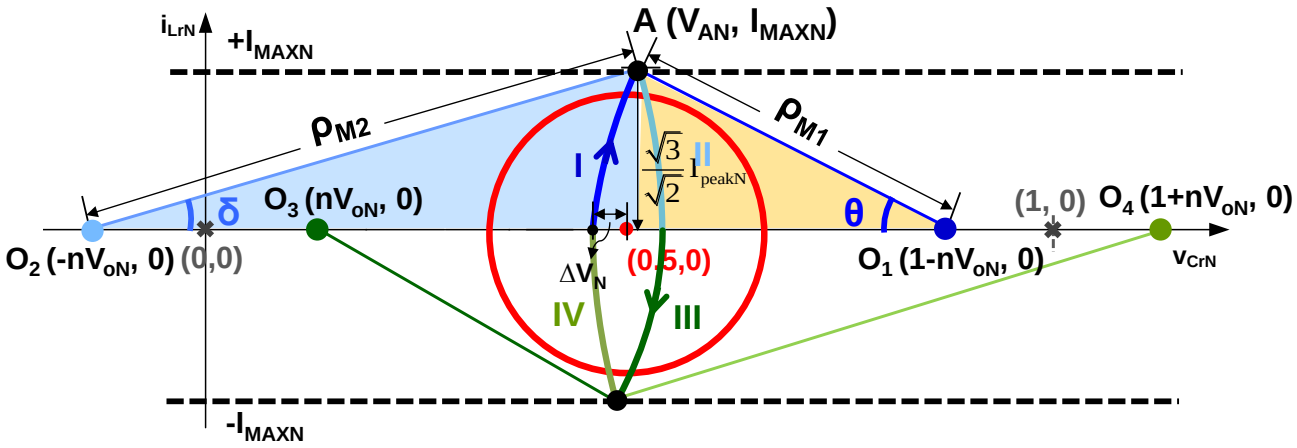


Fig. 4.21 Optimal trajectory control in the current limitation band as V_o increases

Knowing the trajectory when the output voltage increases, the optimal frequency can be determined as below.

The radius of the trajectory circle in Stage I (ρ_{M1}) is

$$\rho_{M1} = \left(\left(1 - nV_{oN}\right) - 0.5\right) + \Delta V_N, \tag{4.12}$$

where ΔV_N is the distance from (0.5, 0) to the point where the trajectory hits the V_{crN} axis.

The radius of the trajectory circle in Stage II (ρ_{M2}) is

$$\rho_{M2} = \left(0.5 - \left(-nV_{oN}\right)\right) + \Delta V_N. \tag{4.13}$$

Solve two triangles in Fig. 4.21, since

$$\left(V_{AN} - \left(1 - nV_{oN}\right)\right)^2 + \left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2 = {\rho_{M1}}^2, \tag{4.14}$$

$$\left(V_{AN} - \left(-nV_{oN}\right)\right)^2 + \left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2 = {\rho_{M2}}^2, \tag{4.15}$$

where V_{AN} is the normalized capacitor voltage at point A. From (4.12) to (4.15), ΔV_N is calculated as

$$\Delta V_N = \sqrt{\frac{1}{4} + \frac{\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN}\right)^2}{1 - 4\left(nV_{oN}\right)^2}} - 0.5. \tag{4.16}$$

Therefore, knowing the output voltage V_o, the radiuses ρ_{M1} and ρ_{M2} is determined from (4.12), (4.13) and (4.16).

After that, the conduction angle θ in Stage I and δ in Stage II are

$$\theta = \sin^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN} \Big/ \rho_{M1}\right), \tag{4.17}$$

$$\delta = \sin^{-1}\left(\frac{\sqrt{3}}{\sqrt{2}} I_{peakN} \Big/ \rho_{M2}\right). \tag{4.18}$$

Thus, the corresponding optimal switching frequency is

$$f_{s\_opt} = \frac{1}{\frac{2(\theta+\delta)}{\omega_0}}. \tag{4.19}$$

The simulated time-domain waveform with the optimal switching frequency in (4.19) is shown in Fig. 4.22, where the resonant current is well limited to the band ($\pm I_{MAX}$).

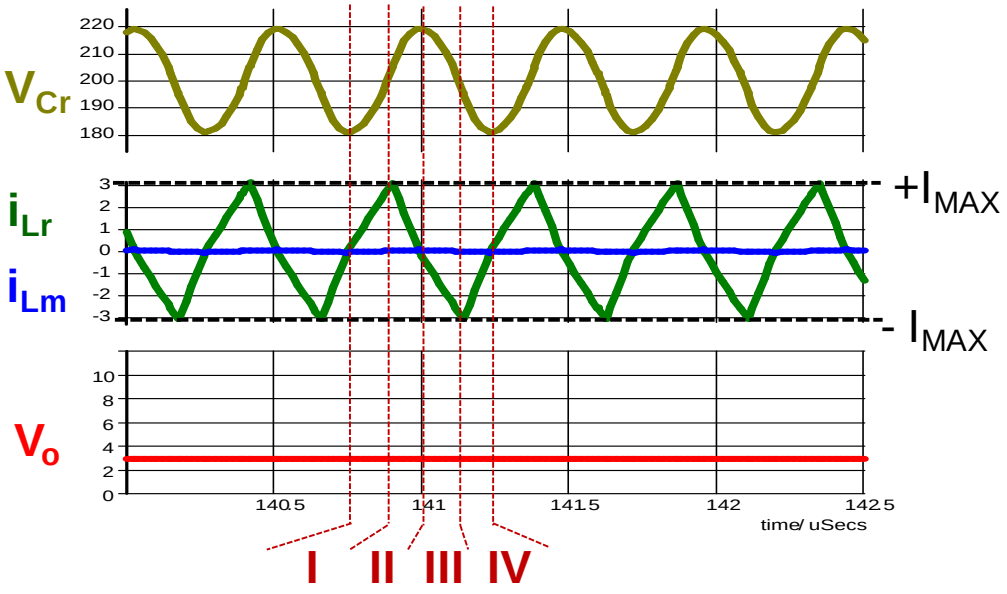


Fig. 4.22 Time-domain waveform of optimal control as V_o increases

To sum up, setting the current limitation band $\pm I_{MAXN}$, and then sensing the output voltage V_{oN}, the optimal switching frequency f_{s_opt} can be determined during the soft start-up process.

The output voltage gradually increases as the start-up continues. When it is close to the steady state, as shown in Fig. 4.23, the resonant current waveform changes to a sinusoid shape from a triangle one. Thus, in order to keep the same RMS value, the current limitation band

should decrease step-by-step, finally to I_{peak}. The corresponding trajectory is shown in Fig. 4.24. The current limitation band changes from I_{MAXN} to I'_{MAXN}, finally to I_{peakN} when it reaches the full-load steady state. Similarly, based on the graphic trajectory analysis, the optimal frequency can be determined as well.

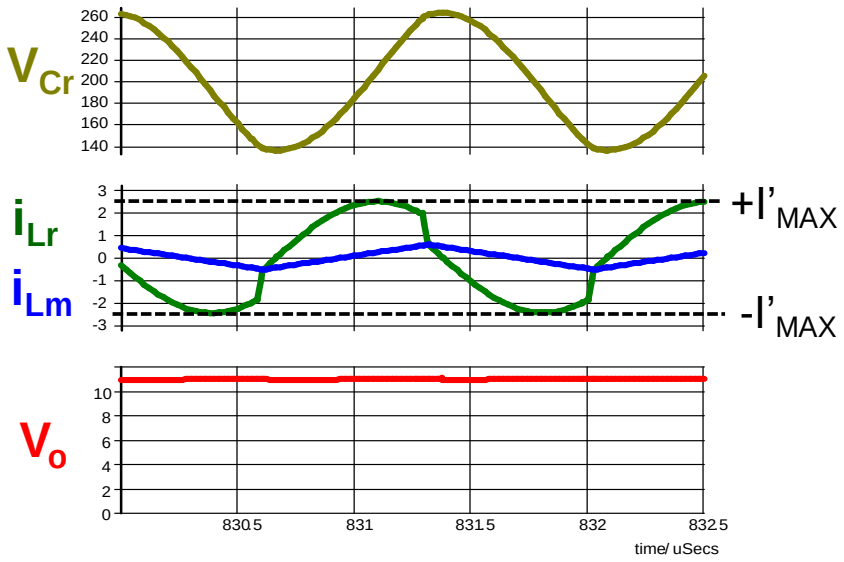


Fig. 4.23 Time domain waveform of reduced band as V_o approaches to steady state

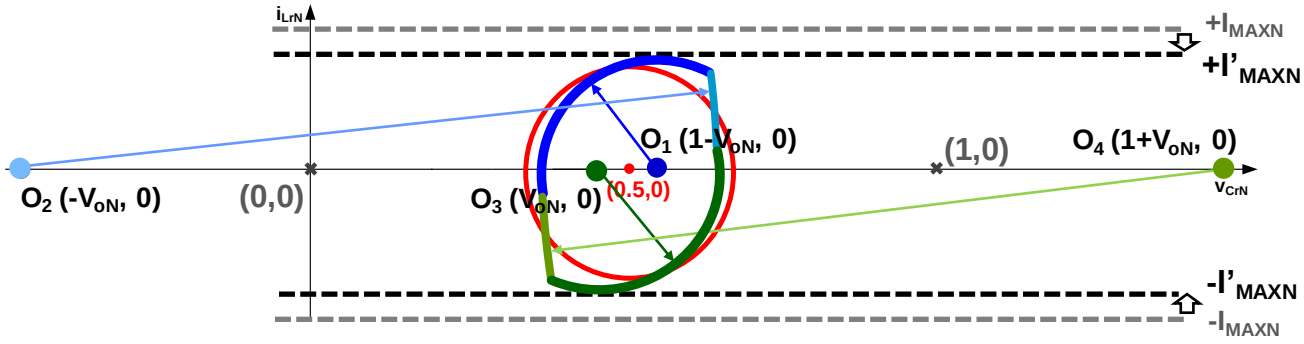


Fig. 4.24 Optimal trajectory with reduced band as V_o approaches to steady state

Figure 4.25 shows the whole process of the proposed optimal soft start-up. Initially, the resonant capacitor voltage v_{Cr} is built to $V_{in}/2$ quickly as discussed in Section II. Then, the symmetrical current limitation band ($\pm I_{MAX}$) is employed. By sensing the output voltage V_o, the optimal switching frequency is determined based on the state-trajectory calculation. As the output voltage increases, the current limitation band decreases gradually to the full-load steady state I_{peakN}. There is no current stress during the start-up, and V_o is built up smoothly and quickly.

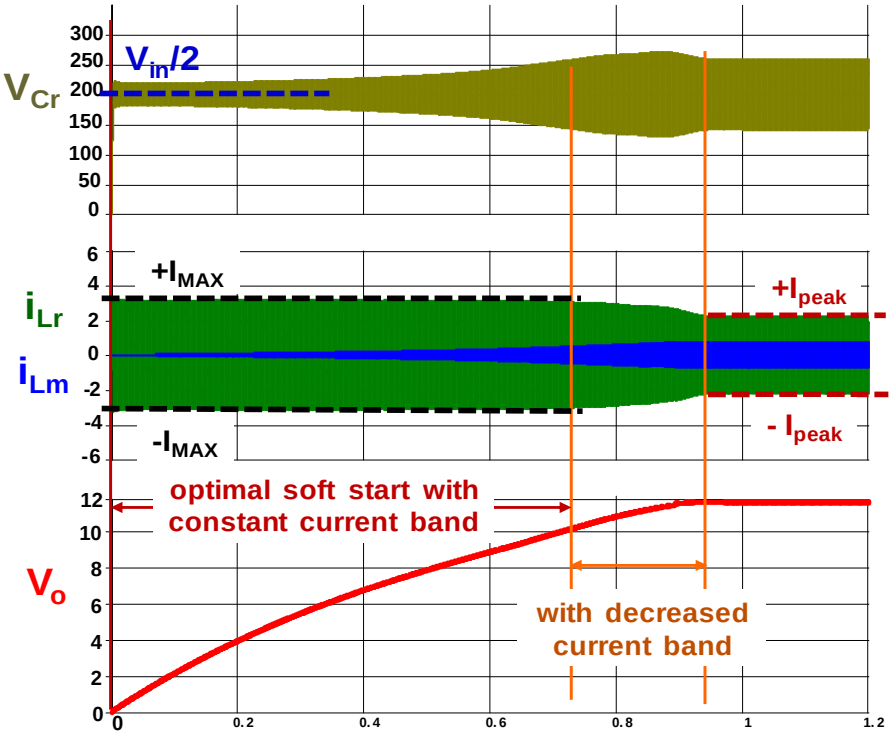


Fig. 4.25 Whole process of the optimal soft start-up

When it comes to the full-bridge LLC resonant topology, at the start up moment, there are two operation stages as shown in Fig. 4.26. It is different from the half-bridge LLC, since there is no $V_{in}/2$ dc bias on the resonant capacitor in the full-bridge topology. At the start-up moment, the

trajectory centers are at point (1, 0) and (-1, 0) respectively. Under the full-load steady state, the trajectory center locates at (0, 0) as shown in Fig. 4.27. Similarly, the current band is set, and then the optimal frequency control is employed to limit the resonant current into the band.

To settle the initial condition, the one-cycle control is presented. Different from the half-bridge LLC, the resonant current has no over-shoot as compared with Fig. 4.17, since the initial point (0, 0) is insider the steady state trajectory.

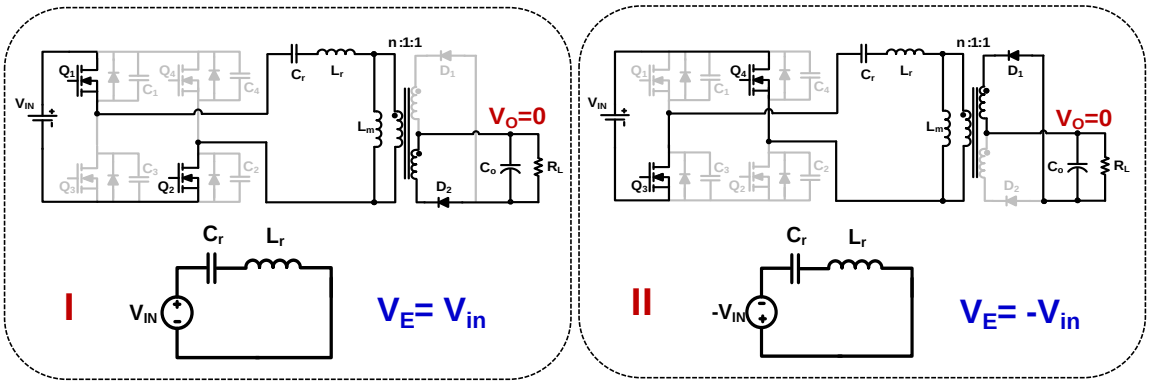


Fig. 4.26 Equivalent circuit of full-bridge LLC at start-up moment

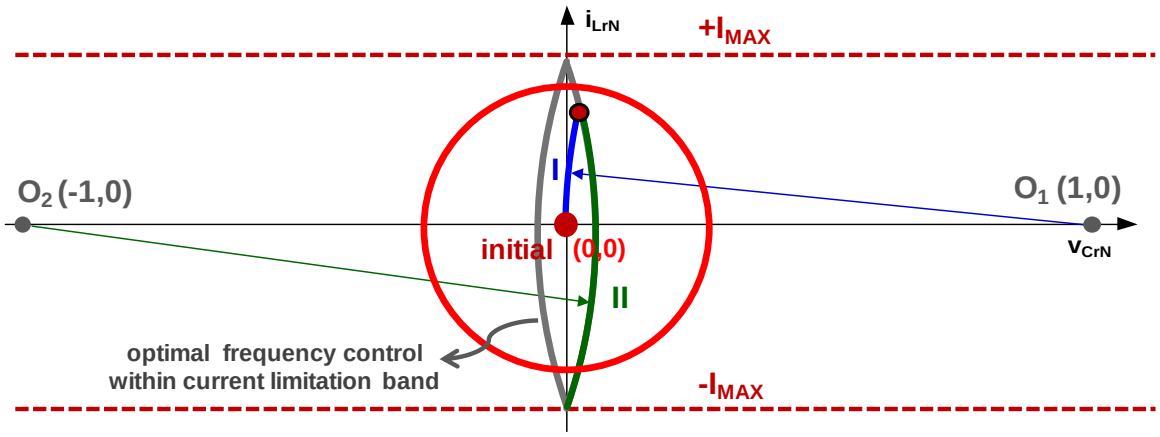


Fig. 4.27 Initial state-trajectory with one-cycle control for full-bridge LLC

The pulse widths of the first switching cycle could be determined based on the state-plane drawing. Fig. 4.28 shows the corresponding time-domain simulation: the first switching cycle is tuned to settle the resonant capacitor initial condition, and then the optimal switching frequency is determined within the symmetrical current limitation band.

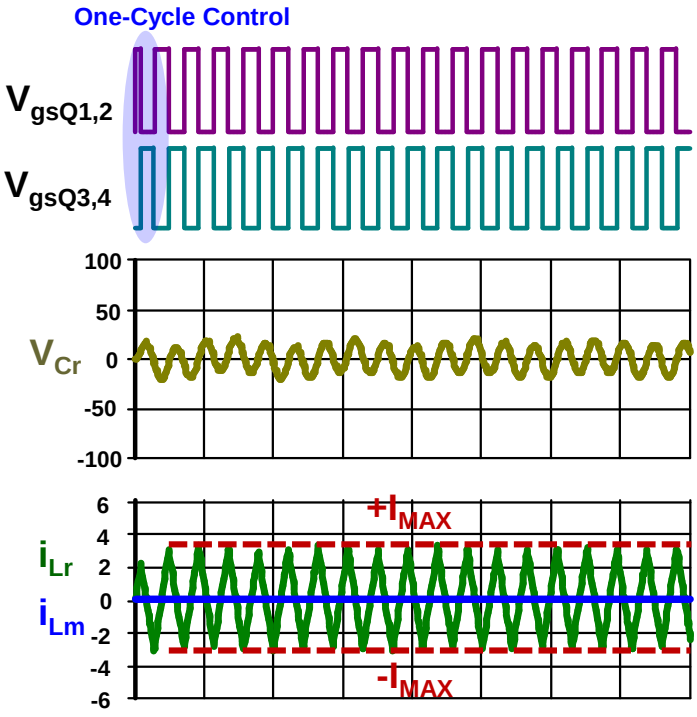


Fig. 4.28 Simulation of one-cycle control for full-bridge LLC

4.4 Over-Load Protection with Optimal Control

The short through is the worst over-load condition. When shoot-through happens, the output capacitor voltage will discharge to zero in a short period of time as shown in Fig. 4.29.

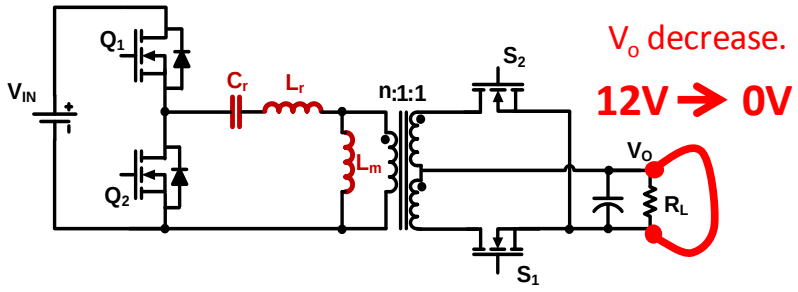


Fig. 4.29 Shoot-though of LLC resonant converter

Different from the LLC soft start-up process where the output voltage V_o is built up to the steady-state value from zero, under the over-load condition, V_o will quickly decrease from the steady-state value. It is a reverse process of soft start-up. When over-load happens, from the state plane, the center of steady state circle will split. If limiting the resonant current i_{Lr} to the same band, the optimal switching frequency can be determined as the soft start-up process. As a result, the energy in the resonant tank can be limited.

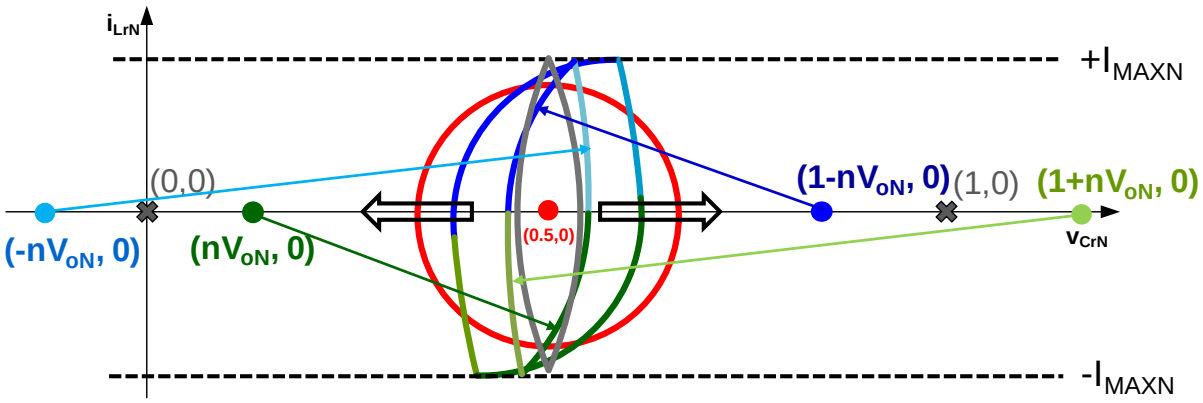


Fig. 4.30 State-trajectory of over-load protection with current limitation band

Fig. 4.31 and 4.32 show the simulated time-domain waveforms and corresponding state trajectory with optimal protection. The output voltage decreases as the shoot-through happens.

The switching frequency responses quickly based on the state-plane calculation to limit the trajectory loci to the current band.

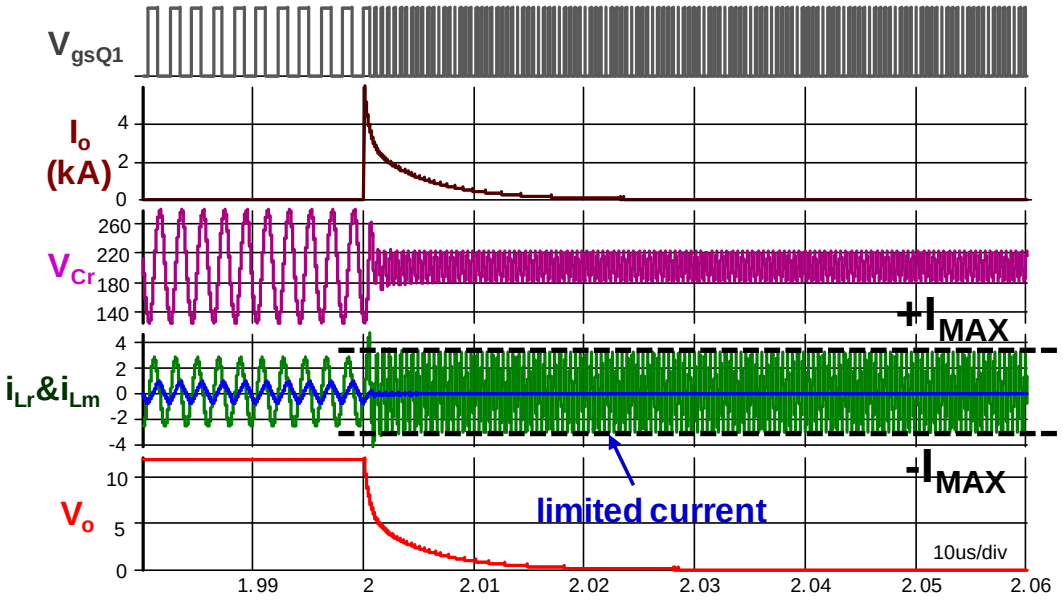


Fig. 4.31 Simulated time-domain response of shoot-through protection

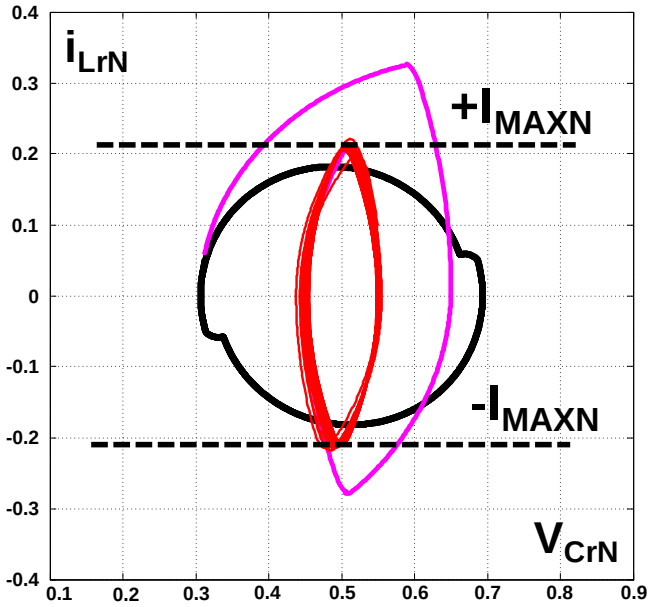


Fig. 4.32 State-trajectory of shoot-through protection

4.5 Experimental Results

To have a comparison, an industry evaluation board of a 300W 400V/12V half-bridge LLC resonant converter [A.39] is tested as shown in Figs. 4.33 and 4.34. The main converter parameters are the same with Table 3.1 in Chapter 3. Since the initial switching frequency (f_{ss_ini}) is not high enough, there is large current and voltage stress at the start-up moment as shown in Fig. 4.33. During the start-up process, f_s is not well controlled, so the energy transporting to the output is not optimized. As shown in Fig. 4.34, at the beginning, the output voltage V_o increases fast, and then it slows down. The whole soft start process approaching to the full-load steady state takes about 23ms.

Figure 4.35 shows the experimental trajectory when mapping the normalized time-domain resonant current i_{LrN} and voltage V_{CrN} to the state plane. Compared with the full-load steady state, the current and voltage stress is much higher.

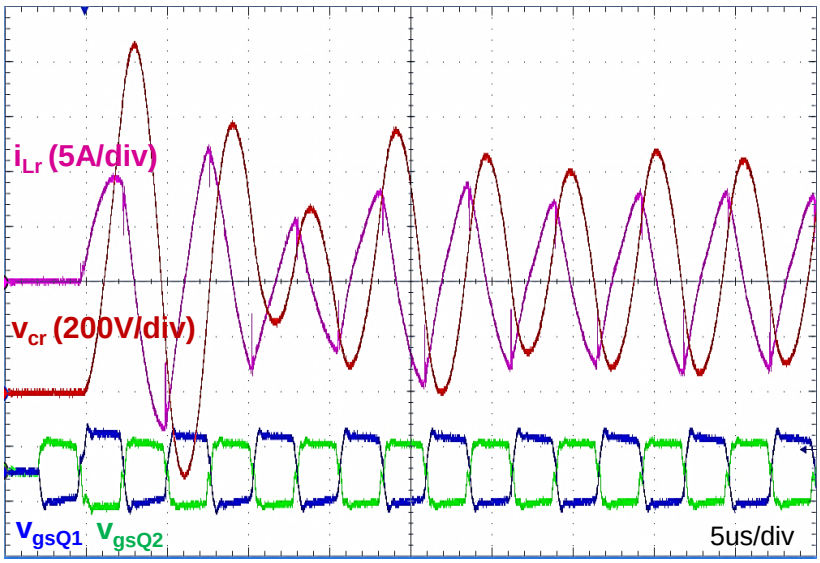


Fig. 4.33 Large voltage and current stresses at the start-up moment

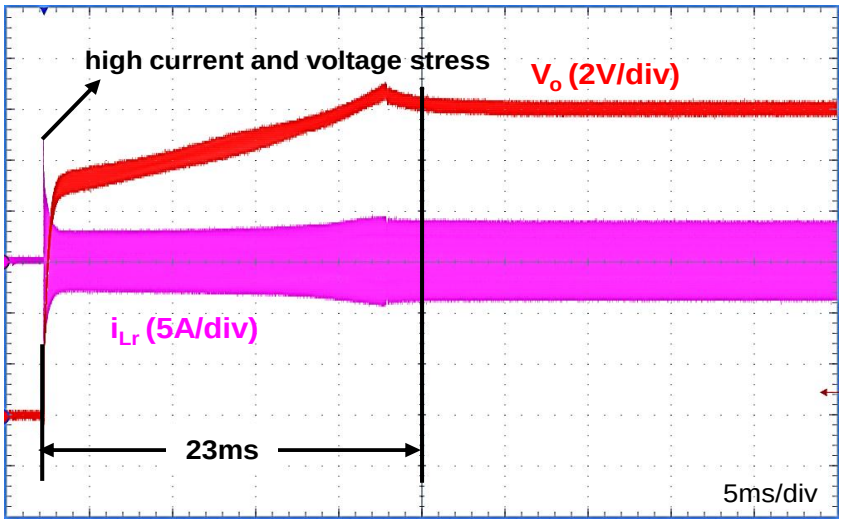


Fig. 4.34 Initial soft start-up process with a commercial controller

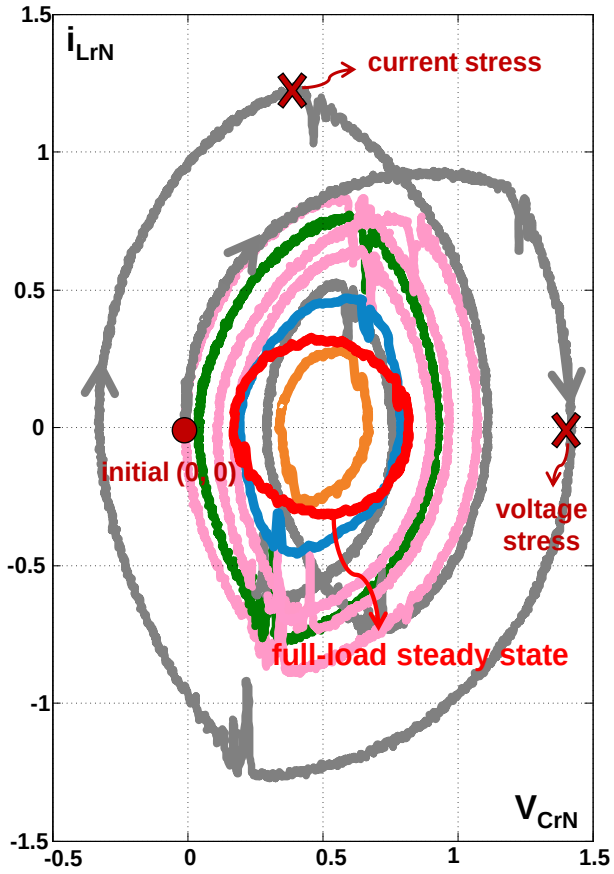


Fig. 4.35 Soft start-up experimental trajectory with a commercial controller

The optimal soft start-up is realized by a digital controller which is built in a Cyclone III FPGA.

With the unsymmetrical band as described in Section 4.2, when the LLC starts up, the optimal pulse widths of Q_1 and Q_2 driving signals are estimated. Therefore, the resonant capacitor reaches to $V_{in}/2$ quickly without any spike as shown in Fig. 4.36.

After that, the LLC starts up from $2.3f_0$ by (4.11). As the start-up continues, the output voltage increases, and the optimal switching frequency is determined by (4.19). By applying these optimal switching frequencies, the experimental time-domain waveform is shown in Fig. 4.37. The resonant current i_{Lr} is well controlled to the current limitation band ($\pm I_{Max}$) as designed, and the output voltage increases much more smoothly and quickly when compared with the performance of a commercial controller.

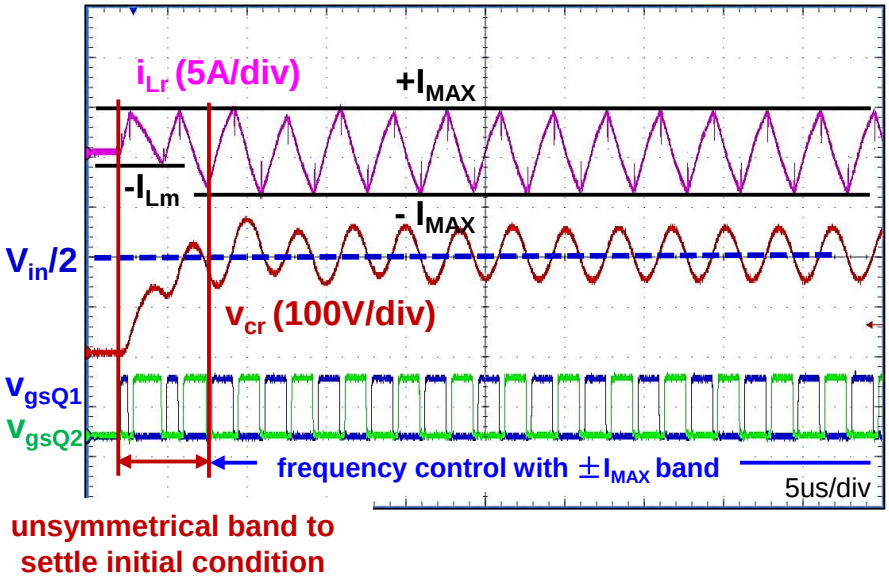


Fig. 4.36 Initial condition settling with unsymmetrical current band

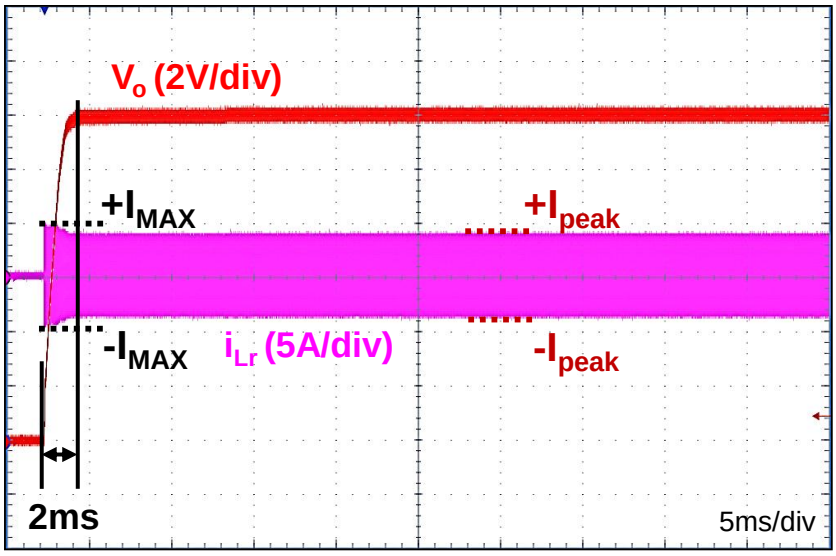


Fig. 4.37 Proposed optimal soft start-up

Figure 4.38 shows the corresponding experimental trajectory. During the soft start-up, the resonant current is well controlled to the band. Compared with Fig. 4.35, there is no current and voltage stress.

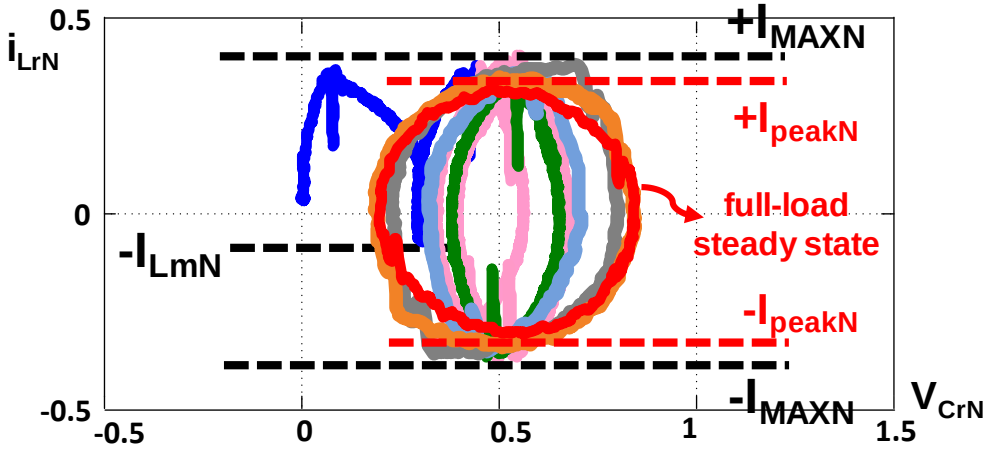


Fig. 4.38 Experimental trajectory of the optimal soft start-up

4.6 Conclusion

An optimal soft start-up process for the LLC resonant converter is proposed based on the graphical state-trajectory analysis. To settle the initial condition, the unsymmetrical-band approach, slop-band control, and one-cycle control are investigated. Then, by sensing the output voltage, the optimal frequency is determined within a current limitation band. Therefore, no current and voltage stress in the resonant tank is guaranteed during the soft start-up. Meanwhile, the output voltage is built up quickly and smoothly. By applying the optimal soft start-up algorithm reversely, the resonant current and voltage stress can be limited under the over-load protection.

Chapter 5. Efficiency Improvement I: Optimal Burst Mode for Light-Load Efficiency

In this chapter, a novel burst mode control for the LLC resonant converter is proposed to improve the light load efficiency. Based on the state-plane trajectory analysis, during the burst on-time, a three pulse switching pattern is implemented. The first pulse width is optimized to settle to the steady state of the highest efficiency load condition in the minimal time. And the next two pulse operation follows the steady-state trajectory of this highest efficiency load. Thus, the best burst efficiency can be achieved. When it comes to the LED PWM dimming application, a similar optimal switching pattern is employed. Thus, the full-load steady state is tracked in one-pulse time. The overall efficiency has been improved in the whole dimming range. Moreover, under lower dimming conditions, the LED intensity can be controlled more precisely.

5.1 Introduction

Today, with the explosive increase of consumer electronics and IT equipment, the efficiency requirement of power conversion circuits is becoming higher and higher. Moreover, the efficiency demand is not only focused on the heavy load but also on the light load. The ever increasing efficiency requirements defined by 80Plus [A.13], Energy Star [A.14], Climate Savers Computing [A.15], and European Code of Conduct, pose a major design challenge.

The LLC resonant converter is becoming more and more popular for its high efficiency, because of both zero-voltage-switching (ZVS) for primary side switches and zero-current-

switching (ZCS) for secondary side rectifiers. However, the light load efficiency still cannot meet the increasingly strict requirements, since certain load-independent losses such as driving losses possess a much higher ratio under the light load condition.

Variable frequency control methods have been widely used to improve the light load efficiency in PWM converters, e.g. PWM/PFM control [C.1] [C.2], constant and adaptive on time control [C.3], and burst mode control [C.4] [C.5]. The idea is to decrease the switching frequency or equivalent switching frequency, to reduce these load independent losses. To the LLC resonant converter, the burst mode control has been used to improve the light load efficiency, by periodically blocking the switch gate driving signals V_{gsQ1} and V_{gsQ2} as shown in Fig. 5.1.

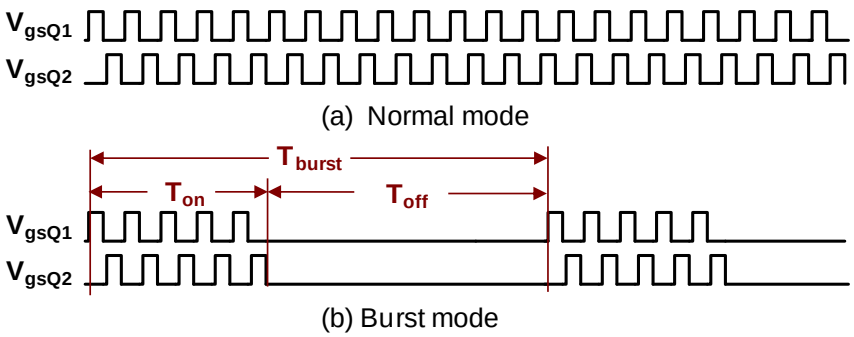


Fig. 5.1 Normal operation mode vs. burst mode

In the hysteresis burst mode [A.38-A.44] [C.5], the switches are periodically on and off, determined by the comparison between the feedback control command (f_{FB}) and the hysteresis band. When the load decreases, f_{FB} increases, that is, the LLC switching frequency (f_s) increases to regulate the output voltage. Until f_{FB} hits the hysteresis band ceiling, the LLC enters the burst mode, and the switches stop working. Then f_{FB} will decrease correspondingly. When it hits the band bottom, the switches start to work again. Although the implementation is simple, using f_{FB}

to determine the light load condition is not accurate. Since it is influenced by the input voltage V_{in} and resonant tank parameters such as resonant inductor L_r, magnetizing inductor L_m, and resonant capacitor C_r. With different V_{in} and tank parameters, the light load conditions triggering the burst mode are different. Moreover, the design of the hysteresis band is critical. Large band induces a large output voltage ripple, and small band leads to low burst efficiency.

[C.6] [C.7] proposed the burst mode for the best light-load efficiency. Fig. 5.2 shows the typical efficiency curve of a LLC resonant converter. The best efficiency is achieved at I_{OPT} load point. When it comes to the light load I_{light}, if the burst duty D_{burst} is determined as

$$D_{burst} = \frac{T_{on}}{T_{burst}} = \frac{I_{light}}{I_{OPT}}, \tag{5.1}$$

where T_{on} is the burst-on time, T_{burst} the burst period as shown in Fig. 5.1, the LLC will treat the equivalent load as I_{OPT} during the burst-on time. Thus, the best efficiency can be achieved under the light load conditions.

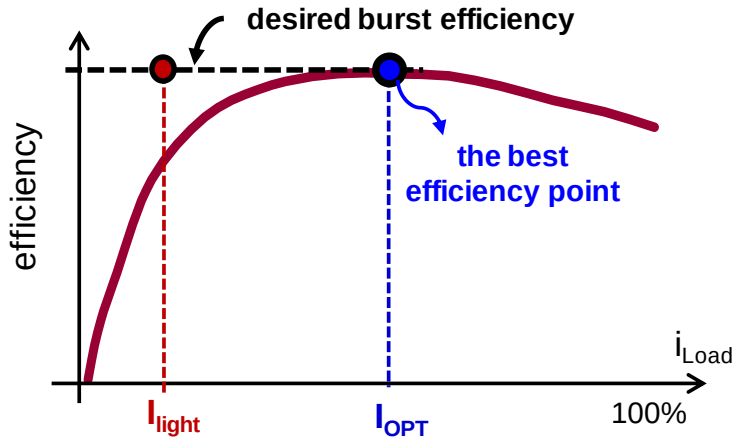


Fig. 5.2 Desired burst efficiency

However, it is not easy to fix to the optimal load (I_{OPT}) steady state during the burst on-time to achieve best efficiency. As illustrated in Fig. 5.3, there will be oscillated current in the resonant tank.

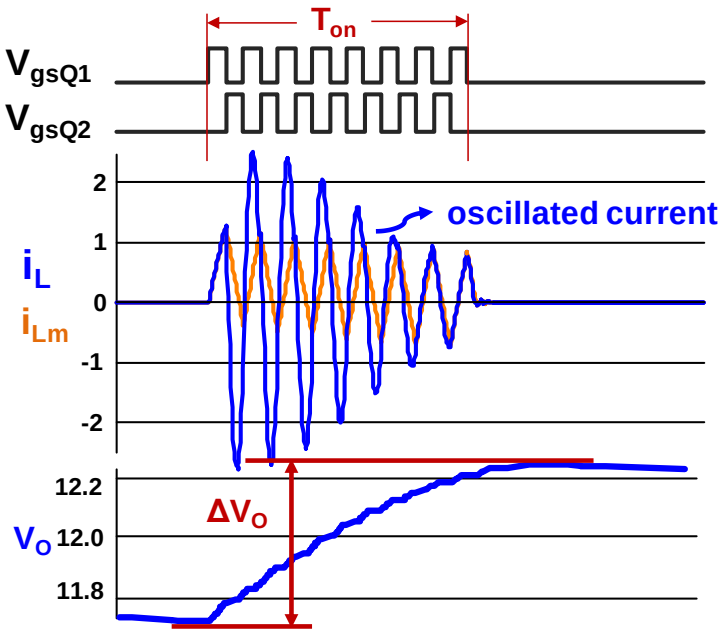


Fig. 5.3 Oscillated resonant current during the burst on-time

Different from the normal operation, the output voltage V_o is regulated to be constant, in the burst mode, V_o has a low frequency ripple as shown in Fig. 5.3. During the burst on-time, switches Q_1 and Q_2 conduct alternatively to charge the output capacitor, thus the output voltage is increased by ΔV_o. When Q_1 conducts as Mode I, the source voltage across the resonant tank will change to V_{in}-nV_o-nΔV_o; and when Q_2 conducts as Mode IV, the source voltage across the resonant tank will change to nV_o+nΔV_o. Therefore, in the state plane, during the burst on-time as shown in Fig. 5.4, center O_1 at Mode I will move to left, from (0.5, 0) to (0.5-nΔV_{oN}, 0); and O_2 at Mode IV will move to right, from (0.5, 0) to (0.5+nΔV_{oN}, 0). As a result, the circle radius ρ

will decrease step by step, which means that the instantaneous energy of the resonant tank will shrink step by step. From the time-domain waveforms, as V_o increases, and resonant current i_{Lr} will decrease step by step as shown in Fig. 5.3, equivalently from the heavy load to the light load, never fixing at the I_{OPT} steady state as desired. This dynamic oscillation increases I_{RMS} value, and then reduces the burst efficiency.

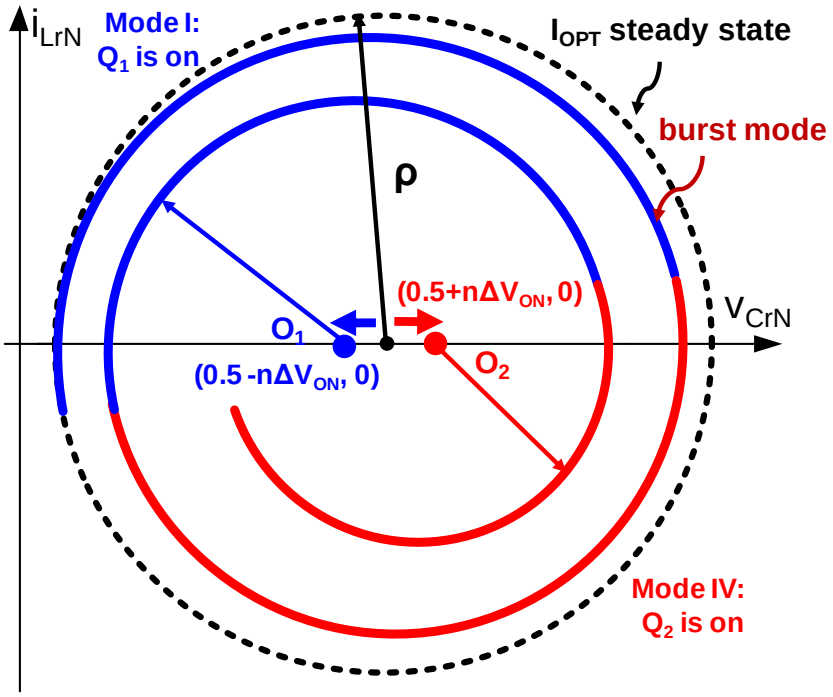


Fig. 5.4 Oscillated circles during the burst on-time

Therefore, an optimal burst mode is needed to keep the LLC always operating at the best efficiency point during the burst on-time. From the state-trajectory analysis, the output voltage variation firstly should be minimized to avoid the oscillation.

5.2 Burst Mode with Optimal Switching Pattern

5.2.1 Minimal optimal three-pulse switching pattern

In order to avoid this shrinking current, the output voltage variation ΔV_o should be minimized. From the state plane point of view, two circle centers O_1 and O_2 should be kept as closed as possible. Thus, the burst trajectory will locate in the vicinity of I_{OPT} steady state, to ensure high efficiency.

One effective way to minimize ΔV_o is reducing the burst on-time. Fig. 5.5 shows the minimal burst on-time solution with the optimal three pulse pattern. The first pulse is fine tuned to settle to the steady state of the highest efficiency load I_{OPT} within one pulse time. And the next two switching pulses operate near the resonant frequency point ($f_s=f_0$) to follow the i_{OPT} steady-state trajectory. Therefore, the high efficiency could be achieved.

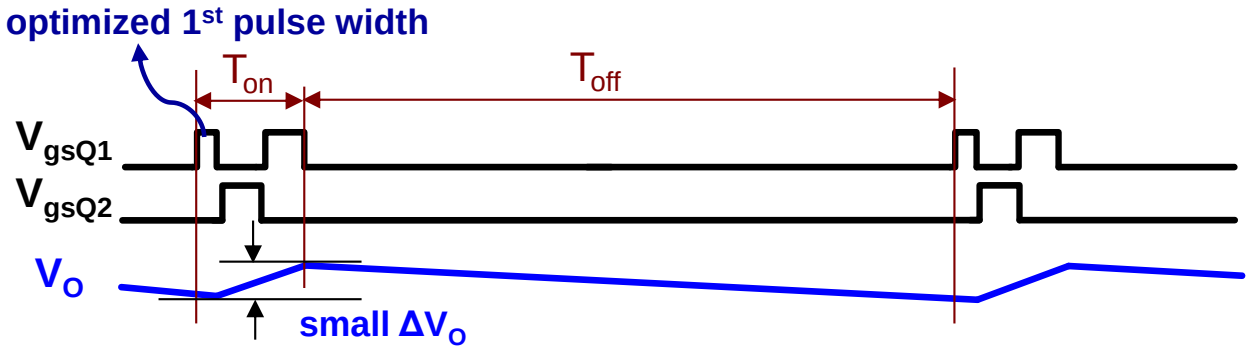


Fig. 5.5 Optimal three-pulse switching pattern during the minimal burst on-time

The simulated waveform of the optimized three pulse pattern is shown in Fig. 5.6. When Q_1 is turned off at t_3 moment, the capacitor voltage v_{Cr} is resonant to a high value. During the burst-off time, both Q_1 and Q_2 are off and the circuit is lossless, so v_{Cr} stays constant. Then Q_1 is

turned on again at time t_0, and the voltage across the transformer primary side is approximately equal to V_{in}-v_{Cr}, which is smaller than nV_o. Thus, from t_0 to t_1, the secondary side doesn't conduct, and L_m, L_r and C_r form the series resonant tank as Mode III described in Chapter 2. Fig. 5.7 state-plane trajectory shows that from time t_0 to t_1, it goes through ellipse trajectory at Mode III.

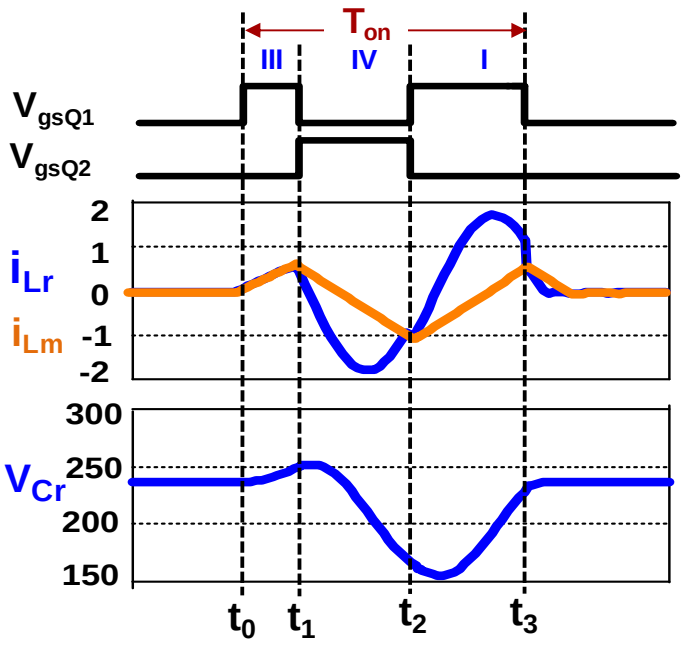


Fig. 5.6 Simulated minimal burst-on time with optimal pulse pattern

As shown in Fig. 5.7, at t_1 moment when the ellipse locus touches the I_{OPT} steady state trajectory, Q_1 is turned off immediately. And then Q_2 and Q_1 are turned on at the resonant frequency as Mode IV and Mode I. It follows the I_{OPT} steady-state circle. Since only with one full resonant period during the burst on-time, ΔV_o is minimized. The circle centers O_1 and O_2 almost locate at (0.5, 0), thus the I_{OPT} steady-state could be tracked well, ensuring high light load efficiency.

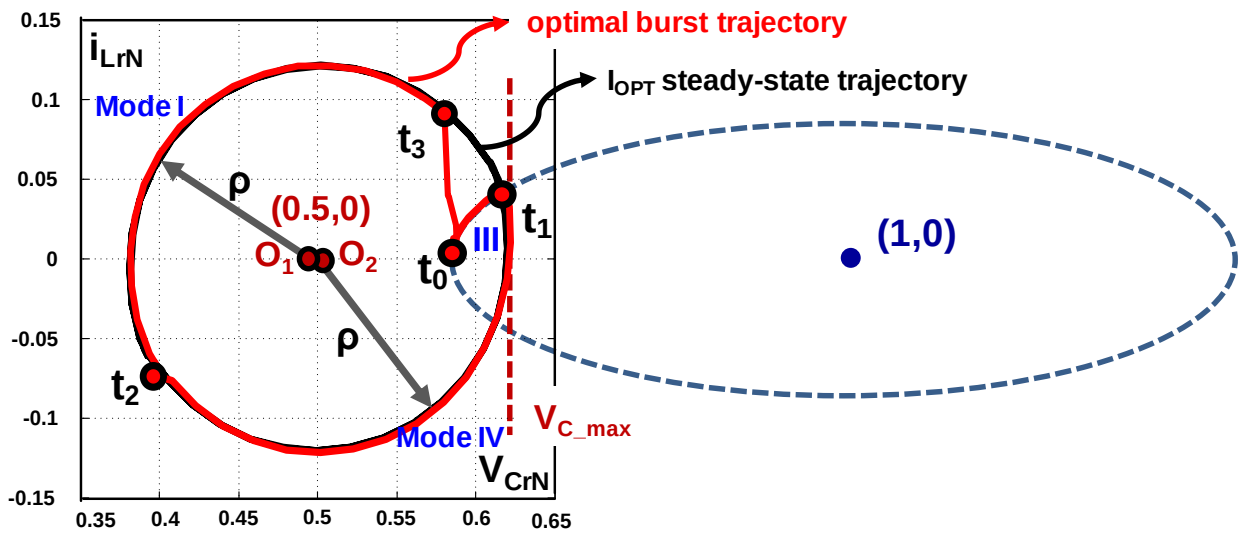


Fig. 5.7 State plane trajectory of the optimal burst pattern

Based on Fig. 5.7 state plane, the first pulse width from t_0 to t_1 could be estimated. By tuning the first pulse width, the next two pulses will track the I_{OPT} steady state trajectory. Thus, when the burst on-time ends at the t_3 moment, the resonant capacitor voltage $v_{Cr}(t_3)$ is the same as Q_1 is turned off under the I_{OPT} steady state in the normal operation. Thus, the normalized resonant capacitor voltage at t_3 moment can be calculated from (3.5):

$$v_{CrN}(t_3) = \frac{\pi}{2} \cdot \frac{I_{OPT}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5. \tag{5.2}$$

After de-normalization with the voltage factor V_{in},

$$v_{Cr}(t_3) = \frac{\pi}{2} \cdot \frac{I_{OPT}}{n} \cdot Z_0 + \frac{V_{in}}{2}, \tag{5.3}$$

where the highest efficiency load condition I_{OPT} could be determined by the experiment test or the loss analysis.

During the burst-off time, because Q_1 and Q_2 both are off and the circuit is lossless, the resonant capacitor voltage v_{Cr} stays constant. Then Q_1 is turned on again in the next burst cycle, the resonant capacitor voltage at t_0 moment is same with $v_{Cr}(t_3)$, that is,

$$v_{Cr}(t_0) = v_{Cr}(t_3). \tag{5.4}$$

Besides, at time t_0, the resonant inductor current i_{Lr} is zero as shown in Fig. 5.6:

$$i_{Lr}(t_0) = 0. \tag{5.5}$$

From t_0 to t_1, it follows the ellipse trajectory as Mode III. And t_1 is the connection point of the ellipse and the circle of the highest efficiency load I_{OPT}. From Fig. 5.7, at t_1 moment, the resonant capacitor voltage $v_{Cr}(t_1)$ can be approximated to be the maximum capacitor voltage, which could be derived from (3.1) and (3.2):

$$\begin{aligned} v_{Cr}(t_1) = v_{Cr\_MAX@i_{OPT}} &= (\rho + 0.5)\cdot V_{in} = \sqrt{2} I_{RMS}\cdot Z_0 + \frac{V_{in}}{2} \\ &= \frac{Z_0}{4}\sqrt{\frac{n^2 V_o{}^2 T^2}{L_m{}^2} + 4\pi^2 \cdot \left(\frac{I_{\mathrm{OPT}}}{n}\right)^2} + \frac{V_{in}}{2}. \end{aligned} \tag{5.6}$$

Now knowing the initial conditions at t_0 as (5.3) (5.4) (5.5), final status at t_1 (5.6), and the equivalent resonance of Mode III (2.13), the first switching pulse width ($\Delta T = t_1 - t_0$) can be solved as

$$\Delta T = \frac{\cos^{-1}\left(\left(v_{Cr}(t_1) - V_{in}\right) \Big/ \left(v_{Cr}(t_0) - V_{in}\right)\right)}{\omega_1}. \tag{5.7}$$

Furthermore, the resonant capacitor voltage v_{Cr} could be sensed as shown in Fig. 5.8, and then compared with $V_{Cr\_MAX@iOPT}$. Q_1 could be turned off when v_{Cr} hits the steady state trajectory of the highest efficiency load.

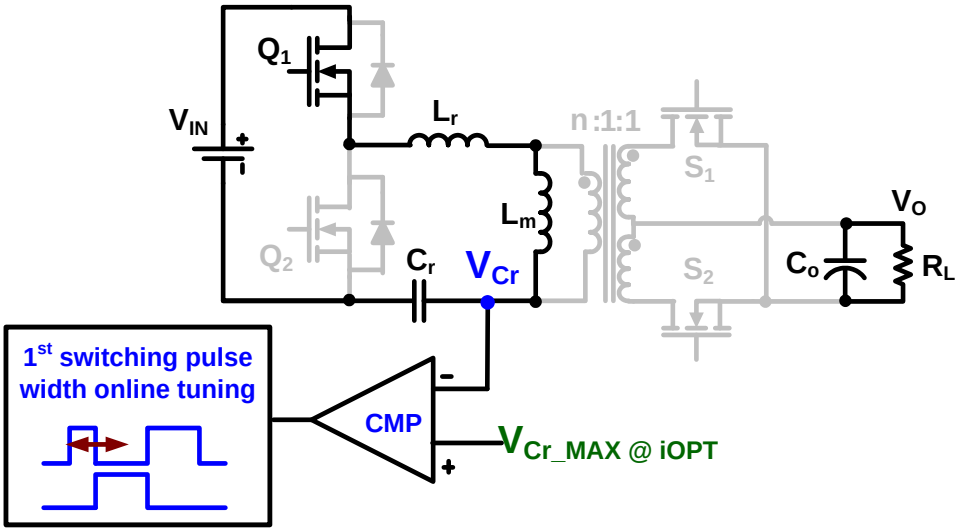


Fig. 5.8 Real-time tuning of the first pulse width by sensing v_{Cr}

To maintain this optimal three pulse pattern during the minimal burst-on time, when the load changes, the burst on-time T_{on} keeps constant, but the burst off-time T_{off} is modulated. As shown in Fig. 5.9, when the load increases, the T_{on} with the optimal three pulse pattern keeps constant, but T_{off} becomes smaller. Therefore, the high efficiency can be ensured. Moreover, the output voltage variation ΔV_o is always minimally maintained, and no additional low-pass filter is needed.

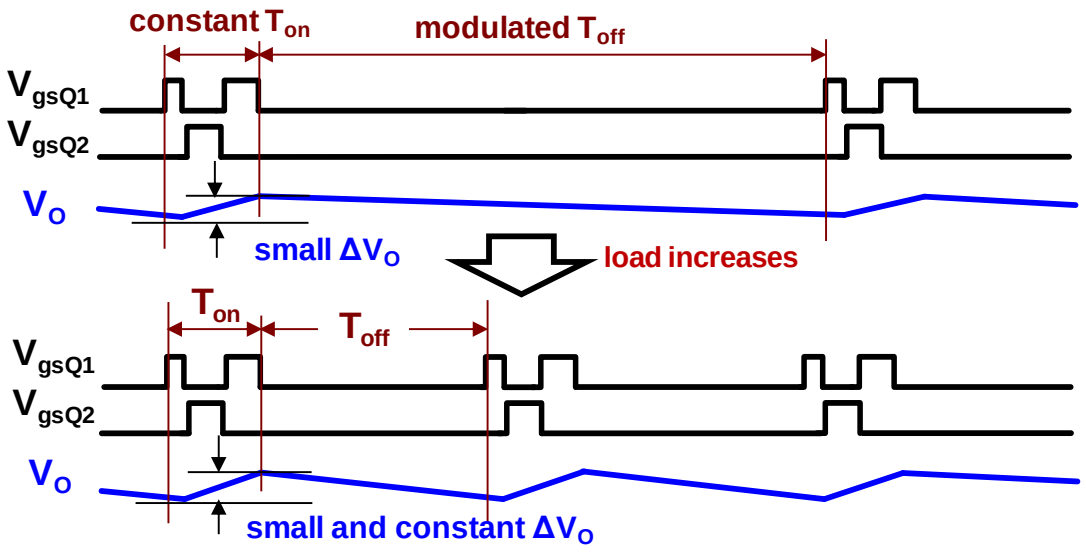


Fig. 5.9 Constant burst on-time implementation when the load changes

5.2.2 First pulse partial ZVS

With the proposed burst mode, by tracking the optimal trajectory, ZVS of second and third switching action is achieved. In order to further improve the efficiency, ZVS of first switching action is investigated.

During the off-time, both Q_1 and Q_2 are off, so switch junction capacitors C_{OSS1} and C_{OSS2} participate in the resonance with L_m and L_r as shown in Fig. 5.10. And the remaining resonant energy will be damped by the loop parasitic resistor R_p. With the constant burst on time implementation, if the load increases, the off time will be modulated to be small. As a result, the resonant current i_{Lr} hasn't been damped to zero yet within the short off time. From Fig. 5.11, when i_{Lr} passes through zero from negative to positive, the middle node voltage V_{dsQ2} just reaches the highest point. Thus, a zero crossing detector (ZCD) circuit is added to sense i_{Lr} zero crossing points. When the burst on time starts, trigger Q_1 turns on at the moment when i_{Lr} goes

through zero from negative to positive. Therefore, a partial ZVS of Q_1 is achieved to reduce first hard switching turn on loss.

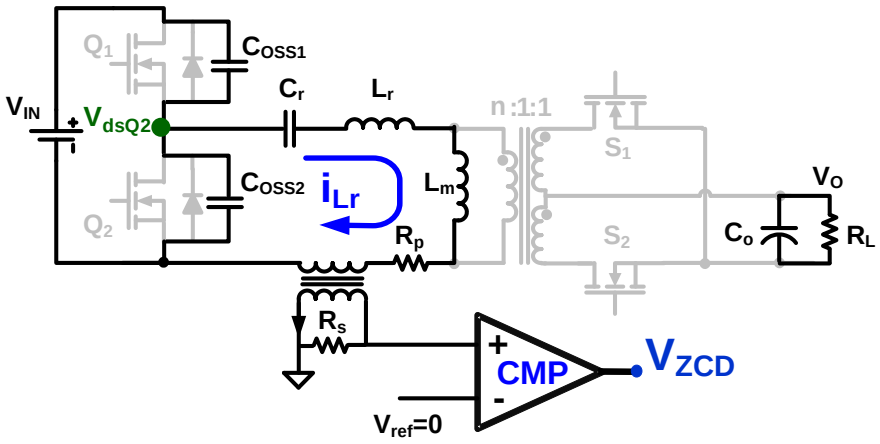


Fig. 5.10 ZCD implementation for the first switch partial ZVS

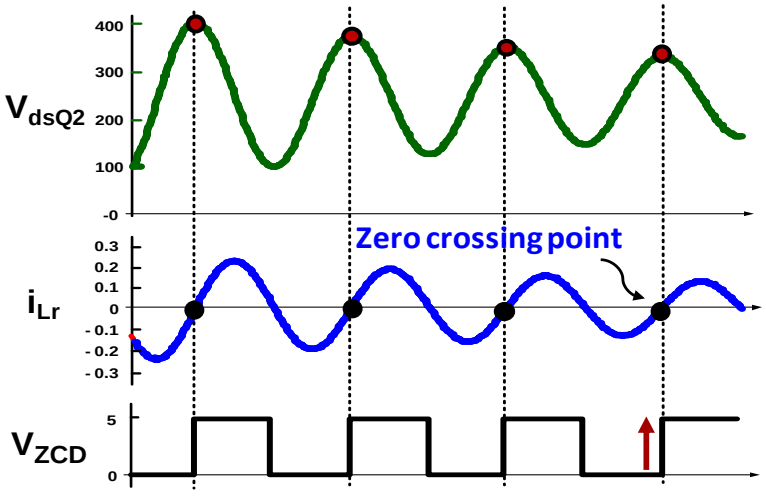


Fig. 5.11 Partial ZVS realization

5.2.3 Constant burst on-time implementation

Fig. 5.12 shows the simplified control scheme of the proposed burst mode under light load conditions. As shown in Fig. 5.13, like the conventional constant on-time voltage mode, the

output voltage ripple is sensed. During the burst-off time, the LLC stops operating, and V_o will decrease. When it touches the control reference V_{ref}, the burst on-time is triggered, during which the optimized three pulse switching pattern is applied to track the steady state trajectory of the highest efficiency load (I_{OPT}). The first switching pulse width could be determined by (5.7) or real-time tuned by sensing resonant capacitor voltage v_{Cr}. The next two pulses operate at $f_s=f_0$, following the desired I_{OPT} steady-state trajectory, to ensure high efficiency.

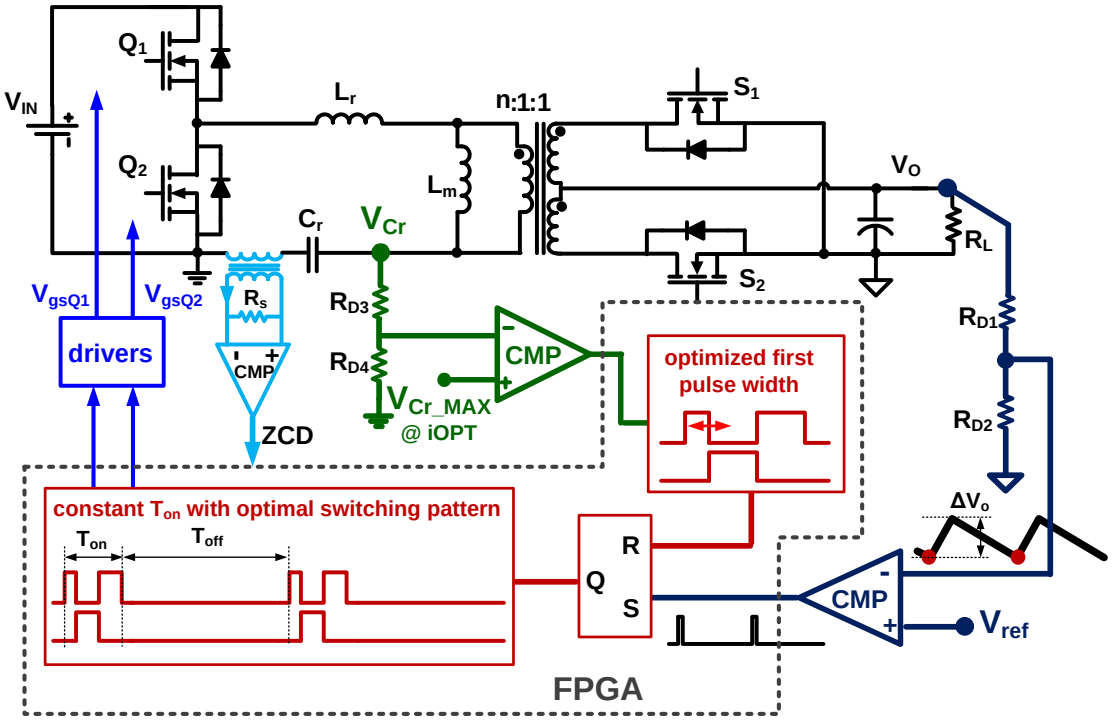


Fig 5.12 Simple control blocks of the optimal burst mode

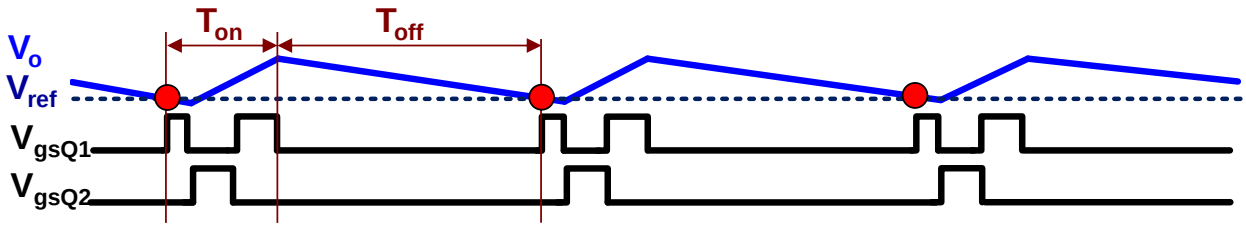


Fig. 5.13 Constant burst on-time implementation based on the output voltage ripple

As shown in Fig. 5.12, no high resolution Analog-to-Digital-Converter (ADC) is needed. Only two comparators are employed. One determines the burst-on time instant, and the other one determines the first pulse width, which could also be pre-calculated in (5.7).

5.2.4 Experimental results

The experiment is carried out on a 300W 400V/12V half bridge LLC resonant converter prototype. The hardware prototype is shown in Fig. 5.14. The main converter parameters are shown in Table 5.1. The proposed burst mode control is built in a Cyclone III FPGA using Verilog HDL.

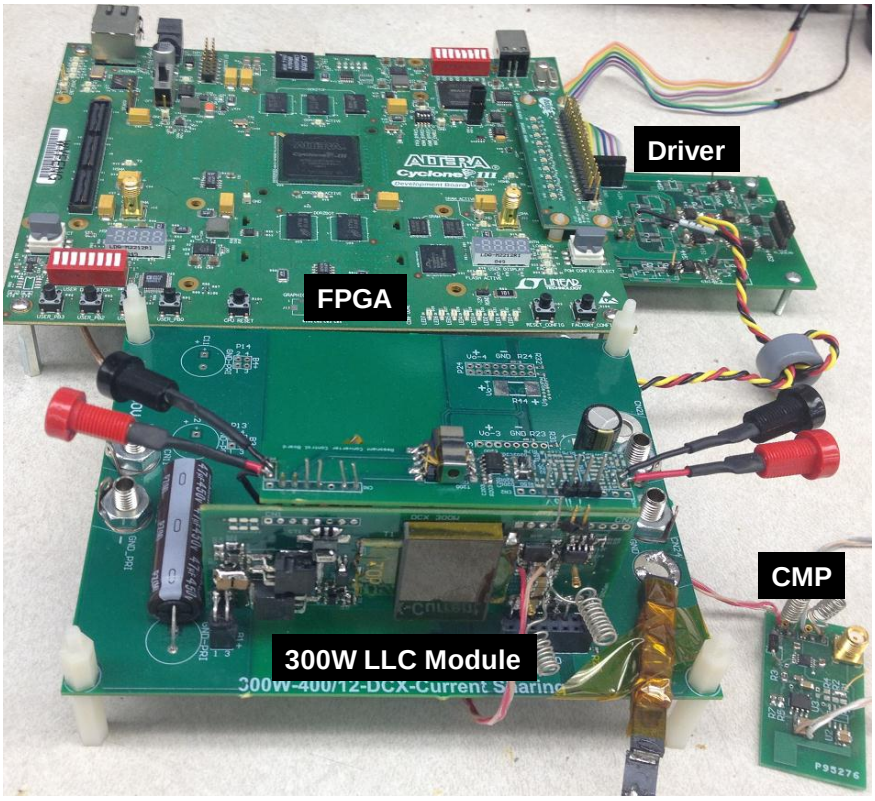


Fig. 5.14 Hardware prototype

Table 5.1 The parameters of LLC resonant prototype

Designed parameters	**Parameters Value**
Resonant capacitor	10nF
Resonant inductor	5.6 μH
Transformer leakage inductor	2.1 μH
Transformer magnetizing inductor	100 μH
Transformer turns ratio	17:1:1
Primary side main switch	2 ×STB11NM60ND
Secondary side SR	2 ×BSC017N04NS
Output capacitor	440 μF

The highest efficiency load is experimentally measured near the 14A load region (full load is 25A). Fig. 5.15 shows the steady state waveform under 14A load condition (I_{OPT}=14A).

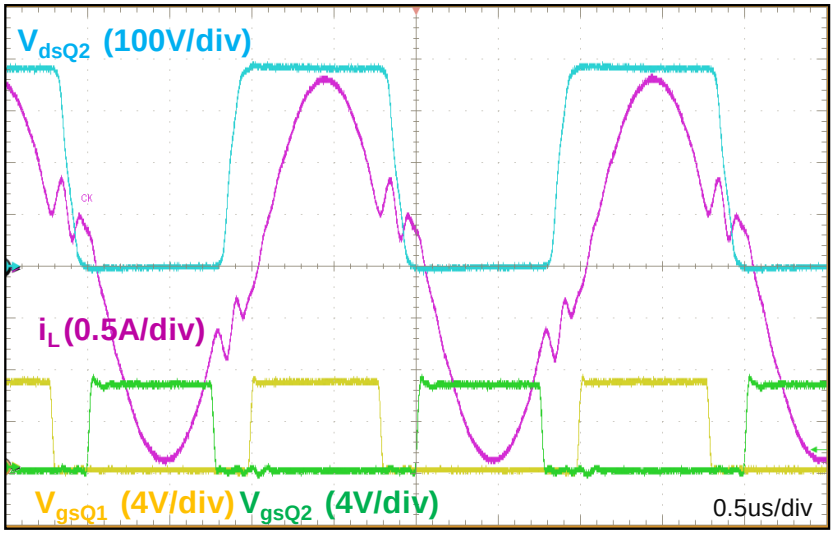


Fig. 5.15 Steady state waveform of the highest efficiency load (i_{OPT}=14A)

If implementing the burst mode proposed in [C.6], when the light load is 2A, the burst duty D_{burst} as in (5.1) is:

$$D_{burst} = \frac{T_{on}}{T_{burst}} = \frac{i_{Load}}{i_{OPT}} = \frac{2A}{14A} = \frac{1}{7} \tag{5.8}$$

If the burst period T_{burst} is set to be 100us (i.e. f_{burst}=10kHz), the burst on-time T_{on} is 14us. Thus, during T_{on}, there will be a lot of switching pulses as shown in Fig. 5.16. As analyzed in Section 5.1, the larger T_{on} with a lot of switching cycles will increase the output voltage variation ΔV_o, producing the shrink current in the resonant tank. As a result, it cannot fix to the I_{OPT} steady state as desired.

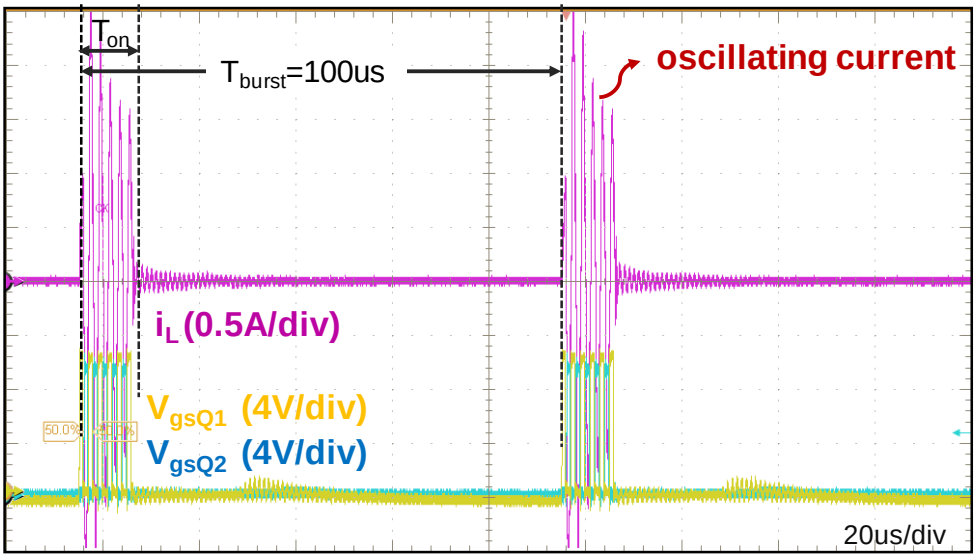


Fig. 5.16 Shrinking current within large burst on-time

If employing the proposed burst mode with the minimal burst-on time, the first pulse width is calculated as in (5.7) with the parameters provided in Table 5.1:

$$\Delta T \approx \frac{T_0}{4}, \tag{5.9}$$

which is about quarter resonant period. It also can be real-time tuned by comparing the resonant capacitor voltage v_c with the maximum resonant capacitor voltage under 14A load condition $V_{Cr\_MAX@14A}$.

Fig. 5.17 shows the burst mode with the optimal three pulse pattern when the load is 2A. During the burst on-time T_{on}, the first switching pulse is tuned to settle to 14A steady state in one-pulse time. Then the LLC equivalently operates under the I_{OPT} steady state within the T_{on} duration.

If the first switching pulse is not optimized, as shown in Fig. 5.18, the I_{OPT} steady state cannot be tracked. As a result, there will be more RMS current in the resonant tank, which produces more conduction losses.

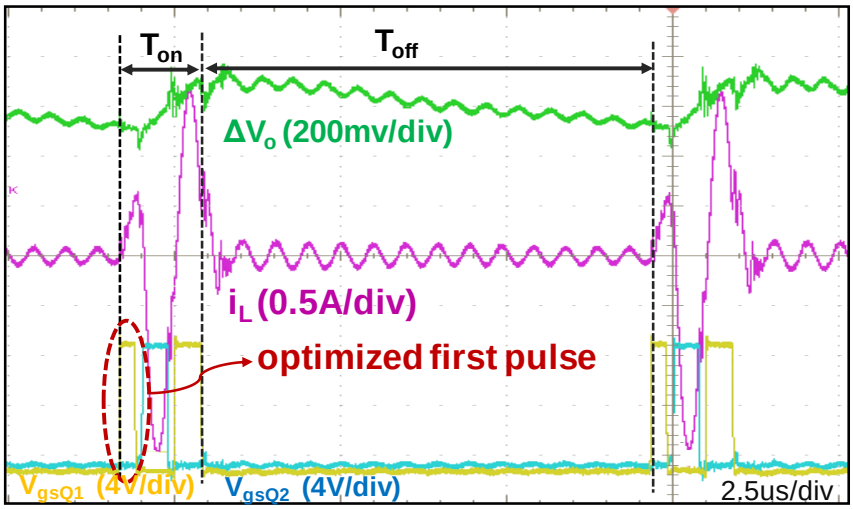


Fig. 5.17 Optimal burst mode under the light load of 2A

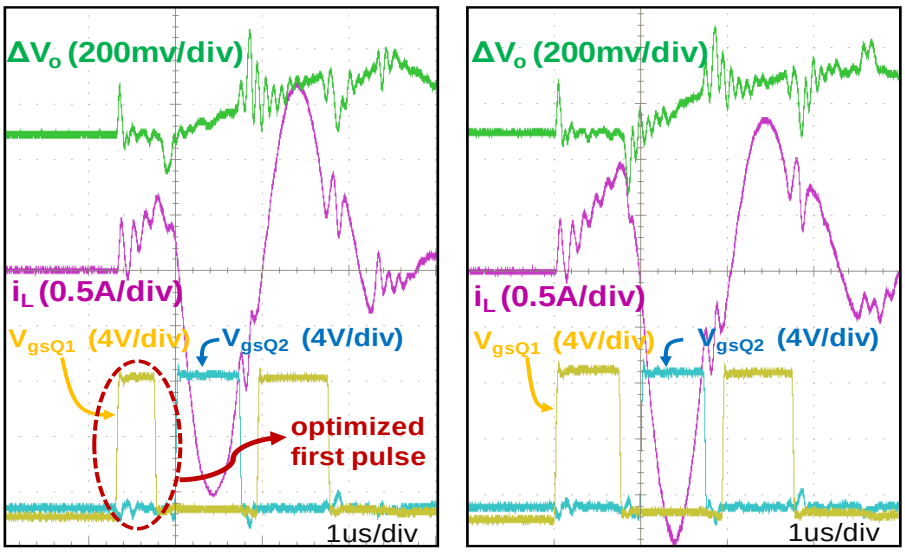


Fig. 5.18 Comparison between with and without 1st pulse width optimization

Fig. 5.19 shows that when the load increases to 4A, T_{on} with optimized three pulse pattern stays constant, but the burst off-time T_{off} decreases.

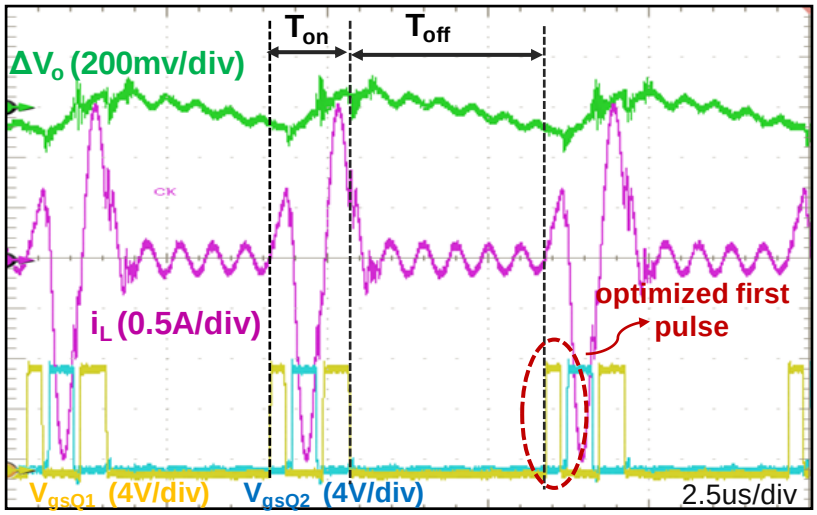


Fig. 5.19 Optimal burst mode under the light load of 4A

Fig. 5.20 shows that when the load decreases to 1A, T_{on} with optimized three pulse pattern still keeps the same, but the burst off-time T_{off} increases.

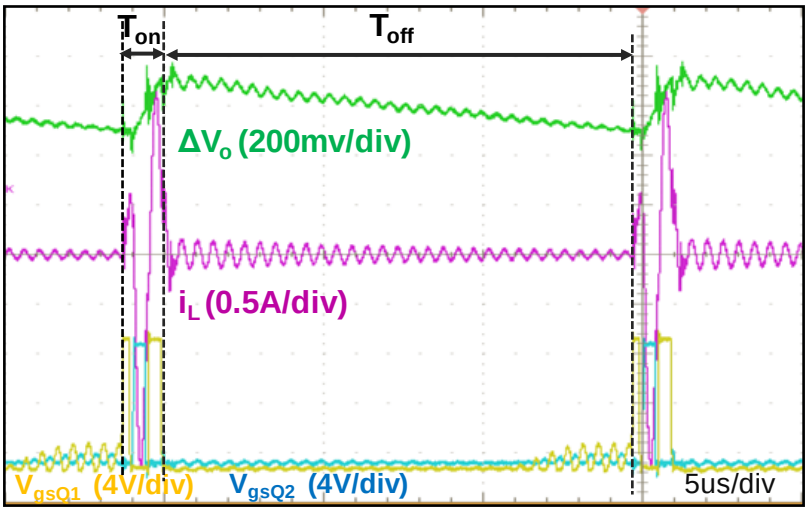


Fig. 5.20 Optimal burst mode under the light load of 1A

Due to the benefit of the minimal and constant burst on-time implementation, the output voltage ripple ΔV_o is always minimized as shown in Figs. 5.17, 5.19 and 5.20, thus no additional low-pass filter is needed. With the optimal three pulse pattern, during the burst on-time, under all light load conditions, the LLC equivalently operates at I_{OPT} steady state. As a result, high efficiency can be accomplished.

As shown in Fig. 5.21, when burst off-time is short and i_{Lr} hasn't been damped to zero yet, with ZCD implementation, the first switch is turned on as the resonant current crosses zero, realizing the partial ZVS.

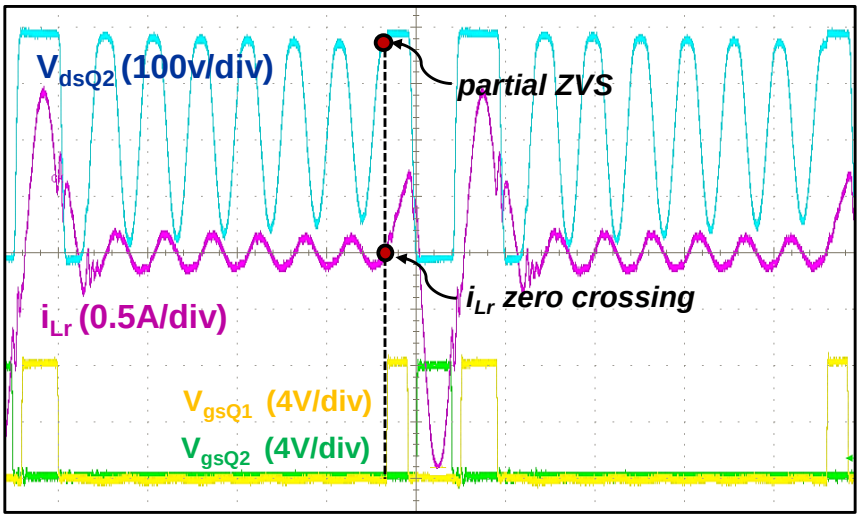


Fig. 5.21 Partial ZVS of the first switching action

Fig. 5.22 shows the experimental efficiency comparison. The LLC resonant converter can achieve a high efficiency within the middle and heavy load regions. But the light load efficiency is lower. By employing the optimal three pulse switching pattern, the highest efficiency can be achieved. Even under 0.4% full load (1.2W), the efficiency is still higher than 92% (The efficiency is tested without considering the FPGA losses, since the final target is the IC integration, whose power consuming is much less than the FPGA).

Based on the experimental measurement, when the load is lighter than 25% full load, the burst mode efficiency starts to become higher than the normal operation mode. Thus the optimized burst approach is employed as the load becomes lighter than 25% full load.

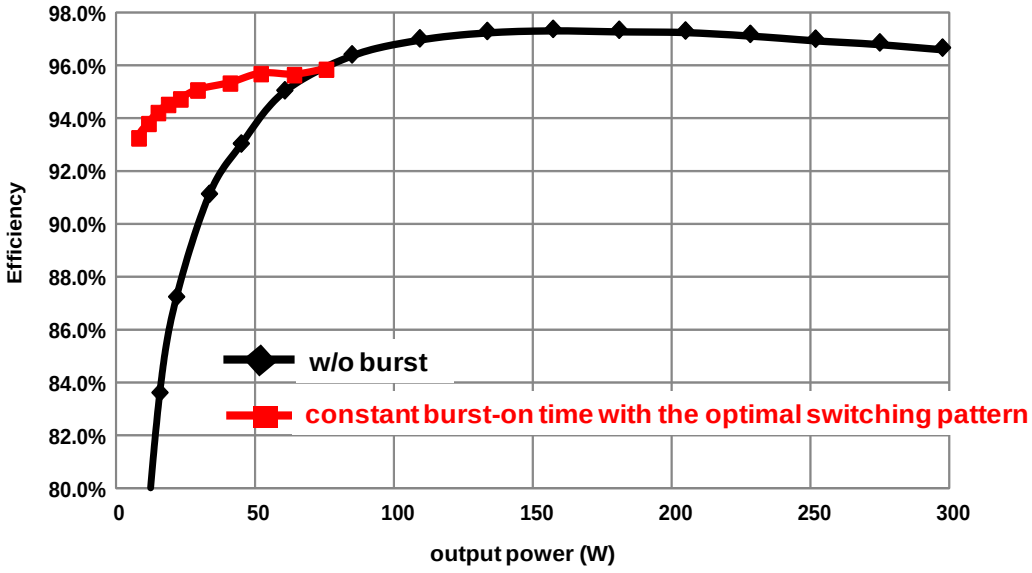


Fig. 5.22 Efficiency improvement with the proposed burst mode control

5.3 Optimal Switching Patterns for LED PWM Dimming

5.3.1 Introduction of PWM dimming for LLC LED driver

As a promising lighting source, LED have been widely used, because of high efficiency, eco-friendliness, long lifetime, good color rendering properties, etc [D.1-D.4]. In many applications, for example, display backlighting, indoor lighting and street lighting, the multi-channel LED structure is chosen from the cost-effective, reliability and safety concerns.

A single stage multi-channel constant current (MC^3) LLC resonant LED driver is proposed in [A.19]. As shown in Fig. 5.23, the multiple transformer structure (primary windings are in series and secondary windings are in parallel) enables the cross-regulation by only controlling one LED channel [A.19]. With the voltage-doubler-rectifier configuration, each transformer can drive two LED strings at the same time, and hence reduces the transformer number by half. The

DC block capacitor (C_{dc}) is used to achieve precise current sharing between two neighboring LED channels.

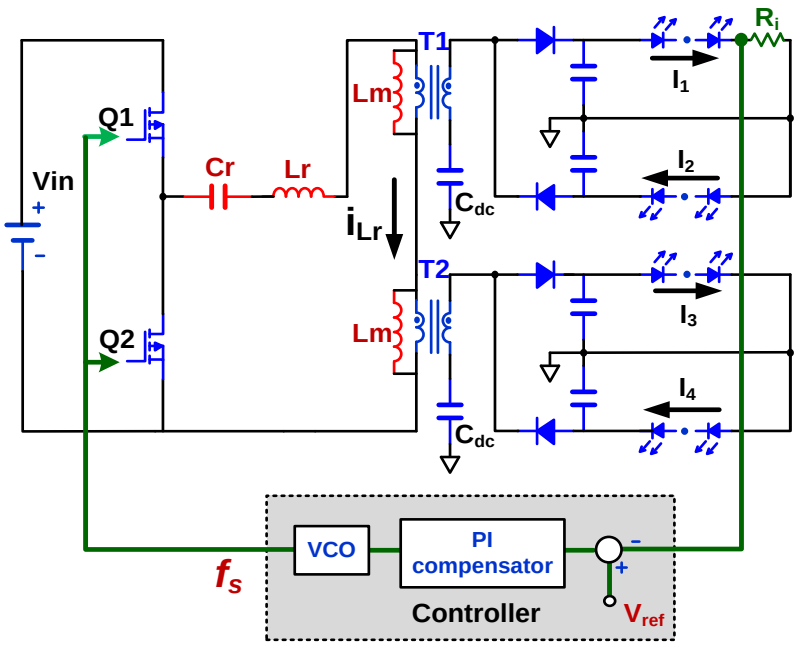


Fig. 5.23 Single stage MC^3 LLC resonant LED driver

Like the conventional LLC resonant converter, the switching frequency (f_s) is controlled to achieve different dimming ratios. Normally, under the full-load condition, the MC^3 LLC resonant converter is designed to operate near the resonant frequency point ($f_s=f_0$) to achieve the best efficiency. When the switching frequency f_s increases, the LED dimming ratio becomes low, that is, it comes to the light load condition. However, as shown in Fig. 5.24, the current gain becomes flat as f_s increases. Even push f_s to as high as $10f_0$, only 15% full load dimming is achieved. Meanwhile, the efficiency as shown in Fig. 5.25 drops quickly as the dimming ratio decreases, since the switching loss and driving loss increases dramatically.

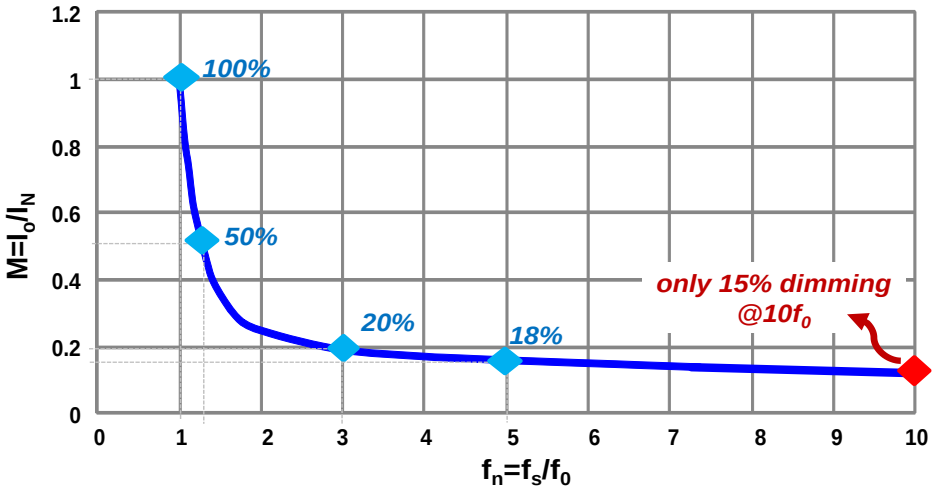


Fig. 5.24 DC characteristics with f_s controlled analog dimming

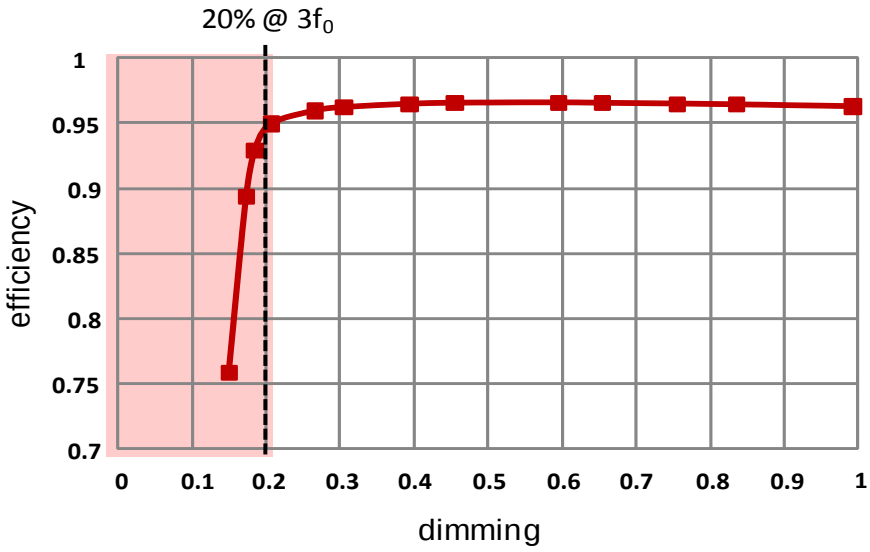


Fig. 5.25 Efficiency of f_s controlled analog dimming

Compared with the switching frequency controlled analog dimming, the PWM dimming approach can achieve much lower dimming ratio by reducing the PWM duty cycle. Moreover, the converter always operates under the full-load condition during the PWM dimming on-time,

thus the overall efficiency will be higher. In addition, there is no chromaticity shift when using the PWM dimming [D.5].

The control scheme for the LED PWM dimming is shown in Fig. 5.26. The PWM dimming frequency is set to be 200Hz, so the discontinue PWM signal is not visible to the human eyes. $V_{S1,2,3,4}$ are same with the PWM dimming signal.

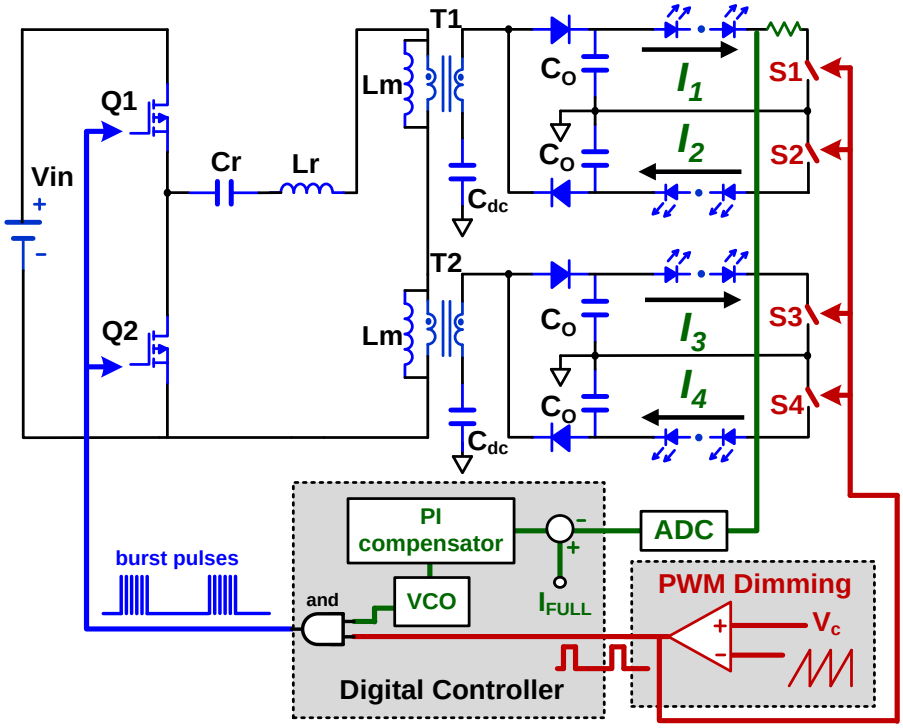


Fig. 5.26 MC^3 LLC resonant LED driver with PWM dimming control

As shown in Fig. 5.27, when the PWM dimming signal is on, the MC^3 LLC resonant converter is regulated to provide the constant full-load current (I_{Full}) to the LED strings. When the PWM dimming signal is off, the MC^3 LLC stops working, and the LED lights become off as well. Therefore, by controlling the PWM duty cycle, the LED intensity can be controlled to get the needed dimming ratio:

$$I_{1,2,3,4} = I_{Full} \cdot D. \tag{5.10}$$

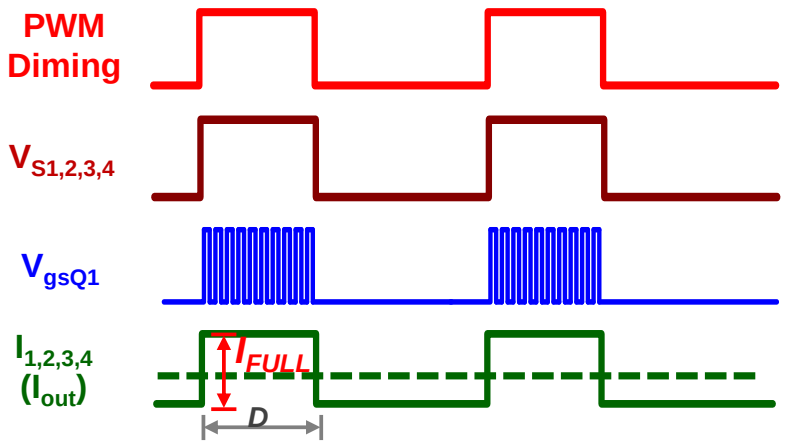


Fig. 5.27 LED PWM dimming

5.3.2 Dynamic oscillation with conventional PWM dimming

However, due to the fast dynamic characteristic of the LLC resonant tank, there will be serious oscillations when switching between the working status and the idle status. Fig. 5.28 shows the simulation waveforms during the PWM dimming on-time. In this switching pattern, the up-switch Q_1 is first turned on and last turned off, in order to reduce the first switching turn-on loss at the moment when the LLC starts to work [C.6]. Since when Q_1 is last turned off, the resonant capacitor voltage would be charged to a high value $v_{Cr}(t_n)$. During the PWM dimming off-time, v_{Cr} stays constant (i.e. $v_{Cr}(t_0)=v_{Cr}(t_n)$). Then Q_1 is firstly turned on again, the drain to source voltage of Q_1 is approximately equal to V_{in}-$v_{Cr}(t_0)$, which is relatively small. Thus, the first hard switching turn-on loss is minimized.

However, as shown in Fig. 5.28, there are dynamic oscillations when the MC^3 LLC LED driver starts to work from the idle status. As a result, the large RMS value of the resonant current

(i_{Lr}) will make additional conduction loss. Moreover, the oscillation on the output current will reduce the control accuracy of the LED intensity.

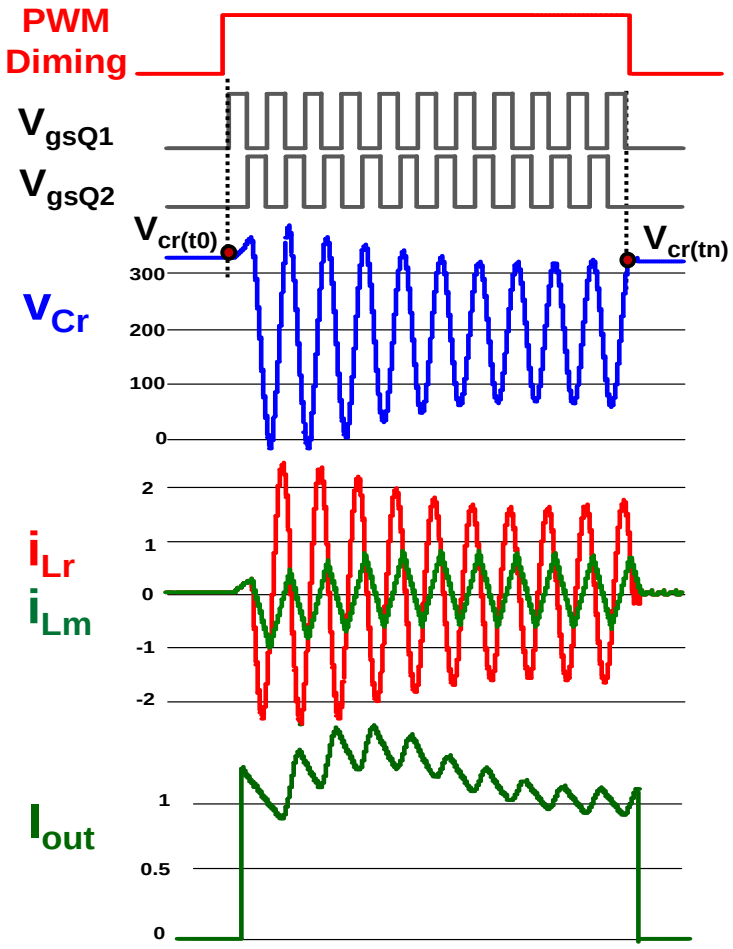


Fig. 5.28 Dynamic oscillation when MC^3 LLC starts to work

To analyze this dynamic oscillation, the time-domain v_{Cr} and i_{Lr} shown in Fig. 5.28 are mapped to the state plane in Fig. 5.29. The red circle represents the full-load steady-state trajectory. When Q_1 is firstly turned on, the secondary side will not conduct [C.6]. As a result, the magnetizing inductor (L_m) will be in the resonance, which represents the Mode III. It is a partial ellipse trajectory on the state plane, as shown in Fig. 5.29 with green color. This first-

pulse ellipse trajectory will cross the desired full-load steady state; then results in serious dynamic oscillation by pulling the larger circles to the smaller steady-state red circle.

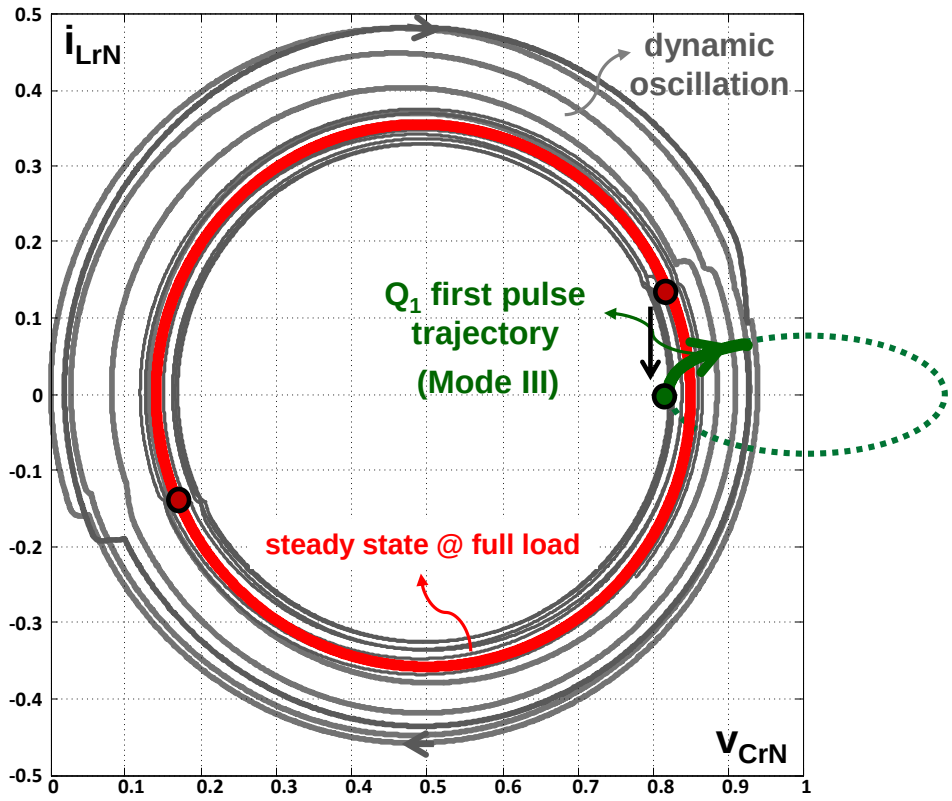


Fig. 5.29 State-trajectory of the dynamic oscillation

5.3.3 First-pulse tuning optimal PWM dimming

To reduce the dynamic oscillation, the first-pulse-tuning optimal switching pattern is proposed, that is, during the PWM dimming on-time, the first-pulse width of Q_1 gate driving signal is tuned to just hit the full-load steady circle rather than crossing it. Fig. 5.30 and Fig. 5.31 show the simulated time-domain waveform and corresponding state-trajectory with the optimal switching pattern. By tuning the first-pulse width, the state variables (v_{Cr} and i_{Lr}) will track to the full-load steady state within the minimum time. There is almost no dynamic oscillation inside the

LLC resonant tank. The lower RMS current will improve the overall efficiency. Moreover, the output current is tuned to be flat, thus the LED intensity can be controlled perfectly.

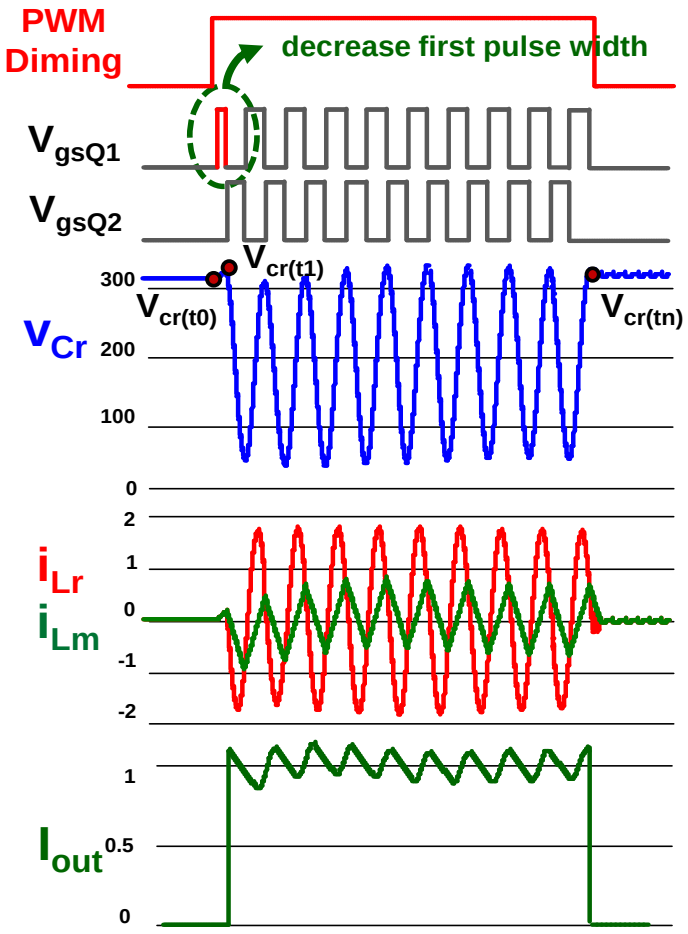


Fig. 5.30 Time-domain waveforms of the first-pulse-tuning optimal switching pattern

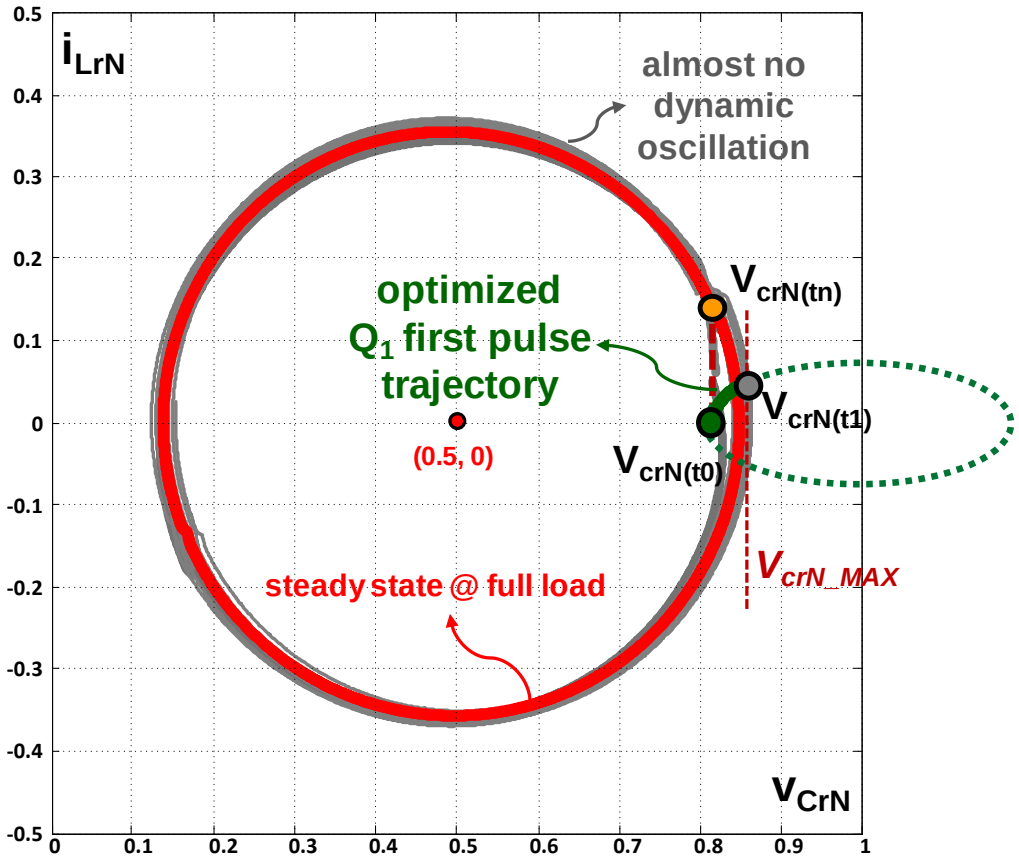


Fig. 5.31 State-trajectory of the first-pulse-tuning optimal switching pattern

The Q_1 first-pulse width from time t_0 to t_1 can be estimated. By tuning the first-pulse width, the full-load steady-state will be tracked quickly. Thus, when the PWM dimming on-time ends, the resonant capacitor voltage $v_{Cr}(t_n)$ is equal to the full-load steady-state value when Q_1 is turned off, that is,

$$v_{CrN}(t_n) = \pi \cdot \frac{I_{full}}{n} \cdot \frac{1}{V_{in}/Z_0} + 0.5. \tag{5.11}$$

During the PWM dimming off-time, because both Q_1 and Q_2 are off and the circuit is lossless, the resonant capacitor voltage v_{Cr} stays constant. Then, Q_1 is firstly turned on again in

the next PWM dimming cycle, the resonant capacitor voltage at t_0 moment is the same with $v_{Cr}(t_n)$:

$$v_{CrN}(t_0) = v_{CrN}(t_n). \tag{5.12}$$

From t_0 to t_1, it follows the ellipse trajectory of Mode III. And t_1 is the connection point of the ellipse and the circle of the full-load steady state. From Fig. 5.31, at t_1 moment, the resonant capacitor voltage $v_{CrN}(t_1)$ can be approximated to be the maximum value, that is,

$$v_{CrN}(t_1) = v_{CrN\_MAX@Ifull} = \rho + 0.5, \tag{5.13}$$

which could be derived from (3.2):

If the resonant current i_{Lr} is normalized with V_{in}/Z_1, where $Z_1 = \sqrt{(L_r + L_m)/C_r}$, the ellipse trajectory of Mode III will change to a circle with center (1, 0) in the new state plane as shown in Fig. 5.32.

Thus, the conduction angle α on the state plane is

$$\alpha = \cos^{-1}\left(\frac{1 - v_{CrN}(t_1)}{1 - v_{CrN}(t_0)}\right). \tag{5.14}$$

Converting the state-plane angle α to the time-domain conduction time:

$$T_{12} = t_1 - t_0 = \frac{\alpha}{\omega_1} = \alpha \cdot \sqrt{(L_r + L_m)C_r}, \tag{5.15}$$

where ω_1 is the resonant frequency of L_m+L_r with C_r.

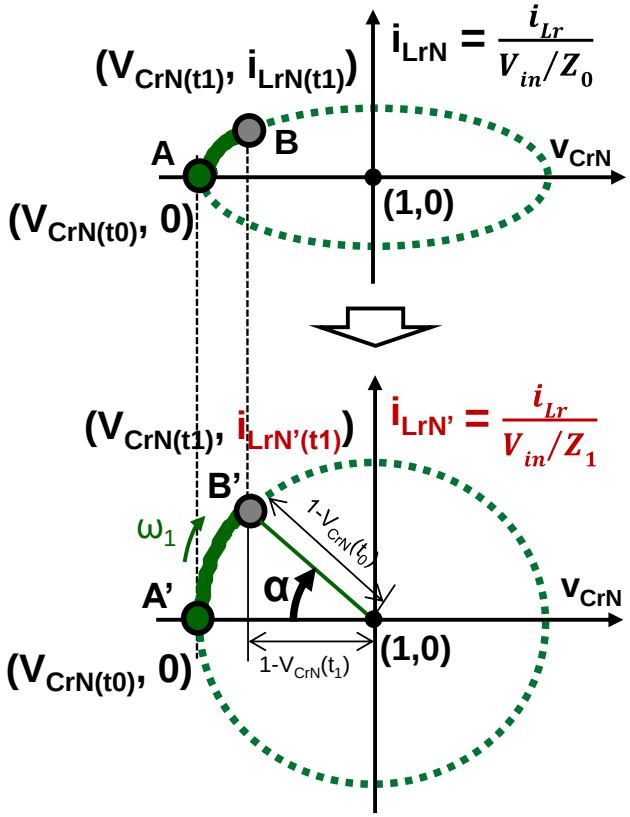


Fig. 5.32 Transformation from ellipse trajectory of Mode III to a circle

Therefore, by tuning Q_1 first-pulse width from (5.12) to (5.15), the dynamic oscillation could be eliminated when PWM dimming on-time starts as verified in Fig. 5.30 and Fig. 5.31.

Due to the variation of temperature and the aging of inductances and capacitances, the estimated first-pulse width might be different from the desired value. Figures 5.33 and 5.34 show the simulation results if Q_1 first-pulse width is 20% larger or 20% smaller. There are some oscillations in the resonant tank and the LED output current. In terms of the state plane, there are a bit more oscillations near the full-load steady-state circle. But the dynamic performance is still much better than the result without any optimal tuning.

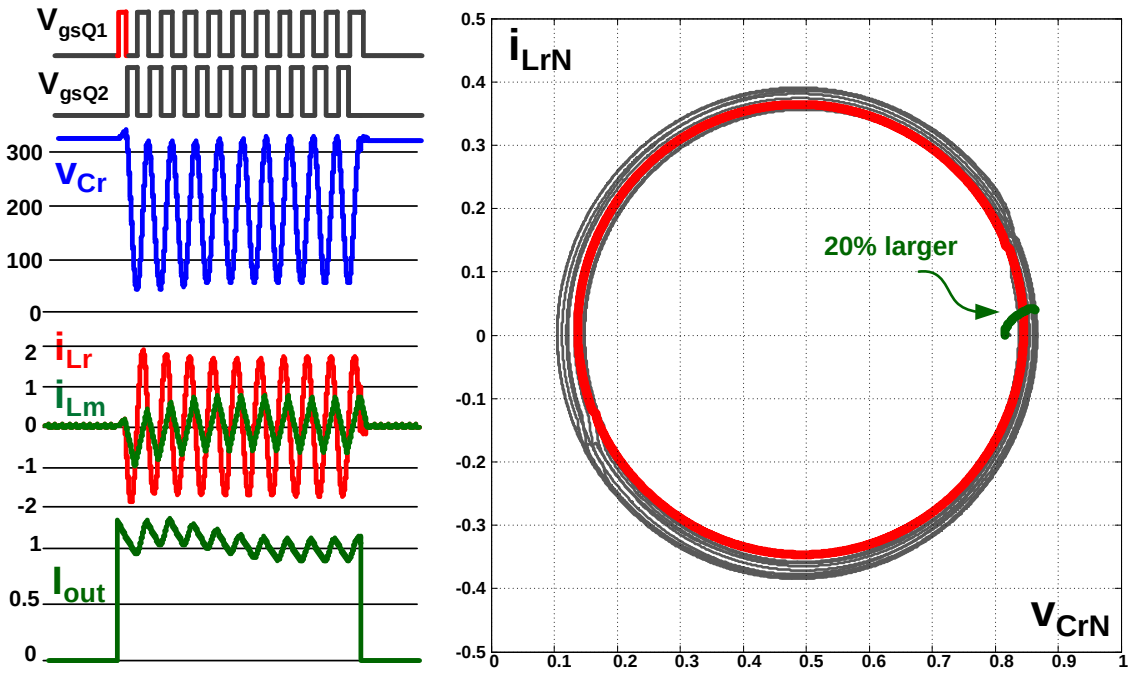


Fig. 5.33 Q_1 first-pulse width is 20% larger than the desired one

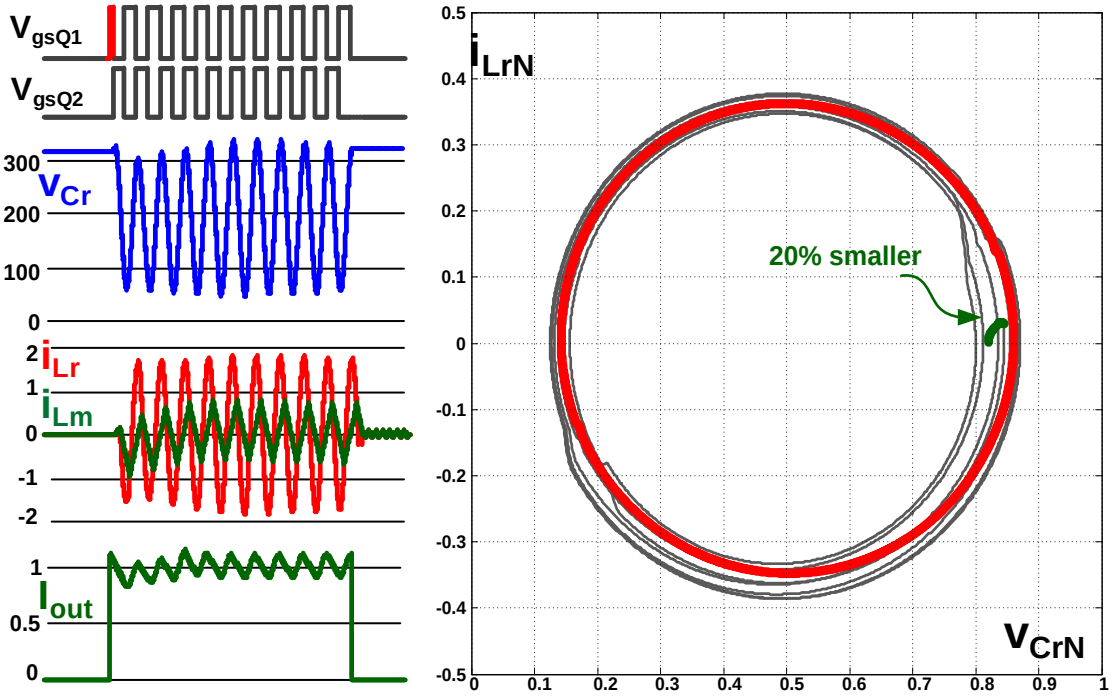


Fig. 5.34 Q_1 first-pulse width is 20% smaller than the desired one

5.3.4 Last-pulse tuning optimal PWM dimming

Similarly, during the PWM dimming on-time, compared with the first-pulse tuning, the last-pulse could be tuned as well to achieve the same good performance. As shown in Fig. 5.35 and 5.36, Q_1 last-pulse width is reduced. As a result, the initial condition $v_{Cr}(t_0)$ will be changed when the MC^3 LLC starts to work again in the next PWM dimming cycle. From Fig. 5.36 state trajectory, by tuning the last-pulse width, the full-load steady-state circle can be reached in one-pulse time.

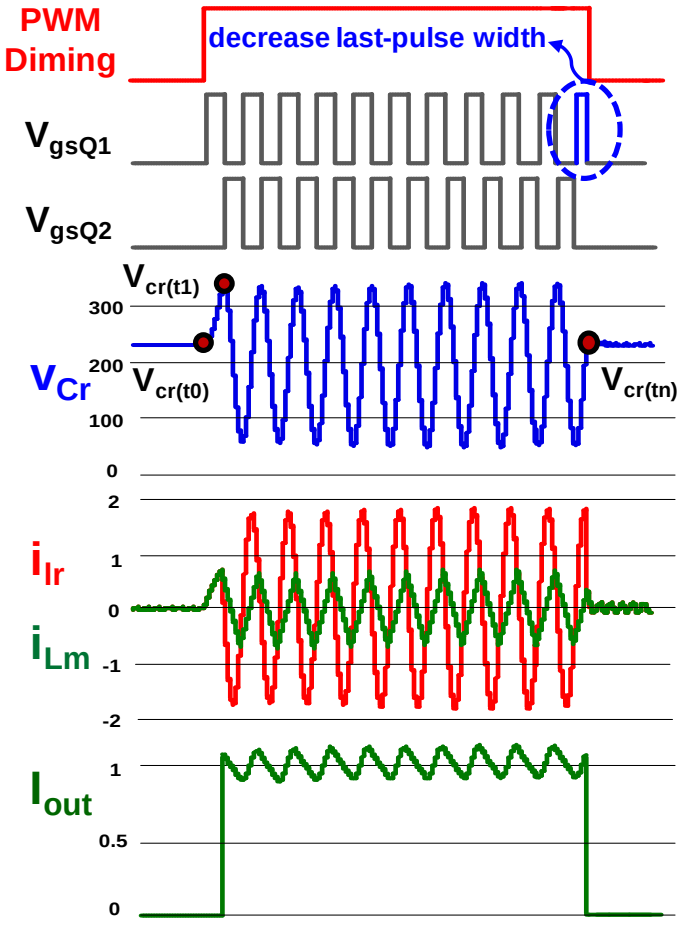


Fig. 5.35 Time-domain waveforms of the last-pulse-tuning optimal switching pattern

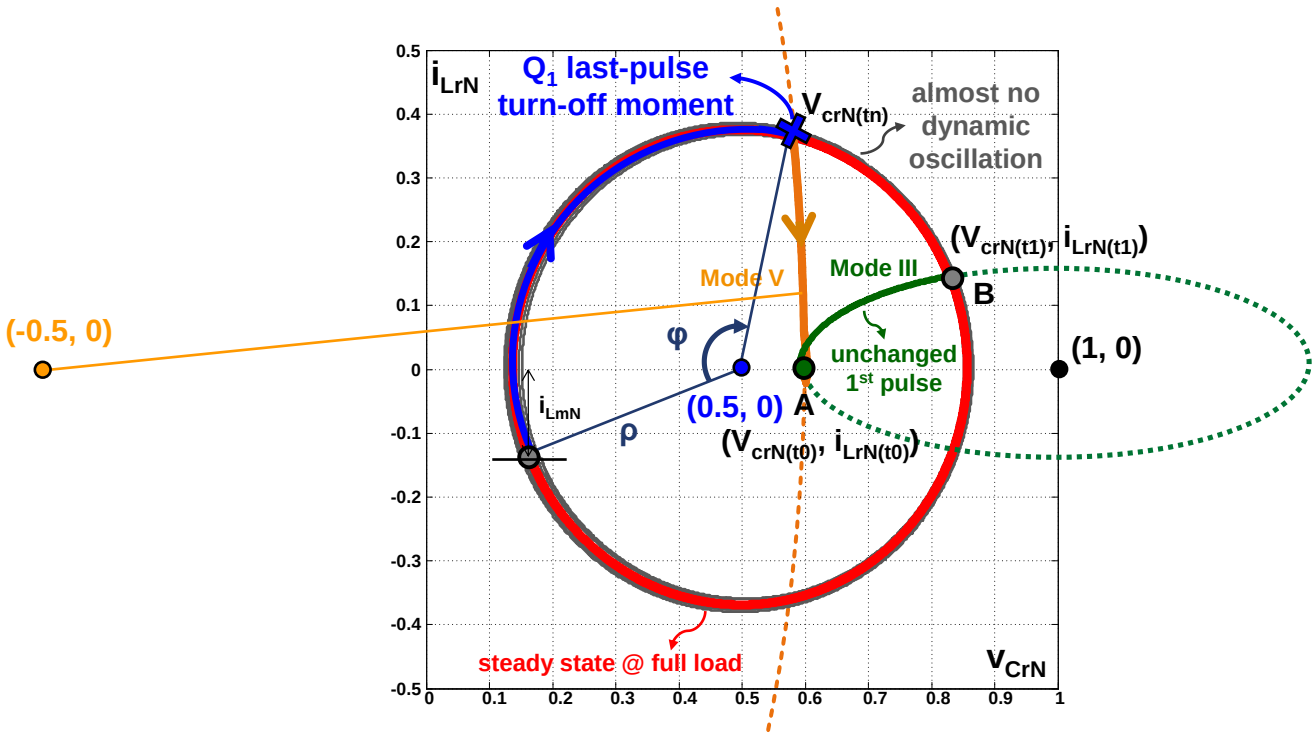


Fig. 5.36 State-trajectory of the last-pulse-tuning optimal switching pattern

Based on the graphic state-plane analysis, Q_1 last-pulse width could be estimated as well. Since Q_1 first-pulse width keeps unchanged, it is half of the resonant period (i.e. $T_0/2$). During this first pulse, the magnetizing inductor L_m is in the resonance of Mode III. It will go through a partial ellipse trajectory as shown in Fig. 5.36. If changing the current normalizing factor to V_{in}/Z_1, this ellipse trajectory will change to partial circle with the center (1, 0) as illustrated in Fig. 5.32. Since the first-pulse duration is $T_0/2$, the corresponding conduction angle α on the new state plane is:

$$\alpha = \frac{T_0}{2} \cdot \omega_1 = \frac{2\pi\sqrt{L_r C_r}}{2} \cdot \frac{1}{\sqrt{(L_m + L_r)C_r}} = \pi\sqrt{\frac{L_r}{(L_m + L_r)}} \tag{5.16}$$

Thus, the coordinate of point B' ($v_{CrN}(t_1)$, $i_{LrN'}(t_1)$) as shown in Fig.5.32 is

$$v_{CrN}(t_1) = 1 - \left(1 - v_{CrN}(t_0)\right) \cdot \cos\alpha, \tag{5.17}$$

$$i_{LrN'}(t_1) = \left(1 - v_{CrN}(t_0)\right) \cdot \sin\alpha, \tag{5.18}$$

where N' represents the current normalizing factor of V_{in}/Z_1.

Converting the current normalizing factor to V_{in}/Z_0, the normalized resonant current at B point is

$$i_{LrN}(t_1) = i_{LrN'}(t_1) \cdot \frac{Z_0}{Z_1}. \tag{5.19}$$

As shown in Fig. 5.36, after Q_1 first-pulse conducting for $T_0/2$, the ellipse trajectory will hit the steady-state red circle. Thus, point B is on the steady-state circle with the center (0.5, 0), which means

$$\left(v_{CrN}(t_1) - 0.5\right)^2 + i_{LrN}{}^2(t_1) = \rho^2. \tag{5.20}$$

Therefore, from (5.16) to (5.20), $v_{CrN}(t_0)$ at point A could be solved.

When Q_1 last-pulse is early turned off, the resonant current i_{Lr} will go through Q_2 body diode. As illustrated in Fig. 2.3, it operates in Mode V. As shown in Fig. 5.36, it is partial circle with the center (-0.5, 0). Since this circle is much larger than the steady-state one. This partial circle can be simplified as a vertical line. Thus, $v_{CrN}(t_n)$ at Q_1 turn-off moment is approximately to be equal to $v_{CrN}(t_0)$, that is,

$$v_{CrN}(t_n) = v_{CrN}(t_0) \tag{5.21}$$

As shown in Fig. 5.36, the last-pulse conduction angle φ on the state plane is

$$\varphi = \sin^{-1}\left(\frac{i_{LmN}}{\rho}\right) + \cos^{-1}\left(\frac{0.5 - v_{CrN}(t_n)}{\rho}\right) \tag{5.22}$$

where i_{LmN} is Q_2 turn-off current under the steady state.

Converting this state-plane angle φ to the time-domain conduction time, the optimized Q_2 last-pulse width could be determined as

$$\Delta T = \frac{\varphi}{\omega_0} = \varphi\sqrt{L_r C_r}. \tag{5.23}$$

To sum up, by tuning Q_1 last-pulse width as (5.23), when the MC^3 LLC starts to work again in the next PWM dimming cycle, the initial condition has been changed. Although maintaining Q_1 first-pulse, the dynamic oscillation could be eliminated as well when PWM dimming on-time starts.

The parameter-tolerance of (5.23) is discussed below. If the pre-determined Q_1 last-pulse width is 20% larger or 20% smaller than the required value, the simulation results are shown in Figs. 5.37 and 5.38. There will be some oscillations near the full-load steady state. However, compared with the result without any optimal tuning in Figs. 5.28 and 5.29, they are quite acceptable.

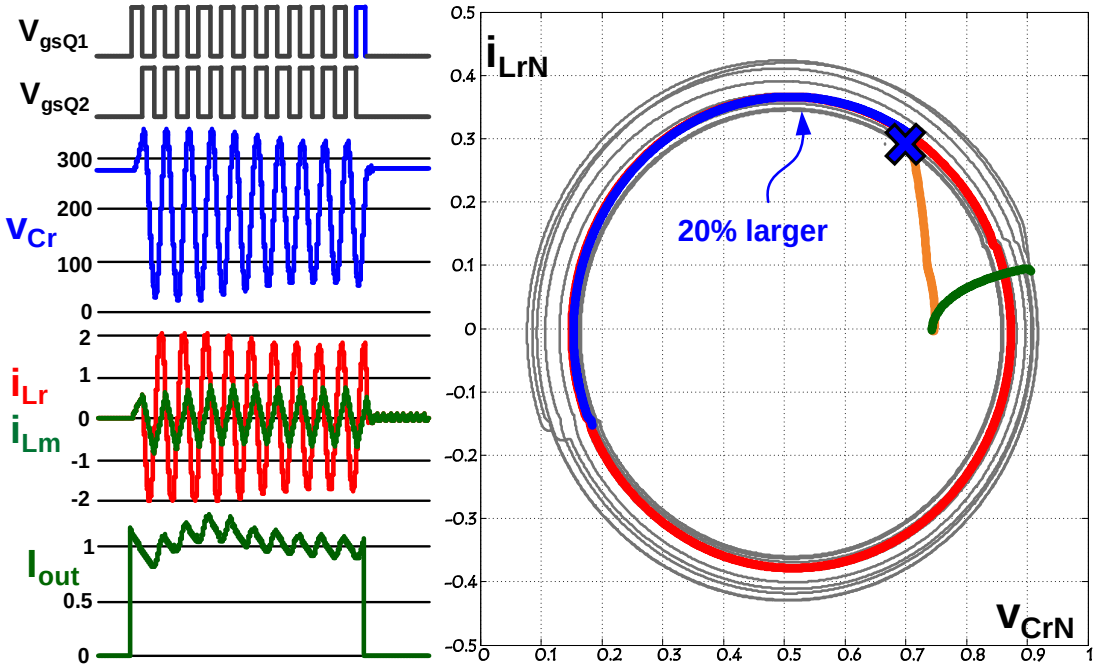


Fig. 5.37 Q_1 last-pulse width is 20% larger than the desired one

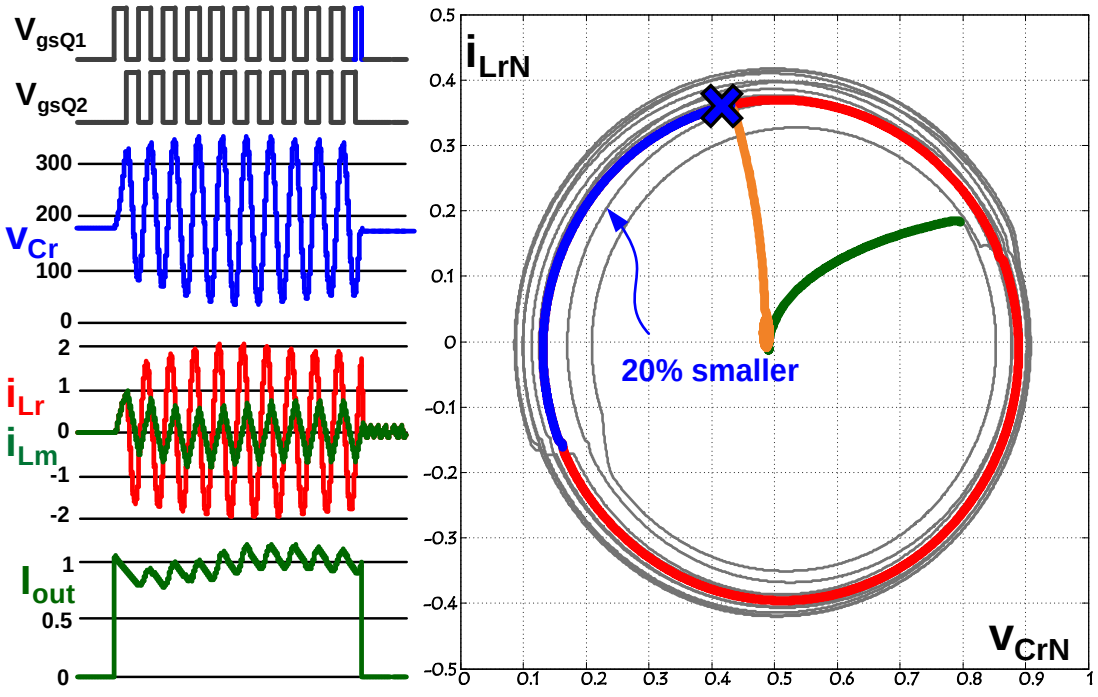


Fig. 5.38 Q_1 last-pulse width is 20% smaller than the desired one

5.3.5 Experimental results

The optimal trajectory approaches for the PWM dimming are verified on the 200W, 4-channel MC^3 LLC resonant LED driver prototype as shown in Fig. 5.39, whose parameters are shown in Table 5.2. The proposed optimal switching pattern is built in a Cyclone III FPGA using Verilog HDL.

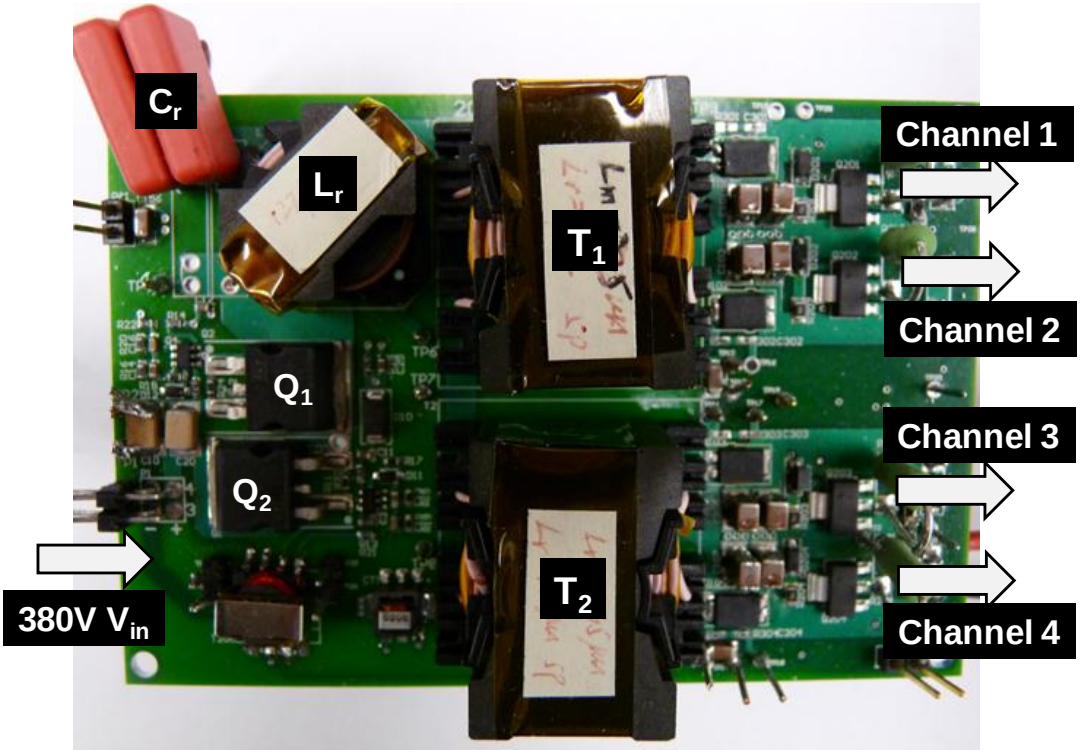


Fig. 5.39 MC^3 LLC resonant LED driver prototype

As shown in Fig. 5.40, when it comes to 2% dimming ratio, if without proposed optimal switching patterns, there are dynamic oscillations when MC^3 LLC LED driver starts to work from the idle status. As a result, the LED current cannot be controlled precisely, especially under lower dimming conditions.

Table 5.2 The parameters of MC^3 LLC resonant converter

	Parameters	**Value**
Initial Design	Input voltage	380V
	LED full-load current I_{Full}	1A
	LED string full-load voltage	48V
	Resonant frequency f_0	100kHz
	Inductor ratio $L_n=L_m/L_r$	5
	Transformer (T_1, T_2) turn ratio	2:1
	PWM dimming frequency	200Hz
Resonant Tank	Resonant capacitor C_r	20nF
	Resonant inductor L_r	123 μH
	T_1 leakage inductor L_{k1}	3.2 μH
	T_2 leakage inductor L_{k2}	3.4 μH
	T_1 magnetizing inductor L_{m1}	336 μH
	T_2 magnetizing inductor L_{m2}	335 μH
Devices	Primary main switches Q_1&Q_2	STD13NM60N
	Secondary schottky diode	PDS4150
	Output switches $S_{1,2,3,4}$	BSC123N08NS3

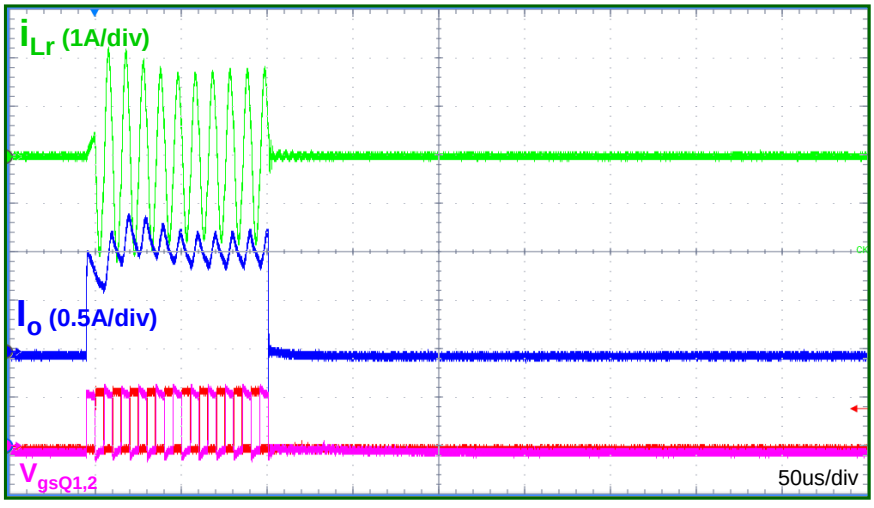


Fig. 5.40 Experiment without optimal switching pattern (2% dimming)

Then the first-pulse-tuning optimal switching pattern is employed as shown in Fig. 5.41. Q_1 first-pulse width is tuned to be about $T_0/4$ as derived from (5.15), which is half of the original one. After that, the resonant current (i_{Lr}) will settle to the full-load steady state in the minimal period of time. There is no dynamic oscillation on the output current. The last-pulse-tuning optimal switching pattern is verified as shown in Fig.5.42. From (5.22), the conduction angle φ is $2\pi/3$, that is, Q_1 last-pulse width is tuned to be $T_0/3$ in (5.23), which is 1/3 less than the original one. Similarly, the full-load steady state can be tracked in one-pulse time.

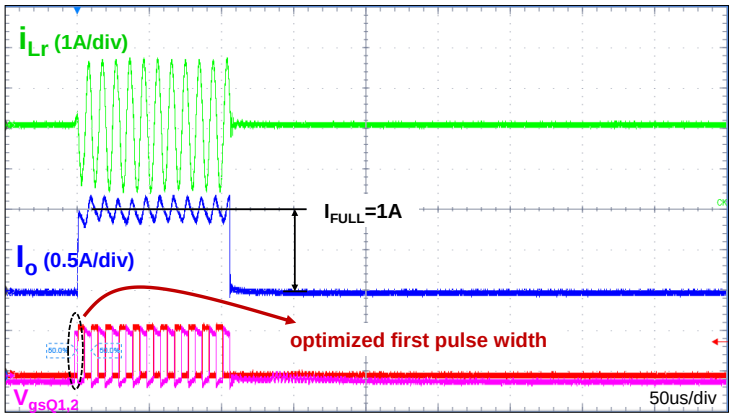


Fig. 5.41 Experiment of the first-pulse-tuning optimal switching pattern (2% dimming)

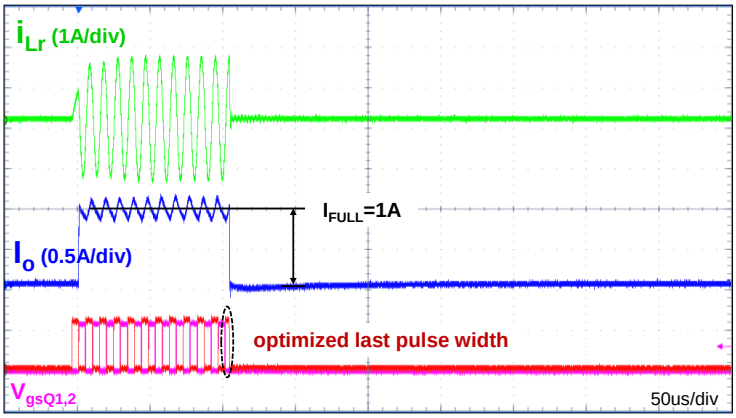


Fig. 5.42 Experiment of the last-pulse-tuning optimal switching pattern (2% dimming)

Since there is no dynamic oscillation by tuning the first or last pulse width, as shown in Fig. 5.43, the LED luminary intensity can be controlled precisely even under 1% dimming condition.

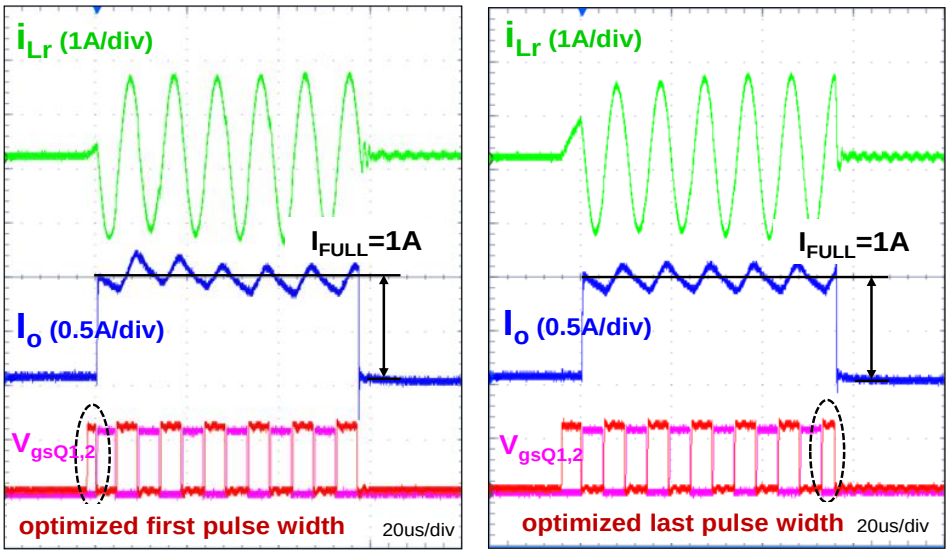
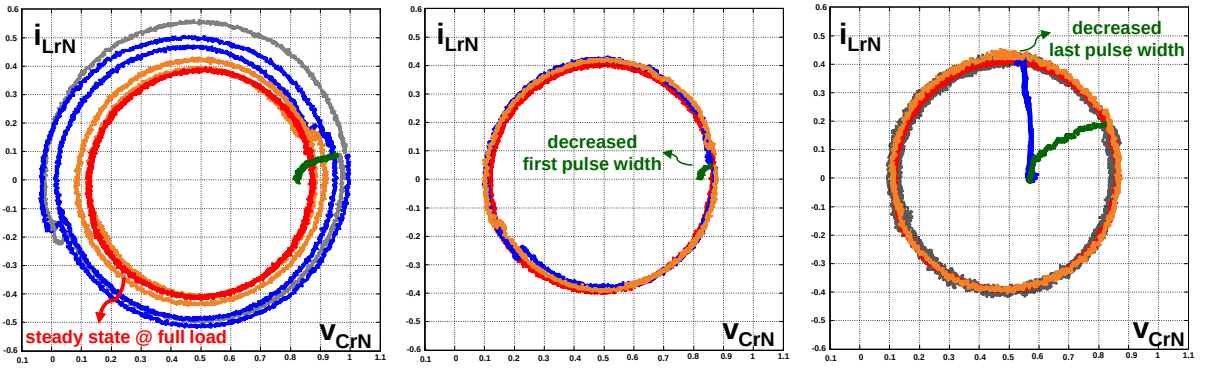


Fig. 5.43 First-pulse and last-pulse tuning optimal switching pattern under 1% dimming

Fig. 5.44 shows the experimental trajectory comparison. By applying the proposed optimal switching patterns, the full-load steady state is tracked quickly. The dynamic trajectories are quite clean.



(a) without optimal switching pattern (b) first-pulse-tuning optimal switching pattern (c) last-pulse-tuning optimal switching pattern

Fig. 5.44 Experimental trajectory comparison

As the LED dimming ratio increases, the PWM dimming on-time increases correspondingly as shown in Fig. 5.45. With the proposed optimal switching patterns, the output current is always flat during the dimming on-time.

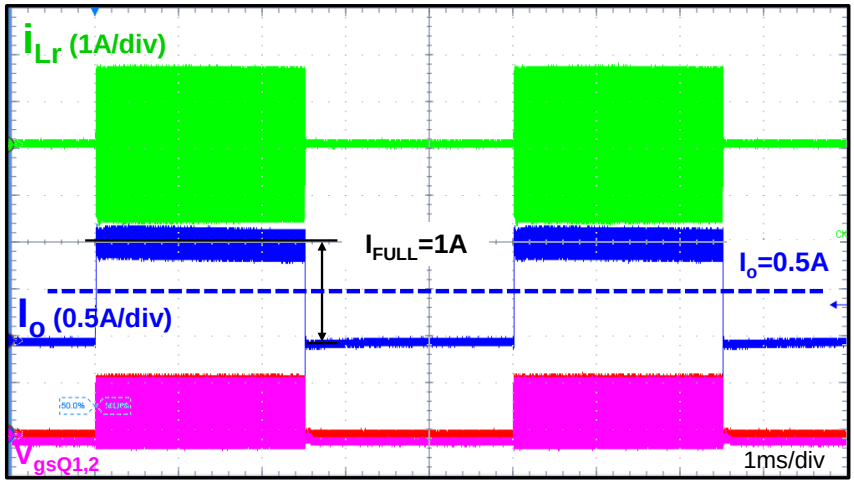


Fig. 5.45 Experiment with optimal switching patterns (50% dimming)

Fig. 5.46 shows the efficiency comparison. Using the switching frequency controlled analog dimming approach, the efficiency drops quickly as the dimming ratio decreases. Since the switching frequency needs to increase to high, and it will produce more switching and driving losses. By employing the PWM dimming with proposed optimal switching pattern, the efficiency curve becomes flat from the full-load status. Since the MC^3 LLC does always operate under the full-load steady state. Even under 1% dimming condition, the efficiency is still higher than 94%. (The efficiency is tested without considering the FPGA losses, since the final target is the IC integration, whose power consuming is much less than the FPGA.)

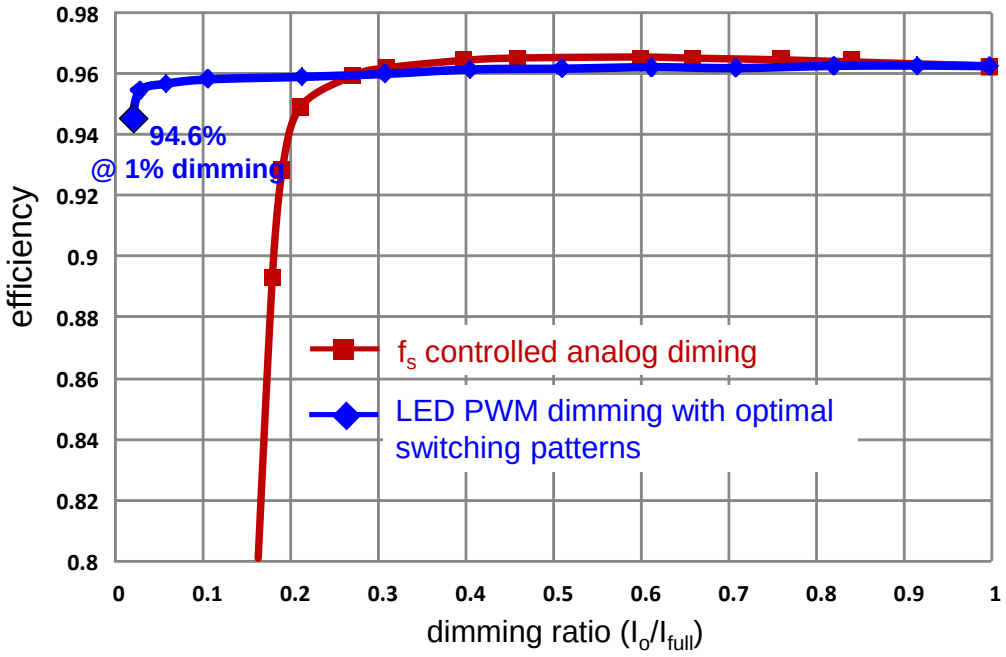


Fig. 5.46 Efficiency comparison with f_s controlled analogy dimming

5.4 Conclusion

In this chapter, some optimal switching patterns for burst pulses are proposed for LLC resonant converters to keep high efficiency within the whole load range.

The three-pulse optimal switching pattern is proposed to achieve the best light-load efficiency and minimal output voltage ripple. The burst on-time is maintained, but the burst off-time is modulated by the light load conditions. Based on the state-plane trajectory, during the burst on-time, the first switching pulse width is optimized to settle to the steady state of the highest efficiency load condition in one pulse time. And the next two pulses operate at the resonant frequency point to follow the steady-state trajectory of the highest efficiency load. With

the proposed burst mode, under all light loads, the LLC equivalently operates under the steady state of the best efficiency load condition. Thus, high light-load efficiency is achievable.

For the LED PWM dimming, two optimal switching patterns of the LLC resonant LED driver are proposed. One is tuning the first-pulse width during the PWM dimming on-time. Thus, the full-load steady state can be tracked within one-pulse time. Another one is tuning the last-pulse width, which will change the initial condition as the next PWM dimming cycle starts. Both of these will eliminate the dynamic oscillations in the resonant tank. Thus, flat output current can be achieved. As a result, the efficiency stays flat from the full-load point. Under low dimming conditions, the LED intensity can be controlled more precisely.

Chapter 6. Efficiency Improvement II: Universal Adaptive SR Driving Scheme and Extended Resonant Frequency Tracking

To improve the efficiency, the synchronous rectifiers (SR) are employed for the LLC resonant converter. A universal adaptive driving scheme for synchronous rectification (SR) is proposed in this chapter. The SR drain to source voltage is sensed, so that the paralleled body diode conduction is detected. Using the proposed SR driving scheme, the SR turn-off time is tuned to eliminate the body diode conduction. The SR gate driving signal can be tuned within all operating frequency regions. Moreover, a simple digital implementation is introduced. Compared with analog ones, it enables more intelligent and precise SR control. In addition, a pulse-width locked loop (PWLL) is presented for LLC-DCX resonant frequency tracking. By minimizing the pulse width difference between the main switch and the well-tuned SR gate-driving signals, the LLC-DCX always runs at the f_0 point to achieve the best efficiency.

6.1 Introduction

The LLC resonant converter is becoming more and more popular for its high efficiency, because of both ZVS for the primary-side main switches and ZCS for the secondary-side rectifiers. To further improve the efficiency, the synchronous rectifiers (SR) are employed, since the conduction loss is much lower than that of the diode rectifiers. However, the efficiency optimization depends on the well-adjustment of SR gate driving signals.

The desired SR gate driving signals for the LLC resonant converter are shown in Fig. 6.1. In different switching frequency regions, when the primary main switches Q_1 and Q_2 are turned on, the secondary side current i_{SEC} starts to go through the SRs, thus the SRs should be turned on synchronously with the main switches. However, the turn-off times of the SRs and the main switches are not exactly in phase. When operating below the resonant frequency (i.e. $f_s<f_0$), the SR should be turned off earlier than the main switch. Otherwise, the SR would conduct circulating energy, namely a reverse current from the load to the source, thus producing a greater increase in the RMS currents and turn-off current, and causing efficiency to deteriorate dramatically. When operating above the resonant frequency ($f_s>f_0$), the SR should be turned off a bit later than the main switch. Otherwise, the sharply decreased current would go through the paralleled body diode, resulting in a serious reverse recovery.

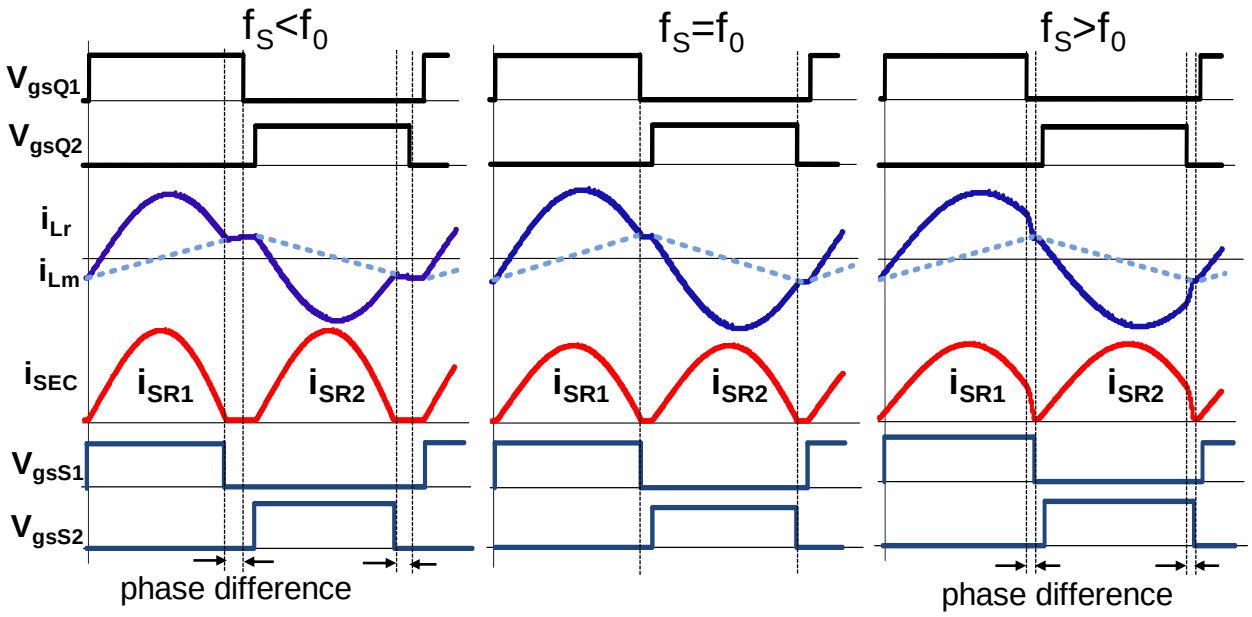


Fig. 6.1 Desired SR gate driving signals in different switching frequency regions

Therefore, the gate driving signals of SRs and main switches cannot derive from the same signal for controlling the conduction times as those in the PWM converters. Presently, there have been proposed several SR driving schemes [E.1-E.8].

One solution [E.1] is sensing secondary side current i_{SEC} to generate SR gate driving signal as shown in Fig. 6.2. This method is precise, but due to the large current on the secondary side, it requires a large size current transformer and it presents a lower efficiency due to the extra resistance of the transformer windings.

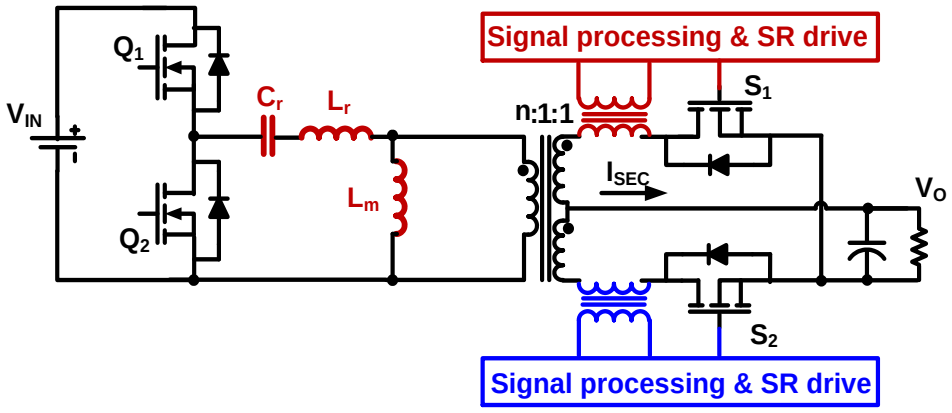


Fig. 6.2 Secondary side current sensing for SR driving

An alternative solution [E.2] is sensing current through the transformer's primary side winding as shown in Fig. 6.3. Provided that the resonant inductor L_r and magnetizing inductor L_m are external to the main transformer, the current though primary side winding is a precise replica of the secondary side current. Although a smaller loss could be achieved when compared to the secondary side current sensing, three magnetic components are needed, losing the integration of leakage, magnetizing inductors and transformer into one single element.

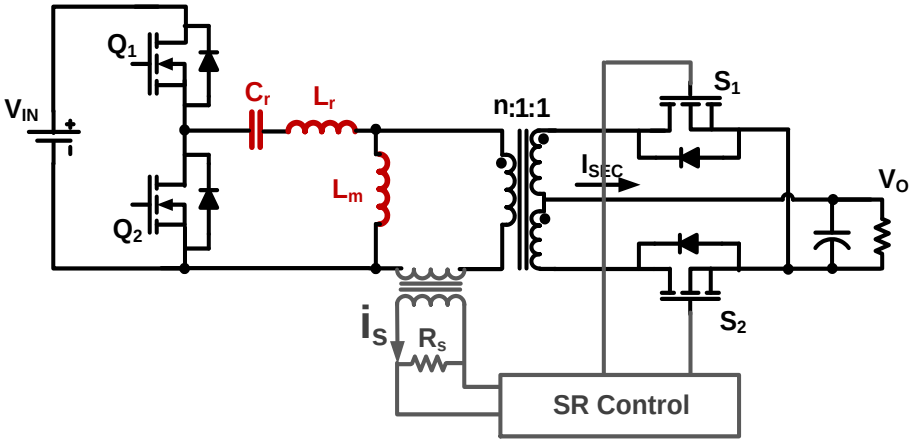


Fig. 6.3 Primary side current sensing for SR driving

In [E.3], the authors proposed a primary side resonant current i_{Lr} sensing method to determine the SR gate driving signals. However, it needs to decouple the magnetizing current i_{Lm}, and thus complicated auxiliary circuit is added.

Figure 6.4 shows a promising driving method based on sensing the SR drain to source voltage V_{dsSR}. The sensed V_{dsSR} is processed by the control circuits as follows [E.4]:

- before the SR is turned on, the paralleled body diode conducts shortly and there is a large forward voltage drop, which is compared with a threshold voltage V_{th_on} to turn on the SR;
- when the SR current is decreasing toward zero, V_{dsSR} also becomes small, which is then compared with another threshold voltage V_{th_off} to turn off the SR.

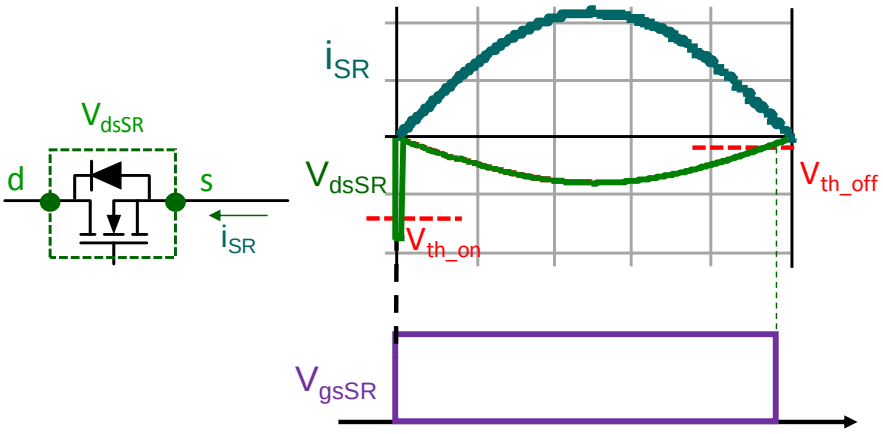


Fig. 6.4 Drain-to-source voltage V_{dsSR} sensing for SR driving

However, the accuracy of this driving scheme is highly affected by the SR package [E.5] [E.6]. Due to the inevitable package inductance, the sensed terminal drain to source voltage of the SR ($V_{d's'SR}$) is actually the sum of the MOSFET's on-status resistive voltage drop and the package inductive voltage drop, which deviates greatly from the purely resistive voltage drop of the MOSFET as the switching frequency increases. Therefore, the actual SR drive signal V_{gsSR} is significantly shorter than the expected value as shown in Fig. 6.5.

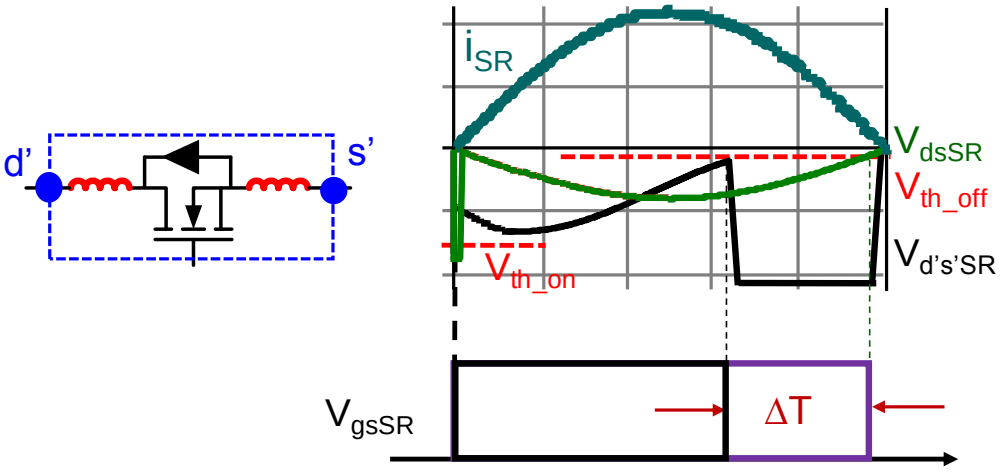


Fig. 6.5 Package inductance influence on SR driving

To compensate for the inductive characteristic of the sensed $V_{d's'}$, a carefully designed capacitive network can be connected to the sensed terminals [E.6], as shown in Fig. 6.6.

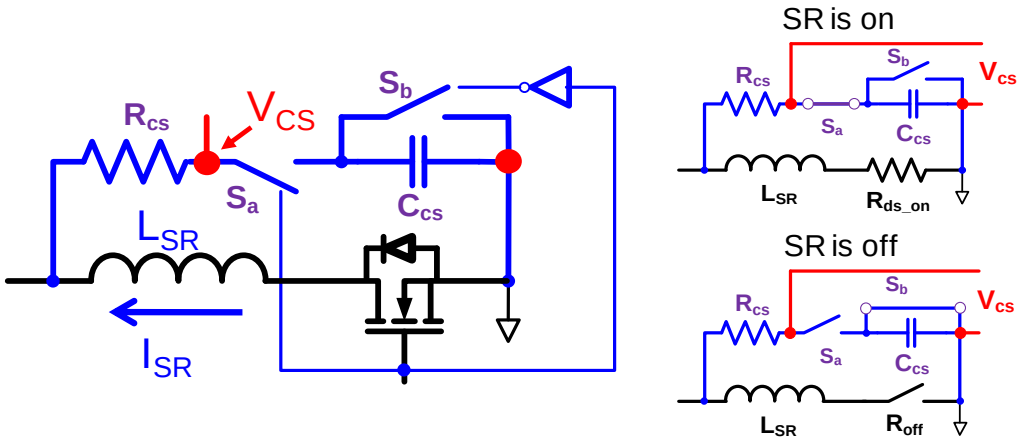


Fig. 6.6 The capacitive compensator network

However, the package inductance L_{SR} and the pure resistor R_{ds_on} need to be determined in advance to calculate the parameters of the components: C_{CS} and R_{CS} in the capacitive network. Although the inductive phase lead influence is diminished, the design and the parameter tuning are complicated.

Different from the above mentioned V_{ds} sensing, in [E.7],[E.8] the SR body diode forward voltage drop is detected to tune the gate driving signal. As shown in Fig. 6.7, V_{gsQ} is the primary main switch driving signal, and it synchronizes the sawtooth waveform V_{saw}, which is then compared with a control signal V_c to generate the SR driving signal V_{gsSR}. If the body diode conducts, the large forward voltage drop is sensed by the valley detection circuit; then V_c increases, and V_{gsSR} pulse width increases accordingly. Finally, the SR is tuned until the circuit cannot detect the body diode conduction. However, the maximum pulse width of the SR driving signal cannot be larger than that of the main switch, and thus it cannot be used when $f_s>f_0$. As

shown in Fig. 6.1, the SR pulse width should be tuned slightly larger than the main switch when $f_s > f_{0.}$ Moreover, the design process of the analog compensator to generate V_c is complicated.

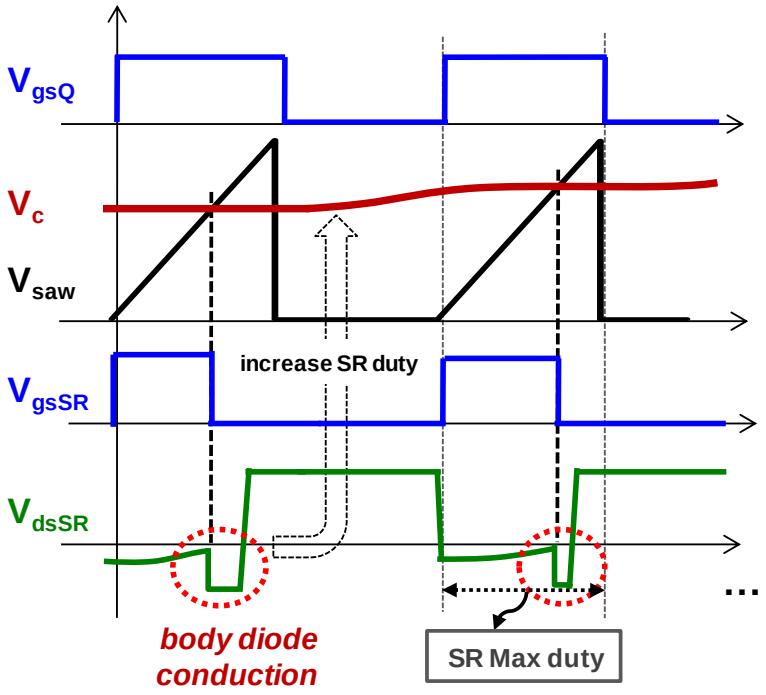


Fig. 6.7 Paralleled body diode conduction elimination for SR tuning

Therefore, an intelligent SR driving scheme is required, which can control the SR gate driving signal in the whole switching frequency regions with simple implementation.

6.2 Universal Adaptive SR Driving Scheme

6.2.1 Auto-tuning principle by detecting SR body-diode conduction

To well tune the SR gate driving signal within all switching frequency regions, the universal adaptive driving scheme is proposed as shown in Fig. 6.8. The turn-on time of the SR is the same with the primary main switch, but the turn-off time is digitally tuned based on the sensed SR

drain to source voltage V_{dsSR}. When the SR is turned off, the body diode conduction is detected by a comparator (CMP), since its forward voltage drop is much larger when compared with the MOSFET's on-status resistive voltage drop. If the body diode conducts, the SR pulse width is increased in the next switch cycle; if not, the SR pulse width is decreased. Thus, the SR gate driving signal is digitally tuned to eliminate the body diode conduction.

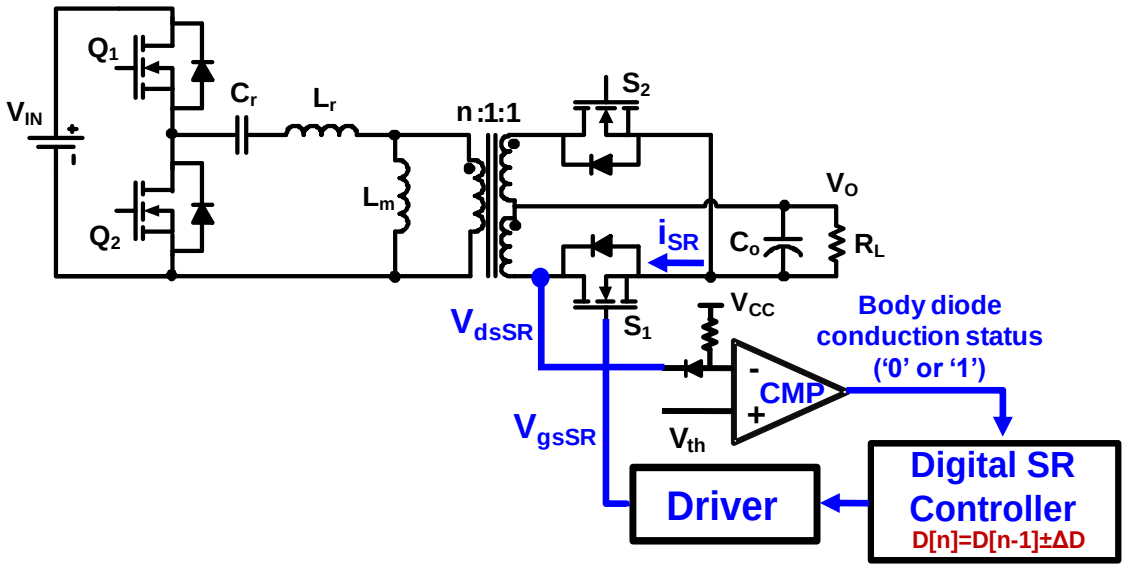


Fig. 6.8 Control blocks of the proposed universal adaptive SR driving scheme

The main waveforms are also reported in Fig. 6.9. The sensed V_{dsSR} is compared with the threshold voltage V_{th} at every turn-off moment, and then the compared result is sent to the digital logics. If body diode conducts, the comparator (CMP) output is high ('1'). As a consequence, the SR pulse width is increased in order to reduce the body diode conduction time. When the comparator output is low ('0'), there is no body diode conduction and the SR is considered to be tuned. Since it is not possible to detect when the SR pulse width is larger than needed, when the

comparator output is low, the SR duty is decreased by ΔD. Finally, the tuning algorithm alternates between the conditions reported in Fig. 6.9 (c) and 6.9 (d).

Since the SR gate driving signal is tuned in the closed loop, the delay effects produced by the comparator propagation, gate-driver propagation and so on can be compensated naturally. Now assuming these delays will make the SR turn off a bit later, and then the comparator will not sense the body diode conduction as in Fig. 6.9 (c). Thus, in the next switching cycle, the pulse width of SR gate driving signal will decrease correspondingly. Finally, it will alternate between the conditions shown in Fig. 6.9 (c) and 6.9 (d), which means that the delay effects have been compensated.

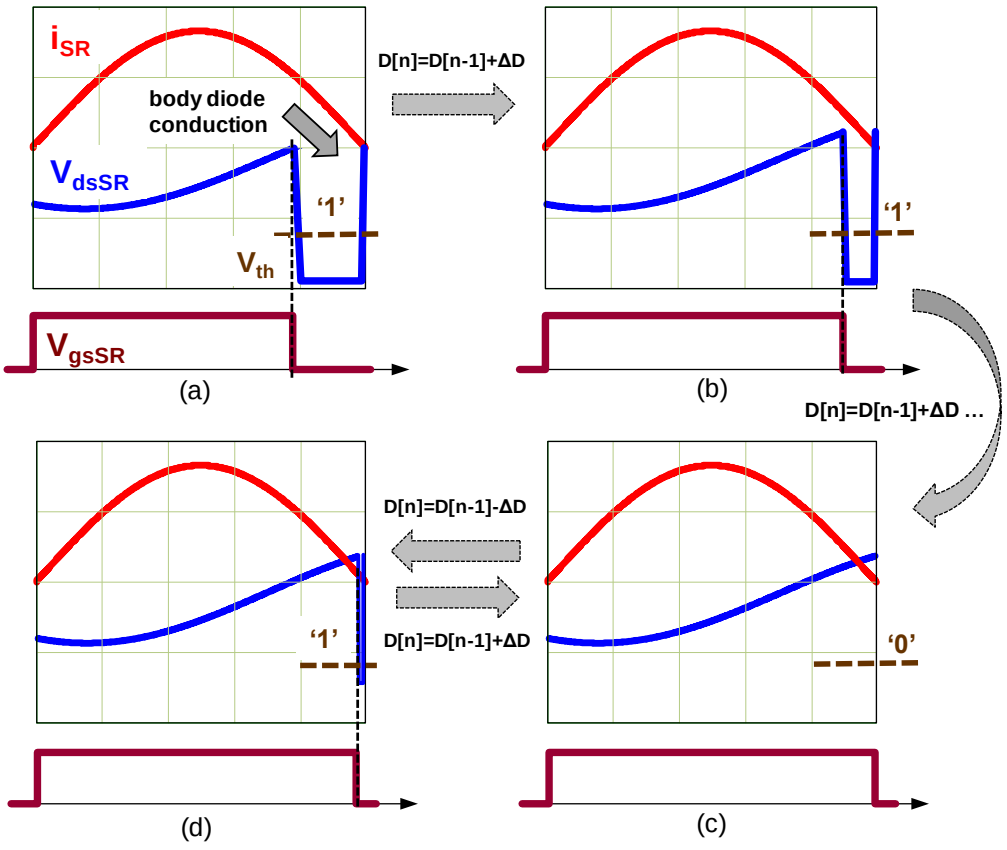


Fig. 6.9 SR turn-off tuning process by eliminating the body diode conduction

When $f_s>f_0$, if the SR is turned off earlier, the sharply decreased current will go through the body diode, producing a serious reverse recovery. However, with the proposed method, if a high time resolution is employed to sense the CMP output, the body diode conduction status could also be detected as well. Therefore, Fig. 6.10 shows that with the same process described above, the SR could be tuned well; to even $f_s>f_0$ region.

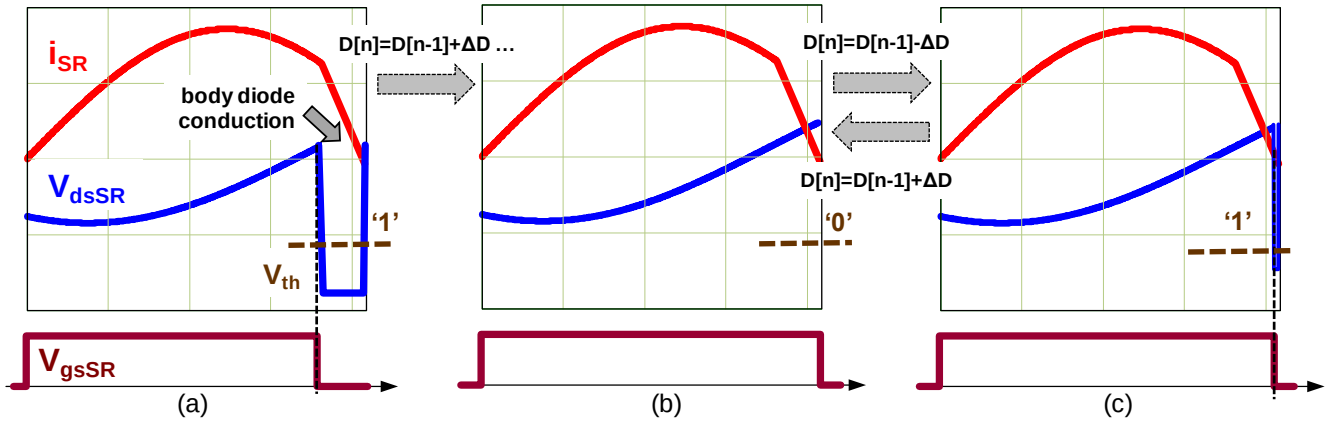


Fig. 6.10 The SR turn-off tuning process when $f_s>f_0$

As a summary, with the proposed universal adaptive SR driving scheme by minimizing the paralleled body diode conduction, the SR gate driving signal could be tuned within all operating frequency regions for the LLC resonant converter.

6.2.2 SR transient performance investigation

In the LLC resonant converter, the regulation of the output voltage is obtained by switching frequency variations. When the input voltage and load change slightly, the corresponding switching frequency f_s changes in the vicinity of resonant point f_0, assuming that this is the designed point at the nominal condition. During the holdup time, the input voltage decreases rapidly; accordingly, f_s decreases with a similar speed to obtain a high gain. During over current

protection (OCP) or the constant current limitation process, f_s increases quickly from a normal operating point to above the resonant frequency region. Therefore, it is important to verify that during all these transient conditions there is no shoot-through. For such purposes, the transients associated to switching frequency variations are hereafter described.

Let's start with an f_s decrease at time t_1 as shown in Fig. 6.11, that is, the pulse widths of main switch signals V_{gsQ1} and V_{gsQ2} increase. For $f_s<f_0$, the SR current goes to zero earlier than the turn-off time of V_{gsQ1} and V_{gsQ2} shown in Fig. 6.1. If the SR gate driving signal is tuned fast, the SR is turned off earlier than the main switch. Even if the SR tuning process is slower, the SR is still turned off earlier, since the pulse widths of V_{gsQ1} and V_{gsQ2} have increased. In both cases, there is no shoot-through.

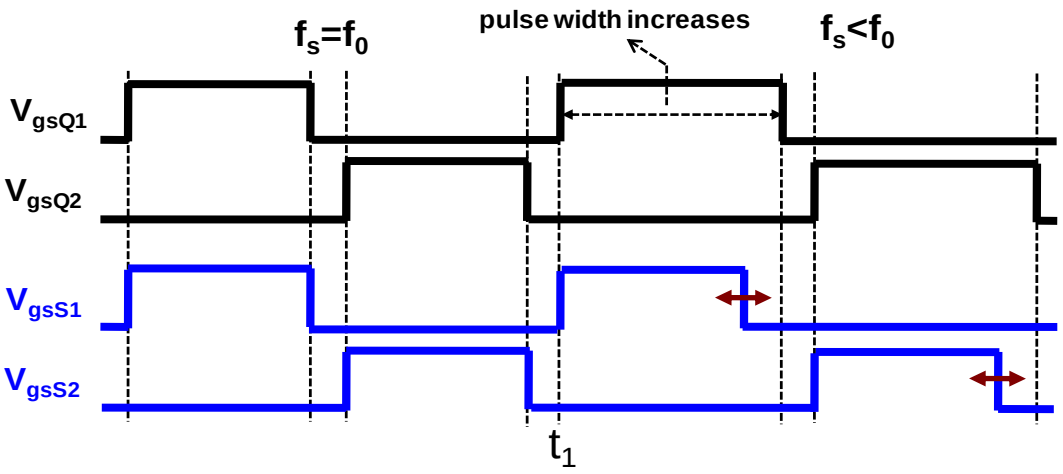


Fig. 6.11 Transient process as f_s decreases

Fig. 6.12 shows the case when f_s increases at time t_1, that is, the pulse widths of the main switch gate driving signals V_{gsQ1} and V_{gsQ2} decrease. If the SR tuning process is slow, as shown in Fig.6.12, this means that the SR doesn't response to the increased switching frequency. If

$$\Delta T_2 > \Delta T_1 + t_{dead}, \tag{6.1}$$

from t_3 to t_4, main switch Q_2 starts to conduct, but synchronous rectifier S_1 is still on. As a result, there will be a shoot-through between the main switch and the SR. Therefore, some protections should be designed to avoid shoot-through when f_s increases but SR does not respond quickly enough to follow the frequency variation.

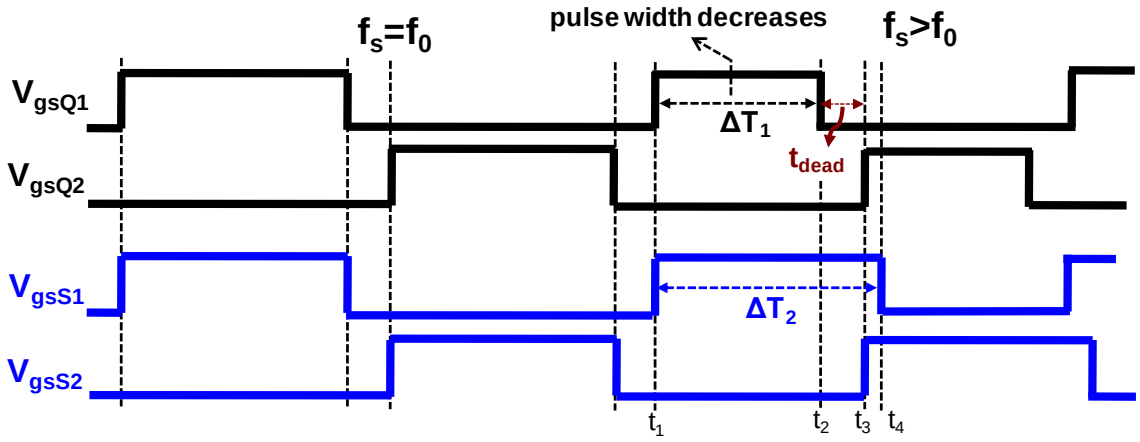


Fig. 6.12 Transient process as f_s increases

The provision that has been adopted is to limit the pulse width of the SR driving signal as shown in Fig. 6.13: if (6.1) is satisfied, the actual SR pulse width is limited to $\Delta T'_2$:

$$\Delta T'_2 = \Delta T_1 + \Delta t. \tag{6.2}$$

As shown in Fig. 6.1, since it is above the resonant frequency region ($f_s > f_0$), the SR should be turned off slightly later than the primary main switch, thus Δt is added as the delayed turn-off time. In order to avoid shoot-through, Δt should be designed smaller than the dead time t_{dead}.

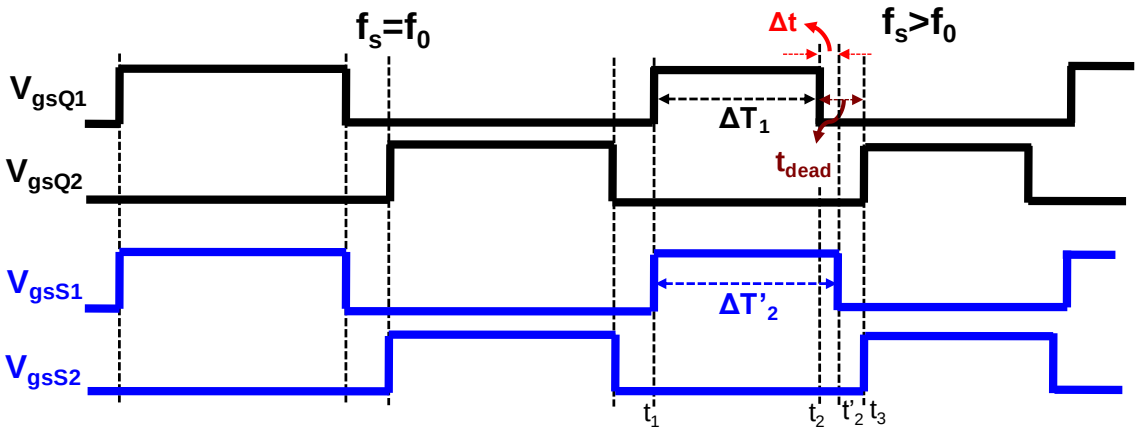


Fig. 6.13 SR pulse width limitation to avoid shoot-through when f_s increases

Sum up, Fig. 6.14 shows the flowchart of the proposed algorithm implemented in the digital logics. ΔD represents the time resolution of digital pulse width modulator (DPWM), which should be as small as possible to precisely tune the SR turn-off moment.

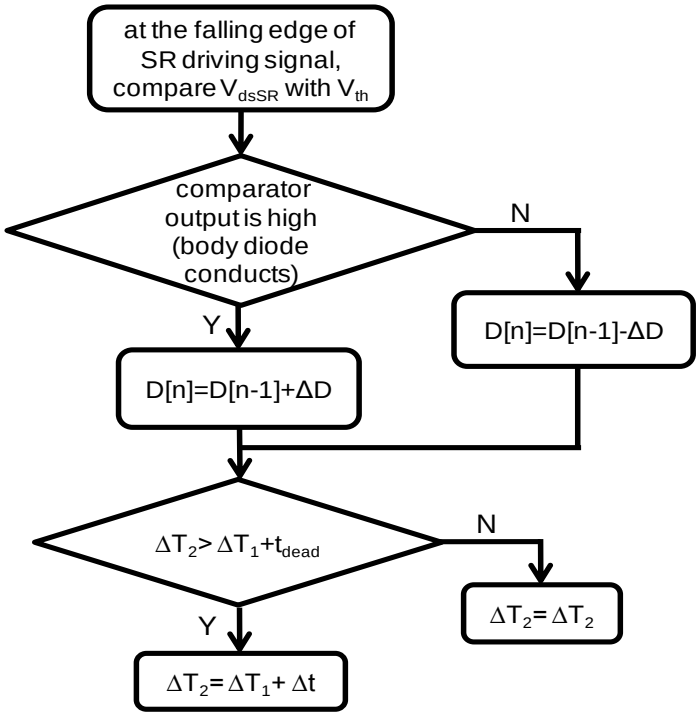


Fig. 6.14 Control flowchart of the proposed SR tuning process

6.2.3 Experimental results

The experiment is carried out on a 300W 400V/12V half bridge LLC resonant converter prototype. The main converter parameters are the same with Table 5.1. Fig. 6.15 shows the FPGA development kit, the LLC power stage, and the comparator board. The comparator board is plugged on the secondary side of the half bridge LLC resonant converter, comparing SR drain to source voltage V_{dsSR} with the threshold voltage V_{th} to determine the body diode conduction. Being a closed loop system, the delay time produced by the comparator, FPGA, and driver are compensated by the tuning algorithm.

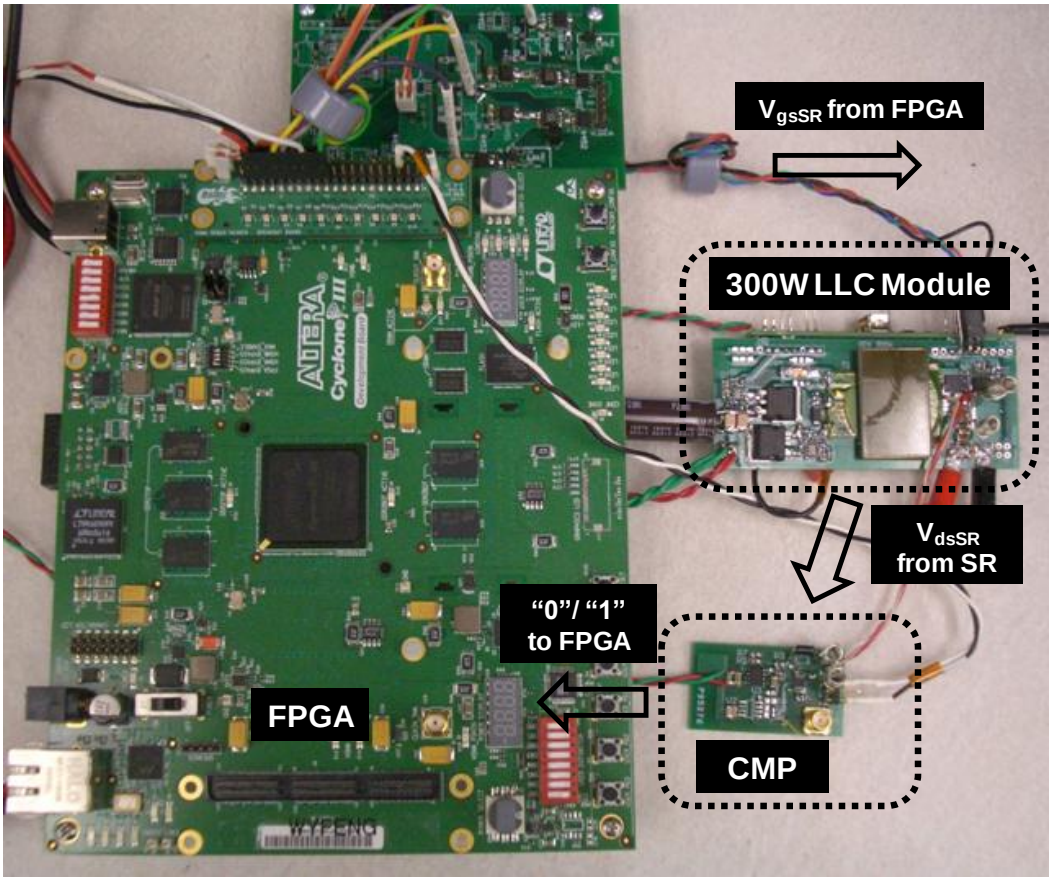


Fig. 6.15 Hardware implementation photograph

Even if the application is targeted to IC integration, for rapid prototyping purposes the SR controller is built in ALTERA Cyclone III FPGA using the Verilog HDL. The maximum clock frequency insider the FPGA is set to be 250MHz, thus the time resolution ΔD is 4ns. After the estimation, there are about 700 logic gates built in the FPGA.

The SR turn-on moment is the same with the primary main switch, but the turn-off time is tuned by the proposed universal adaptive driving scheme.

Fig. 6.16 shows that during SR on status, the voltage drop is much smaller than the body diode forward voltage drop, since the on-status resistor R_{ds_on} is very small. At time t_1, SR is turned off, and V_{dsSR} drops due to the body diode conduction, which is then compared with a threshold voltage V_{th}. Thus, the comparator (CMP) output V_{CMP} is high when body diode conducts.

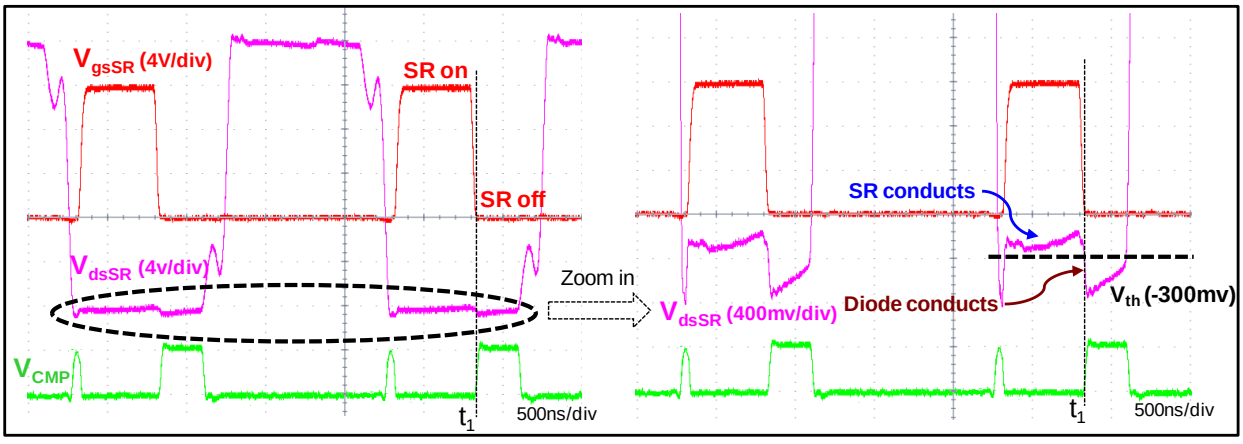


Fig. 6.16 Waveforms before SR tuning

Fig. 6.17 shows that after the tuning process, the SR paralleled body diode conducts for a very short time. The comparator output is '0', '1', … alternately, which demonstrates that the SR gate driving signal is always in the tuning process.

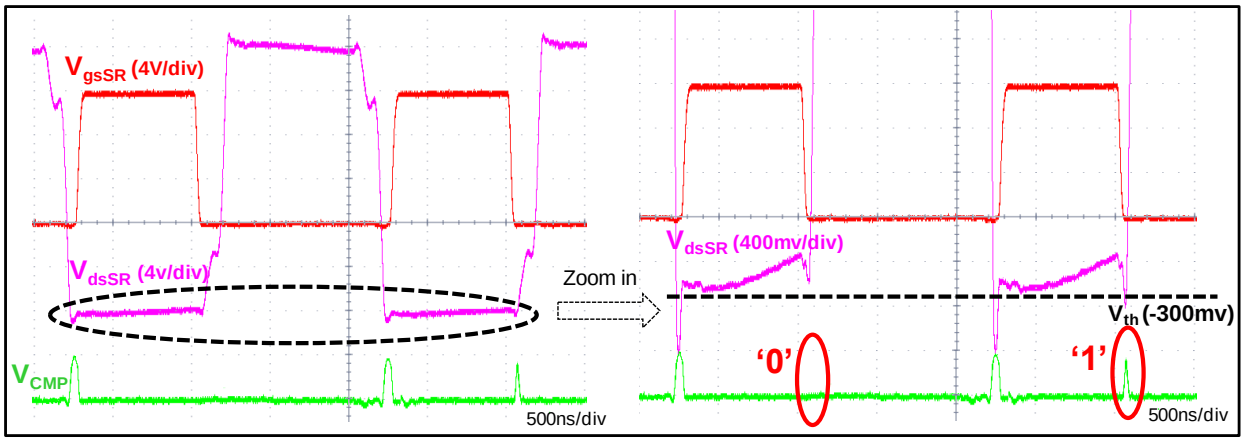


Fig. 6.17 Waveforms after SR tuning

Fig. 6.18 shows the SR gate drive waveforms using a commercial SR controller [E.4] designed for the LLC resonant converter. As analyzed in Section 6.1, due to the inductive characteristic of the sensed SR drain to source voltage, the SR is turned off earlier than desired. When f_s=500kHz, the SR duty cycle loss is nearly 170ns. Compared with this commercial SR controller, when using the proposed digital driving scheme, there is almost no SR duty cycle loss as shown in Fig. 6.19.

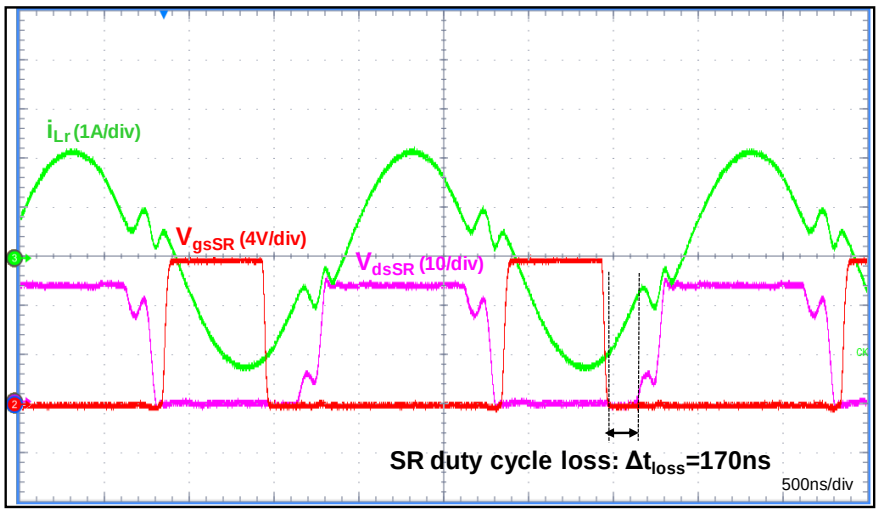


Fig. 6.18 SR duty cycle loss when using the commercial SR driving controllers

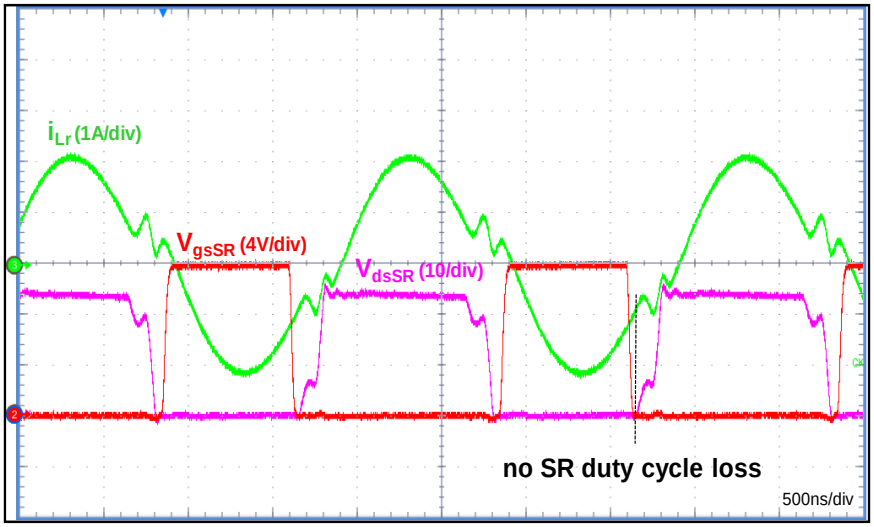


Fig. 6.19 Improved performance when using the proposed SR driving scheme

Fig. 6.20 shows the efficiency comparison between the commercial SR controller and proposed digital SR driving scheme. The LLC resonant converter efficiency is improved by 0.46% at the full load when f_s=500kHz. To increase the power density, the switching frequency f_s will be pushed to even higher in future; as a result, the influence of the parasitic inductance becomes

more serious. Thus there will be more duty cycle loss when using the commercial SR controllers. With the proposed solution, the efficiency improvement will become much more significant.

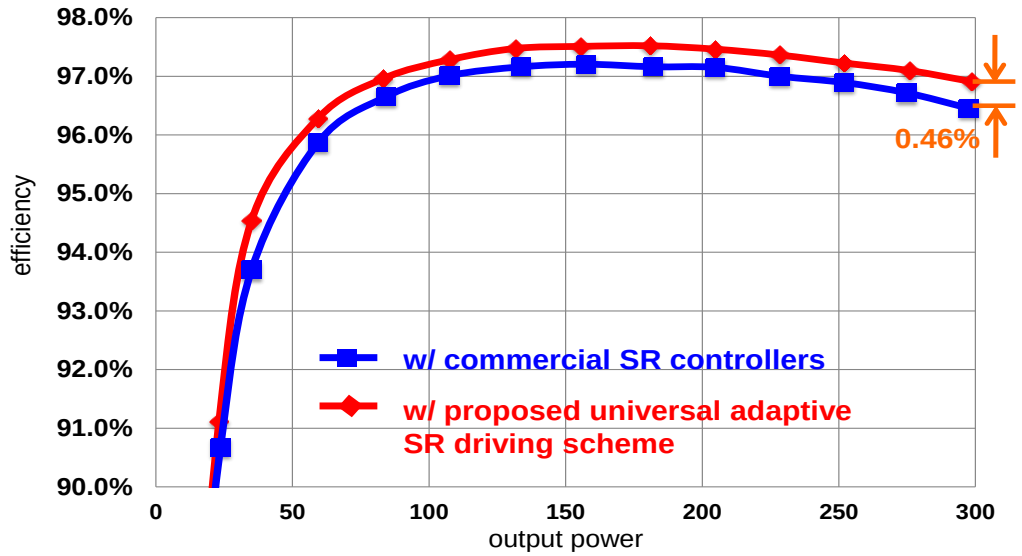


Fig. 6.20 Efficiency comparison with the commercial SR controllers

As analyzed in Section 6.2.2, when f_s decreases, there is no shoot-through concern. Thus the f_s increase transient is tested in Fig. 6.21. When f_s increases, the limitation (6.2) to the pulse width of the SR gate driving signal is active to prevent the shoot-through. Fig. 6.21 shows the waveforms when f_s increases from 500 kHz to 700 kHz in several switching cycles. After SR has been fully turned off, the drain to source voltage V_{dsSR} starts to build up slowly. ZCS is kept and no shoot-through is guaranteed even if f_s increases up to 700kHz.

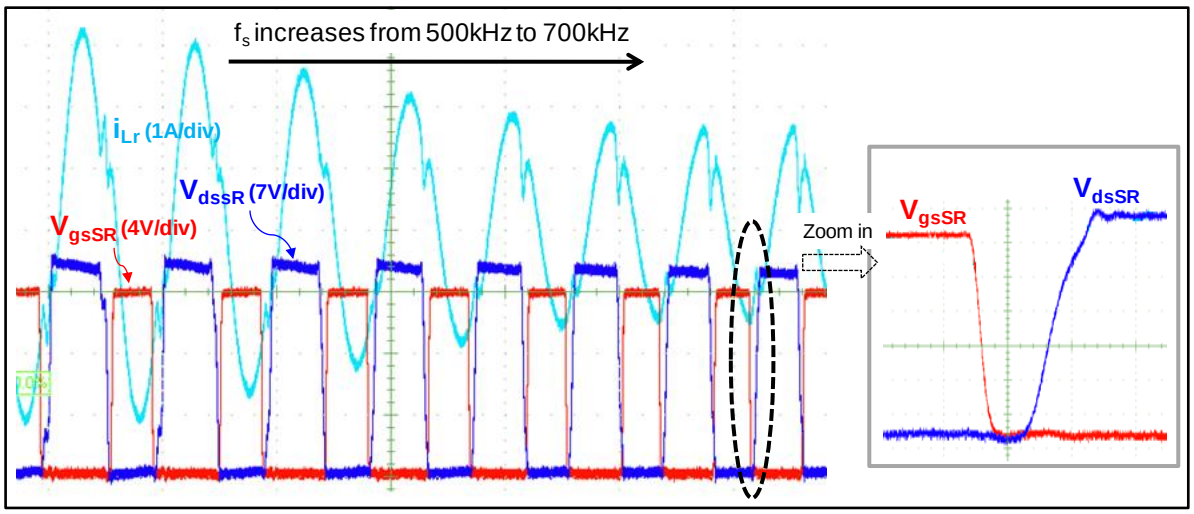


Fig. 6.21 Protection to avoid shoot-through when f_s increases quickly

6.3 Resonant Frequency Tracking based on SR Driving Signal

6.3.1 Pulse width locked loop (PWLL) for resonant frequency tracking

If the synchronous rectifier (SR) driving signals are tuned well, as the secondary side current i_{SEC} goes across zero, the SR should be turned off immediately, so it behaves like a "virtual current sensor". Thus, based on the well-tuned SR gate-driving signals, the resonant frequency f_0 can always be tracked.

With the universal adaptive SR driving scheme, the SR should be turned off when i_{SEC} crosses zero. Fig. 6.22 shows that when $f_s<f_0$, the SR should be turned off earlier than the main switch; that is, the pulse width of SR driving signal (T_2) is smaller than that of main switch (T_1) (i.e. $\Delta T=T_2-T_1<0$).

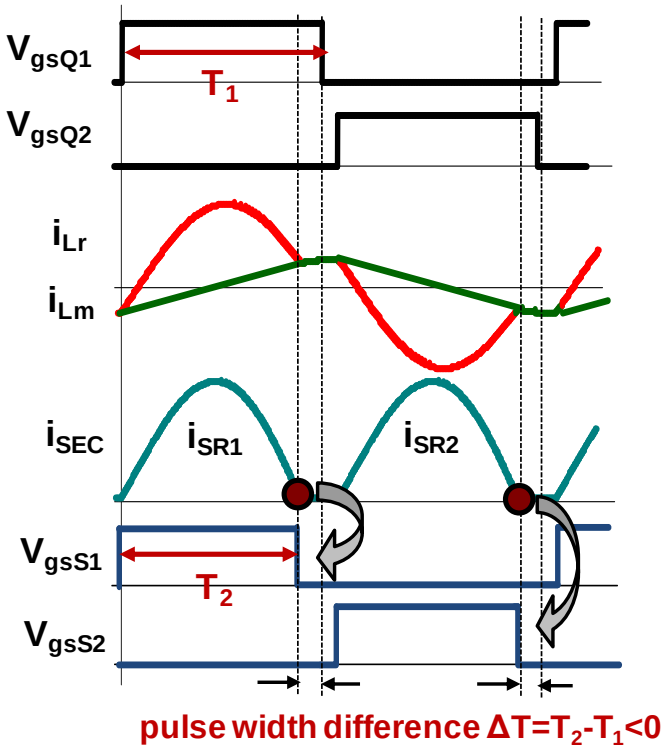


Fig. 6.22 Pulse width of the SR driving signal is smaller than the main switch when $f_s<f_0$

If $f_s>f_0$, Fig. 6.23 shows that the SR should be turned off a bit later than the main switch to conduct the sharply decreased current. This means that the pulse width of the SR driving signal (T_2) is larger than that of the main switch (T_1) (i.e. $\Delta T=T_2-T_1>0$).

When $f_s=f_0$, the well-tuned SR is turned off at the same time with the main switch shown in Fig. 6.24.

From Fig. 6.22 to Fig. 6.24, only when $f_s=f_0$, the pulse width of main switch driving signal T_1 is equal to that of SR T_2 (i.e. $\Delta T=0$). Therefore, by tuning the switch frequency f_s to minimize the pulse width difference between the main switch and the well-tuned SR gate-driving signal, the LLC resonant frequency point f_0 can always be tracked.

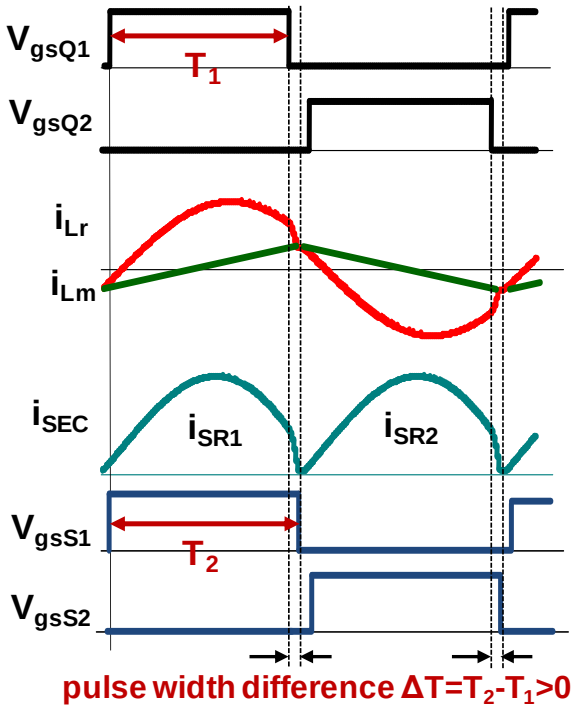


Fig. 6.23 Pulse width the SR driving signal is larger than the main switch when $f_s>f_0$

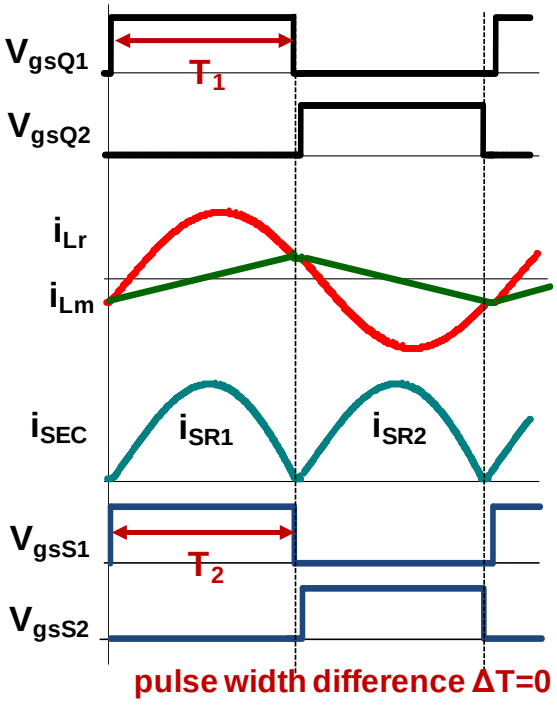


Fig. 6.24 Pulse width of the SR driving signal is the same as the main switch when $f_s=f_0$

Like the phase-locked loop (PLL), the resonant frequency is tracked by minimizing the phase difference. The proposed pulse-width locked loop (PWLL) is illustrated in Fig. 6.25, and is intended to minimize the pulse width difference between the main switch and the well-tuned SR driving signals. Thus, the LLC-DCX is always fixed to operate at the resonant frequency point ($f_s=f_0$).

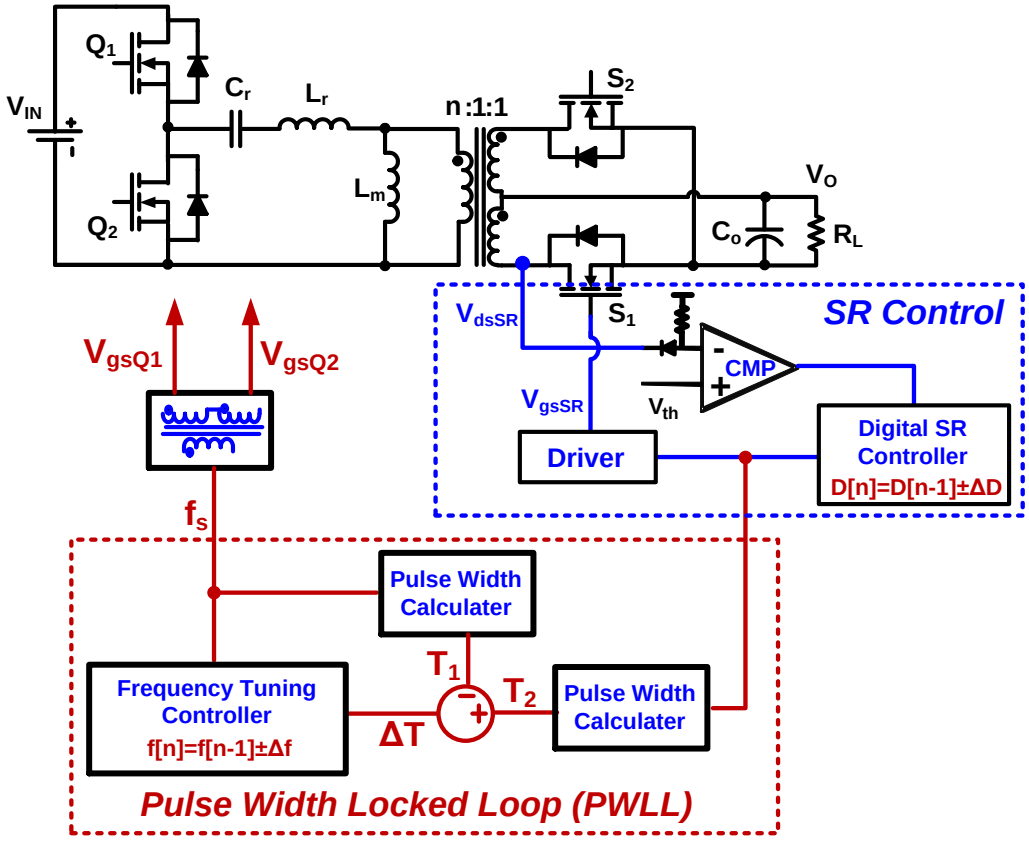


Fig. 6.25 Control block of f_0 tracking based on the SR gate-driving signal

Assuming the LLC initially operates within $f_s<f_0$ region, the pulse width of the SR driving signal is smaller than that of the main switch by ΔT as shown in Fig. 6.22 and Fig. 6.26. With the proposed f_0 tracking approach using PWLL, the switching frequency f_s will increase by Δf. Then at the new switching frequency point (i.e. f_s+ Δf), after the SR has been well tuned, if the pulse

width of the SR driving signal is still smaller than that of the main switch, f_s will increase by Δf again. Thus, f_s increases step by step to minimize the pulse width difference between the main switch and SR driving signals. Finally, f_s is tuned to be equal to f_0 when the main switch is turned off at the same time as SR, as shown in Fig. 6.26.

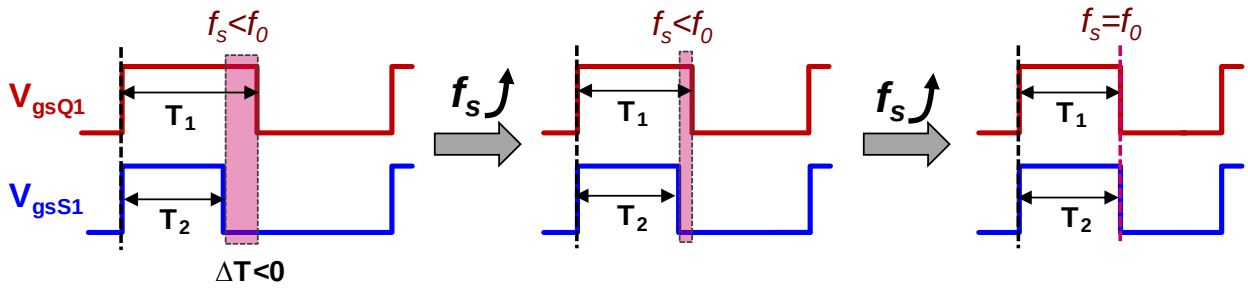


Fig. 6.26 F_0 tracking process (from $f_s<f_0$ to $f_s=f_0$)

Fig. 6.27 shows the tuning process from $f_s>f_0$ to $f_s=f_0$ with the same principle. Due to the tolerance, the LLC may initially operate within the $f_s>f_0$ region, where SR driving signal pulse width is a bit larger than the main switch. During the f_0 tracking process, the pulse-width difference is minimized by decreasing f_s step by step. Similarly, as the main switch turns off at the same time as SR, the switching frequency f_s is tuned to be f_0.

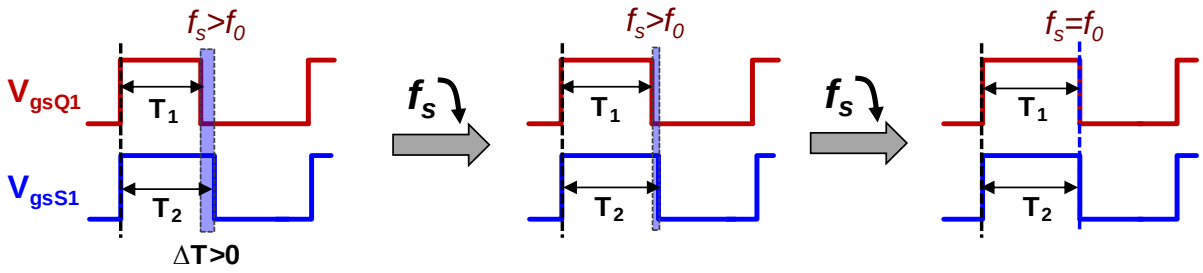


Fig. 6.27 F_0 tracking process (from $f_s>f_0$ to $f_s=f_0$)

Sum up, Fig. 6.28 shows the flowchart implemented in the digital logics.

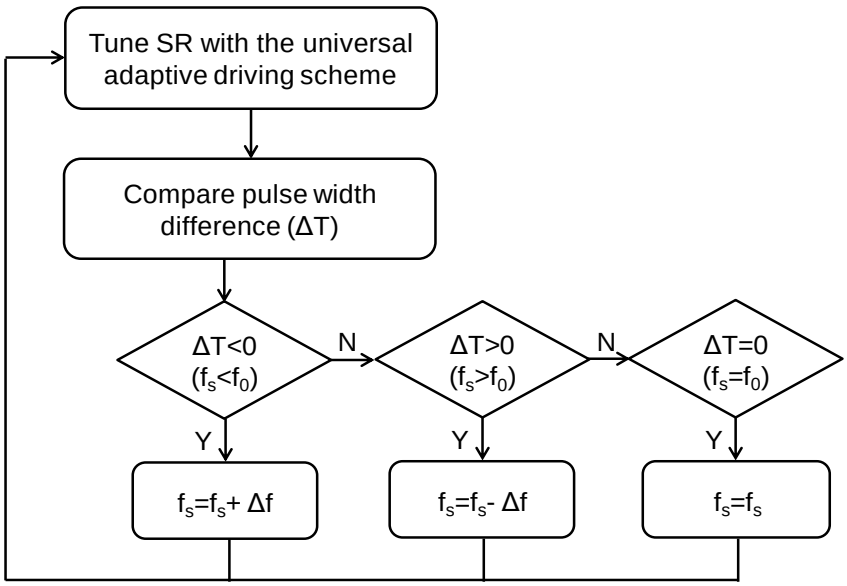


Fig. 6.28 Control flowchart of PWLL to track f_0

In Fig. 6.29, no matter what the initial switching frequency is, the PWLL will tune it converging to the resonant frequency point in a uni-direction. Therefore, the tuning process is always stable.

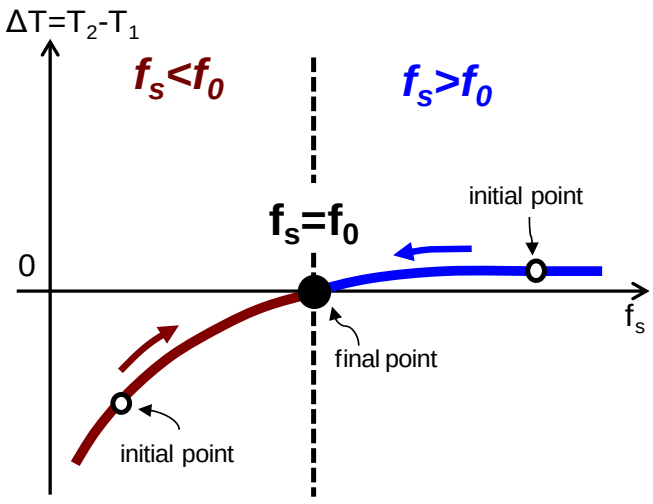


Fig. 6.29 Stable uni-direction tuning process of PWLL

After tuning with PWLL, the resonant frequency f_0 can be tracked quite well. Since f_0 is determined by the resonant components. During the load transient, f_0 does not vary, and the pulse width of the well-tuned SR gate driving signal keeps the same. Thus, PWLL can work normally, and there is no dynamic unstable crisis.

6.3.2 Experimental results

Initially, let the LLC-DCX run below or above the resonant frequency point. Fig. 6.30 shows that within the $f_s<f_0$ region (f_s=400 kHz), after the SR has been tuned well, the pulse width of the SR gate-driving signal is smaller than that of the main switch by ΔT_1. When $f_s>f_0$ (f_s=600 kHz), the SR will turn off a bit later than the main switch by ΔT_2, to let the sharply decreased current go through the SR, as shown in Fig. 6.31.

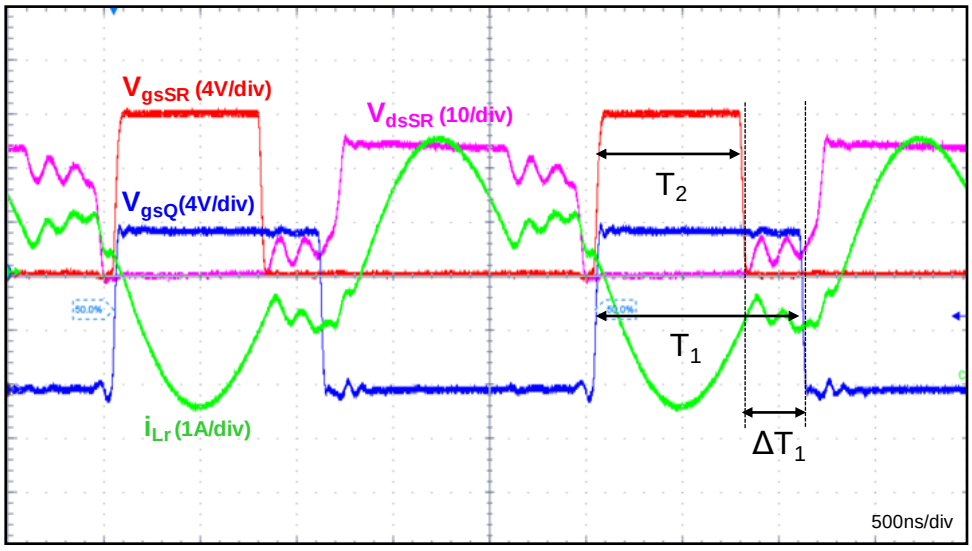


Fig. 6.30 Pulse width of SR driving signal is smaller than main switch when $f_s<f_0$

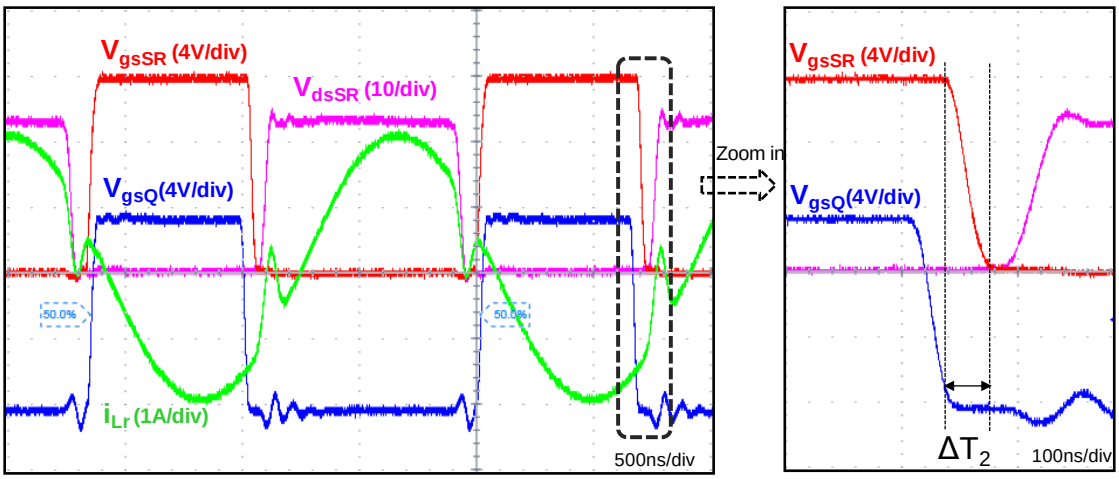


Fig. 6.31 Pulse width of SR driving signal is larger than main switch when $f_s > f_0$

After the SR gate-driving signal has been well tuned, the pulse-width locked loop (PWLL) takes over, to tune the switching frequency f_s by minimizing the pulse width difference between the main switch and the SR gate-driving signals. Fig. 6.32 shows that after tuning, the main switch turns off at the same time as the SR, and f_s is automatically tracked to be 530 kHz.

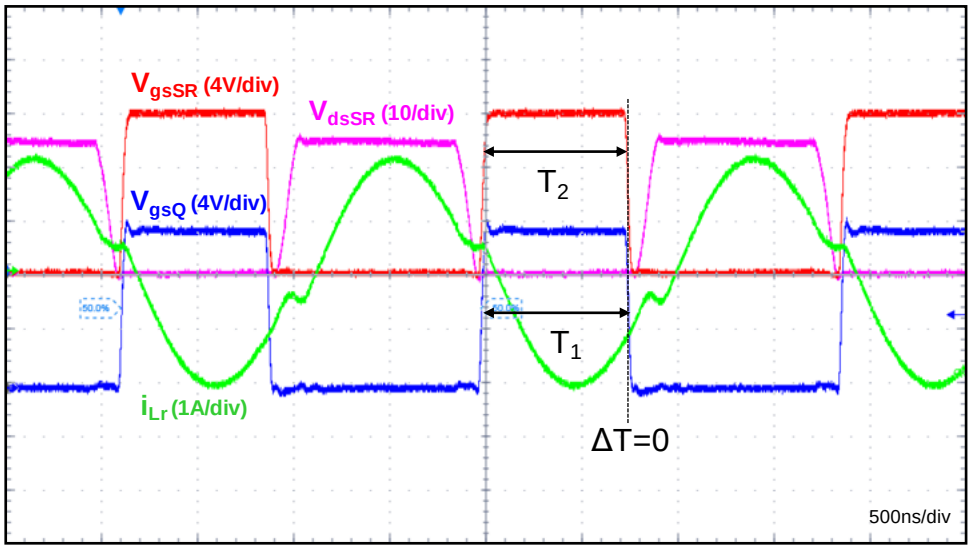


Fig. 6.32 Tracking $f_s=f_0$ by minimizing the pulse width difference between the main switch and the well-tuned SR gate-driving signals

Figure 6.33 verifies the resonant frequency tracking performance as the load changes. According to the sinusoid resonant current waveforms under all load conditions, the resonant frequency f_0 is tracked quite well.

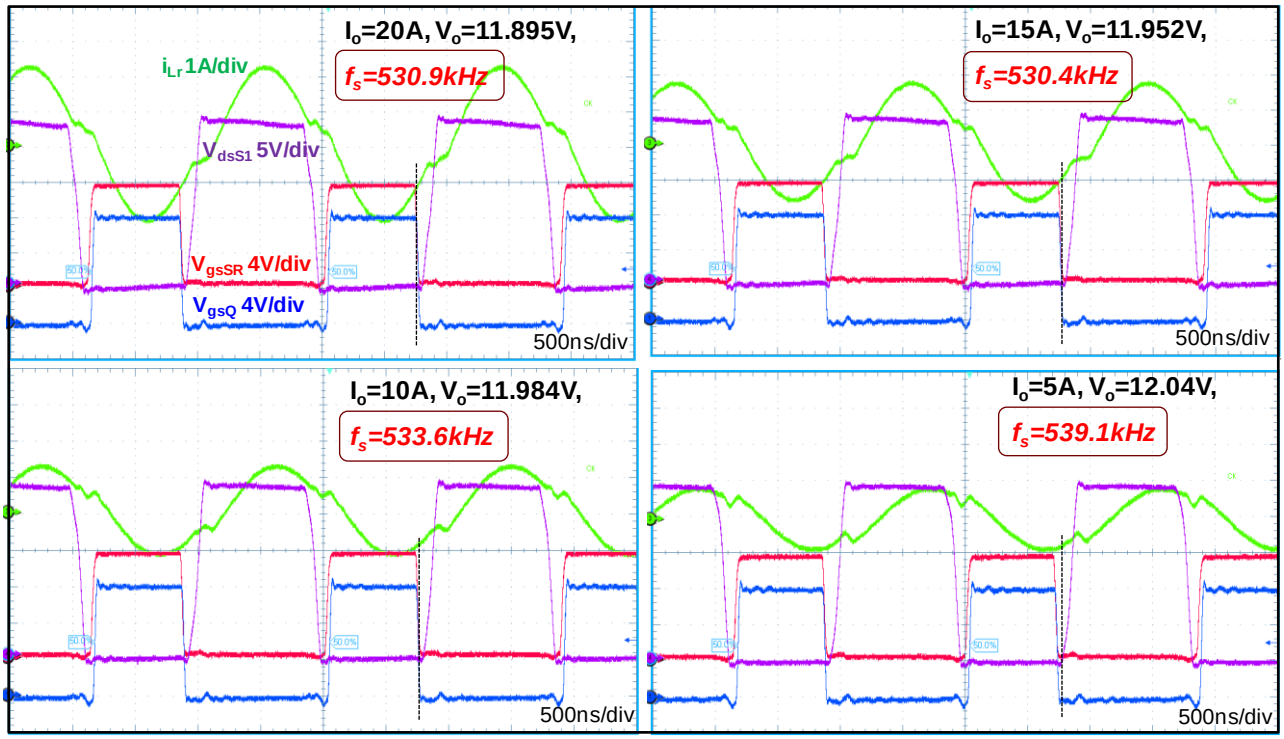


Fig. 6.33 F_0 is tracked well under different load conditions

Figure 6.34 verifies that during load transients, the PWLL can tack f_0 well. There is no dynamic unstable.

Figure 6.35 provides an efficiency comparison, where we see that the highest efficiency can be achieved by using the proposed PWLL resonant frequency tracking approach. This is thanks to the less conduction losses compared with Fig. 6.30 when operating below the f_0 point; as well as no reverse recovery and less switching losses compared with Fig. 6.31 when running above the f_0.

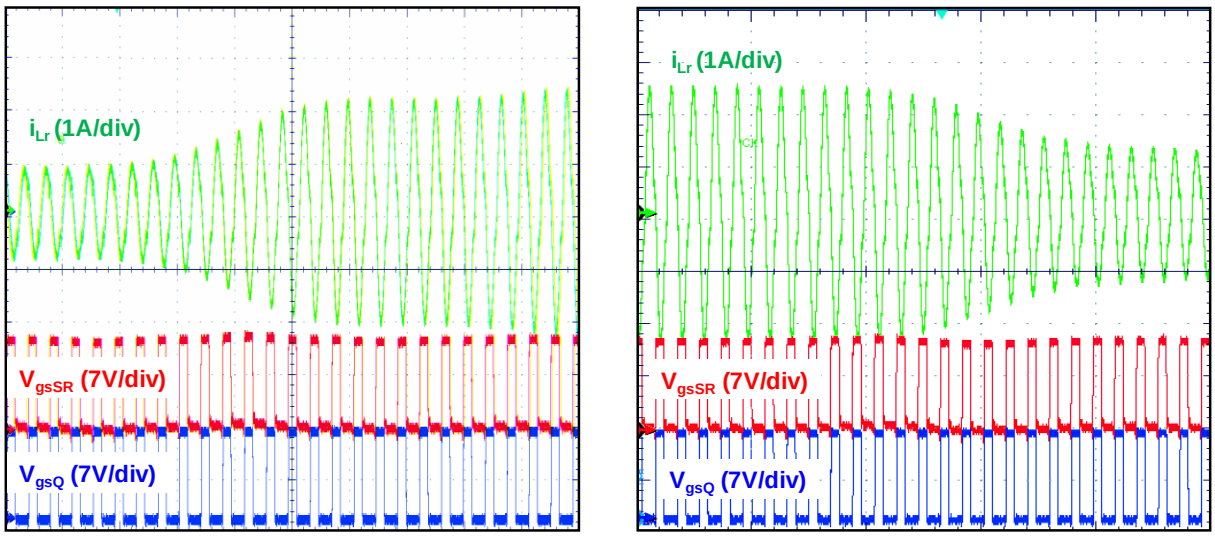


Fig. 6.34 F_0 tracking during load transients

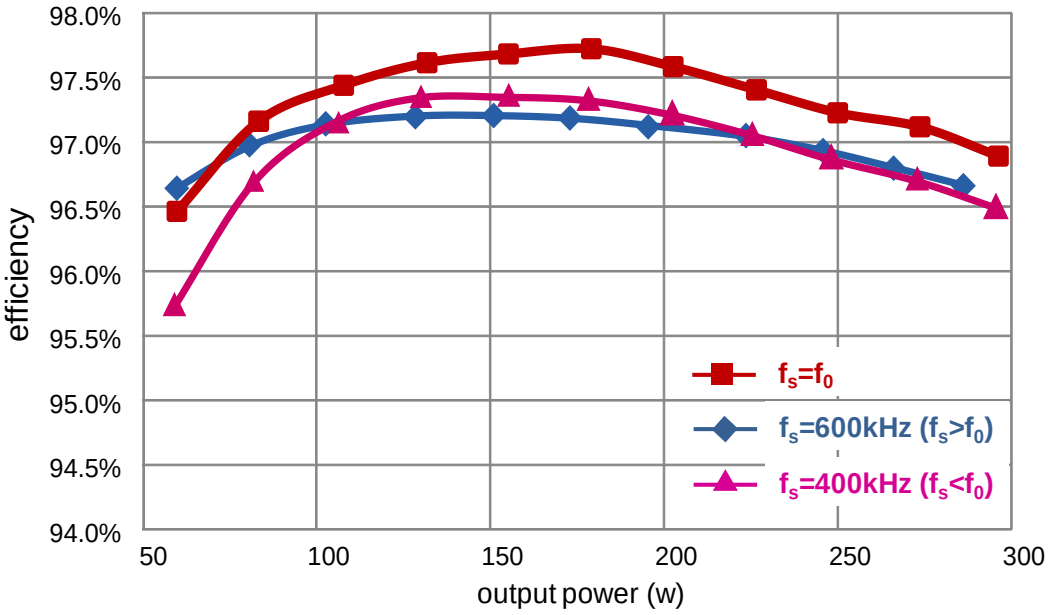


Fig. 6.35 Efficiency improvement with PWLL resonant frequency tracking

6.4 Conclusion

The universal adaptive SR driving scheme for LLC resonant converters is proposed and its digital implementation is experimentally verified in this chapter. By sensing the SR drain to source voltage and comparing with the threshold, the body diode conduction status is detected. The digital logic tunes the SR duty cycle to eliminate the body diode conduction in order to achieve the highest efficiency in all operating frequency regions. Finally, the protection is investigated to avoid shoot-through during the transient process. In addition, a novel switching frequency control scheme for the LLC-DCX is proposed. By setting the well-tuned SR gate-driving signal as the control reference and using the pulse-width locked loop (PWLL) to minimize the pulse width difference between the SR and the main switch driving signals, the resonant frequency is always tracked ($f_s=f_0$).

Chapter 7. Conclusion and Future Work

7.1 Conclusion

The LLC resonant converter exhibits higher efficiency and higher power density than conventional PWM converters. Thus, it has been widely adopted as a desirable power supply for telecoms, servers, desktops, laptops, flat-panel TVs, LED lighting, etc. To further improve the LLC performance, several novel concepts and techniques have been developed in this dissertation.

In the beginning, the two-dimension (2D) state-plane trajectory analysis is proposed for the LLC resonant converter. All the resonant tank information such as the resonant capacitor voltage v_{Cr}, the resonant inductor current i_{Lr}, and the magnetizing inductor current i_{Lm} are clearly presented in the state plane. The steady-state trajectories within the whole operation range are described. The dynamic trajectories during the load transient, start-up and the burst operation are illustrated as well.

Next, to improve the load transient response, a simplified optimal trajectory control (SOTC) for the LLC resonant converter is proposed. Near the steady state, a linear compensator like PI and PID is used, controlling the switching frequency to eliminate the steady-state error. During load transients, the optimal trajectory control (OTC) takes over, tuning the pulse widths of the gate driving signals based on the sensed load current. Using the state plane analysis, the pulse widths are calculated, letting the state variables track the desired trajectory within the minimal

period of time. It features simple implementation, dramatic improvement in load-step response and easy integration with existing analog controllers.

After that, an optimal process for LLC soft start-up and over-load protection is presented based on a graphical state-trajectory analysis. To settle the initial condition, the unsymmetrical-band approach, slop-band control, and one-cycle control are investigated. Then, by sensing the output voltage, the optimal frequency is calculated within a predetermined current limitation band. Therefore, the resonant current and voltage stress is well limited during these highly dynamic processes.

Furthermore, to improve the LLC light-load efficiency, a three-pulse optimal switching pattern is proposed to achieve the best light-load efficiency and minimal output voltage ripple. The burst on-time is maintained, but the burst off-time is modulated by the light load conditions. Based on the state-plane trajectory, during the burst on-time, the first switching pulse width is optimized to settle to the steady state of the highest efficiency load condition in one-pulse time. And the next two pulses operate at the resonant frequency point to follow the steady-state trajectory of the highest efficiency load. With the proposed burst mode, under all light loads, the LLC equivalently operates under the steady state of the best efficiency load condition. Thus, high light-load efficiency can be ensured.

For PWM dimming of LLC resonant LED driver, two optimal switching patterns are proposed. One is tuning the first-pulse width during the PWM dimming on-time. Thus, the full-load steady state can be tracked within one-pulse time. Another one is tuning the last-pulse width, which will change the initial condition as the next PWM dimming cycle starts. Both of these will

eliminate the dynamic oscillations in the resonant tank. Thus, flat output current can be achieved. The efficiency stays high and flat from the full-load point. Under low dimming conditions, the LED intensity can be controlled more precisely

Finally, a universal adaptive SR driving scheme is proposed and its digital implementation is experimentally verified. By sensing the SR drain to source voltage and comparing with the threshold, the body diode conduction status is detected. The digital logic tunes the SR duty cycle to eliminate the body diode conduction to achieve good efficiency. After that, the protection is investigated to avoid shoot-through during the transient processes. In addition, by setting the well-tuned SR gate-driving signal as the control reference, a novel resonant frequency tracking scheme is proposed for the unregulated LLC (LLC-DCX). Using the pulse-width locked loop (PWLL) to minimize the pulse width difference between the SR and the main switch driving signals, the resonant frequency of LLC-DCX is always tracked ($f_s=f_0$).

7.2 Future Work

All of these novel implementations proposed in this work will improve the LLC dynamic responses and overall efficiency. Following this research, there are still some remaining works can be done:

1. The proposed simplified optimal trajectory control (SOTC) can significantly improve the load transient response. However, the load current needs to be sensed precisely to determine the optimal pulse widths, which is difficult to be implemented. Some voltage sensing approaches reflecting the load condition needs to be investigated to further simplify its implementation.

2. Like the load transient response, the LLC dynamic response with the input voltage variation can to be analyzed and improved based the graphic state-plane in the future. During the holdup time operation, the input voltage decreases. The LLC state trajectory can be analyzed to determine the holdup capability with different resonant tank parameters.

3. The loss distribution under the burst mode should be investigated. Thus, the theoretical boundary between the normal operation mode and the burst mode can be determined.

4. All the improvements proposed in this work can be integrated in one universal controller such as FPGA and DSP in the future.

5. The 2D state-plane analysis approach for the LLC resonant converter can be extended to other multi-element resonant converters like LCL, CLL, etc.

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A. Background & Introduction

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