Electrical and Thermal Characterizations of IGBT Module with Pressure-Free Large-Area Sintered Joints

by

Li Jiang

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Khai D.T. Ngo (Chair)

Guo-Quan Lu (Co-Chair)

Louis J. Guido

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Abstract

Silver sintering technology has received considerable attention in recent years because it has the potential to be a suitable interconnection material for high-temperature power electronic packaging, such as high melting temperature, high electrical and thermal conductivity, and excellent mechanical reliability. However, pressure (usually between three to five MPa) was added during the sintering stage for attaching power chips with areas larger than 100 mm^2. This extra pressure increased the complexity of the sintering process. The maximum chip size processed by pressure-free sintering was 6 × 6 mm^2, as reported in the literature. One objective of this work was to achieve chip-attachment with an area of 13.5 × 13.5 mm^2 (a chip size of one kind of commercial IGBT) by pressure-free sintering of nanosilver paste. Another objective was to fabricate high-power (1200 V and 150 A) multi-chip modules by pressure-free sintering. In each module (half-bridge), two IGBT dies (13.5 × 13.5 mm^2) and two diode dies (10 × 10 mm^2) were attached to a DBC substrate. Modules with solder joints (SN100C) and pressure-sintered silver joints were also fabricated as the control group. The peak temperature in the process for pressure-free silver sintering was about 260^oC, whereas that for vacuum reflowing of solder was 270^oC and that for pressure-sintering (three MPa) of silver was 280^oC. The details of processes for wire bonding, lead-frame attachment, and thermocouple attachment are also stated in this thesis.

Modules with the above three kinds of joints were first characterized by electrical methods. All of the modules could block 1200 V DC voltage after packaging, which is the voltage rating of bare dies. Modules were also tested up to the rated current (150 A)

and half of the rated voltage (600 V), the test conditions in the datasheets for commercial modules with the same voltage and current ratings. The I-V characteristics of the packaged devices were similar (on-resistance less than 0.5 mΩ). All switching waveforms at the transient stage (both turn-on and turn-off) were clean. Six switching parameters (turn-on delay, rise time, turn-off delay, fall time, turn-on loss, and turn-off loss) were measured, which were also similar (<9%) among the different kinds of modules. The results from electrical characterizations showed that both static characterizations and double-pulse test cannot be used for evaluating the differences between chip-attach layers.

Thermal characterizations were also performed for all the modules. Transient thermal impedances were measured by gate-emitter signals. Two setups for thermal impedance measurements were used. In one setup, the bottoms of the modules were left in the air, and in the other setup, the bottoms of the modules were attached to a chiller (liquid cooling and temperature controlled at 25^{o}C) with thermal grease. The thermal impedances of all the modules were still increasing after 40 seconds for the measurements without chiller, since the thermal resistance of heat convection from the bottom copper to the air was included, which was much higher than the sum of the thermal resistances of the previous layers (from the IGBT junction, through the chip-attach layer, to the bottom of the DBC substrate). In contrast, the thermal impedances became almost stable (less than 3% variation) after 15 seconds for all the modules when the chiller was used. Among these three kinds of modules, the module with pressure-sintered joints had the lowest thermal impedance and a thermal resistance (measured with the chiller) of about 0.609^{o}K/W. In contrast, the thermal resistance was about 0.964^{o}K/W for the soldered module, and 2.30^{o}K/W for the pressure-free-sintered module.

In summary, pressure-free large-area sintered joints were achieved and passed the fabrication process for IGBT half-bridge module with wiring bonding. Packaged devices with these kinds of joints were verified with good electrical performance. However, thermal performances of pressure-free joints were worse than solder joints and pressure-sintered joints.

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Chapter 1. INTRODUCTION

In the future electronic industry, such as automobile, naval ship, aircraft, electric power, and deep-well drilling, an extreme demand for every-increasing power density is placed on power electronics [1]. To achieve this objective, high requirements are placed on both the power electronic devices and the electronic packaging.

Power devices able to operating at junction temperatures higher than 175°C have received considerable attention. Focuses were set on wide-band-gap semiconductor devices, such as silicon carbide (SiC) and gallium nitride (GaN). The potential advantages of these wide-band-gap devices include higher achievable junction temperatures and thinner drift regions (because of the associated higher critical electric field values) that can result in much lower on-resistance than is possible in Si [2]. For example, SiC's large band-gap allows higher temperature operation and radiation resistance, as well as much higher thermal conductivity, which in turn allows more efficient heat transfer than most semiconductors in use [3]. Table I summarizes the characteristics of several typical wide-band-gap semiconductors.

TABLE I

CHARACTERISTICS OF WIDE-BAND-GAP SEMICONDUCTORS AT 300°K

([4] V. R. Manikam and K. Y. Cheong, "Die Attach Materials for High Temperature Applications: A Review," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 4, pp. 457–478, Apr. 2011.)

Semiconductor Material	Band-Gap (eV)	Thermal Conductivity (W/cm·°K)	CTE (ppm/°K)	Maximum Operating Temperature (°C)
Si	1.1	1.3	2.6	150
GaAs	1.43	0.55	5.73	350
4H-SiC	3.26	7	5.12	750
GaN	3.44	1.1	5.4 to 7.2	>700
Diamond	5.48	6 to 20	0.8	1100

The progress of technologies for wide-band-gap device makes it possible to place electronics in extremely hazardous environments without elaborate enclosures or heavy thermal management systems. However, the packaging supporting such wide-band-gap devices is inadequate in electrical interconnection, thermal management, and thermo-mechanical reliability in high-temperature operation environments. Several systems must accept severe mass penalties required by coolant systems to maintain electronic temperatures below critical levels. High-temperature packaging technologies and design methodologies are therefore becoming a necessity because they are essential to realizing high performance and high reliability in electronic systems [5].

Therefore, chip-attach materials, which connect devices to the rest of the system, play an important role to ensure the consistent operation of the entire system.

1.1. Review of Chip-Attach Techniques

1.1.1. Soldering

Solders are alloys of two or more metals. When these metals are alloyed together, the melting point of the alloy can be considerably lower than the melting point of either of the individual metals. It is commonly accepted that both tin-based solder alloys (leaded [SnPb] and lead-free solder alloys [SnAgCu]) are used widely as chip-attach materials because of their ease of processing at temperatures below 573^{o}K (300^{o}C) [6]. A typical temperature profile is shown in Figure 1 [1].

However, in high temperature applications (>623^{o}K (350^{o}C)) in automotive, down-hole oil and petroleum industry for well logging, aircraft, space exploration, nuclear environment, and radars, these solder alloys and conductive adhesives cannot meet their stringent requirements, and one of the obvious drawbacks is their low melting and operating temperatures [7].

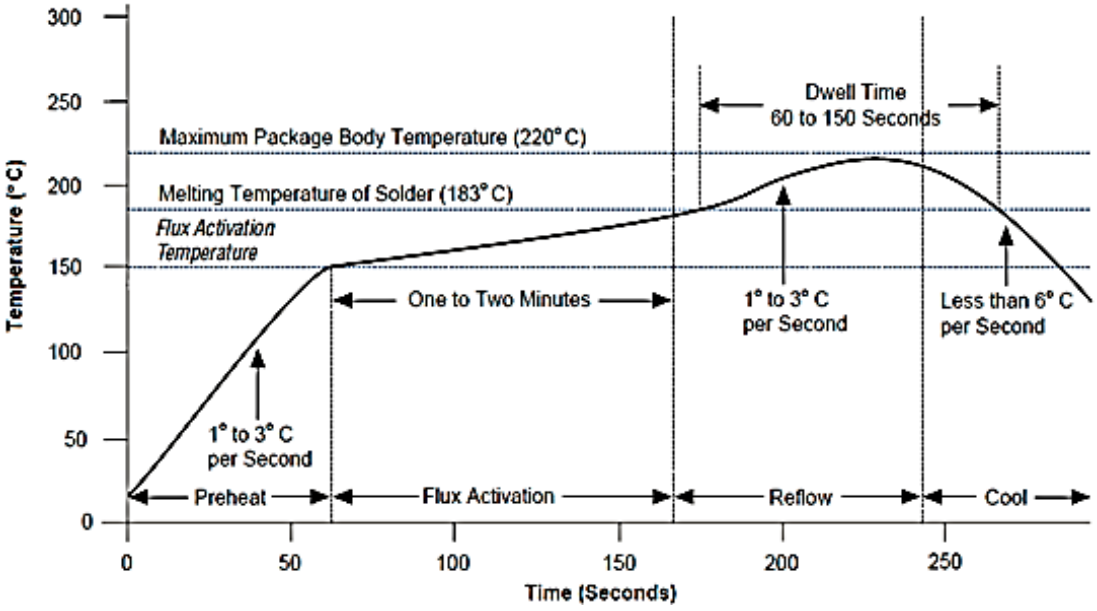

Figure 1. Temperature profile for eutectic solders (Sn63Pb37) ([1]. W.D. Brown and R. K. Ulrich, *Advanced Electronic Packaging with Emphasis on Multichip Modules*, IEEE Press, 2006.) Used under fair use, 2013.

1.1.2. Diffusion Bonding (Transient Liquid Phase)

TLP bonding addresses challenges for high temperature applications by synergistically combining soldering and diffusion bonding. It has a re-melting temperature dramatically higher than its process temperature and requires a bonding pressure (lower than a few hundreds of kilopascals) that is an order of magnitude smaller than that of nanosilver sintering. Therefore, TLP bonding is a promising solution for high-temperature-operation power electronics.

Because of the advantages listed above, TLP bonding of power devices, using Au-In, Ag-In, Ag-Sn, or Cu-Sn, was reported. However, even with their advantages, every listed TLP material has its deficiencies. Au-In is the most expensive (high Ag content) and the most susceptible to oxidation (of indium) among the TLP materials. Ag-Sn also suffers from high material cost. Cu-Sn has a complex phase transition and forms multiple intermetallic compounds and a non-homogenous bonding interface, although it does have high thermal conductivity and electrical conductivity.

Nickel-tin (Ni-Sn) TLP bonding has advantages over other TLP materials. Ni–Sn TLP bonding is cost effective and compatible with manufacturing because both Ni and Sn are commonly used in conventional power electronics and the market prices of Ni and Sn are relatively low. Also, the high re-melting temperature of Ni–Sn TLP material (theoretically 794◦C) enables reliable high-temperature operation. Figure 2 illustrates a conceptual view of the Ni–Sn TLP bonding process [8].

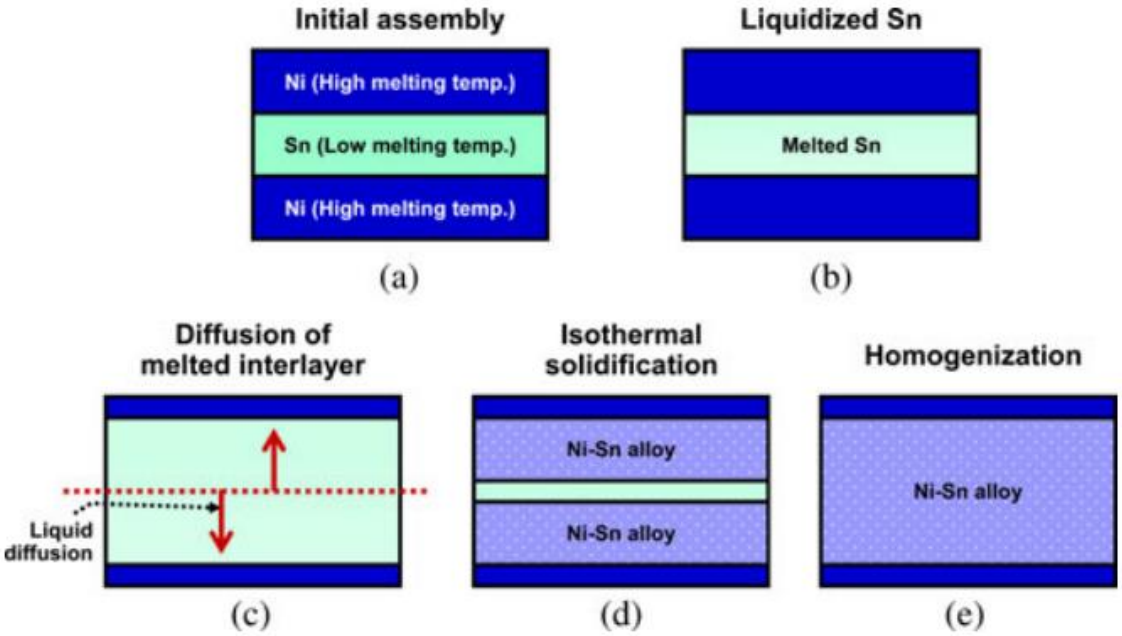

Figure 2. Conceptual views of Ni–Sn TLP bonding process. ([8] S. W. Yoon, K. Shiozaki, S. Yasuda, and M. D. Glover, "Highly reliable nickel-tin transient liquid phase bonding technology for high temperature operational power electronics in electrified vehicles," in *Proc. Appl. Power Electron. Conf. Expo.,* Orlando, FL, Feb. 2012, pp. 478–482.) Used under fair use, 2013.

1.1.3. Silver Sintering

Sintered silver is a lead-free chip-attach material that can substitute for solder alloys and conductive epoxies for packaging power semiconductor devices, especially in high-temperature applications [9]. Sintered silver joints with porous structure have good ductility and low Young's modulus (50-55 MPa for a porosity of 12%-15% [10]) to resist the degradation from thermo-mechanical stresses. The high melting point of silver, 961^{o}C

[11], is much higher than that of any solder (TABLE II), indicating that the sintered joint can operate at a much lower homologous temperature [12], with low inelastic deformation or accumulation of damages during thermal or power cycling.

TABLE II

VARIOUS CHIP-ATTACH MATERIALS, THEIR PROPERTIES

([11] T. G. Lei, J. N. Calata, S. Luo, X. Chen, and G.-Q. Lu, "Low temperature sintering of nano-scale silver paste for attaching large-area (>100 mm2) chips," *IEEE Trans. Comp. Packag. Technol.*, vol. 33, no. 1, pp. 98–104, Mar. 2010.)

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Feature / Material	Processing temperature	Max. use temperature	Electrical conductivity 10^5 $(\Omega\text{-cm})^{-1}$	Thermal conductivity (W/°K-cm)	Die-shear Strength (MPa)	Price ($/gm)
Lead-tin solder	217°C	< 183°C	0.69	0.51	35	< 1.0
Lead-free solder	260°C	< 225°C	0.75	0.70	35	< 1.0
Gold-tin solder	310°C	< 280°C	0.625	0.58	30 - 60	50 – 80
Silver epoxy	100 – 200°C	< 200°C	0.1	0.1	10 - 40	2 – 9
Sintered nano-Ag	< 260°C	< 961°C*	3.8	2.4	20 – 40	competitive

As the mechanical properties of chip-attach materials deteriorate in harsh environments, a safety margin should be kept between the operating temperature and the melting point of the joints. This margin is defined by the so-called homologous temperature, the ratio of operating temperature to melting temperature, both temperatures expressed in kelvin. The homologous temperature should not exceed 0.8, since the mechanical properties of the joint degrade drastically beyond that point [12]. However, even at the threshold of 0.8, as the operating temperature increases, a soldering alloy with a much higher melting point is required; e.g., for an operating temperature of 200°C (473°K), a melting point of 318°C (473/0.8 = 591°K) is needed.

TABLE **III** shows the homologous temperatures of typical lead-free solder, AuGe(3) solder, and sintered silver.

Sintered-silver joints, even with porous structure, have much higher electrical conductivity and thermal conductivity (about 2.6×10^5 Ω·cm and 2 W/^{o}K·cm, respectively, for the sintered nanosilver from NBE Tech [13]) than do the soldered-alloy joints [14] that are currently used for attaching power devices.

TABLE III

HOMOLOGOUS TEMPERATURE OF VARIOUS CHIP-ATTACH MATERIALS

([12] J. Lutz, H. Schlangenotto, *Semiconductor Power Devices: Physics, Characteristics, Reliability*, Springer, 2008.)

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Material	Unit	SnAg(3.5)	AuGe(3)	Sintered Ag
Melting temperature	^{o}K	494	636	1234
Homologous temperature* at 150^{o}C	%	86	67	34
* <40% Considered mechanically stable 40%-60% Creep range, sensitive to strain >60% Unable to bear engineering loads				

1.2. Review of Silver-Sintering Techniques

To achieve sintering of silver particles at low temperatures, two methods are widely used. One is to apply quasi-static pressure, and the other is to reduce the size of the silver nanoparticles [15]. There are trade-offs between these two methods. Using high pressure places critical demands on the flatness of substrate, and the thickness of the chips. Reducing the particle size, on the other hand, makes the fabrication of silver paste complex, especially for particles at the nanoscale. A typical process for making nanoscale silver paste is shown in Figure 3 [1]. Owing to the demand for high power density, chip attachment of large chips (>100 mm^2) is necessary [16]. However, with the increase of the die size of power semiconductor devices, the thermo-mechanical stress in the chip-attach layer keeps increasing. The chip-attach layer becomes more vulnerable to

temperature cycling than the bond wire [10]. To make joints reliable and process easy, the two methods to lower the sintering temperature of silver are often used together for the chip attachment of large chips (>100 mm^2) [17].

The mechanical properties of pressure-sintered silver joints, compared with those of solder, are reviewed in Section 1.2.1. The review focuses on the chip attachment of large chips (>50 mm^2). The performance of pressure-free sintered silver for attaching small chips (<25 mm^2) and the recent progress of pressure-free-sintered silver for attaching large chips are reviewed in Section 1.2.2. The motivation and objectives of this work are stated in Section 1.3.

Figure 3. Preparation procedure of nanoscale silver paste. ([5] G. Q. Lu, J. N. Calata, Z. Zhang, and J. G. Bai, "A lead-free, low temperature sintering die-attach technique for high-performance and high-temperature packaging," in *Proc. 6th IEEE CPMT High Density Microsys. Design Packag. Comp. Failure Anal. (HDP'04)*, pp. 42–46, 2004.) Used under fair use, 2013.

1.2.1. Pressure Sintering of Silver

At early stage of the silver-sintering technique, a high pressure (>40 MPa) was used to lower the sintering temperature of existing thick-film silver pastes to lower than 300°C [15]. By using nanosilver paste, the pressure was greatly reduced.

In Knoeer's work, the die-shear strengths of 10 mm × 10 mm sintered-silver joints (five MPa and 275°C) were compared with those of 10 mm × 10 mm soldered joints without any thermal or power cycling [18]. The die-shear strengths of the soldered and

sintered samples are within the range 40 - 60 MPa, except for high-lead solder, as shown in Figure 4.

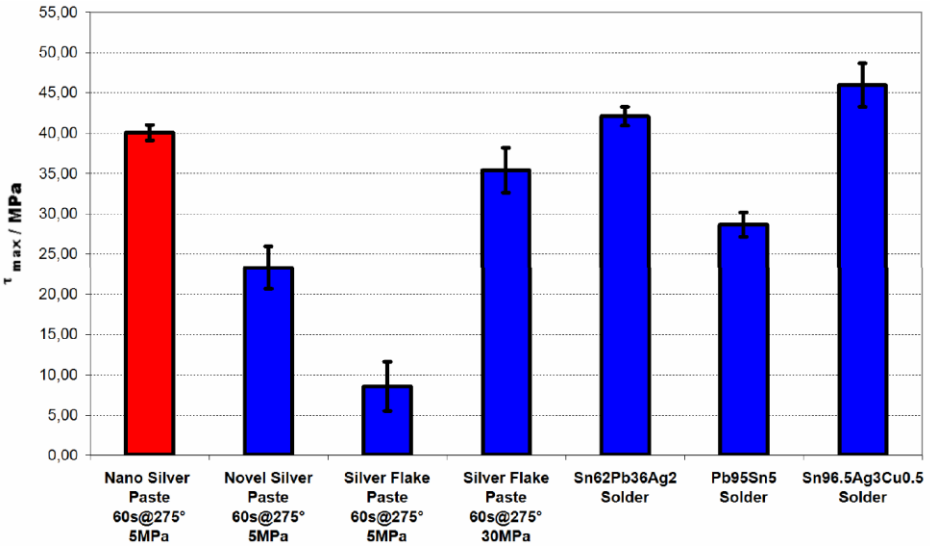


Figure 4. Shear strengths of different interconnection technologies. ([18] M. Knoerr and A. Schletz, "Power semiconductor joining through sintering of silver nanoparticles: Evaluation of influence of parameters time, temperature and pressure on density, strength and reliability," in *Proc. Int. Conf. Integr. Power Electron. Syst.*, Nuremberg, Germany, pp. 1–6, Mar. 2010.) Used under fair use, 2013.

Knower also found that the sintered-silver joints were more reliable, after either thermal cycling (Figure 5) or power cycling, than SAC305 for attaching 7.8 mm × 7.8 mm chips [19]. The lifetime data were evaluated by applying Weibull-statistics. The probability function F was fitted to the cycles to failure N_f.

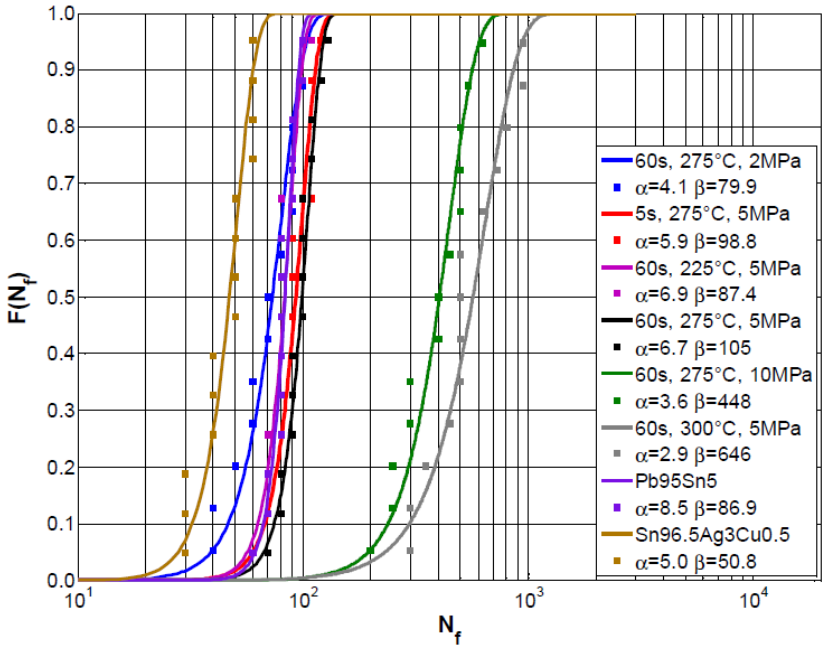


Figure 5. Probability functions for different interconnection technologies with thermal cycling tests between -55°C and +175°C (ΔT=230°K). ([19] M. Knoerr, S. Kraft, and A. Schletz, "Reliability assessment of sintered nano-silver die attachment for power semiconductors," in *Proc. 12th Electron. Packag. Technol. Conf.*, Singapore, pp. 56–61, 2010.) Used under fair use, 2013.

In Jiang's work [20], crack propagations are found in the soldered joints (copper substrates) after 800 cycles (from −40°C to +125°C), as shown in Figure 6. The sintered-silver joint is still intact after the same number of cycles, confirming the higher reliability of silver joints than that of lead-free solders for attaching large chips.

The above results confirmed that the pressure-sintered silver joints (<5 MPa) are more reliable than lead-free solder joints for attaching large chips (>50 mm^2).

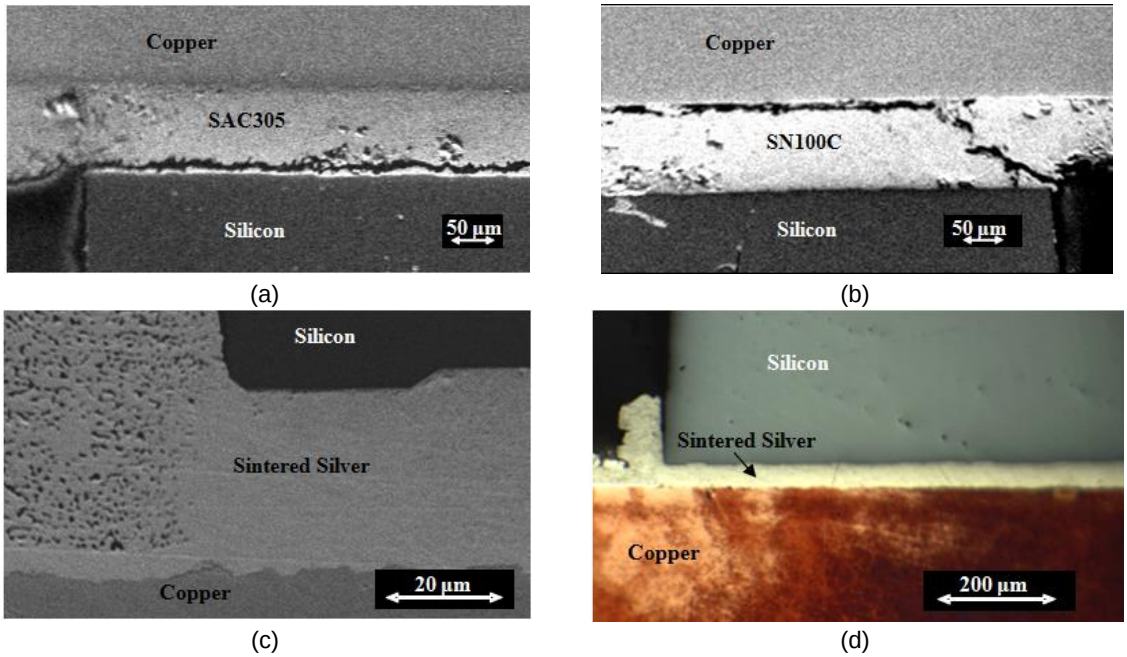


Figure 6. Cross sections of copper samples after 800 cycles for (a) cracked SAC305 soldered joint, (b) cracked SN100C soldered joint, and (c) intact sintered-silver joint, and (d) intact sintered-silver joint under low magnification. ([20] L. Jiang, "Thermo-mechanical reliability of sintered-silver joint versus lead-free solder for attaching large-area devices," M.S. thesis, Dept. Mater. Sci. Eng., Virginia Tech., Blacksburg, 2010.) Used under fair use, 2013.

1.2.2. Pressure-Free Sintering of Silver

By the measurement of thermal impedance, Cao [21] showed that the degradation of sintered-silver joints after thermal cycling was lower than that of two kinds of lead-free solder joints (SN100C and SAC305) for attaching 3.5 mm × 5.5 mm chips as in Figure 7. In his work, nanoscale silver paste was processed without any pressure.

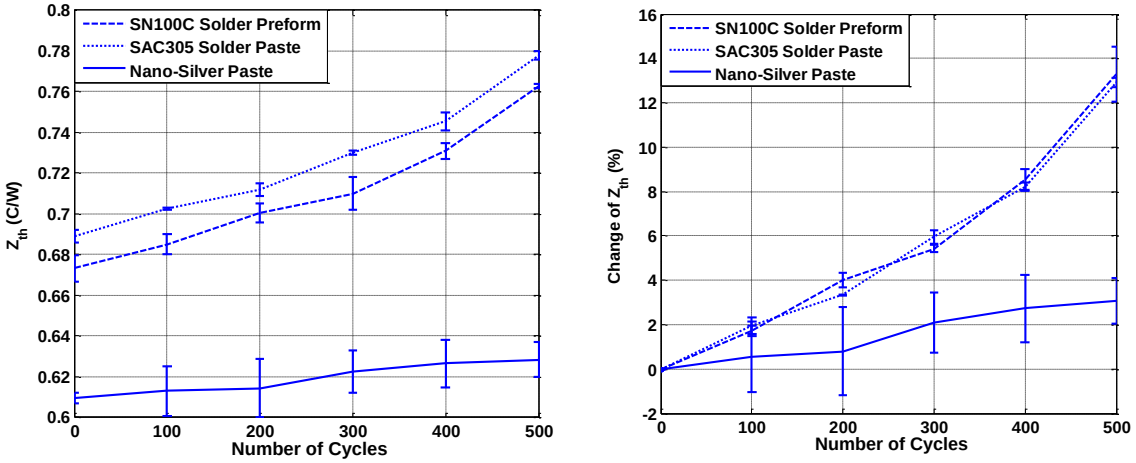


Figure 7. (a) Change of thermal impedance and the (b) percentage change of thermal impedance for samples with different chip-attach materials after 500 cycles (−40°C to +125°C). ([21] X. Cao, T. Wang, K. D. T. Ngo, and G.-Q. Lu, "Characterization of lead-free solder and sintered nano-silver die-attach layers using thermal impedance," *IEEE Trans. Compon. Packag. Manuf. Technol.*, vol. 1, no. 4, pp. 495–501, Apr. 2011.) Used under fair use, 2013.

Recently, other options of silver paste are also available: the mAgic paste from Heraeus [22], SSP-2000 from Henkel Corporation [23], and Alpha Argomax from Cookson Electronics [24]. Henkel claims that pressure-free sintering can be achieved with SSP-2000, without stating the corresponding size of the chip.

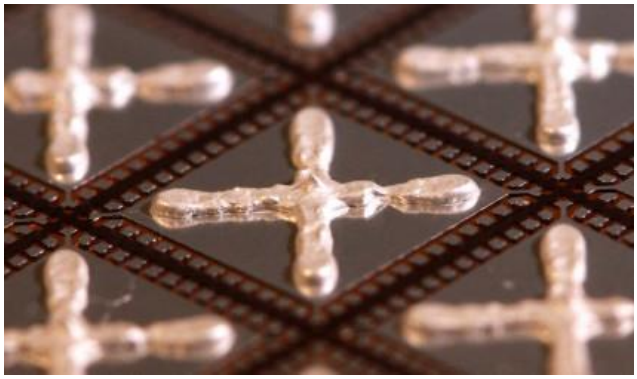


Figure 8. Pressure-free silver sintering technology from Henkel SSP-2000. ([23] Henkel. (2013). *Company Website* [online]. Available: http://www.henkel.com) Used under fair use, 2013.

The maximum chip size for chip-attachment according to Henkel is 6 × 6 mm^2. The silver paste (SSP-2000) shown in Figure 8 is printed in an X-pattern. This pattern actually generates interest for printing paste form of chip-attach materials, as introduced in Lee's

work [25]. The special pattern may be good for achieving pressure-free sintering, since the X-pattern assists the outgassing of binder during the sintering.

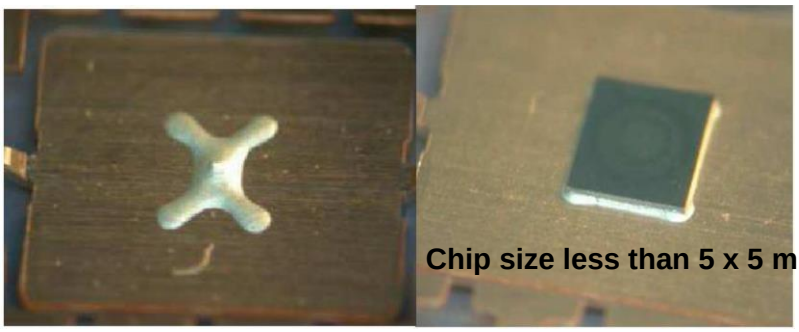


Figure 9. Silver epoxy X-pattern dispensed by writing, and fillet coverage along the die edges. ([25] M, Lee et al., "The squeezing process of complex epoxy patterns in the die-attaching of large IC-chip," *Int. Conf. Integr. Power Electron.*, pp.1- 8, 2006.) Used under fair use, 2013.

Pressure-free sintering of silver nanoparticles to silver substrate is also mentioned in Durairaj's work, in which weakly binding ligands were used [26].

1.3. Motivation and Objectives

Silver sintering technology has been shown to be mechanically reliable for attaching large power devices (100 mm^2). However, pressure (usually between three to five MPa) increases the complexity of the sintering process. As reported in the literature, the maximum chip size processed by pressure-free sintering was 6 × 6 mm^2. One objective of this work was to achieve chip-attachment with area of 13.5 × 13.5 mm^2 (the chip size of one kind of commercial IGBT) by pressure-free sintering of nanosilver.

Another objective was to fabricate multi-chip modules (MCM) by pressure-free sintering. Single-chip attachments were fabricated and tested in most previous studies on the sintering of nanosilver. It was worthy to fabricate IGBT MCM because double-pulse tests could be performed without extra packaged devices.

We mentioned in Section 1.2 that most studies in the past several years focused on the mechanical characterization of the performance of pressure-sintered silver joints for

attaching large chips. However, the electrical and mechanical characterizations of silver joints can also provide information on the robustness and reliability of the chip-attach layers. One objective of this work is to electrically and thermally characterize pressure-sintered joints of nanosilver paste. For electrical characterization, IGBT modules with sintered silver will be tested by basic static performance and switching performance. For thermal characterization, the thermal impedance of sintered silver is measured and compared with that of lead-free solder.

Even though the pressure for sintering joints with large area has been reduced to lower than five MPa, there are still several disadvantages of pressure sintering. Besides the high requirements on the equipment for sintering and the surface roughness of substrates, the pressure distribution is also a serious issue for attaching large-area devices, since without a compliant pad, such as a piece of silicone rubber, the added pressure is localized on a small area of the chip (very likely close to an edge) [20]. Thus, compliant pads are necessary, especially for the pressure sintering of a multi-chip module. Generally, the need for pressure for sintering has hampered the quick adaptation of the technology because this limits production throughput. Similar to the press pack, the application of external pressure tends to complicate the manufacturing process and thus increases the cost. For any chip size, attachment without pressure is much to be preferred.

Recently, NBE has modified their nanosilver pastes. With the new pastes, the die-shear strength is over 15 MPa for attaching 10 mm × 10 mm chip without any pressure. Another objective of this work is to perform electrical and thermal characterizations on the pressure-free sintered joints.

1.4. Thesis Organization

Based on the above objectives, this work is divided into four chapters:

Chapter One provides the background for sintered silver joints and reviews the progress in sintering techniques. Recent studies are introduced, which compare sintered silver joints with solder joints in performance.

Chapter Two records the layout design and fabrication procedures of half-bridge IGBT module. The kinds of IGBT module in this work are identified by the process of chip-attachment: vacuum reflow of solder, pressure sintering of silver, or pressure-free sintering of silver. The processes for wire bonding, lead-frame attachment, and thermocouple attachment are also described.

Chapter Three focuses on the electrical characterization of the fabricated modules. Both the static and the switching performance of the packaged device and the modules are recorded and compared with the performance from the datasheet of the bare die.

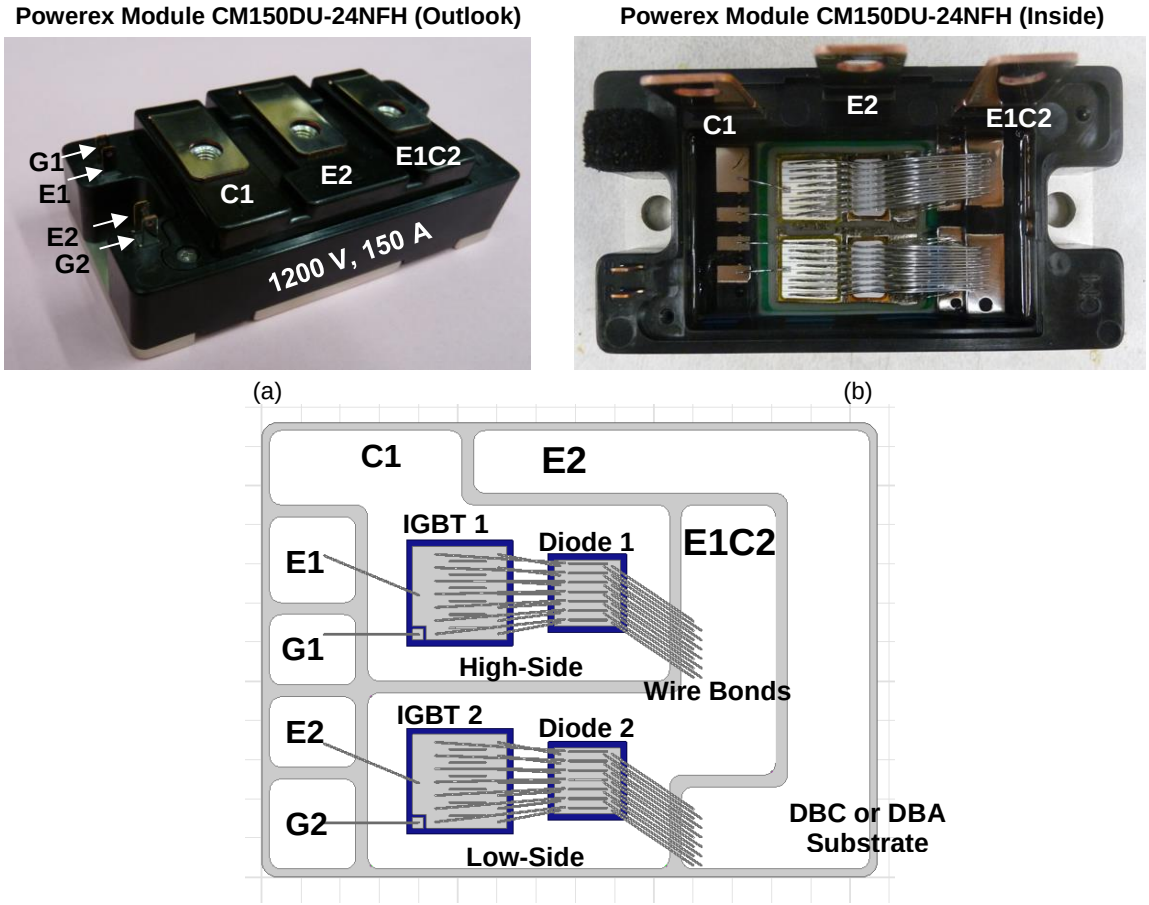
Chapter Four concentrates on the thermal characterization of the fabricated modules. Methods for measuring junction temperature are reviewed. Different setups and results for thermal impedance are recorded. The thermal impedances of different chip-attach joints are compared.

Chapter 2. FABRICATION OF IGBT MODULE WITH PRESSURE-FREE SINTERED JOINTS

2.1. Design and Fabrication of IGBT module

The layout for half-bridge module may vary from one manufacturer to another. Generally, to keep the stray inductance low is a basic requirement for the package design of IGBT module. Also, the effect of thermal cross coupling in a multi-device module should be considered for designing the layout. To avoid the influence of a complete self-designed layout, which may have serious drawbacks, the layout of a commercial module (Powerex IGBT half-bridge module CM150DU-24NFH [27]) is used as the reference, for a good compatibility with the industry standard package. This module has the same voltage and current rating as targeted in this work: 1200 V and 150 A.

The outlook and inside structure of the module are shown in Figure 10 (a) and Figure 10 (b), respectively. Based on Figure 10 (b), a layout is designed and shown in Figure 10 (c). The main difference between the Powerex module and the designed layout is whether the copper traces for the lead-frame and gate pads for the gate driver signals are included. In the Powerex module, these copper traces are installed and integrated with the housing materials. The corresponding fabrication technique is not available in our lab. The copper traces for attaching devices are about 15% larger than the Powerex module. The difference results from the consideration of the dimension of the copper traces designed for the lead-frame, and also the requirement for printing silver paste during the chip-attachment.

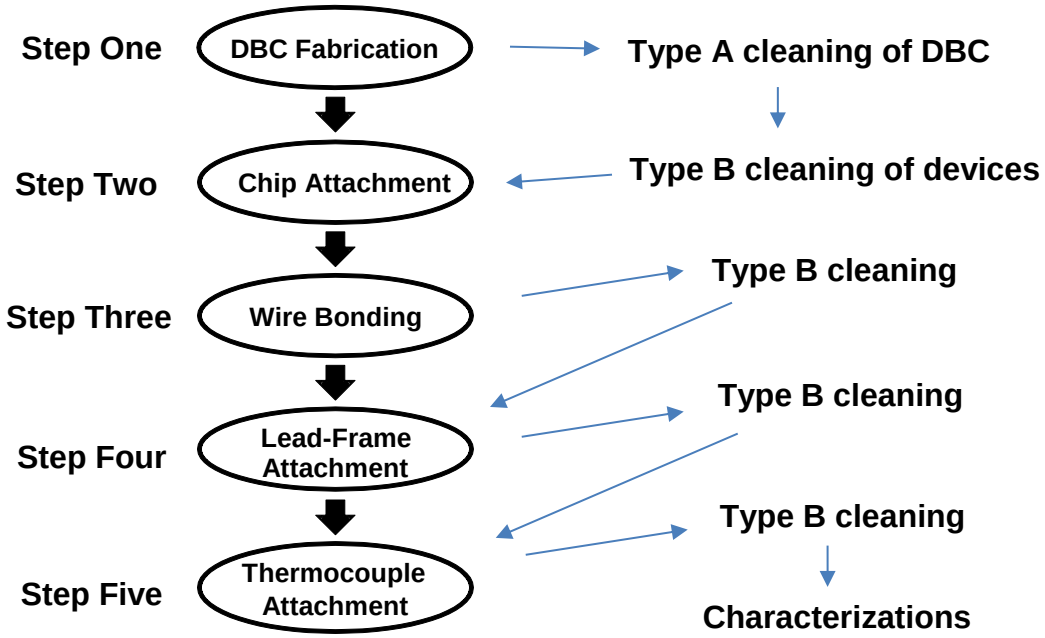


Material properties and component dimensions are shown in **TABLE IV**.

Circuit diagram is shown in **Figure 37** (b).

Figure 10. Based on Powerex module CM150DU-24NFH (a) and (b) [27], layout of IGBT module (c) was designed.

The fabrication of half-bridge IGBT module consists of five steps, as shown in the process flow below.

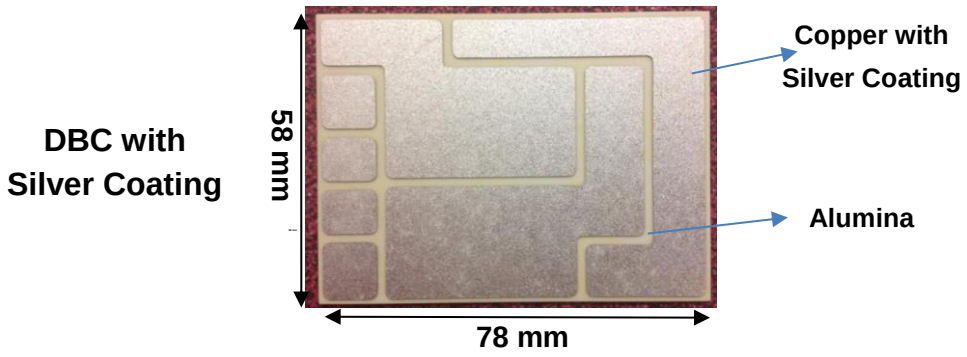


Type A cleaning: Ultrasonic cleaning for 30 minutes

Type B cleaning: Immersed in acetone and ethanol for five minutes

Figure 11. Process flow for fabrication of IGBT module in this work.

The direct-bonded-copper (DBC) used in this work is from Rogers [28], and the surface of copper has already been coated with a thin layer of silver. The original piece of DBC, covered by Kapton tape, was patterned by laser-cutting. A discrete piece of DBC with designed layout was fabricated by chemical etching ($FeCl_3$ solution) and laser cutting on alumina. A single piece of DBC substrate is shown below in Figure 12. The details of procedures and corresponding equipment can be found in [20]. After the chemical etching, the DBC was cleaned by spraying with tap water for 15 minutes to remove the residue of etching solution. Then a big piece of DBC was cut into discrete pieces, each piece went through ultrasonic cleaning for 30 minutes. Even though the piece looks clean after the above ultrasonic cleaning, the residues trapped inside the side of copper traces were difficult to remove completely.



Properties and dimensions of DBC are shown in **TABLE IV**.

Figure 12. Piece of fabricated DBC substrate used in this work.

In this work, IGBT dies [29] and diode dies [30] from ABB were used for the fabrication of modules. There are several considerations for choosing these two devices. First, since an objective of this work is to characterize the joints, the single switch in the half-bridge circuit should have only one IGBT die inside the package to avoid the effect of parallel chips [31]. The ABB IGBT die 5SMY 12M1280 [32] has a footprint of 13.5 × 13.5 mm^2 and the ABB diode die 5SLY 12J1200 [33] has a footprint of 10 × 10 mm^2.

Besides, low forward voltage drop is preferred [34]. Punch Through (PT) has become accepted as the label for relatively thick IGBT dies made from epitaxial wafers and containing an N+ buffer (or Field Stop) layer [35]. Similarly, the term Non-Punch Through (NPT) has become the label for thin chips made from cheaper float zone (FZ) wafers, which do not have the additional N+ layer [36].

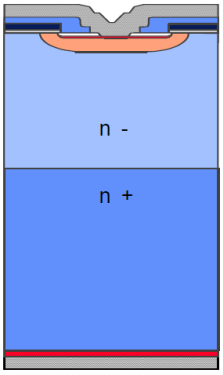
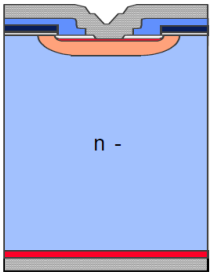
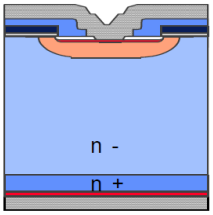
	Punch Through (PT)	Non - Punch Through (NPT)	Soft Punch Through (SPT)
Structure			
Features	Some devices show snappy turn-off at high V_{DC}	Positive temperature coefficient of on-state Extremely rugged	Positive temperature coefficient of on-state Extremely rugged Low losses
Material	Epitaxial	Float Zone	Float Zone

Figure 13. Basics of PT, NPT, and Soft Punch Through (SPT) Technologies. ([36] Semikron Incorporation. (2013). Soft Punch Through (SPT) – Setting new Standards in 1200V IGBT [online]. Available: http://www.semikron.com) Used under fair use, 2013.

The selected devices are fabricated with the technique of "Soft Punch Through +" [36]. This new technique gives a high performance IGBT with much low losses by using an enhanced planar cell design combined with the well-established Soft-Punch-Through (SPT) concept [37].

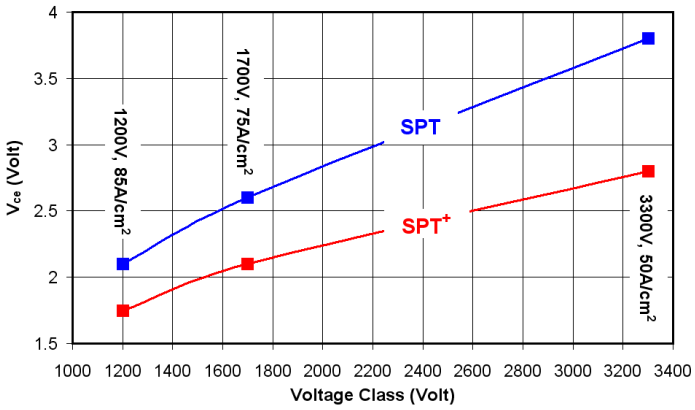


Figure 14. SPT vs. SPT+ IGBT on-state losses at indicated current densities for 1200 V, 1700 V and 3300 V chips at 125°C. ([37] Semikron Incorporation. (2013). Next Generation Planar IGBTs with SPT+Technology [online]. Available: http://www.semikron.com) Used under fair use, 2013.

2.2. Process Profiles of Chip Attachments

This section records the processes of vacuum reflow of solder, pressure sintering of silver and pressure-free sintering of silver. The process and corresponding temperature profile are stated, respectively. Since the surface cleaning of substrate, chip, and chip-attach materials are essential to the quality of joints. All these components went through the cleaning with ethanol and acetone. The material properties and component dimensions are summarized in Table IV. It should be noticed that there is a 210 μm difference of thickness between an IGBT die and a diode die.

TABLE IV

MATERIAL PROPERTIES AND COMPONENT DIMENSIONS FOR DIFFERENT CHIP ATTACHMENT TECHNIQUES

		Thickness (μm)	CTE (ppm/^{o}K)	Young's Modulus (GPa)
Printed Silver [13]		56	18.9	10 (sintered)
SN100C Preform [38]		50	21.5	50
IGBT Dies (Silicon) [32]		140	2.6	185
Diode Dies (Silicon) [33]		350	2.6	185
DBC [28]	Copper	300 (55 × 75 mm^2)	16.5	120
	Alumina	600 (58 × 78 mm^2)	8.1	300

2.2.1. Vacuum Reflow of Solder

Before mounting the materials for soldering, the horizontal level of the graphite boat was adjusted by a gradienter to reduce the tilting of the layup. Weight (approximately eight g for 100 mm^2) was applied on top of the silicon chip. The weight guaranteed contact between the chip, the solder preform, and the substrate and helped reduce the void content in the soldered joint.

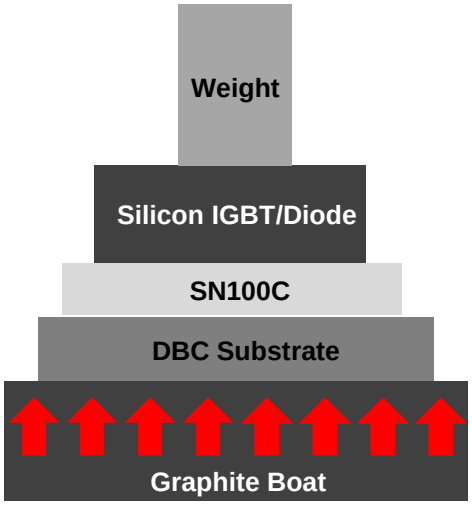


Figure 15. Cross section of vacuum reflow of SN100C.

In the process of vacuum reflow (Figure 16), the graphite boat was heated when current went through it. The temperature of the heated boat was measured and controlled by a thermocouple connected to the graphite boat. By thermal conduction, the materials on the boat were also heated according to a programmed temperature profile. Vacuum reflow is a flux-free process. For the expulsion of the oxygen inside the reflow chamber, vacuum conditions were achieved twice during the pre-heating, with a nitrogen atmosphere in between. Forming gas, a mixture of 10% hydrogen and 90% nitrogen, was applied in the soaking zone at 180^{o}C to remove the oxides at the metal interfaces. It was also applied at the beginning of the cooling stage to avoid the oxidation of soldered joints. The nitrogen atmosphere at the end of the cooling zone increased the cooling rate. A low percentage of voids (usually less than 5% when the area of the spacers was not considered) in the soldered joints were obtained because in a vacuum, gaseous inclusions in the soldered joints expand and disappear into the vacuum.

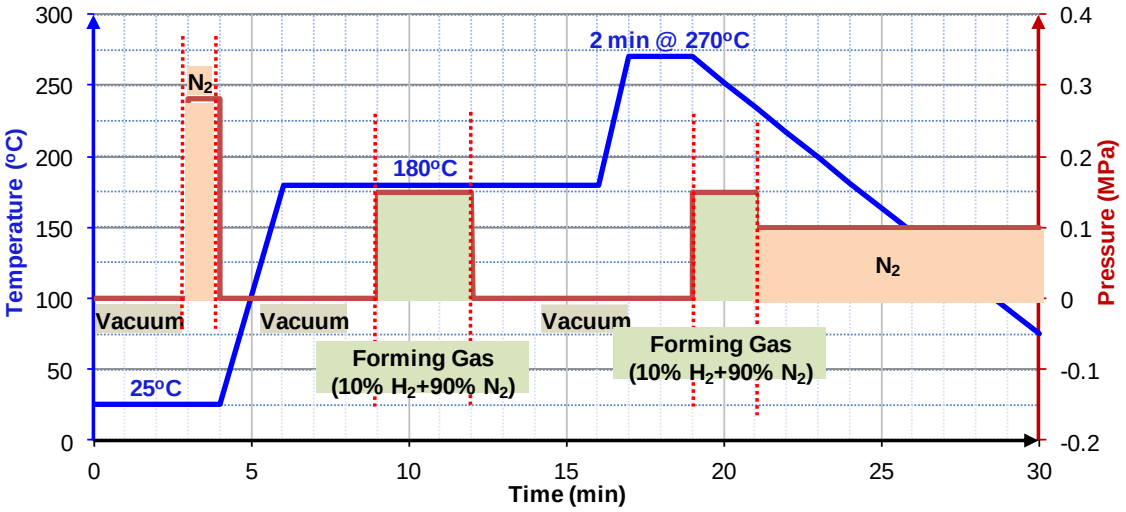
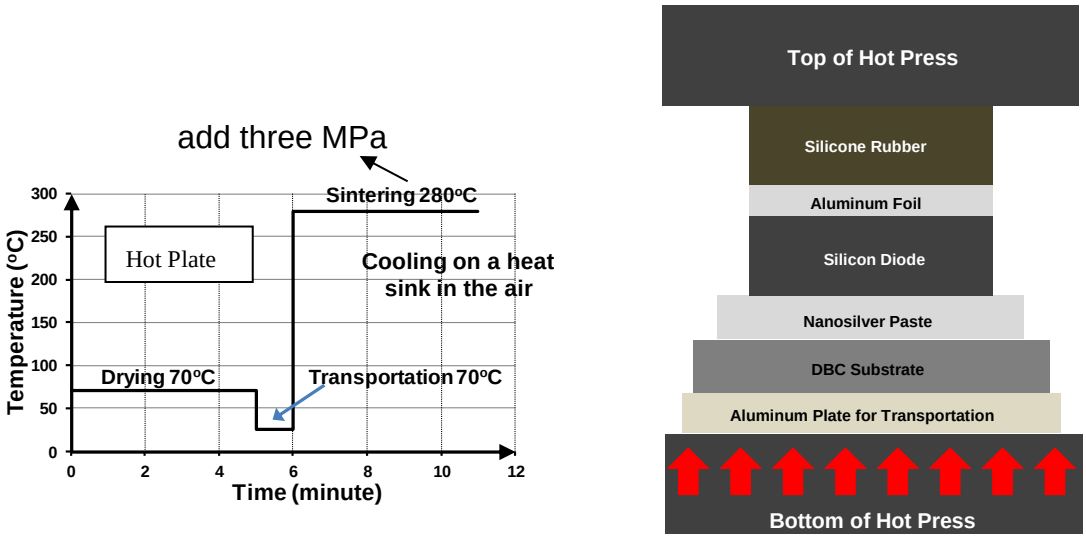


Figure 16. Pressure and temperature profiles for vacuum reflow of solder.

2.2.2. Pressure Sintering of Silver

The nanosilver paste (K-series) was printed onto the DBC by a metal squeegee [39] with a flat tip, using one layer of Kapton tape as stencil, and then dried at 70°C for five minutes. When the paste was dry, the whole substrate was taken away from the hot plate, and chips were added. The substrate with chips was then placed on a thin piece of aluminum (about 1.5 mm thick) for transportation. When the substrate was put in the hot press, pressure was applied within 10 seconds. A piece of aluminum foil was placed over all four chips, and rubber was placed on top of it (Figure 17). Because the IGBT was thinner than the diode, four layers of Kapton tape were put on top of the rubber above the IGBT. The whole assembly was placed under a pressure of three MPa for five minutes in a hot press (about 280°C at the silver paste layer). After sintering, the assembly was placed on a heat sink for cooling.

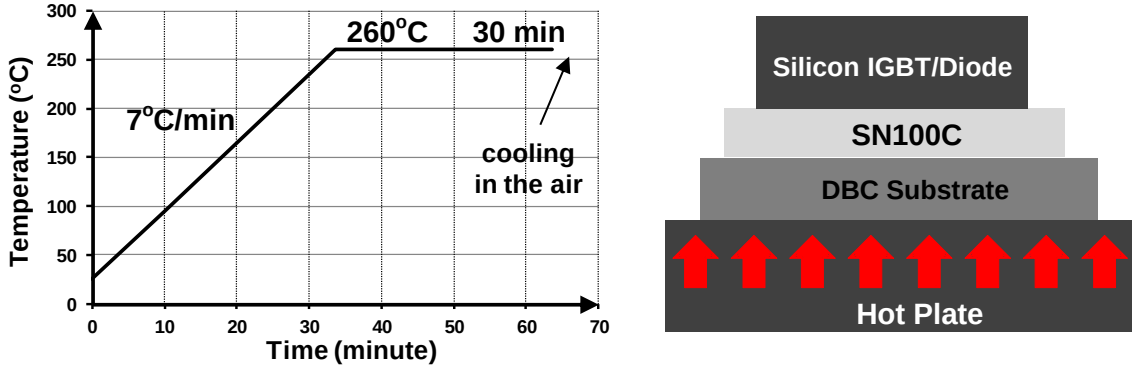


(a) (b)

Figure 17. According to temperature profile (a), printed silver paste was dried at 70°C and then pressure-sintered in the stacked layers (b).

2.2.3. Pressure-Free Sintering of Silver

For the pressure-free sintering, the paste was again printed with the metal squeegee (one layer of Kapton tape as stencil). Chips were placed on the wet paste and transported to a hot plate. A ramp rate of 7°C/min was set to hot plate from room temperature to 260°C, and then soaking for 30 minutes. The whole assembly was cooled to room temperature on the hot plate.



(a) (b)

Figure 18. According to temperature profile (a), printed silver paste was heated at 7°C/min from room temperature to 260°C and then soaked on hot plate in (b).

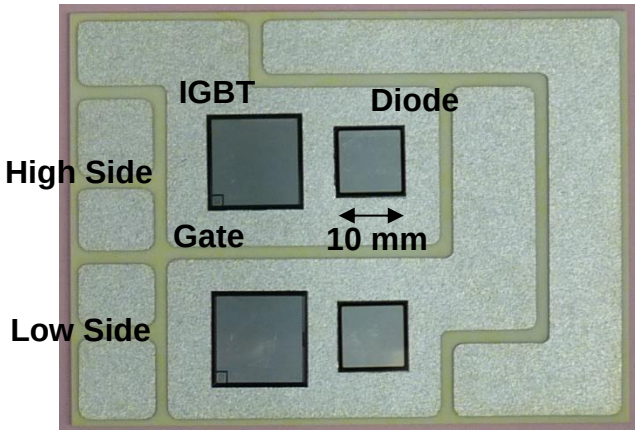
From the description for the three kinds of chip-attach processes, it can be learned that pressure-free sintering is much easier than pressure sintering and vacuum reflow. Besides, pressure-free sintering has much lower requirement on the equipment. Pressure-free sintering has overwhelming advantage in equipment cost over the other two techniques.

TABLE V

COMPARISON OF THREE CHIP-ATTACH TECHNIQUES

Chip-Attach Techniques	Peak Temp. (^{o}C)	Pressure	Atmosphere Requirement	Equipment Requirement
Soldering	272 (**Figure 16**)	8 g/100 mm^2	Forming Gas	Vacuum
Pressure Sintering	280 (**Figure 17**)	3 MPa	Air	Hot Press
Pressure-Free Sintering	260 (**Figure 18**)	N/A	Air	Hot Plate

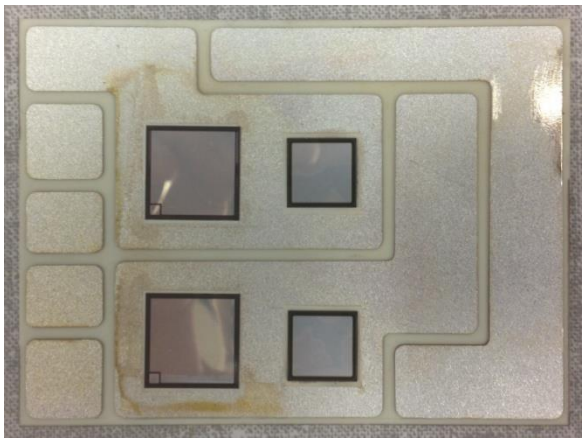
Moreover, the modified paste requires low peak temperature for sintering as shown in Table V. The modules made by the three chip-attach techniques show different surfaces. During sintering, the residue trapped inside the copper trace of the DBC diffused out. In the air atmosphere, it reacts with the silver surface at the sintering temperature. A slight contamination of the surface of the DBC is observed in Figure 19 (c). In the contrast, the contamination on the surface of the module after pressure sintering (Figure 19 (b)) is much worse, owing to the reaction between the binder of the silver paste, surface silver and oxygen in the air [40]. The surface of soldered DBC is clean (Figure 19 (a)), owing to the vacuum condition and the forming gas during the chip-attach process.



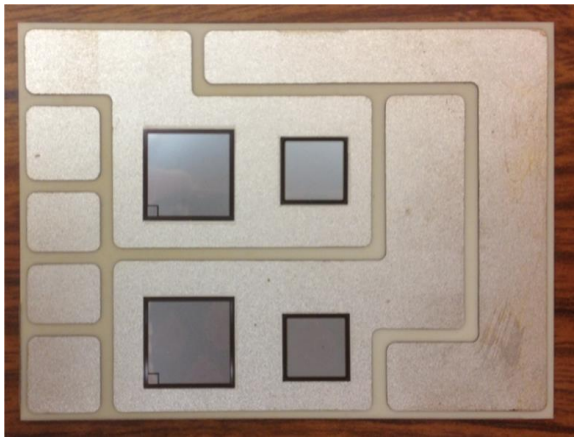
Layout of module is shown in **Figure 10** (c).

Material properties and component dimensions are shown in **TABLE IV**.

(a)



(b)



(c)

Figure 19. Modules after chip attachment by (a) vacuum reflow of solder, (b) pressure sintering of silver paste, and (c) pressure-free sintering of silver paste.

The three kinds of chip-attach joints were characterized by X-ray. The voids in the solder joint (Figure 20 (a)) and the delamination (Figure 20 (b)) in the pressure-free sintered joint can be detected, whereas the fine cracking in the pressure-sintered joint is hardly visible. The voids percentages are calculated by software "ImageJ" [41].

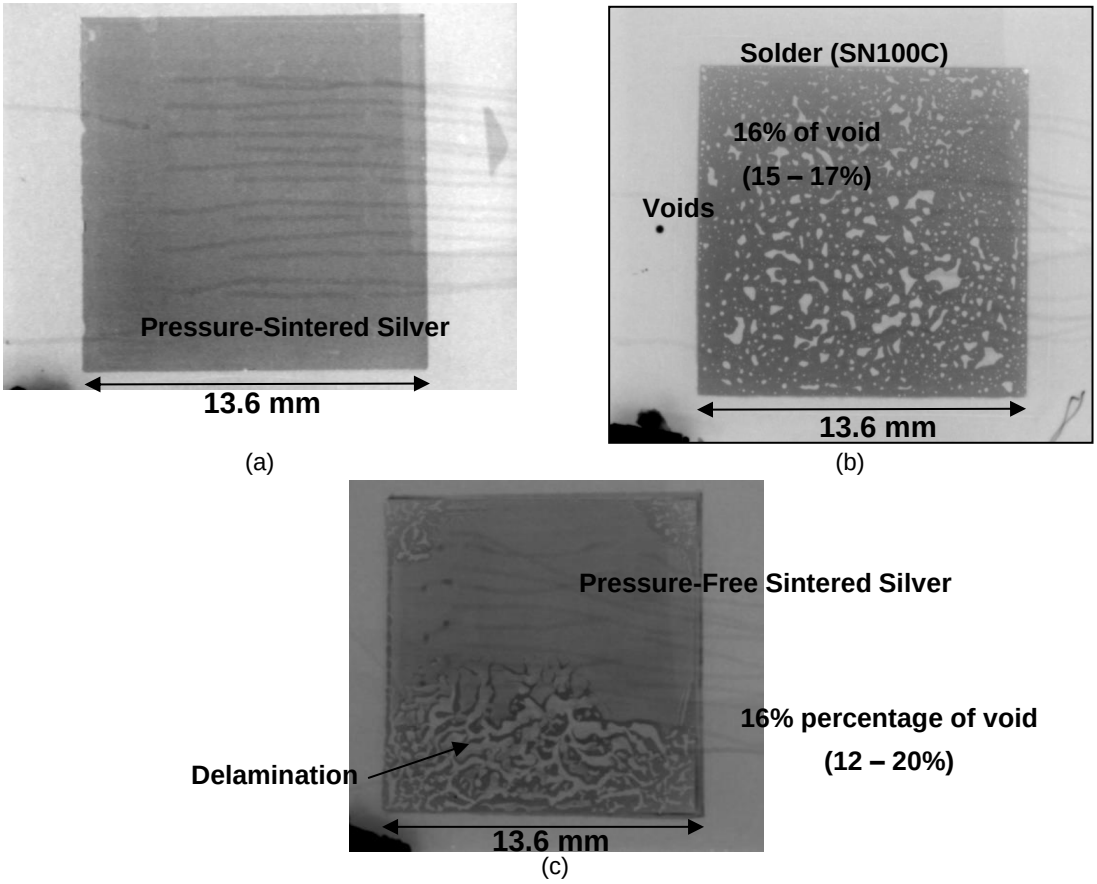


Figure 20. X-ray images of three kinds of chip-attach joints for low-side IGBT dies.

2.3. Other Steps in Fabrication Process

2.3.1. Wire Bonding

This section records the process of wire bonding. 10 mil aluminum wires were available. The number of aluminum wires needed to fabricate a module with 150 A current rating should be calculated. Table VI shows that each 10 mil aluminum wire can safely conduct 15 A current. Allowing for a safe margin, we used 14 pieces of wires in

our designed to connect the two terminals. This number is also the maximum number of wires convenient for fabrication.

TABLE VI

CURRENT CARRYING CAPACITY OF BONDING WIRE

([42] GLX Incorporation. (2013). Current carrying capacity of bonding wire [online]. Available: http://www.circuitsource.com/wiresize.htm) Used under fair use, 2013

Diameter (mil)	Wire Area (mil^2)	Resistivity (Ω/inch)	Typical Fusing Current (A)
1	0.79	1.33	0.27-0.3
1.25	1.23	0.856	0.4-0.5
1.5	1.77	0.595	0.6-0.7
2	3.14	0.335	1.0-1.2
3	7.07	0.149	2-2.5
4	12.57	0.0838	3.5-4.0
5	19.63	0.0537	5-6
8	50.27	0.021	11-12
10	78.54	0.0134	16-18
12	113.1	0.0093	21-23
15	176.71	0.0059	20-35
20	314.16	0.0033	50-60

The pattern of wire bonding is based on the Powerex module. A fabricated module with wire bonds is shown in Figure 21 (b).

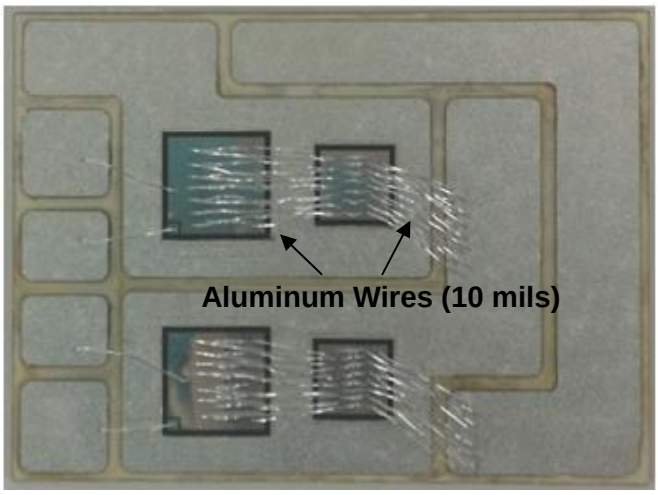
Parameters for Bonding

Bonds on Metal:

Time (400 ms) and Power (280 ultrasonic power)

Bonds on Silicon:

Time (200 ms) and Power (250 ultrasonic power)



Layout of module is shown in **Figure 10 (c).**

Material properties and component dimensions are shown in **Table IV.**

(a) (b)

Figure 21. Wire bonding machine (a) was used to make wire connections (10 mil aluminum), and (b) shows a module with wire bonds.

2.3.2. Lead-Frame Attachment

This section records the process of lead-frame attachment. Two methods have been evaluated for the fabrication.

2.3.2.1. Attachment by Pressure Contact

The pressure is generated from fastening by screws. A plate (top plate in Figure 22) was fastened onto the bottom copper plate. Since the screws have to be at the two ends, a bending of the top plate cannot be avoided. Compliant pads are inserted between the lead-frame and the top plate to ensure uniform pressure distribution. The thickness of the compliant pads needs to be adjusted for each lead-frame. In this work, it was found that for a C1 terminal, the thickness should be one layer of 2.4 mm thick silicone rubber

attached with one layer of Kapton tape. For an E2 terminal, the compliant pad should be the same silicon rubber layer with seven layers of Kapton tape.

The idea of pressure contact is from the MiniSKiiP, which is introduced by Semikron for motor drive applications in the voltage range of 600 V-1200 V and up to 15 kW [43]. Spring contact systems were used to make mounting and removal of the power module easy. The power module is clamped between the cooler and the printed-circuit-board (PCB) with one or two screws, enabling electrical contact and thermal contact at the same time. In case of a defect, the system can be un-screwed to replace the defective components.

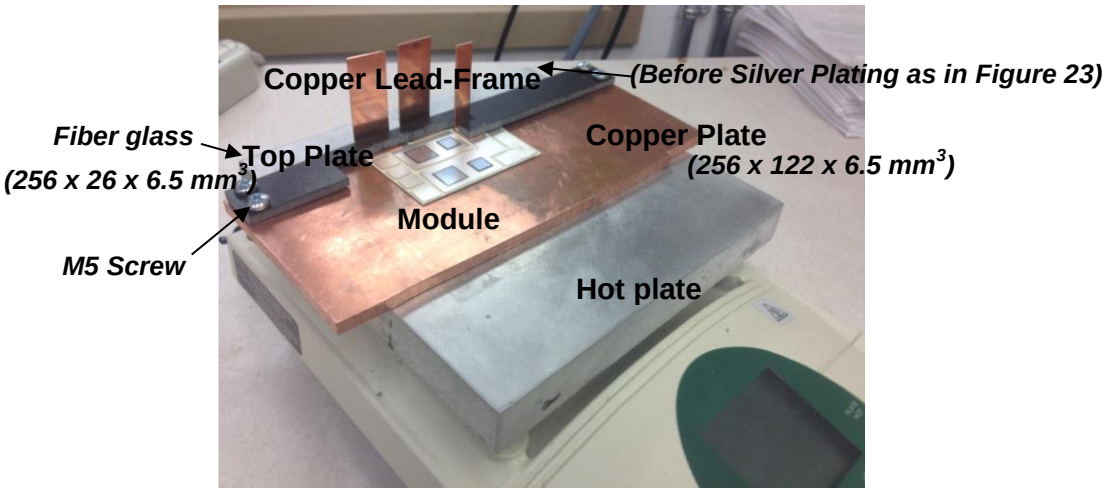


Figure 22. Setup for lead-frame attachment by pressure contact.

Before the lead-frame was applied to the setup, it was bended to the shape that can be fitted to the board for the switching test. Holes were drilled for the connections by screws. After the drilling, it was necessary to coat a thin layer of silver on the copper surface, because the following test condition was at 125^{o}C. The details of the silver plating can be found in [44].

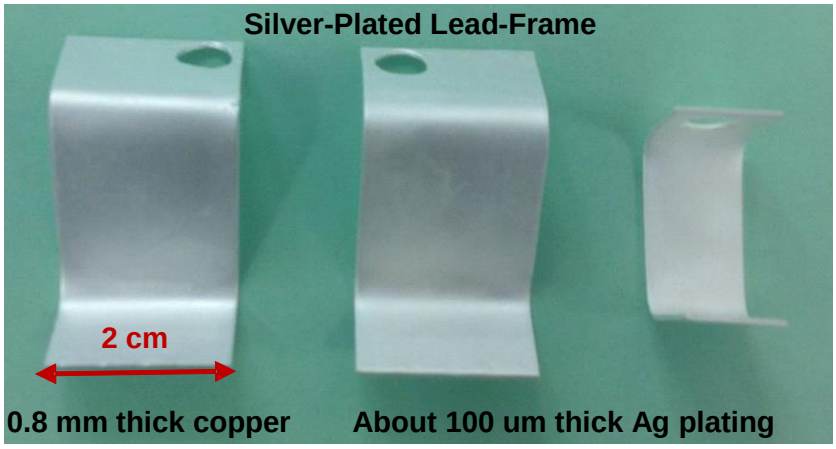


Figure 23. Lead-frame plated with silver.

2.3.2.2. Attachment by Soldering

The lead-frame could also be attached to the DBC by soldering. However, unlike soldering electronic components to the PCB, an iron gun with a chisel tip was good for soldering components to the DBC, owing to a great capability of heat dissipation. In this work, soldering tip STTC-136, with a tip width of 2.5 mm was used. Without the iron gun with a chisel tip, soldering was also achievable with an iron gun with a conical tip. The DBC should be placed on a hot plate for preheating (at 30^{o}C lower than the melting temperature of the solder). A module with a soldered lead-frame is shown in Figure 24 (b).

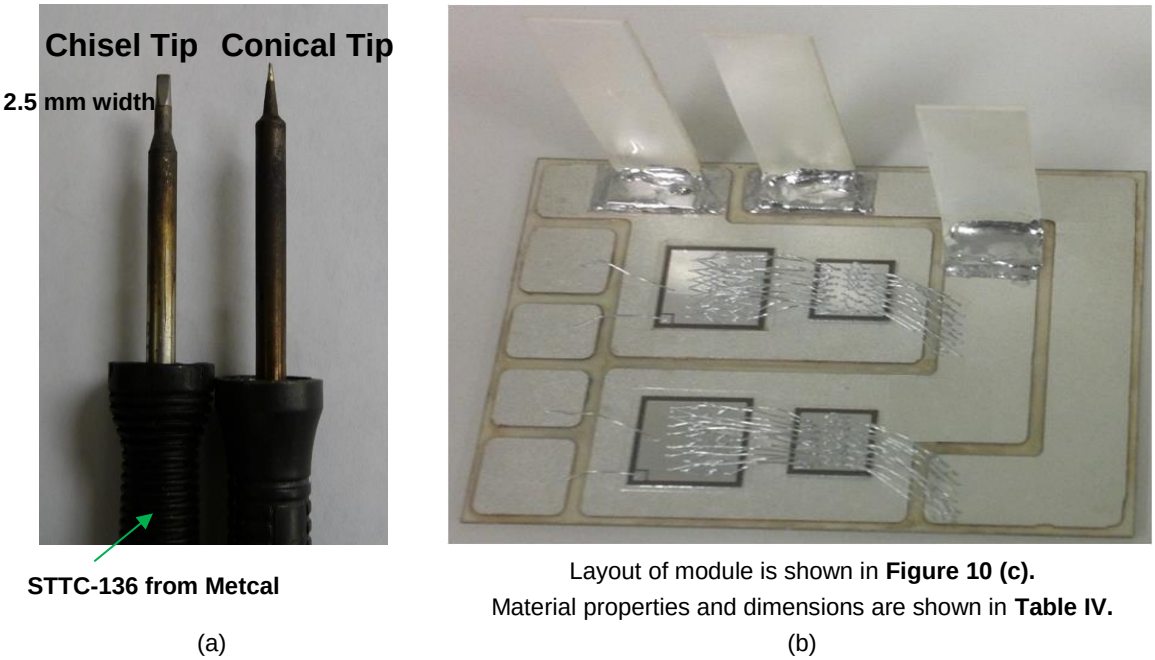


Figure 24. A chisel tip in (a) was used to solder lead-frame, and (b) shows a module with lead-frame.

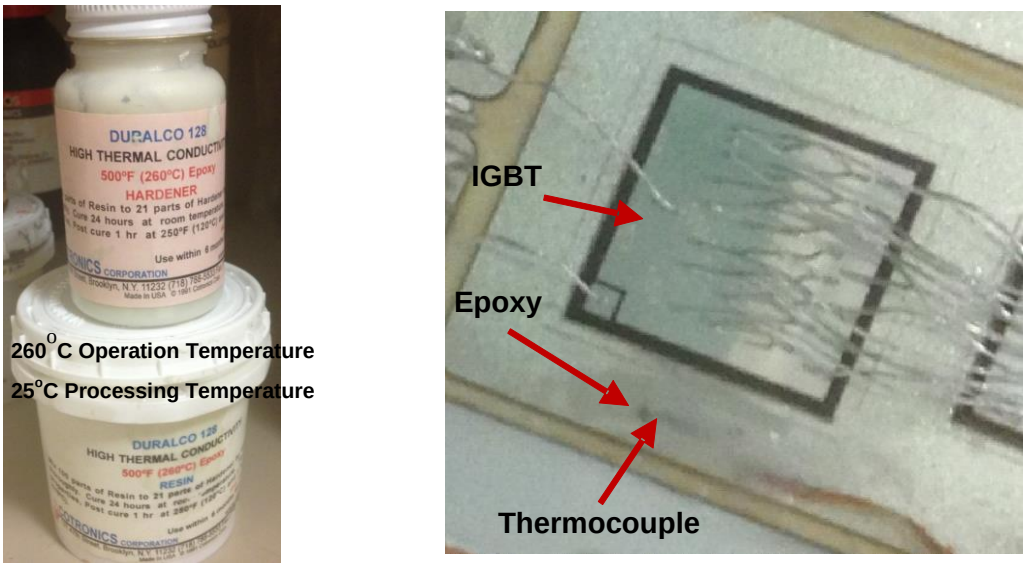
2.3.3. Thermocouple Attachment

There are several ways of attaching a thermocouple to the surface of an electronic component.

Soldering the thermocouple to the surface is recognized as the most reliable method [45]. Due to the high thermal conductivity of solder, the measurement error can be negligible. The soldering of thermal sensors is time consuming and the attachment is permanent. Furthermore, soldering can be done over only several types of metal surfaces and cannot be performed on electronic component without a metal cover.

As an alternative method, tapes, usually aluminum or Kapton tapes have been used to attach the thermocouple to the component [45]. They are easy to apply and remove, inexpensive and readily available. However, care must be taken to ensure that the thermocouple bead contacts the surface during measurement. A contact is not always guaranteed. If the thermal sensor is only slightly off the surface, it could read just the ambient temperature since there is nothing but air between the sensor and the surface,

which provides the best insulation because of its ultra-low thermal conductivity. To ensure good contact, the tape has to be large enough. But for components of small to medium size, the added tapes can act either as an insulation layer (such as Kapton tapes) or as a spreading layer (such as aluminum tapes) and affect the component temperature.



(a) (b)

Figure 25. Epoxy (a) was used to attach thermocouple to module in (b).

The most convenient way so far of attaching a thermocouple to electronic components in a system-level thermal test is using epoxy, especially rapid-bonding epoxy materials [45]. Some of these epoxy materials can dry in just several seconds and provide a relatively strong bond. The thermocouple can be easily removed by applying solvent. The thermal conductivity of the quick-dry epoxy materials is fairly low.

In this work, the epoxy Duralco 128 [46] was used. The process of using epoxy is mixing 100 parts of resin to 21 parts of hardener by weight, followed by curing for 24 hours at room temperature. A module with an attached thermocouple is shown in Figure 25 (b). The peak operation temperature 260 ^{o}C is higher than the required temperature (125^{o}C in this work). The low processing temperature of 25^{o}C makes it possible to skips an extra thermal cycle for modules.

Chapter 3. ELECTRICAL CHARACTERIZATIONS OF IGBT MODULE

The three kinds of fabricated modules went through static characterization first, since it is fast and reveals the basic performance of the devices. The setup and typical results are described in Section 3. In the next step of electrical characterizations, the modules are connected to a double-pulse tester. The components and setup of the double-pulse tester are recorded in Section 3.2 together with the switching performance of the fabricated modules.

3.1. Static Characterizations

Static characteristics, which include the DC characteristics (current-voltage relationship, I-V) and AC characteristics (impedances), provide the most basic evaluations of the performance of a power semiconductor device (called device under test or DUT from here on) [47].

The characteristics of semiconductor devices are sensitive to the operating temperature. For the temperature-dependent characterizations, an additional heating device, in the curve tracer, can be used to heat the DUT [48]

3.1.1. Setup of Static Characterization

An example of the measurement setup with the use of the curve tracer is shown in Figure 26. To heat up the device to a junction temperature of 125^{o}C, which is one test condition in the datasheet of bare die, a hot plate is placed near the curve tracer and control panel. The junction temperature is monitored by a K-type thermocouple attached to the DBC by epoxy as is stated in Section 2.3.3. A GPIB (General Purpose Interface Bus) controller is used to send commands to the curve tracer and to collect the measurement data.

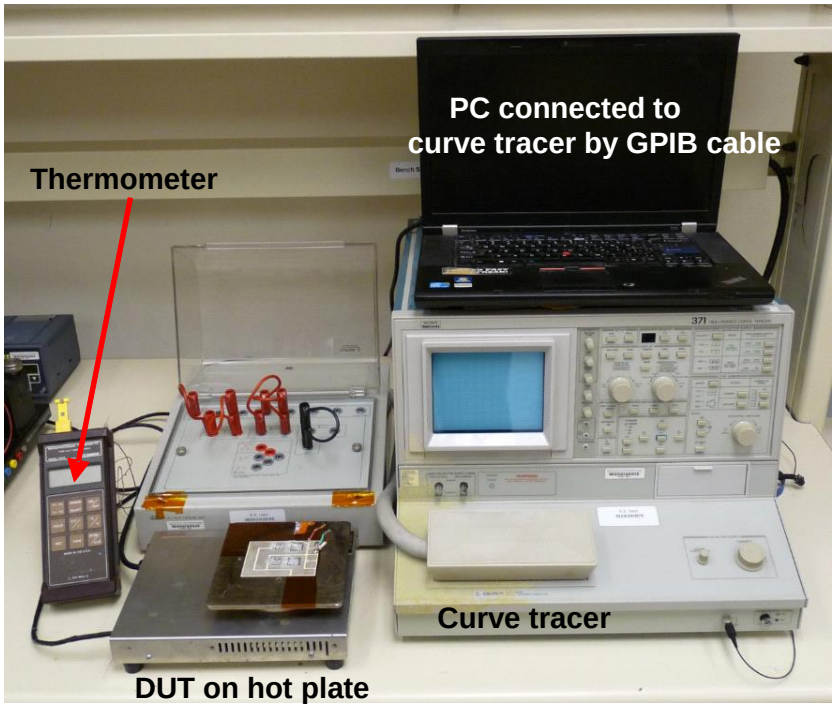


Figure 26. Static characterizations setup with curve tracer.

3.1.2. Breakdown Characteristics

Packaged device should have the same breakdown voltage as the bare device has. **Figure 27** shows that IGBT and diode in the fabricated module can sustain 1200 V as stated in the datasheet.

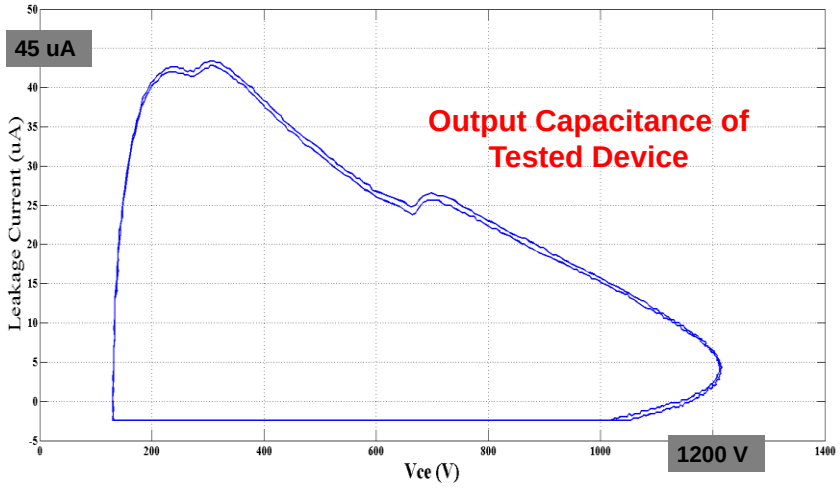


Figure 27. Breakdown capability of IGBT in fabricated module.

3.1.3. I-V Characteristics

For measuring the I-V characteristics of a device, the curve trace provides a circuit similar to four-terminal sensing [49].

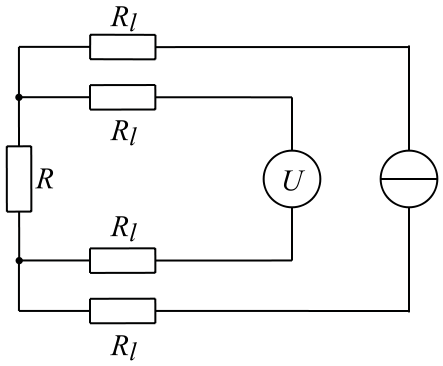


Figure 28. Circuitry for four-terminal sensing. ([49] *IEEE Master Test Guide for Electrical Measurements in Power Circuits,* ANSI/IEEE Standard 120-1989.) Used under fair use, 2013.

Four-terminal sensing is an electrical impedance measuring technique that uses separate pairs of current-carrying and voltage-sensing electrodes to make more accurate measurements than traditional two-terminal (2T) sensing. The key advantage of four-terminal sensing is that the separation of current and voltage electrodes eliminates the impedance contribution of the wiring and contact resistances.

Figure 29 and Figure 30 shows the I-V curves at 25^{o}C and 125^{o}C for IGBT dies and diode dies, respectively.

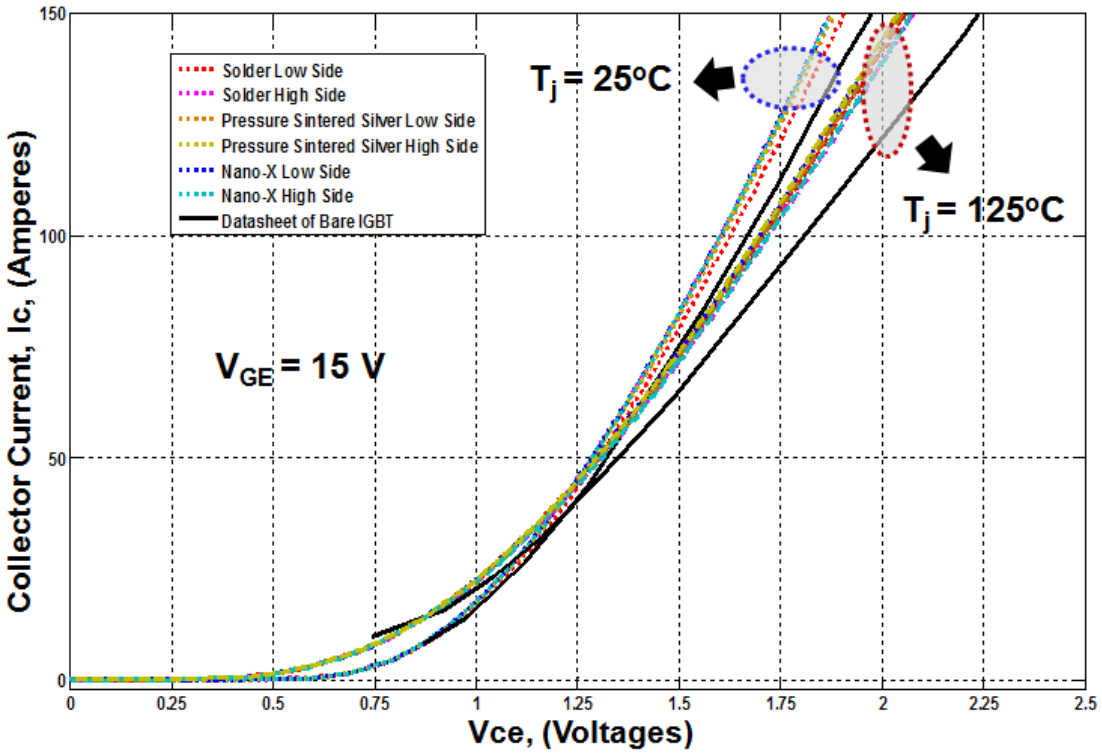


Figure 29. I-V curves of IGBT dies after attachment by three different techniques.

The measurements are compared with the I-V curves in the datasheet of the bare die. The curves in the datasheet are extracted by the "Scanned Data Utility" from Saber, which provides an interactive way of importing data from a scanned graph. The I-V curves of the diode show that the diode in the fabricated module has almost the same performance as stated in the data sheet for tests at both 25°C and 125°C. There is a difference of 0.33 mΩ between the measured I-V curves and the curves in datasheet for IGBT.

The block capability of the packaged IGBT dies and diodes are up to 1200 V, and the gate threshold voltage of the IGBT is within the range stated in the datasheet.

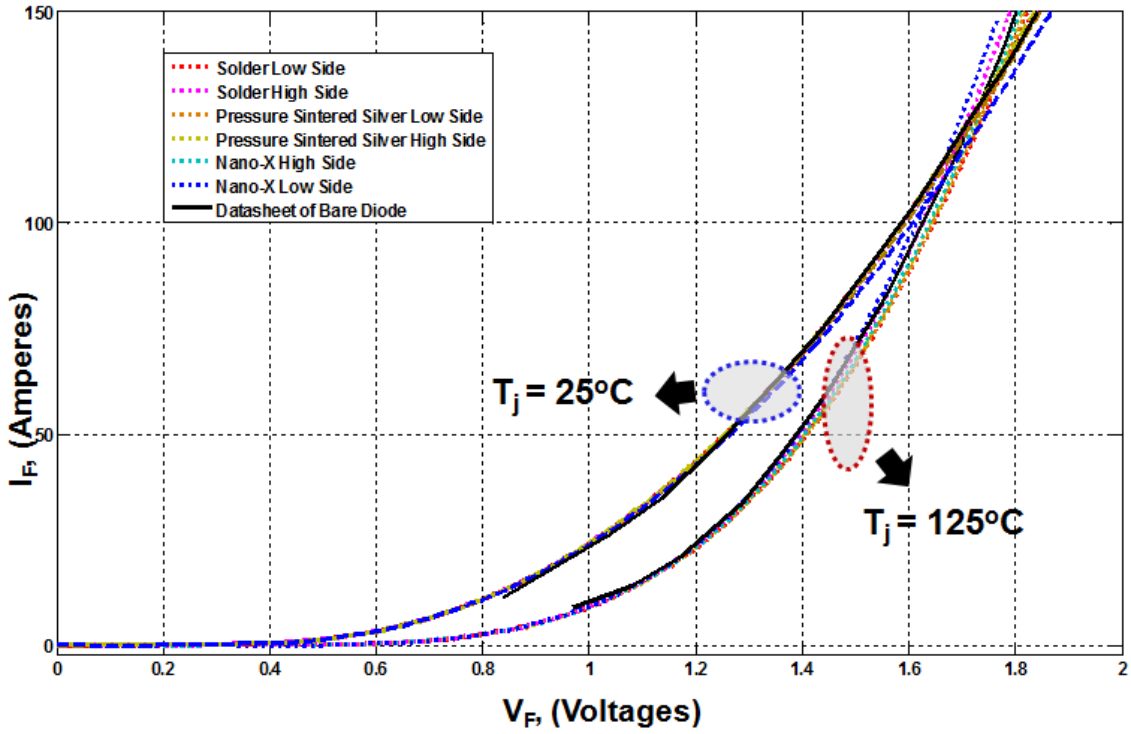


Figure 30. I-V curves of diodes after attachment by three different techniques.

3.2. Switching Characterization

Double-pulse switch testing is a standard and efficient method to investigate the switching energies, turn-on and turn-off power losses, turn-on and turn-off times, and conduction loss of power electronic devices (transistor and FWD) at different voltage and current. The gate drive circuit is attached to the transistors gates, and a double-pulse is applied. The double-pulse is composed of one long pulse followed by a shorter pulse, allowing turning on and turning off at full current, i.e., 150 A in this case. The energy loss is the integral of the power dissipation at the switching transient stage. Because of the reverse recovery of the diode and the parasitic inductance inside the switching loop, there were voltage spikes and current spikes in the switching waveforms. Typical transistor and diode current waveforms in the double-pulse test are shown in Figure 31. The overshoot in the voltage waveform at turn-off transient results from the parasitic

inductance within the switching loop, and overshoot in the current waveform at turn-on transient results from the reverse recovery of the freewheeling diode.

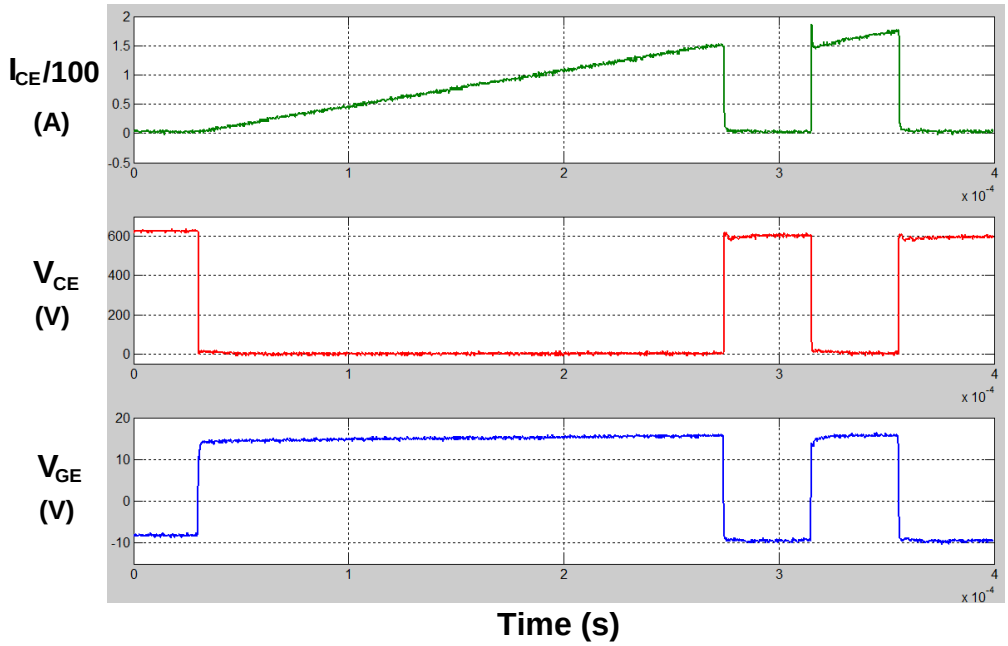


Figure 31. Typical waveforms from double-pulse test.

For the design and fabrication of the double-pulse tester, one basic principle is to minimize the parasitic inductance [50].

3.2.1. Characterization Setup

A schematic and the hardware of double-pulse tester are shown in Figure 32 and Figure 33, respectively.

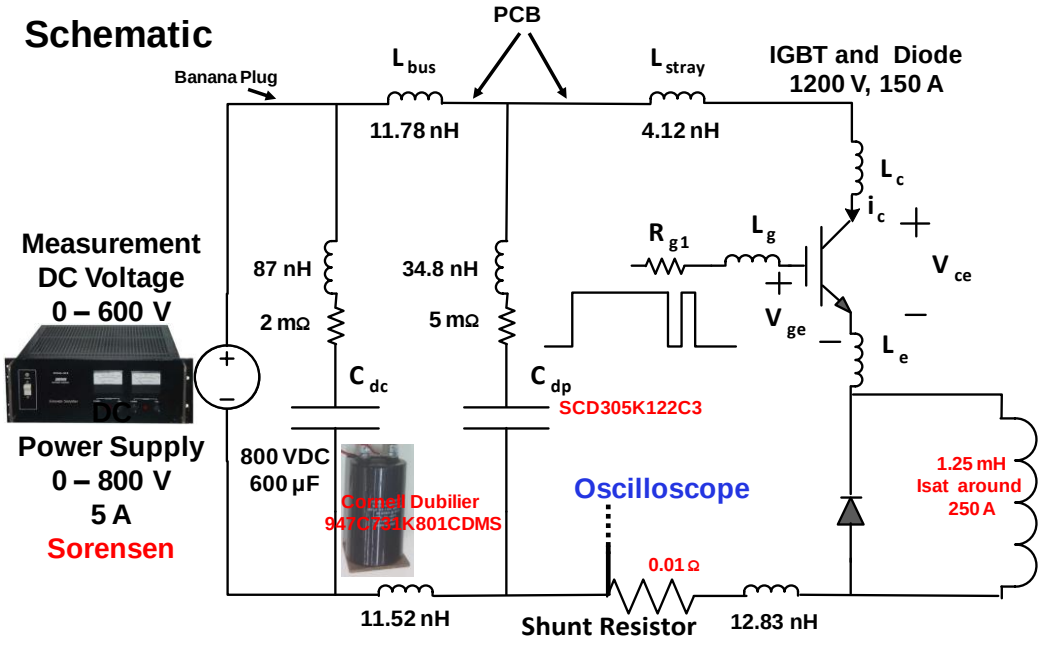


Figure 32. Schematic of double-pulse tester.

The connection between any pair of components was designed in such a way as to minimize the distance between the components, which in turn provides the minimum parasitic inductance.

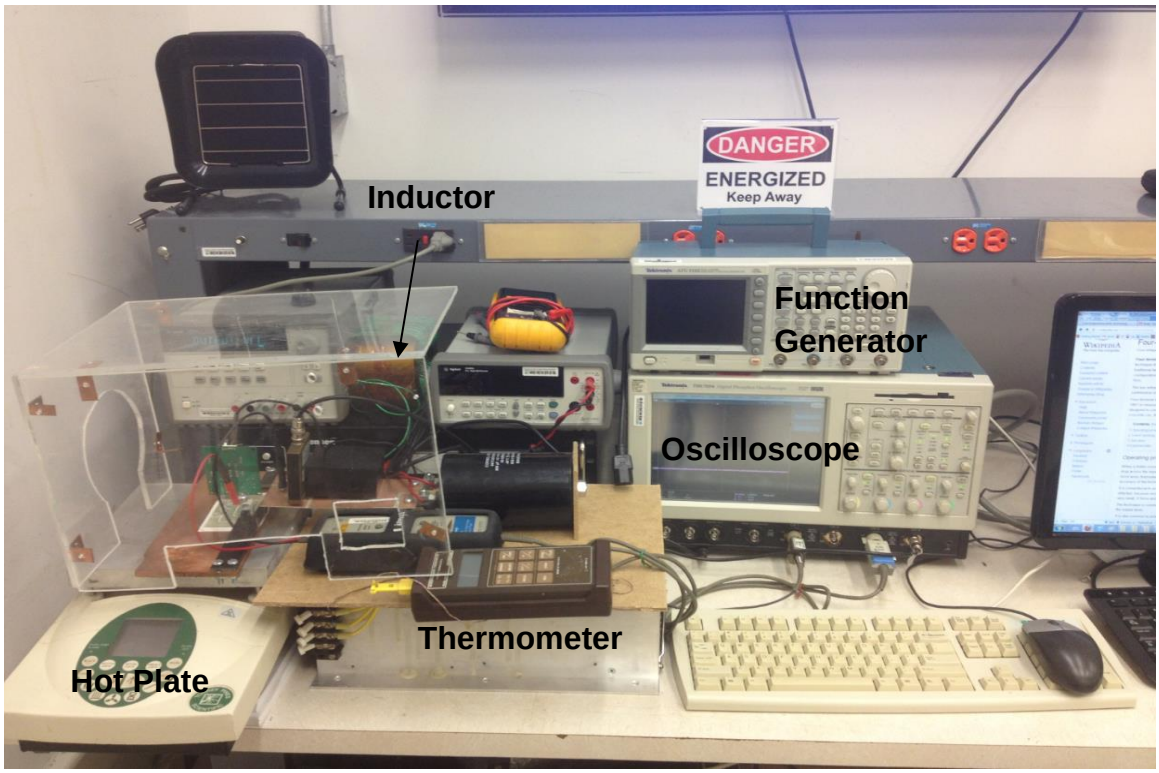


Figure 33. Hardware of double-pulse tester.

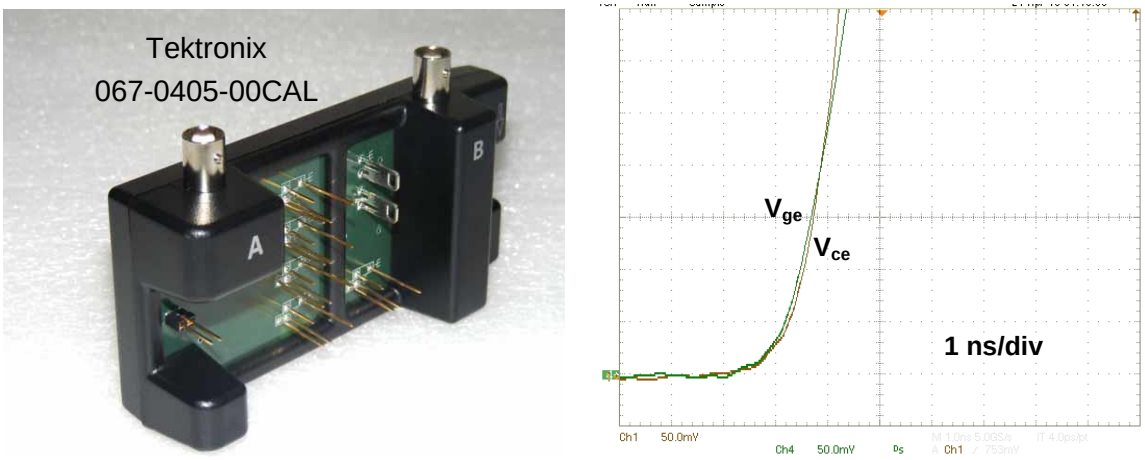
3.2.1.1. Gate Driver

The turn-on of the IGBT was controlled by voltage rather than current, but the speed of turn-on increases with the magnitude of gate current [51]. The input capacitance between the gate and the emitter was charged to a voltage (V_{GE}) greater than the threshold voltage (V_{th}) in order to turn on the IGBT. During the turn-off of the IGBT, the gate-emitter resistance (R_{GE}) provided a path for the input gate-to-emitter capacitance to discharge. The R_{GE} altered the IGBT turn-off time, and it was under the control of the circuit designer.

The gate driver used in this work was Powerex (BG2C) [52]. It had an off-state gate voltage of -8 V. The external gate resistance was 6.8 Ω, which was the same as the value claimed in the datasheet.

3.2.1.2. Deskew

The switching loss at transient is determined by the integration of the product of instant voltage drop and instant current. It is necessary to synchronize the measured signals of current and voltage. Thus, the Tektronix 067-0405-00CAL deskew fixture [53] is used. The final difference between the channels of the oscilloscope is shown in Figure 34 (b). In reference to Channel 1 (Vge), Channel 3 (Vce) has a deskew of 10 ns, and Channel 4 (Ice) has a deskew of -350 ps.



(a) (b)

Figure 34. Deskew bias between channels of oscilloscope by (a) to get negligible difference as in (b).

3.2.1.3. Probe Connection

The voltage probe has a tip-to-ground loop inductance. The ground leads of the probe have inductors in series with the measurements. In the presence of high dv/dt value and large electromagnetic fields, this inductor will create errors in the voltage measurements. To reduce the measurement errors, a probe-tip adaptor, as demonstrated in Figure 35, can be used to reduce the tip-to-ground loop inductance. The probe-tip adaptor also can help reduce the potential problem of overheating the polymer in the probe when used at the junction temperature of 125^{o}C.

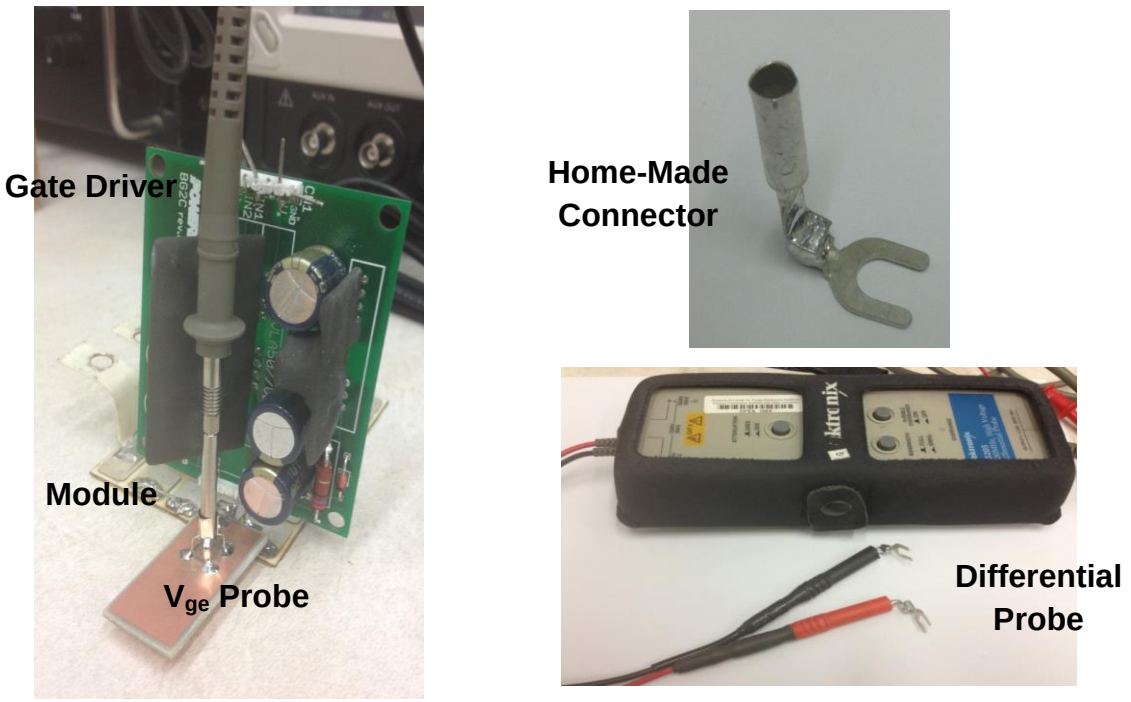


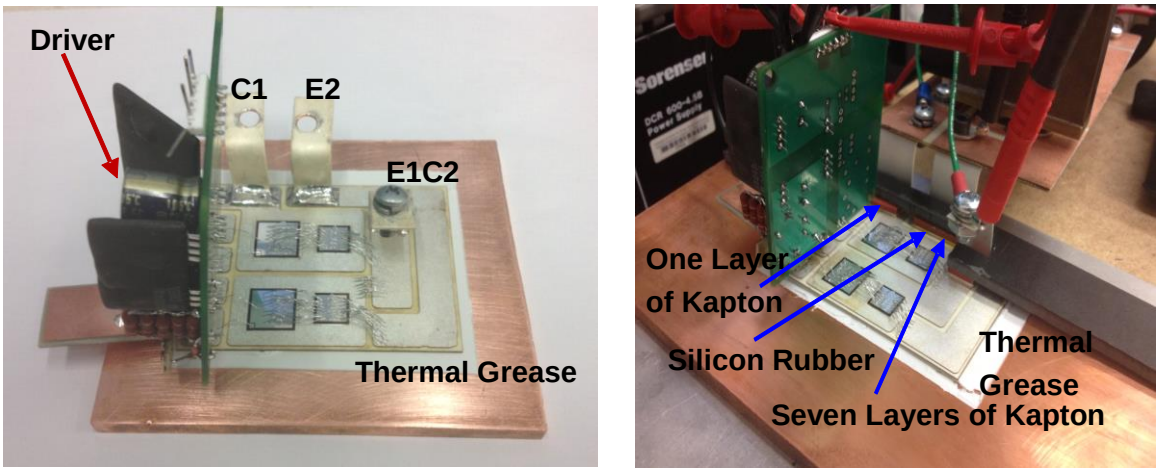
Figure 35. Probe connections for (a) passive probe and (b) differential probe, to avoid overheating polymer on the probes.

3.2.1.4. Shunt Resistor

Coaxial shunts have several advantages over surface mount resistors. The current flowing in the shunt should not produce significant levels of magnetic flux in the region where the sense wires are placed [54]. Therefore, the sense wires are not inductively coupled to the shunt current, and the output voltage does not contain any inductive component. The outer shell of the shunt resistor provides shielding from the external fields generated by the switching action. Protection from the external noise sources and the internal fields of the current traveling through the resistive elements should yield an accurate measurement even for small output voltages and fast transitions [55]. In this work, the shunt resistor "W-1-01-2 stud" from T&M (0.01008 Ω) was used.

3.2.1.5. Thermal Grease

Thermal grease with a conductivity of 3.8 W/(m·^{o}K) was used in this work [56]. Figure 36 shows two modules (obtained by two different methods of lead-frame attachment) attached to copper plate with the thermal grease.

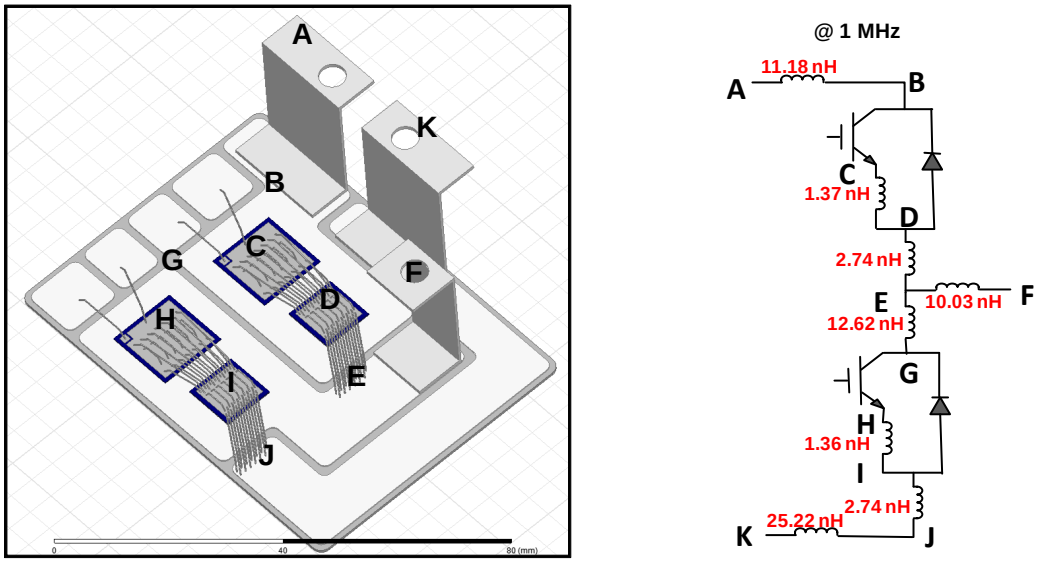


(a) (b)

Figure 36. Module with soldered lead-frame attached to copper block as shown in (a), and module with pressure-contacted lead-frame in (b).

3.2.2. Extraction of Parasitic Inductance in Part of Components

To get an understanding of test condition, it is necessary to know the parasitic inductance within the module itself as shown in Figure 37. In this work, ANSYS Q3D Extractor [57] was used to extract the stray inductance from the designed module [58]. Together with the values in the Figure 32, the loop parasitic inductances could be recorded for the double-pulse tester.



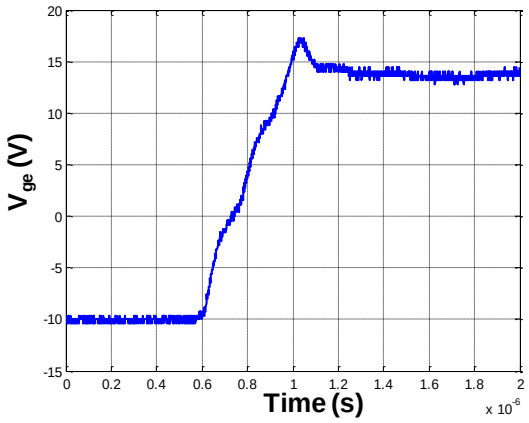
(a) (b)

Figure 37. Q3D extractor was used to build the simulation model (a) and extract the parasitic inductance in the module as shown in (b).

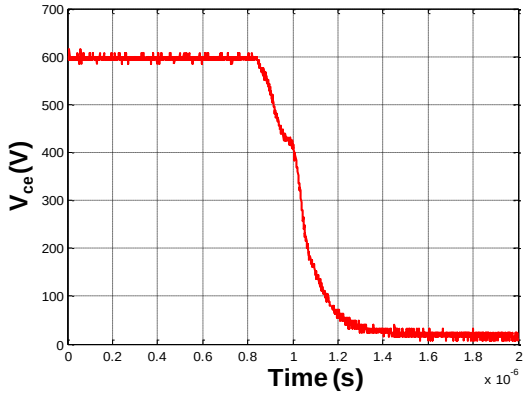
3.2.3. Definitions of Switching Characteristics

Typical waveforms are shown in the following figures from measurements of the double-pulse test at 600 V, 150 A, and an external gate resistance of 6.8 Ω.

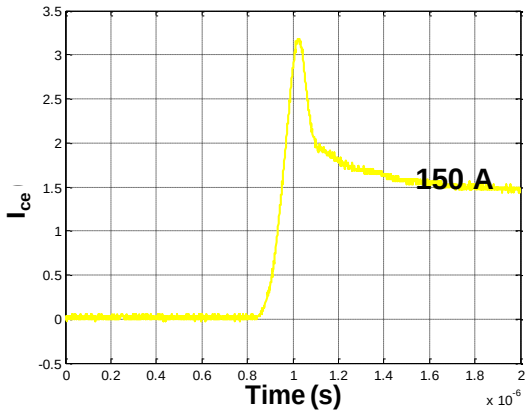
Turn-On Transient



(a)



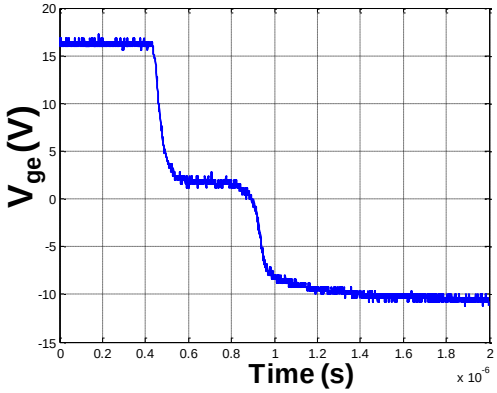
(b)



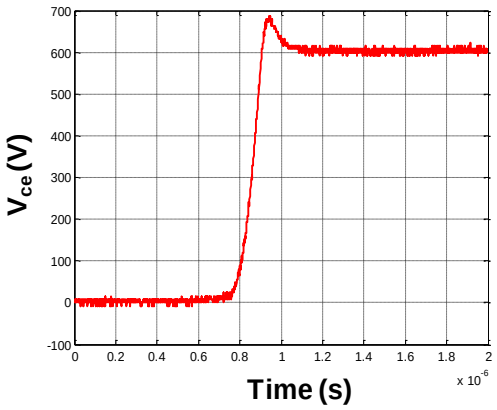
(c)

Figure 38. Turn-on transient of (a) Vge, (b) Vce, and (c) Ice.

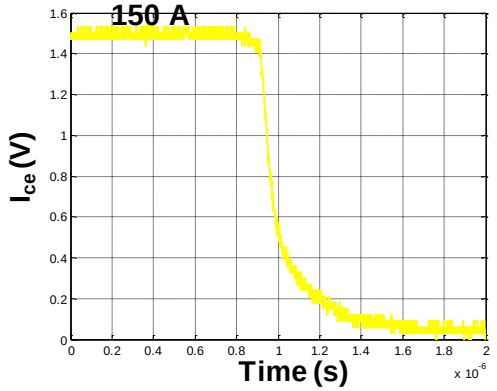
Turn-off Transient



(a)



(b)



(c)

Figure 39. Turn-off transient of (a) Vge, (b) Vce, and (c) Ice.

It can be observed that all the waveforms are clean.

Based on these waveforms, the switching parameters are calculated. It should be noted that different manufacturers may use different definitions of switching parameters ([58]-[61]). Most of the definitions used in this work follow those in the ABB application note [59].

Turn-on Delay ($t_{d(on)}$)

The turn-on delay time is defined as the time between the instant when the gate voltage has reached 10 % of its final value and the instant when the collector current has reached 10 % of its final value.

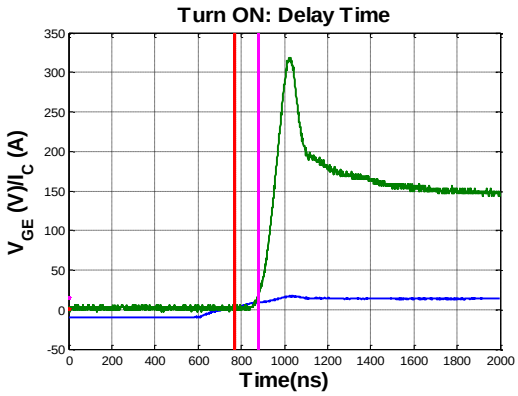


Figure 40. Measurement of delay time for turn-on.

Turn-off Delay

The turn-off delay time is defined as the time between the instant when the gate voltage has dropped to 90 % of its initial value and the instant when the collector current has dropped to 90 % of its initial value.

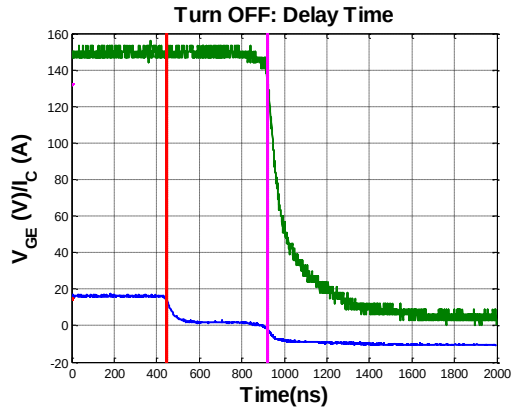


Figure 41. Measurement of delay time for turn-off.

Rise Time

The rise time is defined as the time for the collector current to rise from 10% to 90 % of its final value.

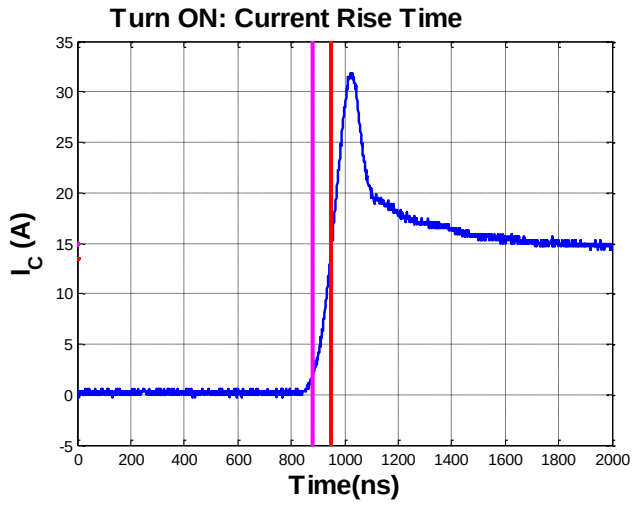


Figure 42. Measurement of rise time.

Fall Time in ABB Application Note

The fall time is defined as the time during which the collector current has dropped from 90 % to 10 % of its initial value along an extrapolated straight line drawn between the instants when the current has reached 90 % and 60 % of its initial value.

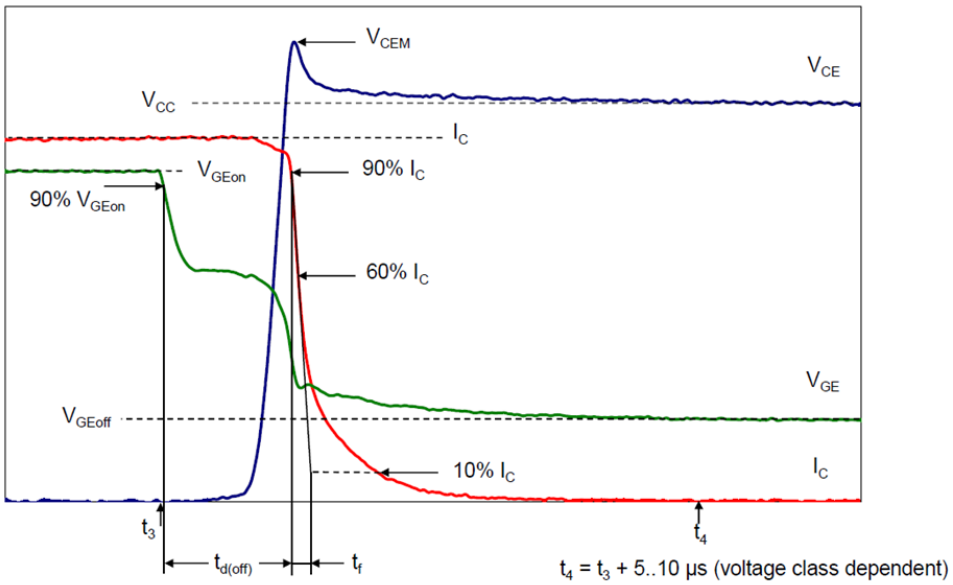


Figure 43. Definitions of turn-off parameters for ABB IGBT. ([59] ABB Switzerland Ltd. (2013). Application note 5SYA 2059-04: Applying IGBT and Diode dies [online]. Available: http://www.abb.com) Used under fair use, 2013.

Fall Time in Measurement

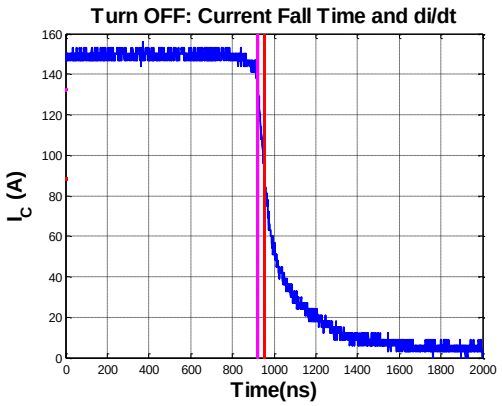
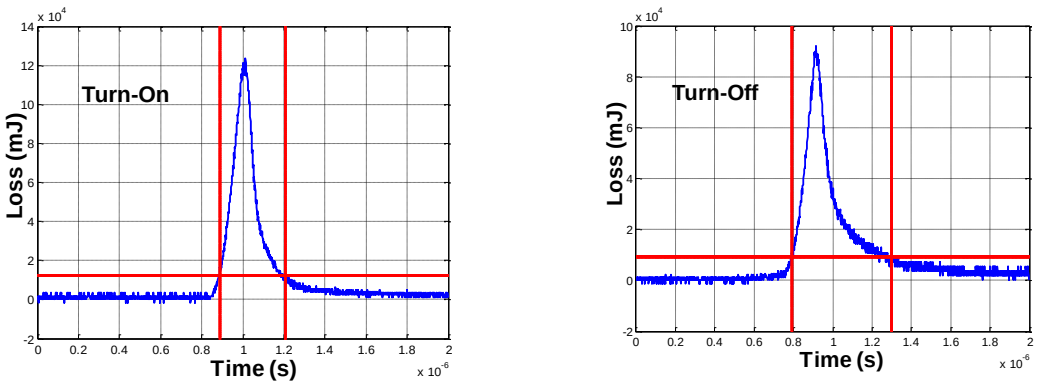


Figure 44. Measurement of fall time.

The datasheet did not provide an accurate way for measuring the switching loss. In this work, the switching loss was defined as the area (the integration of the product between current and voltage over the switching period) above the 10% of peak point.

Switching Loss



(a) (b)

Figure 45. Measurements of switching loss.

3.2.4. Measurement Results

Since all the waveforms are clean and up to the rated voltage and current, the measured results are reliable. The typical results are summarized in the following tables for 600 V and 150A. Table VII and Table VIII summarize the switching performance at 25°C and 125°C, respectively. Table IX summarizes the switching performance under the influence of external gate resistance. Even though, for each type of module, there were

just two pieces of module, there were no difference among the modules, except for the chip-attach layers. Thus, statistically, there were six samples for obtaining following data.

TABLE VII

SUMMARY OF SWITCHING PERFORMANCE OF MODULES FABRICATED WITH DIFFERENT CHIP-ATTACH TECHNIQUES (25°C AND 6.8 Ω)

	Tdon (ns)	Trise (ns)	Eon (mJ)	Tdoff (ns)	Tfall (ns)	Eoff (mJ)
Datasheet	200	70	16	460	50	9.4
Soldered Module	110	68.4	11.734	397.2	56.5	9.49
Pressure-Sintered Module	98.4	72	11.725	388.8	61.87	9.586
Pressure-Free Sintered Module	102.4	73	11.728	393.5	62.1	9.52

TABLE VIII

SUMMARY OF SWITCHING PERFORMANCE OF MODULES FABRICATED WITH DIFFERENT CHIP-ATTACH TECHNIQUES (125°C AND 6.8 Ω)

	Tdon (ns)	Trise (ns)	Eon (mJ)	Tdoff (ns)	Tfall (ns)	Eoff (mJ)
Datasheet	230	70	22	525	75	15
Soldered Module	109.6	72	16.31	474.4	89.6	15.452
Pressure-Sintered Module	120.4	80	15.997	465.4	85.33	15.224
Pressure-Free Sintered Module	113.4	76	16.18	470.8	87.5	15.244

TABLE IX

INFLUENCE OF GATE RESISTANCE ON SWITCHING PERFORMANCE (SOLDER JOINTS AT 125°C)

Rg (Ω)	Tdon (ns)	Trise (ns)	Eon (mJ)	Tdoff (ns)	Tfall (ns)	Eoff (mJ)
6.8	109.6	72	16.31	474.4	89.6	15.452
16.5	152	104.8	26.238	684.8	72.5	15.942
27.5	214.4	134.4	39.151	947.2	66.13	16.595
43.2	310.4	153.6	52.376	1246.4	81.07	18.264

3.3. Conclusions

The electrical tests above showed the devices, after the fabrication, operate properly. All the modules were tested up to 150 A and 600 V, as specified in the datasheet. The I-V characteristics of the packaged devices obtained by different chip-attach techniques were similar. All the switching waveforms at transient (both turn-on and turn-off) were clean. The defined parameters were measured, which were also similar. The results from electrical characterization showed that either static characterization or double-pulse test could not be used for evaluating the performance of the different chip-attach techniques, since there was no obvious difference.

Chapter 4. THERMAL CHARACTERIZATIONS OF IGBT MODULE

The thermal properties of a chip-attach layer play a vital role in the thermal management of the system. The conventional methods for evaluating the thermal properties of the chip attachment are to measure the thermal resistance of the power module. However, these methods can yield only the total value of thermal resistances for the whole structure without any information on the contributions of the individual layer along the heat path. In addition, variables such as the thickness of the thermal interface materials and the ambient temperature could affect the measurement results. With the measurement setup in our lab, the thermal impedances of modules with different chip-attach materials are measured to evaluate the thermal performance and reliability of the joints. By controlling the width of the heating pulse, the depth to which the heat diffuses can be controlled to minimize the interferences of the other layers in the measurement of the thermal impedance of the chip-attach layer.

In this chapter, the methods for measuring junction temperature are reviewed in Section 4. The measurement of gate drive signal, the method used in this work, is introduced in Section 4.2.1. The measurement setup and results are shown in Section 4.2.

4.1. Review of Methods for Measuring Junction Temperature

To measure thermal impedance, it is necessary to get accurate measurements of the junction temperature of the power devices. Thus, the methods for measuring junction temperature are first reviewed.

There are numerous methods for measuring the temperature of an operating semiconductor device. The methods can be broadly placed into three categories: electrical, optical, and physically contacting [63].

In the optical method, the optical properties are used as a thermometer, and naturally emitted radiation, reflected radiation, or stimulated emitted radiation is measured. The advantages of optical methods include very high spatial resolution, ability to measure rapid variations in temperature, and nondestructive testing. Also, temperature maps of the surface of a device can be easily obtained from measurements. Disadvantages are that one must have optical access to the device, something not usually possible if the device is packaged, and the equipment required is often expensive and difficult to use [64].

Physically contacting methods rely on physically contacting the device and include point contacting, such as thermocouples and scanning thermal probes, and multiple contacting or blanket coatings, such as liquid crystals and thermo-graphic phosphors [65]. Disadvantages are that the surface of the device being measured must be available for contacting (thus packaged chips cannot be measured) and the thermal response depends upon the response of the probe, which may be considerably slower than that of the device.

An electrical method was used in this work and is introduced in details in the next section.

4.2. Measurement of Thermal Impedance of IGBT Module by Vge

4.2.1. Principle of Measuring Thermal Impedance by Vge

The forward-voltage of a pn junction is most commonly used to measure the junction temperature and further calculate the thermal impedance of chip-attach joints [66]:

$$\frac{dV_{pn}}{dT} = -\gamma \frac{k}{q} + \frac{(V_{pn} - E_g / q)}{T} \tag{1}$$

where q is the electron charge (1.6×10^{-19} C); k is Boltzmann's constant (1.381×10^{23} J/^{o}K), V_{pn} is the voltage across the junction, T is the temperature, γ is a constant equal to about 3, and E_g is the band-gap of silicon (1.12 eV at 275^{o}K).

Restricted by the properties of silicon material, the slope value (K-factor) of a pn junction is around 2 mV/°C [21]. The K-factor of IGBT is above 10 mV/°C, which shows that V_{ge} is much more sensitive than the pn junction voltage for measuring thermal impedances. Thus, in this work, V_{ge} is used to measure the thermal impedance, according to the following equation, and the details of equation (2) can be found at [21]:

$$Z_{th}(t_h) = \frac{V_{ge\_i} - V_{ge\_f}(t_h)}{K \cdot P} \tag{2}$$

4.2.2. Measurement Setups

In this work, two setups were used for the measurements of thermal impedance: one with chiller (liquid cooling at 25°C) and the other without chiller.

Figure 46 (a) shows the hardware of the setup without chiller. The module is mechanically connected to the interface board by screws. Figure 46 (b) shows a cross section of the setup. The power generated by the IGBT goes through the entire stack of materials and into the air by convection.

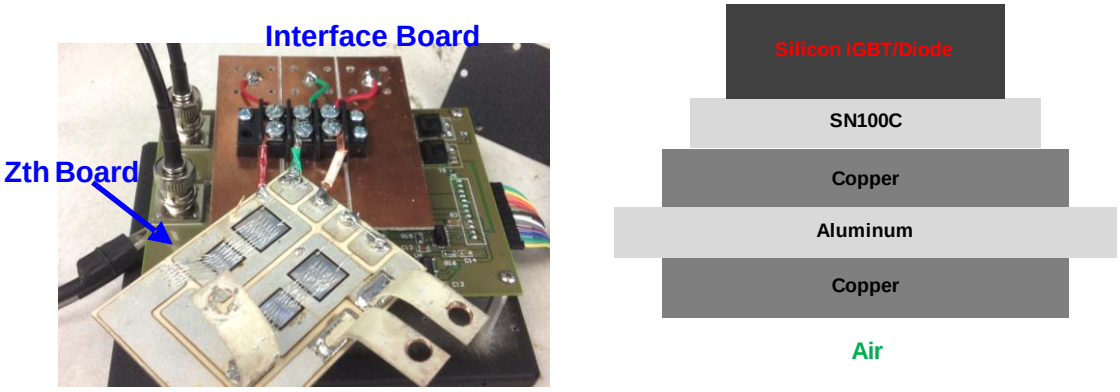


Figure 46. Setup (a) for measuring thermal impedance without chiller, and its cross section (b).

The typical heat transfer coefficients of air range from 10 to 100 W/(m^2·°K). Thus, R_{air} is within the range of 2.42°K/W to 24.24°K/W. The thermal resistance for heat convection from the bottom copper to the air may be much larger than the sum of previous layers.

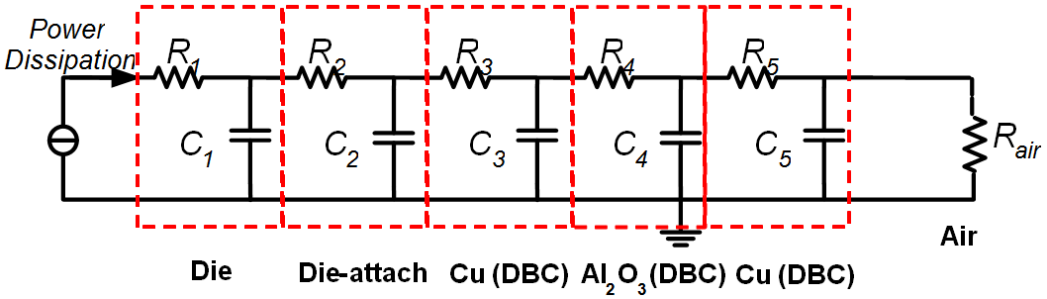


Figure 47. Thermal model for thermal impedance measurement without chiller.

To measure the thermal resistance of each module, we need a constant temperature ground, onto which modules can be attached by thermal grease. Figure 48 shows a cross section of the setup for measuring the thermal impedance of a half-bridge module in ABB application note. A heat sink is used as the constant temperature ground.

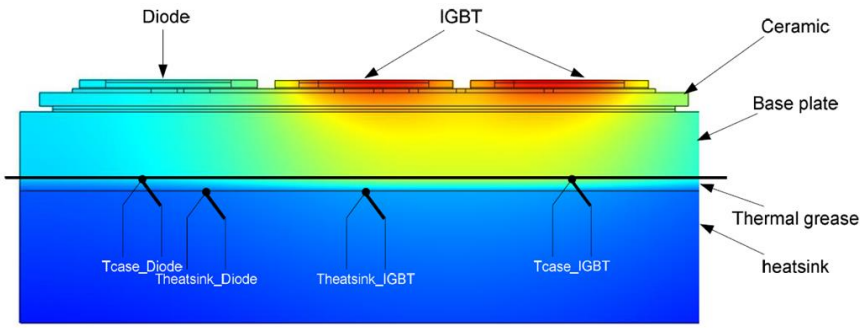


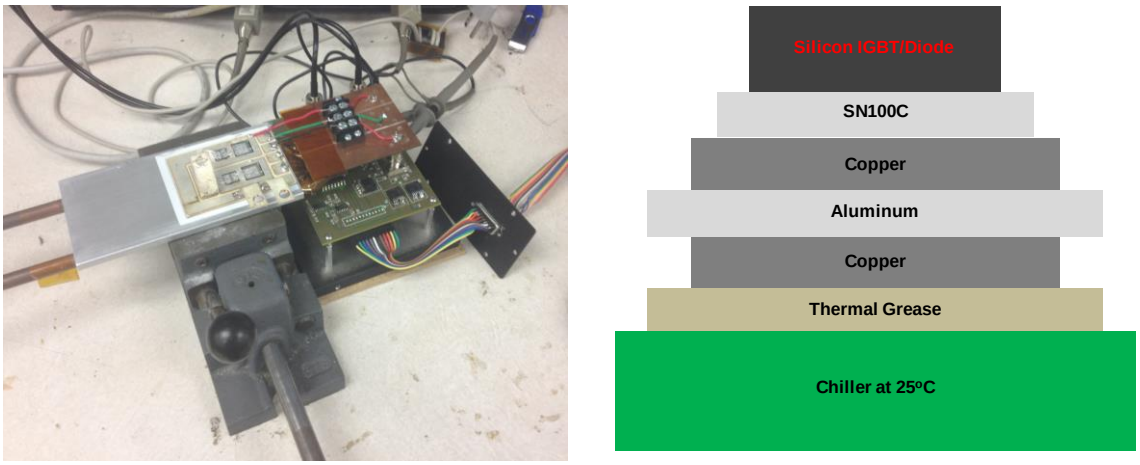
Figure 48. Cross section of setup for measuring thermal impedance of half-bridge module in ABB application note. ([59] ABB Switzerland Ltd. (2013). Application note 5SYA 2059-04: Applying IGBT and Diode dies [online]. Available: http://www.abb.com) Used under fair use, 2013.

The setup with chiller for measuring thermal impedance is very similar to the setup in ABB application note. The difference is that no base plate and solder were used in this work. The DBC substrate of each module is directly attached to the chiller with thermal grease. As shown in Figure 49 (a), a layer of thermal grease [56] with a thickness of about 56 μm, which is the thickness of one layer of Kapton tape, is printed on the chiller. Figure 49 (b) shows the setup with chiller.

(a) (b)

Figure 49. Thermal grease is printed on the chiller as shown in (a), and then connected to the measurement board for thermal impedance as shown in (b).

A close view of the setup with module is shown in Figure 50 (a). In this setup, the heat generated by the IGBT goes through all the layers of materials and is absorbed by the chiller.



(a) (b)

Figure 50. Close view of setup (a) for measuring thermal impedance with chiller, and its cross section (b).

The corresponding thermal model is shown in Figure 51. The calculated thermal resistance of the thermal grease (3.8 W/^{o}K·m) is much lower than 0.1^{o}K/W.

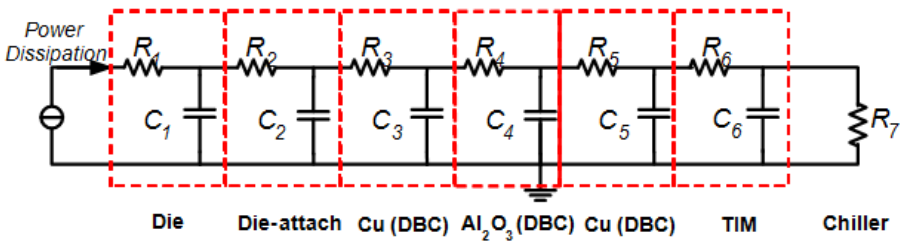


Figure 51. Thermal model for thermal impedance measurement with chiller.

4.2.3. Comparison of Thermal Impedances between Pressure-Free Sintered Modules and Other Modules

The thermal impedance results are shown in Figure 52. The impedances for all three kinds of modules still keep increasing at 40 seconds. The test was stopped at this point, since longer times of heating may damage the IGBT.

The module with pressure sintered joints has a lower thermal impedance than the other two kinds of modules at the same time of measurement, while the thermal impedance of the module with pressure-free sintered joints (Nano-T) is nearly 0.8°K/W higher than that of the soldered module after 5 seconds.

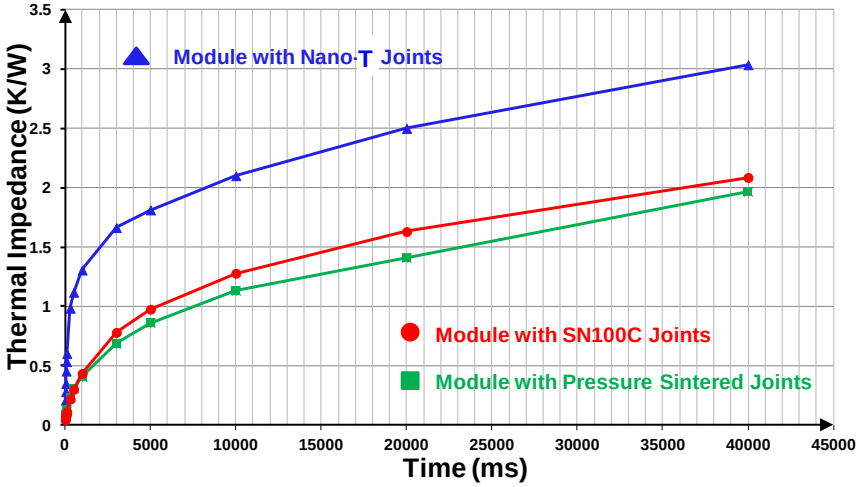


Figure 52. Results of thermal impedance (starting from IGBT junction) vs. time for the above three different kinds of modules (measured without chiller).

Figure 53 compares the thermal impedance results of the pressure sintered module with and without chiller. It shows that the thermal impedance measured with chiller

reaches a constant value, which is the thermal resistance from the IGBT junction to the chiller, after 15 seconds.

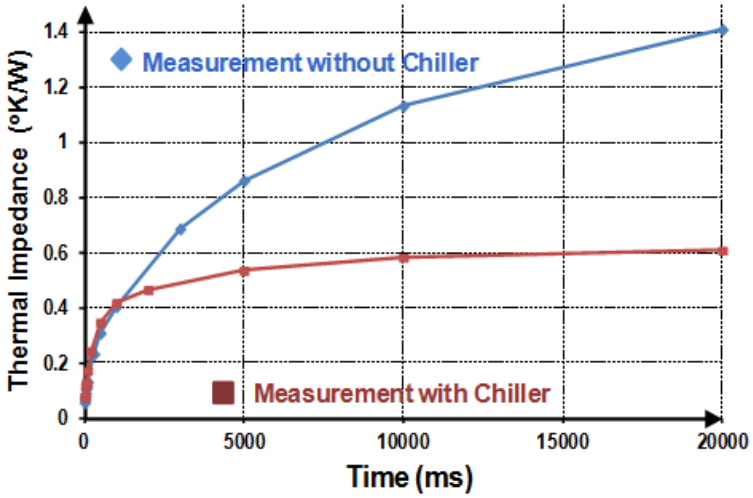


Figure 53. Comparison of thermal impedance results of pressure sintered module with and without chiller.

Figure 54 compares the thermal impedances of all three kinds of modules with chiller. All three modules have similar time constants, but quite different thermal resistances. The thermal resistances of the pressure sintered module, soldered module, and pressure-free sintered module are around 0.609°K/W, 0.964°K/W, and 2.30°K/W, respectively. Nano-X curves were module with modified paste, named nano-X.

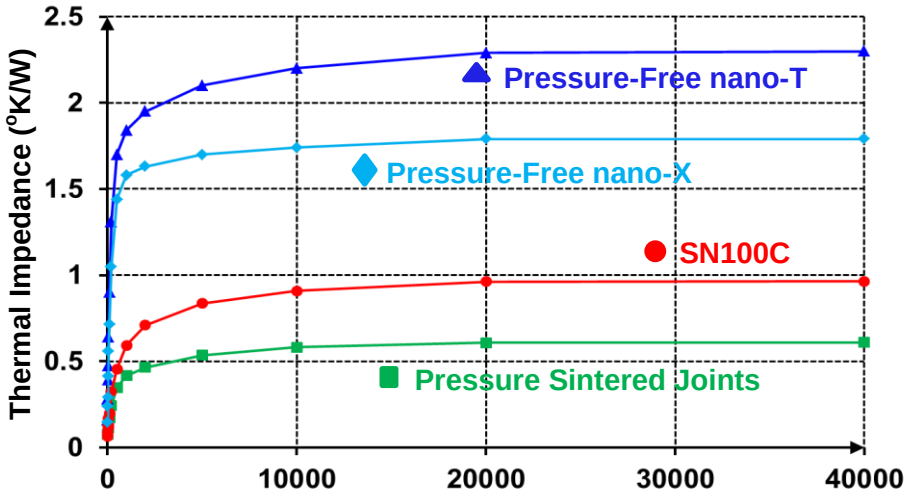


Figure 54. Results of thermal impedance (starting from IGBT junction) vs. time for three different kinds of modules (measured with chiller at 25°C).

4.3. Conclusions

In this chapter, the common methods for measuring junction temperature are first reviewed. Then a method for measuring transient thermal impedance by Vge is introduced and is used in this work. Two setups for thermal measurements are used: one with the IGBT module left in the air and the other with the IGBT module attached to a chiller (liquid cooled and temperature controlled at 25^{o}C). Measured without chiller, the thermal impedance still increases after 40 seconds, since the thermal resistance of heat convection from the bottom copper to the air is much larger the sum of thermal resistances in the previous layers. In contrast, the thermal impedance becomes almost constant after 15 seconds when a chiller is used. For both measurements with and without chiller, the module with pressure sintered joints has the lowest thermal impedance and a final thermal resistance around 0.609^{o}K/W (measurement with chiller). In contrast, it is around 0.964^{o}K/W for the soldered module, and 2.30^{o}K/W for the pressure-free sintered module. The thermal impedance (at 40 ms) and thermal resistance of the three kinds of module are summarized in TABLE X.

TABLE X. SUMMARY OF THERMAL IMPEDANCE (AT 40 MS) AND THERMAL RESISTANCE

	Thermal Impedance (at 40 ms) (^{o}K/W)	Thermal Resistance (^{o}K/W)
Solder (SN100C)	0.126	0.964
Pressure-Sintered Silver	0.102	0.609
Pressure-Free Sintered Silver	0.489	2.30

Chapter 5. CONCLUSIONS AND FUTURE WORK

5.1. Main Contributions and Conclusions

1. Pressure-Free Sintering of Nanosilver Paste for Attaching Large Chips

Before this work, the nanosilver paste from NBE Tech [13] has already been widely studied. However, the main achievements of this work focused on attaching large chip (7.8 mm × 7.8 mm) by sintering under pressures lower than three to five MPa, or attaching small chip (3.5 mm × 5.5 mm) without any applied pressure. In this work, a nanosilver paste with a modified composition from NBE Tech was first tested for attaching chips as large as 13.5 mm × 13.5 mm without any applied pressure. The module fabricated by this technique went through wire bonding (35 pieces of wire bonds on one piece of IGBT), and electrical static test at 125^{o}C and double-pulse test (heating and cooling between room temperature and 125^{o}C for about ten cycles). The pressure-free sintered joints had the threshold strength for joining the chip and the substrate, even though the joints may not yet be reliable for commercial manufacturing.

2. Electrical Characterization of Chip-Attach Joints

IGBT modules, each with a different kind of chip-attach joint, went through the basic electrical characterizations: static performance and double-pulse test. No obvious difference in results can be observed between the modules with different joints. All the modules were tested at the rated current and voltage level: 150 A and 1200 V.

3. Thermal Characterizations of Pressure Sintered Joints for Attaching Large Chips

Pressure sintered joints for attaching large chip have previously been found to provide a more reliable chip-attach joint than lead-free solder from mechanical or thermo-mechanical test. This work extends the study to the thermal and electrical characterizations of pressure sintered joints for attaching large chips. We found that

pressure sintered joints have better thermal performance than solder joints by vacuum reflow for attaching 13.5 mm × 13.5 mm joints.

4. Measurements of Thermal Impedance and Thermal Resistance

In this work, the thermal resistance of packaged modules was also measured. A chiller was used to provide the constant temperature reference. From the results of thermal impedance measurements, IGBT modules with different kinds of chip-attach joints had almost the same time constant. The module with pressure-sintered silver joints had the lowest thermal impedance and thermal resistance (about 0.609^{o}K/W versus about 0.964^{o}K/W for a soldered module). The module with pressure-free sintered joints had the worst thermal performance (a thermal resistance of about 2.30^{o}K/W) among the three.

5. Fabrication of Multi-Chip Modules

The work also describes the fabrication of IGBT multi-chip modules by vacuum reflow of solder, pressure sintering of silver, and pressure-free sintering of silver. It should be noticed that there is a 210 μm difference between the thickness of an IGBT and that of a diode. This difference in thickness creates a potential problem for pressure sintering, since the uniform distribution of pressure during sintering is an important issue for this chip-attach technique.

6. Lead-Frame Attachment by Pressure Contact

Two methods for lead-frame attachment were evaluated in this work: soldering and pressure contact. In the results of double-pulse test, no obvious difference in the switching performance in the transient stage could be found between these two methods.

5.2. Future Work

1. Characterization of Joints after Thermal or Power Cycling

To check the thermal reliability of pressure sintered joints, it is worthwhile to fabricate single-IGBT modules for thermal or power cycling. It is also worthwhile to compare the performance of sintered silver with that of high-temperature solder.

2. X-Pattern for Printing

As mentioned in [25], X-pattern has been studied for printing chip-attach materials, such as the Henkel silver paste (SSP2000). It is worthwhile to combine this technique with pressure sintering or pressure-free sintering of nanosilver paste.

3. Comparison of Thermal Performances with Double-Sided Module

Double-sided module is also a recent hot topic in power electronic packaging. It is worthwhile to compare the thermal and mechanical performance of a wire bonded module with those of a double-sided module. Careful designs should be made for a fair comparison of the two structures.

APPENDIX A: FABRICATION SETTINGS

Settings for several processes (laser cutting, etching, chip-attachments, and wire bonding) are summarized in Table XI.

TABLE XI. SETTINGS FOR MODULE FABRICATION

Machine	Process	Settings	Value
Laser cutting machine: Resonetics CO_2 Laser	Patterning Kapton	Stage lasing velocity (inch/s)	0.6
		Stage lasing velocity (inch/s)	1
		Pulse spacing (inch)	0.002
		Laser power (W)	5
		Pulse number	10
	Cutting Al_2O_3 (0.6 mm thick)	Stage lasing velocity (inch/s)	0.06
		Stage lasing velocity (inch/s)	1
		Pulse spacing (inch)	0.0006
		Laser power (W)	38
		Pulse number	300
	Cutting Cirlex (0.5 mm thick)	Stage lasing velocity (inch/s)	0.03
		Stage lasing velocity (inch/s)	1
		Pulse spacing (inch)	0.0006
		Laser power (W)	25
		Pulse number	100
Etching machine: Kepro BTD-201B	Etching copper	Etching time for 12 mil copper (minutes) Preheat for 30 minutes	30
Vacuum reflow machine: SST MV-2200	Reflowing of SN100C solder	Temperature profile	Shown in Figure Figure 16
Home-made hot-pressure	Nanosilver paste (K series)	Temperature profile	Shown in Figure Figure 17
Hot plate	Nanosilver paste (X series)	Temperature profile	Shown in Figure Figure 18
Wire bonding machine: Orthodyne M20B	Wire bonding of 10-mil aluminum wire	First bonding time (ms)	4
		First bonding power (mW)	250
		Second bonding time (ms)	8
		Second bonding power (mW)	280

APPENDIX B: ELECTRO-PLATING OF SILVER

The electro-plating of Ag is divided into two steps. The first step is the activation of sample surface with a "Silver Strike" plating bath. This plating bath contains a high concentration of cyanide ions and a low concentration of silver ions. By applying "high" current density between the sample and the anode (silver plate), silver ions will attack the sample surface and form a very thin yet porous silver layer. This step has to be very short, up to 30 seconds, so that the porous silver structure would not be too thick to create a weak adhesion problem. The plating bath for the second electro-plating step contains a higher concentration of silver ions than the plating bat for the first step. The plating current density is only half of that used in the strike process. The plating time is about 10 to 15 minutes.

TABLE XII. COMPONENTS AND CONDITIONS OF SILVER STRIKE SOLUTION [44]

Used under fair use, 2013

Silver cyanide	6.6 g/L
Potassium cyanide	75 g/L
Potassium carbonate	15 g/L
Temperature	Room temperature
Current density	20 - 25 mA/cm^2
Duration	Up to 30 seconds
Anode	Silver plate

TABLE XIII. COMPONENTS AND CONDITIONS OF SILVER PLATING SOLUTION

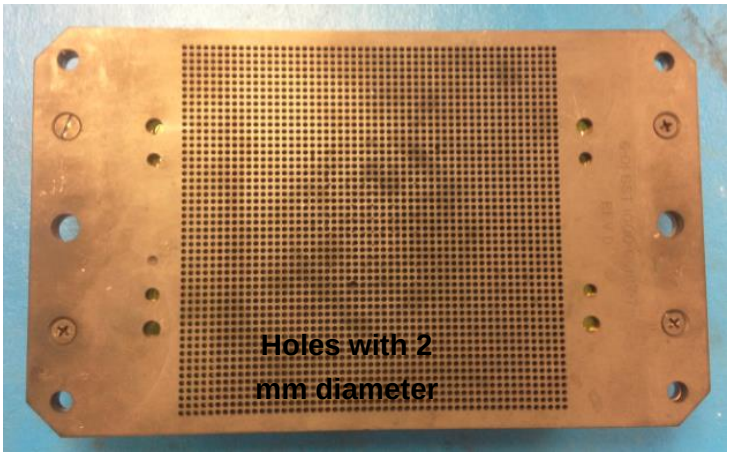
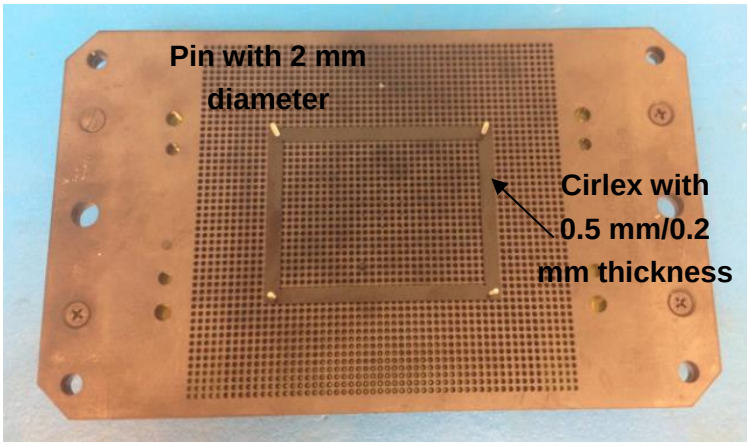
Used under fair use, 2013

Silver cyanide	36 g/L
Potassium cyanide	60 g/L
Potassium carbonate	45 g/L
Temperature	Room temperature
Current density	10 mA/cm^2
Duration	15 minutes for 8.5 μm
Anode	Silver plate

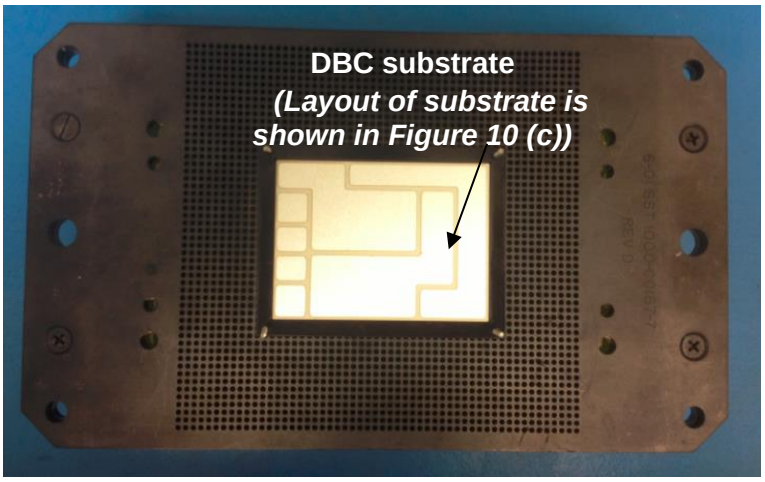
APPENDIX C: ASSEMBLY OF COMPONENTS FOR VACUUM REFLOW

The assembly of components for vacuum reflow is important because the melting of solder may lead to the rotation or movement of chips. Fixture (TABLE XIV) that can withstand high process temperatures was used in this work to fix the location of chips.

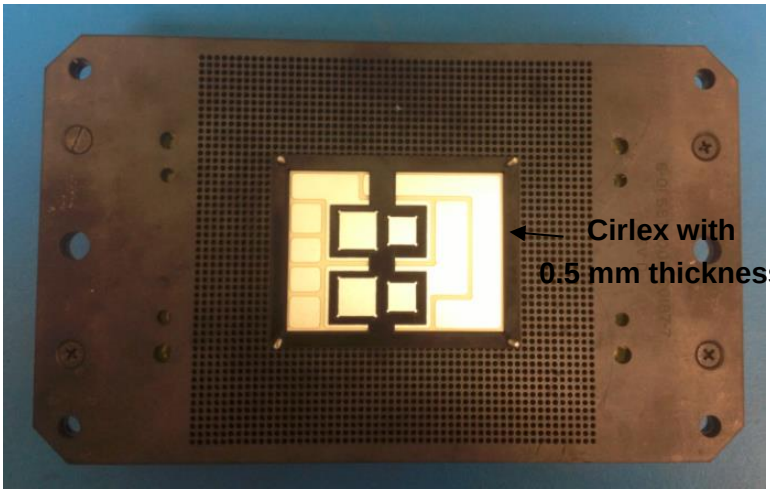
TABLE XIV. STEPS OF ASSEMBLY OF VACUUM REFLOW

	Hardware
Step One Select Graphite Boat	
Step Two Add Cirlex Fixture for DBC	

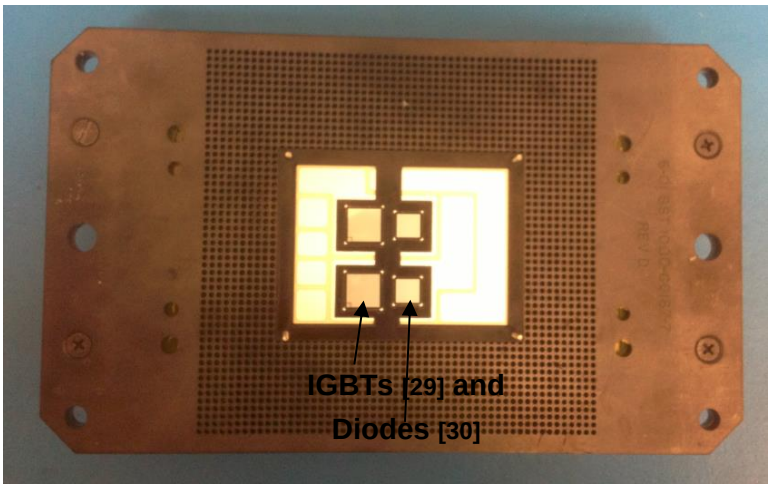
Step Three
Add DBC



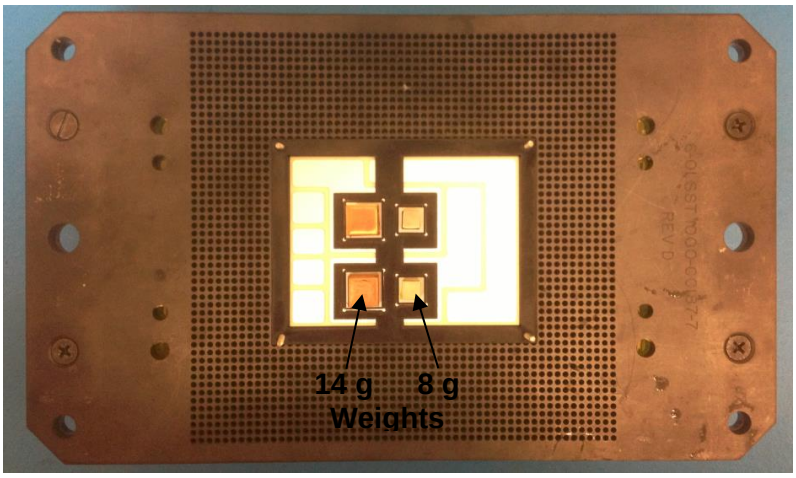
Step Four
Add Cirlex Fixture
for Chips



Step Five
Add Chips



Step Six
Add Weights



A cross section of the assembly for vacuum reflow is shown in Figure 55. The thicknesses of the fixtures were selected based on the thicknesses of the DBC, joints, and chips. The fixtures were fabricated by laser-cutting according to the profile shown in Table XI.

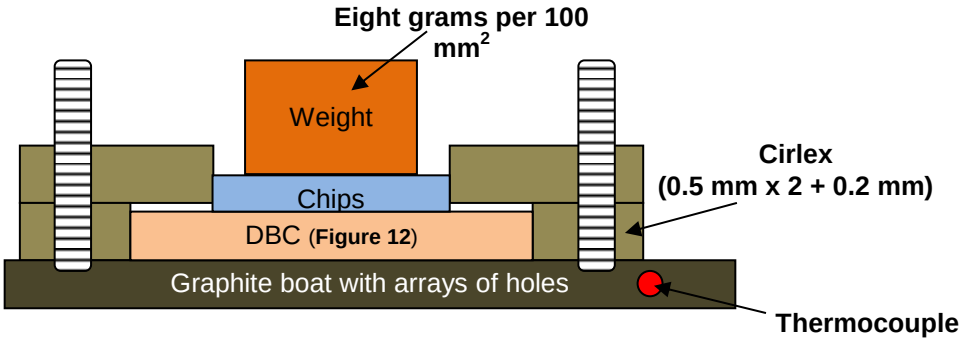


Figure 55. Cross section of assembly for vacuum reflow.

APPENDIX D: SETUPS OF DOUBLE-PULSE TESTER

Details of the components of the double-pulse tester are recorded in TABLE XV.

TABLE XV. COMPONENTS OF DOUBLE-PULSE TESTER

Equipment	Manufacturer	Model	Key Features
Oscilloscope	Tektronix	TDS7054	500 MHz 5 GS/s
Digital Multimeter	Agilent	34405A	1000 VDC
DC Power Supply (for Gate Driver)	Agilent	E3631A	0 - 6 V, 5 A/0 - 25 V, 1 A
DC Power Supply (for DC-Link Voltage)	Sorensen	DCR 600-4.5b	800 VDC
Shunt Resistor	T&M Research	W-1-01-2 stud	0.01 Ω, 12.5 W
Thermometer	OMEGA	HH23	Accurate to 0.1°C
Inductor	AMCC (Core)	800B, D-08	Saturation around 220 A
Decoupling Capacitor	Cornell Dubilier	SCD305k122c3-24	3.0 μF, 1200 VDC
DC-Link Capacitor	Cornell Dubilier	9472601K801CCMS	600 μF, 800 VDC

A piece of home-made PCB board is fabricated to provide connections between the components in Table XV.

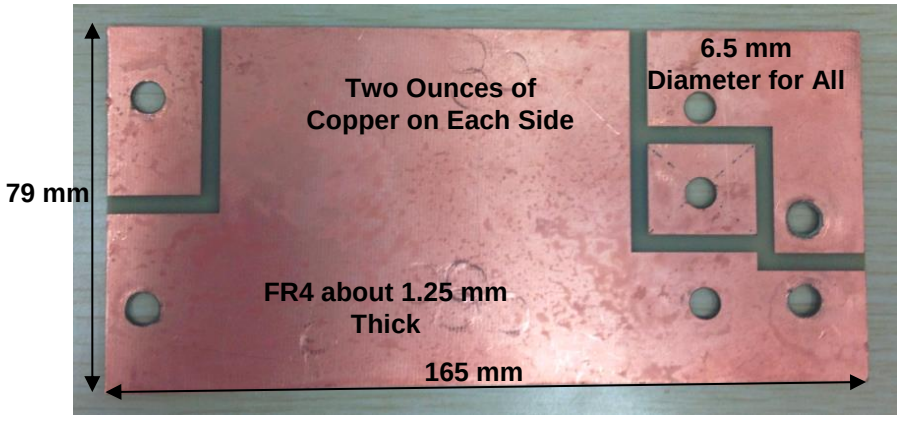


Figure 56. Home-made PCB board for connecting components.

List of Publications

PAPER UNDER REVIEW

[1] L. Jiang, G.Y. Lei, K. D. T. Ngo and G.-Q. Lu, “Evaluation of Thermal-Cycling Reliability of Sintered Nano-silver versus Soldered Joints by Curvature Measurement,” Submitted to Transactions on Components, Packaging and Manufacturing Technology on May 1, 2013.

PAPER TO BE SUBMITTED

[1] L. Jiang, G-Q. Lu, and K. D. T. Ngo, “Effects of Symmetry and Shape of Joints on Failure in Double-Sided Module”

DISCLOSURES FILED

[1] K. D. T. Ngo, L. Jiang, “ Process of One-Step Soldering to Form Multiple Solder Layers with Controllable Shapes”

CONFERENCE PAPERS

[1] L. Jiang, G.-Q. Lu, and K. D. T. Ngo, “Thermo-Mechanical Reliability of Nano-Silver Sintered Joints versus Lead-Free Solder Joints for Attaching Large Area Silicon Devices,” in Proc. SAE Power Syst. Conf., Nov. 2010.

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[1] W.D. Brown and R. K. Ulrich, *Advanced Electronic Packaging with Emphasis on Multichip Modules,* IEEE Press, 2006.

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