Electrical Integration of SiC Power Devices for High-Power-Density Applications

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Abstract

The trend of electrification in transportation applications has led to the fast development of high-power-density power electronics converters. High-switching-frequency and high-temperature operations are the two key factors towards this target. Both requirements, however, are challenging the fundamental limit of silicon (Si) based devices. The emerging wide-bandgap, silicon carbide (SiC) power devices have become the promising solution to meet these requirements. With these advanced devices, the technology barrier has now moved to the compatible integration technology that can make the best of device capabilities in high-power-density converters. Many challenges are present, and some of the most important issues are explored in this dissertation.

First of all, the high-temperature performances of the commercial SiC MOSFET are evaluated extensively up to 200 ℃. The static and switching characterizations show that the device has superior electrical performances under elevated temperatures. Meanwhile, the gate oxide stability of the device – a known issue to SiC MOSFETs in general – is also evaluated through both high-temperature gate biasing and gate switching tests. Device degradations are observed from these tests, and a design trade-off between the performance and reliability of the SiC MOSFET is concluded.

To understand the interactions between devices and circuit parasitics, an experimental parametric study is performed to investigate the influences of stray

inductances on the MOSFET's switching waveforms. A small-signal model is then developed to explain the parasitic ringing in the frequency domain. From this angle, the ringing mechanism can be understood more easily and deeply. With the use of this model, the effects of DC decoupling capacitors in suppressing the ringing can be further explained in a more straightforward way than the traditional time-domain analysis. A rule of thumb regarding the capacitance selection is also derived.

A Power Electronics Building Block (PEBB) module is then developed with discrete SiC MOSFETs. Integrating the power stage together with the peripheral functions such as gate drive and protection, the PEBB concept allows the converter to be built quickly and reliably by simply connecting several PEBB modules. The high-speed gate drive and power stage layout designs are presented to enable fast and safe switching of the SiC MOSFET. Based on the PEBB platform, the state-of-the-art Si and SiC power MOSFETs are also compared in the device characteristics, temperature influences, and loss distributions in a high-frequency converter, so that special design considerations can be concluded for the SiC MOSFET.

Towards high-temperature, high-frequency and high-power operations, integrated wire-bond phase-leg modules are also developed with SiC MOSFET bare dice. High-temperature packaging materials are carefully selected based on an extensive literature survey. The design considerations of improved substrate layout, laminated bus bars, and embedded decoupling capacitors are all discussed in detail, and are verified through a modeling and simulation approach in the design stage. The 200 ℃, 100 kHz continuous operation is demonstrated on the fabricated module. Through the comparison with a commercial SiC phase-leg module designed in the traditional way, it is also shown that

the design considerations proposed in this work allow the SiC devices in the wire-bond structure to be switched twice as fast with only one-third of the parasitic ringing.

To further push the performance of SiC power modules, a novel hybrid packaging technology is developed which combines the small parasitics and footprint of a planar module with the easy fabrication of a wire-bond module. The original concept is demonstrated on a high-temperature rectifier module with SiC JFET. A modified structure is then proposed to further improve design flexibility and simplify module fabrication. The SiC MOSFET phase-leg module built in this structure successfully reaches the switching speed limit of the device almost without any parasitic ringing.

Finally, a new switching loop snubber circuit is proposed to damp the parasitic ringing through magnetic coupling without affecting either conduction or switching losses of the device. The concept is analyzed theoretically and verified experimentally. The initial integration of such a circuit into the power module is presented, and possible improvements are proposed.

To my dearest wife

Yiying Yao

And

My beloved parents

Haixing Chen and Jinhua Liu

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Chapter 1 Introduction

1.1 Application Background

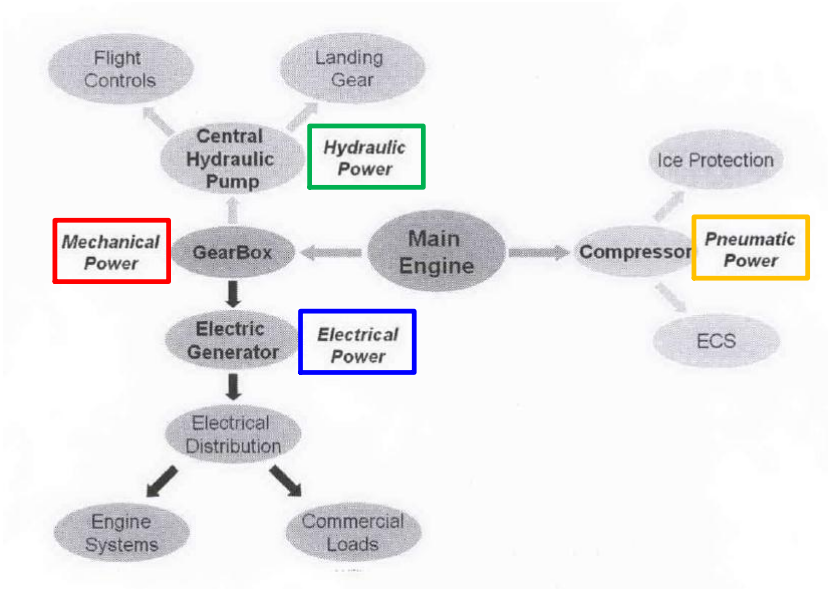
Transportation nowadays accounts for over 20% of the total energy-related emissions [1]. With an increasing concern on the energy crisis and environment conservation, there has been a global trend to reduce the fuel consumption and air pollution in modern transportation applications, such as cars, airplanes, and ships, etc. Towards this target, more and more electrical and electronic features are now being adopted in vehicles to improve not only the fuel economy and emission, but also the system performance, safety, convenience, and passenger comfort [2]. As a result, the electrical loads and the demand for electrical power have been growing continuously in the transportation industry, leading to the fast developments of electric vehicles, more electric airplanes, and electric ships.

Take the airplane industry for example. Traditionally, a civil airplane consists of non-propulsive subsystems driven by four different types of secondary power: Hydraulic, pneumatic, electrical, and mechanical powers. Each type of power obtains the energy from the main engine in a different discipline, and serves different loads and functions on the aircraft, as illustrated in Figure 1-1 (a) [3][5][6]. Nowadays, each subsystem has

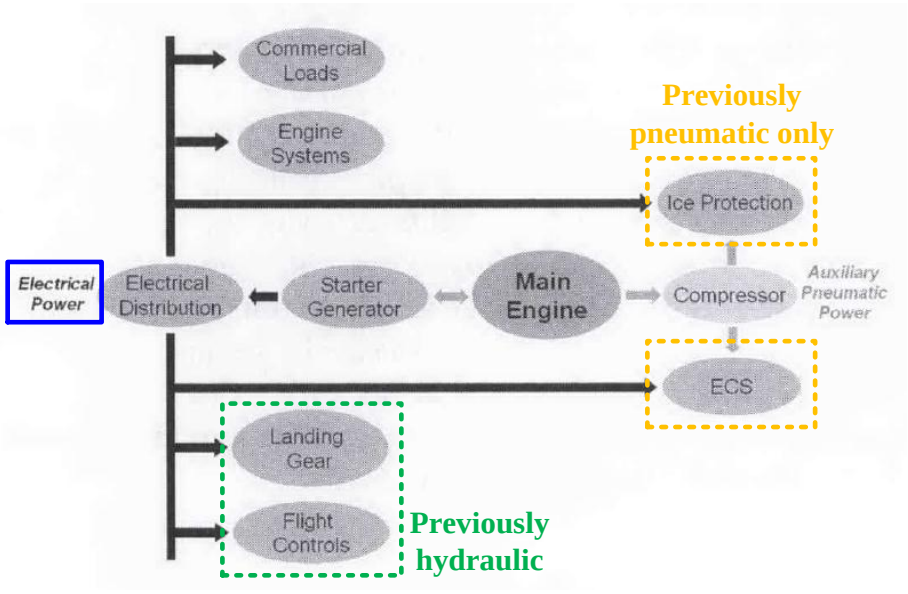
become more and more complicated, and the interactions between different pieces of equipment reduce the overall efficiency of the whole system. Therefore, a current trend for today's advanced airplanes is going "more electric", where the traditional hydraulic, pneumatic and mechanical loads are being replaced by electrical loads, and the electrical power is more extensively used to drive the non-propulsive subsystems, as shown in Figure 1-1 (b) [2][4][7]-[9]. Two good examples following this trend are Airbus 380 and Boeing 787. The advantages of more electric airplanes (MEA) are obvious: The system architecture is simplified; the overall performance is improved; higher efficiency and reliability can therefore be achieved; and most importantly, a great amount of fuel consumption and CO_2 emission can be saved [2]-[4][8]-[10]. Similar stories are also happening for electric vehicles [11] and electric ships [12]. It therefore can be anticipated that power electronics converters will be more and more widely utilized in these applications to distribute energy from sources to loads.

In these applications, being high-power-density is a critical design target for the power electronics converters, since the volume and weight of the power conversion systems onboard will have a great impact on the transport capability and fuel economy of vehicles. The increase of power density is mainly achieved by increasing the converter switching frequency, which helps reduce the sizes and weights of passive components (capacitors, inductors, transformers, and EMI filters, etc.) for the same voltage and current ripples. Approximately, the power density of a converter can be doubled if its switching frequency is increased by a factor of ten [13]. The state-of-the-art Si IGBTs, which are the dominant devices in today's transportation power conversion systems, are

typically switched below 50 kHz due to their bipolar nature [16][18]. It is thus desirable to use even faster switches in power converters to further improve the power density.



(a)



(b)

Figure 1-1. Conventional (a) and more-electric-aircraft (b) power distribution architectures [3]

Another way towards higher power density is through operating power semiconductor devices at higher junction temperatures, thus requiring a smaller and lighter cooling system, which is also a major weight contributor in power converters [14]. In hybrid electric vehicles (HEVs), for instance, a 65 ℃ cooling loop is specially designed in addition to the 105 ℃ engine coolant to dissipate the heat from power converters, which are limited to operation below 175 ℃ junction temperature with Si IGBTs. This means that, if power switches capable of 200 ℃ operation are available, the low-temperature cooling loop can be totally eliminated, and the cost and complexity of HEVs can be reduced significantly [15]-[17]. In MEAs, on the other hand, there even exists a trend to mount the embedded generators, together with their power electronics units, directly onto the engine shafts as a starter and a generator to replace bulky and heavy mechanical parts. This would directly expose the power converters to the engine compartment environment and require the power modules to work in an ambient temperature of 200 to 250 ℃, far beyond the limit of Si devices [2][19].

From either the high-frequency or high-temperature point of view, today's increasing demand for higher power density has approached the fundamental limits of the Si technology. The emerging wide-bandgap silicon carbide (SiC) power semiconductor devices are believed to be the game changer in the future power conversion systems to meet this demand.

1.2 SiC Power Semiconductor Devices

As a wide-bandgap material, SiC offers a critical electric field of 2.0 MV/cm – an order of magnitude higher than that of Si. This significantly increases the blocking capability of SiC power devices, and also allows them to be fabricated with much thinner

and more highly doped drift layers, which greatly reduces the on-state resistance. As a result, high-voltage (≥ 1.2 kV) SiC unipolar switches, such as JFETs and MOSFETs, have become realistic to offer much faster switching speeds than the traditional high-voltage Si devices, which have to be made in bipolar structures (e.g. BJT or IGBT) due to the material limit, without sacrificing the conduction loss. Moreover, the high thermal conductivity of SiC (4.9 W/cm·K) improves the device's heat dissipation, and, along with the wide bandgap energy (3.3 eV), allows high-temperature operation above 300 ℃ in theory [20]-[23]. The main properties of Si and SiC materials are compared in Table 1-1 [20].

Table 1-1. Comparison of Si and SiC Material Properties

Parameter	Si	4H-SiC	Unit
Bandgap energy	1.1	3.3	eV
Relative permittivity	11.8	10	-
Critical electric field	0.3	2.0	MV/cm
Electron saturated drift velocity	1.0	2.0	$\times 10^7$ cm/s
Thermal conductivity	1.5	4.9	W/cm·K

The advantages of SiC have urged the commercialization of SiC Schottky barrier diodes with blocking voltages over 600 V by Infineon and Cree since 2001, which feature ultra-fast turn-on speed and almost zero reverse recovery effect compared to regular Si PiN diodes [22][29][30]. For SiC active switches, on the other hand, the main research focus has been directed on the unipolar devices of JFETs and MOSFETs from 600 V up to approximately 2 kV, with 1.2 kV devices being the mainstream [23]. Both 1.2 kV SiC JFETs and MOSFETs have become commercially available since early 2011, from SemiSouth and Cree respectively (Although SemiSouth has been out of business since

early 2013) [30][31]. Compared to Si IGBTs, these devices provide much better performances in both on-state resistances and switching speeds, and meanwhile, the possibility of high-temperature operation over 200 ℃. All of these advantages have made SiC power devices an ideal substitution for Si in future transportation applications to meet the power density requirement [2][24]-[28].

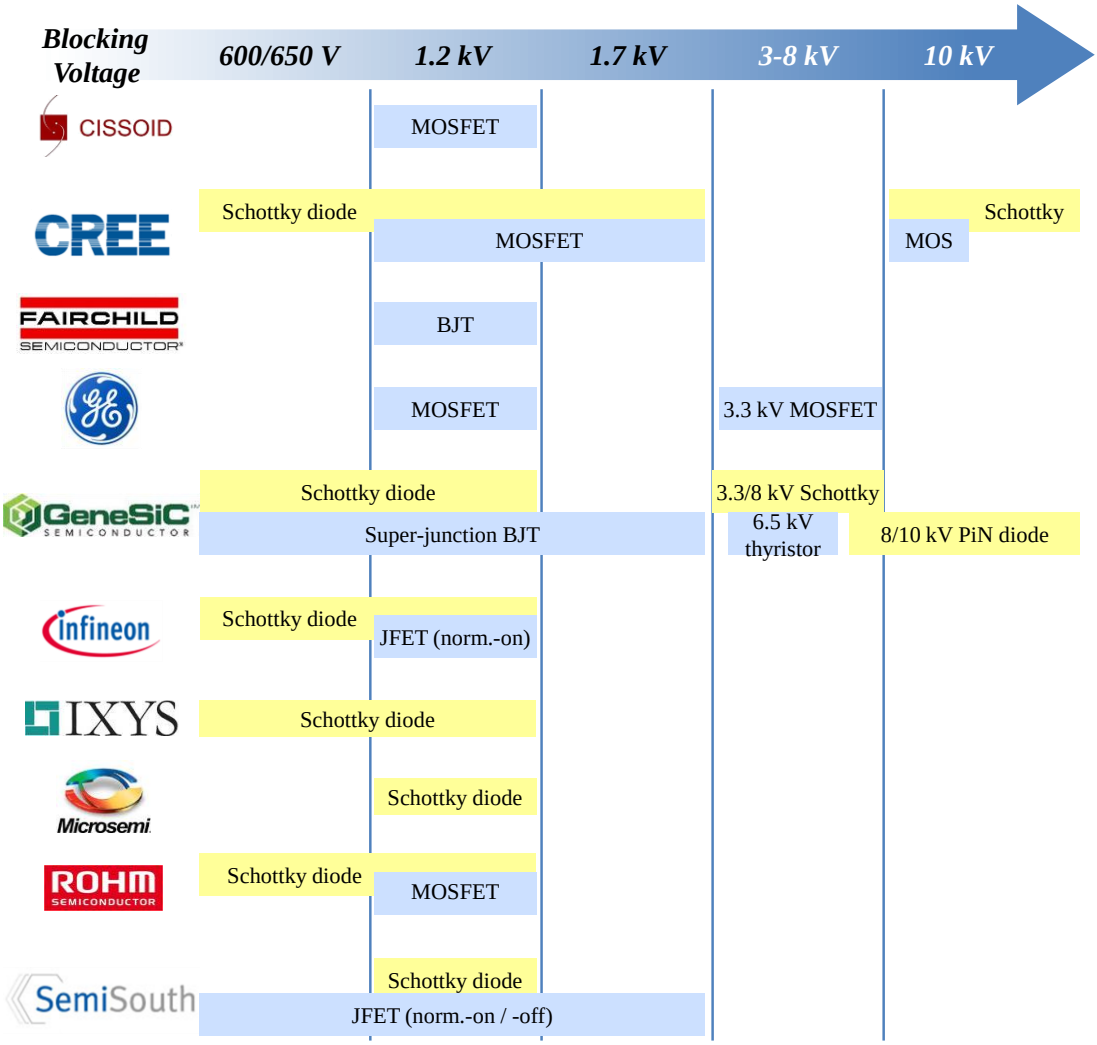


Figure 1-2. Major SiC developers and their focuses. Information is updated to Sept. 2013

Further researches in SiC devices are still continuing on increasing blocking voltage [32]-[35], enlarging single-chip die size [36], developing high-temperature

bipolar switches [37][38], and last but not least, understanding and improving performances and reliability of current commercial products. Figure 1-2 summarizes the main SiC device developers and their focuses based on the published literatures and the company's website information. The scope of this work will be focused on 1.2 kV SiC devices which are most suitable for the voltage and power levels in transportation applications.

1.3 Research Motivations and Objectives

It is obvious from the previous discussion that high temperature and high frequency are the two most critical factors towards a high power density. Both capabilities are ultimately driven by the advancement in semiconductor devices. Between the commercial SiC active switches, SiC MOSFETs are usually preferred over JFETs due to their more desirable normally-off feature and easier gate-driving capability. The commercial MOSFETs, however, are conservatively rated up to only 135 ℃ maximum junction temperature by the manufacturer, mainly limited by its plastic package [39]. Device characteristics above this temperature are therefore missing in the datasheet. Moreover, unlike SiC JFETs whose high-temperature characteristics have been studied extensively, there are not too many publications talking about the high-temperature performances of SiC MOSFETs, and the published results are either incomplete or insufficient in explaining the device behaviors. What is also missing from either the datasheet or publications is whether and how the characteristics of SiC MOSFETs will degrade under both high-gate-voltage and high-temperature stresses due to the well-known gate oxide stability issue. In this sense, there is still not enough evidence or data to support the high-

temperature operations of commercial SiC MOSFETs. Further characterizations are therefore necessary to better understand the device behaviors.

While SiC unipolar switches have taken a large leap in switching frequency, they also turn the parasitic elements in the circuit, e.g. package stray inductances, to become the bottleneck that impedes higher switching speed. Under the existence of these parasitics, faster switching transients are always penalized by more severe device over-voltages and electromagnetic noises due to the parasitic ringing. The interactions between the device and circuit parasitics have been studied through a variety of methods, e.g. analytical calculations, simulation, and experiments, etc., all in the time domain. Using the most basic switch-pair circuit, initial conclusions have been drawn about the influences of stray inductances on device's switching waveforms, but still in a very complicated and time-consuming way. Furthermore, the time-domain analysis will become even less effective in more complex situations, for example, when DC decoupling capacitors are introduced to suppress ringing. A frequency-domain method thus needs to be explored to obtain a deeper insight into the mechanism of parasitic ringing, and, in the meanwhile, simplify the analysis. Such a study will be able to provide very useful layout design guidelines when integrating devices into power modules.

Speaking of device conduction and switching losses, it is commonly acknowledged that SiC MOSFETs are superior to Si IGBTs in both aspects. However, it is not so easy to tell the differences between SiC MOSFETs and their Si counterparts. Device users may wonder whether the old knowledge about Si MOSFETs can be readily applied to SiC ones, since they are both "MOSFETs". The answer is not as straightforward as just comparing datasheets, since these devices are operated under quite different gate-driving

and switching voltage/current conditions, and are influenced by the temperature quite differently. A comprehensive comparison between the two technologies in all major device characteristics is thus necessary to pinpoint the special design considerations for SiC MOSFETs, and their different impacts on converter performances.

Towards high-temperature and high-frequency power converters, the compatible integration technology plays an equally important role to the semiconductor devices. SiC power modules have become commercially available to catch this trend, but these modules are still designed in the same manner as the conventional, wire-bond, Si IGBT ones [40][41]. This means that the module package still cannot sustain high ambient temperatures over 150 ℃, and that the stray inductances are still preventing SiC devices from switching to their speed limit. The gap between powerful devices and high-power-density converters thus needs to be filled by properly designing the SiC wire-bond power modules with the suitable packaging materials and the optimized internal layout.

While the planar packaging is the direction of research for future high power modules to ultimately get rid of bonding wires and their associated stray inductances for ultra-fast switching speed, the technology is still far from industrial implementations due to many manufacture and reliability issues. For this reason, the double-sided solderability of semiconductor chips, a critical feature to the planar packaging, is still not available on today's SiC devices. It is thus meaningful to explore and develop a new packaging structure, which combines the 3-dimensional layout of a planar module with the easiness and maturity of wire-bond interconnections, as an intermediate step towards planar modules. Such a "hybrid" module should be able to be fabricated with the currently

available technology and devices, but in the meanwhile provide much better performance than the traditional wire-bond modules.

To address the above issues, this dissertation is organized as follows.

Chapter 2 presents the static and switching characterizations of a commercial 1.2 kV SiC MOSFET up to 200 ℃. Discussions are provided to explain some of its special temperature behaviors. The gate oxide stability of the device in high-temperature environments is also tested under both gate biasing and gate switching conditions. The degradations in the device's critical parameters are captured from the tests, and their influences on device operations are discussed.

Chapter 3 firstly investigates the influences of stray inductances on the switching waveforms of a power MOSFET through an experimental parametric study. A deeper understanding of the common source inductance is obtained from this study. After that, a small-signal model is derived to reach a deeper insight into the parasitic ringing mechanism at device turn-off. Using this model, the effect of decoupling capacitors in suppressing the ringing can be explained easily in the frequency domain, and a rule of thumb regarding the capacitance selection is also derived.

Chapter 4 presents the development of a Power Electronics Building Block (PEBB) with discrete devices. The PEBB integrates not only the power stage, but also the necessary gate-driving, sensing, and protection functions, so that converters can be built with PEBB modules quickly and reliably. The gate drive and PEBB layout designs for fast switching purposes are discussed in detail in this chapter. Using the same PEBB, a comprehensive comparison is then conducted between the SiC MOSFET and its Si counterpart. The two devices are compared in detail in their static/switching

performances, temperature influences, and finally, loss distributions in a high-frequency DC-DC converter.

Chapter 5 presents the development of two wire-bond-based, SiC MOSFET phase-leg modules capable of both high-temperature and high-frequency operations. An extensive literature survey on packaging materials is firstly conducted to find out the right combination for the high-temperature package. The module structure is then optimized based on a modeling and simulation approach to minimize the parasitic effects from the substrate layouts and power terminals. The 200 ℃, 100 kHz operation of the module is verified experimentally. The switching performances of the developed module are also compared to those of a commercial product. Thanks to the optimized design, the developed module exhibits much better performances with 2x faster switching speed and only 1/3x parasitic ringing.

In Chapter 6, a novel hybrid packaging technology is developed to provide a compromise between the wire-bond and the planar structures. The hybrid module can achieve the same footprint and similar package parasitics compared to a planar module, but is easier to fabricate since it does not require double-sided solderability for the semiconductor devices. The original concept is implemented on a high-temperature, three-phase rectifier module with SiC JFET, whose 250 ℃ operation is later demonstrated successfully in experiment. A modified hybrid structure is then proposed to further simplify fabrication and improve reliability of the module. A SiC MOSFET phase-leg module is developed in this structure. It is shown that the device's switching speed can be pushed to its very limit in this package without suffering from excessive parasitic ringing and over-voltages.

Chapter 7 proposes a new switching loop snubber circuit that provides extra damping to the parasitic ringing without increasing either conduction or switching losses of the device. The concept is first analyzed using the small-signal model developed in Chapter 3, and then verified through experiments. The initial integration of such a circuit in the power module, and the possible improvements in future researches, are all discussed in this chapter.

Finally, Chapter 8 summarizes the main conclusions of this dissertation and proposes potential future work.

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[40] Powerex, QJD1210010 1200 V, 100 A split dual SiC MOSFET module datasheet, available online at http://www.pwrx.com/.

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Chapter 2 High-Temperature Characteristics of SiC Power MOSFETs

2.1 Introduction

The advantages of SiC power switches are driving the development of power converters into two directions: Being high-temperature, and/or being high-switching-frequency. From the temperature point of view, the conventional Si MOSFETs or IGBTs are limited in their junction temperatures up to 150-175 °C, above which both their static and switching characteristics deteriorate significantly and become unacceptable in actual converter implementations. SiC power devices, in comparison, exhibit much better characteristics and performances even under temperatures over 200 °C [1]-[3]. Many previous efforts have shown the superior characteristics and reliable operations of SiC JFETs under over 200 °C junction temperatures [4]-[12]. However, fewer publications can be found on the high-temperature performances of SiC MOSFETs, and these results are still incomplete or insufficient in analysis to explain the device behaviors [13]-[15].

The first-generation commercial SiC power MOSFET, rated at 1.2 kV and 33 A, was introduced by Cree in early 2011. The maximum junction temperature (T_{Jmax}) of the device, however, is conservatively rated at only 135 °C by the manufacturer, due to the

limitations of the plastic package [16]. Device characteristics above this temperature are therefore missing in the datasheet. What is also missing from either the datasheet or publications is whether and how the device characteristics will degrade under both high-gate-voltage and high-temperature stresses due to the well-known gate oxide stability issue of the SiC MOSFET [26][28]. In this sense, the high-temperature performances of this commercial device still remain unclear and thus require further evaluation.

In this chapter, the commercial 1.2 kV, 33 A SiC MOSFET (Cree CMF20120D) is characterized extensively up to 200 °C. The results show the superior static and switching performances of the device under elevated temperatures. Discussions are also provided to explain some of its special temperature behaviors. The gate oxide stability of the device in high-temperature environments is then tested under both gate biasing and gate switching conditions. The degradations in the device's critical characteristics are captured from the tests, and their influences on the device operations are also discussed.

2.2 High-Temperature Characteristics of SiC Power MOSFETs

All major static characteristics of the device under test (DUT) are measured using a Tektronix 371B curve tracer, with the DUT (in the commercial TO-247 package) mounted on a hotplate to regulate its junction temperature. The detailed characterization process is documented in [17].

2.2.1 Blocking Capability

The blocking capability of the device is evaluated by its leakage current I_{DSS} under the rated voltage with the gate-source terminals shorted. As seen in Figure 2-1, I_{DSS} only slightly increases with the temperature, and is measured below 10 μA at all temperature

points. This indicates a very good blocking capability of the SiC MOSFET over a wide temperature range, especially when compared to the conventional Si switches whose leakage currents usually increase significantly as the temperature goes above their T_{Jmax} around 150 ℃ [14].

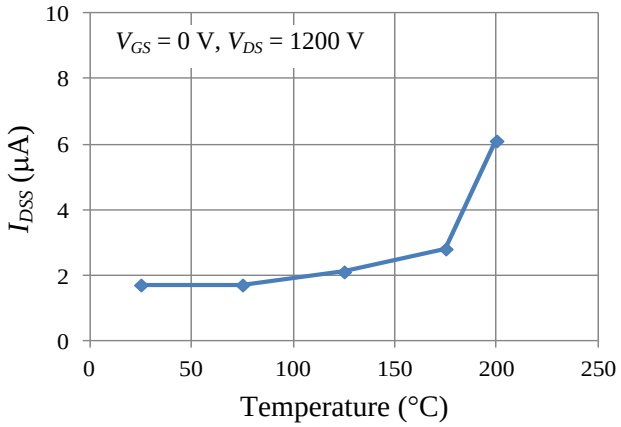


Figure 2-1. Leakage current vs. temperature

2.2.2 Static Characteristics

The measured output characteristics are shown in Figure 2-2. As seen, the temperature dependence of the *I-V* curves is quite different from that of conventional Si MOSFETs. At low gate voltages (e.g. V_{GS} = 8 V), the slope of the *I-V* curve keeps increasing with the temperature, indicating a higher conductivity. At the full gate voltage of 20 V, on the contrary, the *I-V* curve always shifts to the right, showing a monotonously increasing on-state resistance $R_{DS(on)}$. There are also intermediate gate voltages (e.g. V_{GS} = 14 V) at which $R_{DS(on)}$ will first reduce and then increase. This special characteristic is due to the competing temperature dependences of the channel resistance R_{CH} and bulk resistance R_{Bulk} inside the device. For the 1.2 kV SiC MOSFET, R_{CH} is comparable to R_{Bulk}, and under certain conditions may even dominate the overall $R_{DS(on)}$. For the

temperature range of concern in this work, the device channel mobility increases monotonously with the increasing temperature, resulting in a constantly decreasing R_{CH} at a given V_{GS}. The electron mobility in the drift region, however, decreases with the increasing temperature, causing R_{Bulk} to change in the opposite direction [18][19]. The temperature behavior of $R_{DS(on)}$ ($\approx R_{CH} + R_{Bulk}$) is then determined by the ratio of R_{CH} and R_{Bulk} at the corresponding V_{GS}.

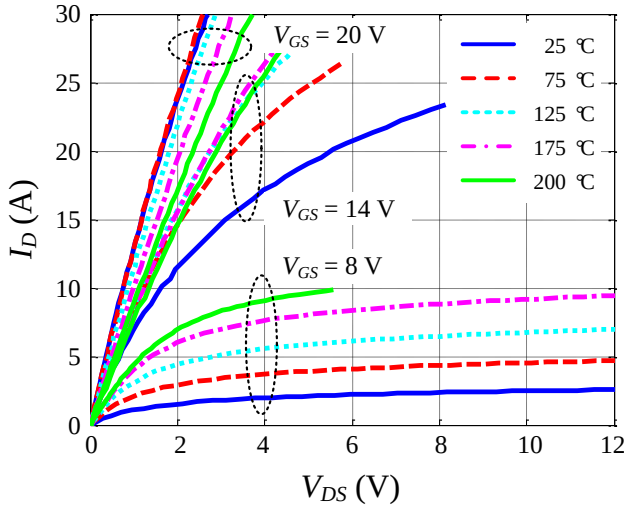


Figure 2-2. Temperature-dependent output characteristics

The $R_{DS(on)}$ vs. temperature curves at two different V_{GS} are plotted in Figure 2-3. The U-shaped curve at V_{GS} = 16 V clearly shows the decreasing effect of R_{CH} below around 100 ℃, beyond which R_{Bulk} starts to dominate and $R_{DS(on)}$ starts increasing. This result is consistent with the analysis in [19]. At higher V_{GS} of 20 V, R_{CH} diminishes, and $R_{DS(on)}$ exhibits a monotonously increasing trend from 25-200 ℃. It is important to note that, according to [19], the competing effect of R_{CH} and R_{Bulk} still exists, but the valley point of $R_{DS(on)}$ falls below 25 ℃ at V_{GS} = 20 V.

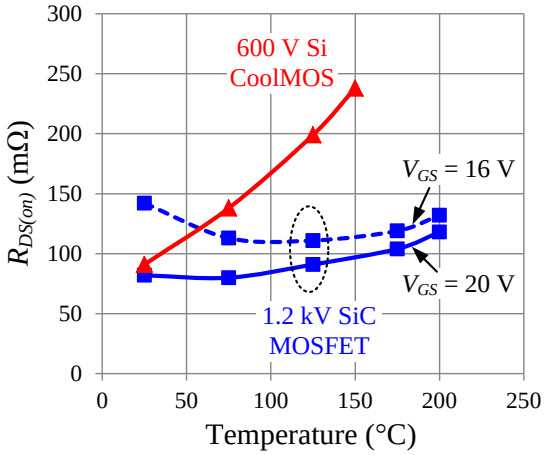


Figure 2-3. On-state resistances vs. temperature

This special characteristic is actually beneficial in lowering the temperature sensitivity of $R_{DS(on)}$ of the SiC MOSFET. When compared to a state-of-the-art Si CoolMOS with half the voltage (600 V) but similar current ratings, the SiC MOSFET exhibits not only lower $R_{DS(on)}$ at the room temperature, but also much less temperature dependence over a wider temperature range, as shown in Figure 2-3. One can further infer from this figure that, if comparing to Si MOSFETs of the same voltage rating, the advantage of SiC MOSFET in $R_{DS(on)}$ would be even more obvious. However, a higher turn-on voltage of 20 V, compared to the usual 10 V for Si MOSFETs, is required for the device to achieve lower conduction loss, and to ease parallel operation from 25-200 ℃.

The device's transfer characteristics are shown in Figure 2-4. Similar to Si MOSFETs, a decreasing trend in the gate threshold voltage $V_{GS(th)}$ can be observed, causing the *I-V* curve to shift left. A more accurate measurement shown in Figure 2-5 indicates that $V_{GS(th)}$ drops from 2.3 V at room temperature to only 1.4 V at 200 ℃. Considering its fast switching speed, the SiC MOSFET usually requires a negative turn-off bias to increase the threshold margin and *dv*/*dt* immunity, in order to avoid the false-triggering in phase-leg operations.

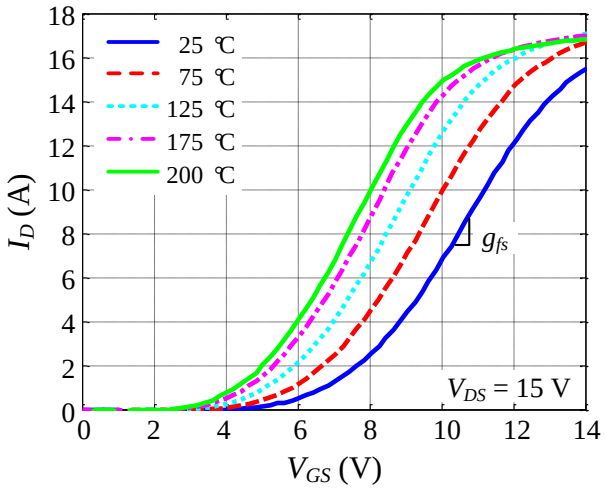


Figure 2-4. Temperature-dependent transfer characteristics

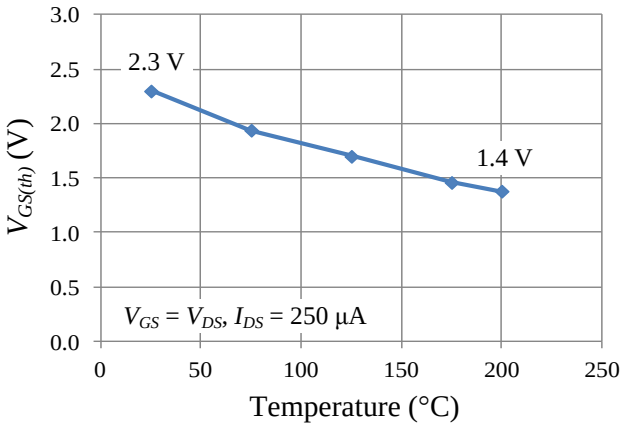


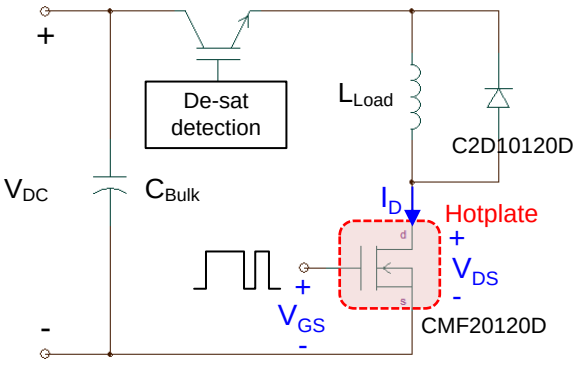
Figure 2-5. Threshold voltage vs. temperature

A usually less emphasized but to some extent more critical parameter of the device is its transconductance g_{fs}. According to Figure 2-4, g_{fs} of the SiC MOSFET increases slightly with the temperature, showing just the opposite trend to that of the Si MOSFET. As this parameter is closely related to the shape of the gate voltage waveform and hence the driving speed, this special trend will consequently cause the switching energies of the SiC MOSFET to exhibit quite different temperature dependence compared to Si.

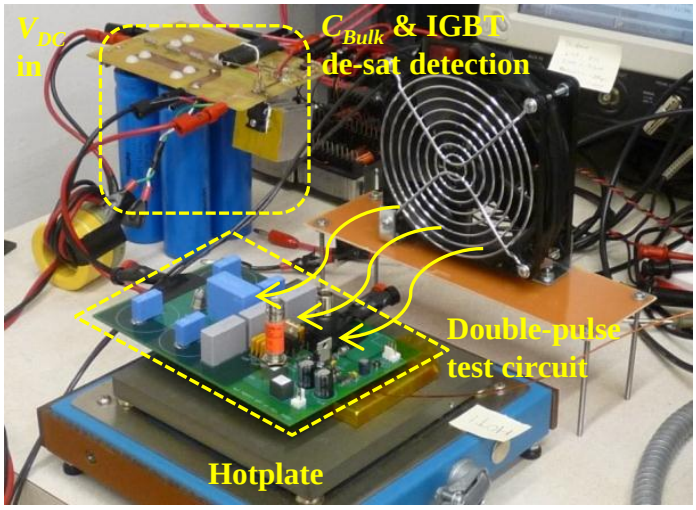
2.2.3 Switching Characteristics

The switching behaviors of the DUT are characterized using the standard double-pulse testing method [17]. Figure 2-6 (a) shows the schematic of the tester. A 1.2 kV, 10 A SiC Schottky diode (Cree C2D10120D) is used as the top freewheeling diode. In order to protect the DUT from any potential over-current failure under high temperature, an IGBT with de-sat detection function is inserted between the bulk capacitors and the tester circuit as a breaker. The entire tester is placed in the room environment, while only the MOSFET alone is heated by a hotplate. Figure 2-6 (b) shows the lab test setup. The DUT (in a TO-247 package) is mounted on a piece of aluminum heat spreader, and soldered onto the bottom side of the tester circuit board. The heat spreader is then placed on the hotplate for heating, and the MOSFET case temperature is measured via a thermocouple. At each temperature point, the device is soaked for a long enough period of time to ensure that the junction temperature is as close to that of the case as possible. In addition, a fan is used to cool down the top surface of the tester PCB, where all the low-temperature peripheral components are located.

The switching tests are conducted under 600 V and varying load currents up to 25 A, and are repeated under several temperatures up to 200 ℃. Figure 2-7 shows the test results at four different temperature points, where the switching waveforms are superimposed and aligned in time to show the influence of temperature. During the turn-on process, a lower plateau voltage $V_{Plateau}$ in V_{GS} can be observed as the temperature rises. Accordingly, slew rates of both the drain voltage V_{DS} and drain current I_D become faster. At turn-off, a lower $V_{Plateau}$ can still be observed, but during this transient both V_{DS} and I_D swings become slower at higher temperatures.



(a)



(b)

Figure 2-6. The double-pulse tester. (a) Circuit schematic, (b) tester setup

The switching energies are calculated based on the experimental waveforms. Figure 2-8 gives the results obtained with 10 Ω gate resistance. Both the turn-on (E_{on}) and turn-off (E_{off}) energies are approximately in linear proportion to the switching current, as shown in the figure. As the turn-on speed gets faster under higher junction temperatures, lower energy is observed for E_{on}. This decrease happens to cancel the increase of E_{off}, resulting in the total switching loss (E_{tot}) curves being almost overlapped for different temperatures. Figure 2-9 plots the switching energies versus temperature for the 600 V,

20 A switching condition, where the temperature effect can be seen more clearly. The same switching characterizations are also repeated with smaller gate resistances and faster switching speeds. Similar results are obtained.

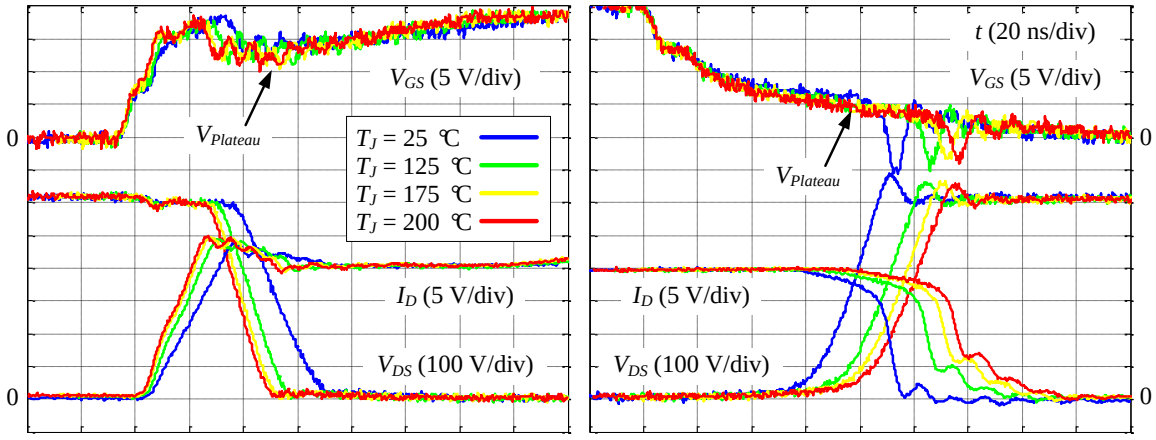


Figure 2-7. Switching waveforms of SiC MOSFET at 600 V, 20 A, with 10 Ω gate resistance (left) Turn-on, (right) turn-off

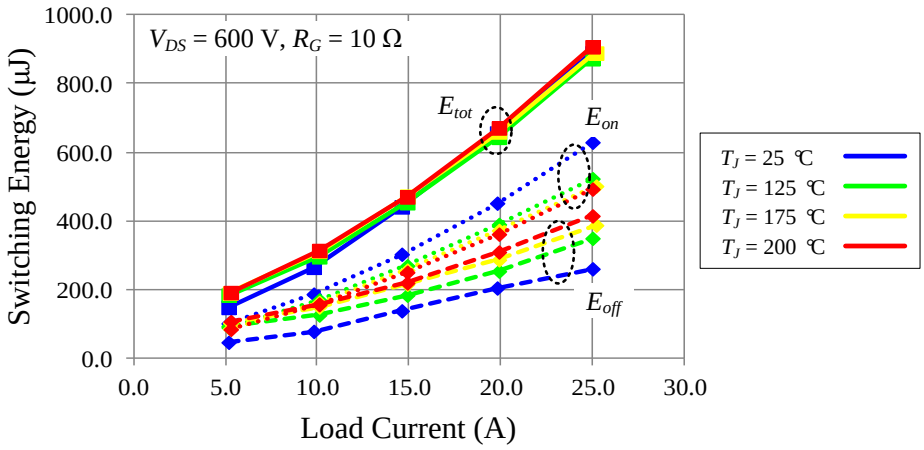


Figure 2-8. Switching energies vs. load current at different temperatures, with 10 Ω gate resistance

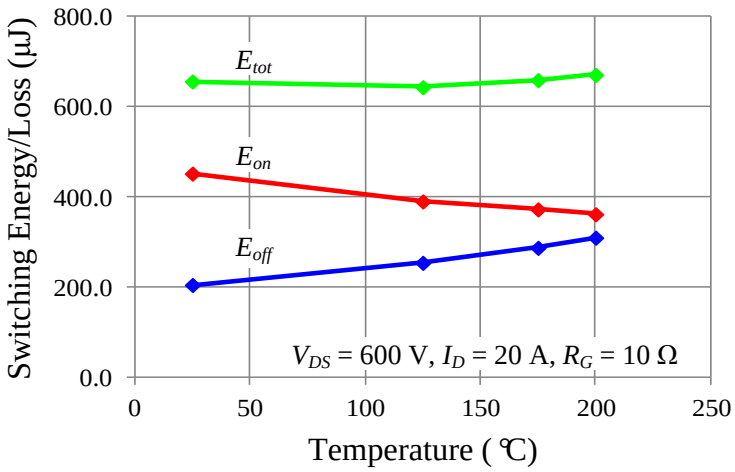


Figure 2-9. Switching energies / loss vs. temperature, with 10 Ω gate resistance

The fact that the turn-on energy reduces under higher junction temperature is contrary to the common knowledge about Si MOSFETs that both E_{on} and E_{off} (and hence E_{tot}) generally increase with the temperature. Considering that the junction capacitances are insensitive to the temperature [13], this special behavior is more closely related to the temperature dependence of the transconductance g_{fs} of the SiC MOSFET.

The MOSFET switching theory can be used to explain this phenomenon. According to [20], the theoretical turn-on process of MOSFET is plotted in Figure 2-10, where four phases can be identified based on the shape of the waveforms. During Phase 1 and 2, the gate driver charges the input capacitance C_{ISS} of the MOSFET through the gate resistance R_G, and V_{GS} starts rising accordingly. V_{DS} and I_D waveforms will not respond in this phase until V_{GS} hits the gate threshold voltage (i.e. the turn-on delay). In Phase 2, V_{GS} keeps rising from $V_{GS(th)}$ until it reaches a voltage plateau $V_{Plateau}$, and meanwhile I_D rises to the full load current. The duration of this phase can be estimated by [17][20]:

$$t_{ir} = R_G C_{ISS} \ln\left(\frac{V_{Drive\_on} - V_{GS(th)}}{V_{Drive\_on} - V_{Plateau}}\right). \quad (2\text{-}1)$$

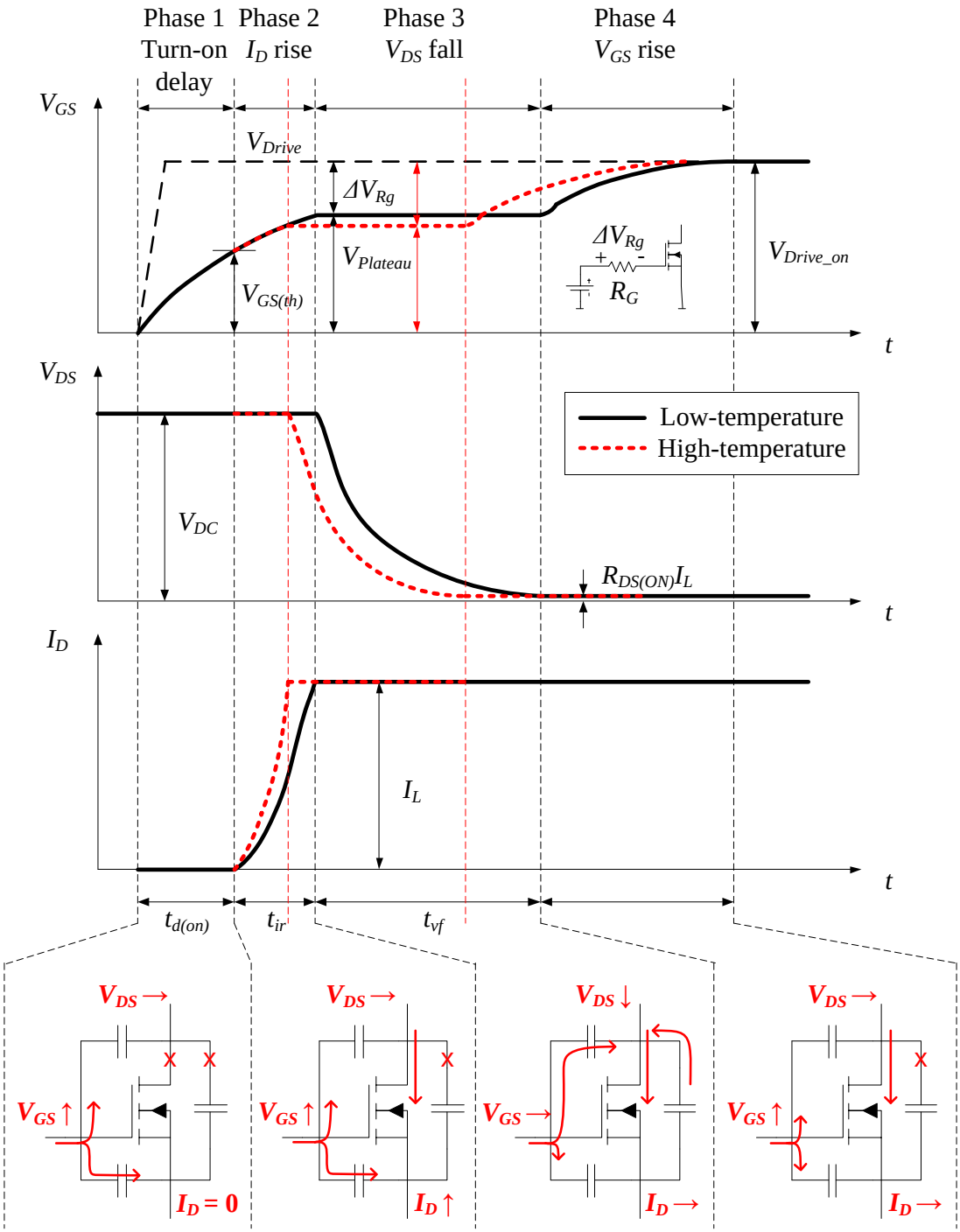


Figure 2-10. Theoretical turn-on process of MOSFET

The height of the plateau level is determined by the load current I_L and the device's transconductance g_{fs} by:

$$V_{Plateau} = g_{fs}^{-1} I_L + V_{GS(th)}. \tag{2-2}$$

In Phase 3, almost all the gate current I_G deviates to discharge the Miller capacitance C_{RSS} due to the Miller effect, and thus V_{GS} stays almost constant at $V_{Plateau}$. During this period, I_G can be calculated as:

$$I_G = \frac{\Delta V_{Rg}}{R_G} = \frac{V_{Drive\_on} - V_{Plateau}}{R_G}. \tag{2-3}$$

Correspondingly, V_{DS} starts to decrease until it drops to its turn-on voltage value, i.e. $R_{DS(on)} \cdot I_L$. The duration of this phase can be estimated by:

$$t_{vf} = \frac{Q_{GD} R_G}{V_{Drive\_on} - V_{Plateau}}, \tag{2-4}$$

where Q_{GD} is the total charge coming from the Miller capacitor.

Because g_{fs} increases and $V_{GS(th)}$ decreases with the temperature for the SiC MOSFET, $V_{Plateau}$ level will be lower at higher temperatures as suggested by Eq. (2-2), which is also observed from the experimental waveforms in Figure 2-7. According to Eq. (2-1), it will then take less time for V_{GS} to rise from $V_{GS(th)}$ to $V_{Plateau}$, and for I_D from zero to I_L, which results in a higher di/dt as shown by the red dashed waveforms in Figure 2-10. During Phase 3, on the other hand, the smaller $V_{Plateau}$ will also enlarge the voltage drop across the gate resistor (ΔV_{Rg}), leading to a higher I_G to discharge the Miller capacitor according to Eq. (2-3). This causes V_{DS} to also drop faster at higher temperatures, resulting in a higher dv/dt.

This explains why the turn-on speed gets faster for the SiC MOSFET as the temperature increases. At turn-off, on the contrary, the sequence of the switching phases is reversed, causing the turn-off delay time, dv/dt, and di/dt to exhibit opposite trends under smaller $V_{GS(th)}$ and $V_{Plateau}$.

2.3 Evaluation of Gate Oxide Stability

There has always been a trade-off between the performance and reliability of SiC MOSFETs ever since their introduction. Compared to their Si counterparts, SiC MOSFETs require a higher gate voltage or higher gate electric field in order to achieve a lower on-state resistance, due to their lower channel mobility [21][22]. However, the smaller effective barrier height of the SiC material, due to its wider bandgap, also makes the SiC MOS structure more vulnerable to the Fowler-Nordheim (F-N) tunneling current even under the same electric field as Si. The F-N current causes time-dependent dielectric breakdown (TDDB) inside the gate oxide layer, leading to oxide defects, and finally the device degradation [22]-[25]. Moreover, a greater density of SiC/SiO_2 interfacial trapped charge has also been reported, which results in non-negligible threshold voltage shifts whenever a voltage bias appears on the gate [22][26]-[29]. In either situation, it can be inferred that the gate oxide stability will be even more adversely affected when both high-gate-voltage and high-temperature stresses exist on the device. However, whether and how the device characteristics, such as I_{DSS}, $R_{DS(on)}$, and $V_{GS(th)}$, etc., will degrade under these conditions have not been reported yet.

Instead of exploring the mechanism, this work mainly focuses on examining the possible degradations in the device's terminal characteristics that are critical for converter operations. Two tests have been conducted, namely the gate biasing test and the gate switching test. In these tests, the DUTs are soaked under a series of temperatures, and the device gate-source terminals are stressed by either a constant voltage of 20 V, or a square waveform from -4 V to 20 V at 70 kHz with 50% duty cycle. Static parameters, such as

$V_{GS(th)}$, I_{DSS}, $R_{DS(on)}$, and input capacitance C_{ISS}, are measured regularly during the tests to capture the possible changes in the device characteristics.

2.3.1 Test Setup

Figure 2-11 shows the schematic of the test circuit. As seen, two DUTs are used for each test condition, and are mounted on the same hotplate to regulate their junction temperatures. Using a relay to change its topology, this circuit achieves two functions. In Figure 2-11 (a), the relay directs the DUT gates to a gate driver, which stresses the device with adjustable voltage waveforms. While in Figure 2-11 (b), the relay shorts the device gate-drain terminals, and the voltage source V_{S2} will generate a DC voltage that produces 1 mA drain current through each DUT. The measured V_{GS} is then the threshold voltage of the MOSFET according to the standard $V_{GS(th)}$ test condition [30].

The test circuit stays in Figure 2-11 (a) state to apply both the temperature and gate voltage stresses. After one hour of stressing, the circuit switches to Figure 2-11 (b) state for threshold voltage measurement, which takes just a few seconds before switching back to (a). This allows $V_{GS(th)}$ to be monitored dynamically during the test without removing the DUTs from the test circuit and the heat source. This process is repeated for 8 cycles (i.e. 8 hours), during which time the relay actions and the measurements are automatically performed by several instruments (i.e. voltage sources, data logger, and signal generator) controlled by Matlab codes over the GPIB bus, as illustrated in Figure 2-12.

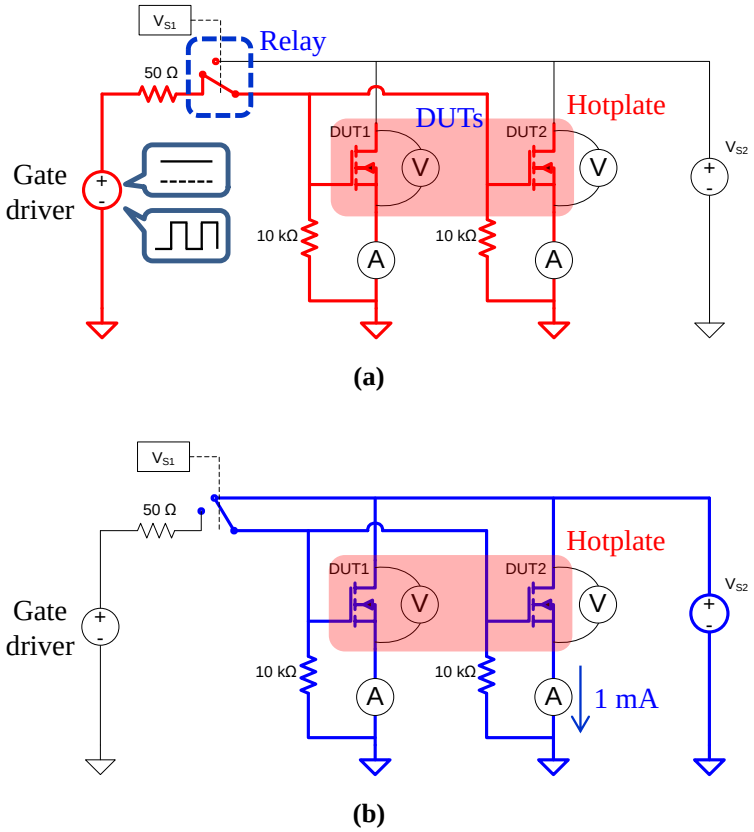


Figure 2-11. Test circuit used to evaluate the gate oxide stability

(a) Circuit that applies the gate voltage and temperature stresses, (b) circuit that measures the threshold voltage at elevated temperatures

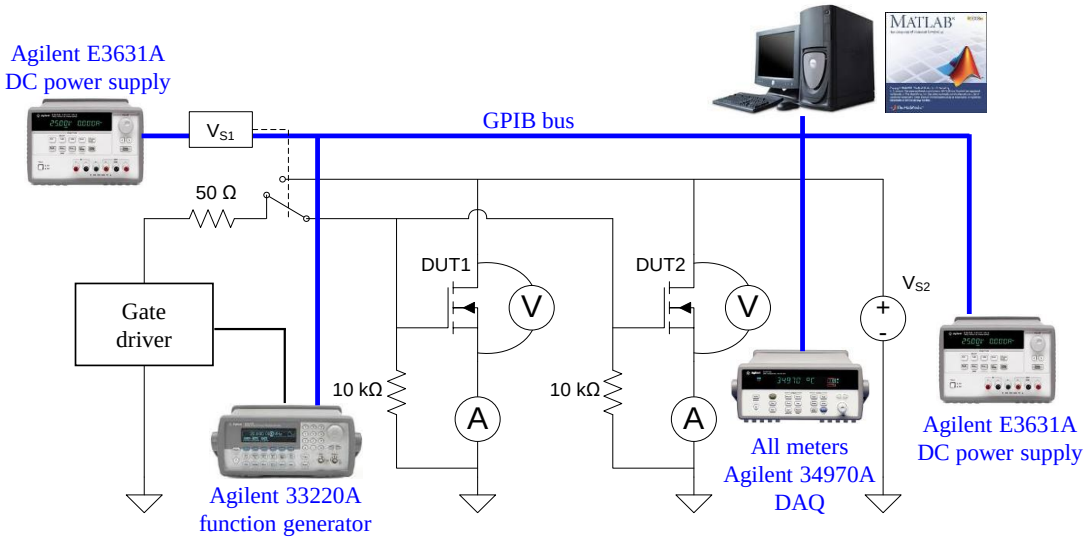


Figure 2-12. Automatic testing system to evaluate the gate oxide stability

After that, the DUTs are cooled down to the room temperature, and the static parameters of $V_{GS(th)}$, I_{DSS}, $R_{DS(on)}$, and C_{ISS} etc., are measured with the curve tracer and the impedance analyzer, so that changes in the other device characteristics can also be captured. The test and measurement conditions are summarized in Table 2-1 for easier understanding.

Table 2-1. Gate Oxide Stability Test and Measurement Conditions

Measured parameters	Interval	Equipment	V_{GS} & T_J conditions
$V_{GS(th)}$	1 hour	Test circuit Figure 2-11 (b)	V_{GS} = gate driver voltage; T_J = hotplate temperature
$V_{GS(th)}$; I_{DSS}; $R_{DS(on)}$; C_{ISS}; output *I-V* curves; transfer *I-V* curves	8 hours	Tektronix 371B curve tracer; & Agilent 4294A impedance analyzer	No gate voltage; T_J = 25 ℃

2.3.2 Gate Biasing Tests

For this test, the DUTs are applied with a 20 V DC gate voltage – the recommended turn-on voltage for the device. The test first starts with two MOSFETs in the commercial TO-247 package. Since T_{Jmax} is only 135 ℃ according to the device datasheet, the soaking temperature for these two samples only goes up to 150 ℃ in the test. Figure 2-13 shows the measured threshold voltage during testing, which is normalized to its room temperature value. The test continues for 24 hours at each temperature point, and a slightly positive shift in $V_{GS(th)}$ can be observed at the end of the test. This trend is consistent with the results presented previously [26]-[28], but the absolute increment is small enough to be neglected (< 0.1 V at 150 ℃). The curve tracer

measurements also show almost no change in the other device characteristics. This result is actually expected, since the highest temperature here is just 15 ℃ above the rated value.

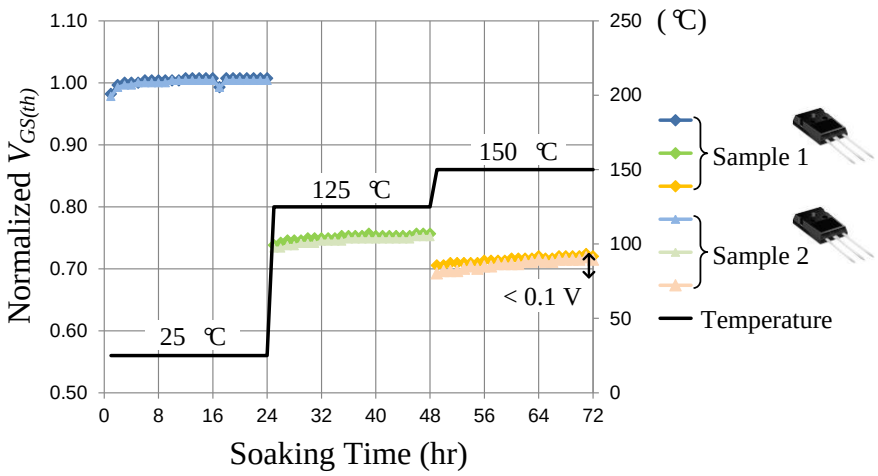


Figure 2-13. Normalized threshold voltage measured during the gate biasing test
Test samples are two SiC MOSFETs in the commercial TO-247 package

Besides the discrete devices, a customized high-temperature single-chip package is also designed to hold the SiC MOSFET bare die for the tests above 150 ℃, as shown in Figure 2-14. Using all materials with working temperatures above 250 ℃, this module avoids any potential influence from the plastic TO-247 package during the long-term high-temperature soaking, and allows the DUT junction temperature to reach 200 ℃ easily.

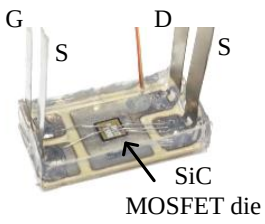


Figure 2-14. Customized high-temperature single-chip module for > 150 ℃ tests

Figure 2-15 shows the gate biasing test results up to 200 ℃ using two high-temperature modules. For the first two 8 hours, the DUTs are soaked under room temperature and 125 ℃ respectively. As expected, no obvious change can be seen in the threshold voltage. However, when the temperature increases to 175 ℃, a maximum of 0.17 V positive shift can be observed from one of the samples, after a time span of 24 hours. For the subsequent soaking at 200 ℃, the threshold shift accelerates and increases by up to 0.3 V after 32 hours of stressing.

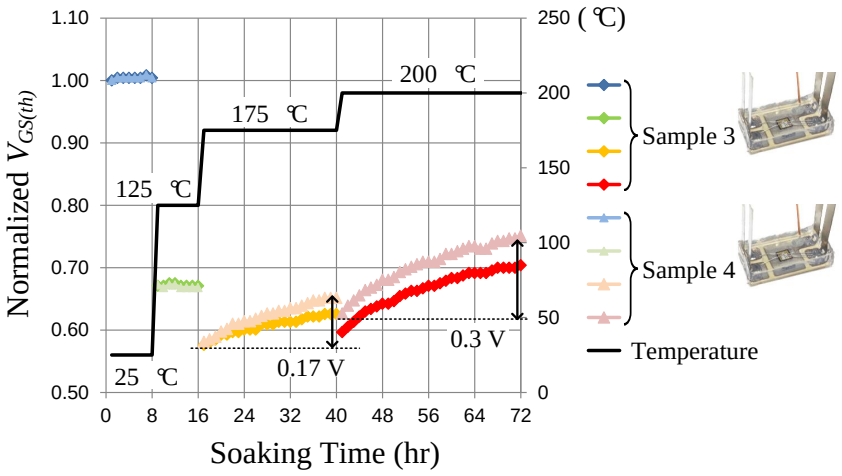


Figure 2-15. Normalized threshold voltage measured during the gate biasing test
Test samples are two SiC MOSFET bare dice in the customized high-temperature package

Other device characteristics are also affected after the stressing test. Figure 2-16 (a) to (d) exhibit the $V_{GS(th)}$, I_{DSS}, $R_{DS(on)}$, and C_{ISS} of the DUTs, measured at room temperature after every 8 hours of soaking. In this case, $V_{GS(th)}$ is seen to increase by around 0.6 V at the end of the test. Fortunately, the small variations of I_{DSS} and $R_{DS(on)}$, as seen in (b) and (c), imply that the blocking capability and the conduction loss of the devices are not greatly affected. Nevertheless, C_{ISS} of the DUTs does decrease by around 5% at the end. The change in C_{ISS} has not been reported previously, and could be related

to the accumulated interfacial charge under the existence of both high gate electric field and high junction temperature.

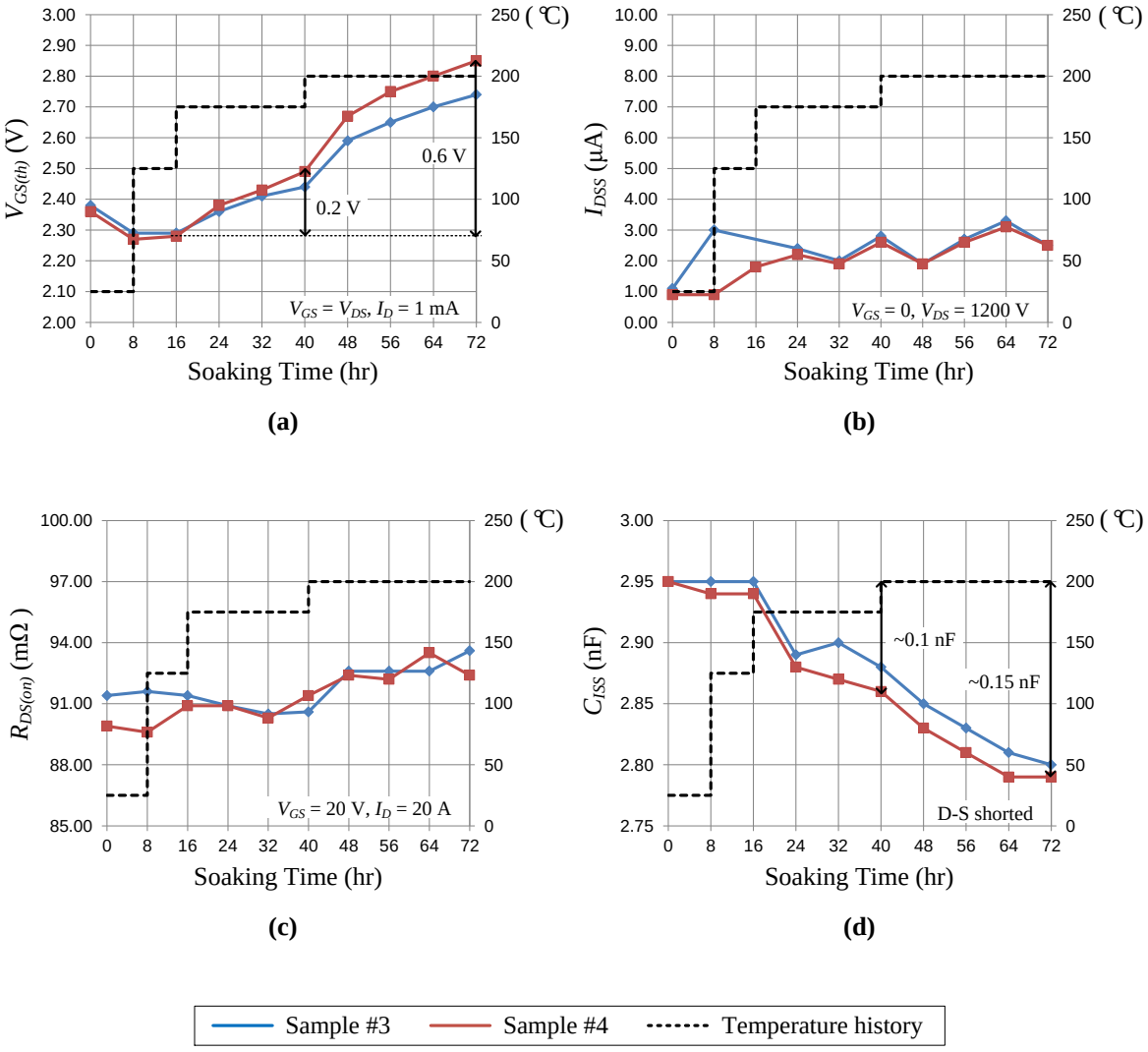


Figure 2-16. Static parameters measured in the high-temperature gate biasing test in Figure 2-15 All measured at room temperature. Black dashed line indicates only the soaking temperature history

Figure 2-17 compares the device *I-V* curves at different moments of the test. The output characteristics shown in Figure 2-17 (a) indicate that the forward *I-V* curve degrades more at lower gate voltages. At V_{GS} = 20 V, there is almost no change in the slope. This explains why the device $R_{DS(on)}$ does not change after the soaking test. In (b),

the transfer *I-V* curve shifts to the right after stressing, showing clearly the positive change in $V_{GS(th)}$.

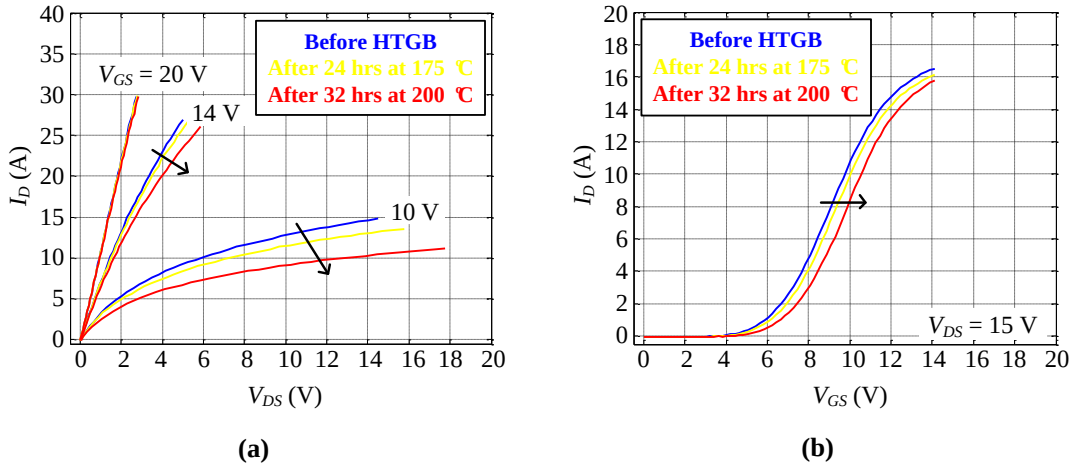


Figure 2-17. Comparisons of (a) output, and (b) transfer characteristics at different moments during the gate biasing test in Figure 2-15. All measured at room temperature

2.3.3 Gate Switching Test

The gate biasing test applies the worst voltage and temperature stresses to the MOSFETs, but it does not reflect the normal operation condition of these devices. For this reason, the gate switching test is conducted on another two samples in the high-temperature package, where the DUTs are applied with a switching gate voltage from -4 V to 20 V at 50% duty cycle and 70 kHz – a condition closer to the real application. The measured $V_{GS(th)}$ under this condition is displayed in Figure 2-18. Again, the threshold does not change below the rated junction temperature. At 175 ℃, contrary to the previous result, $V_{GS(th)}$ starts to decrease, but this trend quickly slows down over the time. After 24 hours soaking at 175 ℃, an absolute negative shift of 0.1 V can be observed. When the temperature increases to 200 ℃, $V_{GS(th)}$ tends to stabilize and no further

decreasing trend can be seen. The maximum variation measured is only 0.05 V at this temperature.

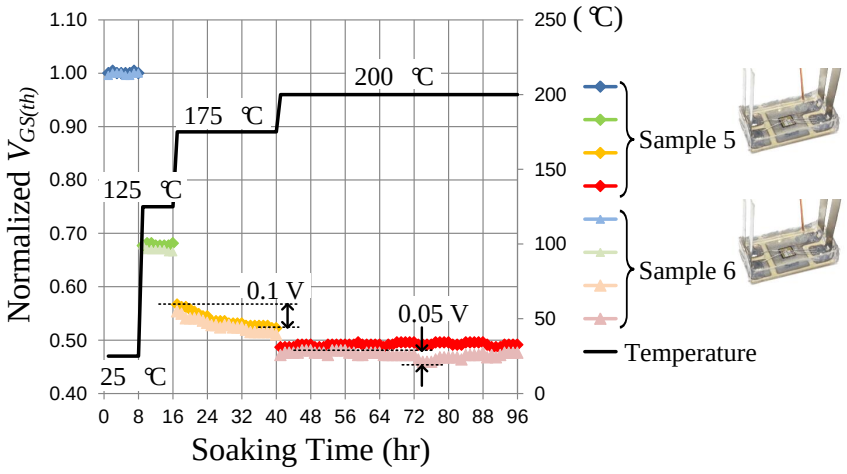


Figure 2-18. Normalized threshold voltage measured during the gate switching test
Test samples are two SiC MOSFET bare dice in the customized high-temperature package

Intuitively, the negative turn-off voltage (-4 V) presents a counter effect to the positive turn-on voltage (+20 V), and therefore results in a smaller threshold voltage shift. This can also be confirmed from the static parameters shown in Figure 2-19. As seen, the maximum variation of $V_{GS(th)}$ is only 0.15 V in this case, compared to 0.6 V in the gate biasing test. The input capacitance C_{ISS} still decreases but by a smaller amount of only 0.08 nF. Also, same as the previous test, the device's blocking capability and on-state resistance are not affected.

Correspondingly, there is also very little change in the output and transfer *I-V* curves. Therefore they are not shown in this section.

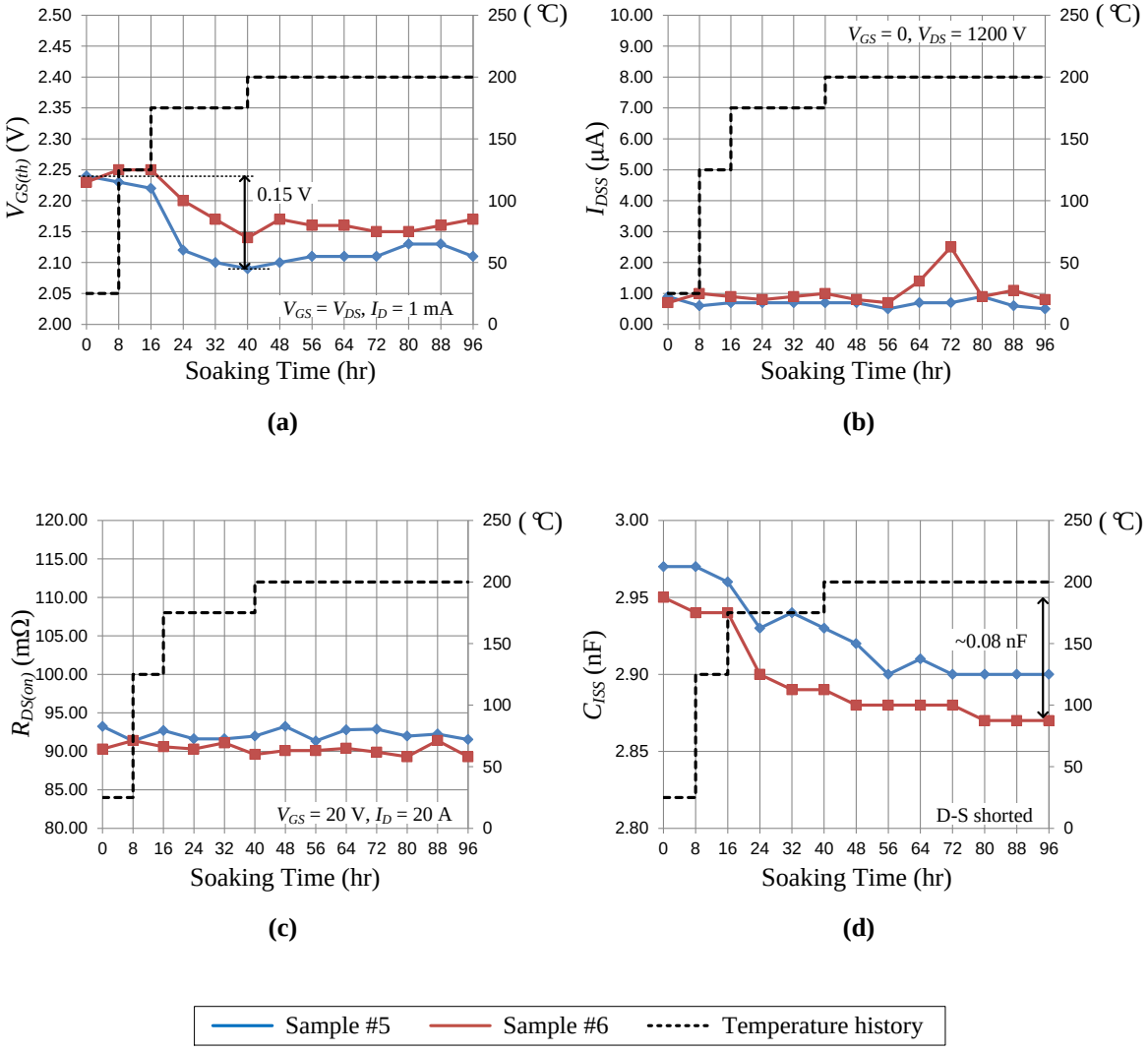


Figure 2-19. Static parameters measured in the high-temperature gate switching test in Figure 2-18 All measured at room temperature. Black dashed line indicates only the soaking temperature history

2.3.4 Discussion on the Gate Oxide Stability Tests

Limited in the number of devices, the sample group used for each test is small – only two, yet the trends presented by both samples are quite consistent under the same test condition. Therefore, the results shown here represent to some extent the general behaviors of the DUTs.

Same as the previous work has shown, $V_{GS(th)}$ of SiC MOSFETs will shift under the gate bias, or the electric field inside the gate oxide layer. The direction and absolute value of this shift are determined by the polarity and magnitude of the field, and the shifting trend will accelerate at higher junction temperatures, especially when exceeding the rated maximum temperature of 135 ℃. In the situation where both positive and negative gate voltages are present, the direction of the threshold shift is also intuitively dependent on the duration of each polarity, i.e. the corresponding duty cycle and switching frequency. In this work, the typical 50% duty cycle is used. The resultant $V_{GS(th)}$ shift is small (0.1 V at 175 ℃), and the change tends to stabilize over the time at 200 ℃. This small amount of change is tolerable in terms of the converter operation, as long as the gate oxide does not degrade further in the long term. However, whether or not the device will behave differently with other modulation methods (e.g. SPWM) remains a question, and needs further investigations.

Fortunately, after both tests, no significant degradation is observed in the DUT's leakage current, meaning that the MOSFET still keeps its blocking capability and normally-off characteristic even though the threshold has shifted. The conduction loss is not affected either as $R_{DS(on)}$ remains almost unchanged. However, this requires that the device is fully turned on at 20 V, as one can infer from Figure 2-17 (a).

What does change in terms of device operation is its switching behavior, due to the changes of $V_{GS(th)}$ and C_{ISS}. A small decrease in C_{ISS} means that the switching delays, at both turn-on and turn-off, will slightly decrease. The $V_{GS(th)}$ shift mainly reshapes the transfer characteristic. As explained in Section 2.2.3, this implies different gate plateau voltage under the same load current, and consequently, different switching speed. For a

positively shifted $V_{GS(th)}$, it can be inferred that the turn-on speed will be slower, while the turn-off becomes faster. The trend will be opposite if $V_{GS(th)}$ shifts negatively. The switching loss will also change accordingly.

2.4 Conclusions

This chapter systematically evaluates the high-temperature characteristics of the commercial SiC power MOSFET. The static and switching characterizations have shown the great potential of the device for high-temperature operations, with the following advantages:

(1) Very small off-state leakage current at high temperatures. This is the main barrier preventing Si devices from operating above 150-175 °C, but is not a critical issue for SiC MOSFETs, thanks to their wider bandgap energy.

(2) Small and temperature-insensitive on-state resistance. The negative temperature coefficient of the MOSFET's channel resistance helps a lot in constraining the overall $R_{DS(on)}$. Even at 200 °C, the conduction loss of the device will only increase by 40% compared to the 25 °C condition, in contrast to over 200% increase for Si MOSFETs at merely 150 °C.

(3) Fast switching speed and temperature-insensitive switching loss. Being a unipolar device, the SiC MOSFET can be switched much faster than Si IGBTs, which means higher switching frequency for the same switching loss. Furthermore, E_{tot} of the SiC device is much less temperature-dependent, due to the canceling effect of its E_{on} and E_{off}.

In terms of the gate oxide stability issue, the gate biasing and gate switching tests presented in this chapter again quantitatively exhibit the trade-off between the performance and reliability of the SiC MOSFET, which will become even more critical if high-temperature operation is expected. The high-temperature converter can be achieved with higher efficiency (i.e. lower $R_{DS(on)}$) and higher power density (i.e. higher junction temperature rise due to smaller cooling system size) at the price of more serious device degradation and perhaps shorter life time. In this sense, the current SiC MOSFETs still need further improvements on their gate oxide stability to address this design trade-off, before they can be utilized in high-temperature converters on a large scale.

2.5 References

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Chapter 3 Influences of Stray Inductances on MOSFET Switching Behaviors

3.1 Introduction

The parasitic elements in power electronic circuits, e.g. device junction capacitances and package stray inductances, which used to be less an issue for slower Si IGBTs, have become a critical barrier for the much faster SiC MOSFETs when trying to push their switching speed to the limit in today's high-frequency, hard-switching converters. Because of these parasitics, faster switching speed will always be penalized by more severe device over-voltages and electromagnetic interferences (EMI), due to the parasitic ringing in the device's switching transients. The influences of stray inductances on the device switching behaviors have been studied previously through analytical calculations, simulation, experiments, or a mix of these methods, all in the time domain [1]-[7]. It has been commonly pointed out that the switching loop inductance, which resonates with the device junction capacitances, contributes most to the parasitic ringing in the switching voltage/current waveforms. However, the mechanism behind that is not so clearly seen from the time-domain-only studies.

In this chapter, an experimental parametric study is firstly presented to investigate the influences of different stray inductances on the switching waveforms of a power MOSFET. Besides verifying the common conclusion about the parasitic ringing, the study also provides a deeper understanding of the origins of the common source inductance. Based on a time-domain equivalent circuit which is developed to model the MOSFET's turn-off ringing, a small-signal AC circuit is further derived to study the ringing issue in the frequency domain. From this angle, the mechanism of the turn-off ringing can be explained and understood in a simpler but deeper way. The same small-signal model is then extended to study the effect of decoupling capacitors – a commonly used method to suppress the ringing. Likewise, the frequency-domain analysis provides a deeper and more general insight into this problem than the traditional time-domain study. A rule of thumb regarding how to select the proper decoupling capacitance value can also be derived from this frequency-domain study.

3.2 Experimental Parametric Study of the Parasitic Inductance Influence on MOSFET Switching Characteristics

Most of the previous efforts used the classic double-pulse circuit to study the effects of circuit parasitics, as shown in Figure 3-1. In [3][5]-[7], differential equations containing both parasitic inductances and capacitances were established and solved to calculate the MOSFET's ringing waveforms analytically. This method, however, is usually very complicated because of the nonlinear nature of the device's junction capacitances, as well as the high order of the system (i.e. six state variables including three junction capacitances and three terminal inductances). Assumptions and

simplifications used to make the differential equations solvable, nevertheless, usually oversimplify the problem and thus lead to inaccurate results in these works.

For this reason, a parametric study has been carried out in this work to study the influences of stray inductances experimentally. The double-pulse circuit in Figure 3-1 is still used to investigate the device's switching waveforms. The study is conducted on a 600 V, 20 A Si CoolMOS (Microsemi APT20N60BCF), but all the results presented below are equally applicable to SiC MOSFETs since they share similar switching characteristics. The MOSFET is driven by a 0-10 V gate voltage from an IXYS IXDD414 gate driver chip, with variable gate resistance R_G to adjust the switching speed. A 1.2 kV, 20 A SiC Schottky diode is used as the freewheeling diode to eliminate the reverse recovery effect. The load inductor L_{Load} is specially designed to have only one layer of winding in order to minimize its equivalent parallel capacitance (EPC). The layout of the printed circuit board (PCB) is also designed with great care to minimize its stray inductances. All of these measures are to ensure that the MOSFET's switching behaviors are affected as little as possible by the parasitics of the tester circuit itself [8].

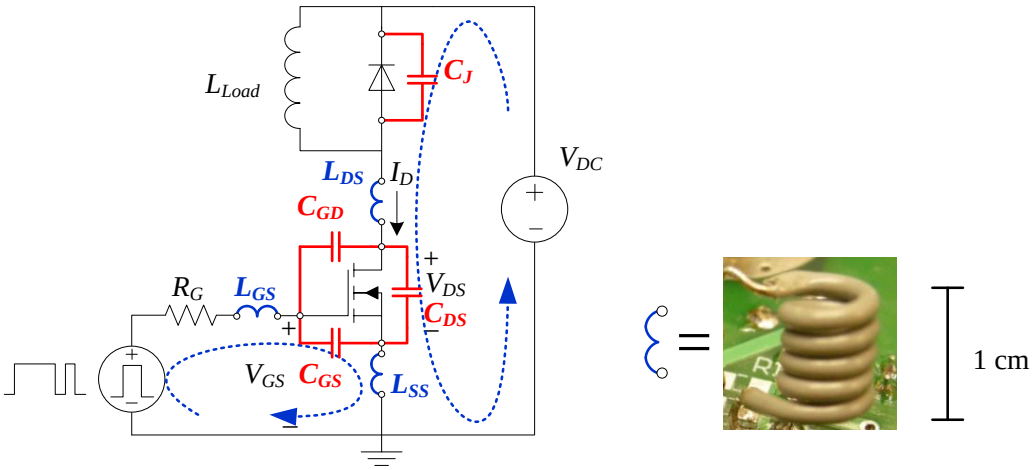


Figure 3-1. Double-pulse circuit schematic with parasitic components

Three most critical stray inductances can be identified in this configuration. The gate loop inductance L_{GS} and the main switching loop inductance L_{DS} represent the lumped total inductances of their respective current loops, while the common source inductance L_{SS} represents the mutual inductance between the two loops. To study the influences of these parasitic parameters, the current paths in the tester are broken at several points, where small air-core inductors, also shown in Figure 3-1, can be inserted into the loops to mimic the circuit parasitics. Each stray inductance is controlled independently in the study, with the other breakpoints simply shorted.

Figure 3-2 shows the MOSFET's switching waveforms under the influence of L_{GS}. The device is switched under 400 V and 10 A, with R_G = 5 Ω. During the experiment, the external L_{GS} is increased step-by-step from 0 to 65 nH (Note that besides L_{GS}, there is also several nH stray inductance associated with the PCB). This inductance, as stated in many publications, tends to resonate with the MOSFET's input capacitance C_{ISS} (= C_{GS} + C_{GD}) and cause oscillation in the gate-source voltage V_{GS} waveform. This effect is apparently seen in the turn-off transient. The V_{GS} oscillation, however, only leads to limited ringing in the drain-source voltage V_{DS} and drain current I_D waveforms. During the turn-on process, V_{DS} and I_D almost do not change, while at turn-off the ringing only deteriorates slightly.

Figure 3-3 shows the effect of L_{DS} under the same switching condition. This inductance essentially resonates with the device's junction capacitances during the switching transients, and the oscillation can be further coupled into the gate loop through the Miller capacitance C_{RSS} (= C_{GD}). Therefore, the increase in L_{DS} introduces higher ringing in all V_{GS}, V_{DS} and I_D waveforms. Compared to L_{GS}, L_{DS} has a much more

significant impact on the MOSFET in worsening the oscillation and the over-voltage stress.

Figure 3-4 shows the influence of L_{SS}. In this case, the MOSFET is tested under the same voltage and current, but with R_G = 15 Ω. Generally, L_{SS} acts as a negative feedback from the switching loop to the gate loop. During the rise and fall periods of I_D, the voltage drop across L_{SS} will counteract the change of V_{GS}, thus slowing down the swings of the current, as seen in the figure [9][10]. The result of a larger L_{SS} is then not to worsen the parasitic ringing across the device – due to its slowing-down effect, but to significantly increase the switching energy at both turn-on and turn-off.

The general understanding about the common source inductance is that it originates from the shared current path between the gate loop and the main switching loop. Therefore, a common practice is to use Kelvin connection for the gate drive circuit to eliminate this inductance. There exists, however, another important but usually overlooked mechanism – L_{SS} may also originate from the magnetic coupling between L_{GS} and L_{DS}, as shown in Figure 3-5. It can be easily proven that the two circuits in the figure are equivalent mathematically. This implies that the Kelvin connection may not be able to eliminate all the common source inductance effect, if the layout of the gate and switching loops is not designed properly and introduces a non-negligible amount of mutual inductance.

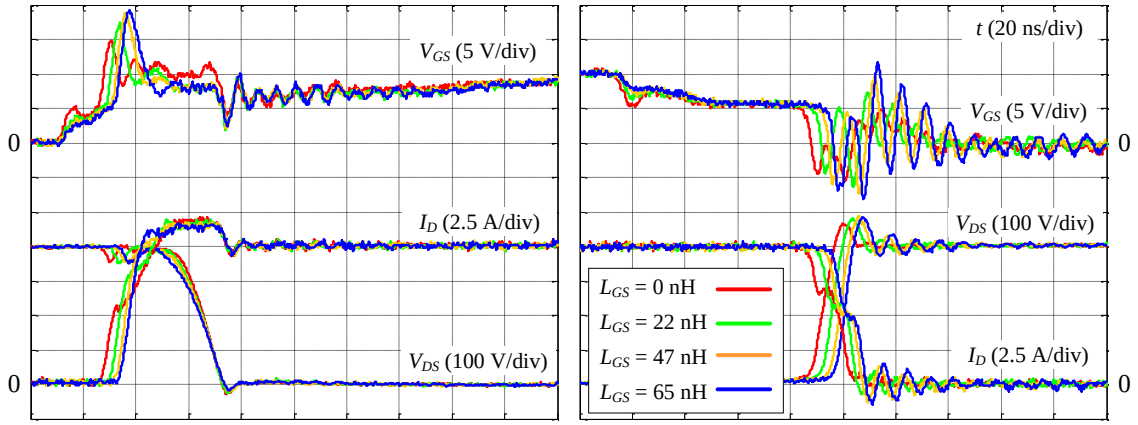


Figure 3-2. Influence of L_{GS} during turn-on (left) and turn-off (right), at 400 V, 10 A, R_G = 5 Ω

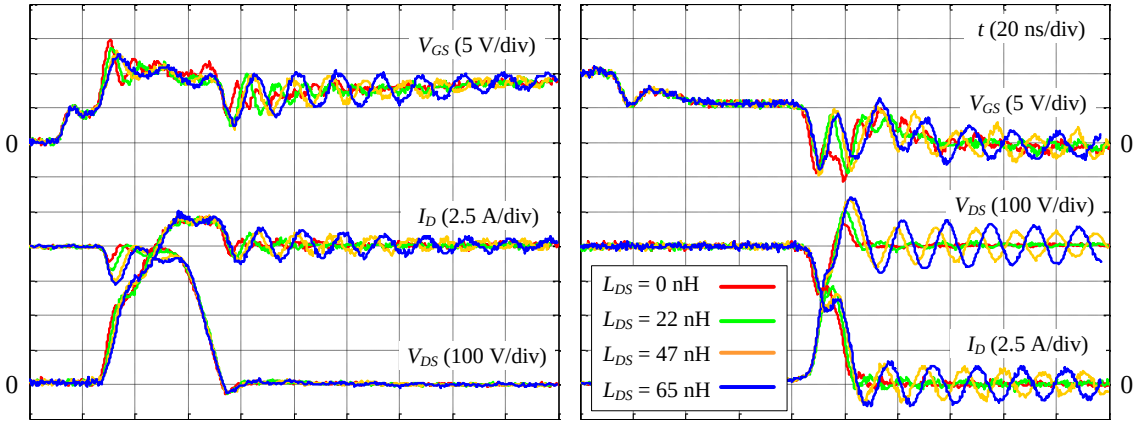


Figure 3-3. Influence of L_{DS} during turn-on (left) and turn-off (right), at 400 V, 10 A, R_G = 5 Ω

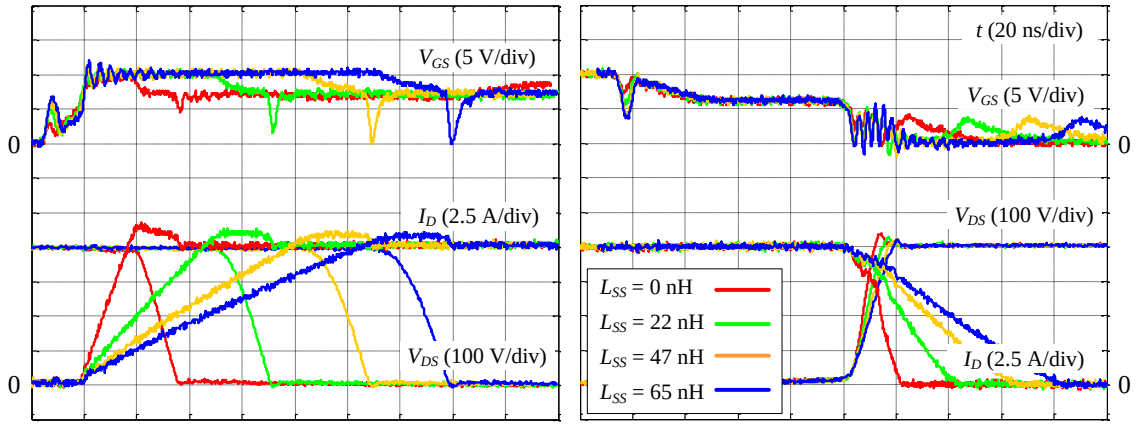


Figure 3-4. Influence of L_{SS} during turn-on (left) and turn-off (right), at 400 V, 10 A, R_G = 15 Ω

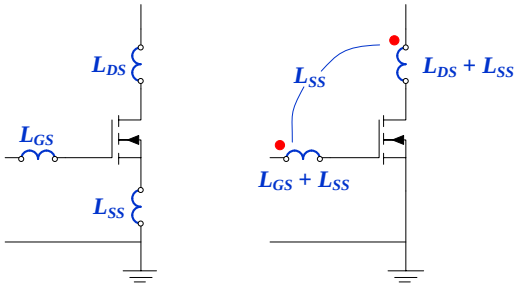


Figure 3-5. Two origins of L_{SS}: Shared current path (left), and magnetic coupling (right)

The above hypothesis is verified through experiments by inserting L_{GS} = 47 nH and L_{DS} = 65 nH into the breakpoints shown in Figure 3-1, while still keeping the Kelvin connection structure. These coils are placed on the tester board in such a way that they produce either decoupled (i.e. very weakly coupled) or coupled inductances, as illustrated in Figure 3-6. As seen, positioning the two coils perpendicular to each other produces the decoupled condition, while putting them side-by-side coaxially produces the coupled conditions. Different coupling polarities can be achieved depending on the relative current directions in the two coils. The red dot polarity marks indicate a condition when a negative feedback is formed by generating an equivalent positive common source inductance M – a condition commonly talked about in literatures. On the other hand, by flipping one of the coils, a positive feedback can even be formed by generating an equivalent negative M, as indicated by the blue star polarity marks. Figure 3-7 shows the corresponding experimental waveforms, evincing how the negatively coupled condition produces slower slew rates and less ringing compared to the decoupled case, while the positively coupled condition exhibits just the opposite – faster switching speed but more severe ringing.

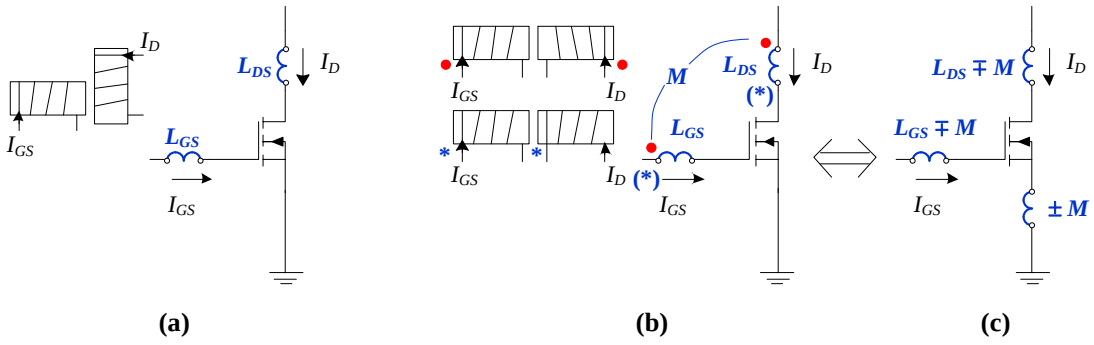


Figure 3-6. Magnetic coupling between the gate loop and main switching loop
(a) Decoupled condition, (b) coupled conditions with different polarities, (c) equivalent circuits

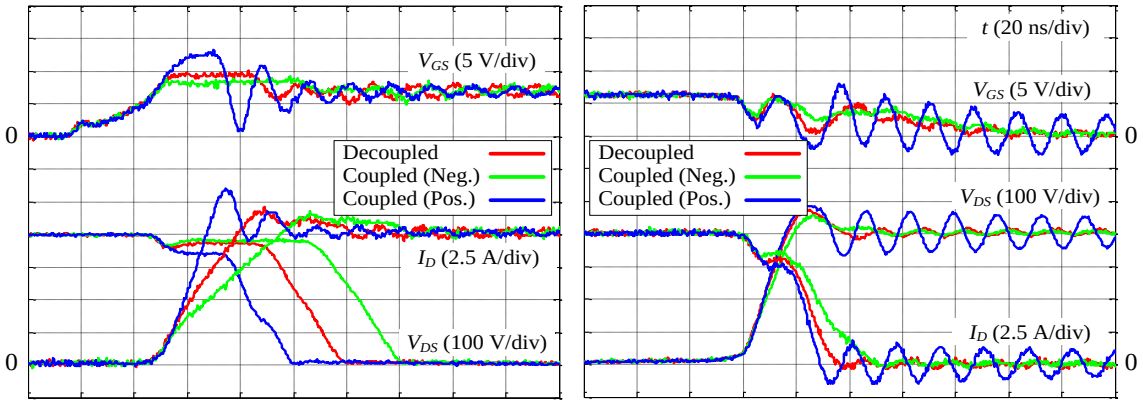


Figure 3-7. Influence of magnetic coupling between the gate loop and main switching loop during turn-on (left) and turn-off (right), at 400 V, 10 A, R_G = 15 Ω

These results can be explained using the coupled inductor model illustrated in Figure 3-6 (c). Specifically, when the two loops are negatively coupled, the equivalent self-inductances become smaller (i.e. (L_{GS} - M) and (L_{DS} - M)), and a positive inductance M appears on the common source path. Both effects tend to reduce the switching speed and switching ringing. On the other hand, for the case of positive coupling, not only do the self-inductances become larger in both loops (i.e. (L_{GS} + M) and (L_{DS} + M)), but a negative common source inductance –M also forms a positive feedback that increases the

di/*dt* and further deteriorates the ringing. This is why much more severe oscillations are observed in all waveforms in the positively coupled condition.

The parametric study has revealed that the main switching loop inductance L_{DS} is the most critical contributor to the parasitic ringing of the switch. The physics behind this result is that the current commutation only occurs between the two devices in a switch pair – the MOSFET and its commutating diode. As illustrated in Figure 3-8, during the turn-off process, a positive *di*/*dt* goes through the freewheeling diode, and the same *di*/*dt* with negative polarity flows through the MOSFET, since these two currents add up to the constant load current for hard switching. Equivalently, there is a current with negative *di*/*dt* flowing through the loop enclosed by the switch pair and the V_{DC} source. This *di*/*dt* produces a voltage drop on the lumped loop inductance, L_{DS}, which adds to V_{DC} and causes over-voltages on the switch. L_{DS} then resonates with the device junction capacitances to produce ringing in the switching waveforms. The same analysis can also be applied to the other switch pair (i.e. top MOSFET and bottom diode) in the phase-leg configuration.

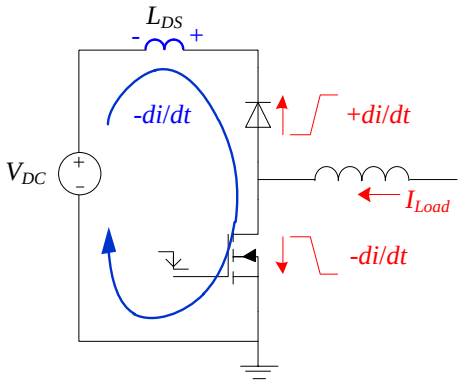


Figure 3-8. The main switching loop with the most severe *di*/*dt* in the switch-pair configuration

3.3 Small-Signal Modeling of the Turn-Off Ringing of Power MOSFETs

As the switching loop inductance is inevitable in the real converter due to the parasitics from device packages and PCB traces, etc., a trade-off always exits between faster switching speed and more severe device stresses for the power MOSFETs. The turn-off transient is of particular concern since the parasitic ringing and the consequent over-voltage may exceed the MOSFET's blocking voltage and damage the device. It is therefore very important to understand the mechanism of the turn-off ringing.

Instead of investigating the ringing in the time domain, a small-signal model will be derived in this section to study this issue in the frequency domain. The circuit in Figure 3-1 is still used to derive the model. A large-signal equivalent circuit with only *R*/*L*/*C* components and voltage/current sources will be firstly derived to reproduce the ringing following a turn-off transient, so that the study will not be constrained to any specific MOSFET. A few assumptions and facts are considered in the derivation of this equivalent circuit:

(1) The load inductor current does not change during the switching transients, which is generally true for hard-switching converters. Therefore, the load inductor can be modeled as a constant current source.

(2) The turn-off ringing occurs only after V_{DS} has crossed the V_{DC} voltage. After this moment, the freewheeling diode will be forward biased and start to commutate current, and thus a di/dt will be formed in the switching loop. This can be verified from the experimental waveforms shown in Figure 3-3. The conducting diode also effectively shunts any capacitance in parallel with it, including its own junction capacitance C_J, and

the EPC of the load inductor. In the other word, these capacitances will not participate in the resonance, and can be neglected in the model. All the ringing current will thus flow through the diode itself, which can be modeled as a voltage source V_{FWD} in series with a resistance R_{FWD}.

(3) According to its switching trajectory, the MOSFET is working in the saturation region during the turn-off process, where its channel behaves like a gate voltage controlled current source [11]. The device channel can then be modeled as a current source with an appropriate di/dt, whose value is determined by the switching speed.

(4) The MOSFET's output capacitance C_{OSS} (= C_{GD} + C_{DS}), although a strong nonlinear function of V_{DS}, can also be treated as linear at high V_{DS} bias at turn-off, since the junction capacitance usually becomes saturated and less sensitive to V_{DS} at high bias voltage.

Based on these, the equivalent circuit can be modeled as Figure 3-9.

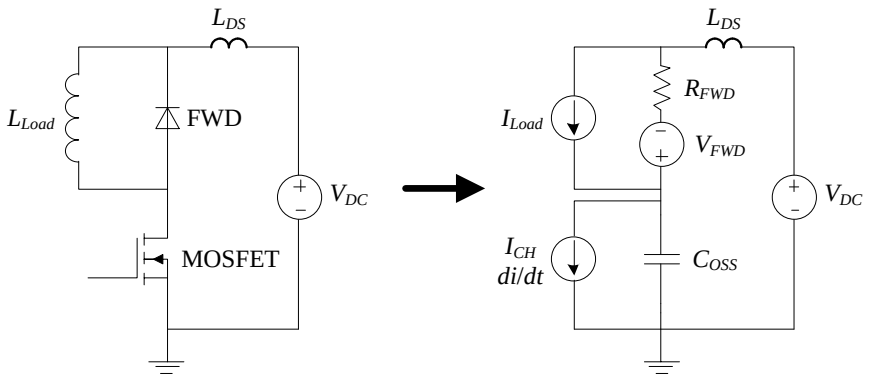


Figure 3-9. Derivation of the large-signal model for the turn-off ringing

Simulation is carried out to validate this model. In Figure 3-10 (a), detailed device models are used to simulate the switching waveforms, while in (b) they are replaced by corresponding R/C components (R_{FWD} = 49 mΩ, C_{OSS} = 121 pF in this example) and V/I

sources. Additional DC decoupling capacitances (12 nF and 1 μF) and bulk capacitance (750 μF) are also included, together with estimated interconnect stray inductances (10, 30 and 100 nH), to make the simulation closer to the real condition.

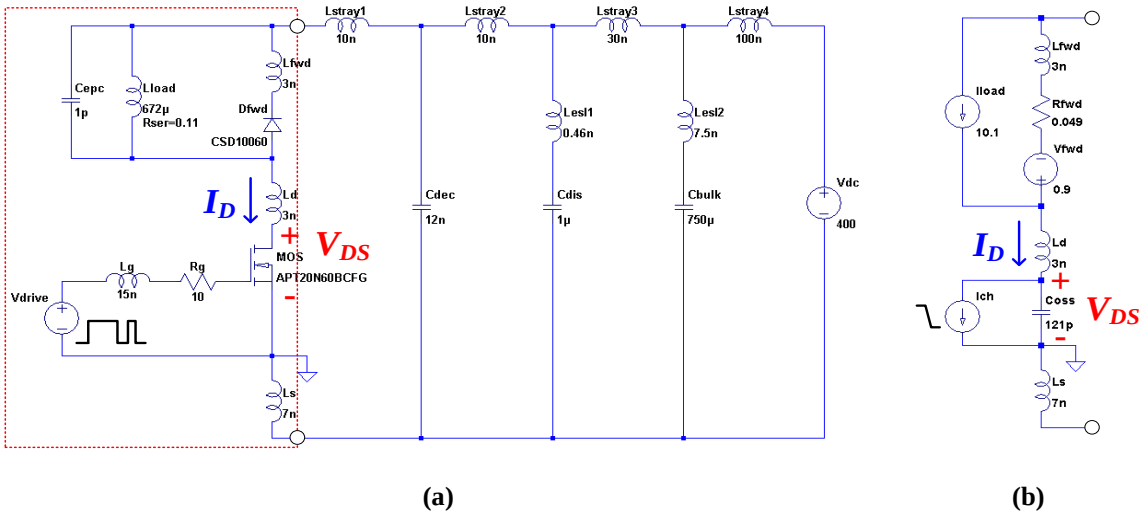
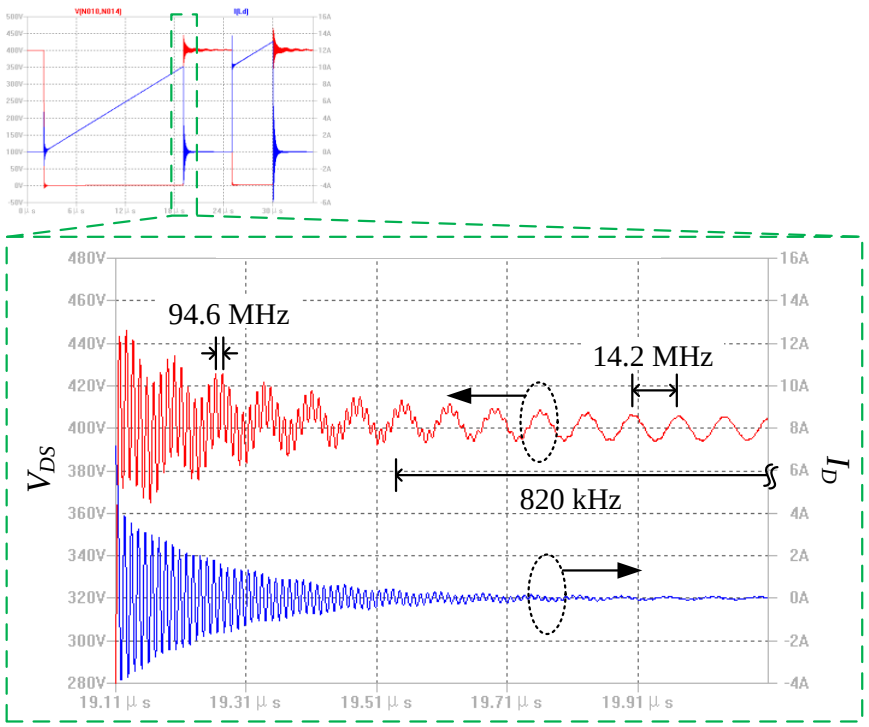
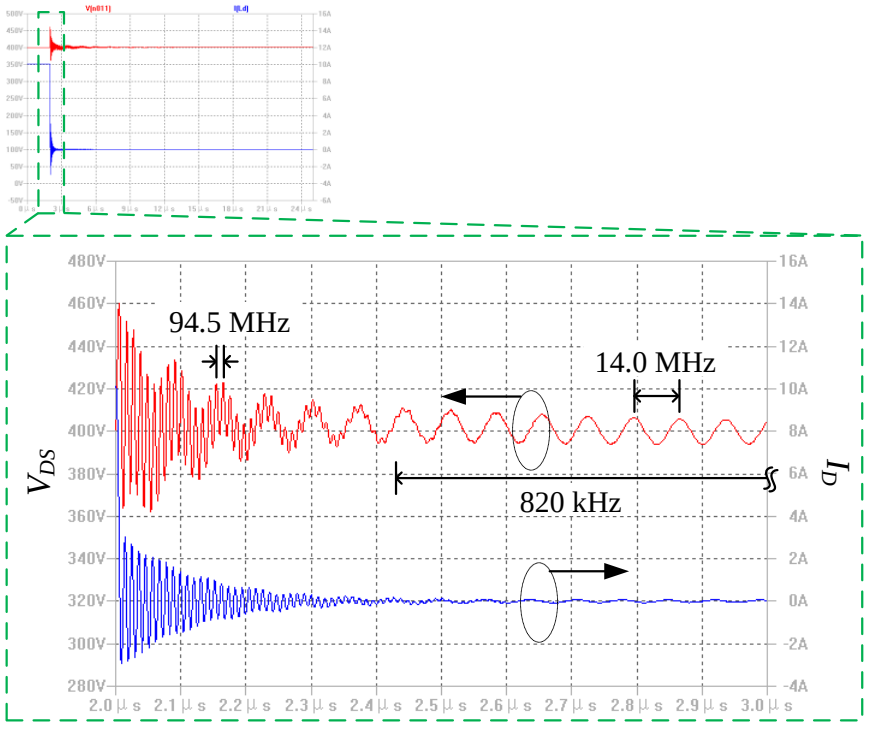


Figure 3-10. Simulation circuits to validate the large-signal model for the turn-off ringing (a) Simulation with device models, (b) the circuit that replaces the red-boxed part in (a) for the simulation with the large-signal model

The simulated turn-off waveforms are shown in Figure 3-11. Multiple ringing frequencies can be observed due to the distributed *L*'s and *C*'s along the DC bus. The equivalent circuit predicts well all of the three main frequencies at around 94.5 MHz, 14.0 MHz, as well as an even lower one at 820 kHz, which can only be clearly seen when zoomed out. Besides the ringing frequencies, the damping of the oscillations is also simulated correctly by the equivalent circuit. This validates the effectiveness of the large-signal model in describing the system during the ringing period.



(a)



(b)

Figure 3-11. Time-domain simulation of the ringing when the MOSFET turns off 400 V, 10 A
(a) Simulation with device models, (b) simulation with equivalent circuit

Several comments can be made regarding this large-signal model:

(1) Since the model assumes the conduction of the freewheeling diode, it only models the ringing part in the turn-off transient, after the *dv*/*dt* and *di*/*dt* processes have ended. Therefore, it cannot replace the device models in simulating the entire switching waveforms.

(2) The model indicates that the damping element in the system is provided by the series resistance of the diode. In the real circuit, the resistance will also come from the interconnection resistances at the relatively high ringing frequency (e.g. MHz range). These resistances can be lumped into R_{FWD} and thus will not change the model topology.

(3) It is also easy to verify in the simulation that, under the same circuit parameters, different switching speeds will only affect the amplitudes of the oscillations. The ringing frequencies will remain unchanged.

The small-signal model can then be easily derived from the equivalent circuit in Figure 3-9. The DC current source is open-circuited and the voltage sources are shorted. The resultant AC equivalent circuit is shown in Figure 3-12. It is clearly seen that an *RLC* parallel resonant network is formed, where *L* originates from the stray inductance L_{DS}, *C* from the MOSFET junction capacitance C_{OSS} (capacitance at the V_{DC} bias), and *R* from the diode series resistance R_{FWD}.

From Figure 3-12, it is natural to see that the parasitic ringing in the MOSFET's V_{DS} waveform is just a response of the *RLC* network under the excitation of the *di*/*dt* source I_{CH}. The Bode plot of the input impedance of such a network is shown in Figure 3-13. A parallel resonance is created by L_{DS} and C_{OSS}, at the frequency of

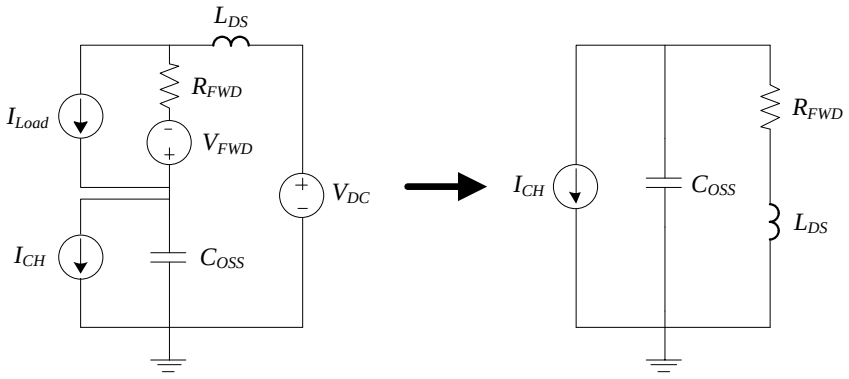


Figure 3-12. Derivation of the small-signal model for the turn-off ringing

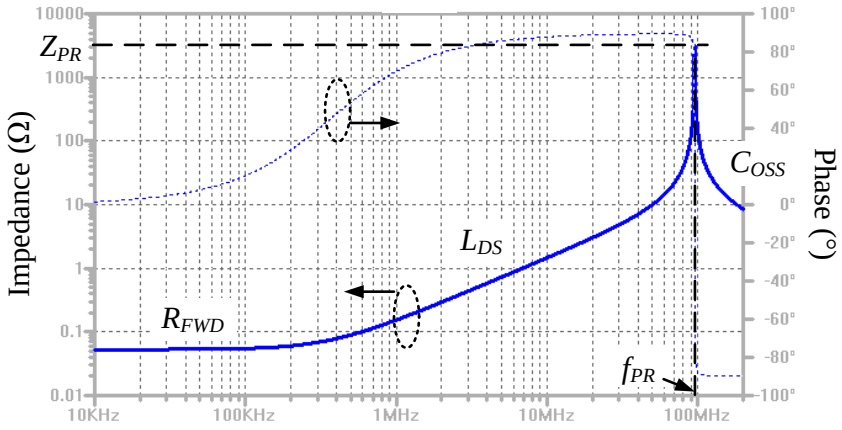


Figure 3-13. Bode plot of the input impedance Z_{IN} of the parallel resonant network

$$\omega_{PR} = \frac{1}{\sqrt{L_{DS}C_{OSS}}} \cdot \sqrt{1 - \frac{C_{OSS}R_{FWD}^{\ 2}}{L_{DS}}} \,. \tag{3-1}$$

For the resonance to exist, it must satisfy that

$$1 - \frac{C_{OSS}R_{FWD}^{\ 2}}{L_{DS}} > 0 \,, \tag{3-2}$$

namely,

$$R_{FWD} < \sqrt{\frac{L_{DS}}{C_{OSS}}} \,. \tag{3-3}$$

This requirement is generally satisfied since power converters usually have very low resistive dissipation to achieve high efficiency. As a matter of fact, in most cases,

$$R_{FWD} << \sqrt{\frac{L_{DS}}{C_{OSS}}} \tag{3-4}$$

is satisfied, in which case the resonant frequency can be simply estimated by

$$\omega_{PR} \approx \frac{1}{\sqrt{L_{DS} C_{OSS}}}. \tag{3-5}$$

If plugging in the parameters in Figure 3-10 (i.e. R_{FWD} = 49 mΩ, C_{OSS} = 121 pF at V_{DS} = 400 V, and L_{DS} = 23 nH), one can calculate the Q-factor of this resonant circuit to be

$$Q_{PR} = \frac{1}{R_{FWD}} \sqrt{\frac{L_{DS}}{C_{OSS}}} \approx 281, \tag{3-6}$$

and the maximum impedance to be

$$Z_{PR} = R_{PR} = \frac{L_{DS}}{C_{OSS} R_{FWD}} = 3.88\,\text{k}\Omega, \tag{3-7}$$

at the resonant frequency of $f_{PR} \approx$ 95.4 MHz. It can be seen that the calculated resonant frequency closely matches the highest ringing frequency in the simulation.

The small-signal model clearly unveils the mechanism of the turn-off ringing: The parallel resonance will "pick out" the current harmonic from the di/dt excitation at the resonant frequency, and produce voltage oscillation across the MOSFET D-S terminals due to the high impedance at this frequency. The large Q value indicates a highly under-damped system, so the oscillation cannot be damped very quickly.

The same analysis can also be extended to the more complicated condition in Figure 3-10. During the turn-off ringing, if one looks from the MOSFET D-S terminals

back to the V_{DC} source, the impedance as shown in Figure 3-14 can be obtained. The parallel resonances are found at multiple frequencies (818 kHz, 14.2 MHz, and 95.9 MHz) due to the distributed *L*'s and *C*'s along the DC bus, which coincide with and explain the ringing frequencies seen in the switching waveforms (820 kHz, 14.2 MHz, and 94.6 MHz).

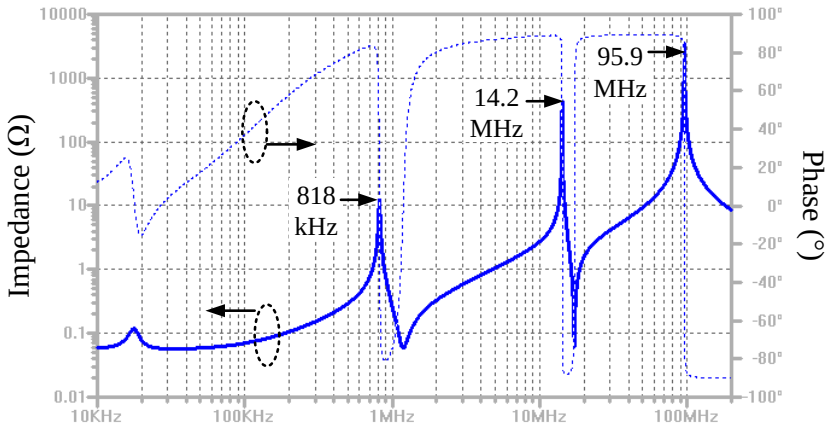


Figure 3-14. Bode plot of the impedance seen from the MOSFET D-S terminals at turn-off

3.4 Analysis of the Effect of Decoupling Capacitors

3.4.1 Frequency-Domain Analysis

In high-frequency, hard-switching converters, DC decoupling capacitors, which are much smaller in capacitance values than the DC-link bulk capacitors, are generally placed right next to the power switches or modules to suppress the switching ringing due to the interconnect stray inductances from the device packages and DC bus bars [8]. Compared to other ringing-suppression methods such as snubber circuits, the decoupling capacitors are easier to implement, and more importantly, do not slow down the device switching speed, which is critical for the efficiency of high-frequency power converters [12].

The effect of decoupling capacitors has also been studied previously in the time domain. In [13], equations were established to calculate the IGBT's ringing waveforms under the existence of decoupling capacitance, and the differential-mode EMI noise spectrum was also measured to verify the results. Nevertheless, the conclusions obtained from the time-domain view angle are hard to be generalized, as the results, either over-voltages in switching waveforms or noise spikes in the EMI spectrum, are closely related to the device and its switching speed, which differ case by case in various studies. Moreover, the analytical solutions have already taken quite complicated forms for a second-order *LC* circuit, and are not suitable to study higher-order systems when decoupling capacitors, or even DC bus distributed capacitors, are introduced.

Therefore, in this section, the effect of decoupling capacitors on suppressing the MOSFET's turn-off ringing is re-examined in the frequency domain with the use of the small-signal model. From this viewpoint, the same conclusion can be drawn as in [13], but in a much simpler form. Plus, the frequency-domain analysis also provides a deeper and more general insight into the problem. A rule of thumb regarding how to select the proper decoupling capacitance can also be derived from the study.

The analysis considers the circuit shown in Figure 3-15. In this circuit, it is assumed that L_{DS} represents the minimum possible stray inductance associated with the device package and the shortest necessary interconnection to access the decoupling capacitance C_{Dec}. The interconnection between the voltage source and the power stage, such as DC bus bar, will then introduce an additional stray inductance L_1. To simplify the analysis, distributed DC capacitances are not considered in this model.

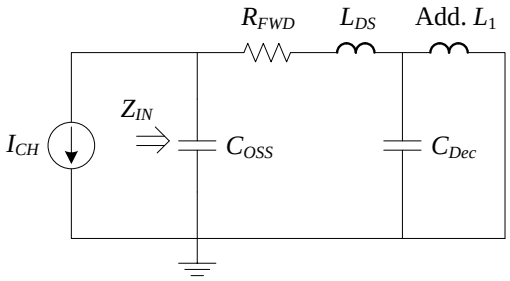
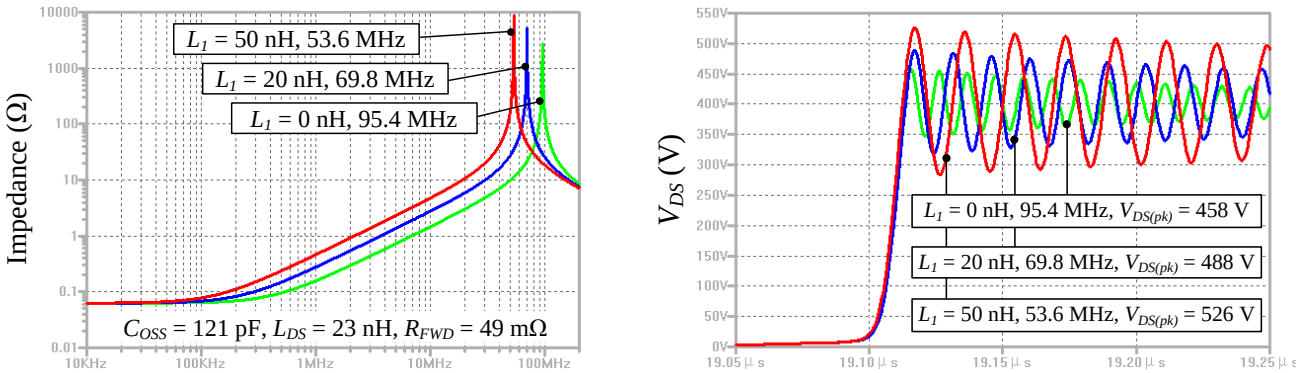


Figure 3-15. Small-signal model with the decoupling capacitance C_{Dec}

Without the decoupling capacitance (i.e. C_{Dec} = 0), it is expected that the additional L_1 will lower the resonant frequency, but increase the peak impedance, based on Eq. (3-5) and (3-7). The time-domain effect is that the parasitic ringing with lower frequency but higher amplitude can be observed, as shown in Figure 3-16. This is consistent with the experimental results in Figure 3-3. Apparently, higher over-voltage needs to be prevented from damaging the MOSFET.



(a) **(b)**

Figure 3-16. Effect of L_1, when C_{Dec} = 0. (a) AC simulation of Z_{IN}, (b) transient simulation of MOSFET V_{DS} turning off 400 V, 10 A, using device models

A small decoupling capacitance C_{Dec} is thus commonly inserted between L_{DS} and L_1 to bypass the high-frequency current. The introduction of C_{Dec} generates another parallel resonant peak in Z_{IN}, as illustrated in Figure 3-17 (a). If C_{Dec} is not large enough, such as

500 pF in the figure, L_1 will not be fully decoupled from the original power stage. The result of such a condition is to have two resonant peaks in Z_{IN} sitting close to each other in frequency, and the impedance of the lower-frequency peak is not significantly reduced. In the time domain, this translates to the non-sinusoidal ringing in the MOSFET's V_{DS} waveform, and the voltage overshoot is not reduced a lot either, as seen in Figure 3-17 (b).

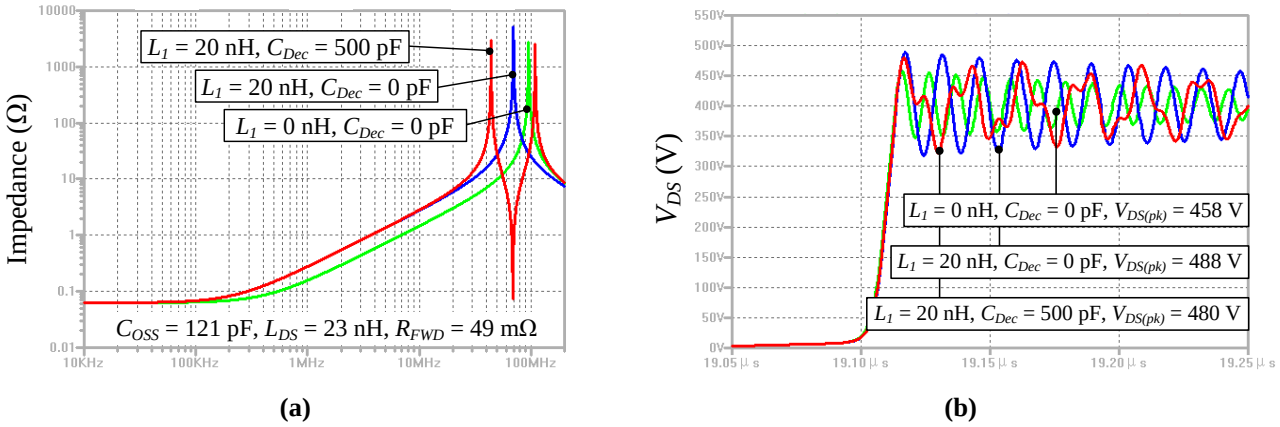


Figure 3-17. Influence of C_{Dec}: Not fully decoupled condition. (a) AC simulation of Z_{IN}, (b) transient simulation of MOSFET V_{DS} turning off 400 V, 10 A

As one keeps increasing C_{Dec}, the higher-frequency peak tends to merge with the original peak formed by L_{DS} and C_{OSS} only. Meanwhile, the lower-frequency peak tends to move to even lower frequency, and its peak impedance also decreases accordingly. This is illustrated in Figure 3-18 (a). In the switching waveforms shown in Figure 3-18 (b), by inserting 15 nF, the voltage overshoot can be reduced by 28 V, but further increasing C_{Dec} to 50 nF will only have a minor improvement – the over-voltage is reduced by only 9 V. Plus, as the higher-frequency peak is almost unchanged in the Bode plot, the 95 MHz ringing is almost the same for 15 nF and 50 nF conditions in the

switching waveforms. Therefore, as long as C_{Dec} becomes large enough, L_1 can be fully decoupled and will no longer affect the higher-frequency ringing, which in this condition is solely determined by C_{OSS} and L_{DS}.

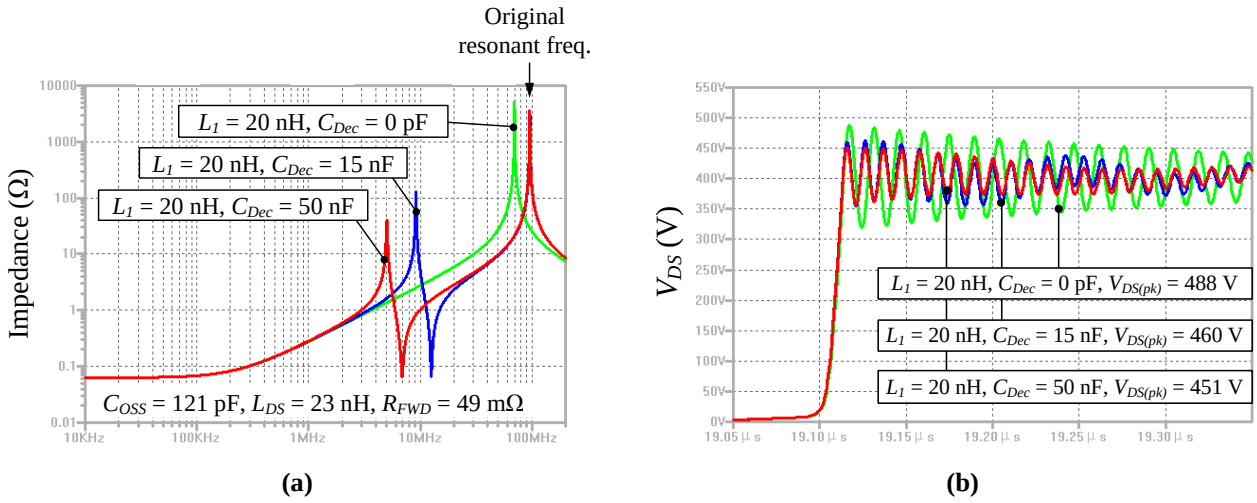


Figure 3-18. Influence of C_{Dec}: Fully decoupled condition. (a) AC simulation of Z_{IN}, (b) transient simulation of MOSFET V_{DS} turning off 400 V, 10 A

A simple calculation can be carried out to determine the effective C_{Dec} to achieve a fully decoupled condition. Basically, the impedance of $|L_1//C_{Dec}|$ needs to be much smaller than that of L_{DS} at $\omega_{PR} \approx 1/\sqrt{L_{DS}C_{OSS}}$, so that it does not affect the resonance between L_{DS} and C_{OSS}. Assuming that

$$L_1 = nL_{DS}, \text{ and } C_{Dec} = mC_{OSS}, \tag{3-8}$$

where n and m are positive real numbers, one has

$$\left| \frac{j\omega_{PR}L_1 \cdot \frac{1}{j\omega_{PR}C_{Dec}}}{j\omega_{PR}L_1 + \frac{1}{j\omega_{PR}C_{Dec}}} \right| << \left| j\omega_{PR}L_{DS} \right|. \tag{3-9}$$

By plugging in $\omega_{PR} = 1/\sqrt{L_{DS}C_{OSS}}$, it is easy to derive that

$$m >> 1 + \frac{1}{n}. \tag{3-10}$$

If assuming $n \geq 1$, one has $m >> 2$, meaning that C_{Dec} needs to be at least 20 times larger than C_{OSS} from the engineering point of view. Since C_{OSS} is usually a small value at high V_{DS} bias, e.g. tens to hundreds of pF, C_{Dec} can be 50 to 100 times higher in practical design, which falls in the range of a few nF to tens of nF. This rule of thumb can be verified in Figure 3-19, where the frequency and impedance of the higher-frequency peak in Z_{IN} are plotted versus m. The two asymptotes are the single-peak resonant frequency and impedance formed by L_{DS} and C_{OSS} only. It can be seen that when m is greater than 50, both curves will merge close enough to the asymptotes, indicating a good decoupled condition. Note that Figure 3-19 is plotted using the same circuit parameters in Figure 3-16 through Figure 3-18, but the conclusion can be verified to be generally true for other circuit parameters.

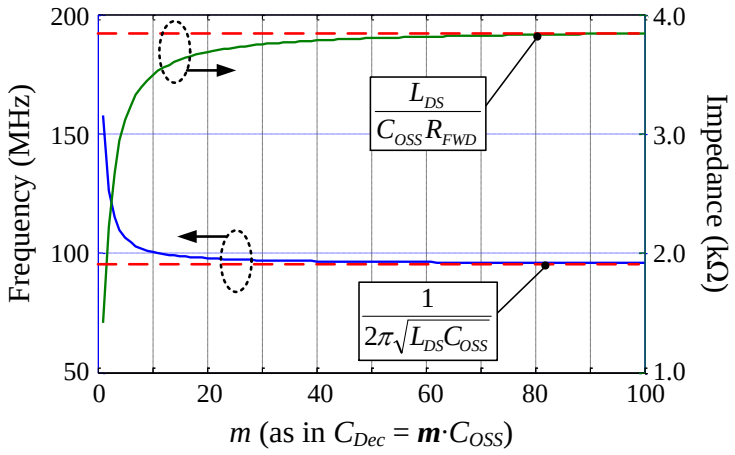
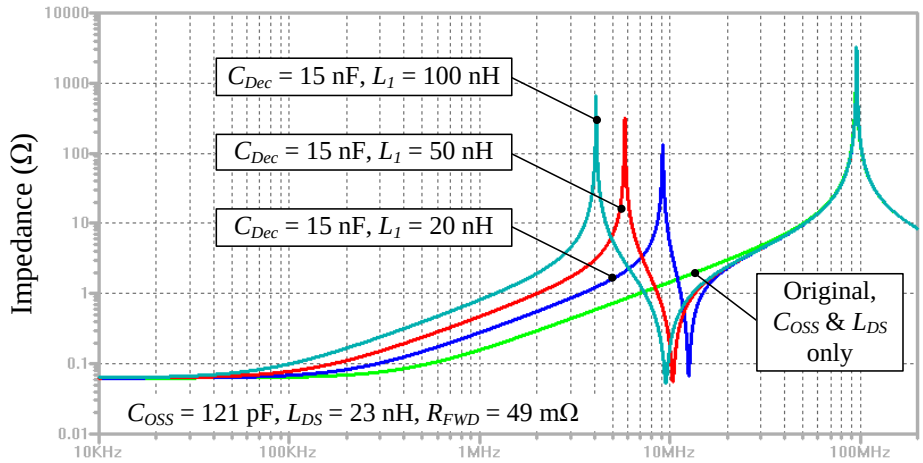


Figure 3-19. Resonant frequency and corresponding impedance of the higher-frequency peak in Z_{IN} as a function of m

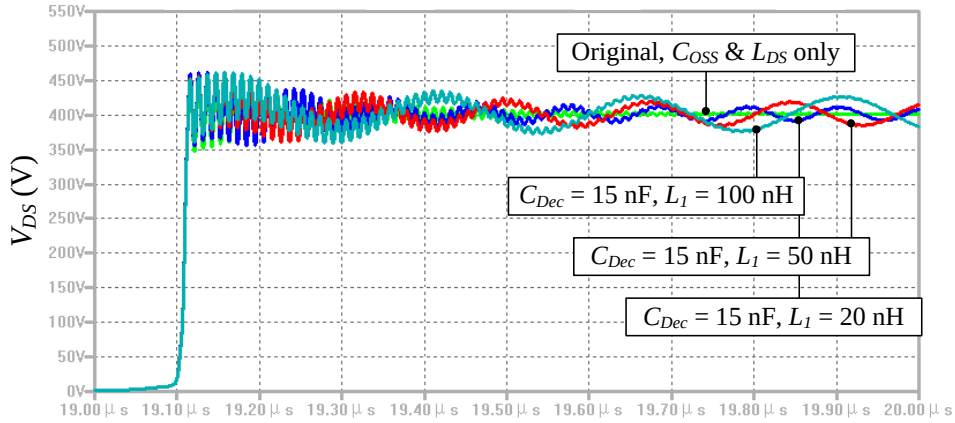
(C_{OSS} = 121 pF, L_{DS} = 23 nH, R_{FWD} = 49 mΩ, and L_1 = 20 nH)

The above analysis leads to several facts about the effect of decoupling capacitors. Generally, C_{Dec} needs to be placed as close as possible to the power stage to minimize L_{DS}, and 50 to 100 times C_{OSS} is a sufficient value for C_{Dec} to achieve the decoupling effect. Further increasing C_{Dec} will not help improve the ringing caused by L_{DS} and C_{OSS}, which is determined by the packaging technology (e.g. the parasitics inside a power module) and the device characteristics. When fully decoupled, L_1 will not affect the high-frequency ringing, but will generate another resonant peak with C_{Dec} located at $1/\sqrt{L_1 C_{Dec}}$ and cause low-frequency oscillation. This effect can be seen clearly from Figure 3-20. In this figure, C_{Dec} is selected as 15 nF, which is around 124 times C_{OSS}. Although the stray inductance L_1 increases from 20 to 100 nH, the higher-frequency resonant peak at 95 MHz does not change, and the corresponding ringing waveform is not affected either. Nevertheless, the parallel resonance from C_{Dec} and L_1 will have lower resonant frequency and higher peak impedance as L_1 increases, which, in the turn-off V_{DS} waveform, translates to an undesirable low-frequency oscillation with high amplitude.

Since the device over-voltage is affected by both high- and low-frequency ringing, it is also important to minimize L_1 and appropriately increase C_{Dec} to reduce the peak impedance at resonance. If L_1 cannot be further reduced, distributed decoupling capacitors should be used along the DC bus, between the V_{DC} source and the power stage. In this more complicated situation, the previous analysis about the MOSFET D-S input impedance can still be utilized in either simulation or measurement to properly select and place the distributed capacitors.



(a)



(b)

Figure 3-20. Influence of L_1 under fully decoupled condition. (a) AC simulation of Z_{IN}, (b) transient simulation of MOSFET V_{DS} turning off 400 V, 10 A

3.4.2 Experimental Verifications

The previous analysis is verified experimentally using a double-pulse tester circuit, as shown in Figure 3-21 (a). The DC voltage source V_{DC} and the bulk capacitors C_{Bulk} are connected to the tester PCB via twisted wires. Since the switching current is mainly provided by C_{Bulk}, the distance between the PCB and these capacitors is relatively closer, with the wire inductance falling in the range of tens of nH. Several DC-link distributed capacitors C_{Dis} are placed at the DC voltage entrance of the board. During the test, a 600

V Si CoolMOS in TO-247 package is used and paired with a 600 V SiC Schottky diode in TO-220 package. The stray inductance between the switch pair and C_{Dis} is intentionally enlarged on the tester PCB, so that the parasitic ringing and the effect of decoupling capacitors can be exaggerated and more clearly seen. The verifications are twofold: First, by using an impedance analyzer Agilent 4294A, small-signal measurements are performed across the MOSFET's D-S terminals to examine its impedance under 400 V turn-off bias. Second, the double-pulse switching tests are conducted at the same V_{DC} to investigate the parasitic ringing. The decoupling capacitance C_{Dec} is varied in these experiments to study its effects.

The impedance analyzer has a frequency sweep limit of 110 MHz, which is another reason to intentionally design a bad layout on the tester PCB, because the parasitic ringing for such a low-current MOSFET can easily exceed 150 MHz on a properly designed, low-inductance layout. Another consideration in the impedance measurement is that the instrument's measurement terminals cannot take more than 40 V DC bias, and thus a blocking capacitor C_{Block} needs to be used, as shown in Figure 3-21 (b). In order to correctly detect the resonant peaks, the selected C_{Block} should have enough voltage rating, large capacitance, and low stray inductance. In this work, a 500 V, 1 μF ceramic capacitor is chosen. Also note in this figure that the freewheeling diode is simply shorted to mimic its DC operating point, and the MOSFET's G-S terminals are also shorted to bypass its gate capacitance C_{GS}.

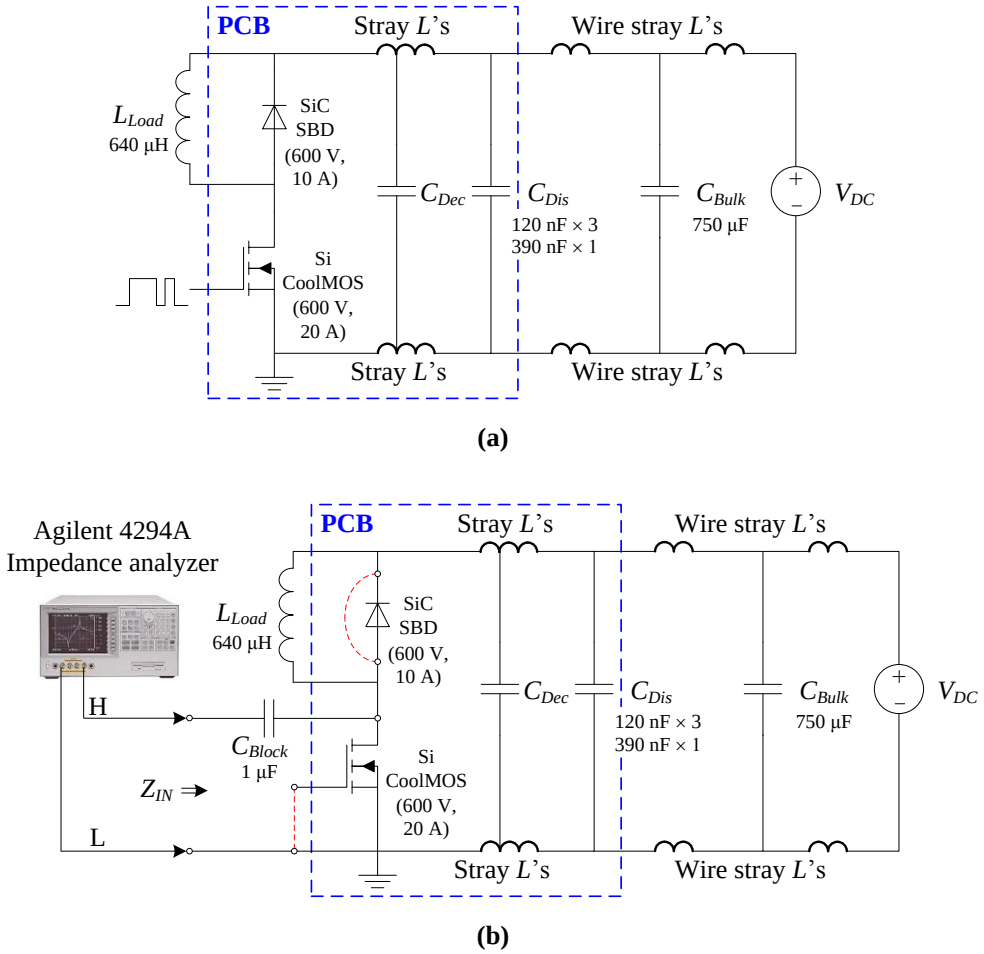


Figure 3-21. Double-pulse circuit used to verify the analysis
(a) Switching test configuration, (b) impedance measurement configuration

Figure 3-22 shows the impedance measurement results at four discrete values of C_{Dec}, and Figure 3-23 (a)-(d) show the corresponding turn-off waveforms of the MOSFET switching 400 V and 10 A load with 10 Ω gate resistance. As seen in Figure 3-22, without any C_{Dec} placed between the switch pair and C_{Dis}, a single-peak resonance can be detected at 52.2 MHz. Considering that C_{OSS} of the MOSFET is approximately 90 pF at 400 V bias, the switching loop inductance can be estimated by Eq. (3-5) to be 103 nH, which includes the inductances from the PCB and the device packages. In the switching waveforms, the parasitic ringing in V_{DS} and I_D occurs at a very close frequency

of 48.1 MHz, with a voltage overshoot of 96 V. The ringing frequency is slightly lower than the resonant frequency, because the freewheeling diode related stray inductances are bypassed in the impedance measurement.

When C_{Dec} = 500 pF (about 5.6x C_{OSS}) is inserted into the circuit, the single-peak resonance seen by the MOSFET splits into two peaks, with the higher-frequency one at 79.4 MHz and the lower one at 25.4 MHz. As mentioned previously, 500 pF is not large enough to provide sufficient decoupling effect, so it causes the two resonant peaks to be close in frequency. That is why in the switching waveforms in Figure 3-23 (b), the two frequency components in V_{DS} are hard to differentiate at the beginning of the ringing. However, the higher-frequency ringing decays more rapidly, so the 25.7 MHz oscillation can still be identified towards the end of the turn-off transient, which is consistent with the impedance measurement.

In the last two conditions, both 5.4 nF (about 60x C_{OSS}) and 22 nF (about 244x C_{OSS}) would provide sufficient decoupling effect according to the previous analysis. From the small-signal measurement, the higher-frequency resonance occurs at 75.8 MHz for the 5.4 nF case, which tends to merge to about 72.4 MHz when C_{Dec} increases to 22 nF and beyond. The lower-frequency peak, on the other hand, moves from 8.1 MHz to 3.7 MHz with reduced peak impedance. Since now the two resonant peaks are far apart in the Bode plot, both ringing frequencies can be identified in the time-domain waveforms shown in Figure 3-23 (c) and (d). Again, the higher-frequency ringing in the waveforms exhibits lower frequency value than the impedance measurement, also due to the diode-related stray inductances. The V_{DS} overshoots in these two cases are very similar (72 V to 68 V), but it is obvious that the lower-frequency oscillation is improved with larger C_{Dec}.

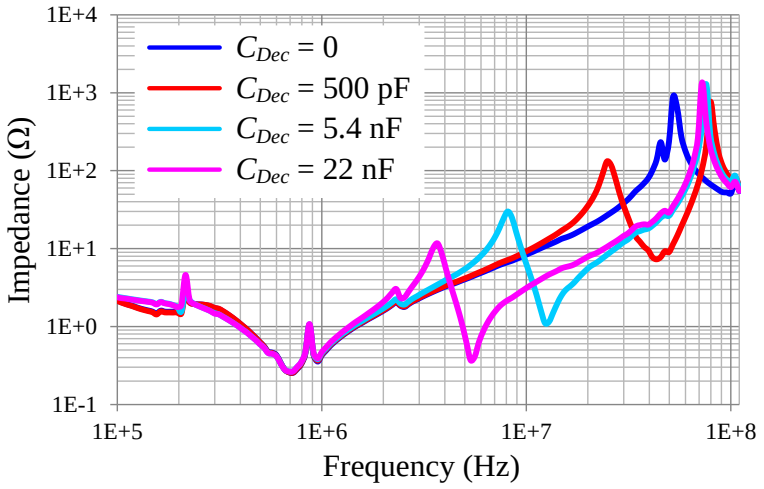


Figure 3-22. Impedance measurements at V_{DC} = 400 V

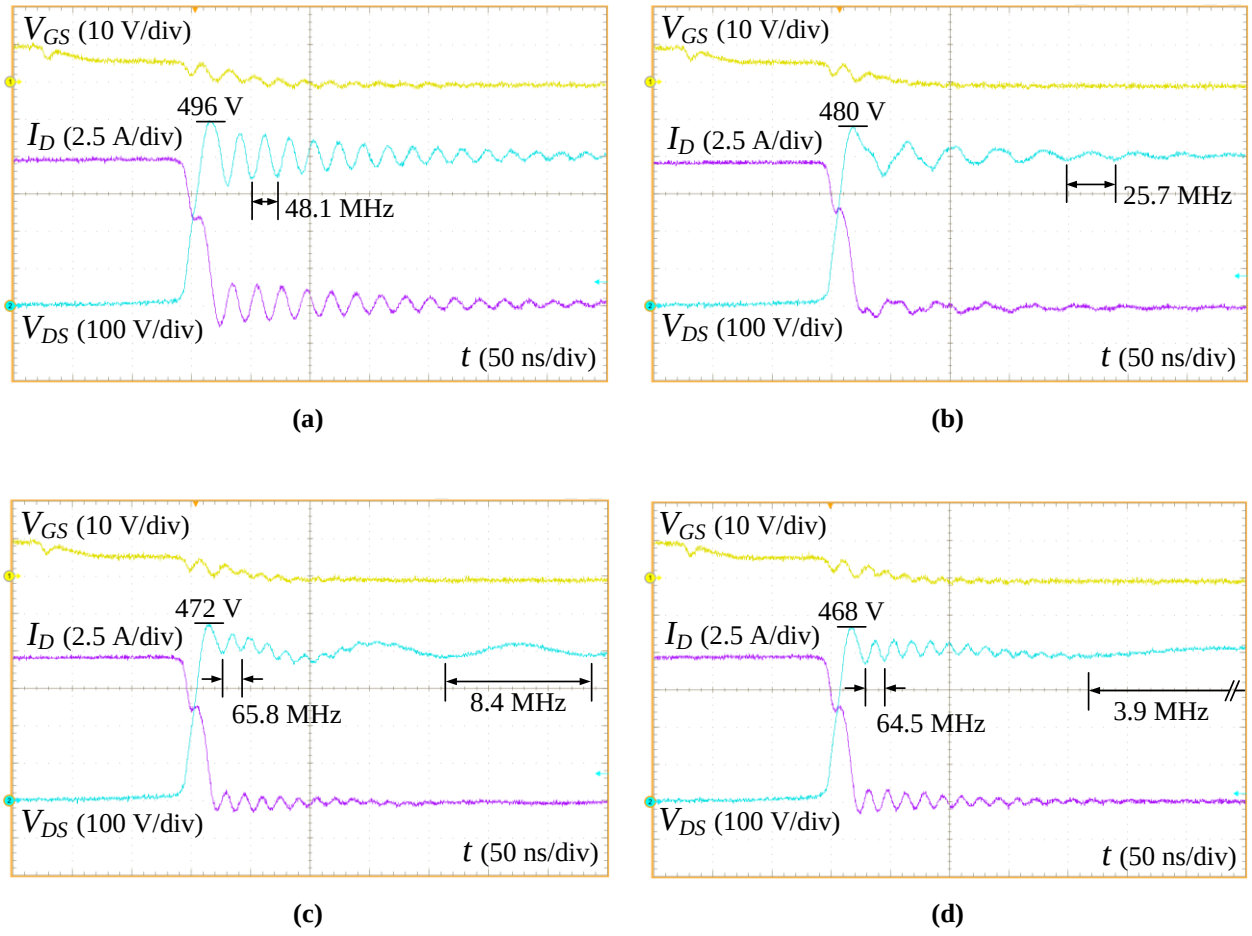


Figure 3-23. Turn-off waveforms of the MOSFET switching 400 V and 10 A

(a) C_{Dec} = 0, (b) C_{Dec} = 500 pF, (c) C_{Dec} = 5.4 nF, (d) C_{Dec} = 22 nF

Figure 3-24 plots how the V_{DS} overshoot in experiments reduces with the increasing C_{Dec}. As seen, the device over-voltage drops quickly at the beginning when small C_{Dec} is introduced, but as C_{Dec} increases, it tends to have less and less effect on reducing the device stress. This saturation trend starts roughly at C_{Dec}/C_{OSS} = 50, from which point C_{Dec} needs to increase by 4 times to achieve only 6% reduction in V_{DS} overshoot. This result is consistent with the observation in [13], but the phenomenon can be well explained by the much simpler small-signal model in this analysis instead of investigating the EMI noise.

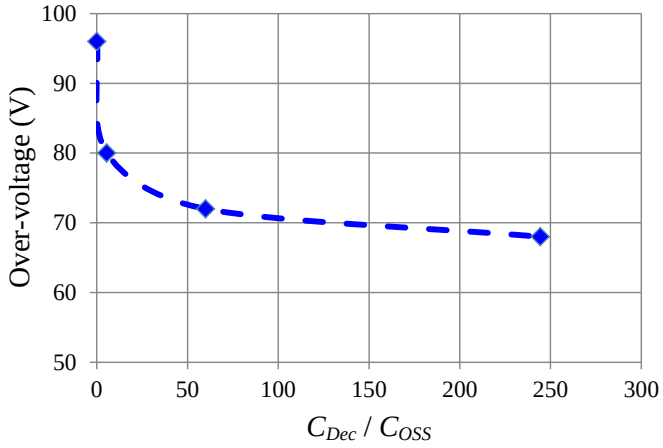


Figure 3-24. MOSFET over-voltage stress vs. C_{Dec}/C_{OSS}

Note that for the simplicity of analysis, the small-signal model in Figure 3-15 does not consider the stray inductances of the decoupling capacitors. This is based on the consideration that in real converter designs, multiple low-inductance capacitors can usually be paralleled to further reduce the inductive effect, so that it will not affect the results of the analysis. Although the double-pulse circuit is studied in this work, the conclusion stays true for the more general phase-leg configuration, except that C_{OSS} needs to be replaced by C_{OSS} + C_J, where C_J is the junction capacitance of the anti-parallel

diode. This lumped small-signal model has been proven effective in the design of a 1200 V, 60 A SiC MOSFET module, whose parasitic ringing frequency is not very high (< 100 MHz) due to the relatively large device capacitances and package stray inductances. This work will be discussed in detail in Chapter 5. However, in the circumstances where both *C* and *L* are small and hence the frequency of interest is high (> 100 MHz), distributed component (or even PCB) models may need to be considered in the small-signal analysis in order to obtain more accurate results.

3.5 Conclusions

In this chapter, the influences of stray inductances on power MOSFET switching behaviors are firstly investigated through an experimental parametric study. The study again points out that the main switching loop inductance contributes most to the parasitic ringing in the MOSFET switching waveforms by resonating with the device junction capacitances. It is also discovered from the study that the common source inductance, commonly known to originate from the shared current path between the gate and the main switching loops, can still come from the magnetic coupling effect between the two loops even if Kelvin connection is used, and, because of that, an equivalent negative common source inductance is also possible. This means that Kelvin connection alone is not sufficient to ensure a minimum common source inductance, and more attention needs to be paid to the layout between the gate driver loop and the main switching loop.

A small-signal model is then derived in this chapter to explain the mechanism of the MOSFET turn-off ringing in the frequency domain. The model establishes the relationship between the device's parasitic ringing at turn-off, and the terminal impedance seen by the device during this process. Compared to the time-domain analysis,

the frequency-domain view angle is more straightforward to understand, and provides a deeper insight into the problem. The same model is then extended to analyze the effect of decoupling capacitors in suppressing the ringing by relocating the resonant frequency and peak impedance of the parallel resonant network. Using frequency-domain analysis, quantitative results can be obtained independent of the device's switching speed. A rule of thumb is also derived from this study about the selection of appropriate decoupling capacitance.

3.6 References

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Chapter 4 Design of General-Purpose, High-Speed Discrete Phase-Leg PEBBs and Behavioral Comparison of Si and SiC Power MOSFETs for High-Frequency Applications

4.1 Introduction

The concept of the Power Electronics Building Block (PEBB) is aimed at achieving better performance, higher reliability, and lower cost for power electronics systems, where a converter can be built quickly and reliably by just connecting several PEBB modules together, without considering the physical realization inside the PEBB [1]. Such a concept makes the PEBB different from conventional power modules in that it integrates not only the power-stage devices, but also the peripheral circuits and functions, such as the gate drive, protection, signal conditioning, and voltage/current monitoring, etc. In this sense, a PEBB is a "smarter" power module, and is more user-friendly in building converters with it – the converter and the PEBB modules will be interfaced by only digital I/O's which dictate and monitor the operation of the module, and the power terminals which form the infrastructure of the converter. The target of the PEBB design is then to make the PEBB function as much like an ideal switch as possible. To this end, a

critical design challenge is to achieve fast switching of the power devices in the PEBB, while keeping the device stresses (over-voltage and over-current) minimized.

For practical applications, a basic building block is usually defined at the phase-leg level, as this is the most commonly used sub-circuit in many topologies. To name a few, Figure 4-1 shows the phase-shifted full-bridge converter for DC-DC applications, and the voltage-source inverter for three-phase applications, with the phase-leg highlighted as the basic subsystem. Modularization and integration of PEBBs at this level will provide many advantages towards converter constructions, such as moderate design complexity, and maximum application flexibility.

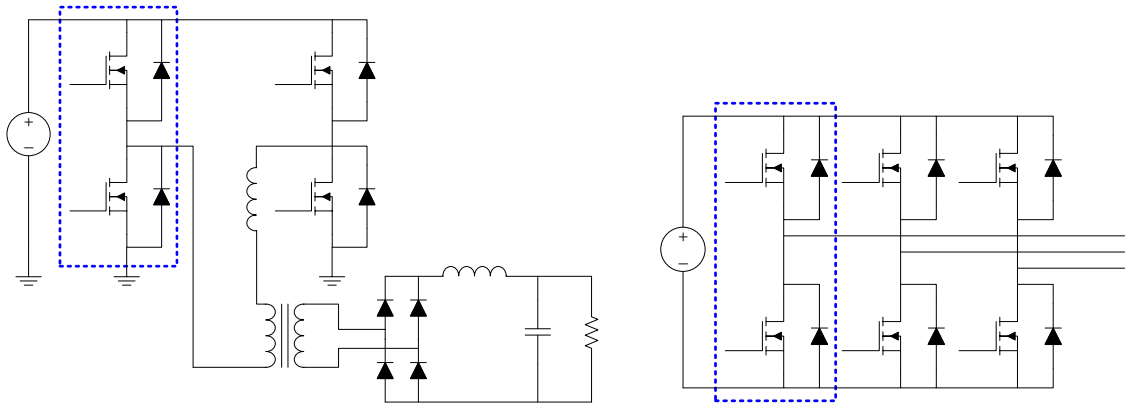


Figure 4-1. Phase-shifted full-bridge converter (a) and voltage-source inverter (b) with phase-legs highlighted as the basic sub-circuits

With their superior electrical and thermal properties, the SiC unipolar switches are promising to replace the dominant Si IGBTs in the medium- to high-voltage applications, achieving higher switching frequency and power density for the converter [2]-[4]. To this end, this chapter firstly presents the modularized design of a general-purpose, high-speed phase-leg PEBB utilizing Cree's commercial SiC MOSFETs (CMF20120D) and SiC

Schottky diodes (C2D10120D), for the converters operating at 600-800 V, and up to 500 kHz. To achieve these goals, a high-speed gate driver with active Miller clamp circuit is designed to drive the MOSFET as fast as possible, while avoiding the potential false trigger issue from the cross-talk effect. The proposed control and dead-time insertion functions allow the phase-leg to operate in 0-100% duty cycle range and various circuit topologies, and meanwhile ensure safe switching of the module without shoot-through failures. Furthermore, the circuit layout of the power stage is also optimized by rearranging the device positions, so that the switching loop inductance, and the resultant parasitic ringing due to the fast switching, can be minimized.

While SiC MOSFETs have shown evident advantages over Si IGBTs in both conduction and switching performances [5]-[7], how these devices are different from their Si counterparts in the detailed device characteristics, and whether they are directly interchangeable in terms of driving, etc., have not been fully discussed. To answer these questions, this chapter also conducts a comprehensive comparison of the two devices in their static characteristics, switching performances, temperature behaviors, and finally, loss distributions in a high-frequency DC-DC converter. As 1200 V Si MOSFETs suffer from large specific $R_{DS(on)}$ due to the material limit, the comparison here is made between a 1200 V, 20 A SiC MOSFET, and a 600 V, 46 A Si CoolMOS, both representing the state-of-the-art technology in their respective domain. For the comparison purpose, the aforementioned PEBB circuit is also designed to be compatible with Si MOSFETs, and therefore is used in this study to evaluate the switching performances of both the Si and SiC phase-legs under the same circuit conditions. For the comparison of loss distributions, because of different device voltage ratings, this work also assumes a power

conversion application that uses the same topology, transfers the same power, but can be realized with different voltage levels. Through these comparisons, design considerations can be summarized about using SiC MOSFETs in high-frequency converters.

4.2 Modularized Design of a General-Purpose, High-Speed Phase-Leg PEBB Based on SiC MOSFETs

4.2.1 Control Stage Design

The control stage of the PEBB is illustrated in Figure 4-2. As seen, the input gating signals are pre-conditioned through a dead-time generation block before reaching the gate drivers. The MOSFET gates are switched between +15 V and -2.5 V. The negative bias is used to increase the gate threshold margin and to reduce the cross-talk effect between top and bottom switches. An over-temperature protection function is added by comparing the MOSFET case temperatures with a preset reference value. When triggered, the protection will block the input signals, notify the upper-level controller, and light the LED indicators. Besides these, an additional shutdown signal is provided to turn off the entire phase-leg in case of a converter failure. To simplify the design, a single CPLD (Xilinx XC9536-15VQ44I) is utilized to coordinate all the digital control functions.

The dead-time generation block accepts independent top and bottom input signals to maximize the driving flexibility for the PEBB. To prevent possible shoot-through failure, the driving signals will be generated with an intrinsic minimum dead time $t_{Instrinsic}$, whose value is determined according to the switching speed of the SiC MOSFETs. When the input signals have a dead time $t_{Controller}$ less than $t_{Instrinsic}$, this block will simply output the actual dead time as $t_{Instrinsic}$. In certain conditions where a longer dead time is needed,

the driving signals can still be actively adjusted by the inputs. This function is important for the phase-leg to keep its generality in different topologies and to ensure its safe operation under all conditions. The behavior of the dead-time generation function can be described by the following equation:

$$t_{DeadTime} = \begin{cases} t_{Intrinsic} & \text{if } t_{Controller} \le t_{Intrinsic} \\ t_{Controller} & \text{if } t_{Controller} > t_{Intrinsic} \end{cases}. \tag{4-1}$$

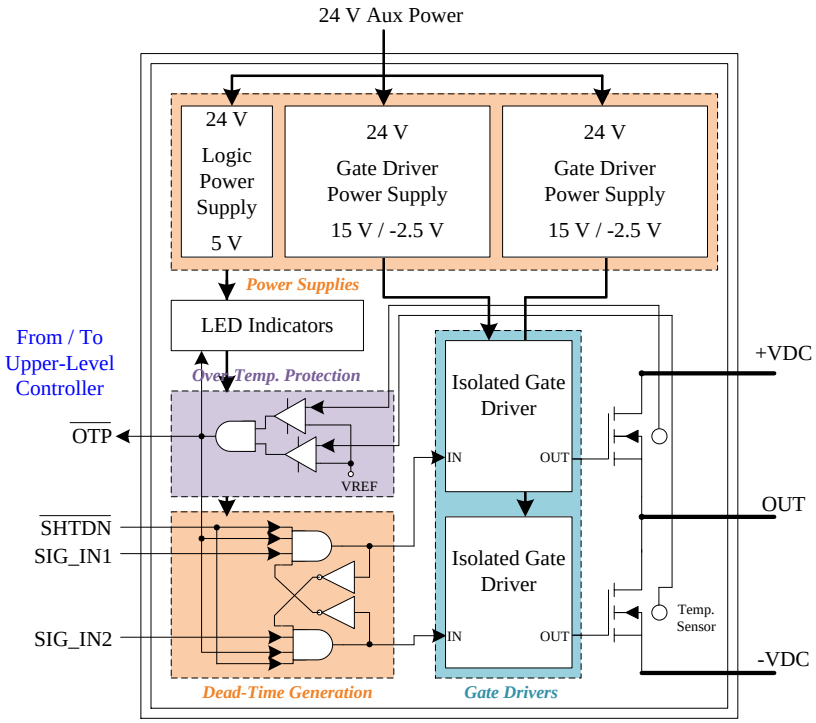


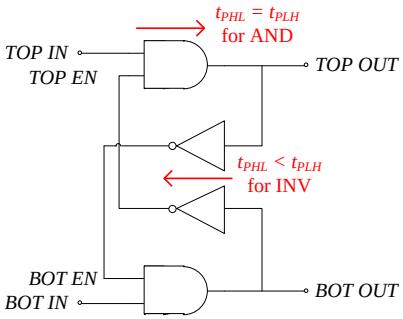
Figure 4-2. Control stage of the PEBB

Figure 4-3 (a) and (b) show the digital logic and the corresponding truth table to realize the function of Eq. (4-1). Similar to an R-S flip-flop, whether an input signal can pass through the AND gate depends on its enable input (e.g. *TOP EN*), which is further dependent on the output state of the other AND gate. Based on that, the key to realizing the minimum dead time is then to have different propagation delays of the inverter gates

for the low-to-high (t_{PLH}) and high-to-low (t_{PHL}) edges, and more specifically, $t_{PLH} > t_{PHL}$. Any input dead time less than t_{PLH} will thus be force delayed to t_{PLH} (= $t_{Intrinsic}$).

Figure 4-3 (c) exhibits a timing diagram example to better illustrate this function. Two conditions are displayed: The first portion of the diagram shows the case of $t_{Controller} < t_{Intrinsic}$, while the latter shows $t_{Controller} > t_{Intrinsic}$. Assume that the initial conditions for *TOP IN* and *BOT IN* are H (High) and L (Low) respectively. It is easy to derive that *TOP EN* = H, *BOT EN* = L, and *TOP OUT* = H, *BOT OUT* = L. When *TOP IN* changes to L, *TOP OUT* becomes L after the AND delay time. Because *BOT IN* becomes H after $t_{Controller}$, which is less than the low-to-high propagation delay t_{PLH} of the inverter, *BOT OUT* needs to wait for *BOT EN* to swap its state. Therefore, although the dead time of the input signal is $t_{Controller}$, the real dead time seen by the gate driver is actually t_{PLH}, or $t_{Intrinsic}$. On the other hand, if assuming the initial conditions are *TOP IN* = L and *BOT IN* = H, it is easy to see that *TOP EN* = L, *BOT EN* = H, and *TOP OUT* = L, *BOT OUT* = H. *BOT IN* swaps to L first, and after $t_{Controller}$, *TOP IN* swaps to H. Because $t_{Controller}$ is longer than t_{PLH} this time, *TOP EN* has already become H before *TOP IN* changes to H state. Therefore, the output signals will have the same dead time of $t_{Controller}$ as the input signals.

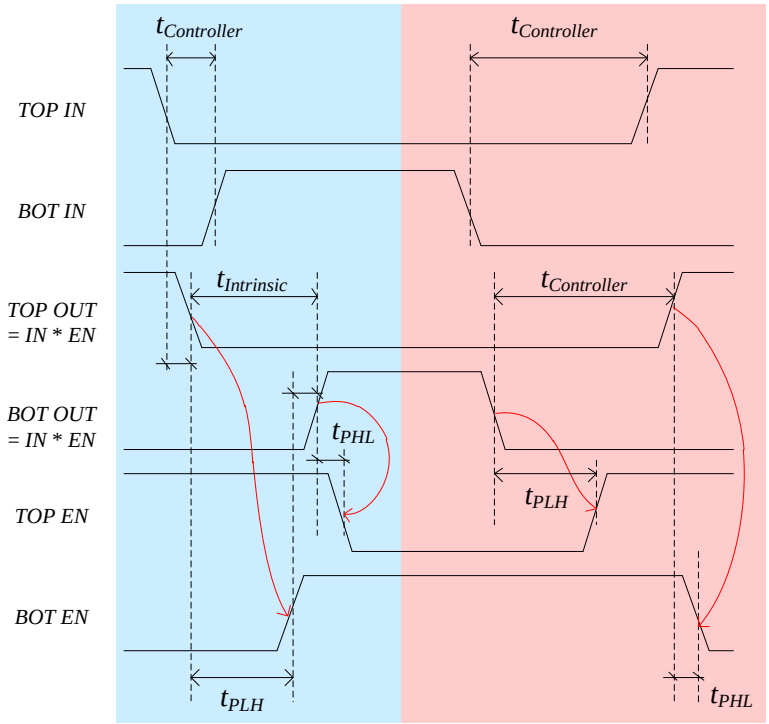
Figure 4-4 (a) and (b) show the digital logic of the asymmetric inverter implemented with the CPLD. As seen, an input signal is passed through two channels with different delays, and then recombined by the multiplexer to produce the different delay times for the rising and falling edges.



(a)

TOP IN	*BOT IN*	*TOP OUT*	*BOT OUT*
0	1	0	1
1	0	1	0
0	0	0	0
1	1	Previous state	

(b)



(c)

Figure 4-3. Realization of the dead-time generation function. (a) Digital logic, (b) truth table, (c) timing diagram showing two conditions: $t_{Controller} < t_{Intrinsic}$ and $t_{Controller} > t_{Intrinsic}$

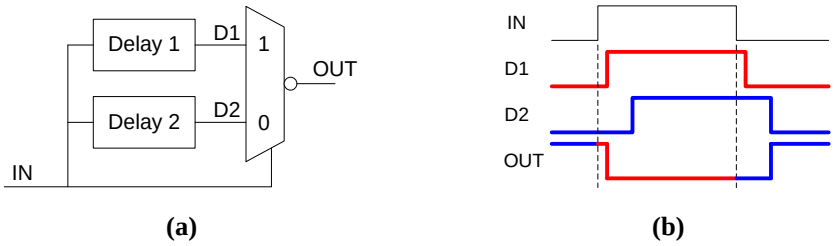


Figure 4-4. CPLD implementation of the inverter with asymmetric propagation delays (a) Digital logic, (b) timing diagram

4.2.2 Gate Driver Design

Besides transmitting the driving signals across its isolation barrier that separates the control circuit from the power stage, the gate driver of the PEBB also needs to source and sink large enough transient currents in order to push the switching speed of the MOSFET. However, a critical problem of doing this is the potential *dv*/*dt* induced turn-on of the device, which is a common issue for MOSFETs and IGBTs [8][9]. The problem is illustrated in Figure 4-5. When the top switch is turned on in a phase-leg, a positive *dv*/*dt* will occur on the bottom switch as it starts to block the bus voltage V_{DC}. This *dv*/*dt* injects a current into the gate loop of the bottom switch through its Miller capacitance, which produces a voltage drop on the gate resistor, and correspondingly, a voltage spike on the gate. This phenomenon is often referred to as "cross-talk". If this spike exceeds the turn-on threshold of the MOSFET, the switch will be falsely triggered, and a shoot-through event will happen, causing catastrophic failure of the phase-leg. The cross-talk issue is usually less serious for IGBTs due to their slower switching speed and the symmetric driving voltage (e.g. ±15 V) that increases the threshold margin. However, for the SiC MOSFET in this work, the solution is not so straightforward, not only because of its higher *dv*/*dt*, but also due to the fact that the device has asymmetric absolute maximum

gate voltages (+25 V and -5 V, according to the datasheet). Extra measures need to be taken to avoid the false trigger issue.

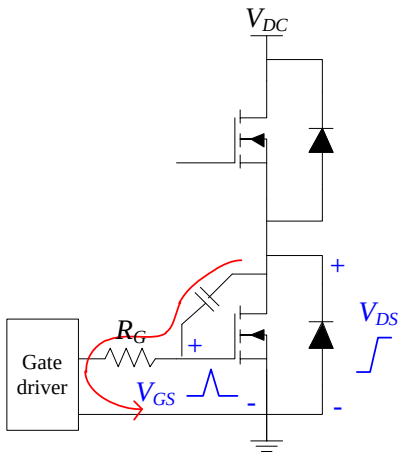


Figure 4-5. *dv*/*dt* induced turn-on due to the Miller effect

The false trigger event relies on two conditions: (1) The MOSFET should be in the static off-state; and (2) there is a positive *dv*/*dt* on the device's drain-source terminals due to the turn-on of the complementary switch. Both are commonly satisfied conditions for hard-switching phase-legs. Given these conditions, the following model can be used to qualitatively study the *dv*/*dt* limit of a MOSFET. As illustrated in Figure 4-6 (a), C_{GS} and C_{GD} represent the gate-source and Miller capacitances of the MOSFET, while R_G is a lumped resistance, including the MOSFET internal gate resistance R_{GI}, external gate resistance $R_{G(ext)}$, as well as the gate driver output resistance R_{Drive}.

To simplify the analysis, it is assumed that both capacitances are linear, and a voltage source with a constant ramp rate (dv_{DS}/dt = constant) is applied to the drain-source terminals. Therefore, one has

$$C_{GD}\frac{d\left(v_{DS}-v_{GS}\right)}{dt}=\frac{v_{GS}}{R_G}+C_{GS}\frac{dv_{GS}}{dt}. \tag{4-2}$$

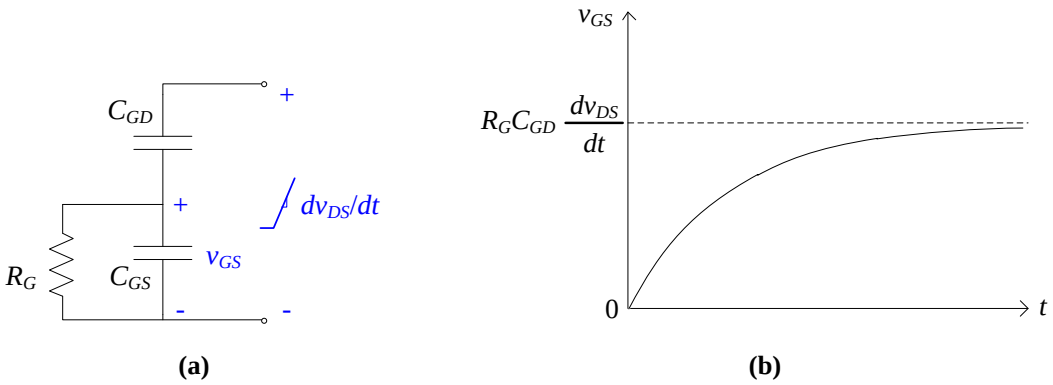


Figure 4-6. MOSFET *dv*/*dt* limit model (a) and time-domain waveform of the model (b)

Rearrange Eq. (4-2) and one can get

$$v_{GS} = R_G C_{GD} \frac{dv_{DS}}{dt}\left(1 - e^{-\frac{t}{\tau}}\right), \tag{4-3}$$

where the time constant τ is given by

$$\tau = R_G (C_{GS} + C_{GD}) = R_G C_{ISS}. \tag{4-4}$$

The time-domain waveform of Eq. (4-3) is displayed in Figure 4-6 (b). As seen, the gate voltage v_{GS} approaches its steady state exponentially. The asymptote is proportional to R_G, C_{GD}, and dv_{DS}/dt, while the approaching speed is determined by R_G and C_{ISS}.

Let $R_G = R_{GI}$, meaning that the gate of the MOSFET is directly shorted to its source, and assume

$$R_{GI} C_{GD} \frac{dv_{DS}}{dt} > V_{GS(th)}, \tag{4-5}$$

then

$$\frac{dv_{DS}}{dt} > \frac{V_{GS(th)}}{R_{GI} C_{GD}}. \tag{4-6}$$

This means that under such a dv_{DS}/dt, the induced turn-on will happen as long as the v_{DS} ramp is applied for long enough time. For this reason, the term $V_{GS(th)}/(R_{GI}C_{GD})$ is usually defined as the MOSFET natural dv/dt limit [10].

However, if

$$R_G C_{GD} \frac{dv_{DS}}{dt} < V_{GS(th)}, \tag{4-7}$$

then the false trigger will not happen under this voltage ramp.

A more commonly seen condition is

$$R_G C_{GD} \frac{dv_{DS}}{dt} > V_{GS(th)}. \tag{4-8}$$

Under such a condition, whether the induced turn-on happens or not depends on the time constant of $R_G C_{ISS}$. As long as dv_{DS}/dt (i.e. the turn-on transient) ends before v_{GS} reaches the threshold voltage, the MOSFET will not be falsely triggered.

Eq. (4-3) through (4-8) qualitatively explain the influences of circuit parameters on the cross-talk effect, from which the following methods can be concluded to mitigate the false trigger problem [11]:

(1) Reducing the gate loop total resistance R_G at turn-off. This method mainly lowers the v_{GS} asymptote to be below $V_{GS(th)}$ under dv_{DS}/dt, as suggested by Figure 4-6.

(2) Paralleling an extra capacitance to the gate-source terminals. This is to increase the time constant and postpone the moment when v_{GS} hits the threshold, so that the false trigger will not happen during the switching transients. However, the disadvantages are longer switching delays, slower switching speed, and more gate drive power consumption.

(3) Providing a negative turn-off bias $-V_{G(off)}$. This will increase the gate threshold margin from $V_{GS(th)}$ to ($V_{GS(th)}$ + $V_{G(off)}$), but will also complicate the gate driver design.

The gate drive circuit design in this work combines the methods of (1) and (3). As shown in Figure 4-7, Avago ACPL-331J optocoupler with active Miller clamp function is selected to be the isolation barrier [12]. The Miller clamp function is further enhanced by an additional PNP transistor (DIODES DPLS325E) connected between the MOSFET gate and the negative bias V_{EE} of the gate drive power supply. The base of the transistor is connected to the CLAMP pin of the optocoupler, which detects the gate voltage and judges the on/off state of the MOSFET. When the MOSFET is turned off, the CLAMP pin turns on the transistor, which forms a very low impedance path shorting the gate to V_{EE}, thus shunting the *dv*/*dt* induced Miller current and suppressing the consequent voltage spikes on the gate [11].

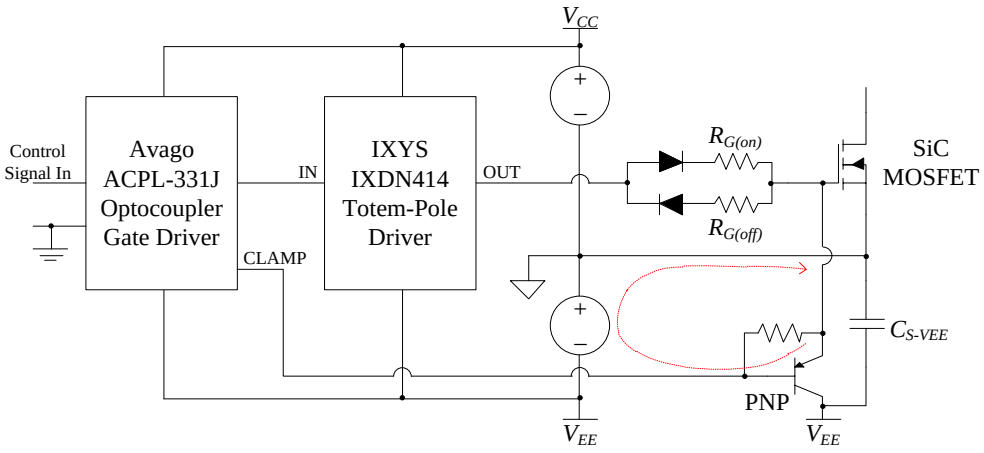


Figure 4-7. Gate drive circuit design

Following the optocoupler is an IXYS IXDN414 totem-pole driver, which boosts the peak driving current from 1.5 A to 14 A. +15 V/-2.5 V gate biases are used to achieve the low on-state resistance and increase the threshold margin. Note that although +20 V

turn-on bias is recommended for the SiC MOSFET to achieve the rated $R_{DS(on)}$, +15 V is used in this work for the gate driver to be also compatible with Si MOSFETs for the future comparison purposes. The bipolar biases are provided by two isolated DC-DC power supplies, with the output power of 1.5 W for the 15 V supply and 1 W for the 2.5 V one. Considering that the gate charge of the SiC MOSFET is around 75 nC with 15 V driving voltage, the gate drive power needed for 500 kHz operation can be calculated as [10]:

$$P_{Gate(on)} = V_{G(on)} \cdot Q_G \cdot f_{SW} \approx 15 \times 75 \times 10^{-9} \times 500 \times 10^{3} \approx 0.56\,\mathrm{W}, \tag{4-9}$$

which leaves enough margin for both power supplies. Moreover, the turn-on and turn-off speeds are independently controlled through two sets of Schottky diodes and gate resistors. All of these measures will ensure that the SiC MOSFET can be driven as fast as possible, while keeping the cross-talk effect minimized.

Special attention should also be paid to the PCB layout of the gate drive circuit. Not only should the gate drive loop be shortened as many have suggested, but the Miller clamp loop needs to be minimized as well, as indicated in Figure 4-7, by placing the PNP transistor as close to the main switch as possible. Furthermore, in case the V_{EE} supply is far from the MOSFET, a local bypass capacitor $C_{S\text{-}VEE}$, which is placed close to both the shunt transistor and the MOSFET, will also help reduce the stray inductance of the Miller clamp loop. Both simulation and experiments show a better clamping effect for this layout design.

4.2.3 Power Stage Design

The main switch of the PEBB is Cree's SiC MOSFET CMF20120D. Since the device's body diode has a high forward voltage, it is usually bypassed by an external SiC

Schottky diode to reduce the reverse conduction loss. In this work, Cree's 1200 V, 10 A SiC Schottky diode C2D10120D is chosen as the freewheeling diode (FWD) considering its compatible current rating.

In Chapter 3, it has been concluded that the main switching loop inductance contributes most to the parasitic ringing. This loop, however, is generally not optimized in conventional phase-leg layout designs, where the MOSFETs and their anti-parallel diodes are placed next to each other. Considering the current commutation process, a better layout can actually be achieved by putting the MOSFETs and their commutating diodes (i.e. the anti-parallel diodes of the complementary MOSFETs) close to each other, which can reduce the switching loop areas effectively.

Keeping this in mind, the designed PCB layout is shown in Figure 4-8. As seen, this design clearly separates the power and control stages of the PEBB, minimizing the interferences between the two parts. In addition, the top MOSFET is placed as close to the bottom FWD as possible to produce a smaller switching loop. Similar arrangement is implemented on the bottom MOSFET and top FWD as well. Parallel copper planes are also designed inside this four-layer PCB to form the DC buses (VDC+ and VDC-), together with eleven 1 kV, 22 nF ceramic capacitors distributed between the DC rails, providing a sufficient decoupling effect for the interconnect stray inductances between the PEBB module and the DC voltage source.

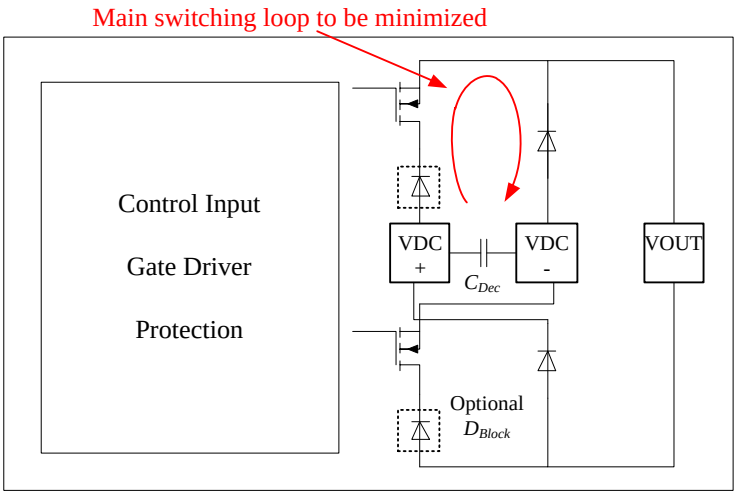


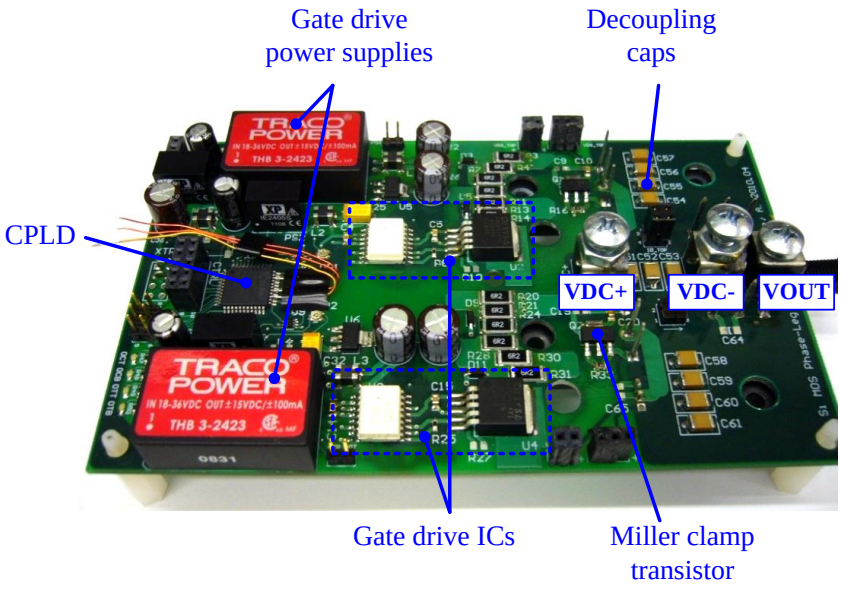
Figure 4-8. Optimized power stage layout of the PEBB circuit board

4.2.4 Experimental Verifications of the PEBB Design

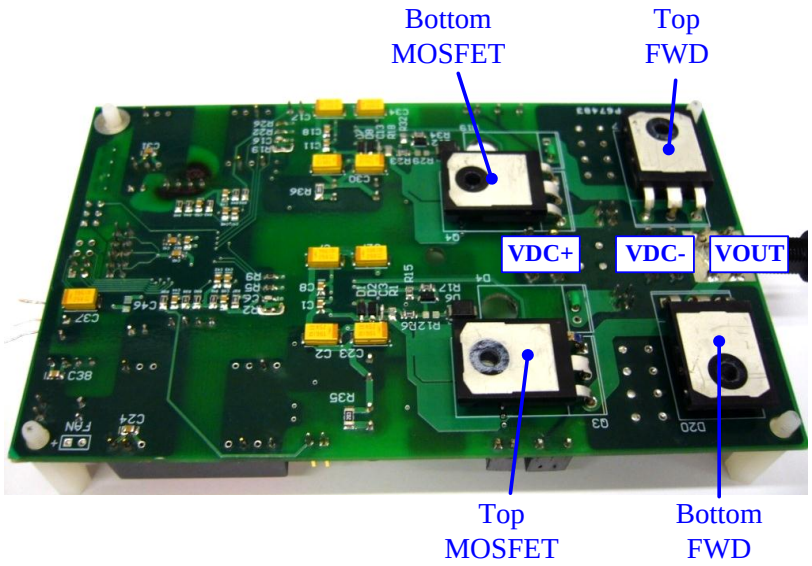
Figure 4-9 shows the SiC phase-leg PEBB. The CPLD, gate drivers, decoupling capacitors, as well as power terminals can all be clearly identified on the front side of this 5.58" × 3.35" board, as seen in Figure 4-9 (a). The power switches are all placed on the back side with their back plates facing downwards, so that they can be mounted on a cold plate for cooling.

(1) Dead-time generation test

Figure 4-10 displays the responses of the dead-time generation block from 500 kHz input signals, with 60% and 40% duty cycles respectively. As seen in Figure 4-10 (a), even though there are overlaps of on-state in the inputs, the outputs still keep the intrinsic dead time of 120 ns in this design. Nevertheless, when the input dead time is increased to 200 ns in the 40% duty cycle case, the output signals will just follow the inputs generating the same dead time.

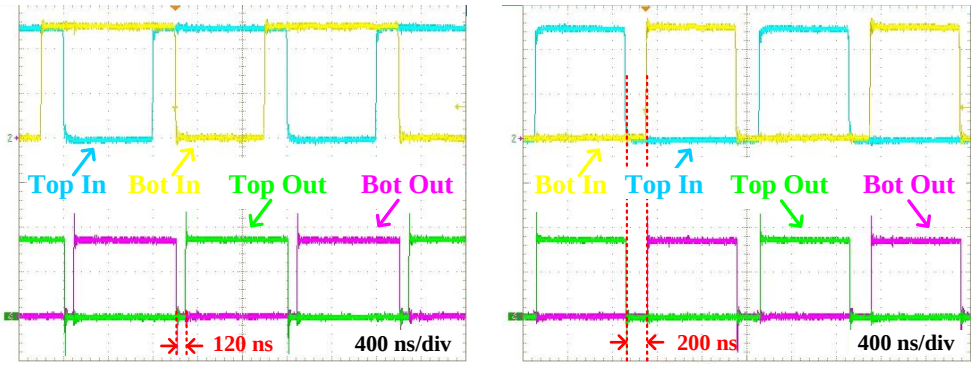


(a)



(b)

Figure 4-9. SiC phase-leg PEBB. (a) Front side, (b) back side



(a) **(b)**

Figure 4-10. Test waveforms of the dead-time generation
(a) 500 kHz, 60% duty cycle input, (b) 500 kHz, 40% duty cycle input

(2) Cross-talk test

The cross-talk effect is measured in a typical double-pulse test. During the test, the double-pulse signal is applied to the top MOSFET, while the bottom one keeps permanently off, as illustrated in Figure 4-11 (a). V_{DS} and V_{GS} waveforms of the bottom MOSFET are then measured with single-ended passive probes. Testing cross-talk on a low-side switch is to avoid the use of *dv*/*dt*-sensitive differential probes, which will be otherwise used on the high-side switch in a regular double-pulse test setup, with the negative end of the probe connected to the switching node [13]. Considering the symmetric layout of the PEBB, the obtained results in this test will also apply to the high-side MOSFET in the phase-leg.

Figure 4-11 (b) shows the test waveforms of the bottom MOSFET under 600 V, 4 A, with $R_{G(on)}$ being only 2.0 Ω. As seen, when the top switch turns on, a positive *dv*/*dt* of around 10.4 V/ns is applied on the bottom MOSFET, and voltage spikes can be observed in the V_{GS} waveform. Thanks to the Miller clamp circuit, the V_{GS} spikes are successfully clamped below 0 V. In comparison, the red dashed waveform in the same figure shows

the condition where the Miller clamp is disabled and the shunt transistor is removed. In this case, the induced Miller current has to go through $R_{G(off)}$, which is also 2.0 Ω in this design, causing a peak voltage of about 1 V in V_{GS}. This is already very close to $V_{GS(th)}$ of the MOSFET, and is unsafe if the device is running at elevated temperatures. To leave enough margin for the cross-talk suppression, the turn-on speed is not pushed further, so $R_{G(on)}$ = 2.0 Ω is the final value used in the phase-leg.

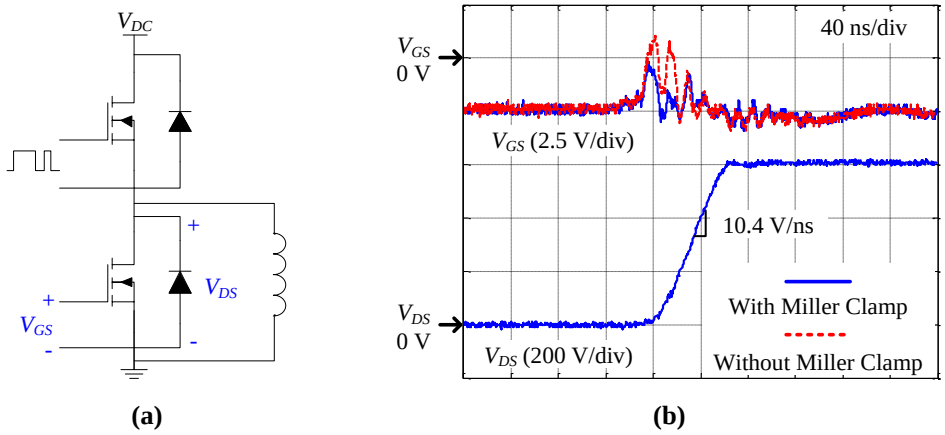


Figure 4-11. Cross-talk test of the phase-leg

(a) Test circuit schematic, (b) test waveforms with and without Miller clamp circuit

(3) Switching performance evaluations

While the turn-on speed is constrained by the cross-talk effect, the turn-off speed of the MOSFET is limited by its over-voltage and ringing during the transient, which are largely affected by the layout of the power stage. To show the improvement of the proposed layout design in reducing the switching loop inductance, both measurement and simulation are carried out on the PCB to compare the new layout with the conventional design. Figure 4-12 (a) shows the improved layout in this design, while in (b) the power switches are rearranged in the software to produce a conventional layout. The two

designs are then simulated in Ansoft Quick 3D Extractor (Q3D) to extract the switching loop inductances [14]. The actual PCB in Figure 4-9 is also measured with Agilent 4294A impedance analyzer. All results are compared in Figure 4-12 (c). As seen, the simulated loop inductance is very close to the measurement for the proposed layout, which shows a reduction of over 40% compared to the conventional layout.

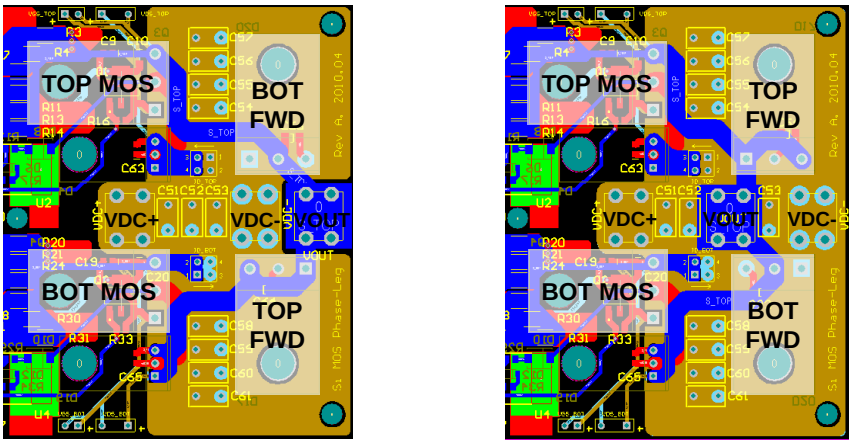


Figure 4-12. Comparison of power stage layouts. (a) Improved layout, (b) regular layout, (c) measured and simulated loop inductances involving the bottom MOSFET

The switching performances of the PEBB are then characterized with the double-pulse test. Thanks to the improved layout, the turn-off gate resistance $R_{G(off)}$ can also be reduced to only 2.0 Ω without introducing excessive parasitic ringing. Figure 4-13 shows the switching waveforms at 600 V and 10 A. It can be seen that the V_{DS} overshoot is controlled to be only 30 V at turn-off. The experiment also shows that, with $R_{G(off)}$ = 2.0 Ω, the turn-off speed has already reached the limit, as V_{GS} has hit the threshold before I_D completely falls to zero. The subsequent turn-off process is then only determined by the charging/discharging speeds of the devices' junction capacitances, and cannot be pushed faster by further reducing $R_{G(off)}$.

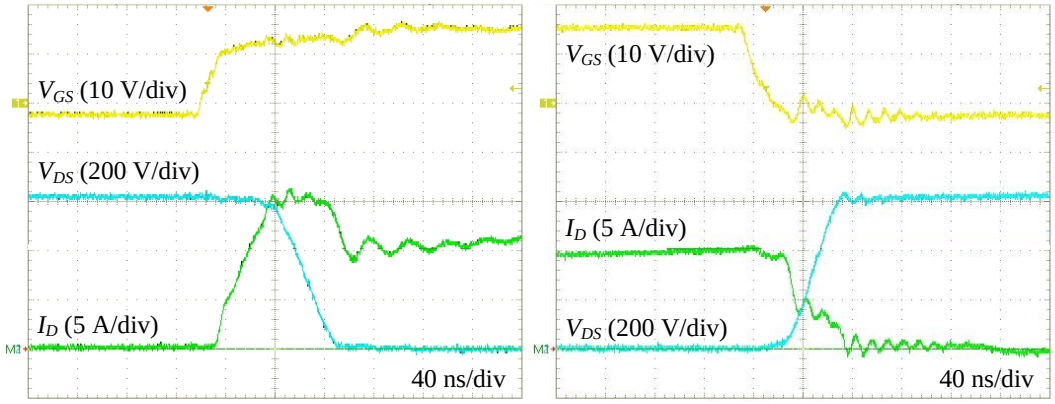


Figure 4-13. Switching waveforms of the SiC PEBB at 600 V and 10 A ($R_{G(on)}$ = $R_{G(off)}$ = 2.0 Ω) (left) Turn-on, (right) turn-off

The switching energies are plotted against the load current in Figure 4-14. The turn-on energy E_{on} of the SiC MOSFET increases almost linearly with the load, while in contrast the turn-off energy E_{off} has a much slower increasing rate, since the turn-off speed becomes faster under higher load [15]. Note that it is possible to achieve even lower switching energies with 20 V gate voltage instead of 15 V, which is shown as the

red dashed curves in the figure, estimated from simulation. In this case, E_{on} can be reduced a lot under higher load currents, but E_{off} will not be affected.

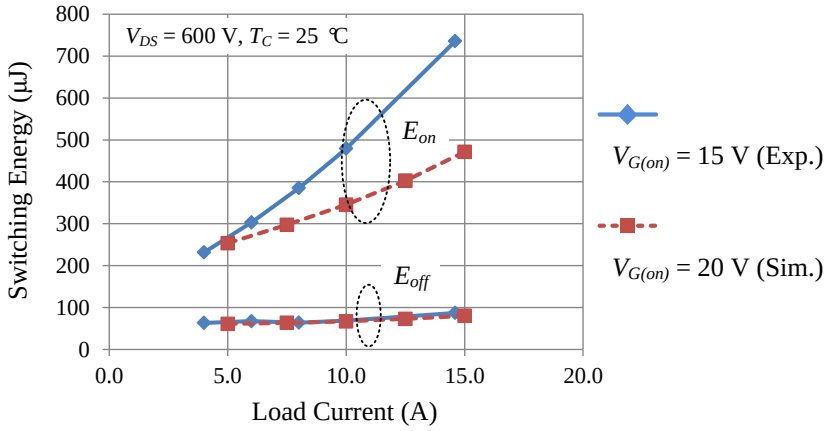


Figure 4-14. Switching energies versus load current

4.3 Design of the Phase-Leg PEBB Based on Si CoolMOS

The Si version of the PEBB utilizes the same PCB board, keeping the control scheme, the gate drive circuit, as well as the power stage layout essentially unchanged. The selected main switch is a 600 V, 46 A Si CoolMOS (APT47N60BCF) from Microsemi. A 600 V, 20 A SiC Schottky diode (C3D20060D) from Cree is chosen as the freewheeling diode. Since the body diode of the Si MOSFET has a lower forward voltage than that of the SiC diode, a 30 V, 60 A Si Schottky diode (62CTQ030PbF) is connected in series with the MOSFET to block the body diode and avoid its reverse recovery effect, as shown in Figure 4-8. The blocking diode selection considers the low voltage drop of the Schottky diode which minimizes its conduction loss, the current compatibility with the main switch, and the low blocking voltage which influences the zero-voltage-switching (ZVS) of the MOSFET.

4.3.1 Influence of the Blocking Diode on the ZVS Operation

In high-frequency converters, the MOSFETs are usually operated in the ZVS mode to eliminate their turn-on losses. This is essentially realized by conducting the anti-parallel diode first before turning on the MOSFET, which creates a zero-voltage condition for the switch. However, with the existence of the blocking diode, V_{DS} of the MOSFET will not be clamped to zero when the anti-parallel diode starts conducting. This phenomenon is illustrated in Figure 4-15.

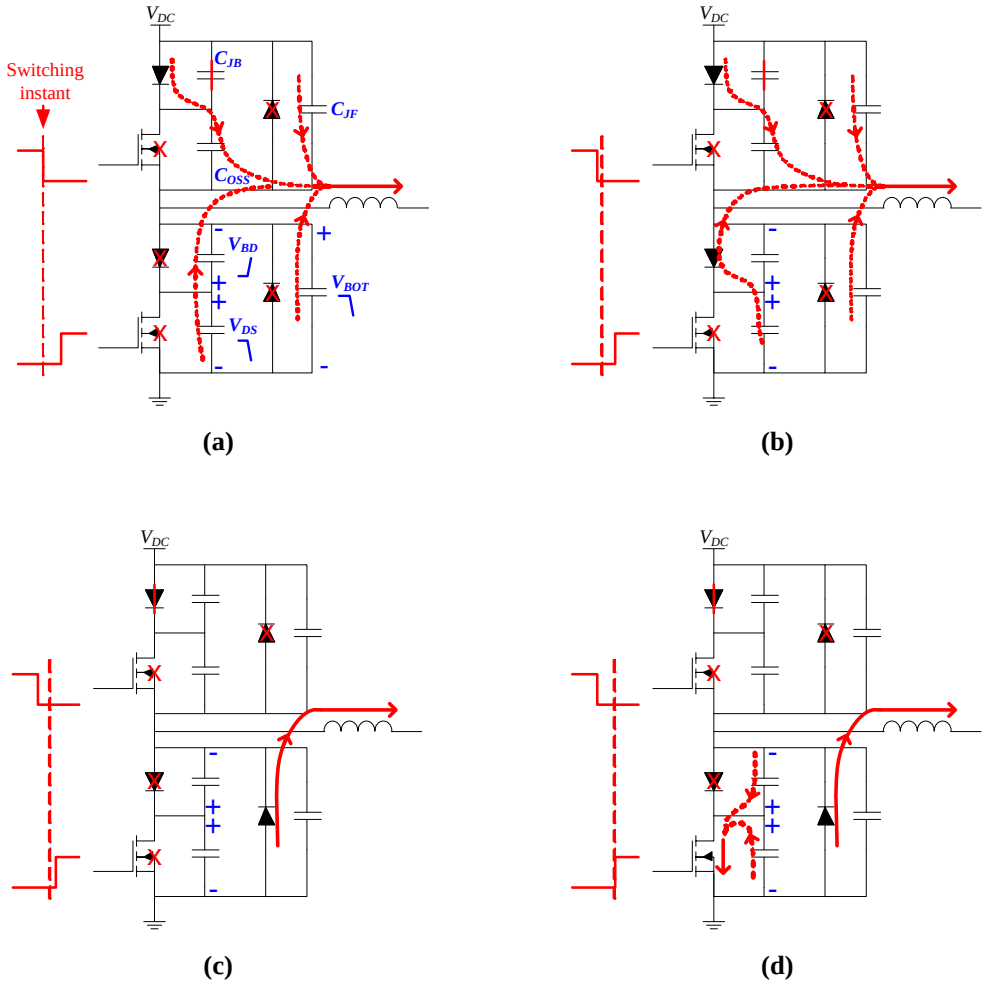


Figure 4-15. Influence of the blocking diode on the ZVS operation

In the figure, the capacitors are the MOSFET output capacitance C_{OSS}, the blocking diode capacitance C_{JB}, and the freewheeling diode capacitance C_{JF}. Assume that the original load current is flowing out of the switching node, as shown in Figure 4-15 (a), the top MOSFET is in the on-state, and the bottom is off. At the turn-off instant of the top MOSFET, the load inductor starts to draw currents from the junction capacitances of both the top and bottom devices. During this interval, the bottom C_{OSS} starts to discharge through C_{JB} of its blocking diode. V_{DS} and the overall V_{BOT} start to decrease while V_{BD} builds up. When V_{BD} reaches the breakdown voltage of the diode, the discharging current is diverted to flow through the diode reversely, and V_{BD} stays at the breakdown voltage, as Figure 4-15 (b) suggests. Meanwhile, V_{BOT} keeps decreasing until the bottom freewheeling diode becomes forward-biased, i.e. the moment when ZVS occurs. However, because of the blocking diode, there is a residual voltage on V_{DS} which is $\leq V_{BD}$, as seen in Figure 4-15 (c). When the bottom MOSFET is turned on, the remaining charge stored in C_{OSS} and C_{JB} will then be dissipated through the MOSFET channel, generating an extra amount of turn-on loss, as illustrated in Figure 4-15 (d).

Note that the interval of Figure 4-15 (b) is not a necessary step. The final residual voltage on V_{DS} (or equivalently, V_{BD}) is determined by the ratio of C_{JB} and C_{OSS}, or the charges stored in these two capacitors. If the freewheeling diode starts conducting before the blocking diode breaks-down, then V_{DS} will be smaller than the breakdown voltage.

The above analysis is verified through a double-pulse test of the PEBB, as illustrated in Figure 4-16. The experimental waveforms in Figure 4-16 (b) clearly show the residual voltage on the MOSFET when the freewheeling diode conducts. For the

selected devices in this design, this residual voltage is around 25 V, less than the breakdown voltage of the blocking diode.

The possibility of breaking-down the blocking diode requires that its junction capacitance should not be too small to incur any destructive reverse current. If necessary, an external capacitance can be paralleled to the blocking diode to reduce the residual voltage. Figure 4-16 (c) shows the test waveforms with 20 nF capacitance paralleled to the diode, where the residual voltage on the MOSFET is accordingly reduced to 10 V.

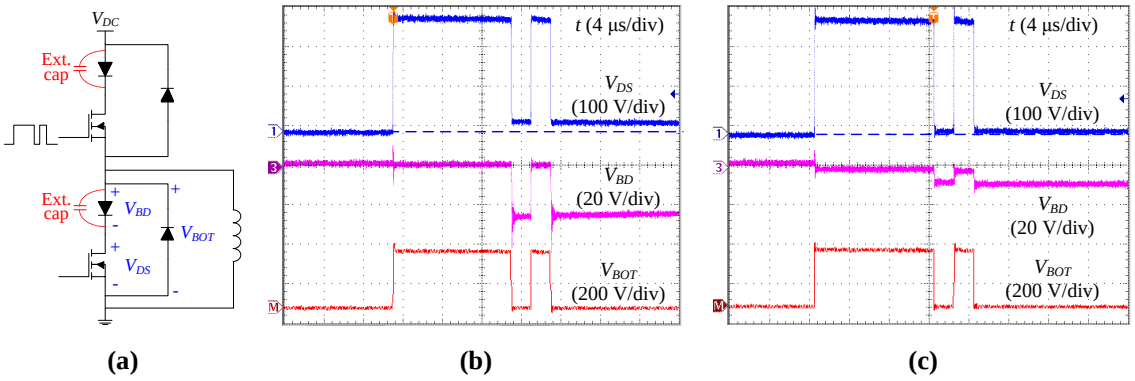


Figure 4-16. Experimental waveforms showing the influence of the blocking diode on ZVS operation (a) Test circuit, (b) waveforms without external capacitance, (c) waveforms with 20 nF capacitance

Both the experiment and simulation show that the external capacitance can help reduce E_{on} and E_{off} of the MOSFET under ZVS operation without affecting the switching speed of the PEBB. This is because the MOSFET and the blocking diode are connected in series, and therefore the equivalent capacitance of this branch will be dominated by the MOSFET C_{OSS}. Enlarging the diode capacitance will thus have very little effect on this equivalent capacitance.

Since the blocking diode does not breakdown in the Si PEBB, no external capacitance is used in this work.

4.3.2 Switching Performance Evaluations

The switching performances of the Si PEBB are characterized in the same way as the SiC PEBB. For the Si version, the DC bus voltage is kept at 300 V. The gate resistances are finely tuned based on the cross-talk effect at turn-on and the V_{DS} overshoot at turn-off. Finally, $R_{G(on)}$ = 5.0 Ω and $R_{G(off)}$ = 2.0 Ω are chosen. Figure 4-17 shows the typical switching waveforms at 300 V and 12.5 A, and Figure 4-18 plots the switching energies against the load current at room temperature.

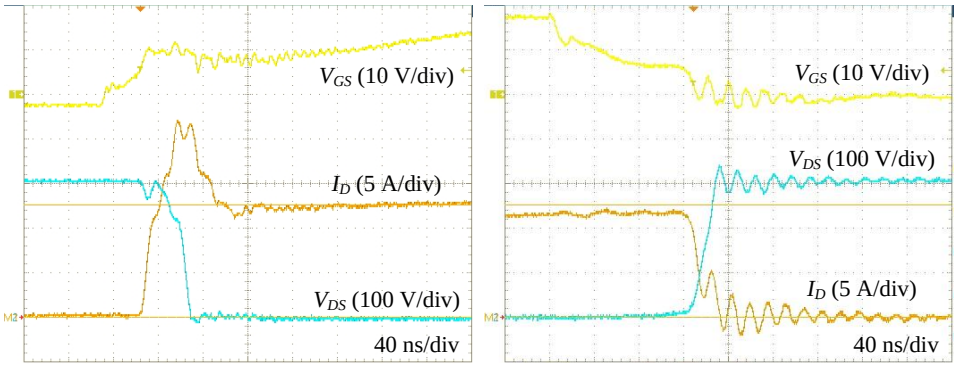


Figure 4-17. Switching waveforms of the Si PEBB at 300 V and 12.5 A ($R_{G(on)}$ = 5.0 Ω, $R_{G(off)}$ = 2.0 Ω) (left) Turn-on, (right) turn-off

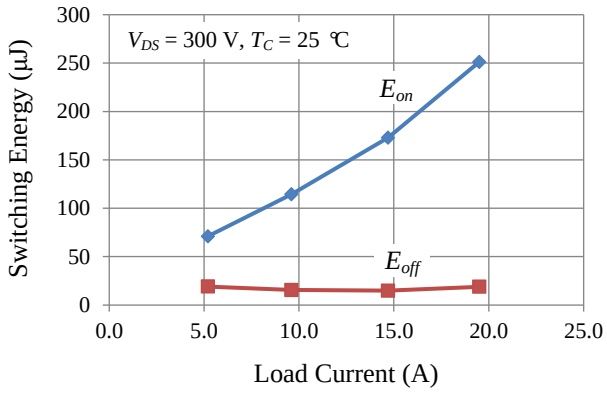


Figure 4-18. Switching energies versus load current for the Si PEBB

4.4 Behavioral Comparison of Si and SiC Power MOSFETs for High-Frequency Applications

In this section, the aforementioned two types of MOSFETs are compared in order to understand how the new SiC devices are different from their Si counterparts. The comparison will firstly be conducted in the static and switching characteristics of the two MOSFETs, and how they are differently influenced by the temperature. The experimental data of the two PEBBs developed above will then be used to calculate and compare the device loss distributions in a high-frequency DC-DC converter. Table 4-1 summarizes the power devices and gate drive parameters used for the Si and SiC PEBBs.

Table 4-1. Summary of Si and SiC PEBBs

	Si PEBB	SiC PEBB
Main switch	Si CoolMOS Microsemi APT47N60BCF 600 V, 46 A	SiC DMOSFET Cree CMF20120D 1200 V, 20 A
Freewheeling diode	SiC Schottky diode Cree C3D20060D 600 V, 20 A	SiC Schottky diode Cree C2D10120D 1200 V, 10 A
Blocking diode	Si Schottky diode Vishay 62CTQ030PbF 30 V, 60 A	None
Gate voltages	+15 V/-2.5 V	+15 V/-2.5 V
Gate resistances	$R_{G(on)}$ = 5.0 Ω, $R_{G(off)}$ = 2.0 Ω	$R_{G(on)}$ = 2.0 Ω, $R_{G(off)}$ = 2.0 Ω

4.4.1 Comparison of Static Characteristics

(1) Output characteristics

Compared to Si CoolMOS, the SiC MOSFET has a much wider quasi-linear region in its output characteristics, and the slope of the *I-V* curve keeps increasing all the way as V_{GS} approaches 20 V, as shown in Figure 4-19. This is quite different from Si whose knee

points between linear and saturation regions are clear, and the linear region slopes are almost overlapped when V_{GS} is greater than 10 V. The difference is mainly due to the smaller transconductance of the SiC MOSFET, which requires that the device must be driven at the full V_{GS} of 20 V in order to achieve the rated $R_{DS(on)}$ [16].

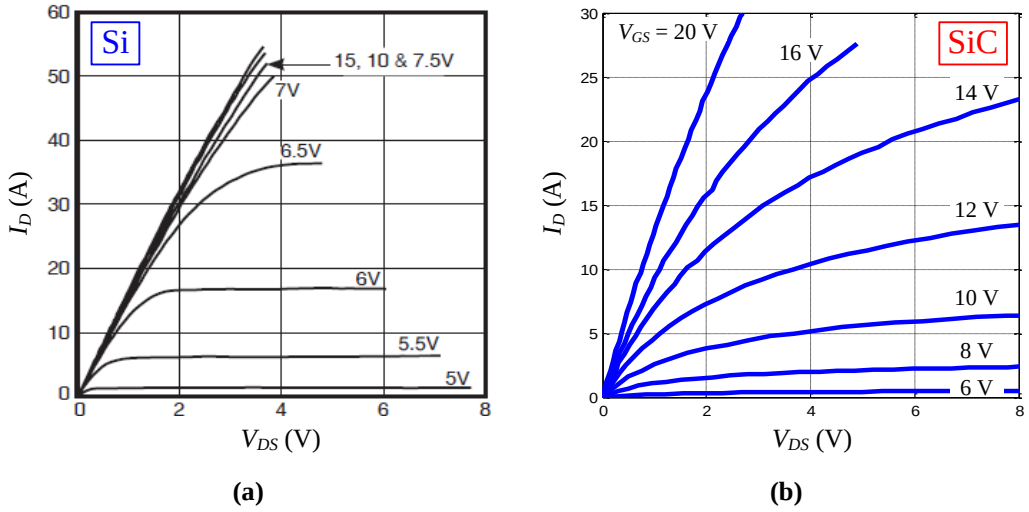


Figure 4-19. Comparison of output characteristics. (a) Si CoolMOS, (b) SiC DMOSFET

(2) On-state resistance

The influence of the gate voltage on the MOSFET's on-state resistance is clearly shown in Figure 4-20. For the Si MOSFET, its $R_{DS(on)}$ keeps almost unchanged as long as V_{GS} > 10 V. Driving the Si device with a higher gate voltage will thus only increase its turn-on speed, but will not reduce the conduction loss. In comparison, $R_{DS(on)}$ of the SiC MOSFET will keep decreasing when V_{GS} increases from 16 V to 20 V. Therefore, a higher gate voltage is beneficial for the SiC MOSFET in both faster switching speed and lower conduction loss.

Temperature-wise, the SiC MOSFET exhibits slightly lower $R_{DS(on)}$ at 25 ℃ and V_{GS} = 20 V, which is already advantageous considering its 2x voltage and 0.5x current

ratings. Moreover, its $R_{DS(on)}$ increases at a much slower rate as the temperature rises, thanks to its channel resistance of negative temperature coefficient. Being less temperature-sensitive in $R_{DS(on)}$ is an especially favorable characteristic for the SiC MOSFET to work under higher junction temperatures than Si.

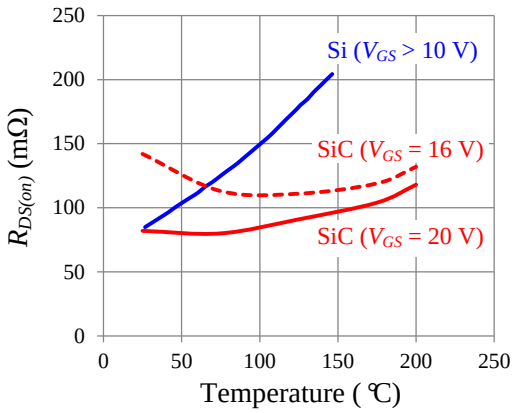


Figure 4-20. Comparison of on-state resistances

(3) Transfer characteristics

Figure 4-21 compares the transfer characteristics of the two MOSFETs. As seen, both devices have threshold voltages decreasing at higher temperatures. The comparison of more accurate $V_{GS(th)}$ is shown in Figure 4-22, where the SiC MOSFET exhibits lower values by approximately 1 V. The lower $V_{GS(th)}$ requires the SiC device to be turned off with a negative bias to increase its threshold margin, especially at high temperatures. This negative bias is again limited by the maximum allowable gate voltage of -5 V for the SiC MOSFET, which poses more challenges in the gate driver design. Such a constraint usually does not exist for the Si MOSFET, whose gate oxide layer can block up to ±30 V according to the datasheet.

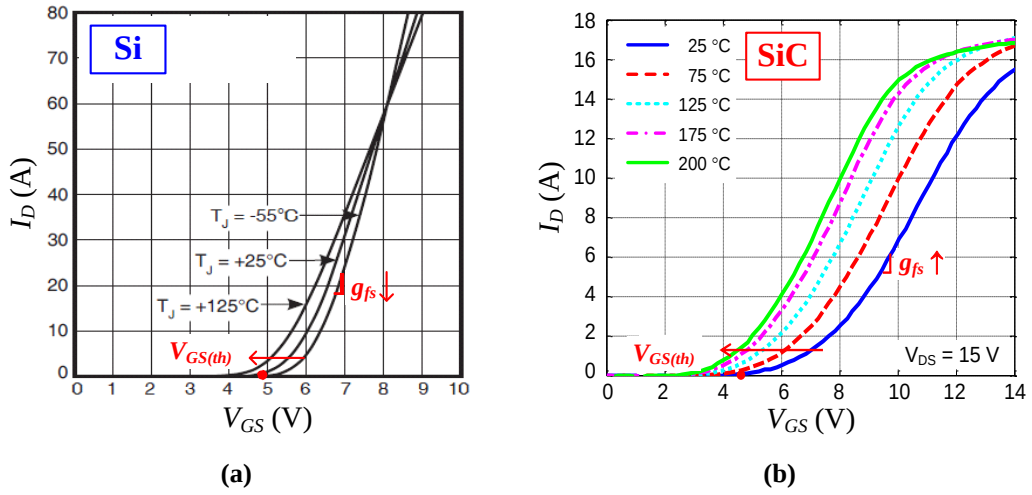


Figure 4-21. Comparison of transfer characteristics. (a) Si CoolMOS, (b) SiC DMOSFET

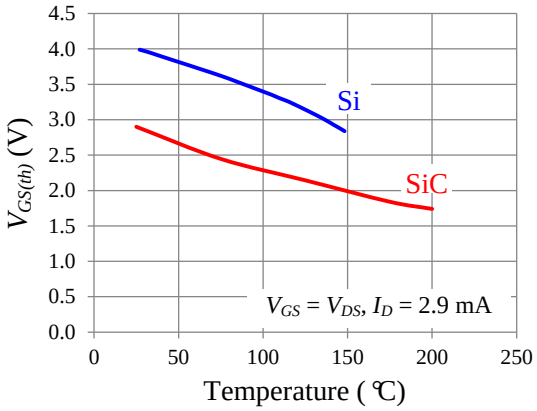


Figure 4-22. Comparison of threshold voltages

It is also important to note the smaller transconductance g_{fs} of the SiC MOSFET. What is even more special for SiC is that its g_{fs} slightly increases with the temperature, showing just the opposite trend to Si, as illustrated in Figure 4-23. This special characteristic will cause the SiC MOSFET to show different switching behaviors at high temperatures.

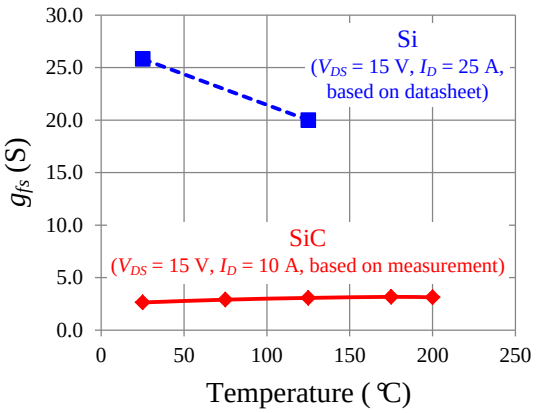


Figure 4-23. Comparison of transconductances

4.4.2 Comparison of Switching Characteristics

The MOSFET's switching waveforms are strongly affected by its junction capacitances. Comparing to Si, the SiC MOSFET features smaller C_{ISS}, but comparable C_{OSS} and C_{RSS}, as shown in Figure 4-24. As a result, the total gate charge Q_G of the SiC device is only 1/4 of that of the Si, which would greatly reduce the power consumption of the gate drive power supplies based on Eq. (4-9). Smaller C_{ISS} also helps shorten the switching delays according to the MOSFET switching theory [17], which is good for reducing the dead time in phase-leg operations. Figure 4-25 (a) compares the turn-on and turn-off delays of the Si and SiC PEBBs, where significant shorter turn-off delay time can be observed for the SiC MOSFET. Consequently, the SiC phase-leg would require a shorter dead time to avoid the potential shoot-through problem, as shown in Figure 4-25 (b). Note that in this figure, the minimum dead time is defined as

$$t_{DeadTime(\min)} = t_{off} - t_{d(on)}, \tag{4-10}$$

where t_{off} is the total turn-off time, and $t_{d(on)}$ is the turn-on delay time. The definitions of the switching times can be found in [18].

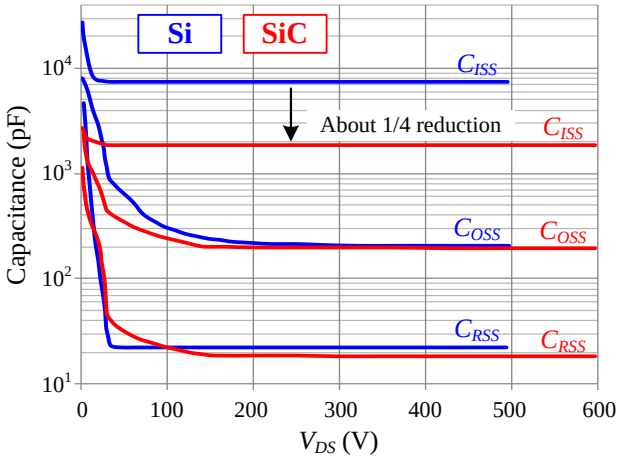


Figure 4-24. Comparison of junction capacitances

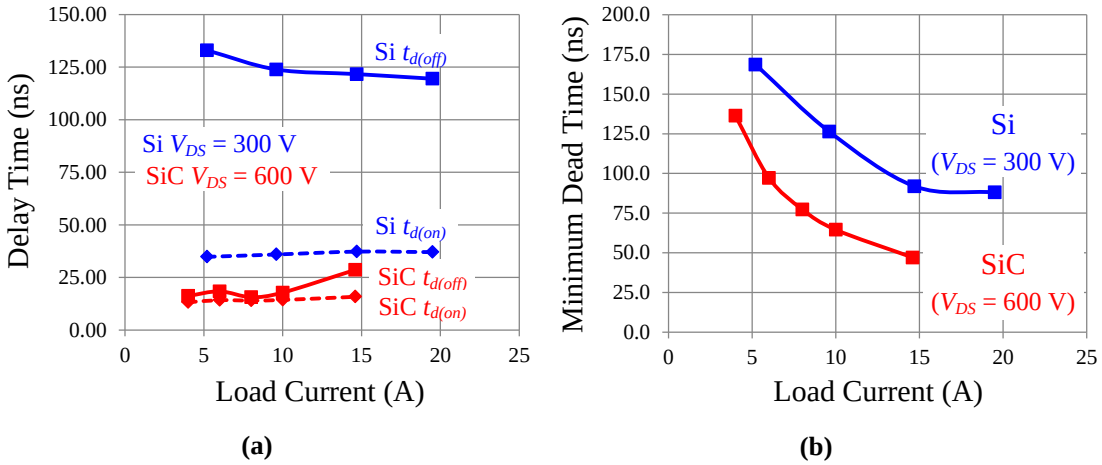
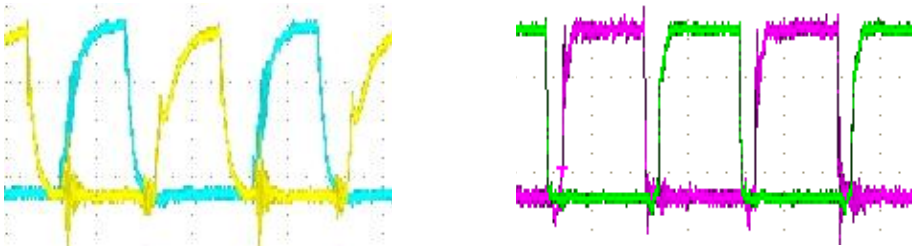


Figure 4-25. Comparison of switching delay times (a) and minimum dead times (b)

As displayed in Figure 4-26, the smaller C_{ISS} also results in a smaller time constant within the gate loop of the SiC MOSFET, leading to much faster response of its V_{GS} waveform. Roughly speaking, the time constant of the SiC PEBB at turn-on ($R_{G(on)}C_{ISS}$) is only 1/10 of that of the Si PEBB. From the gate drive point of view, this is favorable to the high-frequency operation of SiC MOSFETs. However, this does not directly lead to faster switching speed and smaller switching loss for these devices.



(a) **(b)**

Figure 4-26. Comparison of V_{GS} waveforms at 500 kHz. (a) Si CoolMOS, (b) SiC DMOSFET

In Figure 4-24, the SiC MOSFET exhibits only slightly lower C_{OSS} and C_{RSS}. Since these two capacitances are more closely related to the dv/dt of the device than C_{ISS} [17], this implies that the SiC MOSFET may not be significantly faster than Si. As a matter of fact, the SiC switch even shows higher switching loss than its Si counterpart, as illustrated in Figure 4-27. In this figure, the experimental switching energies of the two PEBBs are plotted against the apparent switching power (i.e. $V_{DS}{\cdot}I_D$) to eliminate the difference in the bus voltage. As seen, even with much smaller gate loop time constant, the SiC MOSFET still exhibits roughly two times higher switching energies for both E_{on} and E_{off} at the same apparent power as the Si MOSFET.

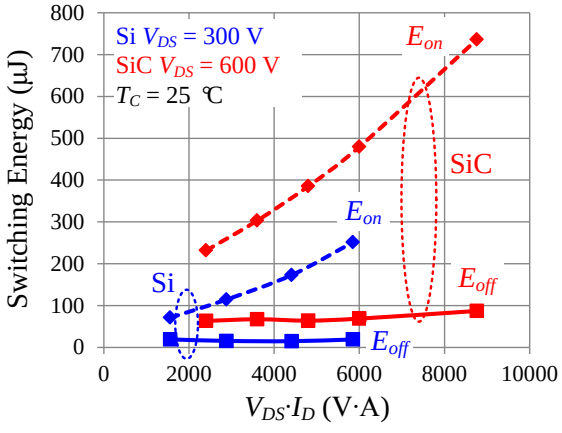
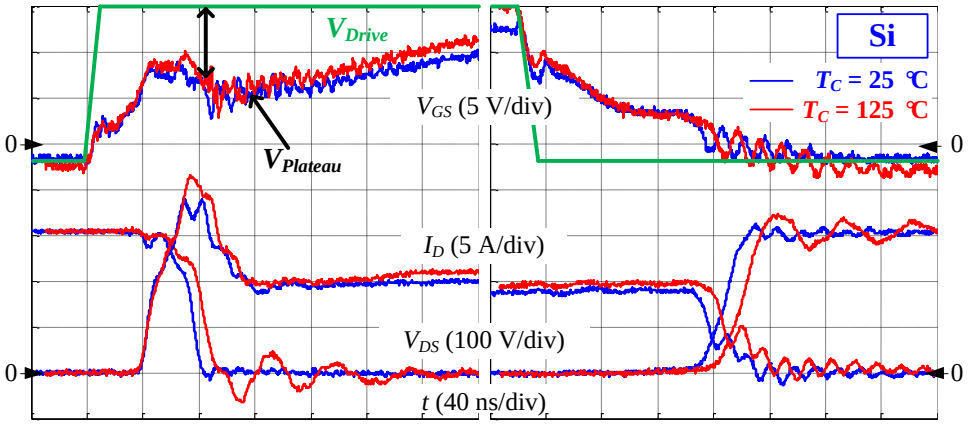


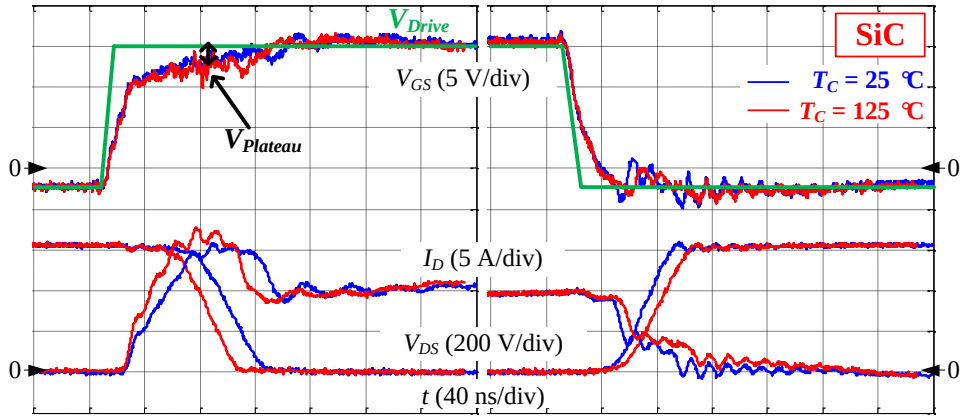
Figure 4-27. Comparison of switching energies

The higher switching loss of the SiC MOSFET can be attributed to its smaller transconductance g_{fs}. The effect of this parameter can be clearly seen if comparing the switching waveforms of the two PEBBs side-by-side, as shown in Figure 4-28. As previously mentioned in Chapter 2, g_{fs} affects the plateau voltage $V_{Plateau}$ in the V_{GS} waveform through Eq. (2-2), with a smaller g_{fs} resulting in a higher $V_{Plateau}$. This is obviously seen in Figure 4-28: When turning on the same load current of 10 A, the SiC MOSFET has the plateau level around 13 V, while for the Si, the plateau is just slightly over 5 V. Higher $V_{Plateau}$ will thus significantly limit the driving current that flows to discharge the Miller capacitance according to Eq. (2-3), and eventually limit the dv/dt of the switch. Therefore, even though the SiC MOSFET is turned on with a much lower time constant $R_{G(on)}C_{ISS}$, and its C_{RSS} is slightly smaller, the dv/dt of the device is still very close to that of the Si CoolMOS, as illustrated in Figure 4-29.

The opposite temperature dependences of g_{fs} of the Si and SiC MOSFETs also change their switching speeds in different directions at elevated temperatures. The switching waveforms at 25 and 125 ℃ of the two PEBBs are also compared in Figure 4-28, and the reason to such changes has been explained in Chapter 2. As a result, the Si phase-leg will have higher E_{on} and E_{off}, and therefore higher total switching loss E_{tot}, when operated at elevated temperatures, as seen in Figure 4-30 (a). For the SiC PEBB, nevertheless, the reduction in E_{on} cancels the increase in E_{off}, thus keeping E_{tot} almost unchanged at different temperatures, as seen in Figure 4-30 (b). This is another favorable feature for the SiC MOSFET to work at higher junction temperatures.



(a)



(b)

Figure 4-28. Comparison of switching waveforms
(a) Si CoolMOS at 300 V, 10 A, (b) SiC DMOSFET at 600 V, 10 A

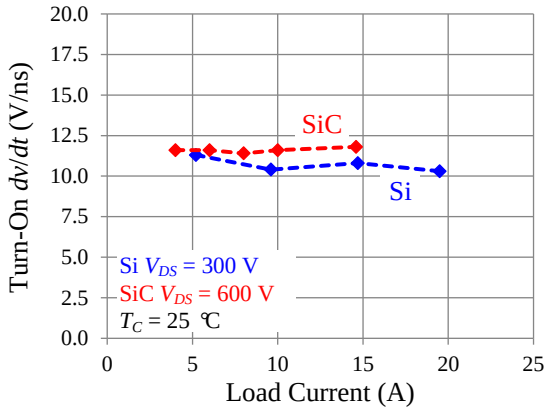


Figure 4-29. Comparison of turn-on *dv/dt*

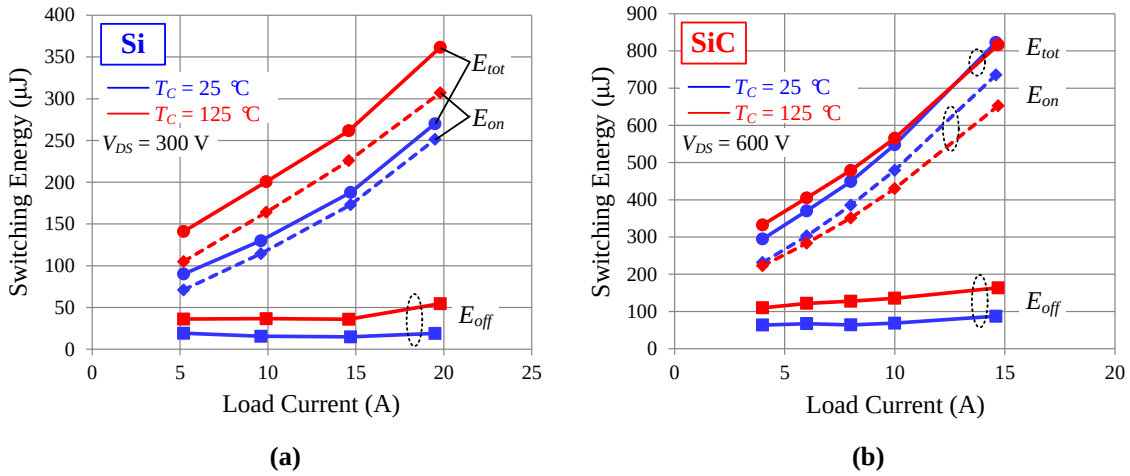


Figure 4-30. Comparison of switching energies influenced by the temperature (a) Si CoolMOS, (b) SiC DMOSFET

4.4.3 Comparison of Device Losses in a High-Frequency DC-DC Converter

In this section, the experimental data of the Si and SiC PEBBs presented above are used to calculate the device loss distributions in a high-frequency DC-DC converter, in order to study how their respective conduction and switching losses affect the overall performance of the system. The isolated dual-active-bridge (DAB) converter is selected in this work to perform the comparison, whose topology is shown in Figure 4-31.

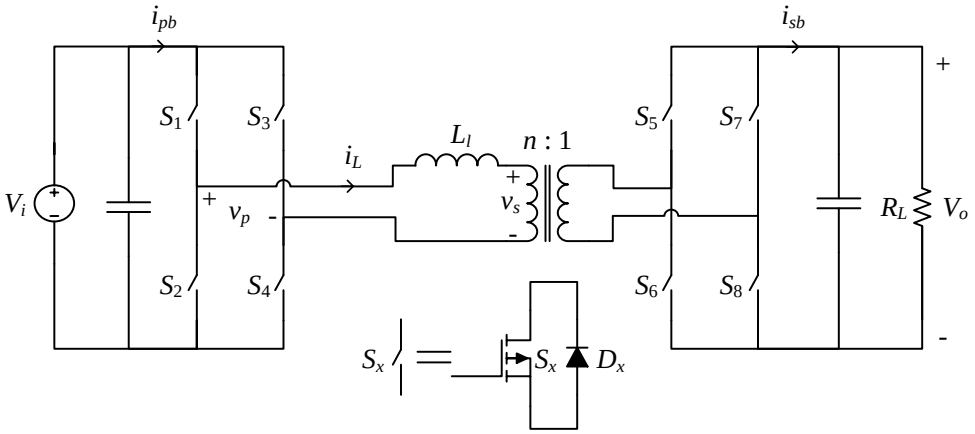


Figure 4-31. Isolated dual-active-bridge converter

Featuring many advantages such as bidirectional power flow, electrical isolation, and soft switching for the switches of both sides, etc., the DAB topology is a promising solution for solid-state transformer and energy storage applications [19]-[23]. Nowadays, there exists a trend towards the high-frequency operation of DAB in order to achieve higher power density. Towards this goal, the semiconductor device losses compose a critical part in the ultimate efficiency of the converter.

Table 4-2 compares the main static parameters of the candidate Si and SiC power transistors for the DAB application. In the first two rows are the devices used for the PEBBs in this work. While in the last two, the state-of-the-art Si MOSFET and Si IGBT with 1200 V blocking voltage are shown. For fair comparison, all 1200 V devices have similar current ratings at the room temperature. As previously mentioned, the high-voltage Si MOSFET suffers from significantly higher $R_{DS(on)}$ and hence higher conduction loss, which directly rules it out from the candidates, not to mention its switching performance. On the other hand, the Si IGBT shows fairly good forward voltages, but its slower switching speed, which has been presented by many researchers, would lead to much higher switching loss under high-frequency operations than SiC MOSFETs [5]-[7][16]. The performances of the 600 V Si CoolMOS and the 1200 V SiC MOSFET are not so easy to tell from the table, and thus will be compared in detail in this section.

Table 4-2. Comparison of Si and SiC Power Transistors

Device	Technology	Voltage rating (V)	Current rating at 25 ℃ (A)	$R_{DS(on)}$ (mΩ)		V_{on} at 20 A (V)	
				25 ℃	125 ℃	25 ℃	125 ℃
Microsemi APT47N60BCF	Si MOSFET	600	46	83	179	1.66	3.59
Cree CMF20120D	SiC MOSFET	1200	33	80	95	1.60	1.90
Microsemi APT28M120L	Si MOSFET	1200	29	450	1098	9.00	21.96
Infineon IGW15N120H3	Si IGBT	1200	30	N/A	N/A	2.37	2.93

The comparison firstly assumes that the converter has the same phase-leg PEBBs on both sides of the transformer. Therefore, the Si and SiC DABs are assumed to operate under different DC bus voltages, but transfer the same amount of power. The main system specifications are summarized in Table 4-3. For simplicity, it is also assumed that the basic phase-shift modulation is used [24], and the nominal output power of both DABs is achieved at the same phase-shift angle of 45 º. Under such assumptions, the voltage and current waveforms of the two converters will be alike in shape, but only differ by two times in amplitude (i.e. the SiC DAB will have twice the voltage but half the current compared to the Si version). Note that the leakage inductances L_l in the two converters are also different for the above assumptions to hold. The device losses are then calculated based on the DAB lossless model [24], and the calculations are repeated at three different switching frequencies of 100, 250, and 500 kHz.

Table 4-3. System Specifications of the DABs in Comparison

Nominal output power P_o (W)	5×10^3
Input DC voltage V_i (V)	Si DAB: 300 V ± 10% SiC DAB: 600 V ± 10%
Output DC voltage V_o (V)	Si DAB: 300 V SiC DAB: 600 V
Switching frequency f_{sw} (kHz)	100, 250, and 500
Transformer turns-ratio n : 1	1.1 : 1
Leakage inductance L_l	Given by: $\frac{nV_iV_o\theta(\pi-\theta)}{2\pi^2 f_{sw}P_o}$
Modulation method	Phase-shift modulation
Phase-shift angle θ at nominal P_o	45 º

The semiconductor switches and the transformer are all considered ideal in the lossless model. Figure 4-32 shows the typical waveforms of the lossless DAB with the phase-shift modulation. As seen, both the primary- and secondary-side H-bridges are modulated by complementary gating signals with 50% duty cycle. The gating signals between the two sides, however, are phase-shifted by an angle of θ. The resultant voltage difference on the transformer then shapes the leakage inductor current i_L, which achieves the power transfer and creates the ZVS condition for the switches of both sides. Detailed operation principles of the converter can be found in [24].

With the phase-shift modulation, the DAB will lose ZVS operation at light load, so ZVS boundaries exist for both the primary- and secondary-side switches. The derivations of these boundaries are documented in [25][26], and the results for this specific example are shown in Figure 4-33. In the figure, the *x*-axis represents the output power, and the *y*-axis represents the "voltage gain" *d* of the converter, which is defined by

$$d = \frac{n \cdot V_o}{V_i}. \tag{4-11}$$

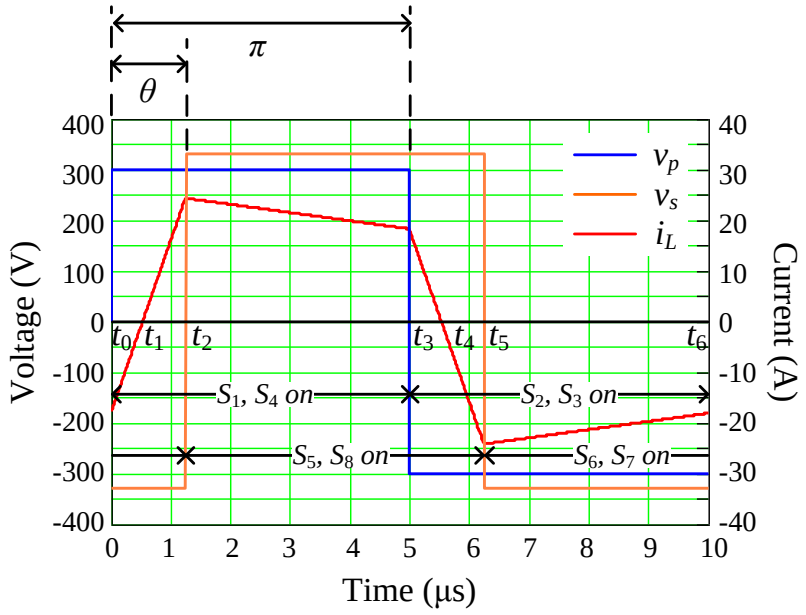


Figure 4-32. Ideal waveforms of DAB with phase-shift modulation

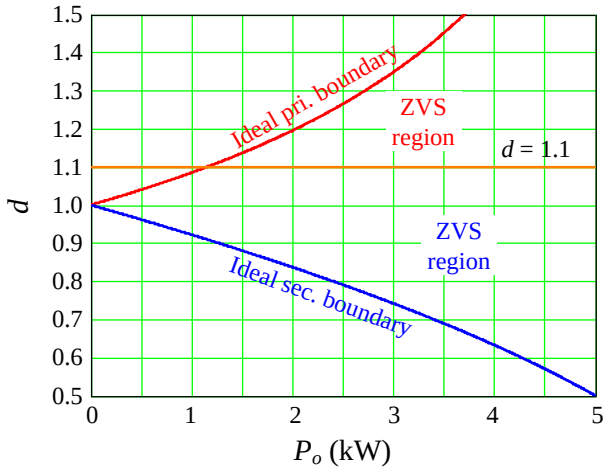


Figure 4-33. ZVS boundaries of DAB

It is easy to see that for the studied DABs in this work, d = 1.1. According to Figure 4-33, ideally the primary-side switches will lose ZVS at about 20% of the nominal output power, while the secondary side can keep ZVS operation over the entire load range. If further considering the effect of device junction capacitances, the primary-side boundary will shift slightly to the higher load, and there will also be a neighborhood of the

boundary where the switches are partially soft-switched. To simplify the analysis, this work will only consider the output range from half to full load, where switches of both sides are fully soft-switched.

The waveform of the leakage inductor current needs to be determined to calculate the device losses. Due to the symmetry of the waveform, only the first half of the switching cycle is calculated.

$$i_L(t) = \begin{cases} i_L(t_0) + \dfrac{V_i + nV_o}{L_l} \cdot (t - t_0), \text{for } t_0 \le t < t_2 \\ i_L(t_2) + \dfrac{V_i - nV_o}{L_l} \cdot (t - t_2), \text{for } t_2 \le t < t_3 \end{cases}, \tag{4-12}$$

where

$$i_L(t_0) = \frac{\pi(nV_o - V_i) - 2\theta nV_o}{4\pi f_{sw} L_l}, \tag{4-13}$$

$$i_L(t_2) = i_L(t_0) + \frac{V_i + nV_o}{L_l} \cdot \frac{\theta}{2\pi f_{sw}}, \tag{4-14}$$

$$t_2 = \frac{\theta}{2\pi f_{sw}} + t_0, \tag{4-15}$$

and

$$t_3 = \frac{\pi}{2\pi f_{sw}} + t_0. \tag{4-16}$$

For the second half of the switching cycle, the current is simply

$$i_L(t) = -i_L\left(t - \frac{1}{2 f_{sw}}\right), \text{for } t_3 \le t < t_6. \tag{4-17}$$

The i_L waveform is solely determined by Eq. (4-12) to (4-17). The transformer current on the secondary side is then given by $n \cdot i_L$.

The average and the RMS values of the device currents can be easily obtained from $i_L(t)$. Note that i_L will have different paths in the two DABs. For the Si version, because of the blocking diodes, the reverse current (e.g. during $[t_0, t_1]$ and $[t_4, t_5]$) will flow through the anti-parallel diodes. While for the SiC version, the reverse current will still flow through the MOSFET channel since it has lower voltage drop. The anti-parallel diodes of the SiC DAB will only conduct for a short period of time during the dead time, so their losses are neglected. Given these simplifications, the device losses are calculated as following:

For the MOSFET, the total loss is

$$P_{MOS} = I_{MOS(RMS)}{}^2 R_{DS(on)} + E_{off} f_{sw}. \tag{4-18}$$

Note that since ZVS is assumed, only E_{off} of the MOSFET is included.

For the diode (blocking and anti-parallel), the total loss is

$$P_D = I_{D(ave)} V_{FWD} + I_{D(RMS)}{}^2 R_{FWD}. \tag{4-19}$$

The device parameters used to calculate the losses are summarized in Table 4-4. Data at both 25 and 125 ℃ are available, so the losses will be evaluated at both temperatures.

Table 4-4. Device Parameters Used to Calculate the Losses

Diode	T_C (℃)	V_{FWD} (V)	R_{FWD} (mΩ)	MOSFET	T_C (℃)	$R_{DS(on)}$ (mΩ)	E_{off} * (μJ)
C3D20060D	25	0.87	28.7	APT47N60BCF	25	83	$0.0198i_D + 17.275$
	125	0.83	48.4		125	179	$1.1514i_D + 26.504$
62CTQ030PbF	25	0.34	3.7	CMF20120D	25	80	$2.1532i_D + 51.695$
	125	0.19	6.9		125	95	$4.8435i_D + 90.257$

* V_{DC} = 300 V for Si MOSFET, V_{DC} = 600 V for SiC MOSFET

Figure 4-34 shows the Si DAB's loss distribution among different devices of both sides under full load. Based on the calculation assumptions, the average and RMS currents will not change under various switching frequencies, so the conduction losses remain the same, while the MOSFET switching loss increases in proportion to the frequency. As seen from the figure, the switching loss of the Si DAB is a relatively smaller portion in the total device losses. At 100 kHz, it is less than 20% of the total losses. At 500 kHz and 125 ℃, it increases to be barely equal to the total conduction losses. The figure also indicates that the MOSFETs are the main contributor to the increasing losses at elevated temperatures, whose conduction and switching losses are seen to be roughly doubled when T_J rises from 25 to 125 ℃.

In contrast, the SiC DAB exhibits a completely different pattern in the loss distribution. Due to the simplifications explained above, only the SiC MOSFETs generate losses in this example, as illustrated in Figure 4-35. The figure clearly shows that the switching loss dominates the total MOSFET losses at all frequencies, and at 500 kHz this loss composes even as high as 90% of the total losses. One of the reasons for this result is that the SiC DAB operates under a higher bus voltage and thus carries a lower current to deliver the same power. This, when combined with the SiC MOSFET's small $R_{DS(on)}$, reduces the conduction loss significantly. On the other hand, as Figure 4-27 has shown, the SiC MOSFET does not exhibit faster switching speed than the Si CoolMOS. As a result, much higher switching loss can be observed for the SiC DAB. As the switching frequency increases, this single loss can even exceed the total device losses of the Si DAB – such as the 500 kHz case shown in the figure. In this sense, the higher bus voltage

with SiC devices is not necessarily favorable in reducing the total losses of the converter under very high switching frequencies.

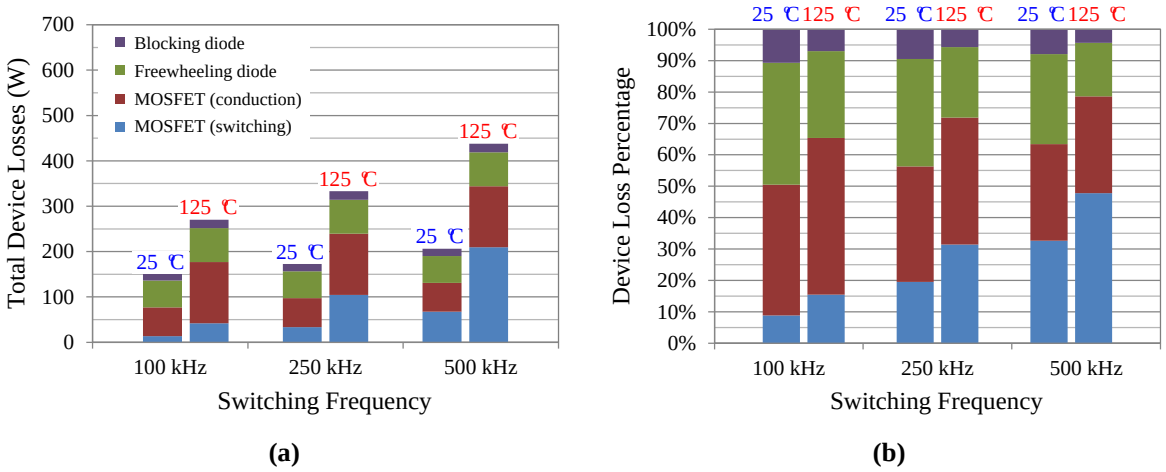


Figure 4-34. Device loss breakdown of the Si DAB at 5 kW and various switching frequencies
(a) Absolute losses, (b) relative losses in percentage

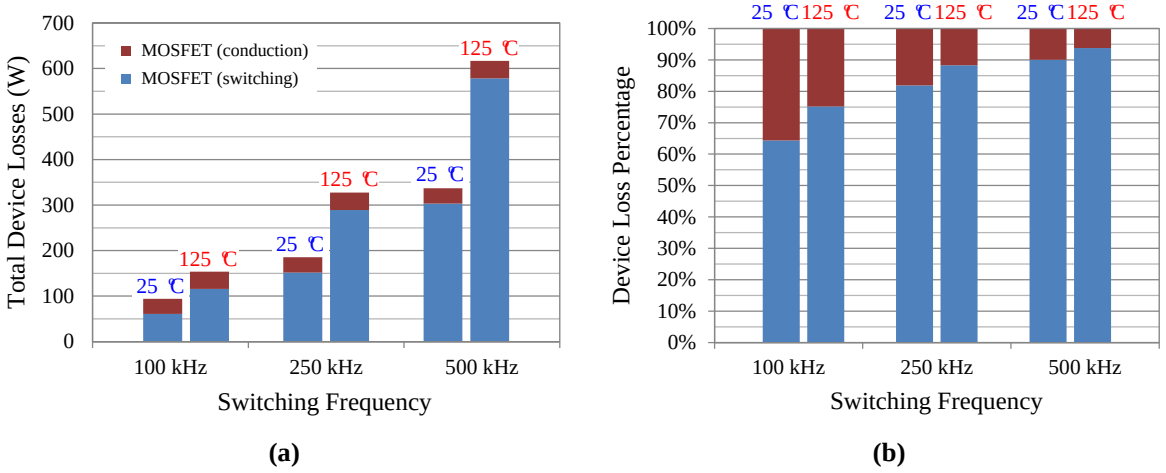


Figure 4-35. Device loss breakdown of the SiC DAB at 5 kW and various switching frequencies
(a) Absolute losses, (b) relative losses in percentage

The benefit of using the SiC MOSFET, though, is the stable conduction loss versus the temperature, thanks to its superior $R_{DS(on)}$ characteristic. As one can infer from Figure

4-35, as long as the switching frequency is reduced and the switching loss takes a lower percentage, the SiC DAB will generate less device losses than the Si one at the room temperature, and this advantage becomes even more obvious at 125 ℃.

Figure 4-36 compares the total device losses of the two DABs at 125 ℃, versus the output power from half to full load. Due to the switching-loss dominance of the SiC DAB, a significant amount of losses can be saved when the converter operates at lower frequencies. For the same reason, the loss curves of the SiC converter also exhibit less dependence on the load compared to the Si ones. So, when the switching frequency is decreased, to 100 kHz for example, smaller device losses can be observed for the SiC DAB than the Si above half load, and the difference becomes more prominent as the load increases. Note that only device losses are compared in this study. If further considering the design trade-offs in the other aspects of the converter, e.g. the losses from the transformer and the PCB traces, etc., one can infer that the SiC system will provide other benefits over its Si competitor to improve the total efficiency of the converter.

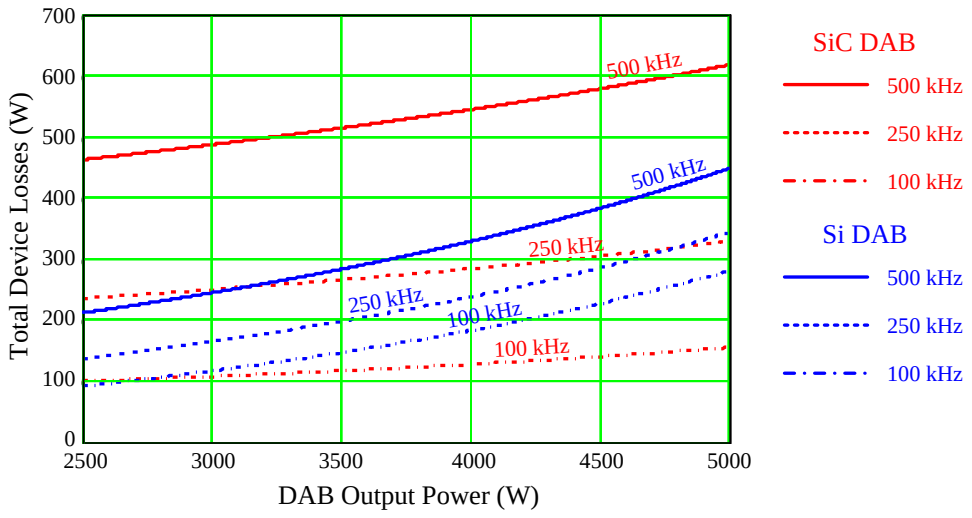


Figure 4-36. Total device losses at 125 ℃ versus the output power

4.5 Conclusions

This chapter firstly presents the design and analysis of discrete phase-leg PEBBs using 1200 V SiC MOSFET and 600 V Si CoolMOS. The work has been focused on the modularization of the phase-leg subsystem so that it can be utilized in various topologies. Technical issues such as the dead-time generation, gate driver, and power stage layout, etc., have been discussed in detail. Particularly, the design optimizes the high-frequency operation of the phase-leg by pushing the device switching speed through improved gate driver and PCB layout designs. The effectiveness of the Miller clamp circuit in minimizing the cross-talk effect, as well as the improved power stage layout in reducing the total loop inductance, has been verified through both simulation and experiments.

In the second part of the chapter, detailed comparisons between the Si and SiC power MOSFETs have been performed. The results have shown that the SiC device does behave differently than Si in many ways, and thus requires different design considerations. For instance, a higher driving voltage is recommended for the SiC MOSFET to achieve lower $R_{DS(on)}$ and faster switching speed, and cares need to be taken to avoid the Miller-effect-induced false triggering owing to its smaller threshold voltage and smaller C_{RSS}/C_{ISS} ratio. Nevertheless, the temperature-insensitive conduction and switching losses make the SiC MOSFET less prone to the thermal runaway failure at elevated temperatures, especially beyond the Si's limit. This feature may result in a smaller size for the thermal management system than Si converters, and thus may improve the overall power density of the SiC converter. A summary and comparison of the general characteristics of the two devices is listed in Table 4-5.

Table 4-5. Summary of General Characteristics of Si and SiC Power MOSFETs

	Si MOSFET	SiC MOSFET
Blocking voltage	600 V in this study (Limited below 1.2 kV due to large specific $R_{DS(on)}$)	1.2 kV in this study (1.7, 3.3, and even 10 kV devices are available with reasonable specific $R_{DS(on)}$'s [27]-[29])
Leakage current at rated voltage	Unacceptable above 150 ℃	Very small up to 200 ℃
Max. gate voltage	±30 V	+25 V/-5 V
On-state resistance	For $V_{GS} \geq 10$ V: Small at 25 ℃ Increases by > 200% at 125 ℃	For $V_{GS} = 20$ V: Small at 25 ℃ Increases by < 200% at 200 ℃
Threshold voltage	Higher	Lower
Transconductance	Much higher	Much lower
Junction capacitances	Approx. 4x higher C_{ISS} Comparable C_{RSS} & C_{OSS}	Approx. 1/4x lower C_{ISS} Comparable C_{RSS} & C_{OSS}
Switching delay	Slightly longer $t_{d(on)}$ Much longer $t_{d(off)}$	Slightly shorter $t_{d(on)}$ Much shorter $t_{d(off)}$
Conduction loss	Larger	Smaller
Switching loss	Smaller E_{tot} increases at higher temperatures	Larger E_{tot} stays almost unchanged at higher temperatures

From the above study, it can be concluded that the strength of the SiC MOSFET lies in its advantages of higher blocking voltage, higher junction temperature, as well as lower conduction loss, compared to its Si counterparts. In these aspects, the SiC device can easily outperform Si thanks to the material's wider band gap. As a unipolar device, the SiC MOSFET also presents much faster switching speed than Si IGBTs, but still cannot beat the state-of-the-art Si MOSFETs due to its low transconductance. Although high-frequency switching, e.g. 500 kHz, is still possible for special applications, the DAB comparison has shown that the SiC MOSFET is more suitable for the converters with higher DC-link voltage, larger current, and switching frequency up to around 100 kHz, if high efficiency and high power density are the design priorities.

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Chapter 5 Development of SiC Multi-Chip Phase-Leg Modules for High-Temperature and High-Frequency Applications

5.1 Introduction

A general trend in today's aerospace industry is for the modern aircrafts to transition towards a "more electric" architecture, in order to simplify the aircraft system, optimize the overall performance, and more importantly, reduce fuel consumption and emission [1]-[3]. In these applications, having high power density is a critical design target for the converters to save the weight and volume of the whole power conversion system onboard. Generally, higher power density can be achieved by either increasing the switching frequency of the converter to reduce the sizes of passive components, or, by pushing the operating temperature of the semiconductor devices to save on the cooling system [4]. In more electric aircrafts, there even exists a trend to mount the embedded generators, together with their power electronics units, directly onto the engine shafts as a starter and a generator in order to replace the bulky and heavy mechanical parts. In such conditions, the power converter will not only be switched at a high frequency, but also be

exposed directly to the harsh engine compartment environment with an ambient temperature of 200-250 ℃ [3].

An example of such a high-temperature and high-frequency converter is a three-phase voltage-source inverter used to operate the embedded generator/starter in the more electric aircraft, as illustrated in Figure 5-1.

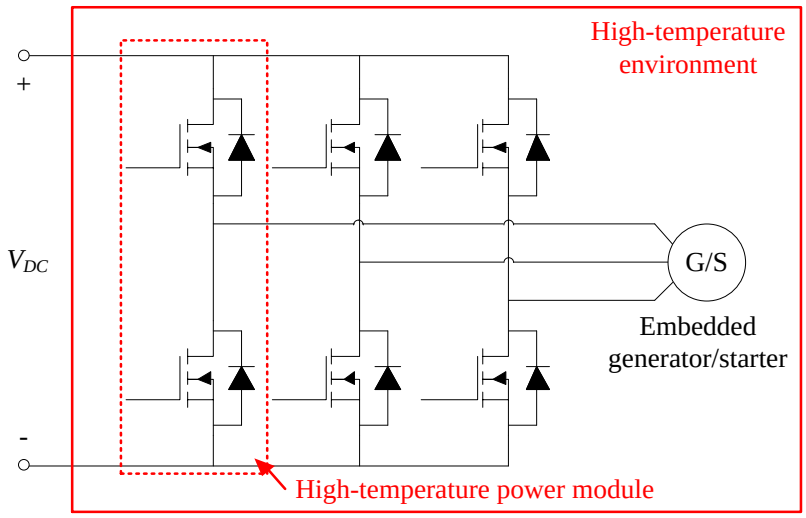


Figure 5-1. A high-temperature, three-phase AC-DC converter with the embedded generator/starter in the future more electric aircrafts

Under the nominal operating condition, the inverter transfers power from a DC voltage source of 540 V to drive the three-phase motor with a RMS voltage of 190 V and a line frequency of 400 Hz. The converter will be exposed to 200 ℃ ambient temperature, and switched at 70 kHz. The switching frequency is selected such that the 2nd-order harmonic at 140 kHz can still avoid the conducted EMI standard starting from 150 kHz. Although a 70 ℃ liquid cooling system is accessible to the power stage, the power modules still need to survive 200 ℃ operation in the worst condition. At the nominal output power of 50 kW, the calculated AC-side RMS current is around 80 A.

Therefore, a 1200 V, 100-120 A phase-leg module will satisfy the electrical specifications of the system, whereas the high-temperature and high-frequency requirements are creating the barrier for common Si IGBT solutions, which are usually limited in both aspects (< 175 ℃ and < 60 kHz).

To achieve the above described power module, two most critical elements are the semiconductor device with high-temperature and high-frequency capabilities, and the module package supporting these operations. In terms of the device, the wide-bandgap, unipolar SiC MOSFET is one of the promising solutions, featuring its potential of operating over 200 ℃ [5]-[8], and switching at a much higher frequency than Si IGBTs [9][10]. Compared to the SiC JFET, the SiC MOSFET also possesses the advantages of being normally-off, easier gate driver design, and commercial availability at the time of the work. Therefore, this work utilizes Cree's first-generation 1200 V, 20 A SiC MOSFET (CPMF-1200-S080B) as the main switch for the power module. The high-temperature performances of the same device in the discrete TO-247 package has been characterized and discussed extensively in Chapter 2.

From the packaging point of view, commercial SiC power modules have become available, but none of them is intended for > 150 ℃ uses [11][12]. For high-temperature and high-frequency operations, various planar packaging technologies have been proposed, intending to achieve lower package parasitics and possible double-sided cooling. However, since the SiC devices are manufactured for wire-bond packaging and have non-solderable aluminum top-side electrodes, all of these works needed to modify the device top metallization by plating, sputtering, or zincating processes, which significantly complicated the module fabrication [13]-[15]. Moreover, none of these top

interconnection methods has been verified in terms of the reliability under either thermal soaking or cycling conditions, making them not suitable for aircraft applications.

In comparison, the wire-bond packaging is still the most mature and widely-adopted technology for high-temperature modules. In [5], a 1200 V, 150 A SiC MOSFET phase-leg module was presented to work at 250 ℃ junction temperature and 15 kHz switching frequency. Ref. [6] and [7] presented two designs of a 1200 V, 100 A SiC MOSFET phase-leg module targeted for 200 ℃ and 20 kHz operations. SiC JFET modules were also presented in [16] as a phase-leg module working at 250 ℃ and 20 kHz, and in [17] as a six-pack module tested to 150 ℃ and 40 kHz. The module structures are basically alike in these works, and the main differences lie in the investigation and implementation of various packaging materials, which has provided a lot of valuable information in their high-temperature performance and reliability [18]-[20]. However, since the wire-bond structure generally suffers from high package parasitics, no work has reported a power module that can take the full advantage of both high-temperature and high-frequency features of the SiC switches.

In this chapter, a wire-bond-based, 1200 V, 60 A SiC MOSFET phase-leg module is firstly designed, fabricated, and fully tested. An extensive literature survey is conducted to find out the right combination of materials for the high-temperature package. The module structure is also optimized based on a modeling and simulation approach to minimize the parasitic effects from the substrate layout and the power terminals. The complete characterizations of the module's static, switching, and continuous operation performances are then conducted to verify the design.

The knowledge and experience obtained from the 60 A module development is then utilized to design a 1200 V, 120 A SiC MOSFET phase-leg module, which has comparable power ratings to the commercial products. The developed module is then compared to its commercial counterpart to show its improvements in both package parasitics and switching performances. Finally, the high-temperature capabilities of the module are verified through complete static and switching characterizations up to 200 ℃.

5.2 Development of a High-Temperature, 1200 V, 60 A SiC Multi-Chip Phase-Leg Module

The state-of-the-art SiC MOSFETs are limited in their single-chip die size out of consideration for the yield. Therefore, the maximum current rating of a single SiC MOSFET commercially available today is only around 20 A (at 100 °C), e.g. Cree's CMF20120D. Other manufacturers, such as GE and Rohm, have also reported their devices with similar current ratings [21]-[23]. Devices with even larger die size have emerged, such as Cree's 1.7 kV, 100 mΩ SiC MOSFET, but are only available in research samples at the time of the work.

For this reason, three SiC MOSFETs (Cree CPMF-1200-S080B) and three SiC Schottky diodes (Cree CPW4-1200-S010B, 1200 V, 10 A each) are paralleled in each switch position in the phase-leg module to reach the rated current of 60 A. The material selection and module layout design are the two critical aspects for the power module to successfully operate in high-temperature and high-frequency conditions.

5.2.1 Material Selections

The cross-sectional structure of the wire-bond module is illustrated in Figure 5-2. Critical materials are carefully selected based on the literature study. The final choices are tabulated in Table 5-1.

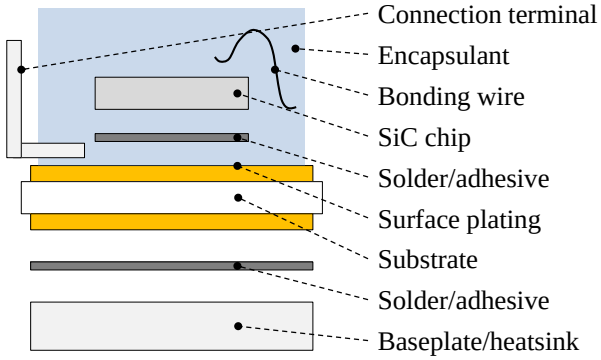


Figure 5-2. Cross-section of the wire-bond module

Table 5-1. Bill-of-Materials for the 1200 V, 60 A SiC MOSFET Power Module

Part	Material	Specifications
Switch	Cree SiC MOSFET	1200 V, 20 A Die size: 4.08 × 4.08 mm^2 Top: gate & source pads, Al metalized Bottom: drain pad, Ag metalized
Diode	Cree SiC Schottky diode	1200 V, 10 A Die size: 2.26 × 2.26 mm^2 Top: anode pad, Al metalized Bottom: cathode pad, Ag metalized
Bonding wire	Al	Dia.: 10 mils 3 wires in parallel for each die, not including wires for gate drive
Solder	Sn5-Pb95	Solidus/liquidus point: 308/312 ℃
Substrate	Curamik AlN DBC	Cu/AlN/Cu thicknesses: 8/25/8 mils Ni-B electroless-plated with 0.5% boron
Encapsulant	NuSil R-2188	-
Connection terminal	Ni (alloy 200)	5 mils in thickness
Baseplate	CPS AlSiC-9	4 mm in thickness

The material selection starts from the direct-bonded-copper (DBC) substrate. A variety of ceramic materials can work as the insulation layer of DBC, among which the most discussed ones are alumina (Al_2O_3) [15], aluminum-nitride (AlN) [5]-[7][14][16][18][24][25], beryllia (BeO) [26], and silicon-nitride (Si_3N_4) [17][27]. The main features of these ceramics are compared in Table 5-2 [28][29].

Table 5-2. DBC Substrate Materials

Ceramic materials		Main features	Thermal conductivity (W/m/K)	CTE* (ppm/K)	Flexural strength (MPa)
Al_2O_3 (99%)	Pros	Very mature, common, and inexpensive	33	7.2	345
	Cons	Lowest thermal conductivity CTE much larger than SiC			
AlN	Pros	Good thermal conductivity CTE matches well with SiC	150-180	4.6	360
	Cons	Average mechanical strength			
BeO	Pros	Mature Best thermal conductivity	270	7.0	250
	Cons	Expensive Dust particles are toxic			
Si_3N_4	Pros	CTE matches very well with SiC Best thermal cycling endurance	70	3.0	932
	Cons	Immature and expensive Average thermal conductivity			

* Coefficient of Thermal Expansion. CTE of SiC is 3.0 ppm/K.

Among the four, Al_2O_3 is the most economic choice but has the worst thermal performance and average mechanical strength. BeO has the highest thermal conductivity, but is also a health hazard in its dust particle form. In comparison, AlN is a safe material featuring much higher thermal conductivity than Al_2O_3, and closer CTE matching with SiC. Its flexural strength is similar to that of Al_2O_3, so is its thermal cycling lifetime

[16][30]. Si_3N_4 is a better choice in terms of its much higher thermal cycling reliability, but the penalties are its higher material cost and lower thermal conductivity. Considering all pros and cons, AlN provides the best balance between performance and cost, and thus is most widely adopted in the high-temperature module developments. AlN is selected in this work for the same reason.

For the bonding wire, aluminum wires are an obvious choice over gold for their thicker diameters and higher current carrying capability. According to the military standard MIL-M-38510, the maximum DC current of an aluminum wire can be determined by

$$I = \kappa \cdot d^{1.5}, \tag{5-1}$$

where I is the maximum current in A, d is the wire diameter in inch, and κ is a constant depending on the wire material and length. For aluminum wires with diameter of 10 mils and length over 40 mils, κ is equal to 15200, meaning that a single wire can carry approximately 15 A current. Considering the current rating, bonding site area, and parasitic impedance, three wires will be bonded in parallel on the source pad of the SiC MOSFET.

The choice of the surface metallization of DBC substrate, nevertheless, is not so obvious. The uses of gold and silver plating have been reported [15][16], but the nickel plating is more widely implemented [5][18][25][26]. Studies have shown that the aluminum-nickel combination generates higher bonding quality and longer thermal cycling lifetime [31][32]. Furthermore, among different types of electroless nickel plating, nickel-boron (Ni-B) provides better bonding quality and solderability than

nickel-phosphor (Ni-P). Therefore, the electroless Ni-B plating with 0.5% boron is used in this work for the substrate surface coating.

As for the die attachment, soldering is still the most popular and mature method [6][7][16]-[18][25], although other techniques have also been reported for high-temperature uses, such as polyimide-based conductive adhesive curing [26], silver-glass composite attaching [24], nano-Ag paste sintering [15], and Ag-Sn transient liquid phase attaching [5], etc. The solder with a melting temperature over 250 ℃ is preferred for the module in this work. Popular materials that fall within this range are summarized in Table 5-3. Since the substrate is nickel plated in this work, Pb-based solders are more suitable choices over Au-based ones for their better solderability. Sn5-Pb95 is finally selected considering its best compromise between performance and cost. During the module fabrication, the soldering is performed by vacuum reflow (using SST MV-2200 vacuum reflow furnace) with Sn5-Pb95 solder preform to achieve less voids and flux-free attachment [33].

Table 5-3. High-Temperature Solder Materials

Solder materials	Solidus/liquidus temperature (℃)	CTE (ppm/K)	Thermal conductivity (W/m/K)
Sn5-Pb95	308/312	28	32
Pb92.5-In5-Ag2.5	300/310	25	25
Pb97.5-Ag1.5-Sn1	309/309	30	23
Au80-Sn20	280/280	16	57
Au88-Ge12	356/356	11	88

A baseplate is necessary for the module to be mounted on the liquid cooling plate. A comparison of commonly used materials is summarized in Table 5-4 [6][28][34]. Pure

copper baseplate is not usually used in high-temperature modules due to its CTE mismatch with the AlN substrate, although it has the highest thermal conductivity. Metal matrix composites (MMC) are becoming more popular, and the uses of Cu/Mo [5][17], Cu/C [6], and AlSiC [18][24], have been reported. Generally, all MMC baseplates can be tailored in their composites to have a closer CTE match with the substrate. Cu-based MMC baseplates usually have higher thermal conductivity, but also suffer from heavier weight and higher cost. AlSiC baseplates have just the complementary features. Therefore, a trade-off needs to be made between the thermal performance, weight, and cost of the module. In this design, AlSiC-9 from CPS Technologies is selected, mainly considering its lighter weight, lower cost, and availability.

Table 5-4. Baseplate Materials

Baseplate materials	Thermal conductivity (W/m/K)	CTE (ppm/K)	Mass density (g/cm^3)
Cu	398	17.8	8.96
Cu/Mo	165-275	6.8-13	9.3-10
Cu/W	130-205	5.6-9	14.8-17
Cu/C	200	4	-
AlSiC CPS AlSiC-9	170-200 180	6.5-13.8 8.4	2.97-3.04 3.01

For the connection terminals of this module, nickel alloy 200 is selected. However, for modules with higher current rating, nickel-plated copper is also suitable.

The encapsulating material is finally chosen to provide chemical protection, mechanical support, and electrical insulation for the module. An extensive study has been conducted to compare seven different encapsulation materials in their processability before curing, and dielectric properties after 250 ℃ thermal aging [35]. A silicone-based

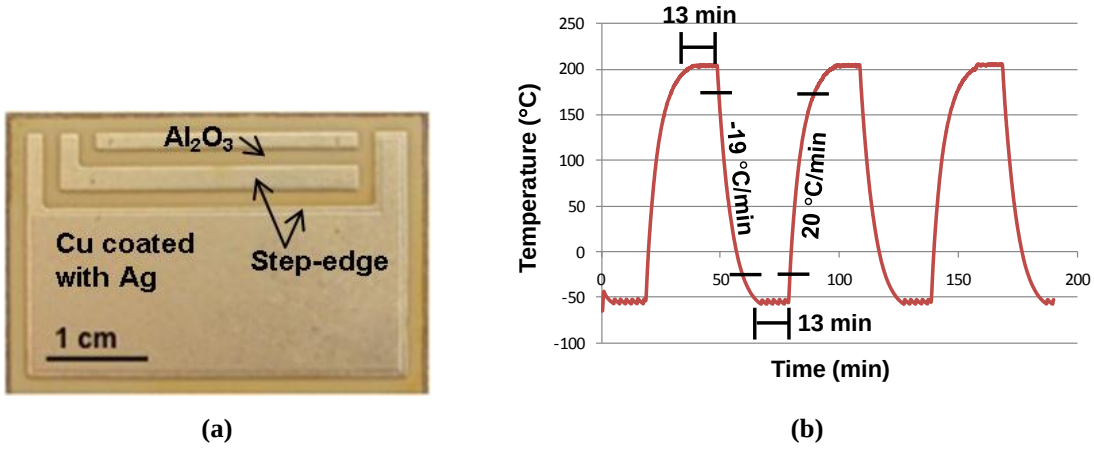
material NuSil R-2188 is finally selected due to its best performance under the high temperature.

5.2.2 Thermal Cycling Reliability of DBC Substrates with Stepped, Sealed Edges

Thermal cycling is a common operating condition of converters in aerospace applications. The CTE mismatch induced stresses between interfacing materials will finally cause module failure by cracking, delamination, etc., due to the thermal cycling fatigue. While the bonding wire lift-off is known to be a main failure mechanism, previous work found that the DBC substrate might fail even faster in the form of copper layer delaminating from the ceramic [7][16]. To improve the reliability of Al_2O_3 or AlN substrates, Ref. [16] proposed to etch out a step surrounding the DBC copper pattern with half the thickness of the copper layer, which helped release the peeling stress on the copper edges. An epoxy adhesive Epo-Tek 600 was further used to seal the stepped edges, providing additional bonding force. By doing so, the thermal cycling lifetime of the Al_2O_3 substrate was improved by almost 20 times, from 60 to 1000 cycles under a profile from -55 to 250 ℃. However, in order to avoid introducing new materials in the module, thermal cycling tests are repeated on DBC substrates with NuSil R-2188 as the sealing material. Al_2O_3 substrates are used to reduce the cost, as shown in Figure 5-3 (a). The adopted cycling profile is illustrated in Figure 5-3 (b). Detailed test results and analysis are documented in [36]. The tests reveal that NuSil R-2188 can also significantly improve the substrate lifetime, as indicated in Table 5-5.

It needs to be noted that there is no established thermal cycling profile for high-temperature power modules, so various low/high temperatures, ramp rates, and dwell time have been used [13][16][18][27]. The adopted profile in this work considers the

ambient temperature requirement, as well as the equipment constraints in the lab. The profile is actually very close to the military standard MIL-STD-883H, except for the slower ramp rates limited by the equipment.



(a) **(b)**

Figure 5-3. Thermal cycling sample with stepped edges (a), and cycling profile (b)

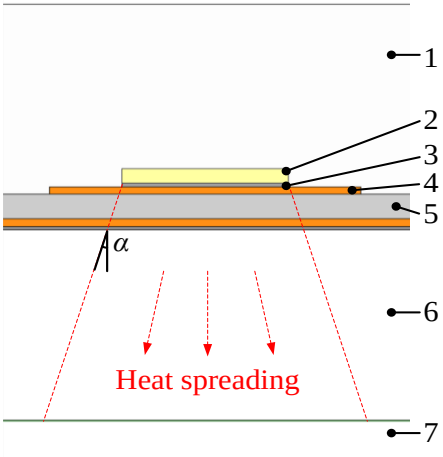
Table 5-5. Al_2O_3 Substrate Thermal Cycling Lifetime

Sample	Lifetime
Original substrate	< 100 cycles
Stepped-edged substrate	100 cycles
Stepped-and-sealed-edged substrate	> 900 cycles

5.2.3 MOSFET Die Spacing and Thermal Design

With the above material selections, the stacked structure of the power module is illustrated in Figure 5-4 (a). The respective thickness and thermal conductivity of each material are tabulated in Figure 5-4 (b). As seen, the heat generated by the device losses will spread through materials at a thermal spreading angle α (Note that the heat dissipated through the encapsulant is neglected in this study since the material is a very bad thermal conductor). Therefore, when the heat flux travels to the bottom of the baseplate, it covers

an area larger than the MOSFET die size. For this reason, if the two paralleled MOSFETs are placed too close to each other, the thermal cross coupling effect may happen, which will increase the effective thermal resistance of each device compared to the single-chip condition [37].



(a)

No.	Material	Thickness (mm)	Thermal conductivity (W/m/K)
1	NuSil R-2188	5	0.16
2	SiC MOSFET	0.365	370
3	Sn5-Pb95	0.1	32
4	DBC Cu	0.2032	398
5	DBC AlN	0.635	180
6	AlSiC-9	4	180
7	Al	-	240

(b)

Figure 5-4. Power module stacked structure (a) and corresponding material properties (b)

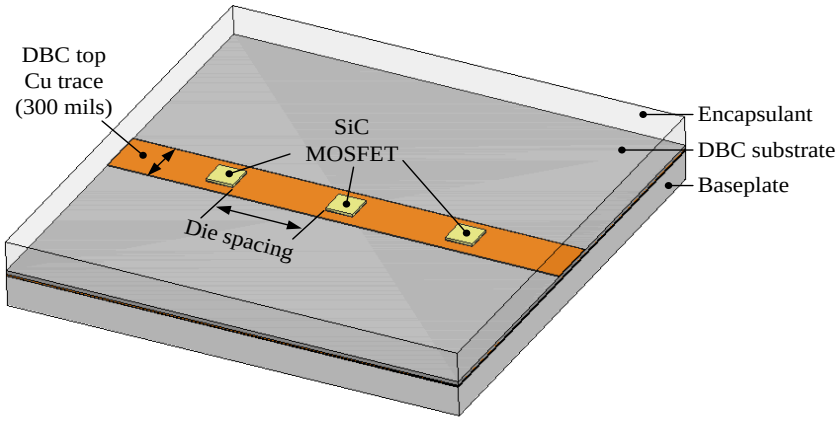
The thermally decoupled condition occurs when the heat spreading areas from the two adjacent MOSFETs do not overlap on the bottom of the baseplate [38]. To calculate the corresponding die spacing distance, it is necessary to know the heat spreading angle. A simple rule of thumb is to assume a 45 ° angle through all stacked materials. However, in this work a more accurate calculation is carried out to obtain the spreading angle which actually changes with the thermal properties of interfacing materials. According to [38], the thermal spreading angle is given by

$$\alpha_a = \arctan\left(\frac{k_a}{k_b}\right), \tag{5-2}$$

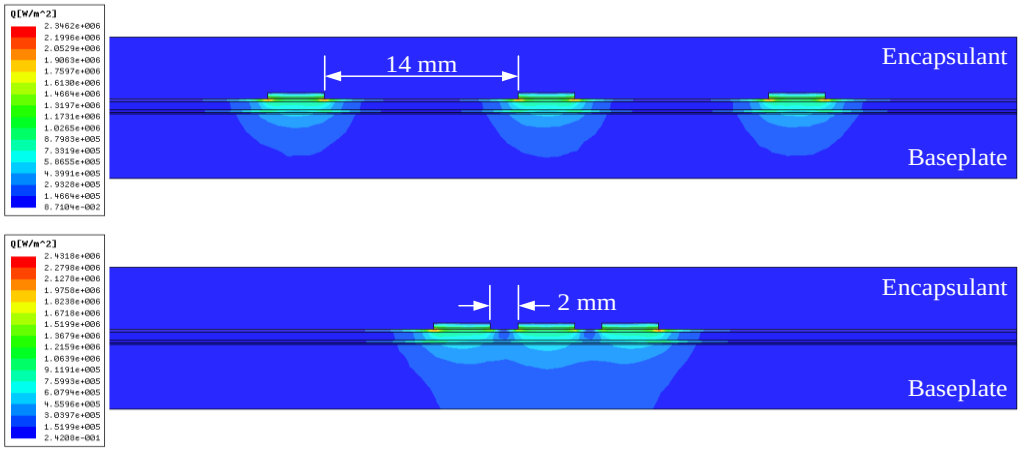
where α_a and k_a are the spreading angle and thermal conductivity in material a, and k_b is the thermal conductivity in material b, which is downstream to a in the heat spreading direction. Note that to calculate the spreading angle in the baseplate, a pure aluminum cooling plate is assumed under the baseplate.

Using Eq. (5-2) and the material properties in Figure 5-4 (b), the minimum die spacing (edge-to-edge) of 13 mm can be obtained to reach a thermally decoupled condition. The corresponding junction-to-case thermal resistance R_{thJC} is calculated to be 0.5 K/W. This distance ensures the full utilization of the heat spreader, but is obviously too large for the multi-chip module. In [28], it is suggested that the thermal intensive chips should be separated by a minimum distance of $D/2$ to reduce the thermal cross coupling, where D is the dimension of the chip. In this work, $D/2$ is 2.04 mm for the SiC MOSFET. Therefore, a design trade-off needs to be made between smaller module size and better heat dissipation to determine the die spacing between 2 and 13 mm.

Thermal simulation is carried out in Ansoft ePhysics to determine the proper die spacing [39]. The simulation model is shown in Figure 5-5 (a). Each MOSFET is assumed to generate a worst-case total loss of 20 W according to the converter simulation results. The bottom surface of the baseplate is assumed to have the same temperature as the cooling plate, which is 70 ℃. The die spacing is then swept from 2 to 14 mm in the simulation. Figure 5-5 (b) shows the heat flux distributions on the cross-section of the model under two extreme conditions. It is clear to see the thermally decoupled condition for the 14 mm spacing case, and the thermal cross coupling for the 2 mm case. In (c), the effective R_{thJC} for the side and center MOSFETs are shown.



(a)



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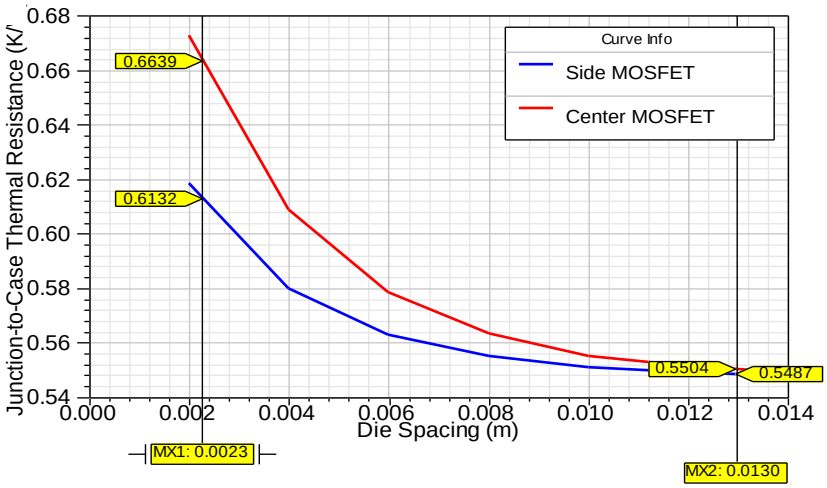


(c)

Figure 5-5. Thermal simulation to determine the die spacing

(a) Simulation model, (b) cross-sectional heat flux distributions, (c) effective R_{thJC}

When thermally decoupled, the adjacent MOSFETs have the same R_{thJC} of about 0.55 K/W, consistent with the theoretical calculation. As die spacing decreases, the effective R_{thJC} increases due to the thermal cross coupling, and the center MOSFET tends to have a higher thermal resistance than the side MOSFETs. At 2 mm, the effective R_{thJC} are 0.67 and 0.62 K/W for the center and side MOSFETs, which correspond to only 1 ℃ difference in the device temperature rise under 20 W loss. Increasing the die spacing from 2 to 14 mm only reduces the temperature rise by 2.4 ℃. Therefore, the thermal cross coupling will not be a severe problem for the module as long as MOSFETs are over 2 mm apart. In the actual design, 90 mils (= 2.286 mm) is determined as the MOSFET die spacing.

5.2.4 Layout Comparison and Module Design

The wire-bond structure generally suffers from high parasitic impedances, which is a detrimental factor for the high-frequency operation of the power module. The layout of the module substrate thus needs to be carefully designed to minimize the parasitic effects.

The conventional layout in most commercial phase-leg modules would place the main switch right next to its anti-parallel diode. As discussed in Chapter 3 and 4, this simple and straightforward arrangement may not lead to the best switching performance. In the hard-switching condition, the current commutation loop, namely the loop formed by the DC buses and the "switch-pair" (i.e. the MOSFET and its freewheeling diode), is more critical in determining the parasitic ringing, as this loop "sees" the most severe di/dt during the switching transients. Based on this concept, an improved layout may be achieved by putting the main switch in close proximity to its freewheeling diode [40]. To further verify this concept in a multi-chip SiC module, in this work both layouts are

designed and compared in their respective package parasitics and how they influence the switching waveforms.

As illustrated in Figure 5-6, the two designs follow the same criteria, such as the minimum trace width and clearance, etc. The conventional design is more straightforward and results in a simpler pattern. In contrast, the improved layout seems more complicated at the first sight because of the rearrangement of die positions, and the resultant area is also 15% larger (2071.5 mm^2 vs. 1807.0 mm^2). Both designs are then modeled and simulated in Ansoft Q3D, and the extracted minimum and maximum possible switching loop inductances are summarized in Table 5-6. Since the proposed design purposefully optimizes the switching loop, the loop inductances are found to be roughly 35% lower than the conventional layout, even though the new design exhibits a larger area.

As expected, the smaller parasitic inductances also translate to less ringing in the switching waveforms. Figure 5-7 shows the simulated waveforms of the two designs, both turning-off 540 V and 60 A, with estimated parasitics from the Q3D simulation. It is clear that the improved layout effectively reduces the ringing at turn-off, with V_{DS} peak seen to decrease from 615 V to 588 V. Similar results can also be obtained at different switching conditions. Therefore, the layout in Figure 5-6 (b) is selected for the module in this work.

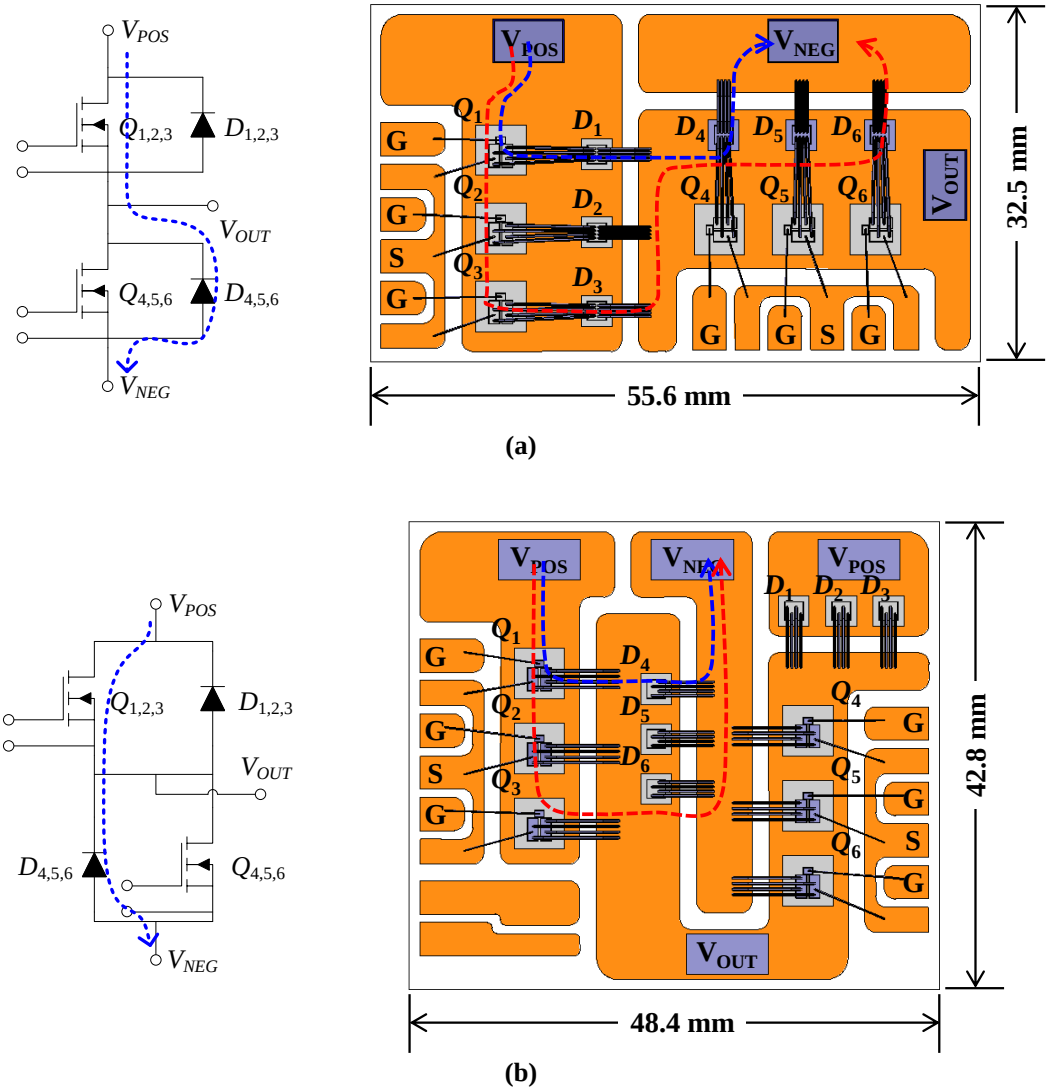


Figure 5-6. Two designs of substrate layouts: Conventional layout (a) and improved layout (b) In right-hand-side figures: Blue dashed – minimum possible switching loop; red dashed – maximum possible switching loop

Table 5-6. Comparison of Switching Loop Inductances (Q3D AC Simulation at 40 MHz)

	Conventional layout		Improved layout		Improvement in %	
	Switch pair $Q_{1,2,3}$ & $D_{4,5,6}$ L_1 (nH)	Switch pair $Q_{4,5,6}$ & $D_{1,2,3}$ L_2 (nH)	Switch pair $Q_{1,2,3}$ & $D_{4,5,6}$ L_3 (nH)	Switch pair $Q_{4,5,6}$ & $D_{1,2,3}$ L_4 (nH)	$\frac{L_3 - L_1}{L_1}$	$\frac{L_4 - L_2}{L_2}$
Min.	12.4	12.4	7.9	7.7	-36.3%	-37.9%
Max.	15.5	12.7	10.3	11.1	-33.5%	-12.6%

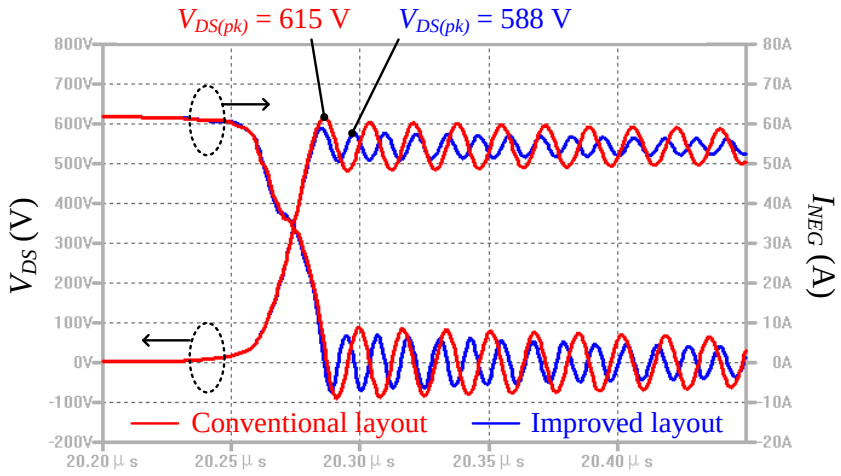


Figure 5-7. Simulated turn-off waveforms of the two designs in Figure 5-6

The final module design together with the connection terminals is illustrated in Figure 5-8. As seen, the DC terminals are designed in the laminated structure to minimize their loop inductance. Even so, these terminals still introduce around 7 nH extra inductance in the switching loop, according to the Q3D simulation. This much inductance would contribute almost 50% of the total parasitic inductance inside the module. To deal with this, two high-temperature, DC decoupling capacitors are directly embedded inside the module to "close the loop" and provide a low-impedance path for the ringing current, as shown in the same figure. Both are ceramic capacitors from Presidio Components, rated at 1 kV, 22 nF, and 225 ℃ maximum working temperature [41]. The capacitance value is selected considering the decoupling requirement discussed in Chapter 3. For this particular module, the total junction capacitance of three MOSFETs and three diodes in parallel is 540 pF at the DC bias of 540 V. The selected capacitors will thus provide around 80 times higher capacitance than that of the devices, and therefore should achieve a sufficient decoupling effect.

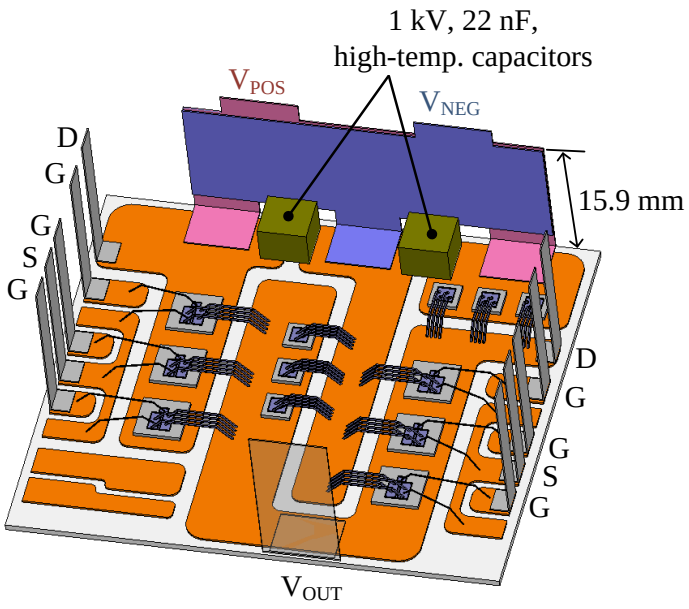


Figure 5-8. 3D package model of the power module

5.2.5 Predicting Module's Switching Performances by Modeling and Simulation

The layout design guideline discussed in the previous section can help module designers minimize the critical parasitic inductances. Nevertheless, once a design is made, designers may also want to evaluate the switching characteristics of the module besides just knowing the package parasitics, since the ultimate module performances are determined by both the power devices and the package. Traditionally, this can only be accomplished after the module is fabricated and tested, which usually makes the design process longer and more costly, especially when the design does not meet the requirements and thus needs iterations. To address this issue, in this section a modeling-and-simulation-based approach, which was introduced in [42], is utilized to predict the power module's switching waveforms before realizing the hardware. It will also be demonstrated below how this method can be used as an effective design tool to improve the module's performance under high-switching-speed conditions.

The 3D package model of the power module is firstly built in Ansoft Q3D, as illustrated in Figure 5-8. Material properties are then assigned to the different parts of the module, such as copper, aluminum, nickel, and AlN ceramic, etc. Note that all semiconductor devices are purely geometry models and are not included in the Q3D simulation.

After assigning electrical excitations to the module terminals, AC-impedance (*R*, *L*, and *C*) simulation is performed. Using the finite element analysis method, Q3D calculates the equivalent inductances of separate conductor nets in the model based on the well-established partial inductance concept [43]. Unlike the previous simulation of Table 5-6 where the loops' self-inductances are evaluated, in this case both the self- and mutual-inductances are extracted in the form of an inductance matrix. Such a matrix contains much richer parasitics information than the lumped loop inductances, and thus will predict the switching waveforms more accurately.

The *R*, *L*, and *C* matrices are then exported to an equivalent impedance network in the SPICE netlist form (i.e. the package model) to be used in a circuit simulator. Figure 5-9 shows the symbol of this model.

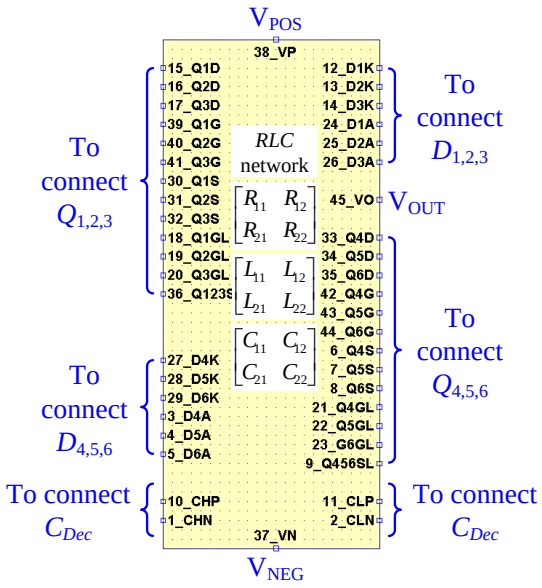
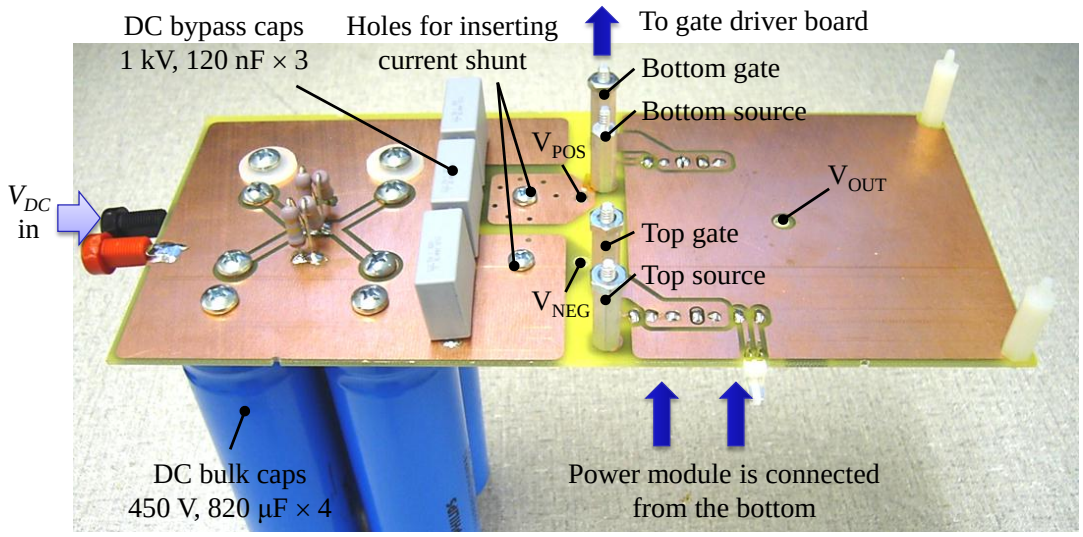


Figure 5-9. The package model symbol for the 60 A module

As discussed in Chapter 3, the parasitic ringing of the switch is not only dependent on the module's own stray inductances, but also on the impedance of the DC bus. In order to faithfully predict the switching waveforms, the bus structure also needs to be modeled and simulated. In this work, the bus structure of the double-pulse tester, which is used to characterize the module, is analyzed in Q3D as well. The tester board is shown in Figure 5-10. Following the same modeling procedure, a similar package model can be obtained for the double-pulse tester. To verify the model accuracy, the DC bus impedance of the tester is measured with Agilent 4294A impedance analyzer and then compared with the simulated results predicted by the model. As illustrated in Figure 5-11, the predicted impedance with both the capacitor and PCB models agrees with the measurement much better than the one with capacitor models only, especially at the high-frequency end where the ringing may occur. Therefore, the package model from Q3D is validated to provide a good approximation of the impedance characteristics of the real circuit.



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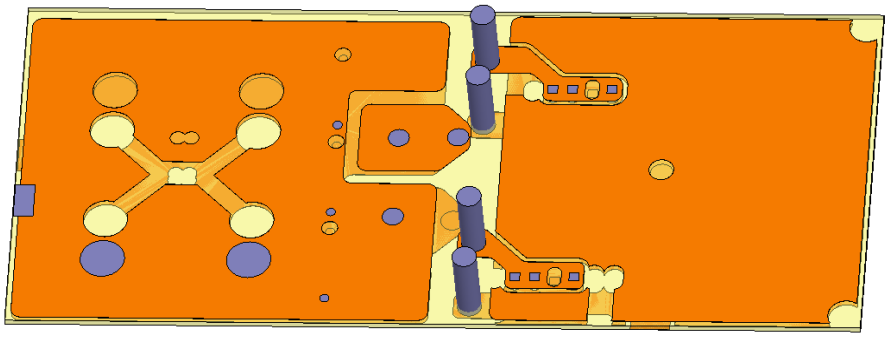

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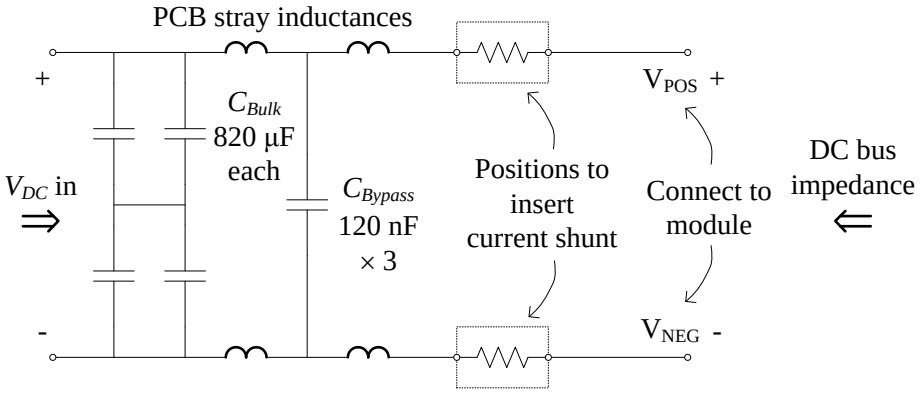


(c)

Figure 5-10. The double-pulse tester used to characterize the power module

(a) Tester board with DC bus capacitors, (b) PCB model in Q3D, (c) DC bus schematic

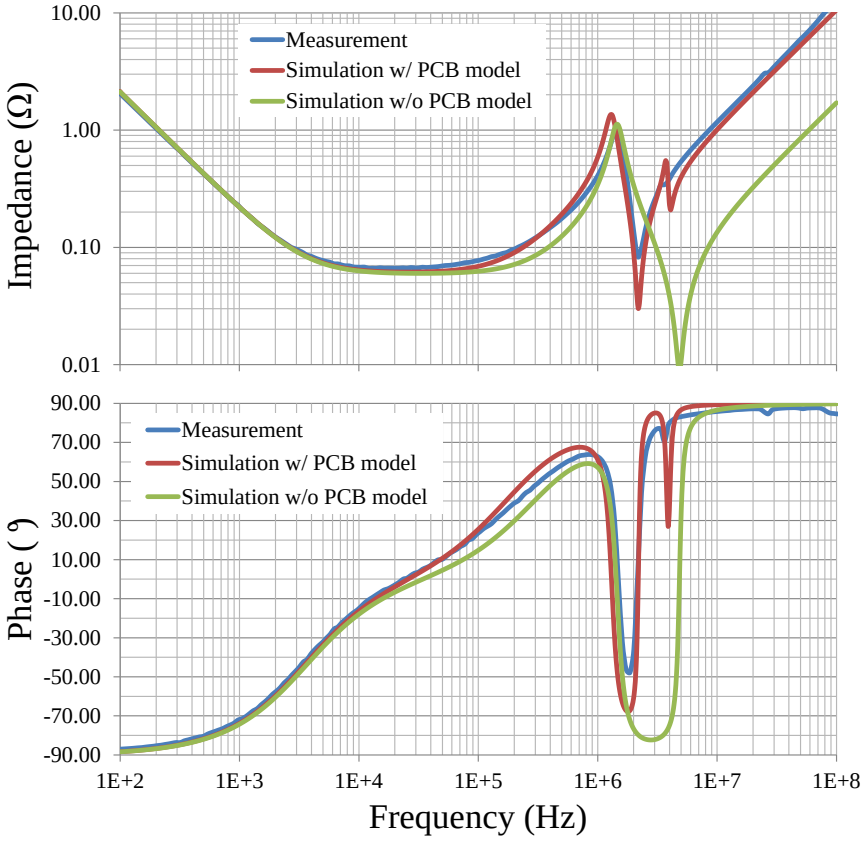


Figure 5-11. Verification of DC bus impedance

The package models of the power module and the double-pulse tester are then combined with the manufacturer's device models to simulate the switching waveforms of the module. The simulation circuit is shown in Figure 5-12. In order to get a more accurate prediction, models of the peripheral circuits are also included in the simulation, such as the bus capacitors, current shunt, load inductor, and gate driver, etc. The modeling processes of the passive components are discussed in detail in [42]. As for the gate driver, a simple voltage source is used in the simulation to catch the same *dv*/*dt* of Cissoid's high-temperature phase-leg driver HADES, which is the actual driver used for the high-temperature converter [44].

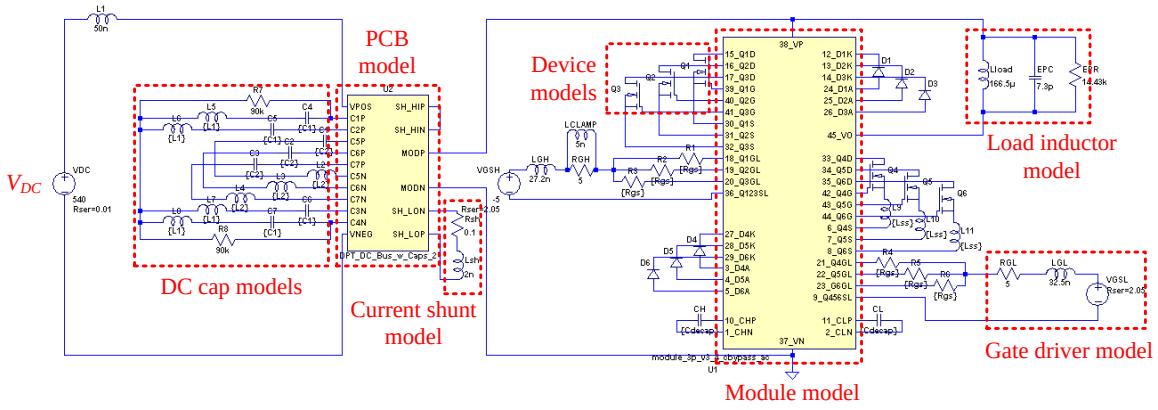


Figure 5-12. Simulation circuit of the module in the double-pulse configuration

The simulation is firstly conducted without including the embedded decoupling capacitors. Figure 5-13 shows the simulated switching waveforms of the bottom MOSFETs with an external gate resistance R_G of 15 Ω, in addition to the gate driver's internal output resistance of 5 Ω. Note that in this figure, the current-sensing shunt resistor is in series with the module's negative terminal (V_{NEG}), so I_{Shunt} represents the current flowing through the bottom devices. As seen, the slow switching speed results in small parasitic ringing, but at the same time long switching delay times and high switching loss.

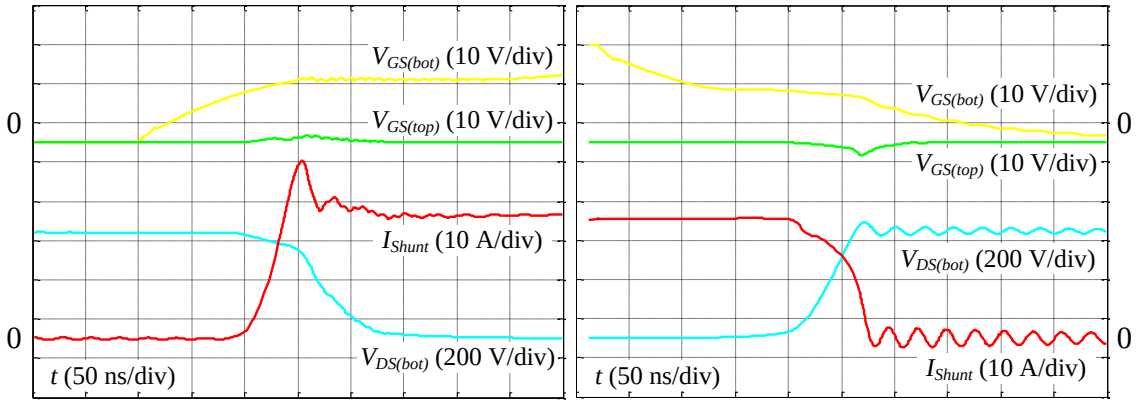
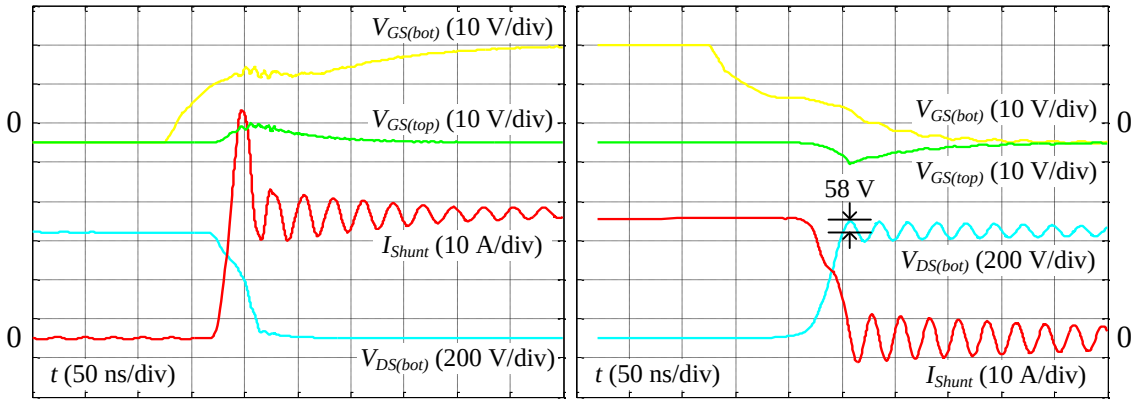


Figure 5-13. Simulated switching waveforms of the bottom MOSFETs at 540 V, 30 A with R_G = 15 Ω

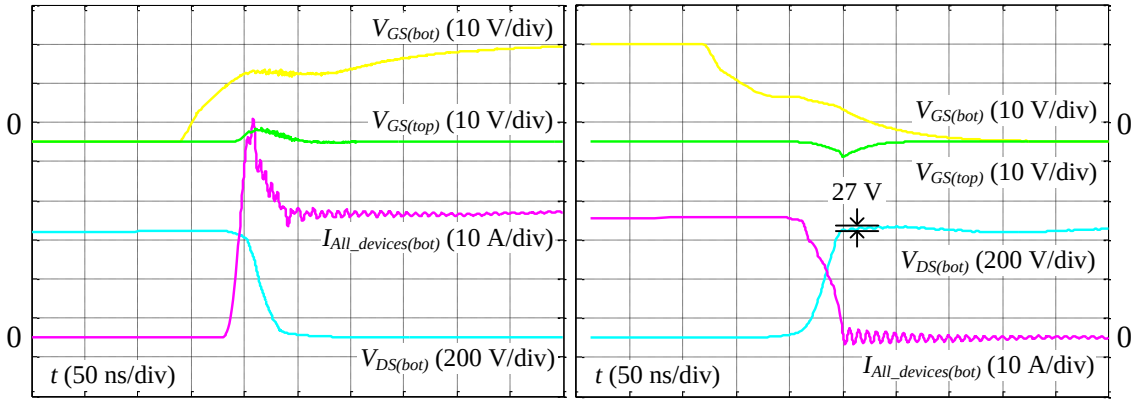
To push the module's switching speed, R_G is reduced to zero in the simulation. Without the decoupling capacitors, smaller switching delays and loss are achieved at the penalty of more severe parasitic ringing, as shown in Figure 5-14 (a). In the $V_{DS(bot)}$ waveform, the voltage dip at turn-on and overshoot at turn-off clearly indicate the *di*/*dt*-induced voltage drop across the module's switching loop inductance.

The ringing in the MOSFET's switching voltage and current waveforms can be reduced substantially when the 44 nF decoupling capacitance is included in the simulation, as seen in Figure 5-14 (b). The MOSFET V_{DS} dip disappears at turn-on, and the over-voltage also decreases from 58 V to 27 V at turn-off. The *dv*/*dt* and *di*/*dt*, however, are essentially the same, indicating unchanged switching speed.

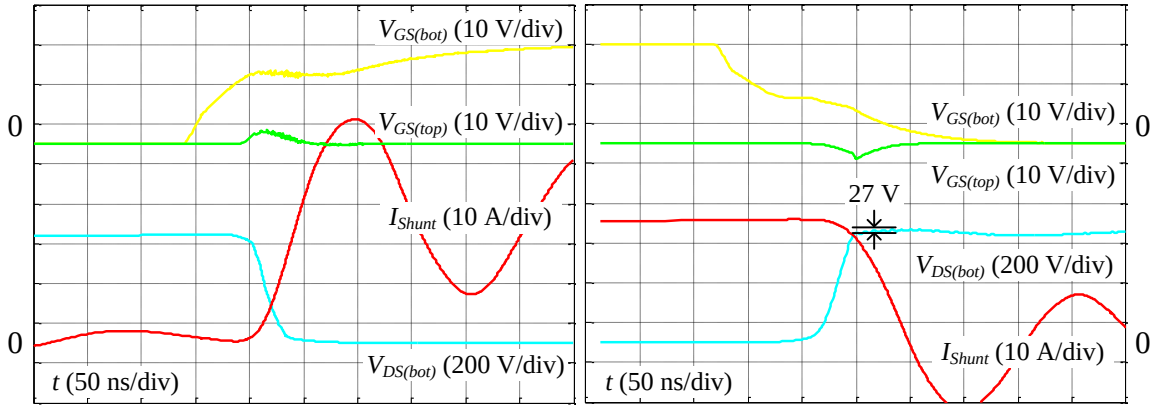
Note that in real tests, the device current is not physically accessible from the module terminal due to the existence of decoupling capacitors. Therefore, the waveforms shown in Figure 5-14 (c) will be measured – the I_{Shunt} waveform will contain a low-frequency oscillation due to the capacitive current.



(a)



(b)



(c)

Figure 5-14. Simulated switching waveforms of the bottom MOSFETs at 540 V, 30 A with R_G = 0 Ω

(a) Module waveforms with C_{Dec} = 0,

(b) module waveforms with C_{Dec} = 44 nF, switching current excluding C_{Dec} current,

(c) module waveforms with C_{Dec} = 44 nF, switching current including C_{Dec} current

5.2.6 Module Characterizations

Two modules, with and without the capacitors, are fabricated to verify the above design. Figure 5-15 shows the module with embedded capacitors. As seen, a thermistor (Honeywell 135-103LAF-J01) is also attached on the bottom left corner of the DBC substrate to measure the module temperature.

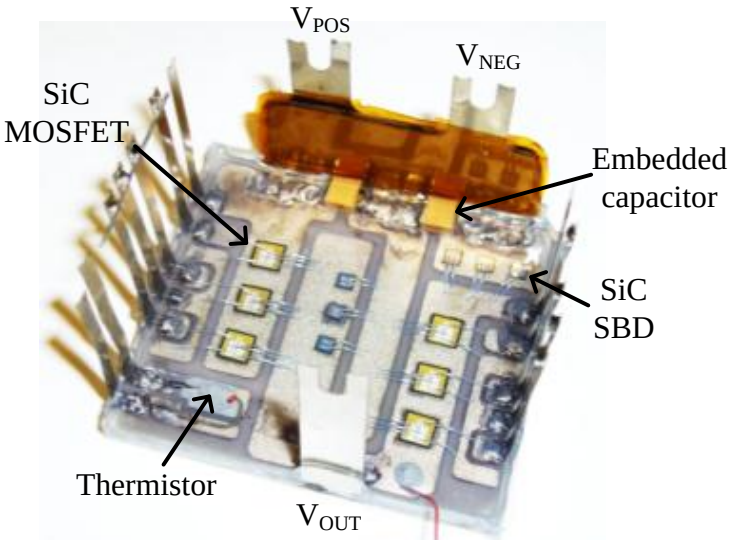


Figure 5-15. Fabricated 1200 V, 60 A SiC MOSFET phase-leg module

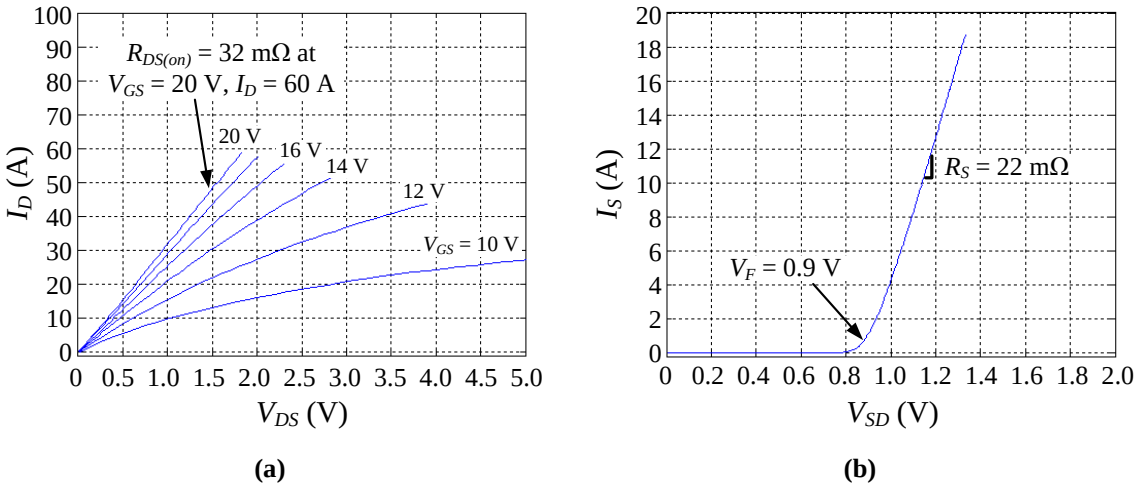


Figure 5-16. Static characteristics of the 60 A module at room temperature. (a) Forward, (b) reverse

Figure 5-16 shows the forward and reverse *I-V* curves of one of the switches in the phase-leg. The measured $R_{DS(on)}$ is 32 mΩ, just 5 mΩ higher than the total die resistance (80 mΩ / 3 ≈ 27 mΩ), indicating a good packaging quality of the module.

To characterize its switching performance, the module is assembled on the double-pulse tester as illustrated in Figure 5-17. Cissoid's half-bridge driver HADES, which is based on the silicon-on-insulator (SOI) technology, is used in this work to provide a complete high-temperature solution for the power stage of the converter. The driver provides +20 V/-5 V gate biases to switch the SiC MOSFETs [44]. A current shunt resistor is also connected in series with the module's negative DC terminal (V_{NEG}) to sense the module current (i.e. I_{Shunt}).

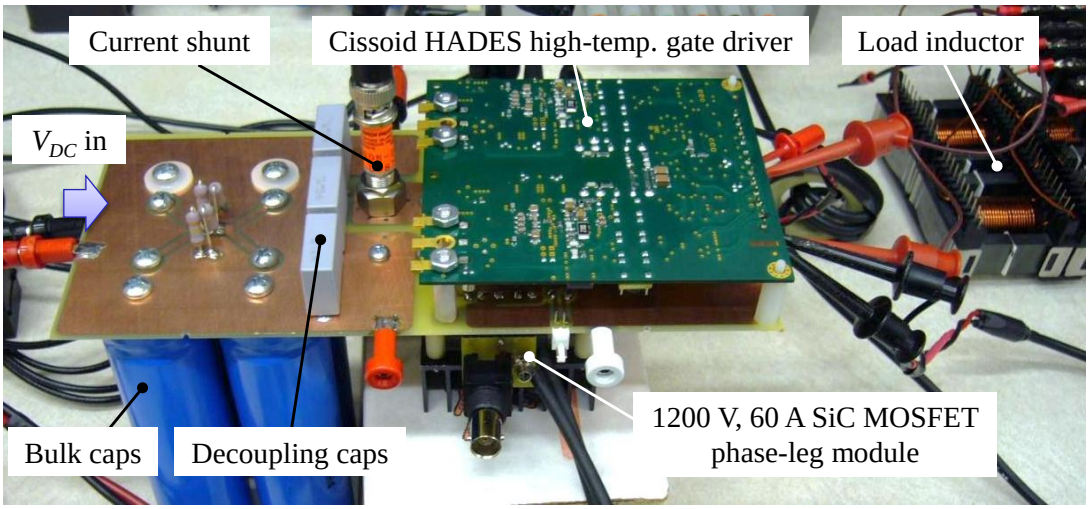


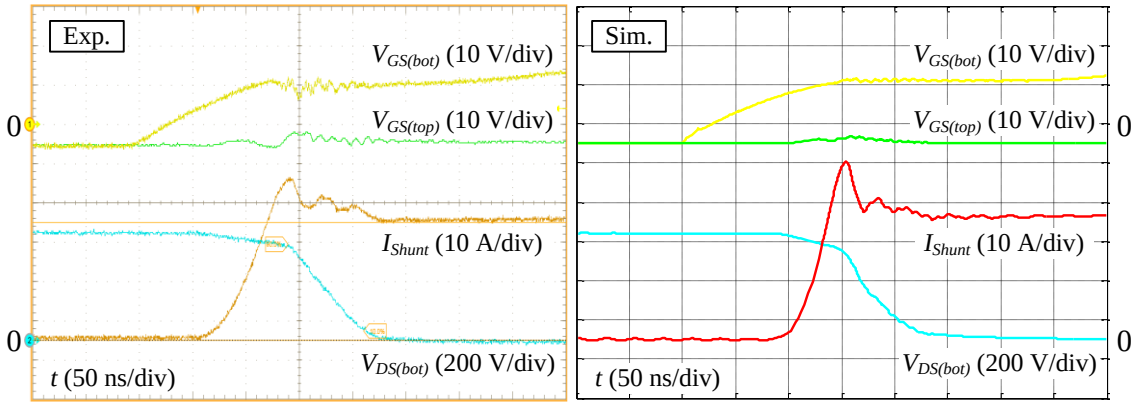
Figure 5-17. Switching test setup for the 60 A module

The module without capacitors is firstly tested at 540 V bus voltage and various load currents. An external R_G = 15 Ω is firstly used, and the resultant turn-on waveforms of the bottom MOSFETs are shown in Figure 5-18 (a). For comparison, the simulated waveforms under the same switching condition are repeated on the right, which show a

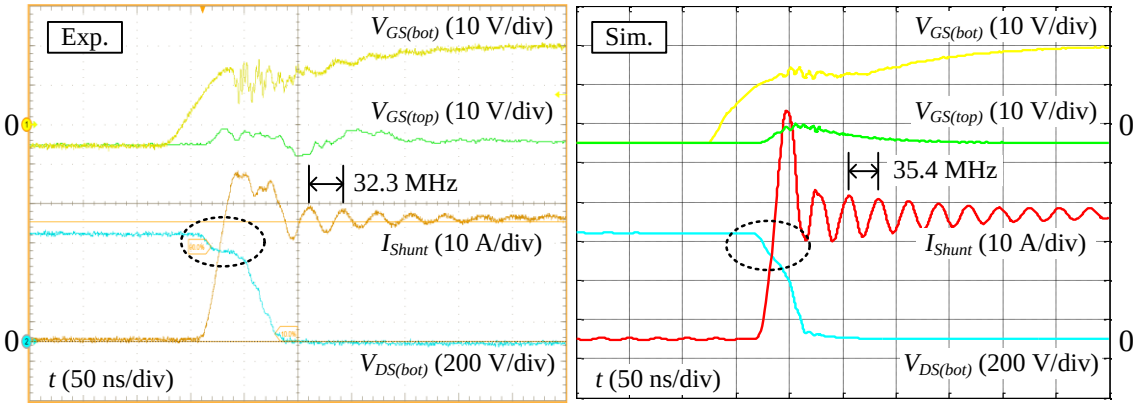
good agreement with the experimental results. When R_G is reduced to zero, more severe ringing can be observed in $V_{DS(bot)}$ and I_{Shunt} waveforms, as seen in Figure 5-18 (b) and (c). Again, the simulation predicts correctly the $V_{DS(bot)}$ dip at turn-on and overshoot at turn-off, which is due to the voltage drop across the switching loop inductance. The simulated ringing frequencies during the switching transients also match the experiment very well. The only mismatch between the simulation and experiment is the I_{Shunt} turn-on overshoot. The experiment shows a smaller current spike than the simulation due to the magnetic coupling effect between the power stage of the double-pulse tester and the Cissoid gate driver, which is not considered in the modeling process.

The module with decoupling capacitors is tested in the same condition. The experimental and simulated results are shown in Figure 5-19. Comparing $V_{DS(bot)}$ waveforms in this figure and Figure 5-18 (b) and (c), one can clearly see that the parasitic ringing reduces significantly. The $V_{DS(bot)}$ dip at turn-on disappears, and the over-voltage at turn-off decreases from 56 V to 32 V – both showing the evidence of smaller loop inductance. Furthermore, V_{GS} waveforms are also cleaner thanks to the less ringing from the power side.

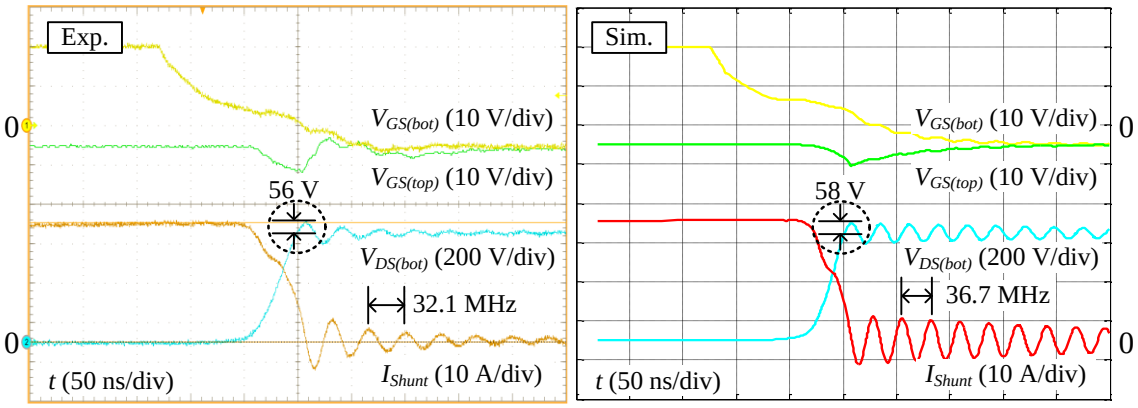
As mentioned previously, in Figure 5-19, the measured I_{Shunt} carries a low-frequency oscillation due to the capacitive current, and this trend has already been captured by the simulation shown on the right. Since the simulation exhibits a good agreement with the experiments in Figure 5-18 and Figure 5-19, it can be inferred from Figure 5-14 that both the switching voltage and current of the power devices have been improved by embedding capacitors inside the module.



(a)



(b)



(c)

Figure 5-18. Experimental and simulated switching waveforms of the 60 A module without capacitors

(a) Turn-on waveforms at 540 V, 30 A, with R_G = 15 Ω,

(b) & (c) turn-on and turn-off waveforms at 540 V, 30 A, with R_G = 0

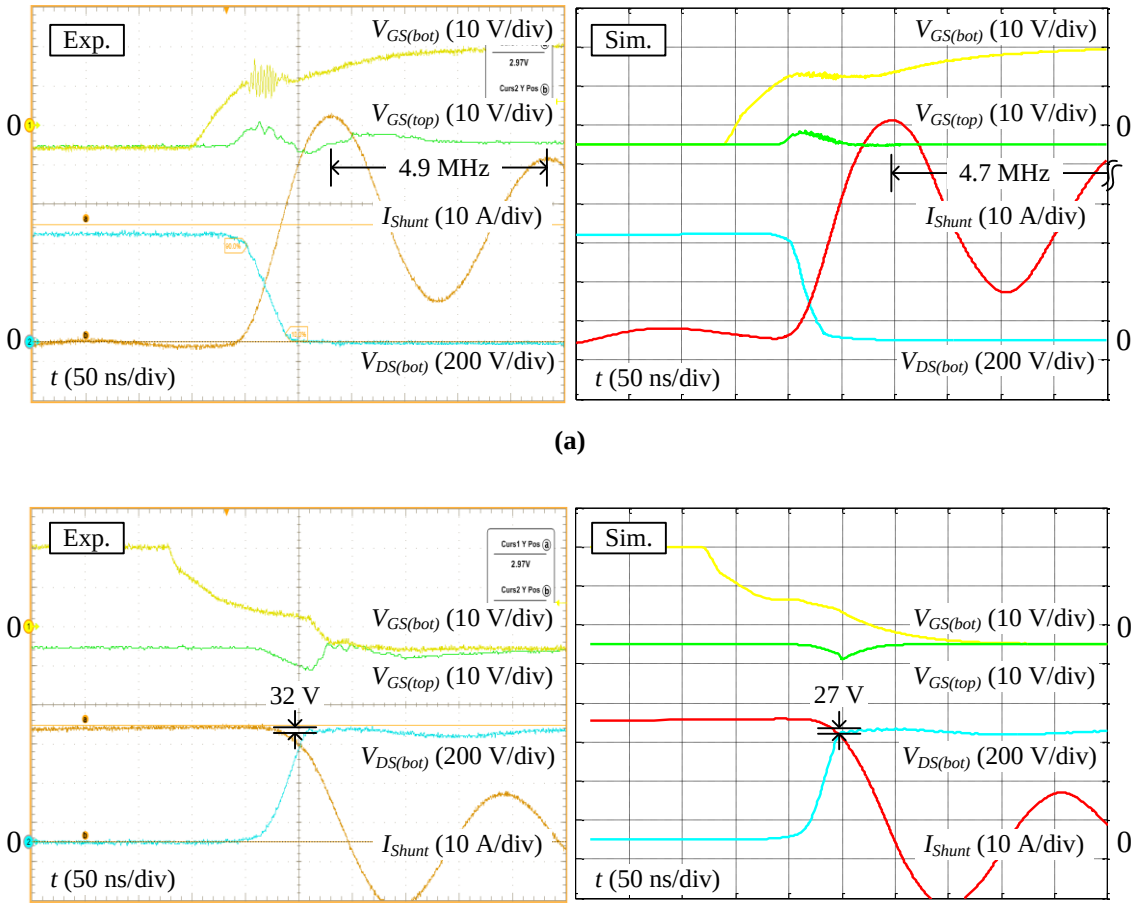


Figure 5-19. Experimental and simulated switching waveforms of the 60 A module with capacitors (a) Turn-on waveforms, and (b) turn-off waveforms at 540 V, 30 A, with R_G = 0

The switching energies of the module are calculated based on the experimental waveforms. As shown in Figure 5-20, E_{on} is still a dominant part compared to E_{off}. The total switching loss is measured to be 930 μJ at 30 A, and is projected to be 1640 μJ at the rated current of 60 A. Thanks to the use of SiC devices, the achieved switching loss is only around 10-20% of that of a similar Si IGBT module. This allows the SiC converter to operate at a higher frequency of 70 kHz or even above, while still generating similar or even less total switching loss compared to an equivalent Si IGBT converter.

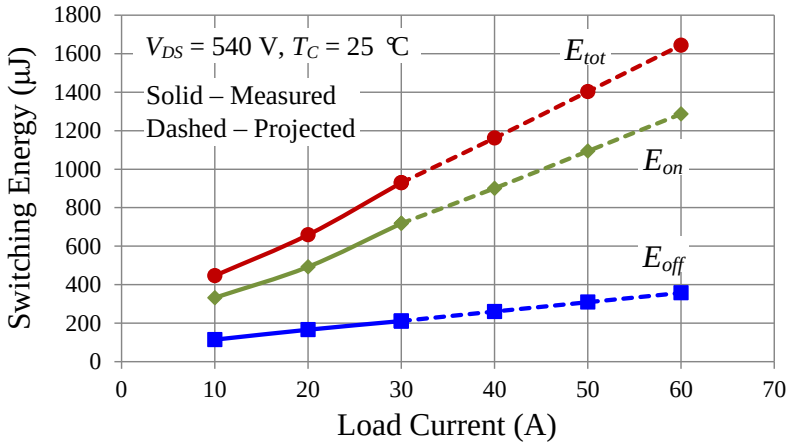
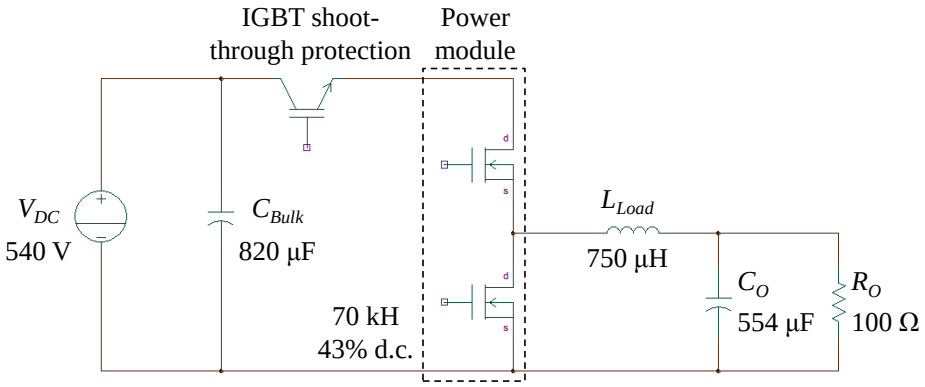


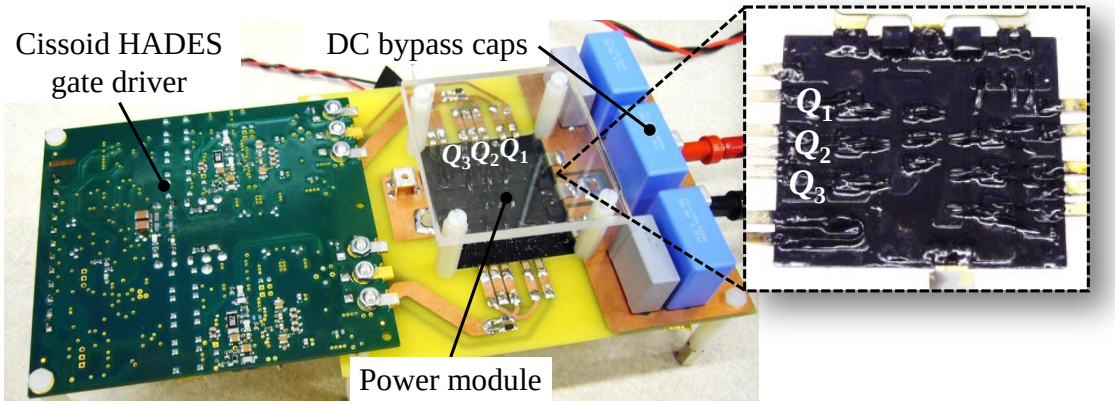
Figure 5-20. Switching energies of the 60 A module vs. load current

5.2.7 High-Temperature Continuous Operation Test

To evaluate the high-temperature operation of the designed package, the module is also operated continuously in buck topology. The test is conducted in the room environment, while the devices are heated by their own losses. Figure 5-21 shows the tester schematic with all circuit parameters, as well as the tester board. The power module is driven with an external R_G of 15 Ω to intentionally increase device losses. The module temperature is monitored using a FLIR infrared thermal camera. Compared to discrete temperature points measured by thermocouples, a thermal map would better reveal the temperature of each single device, as well as the temperature distribution among multiple chips. To enable this measurement, a special module is prepared: Instead of encapsulating the module with R-2188 in the final step of fabrication, a thin layer of high-temperature, black dielectric coating is sprayed onto the module to increase the surface emissivity. A small heatsink (Wakefield 518-95AB) is also attached to the bottom of the module to slow down the temperature rises for easier reading. No fan is used during the test, and the module is cooled with only natural convection.



(a)



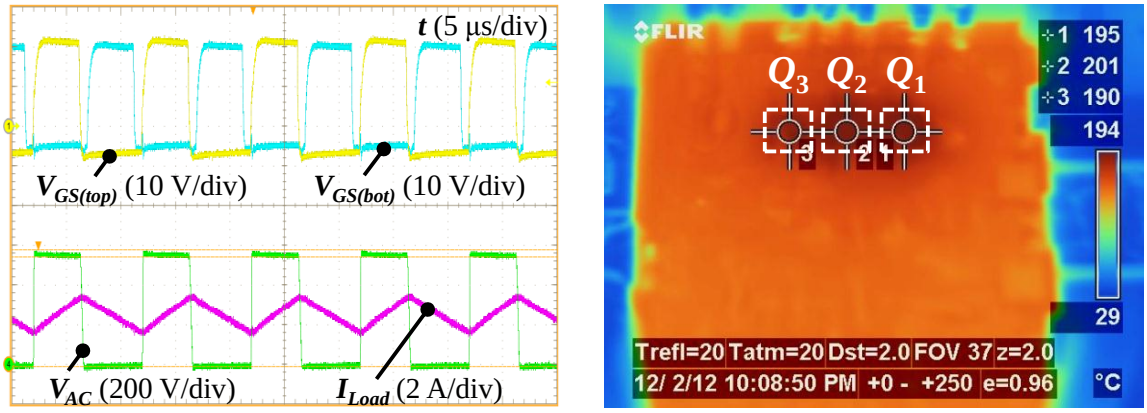
(b)

Figure 5-21. Circuit schematic (a) and tester board (b) of the continuous test

The cooling system is not specifically designed and optimized in this test since it is not the main purpose of the work. Under the conditions given by Figure 5-21 (a), the top switch temperature reaches only 145 ℃. To further push the device temperature, the DC bus voltage and switching frequency are increased to 560 V and 100 kHz respectively. Figure 5-22 (a) shows the test waveforms under this condition, and (b) shows the thermal map of the module when the device temperatures come very close to thermal equilibrium. As seen, all three top MOSFETs are above 190 ℃ and the middle device reaches 200 ℃ successfully. Note that these measurements only indicate the surface temperatures, and

the real junction temperatures will be even higher. No shoot-through failure happens during the test, and no thermal runaway is observed: The device temperatures still increase steadily even when approaching 200 ℃. This again verifies the characterization results in Chapter 2, and indicates good performances of the SiC MOSFET at high temperatures.

The temperature differences between Q_1, Q_2 and Q_3 are higher than expected, and may be decreased by improving the fabrication quality.



(a) **(b)**

Figure 5-22. High-temperature continuous test results of the 60 A module at 560 V and 100 kHz (a) Test waveforms, (b) module thermal map

5.3 Development of a High-Temperature, 1200 V, 120 A SiC Multi-Chip Phase-Leg Module

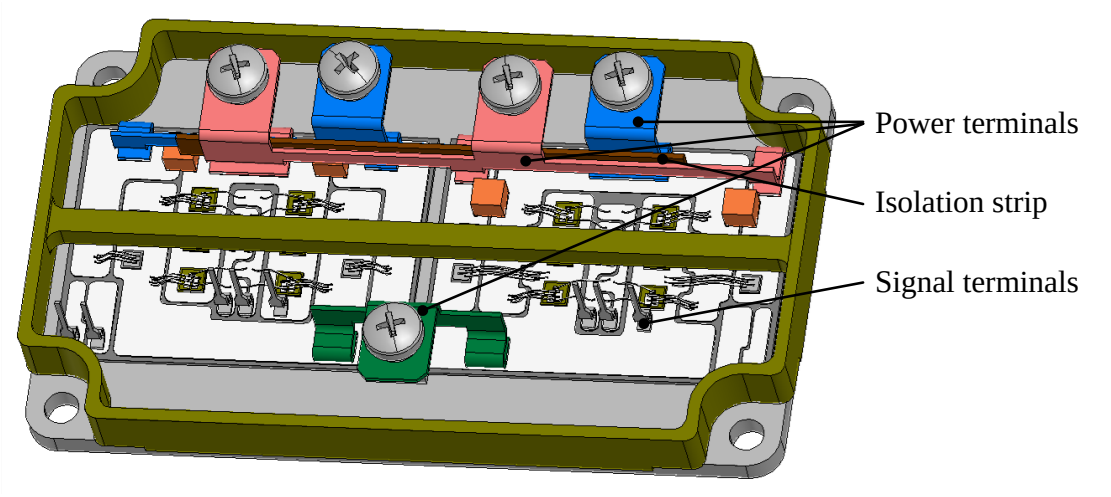
To meet the power requirement of the converter in Figure 5-1, each single phase-leg module should have a current rating of at least 100 A. With the design experience and knowledge obtained from the 60 A module, this section presents the development of a 1200 V, 120 A SiC phase-leg module. The module uses the same SiC MOSFET die as the 60 A version (Cree CPMF-1200-S080B), but with twice the number (i.e. six) to

double the current rating. Four 1200 V, 20 A SiC Schottky diodes (Cree CPW4-1200-S020B) are paralleled in each switch position to provide compatible reverse conduction capability. This module will serve as a drop-in replacement for the commercial SiC modules [11][12], while providing higher operating temperature (up to 200 °C) and higher switching frequency (due to low package parasitics) for the targeted converter.

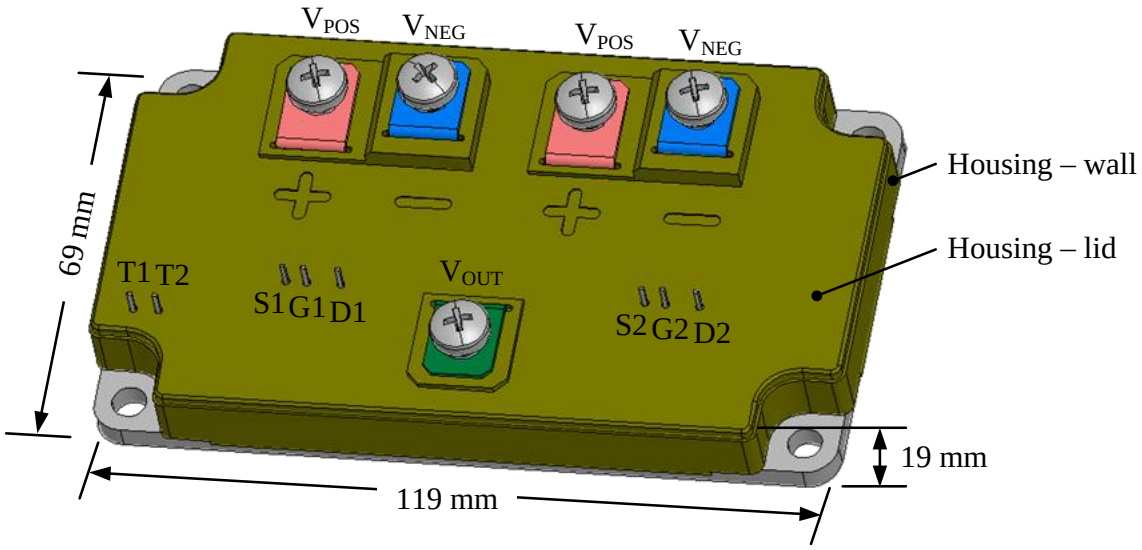
5.3.1 Material Selections

The 3D geometry model of the 120 A module is illustrated in Figure 5-23. Still built in wire-bond technology, the module has the same structure as Figure 5-2 and thus uses very similar packaging materials as the 60 A version. The different materials used for this particular module are summarized in Table 5-7.

In this design, the module's connection terminals are replaced by thicker copper sheets to reduce the interconnection resistances. All terminals are plated by nickel to protect copper from oxidization under high temperatures. DuPont's Nomex pressboard strip is inserted between the DC bus bars inside the module to provide electrical isolation. The module's housing wall and lid are machined from Quadrant T4203 high-temperature plastic blocks.



(a)



(b)

Figure 5-23. 3D geometry model of the 1200 V, 120 A SiC phase-leg module
(a) Module without lid, (b) module with lid

Table 5-7. Bill-of-Materials for the 1200 V, 120 A SiC MOSFET Power Module

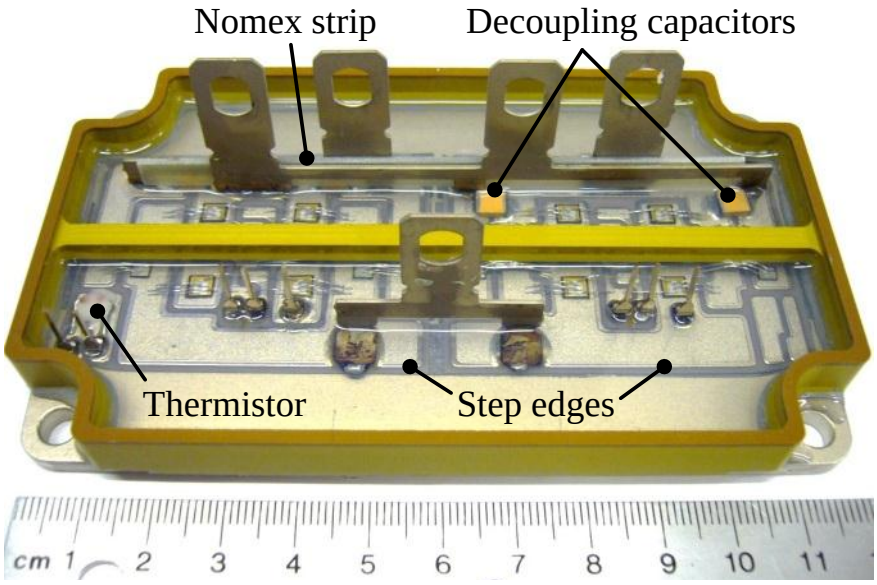
(If not specified, the same material as Table 5-1 is used.)

Part	Material	Specifications
Diode	Cree SiC Schottky diode	1200 V, 20 A Die size: 3.08 × 3.08 mm^2 Top: anode pad, Al metalized Bottom: cathode pad, Ag metalized
Power/signal terminals	Ni-plated Cu	31 mils in thickness
Isolation strip	DuPont Nomex pressboard	1.0 mm in thickness Dielectric strength: 16-27 kV/mm depending on test conditions Service temp. up to 300 ℃
Housing wall and lid	Quadrant Duratron T4203 polyamide-imide	Max. long-term service temp.: 260 °C
Die-substrate attachment	Sn5-Pb95 solder paste	Solidus/liquidus point: 308/312 ℃
Terminal-substrate attachment	Sn89-Sb10.5-Cu0.5 solder paste	Solidus/liquidus point: 242/263 ℃ Thermal conductivity: 42 W/m/K
Substrate-baseplate attachment	Epo-Tek EK2000 silver epoxy	Max. continuous operating temp.: 200 ℃ Thermal conductivity: 26.3 W/m/K
Housing-baseplate attachment	Epo-Tek 353ND epoxy adhesive	Max. continuous operating temp.: 250 ℃

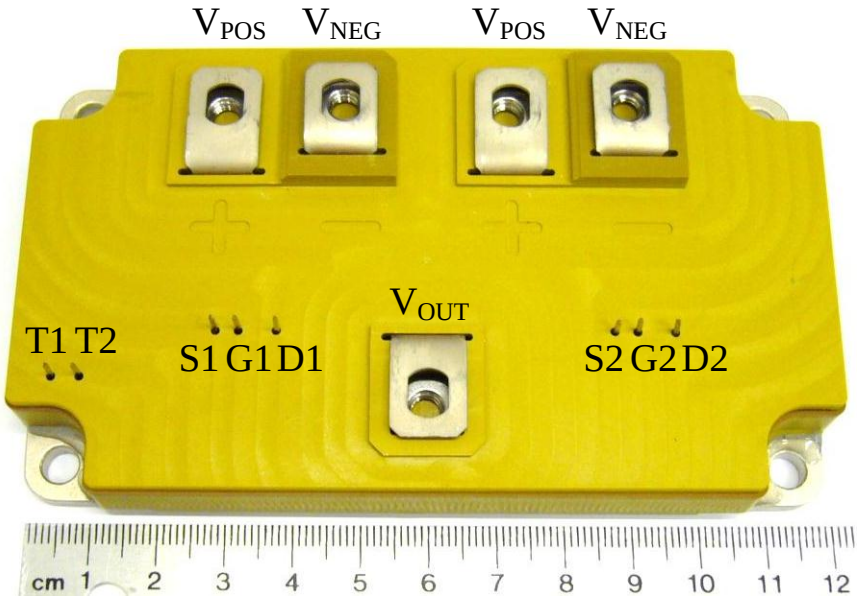
To ease lab prototyping and improve module yield, different bonding materials are used compared to the 60 A module. Instead of Sn5-Pb95 preform, the corresponding solder paste is used to achieve the die attachment on a belt furnace (Sikama Falcon 5x4 belt furnace). This avoids the more complicated vacuum reflow process and saves the effort of machining graphite boat fixtures. After die attachment and wire bonding, the high-temperature lead-free solder Sn89-Sb10.5-Cu0.5, whose melting point is roughly 50 °C lower than Sn5-Pb95, is used to attach all the terminals to the substrates in a second round of belt reflow without affecting the device attachment. The substrates and housing wall are then bonded to the AlSiC baseplate with silver epoxy and epoxy adhesive respectively. Note that the silver epoxy is chosen over solders to simplify the substrate-

baseplate attachment process. Since this bonding layer is in the path of heat dissipation, the thermal conductivity of the selected material is among the highest of its kind. However, for better thermal performance, solder materials should be used instead, such as Sn89-Sb10.5-Cu0.5. After the above steps, the isolation strip is inserted between the DC bus bars, and then the module is potted with NuSil R-2188 silicone. The housing lid is finally attached to the module with Epo-Tek 353ND epoxy.

The fabricated phase-leg module without lid is shown in Figure 5-24 (a). Different module elements discussed above can be clearly identified from the picture. A thermistor is also seen on the bottom left corner of the module to monitor the substrate temperature. The step edges on the DBC substrates can be clearly seen as well. Figure 5-24 (b) displays the module in its final form.



(a)



(b)

Figure 5-24. Fabricated 1200 V, 120 A SiC MOSFET phase-leg module
(a) Module without lid, (b) module with lid

5.3.2 Layout Design and Comparison with Commercial Module

The substrate layouts of the 120 A module are illustrated in Figure 5-25. As seen, the semiconductor devices are distributed on two pieces of DBC substrates with identical dimensions. Compared to a single large substrate, using two smaller substrates effectively reduces the warpage and increases the thermal cycling lifetime of each substrate [28]. Like the 60 A module, the main switching loops of the 120 A version are also optimized by placing switch-pair devices on the same substrate. For example, on the left substrate the top MOSFETs and bottom diodes can be found. The MOSFET die spacing is kept the same as the 60 A module. The copper traces on each substrate are also designed in a symmetrical and forked pattern to achieve better current balancing among paralleled devices than the linear arrangement [19][45]. Two 1 kV, 22 nF high-temperature ceramic capacitors are also soldered together with the devices on each substrate to provide sufficient decoupling effect. In the middle of each substrate are the gate and source traces for Kelvin-type gate drive connection. Note that additional drain pins (D1 and D2) are also provided in the module for the HADES driver to easily access the MOSFETs' drain voltages and achieve over-current protection.

The DC bus bars inside the module are also designed in a laminated structure to reduce the stray inductance. As seen in Figure 5-23 (a), two sets of DC terminal tabs are designed so that each switch pair in the phase-leg can access the converter's DC bus via a shorter path. One can also use only the middle two tabs, which are standard one inch apart, for simpler connection like the other commercial modules.

The layout design of this 1200 V, 120 A module (also referred to as "CPES module" thereafter) is compared to a commercial 1200 V, 100 A SiC MOSFET phase-leg

module in terms of the package parasitics [12]. Figure 5-26 shows the external appearance and internal layout of the commercial module. The two modules in comparison are slightly different in the current rating and number/type of devices used inside, which is summarized in Table 5-8.

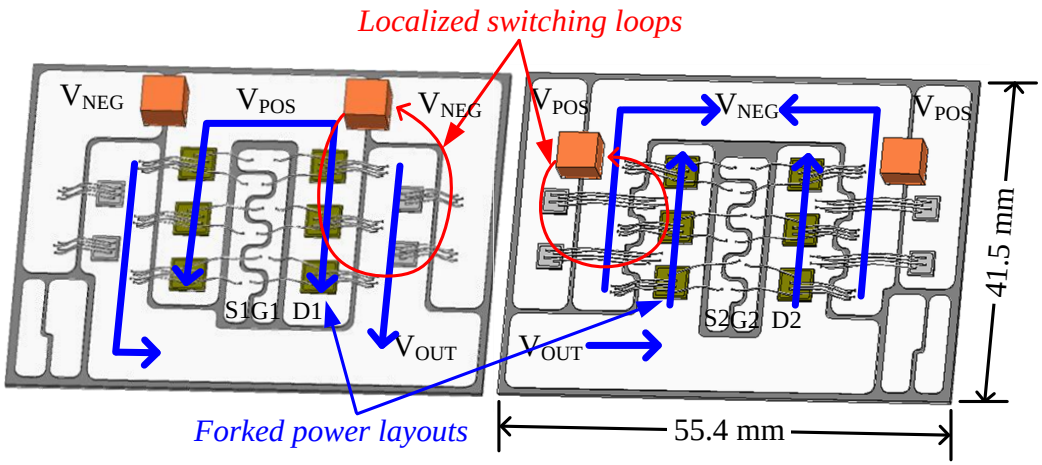


Figure 5-25. Substrate layout design of the 120 A module

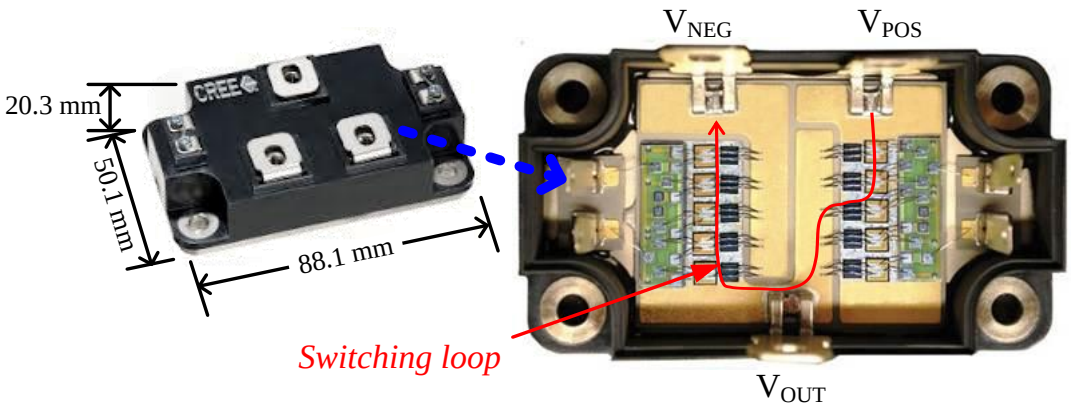


Figure 5-26. Internal layout of a commercial 1200 V, 100 A SiC MOSFET phase-leg module (The pictures are obtained from the Internet)

Table 5-8. Comparison of CPES and Commercial Module Specifications

	CPES module	Commercial module
Ratings	1200 V, 120 A	1200 V, 100 A
Switch	Cree CPMF-1200-S080B 6 in parallel in each switch position	Cree CPMF-1200-S080B* 5 in parallel in each switch position
Diode	Cree CPW4-1200-S020B 4 in parallel in each switch position	Cree CPW2-1200-S010B* 5 in parallel in each switch position
Total junction capacitance (MOSFETs + diodes) at 540 V	726 + 300 = 1026 pF	605 + 275 = 880 pF

* Inferred from the module datasheet

As seen in Figure 5-26, the commercial module adopts the conventional substrate layout and separate DC terminals. According to the previous analysis, this would lead to higher switching loop inductances for the switch pairs. To verify that, both modules are modeled in Ansoft Q3D to extract the package parasitics. The simulated switching loop inductances associated with the bottom MOSFETs are compared in Figure 5-27. The top-MOSFET-associated stray inductances have very similar results.

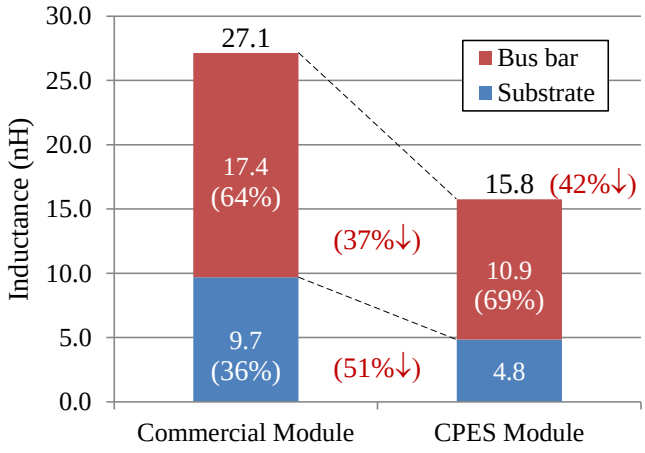


Figure 5-27. Simulated module parasitics breakdown

By using the improved layout design proposed in this work, the substrate-associated loop inductance is seen to drop from 9.7 nH to only 4.8 nH, a more than 50% reduction. The laminated and four-tab design of the DC bus bars again achieves 37% less stray inductance compared to the commercial module. Combined, the total switching loop inductance of the CPES module is only 15.8 nH, 42% less than that of the commercial module.

It is also important to note from Figure 5-27 that, in both modules, the DC-terminal-related stray inductances are actually a more dominant part in the module's overall parasitics. This indicates that the low-inductance design of DC terminals is to some extend more critical for the module, and that placing decoupling capacitors on the substrates will be very effective in reducing the parasitic ringing of the switches – the MOSFET's over-voltage reduction will be more than 42% because of these capacitors.

5.3.3 Switching Performance and Comparison with Commercial Module

The double-pulse switching tests are carried out on both modules to verify the proposed design of the CPES module. During the test, the two modules are mounted on two different tester PCBs which carry the DC bus bypass capacitors and provide connection interfaces to the modules and the HADES gate driver, as illustrated in Figure 5-28. As explained in Chapter 3, since the DC bus impedances also affect the parasitic ringing of the modules, it is critical to design the DC bus structures of the two tester PCBs to be as similar as possible for fair comparison of the modules' switching performances.

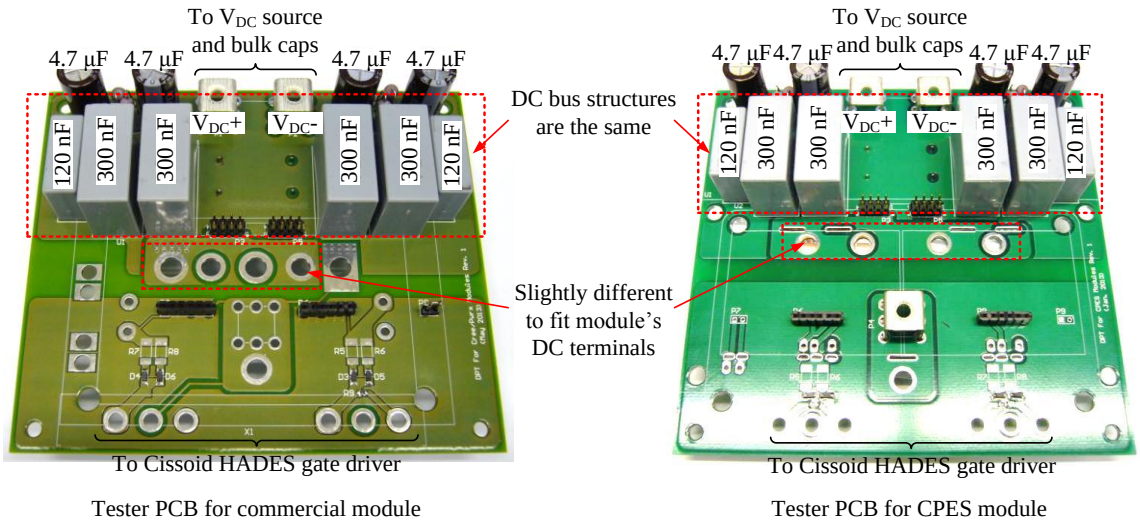
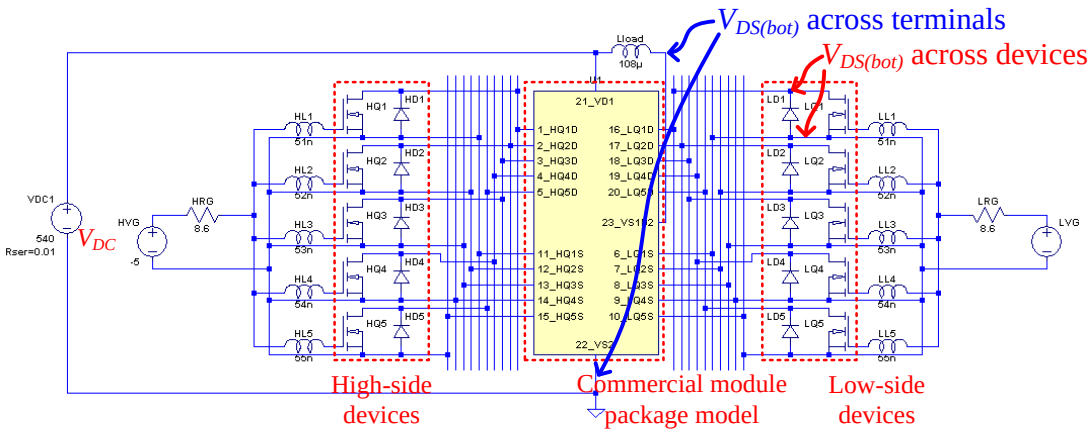
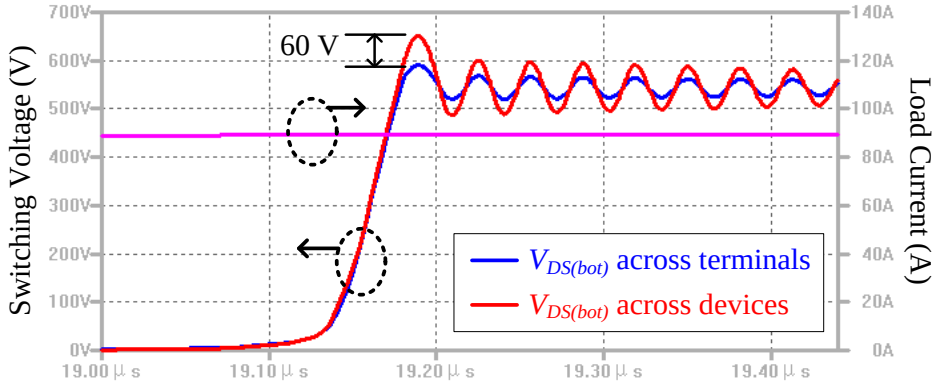


Figure 5-28. Double-pulse tester PCBs for the commercial and CPES modules

When evaluating the MOSFET's turn-off over-voltage, an often overlooked fact is that the voltage measured across the module's terminals (e.g. V_{OUT}-V_{NEG}) does not reflect the real voltage stress seen by the device. This is because the voltage drop across the module's internal stray inductance is included in this measurement, making the observed over-voltage less than the real peak voltage across the MOSFET. Depending on the switching speed (i.e. the *di*/*dt*) and the module's parasitics, the voltage difference can be non-negligible. Since only terminal voltages can be measured experimentally on the commercial module in Figure 5-26, the modeling and simulation approach described in Section 5.2.5 is adopted to verify the above statement. Shown in Figure 5-29 (a) is the simulation circuit combining device models with the commercial module's package model extracted from Ansoft Q3D, while in (b) the simulated switching voltages are presented. As seen, when the module turns off 540 V and 90 A with R_G = 8.6 Ω, the simulated device over-voltage is 60 V higher than that across the module's terminals.



(a)



(b)

Figure 5-29. Simulated switching voltages across terminals and devices of the commercial module (a) Simulation circuit, (b) simulated switching waveforms

For the CPES module, nevertheless, the D1-S1 and D2-S2 pins will provide more accurate MOSFET V_{DS} measurements, since they are much closer to the devices than the power terminals. Likewise, if measuring the bottom MOSFET's V_{DS} across both terminals (V_{OUT}-V_{NEG}) and devices (D2-S2) when the module (decoupling capacitors excluded) turns off 540 V, 90 A with R_G = 7.2 Ω, the peak voltage across the devices will be 40 V higher, as illustrated in Figure 5-30.

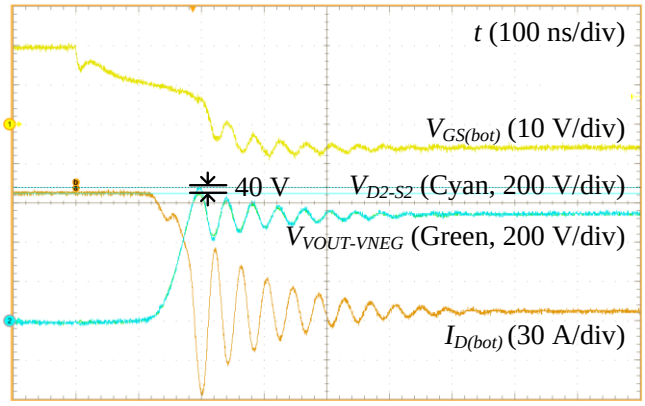
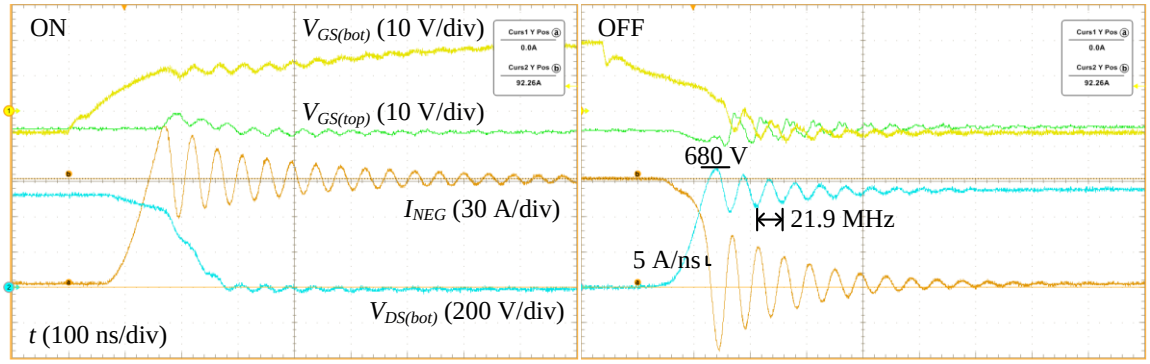


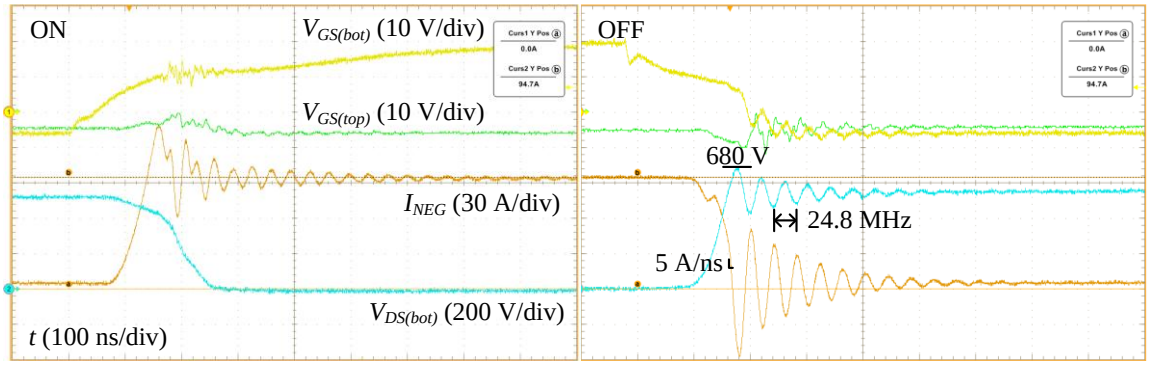
Figure 5-30. Experimental switching voltages across terminals and devices of the CPES module

In the following study, three modules will be tested and compared, i.e. the commercial module in Figure 5-26, the CPES module without embedded capacitors, and the CPES module with all embedded capacitors. The V_{DS} measurements on the CPES modules will be performed across D1-S1 and D2-S2 to evaluate device over-voltages more accurately. V_{DS} of the commercial module, however, can only be measured from the power terminals. For fair comparison, the real device over-voltages will be estimated based on the measured di/dt and the simulated internal stray inductances of the commercial module.

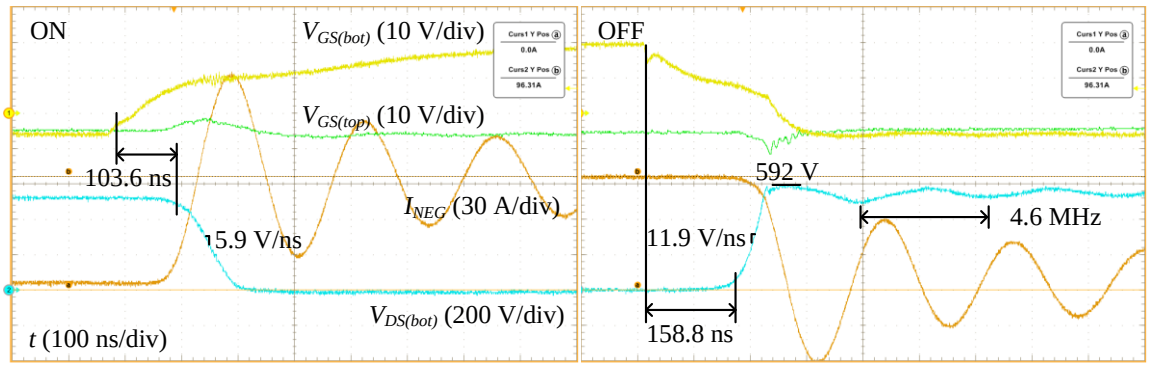
Figure 5-31 compares the switching waveforms of the three modules at 540 V and 90 A. All modules are driven by Cissoid's HADES gate driver, which has an internal gate resistance of 5 Ω. The external gate resistances are tuned separately for the commercial and CPES modules to achieve similar di/dt at both turn-on and turn-off, since these two modules have different number of paralleled MOSFETs. As seen in Figure 5-31 (a) and (b), the commercial module exhibits a lower ringing frequency at turn-off than the CPES one (21.9 MHz vs. 24.8 MHz). With its lower junction capacitance according to Table 5-8, it can be inferred that the switching loop inductance is higher for the commercial



(a)



(b)



(c)

Figure 5-31. Comparison of switching waveforms of three modules at 540 V, 90 A
(a) Commercial module, external $R_{G(on)}$ = 6.8 Ω and $R_{G(off)}$ = 3.6 Ω,
(b) CPES module without embedded capacitors, external $R_{G(on)}$ = 4.6 Ω and $R_{G(off)}$ = 2.2 Ω, and
(c) CPES module with embedded capacitors, external $R_{G(on)}$ = 4.6 Ω and $R_{G(off)}$ = 2.2 Ω

module. Using Eq. (3-5), the switching loop inductance is estimated to be 60 nH for the commercial module, and only 40.1 nH for the CPES module. Out of the total 19.9 nH reduction, 11.3 nH results from the optimized internal layout of the CPES module according to Figure 5-27, while the rest 8.6 nH comes from the different tester board layouts to fit the two modules' terminals.

The measured turn-off over-voltages in Figure 5-31 (a) and (b), however, are both 680 V under the same *di*/*dt* of 5 A/ns. As explained above, the V_{DS} measurement on the commercial module underestimates the real voltage stress of the MOSFETs. Therefore, the device over-voltages are estimated for the commercial module, and then compared to those measured on the CPES module, as shown in Figure 5-32. Even without embedded decoupling capacitors, the CPES module already exhibits roughly 20% lower V_{DS} overshoot than that of the commercial module, thanks to the improved layout design.

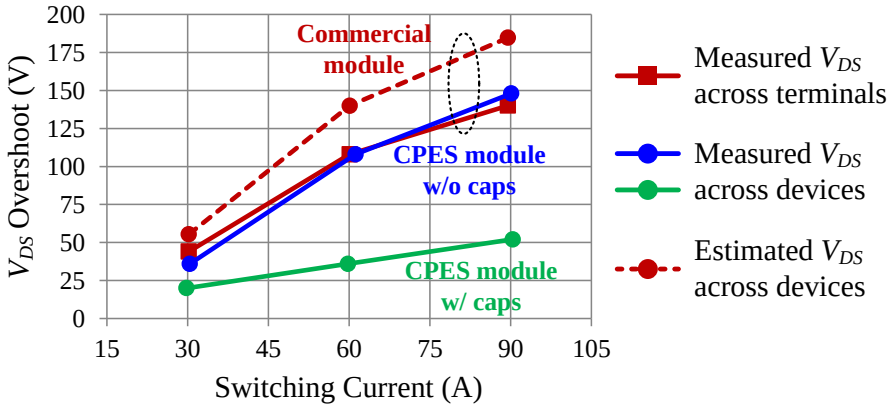


Figure 5-32. Comparison of V_{DS} overshoots of three modules under the switching conditions in Figure 5-31

The device over-voltages are further reduced significantly when the decoupling capacitors are embedded inside the module. As seen in Figure 5-31 (c), the MOSFET peak V_{DS} decreases to only 592 V under the same switching speed. A more complete

comparison under various loads is shown in Figure 5-32, where the V_{DS} overshoots are found to be only 30% of those of the commercial module.

In Figure 5-31 (c), a lower ringing frequency of 4.6 MHz can be observed due to the resonance between the DC bus bar inductance of the module, and the bypass capacitance on the tester board. If necessary, this ringing can be further suppressed by simply adding more capacitance externally. Moreover, the gate voltage waveforms are also seen to be much cleaner thanks to the reduced ringing from the power side. Also, like the 60 A module, the terminal current I_{NEG} no longer reflects the device current when the embedded capacitors exist. Since these capacitors do not affect the switching speed, the switching energies of the CPES module with embedded capacitors can be well approximated by evaluating the module without capacitors.

Less parasitic ringing and lower device over-voltage allow faster switching of the CPES module with capacitors. Figure 5-33 shows the switching waveforms of the module driven with 0 Ω external R_G. Compared to Figure 5-31, higher V_{DS} slew rates and shorter switching delay times are achieved without increasing the MOSFET's voltage stress. As a result, the V_{DS} overshoots of the CPES module still remain around 30% of those of the commercial module, while the switching energies can be cut by 50% due to the faster switching speed, which are shown in Figure 5-34.

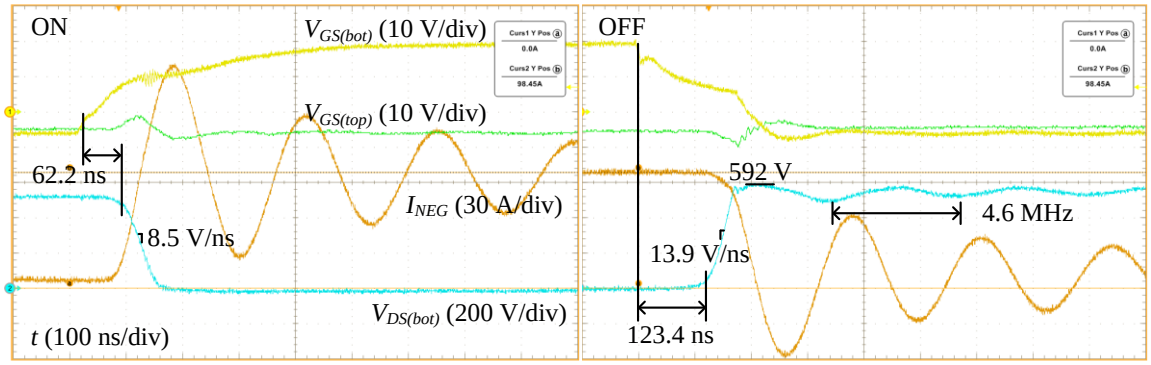
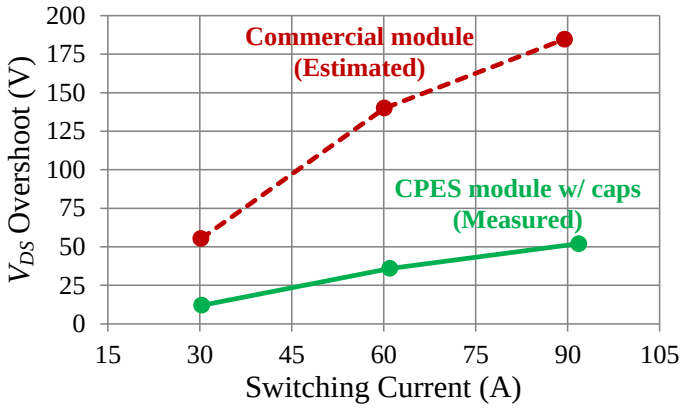
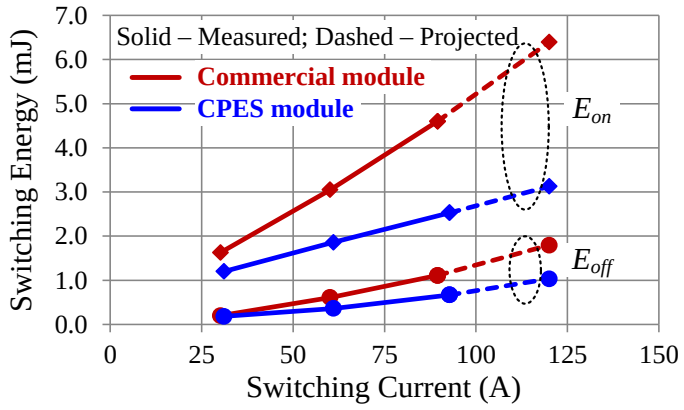


Figure 5-33. Switching waveforms of the CPES module with embedded capacitors at 540 V, 90 A, and external $R_{G(on)}$ = $R_{G(off)}$ = 0 Ω



(a)



(b)

Figure 5-34. Comparison of (a) V_{DS} overshoots and (b) switching energies of the commercial and CPES modules at 540 V

Commercial module is driven with external $R_{G(on)}$ = 6.8 Ω and $R_{G(off)}$ = 3.6 Ω;

CPES module is driven with external $R_{G(on)}$ = $R_{G(off)}$ = 0 Ω

5.3.4 Module Characterizations

The fabricated 120 A module is fully characterized under various temperatures up to 200 °C. Figure 5-35 shows the temperature-dependent static characteristics. The module basically exhibits linearly scaled-up *I-V* curves and the same temperature behaviors compared to those of the single SiC MOSFET presented in Chapter 2.

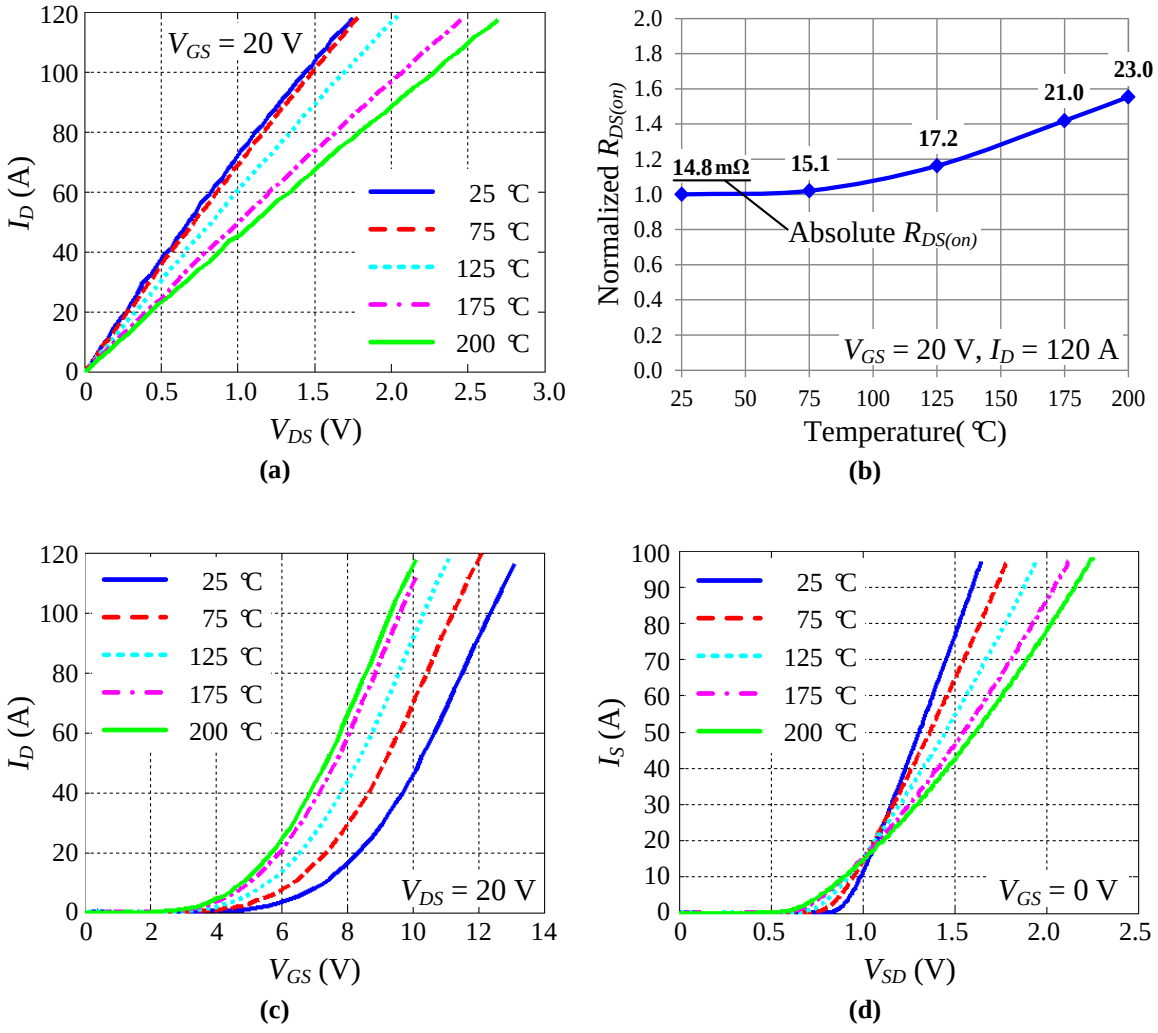
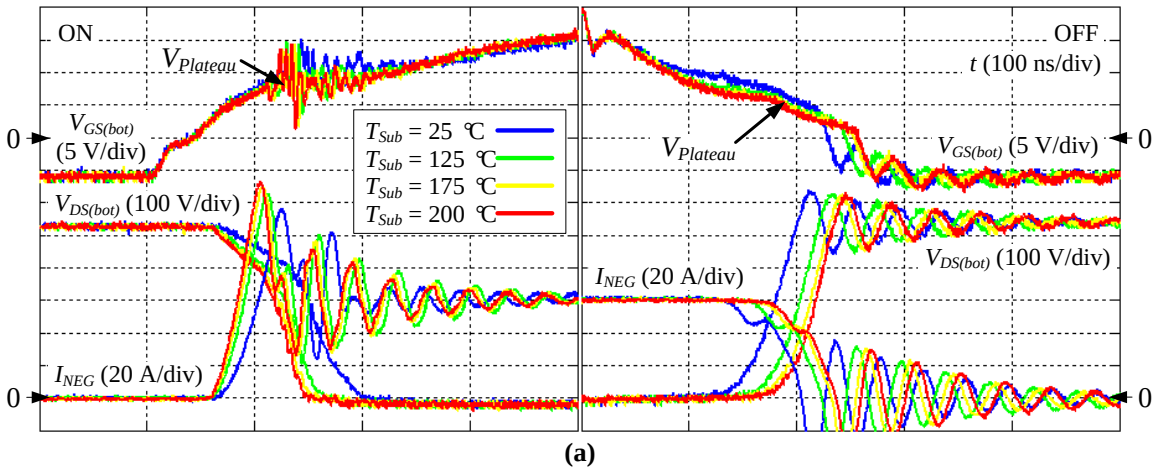


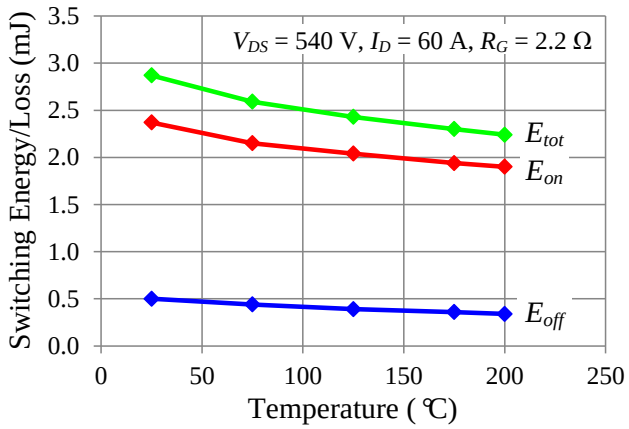
Figure 5-35. Static characteristics of the 120 A module

(a) Forward, (b) $R_{DS(on)}$, (c) transfer, (d) reverse

The switching characteristics are measured from the module without embedded capacitors, so that the switching energies can be evaluated later. The module's substrate temperature is measured with the internal thermistor, and is regulated by a hotplate. Figure 5-36 (a) shows the temperature-dependent switching waveforms of the module at 540 V and 60 A, driven by the HADES driver with an external R_G of 2.2 Ω. Similar to the single MOSFET case, the gate plateau voltage decreases with the increasing temperature, resulting in higher dv/dt and di/dt at turn-on, and consequently, a decreasing E_{on}, as seen in Figure 5-36 (b). At turn-off, nevertheless, the V_{DS} slew rate slightly increases under lower $V_{Plateau}$, causing E_{off} to decrease with the increasing temperature as well, which is contrary to the trend shown in Chapter 2. This phenomenon is found to be related with the temperature dependence of the gate driver's de-sat protection circuit, which is connected to the drain terminal of the switch and modifies its V_{DS} waveform. The same temperature behavior can be observed on the commercial module in Figure 5-26 when it is also driven by HADES, although the module's datasheet shows a contrary E_{off} trend which agrees with the result in Chapter 2.



(a)



(b)

Figure 5-36. Switching characteristics of the 120 A module without embedded capacitors (a) Switching waveforms, (b) switching energies

5.4 Conclusions

This chapter firstly presents the design and test results of a 1200 V, 60 A SiC MOSFET module for high-temperature and high-frequency operations. Packaging materials that can work reliably over 200 ℃ are extensively surveyed and carefully selected. Methods to improve the thermal cycling reliability of DBC substrates are also briefly discussed. The improved substrate layout based on the "switch pair" concept is then adopted over the conventional design to achieve smaller package parasitics. It is

further pointed out how the parasitic effect related to the module's power terminals can be mitigated by embedding decoupling capacitors directly inside the module, which is verified through both simulation and experiments. After that, the continuous power test successfully demonstrates the high-temperature operation of the module.

Following the same design approach, a 1200 V, 120 A SiC MOSFET phase-leg module is then developed in this chapter, which has comparable power ratings to the commercial products. Besides the higher operating temperature enabled by the selected packaging materials, it is also proved from detailed comparisons that the 120 A module developed in this work allows SiC MOSFETs to be switched twice faster, and meanwhile keeps device over-voltages 70% lower than the state-of-the-art commercial module, thanks to the optimized module layout and the embedded decoupling capacitors. The development of such a module will be a promising solution to the high-temperature and high-frequency power converters in future transportation applications.

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Chapter 6 Development of a Novel Hybrid Packaging Structure for SiC Power Modules

6.1 Introduction

As of today, the wire-bond packaging is still the most widely adopted technology for high power electronics modules due to its maturity, reliability, and simplicity of manufacturing, etc. However, the wire-bond modules also suffer from the problems such as low power density and high package parasitics, which have become a bottleneck for the emerging SiC unipolar switches with much faster switching speed than the traditional Si IGBTs. To address these issues, various planar packaging technologies have been proposed to eliminate the bonding wires, such as the metal post interconnect parallel plate [1]-[3], the dimple-array interconnect [4][5], the flip-chip on flex [6]-[11], the embedded power [12][13], and the power overlay [14]-[16], etc. The planar structures bring the benefits of smaller module footprint, lower parasitic impedances, and the possibility of double-sided cooling for the semiconductor devices. Nevertheless, almost all of these structures require the top electrode pads of the semiconductor die to be solderable. Since high-power devices are usually metalized by aluminum on their top pads to work with aluminum bonding wires, double-sided solderability is generally not available without

special treatments to these devices, such as depositing solderable metal (e.g. silver [17]) via sputtering or electroplating, etc. This additional step usually greatly complicates the fabrication of these planar modules, and the reliability of the top-side interconnection is largely dependent on the deposition quality, which in many cases is still unclear.

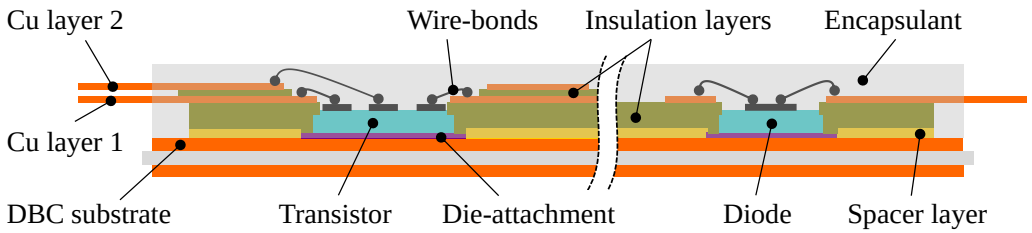
In this chapter, a novel hybrid packaging technology is developed to provide a compromise between the wire-bond and the planar structures. As a combination of the two technologies, the hybrid power module keeps the 3-dimentional (3D) structure of a planar module to achieve the same footprint and volume density, but accomplishes the device top-side interconnections through wire-bonding to simplify fabrication and improve reliability. With this structure, no double-sided solderability is required for the power devices, and the reliability of the top-side interconnection is provided by the wire-bonding, which has been studied for a long time.

6.2 Development of a High-Temperature SiC Rectifier Module in the Hybrid Structure

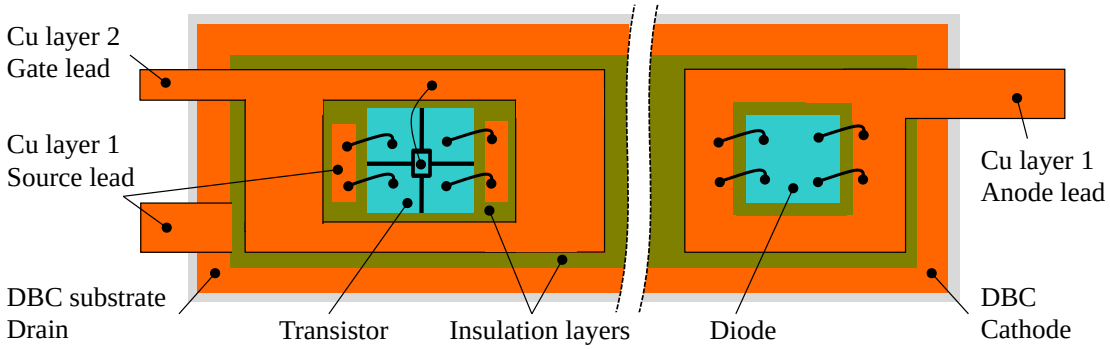
6.2.1 Hybrid Structure, Material Selection, and Fabrication Process

The cross-sectional and top views of the proposed hybrid structure are illustrated in Figure 6-1. As seen, a spacer layer is firstly attached to the DBC substrate as the solder mask and the die-attachment fixture. After the dice are attached to the substrate through either soldering or sintering, an additional copper layer is bonded to the DBC using an insulated polyimide adhesive. Windows are cut on the copper layer to expose the top sides of the devices, so that they can be accessed by bonding wires later. For the transistor with two electrode pads on the top surface (gate and source), another two layers

of polyimide and copper need to be attached in the same way. After wire-bonding, the entire module is then encapsulated in a silicone material.



(a)



(b)

Figure 6-1. Proposed hybrid structure for the transistor and the diode
(a) Cross-sectional view, (b) top view

For the hybrid module to work in high-temperature environments, packaging materials are carefully selected and are summarized in Table 6-1. The selection considerations regarding the substrate, bonding wire, and encapsulant are similar to Chapter 5 and will not be repeated here. Note that the DBC surface is electroplated by silver in this work, so that the devices can be sintered onto the substrate using nano-Ag paste [18][19]. The nano-Ag paste is a die-attachment material which will form a pure silver interface between the die and substrate through a sintering process. Unlike soldering where the solder alloy needs to be melt before forming the bond, the nano-sized

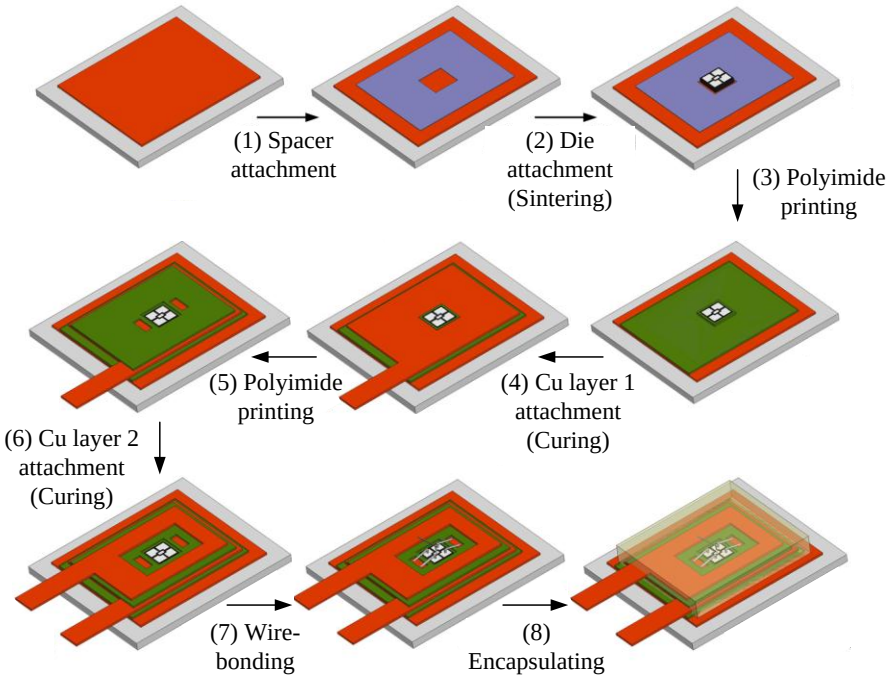
silver particles in the nano-Ag paste are consolidated into a strong and uniform bonding layer by sintering up to only 280 ℃. After sintering, the working temperature of this die-attachment interface is just limited by the melting temperature of silver, i.e. 962 ℃. Moreover, the silver bonding also provides much higher electrical and thermal conductivities than the conventional Pb-Sn or Au-Sn based solders.

Table 6-1. Bill-of-Materials for the High-Temperature, Hybrid SiC Power Module

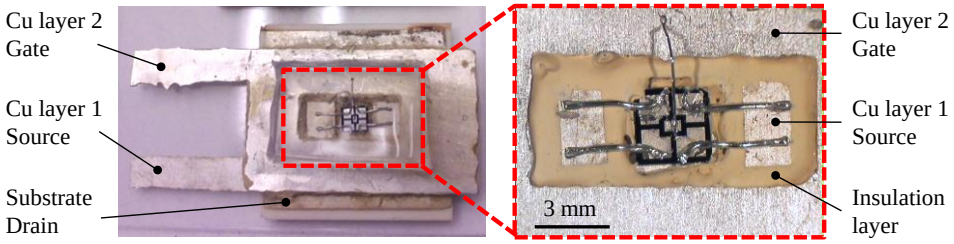
Part	Material	Specifications
Switch	SiCED SiC JFET	1200 V, 5 A Die dimension: 3.0 × 3.0 × 0.38 mm^3 Top: gate & source pads, Al metalized Bottom: drain pad, Ag metalized
Diode	SiCED SiC Schottky diode	1200 V, 5 A Die size: 2.7 × 2.7 × 0.38 mm^3 Top: anode pad, Al metalized Bottom: cathode pad, Ag metalized
Substrate	Curamik AlN DBC	Cu/AlN/Cu thicknesses: 8/25/8 mils Ag electroplated
Spacer	DuPont Kapton tape	Thickness: 2 mils
Die-attachment	Nano-Ag paste	Processing temperature up to 280 ℃
Insulation layer	Epo-Tek 600 polyimide	-
Leadframe	Cu	10 mils, Ag plated
Bonding wire	Al	Dia.: 5 and 10 mils
Encapsulant	NuSil R-2188 silicone	-

A single-chip SiC JFET module is firstly built in this structure to demonstrate the fabrication process, which is illustrated in Figure 6-2 (a). As seen, a layer of Kapton tape is firstly attached to the DBC substrate as the spacer layer, where a window of the die size is cut so that the nano-Ag paste can be stencil-printed. After the die attachment, Epo-Tek 600 polyimide adhesive is printed onto the spacer as the insulation layer. The first layer of copper sheet is then bonded to the substrate by curing the polyimide. The same

printing-and-curing process is repeated for the second copper layer. After that, the device top pads are wire-bonded to the corresponding copper layers. The entire module is finally encapsulated by NuSil R-2188 silicone. Figure 6-2 (b) shows the fabricated prototype module highlighting the 3D structure of the device top-side interconnection. As seen, very short bonding wires are used to connect the device electrodes to the copper layers, which effectively reduces the parasitic impedances from these wires.



(a)



(b)

Figure 6-2. Single-chip SiC JFET module in the hybrid structure
(a) Fabrication process, (b) fabricated prototype module

The complete fabrication process contains one sintering step, two curing steps, and one encapsulating step, which require heating of the module. In Table 6-2, this fabrication process is compared to that of the planar module reported in [17]. For the latter structure, a zincating and electroless-plating step is firstly necessary to make the device top pads solderable. After that, three sintering steps are required to accomplish the device interconnections. If these steps were done with the more popular soldering technique, three different solder alloys with melting temperatures at least 40 ℃ apart would be needed to achieve three steps of soldering [20]. For a high-temperature module with the device operating up to 250 ℃, this may result in a very high processing temperature even over 400 ℃. In contrast, for the hybrid structure, the nano-Ag paste can be easily substituted by conventional solders since only one soldering step would be needed. This makes the selection of die-attachment material much more flexible.

Table 6-2. Comparison of Fabrication Process between Hybrid and Planar Modules

Main processing step	Hybrid structure	Planar structure [17]
1	*Die-attachment (sintering)*	Die zincating and electroless plating with Ag
2	*Polyimide curing for Cu layer 1*	*Die-attachment (sintering)*
3	*Polyimide curing for Cu layer 2*	*Polyimide curing for Cu layer 1*
4	Wire-bonding	*Source pad attachment to Cu layer 1 (sintering)*
5	*Encapsulating*	*Polyimide curing for Cu layer 2*
6		*Gate pad attachment to Cu layer 2 (sintering)*

Italic – Indicates a step that requires heating of the module

The static characteristics of the SiC JFET are measured before and after packaging. No visible change is observed.

6.2.2 Development of the SiC Rectifier Module in the Hybrid Structure

The proposed hybrid packaging technology is implemented on a three-phase, single-switch rectifier module based on SiC JFET and SiC Schottky diode, as seen in Figure 6-3. D_1 through D_6 form the three-phase rectifier stage, followed by a boost stage consisting of Q and D_7 [21].

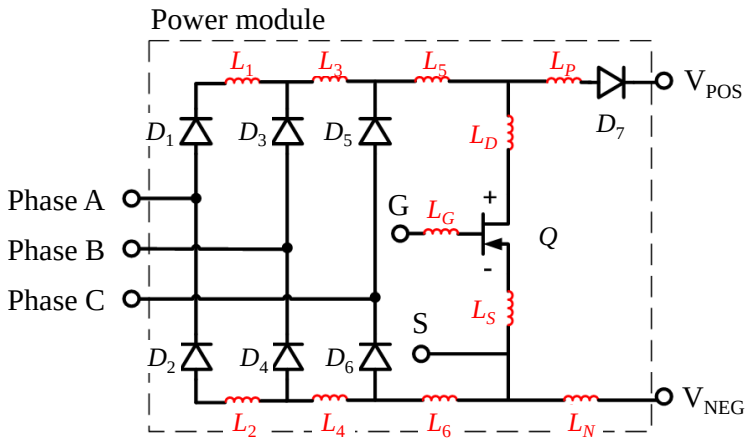


Figure 6-3. Topology of a three-phase, single-switch rectifier

Figure 6-4 (a) to (c) compare three different structures, i.e. wire-bond, hybrid, and planar, that can be used to package the module of Figure 6-3. As seen, the hybrid and planar modules can be designed with the same footprint thanks to their 3D structure, while the wire-bond module needs roughly 40% larger area to provide enough trace widths and wire-bonding sites on the 2D surface of the DBC substrate.

The stray inductances of the three structures are also extracted with Ansoft Q3D. Figure 6-4 (d) compares the most critical boost-stage stray inductances of these designs, i.e. the main switching loop inductance ($L_P + L_D + L_S + L_N$), the gate loop inductance ($L_G + L_S$), as well as the common source inductance L_S. Since the hybrid module has the same footprint, its main loop inductance is also very close to that of the planar structure, and is

35% less than the wire-bond module. The shorter bonding wires in the hybrid structure also cut the gate loop inductance in half compared to the wire-bond package, and meanwhile lead to a smaller common source inductance.

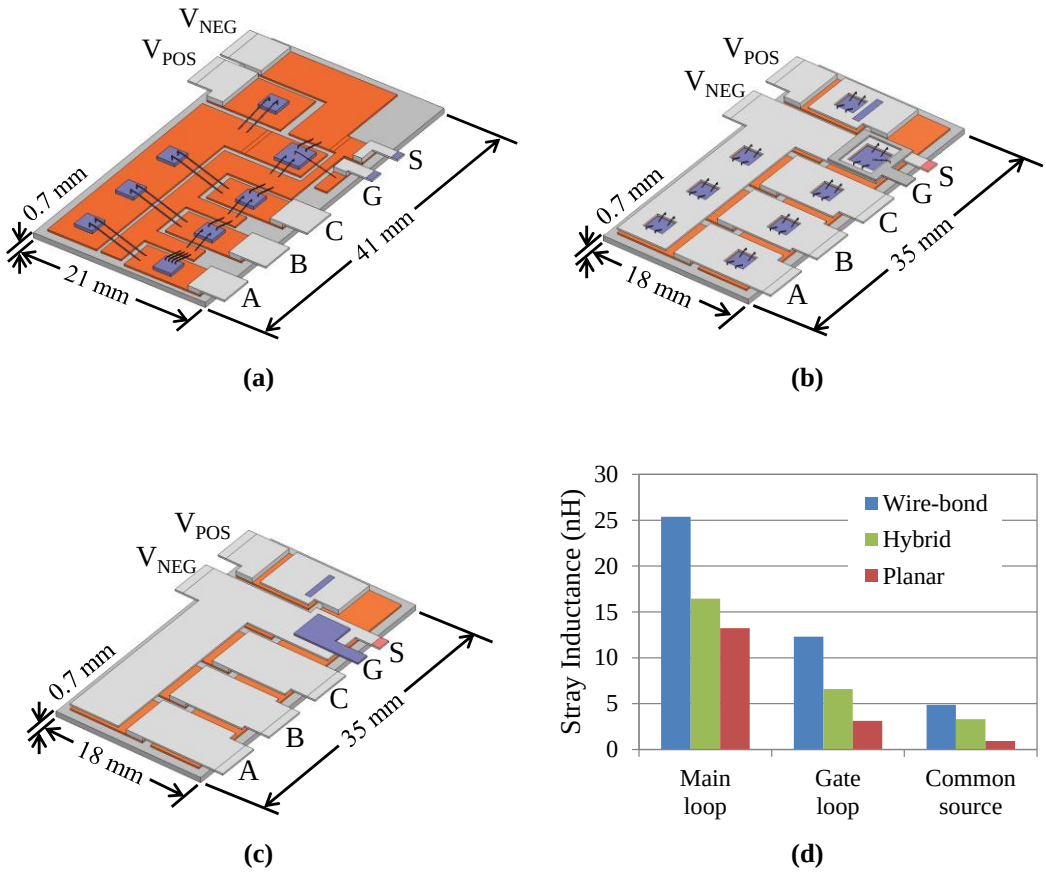


Figure 6-4. Comparison of different structures for the module of Figure 6-3
(a) Wire-bond, (b) hybrid, (c) planar, (d) comparison of stray inductances

The smaller package parasitics translate to better switching performances of the SiC switch. Figure 6-5 compares the simulated turn-off waveforms of the JFET at 270 V, 12 A, in wire-bond and hybrid modules. Since the hybrid structure presents a smaller common source inductance, the *di*/*dt* of the device is faster than in the wire-bond module under the same driving conditions, achieving lower turn-off energy (76.7 μJ vs. 88.4 μJ in

this case). Moreover, thanks to its smaller switching loop inductance, the hybrid module also reduces the V_{DS} spike from 305 V to 290 V, even with the presence of higher di/dt.

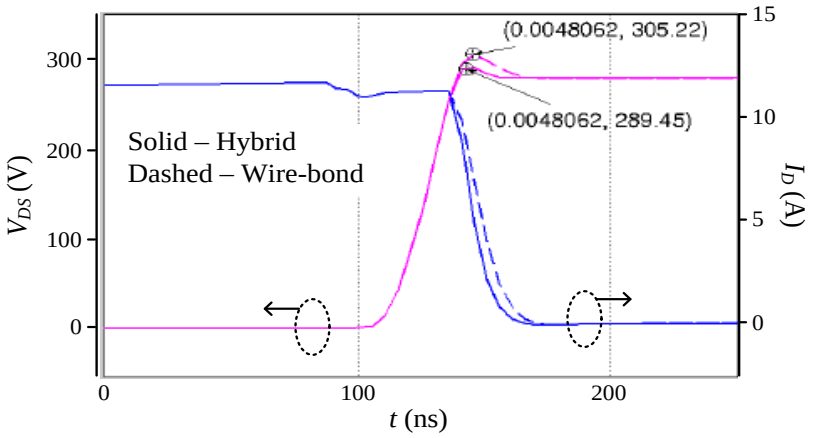


Figure 6-5. Simulated SiC JFET turn-off waveforms in wire-bond and hybrid packages

The three-phase rectifier module is fabricated following the steps in Figure 6-2 with the materials in Table 6-1. Figure 6-6 is a picture of the fabricated module. For this prototype, a T-type thermocouple is also embedded inside the module to monitor the device temperature.

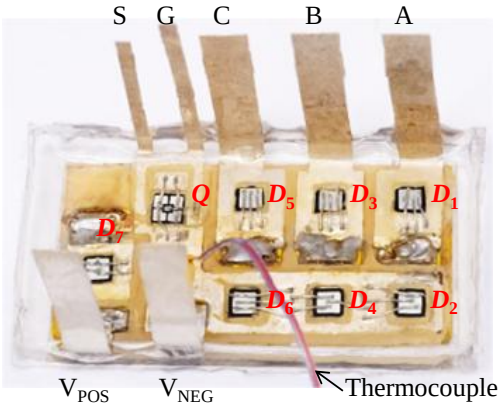
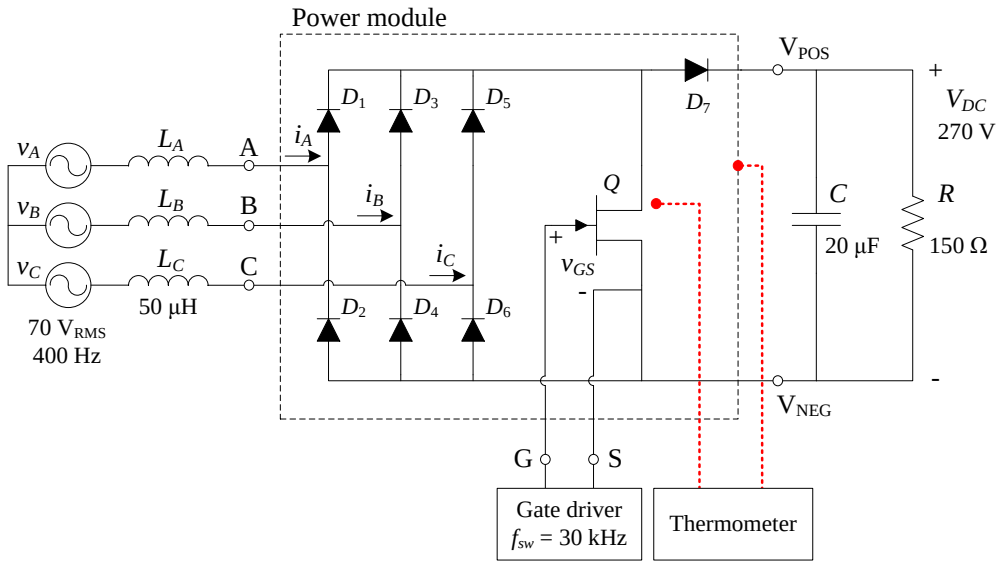


Figure 6-6. SiC JFET three-phase rectifier module in the hybrid structure

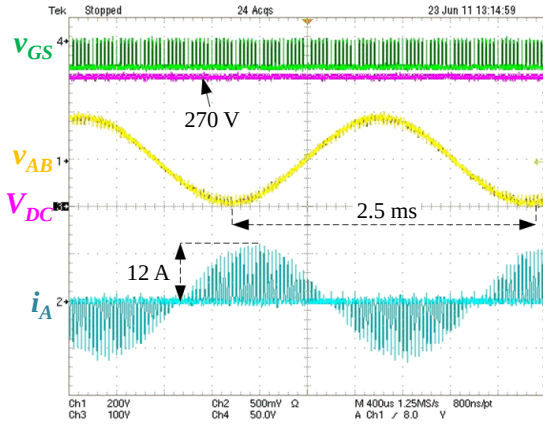
The module test circuit is illustrated in Figure 6-7 (a). As seen, the rectifier is supplied by a three-phase voltage source with 70 V RMS phase voltage and 400 Hz line frequency. The SiC JFET is switched at 30 kHz, and the output DC voltage is regulated at 270 V. The maximum current of the JFET is 12 A, and, correspondingly, the maximum output power is approximately 500 W. The typical waveforms of the converter are displayed in Figure 6-7 (b).

The high-temperature operation of the module is verified in the room environment by using only natural convection cooling without any heatsink attached to the module. Besides the embedded one, another T-type thermocouple is also used to measure the case temperature. After 30 minutes of operation under full load, the embedded thermocouple measures 224.5 ℃, and the case one measures 201.7 ℃, as shown in Figure 6-7 (c). Considering that the embedded thermocouple is roughly 1 cm away from the JFET, the real device junction temperature will be higher than what is measured.

The converter achieves a reasonable total efficiency of 96.1% under full load and over 224.5 ℃ junction temperature, only 0.9% lower than the room-temperature efficiency when the converter just starts. The test results thus verify the high-temperature capability of the proposed hybrid module.



(a)



(b)

(c)

Figure 6-7. Experimental verifications of the hybrid power module

(a) Test circuit, (b) test waveforms, (c) temperature measurements during the test

6.3 Development of an Ultra-Fast SiC Phase-Leg Module in Modified Hybrid Structure

A potential problem for the above hybrid structure, however, is the reliability of the polyimide-copper interface under thermal cycling conditions. In [22], it is shown that the copper layer delaminates from the polyimide after only 100 thermal cycles from -55 to 200 ℃, due to the CTE mismatch between the two materials and the resultant thermal stresses. Also, the process of curing polyimide multiple times during module fabrication is still considered too complicated and time-consuming. To address these issues, a modified hybrid packaging structure is proposed and explored in this section.

6.3.1 Modified Hybrid Structure, Material Selection, and Fabrication Process

Figure 6-8 illustrates the cross-sectional structure of the modified hybrid package. Compared to Figure 6-1, the biggest change in this structure is that a multilayer PCB is used to replace the polyimide-copper combination. Windows are cut on the PCB for the semiconductor dice to be embedded, so that both the PCB and the devices can be attached to the same DBC substrate. Bonding wires are then used to connect the top electrodes of the device to the top copper traces on the PCB.

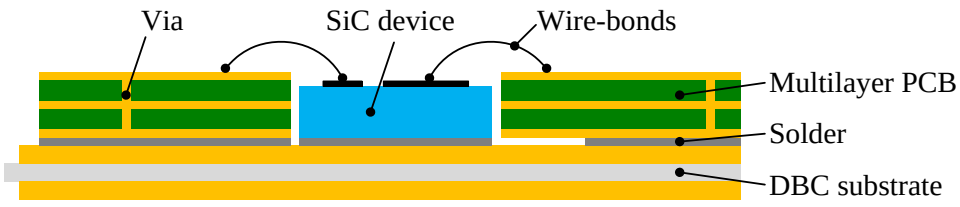


Figure 6-8. Cross-sectional view of the modified hybrid structure

The modified design has many advantages over the original concept. First of all, the PCB layer of the package can be made with long-established, standard PCB fabrication process [23], and can be soldered onto the substrate together with semiconductor dice in a single reflow process, which significantly simplifies the manufacture of the hybrid module. Besides, much more complicated routing can be achieved on the PCB by increasing the copper layers of the board, and/or by using through-hole, blind, or even buried vias. This allows the switching current paths to be controlled more flexibly, and also provides the possibility of embedded gate driver circuit in the module. Furthermore, the thermal reliability issue of PCBs has been investigated for a long time. The primary failure mode has been identified, and thus their operational lifetime is more predictable [24]-[26]. Plus, a variety of laminate materials have been developed for PCBs to work in different applications, among which high-thermal-reliability products are also available for harsh-environment uses [27].

Instead of studying the reliability of the proposed structure, however, this work will mainly focus on the feasibility of the modified hybrid package to realize compact, low-inductance modules which ultimately allow SiC devices to be switched to their speed limit. For this reason, low-temperature packaging materials are selected considering both availability and cost, which are given in Table 6-3. Note that solder pads on the PCB need to be finished by immersion gold for them to become wire-bondable [28].

Table 6-3. Bill-of-Materials for the Modified Hybrid SiC Power Module

Part	Material	Specifications
Switch	Cree SiC MOSFET	1200 V, 10 A Die dimension: 3.1 × 3.1 × 0.365 mm^3 Top: gate & source pads, Al metalized Bottom: drain pad, Ag metalized
Diode	Cree SiC Schottky diode	1200 V, 5 A Die size: 1.69 × 1.69 × 0.377 mm^3 Top: anode pad, Al metalized Bottom: cathode pad, Ag metalized
Substrate	Curamik Al_2O_3 DBC	Cu/Al_2O_3/Cu thicknesses: 8/15/8 mils Ag electroplated
Solder	Sn96.5-Ag3-Cu0.5 (SAC 305) paste	Solidus/liquidus temperatures: 217/221 ℃
PCB	Cu & FR-4	Copper weight: 1 oz. Solder pad plating: Immersion gold FR-4 dielectric strength: 0.51 kV/mil
Leadframe	Cu	10 mils, Au plated
Bonding wire	Al	Dia.: 10 mils

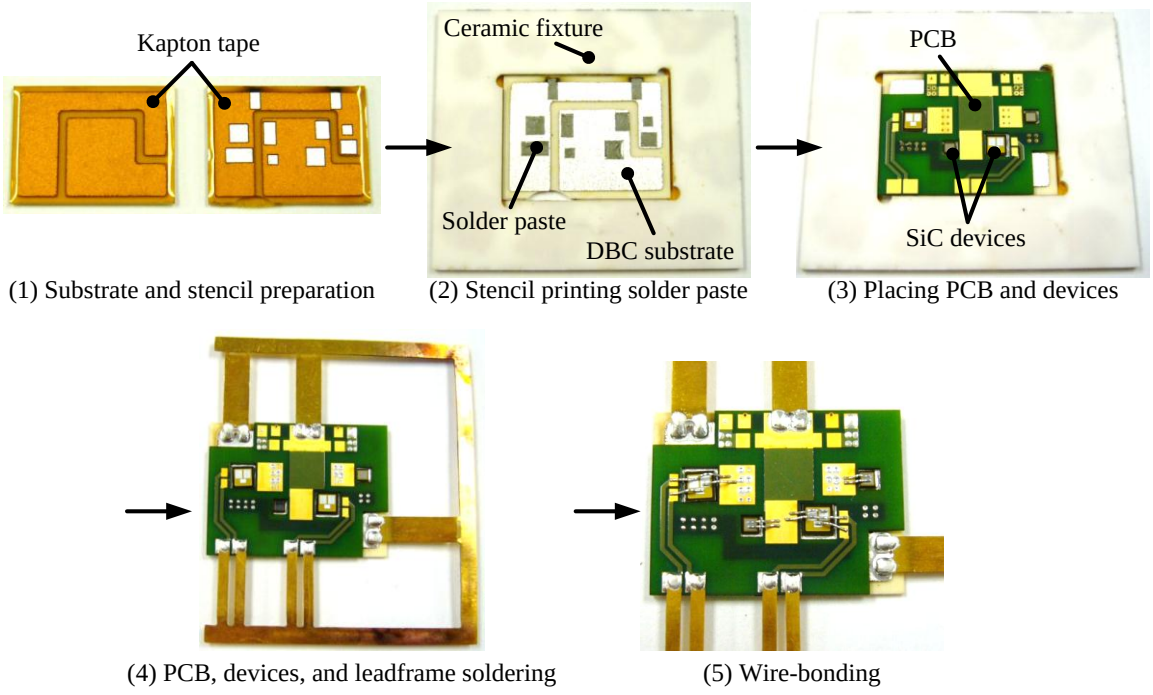


Figure 6-9. Fabrication process of a SiC MOSFET module in modified hybrid structure

The fabrication process of the modified hybrid module is much simpler compared to the original structure. As illustrated in Figure 6-9, the Kapton tape is firstly attached to the patterned DBC substrate working as the stencil for solder printing, which is removed after the solder paste is applied. The PCB, SiC devices, and leadframe are then placed on top of the DBC at the same time. All these components can be attached to the substrate with one single step of solder reflow. Afterwards, the devices' top electrodes are wire-bonded to the corresponding solder pads on the PCB. After necessary encapsulation (e.g. with molding compound), the whole module is fabricated and ready to use.

6.3.2 Development of the Ultra-Fast SiC MOSFET Phase-Leg Module

A SiC MOSFET phase-leg module is designed and fabricated in the proposed structure to demonstrate its potentials in reducing the module's footprint and parasitics. The selected devices are given in Table 6-3. For simplicity, a single MOSFET and a single diode are used in each switch position of the phase-leg. Figure 6-10 shows the internal structure of the module. As seen, the four devices are still grouped by switch pair to minimize switching loops. The DBC substrate carries the V_{POS} and V_{OUT} terminals of the phase-leg, while the V_{NEG} terminal sits on the top side of the two-layer PCB. Also on the top side are the gate drive signal traces which form Kelvin-type connections. The bottom pads of the PCB work as the soldering sites bonding the PCB to the substrate, and meanwhile, connect the top layer traces to the DBC through vias. DC decoupling capacitors (1 kV, 4.7 nF each) can also be easily integrated by simply soldering them on the PCB. The module is designed to be encapsulated by molding compound as suggested in Figure 6-11. To use the module, the molding package side should be mounted onto the

converter PCB, while the back side of the DBC substrate should be attached to the heatsink for cooling.

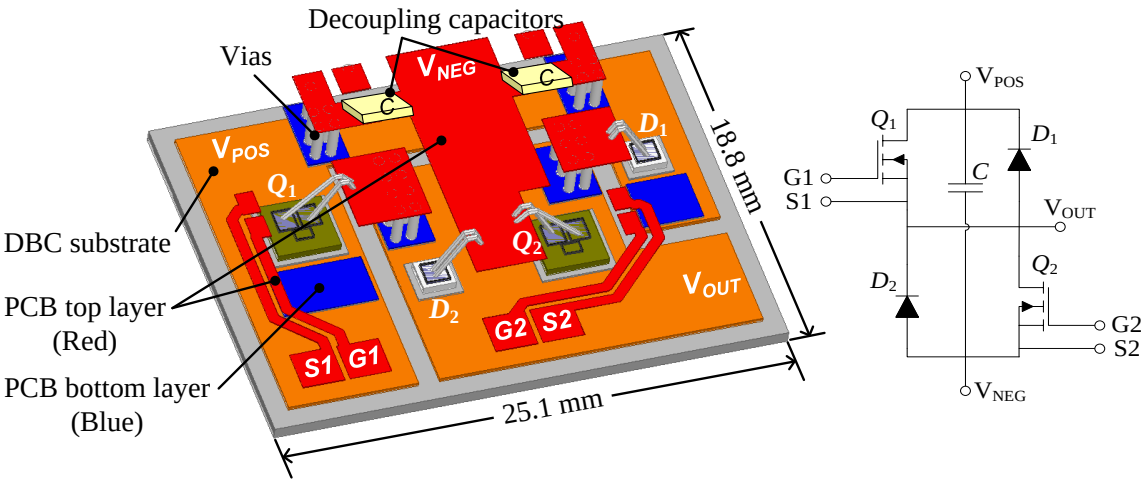


Figure 6-10. Internal structure and circuit schematic of the hybrid SiC MOSFET phase-leg module

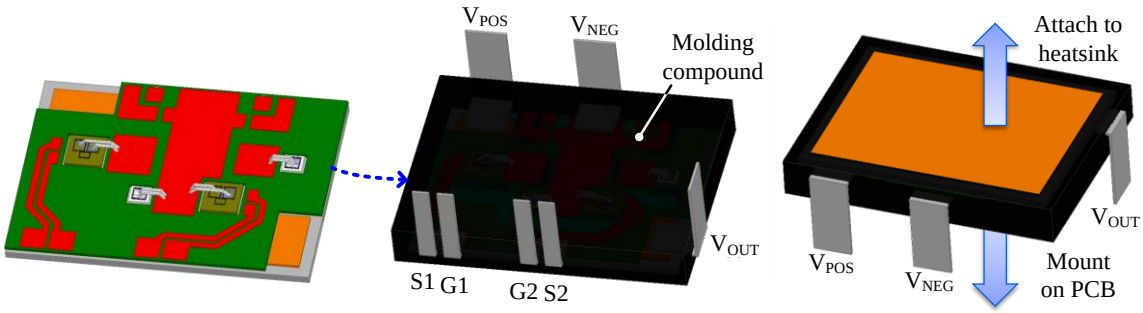


Figure 6-11. Intended encapsulation and use of the phase-leg module

Following the process in Figure 6-9, a phase-leg module is fabricated and is shown in Figure 6-12. For easy module testing, the molding compound is replaced by a thin layer of silicone conformal coating which provides sufficient electrical insulation for the module. Next to the phase-leg module is a typical TO-247 package for footprint comparison. TO-247 is an industrial standard package used to house a single 1200 V, 10 A SiC MOSFET in discrete power converters. Thanks to the compactness of the hybrid

structure, the entire phase-leg now can be integrated into a footprint only 45% larger than a single device package.

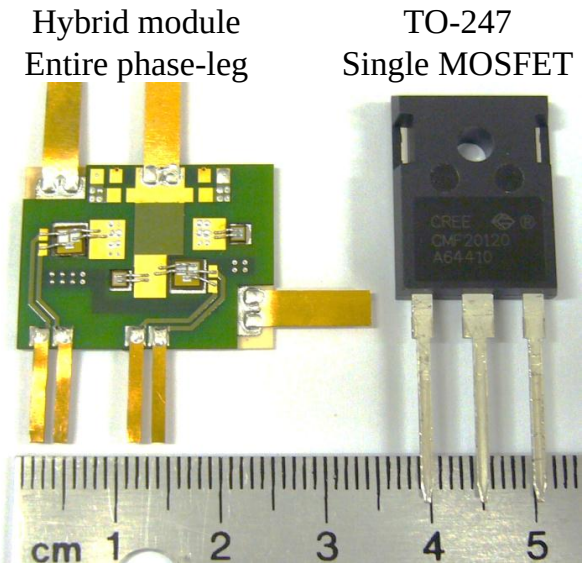


Figure 6-12. Footprint comparison between hybrid phase-leg module and conventional TO-247 single MOSFET package

In addition to the smaller footprint, the hybrid module also features very low package parasitics. Figure 6-13 plots the switching loop inductances (excluding power-terminal-related inductances due to the embedded decoupling capacitors) as a function of the thickness of the PCB's dielectric layer, extracted from Q3D simulation. At the designed thickness of 10 mil, both switch pairs show the same loop inductance of only 3.8 nH. The impedance measurement performed on the actual module shows a loop inductance of 3.6 nH, which agrees well with the simulation.

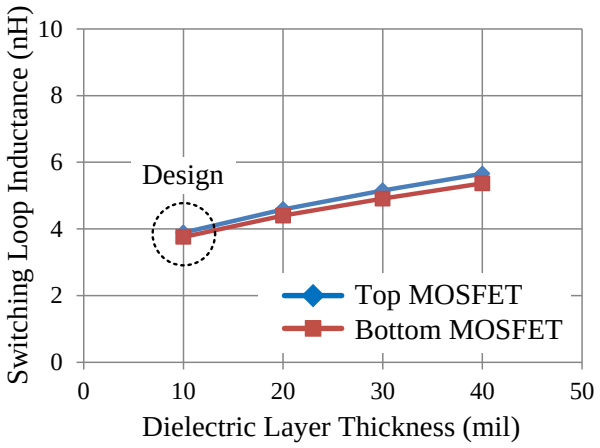
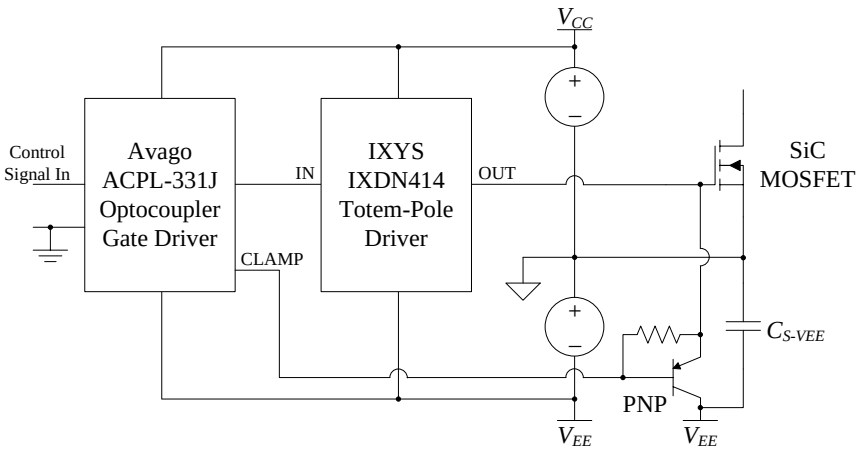
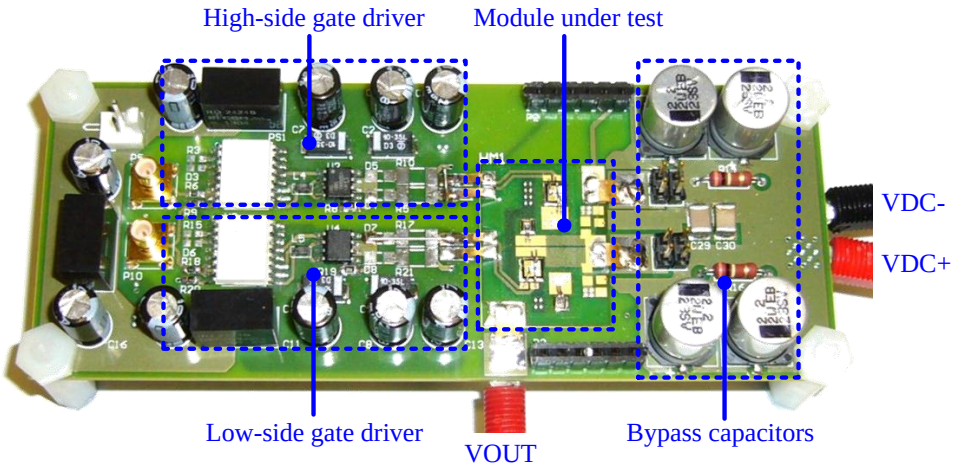


Figure 6-13. Simulated switching loop inductances vs. PCB dielectric layer thickness



(a)



(b)

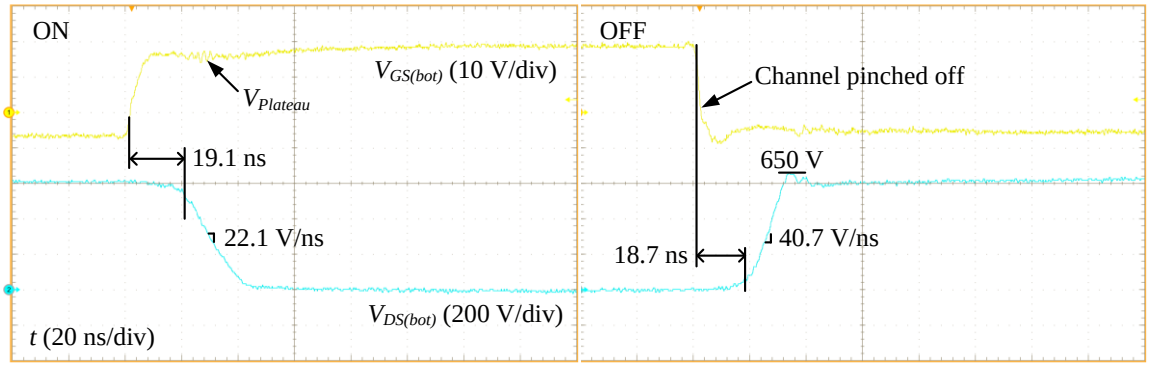
Figure 6-14. Hybrid module tester. (a) Gate drive circuit, (b) tester board

To test the switching performance of the designed module, the high-speed gate drive in Chapter 4 is slightly modified and utilized in this work to drive the SiC MOSFETs, as shown in Figure 6-14 (a). The gate drive now switches the device between V_{CC} of 20 V and V_{EE} of -5 V, without any external gate resistance. The module tester board is shown in Figure 6-14 (b), where the module under test, gate drives, and bypass capacitors, etc., can be identified.

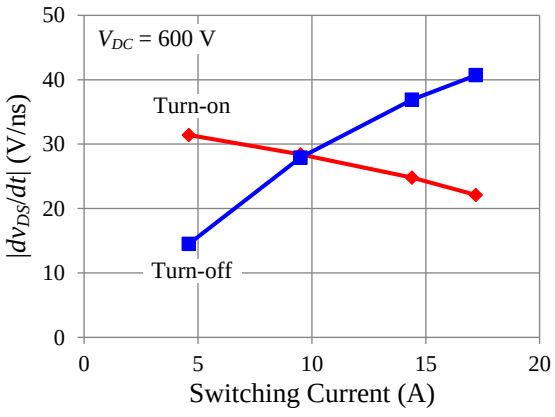
The module's switching waveforms under 600 V, 17.4 A clamped inductive load are displayed in Figure 6-15 (a). The switching current is not measurable due to the embedded capacitors, so is not included in the figure. With 0 Ω gate resistance, ultra-fast switching transients are achieved – the $|dv_{DS}/dt|$ is 22.1 V/ns at turn-on, and 40.7 V/ns at turn-off. Switching delay times are also less than 20 ns for both switching edges. The fast switching speed, however, does not cause excessive parasitic ringing and device over-voltage. Both the gate and drain voltage waveforms are very clean, and the V_{DS} overshoot at turn-off is merely 50 V.

The V_{DS} slew rates are plotted against the switching current in Figure 6-15 (b). During turn-on, the high gate plateau level $V_{Plateau}$, which is due to the low transconductance g_{fs} of the SiC MOSFET, greatly limits the discharging rate of the MOSFET's Miller capacitance, and hence $|dv_{DS}/dt|$, according to Eq. (2-2) and (2-3). With greater switching current, $V_{Plateau}$ becomes even higher, leading to the decreasing $|dv_{DS}/dt|$ under the increasing load. Therefore, low g_{fs} of the SiC MOSFET has now become the bottleneck for the turn-on speed. During turn-off, on the other hand, the MOSFET channel is pinched off very soon when V_{GS} drops below the gate threshold. After that, the load current charges/discharges the junction capacitances of top and

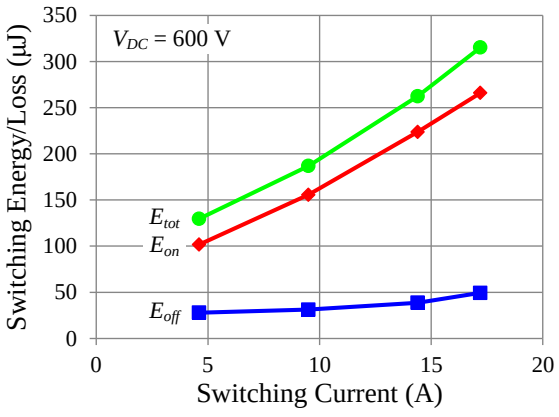
bottom switches, causing V_{DS} to swing between zero and the bus voltage. $|dv_{DS}/dt|$ at turn-off is therefore positively related to the load current, and is limited by the junction capacitances of the SiC devices. In other words, the switching speed limit of the SiC MOSFET has been reached in the designed hybrid phase-leg module almost without any ringing or over-voltage problem. The switching energies corresponding to this extreme speed are measured by sensing the switching current with the embedded capacitors removed, which are shown in Figure 6-15 (c).



(a)



(b)



(c)

Figure 6-15. Switching performances of the hybrid phase-leg module
(a) Switching waveforms at 600 V, 17.4 A, clamped inductive load,
(b) $|dv_{DS}/dt|$ vs. load current, and (c) switching energies vs. load current

6.4 Conclusions

This chapter presents the development of a novel hybrid packaging structure for SiC power modules. As a combination of the wire-bond and planar structures, the hybrid module can achieve the same footprint and similar package parasitics compared to a planar module, but is easier to fabricate since it does not require double-sided solderability for the semiconductor devices. Moreover, the wire-bond interconnections on the device top pads also provide better bonding quality and thus higher reliability than many planar modules. As long as proper devices and packaging materials are used, the hybrid module is also capable of high-temperature operations. This has been proved experimentally on a three-phase rectifier module with SiC JFET and diodes.

A modified hybrid structure is then proposed by replacing the copper-polyimide combination with a multilayer PCB. Keeping all the benefits of the original concept, the proposed method of packaging further provides the advantages of easier fabrication, higher reliability, and more complex module structure. A SiC MOSFET phase-leg module has been designed in such a package to demonstrate its capabilities in reducing the module's footprint and stray inductances. It has been shown that, in this hybrid package, the SiC MOSFETs can be switched to their speed limit without causing serious parasitic ringing or device over-voltages. This allows the switching loss to be minimized in high-frequency SiC power converters, and will ultimately increase the power density and efficiency of the overall power conversion system.

6.5 References

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Chapter 7 Analysis and Implementation of Switching Loop Snubber

7.1 Introduction

Previous chapters have emphasized repeatedly the importance of the switching loop inductance on the parasitic ringing of semiconductor switches. While reducing this stray inductance is the most straightforward way towards cleaner switching waveforms, there exist many other methods to suppress ringing. The most traditional ways are the resistor-capacitor (*RC*) and resistor-capacitor-diode (*RCD*) snubber circuits, which are typically connected across the switch to limit its *dv*/*dt* or *di*/*dt*, and hence reduce the voltage or current spikes [1][2]. Because the ringing is reduced by slowing down the switching speed, these methods are less and less used in today's high-frequency power converters. Besides paralleling snubbers to the switch, the parasitic ringing can also be suppressed by inserting damping elements in series with the switching loop. Ref. [3] proposed to insert a ferrite bead in series with the SiC JFET phase-leg to provide a high damping resistance for the ringing frequency, while keeping the DC resistance very low. The bead, however, introduced another small inductance in the switching loop which increased the turn-off voltage spike of the SiC JFET. Moreover, the power loss on the ferrite bead would also

limit its use in high-current applications. A similar idea was presented in [4], where paralleled resistor and inductor were used in series with the top MOSFET in a buck converter to provide damping. The drawbacks of this method are also similar: Higher turn-off over-voltage, and reduced converter efficiency of over 1% due to the loss on these inserted elements. In [5], a capacitive zone and an inductive zone were integrated into the bus bar of an IGBT phase-leg to limit voltage and current slopes, so that the switching oscillations could be reduced. This method was essentially a combination of the capacitor snubber and the inserted resistor-inductor (*RL*) elements, and thus would experience the same issues described above.

In this chapter, a switching loop snubber circuit will be proposed to suppress the parasitic ringing without either lowering the switching speed of the device, or increasing the conduction loss of the converter. The new concept will firstly be introduced and analyzed, and further verified through experiments. The integration of such a circuit in the power module will then be presented, and possible improvements will also be discussed in the end.

7.2 Analysis of the Switching Loop Snubber

As discussed in Chapter 3, the turn-off ringing of a MOSFET originates from the highly under-damped parallel resonance between its output capacitance C_{OSS}, and the switching loop inductance L_{DS}. The more fundamental state variables behind C and L are the electric charge Q and the magnetic flux Φ. While Q is stored in the device junction capacitance which is not easy to change, Φ is distributed in the space around the current path, determined by the Biot-Savart law. If Φ can be picked up by another lossy inductor

through magnetic coupling, it is then possible to provide additional damping to the resonance between Q and Φ.

To firstly verify this hypothesis, double-pulse simulation is conducted with the use of a Si MOSFET model. The simulation circuit is shown in Figure 7-1. The MOSFET is Microsemi APT20N60BCF, while the diode is Cree CSD10060. Besides the stray inductances associated the device packages, an additional inductance L_{DS} is inserted in the switching loop to mimic the circuit parasitics. L_{DS} is further coupled with a snubber loop inductance L_S with a coupling coefficient k, which is terminated by a damping resistance R_S.

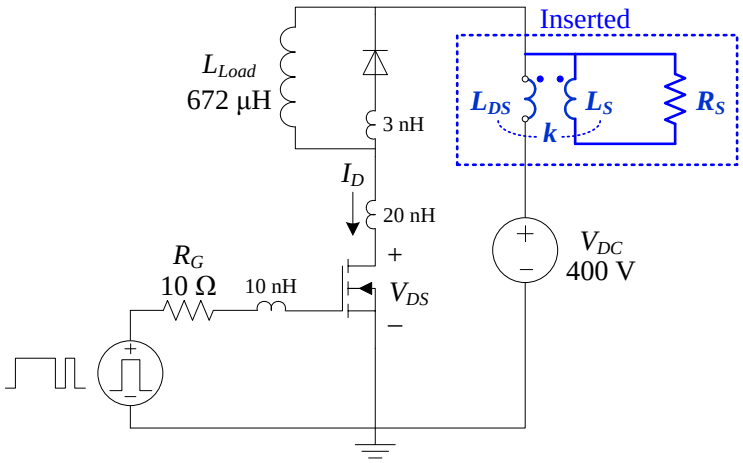


Figure 7-1. Double-pulse simulation circuit with switching loop snubber

Figure 7-2 shows the simulated switching waveforms of the MOSFET at 400 V, 10 A, under L_{DS} = L_S = 97 nH, k = 0.6, and various R_S. Apparently, R_S = Inf represents the condition when the snubber loop does not affect the original circuit, which also has the highest ringing amplitudes among all R_S values according to the figure. The lowest ringing, however, does not happen at R_S = 0 Ω either. Instead, the condition of R_S = 10 Ω gives a better damping effect than the 0 Ω and 100 Ω cases. Furthermore, it is easy to tell

from the waveforms that the switching speed of the MOSFET is not affected by the snubber loop, as both *dv*/*dt* and *di*/*dt* stay the same in all cases.

The simulation reveals two facts about the switching loop snubber: (1) The snubber circuit does help reduce the parasitic ringing of the device without slowing down its switching speed; and (2) there exists an optimal R_S value that would generate the best damping effect for the snubber.

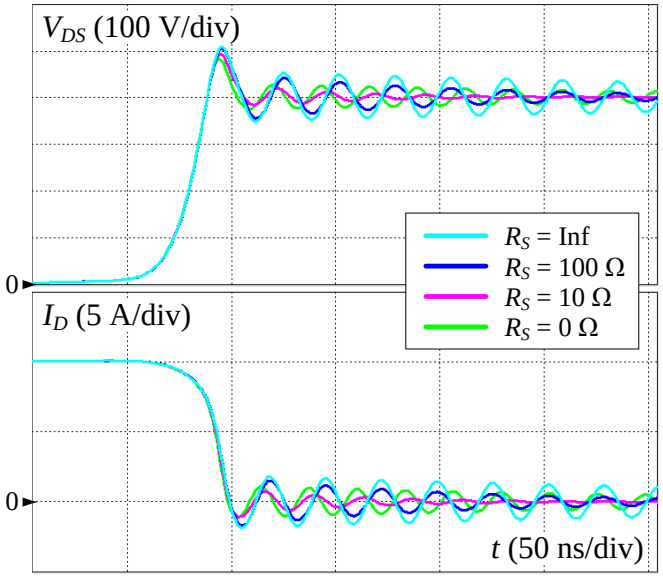


Figure 7-2. Simulated switching waveforms with switching loop snubber

The small-signal model developed in Chapter 3 is utilized in this work to analyze how the circuit parameters influence the snubber's damping effect. The equivalent circuits including the switching loop snubber are illustrated in Figure 7-3. Assuming the coupling coefficient is given as k = 0.6, and the other circuit parameters are C_{OSS} = 121 pF, R_{FWD} = 59.3 mΩ, and L_{DS} = L_S = 97 nH, the Bode plot of the input impedance Z_{IN} is then a function of the damping resistance R_S, which is shown in Figure 7-4. When R_S = Inf, the snubber loop does not have any damping effect, and the parallel resonant peak

occurs at the original frequency of $1/2\pi\sqrt{L_{DS}C_{OSS}}$. At the other extreme of R_S = 0 Ω, the k^2L_{DS} branch is shorted in the small-signal model, and the effective stray inductance is reduced to $(1\text{-}k^2)L_{DS}$, which results in a higher resonant frequency with lower peak impedance. This indicates that the MOSFET's turn-off ringing will have higher frequency but lower amplitude. As R_S decreases from Inf to 0, the resonant frequency moves from $1/2\pi\sqrt{L_{DS}C_{OSS}}$ to $1/2\pi\sqrt{(1-k^2)L_{DS}C_{OSS}}$, and the peak impedance first decreases and then increases. Therefore, a minimum peak impedance, or Q factor, can be achieved at a certain R_S value.

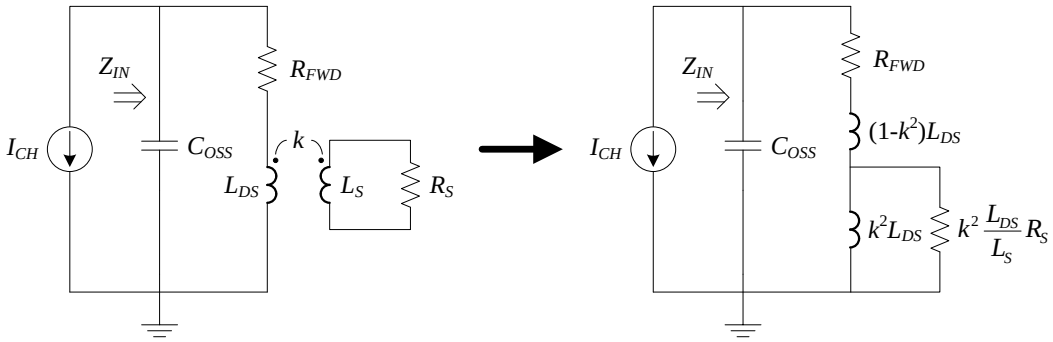


Figure 7-3. Small-signal model for the turn-off ringing with switching loop snubber (left) Model with coupled inductors, (right) equivalent model with decoupled inductors

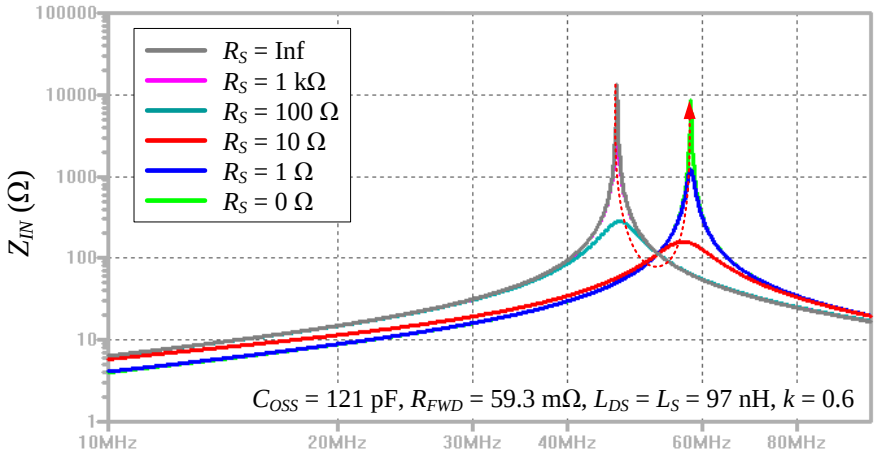
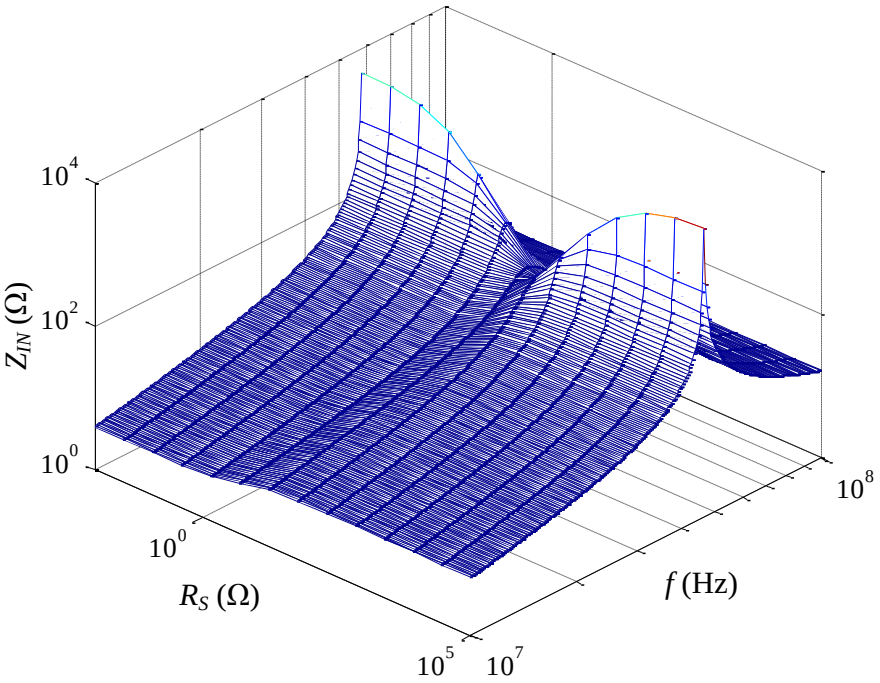


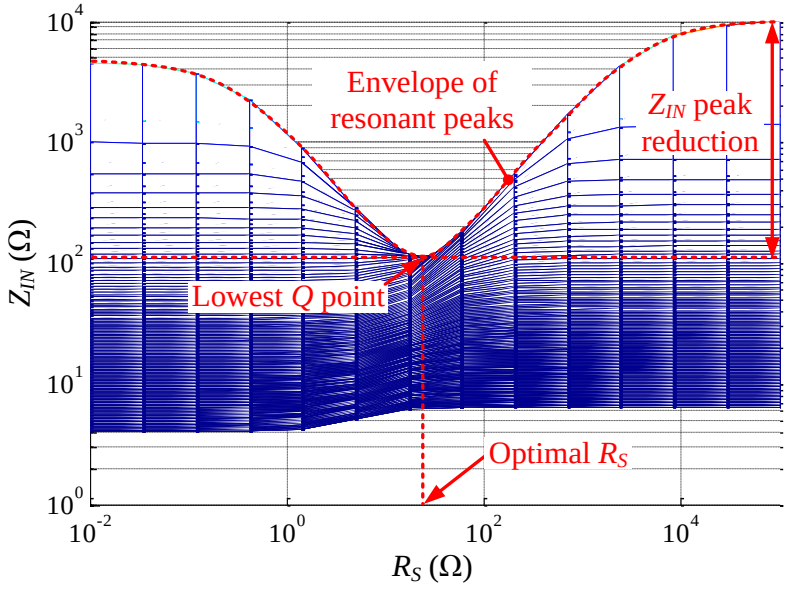
Figure 7-4. AC simulation of Z_{IN} as a function of R_S under the given circuit parameters

The optimal R_S value and the minimum peak impedance are hard to be solved analytically, but can be easily found in either circuit simulators or Matlab by sweeping the parameters. Using the same circuit parameters, Z_{IN} can be plotted against both frequency and R_S in Matlab in a 3D view, as shown in Figure 7-5 (a). Viewing this figure perpendicular to the Z_{IN}-f plane leads to Figure 7-4, while the view angle perpendicular to the Z_{IN}-R_S plane leads to Figure 7-5 (b). In this figure, the valley point on the envelope of the resonant peaks represents the lowest Q-value or the highest damping condition of the system, and the corresponding R_S is the optimal resistance to terminate the snubber loop. Under the assumed circuit parameters, the switching loop snubber can reduce the resonant peak impedance by almost 100 times. From the same figure, the results in Figure 7-2 can also be explained very easily.

The coupling coefficient k of the snubber loop obviously has a great impact on the highest damping the system can achieve. Figure 7-6 plots the envelopes of resonant peaks under various k values. At k = 0, the snubber loop is fully decoupled, so R_S has no influence on the peak impedance of the system. This corresponds to the flat line in the figure. At k = 1, on the other hand, the $(1\text{-}k^2)L_{DS}$ term in the small-signal model becomes zero, and the k^2L_{DS} inductance can be completely bypassed if R_S = 0. This would totally eliminate the inductive elements in the model and result in a non-oscillating, first-order system. In actual circuits, however, k is between 0 and 1. According to Figure 7-6, it is obvious that a lower valley point, or Q factor, can be achieved with a higher k value. In other words, the higher the coupling is, the better the damping can be realized.



(a)



(b)

Figure 7-5. Z_{IN} as a function of both f and R_S. (a) 3D view, (b) Z_{IN}-R_S plane view

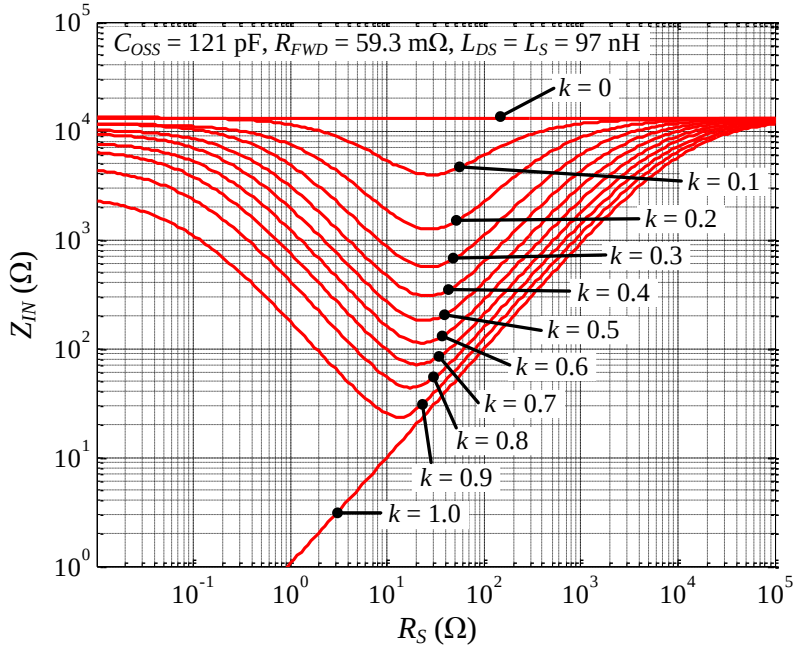


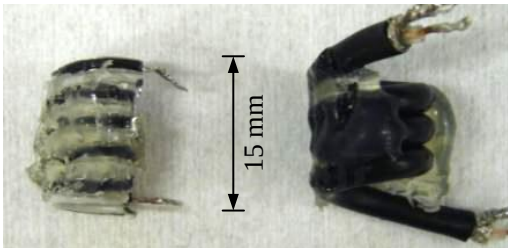
Figure 7-6. Envelopes of resonant peak impedances under various coupling coefficients

Another parameter of the switching loop snubber is the self-inductance L_S of the snubber loop. From the model in Figure 7-3, it can be seen that L_S affects the resistance term $k^2L_{DS}R_S/L_S$ through the ratio of R_S/L_S. Therefore, the absolute value of L_S is not so critical since the terminating resistance R_S can always be tuned in the circuit to achieve the desired R_S/L_S ratio.

Finally, it needs to be noted that Figure 7-4 through Figure 7-6 are plotted using the same specified circuit parameters. The determinant factors for the analyzed system are C_{OSS}, L_{DS}, k, and R_S. Changing these parameters does not change the trends how k and R_S affect the system, but does change the absolute Q factors and damping effects achievable by the switching loop snubber. Therefore, Figure 7-6 needs to be re-plotted for each specific design (e.g. device selection and circuit layout design) to determine the best damping effect that can be achieved with the snubber.

7.3 Experimental Verifications of the Switching Loop Snubber

Switching tests are performed on a Si MOSFET (Microsemi APT20N60BCF) to prove the proposed concept. The test circuit is the same as Figure 7-1. The coupled inductors are realized in two configurations – the parallel wires and the shielded wires, as shown in Figure 7-7. The parallel wires achieve a coupling coefficient of 0.6, while the shielded wires achieve 0.8. The primary-side inductors (97 nH and 100 nH respectively) are inserted in series with the main switching loop, while the snubber loops are terminated by potentiometers to adjust their damping resistances during the test.



Parallel wires	Shielded wires
L_{DS} = 97 nH (Black),	L_{DS} = 100 nH (Core),
L_S = 97 nH (White),	L_S = 65 nH (Shield),
k = 0.6	k = 0.8

Figure 7-7. Coupled inductors used in the switching tests

Figure 7-8 shows the MOSFET turn-off waveforms under k = 0.6 and four different R_S values. As seen, the ringing is most severe when R_S = Inf, i.e. the snubber loop does not provide any damping. As R_S reduces, the ringing frequency starts to increase, and the damping effect becomes more pronounced. The best damping condition occurs at R_S = 40 Ω, with the corresponding V_{DS} over-voltage reduced by 8 V. As R_S keeps decreasing, the ringing frequency becomes even higher, and the settling time becomes longer again. These time-domain behaviors are consistent with the previous frequency-domain analysis.

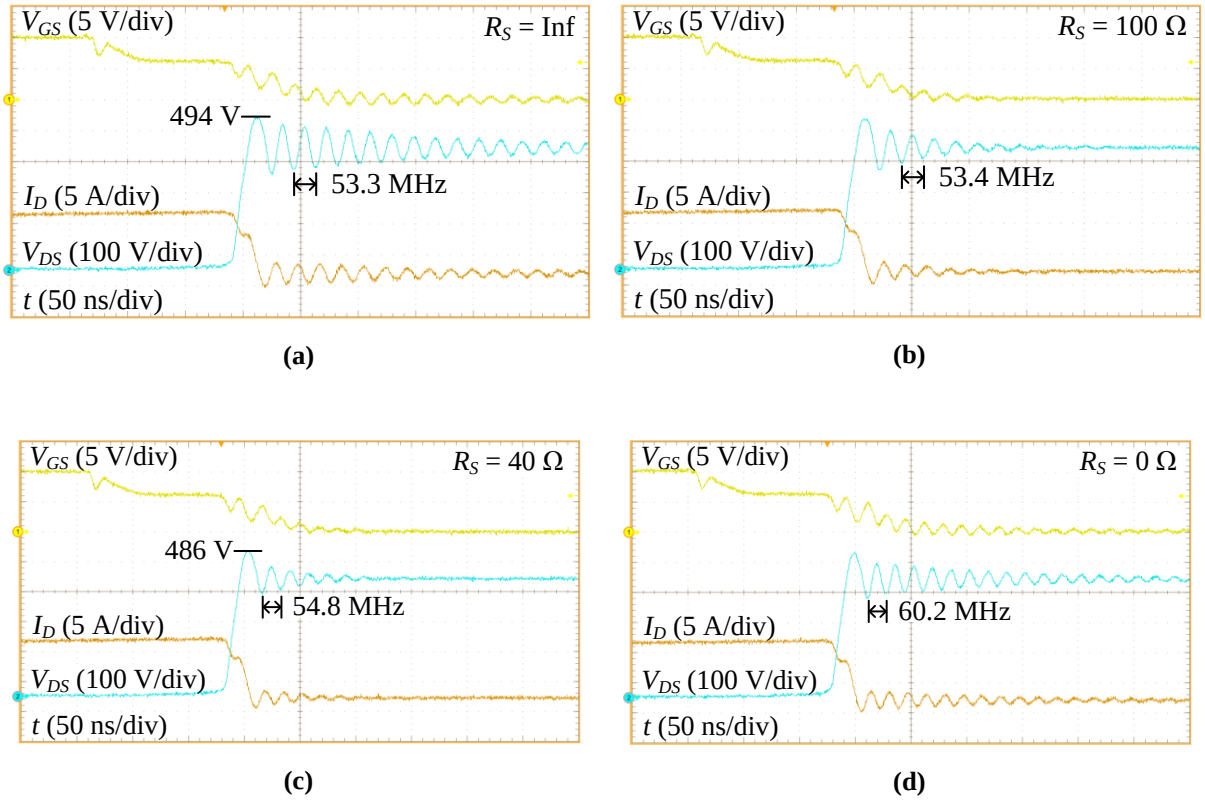


Figure 7-8. MOSFET turn-off waveforms with the switching loop snubber at k = 0.6
(a) R_S = Inf, (b) R_S = 100 Ω, (c) R_S = 40 Ω, (d) R_S = 0 Ω

The waveforms under k = 0.8 condition are shown in Figure 7-9. The parasitic ringing changes in the same trend as R_S decreases from Inf to zero. The best damping in this case occurs at R_S = 20 Ω. Comparing Figure 7-9 (c) with Figure 7-8 (c), it is obvious that the higher coupling of the switching loop snubber generates a better damping performance, and thus is more desirable in the snubber circuit design.

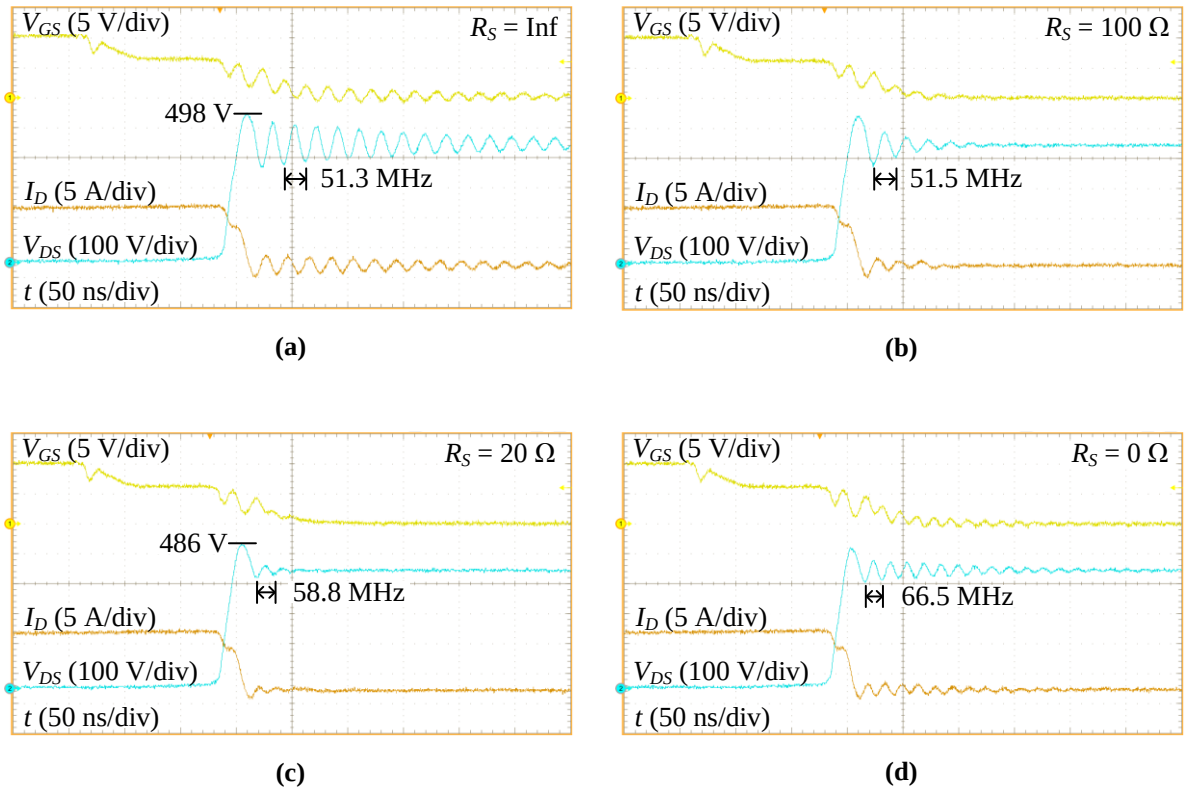
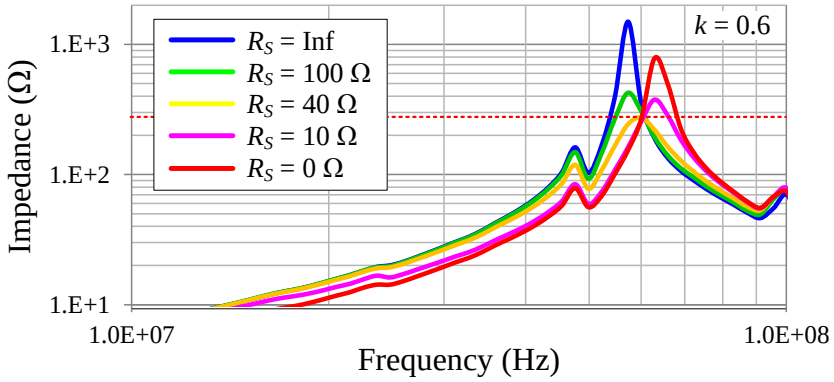
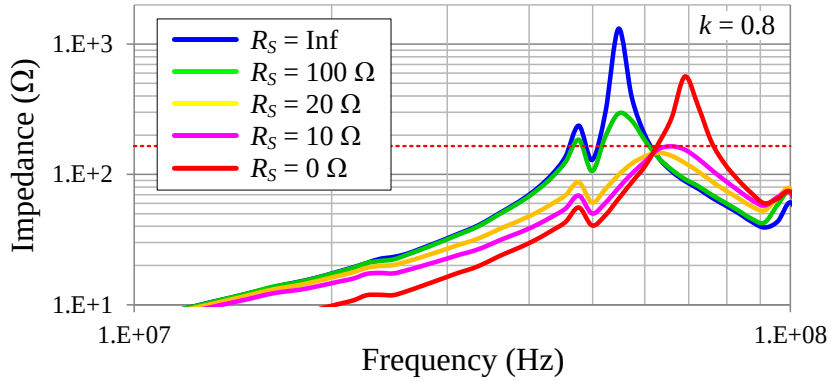


Figure 7-9. MOSFET turn-off waveforms with the switching loop snubber at k = 0.8
(a) R_S = Inf, (b) R_S = 100 Ω, (c) R_S = 20 Ω, (d) R_S = 0 Ω

Following the same method presented in Section 3.4.2, the MOSFET's drain-source impedance at 400 V bias is measured by Agilent 4294A with the switching loop snubber in the circuit. The results displayed in Figure 7-10 are consistent with the simulation in Figure 7-4, further verifying the correctness of the analysis. Comparing the two figures, one can also see clearly that a lower Q factor is achieved under the higher coupling condition, which again accounts for the better damping effect observed in Figure 7-9 (c).



(a)



(b)

Figure 7-10. MOSFET D-S impedance measurement at V_{DC} = 400 V, with the switching loop snubber (a) k = 0.6, (b) k = 0.8

Finally, it needs to be noted that in all previous analysis and experiments, relatively large stray inductances are inserted in the switching loop to exaggerate the ringing for better observations of the subber's effect. In actual circuit designs, however, minimizing the switching loop inductance should always be the top priority. To provide extra damping in the circuit, the switching loop snubber can be implemented in such a way that it generates the highest coupling with the original loop. The terminating resistance should then be tuned based on the previous analysis to achieve the optimal damping effect.

7.4 Implementation of the Switching Loop Snubber

7.4.1 Hybrid Phase-Leg Module with Integrated Switching Loop Snubber

As mentioned in Chapter 6, the hybrid package boasts its flexible structure and therefore offers the possibility of integrated switching loop snubber. The SiC MOSFET phase-leg module developed in Section 6.3 is modified in this work to integrate the snubber circuit. The internal structure of the module is illustrated in Figure 7-11. Based on the original design, an extra middle layer is inserted in the PCB as the snubber loop. The copper pattern is designed in such a way that the snubber loop overlaps with the switching loop as much as it can. Two terminating resistors, one for each switch pair in the phase-leg, are soldered on the top layer and connected to the middle layer through vias.

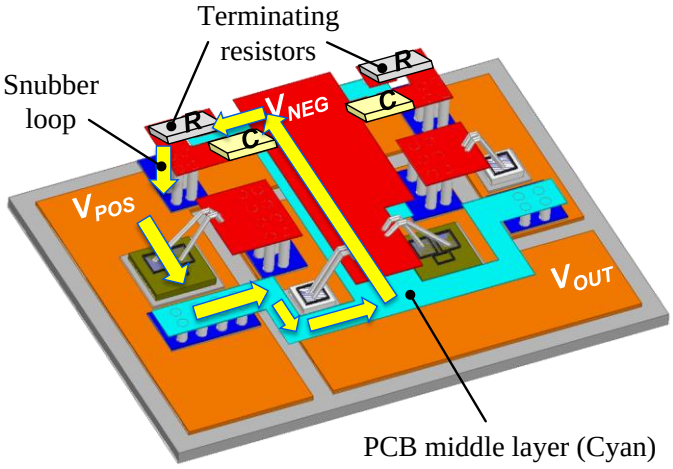


Figure 7-11. Internal structure of the hybrid SiC MOSFET phase-leg module with integrated snubber circuit (Gate drive traces not shown)

The coupling coefficient between the switching and snubber loops is extracted with Ansoft Q3D and is given in Figure 7-12 as a function of the dielectric layer thickness

(between adjacent copper layers). 5 mils thickness is finally selected considering the PCB manufacture capability and cost, as well as the dielectric strength of the FR-4 material. At such a thickness, the achieved coupling coefficient is about 0.4. The low coupling is mainly attributed to the leakage inductances from the PCB traces and, more importantly, the bonding wires. The snubber loop inductance at this thickness is extracted to be 3.3 nH.

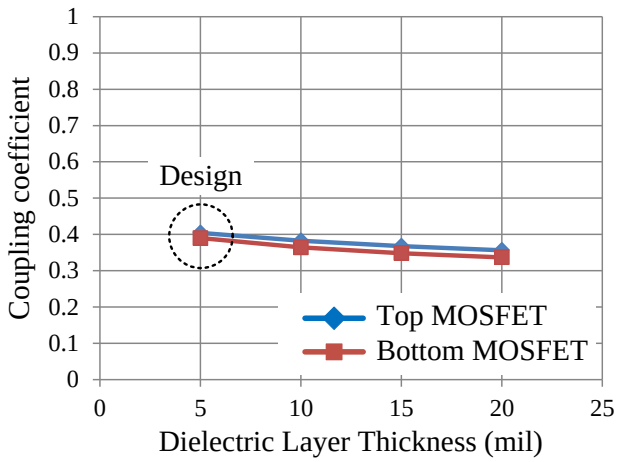


Figure 7-12. Simulated coupling coefficient vs. PCB dielectric layer thickness

Given the device selections and extracted stray inductances, the resonant peak impedance envelopes can be plotted in Figure 7-13. As seen, the snubber reduces the peak impedance by up to 7 times with the optimal damping resistance of 5.0 Ω. Note that the peak impedance reduction is much smaller for this particular module than the example in Section 7.2 for two reasons: (1) The original switching loop inductance is already very small due to the hybrid structure; and (2) the original damping resistances are relatively large due to the small current ratings of the selected devices. Both factors would thus weaken the effect of the snubber circuit.

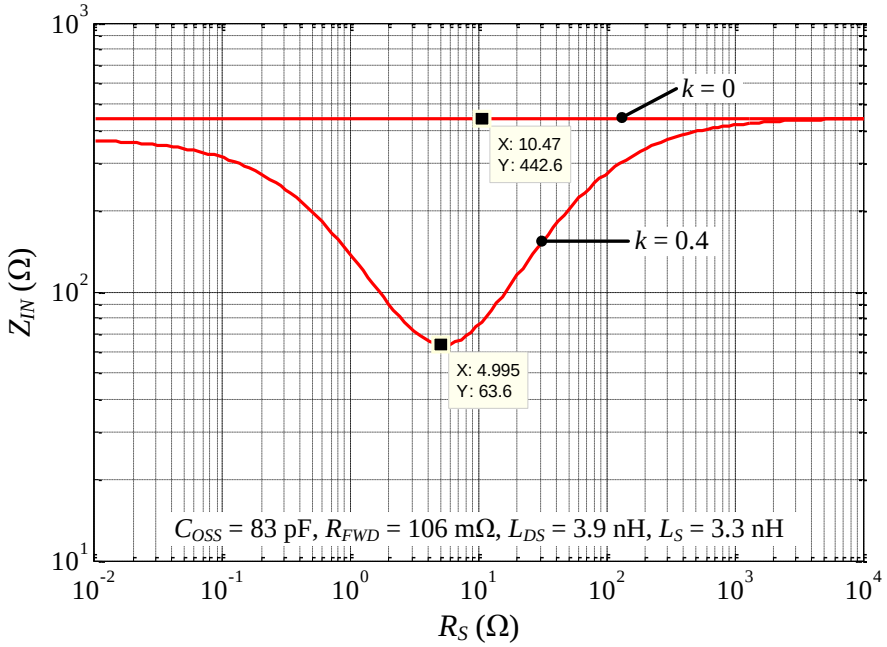


Figure 7-13. Envelopes of resonant peak impedances with and without the snubber loop

The module is fabricated based on the above design and tested using the same circuit in Figure 6-14. The terminating resistance is tuned during the test to find the optimal damping condition, which occurs when 1 Ω is used. The corresponding switching waveforms are shown in Figure 7-14. Because of the reasons stated above, the snubber effect is not very pronounced, and 1 V improvement in the V_{DS} spike can be seen only when the waveform is zoomed in. The small improvement, however, is consistent in all tested load conditions and thus verifies the effect of the snubber circuit, although the current module structure needs to be improved for the switching loop snubber to be more effective in practical use.

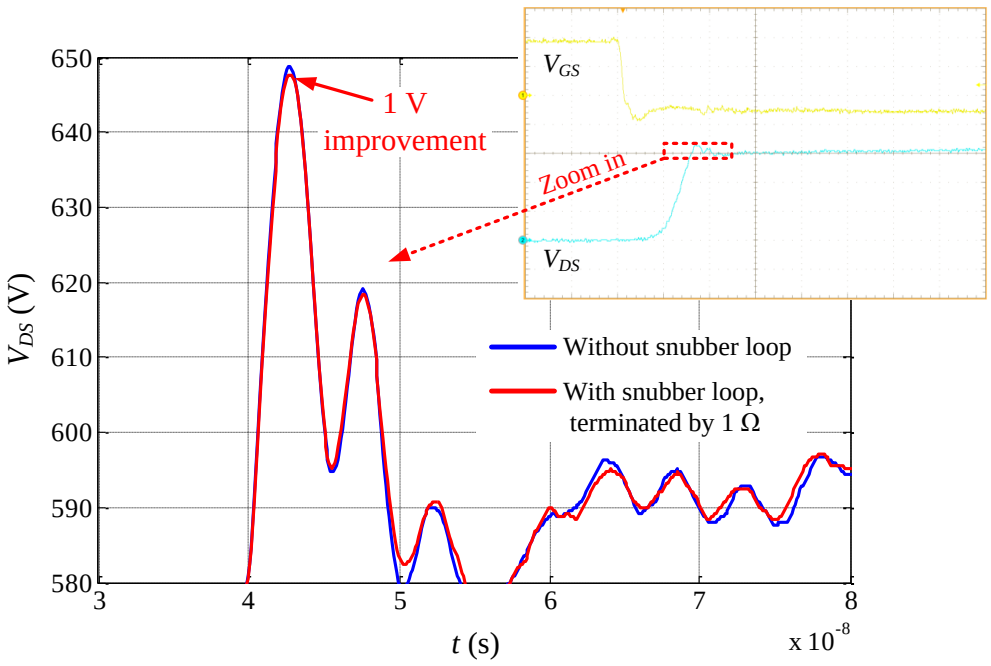


Figure 7-14. Turn-off waveforms of the hybrid phase-leg module at 600 V, 17.4 A, with and without snubber

7.4.2 Potential Improvements on the Coupling Coefficient

The low coupling coefficient between switching and snubber loops is one of the main reasons for the negligible improvement in the hybrid module with integrated snubber. Several methods are therefore proposed in this section to improve the coupling coefficient.

As mentioned in the previous section, the leakage inductances from bonding wires are one of the main causes of loose coupling. If replacing bonding wires by planar interconnections, as shown in Figure 7-15, the coupling coefficient could be increased to 0.49, and the switching loop inductance could be reduced to only 2.7 nH, according to the Q3D simulation.

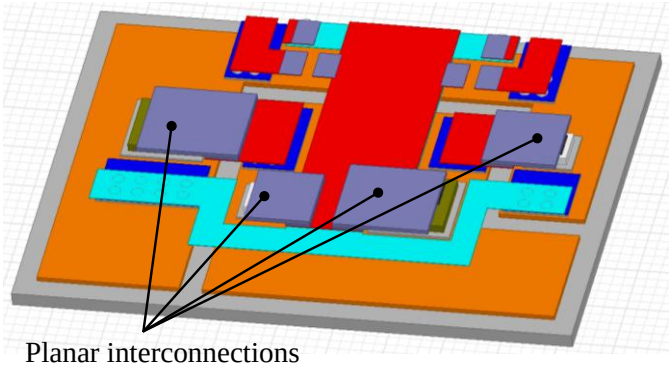


Figure 7-15. Planar interconnections for the module to improve coupling coefficient

Bringing copper layers closer in the PCB is another way to reduce leakage inductances and improve coupling. While FR-4 will experience insufficient dielectric strength below 5 mils, the laminate materials commonly seen in flexible PCBs, such as Kapton, can still provide enough breakdown voltage at a very small thickness (e.g. ≥ 4.5 kV/mil) [6]. The use of flexible PCBs has already been reported on low-voltage power modules, such as Flip-Chip on Flex package [7], and could also be extended to high-voltage SiC modules. For the discussed module in Figure 7-15, if a flexible PCB with 2 mils dielectric thickness were used to replace the original FR-4 version, a coupling of 0.51 could be achieved, while the switching loop inductance could be further reduced to 2.3 nH.

For the module developed in this chapter, the PCB middle layer is designed in such a pattern that the induced current has to flow through the terminating resistors. For the mere purpose of higher coupling coefficient, however, an entire copper plane could be used instead to work as a shield layer. According to the Lenz's law, the magnetic flux of the switching loop will induce opposing eddy currents on this shield layer, whose generated flux partially cancels the change of the original flux, resulting in a smaller effective switching loop inductance. Because the eddy currents are not bounded on the

shield plane, a maximum coupling will be achieved naturally so that the effective switching loop inductance is smallest. For example, Ref. [8] reported that by inserting a copper shield right under the switching loop of a gallium-nitride power module, the loop inductance was reduced from 0.9 nH to 0.18 nH, which corresponded to a coupling coefficient as high as 0.9. For the discussed module in this work, a coupling coefficient of 0.71 and a switching loop inductance of 1.3 nH could be achieved if replacing the PCB middle layer with a copper plane, as shown in Figure 7-16.

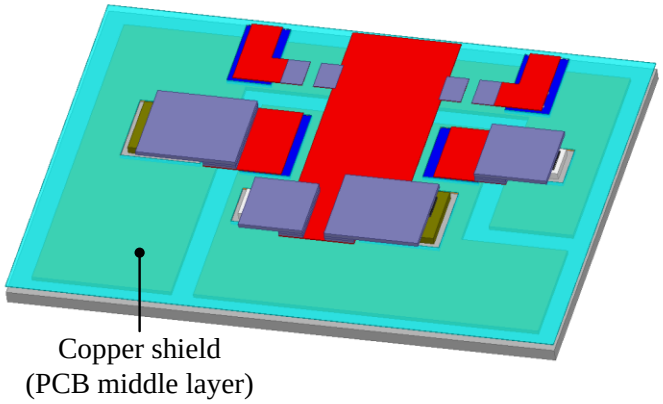


Figure 7-16. Copper shield for the module to improve coupling coefficient

Physically, the copper shield is equivalent to an almost lossless snubber loop, i.e. $R_S \approx 0\ \Omega$ in Figure 7-3, which may not provide the optimal damping effect according to the previous analysis. Therefore, a more resistive metal, such as nickel, could be used instead of copper to make the shield more lossy, which is similar to the idea used in the integrated transmission-line filter [9]. The mixed-metal, multilayer structure is obviously not available from the start-of-the-art PCB manufacturing process, but could be a meaningful future research topic.

Finally, Figure 7-17 summarizes the improvements in the coupling coefficient and switching loop inductance with the module structures proposed above.

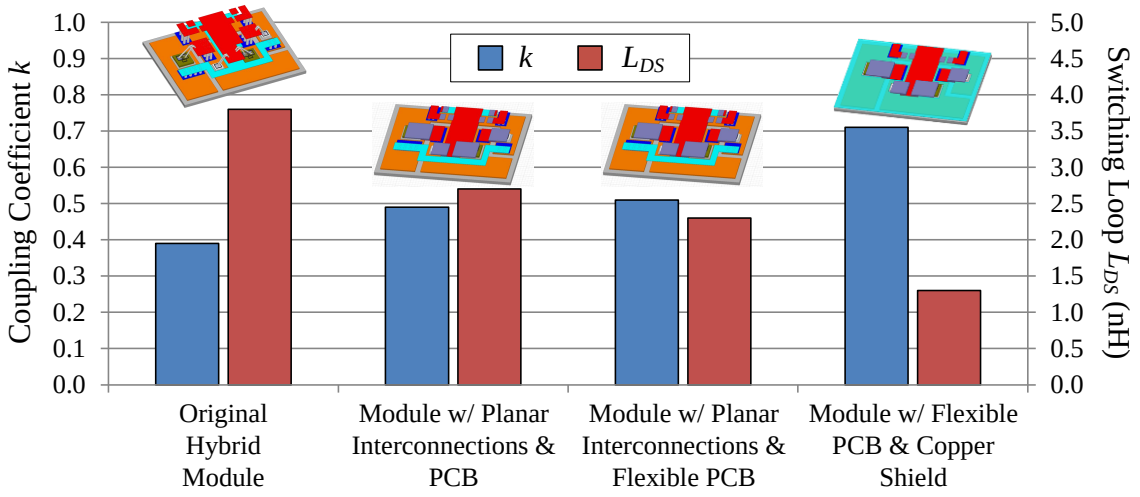


Figure 7-17. Summary of potential module structures to improve coupling coefficient and switching loop inductance

7.5 Conclusions

This chapter presents the concept of a switching loop snubber to suppress the parasitic ringing of power switches without increasing their conduction or switching losses. The concept has been verified in both simulation and experiments. The influences of snubber parameters on the damping effect have also been analyzed and discussed in detail using the small-signal model developed previously.

The snubber loop structure is then integrated in the hybrid phase-leg module to demonstrate its possible implementation in power modules, although the improvement in ringing is very small due to the loose coupling in the current module structure. Therefore, several potential structures are also proposed and discussed at the end of the chapter to improve the coupling coefficient and switching loop inductance for better damping effect.

7.6 References

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Chapter 8 Conclusions and Future Work

8.1 Conclusions

This dissertation systematically studies the electrical integration technologies for SiC power modules to be used in high-power-density applications, where high-temperature and/or high-frequency operations of devices are required. The main conclusions of the dissertation can be summarized in the following aspects.

8.1.1 SiC MOSFETs for High-Temperature and/or High-Frequency Uses

The extensive static and switching characterizations of the commercial SiC MOSFET have shown its superior electrical performances at high junction temperatures beyond the limit of Si devices. More specifically, the SiC MOSFET exhibits much smaller off-state leakage current, lower and less temperature-sensitive on-state resistance, and much faster and more temperature-stable switching waveforms compared to Si IGBTs, especially above 150 ℃. With their prices keeping falling down, SiC MOSFETs have become a very promising substitution for Si IGBTs to improve the performance and reduce the overall cost of power converters in current transportation applications. Furthermore, they also offer the capabilities of operating under even higher temperatures

and higher frequencies to meet the tough challenges of future high-power-density power conversion systems.

One potential problem of the SiC MOSFET that needs attention is its gate oxide stability under both high-gate-voltage and high-temperature stresses. The high-temperature gate biasing and gate switching tests conducted in this work reveal that the device characteristics do degrade after a short time under the extreme conditions, although degradations are not so severe in the latter case – a condition closer to the actual converter operations. The tests have also shown that, when degradations happen, the MOSFET's threshold voltage shifts and input capacitance decreases, which will affect the switching behaviors of the device. Fortunately, the blocking capability and on-state resistance are barely affected, meaning that the device will still be functioning as a switch normally, but with a reduced dynamic performance. In this sense, a design trade-off exists between the long-term reliability and the electrical performance of the SiC MOSFET. Future improvements on the device's gate oxide ruggedness, especially at elevated temperatures, are thus necessary before the device can be used in high-temperature systems on a large scale.

By comparing the state of the art Si and SiC power MOSFETs, it has been concluded that the SiC device needs quite different design considerations in many aspects than its Si counterpart. In terms of driving, the SiC MOSFET requires a higher turn-on gate bias to achieve the lowest $R_{DS(on)}$, and a negative turn-off bias to compensate for its low threshold voltage. Although the SiC device shows a much better figure of merit (FOM) in $Q_G \cdot R_{DS(on)}$ than its Si competitor, the comparison has shown that the switching speed of SiC MOSFET is still slower mainly due to its poor transconductance, which

significantly limits the driving speed. Therefore, high-frequency SiC converters suffer from a dominant amount of switching loss, which will limit the overall efficiency of the system if operating above 100 kHz. However, the SiC MOSFET still wins in terms of the temperature influence, thanks to its $R_{DS(on)}$ and switching energies that are much less temperature-sensitive. The device is thus much less prone to the thermal runaway issue often encountered by the Si MOSFET. For the above reasons, the SiC MOSFET will see more applications in high-voltage, high-power, and/or high-temperature systems.

8.1.2 Interactions between Semiconductor Devices and Circuit Stray Inductances

It is pointed out from the parametric study in Chapter 3 that the common source inductance originates from two mechanisms: (1) The shared current path between the main switching loop and the gate loop; and (2) the magnetic coupling between the two loops. The former mechanism is well understood and can be solved by using Kelvin connection for the gate drive circuit. The latter mechanism, however, is very often overlooked and is actually more critical in compact integrations of power converters. More attention thus needs to be paid to the circuit layout between the gate and switching loops, even if Kelvin connection is utilized.

The parametric study shows again that the switching loop inductance L_{DS} is the main participant in the MOSFET's turn-off ringing. Instead of deriving time-domain equations to explain the ringing, a small-signal model is developed to examine the phenomenon in the frequency domain. The model clearly shows that the parasitic ringing at turn-off is the voltage response of a parallel resonant network, formed by L_{DS} and the MOSFET's output capacitance C_{OSS}, under the excitation of turn-off di/dt. A direct relationship thus can be established between the parasitic ringing in the time domain and

the parallel resonance in the frequency domain. Using this model, the effect of DC decoupling capacitors in suppressing the ringing can be studied and explained in a simpler and deeper way than the previous time-domain analysis. A rule of thumb can also be derived on the proper selection of capacitance value for a sufficient decoupling effect. The frequency-domain analysis has been verified through both simulation and experiments. The conclusion about decoupling capacitors is further utilized and proved correct in the developments of both the wire-bond and hybrid modules in later chapters.

8.1.3 Integrated SiC Power Modules for High-Temperature and/or High-Frequency Applications

Besides advanced devices, the compatible gate drive and packaging method are another two critical factors towards the high-frequency operation. A high-speed gate drive circuit with negative turn-off bias and active Miller clamp function is designed in Chapter 4 to achieve fast switching of discrete SiC MOSFETs, while avoiding the potential phase-leg shoot-through induced by the Miller effect. The circuit is proved effective and is further used to drive the hybrid SiC phase-leg module in Chapter 6 to its speed limit successfully.

By understanding the mechanism of parasitic ringing, it is natural to see that the conventional phase-leg layout, i.e. grouping devices by the switch and its anti-parallel diode, does not generate the best switching performance. Instead, the devices in a phase-leg should be grouped by switch pairs (i.e. the switch and its commutating diode) to minimize switching loop inductances. This proposed layout is firstly implemented on the PEBB PCB in Chapter 4, and later on the wire-bond module substrates in Chapter 5. In

both cases, smaller parasitic ringing and improved switching waveforms can be observed compared to the conventional layout design.

In integrated wire-bond power modules, the stray inductances associated with internal DC bus bars bring additional problems. As Chapter 5 has shown, DC terminals will constitute 50% or more in the module's total stray inductance even if they are designed in a laminated structure. In such a condition, placing DC decoupling capacitors directly on the module substrates will be much more effective than placing them across the module terminals. In Chapter 5, the embedded capacitors are selected by the concluded rule of thumb and are implemented on both 60 A and 120 A modules. Both modules show much cleaner drain and gate voltage waveforms than without these capacitors. The drain current, though not measurable from the module terminal, will also carry much less ringing as predicted by the modeling and simulation approach adopted in this work.

When including all of the above considerations in the module design, i.e. improved substrate layout, laminated DC bus bars, and embedded decoupling capacitors, the wire-bond module can still achieve faster switching speed without sacrificing in the parasitic ringing. Chapter 5 has shown that the developed 1200 V, 120 A SiC MOSFET phase-leg module allows the devices to be switched twice as fast with only one-third device over-voltages compared to a commercial 1200 V, 100 A module, which is designed in the traditional way.

To further reduce parasitics and footprint of SiC power modules, a new hybrid packaging structure is also proposed in this work. As a combination of planar and wire-bond packaging, the hybrid module achieves the same footprint as and similar parasitics

to a planar module, and meanwhile can be fabricated like a wire-bond module without double-sided solderability from the device. It is also demonstrated that, with this proposed structure, the SiC MOSFET can be switched to its speed limit without suffering from excessive ringing. In other words, the hybrid packaging has again turned the device itself to be the speed bottleneck.

A switching loop snubber circuit is also discussed at the end of this dissertation. The proposed snubber suppresses the parasitic ringing by picking up and damping the magnetic flux generated by the switching loop inductance, and thus does not affect either conduction or switching losses of the device. The concept has been analyzed in detail, and is verified in both simulation and experiments. The initial attempt to integrate such a circuit into a power module is presented, although the improvement is not pronounced. Possible improvements in module structures are also proposed to intrigue future researches.

The high-temperature capability of SiC power modules is more closely related to the packaging materials. An extensive literature survey has been carried out in this work to compare and select appropriate materials to achieve 200 and 250 ℃ operations of the SiC MOSFET phase-leg modules and the SiC JFET rectifier module. Since the focus of this work is on the electrical aspects of high-density integration, not too much research has been done in the material field. However, it is totally agreed that investigating the high-temperature capability and thermal cycling reliability of these materials is as critical as understanding the semiconductor devices for high-temperature power modules.

8.2 Future Work

Based on the above conclusions, the following aspects can be considered for further research.

(1) FOM for SiC devices

The popular FOM of $Q_G \cdot R_{DS(on)}$ is often used to highlight the superiority of SiC devices compared to their Si counterparts [1]. However, as pointed out in this work, two critical and perhaps limiting parameters of SiC switches (particularly MOSFETs) are not included in this FOM: The transconductance g_{fs}, and the output capacitance C_{OSS}. Therefore, a new FOM may be necessary to perform more fair comparison between Si and SiC power switches.

(2) Active gate drive for SiC MOSFETs

The turn-on speed of SiC MOSFET is mainly limited by its high gate plateau level and the fixed turn-on bias voltage, according to Eq. (2-3). If the turn-on bias could be higher than 20 V before the plateau phase ends and return to 20 V afterwards, the turn-on speed could be increased without breaking down the gate oxide layer. An immediate solution is to parallel a capacitor to the gate resistor to provide gate voltage spikes during both turn-on and turn-off. A better solution is to develop an active gate drive circuit that can detect the dv/dt of the SiC MOSFET, which is dependent on the load condition, and provide only necessary length of higher turn-on bias.

(3) Embedded current sensor for SiC power modules

With the decoupling capacitors inside the module, the terminal currents no longer represent the real device currents. An embedded current sensor that can measure switching currents will thus make it more convenient to evaluate the module's switching

losses under various driving speeds. The current sensor needs to carry large currents with minimum conduction loss, and provides high enough bandwidth to capture the fast *di*/*dt* accurately.

(4) Integration of gate drive ICs on modified hybrid module

As mentioned in Chapter 6, the PCB structure in the modified hybrid module makes it possible to integrate gate drive ICs directly inside the module. By doing so, an integrated PEBB will become more realistic.

(5) Improvement of coupling coefficient for the integrated snubber circuit

The potential improvements suggested at the end of Chapter 7 could also be very meaningful future researches.

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