Power Converter and Control Design for High-Efficiency Electrolyte-Free Microinverters

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ABSTRACT

Microinverter has become a new trend for photovoltaic (PV) grid-tie systems due to its advantages which include greater energy harvest, simplified system installation, enhanced safety, and flexible expansion. Since an individual microinverter system is typically attached to the back of a PV module, it is desirable that it has a long lifespan that can match PV modules, which routinely warrant 25 years of operation. In order to increase the life expectancy and improve the long-term reliability, electrolytic capacitors must be avoided in microinverters because they have been identified as an unreliable component. One solution to avoid electrolytic capacitors in microinverters is using a two-stage architecture, where the high voltage direct current (DC) bus can work as a double line ripple buffer.

For two-stage electrolyte-free microinverters, a high boost ratio dc-dc converter is required to increase the low PV module voltage to a high DC bus voltage required to run the inverter at the second stage. New high boost ratio dc-dc converter topologies using the hybrid transformer concept are presented in this dissertation. The proposed converters have improved magnetic and device utilization. Combine these features with the converter's reduced

switching losses which results in a low cost, simple structure system with high efficiency. Using the California Energy Commission (CEC) efficiency standards a 250 W prototype was tested achieving an overall system efficiency of 97.3%.

The power inversion stage of electrolyte-free microinverters requires a high efficiency grid-tie inverter. A transformerless inverter topology with low electro-magnetic interference (EMI) and leakage current is presented. It has the ability to use modern superjunction MOSFETs in conjunction with zero-reverse-recovery silicon carbide (SiC) diodes to achieve ultrahigh efficiency. The performance of the topology was experimentally verified with a tested CEC efficiency of 98.6%.

Due to the relatively low energy density of film capacitors compared to electrolytic counterparts, less capacitance is used on the DC bus in order to lower the cost and reduce the volume of electrolyte-free microinverters. The reduced capacitance leads to high double line ripple voltage oscillation on DC bus. If the double line oscillation propagates back into the PV module, the maximum power point tracking (MPPT) performance would be compromised. A control method which prevents the double line oscillation from going to the PV modules, thus improving the MPPT performance was proposed.

Finally, a control technique using a single microcontroller with low sampling frequency was presented to effectively eliminate electrolyte capacitors in two-stage microinverters without any added penalties. The

effectiveness of this control technique was validated both by simulation and experimental results.

Dedication

In memory of my mother, JinFeng Zhu (1954-2008), whose courage and diligence continue to inspire.

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Chapter 1 Introduction

1.1 Research background and motivations

The electrical energy consumption continues to grow as more human activities are dependent on electricity. Due to the depletion of fossil fuels and increasingly serious environmental pollution, the demand for the utilization of renewable energy sources to generate electricity is increasing. Among these renewable energy sources, photovoltaic (PV) energy has experienced remarkable growth over the past decade. The world's cumulative PV capacity has achieved 102 GW in the year 2012 and would expected to reach 288 GW in 2017 [A1].

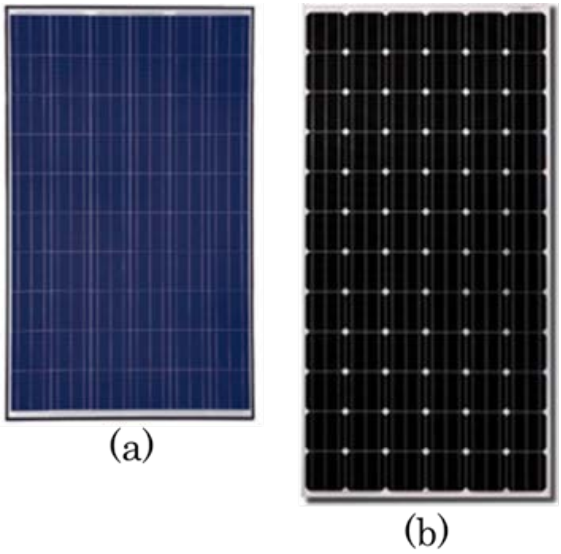


Figure 1.1 Photograph of two mono-crystalline photovoltaic (PV) modules: (a) 60 cells, and (b) 72 cells [F7].

The PV energy generated from sunlight is captured by PV modules in Figure 1.1, which are composed of a cluster of PV cells in series. The power

generated by the PV modules are electric DC power. Integrating the DC power from the PV modules into the existing 'alternating current' (AC) power distribution infrastructure can be achieved through grid-tie inverters. The inverters must guarantee that the PV modules are operating at the maximum power point (MPP), which is the operating condition where the most energy is captured. Another function for inverters to implement is the need to control the current injected into the AC grid synchronous with the grid voltage at the lowest harmonic distortion levels. Therefore PV inverters have a huge impact on the performance of PV grid-tie systems.

Depending on different levels of MPPT implementation for PV modules, several PV inverter technologies coexist [B1]. As shown in Figure 1.2(a), centralized inverters, which are normally three-phase connected, interface a large cluster of parallel-connected PV strings into the grid. Each PV string is composed of a large number of modules in series, generating high voltage to allow the grid-connected operation of centralized inverters. Centralized PV systems have some limitations, such as: high voltage DC cables between PV strings and the inverter, mismatch losses due to centralized MPPT, losses in the string diodes and risks of hotspots in the PV modules during partial shading. String and multi-string inverters, as shown in Figure 1.2(b) are distributed version of the centralized inverters, where each single string of PV modules are independently managed. String-level power process of PV modules can eliminate the cost intensive DC cabling. There are no losses

associated with string-diodes and string-level MPPT is assumed to increase the overall efficiency, when compared to the centralized inverters.

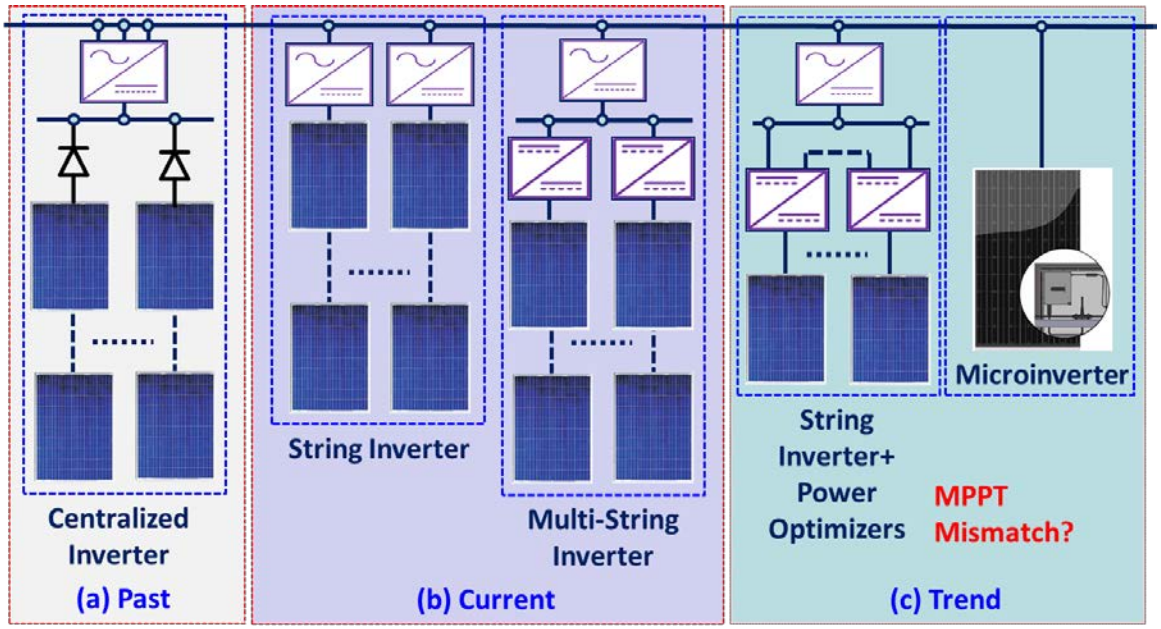


Figure 1.2 PV grid-tie inverter systems.

In order to overcome the mismatch losses between PV modules of traditional string and multi-string inverter architectures, two new PV grid-tie inverter concepts, as shown in Figure 1.2(c) have been developed. A circuit called a power optimizer, which is a dc-dc converter embedded into PV modules of traditional string PV inverter systems. This increases the system energy output for PV modules by constantly tracking the MPPT of each module individually. However, the mismatch losses may still exist due to the series connection of power optimizers.

Microinverter, as shown in Figure 1.2(c), converts the DC power from each individual PV module directly to the AC gird. For PV systems using microinverters, they have the advantage of reducing the impact of shading,

debris or snow covering the PV module, which would reduce the power output. Each microinverter harvests optimum power by performing MPPT for its connected module, eliminating the mismatch losses in PV systems. The installation of each microinverter for an individual PV module can simplify system installation, reduce maintenance cost, and allow flexible upgrade.

The main criteria for widespread adoption of microinverters in PV industry are low cost, high conversion efficiency, and long lifespan. Electrolyte capacitors have been identified as one of the limiting components which determine the lifespan of PV grid-tie inverters [A13]-[A18]. Since microinverters are typically attached to the back side of the PV module, this exposes an individual microinverter to high temperatures causing accelerated operational degradation. So the electrolyte capacitors must be avoided to design a long-lifespan microinverter.

The motivations of this research project are to address the high-efficiency, improved lifespan and low-cost challenges of the microinverters.

1.2 State-of-the-art microinverter technologies

This section will give a review of existing microinverter topologies. The techniques used to eliminate electrolytic capacitor are also studies.

1.2.1 Reviews of the existing microinverter topologies

Microinverters can be categorized into three groups according to the different DC-link configurations: with a DC link, pseudo DC link, and without a DC link, as shown in Figure 1.3 [B2].

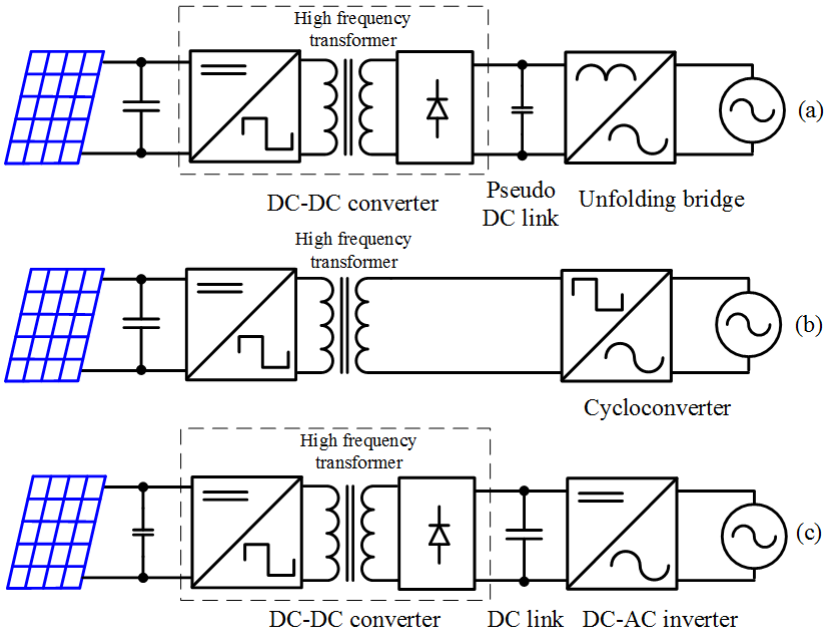
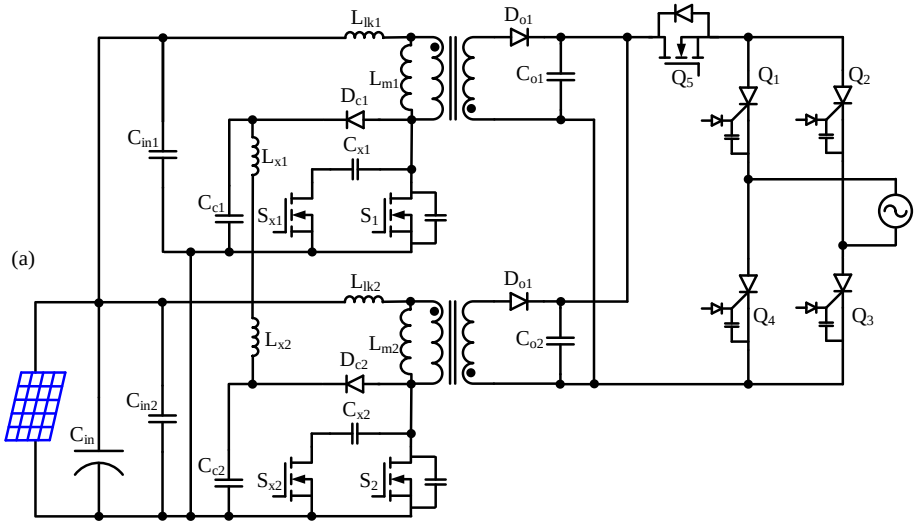


Figure 1.3 Three different types of microinverters.

I) Microinverters with a pseudo DC link

Figure 1.3(a) shows microinverters with a pseudo DC link. The mode of operation for the pseudo DC link microinverter is where the voltage on the pseudo DC link has a rectified sinusoidal waveform, then an unfolding inverter operating at line frequency, which converts the rectified-sine waveform into the sine waveform synchronized with the grid voltage. Normally, the microinverters with pseudo DC links also referred as single-stage microinverters since only the first dc-dc stage works with high-frequency. Quite a few single-stage microinverter topologies have been proposed [F3], [B4]-[B21], as shown in Figure 1.4. The most popular topology for the dc-dc stage is the flyback converter [F3], [B4]-[B20] due to its buck-boost gain feature and simple structure. The dc-dc stage of topology in Figure 1.4(a), [F3], [B4]-[B11] is an interleaved quasi-resonant flyback converter

followed by a full-wave unfolding stage. The quasi-resonant operation dc-dc stage can reduce the switching losses and allow the microinverter to run at higher switching frequencies. The two interleaved units of the dc-dc stage run together at high power to reduce the conduction losses. When the grid side power is low only one unit runs to limit the switching frequency and reduce the core loss. The dc-dc stage in Figure 1.4(b) is also a flyback converter, however a center-tapped transformer [B12]-[B16] is used as the unfolding stage to generate the sinusoidal waveform. Some topologies used active-clamping techniques [B17]-[B20] to capture the leakage energy of the flyback transformer, the downsides to this approach is that there are higher circulating losses and higher number of components. The dc-dc stage of the topology in Figure 1.4(e) is a buck cascaded boost converter, which works as boost converter at high grid line voltage and as buck converter at low grid line voltage.



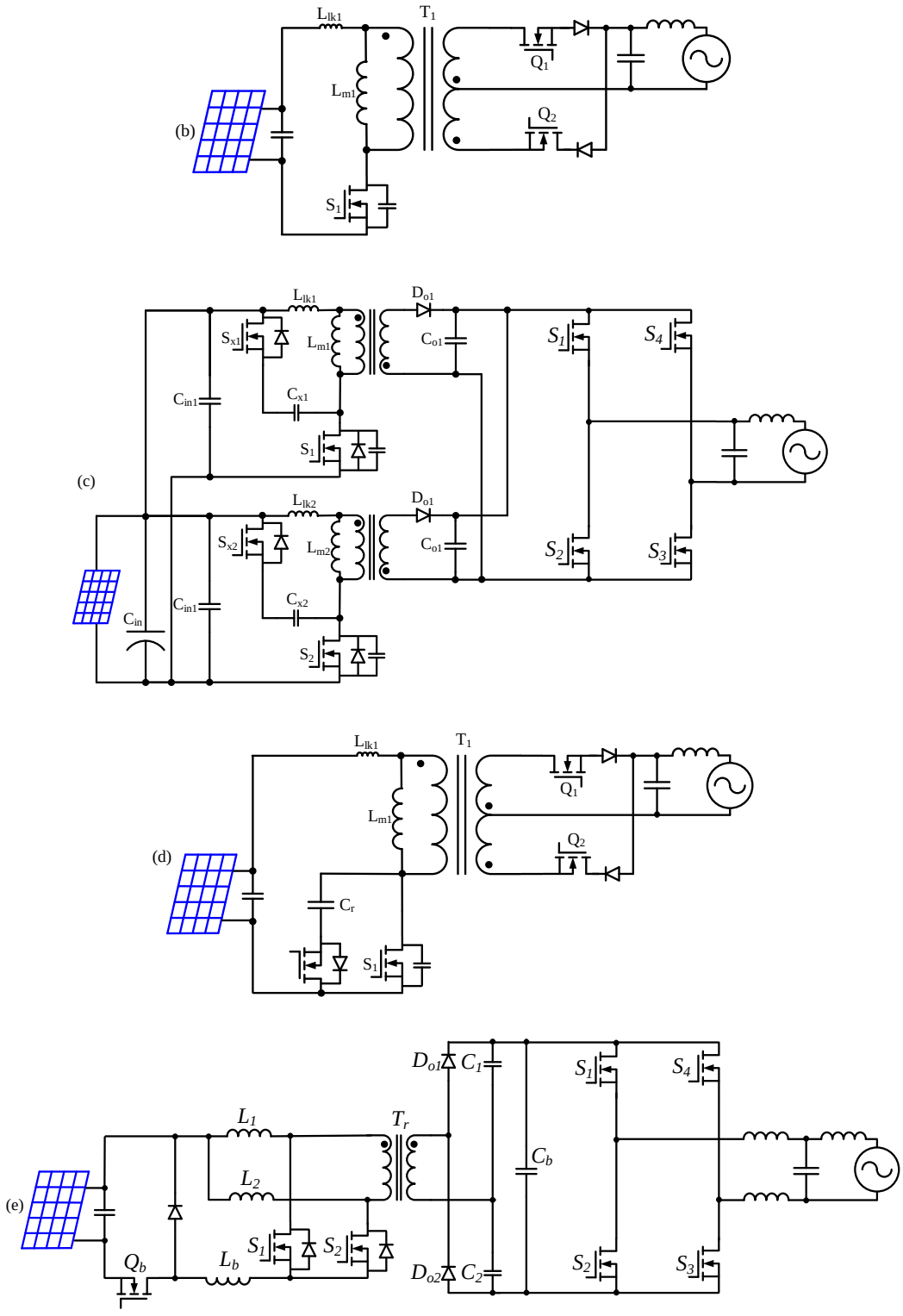


Figure 1.4 Microinverters with a pseudo DC link.

II) Microinverters without DC link

If removing the rectifier diodes and replacing the unfolding bridge with a cycloconverter, microinverters can be implemented without using DC link, as show in Figure 1.3(b). The microinverter topologies using cycloconverters are shown as in Figure 1.5, where the low voltage DC voltage is changed to a high frequency AC voltage and amplified to a higher level compatible with the AC grid. A cycloconverter directly converts the AC voltage or current with high-frequency to grid frequency. Due to the high stresses on the AC bidirectional switches and complex control, the development of this type of microinverter is limited.

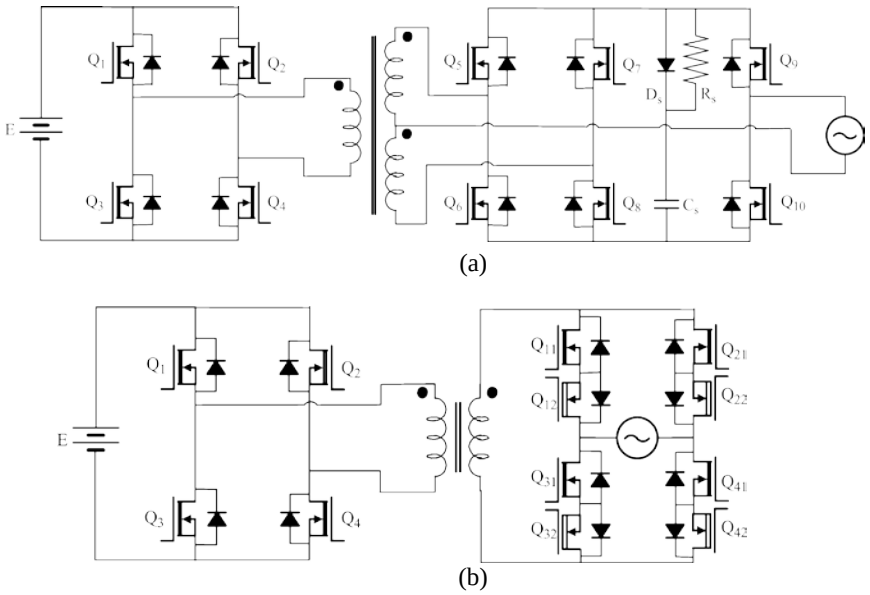
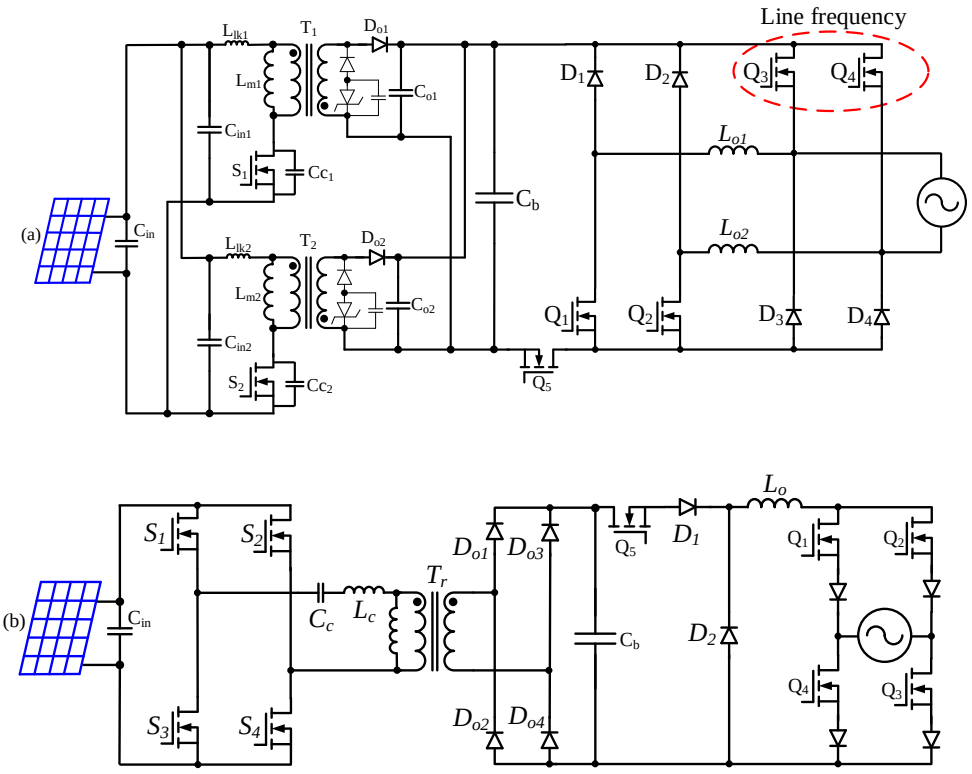


Figure 1.5 Microinverters using cycloconverter technologies [B22], [B23].

III) Microinverters with DC link

Microinverters with DC link, as shown in Figure 1.3(c), are referred to as two-stage microinverters, where both dc-dc and dc-ac stages work at high frequency. The dc-dc stage boosts the low voltage of the PV module to a high DC bus voltage compatible with the AC grid voltage to run the dc-ac inverter.

Normally, the dc-ac stage is a full-bridge inverter, [F4], [B24]-[B29], while the dc-dc stage can be a high boost ratio voltage-fed [F4], resonant [B24], [B25] or current-fed [B26]-[B29] converter. The dc-ac full-bridge inverter normally requires careful design considerations [F4], [B24]-[B27], [B29] to use modern high speed MOSFET devices to achieve high efficiency. The dc-dc stage can use soft-switching techniques, like quasi-resonant [F4], resonant [B24], [B25] or active-clamping [B26], [B28] to reduce the switching losses and achieve high efficiency.



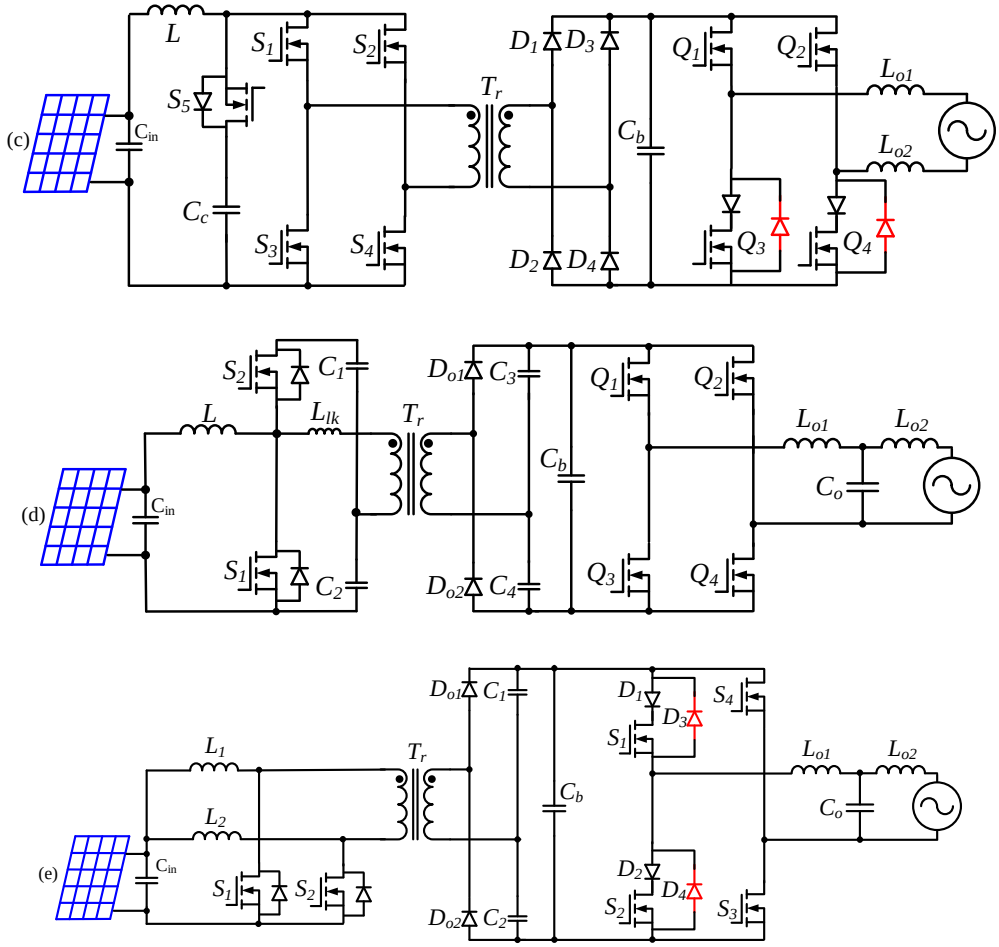


Figure 1.6 Two-stage microinverters.

1.2.2 Techniques to eliminate electrolytic capacitors in microinverters

Microinverters have a power level ranging from 150 W to 300 W, normally use a single-phase connection to the grid. For a single-phase system, the PV-side power is

$$P_{PV} = V_{PV} \times I_{PV} \tag{1.1}$$

which is a DC power. The grid-side power is

$$P_g(t) = P_{g\_avg} + P_{g\_avg}\cos(2\omega_g t) \tag{1.2}$$

which is composed of a DC average power plus a double line ripple power. As shown in Figure 1.7, a basic electrical feature of a single-phase system is that the energy delivered includes both an average power that transfers useful energy and a double line ripple power that flows back and forth in the system. So the energy storage components that are required in single-phase microinverters used to store and retrieve this double line ripple energy must satisfy the power balance of the system.

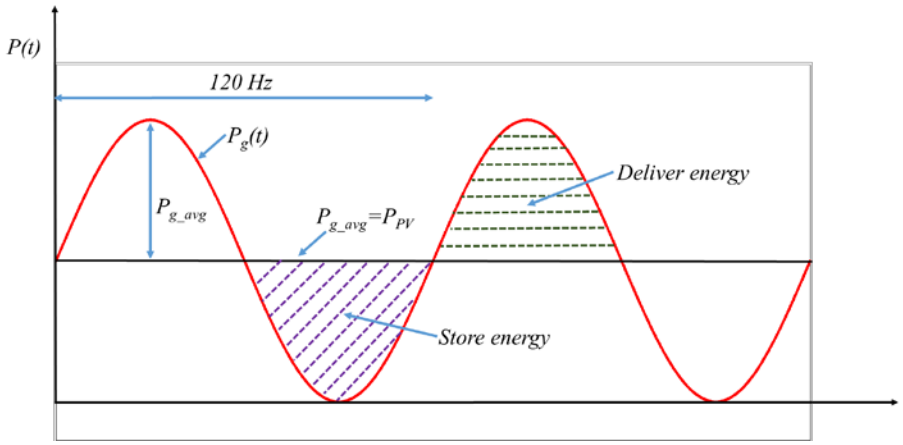


Figure 1.7 Grid side power and its decomposition.

The most commonly-used energy storage component in microinverters are large electrolytic capacitors due to its high energy density. For example, as shown in Figure 1.8, a commercial 175 W microinverter M190-72-240 from Enphase [F3] requires 5×1.8 mF for a total capacitance of 9 mF. This electrolyte capacitor bank is used to buffer the double line ripple from going to the PV module. In order to increase the life expectancy and improve the long-term reliability, electrolytic capacitors need to be avoided in microinverters [A13]-[A17].

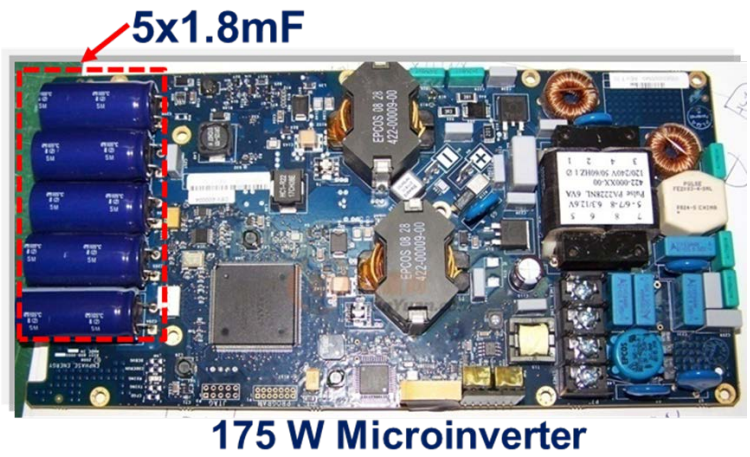


Figure 1.8 Commercial 175 W microinverter M190-72-240 from Enphase [F3], which requires 9 mF of electrolyte capacitors to buffer the double line ripple.

Different techniques have recently been presented to employ film capacitors as energy storage components in single-phase microinverters to increase the lifespan [B3], [B30]-[B37]. These techniques can be categorized three types: PV-side, dc-link, and ac-side decoupling techniques [B3]. Among these three techniques, PV-side and ac-side decoupling techniques requires adding extra circuits, as shown in Figure 1.9, to buffer the double line ripple energy. However this results in cost increase, overall efficiency reduction, and control complexity [B3]. Figure 1.10 shows the dc-link decoupling technique used for single-phase two-stage (SPTS) microinverters that can use the film capacitors as intermediate dc bus capacitors without adding extra circuits [B3], [F4]. Although SPTS microinverters have one more energy transfer stage than single-stage ones, the efficiencies can be comparable to single-stage microinverters by using soft-switching techniques, new converter topologies and modern high performance semiconductor devices. One example

of a two-stage microinverter with high efficiency by the company Power-One Inc., is shown in Figure 1.11, with a reported CEC efficiency of 96% for a power range of 300 W [F4]. This product illustrates that the two-stage architecture is an optimal solution to eliminate the electrolytic capacitors compared to using the "ripple port" technique.

Since SPTS electrolyte-free microinverters have one additional energy transfer stage compared to the single-stage microinverters, both the high boost ratio dc-dc converter and the dc-ac inverters are required to have high efficiency to achieve high system efficiency.

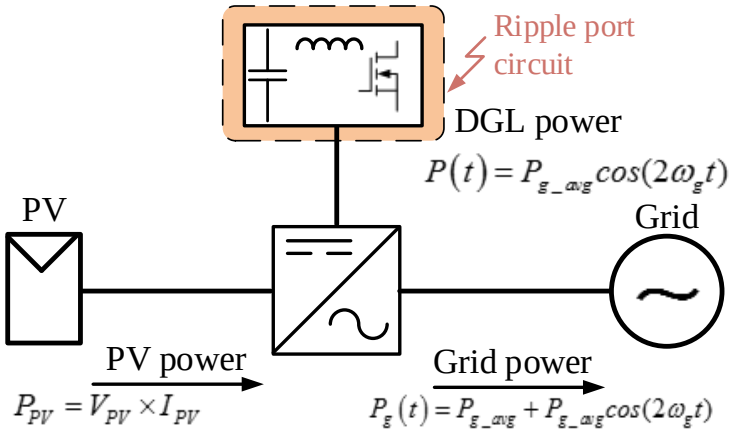


Figure 1.9 Extra ripple power circuit used to buffer the double line ripple power and eliminate electrolytic capacitors in single-stage microinverters with PV-side and AC-side buffing techniques.

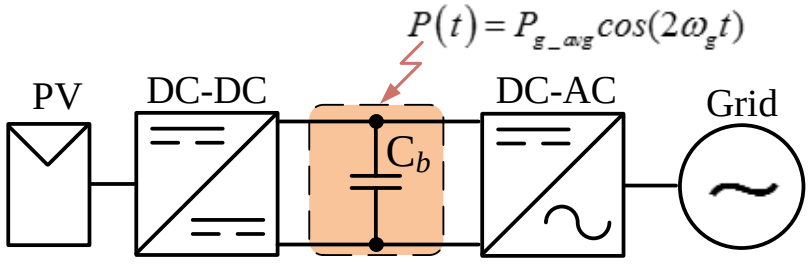


Figure 1.10 Single-phase two-stage microinverters using high voltage intermediate DC bus capacitor C_b as double line ripple power buffer.

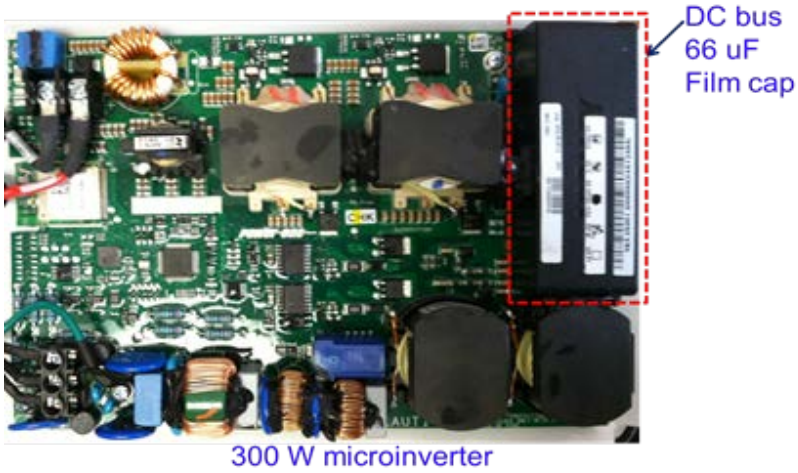


Figure 1.11 commercial 300 W electrolyte-free microinverter MICRO-0.3-I from Power-One Inc. [F4].

1.3 Objectives of the research project

Although the advantages of microinverters have been recognized, wide adoption of microinverters still presents many challenges. The research work in this project is to address these challenges with the following objectives.

- **High CEC efficiency**

A growing demand for maximized energy extraction from PV sources have stimulated substantial technology development efforts towards high-

efficiency PV grid-tie inverters. The efficiency of PV inverters is weighted for specific power levels in the California Energy Commission (CEC). The individual efficiencies, at 10%, 20%, 30%, 50%, 75%, and 100% of nominal power, are weighted and summed up according to:

$$\eta_{CEC} = 0.04\eta_{10\%} + 0.05\eta_{20\%} + 0.12\eta_{30\%} + 0.21\eta_{50\%} + 0.53\eta_{75\%} + 0.05\eta_{100\%} \qquad (1.3)$$

Today's string inverters based on innovative transformerless technologies [D5]-[D16] have reached a CEC efficiency of 98% [D7]. With the latest SiC devices, the CEC efficiency of transformerless inverters have the potential to improve [D8]. Today's commercial PV microinverters normally have a CEC efficiency that ranges from 93.5% to 96.0% [F3]-[F6]. In order to achieve a system CEC efficiency over 95%, the first-stage high boost ratio dc-dc converter must have a CEC efficiency over 97%.

- **Low electronic cost, high power density and low profile**

Figure 1.12 shows the cost breakdown of a 5 kW residential PV system in year 2010, the total cost of which is $5.71/W [A3]. Breaking down the total cost, the inverter hardware accounts for 7% and the installation labor accounts for about 30%. This PV system used the string technology, where a cluster of PV modules share a common inverter. If microinverters are used, each PV module requires its own dedicated microinverter, which leads to increased electronics costs compared to the system using string technology. With the continuous decreasing price of PV modules [A4], the cost of PV inverters and installation labor are becoming more dominant in the overall

system cost. As a result of the SunShot target \$1.5/W in 2020 [A3], cost reduction of microinverters becomes more stringent. Microinverters should be designed with high power density and low profile to make integration with the PV module easier and reduce the installation labor cost.

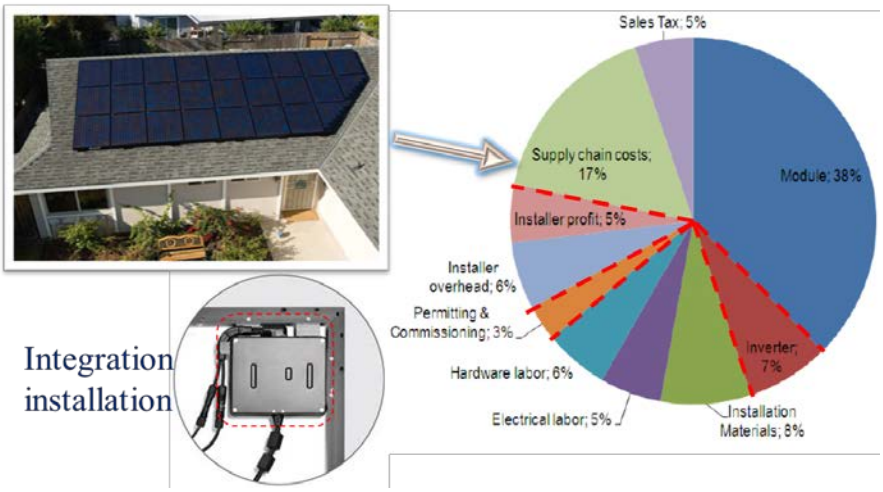


Figure 1.12 Cost breakdown in year 2010 for 5 kW residential PV system with one string inverter: total \$5.71/W; DOE SunShot target is \$1.5/W in 2020 [A3].

- **No electrolytic wear-out mechanism**

In order to fairly compare the capital invested on a PV project, the levelized cost of energy (LCOE) instead of initial investment cost is normally used to evaluate the system cost, which is defined as [A15]

$$\text{LCOE} = \frac{\text{Total Life Cyle Cost}}{\text{Total Lifetime Enegy Production}} = \frac{\sum_{n=0}^{N} \frac{C_n}{(1+d)^n}}{\sum_{n=0}^{N} \frac{Q_n}{(1+d)^n}} \tag{1.4}$$

where C_n is the cost for installation, module, balance of the system, inverter, finance in year n; Q_n is produced energy in year n; N is the lifetime of the system; d is the discount rate.

Lowering LCOE requires not only reducing the electronic cost but also increasing the lifespan of the microinverters. The improved lifespan provided by the avoidance of electrolytic capacitors saves the maintenance and repair costs. This can in turn contribute to the reduction of LCOE of the systems.

- **Improved MPPT performance and grid current quality**

Although film capacitors have far more lifetime, the energy density of film capacitors are much lower compared to the electrolytic counterparts. In order to reduce the volume and save the cost of the microinverters, the capacitance must be reduced. This will lead to high double line ripple oscillation on the DC bus. The propagation of this double line oscillation back to PV module will compromise the MPPT performance. Also if this double line oscillation goes to the grid side, the grid current will be distorted. So advanced control techniques are required to reject the propagation of this double line ripple oscillation to PV side and grid side to improve the MPPT performance and grid current quality.

1.4 Major contributions and outline of the dissertation

High boost ratio dc-dc converters using hybrid transformer with CEC efficiency over 97% are proposed in this project. The magnetic core in the proposed converter combines the functions of traditional transformer and

coupled-inductor. As a result, the power device utilization is improved and magnetic core utilization is optimized compared to traditional transformer-isolated or coupled-inductor high boost ratio dc-dc converters. As a result of incorporating the resonant operation mode into the traditional high boost ratio pulse-width modulation (PWM) converters, the turn-off and turn-on losses of the switches are reduced. The improved power device utilization can reduce the cost of the converter, the optimized magnetic utilization allows the converters to use smaller magnetic core, and the reduced switching losses can increase the efficiency of the converters under all load conditions. Therefore, the proposed converters are attractive for the microinverter applications. Experimental results validate the performance of the proposed converters.

A transformerless MOSFET inverter topology with CEC efficiency 98.6% is presented. The proposed topology works separately during the positive and negative half grid line cycle using a split-phase structure, which eliminates the shoot-through issue of traditional full-bridge inverters. The body diode reverse recovery issue of MOSFET devices are also avoided and fast-speed superjunction MOSFET devices can be employed to achieve ultrahigh efficiency. The effectiveness of the proposed topology is experimentally verified.

An average model of the high boost ratio dc-dc converter is derived. A control technique is proposed to reject the double line ripple voltage oscillation on the PV module, improving the accuracy of the MPPT.

Simulation and experimental results validate the control design. The system model of single-phase two-stage microinverter is derived. A control technique only using simple low cost microcontroller with low sampling frequency to eliminate the electrolytic capacitors without any added penalties is presented. Detailed control methodology is depicted and design guideline is suggested. Experiments are performed and the results are utilized to validate the effectiveness of the proposed control technique.

The dissertation will be organized as following:

Chapter2-The high boost ratio dc-dc converter for SPTS microinverters requires high efficiency over wide power range, low cost and simple structure. A historical review of the existing coupled-inductor, current-fed and resonant high boost ratio dc-dc converter topologies shows that none of them can satisfy these requirements simultaneously. A new high boost ratio dc-dc converter using hybrid transformer concept suitable for microinverter applications is presented. The operation principle of the proposed converter is discussed and a design guideline is suggested. The experimental results are given to justify the effectiveness of the proposed converter. Finally, a family of hybrid transformer dc-dc converters are presented by using basic "resonant voltage doubler" (RVD) cell.

Chapter3-This chapter evaluates the performance of the hybrid transformer dc-dc converters through power device utilization (PDU), magnetic utilization (UD), switching loss characteristics and cost-effectiveness. These evaluations

prove the suitability of hybrid transformer dc-dc topologies for PV microinverter applications.

Chapter4-This chapter analyzes the performance of single-phase transformerless inverter with regards to the efficiency, EMI and leakage current. A review of existing transformerless inverter topologies is presented. The analysis of the loss models for power semiconductor devices used in grid-tie inverter show that using latest superjunction MOSFETs and SiC devices ultrahigh efficiency can be achieved in transformerless inverters. Then a new high reliability and high efficiency transformerless inverter topology that can use superjunction MOSFETs and SiC devices to achieve ultrahigh efficiency is presented.

Chapter5-This chapter analyzes the energy storage requirements in single phase PV inverters. Effects of double line ripple on MPPT accuracy and grid current distortion are elaborated. The small-signal model of the hybrid transformer dc-dc converter using approximate state-space averaging model is derived. A control method to rejection the double line ripple oscillation on the PV module is presented and experimentally justified. The system model of SPTS microinverter is derived. A control technique which can eliminate electrolyte capacitors without any added penalties in microinverter is presented. Experiments are performed and the results justify the effectiveness of the proposed control technique.

Chapter 6- Major results and contributions of this research project are summarized. Based upon the implementation experience and experimental results, future works are directed.

Chapter 2 Hybrid Transformer High Boost Ratio DC-DC Converter Topologies

Solar energy is becoming a mainstream source of electricity. Integrating the solar energy from the PV modules into the existing power distribution infrastructure requires grid-tie inverters. Microinverter, which performs MPPT for each individual PV module and directly feeds ac power from the PV modules to the existing ac grid is becoming a new trend. Microinverter is typically attached at the back, or may be seamlessly integrated onto the metal frame of PV module, hence it is highly desirable that microinverters have a long lifespan that can match PV modules, which routinely warrant 25 years of operation [A13]-[A18], [F7].

The electrolytic capacitors have been identifies as one of the most unreliable components in PV grid-tie inverters [A14]-[A17]. Hence it is desirable to avoid the electrolytic capacitors in microinverters. Two techniques are commonly used to eliminate electrolytic capacitors [B3]. One is “ripple port” technique, which added an additional ripple port circuit buffer the double line ripple power [B3]. However this leads to efficiency suffering, cost penalty and control complexity. Another technique is using two-stage architecture, where the inherent high voltage DC bus can be used as energy buffer to reduce the capacitance requirements hence allowing to use low-capacitance film capacitors. The two-stage technique does not require additional circuits, which avoids cost and complexity penalties [B3].

In two-stage architecture, a high boost ratio dc-dc converter is required to increase the low PV module voltage to a high DC bus voltage for following stage grid-tie inverter. This chapter proposes a new high boost ratio dc-dc converter using hybrid transformer concept, which has advantages of high efficiency over wide input voltage and output power range, smaller size, low cost and low component counts. Experimental results based on a 250 W prototype board justify the effectiveness of the proposed converter. By introducing resonant voltage double (RVD) cell into traditional coupled-inductor PWM converters, a group of hybrid transformer dc-dc converters suitable for microinverters are derived and the performance of these converters are compared.

2.1 Specifications and demands

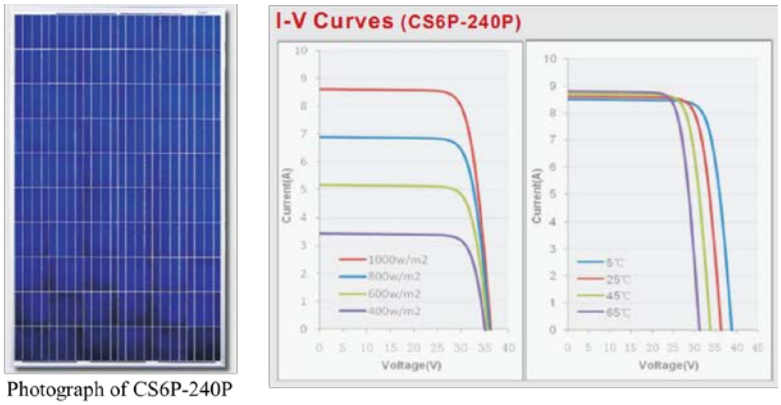
In order to verify the performance of the designed microinverter, PV module CS6P-240P from CanadianSolar Inc. [F7] were ordered for system integration and field demonstration test, which has 25-year module power output warranty with the electrical specifications as shown in Figure 2.1. The nominal maximum power P_{max} is 240 W with optimum operation voltage V_{mp} 29.9 V, open circuit voltage V_{oc} 36.6 V under standard test conditions (STC) of irradiance of 1000W/m^2, spectrum AM 1.5 and cell temperature of 25^{o}C. Figure 2.2 shows a cluster of typical I-V curves of CS6P-240P module under different irradiance and cell temperature conditions. There is only one MPP on each curve, which needs the dc-dc converter to accomplish the tracking of

this point. In order to maximize the energy capture from the PV modules, the dc-dc converter needs to have high efficiencies over wide input voltage and output power ranges.

Electrical Data		CS6P-220P	CS6P-225P	CS6P-230P	CS6P-235P	CS6P-240P
Nominal Maximum Power at STC (Pmax)		220W	225W	230W	235W	240W
Optimum Operating Voltage (Vmp)		29.2V	29.4V	29.6V	29.8V	29.9V
Optimum Operating Current (Imp)		7.53A	7.65A	7.78A	7.90A	8.03A
Open Circuit Voltage (Voc)		36.6V	36.7V	36.8V	36.9V	37.0V
Short Circuit Current (Isc)		8.09A	8.19A	8.34A	8.46A	8.59A
Operating Temperature		-40℃~+85℃				
Maximum System Voltage		1000V (IEC) /600V (UL)				
Maximum Series Fuse Rating		15A				
Power Tolerance		+5W				
Temperature Coefficient	Pmax	-0.43%/℃				
	Voc	-0.34 %/℃				
	Isc	0.065 %/℃				
	NOCT	45℃				

Under Standard Test Conditions (STC) of irradiance of 1000W/m², spectrum AM 1.5 and cell temperature of 25℃

Figure 2.1 Electrical specifications of CS6P-240P PV module [F7].



Photograph of CS6P-240P

Figure 2.2 I-V curves of CS6P-240P PV module [F7].

The designed microinverter in this dissertation feeds the energy from the PV module to the grid through single-phase 240 V_{ac} 60 Hz system, which is normally available for U.S. residential houses. The microinverter has two main tasks under given PV module and grid electrical specifications:

- To amplify and invert the DC PV power with the voltage range from 20 V to 45 V and maximum power 250 W into a 60 Hz current to feed to 240 V_{ac} grid.

- To implement MPP to maximize the energy capture from the PV module

The configuration of two-stage microinverters as shown in Figure 2.3, has a high boost ratio dc-dc converter followed by a dc-ac inverter. The dc-dc conversion stage requires a high efficiency, high boost ratio dc-dc converter to increase the low dc input voltage from the PV module to a higher dc voltage. This voltage has to be higher than the peak output voltage of the dc-ac inverter, nominally in the 380 V-400 V range for the 240 V_{ac} grid system. The main reason why two-stage configuration was selected in this project is that the two-stage design can avoid electrolytic capacitors.

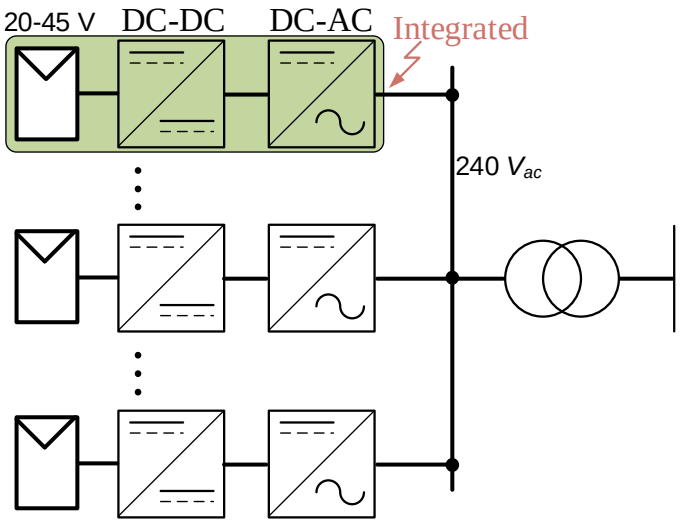


Figure 2.3 Microinverters with two-stage architecture.

2.2 Review of the state-of-the-art high boost ratio dc-dc converter topologies

This section gives a review of the state-of-the-art high boost ratio dc-dc converter topologies, including three groups according to the energy transfer mechanics. The pros and cons of each group of converters will be analyzed according to the suitability for the microinverter applications.

2.2.1 Coupled-inductor PWM converters

The first group of high boost ratio dc-dc converters are converters using coupled-inductors, as shown in Figure 2.4 [C1], [C7]-[C24]. The high boost ratio of this type of converters is from the transformer effect of the coupled-inductor. The structure of this type of converter is simple and duty ratio range is narrow even for wide input voltage applications as a result of the buck-boost gain feature. However, this type of converters has poor magnetic utilization, which results in high volume design for a given transferred power. The voltage stress of output diodes is equal to the output DC bus voltage plus the secondary-reflected input voltage. For two-stage micro-inverters, this voltage may be as high as 800 V, so normally 1200 V SiC diodes with zero reverse-recovery must be used to reduce the diode turn-off losses. However, this will lead to high cost penalty.

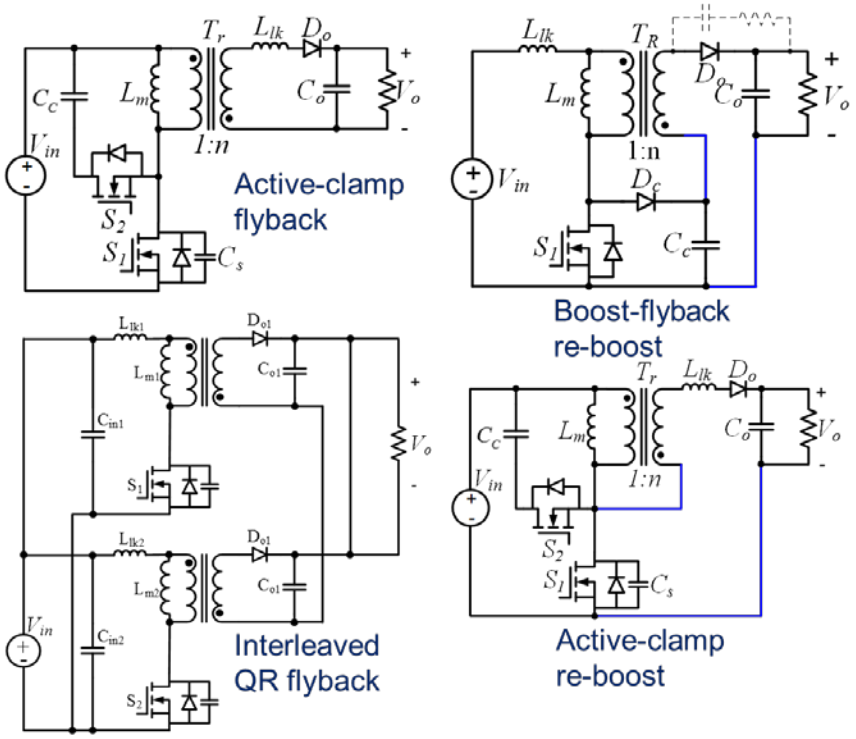


Figure 2.4 Coupled-inductor PWM dc-dc converters.

2.2.2 Current-fed PWM converters

Second type of high boost ratio dc-dc converters are current-fed PWM converters, as shown in Figure 2.5 [C25]-[C43]. This type of converters inherits the high boost gain of traditional simple boost converter and the input current ripple is low. However, this type of converters requires more magnetic components, which result in high cost and large volume. For the circuits like boost half bridge and boost push-pull dc-dc converters, the voltage stresses on the main devices are clamped by the auxiliary switches or diodes, however the efficiency of these two converters suffers from the cascaded structures.

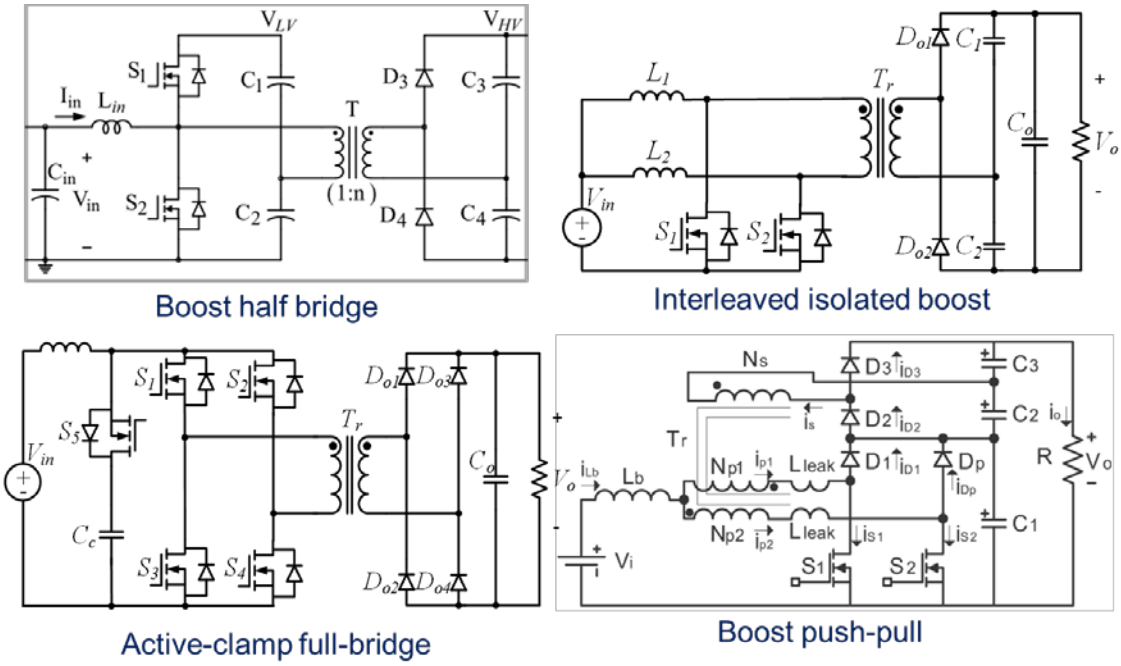


Figure 2.5 Current-fed PWM converters.

2.2.3 LLC resonant converters

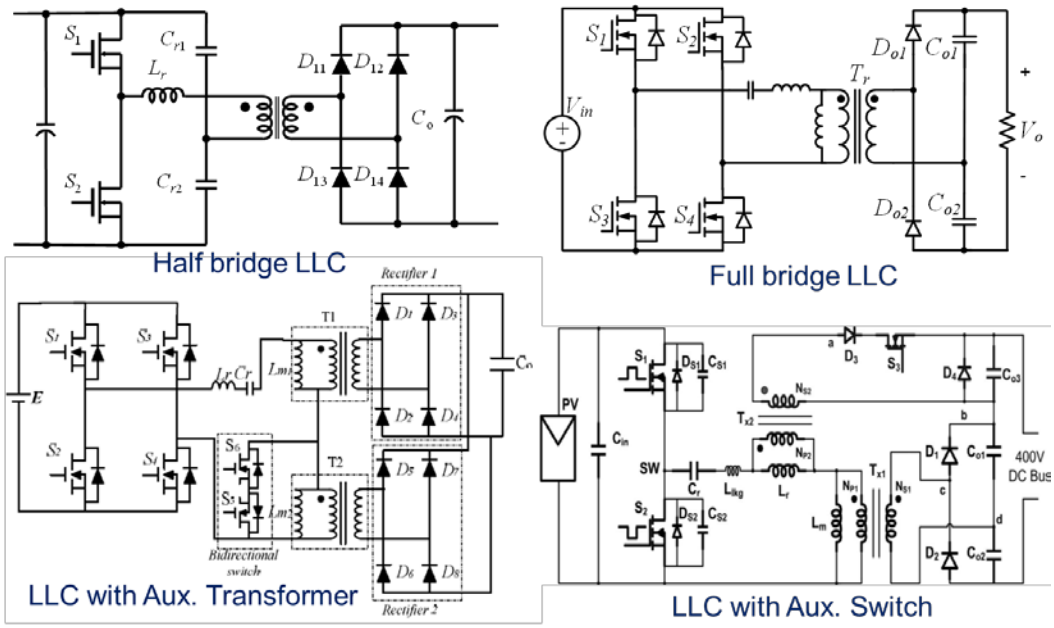


Figure 2.6 LLC resonant converters.

The third type of converters are LLC resonant converters, as shown in Figure 2.6 [C44]-[C55], which are very popular in computer industry for the applications where hold up time is required. Traditional half-bridge and full-bridge LLC resonant converters have high peak efficiency at resonant frequency. They can run with high frequency to reduce the magnetic sizes as a result of zero-voltage-switching (ZVS) of active switches and zero-current-switching (ZCS) of output diodes. The voltage regulation of traditional LLC converters is achieve by variable frequency. For the applications with wide input voltage range, like PV modules, the operation frequencies may be far from resonant frequency. This will results in high circulating losses and LLC converters may lose ZVS or ZCS. In order to improve the voltage regulation capability of traditional LLC resonant converters, some improved versions of LLC resonant converter, such as LLC with auxiliary transformer or LLC with auxiliary switch were proposed. However, these improved converters have very complex structures resulting in high cost and complex control.

Table 2-1 summarizes the pros and cons of the-state-of-the-art high boost ratio dc-dc converters. It indicates that new high boost ratio dc-dc topologies with high efficiency, simple structure and low cost are desired for two-stage microinverters.

Table 2-1 Pros and cons of the-state-of-the-art high boost ratio dc-dc converters

Type	Pros	Cons

Coupled-inductor	• Simple structure • Low duty range	• Poor magnetic utilization • High voltage stresses on output diodes
Current-fed	• High voltage gain • Low input current ripple	• Two or three magnetics • Efficiency suffers from leakage inductors or cascaded-structure
LLC resonant	• High peak efficiency • Potential high frequency operation	• Complex control • Complex structure and high cost due to aux. circuits

2.3 Proposed hybrid transformer high boost ratio dc-dc converter

For application of microinverters, the high efficiency over a wide power range is extremely important because the performance is weighted differently for specific load levels in the CEC or European Union (EU) standards. In this section, a high boost ratio dc-dc converter with hybrid transformer is presented to achieve high system level efficiency over wide input voltage and output power ranges, while still maintain low cost and simple structure. As shown in Figure 2.7, by introducing a RVD, which is composed of leakage inductance of L_{lk}, a small resonant capacitor C_r, diodes D_r and D_o into the energy transfer path, a hybrid operation mode, which combines PWM and resonant power conversions [C4],[C5], is introduced into the proposed high boost ratio dc-dc converter.

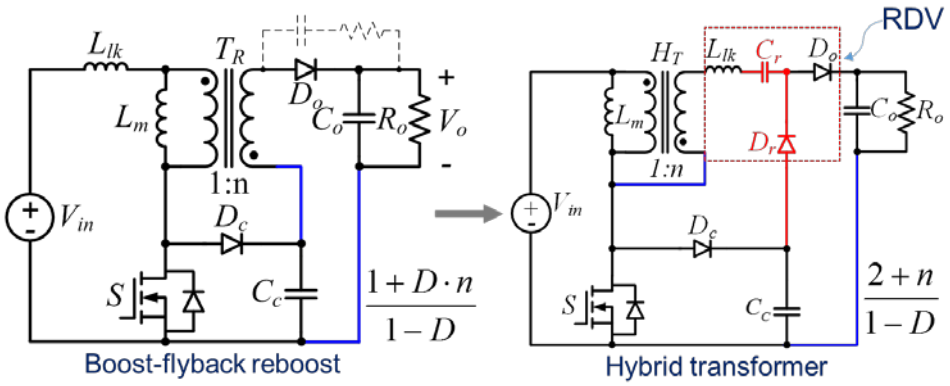


Figure 2.7 Derive hybrid transformer high boost ratio dc-dc converter by introducing resonant voltage doubler into traditional boost-flyback reboost PWM converter.

In the proposed converter, the inductive and capacitive energy can be transferred simultaneously to the high voltage dc bus increasing the total power delivered decreasing the losses in the circuit. As a result of the energy transferred through the hybrid transformer that combines the modes where the transformer operates under normal conditions and where it operates as a coupled-inductor, the magnetic core can be used more effectively and smaller magnetics can be used. The continuous input current of the converter causes a smaller current ripple than that of previous high boost ratio converter topologies that used coupled-inductors. The lower input current ripple is useful in that the input capacitance can be reduced and it is easier to implement a more accurate MPPT for PV modules. The conduction losses in the transformer are greatly reduced because of the reduced input current RMS value through the primary side. The voltage stress of the active switch is always at a low voltage level and independent of the input voltages. Due to

the introduction of the resonant portion of the current, the turn-off current of the active switch is reduced. As a result of the decreased RMS current value and smaller turn-off current of the active switch, high efficiency can be maintained at light output power level and low input voltage operation. Because of the resonant capacitor transferring energy to the output of the converter, all the voltage stresses of the diodes are kept under the output dc bus voltage and independent of the input voltage.

2.4 Operation principle

This section gives the basic operation principle of the proposed converter, then the device voltage stresses and conversion ratio are derived, finally the design procedure is suggested.

2.4.1 Topological stages and key waveforms

Figure 2.8 illustrates the five steady state topology stages of the proposed dc-dc converter for one switching cycle. Figure 2.9 shows the key voltage and current waveforms for specific components of the converter over the switching cycle.

C_{in} is the input capacitor; HT is the hybrid transformer with the turn ratio 1: n; S_1 is the active MOSFET switch; D_1 is the clamping diode, which provides a current path for the leakage inductance of the hybrid transformer when S_1 is off; C_c captures the leakage energy from the hybrid transformer and transfers it to the resonant capacitor C_r by means of a resonant circuit composed of C_c, C_r, L_r and D_r; L_r is a resonant inductor, which operates in the

resonant mode; D_r is a diode used to provide a unidirectional current flow path for the operation of the resonant portion of the circuit. C_r is a resonant capacitor, which operates in the hybrid mode by having a resonant charge and linear discharge. The turn on of D_r is determined by the state of the active switch S_1. D_o is the output diode similar to the traditional coupled-inductor boost converter; C_o is the output capacitor. R_o is the equivalent resistive load.

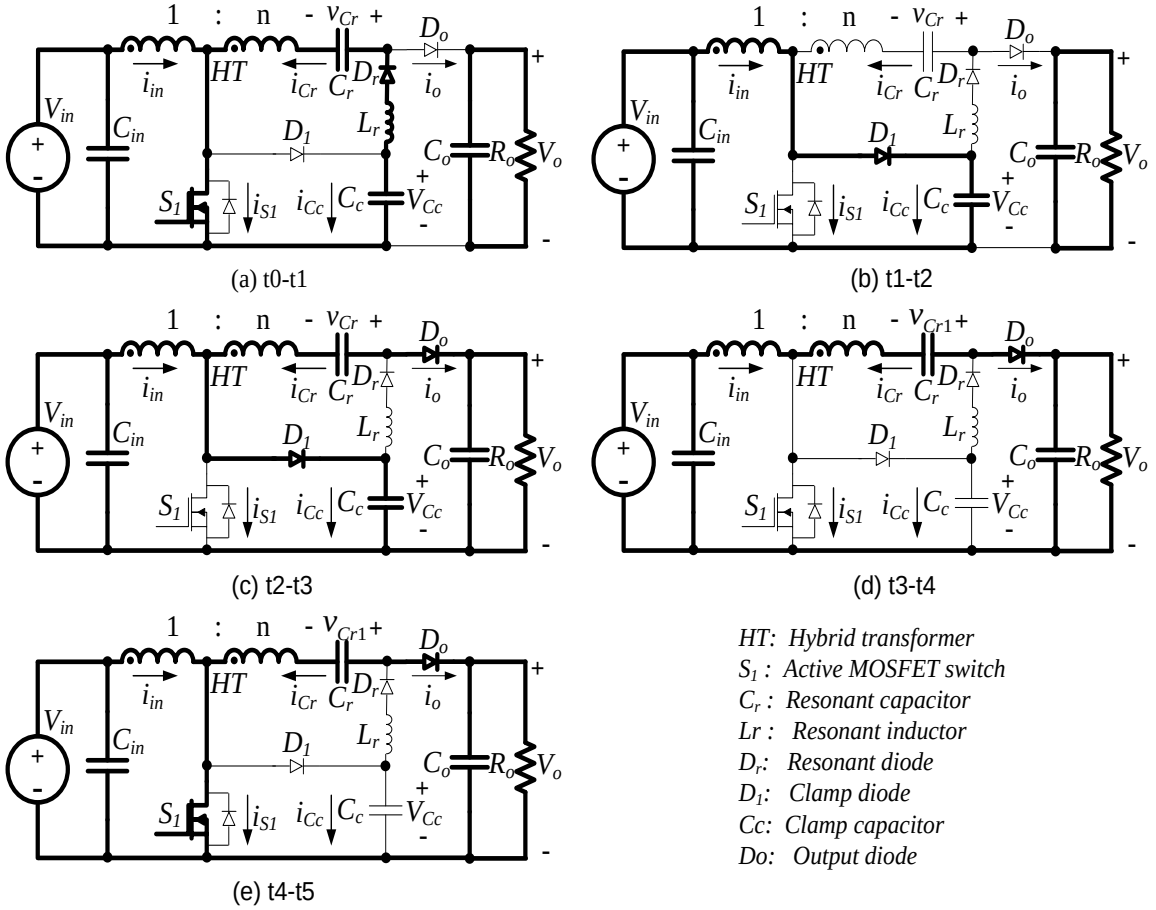


Figure 2.8 Topological states of the high boost ratio dc-dc converter with hybrid transformer.

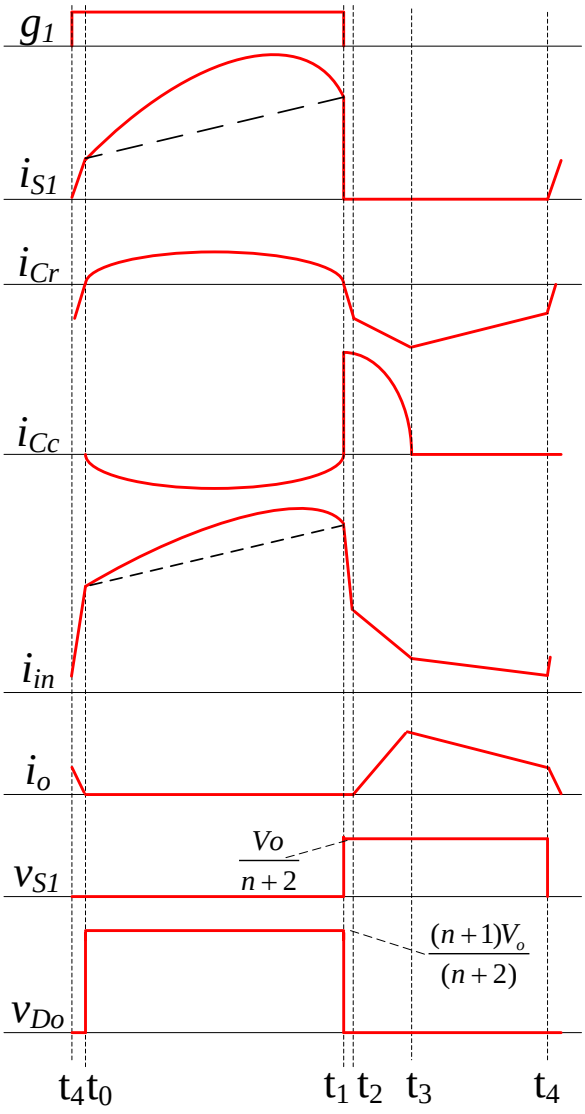


Figure 2.9 Key waveforms for different operation stages.

For the waveforms in Figure 2.9, g_1 represents the driver signal for the active MOSFET switch S_1; i_{s1} is the current of the MOSFET S_1; i_{Cr} is the current of the resonant capacitor C_r; i_{Cc} is the current of clamping capacitor C_C; i_{in} is the primary side current of hybrid transformer; i_o is the current through the output diode; v_{s1} and v_{Do} are the voltage waveforms of the active switch MOSFET S_1 and the output diode D_o respectively. For simplicity, we assume

that the dc input voltage is a stiff voltage source with a constant voltage V_{in}, the load is a resistor and all the switch and diodes are ideal devices.

The five operation modes are briefly described as follows.

$[t_0,t_1]$, [Fig. 2.8 (a)]: In this period, MOSFET S_1 is on, the magnetizing inductor of the hybrid transformer is charged by input voltage; C_r is charged by C_c and the secondary-reflected input voltage $n V_{in}$ of the hybrid transformer together by the resonant circuit composed of secondary side of the hybrid transformer , C_r, C_c, L_r and D_r. The energy captured by C_c is transferred to C_r, which in turn is transferred to the load during the off time of the MOSFET. The current in MOSFET S_1 is the sum of the resonant current and linear magnetizing inductor current as shown in Fig. 5. There are two distinctive benefits that can be achieved by the linear and resonant hybrid mode operation. The first benefit is that the energy is delivered from source during the capacitive mode and inductive mode simultaneously. Compared to previous coupled-inductor high boost ratio dc-dc converters with only inductive energy delivery, the dc current bias is greatly reduced, decreasing the size of the magnetics. Second the turn-off current is decreased; this causes a reduction in the turn-off switching losses.

$[t_1,t_2]$, [Fig. 2.8 (b)]: At time t_1, MOSFET S_1 is turned off, the clamping diode D_1 is turned on by the leakage energy stored in the hybrid transformer during the time period that the MOSFET is on and the capacitor C_c is charged which causes the voltage on the MOSFET to be clamped.

[t_2, t_3], [Fig. 2.8 (c)]: At time t_2, the capacitor C_c is charged to the point that the output diode D_o is forwarded-biased. The energy stored in the magnetizing inductor and capacitor C_r is being transferred to the load and the clamp diode D_1 continues to conduct while C_c remains charged.

[t_3,t_4], [Fig. 2.8 (d)]: At time t_3, diode D_1 is reversed-biased and as a result, the energy stored in magnetizing inductor of the hybrid transformer and in capacitor C_r is simultaneously transferred to the load. During the steady state operation, the charge through capacitor C_r must satisfy charge balance. The key waveform of the capacitor C_r current shows that the capacitor operates at a hybrid-switching mode, i.e., charged in resonant style and discharged in linear style.

[t_4, t_0], [Fig. 2.8 (e)]: The MOSFET S_1 is turned on at time t_4. Due to the leakage effect of the hybrid transformer, the output diode current i_o will continue to flow for a short time and the output diode D_o will be reversed-biased at time t_0 then the next switching cycle starts.

The boost ratio M_b can be obtained by three flux balance criteria for the steady state. The first flux balance on the magnetizing inductor of hybrid transformer requires that in steady state

$$V_{Cc} = \frac{V_{in}}{1-D} \tag{2.1}$$

Second, according to flux balance on the resonant inductor during ON time

$$V_{Cr} = nV_{in} + V_{Cc} = (n + \frac{1}{1-D})V_{in} \tag{2.2}$$

The last flux balance that governs the circuit is voltage-second balance of the magnetizing inductor in the hybrid transformer for the whole switching period

$$V_{in}D = \frac{V_o - V_{Cr} - V_{in}}{1+n}(1-D) \tag{2.3}$$

By substituting equation (2.4) into equation (2.5), the boost conversion ratio can be obtained

$$M_b = \frac{V_o}{V_{in}} = \frac{n+2}{1-D} \tag{2.4}$$

The conversion ratio is similar to the conventional boost converter except that the turns ratio term n is added, so the traditional duty ratio control method that is applied for a standard boost converter can also be applied to the proposed converter.

2.4.2 Voltage stress derivation of the power devices

Voltage stresses for all the power devices of the converter are determined in this section to select power devices with the proper rating and all the results are respect to the output dc voltage. From the circuit diagram of t_0 to t_1 and t_1 to t_2 in Figure 2.8 respectively, the voltage stresses for MOSFET S_1 and clamping diode D_1 are obtained

$$V_{S_1} = V_{D_1} = \frac{V_{in}}{1-D} = \frac{V_o}{n+2} \tag{2.5}$$

From the circuit diagram of t_0 to t_1 and t_2 to t_3 in Figure 2.8, one obtains the voltage stress of diode resonant diode D_r and output diode D_o

$$V_{Dr} = V_{Do} = V_o - V_{Cc} = V_o - \frac{V_{in}}{1-D} = \frac{(1+n)V_o}{2+n} \tag{2.6}$$

From equation (2.5) and equation (2.6), it is obvious that all the voltage stresses of the switches are independent of input voltage and load conditions. In other words, all the voltage stresses of the switches are optimized based on the output voltage and the turns ratio of the transformer. The resonant period T_r and resonant frequency are given by

$$T_r = 2\pi\sqrt{L_r C_r} \tag{2.7}$$

$$f_r = 1/T_r \tag{2.8}$$

If the constant on time control T_{on} is used, choose $T_{on}=1/2T_r$ so that the resonant diode can turn off at zero-current condition and conduction loss can be minimized. In the experimental implementation of the hybrid transformer, the leakage inductance of the hybrid transformer should be considered, so the total resonant inductance is expressed as follows

$$L_{r,total} = L_r + L_{lrs} + n^2 L_{lrp} \tag{2.9}$$

Where, L_{lrs} is the secondary side leakage inductance and L_{lrp} is the primary side inductance of the hybrid transformer. The resonant capacitance C_r is composed by C_r and C_c in series. Normally, we choose $C_r << C_c$ so voltage stress of the MOSFET can be clamped well. The optimal operation mode is the constant PWM on time T_{on} control with variable frequency, however traditional PWM control method is applicable to the proposed converter as described in [C4], [C5].

2.4.3 Energy transfer analysis

The simplified waveforms for energy transfer analysis are shown in Figure 2.10. In order to analyze the energy transfer feature from the low voltage dc energy source to the high voltage dc bus, it is necessary to solve the equivalent circuit in Figure 2.8(a) subject to the initial conditions imposed by the previous PWM OFF-time interval given by

$$i_{L_r}(0) = 0 \tag{2.10}$$

$$v_{Cr}(0) = -\Delta v_{Cr} \tag{2.11}$$

where Δv_{Cr} is the ripple of the resonant capacitor C_r.

The resonant solutions are obtained as

$$i_{L_r}(t) = \Delta i_{L_r} \sin 2\pi f_r \cdot t \tag{2.12}$$

$$v_{Cr}(t) = \Delta v_{Cr} \cos 2\pi f_r \cdot t \tag{2.13}$$

$$\Delta v_{Cr} = R_N \cdot \Delta i_{L_r} \tag{2.14}$$

where R_N is characteristic impedance given by

$$R_N = \sqrt{L_r / C_r} \tag{2.15}$$

For PWM off time interval, the discharge equations of the resonant capacitor C_{r1} are given by

$$\Delta v_{C_r} = \frac{I_{Lm\_\sec} T_{off}}{2C_r} \tag{2.16}$$

$$I_{Lm\_\sec} = \frac{I_o}{1-D} = \frac{P_o}{V_o}\frac{1}{1-D} \tag{2.17}$$

where I_{Lm_sec} is the average linear magnetizing current referred to secondary side of the hybrid transformer, I_o is the average output current, P_o is the output power and V_o is the output voltage.

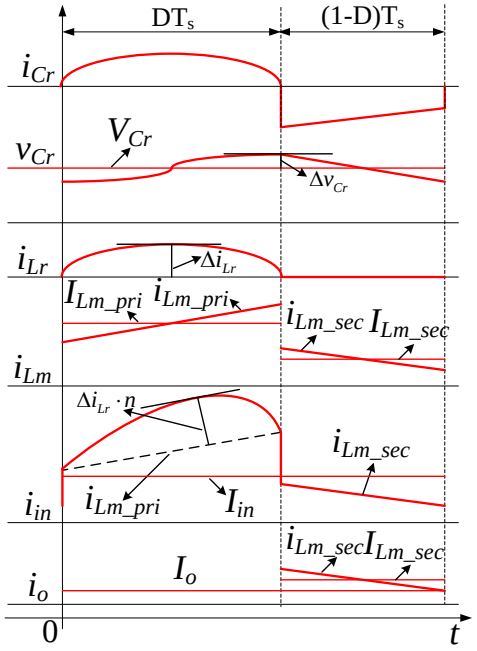


Figure 2.10 Waveforms for energy transfer analysis.

From equations (2.14), (2.15), (2.16) and (2.17), the relationship between and linear magnetizing current and sinusoidal resonant current can be expressed as

$$\Delta i_{L_r} = \pi \cdot f_r \cdot T_s \cdot I_{Lm\_sec} \cdot (1-D) = \pi \cdot f_r \cdot T_s \cdot I_o \tag{2.18}$$

Accordingly, the average primary side sinusoidal resonant current of hybrid transformer is given by:

$$L_{Lr\_pri} = \frac{1}{\pi} n \cdot \Delta i_{L_r} \tag{2.19}$$

Substituting equation (2.18) into equation (2.19) yields:

$$L_{Lr\_pri} = n \cdot f_r \cdot T_s \cdot I_o \tag{2.20}$$

The average input current I_{in} can be obtained from equation (2.5) by power balance:

$$I_{in} = \frac{n+2}{1-D} \cdot I_o \tag{2.21}$$

For the optimal mode operation, the relationship between the resonant frequency and the switching period is:

$$f_r = \frac{1}{2 \cdot D \cdot T_s} \tag{2.22}$$

Substituting equation (2.22) into equation (2.19) yields:

$$L_{Lr\_pri} = \frac{n \cdot I_o}{2D} \tag{2.23}$$

The resonant contribution index k_r of energy transfer by sinusoidal resonant current can be defined as the ratio between the average input resonant current L_{Lr_pri} to the total input current I_{in}

$$k_r = \frac{L_{Lr\_pri}}{I_{in}} = \frac{n \cdot I_o}{2D} / (\frac{n+2}{1-D} \cdot I_o) = \frac{(1-D)}{2D} \cdot \frac{n}{n+2} = \frac{n}{2D} \cdot \frac{V_{in}}{V_o} \tag{2.24}$$

In order to optimize the operation of the proposed converter, k_r needs to be increased, this will reduce the turn-off losses of the MOSFET and decrease the size of the magnetic core used. The curve of the resonant energy transfer contribution index K_r at different input voltage conditions is shown in Figure 2.11. The operating conditions for the curve in Figure 2.11 are for when the output voltage V_o equals 400 V, the turns ratio of the hybrid transformer n equals 16:3 and an input voltage range from 20 V to 45 V. For a given power and fixed output voltage, the resonant energy transfer contribution index

increases along with the increase in input voltage. This feature helps improve the converter efficiency over a wide input voltage range by decreasing the conduction losses which are more dominant at low input voltages and reducing the switching losses that are more dominant at high input voltages.

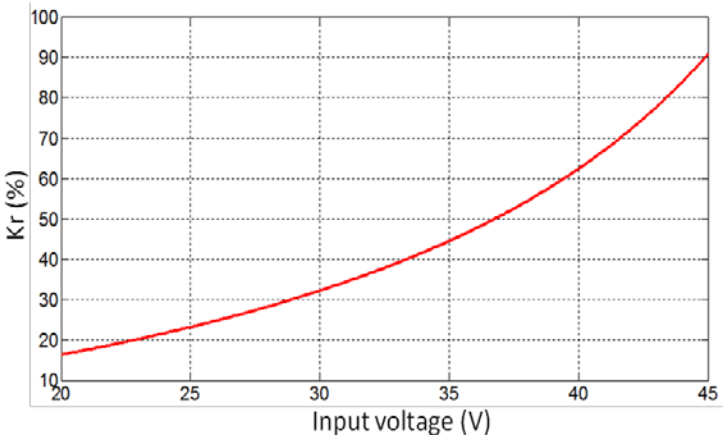


Figure 2.11 K_r *V.S.* V_{in} curve.

2.4.4 Summary of design procedure

A design procedure of the proposed converter according to above specifications is summarized as follows:

1) Magnetic core selection: In order to design with low profile to integrate the converter at the back side of PV module, a RM-14-PLP low profile core with optimized length versus area factor from Ferroxcube [F8] was selected. Another advantage of RM-14-LP core is that we can design a hybrid transformer with minimized leakage inductance.
2) Transformer turns ratio: Two constraints decide the turns ratio of hybrid transformer. First constraint is from the boost ratio of equation (2.4), which should ensure the duty ratio in a reasonable range within the whole

input PV voltage ranges. Second constraint is equation the switch device voltage stress of equation (2.5). For a high boost ratio converter, one of the major losses is due to the primary RMS conduction loss. In order to reduce this loss, MOSFET with low $R_{ds(on)}$ is preferred. This needs the voltage stress of the active switches, which is given by (2.5) should be kept under a low level.

3) Resonant capacitor C_r: The capacitance of Cr can be designed based the ZCS requirements output diodes.
4) Clamping capacitor C_c: The clamping capacitor C_c should be selected such that the voltage ripple on C_c is kept a negligibly low level.

2.5 Experimental verifications

In order to verify the effectiveness of the proposed converter, a prototype circuit with the photograph shown in Figure 2.12 was built and tested.

The design parameters and components selection for the converter are also listed in Figure 2.12. From the analysis of the circuit, two control methods can be adopted for the proposed converter. The first method is utilizing a variable frequency control this is accomplished by using a fixed T_{on} control, and varying the T_{off} internal to obtain the desired gain. Another control method is the traditional PWM converter control by adjusting the duty cycle of the switch for a fixed frequency to obtain the desired boost gain. Although the fixed T_{on} control is optimal, however, in real control

implementation; PWM control with fixed switching frequency is preferred because of its simplicity.

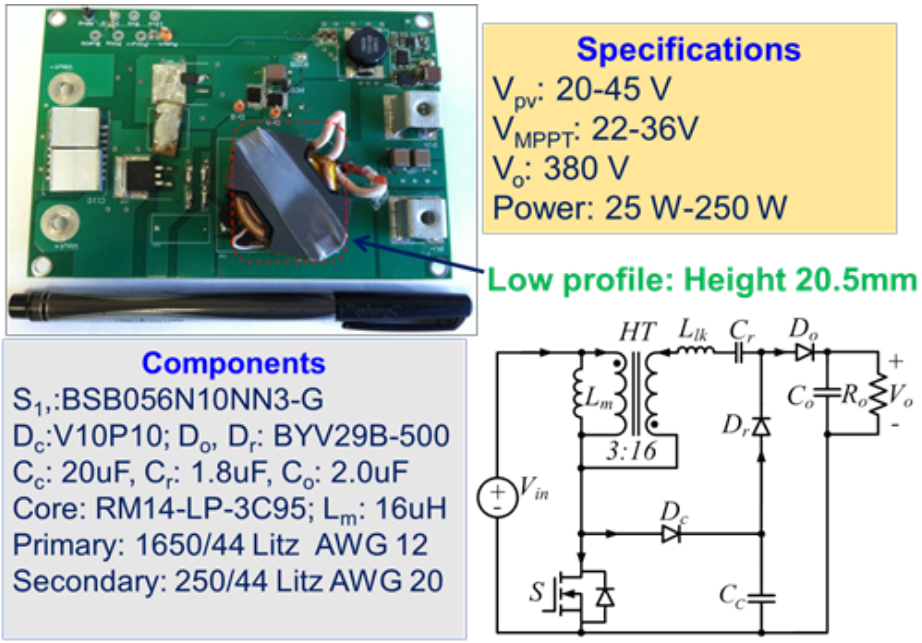


Figure 2.12 Photograph of the prototype circuit, specifications, and selection of components.

In the experiment, the proposed converter was designed to convert the low dc voltage, V_{in} with the voltage varying from 20 V-45 V, to a constant high dc output, V_o=400V. To maintain a low voltage stress on the active switch M_1 and reasonable duty cycle range, the turns ratio n of hybrid transformer was chosen to be 16:3. The calculated voltage stress for switch S_1 using equation (2.5) was about 60V and voltage stress for output diode using equation (2.6) was 340V. The resonant contribution index $k_r = 0.35$ was when D=0.5. The duty ratio range calculated by equation (2.4) for an input PV module voltage range of 20 V to 45 V is 0.28 to 0.68, which is kept within a reasonable range.

Figure 2.13 highlights the experimental waveforms of the resonant capacitor current, input current and voltage of the MOSFET with P_o=220 W, V_o=400 V and V_{in}=30 V. As seen from Figure 2.13, the switch voltage V_{ds} is clamped at 60V and the resonant capacitor is charged by sinusoidal resonant mode and discharge by linear PWM mode, while the input current is composed of linear current and resonant current.

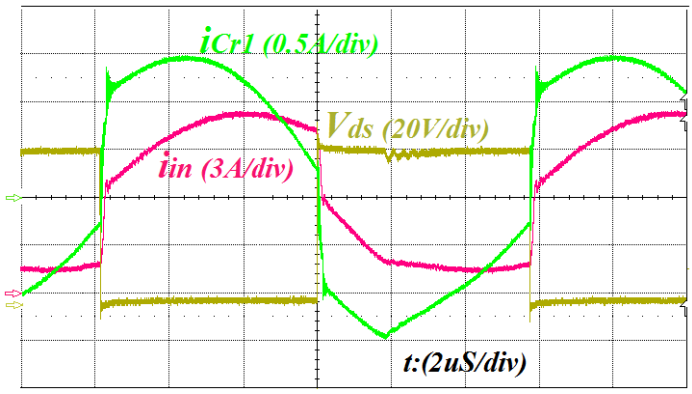


Figure 2.13 Experimental waveforms of current of the resonant capacitor C_{r1}, voltage of switch M_1 and input current with P_o=220W, V_o=400V, V_{in}=30V and f_s=88kHz.

Figure 2.14, figure 2.15 and figure 2.16 show the experimental waveforms of voltage of MOSFET switch, voltage of the output diode and current of the resonant capacitor C_r and input current with the input voltages of 20V, 30V and 45V under different output power level.

Experimental waveforms from figure 2.14 to figure 2.16 show that all the voltages of the MOSFET are clamped at approximately 60V and the voltages of the output diode are clamped under 350V without any voltage over-shoot matching the earlier calculations. The input current is continuous at CCM

operation with low RMS value and low ripple value decreasing the conduction loss. The turn-off current of MOSFET is reduced with the hybrid sinusoidal-linear waveform. DCM occurs at light power output and accordingly the turn-on loss can be slightly reduced with low turn-on voltage.

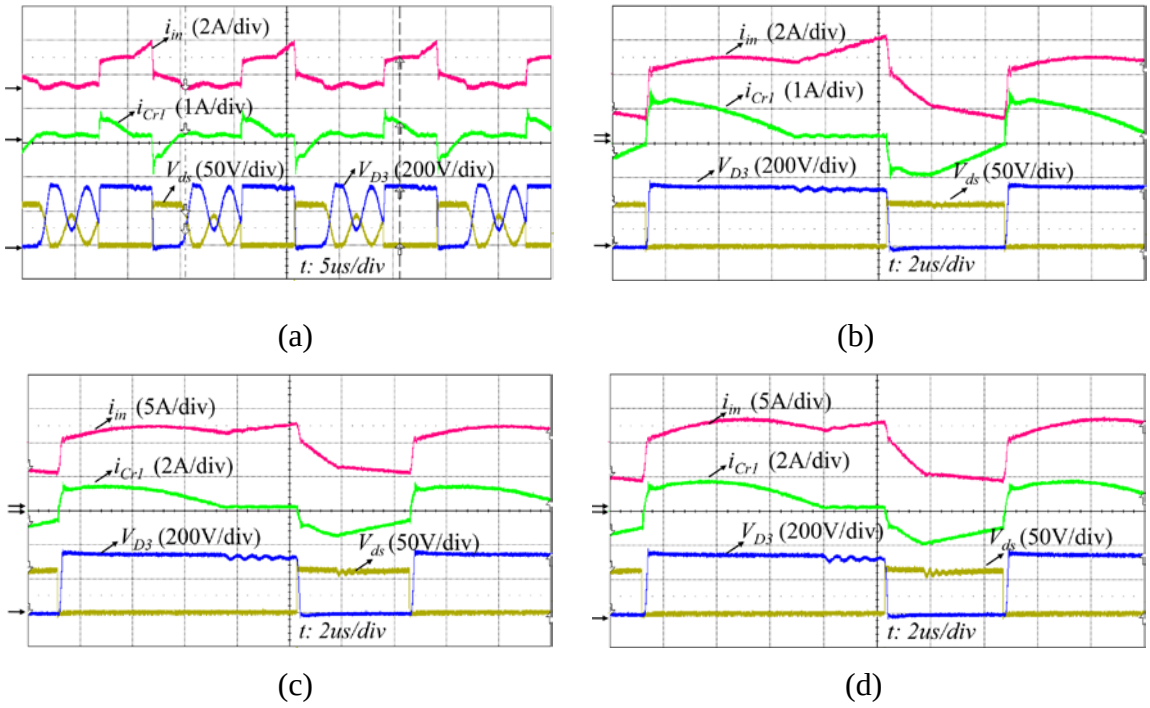


Figure 2.14 Experimental waveforms of switch voltage, output diode voltage, input current and current of resonant capacitor of the proposed converter with 20V input, 400V output under different output power level: (a) 30W, (b) 110W, (C) 160W and (d) 220W.

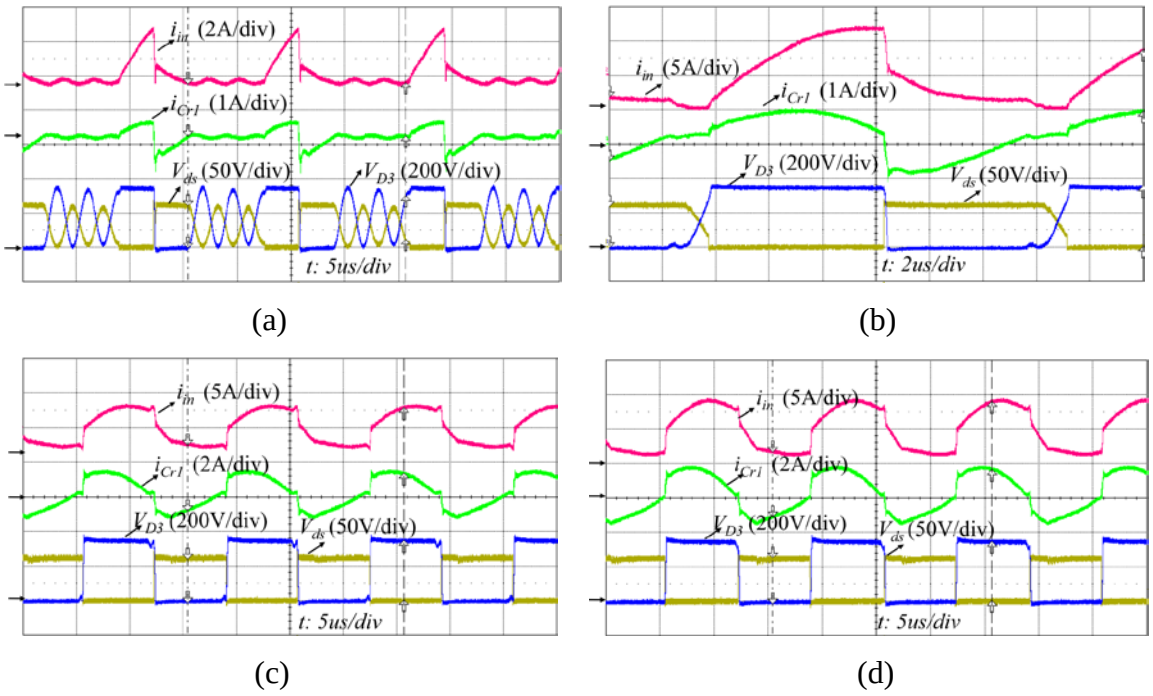


Figure 2.15 Experimental waveforms of switch voltage, output diode voltage, input current and current of resonant capacitor of the proposed converter with 30V input, 400V output under different output power level: (a) 30W, (b) 110W, (C) 160W and (d) 220W.

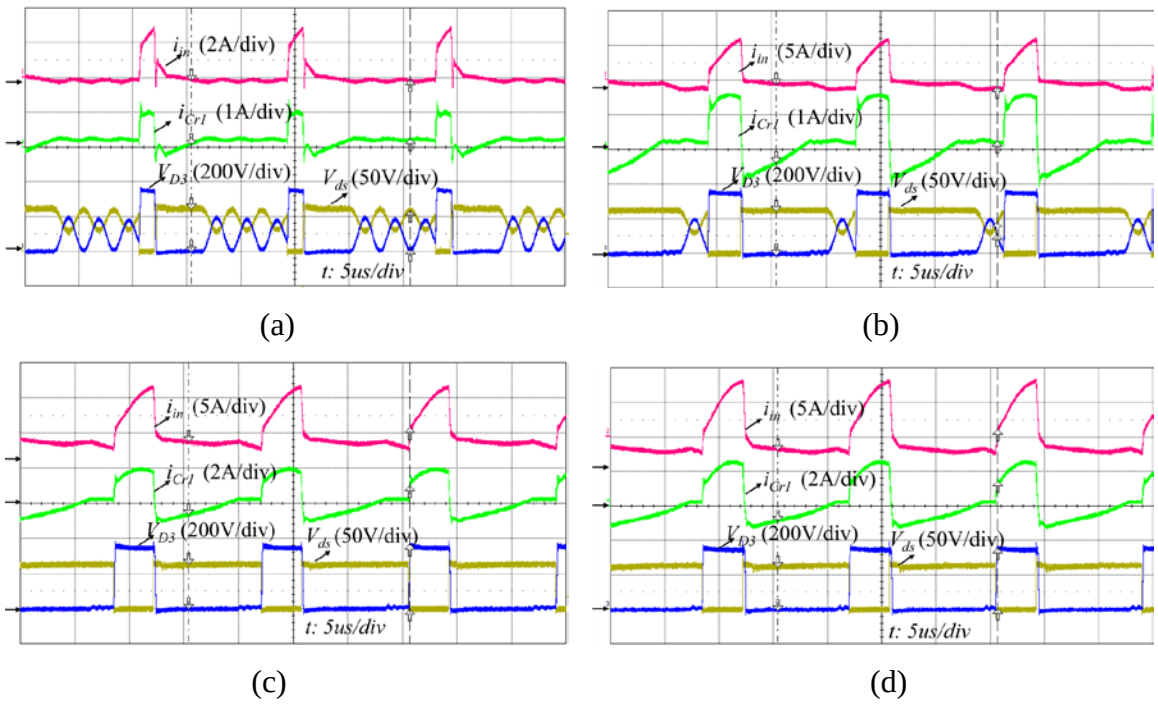


Figure 2.16 Experimental waveforms of switch voltage, output diode voltage, input current and current of resonant capacitor of the proposed converter with 45V input, 400V output under different output power level: (a) 30W, (b) 110W, (C) 160W and (d) 220W.

Figure 2.17 summarizes the conversion efficiencies for different input voltages under different output power levels. All the conversion efficiencies from 30W to 220W are higher than 96% and the peak efficiency is 97.4% under 35V input with 160W output power level. The CEC efficiencies over the 20 V to 45 V input voltage range were over 96.5% due to the relatively flat conversion efficiency curves for all input voltages as shown in Figure 2.17.

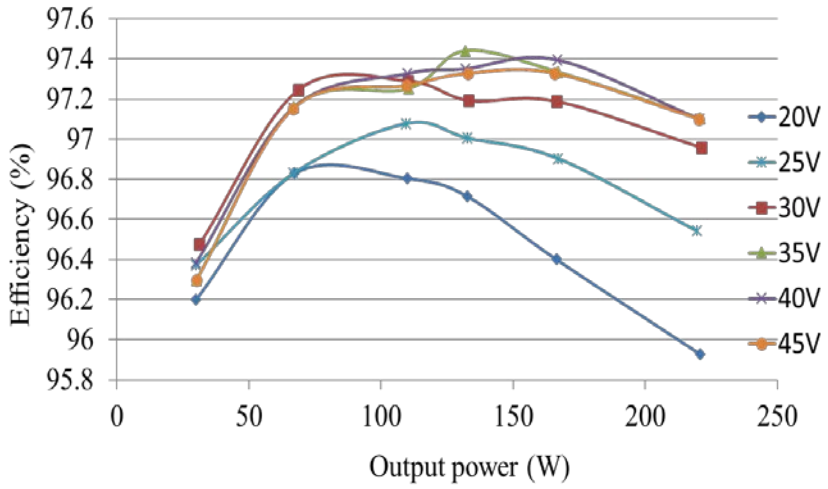


Figure 2.17 Conversion efficiency V.S. output power for different input voltages.

The weighted CEC efficiencies at different input voltage is shown in Figure 2.18. The peak CEC efficiency achieves 97.3% at 35 V input.

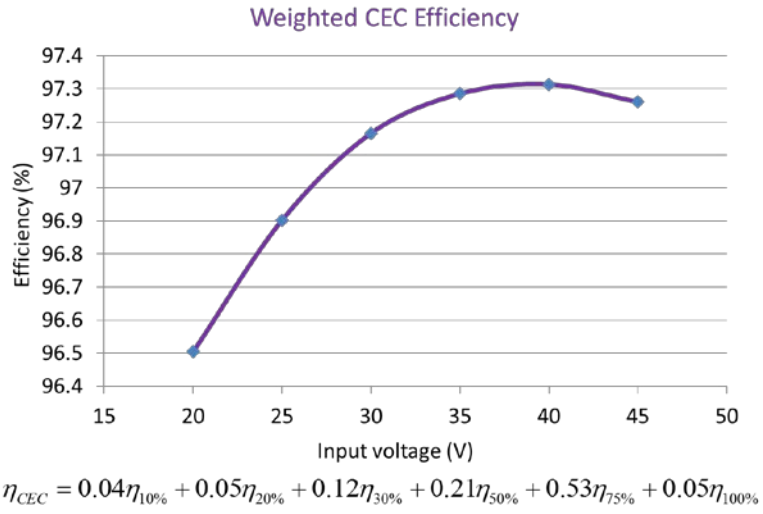


Figure 2.18 CEC efficiency at different input voltages.

In order to understand the loss distribution in the proposed converter, the loss breakdown was estimated using following equations:

- MOSFET conduction loss

$$Cond_{MOS} = I_{rms}{}^2 R_{ds(on)\_Tj} \tag{2.25}$$

where I_{rms} is the rms through the switch, $R_{ds(on)\_Tj}$ is the on-state resistor of the MOSFET, which is temperature dependent.

- MOSFET switching loss

$$Sw_{MOS} = [\frac{2}{3} C_{ds}(V_{ds}) V_{ds}{}^2 + \frac{1}{2} V_{ds} I_d (t_r + t_f)] f_{sw} \tag{2.26}$$

Where $C_{ds\ (Vds)}$ is equivalent junction capacitance, V_{ds} is swithed drain soure voltage of the MOSFET and I_d is the switched current. t_r and t_f reprent the rise and falling times of the MOSFET respetively.

- Tranformer conduction losses

$$Cond_{trans} = I_{rms\_pri}{}^2 R_{pri} + I_{rms\_sec}{}^2 R_{sec} \tag{2.27}$$

where I_{rms_pri} nad I_{rms_sec} represent the primary and secondary RMS currents of the tranformer respectively. R_{pri} and R_{sec} represent the primary and secondary equivalent resistors respectively.

- Diode conduction loss

$$Cond_{diode} = IV_f(I) \tag{2.28}$$

where I mean the average current through the diode and $V_f(I)$ is the forward votlage drop of diode, which is a function of the current throuth the diode.

- Core loss of transformer

$$P_{core} = a(f_{sw})^c (\Delta B)^d V_e f_{sw} \tag{2.29}$$

where a, c and d are loss indexes of magnetic core, which is dependent what material the magnetic uses and can be obained from the datasheet, ΔB is half of the AC flux swing.

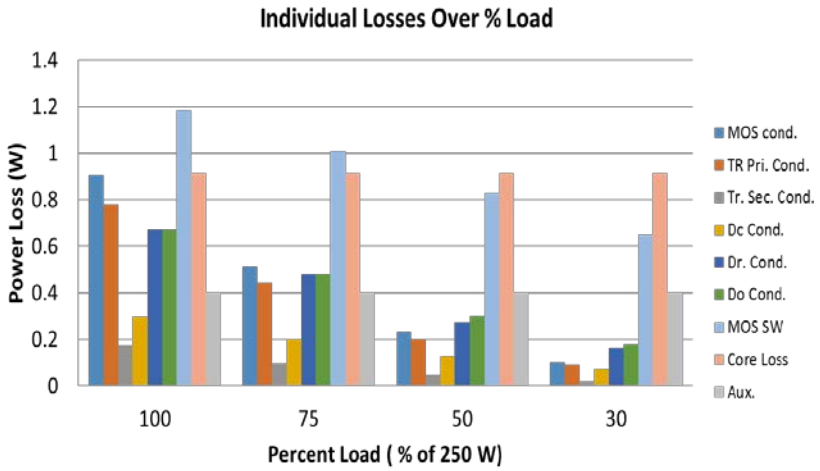


Figure 2.19 Loss breakdown at different load conditions.

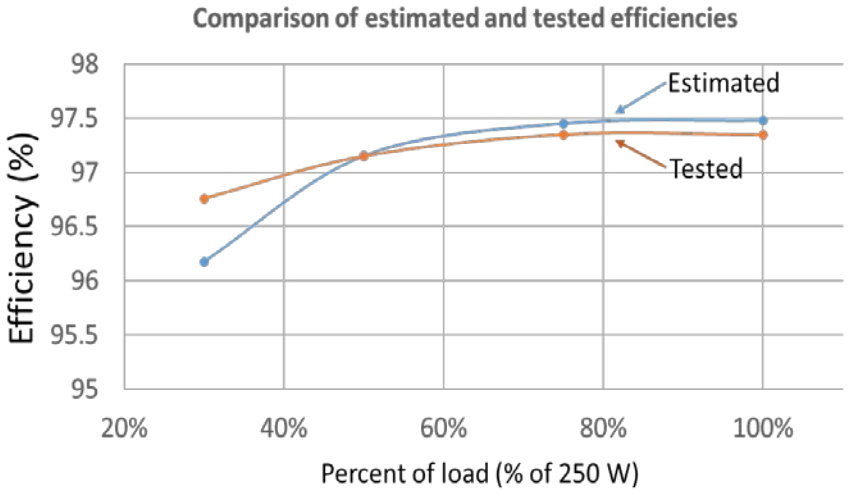


Figure 2.20 Comparison of estimated and tested efficiencies at different load conditions.

The individual loss breakdown at different load conditions is shown in Figure 2.19, where Axu. means the auxiliary losses including the auxiliary

power supply and the gate driver losses. The estimated and tested efficiencies are compared in Figure 2.20 to jusfity the accuracy of the estimation.

2.6 Deriving a family of hybrid transformer dc-dc converters

Due to the simple structure, high efficiency over wide output power and input voltage ranges, hybrid transformer dc-dc converters are very attractive for microinverter applications. Using the same technique to introduce RVD cells into traditional coupled-inductor dc-dc converters, a family of hybrid transformer high boost ratio dc-dc converters, including isolated and non-isolated versions as shown in Figure 2.21 is derived in this section. The performances are compared and evaluated based on the test results.

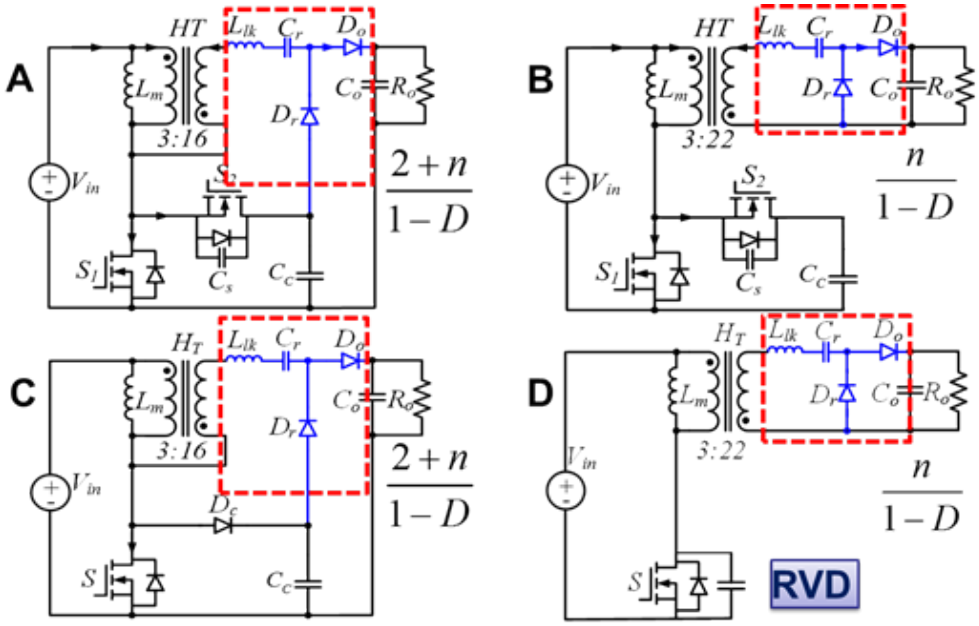


Figure 2.21 A family of hybrid transformer dc-dc converters using RVD for microinverter applications.

Figure 2.22 shows the CEC efficiency curves for three different hybrid transformer dc-dc converters. All experimental prototype use same devices and transformer core. The only difference is that isolated converter need turns ratio of 22:3 instead of 16:3 as that in non-isolated converters. This is because the clamping voltage in the nonisolated converters is boosted to the output leading to low turns ratio.

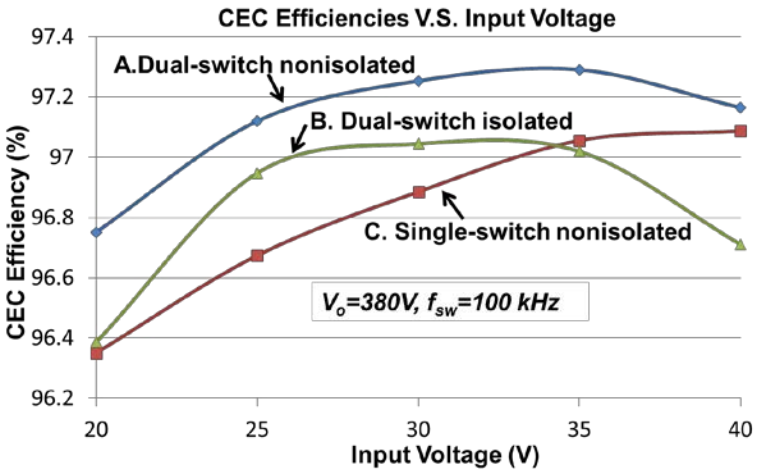


Figure 2.22 CEC efficiency comparison.

The nonisolated dual-switch switch converter in Figure 2.21 (a) has highest efficiency because of its relatively high gain from the voltage of clamping capacitor C_c and ZVS operation. The nonisolated single-switch converter has lowest cost. The dual-switch isolated converter as shown in Figure 2.21 (c) has high efficiency within MPPT voltage range, which is desirable for microinverter applications.

2.7 Summary

Electrolytic capacitors have been identified as one of the most unreliable components in grid-tie inverters. Microinverter using two-stage architecture can avoid electrolytic capacitors without additional penalties. A high boost ratio dc-dc converter is desired for the first stage of two-stage microinverter. The review of the-state-of-the-art high boost ratio dc-dc converters indicates new low cost, high efficiency dc-dc converter topologies are desired. A high boost ratio dc-dc converter with hybrid transformer suitable for microinverter applications is proposed. The resonant conversion mode is incorporated into traditional high step-up PWM converter with coupled-inductor and switched-capacitor obtaining the following features and benefits:

1. This converter transfers the capacitive and inductive energy simultaneously to increase the total power delivery reducing losses in the system.
2. The conduction loss in the transformer and MOSFET are reduced as a result of the low input RMS current and switching loss is reduced with a lower turn-off current. With these improved performances the converter can maintain high efficiency under low output power and low input voltage conditions.
3. With low input ripple current feature, the converter is suitable for PV module and fuel cell PCS, where, accurate MPPT is performed by the dc-dc converter.

A prototype circuit targeted PV module power optimizer with 20V-45V input voltage range and 400V dc output was built and tested. Experimental results show that the MOSFET voltage was clamped at 60 V and the output diode voltage was under 350V. These results were independent of the input voltage level. The conversion efficiencies from 30W to 220W are higher than 96% and the peak efficiency is 97.4% under 35V input with 160W output power.

By introducing basic RVD cell into traditional simple-structure coupled-inductor PWM dc-dc converters, a family of hybrid transformer dc-dc converters, including isolated and nonisolated versions suitable for microinverter applications are presented.

Chapter 3 Advantages of Hybrid Transformer DC-DC Converters

The advantages of hybrid transformer dc-dc converter are analyzed in this section to justify the attractiveness of its application for microinverters. The PV module used for the analysis in this section is CS6P-240P [F7] from CanadianSolar Inc. In order to demonstrate the improvements of introducing resonant operation into traditional PWM converters, the boost-flyback reboost converter in [C9] and the proposed converter will be comparatively analyzed. The compared performance include magnetic utilization (MU), power device utilization (PDU), switching losses, and cost.

Table 3-1 Specification and power stage parameters

Converter	Boost-flyback reboost	Proposed converter
Rated power	250 W	250 W
Output voltage	380 V	380 V
Input voltage range	20-45 V	20-45 V
Output power	25W~250W	25W~250W
Turns ratio	n_1=70/3	n_2=16/3
Switching frequency	100 kHz	100 kHz
Magnetizing inductor	L_{m1}=16 uH	L_{m2}=16 uH
Clamping capacitor	C_c=20 uF	C_C=20 uF
Resonant capacitor	N.A.	C_r=0.33 uF
R-C snubber	Yes	N.A.

The specification requirements and the parameters of two prototype converters are shown in Table 3-1. The notations of the symbols are shown in Figure 3.1.

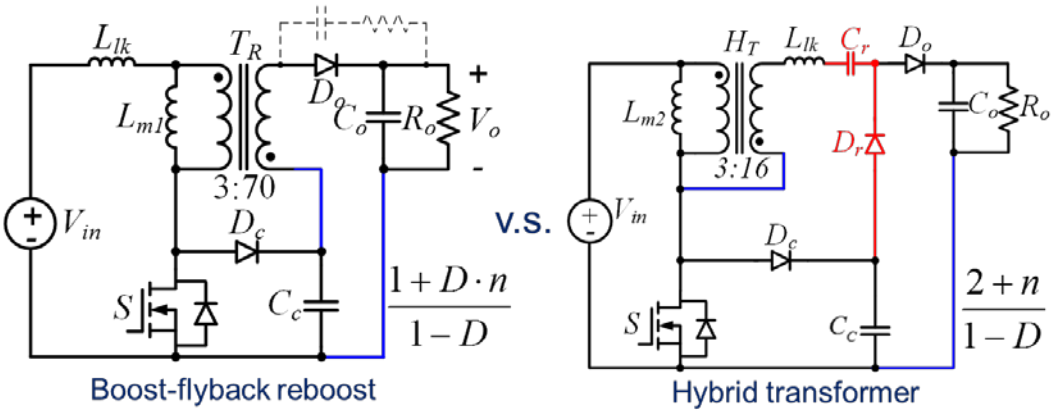


Figure 3.1 Notations of the symbol in Table 3-1.

3.1 Optimized magnetic utilization

One dominant factor of the size of PV module integrated dc-dc converter is the magnetic component. Two methods can be used to reduce the magnetic size, one is increasing the switching frequency, and another is optimizing the MU. However, the main barrier of high switching frequency operation is the switching losses. Hence, improving the MU is very beneficial to reduce the size of the PV module integrated dc-dc converter. The required core-window product, i.e. the size of magnetic component is proportional to the energy store in the magnetic core [F15],

$$A_e W_a \propto \frac{1}{2} L_m I_m i_{m\_pk} \tag{3.1}$$

Where, L_m is the magnetizing inductance, I_m and i_{m_pk} is the average and peak magnetizing current respectively. In the proposed converter and

conventional coupled-inductor based PWM high boost ratio converters, air gap normally is required to store the magnetic energy and prevent saturation. The gapped magnetic core has linear reluctance; hence the total flux in the magnetic core versus magnetomotive force (MMF) for the proposed converter and the boost-flyback reboost converter in [C9] can be illustrated as in Figure 3.2. The DC-bias current for converter in [C9] can be calculated as

$$I_{Lm1} = \frac{(D_1 n_1 + 1)}{(1 - D_1) \cdot D_1} \frac{P_o}{V_o} \tag{3.2}$$

The DC-bias current for proposed converter can be calculated as

$$I_{Lm2} = \frac{(n_2 + 2)}{(1 - D_2)} \frac{P_o}{V_o} \tag{3.3}$$

In (3.2) and (3.3), D_1 and D_2 are the duty cycles for 30 V PV input voltage; P_o is the maximum output power 250 W; V_o is output voltage and equal to 380 V.

The ripple magnetizing currents of the converter in [C9] and the proposed converter can be calculated as

$$\Delta i_{Lm1} = \frac{(1 - D_1) \cdot D_1}{(D_1 n_1 + 1)} \frac{V_o}{f_{sw} L_{m1}} \tag{3.4}$$

$$\Delta i_{Lm2} = \frac{(1 - D_2) \cdot D_2}{n_2 + 2} \frac{V_o}{f_{sw} L_{m2}} \tag{3.5}$$

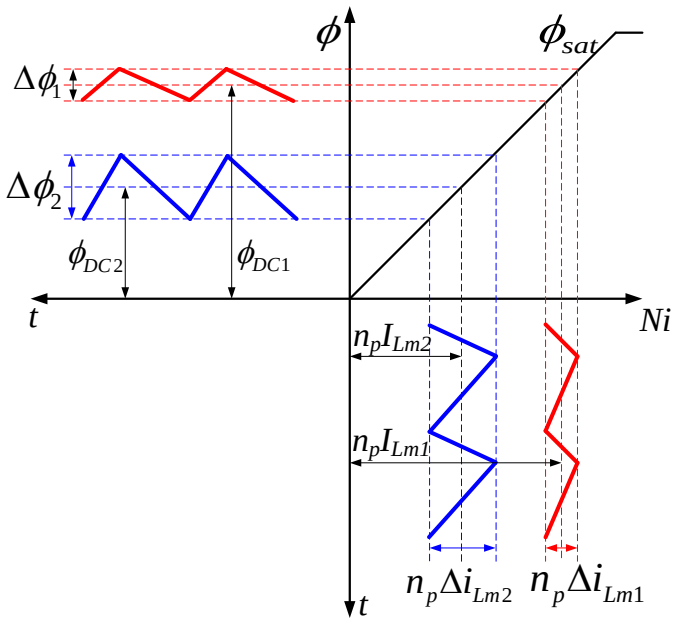


Figure 3.2 Total flux in the magnetic core versus MMF: variables with subscript 1 are for converter in [C9], variables with subscript 2 are for the proposed converter; n_p is primary turns.

The ratio of the required core-window product of magnetic component between the proposed converter and the boost-flyback reboost converter is expressed as

$$R_{A_eW_a} = \frac{\frac{1}{2}L_{m2}I_{Lm2}\cdot(I_{Lm2}+\frac{\Delta i_{Lm2}}{2})}{\frac{1}{2}L_{m1}I_{Lm1}\cdot(I_{Lm1}+\frac{\Delta i_{Lm1}}{2})} \tag{3.6}$$

Substituting (3.1) to (3.5) into (3.6), $R_{A_eW_a}$ is calculated equal to 0.56, which means that the required core-window product of magnetic component in the proposed converter is much smaller than the traditional boost-flyback reboost converter. In other word, the magnetic utilization in the proposed converter is greatly improved. Hence, smaller sized magnetics can be used in the

proposed converter, which allows low profile design to integrate with PV module.

The reason of improved MU in the proposed converter is because the magnetics works as a hybrid transformer [C4] that transfers the energy to high voltage side combined with the normal transformer and coupled-inductor operations. While in the traditional boost-flyback reboost converter, the magnetics simply worked as a coupled-inductor.

3.2 Improved power device utilization

The suitability of a power electronics topology for a specific application can be evaluated by power device utilization (PDU) [F15]. The PDU can be defined as [F15]

$$PDU = \frac{P_{\max}}{\sum_{j=1}^{k} V_j I_j} \tag{3.7}$$

Where V_j is the peak voltage applied to semiconductor device j, and I_j is the RMS or peak current applied to device j. A good candidate topology for a specific application should have minimized voltages and currents imposed on the semiconductor devices, while the transferred power is maximized. Improving the device utilization leads to minimization of the silicon area required to realize the power devices of the converter. The voltage stresses across main switch S_1, auxiliary switch S_2 and output diode D_o in boost-flyback reboost converter are given by

$$V_{S_1} = \frac{V_{in}}{(1-D_1)} \tag{3.8}$$

$$V_{Do} = n_1 \frac{V_i L_{m1}}{(L_{m1} + L_k)} + V_o \tag{3.9}$$

The peak current through S_1 and S_2 are given by

$$I_{S_1,pk} = I_{S_2,pk} = \frac{P_o}{D_{eff} V_{in}} + \frac{1}{2} \frac{V_{in} L_{m1}}{L_{m1} + L_k} \left(\frac{D_{eff} T_s}{L_{m1} + L_k} \right) \tag{3.10}$$

where D_{eff} is the secondary-side effective duty cycle. The average current through D_o in boost-flyback reboost converter is given by

$$I_{D_o,avg} = \frac{P_o}{V_o} \tag{3.11}$$

The voltage stresses of S_1, D_r and D_o in the proposed converter have been given (2.5) and (2.6) respectively. The peak currents through S_1 and S_2 in the proposed converter are given by

$$I_{S_1,pk} = I_{S_2,pk} = \frac{P_o}{V_{in}} + \frac{1}{2} \frac{V_o (1-D_2) D_2 T_s}{(n_2 + 2) L_{m2}} \tag{3.12}$$

The average currents through the diodes are

$$I_{D_r,avg} = I_{D_o,avg} = \frac{P_o}{V_o} \tag{3.13}$$

From equations from (3.8), (3.10), (3.5), and (3.12), the active switch PDU ratio between the proposed converter and the boost-flyback reboost converter can be calculated as

$$R_{PDU\_sw} = \frac{PDU_{proposed}}{PDU_{ACCI}} = 129\% \tag{3.14}$$

This equation indicates that the active switch PDU of the proposed converter is improved 29% compared to the traditional of PWM boost-flyback reboost converter.

Similarly, the diode PDU ratio of the proposed converter over boost-flyback reboost converter can be calculated as

$$R_{PDU\_diode} = \frac{PDU_{proposed}}{PDU_{ACCI}} = 138\% \tag{3.15}$$

This means the diode PDU is improved 38%. (3.14) and (3.15) indicate that although extra diode D_r and small resonant capacitor C_r have been added into the proposed converter, the device utilization was improved, leading to reduction of the silicon area required to realize the power devices of the proposed converter.

3.3 Reduced switching losses

The switching losses of power electronics converter is proportional to the switching voltage and current at the switching transition of the power devices.

$$P_{sw} \propto \frac{1}{2}(VI_{on}t_r + VI_{off}t_f)f_{sw} \tag{3.16}$$

Figure 3.3 shows the switched voltage and current waveforms of the active switch and diode of the proposed converter and traditional boost-flyback reboost converter. For the main device, the switched voltages are same for both converter, however the switched current of the proposed converter is reduced compared to traditional boost-flyback reboost as a result of resonant

converter resonating back to zero at the switching transition. For the output diode, the voltage stress of traditional boost-flyback reboost is much higher than the proposed converter resulting high switching voltage. The switch current in the output diode of the proposed converter is much smaller than that of traditional boost-flyback reboost converter. Because of both smaller switched current and voltage, the switching losses of the output diode of proposed converter is lower. So due to the introduction of resonant operation in the proposed converter, the switching losses of the proposed converter is greatly reduced compared to traditional boost-flyback reboost converter. The reduced switching losses facilitates the proposed converter to achieve flat efficiency curves over wide input voltage and output power ranges, which is very desirable for microinverter applications, where weighted CEC efficiency is crucial.

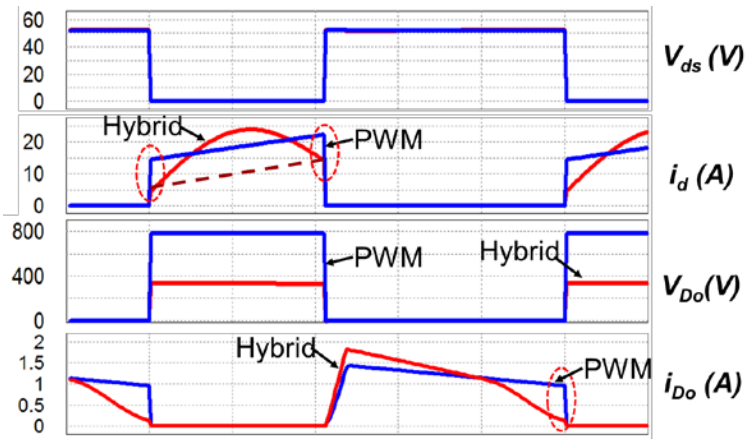


Figure 3.3 Switching waveforms of the hybrid transformer dc-dc converter and traditional boost-flyback reboost PWM dc-dc converter.

3.4 Summary

This section analyzes the suitability of the hybrid transformer dc-dc converter for microinverter applications by evaluating the PDU, MU and switching losses. The comparison between the proposed converter and traditional boost-flyback reboost PWM dc-dc converter indicates that the proposed converter has optimized MU, improved PDU and reduced switching losses over traditional coupled-inductor converter. Due to these improved performances, the hybrid transformer dc-dc converters are very attractive for PV microinverter applications.

Chapter 4 High-Efficiency Transformerless Inverter for Single-Phase Electrolyte-Free Microinverters

In SPTS microinverter, after boosting the voltage from low PV module voltage to a high DC bus voltage, a grid-tie inverter, as shown in Figure 4.1, is required to invert the high DC bus voltage into AC grid voltage feeding the energy to the grid. In small-scale grid-tie PV systems, isolation is not a mandatory if the ground leakage current is under a certain limited level demanded by the codes [D33]. Therefore, there are two circuit architecture options for SPTS microinverters, one is nonisolated dc-dc converter with high efficiency transformerless inverter, and another is isolated dc-dc converter with low-cost traditional unipolar full bridge inverter. For isolated version, the leakage current is prevented by the transformer isolation, and for the nonisolated version, the leakage current is prevented by the circuit topologies themselves.

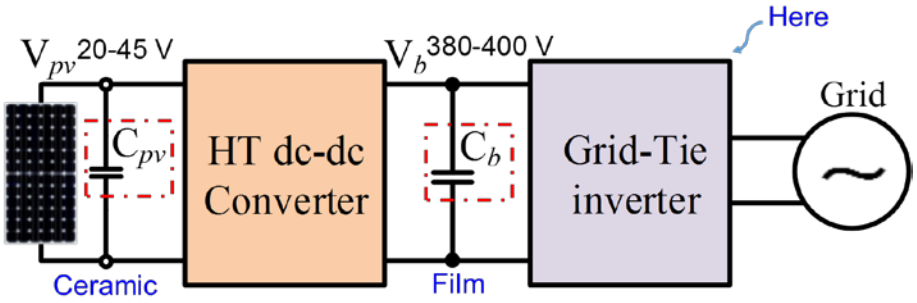


Figure 4.1 Single-phase two-stage microinverters, where a high efficiency grid-tie inverter is required to invert the high DC bus voltage to AC grid voltage.

However, even in the isolated architecture, transformerless inverter topologies may also be an optimal choice due to their relatively high efficiency and low common voltage. The penalty is the cost increase due to the added auxiliary switches using for high-frequency common mode (CM) voltage and leakage current reduction.

4.1 Common mode voltage and ground loop leakage current in single-phase two-stage microinverters

Figure 4.2 shows the system circuit diagram of SPTS microinverter with the high-frequency CM sources and the stray elements influencing the ground leakage current. The differential-mode (DM) filter capacitor C_x and the common-mode (CM) filter components L_{CM}, C_{Y1} and C_{Y2} are also shown in the model. The high-frequency CM sources includes the drain of the main switch S (point 3), the anode of the output diode D_o (point 4) of dc-dc converter, and the middle points of the inverter legs (points 1 and 2). The stray elements include (1) the stray capacitance between PV array and ground C_{PVg}, normally in the range of several to tens of nanofarads (nFs) (2) stray capacitances between power devices and the heatsink ground C_{g1}-C_{g5}, (3) stay capacitor between transformer primary and secondary side C_p, (3) the series impedance between the ground connection points of the inverter and the grid Z_g, which is mainly due to the ground stray inductance l_g; (4) the series impedances of the line conductors Z_{lineA} and Z_{lineB}, also mainly inductive.

The total ground loop leakage current is mainly induced by the CM sources with high dv/dt through all these parasitic ground loops. The CM voltage sources include two parts, one is in the scope of medium-frequency range, normally from 10 kHz to several hundreds of kHz caused by the switching frequency, and another is from the high speed of pulse rise and fall at switching transitions, and from diode reverse recovery, normally around several to hundreds of nanoseconds. The output filter L_{o1} and L_{o2}, C_f are designed for filtering the switching frequency. While the EMI filter, including L_{DM}, L_{CM}, C_X, C_Y are normally designed to filter the high-frequency caused by the high-speed switching transitions. The stray capacitor C_{g1}-C_{g5} and C_p are normally very small, in the range of tens to hundreds of picofards (pFs). If the dc-dc converter is isolated, due to the relatively small C_p in series in all these CM loops, the leakage current i_{LK} could be effectively limited. However for the nonisolated systems, since the primary and secondary sides of transformer are connected, the leakage current must be suppressed by topologies themselves, for example, transformerless inverter topologies which has minimized CM voltage sources.

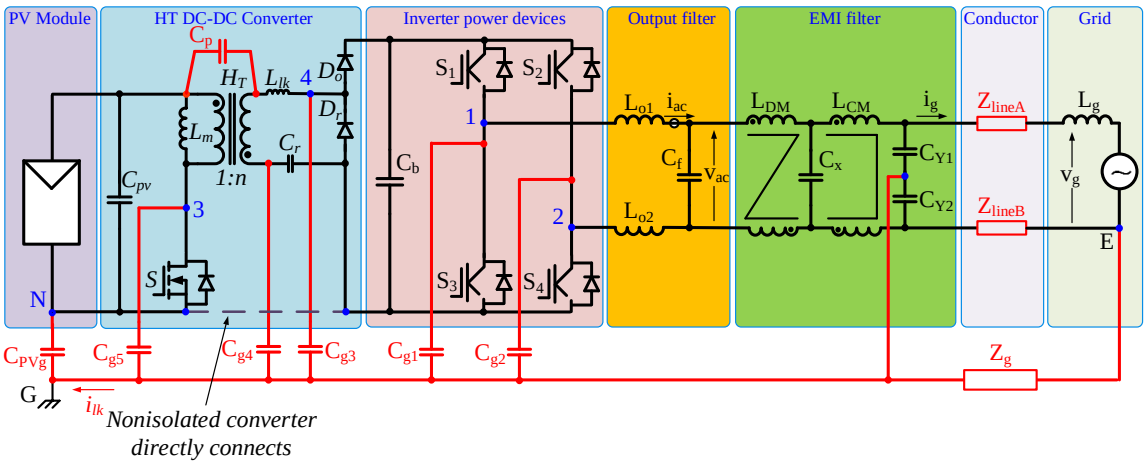


Figure 4.2 System circuit diagram with key common mode voltage sources, key parasitic elements and the total ground leakage current i_{lk}, for isolated version, i_{lk} is limited by C_p, while for nonisolated version, i_{lk} needs to be limited by topologies, i.e., minimizing the magnitude of the CM source voltages.

4.2 Basic full-bridge inverters

The simplest single-phase inverter topology is traditional full-bridge inverter, as shown in Figure 4.3. Traditional full-bridge has two versions. One has two output inductors and all switches work with high frequency, as in Figure 4.3. Another one has one output inductors with one leg running with high frequency, one leg working as line polarity selection switches, as shown in Figure 4.3(b).

4.2.1 Modulation strategies for full bridge inverters

Five modulation strategies can be used for basic full-bridge inverters: bipolar modulation, unipolar modulation and hybrid modulation1, hybrid modulation2, and hybrid modulation3, as shown in Figure 4.4.

- Bipolar modulation

In the case of bipolar modulation the switches are switched diagonal, i.e. S_1 synchronous with S_3 and S_2 with S_4, as shown in Figure 4.4(a). The sum of leg middle point voltages V_A and V_B keep constant, yielding minimized CM voltage and associated leakage current. However, the switching ripple in the current equals to switching frequency and the voltage variation across the filter is bipolar ($+V_b \rightarrow -V_b \rightarrow V_b$), which leads to high filtering requirements and high core losses. The efficiency is low due to the reactive power exchange between the AC side and DC side, and the high core losses.

- Unipolar modulation

In the case of unipolar modulation, each leg is switched according to their own references, which are complementary, as shown in Figure 4.4(b). The switching ripple in the current equals to double of the switching frequency, yielding lower filtering requirements. The efficiency can be high due to the reduced losses during the zero voltage states and the lower core losses from the unipolar voltage across the filter. However, the sum of V_A+V_B changes from $0 \rightarrow +V_b \rightarrow 0 \rightarrow -V_b \rightarrow 0$, i.e. not constant, which leads to high CM voltage and leakage current.

- Hybrid modulation

Hybrid modulation means one pair of switches works in high frequency and another pair of switches works with line frequency. There are three types of hybrid modulation strategies, which are shown in Figure 4.4 (c), (d) and (e).

The efficiency can be high due to the reduced losses during the zero voltage states, the lower core losses from the unipolar voltage across the filter, and lower switching losses of the line frequency switches. If the hybrid modulation1 is applied for the single-inductor full bridge, the CM voltage could be optimized. However, it still may have high leakage current peaks at the switching transitions of the line-frequency switches.

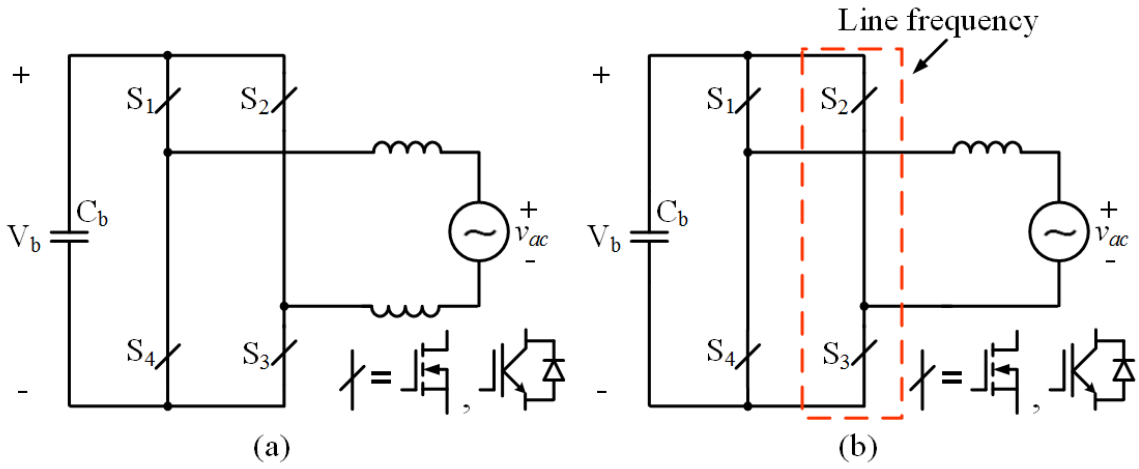
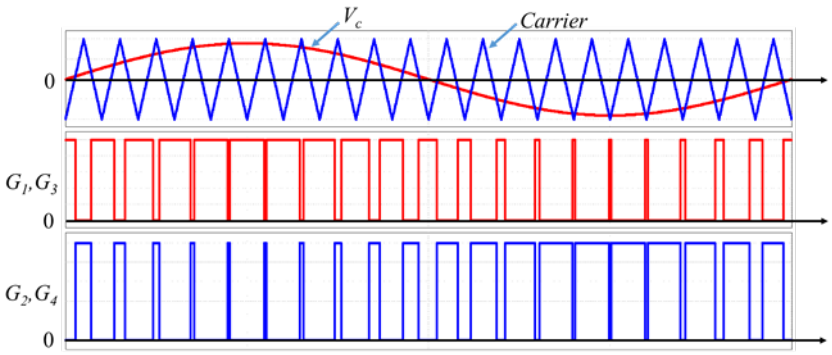
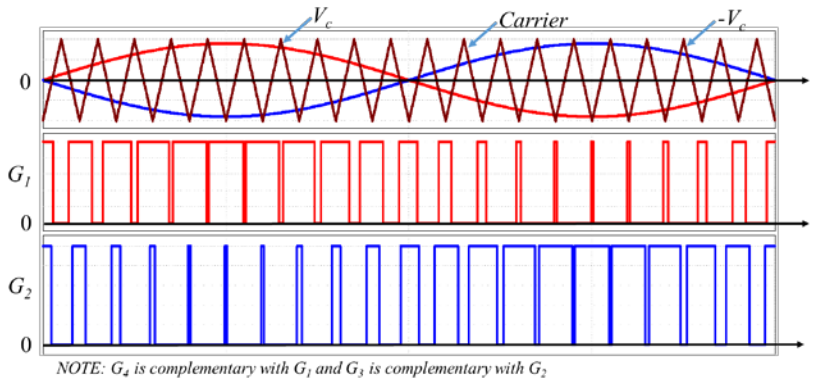


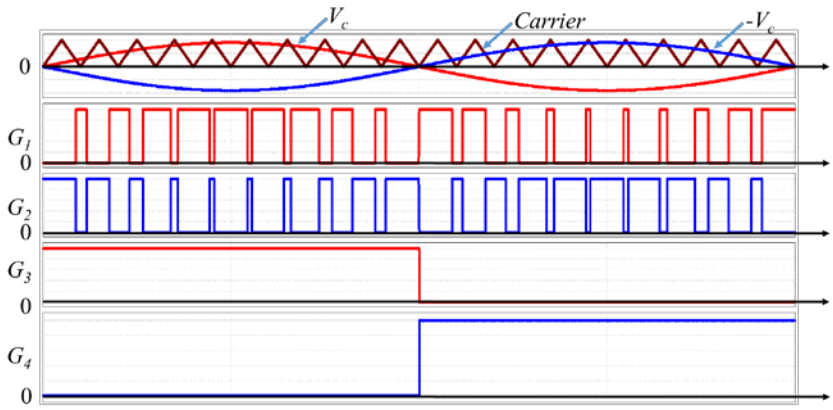
Figure 4.3 Traditional full bridge inverters: (a) with two symmetrical output inductors, (b) with single output inductor.



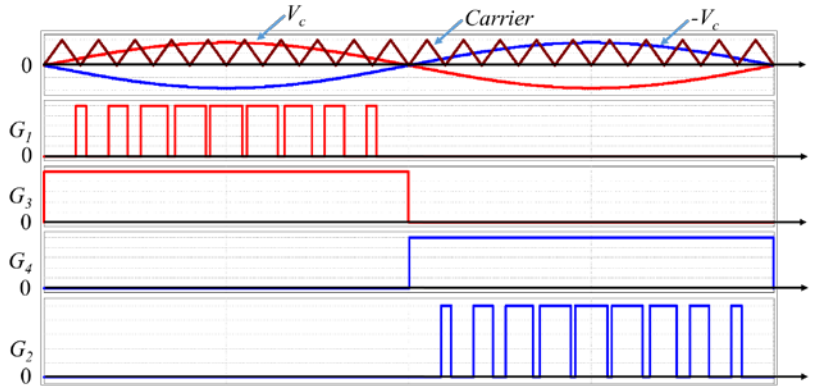
(a)


V_c
Carrier
$-V_c$
0
G_1
0
G_2
0
NOTE: G_4 is complementary with G_1 and G_3 is complementary with G_2

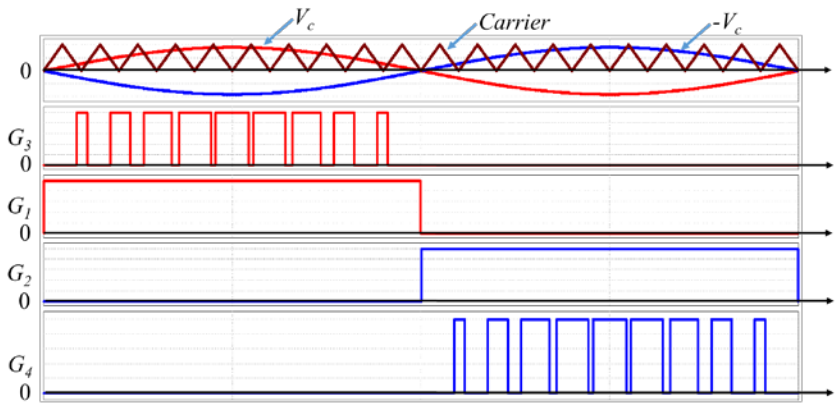
(b)


V_c
Carrier
$-V_c$
0
G_1
0
G_2
0
G_3
0
G_4
0

(c)


V_c
Carrier
$-V_c$
0
G_1
0
G_3
0
G_4
0
G_2
0

(d)

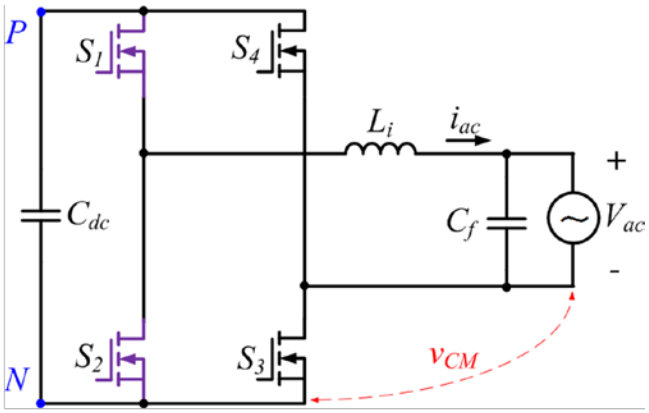


(e)

Figure 4.4 Five different modulation strategies for basic full bridge inverters: (a) bipolar modulation, (b) unipolar modulation, (c) hybrid modulation1, (d) hybrid modulation2, and hybrid modulation3. V_c represents modulation signal, Carrier is carrier signal, G_i $(i=1,2,3,4)$ represents the driver signal for switch i, G_i high means switch on and G_i low means switch off.

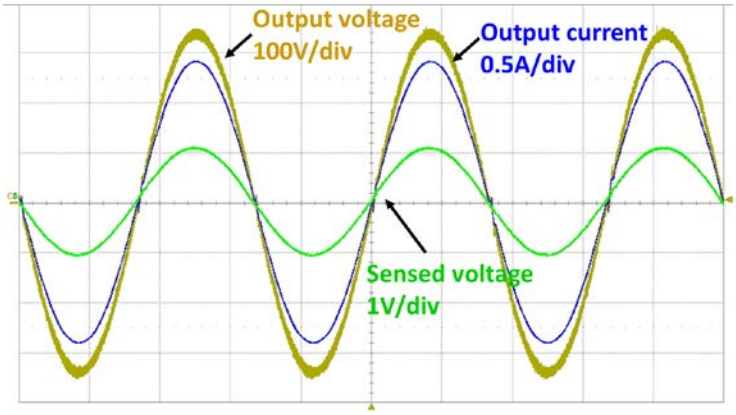
4.2.2 CM voltage test for hybrid unipolar PWM

In order to study the CM voltage of unipolar PWM, two modulation strategies, hybrid modulation1 and modulation2 were compared using the circuit configuration as shown in Figure 4.5. For hybrid modulation1, the CM voltage has 60 Hz fundamental frequency, however, at the transition of line switches, it has very high dv/dt, as shown in Figure 4.6 (b) which may lead to high peak leakage current. For hybrid modulation2, when the bottom switch of the leg without output inductor was switched as high frequency, it had very high CM voltage, as shown in Figure 4.6 (c), which introduced high EMI noise into the sensing circuitry Figure 4.6 (d).

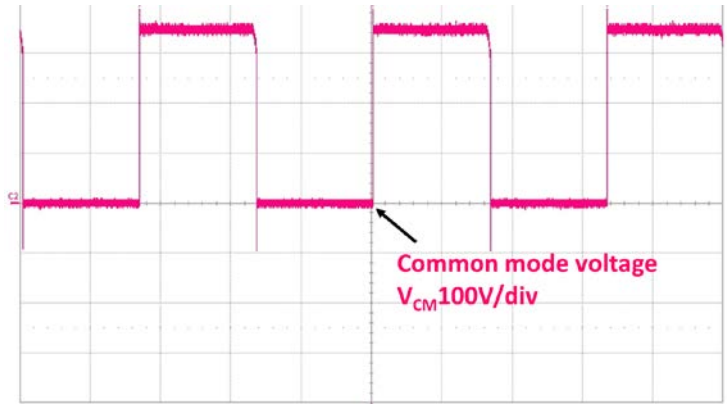


Strategy	High frequency	Line frequency
A	S2,S3	S1,S4
B	S1,S2	S3,S4

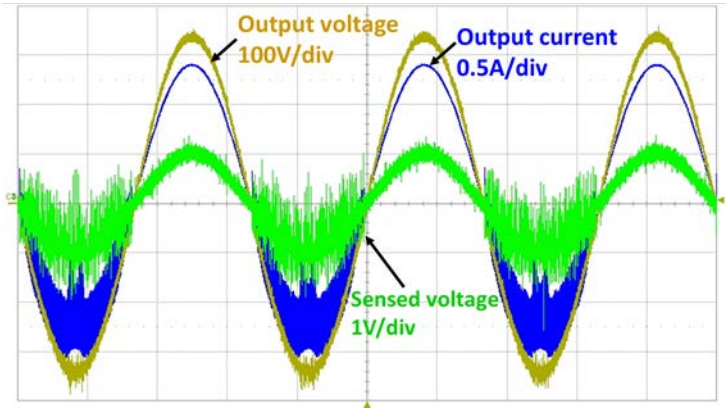
Figure 4.5 CM voltage test for single-inductor full bridge inverter with two different hybrid modulation strategies



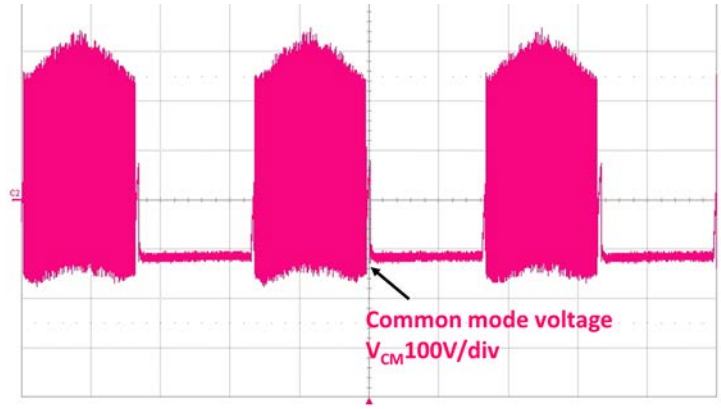
(a)



(b)



(c)



(d)

Figure 4.6 Test waveforms for CM voltages.

4.3 Transformerless inverter topologies

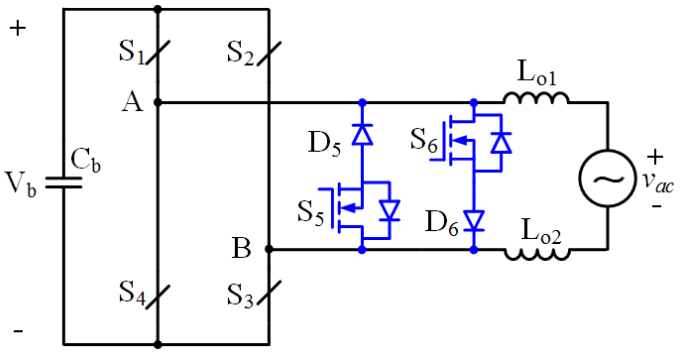
In order to use the unipolar PWM to improve the efficiency of the PV inverters while still maintaining low ground leakage current, quite a few transformerless PV inverters utilizing unipolar PWM control have been presented. The topologies can be categorized into three groups dependent on what leakage current elimination techniques they use.

4.3.1 Topologies using additional freewheeling separation switches

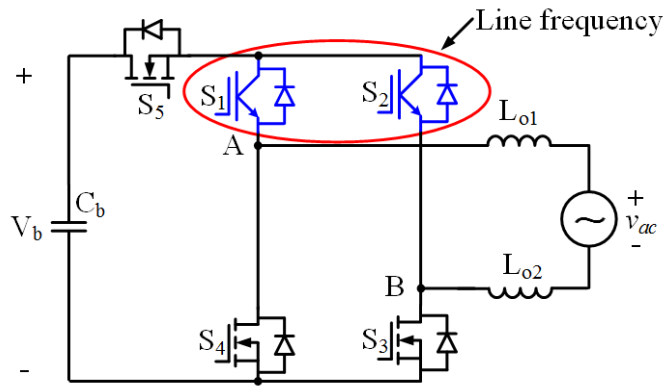
First group are topologies using additional switches to separate the DC and AC sides to eliminate the leakage current, as shown in Figure 4.7, [D5]-[D15]. This type of transformerless inverters are most popular ones for single-phase applications in industry. This group includes HERIC, H5, H6, hybrid-bridge, DC-decoupling and Zero-voltage-rectifier inverter topologies. The additional switches can allow the voltage of middle point of each legs equal to half of the DC bus voltage V_b during the freewheeling states as well as the switching transitions, i.e. $V_A + V_B = \frac{V_b}{2}$. The concept is like a "virtual three-level" converter. This can assure the sum of the voltage of these two middle points always equal to V_b, i.e. $V_A + V_B \equiv V_b$, which is equal to the cases at active states. As a results the sum of V_A and V_B keeps constantly equal to V_b within the whole switching period. This can effectively reduce the ground leakage current.

To achieve minimized leakage current by using this technique, some rules to guarantee symmetric structures should be comply:

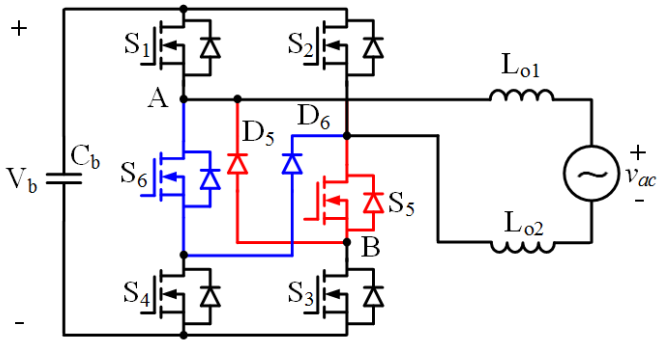
- Select MOSFETs and diodes having identical parameters
- Optimize layout to obtain symmetric parasitic parameters
- If coupled output inductors used, using bifilar winding technique
- Fix all the MOSFETs and diodes on the same heatsink



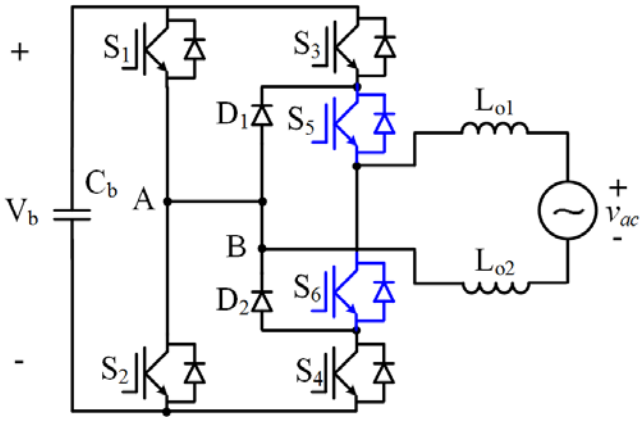
(a) Highly efficient and reliable inverter concept (HERIC) inverter topology



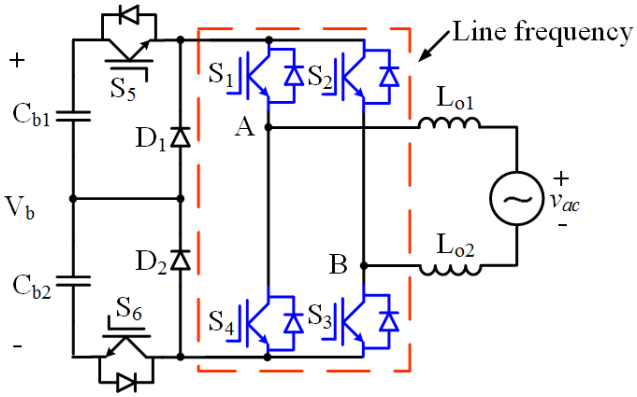
(b) H5 inverter topology



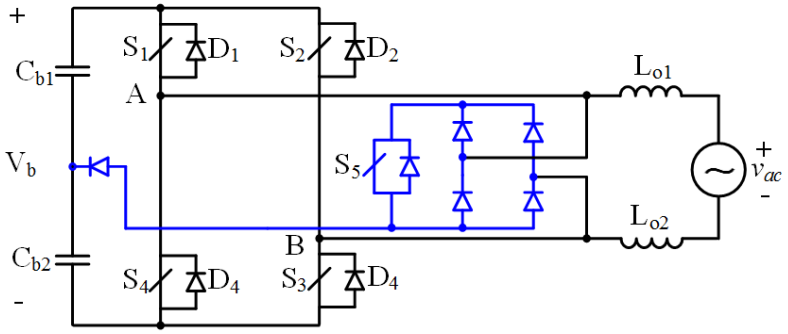
(c) H6 MOSFET inverter topology



(d) Hybrid-bridge inverter topology



(e) DC-decoupling inverter topology



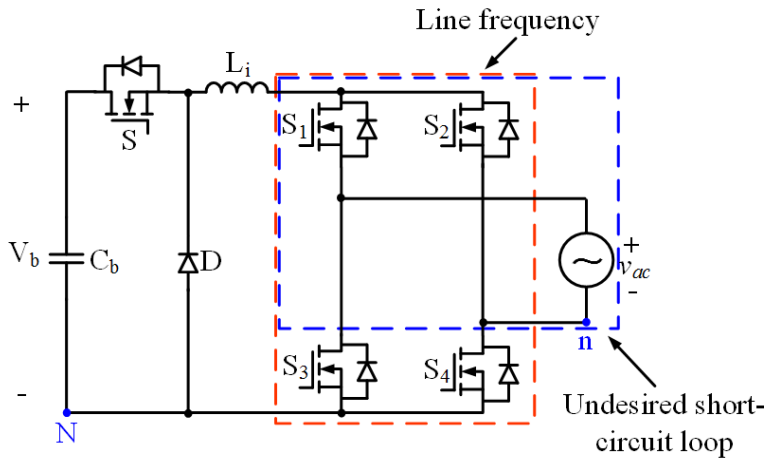
(f) Zero-voltage-rectifier inverter topology

Figure 4.7 Transformerless inverter topologies using additional freewheeling separation switches

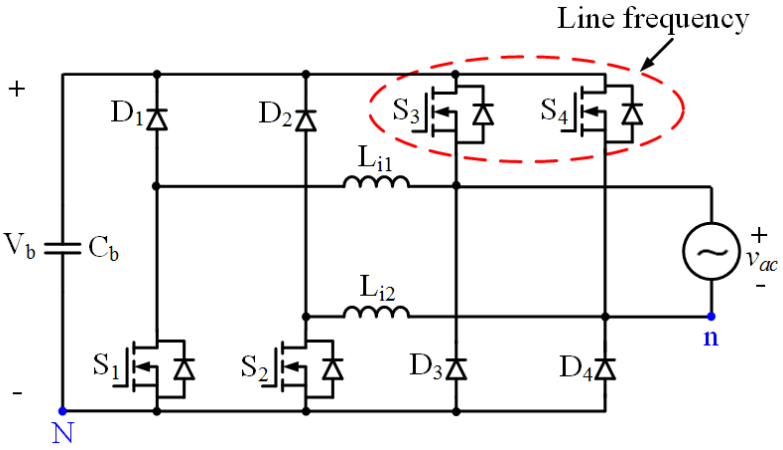
4.3.2 Topologies using asymmetrical buck-choppers

Second group of single-phase transformerless inverter topologies are asymmetrical buck-chopper based topologies, as shown in Figure 4.8, [D16], including single buck chopper inverter, dual buck negative rail, and positive rail chopper inverters. These three inverter topologies can be derived from the traditional bridge-type and bridgeless power factor correction circuits by modifying them for reverse power flow. This group of transformerless inverters use line-frequency polarity selection switches connecting the neutral point *n* of the ac with the negative point N of the DC sides both at the negative and positive half cycle of the grid to prevent the CM voltages. This group of inverters can reliably use the MOSFETs as high-frequency switches to avoid the fixed-voltage drop of IGBT devices and reduce the switching-losses. However, the main problem is the undesired short-circuit loop as shown in Figure 4.8 (a), where the active switch pair of S_1 and S_2 or S_3 and S_4 may short out the grid. So large dead time is required at the zero-crossing of grid [D16]. To enhance the reliability of this group of converters, diodes could be added in series with the polarity section switches or thyristor could be used for the line frequency switches, however at the cost of high conduction losses. Another possible solution for enhancing reliability with the application for is adding two output inductor between the ac grid and the line-frequency switches, however, the penalty is that the CM voltage will increase. Another issue with the two dual-buck type inverter topologies is

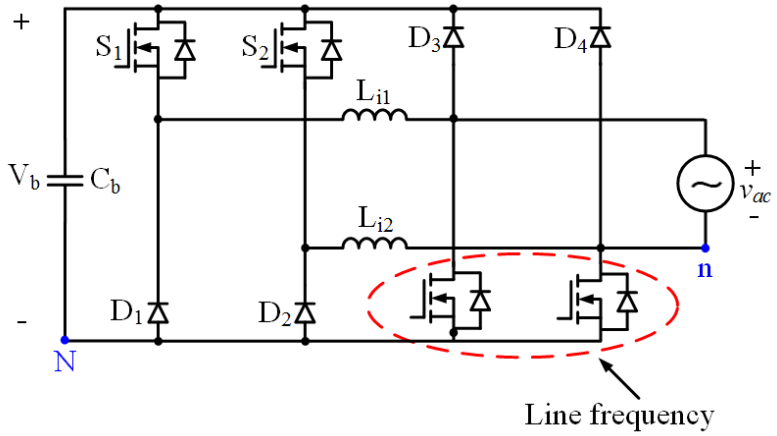
that they required two separate inductors, each of them only works in half-grid cycle resulting in half magnetic utilization and increasing the cost of the inverter system.



(a) Single buck chopper inverter



(b) Dual buck negative rail chopper inverter



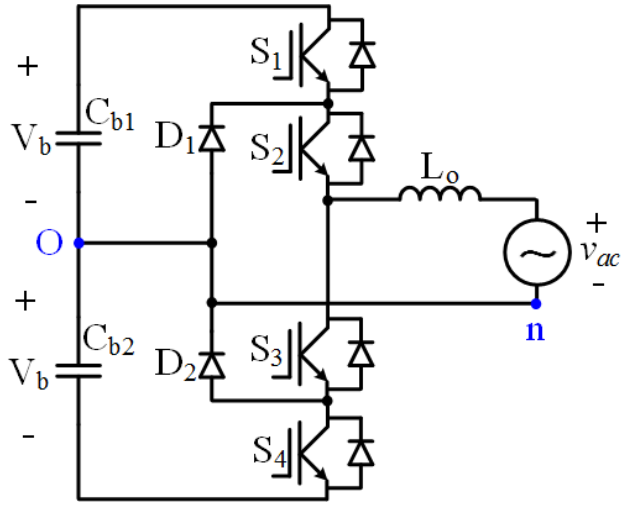
(c)Dual buck positive rail chopper inverter

Figure 4.8 Transformerless inverter topologies using asymmetrical buck-choppers

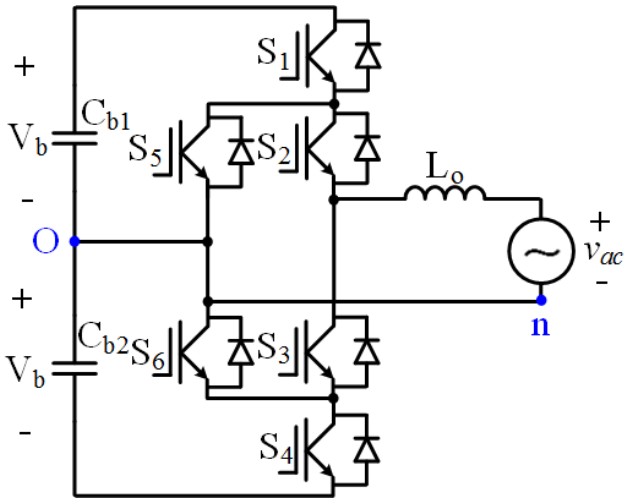
4.3.3 Topologies based on neutral-point-clamped inverter

The neutral-point-clamped (NPC) topology was introduced by Nabae, Magi and Takahashi in 1981 [D17], which has great performance in terms of dv/dt and switch voltage stress in comparison with the classical two-level full bridge inverter. Different three-level NPC inverter topologies suitable for single-phase tranformerless system applications, [D17]-[D20] including classical diode-clamped NPC inverter, active NPC (ANPC) inverter, NPC inverter with DC injection current blocking and Conergy NPC inverter, are shown in Figure 4.9 (a) to (d). The classical NPC inverter and its derived-topologies features the advantages of unipolar voltage across the filter and minimized leakage current due to the grounded DC link midpoint. The output voltage of the middle point is clamped to the middle point of the DC bus in the zero voltage state. However NPC inverters require double input

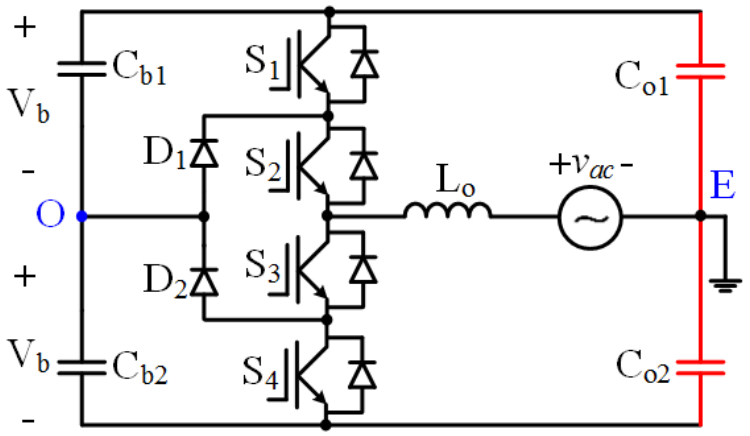
voltage in comparison with full bridge inverters. The switching losses of NPC inverters are unbalanced, higher on the higher switches and lower on the middle switches. The ANPC inverter has more than one way to clamp the midpoint to implement zero voltage state, which can be effectively used to achieve natural double frequency on the output filter and thus to reduce the size of output inductor.



(a) Three-level neutral-point-clamped (NPC) inverter topology



(b) Three-level active-neutral-point-clamped (ANPC) inverter topology



(c) Three-level neutral-point-clamped (NPC) inverter topology with DC injection current blocking

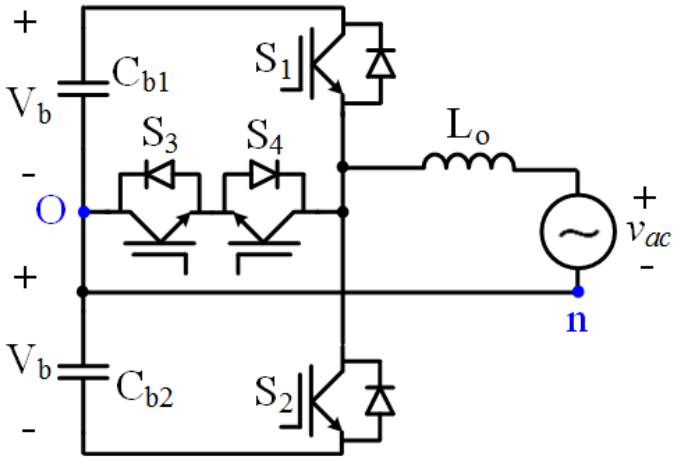


Figure 4.9 Transformerless inverter topologies based on NPC inverter.

4.4 Matched pair of Superjunction MOSFETs with SiC-Schottky diode for high efficiency PV inverter applications

To evaluate and design the transformerless inverters with high efficiency, fully understanding the loss mechanism for active devices and diodes are crucial. This section will give the loss models to facilitate understanding the advantages of using the pair of Superjunction MOSFETs and SiC diodes to

achieve ultra-high efficiency in photovoltaic inverter applications. The superjunction MOSFETs have resistive conduction loss feature which avoids the fixed voltage drop losses of IGBTs. Furthermore, they have much fast switching speed, which can significantly reduce switching losses compared to IGBTs devices. Unfortunately, the body diode of the high voltage MOSFETs have very poor reverse recovery performance. In inverter applications, the reverse recovery of ultrafast silicon diodes induced losses are also notorious. While modern SiC Shottky diodes have zero reverse recovery, which can eliminate the reverse recovery induced losses of traditional silicon diodes. If the pair of Superjunction MOSFETs and SiC Shottky diodes can be used in transformerless PV inverters, ultra high efficiency is expectable.

4.4.1 Conduction loss models

The equivalent circuits of first-order conduction loss models for MOSFETs, IGBTs and diodes are shown in Figure 4.10. The conduction loss equations are

$$MOSFET: v_{ds}(t) = i(t) \cdot R_{ds} \tag{4.1}$$

$$IGBT: v_{ce}(t) = V_t + i(t) \cdot R_{ce} \tag{4.2}$$

$$Diode: v_{ak}(t) = V_f + i(t) \cdot R_{ak} \tag{4.3}$$

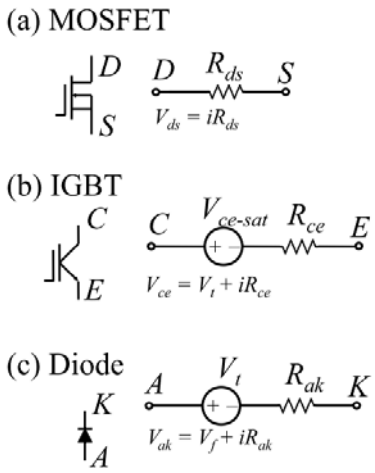


Figure 4.10 Equivalent circuits for first-order conduction loss models for MOSFETs, IGBTs and diodes

where v_{ds} is the MOSFET drain-source voltage drop, R_{ds} is the MOSFET drain-source on resistance, which are greatly dependent on the operation temperature, v_{ce} is the IGBT collector-emitter voltage drop, V_t is the IGBT equivalent voltage drop under zero current condition, R_{ce} is the IGBT on resistance, v_{ak} is the diode anode-cathode voltage drop, V_f is the diode equivalent voltage drop under zero current condition, and R_{ak} is diode on resistance.

4.4.2 Switching loss models

For MOSFET devices, the main loss source for switching transitions is the capacitive turn-on loss resulting from the discharge of the junction capacitor C_{oss} of MOSFETs [D34], which is dependent on the switched dc bus voltage and switching frequency. Normally, this capacitive turn-on energy dissipation can be obtained from the device datasheet. For example, energy stored in the output capacitor C_{oss} of IPB65R099C6 CoolMOS transistor [F9] is shown in

Figure 4.11. Hence, the switching loss of MOSFETs can be simply expressed as

$$P_{sw\_active\_MOSFET} = f_{sw} E_{oss}(V_{ds}) \tag{4.4}$$

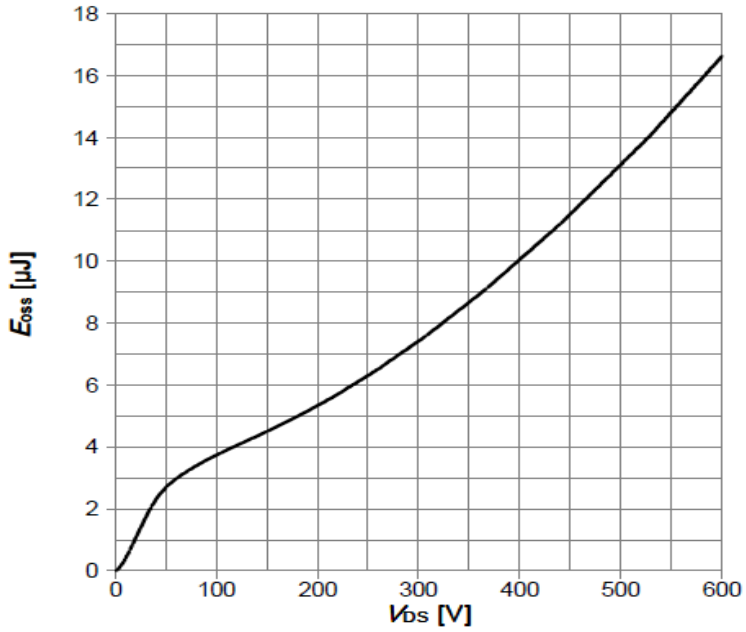


Figure 4.11 Typical C_{oss} stored energy from datasheet of Infineon IPB65R099C6 CoolMOS transistor [F9]

Another part of switching losses of active switches is induced by the diode reverse recovery. The switching energy induced in the main switches during diode reverse recovery period can be approximated as

$$E_{d\_rr} = V_{dc} I_L [(1 + \frac{I_{rr}}{2I_L}) t_a + \frac{I_{rr}}{4I_L} t_b] = V_{dc} I_L t_a + V_{dc} \frac{I_{rr}}{4} (2t_a + t_b) \tag{4.5}$$

Where I_L is the switched load current, and the definitions of t_a, t_b, and I_{rr} are shown in Figure 4.12.

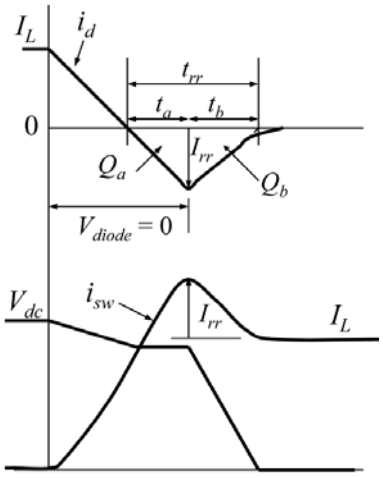


Figure 4.12 Simplified waveforms showing switching losses induced in the main switches and diodes during diode reverse recovery.

The third part of the switching losses is the switching loss induced in the diode during the diode reverse recovery interval, which can be approximated as

$$P_{d\_sw} = f_{sw}(0.5I_{rr})(0.5V_{dc})t_b \tag{4.6}$$

If these two losses are induced by the body diodes of MOSFETs, due to the fact that very high Q_{rr} and long t_a+t_b of the body diodes of MOSFETs, the loss would be very much worse, even killing the devices.

The switching energy of IGBTs caused the overlap of switched current and voltage during the turn-on and turn-off transitions can be estimated as

$$E_{sw\_on} = \alpha_{on} \mathrm{I_m}^{\beta_{on}} k_{g\_on} \frac{V_{dc}}{V_{test}} \tag{4.7}$$

$$E_{sw\_off} = \alpha_{off} \mathrm{I_m}^{\beta_{off}} k_{g\_off} \frac{V_{dc}}{V_{test}} \tag{4.8}$$

where k_{g_on} is gate drive stiffness factor during turn-on; k_{g_off} is gate drive stiffness factor during turn-off; α_{on} and β_{on} are turn-on energy coefficients; α_{off} and β_{off} are turn-off energy coefficients; V_{dc} is the actual switched dc bus voltage and V_{test} is test voltage for switching energy coefficients on the IGBT datasheets. α_{on}, β_{on}, α_{off} and β_{off} can be obtained through matlab curve fitting based on the E_{on} and E_{off} of IGBT datasheet. For example the typical switching energy of an IGBT device IGB15N60T from Infineon is shown in Figure 4.13.

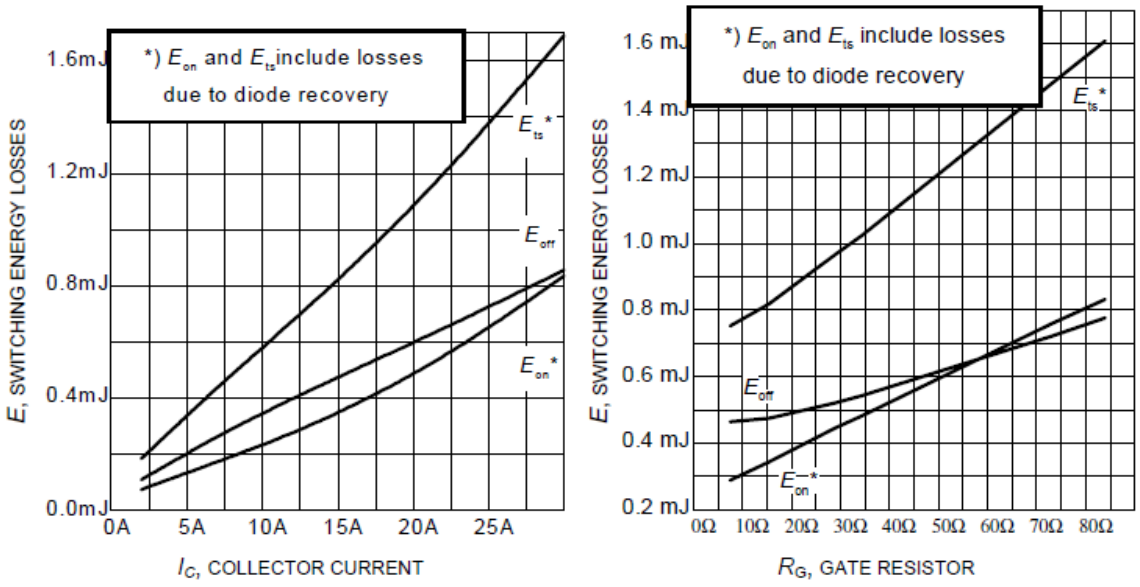


Figure 4.13 Typical switching energy losses of IGB15N60T IGBT [F10], (a) as a function of collector current and (b) as a function of gate resistor. (Test conditions: inductive load, T_j=175°C, V_{CE}=400 V, V_{GE}=0/15 V, R_g=15Ω)

From the loss models, we can see, if MOSFET devices could be used for the transformerless inverters, the fixed-voltage conduction loss of IGBTs would be reduced and also the switching overlap could be reduced due to the

fast switching speed of MOSFETs, yielding reduced switching losses as well. However, the conduction of body diodes of MOSFETs should be eliminated to avoid the slow reverse recovery of silicon MOSFETs. If SiC Shottky diode instead of ultrafast silicon diodes were used in transformerless inverters, the losses induced in active switches and the diodes themselves by the reverse recovery of silicon diodes could be eliminated, significantly reducing the switching losses. So the topologies which has the ability to use MOSFETs as main devices then combined with SiC diodes are very desirable for achieving ultrahigh efficiency in PV inverters.

4.5 Proposed high reliability and high efficiency transformerless inverter

Transformerless photovoltaic (PV) grid-connected inverters have the advantages of higher efficiency, lower cost, less complexity, and smaller volume compared to their counterparts with transformer galvanic isolation [D1]-[D31]. High-frequency common-mode (CM) voltages must be avoided for a transformerless PV grid-connected inverter because it will lead to a large charge/discharge current partially flowing through the inverter to the ground. This CM ground current will cause an increase in the current harmonics, higher losses, safety problems and electromagnetic interference (EMI) issues [D21]-[D30]. For a grid-connected PV system, energy yield and payback time are greatly dependent on the inverter's reliability and efficiency, which are regarded as two of the most significant characteristics for PV inverters.

In order to minimize the ground leakage current and improve the efficiency

of the converter system, transformerless PV inverters utilizing unipolar PWM control have been presented [D5]-[D20]. The weighted California Energy Commission (CEC) or European Union (EU) efficiencies of most commercially available and literature-reported single-phase PV transformerless inverters are in the range of 96%-98% [D12]. Several transformerless inverter topologies have been presented that use superjunction MOSFETs devices [D7], [D9], [D16] as main switches to avoid the fixed voltage-drop and the tail-current induced turn-off losses of IGBTs to achieve ultra-high efficiency (over 98% weighted efficiency).

One commercialized unipolar inverter topology, H5, as shown in Figure 4.7 (b) solves the ground leakage current issue and uses hybrid MOSFET and IGBT devices to achieve high efficiency [D7]. The reported system peak and CEC efficiencies with an 8 kW converter system from the product datasheet is 98.3% and 98% respectively with 345V DC input voltage and a 16 kHz switching frequency. However this topology has high conduction losses due to the fact that the current must conduct through three switches in series during the active phase. Another disadvantage of the H5 is that the line-frequency switches S_1 and S_2 cannot utilize MOSFET devices because of the MOSFET body diode's slow reverse-recovery. The slow reverse-recovery of the MOSFET body diode induces large turn-on losses, and has a higher possibility of damage to the devices and leads to EMI problems. Shoot-through issues associated with traditional full bridge PWM inverters remain

in the H5 topology due to the fact that the three active switches are series-connected to the dc bus.

Replacing the switch S_5 of the H5 inverter with two split switches S_5 and S_6 into two phase legs and adding two freewheeling diodes D_5 and D_6 for freewheeling current flows, the H6 topology, as shown in Figure 4.7 (c) was proposed in [D9]. The H6 inverter can be implemented using MOSFETs for the line frequency switching devices, eliminating the use of less efficient IGBTs. The reported peak efficiency and EU efficiency of a 300 W prototype circuit were 98.3% and 98.1% respectively with 180 V DC input voltage and 30 kHz switching frequency [D9]. The fixed-voltage conduction losses of the IGBTs used in the H5 inverter are avoided in the H6 inverter topology improving efficiency; however, there are higher conduction losses due to the three series-connected switches in the current path during active phases. The shoot-through issues due to three active switches series-connected to the dc-bus still remain in the H6 topology. Another disadvantage to the H6 inverter is that when the inverter output voltage and current has a phase shift the MOSFET body diodes may be activated. This can cause body diode reverse-recovery issues and decrease the reliability of the system.

Another high efficiency transformerless MOSFET inverter topology is the dual buck chopper inverter, as shown in Figure 4.8 (b) or (c). The dual buck chopper inverter was inversely-derived from the dual-boost bridgeless power-factor correction (PFC) circuit in [D16]. The dual buck chopper inverter

eliminates the problem of high conduction losses in the H5 and H6 inverter topologies because there are only two active switches in series with the current path during active phases. The reported maximum and EU efficiencies of the dual-paralleled-buck inverter using CoolMOS switches and SiC diodes tested on a 4.5 kW prototype circuit were 99% and 98.8% respectively with an input voltage of 375 V and a switching frequency at 16 kHz [D16]. However, the main issue of this topology is that the grid is directly connected by two active switches S_3 and S_4, which may cause a grid short-circuit problem, reducing the reliability of the topology. A dead-time of 500 μs between the line-frequency switches S_3 and S_4 at the zero-crossing instants needed to be added to avoid grid shoot-through [D16]. This adjustment to improve the system reliability comes at the cost of high zero-crossing distortion for the output grid current.

As analyzed above, one key issue for a high efficiency and reliability transformerless PV inverter is that in order to achieve high efficiency over a wide load range it is necessary to utilize MOSFETs for all switching devices. Another key issue is that the inverter should not have any shoot-through issues for higher reliability. In order to address these two key issues, a new inverter topology is proposed for single-phase transformerless PV grid-connected systems in this section. The proposed transformerless PV inverter features: (1) high reliability because there are no shoot-through issues, (2) low output ac current distortion as a result of no dead-time requirements at

every PWM switching commutation instant as well as at grid zero-crossing instants, (3) minimized common-mode leakage current because there are two additional ac-side switches that decouple the PV array from the grid during the freewheeling phases and (4) all the active switches of the proposed converter can reliably employ superjunction MOSFETs since it never has the chance to induce MOSFET body diode reverse-recovery. As a result of the low conduction and switching losses of the superjunction MOSFETs, the proposed converter can be designed to operate at higher switching frequencies while maintaining high system efficiency. Higher switching frequencies reduce the ac-current ripple and the size of passive components.

Detailed power stage operation principle, PWM scheme and common-mode leakage current analysis will be described. The total losses of power devices for several existing MOSFET inverters are comparatively evaluated. The loss reduction by replacing IGBTs with superjunction MOSFETs as power switches for the proposed transformerless inverter is analyzed and experimentally demonstrated. To verify the effectiveness and demonstrate the performance of the proposed transformerless inverter, a 250 W prototype circuit was built and tested with the switching frequency 24 kHz. Experimental results show that the proposed inverter topology not only eliminates the issues of MOSFET body diode reverse-recovery, ground leakage current and shoot-through; it also achieves 99.1% maximum efficiency and 98.6% CEC efficiency with high quality output current

waveforms.

4.5.1 Proposed topology and operation analysis

Figure 4.14 shows the circuit diagram of the proposed transformerless PV inverter topology, which is composed of six MOSFETs switches (S_1-S_6), six diodes (D_1-D_6), and two split ac-coupled inductors L_1 and L_2. The diodes D_1-D_4 perform voltage clamping functions for active switches S_1-S_4. The ac-side switch pairs are composed of S_5, D_5 and S_6, D_6 respectively, which provide unidirectional current flow branches during the freewheeling phases decoupling the grid from the PV array and minimizing the common-mode leakage current. Compared to the HERIC topology [D5] the proposed inverter topology divides the AC side into two independent units for positive and negative half cycle. In addition to the high efficiency and low leakage current features, the proposed transformerless inverter avoids shoot-through enhancing the reliability of the inverter. The inherent structure of the proposed inverter does not lead itself to the reverse recovery issues for the main power switches and as such superjunction MOSFETs can be utilized without any reliability or efficiency penalties.

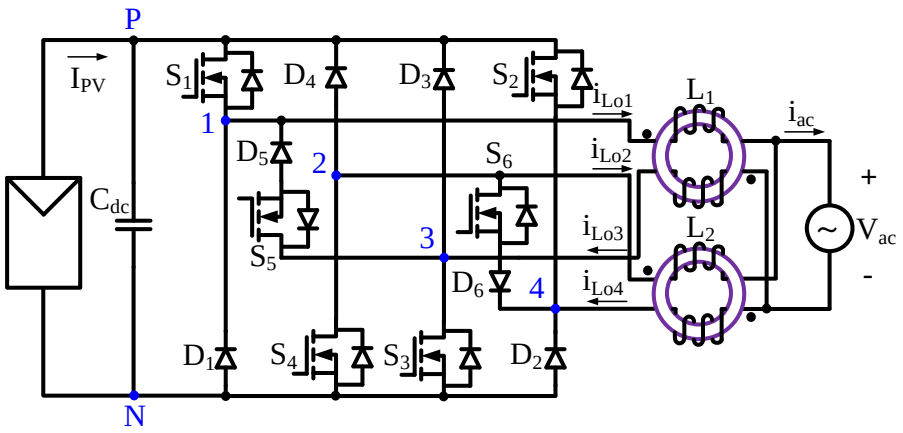


Figure 4.14 Proposed high efficiency and reliability PV transformless inverter topology

Figure 4.15 illustrates the PWM scheme for the proposed inverter. When the reference signal $V_{control}$ is higher than zero, MOSFETs S_1 and S_3 are switched simultaneously in the PWM mode and S_5 is kept on as a polarity selection switch in the half grid cycle; the gating signals G_2, G_4 and G_6 are low and S_2, S_4 and S_6 are inactive. Similarly, if the reference signal $-V_{control}$ is higher than zero, MOSFETs S_2 and S_4 are switched simultaneously in the PWM mode and S_6 is on as a polarity selection switch in the grid cycle; the gating signals G_1, G_3 and G_5 are low and S_1, S_3 and S_5 are inactive.

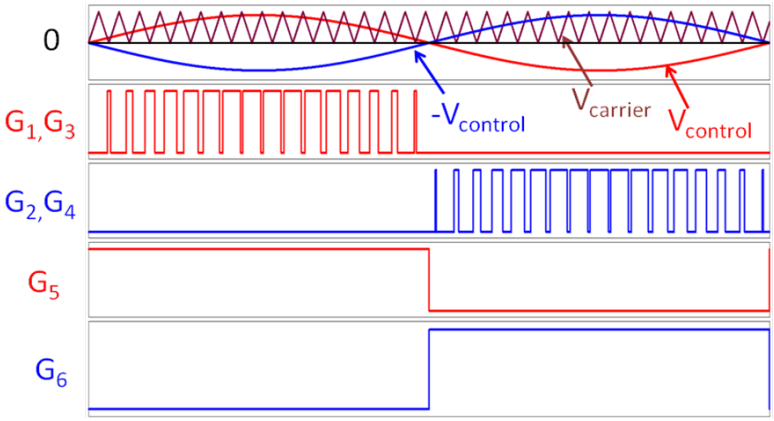
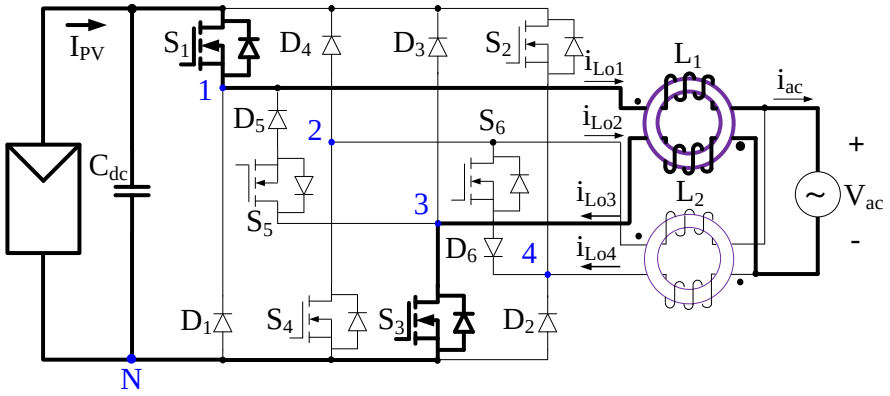
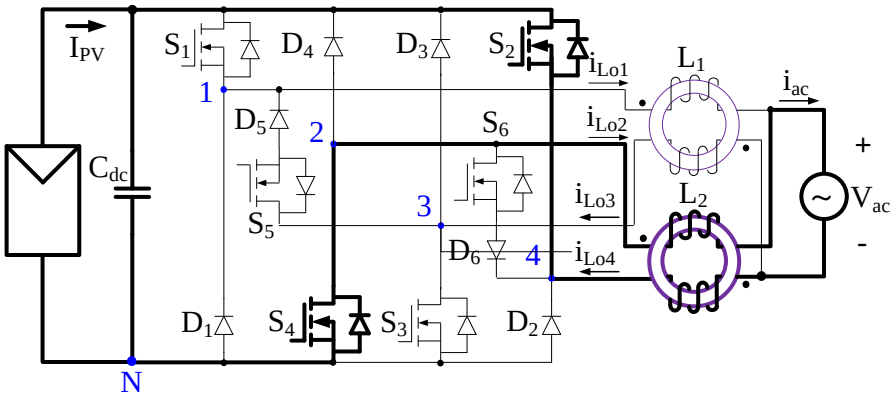


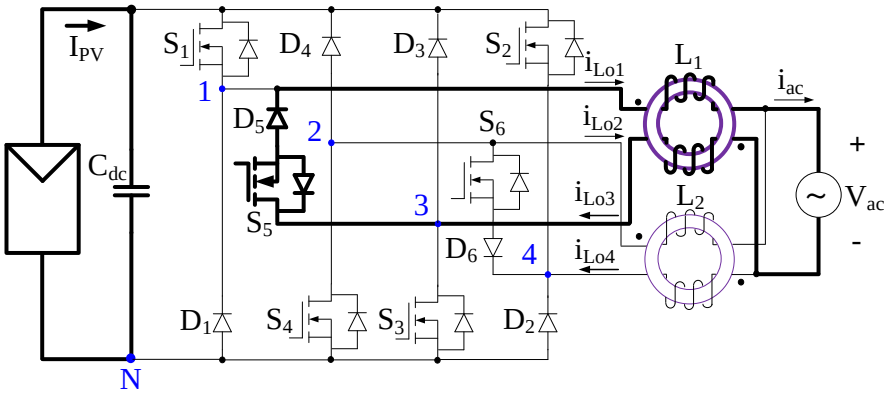
Figure 4.15 Gating signals of proposed transformerless PV inverter


I_{PV}
S_1
D_4
D_3
S_2
i_{Lo1}
L_1
i_{ac}
1
D_5
2
S_6
i_{Lo2}
+
C_{dc}
S_5
3
i_{Lo3}
L_2
~
V_{ac}
D_6
4
i_{Lo4}
-
D_1
S_4
S_3
D_2
N

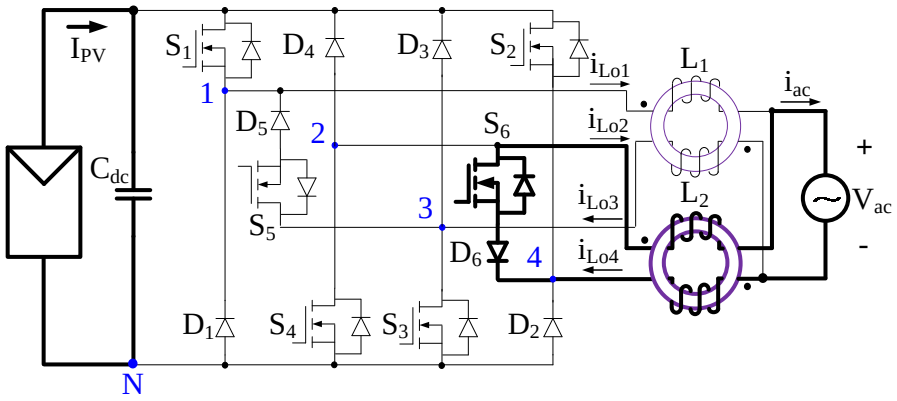
(a)


I_{PV}
S_1
D_4
D_3
S_2
i_{Lo1}
L_1
i_{ac}
1
D_5
2
S_6
i_{Lo2}
+
C_{dc}
S_5
3
i_{Lo3}
L_2
~
V_{ac}
D_6
4
i_{Lo4}
-
D_1
S_4
S_3
D_2
N

(b)


I_{PV}
S_1
D_4
D_3
S_2
i_{Lo1}
L_1
i_{ac}
1
D_5
2
S_6
i_{Lo2}
+
C_{dc}
S_5
3
i_{Lo3}
L_2
~
V_{ac}
D_6
4
i_{Lo4}
-
D_1
S_4
S_3
D_2
N

(c)



(d)

Figure 4.16 Topological stages of the proposed inverter: (a) active stage of positive half-line cycle, (b) freewheeling stage of positive half-line cycle, (c) active stage of negative half-line cycle, and (d) freewheeling stage of negative half-line cycle.

Figure 4.16 shows the four operation stages of the proposed inverter within one grid cycle. In the positive half-line grid cycle, the high frequency switches S_1 and S_3 are modulated by the sinusoidal reference signal $V_{control}$ while S_5 remains turned on. When S_1 and S_3 are on, diode D_5 is reverse-biased, the inductor currents of i_{Lo1} and i_{Lo3} are equally charged, and energy is transferred from the dc source to the grid; when S_1 and S_3 are deactivated, the switch S_5 and diode D_5 provide the inductor current i_{L1} and i_{L3} a freewheeling path decoupling the PV panel from the grid to avoid the CM leakage current. Coupled-inductor L_2 is inactive in the positive half-line grid cycle. Similarly, in the negative half cycle, S_2 and S_4 are switched at high frequency and S_6 remains on. Freewheeling occurs through S_6 and D_6.

4.5.2 Leakage current analysis for the proposed transformerless inverter

A galvanic connection between the ground of the grid and the PV array exists in transformerless grid-connected PV systems. Large ground leakage currents may appear due to the high stray capacitance between the PV array and the ground [D21]-[D30]. In order to analyze the ground loop leakage current, Figure 4.17 shows a model with the phase output points 1, 2, 3, and 4 modeled as controlled voltage sources connected to the negative terminal of the dc bus (N point). Figure 4.17 clearly illustrates the stray elements influencing the ground leakage current, which include (1) the stray capacitance between PV array and ground C_{PVg}, (2) stray capacitances between the inverter devices and the ground C_{g1}-C_{g4}, and (3) the series impedance between the ground connection points of the inverter and the grid Z_g. The differential-mode (DM) filter capacitor C_x and the common-mode (CM) filter components L_{CM}, C_{Y1} and C_{Y2} are also shown in the model.

The value of the stray capacitances C_{g1}, C_{g2}, C_{g3} and C_{g4} of MOSFETs is very low compared with that of C_{PVg}, therefore the influence of these capacitors on the leakage current can be neglected. It is also noticed that the DM capacitor C_x does not affect the CM leakage current. Moreover, during the positive half-line cycle, switches S_2, S_4 and S_6 are kept deactivated; hence the controlled voltage sources V_{2N} and V_{4N} are equal to zero and can be removed. Consequently, a simplified CM leakage current model for the positive half-line cycle is derived as shown in Figure 4.18.

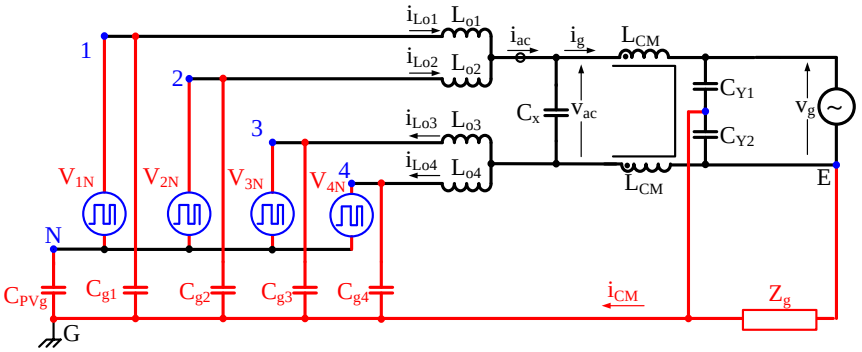


Figure 4.17 Leakage current analysis model for the proposed transformerless PV inverter

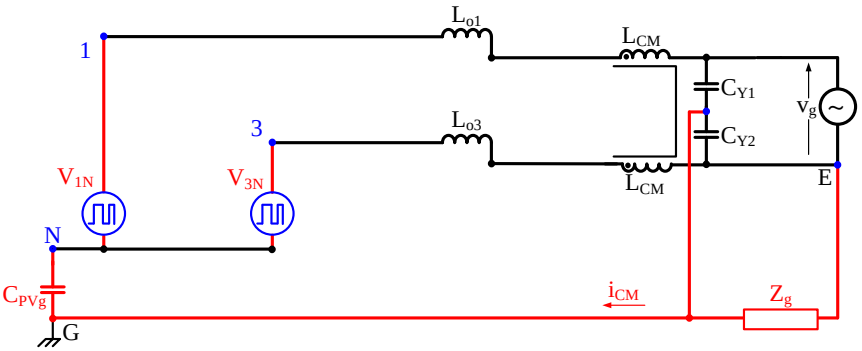


Figure 4.18 Simplified CM leakage current analysis model for positive half-line cycle

With the help of the CM and DM concepts and by introducing the equivalent circuits between N and E, a single-loop mode applicable to the CM leakage current analysis for the positive half-line cycle of the proposed transformerless inverter is obtained, as shown in Figure 4.19, with

$$V_{CM} = \frac{V_{1N} + V_{3N}}{2} \tag{4.9}$$

$$V_{DM} = V_{1N} - V_{3N} \tag{4.10}$$

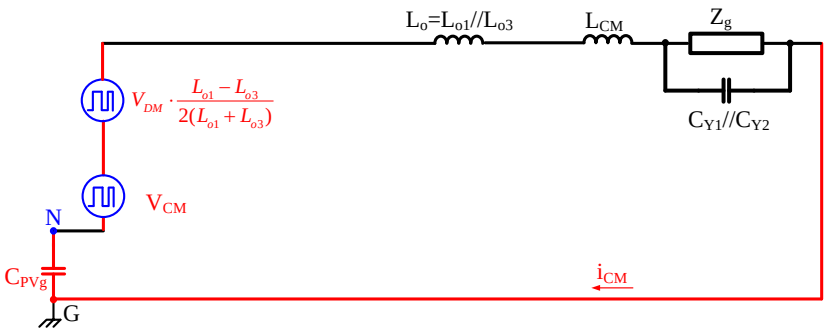


Figure 4.19 Simplified single-loop CM model for positive half-line cycle

A total CM voltage V_{tCM} [D21] is defined as

$$V_{tCM} = V_{CM} + V_{DM} \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} = \frac{V_{1N} + V_{3N}}{2} + (V_{1N} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} \tag{4.11}$$

It is clear that if the total CM voltage V_{tCM} keeps constant, no CM current flows through the converter. For a well-designed circuit with symmetrically structured magnetics, normally L_{o1} is equal to L_{o3}. During the active stage of the positive half-line cycle, V_{1N} is equal to V_{dc}, while V_{3N} is equal to 0. Hence the total CM voltage can be calculated as

$$V_{tCM} = \frac{V_{1N} + V_{3N}}{2} + (V_{1N} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} = \frac{V_{dc}}{2} \tag{4.12}$$

During the freewheeling stage of the positive half-line cycle, under the condition that S_1 and S_3 share the dc-link voltage equally when they are simultaneously turned off, one can obtain

$$V_{1N} = V_{3N} = \frac{V_{dc}}{2} \tag{4.13}$$

Therefore the total CM voltage during the freewheeling stage is calculated as

$$V_{tCM} = \frac{V_{1N} + V_{3N}}{2} + (V_{1N} - V_{3N}) \cdot \frac{L_{o1} - L_{o3}}{2(L_{o1} + L_{o3})} = \frac{V_{dc}}{2} \tag{4.14}$$

Equations (4.12) and (4.14) indicate that the total CM voltage keeps constant in the whole positive half-line cycle. As a result, no CM current is excited. Similarly, during the whole negative half-line cycle, the CM leakage current mode is exactly the same as the one during the positive half-line cycle; the only difference is the activation of different devices. The total CM voltage in the negative half-line cycle is also equal to $V_{dc}/2$. Therefore, in the whole grid cycle the total CM voltage keeps constant, minimizing CM ground leakage current.

4.5.3 Calculation and comparison of the power semiconductor device losses for Several Existing MOSFET transformerless Inverters

Since the efficiency of PV transformerless inverters is normally compared by using weighted efficiency concepts, such as "CEC Efficiency" and "EU Efficiency," it is critical to evaluate power semiconductor device losses at different load conditions rather than at nominal load condition when evaluating the efficiency of MOSFET transformerless PV inverters. The specifications and power devices for efficiency evaluation of several existing MOSFET transformerless PV inverters [D7], [D9], [D16] and the proposed inverter are listed in Table 4-1.

Table 4-1 Specification and power devices for efficiency evaluations

Nominal input voltage	380V
Grid voltage	240Vac
Nominal frequency	60Hz
Nominal output power	250 W

Nominal AC current	1.04 A
Switching frequency	24kHz
MOSFETs	IPB60R099C6
IGBTs	IGB15N60T
Diodes	Lxa08b600

Assuming the inverter output current expressed as

$$i(t) = \mathrm{I_m} \cdot \sin(\omega t) \tag{4.15}$$

where $\mathrm{I_m}$ is the peak inverter output current and ω is the angular frequency of the inverter output current. The duty ratios for active-stage devices and zero-stage devices of unipolar grid-connected PWM inverters are expressed as (4.16) and (4.17) respectively

$$d_{active}(t) = M \sin(\omega t) \tag{4.16}$$

$$d_{zero}(t) = 1 - M \sin(\omega t) \tag{4.17}$$

The conduction losses for active-stage MOSFET switches, active-stage IGBT switches, zero-stage MOSFET switches, zero-stage IGBT switches and zero-stage diodes can be calculated respectively from (4.18) to (4.22)

$$P_{con\_active\_MOSFET} = \frac{1}{2\pi}\int_0^{\pi} i(t) v_{ds}(t) d_{active}(t) d\omega t = I_m{}^2 R_{ds} \frac{2M}{3\pi} \tag{4.18}$$

$$P_{con\_active\_IGBT} = \frac{1}{2\pi}\int_0^{\pi} i(t) v_{ce}(t) d_{active}(t) d\omega t = \mathrm{I_m} V_t \frac{M}{4} + \mathrm{I_m}{}^2 R_{ce} \frac{2M}{3\pi} \tag{4.19}$$

$$P_{con\_zero\_MOSFET} = \frac{1}{2\pi}\int_0^{\pi} i(t) v_{ds}(t) d_{zero}(t) d\omega t = I_m{}^2 R_{ds} (\frac{1}{4} - \frac{2M}{3\pi}) \tag{4.20}$$

$$P_{con\_zero\_IGBT} = \frac{1}{2\pi}\int_0^{\pi} i(t) v_{IGBT}(t) d_{zero}(t) d\omega t = \mathrm{I_m} V_t (\frac{1}{\pi} - \frac{M}{4}) + \mathrm{I_m}{}^2 R_{ce} (\frac{1}{4} - \frac{2M}{3\pi}) \tag{4.21}$$

$$P_{con\_zero\_Diode} = \frac{1}{2\pi}\int_0^{\pi} i(t) v_{ak}(t) (1 - M \sin(\omega t)) d\omega t = \mathrm{I_m} V_f (\frac{1}{\pi} - \frac{M}{4}) + \mathrm{I_m}{}^2 R_{ak} (\frac{1}{4} - \frac{2M}{3\pi}) \tag{4.22}$$

For MOSFET devices, the switching loss can be estimated as

$$P_{sw\_active\_MOSFET} = f_{sw} E_{oss}(V_{ds}) \tag{4.23}$$

Another part of switching losses of active switches is induced by the diode reverse recovery of the zero-stage diodes. The switching energy induced in the main switches during diode reverse recovery period can be approximated as

$$E_{d\_rr} = V_{dc} I_L[(1+\frac{I_{rr}}{2I_L})t_a + \frac{I_{rr}}{4I_L}t_b] = V_{dc} I_L t_a + V_{dc}\frac{I_{rr}}{4}(2t_a + t_b) \tag{4.24}$$

Where I_L is the switched load current, and the definitions of t_a, t_b, and I_{rr} are shown in Figure 4.12.

The switching loss of active-stage switches induced by the diode reverse recovery of the zero-stage devices can be obtained by the integral of equation (4.6) in the whole grid cycle

$$P_{d\_rr} = \frac{1}{2\pi}\int_0^{\pi} f_{sw}[V_{dc} \mathrm{I_m} \sin(\omega t)t_a + V_{dc}\frac{I_{rr}}{4}(2t_a + t_b)]d\omega t = (\frac{\mathrm{I_m} t_a}{\pi} + \frac{I_{rr}(2t_a + t_b)}{8})V_{dc} f_{sw} \tag{4.25}$$

The third part of the switching losses is the switching loss induced in the diode during the diode reverse recovery interval, which can be approximated as

$$P_{d\_sw} = f_{sw}(0.5I_{rr})(0.5V_{dc})t_b \tag{4.26}$$

By substituting the parameters from the datasheets of IPB60R099C6 [F9], IGB15N60T [F10] and Lxa08b600 [F11], the total losses calculated for CEC efficiency evaluation for H5, H6, and the dual buck chopper (abbreviated as DBC) transformerless PV inverters and the proposed inverter are listed in

Table 4-2. It can be seen that the total power semiconductor device losses for H5 is highest due to the IGBT's fixed voltage-drop. The power devices' losses of DBC and the proposed inverters are minimum and the proposed inverter can achieve the same high efficiency as the MOSFET DBC inverter.

Table 4-2 Total losses of power devices at different CEC output power conditions at 24 kHz switching frequency

Po (%)	H5 (W)	H6 (W)	DBC (W)	Proposed (W)
100%	3.85	3.43	2.68	2.68
75%	2.06	2.15	1.73	1.73
50%	1.53	1.19	1.01	1.01
30%	0.90	0.66	0.59	0.59
20%	0.64	0.47	0.44	0.44
10%	0.42	0.39	0.33	0.33

The power semiconductor device losses distribution for H5, H6, DPB and proposed inverters at 75% of the rated output power condition, which is the most dominant term in CEC efficiency evaluation, is also shown in Figure 4.20. It can be seen that the switching losses for these four MOSFET inverters are almost the same. The conduction losses of H5 are highest because of the IGBT's fixed voltage drop. The conduction losses of the H6 inverter are higher than DBC and the proposed inverters because one more switch is in series in the current path during the active stages. The proposed transformerless inverter can achieve the same high efficiency as the DBCMOSFET inverter. However, the reliability of the proposed converter is

greatly enhanced and the quality of output ac-current is improved compared to the DBC MOSFET inverter.

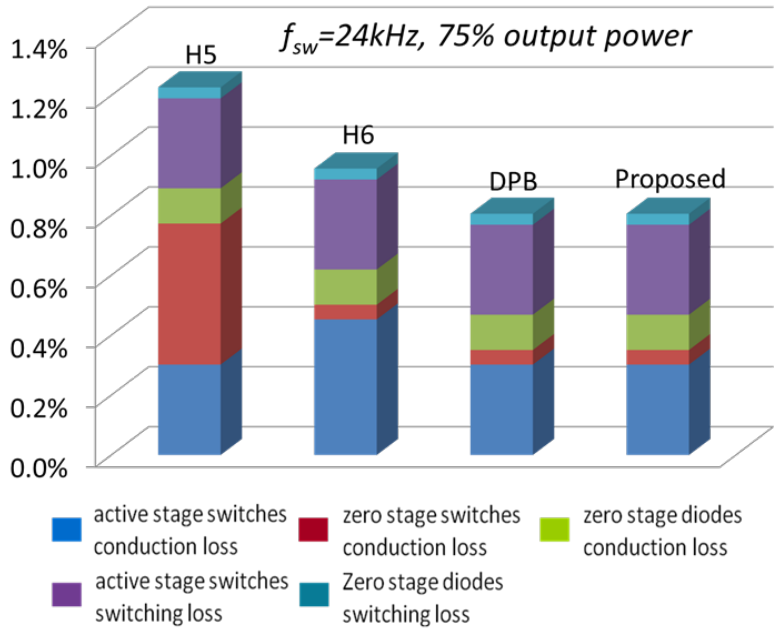


Figure 4.20 Power semicondcutor device losses distribution comparison for H5, H6, DBC and proposed transformerless PV inverters with 75% of the rated output power.

4.5.4 Loss reduction with MOSFETs replacing IGBTs as power switches for the proposed transformerless inverter

In order to highlight the advantages of employing superjunction MOSFETs instead of IGBTs as the main switches to achieve ultrahigh efficiency, the loss reduction with MOSFETs replacing IGBTs as power switches for the proposed transformerless inverter is evaluated in this section.

The turn-on and turn-off switching losses for active-stage IGBTs can be calculated as (4.27) and (4.28) respectively

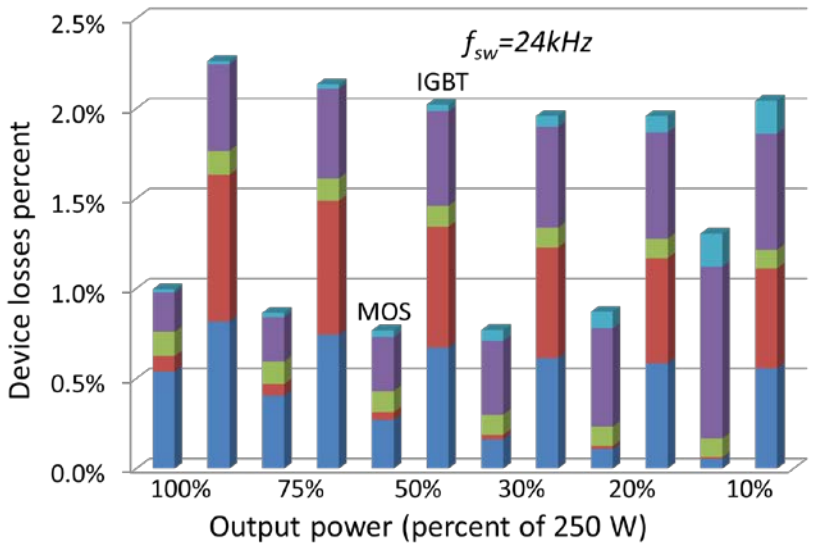
$$P_{sw\_on} = \frac{1}{2\sqrt{\pi}} f_{sw} \alpha_{on} \mathrm{I_m}^{\beta_{on}} k_{g\_on} \frac{V_{dc}}{V_{test}} \frac{\Gamma(\frac{\beta_{on}+1}{2})}{\Gamma(\frac{\beta_{on}}{2}+1)} \tag{4.27}$$

$$P_{sw\_off} = \frac{1}{2\sqrt{\pi}} f_{sw} \alpha_{off} \mathrm{I_m}^{\beta_{off}} k_{g\_off} \frac{V_{dc}}{V_{test}} \frac{\Gamma(\frac{\beta_{off}+1}{2})}{\Gamma(\frac{\beta_{off}}{2}+1)} \tag{4.28}$$

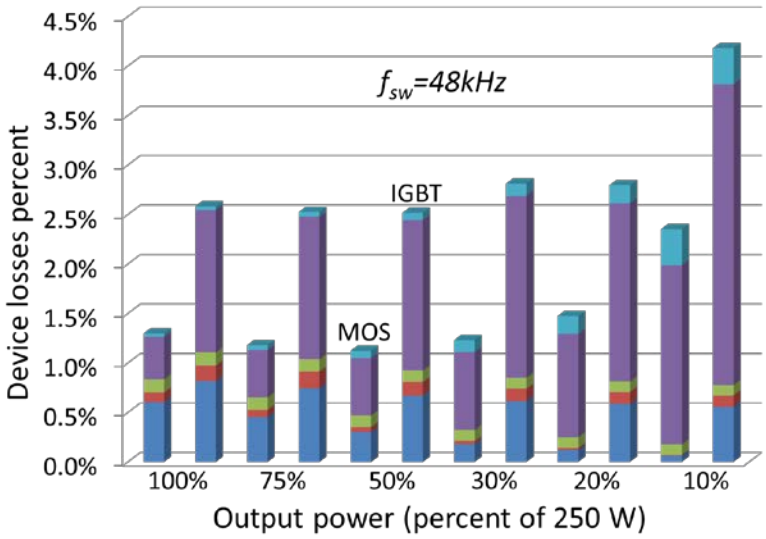
Where $\Gamma(\frac{\beta_{off}+1}{2}) / \Gamma(\frac{\beta_{off}}{2}+1) = \frac{1}{\sqrt{\pi}} \int_0^{\pi} (\sin \omega t)^{\beta_{off}} d\omega t$; k_{g_on} is gate drive stiffness factor during turn-on; k_{g_off} is gate drive stiffness factor during turn-off; α_{on} and β_{on} are turn-on energy coefficients; α_{off} and β_{off} are turn-off energy coefficients; V_{dc} is the actual switched dc bus voltage and V_{test} is test voltage for switching energy coefficients on the IGBT datasheets. α_{on}, β_{on}, α_{off} and β_{off} can be obtained through matlab curve fitting based on the E_{on} and E_{off} of IGBT datasheet.

The power semiconductor device losses distribution for the proposed inverter with MOSFETs and IGBTs at different CEC output power with operating switching frequencies of 24 kHz and 48 kHz are comparatively illustrated in Figure 4.21 (a) and (b) respectively. When IGBTs are employed as power devices, the total power semiconductor device losses of the proposed inverter are already more than 2.4% for all tested power ranges in CEC efficiency calculation at 48 kHz switching frequency. If other losses such as output inductor loss, gate drive loss and control board loss are included, the losses of the whole inverter system will be above 3%. As a result, the efficiency of the whole inverter system is less than 97%, which is relatively low for a transformerless grid-connected PV inverter. On the other hand, for

the MOSFET inverter operating 48 kHz switching frequency, the total power semiconductor device losses are less than 1.2% with the output power higher than 30% of the rated power and no more than 2.4% even at 10% output power. If other losses are included, the CEC and EU efficiencies of the whole inverter can still achieve an efficiency over 98%, which is higher than most of the commercially available transformerless PV inverters. Hence, a higher switching frequency operation can be adopted for the proposed inverter with superjunction MOSFETs to reduce the output current ripple and the size of passive components, while the inverter still maintains an high-level system efficiency.



(a)



(b)

Figure 4.21 Power semiconductor device losses distributaion comparion for the proposed inverter using MOSFETs and IGBTs at different output power: (a) 24 kHz switching frequency, and (b) 48 kHz switching frequency.

4.6 Experimental verification

A 250 W prototype circuit has been designed, fabricated and tested to verify the performance of the proposed transformerless PV inverter topology.

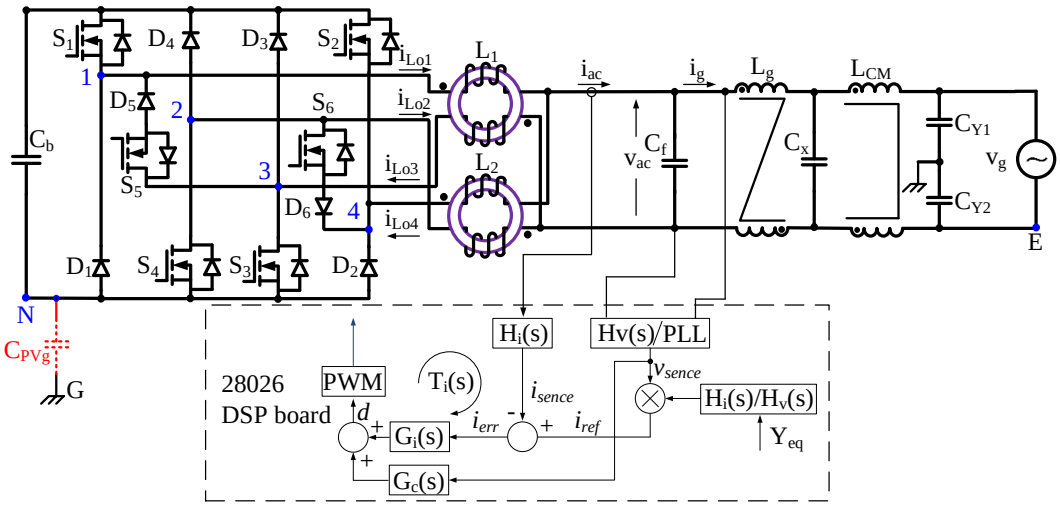


Figure 4.22 Block diagram of the complete inverter test system.

Figure 4.22 describes the block diagram of the complete grid-connected inverter test system. $G_i(s)$ is a quasi-proportional-resonant (QPR) current controller and $G_c(s)$ is a feed-forward term. Specifications of the inverter and the selection of power stage devices are shown in table III. The photograph of the test-bed hardware prototype is shown in Figure 4.23.

Table 4-3 Specifications and power stage devices for prototype circuit

Nominal input voltage	380V
Grid voltage	240Vac
Nominal frequency	60Hz
Nominal output power	250 W
Nominal AC current	1.04 A
S_1~S_6	IPB60R099C6, $R_{ds\ (on),max}$= 99mΩ
D_1~D_6	Silicon Lxa08b600/ SiC
L_1,L_2	5.6mH
C_f	0.44uF
Lg	0.25mH
Cx	0.15uF
Lcm	2.65mH
C_{Y1},C_{Y2}	2.2nF
C_{PVg}	10nF
Digital Controller	Texas Instrument's 28026

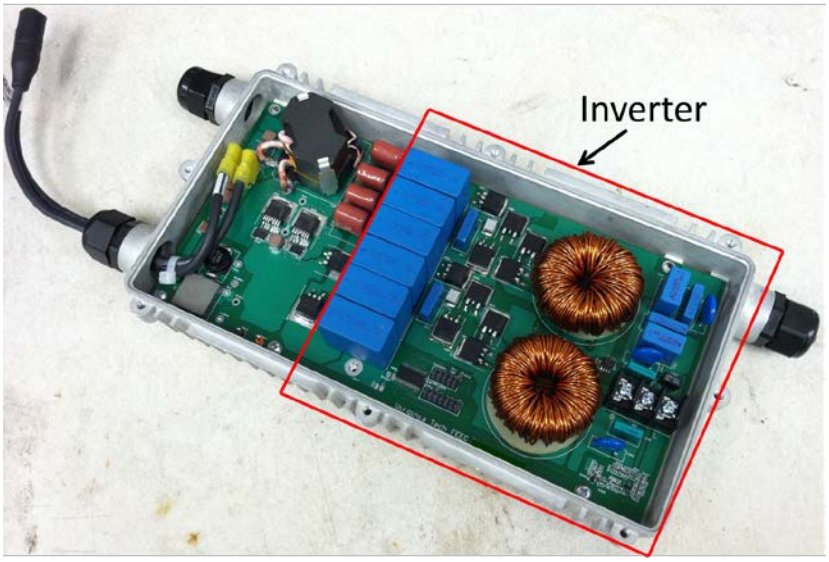
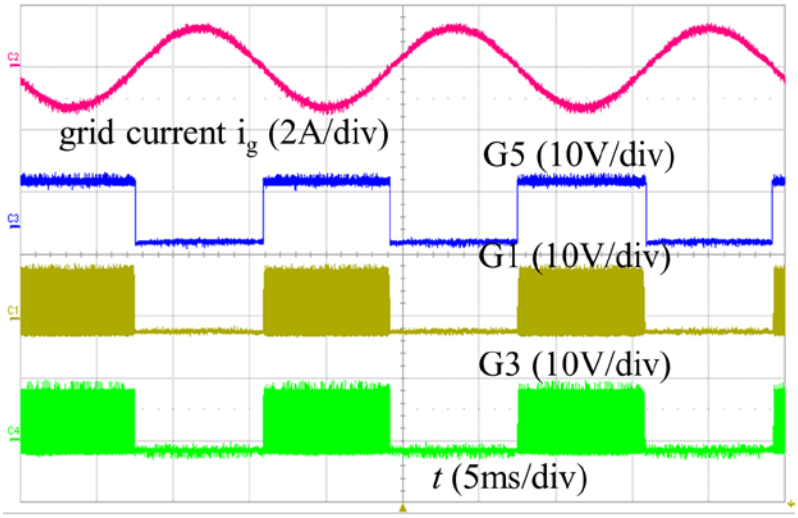
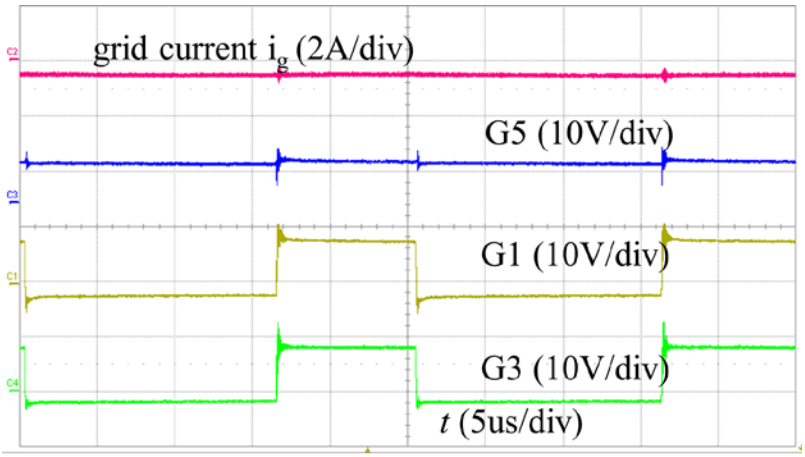


Figure 4.23 Prototype board



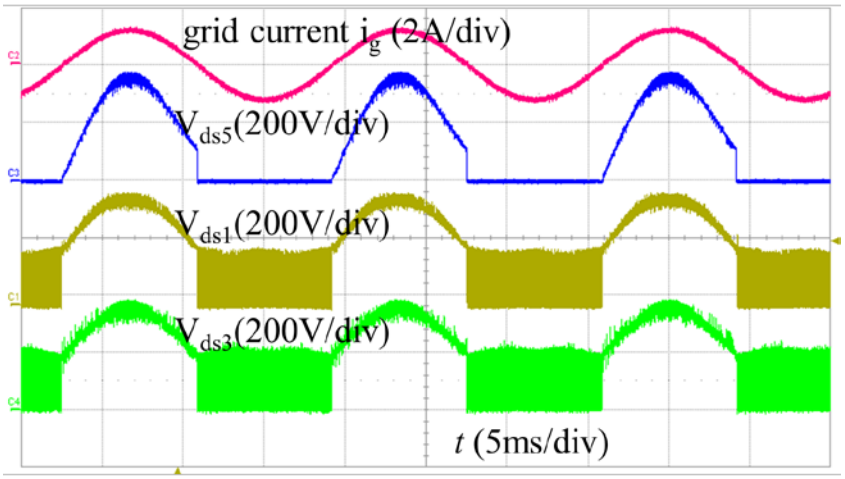
(a)



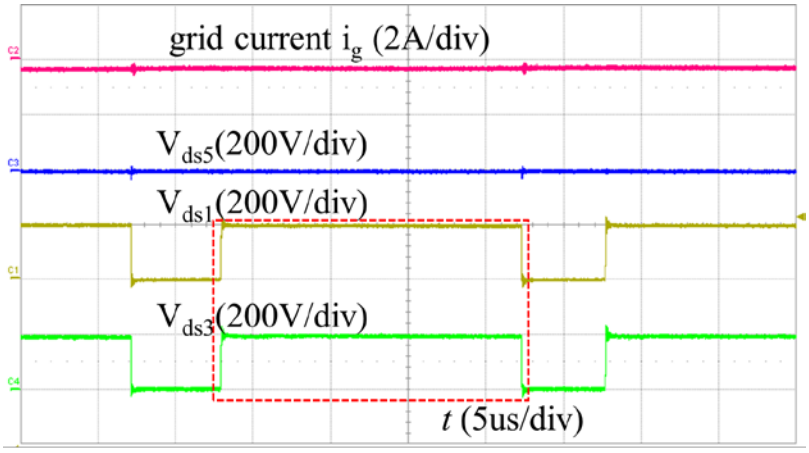
(b)

Figure 4.24 Switch gating signals: (a) in the grid cycle and (b) in the PWM cycle.

The experimental gating signals in the grid cycle and in the PWM cycle are shown in Figure 4.24 (a) and (b) respectively. It can be seen that the experimental gating signals G_1, G_3, and G_5 agree with the analysis results of the PWM scheme and the gating signals of G_1 and G_3 are synchronized well.



(a)



(b)

Figure 4.25 Drain-source voltage waveforms of the switches S_1, S_3 and S_5: (a) in the grid cycle, and (b) in the PWM cycle.

The drain-source voltage waveforms of the switches S_1, S_3 and S_5 in the grid cycle and in the PWM cycle are shown in Figure 4.25 (a) and (b) respectively. The voltage stresses of S_1, S_3 and S_5 are well clamped to the dc bus voltage, 380 V, without any voltage overstress. It can be seen from Figure 4.25 (b) that the switches S_1 and S_3 almost evenly share the dc-link voltage when they switch OFF simultaneously, effectively minimizing the ground loop leakage current.

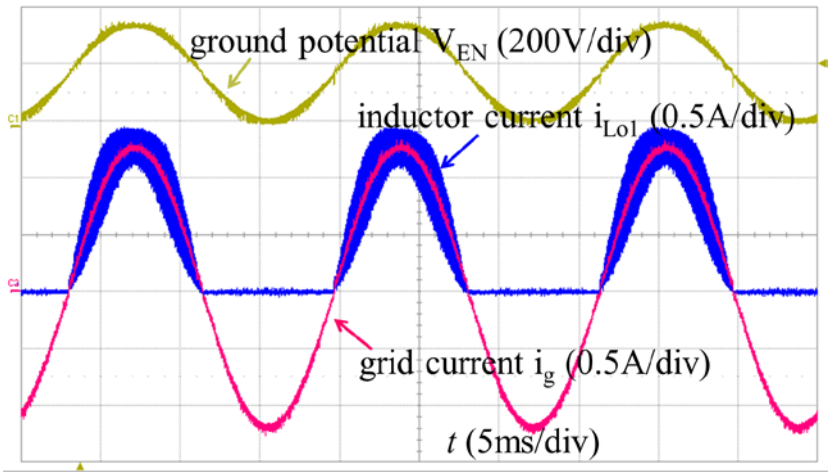


Figure 4.26 Experimental waveforms of ground potential V_{EN}, grid current and current of inductor L_{o1}

Figure 4.26 shows the experimental waveforms of the ground potential V_{EN}. It can be seen that the high ground leakage current is avoided because the high-frequency voltage of the ground potential is eliminated at every PWM switching commutation and at zero-crossing instants.

The experimental waveforms of the grid current i_g, the inductor currents i_{Lo1} and i_{Lo2} under the 240 V_{rms} grid voltage and half-load conditions are shown in Figure 4.27. This figure shows that the proposed inverter presents high power factor and low harmonic distortion.

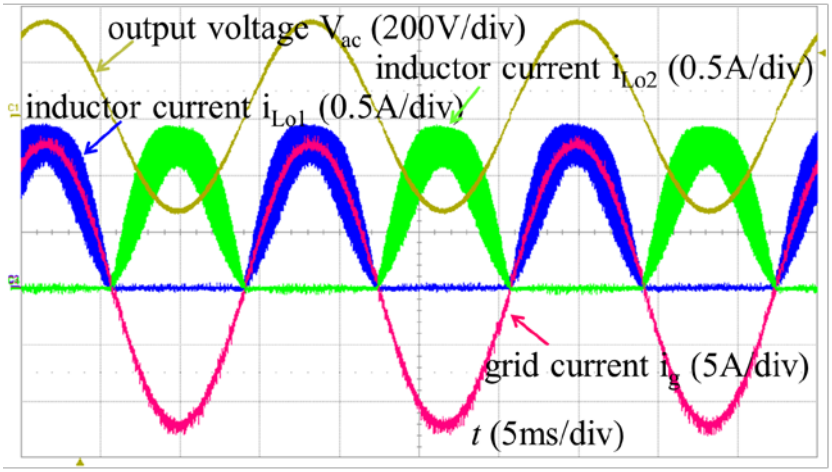


Figure 4.27 The experimental waveforms of grid current and the inductor currents i_{Lo1} and i_{Lo2}

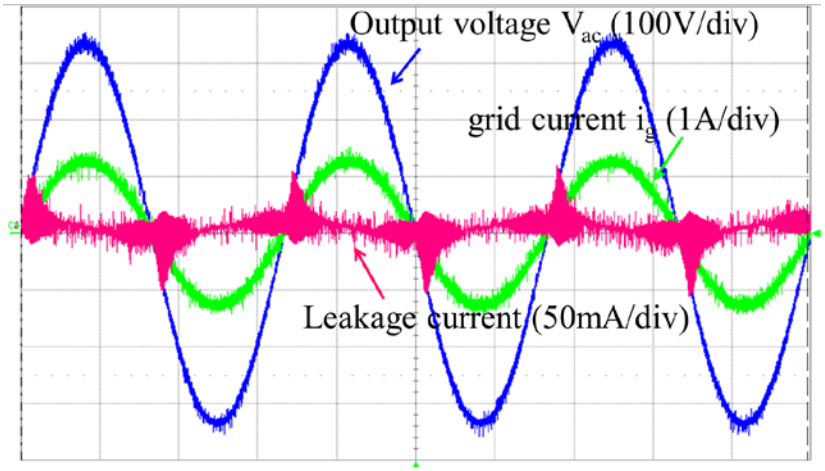


Figure 4.28 Leakage current test waveforms

Figure 4.28 shows the leakage current test waveforms, the common-mode leakage current is successfully limited with the peak value 59.5mA and rms value 10.33mA, which are well below the limitation requirements of the German standard, VDE0126-1-1 [D33].

Figure 4.29 shows the measured efficiencies as a function of the output power for the proposed transformerless PV inverter with silicon ultrafast and

SiC Shottky diodes respectively at switching frequency of 24 kHz. Note that the presented efficiency diagram covers the losses of the main power stage including power semiconductor device losses and output inductor losses, but it does not include the power consumption of control circuit and the associated driver circuit. The maximum experimental efficiency of the prototype circuit is 99.1% and 98.9% with SiC diode and ultrafast respectively.

The calculated CEC efficiencies of the proposed transformerless inverter with SiC diode and ultrafast diode are 98.6% and 98.4% respectively. The CEC efficiency with SiC diodes is about 0.2% higher than that with silicon diodes, however at the penalty a slightly high cost.

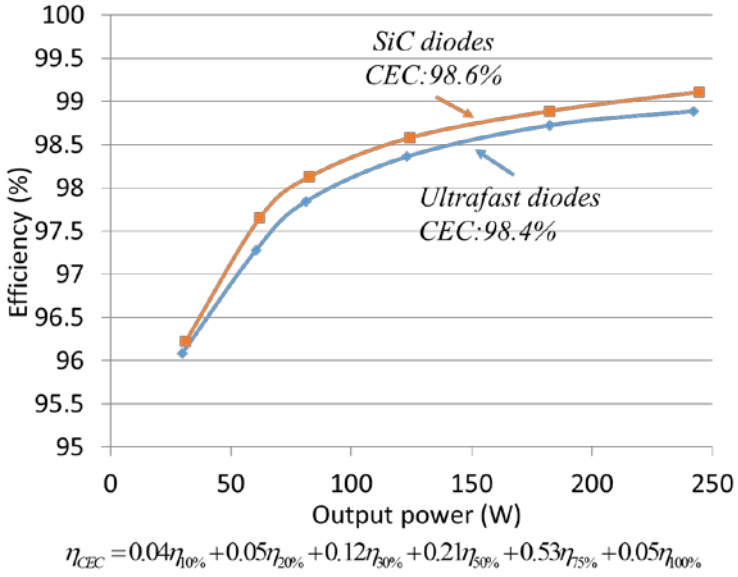


Figure 4.29 Measured efficiency as a function of the output power with ultrafast and SiC diodes respectively at the switching frequency 24 kHz

4.7 Summary

The second stage of SPTS microinverter requires a high efficiency single-phase grid-tie inverter. In order to use the unipolar PWM to improve the efficiency while still maintaining low EMI and leakage current, quite a few tranformerless inverter topologies have been proposed and patented. Transformerless inverters can achieve ultrahigh efficiency by using fast superjunction MOFET devices and non-reverse-recovery SiC diodes even at hard-switching conditions. In order to avoid the slow reverse-recovery of body diode of MOSFETs, a new high efficiency, high reliability split-phase transformerless inverter topology with following advantages was presented:

- Ultra high efficiency can be achieved over a wide output power range by reliably employing superjunction MOSFETs for all switches since their body diodes are never activated.
- No shoot-through issue leads to greatly enhanced reliability.
- Low ac output current distortion is achieved because dead time is not needed at PWM switching commutation instants and grid-cycle zero-crossing instants.
- Low ground loop CM leakage current is present as a result of two additional unidirectional-current switches decoupling the PV array from the grid during the zero stages.

- Higher switching frequency operation is allowed to reduce the output current ripple and the size of passive components while the inverter still maintains high efficiency.
- The higher operating frequencies with high efficiency enables reduced cooling requirements and results in system cost savings by shrinking passive components.

The experimental results tested on a 250 W hardware prototype verify the effectiveness of the proposed converter and show 98.6% CEC efficiency. With the ultrahigh efficiency, low leakage ground loop CM current, high quality of output current and greatly enhanced reliability, the proposed topology is very attractive for microinverter and transformerless PV inverter applications.

Chapter 5 Modeling and Control of Single-Phase Two-Stage Electrolyte-Free Microinverters

5.1 Energy storage capacitors in SPTS microinverters

As shown in Figure 5.1, the energy storage capacitors for double line frequency ripple buffering could be placed at PV side, as C_{pv} or DC bus side as C_b. However the PV side voltage V_{pv} is normally from 20 V to 45 V, which is much lower than the DC bus voltage V_b, which is normally 380 V to 400 V for 240 V_{ac} AC grid system. In order to achieve same low-frequency ripple buffer effect, the capacitance requirements of C_{pv} is about V_b^2/V_{pv}^2, i.e. about 160 times higher than that of C_b. In addition, reducing C_{pv} can improve the dynamic performance of MPPT. So the optimal solution is using C_b as low-frequency energy buffer and C_{pv} only for high-frequency dc-dc switching frequency reduction.

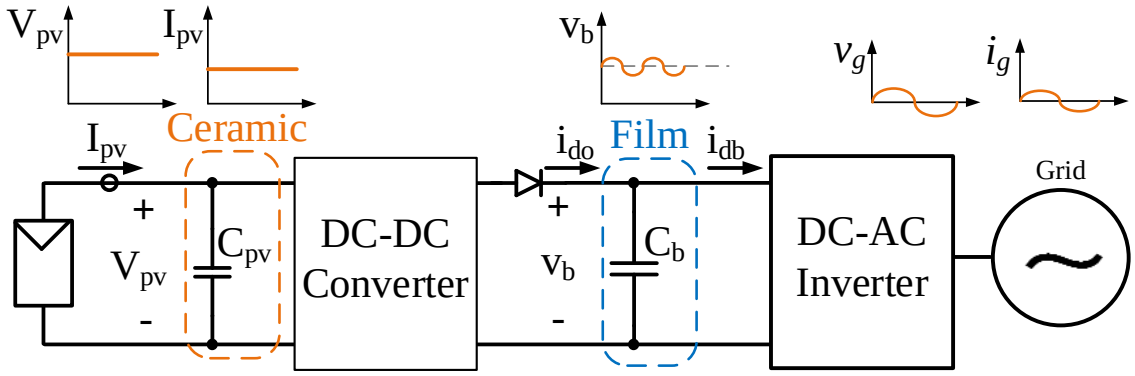


Figure 5.1 Energy storage capacitors in SPTS microinverters

The capacitance requirement for C_b can be expressed as

$$C = \frac{P}{2\pi f V^2 \alpha\%} \tag{5.1}$$

where P is the average output power, f is the fundamental grid frequency, V is the average capacitor voltage, and α% is the allowed peak-to-peak capacitor voltage ripple percent with respect to average capacitor voltage. The equation shows that if the allowed ripple percent is fixed, the capacitance could be reduced by operating with high average capacitor voltage. The high voltage intermediate dc bus in SPTS microinverters provides the opportunity to reduce the energy storage capacitance so that film capacitor with long lifetime can be used. Although film capacitors have far more lifetime than electrolytic capacitors, the energy density of film capacitors are much lower compared to electrolytic counterparts. In order to reduce the size and cost of the electrolyte-free microinverters, according to equation (5.1), the allowed voltage ripple percent α% should be high so that the required numbers of film capacitors can be reduced. However, the high ripple voltage on the dc bus may lead to two issues. One issue is the MPPT performance degradation due to the penetration of double line voltage ripple back to the PV modules and another issue is the grid current distortion due to the distorted sinusoidal current reference from the dc bus voltage loop. This section will give a control technique to address these two issues. The dc bus in the prototype microinverter uses small-capacitance film capacitors, which allows to have high ripple voltage to buffer the double line ripple energy. The presented method controls the PV dc-dc converter with a high loop gain at double line frequency to reject the PV-side double line oscillation and control

intermediate dc-bus voltage loop with a low loop gain at the double line frequency to reduce the grid-side current distortion. The PV-side capacitance in the prototype microinverter can also be greatly reduced because it is only required to filter the high-frequency switching ripple. The design considerations and procedures will be given. The effectiveness of the presented method is experimentally justified using a 250 W microinverter prototype.

5.2 Effects of double line ripple in SPTS microinverters

The propagation of double line frequency back to PV module will cause MPPT efficiency degradation. If it goes into the grid current reference, the grid current will be distorted. The detailed effects and the causes of the effects will be discussed.

5.2.1 Effect of double line ripple on MPPT performance

In a SPTS microinverters, the dc-dc converter accomplishes maximum power point tracking (MPPT). This guarantees that the PV module is operated at the MPP, which is the operating condition where the most energy is captured. The presence of low-frequency fluctuation of the ripple voltage at PV module terminal causes two drawbacks. The first one, as shown in figure 5.2, is the more or less significant sweep at the double frequency of the operating point of the PV module voltage around the true MPP will lead to the waste of available energy [B1], [E1]. The second drawback is that the MPPT controller based on the perturb and observe (P&O) method, can be

confused, and once more, the efficiency of the system can be severely be compromised.

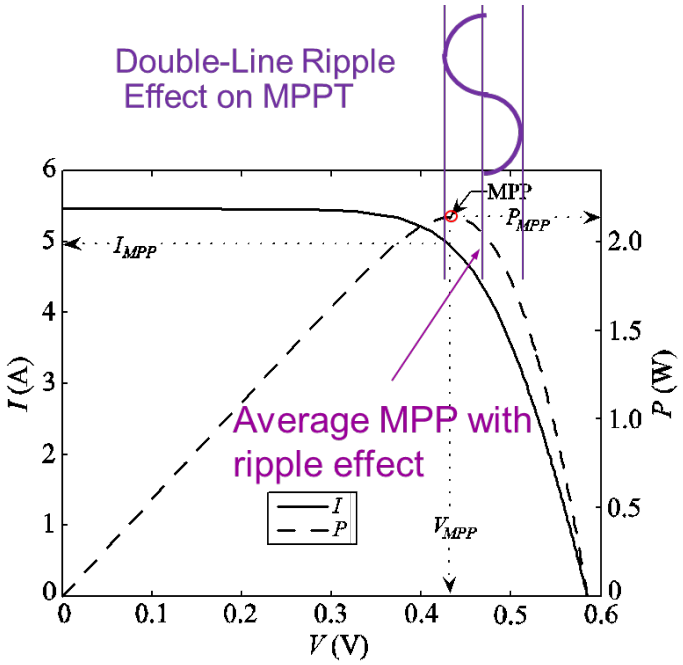


Figure 5.2 MPPT performance suffering from the double line ripple fluctuation of PV module terminal voltage.

Single-stage microinverter required electrolytic capacitor bank at the PV-side to buffer the double line ripple. In order to evaluate the MPPT efficiency degradation due to the double line ripple propagation back to the PV module caused by the dry-out of electrolytic capacitors. One commercial microinverter model M190-72-240 with rated power 175 W from Enphase as shown in Figure 5.3 was studies to evaluate the MPPT efficiency. Originally, the inverter has five 1.8 mF electrolytic capacitors with the total capacitance 9.0 mF. As shown in Figure 5.3, the original MPPT efficiency can be high up to 99.8%. If the capacitance was reduced to 3.6 mF due to the dry-out, the

MPPT efficiency would reduce to 98.7%. When the capacitance was further reduced to 1.8 mF, the MPPT efficiency would drop to 94.7%. The simulations was performed to study the MPPT efficiency degradation caused by the reason of the double line voltage sweeps only. If the efficiency drop caused by the MPPT algorithm confusion due to the double line ripple was also considered, the efficiency drop would be much worse.

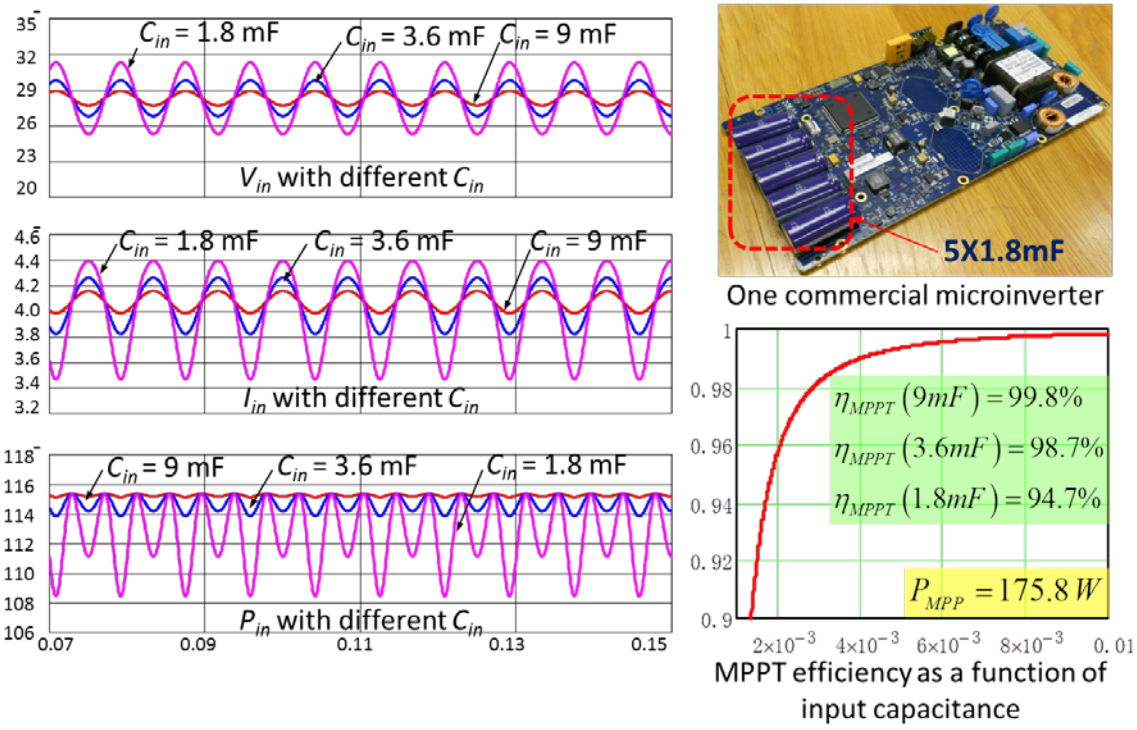
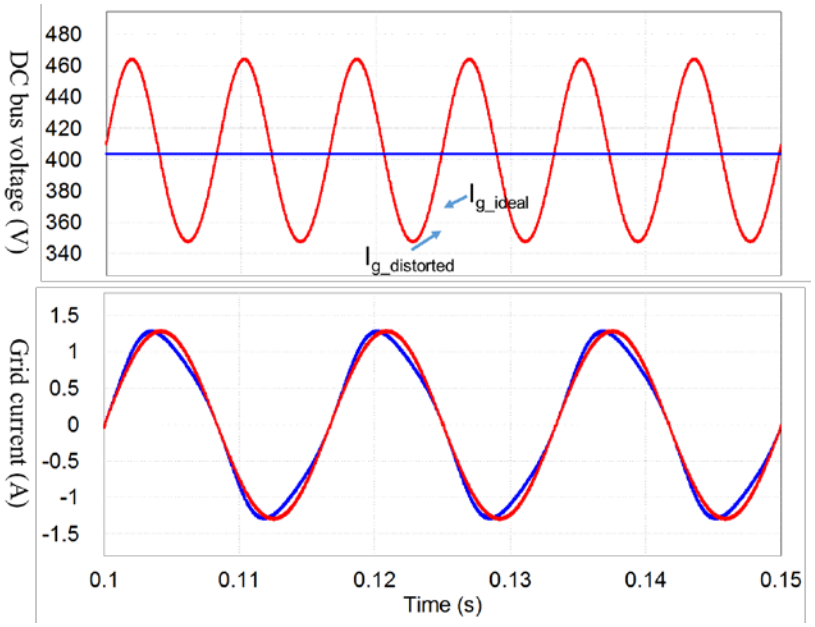


Figure 5.3 MPPT efficiency degradation analysis from the double line ripple current propagation back to PV module caused by the dry-out of electrolytic capacitors.

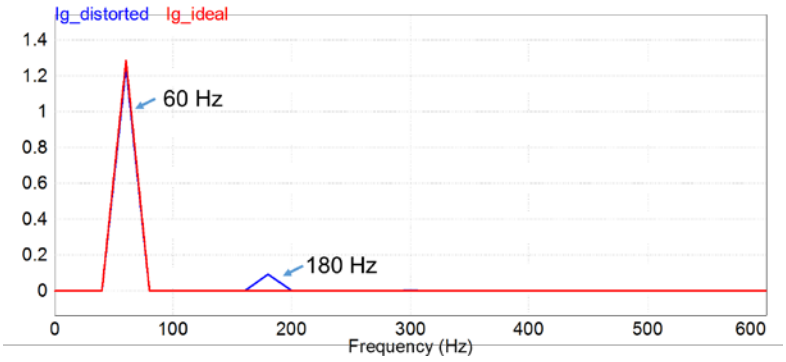
5.2.2 Effect of double line ripple on grid current distortion

As shown in Figure 5.4, the double line ripple on the DC bus voltage will cause grid current distortion. After making a fast Fourier analysis (FFT), it is

found that the double line ripple on the DC bus voltage will produce the third harmonic of the line frequency in the grid current.



(a)



(b)

Figure 5.4 Simulation results showing the double line ripple effect on the grid current (a) time domain, (b) FFT analysis of grid current.

5.3 System control architecture of the electrolyte-free microinverter

The digital control structure for the SPTS electrolyte-free microinverter using presented technique is shown in Figure 5.5, where the first stage is a hybrid transformer dc-dc converter and second stage is a full bridge dc-ac grid-tie inverter.

Essentially, two sub-system controls are included in the system. One is dc-dc converter control, which implements MPPT of the PV module as well as rejects the propagation of double line ripple back into the PV module. Another control is grid-tie inverter control, which regulates the dc bus voltage as well as controls the current injected into the grid. The dc-dc converter implements P&O MPPT control based on the sensed PV module voltage v_{pv_sense} and current i_{pv_sense}. The output of MPPT controller provides a reference V_{pv}^* to the inner voltage loop of dc-dc converter. This inner voltage loop is used for double line ripple rejection. $G_{c\_pv}(s)$ is dc-dc voltage loop controller, which generates a duty d_{dc} to the dc-dc converter. $G_{c\_b}(s)$ regulates the dc bus voltage based the difference of the dc bus voltage reference V_b^* and the sensed dc bus voltage v_{b_sense}. The output of $G_{c\_b}(s)$ provides a current reference i_{con}, which multiplies the PLL output $\sin\omega t$ to give a grid current reference i_{ac}^*. V_{m_cal} is used for calculating the magnitude of the grid voltage. $G_{c\_i}(s)$ is the ac current controller. The sum of the output of $G_{c\_i}(s)$ and the feed-forward term v_{ff} generates a duty d_{ac} for grid-tie inverter. $H_{ipv}(s)$ and $H_{vpv}(s)$ are sense gains of the PV current and voltage sense circuits. $H_{vb}(s)$ is

the dc bus voltage sense gain. $H_{iac}(s)$ and $H_{vac}(s)$ is the ac side current and voltage sense gain respectively. The output filter is grid-tie inverter is an LCL filter, which is composed of L_i, L_s and C_f and damping resistor R_d. C_b is the film dc capacitors and C_{pv} is the PV-side ceramic capacitors. As we can see, no electrolytic capacitors are used in the system. The whole system control is implemented by a single microcontroller TMS28026 from Texas Instruments. The controllers which need to be designed include the $G_{c\_pv}(s)$, $G_{c\_i}(s)$, $C_{c\_b}(s)$. All these controllers as well as the PLL and V_{m_cal} will be implemented in digital domain. In order design these controller, the power stage model must be derived first.

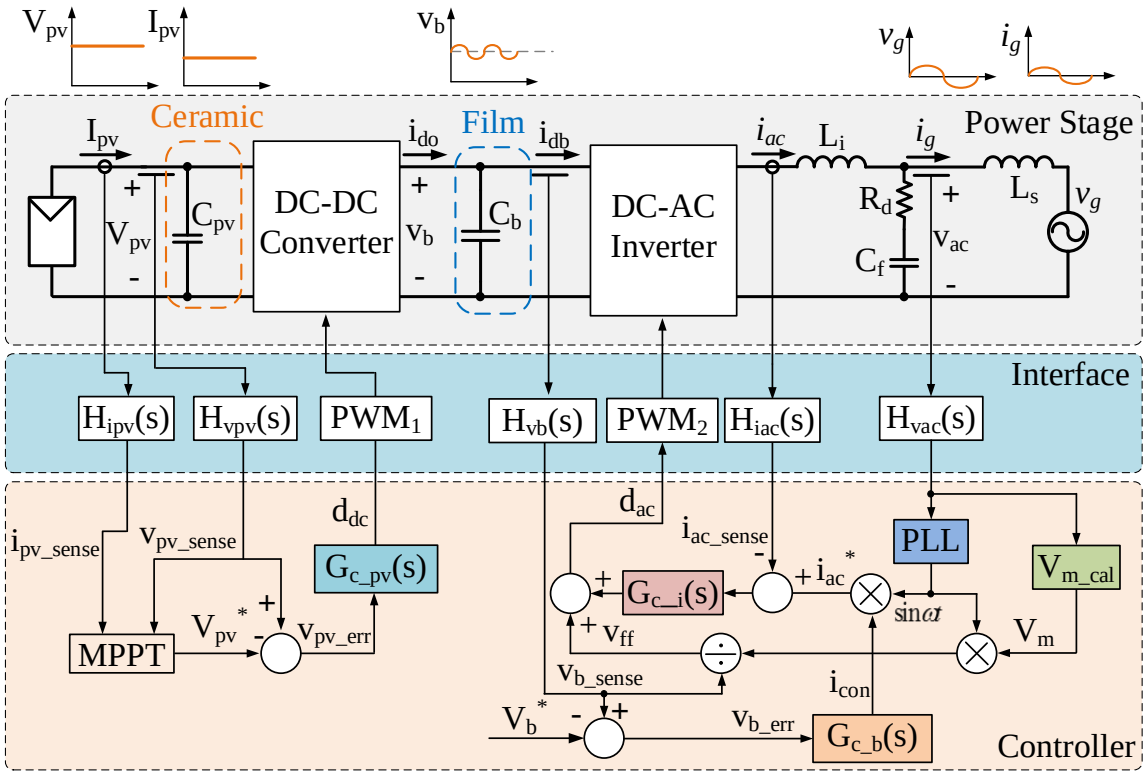


Figure 5.5 System control structure

5.4 Modeling and control of hybrid transformer dc-dc converters with double line ripple rejection

This section derives the small-signal model of the hybrid transformer dc-dc converter. Then based on the derived small-signal mode, $G_{c\_pv}(s)$ is designed to regulator the PV voltage as well as rejects the propagation of double line ripple back into PV module.

In hybrid transformer dc-dc converters, the minor resonant loop composed of the leakage inductor and an external small resonant capacitor has the resonant frequency close to the switching frequency. Although the resonant operation is incorporated, this type of converters still could use traditional fixed-frequency PWM control to alter the boost gain to accommodate the wide changing PV module voltage, which greatly simplifies the control. Due to the resonant capacitor transferring energy in the loop, this type of converters has increased boost gain, optimized magnetic utilization, low device stresses and high efficiency over wide input voltage ranges, which are very attractive for PV module applications. Unfortunately, not like traditional PWM converter, there are more than two topological states within one switching cycle in this type of converters. Although advanced modeling techniques like extended describing function method [E8] may be utilized to accurately model this type of converters. However it is too complex to guide the real practical engineering design. Instead of using complex advanced modeling methods, in this section, traditional simple state-space averaging modeling method [F15]

is used to model the hybrid transformer dc-dc converter by selecting two dominant energy transfer topological states among all the total states within one switching period.

A voltage control loop with high bandwidth inside the MPPT loop can be employed to reject the double line voltage oscillation [E2], [E4]. The rejection capability of the double-line oscillation is dependent on the bandwidth of the voltage control loop, the higher the bandwidth, the higher the rejection capability. A high bandwidth with 10 kHz is achieved by using a wide-bandwidth analog control circuitry in [E2] and a bandwidth with 7.15 kHz in [E4] is achieved by using a dedicated dc-dc FPGA control chip. These implementations increased the complexity of the control board and the cost of the system. Also, this method requires the high fidelity of the converter model. However, in PV module applications, using a single low-cost microcontroller to control the front-end dc-dc converter and the following-stage dc-ac inverter is desirable, because it can save the cost and reduce the system complexity. For a single microcontroller, the sampling frequency is limited due to the low switching frequency (normally about 20 kHz) of inverters and the computation time requirement. So it is hard to design a system bandwidth high enough to provide high rejection capability of double-line ripple. As we discussed above, the state-space averaging modeling method is approximately utilized in the high boost ratio converter we employed, so the model discrepancy between the modeled and the actual

plants at high frequencies caused by the modeling approximation and circuit parasitic uncertainties prevents us from designing a system practically with very high bandwidth.

This section presents a new voltage controller, which cascades proportional-integral (PI) controller and quasi-resonant (QR) controller to regulate the input PV voltage and provides high double line voltage rejection. The introduction of QR controller provides significant double line voltage reduction of PV module while it has negligible impact on the phase and gain margins of the voltage loop gain. Traditional loop gain design method can be used to design the PI controller, while the double line voltage rejection boost from the QR controller can be easily designed by modifying its quality (Q) value. The dependence of the double-line rejection capability on the accuracy of the plant model at high frequencies is greatly reduced compared to high voltage loop bandwidth method in [E2],[E4]. As a result, the approximated model can be effectively utilized to assist the design of the voltage controller. The dc-dc converter and inverter can be controlled with a single low-cost microcontroller with a low sampling frequency (12 kHz in our application) without using additional circuitry. Simulation and experimental results justify the proposed method is a simple and effective way to reject the double line voltage oscillations of PV module without additional cost and complexity penalties.

5.4.1 Small-signal modeling of PV modules

The relation between the terminal current and voltage of PV module is rewritten as following:

$$i_{pv} = i_{ph} - i_D - i_p = i_{ph} - I_o(e^{\frac{v_{pv}+i_{pv}R_s}{AV_t}} - 1) - \frac{v_{pv}+i_{pv}R_s}{R_p} \tag{5.2}$$

where i_{ph} depends on the irradiance of S and on the array temperature T, I_o and V_t depend on T only. Under normal condition, the oscillations of the operation point (v_{pv}, i_{pv}) are small compared to the MPP (V_{MPP}, I_{MPP}), so the relationship among i_{pv}, v_{pv}, S and T can be linearized around MPP as

$$\hat{i}_{pv} = \left.\frac{\partial i_{pv}}{\partial v_{pv}}\right|_{MPP} \hat{v}_{pv} + \left.\frac{\partial i_{pv}}{\partial S}\right|_{MPP} \hat{S} + \left.\frac{\partial i_{pv}}{\partial T}\right|_{MPP} \hat{T} \tag{5.3}$$

where symbols with hats represent small-signal variations around the steady-state values of the corresponding quantities. Due to the facts that the irradiance level and the thermal dynamics of PV module have relatively higher inertia compared to the electrical dynamics of PV module, when we consider designing the controller for power stages of hybrid transformer dc-dc converter, the perturbances of $\hat{S}$ and $\hat{T}$ could be reasonably assumed to be zero. As a result, equation (5.3) can be simplified as

$$\hat{i}_{pv} = \left.\frac{\partial i_{pv}}{\partial v_{pv}}\right|_{MPP} \hat{v}_{pv} \tag{5.4}$$

From (5.2), we can get

$$\left.\frac{\partial i_{pv}}{\partial v_{pv}}\right|_{MPP} = \frac{\hat{i}_{pv}}{\hat{v}_{pv}} = -[R_s + \frac{1}{\frac{I_o}{AV_t}\cdot e^{\frac{V_{MPP}+I_{MPP}R_s}{AV_T}} + \frac{1}{R_p}}]^{-1} = -\frac{1}{R_{MPP}} \tag{5.5}$$

(5.5) indicates that the small-signal electrical model of PV module is equivalent as a simple negative resistor [E2], as shown in Figure 5.6, which is similar to a constant power source.

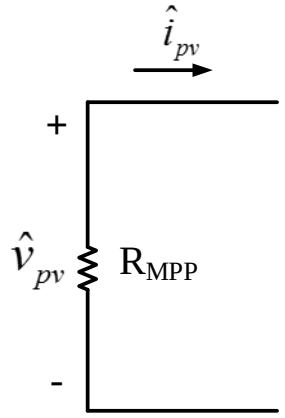


Figure 5.6 Electrical small-signal model of PV module

In the neighborhood of the MPP we have

$$P_{MPP} + \hat{P} = (V_{MPP} + \hat{v}_{pv})(I_{MPP} + \hat{i}_{pv}) = V_{MPP}I_{MPP} + V_{MPP}\hat{i}_{pv} + \hat{v}_{pv}I_{MPP} + \hat{v}_{pv}\hat{v}_{pv} \tag{5.6}$$

(5.6) can be decomposed as,

$$P_{MPP} = V_{MPP}I_{MPP} \tag{5.7}$$

$$\hat{P} = V_{MPP}\hat{i}_{pv} + \hat{v}_{pv}I_{MPP} + \hat{v}_{pv}\hat{i}_{pv} = -\frac{\hat{v}_{pv}^{\,2}}{R_{MPP}} \tag{5.8}$$

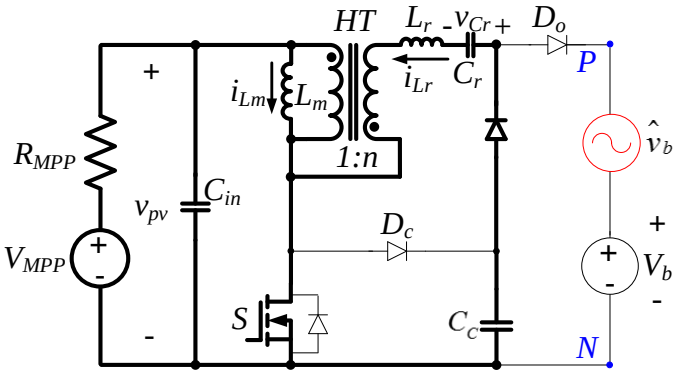
5.4.2 Small-signal model of power stage of hybrid transformer dc-dc converter

Due to minor resonant loop in the energy transfer loop of hybrid transformer dc-dc converter, there are totally five topological states within one switching cycle, as shown in Figure 2.13. However, two topological states

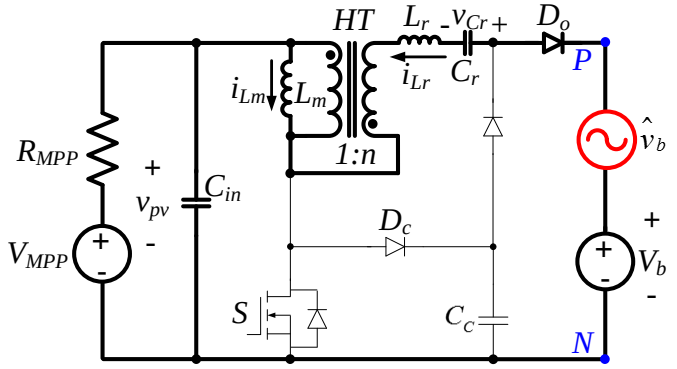
are dominant among these two five states. One is when S is on, the energy is stored in the magnetizing inductor L_m and resonant capacitor C_r simultaneously, as shown in Figure 5.7 (a). Another state is when S is off, the energy from the PV source and stored in the L_m and C_r are transferred to the output together, as shown in Figure 5.7 (b). The state equations representing these two dominant two states are as following,

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = v_{pv} \\ L_r \dfrac{di_{Lr}}{dt} = -n \cdot v_{pv} - v_{Cr} + V_{Cc} \\ C_{in} \dfrac{dv_{pv}}{dt} = \dfrac{V_{MPP} - v_{pv}}{R_{MPP}} - (i_{Lm} + n \cdot i_{Lr}) \\ C_r \dfrac{dv_{Cr}}{dt} = i_{Lr} \end{cases} \quad \text{(S ON, } d\text{)} \tag{5.9}$$

$$\begin{cases} L_m \dfrac{di_{Lm}}{dt} = (v_{pv} + v_{Cr} - v_b) \dfrac{1}{n+1} \\ L_r \dfrac{di_{Lr}}{dt} \cong 0 \\ C_{in} \dfrac{dv_{pv}}{dt} = \dfrac{V_{MPP} - v_{pv}}{R_{MPP}} - \dfrac{i_{Lm}}{n+1} \\ C_r \dfrac{dv_{Cr}}{dt} = -\dfrac{i_{Lm}}{n+1} \end{cases} \quad \text{(S OFF, } 1\text{-}d\text{)} \tag{5.10}$$



(a)



(b)

Figure 5.7 State-space averaging using dominating states: (a) S on, (b) S off.

Averaging state space equations (5.9) and (5.10) using duty *d*, then applying perturbation and linearization, we obtain the small-signal transfer function from duty to the PV voltage as

$$G_{vd}(s)=\frac{\hat{v}_{pv}}{\hat{d}}= \frac{1}{n}\frac{V_b+(n^3C_rL_m-n^2C_rL_mV_b+C_rL_rV_b)}{(C_{pv}C_rL_mL_rs^4+\frac{C_rL_mL_r}{R_{mpp}}s^3+((C_{pv}+n^2C_r)L_m+L_rC_rD'(1+D)+n^2C_rL_mD^2)S^2 +(D^3+D'^3+3DD'^2+3D^2D')\frac{L_m}{R_{mpp}}s+(D^4+D'^4+4DD'^3+4D^3D'+6D^2D'^2))} \approx \frac{V_b}{n}\frac{1}{1+\frac{s}{Q\omega_o}+\frac{s^2}{\omega_o^2}} \tag{5.11}$$

where D is the steady-state duty ratio for S_1, D'=1-D. V_b is the steady-state average voltage of DC bus $\omega_o = \frac{1}{\sqrt{(C_{in} + n^2 C_r)(L_m + \frac{L_r}{n^2})}}$ and $Q = \frac{1}{\omega_o} \frac{R_{MPP}}{L_m + \frac{L_r}{n^2}}$.

The bode plots for $G_{vd}(s)$ are shown in Figure 5.8 with simulation result and mathematical modeling compared. The comparison indicates that the accuracy of the modeling can be accurate up to about 20 kHz, which is enough for following digital controller design with sampling frequency 12 kHz. This will be elaborated in the following section.

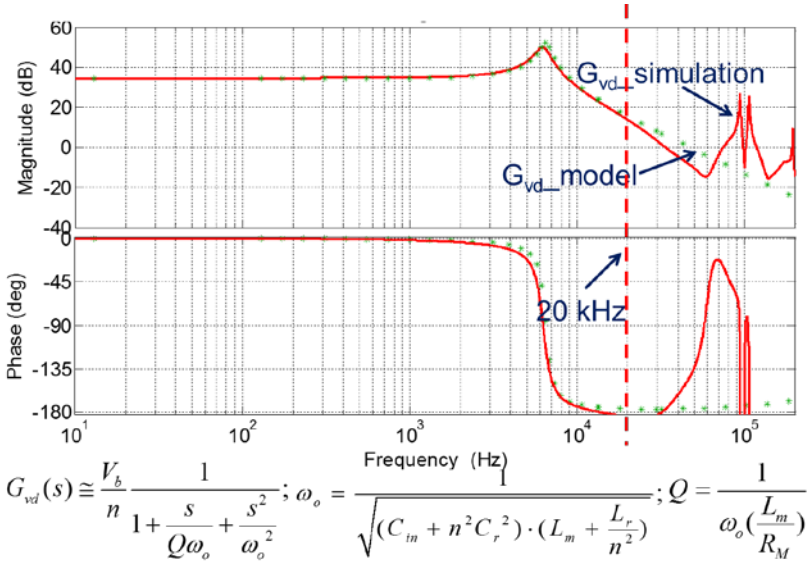


Figure 5.8 Bode plots for transfer function $G_{vd}(s)$: the red one is from simulation using Simplis software and the green one is from mathematical modeling.

5.4.3 Transfer function block diagram

Figure 5.9 and Figure 5.10 show the control block diagram and the transfer function block diagram of the hybrid transformer dc-dc converter.

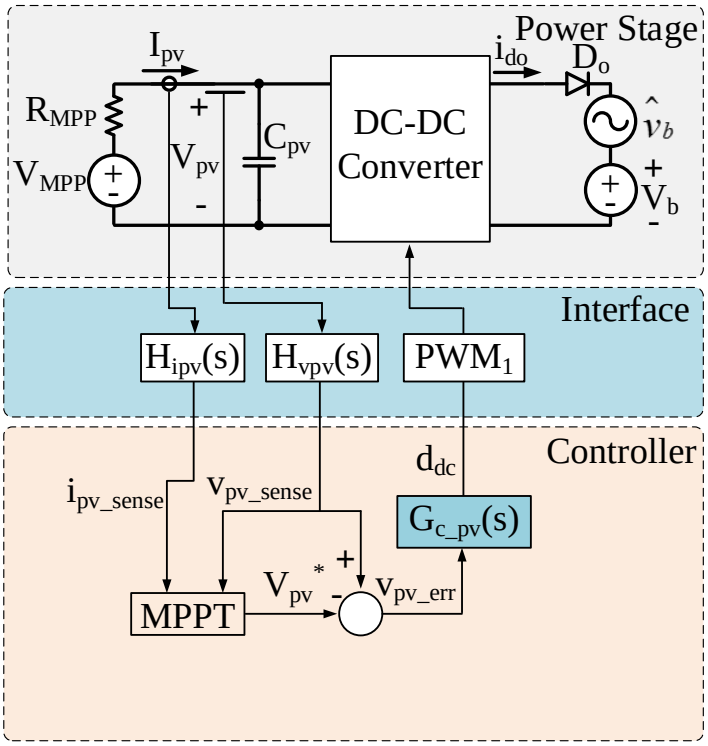


Figure 5.9 Control block diagram of the dc-dc converter

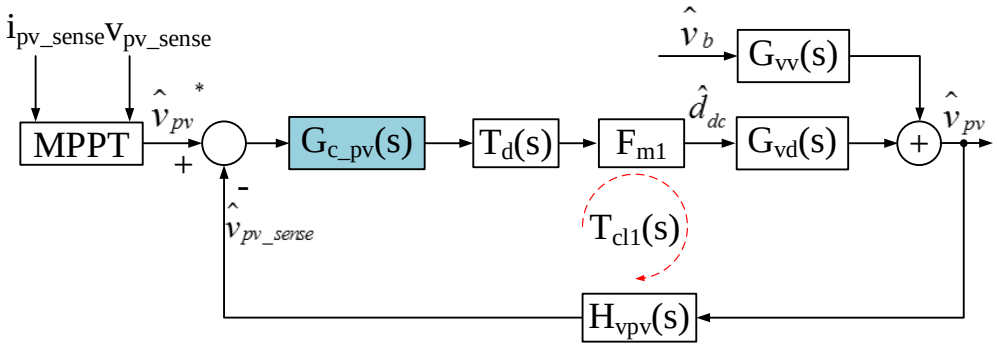


Figure 5.10 Transfer function block diagram of the dc-dc converter

where $G_{vv}(s)$ is the transfer function from dc bus voltage to PV voltage, which is expressed as

$$G_{vv}(s) = \frac{\hat{v}_{pv}}{\hat{v}_b} \cong \frac{D}{n} \frac{1}{1 + \frac{s}{Q\omega_o} + \frac{s^2}{\omega_o^2}} \tag{5.12}$$

where D is the steady state duty cycle of the dc-dc converter. $G_{c\_pv}(s)$ is the PV voltage controller, which needs to be designed. $T_d(s)$ is the digital PWM and control calculation delay of MCU, which is express as

$$T_d(s) = e^{-s\frac{3T_s}{2}} \cong \frac{1 - s\frac{3T_s}{4}}{1 + s\frac{3T_s}{4}} \tag{5.13}$$

where T_s is the sampling period. F_{m1} is dc-dc converter modulator gain, which is expresses as

$$F_{m1} = \frac{1}{PWM_{Period}} \tag{5.14}$$

$H_{vpv}(s)$ is PV voltage sensing network and DSP software scaling gain, which can be approximated as

$$H_{vpv}(s) \cong \frac{1}{1 + + \frac{s}{\omega_{vpv} Q_{vpv}} + \frac{s^2}{\omega_{vpv}^{\ 2}}} \tag{5.15}$$

where ω_{vpv} is the second-order angular cut-off frequency of the voltage sensor circuitry and Q_{vpv} is the corresponding quality factor.

5.4.4 Design of PV voltage loop contorller with high double line rejection capability

This section presents a new controller which has following structure

$$G_{c\_pv}(s) = G_{PI}(s) \cdot G_{QR}(s) = (K_p + \frac{K_i}{s})(\frac{1 + \frac{s}{Q_{oz}\omega_{oz}} + \frac{s^2}{\omega_{oz}^{\ 2}}}{1 + \frac{s}{Q_{op}\omega_{op}} + \frac{s^2}{\omega_{op}^{\ 2}}}) \tag{5.16}$$

It employs PI controller cascaded QR controller structure, where PI controller provides fast dynamic tracking and zero steady-state error and QR controller provides high double line ripple rejection. The bode plots for PI controller, QR controller and the proposed controller are shown in Figure 5.11.

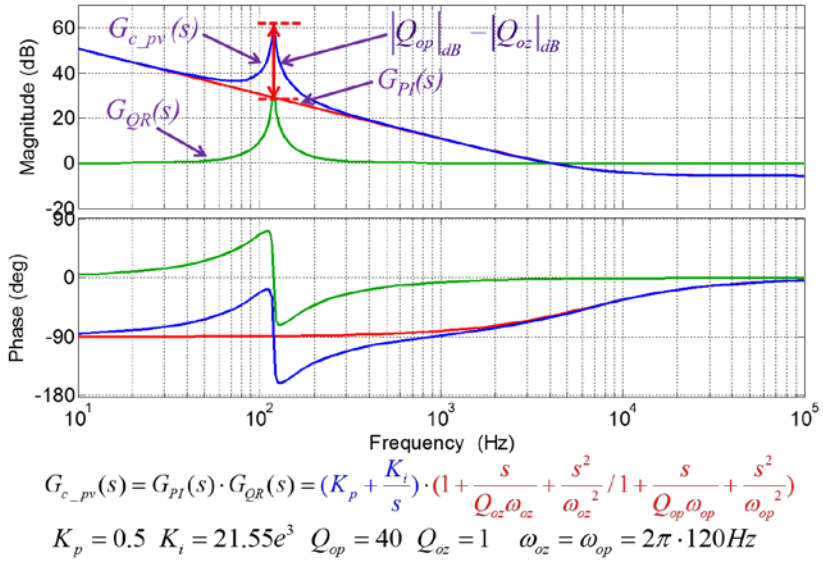


Figure 5.11 Bode plots for PI, QR and proposed controllers.

The bode plots for dc-dc converter voltage loop gain $T_{cl1}(s)$ are shown in Figure 5.12, where three cases, i.e., uncompensated, PI controller only and PI cascaded QR controller are comparatively plotted. The PI controller can be designed based on desired closed-loop phase and gain margins as that in traditional design method. For QR controller, ω_{oz} and ω_{op} are selected at the double line frequency point, i.e, 2π×120 for American grid. As shown in Figure 5.13, the QR controller can provide an extra $dB_{QR} = |Q_{op}|_{dB} - |Q_{oz}|_{dB}$ gain boost at the 120 Hz double line frequency, while it has negligible effect on the phase and gain margin.

The PV-side double line rejection capability can be examined in the frequency domain by the bode plots of $G_{vv}(s)$, as shown in figure 5.14, where the proposed cascaded controller can provide $|Q_{op}|_{dB} - |Q_{oz}|_{dB}$ more gain attenuation than the case with PI controller only at 120 Hz.

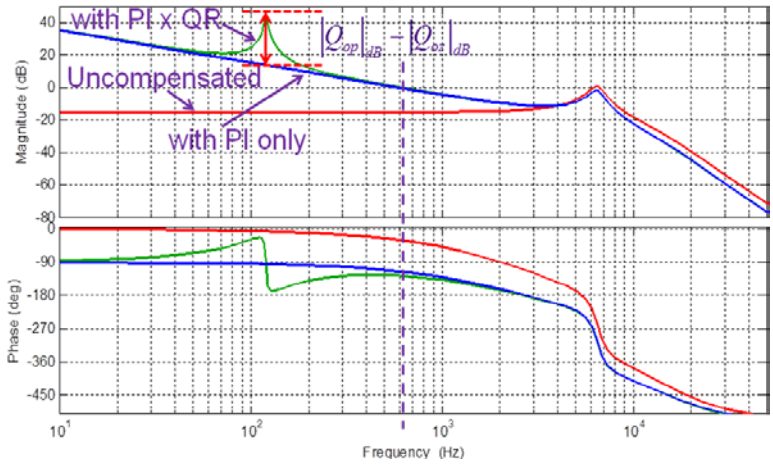


Figure 5.12 Bode plots of $T_{cl1}(s)$ for three cases: uncompensated, compensated with PI controller only and compensated with proposed PI cascaded QR controller

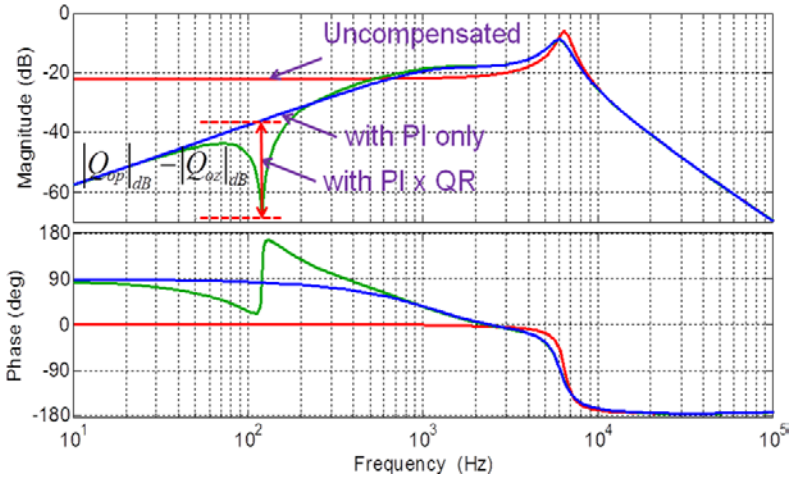


Figure 5.13 Bode plots of $G_{vv}(s)$ for three cases: uncompensated, compensated with PI controller only and compensated with proposed PI cascaded QR controller

5.4.5 Simulation and experimental verifications

The effectiveness of the proposed double line ripple rejection technique was justified by simulation and experimental results in this section.

Figure 5.14 compares the double line ripple rejection using time domain simulation for three cases: uncompensated, compensated with PI controller only and compensated with proposed PI cascaded QR controller, at the condition of DC bus peak-to-peak (P2P) double line ripple voltage 29.1 V. For the uncompensated case, the PV terminal P2P double line ripple voltage is 2 V, for the case with PI controller only, the PV terminal P2P double line ripple voltage is 0.4 V, while for the case with proposed controller, the PV terminal P2P double line ripple voltage is almost reduced to zero. Figure 5.15 shows the step response using the proposed controller.

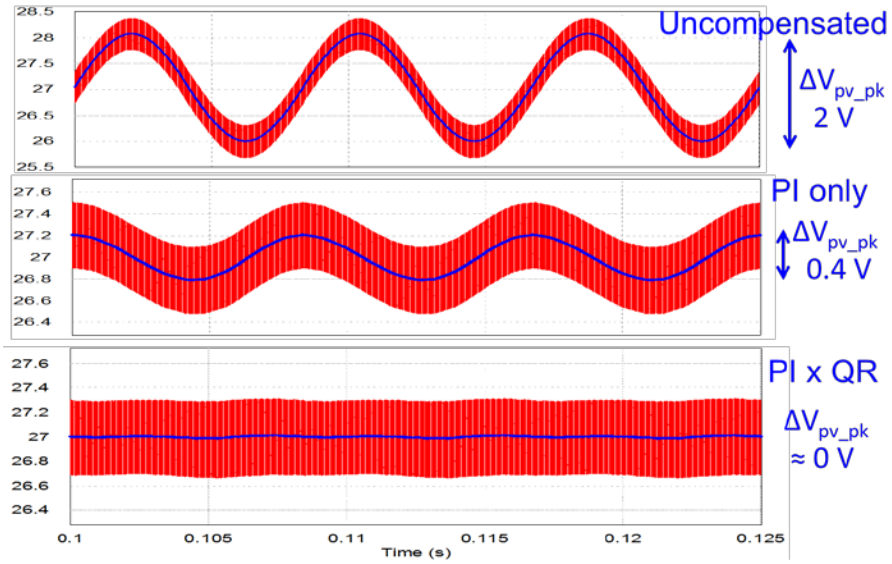


Figure 5.14 double ripple rejection using time domain simulation for three cases: uncompensated, compensated with PI controller only and compensated with proposed PI cascaded QR controller, at the condition of DC bus peak-to-peak double line ripple voltage 29.1 V.

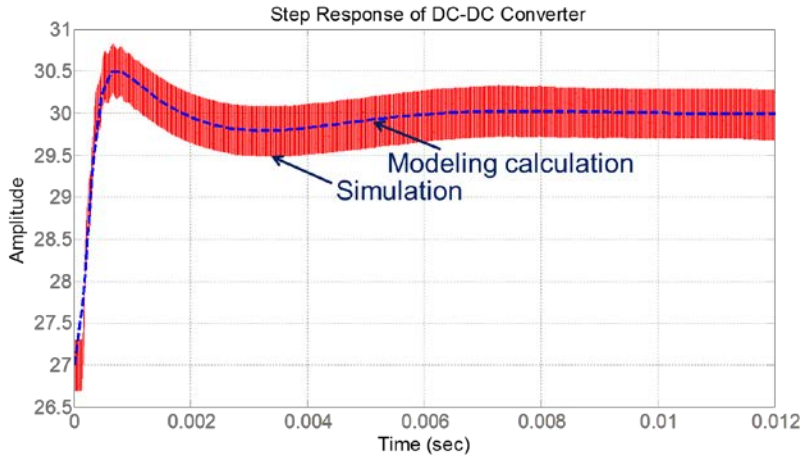


Figure 5.15 Step response of dc-dc converter using the proposed controller.

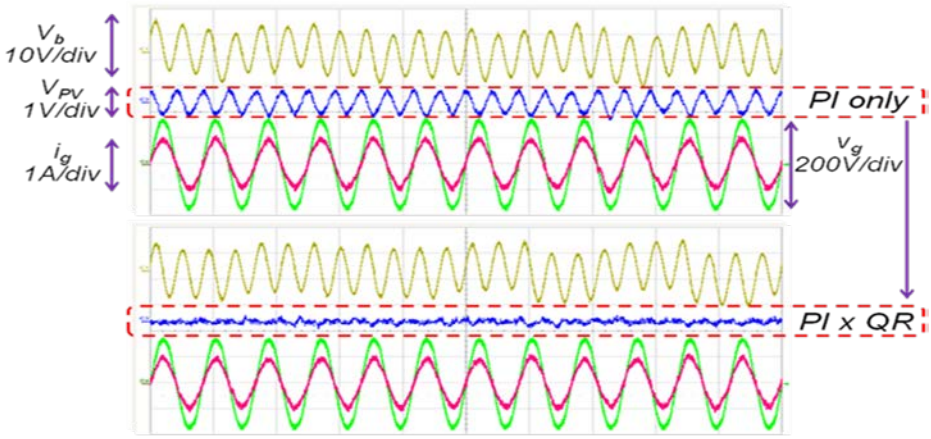


Figure 5.16 Key experimental waveforms showing the improved double line ripple rejection compensated with PI×QR controller compared to PI controller only with the PV module CS6P-240P at the condition of 170 W output power

Figure 5.16 shows key experimental waveforms showing the improved double line ripple rejection compensated with PI×QR controller compared to PI controller only with the PV module CS6P-240P at the condition of 170 W output power and 380 V DC bus voltage. The original P2P ripple of the PV module terminal voltage is about 1 V. After adding QR controller, the P2P ripple voltage is negligible small, almost zero.

5.5 Modeling and control of the grid-tie inverter with grid current distortion reduction

The grid-tie inverter regulates the DC bus voltage, assuring the power from the dc-dc converter being taken out of the DC bus quickly to maintain the power balance as well as injecting a sinusoidal AC current into the grid with minimized harmonics.

5.5.1 Control block diagram

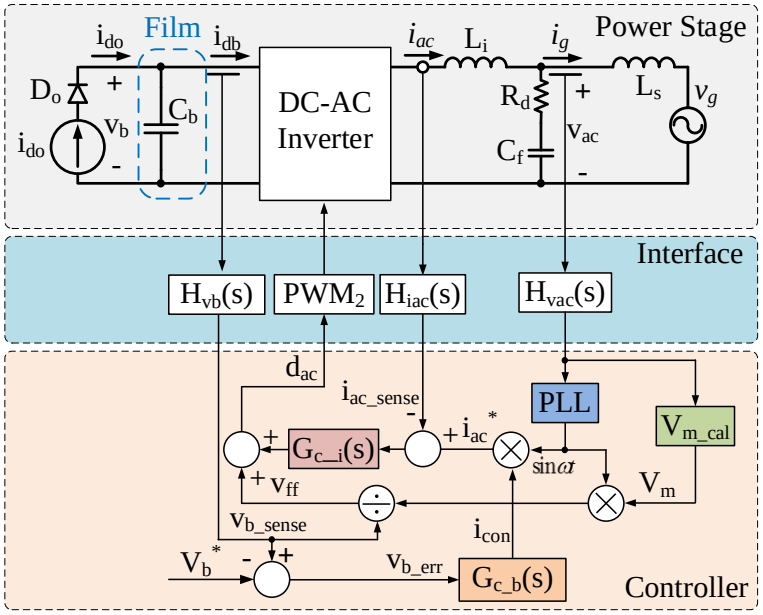


Figure 5.17 Control block diagram of grid-tie inverter.

Figure 5.17 shows the control block diagram of the grid-tie inverter, where the frond-end dc-dc converter is modelled as a current source, and the magnitude of which is dependent on the power extracted from the PV module.

5.5.2 Grid synchronization using phase-locked loop (PLL)

In order to inject an AC current synchronizing with the grid voltage, the grid phase information must be obtained first. The most popular technique to track the phase of the grid voltage is using phase-locked loop (PLL). A PLL is a closed-loop system in which an internal oscillator is controlled to keep the time of some external periodical signal by using feedback loop. The structure for a grid synchronization PLL is shown in Figure 5.18, which consists of three fundamental blocks:

- The phase detector (PD). This block uses a multiplier to generate an output signal v_e proportional to the phase difference between the grid voltage $v_{g(p.u.)}$, and the signal generated by the internal oscillator of the PLL, v_f. Depending on the type of PD, high-frequency AC components appear together with the DC phase-angle difference signal.
- The loop controller (LC). This block presents a lower power filter (LPF) to attenuate the high-frequency AC components from the output of PD, then followed by a bandpass filter (BPF) with the central frequency at 120 Hz furthering attenuating the double line frequency signal. The PI controller tracks the grid phase with a high dynamics and zero-steady-stage error.
- The voltage-controlled oscillator (VCO). This block generates at its output AC signals whose frequency is shifted with the respect to a given central frequency, ω_o.

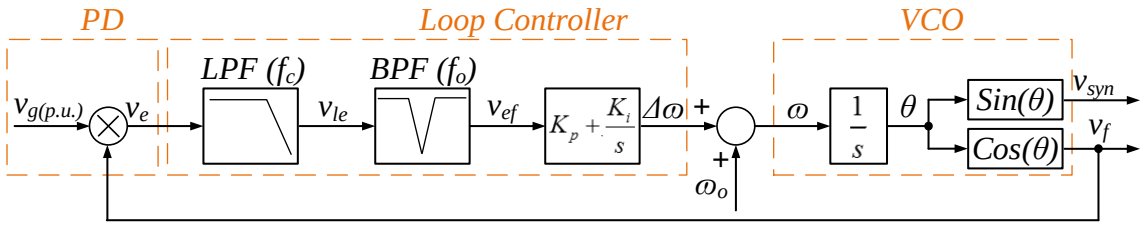
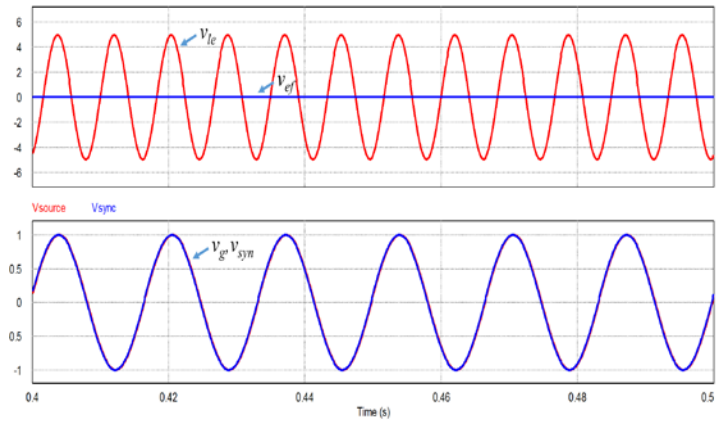
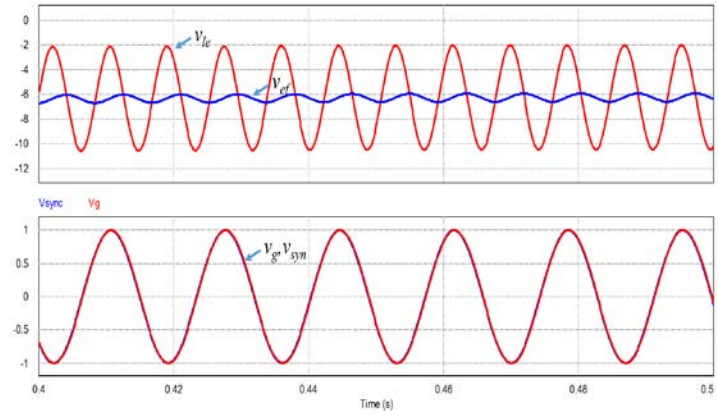


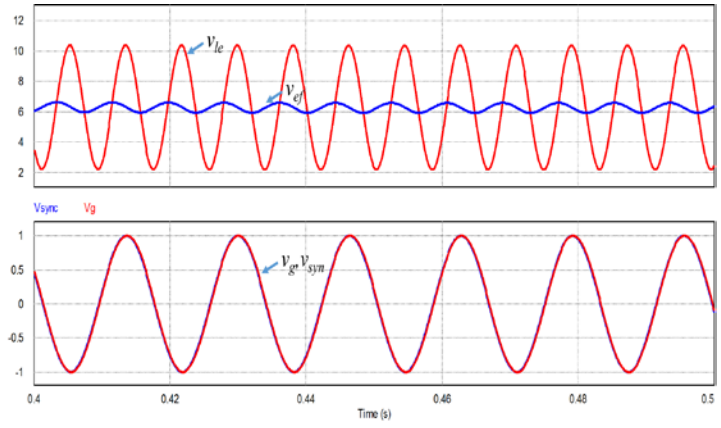
Figure 5.18 Structure of grid synchronization PLL



(a)



(b)



(c)

Figure 5.19 Simulation results for PLL with grid frequencies: (a) f_g=60 Hz, (b) f_g=59 Hz and (c) f_g=61 Hz.

Figure 5.19 shows the simulation results for PLL under the grid frequencies equal to 60 Hz, 59 Hz and 61 Hz respectively. For all three cases, the PLL can track the grid frequency and phase well and the error signals include DC and double line frequency components as well. However for three cases, the steady state error v_{ef} are different. This can be used for under- or over-frequency detection to satisfy the IEEE 1547 requirements.

Figure 5.20 gives the experimental results for the step response of PLL with K_p=30 and K_i=0.3.

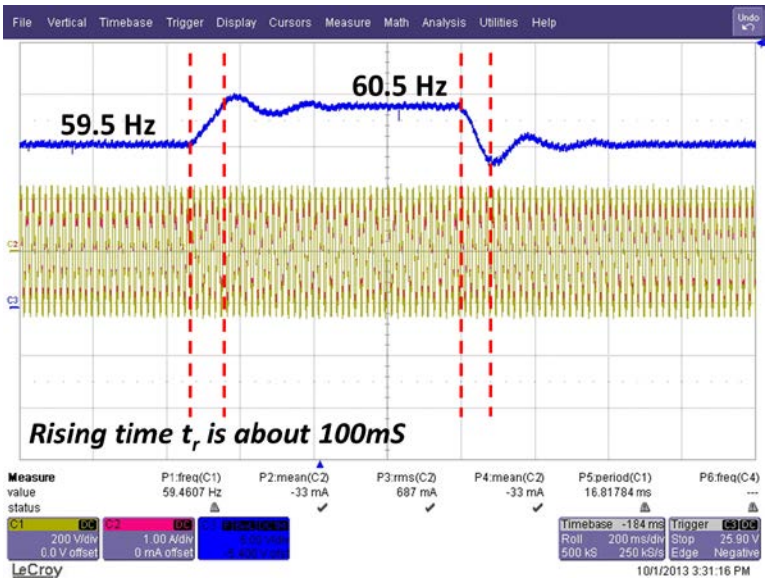


Figure 5.20 Dynamic response of PLL

5.5.3 Grid voltage magnitude V_m calculation

The magnitude of the AC grid voltage is required for a feedforward control of the AC current as well as the over- and under-voltage judgment for the IEEE 1547 code. An all pass filter is used to output a signal V_{ac_APF} with the

phase delay $\frac{\pi}{4}$ with respect to the sensed AC voltage V_{ac_sense}. Then the magnitude of the gird voltage can be calculated by calculating square root of V_{ac_sense} square plus V_{ac_APF} square.

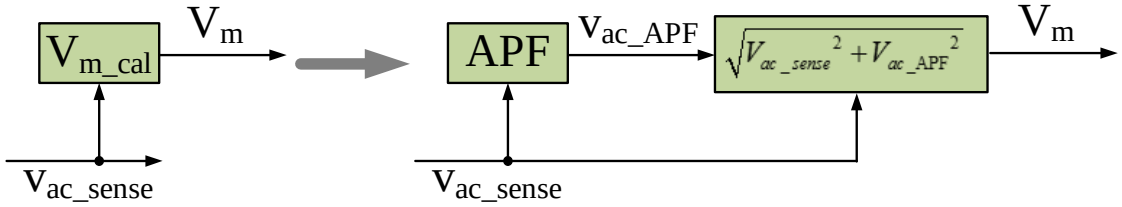


Figure 5.21 Grid voltage magnitude V_m calculation

The equation for APF is

$$\frac{\frac{s}{\omega_o}-1}{\frac{s}{\omega_o}+1} \tag{5.17}$$

where ω_o is grid angular frequency.

5.5.4 Design of grid current controller

Figure 5.22 shows the transfer function block diagram of the grid current control loop. $G_{id}(s)$ is the transfer function from the duty d_{ac} to inverter side current i_{ac}, which can be simplified as

$$G_{id}(s) \cong \frac{V_b}{sL_i} \tag{5.18}$$

$G_{iv}(s)$ is the transfer function from ac capacitor voltage v_{ac} to AC side current i_{ac}, which can be expressed as

$$G_{iv}(s) = \frac{1}{sL_i} \tag{5.19}$$

F_{m2} is the PWM modulator gain of the inverter.

$H_{iac}(s)$ is the ac side current sensing circuit and DSP software scaling gain, which can be approximated as

$$H_{iac}(s) \cong \frac{1}{1++\frac{s}{\omega_{iac} Q_{iac}}+\frac{s^2}{\omega_{iac}{}^2}} \tag{5.20}$$

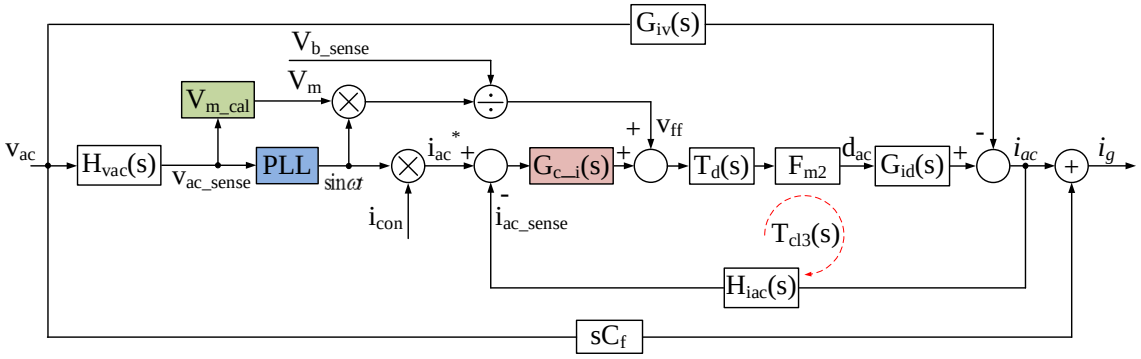


Figure 5.22 Transfer function block diagram of ac current control

The grid current controller $G_{c\_i}(s)$ has following structure,

$$G_{c\_i}(s) = k_p + \frac{2k_{r1}\omega_{c1}s}{s^2+2\omega_{c1}s+\omega_o{}^2} + \sum_{h=3,5,7,.....} \frac{2k_{rh}\omega_{ch}s}{s^2+2\omega_{ch}s+(h\omega_o)^2} \tag{5.21}$$

This controller includes two parts. One is a quasi-proportional-resonant (QPR) controller is minimize the steady-state error at 60 Hz, which is

$$G_{c\_i1}(s) = k_p + \frac{2k_{r1}\omega_{c1}s}{s^2+2\omega_{c1}s+\omega_o{}^2} \tag{5.22}$$

Here, $\omega_o = 2\pi \cdot 60$, K_p is designed to give a good transient response, K_r is designed to allow high gain at the fundamental frequency and ω_c is selected to ensure enough phase margin and implementation realization.

At the grid frequency, substituting $s = j\omega_o$ into (5.22) yields

$$G_{c\_i1}(j\omega_o) = k_p + \frac{2k_{r1}\omega_{c1}j\omega_o}{(j\omega_o)^2+2\omega_{c1}(j\omega_o)+\omega_o{}^2} = k_p + k_r \tag{5.23}$$

So $20\log_{10}(K_p + K_r)$ is the gain at 60 Hz.

The low-frequency harmonic distortion caused by the grid voltage harmonics and the nonlinearity of the power stage can be reduced by different harmonic compensators can be expressed as

$$G_{c\_ih}(s) = \sum_{h=3,5,7,.....} \frac{2k_{rh}\omega_{ch}s}{s^2 + 2\omega_{ch}s + (h\omega_o)^2} \tag{5.24}$$

From Figure 5.22, the total loop gain of the grid current control loop can be found as

$$T_{cl2}(s) = G_{c\_i}(s)T_d(s)F_{m2}G_{id}(s)H_{iac}(s) \tag{5.25}$$

The bode plot for T_{cl2} using 3rd, 5th, 7th, 9thand 11th harmonic compensators is shown in Figure 5.23. The designed phase margin is 53° at 780 Hz, the gain margin is 10.2 dB at 2.52 kHz. The gain at 60 Hz is Kp+Kr=51 dB. The high gain at harmonic frequency provide high harmonic rejection.

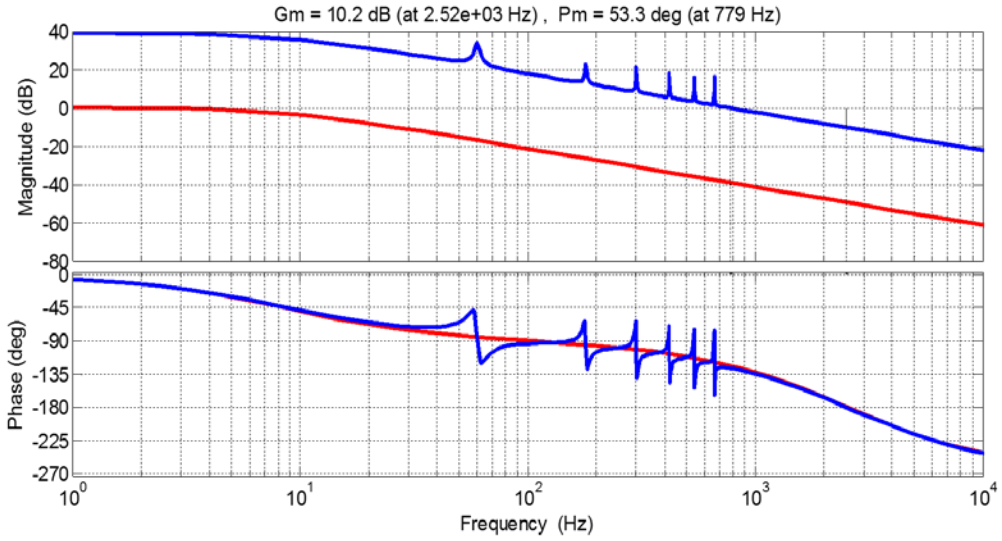
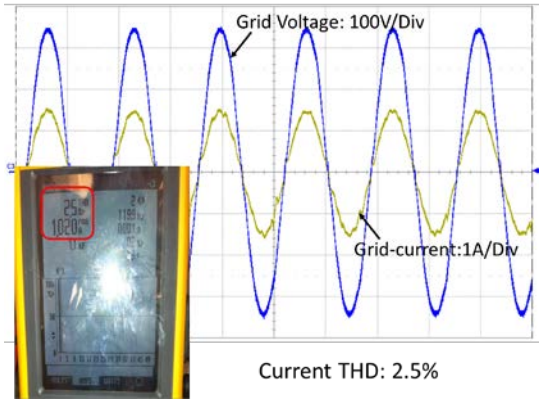
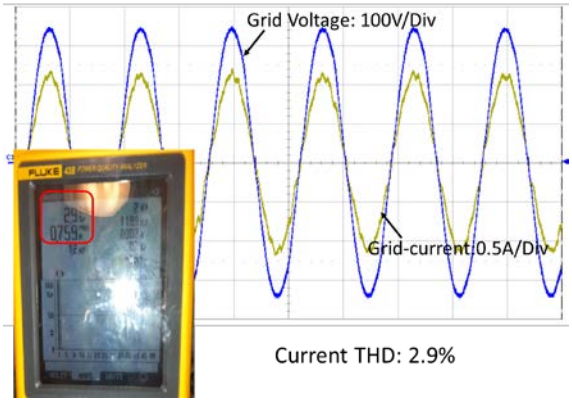


Figure 5.23 Bode plot of the loop gain $T_{cl2}(s)$ with 3rd, 5th, 7th, 9thand 11th harmonic compensators.

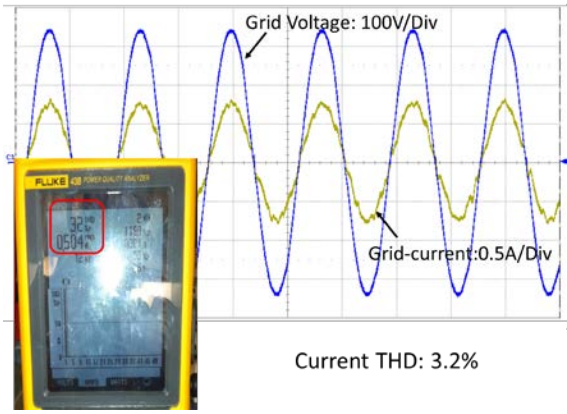
Experiments were made to justify the effectiveness of the designed current controller at different output power condition. The test results are shown in Figure 5.24.



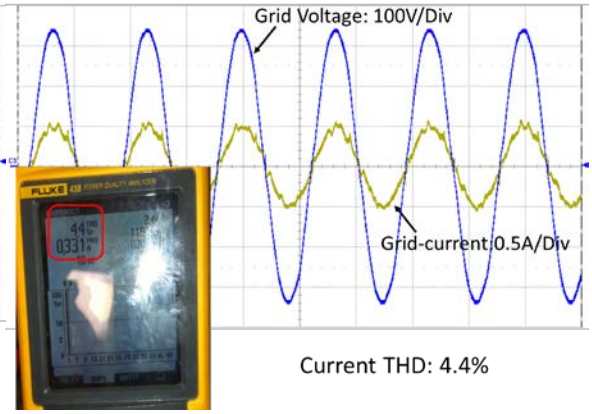
(a)



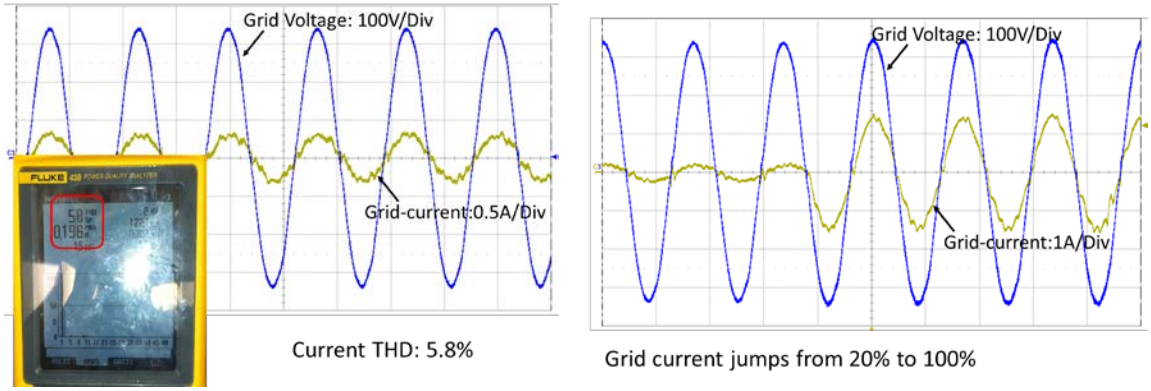
(b)



(c)



(d)



(e) (f)

Figure 5.24 Experimental results for grid current control with V_b=380 V, Vac= 240 Vac, and nominal AC current 1.04 Aac. Test conditions: (a) 100%, (b) 75%, (c) 50%, (d) 30% (e) 20% power and (f) grid current jumps from 20% to 100% power.

5.6 Design of DC bus controller

Figure 5.25 shows the small-signal transfer function block diagram of the dc bus voltage loop. $G_{vc}(s)$ is the current reference i_{con} to dc bus voltage transfer function, which will be derived later.

$H_{vb}(s)$ is dc bus voltage sensing network and DSP software scaling gain, which can be approximated as

$$H_{vb}(s) \cong \frac{1}{1++\frac{s}{\omega_{vb}Q_{vb}}+\frac{s^2}{\omega_{vb}^{\ 2}}} \tag{5.29}$$

$G_{c\_b}(s)$ is dc bus voltage controller, which needs to be designed.

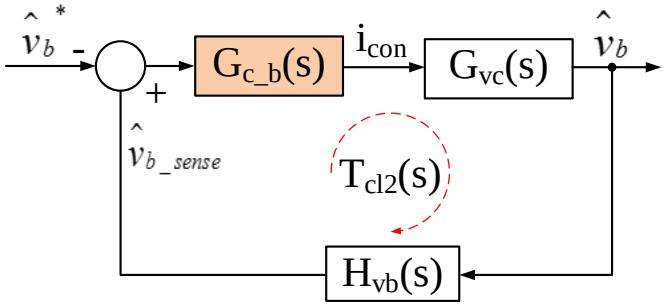


Figure 5.25 Transfer function block diagram of dc bus control loop

The output of the voltage loop controller is admittance term Y_{eq} to control power feeding to the grid. Normally, the double line frequency voltage ripple has to be filtered by the voltage loop controller in order not to cause output current distortion. So the voltage loop bandwidth is typically in the range of 10 Hz-20 Hz, which is much lower than the above-designed inner current control loop bandwidth. Under this condition, the fundamental equation that describes the average switching power balance of the system is as follow:

$$\frac{dE_{Cb}}{dt} = I_{do}V_b - P_g - P_{loss} \tag{5.26}$$

Replacing $E_{C_b} = \frac{C_b}{2}V_b^2$ and $P_o = V_{ac\_rms} \cdot Y_{eq}$ into (5.26) yields

$$\frac{1}{2}C_{dc}\frac{dV_{dc}^2}{dt} = I_{in}V_{dc} - V_{ac\_rms} \cdot Y_{eq} - P_{loss} \tag{5.27}$$

By adding small signal perturbation to (5.27) yields the following result equivalent power admittance to dc bus voltage transfer function

$$G_{vc}(s) = \frac{v_b(s)}{y_{eq}(s)} = \frac{V_{ac\_rms}^2}{I_b}\frac{1}{1+\frac{V_b}{I_b}C_b s} = \frac{V_{ac\_rms}^2}{2R_{eq}}\frac{1}{1+\frac{R_{eq}}{2}C_b s} \tag{5.28}$$

where v_{ac_rms} is RMS value of grid voltage and R_{eq} is the equivalent resistor seen by the DC bus capacitor from current-controlled grid-tie inverter.

Normally the voltage loop bandwidth is much smaller than the current loop bandwidth and current loop is controlled like a current source, so these two loops are well decoupled. The voltage loop transfer function (5.28) illustrates this feature with the dynamics of L_i diminished.

A controller with PI cascaded quasi-notch filter (QNF) is employed for $G_{c\_b}(s)$, which has following structure:

$$G_{c\_b}(s) = G_{PI}(s) \cdot G_{QR}(s) = (K_p + \frac{K_i}{s})(\frac{1 + \frac{s}{Q_{op}\omega_{oz}} + \frac{s^2}{\omega_{oz}^2}}{1 + \frac{s}{Q_{oz}\omega_{op}} + \frac{s^2}{\omega_{op}^2}}) \tag{5.29}$$

where PI controller provides zero steady-state error and fast dynamic tracking, while QNF prevents the double line ripple voltage on the DC bus form penetrating into the grid current reference. Figure 5.26 shows the bode plots of PI, QNF and PI cascaded QNF controller, where PI controller provides infinite gain at DC point and QNF provides a $dB_{QN} = |Q_{op}|_{dB} - |Q_{oz}|_{dB}$ magnitude reduction at the double line frequency 120 Hz. The bode plots for the loop gain T_{cl3} for DC bus voltage loop are shown in Figure 5.27 with uncompensated, PI controller, and PI cascaded QNF controller cases. The PI cascaded QNF controller can provide additional $dB_{QN} = |Q_{op}|_{dB} - |Q_{oz}|_{dB}$ gain reduction at the 120 Hz compared to the case only compensated with PI controller.

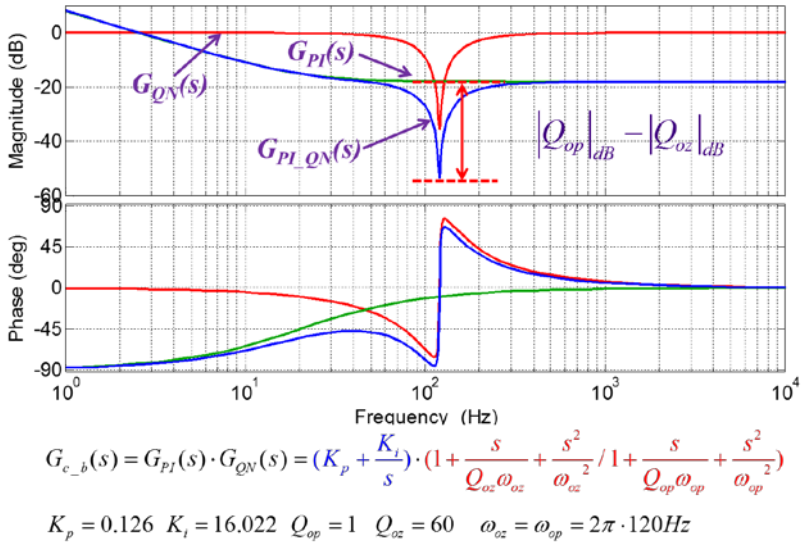


Figure 5.26 Bode plots for PI, QNF and PI cascaded QNF controller

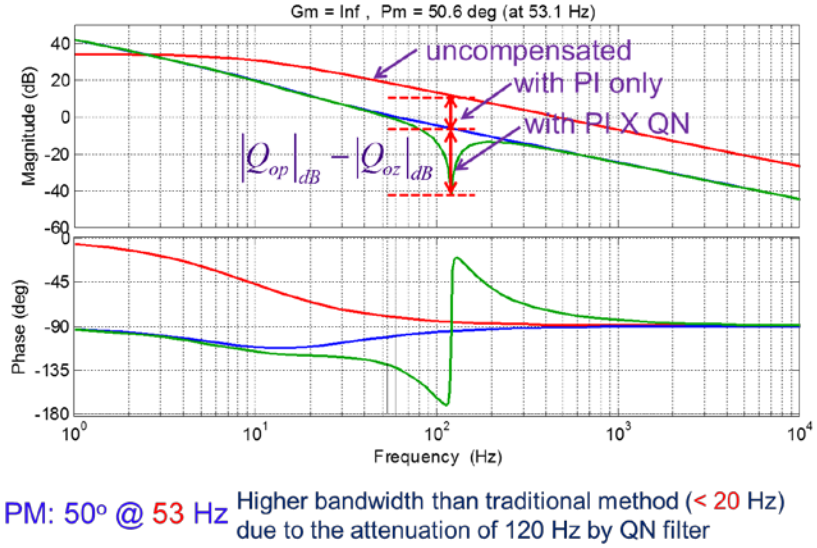
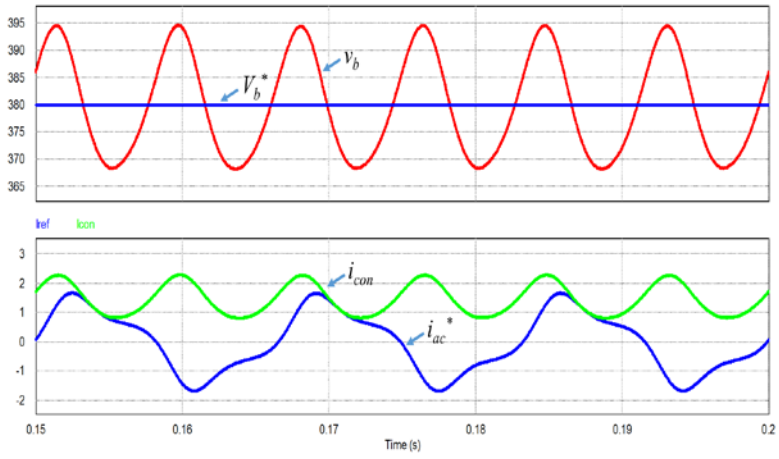


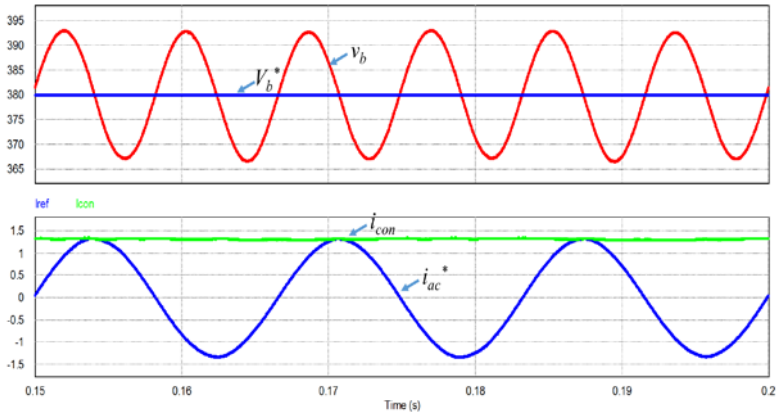
Figure 5.27 Bode plots for loop gain T_{cl3} with the cases of PI, QNF and PI cascaded QNF controllers

Figure 5.28 shows the time domain simulation results for DC bus voltage loop control with PI controller only and with PI cascaded QNF controller. For the case with PI controller only, i_{con}, the output of DC bus voltage loop has high double line frequency ripple, which leads to high distortion in the grid

current reference. While in the case using PI cascaded NQF controller, the double line frequency component in the i_{con} is greatly attenuated. This eliminates the distortion in the AC current reference i_{ac}^*.



(a)



(b)

Figure 5.28 Simulation results for DC bus voltage loop control: (a) PI controller only, (b) PI cascaded QNF controller

5.7 Experimental verifications

In order to validate the effectiveness of the proposed control technique for SPTS electrolyte-free microinverters. A 250 W prototype circuit, as shown in

Figure 5.29, has been designed, fabricated and tested with the specifications shown in Table 5-I. The PV module used for the integration test is the 240 W PV module CS6P-240P.

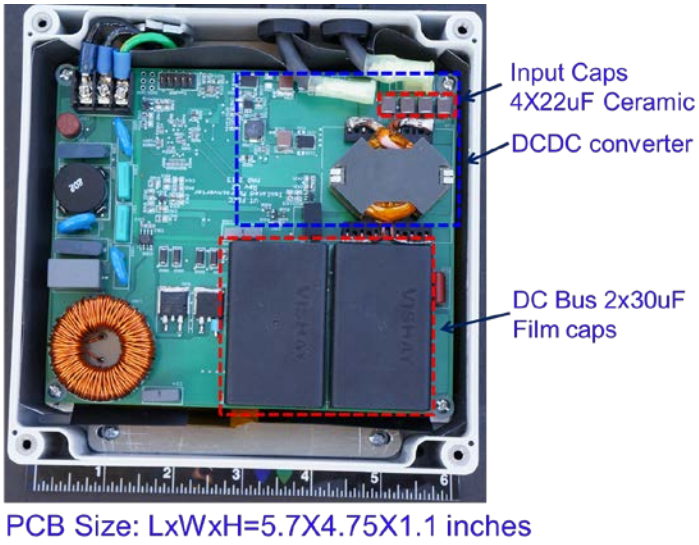
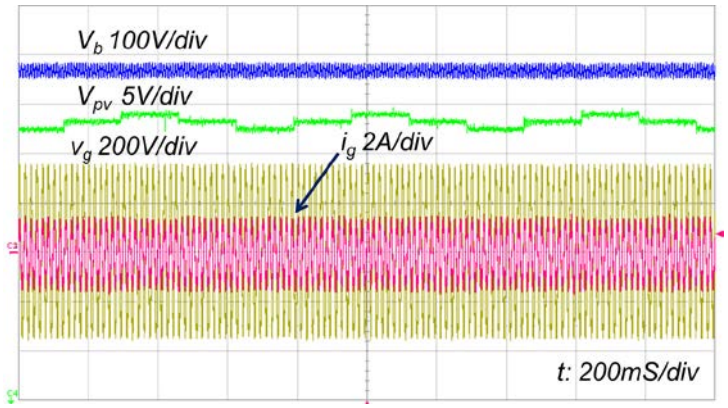


Figure 5.29 Photograph of the prototype board

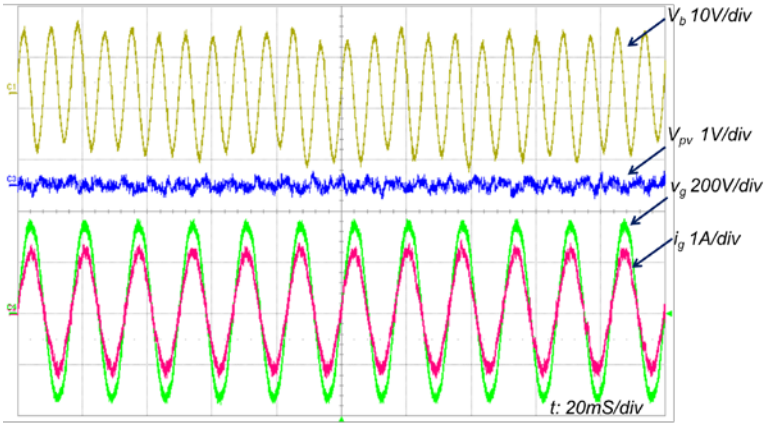
Table 5-1 Specifications for prototype circuit

PV module input voltage	20-40 V
MPPT voltage	25-35 V
Grid voltage	240Vac
Grid frequency	60/59.3-60.5Hz
Nominal output power	250 W
Nominal AC current	1.04 A
dc-dc switching frequency	100 kHz
Inverter switching frequency	24 kHz
System Sampling frequency	12 kHz
MPPT step	1V
MPPT time	167mS
Digital Controller	Texas Instrument's 28026

Figure 5.30 shows the key experimental waveforms of the test. The MPPT algorithm is P&O, which works well without the double line ripple disturbance. The DC bus has about 20 V P2P double line voltage oscillation, while the PV module could see it. The total harmonic distortion (THD) of the grid current was measured the photograph shown in Figure 5.31. The elimination of double line ripple oscillation on the PV module voltage and the low THD of grid current justified the proposed control technique was an effective way to eliminate the electrolyte capacitor for microinverters.



(a)



(b)

Figure 5.30 Key experimental waveforms

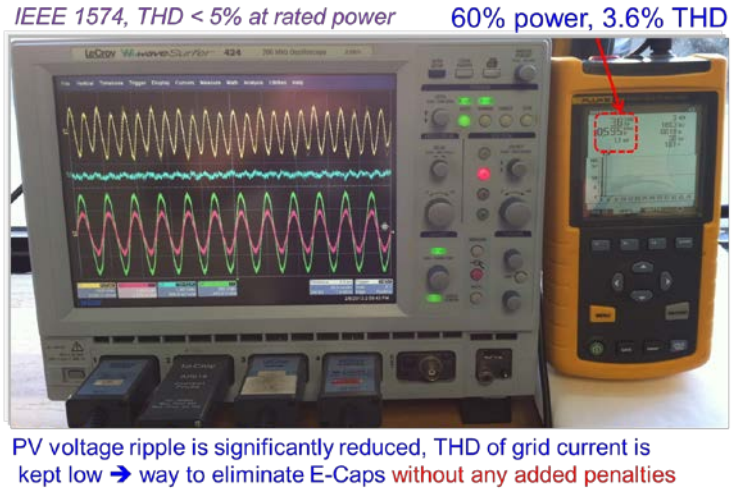


Figure 5.31 Photograph showing the low THD of the grid current and low double line oscillation in the PV terminal voltage

5.8 Summary

This section gives system level modeling of the SPTS microinverter, including hybrid transformer dc-dc converter, grid-tie inverter and the DC bus control loop. A double line ripple rejection method, which is free from the strict requirements of power stage model and no need to add specific control chips was proposed. Then the grid current and DC bus controllers were designed using traditional transfer function method. The effectiveness of the proposed control technique was experimentally verified using a 250 W prototype board. The elimination of double line oscillation on the PV terminal voltage and the low THD of the grid current validated the control technique was an effective way to eliminate the electrolyte capacitors for microinverters without any added penalties.

Chapter 6 Conclusions and Future Works

6.1 Major results and contributions of this dissertation

Microinverter, which performs MPPT at the module level, is becoming an emerging force in the PV inverter market. Since today's PV modules normally have an operating lifetime of 25 years, it would necessitate that the lifespan of a microinverter be long enough to match the lifetime of the PV module. A major source of concern in single-stage microinverters are the electrolytic capacitors that have been identified as one of the most unreliable components. Using a two-stage architecture has been justified as an effective way to get rid of the unreliable electrolytic capacitors in the system. The two-stage microinverter architecture consists of a boost type dc-dc conversion stage and a dc-ac inversion stage.

The challenges of designing this dc-dc converter are the requirements for high CEC efficiency while maintaining low cost and simple structure. A new high boost ratio dc-dc converter was presented in this dissertation to address the aforementioned challenges. The energy transferred through the magnetic core in the proposed converter combines the modes where the transformer operates under normal conditions and where it operates as a coupled-inductor, as a result, the magnetic utilization is improved allowing the use of smaller magnetics. The proposed converter transfers the capacitive and inductive energy simultaneously which increases the total power delivery improving the power semiconductor device utilization. Since the resonant

current resonates back to zero at switching transitions, the switching losses are reduced achieving improved efficiency for all load conditions. The measured peak CEC efficiency of the proposed dc-dc converter reaches 97.3% and maintains high efficiency over wide output power range., High efficiency over a wide power range is desirable for microinverter applications, since the maximum output power of PV modules is time varying due to the different levels of radiation, temperature and shading effects.

Transformerless inverters have been commercially justified as having higher efficiency, lower EMI and leakage current over traditional full-bridge inverters. A transformerless inverter topology employs split-phase structure eliminating the poor body diode reverse-recovery issue allowing the use of high speed superjunction MOSFETs. Combining the fast-switching superjunction MOSFETs with zero-reverse-recovery SiC diodes ultrahigh efficiency can be achieved even under hard-switching conditions. The CEC efficiency of the proposed transformerless inverter is 98.6% based on a 250 W prototype board.

In order to reduce the cost and volume of two-stage electrolyte-free microinverters, the number of energy buffer capacitors must be limited. With the reduced energy storage capacitance, the DC bus would have high double line ripple oscillation. This will lead to degradation of MPPT efficiency if the double line ripple propagates back to PV side. If the double line energy is not stored in the capacitor it could cause grid current distortion. A control

method addressing these two issues is presented. The proposed control method adds a series quasi-resonant (QR) controller into the voltage control loop of the dc-dc converter to provide a high loop gain at double line frequency. This high loop gain causes the dc-dc converter to reject the PV-side double line frequency oscillation. A series quasi-notch filter (QNF) is added in the DC bus voltage loop to provide a low loop gain at double line frequency to prevent the reference current distortion of the grid current loop. The experiments to test these control loop modifications were performed using a 250 W microinverter prototype board. The tested waveforms with zero double-line ripple oscillation on the PV module terminal voltage and the low THD in the grid current justify the proposed method as an effective way to eliminate the electrolytic capacitors in microinverters without any added penalties.

6.2 Future works

Although the presented hybrid transformer dc-dc converter has the advantages of simple structure, low cost and high efficiency. It is not suitable for the applications where isolation is mandatory by the utility code. The challenge of the isolated version, as shown in Figure 2.21 (d) of the proposed converter is how to deal with the leakage inductance. One solution is running the isolated converter in quasi-resonant (QR) mode, which can not only reduce the switching losses but also recycle the leakage energy. For traditional PWM converters running in QR mode, the turn-on instant of the

main switch is determined by the valley voltage of the drain-source. The turn-off instant is decided by the peak magnetizing current. In the hybrid transformer converter, the turn-on of the main switch can be determined by the valley voltage of drain source. The primary current includes not only the linear magnetizing current, but also the resonant current, which makes designing a control method to decide when the turn-off instant of the main switch as an interesting research topic.

Grid support using reactive power control is a new trend for grid-tie inverters. The proposed inverter is the only MOSFET inverter which can support reactive power control due to the split-phase structure. The issue with the proposed topology is for reactive power control if the switches in the separate split phases run together, high circulating current exists between these two phases. How to implement reactive power control for the proposed inverter topology is also an interesting research topic.

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