CHAPTER V

SUMMARY AND CONCLUSIONS

An integrated systems approach to standardizing power electronics components and packaging techniques in the form of power electronics building block has emerged as a new concept in the area of power electronics. Power electronics building blocks are envisioned as integrated power modules consisting of power semiconductor devices, power integrated circuits, sensors and protection circuits for a wide range of applications, such as inverters for motor drives and converters for power processing equipment. This research was focused on the processing of an innovative three-dimensional packaging architecture for power electronics building blocks with soldered device interconnections and subsequent characterization of its critical interfaces.

To successfully implement a packaging concept, it is imperative to resolve many challenging issues related to materials and processing, which would result in improved thermal management of the power electronics modules. Consequently, while the first part of the research was focused towards module fabrication, the other parts of the research were focused into characterizing two specific interfaces of the fabricated module. The first interface of interest was the device interconnection interface while the second one was the module to heat spreader attachment interface. The device-pad to interconnection interface was characterized for its electrical resistance, which is at the heart of implementing a direct chip attachment protocol. On the other hand, the module to heat-spreader interface serves the most critical task of heat dissipation and ensures proper thermal management of a three-dimensional power module structure. Furthermore, from a reliability point for view, the module to heatspreader interface is the most crucial interface in the whole package structure due to the significant mismatching of CTE with the silicon device.

In the following paragraphs, conclusions from the three above-mentioned thrusts of this research are summarized.

5.1 Packaging of Metal Posts Interconnected Parallel Plate Structure Modules

This part of the research was focused to design and fabricate more reliable and high performance packaged PEBB module eliminating the usage of wire bond in the process. To define the structure and devices to be used in generic PEBB design, several power stage topologies were considered. A phase leg design was performed and appropriate gate driver configurations were investigated, including the incorporation of soft switching techniques. These configurations were modeled to demonstrate their applicability for PEBB use. Using modeling tools, we concluded that packaged wire-bond modules have significantly higher parasitic inductance and capacitance due to fine wires for interconnecting power devices and not-optimized circuit layout. We developed a low-cost approach, termed metal posts interconnected parallel plate structure (MPIPPS), for packaging high-performance modules of power electronics building blocks (PEBB). The new concept implemented direct bonding of copper posts, not wire bonding of fine aluminum wires, to interconnect power devices as well as joining the different circuit planes together. Modeling and experimental results of the prototype modules (implemented as an inverter phase leg) support the improved electrical performance of this new packaging technique. Moreover, this packaging approach required less expensive equipment and had shown the potential to produce modules having superior electrical, thermal, and mechanical performance. We have demonstrated the feasibility of this approach by constructing PEBB modules (consisting of IGBTs, diodes, and a few gate driver elements and passive components).

In the 1st phase of module fabrication with IXGD40N60A IGBTs, we had successfully fabricated packaged devices and modules using the MPIPPS technique. These modules were tested and operated at

pulse-switch and high power stages up to 6kW. However, in the 2nd phase of module fabrication with IXSD35N120A devices, we experienced significant yield problems due to metallization difficulties of these devices. Only a few packaged devices and modules passed the pulse-switch test while none passed the high-power stage test.

Despite the yield problems in the 2nd phase, a few advantages of this three-dimensional packaging approach (as observed in the 1st phase module testing) can be summarized as follows:

- The substrate does not need to allocate the conductor traces for bonding wires; the whole real estate can be utilized efficiently at high power level.
- The negative and positive terminal leads are located in different planes allowing the implementation of the laminated terminal design, which cannot be implemented in a wire-bond design. The laminated structure of a three-dimensional design would significantly reduce the termination inductance, which is a major concern in a wire-bond module.
- Ability to carry large currents with negligible parasitic inductance and capacitance due to short and thick metal posts that are used for the interconnections in the module.
- Better thermal management due to additional thermal paths offered by the posts and the option of dynamic cooling with the use of a dielectric fluid flowing through the devices in-between the plates.
- Ease of integration of passive components since multiple plates can be readily stacked on top of one another through metal posts.
- Better reliability due to stress relief at metal posts and low thermal stresses with the use of identical plates for the circuit planes.

Based on the above mentioned advantages and preliminary test results, we conclude that the MPIPPS packaging approach can be effectively implemented for packaging low-cost power electronics modules.

5.2 Processing and Characterization of Solderable Interconnection of Devices

One of the main objectives of this research was to design direct copper interconnection technique for power electronics modules by eliminating the use of wire bonds. When compared to the wire-bonds, solder interconnects provide larger effective contact areas between power semiconductor devices and overlying power metallization. The larger contact area greatly reduced the current crowding and distributes the mechanical and thermo-mechanical forces over a larger area, thus reducing equivalent mechanical stresses at the device connections. However, eliminating wire bonds required the development of a solderable interface on the emitter contact and gate contact of the IGBTs used in the power stage circuit, since solderable devices were not available from the IGBT manufacturers. Based on the requirements and reliability considerations, we employed three different metallization schemes with two different deposition techniques. The first UBM scheme involved physical vapor deposition of Ti-Ni-Cu and Cr-Cu via sputtering. The second UBM scheme included an electroless process of Zn-Ni-Au metallization. Metallization process produced excellent yield in the case of IXGD40N60A devices, which were Si_3N_4 passivated. However, under the same metallization schemes, IXSD35N120A devices (used in the 2nd phase of module fabrication) with a polyimide passivation exhibited inconsistent electrical contact resistance in the case of sputtering, while degradation of breakdown characteristics was observed in the case of electroless deposition.

With all the processing and characterization work on the device interconnection schemes, we can summarize our findings as follows.

- A primary concern with achieving adhesion is the presence of organic contamination on the surface. Contamination can reside in any of the following forms – residues, anti-oxidants, carbon residues and other organic compounds.
- Organic contaminants such as hydrocarbons remain in the form of thin monolayers on the surface, even in the case of as-received devices from the manufacturer. Absorbed monolayers of hydrophobic and

hydrophilic surfaces consist of different chemical compositions and accordingly, the attraction forces of these absorbed layers are also different, which affects the bonding properties of the resulting surfaces.

- In the case of polyimide passivated devices, plasma etching may have introduced a few carbon constituents on the surface. XPS Spectra shows clear evidence of possible carbon contaminants, such as carbide (~282.9eV) and graphite (~284.3eV) on the surface at binding energies below the binding energy of the hydrocarbon peak (C 1s at 285eV). Whereas above the hydrocarbon peak energy level, presence of carbon-nitrogen compounds, single bond carbon compounds (~285.9eV), and double bond carbon compounds (~288.5eV) are present. However, a majority of the carbon is associated with hydrocarbons, which are hydrophobic in nature, thus making the device contact pad less wettable.
- Plasma cleaning process may be modified with an extensive amount of optimization of the process parameters. However, alternative solutions to remove hydrocarbon contaminants do not look promising due to their possible interaction with polyimide.
- Fluorine contaminants were evident on the device contact pads. These contaminants were originated during the etching process of the polyimide to open contact pad areas. Clearly, at the fabrication step, these contaminants were not properly removed.
- Electroless deposition process is not suitable for metallizing polyimide passivated devices due to polyimide degradation with alkaline exposure. The curing of the polyimide passivation needs to provide sufficient chemical resistance, which is not achieved by the device manufacturer at the present time.

The research on the processing and characterization of the device interconnection interface has lead IXYS to replace polyimide passivation on the IXSD35N120A devices with silicon nitride. More importantly, the advantages of solderable contact and subsequent packaging possibilities have prompted them to fabricate IGBTs with solderable source and gate contacts.

5.3 Processing and Characterization of Module to Heatspreader Attachment

In this part of the research, interfacial thermal resistance of a few common attachment materials (solder and thermally conductive epoxy) between the power module and the heat spreader were characterized. Processing parameters such as applied pressure and environment of the solder reflow and epoxy curing were varied to fabricate test samples for subsequent comparison of the resulting interfaces. Typical attachment materials introduced interfaces and/or interlayers of finite thickness. Using a scanning acoustic microscope (SAM), a non-destructive inspection tool, we detected void content in the interface layer, which was then correlated to the measured thermal resistance of an interface. In the following paragraphs, the observations throughout the processing and characterization schemes of interfacial thermal resistance of the heat spreader attachment are summarized.

- We have found that even the same solder paste alloy with no-clean flux (manufactured by different suppliers) has resulted in different void contents with the same reflow process.
- Void content is dependent on flux content and flux activity. On the preform samples, we added a thin layer of no-clean flux for air as well as nitrogen atmosphere. Addition of this flux increased the flux activity during a perform reflow compared to that of the solder paste reflow. It is most likely that the flux added to the preform had a higher fluxing action than the flux contained in the solder paste. Furthermore, a higher fluxing activity suggests that fluxing reaction and activator induced decomposition are not the major sources of outgassing. On the other hand, the outgassing of the entrapped flux profoundly affects the void formation and a lower void content indicates a lesser amount of trapped flux. In the case of a solder paste, the flux is in direct contact with the surface oxide of the powders and the surface to be soldered. Consequently, during reflow, any residual oxide can be expected to have some flux adhered to it. In the case of solder preform with added flux, the higher activity flux usually eliminates the oxide more rapidly and more thoroughly, thus leaving fewer spots for the flux to adhere to.

- As the metal loading of the solder increases, the amount of oxide on the metal surface also increases. In addition, with the increase of metal loading, the flux content decreases, thus increasing void content. Moreover, tighter packing of the solder powder may create more difficulty for entrapped flux to escape.
- Higher dispensed or printed volume of solder paste results in higher void content. For thicker interfaces with a same joint area, we have observed more entrapped voids.
- In our sample preparation scheme, solder reflow profile is kept the same for the solder preform and the paste samples. As a result, we assume that solder profile did not affect the observed differences in void content.
- Void contents in all cases of nitrogen reflow are consistently lower than the air-reflowed samples. In a reduced environment, the effectiveness of fluxing activity improves, thus reducing void content.
- In our sample preparation scheme, all DBC pieces and copper coupons were given the same cleaning treatment before applying solder paste and silver epoxy. Therefore, the human errors are assumed to be the same in all prepared samples.

Based on our characterization work, we recommend the following for an optimized heatspreader attachment process with minimized void content:

- use solder preform as the interface material
- use fluxes with higher flux activity;
- use inert reflow atmosphere to improve substrate solderability; and
- minimize surface roughness and maximize surface flatness.

This investigation has resulted in optimizing the bonding process of the selected interface material, (which is typically ignored in the conventional module fabrication protocol), thus minimizing the void-content to ensure enhanced thermal management of power modules. Also, this research provided sufficient evidence for thermal modeling work to include contact resistance, which evidently constituted the largest part of the interfacial thermal resistance.

Packaging of power electronics building blocks is a critical part of the Navy's strategic approach to power electronic systems. The accomplishments on this research will significantly advance the current packaging effort and establish a solid foundation for the development and implementation of future power electronics modules with enhanced electrical and thermal performance.