

# **Processing and Characterization of Device Solder Interconnection and Module Attachment for Power Electronics Modules**

by

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## (ABSTRACT)

This research is focused on the processing of an innovative three-dimensional packaging architecture for power electronics building blocks with soldered device interconnections and subsequent characterization of the module's critical interfaces. A low-cost approach termed metal posts interconnected parallel plate structure (MPIPPS) was developed for packaging high-performance modules of power electronics building blocks (PEBB). The new concept implemented direct bonding of copper posts, not wire bonding of fine aluminum wires, to interconnect power devices as well as joining the different circuit planes together. We have demonstrated the feasibility of this packaging approach by constructing PEBB modules (consisting of Insulated Gate Bipolar Transistors (IGBTs), diodes, and a few gate driver elements and passive components). In the 1<sup>st</sup> phase of module fabrication with IGBTs with Si<sub>3</sub>N<sub>4</sub> passivation, we had successfully fabricated packaged devices and modules using the MPIPPS technique. These modules were tested electrically and thermally, and they operated at pulse-switch and high power stages up to 6kW. However, in the 2<sup>nd</sup> phase of module fabrication with polyimide passivated devices, we experienced significant yield problems due to metallization difficulties of these devices.

The under-bump metallurgy scheme for the development of a solderable interface involved sputtering of Ti-Ni-Cu and Cr-Cu, and an electroless deposition of Zn-Ni-Au metallization. The metallization process produced excellent yield in the case of Si<sub>3</sub>N<sub>4</sub> passivated devices. However, under the same metallization schemes, devices with a polyimide passivation exhibited inconsistent electrical contact resistance. We found that organic contaminants such as hydrocarbons remain in the form of thin monolayers on the surface, even in the case of as-received devices from the manufacturer. Moreover, in the case of polyimide passivated devices, plasma cleaning introduced a few carbon constituents on the surface, which was not observed in the case of Si<sub>3</sub>N<sub>4</sub> passivated devices. X-Ray Photoelectron Spectroscopy (XPS) Spectra showed evidence of possible carbon contaminants, such as carbide (~282.9eV) and graphite (~284.3eV) on the surface at binding energies below the binding energy of the hydrocarbon peak (C 1s at 285eV). Whereas above the hydrocarbon peak energy level, carbon-nitrogen compounds, single bond carbon compounds (~285.9eV) and double bond carbon compounds (~288.5eV) were evident. The majority of the carbon composition on the pad surface was associated with hydrocarbons, which were hydrophobic in nature, thus making the device contact pad less wettable. XPS data showed that, after the plasma cleaning process, absorbed monolayers on the Si<sub>3</sub>N<sub>4</sub> passivated and polyimide passivated surfaces consisted of different chemical compositions and accordingly, the attraction forces of these absorbed layers are also different, which affects the bonding properties of the subsequent metallization, resulting in different contact resistances. On the other hand, with an electroless Zn-Ni-Au deposition, it was found that the polyimide passivation on the devices degraded due to alkaline exposure in the plating baths, thus lowering the device breakdown voltage significantly.

Furthermore, interfacial thermal resistances of solder preform, solder paste and silver epoxy (between the power module and the heat spreader) were characterized for process optimization. Void content at the resulting interface was found to be dependent on the flux content and flux activity. Solder preform with no-clean flux, reflowed in nitrogen results in the least resistant and minimized void-content interface. It is most likely that the flux added to the preform had a higher fluxing action than the flux contained in the solder paste. On the other hand, the outgassing of the entrapped flux profoundly affects the void formation and a lower void content indicates a lesser amount of trapped flux. In the case of a solder paste, the flux is in direct contact with the surface oxide of the powders and the surface to be soldered. Consequently, during reflow, any residual oxide can be expected to have some flux adhered to it. In the case of solder preform with added flux, the higher activity flux eliminated the oxide more rapidly and more thoroughly, thus leaving fewer spots for the flux to adhere to. Void contents in all cases of nitrogen reflow are consistently lower than the air-reflowed samples. Silver epoxy with a higher thermal conductivity (60W/mK) than Pb-Sn eutectic solder did not produce low-resistance interfaces. We found that thermal conductivity of the interface material is not the most crucial factor in reducing thermal resistance, rather it is the contact thermal resistance of the interfaces, which constitutes the largest part of the total interfacial thermal resistance. Process optimization with applied pressure and nitrogen reflow resulted in a significant lowering of contact resistance (from 0.55°C/W to 0.25°C/W) for the solder preform interfaces. We concluded that contact resistance needs to be duly accounted for in thermal modeling for an accurate representation of an interface; at the same time, the module attachment process must be tailored to reduce contact resistance for improved thermal management.

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## LIST OF ACRONYMS

AISiC	Aluminum Silicon Carbide
AMI	Acoustic Micrography Imaging
BGA	Ball Grid Array
C4	Controlled Collapse Chip Connection
CASING	Crosslinking via Activated Species of Inert Gases
CCGA	Ceramic Column Grid Array
CCMD	Chip Carrier Mounting Device
CFC	Chlorofluorocarbon
CGA	Column Grid Array
CPES	Center for Power Electronics Systems
C-SAM	C-mode Scanning Laser Acoustic Microscope
CSP	Chip Scale Packaging
CTE	Coefficient of Thermal Expansion
DBC	Direct Bond Copper
DCA	Direct Chip Attach
EDX	Energy Dispersive X-Ray
FC	Flipchip
GE	General Electric
HDI	High Density Interconnect
HTP	Harris Thin Pack
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IMS	Insulated Metal Substrate
IR	Infrared
LSI	Large Scale Integrated
MCM-HDI	Multichip Module - High Density Interconnect
MCM-L	Multichip Module - Laminated
MIL-STD	Military Standard
MMC	Metal Matrix Composite
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MPIPPS	Metal Posts Interconnected Parallel Plate Structure
PCB	Printed Circuit Board
PEBB	Power Electronics Building Block
PFC	Polymer Flipchip
PIQ	Polyimide Isoindoloquin Azolinedione
POL	Power Overlay
RF	Radio Frequency
SAM	Scanning Acoustic Microscopes
SBB	Stud Bump Bonding
SCSP	Super Chip Scale Packaging
SEM	Scanning Electron Microscope
SLAM	Scanning Laser Acoustic Microscope
SMT	Surface Mount Technology
SOIC	Small Outline Integrated Circuit
TAB	Tape Automated Bonding
TAMI	Tomographic Acoustic Micrography Imaging
TEM	Transmission Electron Microscope
TOF	Time of Flight
TSP	Temperature Sensitive Parameter
UBM	Under Bump Metallurgy
UV	Ultraviolet
VSI	Voltage Source Inverter
XPS	X-Ray Photoelectron Spectroscopy