Improved Forward Topologies for DC-DC Applications with Built-in Input Filter

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(ABSTRACT)

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Among PWM power conversion topologies, the single-switch forward topology is the one that has been most widely used for decades. Its popularity has been based on many factors, including its low cost, circuit simplicity and high efficiency.

However, several issues need to be addressed when using the forward converter such as the core reset, the voltage spikes caused by the transformer leakage inductance, and the pulsating input current waveform.

The transformer is driven in a unidirectional fashion in the forward converter; a tertiary forward converter (TFC) is an example of this. Therefore, the third winding and reset diode must be provided with an adequate period of reset time so that the flux can be fully reset by the end of each switching cycle to prevent core saturation.

Also, due to the utilization of a transformer, leakage inductances cannot be avoided. The energy stored in the leakage inductance during current ramp-up is not transferred to the load, and is not recovered during its discharge phase. As a result, the V_{DS} waveform has a voltage spike and undesirable high-frequency oscillation. Therefore, a higher voltage-rating switch should be used to reduce the risk of high-voltage breakdown. Although a switch with amply high voltage ratings is available, it would tend to have a

higher on-resistance, $R_{DS(ON)}$, resulting in increased conduction losses. Moreover, selection of a switch with higher voltage ratings than necessary may needlessly increase the cost of the design.

Usually an additional circuit such as a snubber circuit or a clamp circuit or the soft-switching technique is used to absorb these voltage spikes. Consequently, the leakage inductance is intentionally minimized in the PWM power conversion technique so that it will not degrade the circuit performance. In contrast, the leakage inductance of the transformer may enhance rather than detract from circuit performance with a resonant power conversion technique.

To date, however, no single-switch forward converter has been claimed to be able to enhance the converter performance with the PWM power conversion technique by utilizing the leakage inductance. Therefore, research on the utilization of the transformer leakage inductance in the PWM forward converter is needed. Two techniques, input current ripple reduction and an embedded filter, are proposed to enhance the performance of forward converter using the PWM technique.

By inserting a capacitor between two primary windings of the TFC, an input current ripple reduction technique is proposed and a forward converter with ripple reduction (FRR) is presented in this research work. Because the voltage of the capacitor is clamped to input voltage, the capacitor becomes a second voltage source to share part of the load current. As a result, the input current ripple is reduced. Moreover, the capacitor voltage is clamped both at the static and dynamic states; thus the excessive voltage stress on the main switch S_1 of the FAC during low-line to high-line step transient is eliminated.

Furthermore, without an external LC filter, the EMI noise levels can be further reduced as a result of the embedded notch filter formed by the transformer leakage inductance and clamp capacitor if the notch frequency is designed to be the same as the switching frequency. With the help of the clamp capacitor, therefore, the leakage inductance can enhance rather than detract from the converter performance.

The input current ripple can be reduced further by employing the proposed techniques. Two sets of the clamp capacitors and the leakage inductances are utilized, and the current ripple can even be cancelled if the condition is met. Consequently, the input current becomes a non-pulsating waveform and a forward converter with ripple cancellation (FRC) is presented. Moreover, without an external LC filter, the EMI noise levels can be further attenuated as a result of the embedded low-pass filter formed by the transformer leakage inductances and clamp capacitors. Again, the leakage inductance can enhance the converter performance just as the resonant converter does.

In addition to providing the analysis and design procedure, this work verifies the performance of the presented converters, the FRR and the FRC, by the experimental results.

By employing the proposed techniques, eight new topologies have been extended for different power conversion applications. Each member of the FRR and the FRC families is able to enhance the converter performance, in ways such as the elimination of the voltage spikes on the main switch without a snubber circuit and the improvement of the EMI performance with small filter components. Consequently, the cost can be reduced and the space of the converter can be saved.

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To my family

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Chapter 1 Introduction

1.1. Background

Among PWM power conversion topologies, the single-switch forward topology is the one that has been most widely used for decades. Its popularity has been based on many factors, including its low cost, circuit simplicity and high efficiency.

However, several issues need to be addressed when using the forward converter These include the core reset, the voltage spikes caused by the transformer leakage inductance, and the pulsating input current waveform.

The transformer is driven in a unidirectional fashion; a tertiary forward converter (TFC) is given as an example (Fig. 1-1(a)). Therefore, the third winding, L_{P3}, and reset diode, D_3, must be provided with an adequate period of reset time so that the flux can be fully reset by the end of each switching cycle to prevent core saturation.

Also, due to the utilization of a transformer, the leakage inductances (L_1 and L_3) cannot be avoided. The energy stored in the leakage inductance during current ramp-up is not transferred to the load, and is not recovered during its discharge phase. As a result, the V_{DS} waveform has a voltage spike and undesirable high-frequency oscillation, as illustrated in Fig. 1-1(b). Therefore, a higher voltage-rating switch should be used to reduce the risk of high-voltage breakdown. Although a switch with amply high voltage ratings is available, it would tend to have a higher on-resistance, $R_{DS(ON)}$, resulting in increased conduction losses. Moreover, selection of a switch with higher voltage ratings than necessary may needlessly increase the cost of the design.

Usually either an additional circuit, such as a snubber circuit or a clamp circuit, is added or the soft-switching technique is used to absorb this voltage spike. Consequently, the leakage inductance is intentionally minimized in the PWM power conversion technique so that it will not degrade the circuit performance. In contrast, the leakage inductance of the transformer may enhance rather than detract from circuit performance with a resonant power conversion technique.

To date, however, there is no single-switch forward converter that has been claimed to be able to enhance the converter performance with the PWM power conversion technique by utilizing the leakage inductance. Consequently, further research on the utilization of the transformer leakage inductance in the PWM forward converter is needed.

Due to the nature of the buck converter, the forward converter has a pulsating input current, i_G, as illustrated in Fig. 1-1(e). This input current creates high-frequency electromagnetic interference (EMI), which disturbs the operation of nearby digital and communication equipment. Reduction of such noise is required for the design to comply with international standards.

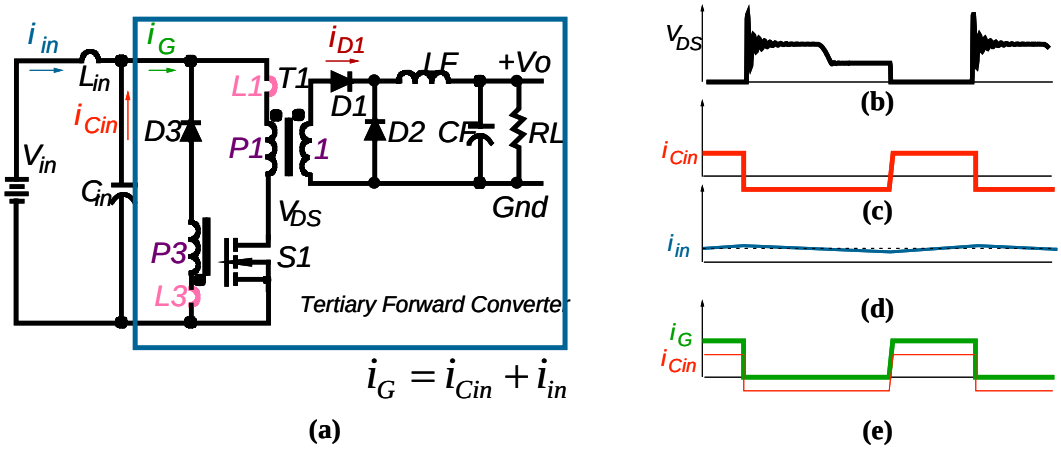


Fig. 1-1 (a) Circuit diagram and (b) key current waveforms of the TFC with an input LC filter.

Therefore, an external LC filter formed by the line parasitic inductance, L_{in}, and the filter capacitor, C_{in}, is mandatory; their addition is shown in Fig. 1-1(a). This is done so that the high-frequency switching current, i_{Cin}, is supplied by the input filter capacitor instead of coming from the input source, as shown in Fig. 1-1(b). The intensity of the EMI seen from the power source can be significantly reduced. Accompanied by additional common mode (CM) and differential mode (DM) filters, the converter can meet international EMI regulations.

However, only a few of the other problems inherent in the forward converter, such as core saturation, voltage spike, and switching loss problems have gained much attention by the proposed forward topologies in the existing literature [1]-[61].

In contrast, the problems caused by the pulsating input current have been ignored and no forward converter has been claimed to provide an effective solution without an external LC filter.

Therefore, the exploration of a comprehensive solution for achieving a better performance of the converter is the motivation of the current research work.

This dissertation provides background information about dealing with the above-mentioned issues in existing forward converters. Based on the results of the strategies used to deal with these problems, desired features for a forward converter are articulated. By utilizing the clamp capacitor and the transformer leakage inductance, input current ripple reduction and embedded filter techniques are proposed so that the PWM converter performance can be enhanced.

1.2. Comparisons of Efficiency and Voltage Stress

Because the single-switch forward converters proposed in the existing literature are focused on solving some of the inherent problems of the converter such as core saturation, voltage spike, and switching loss problems [1]-[61], the voltage stress and converter efficiency become key parameters to be watched for their impact on performance. Several forward converters with various reset schemes, including a forward converter with a Resistor-Capacitor-Diode clamp (RCD), a forward converter with an active clamp (FAC), a ZVS forward converter with an active clamp (ZVS-FAC), a ZVS Multi-Resonant Converter (ZVS-MRC) and a clamp-mode ZVS-MRC, are reviewed and compared below.

1.2.1. Forward Converter with Resistor-Capacitor-Diode Clamp (RCD)

A forward converter with a resistor-capacitor-diode (RCD) clamp circuit is illustrated in Fig. 1-2 [4]-[5]. The reset circuit is composed of a diode and the parallel connection of a resistor and capacitor, which in turn are parallel with the transformer.

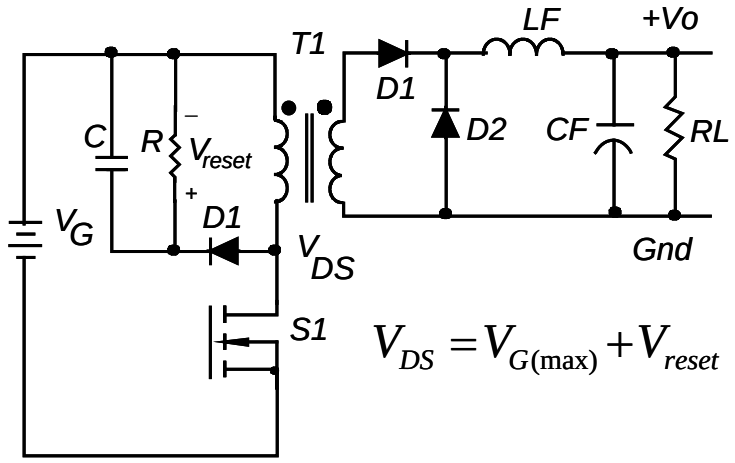


Fig. 1-2 Forward converter with RCD clamp reset circuit.

After the switch has been turned off, the diode in the clamp circuit begins to conduct. Thus a negative reset voltage, consisting of the voltage across the clamp capacitor, is provided to reset the transformer.

Without the reset winding and the additional snubber circuit, the reduction of the transformer's cost and the protection of the switch from voltage spike are the advantages of this reset circuit.

The reset voltage is independent of the input voltage [5].

$$V_{reset} \neq f(V_G) \qquad \text{Eq. 1-1}$$

Thus, the maximum voltage stress is the sum of the high input voltage and the fixed reset voltage, as shown in Eq. 1-2. Consequently, this reset scheme is more suitable than the tertiary reset scheme for wide-input-range applications.

$$V_{DS} = V_G + V_{reset} \qquad \text{Eq. 1-2}$$

It should be noted, however, that the RCD clamp circuit does not recycle the leakage energy stored in the clamp capacitor. Instead, the charge balance of the capacitor is maintained with the dissipative clamp resistor, resulting in a decrease in efficiency of performance, as shown in Fig. 1-3(a). It would be desirable to improve the converter efficiency by recovering the leakage energy and the forward converter, which can be done with the active clamp (FAC) introduced next.

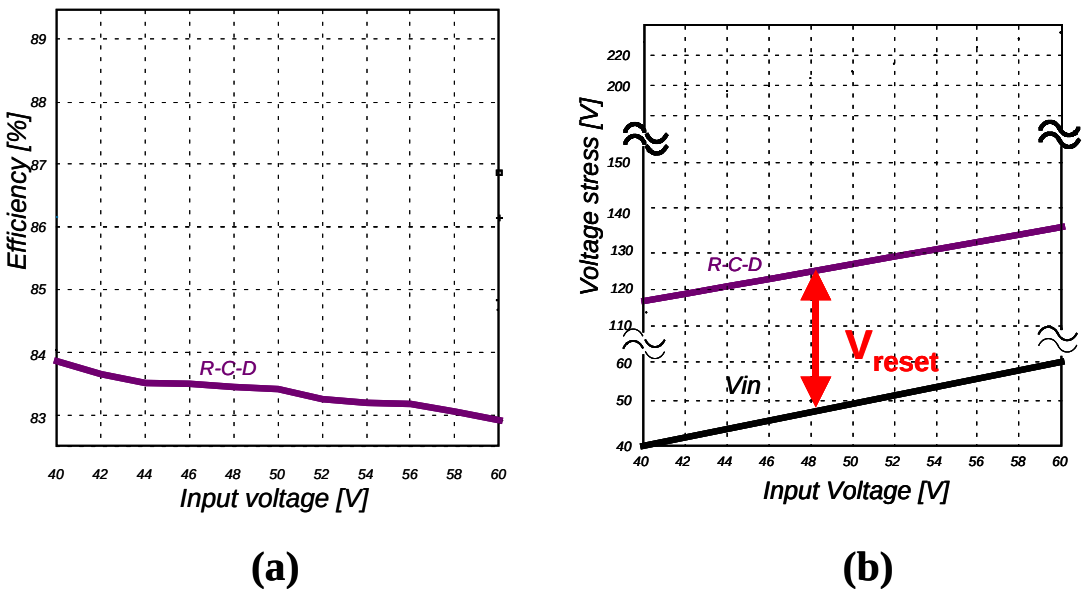


Fig. 1-3 (a) Measured efficiency and (b) measured voltage stress of the RCD forward converter.

1.2.2. Forward Converter with Active Clamp (FAC)

Fig. 1-4 shows the circuit diagram of the forward converter with an active clamp [8]-[19]. The auxiliary switch (S_a) is used to replace the diode and the resistor in the RCD clamp in order to recycle leakage energy.

The voltage across the clamp capacitor, V_{C1}, provides the reset voltage during the off time interval, and it can be derived according to the volt-second balance of the transformer.

$$V_{C1} = V_{reset} = f(V_G, D) = \frac{DV_G}{1-D} = \frac{nV_o}{1-D} \qquad \text{Eq. 1-3}$$

Eq. 1-3 illustrates that the reset voltage decreases as the operating duty cycle decreases for a constant output voltage due to the increment of the line voltage. Additionally, the voltage across the switch V_{DS} can be derived as the following equation.

$$V_{DS} = V_G + V_{reset} = \frac{V_G}{1 - \mathrm{D}} \qquad \text{Eq. 1-4}$$

Since the input voltage increases while the operating duty cycle decreases, V_{DS} tends to remain approximately constant over a certain input voltage. Consequently, this reset scheme features the lowest voltage stress on the main switch S_1 in the steady state.

Instead of being dissipated, as is the case with the RCD clamp circuit, the energy stored in the transformer leakage inductance is recycled to the input source. Consequently, the power loss is reduced and the switch is protected from a voltage spike. In addition, due to the charge balance of the clamp capacitor, the flux of the transformer is almost symmetrical in the first and third quadrants. Therefore, this topology utilizes the transformer most efficiently.

The FAC has 5% efficiency improvements and lower voltage stress than the RCD, as shown in Fig. 1-5.

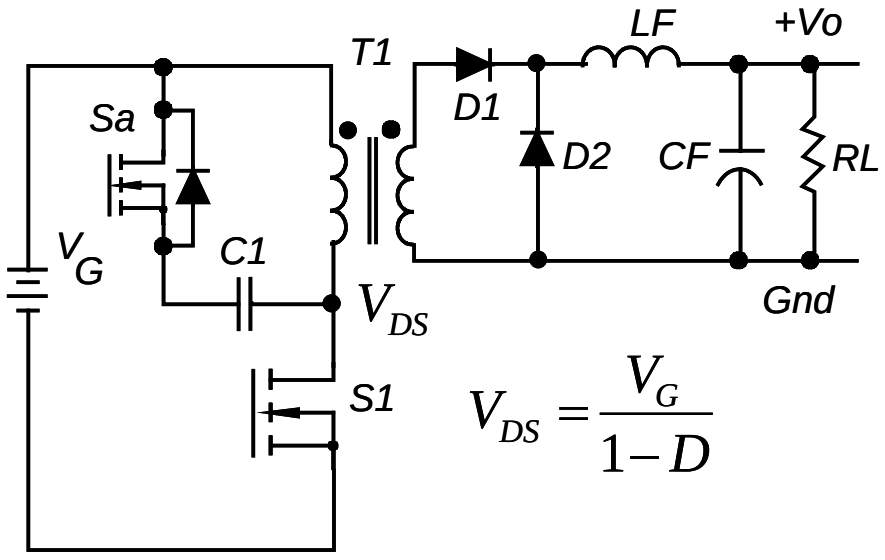


Fig. 1-4 Forward converter with active clamp (FAC).

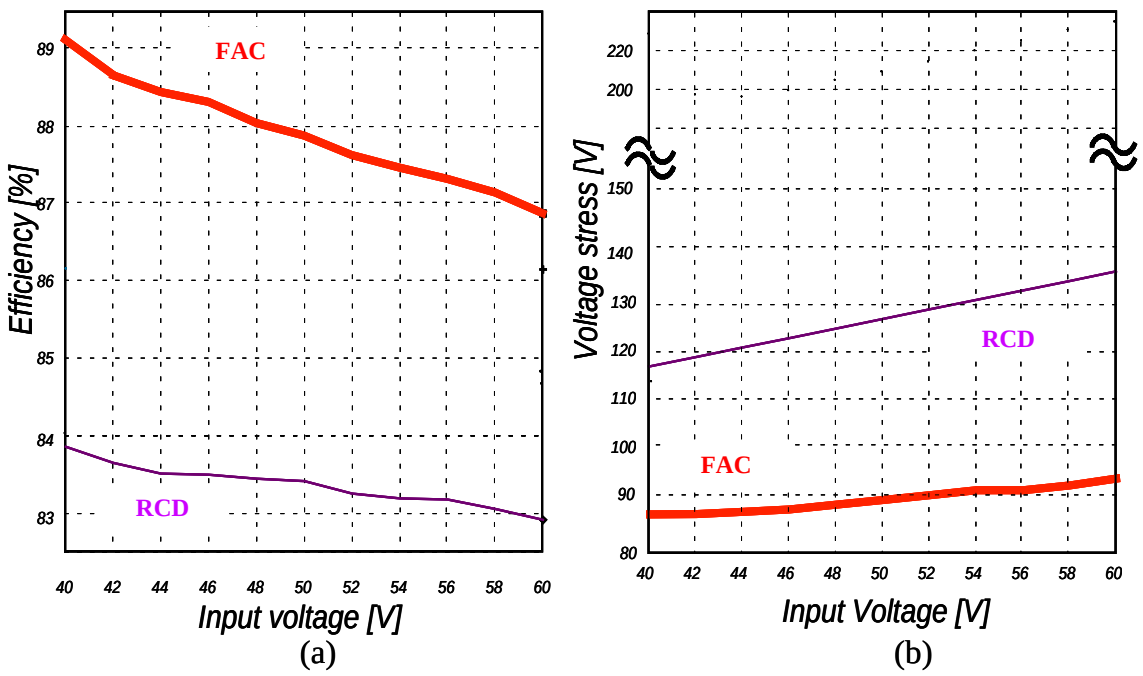


Fig. 1-5 Comparisons of the (a) measured efficiency (b) measured voltage stress between the FAC and the RCD.

It is desirable to operate the converter with zero-voltage-switching (ZVS) for high-frequency high input-voltage applications. ZVS operation of the FAC can be easily achieved, which will help to attain a higher power density, as discussed next.

1.2.3. ZVS Forward Converter with Active Clamp (ZVS-FAC)

To achieve ZVS, the energy stored in the leakage and magnetizing inductances, L_{LK} and L_m, must be large enough to provide the capacitive energy demands of the MOSFET output capacitances.

$$\frac{1}{2}L_m i_m^2 + \frac{1}{2}L_{LK} i_{Pri}^2 \geq \frac{1}{2}C_r (V_G + V_{cr})^2 \qquad \text{Eq. 1-5}$$

where Cr is the total resonant capacitance, and the combination of the two MOSFET output capacitors are in parallel with the transformer primary capacitance. The magnetizing current, i_m, is totally dependent on the transformer design, a function of the

ferrite material permeability and number of turns. Leakage inductance is affected by the winding design and technique, and the output load current reflected to the primary. Due to the light load, the leakage energy will go towards zero. Therefore, the magnetizing inductance is the more significant energy to achieve ZVS.

Consequently, ZVS operation of the FAC can be achieved by simply adding a gap in the transformer to reduce the magnetizing inductance or increase the peak magnetizing current [14].

However, the price to be paid for achieving ZVS is the increased conduction loss of the switch. The primary conduction losses of the ZVS-FAC are approximately 35% higher than the FAC.

The merits of the ZVS-FAC can be summarized as listed below.

1. Low switching losses and low switching noise;
2. Minimum voltage stress of the main switch; and
3. Maintenance of ZVS for the entire load range and line range.

However, the switch loss improvements cannot compensate for the increased conduction loss under the low line operating conditions as shown in Fig. 1-6(a). In contrast with to the FAC, the efficiency improvements are only achieved above the nominal line operating conditions. Another efficiency study for the off-line applications shows the same tendency as illustrated in Fig. 1-7 [15]. It can be concluded that the FAC has good efficiency performance and the soft-switching operation is an optional feature for some applications.

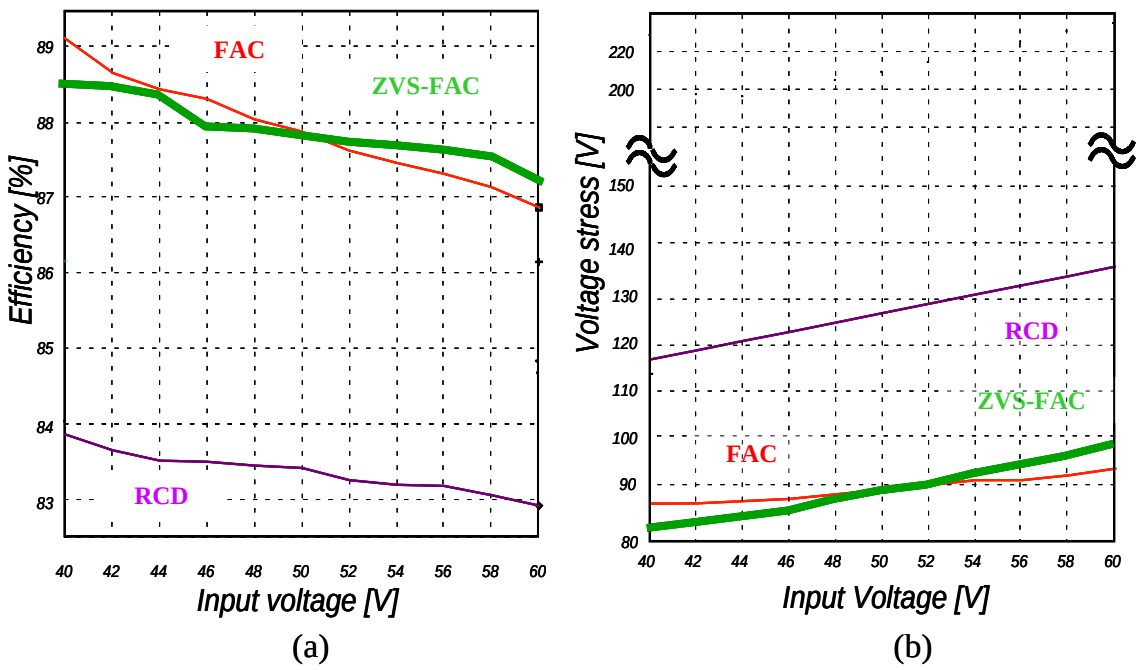


Fig. 1-6 Comparisons of the (a) measured efficiency (b) measured voltage stress of the RCD, the FAC, and the ZVS-FAC.

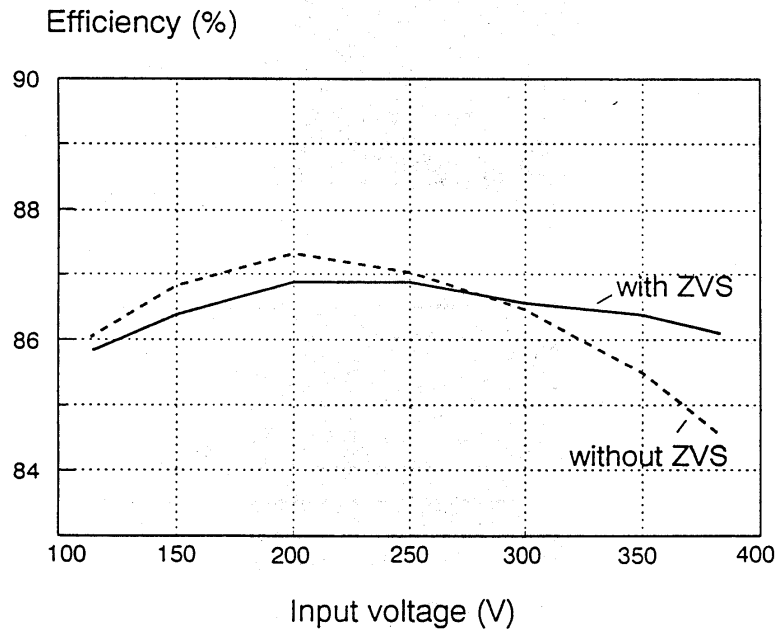


Fig. 1-7 Efficiency comparison between the FAC and the ZVS-FAC for the off-line applications /courtesy of G. Hua [15].

1.2.4. Zero-Voltage-Switched Multi-Resonant Forward Converter (ZVS-MRC)

The circuit diagram of the forward ZVS-MRC is shown in Fig. 1-8. The ZVS-MRC was proposed to achieve optimum soft-switching performance for all semiconductor devices in the power circuit [16]. All the major parasitic components, including the MOSFET output capacitance, diode junction capacitance, and the transformer leakage inductance, are absorbed into the resonant circuit. ZVS of the MOSFET and diode is obtained by shaping the voltage waveforms across the switches so that the device voltage returns to zero before turn-on.

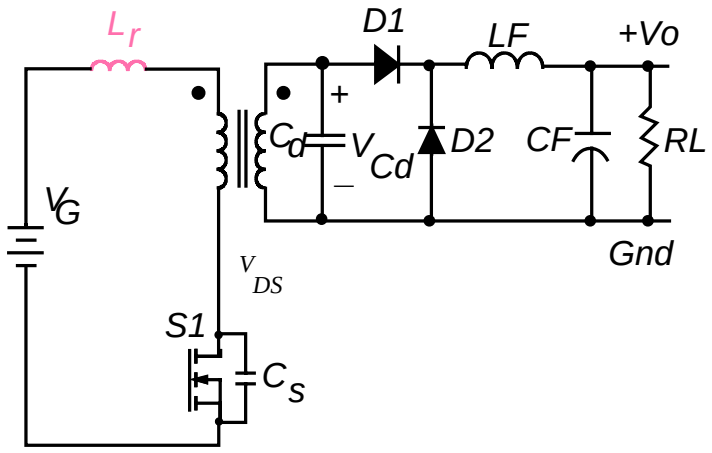


Fig. 1-8 Forward converter with ZVS-MRC.

However, by allowing resonance of the output capacitance of the switch, voltage stress across the MOSFET is three to four times the input voltage. This limits the use of the single-ended ZVS-MRC in off-line applications. Furthermore, conduction loss of the MOSFET is also increased when higher-voltage-rating devices are used.

The forward ZVS-MRC has an inherent automatic reset mechanism due to the interactions between the magnetizing inductance and the secondary-side capacitor. The

volt-second across C_d is equal to the volt-second applied to the transformer. If the net volt-second applied to the transformer is positive during one cycle, it will cause the magnetizing current to increase. This increment of the magnetizing current will cause C_d to be charged more negatively during the next cycle, which will subsequently decrease the magnetizing current. This automatic reset mechanism eliminates the need for an external reset circuit.

The performance of the forward ZVS-MRC is shown in Fig. 1-9.

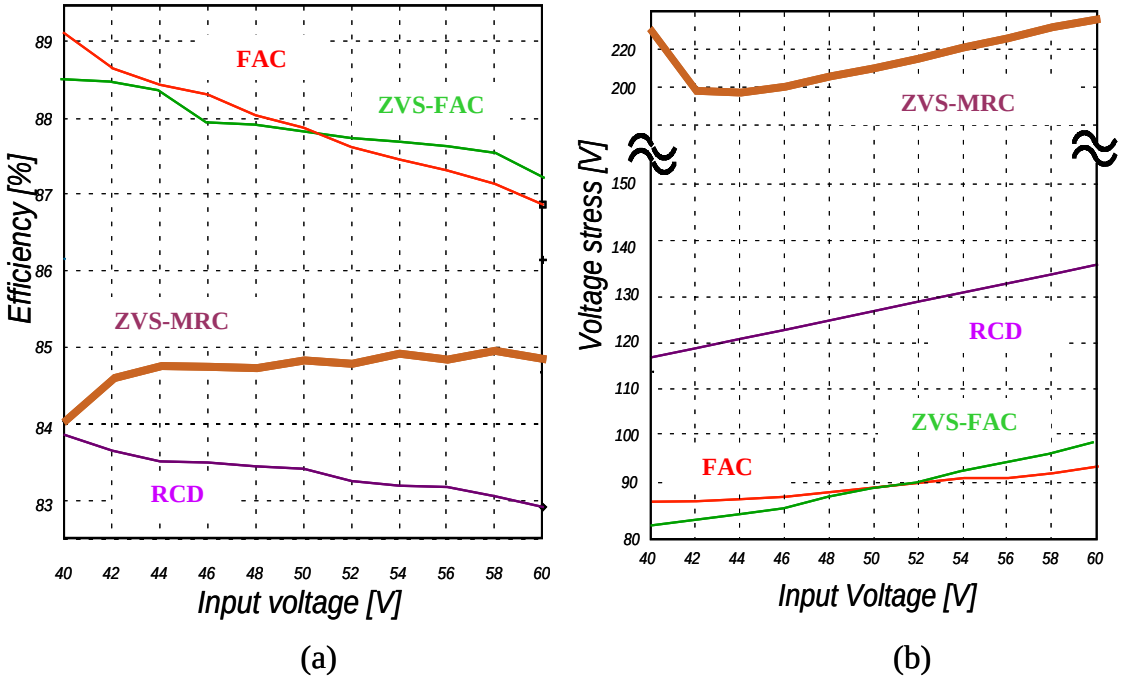


Fig. 1-9 Comparisons of the (a) measured efficiency (b) measured voltage stress of the RCD, the FAC, the ZVS-FAC, and the ZVS-MRC.

Although it operates with zero-voltage switching, the efficiency is not good enough to be compared to the FAC for the following reasons.

1. The presence of the circulating currents, which are caused by the resonance due to the resonant capacitor on the secondary side, results in power dissipation in the transformer and MOSFET.

2. The voltage stress on the MOSFET is higher than in PWM converters resulting in an increased conduction loss.

Also, another disadvantage is the constant off-time control that makes it difficult to optimize the magnetic components.

1.2.5. Clamp-Mode ZVS-MRC

Fig. 1-10 shows the circuit schematic of the clamp-mode forward ZVS-MRC [17]. By employing a soft-switching, non-dissipative active clamp network, the performance of the ZVS-MRC can be significantly improved. The clamping action is obtained by placing a series combination of an active switch and a capacitor in parallel with the power MOSFET, so that the voltage across the main switch is clamped to a lower value as shown in Fig. 1-11. The proposed clamping switch also operates with zero voltage by allowing its anti-parallel diode to conduct before turn-on. Due to the lower voltage stress, the clamp-mode forward ZVS-MRC is more efficient than the MRC.

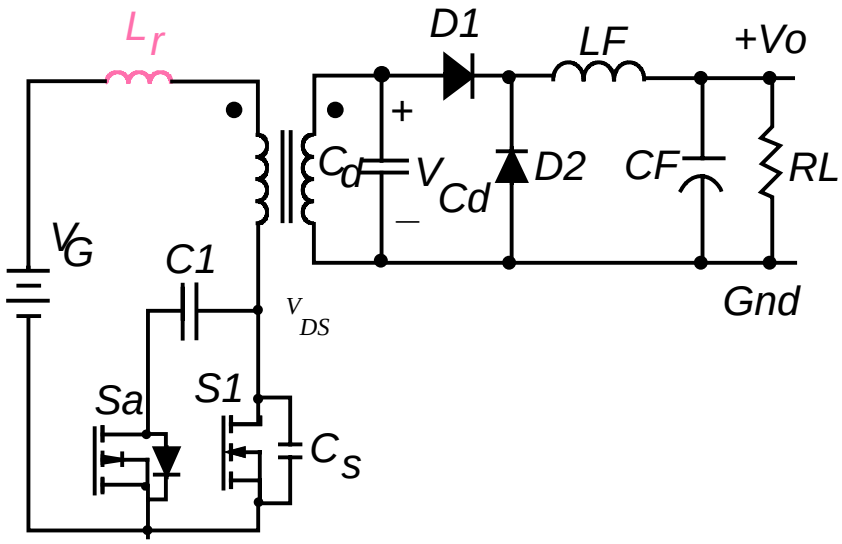


Fig. 1-10 Circuit diagram of the clamp-mode ZVS-MRC.

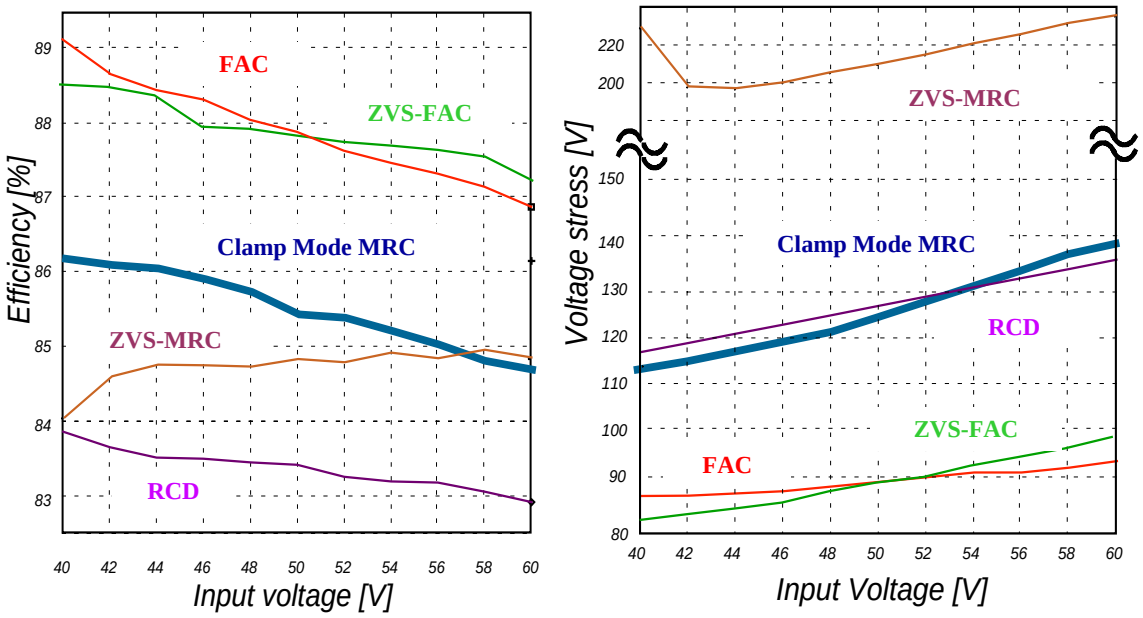


Fig. 1-11 Comparisons of the (a) measured efficiency (b) measured voltage stress of the RCD, the FAC, the ZVS-FAC, the ZVS-MRC, and the clamp-mode ZVS-MRC.

1.2.6. Comparison Summary

Because the single-switch forward converters proposed in the existing literature are focused on solving some of the problems inherent in the forward converter, such as core saturation, voltage spike, and switching loss problems, the voltage stress and converter efficiency become key values to be compared for impact on performance and has been detailed in [14]. Please refer to Fig. 1-11, which is the summary of the performance comparison.

The RCD has the lowest efficiency due to the dissipation of the leakage energy. The conventional MRC experiences the highest voltage stress on the main switch (up to four times the input voltage). Although it is operated in ZVS, the increased conduction losses make the efficiency of the conventional MRC not very high. In contrast, the FAC has the best performance: the lowest voltage stress and the highest efficiency.

Consequently, it is used as a benchmark in this research. The advantages of the FAC are as follows.

1. No additional reset winding or dissipative clamps are required for transformer reset;
2. Higher maximum duty cycle allows wider input voltage range or higher turns ratio resulting in significant reduction in current stresses on the primary side and voltage stresses on the secondary side;
3. The leakage energy can be stored and recycled, resulting in higher efficiency and lower noise;
4. Switch voltage is clamped to a controlled level resulting in lower stress switching devices;
5. The voltage stress across the switches is relatively constant over the full range of input voltage, which is not available in other single-ended implementations due to the switch voltage stress being proportional to the input voltage.
6. The transformer waveforms allow easy implementation of the synchronous switching technique on the secondary side.

However, the FAC requires more components, an additional high-voltage MOSFET clamp switch and an isolated variable-duty-cycle gate drive, rather than the other forward topologies to achieve the advantages listed above.

Recently, it has been widely reported that there will be problems in the FAC if the converter is not properly designed [21] -[24].

Thorough analysis and design trade-offs can be found in [25], but the key problems are briefly described below.

1.3. Problems of the Forward Converter with Active Clamp (FAC)

The dynamic behavior of the FAC could cause excessive switch voltage stress, transformer saturation, or active clamp switch diode reverse recovery problems if it is not correctly designed [25].

Specifically, before the input-voltage transient, the FAC converter operates with a large duty cycle and with a balanced flux in the core so that $V_G \cdot D = V_{C1}(1-D)$. Since the duty cycle and the clamp capacitor voltage V_{C1} do not change instantaneously after the line change, the volt-second product becomes unbalanced, i.e. $V_G \cdot D > V_{C1}(1-D)$. As a result, the magnetizing current of the transformer starts to increase after the input-voltage change. The increased magnetizing energy charges the clamp capacitor, increasing the clamp-capacitor voltage. This transition continues until V_{C1} becomes large enough so that the volt-second product becomes $V_G \cdot D < V_{C1}(1-D)$, and the magnetizing current of the transformer starts to decrease. The described clamp-capacitor voltage increase and the subsequent decrease after the transient can be seen as an oscillatory response of the resonant circuit consisting of the clamp capacitor and the magnetizing inductance of the transformer.

In addition to an excessive voltage stress on the primary switch and/or saturation of the core of the transformer, the body diode of auxiliary switch S_a may conduct due to a positive magnetizing current at the instant when main switch S_1 is turned on. Consequently, the failure of the converter may occur due to a low-impedance current path through the clamp capacitor, the auxiliary-switch body diode, and the main switch.

Moreover, there is an opposite effect with respected to the bandwidth of the control during the load and line transients as illustrated in Fig.1-12(a) - (b) and Fig.1-12(c) - (d), respectively. The bandwidth of the control, f_c, is increased from 830 Hz to 12 KHz in both cases. During the line transient, a larger f_c has smaller current stresses and voltage stress; while in load transient, a smaller f_c has smaller current stresses and voltage stress. Consequently, it becomes an uncertain condition to select proper design parameters.

As a result, the design issues become complicated and an optimal performance of the FAC is hard to achieve. Without providing a clear design guideline, the industry often uses a trial-and-error iteration process in the design of the FAC. This can be time-consuming and increase cost.

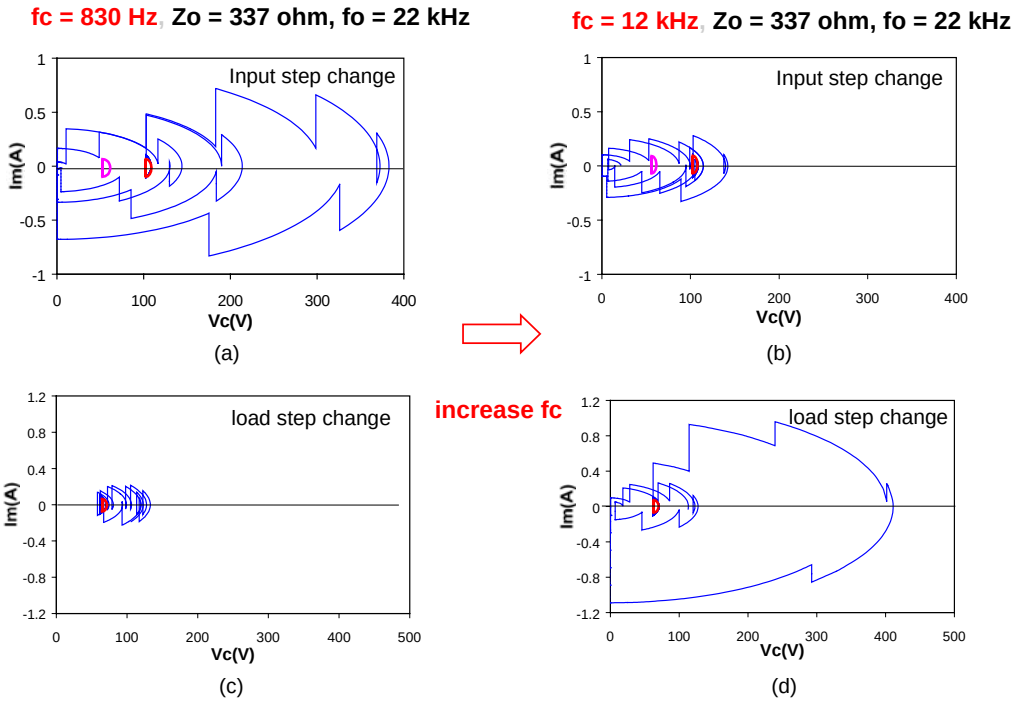


Fig.1-12 Effect of bandwidth of the close loop control, fc. In line transient, a larger fc has smaller current stresses and voltage stress; in load transient, a smaller fc has smaller current stresses and voltage stress /courtesy of Q. Li [25].

1.4. Objectives of the Dissertation

In addition to the voltage stress and converter efficiency, valuable information with respect to the leakage inductance can be obtained from the evaluation of the tested forward converters.

With a resonant power conversion technique, such as the MRC, the circuit requires inductance and capacitance so that the leakage inductance of the transformer can enhance rather than detract from circuit performance.

On the contrary, the leakage inductance energy is either dissipated in the RCD or recycled to the input source in the FAC. Consequently, the leakage inductance is intentionally minimized in the PWM power conversion technique so that it will not degrade the circuit performance.

To date, however, no one has claimed that a single-switch forward converter is able to enhance the converter performance in the PWM power conversion technique by utilizing the leakage inductance. Therefore, it is necessary to research the utilization of the transformer's leakage inductance in the PWM forward converter. This work proposes two techniques, input current ripple reduction and an embedded filter, to enhance performance of the forward converter using PWM technique.

By inserting a capacitor between two primary windings of the TFC, an input current ripple reduction technique is proposed and a forward converter with ripple reduction (FRR) is presented in this research work. Because the voltage of the capacitor is clamped to the input voltage, the capacitor becomes a second voltage source to share part of the load current. As a result, the input current ripple is reduced. Moreover, the capacitor voltage is clamped both at the static and dynamic states, and the excessive voltage stress

on the main switch S_1 of the FAC during the low-line to high-line step transient is eliminated.

Furthermore, without an external LC filter, the EMI noise levels can be further reduced as the result of the embedded notch filter formed by the transformer leakage inductance and clamp capacitor if the notch frequency is designed at the switching frequency. With the help of the clamp capacitor, therefore, the leakage inductance can enhance rather than detract from the converter performance.

The current ripple can be further reduced by employing the proposed techniques. Two sets of the clamp capacitor and the leakage inductance are utilized and the current ripple can even be cancelled if the condition is met. Consequently, input current becomes a non-pulsating waveform and a forward converter with ripple cancellation (FRC) is presented. Moreover, without an external LC filter, the EMI noise levels can be further attenuated as a result of the embedded low-pass filter formed by the transformer leakage inductances and clamp capacitors. Again, the leakage inductance can enhance the converter performance like the resonant converter.

In addition to providing the analysis and design procedure, the performance of the presented converters, the FRR and the FRC, are verified with the experimental results.

By employing the proposed techniques, eight new topologies have been extended for different power conversion applications. Each member of the FRR and the FRC families is able to enhance the converter performance by doing such things as the eliminating the voltage spikes on the main switch without a snubber circuit and improving the EMI performance with reduced filter components. Consequently, the cost and the space of the converter can be reduced.

The major objectives of this dissertation are as follows.

1. To reduce voltage stress, V_{DS}, on the main switch S_1 of the FAC during large signal transient.

   Among the existing forward converters, the FAC has been regarded to be the best topology. However, it requires an additional high-voltage MOSFET clamp switch and isolated variable-duty-cycle gate drive circuitry which is not necessary with the other forward topologies. Furthermore, the dynamic behavior of the FAC could cause excessive switch voltage stress, transformer saturation, or active clamp switch diode reverse recovery problems if it is designed improperly. Additionally, the opposite impact on the control bandwidth during the line and load transients can confuse the designer. As a result, the design issues become complicated and optimal performance of the FAC is hard to achieve. Without providing a clear design guideline, the industry often uses a trial-and-error iteration process in the design of the FAC. This can increase time spent designing as well as the cost.

   An important research objective, therefore, is to explore an effective solution to eliminate the above-mentioned drawbacks of the FAC.

2. To reduce the pulsating input current ripple of the forward converter.

   Due to the fact that there is a pulsating input current in the PWM forward converters, an external LC filter must be added. Consequently, some of the limited space is occupied and the cost is increased. In addition, the temperature rise in the filter capacitor due to a larger RMS current affects reliability.

It is important, therefore, to reduce the input current ripple by utilizing the proposed input current ripple reduction and embedded filter techniques to enhance the converter performance without an external LC filter.

3. To achieve a non-pulsating input current ripple of the forward converter without an external LC filter.

   Therefore, it is important to take full advantage of the proposed techniques to cancel input current ripple so that a non-pulsating input current can be obtained and the performance of the EMI can be further improved without an external LC filter.

4. To extend the power converter topology for different power conversion applications.

   Since the pulsating current occurs at the input port of the PWM buck and buck-derived converter, it would be useful to employ the proposed techniques to derive the topology extensions for different power conversion applications.

The overall objective of this dissertation is to explore an effective solution that incorporates the two proposed techniques, input current ripple reduction and embedded filter, to enhance the converter performance. This would result in new converter topologies that would cost less while performing better.

1.5. Dissertation Organization

This dissertation consists of five chapters. In Chapter 1, several types of forward converter are discussed and compared as the background of the research. Several issues such as the core reset, voltage stress, and the accompanying loss are investigated. Among the five tested forward converters, the forward converter with active clamp (FAC) performances best and is taken as the benchmark of the current research work.

However, several problems occur in the FAC during a large signal transient. To explore a solution to alleviate the problems of the FAC becomes the motivation of the current research work. Two families of the forward converter are presented to reach this end.

In Chapter 2, two techniques, input current ripple reduction and an embedded filter, are proposed and a forward converter with current ripple reduction (FRR) is presented as the entry-level topology to achieve the research objectives listed above. The operational principle and the features of the topology are described. By utilizing the SABER simulation program, several performance comparisons between the FRR and the FAC are made. The performance of the presented converter is verified with experimental results.

In Chapter 3, by fully taking advantage of the techniques proposed in Chapter 2, a forward converter with current ripple cancellation (FRC) is presented to further improve the converter performance. The operational principle and the features of the FRC are described. In addition, the experimental results are presented.

In Chapter 4, several extended topologies of the FRR and FRC are presented. These were created by employing the proposed techniques to enhance the converter performance for different power conversion applications. Moreover, by using a bilateral inversion technique, both ripple reduction and embedded filter techniques can be applied to the isolated PWM boost converter. The output current ripple is thus reduced, and size reduction of the output capacitor is attainable.

The conclusions and the suggestions for the future works are given in Chapter 5.

Chapter 2 Forward Converter with Current Ripple Reduction (FRR)

2.1. Introduction

Several forward converters have been proposed to solve some of the problems inherent with this forward topology, such as core saturation, voltage spike, and switching loss. Among the forward converters proposed in the literature, the FAC has gained widespread acceptance for many low-to-medium power DC/DC converter applications due to its high efficiency and having the lowest voltage stress.

However, the FAC requires more components, an additional high-voltage MOSFET clamp switch and an isolated variable-duty-cycle gate drive, which the other forward topologies to achieve the advantages listed above do not.

Recently, it has been widely reported that there will be problems with excessive voltage over the switch, diode reverse-recovery problems of the body diode of the clamp switch, or transformer core saturation due to large signal transients if the converter is not properly designed [21] -[24].

As a result, the design issues become complicated and optimal performance of the FAC is hard to achieve. Without a clear design guideline, a trial-and-error iteration process is often used by the industry in the design of the FAC. This can increase the time spent and the cost of the design process.

Furthermore, there is a common characteristic of the buck and buck-derived converters; the input current waveform is a pulsating waveform. The problems caused by

this pulsating input current are usually solved by adding an external LC filter. Not only can these filters occupy some of the limited space, but this solution also increases the cost of the converter.

In addition to eliminating the excessive voltage stress of the FAC during the large signal transient, at the same time a comprehensive solution should be able to alleviate the problems caused by both the transformer leakage inductance and the pulsating input current ripple. By utilizing the clamp capacitor and the transformer leakage inductance, two techniques, input current ripple reduction and embedded filter, are thus proposed to enhance the performance of the PWM forward converter.

2.2. Proposed Techniques: Input Current Ripple Reduction and Embedded Filter

Two techniques: input current ripple reduction and an embedded filter, are proposed by utilizing the clamp capacitor and the transformer leakage inductance in this research work so that the performance of the PWM forward converter can be enhanced.

By inserting a capacitor between two primary windings of the TFC (Fig. 2-1(a)), an input current ripple reduction technique is proposed and a forward converter with ripple reduction (FRR) is illustrated in Fig. 2-1(b). In contrast to the TFC (Fig. 2-1(c)), the proposed technique can absorbed the energies of the transformer leakage inductances, L_1 and L_3, when the main switch S_1 is turned off. As a result, the voltage spikes on the main switch is eliminated as illustrated in Fig. 2-1(d).

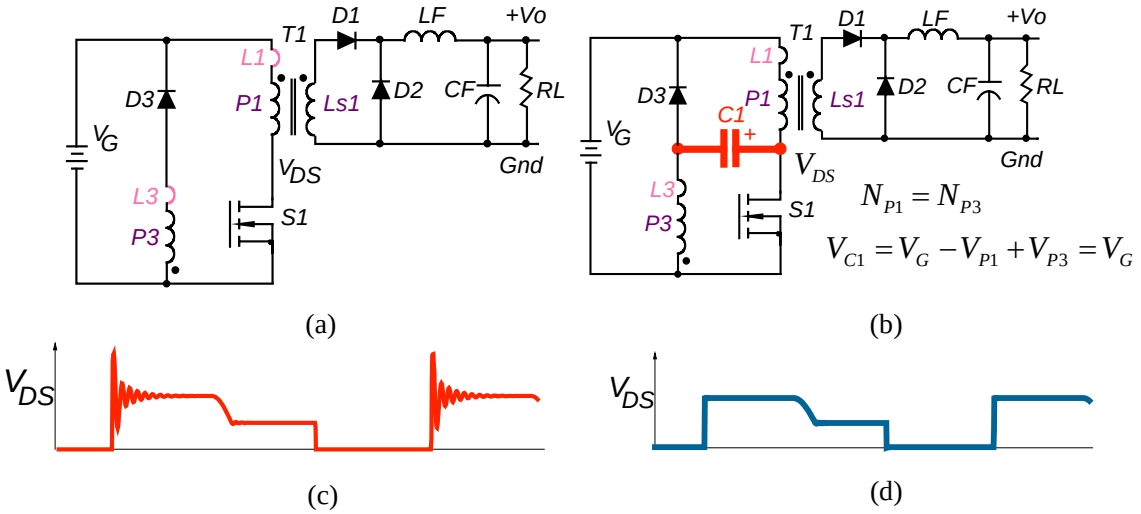


Fig. 2-1 Circuit diagrams of (a) the TFC, (b) the FRR, V_{DS} of (c) the TFC, and (d) the FRR.

As illustrated in Fig. 2-2(a), the primary windings P_1 and P_3 have the same number of turns resulting in the following equation is valid during the off time interval.

$$|V_{P1}| = |V_{P3}| \qquad \text{Eq. 2-1}$$

Due to the opposite parity of P_1 and P_3, therefore, the capacitor voltage V_{C1} is charged and clamped to input voltage, V_G, as derived in the following equation.

$$V_{C1} = V_G - V_{P1} + V_{P3} = V_G \qquad \text{Eq. 2-2}$$

This is different from the other capacitor voltage clamp schemes; for example, the capacitor voltage of the FAC is governed by the volt-second of the transformer as expressed in the following equation.

$$V_{C1} = \frac{DV_G}{1-\mathrm{D}} = \frac{nV_O}{1-D} \qquad \text{Eq. 2-3}$$

Therefore, the capacitor voltage is the function of the operating duty cycle as well as the input voltage.

Referring to Eq. 2-2, on the other hand, the capacitor voltage of the proposed technique is clamped to input voltage and it is able to quickly track the input voltage change both at the static and the dynamic transient states as illustrated in **Fig. 2-2**(b) through **Fig. 2-2**(e).

Therefore, the excessive voltage stress on the main switch S_1 of the FAC during low-line to high-line step transient is eliminated.

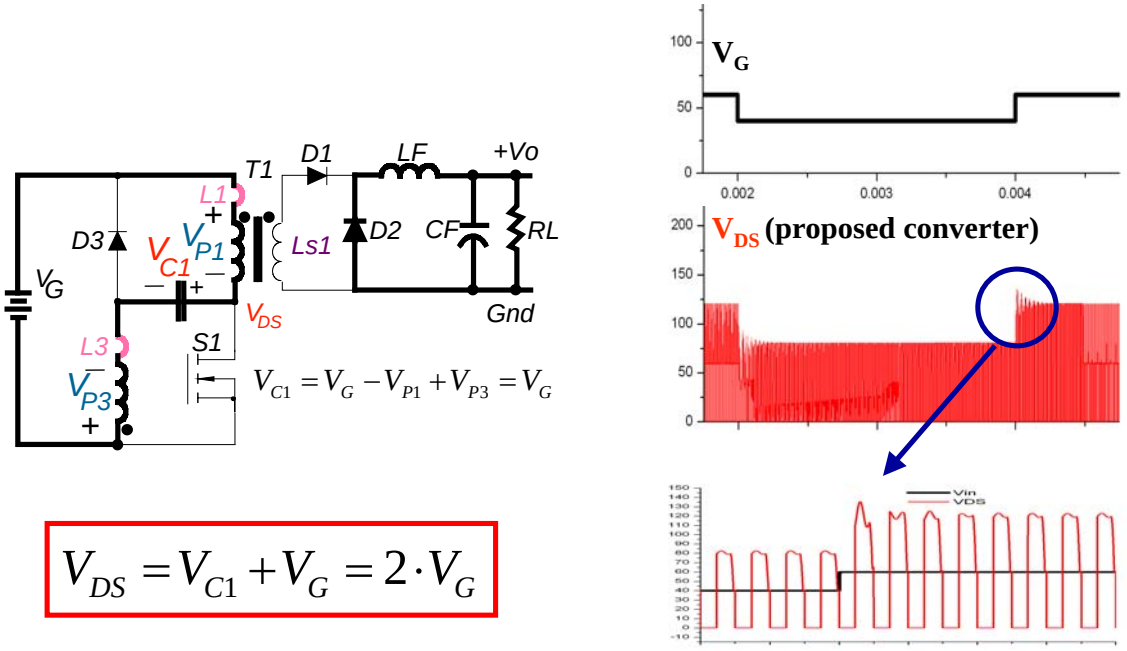


Fig. 2-2. (a) Circuit diagram of the FRR (b) input-voltage step change from 40 V to 60 V, (c) V_{DS} waveform during the transient (L_1 = L3 = 540nH, C_1=20.9uF). (d) zoom in V_{DS} waveform.

Due to V_{C1}=V_G, the load currents are thus provided by the V_G via L_1 and V_{C1} via L_3 when the main switch is turned on as illustrated in Fig. 2-3. Accompanied with the transformer leakage inductance, the input current ripple can be reduced. The leakage inductance plays a key role in reducing the input current ripple at the main switch turn on instant. The load current flows through the main switch S_1 and the input current ripple, Δi_G , and capacitor current ripple, Δi_{C1}, are derived as the following equations.

$$\Delta i_{S1} = \frac{i_O}{n} = \Delta i_G + \Delta i_{C1} \qquad \text{Eq. 2-4}$$

$$\Delta i_G = \frac{V_G}{L_1}\Delta t = \frac{L_3}{L_1 + L_3}\frac{i_O}{n} \qquad \text{Eq. 2-5}$$

$$\Delta i_{C1} = \frac{V_G}{L_3}\Delta t = \frac{L_1}{L_1 + L_3}\frac{i_O}{n} \qquad \text{Eq. 2-6}$$

where i_O is the load current and n is the transformer turns ratio.

The current ripple distribution is dependent on the ratio of the leakage inductances L_1 and L_3 derived from Eq. 2-5 and Eq. 2-6 and expressed in the following equation.

$$\Delta i_G : \Delta i_{C1} = L_3 : L_1 \qquad \text{Eq. 2-7}$$

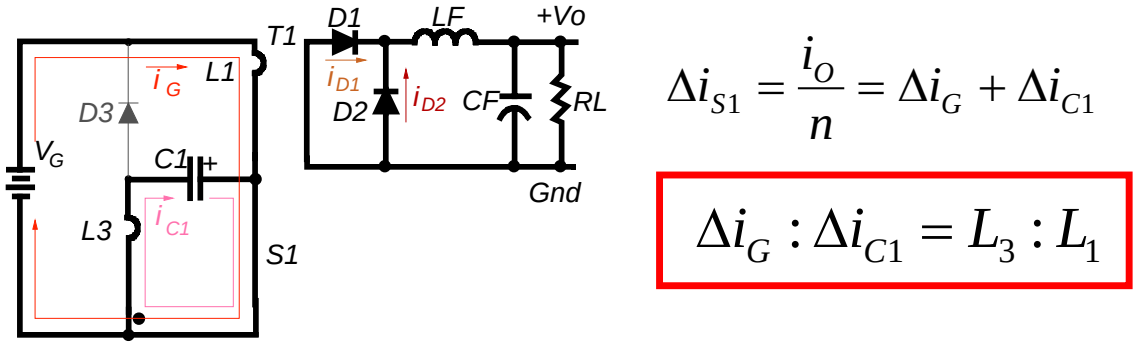


Fig. 2-3 Circuit diagram of the proposed converter and the current ripple distribution of the currents i_G, i_{C1}, and i_{S1}.

In addition to proposing the input current ripple reduction technique, there is an embedded notch filter technique that can be applied to the PWM forward converter so that the EMI performance can be enhanced.

The embedded notch filter technique is illustrated in Fig. 2-4. The derivation begins with shifting the voltage clamp network S_1-C_1-D_3 from Fig. 2-4(a) and the equivalent circuit can be obtained as shown in Fig. 2-4(b). Next, the components are clockwise relocated from P_3-L_3-C_1 to C_1-L_3-P_3. Due to the fact that they have the same

number of turns and polarity, the transformer primary windings, P_1 and P_3, can be connected in parallel, as shown in Fig. 2-4(c). Finally, P_3 is merged into P_1 and the circuit of the FRR is equivalent to a filter cascading with a forward converter as shown in Fig. 2-4(d).

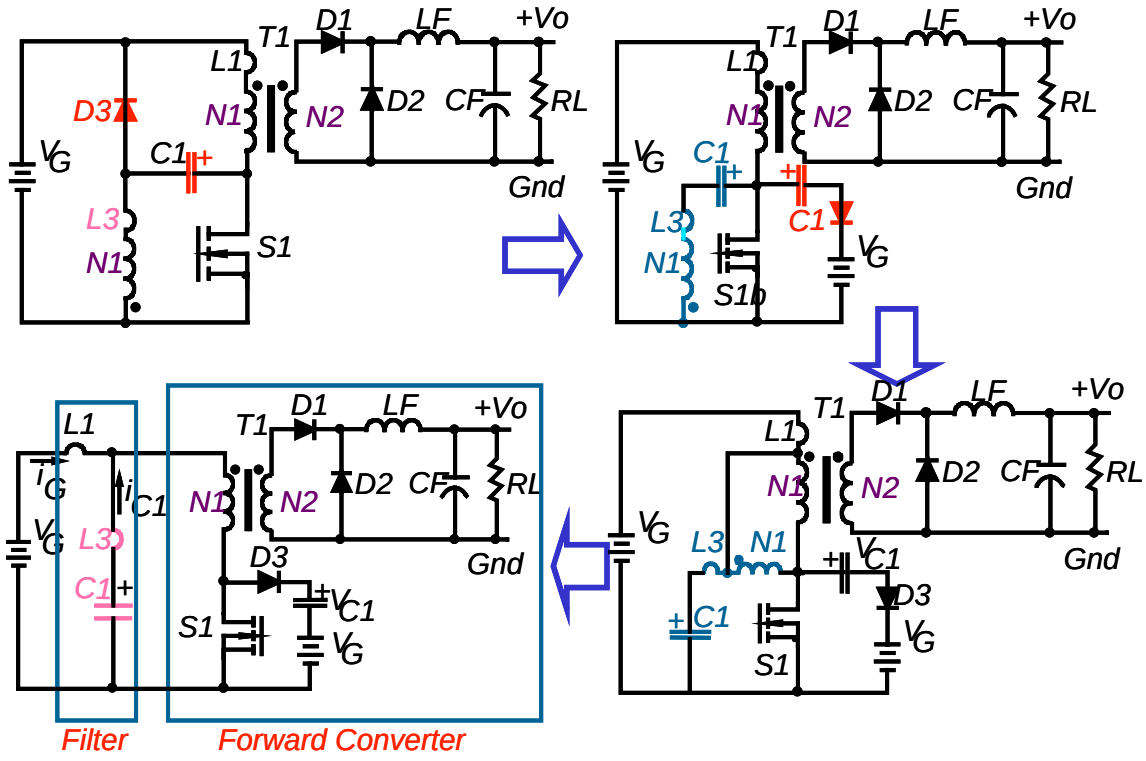


Fig. 2-4. Evolution of the embedded notch filter technique.

Consequently, without an external LC filter, the EMI noise levels can be further reduced as the result of the embedded notch filter formed by the transformer leakage inductance and clamp capacitor, if the notch frequency is designed to be the same as the switching frequency. With the help of the clamp capacitor, therefore, the leakage inductance can enhance rather than detract from the converter performance.

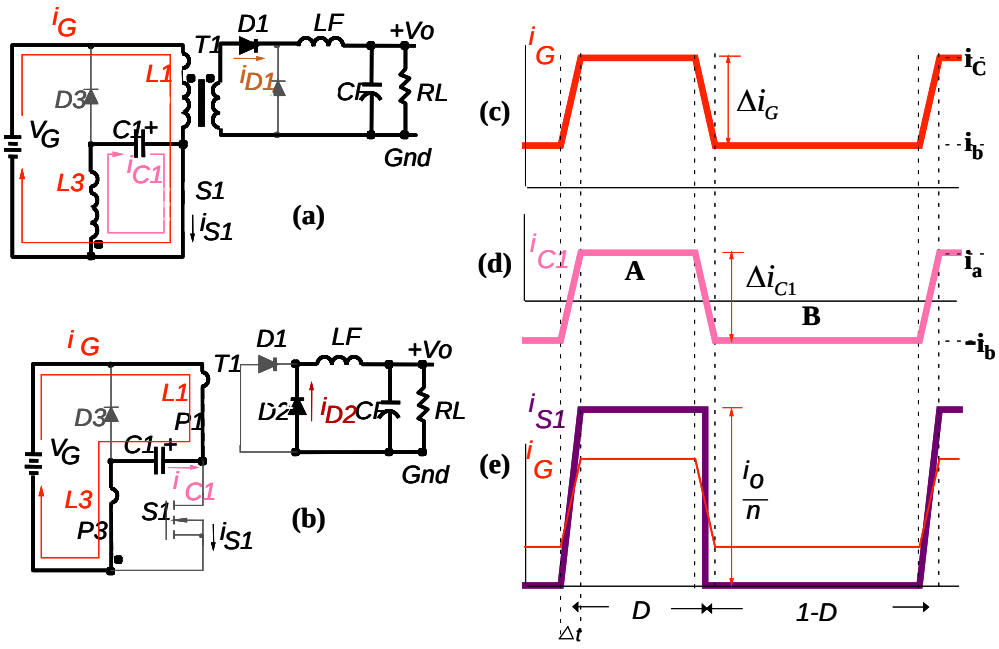
2.3. Steady State Analysis

Three key current waveforms, switch current i_{S1}, the input current i_G, and the clamp capacitor current i_{C1}, are quantified as the reference in introducing the operational principle.

The charge balance property of the clamp capacitor is utilized to explore the current ripple reduction feature of the FRR. Illustrated in Fig. 2-5(a) and Fig. 2-5(b) are the operational modes during the on time and the off time of the FRR. As shown in Fig. 2-5(c), Fig. 2-5(d), and Fig. 2-5(e), the switch current, i_{S1}, the input current, i_G, and the clamp capacitor current, i_{C1}, and their current levels are labeled with i_a, i_b, and i_c during different operating times. In addition, the current ripple distribution between the input source and the clamp capacitor are represented with Δi_G and Δi_{C1}.

Assuming $i_{mag} << i_O$, where i_o is the load current, and i_{mag} is the magnetizing current, the load current is the same as the current that flows through the main switch i_{S1} during the S_1 turn-on time interval with the following equation.

$$i_G + i_{C1} = i_{S1} = \frac{I_o}{n} \qquad \text{Eq. 2-8}$$



$$i_{S1}=i_G+i_{C1}$$

Fig. 2-5. Operational modes of the FRR during (a) the on time and (b) the off time, key current waveforms (c) input current I_G, (d) capacitor current I_{C1} with its charge balance operation, A=B, (e) switch current I_{S1}, $I_{S1}=I_G+I_{C1}$.

During the S_1off time interval, the following equation applies.

$$i_G + i_{C1} = i_{S1} = 0 \qquad \text{Eq. 2-9}$$

The current levels, i_a, i_b, and i_c can be quantified by employing the charge balance of the capacitor and the Faraday law.

C_1 is discharged to the load with i_a during the on time interval and charged by the input source with i_b during the off time interval.

Applying the charge balance, A=B, as illustrated in **Fig. 2-5** (d),

$$i_a \cdot D = i_b \cdot (1-D) \qquad \text{Eq. 2-10}$$

At the turn-on instant, i_G and i_{C1} are linearly charged by the input voltage and the clamp capacitor voltage.

$$\Delta i_{C1} + \Delta i_G = \frac{i_O}{n} \quad \text{Eq. 2-11}$$

$$i_c - i_b = \Delta i_G = \frac{L_3}{L_1 + L_3}\frac{i_O}{n} \quad \text{Eq. 2-12}$$

$$i_a + i_b = \Delta i_{C1} = \frac{L_1}{L_1 + L_3}\frac{i_O}{n} \quad \text{Eq. 2-13}$$

According to Eq. 2-12, the input current ripple value is reduced to ($\frac{L_3}{L_1 + L_3}\frac{i_O}{n}$) in the FRR. Comparing to the FAC, the current ripple reduction is with the ratio of ($\frac{L_3}{L_1 + L_3}$). Referring to Eq. 2-12 and Eq. 2-13, the current ripples Δi_G and Δi_{C1} are strongly dependent on the ratio of the L_1 to L_3. The larger the L_1 to L_3 ratio is, the smaller the input current ripple value Δi_G will be, resulting in a reduction of the EMI intensity. However, a larger L_1 to L_3 ratio would increase the RMS current of the clamp capacitor and the voltage stress of the main switch. Moreover, an external inductor would be needed or a special winding scheme should be applied in the construction of the transformer.

From Eq. 2-10 and Eq. 2-13, i_a and i_b can be derived as the following equations.

$$i_a = \frac{L_1(1-D)}{(L_1 + L_3)}\frac{i_O}{n} \quad \text{Eq. 2-14}$$

$$i_b = \frac{DL_1}{(L_1 + L_3)}\frac{i_O}{n} \quad \text{Eq. 2-15}$$

From Eq. 2-12 and Eq. 2-15, i_c is derived as the following equation.

$$i_c = i_b + \Delta i_G = \frac{DL_1 + L_3}{(L_1 + L_3)}\frac{i_o}{n} \quad \text{Eq. 2-16}$$

2.4. Operational Principle of the FRR

The circuit diagram and key waveforms of the forward converter with current ripple reduction (FRR) are shown in Fig. 2-6. The primary side of the power stage consists of a switch, S_1, one clamp capacitor, C_1, one-clamped diode, D_3, and one transformer. The transformer is comprised of two identical primary windings, P_1 and P_3, and one secondary winding, L_{S1}, with the turns ratio of (n : n : 1). L_1 and L_3 are represented as the leakage inductance of P_1 and P_3, respectively. To simplify the analysis, the output filter inductance is assumed to be sufficiently large to be approximated by a current source with the value equal to the output current, I_O. The clamp capacitor, C_1, is assumed to be sufficiently large that the voltage across it can be assumed to be constant. Also, $i_{mag} << i_O$, and $f_o = \frac{1}{2\pi\sqrt{L_3 C_1}} << f_S$ are assumed, where I_o is the load current I_{mag} is the magnetizing current, and f_0 is the natural frequency defined by L_3 and C_1. During steady-state operation, five operation stages exist within one switching cycle (shown in Fig. 2-7(a)-(e)):

(a) T_0-T_1:

The circuit operation begins with the switch off at T_0. Prior to T_0, the power is transferred from the input source, V_G, and the energy is stored in capacitor C_1. i_{C1} provides part of the load current via P_3, while i_G provides the complementary part of the load current via P_1 so that their sum is equal to the reflected load current. According to Eq. 2-14 and Eq. 2-16,

At T_0, $i_G = i_{L1,}$ $i_{C1} = i_{L3}$ *and* $i_{Mag} << i_o$,

$$i_G + i_{C1} = \frac{i_O}{n} \quad \text{Eq. 2-17}$$

After S_1 turns off at T_0, transformer windings P_1, P_3 and L_{S1} are shorted due to the turning on of D_1 and D_2. Consequently, both leakage inductances L_1 and L_3 are supplied by a negative voltage and thus the currents, i_G and i_{C1}, are linearly decreased to the reflect load current interruption as the following equation.

During $T_0 < t < T_1$,

$$i_G = i_{L1} = i_c - \frac{V_G}{L_1}(t - T_0) \quad \text{and} \quad \text{Eq. 2-18}$$

$$i_{C1} = i_{L3} = i_a - \frac{V_G}{L_3}(t - T_0) \quad \text{Eq. 2-19}$$

When the voltage across the switch reaches $2V_G$, the clamp diode D_3 will be forced to turn on, and the voltage stress V_{DS} on switch S_1 will be clamped to $2V_G$. $-V_{C1}$ and $-V_G$ are thus applied on the windings P_1 and P_3 to start the core-reset function.

At T_1, D_1 is turned off because load current is freewheeled through diode D_2 and i_G and i_{C1} are expressed with following equations.

$$i_G = i_{L1} = i_b \quad \text{Eq. 2-20}$$

$$i_{C1} = i_{L3} = -i_b \quad \text{Eq. 2-21}$$

The time interval, T_1-T_0 can be calculated as

$$T_1 - T_0 = \frac{L_1 L_3}{V_G (L_1 + L_3)} \frac{i_o}{n} \quad \text{Eq. 2-22}$$

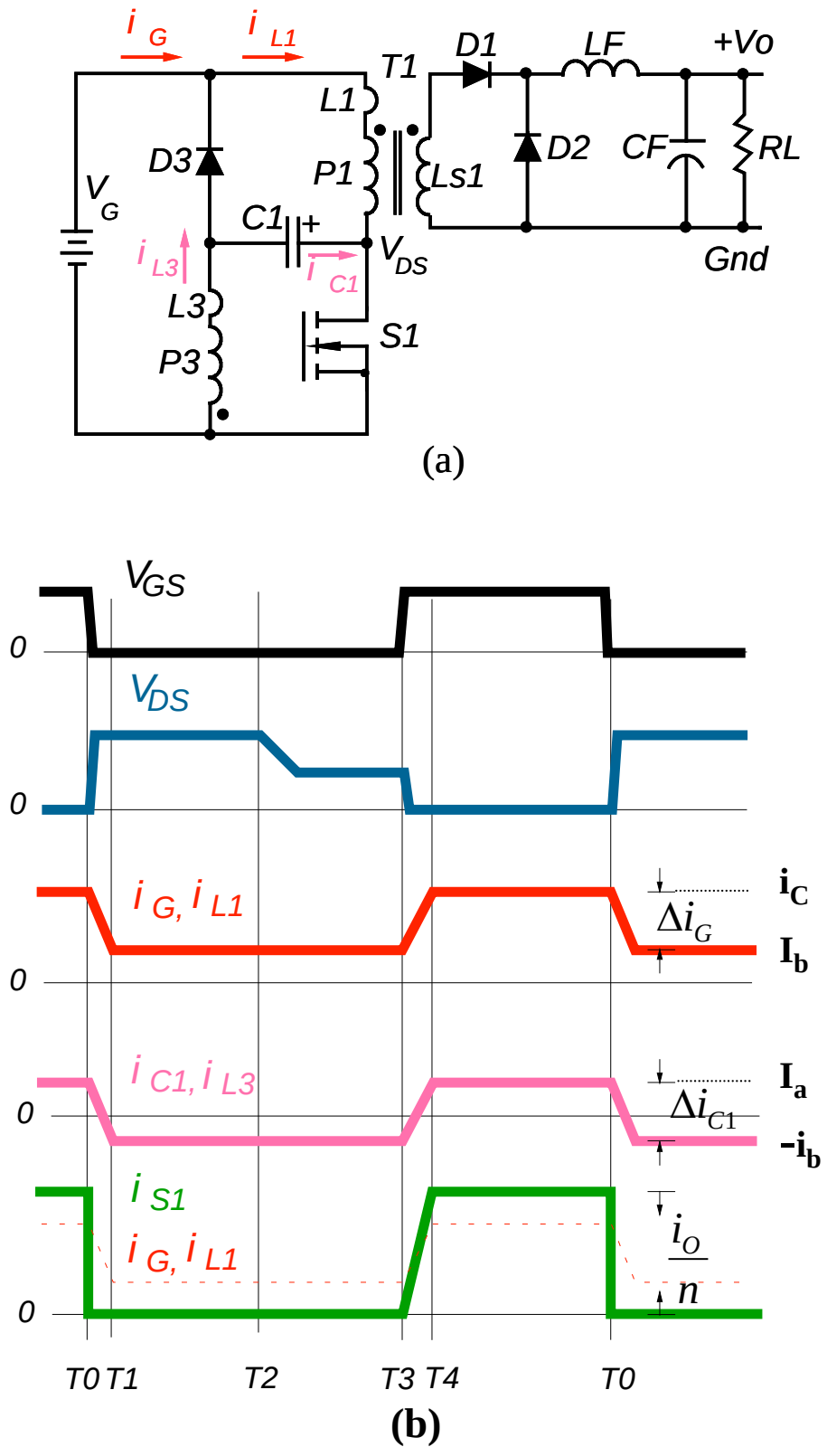


Fig. 2-6 (a) Circuit diagram and (b) key waveforms of the FRR.

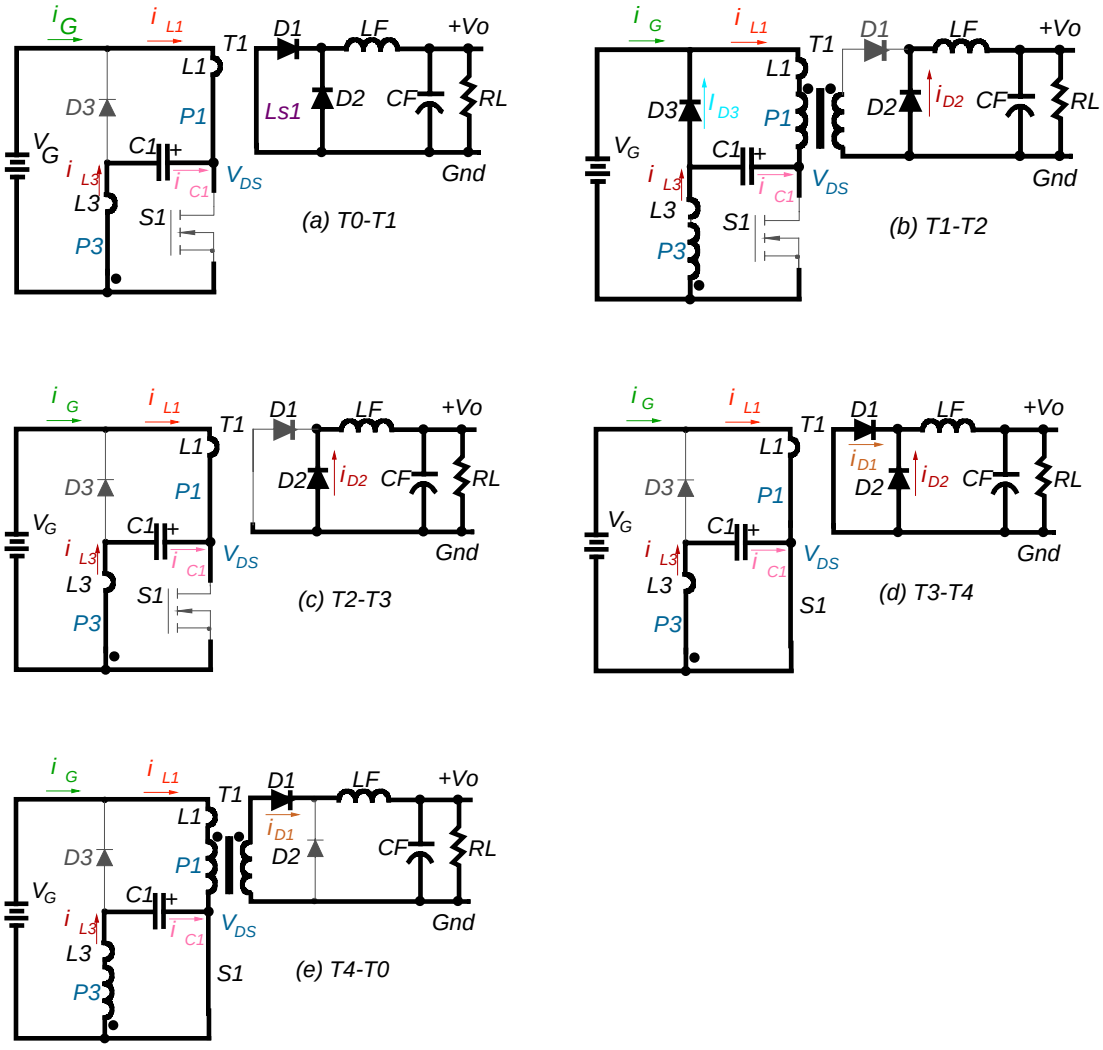


Fig. 2-7 Equivalent circuits of the operating stage of the FRR.

(b) T_1-T_2:

During this time period, the magnetizing current flows through D_3 to provide core reset of the transformer. The primary current i_G flows through L_1-P_1-C_1-L3-P3. Because the voltages across the windings P_1 and P3 cancel each other due to the presence of the opposite winding polarities, C_1 is charged by the input power

source, V_G. At T_2, the zero average-volt-second of the transformer is achieved and D_3 is turned off.

During $T_1 < t < T_2$, V_{DS} is clamped to $2V_G$.

$$V_{DS} = 2V_G \quad \text{Eq. 2-23}$$

The currents i_G and i_{C1} maintain the following relations.

$$i_G = i_{L1} = i_b = -i_{C1} = -i_{L3} \quad \text{Eq. 2-24}$$

(c) T_2-T_3:

During this time interval, V_{DS} is reduced in a resonant fashion due to the magnetizing inductance and the output capacitance of the MOSFET, S_1. V_{DS} will be clamped to V_G because the transformer windings are shorted due to the lack of magnetizing energy. C_1 is charged continuously and V_{C1} is clamped to V_G. Both the voltage stresses on the switch and clamp diode are clamped to the V_G. At T_3, the gate drive signal is applied to switching on the switch.

During $T_2 < t < T_3$, V_{DS} is clamped to V_G.

$$V_{DS} = V_G \quad \text{Eq. 2-25}$$

The currents i_G and i_{C1} maintain the following relations.

$$i_G = i_{L1} = i_b = -i_{C1} = -i_{L3} \quad \text{Eq. 2-26}$$

(d) T_3-T_4:

At T_3, the main switch S_1 is turned on. At T3, the currents maintain the following equations.

$$i_G = i_{L1} = i_b = -i_{C1} = -i_{L3} \quad \text{Eq. 2-27}$$

Due to the turning on of D_1 and D_2, transformer windings P_1, P3 and L_{s1} are shorted. Consequently, both leakage inductances, L_1 and L3, are supplied by a positive voltage and the currents i_G and i_{C1} are linearly increased to reflect the demand of the load current.

During $T_3 < t < T_4$ the currents, i_G and i_{C1}, are derived as the following equations.

$$i_G = i_{L1} = i_b + \frac{V_G}{L_1}(t - T_3), \text{ and} \quad \text{Eq. 2-28}$$

$$i_{C1} = i_{L2} = -i_b + \frac{V_G}{L_3}(t - T_3) \quad \text{Eq. 2-29}$$

At T_4,

$$i_G + i_{C1} = i_c + i_a = \frac{i_O}{n} \quad \text{Eq. 2-30}$$

D_2 is turned off. The time interval can be calculated as

$$T_4 - T_3 = \frac{L_1 L_3}{V_G (L_1 + L_3)} \frac{i_o}{n} \quad \text{Eq. 2-31}$$

The time interval, T_3-T_4, becomes the time delay between the time to turn on the MOSFET in the primary winding and the time to apply voltage on the secondary winding of the transformer. This time interval to the switching period is defined as the duty cycle loss in the converter operation. It will affect the load regulation resulting in reducing the converter efficiency.

(e) T_4-T_0:

The power is transferred from the input source, V_G, and V_{C1}. The input voltage is applied on winding P_1, and V_{C1} is applied on winding P3. Therefore, i_{C1} provides part of load current via P3 while i_G provides the complementary part of the load

current via P_1 so that their sum is equal to the reflected load current as the following equation.

$$i_G + i_{C1} = \frac{i_O}{n} \quad \text{Eq. 2-32}$$

At T_0, S_1 is turned off and another switching cycle begins.

2.5. Input Current Ripple Reduction

Without an effective solution, adding an external LC filter is used to solve the problems caused by the pulsating input current of the FAC. In contrast, the current ripple reduction feature of the FRR alleviates these problems. Before this research work, no single-switch forward converter had been proposed to be able to reduce the input current ripple without adding an external LC filter.

Eq. 2-12 and Eq. 2-13 are the equations of the input current ripple of the Δi_G and Δi_{C1}. Building on these equations, several key current and voltage values can be expressed in the following equations.

$$\Delta i_{S1} = (i_O / n) \quad \text{Eq. 2-33}$$

$$\Delta i_G = \frac{L_3}{L_1 + L_3} \frac{i_O}{n} \quad \text{Eq. 2-34}$$

$$\Delta i_{C1} = \frac{L_1}{L_1 + L_3} \frac{i_O}{n} \quad \text{Eq. 2-35}$$

$$\Delta i_{Cin} = \frac{L_3}{L_1 + L_3} \frac{i_O}{n} \quad \text{Eq. 2-36}$$

The clamp capacitor voltage ripple ΔV_{C1} can be calculated as the following equation.

$$\Delta V_{C1} = \frac{i_{C1} \cdot \Delta t}{C_1} = \frac{i_a \cdot DT_S}{C_1} \quad \text{Eq. 2-37}$$

Referring to Eq. 2-14, ΔV_{C1} can be calculated as the following equation.

$$\Delta V_{C1} = \frac{L_1(1-D)}{L_1 + L_3} \frac{i_O}{n} \frac{DT_S}{C_1} \quad \text{Eq. 2-38}$$

Assuming efficiency $\eta \cong 1$, $i_{in} = \frac{V_o i_o}{V_i}$, *and* $D = \frac{nV_o}{V_i} \Rightarrow i_{in} = \frac{Di_o}{n}$, the RMS current of i_{Cin} can be derived as the following equation.

During $0 < t < DT_S$,

$$i_{Cin} = i_G - i_{in} = \frac{L_3}{L_1 + L_3} \frac{i_O}{n}(1-D), \quad \text{Eq. 2-39}$$

During $DT_S < t < T_S$,

$$i_{Cin} = i_G - i_{in} = -\frac{L_3}{L_1 + L_3} \frac{Di_O}{n}, \quad \text{Eq. 2-40}$$

The RMS current can be calculated as the following equation.

$$i_{C1(RMS)} = \frac{L_1}{L_1 + L_3} \frac{i_O}{n} \sqrt{D(1-D)} \quad \text{Eq. 2-41}$$

$$i_{Cin(RMS)} = \frac{L_3}{L_1 + L_3} \frac{i_O}{n} \sqrt{D(1-D)} \quad \text{Eq. 2-42}$$

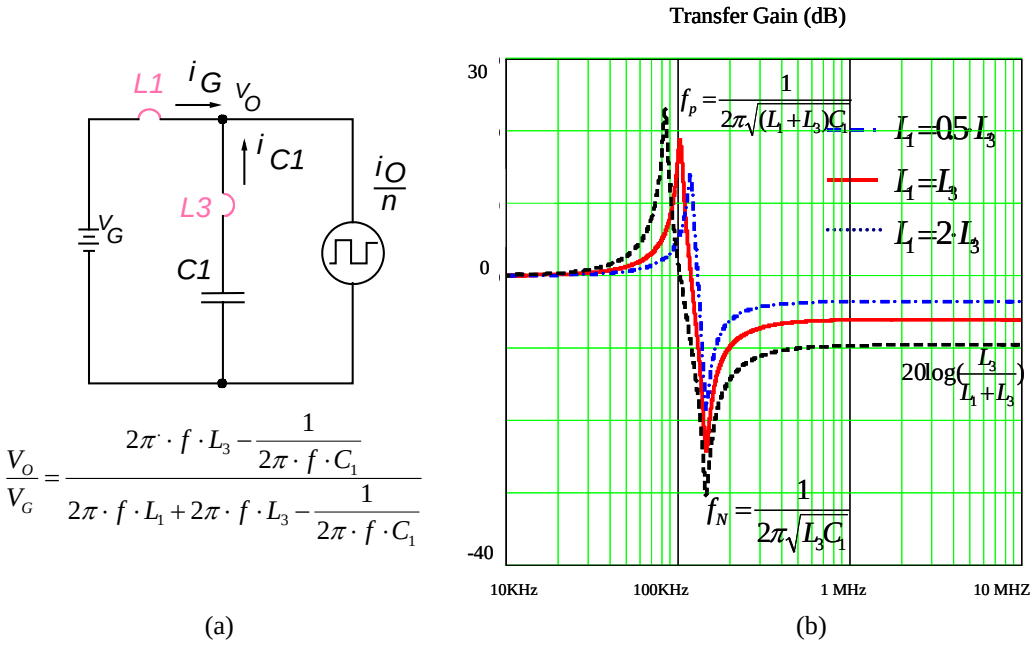
2.6. Embedded Notch Filter

To investigate the characteristics of the filter formed by the L_1, L_3, and C_1 as shown in Fig. 2-8(a), the transfer gain of the V_O/V_G is derived as the following equation.

$$\frac{V_O}{V_G} = \frac{2\pi \cdot f \cdot L_3 - \dfrac{1}{2\pi \cdot f \cdot C_1}}{2\pi \cdot f \cdot L_1 + 2\pi \cdot f \cdot L_3 - \dfrac{1}{2\pi \cdot f \cdot C_1}} \qquad \text{Eq. 2-43}$$

Three curves of the transfer gain with different ratios of L_1 to L_3 are plotted in Fig. 2-8(b). These figures show that there is one peak point at f_p, $f_P = \dfrac{1}{2\pi\sqrt{(L_1 + L_3)C_1}}$, and one valley point at f_N, $f_N = \dfrac{1}{2\pi\sqrt{L_3 C_1}}$, on each curve.

Because $L_1 \fallingdotseq L_3$ can be obtained without making additional efforts in the transformer construction, the design of the filter components (L_1, L_3 and C_1) is thus simplified to two components (L_1=L_3 and C_1) and two design equations are required to solve L_3 and C_1. Because the notch frequency is determined by $f_N = 1/(2\pi\sqrt{L_3 C_1})$, it can be utilized to design L_3 and C_1.



$$\frac{V_O}{V_G} = \frac{2\pi \cdot f \cdot L_3 - \dfrac{1}{2\pi \cdot f \cdot C_1}}{2\pi \cdot f \cdot L_1 + 2\pi \cdot f \cdot L_3 - \dfrac{1}{2\pi \cdot f \cdot C_1}}$$

(a) (b)

Fig. 2-8 (a) Equivalent circuit diagram of the FRR and (b) transfer gain of the notch filter with three different ratios of L_1 to L_3.

By utilizing the SABER program, the input current i_G of the FRR without employing the notch filter technique and with employing the notch filter technique are shown in Fig. 2-9 (a) and Fig. 2-9 (b), respectively. Although both cases have the same amplitude of the current ripple, the input current waveform with notch filter becomes a sinusoidal-like waveform instead of a trapezoidal shape. The fundamental component has a 20dBuv improvement as illustrated in Fig. 2-9(c). As a result, size reduction of the input filter can be achieved.

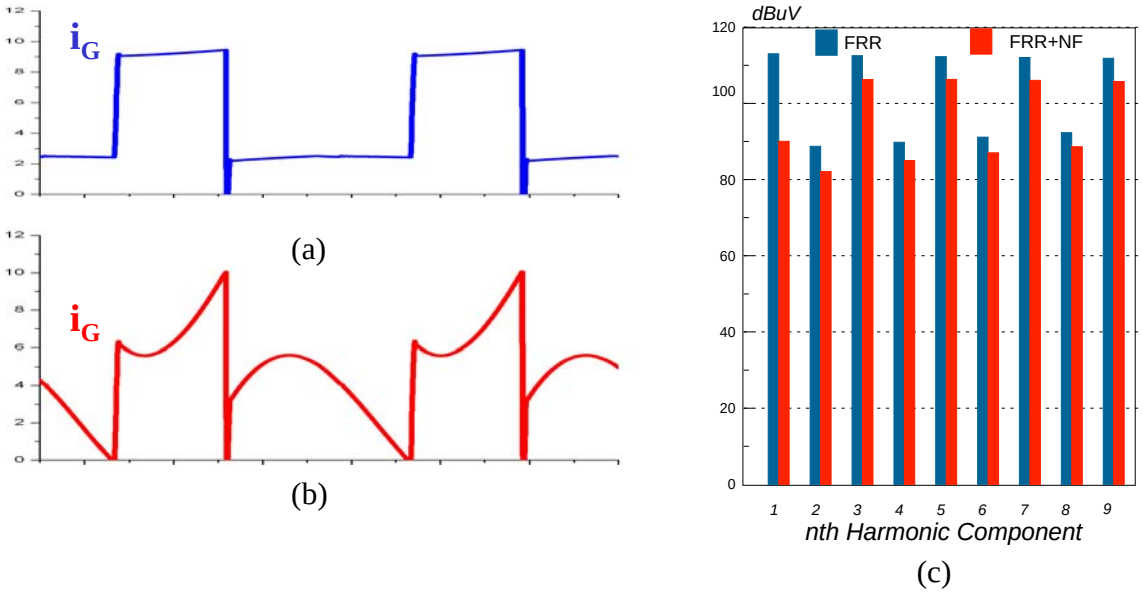


Fig. 2-9 Input current i_G of (a) the FRR without employing notch filter feature (b) FRR employing notch filter feature (c) comparison of the harmonic component of the two cases.

To obtain maximum attenuation, notch frequency can be designed to be at the switching frequency, as the following equation.

$$f_N = 1/(2\pi\sqrt{L_3 C_1}) = f_S \qquad \text{Eq. 2-44}$$

Additionally, the selection of the capacitor voltage can be calculated by utilizing the following equations.

$$V_{DS} = V_G + V_{C1} \qquad \text{Eq. 2-45}$$

$$V_{C1(\max)} = \mathrm{V}_{G1(AVG)} + \frac{1}{2}\Delta V_{C1} = V_G + \frac{L_1}{2(L_1 + L_3)}\frac{(1-D)D \cdot i_O}{n \cdot C_1 \cdot f_S} \quad \text{Eq. 2-46}$$

$$\mathrm{V}_{DS} = \mathrm{V}_G + V_{C1} = 2\mathrm{V}_G + \frac{L_1}{2(L_1 + L_3)}\frac{(1-D)D \cdot i_O}{n \cdot C_1 \cdot f_S} \quad \text{Eq. 2-47}$$

Therefore C_1 can be calculated with the following equation.

$$C_1 = \frac{L_1}{2(L_1 + L_3)}\frac{(1-D)D \cdot i_O}{n \cdot f_S(\mathrm{V}_{DS(\max)} - 2\mathrm{V}_{G(\max)})} \quad \text{Eq. 2-48}$$

The capacitance is the function of several parameters, such as switching frequency f_S, load current i_o, duty cycle, D, and the ratio of the leakage inductance $L_1/(L_1 + L_3)$.

Once the specifications, maximum voltage stress and the switching frequency of the converter have been determined, L_3 (=L_1) and C_1 can be calculated from Eq. 2-44 and Eq. 2-48. However, many combinations of clamp capacitance and the leakage inductance values are possible for a given application.

2.7. Comparisons of the FRR and the FAC

The proposed FRR has some advantages over the benchmark converter, the FAC, and a comparison will be made in this section.

The input current ripple Δi_G of the FAC and the FRR is illustrated in Fig. 2-10(c) and Fig. 2-10(d), respectively.

By utilizing the SABER simulation program, the comparison of the harmonic component of the input current i_G between the FAC and the FRR is made as illustrated in Fig. 2-11. Greater than 20dBuv improvements can be achieved for the FRR and maximum 40dBuv attenuations occur at fundamental and second-order harmonic components.

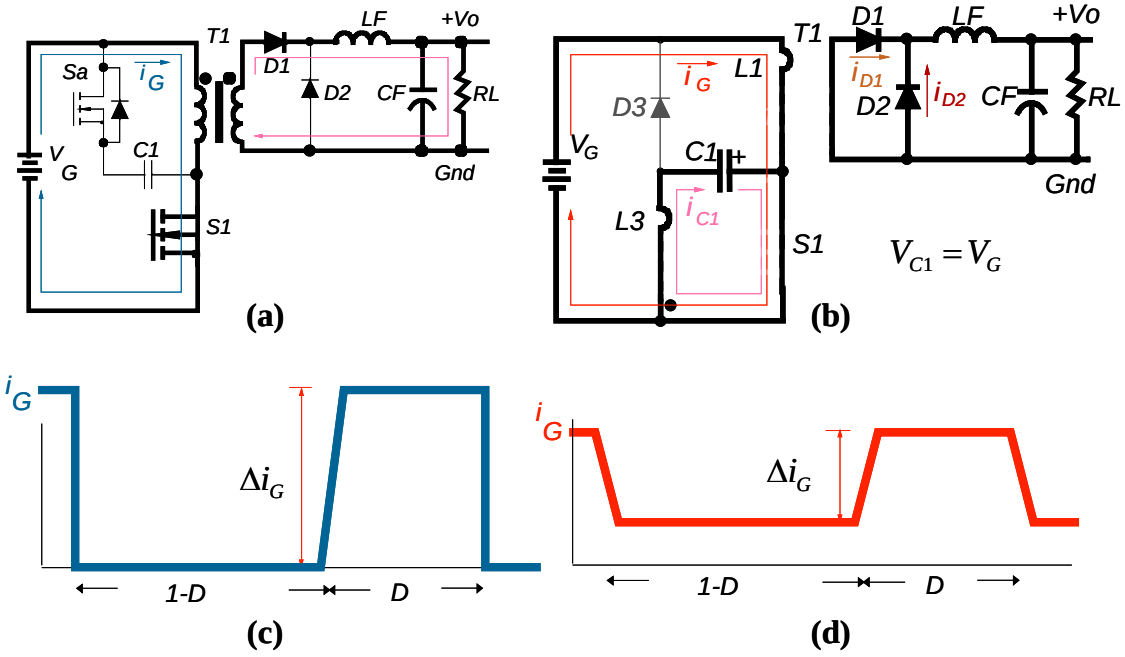


Fig. 2-10. Input current waveforms, i_G, of (a) the FAC and (d) the FRR.

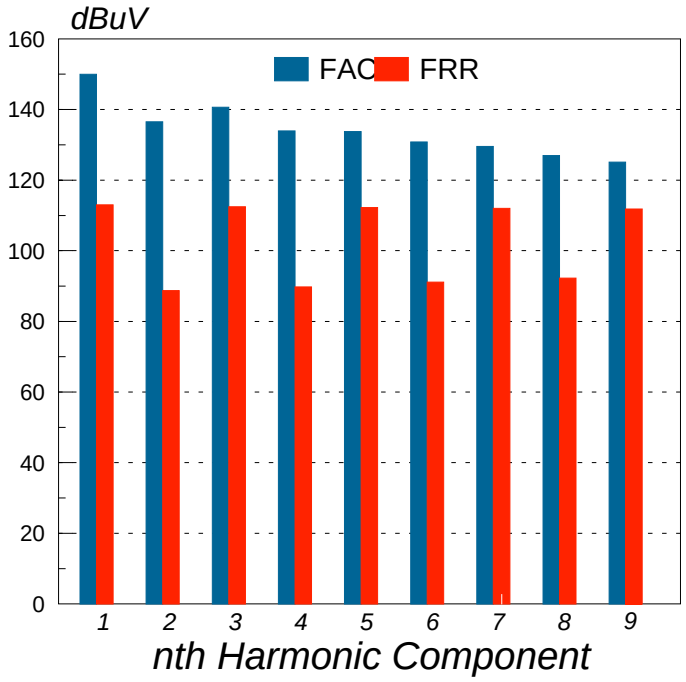


Fig. 2-11 Simulation results of the input current i_G harmonic components of the FAC and the FRR.

Because both input current waveforms i_G are a pulsating shape, an external LC filter must be added for each converter. As illustrated in Fig. 2-12(b)-(b') and Fig. 2-12(c)-(c'), filter capacitor current i_{Cin} inherits the current ripple of input current i_G. Consequently, the filter capacitor RMS current of the FRR would be lower than that of the FAC due to the reduced current ripple value. As a result, size reduction of the filter capacitor of the FRR is attainable or the temperature rise of the filter capacitor is reduced if the same filter capacitor used.

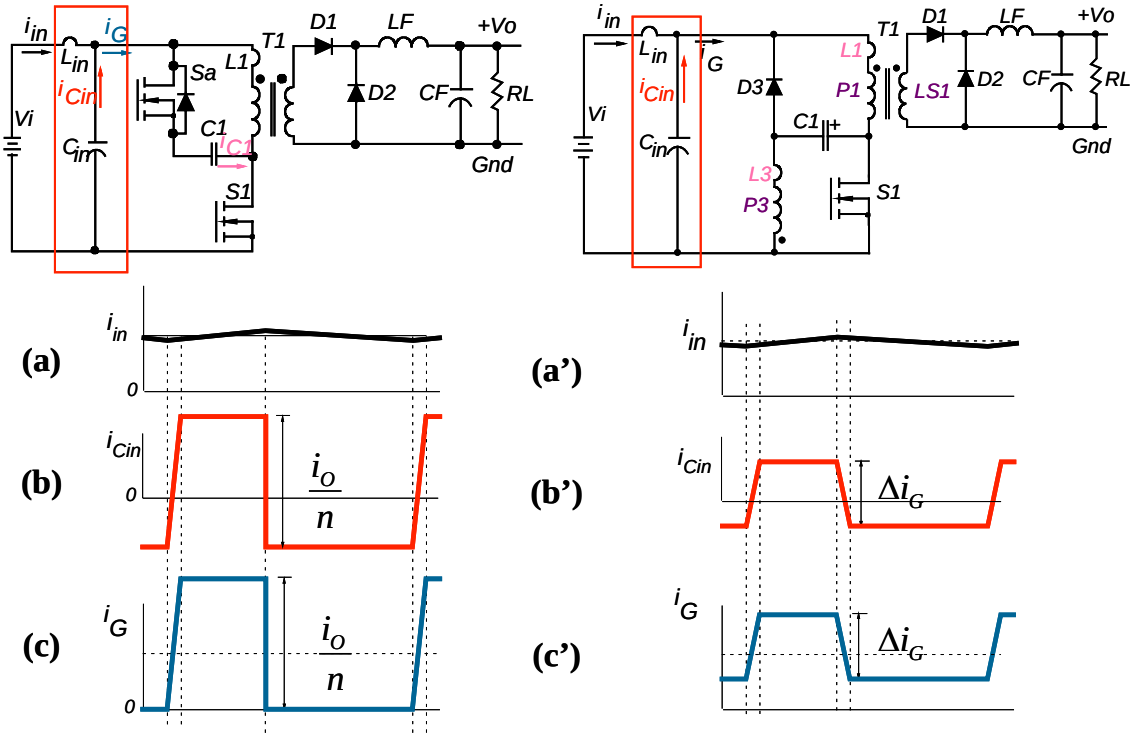


Fig. 2-12 Key current waveforms,(a)-(a') i_{in}, (b)-(b') i_{Cin} and (c)-(c') i_G, of the FAC and the FRR.

Shown in Fig. 2-13(a) is the circuit diagram of the FRR. Because L_1 and L_3 are the leakage inductances of the transformer, the FRR and the FAC (Fig. 2-13(b)) have the same component count in power stage circuitry. Instead of an active switch and a one-primary-winding transformer in the FAC, the FRR has a passive switch and a two-

primary-winding transformer. An additional isolated variable-duty-cycle gate drive makes the FAC circuit implementation more complicated than the FRR.

The leakage energy is stored in C_1 and recycled to the input source to maintain the charge balance in the FAC. In contrast, the leakage energy is stored in the clamp capacitor C_1 and transferred to the load in the FRR. Therefore, the leakage energy in both topologies is efficiently utilized.

Applying the volt-second to the transformer, the clamp capacitor V_{C1} is equal to $DV_G/(1-D)$. Although the voltage stresses on the MOSFET of the FRR and FAC can be calculated as $V_{DS} = V_G + V_{C1}$, the capacitor voltages are different for the FRR and the FAC. For the FRR, the maximum voltage stress is $V_{DS(\max)} = 2V_{G(\max)}$ due to the fact that the capacitor voltage is clamped to V_G. However, the clamp capacitor voltage V_{C1} of the FAC is the function of operating duty cycle as well as the input voltage. Since the input voltage increases while the operating duty cycle decreases, V_{DS} tends to remain approximately constant over a certain input voltage. Consequently, the FAC features the lowest voltage stress on the main switch under steady-state operating condition. During the large signal transient, however, the clamp-capacitor voltage increases and subsequently decreases. This oscillatory response causes excessive voltage stress on the MOSFET, the core saturation and the body diode reverse recovery problem of the active clamp switch [25].

As illustrated in Fig. 2-13(c), Fig. 2-13(d), and Fig. 2-13(e), the voltage stress of the FAC is higher than that of the FRR during 40V to 60V step-line transient.

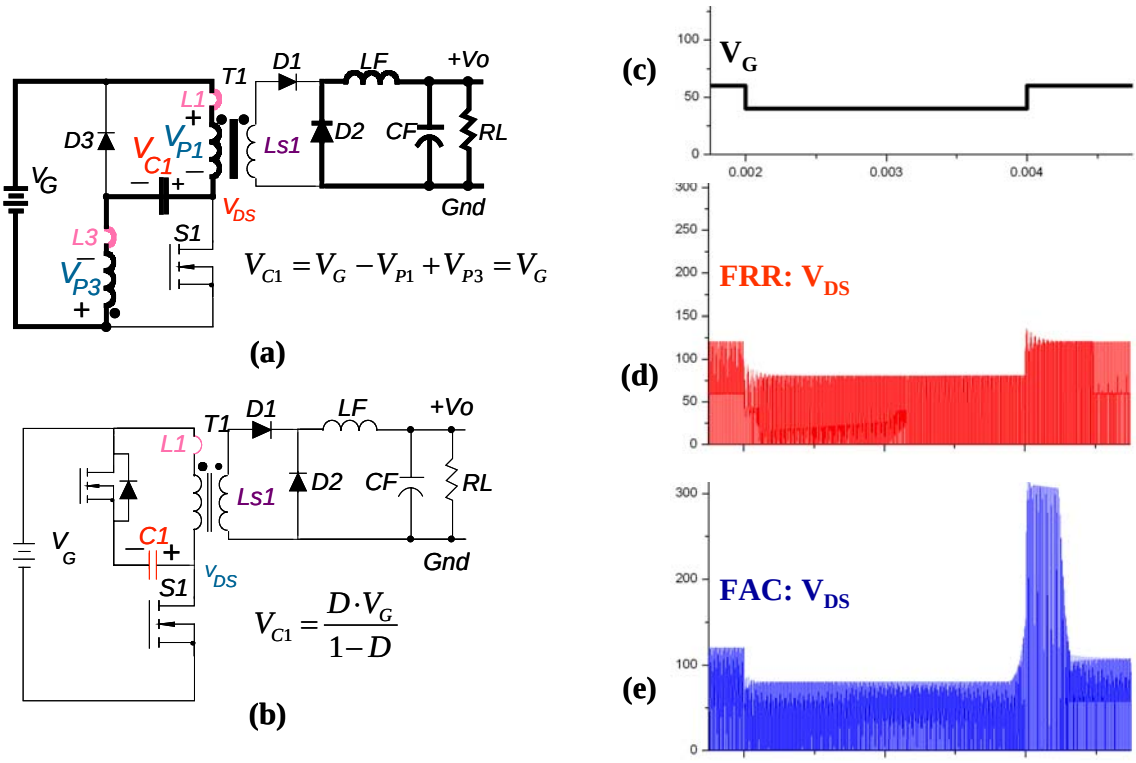
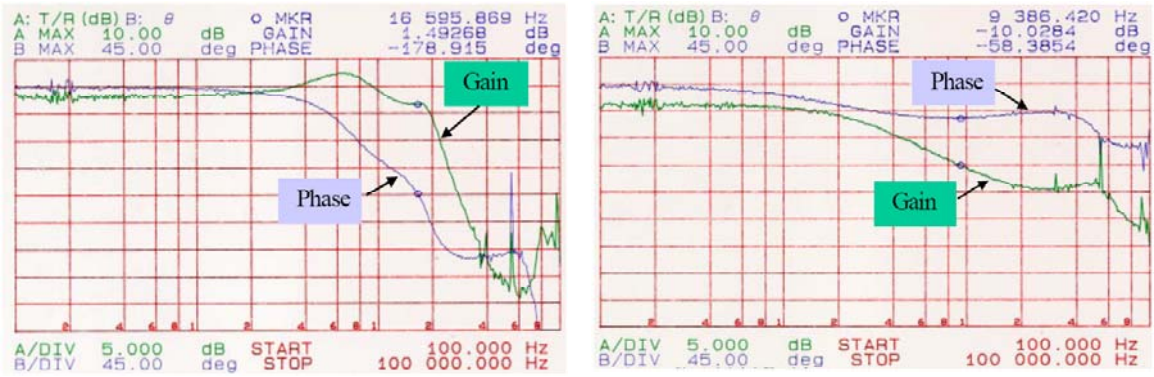


Fig. 2-13 Circuit diagram of (a) FAC (b) FRR (c) input-voltage step change from 40 V to 60 V, V_{DS1} transient waveforms of (d) the FAC (L_m=80uH, C_1=0.015uF) and (e) the FRR (L_1 = L3 = 540nH, C_1=20.9uF).

The small-signal model of the FAC is marginally different from the corresponding single-ended circuits. The ideal clamp circuit does not interfere with the control-to-output transfer function of the forward converter. However, due to the non-ideal nature of the clamp circuit, the available closed loop bandwidth is impacted [62]. It has been shown that the crossover frequency should occur before the complex pole-pair introduced by L_m and C_1. A high value of C_1 forces the crossover frequency to be very low, in addition to posing core saturation potential during transients. Fig. 2-14(a) shows the open-loop control to output bode plot of the flyback-forward converter, an extension of the FAC. It is a fourth-order system that makes its control design very difficult and its close loop bandwidth very low to ensure the system stable.

In contrast, the FRR is a second-order system. Fig. 2-14(b) shows push-pull forward

converter [68], a push-pull version of the FRR. Consequently, the control of the FRR is very easy. Like a buck converter, it can have very large close-loop crossover frequency resulting in faster transient response.



(a) **(b)**

Fig. 2-14 (a) Open loop control to output bode plot of (a) the flyback-forward converter and (b) the push-pull forward converters /courtesy of Xunwei Zhou [68].

Additionally, according to the SABER simulation results, the input current i_G of the FRR and the FRR with the notch filter have greater than 40dB improvements over the FAC at the fundamental component as illustrated in Fig. 2-15.

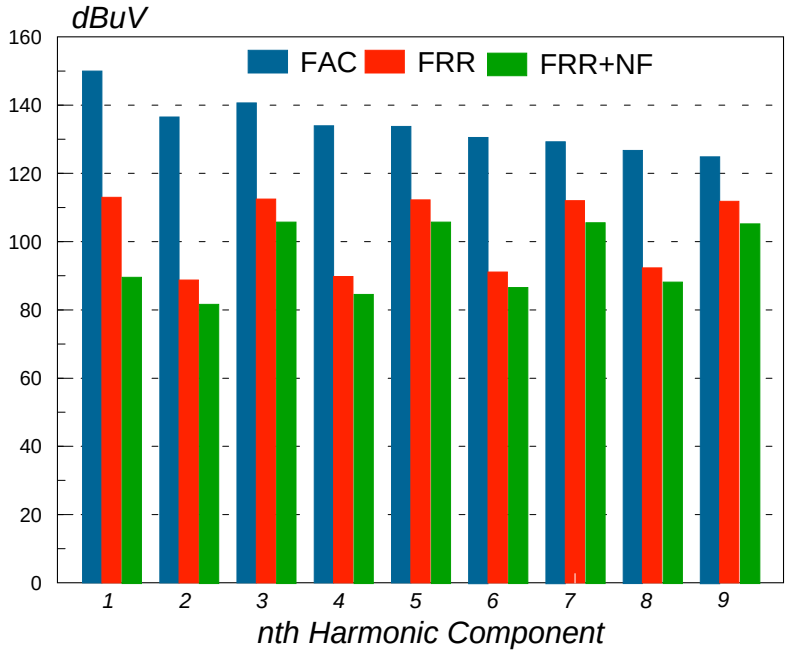


Fig. 2-15.Simulation results of the input current i_G harmonic components of the FAC, the FRR, and the FRR with notch filter.

2.8. Experimental Validation

In this section, a 40-60V input voltage, 5V output-voltage and 200W output power operating at 150kHz FRR is implemented.

The design procedure starts from setting the following parameters:

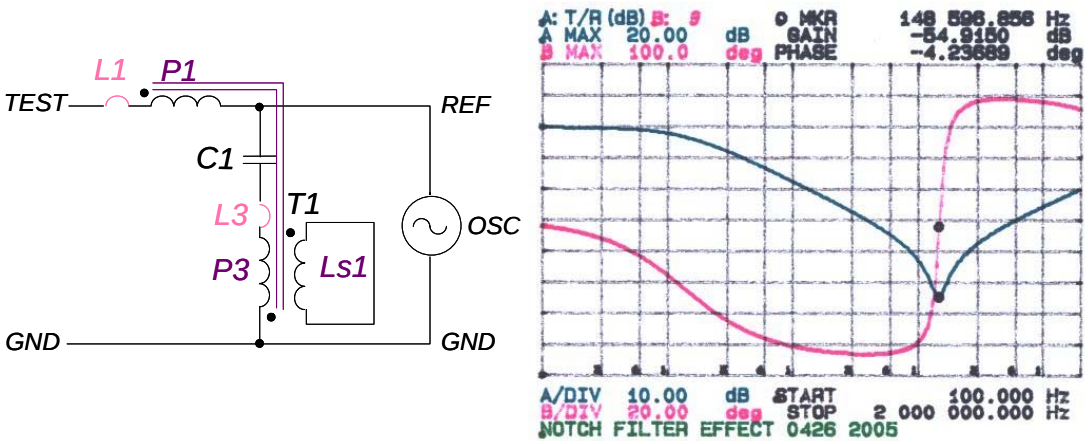
$V_{G(max)}$=60V, V_O=5V, $i_{O(max)}$=40A, D_{max}=0.45, $V_{DS(max)} = 122.5V$, f_S= 150KHz, n=3, and assumes L_1=L_3. According to Eq. 2-48, the clamp capacitor can be calculated.

$$C_1 = \frac{L_1}{2(L_1 + L_3)} \frac{(1-D)D \cdot i_O}{n \cdot f_S (V_{DS(max)} - 2V_{G(max)})}$$ =2.2uF. Therefore, L_3=520nH is calculated according to Eq. 2-44, $f_O = 1/(2\pi\sqrt{L_3 C_1}) = f_S$.

To verify the characteristic of the embedded notch filter, the secondary winding of the transformer, L_{s1}, is shorted and the test circuit is implemented as illustrated in **Fig. 2-16**(a). The measured insertion voltage-gain shows that a maximum attenuation occurs at the surrounding area of the switching frequency 150KHz as illustrated in **Fig. 2-16**(b). Practically, the performance will be degraded due to the component deviation. The embedded notch filter is not the key issue, however, the converter performance has some degree of improvements without an external LC filter.

The design specifications and key components are listed in Table 2-1.

The transformer was constructed with an ER35 core and 9:9:3 turns ratio, which means that the effective turns ratio equals 3. The main switch is a Fairchild FQA55N25. The rectifier is a MOSPEC S60D60CJ with 0.75V forward voltage. The clamp diode, D_3, is BYV 27-200. The primary windings use 0.8 ϕ *3 wires and the secondary windings use 0.2*1.2mm copper sheet.



(a) (b)

Fig. 2-16 (a) Notch filter measurement set up and (b) measured transfer gain of the notch filter.

Table 2-1 Design specification and components used in the prototype of the FRR

Specifications	V_G: 40-60V, 5V/40A, f_s=150KHz
S_1	FQA55N25, $R_{DS(on)}$=0.04 ohms
T_1	ER-35 with 9:9:3 turns
D_1,D_2	MOSPEC S60D60CJ 60V/60A, V_f=0.75V
D_3	BYV27-200 200V, 2A

Fig. 2-17 shows the oscillograms of the FRR under V_{in} = 48V, V_o = 5V, and I_o = 40A operation conditions. The V_{DS} is clamped to two times the input voltages without any voltage spike as shown in Channel 2.

The oscillogram of the input current, I_G, is shown in channel 4. The current ripple is reduced and the noise problems of the converter can be alleviated.

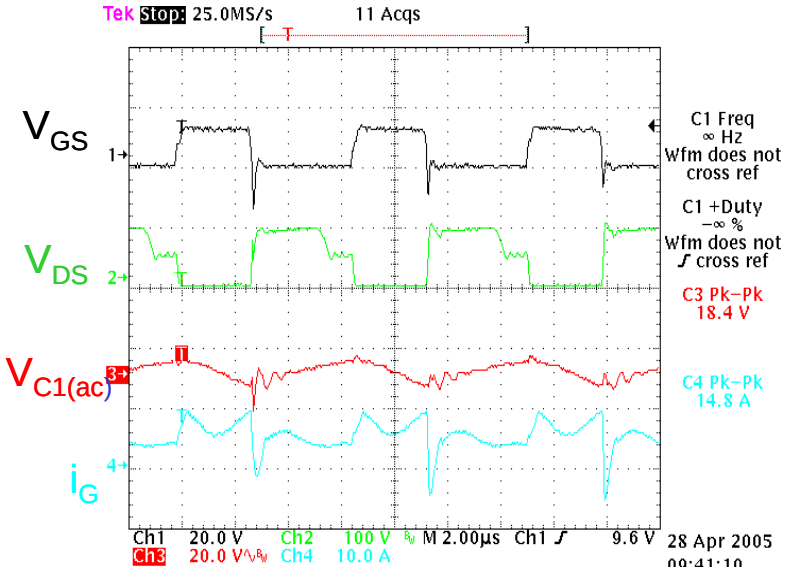


Fig. 2-17. Key experimental waveforms of the prototype FRR.

In addition to the proposed FRR, the forward converter with active clamp (FAC) is implemented with the same specifications to make performance comparisons with respect to the noise level and the converter efficiency.

As shown in Fig. 2-18(a), the input current waveforms of the three tested forward converters are pulsating. These waveforms are obtained with 48V input voltage and 5V/20A operation conditions.

Although the FAC operates in a larger duty cycle, its current ripple is not the lowest. In fact, the FRR has the lowest current ripple among the three converters due to its current ripple reduction feature.

The comparison of the fundamental component of the input current i_G is shown in Fig. 2-18(b). These data are collected by using the scope's built-in Fast-Fourier-Transform (FFT) function from the input current waveform and plotted with different load current operating conditions. Instead of a single curve in the FAC, a band is extended to represent ±10% of leakage inductance and the clamp capacitor deviations

impact on the fundamental component in the FRR. As illustrated, the FRR has better performance due to the current ripple reduction and the embedded notch filter features.

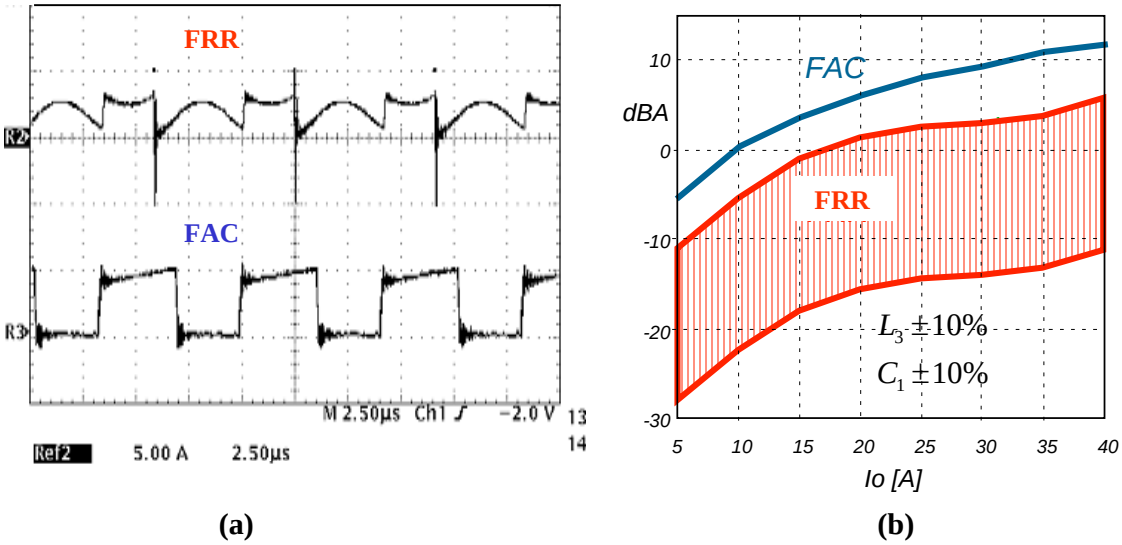


Fig. 2-18. Comparisons of the measured (a) input current waveforms and (b) their fundamental components of the FAC and the FRR.

Fig. 2-19 shows the measured efficiency comparison of the tested converters. Because the maximum operating duty cycle is limited to 50%, the FRR has higher conduction loss. Hence, the FAC has the better efficiency performance under the full load range.

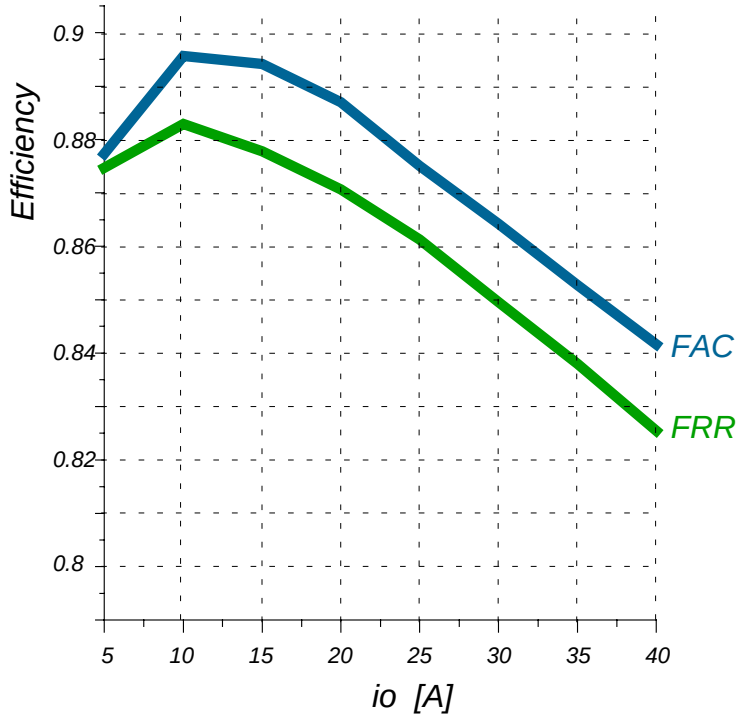


Fig. 2-19. Measured efficiency comparison of the FRR and the FAC.

2.9. Summary

In this chapter, input current ripple reduction and embedded filter techniques are proposed. Applying these techniques, the FRR is presented and the operational principle is introduced. The FRR has several advantages as listed below.

1. It is a very simple circuit, which does not require special timing driving circuit for the reset switch;
2. The voltage spikes caused by the leakage inductance are eliminated;
3. The voltage across the main switch is clamped to input voltage at both static and dynamic states;
4. The input current ripple is reduced to $(\frac{L_3}{L_1+L_3}\frac{i_O}{n})$;
5. The embedded notch filter can reduce the fundamental component intensity.

However, there are also some limitations as follows.

1. The reset is not “optimized” as it is in the FAC, and a voltage across the primary switcher is higher for the same duty cycle;
2. The maximum operating duty cycle is limited to 50%;
3. It is hard-switching operation for the main switch.

In addition to the analysis, several performance comparisons between the FRR and the FAC have been made by utilizing the SABER simulation program. Finally, the experimental results are collected to verify the performance of the FRR.

Using the FRR as an example, the performance of the PWM converter can be enhanced with the proposed techniques by utilizing the leakage inductance and the clamp capacitor. Moreover, further improvements can be achieved by taking advantage of the proposed techniques, and a forward converter with current ripple cancellation (FRC) that will be presented in the next chapter.

Chapter 3 Forward Converter with Current Ripple Cancellation (FRC)

3.1. Introduction

As illustrated in Fig. 3-1, the FRR has a lower input current ripple than the FAC. Therefore, referring to Fig. 2-15, the EMI noise problem can be alleviated. However, its current waveform holds the pulsating shape so that the benefits are limited. As shown in Fig. 3-1(b), the input current ripple of the FRR ($\Delta i_G = \frac{L_3}{L_1 + L_3}\frac{i_O}{n}$) can be further reduced if $L_1 >> L_3$. However, an additional inductor or a special winding scheme is needed to realize the relation of $L_1 >> L_3$.

In contrast, the current ripple can be further reduced achieved by taking advantage of the proposed techniques without adding an external inductor. Two sets of the clamp capacitor and the leakage inductance are utilized and the current ripple can even be cancelled if the condition is met. Consequently, input current becomes a non-pulsating waveform as shown in Fig. 3-1(c) and a forward converter with ripple cancellation (FRC) is presented in this chapter.

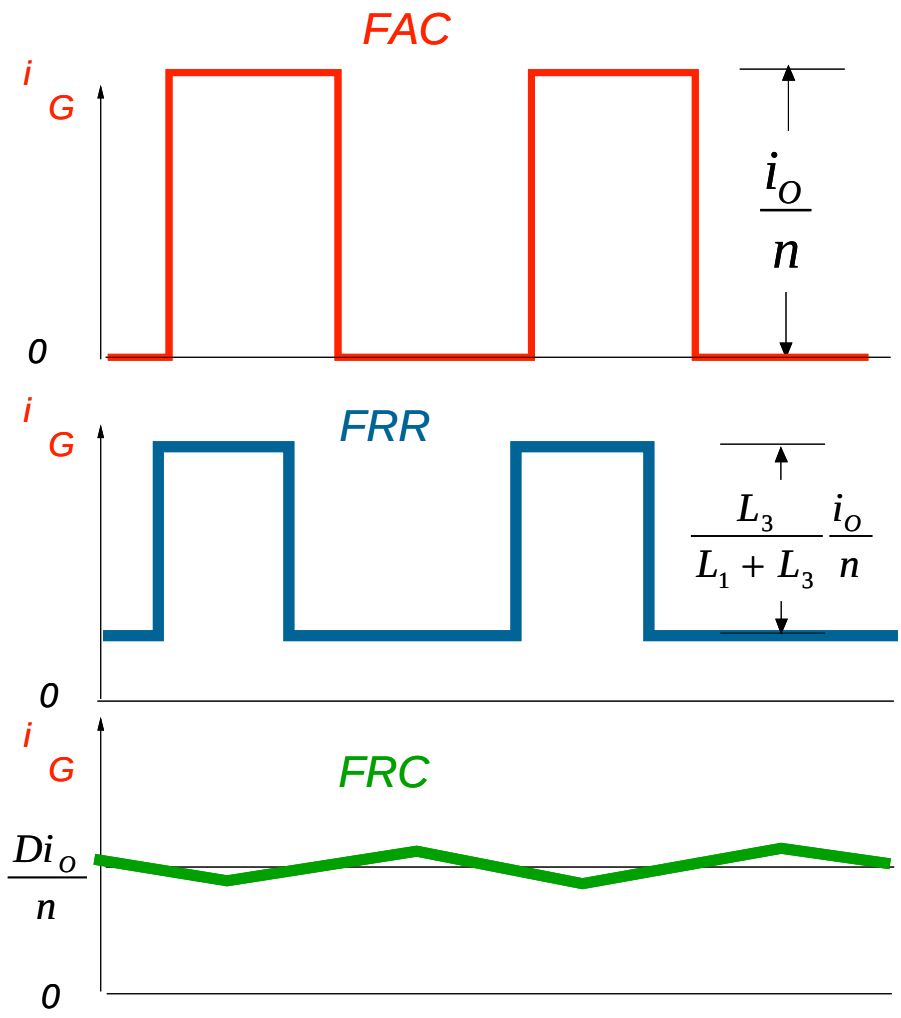


Fig. 3-1 Pulsating input current waveforms of (a) the FAC (b) the FRR (c) desired non-pulsating waveform of the FRC.

3.2. Derivation of the Forward Converter with Current Ripple Cancellation (FRC)

Fig. 3-2(a) and (b) are the circuit diagrams of the FRR and its mirrored forward converter with current ripple reduction (MFRR). The MFRR is obtained by mirroring the components of the FRR in an upside-down manner. As illustrated, the input currents of the FRR and MFRR can be decomposed into two current components, i_{L1}-i_{D3} and i_{L3}-i_{S2}, respectively. It is assumed that all the leakage inductances of the transformer, L_1 – L_4,

are equal so that i_{L1} and i_{L3} have the same amplitude but the pulsating current ripples move in opposite directions, as illustrated in Fig. 3-2(c)-(d). The sum of i_{L1} and i_{L3} becomes a continuous waveform due to the cancellation of the pulsating input current ripple in Fig. 3-2(e). This leads to the evolution of the forward converter with current ripple cancellation (FRC). The forward converter with current ripple cancellation (FRC) is proposed as shown in Fig. 3-2(f) [66]. The current ripple cancellation mechanism is employing by connecting the FRR and MFRR in a series-and-parallel to derive the FRC. The FRC can be decomposed of the FRR (or MFRR) by shorting the winding L_{P3}-L_{P3} (or L_{P1}-L_{P4}), and C_2 (or C_1) can be regarded as an input filter capacitor.

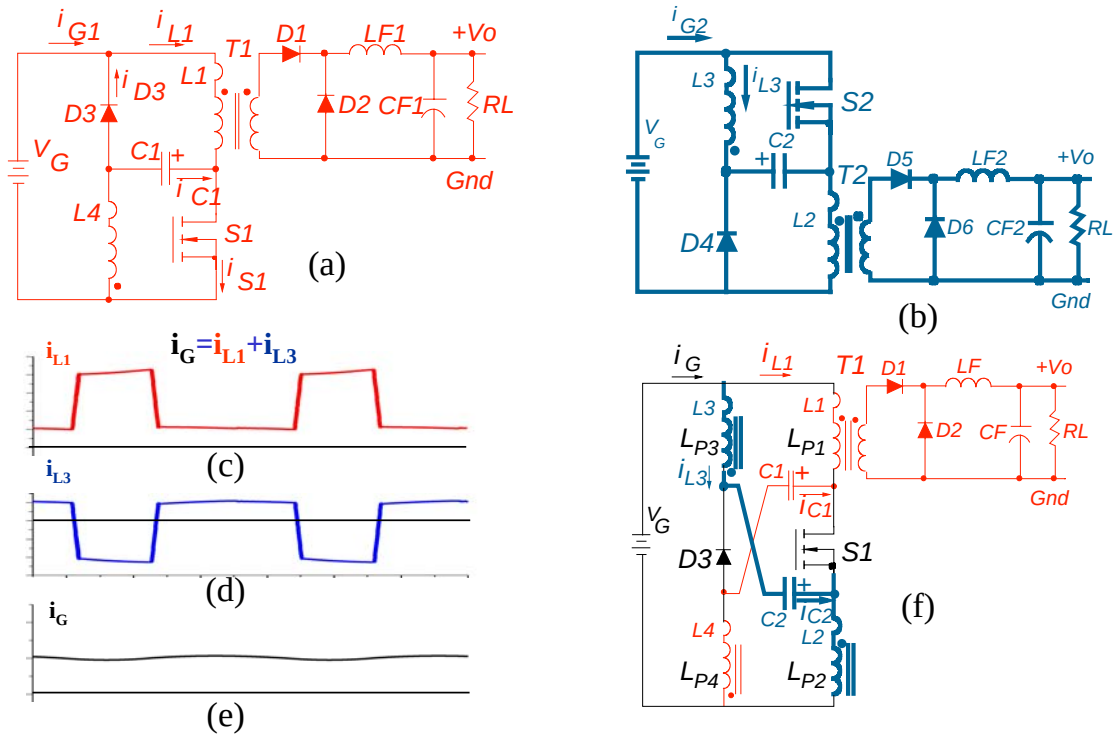


Fig. 3-2 Circuit diagram of (a) the FRR, (b) the MFRR, and (c)-(e) current ripple cancellation mechanism, $i_G=i_{L1}+i_{L3}$ (f) the proposed FRC.

The high-frequency switching current, i_{L1}, is thus supplied by the i_{L3}, and the input current, i_G, becomes a continuous waveform in the FRC.

3.2.1. Conditions for Current Ripple Cancellation

To achieve the current ripple cancellation, a four-primary-winding transformer is needed, in contrast to the two-primary-winding transformer needed in the FRR. Based on the identical primary leakage inductances of the transformer, the waveforms of the i_{L1} and i_{L3} or i_{L4} and i_{L3} have the same amplitude but opposite pulsating current ripples resulting in a non-pulsating input current waveform. However, the leakage inductances have variations in practice. As a result, the input current ripple cancellation performance would be degraded to that of an FRR with a smaller current ripple.

Therefore, the current ripple cancellation performance with respect to the leakage inductance distribution is analyzed. Fig. 3-3 shows the equivalent circuit for load current distribution during the S_1 turning-on transition (T_3-T_4).

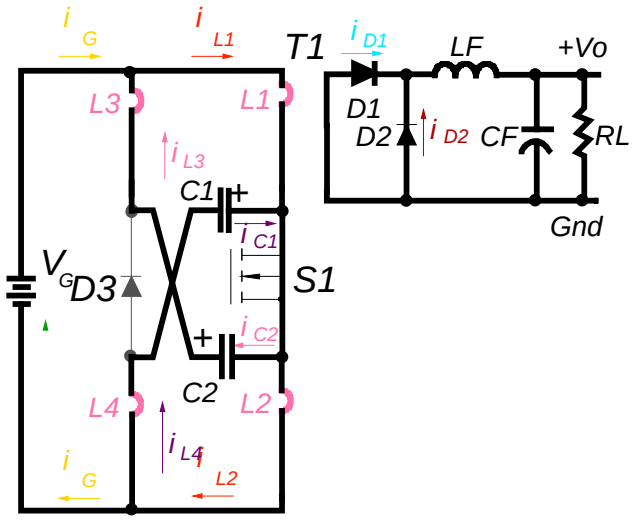


Fig. 3-3 Equivalent circuit diagram for load current ripple distribution during S_1 turn-on transition.

The load current ripple distribution among V_G, V_{C1}, and V_{C2} is determined by the different leakage inductance components, i.e. the load current ripple distribution of V_G is applied on the sum of the leakage inductances, L_1 and L_2; the capacitor voltage, V_{C1}, which is equal to the input voltage is applied on the sum of the leakage inductance, L_2 and L_4; the capacitor voltage, V_{C2}, which is also equal to the input voltage is applied on the sum of the leakage inductances, L_1 and L_3. Because V_{C1} and V_{C2} are clamped to V_G, each current component can be calculated as the following equation.

$$\Delta i_{L1} = \frac{V_G}{L_1 + L_2}(T_4 - T_3) \quad \text{Eq. 3-1}$$

$$\Delta i_{L2} = \frac{V_G}{L_2 + L_4}(T_4 - T_3) \quad \text{Eq. 3-2}$$

$$\Delta i_{L3} = \frac{V_G}{L_1 + L_3}(T_4 - T_3) \quad \text{Eq. 3-3}$$

To achieve a perfect pulsating current ripple cancellation, the following equations should be met.

$$\Delta i_{L1} = \Delta i_{L2} \text{ if } L_1 = L_4 \quad \text{Eq. 3-4}$$

$$\Delta i_{L1} = \Delta i_{L3} \text{ if } L_2 = L_3 \quad \text{Eq. 3-5}$$

Otherwise, the current ripple cancellation performance would be degraded to be current ripple reduction instead.

The effect of the leakage inductance variation on the current ripple cancellation performance is verified by utilizing the SABER simulation program. Two cases are studied. Following the perfect cancellation requirements, Eq. 3-4 and Eq. 3-5, the leakage inductances are set to $L_1=L_4=10uH$ and $L_2=L_3=1uH$, the input current is a non-pulsating

waveform due to the perfect ripple cancellation as shown in Fig. 3-4(a). In contrast, a 10% deviation between L_1-L_4 or L_2-L_3 makes input current a small pulsating waveform as shown in Fig. 3-4(b).

Therefore, to achieve a continuous input current waveform, the equations of L_1=L_4 and L_2=L_3 are required, and the bifilar winding scheme is strongly recommended for each pair of the winding, L_1-L_4, and L_2-L_3.

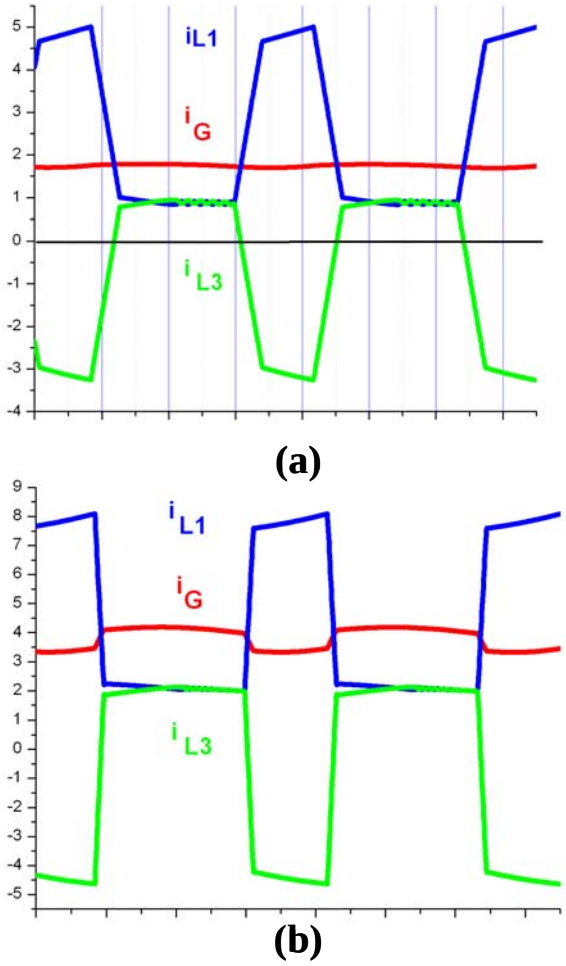


Fig. 3-4 Simulation verification of (a) current ripple cancellation with L_1=L_4=10uH and L_2=L_3=1uH, (b) degraded to current ripple reduction performance if 10% deviation between L_1 and L_4 or L_2 and L_3 (L_1=L_2=1.1uH and L_3=L_4=1uH).

3.3. Steady-State Analysis

Due to the two clamp capacitors, the FRC is like three forward converters in parallel during the on time period as illustrated in Fig. 3-5(a). When the main switch S_1 is turned on, the transformer windings (L_{P1}-L_{P3}, L_{P3}-L_{P4}, and L_{P1}-L_{P3}) are applied by three voltage sources (V_G, V_{C1}, and V_{C2}) and the leakage inductance energies are transferred to the load. After the main switch S_1 is turned off, both clamp capacitors C_1 and C_2 are charged by the input source as illustrated in Fig. 3-5(b).

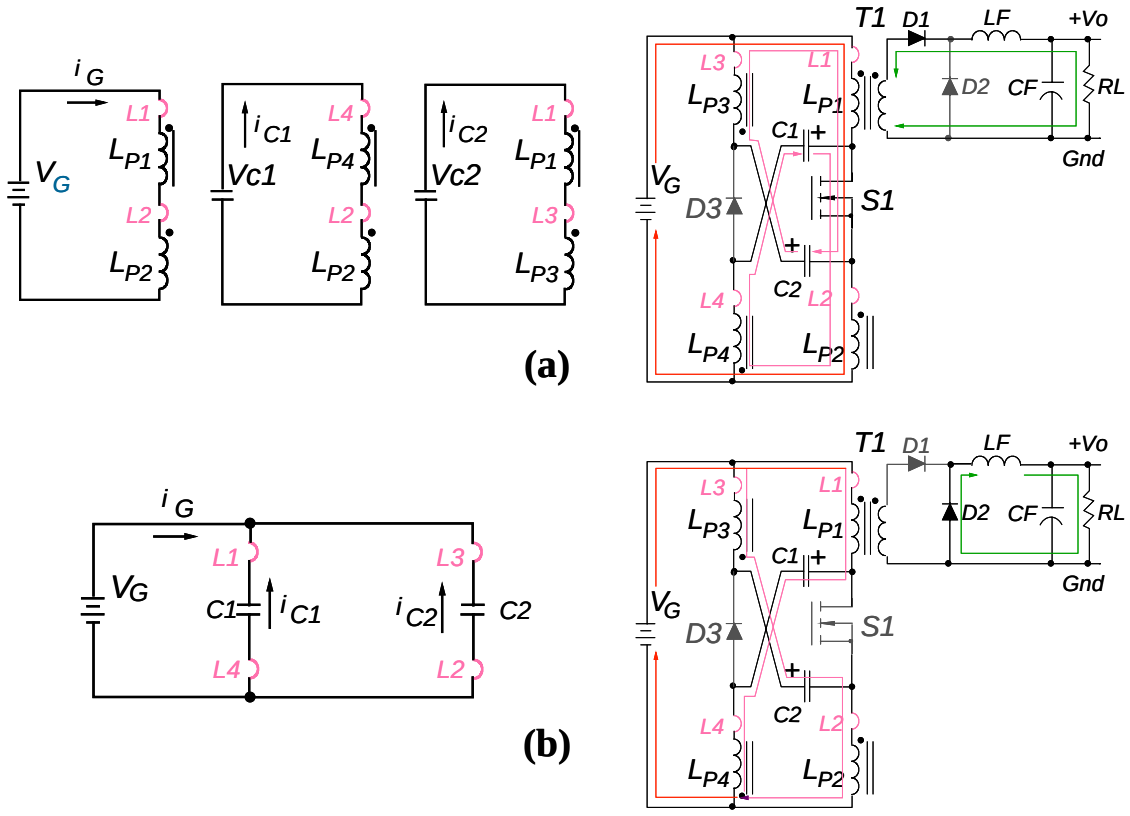


Fig. 3-5 Operating modes of the FRC during (a) the on time (b) the off time.

As illustrated in Fig. 3-6(b), the charge balance property of the capacitor is utilized and the expression of the key current waveforms can be derived.

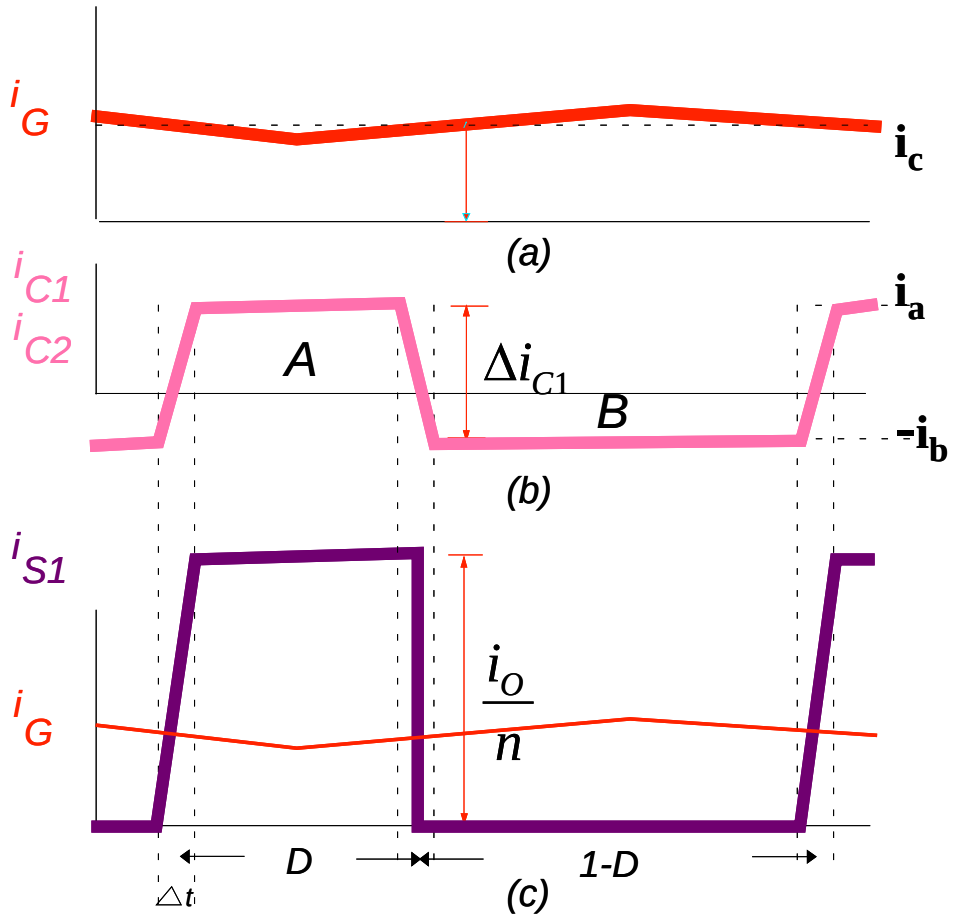


Fig. 3-6. Current waveforms, (a) I_G, (b) I_{C1}, and I_{C2} , charge balance A=B, (c) switch current $I_{S1}$of the FRC.

Assuming $i_{mag} << i_O$, where I_o is the load current, and I_{mag} is the magnetizing current, then the following equation applies.

$$i_G + i_{C1} + i_{C2} = \frac{I_o}{n} \qquad \text{Eq. 3-6}$$

The capacitor C_1 and C_2 discharge their energies to load current during the on time interval and are charged by the input current during the off time interval as shown in Fig. 3-5(b).

The charge current of each capacitor is expressed in the following equation.

$$i_b = i_{C1} = i_{C2} = -\frac{1}{2} i_G \qquad \text{Eq. 3-7}$$

The reflected load current is supplied by I_G, I_{C1}, and I_{C2} during the on time.

$$i_C + 2i_a = \frac{I_o}{n} \qquad \text{Eq. 3-8}$$

According the charge balance of the capacitor, I_C can be calculated as follows.

$$i_a \cdot D \cdot T_S = \frac{1}{2} |i_b| \cdot (1 - D) \cdot T_S \qquad \text{Eq. 3-9}$$

$$i_C = \frac{D i_o}{n} = i_{AVG} \qquad \text{Eq. 3-10}$$

Therefore,

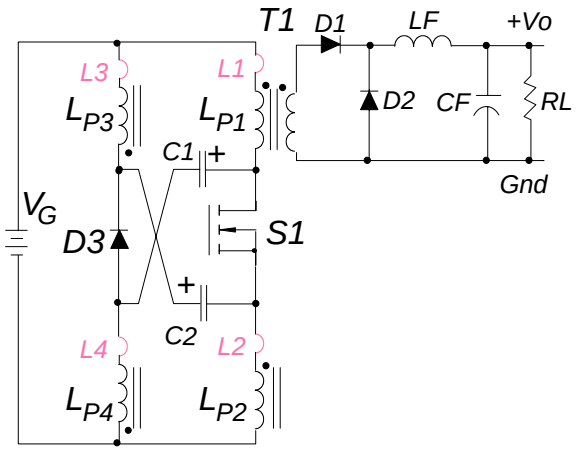
$$i_a = \frac{1 - D}{2n} i_o \qquad \text{Eq. 3-11}$$

and

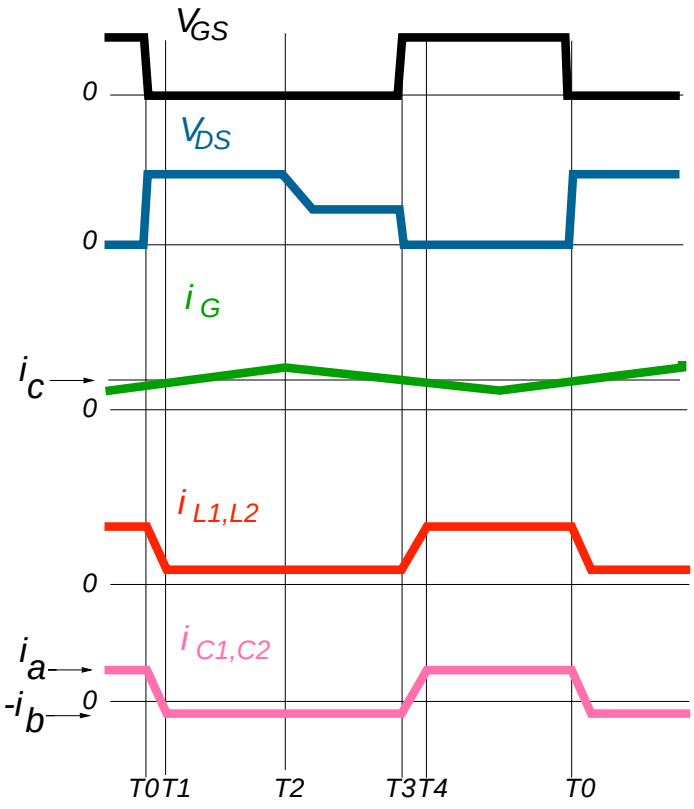
$$i_b = \frac{D}{2n} i_0 \qquad \text{Eq. 3-12}$$

3.4. Operational principle of the Forward Converter with Current Ripple Cancellation (FRC)

The circuit diagram and key waveforms of the forward converter with current ripple cancellation (FRC) are shown in Fig. 3-7. The primary side of the power stage consists of a switch, S_1; two clamp capacitors, C_1 and C_2; one clamp diode, D_3; and one transformer. The transformer is comprised of four identical primary windings and one secondary winding with the turns ratio of (n : n : n : n : 1). L_1-L_4 are represented as the leakage inductance of L_{p1}-L_{p4}, respectively.



(a)



(b)

Fig. 3-7 (a) Circuit diagram and (b) key waveforms of the FRC.

To simplify the analysis, the output filter inductance is assumed to be sufficiently large to be approximated by a current source with a value equal to the output current, I_o. The clamp capacitors are assumed to be sufficiently large that the voltage across each

capacitor can be assumed to be constant. Also, $i_{mag} << i_O$, $L_1 = L_2 = L_3 = L_4 = L_k$, $C_1 = C_2 = C_C$, and $f_o = \frac{1}{2\pi\sqrt{2L_kC_c}} << f_S$ are assumed, where f_0 is the corner frequency defined by $2L_k$ and C_c and I_o is load current, and I_{mag} is the magnetizing current. During steady-state operation, five operation stages exist within one switching cycle as shown in Fig. 3-8(a)-(e):

(a) T_0-T_1:

The circuit operation begins with the switch off at T_0. Prior to T_0, the power is transferred from the input source, V_G, and the energy stored in capacitors, C_1 and C_2. I_{C1} and I_{C2} provide part of the load current via L_{P3}-L_{P4} and L_{P3}-L_{P1}, while I_G provides the complementary part of the load current via L_{P1} –L_{P3} so that their sum is equal to reflected load current, according to Eq. 3-10 and Eq. 3-11.

At T_0, the following equations apply.

$$i_G = \frac{D}{n} i_o \qquad \text{Eq. 3-13}$$

$$i_{S1} = i_G + i_{C1} + i_{C2} = \frac{i_o}{n} \qquad \text{Eq. 3-14}$$

$$i_{C1} = i_{C2} = i_a = \frac{1-D}{2n} i_o \qquad \text{Eq. 3-15}$$

After S_1 turns off at T_0, transformer windings L_{P1}-L_{p4} and L_{s1} are shorted due to the turning on of D_1 and D_2. Consequently, three pairs of the sum of the leakage inductances, L_1-L_3, L_1-L_2, L_2-L_4, are supplied by a negative voltage and thus the

currents, I_G, I_{C1}, and I_{C2}, are linearly decreased to the reflect the load current interruption as the following equation.

During $T_0 < t < T_1$,

$$i_{C1} = i_{C2} = \frac{(1-D)i_o}{2n} - \frac{V_G}{2L_K}(t - T_0) \qquad \text{Eq. 3-16}$$

The clamp diode D_3 will be forced to turn on by the leakage and the magnetizing currents and the leakage energies are stored in C_1 and C_2. The voltage stress V_{DS} on switch S_1 will be clamped by the sum of V_{C1} and V_{C2}, $2V_G$. The reset voltages, $-V_G$, $-V_{C1}$, and $-V_{C2}$ are thus applied on the three pairs of the windings, L_{P1}-L_{P3}, L_{P3}-L_{P1}, and L_{P4}-L_{P3}, to start the core-reset function.

At T_1, D_1 is turned off because load current is freewheeled through diode D_2 and

$$i_{C1} = i_{C2} = -i_b = -\frac{D}{2n} i_o \qquad \text{Eq. 3-17}$$

(b) T_1-T_2:

During this time period, the magnetizing current flows through D_3 to provide core reset of the transformer. The primary current I_G flows through L_1-L_{P1}-C_1-L_4-L_{P4} and L_3-L_{P3}-C_2-L_2-L_{P2}. Because the voltages across the windings L_{P1} and L_{P4} (or L_{P2} and L_{P3}) cancel each other due to the presence of the opposite winding polarities, C_1 (or C_2) is charged by the input power source, V_G. At T_2, the zero average-volt-second of the transformer is achieved and D_3 is turned off.

During this time interval, the following equation applies.

$$V_{DS} = 2V_G \qquad \text{Eq. 3-18}$$

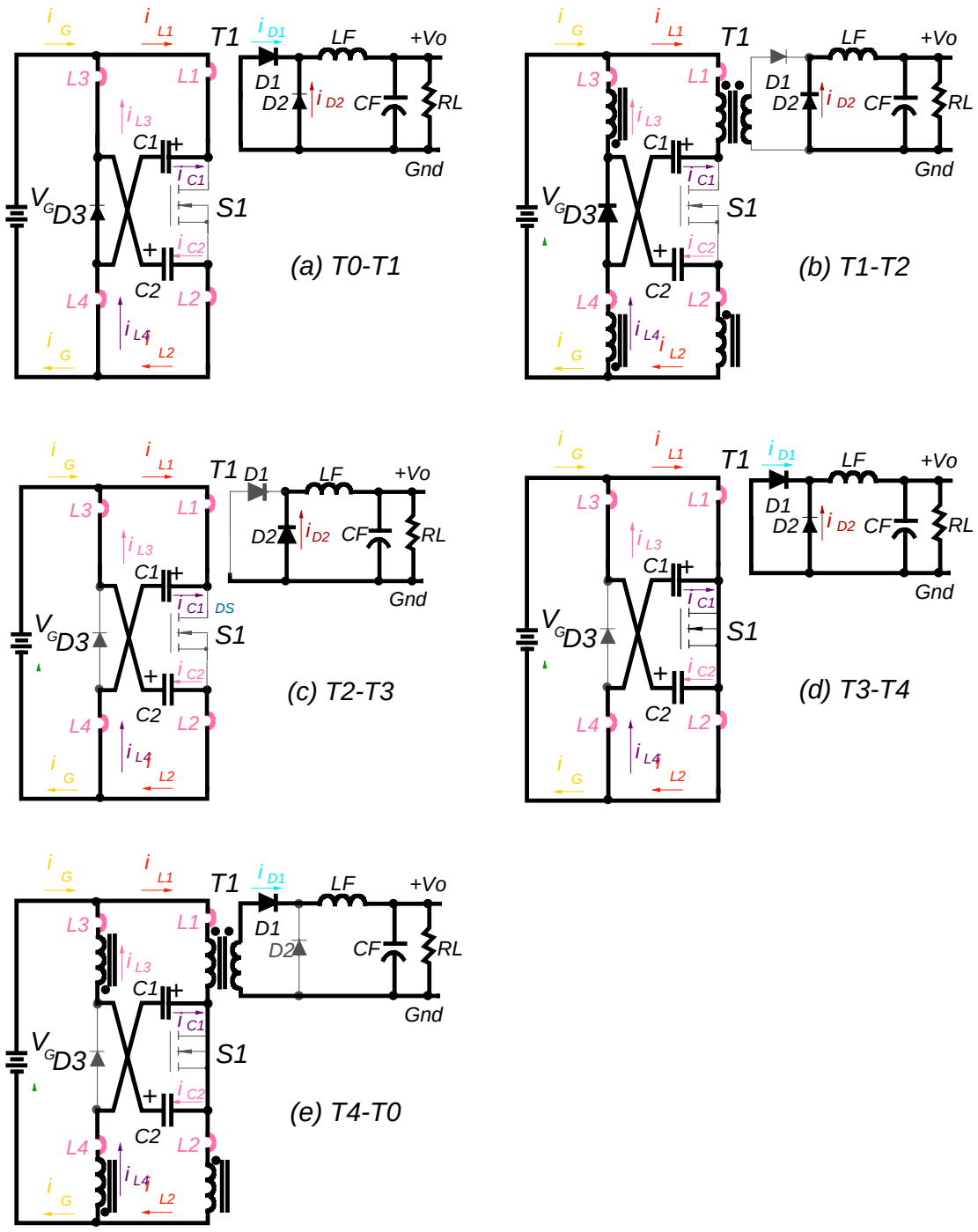


Fig. 3-8 Equivalent circuits of the FRC operating stage.

$$i_G = \frac{D}{n} i_o \quad \text{Eq. 3-19}$$

$$i_{L1} = i_{L2} = i_b = \frac{D}{2n} i_o \quad \text{Eq. 3-20}$$

$$i_{C1} = i_{C2} = -i_b = -\frac{D}{2n} i_o \quad \text{Eq. 3-21}$$

(c) T_2-T_3:

During this time interval, the transformer windings are shorted due to the lack of magnetizing energy. C_1 and C_2 are charged continuously and V_{C1} and V_{C2} are clamped to V_G. Both voltage stresses on the switch and clamp diode are clamped to V_G. At T_3, the gate drive signal is applied to turn on the switch.

During this time interval, the following equations are applied.

$$V_{DS} = V_G \quad \text{Eq. 3-22}$$

$$i_G = \frac{D}{n} i_o \quad \text{Eq. 3-23}$$

$$i_{L1} = i_{L2} = i_b = \frac{D}{2n} i_o \quad \text{Eq. 3-24}$$

$$i_{C1} = i_{C2} = -i_b = -\frac{D}{2n} i_o \quad \text{Eq. 3-25}$$

(d) T_3-T_4:

At T_3, the main switch S_1 is turned on. Due to the turning on of D_1 and D_2, transformer windings are shorted. Consequently, all the leakage inductances L_1 - L_4

are supplied by a positive voltage and the currents i_{C1} and i_{C2} are linearly increased to reflect the demand of load current.

During $T_3 < t < T_4$,

$$i_{C1} = i_{C2} = -\frac{Di_o}{2n} + \frac{V_G}{2L_K}(t - T_4) \quad \text{Eq. 3-26}$$

At T_4,

$$i_{C1} = i_{C2} = \frac{(1-D)i_o}{2n} \quad \text{and} \quad \text{Eq. 3-27}$$

$$i_G + i_{C1} + i_{C2} = \frac{i_O}{n} \quad \text{Eq. 3-28}$$

(e) T_4-T_0:

During this time interval, the power is transferred from the input source, V_G, and the energy stored in capacitors, C_1 and C_2. Currents i_{C1} and i_{C2} provide part of the load current via L_{P3}-L_{P4} and L_{P3}-L_{P1}, while i_G provides the complementary part of the load current via L_{P1} -L_{P3} so that their sum is equal to reflected load current, $i_G + i_{C1} + i_{C2} = \frac{i_O}{n}$. At T_0, the following equations apply.

$$i_G = \frac{D}{n} i_o \quad \text{Eq. 3-29}$$

$$i_{S1} = i_G + i_{C1} + i_{C2} = \frac{i_o}{n} \quad \text{Eq. 3-30}$$

$$i_{C1} = i_{C2} = i_a = \frac{1-D}{2n} i_o \quad \text{Eq. 3-31}$$

S_1 is turned off and another switching cycle begins.

3.5. Embedded Low-Pass Filter

In addition to the steps above, the embedded filter technique is applied to the FRC, and the performance with respect to current ripple reduction can be further improved.

The embedded filter technique is applied to the FRC as explained in Fig. 3-9. Circuit evolution begins with shifting the clamp network S_1-C_1-D_3-C_2 from Fig. 3-9(a) and the FRC becomes a forward converter with two L-C-L networks in parallel as shown in Fig. 3-9(b).

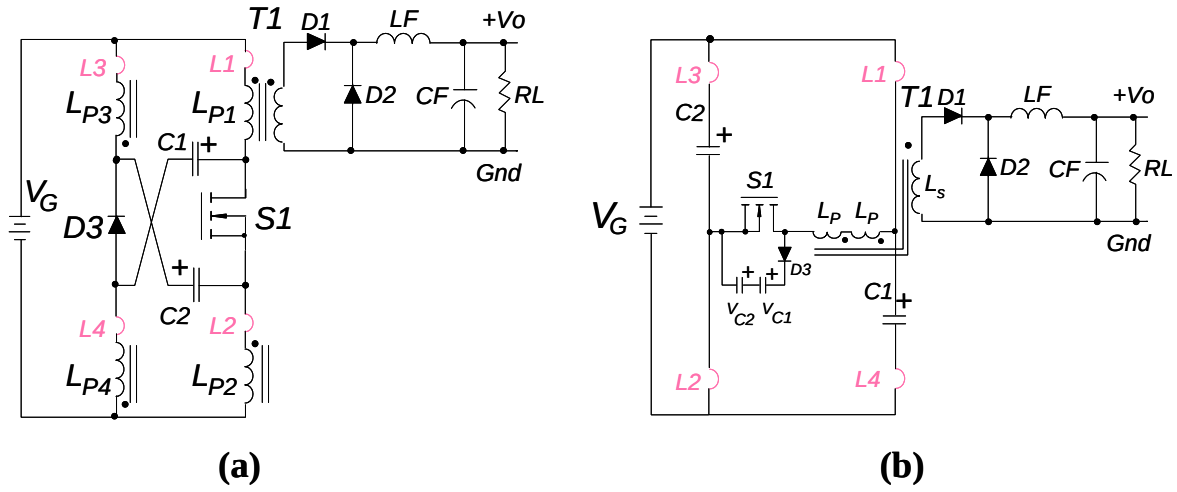


Fig. 3-9 Evolution of the FRC with an embedded low-pass filter.

The FRC is simplified by adding a pulsating current source to replace the forward converter power stage as illustrated in Fig. 3-10(a).

This filter can be characterized by the transfer gain T, defined as Eq. 3-32. Assuming the leakage inductances the clamp capacitors are equivalent to L and C, respectively.

$$T = \frac{V_{AB}}{V_G} = \frac{V_A - V_B}{V_G} \qquad \text{Eq. 3-32}$$

where V_A and V_B are derived as the following equations.

$$V_A = \frac{(j \cdot 2\pi \cdot f \cdot L_4) + R_L + R_C + \frac{1}{j \cdot 2\pi \cdot f \cdot C_1}}{j \cdot 2\pi \cdot f \cdot (L_1 + L_4) + 2R_L + R_C + \frac{1}{j \cdot 2\pi \cdot f \cdot C_1}} \cdot V_G \quad \text{Eq. 3-33}$$

$$V_B = \frac{j \cdot 2\pi \cdot f \cdot L_2 + R_L}{j \cdot 2\pi \cdot f \cdot (L_2 + L_3) + 2R_L + R_C + \frac{1}{j \cdot 2\pi \cdot f \cdot C_2}} \cdot V_G \quad \text{Eq. 3-34}$$

where R_C and R_L represent as the ESR of the capacitor and the transformer winding resistance.

The resonant frequency is defined as the following equation.

$$f_o = \frac{1}{2\pi\sqrt{2L\ C}} \quad \text{Eq. 3-35}$$

As illustrated in Fig. 3-10(b), three curves are plotted with different combinations of the L and C. From the transfer gain, therefore, the filter is classified as a low-pass filter. Unlike the notch filter in the FRR, a higher attenuation is obtained by designing a lower resonant frequency of the embedded low-pass filter.

Additionally, the selection of the capacitor voltage can be calculated by utilizing the following equations.

$$\mathrm{V_{DS}} = \mathrm{V_{C1}} + V_{C2} \quad \text{Eq. 3-36}$$

$$V_{C1(\max)} = V_{C2(\max)} = \mathrm{V_{C1(AVG)}} + \frac{1}{2}\Delta V_{C1} = V_G + \frac{1}{2}\frac{(1-D)D \cdot i_O}{2n \cdot C \cdot f_S} \quad \text{Eq. 3-37}$$

$$\mathrm{V_{DS}} = \mathrm{V_{C1}} + V_{C2} = 2\mathrm{V_G} + \frac{(1-D)D \cdot i_O}{2n \cdot C \cdot f_S} \quad \text{Eq. 3-38}$$

Therefore C_1 can be calculated with the following equation.

$$C = \frac{(1-D)D \cdot i_O}{2n \cdot f_S(\mathrm{V_{DS(max)}} - 2\mathrm{V_{G(max)}})} \quad \text{Eq. 3-39}$$

The capacitance is the function of several parameters, such as switching frequency f_S; load current, i_o; and the duty cycle, D.

Once the specifications and the switching frequency of the converter have been determined, L and C can be calculated from Eq. 3-35 and Eq. 3-39.

The design considerations are then the trade-offs between efficiency and the size of the capacitor. After determining the voltage stress on the main switch, a clamp capacitor is selected. However, a larger inductance is required to achieve a lower resonant frequency resulting in a longer turn-on transition time period, T_3 to T_4. As a result, the duty cycle loss is increased and the efficiency performance may be degraded if the turns ratio of the transformer is adjusted to meet the line and load regulation specifications. Many combinations of clamp capacitance and leakage inductance values are possible for a given application.

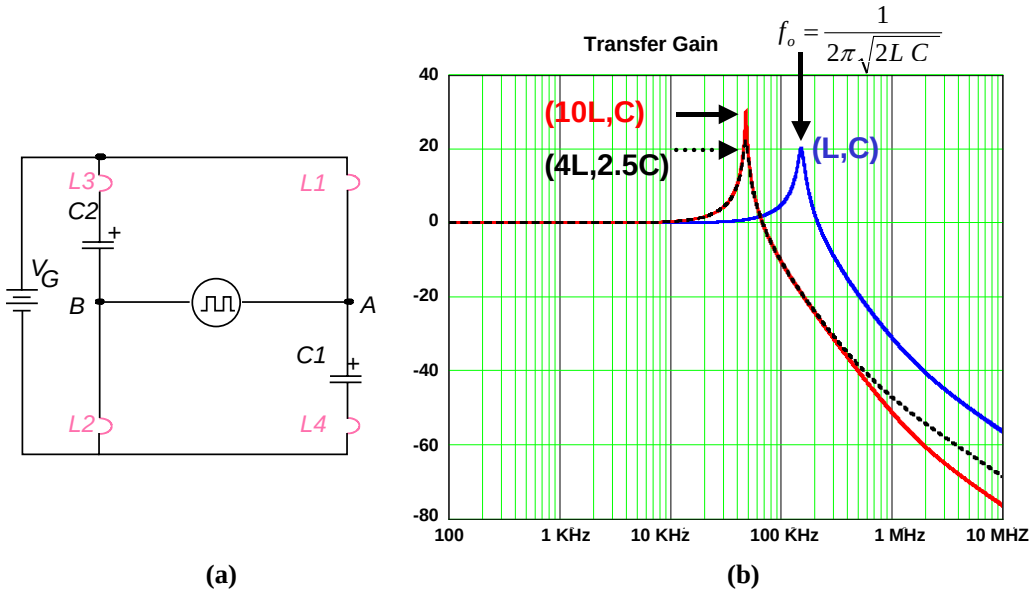


Fig. 3-10 (a) Circuit diagram of the low-pass filter derivation of the FRC, (b) Transfer gain of the embedded low-pass filter.

To demonstrate the benefits of the non-pulsating current waveform, a current spectrum harmonic component comparison is made among the FAC, the FRR, and the

FRC by utilizing the SABER simulation program, and the FRC has the best current spectrum performance as shown in Fig. 3-11.

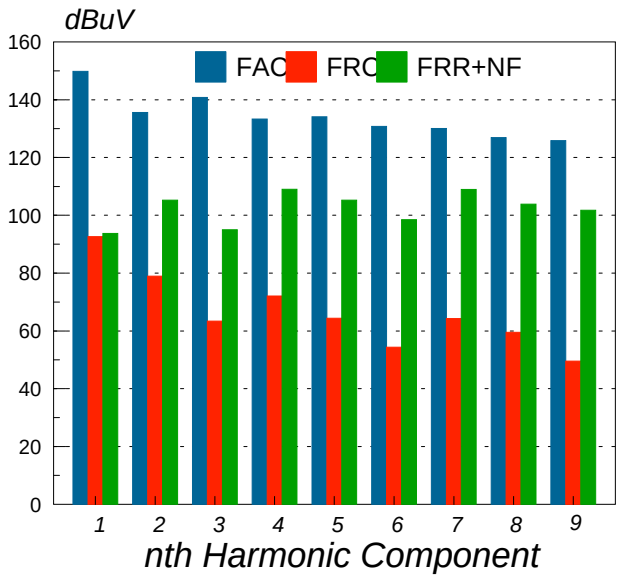


Fig. 3-11 Input current harmonic comparison of the FAC, the FRR with notch filter and FRC.

Consequently, the FRC has a continuous input current waveform with a small sinusoidal current ripple and has less $I_{CIN(RMS)}$. Further size reduction of the EMI filter is attainable.

3.6. Experimental Validation

In this section, a 40-60V input voltage range and 5V output voltage at 200W output power forward converter with current ripple cancellation (FRC) is implemented to illustrate the benefits obtained from the current ripple cancellation mechanism. The FRC operates at 150 kHz. The transformer was constructed with an ER35 core and a turns ratio of 3:3:3:3:2, which means that the effective turns ratio equals 3. The main switch is a Fairchild FQA55N25. The rectifier is a MOSPEC S60D60CJ with 0.75V forward voltage drop. The leakage inductance for each winding is 800nH and each clamp capacitor is 4.4uf.

Fig. 3-12 (b) shows the oscillograms of the FRC. All the waveforms were taken at V_{in} = 48V, V_o = 5V, and I_o = 20A operation conditions. Channel 2 shows the V_{DS} waveform of the primary switch. The voltage is clamped to twice the input voltages without any voltage spike.

The oscillogram of the input current, I_G, is shown in channel 4. Because the leakage inductances are not exactly identical, a small amount of pulsating current ripple can be seen.

An experimental result comparison is made between the FAC and the proposed forward converter with current ripple cancellation (FRC).

Fig. 3-13 shows the fundamental component spectra of the FAC and the FRC. In the FRC, the attenuation of the fundamental component spectrum is performed by the ripple cancellation mechanism. Therefore, the FRC has a lower fundamental component spectrum component than the FAC.

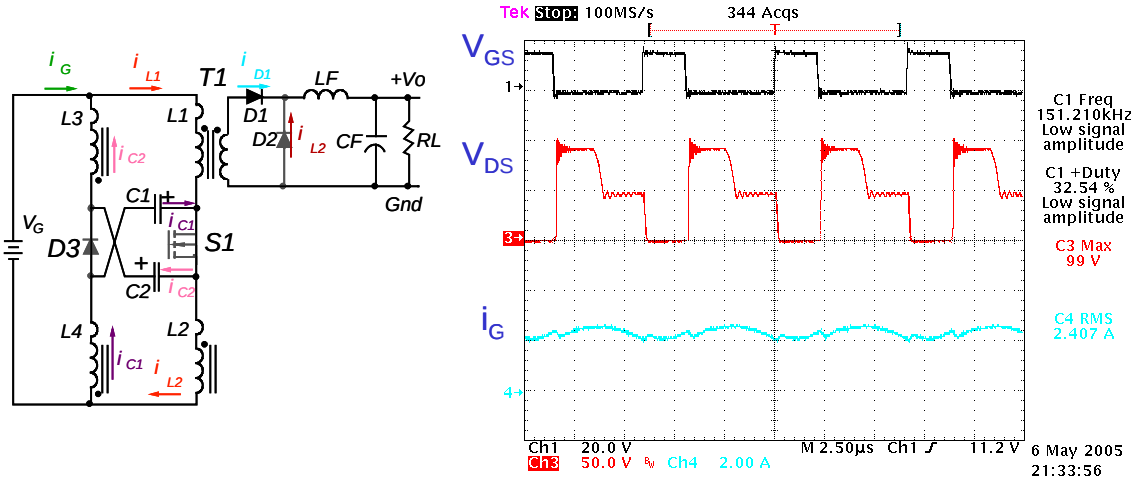


Fig. 3-12 Circuit diagram and key waveforms of the FRC.

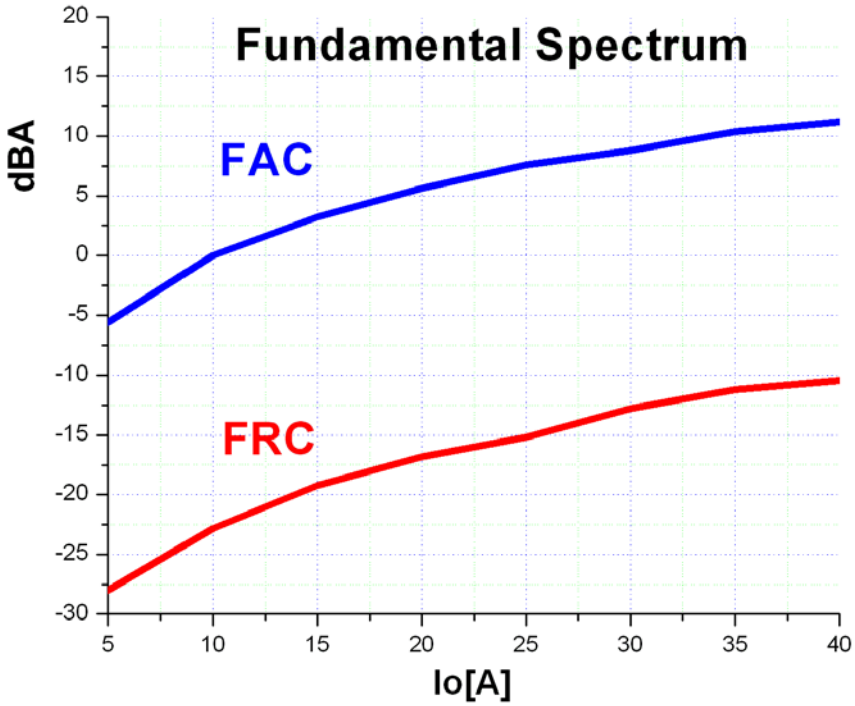


Fig. 3-13 Measured fundamental component of the input current i_G of the FAC and FRC.

As shown in Fig. 3-14, an efficiency comparison of three converters is made. Although the FRC has the highest light load efficiency, it operates with a limited duty cycle resulting in an increase in the conduction loss during heavy load operating conditions. Hence, the FAC has the best efficiency performance under full-load conditions.

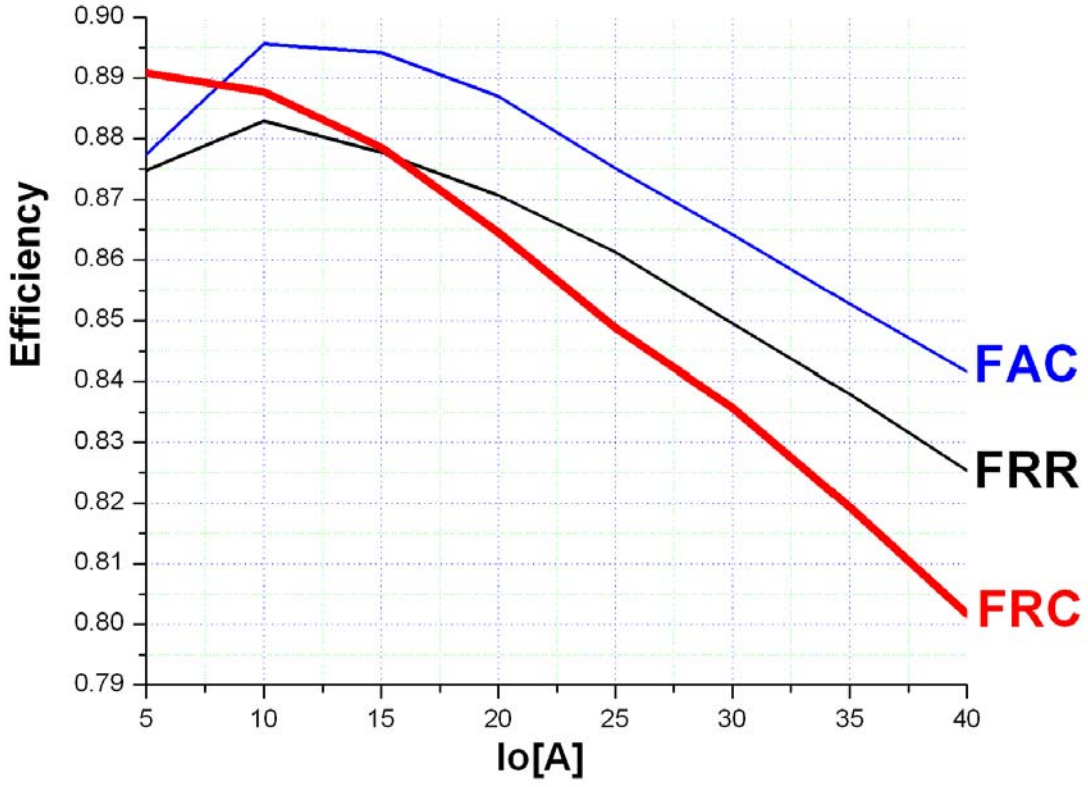


Fig. 3-14 Measured efficiency comparison of the three tested converters.

3.7. Summary

In this chapter, the proposed techniques are employed to achieve further converter performance improvements. Two sets of clamp capacitors and leakage inductances are utilized to realize a mirrored forward converter with current ripple reduction (MFRR) and the FRR. MFRR is obtained by mirroring the components of the FRR in an upside-down manner. After investigating the waveforms, the MFRR has the same circuitry behavior as the FRR. By connecting the FRC and MFRR in series- and -parallel, the current ripple reduction technique is applied to cancel the input current ripple. Therefore, a forward converter with current ripple cancellation (FRC) is presented and the operational principle is introduced.

Due to the non-pulsating input current, the EMI intensity is significantly reduced.

In addition to the analysis, several performance comparisons among the FRR, the FAC, and the FRC have been made by utilizing the SABER simulation program and the experimental results are collected to verified the performance of the FRC.

However, the efficiency of the FRR and FRC are inferior to that of the FAC. To overcome the low efficiency drawback, several topology extensions are derived in the next chapter.

Chapter 4 Improvements and Extensions of the Current Ripple Reduction and Current Ripple Cancellation Converters

4.1. Introduction

Among the existing forward topologies, the FAC has for decades been regarded as having the best performance and it serves as a benchmark in this research.

As illustrated in **Fig. 4-1**(a) and **Fig. 4-1**(b), the proposed FRR and FRC presented in Chapter 2 and Chapter 3 have several advantages over the FAC, such as the alleviation of EMI noise and fast dynamic response with minimum **component count.**

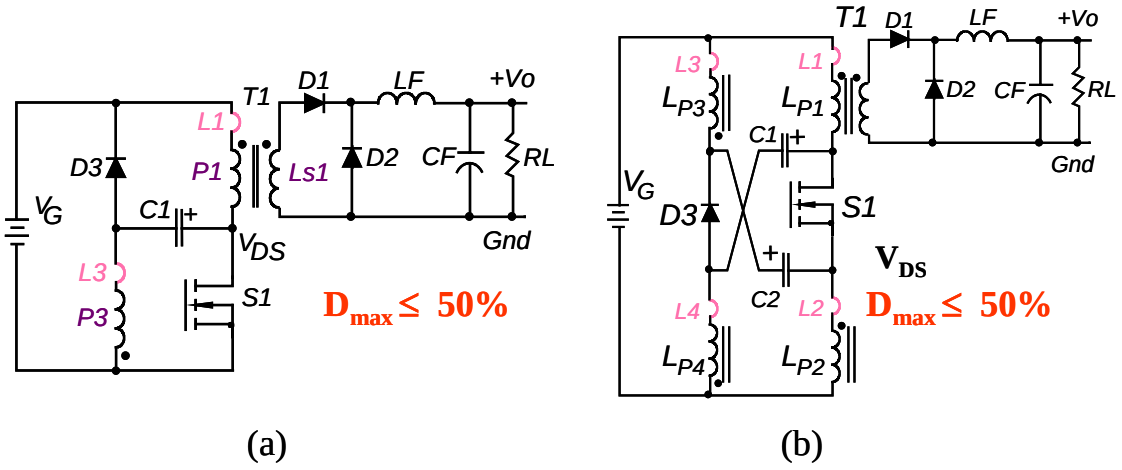


Fig. 4-1 Circuit diagram of (a) the FRR and (b) the FRC, the operating maximum duty cycles are limited to 50% due to the reset voltage being equal to the input voltage.

However, the maximum operating duty cycle of the FRR/FRC is limited to 50% to avoid saturating the transformer. A penalty is thus incurred to use a lower turns ratio of the transformer resulting in a higher primary RMS current. For example, a 3:1 turns ratio is used, as opposed to a 4:1 turns ratio in the FAC for 40-60V to 5V/40A power

conversion applications. Thus, the FRR and FRC have a higher primary RMS current as illustrated in Fig. 4-2(a) and Fig. 4-2(b). Meanwhile, due to the smaller turns ratio of the transformer, a higher voltage rating of the secondary rectifier diodes has to be used. Accompanied with a higher forward voltage drop, this higher voltage rating contributes another major conduction loss in the FRR and the FRC as shown in Fig. 4-2(d). Consequently, the proposed converters are inferior to the FAC with respect to efficiency.

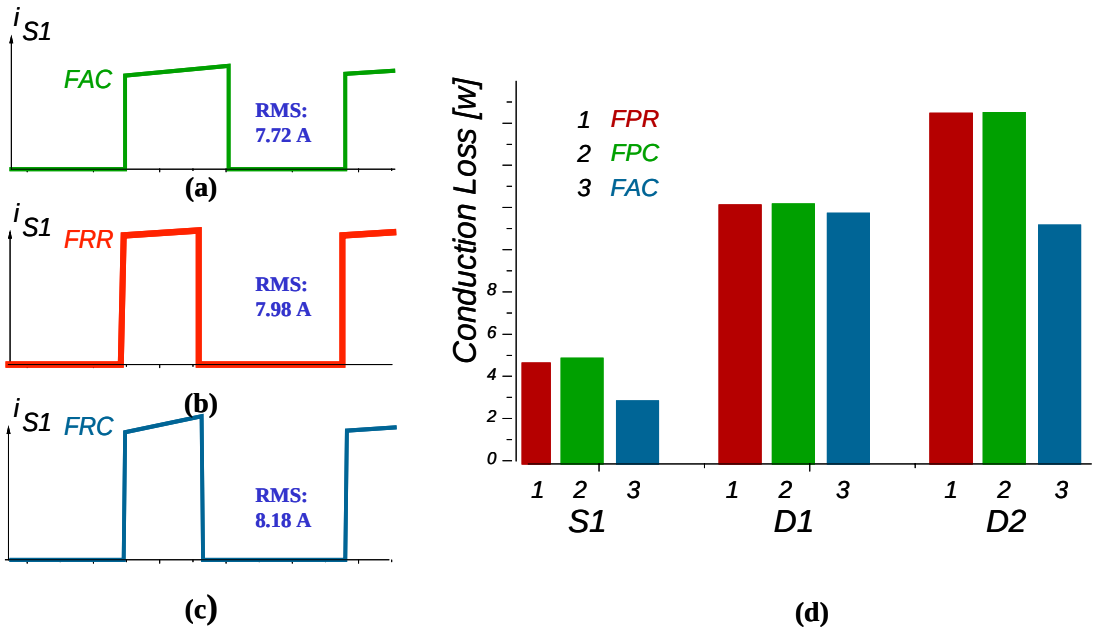


Fig. 4-2 Comparisons of the (a) RMS switch current i_{S1} and (b) semiconductor devices loss breakdown of the FRR, the FRC, and FAC.

Therefore, the extended operating duty cycle scheme is employed to enlarge the turns ratio of the transformer so that the primary RMS current and the voltage rating of the rectifier diode can be reduced.

On the other hand, the reduction of the equivalent $R_{DS(on)}$ by the series-connecting device technique can be also applied to improve the efficiency.

In this chapter, employing the techniques of extended duty cycle and series-connected semiconductor devices, several extended topologies of the FRR and FRC are proposed to achieve improvement in efficiency performance.

Moreover, by using a bilateral inversion technique, both ripple reduction and embedded filter techniques can be applied to the isolated PWM boost converter. The output current ripple is thus reduced, and size reduction of the output capacitor is attainable.

4.2. Efficiency Improvement by Extending Duty Cycle Scheme

To improve the converter efficiency, the turns ratio of the transformer becomes a key factor. Not only can increasing the turns ratio decrease the primary current, but can also reduce the voltage stress on the secondary rectifier. Consequently, the reduced conduction loss results in improving the efficiency of the converter. To extend the operating duty cycle beyond 50%, an extended duty cycle FRR (XFRR) is proposed and two existing topologies, the push-pull forward converter (PPF) and the symmetrical push-pull power converter (SPPPC) are investigated. The PPF and the SPPPC have been proposed by Xunwei Zhou [68] and Edward Herbert [64], respectively. All three converters can operate beyond a 50% duty cycle resulting in more efficient performance.

Having current ripple reduction and the current ripple cancellation properties, accordingly, the PPF and the SPPPC can be regarded as the members of the FRR and FRC families and will be presented in the next three sub-sections.

4.2.1. Extended Duty Cycle Forward Converter with Current Ripple Reduction (XFRR)

As illustrated in Fig. 4-3(a), an extended duty cycle forward converter with current ripple reduction (XFRR) is proposed to obtain a larger turns ratio, because the maximum operating duty cycle can be up to 66%. In addition to modifying from the FRR with two central-taping primary windings, L_{p1}-L_{P2} and L_{p3}-L_{p4}, with the same number of the turns for each winding, two more components, C_2 and D_4 are added. Due to the turning on of D_3 and D_4, the reset voltage is provided by input voltage V_G or clamp capacitor voltage, V_{C1} and V_{C2}. The transformer primary winding, L_{P4}, L_{P2} or L_{p3}, are applied with input voltage because $V_{C1}=V_{C2}=V_G$. Therefore, the core reset-voltage becomes $2V_G$ and up to 66% duty cycle can be operated without saturating the transformer. However, this topology suffers from $3V_G$ voltage stress on the main switch S_1 as illustrated in Fig. 4-3(b).

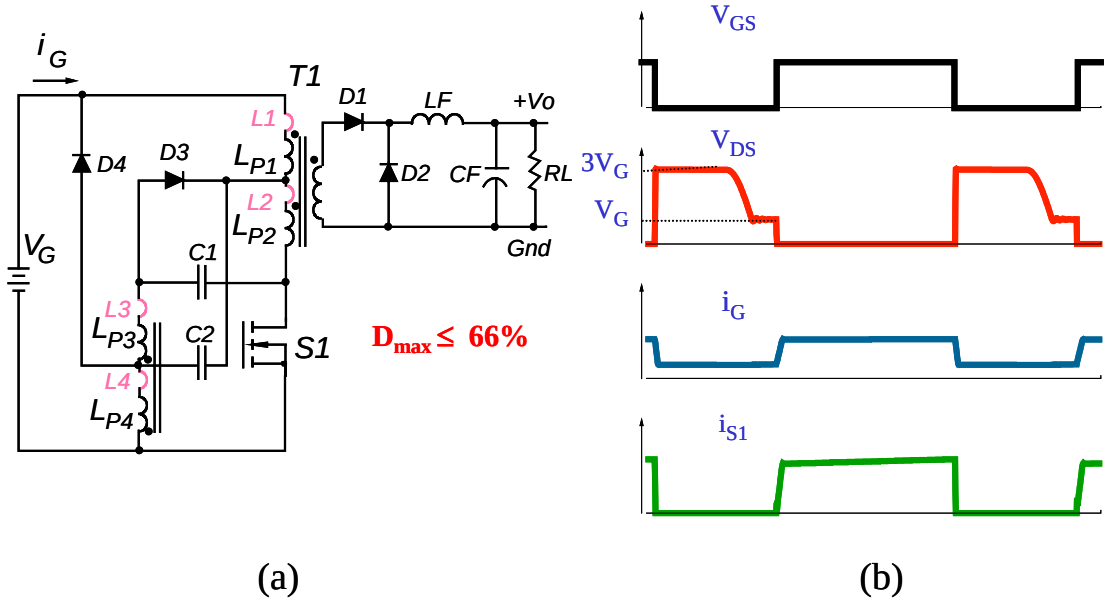


Fig. 4-3 (a) Circuit diagram and (b) key waveforms of the FRR with extended duty cycle.

Therefore, the 4:1 turns ratio can be used as the FAC in the 40-60V 5V/40A DC-DC applications. Because the RMS primary current and the voltage stress of the secondary rectifier would be the same as that of the FAC, the conduction losses of the semiconductor devices are decreased and the efficiency can be improved.

Moreover, the XFRR has double notch frequencies, $f_{N1}=1/\left(2\pi\sqrt{(L_2+L_4)C_2}\right)$ and $f_{N2}=1/\left(2\pi\sqrt{(L_3+L_4)C_1}\right)$. By setting theses two notch frequencies to approach to the switching frequency, such as 137KHz and 150 KHZ, a better notch filter performance can be obtained as illustrated in Fig. 4-4. Compared to the FRR, the XFRR has wider notch band and an 8dB improvement at switching frequency 150 KHz as shown in Fig. 4-4(c) and Fig. 4-4 (d).

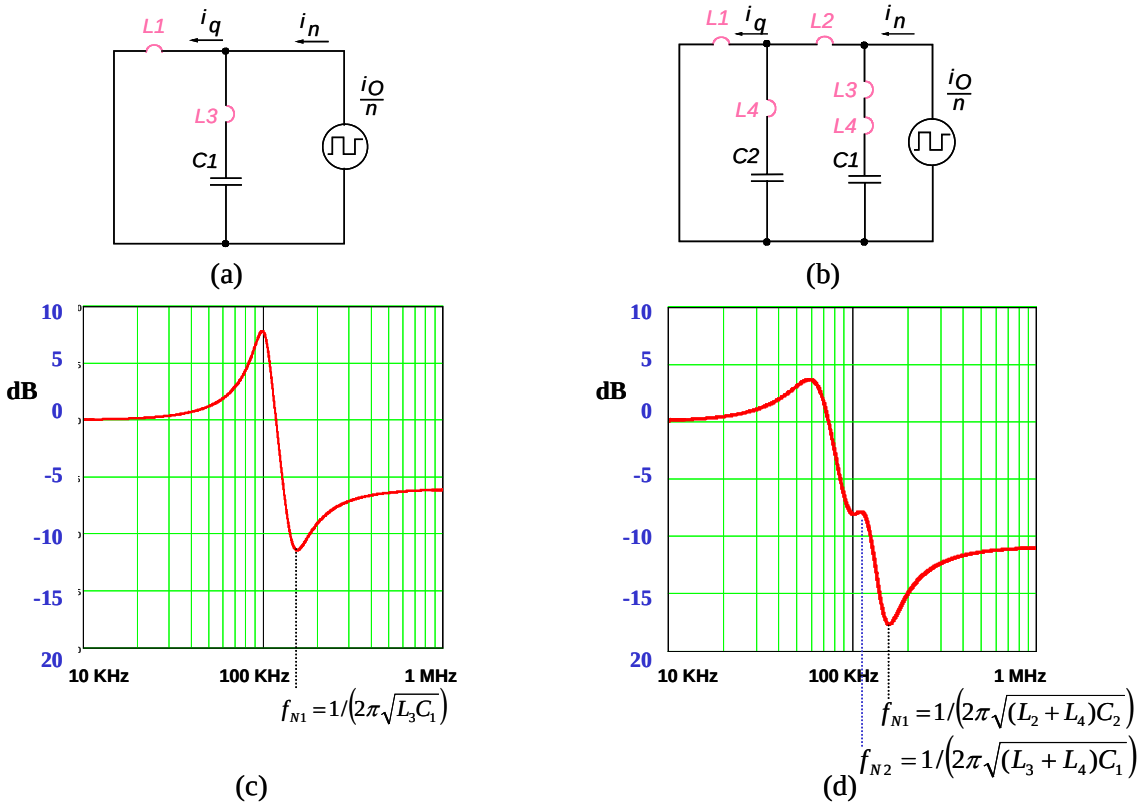


Fig. 4-4 (a) Equivalent circuit of the FRR notch filter and (b) equivalent circuit of the XFRR notch filter (c) notch filter transfer gain of the FRR and (d) notch filter transfer gain of the XFRR.

4.2.2. Push-Pull Forward Converter (PPF)

To extend the operating duty cycle beyond 50%, a full-bridge or a push-pull circuit is used. Because of its fewer power devices and simple control scheme, the push-pull converter is more popular than the full-bridge. It is realized by employing the interleaved technique on the two existing forward converters. However, the voltage spikes and the flux unbalance in the transformer become two major problems in a push-pull converter.

In contrast, there are no voltage spike or flux unbalance problems by employing the interleaved technique to the FRR. However, two identical converters make the circuit implementation of the FRR complicated and increase the cost of the converter.

Instead, a simple circuit can be realized by employing the interleaved technique to the FRR with its mirror circuit (MFRR); a push-pull forward converter (PPF) is thus derived as shown in Fig. 4-5.

It should be noted that the body diodes of the MOSFET are used as the clamp diode during its off time interval.

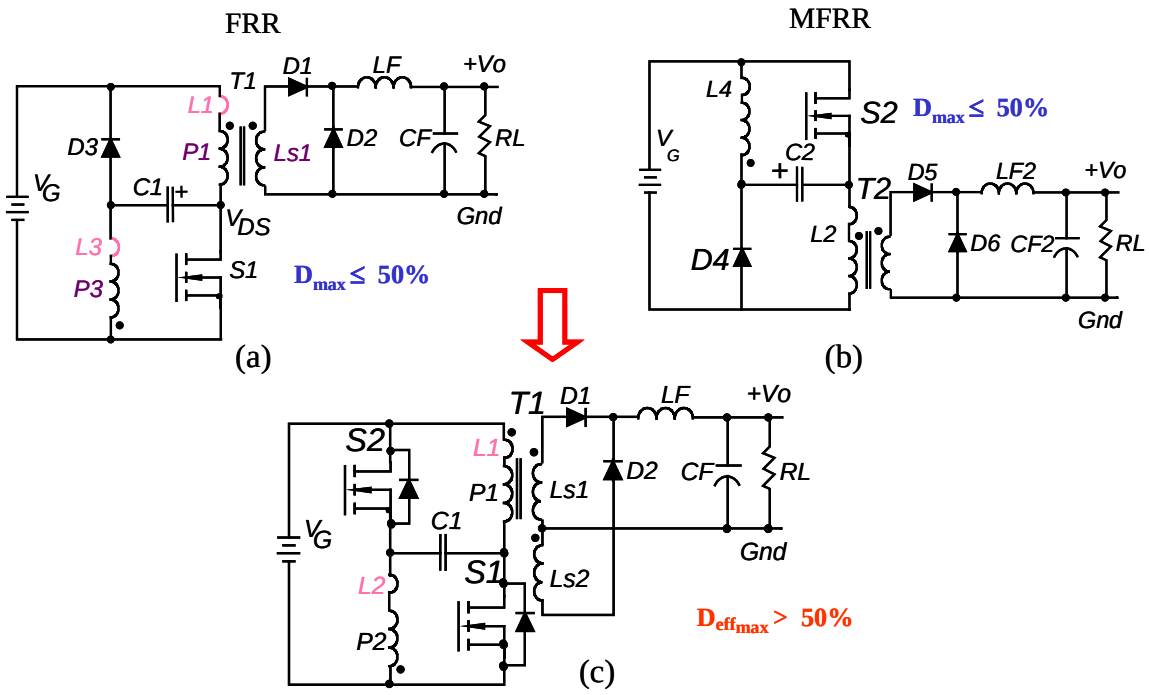


Fig. 4-5 Circuit diagrams of (a) the FRR and (b) the MFRR and the derivation of (c) the PPF.

Several advantages of the PPF over the push-pull converter have been explored by the authors [68], such as the switch being free of voltage spikes, the transformer operating symmetrically without a flux unbalance problem, and the input current ripple reduction making the design of using a smaller input filter. However, the embedded notch filter feature is not explored.

As illustrated in Fig. 4-6(a)-(d), the main switch current i_{S1} waveforms of the four converters, the FAC, FRC, FRR and PPF, are plotted, and their individual RMS current values are obtained by utilizing the SABER program. Because the effective duty cycle is extended beyond 50% resulting in a larger turns ratio; alarger turns ratio, for example, 5:1 can be used for the same DC-DC power conversion applications.

Because the primary RMS current of the PPF is shared by the two MOSFETs and the lower voltage rating of the secondary diode can be used with lower voltage drop, the

PPF has the lowest conduction losses among the four topologies as illustrated in Fig. 4-6(e).

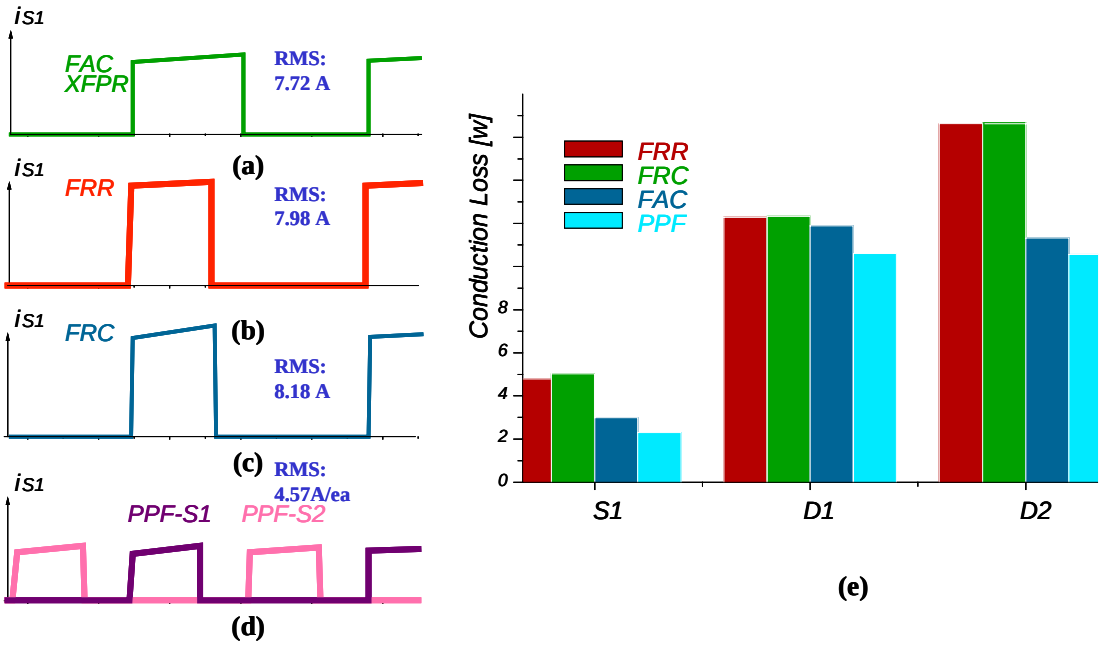


Fig. 4-6 Comparisons of the (a)-(d) RMS switch current i_{S1} and (e) semiconductor devices loss breakdown of the FRR, the FRC, FAC, and the PPF.

To demonstrate the efficiency performance, a 40-60V input voltage, 5V output-voltage and 200W output power operating at 150kHz PPF was implemented.

Because the equivalent duty cycle is greater than 50%, the turns ratio of the transformer is 5:1 in the PPF. The MOSFET has low RMS current and the rectifier diodes experience lower voltage stress. Both factors contribute to the efficiency improvements and make the PPF the most efficient among the four converters as illustrated in Fig. 4-7.

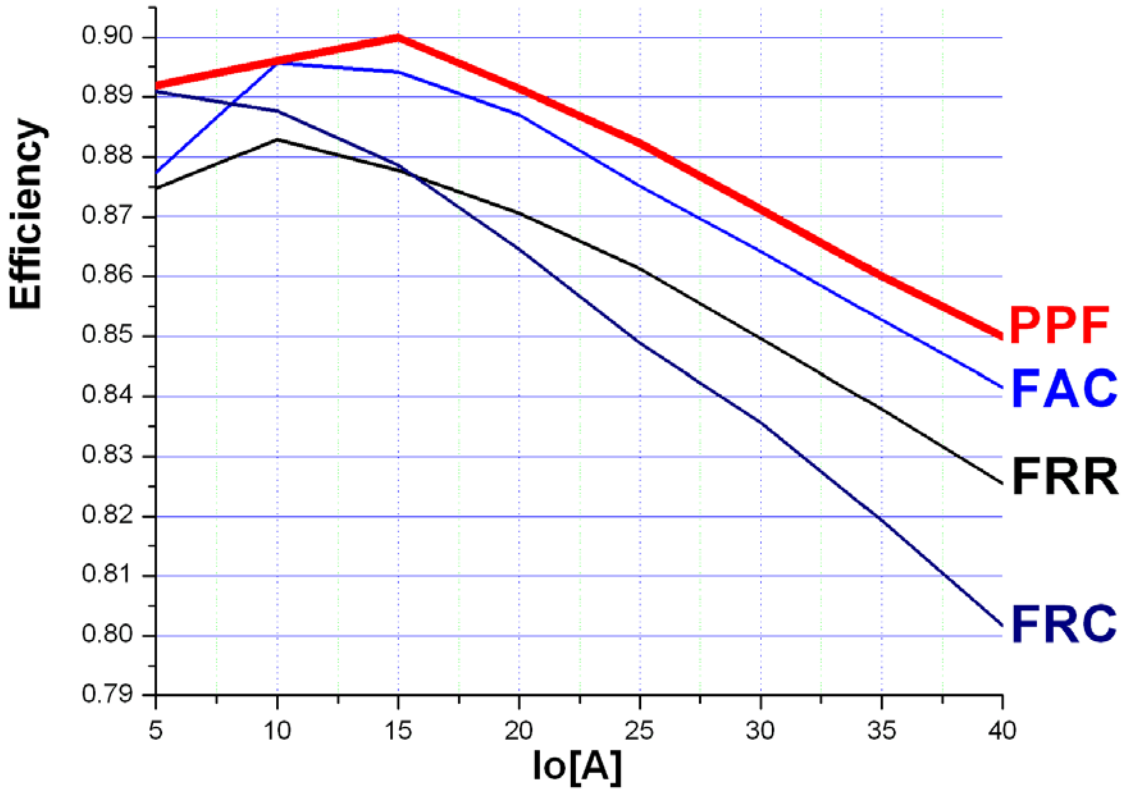


Fig. 4-7 (a) Measured efficiency comparison and (b) modified efficiency comparison with compensating LC filter loss of the four tested converters.

4.2.3. Symmetrical Push-Pull Power Converter (SPPPC)

Again, the operating duty cycle can be extended by employing the interleaved technique to the FRC and MFRC as shown in Fig. 4-8(a) and (b). A symmetrical push-pull power converter (SPPPC) can be derived as shown in Fig. 4-8(c). This was proposed by Edward Herbert in 1989 [64].

The author has observed that the converter has a near zero input current ripple performance and his explanation is focused on the equivalent L-C input filter formed by the input lead inductance and the floating capacitors. However, the ripple cancellation mechanism is not fully explored.

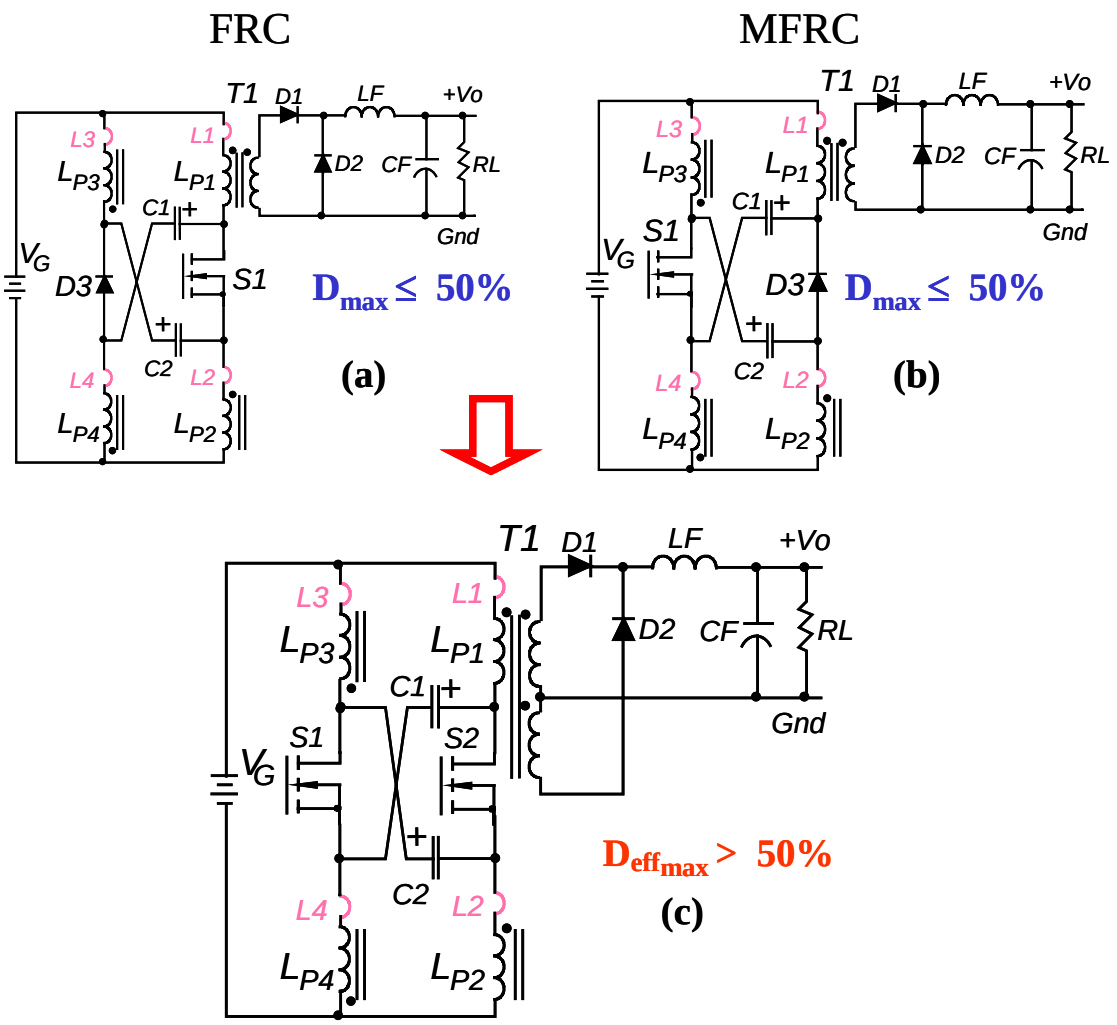


Fig. 4-8 Circuit diagrams of (a) the FRC and (b) the MFRC, and the evolution of (c) the symmetrical push-pull power converter.

Recently, this topology was implemented as the improved push-pull forward converter [71]. Instead of using as the transformer, the magnetic is used as the coupled inductor for non-isolated VRM applications. The input current is almost flat because the two windings that conduct the input current ripple s cancel each other out by employing the integrated magnetic technique. Therefore the input filter is a built-in function of this new topology, and the leakage inductances of the primary side windings are utilized as the input filter.

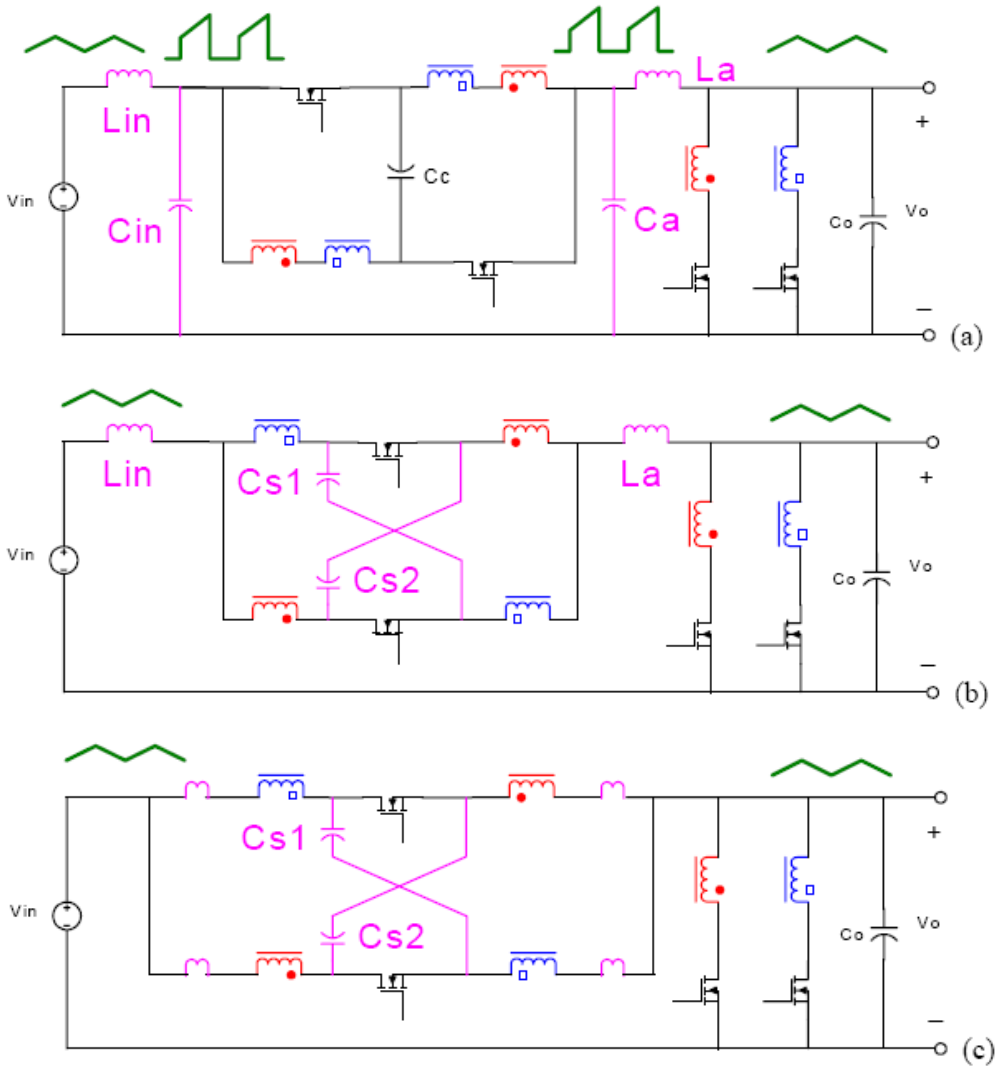


Fig. 4-9 Integration of L-C filters in multiphase coupled buck converter: (a) with additional L-C filters, (b) capacitor shifting, and (c) inductor shifting / courtesy of Peng Xu [71].

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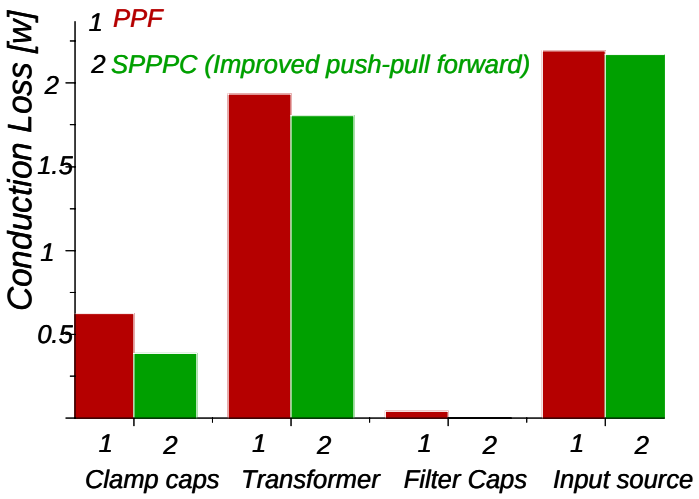
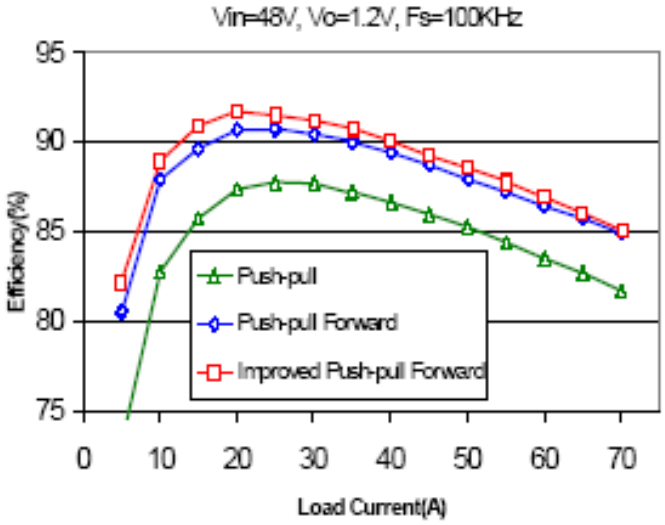
The loss breakdown of the PPF and the symmetrical push-pull power converter (SPPPC) are obtained by utilizing the SABER program, and is illustrated in Fig. 4-10(a). Because reflected load current waveforms and the current RMS values are equivalent to each other, the comparison focuses on the minor factors only, such as capacitor current and the transformer winding losses. Both converters have been successfully implemented as the voltage regulator module (VRM) for computer applications and the efficiency of

the three VRMs is measured and illustrated in Fig. 4-10(b) [71]. As these figures show, the improved push-pull forward has the highest efficiency for the entire load range.



(a)



(b)

Fig. 4-10 (a) Loss breakdown and (b) efficiency comparison between the PPF and improved push-pull forward converter / courtesy of Peng Xu [71].

4.3. Efficiency Improvement by Reducing Voltage Stress

In addition to the extended duty cycle scheme, the series-connected switch technique is a scheme that can be used to improve efficiency.

As shown in **Fig. 4-11**(a) and **Fig. 4-11**(b), the voltage stresses on the MOSFET are twice the input voltage in the FRR and FRC converters. Switches with amply high voltage ratings are available for DC-DC applications. However, a higher-voltage-rated switch would tend to have a higher on-resistance, resulting in increasing conduction losses. To take advantage of a low-voltage-rating MOSFET with low R_{DSON}, the series-connected switch technique can be used as an efficiency improvement scheme. For example, two low-voltage rating MOSFETs (500V, 0.07Ω, SPW52N50C3, Infineon) in series have a lower equivalent $R_{DS(on)}$ than that of a single high-voltage MOSFET (800V, 0.29Ω, SPA17N80C3, Infineon or 900V, 0.95Ω, FQA11N90, FAIRCHILD), for off-line DC-DC applications. This **allows less conduction loss.**

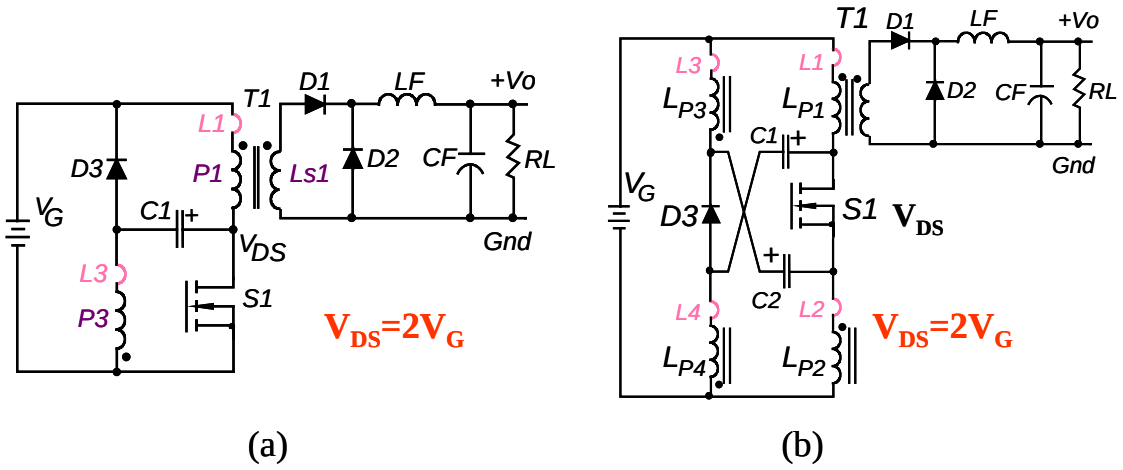


Fig. 4-11 Circuit diagram of (a) the FRR and (b) the FRC, the MOSFET suffers from $2V_G$ voltage stress in both converters.

However, how to guarantee voltage balance among the devices at both the static and the dynamic transient states is the main problem associated with the series-connected devices technique. Therefore, an additional voltage clamp network should be added.

Thanks to a simple and reliable voltage clamped circuit provided by the clamp capacitor in the FRR and FRC, a two-switch forward converter with current ripple

reduction (2S-FRR) and a two-switch forward converter with current ripple cancellation (2S-FRC) can be proposed. Two clamp diodes are added to ensure the voltage balance between the two series switches at both static and dynamic states. Consequently, the voltage stress of the 2S-FRR and the 2S-FRC on the MOSFET are reduced to the input voltage. Although the circuit complexity and parts count are increased, this is a small price to pay for the benefits gained by using this technique.

4.3.1. Two-Switch Forward Converter with Current Ripple Reduction (2S-FRR)

To achieve the properties of input current ripple reduction and low-voltage stress, two FRR converters can be connected in series. However, the complicated circuitry hinders its applications.

In contrast, by employing the series-connected switch technique, a two-switch FRR is proposed as shown in Fig. 4-12. An embedded clamp voltage circuit is provided by the clamp capacitor with adding two additional clamp diodes, D_{C1} and D_{C2}. As illustrated in Fig. 4-12(b), the voltage across S_1 or S_2, V_{DS1} and V_{DS2}, are clamped to the input voltage by turning-on D_{C1} and D_{C2}. Therefore, the voltage sharing between the two series-connected switches is well utilized during both the static and the dynamic transient states.

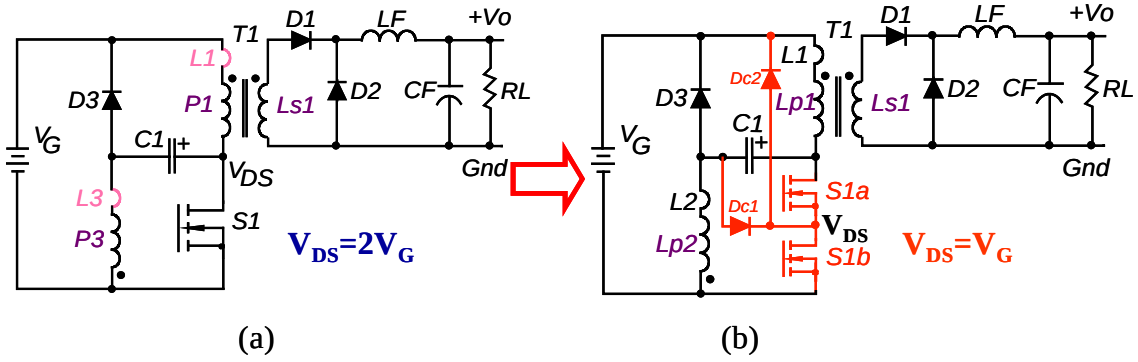


Fig. 4-12 (a) Circuit diagram of the FRR and (b) the 2S-FRR is derived by employing the series-connected devices technique.

A 270-330V input and 10V output voltages at 200W output power 2S-FRR operating at 100 kHz was implemented.

The transformer was constructed with an SP35 core and 33:33:3 turns ratio, which means that the effective turns ratio equals 11.

The main switches are Toshiba K2837. The rectifier is a C30P10Q. The clamp capacitance and C_{in} are 1uf. The primary windings use 0.55 ϕ wires and the secondary winding use 0.1 ϕ * 60 * 3.

Two extra diodes, D_4 and D_5, are added to assure voltage sharing between S_1 and S_2. Because V_{DS} is clamped to $2V_{in}$, the maximum voltage across each switch is thus limited to V_{in}.

The oscillograms of the prototype 2S-FRR are shown in Fig. 4-13. All the waveforms were taken for V_{in} = 300 V, D=0.42, V_o = 10.0 V, and I_o = 20 A

Fig. 4-13(a) shows the current waveform of I_{in}. During the on time interval, the input capacitor, C_{in}, is discharged to transfer energy to load and charged from the source in the off time interval, as shown in Fig. 4-13 (b). This small capacitor shapes the input current to a sinusoidal waveform.

The oscillogram of I_{in1} is shown in Fig. 4-13 (c). Due to the input current ripple reduction property, the current ripple reduces to one half of reflected load current and the noise problems of the converter can be alleviated. I_{in1} is almost the same as Fig. 4-13(d), I_{P1}, except for a small current spike introduced by the turning-on of the clamped diode, D_3. When the main switches are turned on, the current increases linearly from 300mA to 1.5A to provide the desired output currents. During the off time interval, the current drops abruptly to 300mA because of the turning off the forward diode, D_1, in the secondary. In the rest time interval, it charges capacitor C_1.

Unlike the waveform of I_{P1} (higher than zero), I_{P3} is between 600mA and -600mA as shown in Fig. 4-13 (e). I_{P3} represents charge balance on the clamp capacitor, C_1.

As shown in Fig. 4-13 (f) and Fig. 4-13 (g), S_1 and S_2 are turned on simultaneously. However, because of the difference between diver layout path and the MOSFET's characteristics, they will not turned off at the same time. V_{DS1} as well as V_{DS2} are clamped to the input voltage, and the voltage-sharing function is done well due to the turning-on of D_{C1} and $D_{C2.}$ Moreover, the spike-free voltage waveforms at the on/off transitions instant confirm that the leakage inductance energy is effectively absorbed.

Also, as shown in Fig. 4-13 (h) and Fig. 4-13 6(j), the clamped diodes, D_3, D_{C1} and D_{C2}, are turned on at the same time to perform the voltage-clamped and voltage-sharing functions.

Fig. 4-13 (k) and Fig. 4-13 (l) show the waveforms of I_{D1} and I_{D2}, respectively. Current overlap occurs at both on/off transition instants.

Finally, the efficiency of the power stage of the 2S-FRR has been measured under different load and input range operating conditions, as shown in Fig. 4-14. A maximum

efficiency, 88.1%, is achieved under low-line and 60% full-load condition. The converter efficiency can be improved for the following reasons:

1. The conduction losses in the primary side are decreased due to the low RMS input current and the low $R_{DS(on)}$ MOSFET used.

2. Before the switch is turned on, the voltage across each switch is one half of the input voltage and the switching turn-on losses are expressed as the following equation.

$$2 \cdot (\frac{1}{2} \cdot C_S \cdot {V_{DS}}^2) = 2 \cdot (\frac{1}{2} \cdot C_s \cdot \left(\frac{1}{2} V_{in}\right)^2) = \frac{1}{2} \cdot \left(\frac{1}{2} \cdot C_s \cdot {V_{in}}^2\right) \quad \text{Eq. 4-1}$$

Consequently, the switching turn-on loss is reduced to one-half that of single-switch forward topology.

3. Due to the clamp capacitor, the leakage inductance energy is stored and transferred to the load.

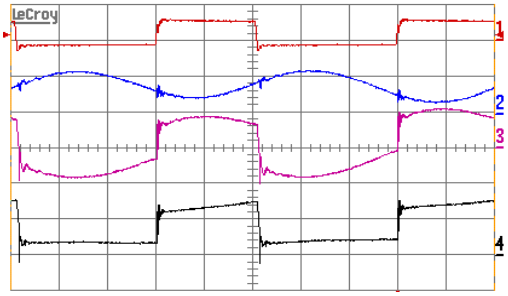
Because the voltage stress is equal to the input voltage, the proposed 2S-FRR is suitable for off-line power conversion applications

V_{GS} (20V/div)

(a)I_{in} (1A/div)

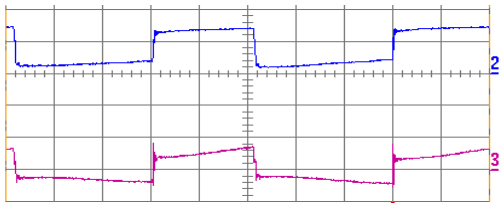
(b) I_{cin} (1A/div)

(c) I_{in1}(1A/div)



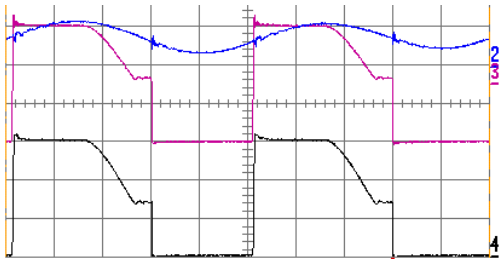
(d)I_{P1A} (1A/div)

(e) I_{P3} (1A/div)



(f) V_{DS1} (100V/div)

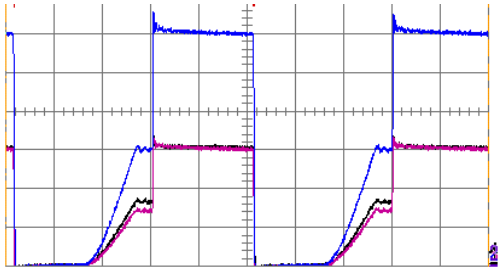
(g) V_{DS2} (100V/div)



(h) V_{D3} (100V/div)

(i) V_{DC1} (100V/div)

(j) V_{DC2} (100V/div)



V_{DS1} (100V/div)

(k) I_{D1} (10A/div)

(l) I_{D2} (10A/div)

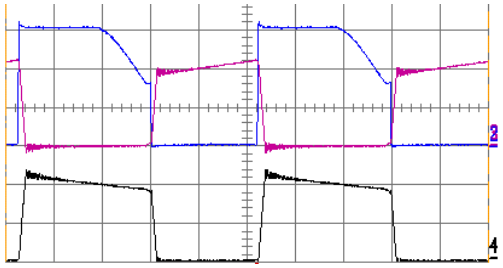


Fig. 4-13 Oscillograms of the 2S-FRR.

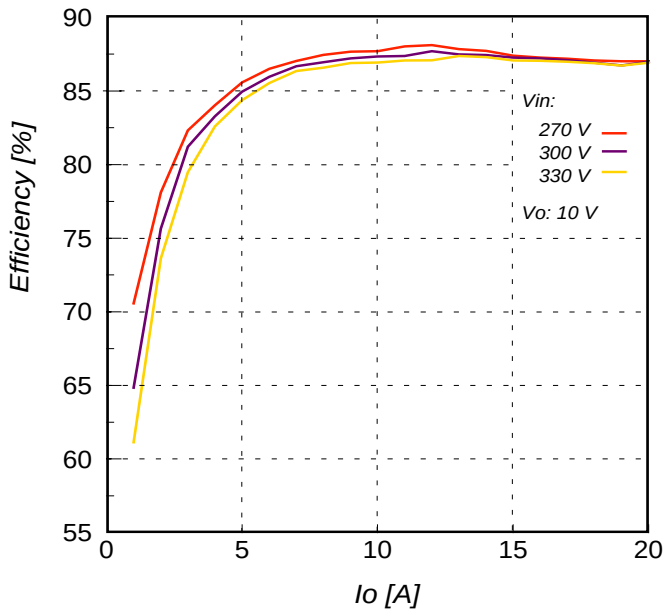


Fig. 4-14 Measured efficiency of the power stage of the prototype 2S-FRR.

4.3.2. Two-Switch Forward Converter with Current Ripple Cancellation (2S-FRC)

To achieve the non-pulsating input current and low-voltage-stress properties, two FRC converters can be connected in series. However, the complicated circuitry hinders its applications.

On the other hand, a simple two-switch forward converter with current ripple cancellation (2S-FRC) is proposed and shown in Fig. 4-15(b) [67]. An embedded clamp voltage circuit is provided by the clamp capacitors, C_1 and C_2, while adding two additional clamp diodes, D_{C1} and D_{C2}. The voltage V_{DS1} and V_{DS2} across S_1 or S_2, are clamped to the input voltage by turning-on the D_{C1} and D_{C2}. Therefore, the voltage sharing between the two series-connected switches is well utilized both at the static and the dynamic transient states.

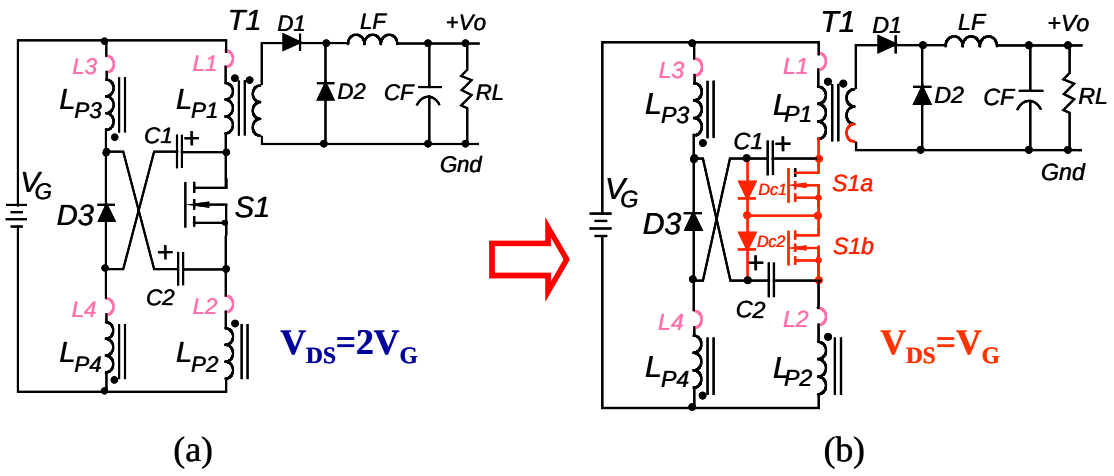


Fig. 4-15 (a) Circuit diagram of the FRC (b) the derivation of the 2S-FRC.

A 270-330 V input and 5V output voltage at 100W output power 2S-FRC operating at 100 kHz was implemented. The transformer was constructed with 30:30:30:30:3 turns ratio, which means that the effective turns ratio equals 20.

The main switches are IRF740. The rectifier is a 62CNQ45. The clamp capacitors are 2.2uf. The primary windings use #26 AWG wires and the secondary winding use copper foil.

Fig. 4-16 (a) - Fig. 4-16 (k) show the oscillograms of the prototype converter. All the waveforms are taken for V_{in} = 300 V, D=0.39, V_o = 5.0 V, and I_o = 10 A.

S_1 and S_2 are turned on and off simultaneously. As shown in Fig. 4-16(a) and Fig. 4-16(b), the spike-free voltage waveforms at the on/off transition instant confirm that the leakage inductance is effectively stored. Also, the voltage across each switch is clamped to the input voltage, while the clamped diode, D_{C1} and D_{C2}, are turned on, as shown in Fig. 4-16(c).

The input current I_{in} has a 175mA DC value with a 100mA current ripple, as shown in Fig. 4-16(d). Instead of the pulsating shape as that of the conventional two- switch

forward converter, the input current of the 2S-FRC maintains in a non-pulsating sinusoidal waveform due to the ripple cancellation mechanism.

The oscillogram of I_{Lp1} or I_{LP3} is shown in Fig. 4-16(i). When the main switches are turned on, the oscillogram increases linearly from 40mA to 380mA. During the off time interval, it drops abruptly to 120mA because of the turning off the forward diode, D1, in the transformer secondary. In the rest time interval, it charges the capacitors, C_1 or C_2.

Unlike the waveform of I_{Lp1} or I_{LP3} (higher than zero), I_{Lp3} or I_{Lp4} is between 150mA and -155mA as shown in Fig. 4-16(j). It represents the charge balance behavior of the clamp capacitors, C_1 and C_2.

Like the 2S-FRR, the low voltage stress makes the proposed 2S-FRC suitable for off-line power conversion applications.

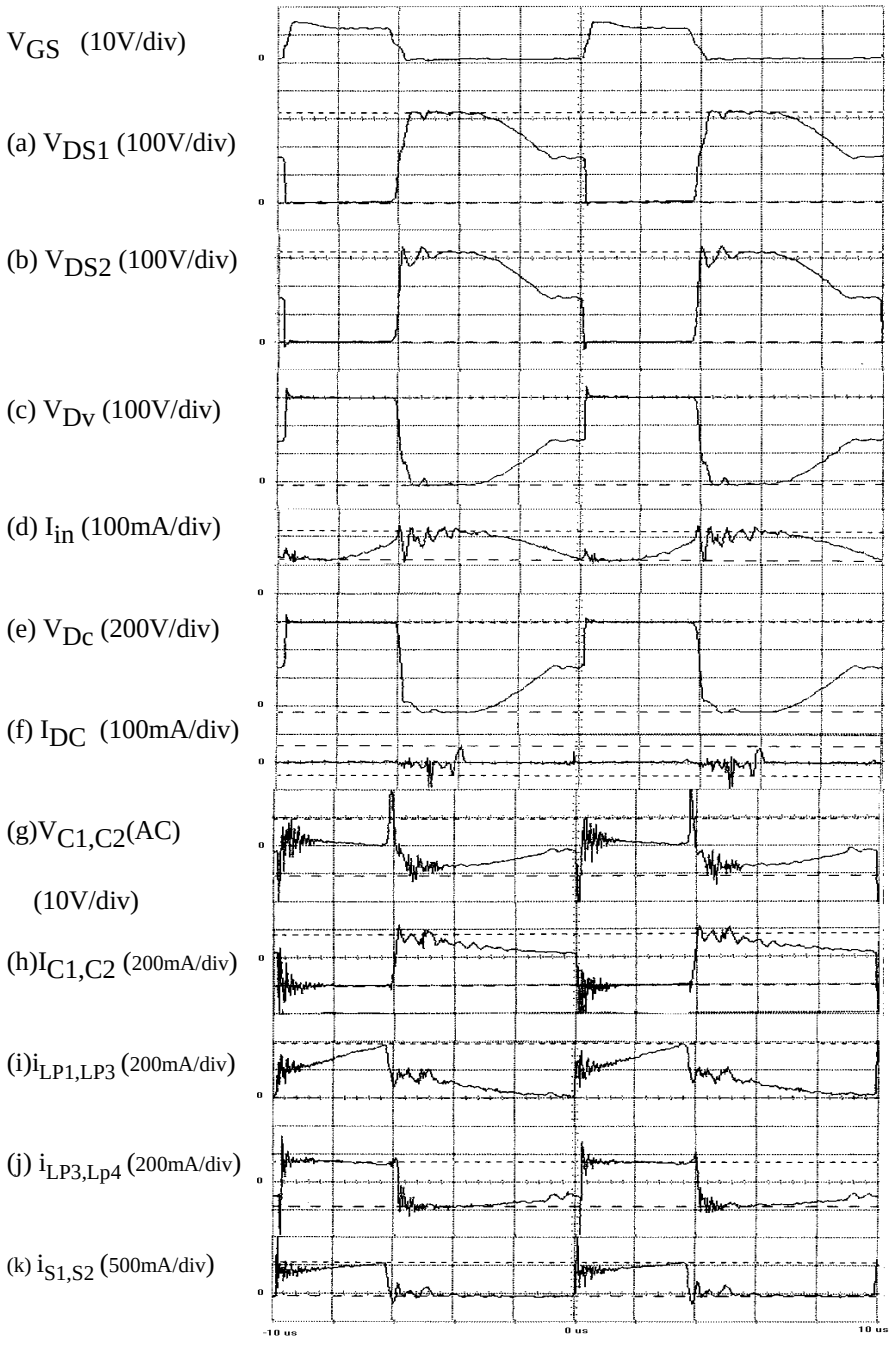


Fig. 4-16 Measured key waveforms of the prototype of the 2S-FRC.

4.3.3. Four-Switch Forward Converter with Current Ripple Cancellation (4S-FRC)

Illustrated in **Fig. 4-17**(a), each MOSFET is clamped to the input voltage during its off time. By series-connecting two 2S-FRC converters, a four-switch forward converter with current ripple cancellation (4S-FRC) is proposed to further reduce the voltage stress as illustrated in Fig. 4-17(b). Based on the FRC with the series-connection of the primary circuitry, the voltage stress of each switch is shared equally to 1/2 V_G thanks to the help of the clamp capacitors and the clamp diodes.

A 360-400V input 5V output voltage 100W output power 4S-FRC was implemented. It operates at 100 kHz. The transformer has a 20:40:20:20:40:20:3 turns ratio, which means that the effective turns ratio equals 80/3. The main switches are IRF644s (250V). The rectifier is a 62CNQ45. The clamp capacitors are 4.7uf. The primary windings are #26 AWG wires and the secondary windings are copper foil.

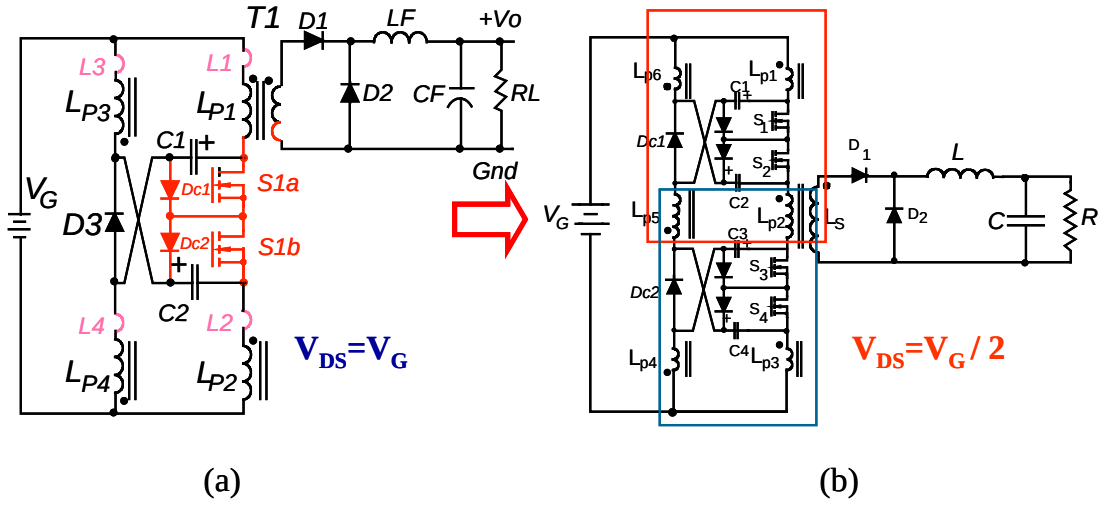


Fig. 4-17 Circuit diagram of (a) the 2S-FRC and (b) the 4S-FRC.

The oscillograms of the prototype converter are shown in Fig. 4-18 through Fig. 4-20. All the waveforms were taken with V_G = 400V, V_O = 5V, and I_O = 10A.

The voltage between the drain and source of each MOSFET is shown in **Fig. 4-18**. Four main switches, S_1-S_4, are turned on and off simultaneously. The spike-free voltage waveforms at the on/off transition instant confirm that the leakage inductance is effectively stored in the clamp capacitor. In addition, voltage sharing is achieved due to the clamp diodes turning on and the voltage across each switch being clamped to one-half the input voltage. The low-voltage MOSFET, IRF644, can be used resulting in reduced cost and conduction loss due to its low Rds(on). Hence, the efficiency is much improved.

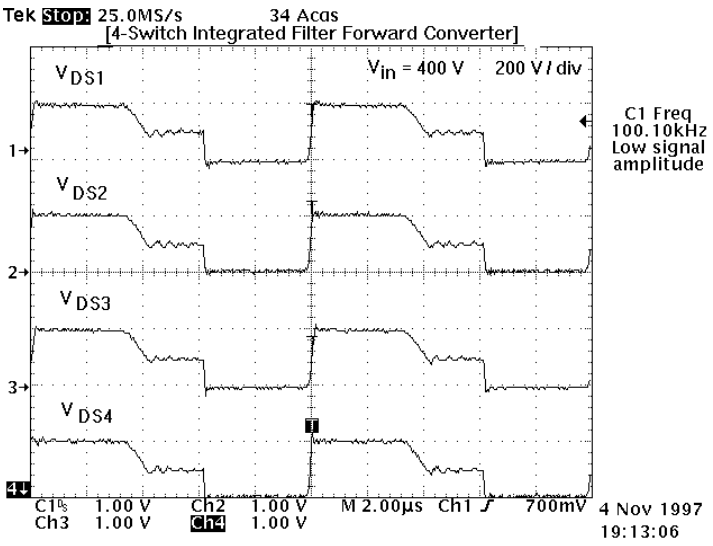


Fig. 4-18 V_{DS} waveforms of the 4S-FRC, each switch is clamped and shared to $V_G/2$..

Moreover, the voltage on the MOSFET is one-quarter of the input voltage before turning on, and the switching turn-on losses are expressed as the following equation.

$$4 \cdot (\frac{1}{2} \cdot C_S \cdot {V_{DS}}^2) = 4 \cdot (\frac{1}{2} \cdot C_s \cdot \left(\frac{1}{4} V_{in}\right)^2) = \frac{1}{4} \cdot \left(\frac{1}{2} \cdot C_s \cdot {V_{in}}^2\right) \cdot \qquad \text{Eq. 4-2}$$

Consequently, the switching turn-on loss is significantly reduced to one-quarter that of a single-switch forward topology.

The clamp capacitor and clamp diode voltage waveforms are shown in Fig. 4-19. Channel 3 illustrates the voltage across the clamp capacitor. By storing and transferring the leakage energy, it becomes a voltage source with a value of one-half the input voltage during the entire switching period. Channel 4 illustrates the voltage across the clamp diodes D_{c1} and D_{c2}. The voltage stress is clamped to the input voltage.

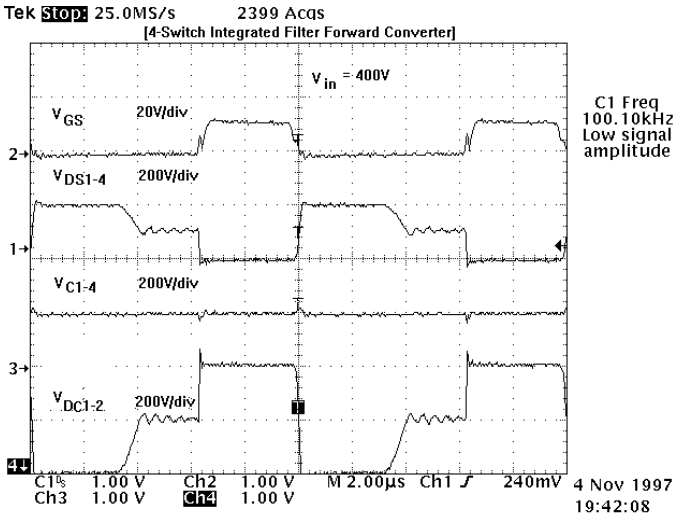


Fig. 4-19 Gate drive signal and voltage waveforms of the 4S-FRC.

As shown in **Fig. 4-20**, the input current I_{in} is 150mA DC with a 75mA current ripple. It is a non-pulsating waveform due to the ripple cancellation mechanism.

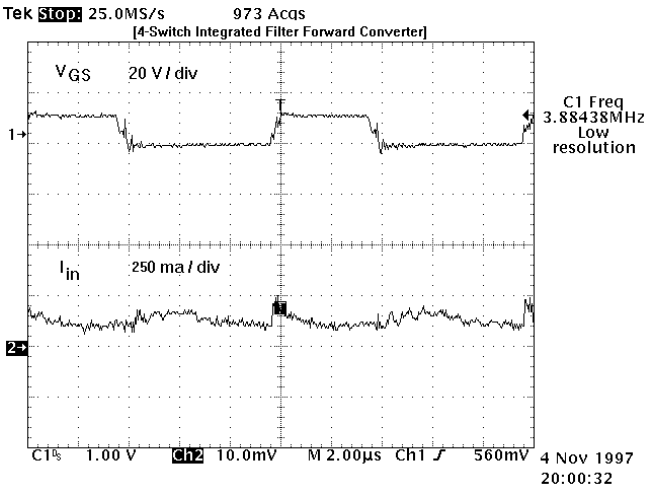


Fig. 4-20 Gate drive signal and input current waveforms of the 4S-FRC.

4.4. Efficiency Improvement by Extending Duty Cycle and Reducing Voltage Stress

The efficiencies of the FRR and FRC have been improved either by extending duty cycle or reducing voltage stress schemes to the converters. Accordingly, further efficiency improvements can be expected by applying both schemes at the same time at the expense of increasing circuit complexity and the cost. However, it is a small price to pay for the benefits obtained for the high-input-voltage and high-output-power applications.

4.4.1. Full-Bridge Converter with Current Ripple Reduction (FBCRR)

Referring to Fig. 4-5, a full-bridge converter with current ripple reduction (FBCRR) is proposed to take advantage of the voltage-clamped function of the PPF for high input input-voltage high output-power applications as shown in Fig. 4-21.

A 270-330V input and 15V output voltages and 300W output power FBCRR operating at 100 kHz was implemented.

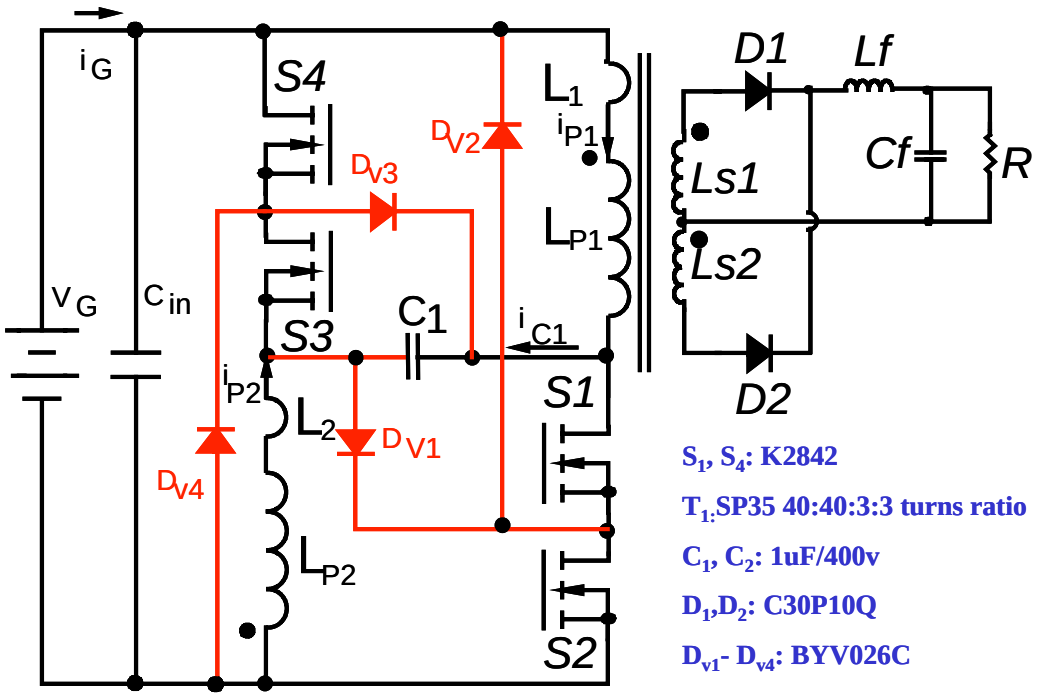


Fig. 4-21 Circuit diagram and key components used in the full-bridge converter with current ripple reduction (FBCRR).

Four extra diodes, D_{V1} ~ D_{V4}, are added to assure voltage sharing between S_1-S_2 and S_3-S_4, and the maximum voltage across each switch is thus limited to V_G.

The transformer was constructed with an SP35 core and 40:40:3:3 turns ratio. The main switches are Toshiba K2842. The rectifier is a C30P10Q. The clamp capacitor and filter capacitor are 1uf. The primary windings use 0.55 ϕ wires and the secondary winding uses 0.1 ϕ * 60 * 3.

Fig. 4-22(a)-(d) show the oscillograms of the prototype converter. All the waveforms were taken for V_{in} = 300V, D=0.42, V_o = 15V, and I_o = 20A. The continuous input current waveform is obtained by the small filter capacitor, C_{in}, as shown in Fig. 4-22 (a).

Fig. 4-22(b) and Fig. 4-22 (c) show that i_{P1} and i_{P3} provide the output load currents with variable percentages in different time intervals.

Fig. 4-22(d) presents the charge balance on the C_1; it is charged during the dead time interval and discharged to the load during the S_1-S_2 or S_3-S_4 turning-on intervals.

As shown in Fig. 4-23 (a) through Fig. 4-23(d), two pairs of main switches (S1-S2 and S3-S4) are alternately turned on and off. However, due to the difference between the driver layout path and the MOSFET's characteristics, they will not be turned off at the same time. Voltage-clamped and voltage-sharing mechanisms are thus required. V_{DS1} and V_{DS2} (V_{DS3} and V_{DS4}) are clamped to the input voltage due to the turning-on of S_3-S_4 (S_3-S_4), and the voltage-sharing function is achieved by turning on D_{V1}-D_{V2} (D_{V3}-D_{V4}). Also, the spike-free voltage waveforms on the on/off transitions confirm that the leakage inductance energy is effectively absorbed.

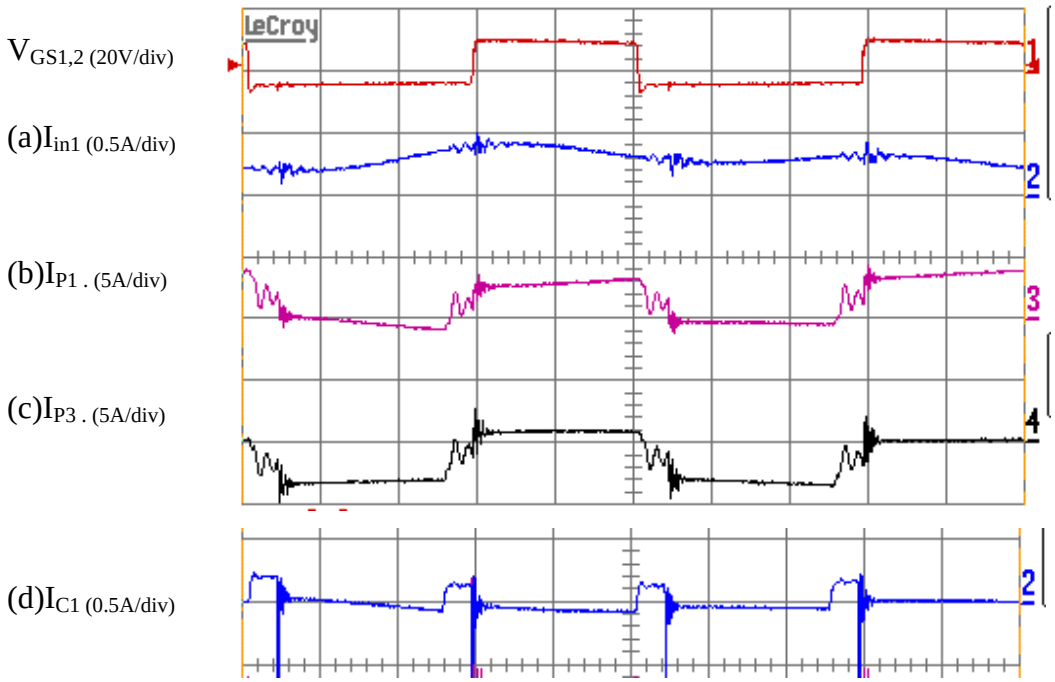


Fig. 4-22 Current waveforms of the power stage of the FBCRR.

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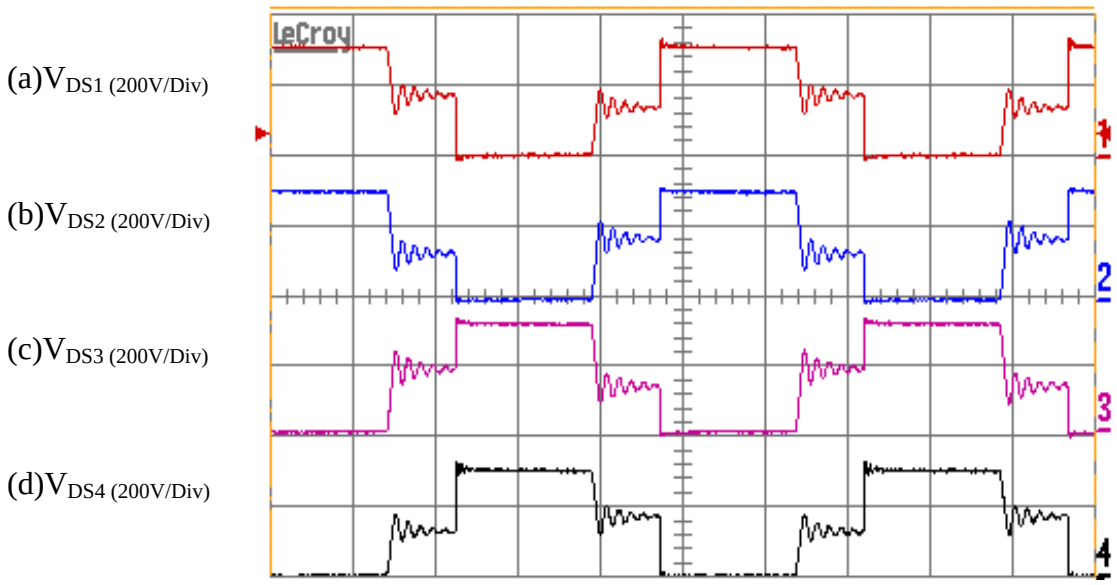

Fig. 4-23 Voltage waveforms of the power stage of the FBCRR

4.4.2. Full-Bridge Converter with Current Ripple Cancellation (FBCRC)

Referring to Fig. 4-8, a full-bridge converter with current ripple cancellation (FBCRC) is proposed to take advantage of the voltage-clamped function of the symmetrical push-pull power converter (SPPPC) for high-input-voltage high-power applications as shown in Fig. 4-24.

A 210W, 270-330V input voltage and 15V output voltage FBCRC operating at 150kHz was constructed. The transformer has a 24:24:24:24:3:3 turns ratio, which means that the effective turns ratio equals 16. The main switches are IRFP350. The rectifier is a 62CNQ45. The clamp capacitors are 2.2uf. The primary windings are AWG #26 wires and the secondary windings are copper foil.

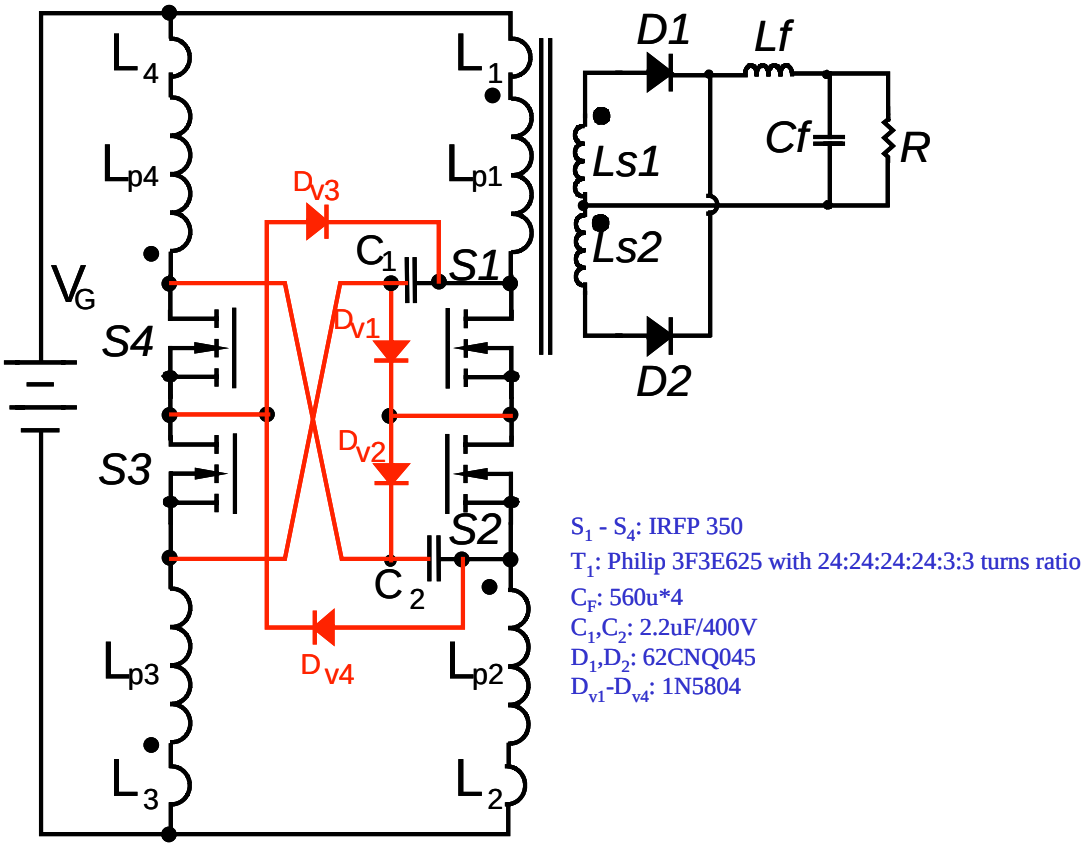

Fig. 4-24 Circuit diagram and key components used in the full-bridge converter with current ripple cancellation (FBCRC).

The oscillograms of the prototype converter are shown in Fig. 4-25 through Fig. 4-27. All the waveforms were taken with V_G = 270V, V_o =15V, and I_o = 14A.

Two pairs of main switches (S_1-S_2 and S_3-S_4) are alternately turned on and off. The spike-free voltage waveforms of the on/off transitions confirm that the leakage inductance is effectively absorbed and clamped. Also, the voltage across each switch is clamped to the input voltage because its individual clamp diode is turned on.

The input current, I_G, is 730mA DC with a 120mA current ripple as shown in Fig. 4-26. Instead of the pulsating shape of the PWM counterpart, it is a non-pulsating waveform due to the current ripple cancellation function.

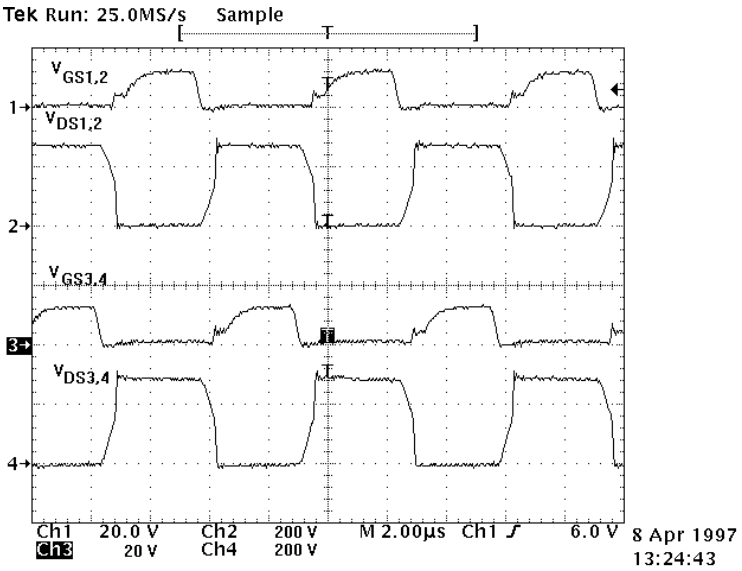

Fig. 4-25 Gate drive signals and V_{DS} of the FBCRC.

During the dead-time period, the voltage across the off-switches varies due to resonance between the leakage inductance and the parasitic capacitances. Fig. 4-27 shows this voltage drops to 148V before the gate signals are applied. Hence, switching losses are reduced and the efficiency is improved.

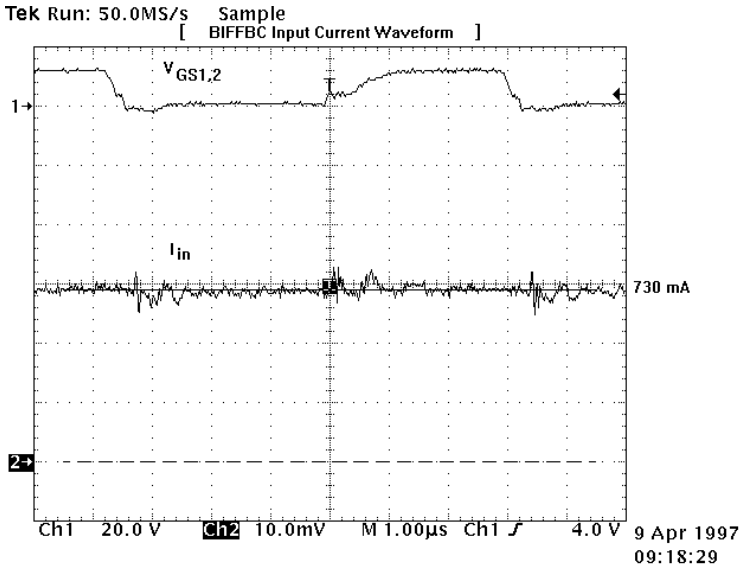

Fig. 4-26 Gate drive signals and the input current waveform of the FBCRC.

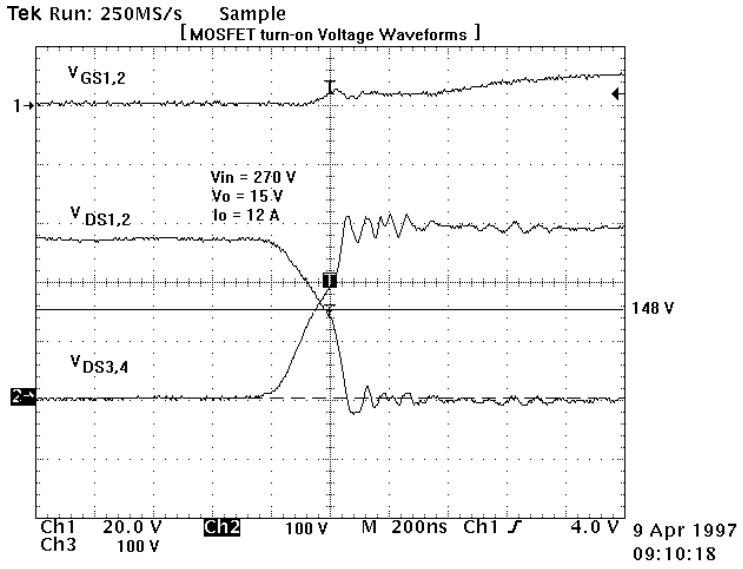

Fig. 4-27 Turn-on voltage waveform of the FBCRC.

4.5. Topology Extensions for Isolated Boost Converters

Those who have proposed PWM forward converters concentrate their efforts on solving some of the inherent problems, such as voltage stress and efficiency performance. However, there is a pulsating input current, and no PWM converter has been claimed to

be able to reduce the current ripple or shape the current waveform into a non-pulsating waveform without adding external LC filter, according to the existing literature.

The FRR and the FRC presented in Chapter 2 and Chapter 3 have been proven to be able to alleviate the problems generated by the pulsating input current.

Besides occurring in the PWM buck-derived converter, the pulsating current occurs at the output port of the PWM boost and its derived isolated converter. Without an effective solution, however, the output filter capacitor is added so that a non-pulsating waveform can be achieved at the output of the isolated boost-derived converter.

According to the existing literature, there is currently no effective solution to reduce the output current ripple of the boost converter without an external LC filter.

A buck converter can be seen as an inverted boost converter **[2]**. Therefore, applying the bilateral inversion technique to the PPF and the SPPPC, the extensions of the isolated boost converters, boost converter with ripple reduction (BCRR), and boost converter with ripple reduction (BCRC), are present.

The bilateral inversion technique is a general topological property in converter circuits. By making all switches bidirectional, i.e., adding an anti-parallel diode to a transistor and vice versa, the converter can be made to process the power bilaterally. A detailed discussion on the bilateral inversion and extension of this technique can be found in **[2]**.

Fig. 4-28(a) shows the PPF. By adding diodes D_1 and D_2 to switches S_1 and S_2 and switches S_3 and S_4 to diodes, D_3 and D_4, the circuit now becomes a bilateral converter, which can transfer power either from left to right or right to left, as shown in Fig. 4-28(b). When the switch-diode sets of S_1-D_3 and S_2-D_4 are activated, the circuit degenerates into

the push-pull forward converter, and power flow is from left to right. When the switch-diode sets of S_3-D_1 and S_4-D_2 are activated, the circuit degenerates into the current-fed push-pull converter with ripple reduction, and power flow is from right to left, as shown in Fig. 4-28(c). It is an isolated boost converter, one of the extensions of the current-fed push-pull converter. Since the input current is restricted by the input inductor, it allows the overlapping conduction of S_1 and S_2. Some circuit variations of the current-fed converters and their operation can be found in [78] - [82].

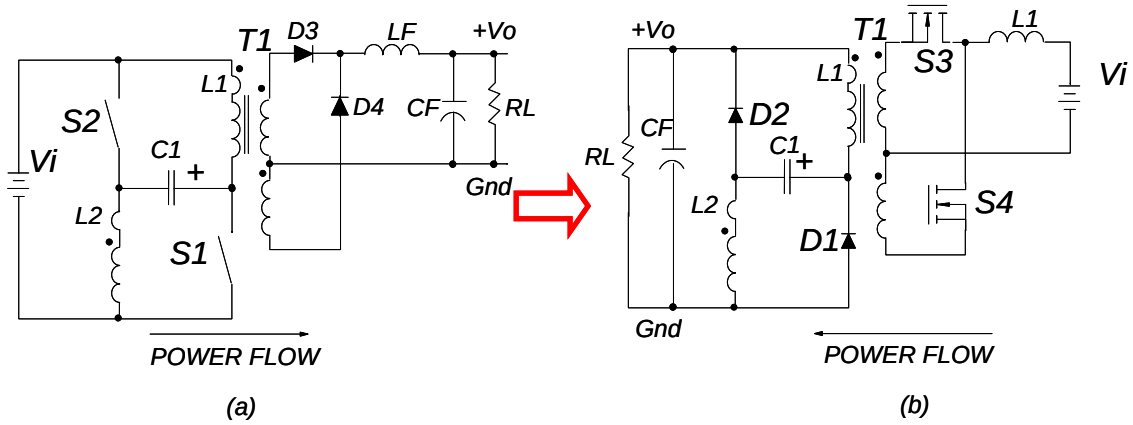

Fig. 4-28 Circuit diagrams of (a) the PPF, (b) bilateral inversion of the PPF.

The circuit diagram and the key waveforms of the BCRR as illustrated in Fig. 4-29.

Due to the leakage energy bing stored in the clamp capacitor and then transferred to the load, the secondary rectifier diodes are free of voltage spikes and clamped to 2Vo. With the help of the clamp capacitor, the output current ripple is reduced and reduction of the output capacitor can be achieved. It is suitable for the high-output-voltage applications.

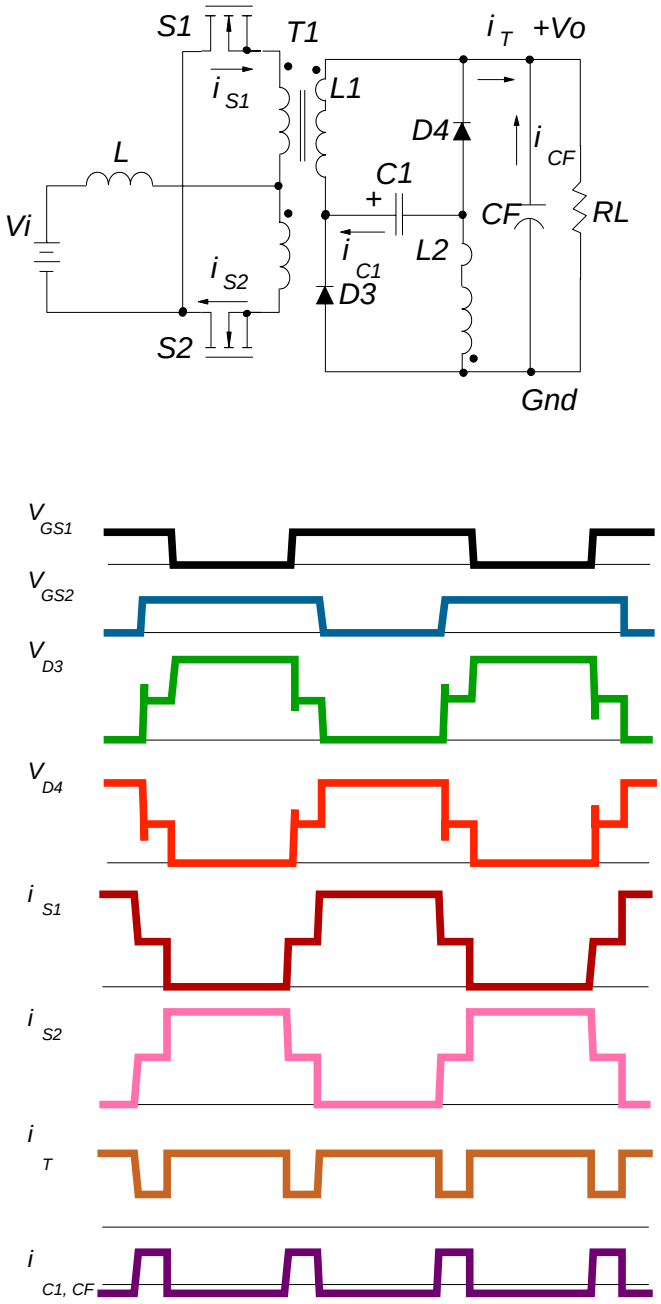

Fig. 4-29 Circuit diagram and key waveforms of the boost converter with ripple reduction (BCRR).

Again, by employing the bilateral inversion technique to the SPPPC, the boost converter with ripple cancellation is presented. The circuit diagram and the key waveforms of the boost converter with ripple cancellation as illustrated in the Fig. 4-30.

Due to the leakage energy being stored in the clamp capacitor and transferred to the load, the secondary rectifier diodes are free of voltage spikes and clamped to 2Vo. With the help of the output current ripple cancellation, the output current becomes continuous waveforms, and the output capacitor can be significantly reduced. This is suitable for the high-output-voltage applications.

4.6. Summary

Employing the proposed techniques, the FRR and the FRC presented in Chapter 2 and Chapter 3 illustrate some advantages over the FAC. Not only do they have a minimum component count, but also they recycle the transformer leakage inductance energy. Moreover, the alleviation of the EMI intensity results in size reduction of the EMI filter..

However, both converters are inferior to the FAC in terms of efficiency. The reduction of the semiconductor devices' conduction losses is found to be the key factor for improving efficiency. Consequently, extending the operating duty cycle and use of the series-connecting semiconductor devices techniques are applied to reach this goal. The former scheme can reduce the I_{RMS} and the diode voltage stress while the latter scheme can reduce the equivalent $R_{DS(on)}$ by series-connected low-voltage-rating MOSFETs. In addition to the conduction loss, the switching turn-on loss can also be reduced by the latter scheme. Six topology extensions, XFRR, 2S-FRR, 2S-FRC, 4S-FRC, FBCRR, and FBCRC are proposed.

In addition, the experimental results verify that the efficiency of these proposed converters are improved due to the reduction of the conduction losses and/or switching loss.

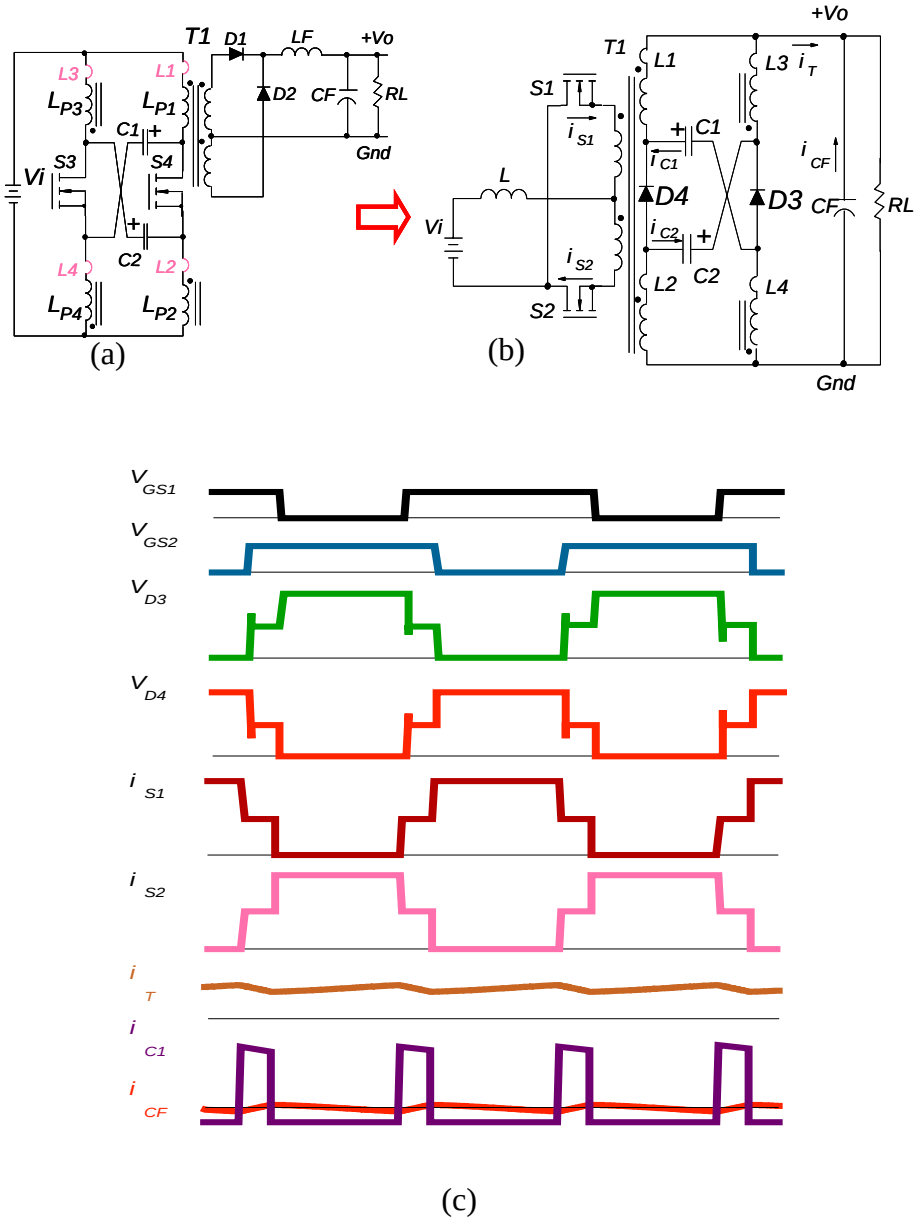

Fig. 4-30 (a) Circuit diagram of the SPPPC, (b) the circuit diagram and (c) key waveforms of the boost converter with ripple cancellation (BCRC).

Moreover, the ripple reduction and the embedded filter techniques are applied to alleviate the output current ripple of the isolated boost converter without using an

external LC filter. By employing the bilateral inversion technique, a boost converter with ripple reduction and a boost converter with ripple cancellation are presented. Having no voltage spikes on the rectifier diode and size reduction of the output filter capacitor is possible. These two converters are suitable for high-output-voltage applications.

Chapter 5 Conclusions and Future Works

This chapter summarizes the entire dissertation and offers some suggestions for future works.

5.1. Conclusions

This dissertation is engaged in exploring an effective solution to enhance the PWM converters performance. Five forward converters with different reset schemes are evaluated as the beginning of this research. In addition to voltage stress and converter efficiency, valuable information with respect to the leakage inductance is obtained from this evaluation.

With a resonant power conversion technique, such as the MRC, the circuit requires inductance and capacitance so that the leakage inductance of the transformer can enhance rather than detract from circuit performance.

In contrast, the leakage inductance energy is either dissipated in the RCD or recycled to the input source in the FAC. Consequently, the leakage inductance is intentionally minimized in the PWM power conversion technique so that it will not degrade the circuit performance.

To date, however, no single-switch forward converter has been claimed to be able to enhance the converter performance in the PWM power conversion technique by utilizing the leakage inductance. In contrast with the MRC, research on the utilization of the transformer's leakage inductance in the PWM forward converter has been needed.

Two techniques, input current ripple reduction and an embedded filter, are thus proposed and the performance of a forward converter using the PWM technique can be enhanced.

By inserting a capacitor between the two primary windings of the TFC, a forward converter with ripple reduction (FRR) is presented in this research work. Due to the fact that the voltage of the capacitor is clamped to input voltage both at the static and dynamic states, the excessive voltage stress on the main switch S_1 of the FAC during low-line to high-line step transient is eliminated.

Moreover, the FRR is like a two-input-source, V_G and V_{C1}, forward converter. Accompanied by the transformer leakage inductance, the reduction of the current ripple of the input voltage can be achieved. Furthermore, without an external LC filter, the EMI noise levels can be further reduced as the result of the embedded notch filter formed by the transformer leakage inductance and clamp capacitor if the notch frequency is designed to be at the switching frequency. With the help of the clamp capacitor, therefore, the leakage inductance can enhance rather than detract from the converter performance.

Reduction in the current ripple can be achieved by employing the proposed techniques. Two sets of the clamp capacitors and the leakage inductances are utilized, and the current ripple can even be cancelled if the necessary conditions are met. Consequently, input current becomes a non-pulsating waveform and a forward converter with ripple cancellation (FRC) is presented. Moreover, without an external LC filter, the EMI noise levels can be further attenuated as the result of the embedded low-pass filter formed by the transformer leakage inductances and clamp capacitors.

Again, the leakage inductance can enhance the converter performance just like the resonant converter.

In addition to providing the analysis and design procedure, the performance of the presented converters, the FRR and the FRC, are verified with the experimental results.

By employing the proposed techniques, eight new topologies have been extended for different power conversion applications. Each member of the FRR and the FRC families is able to enhance the converter performances such as the elimination of the voltage spikes on the main switch without snubber circuit and the improvement of EMI performance with small filter components. Consequently, the cost and the space of the converter can be saved.

The major accomplishments and conclusions are summarized below.

1. The excessive voltage stress, V_{DS}, of the FAC during the large signal transient has been reduced.

   By employing capacitor voltage clamp technique, the FRR is presented in this research work. Due to its voltage clamp to the input voltage, the voltage stress on the main switch of the FAC during the large signal transient has been reduced.

2. To reduce the pulsating input current ripple of the forward converter.

   By employing the current ripple reduction technique, the pulsating input current ripple as well as the EMI noise levels of the forward converter has been reduced. Consequently, some of the limited space and the cost used by the external LC filter can be saved. Also, the temperature rise in the filter capacitor due to a larger RMS current is alleviated.

3. To achieve a non-pulsating input current ripple of the forward converter without an external LC filter.

   To take proper advantage of the proposed techniques, the pulsating input current ripple of the forward converter has been cancelled without an external LC filter. As a result, further size reduction of the differential mode EMI filter components is achieved

4. To extend the power converter topology for different power conversion applications.

   Since the pulsating current occurs at the input port of the PWM buck and buck-derived converter, it would be important, therefore, to employ the proposed techniques to extend power converter topology for different applications. Eight new topologies, the XFRR, 2S-FRR, 2S-FRC, 4S-FRC, FBCRR, FBCRC, BCRR, and BCRC, have been proposed for different power conversion applications.

   Moreover, two e existing topologies, the push-pull forward converter (PPF) and the symmetrical push-pull power converter (SPPPC), have been proven to be members of the FRR and FRC families. Consequently, the converter characteristic can be fully understood.

In conclusion, this dissertation has proposed several new PWM topologies for different power conversion applications. All have been proposed according to apply the following techniques.

1. Input current ripple reduction;
2. Embedded filter.

Throughout the entire dissertation, these two techniques are interconnected by utilizing leakage inductance and the clamp capacitor to enhance converter performance using the PWM power conversion technique.

Like the resonant converter, the PWM technique can enhance rather than detract from the circuit performance by utilizing the leakage inductance.

As a result, the construction of the transformer becomes less complicated, a snubber circuit is not needed, and smaller filter components can be used to meet EMI regulations with the PWM power conversion technique.

Finally, the family tree of the FRR and FRC are illustrated in Fig. 5-1 and Fig. 5-2 to show that the proposed techniques have the potential capability to extend to different power applications.

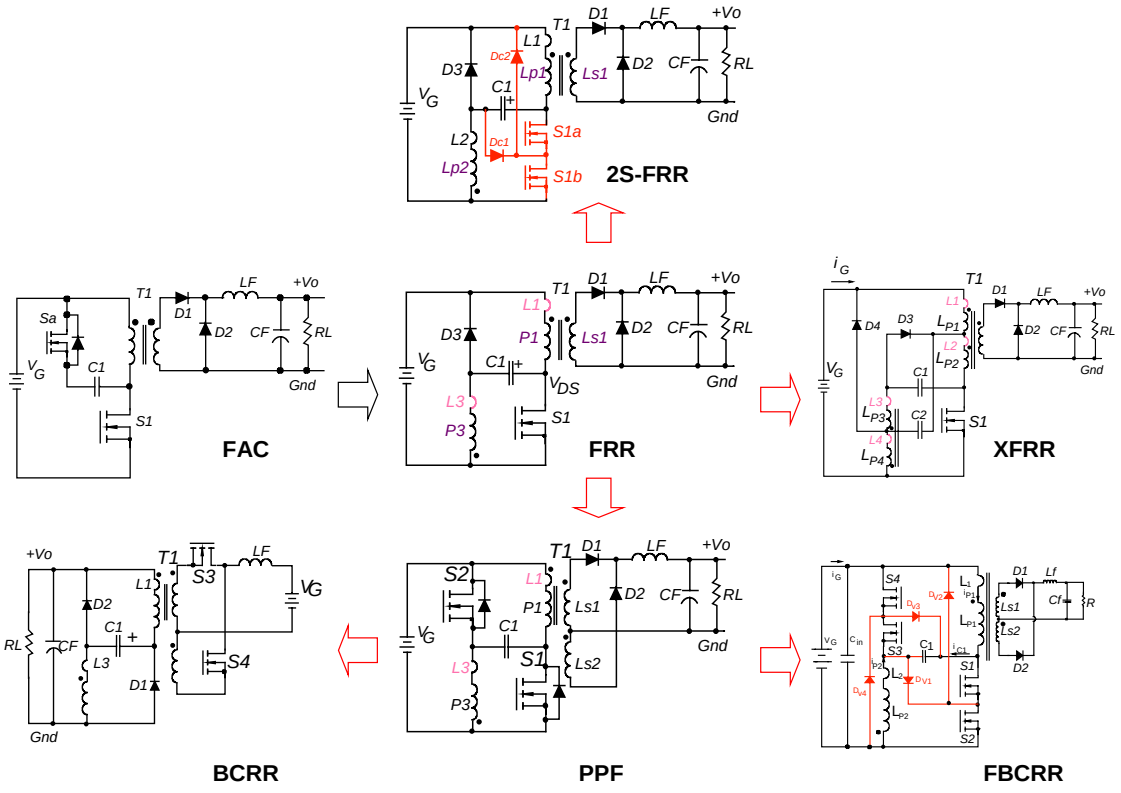

Fig. 5-1 Circuit diagrams of the FAC and the family tree of the FRR.

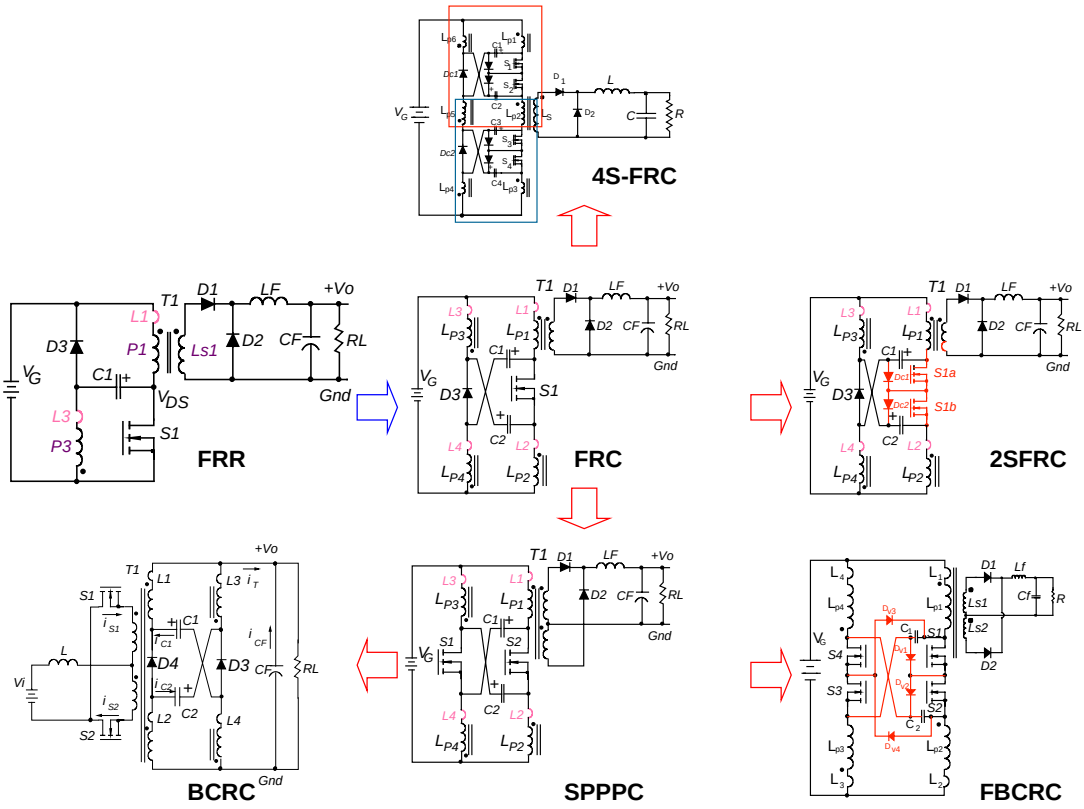

Fig. 5-2 Circuit diagrams of the FRR and the family tree of the FRC.

5.2. Future Works

Without an external LC filter, the leakage inductance of the transformer and the clamp capacitor are utilized and performance enhancement of the PWM forward converter can be achieved. This work provides a systematic basis for further studies and can be carried out in the following directions.

1. Based on the proposed voltage clamp of the capacitor and pulsating input current ripple distribution properties of the leakage inductance, the topologies can be further extended for different power conversion applications.

2. Topology synthesis can be obtained by utilizing the existing filter configuration and the available power converters.

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